Fabrication and characterization of silicon nanowires for devices applications compatible with low temperature ($\leq$300 °C) flexible substrates

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Résumé du mémoire de thèse intitulé

Fabrication and characterization of silicon nanowires for devices applications compatible with low temperature (<300°C) flexible substrates

Fabrication et caractérisation de nanofils de silicium pour des applications électroniques compatibles sur substrats flexibles basse temperature (<300°C)

de
Mr Kai Yang
En vue de l'obtention du Doctorat de l'université de Rennes 1
Mention Electronique

1. Introduction

L'objectif de la thèse est la mise au point des procédés de synthèse de nanofils de silicium en technologie basse température (≤ 300°C) compatibles avec des substrats flexibles bas côuts. Deux approches ont été abordées dans ce travail:

- la réalisation de nanofils de silicium en technologie planaire à partir de la méthode des espaceurs (approche top down),
- la synthèse de nanofils de silicium 3D par procédé SLS (Solide Liquide Solide) (approche bottom up)

2. Synthèse de nanofils de silicium par le méthode des espaceurs

2. 1 Principe de la méthode des espaceurs

Une couche structurelle (dioxyde de silicium - SiO_2) est d'abord déposée sur un substrat (silicium, verre ou plastique), puis gravée par plasma pour former des pavés aux parois verticales. Ensuite, une couche de matériau fonctionnel (silicium par exemple) utilisée pour la fabrication des nanofils est déposée puis gravée par gravure plasma anisotrope. Après gravure de cette couche, grâce à l'excès d'épaisseur au niveau des parois verticales, des résidus (ou espaceurs) apparaissent. Pour une épaisseur de la couche structurelle de 100nm, ces espaceurs peuvent être considérés comme des nanofils (figure 1).

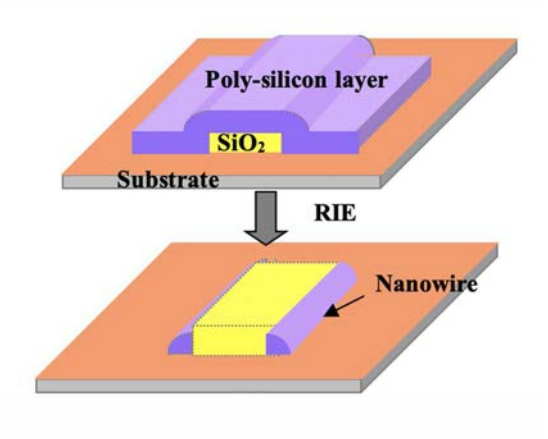


Fig. 1. Illustration de la formation des nanofils par la méthode des espaceurs

La faisabilité des tels nanofils de silicium a été explorée à partir de deux technologies de dépôts chimique en phase vapeur CVD (Chemical Vapor Deposition) : le dépôt classique assisté par plasma (plasma enhanced – PECVD), et le dépôt plasma par couplage inductif (inductively coupled plasma - ICP CVD), ce dernier permettant le dépôt de couches minces à partir d'un plasma très dense. Ces deux procédés permettent des dépôts à basse temperature (<300°C) compatibles avec des substrats plastiques bon marché.

La faisabilité des nanofils par cette méthode, repose d'une part sur la maîtrise de la gravure de la couche structurelle de SiO_2 pour l'obtention d'une bonne verticalité des parois latérales, et d'autre part sur le contrôle de la gravure plasma de la couche mince de silicium, notamment de la detection de fin de gravure.

2. 2 Résultats expérimentaux

2. 2. 1 Optimisation de la gravure de la couche structurelle (SiO_2)

Des études de gravure par plasma réactif (Reactive Ion Etching – RIE) ont été menées en fonction de la pression et de la puissance du plasma.

Des marches d'oxyde structurel aux parois verticales ont été obtenues pour des couches déposées par PECVD à une pression de plasma de 4 mtorr (sous gaz CF4) à une puissance de travail de 50W. (voir tableau 1).

Tableau 1. Paramètres de gravure optimisés de la couche structurelle

	Après
Puissance RF	50W

Flux gaz	CF_4, 30sccm
Pression	4mTorr
Épaisseur de SiO_2	~172nm
Vitesse de gravure	~17.6 nm/min

Les images SEM (Scanning Electron Microscopy) obtenues par microscopie électronique à balayage reportées sur la figure 2 montrent une bonne verticalité des parois de la couche de SiO_2 pour les conditions de gravure optimisées.

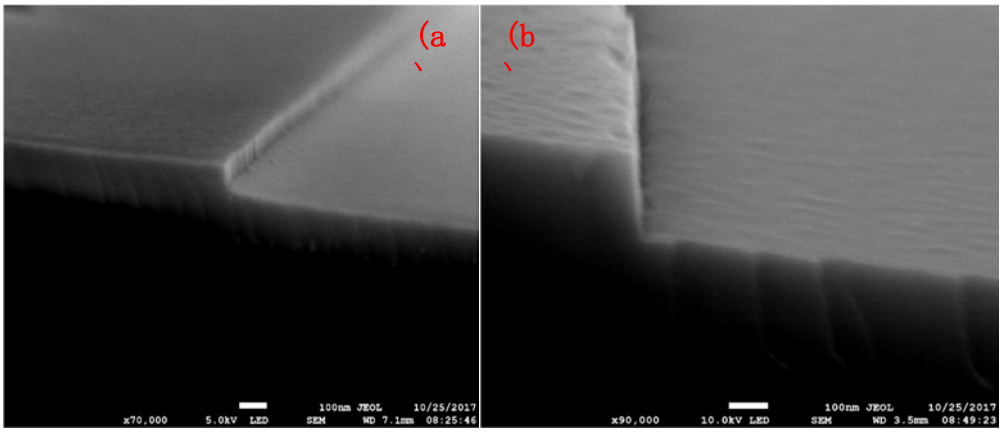


Fig. 2 : Images SEM des marches de SiO_2 après (a) 5 minutes; (b) après 10 minutes de gravure plasma RIE.

2. 2. 2 Optimisation de la gravure la couche fonctionnelle (silicium microcristallin)

Dans la suite du travail, la gravure de la couche fonctionnelle en silicium microcristallin, déposée soit par procédé PECVD soit ICP CVD, a été étudiée en fonction de la puissance et de la pression du plasma. Pour les couches de silicium déposées par le procédé PECVD il n'a pas été possible de réaliser des nanofils-espaceurs (lié à un problème de contrôle de gravure). En revanche, la faisabilité de nanofils a été démontrée lorsque la couche fonctionnelle de silicium microcristallin a été déposée par ICP CVD à 180°C pour une pression du plasma (sous gaz SF6) de 30W et une pression de 5mtorr (Fig. 3 et 4). Toutefois, la reproductibilité n'est pas satisfaisante. Des études complémentaires sur les paramètres de dépôts et de gravure de la couche de silicium sont nécessaires afin d'optimiser le procédé de fabrication.

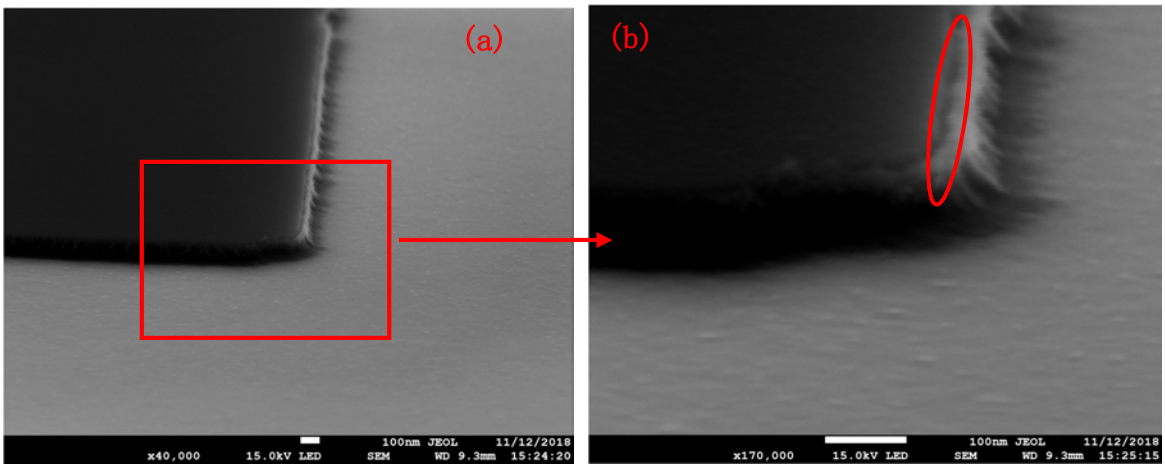


Fig. 3 : Image SEM montrant les espaceurs le long de la marche d'oxyde structurel après gravure optimisée de la couche de silicium microcristallin déposée par procédé ICP CVD.

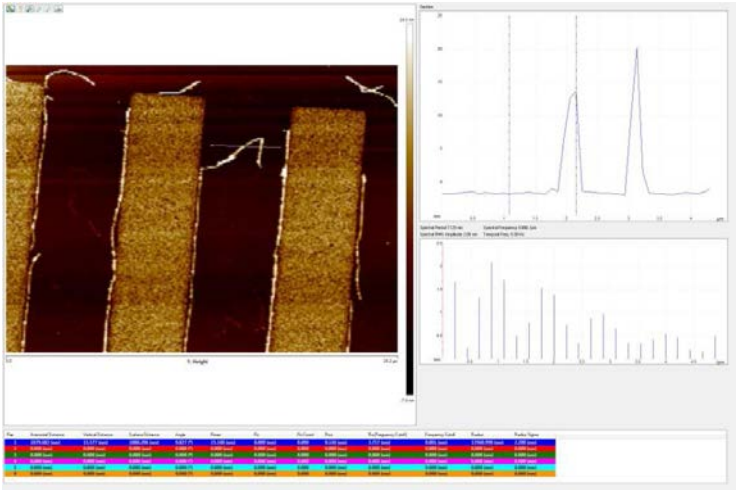
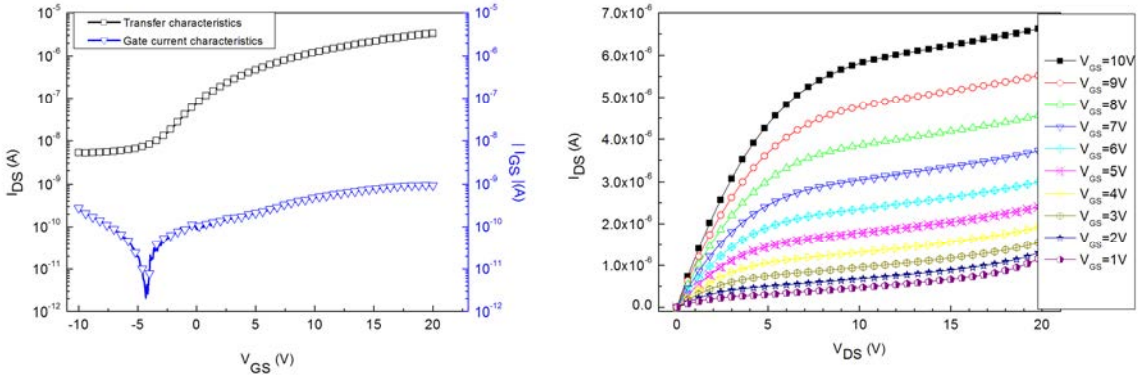


Fig. 4 : Image AFM révélant le relief des nanofils après gravure partielle (par voie humide) de la marche d'oxyde structurel.

2. 2. 3 Qualité électrique de dioxyde de silicium et fabrication de TFTs obtenus par ICP CVD

Parallèlement des études d'isolation électrique des couches dioxyde de silicium, ainsi que la réalisation de transistors à effet de champ en couches minces (ou TFTs pour Thin Film Transistors) ont été démontrées (fig. 5) en utilisant la technologie de dépôt par plasma ICP CVD. De plus, un protocole de caractérisation de la technologie de fabrication par l'extraction de la densité des états d'interface a été établi (fig. 6).



(a) (b)

Fig. : 5 (a) Caractéristique de transfert , (b) caractéristiques de sortie des transistors en couche de silcium microcristallin réalisés en technologie ICP CVD

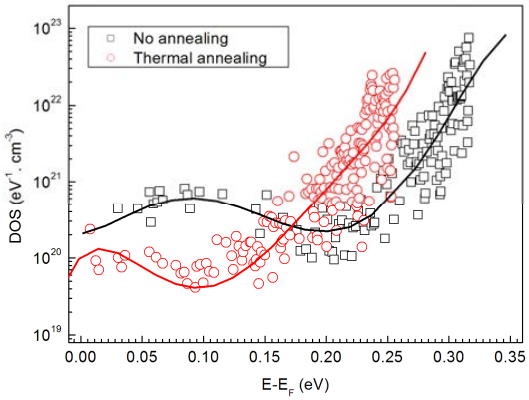


Fig 6 : Distribution des états d'interface pour des transistors en couches minces (non recuits et recuits à 220°C pendant 2h)

3. Synthèse des nanofils de silicium par procédé Solid Liquide Solide (SLS)

3. 1 Principe

La synthèse de nanofils de silicium 3D par procédé SLS (Solide Liquide Solide) repose sur la croissance de nanofils à partir d'un catalyseur métallique (nickel, aluminium…) sous forme de nano-droplets en phase liquide. Le croissance des nanofils se fait à partir d'un substrat de silicium en phase solide (fig. 7).

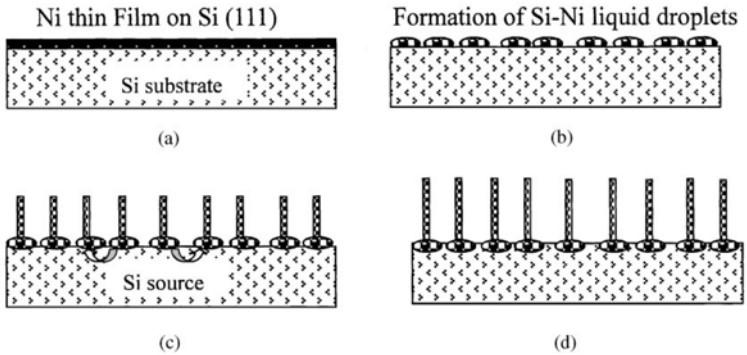
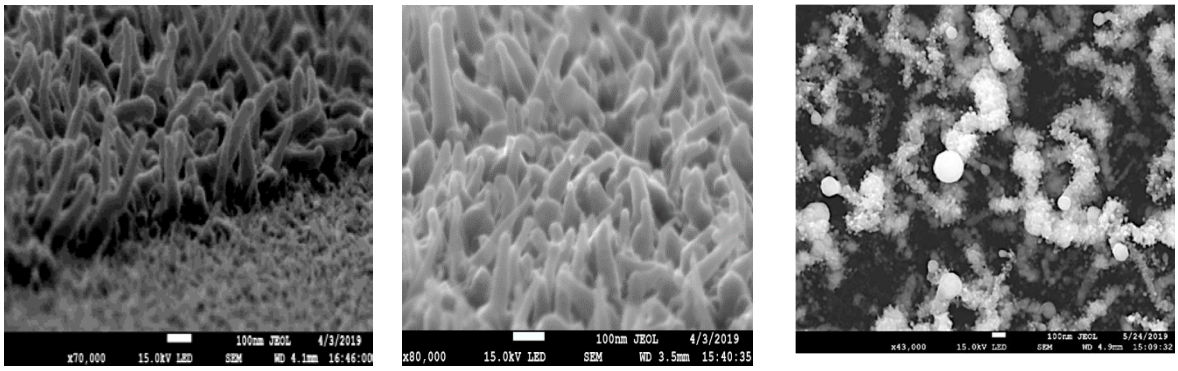


Fig. 7 : Schéma de principe de la croissance SLS 3D de nanofils de silicium par proceed SLS utilisant le nickel comme catalyseur

3. 2 Résultats expérimentaux

La synthèse de nanofils de silicium 3D par procédé SLS (Solide Liquide Solide) à partir de substrats de silicium (monocristallin ou couche mince de silicium amorphe), utilisant l'indium comme catalyseur a été démontrée. La croissance des nanofils est obtenue sous plasma hydrogène. Des études ont été menées en fonction de l'épaisseur d'indium déposée, de la durée et de la température du plasma d'hydrogène. Les résultats ont mis évidence une croissance de réseaux de nanofils à parois lisses (diamètre 100nm, longueur 500 nm) pour une durée de 30 min de plasma d'hydrogène à 250°C, à partir d'une épaisseur d'indium de 20 nm (fig. 8. (a) et (b)). La croissance de nanofils pour des durées de plasma d'hydrogène et d'épaisseurs d'indium supérieures a conduit à la synthèse de nanofils de diamètre plus important, aux parois rugueuses laissant apparaître un début de croissance secondaire de nanofils sur ces mêmes parois, probablement due à la présence de résidus d'indium (fig. 8(c)).



(a) (b) (c)

Fig. 8 : Nanofils de silicium obtenus par synthèse SLS à 250°C sous plasma d'hydrogène, (a) pendant 30 min sur substrat silicium monocristallin, (b) pendant 30 min sur couche mince de silicium amorphe, (c) pendant 60 min sur couche mince de silicium amorphe

4. Conclusion

La faisabilité des nanofils de silicium dans une technologie basse température (<300°C) compatible avec des substrats flexibles faibles coûts (plastiques) a été étudiée suivant deux approches.

La méthode des espaceurs a permis de mettre en évidence la fabrication de nanofils de silicium en utilisant le procédé de dépôt ICP CVD avec une température de dépôt maximale (180°C). Toutefois, cette approche ne permet pas d'avoir une bonne reproductibilité de réalisation. Parallèlement, ces travaux ont aussi permis de démontrer la faisabilité de transistors en couches minces par la technologie ICP CVD.

La synthèse 3D de nanofils de silicium par procédé SLS utilisant l'indium comme catalyseur sous plasma d'hydrogène à une température de 250°C a été démontrée. Des nanofils de 500 nm de longueur et de 100 nm de diamètre ont été obtenus pour une durée de croissance de 30 min. Notons

que la croissance SLS de nanofils de silicium à partir de catalyseurs métalliques n'avait été jusqu'alors observée qu'à des températures bien supérieures (>450°C).

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List of abbreviations

AC/DC: Alternating Current/Direct Current

AFM: Atom Force Microscope

AI-IC: Aluminum Induced Crystallization

APCVD: Atmospheric Pressure Chemical Vapor Deposition

Au-IC: Gold Induced Crystallization

BJT: Bipolar Junction Transistor

BLA: Blue Laser Annealing

C-beam: Carbon nanotube electron beam

CF_4: *Tetrafluoromethane*

CMOS: Complementary Metal-Oxide-Semiconductor

CNTs: Carbon Nanotubes

C-V: Capacitance Voltage

CVD: Chemical Vapor Deposition

CW: Continuous Wave

DOS: Density of States

EBL: Electron Beam Lithography

EDP: Electron Diffraction Pattern

ELA/ELC: Excimer Laser Annealing/Crystallization

EPD: Electrophoretic Deposition

FG: Forming Gas

FLA: Flash Lamp Annealing

FWHM: Full Width at Half Maximum

HFCV: High Frequency Capacitance Voltage

ICP-CVD: Inductively Coupled Plasma Chemical Vapor Deposition

IPSLS: In-Plane Solid-Liquid-Solid

ITO: Indium Tin Oxide

LF: Low Frequency

LFCV: Low Frequency Capacitance Voltage

LPC/LAC: Laser Phase Crsytallization/Laser Annealing Crystallization

LPCVD: Low Pressure Chemical Vapor Deposition

MEMS: Micro-Electro-Mechanical System

MIC: Metal Induced Crystallization

MILC: Metal Induced Lateral Crystallization

MIS: Metal-Insulator-Semiconductor

MOS: Metal-Oxide-Semiconductor

MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor

NIL: Nanoimprint Lithography

N_{SS}: Energy distribution of surface state density

PEN: Polyethylene Naphthalate

PET: Polyethylene Terephthalate

PH_4: Phosphine

PI: Polyimide

PIC: Plasma Induced Crystallization

Q_{SS}: Surface Charge Density

RF: Radio Frequency

RIE: Reactive Ion Etching

SEM: Scanning Electron Microscope

SF_6: Sulfur hexafluoride

SiH_4: Silane

SiNWs: Silicon Nanowires

SLS: Solid-Liquid-Solid

Sn-IC: Tin Induced Crystallization

SOI: Silicon on Insulator

SPC: Solid Phase Crystallization

SSLPE: Steady State Liquid Phase Epitaxy

TEM: Transmission Electron Microscope

TFT: Thin Film Transistor

VLS: Vapor-Liquid-Solid

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Obviously, the thesis is for my parents and other family members. Here I would like to pray for my grandfather who is currently under bad health condition, really wish he will be restored form the disease.

General introduction

Semiconductor industry has seen an enormous development for last four decades. Along with the boom of the whole industry, silicon played the most important role. From BJT (Bipolar Junction Transistor), MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) to TFT (Thin Film Transistor), silicon has been the solid foundation of these most frequently researched and used electronic devices. Even silicon has been researched since the very beginning of semiconductor industry, it is still the one of the most competitive semiconductor materials which has more potential to be explored.

When the world entered into the second decade of 21st century, some new applications such as flexible displays, wearable electronic devices and other flexible electronics have emerged. Although silicon technology is still the prior solution in most cases, the request for low temperature compatible with silicon technologies is more and more urgent. Conventional silicon technologies such as thermal oxidation, APCVD (Atmospheric Pressure Chemical Vapor Deposition) and LPCVD (Low Pressure CVD) are processed at least at 420 ˚C, temperature which is not compatible with most of the low cost and low temperature flexible substrates, like PI (polyimide) and PEN (polyethylene naphthalate) substrates.

In most cases, the highest process temperature would occur during the film deposition in silicon involved technological processes. A deposition technique with much lower temperature is then required. Unlike the conventional APCVD or LPCVD, plasma assisted CVD is the better choice. In order to develop the proper silicon technology on flexible substrates, the first goal of this thesis is to develop the silicon related technology at the temperature lower than 300˚C. Therefore, the PECVD (Plasma Enhanced-CVD) and ICP-CVD (Inductively Coupled Plasma-CVD) technologies are introduced and explored due to their very low temperature deposition (≤200 ˚C), for silicon films as key part for the formation of electronic devices at low temperature.

On the other hand, many techniques developed in nanotechnology allow us to produce various forms of structures such as nanotubes, nanoparticles and especially nanowires, which open the way for the manufacture of electronic devices with innovative electronic properties. These properties specific to semiconductor nano-objects used as active elements in electronic devices suggest their great potential for new applications in many fields (chemistry, biology, mechanics…). However, the vast majority of nano-objects are manufactured at temperatures that are not compatible with flexible substrates. We have undertaken research in this thesis to find a technical way to manufacture nano-objects at temperatures compatible with flexible substrates.

Silicon nanowires (SiNWs) can be categorized into two types based on the synthesis approach: top-down and bottom-up. These two approaches mainly focus on whether the nanowires are implemented by performing the photolithography on stacked layers or are synthesized from the substrate with the help of precursors. In this thesis, both approaches are discussed. All the approaches are of course implemented at low temperature (≤300 ˚C).

This manuscript consists of four main chapters.

In chapter 1, different deposition techniques are firstly reviewed. Unlike the deposition techniques compatible with low temperature process, traditional techniques such as APCVD and LPCVD are no longer suitable. Sputtering, hot-wire CVD and PECVD are all possible low temperature alternatives. The system setup, deposition parameters and properties of deposited films would be discussed. Unfortunately, silicon deposited by using these low temperature techniques mentioned above usually suffers from poor electrical properties. Therefore, proper crystallization is necessary in this case but should be performed at low temperature just as same as deposition. Metal induced crystallization (MIC), ELA (Excimer Laser Annealing), hydrogen plasma induced crystallization, C-beam (Carbon nanotube electron beam) crystallization and BLA (Blue Laser Annealing) will be reviewed since they also provide interesting alternatives to well crystallize amorphous silicon compatible with low temperature substrates.

In chapter 2, a possible path that has not yet been explored in the literature is the use of ICP-CVD, which is the key process to research. Unlike the other deposition techniques like LPCVD, PECVD, etc., ICP-CVD can offer several advantages such as higher density of plasma during the deposition and good homogeneous of deposited layers and lower process temperature. These advantages enable the possibility of depositing high quality thin film under relatively low temperature. Although ICP-CVD has been adopted as one of the deposition techniques in this thesis, the characteristics of these films need to be more explored and optimized. As a good candidate for gate insulator in MOS (metal-oxide-semiconductor) transistors, SiO_2 has been widely studied under different CVD techniques. Since there are several advantages of ICP-CVD compared to the other CVD techniques, the electrical properties of ICP-CVD deposited SiO_2 should also be investigated. Therefore, in this chapter, we firstly fabricated ICP-CVD MOS capacitors based on SiO_2 by modifying several key deposition parameters to evaluate and thus to optimize the SiO_2 deposition. Then, ICP-CVD TFTs were accordingly fabricated to characterize electrical properties of the ICP-CVD silicon layer and to complete the electrical characterization on ICP-CVD SiO_2.

In chapter 3, experiments were carried out to develop a process for manufacturing silicon nanowires using the top-down method, at temperatures compatible with flexible substrates. Unlike the other top-down approaches with EBL (Electron Beam Lithography) involved, spacer method classically used in sub-micron technology could be implemented only by using conventional photolithography and RIE (Reactive Ion Etching). The deposition of material layer, etching of material steps and active layers are optimized and characterized by SEM.

In chapter 4, as in the frame of low temperature process research, the crystallization should be carried out at the temperature lower than 300 ˚C. Under this circumstance, we decided to investigate the metal catalyzed silicon nanowire growth by using indium thanks to its lower eutectic temperature (~157 ˚C). First, the thermal evaporation of indium will be presented in terms of morphology of evaporated indium layers. Different conditions were set up to mainly study how different thicknesses of indium layers would look like under SEM and AFM (Atomic Force Microscope) characterizations. The research on indium catalyzed silicon nanowire growth will be carried out afterwards.

In the end, we will conclude on all the work done and the perspectives will provide possible ways for improvement.

Chapter 1

State of the art of low temperature deposition and crystallization techniques

1.1 Introduction

Low temperature semiconductor technology has been intensively researched over the last two decades since the increasing demand of the bent displays, wearable electronics and other flexible electronics both in our daily lives and more specific domains. To realize all these devices and thus corresponding applications, temperature as low as 300 ˚C is considered the highest process temperature because most researched plastic substrates such as PET (Polyethylene terephthalate), PEN (Polyethylene naphthalate) and PI (Polyimide) are unlikely to survive at 300˚C (PI is generally more thermally stable when temperature is lower than 350 ˚C) [1].

When we consider the essential process to fabricate electronic devices like photolithography, deposition and etching, the only process requiring the highest temperature is deposition. Hence, we firstly review different deposition techniques. Unlike the deposition techniques compatible with low temperature process, traditional techniques such as APCVD (Atmospheric Pressure Chemical Vapor Deposition) and LPCVD (Low Pressure CVD) are no longer suitable. Sputtering, hot-wire CVD and PECVD are all possible low temperature alternatives. The system setup, deposition parameters and properties of deposited films would be discussed in section 1.2.

It is still not the end of the story if we only talk about the deposition because silicon deposited by using these low temperature techniques mentioned above usually suffers from poor electrical properties. Therefore, proper crystallization is necessary in this case but should be performed at low temperature just as same as deposition. Here we divided crystallization roughly into two categories: 1) metal catalyst crystallization and 2) other approaches. Since metal catalyst crystallization is more widely and frequently used than the other approaches, here we review them in details. In the topic of metal catalyst crystallization, MIC (Metal Induced Crystallization) and MILC (Metal Induced Lateral Crystallization) will be discussed separately because of the different crystallization mechanisms. The other approaches like thermal annealing, ELA (Excimer Laser Annealing), hydrogen plasma induced crystallization, C-beam (Carbon nanotube electron beam) crystallization and BLA (Blue Laser Annealing) will also be reviewed since they also provide interesting solutions to well crystallize amorphous silicon. The mechanism of each crystallization technique will be illustrated in section 1.3. The corresponding crystallinity will also be discussed.

1.2 Low temperature deposition techniques for SiNWs synthesis and silicon thin films

As a key process involved in SiNWs synthesis, deposition almost decides the highest temperature among all the processes because the other processes such as photolithography and etching normally could be operated at room temperature. Hence, low temperature synthesis of SiNWs could be included in the discussion of low temperature deposition to a large extent.

Speaking of low temperature deposition, silicon and silicon dioxide (SiO_2) are the most important materials in terms of SiNWs synthesis. Amorphous silicon (a-Si) as a semiconductor material undertakes a very important role in fabricating a variety of devices such as complementary metal-oxide-semiconductor (CMOS), thin film transistor (TFT) and even microelectromechanical systems (MEMS) devices [2]. Silicon dioxide not only can act as material layer in SiNWs synthesis, more specifically, the sidewall spacer method that will be discussed in chapter 2, but can be the gate oxide in TFT fabrication as well. Therefore, possible low temperature deposition of SiO_2 will also reviewed in this section.

But with the agreement of the low temperature technology which is used to realize the potential flexible applications, a-Si and SiO_2 deposition have met some confinement. In the context of our research, the materials should be deposited under a low temperature (≤300 ˚C) to be compatible with many flexible substrates [3]. By this consideration, we need to review the low temperature a-Si and SiO_2 deposition approaches.

Most of the low temperature deposition approaches can be divided into two categories which are physical way and chemical way. For physical approach, a-Si and SiO_2 can be deposited by sputtering [4]–[8], and for chemical approach, they can be deposited by hot-wire chemical vapor deposition (hot-wire CVD) [9]–[13], plasma enhanced CVD (PECVD) [2], [14]–[21], etc.

1.2.1 Reactive sputtering

Reactive sputtering of thin films has been broadly researched since 1980s because of the possibility of making compound films such as oxides, nitrides, etc. [4]. Besides the low temperature during the process of reactive sputtering, several limitations and difficulty on the formation of certain combined compound films should be aware of.

Using reactive sputtering to deposit a-Si:H is quite different from using other chemical vapor deposition methods in terms of the working mechanism of introduced hydrogen [5]. In general, hydrogen gas can be introduced during the deposition by different partial pressure in order to independently change the hydrogen content of the sputtered a-Si:H film. A variety of processes can take place at the target surface, including the formation of silicon hydrides and the ejection of surface species by the cascade of atoms elastically scattered by the impinging ions, i.e. chemical sputtering effects. These species, as well as neutral hydrogen atoms from the plasma, arrive at the substrate and react to form the a-Si:H film.

M. Pinarbasi et al. prepared a-Si:H films by using dc magnetron reactive sputtering [5]. What is distinct for this approach is that the hydrogen plasma generated in the reactor is confined by a magnetic field loop to the vicinity of the target. This greatly reduces the bombardment of the substrate by energetic ions and electrons, which also can improve the quality of the amorphous silicon layers.

Films were grown over a wide range of deposition conditions: 100 ˚C < T < 350 ˚C according to table 1, deposition rate with 2-22 nm/min, hydrogen partial pressure with 0.05-1.2 mTorr and the argon partial pressure was maintained constant at 1 mTorr. The experimental conditions and consequential film properties are shown in table 1. The sputtering used in [5] is specifically the DC magnetron reactive sputtering.

Table 1. Range of experimental conditions and film properties of amorphous silicon [5].

Range of deposition conditions	Deposition temperature (˚C)	100-350
	Hydrogen partial pressure (mTorr)	0.05-1.2
	Argon partial pressure (mTorr)	1.0
	Cathode current (A)	0.25-0.8
	Deposition rate (nm/min)	2-22
	Hydrogen content (at%)	2-40
Range of deposited film properties	Optical band gap (eV)	1.6-2.0
	Dark conductivity activation energy (eV)	0.7-1.0
	Dark conductivity (Ω cm^{-1})	1×10^{-12} - 1×10^{-6}
	Electron mobility-recombination lifetime	5×10^{-9} - 4×10^{-7}
	Density of midgap states (cm^{-3})	1×10^{15} - 5×10^{16}

C. S. McCormick et al. also adopted the same approach to fabricate a-Si:H layer at 125 ˚C to eventually fabricate the TFT [6]. In their work, thin film transistors were deposited by RMS (Reactive Magnetron Sputtering) in a UHV (Ultra High Vacuum) deposition system with water and oxygen background pressures less than 10^{-9} Torr. They deposited films at low total pressure conditions ($Ar+N_2$ < 3 mTorr) to ensure a dense homogeneous microstructure. The best a-Si:H layers in this paper were produced at $P(H_2)$ equaling to 0.4 mTorr and P(Ar) equaling to 1.5 mTorr. The dark conductivity of amorphous silicon layer is 4×10^{-12} $(\Omega\ cm)^{-1}$. The optical bandgap is 1.81 eV. These results indicate that the sputtered a-Si:H films depositied at 125 ˚C have quality comparable to PECVD films deposited at higher temperatures [6].

Deposition of SiO_2 film using reactive sputtering was rarely reported. In [7], amorphous SiO_2 films were reactively sputtered at temperature as low as 20˚C. In our lab, previous work of A. Saboundji et al. presented the SiO_2 deposited by RF sputtering with the target consisting of Ar/O_2 mixture [8]. There was no deliberate heating of substrate during sputtering, but the temperature of film would reach 80 ˚C.

1.2.2 Hot-wire CVD

Hot-wire CVD (also known as catalytic CVD) is a chemical phase deposition technique which allows a-Si to be deposited on the substrate without any help from plasma. Therefore, in hot-wire CVD, source gases are decomposed by the catalytic cracking reaction with heated catalyzer (for example the tungsten), usually placed near substrates. This difference of decomposition mechanism between PECVD and hot-wire CVD causes the difference in properties of prepared thin films [9], [10].

As shown in Fig. 1, with the aid of catalyzer, source gases are readily to decompose. Moreover, low temperature deposition could be realized due to the noncontact between the heated catalyzer and the substrate. Hence the temperature of substrates in hot-wire CVD can be configured independently of the heating temperature of catalyzer, which can be the interest of lowering down the substrate temperature.

J.P. Conde and P. Alpuim presented hot-wire CVD of a-Si:H on glass and PET substrates at 100˚C and 25˚C [12], [13]. For the detail of the deposition, a single tungsten filament of 0.5 mm diameter and approximately 7 cm length was placed 5 cm from the substrate and was resistively heated with a dc power supply. The filament temperature was measured with an optical pyrometer (T_{fil}=2500 ˚C) and the pressure was kept constant at 20 mTorr. The thickness

of the deposited films was between 0.2 and 0.8 µm, and the gas flow was kept at around 10 sccm. The results show a photosensitivity which is strongly dependent on substrate temperature (decreasing from 10^6 at T_{sub}=220 ˚C to 10^3 at T_{sub}=25 ˚C).

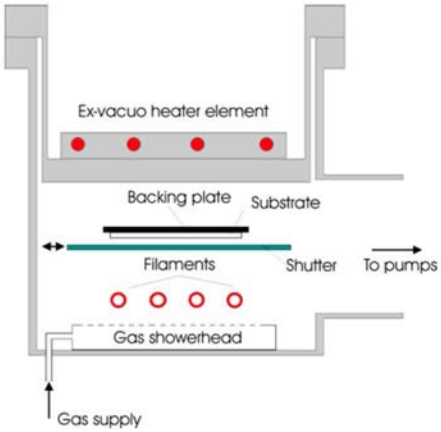

Fig. 1. Schematic view of a hot wire chemical vapor reactor [11].

From Fig. 2 we can conclude that the dark conductivity of hot wire chemical vapor deposited a-Si:H with deposition temperature at 25˚C shows no significant difference from that with higher deposition temperature (lower part of Fig. 2), which is not the same for radio frequency CVD (upper part of Fig. 2). In addition, we can consider that hot-wire CVD amorphous silicon can have moderate electrical quality even at very low deposition temperature.

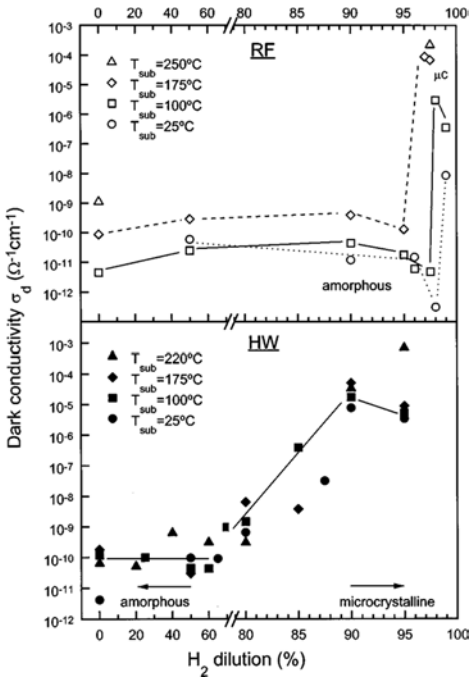

Fig. 2. Room-temperature dark conductivity of HW samples(bottom) plotted as a function of hydrogen dilution of different values of T_{sub} [12].

1.2.3 PECVD (Plasma Enhanced Chemical Vapor deposition)

Thanks to the assistance of the plasma, PECVD has the potential to reach lower temperature during the deposition. Unlike the low temperature SiO_2 deposition rarely researched by using Hot-Wire CVD, PECVD can realize SiO_2, SiN_x and silicon film deposition at low temperature.

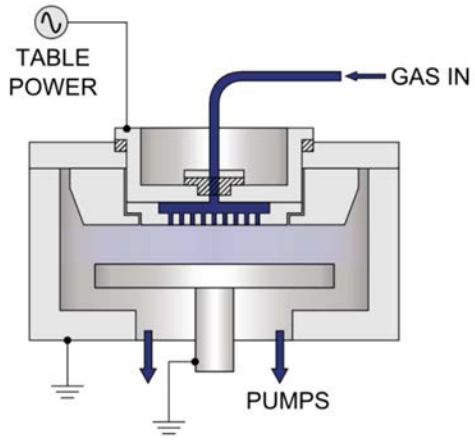

Fig. 3. Schematic of PECVD reactor [14].

Fig. 3 illustrates the working principle of a typical PECVD system. The gas would be introduced into the pumped reactor and then become reactive plasma thanks to the RF (radio frequency) power applied between anode and cathode. Normally the sample would be attached on the chuck that is also the anode of the system. The variety of the deposited films would depend on the gas mixture introduced into the reactor.

The most used gas mixture in PECVD to deposit SiO_2 is SiH_4 and N_2O/O_2, deposition temperature which is lower than 300 ˚C could be found in J. Batey and E. Tierney's work [15]. In their work, SiO_2 film deposited at 275 ˚C has been studied and confirmed having similar properties with those deposited at higher temperature except for density of deep bulk traps. Actually, as deposition temperature decreases, the quantity of hydrogen incorporated in SiO_2 increases, which eventually degrades the quality of oxide [16].

In order to reach even lower deposition temperature but to keep comparable properties at the same time, the gas mixture of TEOS (tetraethylorthosilicate) and oxygen has been explored and developed. Shashank C. Deshmukh et al. deposited SiO_2 films at temperature of 40 ˚C and 260 ˚C by using TEOS and O_2 mixture as the source material. Deposition conditions are listed in table 2 and corresponding transmission infrared spectra are shown in Fig. 4.

Table 2. Deposition conditions and wet etch rate of films A-E in P-etch solution [17].

Film	Deposition T (˚C)	$TEOS/O_2$ ratio	Etch rate (nm/s)
A	260	0.03	0.5
B	260	0.24	2.6
C	40	0.03	0.7
D	40	0.24	42.5
E	40	1.06	190

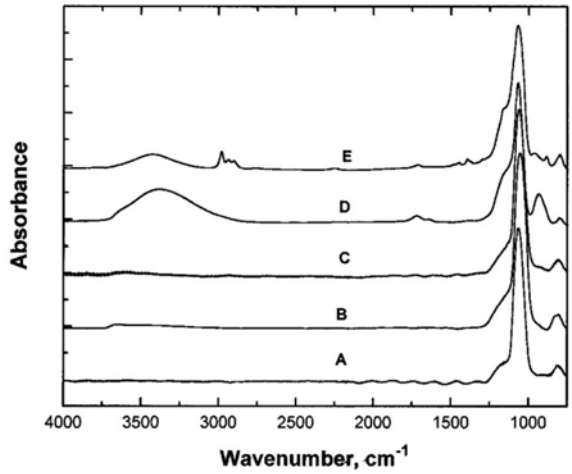

Fig. 4. Transmission FTIR spectra of the films deposited under various conditions (that are given in table 2) [17].

From Fig. 4, bumps in the spectra for film D and E at around 3300 cm^{-1} are due to O-H stretches in water trapped in film, most likely the pores in SiO_2 [17], [18]. By comparing the spectra of film D and E with that of film C, we can find inferior properties of deposited films in higher TEOS/O_2 ratio compared to the films which have lower ratio. In addition, no obvious differences could be detected among film A, B and C, which tells us SiO_2 deposited at 40 ˚C has similar properties with the one deposited at 260 ˚C. Moreover, these results indicate that deposition temperature and TEOS/O_2 ratio both play important roles in PECVD of SiO_2 [18].

A. Bousquet et al. used O_2/HMDSO (hexamethyldisiloxane) as gas mixture to deposit SiO_2 at low temperature (<100 ˚C) [19]. The ratio of O_2/HMDSO is 95:5 for total gas flow of 16 sccm, which corresponds to pressure of 0.33 Pa. The electrical properties of SiO_2 were characterized by performing C-V (Capacitance-Voltage) measurements on SiO_2 based MIS (Metal-Insulator-Semiconductor) capacitors.

Table 3 listed two different plasma conditions: continuous wave and pulses. The pulsed plasma was regulated at 50Hz with DC=0.25. DC refers to duty cycle where calculated by $T_{on}/(T_{on}+T_{off})$. From Fig. 5 we can see the SiO_2 deposited by pulse mode has larger flatband voltage than standard mode, which leads lower fixed charge densities shown in table 3. On the other hand, the breakdown field is not sensitive to the ion flux modulation.

Table 3. Ion flux (over a pulse period for pulse mode) and electrical characteristics of SiO_2 with two different conditions [19].

	300W, continuous	300W, pulsed 50Hz
Average ion flux ($cm^{-2}\,s^{-1}$)	6.8×10^{14}	2.0×10^{14}
Average breakdown field (MV cm^{-1})	7.9	8.1
Dielectric constant	4.8	4.9
Fixed charge density (cm^{-2})	2×10^{12}	4×10^{11}

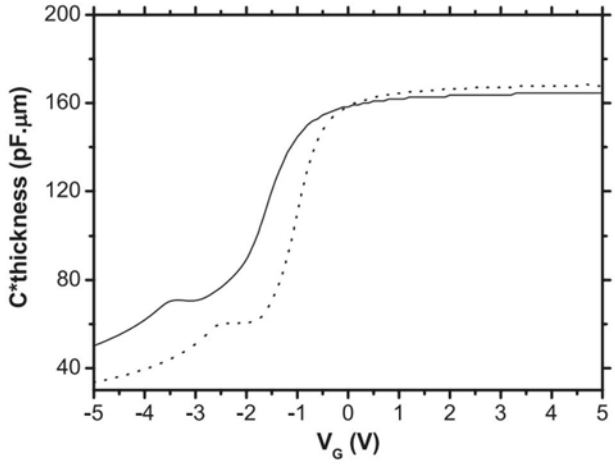

Fig. 5. C-V curves at 1 MHz (corrected by film thickness) for films deposited with 300 W in continuous mode (line) and pulsed mode at 50 Hz, DC = 0.25 (dot) [19].

Depositing amorphous silicon (a-Si) at low temperature is also very important when we tend to fabricate some electronic devices for low temperature purpose. This makes PECVD a good candidate for the a-Si deposition because it can reach temperature down to 150 ˚C[4], [20], [21] or even less compared to other chemical vapor deposition methods for example the low pressure chemical vapor deposition (LPCVD) and atmospheric pressure CVD (APCVD).

In practice, PECVD a-Si would suffer a temperature limit during the process since the structural quality of a-Si layer will degenerate when deposition temperature of the substrate decreases below 100 ˚C [21]. Therefore, it is necessary to review the quality of PECVD a-Si layer.

S. Chang and S. Sivoththaman have developed a PECVD of hydrogenated amorphous silicon (a-Si:H) as the structural layer of MEMS devices at 150 ˚C [2]. During the process, in

order to achieve a practical deposition rate, the chamber pressure and the RF power were varied while maintaining stable plasma. Measured deposition rates are listed in table 4.

Table 4. Variation in deposition rate for PECVD a-Si:H films (SiH_4 gas flow = 10 sccm, Ar gas flow = 7 sccm, substrate temperature = 150 ˚C). The 0.51 nm s^{-1} deposition rate was the maximum rate obtained (100 kHz parallel plate system with 8-inch electrode) [2].

Pressure (mTorr)	RF power (mW cm^{-2})	Deposition rate (nm s^{-1})
500	77	0.38
500	93	0.41
750	93	0.46
750	114	0.51

Seen from Fig. 6, there is a 1.5 μm a-Si:H film deposited over 2.7 μm step of photoresist on c-Si substrate forming an 80º sidewall angle, viewed at 75º tilt.

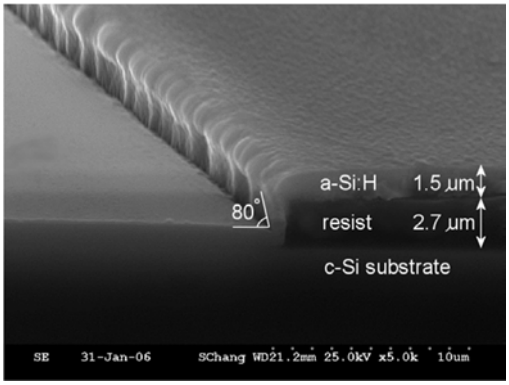

Fig. 6. SEM cross-section of a-Si:H film deposited over step of resist [2].

The electrical conductivity of deposited a-Si:H layer was measured by current-voltage characteristics. A dark conductivity of 1×10^{-10} S cm^{-1} and due to the light-induced properties of a-Si:H, a photoconductivity of 1×10^{-6} S cm^{-1} was measured under illumination intensity of 4 mW cm^{-2} by a halogen tungsten lamp.

C. -S. Yang et al. investigated a-Si:H deposition which was dedicated to fabricate a-Si TFTs on glass and PET plastic substrates at 110 ˚C [20]. For intrinsic a-Si deposition, a H_2 /SiH_4 flow ratio of 20 was used at a power density of 35 mW/cm^2 using processing pressures

from 0.225 to 1.5 Torr. The deposition conditions that produced the most typical and reproducible results for TFT fabrication were as follows:

Table 5. PECVD condition sets for various TFTs [20].

PECVD condition set No.	a-Si:H
1	H_2 /SiH_4=1000/50 sccm, 1.5 Torr, 35 mW/cm^2
2	H_2 /SiH_4=1000/50 sccm, 0.6 Torr, 35 mW/cm^2
3	H_2 /SiH_4=1000/50 sccm, 1.5 Torr, 35 mW/cm^2
4	H_2 /SiH_4=1000/50 sccm, 0.225 Torr, 35 mW/cm^2
5 (glass or PET substrate)	H_2 /SiH_4=1000/50 sccm, 1.5 Torr, 35 mW/cm^2

The electrical properties of deposited a-Si:H were not characterized independently in this paper, but the authors characterized the electrons mobility and threshold voltage of the TFTs which were fabricated using a-Si:H layers mentioned above in table 5, and reported in table 6.

Table 6. Summary of a-Si:H TFT performances. TFTs were fabricated on glass substrates except where otherwise indicated. The range of values reported for the 250 ˚C devices represent samples prepared using otherwise similar conditions as those of PECVD condition No. 1–5 [20].

PECVD condition set No.	Threshold voltage (V)	Effective linear mobility of electrons (cm^2/V s)	Inverse subthreshold slope (V/decade)
1	4.2	0.54	0.8
2	8.0	0.45	0.6
3	4.5	0.36	0.7
4	7.0	0.14	2.0
5(on glass)	5.0	0.33	0.7
5(on PET)	5.0	0.12	0.9
250 ˚C PECVD	0.5-3.0	0.5-1.0	0.3-0.7

One should notice that at the same condition of PECVD but on different substrates (on glass and on PET), the threshold voltage is higher at lower pressure while the effective linear mobility of electrons of TFT decreases with the pressure, and is nearly nearly 3 times higher on glass substrate as that on PET substrate.

C. Koch et al. developed low temperature a-Si:H PECVD for solar cell application at various temperature from 50 to 150 ˚C [21]. For the T_s=100 ˚C films they keep the deposition pressure at P=0.375 mTorr and the plasma power density at p=120mW/cm^2.

The growth rate r_d, optical band gap E_g and the mobility-lifetime product μ×t of a-Si:H at each temperature are listed in table 7.

Table 7. The growth rate, optical band gap and mobility-lifetime product of deposited a-Si:H as a function of deposition temperature [21].

T_s (˚C)	r_d (nm/s)	E_g (eV)	μt (cm^2/V)
50	0.382	1.92	1.5×10^{-11}
75	0.28	1.87	1.7×10^{-9}
100	0.242	1.85	3.0×10^{-8}
150	0.183	1.83	4.0×10^{-7}

Which can be observed from the table is an increase in the growth rate from 0.2 to 0.4 nm/s towards low temperatures due to an increased sticking coefficient of the precursors on the growing surface. A remarkable deterioration of electronic properties can also be observed through the μ×t-product which drops by more than four orders of magnitude with reduced deposition temperature while the optical band gap keeps almost the same value through temperature variation. In addition, faster deposition would lead to more porous film which eventually deteriorates its electrical properties. Therefore, depositing a-Si at around 150 ˚C is a good compromise between thermal budget and electro properties. Obviously, the electrical properties can be improved if the deposition temperature keeps increasing but no more than 300˚C (to be considered as low temperature deposition).

In a brief summary, amorphous silicon and silicon dioxide can be deposited by using PECVD at low temperatures but a-Si layers still present poor electrical properties.

1.3 Low temperature silicon crystallization methods

Since amorphous silicon suffers from very poor electrical properties compared to poly-crystalline or crystalline silicon, the crystallization of a-Si has attracted intense research interest around the world. On the one hand, the crystallization plays an important role in improving the electrical performance of a-Si; on the other hand, it is confined by the thermal budget which restricts the crystallization temperature down to 350˚C at least [22]–[26] for compatibility with low temperature substrates.

Crystallized microcrystalline silicon (μc-Si) or poly-Si has been obtained by using a variety of techniques, such as solid phase crystallization (SPC) [23], [24], laser phase crystallization (LPC) [23], [25], [26], flash lamp annealing (FLA) and metal induced crystallization or metal induced lateral crystallization (MIC/MILC). To eliminate the potential ambiguity, there are some alternative names of certain techniques, for example LPC may also be known as laser-annealing-crystallization (LAC) or more specifically excimer laser crystallization (ELC). These techniques work in different mechanisms thus have different working temperature limits.

With rapid development of flexible electronics such as wearable electronic devices, flexible displays and solar cells, silicon-based technologies show great value in mass production probability. In order to get relatively high performance of silicon layers, the thermal budget of crystallization must be taken into account as we mentioned above. Under this circumstance, the commonly used SPC conducted in a furnace requires a high temperature (>600 ˚C) and a long-time (>10 h) thermal annealing because the formation of crystalline nuclei in the precursor a-Si matrix has to overcome a large barrier energy of ~5 eV [26]. This makes SPC a bad candidate when crystallization is performed on plastic substrates. FLA may also not be a wise option since precise thickness penetration of flash lamp is difficult to control and the heat distribution profile in the silicon layers is much wider compared to ELC technique. This is more critical when very thin layer of silicon (sub-micrometer thick) is needed. For this reason, we will review MIC/MILC [22], [27]–[42] as the mainstream of low temperature silicon crystallization techniques. Besides, we will also review the other approaches such as ELC, H_2 plasma induced crystallization, C-beam crystallization, blue laser annealing, etc. These approaches are all compatible with low temperature process (≤300˚C).

1.3.1 Metal Induced Crystallization (MIC)

Using a metal/a-Si bilayer structure in MIC is effective for decreasing the activation energy of crystallization, and can easily induce transformation from a-Si to poly-Si at relative low temperature. In practice, a metal film would be deposited on top of and in contact with the a-Si layer in prior to crystallization [31], [37].

In comparison with SPC, crystallization temperature of MIC can be significantly reduced if we choose the metal in a specific manner. Actually, various metal materials have been proved to effectively crystallize the amorphous silicon, such as Ni, Pd, Pt, Cu, Ag, Au and Al. Figure 7 shows the theoretical crystallization temperature when different metals involved and maximum operating temperatures of some typical flexible substrates.

The different metals used in MIC have generally two groups. The first group consists of metals that form silicide phase (Ni, Pd, Pt and most researched metals) during the crystallization process, while the second group of metals have eutectic reaction with a-Si (Au, Ag and Al). The second group would be more interesting because the crystallization can actually be activated even lower than the eutectic temperature between the metal and silicon, which enables the low temperature crystallization of a-Si. Therefore, in this part, Al-IC, Au-IC and Sn-IC would be reviewed in detail.

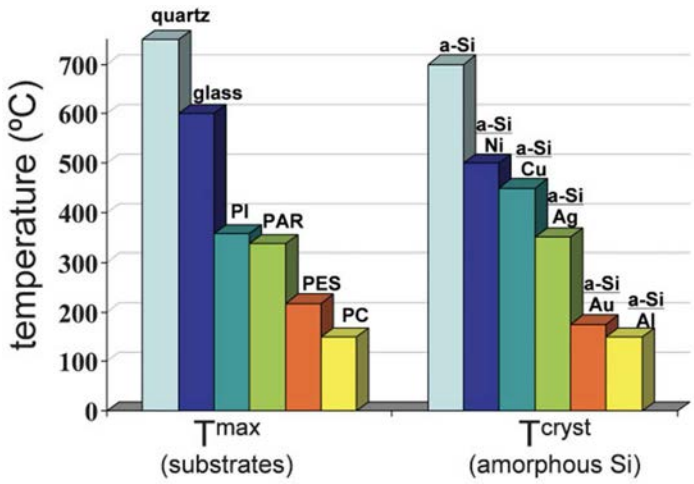

Fig. 7. The left-hand side shows the maximum operating temperatures (Tmax) of some technologically important substrates: quartz glass, conventional glass, polyimide (PI), polyarylate (PAR), polyethersulfone (PES), and polycarbonate (PC). The right-hand side shows the reduction in the crystallization temperature of a-Si (Tcryst) induced by contact with various metals [25].

Aluminum induced crystallization (Al-IC)

Al-IC has been widely researched thanks to the easy access to this metal and relative low operating temperature. Fig. 8 shows the Al-IC mechanism. One should notice that there would be a phenomenon of "layer exchange" during the Al-IC. But this phenomenon would be absent when there is existence of aluminum oxide layer at the interface of aluminum and silicon. Consequently, a mixed film of Al and poly-Si will form after crystallization. Therefore, a complete crystallization by using Al as catalyst should guarantee a pure interface just between aluminum and a-Si.

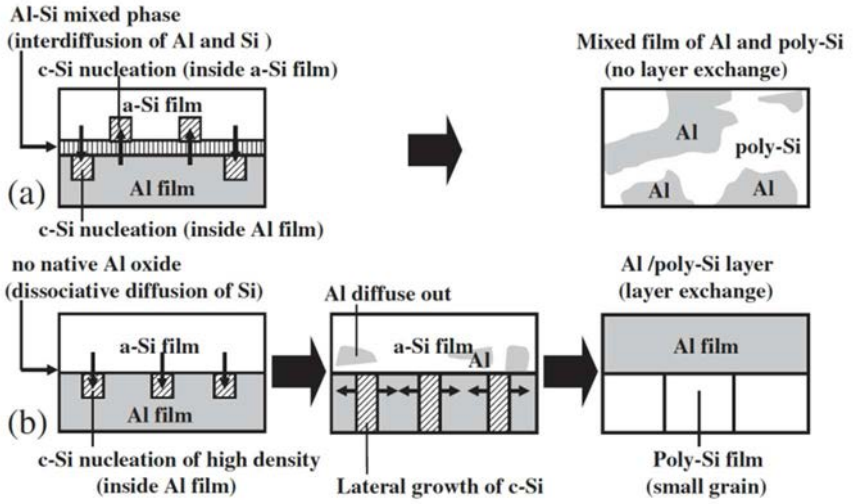

Fig. 8. (a) Schematic Al-IC models having Al-Si mixed phase and (b) no native oxide (or very thin Al oxide film) at a-Si/Al interface [31].

R. Kishore et al. performed Al-IC for 50 nm thick a-Si:H at a temperature as low as 150 ˚C [28]. The samples were transferred to a vacuum evaporation system immediately after a-Si:H deposition, then the 50nm thick Al was deposited over the entire surface of the a-Si:H film. After this, the crystallization was performed under vacuum (2mTorr) in a clean, optically heated quartz tube furnace.

Fig. 9 shows the microstructure of a film annealed at 150˚C for 30 min. Here, the microstructure (recorded at 50 K magnification) and the EDP (Electron Diffraction Pattern) in the inset shows that the a-Si:H is completely crystallized into randomly oriented polycrystalline silicon, in which the 111, 220, and 311 silicon rings are prominent. Grains as large as 0.2-0.3 μm can be seen in the micrograph and the distribution appears uniform. In addition, the

crystallized volume is the function of the annealing time, which means bigger crystallization volume requires longer annealing duration.

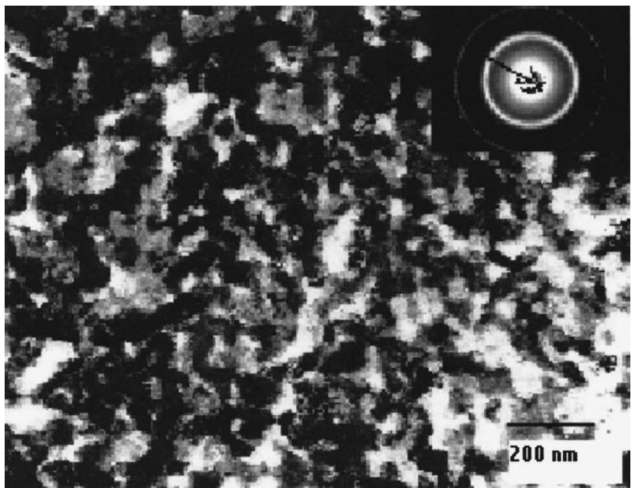

Fig. 9. Plan view TEM of a specimen annealed at 150˚C for 30 min. Inset, an EDP (electron diffraction pattern) of the selected area from which the Al film was removed after annealing. Si<111, 220, and 311> rings are clearly observed. The material is randomly oriented poly-Si with a grain size ranging from 0.2 to 0.5 μm [28].

Gold induced crystallization (Au-IC)

As the same mechanism as Al-IC, Au-IC has layer exchange during the crystallization as well. Ch. Kishan Singh et al. studied Au-IC of a-Si on Corning glass substrate at temperature down to 350 ˚C which is lower than the eutectic temperature of Au and Si [32].

In this study, Au thin films with thickness of ~250nm were pre-deposited on cleaned Corning soda lime glass 0215 substrates using DC sputtering. Subsequently, layer of a-Si thin films with thickness of ~100 to 200nm were deposited onto the substrates by electron beam evaporation to form a-Si/Au/glass thin film structure. The specimens were then isochronally annealed at 350 ˚C in vacuum at ~10^{-8} mbar.

From Fig. 10, the average grain size measurements of the poly-Si were investigated using an optical microscope. It shows the optical micrograph obtained from the bottom side of the specimen annealed at 350 ˚C and it reveals that the grain sizes are in sub-micrometer range. This indicates that the nucleation density of c-Si (which ultimately decides the grain sizes) is very high and uniform throughout the film. The corresponding Raman spectra acquired from

both the top and bottom-sides (through the glass substrate) of the specimen vacuum annealed at 350 ˚C are shown in Fig. 11. The spectrum acquired from the bottom side exhibits a well-defined characteristic Si peak at wave number ~ 521 cm^{-1}. This peak originates from the vibrational mode of Si-Si bond in the crystallized Si grains and reveals crystallization of Si layer.

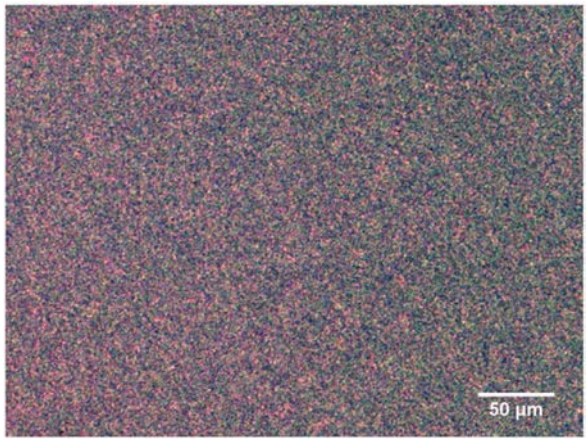

Fig. 10. Optical micrograph of the specimen annealed under vacuum at 350˚C for 6h observed from the bottom side of the glass substrate [32].

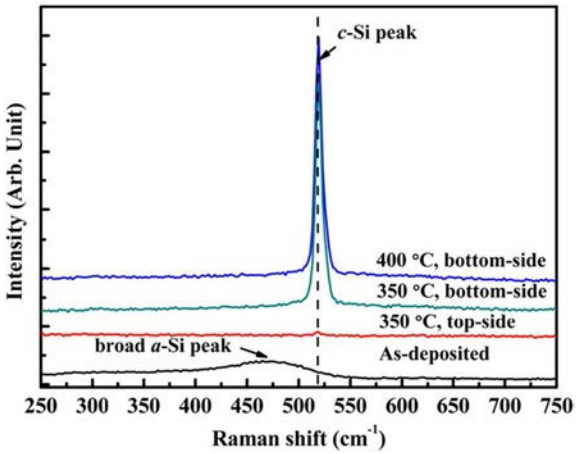

Fig. 11. Raman spectra for the as-deposited and vacuum annealed specimens (at 350˚C for 6h) [32].

Tin induced crystallization (Sn-IC)

M. Jeon et al. presented the study of a-Si crystallization on glass substrates by using a Sn metal with low Si-Sn eutectic temperature of 232˚C [33]. In this study, Sn metal film was

evaporated at a rate of <0.7 nm/s, and the samples were continuously annealed for 1h at various temperature (300, 350, 400 and 450˚C) in an atmosphere of air.

In Fig. 12, all images have same scale bar of 1μm. The grain size of surface in the poly-Si films became larger, compared to the as deposited a-Si:H thin film surface according to this paper. Moreover, although the annealing temperature was as low as 300 ˚C, the grains of crystallised poly-Si were clearly revealed (see Fig. 12(a)).

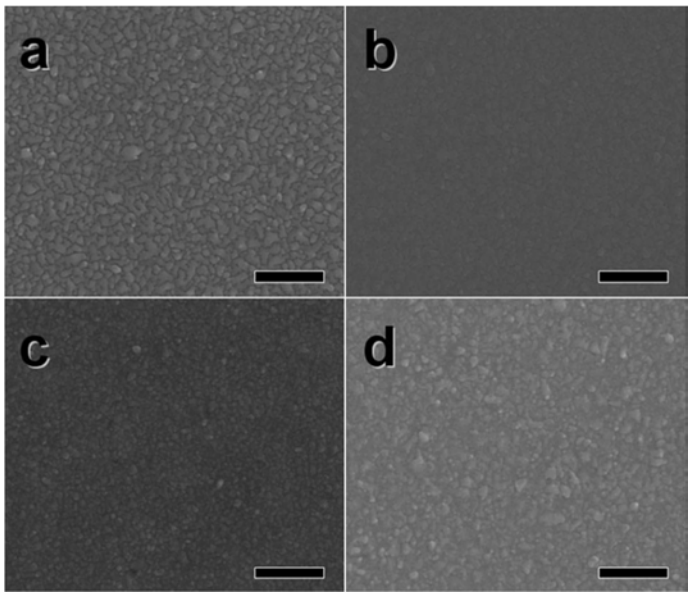

Fig. 12. SEM images of fabricated poly-Si films annealed at (a)300 ˚C, (b)350 ˚C, (c)400 ˚C and (d)450 ˚C [33].

By observing four images in Fig. 12, the grain sizes of samples fabricated at all annealing temperatures were about 100–250 nm. Therefore, there is no significant influence of the annealing temperature on the grain size. In addition, good crystallization could be obtained at temperature as low as 300 ˚C.

Fig. 13 indicates that the Hall mobility increased and the resistivity decreased as the annealing temperature increased from 300 to 450˚C. The measured values of resistivity were 54, 3.1, 0.56 and 0.4 Ω cm for fabricated poly-Si films annealed at 300, 350, 400 and 450˚C respectively. Furthermore, the values of Hall mobility were 3.5, 2.6, 4.2 and 6.4 $cm^2 V^{-1} s$ for fabricated poly-Si films annealed at 300, 350, 400 and 450˚C respectively.

In conclusion, Sn metal induced crystallization of the a-Si thin films as low as temperature of 300˚C gives better electrical properties than a-Si layers.

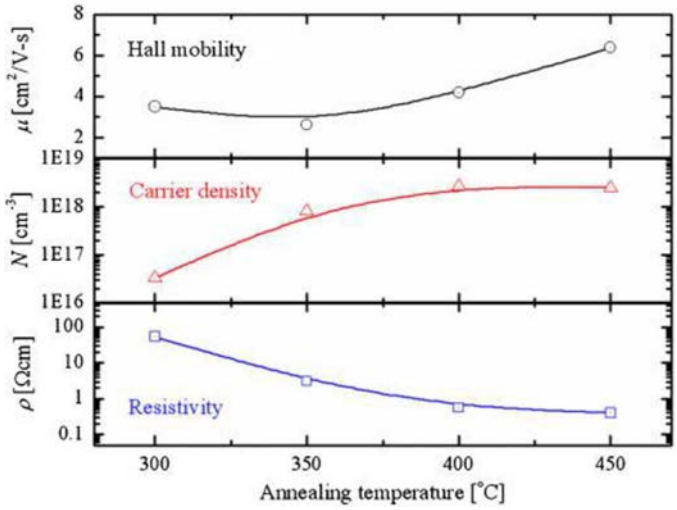

Fig. 13. Hall mobility, carrier density and resistivity of fabricated poly-Si films induced by Sn thin film with various annealing temperatures [33].

1.3.2 Metal Induced Lateral Crystallization (MILC)

Although MIC presents many advantages such as lower crystallization temperature and simple manipulation of process, it still suffers from the problem of introducing contamination into the silicon films. By considering this, MILC has been intensively researched as an alternative approach of MIC.

Generally, the MILC is carried out by depositing and patterning a small area of metal films instead of depositing the metal films on entire a-Si surface, and then the a-Si film right under the metal films was crystallized to a poly-Si at the initial stage of annealing. These seeds were then grown laterally into the metal-free area without further nucleating [38]. Therefore, by this approach, obtained poly-Si films not only have large grains but have few metal contaminations as well.

K. H. Lee et al. developed the gold MILC for crystallizing 100nm thick a-Si:H films on glass substrates at various temperature (200, 300, 350 and 400˚C) [34]. The 100nm thick Au layer was locally deposited by thermal evaporation through a finger metal mask. And then the samples were annealed at different temperatures listed above for 10-40h.

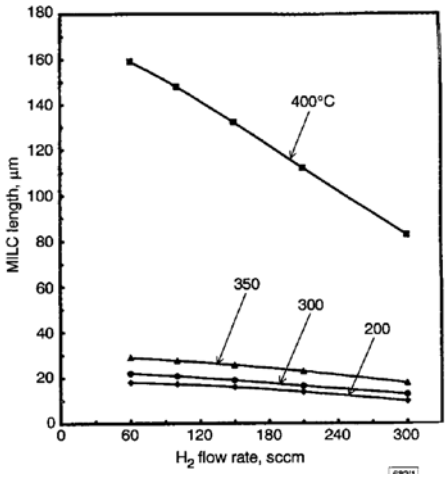

Fig. 14. Relations between flow rate of H_2 and MILC length with different annealing temperature ranges [34].

Fig. 14 shows that the higher the annealing temperature is, the longer the MILC length. The formation of Au-Si compounds and hence the metal induced lateral crystallization of a-Si:H film will be accelerated by the increased energy due to the higher temperature. Notice that the MILC length of crystallization temperature of 400˚C is phenomenal higher than that of other crystallization temperatures. Since 400˚C is slightly higher than the eutectic temperature (~363˚C), the Si film in this case is partially in the crystallized state or in the liquid phase which will promote the Si atoms to diffuse towards the front edge of the MILC range and crystallized there, thus forming longer MILC lengths. The quality of Au-MILC was examined by SEM analysis, which indicated a homogeneous poly-Si film.

One fact is that nearly all the MILC approaches are performed at relative high temperature (≥400˚C) [22], [35], [36]. This can be attributed to the metals that were used in these researches. Those metals have quite high eutectic temperature with Si, thus increasing the crystallization temperature. Hence, it will be interesting to carry out research on MILC using low eutectic temperature metal. In this case, indium (eutectic temperature is 158˚C) could be a very potential candidate for the MILC process.

1.3.3 Indium induced crystallization

Indium induced crystallization here is discussed independently as a section because it does not strictly follow the rules of "lateral crystallization" as we mentioned above. In some cases, the crystallization catalyzed by indium could be classified either into MIC or MILC. Since indium has extremely low eutectic temperature compared with the other metal catalysts, the indium induced crystallization provides a promising way to realize low temperature crystallization.

R. Heimburger et al. reported indium induced crystallization on glass substrate below 330˚C [38]. A 25nm thick indium layer was deposited after the deposition of amorphous silicon with the thickness of 400 or 800nm, then the annealing was carried out at temperature between 266 and 328 ˚C. The samples were characterized by using SEM (Fig. 15) and micro-Raman spectroscopy (Fig. 16).

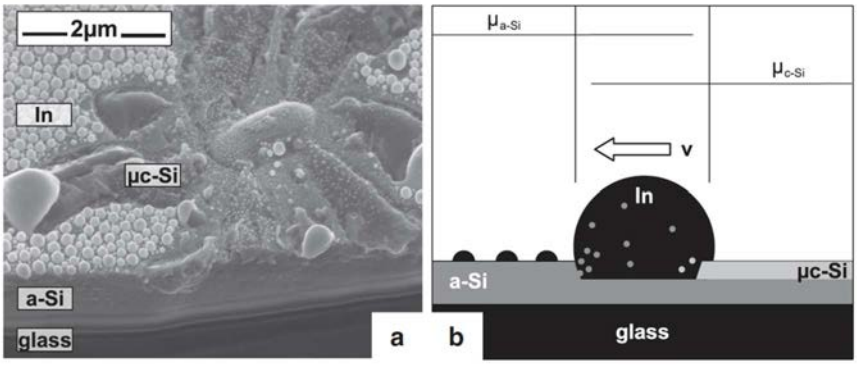

Fig. 15. (a) 45° tilt SEM image of an initial μc-Si cluster near breaking edge; (b) schematic view of the ALC (Amorphous-Liquid-Crystalline) mechanism [38].

In Fig. 15(b) the process of crystallization is illustrated schematically, the a-Si is dissoved in the front margin of indium droplet, and μc-Si is segregated at the rare margin. The movement of crystallization is considered in-plane, which is clearly shown in Fig. 15(a).

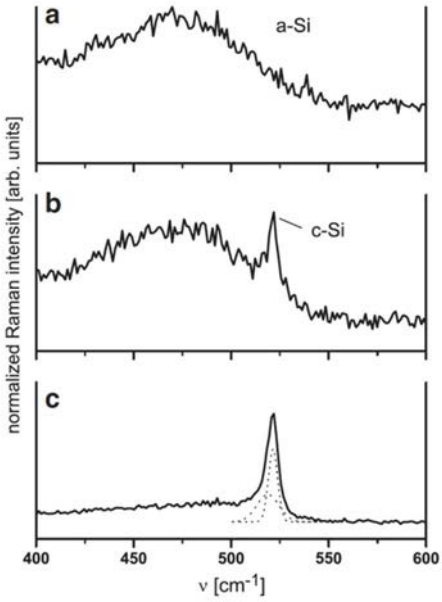

Fig. 16. Raman spectrum recorded (a) outside μc-Si domain; (b) crossing of the domain boundary and (c) inside the domain (stepwidth: 2μm) [38].

From the Raman spectra in Fig.16 we can observe a clear change in crystallinity from the outside of μc-Si cluster to the inside of that, which indicates a good crystallinity. Full area crystallization has been observed at 320 ˚C within one hour of annealing. Their further research even took a leap after successfully crystallizing a-Si, they added a thicken layer of a-Si on top of crystallized nc-Si layer, then they initialized SSLPE (Steady-State Liquid-Phase Epitaxy) to form crystalline silicon. First step crystallization could be realized at temperature as low as 300˚C with size of crystallized grains up to 100nm [39].

L. Yu team has developed an in-plane SLS (Solid Liquid Solid) method to grow the SiNWs and to crystallize them at the same time by using ITO (indium tin oxide) as the catalyst [40]–[42].

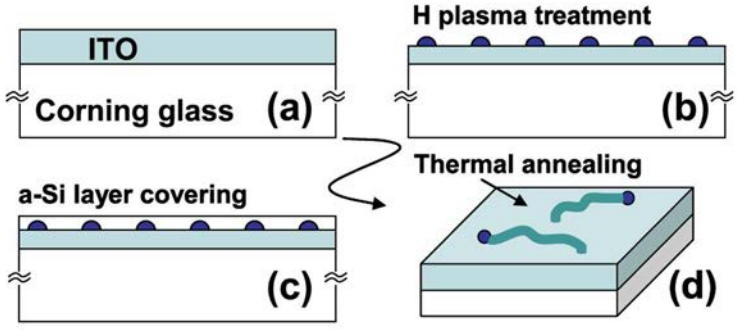

Fig. 17. Basic experimental procedure for the growth of IP (In-Plane) SLS SiNWs [40].

The ITO layer was first treated by using hydrogen (H_2) plasma in PECVD reactor to form indium drops on the surface. Then the substrate was covered by a-Si:H deposited at 100-200 ˚C. Finally, the substrate was annealed in vacuum (~10^{-6} mbar) at a temperature range between 300 ˚C and 500 ˚C for the activation of the growth of SiNWs. Two things should be cleared for this technique: 1) the crystallization could be considered as the "indium catalyzed" crystallization since major part in ITO is indium and therefore the drops formed by indium; 2) the crystallization could be classified into MILC because the nanowires grow laterally instead of globally on the surface of a-Si.

The crystallinity was examined by Raman analysis and the result is shown in Fig. 18. A SiNW segment was visualized by AFM in Fig. 18(a) and corresponding Raman signal intensity was targeting at the same region of SiNW in Fig. 18(b). From the inset in Fig. 18(a), a clear peak centered at 521 cm^{-1} confirms good crystallinity of the SiNW, which therefore implies the feasibility of this crystallization technique.

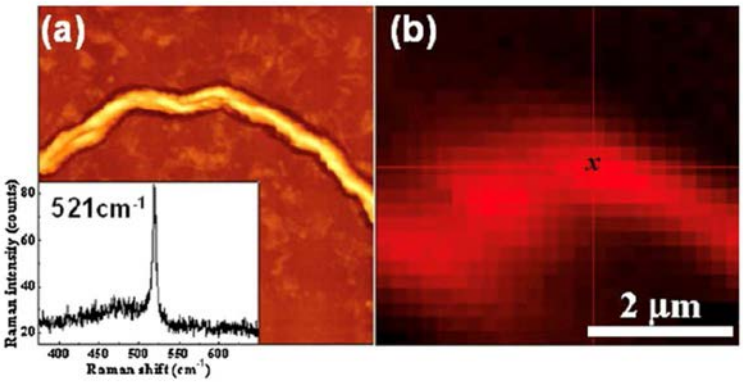

Fig. 18. (a) AFM image of a single SiNW with vertical scale from black to white of 160 nm, and (b) its corresponding crystalline Si Raman peak signal mapping (integrated in the spectral window 521±5 cm-1). The inset in (a) shows the Raman spectrum recorded from the position marked with an x in (b) [40].

The mechanism of crystallization of a-Si as well as growth of SiNWs is well explained in [40], [41]. At the early phase of crystallization, when temperature exceeds the eutectic temperature of indium (~157 ˚C), the indium drops turn into liquid state and begin to absorb a-Si. When concentration of silicon absorbed in indium increases until saturation occurs, the

silicon seeds would happen in In drops. Since there is a difference of Gibbs energy between a-Si and c-Si, the crystallization would continue under the driving force generated from the difference.

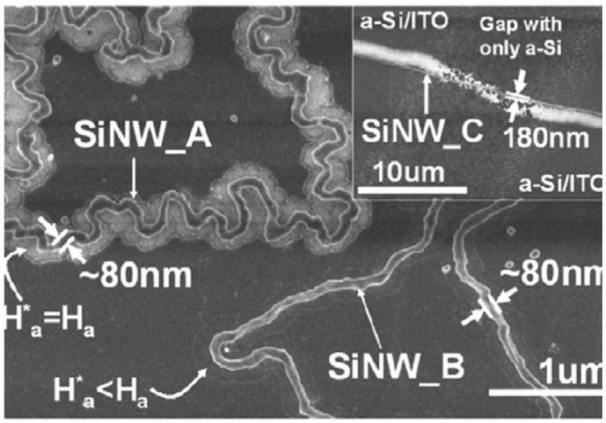

Fig. 19. Three SiNWs (A, B, and C) obtained on the same sample but with different morphologies [40].

The in-plane SLS grown SiNWs normally have three forms which are shown in Fig. 19 noted as SiNW_A, B and C. SiNW_A and B could be easily distinguished by the real thickness of a-Si absorbed into In drops during crystallization. When all thickness of a-Si is absorbed, the SiNWs tend to grow as zig-zag wires, whereas the SiNWs grow straighter when the real absorbed thickness of a-Si is less than total thickness of a-Si. Specifically, when speed of precipitation of crystallized silicon is faster than the absorption of a-Si, the In drops could be stretched when they move, thus produce even straighter nanowires than the case of SiNW_B. This is the exact case of SiNW_C shown in the inset of Fig. 19. An irregular growth type of SiNWs called suspended growth is discussed in detail in [42], which could help researcher understand better on the growth mechanism of In Plane-SLS (IPSLS) SiNWs. In addition, the size of SiNW is proportional to the diameter of In drop.

In conclusion, crystallization of a-Si could be accomplished by using indium as catalyst. The low eutectic temperature of indium enables lower temperature crystallization compared to the other metal materials.

1.3.4 Other approaches

Beside the low temperature compatible crystallization techniques we reviewed above, there are some other approaches of a-Si low temperature crystallization techniques. They all show a good compromise between the thermal budget and the electrical properties. Here we review four approaches of crystallization such as excimer laser annealing (ELA) [23], [43]–[45], hydrogen induced crystallization [26], [46], carbon nanotube electron beam crystallization (C-beam crystallization) [47] and blue laser annealing (BLA) [48]–[50].

Excimer Laser Annealing (ELA)

Excimer laser annealing is another mature technology to crystallize amorphous silicon by injecting excimer laser shots onto the surface of amorphous silicon. This technology has been broadly researched and has improved and matured over the past 30 years [23].

Typical excimer lasers operate in pulse mode, at frequencies around 300 Hz, with pulse duration in the range of 10-50 ns. The energy output of excimer lasers for fabricating TFTs is in the order of 0.6-2 J. In prior to all the parameters in ELA, pulse-to-pulse repeatability of the excimer laser is the most important manner of the process, and followed by the discharge frequency, output energy and pulse duration.

In general, the energy of one shot of excimer laser is enough to melt silicon at the surface, but the most extreme heating is confined to the near region of the amorphous layer due to the short duration of the laser pulse. As a result, the total integrated energy is generally small since only a small depth of material is processed. Therefore, although the laser pulse can melt a-Si, temperature into the underlying layer that risen by laser is no more than a few hundred degrees [43].

Previously in our lab, T. Pier et al. developed excimer laser crystallization on μc-Si to improve its crystallinity [44]. 200 nm thick μc-Si film was deposited by PECVD on PEN substrate with highest temperature of 165 ˚C. After that, the μc-Si was laser annealed by a pulsed KrF excimer laser emitting at 248 nm. To prevent abrupt hydrogen evolution from the silicon layer leading to μc -Si film destruction, the annealing energy started from 80 mJ/cm^2 and increased with a step of 5 mJ/cm^2.

From Fig. 20 we can see grain size of silicon has increasingly enlarged after performing ELC with energy of 180 mJ/cm^2. Highest grain size is around 100 nm. According to T. Pier's

work, energy larger than 180 mJ/cm^2 would destroy the PEN substrate. The TFTs based on annealed and non-annealed µc -Si have been fabricated. The transfer characteristics have been extracted for both cases and are shown in Fig. 21. From this figure we can see the field effect mobility has been seeing a huge improvement from 1 to 46 cm^2/V.s after crystallization. In addition, the off current also increased as expected.

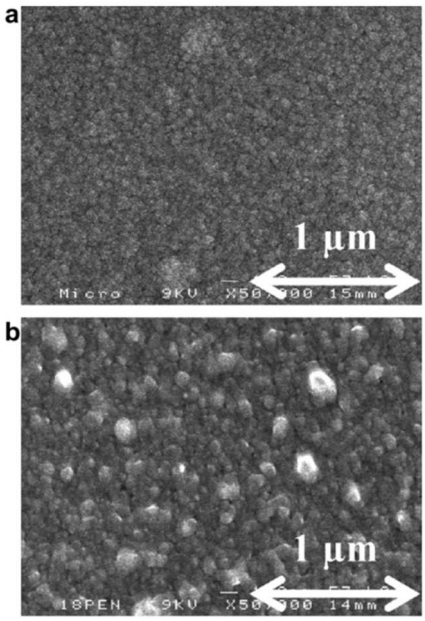

Fig. 20. SEM observation of (a) starting µc -Si film deposited on PEN and (b) after laser annealing at a maximum laser energy of 180 mJ/cm^2 [44].

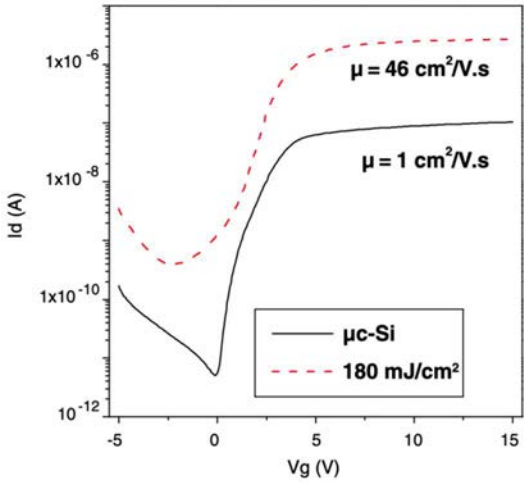

Fig. 21. Transfer characteristics of two same size TFTs (W/L = 40/60) on the same PEN plate produced from starting lc-Si (full line) and lc-Si annealed at a maximum laser energy of 180 mJ/cm2 (dashed line) [44].

P. M. Smith et al. set an extreme case by using a laser energy fluence of 450 mJ/cm^2 [43]. This results in a simulated melt depth of 100nm thick in the Si film. But in practical cases, the energy as high as 450 mJ/cm^2 is not tend to applied. From the Fig. 22 we can observe that temperature at the depth of 1μm into the plastic substrate reaches a maximum of 250˚C 30μs after the laser pulse is initiated, which could be accepted by various plastic substrates.

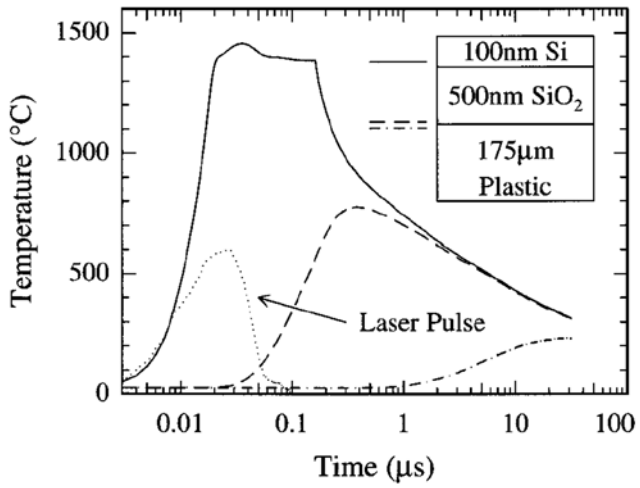

Fig. 22. Transient thermal calculations for an incident XeCl laser pulse of approximately 35ns full width at half maximum (FWHM) (dotted line-actual temporal profile used in the calculation) on a thin film stack consisting of 100 nm Si, 500 nm SiO_2 and 175 μm polyester. The calculated temperatures at the Si/SiO_2 interface (solid line), in the SiO_2 just before the SiO_2/plastic interface (dashed line), and 1 μm into the plastic (dot-dashed line) are shown vs. time. The laser fluence was 450 mJ/cm^2 [43].

Therefore, in order to prevent plastic substrates from melting, the laser pulse energy and the pulse duration should be carefully configured. Otherwise, a barrier layer like SiO_2 should be used to prevent the substrate from melting by high energy laser [44].

From the same group, they subsequently crystallized the a-Si by using a 35ns excimer laser pulse (XeCl: 308 nm) in a vacuum (~1mTorr) for crystallization. Beam intensity uniformity within the 8×8 mm beam spot is measured at ±3%. They started with 30 pulses of 130 mJ/cm^2, followed by another 30 pulses at 160 mJ/cm^2. And subsequent irradiations at fluences of 20 mJ/cm^2 were then used to repeatedly melt and crystallize the film. Cross-sectional transmission

electron microscopy (TEM) confirms the complete crystallization of the a-Si film, as shown in Fig. 23. Sheet resistances for the crystallized films measured down to 450 Ω/□, a value more than adequate for poly-Si TFT devices.

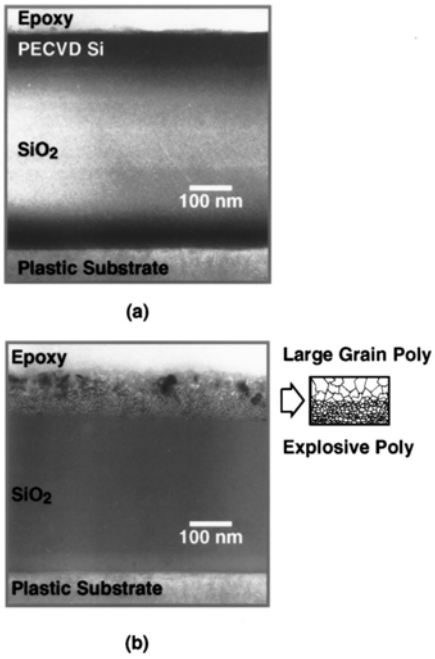

Fig. 23. Cross-sectional TEM micrograph of the Si/SiO_2/plastic stack; (a) as-deposited (100 ˚C), and (b)after 30 laser pulses at fluences of 130, 160 and 200 mJ/cm^2 [43].

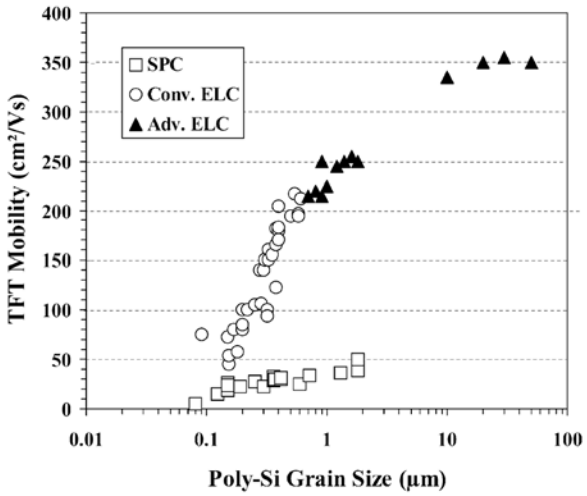

Fig. 24. TFT mobility as a function of poly-Si grain size [23].

As a comparison, we can observe from the Fig. 24, the typical ELA can induce the crystallized poly-Si grain size between 0.3-0.6μm, thus have the TFT mobility from 50 cm^2/V

s up to 200 cm^2/V s, which is 2 to 4 times higher than that of SPC poly-Si. The advanced ELC appears in Fig. 24 is a lateral crystallization technique. It was developed from the conventional ELC by precisely controlling the melt silicon and solid silicon interface into a certain thickness and using the solid silicon as seed for lateral crystallization. In this case field effect mobility can reach 350 $cm^2/V.s$.

Nevertheless, ELA still suffers from bad morphology of silicon layer, which can cause more states density on the surface of and into silicon. Besides, ELA would obviously increase the complexity of crystallization process with which the repeatability of crystallization would be difficult to control.

Hydrogen plasma induced crystallization

Plasma-induced-crystallization (PIC) has been proposed as an evidenced crystallization approach, it has been proved that this technique can effectively lower down the crystallization temperature [26]. Hydrogen plasma as one of the most commonly used plasma was introduced to the PIC category by S. Sriaman et al. in 2002 [46]. The highest temperature for this crystallization method is 300 ˚C.

In general, H_2-induced crystallization is mediated by insertion of H atoms into strained Si-Si bonds through the formation of intermediate bond-centered Si-H-Si configurations as the H atoms diffuse through the a-Si:H film. And subsequent structural relaxation of these Si-Si bonds results in the transformation of film's structure from amorphous to nanocrystalline. The film would keep transforming to crystalline silicon with increasing H exposure.

H. P. Zhou et al. proposed a relative rapid H_2-induced crystallization of ~2μm thick a-Si:H films at temperature of 300 ˚C [26]. In this work, they introduced high-density inductively coupled plasma (ICP) of H_2 (up to ~$10^{13}/cm^3$) into reactor at low pressure to process the crystallization, the input RF power density and the sample-holder temperature for this stage are 42 mW/cm^3 and 300˚C respectively. The treatment duration was varied from 0 to 30 minutes in order to investigate the time evolution of hydrogen in-diffusion in a-Si:H films.

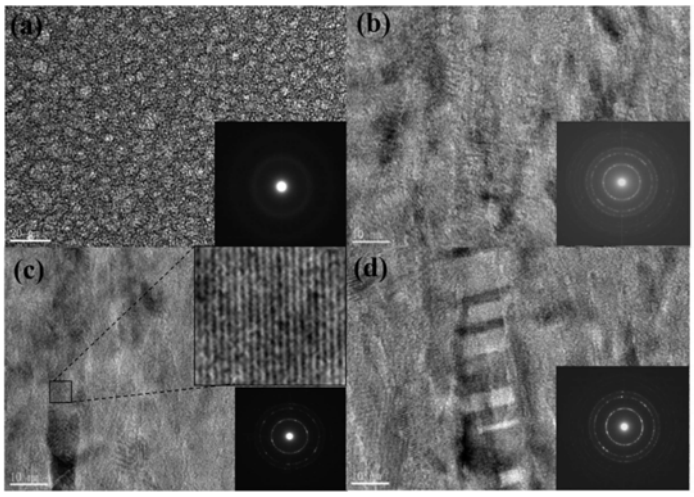

Fig. 25. HRTEM images and corresponding electron diffraction patterns (inset) of the middle crystallized layer in (a) a-Si:H films treated by hydrogen plasma for durations of 7(b) 15(c) and 30 minutes(d) [26].

Fig. 25 shows high-resolution TEM images of crystallized layer in the samples treated for 7, 15 and 30 minutes, respectively. Plus, the scale bars for Fig. 25(a) and Fig. 25(b-d) are 20nm and 10nm, respectively. The case of as-deposited film is included in Fig. 25(a), the diffraction pattern of it demonstrates the amorphous structure of the as-deposited film. The inset of Fig. 25(b) represents a variety of diffraction rings, indicative of poly-Si structure without a preferred orientation in the 7-min case. The inset of Fig. 25(d) shows 3 clear diffraction rings corresponding to the (111), (220) and (311) orientations respectively. It indicates that there is an increasing crystallinity of the crystallized layer.

Micro-Raman analysis in Fig. 26(a) demonstrates a gradual phase transition from completely amorphous to highly crystal phase. Considering the TEM experiments, the crystallinity is improved from 3% (as-deposited) up to 100% (30-min). A linear fitting is included in Fig. 26(b) giving an approximate crystallization ratio of ~0.033/minute.

For the possible etching of silicon layer during the crystallization due to the existence of H_2 plasma, researchers have reached an agreement that the competition between hydrogen insertion into the amorphous network and silicon etching by hydrogen exposure results in the occurrence of a hydrogen-rich surface layer with an ultimately steady thickness [26]. In addition, atomic hydrogen plays an important role in the transition of amorphous to microcrystalline silicon. When the growth surface is exposed to atomic hydrogen, there can be abstraction of hydrogen bonded to silicon which consequently creates dangling bonds. After the breakage of

weak silicon–silicon bonds, the Si–H bonds combine with the surface dangling bonds and diffuse into the film.

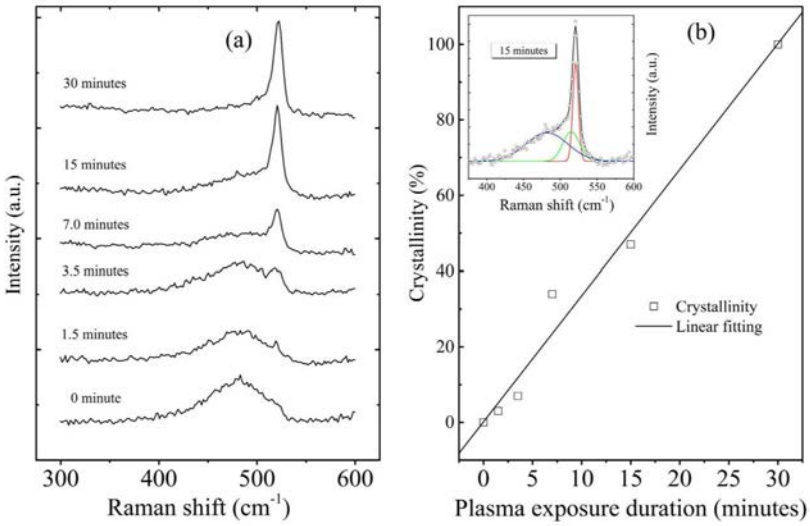

Fig. 26. Micro-Raman scattering spectra of the samples plasma-exposed for different durations (a) and the exposure duration dependent average crystallinity (b) (denoted as open squares) estimated from the Raman scattering spectra shown in (a) as well as the linear fitting (solid line) of the average crystallinity [26].

C-beam (Carbon nanotube electron beam) crystallization

Carbon nanotubes (CNTs) have superior properties such as high aspect ratio, chemical stability, long term stability and high current emission in electrical, thermal and mechanical parts. Thus, CNTs are strong and practical electron emitters for vacuum nano-electronic device applications. What should be noticed is that the property of emitting electrons can be used to crystallize the amorphous silicon layers.

S. W. Lee et al. presented a novel technique for crystallizing amorphous silicon at 300˚C by using CNT emitter that emits electrons from a structure based on the field emission principle [47]. They firstly fabricated CNTs vertically on silicon wafer with 60 μm in length. Then a triode beam exposure system with CNT emitters on the wafer was attached at the cathode and placed under the gate mesh. The distance between the cathode and the gate mesh was 150 μm. The CNT emitters are aligned with gate mesh electrode, and the gate mesh had a pattern structure. The bare silicon thin film on glass substrate was affixed at the anode by copper tape. (See Fig. 27.)

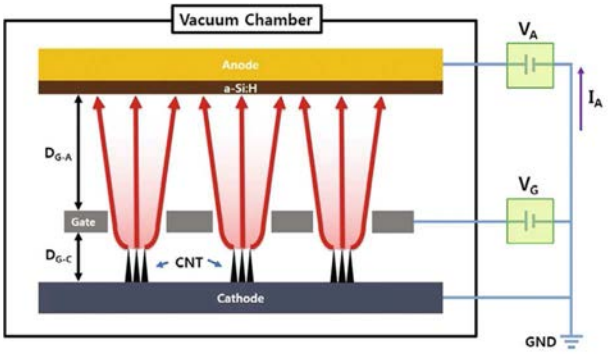

Fig. 27. Schematic diagram of C-beam exposure using a CNT emitter as a cathode [47].

After the set-up process, the chamber was set at a vacuum pressure of 10^{-7} Torr. Then the bias was applied to the triode system. Therefore, a locally-enhanced electric field near the CNT emitter was established, through the electric field, C-beam was generated and then crystallize the amorphous silicon. In addition, the substrate coated with a-Si is not necessary to heated up in C-beam crystallization, which makes it a low temperature crystallization technique.

Fig. 28 shows that after crystallization, the silicon film had a surface consisting of nano-sized grain boundaries. The grains of the nano-crystallized silicon thin film had a size distribution in the range of 10-30 nm.

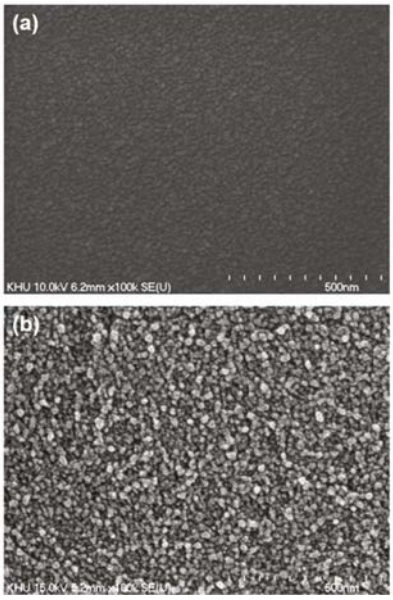

Fig. 28. High-resolution SEM images of silicon thin films: (a) before C-beam exposure and (b) after C-beam exposure [47].

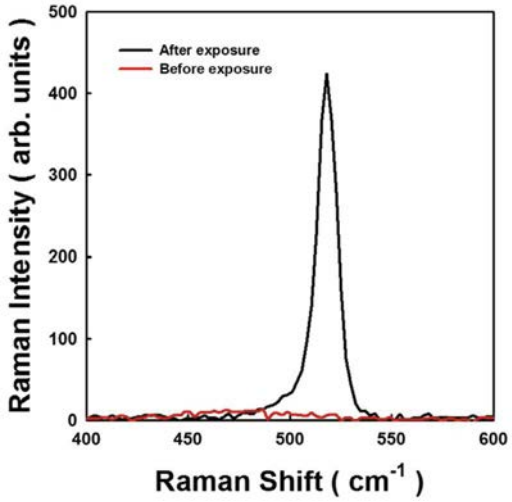

Fig. 29. Raman spectra from silicon thin films before and after C-beam exposure [47].

Fig. 29 presents Raman spectra to compare a a-Si:H film before (red line) and after (black line) C-beam exposure. The peak after exposure is at 518.4 cm^{-1}, this confirms that the C-beam-exposed area was transformed to crystalline structure.

The TFTs which were fabricated by C-beam crystallized silicon show max current of 10^{-4} A and on/off ratio of more than 10^{7}. And the linear mobility of the TFTs is of 20 cm^2/Vs when the gate voltage is of -34.0 V.

Blue Laser Annealing (BLA)

Although excimer laser annealing shows very good feasibility in crystallizing amorphous silicon, with good mobility and stability, it suffers from poor uniformity caused by unreproducible pulse energy [49]. For this reason, blue laser annealing (BLA) is promising as a new alternative approach. BLA works in the continuous wave (CW) mode at wavelength of 445 nm generally, the laser power can vary from several watts to several tens watts [48]–[50].

Fig. 30 shows the schematic of BLA system. From this figure we can notice the laser beam would scan the amorphous silicon surface column by column since the laser beam has a specific area and works under CW mode.

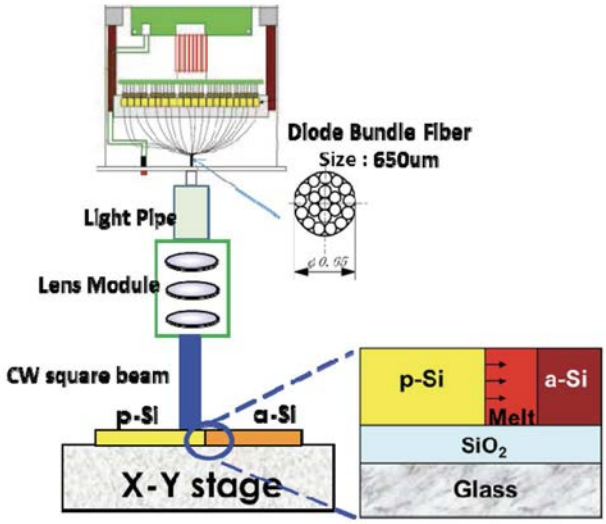

Fig. 30. The scheme of blue laser annealing equipment [50].

BLA has a penetration depth longer than that of UV excimer lasers (248-308 nm) due to the shorter wavelength of blue laser. This means the laser power must be chosen carefully to prevent the layers under amorphous silicon from melting, otherwise the possible flexible substrates will be exposed to danger of melting for the flexible electronics fabrication.

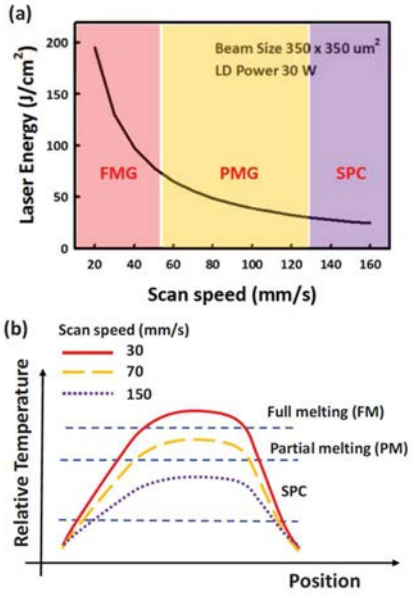

Fig. 31. (a) Laser energy as a function of scan speed of blue laser annealing system with laser diode (LD) power of 30 W. (b) The schematic laser energy profile for crystallization of the a-Si film [50].

From Fig. 31 we can see, at the same power of photo diode, the laser energy irradiated on the silicon is in function of scan speed. Fig. 31(b) shows the temperature profile into the a-Si layer with different scan speeds. Three different modes can be defined by the nature of the transition of crystals (full melting, partial melting and SPC, respectively).

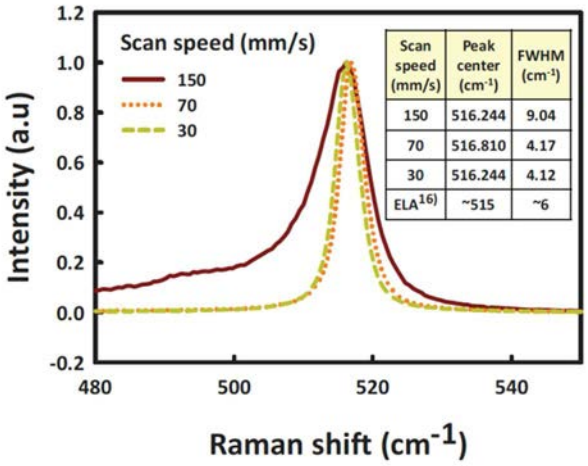

Fig. 32. Raman spectra as a function of laser scan speed for crystallization of blue laser annealed poly-Si film. The inset table shows the parameter of Raman scattering [50].

Subsequent Raman analysis illustrates more specifically the quality of crystallinity accomplished by three different scan speeds but at same power. From the table in Fig. 32 we can see under different scan speeds they all show clear peak centers at close to 521 cm^{-1}. Since smaller FWHM indicates better crystallinity, partial melting and full melting modes are better choices if we do not take thermal budget into account. Therefore, in order to crystallize a-Si at a relatively low temperature, we have to do trade-off between scan speed of laser diode and the crystallinity.

1.4 Conclusion

In this chapter, we reviewed two most important low temperature techniques that dedicated to deposition and crystallization of a-Si layer compatible for flexible substrates. These two technological processes usually define the highest process temperature among all the steps to build the devices that meet our requirements. Therefore, it is essential to have a general idea

about the advantages and disadvantages of these techniques when we try to develop an entire low temperature process for our devices.

First, the low temperature deposition techniques were reviewed. Reactive sputtering, hot-wire CVD and PECVD could all work at temperature as low as 300 ˚C. PECVD is more frequently adopted due to its good film uniformity and electrical properties of deposited films.

Second, different crystallization methods have been discussed. Mainstream methods like MIC and MILC were reviewed at first, some other approaches such as ELC, H_2 plasma induced crystallization, C-beam crystallization and BLA were presented afterwards. They all meet the limitation of temperature and show promising quality of crystallinity at the same time. Nevertheless, metal induced crystallization features more because of the easy realization. Especially indium induced crystallization could provide even lower crystallization temperature compared to the other metal materials.

Our work is to adopt proper techniques dedicated to low temperature electronics fabrication. For this case, many investigation and research would be carried out on whole process build and electrical characterization. All the techniques we reviewed could help us to better understand the context of low temperature process and improve the electrical properties of the devices we are about to fabricate.

Chapter 2

ICP-CVD TFT fabrication and characterization

2.1 Introduction of ICP-CVD (Inductively Coupled Plasma Chemical Vapor Deposition) technique

Unlike the other deposition techniques like LPCVD, PECVD, etc., inductively coupled plasma chemical vapor deposition (ICP-CVD) can offer several advantages such as higher density of plasma during the deposition and good homogeneous of deposited layers and lower process temperature [51], [52]. These advantages enable the possibility of depositing high quality thin film under relatively low temperature.

The ICP-CVD is operated by introducing inductively coupled plasma which is driven by a magnetic potential set up by induction coil located outside the chamber. The typical design of ICP-CVD system is shown in Fig. 33, in which the ICP coil controls the dissociation of plasma and density of incident ions in the chamber. The ICP coil is connected to LF generator whereas the lower electrode is connected to 13.56 MHz RF generator, which allows independent control of the bias voltage on the substrate.

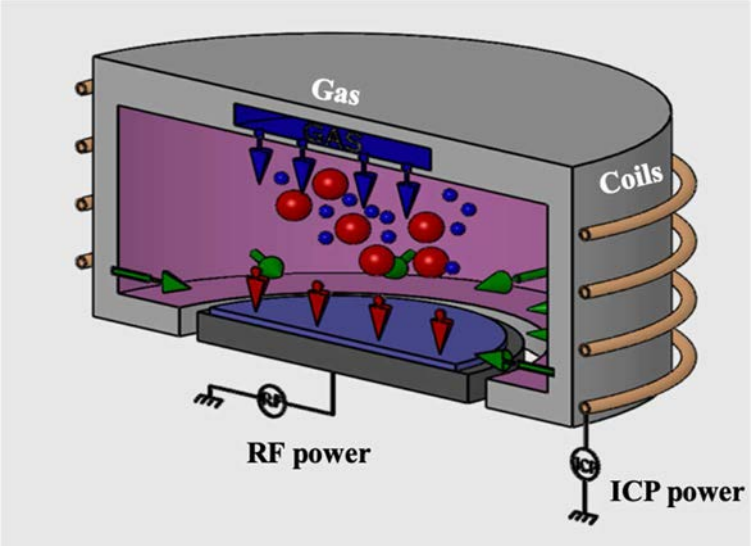

Fig. 33. Schematic of ICP-CVD system [53].

The equipment used in this work is Corial 210D ICP-CVD system. The composition of this system is illustrated in Fig. 34:

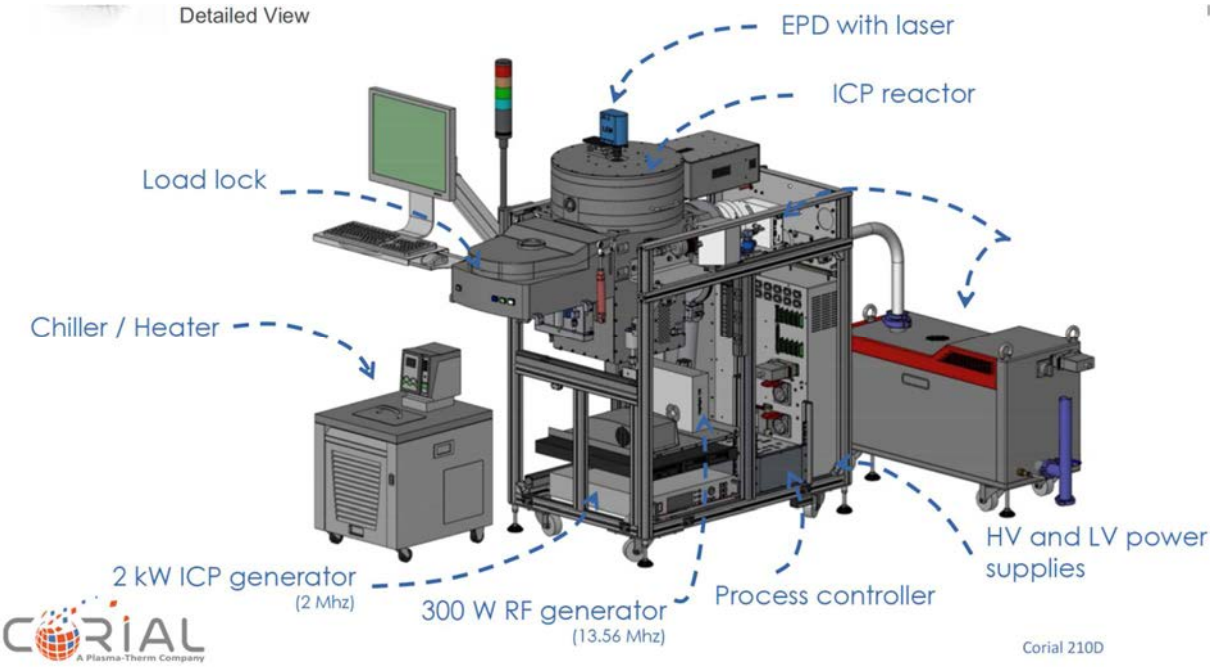

Fig. 34. Detailed view of Corial 210D ICP-CVD system [53].

Besides the reactor we mentioned before, the ICP generator and RF generator provide the bias during the deposition, chiller regulates the temperature of the chuck and EPD (electrophoretic deposition) allows us to monitor the deposited thickness of the films.

Although ICP-CVD has been adopted as one of the new deposition techniques in our lab and used in this thesis, the characteristics of these films need to be more explored and optimized.

As a good candidate for gate insulator in MOS (metal-oxide-semiconductor) transistors, SiO_2 has been widely researched under different CVD techniques. Since there are several advantages of ICP-CVD compared to the other CVD techniques, the electrical properties of ICP-CVD deposited SiO_2 should also be investigated. Few publications have reported the gap filling capability [51], C-V characteristics and breakdown field [54], [55] on SiO_2 films deposited by ICP-CVD. For instance, previous works reported -1.8V of flatband voltage [55] and 8.6 MV/cm of breakdown field [54] on ICP-CVD SiO_2.

Silicon layer is also an essential material for building either SiNWs based electronics or thin film electronics. Several structural researches on silicon deposited by ICP-CVD have been reported. These researches covered a complete silicon crystallinity: from amorphous silicon, nanocrystalline silicon [56], microcrystalline silicon [57] until polycrystalline silicon [58]. Due to the higher density of plasma in ICP-CVD, the deposition temperatures were all below 300 ˚C.

SiO_2 films were deposited with a fixed set of parameters during process, it is therefore not clear to see how different parameters can influence the electrical properties of deposited films. In addition, the bibliography on the electrical properties of deposited silicon layers is rarely found. Therefore, in this chapter, we firstly fabricated ICP-CVD MOS capacitors based on SiO_2 by modifying several key deposition parameters to evaluate and thus to optimize the SiO_2 deposition. Then, ICP-CVD TFTs were accordingly fabricated to characterize electrical properties of the ICP-CVD silicon layer and to complete the electrical characterization on ICP-CVD SiO_2.

2.2 Fabrication and characterization of ICP-CVD SiO_2 MOS capacitors

In this work, SiO_2 is not only used as material layer but also as an insulator for electronic devices. For this reason, electrical properties of ICP-CVD SiO_2 layers will be analyzed and optimized in this chapter.

In order to characterize ICP-CVD SiO_2 electrically, we fabricated MOS capacitors on silicon substrates. HFCV (High Frequency Capacitance Voltage) and I-V measurements were performed and several parameters such as flatband voltage and field breakdown were subsequently extracted. As mentioned, the research was carried out on the comparison of the results corresponding to different deposition parameters (LF and RF powers, pressure and temperature). In this way, the deposition parameters of SiO_2 would be optimized and be more adapted to serve as insulator in low temperature ($\leq$300 ˚C) electronic devices compatible with flexible substrates.

Research in this section is a two-step optimization. Several deposition parameters are tested for the first batch of capacitors and the optimized ones are set for the second batch of capacitors. For second batch, some other deposition parameters are tested to finish the optimization.

2.2.1 Principles of C-V curves of MOS capacitors in brief

The C-V measurements are carried out by applying the DC bias between gate (the metal) and the substrate (the semiconductor) (see Fig. 35). During the measurement the DC voltage will sweep from negative to positive and at the same time a small AC voltage with certain frequency is also applied on the gate. The capacitance is recorded through the measurement and then is plotted in function of the DC sweep voltage.

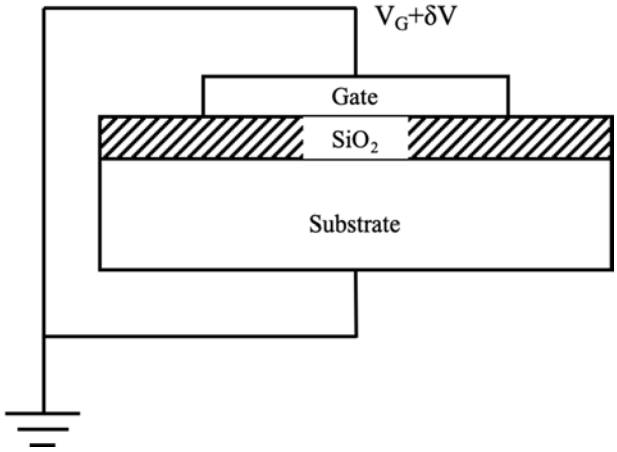

Fig. 35. Schematic of capacitance measurement setup.

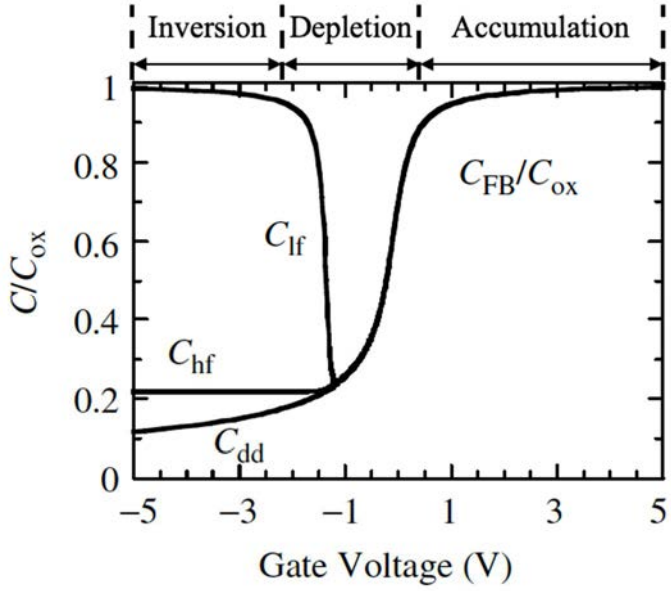

Fig. 36. Low-frequency (lf), high-frequency (hf), and deep-depletion (dd) normalized SiO_2-Si capacitance-voltage curves of a MOS capacitor with N-type substrate [59].

While the gate voltage sweeps from positive to negative (for N-type substrate case), the charges appearing at the SiO_2/Si interface at first are electrons which are majority carriers for N-type silicon. This refers to accumulation region shown in Fig. 36. When voltage keeps decreasing, the charges at the interface will be depleted, known as the depletion region. Until now, no deviation of the curves can be seen either for low frequency of high frequency C-V measurements, where low or high frequency refers to the frequency of the small AC voltage applied on gate. When entering into inversion region, if the frequency of the AC voltage is low

enough to allow the formed holes to respond to the AC voltage, then LFCV (low frequency capacitance voltage) curve is obtained. If the frequency is too high (normally up to 900 kHz) for the formed holes to follow, HFCV (C_{hf}) is obtained. The deep depletion curve (C_{dd}) would be obtained when DC voltage sweeps too fast, no matter how high or slow is the frequency of AC voltage.

The flatband voltage can be determined from HFCV curves. Since the capacitance increase for n-type substrate case is strongly related to transition from minority carriers to majority carriers, the approximate flatband voltage can be determined following the flatband capacitance method described in [60]:

$$C_{FB} = \frac{C_{OX}C_{SFB}}{C_{OX}+C_{SFB}} \quad (1)$$

$$C_{SFB} = \frac{\sqrt{2}A\varepsilon_S\varepsilon_0}{L_D} \quad (2)$$

Where C_{FB}, C_{OX} and C_{SFB} are capacitance in HFCV when applied voltage equals flatband voltage, oxide capacitance and substrate capacitance when MOS capacitor is in flatband state, respectively. A, ε_S, ε_0 and L_D are area of gate, relative permittivity of silicon, vacuum permittivity and extrinsic Debye length, respectively. Debye length can be calculated following the equation (3):

$$L_D = \sqrt{\frac{2kT\varepsilon_S\varepsilon_0}{q^2N_{sub}}} \quad (3)$$

Where k, T, q and Nsub are Boltzmann constant, temperature in Kelvin, elementary charge and doping level of substrate, repectively. Finally, flatband voltage can be determined from the corresponding C_{FB} in HFCV characteristics.

The occurrence of breakdown generally refers to the intrinsic breakdown of SiO_2 layer, more specifically, Fowler-Nordheim tunneling. When high field imposed across the oxide layer, which is necessary for tunneling (approximately in range of 7.5-10 MV/cm [62]), it results in a large density of electrons injected from silicon to SiO_2. This is illustrated in Fig. 37.

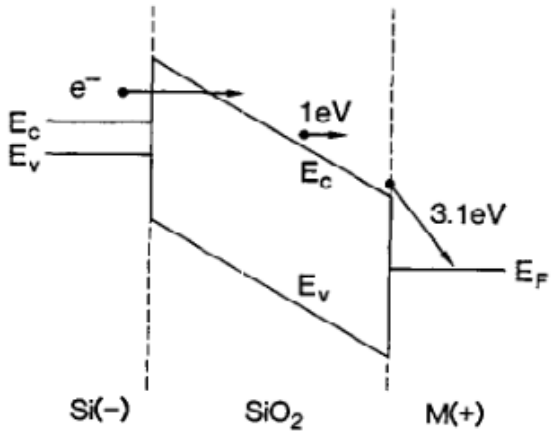

Fig. 37. Energy band diagram of the MOS system, during electron (e) injection from the silicon [63].

In Fig. 37, E_c and E_v represent the bottom of conduction band and top of valence band, respectively, E_F is the Fermi level. The electrons are injected from conduction band of silicon into SiO_2 conduction band as indicated by the arrows in the figure. This phenomenon will give a rise to the measured current and lead to a breakdown eventually.

The breakdown field is determined by: $E_{BF}=V_B/t_{SiO2}$. Where V_B and t_{SiO2} are breakdown voltage and thickness of SiO_2, respectively. The breakdown voltage is extracted from the I-V curve where corresponding measured current instantly rises up to 1uA in our case (seen as the breakdown happens).

2.2.2 First batch of MOS capacitors

The first batch of MOS capacitors was fabricated through one-mask process. Highest process temperature occurred during ICP-CVD of SiO_2. The cross-sectional schematic of capacitor is shown in Fig. 38.

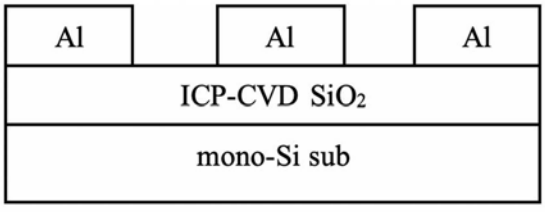

Fig. 38. Cross-sectional schematic of ICP-CVD SiO_2 MOS capacitor.

Fabrication process

First, the N-type mono-crystalline silicon wafers were RCA cleaned to remove contaminations and native oxide on the surface of the wafers. Second, SiO_2 layers with different thickness were deposited by ICP-CVD. Third, 300nm thick aluminum layers were thermally evaporated on SiO_2 layers. After photolithography, the samples were wet etched in aluminum etchant under 40 ˚C. At last, the forming gas (FG) annealing was implemented at 390 ˚C for 30 minutes. Each pad of aluminum electrodes has area of 0.81 μm^2, which can be considered as the area of the conducting plate of capacitors. Different combinations of deposition parameters of SiO_2 were selected and listed in following table.

From table 8 we can compare the electrical properties of SiO_2 in terms of LF power, RF power, deposition temperature and pressure. HFCV and breakdown test were performed on each sample by using Agilent semiconductor analyser-B1500A.

Table 8. Deposition parameters of ICP-CVD SiO_2 layers.

No. of sample	LF Power (W)	RF Power (W)	Deposition temperature (˚C)	Pressure (mTorr)	Thickness of SiO_2 (nm)
A	200	-	20	5	300
B	500	-	20	5	300
C	500	50	20	5	300
E	500	-	120	5	300
F	500	-	120	10	300
H	500	-	120	2.5	300
I	500	50	5	2.5	150
J	500	50	8	2.5	150
K	500	50	10	2.5	150
L	500	50	15	2.5	150
M	500	50	20	2.5	150

LF power comparison

In order to compare the different LF powers (200W and 500W in this batch), HFCV and breakdown field of sample A and B were compared and the results are shown in Fig. 39.

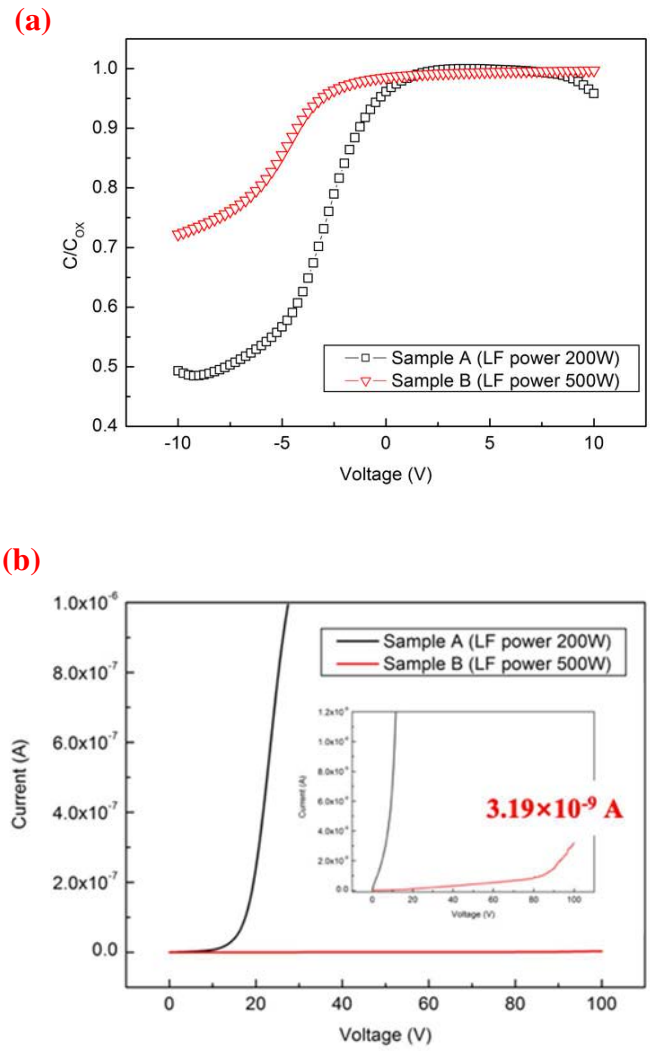

Fig. 39. (a) HFCV of sample A and B (with LF power of 200W and 500W, respectively); (b) breakdown test on sample A and B.

From Fig. 39(a) we can observe that HFCV for both sample A and B shows deep depletion when applied voltage decreases down to -10V. This is due to the fast sweep of the DC voltage. When we calculated the flatband voltage for both samples by using equation (1)-(3), we have -1.75V for sample A and -4V for sample B, respectively. It seems that sample A with LF power of 200W outweighs sample B due to its smaller flatband voltage because smaller flatband voltage indicates the easier reach of the voltage boundary of the strong inversion for MOS capacitors [60], [61]. Unfortunately, we observe a capacitance drop after 7V of the applied voltage on sample A, which implies higher trapped charges into the SiO_2 layer. This is also confirmed by the breakdown test in Fig. 39(b). Sample A sees a breakdown just at 20V of applied voltage, which shows the breakdown field (E_{BF}) is 0.67 MV/cm. In contrast to sample

A, sample B does not have a breakdown even the applied voltage reaches 100V (measured current is 3.19nA), which means sample B with LF power of 500W has the $E_{BF} \geq 3.3$ MV/cm. Therefore, combining the HFCV and breakdown test for both samples, when RF power is absent, capacitor with larger LF power as 500W provides better insulating property.

With/without RF power

Since the RF power is also an adjustable parameter in ICP-CVD system, it is important to evaluate the impact of the presence and the absence of RF power source. Therefore, sample B and C were compared in Fig. 40.

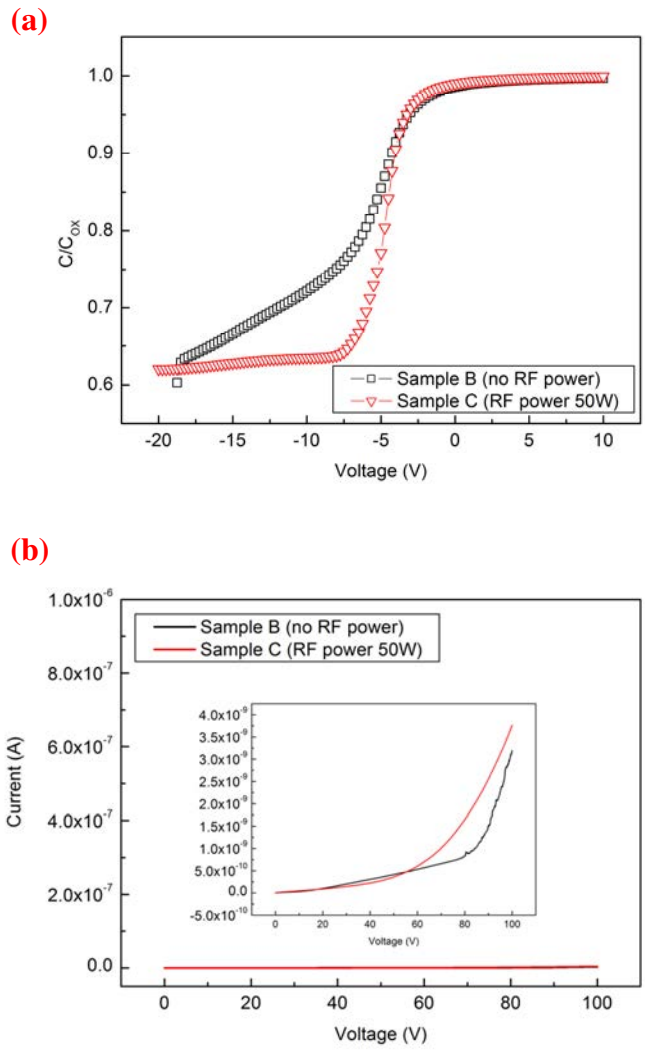

Fig. 40. (a) HFCV of sample B and C (B without RF power while C with RF power); (b) breakdown test on sample B and C.

The flatband voltage for both samples is -4V and the breakdown behavior of these two samples is coincidently similar since no breakdown occurred until the applied voltage reached 100V (the highest current for both samples is around 4nA in Fig. 40(b)). Even like this, the HFCV characteristics show big difference between these two samples in Fig. 40(a). HFCV of sample B in Fig. 40(a) shows a deep depletion region at the negative applied voltage whereas the HFCV of sample C shows the typical inversion region. This means under the same DC voltage sweep rate, the minority carriers of capacitor without RF power added (sample B) during deposition of SiO_2 could not respond in time to prevent the capacitance from decreasing when applied voltage decreases. Therefore, in order to have a faster transition from depletion region to inversion region, introducing RF power during SiO_2 deposition is necessary.

Pressure comparison

Pressure of deposition into the chamber is regulated at a certain value in the ICP-CVD reactor during the deposition process. It is also interesting to investigate how pressure would influence the electrical properties of SiO_2. For this purpose, different chamber pressures of 2.5 mTorr (sample H), 5 mTorr (sample E) and 10mTorr (sample F) were compared, for a higher deposition temperature chosen at 120 ˚C. Fig. 41 presents the results:

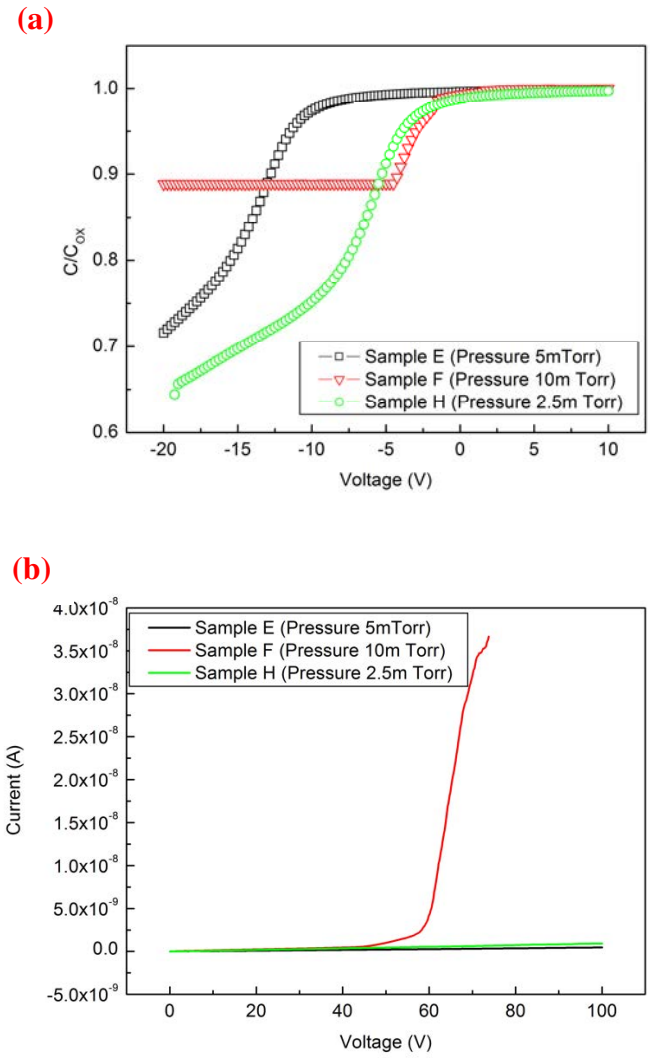

Fig. 41. (a) HFCV of sample E, F and H, with pressure of 5, 10 and 2.5mTorr, respectively (500W of LF power and 120˚C of temperature); (b) breakdown test on sample E, F and H.

Calculated flatband voltage for sample E, F and H is -12.25V, -3.5V and -4.9V, respectively. From Fig. 41(a) we can see although sample F (with deposition pressure of 10 mTorr) does not have depletion region as the other two samples and yields the smallest flatband voltage, only 0.1 of the relative capacitance (C/C_{OX}) drop indicates the massive defects existing into SiO_2 layer. This is confirmed by the breakdown test in Fig. 41(b) that the sample F broke down at the applied voltage of 70V (E_{BF}=2.3 MV/cm). In the contrary, sample E and H do not breakdown until 100V of voltage applied, which means the breakdown fields of these two samples are at least 3.3 MV/cm. By comparing sample E and H, sample H with deposition pressure of 2.5 mTorr is the best compromise since sample H has smaller flatband voltage than sample E. Therefore, 2.5 mTorr would be the optimized deposition pressure.

Deposition temperature comparison

Temperature in ICP-CVD system is substantially the temperature of the chuck on which the samples are put in the reactor during deposition. The deposition temperature was roughly compared between 20 ˚C and 120 ˚C in prior to smaller range of temperatures because it could reveal more obvious effect on larger temperature gap, which could be a good start for optimizing the deposition temperature.

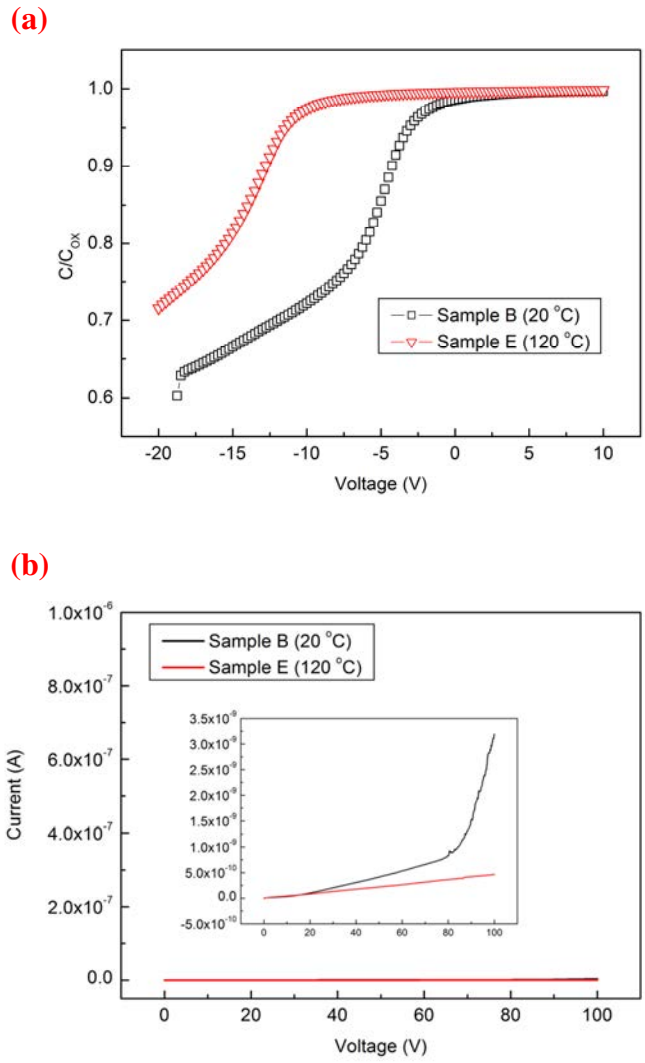

Fig. 42. (a) HFCV of sample B and E (with temperature of 20 and 120 ˚C, respectively); (b) breakdown test on sample B and E.

From Fig. 42(a) we can easily notice the flatband voltage difference, the flatband voltage for sample B and E has been calculated before, which is -4V and -12.25V, respectively. By observing Fig. 42(b), even the measured current for sample B is almost 10 times than that of

sample E when applied voltage reaches 100V, the highest current is around 3.5nA, which is still in a low level. In other words, both samples do not show breakdown until the applied voltage is 100V, which indicates E_{BF}≥3.3 MV/cm. Therefore, sample B with lower flatband voltage holds better electrical properties, which also shows that 20 ˚C as the deposition temperature is better compared to 120 ˚C.

From the results above, the optimized parameters that we have decided to use for the rest of the process are LF power of 500W, RF power of 50W and pressure of 2.5mTorr. Sample I to N were thus fabricated by playing temperature in a narrower range between 5˚C and 20 ˚C. The results were shown in Fig. 43.

From Fig. 43(a), the HFCV characteristics of these capacitors overlap to a large extent, which could be explained by the small variation of the temperatures. Nevertheless, some deviations can still be observed when the capacitances increase from inversion to accumulation region. Flatband voltage for sample I to M is -1.59V, -2.6V, -2.3V, -2.25V and -3.25V, respectively. Interestingly, the flatband voltage increases from -1.59V to -3.25V when deposition temperature increases from 5 ˚C to 20 ˚C, while the flatband voltage for 8-15˚C case has a reverse trend. Since the flatband voltage difference for 8-15 ˚C case is so subtle, we can still consider that the flatband voltage would decrease with the deposition temperature decreasing. When we take a look at the breakdown test in Fig. 43(b), measured current start to increase from applied voltage of 60V, stop at around 35nA for all samples. This means no significant breakdown occurs when voltage reaches 60V, indicating E_{BF}≥4 MV/cm (consider the thickness of SiO_2 of these samples is 100nm). When we take these results into account, depositions developed at 5 ˚C perform best. One should be noticed that although 20 ˚C of the temperature has higher flatband voltage, the difference of flatband voltages under different temperatures is not significant. Since the capacitor fabricated at 20 ˚C can already yield good electrical property, 20 ˚C can be an optimized temperature. In addition, 20 ˚C is closer to room temperature, which is easier to regulate and maintain compared to the other lower temperatures.

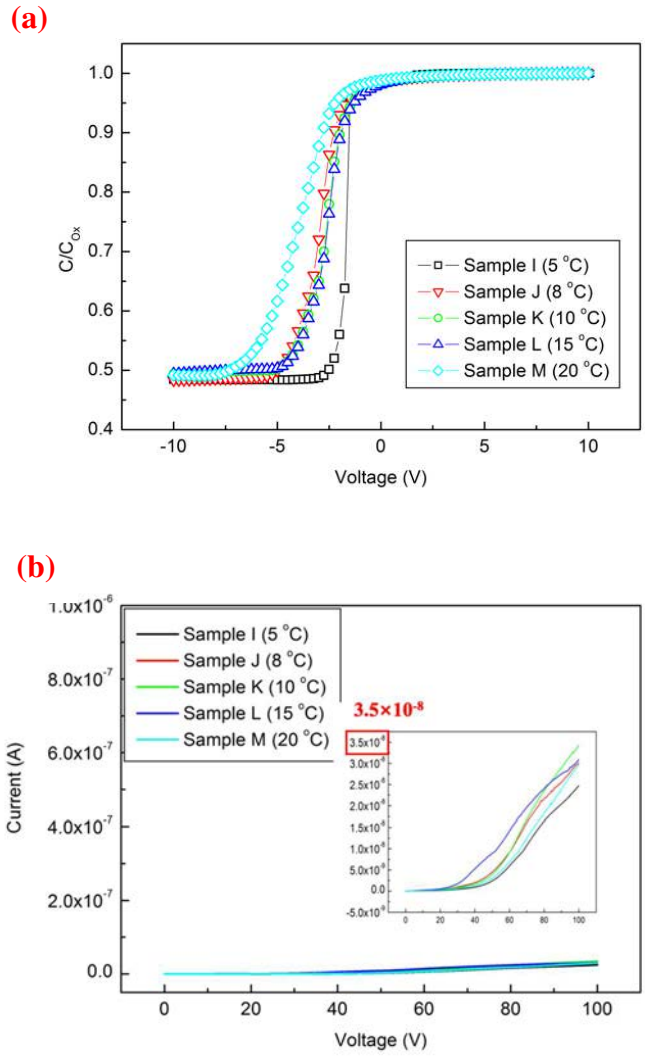

Fig. 43. (a) HFCV of sample I to M (with temperature of 5, 8, 10, 15 and 20 ˚C, respectively); (b) breakdown test on sample I to M.

After comparing the first batch of capacitors, we can obtain the optimized parameters of fabricating ICP-CVD SiO_2 capacitors, which are 500W of LF power, 50W of RF power, 2.5mTorr of pressure and 20 ˚C of temperature. Further research on optimizing the deposition of SiO_2 continued more in detail and the results will be presented in the following part.

2.2.3 Second batch of SiO_2 MOS capacitors-detailed comparison

RF power was only investigated by adding or not into the deposition process before, so it will be interesting if we dig more on RF power in second batch of capacitors. LF power will also be investigated again by trying more possibilities on new batch of capacitors. In addition, forming gas (FG) annealing effect will be discussed as well in this section.

The fabrication of the new batch of capacitors followed the same structure depicted in Fig. 38 and the fabrication process except for FG annealing remained same. This time the temperature of FG annealing was adjusted to 200˚C from 390˚C because lower FG annealing temperature would be compatible with flexible electronics fabrication. The details of each important parameter involved in the fabrication process are listed in table 9. To eliminate any ambiguity, the samples in second batch were re-ordered from A to R. Therefore, in this section, the number of the samples mentioned will be for the new samples.

Table 9. Deposition parameters of 2nd batch of ICP-CVD SiO_2 layers.

No. of sample	LF Power (W)	RF Power (W)	Temperature (˚C)
A	200	-	20
B	500	-	20
C	700	-	20
D	900	-	20
K	500	80	20
L	500	80, ramp-up	20
M	500	50, ramp-up	20
O	500	40, ramp-up	20
R	500	30, ramp-up	20

Since the pressure has been well optimized, all the samples in second batch used 2.5mTorr as the pressure. In addition, all deposited SiO_2 have the same thickness of 100nm.

The capacitors were characterized by performing HFCV measurements and breakdown tests as we have done on the first batch of capacitors. We first present the results on samples without annealing, while at last we will show the FG annealing effect on optimized samples.

LF power comparison

LF power has been compared in last section but with only two different powers. In this section, larger LF powers (>500W) were compared to have detailed information on optimization. Fig. 44 shows the results of HFCV and breakdown tests.

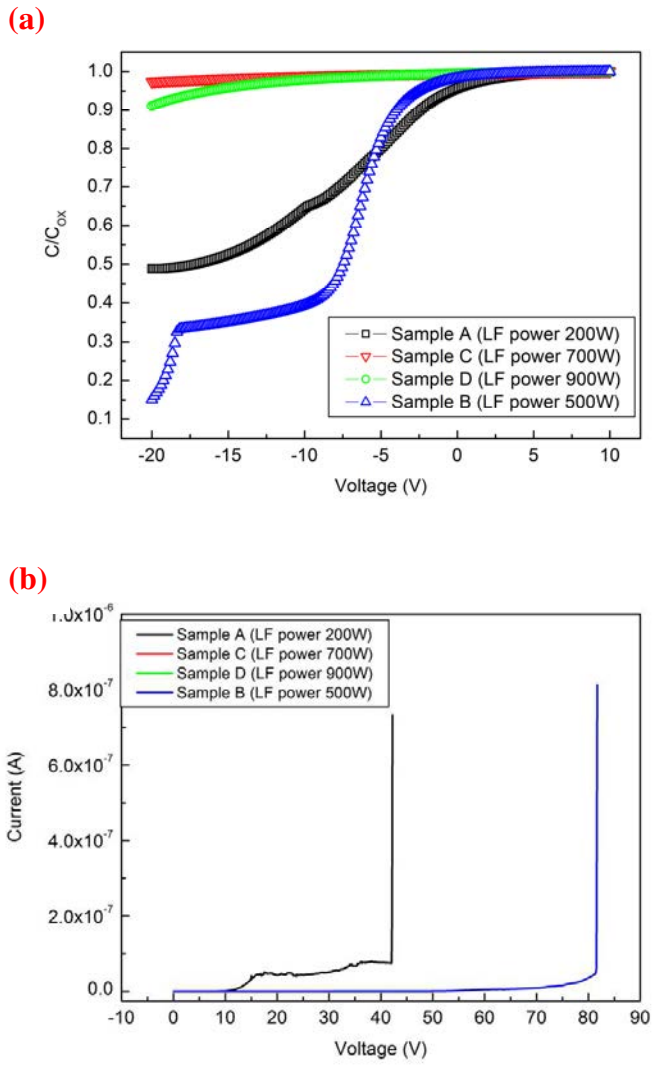

Fig. 44. (a) HFCV of sample A, B, C and D at 20 ˚C (with LF power of 200W, 500W, 700W, and 900W, respectively); (b) breakdown test on the same samples.

From Fig. 44(a) we can see that the HFCV curves of sample C and D are almost flat (close to C_{OX}), which means the silicon near the SiO_2/Si could not be inverted. This accordingly shows that the insulation of SiO_2 layers in these samples is really inferior. Although both sample A and B have clear transition from accumulation region to inversion region, the transition of sample A is much slower than that of sample B. Even the flatband voltage of sample A (-4.3V) is smaller than sample B (-5V), the slow transition would not be tolerated when the corresponding SiO_2 is used as the insulating layer in TFT fabrication. In addition, sample A

tends to breakdown more easily, yielding breakdown field of 4 MV/cm, which is only half of sample B (Fig. 44(b)). The breakdown curves of sample C and D are invisible since they coincide with the curve of sample B until 50V of applied voltage (which is the end voltage of breakdown test for sample C and D). Therefore, sample B is the best compromise among these samples, which means 500W is still the optimized LF power even larger powers were tested.

Constant RF power comparison

In order to optimize the properties of SiO_2 layers, different RF powers are thus researched in details. Since higher RF power would lead to higher energy of the plasma which could introduce potential damage to the deposited layer, the RF powers were confined under 80W. Moreover, the way to apply RF power during the deposition process is also an interesting variable which could cause different qualities of deposited layers. For example, the normal way to apply RF power is to increase the power to set value instantly and hold the power constantly during the whole deposition process. The other way is the "ramp-up" of RF power which means increasing the RF power gradually to the target value. All these ways would be discussed in this section.

First of all, same RF power (80W) but applied in different manners were researched. The results are shown in Fig. 45:

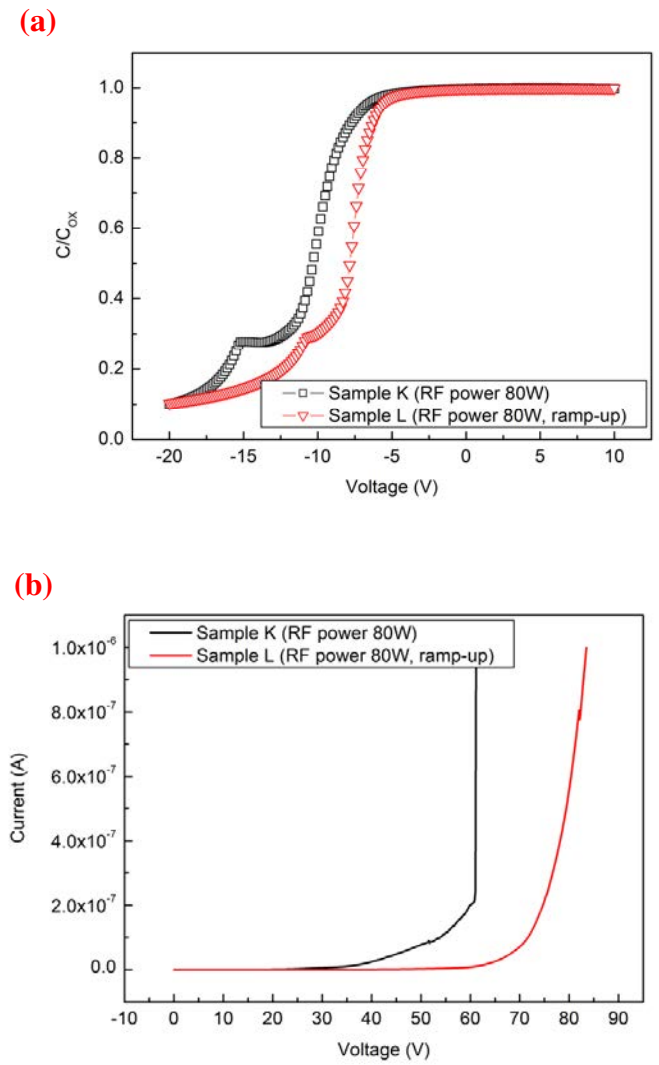

Fig. 45. (a) HFCV of sample K and L at 20 ˚C (with the RF power held constantly and increased gradually, respectively); (b) breakdown test on the same samples.

By comparing the flatband voltage for both samples in Fig. 45(a), the capacitor with the ramped RF power (sample L) shows smaller flatband voltage of -6.85V compared to that of -8.9V of the capacitor with constant RF power. Furthermore, larger breakdown field of 7.5 MV/cm can be obtained for the ramped RF power case, which is 1.5 MV/cm larger than that of constant RF power case (see Fig. 45(b)). These results indicate that the better way to apply RF power during the deposition is to increase the power gradually rather than keeping it constantly.

Ramp-up RF power comparison

After the comparison between constant and ramped RF power, samples with different ramped RF powers were tested and compared. The results are presented in Fig. 46.

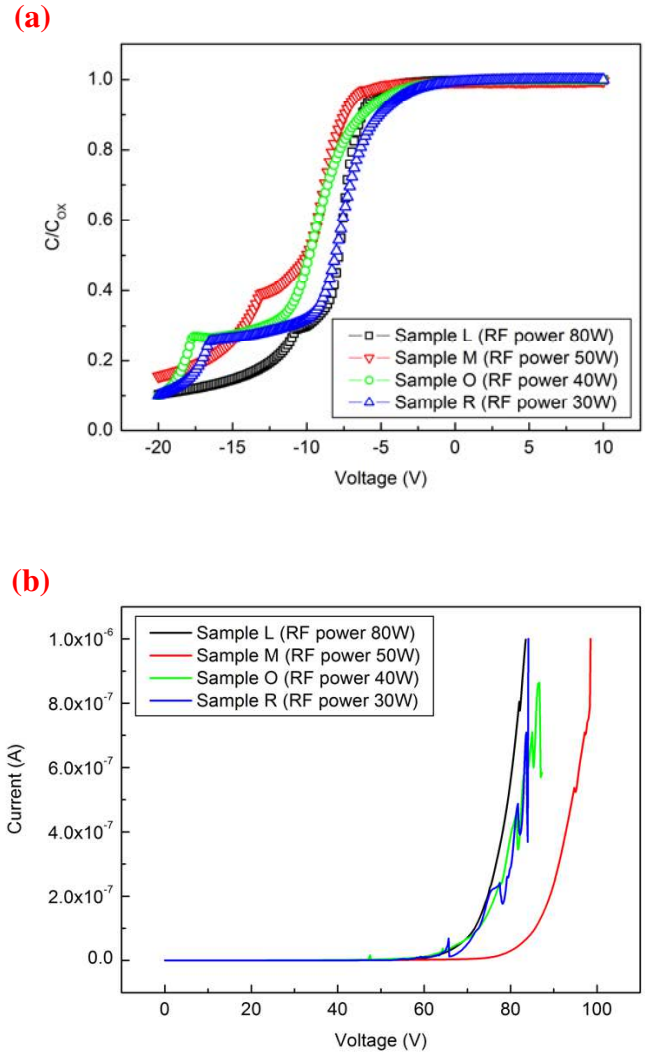

Fig. 46. (a) HFCV of sample L, M, O and R at 20 ˚C (with ramp-up RF power of 80W, 50W, 40W and 30W, respectively); (b) breakdown test on the same samples.

From Fig. 46(a), no consistent tendency of HFCV can be summed up with increase of ramped RF powers in terms of flatband voltage. The flatband voltage for sample L, M, O and R are -6.85V, -7.8V, -7.85V and -6.6V, respectively. The lowest RF power of 30W (sample R) shows almost the same flatband voltage as the highest RF power which is 80W (sample L). The performance in terms of flatband voltage slightly decreases when ramped RF power is within the range between 30W and 80W. Nevertheless, the flatband voltage differences are less than 1.3V according to the HFCV curves. When we consider the breakdown field in Fig. 46(b), they are extracted from the curves and listed together with the flatband voltage of each sample in table 10. Since the breakdown field of the capacitor for 50W case (sample M) is at least 1.5

MV/cm larger than the other capacitors as we can observe from Fig. 45(b), the best compromise is 50W of the ramped RF power. Nevertheless, we have to admit that the differences among these samples are subtle.

Table 10. Flatband voltages and breakdown fields for sample L, M, O and R (ramped RF powers for these samples are 80W, 50W, 40W and 30W, respectively).

	Sample L	Sample M	Sample O	Sample R
Flatband voltage (V)	-6.85	-7.8	-7.85	-6.6
Breakdown field (MV/cm)	~7.6	~9.5	~8	~8

The forming gas annealing effect

The new batch of capacitors were fabricated and annealed in forming gas (N_2/H_2=90%/10%) at 200 ˚C for 30 minutes, with the objective to fabricate high quality TFTs at low temperature and build electronic devices on flexible substrates.

Therefore, the effect of relatively low temperature forming gas annealing should be validated. Sample B (LF power of 500W) was chosen to compare the HFCV characteristics and the breakdown field before and after FG annealing. The results are shown in Fig. 47.

From Fig. 47(a) we can see after FG annealing, the HFCV curves shifts towards positive applied voltage, indicating better performance on flatband voltages. Here the calculated flatband voltage decreased from -5V to -2.05V. Such FG annealing is commonly used in classical silicon technology to reduce the contact resistances between aluminum pads and silicon layers, this annealing might probably also cure some defects at the SiO_2/Si interface leading to better flatband voltage of the capacitors. On the other hand, the breakdown field of annealed capacitor is inferior to the same capacitor just before the FG annealing, which is ~8.1 MV/cm and ~7.5 MV/cm, respectively (see Fig. 47(b)). Since the degradation of the breakdown field is less than 7.5%, it could be neglected.

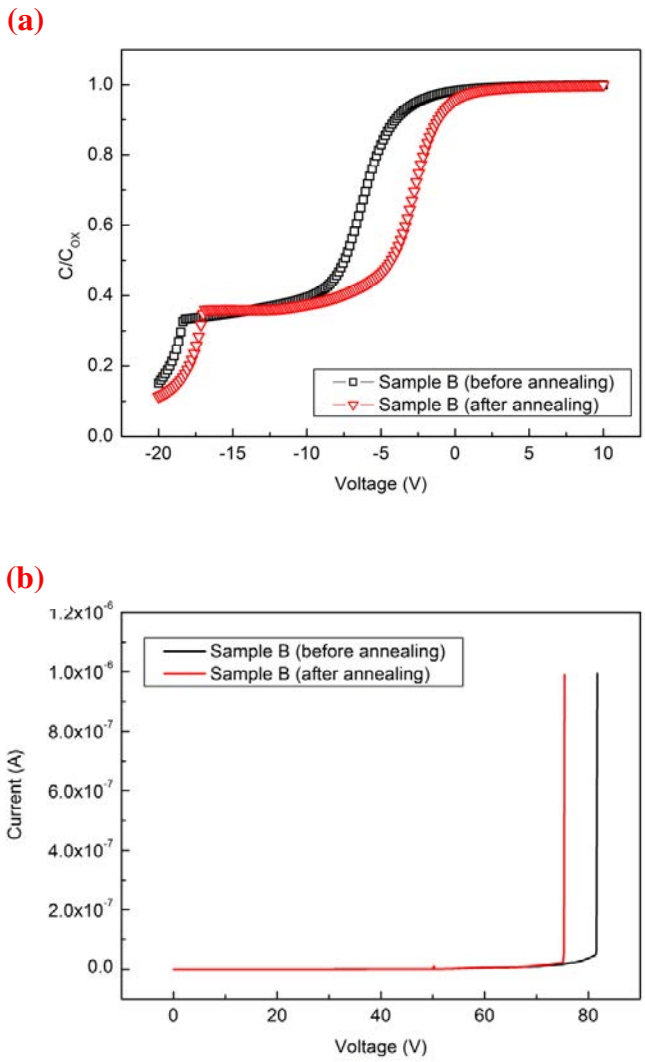

Fig. 47. (a) HFCV of sample B before and after forming gas annealing (with LF power of 500W and temperature of 20 ˚C, respectively); (b) breakdown test on the same samples.

In order to have a perspective on the breakdown field of optimized ICP-CVD MOS capacitors, we compare breakdown field of ICP-CVD MOS capacitors with the MOS capacitors which SiO_2 layers were deposited by the other techniques and show in table 11:

Table 11. The breakdown field comparison of SiO_2 MOS capacitors with its SiO_2 layers deposited by different techniques.

Deposition techniques	Breakdown field (MV/cm)	Process temperature (˚C)
Thermal oxidation [64], [65]	10-30	900-1100
APCVD [66]	4.7-5.9	300-450
LPCVD [67], [68]	5-10	650-950
PECVD [69]–[71]	3-9	250-440
Sputtering [72], [73]	2-8	80-200
Our results	2.3-9.5	5-120

Through table 11 we can conclude, at much lower process temperature (5-120 ˚C), ICP-CVD MOS capacitors can yield comparable breakdown fields to the other deposition techniques.

2.2.4 Conclusion

ICP-CVD SiO_2 MOS capacitors have been fabricated for two batches with several parameters changed and each sample with capacitors has been characterized by performing HFCV and breakdown test. After comparing these samples, the parameters which lead to better electrical properties of the ICP-CVD SiO_2 based capacitors are determined. LF power of 500W, RF power of 50W, pressure of 2.5mTorr and temperature of 20 ˚C have been validated as the best combination of the deposition parameters. In addition, the ramp-up of RF power will also improve the performance of capacitor in terms of flatband voltage. At last, forming gas annealing with lower temperature (200 ˚C) has been confirmed as an effective way to continuously improve the electrical quality of SiO_2 layers.

2.3 ICP-CVD Thin Film Transistors (TFTs)

ICP-CVD has been proved an appropriate technique to deposit good SiO_2 insulating layers at low temperature (≤220 ˚C). Besides SiO_2 which can act as insulating layer in TFT, ICP-CVD can also be used to deposit active layer like microcrystalline silicon. Therefore, to fully implement the ICP-CVD and to take advantage of this deposition technique, TFTs with both active layer and insulating layer deposited by ICP-CVD have been fabricated and characterized.

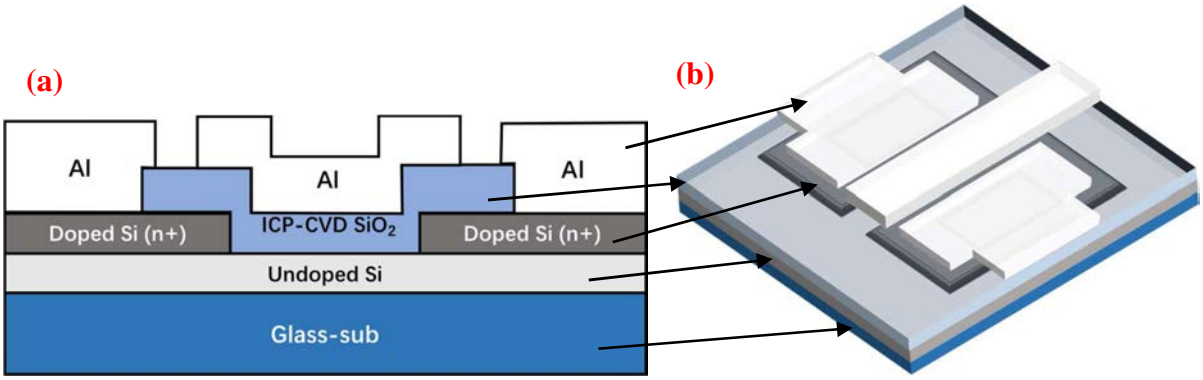

Fig. 48. (a) 2-D cross section schematic of ICP-CVD top gate TFT; (b) related 3-D schematic of the same TFT.

Fig. 48(a) shows the cross-sectional schematic view of the fabricated N-channel top gate silicon TFT on glass substrate. The active layer, source/drain and gate oxide were all deposited by ICP-CVD during the fabrication of TFT. Fig. 48(b) shows the corresponding 3-D schematic of the TFT.

2.3.1 Fabrication process

Fabrication followed a classical three-mask process. First, a 100 nm thick undoped μc-Si layer and a 100 nm thick n-type *in-situ* doped μc-Si (the characterization of crystallinity is shown afterwards in Fig.49) layer were deposited consecutively in ICP reactor, using silane (SiH_4) as precursor gas and phosphine (PH_4) as doping gas. During deposition of *in-situ* doped μc-Si film, substrate temperature reached 180 ˚C. Then, the source/drain areas were patterned by first photolithography and following RIE (Reactive Ion Etching) etched the n-doped layer by using SF_6 plasma. Second, a 100 nm thick SiO_2 as the insulating layer was deposited in ICP reactor following parameters optimized in 3.2. In order to pattern the gate insulator, the second photolithography was performed after the deposition, followed by the RIE of SiO_2 under CF_4 plasma. At last, a 300 nm thick aluminium layer which acts as the electrode material was evaporated onto the patterned SiO_2 layer. Following the third photolithography and wet etching of aluminium, the TFTs underwent both the forming gas annealing and the thermal annealing. Forming gas annealing was performed first at 200 ˚C in hydrogen and nitrogen ambience with

the H_2/N_2 ratio of 10%/90%. A second thermal annealing was performed afterwards at around 220 ˚C expected to yield better electrical properties. The parameters of both forming gas annealing and thermal annealing are summarized in table 12.

Fabricated TFTs were electrically characterized by collecting I-V curves using an Agilent B1500A semiconductor analyser.

Table 12. Parameters of performed forming gas annealing and thermal annealing.

	Forming gas annealing	Thermal annealing
Temperature	200 ˚C	~220 ˚C
Gas flow	N_2 1800 sccm, H_2 200 sccm	N_2 70 sccm
Pressure	atmospheric	0.9 mbar
Duration	30 mins	120 mins

Raman analysis was carried out to characterize the crystallinity of deposited silicon layer.

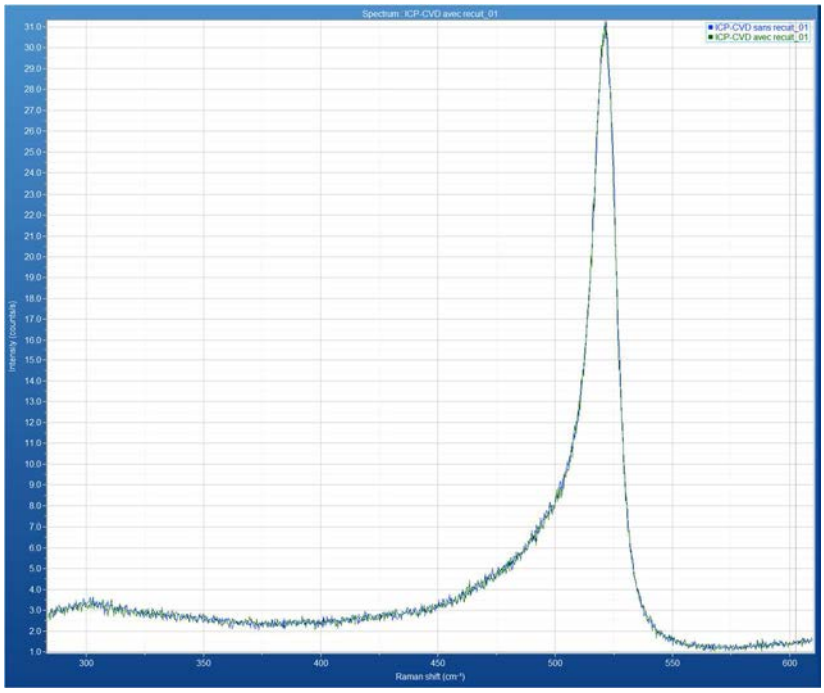

Fig. 49. Raman spectrum of ICP-CVD silicon

From the Raman spectrum we can see a clear peak located at ~520 cm^{-1}, which indicates a good crystallinity. The crystalline fraction according to this measurement is 75%.

2.3.2 Electrical properties of fabricated TFT

The transfer characteristics of TFT before undergoing any annealing process are presented in black curve in Fig. 50, Electrical parameters of the TFT as threshold voltage (V_{TH}), field effect mobility (μ) and subthreshold slope (S) were then extracted. Threshold voltage and field effect mobility are determined following the simplified electrical conduction model of the MOSFET [61]. In this way, V_{TH} is deduced by the intersection with the gate axis of the linear interpolation of the drain current with gate voltage curve, and field effect mobility is estimated from the maximum value of the transconductance, plotted in the linear mode. The subthreshold slope is checked from the reverse slope in the switching region of the transfer characteristics plotted in a semi-log-scale. Values of electrical parameters reported in table 13 reveals poor electrical properties of TFT related to bad quality of both active layer and SiO_2-active layer interface. In this way, in order to improve the electrical properties of fabricated TFT, device was thermally annealed in forming gas to improve quality of SiO_2 gate insulator and the contact resistances, and followed by a thermal annealing in nitrogen ambience at 220 ˚C during 2 hours (parameters see table 12) to improve interface and active layer qualities.

Compared to the black counterpart, the red transfer characteristics curve which represents the same device after performing annealing shows two decades higher in drain current level. This result can be attributed to two phenomena: the decrease of contact resistances at source and drain electrodes, and also to the improvement of active layer and interface qualities.

Table 13. Electrical parameters of ICP-CVD TFT under different stage of annealing process

Parameters	TFT without annealing	TFT with FG and thermal annealing
Threshold voltage (V)	5.6	3.7
I_{ON}/I_{OFF}	8.1×10^2	6.4×10^2
Field effect mobility (cm^2/Vs)	0.02	1.2
Subthreshold slope (V/dec)	4.4	3.9

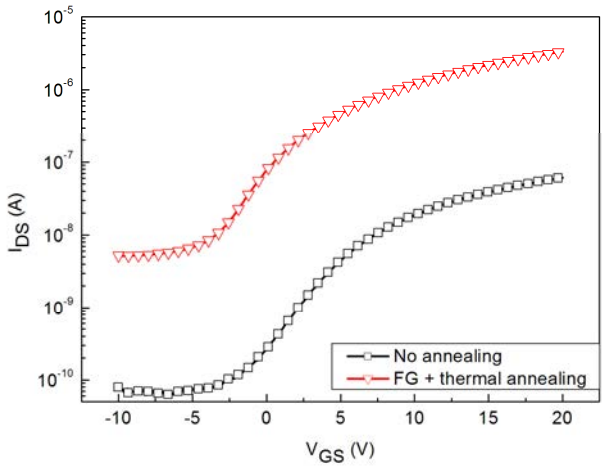

Fig. 50. The transfer characteristics of the same TFT with W/L=450µm/80µm and V_{DS}=1V, at different stage of annealing: black curve represents for TFT without any annealing and red one is with FG annealing at 200˚C and thermal annealing at 220 ˚C consecutively.

More specifically, the contact resistance is strongly related to the existence of the defects at the interface between aluminum layer and doped silicon layer (source/drain regions). Assuming that contact resistances (R_C) at source (R_S) and drain (R_D) regions are identical (see (Fig. 51)) in the linear mode, and neglecting the field effect mobility degradation, thus R_C is determined from the channel resistance (R_{DS}) following: [74]

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = 2R_C + \left(\frac{1}{\mu C_{OX}}\frac{L}{W}\right)\frac{1}{V_{GS}-V_{TH}} \qquad (4)$$

where C_{OX} is the oxide capacitance per unit area of the transistor, W and L the width and the length of the channel respectively. Then, extrapolated values of RC from the linear interpolation of the R_{DS}= f($1/V_{GS} - V_{TH}$)) plot with the R_{DS} axis (see. Fig. 52) are 222.5kΩ and 17.8kΩ for non-annealed and annealed TFT respectively. This lower value of the contact resistance for the annealed device (more than one decade) explains the significant increase with the same ratio from Off- to On-state of the drain current of the transfer characteristics plotted in Fig. 50 of the device submitted to FG annealing. Indeed, in case of TFT, FG annealing is generally believed to heal the defects existing at the interface of aluminum layer and undoped silicon layer to minimize contact resistance effect and thus to increase the drain current level.

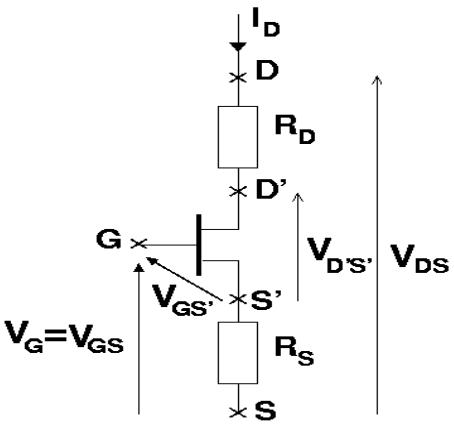

Fig. 51. Equivalent electrical model of the transistor taking into account the contact resistances.

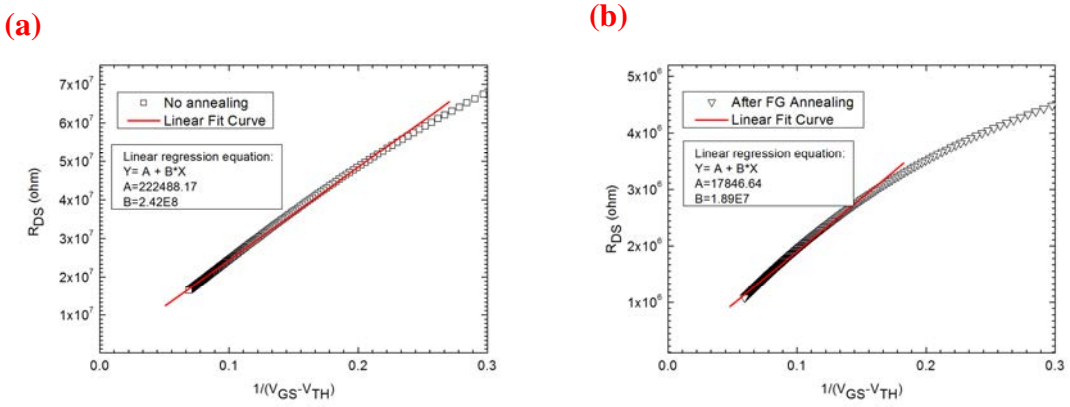

Fig. 52. Plots of the channel resistance in function of the reverse of the effective gate voltage ($V_G^* = V_{GS'} - V_{TH}$) for: (a) no annealed TFT, (b) FG annealed TFT.

Electrical parameters deduced from the transfer characteristics of the same TFT after going through the two thermal annealing are reported in table 13. By comparing threshold voltage and subthreshold slope before and after performing two annealing processes, they both see decrease. In addition, the calculated field effect mobility (1.2 cm^2/Vs) is almost 60 times higher after two thermal annealing. Such relatively low value is comparable for TFTs fabricated using other low temperature thin films deposition technologies [75]–[77], but still reveals poorer crystal quality of the silicon thin layer compared to higher temperature fabrication process.

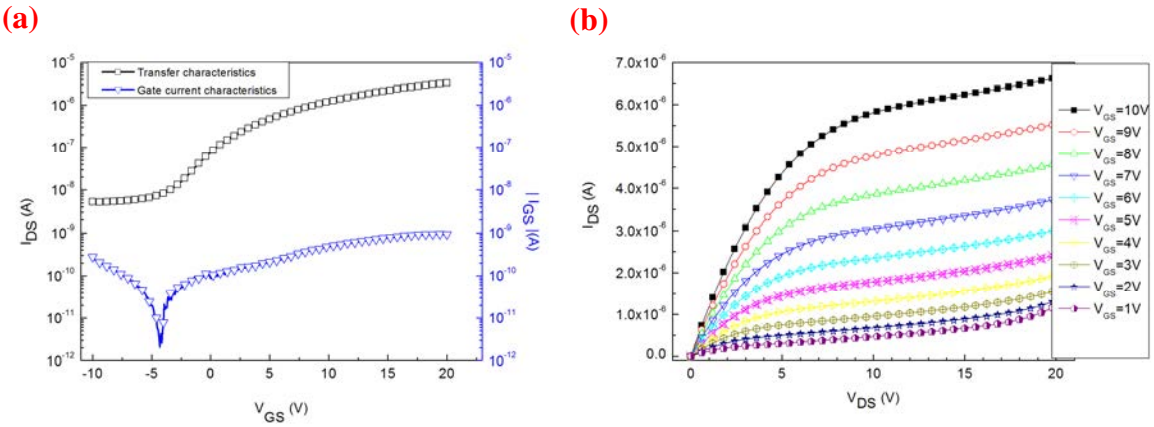

Fig. 53. (a) Transfer characteristics and gate current characteristics of TFT with W/L=450µm/80µm after two annealing processes (V_{DS}=1V); (b) Output characteristics of the same TFT measured under VGS set from 1 to 10V for 1V as the step.

The transfer characteristics and gate current of the TFT undergoing two annealing processes are plotted in Fig. 53(a). For applied gate voltage exceeding V_{TH}, the gate current that can also be noted as leakage current is at least 3 decades lower than On-state drain current. In addition, the gate current does not exceed 1nA when gate voltage is up to 20V, which reveals quite good gate insulation. Furthermore, the corresponding output characteristics plotted in Fig. 53(b) show distinguishable linear region and quasi-saturated region. This indicates a good ohmic contact between the electrodes and the drain/source regions and good field effect. One can conclude is that the TFTs processed under low temperature (≤220 ˚C) ICP-CVD technology yield promising electrical properties, following a lower cost process flow in comparison to other work, in particular in terms of dopant activation for source and drain regions [78].

As mentioned earlier, electrical properties of these TFTs are strongly related to the active layer and interface qualities. In this way, energy distribution of defects into the bandgap at the interface and into active layer will be discussed in the following section.

2.3.3 Energy distributions of defects into the bandgap

Theoretical model of Suzuki

Two main complementary approaches were previously established to determine the energy distribution of states in amorphous or polycrystalline silicon TFTs. Methods are based on the analysis of the field-effect conductance using analytical methods [79] or temperature

measurements of the current [80], or others combining both [81]. In our case, energy distribution of defects is determined from the transconductance ($G = \partial I_{DS}/\partial V_{GS}$) characteristics of the transistors by using the incremental method of Suzuki [79].

The model classically used to determine the desity of states (DOS) into the bandgap related to defects density into the active layer follows:

$$N_{DOS}(E_F + q\Psi_S) = \frac{\varepsilon_{Si}}{2q^2}\frac{\partial^2}{\partial {\Psi_S}^2}\left[\frac{d\Psi(x)}{dx}|_{x=0}\right]^2 \qquad (5)$$

Where $\frac{d\Psi(x)}{dx}|_{x=0}$ stands for the electric field at the SiO_2/Si interface and

$$\frac{d\Psi(x)}{dx}|_{x=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\frac{V_{GS}-V_{FB}-\Psi_S}{d_{ox}} \qquad (6)$$

Here E_F refers to the Fermi level, Ψ_S to the potential at the SiO_2/Si interface，ε_{Si} the dielectric constant of the silicon, ε_{ox} the dielectric constant of the oxide, d_{OX} the thickness of the gate oxide, V_{FB} the flatband voltage (taken at the minimum current of the transfer characteristics, i.e. $\Psi_S = 0$), V_{GS} the gate bias, and q the elementary electrical charge.

This approach is based on the use of the experimental variations of the conductance G with the gate voltage V_{GS}, and the knowledge of the dependence of the surface potential Ψ_S with V_{GS}. To calculate the surface potential, two approaches are usually adopted. The first method, iterative process with $\Psi_S(i) = \Psi_S(i-1) + d\Psi_S$ is used to numerically approximate the relation between Ψ_S and V_{GS}: $\Psi_S = f(V_{GS})$. In the second method [80], the experimental measurements of the drain current with temperature are exploited: the deduced activation energy, E_a, makes it possible to state Ψ_S dependence on V_{GS} following (see Fig. 54):

$$q\Psi_S \cong E_{F0} - E_a(V_{GS}) \qquad (7)$$

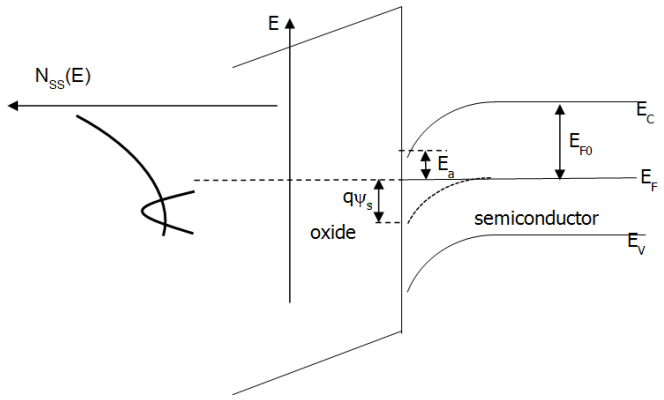

Fig. 54. Energy band diagram of TFT [82].

Where E_{F0} is the activation energy for $V_{GS}=V_{FB}$ (corresponding to the minimum of the drain current of the transfer characteristics).

This Suzuki model is basically used for the DOS calculation in the active layer, and thus refers to the active layer morphology. Otherwise, the theory of Suzuki also predicts calculation of the energy distribution of surface states density using C-V characteristics of MOS capacitors. In this model, the induced surface charge density, Q_{SS}, at localized interface traps is given by [79]:

$$Q_{SS}(\Psi_S) = d\Psi_S \frac{G_0}{dG}\frac{\varepsilon_{Si}}{d_{Si}}\left[exp\frac{q\Psi_S}{kT} - 1\right] - \frac{\varepsilon_{ox}}{d_{ox}}(V_{GS} - V_{FB} - \Psi_S) \quad (8)$$

Where d_{Si} the active layer thickness, k the Boltzman constant, T the Kelvin temperature.

The induced charge trapped at the interface is given by:

$$Q_{SS}(\Psi_S) = -q\int_{E_{F0}}^{E_{F0}+q\Psi_S} N_{SS}(E)dE \quad (9)$$

Where N_{SS} stands for the energy distribution of surface state density. Therefore, the surface state density is deduced from [79]:

$$N_{SS}(E_{F0} + q\Psi_S) = -\frac{1}{q}\frac{\partial Q_{SS}(\Psi_S)}{\partial(q\Psi_S)} \quad (10)$$

A calculation of Q_{SS} given by (8) is firstly needed for the determination of N_{SS}. In this case the increment of Ψ_S is obtained from iterative process. Moreover, variation of the conductance is obtained by $dG=dV_{GS}(g_m/V_{DS})$ for TFTs operating in the linear mode.

According to (8), the negative values, due to electrons trapping at defects, were admitted for calculations of Q_{SS}.

DOS and N_{SS} calculation for ICP-CVD TFT

We will first present the DOS distribution comparison of ICP-CVD TFT before and after performing thermal annealing. After this, N_{SS} distribution comparison is accordingly calculated and presented. Surface potential in both defect density distributions is deduced from the iterative process we mentioned in the section above.

In Fig. 55, we first present the DOS before and after thermal annealing on the ICP-CVD TFT by applying Suzuki model. The first discrete value of the surface potential is approximated by Taylor Theorem and following values are obtained by iterative calculation.

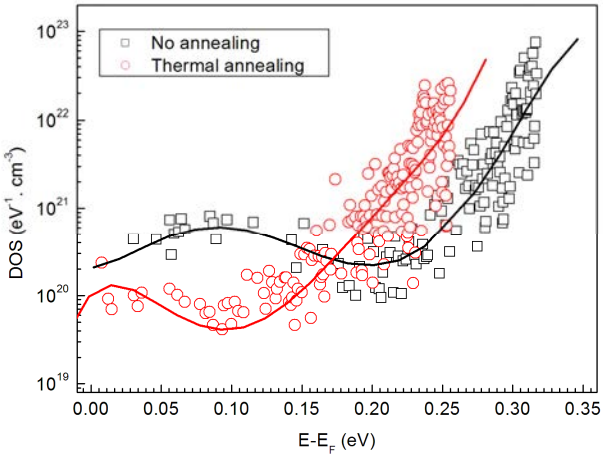

Fig. 55. Comparison of DOS for the same ICP-CVD TFT before and after performing FG annealing (Full lines: fitted curves).

From Fig. 55, we can observe the DOS related to deep states into the bandgap shows one decade higher than before performing annealing. This is explained by a lowering of defect density into the active layer and at the gate insulator interface after thermal annealing.

For the determination of N_{SS} on the same ICP-CVD TFT, we adopted also the iterative process to calculate surface potential and applying surface potential to finally calculate the N_{SS} before and after thermal annealing. The distribution is shown in Fig. 56.

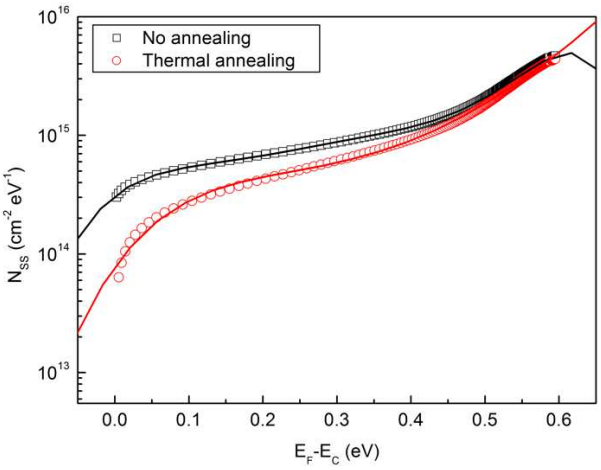

Fig. 56. Surface states density comparison of TFT before and after performing thermal annealing calculated by using iterative method.

From Fig.56 we can observe that after thermal annealing, N_{SS} is lower and almost one decade decrease for deep states, which indicates the healing of the defects locating at the interface of SiO_2/Si by the thermal annealing process. This decrease results in better electrical properties of TFT after thermal annealing.

2.4 Conclusion

ICP-CVD was introduced to deposit SiO_2 and Si layers in this chapter. Following the novel technique of deposition, the optimization of SiO_2 deposition and electrical properties of SiO_2 are presented. Besides, the properties of ICP-CVD silicon layer have been presented by fabricating the ICP-CVD TFTs.

First, as a promising approach of depositing thin films at low temperature, ICP-CVD was researched in detail on SiO_2 deposition and SiO_2 MOS capacitors characterization. Two batches of capacitors were fabricated under various parameters, and optimized parameters were obtained after characterizing these capacitors in terms of HFCV and breakdown field. LF power of 500W, RF power of 50W, pressure of 2.5mTorr and temperature of 20 ˚C have been validated

as the best combination of the deposition parameters. In conclusion, SiO_2 layers deposited by ICP-CVD can yield good electrical properties and act as the insulating layers in TFTs.

Second, the ICP-CVD TFTs with gate oxide and microcrystalline silicon active layers deposited without deliberately heating the substrate is demonstrated. After thermal annealing at temperature no higher than 220˚C, TFTs yield promising electrical properties. Thanks to the low temperature process of ICP-CVD, it offers the opportunity to explore the applications on flexible substrates.

At last the temperature measurements were also carried out to determine the distribution of surface potential which helped validate the N_{SS} calculation through Suzuki's model experimentally. In addition, the N_{SS} of ICP-CVD TFT was also calculated.

Later in next chapter, the ICP-CVD would be used to explore the possibility of silicon nanowires fabrication. The corresponding details and results will be discussed in chapter 3.

Chapter 3

Spacer approach of SiNWs fabricated at low temperature

3.1 Introduction

As an interesting research topic in semiconductor research community, SiNWs has seen a remarkable progress not only in various synthesis methods, but also in large scale integration and better electrical properties in the past two decades [83]. SiNWs may not have a strict definition but generally mentioned "silicon nanowires" in publications could refer to the silicon wires with diameter rather down to one hundred nanometers. Therefore, SiNWs present high aspect ratio, feasibility of large-scale integration and low cost compared to the other conventional silicon materials for integration at nanometric scale. In addition, process fabrication compatibility with mass production CMOS silicon technology makes SiNWs as good candidate for nanoelectronics devices.

The synthesis methods of SiNWs generally could be divided into two categories: bottom-up and top-down.

When we talk about bottom-up approach, VLS (Vapor-Liquid-Solid) method almost dominates this category since it is the most researched nanowires synthesis approach started from work of R. S. Wagner and W. C. Ellis back to 1960s [84]. VLS implements the growth of nanowires by introducing the precursor gas into the reactor to form liquid droplets of certain metal catalyst in which silicon coming from precursor is incorporated and to initiate the growth of nanowires at the interface between liquid droplets and substrate due to the silicon supersaturation in droplets. Gold (Au) is the most frequently used catalyst [85], [86] because Au is nontoxic, reachable and has high solubility in silicon. Other metals like silver (Ag) and aluminum (Al) were also reported to fabricate silicon nanowires successfully [87]–[89]. SLS as we mentioned in chapter 1 can also be considered as bottom-up approach since nanowires precipitate with the help of catalyst but when precursor gas is absent.

Fig. 57 illustrates the principle of VLS method of nanowires growth. A small Au particle is placed on the surface of Si wafer and heated to a certain temperature to form a droplet of Au-Si alloy as shown in Fig. 57(a). Then a mixture of hydrogen and $SiCl_4$ is introduced. The liquid alloy acts as a catalyst for the nanowire formation. The Si enters the liquid and freezes out, with a very small concentration of Au in solid solution, at the interface between solid Si and the liquid alloy. By a continuation of this process the nanowire keeps growing and the alloy droplet still places on top of the nanowire as shown in Fig. 57(b).

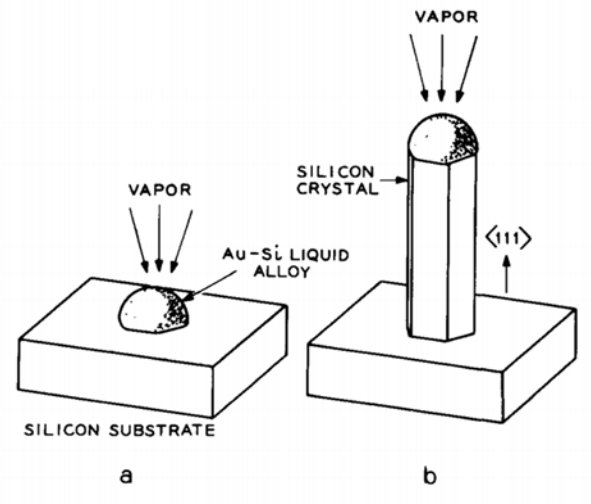

Fig. 57. Schematic illustration of silicon nanowires growth by VLS [84].

Top-down on the other hand is the reverse synthesis direction to bottom-up. Top-down approach often refers to a sequence of processes like film deposition, photolithography/nanolithography and reactive ion etching. A direct way to fabricate nanowires is to use electron beam lithography (EBL) to pattern the nanowires and to perform Reactive Ion Etching (RIE) to realize nanowires with sub-micrometer scale. Z. Li et al. [90] and H. D. Tong et al. [91] both presented SiNWs fabrication by using EBL.

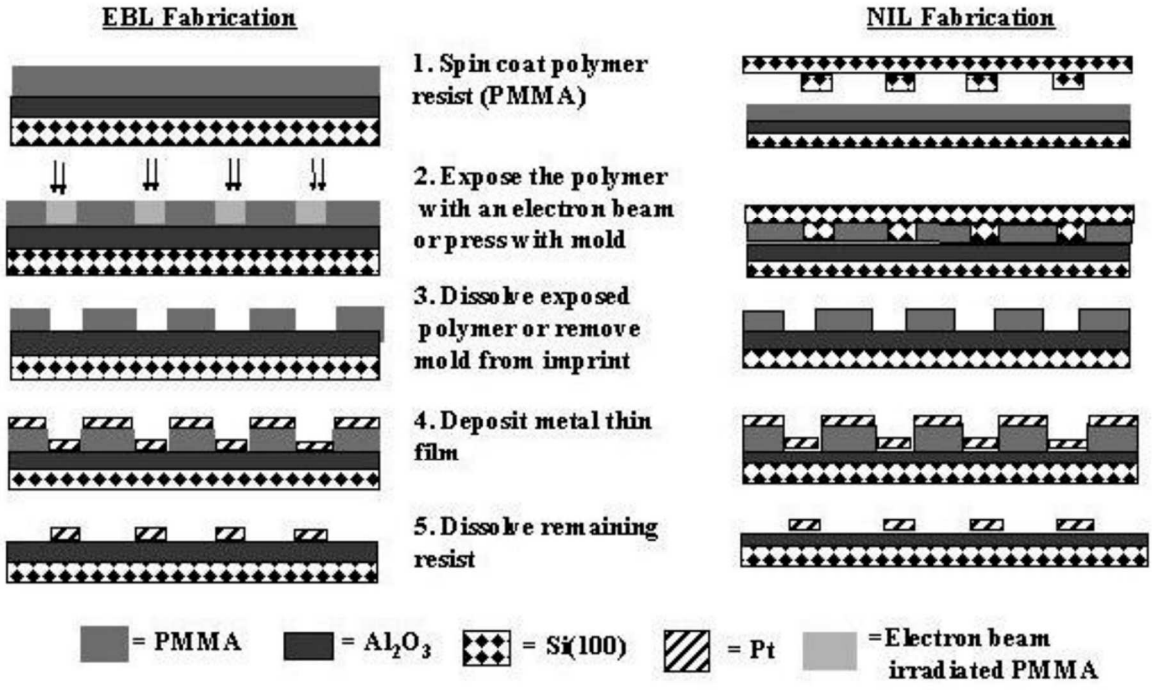

Fig. 58. Fabrication process of EBL and NIL (Nanoimprint Lithography) [92].

Fig. 58 illustrates EBL fabrication of nanowires. EBL works in same manner as conventional photolithography but in much smaller scale. Nanoimprint lithography (NIL) enables another approach of fabricating nanowires in more or less the same scale as EBL method. In NIL approach, a mold which consists of the nanowire patterns is generally used to compress onto imprint resist (PMMA in Fig. 58). When the nanowire patterns are transferred on the resist, the resist can work as the mask of following etching process to finally form the nanowires with the expected materials.

Besides EBL, conventional photolithography is also qualified for SiNWs synthesis but in less direct manner using SOI (Silicon on Insulator) substrate. S. Chen et al. [93] provided a solution based on combination of photolithography and plane dependent wet etching (PDE). The sidewall of nanowire was defined by (100) crystal orientation of silicon layer. Therefore, the size of nanowires could be well controlled by adjusting the thickness of top silicon layer. M. Lee et al. [94] used the same idea to fabricate SiNWs arrays and M. D. Marchi et al. [95] fabricated stacked nanowires.

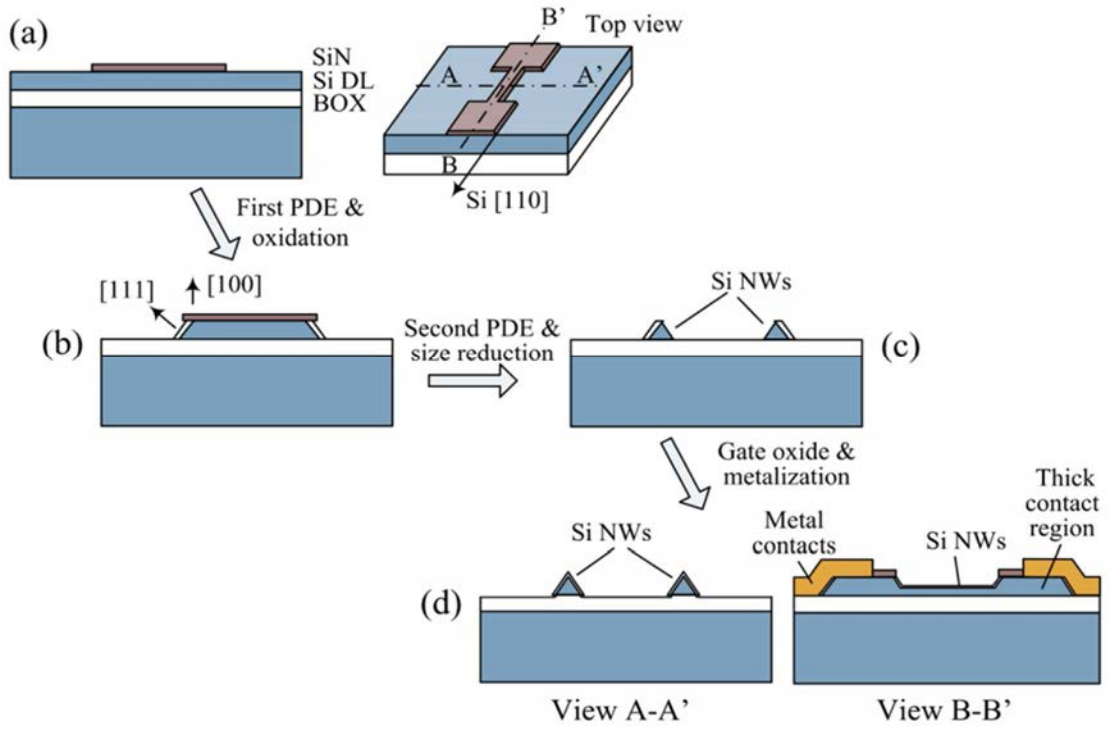

Fig. 59. Top-down SiNW microfabrication procedure from [93] (not to scale).

In Fig. 59, S. Chen et al. presented the fabrication procedure by using conventional photolithography and wet etching. First a silicon nitride (SiN) layer was patterned and etched

as shown in Fig. 59(a). Since the (100) planes of silicon etch 5-10 time faster than the (111) planes in alkaline etchant, resulting in a trapezoid-shaped profile of silicon (Fig. 59(b)). After removing the SiN layer and performed second wet etching, the triangle-shaped nanowires in sectional view were fabricated (Fig. 59(c)).

When we compare two top-down approaches, conventional photolithography is generally a lower cost and more easily accessible approach. The important point is to well combine photolithography with other process to break the size limit of photolithography itself (at least lower than one hundred nanometers) and to finally fabricate qualified nanowires.

In our work, we will focus on top-down approach since we can have well-organized SiNWs at lower cost. More specifically, spacer method presented in this work would be the solution for fabricating nanowires at low temperature.

3.2 Basics of low temperature spacer method

Unlike the other top-down approaches with EBL involved, spacer method classically used in sub-micron technology could be implemented only by using conventional photolithography and RIE. Spacer method was adopted as the nanowires synthesis approach first found in the work of H. C. Lin. et al [96]. The spacers were realized by RIE etching on LPCVD poly-Si layer.

Our laboratory started research of spacer method from F. Demami [97], [98], followed by B. Le Borgne [99]. The nanowires were successfully fabricated by using LPCVD poly-Si as well.

3.2.1 Principle of spacer method

Spacer method offers the opportunity to form the spacers after performing RIE etching on the silicon layer, these spacers locate at the sidewalls of the material steps and could be considered as SiNWs. The formation of SiNWs is illustrated in Fig. 60, as showed in this figure, structural layer (SiO_2) is firstly deposited on the substrate, then is etched to form the material steps. After this, the deposition of materials that are used to make nanowires and subsequent etching are performed. Finally, the spacers are made thanks to the height difference of coated layer at the sidewalls of material steps. More specifically, the formation of SiNWs is based on the anisotropic effect of RIE etching, which etches silicon more laterally than vertically.

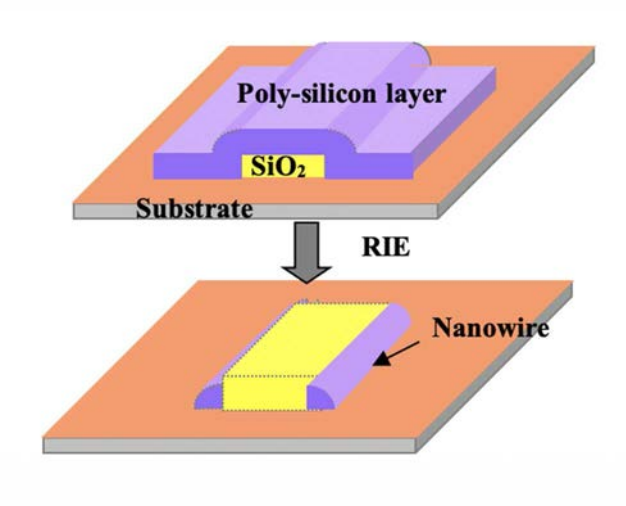

Fig. 60. Schematic of nanowires formation by top-down approach [98].

3.2.2 Low temperature spacer method

Previous works [97]–[100] were conducted in our laboratory and the SiNWs fabricated by spacer method are polycrystalline silicon which originally deposited by using LPCVD. This deposition process always requires temperature as high as 550 ˚C which exceeds the temperature limit for flexible applications. Therefore, we will need to investigate a low temperature spacer method in which whole process flow runs at temperature below 300 ˚C, in relation with different qualities of materials (SiO_2 and silicon layers) used.

When we go through the technological process of spacer method: 1) photolithography to pattern the material steps, 2) first RIE etching to form the steps, 3) deposition of silicon dedicated to nanowires, 4) second etching to form spacers, we realize that only the deposition of steps raises the thermal problem. LPCVD is certainly not appropriate for flexible substrates, so adopting lower temperature deposition technique is the only way to realize low temperature spacer method.

PECVD is a good candidate for its good film quality and relatively lower deposition temperature as we discussed in section 1.2. Therefore, in this work, the investigation of PECVD based spacer method was first investigated for fabricating SiNWs at low temperature (≤300 ˚C). Secondly, the investigation on ICP-CVD was also conducted to fabricate SiNWs by using spacer method.

3.2.3 Fabrication process of low temperature spacer method

The fabrication process of low temperature spacer method requires one mask only. First as illustrated in Fig. 61(a), a 100/200 nm thick SiO_2 layer was deposited on cleaned silicon wafer at 250 ˚C by using PECVD. Then photolithography was performed with mask patterned to define the material steps. First RIE was carried out subsequently to form the steps (Fig. 61(b)). Ideal steps would have quite vertical and smooth sidewalls. After remaining photoresist was removed, a 400nm thick a-Si/μc-Si layer was deposited by using PECVD (Fig. 61(c)). At last, second RIE was performed on the sample (Fig. 61(d)). Spacers are expected to form thanks to the thickness difference at the sidewalls of these SiO_2 steps.

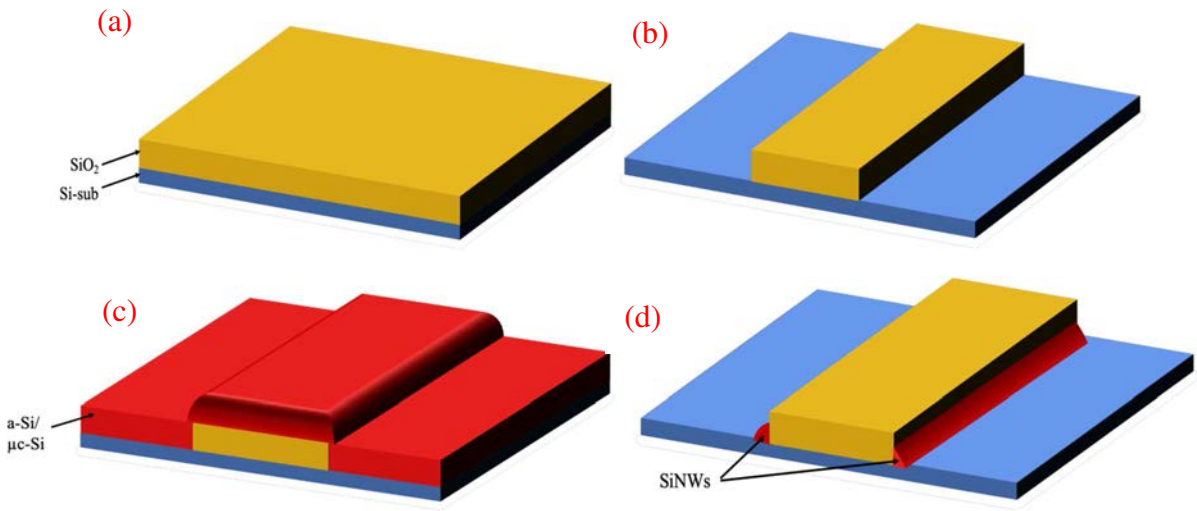

Fig. 61. Technological process flow of spacer method.

3.2.4 Parameters of deposition process

In prior to optimizing the parameters of RIE, the parameters of other processes would be provided. The parameters of photolithography, SiO_2 deposition and silicon deposition are generally standard in terms of making material steps and layer deposition. The parameters of photolithography could be found in annex of this thesis.

The parameters of PECVD SiO_2, a-Si and μc-Si are listed in table 14, 15 and 16, respectively.

SiO_2 deposition

Table 14. Parameters of PECVD SiO_2 deposition.

Gas mixture and mass flow	SiH_4 (4 sccm) + N_2O (17 sccm)
Temperature (˚C)	300
Pressure (mbar)	0.9
RF power (W)	15

a-Si deposition

Table 15. Parameters of PECVD a-Si deposition.

Gas mixture and mass flow	SiH_4 10 sccm
Temperature (˚C)	240
Pressure (mbar)	0.16
RF power (W)	6

µc-Si (microcrystalline silicon) deposition

Table 16. Parameters of PECVD µc-Si deposition.

Gas mixture and mass flow	SiH_4 (1.5 sccm) + Ar (75 sccm) + H_2 (75 sccm)
Temperature (˚C)	185
Pressure (mbar)	0.9
RF power (W)	15

3.3 Optimization of SiO_2 step etching

Since the etching is the most important process among all these processes for making spacers, we firstly optimized the SiO_2 step etching on Microsys 400 RIE system. The requirements for SiO_2 steps are vertical and smooth sidewalls because it will contribute to the formation of spacers. Therefore, the optimization would focus on the verticality and good morphology of sidewalls of SiO_2 steps.

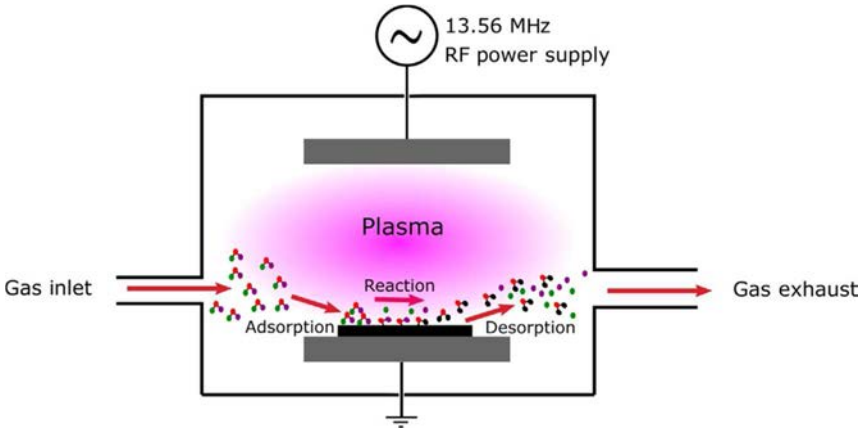

Fig. 62. Schematic of RIE [101].

Fig. 62 shows the working principle of RIE. The injected gas (CF_4 for SiO_2 etching and SF_6 for silicon etching) is ionized by the RF power applied between the anode and the cathode and the ionized gas species would react with the material on the sample and finally etch them. There are several parameters that should be well studied: RF power, gas flow, pressure and chuck temperature. The chuck temperature is always set at 20 ˚C since the plasma etching is mostly working near room temperature (to avoid the adsorption of etching species). The pressure is set at 1 mTorr because low pressure would lead to more directional etching of SiO_2 to promote verticality of the sidewalls [97]. RF power is very important due to its direct control of the intensity of bias, so we focus on the RF power adjustment for the optimization of SiO_2 material step etching.

First, the etching of the SiO_2 steps was carried out following the parameters in table 17. Two samples coated with SiO_2 layer (PECVD SiO_2, parameters see table 14) were etched during 330s. The step height was measured by using profilometer and then averaged. Etch rate is also shown in this table.

Table 17. Parameters of first SiO_2 step etching on Microsys 400.

RF power	Gas flow	Pressure	Etched step height	Etching duration	Etch rate
100W	CF_4, 30sccm	1mTorr	~120 nm	5’30’’	~21.8nm/min

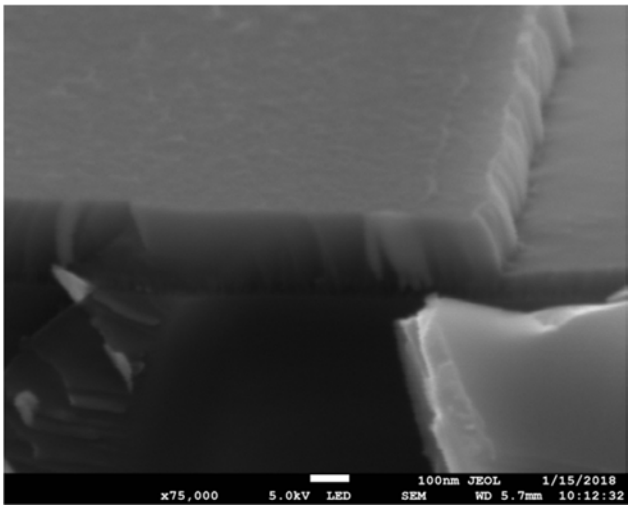

Fig. 63. SEM images of etched SiO_2 step (SiO_2 layer was deposited by PECVD) following the parameters in table 17.

Fig. 63 shows the SEM images of SiO_2 step after etching. Rough side wall of the SiO_2 step is nearly perpendicular to the surface of the samples and a trench can be detected at the bottom of step mainly due to the over etch during RIE.

In order to get better morphology of the sidewalls of SiO_2 steps, lower RF power was adopted since lower RF power is believed to have less bombardment effect. In addition, the plasma was not stable with pressure of 1mTorr during the RIE process, therefore the pressure was increased slightly up to 4mTorr to ensure stable plasma. The new parameters are compared with the previous ones in table 18.

Table 18. Comparison of etching parameters before and after optimization.

	Before	After
RF power	100W	50W
Gas flow	CF_4, 30sccm	CF_4, 30sccm
Pressure	1mTorr	4mTorr
Step height of SiO_2	~140nm	~172nm
Etch rate	~24.7 nm/min	~17.6 nm/min

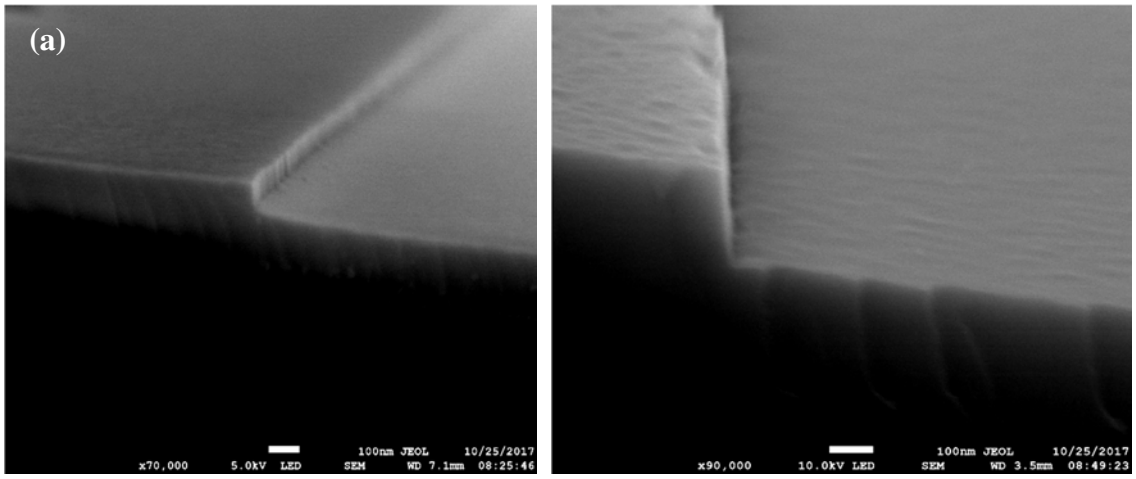

Fig. 64. (a) SEM images of SiO_2 steps which were etched during 5 minutes; (b) SEM images of the same conditioned SiO_2 steps which were etched during 10 minutes.

Following new parameters, two samples were etched after 5 and 10 minutes, respectively. Fig. 64 present the SEM images after performing RIE etching. As the only difference during the etching process is the duration, these two samples show almost the same etching profile if we neglect the difference on step height. Compared with the samples etched by parameters mentioned in table 17, the morphology of the sidewalls of SiO_2 steps has been improved with new parameters. Moreover, the nearly smooth sidewalls are as vertical as those realized before, which indicates good capability of spacers forming.

3.4 Optimization of silicon etching

After we managed to get the vertical SiO_2 steps, the research on optimization of silicon etching started. The formation of silicon nanowires takes place when the deposited silicon layer is anisotropically etched by SF_6 plasma due to the different etch rate between the direction in parallel and in perpendicular to substrate, and more importantly, due to the thickness difference at the sidewall of SiO_2 step (see Fig. 60).

3.4.1 PECVD silicon etching optimization

In order to promote the formation of spacers, the RF power and the pressure are the most important parameters to study during the silicon optimization. Pressure of 10 mTorr was our first approach since it was confirmed in thesis of G. Wenga [102] for the formation of poly-Si nanowires. Although 10 mTorr as the pressure is less anisotropic than 1 mTorr, it is expected

to have more rounded profile of the formed nanowires. RF power of 50 W and gas flow of 30 sccm were tested and then were lowered down to 30 W and 20 sccm, respectively. It was expected to have a lower etching kinetics to easily detect the etching endpoint.

RIE etching was tested both on a-Si (table 15) and µc-Si (table 16) because either a-Si or µc-Si could be deposited at low temperature. More importantly, it is also convenient to know the kinetics of silicon etching with different crystal lattice orders. Furthermore, if µc-Si based spacers could be successfully fabricated, they could be exempt from subsequent annealing.

The etching was carried out first on several pieces of silicon coated samples following the parameters in table 19:

Table 19. The etching parameters and etch rate of samples with different silicon layers.

<table>
<tr><th>No. of samples</th><th>Silicon layer</th><th>Etching parameters</th><th>Etch rate</th></tr>
<tr><td>1 and 2</td><td rowspan="2">a-Si</td><td>RF power: 50W
Gas flow: SF_6, 30sccm
Pressure: 10mTorr</td><td>169 ± 15 nm/min</td></tr>
<tr><td>3 and 4</td><td rowspan="2">RF power: 30W
Gas flow: SF_6, 20sccm
Pressure: 10mTorr</td><td>169 ± 3 nm/min</td></tr>
<tr><td>5 and 6</td><td>µc-Si</td><td>201 ± 17 nm/min</td></tr>
</table>

The etching parameters used on sample 1 and 2 changed to the other set of parameters used on sample 3-6 because it was expected to lower down the etch rate thus to have a better control of the end-point detection. But unfortunately, etch rate did not decrease after decreasing RF power and gas flow, indicating that the change in these parameters has a negligible effect in terms of etch rate. The etch rate of the µc-Si is faster than that of the a-Si. This could be attributed to an organization of crystalline lattice in the layers. Therefore, in the following, a-Si layer will used in our study.

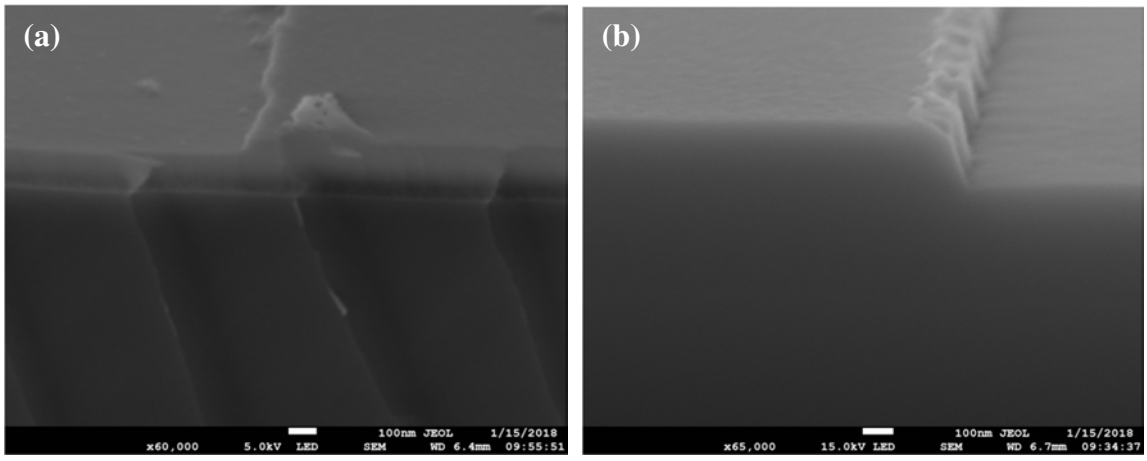

Fig. 65. SEM image of SiO_2 step after silicon etching: (a) a-Si etching; (b) µc-Si etching.

From Fig. 65 we can observe that after etching of silicon layers, no nanowires can be seen either for a-Si or µc-Si. The possible reason of failure could be less vertical etching compared to lateral etching during the silicon etching due to higher pressure adopted compared to SiO_2 etching, especially compared to the parameters adopted to etch poly-Si by G. Wenga in our laboratory several years ago [102].

In prior to studying the pressure during the etching process, it is also important to have an idea about the coverage of silicon layer on SiO_2 step, since non-conformal silicon coverage would lead to failure of formation of spacer as well. Fig. 66 makes it possible to verify the conformal appearance of the deposition of a-Si coating the SiO_2 steps on Si substrate.

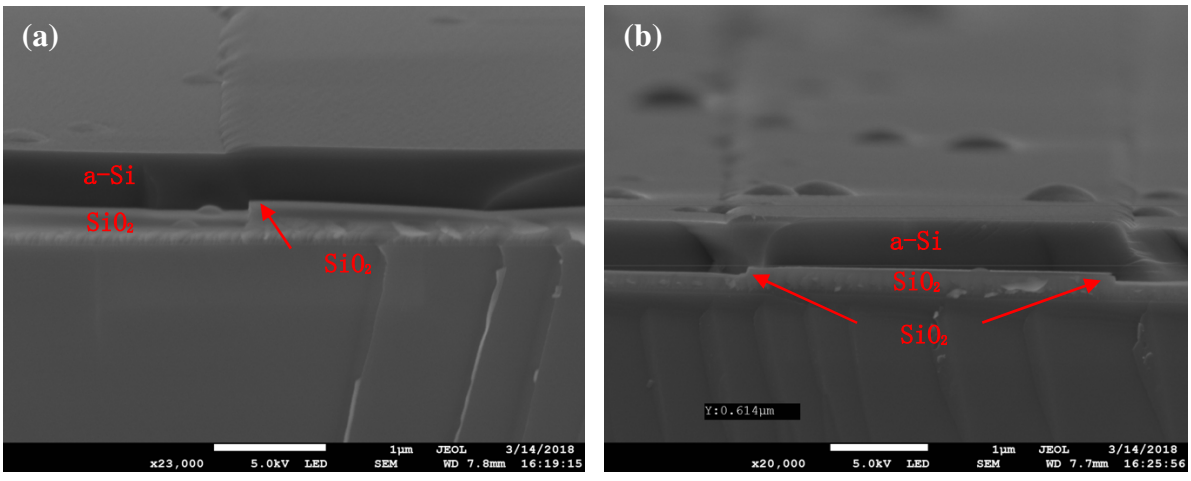

Fig. 66. (a) a-Si layer coverage on left end SiO_2 step; (b) a-Si layer coverage on whole SiO_2 step.

In order to verify the speculation on high pressure during silicon etching, 3 different pressures were used while the other parameters were remained same. The parameters of a-Si etching on different samples are summarized in table 20.

Table 20. Parameters of silicon etching with only pressure altered.

No. of samples	RF power	Gas flow	Pressure
1	30W	SF_6, 20sccm	10mTorr
2			8mTorr
3			5mTorr

Lower pressures such as 8mTorr and 5mTorr were tested on sample 2 and 3 because we suspect the pressure as high as 10mTorr would reduce the anisotropic effect (Fig. 65(a)). In addition, according to a previous study in our laboratory based on elaboration of nanowires made of a-Si layer deposited by LPCVD at 550 ˚C [97], it has been shown that a low pressure during plasma etching promotes the formation of spacers. Sample 1 with pressure of 10mTorr is the reference in this process.

From Fig. 67 (a)-(d) we cannot observe any residues at the sidewalls of SiO_2 steps, whereas from Fig. 67 (e)(f) there are some possible residues can be seen at the edges between the bottom surfaces of sample and the sidewalls of SiO_2 steps. This could partially support our speculation on the pressure. By regarding the rough morphology along the sidewalls of SiO_2 steps which can be detected at all pressures, these residues observed with lower pressure of 5mTorr could come from SiO_2 itself. However, at this stage of study we can conclude that high reliable elaboration of nanowire offering a conformal shape using PECVD technique is not possible. In this way, the use of ICP-CVD technique was investigated.

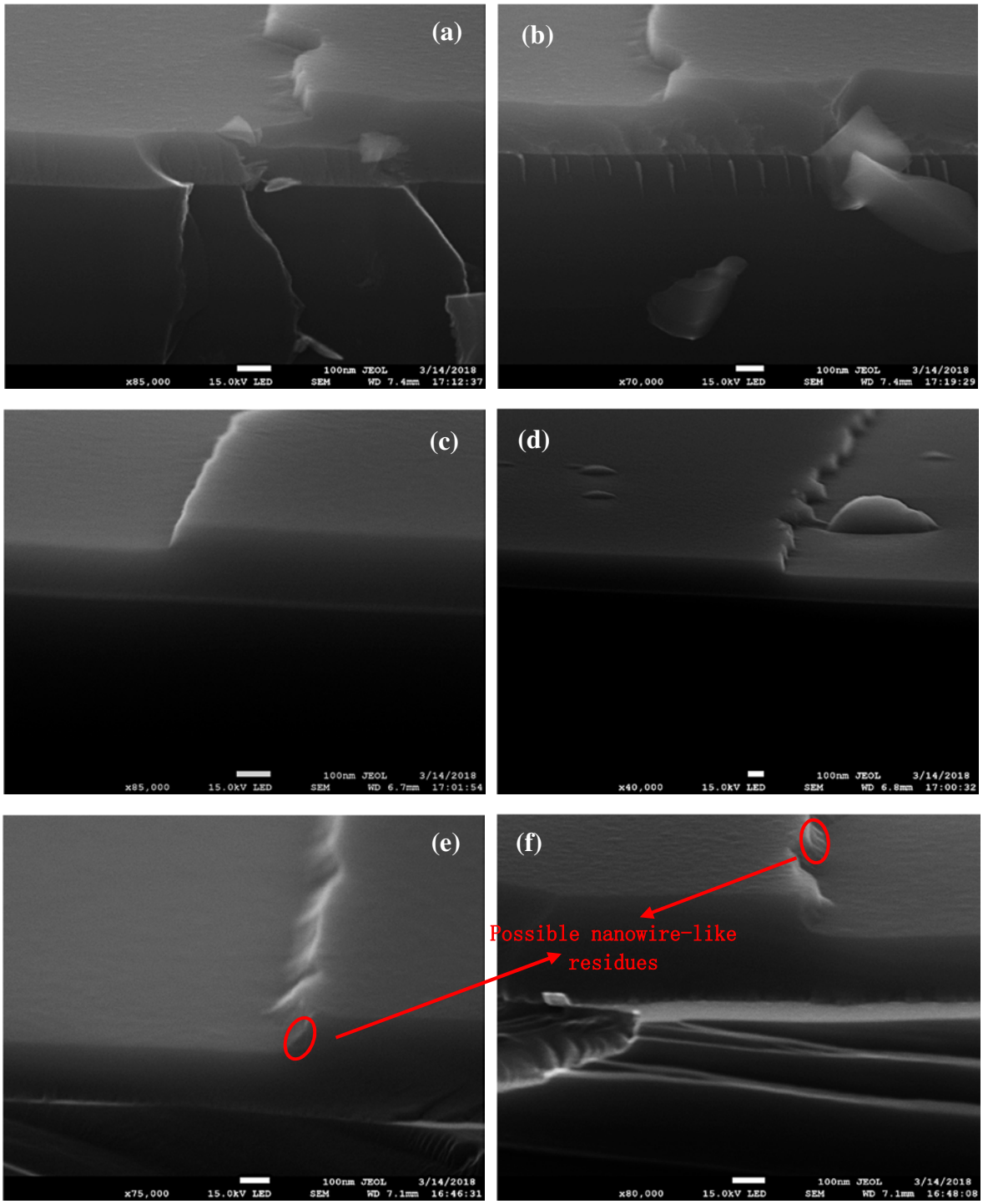

Fig.67. SEM images with different pressures during the silicon etching (RF power of 50W and gas flow of SF_6, 20sccm): (a)(b) 10mTorr; (c)(d) 8mTorr; (e)(f) 5mTorr.

3.4.2 ICP (Inductively Coupled Plasma) -CVD Si etching optimization

The issues could lead to the failure of making spacers after RIE on silicon are the uniformity, density and texture of deposited SiO_2 and even silicon layer. We decided to introduce ICP-CVD technique. Compared with the other low temperature deposition techniques we reviewed in

chapter 1, this technique roughly introduced from 1990s [103] is gaining a massive research interest from last decade.

Since ICP-CVD technology has better uniformity of the deposited layers compared to those deposited by other CVD technologies [51], [52] and has been researched for SiO_2 and Si layers deposition in last chapter, the research on etching of ICP deposited layers (both SiO_2 and Si layers) was carried out following the optimized etching parameters used in the section above.

The details of ICP-CVD technology have been discussed in chapter 2. Therefore, in this section, only the results of RIE etching will be presented.

First, 100nm of SiO_2 layer was deposited by ICP-CVD on silicon substrate and etched by the set of parameters listed in the right column of table 18. Then 400nm silicon layer was deposited on SiO_2 steps and etched. The deposition parameters of ICP-CVD SiO_2 and silicon are listed in table 21 and 22.

Table 21. Parameters of ICP-CVD SiO_2.

Gas mixture	SiH_4/O_2 diluted in Ar
Temperature (˚C)	No substrate annealing
Pressure (mTorr)	2.5
LF power (W)	500

Table 22. Parameters of ICP-CVD Si.

Gas mixture and mass flow	SiH_4/PH_4
Temperature (˚C)	70 (sample reaches 180 during deposition)
Pressure (mTorr)	10
LF power (W)	500

The SiO_2 steps are found very vertical in Fig. 68. It means that the optimized etching parameters on PECVD SiO_2 also work perfectly on ICP-CVD SiO_2. It is not surprised since ICP-CVD's working principle is based on assisted plasma as well.

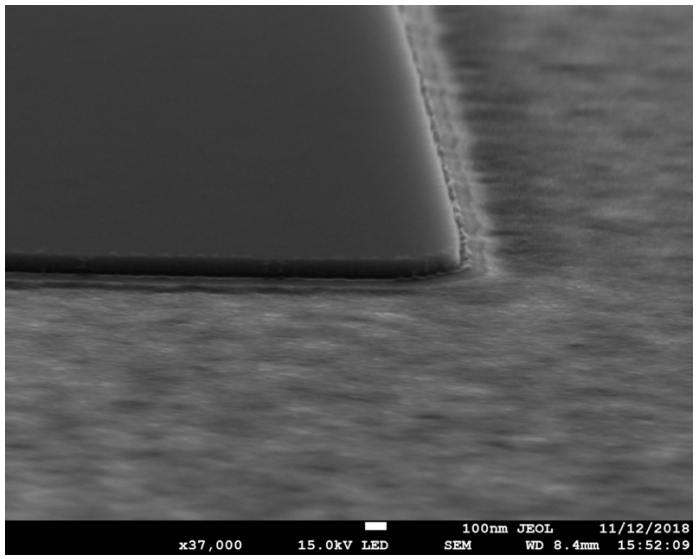

Fig. 68. SEM image of ICP-CVD SiO_2 step.

Since we previously observed nanowire-like residues under the chamber pressure of 5 mTorr using PECVD technology, the same pressure was tried again on ICP-CVD silicon. Beside the pressure, the other parameters were kept the same as listed in table 20.

Fig. 69 shows the SEM images after performing RIE etching on SiO_2 steps. As we can see, residues can be detected. A clear boundary exists between the residue (brighter part) and the SiO_2 step (darker part) in Fig. 69(b). This could be attributed to ICP-CVD which has outstanding uniformity during deposition. The uniform deposition can be considered to benefit the etching process, and accordingly to yield residues after the etching of Si layer. Since the endpoint of etching of Si is controlled by the period change of the reflective oscillation of interferometry laser system, when the endpoint has been reached on one spot on the sample, the Si on whole sample is just equally etched thanks to the uniform deposition. Therefore, residues can be more easily detected.

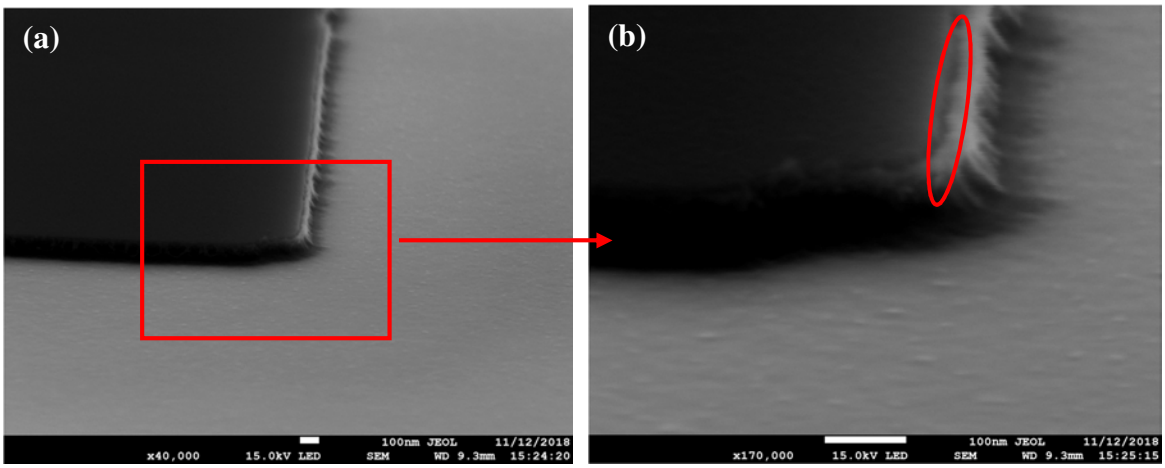

Fig. 69. SEM images after ICP-CVD Si etching under RF 30W, SF_6 20sccm and 5 mTorr.

Nevertheless, further experiment should be performed to know better about the residues after Si etching. In this case, wet etching of the SiO_2 vertical material step was carried out. Ideally, the residues at the side walls of SiO_2 steps would form rings surrounding the areas in which the SiO_2 steps existed and thus after SiO_2 etching nanowires would be revealed. In this way, all samples were immersed in 5% HF solution for 1min to etch 100nm height of the SiO_2 steps. SEM observation was taken after wet etching.

Fig. 70 shows the SEM images after SiO_2 wet etching. Continuous line-structured residues can be observed with plasma etching at 5 mTorr, which implies the existence of the silicon nanowires. The rough surface inside the silicon nanowire ring could be attributed to the incomplete wet etching of SiO_2 step, thus some SiO_2 still remains on the sample after etching.

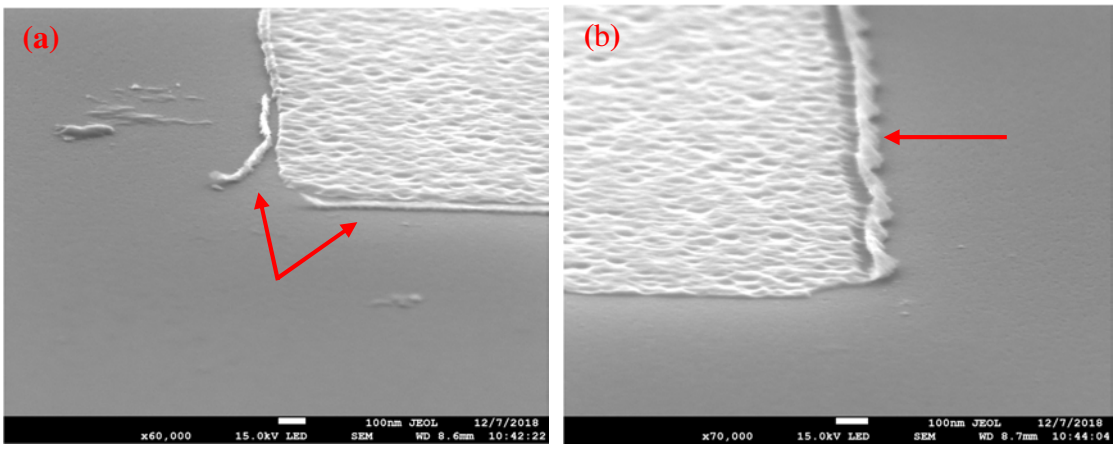

Fig. 70. SEM images after SiO_2 wet etching.

The nanowires were also confirmed by the AFM (Atomic Force Microscope) measurements. The AFM images are shown in Fig. 71.

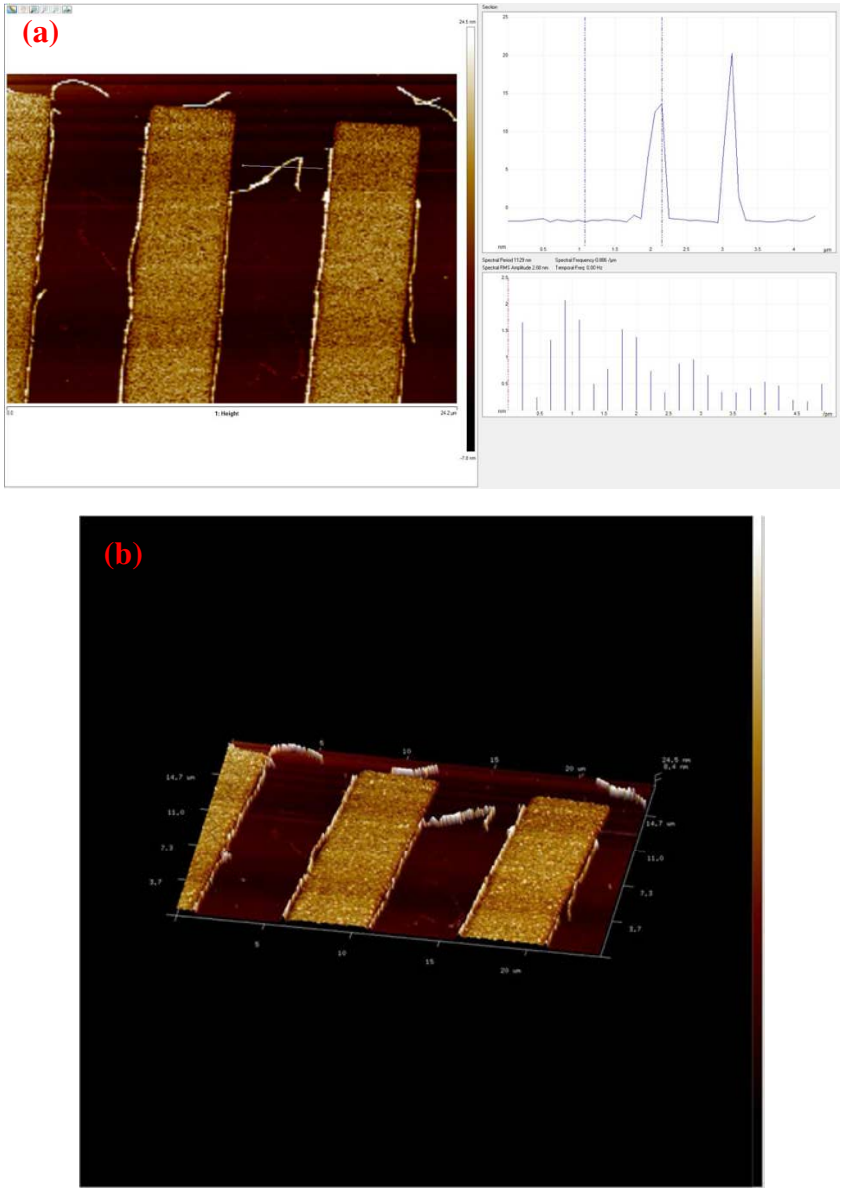

Fig. 71. AFM images of sample with residues after SiO_2 wet etching (5mTorr as chamber pressure during RIE etching of silicon): (a) Top-view, (b) 3D view.

From Fig. 71 we can see the clear existence of the silicon nanowires. It means 30W of RF power, 20sccm of SF_6 gas and 5mTorr of pressure are the best combination of etching parameters to get nanowires as the SiO_2 and Si are deposited by using ICP-CVD.

After making the first successful nanowires, same process was performed again to validate the reproducibility. Unfortunately, the "optimized process" could not be reproduced on the

whole surface of the 2-inch substrate. This time, no residues were observed in SEM images. Therefore, as what we tried on PECVD a-Si, we observed the step coverage of ICP-CVD μc-Si under SEM.

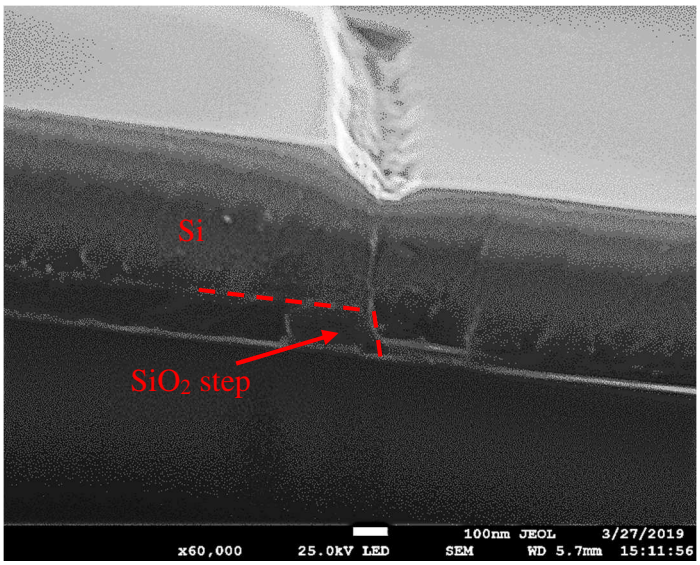

Fig. 72. ICP-CVD silicon layer coverage on ICP-CVD SiO_2 step.

SEM was performed after 400nm thick μc-Si deposition on 100nm SiO_2 step. Both SiO_2 and μc-Si layers were deposited by using ICP-CVD. From Fig. 72, we can see even μc-Si layer fully covers the SiO_2 step, the profile does not present a conformal step coverage. Two flaws could be seen clearly: 1) the sidewall of the silicon layer deforms inwards instead of outwards, 2) a trench occurs at the seam of upper surface and lower surface of silicon. These flaws could lead to a severe problem when RIE is performed to make the spacers.

RIE on μc-Si layer of this sample was carried out following the optimized parameters. The SEM images are shown in Fig. 73.

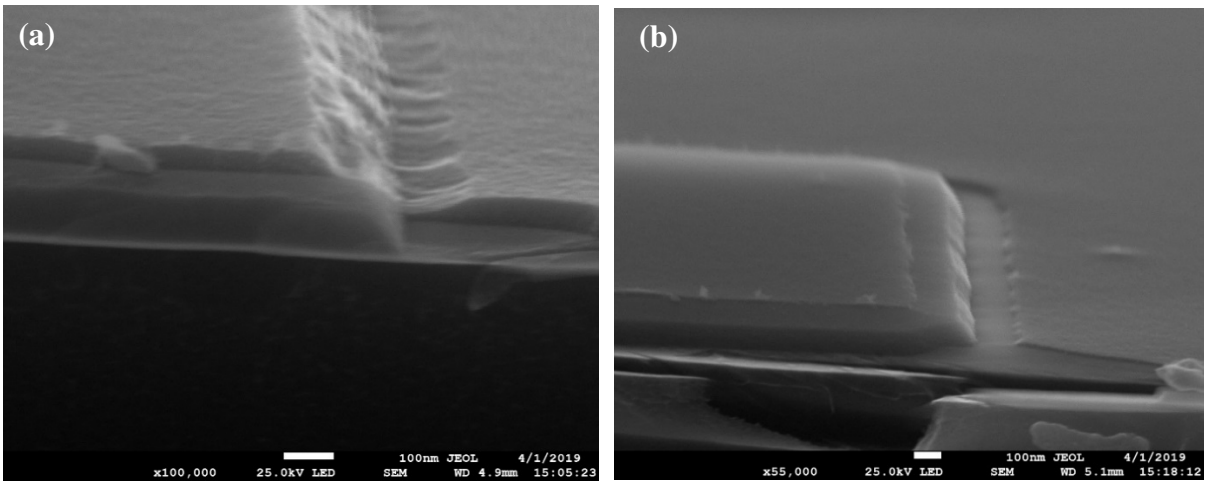

Fig. 73. SEM images after Si etching performed on the same sample in Fig. 72.

Fig. 73 just better revealed the problem caused by non-conformal ICP-CVD deposition. The silicon remaining on upper and lower surfaces is not continuous, which confirms the imperfect profile of the sidewall of silicon layer (Fig. 72). As the sidewall of silicon deformed inward, as we have indicated, the silicon would lose more than its conformal shape laterally during etching.

Therefore, we can speculate that nanowires could be successfully made as long as we can ensure the silicon conformal step coverage using ICP-CVD. Unfortunately, it is hard to realize because ICP-CVD deposition process has already been optimized. Further efforts can still be made to improve silicon layer conformality if the time cost is not taken into account.

3.5 Conclusion

In order to fabricate silicon nanowires at low temperature, the spacer method has been introduced in our research. Unlike the spacer method successfully developed on poly-Si deposited at 550 ˚C, the low temperature deposition methods as PECVD and ICP-CVD techniques working at temperature lower than 300 ˚C have been investigated.

First, SiO_2 steps have been optimized on Microsys 400 RIE system, and the relatively vertical sidewalls of SiO_2 steps can be achieved under RF power of 50W, CF_4 gas flow of 30sccm and pressure of 4mTorr. This set of etching parameters are perfectly suitable for SiO_2 deposited by using ICP-CVD.

Second, etching of silicon that is deposited by PECVD leads to the formation of silicon nanowires has not been perfectly optimized even some efforts were made. Some residues can

be obtained when RF power, SF_6 gas flow and pressure are set at 30W, 20sccm and 5mTorr, respectively. Fortunately, silicon nanowires are finally obtained when the deposition method of SiO_2 and silicon changed from PECVD to ICP-CVD. Thanks to better uniformity ICP-CVD provides, silicon nanowires can be detected after RIE of μc-Si layer. RF power of 30W, SF_6 gas flow of 20sccm and pressure of 5mTorr are the optimized parameters for μc-Si etching.

Same process has been performed after the first successful result about nanowires, it was found that the process could not be reproduced. By evaluating the step coverage of ICP-CVD Si layer under SEM, we can tell that poor step coverage of Si layer leads to failure of fabricating nanowires. It is reasonable to speculate that the nanowires could be stably reproduced when ICP-CVD Si coverage will be improved.

Chapter 4

Indium catalyzed SLS SiNWs at low temperature

4.1 Introduction

Although the ICP-CVD TFTs have been successfully fabricated, the devices still suffer from poor electrical properties due to the crystallinity of the silicon layer. The most likely approach to improve the performance of silicon layers is crystallization which requires a higher temperature treatment. As in the frame of our low temperature process research, the crystallization should be carried out at the temperature lower than 300 ˚C. In addition, and as mentioned previously PECVD and ICP-CVD technologies cannot provide reproducible fabrication of SiNWs using sidewall spacer method. Under this circumstance, we decided to investigate the metal catalyzed silicon nanowire growth by using indium thanks to its lower eutectic temperature (~157 ˚C).

Most of the time, the indium catalyzed silicon nanowire growth follows VLS growth method. In this method, the indium is firstly deposited and is treated by hydrogen plasma. After this, in same reactor, the silane would be introduced as the gas precursor to trigger the growth of nanowires.

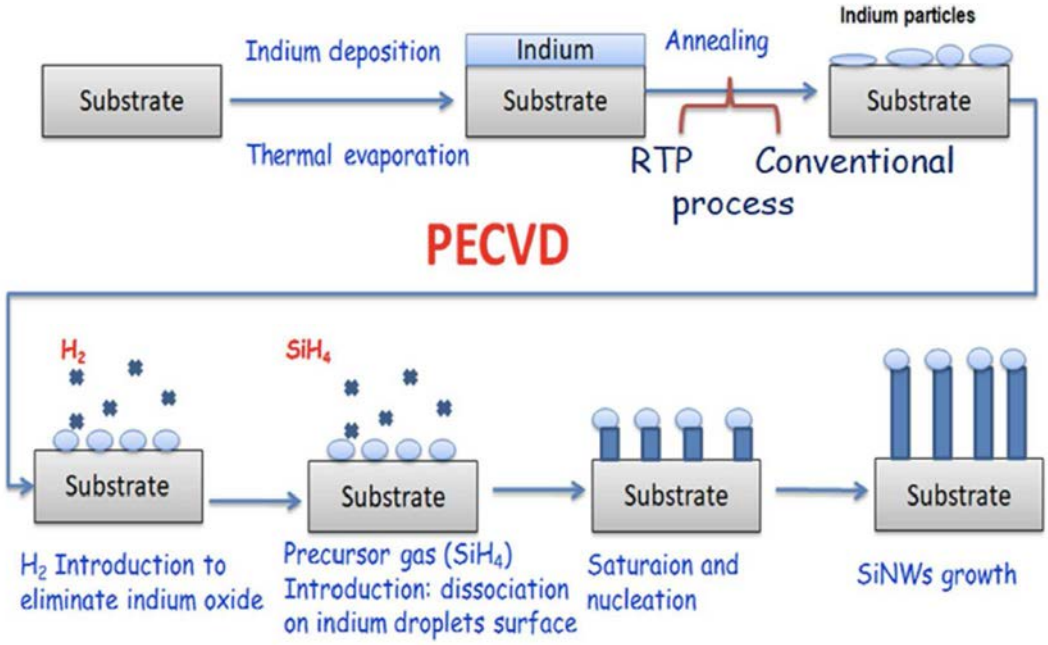

Fig. 74. Schematic illustration of indium catalyzed SiNW growth by using VLS method[104].

Fig. 74 illustrates the synthesis process of indium catalyzed SiNW from the work of R. Benabderrahmane Zaghouani's group [104]. The other groups also used the VLS method to synthesize indium catalyzed SiNWs, but unfortunately the synthesis temperature locates

between 400 and 600 ˚C [105]–[107], which is not compatible with the low temperature flexible substrates.

As we reviewed in chapter 1, R. Heimburger's group introduced the indium induced crystallization of a-Si to poly-Si [38]. This approach is more like Solid-Liquid-Solid (SLS) process. In Plane-SLS (IPSLS) SiNWs have been successfully synthesized by L. Yu's group at low temperature [40]–[42]. Here in our research we will adopt three dimensional (3D) SLS approach to investigate the possibility of SiNWs synthesis.

First, the thermal evaporation of indium will be presented in terms of morphology of evaporated indium layers. Different conditions were set up to mainly study how different thicknesses of indium layers would look like under SEM and AFM (Atomic Force Microscope) characterizations.

Second, the research on indium catalyzed silicon nanowire growth will be carried out. The essence of nanowire growth is hydrogen plasma treatment. Temperature was chosen at 250 ˚C because this temperature was adopted in previous work in our laboratory on VLS SiNWs also catalyzed by indium [108]. The effect of H_2 plasma treatment and thermal annealing was revealed in our study and different durations of H_2 plasma treatment were tried on different thickness of indium layers.

4.2 Indium thermal evaporation

Indium is thermally evaporated on the N-type silicon wafer or a-Si coated silicon wafer in our study. The evaporation is low temperature compatible. Morphological observation through SEM and AFM will be the priority in this section and the comparison of different thicknesses of indium layers will also be presented.

4.2.1 Layer stack and fabrication process

The layer stack adopted in the experiments of indium deposition is illustrated in Fig. 75:

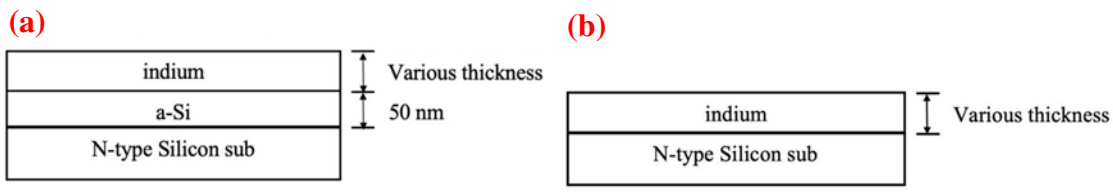

Fig. 75. Schematic of layer stack of samples dedicated to indium induced crystallization.

Deposition of a-Si is an option in the experiments of indium deposition. Therefore, the sample without a-Si layer (see Fig. 75(b)) is more like the reference to the samples coated with a-Si. The samples with a-Si have the thickness of 50nm and various thicknesses of indium (see table 23) deposited by PECVD following the parameters listed in table 15. At last, indium layers with various thicknesses were thermally evaporated.

For the fabrication process, first, the N-type silicon wafers were prepared and went through RCA cleaning.

The conditions for different types of samples are listed below:

Table 23. Conditions of layer stack for research on indium deposition.

Name of sample	Layer stack	Thickness of indium
Test	mono-Si/In	20 nm
No. 2	mono-Si/a-Si/In	10 nm
No. 3	mono-Si/a-Si/In	20 nm
No. 4	mono-Si/a-Si/In	50 nm

4.2.2 SEM and AFM characterization of evaporated indium

SEM and AFM were used to characterize the indium deposition. The morphology of the indium and the indium layer roughness would be revealed.

SEM characterizations are presented with the scale bars representing 100 nm in each image. AFM images show information of height and peak force error and the scan area for sample test, no.2, 3 and 4 are 1μm×1μm, 0.5μm×0.5μm, 1μm×1μm and 2μm×2μm, respectively. AFM images were obtained by implementing AM-AFM (amplitude-AFM) mode which refers to a collection of oscillation coming from the cantilever when it scans over the surface of samples. Peak force error is the feedback signal we can get during the scan, which reveals more clearly the boundaries of each grain of indium. Along with the height image, we can have a vivid impression on the morphology and size of the grains and also on the roughness of deposited indium. These results are shown from Fig. 76 to Fig. 83.

Sample Test

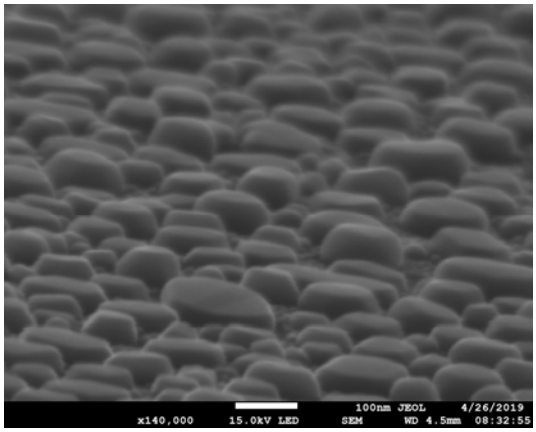

Fig. 76. SEM image of deposited indium of sample Test (mono-Si/20nm In).

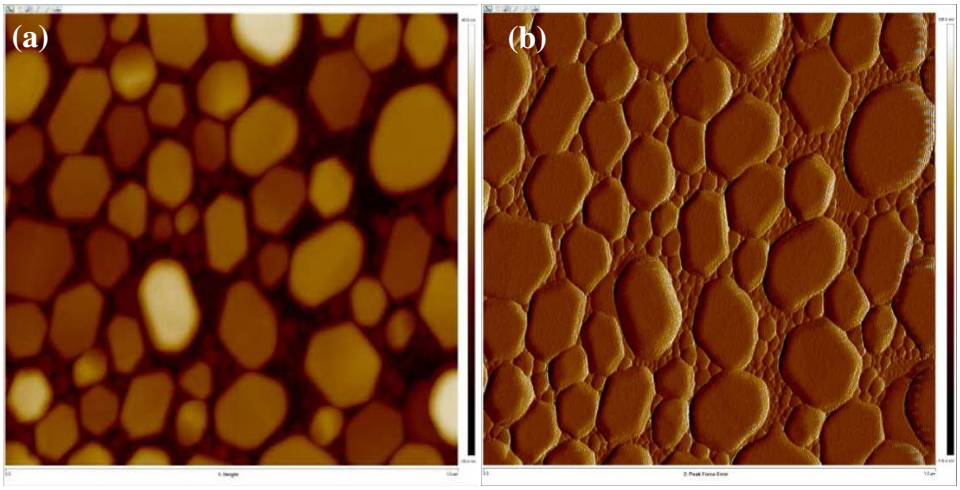

Fig. 77. AFM images of deposited indium of sample Test (mono-Si/20nm In): (a) height; (b) peak force error (scan area 1μm×1μm).

Sample No. 2

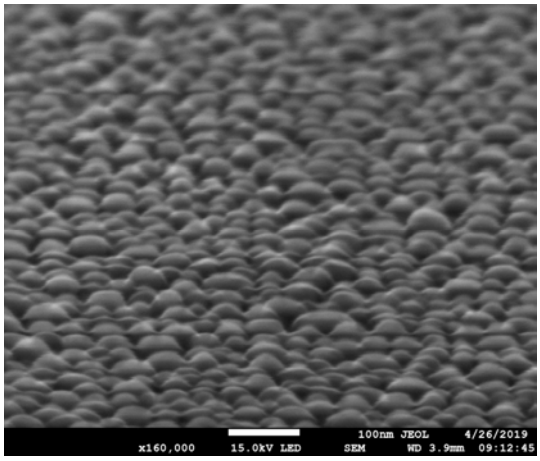

Fig. 78. SEM image of deposited indium of sample No. 2 (mono-Si/50nm a-Si/10nm In).

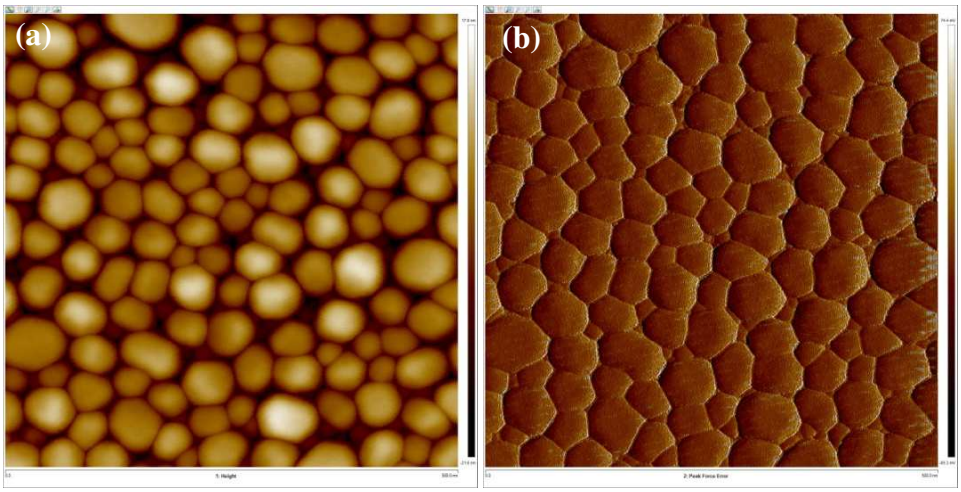

Fig. 79. AFM images of deposited indium of sample No.2 (mono-Si/50nm a-Si/10nm In): (a) height; (b) peak force error (scan area 0.5μm×0.5μm).

Sample No.3

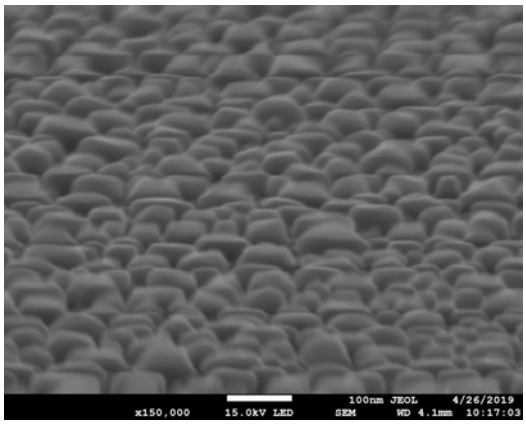

Fig. 80. SEM image of deposited indium of sample No. 3 (mono-Si/50nm a-Si/20nm In).

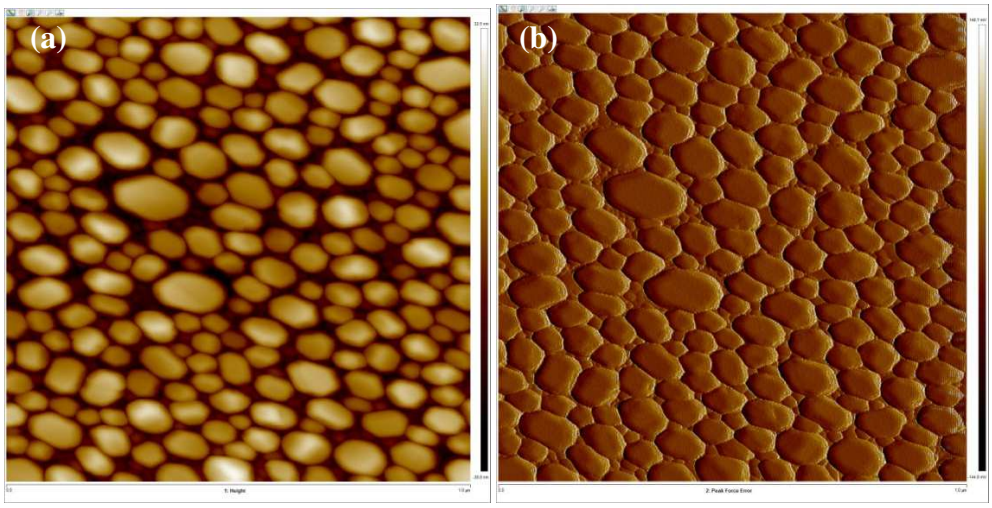

Fig. 81. AFM images of deposited indium of sample No.3 (mono-Si/50nm a-Si/20nm In): (a) height; (b) peak force error (scan area 1μm×1μm).

Sample No. 4

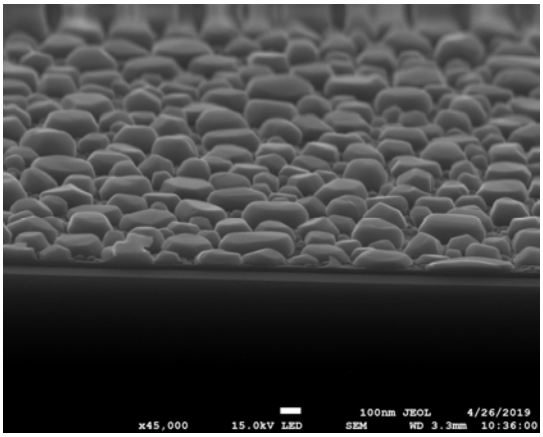

Fig. 82. SEM image of deposited indium of sample No. 4 (mono-Si/50nm a-Si/50nm In).

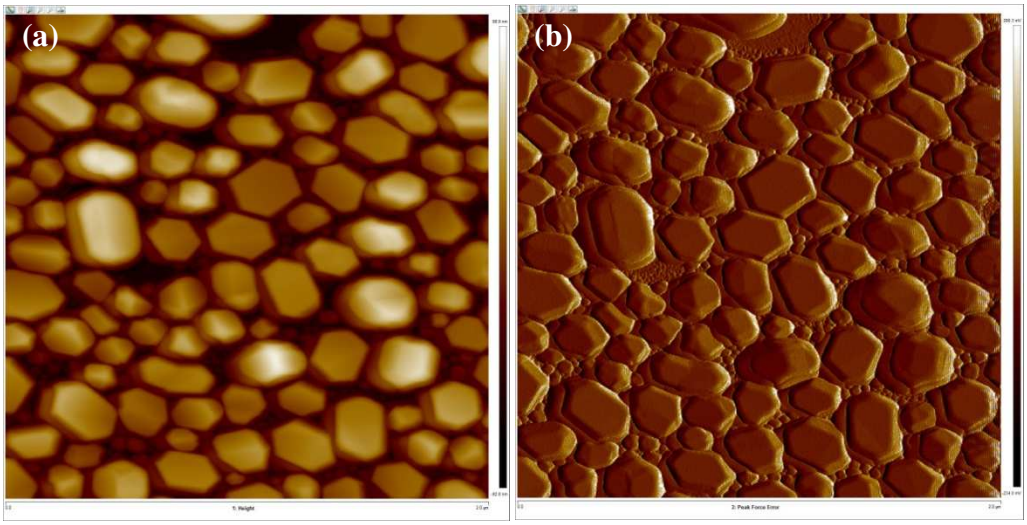

Fig. 83. AFM images of deposited indium of sample No.4 (mono-Si/50nm a-Si/50nm In): (a) height; (b) peak force error (scan area 2μm×2μm).

The deposited indium layers under AFM show polygonal shaped grains, which are consistent with the results presented in corresponding SEM images. From these SEM images, we can see the upper surface of indium grains is quasi flat. In addition, a clear trend shows that the indium grain sizes are proportional to the thickness of deposited indium, which are roughly 50nm, 100nm and 200nm (statistically averaged most of the indium grains in each AFM image) for 10nm thick, 20nm thick and 50nm thick indium layer, respectively.

The roughness of deposited indium layers is characterized by using parameter Ra (arithmetic average) which is calculated following:

$$\mathrm{Ra} = \frac{1}{N}\sum_{i=1}^{N}|Z_i| \qquad (11)$$

Where N is the number of data points and Z_i is the distance from the mean surface level. The calculated Ra for each thickness of indium layer is listed in table 24:

Table 24. Average roughness for each thickness of deposited indium.

Thickness of In	10 nm	20 nm (sample Test)	20 nm (sample No. 3)	50 nm
Ra (nm)	4.75	10.2	10.1	24

From table 24, as expected, we can easily see that the roughness of indium layers is proportional to its thickness. Plus, one should notice is that, even the indium grains on sample Test (mono-Si/20nm In) are more dispersed with larger size than those on sample No. 3 (mono-Si/50nm a-Si/20nm In), they have almost the same roughness.

4.2.3 Relation between the real indium thickness and the thickness shown on indicator

During the thermal evaporation of indium, there is always a mismatch between the real thickness and the thickness shown on indicator of the machine. Because of this, several indium evaporations were performed and the real thickness was measured by profilometer. After plotting the data points on the graph shown in Fig. 84, a fitting was made. From the red line in this figure, we can see it has a linear relationship between the real thickness and the thickness shown on indicator.

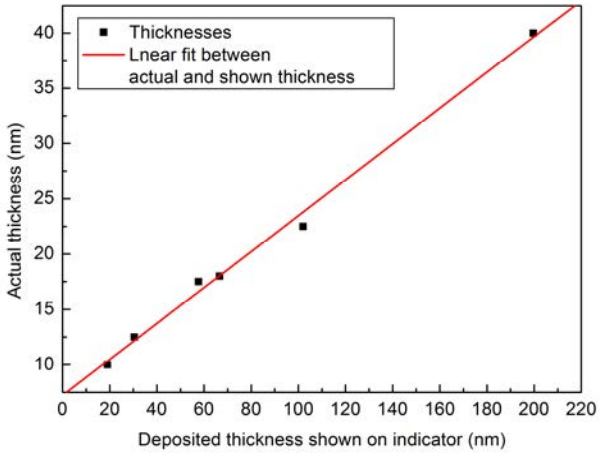

Fig. 84. Relation between real indium thickness and thickness shown on indicator.

The relationship can be described in following equation:

$$\mathrm{Th_{real}(nm)} = 0.16\mathrm{Th_{indi}} + 7.22 \qquad (12)$$

Where $\mathrm{Th_{real}}$ is the real thickness while $\mathrm{Th_{indi}}$ is the thickness shown on indicator. Thus, the real thickness of deposited indium could be easily controlled.

4.3 Indium catalyzed SLS silicon nanowires

Based on the layer stack illustrated in Fig. 75 (a), a 50 nm a-Si layer was deposited by PECVD and an indium layer was thermal evaporated onto a-Si. After these processes, hydrogen plasma is performed on the samples by which the indium layer is believed to be deoxidized and to form indium droplets and accordingly to promote silicon nanowire growth. Along with the samples heated up to and then above the eutectic temperature of indium, the crystallization of silicon will be triggered.

Since there is no gas acted as precursor of silicon nanowire growth, the nanowire growth by the help of indium is considered as solid-liquid-solid (SLS) mode. In this mode, indium forms dissolved droplets by the help of H_2 plasma treatment and absorb a-Si beneath and finally the silicon nanowires growth from the catalyst droplets.

The mechanism of SLS silicon nanowire growth is well studied in Linwei Yu and Pere Roca i Cabarrocas' work [42].

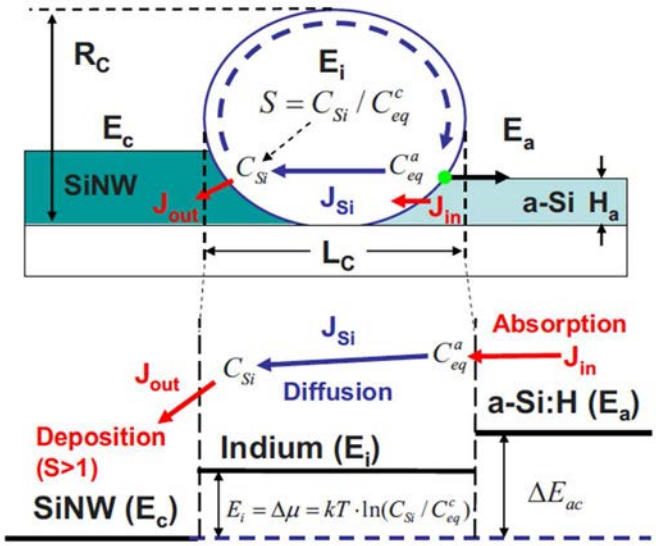

Fig. 85. Schematic illustration for the absorption, diffusion, and deposition steps involved in the growth of lateral SiNW via IPSLS (In-Plane SLS) mechanism. E_a, E_c, and E_i denote the Gibbs energy of Si atoms in the amorphous, crystalline, and dissolved (in In catalyst drop) states, respectively; C_{Si} is the dissolved Si atom concentration in the catalyst drop; J_{in}, J_{out}, and J_{Si} are the absorption, deposition, and mass transport (diffusion) flux rates of Si atoms [42].

The growth of silicon nanowires in SLS mode can also be seen as a solid-state crystallization process which is driven by the Gibbs energy difference between a-Si (E_a) and silicon nanowires (E_c). From Fig. 85 we can see the synthesis process: Si atoms from a-Si:H firstly is absorbed into In droplet and a-Si/In interface forms; the absorbed Si atoms diffuse across the In droplet and finally the deposition of nanowires occurs at the rare SiNW/In interface. The Gibbs energy into the In droplet (E_i) could be described as following if we consider the Gibbs energy of Si atoms in SiNW (E_c) as zero:

$$\Delta\mu = E_i - E_c = kT \ln S = kT \ln(C_{Si}/C_{eq}^c) \qquad (13)$$

Where $S = C_{Si}/C_{eq}^{c}$ is the supersaturation state in the In droplet, the C_{Si} is the Si concentration at the SiNW/In interface and C_{eq}^{c} is the equilibrium Si concentration at the same interface, respectively.

4.3.1 The effect of H_2 plasma treatment

H_2 plasma treatment plays a dominant role in indium induced crystallization of silicon thus the growth of silicon nanowires. An experiment was firstly carried out on samples with 20 nm thick indium layers. The layer stack followed the experiments of indium deposition, which is In/a-Si on monocrystalline silicon substrates.

The same layer stacked samples underwent different conditions of treatment which are listed in table 25:

Table 25. Different durations of H_2 plasma treatment and annealing.

No. of samples	Layer stack	Duration of H_2 plasma	Duration of annealing	Temperature of H_2 plasma/annealing
1	20 nm In/50 nm a-Si/mono-Si	No	30 min	250 ˚C
2		1 min	30 min	
3		1 min	60 min	

Both H_2 plasma treatment and annealing were carried out in same reactor that performed PECVD, the conditions of these treatments are listed in table 26:

Table 26. Parameters of H_2 plasma treatment and annealing.

	H_2 plasma treatment	Annealing
Gas mixture and mass flow	H_2	N_2
Temperature (˚C)	250	250
Pressure (mbar)	0.9	0.9
RF power (W)	6	6

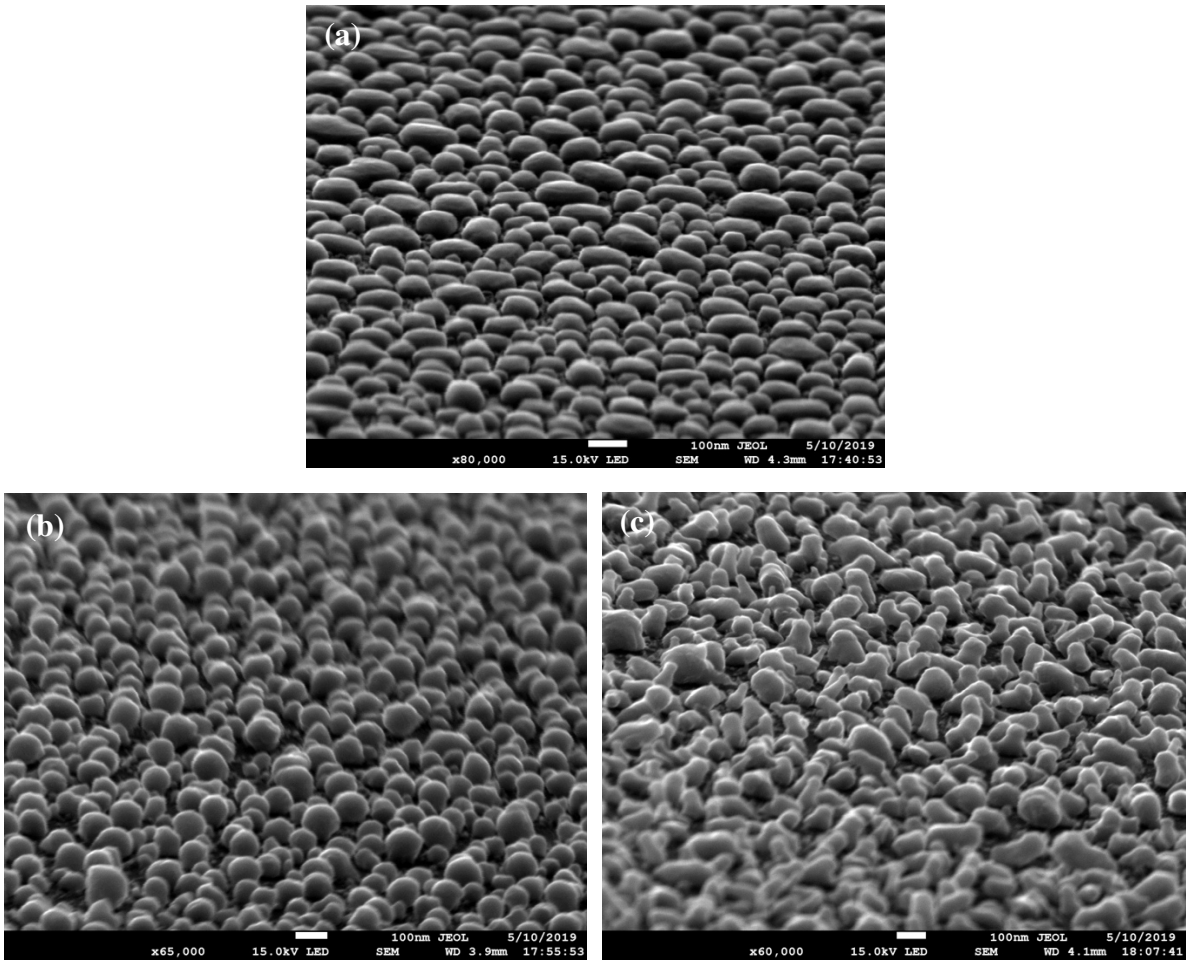

Fig. 86. SEM images of 20 nm In/50 nm a-Si samples tested under the conditions listed in table 23: (a) no H_2 plasma+30min annealing; (b) 1min H_2 plasma+30min annealing; (c) 1min H_2 plasma+60min annealing.

SEM observations were performed on each sample mentioned in table 23. From Fig. 86(a) we can see, only 30 minutes of annealing performed on indium layer did not significantly change the morphology of indium grains since they still maintain the polygonal shape as we saw in Fig. 80 (same layer stack with 20 nm thick of deposited indium). By comparing Fig. 86(a) and (b) we can realize that for same duration of annealing, only 1 minute of H_2 plasma treatment can transform indium grains into round shaped droplets which could initialize the crystallization thus the growth of possible silicon nanowires.

Once the indium layer was treated by H_2 plasma, annealing could continuously contribute to the growth of silicon nanowires. In Fig. 86(c), nearly half of the In droplets have been elongated into cone-like wires with the length of 100-200 nm for an annealing of 60 minutes after H_2 plasma treatment. This confirms that the annealing is only effective to the indium layers that underwent H_2 plasma treatment.

The H_2 plasma treatment is believed to deoxidize the indium oxide that covers the indium grains and change the indium into dissolved droplets. This treatment creates the interface between In drops and a-Si and therefore the Gibbs energy difference at the interface triggers the crystallization of a-Si. After plasma treatment, longer annealing (60 minutes) caused the growth of short nanowires because the temperature as high as 250 ˚C maintains In droplets in dissolving state to ensure the transition continues.

4.3.2 Different durations of plasma treatment

Since we have confirmed the effect of H_2 plasma treatment in the formation of nanowires, here in this section, we will focus on the different duration of H_2 plasma treatment (thermal annealing is not performed) to explore how different durations of plasma treatment could influence the synthesis of nanowires.

The tests were carried out on two different thicknesses of indium layer, one is 20 nm kept the same as the samples tested before, the other one is 50 nm, which is still the thickness that we tested in the experiment of indium evaporation. The parameters of H_2 plasma treatment are listed in table 27:

Table 27. Different durations of H_2 plasma treatment on 20nm and 50nm thick indium.

No. of samples	Layer stack	Duration of H_2 plasma treatment	Temperature of H_2 plasma
1	20 nm In/50 nm a-Si/Si-mono	30 min	250 ˚C
2		60 min	
3		90 min	
4	50 nm In/50 nm a-Si/Si-mono	30 min	
5		60 min	
6		90 min	

From 30 to 90 minutes of H_2 plasma treatment were performed on the samples. The results for 20 nm-thick-indium samples would be presented first.

By observing the four images (Fig. 87), we can clearly see the tendency of nanowires growing from the In droplets by increasing the duration of H_2 plasma treatment. The scale bar for Fig. 87 (a)(b)(d) and Fig. 87(c) is 100 nm and 1μm, respectively. The dramatic change took place between 30 and 60 minutes of plasma treatment. Only In droplets could be observed for 30 mins of H_2 plasma treatment, whereas nanowires are more 100 nm long after 60 minutes of the same plasma treatment process.

One interesting point of our results is that, the SLS nanowires grew off the substrate, which is considerably different from the IPSLS nanowires synthesized by L. Yu's group. It is also the first time to realize such off-plane SLS nanowires by using indium as the catalyst. Although the quasi-vertical nanowires have been synthesized by using nickel following SLS mode [109], nanowires in our study were fabricated at much lower temperature (250 ˚C compared to 950 ˚C in [109]).

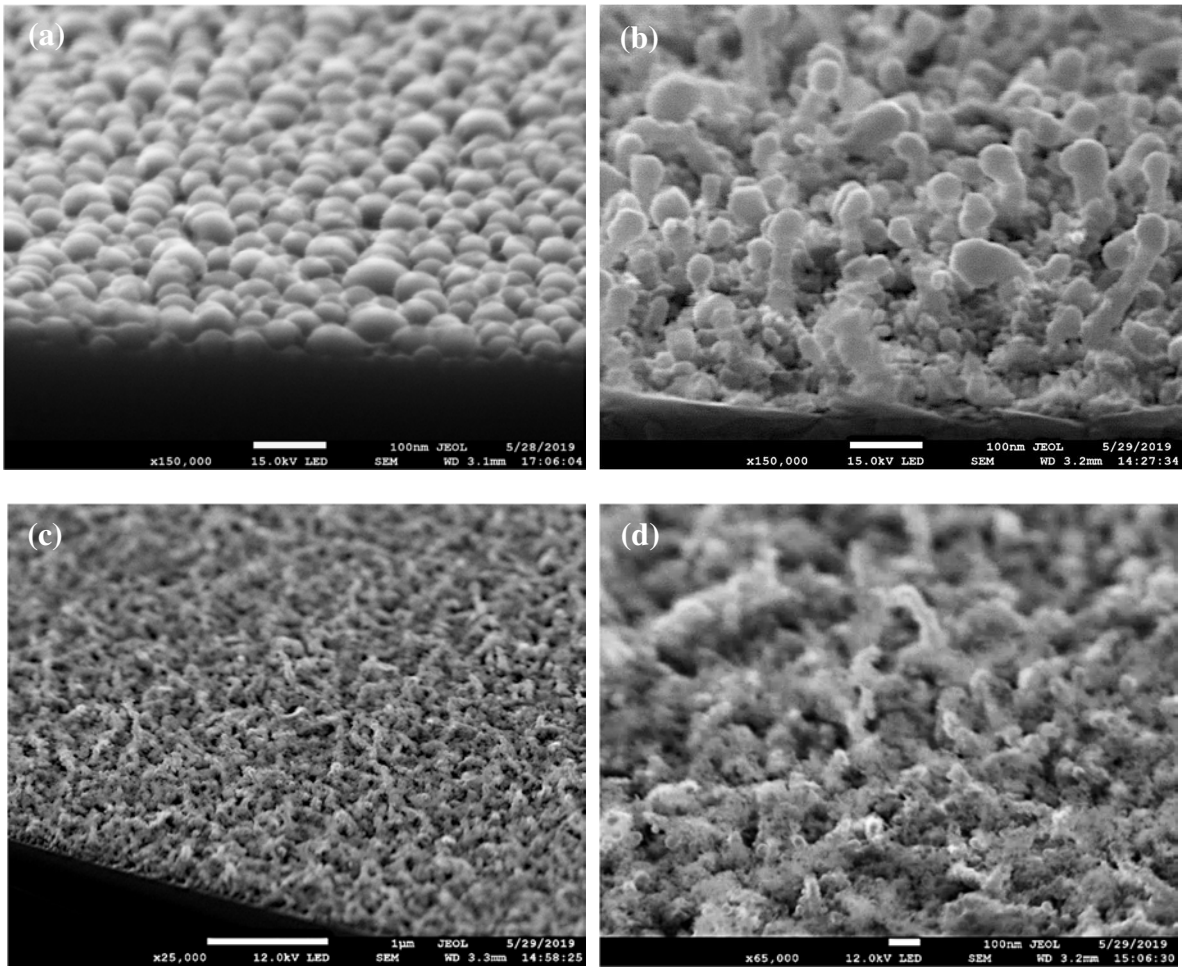

Fig. 87. SEM images of 20 nm In/50 nm a-Si samples tested under the conditions listed in table 25: (a) 30 min H_2 plasma; (b) 60 min H_2 plasma; (c)(d) 90 min H_2 plasma.

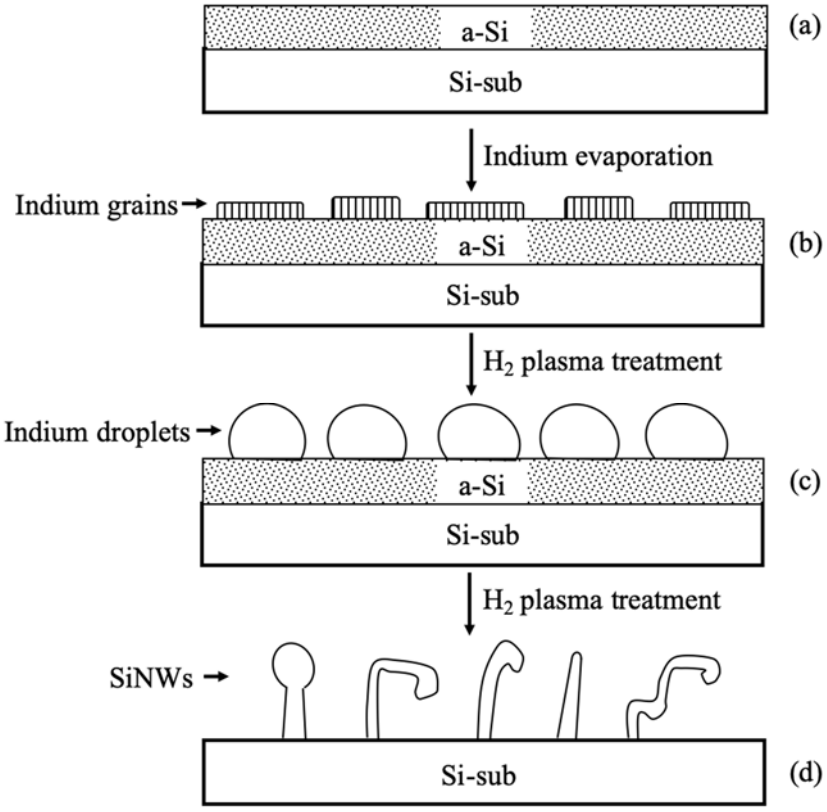

Fig. 88. Schematic of indium catalyzed SLS SiNWs growth.

Fig. 88 illustrates the SLS SiNWs growth catalyzed by indium. First, indium is evaporated onto a-Si, under SEM the indium layer is shown as indium grains (see Fig. 88(a)(b)). Then after H_2 plasma treatment is performed, the grains turn into indium droplets (Fig. 88(c)). When H_2 plasma treatment continues on these droplets, the dissolved silicon atoms will precipitate at the SiNW/In interface and form the SiNWs eventually (as shown in Fig. 88(d)).

In Fig. 87(b) we can observe the tips occur at the top of the nanowires since the diameter of these tips is larger than that of their corresponding nanowires. These tips are speculated as In droplets, which tells the nanowire growth in our study might be considered as the float growth process mentioned in Kurt W. Kolasinski's publication [110]. In contrast of float growth, the so called "root growth" mentioned in same publication defined as the droplets ending up at the bottom of the nanowires. The schematic illustrating the difference between float growth and root growth is shown in Fig. 89. In S. H. Yun et al's work [111], they found their VLS boron nanowires could switch between float growth and root growth. The key for realizing different growth modes is to control the synthesis temperature. A high temperature close to B-Au eutectic temperature would have the float growth mode whereas a much lower temperature would have

the root growth mode. Although here in our study the nanowires were fabricated following SLS mechanism, the synthesis mechanism is analogous in terms of eutectic droplets formation and atoms absorption and diffusion into the droplets. Therefore, the reason that we have indium tips on top of our nanowires is that the synthesis temperature (250 ˚C) is higher than indium eutectic temperature (157 ˚C).

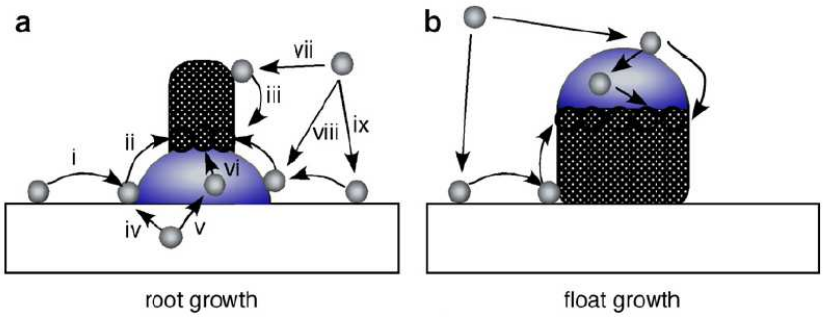

Fig. 89. The schematic of different growth mode of nanowires: (a) root growth, the particle stays at the bottom of the nanowire; (b) float growth, the particle remains at the top of the nanowire [110].

Another thing should be noticed is that, the nanowires we fabricated are not morphologically smooth, some wrinkles can be seen, especially for longer duration of H_2 plasma treatment (60 mins or more). When these "wrinkles" are observed on the nanowires, the corresponding nanowires are usually distorted which means less straight. This is probably related to the absorption rate (Va) and deposition rate (Vd) which happen at the a-Si/In interface and SiNW/In interface, respectively. One possible explanation for this is, when the synthesis is proceeding, the mismatch between absorption rate at the a-Si/In interface and deposition rate at the SiNW/In interface distorts the nanowires. Since Va and Vd would change all the time during the synthesis, the In droplets would be frequently pushed (Va<Vd) or pulled (Va>Vd), which changes the growth direction of the nanowires thus eventually causes the wrinkled and distorted nanowires.

The same set of H_2 plasma treatment (30, 60 and 90 min as the duration) was also tested on the 50 nm thick indium samples as shown in table 27. Since we have already performed 50 nm thick indium evaporation before, the larger In droplets are expected to bring some new results.

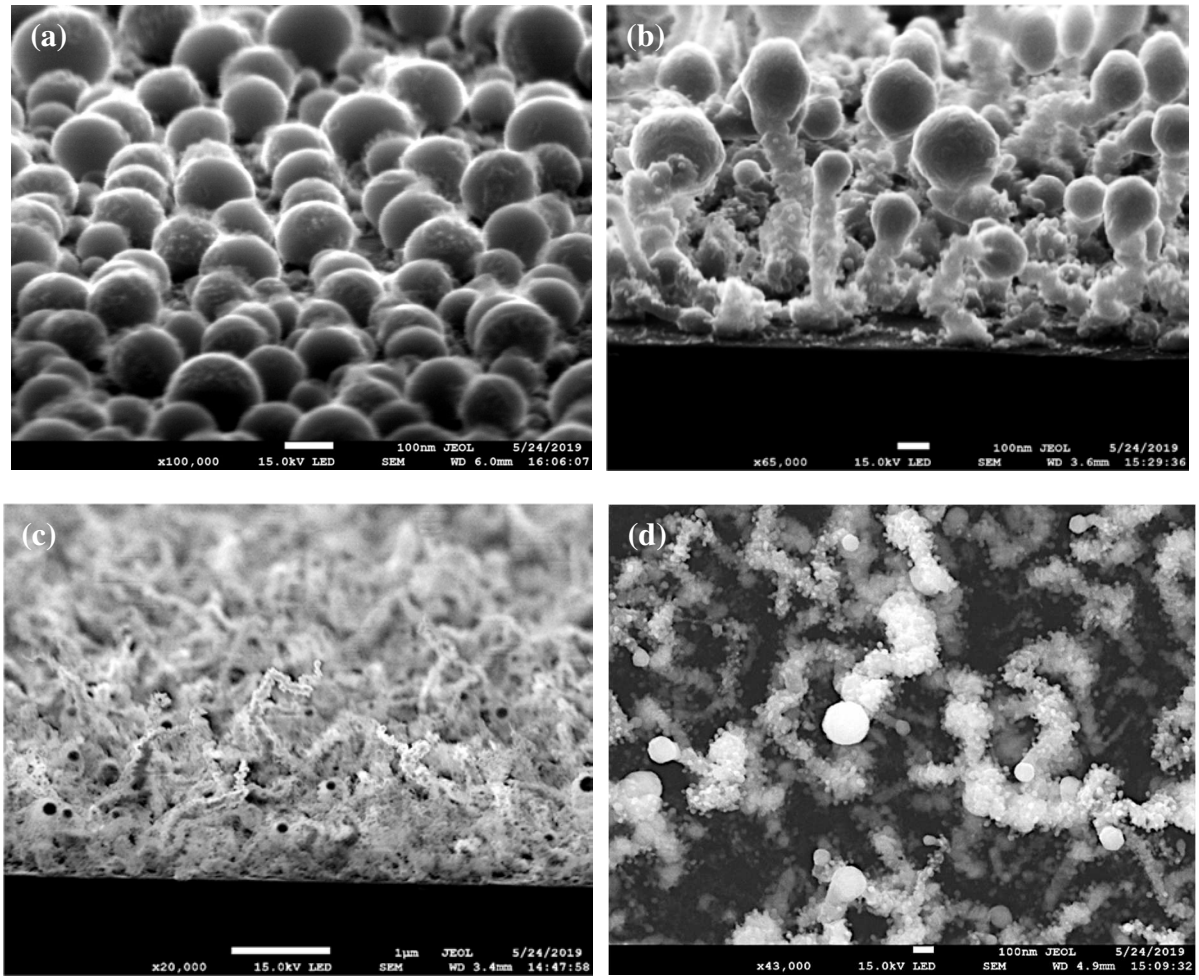

Fig. 90. SEM images of 50 nm In/50 nm a-Si samples tested under the conditions listed in table 25: (a) 30 min H_2 plasma; (b) 60 min H_2 plasma; (c)(d) 90 min H_2 plasma where (d) presents the top view.

Except for Fig 90(c) the scale bar is 1μm, the other three images have same 100 nm as the scale bar. Fig 90(a) shows the In droplets, which means 30 minutes are not enough to grow nanowires.

In Fig. 90(b), for 60 min of H_2 plasma treatment, nanowires are already very obvious. The length of these nanowires locates between 300 and 400 nm, which is 3-4 times longer than the 20 nm counterpart treated by the same condition of hydrogen plasma. It shows the length of nanowires fabricated under our process is higher with thicker indium layer.

The nanowires in Fig. 90(b) are generally vertical and they are found to be distorted and to have wrinkled shell as its 20 nm counterparts. Besides these, the “bumps” locating at the shell

of the nanowires in Fig. 90(b) are newly found. Since there are no such "bumps" can be seen on the In droplet tips, we suspect they are the indium residues left in the near surface of grown nanowires during the process. The indium residues inside the nanowires would be secondarily deoxidized by the hydrogen plasma into small droplets and eventually form the bumps which we observed on the surface of these nanowires. This could be confirmed by the texture of the tips onto the nanowires, no small bumps were observed just because the tips were already transferred into In droplets at the early phase of the whole process. In addition, one can observe the bigger size of top In droplets than for 20 nm In/a-Si sample because of the higher indium layer thickness.

We can see the same bumps in Fig. 90(c) and (d) for 90 min of H_2 plasma treatment. Fig. 90(c) presents the cross-sectional view while Fig. 90(d) presents the top view of nanowires. The nanowires tend to be more zigzag shape after 90 min of H_2 plasma treatment. In addition, the longest length is up to ~1μm which implies longer plasma treatment will further elongate the nanowire. This is also confirmed by the decreased average size of the left In droplets in Fig. 90(d) compared with the In droplets only after 60 min of same plasma treatment process. Longer plasma treatment would persistently consume the In droplets, which leads to smaller size of In droplets. In addition, as observed in Fig. 87(d), the size of bumps on the surface of nanowires is bigger, which could result in a higher apparent indium bump density on the surface of the nanowires. In fact, this apparent density should be probably related to an incipient secondary growth of nanowire on the surface because of the long duration of the H_2 plasma treatment.

4.3.3 Various thickness of indium layer

Based on the results presented in 4.3.1, 1 minute of H_2 plasma treatment has been confirmed enough to trigger the silicon nanowire growth. Here in this section, 10 min and 30 min of H_2 plasma treatment were carried out on 20 nm thick indium to see what the difference it would offer.

The parameters are listed below:

Table. 28. 10 min and 30 min as the duration of H_2 plasma treatment on 20nm thick indium.

No. of samples	Layer stack	Duration of H_2 plasma treatment	Temperature of H_2 plasma
1	20 nm In/50 nm a-Si/Si-mono	10 min	250 ˚C
2		30 min	

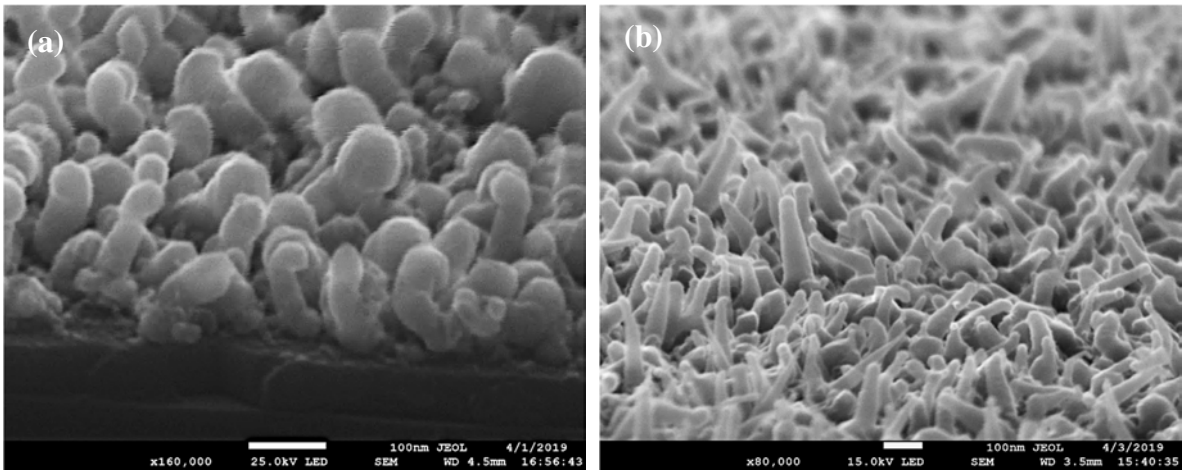

Fig. 91. SEM images of 20 nm In/50 nm a-Si samples underwent H_2 plasma treatment for different durations: (a) 10 min; (b) 30 min.

The scale bar for both figures in Fig. 91 is 100 nm. From Fig. 91 we can see nanowires in both durations of plasma treatment (10 min and 30 min). In Fig. 91(a) nanowires are in length of ~100-150 nm where in Fig. 91(b) the nanowires are in length of ~100-400 nm. One thing which is clear is that the length of most nanowires with 30 min H_2 plasma treatment is longer than that of nanowires with only 10 min H_2 plasma treatment. It reveals that the longer H_2 plasma treatment will dramatically promote the length of the nanowires. This is consistent with the results of the 50 nm thick indium samples but with longer H_2 plasma treatment in 4.3.2.

One interesting thing is that, as we can see in Fig. 91(b), the nanowires have tapered shape which means the diameter of the nanowires decreases gradually from its bottom to its top. The possible explanation of this phenomenon is that the absorbed Si atoms into the In droplets decrease when the length of nanowire keeps increasing. The process is not obvious for shorter nanowires (see Fig. 91(a)), but becomes dominant when nanowires' length reaches a limit.

According to S. K. Chong et al's work [112], the existence of the tips on the fabricated nanowires is simply related to the size of In droplets before the growth of nanowires. Bigger In droplets would tend to have tips after nanowire growth whereas smaller droplets would have unobvious tips. This is partially right because they did not take the duration of plasma treatment into account. For same indium thickness, In tips are obvious in Fig. 91(a) for 10 min of H_2 plasma treatment whereas the nanowires show unnoticeable tips and tapered shape. This means the existence of In tips on top of nanowires not only depends on the initial size of In droplets but also depends on the duration of H_2 plasma treatment. Moreover, bumps on the SiNWs' surface inducing possible secondary growth of nanowires is not observed, this is probably explained by the fact of too short H_2 plasma treatment.

On the other hand, what is not consistent with the 20 nm thick indium samples undergone exact same H_2 plasma treatment in 4.3.2 (30 min of H_2 plasma treatment) is no wrinkles could be found on the nanowires fabricated in this section. In addition, in the new round of test, nanowires are widely observed just after 10 min of H_2 plasma treatment whereas no nanowires detected even after 30 min of same plasma treatment for previous test in 4.3.2. This could be attributed to undesirable indium oxide formed at the interface of In droplet and a-Si layer.

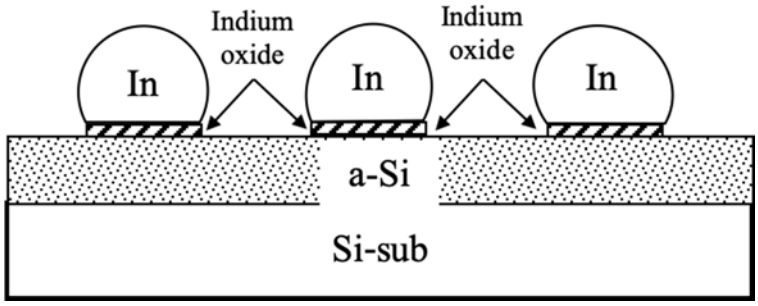

Fig. 92. Schematic of indium oxide barriers locating at the In droplet/a-Si interface.

As shown in Fig. 92, the indium oxide existing at the In droplet/a-Si interface would act as the barrier of Si atoms absorption from a-Si to In droplet. Therefore, it would require much longer duration of H_2 plasma treatment to absorb enough Si atoms into In droplet to finally trigger the SiNW deposition. This could explain why in previous test, it took us 60 minutes to have nanowires having length just comparable with the nanowires in the new test but undergone only 10 minutes of the same plasma treatment.

How did the indium oxide form at the interface? It is likely due to the indium thermal evaporation. The presence of a residual indium oxide at the base of the indium droplets is probably related to our modus operandi. Indeed, the deposition of the amorphous silicon layer and/or the evaporation of indium takes place in two different reactors. Although hydrogen plasma allows indium to be deoxidized at first when placed in the PECVD reactor, the oxide at the base of the indium droplets may remain. To avoid the persistence of such oxide, it would be ideal to perform hydrogen plasma before and after indium deposition, which would require the use of a single reactor. In addition, our operating conditions regarding the thermal evaporation of indium do not guarantee the absence of indium oxide at the base of the droplets. Indeed, during the melting of indium, a thin layer of indium oxide is observed on the surface which must be evaporated before exposing the samples to indium in vapor form. This tricky operation is very difficult to reproduce in our case according to very slow evaporation kinetics specifically to indium. This means that the indium oxide evaporation at the beginning phase of deposition is possible, and therefore of indium oxide at the base of indium droplets.

Since we deposited 10 nm, 20 nm and 50 nm thick indium layers in previous test, we performed nanowire synthesis also on 10 nm and 50 nm thick indium layer samples which are coming from the same batch as the samples tested just before in this section. This time, the duration of H_2 plasma treatment was fixed at 30 minutes and the temperature was still kept at 250 ˚C. The parameters are listed below:

Table. 29. H_2 plasma treatment on 10 nm and 50 nm thick indium.

No. of samples	Layer stack	Duration of H_2 plasma treatment	Temperature of H_2 plasma
1	10 nm In/50 nm a-Si/Si-mono	30 min	250 ˚C
2	50 nm In/50 nm a-Si/Si-mono		

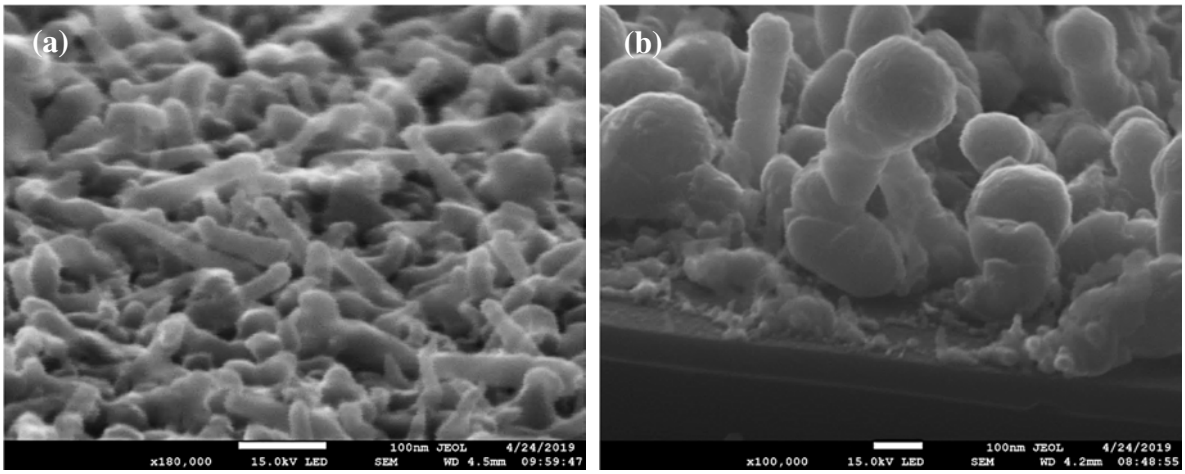

Fig. 93. SEM images of samples underwent 30 min of H_2 plasma treatment with different thickness of indium layer: (a) 10 nm In/50 nm a-Si; (b) 50 nm In/50 nm a-Si.

The scale bar is 100 nm in both figures. The proximate length range of nanowires for 10 nm and 50 nm of indium layer is ~50-100 nm and ~200-500 nm, respectively. If we put Fig. 91(b) and Fig. 93 together to compare (since the only difference on these three samples is thickness of indium layer), we can find that the nanowires are more vertical after H_2 plasma treatment as thickness of indium layer increases. In other words, the verticality of synthesized nanowires is related to the indium layer thickness. This could be attributed to the volume of In droplets at the early stage of plasma treatment since the bigger In droplets would absorb more Si atoms at the same time compared to smaller counterparts. The larger flux of Si atoms diffusing in In droplets would benefit the vertical growth of the nanowires.

Some nanowires in Fig. 93(b) do not show tapered shape as we observed in Fig. 91(b) and Fig. 93(a). This could also be explained by the bigger In droplets for 50 nm thick indium layer and relatively short duration of plasma treatment. The SiNWs grown from different diameter of In droplets are found having different growth rates while the other growing parameters were kept the same in [44]. According to their work, the flux of absorbed Si atoms is inversely proportional to the diameter of the In droplet, which could be applied for the nanowires in our study since the mechanisms of synthesis resemble to a large extent.

4.4 Conclusion

In this chapter, we focused on the investigation of indium induced nanowire fabrication. The idea was originally to explore the possibility of silicon nanowires fabrication by the help

of metal catalyst at low temperature since we use the indium as catalyst which has the low eutectic temperature.

We first tested the indium evaporation and characterized the indium layers by SEM and AFM. These images both show polygonal shapes of indium grains and the size of these grains is proportional to the thickness of deposited indium.

Secondly, the investigation of silicon nanowire growth was carried out. We adopted the "indium-amorphous silicon-silicon substrate" stack to perform the nanowire synthesis. Several different conditions of H_2 plasma treatment and different thickness of indium (10, 20 and 50 nm) have been tested and characterized by SEM. The fabricated nanowires are firstly found to be the SLS growth mode with the help of indium at low temperature (250 ˚C).

The fabricated nanowires tend to show tapered shape with the indium tip on top of them, and more importantly, the nanowires are quasi vertical. The length of the nanowires strongly depends on the duration of H_2 plasma treatment and the thickness of indium layer, where the longer duration of plasma treatment and thicker indium lead to longer nanowires in general. The mechanism of the nanowires was also briefly discussed since we are still at the early phase of the study.

Conclusions and perspectives

The subject of this thesis was to investigate low temperature SiNWs synthesis approaches. All the process researched in this thesis was implemented at the temperature lower than 300 ˚C, which is well serving the purpose of low-cost flexible substrates compatibility.

First, we reviewed two most important low temperature techniques that dedicated to deposition and crystallization of a-Si or μc-Si layer compatible for flexible substrates. Reactive sputtering, hot-wire CVD and PECVD could all work at temperature as low as 300 ˚C. PECVD is more frequently adopted for thin film devices application flexible substrates. Different crystallization methods have also been discussed. Mainstream methods like MIC and MILC were reviewed at first, some other approaches such as ELC, H_2 plasma induced crystallization, C-beam crystallization and BLA were presented afterwards. They all meet the limitation of temperature and show promising quality of crystallinity at the same time. Nevertheless, metal induced crystallization features more because of the easy realization. Especially indium induced crystallization could provide even lower crystallization temperature compared to the other metal materials.

ICP-CVD has accordingly researched in chapter 2 on the optimization of SiO_2 deposition and electrical properties of SiO_2. Besides, the properties of ICP-CVD silicon layer have been presented by fabricating the ICP-CVD TFTs. Two batches of capacitors were fabricated under various parameters, and optimized parameters were obtained after characterizing these capacitors in terms of HFCV and breakdown field. LF power of 500W, RF power of 50W, pressure of 2.5mTorr and temperature of 20˚C have been validated. In conclusion, SiO_2 layers deposited by ICP-CVD can yield good electrical properties and act as the insulating layers in TFTs. Besides, the ICP-CVD TFTs with gate oxide and microcrystalline silicon active layer deposited without deliberately heating the substrate is demonstrated. After thermal annealing at temperature no higher than 220 ˚C, TFTs yield competitive electrical properties: V_{TH} of 3.7V, I_{ON}/I_{OFF} of 6.4×10^2, field effect mobility of 1.2 cm^2/Vs and subthreshold slope of 3.9 V/dec. Thanks to the low temperature process of ICP-CVD, it offers the opportunity to explore the applications on flexible substrates.

Following the optimized silicon and SiO_2 deposition by ICP-CVD, the synthesis of SiNWs has been investigated by coupling ICP-CVD and spacer method. First of all, SiO_2 steps have been optimized on Microsys 400 RIE system, and the relatively vertical sidewalls of SiO_2 steps can be achieved under RF power of 50W, CF_4 gas flow of 30sccm and pressure of 4mTorr. This set of etching parameters are perfectly suitable for SiO_2 deposited by using ICP-CVD. Etching of silicon that is deposited by PECVD leads to the formation of silicon nanowires has not been

perfectly optimized even some efforts were made. Some residues can be obtained when RF power, SF_6 gas flow and pressure are set at 30W, 20sccm and 5mTorr, respectively. Fortunately, silicon nanowires are finally obtained when the deposition method of SiO_2 and silicon changed from PECVD to ICP-CVD. Thanks to better uniformity ICP-CVD provides, silicon nanowires can be detected after RIE of μc-Si layer. RF power of 30W, SF_6 gas flow of 20sccm and pressure of 5mTorr are the optimized parameters for μc-Si etching.

Same process has been performed after the first successful result about nanowires, it was found that the process could not be reproduced. By evaluating the step coverage of ICP-CVD Si layer under SEM, we can tell that poor step coverage of Si layer leads to failure of fabricating nanowires. It is reasonable to speculate that the nanowires could be stably reproduced when ICP-CVD Si coverage is improved.

In last chapter, still with the objective of providing for SiNWs synthesis at temperatures lower than 300 ˚C, we have investigated indium as catalyst. We observed polygonal shapes of indium grains after thermal evaporation and the size of these grains is proportional to the thickness of deposited indium. In addition, the investigation of silicon nanowire growth was carried out. The fabricated nanowires are firstly found to be the 3D SLS growth mode with the help of indium at low temperature (250 ˚C). The fabricated nanowires tend to show tapered shape with the indium tip on top of them, and more importantly, the nanowires are quasi vertical. The length of the nanowires strongly depends on the duration of H_2 plasma treatment and the thickness of indium layer, where the longer duration of plasma treatment and thicker indium lead to longer nanowires in general.

Unfortunately, the technique of indium induced SLS SiNWs is not very stable currently. We suspect that this is because the indium oxide formed at the interface between indium droplets and a-Si layer. The indium oxide forms during the thermal evaporation of indium since there is always oxidized indium drops which are unexpected to evaporate onto the a-Si layer. To solve this problem, we propose two ways.

First, using the same reactor to perform indium deposition and following H_2 plasma treatment. In this way, the indium would not expose to the air between two process (indium evaporation and H_2 plasma treatment), which could reduce the risk of re-oxidation of the indium. In this case, the well-controlled 3D growth of indium catalyzed SLS SiNWs would offer possibilities for flexible electronics and sensors applications.

Second, using inverted layer stack to perform SLS SiNWs growth. In this thesis, we used In/a-Si/Si-sub layer stack where the indium layer is deposited onto a-Si. If the stack of a-Si/In/Si-sub is used, the indium oxide on the upper surface of indium droplets will be surely deoxidized by priorly performing H_2 plasma treatment. Then comes the a-Si deposition, this will ensure no existence of the indium oxide at the a-Si/In interface. In this case, in plane SLS crystallization of the a-Si layer is expected. Such indium-induced crystallization process would benefit for silicon layer functional layer used for the synthesis of silicon nanowires by spacer method. In addition, it could also benefit for the fabrication of TFTs with expected better electrical performances.

The first results on ICP-CVD TFTs enable the possibility of flexible applications. Since the process temperature of ICP-CVD can be controlled under 220 ˚C, it will work well on the series of flexible substrates. In addition, the TFTs have been successfully fabricated, which indicates some more complex electronic devices could be realized on these flexible substrates.

Following research on the nano spacer fabrication is facing a problem of reproducibility. The nano spacers could be obtained occasionally by using ICP-CVD. The reason is presumably the poor step coverage of silicon that ICP-CVD delivers. The future work could continue to focus on the ICP-CVD to optimize the silicon step coverage. Another reason could be related to the crystallinity of deposited silicon layer by ICP-CVD.

To improve the silicon crystallinity, indium induced crystallization is a good candidate thanks to its low eutectic temperature. In fact, in this thesis, we have investigated the indium catalyzed SiNWs growth which we believe could yield crystallized silicon and silicon nanowires at the same time.

References

[1] W. S. Wong and A. Salleo, *Flexible Electronics: Materials and Applications*. Springer Science & Business Media, 2009.

[2] S. Chang and S. Sivoththaman, "Development of a low temperature MEMS process with a PECVD amorphous silicon structural layer," *J. Micromech. Microeng.*, vol. 16, no. 7, p. 1307, 2006.

[3] G. Fortunato, A. Pecora, and L. Maiolo, "Polysilicon thin-film transistors on polymer substrates," *Materials Science in Semiconductor Processing*, vol. 15, no. 6, pp. 627–641, Dec. 2012.

[4] J. Musil, P. Baroch, J. Vlček, K. H. Nam, and J. G. Han, "Reactive magnetron sputtering of thin films: present status and trends," *Thin Solid Films*, vol. 475, no. 1, pp. 208–218, Mar. 2005.

[5] M. Pinarbasi, N. Maley, A. Myers, and J. R. Abelson, "Hydrogenated amorphous silicon films deposited by reactive sputtering: The electronic properties, hydrogen bonding and microstructure," *Thin Solid Films*, vol. 171, no. 1, pp. 217–233, Apr. 1989.

[6] C. S. McCormick, C. E. Webe, and J. R. Abelson, "An Amorphous Silicon Thin Film Transistor Fabricated at 125˚C by dc Reactive Magnetron Sputtering," *MRS Online Proceedings Library Archive*, vol. 424, Jan. 1996.

[7] H. Seifarth, R. Grötzschel, A. Markwitz, W. Matz, P. Nitzsche, and L. Rebohle, "Preparation of SiO_2 films with embedded Si nanocrystals by reactive r.f. magnetron sputtering," *Thin Solid Films*, vol. 330, no. 2, pp. 202–205, Sep. 1998.

[8] A. Saboundji *et al.*, "Top-gate microcrystalline silicon TFTs processed at low temperature (<200 ˚C)," *Thin Solid Films*, vol. 487, no. 1, pp. 227–231, Sep. 2005.

[9] J. P. Conde, P. Alpuim, M. Boucinha, J. Gaspar, and V. Chu, "Amorphous and microcrystalline silicon deposited by hot-wire chemical vapor deposition at low substrate temperatures: application to devices and thin-film microelectromechanical systems," *Thin Solid Films*, vol. 395, no. 1, pp. 105–111, Sep. 2001.

[10] H. Matsumura, H. Umemoto, and A. Masuda, "Cat-CVD (hot-wire CVD): how different from PECVD in preparing amorphous silicon," *Journal of Non-Crystalline Solids*, vol. 338, no. Supplement C, pp. 19–26, Jun. 2004.

[11] R. E. Schropp, "Hot Wire Chemical Vapor Deposition: Recent Progress, Present State of the Art and Competitive Opportunities," *ECS Trans.*, vol. 25, no. 8, pp. 3–14, Sep. 2009.

[12] P. Alpuim, V. Chu, and J. P. Conde, "Amorphous and microcrystalline silicon films grown at low temperatures by radio-frequency and hot-wire chemical vapor deposition," *Journal of Applied Physics*, vol. 86, no. 7, pp. 3812–3821, Sep. 1999.

[13] P. Brogueira, J. P. Conde, S. Arekat, and V. Chu, "Amorphous and microcrystalline silicon films deposited by hot-wire chemical vapor deposition at filament temperatures between 1500 and 1900 ˚C," *Journal of Applied Physics*, vol. 79, no. 11, pp. 8748–8760, Jun. 1996.

[14] "Plasma Enhanced Chemical Vapour Deposition (PECVD)," *Oxford Instruments*. [Online]. Available: https://plasma.oxinst.com/campaigns/technology/pecvd.

[15] J. Batey and E. Tierney, "Low-temperature deposition of high-quality silicon dioxide by plasma-enhanced chemical vapor deposition," *Journal of Applied Physics*, vol. 60, no. 9, pp. 3136–3145, Nov. 1986.

[16] J. Alonso, A. Ortiz, and C. Falcony, "Low temperature SiO_2 films deposited by plasma enhanced techniques," *Vacuum*, vol. 43, no. 8, pp. 843–847, Aug. 1992.

[17] S. C. Deshmukh and E. S. Aydil, "Low-temperature plasma enhanced chemical vapor deposition of SiO_2," *Appl. Phys. Lett.*, vol. 65, no. 25, pp. 3185–3187, Dec. 1994.

[18] S. C. Deshmukh and E. S. Aydil, "Investigation of low temperature SiO_2 plasma enhanced chemical vapor deposition," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 14, no. 2, pp. 738–743, Mar. 1996.

[19] A. Bousquet, A. Goullet, C. Leteinturier, N. Coulon, and A. Granier, "Influence of ion bombardment on structural and electrical properties of SiO_2 thin films deposited from O_2/HMDSO inductively coupled plasmas under continuous wave and pulsed modes," *The European Physical Journal - Applied Physics*, vol. 42, no. 1, pp. 3–8, Apr. 2008.

[20] C.-S. Yang, L. L. Smith, C. B. Arthur, and G. N. Parsons, "Stability of low-temperature amorphous silicon thin film transistors formed on glass and transparent plastic substrates," *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures Processing, Measurement, and Phenomena*, vol. 18, no. 2, pp. 683–689, Mar. 2000.

[21] C. Koch, M. Ito, and M. Schubert, "Low-temperature deposition of amorphous silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 68, no. 2, pp. 227–236, May 2001.

[22] Z. Meng, M. Wang, and M. Wong, "High performance low temperature metal-induced unilaterally crystallized polycrystalline silicon thin film transistors for system-on-panel applications," *IEEE Transactions on Electron Devices*, vol. 47, no. 2, pp. 404–409, Feb. 2000.

[23] A. T. Voutsas, "A new era of crystallization: advances in polysilicon crystallization and crystal engineering," *Applied Surface Science*, vol. 208, no. Supplement C, pp. 250–262, Mar. 2003.

[24] J. F. Michaud, R. Rogel, T. Mohammed-Brahim, M. Sarret, and O. Bonnaud, "Solid phase post-treatment of polysilicon films by a continuous argon laser," *Thin Solid Films*, vol. 487, no. 1, pp. 81–84, Sep. 2005.

[25] Z. Wang, L. P. H. Jeurgens, J. Y. Wang, and E. J. Mittemeijer, "Fundamentals of Metal-induced Crystallization of Amorphous Semiconductors," *Adv. Eng. Mater.*, vol. 11, no. 3, pp. 131–135, Mar. 2009.

[26] H. P. Zhou, M. Xu, S. Xu, L. L. Liu, C. X. Liu, L. C. Kwek, and L. X. Xu, "Hydrogen-plasma-induced Rapid, Low-Temperature Crystallization of μm-thick a-Si:H Films," *Sci. Rep.*, vol. 6, pp. 32716, Sep. 2016.

[27] M. S. Haque, H. A. Naseem, and W. D. Brown, "Aluminum-induced crystallization and counter-doping of phosphorous-doped hydrogenated amorphous silicon at low temperatures," *Journal of Applied Physics*, vol. 79, no. 10, pp. 7529–7536, May 1996.

[28] R. Kishore, C. Hotz, H. A. Naseem, and W. D. Brown, "Aluminum-Induced Crystallization of Amorphous Silicon (α-Si:H) at 150˚C," *Electrochem. Solid-State Lett.*, vol. 4, no. 2, pp. G14–G16, Feb. 2001.

[29] M. Shahidul Haque, H. A. Naseem, and W. D. Brown, "Interaction of aluminum with hydrogenated amorphous silicon at low temperatures," *Journal of Applied Physics*, vol. 75, no. 8, pp. 3928–3935, Apr. 1994.

[30] H. Kim, D. Kim, G. Lee, D. Kim, and S. H. Lee, "Polycrystalline Si films formed by Al-induced crystallization (AIC) with and without Al oxides at Al/a-Si interface," *Solar Energy Materials and Solar Cells*, vol. 74, no. 1, pp. 323–329, Oct. 2002.

[31] Y. Sugimoto, N. Takata, T. Hirota, K. Ikeda, F. Yoshida, H. Nakashima and H. Nakashima, "Low-Temperature Fabrication of Polycrystalline Si Thin Film Using Al-Induced Crystallization without Native Al Oxide at Amorphous Si/Al Interface," Jpn. J. Appl. Phys., vol. 44, no. 7R, p. 4770, Jul. 2005.

[32] Ch. Kishan Singh, T. Tah, K. K. Madapu, K. Saravanan, S. Ilango, and S. Dash, "Au induced crystallization and layer exchange in a-Si/Au thin film on glass below and above the eutectic temperature," Journal of Non-Crystalline Solids, vol. 460, no. Supplement C, pp. 130–135, Mar. 2017.

[33] M. Jeon, C. Jeong, and K. Kamisako, "Tin induced crystallisation of hydrogenated amorphous silicon thin films," *Energy Materials*, vol. 5, no. 1, pp. 875–878, Mar. 2010.

[34] K. H. Lee, Y. K. Fang, and S. H. Fan, "Au metal-induced lateral crystallisation (MILC) of hydrogenated amorphous silicon thin film with very low annealing temperature and fast MILC rate," *Electronics Letters*, vol. 35, no. 13, pp. 1108–1109, Jun. 1999.

[35] C. W. Byun, S. W. Son, Y. W. Lee, H. M. Kang, S. A. Park, W. C. Lim, T. Li and S. K. Joo, "Improvement of Electrical Performance of Metal-Induced Laterally Crystallized Polycrystalline Silicon Thin-Film Transistors," *J. Electrochem. Soc.*, vol. 159, no. 4, pp. J115–J121, Jan. 2012.

[36] S-W. Lee, Y-C. Jeon and S-K. Joo, "Pd induced lateral crystallization of amorphous Si thin films", *Applied Physics Letters*, vol. 66, no. 13, pp. 1671-1673, Jan. 1995.

[37] W. Knaepen, C. Detavernier, R. L. Van Meirhaeghe, J. Jordan Sweet, and C. Lavoie, "In-situ X-ray Diffraction study of Metal Induced Crystallization of amorphous silicon," *Thin Solid Films*, vol. 516, no. 15, pp. 4946–4952, Jun. 2008.

[38] R. Heimburger, N. Deßmann, T. Teubner, H.-P. Schramm, T. Boeck, and R. Fornari, "Polycrystalline silicon films on glass grown by amorphous–liquid–crystalline transition at temperatures below 330˚C," *Thin Solid Films*, vol. 520, no. 6, pp. 1784–1788, Jan. 2012.

[39] R. Bansen, R. Heimburger, J. Schmidtbauer, T. Teubner, T. Markurt, C. Ehlers and T. Boeck, "Crystalline silicon on glass by steady-state solution growth using indium as solvent," *Appl. Phys. A*, vol. 119, no. 4, pp. 1577–1586, Jun. 2015.

[40] L. Yu, P.-J. Alet, G. Picardi, and P. Roca i Cabarrocas, "An In-Plane Solid-Liquid-Solid Growth Mode for Self-Avoiding Lateral Silicon Nanowires," *Phys. Rev. Lett.*, vol. 102, no. 12, p. 125501, Mar. 2009.

[41] L. Yu and P. Roca i Cabarrocas, "Initial nucleation and growth of in-plane solid-liquid-solid silicon nanowires catalyzed by indium," *Phys. Rev. B*, vol. 80, no. 8, p. 085313, Aug. 2009.

[42] L. Yu and P. R. i Cabarrocas, "Growth mechanism and dynamics of in-plane solid-liquid-solid silicon nanowires," *Phys. Rev. B*, vol. 81, no. 8, p. 085323, Feb. 2010.

[43] P. M. Smith, P. G. Carey, and T. W. Sigmon, "Excimer laser crystallization and doping of silicon films on plastic substrates," *Appl. Phys. Lett.*, vol. 70, no. 3, pp. 342–344, Jan. 1997.

[44] T. Pier, K. Kandoussi, C. Simon, N. Coulon, T. Mohammed-Brahim, and H. Lhermite, "Excimer laser crystallization of microcrystalline silicon for TFTs on flexible substrate," *Journal of Non-Crystalline Solids*, vol. 354, no. 19, pp. 2300–2304, May 2008.

[45] M. He, R. Ishihara, E. J. Neihof, Y. van Andel, H. Schellevis, W. Metselaar and K. Beenakker, "Large Polycrystalline Silicon Grains Prepared by Excimer Laser Crystallization of Sputtered Amorphous Silicon Film with Process Temperature at 100 ˚C," *Jpn. J. Appl. Phys.*, vol. 46, no. 3S, pp. 1245-1249, Mar. 2007.

[46] S. Sriraman, S. Agarwal, E. S. Aydil, and D. Maroudas, "Mechanism of hydrogen-induced crystallization of amorphous silicon," *Nature*, vol. 418, no. 6893, p. 62, 2002.

[47] S. W. Lee, J. S. Kang, and K. C. Park, "Carbon-nanotube electron-beam (C-beam) crystallization technique for silicon TFTs," *Journal of the Korean Physical Society*, vol. 68, no. 4, pp. 528–532, Feb. 2016.

[48] T. Noguchi, Y. Chen, T. Miyahira, J. de Dieu Mugiraneza, Y. Oino, Y. Iida, E. Sahota and M. Terao, "Advanced Micro-Polycrystalline Silicon Films Formed by Blue-Multi-Laser-Diode Annealing," *Jpn. J. Appl. Phys.*, vol. 49, no. 3S, p. 03CA10, Mar. 2010.

[49] J. de Dieu Mugiraneza, K. Shirai, T. Suzuki, T. Okada, T. Noguchi, H. Matsushima, T. Hashimoto, Y. Ogino and E. Sahota, "Crystallization of silicon films of submicron thickness by blue-multi-laser-diode annealing," *Journal of the Korean Physical Society*, vol. 60, no. 1, pp. 88–93, Jan. 2012.

[50] S. Jin, M. Mativenga, and J. Jang, "P-7: High Performance LTPS Thin-film Transistors using Low Cost Polycrystalline Silicon by Blue Laser Annealing," *SID Symposium Digest of Technical Papers*, vol. 47, no. 1, pp. 1143–1146, May 2016.

[51] J. W. Lee, K. D. Mackenzie, D. Johnson, J. N. Sasserath, S. J. Pearton, and F. Ren, "Low Temperature Silicon Nitride and Silicon Dioxide Film Processing by Inductively Coupled Plasma Chemical Vapor Deposition," *J. Electrochem. Soc.*, vol. 147, no. 4, pp. 1481–1486, Apr. 2000.

[52] B. Y. Moon, J. H. Youn, S. H. Won, J. Jang, and S. M. Pietruszko, "Study on the Polycrystalline Silicon Films Deposited by Inductively Coupled Plasma Chemical Vapor Deposition," *MRS Online Proceedings Library Archive*, vol. 685, ed 2001.

[53] "Corial 210D ICP-CVD system," *Corial*, 16-Jan-2017.

[54] J. Jung, J. Kwon, Y. Park, D. Kim, H. Cho, K. Park, W. Xianyu and H. Yin, "SiO_2 Film Formed by Inductivity Coupled Plasma Chemical Vapor Deposition at Low Temperature for Poly-Si TFT," *Journal of the Korean Physical Societ*y, vol. 45, pp, S861-S863, Dec. 2004.

[55] S.-M. Han, M.-Y. Shin, J.-H. Park, and M.-K. Han, "High quality SiO_2 gate insulator suitable for poly-Si TFTs on plastic substrates employing inductively coupled plasma-chemical

vapor deposition with N2O plasma treatment and excimer laser annealing," Journal of Non-Crystalline Solids, vol. 352, no. 9, pp. 1434–1437, Jun. 2006.

[56] G. Nogay, E. Özkol, S. Ilday, and R. Turan, "Structural peculiarities and aging effect in hydrogenated a-Si prepared by inductively coupled plasma assisted chemical vapor deposition technique," *Vacuum*, vol. 110, pp. 114–120, Dec. 2014.

[57] J.-H. Wu, J.-M. Shieh, B.-T. Dai, and Y. S. Wu, "Synthesis of Microcrystalline Silicon at Room Temperature Using ICP," *Electrochem. Solid-State Lett.*, vol. 7, no. 6, pp. G128–G130, Jun. 2004.

[58] B. Yeon Moon, J. Hyoung Youn, S. Hwan Won, and J. Jang, "Polycrystalline silicon film deposited by ICP-CVD," *Solar Energy Materials and Solar Cells*, vol. 69, no. 2, pp. 139–145, Sep. 2001.

[59] D. K. Schroder, *Semiconductor Material and Device Characterization*. John Wiley & Sons, 2015.

[60] E. H. Nicollian and J. R. Brews, *MOS /metal oxide semiconductor/ physics and technology*. 1982.

[61] S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*. John Wiley & Sons, 2006.

[62] N. M. Ravindra and J. Zhao, "Fowler-Nordheim tunneling in thin SiO_2 films," *Smart Mater. Struct.*, vol. 1, no. 3, p. 197, Sep. 1992.

[63] J. F. Verweij and J. H. Klootwijk, "Dielectric breakdown I: A review of oxide breakdown," *Microelectronics Journal*, vol. 27, no. 7, pp. 611–622, Oct. 1996.

[64] E. Harari, "Dielectric breakdown in electrically stressed thin films of thermal SiO_2," *Journal of Applied Physics*, vol. 49, no. 4, pp. 2478–2489, Apr. 1978.

[65] D. J. DiMaria, E. Cartier, and D. Arnold, "Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon," *Journal of Applied Physics*, vol. 73, no. 7, pp. 3367–3384, Apr. 1993.

[66] H. Kotani, M. Matsuura, A. Fujii, H. Genjou, and S. Nagao, "Low-temperature APCVD oxide using TEOS-ozone chemistry for multilevel interconnections," in *International Technical Digest on Electron Devices Meeting*, Washington, DC, USA, 1989, pp. 669–672.

[67] J. Lee, I.- Chen, and C. Hu, "Comparison between CVD and thermal oxide dielectric integrity," *IEEE Electron Device Letters*, vol. 7, no. 9, pp. 506–509, Sep. 1986.

[68] S. Rojas, A. Modelli, W. S. Wu, A. Borghesi, and B. Pivac, "Properties of silicon dioxide films prepared by low-pressure chemical vapor deposition from tetraethylorthosilicate,"

Journal of Vacuum Science & Technology B: Microelectronics Processing and Phenomena, vol. 8, no. 6, pp. 1177–1184, Nov. 1990.

[69] M. S. Haque, H. A. Naseem, and W. D. Brown, "Characterization of High Rate Deposited PECVD Silicon Dioxide Films for MCM Applications," *J. Electrochem. Soc.*, vol. 142, no. 11, pp. 3864–3869, Nov. 1995.

[70] S. K. Ray, C. K. Maiti, S. K. Lahiri, and N. B. Chakrabarti, "TEOS-based PECVD of silicon dioxide for VLSI applications," *Advanced Materials for Optics and Electronics*, vol. 6, no. 2, pp. 73–82, Mar. 1996.

[71] W. J. Patrick, G. C. Schwartz, J. D. Chapple-Sokol, R. Carruthers, and K. Olsen, "Plasma-Enhanced Chemical Vapor Deposition of Silicon Dioxide Films Using Tetraethoxysilane and Oxygen: Characterization and Properties of Films," *J. Electrochem. Soc.*, vol. 139, no. 9, pp. 2604–2613, Sep. 1992.

[72] S. Suyama, A. Okamoto, and T. Serikawa, "The Effects of Oxygen-Argon Mixing on Properties of Sputtered Silicon Dioxide Films," *J. Electrochem. Soc.*, vol. 134, no. 9, pp. 2260–2264, Sep. 1987.

[73] H. Klauk, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, "Pentacene organic thin-film transistors for circuit and display applications," *IEEE Transactions on Electron Devices*, vol. 46, no. 6, pp. 1258–1263, Jun. 1999.

[74] P. I. Suciu and R. L. Johnston, "Experimental derivation of the source and drain resistance of MOS transistors," *IEEE Transactions on Electron Devices*, vol. 27, no. 9, pp. 1846–1848, Sep. 1980.

[75] K. Kandoussi, C. Simon, N. Coulon, K. Belarbi, and T. Mohammed-Brahim, "Nanocrystalline silicon TFT process using silane diluted in argon–hydrogen mixtures," *Journal of Non-Crystalline Solids*, vol. 354, no. 19, pp. 2513–2518, May 2008.

[76] H. Gleskova, S. Wagner, and Z. Suo, "a-Si:H TFTs Made on Polyimide Foil by PE-CVD at 150˚C," *MRS Online Proceedings Library Archive*, vol. 508, Jan. 1998.

[77] A. Sazonov, D. Striakhilev, C.-H. Lee, and A. Nathan, "Low-Temperature Materials and Thin Film Transistors for Flexible Electronics," *Proceedings of the IEEE*, vol. 93, no. 8, pp. 1420–1428, Aug. 2005.

[78] S.-J. Kim, S.-M. Han, and M.-K. Han, "Nanocrystalline Silicon Thin-Film Transistor Fabricated without Substrate Heating for Flexible Display," *Jpn. J. Appl. Phys.*, vol. 48, no. 8R, p. 081202, Aug. 2009.

[79] T. Suzuki, Y. Osaka, and M. Hirose, "Theoretical Interpretations of the Gap State Density Determined from the Field Effect and Capacitance-Voltage Characteristics of Amorphous Semiconductors," *Jpn. J. Appl. Phys.*, vol. 21, no. 3A, p. L159, Mar. 1982.

[80] G. Fortunato, D. B. Meakin, P. Migliorato, and P. G. L. Combers, "Field-effect analysis for the determination of gap-state density and Fermi-level temperature dependence in polycrystalline silicon," *Philosophical Magazine B*, vol. 57, no. 5, pp. 573–586, May 1988.

[81] G. Fortunato and P. Migliorato, "Determination of gap state density in polycrystalline silicon by field-effect conductance," *Appl. Phys. Lett.*, vol. 49, no. 16, pp. 1025–1027, Oct. 1986.

[82] L. Pichon, K. Yang, and A.-C. Salaün, "Experimental validation of the surface state distribution model in the Suzuki theory to qualify the thin film surface materials," *Solid-State Electronics*, vol. 154, pp. 12–15, Apr. 2019.

[83] V. Schmidt, J. V. Wittemann, S. Senz, and U. Gösele, "Silicon Nanowires: A Review on Aspects of their Growth and their Electrical Properties," *Advanced Materials*, vol. 21, no. 25–26, pp. 2681–2702, 2009.

[84] R. S. Wagner and W. C. Ellis, "Vapor-liquid-solid mechanism of single crystal growth," *Appl. Phys. Lett.*, vol. APLCLASS2019, no. 1, pp. 89–90, Dec. 2004.

[85] S. Hofmann, C. Ducati, R. J. Neill, S. Piscanec, J. Geng, R. E. Dunin-Borkowski, J. Robertson and A. C. Ferrari, "Gold catalyzed growth of silicon nanowires by plasma enhanced chemical vapor deposition," *Journal of Applied Physics*, vol. 94, no. 9, pp. 6005–6012, Oct. 2003.

[86] N. Sakulchaicharoen and D. E. Resasco, "Temperature dependence of the quality of silicon nanowires produced over a titania-supported gold catalyst," *Chemical Physics Letters*, vol. 377, no. 3, pp. 377–383, Aug. 2003.

[87] V. A. Nebol'sin and A. A. Shchetinin, "Role of Surface Energy in the Vapor–Liquid–Solid Growth of Silicon," *Inorganic Materials*, vol. 39, no. 9, pp. 899–903, Sep. 2003.

[88] V. A. Nebol'sin, A. A. Shchetinin, A. A. Dolgachev, and V. V. Korneeva, "Effect of the Nature of the Metal Solvent on the Vapor-Liquid-Solid Growth Rate of Silicon Whiskers," *Inorg Mater*, vol. 41, no. 12, pp. 1256–1259, Dec. 2005.

[89] Y. Wang, V. Schmidt, S. Senz, and U. Gösele, "Epitaxial growth of silicon nanowires using an aluminium catalyst," *Nature Nanotechnology*, vol. 1, no. 3, p. 186, Dec. 2006.

[90] Z. Li, Y. Chen, X. Li, T. I. Kamins, K. Nauka, and R. S. Williams, "Sequence-Specific Label-Free DNA Sensors Based on Silicon Nanowires," *Nano Lett.*, vol. 4, no. 2, pp. 245–247, Feb. 2004.

[91] H. D. Tong, S. Chen, W. G. van der Wiel, E. T. Carlen, and A. van den Berg, "Novel Top-Down Wafer-Scale Fabrication of Single Crystal Silicon Nanowires," *Nano Lett.*, vol. 9, no. 3, pp. 1015–1022, Mar. 2009.

[92] A. M. Contreras, J. Grunes, X.-M. Yan, J. A. Liddle and G. Somorjai, "Fabrication of platinum nanoparticles and nanowires by electron beam lithography (EBL) and nanoimprint lithography (NIL): comparison of ethylene hydrogenation kinetics," *Catalysis Letters,* vol. 100, no. 3-4, pp. 115-124, Apr. 2005.

[93] S. Chen, J. G. Bomer, W. G. van der Wiel, E. T. Carlen, and A. van den Berg, "Top-Down Fabrication of Sub-30 nm Monocrystalline Silicon Nanowires Using Conventional Microfabrication," *ACS Nano*, vol. 3, no. 11, pp. 3485–3492, Nov. 2009.

[94] M. Lee, Y. Jeon, T. Moon, and S. Kim, "Top-Down Fabrication of Fully CMOS-Compatible Silicon Nanowire Arrays and Their Integration into CMOS Inverters on Plastic," *ACS Nano*, vol. 5, no. 4, pp. 2629–2636, Apr. 2011.

[95] M. De Marchi, D. Sacchetto, J. Zhang, S. Frache, P.-E. Gaillardon, Y. Leblebici and G. De Micheli, "Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity," *IEEE Transactions on Nanotechnology*, vol. 13, no. 6, pp. 1029–1038, Nov. 2014.

[96] H.- Lin, M.- Lee, C.- Su, T.- Huang, C. C. Lee, and Y.- Yang, "A simple and low-cost method to fabricate TFTs with poly-Si nanowire channel," *IEEE Electron Device Letters*, vol. 26, no. 9, pp. 643–645, Sep. 2005.

[97] F. Demami, L. Pichon, R. Rogel, and A. C. Salaün, "Fabrication of polycrystalline silicon nanowires using conventional UV lithography," *IOP Conf. Ser.: Mater. Sci. Eng.*, vol. 6, p. 012014, Nov. 2009.

[98] F. Demami, L. Ni, R. Rogel, A. C. Salaun, and L. Pichon, "Silicon nanowires based resistors as gas sensors," *Sensors and Actuators B: Chemical*, vol. 170, pp. 158–162, Jul. 2012.

[99] B. Le Borgne, A.-C. Salaün, and L. Pichon, "Electrical properties of self-aligned gate-all-around polycrystalline silicon nanowires field-effect transistors," *Microelectronic Engineering*, vol. 150, pp. 32–38, Jan. 2016.

[100] G. Wenga, E. Jacques, A.-C. Salaün, R. Rogel, L. Pichon, and F. Geneste, "Bottom-gate and Step-gate Polysilicon Nanowires Field Effect Transistors for Ultrasensitive Label-free Biosensing Application," *Procedia Engineering*, vol. 47, pp. 414–417, Jan. 2012.

[101] A. Solanki and H. Um, "Chapter Two - Top-Down Etching of Si Nanowires," in *Semiconductors and Semimetals*, vol. 98, S. Mokkapati and C. Jagadish, Eds. Elsevier, 2018, pp. 71–149.

[102] G. Wenga, "Elaboration of chemical and biological silicon nanowires based sensors," Theses, Université de Rennes 1, 2013.

[103] T. Ichiki and T. Yoshida, "Preparation of cubic boron nitride films by low pressure inductively coupled plasma enhanced chemical vapor deposition," *Appl. Phys. Lett.*, vol. 64, no. 7, pp. 851–853, Feb. 1994.

[104] R. Benabderrahmane Zaghouani, M. Yaacoubi Tabassi, K. Khirouni, and W. Dimassi, "Vapor–liquid–solid silicon nanowires growth catalyzed by indium: study of indium oxide effect," *J Mater Sci: Mater Electron*, vol. 30, no. 10, pp. 9758–9766, May 2019.

[105] F. Iacopi, P. M. Vereecken, M. Schaekers, M. Caymax, N. Moelans, B. Blanpain, O. Richard, C. Detavernier and H. Griffiths, "Plasma-enhanced chemical vapour deposition growth of Si nanowires with low melting point metal catalysts: an effective alternative to Au-mediated growth," *Nanotechnology*, vol. 18, no. 50, p. 505307, Nov. 2007.

[106] I. Zardo, S. Conesa-Boj, S. Estradé, L. Yu, F. Peiro, P. Roca I Cabarrocas, J. R. Morante, J. Arbiol and A. Fontcuberta I Morral, "Growth study of indium-catalyzed silicon nanowires by plasma enhanced chemical vapor deposition," *Appl. Phys. A*, vol. 100, no. 1, pp. 287–296, Jul. 2010.

[107] A. Convertino, M. Cuscuna, G. Nicotra, C. Spinella, L. Felisari, G. Fortunato and F. Martelli, "Low-temperature growth of In-assisted silicon nanowires," *Journal of Crystal Growth*, vol. 335, no. 1, pp. 10–16, Nov. 2011.

[108] B. Pierre, "Elaboration de réseaux de nanofils de silicium par procédé VLS basse température (＜ 250 ˚C)," *Private communication*, Jun. 2015.

[109] D. P. Yu, X. J. Xing, Q. L. Hang, H. Yan, J. Xu, Z. H. Xi and S.-Q. Feng, "Controlled growth of oriented amorphous silicon nanowires via a solid–liquid–solid (SLS) mechanism," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 9, no. 2, pp. 305–309, Feb. 2001.

[110] K. W. Kolasinski, "Catalytic growth of nanowires: Vapor–liquid–solid, vapor–solid–solid, solution–liquid–solid and solid–liquid–solid growth," *Current Opinion in Solid State and Materials Science*, vol. 10, no. 3, pp. 182–191, Jun. 2006.

[111] S. H. Yun, J. Z. Wu, A. Dibos, X. Gao, and U. O. Karlsson, "Growth of inclined boron nanowire bundle arrays in an oxide-assisted vapor-liquid-solid process," *Appl. Phys. Lett.*, vol. 87, no. 11, p. 113109, Sep. 2005.

[112] S. K. Chong, B. T. Goh, Z. Aspanut, M. R. Muhamad, C. F. Dee, and S. A. Rahman, "Synthesis of indium-catalyzed Si nanowires by hot-wire chemical vapor deposition," *Materials Letters*, vol. 65, no. 15, pp. 2452–2454, Aug. 2011.

List of communications

Journal publications:

- L. Pichon, **K. Yang**, and A.-C. Salaün, "Experimental validation of the surface state distribution model in the Suzuki theory to qualify the thin film surface materials," *Solid-State Electronics*, vol. 154, pp. 12–15, Apr. 2019. (https://doi.org/10.1016/j.sse.2019.02.002)

- (Accepted) **K. Yang**, O. De Sagazan, L. Pichon, A-C. Salaün and N. Coulon. "Low temperature inductively coupled plasma chemical vapor deposition compatible with silicon flexible electronics applications." *Physica Status Solidi (a)*.

Conferences:

- (oral) **K. Yang**, N. Coulon, A-C. Salaün and L. Pichon, "Croissance 3D de nanofils de silicium par procédé SLS à basse température (250 ˚C)", *Journées Nationales des Nanofils Semiconducteurs (J2N)*, 13-15 November 2019, Lyon (France).

- (poster) **K. Yang**, O. De Sagazan, L. Pichon, A-C. Salaün and N. Coulon, "Investigation of low temperature inductively coupled plasma chemical vapor deposition for flexible electronics", *European Materials Research Society (EMRS) Spring meeting 2019*, 27-31 May 2019, Nice (France).

- (poster) **K. Yang**, A-C. Salaün, N. Coulon, O. De Sagazan and L. Pichon, "Low temperature SiNWs based devices fabrication for flexible electronic applications", *20eme Journées Nationales du Réseau Doctoral en Micro-nanoélectronique (JNRDM)*, 6-8 November 2017, Strasbourg (France).

UNIVERSITE BRETAGNE LOIRE / MATHSTIC

UNIVERSITÉ DE RENNES 1

Titre : Fabrication et caractérisation de nanofils de silicium pour des applications électroniques sur substrats flexibles basse température (≤300 °C)

Mots clés : Nanofils de silicium, basse température, procédé SLS, méthode des espaceurs, ICP-CVD

Résumé : La fabrication et la caractérisation de nanofils de silicium à basse température (≤300 °C) a été menée suivant deux approches: par la méthode des espaceurs et par la méthode de croissance Solide Liquide Solide (SLS). La synthèse des nanofils de silicium a été étudiée à l'aide de deux technologies de dépôts : le dépôt CVD assisté par plasma (PECVD) et le dépôt par plasma à couplage inductif (ICP CVD). Les études ont démontré la faisabilité des nanofils de silicium par le procédé ICP-CVD. De plus, les propriétés d'isolation électrique des couches de SiO2 et la fabrication de transistors à effet de champ à couche mince ont été démontrées à l'aide de la technologie de dépôt plasma ICP.

Par ailleurs, des nanofils de silicium ont été synthétisés par le procédé SLS à 250 °C utilisant l'indium comme catalyseur. La croissance 3D de ces nanofils à partir de substrats de silicium (film mince de silicium monocristallin ou amorphe) a été démontrée. Les nanofils sont obtenus sous plasma d'hydrogène. Des études ont été menées en fonction de l'épaisseur de l'indium déposé, de la durée et de la température du plasma d'hydrogène. Les résultats originaux obtenus permettent d'envisager la possibilité de fabriquer des dispositifs électroniques à base de ces nanofils de silicium sur des substrats flexibles basse température.

Title : Fabrication and characterization of silicon nanowires for device applications compatible with low temperature (≤300 °C) flexible substrates

Keywords : Sillicon nanowires, low temperature, SLS process, spacer method, ICP-CVD,

Abstract : The fabrication and characterization of silicon nanowires (SiNWs) at low temperature (≤300 °C) has been focused for two mainstream approaches: spacer method and Solid Liquid Solid method. The feasibility of such silicon nanowires has been explored using two deposition technologies: conventional plasma enhanced deposition (PECVD), and inductively coupled plasma deposition (ICP CVD). The studies demonstrated the feasibility of silicon nanowires using the ICP CVD process. In addition, the electrical insulation properties of SiO2 layers and the fabrication of thin-film field effect transistors were demonstrated using ICP plasma deposition technology.

Furthermore, indium catalyzed SLS SiNWs were fabricated for the first time at 250 °C. Synthesis of 3D SiNWs by SLS process from silicon substrates (monocrystalline or amorphous silicon thin film) has been demonstrated. The growth of nanowires is obtained under hydrogen plasma. Studies were conducted based on the thickness of indium deposited, duration and temperature of the hydrogen plasma. All these results were concluded originally and they enable the possibility of fabrication of SiNWs based electronic devices onto low temperature flexible substrates.