MEMS inertial sensors design and fabrication based on an innovative process

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THÈSE

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préparée au sein du ***CEA-LETI/DCOS/SCMS/LCMC*****,**
École Doctorale EEATS et Politecnico di Milano

Conception et réalisation de capteurs inertiels basés sur un procédé innovant

MEMS inertial sensors design and fabrication based on an innovative process

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Résumé

La plupart des capteurs inertiels MEMS commerciaux comportent une masse d'épreuve et des moyens de transduction issus d'une même couche de silicium. Il en découle des compromis forts, notamment pour la détection capacitive: une couche épaisse permet d'augmenter la masse et donc de réduire le bruit brownien; inversement, une couche fine permet de réduire la taille des entrefers entre les électrodes, d'obtenir une variation de capacité plus importante, et donc de réduire la contribution du bruit électronique. Plusieurs composants MEMS multicouches ont déjà été réalisés et rapportés dans la littérature, mais aucun n'a cherché à augmenter la densité capacitive tout en réduisant le bruit thermomécanique. Pourtant, la disparition du compromis lié au procédé monocouche permet d'atteindre les hautes performances nécessaires aux applications émergeantes, en conservant la surface d'un capteur grand public. Cette thèse présente des accéléromètres multicouches à détection dans le plan et hors plan. Le procédé de fabrication combine une couche épaisse, dédiée à la réalisation de grandes masses d'épreuve, et une couche fine, permettant d'obtenir de fortes densités capacitives. Ces deux avantages, combinés à une détection par variation de surface, permettent d'obtenir une résolution de l'ordre du $\mu g/\sqrt{Hz}$, une grande gamme dynamique, tout en conservant une taille réduite. Le dimensionnement des capteurs a cherché à maximiser la gamme dynamique et minimiser le bruit en partant d'une taille fixée. D'abord analytique, il a été validé par des simulations par éléments finis. Le procédé de fabrication VLSI a été appliqué à des plaques 200mm. Plusieurs points critiques ont été rencontrés, notamment la surgravure des fonds de tranchée (notching). Combinée à la disparité de vitesse de gravure, elle a entrainé la destruction de beaucoup de capteurs hors plan. Ce problème a été résolu en amincissant pour ces derniers la couche épaisse, entrainant une légère perte de performances. Les capteurs ont été caractérisés sur plaque (capacité statique, fréquence de résonance), puis au niveau puce (sensibilité, niveau de bruit, gamme dynamique). Ces dernières mesures ont nécessité le développement d'une électronique dédiée, à partir de composants discrets. Les accéléromètres dans le plan présentent une capacité statique et une fréquence de résonance très proches de la théorie. Ils atteignent une résolution de $8\mu g/\sqrt{Hz}$ pour une gamme dynamique de l'ordre de 160g. Cette dynamique de 145dB est fournie par un composant de seulement 0.24mm^2; elle est 100 fois plus élevée que la dynamique d'un com-

posant grand public de même taille. De plus, la bande passante est importante et le capteur est lu en boucle ouverte. Les accéléromètres hors-plan présentent une haute fréquence de résonance, au-delà de 8kHz. La masse sismique plus fine, combinée à des ressorts plus larges, explique ce décalage par rapport au dimensionnement initial. Malgré la réduction de sensibilité induite, les capteurs présentent une résolution de 50 à $80\mu g/\sqrt{Hz}$. L'encombrement est faible (jusqu'à 0.22mm^2) et la gamme dynamique a été évaluée à plus de 200g. Dans le futur, des corrections de design et des améliorations dans le procédé de fabrication permettront d'utiliser l'épaisseur initialement prévue, afin d'harmoniser les performances avec celles de l'accéléromètre dans le plan et d'obtenir un accéléromètre 3-axes hautes performances. Ce type de capteurs pourrait jouer un grand rôle dans les applications émergentes en fournissant une bonne stabilité, un faible bruit et une grande gamme dynamique, tout en conservant l'encombrement d'un capteur grand-public. Ce nouveau procédé de fabrication montre donc déjà un gros potentiel à travers les premiers composants réalisés, mais ouvre également de nouvelles possibilités en termes de design. Dans le futur, il pourrait servir de plateforme technologique pour les capteurs inertiels, notamment les gyromètres, mais aussi pour les actionneurs, comme les micro-miroirs.

Abstract

In the vast majority of commercial MEMS inertial sensors, both seismic mass and sensing elements are patterned in the same silicon layer. This sets stringent design trade-offs, in particular for a capacitive sensor: a large silicon thickness increases seismic mass and decreases the Brownian noise floor. A low silicon thickness on the other hand, allows smaller gaps between electrodes, higher capacitance variation and lower electrical noise floor. For this reason, several examples of multi-layer MEMS devices were presented in the past. Yet, increasing capacitance density while reducing mechanical noise floor has not been achieved so far. Breaking the single-layer trade-off could enable new emerging applications that require high-performance sensors within a consumer size. In this work, multi-layer, in-plane and out-of-plane accelerometer are presented. Thanks to the multi-layer process the devices can feature a thick layer for large inertial mass, as well as a thin layer for high capacitive density. These aspects, together with surface-variation detection, allow to obtain $\mu g/\sqrt{Hz}$ resolution and large full-scale while keeping compact size. The sensors are designed through analytical modeling and finite elements method simulations in order to reach the highest dynamic range with the lowest noise at given footprint. Few critical aspects were encountered during the fabrication of the sensors, especially for out-of-plane accelerometers. The notching of the thick-layer etching coupled to the strong lag effect caused most of the z-axis sensors to fail. This forced a reduction of the process thickness and relative loss of performance for this type of sensors. The characterization of the sensors is performed both at wafer-level (static capacitance, resonance frequency) and at die level (scale factor, noise-floor, full-scale). The die-level measurements are carried out with a dedicated electronic circuit implemented with discrete components, developed during this work. In-plane accelerometers showed static capacitance and resonance frequency in line with theory. They achieved resolution smaller than 8 $\mu g/\sqrt{Hz}$ and full scale in the order of 160g. These aspects together lead to a dynamic range of more than 145dB (BW=1Hz) for a device with a footprint of only 0.24 mm^2. This it more than 100 times larger than the DR of consumer device of similar size. These results are achieved while keeping a large bandwidth and working with an open-loop readout. Out-of-plane sensors showed resonance frequency higher than expected due to fabrication tolerances. The devices had both smaller mass and thicker

springs explaining the observed mechanical behavior. Despite the loss of scale factor due to the larger resonance frequency, these sensors achieved resolution ranging from 50-80 $\mu g/\sqrt{Hz}$. Again, such performance was obtained while keeping large resonance frequency (>8 kHz), small footprint (down to 0.22 mm^2) and a potential full-scale of more than 200g. In the future, design corrections and process improvement could lead to device with thicker inertial layer, aligning the performance of out-of-plane sensors to those of in-plane ones and leading to a high-performance 3-axis accelerometer. This type of sensor could address the demand of emerging applications for high-stability, low-noise and large DR accelerometers within consumer footprint. Finally, the proposed technology offers a fabrication platform for inertial MEMS sensors and actuators. New design possibilities and great potentialities have been demonstrated with the first fabricated accelerometers. In the future this new concept could be applied to several other types of MEMS, like gyroscope or micro-mirrors.

Chapter 1

Introduction

1.1 MEMS accelerometers

1.1.1 From the origin of the accelerometer

The first electrical device used to measure acceleration is credited to B. McCollum and O. S. Peters [1], and it was developed in the early 1920s at the Bureau of Standards in the US. The sensor was composed by two stacks of carbon rings set in a Wheatstone half-bridge configuration: when a strain was applied to the central point of the bridge the compression and extension of the rings would generate a resistive change due to the piezoresistive properties of the stacks therefore leading to a voltage variation at the bridge output. The first accelerometer weighted about half a kilogram and it was used to measure acceleration from different sources ranging from common passengers elevator to aircraft catapults used on military ships. A schematic of the device and a photograph of two stacks used in strain detection system are shown in Figure 1.1.

In 1938, the bulky carbon rings were replaced by thin strain gauges triggering a drop of volume and price of this type of sensor and allowing large diffusion of the accelerometers in several new fields. Nevertheless this technology proved limited in both achievable resolution and frequency range. It was subsequently replaced by the piezoelectric principle which showed higher scale factor and better shock resistance. These new accelerometers experienced a technological improvement during the following decades and are nowadays still used as macroscopic scale sensors [2]. Yet, the era of piezoresistive accelerometers was not over: in 1979 L. M. Roylance and J.B. Angels produced a batch of devices composed by a suspended silicon mass held by a cantilever beam with piezoresistive properties [3]. Under acceleration the mass displaced with respect to the fixed frame generating a stress on the cantilever and therefore allowing transduction of the acceleration signal: it was the first micro-machined accelerometer. After the introduction of the basic principle of inertial sensors, *i.e.* a suspended proof mass free to move with respect to a fixed frame, several methods were used in order to

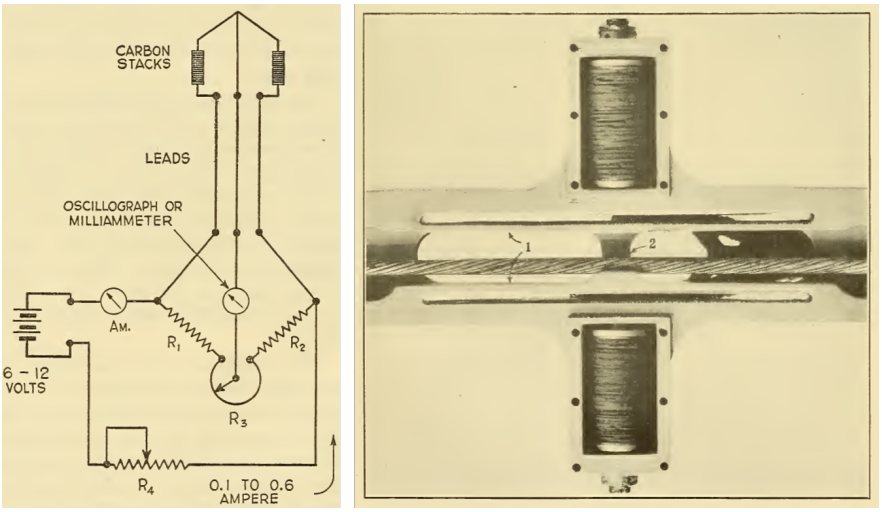


Figure 1.1: *(left) Schematic of the first accelerometer readout configuration; (right) picture of the two carbon stacks used to detect strains on a cable[1]*

detect the moving element displacement: capacitive detection between fixed and moving plates, shift of resonance frequency of a stressed cantilever, piezoelectric generation, heated gas displacement or more complex methods as tunneling current variation and light transmission. The large commercial diffusion of MEMS began only ten years later with the introduction of accelerometers in airbags for automotive applications [4]. From that moment the inertial MEMS market has kept growing, continuously reaching new applications and encouraging the development of more powerful and compact sensors.

1.1.2 Markets and Application

In 2016 the total revenues from the inertial MEMS market were estimated in the order of 3.5 billion dollars [5]. According to Yole Development, the inertial MEMS production is expected to keep growing in the following years mainly driven by an increasing demand for inertial measurement units *i.e.* combination of 3-axis gyroscope and accelerometer on the same chip. The automotive market makes extensive use of accelerometers and gyroscopes since the birth of this technology. Yet, following the introduction of inertial sensors in smart phones and gaming stations, the consumer market has taken an important share of the total revenues. Moreover a growth of this share is expected in the following years with the emerging of new consumer applications such as augmented reality and Internet of Things. Figure 1.2 shows the forthcoming trend of the MEMS industry and the distribution of the market for each application.
The main players in the MEMS industry are both big groups of the electronic business (STM, Bosch, Analog Devices) as well as young companies such as mCube and Invensense founded respectively in 2009 and 2003. The latter has soon be-

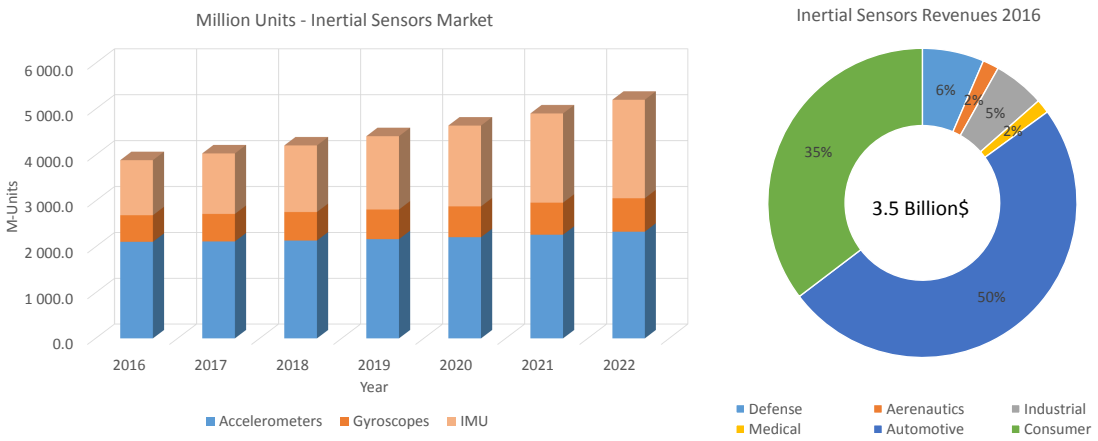


Figure 1.2: *2017 Yole development report showing upcoming trend in inertial sensors market and application distribution [5]*

come a leader in the MEMS field, providing sensors for large consumer products such as Nintendo Wii and iPhone 6. The main break-through of their technology, came from the direct bonding of MEMS sensor and their Application Specific Integrated Circuit (ASIC). Recently, it has been acquired by the TDK group which has entered the MEMS market following the previous examples of other Japanese companies such as Panasonic, RoHm and Murata.
MEMS economy keeps growing thanks to the increasing number of electronic devices but also thanks to new applications. Here reported are some of the existing and future applications of these sensors:

- **Consumer**: electronic stability control for drones, cameras etc., smart phones tilt sensor, gaming stations, step counter, drop protection, virtual/augmented/mixed reality
- **Medicine**: motion study and rehabilitation, robotic exoskeleton for handicapped people, ballistocardiology
- **Automotive**: Airbag, dead reckoning, rollover, anti-theft, electronic stability control, seatbelt activation
- **Military and Aerospace**: rocket launch, intelligent guidance system
- **Others**: earthquake monitoring, gravimetry, oil&gas drilling, movement detection for safety applications, structural monitoring

1.1.3 Different types of MEMS accelerometers

As mentioned at the beginning of the chapter, after the development of the first inertial MEMS a multiplicity of detection method were introduced in order to

detect the displacement of the proof mass. Here, some of the most diffused and effective detection method are reported, highlighting for each technology the main advantages and drawbacks.

Piezoresistive accelerometer

As seen before, the displacement induced by the acceleration can be detected by resistive change of one or more piezoresistive elements stressed by the suspended proof mass [6, 7]. The resistive elements are usually set in Wheatstone bridge configuration in order to compensate for thermal drift or other common mode perturbations. The piezoresistive properties of the stressed gauges depend on both the doping and the geometry of the deformed structures. This readout technique allows compact detection area thanks to the reduced size of the sensing elements. On the other hand the piezoresistive detection suffers from the Johnson noise and the 1/f noise of the resistor which limit the achievable resolution of this technology, especially at low frequency. MEMS piezoresistive accelerometers are present on the market and are mostly used for high-g applications [8, 9].

Piezoelectric accelerometer

Piezoelectric accelerometers are similar to piezoresistive ones: a suspended proof mass is used to generate stress on deformable structures like beams or membranes. This time, the stress generates charges on the electrodes of a piezoelectric material deposited on the stressed elements [10, 11]. This technology offers low power consumption, thanks to the intrinsic charge generation and is best suited for ac detection and transient analysis of acceleration [10]. Indeed the charge losses due the dielectric layer limit the use of these devices for low frequency signals. Furthermore the use of piezoelectric materials is less common than standard semiconductors, increasing the complexity of the fabrication process and limiting the use of this technology for consumer applications. Piezoelectric accelerometers available on the market are mostly macroscopic sensors [8, 9]. As piezoresistive sensors, they are used for the detection of high-g and high-frequency accelerations.

Thermal accelerometer

Thermal accelerometers take advantage of the inertial principle of a moving mass free to move with respect to a fixed frame, however this time the mass is not solid silicon but a gas volume confined in a cavity: the gas is heated by thermal dissipation of resistive structures while its displacement is detected by temperature detector which measured the thermal gradient generated by the acceleration [12, 13]. This readout method allows high shock resistance thanks to the absence of a moving solid structure, on the other hand the slow dynamic response of the gaseous mass sets an important limit to the signal bandwidth. Furthermore, the need of heaters in the sensor leads to considerable power consumption, not in line

with most consumer requirements. This type of accelerometer is currently found on the market, mainly produced by MEMSIC company [14].

Resonant accelerometer

Resonant accelerometers are composed by oscillating structures, beams or moving mass, kept in oscillation by electrostatic or piezoelectric actuation. The displacement of the moving mass generates either a stress on the vibrating structures or a variation of the gap with respect to the fixed electrodes leading to change in the electrostatic stiffness: in both cases the acceleration induces a change of the resonator stiffness leading to a shift in resonance frequency [15, 16, 17]. The design of low power oscillators and accurate frequency to digital converters have brought large improvement to this type of detection making it a valuable alternative to existing commercial devices. Only few high-end products take advantage of this technology, while no consumer device is currently available on the market. Besides the larger complexity, this device suffers from external vibrations: an acceleration signal at the device resonance frequency can induce an excessive displacement (Q>>1) causing malfunctioning.

Capacitive accelerometer

The vast majority of MEMS accelerometers found on the market uses capacitive detection: a moving electrode directly connected to the mass is set parallel to a fixed electrode in order to form a capacitive coupling, the displacement of the moving plate generates a capacitive variation which can be detected by an electronic readout circuit. Such variation can be related to a change of overlapping area between the fixed and moving plates or to change of the capacitive gap. The success of this type of architecture is related to several advantages: it does not suffer from 1/f noise as piezoresistive/piezoelectric devices, it can be implemented using a relatively simple process with no need of piezoelectric materials, it has good temperature stability and it only requires a capacitive to voltage circuit operating in open loop mode with no need for oscillators or closed loop architectures as in the case of resonant accelerometers.
As mentioned in the beginning of the chapter, several other types of accelerometers exist *e.g.* optomechanical [18, 19], tunneling-effect [20], electrostatically levitated [21]. Most of these techniques are still under development and not commercially available, for this reason they are not discussed here. Instead, as this work focuses on MEMS capacitive accelerometers, a more detailed description of this type of sensors is given in the next section, analyzing state of the art performance and current limitations of this type of architecture.

1.1.4 Parameters and performance of MEMS capacitive accelerometers

The range of applications for accelerometers is endless and so is the range of performance delivered by this type of sensor. As an example, the interest in measuring gravity has brought several physicists to develop an extremely resolved accelerometer based on free-fall platinum mass orbiting around the earth with the aim of detecting gravitational wave [22]: the resolution of the sensor was more than 10 orders of magnitude better than the accelerometer found in a smart phones. On the other hand there are devices able to detect ultra-high accelerations like those generated by a bullet or an explosion: these devices can reach a Full Scale Range (FSR) of more than 60.000 gravitational units (g) [2]. MEMS capacitive accelerometers have gained interest thanks to their small size and low cost, nevertheless during the last twenty years, the performance delivered by these sensors has improved to the point of becoming a valuable alternative to macroscopic detectors for many inertial applications. Typical performance figures are reported in Table 1.1 for the following four families of MEMS capacitive accelerometers: i) high-resolution devices [23, 24], usually used for seismology or gravimeter ii) Consumer devices [25, 26, 27], low cost sensors found in most consumer objects iii) high-g family [28, 9, 29], devices used for shock detection applications iv) and high-stability sensors [30, 31] used for instance in structural monitoring or navigation systems. These sensors require good resolution in order to detect small vibrations, at the same time they also need high offset stability to offer reliable measurement over a large span of time. Here, the main parameters reported in the table are described:

- **Bandwidth**: it is the frequency at which the output signal differs by 3dB with respect to the in band signal. It is related to both the resonance frequency of the devices and the ASIC used for the readout. High-resolution devices usually have low resonance frequency in order to reach high displacement to acceleration scale factor and therefore have a smaller bandwidth. On the contrary high-g devices are stiff structures able to withstand large accelerations and therefore present large resonance frequencies. Consumer devices usually have an electronically selectable bandwidth: a large bandwidth requires high output data rate increasing the power consumption of the system.

- **Stiffness**: it is the ratio of the applied force to the device displacement in quasi-stationary condition. Together with the mass of the device it sets the resonance frequency of the structure and therefore its mechanical scale factor. For gap variation devices it is the difference between the mechanical stiffness and the electrostatic one as later described in subsection 2.2.2. High stiffness values are important to avoid adhesion of the moving mass to the stopper after a mechanical shock.

- **Noise density**: it is the noise spectral density expressed in terms of acceleration. The noise has both a mechanical origin (Brownian Noise (BN) or thermo-mechanical noise) and an electronic one (noise related to the readout circuit): the first term is related to the mechanical structure and the operating pressure of the sensor; the second term is proportional to the intrinsic noise of the ASIC and the scale factor of the device as later explained in 2.2.4. High resolution devices can reach noise floor in the order of few $ng/\sqrt{Hz}$ thanks to the large area consumption or the closed-loop readout. The latter allows the operation of the device in vacuum condition strongly reducing the damping mechanism. On the other hand, noise performance of consumer devices are in the order of 50 to 200 $\mu g/\sqrt{Hz}$: in this case the resolution is usually limited by the small size of the device and the low power consumption of the circuit.

- **Full Scale Range (FSR)**: it is the maximum acceleration signal that can be detected with a linearity error smaller than the limit set by the application. The maximum detectable signal is directly related to the maximum displacement and the readout technique. Devices with high mechanical scale factor like seismometer usually have a small FSR. Conversely high-g devices can reach FSR of several thousand g paying the price of a poor scale factor *i.e.* electronic noise limited resolution.

- **Nonlinearity (NL)**: Error with respect to the linear fit of the data evaluated as a % of the FSR. The maximum linear error allowed by most applications is set at 1% of the FSR.

- **Zero-g offset**: Residual offset of the sensors after trimming of the value through a calibration procedure. It can vary over the lifetime of the sensor as a consequence of stress and aging of components.

- **Temperature offset drift**: it is the variation of the residual offset with respect to temperature. This term is important for all the applications that require stability of the sensors in harsh environment or over a large temperature range. The causes of the drift are related to both the mechanical structure and the readout circuit.

- **Footprint**: it is the typical area occupied by a single axis device without package or ASIC. It can vary from a few square millimeters as in the case of seismometer down to fractions of square millimeters for most compact consumer sensors.

All the trade-offs mentioned so far are visible in Table 1.1. Increasing the bandwidth, the full scale, the stiffness or reducing the size of the device leads to a decrease in the achievable resolution. Overall, larger devices offer larger dynamic range. Less evident in the table, it also exists a trade-off between the offset

Parameter	Unit	High-res.	Consumer	High-g	High-stability
Bandwidth (BW)	$[kHz]$	<0.2	0.4-2	>10	0.01-1.15
Stiffness	$[N/m]$	≤ 1	1-10	>10	-
Noise density	$[\mu g/\sqrt{Hz}]$	<0.01	50-200	>1000	<10
FSR	$[g]$	$\leq$1	2-16	100-60000	$\leq$2
DR (BW=1Hz)	$[dB]$	120-150	80-90	80-90	110-120
Nonlinearity	$[\%FSR]$	0.1	1	0.1-2	<0.1
Zero-g offset	$[\%FSR]$	-	<1	<1	<1
T-offset drift	$[ppmFSR/K]$	-	<100	<100	<30
Footprint	$[mmxmm]$	5-100	0.01-0.5	-	>1

Table 1.1: *Typical performance and parameters of four families of MEMS devices: high-resolution sensors, consumer sensors, high-g sensors and high-stability sensors.*

stability and the scale factor of the device ([32]), again the size of the device plays a role. All these trade-offs set a limit to those applications that require compact size, high-stability, high-resolution and large FSR, as for instance emerging applications like mixed reality or inertial navigation. At the same time, high-end sensors require large die-size and high cost production. In the next section, in order to understand the reason behind these constraints and the possible solutions, a study of the working principle of MEMS capacitive accelerometers is addressed.

1.1.5 The single layer trade-off

Figure 1.3 shows the basic scheme of a capacitive in-plane accelerometer: a structure made of a proof mass with externally attached moving electrodes is suspended by springs and free to move in one direction with respect to the substrate. An external acceleration induces a relative movement of the suspended

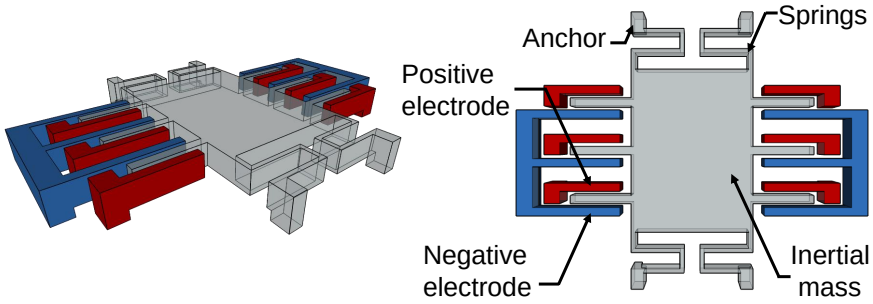


Figure 1.3: *Schematic view of a standard in-plane capacitive accelerometer. A moving mass is suspended by springs while detection is obtained by differential capacitive variation with respect to fixed electrodes. The electrical contacts are fabricated in a poly-silicon layer deposited on the substrate. This layer is used only for electrical connection and has no mechanical use.*

structure with respect to the fixed electrodes (blue, red) producing a differential capacitive variation. As later explained in subsection 2.2.2, the scale factor of this type of device expressed in capacitive variation per gravity unit (g) is summarized in equation 1.1:

$$S = 2\frac{x_{n_M} C_0}{FSR} \quad \left[\frac{F}{g}\right] \tag{1.1}$$

where C_0 is the static capacitance of a single electrode, x_{n_M} is the maximum allowable normalized displacement of the device and FSR is the Full Scale expressed in gravity units. As mentioned before, maximizing the scale factor allows to reduce the impact of electronic noise on the device resolution. As the FSR is defined by the application and x_{n_M} is usually a fixed value, it is clear that in order to maximize the scale factor of the device it is necessary to increase its static capacitance.
The capacitive couplings between the moving mass and the fixed electrodes can be written as follows:

$$C_0 = N_m \epsilon_0 A_R L_c \tag{1.2}$$

where N_m is the number of moving plates, A_R is the aspect ratio between the height and the gap of the capacitor and L_c is the length of the parallel plate. Indeed, the first way to improve the static capacitance is to increase the aspect ratio of the etching process. Several groups have followed this path [33, 34, 35] however this procedure often requires additional refilling steps after the etching of the electrodes. Alternatively it is possible to increase the length of the single capacitor or the number of detection units N_c. The first solution requires a larger area consumption (higher cost) or smaller inertial mass, as a result the mechanical performances of the device are worsen. The second option instead could be achieved by reducing the thickness of the MEMS layer and obtaining therefore smaller Critical Dimension (CD) for the electrodes. Unfortunately also this solution would lead to structures with both low mechanical stiffness (also in the out-of-plane direction) and large Brownian Noise due to mass reduction.
Therefore a trade-off exists between the increase of capacitive density and the mechanical properties of the device such as stiffness and intrinsic noise floor. Such trade-off is the main actor of the trends observed in Table 1.1 and mentioned before. Reducing the size, means sacrificing either mechanical performance or electrical one. For this reason, high-end accelerometers rely on large area consumption to maximize the scale factor and minimize the Brownian noise of the sensor. In the past years, several solutions have been proposed in order to overcome such trade-offs and are presented here.
The solution proposed by Yamane et al. consists in fabricating inertial elements using higher density materials typical of MEMS fabrication such as gold [36]. Yet

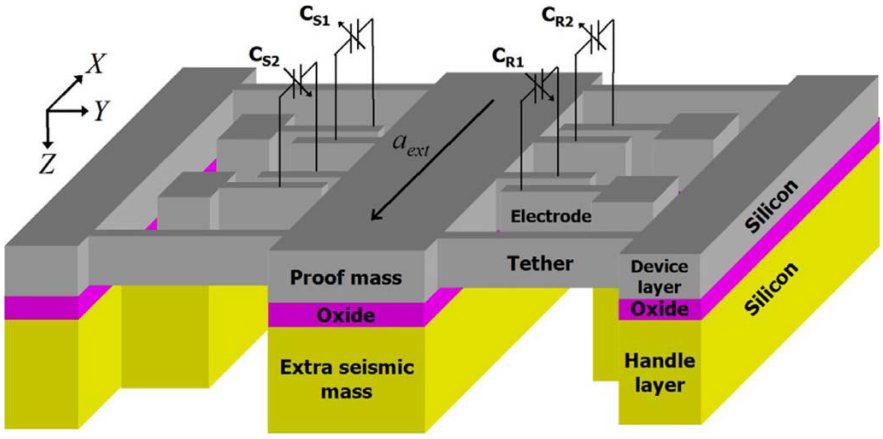


Figure 1.4: *Schematic view of a double layer accelerometer proposed by Amini et al. [35].*

the temperature dependency of gold mechanical properties remains an important constraint together with the price of this material.

Another possible solution was proposed by Ayazi et al. [35], followed by several other groups [37][38]: rather than working with a single mechanical layer the authors proposed to leave the holder substrate attached to the proof mass. This approach allowed to increase the total mass of the device without sacrificing the capacitive density as shown in Figure 1.4. Coupled to high-aspect ratio etching process, this solution allowed low intrinsic Brownian noise and high scale factor. Despite the considerable performance improvement, this device still suffered from large footprint (7x7 mm^2) and relatively large electrode gap. The main drawback of this technology is due to the oxide areas connecting the two MEMS layers: (i) in order to resist the release step and to guarantee mechanical connection large oxide areas are needed, therefore constraining the capacitive density of the device layer and blocking technological scaling (ii) the SiO_2 prevents electrical connection between the MEMS layers limiting the design possibilities.

In the following years, several groups have tried to move towards multi-layer devices. First Geisberger et al., from Freescale, proposed suspended fixed electrodes in order to reduce the connection point and allow new design possibilities [39]. The first etching of the device layer was refilled by an oxide deposition, allowing to deposit another layer of poly-silicon to produce suspended electrodes and vertical travel stops as shown in Figure 1.5. This new process allowed electrical interconnections between the layers reducing the number of anchor points, however all moving elements were still obtained in a single layer, still limiting the performance improvements.

More recently, Classen et al. from Bosch have presented a 3D process inspired by the work of Geisberger [40]. The new process takes advantage of trench refilling proposed in the Freescale fabrication, integrating it with the standard Bosch pro-

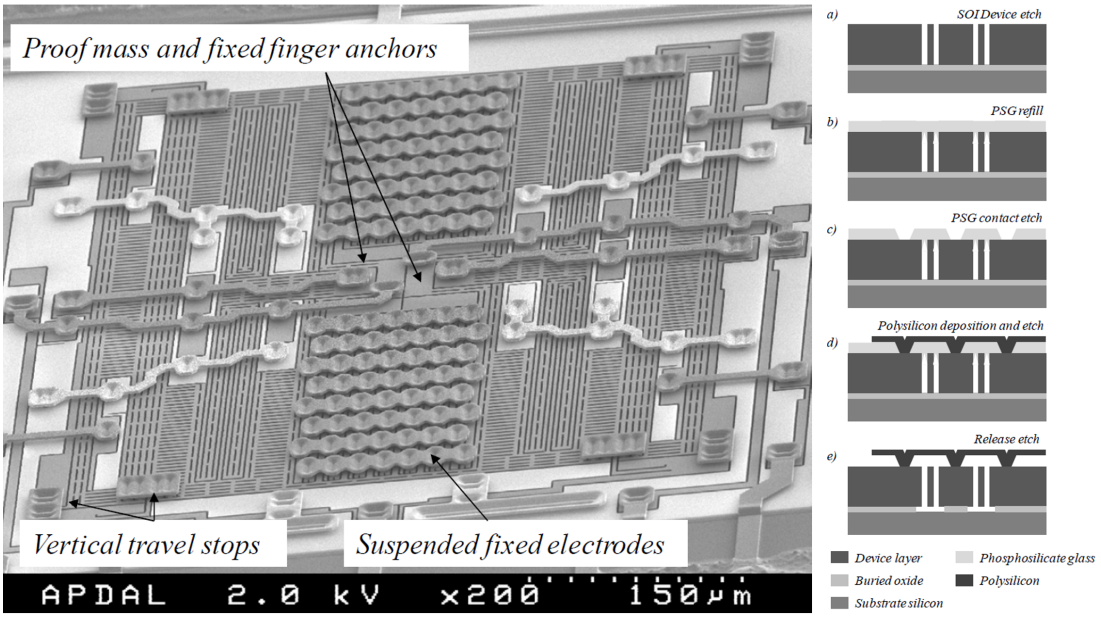


Figure 1.5: *(left) Image taken with a Scanning Electron Microscope (SEM) of the 3D process proposed by Geisberger et al. in 2013 having suspended fixed electrodes and interconnections; (right) schematic view of the process, first etched trenches are refilled with oxide in order to deposit further poly-silicon layers. [39].*

cess for inertial sensors. This time not only the electrodes are fabricated in the additional layer, but also part of the moving structure; as shown in the schematic view of the z-axis accelerometer in Figure 1.6. This new process allows stress isolation (offset-stability) and reduced area consumption, by reducing the number of anchor points, together with new design possibilities. It is the case of the z-axis devices which featured also top electrodes, instead of only bottom electrodes as in standard technologies. Such results are achieved at the cost of an increased process complexity, while improvement in the capacitive density and the inertial properties of the sensors are still limited, also likely due to industrial constraints. As a matter of fact the thickness of the inertial layer and the critical dimension of the electrodes remain the same as those of the standard Bosch process, therefore leaving most of the single layers trade-offs unchanged.

1.1.6 A new process for multi-layer inertial sensors

The present work develops and characterizes a novel fabrication process for multi-layer inertial sensors aiming at overcoming the existing trade-offs of the single layer fabrication. The new concept offers at the same time improved mechanical and electrical performance together with new design possibilities seen for other 3D-process, for both in-plane and out-of-plane devices. Figure 1.7 shows an ex-

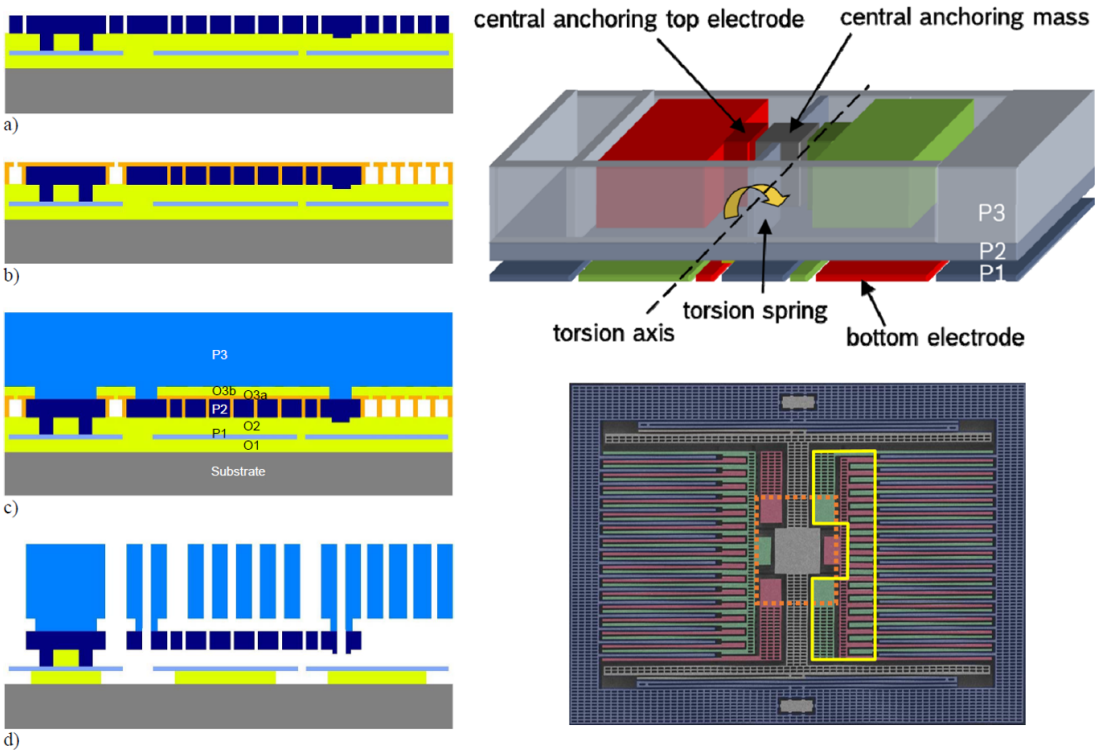


Figure 1.6: *(left) Schematic view of the 3D process from Bosch. The etching of P2 is refilled with two oxide layers in order to deposit P3; (top-right) z-axis accelerometers presenting differential electrodes thanks to the 3D technology; (bottom-right) in-plane accelerometer with reduced anchor points for stress isolation. All anchor points are placed within the area delimited by the dashed orange line [40].*

ample of an accelerometer implemented with the new fabrication concept: the seismic mass and springs are patterned in a thick layer while electrodes are fabricated in a thin layer. Fixed elements and springs are anchored to a substrate below the structure. Figure 1.7.b shows the bottom view of the 3D structure: the overlapping surface between fixed and moving electrodes varies due to the proof mass motion in the x direction. As later explained in Section 2.2.2, surface variation detection is the best suited solution when working with sub-micrometric gaps. As a matter of fact the double layer concept allows electrostatic combs with sub-micrometric-scale gaps along with an increase of the seismic mass thickness with respect to standard processes [41]. It should be noted that the moving elements are directly connected to the mass, with no need for large contact area as in the case of [35]. This aspect, together with the sub-micrometric size of the elements open the way to high capacitive density. Finally, the increased thickness allowed by the two-layer concept offers significant advantages with regard to mechanical performance: i) low intrinsic noise floor ii) large mechanical stiffness

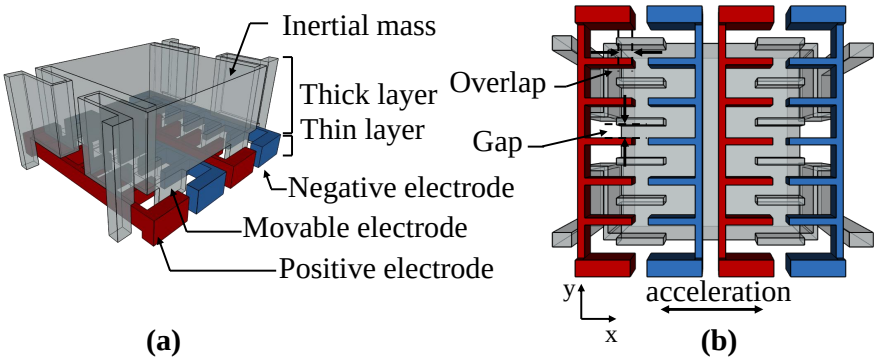


Figure 1.7: *(a) Schematic view of the 2-layer in-plane accelerometer: mass and springs are implemented in the thick layer while electrodes are obtained from the thin one. Fixed elements are anchored to a substrate below the structure; (b) details of the comb sensing region: capacitive detection is implemented by surface variation between the fixed electrodes and the moving ones which are directly connected to the thick layer.*

without increase of resonance frequency, which allows stronger restoring force to avoid adhesion. As later explained in Chapter 2, out-of-plane devices can benefit as well from the novel fabrication process. Among the new design features, the possibility of implementing out-of-plane comb-fingers allows large increase of capacitive density and linear range for the z-axis sensors.
Chapter 2 presents the fabrication and the design of in-plane and out-of-plane accelerometers using this innovative process. Chapter 3 addresses the design of the ultra-low noise electronics readout circuit for device characterization. Finally in Chapter 4 and 5 the results for xy-axis and z-axis devices are respectively presented.

1.2 First chapter conclusion

In this chapter an overview on the existing inertial MEMS technology and its currents limitations have been presented. Capacitive sensing is the main detection method in existing MEMS accelerometers thanks to the low cost, small size and good reliability. The existing MEMS technology mainly relies on a single-layer fabrication, where electrical and mechanical elements are obtained from the same silicon layer. This constraints sets a trade-off between the size and the performance of the device. New emerging applications requiring low noise, small size, high-stability and relatively large full scale, are pushing to overcome such trade-off. Several groups and industrial players have moved to a multi-layer process, yet the performance of the device is often still limited by single-layer constraints. For this reason, this work presents a new multi-layer process that aims to overcome the existing trade-off, offering high-end performance within a reduced footprint, enabling new emerging applications. The main advantages offered by the new fabrication process is the possibility of implementing large inertial mass together with detection units having sub-micrometric gaps. This feature enables improved mechanical properties together with increased capacitive density.

Chapter 2

Fabrication and design

2.1 Fabrication

The fabrication procedure used to implement the novel double-layer concept is presented here. First in-plane device fabrication is addressed, while the process flow of out-of-plane accelerometers is described in the subsequent subsection: all the steps are represented in Figure 2.1 and Figure 2.2 .

2.1.1 In-plane accelerometers process

(a) The process starts with deposition of an oxide layer on a p-doped silicon 200 mm substrate. The oxide layer is deposited by chemical vapor deposition using tetra-ethyl orthosilicate and its density is increased by heating in oven at 1100 °C. The obtained layer is patterned in order to form the connection point between the doped substrate and the subsequent layer. Patterning is followed by deposition of a doped silicon epitaxial layer which generates single-crystal structures when formed directly on the substrate and poly-crystal structures when grown on the oxide. The deposition step is followed by Chemical Mechanical Planarization (CMP) in order to reduce the epitaxial layer to the desired thickness and to obtain a flat surface for the Deep Reactive Ion Etching (DRIE).

(b) The epitaxial layer is patterned by DRIE in order to form comb-fingers, wafer-bonding anchorages and stoppers. The etching process is divided in two steps in order to obtain partially etched structures as explained in 2.1.2. The maximum achievable aspect ratio is limited by both the etching process and the misalignment between process masks as later explained in subsection 2.1.3. The moving electrodes are directly connected to the mass, with no need of oxide layer as in [35], while fixed electrodes remain separated from the substrate by the oxide layer.

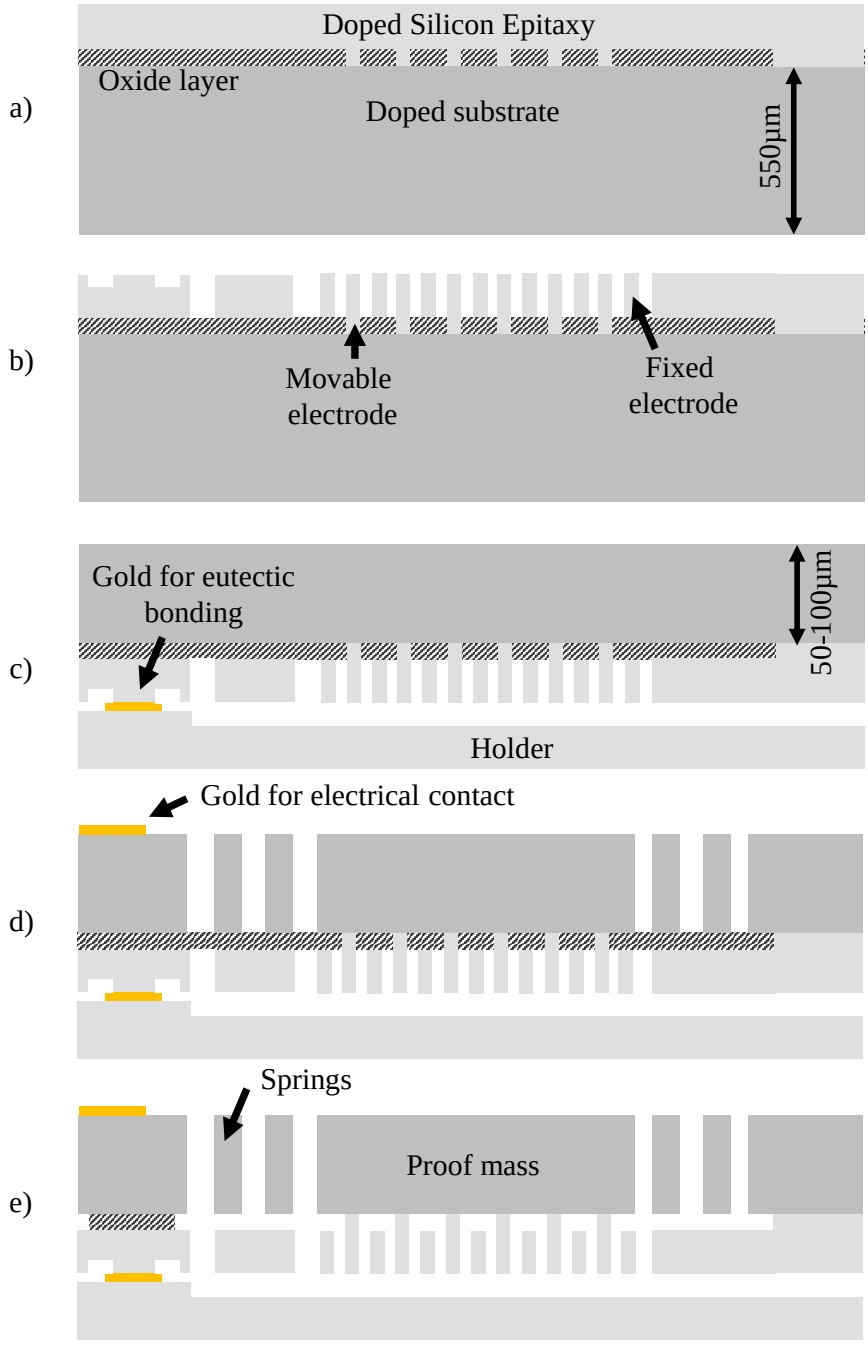


Figure 2.1: *Schematic view of the fabrication process.*

(c) The obtained wafer is flipped and bonded to a second holder wafer, which has a cavity facing the device surface. Eutectic bonding is made by contact points fabricated in the epitaxial layer and gold deposition on the holder substrate, any gold overflow is confined by partially etched trenches around

the contact points. The depth of the cavity can be easily controlled in order to avoid stray capacitance to substrate. After wafer-bonding, the stack of two wafers undergoes grinding and CMP in order to reduce the thickness of the doped substrate down to the desired height (50-100μm) which allows the fabrication of both large proof mass and relatively small CD for the spring etching.

(d) CMP is followed by metal deposition and patterning in order to form the electrical contacts for the devices. As the thick layer is conductive, polarization of the thin layer can be performed from the top of the device. After metal deposition, the wafer stack undergoes a second DRIE etching in order to define all the elements of the thick layer: mass, springs and anchor points. The oxide deposited during initial steps acts as stop layer.

(e) Finally the sacrificial oxide layer is etched with HF vapor for a time-controlled release step.

2.1.2 Out-of-plane accelerometers process

While implementing sub-micrometric comb-fingers for in-plane devices is quite straight-forward, fabricating out-of-plane combs structures requires a few additional process steps (Figure 2.2).

(b1) While, for in-plane devices, the etching step of the thin layer is performed by protecting both fixed and moving electrodes with a hard $Si0_2$ mask, for out-of-plane devices the oxide is partially replaced by a photo-resist layer which covers only the moving electrodes.

(b2) A first time-controlled etch step is performed, during this step both masks are present and protect all the necessary structures while trenches between the electrodes start forming.

(b3) The photo-resist mask is removed before a second DRIE step, this time both the trenches and part of the electrtodes are etched. In this way a partial overlap between electrodes is formed, producing out-of-plane comb-fingers structures.

As mentioned before, the partial etch step is also used to fabricate confinement trenches for gold overflow during wafer bonding, moreover as the springs of out-of-plane devices are fabricated in the thin layer, the partial etch allows the reduction of the springs thickness adding a degree of freedom in the stiffness control. All the other steps of the fabrication of the out-of-plane devices are identical to those of in-plane devices and are therefore not reported.

2.1.3 Critical aspects and limitations

While moving to a 3D fabrication process enables new design possibilities and more compact design, it involves a few technological challenges. Some of the critical aspects of the new process-flow and possible relative improvements are listed here:

1. Anchor points: one of the main limitations in the scaling of this technology is the size of the anchor points. As shown in Figure 2.3 several features has to be taken into account when defining the size of the bonding areas: (i) the width of contact point is the first limitation in reducing the size of the bonding pads. In order to guarantee solid adhesion this term is set equal to 20 μm; (ii) the gold deposited on the holder wafer has to take into account a possible misalignment (MSL) between the two wafers. For this reason its critical dimension is equal to the size of the contact point plus two times MSL. As the trench surrounding the contact points has to confine the gold overflow generated during the bonding process, the minimum trench width is equal to two times the MSL. The misalignement can be as high as 10 μm leading to 20 μm-large trenches; (iii) the width of the trench wall is usually

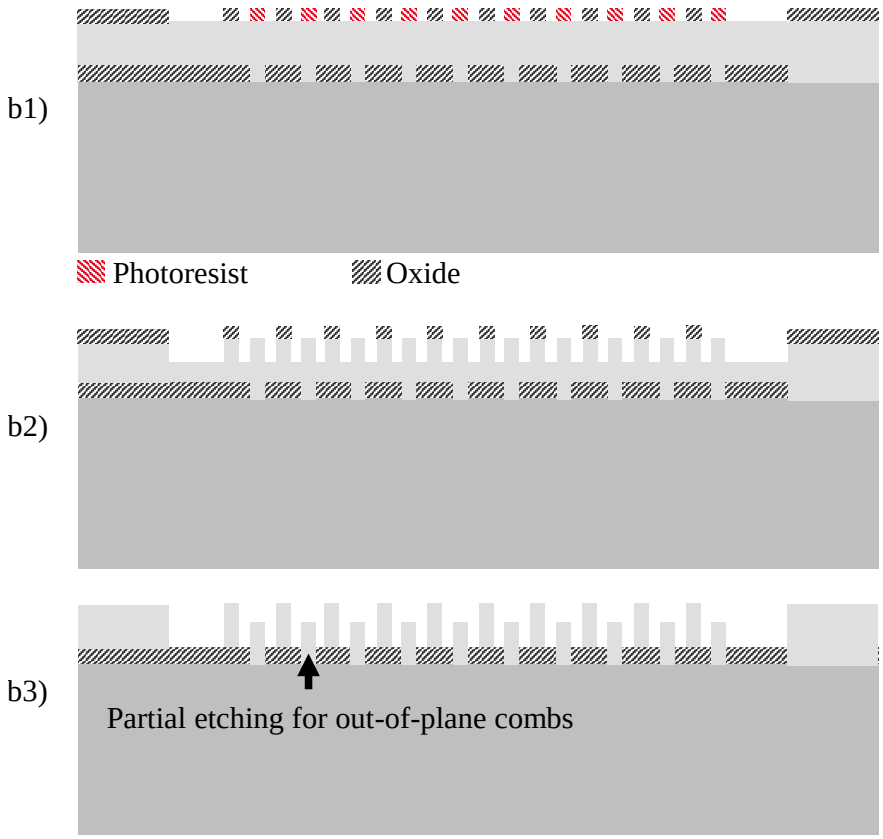


Figure 2.2: *Schematic view of the fabrication process for out-of-plane devices.*

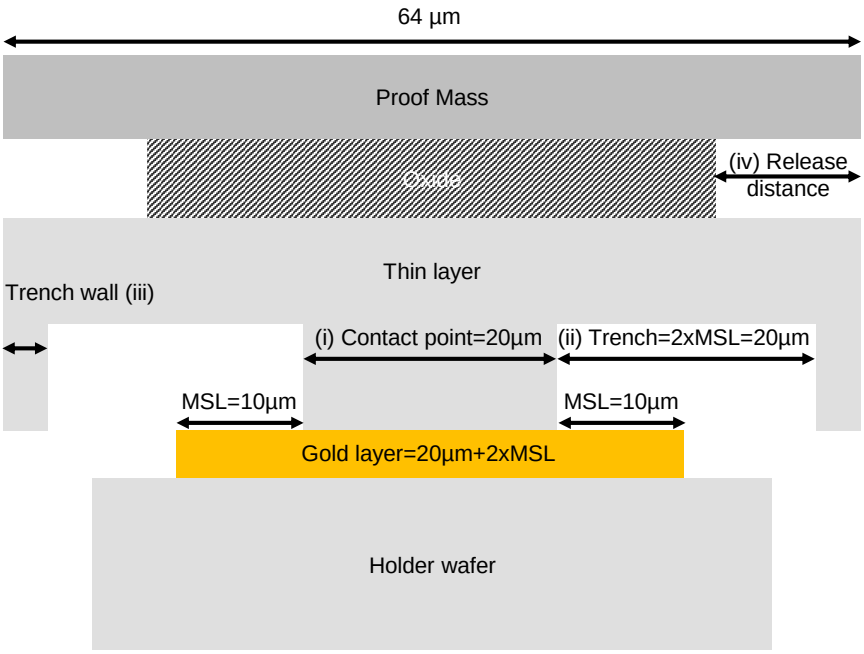


Figure 2.3: *Cross section of an anchor point: the thin layer is partially etched in order to form a trench around the contact point. The potential misalignment between the holder wafer and the device wafer has to take into account, this leads to an increase in the trench size.*

set equal to 2 microns and is therefore less influent on the overall size;(iv) finally, the etching distance used to release the structure from the oxide sets another constraint. The SiO_2 that remains after the release step has to ensure solid bond between the two MEMS layers. With typical release distance in the order to 10 μm this condition is not the limiting one.
Taking into account all contributions, the fabricated devices had minimum anchor points side length of 64 μm. For a device of 400 μm of width, this means a significant reduction of the available area dedicated to sensing units and an intrinsic limit to further scaling. The relatively large bonding points and the strong potential misalignment between the two wafers represents the main limitation to the scaling of the bonding areas. For instance, reducing the misalignment to 1 μm would lead to a anchor points size reduction of 50% ($64^2\mu m^2 \rightarrow 46^2\mu m^2$).

2. Thin layer masks alignment: a misalignment exists also between the mask used to etch the first deposited oxide layer and the one used to pattern the silicon epitaxial layer. Figure 2.4 shows the effect of an alignment error between the two masks. In the case of no alignment error, fixed electrodes are centered on the oxide areas while moving electrodes are placed in between them. As long as the misalignment is smaller than half of the

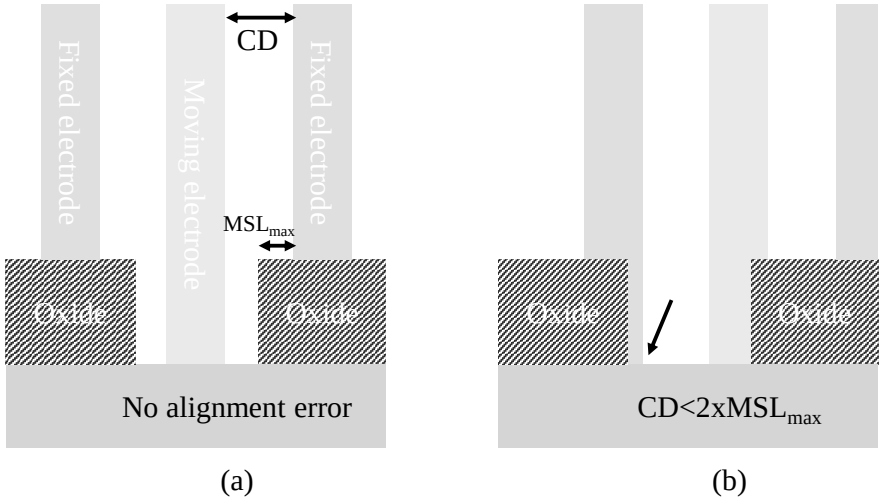


Figure 2.4: *Two different fabrication outcome are presented: (a) Ideal situation where no misalignment is present, electrodes are centered on the oxide (b) The misalignment is larger than CD/2, some of the electrodes are partially connected to the moving layer.*

gap size, the fixed electrode remain confined on the oxide layer. If this condition is not met, the situation presented in 2.4.b can appear. In this case electrodes are formed on both the doped substrate and the oxide layer generating a contact point between the fixed structure and the moving one. For this reason the critical dimensions of the trenches has to take into account such non-ideality and it is therefore limited to twice the maximum misalignment distance (MSL_{max}). In the case of the first fabrication run the maximum error was assumed equal to 250 nm giving a CD of 500 nm, this condition was more stringent than the one set by the aspect ratio of 20 ($7\mu m/20 = 350nm$). Yet, 350nm devices were successfully fabricated, proving that the maximum misalignment was overestimated. In conclusion, the optimum condition for the thickness of the epitaxial layer is reached when the misalignment error equals the DRIE critical dimension.

3. DRIE notching. The etching speed depends on the geometry of the device (lag effect): ions etching is more effective when opening large areas, e.g. the proof mass perimeter, than for small openings, as for instance the release holes. Therefore while the etching of the smaller features is being completed, the ion beam has already reached the silicon oxide below larger openings. As shown in Figure 2.5 once encountered the SiO_2 layer, the ions start spreading perpendicular to the etching directions digging the silicon layer and risking to bypass the protection layer. This phenomenon is called notching. For short etching time this undesired effect is usually limited, however in the case of thick silicon layers long etching time are needed,

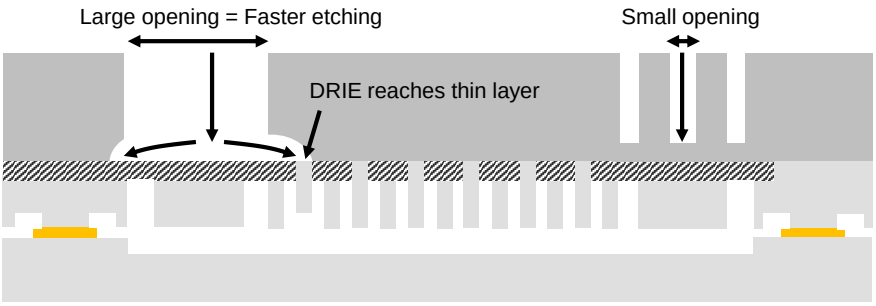


Figure 2.5: *Schematic cross section of the device during etching of the thick layer. While small opening are being opened, the plasma beam has already reached the stop layer and starts to etch the surrounding silicon affecting some of the thin layer structures.*

generating notching of several microns which can easily damage the structures underneath the protective layer. As shown in the result section, this problem was underestimated and caused most of the out-of-plane structures to fail. For this reason it was necessary to fabricate also structure with 50 μm proof mass.

4. 3-axis integration. Producing a single die with both in-plane and out-of-plane accelerometers requires to find good balance between the two design and ensure that each process step fits both accelerometers. For instance, the above mentioned notching problem pushed us to split the fabrication of the two types of sensors. It was possible to obtain working in-plane devices at 50 μm, but their performance were obviously less interesting.

2.2 Design

In this section a detailed description of the accelerometer working principle is given: electro-mechanical aspects and their relation with the sensor performance are addressed. Finally, the design flow of in-plane and out-of-plane accelerometers developed using the innovative fabrication concept is presented.

2.2.1 Working principle of a MEMS accelerometer

As mentioned in Chapter 1, MEMS capacitive accelerometers are made of a moving mass suspended by springs and free to move along one axis. In order to study the response of the system to an external stimulus (a_{ext}), the accelerometer can be represented with an equivalent spring-mass-damper model and its dynamic behavior can be described by Newton's principle:

$$m\,\ddot{x} + b\,\dot{x} + k\,x = -m\,a_{ext} \tag{2.1}$$

where x is the displacement in the acceleration direction, m the mass of the accelerometer, b the damping coefficient and k the elastic stiffness of the structure. Obtaining the solution of the equation in the time domain is not straight forward, for this reason Equation 2.1 is usually rewritten using Laplace transform:

$$m\,s^2\,X(s) + b\,s\,X(s) + k\,X(s) = -m\,a_{ext} \tag{2.2}$$

now, by substituting the Laplace variable s with Fourier's one $j\omega$ to study steady state behavior, the displacement versus acceleration as a function of frequency can be obtained:

$$\frac{X(j\omega)}{a_{ext}} = \frac{1}{\omega^2 - j\omega\,\frac{b}{m} - \frac{k}{m}} = \frac{1}{((\omega^2 - \omega_0^2) - \frac{j\omega\,\omega_0}{Q})}. \tag{2.3}$$

Where w_0 and Q are respectively the resonance frequency of the accelerometer and its quality factor:

$$\omega_0 = \sqrt{\frac{k}{m}} \quad Q = \frac{\sqrt{k\,m}}{b}. \tag{2.4}$$

The relation obtained in Equation 2.3, is represented in Figure 2.6. The first consideration to draw is that, independently of the quality factor of the system, for $\omega << \omega_0$ the accelerometer transfer function is flat and can be written as follows:

$$\left|\frac{X(j\omega)}{a_{ext}}\right| \approx \frac{1}{\omega_0^2}. \tag{2.5}$$

This is the standard working region of MEMS acccelerometers. The first design trade-off appears in Equation (2.5). In order to have a large mechanical sensitivity it is necessary to have low resonance frequency, however a low resonance frequency means a small bandwidth as the $\omega << \omega_0$ condition is satisfied only at lower frequency. Yet, the choice between a large bandwidth and high mechanical sensitivity is not the only aspect to take into account when choosing the resonance frequency of the device. As explained in the following section, the characteristics of the detection system and the required acceleration range have to be considered when designing the device. Lastly, the resonance frequency is directly related to the stiffness of the device which plays an important role in restoring the sensor position after a shock. In order to avoid adhesion problems, particular attention should be paid to this parameter as well.
The second device characteristic which appears in Equation 2.3 is the damping condition of the accelerometer *i.e.* its quality factor.

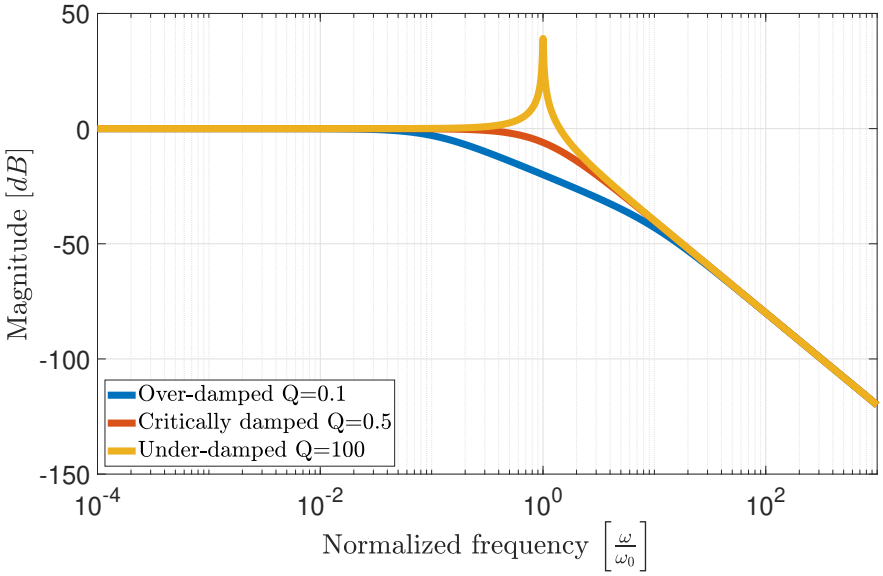


Figure 2.6: *Magnitude of the accelerometer transfer function versus frequency for three different damping conditions. (a) For an under-damped system the transfer function presents a peak at resonance frequency. The device has lower intrinsic noise and larger bandwidth, but it is also more sensitive to undesired vibrations. (b) For critically damped system the transfer function has the -3dB point at ω_0 and two superposed reals poles. (c) For over-damped system the real poles are split, and the device bandwidth is reduced.*

While an under-damped system ($Q > 0.5$) reduces the intrinsic noise of the accelerometer, it also makes the device more sensitive to shocks and vibrations. As a matter of fact, the accelerometer transfer function presents a peak at resonance where the displacement is equal to Q-times the value obtained for $\omega << \omega_0$. This means that a displacement related to an external vibration, in resonance with the device, would be amplified by a factor Q possibly causing the mass to exceed the allowed motion as the case of resonant accelerometer. The speed of recovery of a device after a shock depends on its quality factor: a low damping coefficient increases the dead-time between a received shock and the new useful detection of the accelerometer. For instance, a device with Q=1000 and f_0=3kHz, has a decay time constant (τ) of 9 seconds. For most applications, it is therefore desirable to keep a low quality factor.
In the case of a critically damped system ($Q = 0.5$), the transfer function does not present any peak and the -6dB point is reached at the resonance frequency. This is often considered as the optimum condition for an accelerometer, having therefore large bandwidth and being vibration insensitive. Finally for over-damped system ($Q < 0.5$), the transfer function presents two separates real poles. The -6dB point is reached at a frequency lower than the resonance frequency causing a reduction of the useful bandwidth.

2.2.2 Comparison between surface variation and gap variation for in-plane accelerometers

Figure 2.7 shows the working principle of the two main capacitive detection techniques: (a) gap variation and (b) surface variation. In both architectures the sensing unit is composed of a moving electrode forming at least two capacitive couplings with respect to fixed electrodes of different polarity. In the case of gap variation, following an external acceleration, the central plate moves perpendicularly to the fixed electrodes increasing the gap of C_{01} and decreasing the gap of C_{02} and therefore obtaining a differential capacitive variation. The capacitive change as a function of the displacement x can be written as follows:

$$\begin{aligned}\Delta C = C_{01} - C_{02} = \epsilon_0 hOL\left(\frac{1}{g-x} - \frac{1}{g+x}\right) = 2\frac{C_0}{g}\frac{x}{1-\frac{x^2}{g^2}} \\ = 2\frac{C_0}{g}\left[x + \frac{x^3}{g^2} + o(x^3)\right] \xrightarrow{x<<g} 2C_0 \underbrace{\frac{x}{g}}_{\leq 16\%}.\end{aligned} \tag{2.6}$$

The dependency of the capacitive variation to the displacement is intrinsically non linear however for small displacement the equation can be approximated with its linear form. Yet the nonlinearity remains a limitation of the maximum displacement achieved by this technique: as it can be noticed in Figure 2.8 the linearity error exceeds 1% for a displacement larger that 16% of the initial gap.

Figure 2.7.*b* presents a scheme of the second detection method, the electrodes are set in a comb-like structure and this time the central electrode moves parallel to the fixed electrodes generating a change in the overlapping area between the fixed and the moving plates. In this case the capacitive variation as a function of displacement takes the following form:

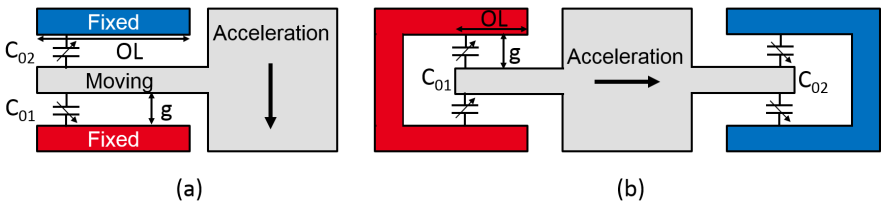


Figure 2.7: *Scheme of the two main capacitive detection techniques: (a) in gap variation the moving electrodes moves perpendicularly to two fixed electrodes inducing a differential capacitive change, (b) in surface variation the moving electrodes slide parallel to fixed electrodes causing a change in the overlapping area. The two sensing capacitors are referred as C_{01} and C_{02}, the gap as g and the overlap between the two parallel plates as OL.*

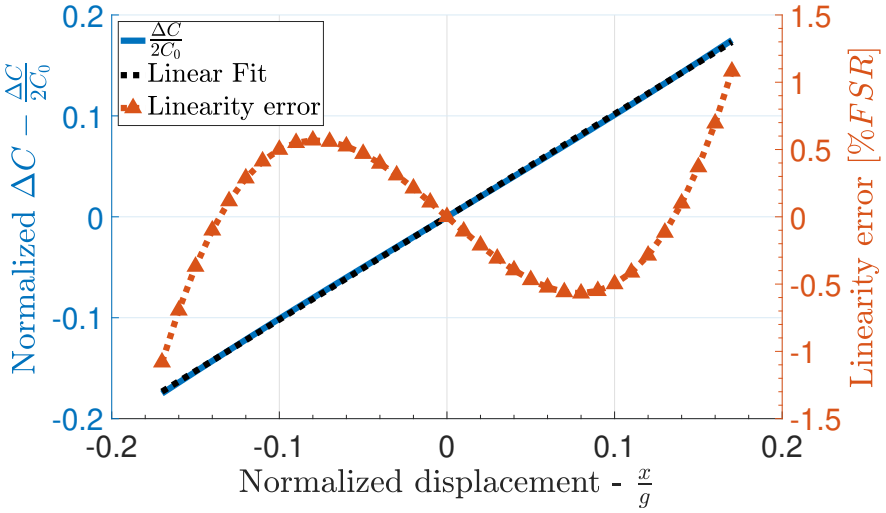


Figure 2.8: *Normalized capacitive variation with respect to normalized displacement. Non linear error is evaluated with respect to the maximum value of the linear fit.*

$$\Delta C = C_{01} - C_{02} = 2\epsilon_0 \frac{h}{g}(OL + x - (OL - x))) = 2C_0 \overbrace{\frac{x}{OL}}^{\approx 100\%} \tag{2.7}$$

now the capacitive variation is linear up to the point where x equals the overlap; in reality fringe fields effects and process non idealities have to be taken into account to evaluate the maximum linear range.
According to the equations written so far, given the same static capacitance, surface variation seems to be the most effective method for detection of the device displacement as it allows the largest capacitive variation. Nevertheless, in a real implementation, this technique is the less sensitive solution:

1. in order to have capacitive density, comparable to the gap variation technique, the condition $OL >> g$ is required (Figure 2.9.*a*). Assuming typical accelerometer gap ($1.5-3\mu m$) the resulting overlap would be in the order of several tens of microns. Such large displacement is not possible for typical MEMS accelerometers, therefore only a small percentage of the potential linear range could be used.

2. the alternative configuration is shown in Figure 2.9.*b*. This time the OL dimension is in the same order of magnitude of the gap size allowing to take advantage of the entire linear range. In this case, however, the capacitive density of the device decreases to the point of losing the advantage introduced by the smaller OL. Indeed reducing the overlap requires an increase of detection units and each detection unit requires anchor points to the

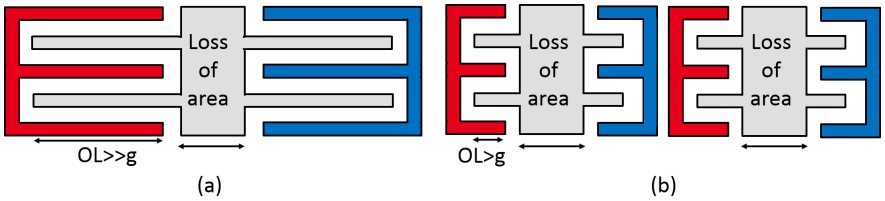


Figure 2.9: *Possible configurations for surface variation detection: (a) large overlap allows large capacitive density, but the travel range is limited; (b) small OL allows the use of the entire linear range at the cost of reduced capacitive density.*

substrate, which bring large area consumption, but do not contribute to the static capacitance of the device.

For these reasons almost all commercial accelerometers take advantage of gap variation architecture which allows higher scale factor for a given footprint. On the other hand surface variation is mainly used to obtain large displacement for devices than need to be actively moved, as for instance MEMS gyroscopes and micromirrors.
Yet, when moving to submicrometric gaps this rule might not hold due to the increase of non-linear effects that could further limit gap variation and not surface variation, therefore it is necessary to question again: is gap variation still better than surface variation when using a 3D technology that allows less anchor area and smaller gaps?
For this reason, the following subsection presents an analytical-numerical study that aims to compare the two mentioned topologies, in terms of scale factor, when implemented with the new fabrication process. The study takes into account both the capacitive density and the maximum allowed linear range. The latter is computed by combining the effects of the two main sources of nonlinearity: the electrostatic force and the capacitive detection.

Electrostatic nonlinearity

Applying a voltage across two electrodes generates an electrostatic force. The formula of the force can be obtained by taking the derivative of the energy stored on the capacitor (E):

$$F_{el} = \frac{\partial \overbrace{E}^{C_0 V/2}}{\partial x} = \frac{\partial C}{\partial x}\frac{V^2}{2}. \tag{2.8}$$

This is an attractive force which pulls together the two plates of the capacitor. For this reason, the moving electrode of a MEMS structure usually experiences two forces of opposite sign pulling towards the fixed electodes.

In the case of surface variation the term $\partial C/\partial x$ is constant and equal to C_0/OL. For any position of the device the forces generated by the positive and negative electrodes are always equal and counterbalanced making this architecture insensitive to the phenomenon. In the case of gap variation instead, the net force between the two capacitors can be written in the following form:

$$F_{el} = \frac{V^2}{2}\left[\frac{hOL}{(g-x)^2} - \frac{hOL}{(g+x)^2}\right] = \frac{C_0}{g}\frac{V^2}{2}\left[\frac{1}{\left(1-\frac{x}{g}\right)^2} - \frac{1}{\left(1+\frac{x}{g}\right)^2}\right]. \tag{2.9}$$

By using Taylor series development to the third order the equation can be rewritten as follows:

$$F_{el} = \frac{C_0}{g^2}\frac{V^2}{2}\left[4x + \frac{8x^3}{g^2} + o(x^3)\right] = \overbrace{2\frac{C_0V^2}{g^2}}^{k_{el}} x + k_{el}\frac{2x^3}{g^2} + k_{el}o(x^3) \tag{2.10}$$

where k_{el} is called electrostatic stiffness due to its linear dependency with the displacement. The linear term of the electrostatic force is usually compensated by an accurate design of the mechanical part (stiffer springs), on the other hand a non-linear component of the force remains. The presence of such non-linear term has to be considered when computing the displacement of the device following an external acceleration:

$$\begin{aligned} m\,a_{ext} = F_m - F_{el} \approx (k_m - k_{el})\,x - k_{el}\frac{2x^3}{g^2} = k_{eq}x - k_{el}\frac{2x^3}{g^2} \\ \rightarrow \underbrace{\frac{m\,a_{ext}}{k_{eq}}}_{x_{lin}} = x - \frac{k_{el}}{k_{eq}}\frac{2x^3}{g^2} \rightarrow x_{lin} = x - \alpha x^3 \end{aligned} \tag{2.11}$$

In the equation, higher order non-linear terms have been neglected for the sake of clarity. Several coefficients appear in the equation: k_{eq} is the equivalent stiffness of the system when taking into account the electrostatic softening $(k_m - k_{el})$; x_{lin} is the linear expected displacement due to an external acceleration $(m\,a_{ext}/k_{eq})$ and α is the nonlinearity coefficient equal to $2k_{el}/g^2k_{eq}$.
Assuming $x/g << 1$, Equation 2.11 can be rewritten in the following approximated form:

$$x \approx x_{lin} + \alpha x_{lin}^3 \tag{2.12}$$

This is the relation between the real and linear displacement taking into account electrostatic nonlinearity.

Capacitive and electrostatic non-linearities

In order to combine the two electrostatic effects, the displacement described by Equation 2.12 has to be used to evaluate the capacitive variation defined by Equation 2.6:

$$\begin{aligned}\Delta C &\approx 2\frac{C_0}{g}\left[x+\frac{x^3}{g^2}\right] \approx 2\frac{C_0}{g}\left[x_{lin}+\alpha x_{lin}^3+\left(\frac{x_{lin}+\alpha x_{lin}^3}{g^2}\right)^3\right] \\ &\approx 2\frac{C_0}{g}\left[x_{lin}+x_{lin}^3\left(\alpha+\frac{1}{g^2}\right)\right] = \underbrace{2C_0\frac{x_{lin}}{g}}_{(1)}\left[1+\underbrace{\underbrace{\frac{x_{lin}^2}{g^2}}_{(2)}\underbrace{\left(\frac{k_m+k_{el}}{k_m-k_{el}}\right)}_{(3)}}_{\text{Nonlinearity (NL)}}\right].\end{aligned} \tag{2.13}$$

Three terms are highlighted: (1) The linear term of gap variation detection, (2) the nonlinearity due to the capacitive change and (3) the amplification factor due to the electrostatic force (3). Assuming typical values of a consumer device ($k_m = 3.5N/m$, $g = 1.7\mu m$, $C_0 = 200fF$, $V = 1.8V$, $m = 6nKg$, $FSR = 8g$, $k_{el} = 0.44N/m$), the term related to the electrostatic force increases the non-linearity by 20%, therefore reducing the maximum allowed relative displacement. Although not negligible, in a typical MEMS accelerometers the electrostatic effect does not limit gap variation to the point of preferring surface variation.
When moving to sub-micrometric gap things can be different. In order to understand the dependency of the NL with the scaling of the gap, k_m and k_{el} should be replaced with more fundamental parameters like static capacitance, gap and FSR.

$$NL = \frac{x_{lin}^2}{g^2}\left(\frac{k_m+k_{el}}{k_m-k_{el}}\right) = x_n^2\left(1+\frac{\overbrace{2k_{el}}^{4C_0V^2/g^2}}{\underbrace{k_{eq}}_{mFSR/gx_{n_M}}}\right) = x_n^2\left(1+\underbrace{\frac{4C_0V^2}{mgFSR}}_{\gamma}x_{n_M}\right) \tag{2.14}$$

In the equation, the displacement was normalized to the gap ($x_{lin}/g = x_n$) while the electrostatic amplification was expressed as a function of γ, a coefficient directly related to the device parameters. x_{n_M} is defined as the maximum allowed normalized displacement.
The effect of the scaling is now visible. γ is inversely proportional to the gap and directly proportional to the capacitive density. As decreasing the gap means also

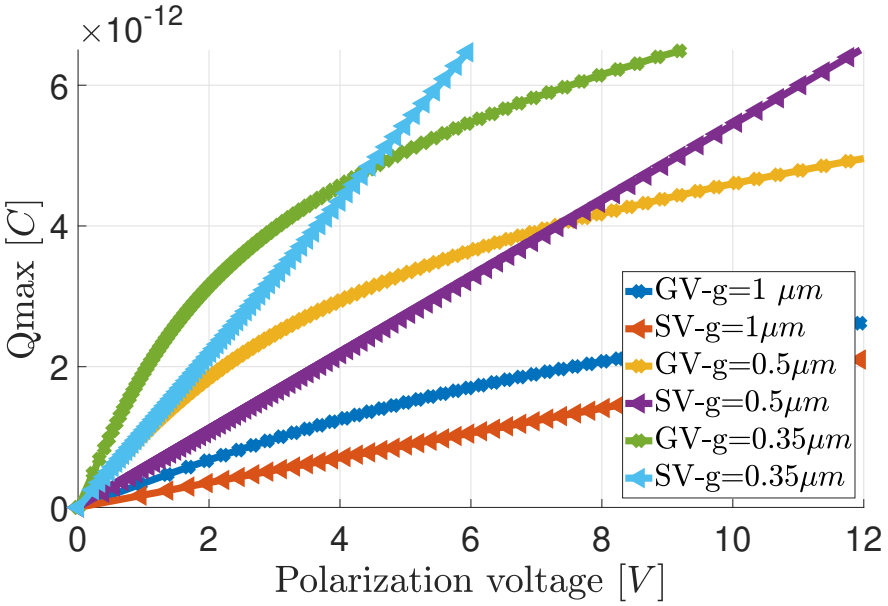


Figure 2.10: *Delivered maximum charge versus voltage for surface variation and gap variation topologies at three different gap sizes: 1μm, 0.5 μm and 0.35 μm. Scaling the gap lowers the voltage at which the surface variation becomes more efficient, allowing to reach better performances also at low voltages.*

linearly increasing the static capacitance, the γ factor decreases quadratically with the gap. For instance, using a 350nm gap, would increase the γ factor by more than 20 times with respect to a device with a consumer gap of $1.7\mu m$. This phenomenon forces a reduction of the maximum allowed displacement *i.e.* the maximum capacitive variation. Taking again the example of the consumer device presented before, the term x_{n_M} evaluated with Equation 2.14 decreases from 0.13 to 0.065, causing a reduction of the maximum relative capacitive change by 50%. The higher capacitive density offered by this topology is nulled by the loss of relative displacement for strong scaling of the gap.
In order to complete the study, the performance delivered by the two detection methods are evaluated for different gap sizes and plotted on the same graph. For each gap size, the two topologies are compared in terms of maximum delivered charge, evaluated according to this equation:

$$\Delta Q_{max} = 2C_0 x_{n_M} V \tag{2.15}$$

where x_{n_M} is evaluated by numerically solving Equation 2.14 at each polarization voltage given NL=1%. As a matter of fact the capacitive variation is always converted into charge by polarizing the electrodes. Since, the polarization voltage plays a role in the γ factor, expressing the performance in terms of charge, allows a more comprehensive comparison.
Figure 2.10 shows the dependency of the sensitivity with respect to the polariza-

tion voltage for both surface variation and gap variation at three different gap sizes. Ideally, surface variation becomes more efficient than gap variation at any gap size if large voltages are applied, however this condition is not achievable for most applications and second order electrostatic effects could start to appear also in surface variation. It is important to notice that gap scaling drastically reduces the voltage at which surface variation becomes more efficient, showing that the limitations introduced by the electrostatic effect becomes dominant at smaller gaps. The values of capacitors used for the simulations are based on the real devices fabricated using the new technology: capacitive density of gap variation is overestimated to prove the robustness of this law and is assumed to be ten times larger than the capacitance of surface variation. Full Scale Range is assumed to be 140 g in line with the devices design in this work, such Full Scale is at least a factor ten larger than most consumer products. In this way, it is shown that even for large FSR (smaller γ) surface variation is more effective. All values used for simulation are resumed in Table 2.1.

In conclusion, gap variation performance is limited by the combination of two sources of nonlinearity: non-linear capacitive transduction and electrostatic force unbalance. The first term is an intrinsic limit to the maximum achievable displacement of gap variation, however such limit is equal to a fixed percentage of the gap and therefore does not suffer from gap scaling. On the other hand the electrostatic force unbalance is inversely proportional to the polarization voltage, meaning that in principle at a certain voltage the electrostatic effect makes gap variation less efficient than surface variation. While such voltage is high for large gap devices, it soon lowers when scaling the gap, making surface variation more efficient also at low polarization voltage. Finally it should be mentioned that gap variation has to compensate the electrostatic force to first order, forcing the system to work at a given voltage and to require calibration of mechanical non-idealities. On the contrary, surface variation does not suffer from electrostatic softening and it can take advantage of different polarization voltage while keeping the same mechanical response.

Topology	Mass	Gap	C_0	FSR	x_{nM} (NL=1%)	$\omega_{0sv}/\omega_{0gv}$@1$V$
	$[nKg]$	$[\mu m]$	$[pF]$	$[g]$	[%]	$[kHz]$
SV	30	0.35/0.5/1	0.68/0.34/0.17	140	80	4.17
GV	30	0.35/0.5/1	6.8/3.4/1.7	140	$x_{n_M}(V)$	16/22/27

Table 2.1: *Parameters used for surface (SV) and gap (GV) variation comparison. The linearity limit is set at* 1%*, while the maximum normalized displacement for surface variation is set at 80 % in line with the experimental values. A FSR of 140g is taken, in-line with designed sensors and to prove the robustness of the law also at large full-scale (smaller* γ*)*

.

2.2.3 Comparison between surface variation and gap variation for out-of-plane accelerometers

The vast majority of out-of-plane accelerometers are made of moving structures suspended by torsional springs. The center of gravity of the moving mass is misaligned with respect to the springs axis of rotation, causing an external acceleration to induce a tilt of the mass. In this way, the moving structure approaches the substrate on one side and it separates from it on the other. Such movement causes a differential capacitive variation with respect to electrodes placed on the substrate [43]. The need of a tilting mechanism comes mainly from the impossibility of implementing electrodes above the moving mass for most of the industrial fabrication process, however using a rotation instead of a pure translation implies further limitations in the displacement of the device which can be linearly approximated only for small displacements. Such drawback can be over-

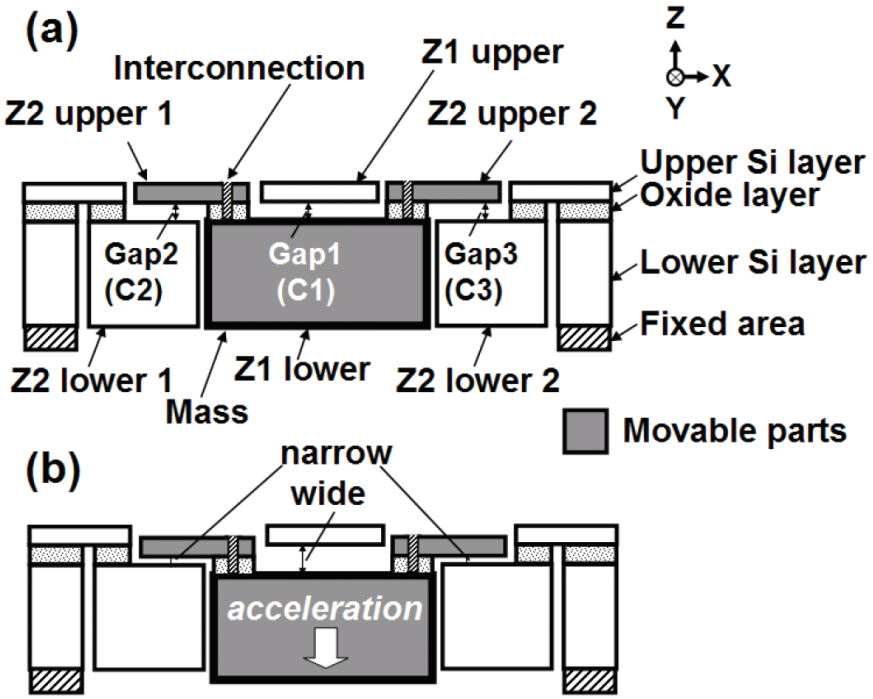


Figure 2.11: *Schematic cross-section of out-of-plane accelerometers using double-layer MEMS technology [42]. a) Fixed electrodes and moving elements are obtained in both upper and lower Si-layers which are held together with oxide. The first sensing capacitance is C1 while the second sensing capacitance is divided into C2 and C3. (b) During operation, the moving mass, held by upper layer springs, translates in the out-of-plane direction. The zig-zag configuration of the electrodes allows differential capacitive detection (C1 decreases while C2-C3 increase or vice-versa).*

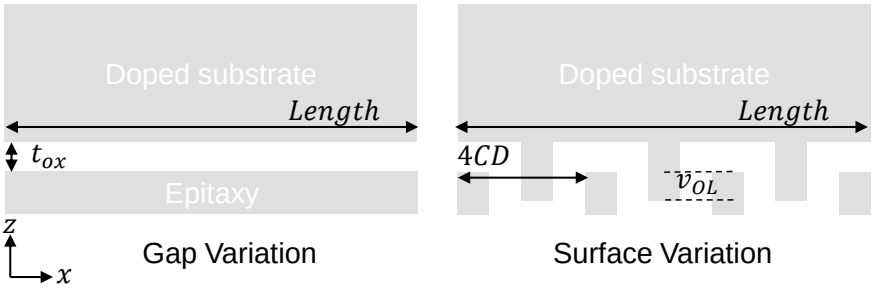


Figure 2.12: *Schematic cross section of two possible detection methods using novel fabrication process. A single-ended view is represented for clarity, however differential detection is possible in both cases.*

come using a double-layer fabrication where each layer can be used for both fixed electrodes and moving elements as shown in Figure 2.11. This time the device has top and bottom electrodes and it can therefore be designed to move in a pure out-of-plane translation.

The technique proposed by [42] could be used also for the z-devices implemented in this work thanks to the multi-layer fabrication. On the other hand, the new process allows the implementation of out-of-plane comb-fingers in order to exploit surface variation also for z-accelerometers. As for in-plane devices, the comparison between gap variation and surface variation detection for out-of-plane sensors is reported here. Figure 2.12 shows a schematic cross-section for two different sensing topologies of out-of-plane devices: gap variation method as presented in [42] and surface variation using novel out-of-plane combs. The advantages of surface variation over gap variation presented in subsection 2.2.2 are still valid, however further considerations on the capacitive density should be made in this case. The calculation is based on the cross-section represented in Figure 2.12. For the sake of simplicity, the two architectures are assumed to be uniform in the y direction (Depth). For the two topologies the following equations are obtained:

$$c_{0g} = \epsilon_0 \frac{1}{t_{ox}} \quad \text{and} \quad c_{0s} = 2 \frac{\overbrace{N_c}^{Length/4CD}}{Length} \epsilon_0 \frac{v_{ov}}{CD} = \epsilon_0 \frac{v_{ov}}{2CD^2} \tag{2.16}$$

where c_{0g} and c_{0s} are the capacitive densities of respectively gap and surface variation while t_{ox} is the thickness of the oxide layer. Both the gap and the comb-fingers width are assumed equal to the critical dimension of the thin layer etching. Taking the ratio between the two capacitive terms allows the comparison of the two architectures:

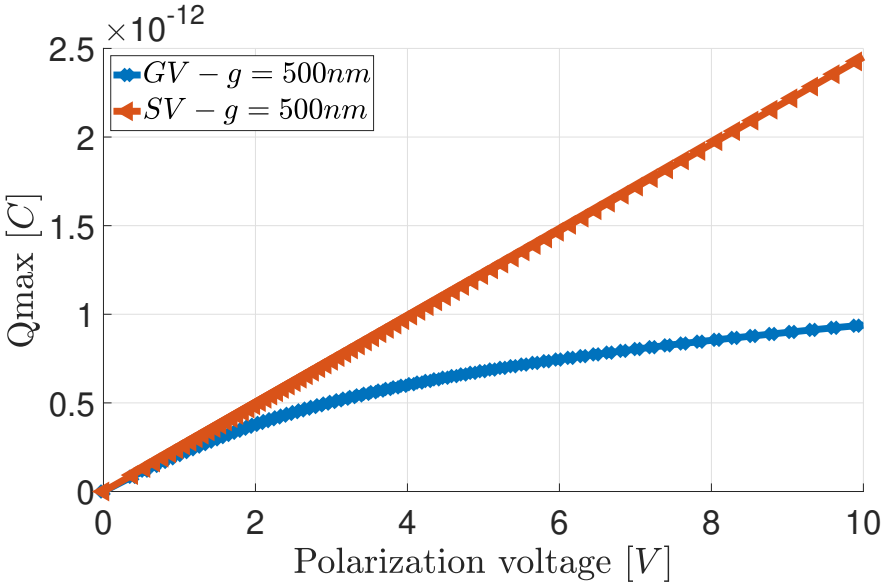


Figure 2.13: *Delivered maximum charge versus voltage for surface variation and gap variation topologies for out-of-plane sensors assuming gap size of 500nm and parameters reported in* 2.2.

Topology	Mass	Gap	C_0	FSR	x_{nM} (NL=1%)	$\omega_{0sv}/\omega_{0gv}$@1V
	$[nKg]$	$[\mu m]$	$[pF]$	$[g]$	[%]	$[kHz]$
SV	6	0.5	0.35	140	35	5
GV	6	0.5	0.7	140	$x_{n_M}(V)$	22.5

Table 2.2: *Parameters used for surface (SV) and gap (GV) variation comparison for out-of-plane sensors. This time the maximum normalized displacement for surface variation is set at 35 % in line with the assumptions made in the results section. This is half of the expected linear range according to numerical simulations.*

$$\frac{c_{0g}}{c_{0s}} = \frac{4CD^2}{\underbrace{v_{ov}}_{\approx 4CD}\, t_{ox}} \approx \frac{CD}{2t_{ox}} \tag{2.17}$$

where the vertical overlap is realistically assumed to be equal to 4 times the critical dimension to guarantee a comb-like shape. Assuming a CD and oxide thickness of 500nm the two capacitive densities differ by only a factor two. Figure 2.13 shows how the maximum charge delivered by surface variation is higher already at low voltages.

For this reason also for out-of-plane devices, surface variation seems to be the most effective detection method, allowing large linear range and high capacitive density and finally obtaining performance in line with in-plane devices.

2.2.4 Noise analysis

MEMS accelerometers suffer from two main noise sources, the Brownian Noise and the electronic noise of the detection system. The main source of Thermal noise or Brownian noise for MEMS accelerometers at atmospheric pressure is the collision of the device with the air molecules in the surrounding. This phenomenon generates a mechanical agitation of the sensor which leads to imprecision in the measurement. Such source of noise is the intrinsic limit of the detection of the accelerometer and its spectrum can be evaluated as follows [44]:

$$S_b = \frac{\sqrt{4\,k_b\,T\,b}}{m} = \sqrt{\frac{4\,k_b\,T\,\omega_0}{m\,Q}} \quad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{2.18}$$

where k_b is the Boltzman constant and T is the temperature of the system. In the first part of Equation 2.18, it can be seen how the Brownian Noise depends on the agitation of the air molecules: by lowering the temperature and the damping of the system or increasing the mass of the device, the influence of the collisions on the final resolution is reduced. However, as seen in subsection 2.2.1, the damping condition of the system are usually fixed by design and it is therefore better to express the Brownian Noise in terms of quality factor and resonance frequency. In this case it can be noticed that for a given factor Q, in order to reduce the Brownian noise is desirable to increase the mass of the accelerometer or reduce its resonance frequency. The force generated from the collision is equivalent to an external acceleration and it is therefore reported at the output of the system according to the device transfer function. This leads to a shaping of the noise spectrum, which presents a flat area for $\omega << \omega_0$ and it decreases by 40dB per decade after the device cut-off frequency.
The second source of noise is the electronic noise of the readout circuit. As described in Chapter 3, such noise depends on the chosen topology and the working condition, however the noise limit of any front-end is usually represented by its input referred voltage noise. In the case of a charge amplifier architecture, as the one used in this work, the electronic noise spectrum expressed in terms of charge can be written as follows (Equation 3.4):

$$S_q = S_v\,(C_p + C_0 + C_f) \quad \left[\frac{C}{\sqrt{Hz}}\right] \tag{2.19}$$

where S_v is the input referred voltage noise, C_p are the parasitic capacitance and C_f is the feedback one. In order to report this source of noise in terms of equivalent acceleration, Equation 2.19 is divided by the device scale factor expressed in charges per gravity unit. The scale factor can be computed by dividing the maximum charge delivered by the device (Equation 2.15) by the FSR. Here, the single-ended case is considered to remain consistent with the previous equation:

$$SF_{charge} = \frac{C_0 x_{n_M} V}{FSR} \tag{2.20}$$

the electronic noise equivalent acceleration (ENEA) can finally be computed.

$$S_{ENEA} = \overbrace{\frac{S_v}{V}}^{1} \overbrace{\frac{(C_p + C_0 + C_f)}{C_0}}^{2} \overbrace{\frac{FSR}{x_{n_M}}}^{3} \quad \left[\frac{m/s^2}{\sqrt{Hz}}\right] \tag{2.21}$$

In 2.21 three contributions are highlighted. The first term is related to voltage sources: increasing the actuation voltage or reducing the input referred voltage noise of the front end amplifiers, lowers the electronic noise floor. The second term is the capacitive term: the electronic noise is amplified by all capacitors referring to the input node of the operational amplifier while the signal depends on the active capacitance of the device (Figure 3.2). Minimizing parasitics and feedback capacitor with respect to static one improves the signal to noise ratio. The third term is related to the mechanical and electrical aspects of the device: as discussed in the previous subsection the normalized displacement needs to be maximized in order to take advantage of the maximum capacitive change, while reducing the FSR means reducing the resonance frequency and therefore increasing the mechanical sensitivity of the device. It should be pointed out, in order to complete the comparison between gap variation and surface variation, that in an ideal system where the capacitive term is equal to one (parasitic and feedback capacitor are negligible), the surface variation proves to be the most effective solution thanks to the higher maximum normalized displacement.
In conclusion, while the Brownian noise can be lowered by increasing the inertial mass of the sensor, the reduction of the electronic noise equivalent acceleration can be obtained by the following design choices: (i)increase of actuation voltage, (ii) reduction of input referred voltage noise, (iii) decrease of the parasitic capacitances and finally (iv) by having large linear range or reduced FSR. Before addressing the design of the first devices using the proposed fabrication process, Table 2.3 presents a summary of the main parameters discussed in this section together with the related performance considerations.

2.2.5 In-plane accelerometer design

After having discussed the main parameters of MEMS accelerometers and their relation to the sensor performance, the design flow of the devices is discussed here. The layout of the first MEMS accelerometers aimed to verify the potentiality of the novel fabrication process by designing devices for different type of applications and, at the same time, showing the possibility of achieving high-performance with a reduced footprint. Five families of devices have been designed: the main difference between each group is the size of the sensor, the acceleration to capac-

Parameter	Symbol	Unit	Design considerations
Resonance Frequency	ω_0	rad/s	Bandwidth/Scale factor/Stiffness
Mass	m	Kg	Brownian noise/Stiffness
Stiffness	k	N/m	Adhesion problems
Quality factor	Q	-	Brownian noise/Shock and vibrations response
Static capacitance	C_0	F	Electrical scale factor/ENEA
Max Normalized Displacement	x_{n_M}	-	Scale factor/Resonance frequency

Table 2.3: *Summary of the main device parameters which are set during the design of the sensors. For each parameter, the relation with the sensor performance is listed.*

itance Scale Factor (SF) and the thermo-mechanical noise. For each family, the following work-flow was followed:

1. The design started by defining the fabrication rules allowed by the process and by modeling of the possible device architecture with 3D-CAD software. Indeed, working with a multi-layer technology implies overlapping of different mechanical layers and therefore graphical visualization helped avoiding design errors.

2. Analytical study of the mechanical and electrical properties of the sensors. Resonance frequency, damping coefficient and static capacitance were estimated during this step and designed to match the desired performance.

3. Finite Element Method (FEM) simulations were used to perform modal analysis and linearity study of the transduction process and to verify analytical estimates.

4. Finally, the layout of the sensors was performed with a software developed at CEA-Leti: the program allows the design of parametric cells (p-cells) which are then translated into the real layout using a list of desired parameters. In this way several variants of the same structure can be obtained with a single parametric cell. At the end, using few p-cells, more than 80 different devices were laid out only for in-plane accelerometers.

Table 2.4 gives an overview of the five groups of designed devices. The performance range given for each group is due to different gap sizes and variants in the mechanical design of the springs. The advantages of the novel fabrication are already visible for large sensors (XL-L). These devices reach sub-μg Brownian noise and large scale factor within a footprint 3 to 30 times smaller than similar devices [45, 33]. Strong improvement is visible also for smaller topologies (S-XS), which achieve large DR within a consumer footprint thanks to the high capacitive density and the relatively low thermo-mechanical noise.
In this work, only the S-devices family is discussed. Characterization of larger

Family	f_0	BN	SF	FSR	Dynamic Range (DR)(BW=1Hz)	Size
	kHz	$\mu g/\sqrt{Hz}$	fF/g	g	dB	$\mu m x \mu m$
XL	0.25-0.5	1-2	1e3-10e3	0.5-2	120	1200x1400
L	0.8-1.6	3-6	100-400	5-20	130	600x1000
M	2.5-5	5-10	3-12	70-280	150	500x600
S	3.3-6.6	6-12	1.5-6	90-360	151	400x600
XS	5-9	20-40	0.4-1.5	180-700	150	350x400

Table 2.4: *Overview of the five different families of in-plane accelerometers. Performance span from seismic grade accelerometers to compact high dynamic range sensors.*

devices was not possible due to an issue in the mask design, while extra-small sensors required a dedicated thickness and were therefore not fabricated for the sake of time. The design flow of the S-devices with double fold springs is presented here, however the same procedure was followed for all structures.

Analytical study for in-plane devices

As mentioned before, one of the goal of the first design was to fabricate devices with $\mu g/\sqrt{Hz}$ resolution and the largest possible full scale within a consumer footprint. The accelerometer thus requires low Brownian noise, sufficiently high scale factor in order for the mechanical noise to dominate over electronic noise, and large linear capacitive variation to ensure high-g FSR. Table 2.5 summarizes the main parameters of the two accelerometers discussed in the results section: the S-500nm and S-350nm. The two sensors have the same mechanical structure, with respectively 500 and 350 nanometer gap size. The devices are suspended by four folded springs. The folded beam is made of 2 beams connected in series, each beam is referred to as fold (2.16). Mechanical stiffness (k) is calculated by combining the stiffness of each fold (k_f), evaluated according to Equation 2.22:

$$k_f = ET\left(\frac{L_{fold}}{W_{fold}}\right)^3 \tag{2.22}$$

where E is the Young modulus of $< 110 >$ single crystal silicon, L_{fold} is the length of each fold, W_{fold} their width and T the thickness of the thick silicon layer. As the last two parameters are fixed, the springs are designed to have the maximum length for a given footprint. For this reason, the connection between the mass and the springs is made with protruding structures which allows the extension of the springs up to the limit of the footprint. This permits to avoid excessively stiff structures with poor mechanical scale factor. Moreover, the new technology allows the reduction of the area dedicated to the anchor points, by using common anchors for all the fixed elements. For instance, all suspended electrodes share the same two anchor points. This allows maximizing the area dedicated to the inertial mass further increasing the mechanical scale factor. Af-

ter the sensor structure has been defined, the mass of the device is evaluated with a 3D-virtual model and together with the calculated stiffness, is used to compute the resonance frequency (f_{0th}).
The total damping coefficient is estimated by summing the squeeze film damping (b_{sq}) of the thick layer and the slide film damping of the comb-fingers (b_{sl}), calculated as follows [46, 47]:

$$b_{sq} = \frac{\mu L_{fold} T^3}{g_{sp}^3}\beta \quad b_{sl} = 4\,Nm\frac{\mu OLt}{g} \tag{2.23}$$

In the case of squeeze film the main contribution comes from the springs motion therefore g_{sp} is the gap between the spring fold ($5.4\mu m$) and β is a geometrical coefficient as reported in [46]. For this rough estimate, the springs are assumed to be two surfaces moving parallel to each other. For the slide film damping, OL and g are the overlap and the gap between fixed and moving electrodes, N_m the number of moving combs and t is the thickness of the fixed combs. μ is the viscosity of air at room temperature and atmospheric condition. By computing Equation 2.23, values of b_{sq} of 5.2e-4 Ns/m and b_{sl} of 1.2-2e-6 Ns/m are found, showing that the dominant damping source is the springs squeeze film effect. This effect is identical for both 350 and 500nm devices. Together with the mass of the device, the damping coefficient can be used to evaluate the Brownian noise floor. The estimated value of 9.5 $\mu g/\sqrt{Hz}$ is found in line with desired performance.
After the mechanical analysis of the sensor, the electrostatic study was performed. As explained in the previous part of the chapter, surface variation was chosen over gap variation as the best detection method. While thickness and minimum gap of the electrodes were defined by the fabrication process, the overlap was set equal to 2 μm for the following reasons: (1) it has to be greater than the gap in order to ensure a comb-like shape (2) this way, it is equal to the vertical overlap of out-of-plane devices which is set again by process flow. After the geometry and the number of moving electrodes have been defined, the static capacitance of the device can be computed using the following equation:

$$C_{0th} = 4F_f\epsilon_0\frac{N_m OLt}{g} \tag{2.24}$$

where ϵ_0 is the vacuum permittivity, F_{fxy} is the fringe field coefficient calculated from finite elements simulations (1.098 and 1.139 for 350nm and 500nm devices respectively).

Parameter	**Symbol**	**S-500nm**	**S-350nm**	**Unit**
Young Modulus <110> Si	E_p	169	169	GPa
Mass	m	30e-9	30e-9	Kg
Length of first fold	l_{fold1}	480	480	μm
Length of second fold	L_{fold2}	495	495	μm
Width of each fold	W_{fold}	4.6	4.6	μm
Fold thickness	T	100	100	μm
Stiffness	k	28.4	28.4	N/m
Analytical resonance frequency	f_{0a}	4894	4894	Hz
FEM resonance frequency	f_{0th}	4890	4890	Hz
Gap between springs	g_{sp}	5.4	5.4	μm
Beta coefficient	β	0.9	0.9	
Slide film damping	b_{sl}	1.2e-6	2.6e-6	Ns/m
Squeeze film damping	b_{sq}	5.2e-4	5.2e-4	Ns/m
Number of moving electrodes	N_m	800	1032	
Overlap	OL	2	2	μm
Heigth of fixed combs	t	5	5	μm
Gap between combs	g	0.5	0.35	μm
Fringe field coefficient	F_{fxy}	1.139	1.098	
Differetial static capacitance	C_{0th}	645	1147	fF
Brownian Noise	BN	9.5	9.5	$\mu g/\sqrt{Hz}$
Scale factor	SF	3.35	5.95	fF/g
Full Scale Range (NL=1%)	FSR	192	192	g
Dynamic Range	DR	146	146	dB
Footprint		400x600	400x600	μmxμm

Table 2.5: *Electrical and mechanical parameters of the first designed XY-axis accelerometers*

Numerical simulation for in-plane devices

After analytical considerations the devices were simulated by FEM, (Comsol multiphysics) in order to verify the frequencies of the mode of interest, but also of the other modes and most importantly to assess the linearity of the surface variation transduction. Figure 2.14 shows the 3D model of a comb-finger unit. The position of the moving plate was swept across the entire travel range while keeping a constant potential across the fixed and moving parts. The capacitance variation was calculated from the variation of electrical energy between the air volumes around the two fixed structures, see Figure 2.15.

The linear fit (ΔC_{fit}) of the data was performed and the value of static capacitance (C_0) was extracted assuming the following relation:

$$\Delta C_{fit} = C_0 \frac{x}{OL} \tag{2.25}$$

where x is the displacement of the moving plate with respect to the initial central position and OL the geometrical overlap. The evaluated C_0 is compared to the theoretical one and used to compute the fringe field coefficient for both 500nm and 350nm devices while the linearity error (ϵ) is evaluated as follows:

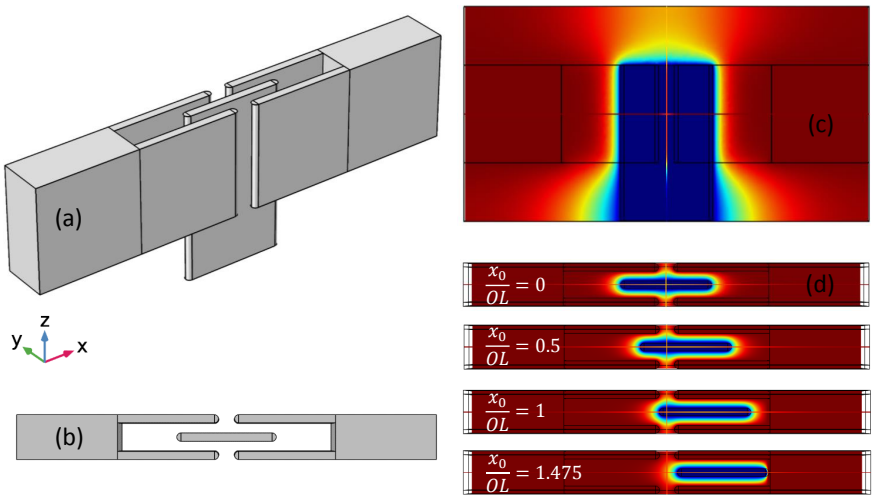


Figure 2.14: *(a-b) 3D and top view of FEM model of a comb-finger unit used to evaluate linearity and fringe fields coefficient. (c) Side view of the electric potential distribution. (d) Top view of electrical potential distribution between the combs for different positions. The two fixed electrodes are grounded while the moving plate is set at 1V. The differential capacitive variation is obtained by computing the difference between the electrical energy in the air volumes around the two fixed elements while sweeping the central plate position.*

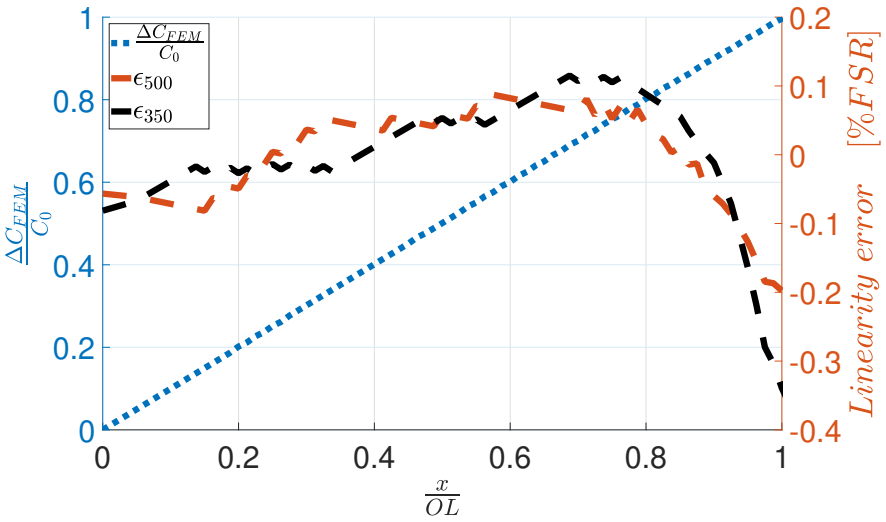


Figure 2.15: *Plot of the relative capacitive variation and related linearity error with respect to the displacement of the moving comb normalized to the initial overlap for both 500 and 350nm devices. According to simulation the linearity remains within 1% also beyond complete static capacitance variation thanks to fringe fields and differential detection.*

$$\epsilon(x) = \frac{\Delta C_{FEM}(x) - \Delta C_{fit}(x)}{C_0} \tag{2.26}$$

The plot representing the linearity error versus normalized displacement is reported in Figure 2.15. The simulated capacitive variation remains within 0.5% of linearity even when the displacement is equal to the initial overlap, *i.e.* when one of the fixed electrode does not overlap with the moving electrode anymore. As shown in the sequence of images in Figure 2.14.*d* such linear behavior is due to the extent of the fringe field and the differential architecture. The simulation shows how the nonlinearity error increases when the moving plate approaches the point of zero overlap: at this stage one of the fixed electrode is not effective anymore and the sensitivity tends to decrease.
Next, a modal analysis was performed and the results are shown in Figure 2.16, for a device with four 4.6 μm wide springs (value according to SEM observations) having two folds each. The first mode is the mode of interest with a frequency around 4.9 kHz. Modes from 2 to 5 are spring modes and fall between 25 to 34 kHz; finally the first out-of-plane mode is located at 62 kHz. This large shift from the mode of interest is obtained thanks to the 100 μm thick layer. It should be noted that no spurious modes are located inside the audible range making the structure robust against sound vibrations, assuming a low quality factor for the first mode.
Finally, three different structures having respectively one, two and four spring

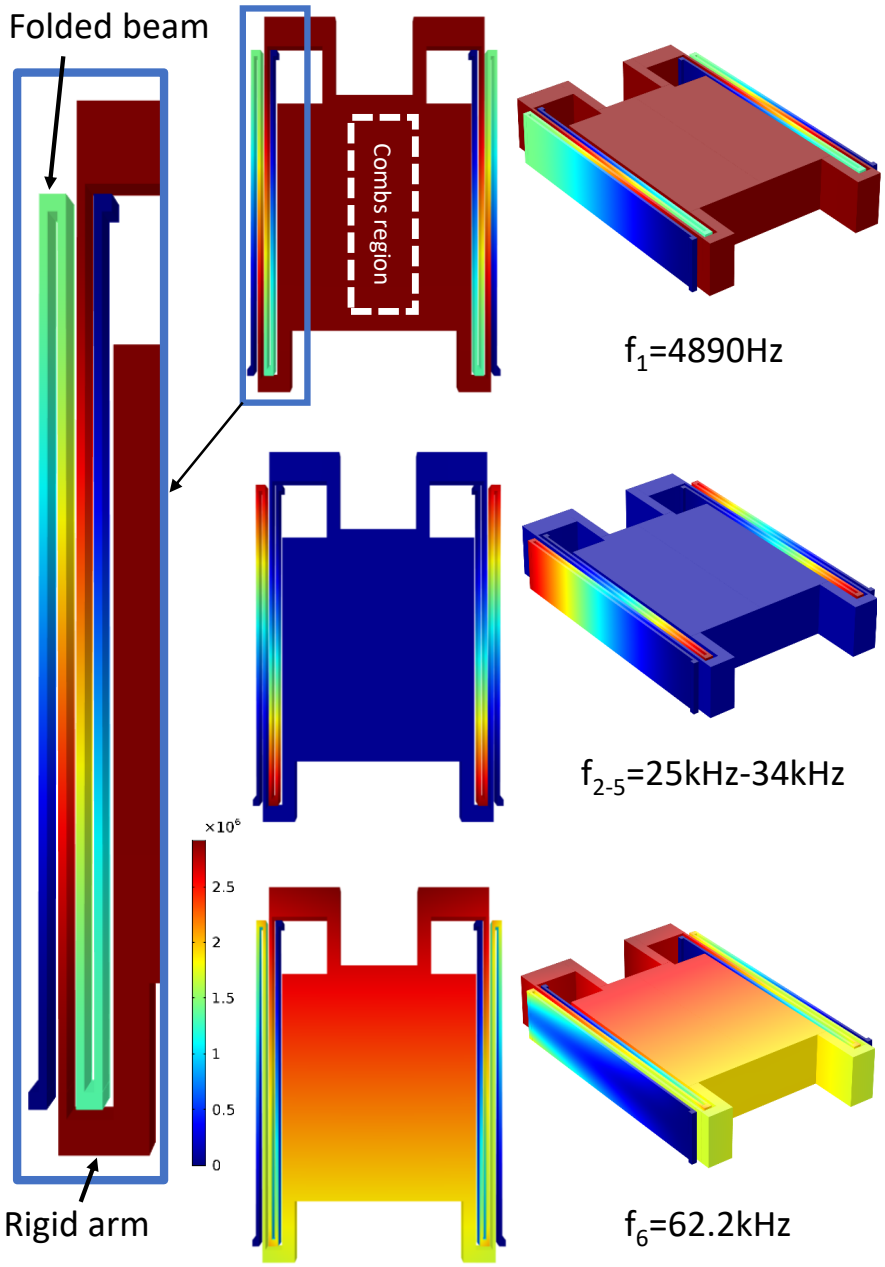


Figure 2.16: *Bottom and 3D view of modes analysis using COMSOL Multiphysics. The first mode confirm the analytical prediction, while higher modes are found outside the audible range. The out-of-plane mode shows a stiffness more than 100 times bigger than the one in the desired in-plane direction. The combs region is highlighted in the bottom view image of the first mode. (left) Zoomed image of the springs system during first mode displacement. The springs are folded beams connected to the mass using rigid arms.*

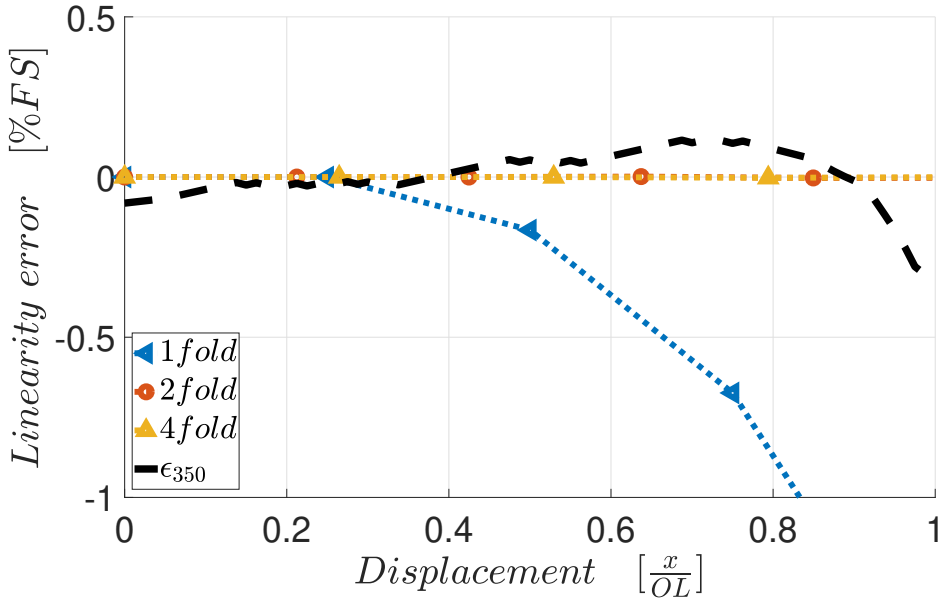


Figure 2.17: *Linearity error versus displacement for three spring types having one, two and four folds compared to electrostatic error. Different values of force were applied to the entire device volume in order to generate the desired displacement. 10 % of the force was directed in each of the two cross-axis direction in order also to verify the effects of cross-axis on the linearity. The final results show that for a displacement equal to the initial overlap, the mechanical nonlinearity and cross-axis are negligible for both four folds and two folds structures compared to the electrostatic nonlinearity.*

folds were simulated. The spring linearity limit was studied by applying a force, yielding a 2 μm displacement (*i.e.* the overlap). At the same time, 10% of the force was pointed in each of the two cross-axis directions to assess potential cross-axis effects due to, for example, incorrect mounting of the device during tests. Figure 2.17 shows that the linearity error is negligible for the two- and four-fold devices and that it remains within 2 % for the single fold device. Both mechanical nonlinearity and cross-axis sensitivity should then be negligible with respect to the electrostatic one. Table 2.5 summarizes the performance expected from design. Theoretical scale factor from 3 to 6 fF/g are expected. As the theoretical Brownian noise is equal to 9.5 μg, the required electronic noise floor is in the order few tens of $zF/\sqrt{Hz}$.

2.2.6 Out-of-plane accelerometer design

As for the in-plane devices, different types of Z-axis accelerometers have been designed. This time the thickness of the proof mass layer was reduced to 50 μm due to problems related to the notching as explained in the fabrication section.

Family	$\mathbf{f_0}$	**BN**	**SF**	**FSR**	**DR**(BW=1Hz)	**Size**
	kHz	$\mu g/\sqrt{Hz}$	fF/g	g	dB	μmxμm
L	0.5-4.2	2.2-7.4	40-5700	2-140	115-143	1000x1000
M	6-12	20-32	0.4-9	100-1200	134-150	600x600
S	3.2-5.6	20-26	2-12	80-250	133-140	470x470

Table 2.6: *Overview of the three different devices family of out-of-plane accelerometers. Performances span from seismic grade accelerometers to compact high dynamic range sensors. All performances refer to 50 μm thick devices, however the use of 100 μm layer would lead to considerable improvement in the Brownian noise and scale factor of the sensors aligning the performance to those of in-plane accelerometers.*

Nevertheless, the same structures could be fabricated with a 100 μm MEMS layer, allowing further reduction of the thermo-mechanical noise and the resonance frequency *i.e.* increase of SF. This would align the performance with in-plane sensors and allow the fabrication of a 3-axis accelerometer with 100 μm thickness. Table 2.6 reports the main parameters for each family of sensors. With respect to in-plane devices, a larger performance range is present. The higher variability is mainly related to a large number of degrees of freedom in designing the spring system. As a matter of fact width, thickness and length of the springs were changed for different designs leading to consistent changes in the resonance frequencies and the scale factor of the sensors. The Brownian noise values reported in the table are given assuming a quality factor equal to 1. Considering the experimental results, this is a reasonable assumption. Once again, the L-devices reach thermo-mechanical noise floor in the order of few $\mu g/\sqrt{Hz}$ and SF up to few pF per g with a footprint of only one squared mm, showing again drastic size reduction with respect to devices having similar performance [48, 49]. M and S-devices reach theoretical FSR of several hundreds gravity units and Brownian Noise floor of few tens of $\mu g/\sqrt{Hz}$, achieving very large DR within a consumer sensor size.
As for in-plane devices analytical and numerical simulations are here presented. The specific case of an M-500nm and S-500nm sensors are taken in order to give specific example of the design flow.

Analytical study of z-axis accelerometers

One of the main feature of the new fabrication is the possibility of implementing out-of-plane comb-fingers (2.2.3). Using such detection method requires the sensor to move in a pure vertical translation as a tilting movement could cause nonlinearity of the transduction process. The most simple way to obtain a vertical displacement is to implement flexural springs using the thin MEMS layer. The reduce thickness enables sufficiently low resonance frequency, which would not

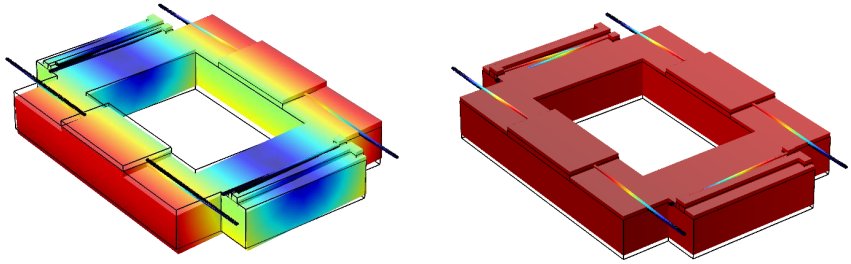
be possible with typical thickness of an industrial process. In this way, however, nothing impedes an out-of-plane tilt motion of the structures; causing undesired mode to appear close to the pure translational mode (Figure 2.18). For a single-layer process, the tilting mode would be actuated by a rotational acceleration. In the case of a double-layer process however, the center of gravity of the device and the springs do not lay on the same horizontal plane. For this reason, any in-plane acceleration acts on the lever arm between the springs anchor point and the center of gravity. This causes a momentum which leads to a tilt of the structure. The obtained out-of-plane devices would therefore be sensitive also to in-plane accelerations.

In order to avoid this problem it is necessary to implement a spring system which would allow only out-of-plane pure translation.

Figure 2.19 shows a schematic view of the proposed anti-tilt architecture. As shown in the cross-section, for a pure translational movement, the torsional springs undergo the same pure torsion and the rigid central connection moves parallel to the substrate opposite to the mass. Instead, in the case of a tilting movement, the central connection is pulled in opposite directions by the rigid arms which are bound to both the mass and the anchor points. In order to allow such movement, the central connection or the connected springs should strain in the out-of-plane direction. Such deformation required additional energy and leads to an increase of device stiffness for the tilt mode.

The same result could be obtained by coupling the two arms with a single torsional spring, as shown in Figure 2.20 for the S-device. In this case, the need for a flexural deformation of the spring connecting the two arms is even more evident.

Figure 2.20 shows the top view of the two main Z-axis architectures: the M-Z and S-Z. The images are taken from the Comsol Multiphysics model of the two accelerometers, image editing is used to add fixed parts. The M-Z device was



$f_{tilt} = 3861Hz$ $f_{trasl} = 4104Hz$

Figure 2.18: *Mass suspended by flexural springs. Tilting mode is close to desired out-of-plane mode or even at lower frequency. Normal flexural springs allow pure translational movement, but do not impede the tilting of the structure. The problem is worsen by the misalignment between the center of mass and the springs plane.*

designed to be highly symmetrical and with large stiffness to ensure robustness. The devices present four anti-tilt springs system identical to the one described above together with four pairs of flexural springs which are used to increase the stiffness of the device for the in-plane direction. In this way the xy-motion of the device is small even for large accelerations (shocks), avoiding contact between fixed and moving structures, which could damage the sensor. For this reason, these springs are referred to as anti-shock springs.
In order to evaluate the total stiffness of the sensors it is necessary to compute the stiffness of the two springs systems.
The stiffness related to the flexural springs takes the following form:

$$k_f = \sum_{i=1}^{N_f} E_p \left(\frac{t_{fi}}{l_{fi}}\right)^3 w_{fi} \tag{2.27}$$

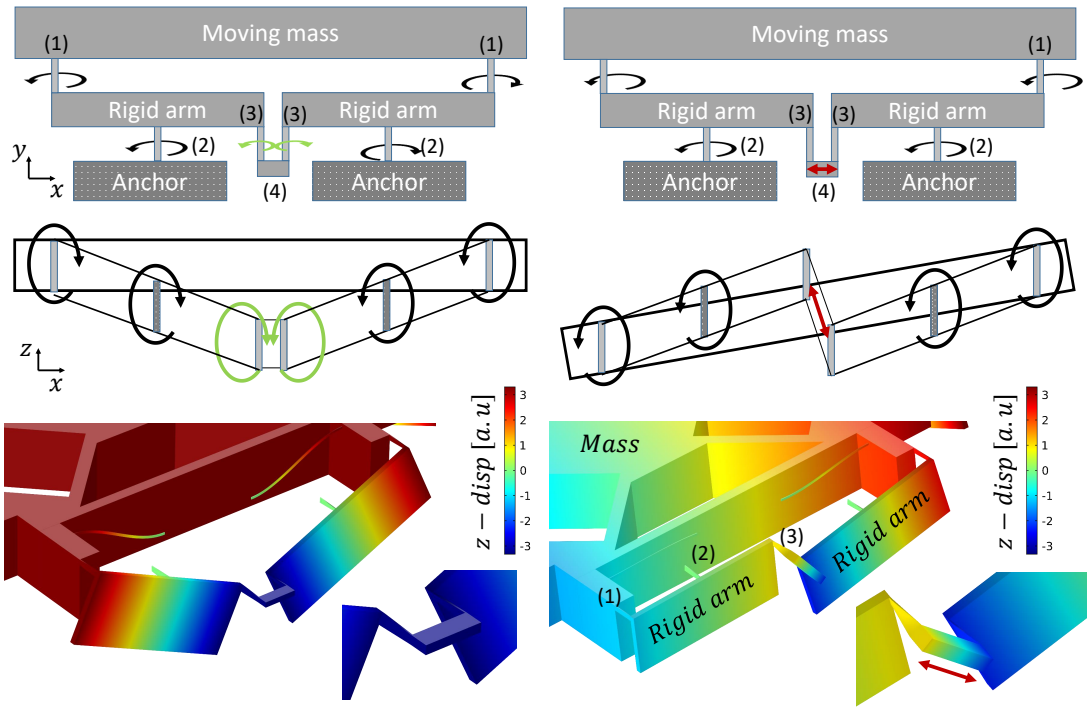


Figure 2.19: *Different views of the proposed anti-tilt springs: the mass is linked to two rigid arms by a pair of torsional springs (1), the two arms are connected to anchor points by a second pair of torsion bars (2); finally the two levers are bounded in the center region to a rigid connector (4) by a third springs pair (3). During pure out-of-plane translation all the springs are subject to torsional movement. In the case of tilt, the central springs (4) are pulled in opposite directions by the two arms and undergo flexural deformation. The introduction of the additional stiffness induces a frequency increase of the undesired mode.*

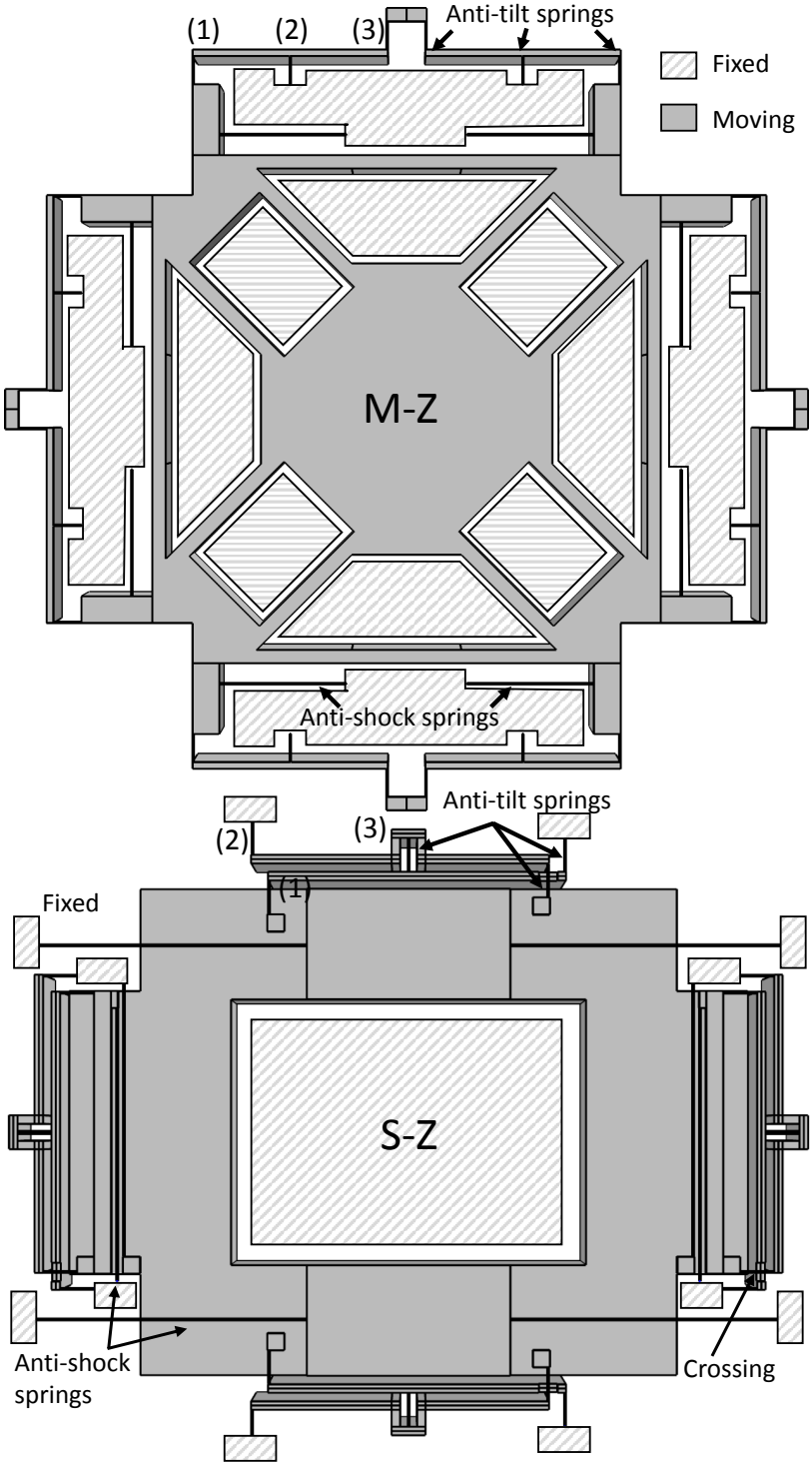


Figure 2.20: *Top view of two main Z-axis architectures, the M-Z and the S-Z. Anti-tilt and anti-shock spring systems are highlighted.*

where N_f is the number of flexural springs, t_f and l_f their thickness and length and w_f their width. E_p is the Young modulus of polycrystalline silicon. As a matter of fact, the springs are mainly grown above the oxide layer, having therefore an amorphous structure as mentioned in subsection 2.1.
The anti-tilt spring stiffness (k_{at}) has a slightly more complicated form. The elastic modulus for the tilt motion can be obtained by computing the dynamic equilibrium of the system for an out-of-plane displacement (Δz). The torque induced by an external force F_z is absorbed by torsion beams angular stiffness k_t:

$$\overbrace{\Delta z\, k_{at}}^{F_z} L_l = \sum_{j=1}^{N_t} k_{t_j} \overbrace{\theta}^{\approx \frac{\Delta z}{L_l}} \rightarrow k_{at} = \sum_{j=1}^{N_t} \frac{k_{t_j}}{L_l^2} \tag{2.28}$$

L_l is the lever arm between the anchor points and the torsion bars connected to the mass (Figure 2.18). All levers are of equal length, therefore the contribution of the eight arms can be expressed with a single term ($F_z L_l$). N_t is the number of torsional springs and θ is the angle described by the rigid connections which can be approximated with $\Delta z / L_t$ for small displacements. Finally k_t is the torsional stiffness of the springs, which can be expressed as [50]:

$$k_t = \beta_t \frac{t_t\, w_t^3}{l_t} \frac{E_p}{2(1+2\nu)} \tag{2.29}$$

with w_t, l_t and t_t being respectively the width, the length and the thickness of the torsional springs and ν is the Poisson ratio of polycrystalline silicon. β_t is a geometrical coefficient with the following equation:

$$\beta_t = \left(\frac{1}{3} - 0.21\frac{b}{a}\left(1 - \frac{b^4}{12a^4}\right)\right) \quad a = min(w_t, t_t);\ b = max(w_t, t_t); \tag{2.30}$$

According to Equation 2.28, it is clear that, increasing the length of the lever or reducing the value of (k_t), lowers the resonance frequency of the device.
Both these solutions are adopted for the S-devices. The torsional stiffness is reduced by partially etching the springs. This allows the reduction of the stiffness by more than a factor two, yet it introduces another dependency to process non-idealities. Second, the springs connecting the rigid arms to the anchor points are set at the end of the lever system (and not in the center as in M-Z), this allows the reduction of the device footprint without worsening its mechanical scale factor. Such configuration is possible thanks to the multi-layer process which allows crossing of the rigid arm and the torsion bars using different layers. Concerning the central springs connecting the two rigid arms (3), their stiffness has to be accounted twice when computing Equation 2.28. The width of the central springs of each axis has to be tuned in order to compensate the slight asymmetry of the sensor and obtained matched tilting modes. In this way the

device has the same response to any in-plane accelerations. The total stiffness of the device can finally be written in its general form:

$$k_{tot} = \sum_{i=1}^{N_{fl}} k_{fl_i} + \sum_{j=1}^{N_t} \frac{k_{t_j}}{L_l^2}. \tag{2.31}$$

Finally, the mass of the devices is calculated starting from the volume of the device in the FEM model and is used to compute the resonance frequency.
After having described the mechanical structure, the detection system can be addressed. Figure 2.21 shows the schematic top view and the cross-section of the two architectures this time highlighting the electrodes areas. As for the mechanical design, the M-Z presents a highly symmetric structure. In this way any cross-axis acceleration or undesired mode is rejected by the capacitive detection. The electrodes of the S-devices are designed with a different approach. This time the mass has two different polarizations while there is only a fixed electrode anchored in the central region. This configuration allows the reduction of the anchor points for the fixed electrodes reducing the footprint of the sensor. This a clear advantage of the new technology, indeed having different polarization for the moving mass is not possible with a standard MEMS process. Furthermore, having a single central connection allows the increase of the area used for the eutectic bonding and the oxide surface connecting the two layers, in this way the anchor is more solid.
The schematic view of the detection unit is shown in the zoomed area of Figure 2.21: a regular grid interdigitated with partially etched comb-fingers.
The differential static capacitance can therefore be calculated as follows:

$$C_{0thz} = 4F_{fz}\epsilon_0 \frac{N_c(L_c + W_c)V_{OL}}{g_c} \tag{2.32}$$

where N_c is the number of central comb-fingers for each electrode, L_c and W_c the length and the width of the comb-finger and g_c is the gap separating the grid and the finger. Like for the in-plane devices F_{fz} is the fringe field correction factor evaluated with FEM simulations.

The equations described so far have been used to evaluate the theoretical resonance frequency and static capacitance of all the devices listed in table 2.6. Table 2.7 summarizes the theoretical and simulated values of two devices from the M and S families corresponding to the devices tested in the result section. Like for in-plane devices, the detailed design-flow of two sensors is addressed in the following subsections.

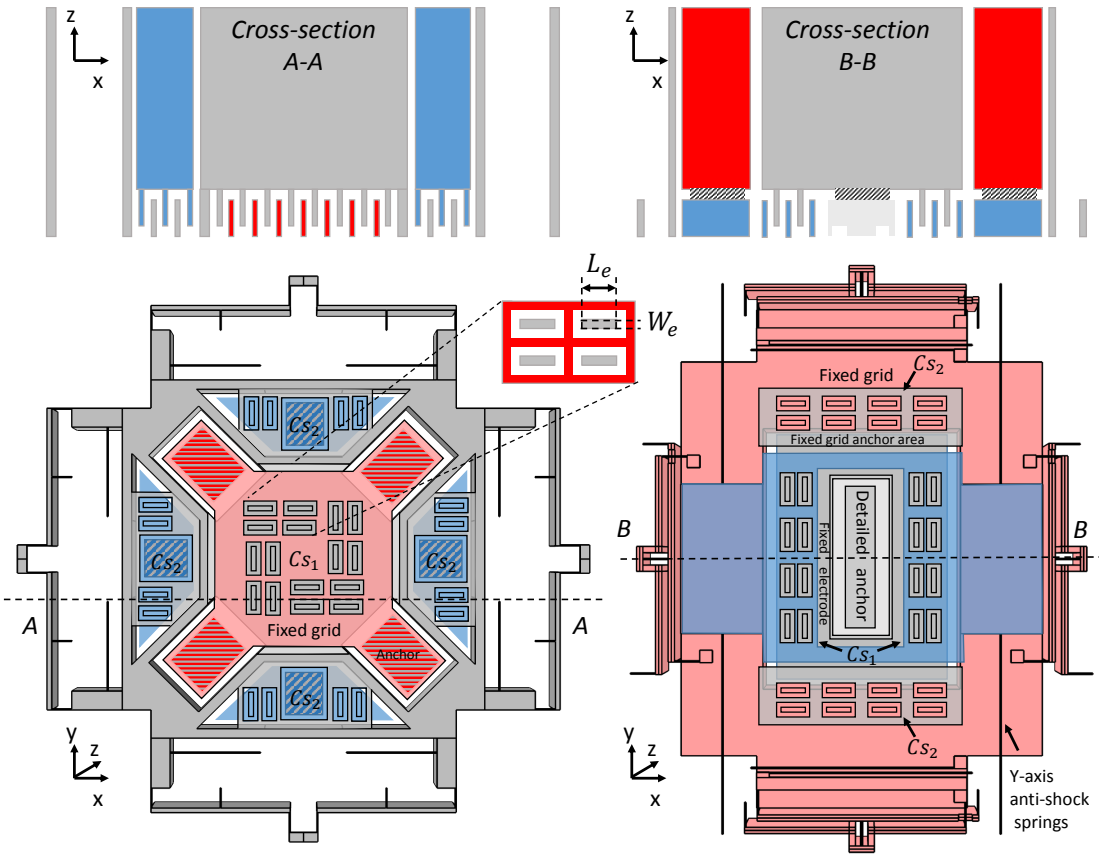


Figure 2.21: *Schematic cross-section and bottom view of the M-Z and the S-Z architectures with highlighted electrodes areas. Both structures have a differential readout, polarization of the fixed elements is obtained by suspended connections not represented here. M-Z) The first sensing capacitor (Cs1) is made of a fixed grid (red) implemented in the thin layer, suspended by four anchor points below the thick layer and interdigitated with comb-fingers directly connected to the mass. The second capacitor (Cs2) is made of fixed thick-layer structures (blue) having vertical comb-fingers interdigitated with moving grids attached to the mass. S-Z) In the center, fixed fingers directly connected to the thick layer are interdigitated with a movable grid attached to the proof mass (Cs1); in the external region two suspended grids, fixed to the central thick layer, are interdigitated with comb-fingers directly connected to the proof mass (Cs2). The two mass portions are isolated by an oxide layer and independently biased.*

Parameter	Symbol	M-Z	S-Z	Unit
Number of flexural springs	N_f	8	8	
Young Modulus PolySi	E_p	160	160	GPa
Thickness of flexural spring	t_f	2	2	μm
Length of flexural springs	l_f	96	161.1	μm
Width of flexural springs	w_f	0.7	1	μm
Number of torsional spring per arm	N_t	3	3	
Number of rigid arms	N_a	8	8	
Length of lever	L_l	72.5	176.4	μm
Beta coefficient	β_t	0.304	0.229/0.187	
Thickness of torsional springs	t_t	5	2	μm
Length of torsional springs	l_t	21	20	μm
Width of lateral torsional springs	w_{lt}	0.7	1	μm
Width of 1st central torsional spring	w_{ct1}	0.7	2.8	μm
Width of 2nd central torsional spring	w_{ct2}	0.7	1	μm
Poisson ratio of PolySi	ν	0.22	0.22	
Flexural stiffness	k_f	8.36	2.45	N/m
Torsional stiffness	k_{at}	7.43	4.61	N/m
Mass	m	10.53e-9	9.67e-9	Kg
Thick layer thickness	T	50	50	μm
Analytical resonance frequency	f_{0a}	6164	4300	Hz
FEM resonance frequency	f_{0th}	6266	4317	Hz
Number of comb-fingers per electrode	N_c	1184	960	
Length of comb-finger	L_c	5	5	μm
Width of comb-finger	W_c	0.4	0.4	μm
Vertical overlap	V_{OL}	2	2	μm
Gap	g_c	0.5	0.5	μm
Fringe field coefficient	F_{fz}	1.097	1.097	
Differetial static capacitance	C_{0th}	994	806	fF
Brownian Noise (Q=1)	BN	26	23	$\mu g/\sqrt{Hz}$
Scale factor	SF	2.9	5.4	fF/g
Full Scale Range (NL=1%)	FSR	220	104	g
Dynamic Range	DR	139	133	dB
Footprint		600x600	470x470	μmxμm

Table 2.7: *Electrical and mechanical parameters of the first designed Z-axis accelerometers.*

Numerical simulations for z-axis

The linearity of the transduction process and the modal analysis have been performed using FEM simulations. Figure 2.22 shows the 3D model of a 3x3 array of comb-fingers for out-of-plane devices. The simulation procedure is similar to the one used for in-plane sensors: the position of the combs is swept in the vertical direction while keeping a constant potential between moving and fixed electrodes; at each position the electrical energy between the electrodes is measured and used to extract the capacitance value. This time only the air volume around the central comb-finger is used to extract the electrostatic energy: this way, the effect of the electric field propagating towards other part of the grid is taken into account without introducing any error related to boundary conditions of the simulation. The differential measurement is obtained by subtracting the energy measured at position $-x$ from the one computed at position x assuming symmetry between the positive and negative electrodes. The results are shown in Figure 2.23. 1% nonlinearity is reached at 70% relative displacement. This error is due to the stray capacitance between the grid and the proof mass: as the mass gets closer to the grid, the parasitic capacitance between the two elements increases, like in a standard gap variation. In the future, the linear range could be extended by increasing the oxide thickness separating the two MEMS layers.

The modal analyses of M and S devices are shown in Figure 2.24 and 2.25. The

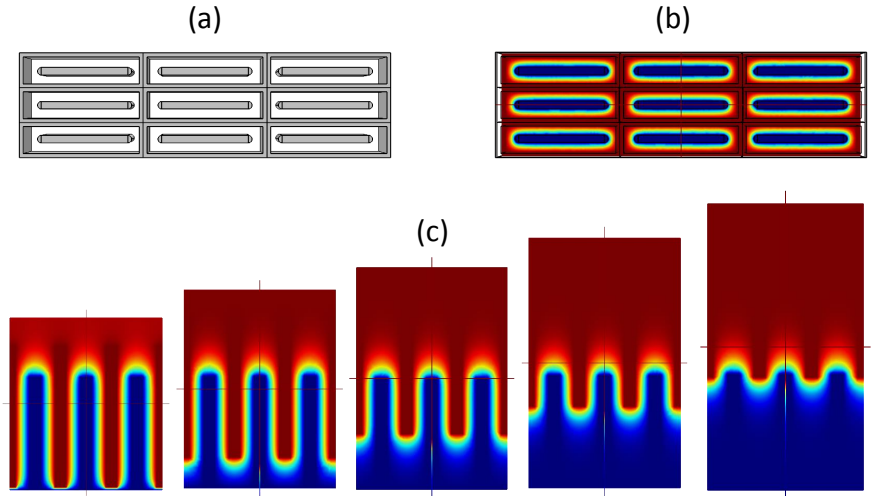


Figure 2.22: *(a) Top view of FEM model of 3x3 comb-fingers array in z-axis electrodes used to evaluate linearity and fringe fields coefficient. (b) Top view of the electric potential distribution in the array. (c) Cross-section view of electrical potential distribution between the combs for different positions. The central finger and the bottom plane are grounded while the grid is set at 1V. Only the central detection unit is used for energy computation in order to avoid error due to boundary conditions.*

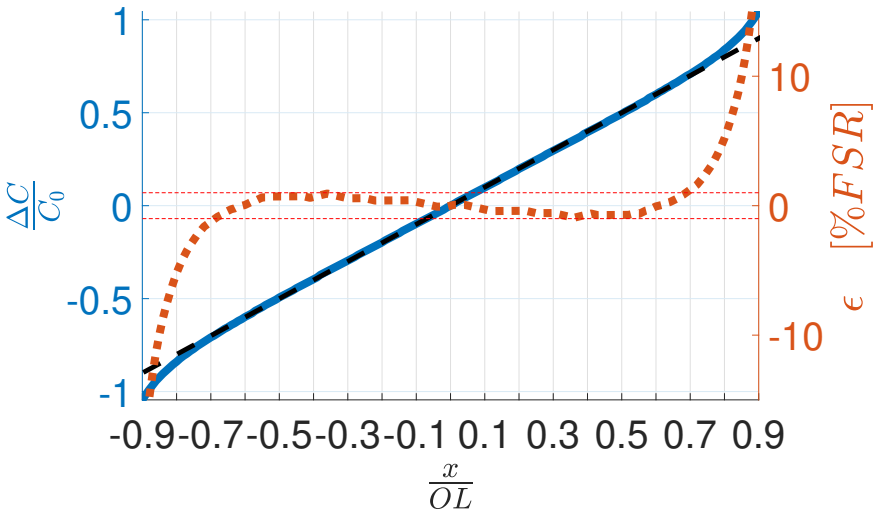


Figure 2.23: *Plot of the relative capacitive variation and related linearity error with respect to the displacement of the moving comb normalized to the initial overlap for z-axis detection system at 500nm gap. Nonlinearity greater than 1% occurs at 70% of the relative displacement due to the stray capacitance between the grid and the proof mass. The FSR is evaluated at the point of 1% nonlinearity.*

desired mode is close to the analytically computed frequency for both structures. The effectiveness of the anti-tilt system can be appreciated comparing the mode analysis presented at the beginning of the subsection (Figure 2.18) and the one of the S-Z shown here (Figure 2.25). It is the same sensor, having only flexural springs in the first case and both springs system in the second. The tilt mode frequency changes from 3.8kHz to 11.3kHz. The x-axis and y-axis tilt modes are perfectly matched for the M-Z structure thanks to the high symmetry of the architecture. The modes matching of the S device is achieved within 200Hz with fine tuning of the central springs width in order to balance the slight asymmetry of the sensor. Higher modes are related to motion of the rigid arms and are found at respectively 118kHz and 43kHz for the M and S structures at least a factor 10 higher than the desired resonance frequency.

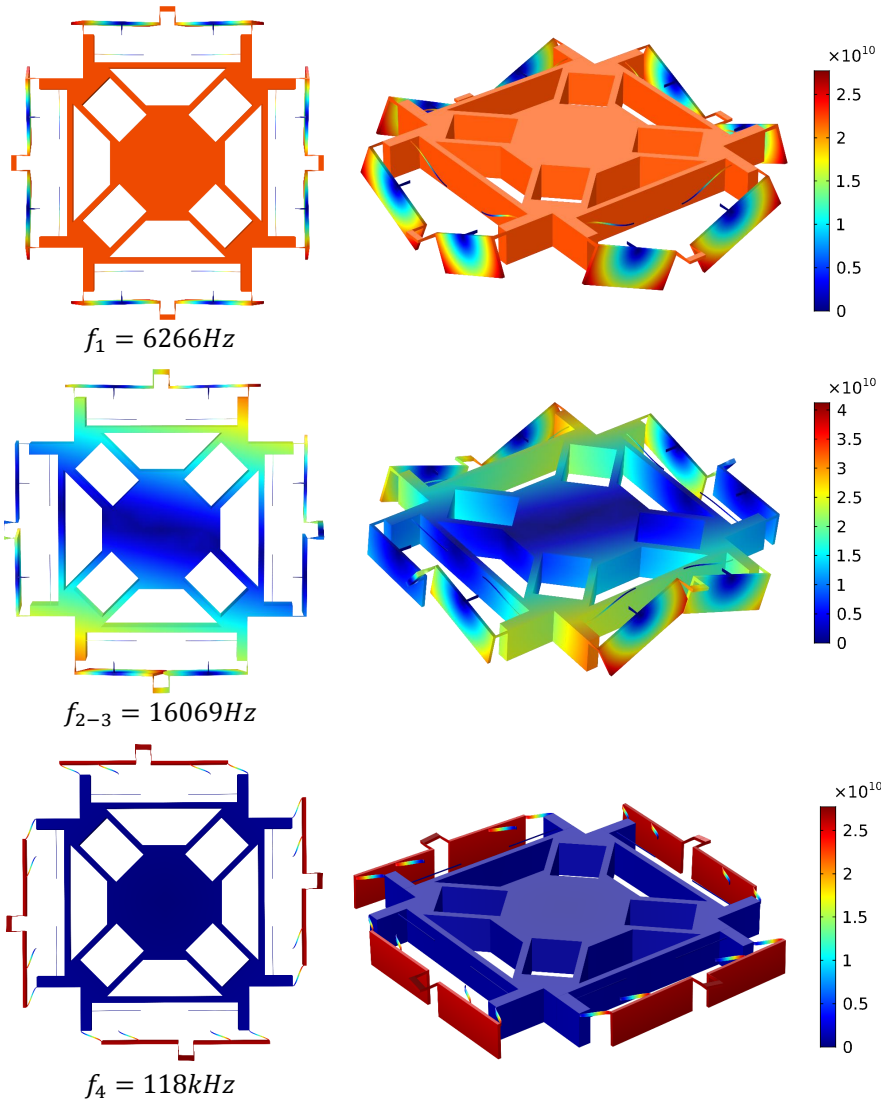


Figure 2.24: *Different view-points of the modal analysis results for the M-Z device. The desired mode matches analytical prediction within a few percent. The tilting modes are more than a factor two higher than the principal mode thanks to the anti-tilt system. Undesired modes related to the rigid arms are found at 118kHz.*

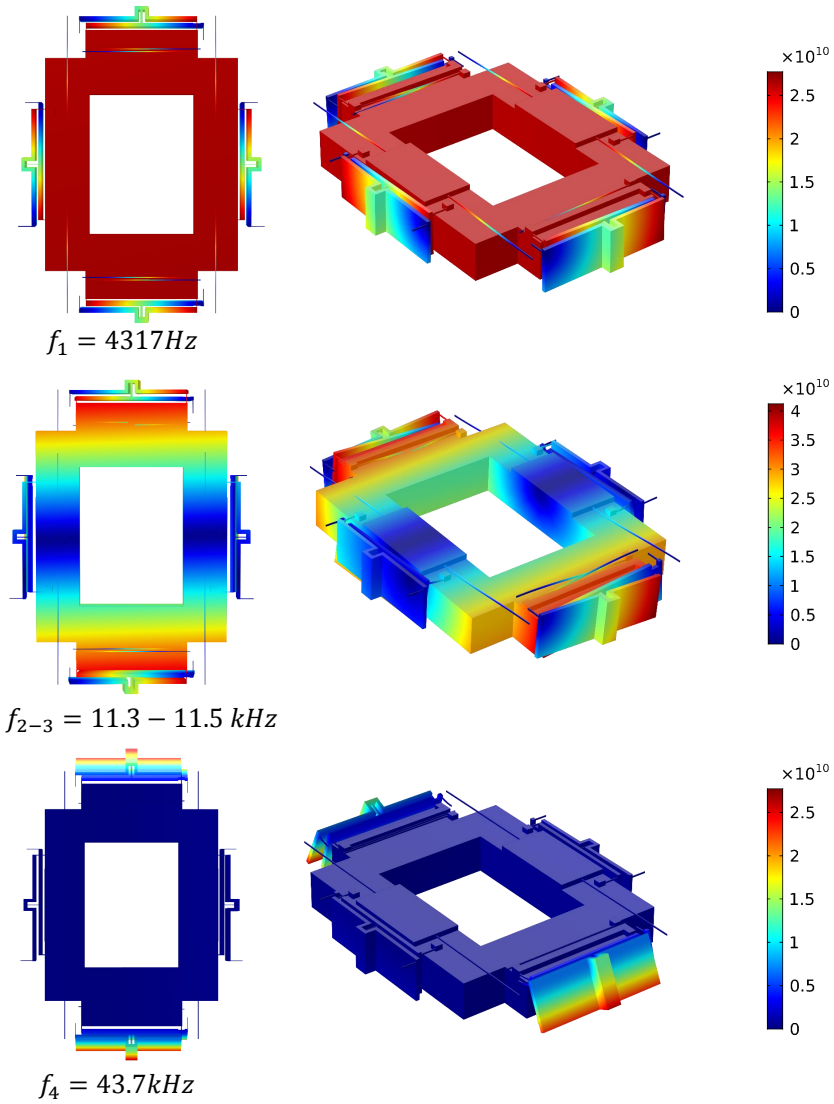


Figure 2.25: *Modal analysis results for the S-Z device. Again, the mode of interest mode is in line with analytical prediction. The tilt mode frequency changes from 3.8kHz of previous structure to 11.3kHz. The two tilting modes are matched by tuning the width of the central springs, compensating the asymmetry of the structure. High frequency modes related to the rigid arms are a factor ten higher than the desired mode.*

2.3 Second chapter conclusion

In this chapter, the fabrication process and its critical aspects have been addressed. The new fabrication allows the combination of a thick inertial layer (50-100μm thick) with sub-micrometric capacitive detection units. The integration of 3-axis accelerometer on a 100μm process is not possible due to problems related to the excessive notching of the DRIE, which limits the z-axis sensors. After, the mechanical and electrostatic design-flow of in-plane and out-of-plane devices is addressed. Both analytical and numerical simulations are used to study the mechanical response and the linearity of the capacitive transduction. For both types of sensors, surface variation is shown to be the best detection technique. Such technique requires pure out-of-plane translation for z-axis sensors. For this reason, z-devices feature an innovative anti-tilt spring system together with standard flexural springs. According to numerical simulations, the anti-tilt structures increase the spurious mode frequency by a factor 3 (11.3kHz/3.8kHz)), strongly reducing the problems related to cross-axis accelerations.
Tables 2.5 and 2.7 present all the parameters of the studied devices and the expected performance. In-plane devices are expected to reach Brownian noise floor of few $\mu g/\sqrt{Hz}$ together with mechanical stiffness of 28 N/m and large resonance frequency (4.9kHz) within a compact size (400x600 μm^2).
Out-of-plane sensors are expected to reach Brownian noise floor slightly higher than in-plane devices (20-30 $\mu g/\sqrt{Hz}$) due to the smaller inertial layer thickness ($100\mu m \rightarrow 50\mu m$). Yet, they show large resonance frequency and large stiffness (4-6kHz, 6-15 N/m) within a even smaller footprint (470x470 μm^2). Before addressing the results section in Chapter 4, the design and implementation of the ultra-low noise readout circuit are presented in Chapter 3.

Chapter 3

Electronic readout circuit

In this chapter the development of the electronic readout circuit used for characterization of the fabricated accelerometers is discussed. First an overview of the possible readout architectures is given, followed by a comparison of different types of analog front-end solutions. Finally, numerical simulations of the circuit operation and stability are addressed.

3.1 Capacitive readout

The need for measuring the value of a capacitor has been present in almost any electronic application long before the introduction of MEMS technologies. Therefore, several detection methods have been developed throughout the years. The MEMS community has taken advantage of this prior knowledge. The design choices made in this work regarding the readout circuit are presented below:

1. **Closed loop vs open loop.** The first main distinction in sensing techniques is the presence or the absence of a feedback path. Open loop architectures correspond to the situation described in the previous chapters: the capacitive variation induced by the acceleration signal is sensed by a front-end amplifier and provided as output signal without any effect on the device displacement [51, 52]. On the other hand, in closed loop architectures, the device motion is sensed by a front-end and fed-back to the device in order to either prevent its displacement (force rebalanced) [4, 53, 54, 55] or to reduce the electrostatic effects (charge rebalanced) [56, 57]. Usually, closed loop architectures allow increased linear range, signal bandwidth and offset stability at the cost of increased circuit complexity and power consumption.

2. **Discrete time vs continuous time.** Most integrated circuits for capacitive detection operate with discrete time readout in order to ease the interfacing with the digital domain and keep low power consumption. The

main architecture used in this case is the switched capacitors charge amplifier [58, 59, 60]. In terms of resolution, this solution does not offer any performance improvement with respect to a continuous time circuit, instead it could suffer from additional noise sources [61]. Most readout techniques with analog output operate in the continuous-time domain [51, 52, 54, 55]. This solution offers good resolution and high versatility and it can be implemented with discrete components.

3. **Voltage readout vs current readout:** finally a distinction should be made between voltage sensing or current/charge sensing. The first detection method consists in setting the sensing capacitance of the device in a full or half-bridge configuration polarized by an AC voltage source (Figure 3.1.*a*). The capacitive change is detected by measuring the voltage variation at the bridge output [62, 51]. Most of MEMS accelerometers do not have four independent sensing capacitors and cannot implement a full bridge configuration. For this reason reference capacitors are needed and trimming of the readout interface is required. Moreover any stray capacitance referring to the central node of the bridge has an impact on the readout transfer function and needs to be properly compensated for.
   Also in current sensing the capacitors are set in half-bridge configuration polarized by an AC voltage source. This time, however, the central node of the bridge is set at low impedance by the virtual ground of the front-end amplifier (Figure 3.1.*b*). The charge generated by the capacitive variation flows into the current to voltage amplifier which provides an output signal proportional to the capacitive change. As later explained in detailed, this solution does not suffer from the parasitic capacitance referring to the central node of the bridge and does not require reference capacitors [55, 52].

Each technique offering advantages and drawbacks, the choice of the best readout scheme depends on the required application and on the underlying MEMS technology. The electronics developed in this work is mostly for characterization purposes, therefore the following choices were made: (i) implementing the circuit using discrete components. This allows a more versatile electronics and ease in the debugging process. An ASIC is time consuming and less suited for characterization purposes. (ii) Use of an open-loop architecture. One of the key features of the new fabrication concept is the enhanced dynamic range of the sensors, achievable without any need of feedback compensation. Using open loop readout reduces the complexity and takes full advantage of the device characteristics. (iii) Work in the continuous time domain. Switched capacitor is not a suitable solution when working with discrete components and the increase of circuit complexity is not justified by better performance. (iv) Finally, a current readout technique was chosen. As explained in the above paragraph, this solution is insensitive to stray capacitance and does not require trimming of reference

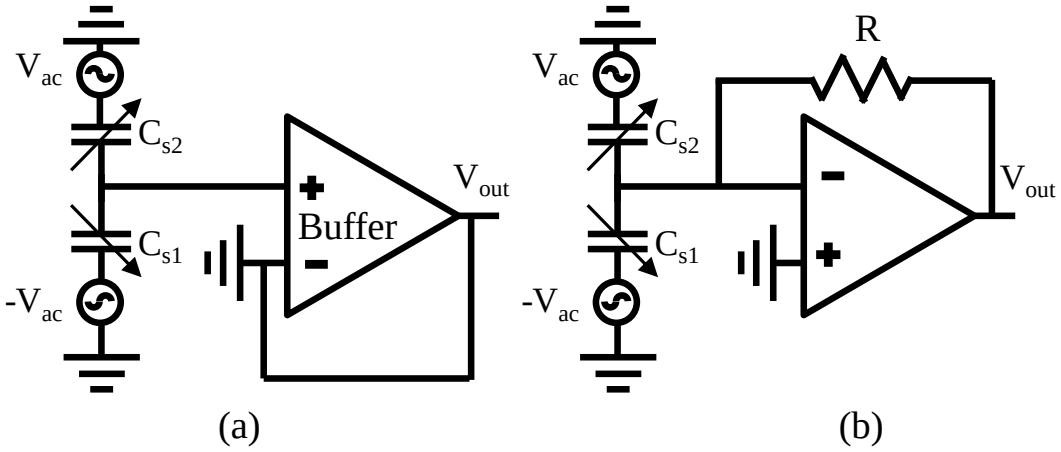


Figure 3.1: *Schematic view of of: (a) the voltage readout, (b) and current readout for capacitive detection. In voltage readout, the output of the half-bridge is connected to high-impedance node. The voltage change due to the bridge unbalance is reported at the output. In current readout, the bridge output is connected to a low-impedance node. This time the voltage is kept at virtual ground and the current flows into the feedback path of the current to voltage circuit.*

accelerometers.
In the following section, different current sensing architectures are discussed.

3.2 Current sensing

In current sensing, the MEMS capacitance is place between an AC voltage source and the low impedance node of the circuit which collects the current produced by the polarization of the capacitor (Figure 3.2). In static operation, the only source of current is the variation of the amplitude of the polarization voltage ($\frac{\partial V_m(t)}{\partial t}$). Yet, when the value of the capacitance changes with time, as in the accelerometer case, a second source of current proportional to the capacitive variation appears ($\frac{\partial C_s(t)}{\partial t}$). This source of current is undesired and should be controlled. The complete current equation that takes into account both terms is the following:

$$\begin{aligned} i_{MEMS} = \frac{\partial(C_s(t)V_m(t))}{\partial t} &= \frac{\partial C_s(t)}{\partial t}\overbrace{V_m(t)}^{V_m\,sin(\omega_m t)} + \frac{\partial V_m(t)}{\partial t}\overbrace{C_s(t)}^{\Delta C sin(\omega_a t)} \\ &= \Delta C V_m[\omega_a cos(\omega_a t)sin(\omega_m t) + \omega_m sin(\omega_a t)cos(\omega_m t)] \end{aligned} \tag{3.1}$$

The equation is written assuming a sinusoidal capacitive variation (ΔC) at frequency ω_a. The obtained current is a high-frequency signal. In order to recover

the useful information, the current is usually demodulated with two reference signals at ω_m and filtered in order to eliminate high-frequency modulation products. After demodulation, the in-phase ($\phi = 0$) and in-quadrature ($\phi = \pi/2$) components of the current can be written as follows:

$$\begin{aligned} i_{(\phi=0)} &= \Delta C V_m[\omega_a cos(\omega_a t)sin(\omega_m t) + \omega_m sin(\omega_a t)cos(\omega_m t)]sin(\omega_m t) \\ &\xrightarrow{\text{after LPF}} \frac{\Delta C V_m}{2}\omega_a cos(\omega_a t) \\ i_{(\phi=\pi/2)} &= \Delta C V_m[\omega_a cos(\omega_a t)sin(\omega_m t) + \omega_m sin(\omega_a t)cos(\omega_m t)]cos(\omega_m t) \\ &\xrightarrow{\text{after LPF}} \frac{\Delta C V_m}{2}\omega_m sin(\omega_a t) \end{aligned} \tag{3.2}$$

The two sources of current have a 90 ° phase difference, therefore both signals can be easily separated. In the case of a phase error between the modulating and demodulating signal, part of the in-phase current could be read at the output. It is therefore useful to use a modulating signal at much higher frequency than the maximum acceleration signal ($\omega_m >> \omega_a$). This way, the in-phase component, proportional to ω_a, is negligible with respect to the useful in-quadrature component proportional to ω_m even in the case of a demodulation error.
Two different solutions to sense the current signal can now be discussed: trans-impedance amplifier and charge amplifier.

3.2.1 Trans-impedance amplifier

Figure 3.2 shows a schematic view of a trans-impedance architecture. The current generated by the polarization of the capacitance flows in the feedback path and is amplified by the impedance Z_f. In the trans-impedance readout, at the working frequency, such impedance is dominated by the resistor R_f. The signal transfer function ($T_T(\omega)$) expressed in terms of capacitance to voltage is the following:

$$T_T(j\omega) = \frac{V_{out}(j\omega)}{C_s} = j\omega V_m Z_f = j\omega V_m \frac{R_f}{1 + j\omega R_f C_f} \tag{3.3}$$

In order to understand the limitations of this architecture, it is necessary to study all the noise contributions reported in schematic of Figure 3.2. The input-referred noise expressed in terms of capacitance noise density can be obtained as follows:

$$\begin{aligned} S_{in}(j\omega) = \frac{S_{out}(j\omega)}{|T_T(j\omega)|^2} &= \frac{S_v \left|1 + j\omega(C_p + C_s)Z_f\right|^2 + S_i|Z_f|^2 + \frac{4k_bT}{R_f}\left|Z_f\right|^2}{\left|j\omega\, V_m\, Z_f\right|^2} \\ &= \underbrace{\frac{S_v}{V_m^2}\left|\frac{1}{j\omega R_f} + C_f + C_p + C_s\right|^2}_{1} + \underbrace{\frac{S_i}{\left|j\omega\, V_m\right|^2}}_{2} + \underbrace{\frac{4k_bT}{R_f}\frac{1}{\left|j\omega\, V_m\right|^2}}_{3} \end{aligned} \tag{3.4}$$

There are three different contributions. All of them can be reduced by increasing the amplitude of the modulation voltage *i.e.* amplifying the useful signal.

1. The first contribution is related to input-referred voltage noise of the amplifier. This term is proportional to all the capacitors referring to the input node of the amplifier and to a term related to feedback resistor. For a given input-referred noise, this source of noise can be minimized by reducing the stray capacitance referring to the input node of the amplifier.

2. The second contribution is related to the input current noise of the amplifier. It can be minimized by properly choosing an amplifier with low current noise and by working at high frequency.

3. Finally, the third term is due to the Johnson noise of the feedback resistor. Increasing the value of the resistor or working at high frequency helps reducing this noise source.

To understand how the three sources contribute to the total noise of the circuit, numerical simulations using typical values of commercial discrete components are performed. The input-referred noise sources are set equal to $4nV/\sqrt{Hz}$ and $2.5fA/\sqrt{Hz}$. The feedback capacitance is set to 500fF. Reducing the value of

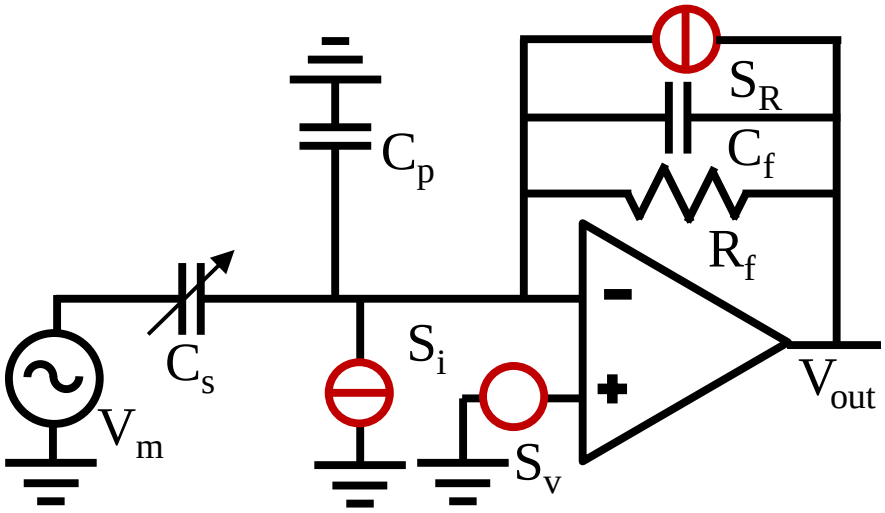


Figure 3.2: *Schematic view of a generic current to voltage architecture for capacitive detection. The parasitic capacitance referring to the input node of the front-end amplifiers is shown (C_p). The feedback path presents a feedback resistor (R_f) together with the feedback capacitance (C_f). In the case of a trans-impedance readout the feedback path is dominated by the resistor impedance. Three noise sources are present: input-referred voltage noise (S_v), input-referred current noise (S_i) and the Johnson noise associated to the feedback resistor (S_r). The sensing capacitor (C_s) is polarized by an AC voltage source (V_m).*

this parameter is usually not possible when using discrete components which suffers from stray capacitors in the feedback path. Input node stray capacitance and device one were assumed to be equal to 10pF and 500fF respectively. Modulation voltage is set to 1V. Finally, the only degree of freedom in the design remains the feedback resistor. In order to chose its value, the following conditions are set:

$$\begin{cases} \omega_m = \frac{1}{10}\frac{1}{C_f R_f} \\ \frac{S_v}{V_m^2}\left|\frac{1}{j\omega_m R_f} + C_f + C_p + C_s\right|^2 = \frac{4k_bT}{R_f}\frac{1}{|j\omega_m V_m|^2} \end{cases} \rightarrow \begin{cases} \omega_m = \frac{1}{10}\frac{1}{C_f R_f} \\ R_f = \frac{S_v}{4k_bT}\left[1 + \frac{(C_f+C_p+C_s)^2}{(10C_f)^2}\right] \end{cases} \tag{3.5}$$

The first condition requires that the frequency of the modulation voltage (ω_m) should be an order of magnitude smaller than the cut-off frequency of the feedback RC filter. This way the stage works as a pure trans-impedance amplifier. The second condition sets that the term related to the voltage noise of Equation 3.4 and the one due to the resistor noise should be equal. The value of the feedback resistor that satisfies both conditions is $5.6k\Omega$.
From the plot in Figure 3.3, it can be seen that the equality between the two noise sources is obtained at 5.6 MHz. This means that in order to be limited by only voltage noise, even higher frequency is necessary. Working at such high frequency can become challenging and adds complexity to the circuit design. In order to relax the working frequency constraint, another current readout technique should

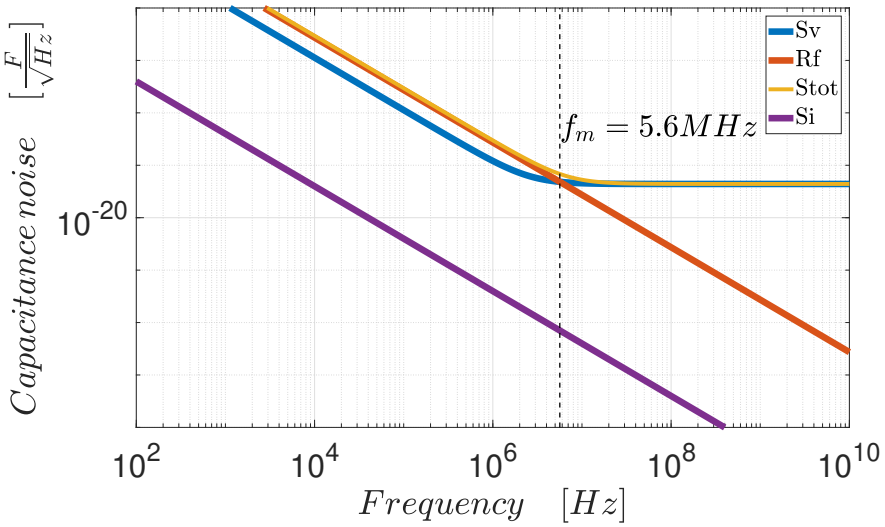


Figure 3.3: *Numerical simulation of the three main noise sources in the trans-impedance circuit. The impact of the current sources (red,purple) decreases with frequency, while the term related to the voltage noise (blue) remains the intrinsic detection limit. In order to be voltage-noise limited, the working frequency should be higher than 5.6MHz.*

therefore be considered.

3.2.2 Charge amplifier

The second solution to sense the signal current is the charge amplifier stage. The circuit is identical to the one shown in Figure 3.2. However, the feedback path is now dominated at the working frequency by the capacitor impedance and not by the resistor one. Before addressing the noise analysis, a time domain study is performed in order to evaluate the effects of the current integration performed by the stage. The time-dependent output of this front-end can be obtained by integrating the current defined in Equation 3.1 into the feedback capacitor:

$$V_{out} = \frac{1}{C_f}\int \frac{i_{MEMS}}{\partial t}dt = \frac{1}{C_f}\int \frac{\partial(C_s(t)V_m(t))}{\partial t}dt = \frac{C_s(t)V_m(t)}{C_f} \tag{3.6}$$

Also in this case, the output signal can be demodulated and filtered with a low-pass filter:

$$\begin{aligned} V_{(\phi=0)} &= \left[\frac{\Delta C sin(\omega_a t)V_m sin(\omega_m t)}{C_f}\right] sin(\omega_m t) \xrightarrow{\text{after LPF}} \frac{\Delta C sin(\omega_a t)V_m}{2} \\ V_{(\phi=\pi/2)} &= \left[\frac{\Delta C sin(\omega_a t)V_m sin(\omega_m t)}{C_f}\right] cos(\omega_m t) \xrightarrow{\text{after LPF}} 0 \end{aligned} \tag{3.7}$$

This time no quadrature signal is present. Therefore demodulation error due to a phase difference would only reduce the amplitude of the demodulated signal. Yet, the modulation frequency should be higher than the 1/f noise of the readout circuit, in order to guarantee the best noise performance.
Now, the time domain study can be addressed. The transfer function of the charge amplifier and its input-referred noise are identical to the one seen before in Equations 3.3 and 3.4. However this time the circuit is working after the cut-off frequency of the RC filter, meaning that the value of the feedback resistor can be arbitrary chosen in order to minimize the related noise.
Figure 3.4 shows the input-referred noise contributions in the case of charge amplifier having the same characteristics of the trans-impedance scheme but with $R_f = 1G\Omega$ and $C_f = 1pF$. The current noise of the resistor equals the voltage noise already at 13kHz, while working at 100kHz allows reaching the intrinsic limit of the circuit *i.e.* the voltage noise term.
In conclusion, in order to reach the detection limit, the trans-impedance architecture requires a modulation frequency of more than 5MHz. This implies complex circuit design and high-frequency adaptation. On the other hand, charge amplifiers can take advantage of large feedback resistor and reach the best noise

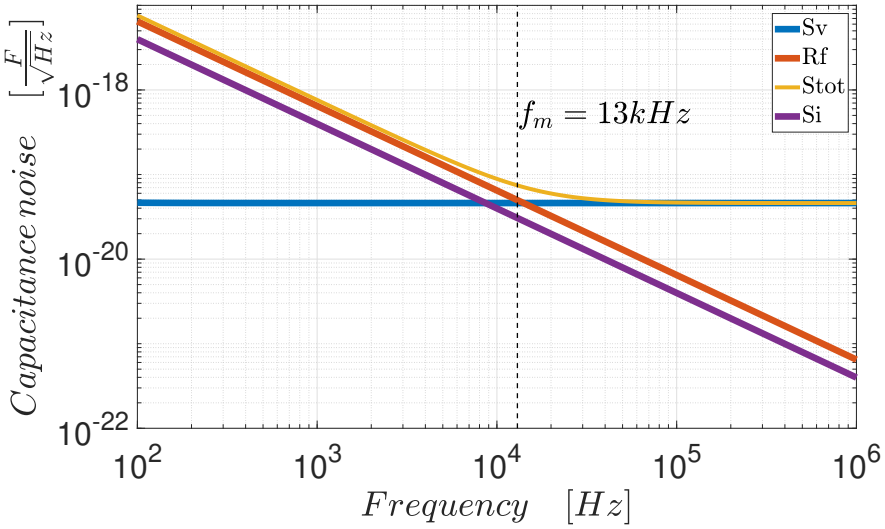


Figure 3.4: *Input-referred noise expressed in terms of $F/\sqrt{Hz}$ according to matlab model of the charge amplifier. The input-referred noise of the operational amplifier becomes the dominant source of noise already around 20kHz thanks to the increased feedback resistor value.*

performance already in the hundreds of kHz range. It is therefore the most effective solution for the readout circuit. Before addressing the stability study and circuit simulation, a few further considerations are required.

3.2.3 Differential architectures

All considerations presented so far took into account only a single branch of the detection system. However, the designed accelerometers have two electrodes of different polarity and need therefore a differential readout. Two possible configurations are available: (i) a fully differential configuration (ii) or two identical branches with single-ended topology.

Fully differential architecture

Figure 3.5 shows a scheme of a fully differential charge amplifier. This circuit usually offers good Common Mode Rejection Ratio (CMRR) having the two branches implemented on a single integrated amplifier. For the sake of simplicity, the circuit is assumed symmetric with respect to the x axis, exception made for the two stray capacitance referring to the input nodes. As a matter of fact, even designing the circuit and the connections between the device and the front end as symmetric as possible, the parasitic source on the two branches can be uneven and difficult to characterize.
In order to obtain the circuit capacitance to voltage gain, it is first necessary to

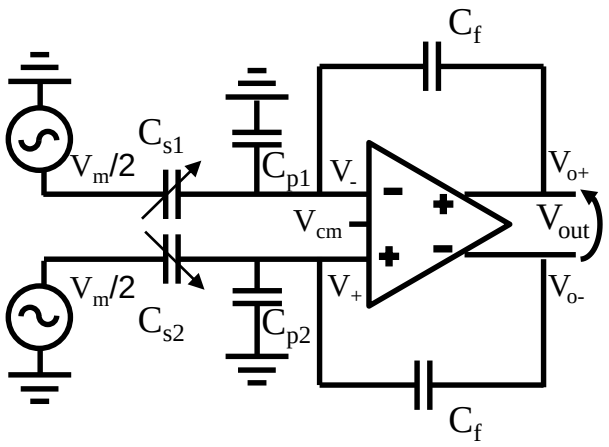


Figure 3.5: *Schematic view of a fully differential charge amplifier. The voltage generator has been split in two identical sources of halved amplitude. The circuit is considered symmetric exception made for the parasitic capacitance.*

write the equations that links the output and input nodes of the circuit:

$$V_{out}(j\omega) = V_{o+} - V_{o-} = A(j\omega)(V_+ - V_-) \qquad V_{ocm} = \frac{V_{o+} + V_{o-}}{2} \tag{3.8}$$

Where $A(j\omega)$ is the open loop gain of the amplifier and V_{ocm} is the output common mode of the circuit. Such voltage is kept at the value set from the V_{cm} node by the internal common feedback circuit of the amplifier. The second step consists in rewriting the voltage at the input nodes in terms of the modulation and output voltage.

$$\begin{aligned} V_- &= \frac{C_f}{C_{p1} + C_{s1} + C_f} V_{o+} + \frac{C_{s1}}{C_{p1} + C_{s1} + C_f} \frac{V_m}{2} = \alpha_1 V_{o+} + \beta_1 \frac{V_m}{2} \\ V_+ &= \frac{C_f}{C_{p2} + C_{s2} + C_f} V_{o-} + \frac{C_{s2}}{C_{p2} + C_{s2} + C_f} \frac{V_m}{2} = \alpha_2 V_{o-} + \beta_2 \frac{V_m}{2} \end{aligned} \tag{3.9}$$

By combining the above equation with those written in 3.8, the transfer func-

tion of the circuit can be obtained:

$$\begin{aligned}
&\overbrace{V_{o+} - V_{o-}}^{V_{out}} = A(j\omega)\overbrace{\left[\alpha_2 V_{o-} - \alpha_1 V_{o+} + (\beta_2 - \beta_1)\frac{V_m}{2}\right]}^{V_+ - V_-} \\
&\rightarrow V_{o+} - \overbrace{(2V_{ocm} - V_{o+})}^{V_{o-}} = A(j\omega)\left[\alpha_2 \overbrace{(2V_{ocm} - V_{o+})}^{V_{o-}} - \alpha_1 V_{o+} + (\beta_2 - \beta_1)\frac{V_m}{2}\right] \\
&\rightarrow V_{o+} = \frac{2V_{ocm}A(j\omega)(\alpha_2)}{A(j\omega)(\alpha_2 + \alpha_1)(1 + \frac{2}{A(jw)(\alpha_1+\alpha_2)})} + \frac{\frac{V_m}{2}A(j\omega)(\beta_2 - \beta_1)}{A(j\omega)(\alpha_2 + \alpha_1)(1 + \frac{2}{A(jw)(\alpha_1+\alpha_2)})} \\
&\approx 2V_{ocm}\frac{\alpha_2}{\alpha_2 + \alpha_1} + \frac{V_m}{2}\frac{\beta_2 - \beta_1}{\alpha_2 + \alpha_1}
\end{aligned} \tag{3.10}$$

Where the open loop gain of the circuit was assumed to be infinite for the sake of simplicity. The same equation can be written for the negative output node (V_{o-}). Combining both equations, the differential output equation is:

$$V_{out} = V_m\frac{\beta_2 - \beta_1}{\alpha_2 + \alpha_1} + 2V_{ocm}\frac{\alpha_2 - \alpha_1}{\alpha_2 + \alpha_1} \tag{3.11}$$

The output equation presents two terms. A common mode contribution which can be nulled by setting V_{ocm} equal to zero and a contribution related to the modulation voltage which carries the signal information. In an ideal system, the parasitic referring to the input nodes are equal and the two sensing capacitors are assumed to be balanced ($\Delta C << C_s$). Therefore the equation takes the following form:

$$V_{out} = V_m\frac{2\Delta C}{C_f} \tag{3.12}$$

where ΔC is the capacitive variation due to an external acceleration induced on each sensing capacitance. However, it can be noticed how the terms β and α depend on any asymmetry of the circuit. Therefore the real transfer function of the fully differential stage should take into account any asymmetry of the parasitic branches, which could also change due to change in the setup. For instance change of the stray capacitance of the carrier holding the device. Therefore, while this architecture usually offers good CMRR, it also suffers from any asymmetry in the two branches, making it less suitable for a discrete components implementation.

Double single ended readout

Figure 3.6 presents a differential architecture implemented using two single ended readout branches. This time the two branches are independent from each other.

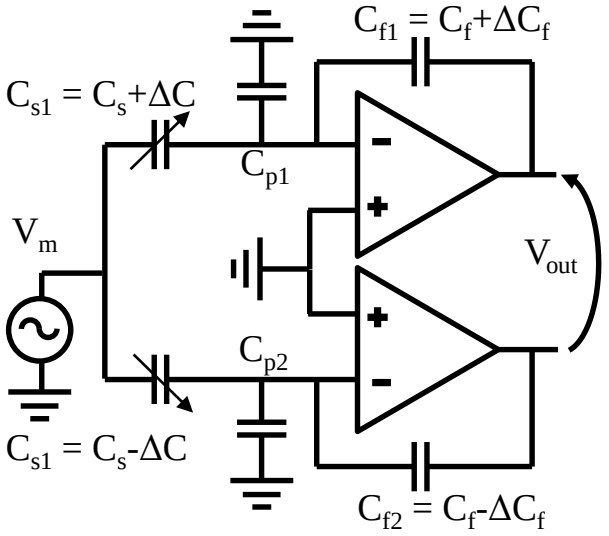


Figure 3.6: *Schematic view of a double single ended differential charge amplifier. Potential asymmetry in both the stray capacitance and feedback path are considered.*

Assuming the open loop gain of the operational amplifier to be infinite, the input-output relation takes the following form:

$$\begin{aligned} V_{out} = V_m\frac{C_{s1}}{C_f 1} - V_m\frac{C_{s2}}{C_{f2}} = V_m\frac{C_s+\Delta C}{C_f+\Delta C_f} - V_m\frac{C_s-\Delta C}{C_f-\Delta C_f} \\ = V_m\frac{\Delta C_f C_s}{C_f^2-\Delta C_f^2} + V_m\frac{2\Delta C C_f}{C_f^2-\Delta C_f^2} \approx V_m\frac{2\Delta C}{C_f} \end{aligned} \tag{3.13}$$

In the assumption of having perfectly matched feedback paths, the transfer function takes the same form seen for the ideal fully differential architecture. In the case of asymmetry in the two branches two considerations can be made: (i) to first order, the stray capacitance is not present in the equations and does not cause a change in the circuit transfer function; (ii) the unbalance in the feedback path causes an offset term to appear, however the capacitance to voltage gain remains constant and can be characterized using a reference accelerometer or a known ΔC. Therefore, this architecture offers a simpler and more solid solution for capacitive sensing at the cost of large power consumption and possibly less CMRR. Neither large common mode signal nor power constraint is present during testing, therefore this topology is most suited for the device characterization.

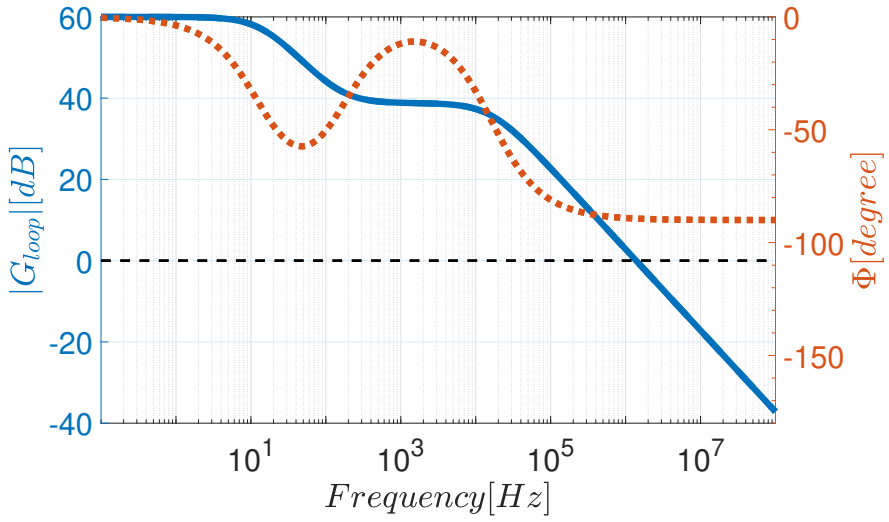


Figure 3.7: *Bode plot of the circuit G_{loop}. The phase shift for $G_{loop} = 1$ is equal to 90° ensuring circuit stability. The singularities of the feedback path cancel each other out and are well below the internal pole of the amplifier.*

3.3 Circuit stability and numerical simulations

3.3.1 Circuit stability and closed loop pole

Knowing the readout technique, the circuit stability can be addressed. To this end, the closed loop gain ($G_{loop}(j\omega)$) of the circuit has to be calculated. All the computations refer to a single branch of the circuit. Thanks to the double single-ended topology the behavior of the two branches is identical and independent. The closed loop gain (G_{loop}) of the circuit can be calculated starting from the negative input node of the operational amplifier.

$$G_{loop}(j\omega) = -\frac{A_0}{1+j\omega\tau_0}\frac{1+j\omega R_f C_f}{1+j\omega R_f(C_f+C_s+C_p)} \tag{3.14}$$

where A_0 is the open loop gain of the operational amplifier and τ_0 is the time constant of its internal pole. The G_{loop} has two poles and a zero. The circuit stability is guaranteed if the phase shift for $G_{loop} = 1$ is smaller than 180 degrees *i.e.* if at least the effect of one of the two poles has been compensated by the zero. This condition can be easily achieved by using a large feedback resistor, lowering the frequency of the singularities related to the feedback paths below the internal pole frequency.

Figure 3.7 shows the Bode plot of the closed loop gain. The open loop gain of the amplifier is set equal to 60dB while the internal pole is set to 100kHz. All the other terms are identical to the one used for noise modeling in subsection 3.2.2 (R_f=1GΩ,$C_f = 1pF$,$C_p = 10pF$,$C_s = 500fF$). The phase margin is greater than 90 degrees, ensuring circuit stability. The closed-loop pole of the circuit can be

estimated by evaluating the frequency at which the G_{loop} crosses the 0 dB line. This point can be found from equation 3.14:

$$f_{pCL} = \frac{A_0}{\tau_0}\frac{C_f}{C_{tot}} = GBWP\frac{C_f}{C_{tot}} \tag{3.15}$$

The closed loop pole frequency depends on the GBWP (gain-bandwidth product) of the amplifier and on the ratio between the feedback capacitor and the total capacitance referring to the input node. This aspect sets a trade-off between the best noise performance and the bandwidth of the stage. Minimizing the feedback capacitor to amplify the signal and reduce the noise of the subsequent stages is allowed until the closed loop pole remains at much higher frequency than the working frequency. In order to find the best value for the capacitor, software simulations are performed using the complete circuit topology and are presented in the following subsection.

3.3.2 Circuit simulation

The circuit simulations have been performed using the software Multisim from National Instrument. Data are exported and plotted using Matlab. Figure 3.8 shows the schematic of the circuit in the software interface. The differential amplifier is implemented using two operational amplifiers model AD4817 from Analog Device [63]. The difference between the output signal of the two branches is performed by an Instrumentation Amplifier (INA) model AD8429 [64]. The use of

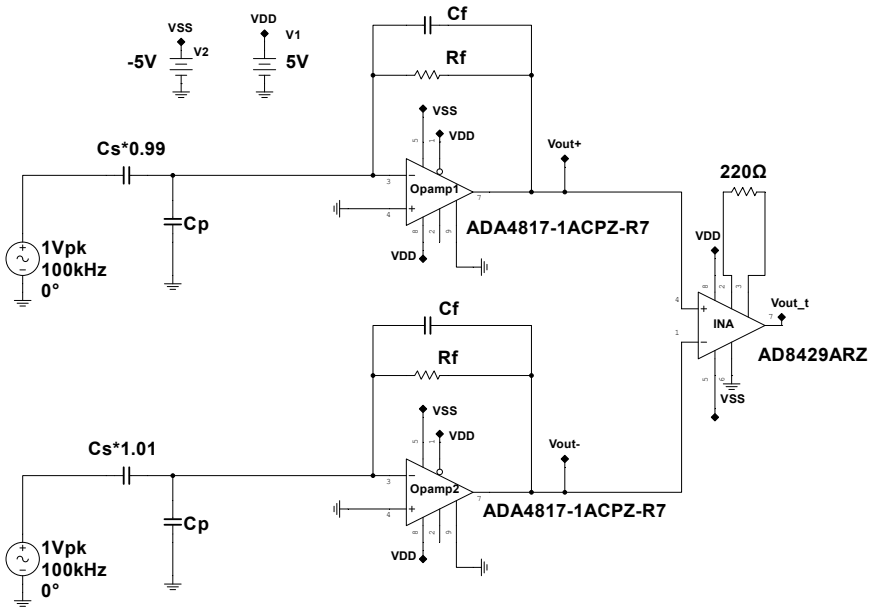
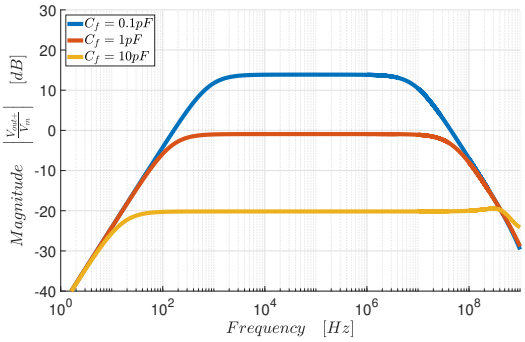
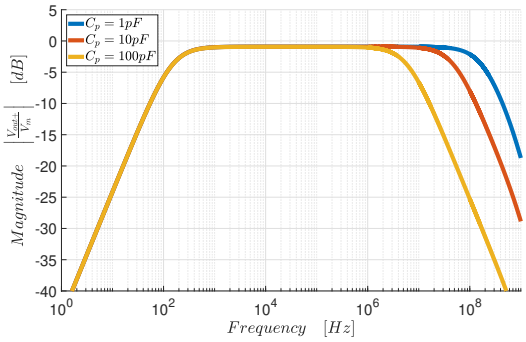


Figure 3.8: *Schematic of the complete circuit architecture used for software simulations and real PCB implementation.*

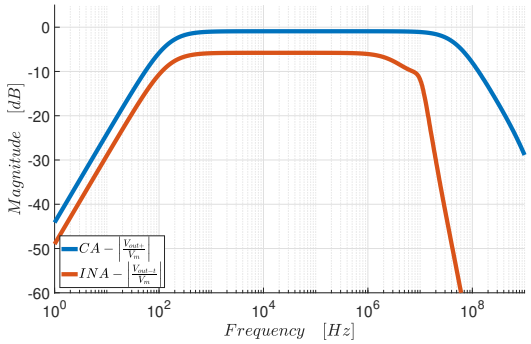
the INA is not essential, however it ensure sufficient amplification of the signal before demodulation or readout by means of an external equipment. The gain resistor of the INA sets its gain to 28.27. This value was chosen as the best trade-off between the amplifier bandwidth and its input-referred noise. Stray capacitance referring to the input nodes are added for both amplifiers. The feedback resistor are set equal to 1 $G\Omega$ as for the Matlab model. While the input-referred noise of the two amplifiers implemented in the model is equal to 1.9 $nV/\sqrt{Hz}$ (according to the data-sheet the real value should be 4 $nV/\sqrt{Hz}$ [63], the same value used in the Matlab model). The two branches are considered identical, exception made for the input capacitance (C_{in}) which is unbalanced in order to obtain a signal output during AC analysis.
The first simulation performed on the circuit is a parametric sweep of the feedback capacitance. The AC analysis of the circuit transfer function (V_{out+}/V_m) is performed for three different values of the feedback capacitor (3.9*a*). The simulation is performed on a single branch, but the same result could be obtained on both paths. The gain of the charge amplifier changes accordingly to the capacitor value. The frequency of the closed-loop pole of the circuit (f_{pCL}) lowers for smaller value of feedback capacitor in line with Equation 3.15.
Figure 3.9*b* shows the second simulation performed on the circuit model: the same AC analysis of Figure 3.9*a* has been computed for different values of stray capacitance in order to test the robustness of the circuit against parasitic. For this simulations the feedback capacitance was assumed equal to 1 pF. The result shows how the circuit gain in the flat area is not affected by the increase of parasitic, in line with the considerations of subsection 3.2.3. On the other hand, the increase of stray capacitance reduces the closed-loop frequency value, as predicted in Equation 3.15.
The third circuit simulation is presented in Figure 3.9*c*. Both the AC analysis of the first charge amplifier output and the INA one are plotted. When looking at the plot, it is clear how the cut-off frequency of the instrumentation amplifier is the limiting factor of the circuit bandwidth. Yet, the cut-off is larger than 1MHz, ensuring a large working frequency range for the circuit.
Finally, the noise analysis of the circuit is presented. The plot of Figure 3.9*d* shows the input-referred noise spectrum expressed in terms of $F/\sqrt{Hz}$. The low frequency part of the noise spectrum is dominated by the Johnson noise of the feedback resistor as discussed in the relative subsection (3.2.2). The high frequency noise is limited by the voltage noise of the two amplifiers together with the INA contribution. The spectrum is shaped by the INA transfer function. Two spectra are shown in the plot: the first assuming a 10pF feedback capacitor, the second using a 1pF one. Using a feedback capacitor smaller than the parasitic allows better noise performance as shown in Equation 3.4. Therefore, in order to obtain the best noise performance, a small feedback capacitance should be used. Nevertheless, an increase of C_f allows extending the amplifier bandwidth and increasing the robustness against stray capacitances. Moreover, in presence



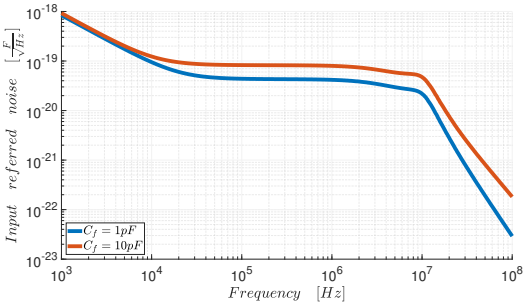
(a) Sweep of feedback capacitance value. The value of the feedback capacitor is swept from 0.1pF to 10pF. Both the gain of the stage and its closed-loop pole shift with the capacitor values.



(b) Sweep of parasitic capacitance value. The value of the stray capacitor is swept from 1pF to 100pF. The gain of the circuit in the flat area is not affected, while the closed-loop pole frequency is reduced for larger value of parasitic.



(c) AC sweep analysis of both charge amplifier and instrumentation amplifier output. This simulation shows how the instrumentation amplifier is the limiting component in terms of signal bandwidth.



(d) Input-referred noise spectrum expressed in terms of capacitance. The spectrum is evaluated for both a feedback capacitor of 1pF and 10 pF. The effect of the resistor noise is visible at low frequency. For the 10pF configuration, the input-referred noise is about 100 $zf/\sqrt{Hz}$ at 1V of polarization.

Figure 3.9: *Circuit simulations performed using the software Multisim from National Instrument.*

of parasitic capacitance in parallel to the feedback path, a larger C_f allows better symmetry among the two branches. For these reasons, it was preferred to use a 10pF feedback capacitor, paying the price of relatively small resolution loss.
In conclusion, the double single ended charge amplifier was chosen as the best circuit topology. The circuit has been implemented on a PCB using two operational amplifiers model AD4817 followed by an instrumentation amplifier model AD8429 for signal amplification. The AC polarization voltage is generated by an external Lock-In Amplifier (LIA). The modulation frequency is chosen greater than 100 kHz in order to ensure negligible gain error and to bypass the 1/f noise of the operational amplifier.

3.4 Third chapter conclusion

In this chapter, the main types of capacitive readout have been presented. For the characterization of the device it is chosen to use an open-loop, time-continuous current readout technique implemented with discrete components. This technique enables high resolution with relatively low complexity and low sensitivity to stray capacitance. Among the different current-sensing methods, the differential charge amplifier with independent branches is found the be the most effective solution. Such solution does not suffer the potential asymmetry of the input stray capacitances, as in the case of the fully differential amplifier. Circuit stability, noise analysis and parasitic rejection are studied in order to chose the best sizing for the circuit components. The circuit can be made stable by compensating one of the poles with a low frequency zero. This can be done by using large feedback resistor. Such feature also reduces the Johnson noise of the resistor, allowing optimum noise performance already in the 100kHz range. This is not the case of the trans-impedance amplifier, which requires large modulation frequency (>5MHz) in order to reduce the impact of the resistor noise. The final circuit has the following characteristics: (i) $R_f = 1G\Omega$ to reduce Johnson noise and ensure feedback stability, (ii) $C_f = 10pF$ to reduce the asymmetry caused by the parasitic in parallel to the feedback paths and to ensure large frequency of the closed-loop pole even for strong input stray capacitance, (iii) a INA with gain equal to 28 that amplifies the signal of the charge amplifier in order to lower the impact of the input-referred noise of the following stages (LIA). Assuming a polarization voltage of 1V and an input stray capacitance of 10pF on each branch, the expected resolution of the circuit is in the order of 100 $zF/\sqrt{Hz}$. Yet, this value is underestimated as the amplifier model used for software simulation has

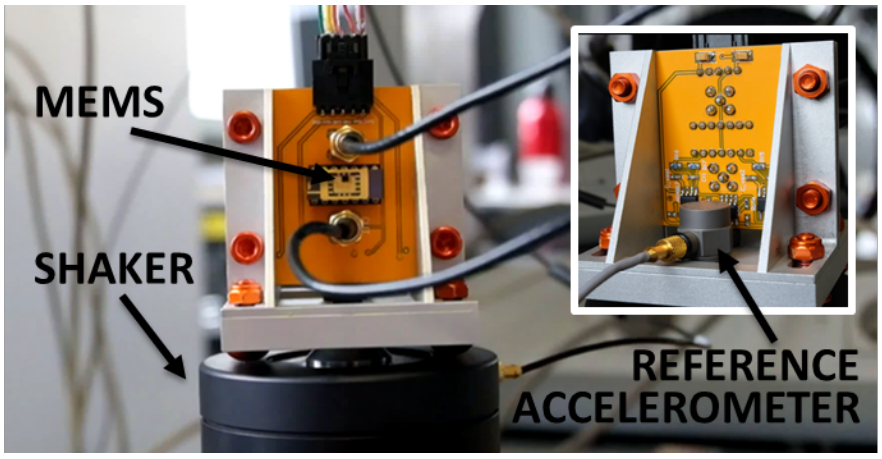


Figure 3.10: *PCB mounted on a shaker during characterization of commercial accelerometers. One side of the PCB carries the socket and the connectors, while the electronic components are soldered on the other side.*

smaller input-referred noise with respect to the real component. Considering this aspect together with the loss of signal to noise ratio due to the LIA demodulation (factor $\sqrt{2}$), the final resolution should be in the order of 300-350 $zF/\sqrt{Hz}$. Finally the circuit is implemented on a compact PCB adapted for acceleration test setups. Figure 3.10 reports an image of the PCB mounted on a shaker during characterization of commercial accelerometers.

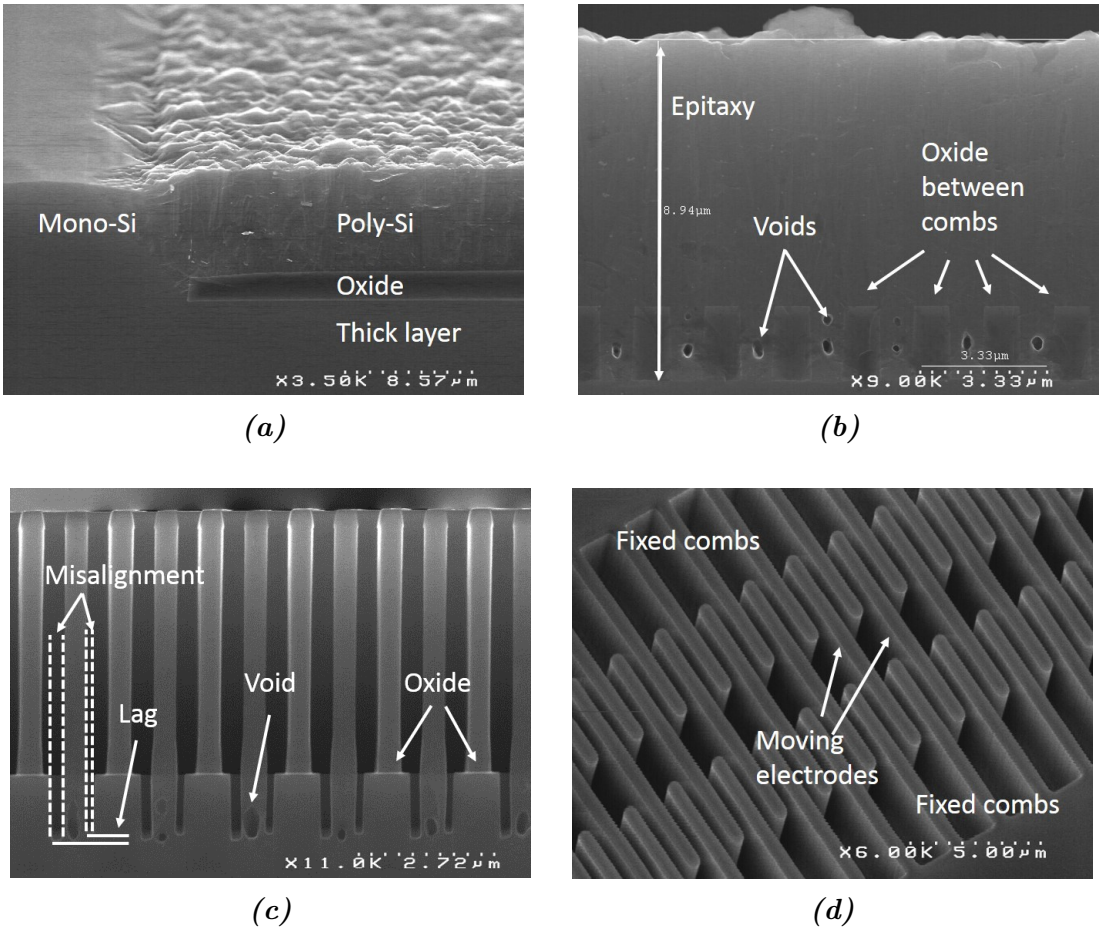
Chapter 4

Characterization of in-plane accelerometers

First, this chapter presents the result of the fabrication process: obtained mechanical structures and critical points in the process flow are shown. The fabrication result is followed by the electro-mechanical characterization of the sensors both at wafer level and at die level. The description of each measurement setup is presented together with the relative results.

4.1 Fabrication results

Figure 4.1 shows four SEM pictures of the device during the fabrication of the thin-layers features. In 4.1*a* the transition between mono-crystalline to poly-crystalline silicon is shown. As mentioned in Chapter 2, the epitaxial layer grows accordingly to the underlaying structure, taking an amorphous form when deposited over the oxide. Figures 4.1*b* and 4.1*c* show a critical aspect encountered during the first fabrication run. The excessive growing speed of the epitaxial layer led to the formation of voids between the oxide structures of the comb-fingers. The epitaxial deposition is faster next to the oxide walls causing the silicon to close on itself before completely filling the gap between the oxide blocks. The size and the length of the void does not cause failure of the comb structures (4.1*c*), however their presence makes the fingers more fragile. This problem could be solved in the future by dividing the epitaxial layer in two subsequent steps. A first slow deposition step necessary to fill the space between the oxide blocks followed by a faster deposition step to grow the remaining silicon layer. Otherwise, a more simple solution would consist in increasing the area between the oxide blocks, at the price of lower capacitive density. Figures 4.1*c* and 4.1*d* show the comb-fingers structures resulting from the first DRIE step. In Figure 4.1*c*, a slight misalignment of the oxide and etching masks is visible: the trenches that separate the combs and the adjacent oxide blocks are uneven. This is also visible



(a) *(b)*

(c) *(d)*

Figure 4.1: *SEM images concerning the fabrication of the thin-layer features. (a) Transition between mono to polycrystalline silicon during thin layer epitaxy. (b) Cross-section of the epitaxial layer showing the presence of voids between the oxide separating the combs. (c) Same cross-section of (b) after the etching of the thin layer. The voids are contained withing the comb-fingers making them more fragile, but do not cause the failure of the structure. (d) Top-view of the comb-fingers region before wafer bonding. Fixed combs are held by suspension bars while moving electrodes are directly connected to the mass.*

from the different depths reached by the etching step (lag effect). The separation between moving and fixed electrode is clearly visible. The top view of Figure 4.1*d* shows the comb-fingers units with a 350nm gap. The central moving electrode, directly connected to the mass, is surrounded by fixed external combs.

The second group of SEM images concerns the etching of the thick layer. Figure 4.2*a* shows the cross-section of a device after the DRIE step. The pad used for the wafer-bonding is highlighted: the partially etched trench and the confinement wall are visible; the substrate and the device wafer merge in the central area of

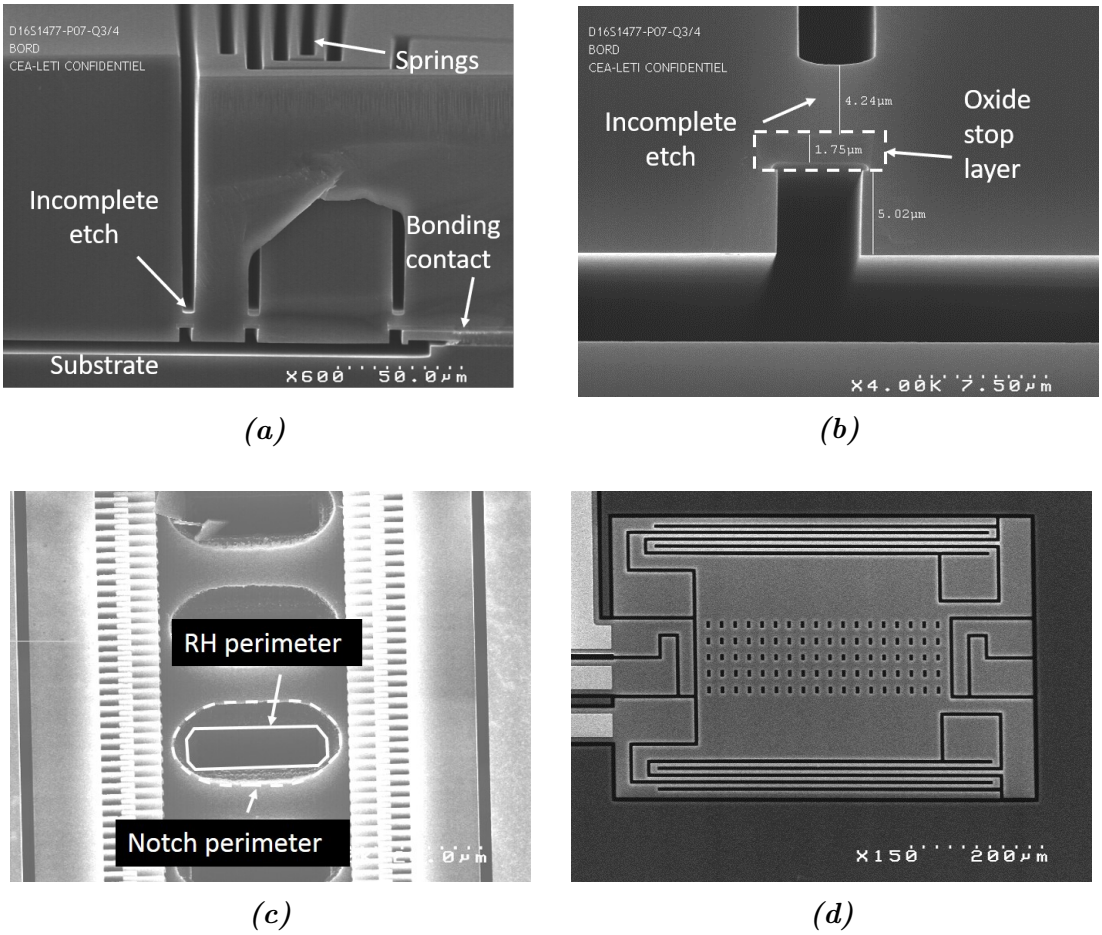


Figure 4.2: *SEM images of the device after etching of the thick layer. (a) Cross-section of the device at the end of the process. The thick-layer etching is incomplete. (b) Zoom on the incomplete etching zone, the oxide-stop layer is highlighted. (c) Example of notching at the bottom of the release holes etch. The image is taken after stripping of the device with carbon-tape and removal of the suspension bars covering the release-hole. (d) Top-view image of the device at the end of the process.*

the pad, while the remaining part of the device is suspended above a cavity. Figure 4.2*b* shows a zoomed image of the first cross-section. The oxide that separates the fixed electrode from the moving mass, acts also as a stop layer for the thick layer etching. On this device, the etch-time is too short and the etching is not completed. Figure 4.2*c* shows the opposite situation. The image was taken after stripping of the device with tape film in order to observe the structures hidden below the thick layer. This time the structure is over-etched and notching is visible. The section of the release holes evolves from a rectangular shape to a ellipsoidal one. After the plasma encounters the stop layer, the etching process spreads uniformly, potentially damaging part of the thin layer elements. As explained in Subsection 2.1.3, the notching of the etch process is related to

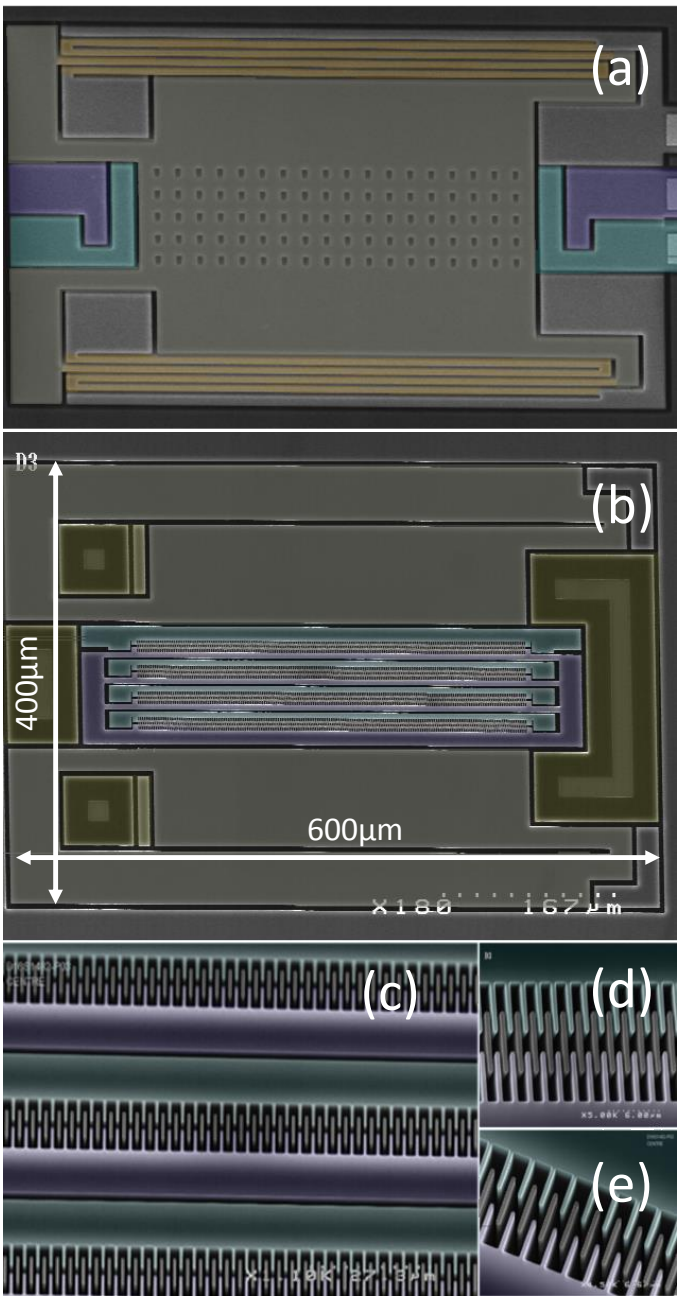


Figure 4.3: *SEM images of the in-plane device: (a) Top view of the device at the end of the process (b) Bottom view of the device before wafer bonding (c) Zoom on the suspensions bars holding the fixed electrodes (d) Image of the comb-fingers region for a 350nm device and (e) for a 500nm device . Image is food-colored in order to highlight each element of the device: electrodes (purple, jade-green), moving mass (brown), anchor points (green), springs (ochre); substrate and springs anchor points are not colored.*

the lag effect which is a critical aspect when performing etching of thick silicon. Moreover, the risk of incomplete etch (Figure 4.2*a*) led to take a safe margin in the etching process, worsening this phenomenon. Figure 4.2*d* shows the top view of an in-plane S-device. Finally, Figure 4.3 shows an overview of the fabricated in-plane S-device highlighting each component with different colors.

4.2 Wafer-level characterization

This section and the following focus on the results obtained from two devices having respectively 500nm and a 350nm gap and 2-folds springs, in line with the design section. The first device will be referred to as D1-500 the second device as D2-350. Along with the characterization of these two sensors, results from other accelerometers are shown in order to highlight specific features of the novel technology.
The characterization of the fabricated devices is performed in two steps: first, wafer-level tests are carried out in order to evaluate the resonance frequency, static capacitance and SF of the accelerometers; second, the devices are tested at die level in order to verify their operational performance and confirm wafer-level observations.

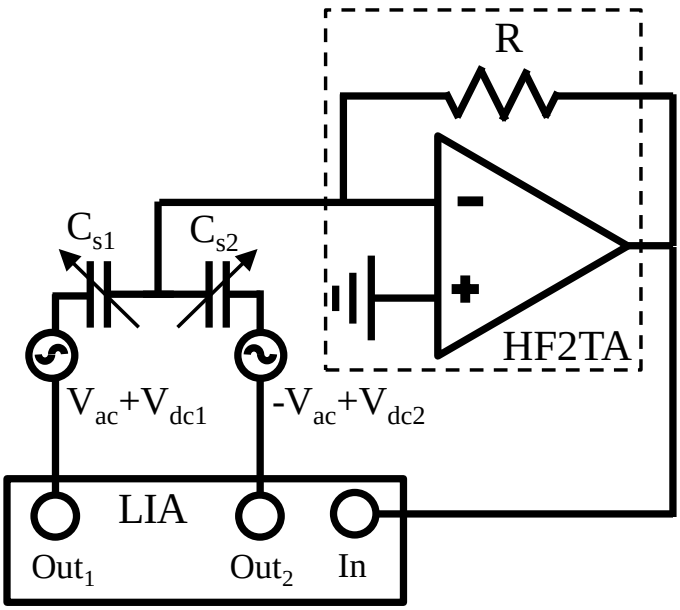


Figure 4.4: *Schematic of the readout scheme adopted for wafer-level tests: fixed electrodes are polarized with two AC signals of opposite phase, generated by the lock-in amplifier. The current signal is converted into voltage by a dedicated trans-impedance amplifier and demodulated with the LIA. The mass motion is obtained by superposing an actuation voltage to the AC signal.*

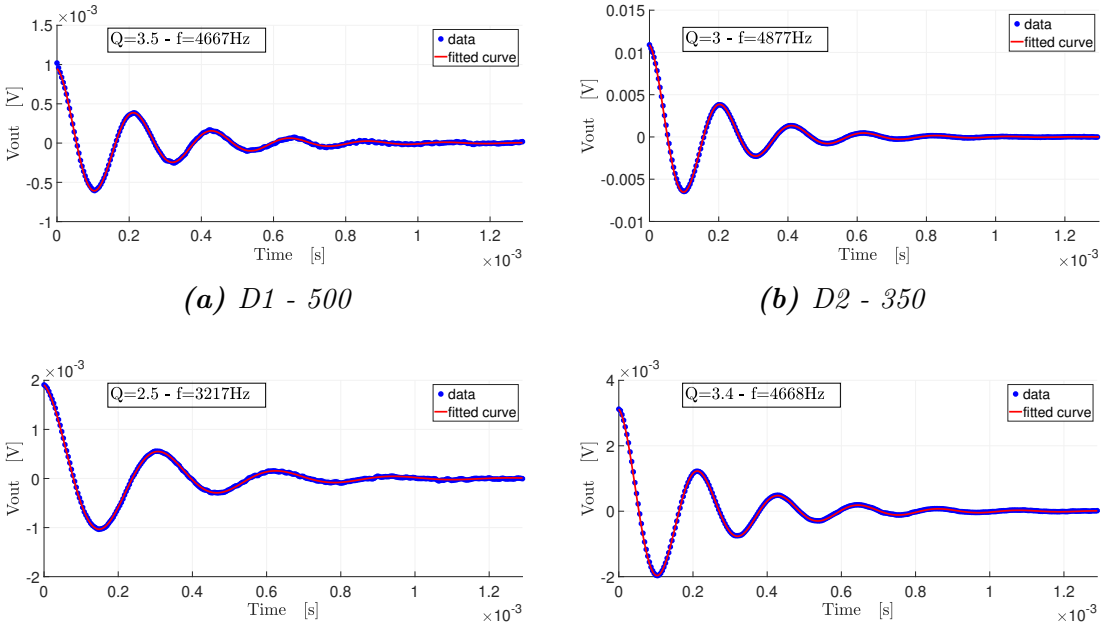
All devices are characterized at wafer level with a semi-automatic probe station compatible with 200mm wafers. A ring-down measurement is performed for resonance frequency and quality factor determination as well as a Capacitance-voltage profiling (C-V) measurement to determine static capacitance.

Ring-down measurement

The ring-down measurement is performed with a lock-in amplifier (Model HF2LI from Zurich Instrument). The current to voltage conversion is made with a dedicated trans-impedance amplifier (HF2TA). A schematic view of the setup is shown in Figure 4.4. Both electrodes are polarized with two AC signals of opposite sign in order to balance the electrostatic force acting on the device and to null most common-mode contributions. At the same time a voltage step, used to obtain the ring-down response, is applied to only one electrode to unbalance the structure. The output current signal is readout from moving mass which is kept at virtual ground by the trans-impedance readout circuit. The demodulated signal is acquired within a bandwidth larger than 5 times the device resonance frequency. The measurement is repeated and averaged n times in order to improve the signal to noise ratio. The obtained time trace is plotted and fitted against the response of a second-order resonator [65]:

$$V_{out}(t) = \Delta V e^{-\frac{t\pi f_0}{Q}} cos\left(2\pi f_0 t\sqrt{1-\frac{1}{4Q^2}}\right) \tag{4.1}$$

where ΔV is the voltage difference generated by the DC step with respect to the static output. The resonance frequency (f_0) and quality factor are extracted from the parameters of the fit function.
Figure 4.5 shows four ring-down measurements plots. The quality factor and resonance frequency of each device are reported in the relative graphs. First, it can be noticed that the data show good matching with the fit function. This is possible thanks to the clear signal obtained with the averaging technique. The second consideration can be made by comparing plots 4.5*a* and 4.5*d*. The two sensors have different gaps, identical springs and are taken from the same stepper exposure field. They show the same resonance frequency and quality factor. This experimentally confirms the theoretical findings in Subsection 2.2.5: the damping coefficient is related to the squeeze film damping of the spring system and does not change with the gap dimension.
The last consideration is related to the accuracy of the resonance frequency estimate. Device D2-350 matches very well the theoretical model while device D1-500 remain within a 5 % margin. This discrepancy is due to the etching gradient on the wafer. Some devices undergo stronger etching, which leads to lower resonance frequency and slightly larger quality factor (the gap between springs is larger, therefore the squeeze film effect is reduced).



(a) D1 - 500

(b) D2 - 350

(c) D3 - device with 500nm gap with 4-folds springs

(d) Device with 350nm gap from same fields as D1

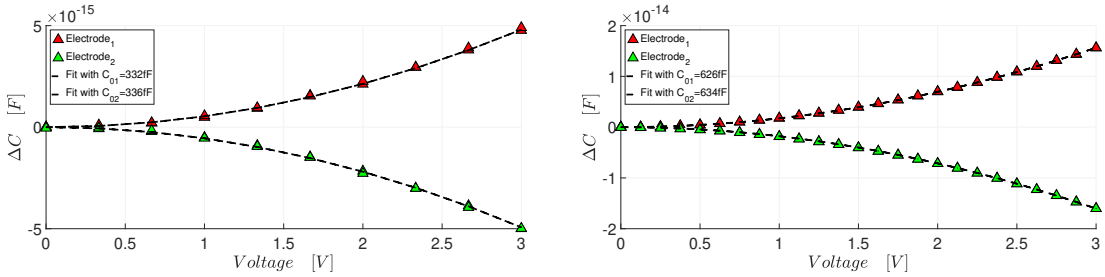
Figure 4.5: *Examples of ring-down measurement.*

Capacitance-voltage profiling

The same readout scheme is used to extract the static capacitance of the devices. This time the voltage used to set the device in motion is gradually swept from 0 to a preset voltage (which allows sufficiently large capacitance variation) while the demodulated voltage is acquired at each point. The procedure is repeated for the second electrode to obtain motion in both directions and data are fitted with a parabolic function. The static capacitance value of each sensing capacitor is deduced from the measured structure stiffness and the fit functions according to the following equations:

$$\Delta C = \overbrace{\frac{\partial C_s}{\partial x}}^{\frac{C_s}{OL}} \overbrace{x}^{\frac{F_{el}}{k}} = \frac{C_s}{OL} \underbrace{\frac{\overbrace{F_{el}}^{\frac{C_s}{OL}\frac{V^2}{2}}}{k}}_{m\omega_0^2} = \left(\frac{C_s}{OL}\right)^2 \frac{V^2}{2m\omega_0^2} = b_2 V^2 \rightarrow C_s = OL\sqrt{2\, b_2\, m\, \omega_0^2} \tag{4.2}$$

where F_{el} is the electrostatic force between the mass and the actuating electrode, m is the proof mass and b_2 is the quadratic coefficient of the polynomial fit of the data. It should be pointed out that two sources of error exist in this measurement: the first is the variation of the overlap with respect to designed values. Larger estimated overlap leads to larger static capacitance. Yet, this type



(a) D1 - 500 *(b) D2 - 350*

Figure 4.6: *Examples of capacitance versus voltage measurement.*

of error does not influence the determination of the sensor SF which depends on the ratio C_s/OL. The second source of error depends on the accuracy in determining the mass of the device. Assuming a smaller mass leads to underestimated static capacitance according to 4.2. The mass estimation error is mainly related to change in the process thickness and to discrepancies between the virtual 3D model used to compute the mass and the real structure.
Once the resonance frequency of the device and its $\partial C_s/\partial x$ are known a first estimate of the SF can be obtained:

$$SF_{wl} = \frac{1}{\omega_0^2}\frac{\partial C_s}{\partial x} = \frac{1}{\omega_0^2}\frac{C_s}{OL} \tag{4.3}$$

It is referred to as wafer-level SF (SF_{wl}).
Figure 4.6 shows the capacitance versus voltage curves for the considered devices. This time the voltage used to set the device in motion is gradually swept from 0 to 3V while the demodulated voltage is acquired at each point. The procedure is repeated for the second electrode and data are fitted with a parabolic function. The total static capacitance value is deduced from the measured structure stiffness and the fit functions. The obtained values of differential static capacitance are around 670 fF and 1.26 pF for the 500 and the 350nm devices respectively. These results match theoretical predictions of 645fF and 1147fF (Table 2.5) within 10%. Now, a first estimate of the scale factor can be computed. The wafer-level SF (Eq.4.3) for devices D1-500 and D2-350 is equal to 3.8 and 6.6 fF/g, respectively, also these values match the theoretical estimate of 3.35 and 5.95fF/g.

4.3 Dicing

After wafer-level characterization, the wafer needs to be diced in order to proceed with the acceleration tests. The ceramic carrier used to mount the devices on the PCB has an available area of less than 5x5 mm^2, allowing to fit at most 2 dies at a time (2.75x2 mm^2 per die). On each die there are three acceleromters (x/y/z-axis). For this reason the splitting of the wafer requires die-level resolution.

Several options are available, yet due to the absence of a wafer-cap and to the presence of moving structures, most of the solutions are not possible. A list of the considered options and the related limitations is presented here:

1. Saw dicing with no film protection. The wafer could be diced with a water-cooled saw. The presence of water and debris, however, would damage the devices. For this reason, this solution has to be excluded for the proposed sensors.

2. Saw dicing with film protection. A ultra-violet (UV) sensitive film can be used to protect the devices during the dicing. However, removal of the film can cause failure of the sensors, which could stick to the film even after UV exposure. Tests performed using this option showed that even when the devices are not released, the adhesion force of the film causes failure of most of the sensors, especially out-of-plane devices.

3. Mechanical dicing. The device can be separated by applying a mechanical stress between two dies using a metal-tip. The strong shocks generated by the dicing can cause failure of the device. For this reason, such solution should be avoided except if the mechanical resistance of the wafer has been previously reduced with other techniques.

4. Laser dicing. This is the solution adopted for the dicing of the wafers as it does not require a cap-protection and it generates the smallest stress on the

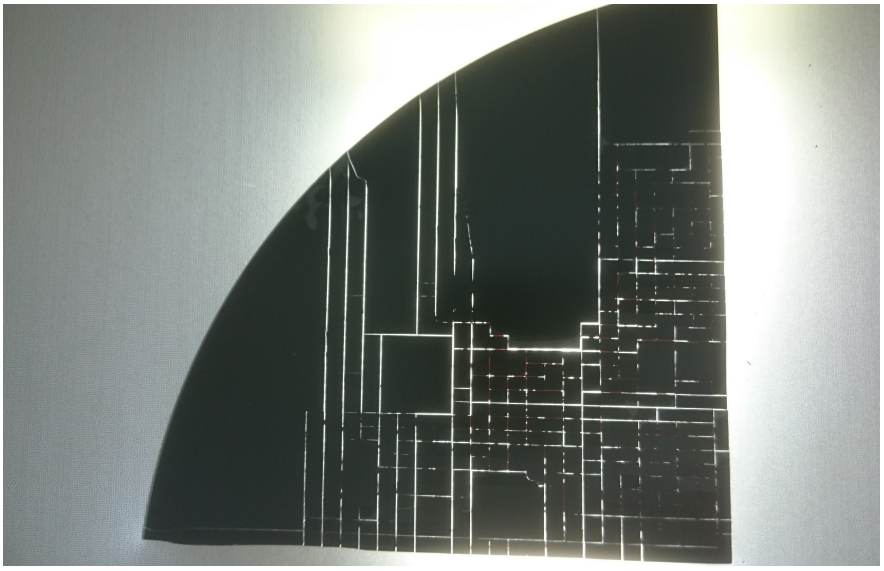


Figure 4.7: *Image of a quarter of wafer after the dicing procedure. In some areas the separation of the dices was not completed after the laser cut. In those cases, it was necessary to complete the dicing with a mechanical tip.*

device. The wafer is glued to an adhesive film held by an external metal frame. A laser beam is used to produce stress between the dies which are then separated by stretching the adhesive film. The laser cannot penetrate thick layers of doped silicon or metallic materials. For this reason, during the device fabrication, a trench is etched in the thick layer around each die. No trench is opened in the thin-layer in order to avoid using the same etching process to remove large silicon areas and fabricate sub-micrometric combs. Despite its small thickness, the highly doped epitaxial layer absorbs most of the laser power causing poor yield in the dicing process. Yet, it helps in making the wafer more fragile. The dicing of the device is often completed using a dicing tip. In the future design, also the thin layer should be partially removed in order to avoid laser blocking. As an alternative, the presence of a cap-wafer could solve most of the problems related to the dicing procedure.
Finally, it should be mentioned that the laser dicing is outsourced to an external company introducing a delay in the characterization process, yet it is the only available solution for the moment.

Next, each die is glued with conductive glue to a ceramic carrier and bonded to the gold pads. The carriers are placed into a socket directly soldered on the PCB with the readout electronics presented in Subsection 3.3.2 (Figure 4.9). The modulation signal V_m is generated by an external lock-in amplifier which act also as demodulator.

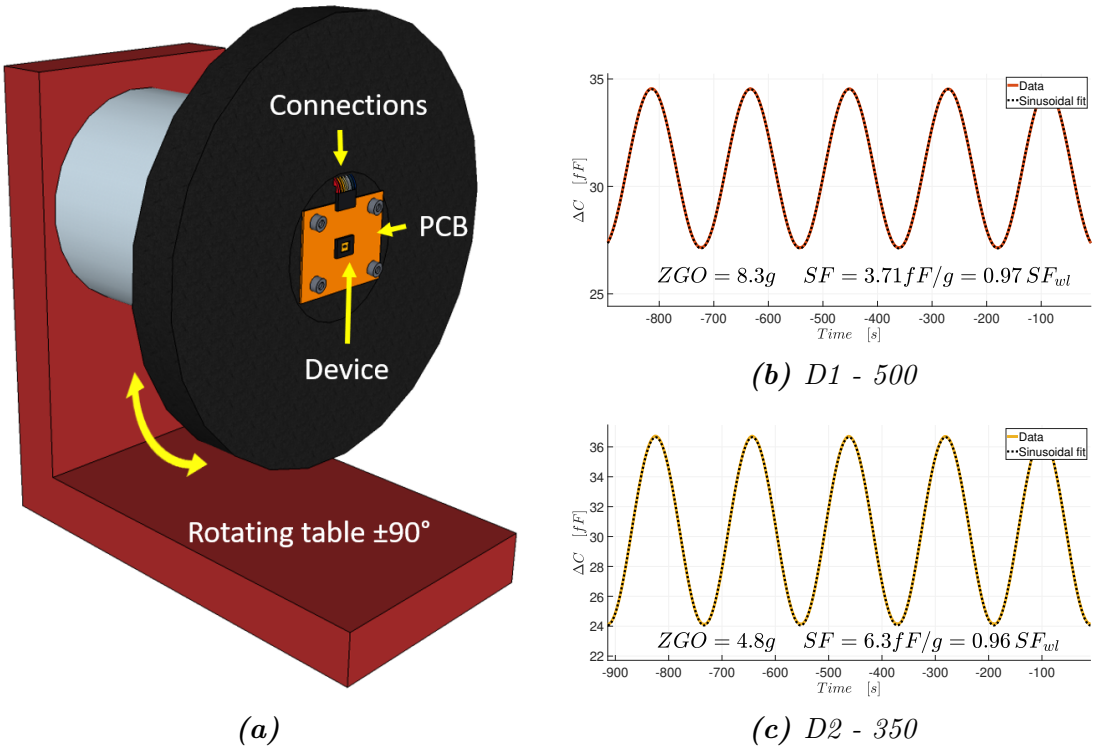
4.4 Die-level characterization

$\pm 1g$ test

The first operational test of the fabricated devices consists in placing the sensor on a rotating table with the moving plate set parallel to the gravity force. In-plane devices are set parallel to the plate, while out-of-plane devices are held perpendicular to it using a dedicated metal frame (Figure 4.8*a*). The moving plate is set in periodic motion at constant speed covering a rotation angle of 180°. In this way, the orientation of the gravity force with respect to the sensor is modulated, generating a sinusoidal output from the sensors of 2g peak to peak amplitude. The aim of this test it to confirm the SF measured at wafer level and to perform a quick check of the device behavior under an acceleration signal.
The scale factor of the sensor and its Zero-g Offset (ZGO) are extracted from the sinusoidal fit of the data according to the following equations:

$$SF = \frac{\Delta C_{max} - \Delta C_{min}}{2} \quad ZGO = \frac{\Delta C_{max} + \Delta C_{min}}{2} \tag{4.4}$$

Figures 4.8*b* and 4.8*c* show the measurement output plots for devices D1-500 and D2-350: SF and ZGO are reported in text in each figure.



(a)

(b) D1 - 500

(c) D2 - 350

Figure 4.8: *(a) 3D model of the ±1g test. The device is placed at the center of the rotating table which spins by ± 90 degrees in order to generate a sinusoidal acceleration of ±1g. (b-c) Scale factor and ZGO evaluation for devices D1-500 and D2-350. The actuation voltage (V_m) is set at 1V. The rotating table spins at 2 dps leading to a sinusoidal acceleration of 5.5 mHz. A 4th order 200 mHz LIA filter is used to filter the signal.*

The LIA output signal is acquired over five rotation cycles. The rotating speed is kept low in order to minimize the impact of environmental noise. The first observation is the good matching between the acquired signal and the sinusoidal fit, this proves the proper functioning of the device.
Second, it can be observed that the measured SF matches the wafer level estimate within 4%, proving that this type of measurement could be a valuable alternative to the rotating table procedure. There are two main explanations for the slight mismatch. The first is a misalignment in the setup: the device might not be perfectly aligned with the acceleration signal. For instance an alignment error could be generated when manually gluing the device to the carrier. The second explanation is related to an over-estimation of the mass which leads to a larger estimated stiffness and $\partial C_0/\partial x$ (Equation 4.2). Assuming the misalignment to be low, the measured value of SF are taken as reference for upcoming computations. The values are reported in Table 4.1 and compared to the theoretical values reported in Subsection 2.2.5, showing good agreement with theoretical predictions.

Regarding the ZGO level, values of 4.8g and 8.3g are found. It can be noticed that the offset value expressed in terms of capacitance is similar for both structures. This suggests that the ZGO is not related to electronic: in this case it should be proportional to the static capacitance value (Equation 3.13). More likely, the offset source is mainly related to a mismatch of the stray capacitance in parallel to the sensing capacitors inside the accelerometer die. For instance the two arms holding the fixed suspension bars of the jade-green electrode (visible in Figure 4.3.*a*) are facing the moving mass on both sides, while the purple electrode has no such capacitive surface. This asymmetry in the design can cause an offset in-line with the observed one. A future re-design could reduce this type of error.

High-g test

High-g tests are performed using the rotating table again. This time the measurement aims to verify the FSR and linearity of the sensor. While all other tests were performed at CEA-Leti, this measurement was performed at Politecnico di

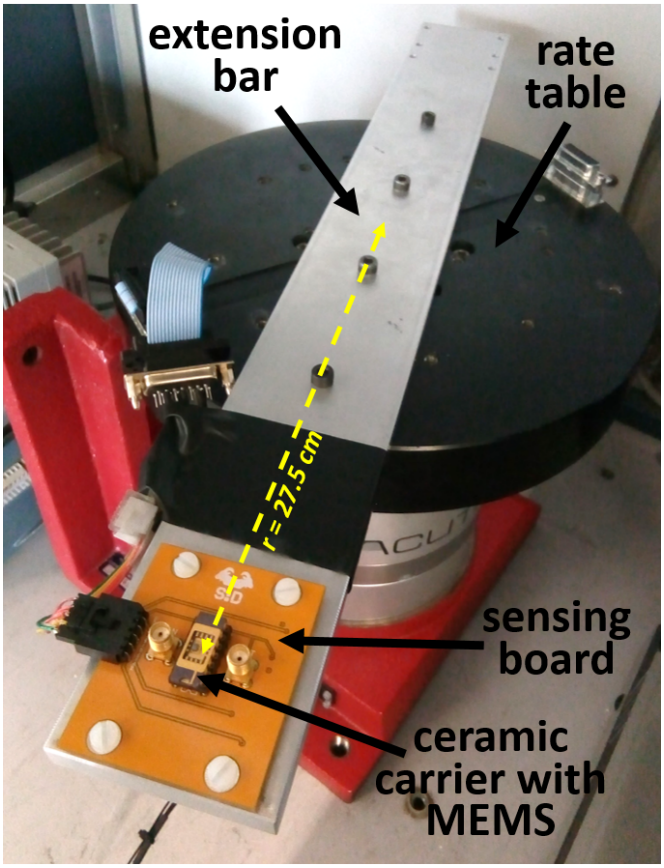


Figure 4.9: *Image of the setup used for high-g tests. The second PCB used to balance the structure is not shown in the image.*

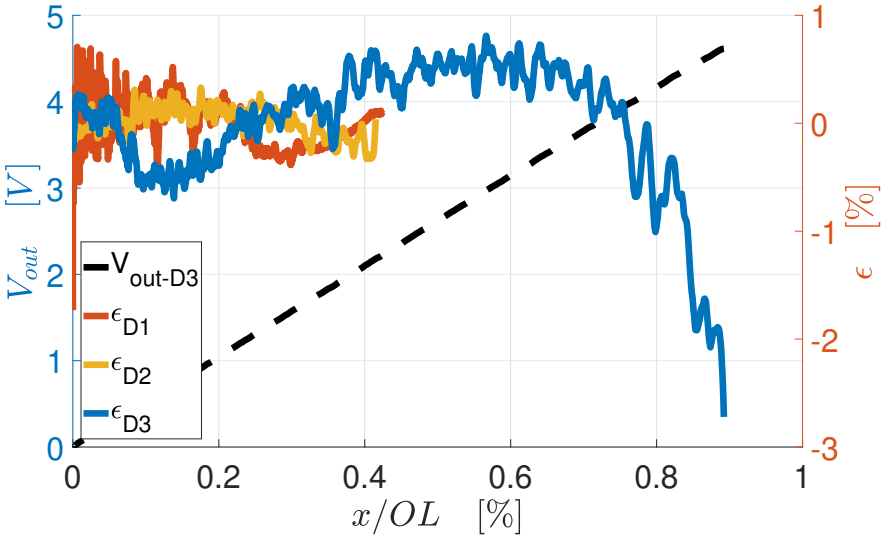


Figure 4.10: *Rate table measurement using custom electronic and devices 1-2-3, signal modulation and demodulation is performed with a LI model SR830 from Stanford Research System: output voltage and linearity errors versus acceleration signal. The devices are polarized with 500mV signal at 100kHz, the lock-in amplifies the demodulated signal by a factor* $10/\sqrt{2}$ *before acquisition. The linearity error is evaluated with respect to the linear fit of the data as a % of the FSR.*

Milano which provided a rotating-tale with continuous angular freedom and high spinning rate. Figure 4.9 shows an image of the setup. In this case the moving plate is set parallel to ground. A metal bar is anchored to the rate-table in order to increase the distance of the device from center. On the two ends, two identical printed component boards (PCBs) are used to balance the setup. One of the two cards is hosting the device and amplifies the signal before sending it through sliding connections. For each measurement, the table spins at an increasing speed ranging from 0 to 2950 $^{\circ}/s$.
The maximum acceleration (a_{max}) is given by:

$$a_{max} = \omega_{max}^2 R = 74.3g \tag{4.5}$$

with R the distance from center, g the gravity signal and ω_{max} the rotation speed in radiant per second.
Figure 4.10 reports the high-g acceleration test performed on three different devices: a device with 500nm gap and 4-folds springs (D3), and two devices with 500nm and 350nm gap and 2-folds springs (D1-D2). The three sensors undergo an acceleration sweep ranging from 0 to 74.3g as previously described. The left y-axis report the output voltage of the 4-folds sensor, while on the right y-axis the linearity error of the three accelerometers is reported. The x-axis unit is the displacement as a percentage of the initial overlap. D1 and D2 are stiffer

than D3, therefore the achieved maximum displacement stops at around 40 % of the initial overlap. More interesting is the result coming from D3. This sensor has a resonance frequency of 3216 Hz (Figure 4.5*c*) which, at maximum spinning speed, translates into a 1.785 μm mass displacement, *i.e.* 89.2% of the initial comb-finger overlap. The nonlinearity remains within 1% up to 70g, *i.e.* 84% of the initial overlap. The linearity error is larger than the one expected from simulations (≈0.1%); this discrepancy can be attributed to geometric non-idealities. However, the plot shape of the error versus acceleration is in line with the FEM simulations and the measurement demonstrates a very high linear range. Finally, considering the agreement with design expectations and the small linear error observed up to 40% of the travel range, this result can be extended with reasonable confidence to double fold structures, leading to a FSR of more than 140g.

Noise floor measurement

In order to test the sensors noise-floor, the devices are placed in an anechoic chamber together with a reference accelerometer from Colybris (model VS1002) (Figure 4.11.a). The devices are not packaged and are therefore sensitive to external sounds. For instance, it has been observed that the noise of cooling-fan of the power generator induces a peak in the acceleration noise spectrum. For this reason the lock-in amplifier and voltage source are placed outside the chamber and the cables slide into the chamber using a foam connector (Figure 4.11.b). First

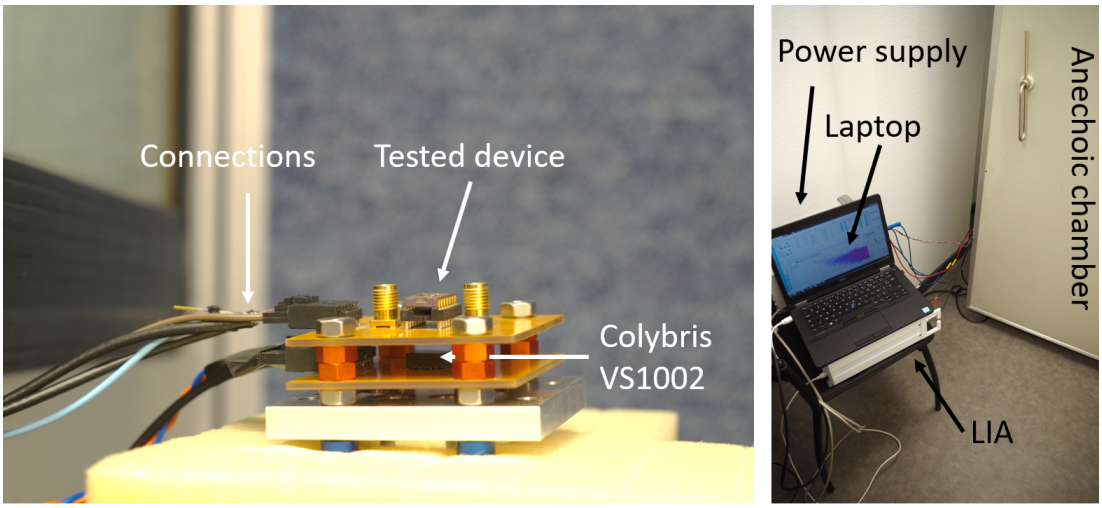


Figure 4.11: *Images of the setup used for high-g tests: (a) the PCB hosting the device is mounted with the reference accelerometer and placed on a foam rubber base in the anechoic chamber. (b) The cables connect the PCB to the external setup: a laptop, a lock-in amplifier and a power supply.*

Device	f_{0th} $[Hz]$	f_{0m} $[Hz]$	SF_{th} $[fF/g]$	SF_m $[fF/g]$	BN_{th} $[\mu g/\sqrt{Hz}]$	BN_m $[\mu g/\sqrt{Hz}]$	FSR_{th} $[g]$	FSR_m $[g]$
D1-500	4890	4667	3.35	3.71	8.8	7.5	>192	≈140
D2-350	4890	4877	5.95	6.3	8.8	7.5	>192	≈160

Table 4.1: *Comparison between theoretical (th) and measured/deduced (m) device performance*

Device	FSR $[g]$	Resolution $[\mu g/\sqrt{Hz}]$	DR (1Hz) $[dB]$	Footprint $[mm^2]$	BW $[kHz]$
This work	**≈ 160**	**7.9**	**≈ 146**	**0.24**	**≈ 4.5**
[66]	<3	0.35	138	>100	4.5
[67] (Closed loop)	20	6.2	130	>10	0.25
[68] (Resonant accelerometer)	30	1	149	>10	0.2

Table 4.2: *Comparison between performance obtained with novel fabrication and previous works found in the literature.*

the ambient noise is characterized by using the reference accelerometer. The VS1002 output is acquired in terms of Fast Fourier Transform (FFT) (directly computed by the lock-in interface) and plotted against frequency. The FFT spectrum is averaged over 100 acquisitions in order to improve the noise spectrum accuracy. Next, the demodulated output signal of the lock-in amplifier is acquired when no modulation voltage is applied to the sensor ($V_m = 0$). This procedure is necessary to evaluate the electronic noise floor of the readout. Finally, the modulation voltage is turned on and set to the maximum allowed amplitude. For in plane sensors the voltage was set to the maximum amplitude allowed by the lock-in amplifier *i.e.* 10V. The FFT of the output is acquired and plotted against frequency. The measured noise spectra are expressed in terms of input equivalent acceleration by dividing the output noise by the gain of the readout chain and compared on the same plot.

The top panel of Figure 4.12 shows three noise spectra. The total noise plot confirms the resonance frequency and quality factor of the sensor and proves the possibility to detect the Brownian noise floor even for the less sensitive design. The thermo-mechanical noise of the seismic mass is resolved, yielding a resolution better than 10 $\mu g/\sqrt{Hz}$. The measurement is very consistent with the signal given by the reference accelerometer: the peak at 20 Hz in both measurements is due to low frequency ambient noise, despite the anechoic chamber. The amplitude difference between the two detected signals is likely due to different mounting orientations of the two devices: the reference device is an out-of-plane accelerometer. The measured Brownian noise is close to the predicted value, validating our damping term estimation. Finally, when polarizing the device at 10V, the capacitive resolution of the circuit is equal to 19 $zF/\sqrt{Hz}$ ($ENEA \times SF$).

Such resolution is in line with results obtained in literature using dedicated integrated circuits [51, 69]. Moreover the noise floor is lower than the one expected from simulations at 10V of polarization (350/10=35 $zF/\sqrt{Hz}$) likely due to the smaller stray capacitance.
Nevertheless, generating such a large polarization signal (10V) is not always possible due to power budget and integrated circuits constraints. It is shown here how the same performance could be achieved at lower voltage by reducing the gap of the electrodes i.e. increasing the number of detection units. The bottom panel of Figure 4.12 shows the noise measurement with the D2-350 device. The

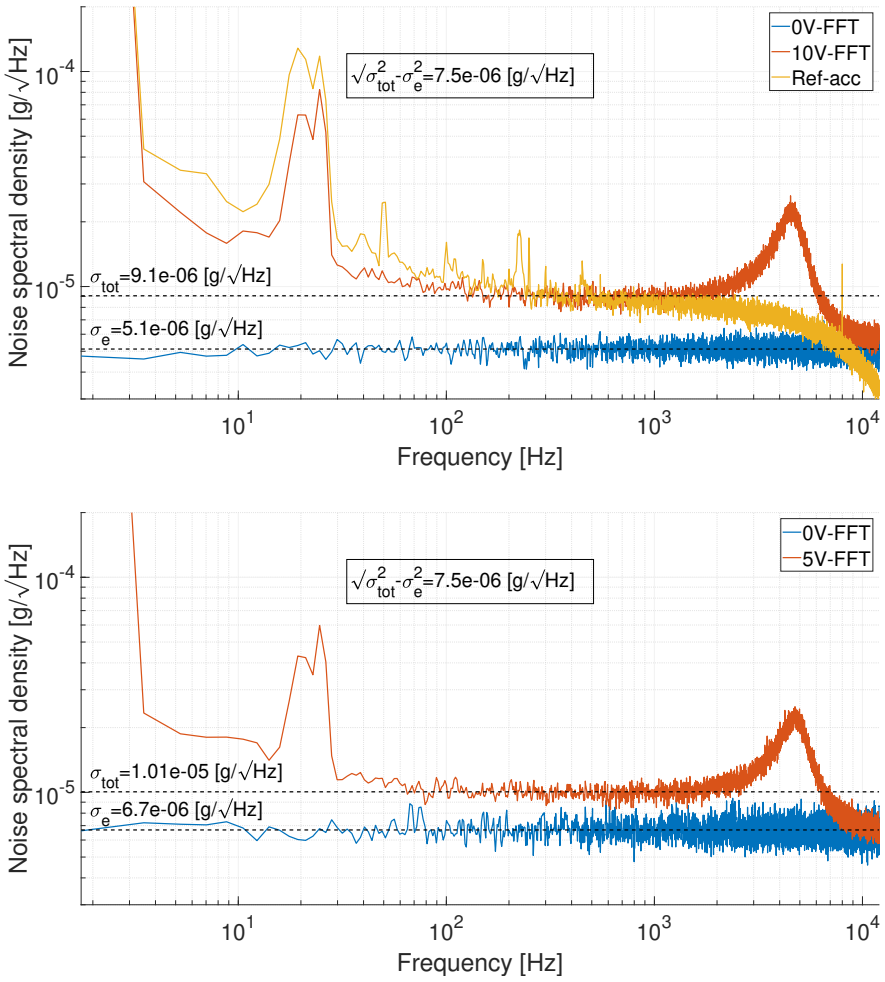
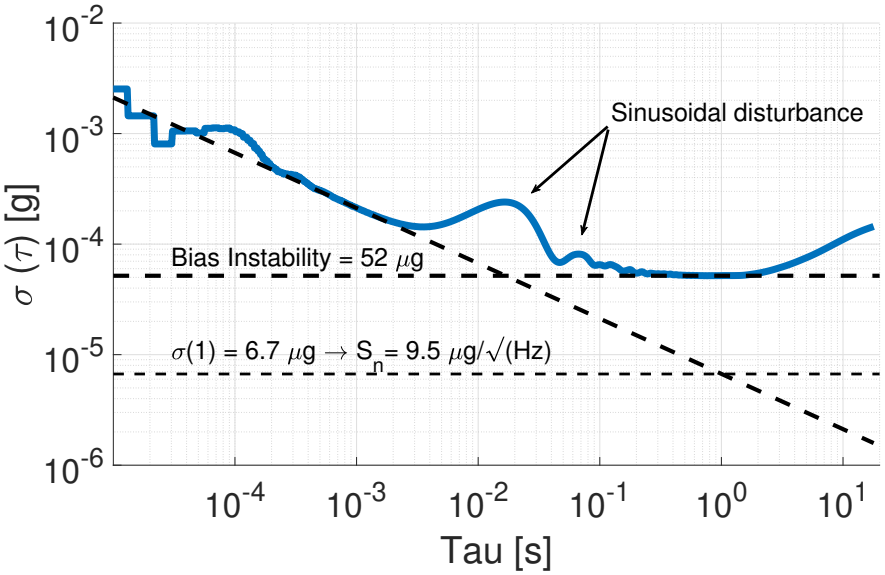


Figure 4.12: *Top: Fast Fourier Transform of three different signals acquired with the 500nm device: (blue) Electronic noise of the readout chain i.e. when Vm=0; (red) Total noise of the readout chain when Vm=10V; (yellow) Output noise of a commercial reference accelerometer with resolution of 7 $\mu g\ \sqrt{Hz}$. Bottom: FFT of the 350nm device with the same principle used for 500nm device. Similar noise performance is achieved with half the polarization voltage.*

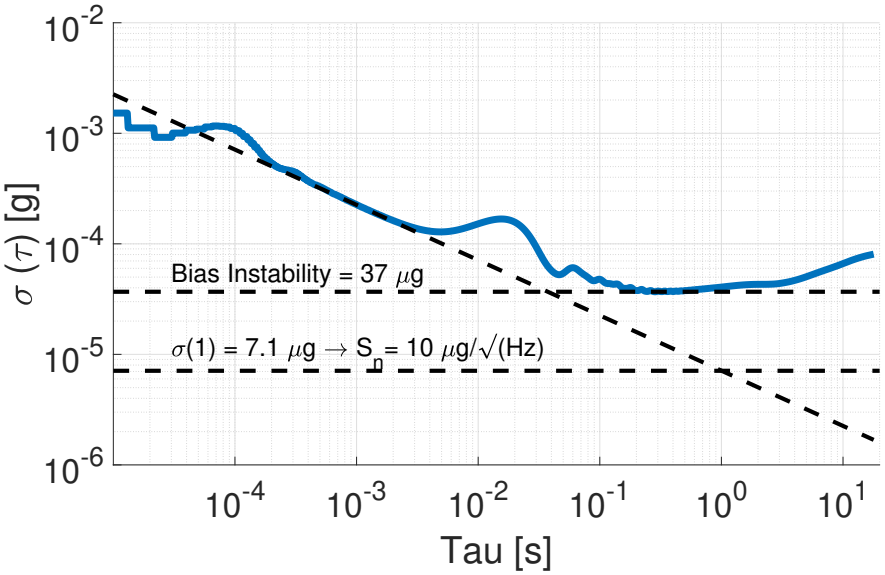
thermo-mechanical noise is visible with a 5V polarization despite the large parasitic of the discrete board. A peak at the device resonance frequency (4.9kHz) appears. At the same time, using a polarization voltage of 10V would lead to a total noise of 8.2 $\mu g/\sqrt{Hz}$. Considering the measured FSR, this yields a dynamic range of more than 145 dB over a 1 Hz bandwidth. Table 4.2 compares this result to some of the most recent works on large dynamic range accelerometers. The new multi-layer device displays better or similar dynamic range than these works and achieves such performance with a footprint almost two orders of magnitude smaller, while keeping a large bandwidth.

Bias stability

The last functional test performed with the sensors is a the measurement of the Allan variance. This analysis studies the resolution of the device versus the integration time highlighting the difference noise sources. The lowest detectable acceleration is called bias instability. The Allan variance test is performed in the same condition used for the noise floor evaluation. This time the demodulated signal is acquired for 180s and then processed with a numerical algorithm in order to compute the Allan variance. The measurement is used to confirm the white noise floor observed with the FFT method and to study the bias stability of the sensor. Figure 4.13 shows the Allan deviation of the device D1-500 and D2-350 for an integration time up to 10 seconds. The white noise value is in line with FFT measurement, while the bias instability is around 35 μg for the 350nm device and 50 μg for the 500nm one. It should be pointed out that no specific design solution was taken in order to reduce the bias instability of the sensor and no temperature compensation was present.



(a) Device D1-500. The device is polarized with $V_m = 10V$.



(b) Device D2-350. The device is polarized with $V_m = 5V$.

Figure 4.13: *Allan deviation of devices D1-500 and D2-350. The sinusoidal disturbance at 20Hz is clearly visible in the plot. Measured white noise value confirms the FFT measurement while bias instability is around 35 and 50 for the two devices μg.*

4.5 Fourth chapter conclusion

In this chapter the characterization of in-plane sensors was shown. The fabrication process of in plane sensors presents two main critical points. During the growth of the epitaxial layers voids are formed within the oxide pattern, this causes a risk of failure of the comb-fingers and make the structure more fragile. The second critical aspect concerns the etching of the thick-layer. In order to reduce the risk of incomplete etching, the structures are over-etched. This aspect together with the lag effect causes severe notching when the plasma encounters the oxide stop-layer. The notching can damage the thin layer structures like the comb-fingers. Despite these fabrication issues, good yield and sizes in-line with the design rules are obtained. Next, results from the wafer-level characterization are shown together with the description of the setup. The device shows static capacitance and resonance frequency in good agreement with theoretical estimates (within 10 and 5% margin respectively). Also the observed damping mechanism is in line with expectations. Next, dicing of the devices is addressed. The sensors are diced with a laser technique due to the absence of a cap wafer and to avoid excessive shocks during die separation. Finally, die-level results show noise floor of less than 9 $\mu g/\sqrt{Hz}$ and expected FSR of 160g for a sensor of 400x600 μm^2. Such noise performance are at least a factor 5 better than consumer sensors of comparable size. Obtaining such resolution is possible also due to an electronic noise floor as low as 19 $zF/\sqrt{Hz}$ enabled by the large polarization and the low noise electronics. The obtained dynamic range is about 10 dB higher than most of the works found in literature and it is obtained despite the strong size reduction (factor 40-400) and the large bandwidth ($\approx 4.5kHz$).

Chapter 5

Characterization of out-of-plane accelerometers

As in the previous chapter, first the results from fabrication flow are presented. The fabrication section is followed by the characterization results at wafer and die level.

5.1 Fabrication results

Figures 5.1*a* and 5.1*b* show an overview and a zoomed image of the springs system of an S-Z accelerometer. In Figure 5.1*a* all elements of the spring system are visible: two flexural springs for in-plane shock resistance and five torsional bars constituting the anti-tilt system described in Subsection 2.2.6. In the zoomed image (5.1*b*) the partial etch of the springs, required to lower the total stiffness of the accelerometer, is clearly visible. Figures 5.1*c* and 5.1*d* show SEM images of the vertical comb-fingers. The thickness of the electrodes connected to the thick layer is reduced by the same partial etch used for the springs system. On the side of the electrodes a residue is visible. The distribution of such leftover is not uniform and seems to be present only on the smallest etched features. The origin of the residue seems to be related to an incomplete removal of the photo-resist used for the partial etch. The measured resistance between the electrodes is high ($G\Omega$), suggesting that the residue is not doped silicon, but most likely the passivation layer used for the DRIE. The effects of the residues on the device performance should be further investigated.
The second group of images of Figure 5.2 shows details of the device after the thick layer etching. Besides Figure 5.2*c*, all other images were obtained after stripping of the device with a carbon-tape. The tape was applied once on the wafer in order to strip-off the entire device area and expose the bottom area of the sensor. Next, the tape was folded on the bottom part of the device and unfolded: this way, the thin layer grid covering the combs and the release holes

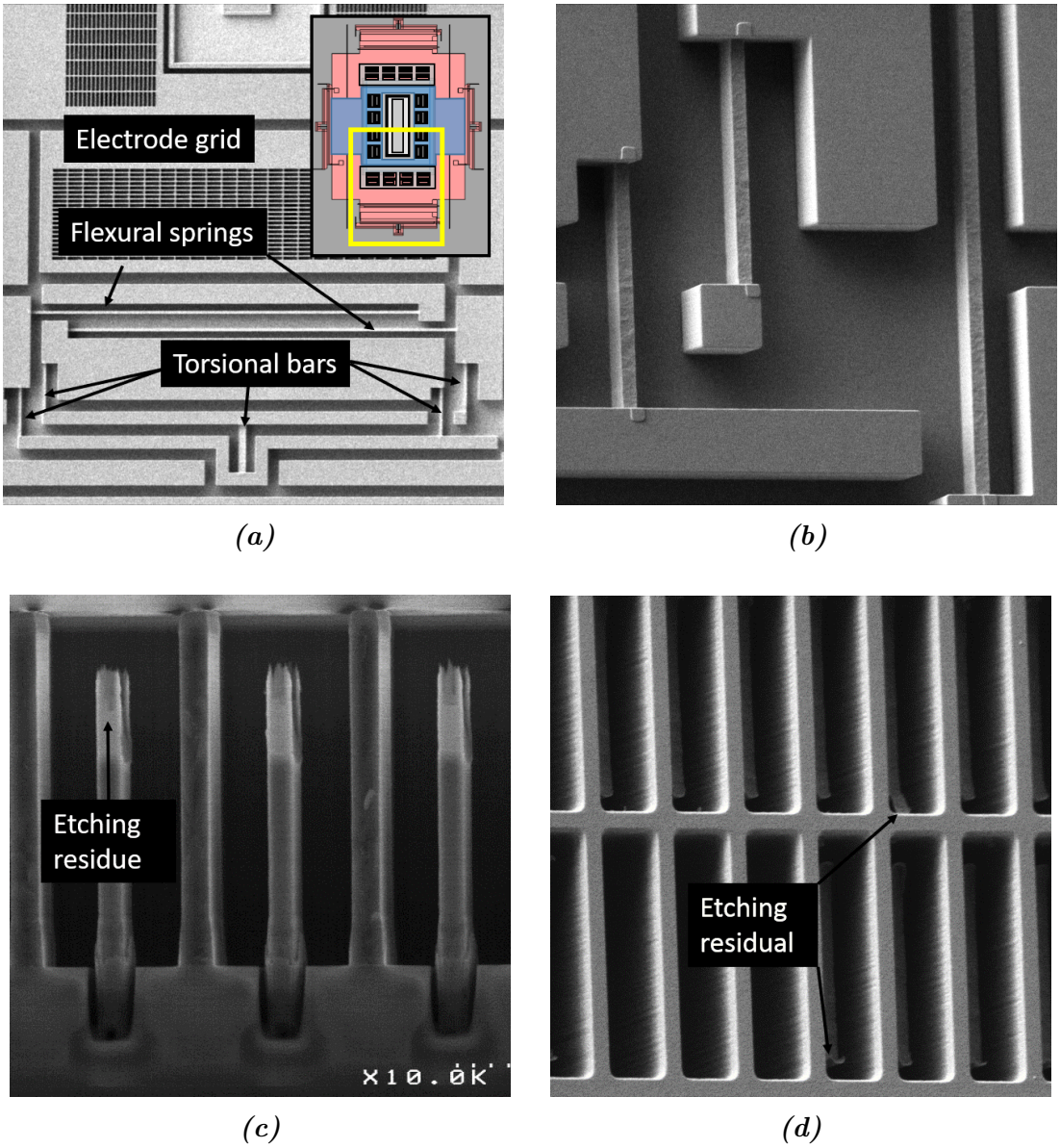


Figure 5.1: *SEM images of the thin layers features for out-of-plane accelerometers. (a) Top-view of the device portion highlighted in the schematic image in the left corner. The torsional and flexural springs of the device are visible together with the electrodes grids. (b) Zoom on the torsion bars of the first image. The partial etching is visible. (c) Cross-section of the vertical comb-fingers interdigitated with the suspended grid. Etching residue is visible. (d) Zoom on the electrode grid. Vertical comb-fingers are visible as well.*

was removed allowing to take images as the one in Figure 5.2*b*. In this specific case it is a $100\mu m$ thick device. Figure 5.2*a* shows the effects of the etching lag. While the release hole which confines with a large aperture is completely opened

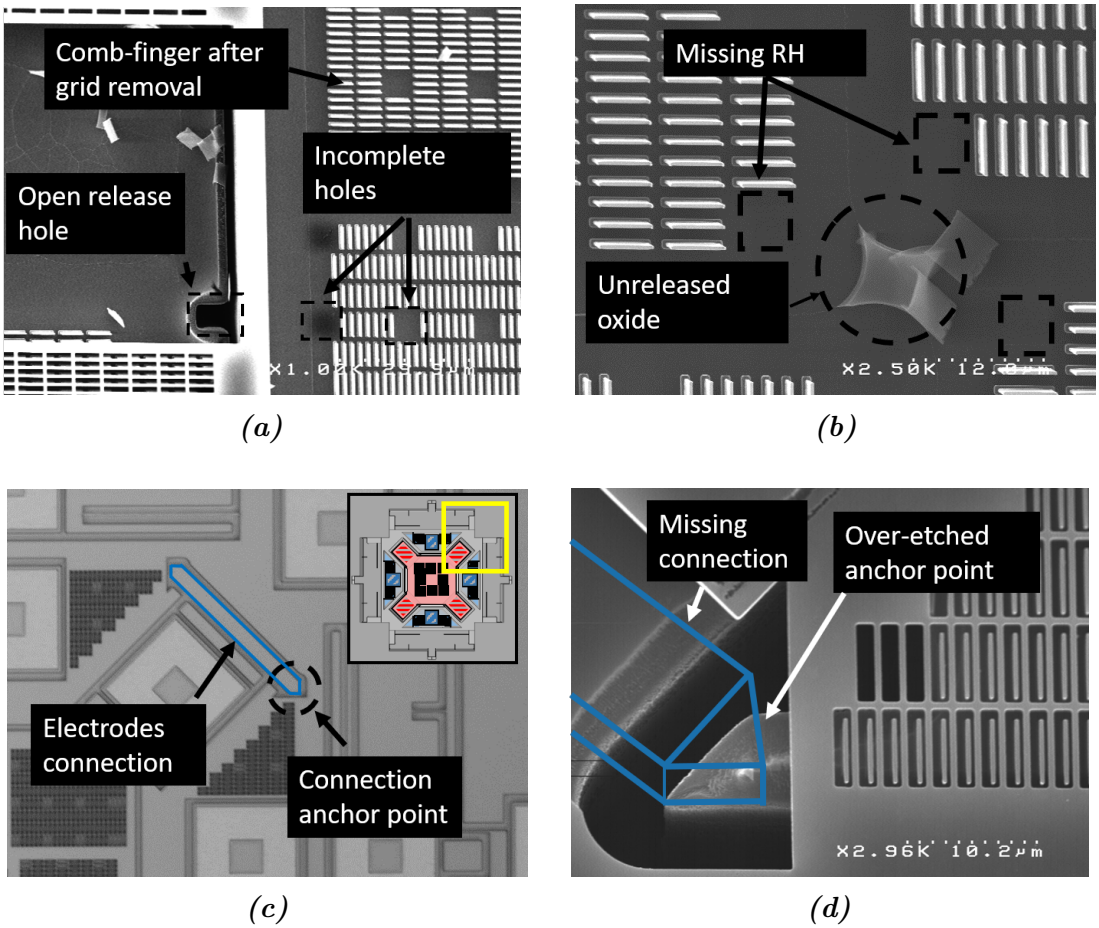


Figure 5.2: *SEM images of the device after thick layer DRIE etching and stripping with carbon-tape. (a) Example of the lag problem. In the image an open release hole is highlighted. This hole is communicating with a larger aperture and therefore its etching speed is faster than the isolated holes like those shown in between the comb-fingers. (b) Zoom image of the comb-fingers area. Unreleased oxide is present due to the incomplete release holes. The device is not fully released. (c) View of the M-Z device before wafer bonding. The shown area is highlighted in the schematic view. The thin-layer connection between two thick layer structures is highlighted in blue. (d) Image of the connection anchor point at the end of the process. The excessive notch caused the connection to fail.*

by the DRIE etching, internal holes remain not entirely etched. This problem leads to the effect observed in Figure 5.2*b*: the missing release-holes cause defects in the release process, leaving un-released oxide areas which prevent the device release. In order to fully complete the release holes opening, the etching time is increased. As seen for the in-plane devices this causes notching. While for XY-devices the notching did not damage the underlying thin layer, for out-of-plane sensors several problems were encountered. Figure 5.2*c* shows the bottom view

of the device before wafer bonding. The dashed line highlights the anchor point of a connection between two electrode blocks. The connection is fabricated in thin layer and connects two thick layer structures. Figure 5.2*d* shows the point where the connection is anchored to the thick layer, after the final DRIE step. The notching of the etching process of the external opening causes the anchor point to fail, breaking the electrode connections. It was observed that some of the M-Z devices had only a fraction of the expected capacitance, as one or more sub-section of the electrode were not in contact anymore. For this reason it was necessary to reduce the inertial layer thickness from 100 μm down to 50 μm. In this way the etching time would be reduced and so would the lag effect and its consequences. A future design could take this into account by increasing the distance between the etching areas of the thick layer and the thin layer structures. Moreover, a more uniform design in terms of etching openings could reduce the lag effect and allow the implementation of devices with thicker structures.
Finally, figures 5.3 and 5.4 show SEM images of the two sensors type M-Z and S-Z. The images are colored according to the voltage polarity of each component. Reducing the thickness of the inertial layer allowed to obtain fully working sensors. Yet, it should be mentioned that the yield of out-of-plane accelerometers remained low. To give an idea, for the 50 μm process only one device out of 30 would be working properly. Such ratio would further decreases after the dicing due to stresses during the procedure and the transportation. At the end, it was possible to obtain only a handful of devices to perform all the tests out of an entire wafer. The reason behind such poor yield is related to all the problems mentioned so far (notching, residues) as well to problems with the release of the sensors from the oxide. Indeed, the release distance was often non homogeneous, either making the anchor points more fragile or non entirely releasing the moving mass.

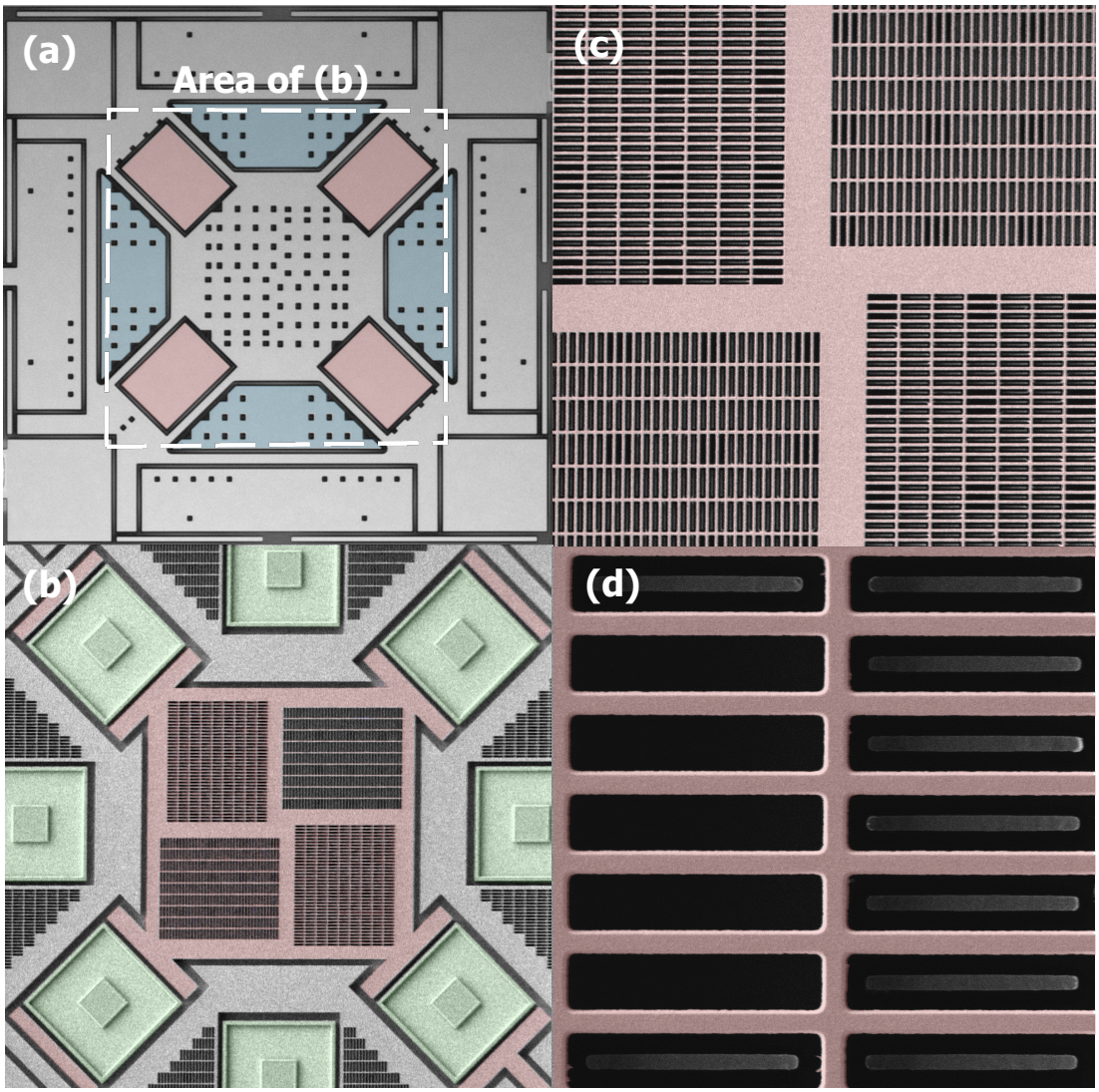


Figure 5.3: *SEM images of the device M-Z: (a) Top view of the device at the end of the process (b) Bottom view of the device before wafer bonding, the moving mass is highlighted with a white dashed line (c) Zoom on the central electrode suspended grid (d) Image of the comb-fingers region in the suspended grid. Image is food-colored in order to highlight each element of the device: electrodes (red, jade-green), anchor points (green); mass and springs anchor points are not colored.*

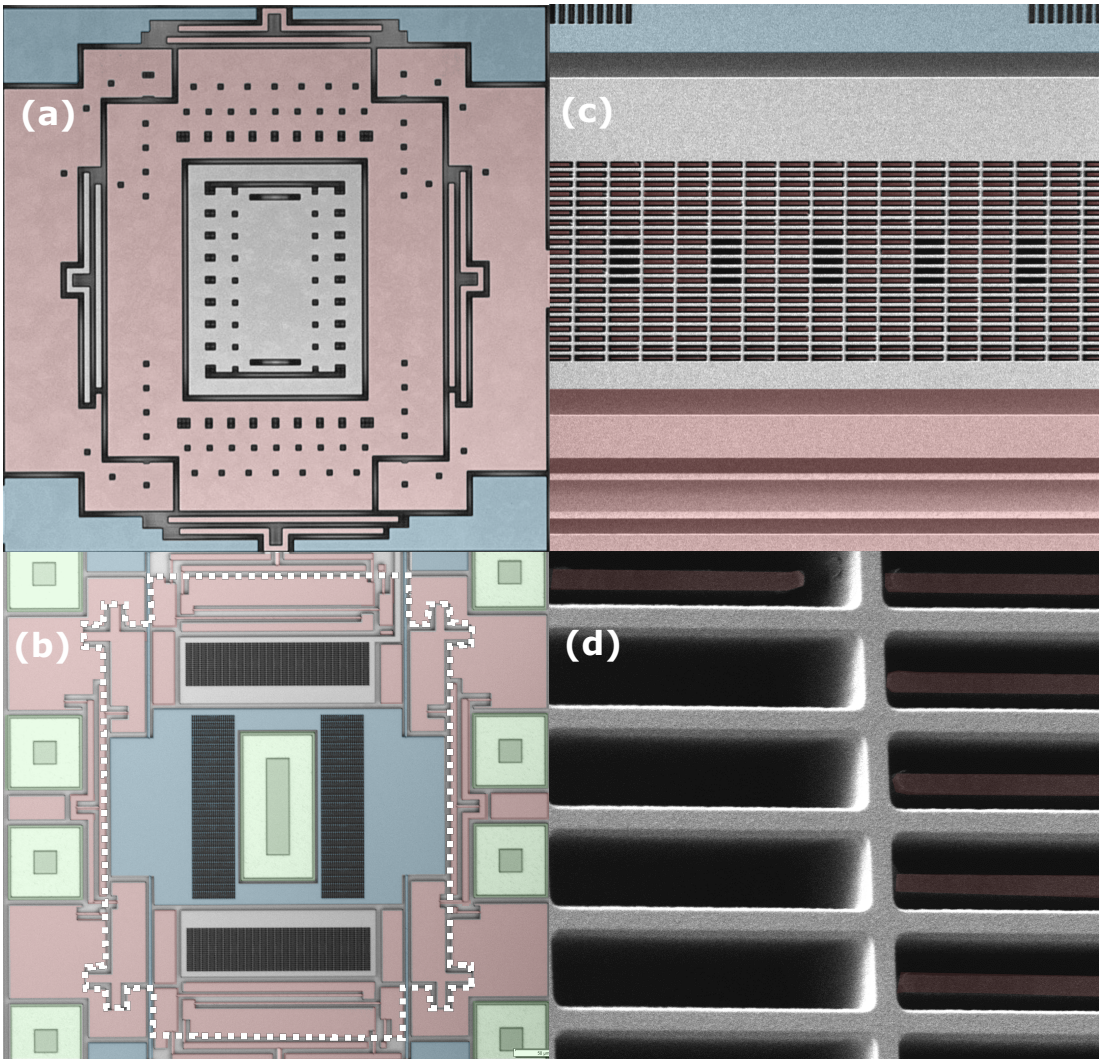
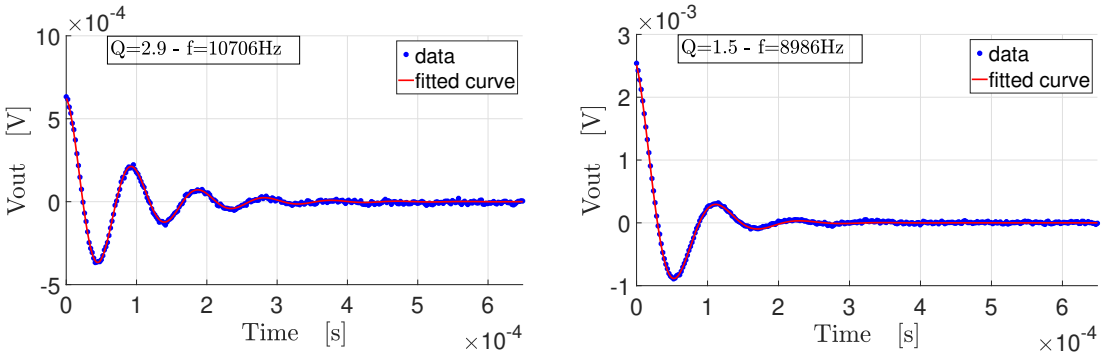


Figure 5.4: *SEM images of the device S-Z: (a) Top view of the device at the end of the process (b) Bottom view of the device before wafer bonding (c) Zoom on the suspended grid held by the central anchor point (d) Image of the comb-fingers region in the suspended grid. Image is food-colored in order to highlight the different polarity of the sensor: positively and negatively polarized areas of the device (red, jade-green), anchor points connected to substrate (green), central fixed electrode is not colored.*

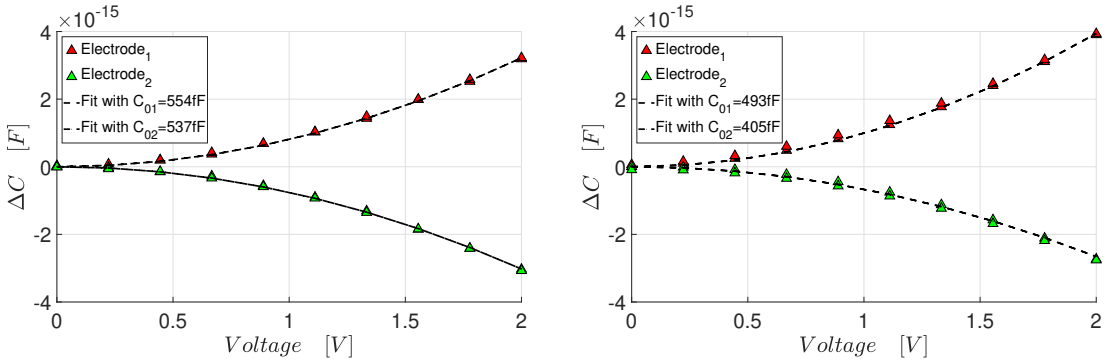
5.2 Wafer-level characterization

Wafer-level and die-level characterization are performed using the setup described in section 4.2 and 4.4. Figure 5.5 shows the ring-down measurement of the two sensors. The measured frequency is higher than expected for both accelerometers ($f_{0th} = 6266$ for M-Z and $f_{0th} = 4317$ for S-Z): a 70% and 100% discrepancy is observed for the M-Z and S-Z respectively.
The first explanation behind this discrepancy is the variation of inertial layer thickness (T). For in-plane accelerometers, both the springs stiffness and the mass of the device have a linear dependency with T. A variation of the inertial layer thickness does not cause a change in resonance frequency as the two terms cancel each other out. On the other hand, for out-of-plane sensors the two parameters are uncorrelated. This means that any variation of the inertial layer thickness leads to a change of resonance frequency. No direct measurement of T is available for these specific sensors, yet the later-shown $\pm 1g$ test suggests that the actual thickness value should be equal to 40 μm, partially explaining the observed resonance frequency.
The second explanation behind the measured frequency is related to variations in the springs geometry, as for instance the thickness of the partially etched springs. According to the analytical model used in the design section, a springs thickness of 3 μm, together with a reduced mass, could explain the error observed for the M-Z device. This would mean a 30% variation on the etching depth ($2\mu m$ instead of 3 μm) which is in line with SEM observations. A value of about 3.8 μm would explain the S-Z frequency variation. This value seems too high even considering large tolerances in the etching depth. In this case other geometric non-idealities might play a role, as for instance the change of the springs width.
The fact that the partial etch depth is smaller than expected is also confirmed by the observations performed on an out-of-plane sensor of type S-Z having only flexural springs and similar resonance frequency. For this type of device, the



(a) M-Z *(b) S-Z*

Figure 5.5: *Ring-down measurement for devices M-Z and S-Z.*

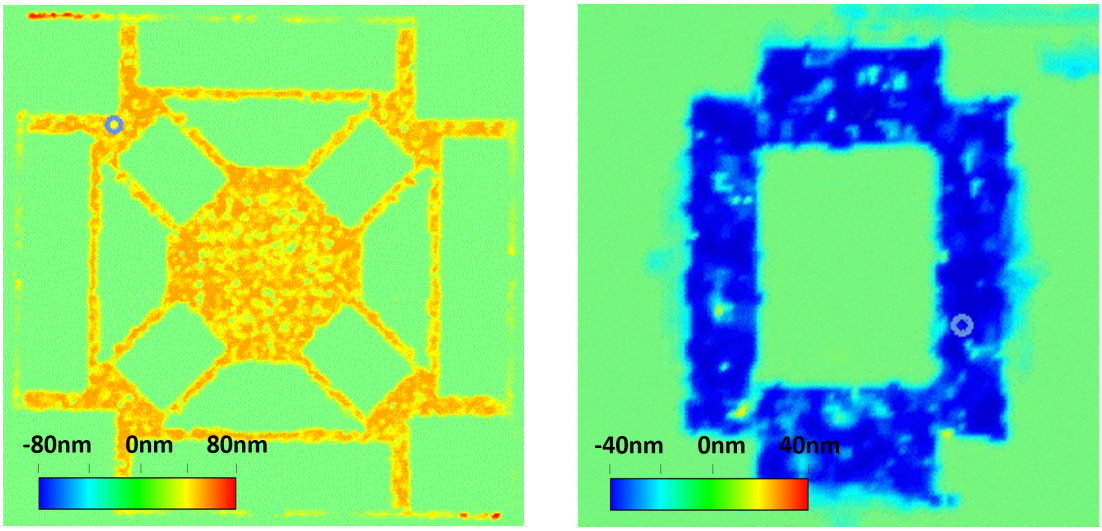


(a) M-Z *(b) S-Z*

Figure 5.6: *Capacitance versus voltage measurements for devices M-Z and S-Z.*

measured frequency was 2.4 times higher than the designed value. This is due to the fact that the flexural springs have a cubic dependency to the partial etch step and are therefore more sensitive than the torsional ones to process variations.
Figure 5.6 shows the C-V tests for both studied devices. The symmetry of the C-V curves can first be commented. The M-Z device shows good balance between the two electrodes, while for S-Z the two capacitors shows a 20% difference. The reason behind this asymmetry might be related to variation in the etching process depending on the silicon orientation. While the single-crystal fingers in the M-Z device are homogeneously distributed in the x and y direction for both electrodes, the S-Z device presents all the x-axis oriented fingers on one electrode and the y-axis oriented fingers on the other.
The second information given by the C-V curve is the capacitance value or the $\partial C/\partial x$. The measured static capacitance are equal to 1.091pF and 898fF for the M and S device, respectively. These values are about 10% higher than expected. However, as mentioned before, due to process variation, the real mass of the sensor is about 80% of the theoretical one. This leads to an overestimate of the stiffness and the static capacitance (Equation 4.2).

The last wafer-level test performed on the two sensors is a vibration test carried out with vibrometer model MSA-400 from Polytec. This equipment uses laser Doppler vibrometry in order to evaluate the velocity of the vibrating object. By integrating the velocity information also the device displacement can be computed. The two sensors were actuated with an electrostatic force at their resonance frequency. The actuating force was obtained by superposing an AC signal to a DC voltage in order to obtain a linear displacement [15]. Figure 5.7 shows two images from the interferometer measurement performed on two devices type M-Z and S-Z. For both structures the motion of the moving mass is indeed out-of-plane. The same displacement is measured on the entire structure proving a pure out-of-plane translation.



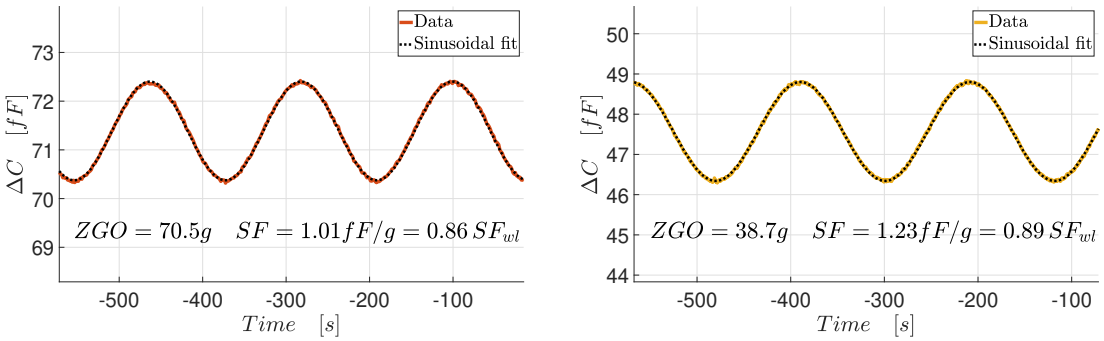
(a) M-Z *(b) S-Z*

Figure 5.7: *Doppler vibrometer measurement performed on M-Z and S-Z sensors in order to measure out-of-plane motion. The devices are actuated at resonance. The displacement of each device is represented according to the relative color scales. Both accelerometers show a pure translational movement.*

5.3 Die-level characterization

Scale factor

The $\pm 1g$ test was performed for both accelerometers and the results are presented in Figure 5.8. The data fit well the sinusoidal fit showing proper functioning the



(a) M-Z *(b) S-Z*

Figure 5.8: *Scale factor and ZGO evaluation for devices M-Z and S-Z. The actuation voltage (V_m) was set at 0.1V and 0.2V respectively. Devices were tilted at 2 dps leading to a sinusoidal acceleration of 5.5 mHz. A 4th order 200 mHz LIA filter was used to filter the signal.*

sensors. The measured SF is lower than expected according to wafer level tests. As mentioned before, this is consistent with an over estimation of the sensor mass. Indeed, assuming a proof mass thickness of 40 μm (instead of 50 μm) allows good match between the wafer and die level scale factors for both devices. SF of 1 and 1.2 fF/g are measured for the M-Z and S-Z devices, respectively. These values are lower than the designed one due to the undesired mechanical stiffening of the structures. The ZGO of the two devices is in the order to 71 and 50 fF, respectively. These values are not far from those measured for in-plane devices. Yet, the smaller SF of the out-of-plane sensors cause this capacitive offset to translate in a quite large ZGO. A re-design that could compensate the existing asymmetries or a larger SF would reduce this aspect.

Noise floor

Figure 5.9 shows the noise floor measurement of three sensors: the M and S devices presented so far and the S-Z with only flexural springs (S-Z-f). With respect to in-plane sensors, the noise of the sensor is evaluated according to the following formula:

$$S_B^{1/2} = \frac{\sqrt{S_{tot}(f_0) - S_e}}{Q} \tag{5.1}$$

.

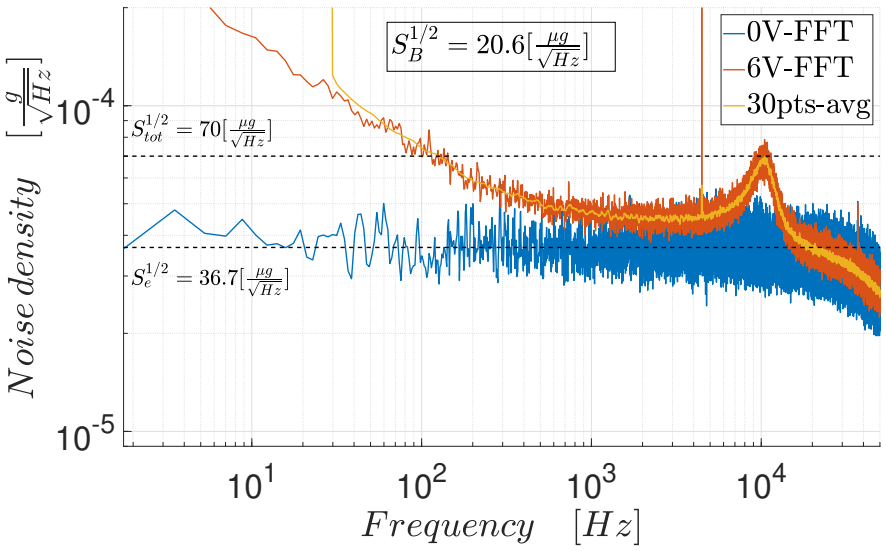
where $S_{tot}(f_0)$ is the noise power spectral density at the resonance peak, S_B and S_e are the Brownian and electronic noise respectively. In order to have a more accurate peak value the noise spectrum of the sensor is filtered using a moving average filter. It was observed that evaluating the noise in the flat area of the transfer function caused an over-estimate of the sensor noise likely due to the presence of low-frequency contribution visible in the images.

The reason behind this contribution is not clear. It could be partially due to ambient noise, but it could also be related to device problems such as for instance the presence of the residues in the comb-fingers. The actuation voltage used to extract the three measurements is different. The M-Z device showed linear behavior up to 6V, while for S-Z-f it was possible to reach 10V polarization. The plot shown for the standard S-Z comes from a preliminary measurement performed outside the anechoic chamber. For this reason only three volts polarization were used. Unfortunately the device failed before the final test.
The three plots show that the Brownian noise of the sensors was resolved. With respect to in-plane devices, the overall noise performance remain in the tens of $\mu g/\sqrt{Hz}$ due to the higher intrinsic noise of the devices (smaller mass) and higher electronic noise equivalent acceleration (smaller SF and lower actuation voltage). The frequency of the peak in the spectrum and its shape match with the expected resonance frequency and quality factor. The measured Brownian noise

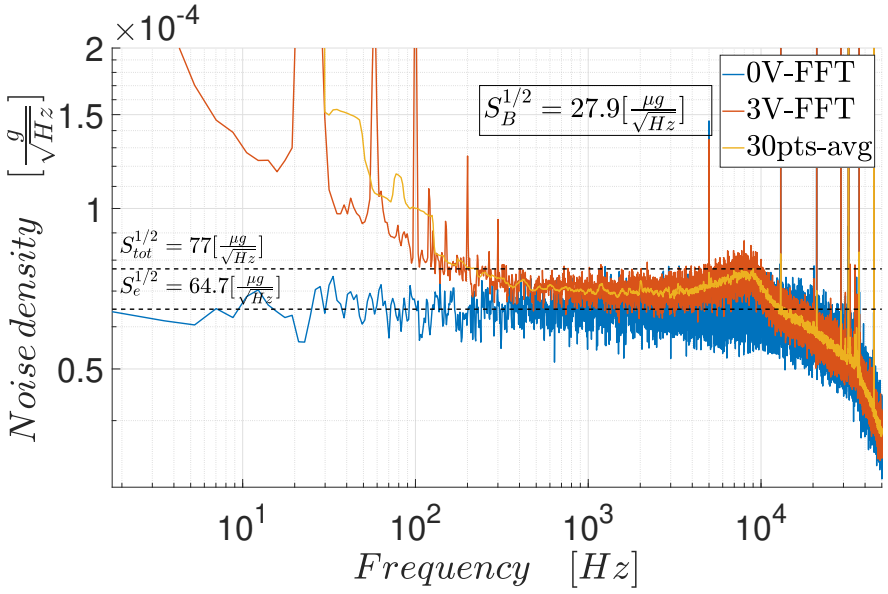
spectrum is compared to the theoretical value, re-computed taking into account the measured parameters as well as the reduced mass thickness.

$$S_{B-th}^{1/2} = \sqrt{\frac{4k_bT\omega_0}{mQ}} \tag{5.2}$$

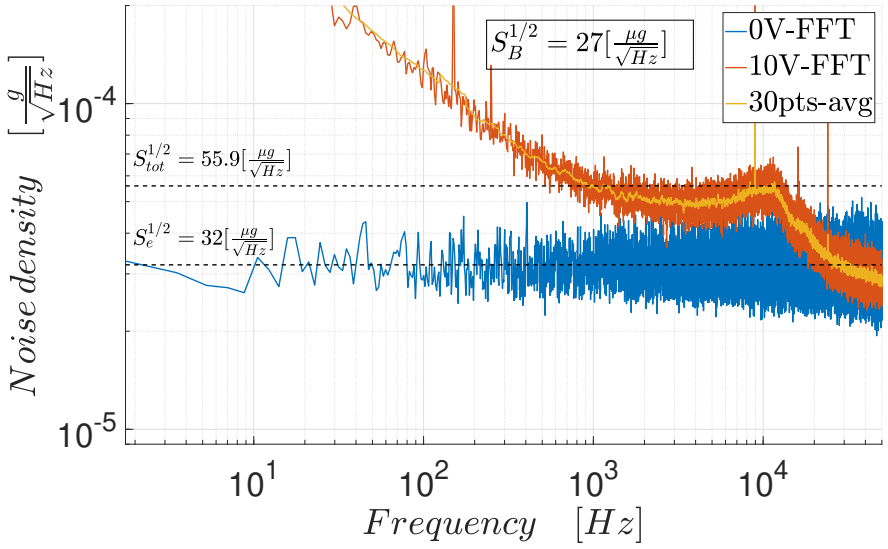
According to this equation, values of 21.5 and 28.5 $\mu g/\sqrt{Hz}$ are found for the M-Z and S-Z devices respectively. These values match the measured noise floor reported on the plots within a few percent. They also match the initial estimate reported in Table 2.7. The obtained devices show quality factor larger than 1, however the reduced thickness partially compensate this effect. Due to time constraints, it was not possible to test the FSR of the sensors. Moreover, their large stiffness would have allowed to verify only a small percentage of the travel range with our rate-table (10-20%). Based on the result from the linearity of in-plane sensors and safely assuming a 0.7 μm maximum displacement (i.e. half of the expected linear travel range), the M and S devices would display a FSR of 322 and 227 gravity units. These values together with the measured noise floors lead to a dynamic range of 137 and 130 dB respectively. This performance is obtained within footprints of 0.36 and 0.22 mm^2. Table 5.1 shows the comparison with recent works on out-of-plane accelerometers. The device displays resolution in line with a few prior sensors and potential FSR of at least an order of magnitude larger. This performance is achieved within a footprint that is 1.5 to 25 times smaller. Finally, it should be mentioned that implementing these sensors with a 100 μm inertial layer would further reduce the noise floor and extend the DR.



(a) *M-Z*



(b) S-Z



(c) S-Z-f

Figure 5.9: *FFT measurement for three type of Z-devices. As for in-plane sensor the electronic noise floor is evaluated with $V_m = 0$ while the total noise is obtained by polarizing the device $V_m > 0$. The device noise is extracted from the resonance peak value in order to avoid low-frequency noise contributions.*

Device	FSR $[g]$	Resolution $[\mu g/\sqrt{Hz}]$	DR (1Hz) $[dB]$	Footprint $[mm^2]$	BW $[kHz]$
This work	**≈ 227**	**70**	**≈ 130**	**0.22**	**≈ 8.8**
[70]	4	70	95	5.6	<12.7
[71] (Resonant accelerometer)	15	160	99	0.32	-

Table 5.1: *Comparison between performance obtained with novel fabrication and previous works found in literature*

5.4 Fifth chapter conclusion

In this chapter, the results from out-of-plane sensors have been presented. With respect to in-plane sensors, z-accelerometers are more subject to process non-idealities. The large notching induced by the etching of the thick-layers damages thin-layers structures such as springs and connections. In order to reduced undesired effects, the process thickness is reduced to 50 μm leading to a loss of performance. Yet, the process yield remains low, likely due to the presence of residues on the comb-fingers and variability in the release process. Wafer-level measurements show static capacitance in line with theory and resonance frequency a factor 1.5-2 higher than expected. This discrepancy is mostly due to variation in the partial etching of the thin layer (30% variation of the etching depth). The die-level tests suggest that the actual thickness of the mass is smaller than expected (20%) leading to a scale factor smaller than the wafer-level estimate. Finally, the noise floor evaluation shows how the sensors are more sensitive to high voltage with respect to in-plane sensors. Only one device could reach 10V of polarization. Despite all these problems, it was possible to measure a noise floor of less than 80 $\mu g/\sqrt{Hz}$ for a device with theoretical FSR of more than 220g, large resonance frequency and a total footprint of 0.22 mm^2. Such performance are in-line or better of device implemented with larger footprint or with other techniques which offer large DR (resonant accelerometers). In the future the noise floor of the sensor could be reduced by at least a factor 5, by implementing the sensor in a 100 μm inertial layer, reducing the size of gap and lowering the resonance frequency. Such sensor would have performance in line with the in-plane accelerometers and even smaller footprint.

Conclusions

In this work a novel multi-layer fabrication concept for MEMS inertial sensors was presented and demonstrated with a 3-axis accelerometer. The multi-layer process enables the following features: (i) a thick inertial layer that allows the reduction of the Brownian noise floor and the increase of the device stiffness for a given resonance frequency (ii) a thin layer that allows the fabrication of capacitive units with sub-micrometric size, enabling large capacitive density and 3-axial surface-variation detection. Several families of devices were presented, however only the design flow and the characterization of the most compact devices are shown in details. These sensors have been designed in order to achieve $\mu g/\sqrt{Hz}$ resolution and large FSR within a consumer footprint, enabling large dynamic range with small area consumption. The main goal of such design was to prove that the trade-off between size and dynamic range could be overcome when moving from a single-layer fabrication to a multi-layer one. The design of the sensors was performed with analytical modeling and FEM simulations. Both the mechanical behavior and the linearity of the transduction process were studied.
A few critical aspects were encountered during the fabrication of the sensors. These aspects did not influence the yield and performance of in-plane sensors while they had strong effect on out-of-plane accelerometers. The notching of the thick-layer etching coupled to the strong lag effect caused most of the z-axis sensors to fail. This forced a reduction of the process thickness and relative loss of performance for this type of sensors.
The characterization of the sensors was performed both at wafer-level and at die level. The die-level measurements were carried out with a dedicated electronic circuit implemented with discrete components, developed during this work. The circuit is composed of a differential charge amplifier followed by an instrumentation amplifier. The polarization of the MEMS device is performed with an external lock-in amplifier that acts also as demodulator. This configuration was chosen among several different readout schemes, as it offers the best noise performance already at low modulation frequency.
In-plane accelerometers showed static capacitance and resonance frequency in line with theory. They achieved resolution smaller than 9 $\mu g/\sqrt{Hz}$ and full scale on the order of 160g. These aspects together lead to a dynamic range of more than 145dB for a device with a footprint of only 0.24 mm^2. These results are

achieved while keeping a large bandwidth and working with an open-loop readout. With respect to previous works on large DR accelerometers, the new devices show similar or better dynamic range (up to 10dB improvement) while keeping large bandwidth and reducing the footprint by almost two orders of magnitude. Out-of-plane sensors showed resonance frequency higher than expected due to fabrication tolerances. The devices had both smaller mass and thicker springs explaining the observed mechanical behavior. Despite the loss of scale factor due to the larger resonance frequency, these sensors achieved resolution ranging from 50-80 $\mu g/\sqrt{Hz}$. Again, such performance was obtained while keeping large resonance frequency (>8kHz), small footprint (down to 0.22 mm^2) and a potential full-scale of more than 200g. The obtained resolution is in-line with z-accelerometers from recent works, yet it is achieved with a footprint reduction by a factor 1.5-25 and a FSR improvement of more than an order of magnitude.

Future development

In the future, most of the fabrication problems could be solved by changing the fabrication method or by re-designing the devices. Concerning the thin layer fabrication the following improvement could be obtained: (i) the voids in the combs could be avoided with two different solutions. First, by splitting the deposition process in two subsequent steps, a slow step to fill the trenches and a fast step to grow the rest of the epitaxy. Second, by inverting the process order i.e. depositing oxide on a etched silicon layer in order to fill the trenches and then, after CMP, cover the oxide-silicon layer with a Si-epitaxy (damascene); (ii) the residues on the partially etched combs could be reduced by designing longer electrodes. The residues are found mostly on the short side of the combs perimeter, increasing the length with respect to the width would reduce the total area of residues; (iii) finally, the accuracy of the partial etch could be improved by tuning the etching time enabling more accurate resonance frequency.
Regarding the thick-layer, these are the possible improvements: (i) the lag effect could be reduced by designing structures with more homogeneous openings and by better tuning of the etching time; (ii) a larger margin should be taken between the thin layer structures and the thick layer openings. This way the notching would not damage the thin-layer features.
Solving the fabrication issues would allow to implement z-axis accelerometers with 100 μm thick layer, aligning the performance of out-of-plane sensors to that of in-plane one and leading to a high-performance 3-axis accelerometer. This type of sensor could address the demand of emerging applications for high-stability, low-noise and large DR accelerometers within consumer footprint, as for instance mixed reality and inertial navigation. Regarding this aspect, while the first design focused on optimizing the noise and dynamic range performance, no design choice was taken to improve the offset stability of this type of sensors. Yet, in a future design, the large scale factor and the possibility of increasing stress iso-

lation by anchor points reduction, could lead to improved offset-stability with respect to existing sensors.
Finally, the proposed technology offers a fabrication platform for inertial MEMS sensors and actuators. New design possibilities and great potentialities have been demonstrated with the first fabricated accelerometers. In the future this new concept could be applied to several other types of MEMS, like gyroscope or micro-mirrors.

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Acronyms

ASIC Application Specific Integrated Circuit. 7, 10–12, 62

BN Brownian Noise. 11, 41, 43, 48, 55, 91

C-V Capacitance-voltage profiling. 81, 102

CD Critical Dimension. 13, 21, 24, 37

CMP Chemical Mechanical Planarization. 19, 21

CMRR Common Mode Rejection Ratio. 68, 70, 71

DR Dynamic Range. 40, 41, 43, 48, 55, 91, 105, 107, 110

DRIE Deep Reactive Ion Etching. 19, 21, 24, 57, 77, 78, 97, 98

FEM Finite Element Method. 40, 43, 44, 53, 55, 56, 109

FFT Fast Fourier Transform. 90–94, 106

FSR Full Scale Range. 11–13, 32, 34, 38, 39, 41, 43, 48, 55, 57, 88, 90, 93, 105, 109

INA Instrumentation Amplifier. 73, 74

LIA Lock-In Amplifier. 74, 82, 87, 103

NL Nonlinearity. 11, 32, 55

PCB Printed Component Board. vi, vii, 73, 74, 76, 86, 90

SEM Scanning Electron Microscope. 15, 45, 77–80, 95–99, 101

SF Scale Factor. 40, 43, 48, 55, 81, 84, 86, 87, 104

ZGO Zero-g Offset. 86–88, 103, 104

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