Back-gate feedback for auto-calibration of analog and mixed cells in UTBB-FDSOI technology

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UNIVERSITÉ CÔTE D'AZUR

ÉCOLE DOCTORALE
SCIENCES ET TECHNOLOGIES DE L'INFORMATION ET DE LA COMMUNICATION

THÈSE DE DOCTORAT

Auto-Polarisation de la Grille Arrière pour Auto-Calibration de Cellules Analogiques et Mixtes en Technologie UTBB-FDSOI

Zhaopeng WEI

Polytech'Lab

Présentée en vue de l'obtention du grade de docteur en Electronique **d'**Université Côte d'Azur
Dirigée par : Gilles Jacquemod
Soutenue le : 24 mai 2019

Devant le jury, composé de :
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Jury :

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Glossaire

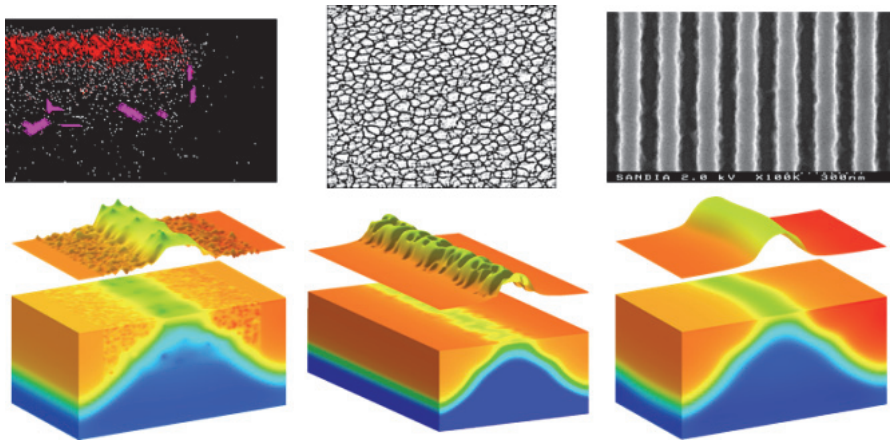
Pour faciliter la lecture du manuscrit, nous rappelons dans le tableau ci-dessous les acronymes les plus utilisés. Ils sont également décrits lors de leur première utilisation dans ce mémoire.

ADC	Analog to Digital Convertor (or DAC : Digital to Analog Convertor)
ADPLL	All-Digital PLL
BG	Back-Gate
BJT	Bipolar Junction Transistor
CDR	Clock and Data Recovery
CP	Charge Pump
DCVSL	Differential Cascode Voltage Switch Logic
DIBL	Drain Induced Barrier Lowering
DPLL	Digital PLL
DVFS	Dynamic Voltage Frequency Scaling
ECL	Emitter-Coupled Logic
FDSOI	Fully Depleted Silicon On Insulator
GIDL	Gate Induced Drain Lowering
ISF	Impulse Sensitivity Function
LER	Line Edge Roughness
LFSR	Linear-Feedback Shift Register
LPF	Low-Pass Filter
LPLL	Analog or Linear PLL
LPT	Linear Phase Time
LTI	Linear Time Invariant
LVT	Low Voltage Transistor (Low V_{Th})
PD	Phase Detector
PDF	Probability Density Function
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PN	Phase Noise
QVCO	Quadrature VCO
RDF	Random Dopant Fluctuations
RMS	Root Mean Square
RO	Ring Oscillator
RVT	Regular Voltage Transistor (Regular V_{Th})
TOx	Thickness Oxide
SCE	Short Channel Effect
SNR	Signal to Noise Ratio
UTBB	Ultra-Thin Buried Box
VCO	Voltage Controlled Oscillator
VCRO	Voltage Controlled Ring Oscillator
V_{Th}	Threshold Voltage

General introduction

1. Introduction

The continuous increase for over 40 years of the performance of microelectronics technology is made possible by miniaturization of elementary components. The prediction of Gordon Moore [1], known as Moore's law (the density of transistors on a chip doubles every 18 months), proved to be uncannily accuracy, partly because the law was the keystone in long term planning in the semiconductor industry for research and development. However, the traditional MOS bulk transistor reaches its limits: short channel effect (SCE) and drain induced barrier lowering (DIBL), lowering of the threshold voltage (V_{th}) and slowing down of the decrease of the supply voltage Vdd, more power dissipation, less speed gain, less accuracy, variability and reliability issues, ... As shown in Figure 1, this is mainly the result of random fluctuations in the number of doping (RDF: random dopant fluctuations, cf. Figure 1.a) in the channel region, the roughness of the photolithography (LER: Line Edge Roughness, cf. Figure 1.b), and to a lesser extent, among other things, the variation in oxide thickness (TOx: Thickness Oxide, cf. Figure 1.c) [2].



(a) RDF (b) LER (c) TOx

Figure 1: Different sources of variability [2]

To overcome these problems induced by the increasingly aggressive technological nodes of 28nm and beyond, two solutions have adopted transistors whose channel is not doped [3] like the FinFET [4] and FDSOI [5] technologies. However, these technologies were initially designed for digital applications, so we can ask whether these transistors are suitable for analog and RF circuits? Moreover, while the digital blocks continue to follow Moore's law (i.e. to decrease area), this is not the case for analogue circuits and especially for passive components (cf. Figure 2) [6]. Decreasing the analogue part and removing the passive components of a complex chip system reduces the total area

of the circuit, or even its consumption. For example, ring oscillators (oscillators without passive elements like inductors and capacitors) are known to present high phase noise, but this design aggressively tackles the size and reduction of energy consumption. We propose, by the possibility of the bias of the back-gate offered by FDSOI technology, to compensate for variability, short channel effects ... in order to increase the performance of such circuits.

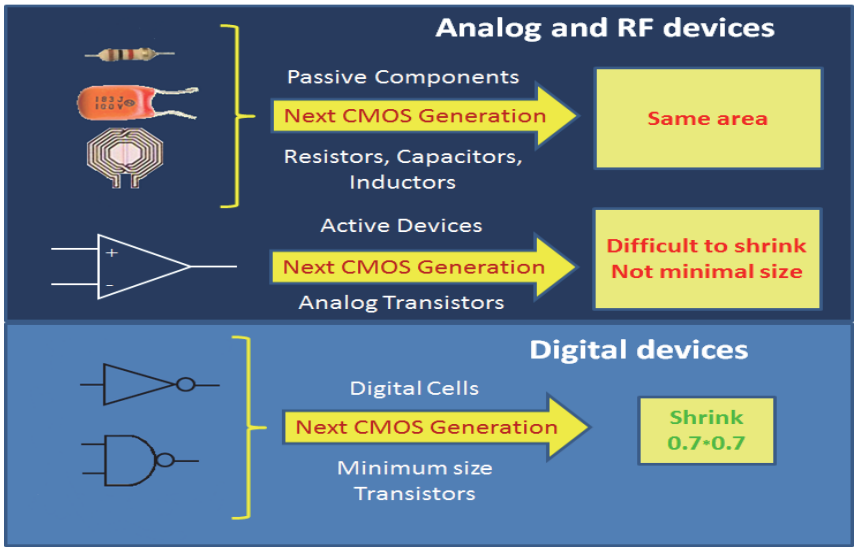


Figure 2: Area reduction problems for analogue components

2. Objectives et motivation

In the competition of the miniaturization of integrated electronic circuits, it now seems to be assumed that UTBB-FDSOI (Ultra-Thin Body and Buried oxide Fully Depleted Silicon on Insulator) technologies are better suited to nanometric sizes. Indeed, they can limit the problems due to random variations of the doping used in conventional transistors of the "bulk" type and make a significant improvement in terms of performance and low power design. The thesis work presented here makes a significant contribution to the development and design of new basic blocks for the design and realization of a phase-lock loop (PLL) using the logic in 28nm FDSOI technology. Thanks to the latter, we have proposed a complementary inverter based on a pair of inverters with cross-coupling of the back-gates providing output of symmetrical and complementary signals. This concept can be extended to all digital cells to generate more stable, symmetrical and resilient output signals. First we designed an oscillator in fast and efficient rings composed by four complementary inverters delivering quadrature quality clocks with a measured oscillation frequency of 2.3GHz.

Then, using the complementary logic and control of the back-gate of this technology, we propose an effective solution to design new structures of VRCO, charge pump based on a new

topology of current mirror, PFD, divisor etc., which are the basic elements of high-speed and low-noise PLL. All these designs have been simulated and verified under Cadence. In addition, a test chip composed by complementary inverter, RO, current mirror and VCRO has already been made in silicon and tested, validating all our work.

3. Thesis work

The present dissertation is composed of 5 chapters, framed by a general introduction and a conclusion including some perspectives for improvement and trends. At the end of the manuscript there are also some annexes, as well as all the publications related to this thesis work.

In the first chapter, we present the limits reached by the classic bulk MOS technology and the announced end of Moore's law. For 22nm technology nodes and beyond, the transistor channel is no longer doped, either for FinFET or UTBB-FDSOI transistors. The main features of the FDSOI technology are then described as well as these advantages and applications. To illustrate the latter for analogue designs, our choice has been to design a phase-locked loop (PLL). The operating principle and characteristics of a PLL are given also in this chapter. The focus is on jitter and phase noise, generally low point of ring oscillators (RO). The aim of this thesis is to take advantage of the FDSOI technology to propose a new structure of RO in order to reduce jitter while continuing to limit the consumption and the area of the final circuit.

The second chapter is dedicated to complementary logic. We describe the difference between differential logic and complementary logic, before presenting the implementation of a complementary inverter in FDSOI technology. The innovative structure of such an inverter is based on the crossing of the back-gates of each inverter to mirror the complementary output signals. The objective of this structure is to limit the switching noise and to offer identical propagation times between the two inverters in order to limit the jitter of a ring oscillator made from these complementary inverters. A static and dynamic study allows to validate this concept and optimize the size of transistors. This concept is then extended to all digital logic gates and an example of a clock generator is proposed.

In the third chapter, we describe the theory of oscillators with a focus on the basic topologies of ring oscillators (RO). We show in particular that the complementary inverters allow to realize quadrature oscillators with a very simple design. A thorough study of this architecture allows to investigate the advantages and limitations. Again, this study also allowed us to optimize the sizing of transistors and to evaluate the performance of the RO, by SPICE simulations.

Chapter four describes all the basic blocks of a PLL, namely the VCRO, the phase detector (PD and PFD), the charge pump and the frequency divider. For each block, basic topologies are described, and then adapted to our concept of complementary logic implemented in FDSOI technology. SPICE simulations allow each time to optimize the size of the transistors and to evaluate the performance of the circuits. A special effort has been made in the design and realization of the new structure of the current mirror which allows to limit the short channel effects while drastically decreasing the size of the transistors. To conclude this chapter, a high-level simulation, based on the NAPA Simulator, validated the PLL topology build from these basic blocks.

The final chapter is dedicated to the realization of a test circuit in FDSOI technology. We present the realization of the layout design, then the one of the final circuit implementing all the basic blocks in order to test them separately to the VCRO. The entire PLL was not realized. All the measurements carried out are present in this chapter and allow to validate the concept of complementary logic using the crossover of the back-gates of the UTBB-FDSOI transistors. The results, in terms of performance, are very promising for the continuation of this work.

Finally, general conclusions and some perspectives end this manuscript. Publications related to this thesis work are also presented, followed by a few annexes.

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Chapter I – FDSOI technology and PLL

1. Introduction of FDSOI technology

1.1. End of Moore Law

In 1958, Jack Kilby from Texas Instruments invented the first integrated circuit (IC) composed of a simple flip-flop with two bipolar transistors on a single chip of germanium, thereby initiating the "Silicon Age". Early ICs used bipolar junction transistors which suffer from more static power dissipation problems. In 1959, the first metal–oxide–semiconductor field-effect (MOSFET) transistor was realized by Kahng Dawon from Bell Labs. Because of its low power, reliable performance and high speed, CMOS technology composed by MOS transistors replaced bipolar technology for all digital applications and plenty of analog applications. Both IC and MOSFET create together a grand "micro world" (cf. Figure 1.1).

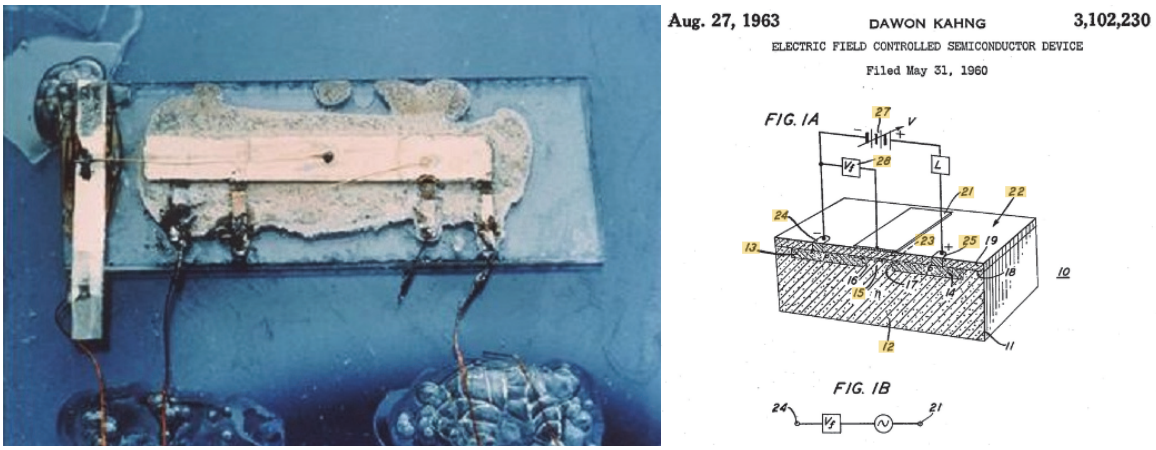


Figure 1.1: The first integrated circuit by Jack Kilby and the first MOSFET by Kahng Dawon [1] [2]

In the past few decades, the integrated circuits and the semiconductor industries have been experienced a rapid development. The size of transistors is getting smaller and smaller, the degree of IC integration is getting higher and higher and the number of integrated circuits has increased rapidly. From the beginning a transistor has a big size of centimeters until now a fingernail-sized CPU integrates more than billions of transistors. The size scaling and CMOS process technology improvements continue to increase circuit speeds. Moreover, with the help of chip packaging technology, the price/performance ratio of CMOS-based microelectronics products is further improved.

In a word, the development of microelectronics technology improves our daily lives.

Gordon Moore predicted in 1965, known as Moore's Law: the complexity for minimum component costs has increased at a rate of roughly a factor of two per year [3]. After corrected that the density of transistors on a chip doubles every 18 months by Intel executive David House, Moore's Law has proven to be uncannily accurate according to the statistics of International Technology Roadmap for Semiconductor (ITRS) (cf. Figure 1.2). Moore's Law has always been an important leading target for semiconductor industry research and development planning.

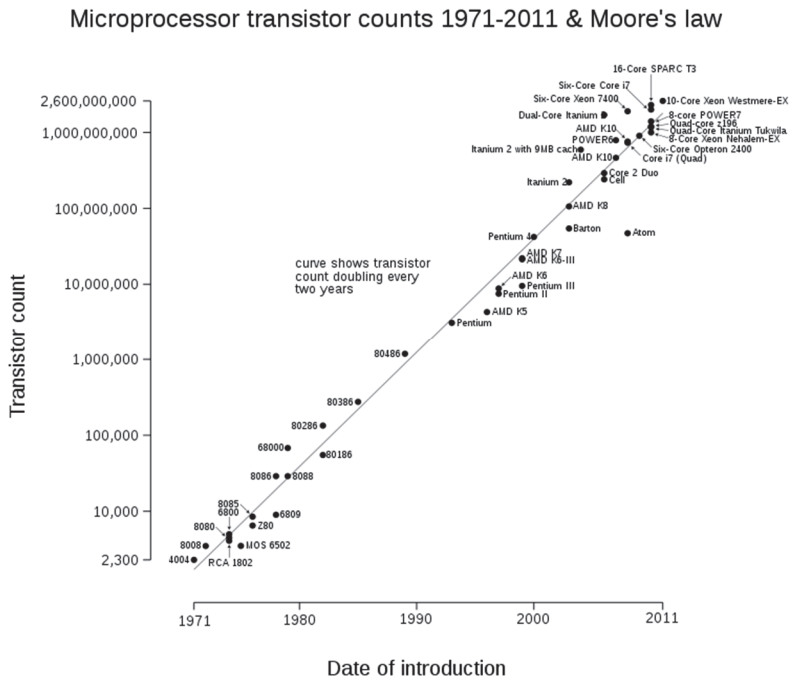


Figure 1.2: Moore's law and number of transistors in Intel microprocessors

However, in recent years the development of integrated circuits is likely to be not kept up with the trend of Moore's Law. The traditional bulk MOS transistor cannot continue to shrink below 32nm technology node due to various limitations encountered: Sub-threshold Slope (SS), Short Channel Effect (SCE), Drain Induced Barrier Lowering (DIBL) (cf. Figure 1.3), Threshold Voltage (V_{Th}) and Vdd scaling slowing down, more power dissipation, less speed gain, less accuracy, variability and reliability issues.

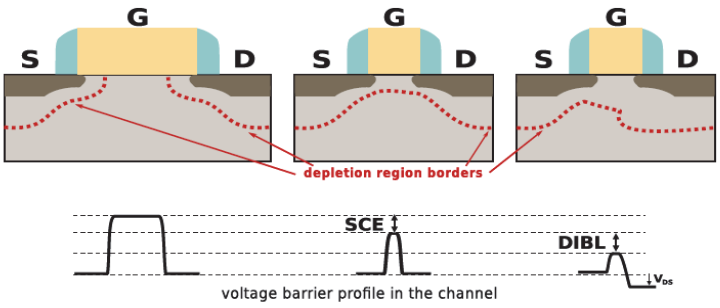


Figure 1.3: SCE and DIBL effects

Moreover, random dopant fluctuation problem is a big challenge for traditional bulk MOS transistors because they should rely on doping n+ electrons or p+ holes to improve the electronic characteristics. However, channel doping based on random distribution of small concentration of dopants is an inevitable hit by the technology scaling of bulk MOS Transistor. As show in Figure 1.4, as the size is scaled to tens of nanometers, the number of dopant atoms is few even can be counted on finger. In fact, the channel region has only about 50 atoms of dopants at 22 nm node.

a side of	# atoms Dopants
100 nm	3 000
50 nm	390
20 nm	25
10 nm	3
5 nm	0.390
2 nm	0.0250
1 nm	0.003

a side of	# atoms Si
100 nm	27 000 000
50 nm	3 400 000
20 nm	220 000
10 nm	27 000
5 nm	3 400
2 nm	220
1 nm	27

Figure 1.4: Atoms dopants and atoms Si scaling

We expect a lot of variability between adjacent transistors on the same die and the dopant variation will cause directly a threshold voltage mismatch between adjacent transistors (V_{Th} variability). Other materials may be taken as the base to reduce the introduction of doping. But one of the main points is the manufacturability, which can be summarized by the ability to create profitable IC's. Up to now, the industrial solutions are focus on silicon CMOS technology.

We can notice from Figure 1.4 that as the channel size scales, the Si atom still has a large amount. So, undoped channel transistor is a good solution for 28 nm node and beyond. FinFET and UTBB-FDSOI technology are two silicon technologies which have undoped transistors and only rely on work functions of the metal gate electrode.

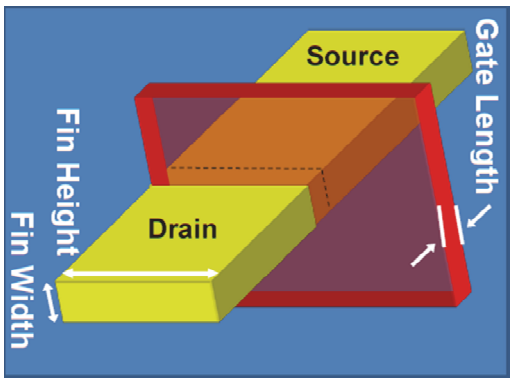


Figure 1.5: Double-gate FinFET structure [5]

Fin Field-effect transistor (FinFET) [4] is a MOSFET built on a substrate where gate controls a thin body from more than one side of the channel, forming a double gate structure as shown in Figure 1.5. Different from conventional bulk MOS transistor, the gate structure in FinFET is wrapped around the channel and the body is thin, providing better SCEs, it means that FinFET suffers less from dopant-induced variations.

In bulk MOS transistor, the channel is horizontal; while it is vertical in FinFET. So for FinFET, the height of the channel (Fin) determines the width of the transistor. The total width of the channel is given by Equation 1.1:

$$\text{Width of Channel} = 2 \text{ X Fin Height} + \text{Fin Width} \tag{1.1}$$

FinFET technology provides higher drive current for a given transistor footprint, hence lower gate delay, lower leakage, no random dopant fluctuation, hence better mobility and scaling of the transistor beyond 28nm. FinFET chips have already utilized in today's commercial chips at 22 nm and below for digital applications.

Nonetheless, FinFET technology suffers from complex manufacturing process, and its supply voltage is difficult to shrink below 0.7 V. So, it is not suitable for flexible analog circuit design.

UTBB-FDSOI technology is a good choice for analog & RF design, especially for low power applications, which we will introduce in the next section.

1.2. Overview of FDSOI technology

Contrary to FinFET technology, Fully Depleted Silicon on Insulator (FDSOI) technology is a planar process technology that delivers the benefits of reduced silicon geometries while containing the complexity of the manufacturing process. Compared to classical bulk MOS transistor technology, FDSOI technology brings a significant improvement in terms of performance and low power design at 28nm node and beyond [6]. Its strength comes from two major innovations as shown in Figure 1.6.

First, an ultra-thin layer of insulator about 25 nm, called the buried oxide (BOx), is positioned on top of the base silicon. Secondly, a very thin silicon film about 7 nm implements the transistor channel. Thanks to its thinness, there is no need to dope the channel, thus making the transistor fully depleted. The combination of these two innovations is called "ultra-thin body and buried oxide fully depleted SOI" or UTBB-FDSOI [7].

As shown in Figure 1.7, the buried oxide separates the conductive channel and substrate. There is no current leakage from channel to substrate which greatly reducing the leakages. Thin Si-

film helps to improve the electrostatic control, resulting in high speed at low voltage. Moreover, the body being fully depleted, the random dopant fluctuation that plagues bulk CMOS is reduced which helps to lower minimum usable supply voltage.

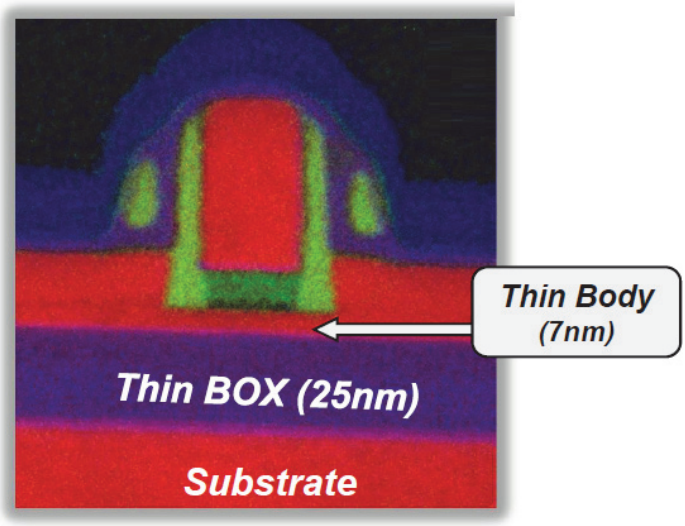


Figure 1.6: Electron micrograph for ultra-thin body and buried oxide

Figure 1.7: From Bulk-MOS Transistor to UTBB-FDSOI transistor (Source: ST.com)

Power/performance claims of 30% to 40%, versus classical Bulk, are not uncommon and FDSOI is already in production at 28 nm and is positioned as an alternate option to bulk 20nm. FDSOI transistors correspond to a simple evolution from conventional MOS transistor. One of the main features of this technology is the possibility to vary the threshold voltage (V_{Th}), using the back-gate structure of UTBB-FDSOI transistors. Figure 1.8 presents the back-gate contact and Figure 1.9 gives the influence of the back-gate biasing on the V_{Th} variation[8]. It shows that we have more possibility to control V_{Th} in UTBB-FDSOI technology.

Concern on the process variation on aggressive mode for FDSOI: As the technology scales down into deca-nanometer range the variation of the threshold voltage (V_{Th}) becomes an ever-larger problem. These phenomena are captured by the Pelgrom coefficient (AVT) [9][10] used to define the V_{Th} variation for each transistor. The standard deviation of the V_{Th} variation is given by relation 1. As

shown in Figure 1.10 [11], the A_{VT} for 32 nm bulk CMOS is over 2.5-3.5 mV.µm. For UTBB-FDSOI transistors, the A_{VT} is at 1.1 mV.µm and 1.25 mV.µm for 32 nm and 22 nm nodes respectively, mostly due to an undoped channel and hence a significantly limited influence of RDF [12].

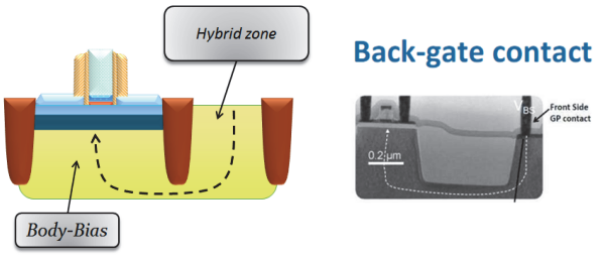


Figure 1.8: Back gate biasing possibility [7]

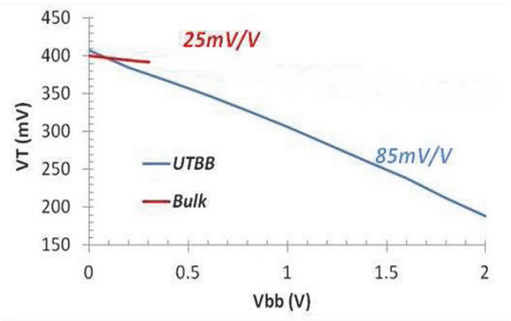


Figure 1.9: V_{Th} variation versus BG biasing [7]

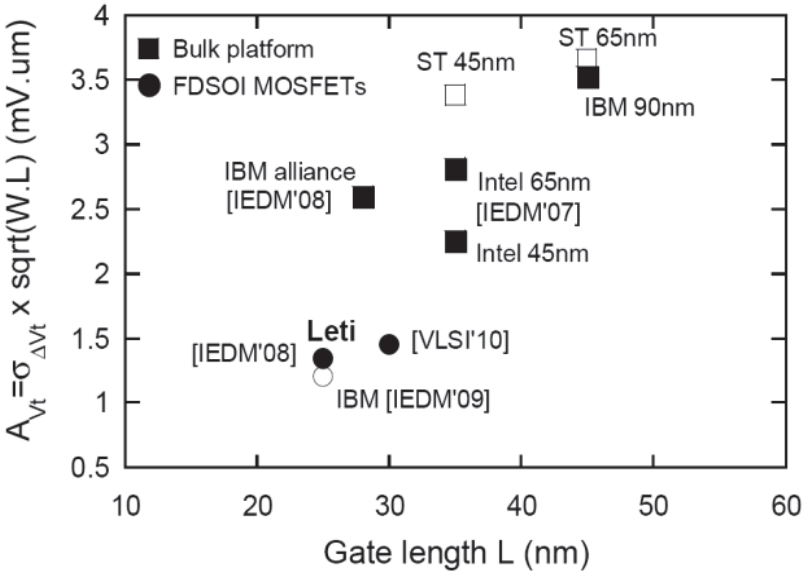


Figure 1.10: Pelgrom coefficient versus gate length [11]

The standard deviation on the threshold voltage due to the process variations between a standard CMOS bulk technology and a FDSOI technology is given by the following equations (Equation 1.2 to 1.4).

$$\sigma_{V_{Th}} = A_{Th}\frac{1}{\sqrt{WL}} = \frac{\sqrt[4]{2\varepsilon_s\varepsilon_0 q^3 N_a \Phi_d}}{\varepsilon_{ox}\varepsilon_0} T_{ox}\frac{1}{\sqrt{WL}} \quad (1.2)$$

$$\sigma_{V_{Th}} \propto N_a^{0.25} with \begin{cases} N_{a_{Bulk}} \approx 1E18\ cm^{-3} \\ N_{a_{SOI}} \approx 1E16\ cm^{-3} \end{cases} \quad (1.3)$$

$$\frac{\sigma_{V_{VTh_{SOI}}}}{\sigma_{V_{Th_{Bulk}}}} \approx \frac{1}{3} \quad (1.4)$$

Concern on UTBB FDSOI Transistors: Since UTBB-FDSOI transistors use undoped silicon films for the channel, the implant techniques from classical bulk CMOS technology are not relevant. However, the threshold voltage planar UTBB-FDSOI transistors could be set using other methods such as controlling the gate stack work function, trimming the gate length, counter-doping, body-well doping and other methods. The official starting offer of the STMicroelectronics UTBB 28 nm FDSOI technology consists of NMOS and PMOS transistors with two types of threshold voltage, V_{Th}:

Regular V_{Th} (RVT) mode for low-power (LP) applications, as shown in Figure 1.11 and low V_{Th} (LVT) mode for high-performance (HP) applications, as shown in Figure 1.12.

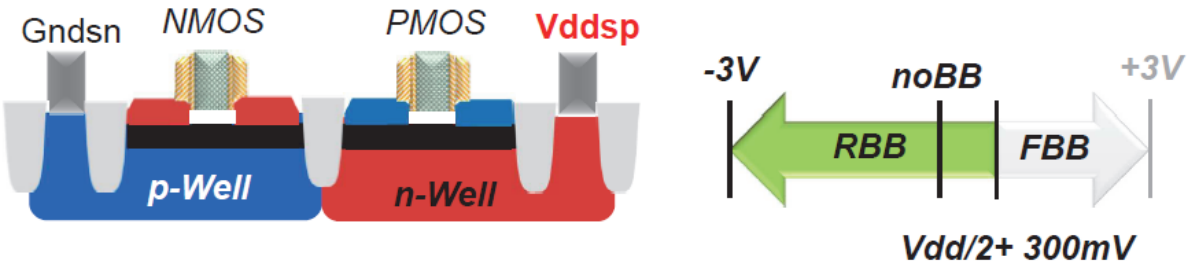


Figure 1.11: Conventional well architecture in UTBB-FDSOI for LP RVT transistors [13]

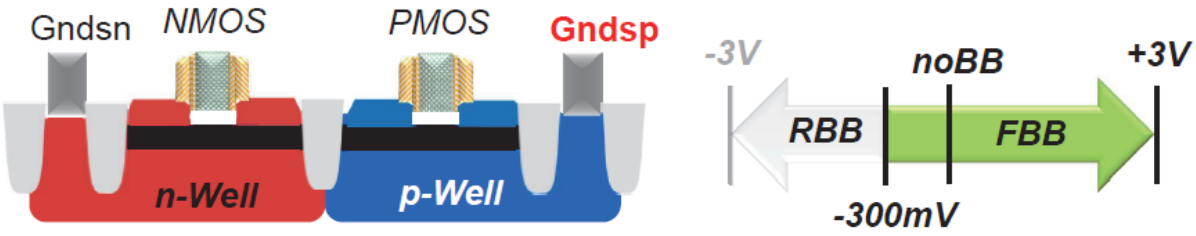


Figure 1.12: Flip-well architecture in UTBB-FDSOI for HP LVT transistors [13]

The RVT transistors keep the same layout of a planar bulk CMOS, an n-well underneath PMOS and a p-well underneath the NMOS. The lower V_{Th} needed for high-performance designs is achieved by exchanging places of an n-well and a p-well, making PMOS laying in a p-well and NMOS in an n-well. Because of the chosen well-schedule, the RVT transistors allow full reverse body biasing (RBB) with only slight forward body bias (FBB) capabilities, while it is opposite for the LVT transistors: full FBB up to 3V or more is possible to apply but only limited amount of 300mV of RBB.

The LVT type is often referred as a flip-well and its chosen well-schedule made available one more functionality called dynamic threshold MOS (DTMOS). This means that gate and back-gate of the transistor can be bind together and when the gate is turned ON the threshold voltage is reduced with FBB providing minimal on-resistance per area. FBB mode provides an extremely powerful technique to optimize performance and power consumption. Easy to implement, FBB can be modulated dynamically during the transistor operation, bringing a great flexibility for designers and

letting them design their circuits to be faster when required and more energy efficient when performance isn't as critical.

It is noticed that in bulk technology the body bias range is limited to -300mV in the RBB case due to gate-induced drain lowering (GIDL) constraints, and to +300mV in the FBB case due to the source-to-drain leakage at the junctions as well as the increased risk of latch-up at high voltage and temperature. Contrarily, the body bias range spans from -3V for the RBB case up to 3V for the FBB case in UTBB FDSOI technology, as shown in Figure 1.13. This is mainly aided by the total dielectric isolation of the source and drain provided by the BOX.

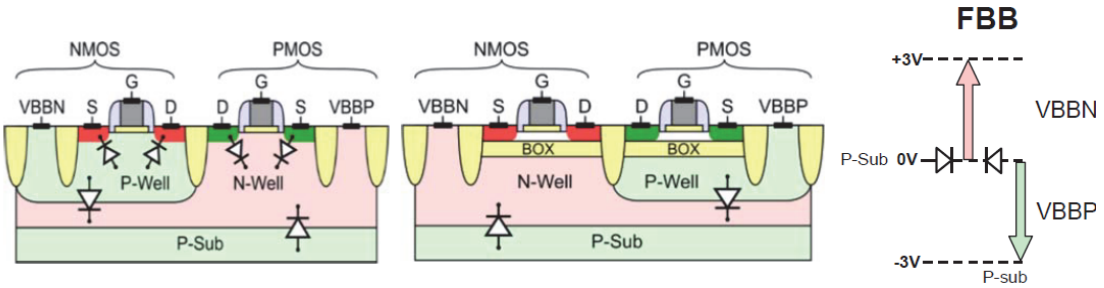
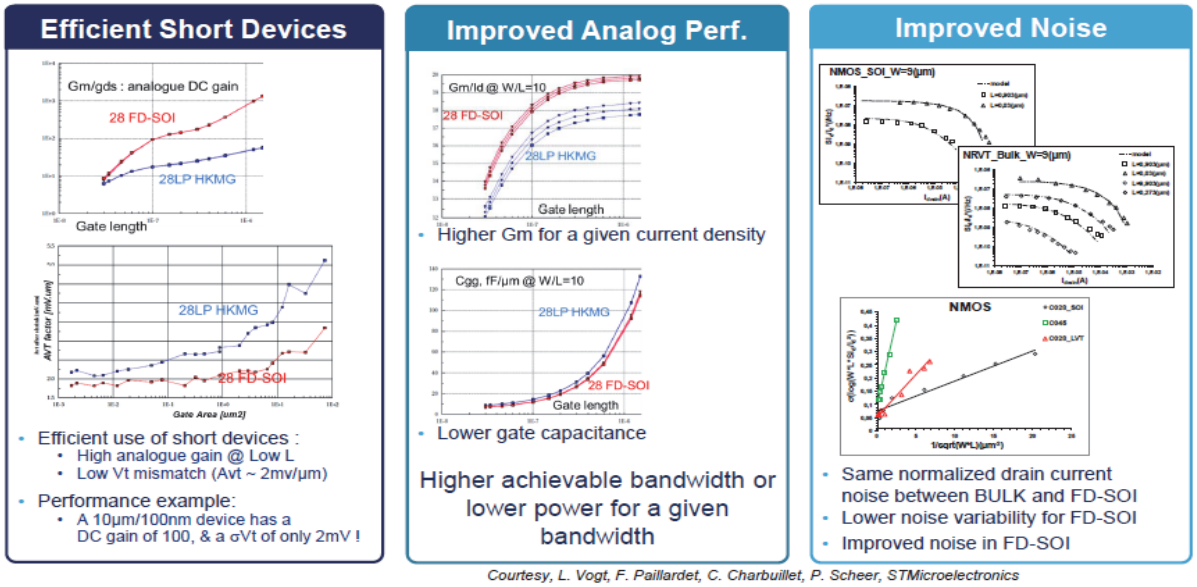


Figure 1.13: UTBB-FDSOI flip-well transistor (Triple well) vs bulk body biasing structure

UTBB-FDSOI technology has proven to be a suitable role in analog and RF design. Figure 1.14 illustrates some advantages of this technology, especially for analog design.



Courtesy, L. Vogt, F. Paillardet, C. Charbuillet, P. Scheer, STMicroelectronics

Figure 1.14: Advantages of FDSOI technology for analog design

While the digital blocks continue to shrink, analog one hardly shrinks at all. For example, ring oscillators (digital oscillators without passive elements) are known to exhibit high phase noise, but this design is attractive as it will address aggressively the size (only inverters) and power consumption reduction.

Indeed, we will use the unique back-gate control structure offered by UTBB-FDSOI transistors to compensate the mismatches between the different inverters of the ring oscillator to decrease jitter and phase noise.

1.3. Applications of FDSOI technology

Because UTBB-FDSOI technology has such excellent performances above, it has a wide range of applications as follows [13]:

1 - Infrastructure Networking: The network infrastructure products benefit from UTBB-FDSOI to adapt performance and power to workload thanks to FBB. FDSOI provides not only more performance at same voltage than bulk, but also much lower performance degradation when lowering the supply voltage. As a result, it will have a good efficiency on multiprocessing applications.

2 - Consumer devices: UTBB-FDSOI technology can help optimized SoC integration in Mixed-signal and RF applications. Circuits in UTBB-FDSOI technology show a wide dynamic voltage and frequency scaling (DVFS), extend performances and reduce the power consumption using back-gate control. For example, a 3GHz dual-core ARM Cortex TM-A9 (A9) manufactured in the 28nm UTBB FD-SOI technology, compared with equivalent 28 nm bulk CMOS chip, shows an improvement of +240% at 0.6V or +540% at 0.61V with 1.3V FBB [14].

3 - Automotive: UTBB-FDSOI features low power consumption, fast speed, low cost, etc. It is suitable for use in automotive cameras, processors and radars. It also manages leakages in high temperature environment and guarantees high reliability thanks to highly-efficient memories.

4 - Internet of things (IoT): The Internet of Things is an environment where each object is provided with unique identifiers and the ability to transfer data over a network without requiring human-to-human or human-to-computer interaction as shown in Figure 1.15. LoT of embedded objects become more and more popular in our daily lives.

Figure 1.15: Internet of things: a world of connection (Source: datafloq.com)

But IoT is not “green”, because every terminal needs energy. The number of connected devices has increased exponentially in recent years as shown in Figure 1.16. With the back-gate control, UTBB-FDSOI technology can offer an ultra-low voltage operation in each device. It can balance power, performance and cost, so FDSOI is a good choice for IoT chips that have special power and cost requirements.

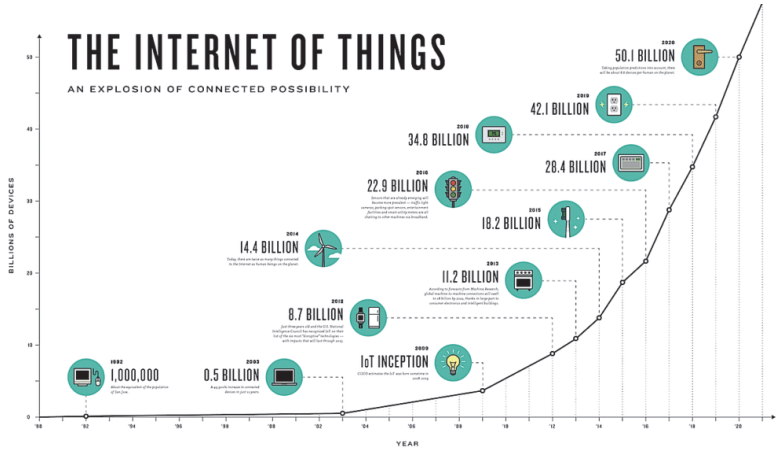


Figure 1.16: IoT terminal development trend (Source: Disruptionhub.com)

1.4. Conclusion

In this section, we first reviewed the development of the integrated circuit industry and the trend of transistor scaling. With the development of Moore's Law, FinFET technology and UTBB-FDSOI technology help Moore's continuation. FinFET is suitable for today’s digital IC applications while UTBB-FDSOI technology, thanks to its specific back-gate structure, provides low-power and more flexible multi-V_{th} design for analog and RF applications. Then we introduced the possible applications for UTBB-FDSOI. What we are very interested in is the application of IoT. We will design novel structure of oscillators and phase-locked loops in UTBB-FDSOI technology for low-power applications. PLL is a very interesting circuit to evaluate this technology for analog, RF and mixed-signal design.

2. Phase-Locked Loop

2.1. Introduction

Clock signals are widely used in a variety of circuits. For digital circuits, whether it is synchronous timing or non-synchronous timing, the correct operation of digital information processing, including calculation, transmission and storage, requires a stable clock. In radio frequency communication, wireless signals are transmitted strictly according to a specific frequency.

Therefore, in RF receiving and transmitting systems, a clock generation circuit called frequency synthesizer is required to generate an accurate clock signal. Also, in wired communication systems, such as in fiber-optic communications, and in communication systems using metal wires as carriers, digital signals are also modulated to a certain frequency. Accurate clock generation and recovery circuits are a very important part of such systems. A Phase-Locked Loop (PLL) is such circuit that satisfied all the above functions.

A phase-locked loop (PLL) is a control system that generates an output signal whose phase is related to the phase of an input signal. More precisely, a PLL is a circuit synchronizing an output signal which is generated by an oscillator with a reference signal in frequency as well as in phase [15]. In the synchronized, often called locked state, the phase error between the output signal and the reference signal is zero, or very small. As a result, a PLL can track the input frequency, or it can generate a frequency that is a multiple (in fact a fractional number) of the input frequency.

The classic PLL topology usually consists in four following blocks:

- Phase Frequency Detector (PFD) or Phase Detector (PD): compares the frequency of the input reference signal (from the frequency stable crystal oscillator) and the feedback signal, and outputs a signal representing the difference between the two signals.
- Loop filter (LF) or low-pass filter (LPF): Filters the high-frequency components of the signal generated from PD, keeping the DC part signal.
- Voltage Controlled Oscillator (VCO): Outputs a periodic signal of the corresponding frequency according to the input voltage.
- Feedback Loop: usually implemented by a divider, reduces the frequency of the VCO to be compared with the reference signal to compare in PD.

Here we take the RF clock generation circuit as an example to describe the basic operating principle of the PLL circuit. First, a high-quality reference clock source is used in the clock generation circuit, usually achieved with a quartz oscillator. The frequency of a quartz oscillator cannot be adjusted outside a very limited range around its fundamental frequency or harmonics and produces usually only a fixed clock frequency. So a PLL is required to generate the various desired frequencies. For example in quad-band GSM RF transmitter, the clock reference source may work at 26 MHz, a PLL is required to generate two distinct signal paths one for low frequency bands (824 to 915MHz) and one for high frequency bands (1710 to 1980MHz) [16].

As shown in Figure 1.17, the PLL is a negative feedback system. In the feedback loop, the output of the VCO is divided by the frequency divider to the low frequency (f_{VCO}/N), and the phase

difference signal is generated comparing with the reference clock in PD. Then the phase difference signal is processed by loop filter in the forward channel generating a voltage signal to control the VCO. As a result, the output clock of the VCO at the back end of the loop is locked at N times the reference clock frequency.

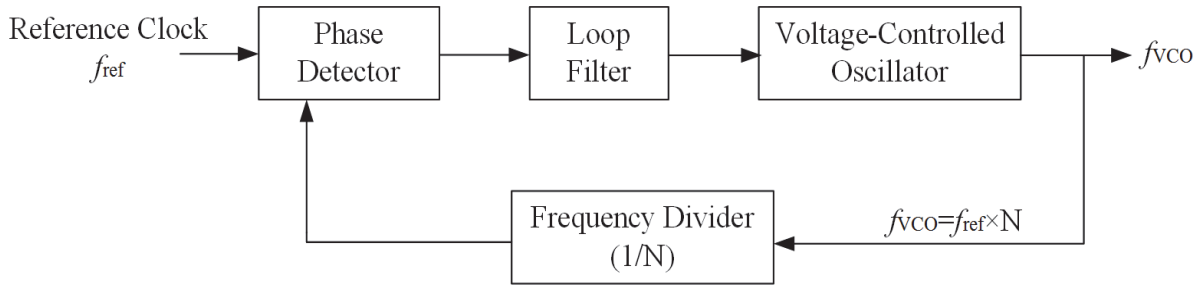


Figure 1.17: PLL block diagram for clock generator application

2.2. PLL characteristics

The PLL has the following basic characteristics during normal operation:

1) Good narrow band characteristics:

   When the PLL is in the locked state, the error voltage output from the PD is a DC voltage that can smoothly pass through the loop filter. If there is an interference component in the input signal at this time, the error voltage formed by the interference signal and the output signal of the VCO in the phase detector PD is suppressed by the loop filter (outside the passband of the LPF). Therefore, the interference component in the output signal of the VCO is greatly reduced. The loop of PLL is equivalent to a high-frequency narrow-band filter to filter out noise. This narrow-band filtering characteristic is difficult to achieve with LC, RC, quartz crystal and other filters.

2) No frequency difference in locked state

   When the PLL is in the locked state, the output signal of the loop is equal to the frequency of the input signal, there is no residual frequency difference, only the remaining phase difference. It achieves better frequency control than the conventional AFC system, and thus has been widely used in automatic frequency control, frequency combining and other applications.

3) Automatic tracking feature

   When the frequency of the input signal changes slightly in a locked loop, the frequency of the VCO changes rapidly, making the output frequency close to the input frequency and eventually equal. Even if the loop does not immediately reach the locked state, it can capture the input signal and finally enter the locked state through its own adjustment.

4) Easy to integrate

The building blocks of PLL should be easy to use in integrated circuits. With the development of integration technology, the entire loop, including some amplifying components, control components, etc., can be integrated on a single chip. The circuit integration can reduce chip's size, save costs, improve reliability and stability, and greatly improve the overall performance.

2.3. PLL applications

Because of its outstanding performances above, PLLs are widely used in signal filtering, modulation and demodulation of analog and digital signals, frequency multiplication or division, mixing, frequency synthesis etc. We will show some examples to explain the classic applications of PLL as follows:

1) Frequency multiplication, division and mixing

In the basic PLL circuit, if we add a frequency divider, a frequency multiplier or a mixer in the feedback loop, the output frequency of the VCO will be locked at the required frequency, thus achieving frequency multiplication, frequency division or frequency mixing functions respectively.

2) Clock generation

Many microelectronic systems, including processors, operate at hundreds of MHz or GHz frequency. Generally, the clocks supplied to these systems are made with PLL, which multiplies a lower frequency reference clock (usually 50 or 100 MHz) up to the operating frequency of these systems [17].

3) Demodulation of Frequency modulation (FM)

If a PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated out. If the VCO used in the PLL is highly linear, it is possible to realize highly linear FM demodulators.

4) Phase-locked receiver

The phase-locked receiver is a narrow-band tracking PLL with a mixer and intermediate frequency (IF) amplifier at the feedback loop as shown in Figure 1.18 [18]. This receiver is suitable for long-distance transmission, such as in space technology applications. When the ground receiving station receives the radio signal from satellites, the signal received is extremely weak because of the long distance, small transmitting power and low gain in

antenna. Moreover, because of the Doppler effect, the frequency of the signal received will deviate from the frequency of the signal transmitted by the satellite, and its value tends to vary over a wide range. For such weak signals whose center frequency varies over a wide range, if a conventional receiver such as a superheterodyne receiver is used, the frequency band of the intermediate frequency (IF) amplifier should have a large bandwidth, so that the output signal-to-noise ratio (SNR) of the receiver will be seriously degraded. It will not be able to effectively detect the signal. If a phase-locked receiver is used, which has the narrow-band tracking characteristic, the output SNR can be effectively improved, and we can obtain a satisfying receiving effect.

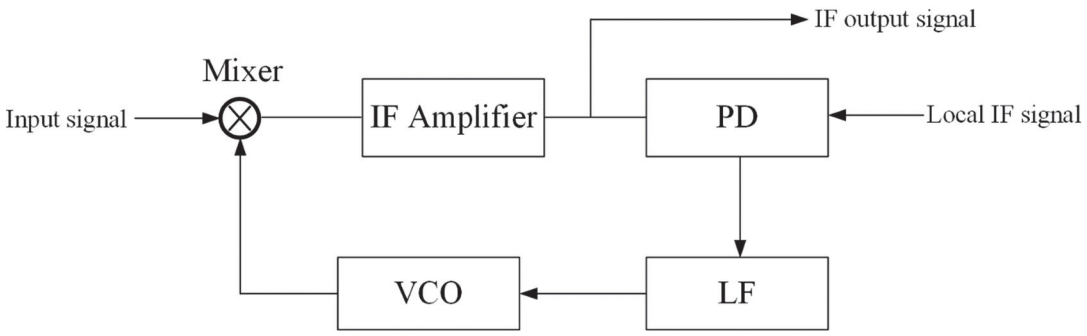


Figure 1.18: Block diagram of PLL receiver

5) Frequency synthesis

RF frequency synthesizer is one of the most important applications for PLLs, which can be found in every communication integrated circuit. As shown in Figure 1.19, the RF receiver & transmitter usually have three main functional subsystems: receiver, transmitter and frequency synthesizer. The function of the frequency synthesizer is to generate the required local oscillation signal for the mixer to receive and transmit at the required frequency. As the PLL can convert the stable and accurate reference frequencies which are provided by crystal oscillators to the specified frequency, it is the ideal module for frequency synthesizers to generate local oscillation signals. The precision of the frequency synthesizer determines the stability and the accuracy of the whole system. As signals are transmitted in specific frequencies in modern communication systems, frequency synthesizers are indispensable components in such systems (cf. Figure 1.19).

Moreover, PLL circuits are also widely used but not limited in clock and data recovery (CDR) [19] [20], jitter and noise reduction, and FSK Frequency-Hopped Communications [21].

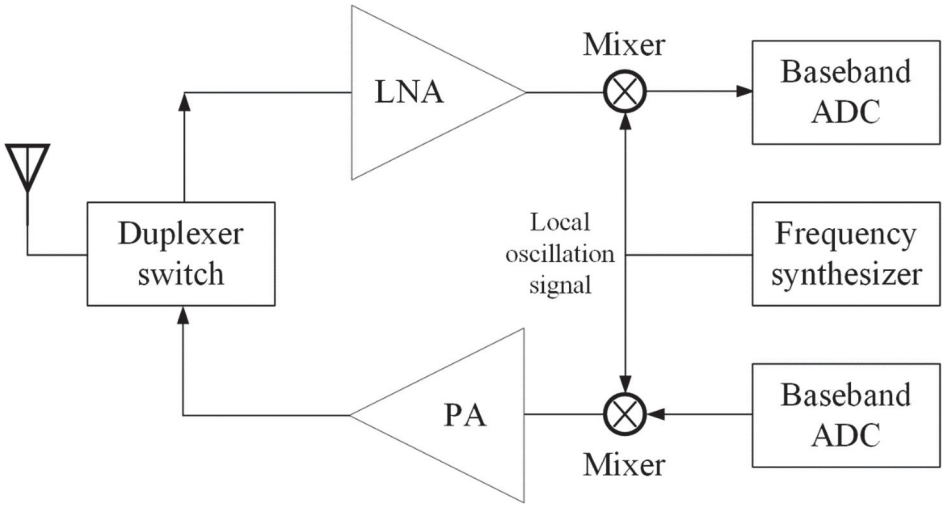


Figure 1.19: Block diagram of RF transceiver

2.4. PLL classifications

According to the degree of digitization of the building blocks of the PLL, there are 3 types of PLL possible on the hardware level: Linear PLL, digital PLL and all-digital PLL.

Figure 1.20 illustrates the block diagram of a linear PLL (LPLL) which is also the structure of the early PLLs. In LPLLs, the four-quadrant analog multiplier is used as a PD. The loop filter is built from a passive or active analog RC filter and the well-known VCO is used to generate the output signals of the LPLL. In most cases the input signal is a sine wave with angular frequency, and the output signal is a symmetrical square wave with angular frequency [15]. In a word, all building blocks in LPLL are based on analog devices and only process analog signals: frequency, phase, or analog voltage etc.

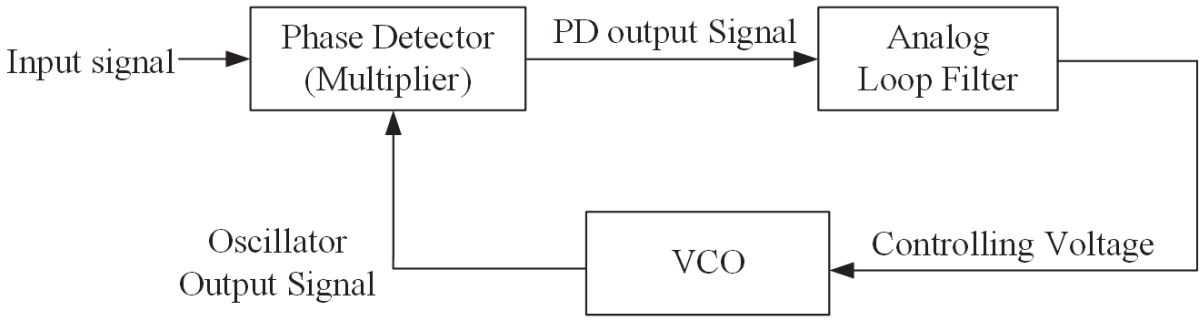


Figure 1.20: Block diagram of the Linear PLL (LPLL)

The PLL gradually evolved into digital territory. If a digital PD (EXOR gate, J-K flip-flop or phase frequency detector) is used and all other blocks remain the same (analog filter and VCO), this system is called the digital PLL (DPLL) as shown in Figure 1.21. In many DPLL applications such as frequency synthesizer, a divide by N counter is added in the feedback loop as the frequency divider, so the VCO generates a high frequency which is N times the frequency of reference signal.

The DPLLs are used for digital signal processing, but the DPLL performs similarly to the LPLL. The error signal from PD is a binary signal which carries analog information (duty cycle) that modulates the after blocks. The noise of DPLL is better than LPLL because the phase detector is only sensitive to rising edge or falling edge of the compared signals (reference and feedback).

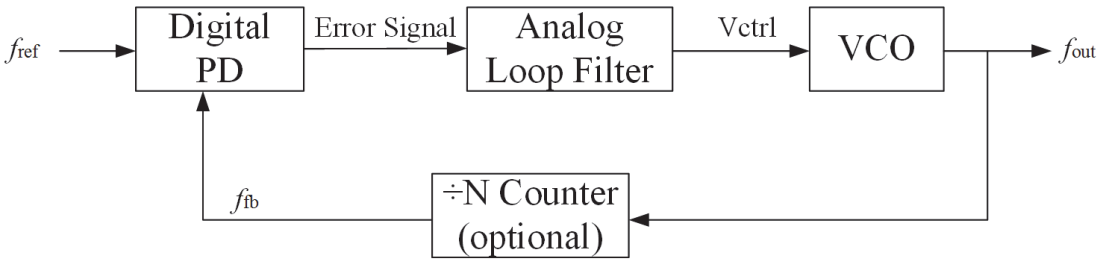


Figure 1.21: Block diagram of the Digital PLL (DPLL)

If the PLL is completely implemented only by digital blocks, without any passive components or linear components, it is called an all-digital PLL (ADPLL). The block diagram of ADPLL is shown in Figure 1.22. From the figure we can see that the analog loop filter is replaced by a much smaller digital loop filter which allows more flexibility than an analog filter, such as a polyphase or adaptive filter [22]. The VCO is renamed by DCO (Digitally Controlled Oscillator) controlled by digital clock. The signals processed by ADPLL are all digital (binary) and may be a single digital signal or a combination of parallel digital signals.

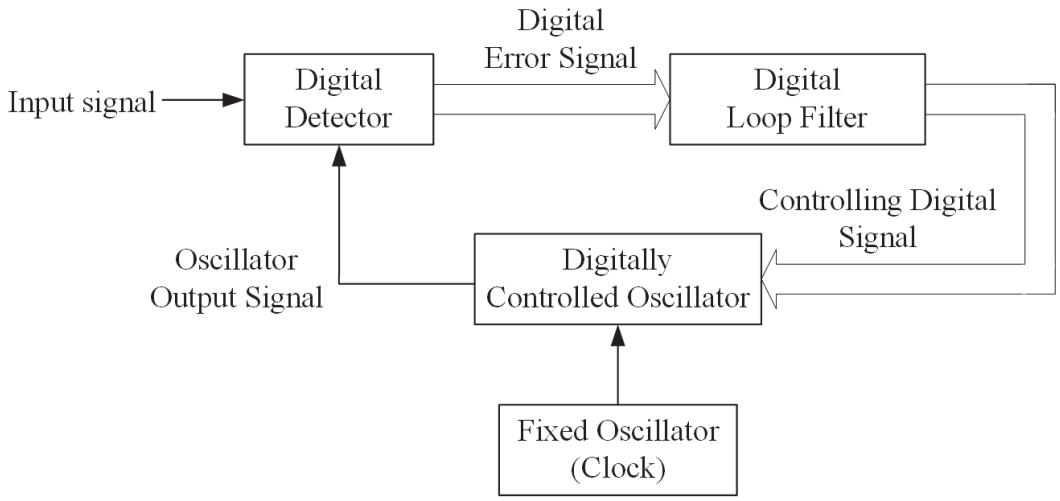


Figure 1.22: Block diagram of the All-Digital PLL (ADPLL)

Compared to traditional LPLLs and DPLLs, ADPLLs have the advantage of no off-chip components. ADPLLs are insensitive to technology but at the cost of performance [23]. Moreover, the loop bandwidth and center frequency are programmable and the ADPLL systems do not require A/D (Analog to Digital or D/A: Digital to Analog) conversion when used in digital systems.

Those are three classic PLL structures based on the hardware level. In fact, with the development of today's PLL technology, PLLs can also be implemented in the software domain. The function of this type of PLL is executed by software and runs on the DSP which is called software PLL (SPLL) [24]. Compared with hardware based PLL, the SPLL is free from complicated hardware circuit design, simple and convenient to modify parameters, has good scalability and anti-interference ability, and can achieve good speed and good precision at the cost of a higher power consumption. The performance of the SPLL is based on a high-performance microprocessor or DSP, but in area limited integrated circuits, traditional LPLL and DPLL are still indispensable.

In the actual PLL applications, we should make a careful trade-off according to performances, price, area, power consumption … to choose appropriate type of PLLs.

2.5. Conclusion

In this section, we studied the basic components and working principle of the PLL circuits. The working characteristics and application of PLL circuits are given. According to the degree of digitization of the building blocks, we also introduced the different type of PLLs. Our target is to build a very low power PLL using a novel structure for VCO, and then all the building blocks of DPLL in UTBB-FDSOI technology.

3. Jitter and phase noise

3.1. Introduction

In today's high-speed communication systems especially in PLL circuits for critical timing applications in systems, it is important to accurately characterize and quantify their noise to determine system performance and reliability [25]. Jitter and phase noise are the major concerns. The former is the performance measurement of noise in the time domain, while the latter is the performance measurement of noise in the frequency domain.

3.2. Timing jitter definition

In application using clock recovery and clock generators, the clock jitter is a very important feature [26]. General speaking, time jitter means the uncertainty of the clock cycle. In another word, jitter is the deviation from true periodicity of a presumably periodic signal as shown in Figure 1.23.

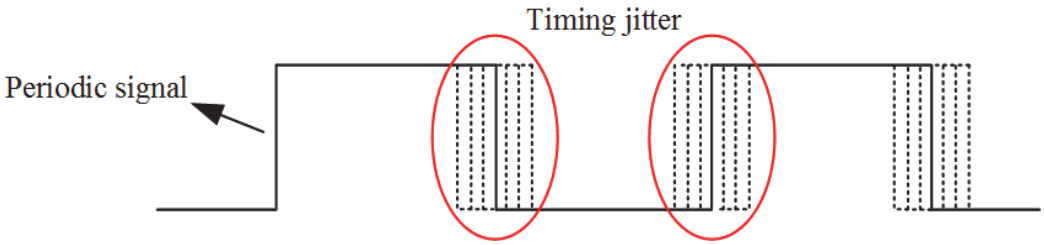


Figure 1.23: Definition of timing jitter

For clock jitter, there are three commonly used metrics:

Absolute jitter or edge-to-edge jitter is a concept of uncertainty that measures the point in time. Absolute jitter represents the time interval error between the real clock edge position measured and the ideal position referenced by an ideal clock. The uncertainty of the time point caused by absolute jitter will affect many sampling circuits. For example, in the clock data recovery circuit (CDR), it is necessary to use the clock edge to sample the center of the data and the edge of the data change. The absolute jitter of the sampling clock has a direct impact on the jitter tolerance of the CDR [27].

Period jitter or cycle jitter is a concept of uncertainty that measures time period and is defined as the periodic deviation between the actual clock period and the ideal or average clock period. Period jitter is important in synchronous circuit which benefits from minimizing period jitter, so that the shortest clock period approaches the average clock period.

Cycle-to-cycle jitter or adjacent period jitter is defined as the period difference of any two adjacent clock periods which is important for some types of clock generation circuit. In order to reduce electromagnetic interference (EMI), many clocks have the spread spectrum function to send the signal energy to a certain frequency band. For example, the spread spectrum modulated by periodic sawtooth, its noise jitter characteristics can be measured by cycle-to-cycle jitter [28].

The amount of jitter can be approximated as a random process, so many statistics can be used. For example, expectations, variance, standard deviation, root-mean-square error (RMS), peak-to-peak value etc. Here we are interested in jitter histogram and eye diagram to present the amount of timing jitter.

The jitter histogram is a histogram obtained by counting the jitter frequencies of different amplitude ranges, and the jitter distribution trend can be visually observed, or obtain a probability density function (PDF) by mathematical approximation to describe the distribution of jitter histogram. Figure 1.24 shows a period jitter histogram example of a 3.3V SiT8102 oscillator running at 125MHz [29]. Then compute the RMS and the peak-to-peak values from the 10 000 samples.

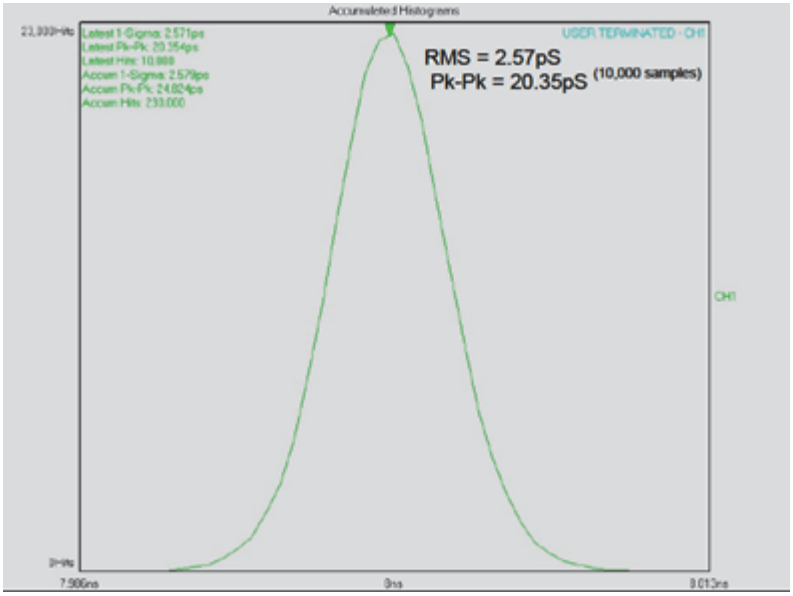


Figure 1.24: Histogram of 10 000 period jitter measurements [29]

Another popular way to observe period jitter is the eye diagram. An eye diagram is a waveform signal is divided into fixed time period, which are superimposed on each other. The result is a plot that has many overlapping lines enclosing an empty space known as the eye. An eye diagram provides many parameters for jitter analysis, such as rise and fall time, eye height and weight etc. as shown in Figure 1.25. The quality of the receiver circuit is characterized by the dimension of the eye. We can observe the jitter state qualitatively through the eye diagram. A better eye-opening state shows a small additive jitter in the signal and a less probability of bit-error-rate (BER) for digital blocks. For the correct functioning of a system, eye should not be closed (width and/or height too small).

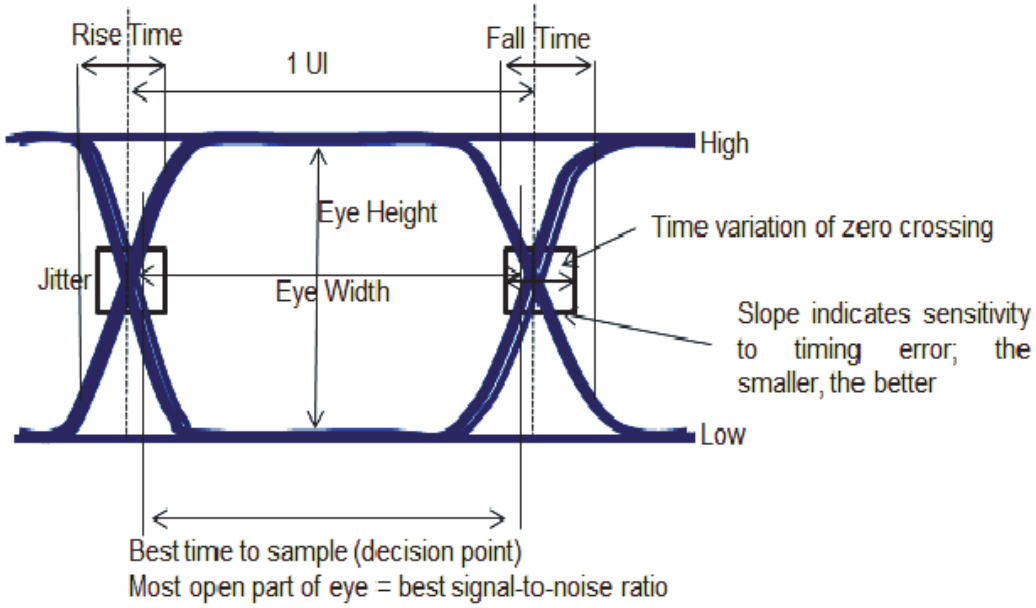


Figure 1.25: Eye diagram analysis [30]

3.3. Phase noise definition

While in frequency domain, the phase noise is usually used to represent the random fluctuations in the phase of a waveform. For an ideal oscillator, the signal spectrum shows an impulse shape. However, in actual case, the spectrum will expand around the carrier frequency, as shown in Figure 1.26.

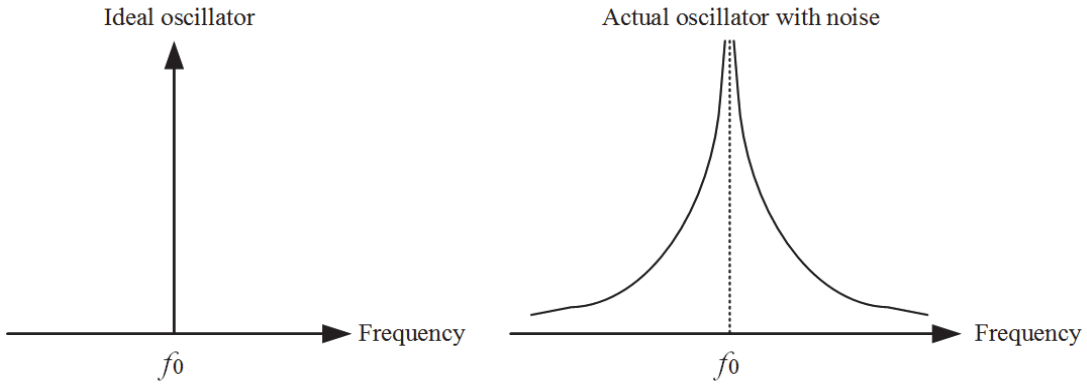


Figure 1.26: Oscillator phase noise

In definition, phase noise (PN) is the one-sided of the phase spectrum $S_\Phi(f)$

$$L(f) = \frac{1}{2}S_\Phi(f) \tag{1.5}$$

The phase noise at f_m is calculated as the ratio of single-sideband (SSB) modulation power to the total carrier power in the 1Hz bandwidth, where f_m is the frequency offset Δf from carrier frequency f_0.

$$L(f_m) = \frac{P_{SSB}}{P_S} = \frac{SSB\ spectral\ density(1\ Hz)}{Total\ carrier\ power} \tag{1.6}$$

Phase noise is usually expressed as a logarithm, the unit is dBc/Hz.

$$PN = 10\log(\frac{L(f_m)}{1Hz}) \tag{1.7}$$

The calculation method can also be seen intuitively in Figure 1.27.

The phase noise closed to the carrier is called “close-in” phase noise, which limits the frequency resolution mainly caused by $\frac{1}{f^3}$ noise, $\frac{1}{f^2}$ noise and flicker noise. The phase noise far away from carrier frequency is called broadband phase noise, which effects SNR (Signal to Noise Ratio) and mainly caused by white noise [31]. On the phase noise curve, it is sometimes observed that there are relatively large spurious components at several frequency points. In fact, we need to analyze the causes of the occurrence of frequency points that contribute to the noise due to the spur, so as to optimize the design and improve the performance.

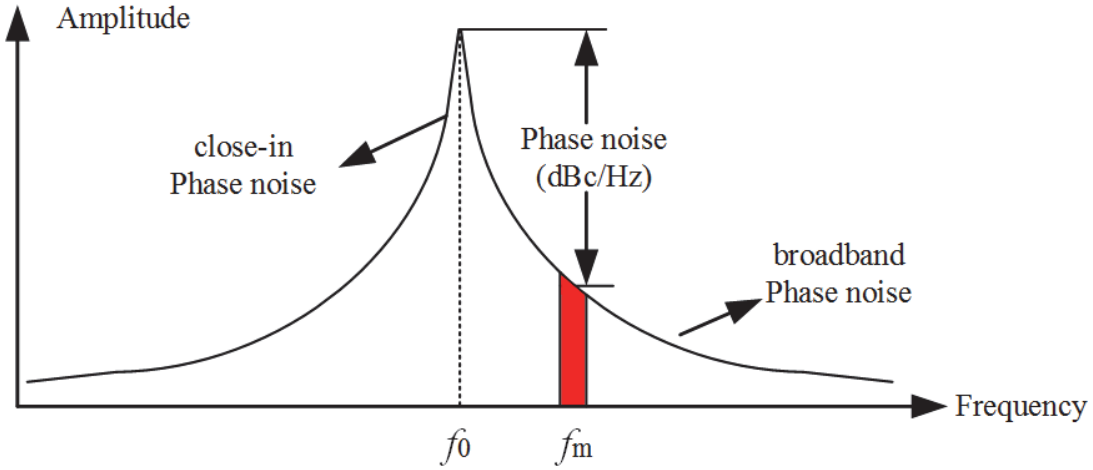


Figure 1.27: Definition of phase noise

Since any device can contribute noise, the theoretical study of phase noise is very complicated. There are three models to help study phase noise.

The very first one was an empirical noise model proposed by D.B. Leeson in 1966 [32]. This model is suitable for an oscillating circuit composed of RLC resonators because this model matches the quality factor definition of the RLC network. The phase noise can be calculated by equation 1.8.

$$L(\Delta f) = 10\log\left(\frac{2kTF}{P_s}\left(1+\left(\frac{f_0}{2Q_L\Delta f}\right)^2\right)\left(1+\frac{\Delta f_{\frac{1}{f^3}}}{\Delta f}\right)\right) \quad (1.8)$$

Where F is the additional noise figure, empirical parameter, P_s is the average power loss, Q_L is loaded quality factor, Δf is the frequency offset and $\Delta f_{\frac{1}{f^3}}$ is the corner frequency between $\frac{1}{f^3}$ and $\frac{1}{f^2}$ areas. Lesson's model considers both flicker noise and white noise as presented in Figure 1.28.

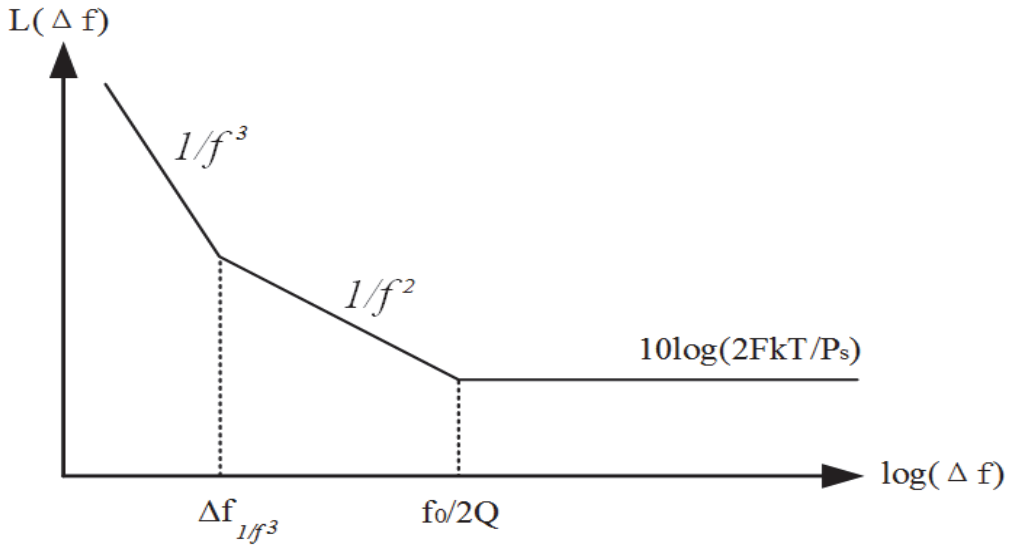


Figure 1.28: Definition of phase noise

The phase noise model by Lesson shows that increasing the resonant value Q and increasing the amplitude can reduce phase noise. However, the empirical parameters F is difficult to evaluate, so as $\Delta f \frac{1}{f^3}$. But this model is still a successful attempt.

In 1996, Razavi proposed an analysis method for the phase noise of a ring oscillator. The basic method is to apply the analysis method similar to the Lesson model to the analysis of the ring oscillator premised on linear time invariant (LTI) assumptions. The main difference is its definition of the open-loop Q which is described in reference [33] and the final formula of the sum of noise contribution from all devices is:

$$\frac{\overline{V_n^2}}{\Delta f} = kTR_{eff}(1+A)\frac{f_0}{\Delta f}^2 \tag{1.9}$$

Where R_{eff} is the equivalent series resistance and A is the multiple of additional noise figure. So, the single sideband noise spectral density to the carrier power ratio at frequency offset is:

$$L(f_m) = 10\log\left(\frac{\overline{V_n^2/\Delta f}}{P_S}\right) = 10\log(\frac{kT}{V_{swing}^2/2}R_{eff}(1+A)\frac{f_0}{\Delta f}^2) \tag{1.10}$$

Where V_{swing} is the resonance amplitude. From this formula (Equation 1.10), we can see that increasing the resonance amplitude V_{swing} and reducing the equivalent series resistance R_{eff} can help reduce phase noise.

This model proposed by Razavi assumes a linear time-invariant negative feedback network explains the effect of additive noise (flicker noise and white noise) on phase noise However, it cannot explain the phenomenon that single-frequency noise will generate noise on both sides of the carrier and there are still empirical fitting parameters.

In 1999, Hajimiri introduced a novel method for analyzing phase noise by introducing an impulse sensitivity function (ISF) [34]. The basic idea is to solve the system's impulse response (with the disturbance of the noise current as input) and attribute the time-varying characteristics of the system to the ISF function based on linear phase time (LPT) assumptions.

The ISF function characterizes the sensitivity of each point on the waveform to interference and is mainly obtained by simulation methods, and can also be approximated by the slope of the oscillating waveform [35] :

$$\mathrm{T}_i(x) = \frac{f_i'(x)}{f_{max}'^2} \tag{1.11}$$

There is an example of the oscillation waveforms and its corresponding ISF functions for a typical LC oscillator and a typical ring oscillator in Figure 1.29.

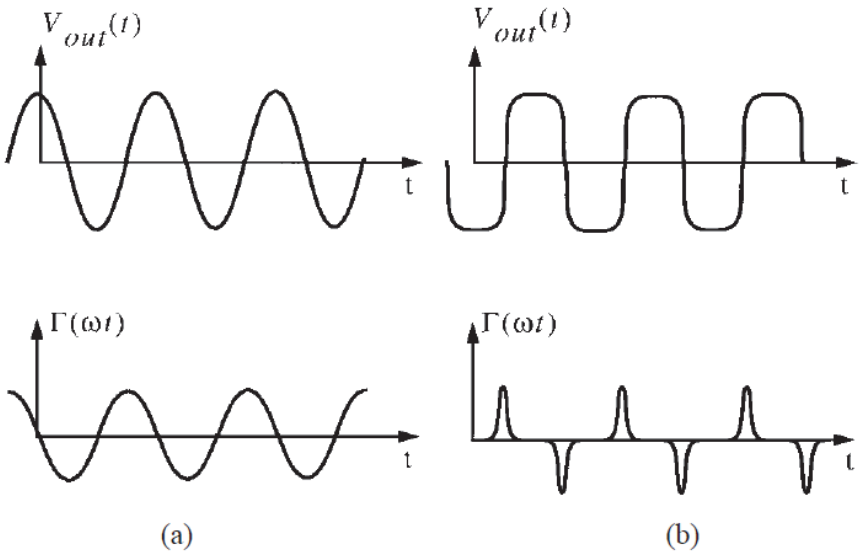


Figure 1.29: Waveforms and ISF's for (a) LC oscillator and (b) ring oscillator [34]

Once the ISF is obtained, superposition integral can be used to calculate the extra phase θ(x), and then the total spectrum of the output oscillation signal is obtained.

The analysis results in reference [36] shows that $\frac{1}{f^3}$ area noise mainly comes from the low frequency 1/f noise of the device, $\frac{1}{f^2}$ area noise is device's white noise on the harmonic and the white noise region is the white noise of the oscillator itself. Moreover, it also noted that in order to reduce the contribution of 1/f noise, the oscillating waveform should be designed to be as symmetrical as possible.

This model proposed by Hajimiri can analyze the case that device 1/f noise is converted into phase noise an analyze stationary noise, even periodic stationary noise. It is a general, accurate, quantitative analysis method for phase noise analysis.

3.4. Conversion between timing jitter and phase noise

As presented before, jitter and phase noise are two forms of noise in the time and frequency domains which can be converted to each other by theoretical calculation.

From reference [37] and [38], we can see that the period jitter is the standard deviation of the variation in one period and it can be expressed by:

$$J = \sqrt{cT} \tag{1.12}$$

Together with the following formula (cf. Equation 1.13), also expressed in [37]and [38]:

$$c = L(\Delta f)\frac{\Delta f^2}{{f_0}^2} \tag{1.13}$$

We can then deduce the phase noise at a certain offset, described by equations (1.14) and (1.15).

$$L(\Delta f) = J^2\frac{{f_0}^3}{\Delta f^2} \tag{1.14}$$

$$PN = 10\log(L(\Delta f)) = 10\log(J^2\frac{{f_0}^3}{\Delta f^2}) \tag{1.15}$$

Where J the period jitter, Δf is the frequency offset and f_0 is the carrier frequency. Attention that Δf should be well above the corner frequency (f_c) to avoid ambiguity and well below f_0 to avoid the noise from other sources that occur at these frequencies. In another word, this equation can be used in the case where the flicker noise is negligible.

Similarly, based on the obtained phase noise, the jitter value in the time domain can be obtained by the integrated power in the frequency range of interest.

First, with the help of Wiener–Khinchin theorem, the variance of the spectrum ${\varphi_{e\_rms}}^2$ at the corresponding frequency interval can be obtained which is also called phase jitter.

$${\varphi_{e\_rms}}^2 = 2\int_{f_1}^{f_2} L(f)df \tag{1.16}$$

It should be noted that if the phase noise $L(f)$ is a logarithmic representation of dBc/Hz, it needs to be converted into linear coordinate form first.

$${\varphi_{e\_rms}}^2 = 2\int_{f_1}^{f_2} 10^{\frac{L(f)}{10}}df \tag{1.17}$$

Then, timing jitter can be deduced from the phase jitter divided by angular frequency:

$$J_{rms} = \frac{\varphi_{e\_rms}}{2\pi f_0} \tag{1.18}$$

To easily estimate jitter, a line graph can be used to roughly approximate the phase noise curve. That is, using segmentation statistical accumulation calculation with a finite number of frequency points. The interval between the two frequency points is then actually a trapezoidal area. The integral value of the region can be obtained by using the trapezoidal area calculation formula, and then calculated separately and then added to obtain the total integrated power.

Here is an example where the phase noise of the ADF4360-1 2.25GHz PLL is shown in Figure 1.30 and the line-segment approximation and jitter calculations shown in Figure 1.31 [31].

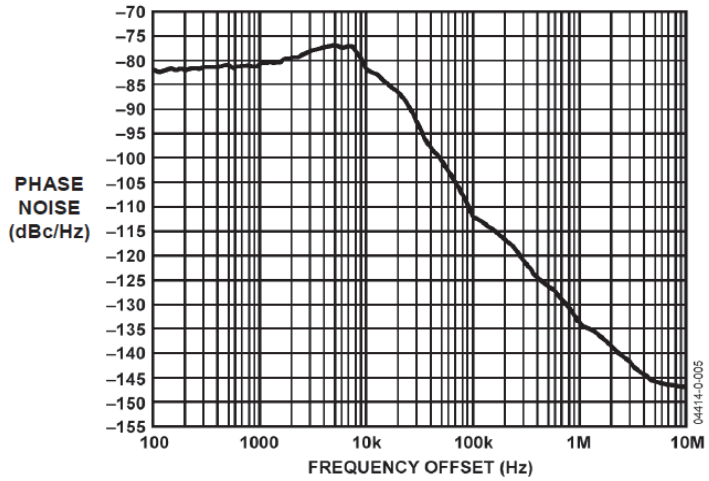


Figure 1.30: Phase Noise for a 2.25GHz PLL with loop filter bandwidth=10kHz [31]

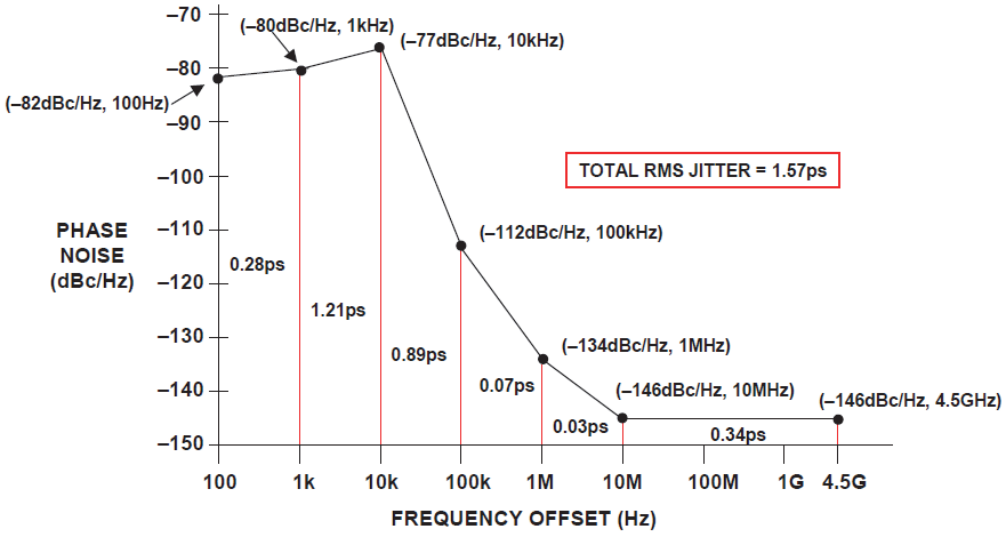


Figure 1.31: Line segment approximation method showing RMS jitter [31]

The relationship between the jitter of each integration interval and the total jitter is root-sum-squares (RSS), so we can calculate the total RMS jitter as follows (cf. Equation 1.19).

$$\sqrt{0.28^2 + 1.21^2 + 0.89^2 + 0.07^2 + 0.03^2 + 0.34^2} \approx 1.57ps \tag{1.19}$$

So, we have derived this PLL shows a RMS jitter of 1.57ps with the help of its phase noise spectrum.

3.5. Conclusion

In this section, we introduced an important indicator to measure the noise of the PLLs: jitter in time domain and phase noise in frequency domain. We have shown their definitions and measurement methods, as well as introduced the conversion method between time jitter and phase noise.

In our actual work, there are non-convergence problems in DC and AC simulations due to the incompatibility between PDK and Cadence version, we cannot directly measure phase noise. So, we can judge the anti-noise ability of the circuit through the period jitter and we can also estimate the approximate phase noise by measuring the period jitter in the conversion method above.

4. State of the art for VCO

In the above sections, we introduced the structure of the PLL and the important parameter of phase noise. The VCO is the most important building block of the PLL, determining the characteristics of the whole system. Our work begins with a VCRO, so we have studied the previous VCOs with different types and different technologies as shown in Table 1.1.

The main characteristics on which we based our study for VCO are topology, oscillating center frequency, tuning range, power consumption, phase noise and Figure of Merit (FOM) which is a quantity used to characterize the performance of oscillators with different operation frequency.

The Figure of Merit is given by the following equation [39]:

$$FOM = -L(f_m) + 20log\frac{f_0}{f_m} - 10log\left(\frac{P_{DC}}{1mW}\right) \quad (1.20)$$

where f_m is the frequency offset, f_0 the central frequency, $L(f_m)$ is the phase noise and P_{DC} is the power consumption.

Table 1.1: Comparison of different types of VCO

Publications	[40]	[41]	[42]	[42]	[43]
Topologies	LC	LC	RTW VCO	LC QVCO	VCRO
Technology	CMOS 0.35um	CMOS 0.18um	CMOS 130nm	CMOS 130nm	FDSOI 28nm
Frequency	9.8GHz	10GHz	11.5GHz	13GHz	2.45GHz
Tuning range	245MHz	2.5GHz	1.2GHz	900MHz	1.GHz
Consumption	12mW	15mW	30mW	8mW	788uW
PN	115dBc/Hz@1MHz	115dBc/Hz@1MHz	105dBc/Hz@1MHz	100dBc/Hz@1MHz	105dBc/Hz@2MHz
FOM	184	183	171	173	167

From the table, we can see that the work by Alexandre Fonseca realized in FDSOI technology, which has a significant advantage in low power consumption.

5. Conclusion

In this chapter, we first reviewed the development of the integrated circuit industry and the trend of transistor scaling and studied the characteristics of FinFET and UTBB-FDSOI technology. After understanding the characteristics of UTBB-FDSOI transistor and the working principle of the PLL circuits, we make it clear that our target is to build a novel structure for VCO, then all the building blocks for DPLL in UTBB-FDSOI technology. Then, we introduced the definitions and measurement method for jitter and phase noise, as well as the conversion method between them. Finally, we briefly introduced some completed work for VCOs with different types and different technologies.

We will begin our design from a simple inverter to all the building blocks for PLL step by step starting from the next chapter.

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Chapter II – Complementary Inverter and Complementary logic

1. Why to introduce complementary logic?

1.1. Introduction

When two or more input signals of a logic gate are changed, the moments when their states change are in sequence. These variables are generated through different paths, which are called competition. The consequence of this competition will likely lead to race hazards and glitches [1].

Traditional logic in Karnaugh map design [2] suffers of glitches due to the inverters that introduce unwanted delays in the process of the digital signals as illustrated in Figure 2.1.

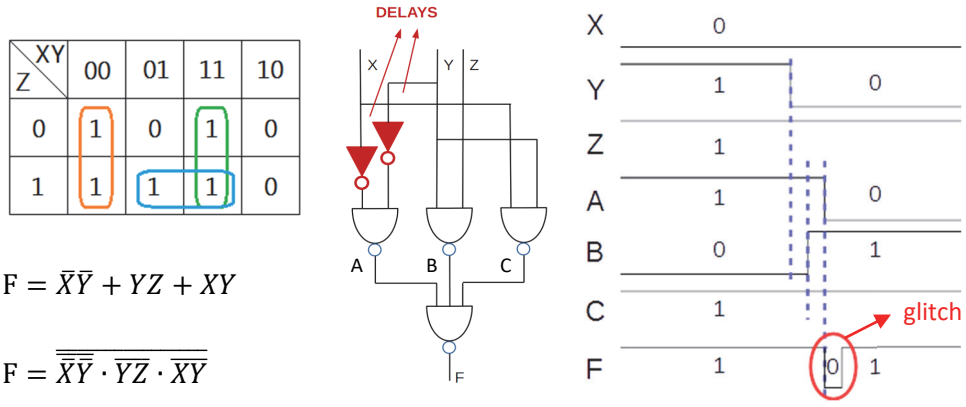

Figure 2.1: Karnaugh map design example in 'traditional' logic and its glitch problems

The combinatorial logic circuit's risk of glitches occurs only when the signal state changes. This risk is temporary and it doesn't deviate from the normal value. However, in high-speed circuits, glitches are very sensitive to signal changes, where precise signal transitions are required. What's more, in the state machine and asynchronous circuit, the risk is essential, which can cause the output value of the circuit to deviate from the normal value or oscillate forever.

Glitch is a thorny problem in digital circuit design. Its appearance will affect the stability and reliability of the circuit work even lead to malfunction and logic disorder of the entire digital system.

There are several existing methods to eliminate glitches problems such as adding extra flip-flop, using synchronous clock circuit or gray code counter etc., but those methods have certain

drawbacks and limitations. Complementary logic design is a good solution to free digital circuits from mismatches to build glitchless quality signals which is applicable under any circumstances.

Complementary logic circuit provides both inverted and non-inverted outputs. It allows to build more efficient gates where glitches are removed. For example, a two-input gate that provides both the AND and the NAND functions in a single circuit. Such gates exist and are referred to as complementary output gates [3].

The ideal complementary output gates provide both inverted and non-inverted output signals, in such a way that neither one is delayed related to the other. However, there is no solution to build a simple gate producing the signal and its inverse at the same instant. The delay necessary to invert the signal cannot be compensated in a safe way. Playing with sizing may reduce the glitches and improve the timing but cannot provide a reliable solution in any way as shown in Figure 2.2. So, these gates are not suitable in precise and high-frequency digital circuit.

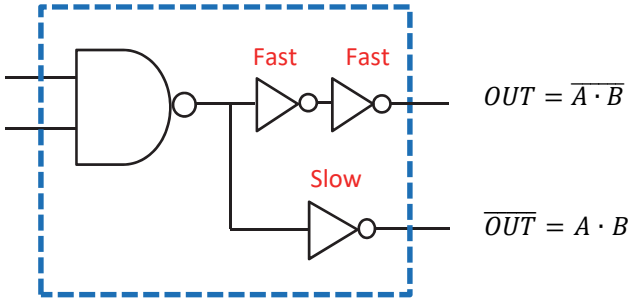

Figure 2.2: Example of a gate with two complementary outputs

Therefore, we need to find another architecture without these extra delays. To remove these inverters introduced in series in the process of the digital signals, we will use a parallel structure with a positive and a negative logic plane. A positive logic plane uses positive logic that we usually perceive as 0 is false, 1 is true and negative logic plane is on the contrary.

Taking the same example in Figure 2.1, the way is first set up a positive plane and then its opposite negative plane as shown in Figure 2.3. It should be notice that the negative plane of NAND is NOR referring to De Morgan's laws ($\overline{A + B} = \bar{A} \cdot \bar{B}$). We can see that to build the signal A, we need to introduce two inverters to invert the signal X and Y, also to build the signal $\bar{A}$. Two inverters are also needed to invert the signal $\bar{X}$ and $\bar{Y}$. But if we combine the positive plane with the negative plane together, this pair of positive and negative inputs can be obtained directly, so we do not need to add additional inverters to get its opposite signals.

Combining both planes together, the Figure 2.4 represents the complementary solutions where complementary signals are represented by a couple of a signal and its inverse. These are no

extra delay introduced which could produce unwanted glitches because all the signal changes are at the same time, no inverter needed.

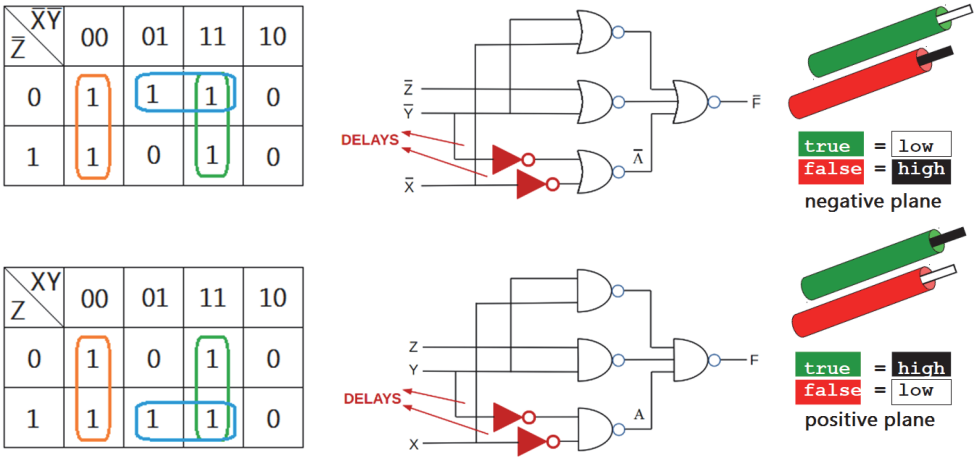

Figure 2.3: K-map design in positive and corresponding negative plane

So, what we found is such gate where signals and their complement are built at the same instant. There are several solutions to realize these structures, like the differential logic or the complementary logic.

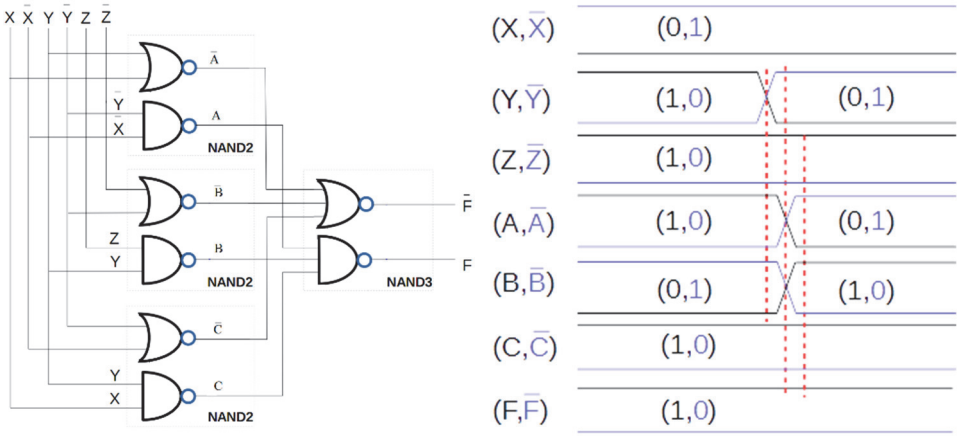

Figure 2.4: Complementary logic example and its glitchless symmetrical outputs

1.2. Differential logic

In differential logic, the differential signal is a pair of symmetrical signals both in input and output. Introduced by IBM in the fifties [4], the emitter-coupled logic (ECL) shown in Figure 2.5 represents a popular solution to build differential logic [5]. Overdriven BJT (Bipolar Junction Transistor) differential amplifiers are used in ECL structure with single-ended inputs and restricted emitter currents, which helps to avoid the saturated operating region and its slow turn-off behavior. The constant differential amplifier current can minimize the time delays and glitches caused by

power-line inductance and capacitance. Moreover, complementary output can reduce the propagation time of the entire circuit by reducing the number of inverters.

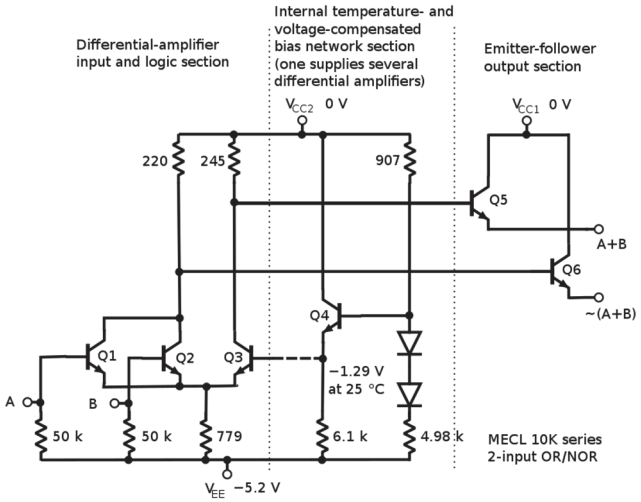

Figure 2.5: ECL basic gate circuit diagram

ECL's (and its similar architectures) major disadvantage is that each gate continues to have current pass through, which means it requires more power consumption than other logic structures, especially when quiescent. Moreover, it suffers from nonstandard logic levels.

There are other solutions like the structures presented in Figure 2.6 and 2.7. Differential cascode voltage switch logic (DCVSL) (cf. Figure 2.6) refers to a CMOS-type logic which requires mainly N-channel MOSFET transistors to implement the logic using true and complementary input signals, and needs two P-channel transistors at the top to pull one of the outputs high [6].

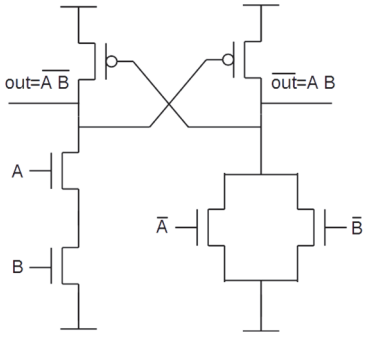

Figure 2.6: Basic differential cascode voltage switch logic (DCVSL) NAND-NOR gate

Performances of the circuit of DCVSL are limited by the set time of PMOS latch, a better performance clocked DCVSL circuit is illustrated in Figure 2.7. The outputs out and $\overline{out}$ are precharged low when the clock phase clk is low and data are propagated in a domino mode when clk goes high. During switching either c1 or c2 is pulled down and either device P1 or P2 is shut off, so

that no direct current flows after switching, but a clock signal should be introduced in each gate which is quite complex.

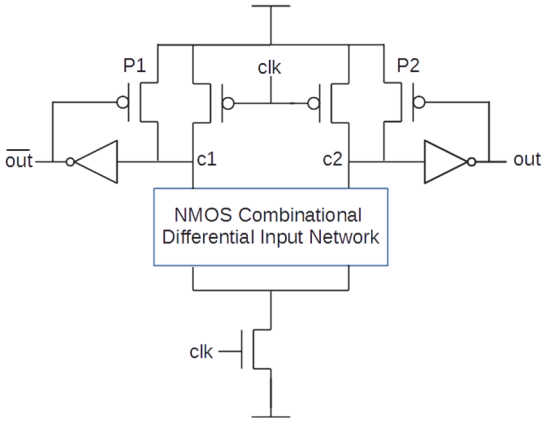

Figure 2.7: Clock DCVSL gate

There are several disadvantages in these proposed differential logic circuits. Some solutions do not provide CMOS logic level, others cause extra power consumption when the output signals are latched or use a clock.

1.3. Complementary logic

With symmetrical inputs in theory, complementary logic has symmetrical outputs which provide plain CMOS compatible level and minimize power consumption. A complementary NAND is shown in Figure 2.8 which is composed by a NAND gate and a NOR gate, and the NAND and NOR gates have inversed inputs.

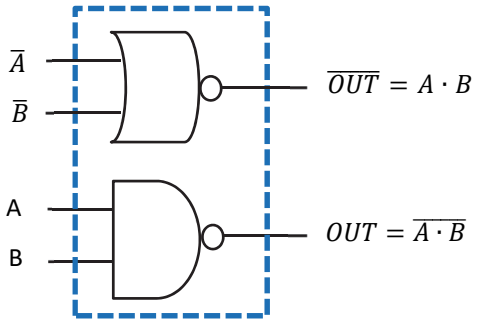

Figure 2.8: Complementary NAND without interaction between positive and negative plane

In fact, complementary logic is a generalized differential logic because their inputs can have any signal values, if symmetrical signals are used in the positive and negative logic plane, we can call it also differential logic.

In a structure like Figure 2.8, signals in positive and negative logic plane are built in totally separated ways. It works well in normal conditions, but optimization is a process that can always be

considered. There is no warranty that inputs are symmetrical, and outputs are not forced to be symmetrical, so the gates like that don't spontaneously symmetrize output signals. If there are unexpected delays between the symmetrical input signals, mismatches of delays between positive and negative plane are accumulated without the possibility to resynchronize them, something that differential logic was doing. It is possible to design circuits where inputs are built to be symmetrical; outputs are therefore symmetrical but can suffer of small asymmetries (cf. Figure 2.9).

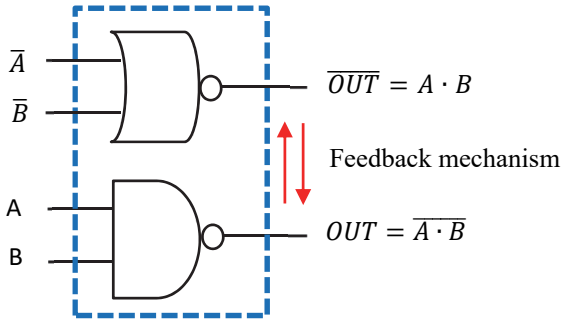

Figure 2.9: Complementary NAND with symmetrization feedback

We need to find a simple solution to provide a symmetrization feedback between positive and negative planes as shown in Figure 2.9. Being in symmetrical structure and considering the power consumption, the symmetrization doesn't need to be very strong. So, the differential structure with a latch at the outputs is not a good choice.

Another solution is to use feedback V_{Th} control of MOS transistors to symmetrize the structure. Compared to classical bulk transistors, UTBB-FDSOI transistors are more effective for back-gate control as shown in Figure 2.10 [7] and are compatible with CMOS structures. What's more, it also gives a good solution in terms of layout design. So, the UTBB-FDSOI technology gives us an opportunity to design circuits which will have a better performance.

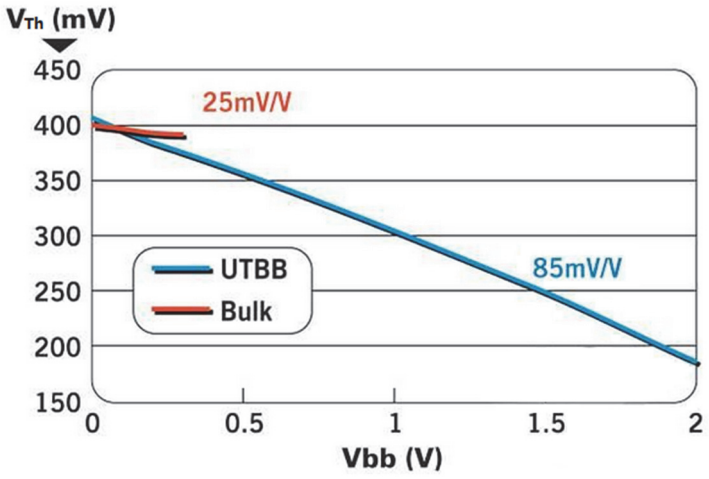

Figure 2.10: V_{Th} variation versus back-gate biasing between bulk and UTBB-FDSOI transistors

2. Complementary inverter in UTBB-FDSOI

2.1. Topology of complementary inverter

Figure 2.11 presents four available implementations of “classical” inverters in UTBB-FDSOI technology to explain the behaviors and performances of our proposed complementary inverter [8]. We can notice that configuration (a) corresponds to the classical bulk transistor (back-gate of NMOS is biased to Vss and back-gate of PMOS to Vdd), and configuration (b) is a “faster” inverter because it has both low threshold voltages in PMOS and NMOS (back-gate of NMOS is biased to Vdd and back-gate of PMOS to Vss). Configurations (c) and (d) on the other hand, where the back-gates are biased at the same voltage Vss or Vdd, will be used to illustrate the behavior of the new topology: complementary inverter (cf. Figure 2.12).

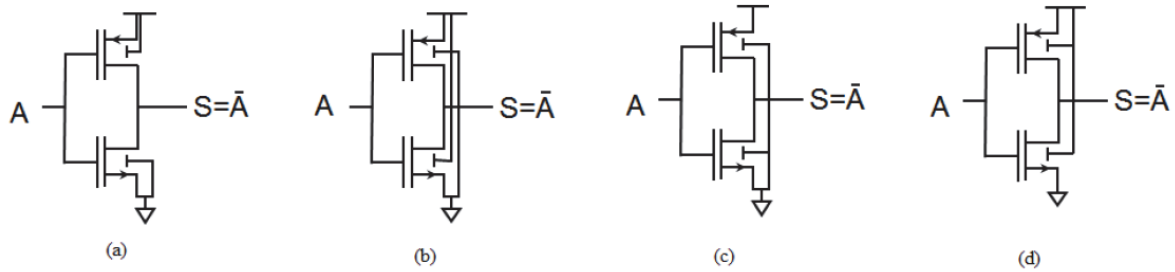

Figure 2.11: Different classical inverter implementations in UTBB-FDSOI technology

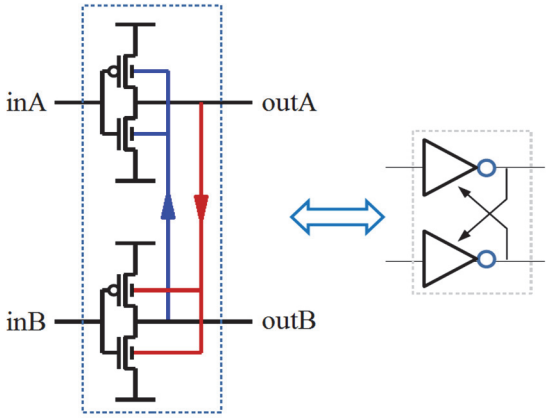

Figure 2.12: Basic complementary inverter gate

Figure 2.12 describes a complementary inverter composed by two identical inverters where both back-gates of PMOS and NMOS of one inverter are biased by the other. This is the structure that we propose to use in the complementary logic in our work.

The main idea is as follows: in each inverter, back-gates of both PMOS and NMOS transistor are controlled by the output voltage of the other inverter, their threshold voltages vary as the output of the other inverter changes. As a result, the output voltages of the gate control the back-gate

voltages. In such a way that if one output has a faster signal transition, the other output will be accelerated, and on the contrary, if one side has a slower signal transition, the other output will be decelerated. It means that asymmetry is attenuated. In other words, the complementary inverter improves the symmetry of the pair of outputs if its pair of inputs is 'reasonably' symmetrical.

The idea without considering of reality is meaningless. To be physically realized, such a structure need an extra well to control back-gate to avoid mixing with Vdd and Vss. UTBB-FDSOI technology also proposes a triple-well implementation solution.

2.2. Layout implementation for complementary inverter

Figure 2.13 presents the "nfettw" and "lvtpfettw" transistors structure which we choose for design from STMicroelectronics' UTBB-FDSOI 28 nm library [9]. They have the advantage of having a triple-well structure. It allows to use one back-gate to control the subtract voltage without any short circuit or leakage because of the equivalent two diode structure, if correct voltages are set in each well and substrate. It also takes profit of the ultra-thin oxide layer below the transition canal, the well and canal are separated, so both PMOS and NMOS can be built in the same P well. This is a mandatory advantage to organize the layout of complementary inverter as follows.

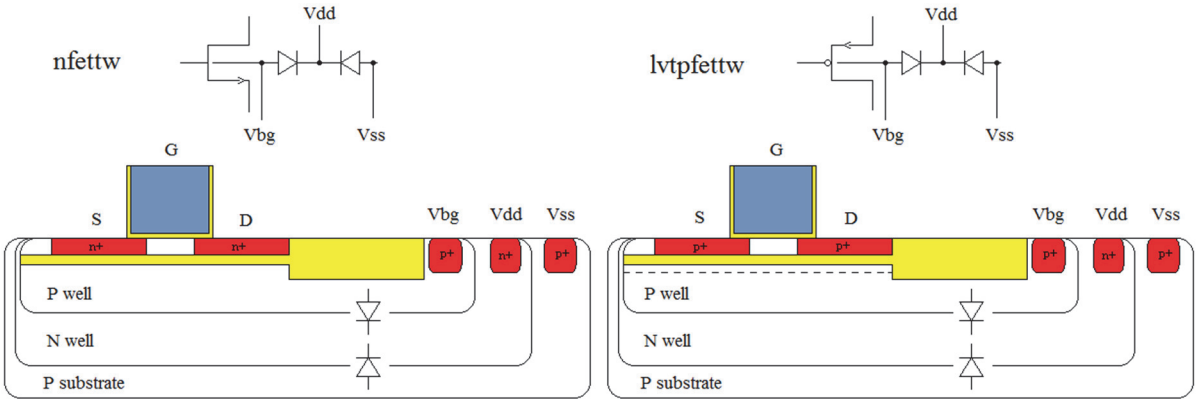

Figure 2.13: Triple-well structure in UTBB-FDSOI technology

In this layout implementation of complementary inverter as shown in Figure 2.14, one output can control both the back-gate voltages of PMOS and NMOS of the other inverter. The voltage of P substrat is fixed at Vss and middle N-well at Vdd as a blocked diode. The voltage of each P-well below the oxide layer varies from Vss to Vdd following the output voltages. So, it simplifies the layout without short circuit in the substrate area.

These pairs of "nfettw" and "lvtpfettw" transistors are used in all the following design and we will talk about layout implementation for different circuits in detail in chapter 5.

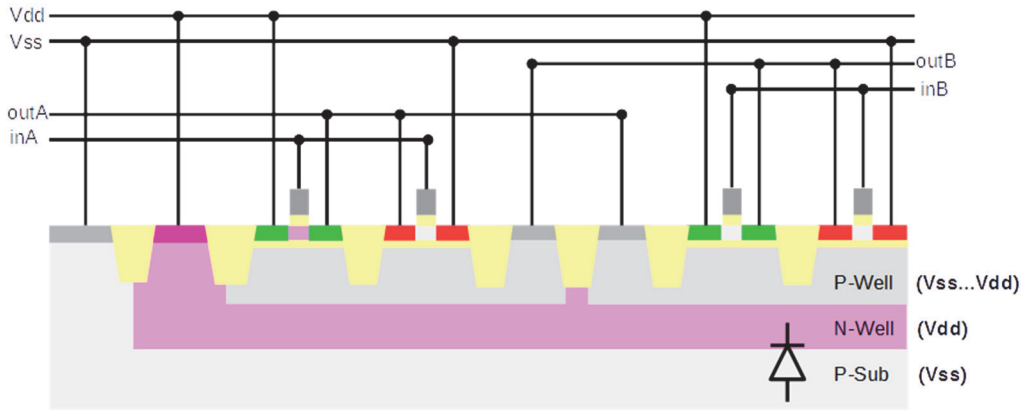

Figure 2.14: Layout structure of complementary inverter in UTBB-FDSOI technology

3. Static and dynamic study

3.1. Sizing strategy

The proposed complementary inverter provides both the low-to-high signal and high-to-low signal at the same transition with symmetrical characteristics, although the input signal is symmetrical, the output signal is sometimes asymmetrical due to internal sizes of transistors as shown in Figure 2.15.

To have good symmetry, the complementary outputs should cross at Vdd/2 (cf. Figure 2.15) and high-to-low time (Tp_{HL}), low-to-high time (Tp_{LH}) should be equalized.

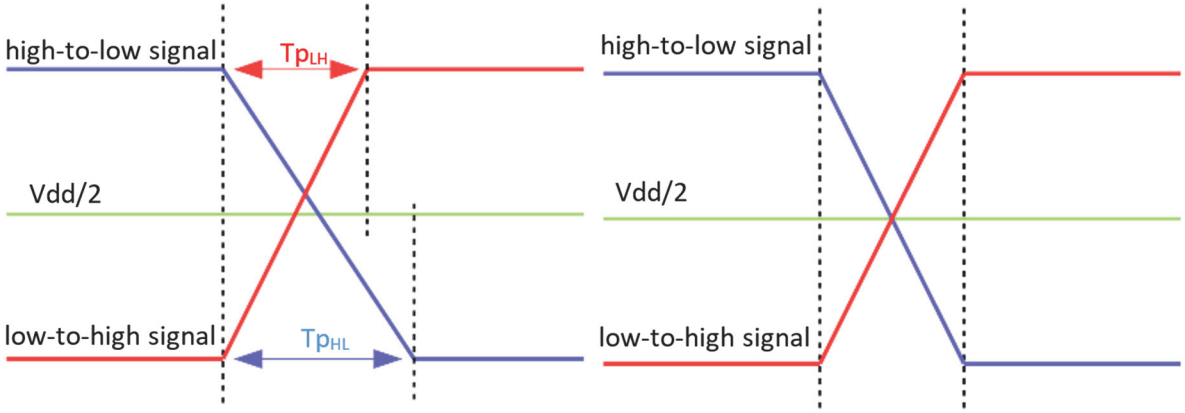

Figure 2.15: Asymmetrical and symmetrical signal transitions between the complementary signals

To get the "best" symmetry, in addition to the back-gate feedback described above, we equalize the DC output current of the NMOS driving the rise of the output signal and the DC output current of the PMOS transistor driving the fall of the output signal. This is not enough to get the symmetry, we need also to equalize the input capacitances of both transistors.

Figure 2.16 illustrates the transition situation for a complementary inverter charging inverters for example. We can observe that only one of the two transistors is "ON" in stable state. So, the input capacitance of an inverter is essentially the Cox capacitance of the NMOS when the input signal is high and the Cox capacitance of the PMOS when the input signal is low. During a transition the input capacitance is therefore changing dynamically. No matter how the transition changes, as long as the Cox capacitances of PMOS and NMOS are the same, the total input capacitance stays unchanged.

So, in addition to equalize the output currents, it is therefore important to build an inverter where the NMOS and PMOS Cox capacitances are also equal. The same current charging the same capacitance gives the same transition time.

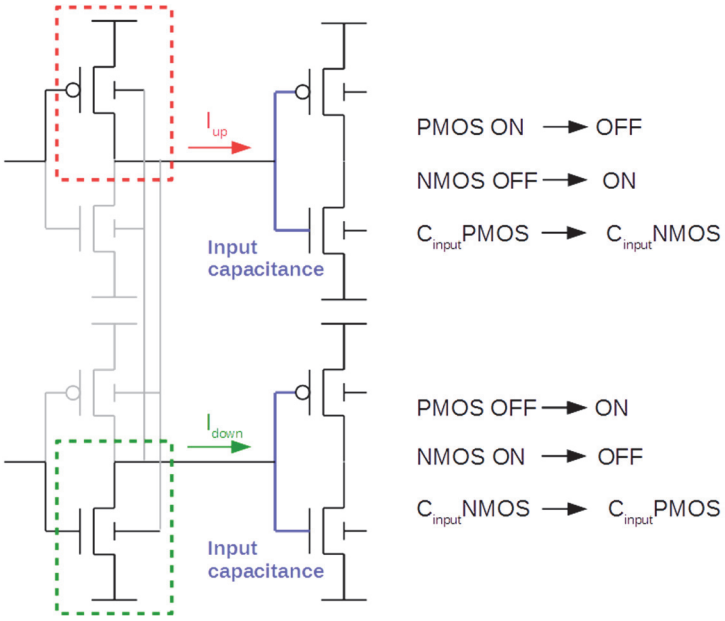

Figure 2.16: Symmetry ➔same current charging the same capacitance

To match the output currents (I_{up}=I_{down}), we will compensate the difference between KP_N and KP_P. So, we have to choose:

$$KPp * \frac{Wp}{Lp} = \mathrm{KPn} * \frac{Wn}{Ln} \tag{2.1}$$

In the first approximation, we can consider here that KP_N=3*KP_P. So, the sizes of the transistors are given by relation (2.2).

$$\frac{Wp}{Lp} = 3 * \frac{Wn}{Ln} \tag{2.2}$$

To match the capacitance for all the transition time, Cox_{PMOS} and Cox_{NMOS} should be the same. As capacitance is proportional to W*L, the sizes have to verify equation (2.3).

$$Wp*Lp = Wn*Ln \tag{2.3}$$

From equation 2.2 and 2.3, we can obtain the sizes to symmetrize the shapes of the transition up and down. First, we choose Wn=W and Lp=L as a reference (cf. equation 2.4 and 2.5), the other values can be verified by equation 2.5 to 2.7:

$$Wn = \boldsymbol{W} \tag{2.4}$$

$$Lp = \boldsymbol{L} \tag{2.5}$$

$$Wp = \sqrt{3} * \boldsymbol{W} \tag{2.6}$$

$$Ln = \sqrt{3} * \boldsymbol{L} \tag{2.7}$$

Figure 2.17 shows a layout example using this sizing strategy for inverter when $\frac{W}{L} = \frac{3um}{1um}$. In this configuration, both the PMOS and NMOS have the same current and the same input capacitance so it will have the same high-to-low time and low-to-high time.

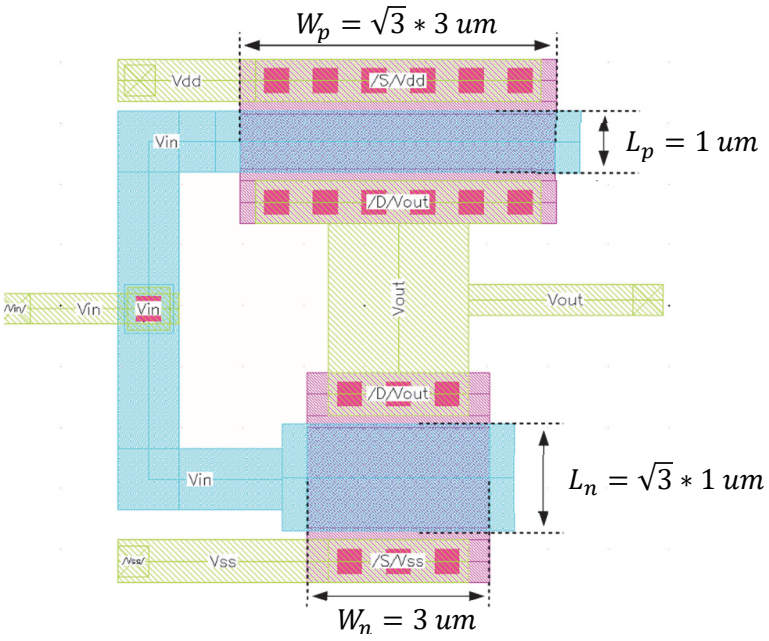

Figure 2.17: Layout example for inverter when W/L=3um/1um

This is the principle of our sizing strategy to symmetrize up and down transitions of a complementary inverter. Together with the short channel effects and other secondary effects [8], we finally fixed W=7um and L=30nm to obtained the following sizes (cf. relation 2.8) to take into account in SPICE simulation:

$$\text{PMOS: } Wp = 9.1\mu m/Lp = 30nm \quad \text{NMOS: } Wn = 7.0\mu m/Ln = 39\ nm \tag{2.8}$$

With these sizes, we made a DC simulation in Figure 2.18. The result shows that the complementary outputs S in blue and $\bar{S}$ in red are “perfectly” symmetrical and cross at 0.5V (Vdd/2), meeting the above requirements verifying the correctness of this sizing strategy.

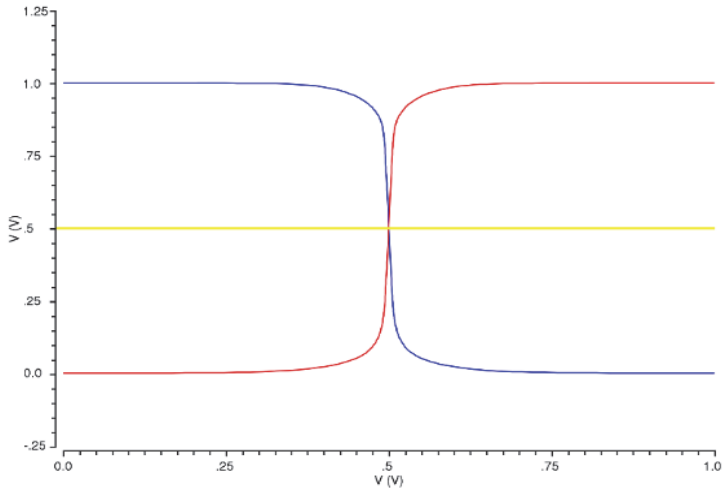

Figure 2.18: Simulated transfer function of the complementary inverter in typical conditions

3.2. Static study

To illustrate the static features for the proposed complementary inverter, first we have studied the DC transfer function. In Figure 2.19, we have plotted one output of a complementary inverter (blue curve in Figure 2.18) and the DC transfer function of the configurations (c) (green curve) and (d) (red curve) of the inverters presented in Figure 2.11 when the input signal is from 0 to 1 V. The output signal of complementary inverter gives a maximum slope of -50 at 0.5V which is clearly see much higher than that of the other two configurations.

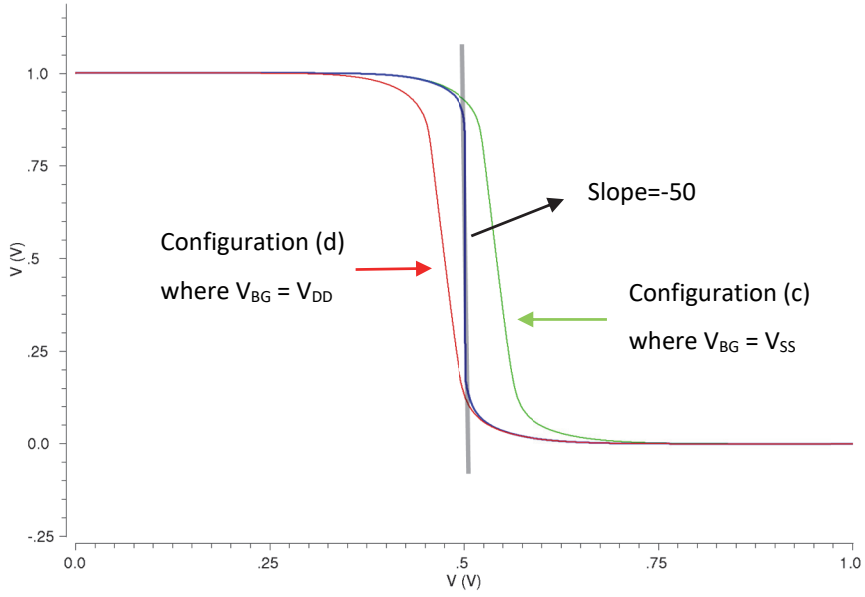

Figure 2.19: DC transfer functions of a complementary inverter and inverters of configuration (c) and (d)

Now we need discussions to explain these features. With back-gate connected to V_{DD}, the inverter in configuration (d) has a lower V_{TN}, at a result the output signal is easy to have a high-to-low transition as input signal rises. By contraries, with back-gate connected to V_{SS}, the inverter in configuration (c) has a lower V_{TP}, the output signal is more likely to keep high level and need a higher input voltage to force it to change from high to low.

Considering the upper inverter of complementary inverter as shown in Figure 2.20, we start with Vin=A=V_{SS}, so we have $\bar{A}$=V_{DD}, S=V_{DD} and $\bar{S}$=V_{SS} respectively. The back-gate of upper inverter is connected to output of the other inverter ($\bar{S}$=V_{SS}) corresponding to configuration (c). As a result, the upper inverter's output of complementary inverter (blue curve) follows the rise-to-fall trend of configuration (c) (green curve) at first. The DC simulation ends with Vin=A=V_{DD}, so we have $\bar{A}$=V_{SS}, S=V_{SS} and $\bar{S}$=V_{DD} respectively. In this case, the structure of the upper inverter corresponds to configuration (d). So, this output follows the red one. During the transition, the output goes down "directly" from V_{DD} to V_{SS} to have a relatively high slope of about -50.

The proposed complementary inverter combines the advantages of these two structures (configurations c and d) together, as a result, it works like a high gain inverter with a low V_{TN} for low voltage input and a low V_{TP} for high voltage input; therefore it has a better noise margin than classical inverters.

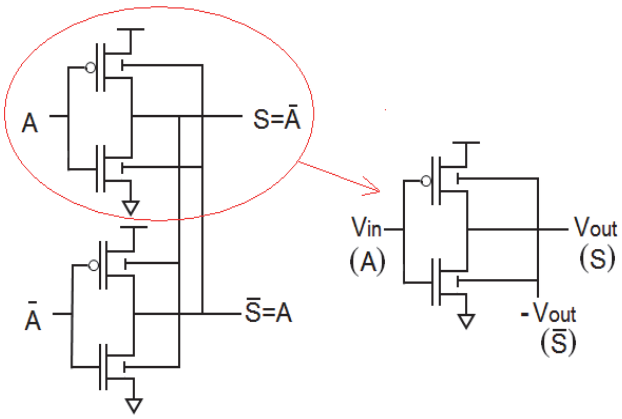

Figure 2.20: Analysis of one of the two inverters of the complementary structure

A small signal model around the midpoint (operating point at Vdd/2) helps to understand the feedback mechanism.

The back-gate of the proposed complementary inverter is controlled by the other inverter as described in Figure 2.21. The complementary inverter has two inputs and two outputs, which are defined in small signal as v_{in1}, v_{in2}, v_{out1}, v_{out1} respectively.

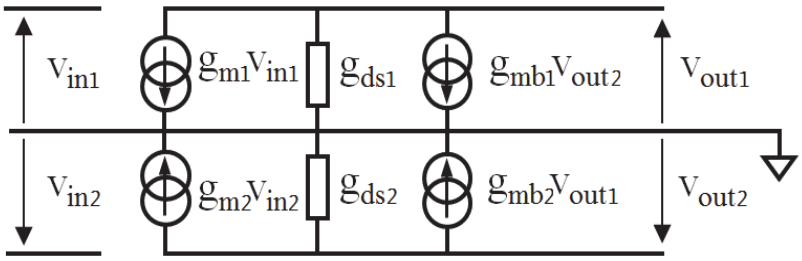

Figure 2.21: Small signal model during the signal transitions around $V_{DD}/2$

Thanks to these considerations, we can establish the small signal equivalent circuit of the complementary inverter, with:

$$g_{mi} = g_{mPi} + g_{mNi} \tag{2.9}$$

$$g_{dsi} = g_{dsPi} + g_{dsNi} \tag{2.10}$$

$$g_{mbi} = g_{mbPi} + g_{mbNi} \tag{2.11}$$

where $i = (1,2)$.

As we consider that the complementary inverter handles symmetrical signals which mean the complementary inputs and outputs, we have also the following relations:

So, the gain (i.e slope of signals) Avi of the proposed complementary inverter is deduced as:

$$Avi = \frac{-g_{mi}}{g_{dsi} - g_{mbi}} \qquad where \ \ i = (1,2) \tag{2.12}$$

The results could be optimized in order to simplify this equation. If we consider only one of the complementary inverter for example the upper inverter, as shown in Figure 2.20, which have one input and one output, we define as v_{in} and v_{out} in small signal. If the two inverters are perfectly symmetric, we can assume that the output variations (small signal around the static point Vdd/2) of the two inverters are differential. So, we can consider that the back-gate of the upper inverter is equal to $-v_{out}$. Moreover, because of its symmetry, these three parameters g_m, g_{ds} and g_{mb} have the same value in the two inverters. The small signal equivalent circuit of the upper inverter is shown in figure 2.22.

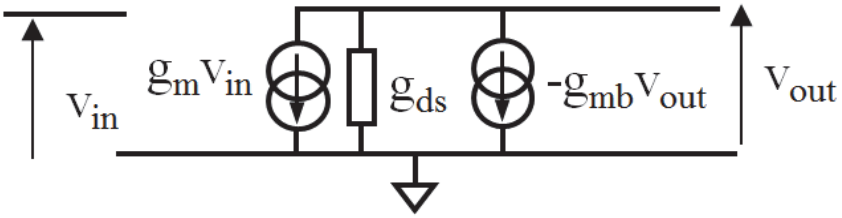

Figure 2.22: Small signal equivalent circuit of the half of complementary inverter

The gain of this circuit is given by equation 2.13.

$$Av = \frac{-g_m}{g_{ds}-g_{mb}} \tag{2.13}$$

In fact, this small signal equivalent circuit in Figure 2.22 and the gain in equation 2.13 are applicable for both inverters of the proposed complementary inverter because of its symmetry. So we can study one of the inverters to get the whole characteristic.

In our case with specific sizes, we have chosen (W=7um and L=30nm), we can extract the parameters using SPICE simulation which are given in Table 2.1.

Table 2.1: SPICE parameters and characteristics of the UTBB-FDSOI transistors

	g_m (µA/V)	g_{ds} (µA/V)	g_{mb} (µA/V)	V_{Th} (V)	I_{DS} (µA)	KP (µA/V^2)
PMOS	3180	380	230	-0,26	-385	44
NMOS	4350	290	285	0,33	380	146

We can therefore deduce from equations 2.9, 2.10, 2.11 and Table 2.1:

$$g_m = (3180 + 4350)\ \mu A/V = 7530\ \mu A/V$$
$$g_{ds} = (380 + 290)\ \mu A/V = 670\ \mu A/V$$
$$g_{mb} = (230 + 285)\ \mu A/V = 515\ \mu A/V \tag{2.14}$$

Finally, from equation 2.13 we obtain the gain at operation point Vdd/2 which is much high than the existing inverters:

$$|A_v| = \frac{7350}{670-515} = 49 \tag{2.15}$$

With the relatively high gain, this complementary structure gives us an opportunity in other analog design especially in ring oscillator and VCRO which will have better performances.

Moreover, from the equation 2.13, it is possible to obtain g_{mb}=g_{ds} in theory to reach an infinite gain and so to strongly decrease the jitter and increase the noise margin of the inverter. The gain could be optimized by adjusting further the length L of the transistors to match better g_{mb} and g_{ds}. Table 2.2 summarizes the slope of the DC transfer function for two other sizes of the transistors.

Table 2.2: Gain of the inverter vs transistors' size

	W (µm)	L (nm)	Gain |A|	W (µm)	L (nm)	Gain |A|
PMOS	9.2	32	116	9.33	33	348
NMOS	7.0	42		7.0	44	

It should be notice that if the value of g_{ds}-g_{mb} is negative, the complementary inverter becomes a latch as shown in Figure 2.23, although it will not affect too much our application, it's better to avoid this situation by choosing the right size.

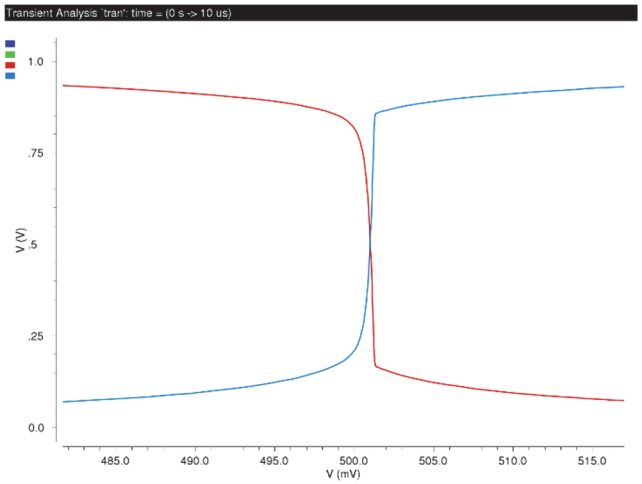

Figure 2.23: A latch appears when g_{ds}-g_{mb} is negative

So, these results show that it is possible to adjust DC gain with the choice of sizes to reach an infinite gain. In practice, this ideal value is only a theoretical target. However, it should be noted that this gain will be very sensitive to variations in transistor sizes.

3.3. Dynamic study

Thanks to the back-gate control structure, we proposed this complementary inverter whose faster output can accelerate the slower one, and the slower output can decelerate faster one also. Here we will design a simulation method to validate this concept.

Our approach is to introduce two opposite signals at the input of a complementary inverter with some delay between each other. We measure the input delay (Δt_{in}) and output delay (Δt_{out}). If $\Delta t_{out} < \Delta t_{in}$, we can conclude that mismatch is effectively reduced by the symmetrization capability of the complementary inverter.

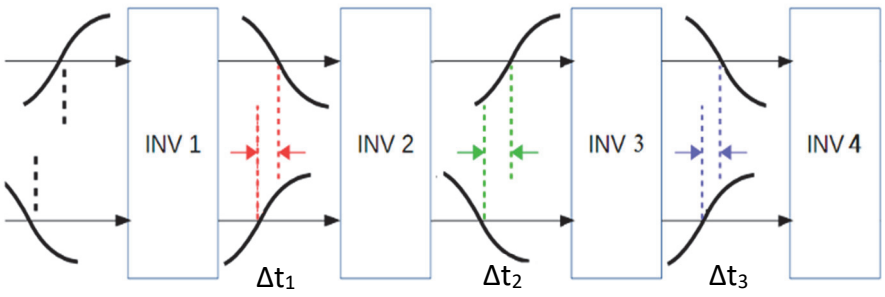

Figure 2.24: Topology to validate the symmetrization of complementary inverter

In practice, there is a little difference as shown in Figure 2.24, because a small offset exists at Vdd/2 even there is no delay between the two opposite signals. So it's better to measure the delay Δt_1 after INV1 and the delay Δt_3 after INV3 because they have the same fall-to-rise or rise-to-fall trend.

If α represents the symmetrization capability for complementary inverter, this value is given by equation 2.16:

$$\alpha = \frac{\Delta t_2}{\Delta t_1} = \frac{\Delta t_3}{\Delta t_2} \tag{2.16}$$

From this equation, we can therefore deduce:

$$\Delta t_2 = \sqrt{\Delta t_1 * \Delta t_3} \tag{2.17}$$

The simulation result is shown in Figure 2.25, Δt_1 is considered as Δt_{in}, and Δt_2 as Δt_{out}. We can see the red curve is the y=x uncorrected reference and the blue curve is the complementary inverter result: the output delay is reduced by about 10%:

$$\Delta t_{out} = 0.9 * \Delta t_{in} \tag{2.18}$$

in the linear part of the characteristic curve when the input error is less than 30ps. So, an eventual asymmetry of an input signal is reduced thanks to the back-gate control structure of the proposed complementary inverter.

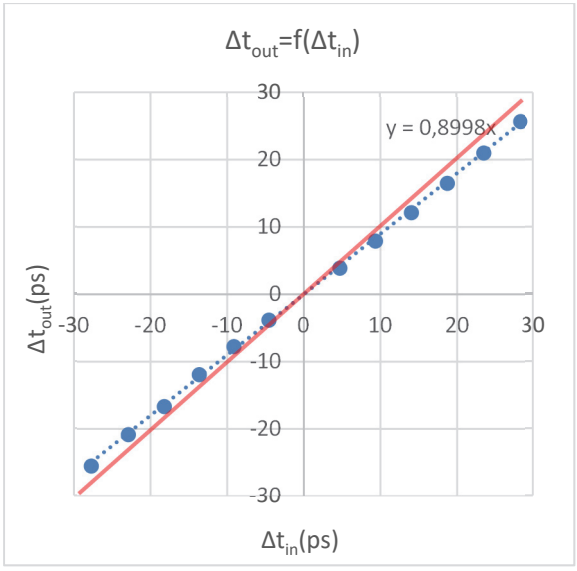

Figure 2.25: Output delay in relation to input error

This advantage can be used in ring oscillator which is composed by four complementary inverters for example, because if there are noises or mismatches, it will automatically correct during the oscillation which we will talk about in the next chapter.

4. Complementary logic with back-gate controlled in UTBB-FDSOI

Using the same back-gate control mechanism, we can build more complex logic gates [11]. For instance, a NAND complementary gate will be made from two NAND elementary functions realized respectively with the structure of a standard NAND gate (NAND function in positive logic) and a standard NOR gate (NAND function in negative logic) linked by their back-gate. Table 2.3 gives the true table of a complementary NAND cell which shows all possible inputs and corresponding symmetric outputs.

Table 2.3: True table of a complementary NAND cell

A	$\bar{A}$	**B**	$\bar{B}$	**X**	$\bar{X}$
0	1	**0**	1	**1**	0
0	1	**1**	0	**1**	0
1	0	**0**	1	**1**	0
1	0	**1**	0	**0**	1

This complementary structure is flexible because by simply crossing inputs and/or outputs as shown in Figure 2.26, the same physical layout realizes also complementary AND, NOR and OR functions. All of them, built with the same physical structures and elements, exhibit therefore the same speed.

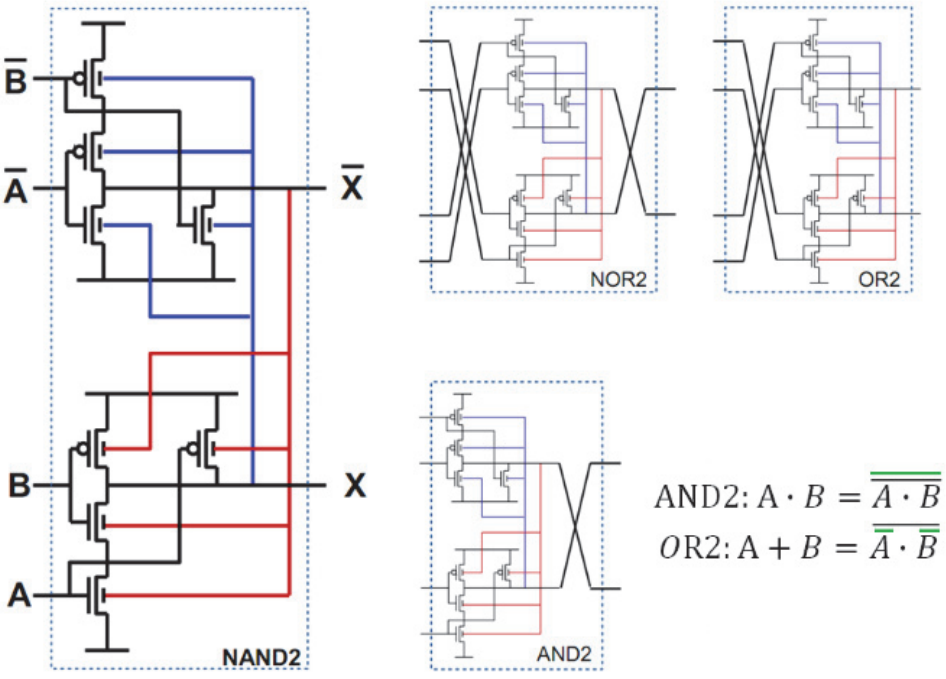

Figure 2.26: Different logic gates realized by complementary NAND

According to the discussion above, combining complementary logic and back-gate control together is the best solution to satisfy the requirements of high precision symmetry signal circuit.

We can still make further improvement on structure as shown in Figure 2.27.

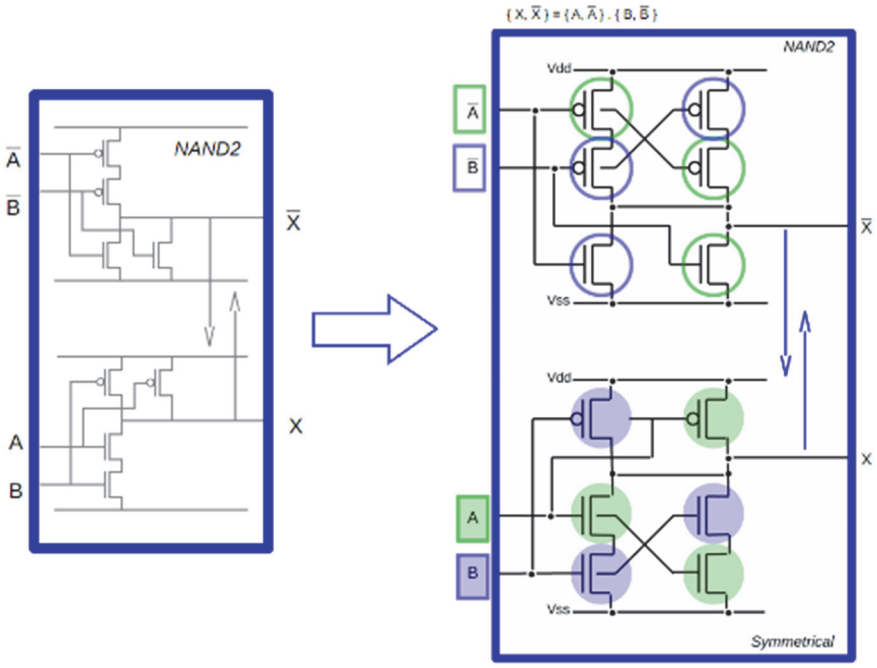

Figure 2.27: Improved structure for complementary logic

Because in original complementary NAND, we consider the lower gate for example, the two inputs A and B control the PMOS in parallel, and NMOS in series, if only one of the two inputs is on and the other is off, one of the two PMOS and NMOS is on also. There is no difference for parallel PMOS, but for series NMOS, one is closer to output X and the other is closer to Vss from which the equivalent impedances will be different. The difference is small but still affects the performance.

This structure can be improved to be more symmetrical by separating each NMOS in two, and there are two branch of series NMOS, put the two NMOS in different position for each branch (cf. Figure 2.27), then we have the same structure when only one of the two inputs is on. In actual situations, digital circuits are composed of different logic gates. A deeper study is done to make different logic gates have the same time delay. We use a similar formula according to equation 2.1 to 2.3 to symmetrize not only input capacitance but also output current in different gates.

Table 4 describes a size example in detail for complementary inverter, complementary NAND and complementary AO22 using the sizing strategy proposed in chapter 2.3.1 to get a better symmetry.

Table4: Size examples for different complementary logic gate

	Wp(nm)	Lp(nm)	Wn(nm)	Ln(nm)	Wp*Lp	Wn*Ln	Wp/Lp	Wn/Ln	Cin	Cin total Value	Drive
COMP INV	346	30	200	52	10392	10392	11,5	3,8	Wp*Lp+Wn*Ln	20785	Wp/Lp=3*Wn/Ln
NOR for COMP NAND2	173	30	200	52	5196	10392	5,8	3,8	2*Wp*Lp+Wn*Ln	20785	2*Wp/Lp=3*Wn/Ln
NAND for COMP NAND2	346	30	100	52	10392	5196	11,5	1,9	Wp*Lp+2*Wn*Ln	20785	Wp/Lp=3*2*Wn/Ln
COMP AO22	173	30	100	52	5196	5196	5,8	1,9	2*(Wp*Lp+Wn*Ln)	20785	Wp/Lp=3*Wn/Ln

Figure 2.28 illustrates a simulation example for a complementary NAND of all the inputs and outputs using appropriate sizes. The complementary output signals conform to the truth table and cross at Vdd/2. Moreover, it has almost the same Tp_{HL} and Tp_{LH} at both complementary signals in one transition and each transition when the same input signal rises or falls which verifies a good symmetrical performance.

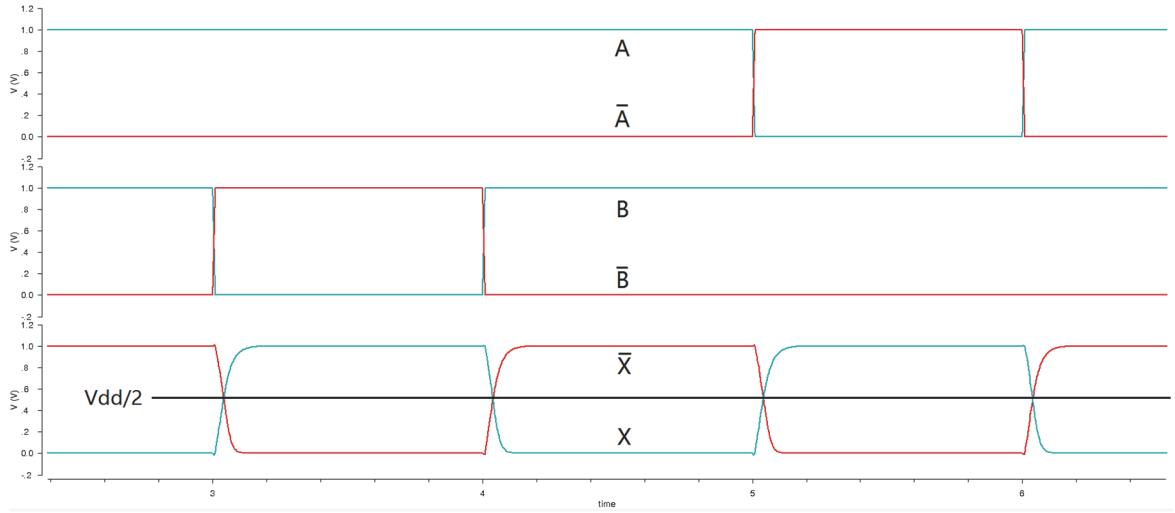

Figure 2.28: Transient simulation of a complementary NAND gate

The complementary logic with back-gate control in UTBB-FDSOI technology opens a new world in “analog quality” digital logic which could be build a standard cell library having compatible structures, the same delay and better performances.

5. Conclusion and application examples

In this chapter, first we have studied the glitch problems in traditional Karnaugh map logic design, so it is necessary to introduce differential logic or complementary logic where high-performance and symmetrical signals are needed. Then we give our opinion: using back-gate V_{th} control, complementary logic in UTBB-FDSOI technology is the best solution to satisfy the requirements of high precision symmetry signal circuit.

Here we proposed a novel structure: complementary inverter which has a high gain and better noise margin compared to classic inverters. Moreover, it can reduce the mismatches between the

two opposite signals because of back-gate control. Static analysis, dynamic analysis and sizing strategy are considered to verify our idea.

Then we extend this design concept to complementary logic which can be used for any digital cells to generate more stable, symmetrical and resilient output signals. It also provides new design solutions for some current circuits.

For example, complementary logic can help to build no-overlap symmetrical signals for switched-capacitor circuits. Clock generators are important elements interfacing the analog and digital modules of integrated mixed-signal circuits. The analog modules built from switched capacitors circuits (cf. Figure 2.29) are very sensitive to the quality of their driving clocks.

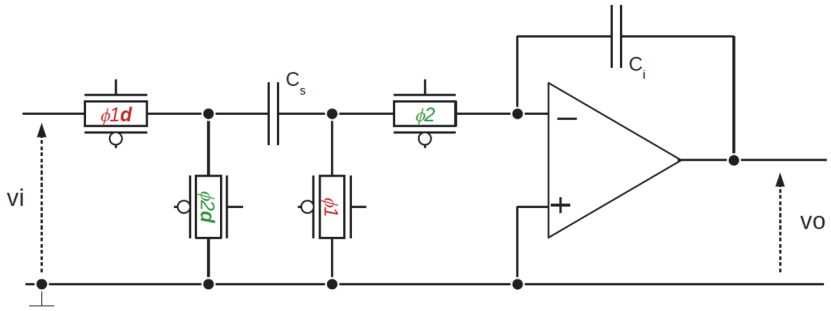

Figure 2.29: A simple switched capacitor integrator with four CMOS switches

We have already built a novel analog clock generator with complementary logic cells in UTBB-FDSOI delivers the robust symmetrical clocks required to control high performances differential switched capacitor circuits. Using back-gate feedback and sizing respecting static and dynamic symmetry, the proposed solution is very tolerant to inherent process variations to the deep nanometer CMOS processes. More details are given in reference [12].

Another example is to build the components of quadrature clock generator, for example ring oscillator which will be presented in the next chapter.

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Chapter III – Ring oscillators

1. Presentation of LC and ring oscillators

1.1. Introduction

An oscillator is an electronic circuit that produces a periodic, oscillating signal. An oscillator can be controlled to constitute the central part of PLL to make frequency synthesizer. The oscillator is often the sub-circuit with the highest operating frequency in RF circuits, its phase noise, power consumption and adjustable frequency range determine the performances of the whole bloc of PLLs.

The essence of the oscillator is a nonlinear feedback system as shown in Figure 3.1, where A is the gain of the amplifying element of the circuit and β(jω) is the transfer function of the feedback path. To produce a stable oscillation, two conditions must be met, the so-called "Barkhausen's criterion" [1]:

1 - The loop gain is equal to unity in absolute magnitude, that is, $|\beta A| = 1$;

2 - The phase shift around the loop is 0 or an integer multiple of 2π: $\angle \beta A = 2n\pi$, $n \in \{0, 1, 2, \ldots\}$.

Intuitively, only when the loop gain is 1, the oscillation amplitude can be stabilized, neither increasing nor attenuating. When the signal along the feedback loop has a total phase of zero, the starting point is the ending point, becoming a self-circulating autonomous system which doesn't require any external drive signals.

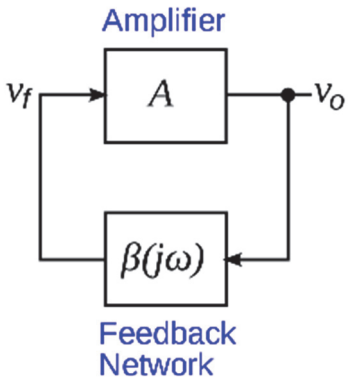


Figure 3.1: Block diagram of a feedback oscillator circuit

Barkhausen's criterion is a necessary condition for oscillation but not a sufficient condition: some circuits satisfy the criterion but do not oscillate. A classic counterexample is that two inverters

are connected in series to form a loop with a loop phase of zero and a loop gain of 1, but the node voltage of the circuit will only saturate at Vdd or Vss without oscillation.

There are two main types of electronic oscillator in today's CMOS technology: harmonic oscillators and relaxation oscillators [2] [3] [4].

Harmonic Oscillators, which are known as linear oscillators, generates a purely sinusoidal waveform with constant amplitude and frequency. In harmonic oscillators, the combination of the inductor and capacitor produces a "tuned" circuit that has a resonant frequency (f_r), in which the reactance of active components such as capacitive and inductive are equal and cancel out each other, leaving only the resistance of the circuit to oppose the flow of current.

Relaxation Oscillators on the other hand, generate complex non-sinusoidal waveforms that change very quickly from one condition of stability to another such as "square-wave", "triangular-wave" or "sawtooth-wave" type waveforms. The period of these oscillations is determined by the duration of equivalent resistor and capacitance charge and discharge.

LC oscillators and ring oscillators are classical representatives of these two types of high speed oscillators in high frequency applications which we will study in following sections.

1.2. LC oscillators

Figure 3.2 is an equivalent small-signal circuit of LC oscillator, where the inductor and capacitor form a resonator. The essence of a resonator is a passive network which can produce some form of damped oscillation under a certain initial excitation. There is energy loss in the process of forming an oscillation, if no active source continuously injects new energy into the system, the resonator itself will gradually decay to zero.

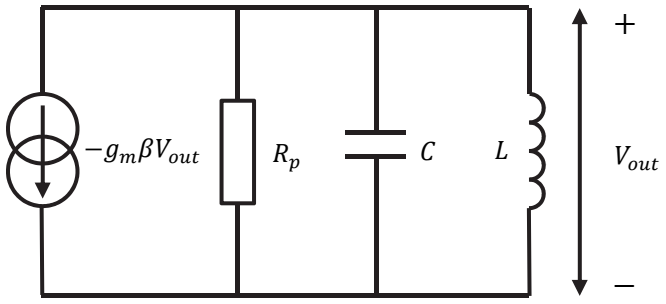


Figure 3.2: Small-signal circuit for LC oscillators

For this LC resonator, the energy loss is represented by the equivalent resistance R_P. Here a simple model of a transistor is used to represent an active source, which function is to initiate

oscillation and keep stable oscillations by its own nonlinearity and supplement the energy loss of the resonator. The main parameter is the transconductance g_m. If the feedback coefficient from the resonator to the transistor gate is β, the loop transfer function is:

$$\mathrm{H}(s) = \frac{-g_m\beta}{\frac{1}{sL}+sC+\frac{1}{R_P}} \tag{3.1}$$

According to the root locus method, the solution that makes H(s) = -1 can be obtained, and its real part is equal to $\frac{-(\frac{1}{R_P}+g_m\beta)}{LC}$.

Only when the pole is at the right side of s plane, the system can produce oscillation, i.e.:

$$g_m\beta < -\frac{1}{R_P} \tag{3.2}$$

This is an important condition for oscillation. After the oscillation occurs and the signal increases, the transconductance g_m of the active source gradually decreases. When the equivalent value is exactly equal to $1/R_P$, the complementary energy of the active source just counteracts energy loss of the resonator; the system thus realizes stable oscillation.

The resonator is a key component of LC oscillators, and its performance essentially determines the overall performances. The most important indicator of a resonator is the quality factor Q which characterizes a resonator's bandwidth relative to its center frequency [5]. Higher Q indicates a lower rate of energy loss relative to the stored energy of the resonator; the oscillations die out more slowly.

There are three common definitions of the quality factor Q [6]. For an RLC circuit, Q is defined as the frequency-to-bandwidth ratio of the resonator:

$$\mathrm{Q} = \frac{f_r}{\Delta f} = \frac{\omega_r}{\Delta\omega} \tag{3.3}$$

where f_r is the resonant frequency, Δf is the resonance bandwidth.

A more general definition is 2π times the ratio of the energy stored in the oscillating resonator to the energy dissipated per cycle:

$$\mathrm{Q} = 2\pi\frac{energy\ stored}{energy\ dissipated\ per\ cycle} = 2\pi f_r\frac{energy\ stored}{power\ loss} \tag{3.4}$$

It can be measured by adding a step input and observing the decay of the output signal.

In the third definition, the resonator is connected to an oscillator and behaves as a feedback system. Q is equal to the rate of change of the oscillator loop transfer function around the oscillation frequency ω_0 multiplied by the resonant angular frequency divided by 2:

$$\mathrm{Q} = \frac{\omega_0}{2}\cdot\frac{dH(\omega)}{d\omega}\Big|_{\omega_0} \tag{3.5}$$

Since the amplitude of H(ω) is the largest near the oscillation frequency, where the amplitude change rate is 0, thus the Q value is equal to its phase change rate, that is,

$$Q = \frac{\omega_0}{2} \cdot \frac{d\varphi(\omega)}{d\omega}\Big|_{\omega_0} \tag{3.6}$$

As shown in Figure 3.3, the higher the phase change rate near the oscillation frequency ω_0, the higher quality factor Q of oscillators.

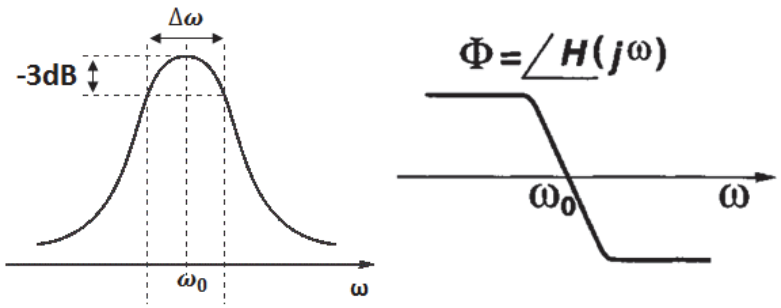


Figure 3.3: Definition of quality factor Q

LC oscillators are the most common type of oscillators in integrated wireless communication circuits. Due to good phase noise characteristics and their ease of implementation, LC oscillators are basically the only oscillator type that can meet the requirements of wireless communication. Nowadays there are different kinds of LC oscillators in CMOS technology such as Cross-coupled oscillator, Colpitts oscillator, Hartley oscillator etc. which generally use on-chip integrated inductors and capacitors [7][8]. The inductor is usually realized by a special thick metal wiring layer, which requires a wide metal and narrow space and capacitor is realized by MOM (Metal Oxide Metal) capacitor or MIM (Metal Insulator Metal) capacitor. The quality factor Q of these special process manufacturing inductors and capacitors is quite good, but the process requirements are very strict, and it will enlarge the area, therefore the cost is relatively high.

1.3. Ring oscillators

The Ring Oscillator (RO) is another widely used oscillator type. Compared with LC oscillator, the ring oscillator is mainly used in circuits with relatively low phase noise specifications, such as digital clock generation and short-distance wired data transmission.

The simplest ring oscillator structure connects an odd number of inverters in a loop as shown in Figure 3.4. The oscillation period is twice the total inverter chain delay:

$$T_o = 2nT_d \text{ and } f_o = \frac{1}{2NT_d} \tag{3.7}$$

where N is the number of stages in ring oscillators.

In the example of Figure 3.4, n=3, it has an oscillation period of $6T_d$.

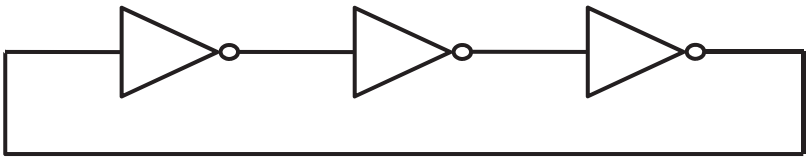


Figure 3.4: Three-stage single-ended ring oscillator

Because no inductor is needed, a significant advantage of the ring oscillator is its small footprint and high integration, as well as a large adjustment frequency range.

The self-oscillation frequency of ring oscillators is based on the time constant of the charge and discharge of capacitors through resistors. Resistors being pure loss components, these oscillators have small Q values. This is in strong contrast with LC oscillators, because the self-oscillation frequency of a LC oscillator is based on the resonant frequency of its quasi-lossless LC resonator, its Q value is much larger than 1. As a result, the phase noise of a typical ring oscillator is far less than that of an LC oscillator.

We can use the third definition of quality factor i.e. the rate of change of the oscillator loop transfer function around the oscillation angular frequency ω_0 multiplied by the resonant angular frequency divided by 2 to evaluate the effective Q value of ring oscillators.

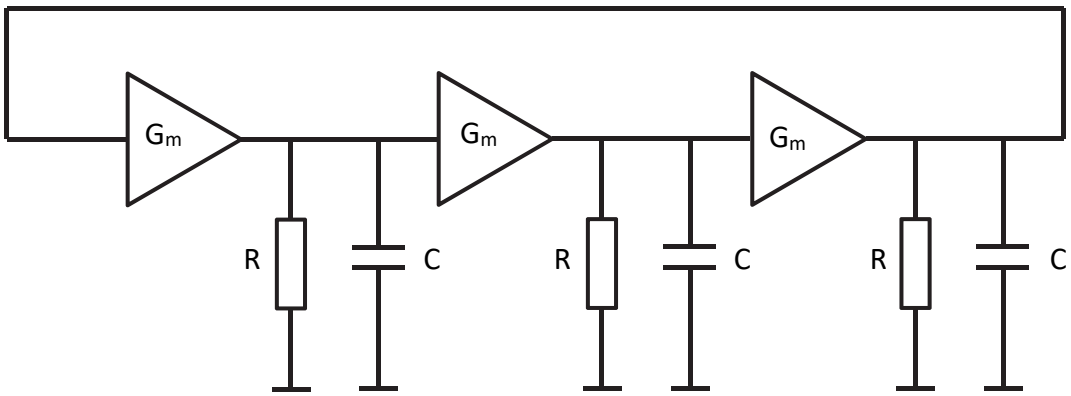


Figure 3.5: Three-stage single-ended ring oscillator equivalent model

A three-stage single-ended ring oscillator is taken as an example as shown in Figure 3.5, where the inverter is modeled by a transconductance G_m and RC load. The transfer function of each stage inverter is:

$$A_0(\omega) = -\frac{G_m R}{j\omega RC+1} \tag{3.8}$$

The transfer function of the whole loop is therefore:

$$\mathrm{H}(\omega) = A_0(\omega)^3 = (-\frac{G_m R}{j\omega RC+1})^3 \tag{3.9}$$

According to Barkhausen's criterion, the loop transfer function has a magnitude of 1 and a phase of 0 near the oscillation pulsation ω_{0SS} ($\omega_{0\ Small\ Signal}$), it can be deduced that:

$$\omega_{0SS} = \frac{\sqrt{3}}{RC} \tag{3.10}$$

$$G_m R = 2 \tag{3.11}$$

Thus, the equivalent Q value can be derived:

$$Q = \frac{\omega_{0ss}}{2} \cdot \frac{d\varphi(\omega)}{d\omega}\Big|_{\omega_{0ss}} \approx 1.3 \tag{3.12}$$

Here it is confirmed by an example of three-stage ring oscillator that the quality factor Q of a ring oscillator is quite small, generally less than 2 which is smaller than the quality value Q of LC oscillator.

In fact, G_mR is the gain of a single-stage inverter and the oscillation condition of the three-stage ring oscillator is that the minimum low-frequency gain of each inverter is 2, and the starting frequency is $f_{0SS} = \sqrt{3}/2\pi RC$. It can be notice that it's difference between equations 3.7 and 3.10, after all f_{0SS} is determined by small-signal equivalent R and C of each invertor and f_o results from large-signal current drive and capacitance of each stage. In other words, at the beginning the starting frequency of ring oscillator is determined by f_{0SS}, as the amplitude grows (cf. Figure 3.6), the frequency shifts to $f_o=1/2NT_d$ (cf. rel 3.7) and the system keeps stable [9].

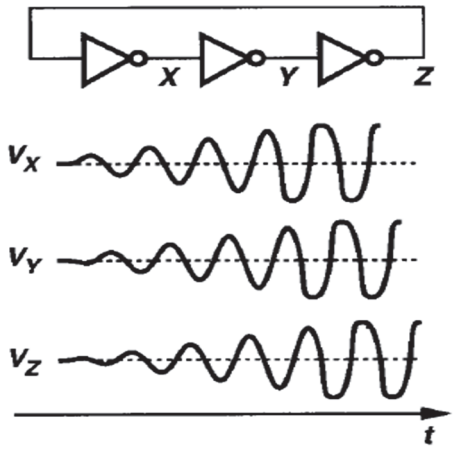


Figure 3.6: Oscillation process in ring oscillators

The number of stages in a ring oscillator is determined by requirements including speed, power dissipation, noise immunity etc. An oscillator with minimum phase noise is our focus. For a given oscillation frequency, phase noise can be degraded by increasing the number of stages of inverters, but at the expense of power consumption [10]. In [10], a relationship predicts phase noise of M-stage single-ended ring oscillator basing a known phase noise of N-stage:

$$L\{\Delta f\}_{M-stage} = L\{\Delta f\}_{N-stage} - 10log(\frac{M}{N})^{\frac{1}{2}} \tag{3.13}$$

With the help of this equation and taking an example of 5-stage single-ended ring oscillator using a 2um, 5V CMOS process [11], we can predict power dissipation and phase noise of M-stage ring oscillator as shown in Figure 3.7.

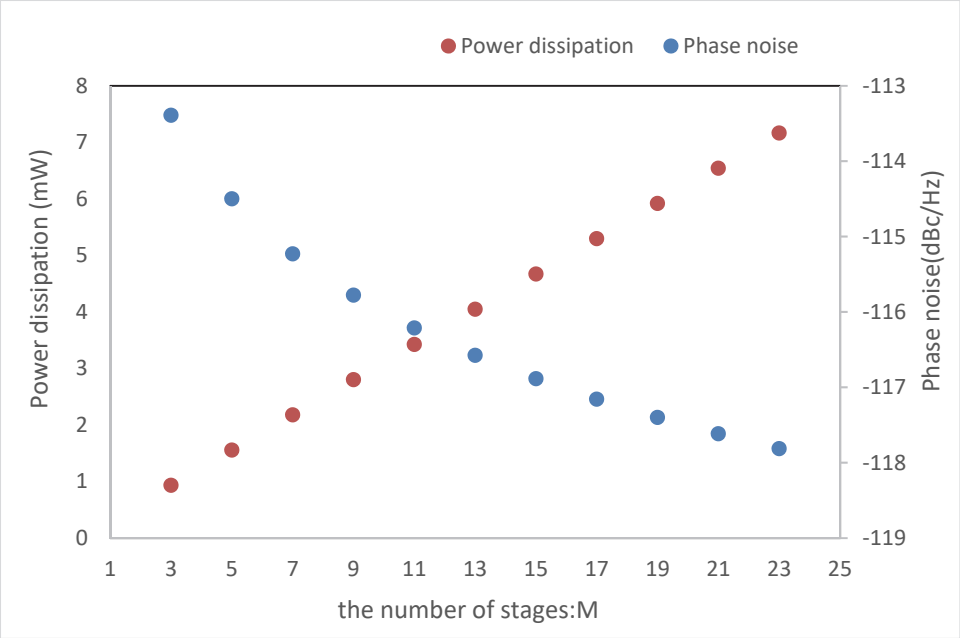


Figure 3.7: Power dissipation and phase noise of M-stage single-ended ring oscillator

Therefore, we should take a compromise among phase noise, power dissipation and number of stages to design ring oscillators that meet speed requirement. However, if power consumption is fixed at the same time, phase noise is independent on the number of stages and keeps constant. In this case, it's better to use a small number of stages to save costs [10].

Moreover, the number of inverting stages of a sing-ended ring oscillator stage must be odd, so that the circuit will not be locked. If differential structure inverters are used, an even number of inverters can also form a differential ring oscillator by simply configuring one stage such that it does not invert as shown in Figure 3.8.

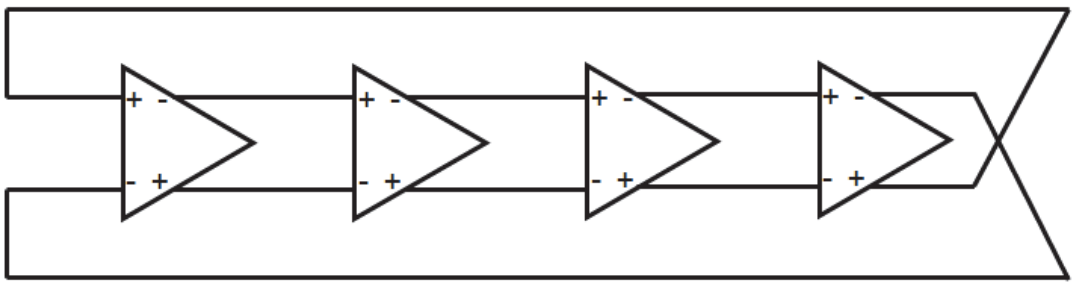
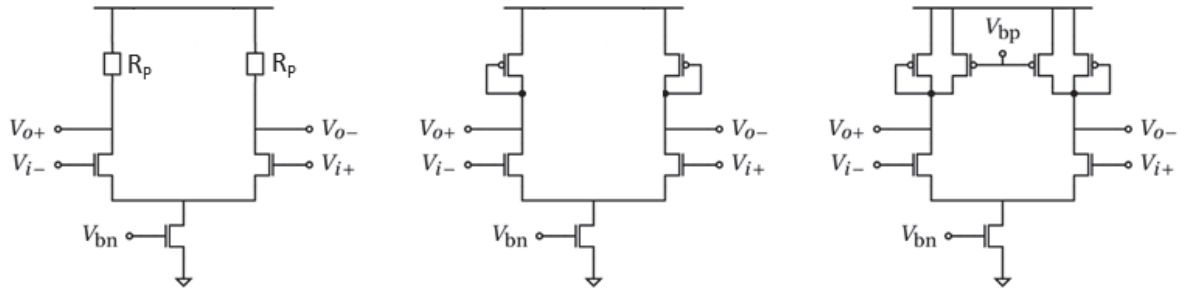


Figure 3.8: Example of a four-stage differential ring oscillator

Using the similar equations as described in equation 3.9 - 3.12, it can be deduced that the minimum gain is $\sqrt{2}$ which is smaller than that required in three-stage ring oscillator. In fact, the more stages the inverter has, the lower the start-up requirements of the ring oscillator.

Figure 3.9 illustrates three differential inverters used in differential ring oscillators [9], [12]. Figure 3.9(a) is the original differential structure where the resistor R_P is easy to cause errors. In Figure 3.9(b) the load is realized as a diode-connected PMOS but needs to cost one threshold voltage margin. Figure 3.9(c) is a more popular choice for implementing the differential inverter cell where symmetric load approximates a voltage-controlled resistor.



(a) (b) (c)

Figure 3.9: Three differential inverters using different loads

All of these have a few common disadvantages:

- The rate of voltage change at output is low and the voltage output amplitude is quite small, so it is not suitable for applications with low power supply voltage. Since our Vdd requirement is 1V, we need other solutions to replace differential inverters.

- The current source at the bottom produces additional noise.

- The output is not compatible with standard CMOS digital levels.

We will therefore propose to use the complementary inverters to avoid these problems.

1.4. Quadrature design

Oscillators can generate output signals with the same amplitude but different phases, among them, signals with a phase difference of 90 degrees are called quadrature signals or IQ signals which are often used in RF applications. They form the basis of complex RF signal modulation and demodulation, both in hardware and in software, as well as in complex signal analysis. In this section, we will present some classic methods to generate quadrature signals as follows.

A simple example of quadrature technique is to shift signal phases by ±45° by using RC-CR network as shown in Figure 3.10. It can be easily seen that the phase difference between Vout1 and

Vou2 is 90° for all frequency, but the output amplitudes are equal only at ω=1/RC. Since the absolute value of RC varies with temperature and process, the frequency varies at the point of equal-amplitude quadrature signals. The amplitudes can be equalized by means of "limiting stages", e.g. differential pairs in LO path. But it turns out that the phase and gain mismatch of the chains of limiters in I and Q paths will become significant [13].

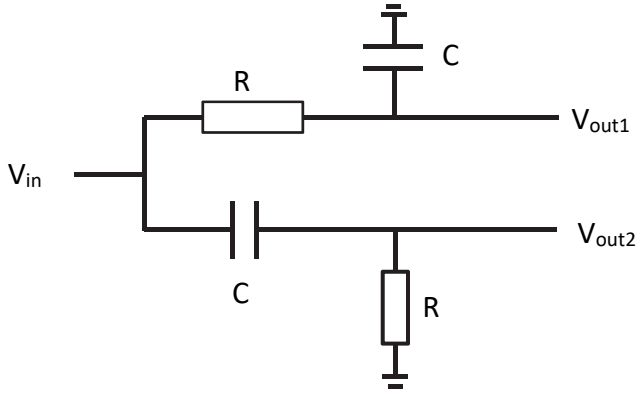


Figure 3.10: Quadrature network using RC-CR circuit

Havens' technique first splits the signal by approximately 90°, generating V_1 and V_2, and subsequently adds and subtracts these two phases, producing Vout1 and Vout2 as illustrated in Figure 3.11(a). If V_1 and V_2 have the same amplitudes, the angle between V_{out1} and V_{out2} is 90°, as shown in Figure 311(b). This can be proved by expressing $v_1 = Acos(\omega t)$, $v_2 = Acos(\omega t + \theta)$, then we have:

$$v_1(t) + v_2(t) = 2Acos\frac{\theta}{2}cos(\omega t + \frac{\theta}{2}) \quad (3.14)$$

$$v_1(t) - v_2(t) = 2Asin\frac{\theta}{2}sin(\omega t + \frac{\theta}{2}) \quad (3.15)$$

The limiting stages will equalize the amplitudes of v_1 and v_2 by phase shift circuit. Moreover, the adders' outputs will have different amplitude if θ ≠90°. These both applied to limiters, and AM-to-PM conversion becomes main concern. Amplitude mismatch is an important problem which have significant effect in the phase imbalance at the input if output impedance of the limiter is not low [14].

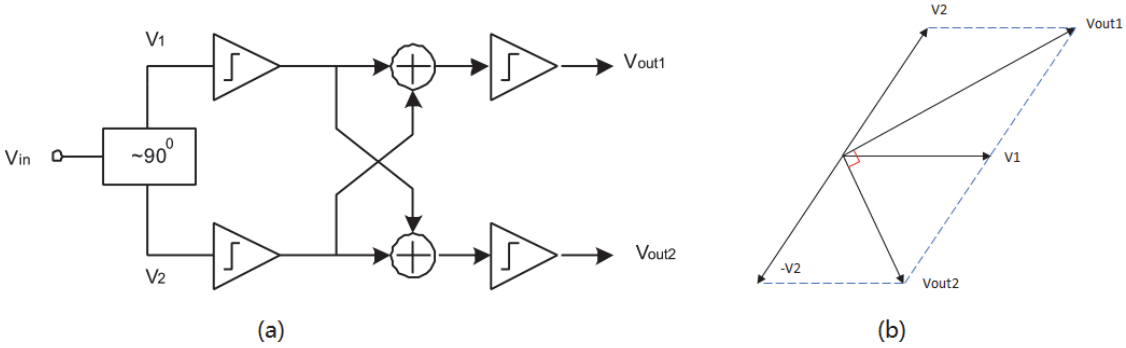


Figure 3.11: Quadrature network using RC-CR circuit

Figure 3.12 illustrates another approach to generating quadrature signals by using a master-slave flip-flop to divide a signal frequency by factor 2. If V_{in} has a 50% duty cycle, the two outputs have 90° out of phase. The main problem of this method is that generation and division of the signal may consume substantial power or simply be impossible due to technology limited [14].

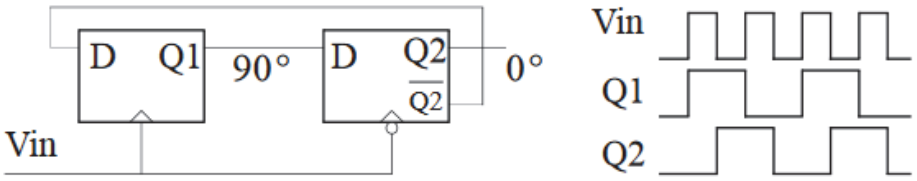


Figure 3.12: Frequency divisor as a quadrature generator

We proposed using quadrature ring oscillators to output quadrature signals that have simple structure, stable and symmetrical phases which will be presented in the next section.

2. Structure of RO in UTBB-FDSOI technology

2.1. Introduction

Since the body is fully depleted in UTBB-FDSOI technology, the random dopant fluctuation that plagues bulk CMOS is reduced as presented in chapter 1, which helps to improve performance even at lower Vdd. It can be predicted that the time jitter and phase noise of simple ring oscillator in UTBB-FDSOI technology is better than that in classic CMOS bulk technology built in the same situation. Not only that, as presented in chapter 2 section 2, in back-gate control structure of proposed complementary inverter, asymmetry of input signals could be reduced. So a ring oscillator with proposed complementary inverters in UTBB-FDSOI technology promises interesting performances.

2.2. Topology of ring oscillator built with complementary inverters

We start our analysis with a simple chain of 5 complementary inverters in series (Figure 3.13) and use the specific size in equation 2.8.

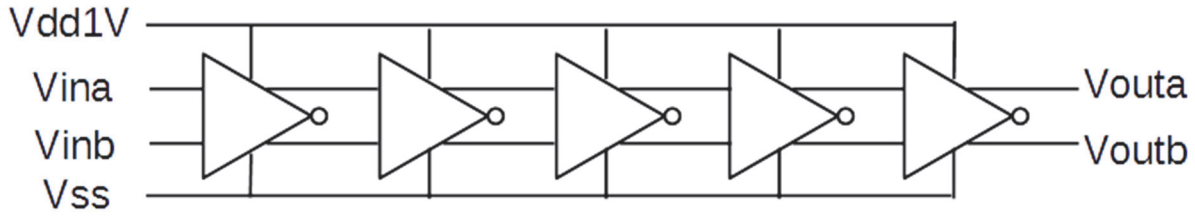


Figure 3.13: A chain of 5 complementary inverters

Using differential input signals, the differential output signals can be measured by a transient simulation.

The average delay time is the total delay time divided by the number of inverter cells:

$$T_d = \frac{T_d \, in \, total}{N} = 16.4 \, ps \tag{3.16}$$

Therefore, the theoretical oscillation frequency of a ring oscillator composed by four complementary inverters for example is

$$f_o = \frac{1}{2NT_d} = 7.6 \, GHz \tag{3.17}$$

Figure 3.14 illustrates two different topologies of ring oscillator built with complementary inverters. The structure on the left is composed by an odd number of complementary inverters in series forming two single ring oscillators where the two chains are independent of each other, only use back-gate to improve stability and slow down the oscillation frequency. The latter structure uses an even number of complementary inverters in series forming a quadrature ring oscillator which can output the required quadrature phases in ideal case.

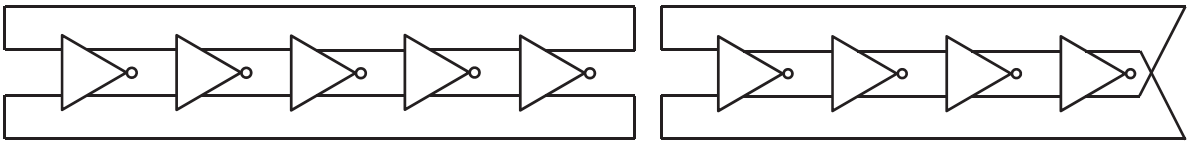


Figure 3.14: Two different topologies of ring oscillator

Because the circuit in a real environment has noise, disturbance, initial state, etc., so we set the initial state of the Spectre simulation [15], and the oscillator will start up automatically. Figure 3.15 shows the transition situation in another perspective, five stages repeat two states '0' and '1' sequentially and the states won't be locked, oscillation is like a small bubble that repeats circular motion in a round in each circular chain. In each complementary inverter, the back-gates are controlled by the other outputs, so it can output more robust and stable differential signals in each complementary inverter than in two single ring oscillators.

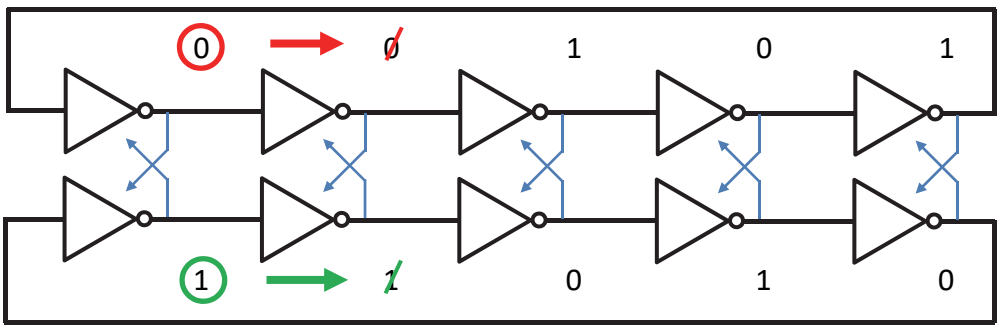


Figure 3.15: Transition situation in two single ring oscillators

A ring oscillator composed by five complementary inverters is build and from the transient simulation result as shown in Figure 3.16. We can see the measured period is about 165 ps, which corresponds to a frequency oscillation of 6 GHz with five phases (0°, 72°, 144°, 216°, 288°).

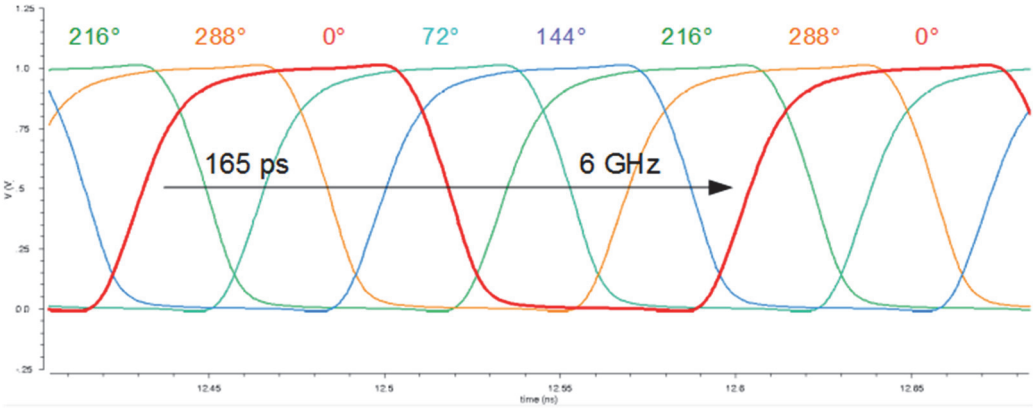


Figure 3.16: Transient simulation result of one of the two five-complementary-inverter ring oscillators

As presented in chapter 3.1.3, quadrature LO signals are frequently needed in both the RF receive path and transmit path, so we want to build ring oscillators consisting of an even number of stages to function as a quadrature clock generator.

2.3. Startup analysis for quadrature ring oscillators

The proposed quadrature ring oscillator consists of four stages of complementary inverter connected in series, where one stage should cross the outputs to the inputs of the next stage. It can be considered as eight single inverters forming a ring, where each pair of inverters are controlled by back-gates and output complementary signals.

First, we take the quadrature ring oscillator without back-gate control into account; a ring oscillator consisting of four complementary inverters can be equivalent to a ring oscillator consisting of eight common inverters. If given only one reset signal, as a ring oscillator composed of an even number of inverters has a locked state (cf. Figure 3.17), there is no state transition at each output, so it can't keep oscillating at all.

If given two differential signals at one output of complementary inverter, there is no locked state and fixed value at each output, during the oscillation, the differential signals in each pair of outputs transfer alternately from 0 to 1, just like two bubbles circulating in the circular chain as shown in Figure 3.18. However, without specific control the oscillation is not stable, the differential pair output signals cannot be maintained due to noise and interference, as a result the two bubbles will eventually collapse, and the oscillations will stop and lock at the state as shown in figure 3.17.

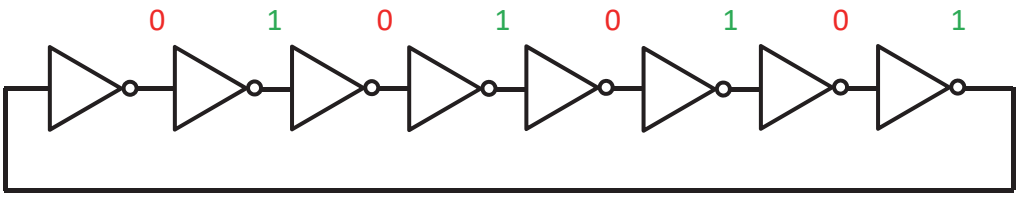


Figure 3.17: Transition locked situation in quadrature ring oscillators

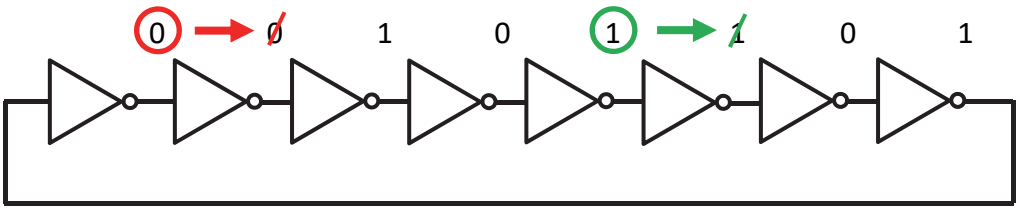


Figure 3.18: Transition situation in quadrature ring oscillators without back-gate control

Moreover, since quadrature ring oscillator has a transition locked state, it can't oscillate automatically, a startup design should be considered. Normally a transistor is seen as a simple switch and control the gate to change "on" and "off" state of Vds where a PMOS is used to pull up the target voltage to Vdd and NMOS is used to pull down to Vss.

For the "perfect" symmetry of the output signals of the complementary inverters, it is necessary to ensure that each output has the same load. As NMOS is more efficient than PMOS, in our design a NMOS is chosen after each output of complementary inverters to pull down the initial voltage to Vss for startup as shown in Figure 3.19. It should be noted that the back-gate and gate are connected to form a 'strong' transistor so that to reduce the load capacitance. For example, to pull down the output voltage of the upper inverter of complementary inverter outA to Vss, the gate voltage resetA is set to 1 to open Vds, and when resetA is 0, the outA keeps the original state unchanged.

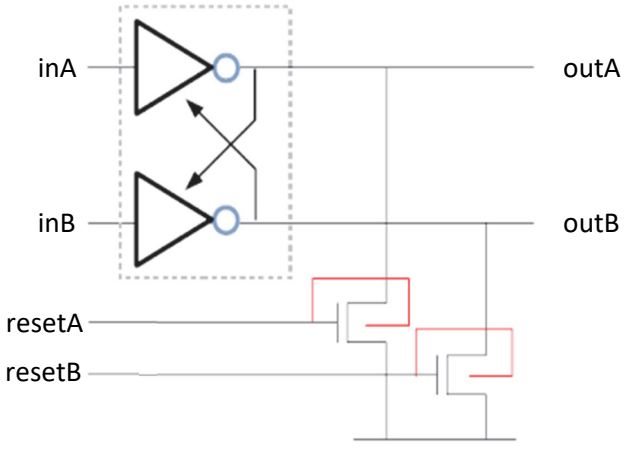


Figure 3.19: Structure of complementary inverter cell with startup NMOS

Table 3.1 gives all the four possibilities of reset configuration. When both resetA and resetB are set to 0, the two transistors are “off”, the outputs of complementary inverters are retained; when one of the two reset signals is set to 1, the associated output signal will be reset to Vss as expected; when both of the two reset signals are set to 1, the two outputs of this complementary inverter will be set to Vss, and the ring oscillator will be locked and can’t oscillate anymore as shown in Figure 3.20, so this state should be forbidden.

Table3.1: Output status in each reset configuration

resetA	0	0	1	1
resetB	0	1	0	1
outA	No action	No action	Reset to Vss (0)	Reset to Vss (0)
outB	No action	Reset to Vss (0)	No action	Reset to Vss (0)
State	Oscillation	Startup configuration		Forbidden

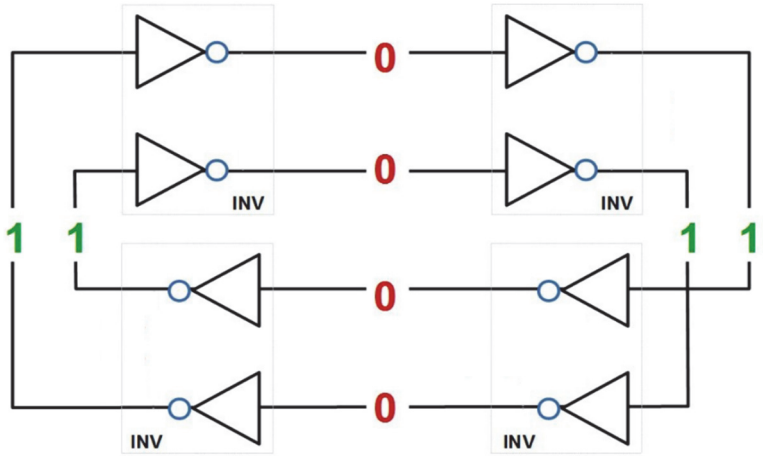


Figure 3.20: Forbidden state which is locked

Being differential signals of outputs for one complementary inverter is a necessary condition for the oscillator to start. Using NMOS transistors can only pull down the voltage to 0, notice the complementary signal can be obtained from the output of the next stage inverter, so two stages of complementary inverter (cf. Figure 3.21) should be considered to study the start up for oscillators. For example, if outA1 and outB2 are set to 0 at the same time, outA2 will change to 1 after one transition time T_d, which gives a rough differential signal pair (outA2, outB2), because of the self-correction characteristic of complementary inverter; it will form a robust and stable complementary signal after several transitions and the oscillator keeps oscillate as shown in Figure 3.22.

Table 3.2 gives all the configuration possibilities for two-stage complementary inverters. To obtain a rough differential signal pair at the output of the second stage, we need to initialize one of the output voltages of the first stage and the other output voltage of the second stage (blue areas).

During the oscillation, all switches are kept “off”, that is to say, the reset signal are all set to 0 (green areas).

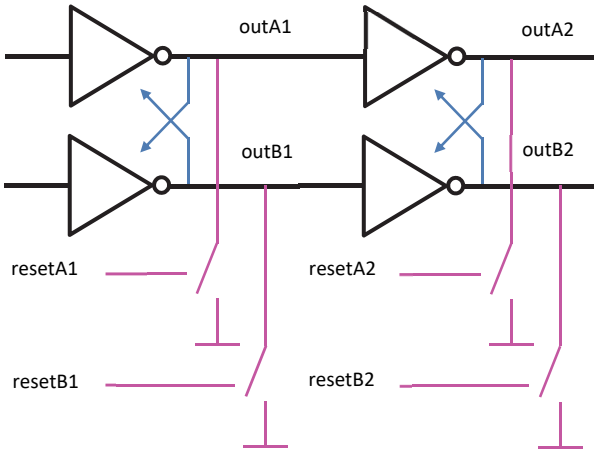


Figure 3.21: Two stages of complementary inverter with startup NMOS

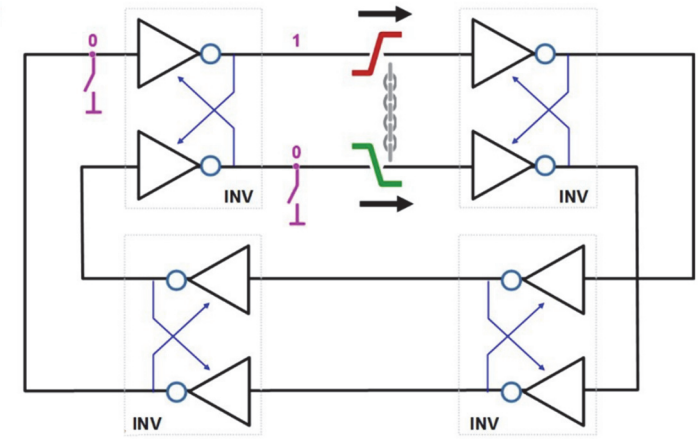


Figure 3.22: Startup design in quadrature ring oscillators

Table3.2: Output status in each reset configuration of two stages

resetA1	**0**	1	0	0	1	**0**	0	**1**	0	1	X
resetB1	**0**	0	1	0	0	**1**	0	**0**	1	1	X
resetA2	**0**	0	0	1	1	**1**	0	**0**	0	X	1
resetB2	**0**	0	0	0	0	**0**	1	**1**	1	X	1
State	**Oscillation**	reset outA1	reset outB1	reset outA2	Contradiction	**reset outB1&outA2**	reset outB2	**reset outA1&outB2**	Contradiction	Forbidden	Forbidden

Figure 3.23 shows the schematic of a four-stage quadrature ring oscillator which is composed by four complementary inverter cells (as described in Figure 3.19) with startup NMOS at each output. A reset signal is added to control resetA of one stage and resetB of the next stage; all the other reset ends are connected to Vss to keep startup NMOS “off”. The reset signal should be set first to 1 for initialization and then 0 to launch the oscillation. During the oscillation, all the NMOS for reset are “off” and all the outputs have the same charge.

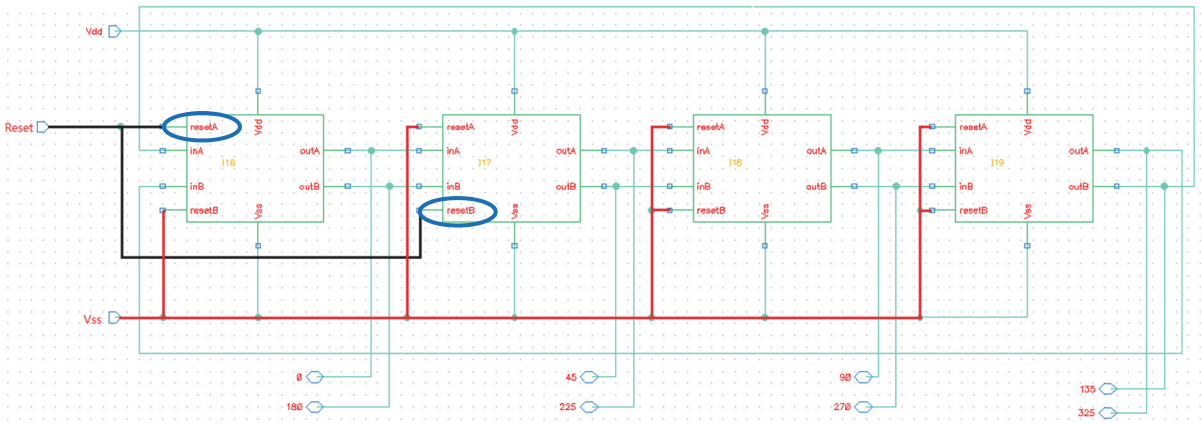


Figure 3.23: Structure of quadrature ring oscillator with startup signal

2.4. Simulation results of four-complementary RO

A four-stage ring oscillator is built with complementary inverters which could combine the outputs and produce output signals in quadrature. The size is determined as described in equation 2.8 to symmetrize both the input capacitances and output currents. In this configuration, a pair of signal transitions is produced, and it circulates respectively in opposite side. Thanks to the back-gate control structure, the two transitions are linked together robustly so that the proposed ring oscillator has a good capacity of jitter resistance.

We have realized several simulations of a four-stage complementary inverters ring oscillator to validate our concept. Figure 3.24 illustrates a short time transient simulation to verify the startup situation. First a reset signal is given and kept 5 ns to initialize the outputs, and after the reset signal is set to 0, the ring oscillator begins to oscillate thanks to the back-gate self-correction structure. The same case without back-gate control structure is also simulated, but that system cannot begin to oscillate as expected.

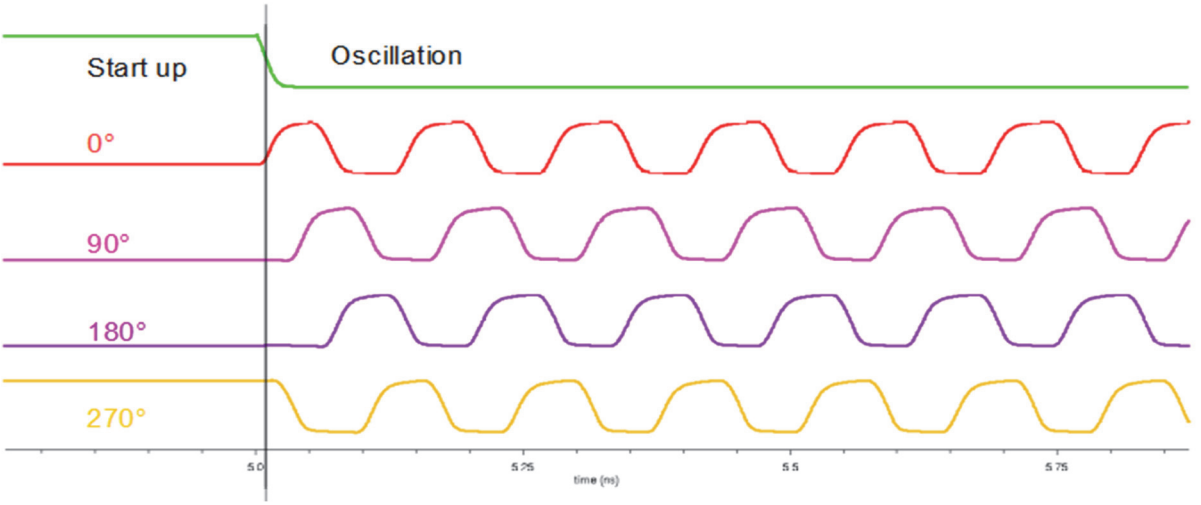


Figure 3.24: Transient simulation of the proposed ring oscillator including start up signal

Another transient simulation is shown in Figure 3.25, where the eight single ended outputs are plotted together which produces clocks equally spaced by 45°. Each pair of signals is “perfectly” symmetrical to each other and crosses at Vdd/2 (0.5V). There are no glitches caused by Miller capacitance, because of back-gate control, the output signal pair can compensate each other. Among the eight phases, four phases (0°, 90°, 180°, 270°) or (45°, 135°, 225°, 315°) can form a quadrature signals. The measured period is about T = 136 ps, which corresponds to a frequency oscillation of 7.3 GHz. The power consumption is 5mW (the rms current of the whole oscillator is 5 mA).

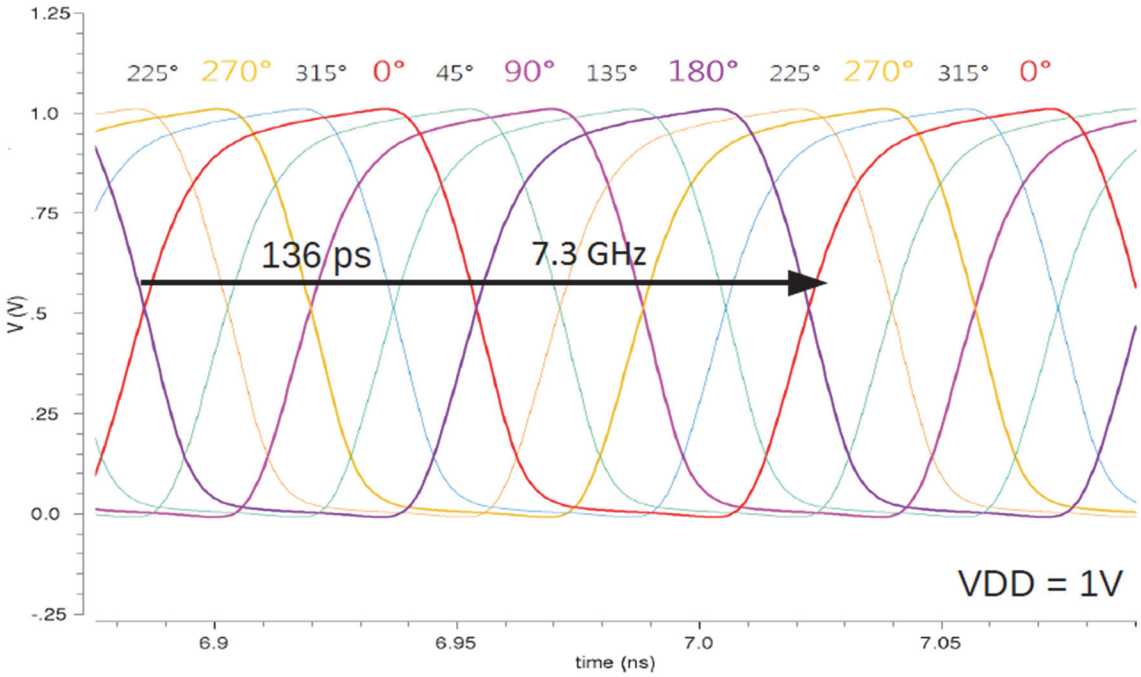


Figure 3.25: Transient simulation result of a four-complementary-inverter ring oscillator

Figures 3.26 and 3.27 illustrate the jitter using transient noisy simulations by 14000 cycles. The ring oscillator exhibits a low jitter, its RMS value is equal to 35 fs.

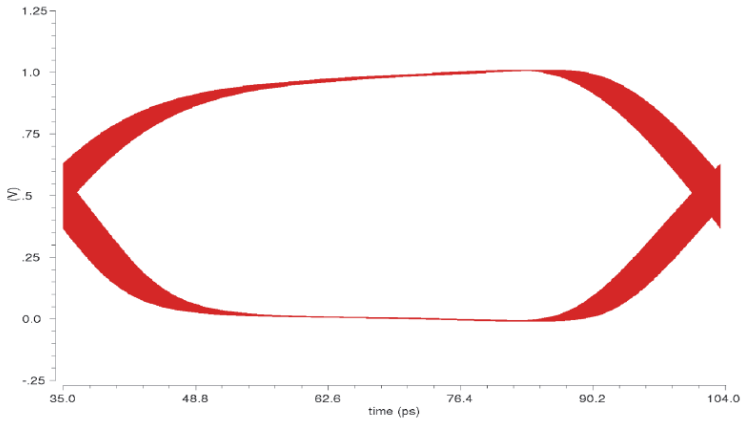


Figure 3.26: Jitter transient simulations (Eyes diagram)

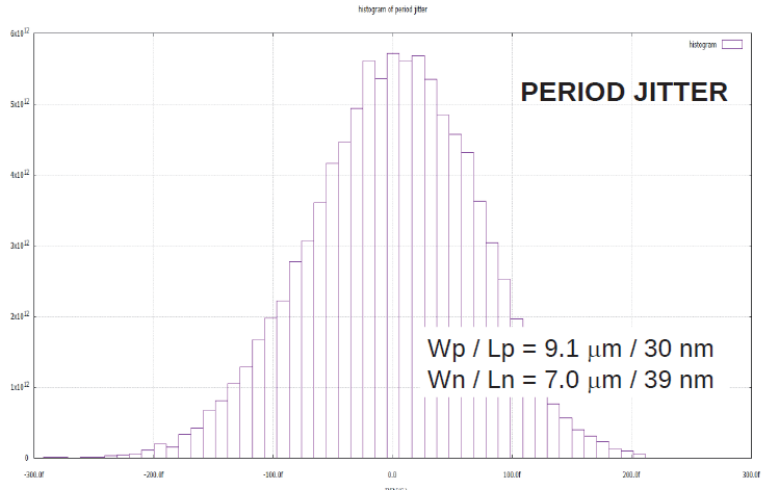


Figure 3.27: Period jitter histogram

If the flicker noise is negligible at an offset of Δf=1MHz from the carrier (f_0=7.3GHz), we can estimate the phase noise using equation 3.18 [16]. So, we obtain: PN=-93.2dBc/Hz@1MHz.

$$PN = 10\log\left(\frac{jitter^2 {f_0}^3}{\Delta f^2}\right) \quad (3.18)$$

2.5. Comparison of different Vdd

We are interested by the impact of the supply voltage Vdd on the oscillator performance. Figures 3.28 and 3.29 illustrate the relationship between oscillation frequency and Vdd (left), charging current and Vdd (right) in linear and logarithmic scales respectively.

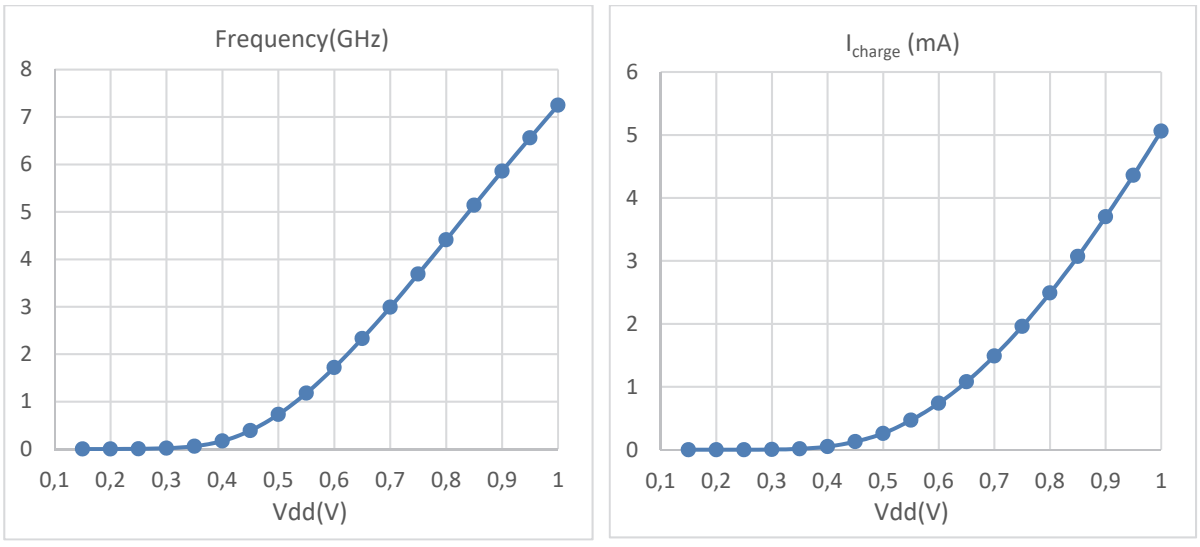


Figure 3.28: Frequency and charging current of ring oscillator in function of Vdd in linear scale

It can be noted that as Vdd decreases from 1V, the oscillation frequency and charging current decrease approximately linearly. When the voltage is less than 0.6V, the oscillation frequency and current decrease slowly, but the oscillation doesn't stop, the minimum oscillation voltage is 0.15V,

where the oscillation frequency is 600 kHz. This back-gate controlled quadrature ring oscillator can work in the moderate inversion region or even the weak inversion region of transistors.

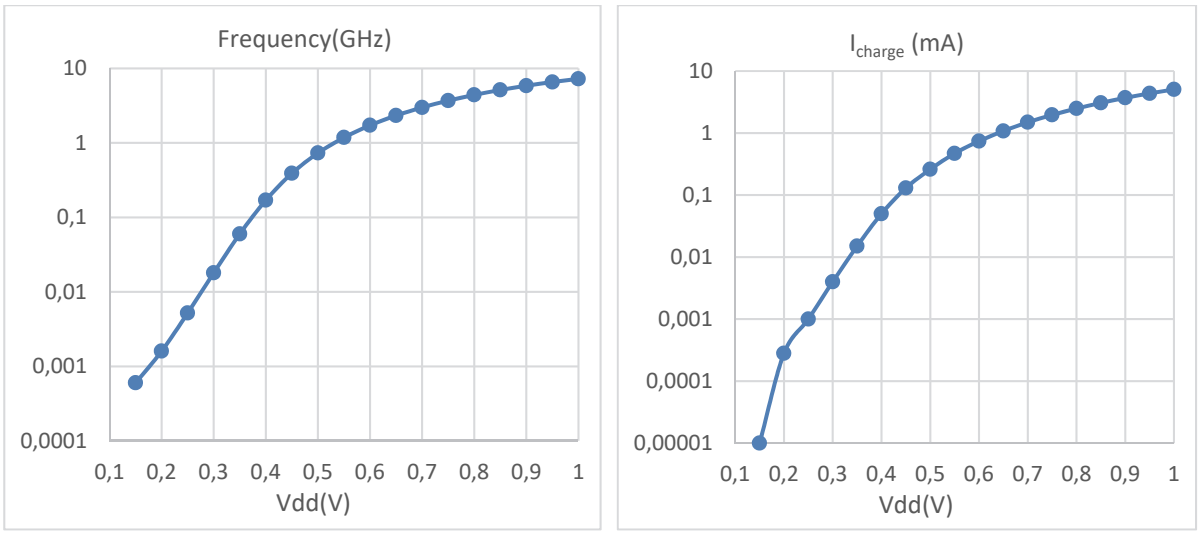


Figure 3.29: Frequency and charging current of ring oscillator in function of Vdd in logarithmic scale

If we consider the delay of the inverter as a process of charging the equivalent capacitor, we have

$$I_{charge} * T_d = C_{tot} * Vdd \tag{3.19}$$

Together with equation 3.17, the oscillation frequency is therefore given by

$$f_o = \frac{1}{2NT_d} = \frac{1}{2NC_{tot}} * \frac{I_{charge}}{Vdd} \tag{3.20}$$

where I_{charge} is the rms charging current, C_{tot} is the total parasitic capacitance of the output node of the delay unit, and Vdd is the supply voltage. We observed that the oscillation frequency f_o is proportional to the ratio I_{charge}/Vdd which is validated by Figure 3.30.

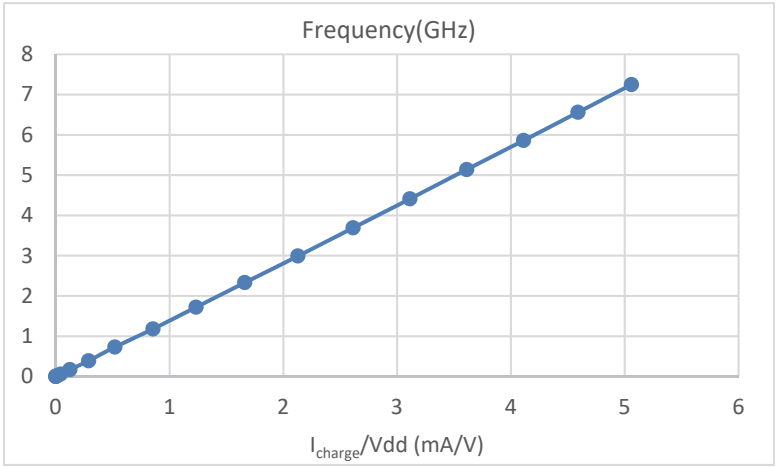


Figure 3.30: Frequency in function of I_{charge}/Vdd

Typically, the dissipation power of a CMOS inverter is calculated using equation 3.21 [17], this value can be multiplied by the number of gates 2N to obtain the power consumption of ring oscillator in equation 3.22.

$$\mathrm{P} = C_{tot} * Vdd^2 * f \tag{3.21}$$

$$\mathrm{P}_{ro} = 2\mathrm{N} * C_{tot} * Vdd^2 * f_o \tag{3.22}$$

Together with equation 3.20, we can deduce the power consumption in another form:

$$\mathrm{P}_{ro} = I_{charge} * Vdd \tag{3.23}$$

So, the total power consumption of ring oscillator can be calculated by multiplying the RMS charging current by the supply voltage. Power consumption in function of Vdd is plotted in Figure 3.31. The simulation result shows that voltage supply has a positive correlation with power consumption.

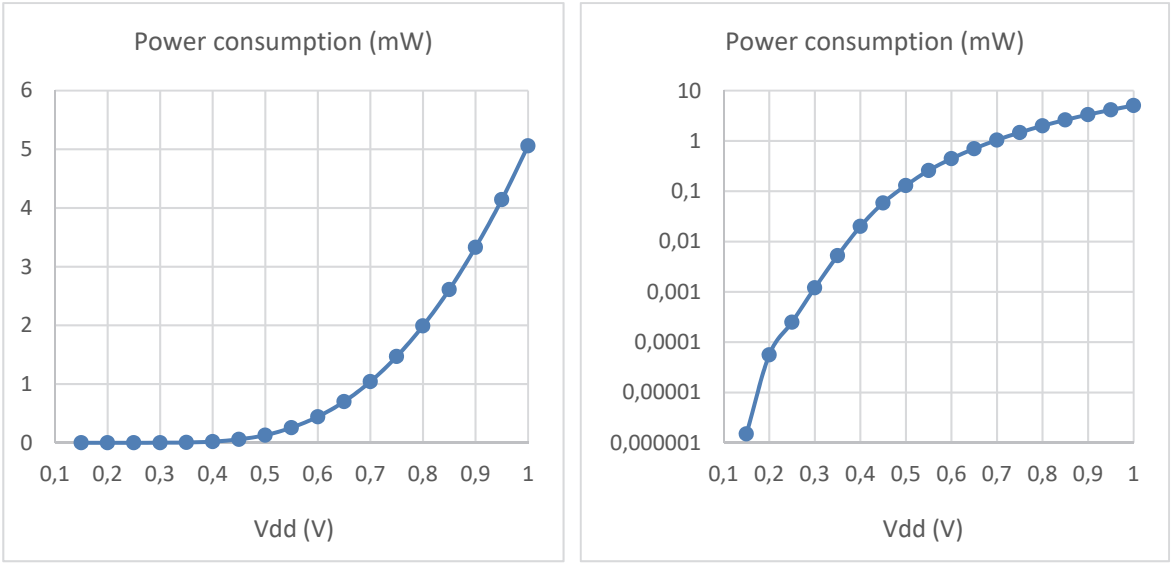


Figure 3.31: Power consumption in function of Vdd in linear and logarithmic scales

In fact, the supply voltage is very important to determine the performances of ring oscillator. To decrease the power consumption, the supply voltage should be lowered also. Of course, lowering the voltage will decrease the oscillation frequency.

According to Figure 3.28 and 3.31, we plotted the power consumption in function of the oscillation frequency in Figure 3.32 which illustrated that oscillation frequency has a positive correlation with power consumption. We need to find a compromise between the power consumption and the frequency, by choosing the right supply voltage. This ring oscillator can achieve great power savings with a suitable oscillation frequency.

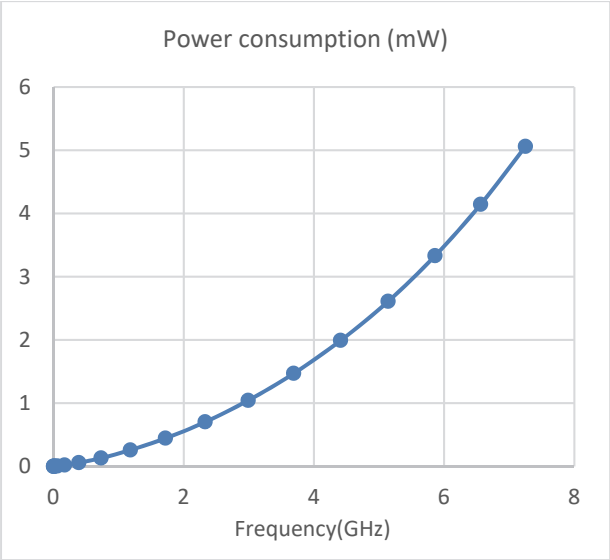


Figure 3.32: Power consumption in function oscillation frequency

2.6. Comparison of different sizes

For all previous simulations, we kept the same transistors size given by rel. 2.8 in chapter 2, where Wp=9.1 µm, Lp=30 nm, Wn=7.0 µm and Ln=39 nm, to symmetrize both the input capacitances and output currents. Next, we evaluate the impact of the size on the oscillator performance with power supply fixed at 1 V. There are two types of size evaluation: Variation of W with L fixed and variation of the size with the ratio W/L fixed.

First, let's discuss the first case. With Lp=30nm and Ln=39nm are fixed, taking Wp=9.1um and Wn=7um as benchmark, W is reduced proportionally and normalized as shown in Table 3.3.

Table3.3: Size configuration for RO with L fixed

Normalization	0,1	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9	1
Wp(um)	0,91	1,82	2,73	3,64	4,55	5,46	6,37	7,28	8,19	9,1
Wn(um)	0,7	1,4	2,1	2,8	3,5	4,2	4,9	5,6	6,3	7

Figure 3.33 illustrates oscillation frequency in function of normalization value (left) and consumption in function of normalization value (right) respectively. It can be noted that as W decreases, the oscillation frequency is almost constant from the beginning, and then decreases from slow to fast. The power consumption on the other hand, is proportionally reduced as W decreases.

We can observe from equation 3.20 that, as power supply fixed, the oscillation frequency is proportional to I_{ds}/C_{tot} (cf. equation 3.24):

$$f_o \propto \frac{I_{ds}}{C_{tot}} \tag{3.24}$$

where I_{ds} is proportional to W with L fixed, and C_{tot} is the total equivalent capacitance of the output node of each delay unit. This total value is including the parasitic capacitance C_{par}, the back-gate capacitance C_{bg} and load capacitance C_{load} where C_{par} and C_{load} are proportional to W.

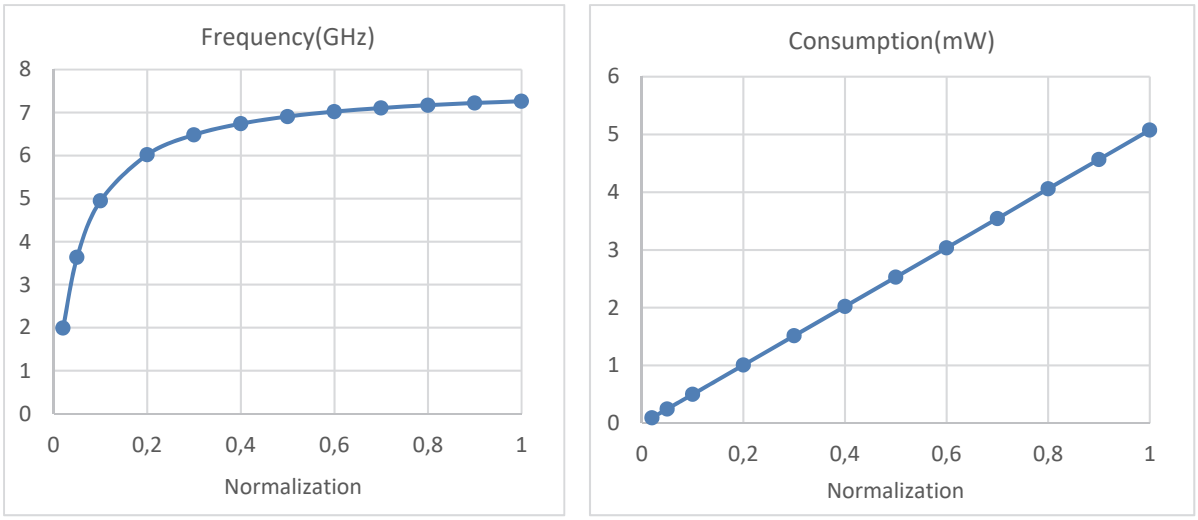


Figure 3.33: Frequency in function of W and power consumption in function of W with L fixed

The frequency will remain the same without C_{bg}. However if C_{bg} is considered, the frequency will change.

$$C_{tot} = C_{par} + C_{bg} + C_{load} \tag{3.25}$$

Figure 3.34 illustrates the diagram to calculate C_{bg} with W and 2W for example, where Δ is the edge length of the whole layout footprint of transistors.

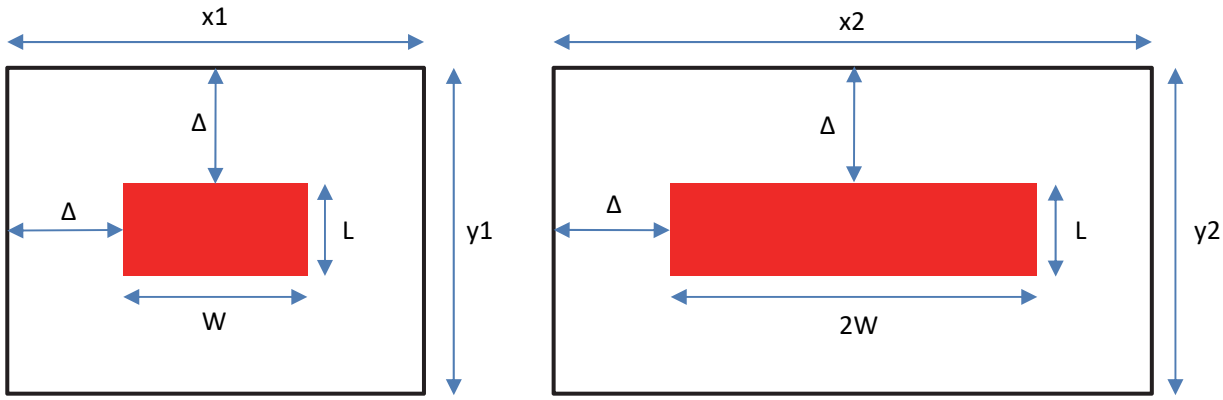


Figure 3.34: Diagram to calculate C_{bg} with W and 2W

Thanks to the geometry depicted in figure 3.34, we can deduce:

$$C_{bg1} \propto (W + 2\Delta) * (L + 2\Delta) \tag{3.26}$$

$$C_{bg2} \propto (2W + 2\Delta) * (L + 2\Delta) \tag{3.27}$$

Finally, we obtain:

$$2C_{bg1} > C_{bg2} \tag{3.28}$$

$$2C_{tot1} > C_{tot2} \tag{3.29}$$

The smaller the W, the larger the proportion of Δ in the total capacitance, so the frequency will be slower as shown in Figure 3.33 (left).

I_{ds} is proportionally with W with L fixed, together with power supply voltage is fixed also, we have:

$$P_{ro} \propto W \tag{3.30}$$

So, the power consumption is proportionally reduced as W decreases as shown in Figure 3.33 (right). Then, to reduce device area and cost savings, the other case of varying size with the ratio W/L fixed should be considered which we called "fixed-voltage scaling model" [18], [19].

With the ratio W/L fixed and taking Wp=9.1um, Lp=30nm, Wn=7um, Ln=39nm as benchmark, the sizes of transistors of both PMOS and NMOS are reduced proportionally and normalized as shown in Table 3.4.

Table3.4: Size configuration for RO with the ratio W/L fixed

Normalization	0,1	0,2	0,3	0,4	0,5	0,6	0,7	0,8	0,9	1
PMOS(um/nm)	0,91/30	1,82/60	2,73/90	3,64/120	4,55/150	5,46/180	6,37/210	7,28/240	8,19/270	9,1/300
NMOS(um/nm)	0,7/39	1,4/78	2,1/117	2,8/156	3,5/195	4,2/234	4,9/273	5,6/312	6,3/351	7/390

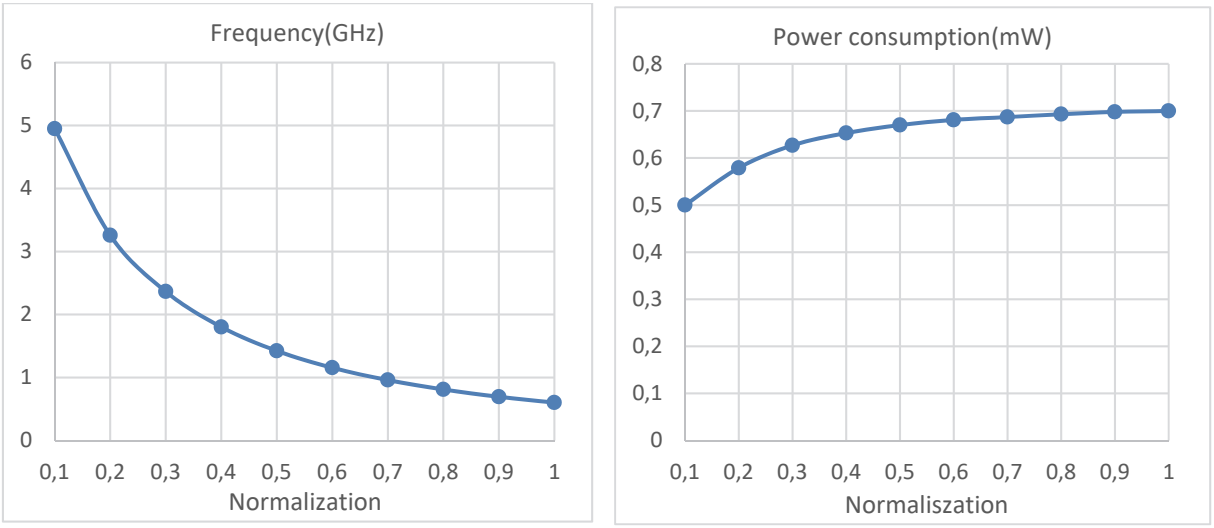


Figure 3.35: Frequency in function of size and power consumption in function of size

Figure 3.35 illustrates oscillation frequency in function of normalization value (left) and consumption in function of normalization value (right) respectively. It can be noted that as size

decreases, the oscillation frequency increases from slow to fast but power consumption is almost constant from the beginning to a slight decrease.

This trend can still be obtained from theory. The scaling relationship is quite different between long channel devices and short channel devices [20]. Since the transistor we used is nanometer level, short-channel effects should be considered. The charging current is constant when keep the ratio W/L constant in long channel devices, but for velocity saturated devices, the current depends on the value of channel length:

$$I_{ds} = \frac{1}{2}\mu_0 C_{ox}\frac{W}{\mathrm{L}}\frac{(V_{GS}-V_{TH})^2}{1+(\frac{\mu_0}{2v_{sat}L}+\theta)(V_{GS}-V_{TH})} \quad (3.31)$$

From the equation 3.31 [9], we can see that in the case of a fixed ratio of W/L, the current is also related to the length itself. When the size scaling is reduced, the current is reduced also, but less than proportionally reduced, and together with constant power supply. The power consumption is also slightly reduced. On the other hand, as the size decreases, the total capacitance decreases, so the oscillation frequency increases as shown in Figure 3.35.

2.7. Comparison between classic ring oscillator and complementary ring oscillator

In this part, our goal is to compare the performance characteristics of the classic ring oscillator and the proposed complementary ring oscillator. We can compare from the power consumption and time jitter and assure all the configuration conditions such as the transistor sizing, simulation precision are the same.

We have already designed and simulated a four-stage ring oscillator built with complementary inverters which could combine the outputs and produce output signals in quadrature in chapter 3.2.3. Then we designed a classic ring oscillator built with normal inverter where the back-gate of PMOS is connected to Vdd and the back-gate of NMOS is connected to Vss. It is important to note that single-ended ring oscillator with an even number of inverters cannot oscillate because it has a fixed state. So, we introduce a VCVS (Voltage Controlled Voltage Source) with a '-1' gain to force the state to change (cf. Figure 3.36). In this case each output doesn't be controlled by the back-gate, this system can't get differential signal pairs, although it also output eight phases, these signals are not equally spaced by 45°, so the required quadrature signal cannot be output (cf. Figure 3.37).

Also, the oscillation frequency is more rapid which is 13GHz without back-gate control structure; we add a small charge capacitor in every output to force the oscillation slow down.

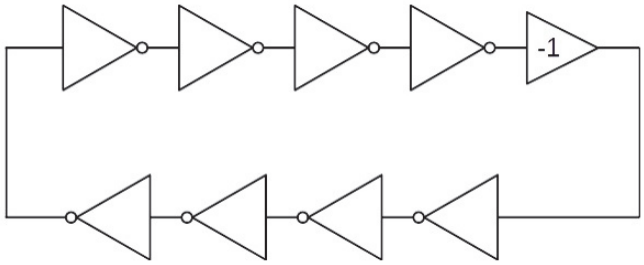


Figure 3.36: Ring oscillator composed by 8 inverters and a VCVS

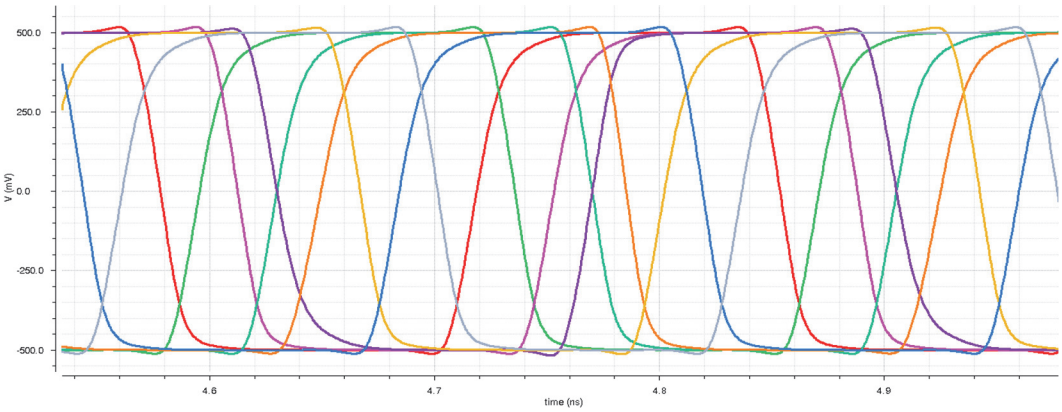


Figure 3.37: Transient simulation for a classic ring oscillator composed by 8 inverters and a VCVS

The graph characteristic of oscillation frequency in term of the value of the charge capacitor is shown in Figure 3.38, as we predicted, bigger the capacitor is, slower the ring oscillator oscillate. The half frequency of complementary ring oscillator (3.63GHz) is observed when the charge capacitor is 57.5fF. We are interested in this frequency because it has the same transition status between classic ring oscillators and complementary ring oscillators.

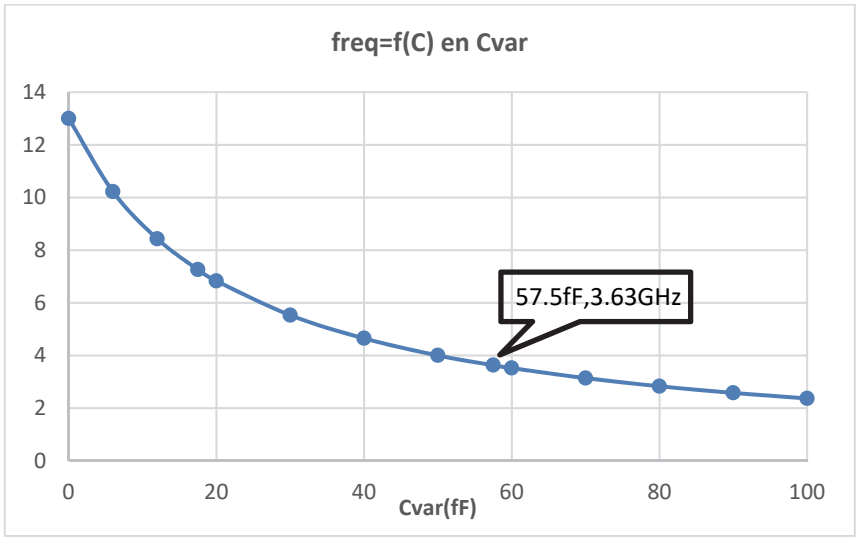


Figure 3.38: Oscillation frequency in function of charge capacitor for classic ring oscillator

Then we compare the timing jitter in sixty periods with a small maxstep, the simulation results (cf. Table 3.5) are as expected: the proposed complementary ring oscillator has a lower period jitter of about 35 fs compared to the classic ring oscillator 70 fs because the complementary ring oscillator take profit of the back-gate control structure and it could calibrate and reduce the error in each transition.

Table3.5: Period jitter comparisons between complementary RO and classic RO

	Frequency	60 periods, maxstep 0.01ps			
Complementary Ring Oscillator	7.26 GHz	Phase 0	Phase 90	Phase180	Phase270
		35.3 fs	34.4 fs	39.5 fs	35.9 fs
Classic Ring Oscillator	3.63 GHz	60 periods, maxstep 0.02ps			
		Phase 1	Phase2	Phase 6	Phase7
		69 fs	68 fs	72 fs	70 fs

To study the physical limit of the proposed complementary oscillator for the low power utilization, we reduce the supply voltage as low as possible until the oscillator doesn't work anymore. We can find a minimum supply voltage of 0.15 V with an oscillation frequency of 600 kHz. We did the same thing to the classic ring oscillator and we found the minimum supply voltage is 0.16 V with an oscillation frequency of 250 kHz but distortion of the waveform is obvious.

3. Conclusion

In this chapter, first we have studied the theory of oscillation and introduced two main structures of oscillators: LC oscillators and ring oscillators. In general, LC oscillators have higher accuracy and higher quality factor Q, but the area is large, and cost is high also. Ring oscillators on the other hand, have simpler structure, smaller area and lower cost; however it has a poor jitter (i.e. phase noise) performance compared to LC oscillators. To meet the low cost of production targets, the small area occupied by a ring oscillator seems more adequate, plus, we need quadrature signals in RF receiver architectures describe the processing that takes place in modern digital communications systems. So, we proposed a quadrature ring oscillator using an even number of complementary inverters in UTBB-FDSOI technology.

Then, we studied the startup analysis and configured the settings of startup. A four-stage ring oscillator is built with complementary inverters and simulated; some results are already published [21]. In this configuration, a pair of signal transitions is produced, and it circulates respectively in

opposite side. The symmetry of the slopes of the signals shows the effectiveness of the back-gate feedback in FDSOI technology. This structure makes it easy to perform a quadrature signals: four identical outputs (same amplitude and same frequency) but with different phases (0°, 90°, 180° and 270°). The simulated period is about T=136ps, which corresponds to a frequency oscillation of 7.3GHz. This ring oscillator exhibits a dynamic power consumption of 5mA. This high value (1.27mA per complementary inverter), for a ring oscillator, is due to the size (W) of the transistors. We have not optimized this value in term of power consumption at first, but to decrease the phase noise.

Next, we made several comparisons to evaluate the performance of frequency, power consumption as well as jitter analysis for this quadrature ring oscillator structure, the simulation results shows that the proposed quadrature ring oscillator has better performances, simpler structure and is suitable for low power design.

The proposed quadrature ring oscillator is ideal to build the components of a quadrature clock generator as well as quadrature VCOs. We are now designing VRCO taking advantage of this ring oscillator to build a competitive low noise high speed PLL in FDSOI 28nm technology which will be present in the next chapter.

4. Bibliography

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Chapter IV – PLL building blocks

1. Introduction

In this chapter, we will present all the building blocks for Digital Phase-Locked Loop (DPLL), including VCO, PFD, charge pump and frequency divider. All blocks are designed using the complementary logic concept and 28nm UTBB-FDSOI technology for transistor implementation. Each block will elaborate on the basic functions using both conventional and optimized structures and SPICE simulations. At the end, we will introduce a second-order loop filter and make a synthesis simulation to show the result for the behavioral level of the final DPLL.

2. Voltage controlled ring oscillator design

2.1. Introduction of VCO

In the last chapter, we presented an efficient quadrature ring oscillator composed by complementary inverters. In most cases, the frequency of oscillators must be adjustable. If the output frequency of an oscillator can be controlled by an input voltage, this type of oscillator is called a Voltage controlled oscillator (VCO) as shown in Figure 4.1.

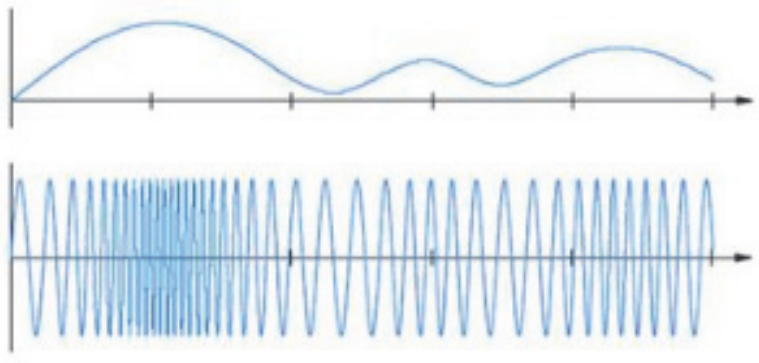


Figure 4.1: Definition of general VCO

The output frequency of an ideal VCO is a linear function of the input voltage as shown in Figure 4.2a. The relation between output frequency and controlled voltage can be written by:

$$\omega_{out} = \omega_0 + K_{VCO}V_{ctrl} \tag{4.1}$$

where ω_0 is the intercept value of angular frequency when V_{ctrl}=0, and the slope K_{VCO} represents the sensibility of VCO in rd/s/V (or often in Hz/V).

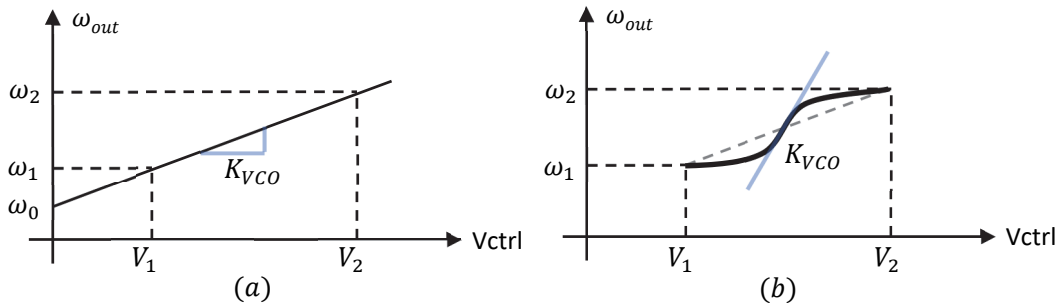


Figure 4.2: Characteristics of ideal VCO (a) and non-linear VCO (b)

VCOs have different performance requirements for different application environments. The commonly required performance parameters are as follows [1]:

- **Center frequency and tuning range**: The output signal frequency range of the VCO. In this range, the variation of the output amplitude and jitter must be minimal. The tuning range is typically at least ±20% ω_0 [2].
- **Jitter and phase noise**: This is discussed in detail in chapter 1.
- **Tuning linearity**: Due to structural limitations, the output frequency and tuning voltage of actual VCOs usually exhibit a nonlinear characteristic where K_{VCO} is not constant during the whole tuning range. The typical characteristic of VCO exhibits a high gain in the middle of tuning range and a low gain at the two sides (cf. Figure 4.2b).
- **Output amplitude**: Large output amplitude makes the waveform less sensitive to noise and compatible with the next stage. The increase in amplitude can be obtained by sacrificing power consumption, adjusting the tuning range, adding a level shifter, etc.
- **Power dissipation**: The oscillator is limited by the tradeoff between speed, power consumption, and noise like the other circuits. The typical power consumption of oscillators is around 1 to 10mW [3].

As shown in equation 3.20, the oscillation frequency of a structure-determined RO depends on charging current I_{charge} and supply voltage Vdd. Figure 4.3 illustrates the two models to use the bias current and voltage to control RO. In practice, the bias current and supply voltage always affect each other at the same time; current mirror is an appropriate structure to provide bias current.

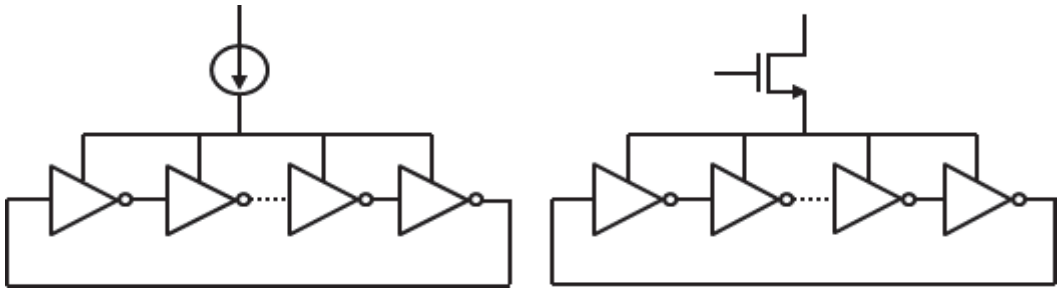


Figure 4.3: Bias current control and bias voltage control for frequency variation

Some typical VCO structures have been presented in chapter 1. In this section, a quadrature VCO (QVCO) composed by a current mirror and a quadrature RO will be introduced.

2.2. Current mirror with back-gate control

We will use a current mirror as part of the control of our VCO to provide bias currents and active loads to circuits. A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading [4]. Figure 4.4 shows a basic current mirror.

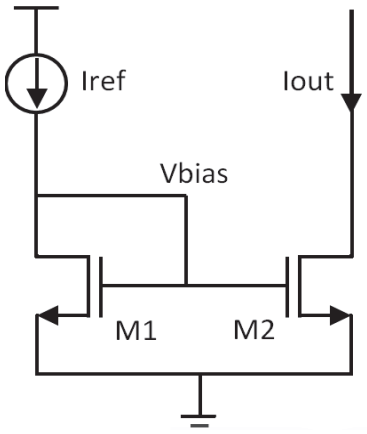


Figure 4.4: Basic current mirror

Neglecting channel length modulation, the two currents, I_{ref} and I_{out}, are given by Equations (4.2) and (4.3).

$$I_{ref} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_{gs} - V_{thn})^2 \tag{4.2}$$

$$I_{out} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 (V_{gs} - V_{thn})^2 \tag{4.3}$$

As they have the same V_{gs}, we have:

$$\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2}{(W/L)_1} \tag{4.4}$$

From equation (4.4), we can see that the current copy is independent of process and temperature, only depends on the ratio of transistor sizes. So, the output current I_{out} is directly related to the input current I_{ref}, and I_{out}=I_{ref} if both transistors are identical in theory.

But this ideal situation does not exist due to the channel length modulation [5], where λ is the channel length modulation coefficient which depends on length size. This effect results in significant error in copying current, especially if we reduce the length of the transistors. For the basic current mirror in Figure 4.4, we can rewrite relations (4.2) and (4.3):

$$I_{ref} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_{gs} - V_{thn})^2 (1 + \lambda V_{ds1}) \tag{4.5}$$

$$I_{out} = \frac{1}{2}\mu_n C_{OX}(\frac{W}{L})_2(V_{gs} - V_{thn})^2(1 + \lambda V_{ds2}) \quad (4.6)$$

So the ratio of the currents becomes:

$$\frac{I_{out}}{I_{ref}} = \frac{(W/L)_2(1+\lambda V_{ds2})}{(W/L)_1(1+\lambda V_{ds1})} \quad (4.7)$$

We can see that the current copy depends not only on the ratio of transistor sizes, but also on V_{ds1} and V_{ds2} which are not necessarily always equal. Current mismatch is more severe in short channel conditions where λ is relatively large.

Many structures of current mirrors exist to suppress short channel effect, for example, cascode current mirror [6], Wilson current mirror [7] as shown in Figure 4.5 and other active-input regulated-cascode current mirrors [8]. The commonality of all these current mirrors is ensuring that V_{ds} of two main transistors is equal (V_X=V_Y) to guarantee the channel modulation effect is the same. However, cascoded variants of the basic current mirror are not a realistic option when the voltage of the power supply is 1V or below 1V because these structures reduce voltage margin or increase power consumption.

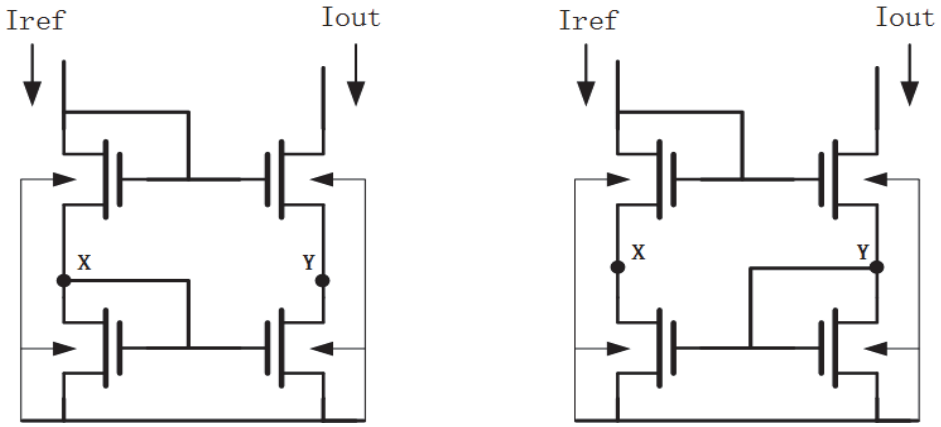


Figure 4.5: Structure of cascode current mirror and improved Wilson current mirror

We propose another solution of biasing dynamically the back-gate of UTBB-FDSOI transistors in order to compensate the short channel effect even if V_{ds} of two main transistors are not equal. Take the basic current mirror in Figure 4.4 again for example, and configure back-gates of UTBB-FDSOI transistors as shown in Figure 4.6.

Figure 4.6(a) is the basic current mirror with two back-gates connected to Vss as usual. The two transistors have the same value of biasing voltage and threshold voltage. In this case, the copy current follows equation 4.7 and channel modulation effect causes mismatch.

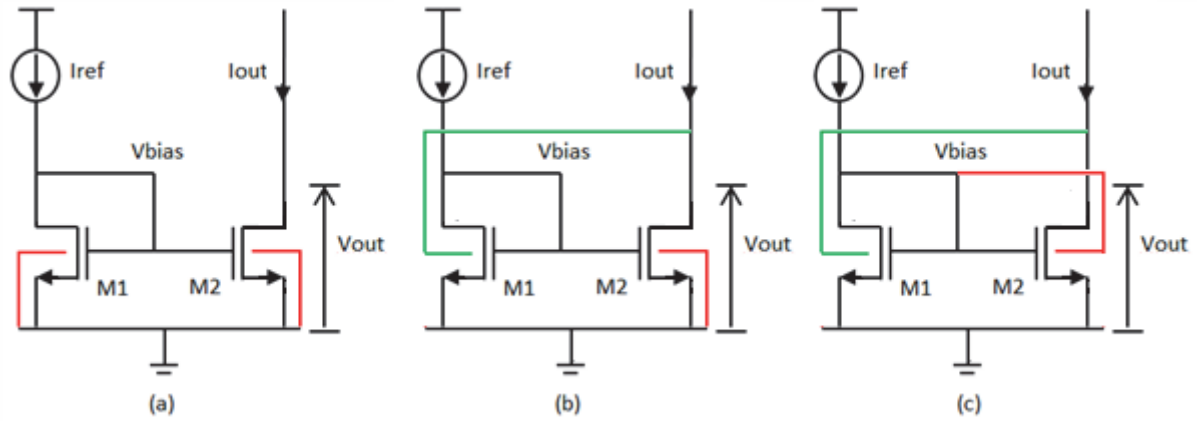


Figure 4.6: Basic current mirrors with different back-gate configurations

Our idea is to reduce the slope of Ids in the saturation region by controlling back-gate voltages. So, we propose the two following current mirrors. Figure 4.6(b) uses back-gate of M1 to connect Vout. In this configuration, the back-gate voltage of M1 follows the drain voltage of M2 which ranges from 0 to 1 V, the threshold voltage decreases due to increase of the back-gate voltage; so to achieve the same source current, the biasing voltage(V_{gs}) decreases (cf. equation (4.5)). Therefore, we have the possibility to control the slope of the output current which becomes horizontal or negative depending on the lengths of the transistors.

Moreover, we can use the drain voltage of M1 to control the back-gate of M2 as described in Figure 4.6(c). In this case, back-gate of transistor M2 is connected to the drain voltage of M1 instead of ground to have a smaller threshold voltage for M2 which can increase the output current (cf. equation (4.6)).

It should be noted that in our environment the supply voltage Vdd is 1V. With such a small voltage, the transistors operate maybe in moderate inversion and even weak inversion. The proposed idea applies in all inversion modes. In the following simulations, we have chosen to operate in moderate region, by setting a small reference current (1uA for example).

Figure 4.7 illustrates the simulation results of I_{out} in function of V_{out}(=V_{ds}) for basic current mirror with different back-gate configurations. Here to reflect the short channel effect, we have chosen a quite small size of transistors (W_N/L_N=80nm/33nm).

As expected, the output current, I_{out}, and the output voltage V_{ds} present an exponential relationship in moderate region (red curve). So the mismatch between reference current and output current is quite serious in basic current mirror without back-gate control.

We use the drain voltage of M2 to control the back-gate of M1, with an appropriated size; short channel effect could be compensated by decreasing V_{bias} (blue curve). More, when both back-

gates of the two transistors are connected to the drain voltages, output current can still increase to the reference current 1 µA (green curve).

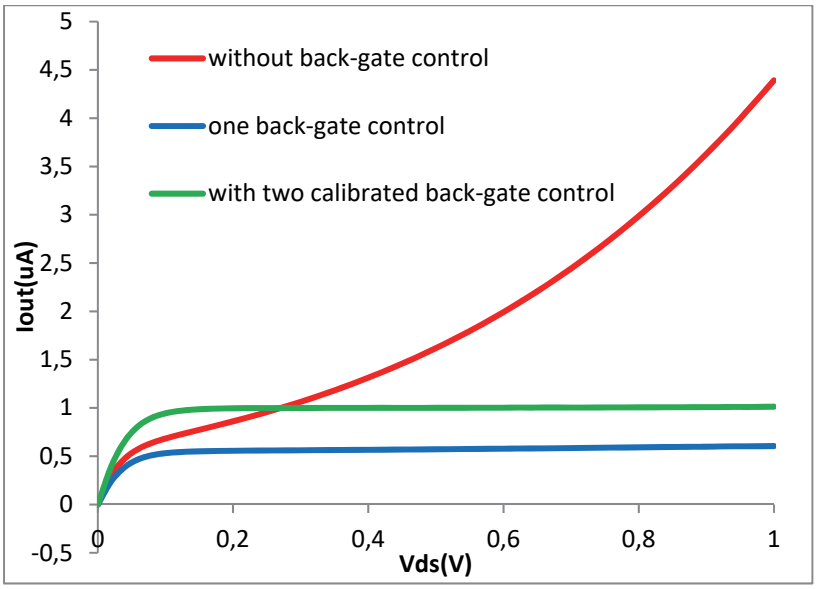


Figure 4.7: I_{out} comparison with different back-gate configurations

We can see from Figure 4.8 that V_{bias} decreases as V_{ds} increases because of the back-gate's control. As a result, channel modulation effect is well compensated and output current stays at about 1µA.

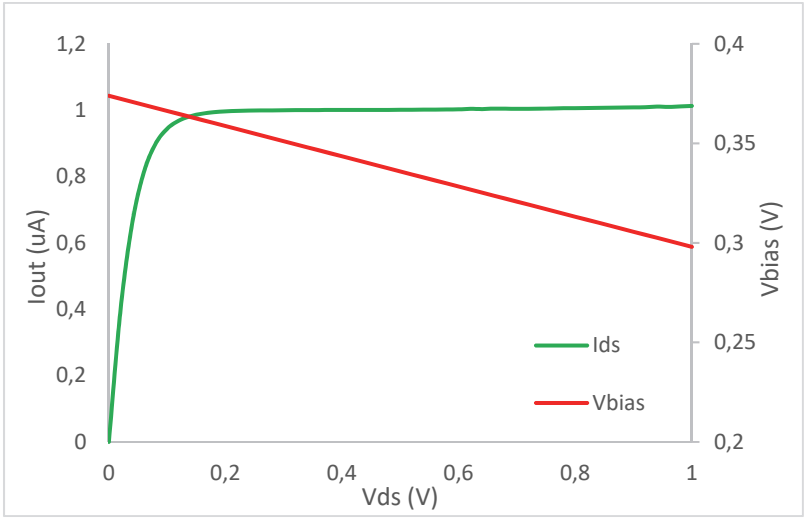


Figure 4.8: I_{out} and V_{bias} in terms of V_{ds} with back-gate control in small size (80nm/33nm)

In all above simulations, the sizes of two NMOS is 80nm for the width and 33nm for the length, this is the appropriate size to make the reference current and output current as equal as possible. In another word, by changing the lengths of the transistors, we change g_{ds} and g_{mb} of the transistors. With 80nm fixed for width, 33nm is the appropriate length where g_{mb} compensates g_{ds}.

If we increase the lengths of the transistors, the feedback could be overcompensated. For example, increasing the length by 10 (330nm) and keeping the same W/L ratio with a width of 800nm, we obtain the result shown in Figure 4.9 where a strong negative output resistance is built.

With such a large length (L=330nm), the channel modulation effect is weakened, so the slope of current in the saturation region is almost flat without back-gate control, and if we use drain voltage to control the back-gate, the output current decreases because of the change of V_{bias}.

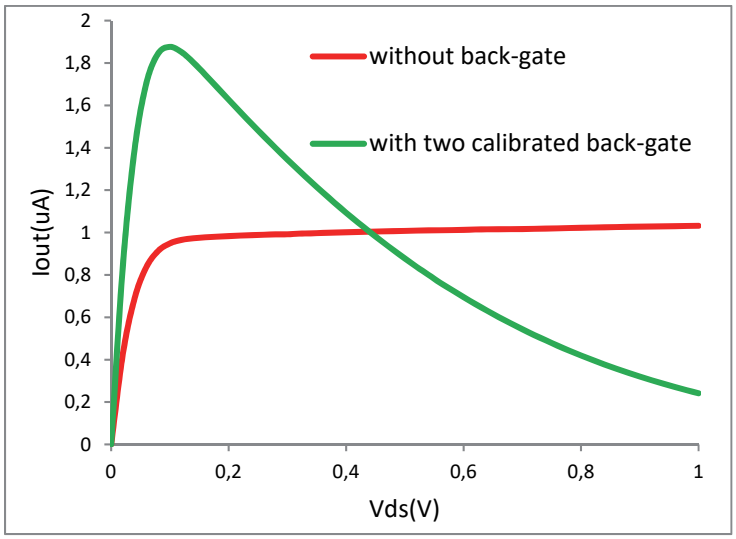
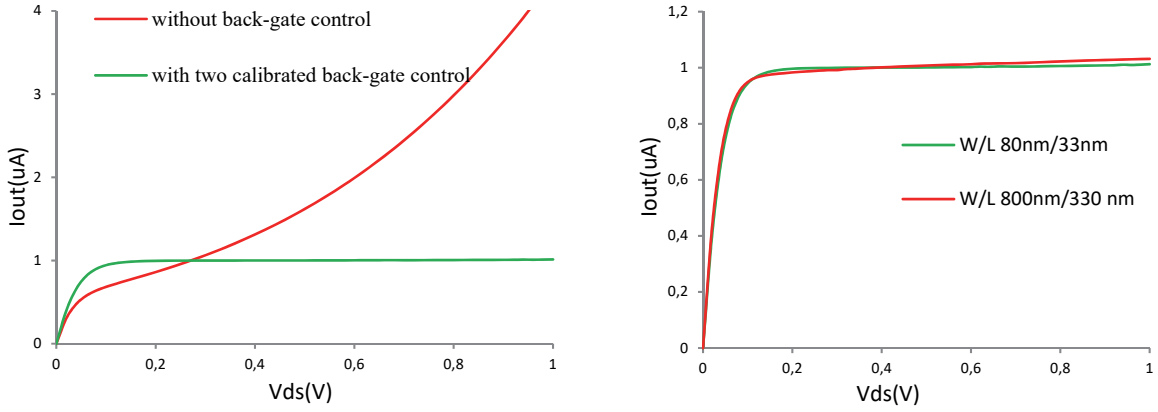


Figure 4.9: I_{out} comparison with and without back-gate control in large size (800nm/300nm)

For a better understanding, another comparison is simulated in Figure 4.10. Figure 4.10(a) illustrates in small sizes, channel modulation effect could be compensated by choosing appropriate size. Figure 4.10(b) illustrates that current mirrors using back-gate controls and appropriate small sizes obtain performances comparable to a basic configuration using large sizes.



(a) small size with and without back-gate control (b) with small and large size

Figure 4.10: I_{out} comparison in different cases

In fact, channel modulation effect is very weak but still exists in large size. So the slope of current in saturation region increases weakly, but if we adjust an appropriate size to the current mirror in small size with back-gate control, the slope of current could be close to zero although the length of the transistor is quasi-minimal. However, the output current is very sensitive to the channel length with back-gate control.

2.3. Structure of the VCRO

Now, we have a small-size good performances current mirror to bias ring oscillator for frequency variation (cf. Figure 4.3), a simple source amplifier is used to provide reference current.

Figure 4.11 illustrates the proposed VCRO composed by the four-stage quadrature ring oscillator and current mirror with back-gate control structure. The input current is converted from input voltage by NMOS transistor and is transformed by current mirror which controls the ring oscillator.

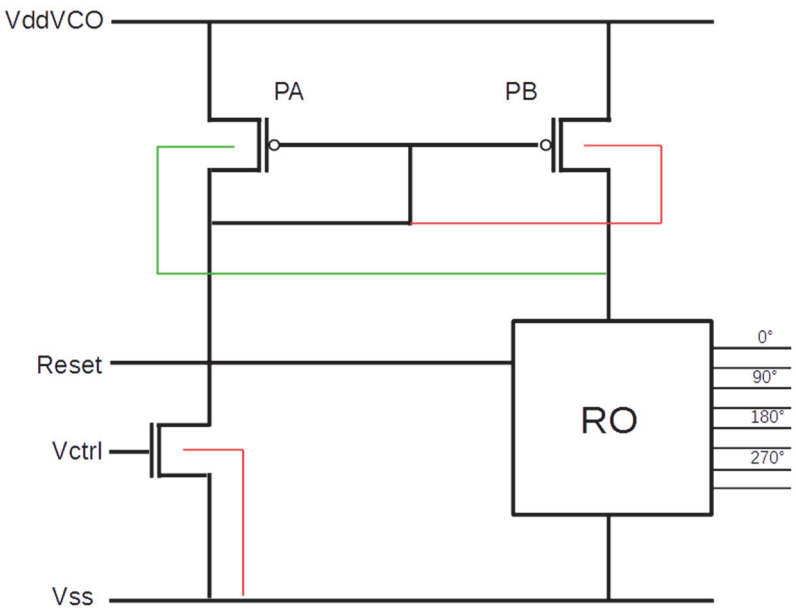


Figure 4.11: Structure of the proposed VCRO

In fact, the ring oscillator, we used, has a large size to reduce noise. So we need to drive with a relatively large transistor for the current mirror (W_P/L_P=100um/30nm in our case). What's more, as the bias current varies, the bias voltage for RO also changes at the same time. Their relationship was described in section 2.4 (chapter 3). As a result, the amplitude of output signals will also change.

2.4. Level shifter

We have noted that the output of the VCRO has a fixed low voltage level Vss, and a varied high voltage level which decreases as the input control voltage decreases. In most applications, the output

of VCO is expected to be equal to the supply voltage Vdd or stabilized at a desired level to be compatible with other modules. A voltage level shifter can help achieve this function.

Generally, a pull-up resistor can be used between output and Vdd, on the other hand, a pull-down resistor can be used between output and ground. This function works well but it causes DC current problem which will greatly increase power consumption.

DC current problem can be solved if we can replace the load resistor with a transistor which can be turned on or off as needed. A more popular voltage level shifter with cross-coupled PMOS loads is shown in Figure 4.12 [9].

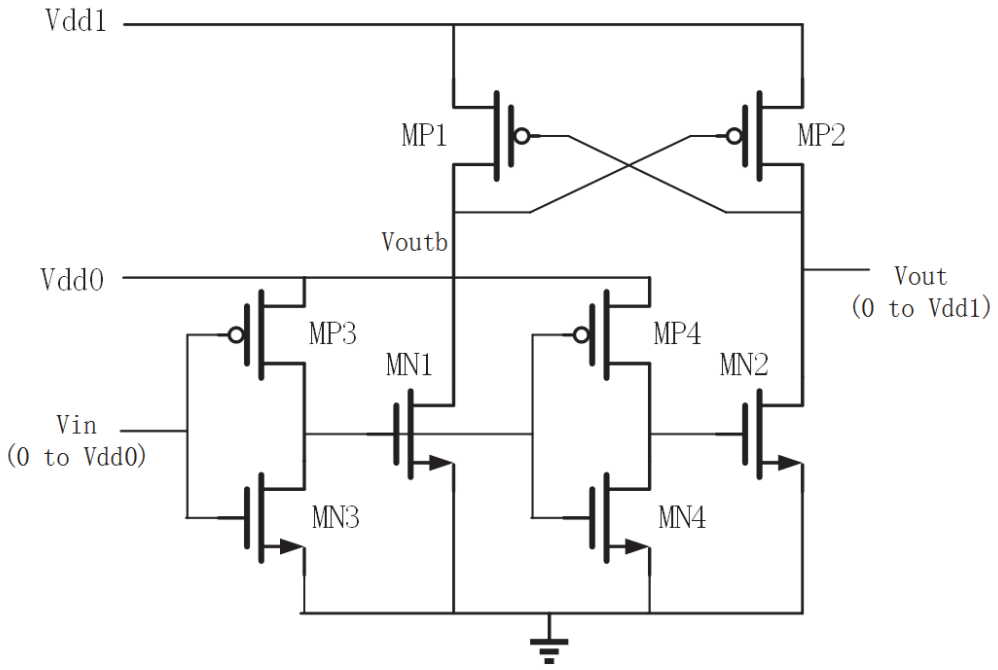


Figure 4.12: Pull-up level shifter with low quiescent current

When the input signal Vin is in a logic low level (ground), MN1 turns on and MN2 is off which pulls the point Voutb to ground. This transition of Voutb turns on MP2 which pulls up the Vout node to the Vdd1 voltage level which turns off MP1. On the contrary, when Vin is in Vdd0 level, MN1 is off and MN2 is on, which turns on MP1. MP1 pulls up Voutb to the Vdd1 level which turns off MP2, so Vout stays at ground.

This structure ensures that there is never a steady-state DC current path from Vdd0 or Vdd1 to ground, which insures a relatively low quiescent current consumption.

Since the proposed VCO have quadrature output signals, it already has two inversed signals, so the two inverters M3 and M4 can be eliminated, which simplifies the structure of the level shifter. To

be used to pull up the voltage level for VCO, this block should two symmetrical inputs and desire two symmetrical outputs as well as power supply inputs (cf. Figure 4.13).

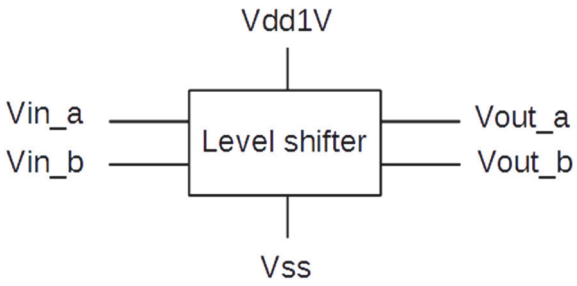


Figure 4.13: Block diagram of level shifter

First, we choose a pull-up level shifter to pull up the logic high level to 1V. However, the simulation results show that when the input voltage level is lower than 0.5V, the PMOS is too strong and the logic low level can't stay at ground, so another pull-down level shifter is mandatory.

The proposed voltage level shifter is composed by a level shifter with PMOS pull-up loads and a level shifter with NMOS pull-down loads as shown in Figure 4.14. After the necessary size adjustment (in our case: WP1/LP1=15um/30nm, WN1/LN1=4um/30nm, WP2/LP2=12um/30nm and WN2/LN2=5um/30nm), we can output a symmetrical high voltage level from the relatively low voltage level of VCO.

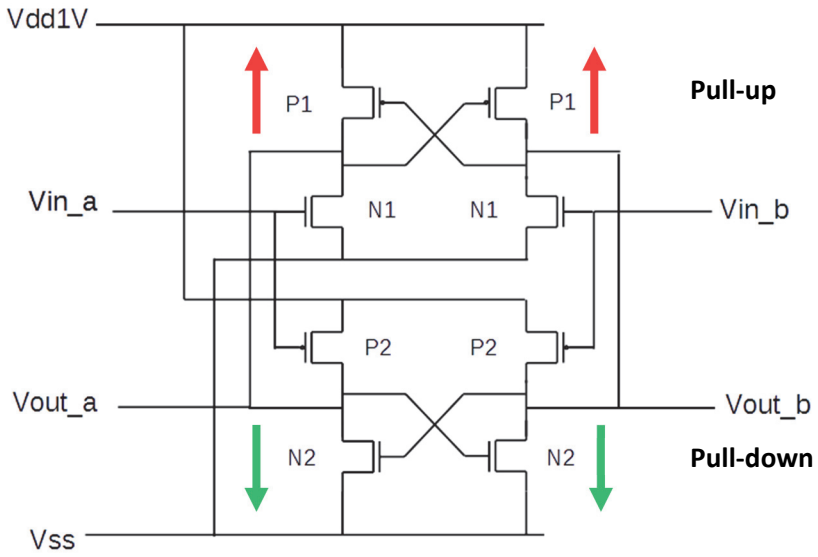


Figure 4.14: Structure of the proposed level shifter

Figure 4.15 shows a simulation example for this level shifter; it can pull up the voltage level from 0.7 up to 1V. The proposed level shifter works well when the output level decreases from 1V down to 0.35V which satisfies our requirements.

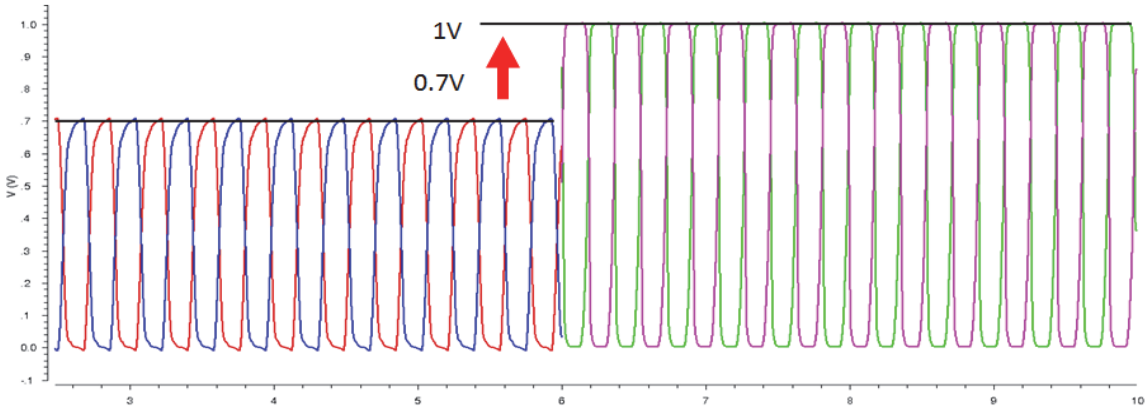


Figure 4.15: Simulation result for voltage level shifter

2.5. Simulation results and discussion

Thanks to the voltage level shifter, a complete VCRO is built in figure 4.16. The Four quadrature signals are what we care about, so we add two level shifters to these signals (0°, 90°, 180°, 270°). The load of the ring oscillator is still symmetrical and will not cause much impact.

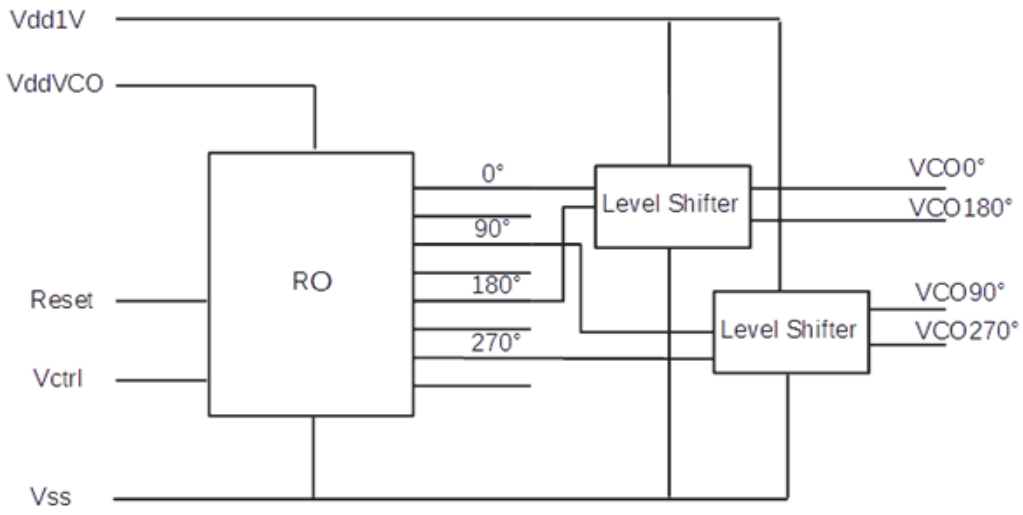


Figure 4.16: Complete structure of the VCRO

We have realized this circuit using Cadence and the frequency characteristic curve is depicted in Figure 4.17. The simulated result shows that this VCO has an output frequency range from 0.02GHz to 5.9GHz for an input voltage from 0.2V to 1.0V, and it operates almost linearly in two parts: when the input voltage is from 0.4 to 0.6V, the frequency varies from 0.9GHz to 5.9GHz which offers a slope of K_{VCO}=19GHz/V; when the input voltage is from 0.7 to 1.0V, the frequency range is from 5.5GHz to 5.9GHz, and its slope K_{VCO} is 2 GHz/V.

The maximum power consumption for the complete VCRO is 24mW, in which 8mW for level shifter and 16mW for the main VCRO block. It consumes the most power at the highest frequency

where input control voltage (Vctrl) is 1V. As Vctrl decreases from 1V, the power consumption of the main VCO block decreases much faster than that of level shifter.

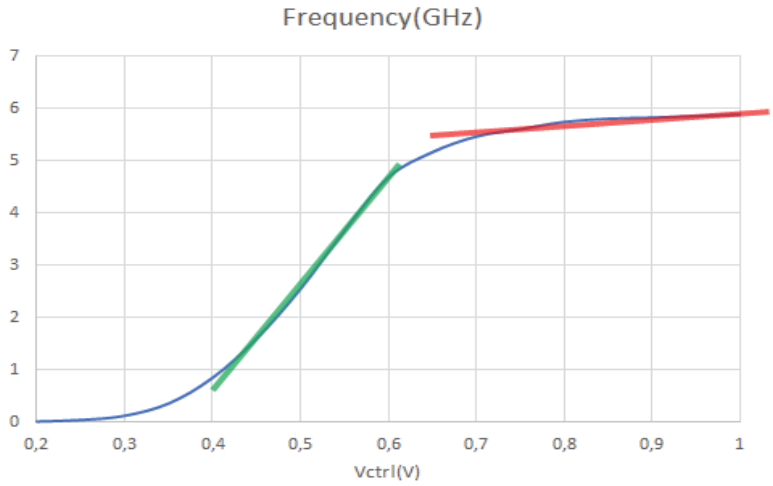


Figure 4.17: Complete structure of the VCRO

We noticed that when Vctrl is higher than 0.6V, the increase speed of VCO's oscillation frequency slows down. The reason is that when the oscillation frequency is high, the ring oscillator needs more input current and bias voltage, which causes the V_{ds} of upper PMOS transistor to become smaller and moves into linear region, so that the current of current mirror can't be well copied, thus a small K_{VCO} appears.

The way to keep V_{ds} in the saturation region is to reduce the bias voltage and current of the ring oscillator. Increasing the length L of the input NMOS transistor to decrease the current can do that. Figure 4.18 illustrates the frequency characteristic for VCO with different size of L. The larger L is, the better the linearity, but at the expense of the highest frequency and frequency tuning range.

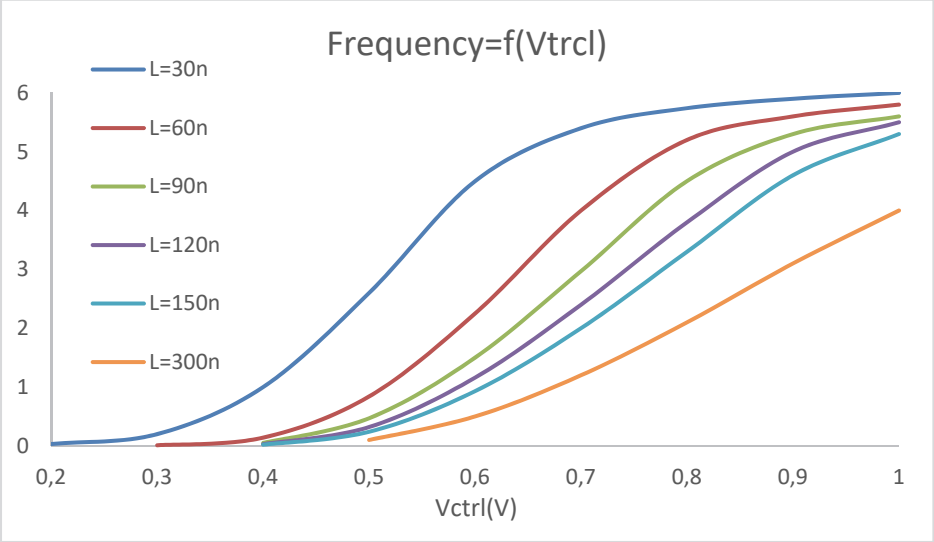


Figure 4.18: Frequency characteristic for different sizes of input NMOS

So in practical applications, we need to make a trade-off between linearity and frequency tuning range.

2.6. Conclusion

In this section, we proposed a novel structure of VCRO, implemented in 28nm UTBB-FDSOI technology and verified by simulation. The main block of VCO is composed by back-gate controlled current mirror and four-stage complementary ring oscillator. It should be noted that the proposed current mirror controlled by back-gate structure can reduce the small channel effect and offer therefore high output impedance. To make the oscillator compatible with other modules, a voltage level shifter is also considered.

The simulation results show that the proposed VCO has a wide input range from 0.2V to 1.0V and it operates almost linearly in two parts which offers a slope of K_{VCO}=19 GHz/V and 2GHz/V respectively. The maximum power consumption for the whole VCRO is 24mW where the input voltage is 1V.

3. Phase detector

3.1. Introduction of phase detector

A phase detector (PD) outputs a voltage signal which represents the difference in phase between the reference clock signal and the feedback signal, together with charge pump and filter to generate the input voltage for VCO.

As shown in Figure 4.19, the transfer function of an ideal PD is a straight-line crossing with zero, i.e. the output signal value is proportional to the input phase difference. Such a phase detector can be described by its linear gain Kpd. The actual PD has many non-ideal characteristics, such as nonlinearity, phase error, limited output range, etc.

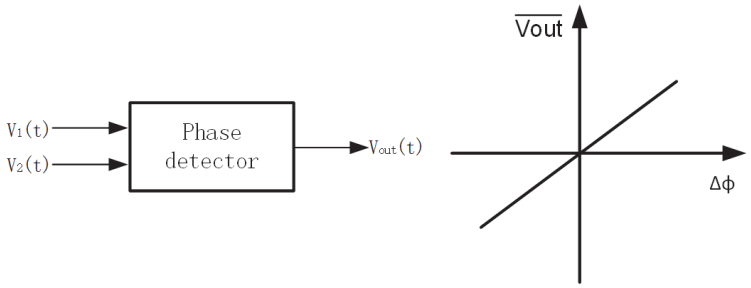


Figure 4.19: Definition of phase detector

Analog multiplier is used for PD in LPLL (Analog or Linear PLL) to compare sinusoidal signals. For DLPL, the simplest PD can be made from an XOR logic gate to detect square wave signals. Figure 4.20 illustrates the operation of XOR gate as a phase detector. As phase difference between the two inputs varies, so does the width of output pulse, which provides a DC signal proportional to the phase difference Δϕ. When the two input signals are completely in-phase, output will have a constant level of zero.

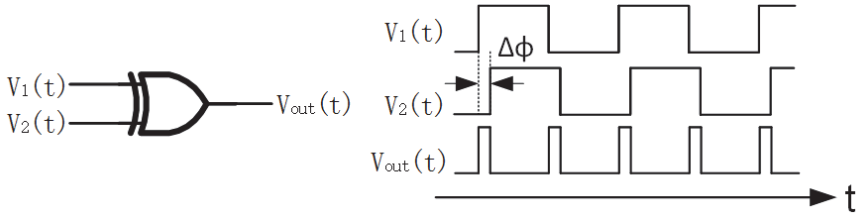


Figure 4.20: XOR gate as phase detector

Assuming that the average value of Vout is shifted to zero for zero phase error, Input-output characteristic for XOR phase detector can be plotted in Figure 4.21. We can see from the figure when input phase difference is between -π to π, Input and output characteristic have a linear relationship, which gain is Vout/π. When the absolute phase difference is large than π, the slope will decrease in the opposite direction, causing the phase-locked loop to be unstable. PD-based on XOR is only suitable for applications where the frequency of two clock signals is close. Moreover, XOR PD is sensitive to asymmetry input signal or different duty cycles signals. The effect of input asymmetry is to reduce the loop gain of the DPLL and also results in a smaller lock range, pull-in range, etc [10]. PD is therefore not an ideal choice for PLL and is now superseded by phase frequency detector described in next paragraph.

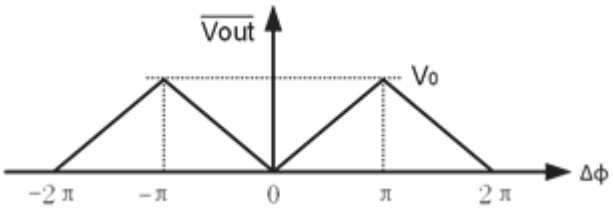


Figure 4.21: Input-output characteristic for XOR phase detector

3.2. Introduction of phase-frequency detector

For periodic signals, we prefer a PD which can detect both the phase and frequency difference between the two input signals which is called phase frequency detector (PFD). Figure 4.22 shows PFD bloc symbol and plots the output versus phase error, it works well in all the phase differences.

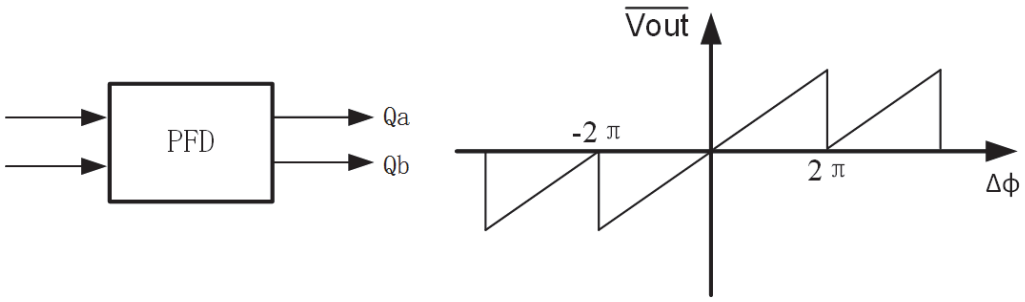


Figure 4.22: Input-output characteristic for three-state PFD

The PFD circuit is built with sequential logic to create three-state and responses to raise edges of the two inputs. Q_A and Q_B provide pulse widths which are proportional to ϕ_A-ϕ_B or ω_A-ω_B; generally Q_A and Q_B are called 'up' and 'down' signals respectively. Figure 4.23 Illustrates an example when $\phi_A>\phi_B$ or $\omega_A>\omega_B$, Q_A is therefore detected and rises to high voltage level. When $\phi_A<\phi_B$ or $\omega_A<\omega_B$, Q_B will be detected in the same way.

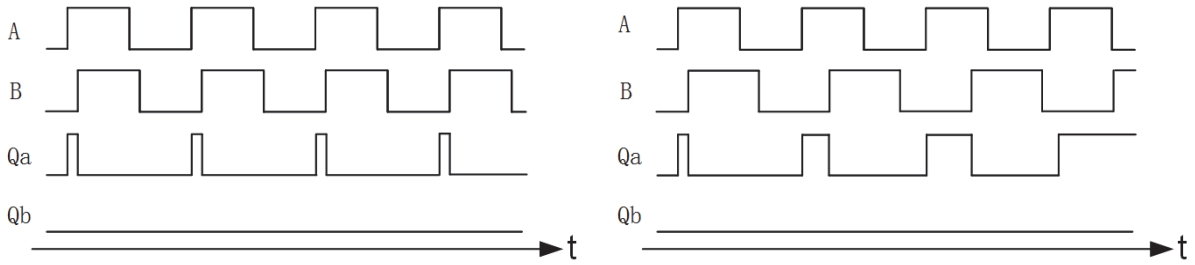


Figure 4.23: Conceptual operation of PFD

The PFD improves the pull-in range and lock time over simpler phase detector designs such as XOR gates which have a poor perform when the phase difference is too large. The PFD has the advantage of producing an output even when the two signals being compared differ not only in phase but in frequency. The output signal of the PFD depends on the phase error in the locked state and on the frequency error in the unlocked state. Consequently, the PFD will lock under any condition [10]. A phase frequency detector prevents a "false lock" condition in PLL applications, in which the PLL synchronizes with the wrong phase of the input signal or with the wrong frequency (e.g., a harmonic of the input signal) [11]. Therefore, PFD has a wider range of applications in DPLLs.

There are many implementation structures for PFD. Figure 4.24 illustrates a simple implementation composed by two triggers and a AND gate for reset. Assume that the initial values for reference and feedback signals are '0'. When Reference varies from '0' to '1', Up will follow to '1' also. Then Feedback changes from '0' to '1', so does Down. At that time both Up and Down are '1', reset signal functions, thus activating the enable side of the flip-flop to force Up and Down to '0'.

Unlike XOR gate PD, PFD generates two outputs 'Up' and 'Down' which are not complementary and reset, so called 'three-state PFD'.

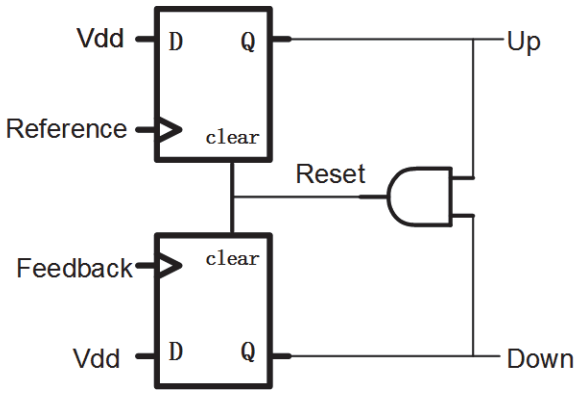


Figure 4.24: Three-state PFD

Figure 4.25 shows a PFD structure in gate level [12]. The circuit speed depends on the delay time necessary to reset all internal nodes. The critical path consists of 6 gate delays in this case. If the phase difference is too small, reset signal can't work correctly which we called dead zone problem (cf. Figure 4.25). The simulation result of conventional PFD shows that it suffers from dead zone of hundreds of picoseconds which causes phase jitter.

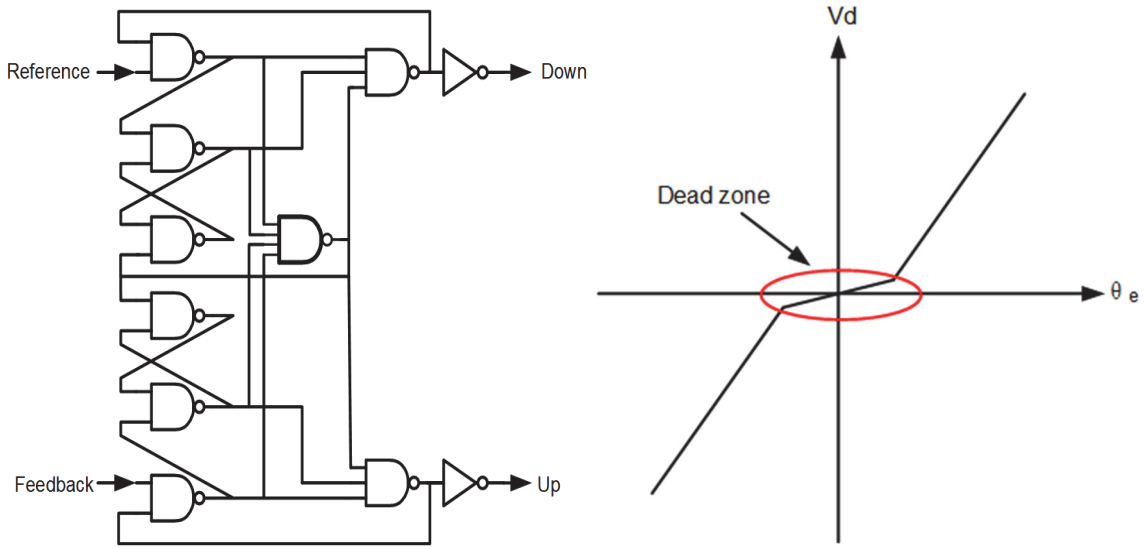


Figure 4.25: Gate level of conventional PFD and its dead zone problem

There are several other structures of PFD to reduce dead zone. For example, pre-charge PFD in 3.3V supply 0.6µm CMOS technology and modified pre-charge PFD in 5V supply 0.8µm CMOS technology presented in reference [13] and [14]. Pre-charge PFD reduces dead zone to 200ps in low frequency and modified pre-charge PFD is even less, but it grows fast when frequency is more than 1GHz. Dead zone problem is still a big challenge for the PFD to operate in high speed PLLs.

3.3. Structure of complementary PFD

A novel PFD circuit, by Thakore et al. [15], has been built with the smallest size drawn in 0.18µm CMOS process to obtain a high-speed phase frequency detector. In their works, the PFD has two input clocks 'REF" and 'FB', two output signals 'Up' and 'Down'. As shown in Figure 4.26, we have modified this structure by doubling all the input clocks and output signals to adapt the negative logic which will be used later in the charge pump and the overall complementary PLLs.

Figure 4.27 illustrates the inner structure for one bloc of complementary PFD which has four inputs (two pairs of complementary inputs) and two outputs (a pair of complementary output). This circuit uses complementary logic design concept introduced in chapter 2, which outputs complementary logic signals. Here we use the upper circuit as an example to analyze its functions.

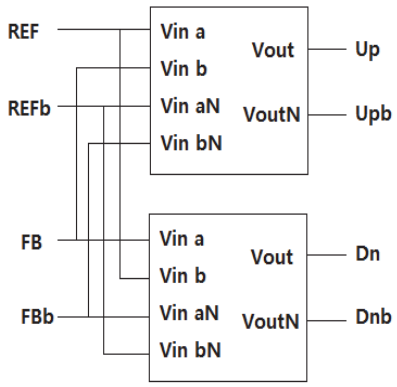


Figure 4.26: Optimized complementary PFD

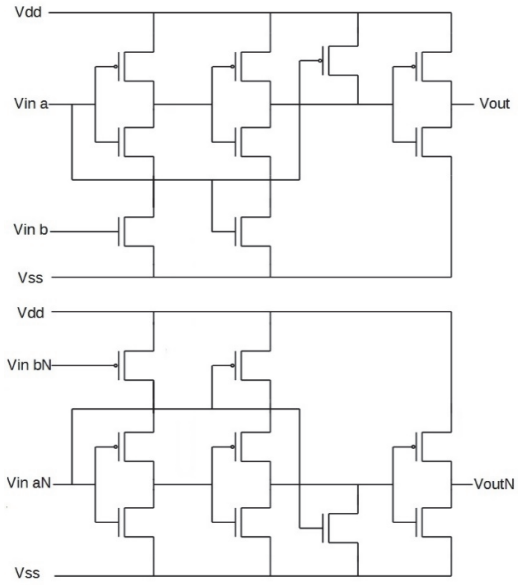


Figure 4.27: Structure of a complementary PFD block

From upper circuit in Figure 4.27, here are a major input 'Vin_a' and a secondary input 'Vin_b'. The Vin_a largely determines the change Vout, and the function of the Vin_b is similar to the reset signal. Figure 4.28 describes the operation details for proposed PFD in all the three input conditions:

- Case 1: When Vin_a is '0', M1 and M7 turn on to pull up the tension of a1 and a2 nodes to '1' regardless of Vin_b (normally Vin_b is '0'), Vout is '0' after the last stage inverter.
- Case 2: When Vin_a changes to '1' and Vin_b stays at '0', M6 turns on and M7 turns off, the previously stored high level '1' at node a1 will pass through two inverters and reach the output.
- Case 3: When Vin_a and Vin_b both change to '1' (like the two input signals have the same phase and frequency), M3 and M5 turn on and M7 turn off. This circuit is now equivalent to three inverters in series and Vout will be '0' as if it is reset.

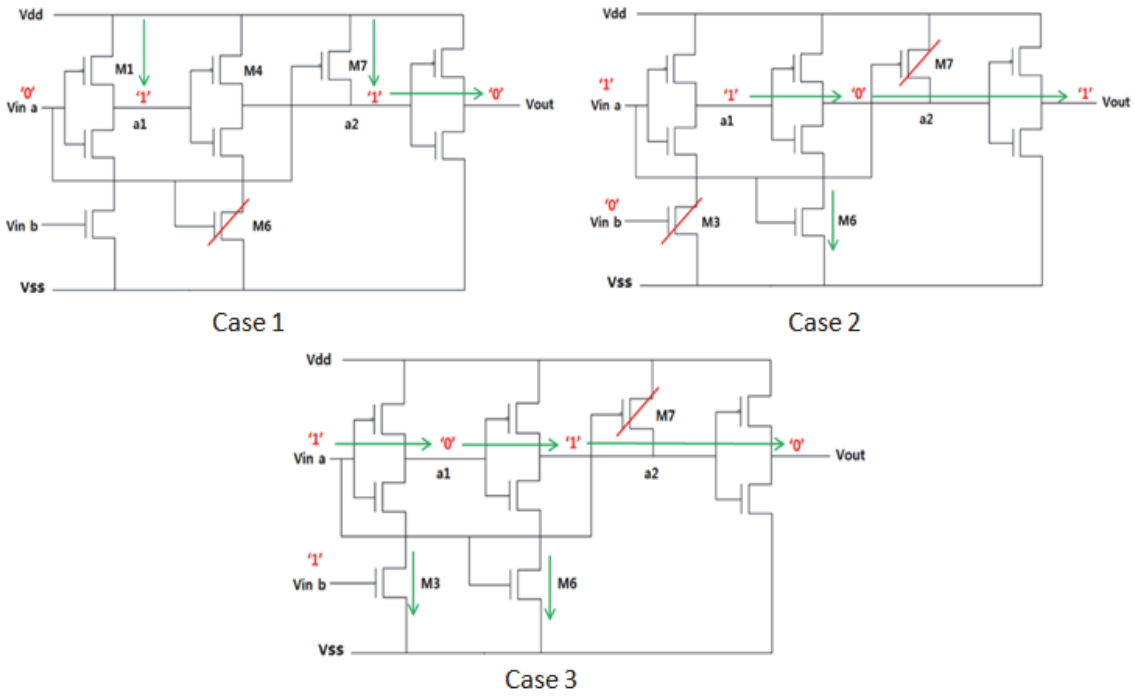


Figure 4.28: Operation details for PFD in all the input conditions

What's more, this circuit doesn't have special reset path as three-state PFD depicted in Figure 4.24, as a result, it can reduce greatly the dead zone caused in reset routing path. The circuit delay is maximum at reset case, which is only three-stage inverter delay. If appropriate sizes are used, we can adjust the delay to be small enough.

3.4. Simulation results and discussion

We have realized this circuit depicted in Figures 4.26 and 4.27 using Cadence and run some transient simulations to verify its behavior. The voltage supply is 1V, with typical conditions of process and temperature in 28nm FDSOI technology. Let's take the two input signals' frequency are 1GHz for example (cf. Figure 4.29).

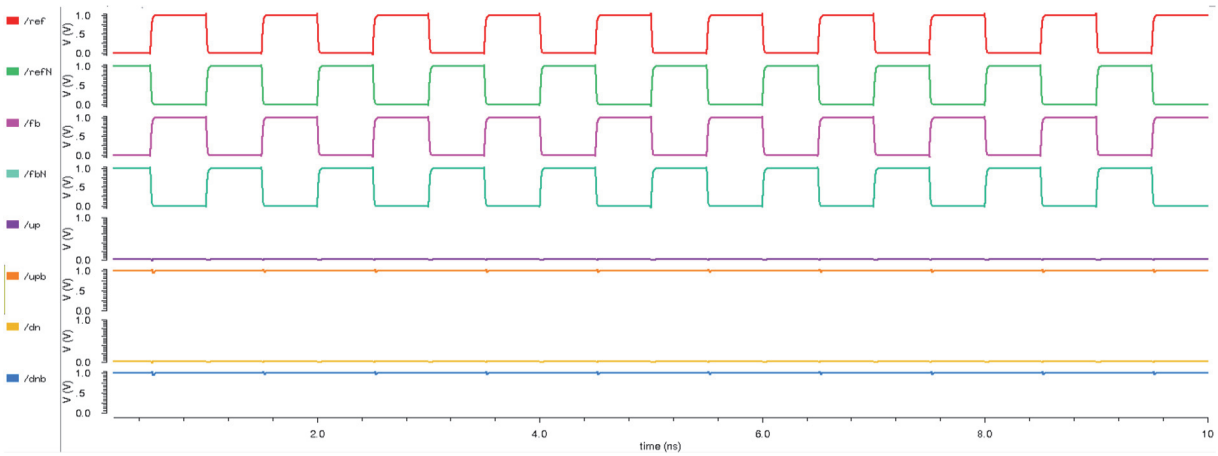


Figure 4.29: Condition when two input signals are completely in-phase

As shown in Figure 4.29, when reference signal and feedback signal are completely in-phase, output will have a constant level of zero (high level in negative logic). There is no glitch at all which is better than the reference[15].

We have implemented this structure in complementary logic without back-gate control. We have shown here only the positive logic. Another transient simulation result is shown in Figure 4.30, where the reference signal turns up before the feedback signal. In this condition, the output signal 'Up' turn to '1' when the reference signal rises as shown in green marker, and its reset function occurs after the transition of feedback clocks as shown in black marker. The other output signal 'Down' stays at '0' because the phase of the reference signal is always ahead of feedback signal's phase.

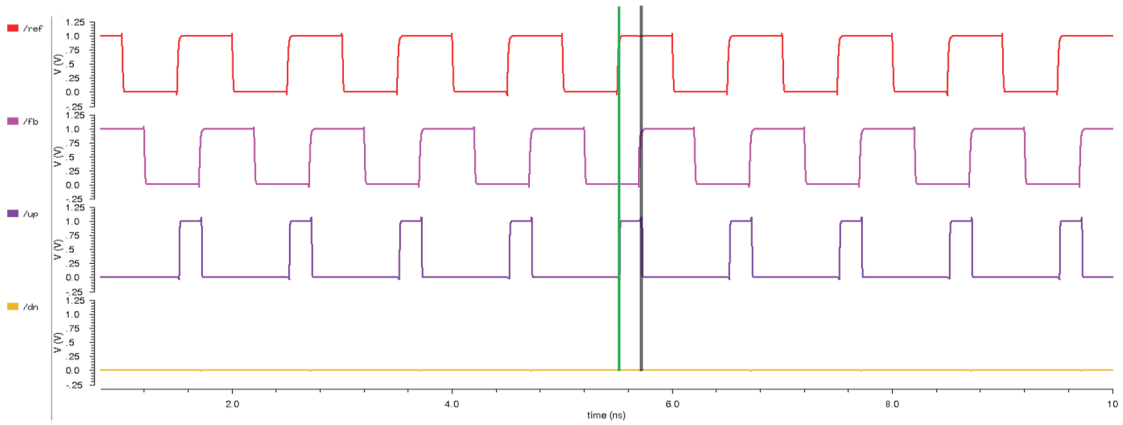


Figure 4.30: Condition when reference signal turns up before feedback signal

Figure 4.31 illustrates the opposite condition where reference signal turns up after the feedback signal. So, the phase difference between the two inputs signals is converted to pulse width for output signal 'Down', and 'up' stay at '0'.

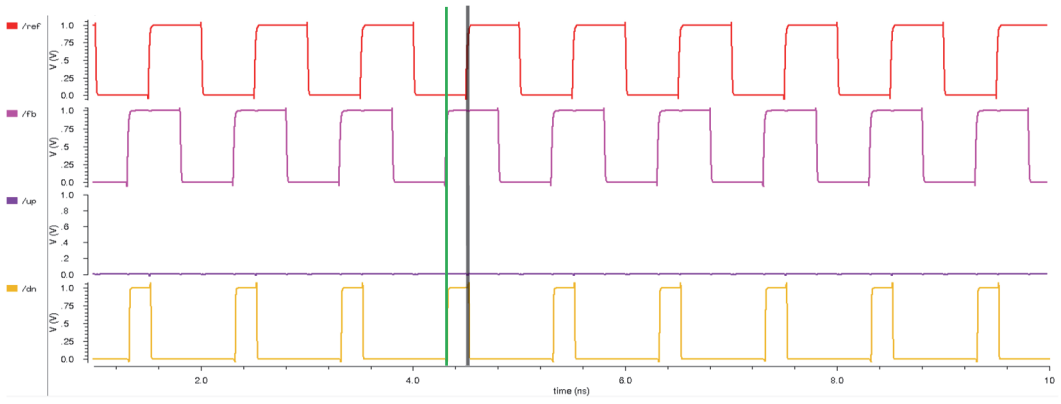


Figure 4.31: Condition when reference signal turns up after feedback signal

We can also put all the input and output signals together to verify the signal symmetrization as shown in Figure 4.32.

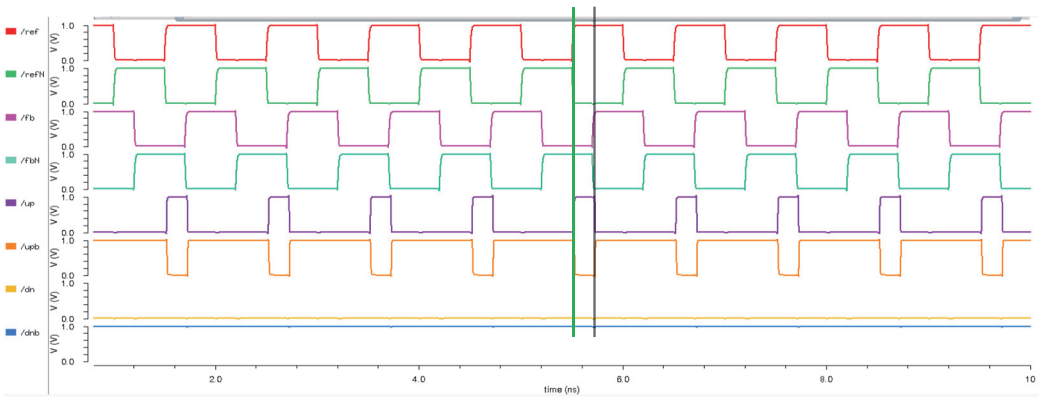


Figure 4.32: Validation of signal symmetrization

All the simulations above are based on the same input frequency of 1GHz. Figure 4.33 described a condition where frequency of reference signal is 1GHz; feedback signal's frequency is 0.95GHz. As $\omega_{ref}>\omega_{fb}$, output signal 'Up' turns up to high level with different duty cycles to force following VCO to increase its input voltage, thereby increasing the output or feedback frequency.

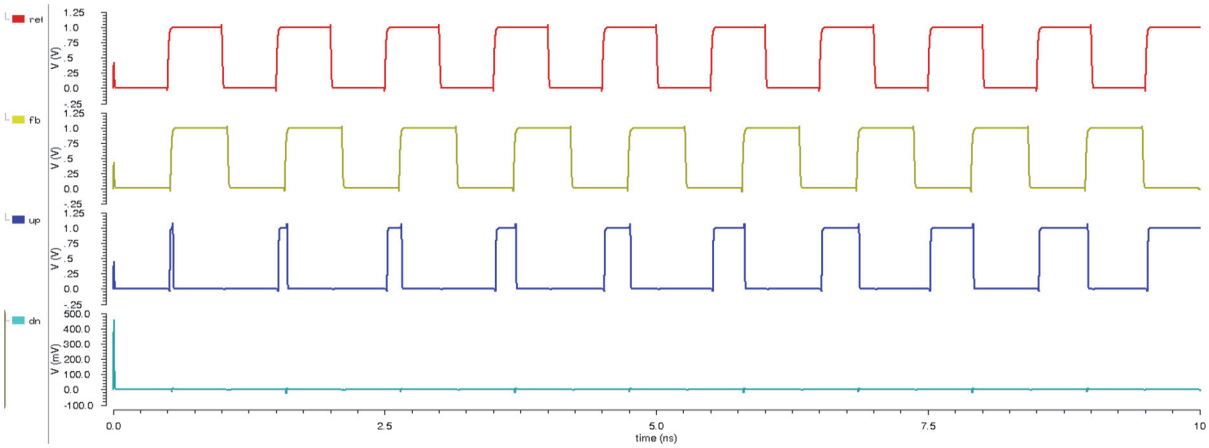


Figure 4.32: Condition when $\omega_{ref}>\omega_{fb}$

The power consumption of this PFD is about 10uW, and the minimum delay between the two input signals is only 10ps, which is much smaller than other conventional PFDs.

Moreover, a back-gate control structure could be added as indicated by the arrows to calibrate the symmetrical signals, as shown in Figure 4.34, but at the cost of speed slowing down and increasing unwanted glitches. In order to balance speed, we use the PFD without back-gate controlled structure in our design.

Figure 4.35 shows a low power simulation example when reference signal turns up before feedback signal. As Vdd decreases from 1V to 0.5V, the output signals work correctly, but also at the cost of speed. This is not an issue as for lower supply voltages the ring oscillator will be also slower.

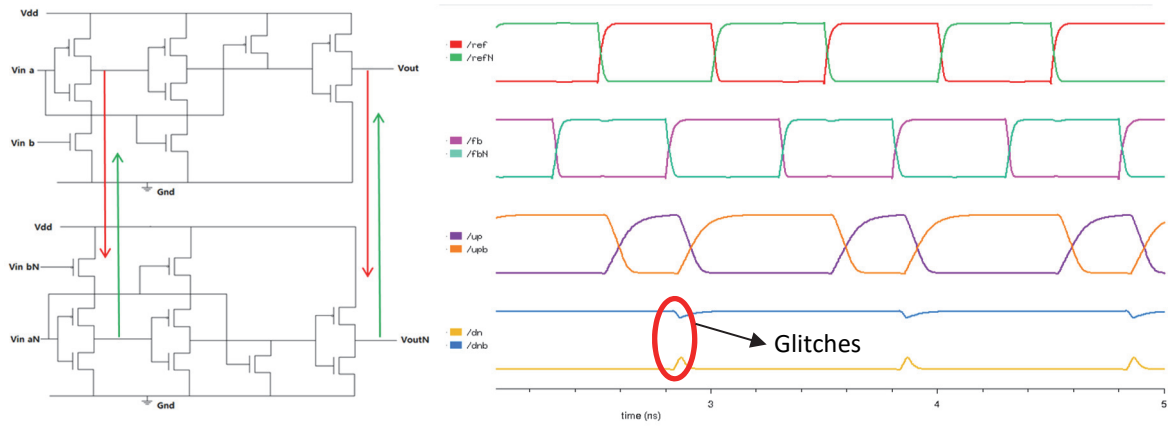


Figure 4.34: Structure and simulation result for PFD with back-gate control

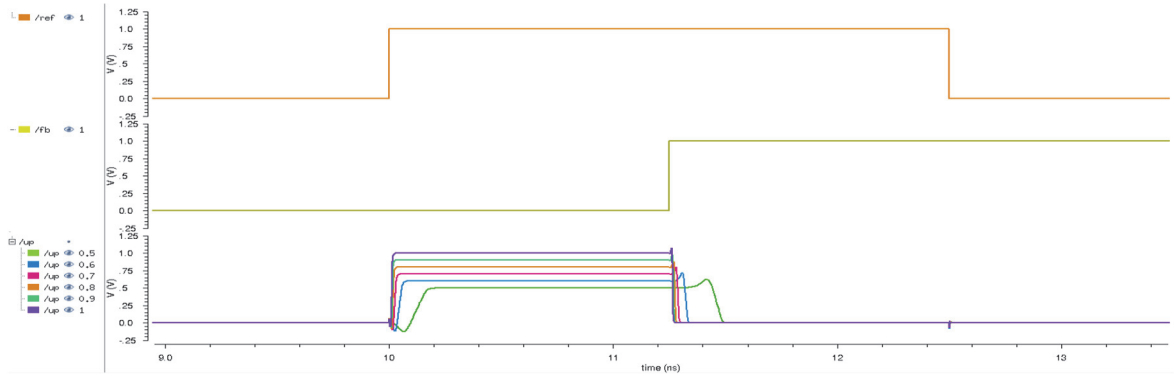


Figure 4.35: PFD performances at low voltage

3.5. Conclusion

In this section, we proposed and realized in simulation a complementary PFD which can overcome dead zone problem. The proposed PFD has a small power consumption of about 10uW at 1V power supply. The minimum delay between inputs and outputs is only 10ps, which determines working frequency up to several GHz. What's more, this PFD can work normally at low power supply down to 0.5V, at the cost of speed.

4. Charge pump

4.1. Introduction of charge pump

Charge pump (CP) is an important PLL's block placed after PFD which converts the phase or frequency difference information into a voltage to tune the VCO. A charge pump can be considered as a three-position switch controlled by output signals of PFD as shown in Figure 4.36. The following table 4.1 summarizes all the states of classic three-state charge pump.

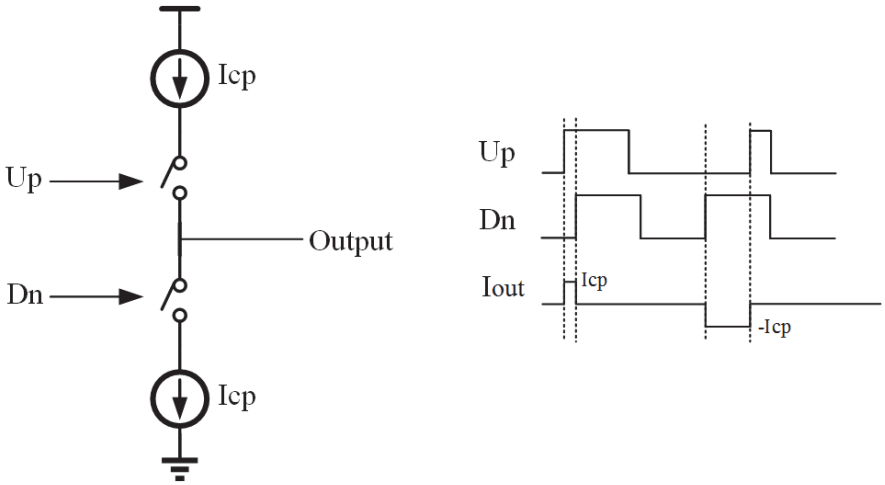


Figure 4.36: Conceptual operation of CP

Table 4.1: Operation states of three-state charge pump

Up	Down	Iout	State of CP
'0'	'0'	0	Constant Vout
'1'	'0'	Icp	Vout Pull-up
'0'	'1'	-Icp	Vout Pull-down
'1'	'1'	0	Constant Vout

From the figure 4.36 and table 4.1, we can see when switch is set in 'Up' position, it delivers a positive pump current Icp at the output to charge the load capacitor thereby pull up the output voltage. On the other hand, when switch is set in 'Down' position, it delivers a negative pump current -Icp at the output to discharge the load capacitor therefore pull down the output voltage. When both 'Up' and 'Down' of PFD are off, i.e. the two switches are open, thus isolating the loop filter from the charge pump to keep output voltage constant. In ideal case, when both 'Up' and 'Down' are on, the two switches are closed, positive and negative current compensate each other. As a result, output voltage also keeps constant because of zero output current. The two output signals 'Up' and 'Down' of three-state PFD we proposed will not be '1' at the same time, so the last state doesn't appear and thus avoids the current mismatch.

The switches in Figure 4.36 can be implemented by MOS transistors with current mirror, but there are many limitations in such so called drain-switching charge pumps.

First, as switch from open to closed, the drain capacitance of the current source needs to follow the process of charging and discharging to make the current source works normally. So, this charge pump switch is relatively slow. Second, since the switch is directly connected to the charge pump output and non-ideal characteristics of the MOS switch, such as charge injection and clock feedthrough, the change in the source voltages can creates glitches in the capacitor current, which

can result in a jump in the stored voltage and therefore cause undesirable spurious tone and charge error [16].

Figure 4.37 illustrates an improved conventional charge pump called current steering charge pump which can improve those problems above. This circuit introduces complementary switches and an amplifier as feedback to stabilize output voltage from charge jump [17]. What's more, as current source can always keep current flowing through one of the complementary switches, the charge pump opening and closing speed will be greatly improved. However, performance enhancement is at the cost of extra complexity, area, and power consumption.

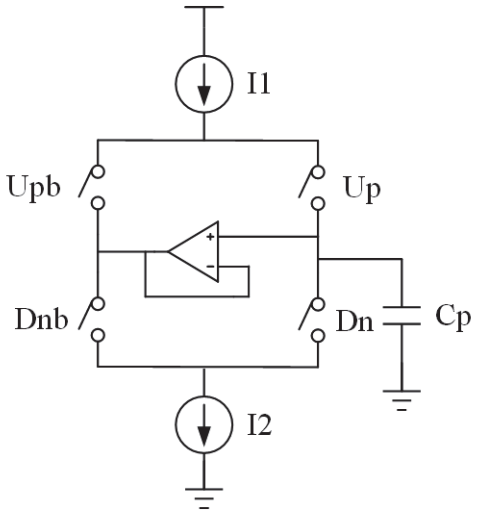


Figure 4.37: Current steering CP

4.2. Structure of proposed CP

A new CP circuit, by R.A. Baki and M.N. El-Gamal [18], has been built in 0.18µm CMOS process with 1V power supply. In their works, both pull-up current and pull-down current are set to 10µA, the output range is from 100mV up to 900mV, working frequency is up to 500MHz with an average power consumption of 60µW.

Based on this circuit, we proposed a novel charge mirror with back-gate controlled output current mirror. Illustrated in Figure 4.38, this charge pump is composed by pull-up and pull-down networks. Let's take the upper pull-up sub circuit for example:

- When 'Up'= '0', P1, N1 and P3 are all on; the small current in P3 and P5 can be negligible. Then, the output voltage Vcp at the capacitor therefore should remain stable.
- When 'Up'= '1', P1 and N1 are both off, P3 is off because there is not enough V_{gs} for P3 to open.

Thus, current source I1 drives P4 and P5 which form a current mirror. The output capacitor will be charged by the copied current from I1 to raise output voltage Vcp.

The working principle of pull-down network below is the same as that of pull-up network.

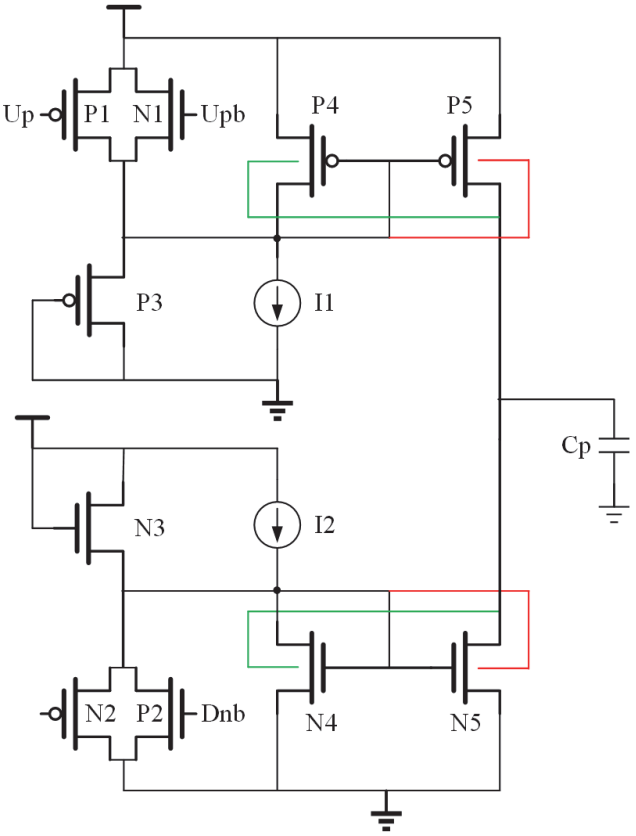


Figure 4.38: CP with back-gate controlled current mirror

In our design, both pull-up and pull-down current are set to 20µA. The two pairs of current mirrors P4, P5 and N4, N5 therefore use large size of transistors for current match.

As presented in chapter 4 section 1.2, a relatively small size of back-gate control current mirror can be used to replace of convenient current mirror in large size offering high output impedance.

4.3. Simulation results and discussion

We have realized this circuit using Cadence and run some transient simulations to verify its functions. The voltage supply is 1V, with typical conditions of process and temperature in 28nm FDSOI technology. To detect the working state of charge pump, a capacitor Cp of 300fF is added to observe the pull-up, pull-down and hold-on states of the output voltage.

First, Figure 4.39 shows all the three cases where 'Up'= '1', 'Down'= '1' and both 'Up' and 'Down' are '0' respectively. When the simulation time is before 30ns, 'Up'= '1', pull-up network

works. A pull-up current from I1 charges output capacitor Cp to raise output voltage. When transient time is between 3ns and 60ns, 'Down'= '1', on the other hand, a pull-down current from pull-down network discharges Cp to let output voltage down. When time is after 60ns, both 'Up' and 'Down' are '0', no current is steered from current mirror therefore output voltage remains stable.

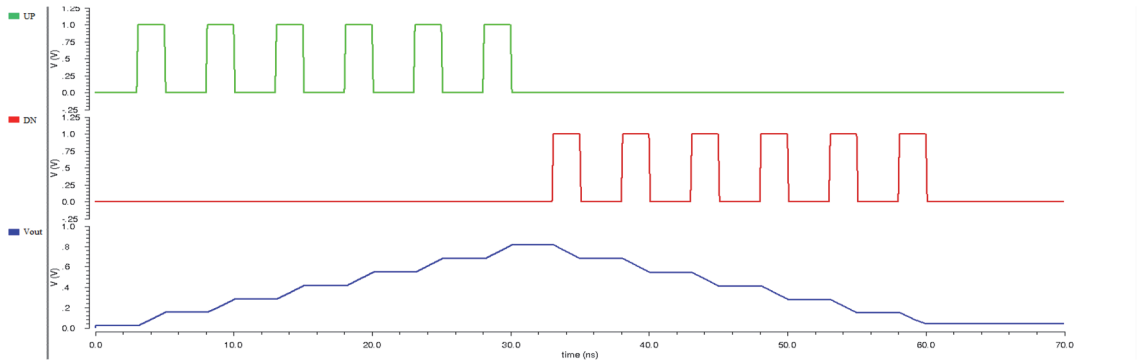


Figure 4.39: Simulation of pull-up, pull-down and hold-on

Then, we performed a mismatch test between the two output currents from pull-up current I1 and pull-down current I2. We configured 'Up' and 'Down' signals alternately in high level which have the same duty cycle therefore output capacitors are repeatedly charged and discharged in the same way and never in hold-on state. In the PLL system, this case happens when the transient phase difference between the reference signal and the feedback signal is π.

From the simulation result (cf. Figure 4.40), we can see that the output voltage level is almost stable, resulting from two output currents that are approximately symmetrical and equal in magnitude. With our optimized sizes, the measured pull-up current and pull-down current are about 20µA in absolute value which have a quiet small current mismatch.

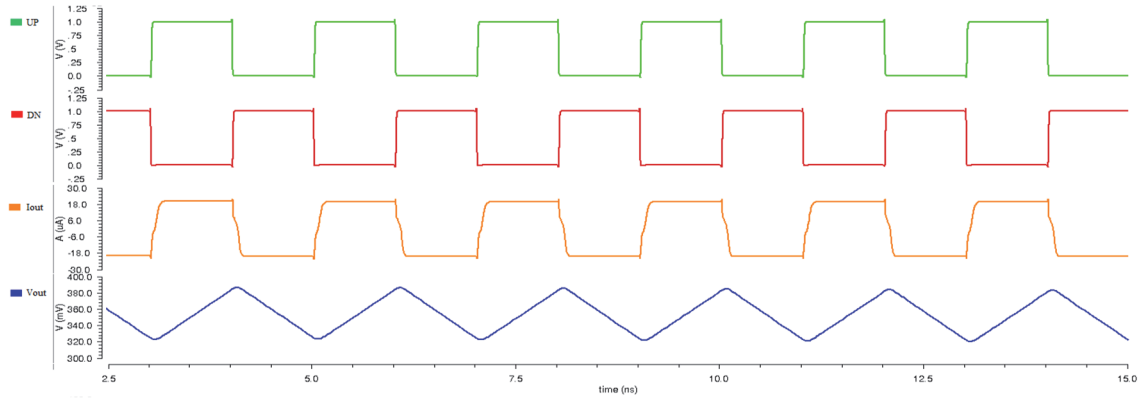


Figure 4.40: Verification of mismatches between output I1 and I2

Then, another simulation is realized to compare the proposed CP with and without back-gate control structure in output current mirror. Figure 4.41 shows the simulation result taken the pull-up state for example.

We can observe from the red waveform that without back-gate control structure, the output current is not constant in such a small size (L=30nm) which causes a varied slope for voltage ramp. This unwanted nonlinearity results in the difficulty for PLL system calculation. A current mirror with back-gate structure can overcome this problem. As shown in blue waveform, it has a stable output current about 20µA and therefore a constant slope for voltage ramp. It can be noticed that as the output voltage increases up to about 0.8V, the transistor P5 can't be kept in saturation region and the output current will be significantly reduced. Conversely N5 can't be kept in saturation region when output voltage decreases down to about 0.2V. So, the proposed charge pump presents linearity when the voltage output range is between 200mV and 800mV.

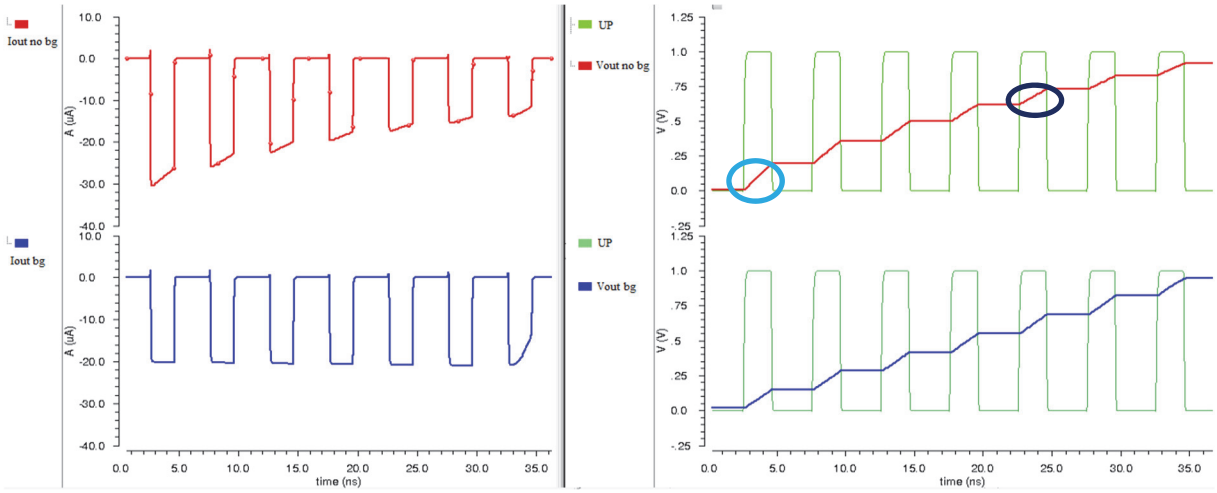


Figure 4.41: Simulation with and without back-gate control structure

Moreover, our simulation results show this charge pump can work with the frequency up to 2GHz with a power consumption of 72µW in average under 1V power supply. If the current source is 10uA, the average power consumption is 51µW which is smaller than reference [18].

Figure 4.42 shows a low power simulation example of varying Vdd for charge pump with same input configuration of Figure 4.40. When Vdd decreases from 1V to 0.6V, the charge pump can output approximate stable and symmetrical current for pull-up and pull-down networks. When Vdd is 0.5V, push-down current is visibly reduced resulting in a significant mismatch.

Figure 4.43 and 4.44 illustrate the simulation results of the two blocks of PFD and CP together. When reference signal turns up before feedback signal, PFD output signal 'Up' drives pull-up network of charge pump to charge output capacitor resulting in a voltage raise. On the other hand, when reference signal turns up after feedback signal, PFD output signal 'Down' drives pull-down network of charge pump to discharge output capacitor resulting in a voltage fall. Both output voltages don't exhibit any spurious jump phenomenon and our circuit turns out to work well.

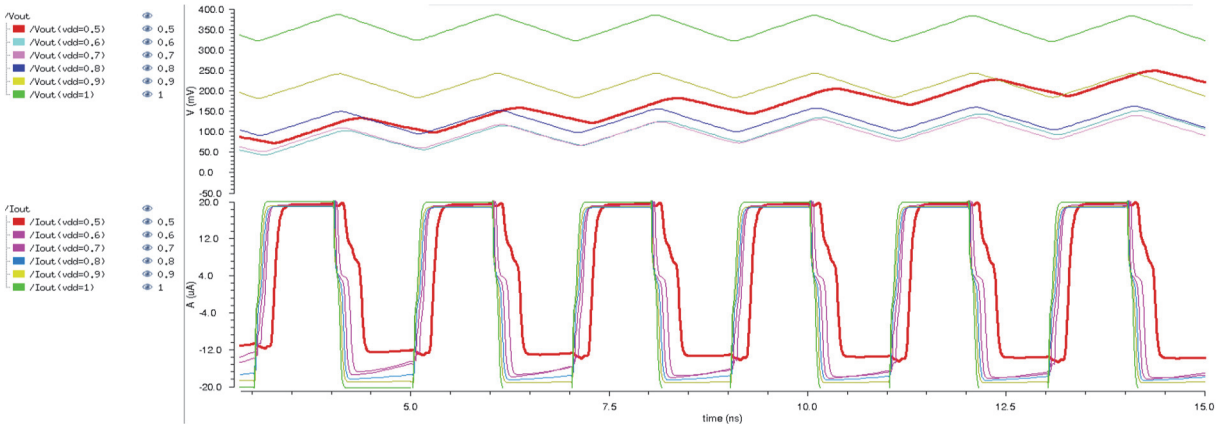


Figure 4.42: Low power simulation results for power supply varies from 1V to 0.5V

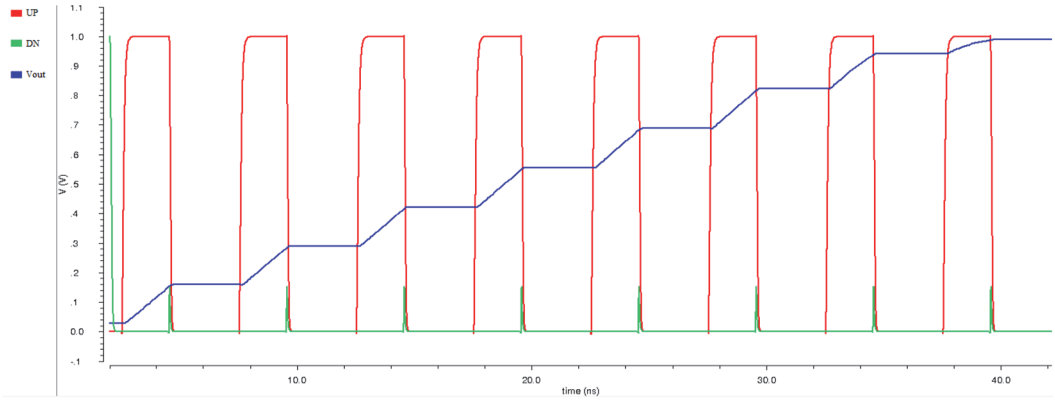


Figure 4.43: Simulation result of reference signal turns up before feedback signal

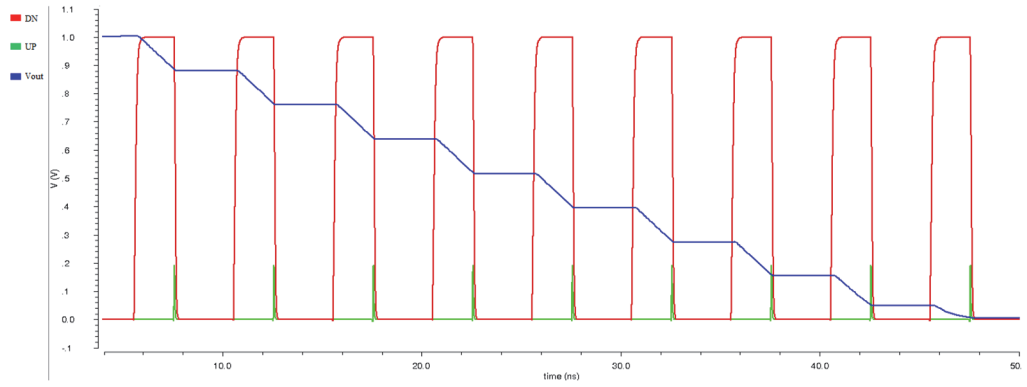


Figure 4.44: Simulation result of reference signal turns up after feedback signal

Concerning low power design, we tried to decrease the power supply for both PFD and CP. We take reference signal turns up before feedback signal and the input signal frequency is 250MHz for example. The simulation results in Figure 4.45 show that the PFD and CP blocks works correctly with the power supply down to 0.6V. When the power supply is 0.5V, output voltage (blue curve) is still charged by pull-up current (green curve). This is because when Vdd is too low, P1 and N1 in pull-up

network can't be in on state completely, so there is current of about 5 µA pass through the current mirror to the output resulting in such error.

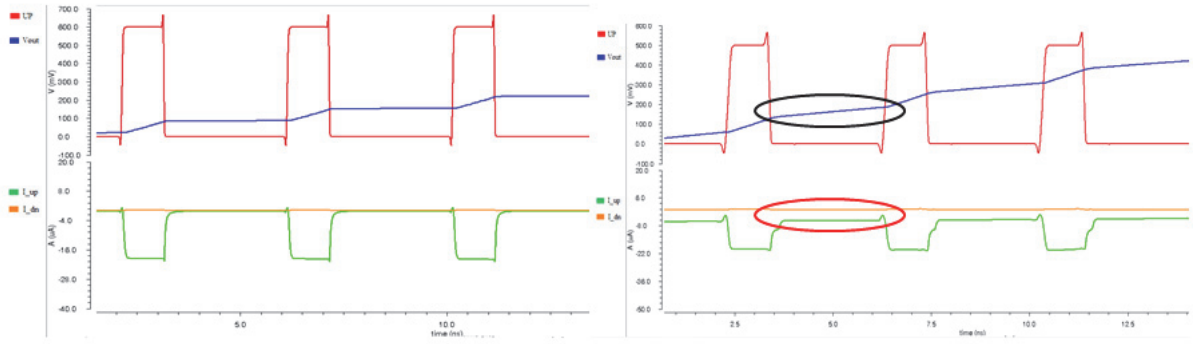


Figure 4.45: Low power simulation results for Vdd is 0.6V and 0.5V respectively

4.4. Conclusion

In this section, we proposed a new structure of charge pump composed by pull-up and pull-down network with back-gate controlled current mirror. The proposed charge pump can work with a small mismatch at frequency up to 2GHz with a power consumption of 72µW in average under 1V power supply. We also did some simulations of PFD and CP together; the simulation results turned out that the whole block of PFD and CP can work correctly in a low power supply down to 0.6V and the output don't exhibit any spurious jump phenomenon.

5. Frequency divider

5.1. Introduction

The frequency divider constitutes an important part of the feedback loop of a PLL, which function is to divide the high-frequency signal of oscillator to compare with the reference clock. The basic performance requirements for the divider are speed and low phase noise. The input of the frequency divider is the circuit with the highest operating frequency in the whole PLL system and is the main power consuming block, especially in a CMOS implementation [19].

5.2. Introduction of prescaler based divider

Generally, a programmable counter can be used as the frequency divider. For example, a counter which exports a rising edge signal when every N input clock rising edges count could realize the function of a divider with a frequency division ratio of N. However, programmable counter

usually works at a lower frequency of about 1 GHz or less and cannot achieve the desired high frequency division.

The common used structure of frequency divider is composed by two parts of the front end and the back end, according to the operating frequency. The high frequency front end part which we called prescaler first divides the high frequency signal to a relatively lower frequency. Then there is a programmable counter at the back end to further divide the frequency to the final desired frequency. The most common prescaler is the dual-modulus prescaler composed by two possible frequency dividers with division ratios of N and N+1, which is decided by a modulus control signal [20].

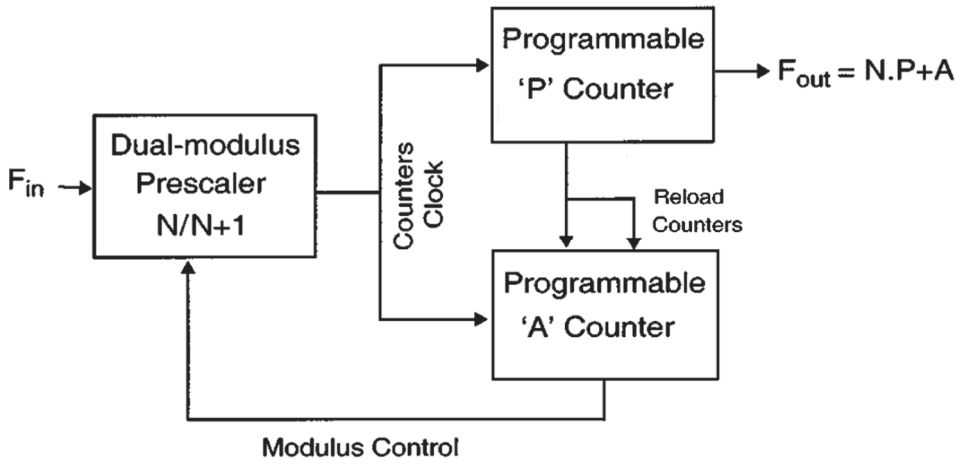


Figure 4.46: Programmable divider based on a dual-modulus prescaler [20]

Figure 4.46 shows a classic fully programmable divider based on a dual-modulus prescaler. Prescaler is controlled by the control signal to have a frequency division ratio of N or N+1, and there are two programmable counters in back end which satisfy P≥A. Prescalers are available usually in modulus 2, 4, 8, 5 and 10.

The working principle is as follows:

At a new cycle, the division ratio of prescaler is N+1, that is, after every N+1 oscillation cycles, prescaler outputs one clock edge to the two counters at the back end. When counter A receives A input clock edges (we have the limitation of P≥A), it outputs a clock edge as the modulus control signal which change the division ratio of prescaler to N and then counter A stops. At this point, the divider has received (N+1)A oscillator clock edges. After the P counter receives the next P-S clock edges from prescaler, the P counter outputs a clock edge. This means that the divider receives (P-A)N oscillator clock edges again. The output clock edge of counter A resets the entire divider, and a whole frequency division cycle is over.

In one division cycle, counter P received (N+1)A+(P-A)N cycles, which NP+A cycles. In this way the divider achieves a frequency division ratio of PN+A.

Common fixed-integer prescalers are available in modulus 2, 4, 8, 5 and 10, and can operate at frequencies in excess of 10 GHz [21].

Because of high speed and simple circuit structure, this frequency divider is widely used in high-speed communication circuits. But the limitation is the dual-modulus programmable divider can't realize any division ratio like a fully programmable counter. For example, when N/N+1 is 8/9, the possible division ratio is P*8+A, P≥A. Only when division ratio is 56(7*8+0) or more, the divider can achieve all the continuous division ratios, but can't achieve any frequency division ratio less than 56. Such as 55(6*8+7), 46(5*8+6) and 47(5*8+7), because these division ratios don't satisfy the limitation of P≥A.

5.3. Proposed LFSR based divider

We propose a Linear-Feedback Shift Register (LFSR) using complementary logic to avoid the above prescaler limitations.

A linear-feedback shift register is a shift register whose input bit is a linear function of its previous state [22], [23]. Normally, a XOR gate is used to change the state of a certain bit and other bits are shifted by the previous bits. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its previous state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle it must eventually enter a repeating cycle with can produce a sequence of bits that appears random and has a very long cycle as a counter.

Applications of LFSRs include generating pseudo-random numbers, pseudo-noise sequences, whitening sequences and what we will use here, fast digital counters [24].

There are two main structures of LFSR: Fibonacci LFSR and Galois LFSR. Figure 4.47 and 4.48 illustrate the example of 16-bit Fibonacci LFSR and Galois LFSR respectively.

A LFSR in Fibonacci mode strictly applies the definition of an LFSR: the bits of the different stages are added and propagated to a certain stage and all the stages shift one state towards the propagation direction. The bits in the LFSR state that influence the input are called taps. In this example, tap 1 is determined by bits 11, 13, 14, 16 together. The maximum delay appears in bit 16 which is 3 times unit XOR gate.

In Galois LFSR mode, the bit of a certain stage is added to another bit before they are stored in the next position, the new output bit is the next input bit directly. The XOR of Galois LFSR is done within the LFSR, and no XOR gates are run in serial, therefore the propagation times are reduced to that of one XOR rather than a whole chain, thus it is possible for each tap to be computed in parallel, increasing the speed of execution. In hardware level LFSRs are often implemented using this mode because it is more efficient and has less latency than the Fibonacci mode since the stages are updated at the same one clock time.

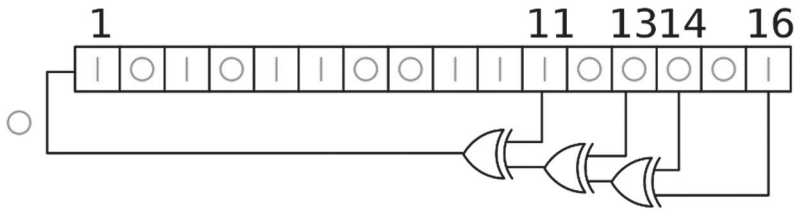


Figure 4.47: Structure of a 16-bit Fibonacci LFSR

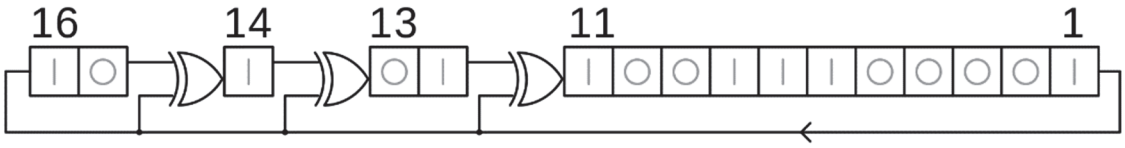


Figure 4.48: Structure of a 16-bit Galois LFSR

In theory, a M-bit LFSR can generate up to 2M non-repeating periodic sequences. If introduce a reset signal which is trigged at the Nth cycle, the register is reload at the beginning seed and repeats the loop operation, therefore a counter with a period of N is realized. We use this idea to design our frequency divider as shown in Figure 4.49.

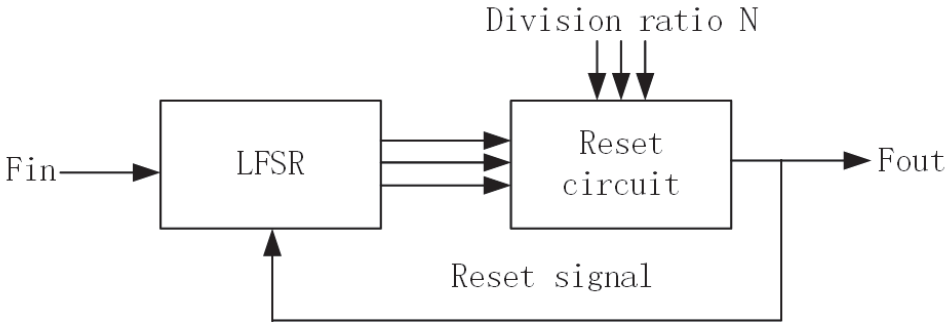


Figure 4.49: Frequency divider based on LFSR

Our design is based on a 15-bit Galois LFSR for example which could have a division radio from 1 up to 2^{15} (32768). The proposed frequency divider is composed by Galois LSFR and reset circuit. The output LFSR is a 15-bit random sequence. The random sequence means a sequence that is not in

numerical order, but a specific sequence determined by LFSR structure. The frequency division ratio N is converted into a corresponding N^{th} sequence by using the outside programmable module. When the two sequences match, the reset module outputs a reset signal reloading LFSR to the seed bit and produces an output signal frequency divided by N.

5.4. Design of LFSR based divider

Each bit of the LFSR can be replaced with a time delay block. The simulator NAPA is used to find out the structure of Galois LFSR [25]. Figure 4.50 shows the simplest 3-bit Galois LFSR which has one XOR gate to change state. A 15-bit LFSR can be implemented by simply extending 13 times the register between b2 and b1 to shift sequence (cf. Figure 4.51).

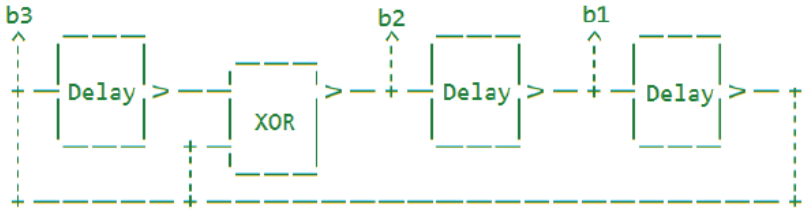


Figure 4.50: Structure of 3-bit Galois LFSR

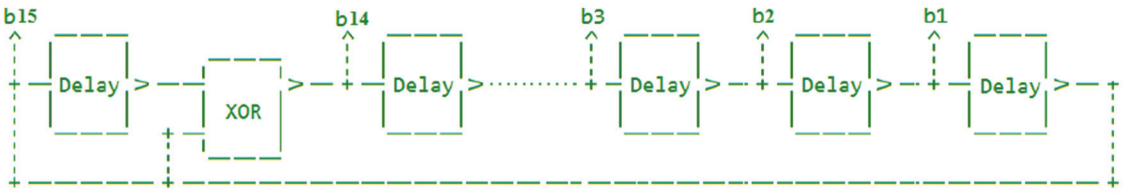


Figure 4.51: Structure of 15-bit Galois LFSR

For gate level implementation, the time delay block can be realized by 2 inverters and signal transmission is controlled by switches as shown in Figure 4.52. In fact, the two switches (SW1 and SW2) are controlled by two complementary clocks clk1 and clk2 which are the complementary outputs of VCO. As a result, after one rising edge of clk1, the input b(n+1) begins to be transmitted and arrives at the output bn after one cycle to finish one bit shifting.

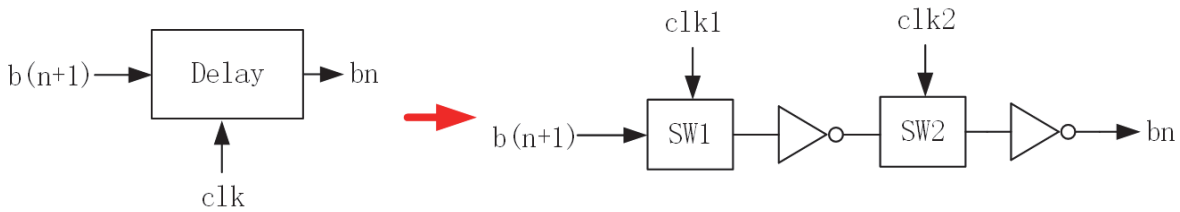


Figure 4.52: Gate level implementation for the time delay block

We should notice that our aim is to design a divider which could divide high-frequency signal by a specified frequency division ratio, so a reset signal should be added to restart this counter when required. The first inverter can be replaced with a NAND2 gate and introduce a reset signal to achieve this operation. When reset signal is triggered, the initial output value of each time delay block is 0. Otherwise, NAND2 with no triggered reset signal can be regarded as an inverter as before.

In addition, we hope that the proposed divider has a complimentary structure and thus it is compatible with other PLL building blocks. So, complementary inverter, complementary NAND2 and AO22 gates are introduced to replace inverter, NAND2 and XOR gates, whose structures are shown in chapter 2, section 4. Moreover, we use complementary switches for SW1 and SW2 which can be easily controlled by complementary clocks clk1 and clk2. Here, we only use the positive logic plane as examples to illustrate our design concept.

The 15-bit Galois LFSR with reset signal is shown in Figure 4.53. The structure consists of three blocks: Cell x is the block for delay and NXOR operations to change LFSR's state. This is the main difference with the Fibonacci, there is no complex multiple inputs gates at the exception of a 2 inputs XNOR efficiently implemented in complementary logic. Cell 1 is the time delay block as talk before. There are 13 blocks of cell 1 to form the register shifting. Cell 2 is the time delay block that lacks an inverter whose output can be regarded as a feedback for NXOR of Cell x. The reason for splitting the last time delay block into Cell 2 and an inverter is, in this configuration, there is only one logic gate between any two clocks. As a result, the overall delay of LFSR is determined by only a gate level delay, so this LFSR can work at a relatively high frequency. It is important to note that we will use the complementary logic without back-gate control as there is no need of specific synchronization between positive and negative planes in synchronous logic. The resulting circuit will therefore not be impacted by the heavy load represented by the back-gate and will therefore significantly faster that the back-gate controlled ring oscillator.

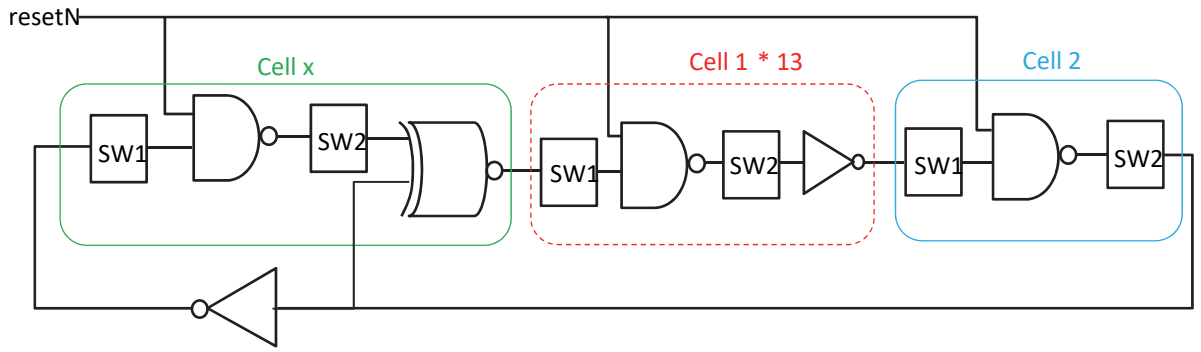


Figure 4.53: Gate level implementation of a 15-bit Galois LFSR with reset signal

For better performances, a buffer is added at each output stage of blocks and appropriate sizes are necessary for transistor implementation. We use the proposed sizing strategy (symmetrical output current and input capacitance) in chapter 2 (section 4) and choose the base sizes described in Table 2.4 as the unit size. The sizes of all gates are multiples of the unit size.

LFSR is a loop like RO, in which the input of each block is the output of the previous block. Each inverter of RO is charged with a load of the same size, this is the optimal solution. But there will be contradictions in the actual size setting for LFSR.

Figure 4.54 illustrates a size implementation example for 4-bit LFSR. We set the size of buffer and Cell x as the unit size (1). The feedback inverter in blue is charged by two gates buffer and NAND2 with unite size, so the size of this inverter is set to twice of the unit size (2). Then, the size of NAND2 in green is set to three times the unit size (3), because it is charged by an inverter of twice the unit size and a XNOR gate of the unit size. We repeat the same process until meeting with the first Cell x. At the red point, the NXOR gate of unit size is charged by a buffer of unit size and a NAND gate of five times unit size. Compared to the load capacity of previous block, this six-time larger load causes the whole system of LFSR to slow down.

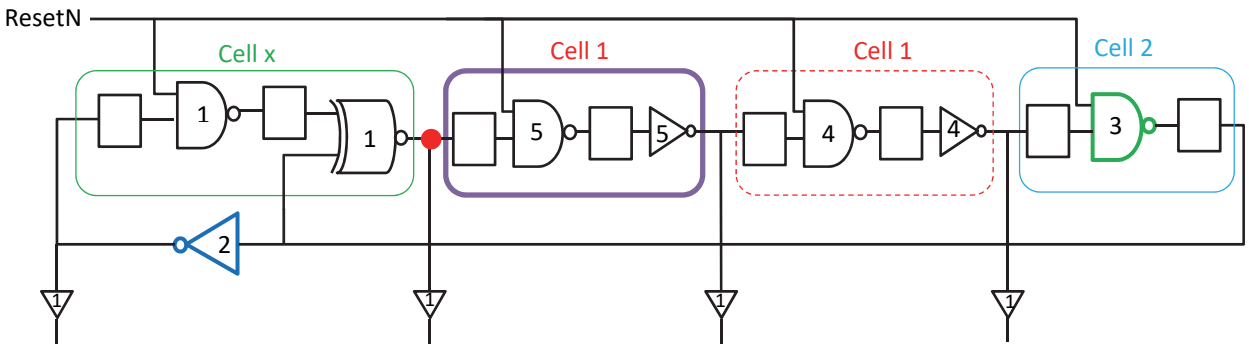


Figure 4.54: Contradiction of size implementation

As perfect match with the proposed sizing strategy for all transistors is impossible theoretically, we made some compromises in size. That is, the size of load for each stage is slightly larger than the size of the previous stage, and size increase rate of each stage maintains the same ratio. The specific method of size implementation is as follows.

In each time delay block, input gate is marked as ‘a’ and output gate is marked as ‘b’, following a number in order as shown in Figure 4.55.

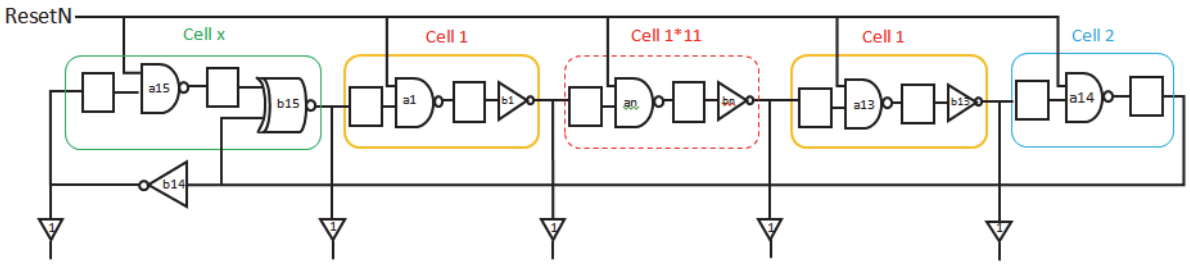


Figure 4.55: Size implementation strategy of a 15-bit Galois LFSR

For Cell x and Cell 2, we have the related equations:

$$\frac{a15}{b15} = \frac{b14}{a15+1} \tag{4.8}$$

$$\frac{b14}{a15+1} = \frac{a14}{b14+b15} \tag{4.9}$$

$$\frac{a14}{b14+b15} = \frac{b13}{a14+1} \tag{4.10}$$

With a15 and b15 as initial values, we can deduce,

$$b14 = \frac{a15(a15+1)}{b15} \tag{4.11}$$

$$a14 = \frac{b14(b14+b15)}{a15+1} \tag{4.12}$$

$$b13 = \frac{a14(a14+1)}{b14+b15} \tag{4.13}$$

Then, other values of the same cell 1 until a1 and b1 can be expressed by the same formula:

$$an = \frac{bn^2}{a(n+1)+1} \text{ with n=1, … 13} \tag{4.14}$$

$$b(n-1) = \frac{an(an+1)}{bn} \text{ with n=2, … 13} \tag{4.15}$$

a15 and b15, that are set to the initial value can be also expressed with a1 and b1:

$$a15 = \frac{b15^2}{a1+1} \tag{4.16}$$

$$b15 = \frac{a1(a1+1)}{b1} \tag{4.17}$$

After the relationship between each gate is determined, we can give a15 and b15 initial values and use the iterative method to obtain the output values of a15 and b15 through a loop.

Table 4.2 describes the iterative results of a 15-bit LFSR. Through iteration, the resulting output value of a15 is 4.51, b15=5.01 which are almost the same as the initial value.

Table 4.2: 15-bit LSFR iteration

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1
5	4.95	8.96	8.16	7.51	6.98	6.55	6.21	5.93	5.7	5.52	5.37	5.25	5.15	5.07
a15	a14	a13	a12	a11	a10	a9	a8	a7	a6	a5	a4	a3	a2	a1
4.5	8.96	8.06	7.34	6.76	6.28	5.9	5.59	5.34	5.13	4.97	4.83	4.73	4.64	4.57

For simplicity, we use 5 stages for iteration (cf. Table 4.2) and the result doesn't have much impact. Using 11 times the value of a3 and b3, we have finally determined the appropriate and simplified size of 15-bit Galois LFSR as shown in Figure 4.56.

Table 4.3: 5-bit LSFR iteration

b5	b4	b3	b2	b1
4.0	3.5	5.9	4.8	4.0
a5	a4	a3	a2	a1
3.3	6.2	4.8	3.9	3.3

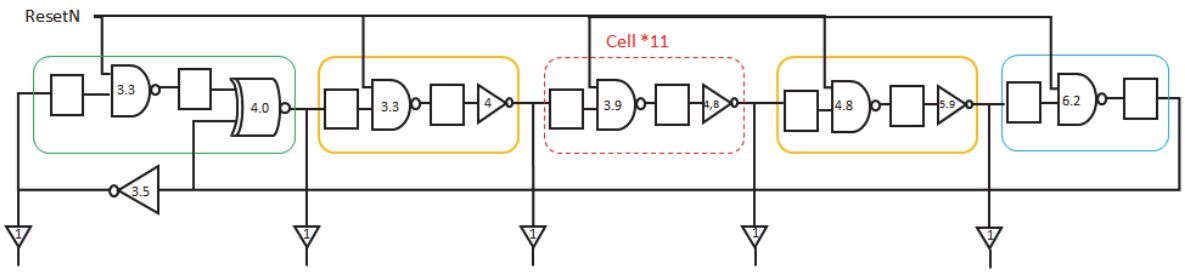


Figure 4.56: Simplified size implementation of a 15-bit Galois LFSR

The reset circuit consists of six stages of logic gates controlled by clk1 and clk2 as shown in Figure 4.57. For the proposed 15-bit LFSR, division ratio N is converted by the external compiling circuit into a 15-bit comparison signal a15…a1.

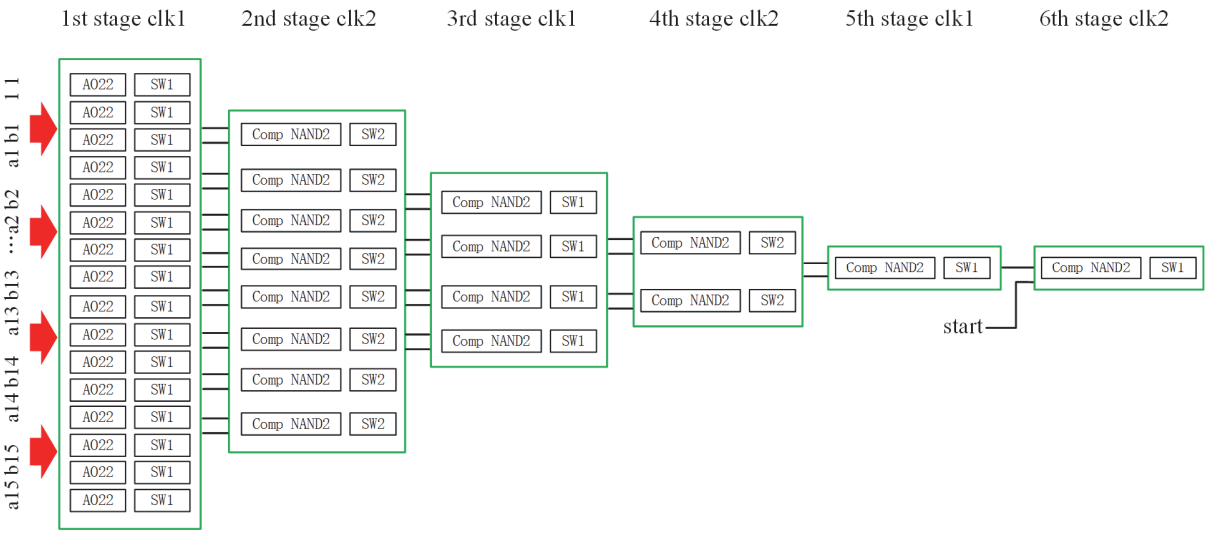


Figure 4.57: Gate level implementation of reset circuit

The working principle of reset circuit is explained as follows (always use positive logic plane to illustrate):

When the output of a certain bit of LFSR is the same as the corresponding comparison signal, whether 0 or 1, AO22 gate will output a high level '1', indicating that this bit is matched. The first stage is composed of 16 AO22 gates, so one of them is configured to always output '1'. When two adjacent AO22 gates have '1' at output, NAND2 gate of the second stage will output a high level '1'. Thank for complementary logic structure, we can always get high level '1' at output of each stage when the two inputs match. By comparing the output signals stage by stage, the output number is reduced by the power of 2. If any of the 15-bit for LFSR and comparison signal are matched, the fifth stage will output a high level '1'. In addition, we introduce a detect enable signal 'start' and when start=1, the circuit begins to detect the matching state of inputs.

In summary, when the reset circuit is in working operation, positive logic plane will get a high level '1' only if the LFSR counts the given division ratio. It should be noted that the reset circuit is controlled by six stage of clocks, or, three complementary clocks. That means there are two extra delays in reset circuit. If we want to achieve N frequency division, the input division ratio should be set to N-2. The size of reset circuit is computed in the same way as LFSR and will not be described in detail here.

5.5. Simulation and discussion

First, we use the coefficients proposed in reference papers like [26], and according to the input and output relationship of each blocks, we have built the 15-bit LFSR code in Annex 2, where the initial input value for each block is set to 0. The corresponding NAPA [7] simulation result is shown in Figure 4.58.

We can observe the initial output sequence for b15…b1 is 010000000000000. The initial bit b14 is '1' because there is a XOR gate between b14 is the output of XOR gate where the two inputs b15 and b1 are '0' (b15 XOR b1=0 XOR 0=1). During counting, the system performs a shift operation from b13 b12…b1 until b15, except b14 is the output of XOR of b1 and b15, therefore realizing the loop operation of the LFSR. This can be observed at the green arrow, when '1' from b14 is shifted until b1, b14 will output '0' (b15 XOR b1= 0 XOR 1=1) at the next cycle, at this time, b15 receives '1' shifted from b1, and then b14 will output '1' again after the next cycle, but '0' produced by XOR gate will continue to shift. In addition, the next occurrence of the initial sequence is at the 32768 cycle (32783-15+1=32768 in red circle), which satisfies the expected maximum cycle 2^{15} of 15-bit LFSR.

	y	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1
16	8192	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
17	12288	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
18	14336	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
19	15360	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
20	15872	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
21	16128	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
22	16256	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0
23	16320	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0
24	16352	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0
25	16368	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0
26	16376	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0
27	16380	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0
28	16382	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0
29	16383	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
30	24575	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
31	28671	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
32	30719	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
33	31743	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
32780	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
32781	16384	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32782	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
32783	8192	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
32784	12288	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
32785	14336	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Figure 4.58: Simulated truth for the proposed 15-bit Galois LFSR

After the verification of this LFSR, we have implemented the proposed 15-bit Galois LFSR divider in complementary logic and run some transient simulations. The voltage supply is 1V, with typical conditions of process and temperature in 28nm FDSOI technology as before.

Figure 4.59 confirms the symmetry of the complementary outputs by LFSR. So, we can use only positive logic plane to verify the functionality of system.

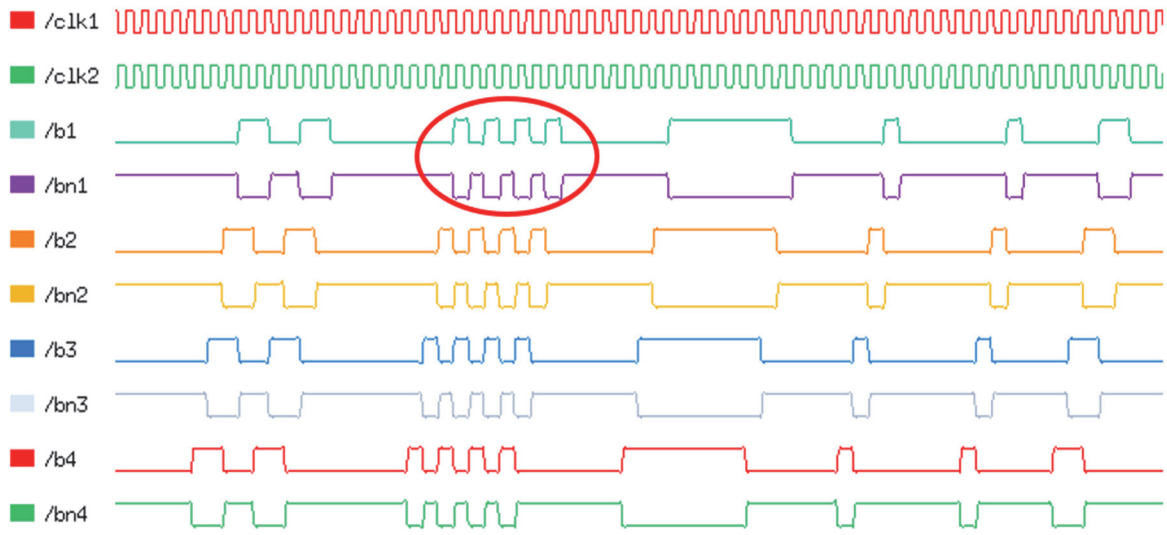


Figure 4.59: Verification of LFSR symmetry

Figure 4.60 shows a transient simulation of the LFSR with a clock frequency of 20GHz. When reset signal is '1', LFSR is in reset state, where the initial output sequence for b15…b1 is 010000000000000. Once LFSR leaves reset state (in red arrow) and when clk1 is on the rising edge, output sequence will therefore turn to the next state 011000000000000. Then output sequence will

turn to the state 011100000000000 after the next rising edge of clk1. The overall trend of transition state is based on b14 which is the output of XOR gate and shift to the adjacent following bit. By comparison, the simulated results match well with the simulated truth table therefore we have verified the functionality of LFSR circuit. Since we have configured the appropriate size, the proposed LFSR can operate at a high frequency up to 25 GHz.

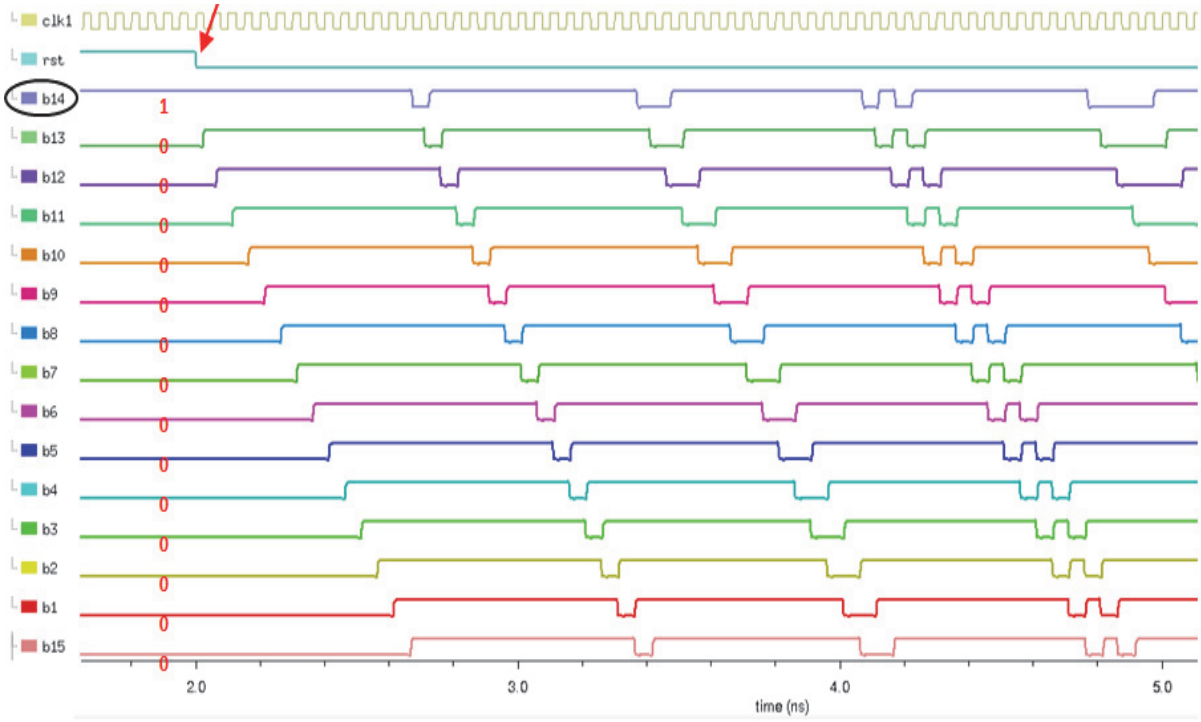


Figure 4.60: Transient simulation for LFSR at 20GHz

Then we launched other simulations for the whole frequency divider consist of LFSR and reset circuit. Taking division ratio N is 8 for example, as talked before, two extra delays are introduced in reset circuit, so the input ratio should be set to 6. According to the simulated truth table, the comparison signal a15…a1 should be set to 011111100000000.

The simulated results are shown in Figure 4.61. When the detect enable signal 'start' is '0', the divider is always in a quiescent sequence of 010000000000000 which means the LFSR is in reset mode. Once 'start' turns to 1 and when clk1 is on the rising edge (in red arrow), the reset signal changes to 0, LFSR begins to count in its sequence and detect the comparison sequence. When it is detected that LFSR output sequence at a certain time matches with the comparison sequence 011111100000000, reset signal will turn to '1' after two delays. At this moment, LFSR is rest to the initial sequence, then restarts counting and creates a loop of 8.

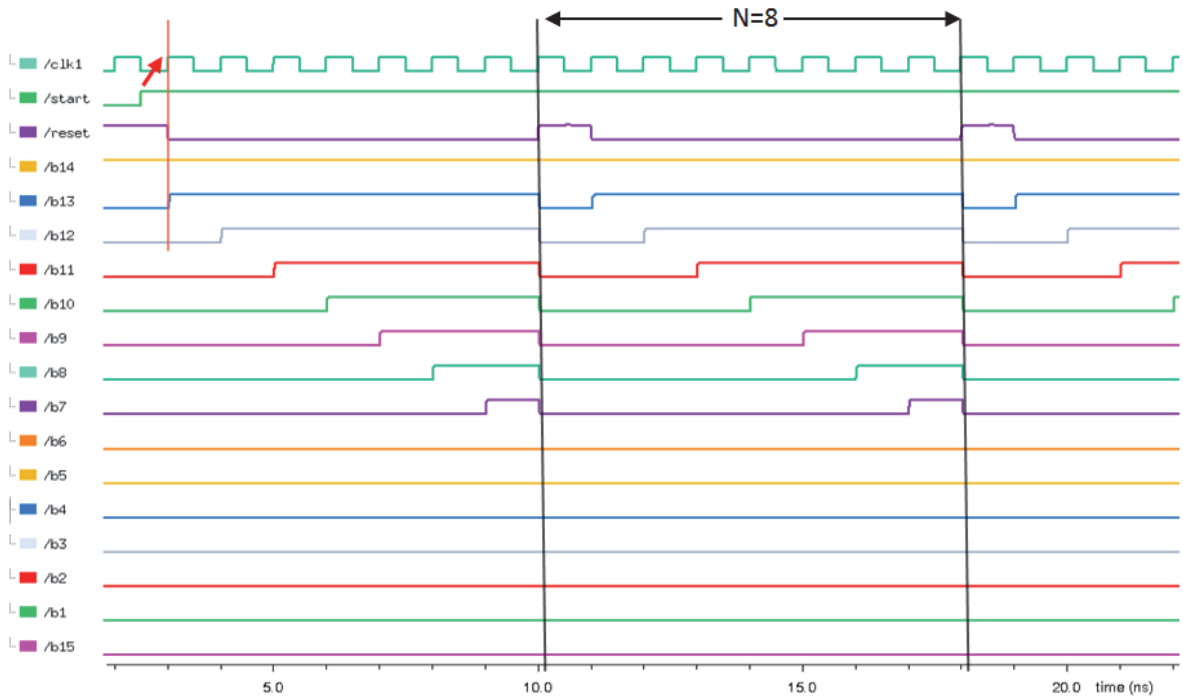


Figure 4.61: Transient simulation for divider with rand division of 8

The proposed divider has a minimum division ratio of 4. Because when the comparison input sequence is the initial sequence, LFSR is in reset mode and cannot count. LFSR starts counting only when the reset circuit detects the second sequence. Together with the extra two delay, the reset signal is therefore triggered every four cycles to form a loop. The simulated result is verified and presented in Figure 4.62.

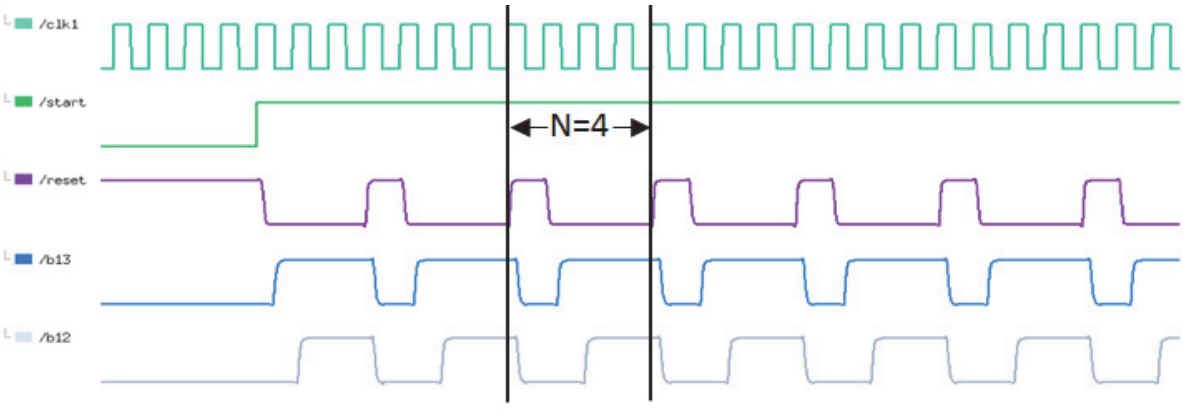


Figure 4.62: Transient simulation for divider with minimum rand division of 4

5.6. Conclusion

In this section, we proposed a high-speed frequency divider without prescaler. This divider consists of 15-bit Galois LFSR and corresponding reset circuit. The whole divider can work at a high frequency up to 15GHz and can achieve any division ratio from 4 up to 2^{15} (32768). As divider mainly

consumes during clock transition, power consumption is related to clock frequency. The simulated results show under 1V power supply, the divider consumes 5.4mW at 1GHz and 15.6mW at 10GHz, of which LFSR consumes 2.5mW at 1GHz and 7.8mW at 10GHz. In terms of low power design, the transmission speed will slow down as decreasing the power supply, which limits the maximum operation frequency. The proposed divider can work down to 0.6V power supply with 1.9mW consumption at its maximum 2GHz.

6. PLL behavioral level simulation

All the building blocks of PLL related to transistors having been designed and simulated before, we can make a behavioral simulation to study the complete DPLL. Figure 4.63 illustrates the block diagram for DPLL. All the other building blocks have been studied, there left a loop filter LPF that needs structural design and parameter setting.

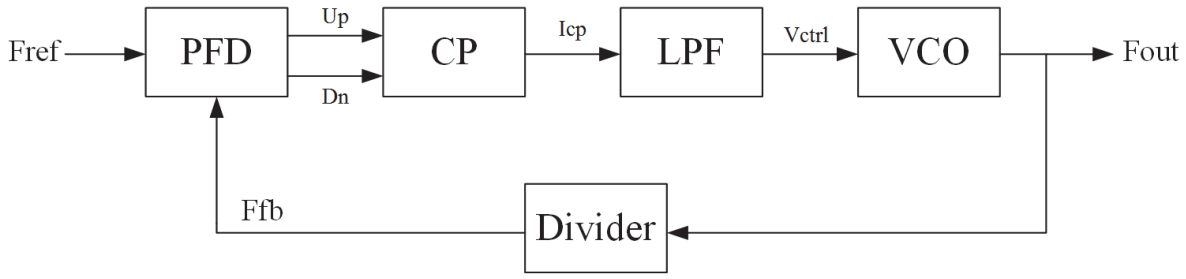


Figure 4.63: Block diagram of the DPLL

The filtering characteristics of the loop filter determine the whole PLL loop performance. The function of loop filter is to remove high frequency noise from the output of PFD and CP, influence the hold and captures ranges, as well as influence the switching speed of the loop in lock [27]. Usually the loop filter is a low-pass filter (LPF) easily implemented by passives capacitors and resistors, there are other types of loop filter such as active op-amp filters, digital filters etc. can also be used. Here we use a second-order LPF for behavioral level simulation of PLL. Second-order LPF is used to form the type-II PLL which has infinite DC forward loop gain, theoretically achieves a zero phase difference between reference and feedback signals [28].

Figure 4.64 illustrates a typical second-order loop filter. The capacitor C1 can filter out high frequency noise and voltage fluctuations. Series resistor R2 and capacitor C2 introduce a zero in the loop which increases phase margin and therefore increases the system stability. The parameters of filter can be obtained from online loop filter calculator [29]. To achieve a PLL with a 45° phase margin

and a filter bandwidth of 80MHz, we have C1=10pF, C2=3pF and R2=7.597kΩ. The calculated loop bandwidth is 7.2GHz which satisfies our design requirements.

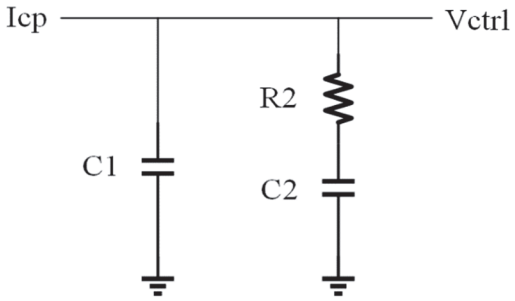


Figure 4.64: Second order loop filter

Now having all the key parameters for DPLL such as the delay of PFD, output current of CP, loop filter parameters, frequency characteristic of VCO etc., we made a synthesis simulation to study the behavioral level of this DPLL in simulator NAPA [25]. We have built the DPLL code in Annex 3 which contains the specifications of each PLL building blocks.

We have chosen for example M=6 and N=5 for the frequency divider factors of the input reference signal (Fref) and output signal (Fout). For input signal, we chose a suitable periodic signal with different frequencies at different times. In this example, the divided reference signal and feedback signal work between 0.5 and 1GHz, which is also the operation frequency of PFD.

The time domain simulation is shown in Figure 4.65. The simulated result shows that the output signal in green can follow the input signal in purple correctly. Especially, when signal frequency jumps up from 4GHz to 6GHz at 1.5µs or jumps down from 6GHz to 3GHz at 6µs suddenly like a step signal, the output can follow the input with a moderate delay and tolerated transitions.

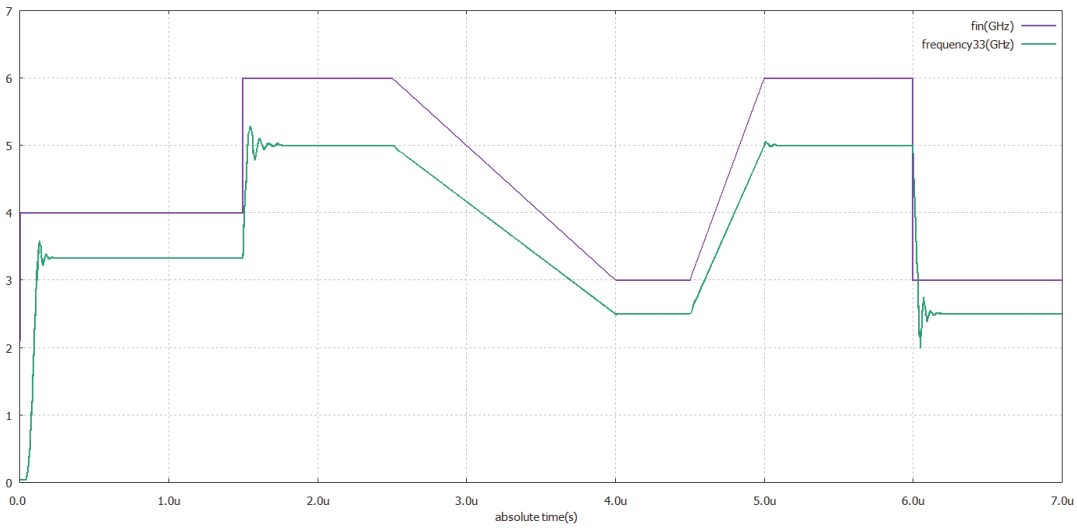


Figure 4.65: PLL behavioral level simulation

Obviously, silicon implementation and measurement results are mandatory to verify the functionality of the proposed DPLL. Behavior level simulation is still important to help us better understand the entire PLL system and optimize the parameters of each building block. Our main research direction during the Ph.D. study is the circuit design and simulation for PLL building blocks, subsequent we will make more detailed behavior level simulations for PLL according to the specifications.

7. Conclusion

In this chapter, we have proposed all the building blocks of DPLL based on complementary structure. All these building blocks are implemented in 28nm UTBB-FDSOI technology and verified by SPICE simulation under 1V power supply.

The first main block VCO is composed by a four-stage quadrature ring oscillator presented in the previous chapter and the current mirror with back-gate control structure. The input current is converted from input voltage by NMOS transistor and is transformed by current mirror which controls the ring oscillator. The small-size back-gate controlled current mirror can reduce small channel effect and therefore provide high impedance output. The proposed VCRO can output four-phase quadrature signals because of the ring oscillator and is followed by a level shifter to make it compatible with other blocks. It has a wide input range from 0.2V to 1.0V and it operates almost linearly in two parts which offers a slope of KVCO = 19GHz/V and 2GHz/V respectively.

PFD can detect both the phase and frequency difference between reference and feedback signals. We proposed a complementary PFD in which each module has three stages and only nine transistors to greatly reduce time delay. Moreover, there is no reset routing path so it can overcome dead zone problem. The minimum delay between inputs and outputs is only 16ps, which determines working frequency up to several GHz.

Then we proposed a new structure of charge pump composed by pull-up and pull-down network with back-gate controlled current mirror. The switch of charge pump is controlled by complementary signals from output of PFD that makes CP input more accurate. Because of the back-gate controlled current mirror, this CP has a larger linear output range. The proposed charge pump can work with a small mismatch at frequency up to 2GHz and the output don’t exhibit any spurious jump phenomenon.

Next, we proposed a high-speed frequency divider without prescaler. Our design is based on a 15-bit Galois LFSR which has a division radio from 1 up to 2^{15} (32768). The proposed frequency divider is composed by this LSFR and its corresponding reset circuit. The whole divider can work at a high frequency up to 15GHz and can achieve any division ratio from 4 up to 32768.

All these building blocks above are implemented in 28nm UTBB-FDSOI technology and verified by SPICE simulation under 1V power supply.

The total consumption of PLL can be estimated by summing the consumption of each building block: VCRO: 24mW maximum, PFD: 10µW, CP: 72µW, Divider: 5.4mW at 1GHz and 15.6mW at 10GHz.

In terms of low power design, all the blocks of PFD, CP and divider can operate at a relatively low power supply down to 0.6V, but at the cost of reducing the operating frequency range. This is not an issue as for lower supply voltages the frequency of ring oscillator will be reduced. We only need to adjust the power supply of level shifter to be compatible with all the other building blocks.

Finally, we introduced a second-order loop filter and made a synthesis simulation to show the result for the behavioral level of the final DPLL. Next and final step is to validate all these results by measurements on a test chip.

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Chapter V – Test chip and measurements

1. Introduction

In this chapter, we will present the layout design of the test chip, in particularly the RO. In fact, this RO is based on the new topology of the complementary inverter in order to have a very good symmetry of the outputs. To keep this feature, the layout has been studied with specific care on the symmetries between each inverter, but also on global symmetry regarding RO outputs using common centroid design. We have implemented on the same test chip different circuits such as only an inverter, a chain of inverters, a current mirror (with and without back-gate control), a ring oscillator and a VCRO including level shifters and buffers. The test chip was realized in 28nm FDSOI technology and the measurements are compared with simulations and validate our concept of BG cross-coupling.

2. Common-centroid layout

In section 2.2 of chapter 2, we presented the “nfettw” and “lvtpfettw” transistors from STMicroelectronics' UTBB-FDSOI 28nm library chosen for our design. From Figure 5.1 we can see that having a triple-well structure, both PMOS and NMOS used for the complementary inverter can be built in the same P well. As a result, it could simplify the layout for complementary inverter without short circuit in the substrate area.

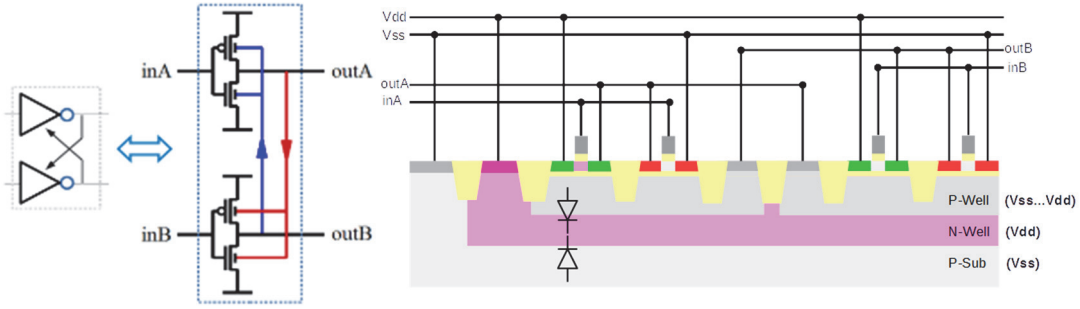


Figure 5.1: Schematic and layout structure of complementary inverter in UTBB-FDSOI technology

However, the proposed ring oscillator is composed by four identical complementary inverters. In order to make the RO works at its best, all inverters should be as identical as possible to reduce the mismatch and then keep the symmetry of output signals.

For example, as shown in Figure 5.2, the shadowed region is caused by the gate polysilicon during the source /drain implantation because the implant is tilted by about 7° to avoid channeling. As a result, a narrow strip in the source or drain region receives less implantation, creating a small asymmetry between the source and drain side diffusions after the implanted areas are annealed [1]. If there are two or more transistors with the same size placed in improper position, these transistors will be asymmetry due to the shadowing.

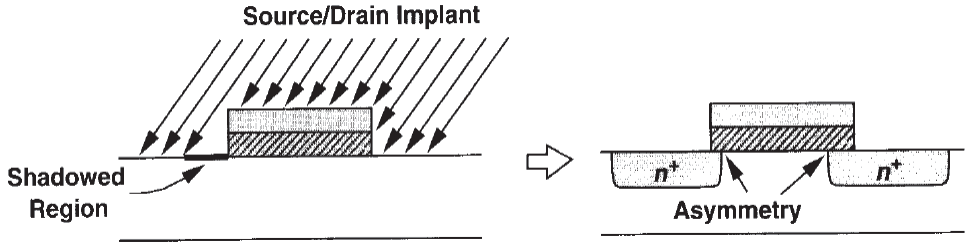


Figure 5.2: Shadowing due to implant tilt [1]

What's more, there are always gradient errors due to process variations on the produced chip. For example, uneven temperature can cause slight differences between two left and right placed transistors resulting in mismatch.

The best solution is to use the 'common-centroid' concept in layout. As illustrated in Figure 5.3, both transistor M1 and M2 are separated into two halves and placed diagonally opposite to each other and connected in parallel. In this way, the linear gradient errors from any direction can be compensated.

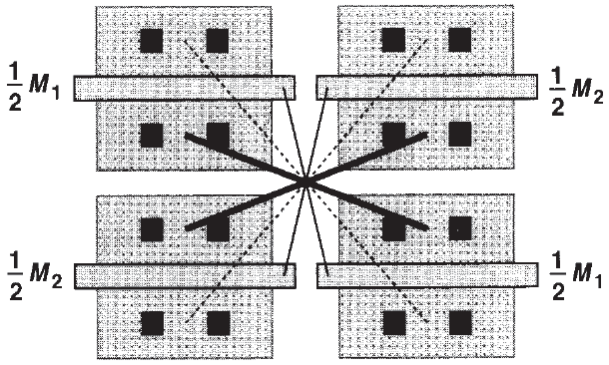


Figure 5.3: Common-centroid layout [1]

In our ring oscillator composed by four identical complementary inverters, matching accuracy plays a key role in the performance. We should ensure that not only the two inverters that make up any complementary inverter have the smallest mismatch, but also the mismatch of the four complementary inverters is minimized.

Figure 5.4 illustrates the layout strategy for reducing mismatch of parameters for four matching-critical complementary inverters when linear gradients errors are present [2]. In this strategy each complementary inverter is divided into four small blocks of the same size and the ring oscillator is reconstituted in center-symmetric pattern to assure the symmetrical gravity of each complementary inverter is at center. As a result, whatever the variation direction is, all can be compensated.

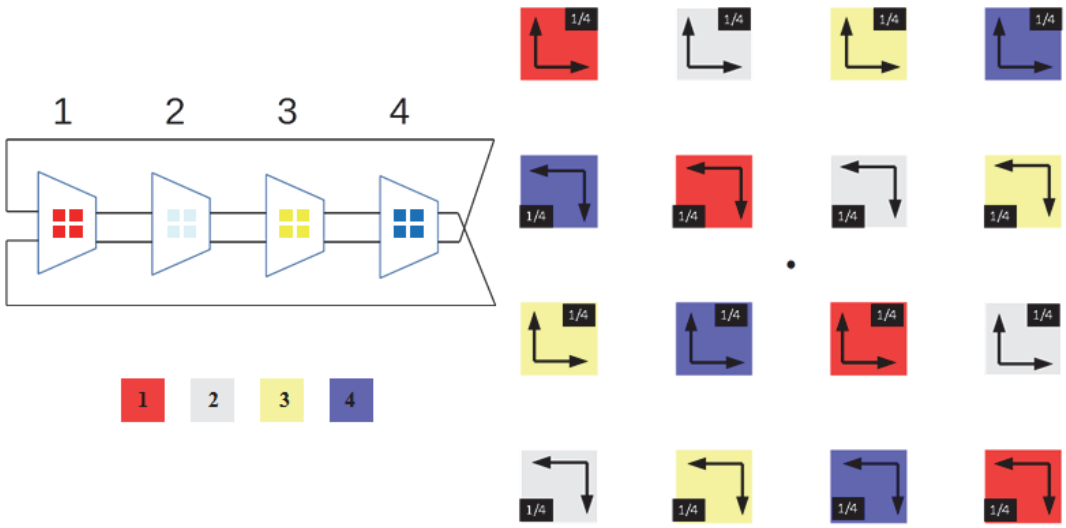


Figure 5.4: Common-centroid design of the RO

In addition, the small cells should be connected to minimize the parasite capacitors and resistors as much as possible as shown in Figure 5.5.

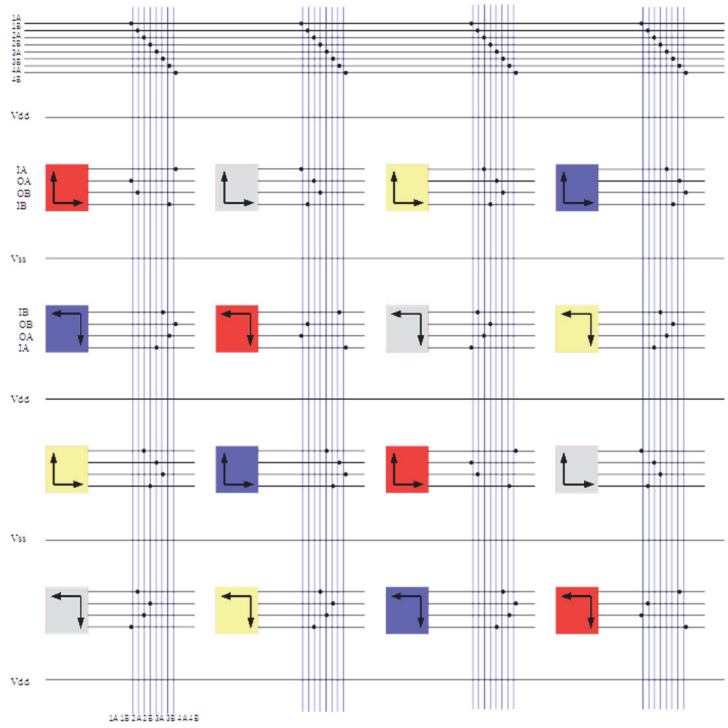


Figure 5.5: Interconnection for a common-centroid placed ring oscillator

Using this design, all the interconnections between each inverter have the same length, so introduce the same delay and finally keep the symmetry of the signals.

3. Layout design

3.1. Overview of the ROSCOE test chip

In fact, we have implemented a complementary inverter, a chain of complementary inverters, a current mirror (with and without back-gate control), a ring oscillator and a voltage-controlled ring oscillator on the same test chip as shown in Figure 5.6. This figure also illustrates the Pad ring of this test chip: power supply and I/O pins.

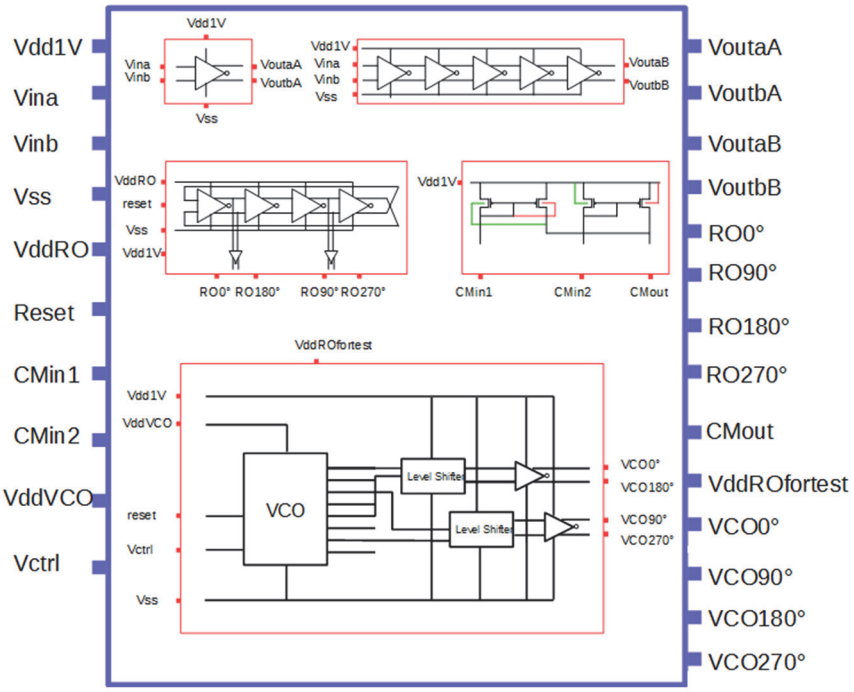


Figure 5.6: Building blocks of the test chip and pin names

Table 5.1 gives the type of all the input and output pins for correct measurements. The VddROfortest pin of the VCRO is both the output of current mirror and input of ring oscillator. We can measure the bias voltage for RO in VCRO and can also provide the voltage for the RO via this port, in order to control its frequency oscillation.

We also notice that the type of output ports for RO and VCRO are 50Ω AC port. Because we will test the function of RO and VCRO in high frequency, impedance matching is a must. As shown in Figure 5.7, complementary inverters are used to implement output buffers. The value to get 50Ω buffers is obtained with Wp/Lp=22.75um/30nm and Wn/Ln=17.5um/39nm transistors size

respectively. Because complementary inverter has two complementary outputs, we don't need two inverters in series to get the correct sign, only need to cross the output.

Table 5.1: Power supply and I/O pins description

	Power	Type	**Input**	Type	**Output**	Type	**Input/Output**	Type
Complementary inverter	Vdd1V	DC	Vina	DC	VoutaA	DC		
	Vss	DC	Vinb	DC	VoutabA	DC		
Chaine of complementary inverters	Vdd1V	DC	Vina	DC	VoutaB	DC		
	Vss	DC	Vinb	DC	VoutabB	DC		
Current mirror	Vdd1V	DC	CMin1	DC	CMout	DC		
	Vss	DC	CMin2	DC				
Ring oscillator	Vdd1V	DC	RESET	DC	RO0°	50Ω		
	VddRO	DC			RO90°	50Ω		
	Vss	DC			RO180°	50Ω		
					RO270°	50Ω		
Voltage controlled ring oscillator	Vdd1V	DC	RESET	DC	VCO0°	50Ω	VddROfortest	DC
	VddRO	DC	Vctrl	DC	VCO90°	50Ω		
	Vss	DC			VCO180°	50Ω		
					VCO270°	50Ω		

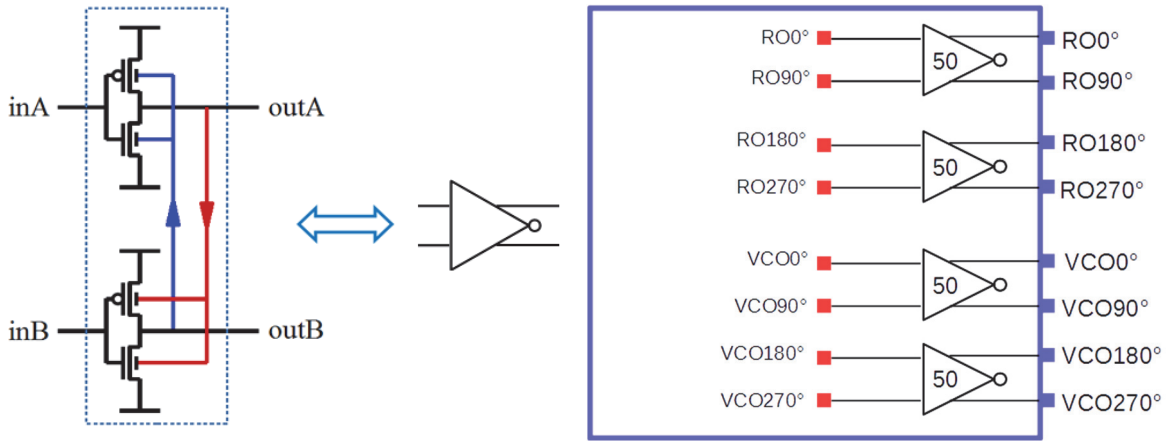
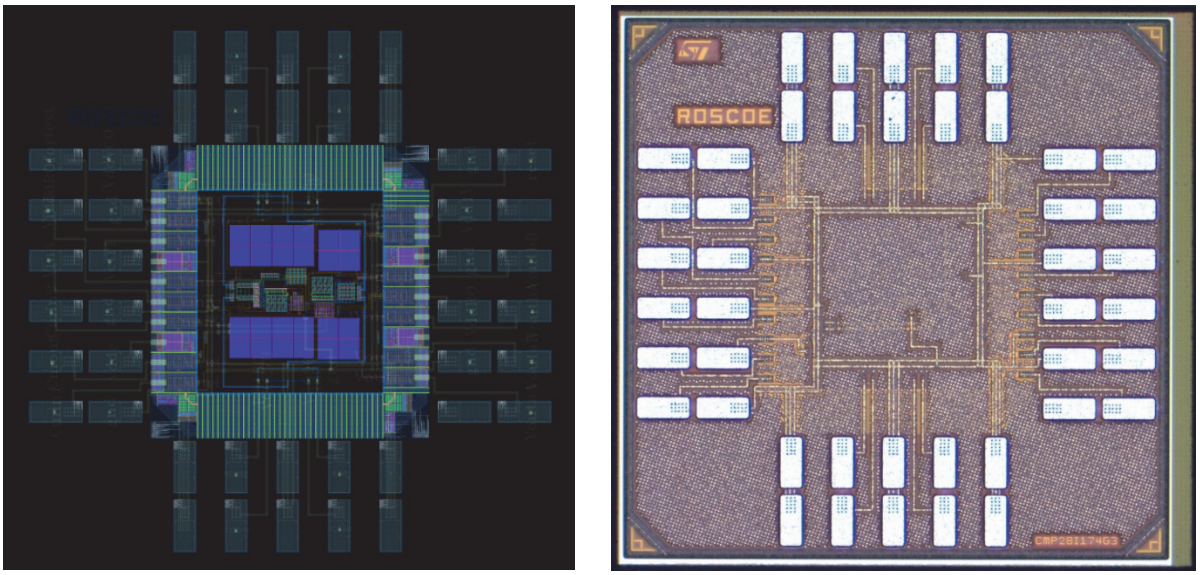


Figure 5.7: 50Ω output buffer implemented with complementary inverter

The ROSCOE (Ring Oscillator Soi COmplEmentary) test chip was implemented in 28nm FDSOI technology and realized with the help of CEA-LETI, CMP and STM. Figure 5.8 presents the final layout (a) and a picture of the die (b) with the pad ring. The total area is about 600*600µm² and the pitch between two pads is equal to 90µm (i.e. 100µm with a shrinking factor of 90%).



(a) Layout (b) Micrograph

Figure 5.8: ROSCOE test chip

DC probes and GSG probes are needed for power supply and measurements, as shown in Figure 5.9. Some sizes of the chip are also given.

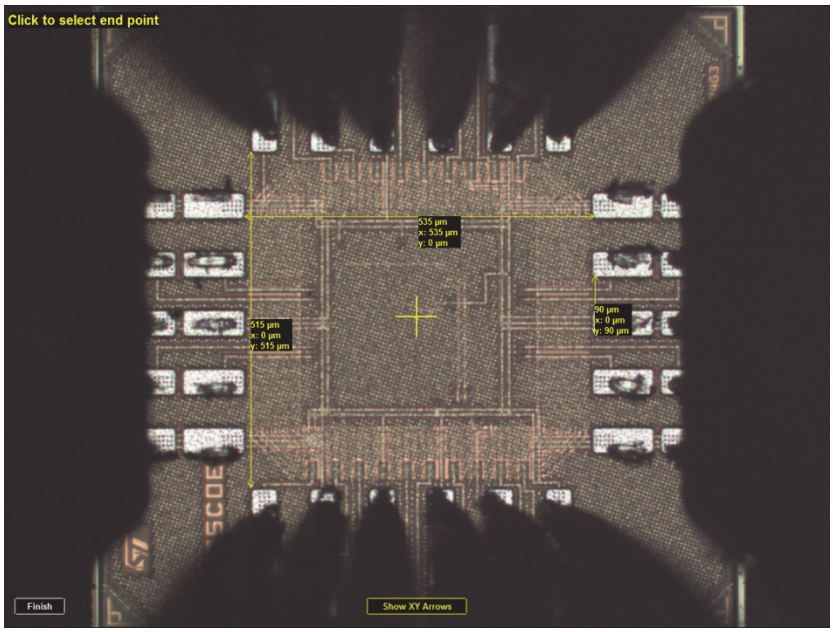


Figure 5.9: ROSCOE test chip under test with DC and GSG probes

3.2. Layout implementation for each block

In this section, we present the design of layout implementation for the complementary inverter (cf. Figure 5.10), chain of 5 complementary inverters (cf. Figure 5.11), current mirror (cf. Figure 5.12), ring oscillator (cf. Figure 5.13) and voltage-controlled ring oscillator (cf. Figure 5.14) respectively.

From the figure 5.10, we can see that four quarter-size complementary inverter form the complementary inverter of required size (PMOS: 9.1um/30nm, NMOS: 7um/39um). The chain of complementary inverters is made up of five complementary inverters connected in series.

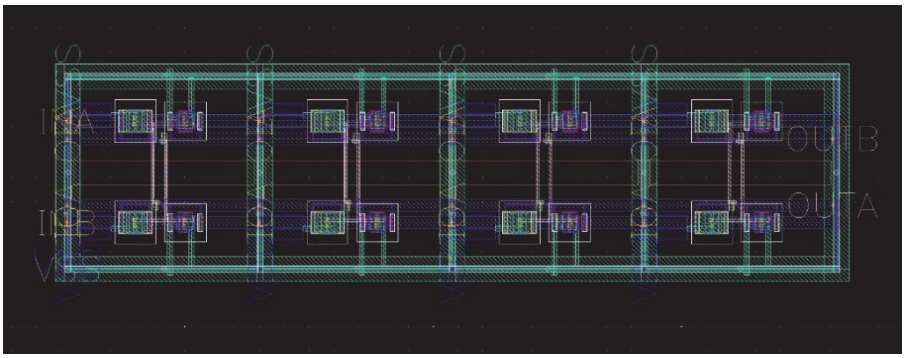


Figure 5.10: Layout of complementary inverter (30*8μm²)

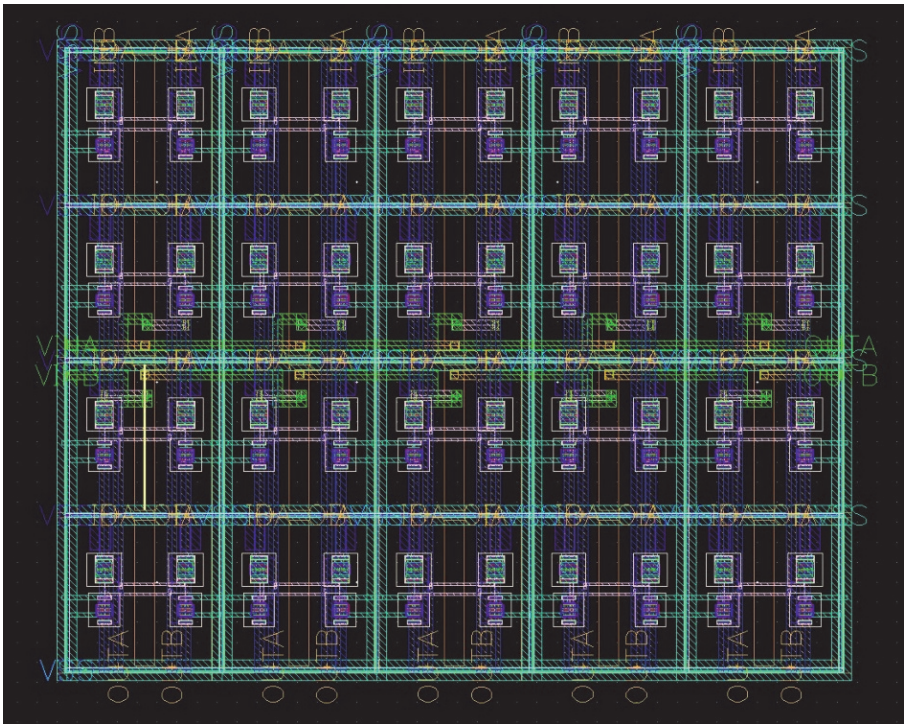


Figure 5.11: Layout of a chain of 5 complementary inverters (40*30μm²)

While in ring oscillator, the complementary inverters follow common-centroid conception described in section 5.1. There are four pairs of matched NMOS transistor for reset which are placed axisymmetrically like ABCDDCBA.

The VCRO is composed of well-placed current mirror, ring oscillator, level shifter and output inverter.

All the circuits are placed very regular and the connection lines are also symmetrical in order to minimize the mismatch, parasite capacitors and resistors as much as possible.

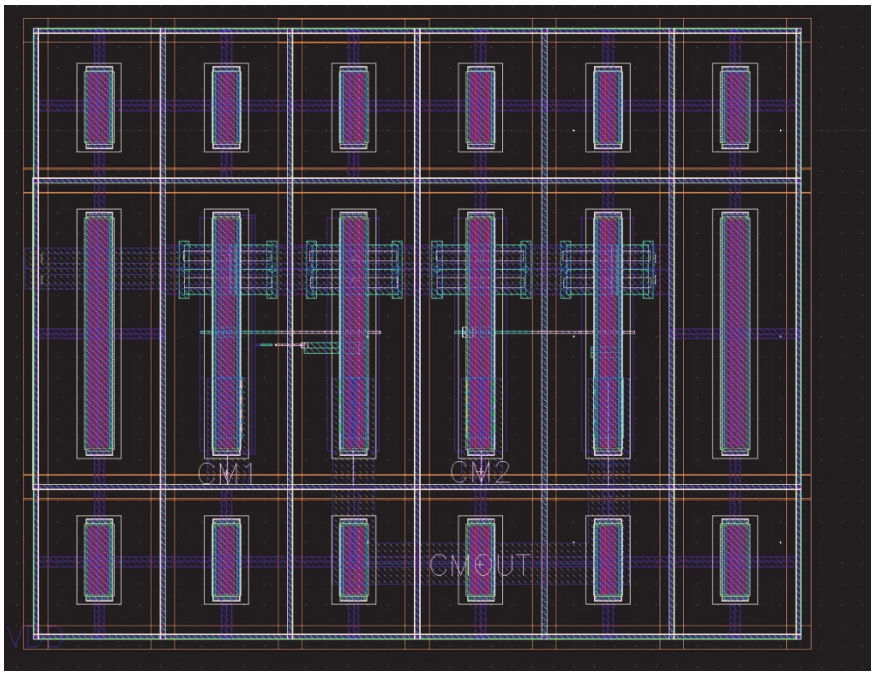


Figure 5.12: Layout of current mirror (40*30µm²)

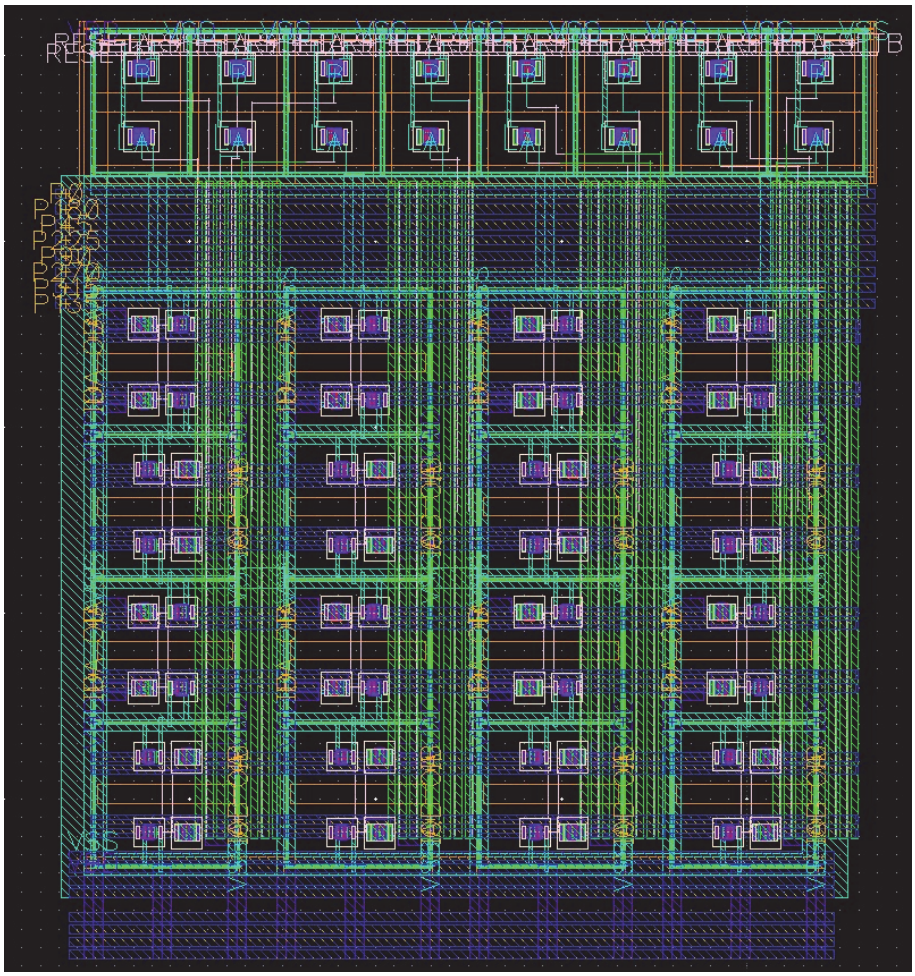


Figure 5.13: Layout of a chain of ring oscillator (60*40µm²)

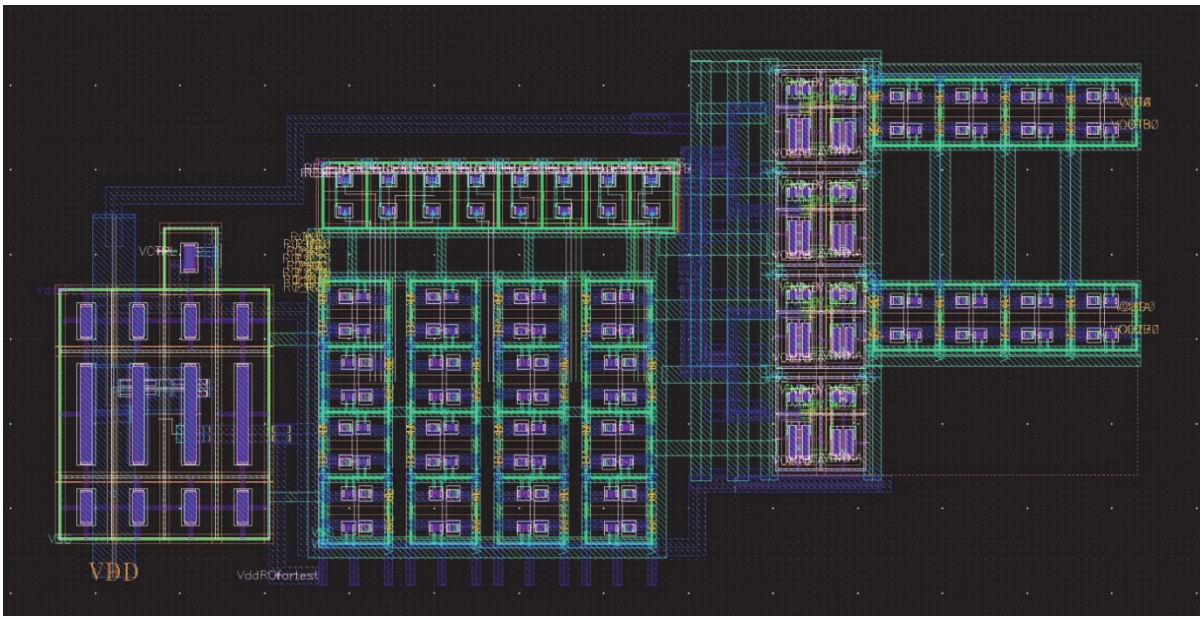


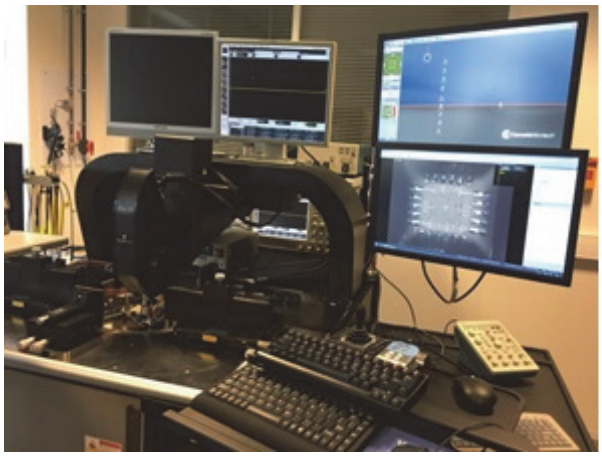
Figure 5.14: Final layout of the VCRO including level shifters and buffers (130*60µm²)

From left to right in Figure 5.14, we can observe first the current mirror (cf. Figure 5.12) with and without the back-gate control technique (only the output transistor with BG control is connected to the RO), then the ring oscillator (cf. Figure 5.13) cascaded to the level shifters and the 50Ω buffers on the right. The latter two will therefore not be tested separately.

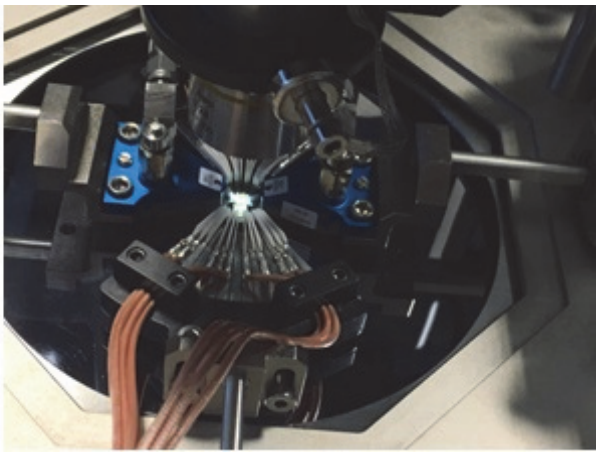
4. Measurements and discussion

4.1. Measurement test bench

All the measurements are realized with the CEA-LETI microprobe tester, as depicted in Figure 5.15 (a) with a zoom of the test chip and the probes (cf. Figure 5.15 (b)).



(a) Test bench



(b) Zoom on chip and probes

Figure 5.15: Probe tester

In the following sections, each block, starting with the complementary inverter, is measured and compared with simulation. Due to unexplained differences, simulations were redone using the 28nm FDSOI Design kit of the CEA-LETI and taking into account interconnections (i.e. post-layout simulation).

4.2. Complementary inverter

To realize the DC transfer function measurement of the complementary inverter, we have preferred to use directly the chain of 5 complementary inverters to improve the symmetry of the complementary output signals. Despite this, a very strong dissymmetry was observed at the output of the inverter chain. In fact, the output signals do not cross at Vdd/2=500mV (as expected by simulation: cf. Figure 2.18), but at a much lower value. This asymmetry is due to the extra voltage loss on Pads and wires. Although the supply voltage Vdd is 1V, the output signal can only vary from 10mV to 940mV. So, the midpoint of the signal crossing is no longer 0.5V. To overcome this problem, we have modified the complementary inputs on the inverter where INA=470mV+ε when INB=470mV-ε, with -470mV≤ ε ≤+470mV (470mV is supposed to be very close to the mean value). Figure 5.16 illustrates the DC measured results of the outputs of the complementary inverter versus one input (INA) with an average input value (between INA and INB) of 469mV.

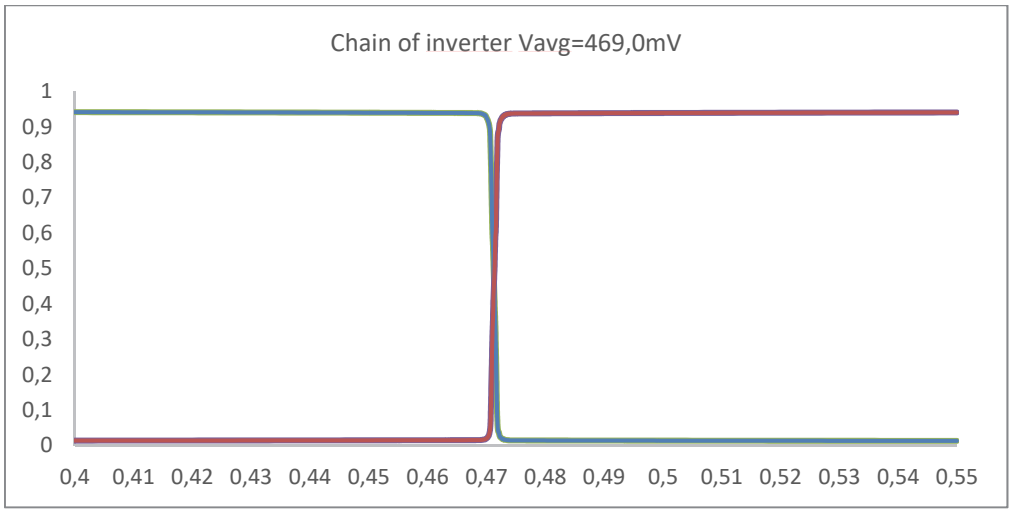


Figure 5.16: DC measured transfer function of the 5 complementary inverters chain

In order to determine the crossing point of the complementary outputs and the slope of one output (so the gain on the inverter), Figure 5.17 depicts a zoom of this measurement result. The crossing point is about 460mV for the output and 470mV for the input (in fact 461mV and 471mV respectively). The switching "noise" is lower than 2 mV for 5 inverters, so lower than 10mV for only one inverter as expected. We can roughly estimate from the graph that the slope at crossing point is

546, so the gain at midpoint VDD/2 is 109 after divided by the number of inverters 5. This gain is better than the simulated one which is about 50, in section 3.2 of chapter 2.

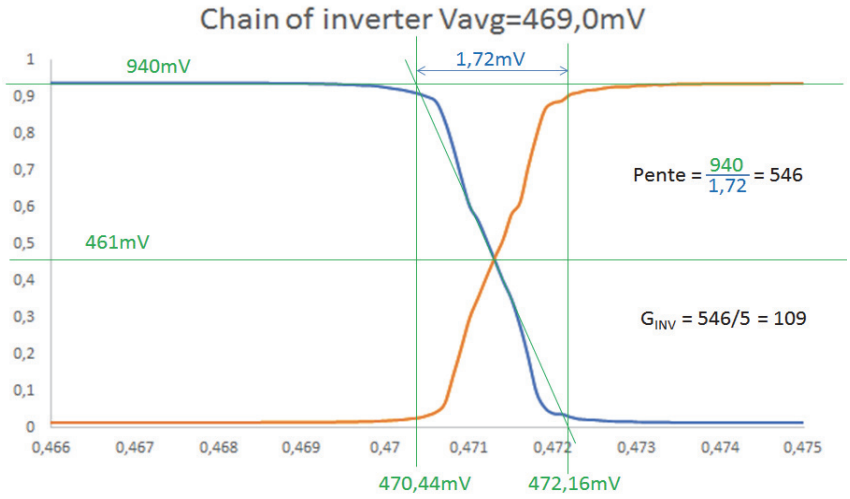


Figure 5.17: Zoom around the crossing point of the DC measured results

We can estimate that these results (crossing point and gain) have validated our concept on complementary inverter based on back-gate cross-coupling of UTBB-FDSOI transistors.

4.3. Current mirror

First measurements are performed on digital cells (i.e. complementary inverters), lets us now consider analog cell like current mirror. To optimize the length of the output transistor, we have realized different DC simulations with 3 values of L (34, 35 and 36 nm) and with the same width W=100µm. The simulated results, with CMin=45µA, are summarized in Figure 5.18.

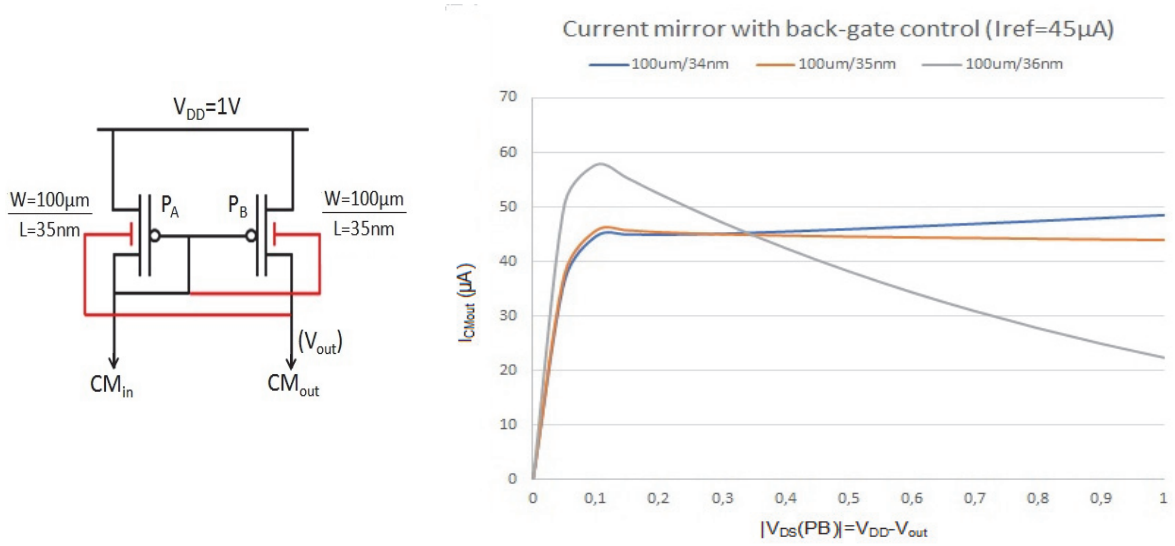


Figure 5.18: Current mirror with BG control topology and Simulations of a current mirror with BG control for different lengths of the output transistor

This result shows that the response (i.e. the output current) of the current mirror is very sensitive with the length of the transistors; secondly the optimum value is L=35nm.

As explained before, this current mirror is meant to be embedded in a VCRO and is tested with three different values of current (CMin=45, 90 or 180µA). We have implemented both with and without back-gate control. In the later, the back-gate is connected to VDD=1V. The sizes of the two transistors are the same for the two configurations with the optimum L value.

The respectively measurements, compared with simulations, are depicted in figures 5.19 and 5.20, where the abscissa represents the absolute value of the voltage $V_{DS}(P_B)$=Vout-V_{DD}.

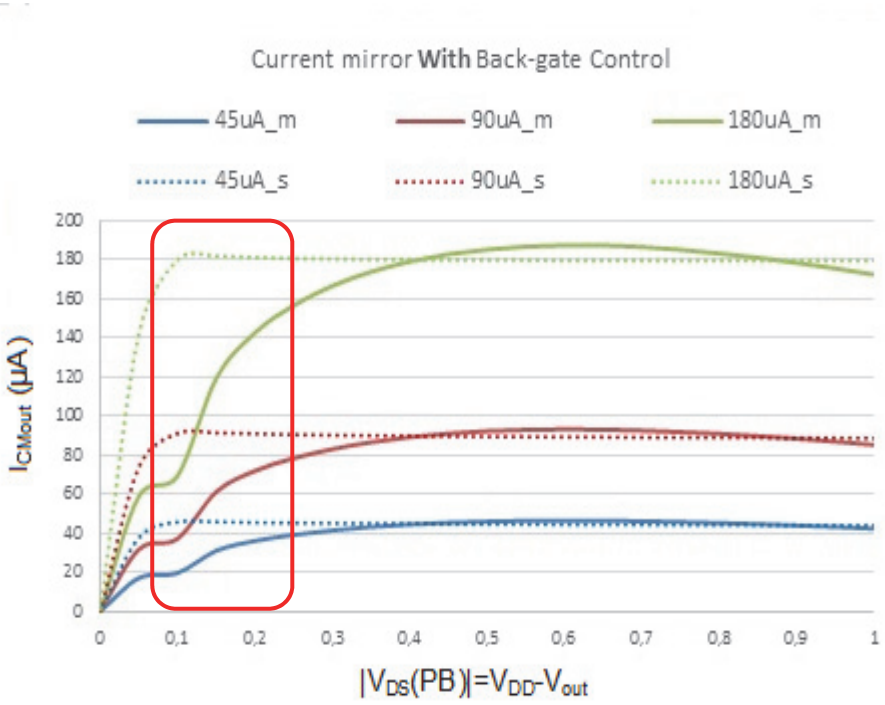


Figure 5.19: Comparison with back-gate control

In Figures 5.19 and 5.20, the solid-line corresponds to the measured results and the dotted-line to the simulations. We can notice some differences of the saturation voltage values between simulations and measurements (0.1V for simulation and higher value for measurement in red). However, in the measured saturation region, there is a good agreement between measurement and simulation. We can claim that, using the cross-coupled back-gate auto-biasing technique, there is a stabilization of the current in saturation region with a value equals to 45, 90 and 180µA respectively.

In order to estimate the maximum gain in terms of area between the two topologies (with and without BG control) of current mirror, we have realized some other simulations with different sizes of transistors for the basic current mirror, where the BG (as the bulk for MOS bulk transistor) is connected to the source (i.e. V_{DD}). Figure 5.21 illustrates the DC simulations of this current mirror

with different sizes of transistors with a constant W/L ratio which is equal to 100µm/35nm (for the minimum L, red curve) and 1000µm/350nm (for the maximum L, blue curve). For all cases, the input current CMin (i.e. Iref) is equal to 45µA, and the two transistors, P_A and P_B, are identical (same sizes).

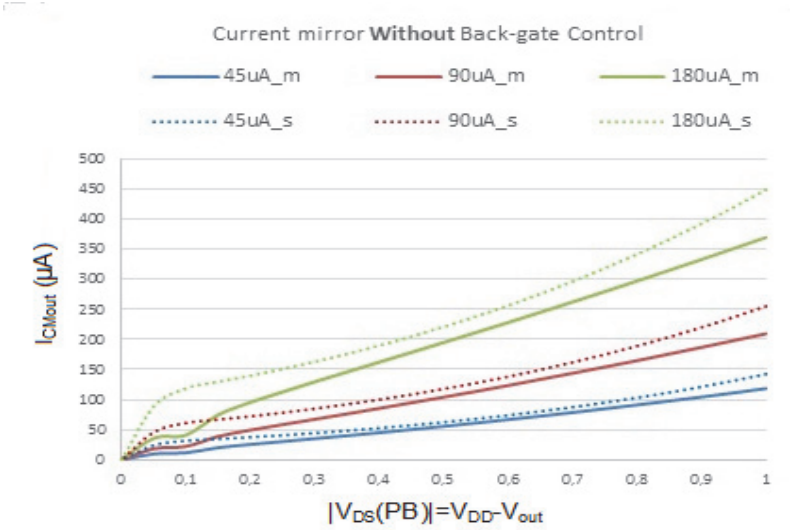
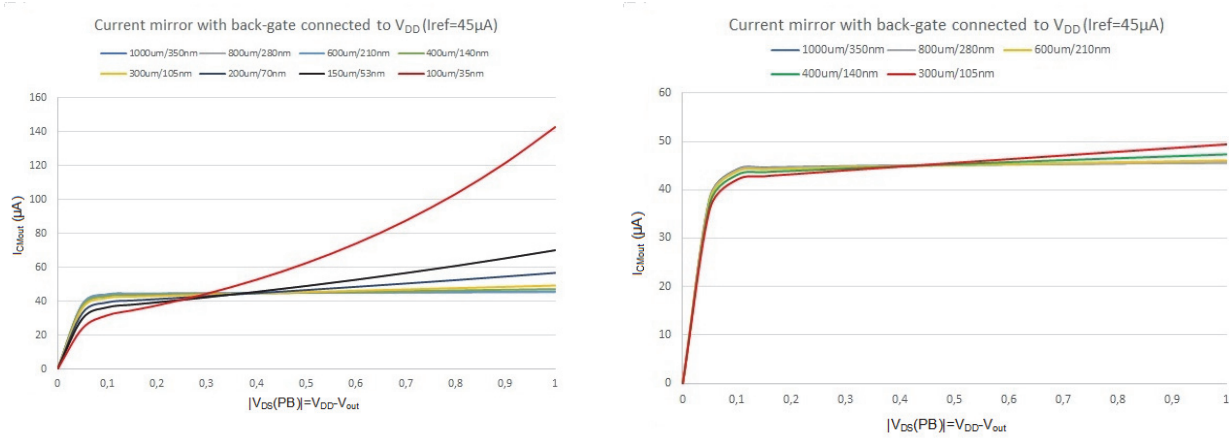


Figure 5.20: Comparison without back-gate control



(a) DC simulations for different transistor sizes (b) Zoom of DC simulations for a few transistor sizes

Figure 5.21: DC simulations of a basic current mirror (without BG control)

The length of the transistor has to be higher than 210nm to assume the behavior of a current generator (cf. Figure 5.21 (b)). To determine this minimum value of L, we have plotted the same simulations with only high values of L, from 105 to 350nm. The third last curves (L=210, 280 or 350nm) are quite identical and correspond to a good current mirror. After $|V_{DSsat}|$, I_{DS} is very close to a constant which is equal to 45µA.

In conclusion, for this current mirror, it is possible to reduce the size of the two transistors, P_A and P_B, by a factor of 6*6=36. This is a very impressive area saving. However, we should know also that there is a risk that the current mirror with back-gate control is easier to go into the linear region.

4.4. Ring oscillator

The two first previous measurements are realized in DC and a good agreement was found between measurements and simulations. The most important characteristic of the RO is its oscillation frequency which is a dynamic parameter. In chapter 3, this simulated result at transistor level is around 7.3GHz as depicted in Figure 3.25. With the same schematic (i.e. same file under Cadence, with the same sizes of transistors), this value becomes 3GHz using the design kit (PDK) of the CEA-LETI labs. Figure 5.22 illustrates the same transient simulation after layout extraction. This result exhibits a period of 378ps (close to 380ps given a frequency of 2.64GHz) with a power consumption of 5.1mA. Measured results will be compared with these new values. The test chip measurements exhibit an oscillation frequency of 2.14GHz for V_{DD}=1V with a power consumption of 5.9mA.

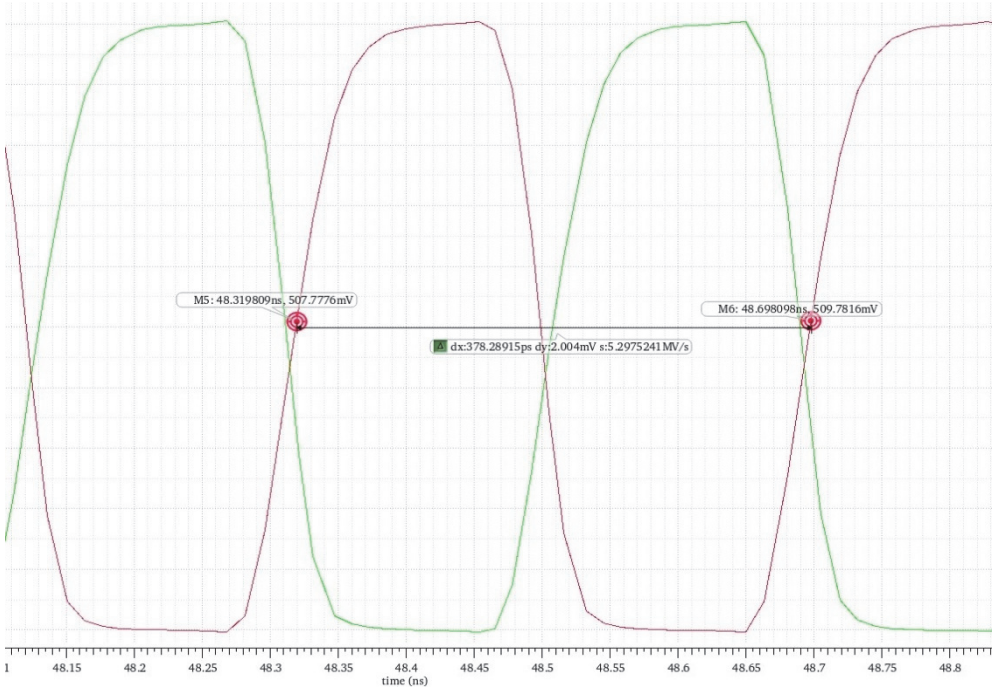


Figure 5.22: Post-layout transient simulation of the ring oscillator using CEA-LETI PDK

We have modulated the power supply (V_{DD}) to control the oscillation frequency. The tuning range of the oscillation frequency in function of V_{DD} is presented in Figure 5.23. We can observe a linear part from V_{DD}=0.6V to V_{DD}=1V, corresponding respectively to an oscillation frequency of fmin#480MHz to fmax#2.14GHz. The central frequency f_0=1.3GHz is obtained with V_{DD}=0.8V for a power consumption of 2.88mA (2.3mW). So, we can deduce the gain of the RO: KVCO=4.3GHz/V. Moreover, this high gain added to the power supply stability and the process variations can explain the frequency difference between measurements and simulations.

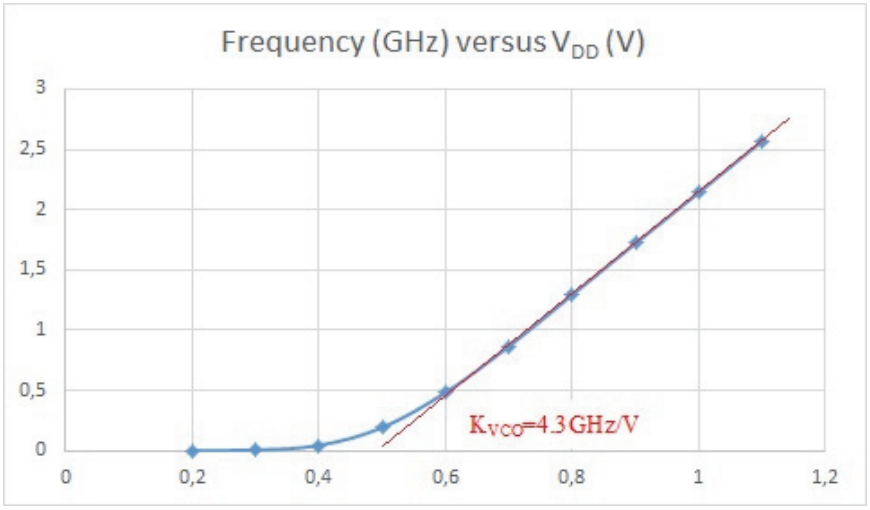


Figure 5.23: Oscillation frequency versus V_{DD}

Figure 5.24 illustrated the measured complementary outputs of an inverter of the RO. This result exhibits a 190MHz oscillation frequency obtained with V_{DD}=0.5V and a power consumption of 0.25mA (125µW).

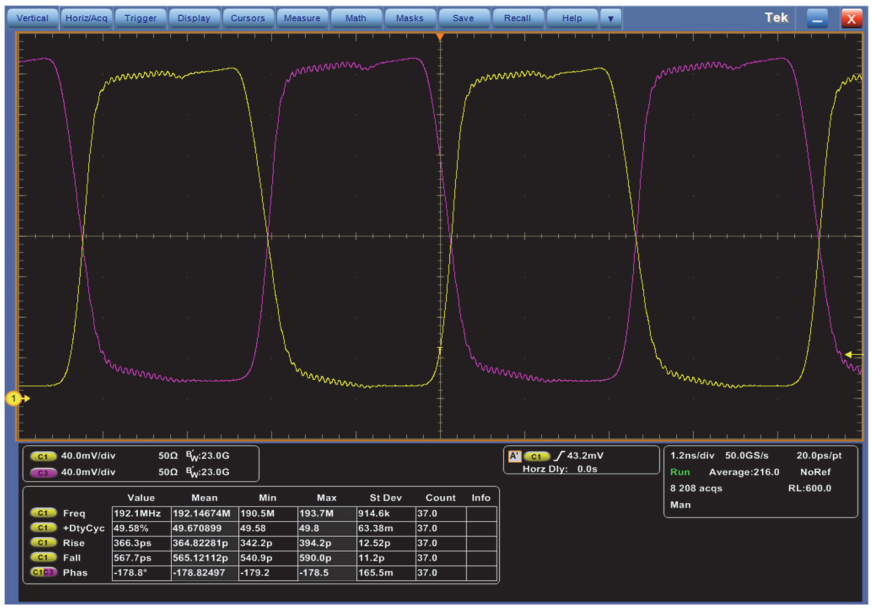


Figure 5.24: Time domain measurement of the RO at V_{DD}=0.5V

Figure 5.24 shows that the mean value of the duty cycle is equal to 49.67% (very close to 50%). The symmetrization of the two complementary outputs is quite good. However, the output dynamics is limited by V_{DD}, so a lever shifter will be needed for the design of the VCRO.

For each value of V_{DD} (i.e. oscillation frequency), we have also measured the power consumption, depicted in Figure 5.25. This result shows that this circuit is very efficient for low frequency application. For example, when VDD=0.5V for a frequency of 190MHz, the power consumption is only 0.25mA, then 125µW.

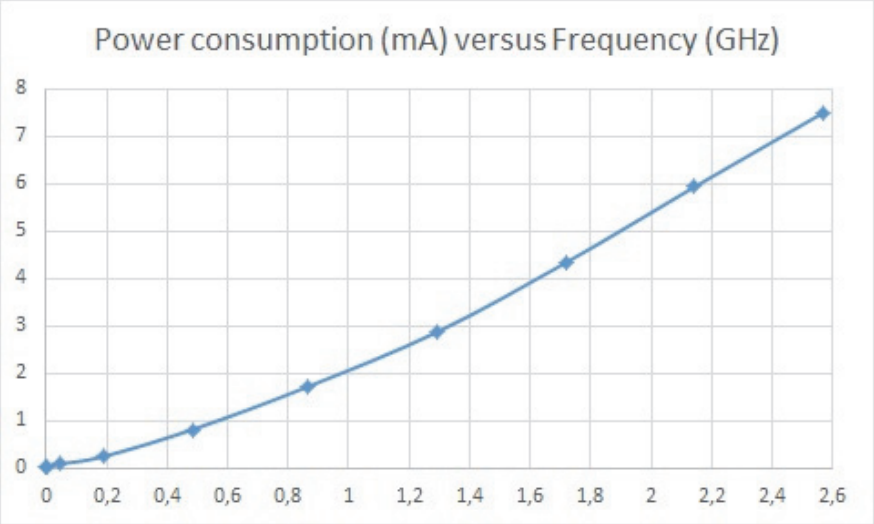
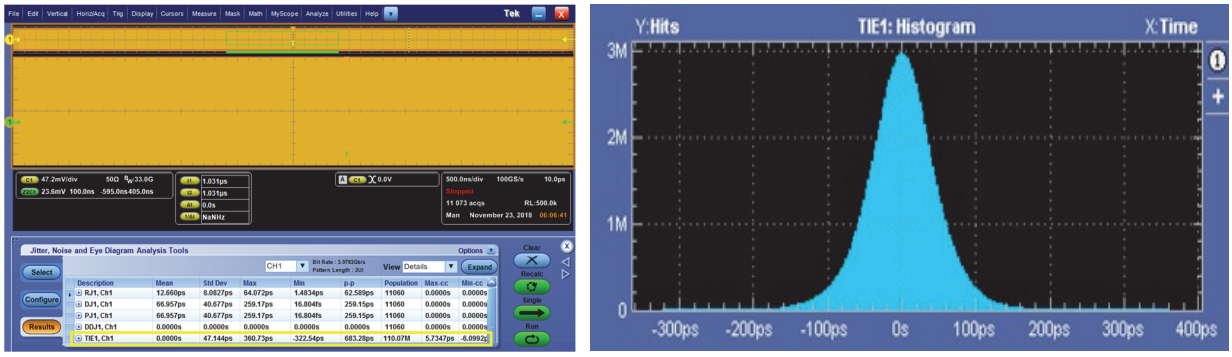


Figure 5.25: Power consumption versus oscillation frequency

Then, we have measured the jitter and the phase noise of the RO working at f_0=1.3GHz with V_{DD}=0.8V. Figure 5.26 illustrates this jitter measurement, its RMS value (standard deviation) is equal to σ=47ps (cf. Figure 5.26 (a)). Figure 5.26 (b) depicts the histogram of the jitter.



(a) Time domain (TIE1 configuration) (b) Jitter histogram

Figure 5.26: Jitter measurement

Figure 5.27 illustrates the phase noise measurement and exhibits a PN=-84dBc/Hz@1MHz. Using the complementary logic and the cross-coupled back-gate topology, the PN is improved compare with a classical RO. However, this PN has to be validated by another measurement. In fact, due to the high value of K_{VCO} and the variations of the power supply, it was not possible to measure directly the phase noise. The integration of this RO in a VCRO will make possible this measurement and will decrease the PN.

Table 5.2 gives a comparison of this circuit with two other QVCO topologies (LC tank and Rotary Traveling Wave: RTW) [4]. The Figure of Merit considered with area is given by the following equation:

$$FOM = -L(f_m) + 10log\left(\left(\frac{f_0}{f_m}\right)^2 . T_{\%}\right) - 10log\left(\frac{P_{DC}}{1mW}\frac{S}{1mm^2}\right) \quad (5.1)$$

where f_m is the frequency offset (f_m=1MHz in our case), f_0 the central frequency, L(f_m) the phase noise, P_{DC} the power consumption, S the surface of the VCO and T% is the relative tuning range given by T%=Tuning range/f_0.

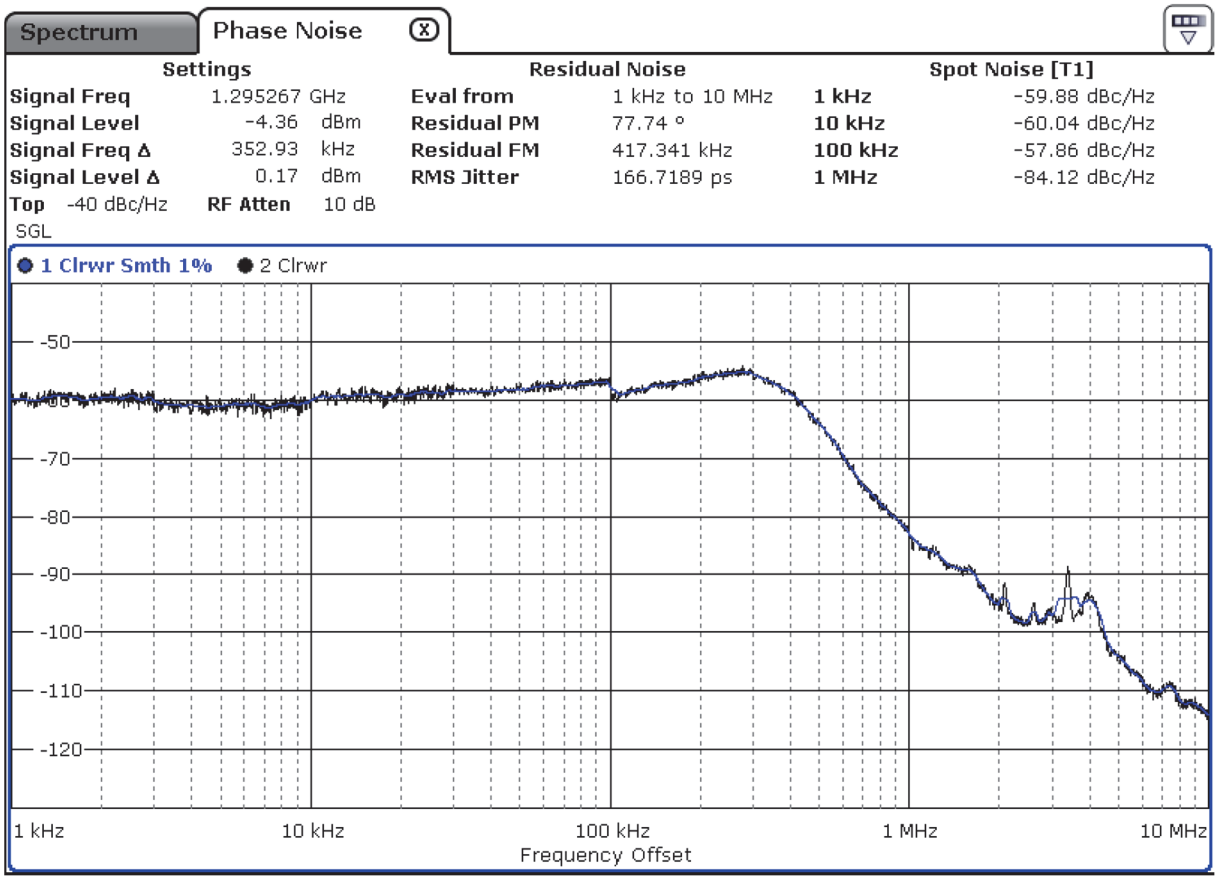


Figure 5.27: Phase noise measurement for f_0=1.3GHz at V_{DD}=0.8V

Table 5.2: Comparison of different types of VCO

	RTW VCO	LC QVCO	RO
Technology	CMOS 130nm	CMOS 130nm	FDSOI 28nm
Frequency	11.5GHz	13GHz	1.3GHz
Tuning range	1.2GHz	900MHz	1.7GHz
Consumption	30mW	8mW	2.3mW
Surface	0.105mm2	0.450mm2	0.0024mm2
PN@1MHz	105dBc/Hz	100dBc/Hz	-84dBc/Hz
FOM	171dB	165dB	171dB

Although a VCRO has higher phase noise compare with LC or RTW VCO, its low power consumption and particularly its very low surface make it a good candidate for some applications (especially at low frequencies) and exhibits a higher FOM.

The next step is to implement this RO in a complete VCO, then a PLL. However, modulating the supply voltage (V_{DD}) is not a good solution to realize a VCRO, a current starved topology of VCRO has been chosen as shown in chapter 4, section 2.3 (cf. Figure 4.11).

4.5. VCRO

We have implemented a VCRO using the current mirror studied and measured in section 4.3 of this chapter and the previous RO based on 4 complementary inverters. As explained before, a level shifter is needed as well as a 50Ω buffer.

Unfortunately, we cannot compare the measured results with the simulated ones. We have only realized some simulations using our PDK, which give an oscillation frequency of 7.3GHz for the RO at V_{DD}=1V. All these simulated results are given in chapter 4. For example, Figure 5.28 illustrates the simulated results and measured results of the tuning range. Other post-layout simulations using the CEA-LETI PKD are mandatory for better comparison.

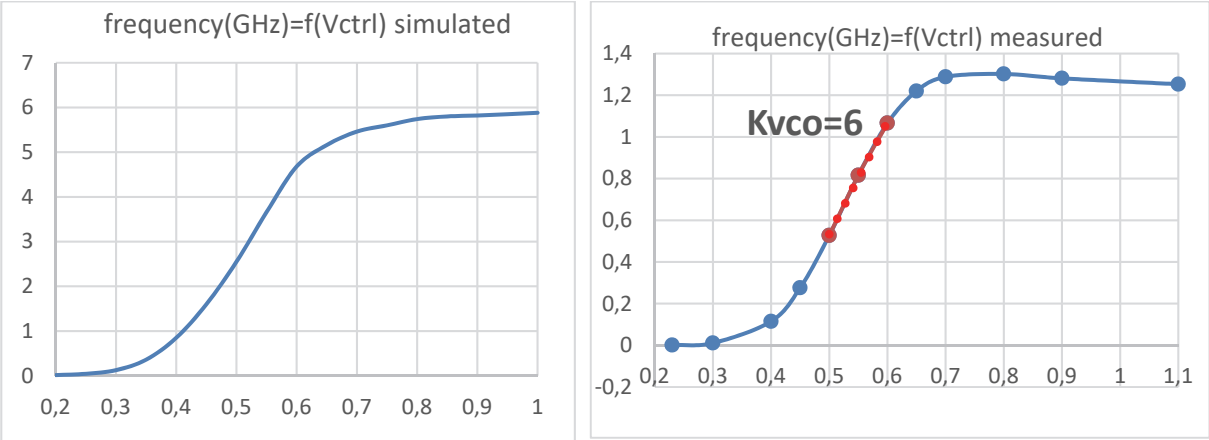


Figure 5.28: VCRO frequency versus Vctrl simulated and measured results

Considering only measurements, when control voltage (Vctrl) is bigger than 0.7V, the oscillation frequency is decreasing instead of expected increasing. That is because when Vctrl is bigger than 0.7V, the PMOS transistor that controls the input current of RO is no longer saturated, causing a mismatch between the input and output of the current mirror, resulting in a small current supply for RO, as well as a lower oscillation frequency. That is exactly the risk we mentioned in section 4.3 of this chapter.

Although we can still find an application when control voltage is between 0.5V and 0.6V, in which the simulated central frequency is 0.55GHz and the tuning range is 600MHz with a K_{VCO} of 6GHz/V, We are more looking forward to avoiding such problems in the next design.

The improvement is to independently simulate the characteristic curves of the current mirror and RO, as well as its impedance and adjust the transistor sizes to match each other in the simulation, to ensure that the current is regulated at its operating point.

5. Conclusion

In this chapter, we first introduced the common-centroid concept for layout design to help reduce mismatch and keep the symmetry of the output signals of a complementary inverter. Then, an overview of our ROSCOE test chip is given as well as all the layout implementation for complementary inverter, chain of inverters, current mirror, ring oscillator and VCRO respectively. Measurements of these building blocks give quite good agreement with simulations and validate the concept of back-gate cross-coupling for auto-calibration of analog and mixed-signal cells.

The proposed oscillator is easy to start and can work with the power supply V_{DD} down to 0.2V. As shown in Figure 5.29, RO exhibits a very good quality of the output signal at low frequency of 385kHz when V_{DD}=0.2V. Moreover, the power consumption is very low 30µA (6µW) and the duty cycle is always good with a mean value of 49.7%. Compared to other types of oscillator, the phase noise is always higher but FOM is quite good, and this kind of VCRO is very efficient for low power and low frequency applications.

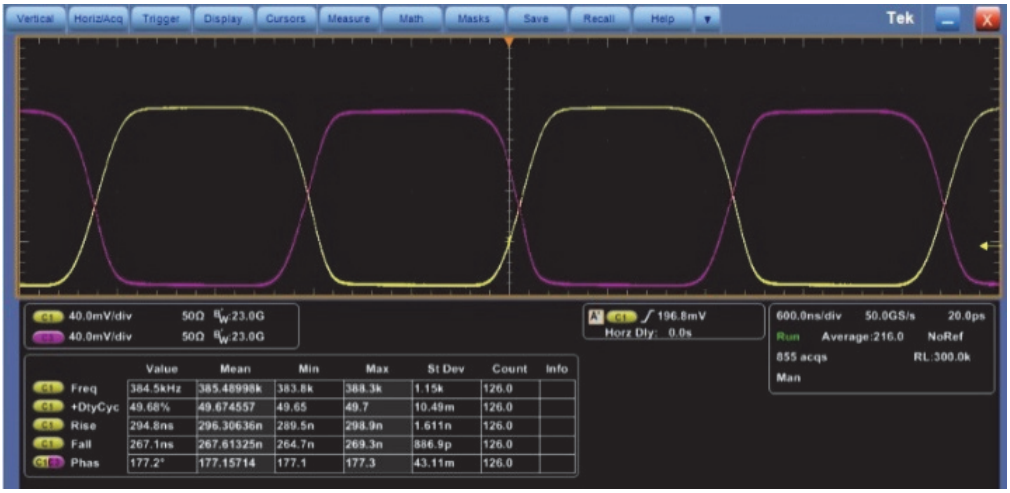


Figure 5.29: Complementary outputs of the RO at 385kHz (V_{DD}=0.2V)

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General conclusion and trends

1. Conclusion

This thesis is a contribution to the development of ring oscillator and novel building blocks for PLL using complementary logic in 28nm UTBB-FDSOI technology.

First, we reviewed the history of development of the integrated circuit and the trend of transistor scaling. It turned out that UTBB-FDSOI technology is an ideal candidate to continue Moore's law because of its unique structure and characteristics.

We proposed a complementary inverter based on the back-gate control structure in FDSOI technology offering two symmetrical output signals in which mismatches can be reduced and takes the advantage of high gain and better noise margin compared to classic inverters. The concept of back-gate control is the base for our thesis works and can be extended in digital complementary logic gate for more stable, symmetrical and resilient output signals.

Then a quadrature ring oscillator is built with four-stage complementary inverters which has better performances, simpler structure and is suitable for low power design. Since its quadrature signals are widely used in RF and modern digital communication applications. The proposed quadrature ring oscillator is ideal to build the components of a quadrature clock generator as well as quadrature VCO for digital PLLs.

Then we proposed all the building blocks for a digital PLL including VCRO, PFD, charge pump and frequency divider in complementary logic. The first main block VCO is composed by the proposed quadrature RO and a current mirror with back-gate control structure. The small-size back-gate controlled current mirror is a patent during this thesis work which can reduce small channel effect and therefore provide high impedance output. The complementary PFD has only nine transistors and there is no reset routing path, so it can overcome dead zone problem and greatly reduce time delay. Together with the charge pump composed by pull-up and pull-down network with back-gate controlled current mirror, PFD and CP together can work with a small mismatch at frequency up to up to several GHz and the output don't exhibit any spurious jump phenomenon. Then based on a 15-bit Galois LFSR, a high-speed frequency divider without prescaler is proposed which can work at a high frequency up to 15GHz and can achieve any division ratio from 4 up to 32768. All these building blocks above are implemented in 28nm UTBB-FDSOI technology and verified by SPICE simulation under 1V power supply.

At last the ROSCOE test chip was implemented in 28nm UTBB-FDSOI technology and realized with the help of CEA-LETI, CMP and STM. The test chip consists of several building blocks: complementary inverter, chain of 5 inverters, current mirror, ring oscillator and VCRO and its layout implementation is based on common-centroid concept to reduce mismatch and keep the symmetry for complementary outputs. Although the PDK is different between us and CEA-LETI lab, the measurements of these building blocks give quite good agreement with simulations and validate the concept of back-gate cross-coupling for auto-calibration of analog and mixed-signal cells: Complementary inverter has a better static gain than simulation; The proposed small-size current mirror with back-gate control structure has a similar performance with a conventional current mirror with 36-times larger in area; especially the RO is easy to start and exhibits a very good quality for the output signals. This RO exhibits the phase noise of -86dBc/Hz@1MHz and f_0=1.3GHz with 0.8V power supply and can work with in low power down to 0.2V. Compared to other types of oscillator, the phase noise is always higher but FOM is quite good considering the small area and low power consumption; Although the VCO measurement results are different from what we expected, it gives us a valuable experience of reminding us that impedance matching, operating point biasing are important and post-layout simulations using the right PKD are mandatory for better understanding.

To conclude, with back-gate control structure of UTBB-FDSOI technology, the complementary inverters allow to realize quadrature ring oscillators with a very simple design and all the novel building blocks for DPLLs based on complementary logic structure are proposed. In terms of low power design, all the blocks of PLL including PFD, CP and divider can operate at a relatively low power supply down to 0.6V according to the simulated results. Moreover, it turned out that the oscillator is very efficient at extremely low voltages in measurement. So, the proposed ring oscillator and PLL are clearly competitive in low power applications and other integrated circuit with limited areas.

2. Trends

The first measurement results for test chip are extremely encouraging. The future work consists of:

- Study and redesign the VCRO.
- More complex modeling analysis and high-level simulation to validate the topology of the PLL composed from these proposed building blocks.
- Layout implementation for all the building blocks of DPLL including independent circuits and complete system, realization in silicon and measurement.

• Propose new solutions in back-gate control structure for mixer and the other blocs as well as the complete RF receiver in UTBB-FDSOI technology

The digital PLL is expected to have quadrature outputs with low noise and high-speed. Its small surface and low power consumption make it a good candidate for some applications. For example, image rejection for mixer and receiver thanks to its quadrature and stable outputs; in 800/900MHz ultra-high frequency (UHF) RFID (radio-frequency identification) applications such as mobile vehicle identification, Logistics tracking, electronic latching theft (electronic remote door lock controller) and other industries, as depicted in Figure 3.

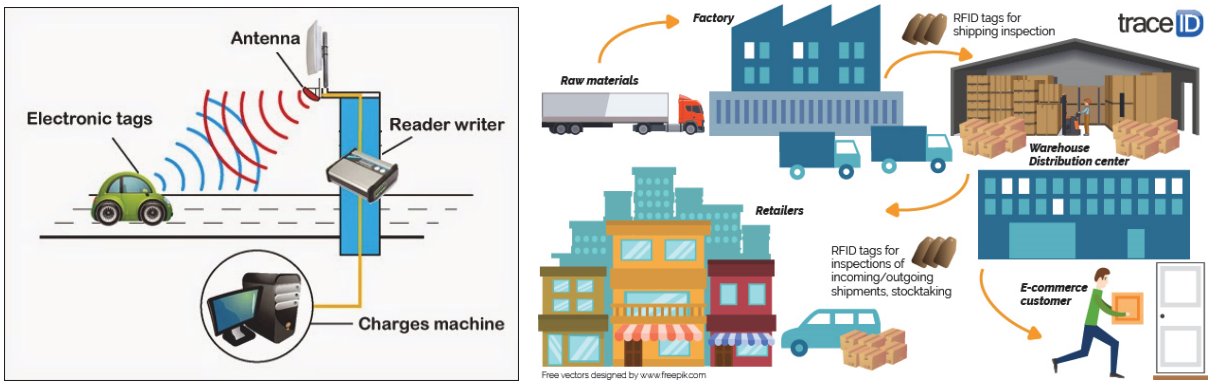

Figure 3: Application in RFID (source: asiarfid.com and trace-id.com)

Publications liées à cette thèse

Revues Internationales

1. Z. Wei, G. Jacquemod, P. Lorenzini, F. Hameau, E. de Foucauld & Y. Leduc, «Study and reduction of variability in 28nm Fully Depleted Silicon on Insulator technology», Journal of Low Power Electronics, vol. 12, n° 1, 2016, p. 64-73

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6. G. Jacquemod, Z. Wei, J. Modad, E. de Foucauld, F. Hameau, Y. Leduc & P. Lorenzini, «Study and reduction of variability in 28 nm FDSOI technology», VARI/PATMOS, Salvador de Bahia, Brazil, 2015, p. 19-22
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12. Z. Wei, G. Jacquemod, J. Prouvee, E. de Foucauld & Y. Leduc, «Low Power IoT Design using FDSOI Technology», SENSO, Gardanne, France, 2017

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13. Z. Wei, “Auto-Polarisation de la Grille Arrière pour Auto-Calibration de Cellules Analogiques et Mixtes en Technologie UTBB FDSOI”, FETCH, Villard-de-Lans, France, 2016
14. Z. Wei, Y. Leduc & G. Jacquemod, «Auto-Polarisation de la Grille Arrière pour Auto-Calibration de Cellules Analogiques et Mixtes en Technologie UTBB FDSOI», JNRDM, Toulouse, France, 2016
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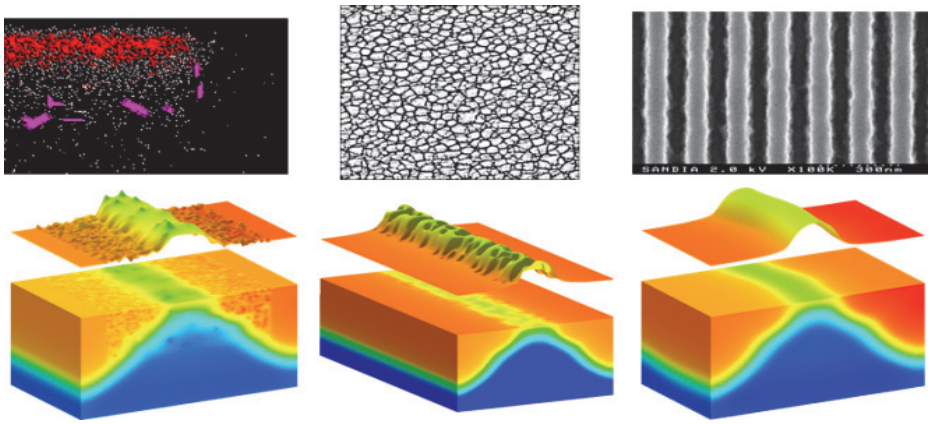
Brevets

16. P. Audebert, E. de Foucauld, Y. Leduc, G. Jacquemod, Z. Wei & P. Lorenzini, «Circuit électronique élémentaire pour étage d'amplification ou de recopie de signaux analogiques», Brevet Français CEA-LETI et UNS, 6 Avril 2017, WO2017055709 A1, PCT/FR2016/052394

Annex 1: Introduction générale en français

1. Introduction

L'augmentation continue depuis plus de 40 ans des performances de la technologie microélectronique est rendue possible par une miniaturisation des composants élémentaires. La prédiction de Gordon Moore [1], connue sous le nom de loi de Moore (la densité des transistors sur une puce double tous les 18 mois), s'est révélée d'une précision inégalée, en partie parce que la loi a été la clé de voûte de la longue planification à terme dans l'industrie des semi-conducteurs pour la recherche et le développement. Cependant, le transistor bulk MOS atteint ses limites : effet de canal court (SCE: Small Channel Effect et DIBL: Drain Induced Barrier Lowering), abaissement de la tension de seuil (Vth) et ralentissement de la diminution de la tension d'alimentation V_{DD}, plus de dissipation de puissance, moins de gain de vitesse, moins de précision, les problèmes de variabilité et de fiabilité, ... Comme le montre la figure 1, cela est principalement le résultat des fluctuations aléatoires du nombre de dopants (RDF : Random Dopant Fluctuations, Fig. 1.a) dans la région du canal, de la rugosité de la gravure (LER: Line Edge Roughness, Fig. 1.b), et dans une moindre mesure, entre autres, de la variation de l'épaisseur d'oxyde (TOx : Thickness Oxide, Fig. 1.c) [2].



(a) RDF (b) LER (c) TOx

Fig.1: Différentes sources de variabilités [2]

Pour surmonter ces problèmes induits par les nœuds technologiques de plus en plus agressifs de 28 nm et au-delà, deux solutions ont adoptés des transistors dont le canal n'est pas dopé [3] comme les technologies FinFET [4] et FDSOI [5]. Toutefois, ces technologies ont été dans un premier temps conçues pour des applications numériques, on peut donc se demander si ces transistors sont adaptés pour les circuits analogiques et RF? De plus, alors que les blocs numériques continuent à suivre la loi de Moore (i.e. à diminuer de surface), ce n'est pas le cas pour les circuits analogiques et en particulier pour les composants passifs (cf. Fig.2) [6]. Diminuer la partie analogique et supprimer les composants passifs d'un système sur puce complexe permet de diminuer la surface totale du circuit, voire sa consommation. Par exemple, les oscillateurs à anneaux (oscillateurs numériques sans

éléments passifs) sont connus pour présenter un bruit de phase élevé, mais cette conception aborde de manière agressive la taille et la réduction de la consommation d'énergie. Nous proposons, par la possibilité de la polarisation de la grille arrière offerte par la technologie FDSOI, de compenser la variabilité, les effets de canal court, … afin d'augmenter les performances de tels circuits.

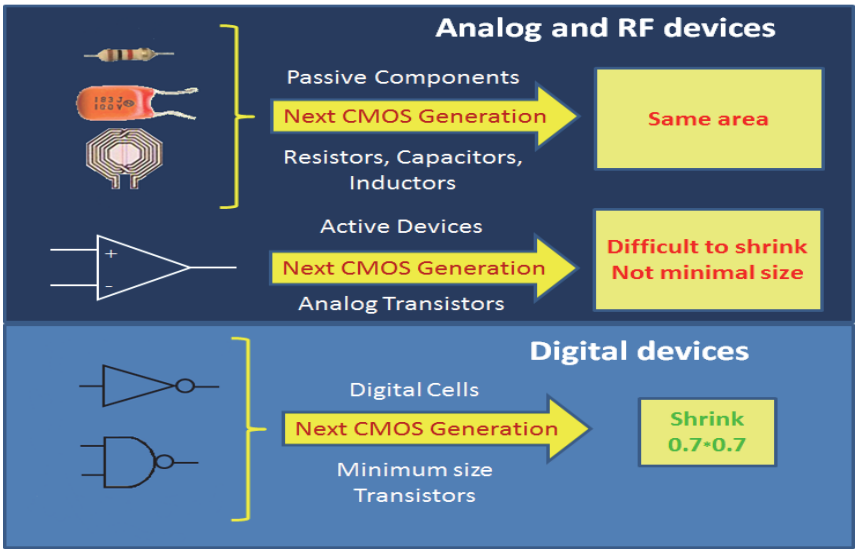


Fig.2: Problèmes de diminution de la surface pour les composants analogiques

2. Objectifs et motivation

Dans la course à la miniaturisation des circuits électroniques intégrés, il semble maintenant acquis que les technologies UTBB-FDSOI (Ultra-Thin Buried Box - Fully Depleted Silicon On Insulator) sont mieux adaptées aux tailles nanométriques. En effet, elles peuvent limiter les problèmes dus aux variations aléatoires des dopages utilisés dans les transistors classiques de type "bulk" et apporter une amélioration significative en termes de performances et de conception de faible puissance. Les travaux de thèse présentés dans ce mémoire apportent une contribution significative au développement et à la mise au point de nouveaux blocs de base pour la conception et la réalisation d'une boucle à verrouillage de phase (PLL) utilisant la logique complémentaire en technologie FDSOI 28 nm. Grâce à cette dernière, nous avons proposé un inverseur complémentaire basé sur une paire d'inverseurs à couplage croisé des grilles arrières offrant en sortie des signaux symétriques et complémentaires. Ce concept peut être étendu à toutes les cellules numériques pour générer des signaux de sortie plus stables, symétriques et résilients. D'abord nous avons conçu un oscillateur en anneaux rapide et performant composé par quatre inverseurs complémentaires délivrant des horloges de qualité en quadratures dont la fréquence d'oscillation mesurée est de 2.3 GHz. Puis, en utilisant la logique complémentaire et le contrôle de la grille arrière de cette technologie, nous proposons une solution efficace pour concevoir de nouvelles structures de VRCO, pompe de

charge basée sur une nouvelle topologie de miroir de courant, PFD, diviseur etc., qui sont les éléments de base des PLL à grande vitesse et à faible bruit. Toutes ces conceptions ont été simulées et vérifiées sous Cadence. En outre, une puce de test de RO, miroir de courant et VCRO a déjà été réalisée en silicium et testée, validant l'ensemble de nos travaux.

3. Travaux de Thèse

Le présent mémoire est composé de 5 chapitres, encadrés par une introduction générales et une conclusion incluant quelques pistes d'amélioration et de perspectives. On trouvera également en fin du manuscrit quelques annexes, ainsi que l'ensemble des publications liées à ces travaux de thèse.

Dans le premier chapitre, nous présentons les limites atteintes par la technologie MOS bulk classique et la fin annoncée de la loi de Moore. Pour les nœuds technologiques 22nm et au-delà, le canal des transistors n'est plus dopé, que ce soit pour des transistors FinFET ou UTBB-FDSOI. Les principales caractéristiques de la technologie FDSOI sont ensuite rappelées ainsi que ces avantages. Pour illustrer ces derniers pour des designs analogiques, notre choix s'est porté sur la conception d'une boucle à verrouillage de phase ou PLL (Phase-Locked Loop). Le principe de fonctionnement et les caractéristiques d'une PLL () sont donnés dans ce chapitre. L'accent est mis sur le jitter et le bruit de phase, point généralement faible des oscillateurs en anneau (RO : Ring Oscillator). L'objectif de cette thèse est justement de profiter de la technologie FDSOI pour proposer une nouvelle structure de RO afin de réduire ce jitter tout en continuant à limiter la consommation et la surface du circuit final.

Le second chapitre est dédié à la logique complémentaire. Nous rappelons ainsi la différence entre logique différentielle et logique complémentaire, avant de présenter l'implémentation d'un inverseur complémentaire en technologie FDSOI. La structure innovante d'un tel inverseur est basée sur le croisement des grilles arrières de chaque inverseur afin de symétriser les signaux de sortie complémentaire. L'objectif de cette structure est de limiter le bruit de commutation et d'offrir des temps de propagation identiques entres les deux inverseurs afin de limiter le jitter d'un oscillateur en anneau réalisé à partir de ces inverseurs complémentaires. Une étude statique et dynamique permet d'une part de valider ce concept et d'optimiser la taille des transistors. Ce concept est ensuite étendu à l'ensemble des portes numériques et un exemple d'application d'horloge est proposé.

Dans le troisième chapitre, nous rappelons la théorie des oscillateurs, les topologies de base en se focalisant sur les oscillateurs en anneau (RO : Ring Oscillator). Nous montrons en particulier que les inverseurs complémentaires permettent de réaliser des oscillateurs en quadrature avec un design très simple. Une étude approfondie de cette architecture permet d'en étudier les avantages et limitations. Là encore, cette étude nous a également permis d'optimiser le dimensionnement des transistors et d'évaluer les performances du RO, par des simulations Spice.

Le Chapitre quatre décrit l'ensemble des blocks de base d'une PLL, à savoir le VCRO, le détecteur de phase (PD et PFD), la pompe de charge et diviseur de fréquence. Pour chaque bloc, les topologies basiques sont rappelées, puis adaptées à notre concept de logique complémentaire. Des simulations Spice permettent à chaque fois d'optimiser la taille des transistors et d'évaluer les performances des circuits. Un effort particulier a été apporté à la conception et réalisation de la nouvelle structure du miroir de courant qui permet de limiter les effets de canal court tout en diminuant drastiquement la taille des transistors. Pour conclure ce chapitre, une simulation haut niveau, basée sur le simulateur NAPA, a permis de valider la topologie de la PLL réalisée à partir de ces blocs de base.

Le dernier chapitre est consacré à la réalisation d'un circuit de test en technologie FDSOI. Nous présentons la réalisation du dessin des masques, puis celle du circuit final implémentant l'ensemble des blocs de base afin de les tester séparément jusqu'au VCRO. La PLL entière n'a pas été réalisée. L'ensemble des mesures réalisées est présenté dans ce chapitre et permet de valider le concept de logique complémentaire utilisant le croisement des grilles arrières des transistors UTBB-FDSOI. Les résultats, en termes de performances, sont très prometteurs pour la suite de ce travail.

Enfin, des conclusions générales et quelques perspectives terminent ce manuscrit. Les publications liées à ce travail de thèse sont également présentées, suivies de quelques annexes.

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[6] http://download.intel.com/newsroom/kits/idf/2012_fall/pdfs/IDF2012_Justin_Rattner.pdf

Annex 2: NAPA code for 15-bit LFSR

```
header  <napa.hdr>
header  <toolbox.hdr>
title  "feedback counter order 15, phase based description"
fs     2.0e+6    //  twice clk frequency
node    void  cell pls1  "./galois_15.net" b15..1
decimate fs 2 1    //phase2  cycle 0
node      y    btoi  b15..1
tool    pdetect "periode_g15.out"  y 1
directive PDETECT 100
node      loop_index dalgebra LOOP_INDEX/2
output  stdout      loop_index y  b15..1   //15 bits output:b15,b14,…,b1
format (digital)  S
terminate 500000 < LOOP_INDEX
cell interface  $dummy $b15..1

galois_15.net
node $b14    cell   c15 "cellx.net"  $b15 $bn15
node $b13    cell   c14 "cell1.net"  $b14
node $b12    cell   c13 "cell1.net"  $b13
node $b11    cell   c12 "cell1.net"  $b12
node $b10    cell   c11 "cell1.net"  $b11
node $b9     cell   c10 "cell1.net"  $b10
node $b8     cell   c09 "cell1.net"  $b9
node $b7     cell   c08 "cell1.net"  $b8
node $b6     cell   c07 "cell1.net"  $b7
node $b5     cell   c06 "cell1.net"  $b6
node $b4     cell   c05 "cell1.net"  $b5
node $b3     cell   c04 "cell1.net"  $b4
node $b2     cell   c03 "cell1.net"  $b3
node $b1     cell   c02 "cell1.net"  $b2
node $bn15     cell   c01 "cell2.net"  $b1
node $b15    inv    $bn15

cellx.net
cell interface  $out $in $fb
declare (digital) $in $fb
decimate fs 2
node $s1   delay  $in
node $s2   inv   $s1
decimate fs  2 1
node $s3   delay  $s2
node $out  xnor   $s3 $fb
nominal fs
init $in    0

cell1.net
cell interface  $out $in
declare (digital) $in
```

```
decimate fs 2
node $s1   delay  $in
node $s2   inv    $s1
decimate fs  2 1
node $s3   delay  $s2
node $out  inv    $s3
nominal fs
init $in    0
```

```
cell2.net
cell interface  $out $in
declare (digital) $in
decimate fs 2
node $s1   delay  $in
node $s2   inv    $s1
decimate fs  2 1
node $out   delay  $s2
nominal fs
init $in    0
```

Annex 3: NAPA code for DPLL

```
header <napatool.hdr>
fs   1000.00e+9                //Sampling frequency
title "(Polytech) PLL, frequency domain analysis"
ivar M  1
ivar N  1                      //Divider set to its initial
data  "./myPFD3.dat"    Pfd31     //  PFD type 3
data  "./myCP3.dat"     Cp31      //  Charge pump 3 levels
data  "./myLPF.dat"     Lpf1
string  Vco1     "./myVCO.dat"    //VCO frenquency in function of voltage
string  filefr   "./freq.dat"     // read the clock reference
node fin    cell  pwl1  <PWL/d.net>  filefr  1  1.0 0.0  (aperiodic)
node in     iuser fm    fin
node tag1   duser dpll  in   M  N  Pfd31 Cp31 Lpf1 Vco1
node fout1  duser dpll  tag1   (frequency)
node cout1  duser dpll  tag1   (control)
terminate  TIME > 3.5e-6         //Running time
output  stdout    cout1(_V) fout1(G_Hz)
output  "dpll_weitest33.out"     fin(M_Hz) fout1(G_Hz)
ping
debug DPLL

myPFD3.dat
data interface  $pfd
#* PLL Phase Frequency Detector parameters
string  $nam      "PFD"
ivar    $typ      3            // PFD type  negative feedback
dvar    $del_sig   16e-12       // PFD delay for the reference signal
dvar    $del_ref   16e-12       // PFD delay for the feedback reference
ganging $pfd[4]    $nam  $typ  $del_sig  $del_ref
myCP3.dat
data interface $cp
#   PLL Charge Pump parameters
dvar $im   -20e-6     // current
dvar $iz    $ip + $im   // by construction
dvar $ip    20e-6     // current
ganging  $cp[3]  $im $iz $ip

myLPF.dat
data interface  $Coef
# Second Order Low Pass Filter for PLL
dvar    $C1   0.001e-9
dvar    $R2   7.597e3
dvar    $C2   0.003e-9
#* numerator  $n0 + $n1*s + $n2*s^2  =  1.0 + (R2*C2)*s
dvar    $n0   1.0
dvar    $n1   $R2 * $C2
dvar    $n2   0.0
#* numerator  $d0 + $d1*s + $d2*s^2  =  (C1+C2)*s + (R2*C1*C2)*s^2
```

```
dvar    $d0   0.0
dvar    $d1   $C1 + $C2
dvar    $d2   $R2 * $C1 * $C2
ganging $Num[3]  $n0..2
ganging $Den[3]  $d0..2
ganging $Coef[2] $Num  $Den

myVCO.dat
# VOLTAGE FREQUENCY
0.2     0.028e9
0.25    0.078e9
0.3     0.21e9
0.35    0.5e9
0.4     1.01e9
0.45    1.74e9
0.5     2.61e9
0.55    3.57e9
0.6     4.51e9
0.65    5.11e9
0.7     5.41e9
0.75    5.59e9
0.8     5.7e9
0.85    5.79e9
0.9     5.85e9
0.95    5.9e9
1       5.93e9

freq.dat
# fm clock modulator input
#    TIME    Frequency
  0.0                 0.0e9
 1.0e-9             4.0e9
 1499.9e-9       4.0e9
 1500.1e-9       6.0e9
 2500.0e-9       6.0e9
 4000.0e-9       3.0e9
 4500.0e-9       3.0e9
 5000.0e-9       6.0e9
 6000.0e-9       6.0e9
 6001.0e-9       3.0e9
10000.0e-9       3.0e9
# end
```

Auto-Polarisation de la Grille Arrière pour Auto-Calibration de Cellules Analogiques et Mixtes en Technologie UTBB-FDSOI

Résumé : Dans la course à la miniaturisation des circuits électroniques intégrés, il semble maintenant acquis que les technologies UTBB-FDSOI sont mieux adaptées aux tailles nanométriques, car elles peuvent limiter les problèmes dus aux variations aléatoires des dopages utilisés dans les transistors classiques de type “bulk” et apporter une amélioration significative en termes de performances et de conception de faible puissance.

Les travaux de thèse présentés dans ce mémoire apportent une contribution significative au développement et à la mise au point de nouveaux blocs de base pour la conception et la réalisation d’une boucle à verrouillage de phase (PLL) utilisant la logique complémentaire en technologie UTBB-FDSOI 28 nm. Grâce à cette dernière, nous avons proposé un inverseur complémentaire basé sur une paire d’inverseurs à couplage croisé des grilles arrières offrant en sortie des signaux symétriques et complémentaires. Ce concept peut être étendu à toutes les cellules numériques pour générer des signaux de sortie plus stables, symétriques et résilients. D’abord nous avons conçu un oscillateur en anneaux rapide et performant composé par quatre inverseurs complémentaires délivrant des horloges de qualité en quadratures dont la fréquence d’oscillation est de 7.3 GHz. Puis, en utilisant la logique complémentaire et le contrôle de la grille arrière de cette technologie, nous proposons une solution efficace pour concevoir de nouvelles structures de VRCO, pompe de charge, PFD, diviseur etc., qui sont les éléments de base des PLL à grande vitesse et à faible bruit. Toutes ces conceptions ont été simulées et vérifiées sous Cadence. En outre, une puce de test de RO, miroir de courant et VCRO a déjà été réalisée en silicium et testée, validant l'ensemble de nos travaux.

Mots clés : Technologie UTBB-FDSOI, contrôle de la grille arrière, inverseur complémentaire, logique complémentaire, oscillateur en anneau, oscillateur commandé en tension, boucle à verrouillage de phase

Back-gate Feedback for Auto-Calibration of Analog and Mixed Cells in UTBB-FDSOI Technology

Abstract: In the competition of the miniaturization of integrated electronic circuits, UTBB-FDSOI technologies are better adapted to nanometric sizes, because they can limit the problems due to the random doping variations used in conventional “bulk” transistors and bring a significant improvement in terms of performance and low power design.

This thesis is a contribution to the development of novel building blocks for PLL using complementary logic in 28nm UTBB-FDSOI technology. Using this technology, we proposed a complementary inverter based on a pair of back-gate cross-coupled inverters offering a fully symmetrical operation of complementary signals. This design concept can be extended to any digital cells to generate more stable, symmetrical and resilient output signals. First, we designed a fast and efficient ring oscillator composed by four complementary inverters delivering quadrature clocks which oscillation frequency is 7.3GHz. Then using complementary logic and back-gate control structure, we proposed an efficient solution to produce novel structures of VRCO, PFD, Charge pump, divisor etc., which are the key building blocks of high-speed low noise PLLs. All these designs have been simulated and verified using Cadence. Moreover, a test chip of RO, current mirror and VCRO have already been realized in silicon and tested.

Keywords: UTBB-FDSOI technology, back-gate control, complementary inverter, complementary logic, Voltage-controlled ring oscillators, Phase locked loops