Millimeter-wave and terahertz frequency synthesis on advanced silicon technology

Raphael Guillaume

THÈSE PRÉSENTÉE
POUR OBTENIR LE GRADE DE

DOCTEUR DE L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES DE L'INGÉNIEUR
SPÉCIALITÉ : ÉLECTRONIQUE

par **Raphaël GUILLAUME**

Millimeter-Wave and Terahertz Frequency Synthesis on Advanced Silicon Technology

Directeurs de thèse : Andreia CATHELIN
Yann DEVAL

Préparée à STMicroelectronics
et au Laboratoire IMS

Soutenue le : 18 décembre 2018

Devant la commission d'examen formée de :

Sylvain BOURDEL	Professeur des Universités	Grenoble INP	*Rapporteur*
Franck BADETS	Docteur Ingénieur – HDR	CEA LETI Grenoble	*Rapporteur*
Andreas KAISER	Directeur de recherche CNRS	ISEN Lille	*Président*
Cristell MANEUX	Professeur des Universités	Université de Bordeaux	*Examinateur*
François RIVET	Maître de Conférence	Bordeaux INP	*Examinateur*
Nathalie DELTIMPLE	Maître de Conférence – HDR	Bordeaux INP	*Examinateur*
Andreia CATHELIN	Docteur Ingénieur – HDR	STMicroelectronics	*Co-directrice*
Yann DEVAL	Professeur des Universités	Bordeaux INP	*Directeur*

Thèse réalisée au Laboratoire de l'Intégration du Matériau au Système (IMS)
de Bordeaux, au sein de l'équipe CAS du groupe Conception.

Laboratoire IMS – Bâtiment A31
351 Cours de la Libération
33405 Talence Cedex

Thèse CIFRE réalisée dans l'entreprise STMicroelectronics,
au sein de l'équipe Process R&D.

STMicroelectronics
850 Rue Jean Monnet
38926 Crolles Cedex

"La science est une lanterne sur les faits.
Elle éclaire les choix, qui eux sont politiques."
Anonyme

Résumé

Ces dernières années les bandes de fréquence millimétriques et térahertz (THz) ont montrées un fort potentiel pour de nombreuses applications telles que l'imagerie médicale et biologique, le contrôle de qualité ou les communications à très haut débit. Les principales raisons de cet intérêt sont les nombreuses propriétés intéressantes des ondes THz et millimétriques, telles que leur capacité traverser la matière et ceci de manière inoffensive ou le large spectre disponible à ces fréquences. Les applications visées nécessitent des sources de signaux énergétiquement efficaces, à forte puissance de sortie et, pour certaines applications, à faible bruit de phase. De plus, la demande croissante pour des applications dans ces bandes de fréquence imposent l'utilisation de technologie de hautes performances à coût métrisé et permettant une intégration à très grande échelle, telle que la technologie 28nm CMOS FD-SOI.

Dans ce contexte, cette thèse propose une solution innovante pour la génération de fréquence millimétrique et THz en technologie CMOS : l'oscillateur distribué verrouillé par injection. Les travaux présentés dans ce manuscrit englobent l'analyse détaillé de l'état de l'art et de ses limites, l'étude théorique approfondie de la solution proposée pour une intégration en ondes millimétriques, le développement d'une méthodologie de conception spécifique en technologie CMOS ainsi que la conception de démonstrateurs technologique. Les différents oscillateurs intégrés en technologie 28nm FDSOI et opérant à des fréquences respectivement de 134 GHz et 200 GHz ont permis de démontrer la faisabilité de sources de signaux millimétrique et THz, à forte efficacité énergétique, forte puissance de sortie et faible bruit de phase en technologie CMOS à très grande échelle d'intégration. Enfin, la capacité de verrouillage par injection de tels oscillateurs distribués a été démontrée expérimentalement ouvrant la voie à de futurs systèmes THz totalement intégrés sur silicium. Les solutions intégrées démontrées dans cette thèse ont, à l'heure actuelle, la plus grande fréquence d'oscillation dans un nœud Silicium 28nm CMOS.

Abstract

In recent years, millimeter-wave (mm-wave) and terahertz (THz) frequency bands have revealed a great potential for many applications such as medical and biological imaging, quality control, and very-high-speed communications. The main reasons for this interest are the many interesting properties of THz and millimeter waves, such as their ability to harmlessly penetrate through matter or the broad spectrum available at these frequencies. Targeted applications require energy efficient signal sources with high power output and, for some applications, low phase noise. In addition, the increasing demand in mm-wave/THz applications requires the use of a cost-optimized, high-performance, and very large scale integration (VLSI) technologies, such as the 28nm CMOS FD-SOI technology.

In this context, this thesis proposes an innovative solution for mm-wave and THz frequency generation in CMOS technology: the injection locked distributed oscillator (ILDO). The work presented in this manuscript includes the detailed analysis of the state-of-the-art and its limitations, the detailed theoretical study of the proposed millimeter-waves band solution, the development of a specific design methodology in CMOS technology as well as the design of technological demonstrators. The several 28nm FDSOI integrated distributed oscillators at 134 GHz and respectively 200 GHz have demonstrated the feasibility of mm-wave and THz signal sources with high-energy efficiency, high output power, and low phase noise in a VLSI CMOS technology. Finally, the injection locking capability of such distributed oscillators has been demonstrated experimentally paving the way for a future silicon-based fully integrated THz systems. The proposed circuits are as of today the highest oscillation frequency solutions demonstrated in a 28nm CMOS Silicon technology.

Remerciements

Cette section a sans doute été pour moi la plus difficile à rédiger. Il y a tant de personnes qui ont participé à la réussite de ces travaux et tous les mots que j'écris aujourd'hui me semblent trop faibles pour refléter la profonde gratitude que je ressens.

En premier lieu, je tiens à remercier les membres du jury pour l'intérêt qu'ils ont porté à ces travaux et pour les échanges scientifiques très enrichissant qui ont suivi.

Je souhaite sincèrement remercier mes directeurs de thèse pour l'honneur qu'ils m'ont fait d'encadrer ces travaux. Merci Yann, ces trois années à travailler à tes côtés resteront inoubliables. Merci Andreia d'avoir su me guider pour hisser ces travaux au plus haut niveau.

Merci à tous mes collègues du laboratoire IMS et de STMicroelectronics d'avoir contribué à l'excellente ambiance de travail. Ainsi, merci Yoan, David P., Manuel, Jérémie, Boris, Florent, Florian, David G., Thibaut D., Dwight, Julian, Nassim, Khoa, Samuel, Romane, Magali, Hervé, Dominique, Camille, Arnaud, Eric. Merci également à Thomas, Louise, Mohammed, Ronan, Angel, Philippe et Robin.

Je tiens tout particulièrement à adresser un énorme merci à Thibaud et Fanny sans qui ces années de thèse auraient été radicalement différentes.

Merci à François, tu as été un chef d'équipe exemplaire et c'était un honneur de faire vivre l'équipe CAS à tes côtés. Mais tu as surtout été un ami sans faille dans les moments difficiles.

Je tiens également à remercier tout particulièrement Nathalie pour m'avoir fait découvrir le monde de la recherche et sans qui il ne me serait pas venu l'envie de réaliser une thèse.

Un grand merci à tous mes amis et à mes parents pour m'avoir supporté dans mes choix, mes réussites et mes échecs. Merci Niels et Sarah, les meilleurs frère et soeur du monde.

Infine, ringrazio amorevolmente Elisa per avermi aiutato a realizzare questa avventura.

Contents

List of Figures

List of Tables

Introduction

Millimeter-wave (mm-wave) and terahertz (THz) frequency bands have many attractive properties, such as the ability to penetrate through matter, non-ionizing radiation, and large bandwidth availability. These features make mm-waves and THz systems suitable for many applications such as non-ionizing biomedical imaging, non-destructive quality control, and very high data rate communication.

Because of the recent increasing demand on mm-wave/THz applications, many researchers have been interested in integrating signal sources in this frequency range, especially in cost-optimized silicon technology as SiGe and CMOS.

Several silicon-based mm-wave and THz oscillators have been recently reported. Nevertheless, most of them are integrated in SiGe technology and the targeted applications drive the need for high performances and very large scale integration that FD-SOI CMOS can offer. Moreover, all these mm-wave/THz systems require an efficient signal source with a maximized output power and, for some applications, the phase noise performances are critical. For these reasons, this thesis, realized in the frame of the ST-IMS common laboratory, is focusing on the following goals:

- Highlight the intrinsic limitations of classic oscillator topologies for efficient silicon integration of mm-wave and THz sources.
- Propose and demonstrate an alternative design solution to overcome these limitations and meet the challenging performances in terms of output power, energy efficiency, and phase-noise.
- Explore the 28nm FD-SOI CMOS technology for mm-wave/THz applications and demonstrate its capabilities for mmW design with industrial margin, through a well defined design methodology.

This manuscript is composed of four chapters. The first chapter is defining the context

of this work and presents the state-of-the-art of silicon-based mm-wave and THz signal source. The main limitations of classic oscillator topologies are highlighted and recent design techniques are introduced. The challenges for future THz applications are then discussed and key mm-wave source parameters are exposed.

The second chapter is proposing an alternative for mm-wave and THz frequency generation in CMOS technology: the injection locked distributed oscillator (ILDO). In this chapter, injection locked oscillator (ILO) theory is introduced and extended to the study of ILDO for operation close to transistors' f_{max}.

The third chapter presents first the 28nm FD-SOI CMOS technology for mm-wave and THz applications. A distributed oscillator design methodology is then presented and this methodology is used to realize two distributed oscillators at mm-wave/THz frequencies taking advantage of the high performances of the 28nm FD-SOI technology.

The fourth chapter describes the experimental results of this thesis work. First standalone transistor measurements are presented, highlighting the excellent high-frequency performances of the 28nm FD-SOI NMOS transistors. Then, the two designed distributed oscillators results are described. Excellent performances in terms of output power and DC-to-RF efficiency are reported, despite the limited back-end performances of such very dense technology nodes. The presented oscillators exhibit the measured highest oscillation frequency for an integrated CMOS oscillator in a 28nm node, upon the state-of-the-art at the date this manuscript is proposed. On-wafer probing measurements have been conducted exhibiting the low variability feature of such distributed oscillator architectures. Moreover, phase-noise optimization feature is introduced taking advantage of FD-SOI uniquely large body-bias tuning range. Finally, the injection locked capability of such distributed oscillators is demonstrated by experimental injection trials.

The final part of this thesis manuscript is dedicated to the general conclusion and presents research perspectives for future mm-wave and THz integration in CMOS VLSI technology.

1 Millimeter-wave and Terahertz Technologies

In recent years, millimeter-wave (mm-wave) and terahertz (THz) systems have attracted many researchers due to the promising applications in these frequency bands, from imaging to high data rate applications. The most important block of such systems is the signal source which needs to reach the highest possible output power, high efficiency, and low phase noise.

In this chapter, we will first introduce the context of silicon-based mm-wave and THz applications. Then, mm-wave and THz oscillator topologies will be described to highlight their intrinsic limitations. Finally, a state-of-the-art analysis of mm-wave and THz sources will be performed in order to identify the most relevant research axes for future silicon-based mm-wave and THz systems.

1.1 Mm-wave and THz applications

Since the beginning of 21^{th} century, millimeter-wave (mm-wave) and terahertz (THz) frequency ranges become increasingly attractive for many applications [1–3]. The main reasons for this interest are linked to the interactions between THz rays and matter. Indeed, THz radiations are able to penetrate through dielectric matter like plastics, clothes, ceramic, etc...

Nevertheless, the THz frequency band suffers from its position in the electromagnetic spectrum. Indeed, as depicted in figure 1.1, this band is located at the frontier between optics and electronics. Also named the *THz Gap*, this band cannot be approached using classic optic principles because of the larger wavelengths of the THz radiations. From an electronic point of view, this band is also extremely hard to reach due to the limited f_T/f_{max} of silicon technologies.

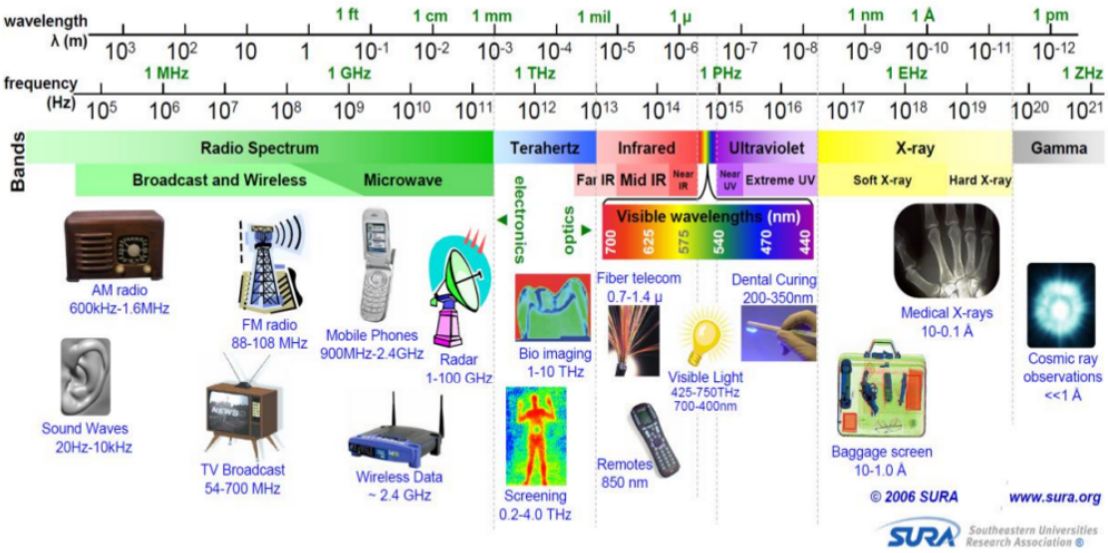
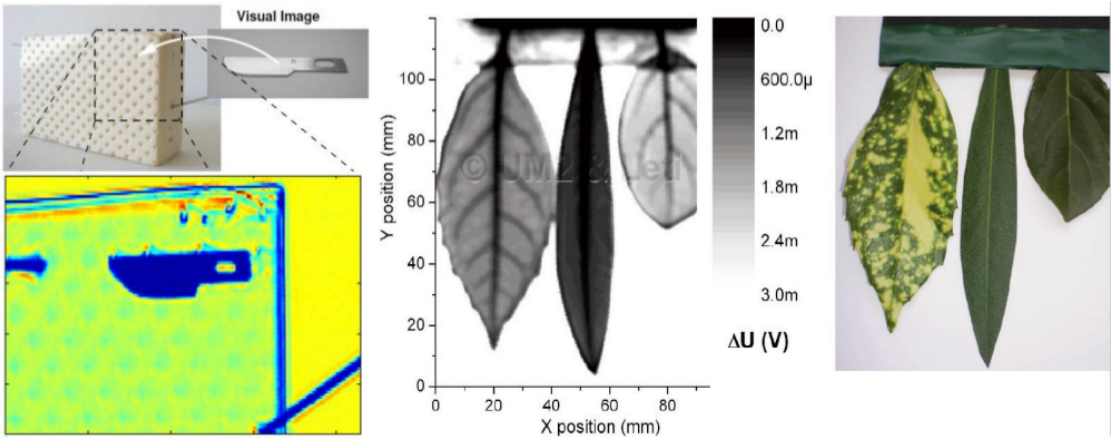


Figure 1.1 – Electromagnetic spectrum (From the Southeastern Universities Research Association).

1.1.1 Non-ionizing imaging

THz radiations have low photon energy: ~ 4 meV at 1 THz compared to several MeV for X-ray. Consequently, this kind of technology does not cause harmful photon ionization in biological tissues. This characteristic enables the use of this technology in safety and security areas.

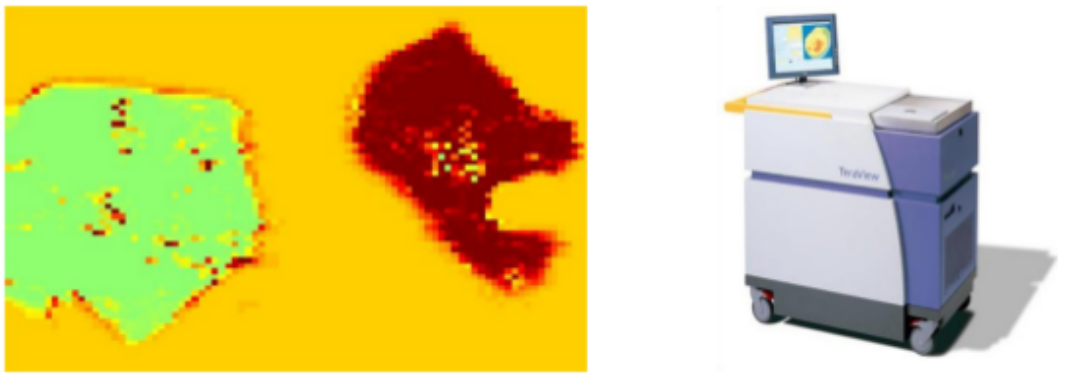
As a matter of example, THz imaging can detect objects such as guns or blades hidden inside packages, clothing, or foams [4]. (see figure 1.2(a)) This allows them to be used at airport or post offices for example. The fact that dielectrics are transparent for THz rays also allows the use of THz imaging in the field of non-destructive quality control. Biomedical THz imaging can also, for example, see the humidity level and structure of different living cells thanks to a THz image [5]. (see figure 1.2(b))



(a) (b)

Figure 1.2 – Terahertz image examples. (a) Hidden knife in mattress from [4] and (b) structure of leaves from [5].

Finally, medical imaging is also a promising field for THz applications. The major benefit comes from the safe energy levels of THz rays. Indeed, THz radiation was recently used in several works to detect various cancerous tissues as for example the one presented in figure 1.3 [6].



(a) (b)

Figure 1.3 – (a) THz image of colon tissue showing healthy tissue in green and cancerous tissue in dark red (fake colors). (b) Imaging performed by THz system from Teraview [6].

1.1.2 High-speed communications

THz and mm-wave have attractive bandwidth to realize high-speed communications with data rates above 10Gbit/s. Indeed, the demand for high data rate is increasing with new technologies and the congestion of traditional communication spectrum drives researchers to exploit the unlicensed THz bands between 100 GHz and 300 GHz [7–9].

Actual studies are mainly focused on exotic technologies. The main reason for this is the lack of output power of classic silicon technologies due to the proximity between operating frequency and cut-off frequency.

Nevertheless, some works present promising results in advanced silicon technologies [10–12]. As a matter of example, Yu *et al.* have presented in [12] a 165 GHz ON-OFF keying transmitter in a 65 nm CMOS technology.

1.2 Mm-wave and THz silicon oscillators

An oscillator is a circuit which produces a stable periodic signal without any input signal. The oscillator behavior can be explained using the simple model depicted in figure 1.4.

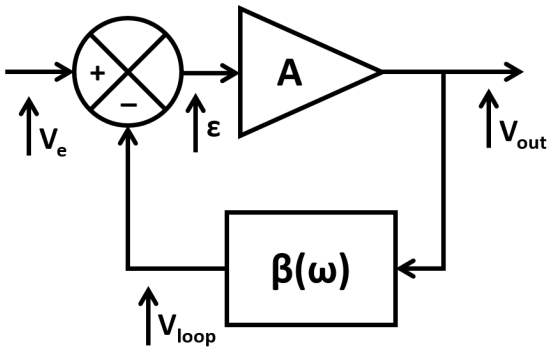


Figure 1.4 – Simple oscillator behavior model.

The closed loop transfer function of this model can be expressed as:

$$H(j\omega) = \frac{V_{out}}{V_e} = \frac{A}{1 + A\,\beta(j\omega)} \tag{1.1}$$

Thus, if it exists a specific frequency at which $A\,\beta(j\omega) = -1$, the closed loop gain is theoretically infinite and hence an output signal V_{out} can appear in the absence of input signal V_e. This condition is usually named the *Barkhausen criterion*.

Barkhausen criterion can be decomposed in two criteria. The phase Barkhausen criterion describes the phase condition to ensure the oscillation starting at a giving frequency. The gain Barkhausen criterion describes the minimum loop gain to maintain oscillations. These two criteria are represented by the following expressions:

$$|A| \geqslant \frac{A}{|\beta(j\omega)|} \tag{1.2}$$

$$arg\,(A\,\beta(j\omega)) = \pi \tag{1.3}$$

There are two main classes of integrated oscillators at mm-wave and THz frequencies. The first one generates directly the output frequency at fundamental while the second performs an indirect frequency generation by oscillating at a lower frequency and using harmonic recombination to generate an output signal at a high frequency.

1.2.1 Mm-wave and THz fundamental frequency generation

At mm-wave and THz frequency bands, the main used fundamental generation oscillator topologies are based on LC oscillators. These oscillators use passive resonators, such as LC tank, to create a band-pass filter and hence set the oscillation frequency.

There are different kinds of LC oscillator. In single mode, the two main used are the Colpitts and the Hartley oscillators, introduced in figure 1.5.

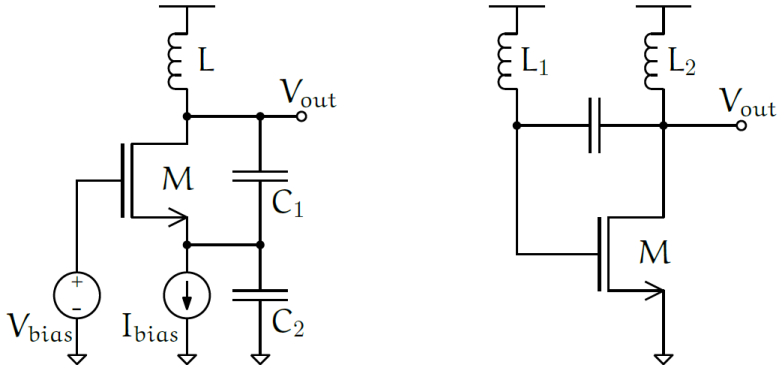


Figure 1.5 – Schematic examples of (a) Single mode Colpitts oscillator and (b) single mode Hartley oscillator.

The oscillation frequency of the Colpitts and Hartley oscillators can be expressed respectively as:

$$f_{osc|colpitts} = \frac{1}{2\pi\sqrt{\frac{C_1 C_2}{C_1+C_2}\cdot L}} \tag{1.4}$$

$$f_{osc|hartley} = \frac{1}{2\pi\sqrt{(L_1+L_2)\cdot C}} \tag{1.5}$$

These two single-mode oscillators can be adjusted to work in differential mode. The figure 1.6 presents the differential version of the Hartley oscillators.

This structure, also known as the cross-coupled oscillator, is the most used topology for fundamental THz and mm-wave oscillator [13, 14].

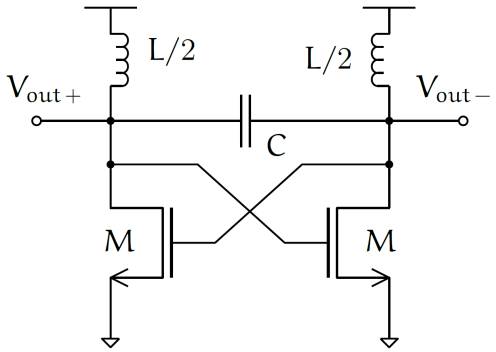


Figure 1.6 – Schematic differential cross-coupled oscillator.

1.2.2 Mm-wave and THz indirect frequency generation

Fundamental generation oscillators are limited by the transistors cut-off frequency. To overcome this limitation, indirect frequency generation oscillators have been proposed in literature. These oscillators use a technique named *harmonic recombination* to generate an output signal at a frequency beyond the transistor f_T/f_{max}.

The harmonic recombination techniques are based on the current recombination of multi-stage oscillators. This technique allows the N^{th} harmonic extraction of an N-stages oscillator.

Thus, to extract a signal at a frequency f_{osc}, one can use an N-stages oscillator with a fundamental frequency of f_{osc}/N. Nevertheless, the output level of the extracted signal is decreasing with the number of stages. For an N-stages oscillator, the extracted signal amplitude is theoretically reduced by a factor $1/2^{(N-1)}$. For this reason, the stage number of this kind of oscillator is usually limited at two or three (even if it exists some examples with four or five stages in literature [2, 15]).

Push-push oscillators

The two stages harmonic recombination oscillator is named *push-push* oscillator. This is probably the most used architecture in mm-wave and THz design due to its relatively high output power compared to architectures with a higher number of stages.

The push-push oscillator is usually based on a crossed-coupled architecture, as depicted in figure 1.7. However, instead of taking the output signal in differential mode on the two MOS drains, the output signal is probed at the common node beyond the two inductances. A $\lambda/4$ (@ f_{out}) TL performs an AC isolation between the supply and the output node.

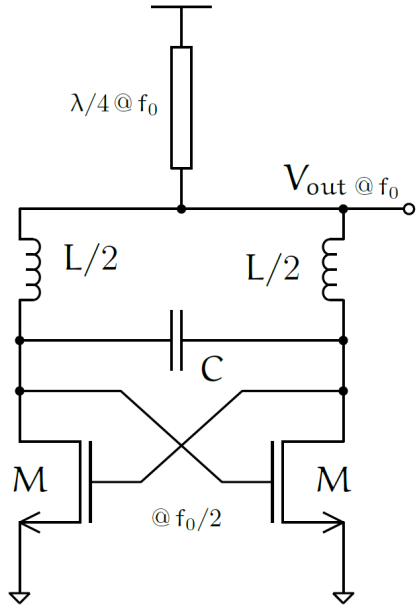


Figure 1.7 – Push-push oscillator architecture based on crossed-coupled oscillator.

This kind of architecture has been widely used in literature [16–21]. Indeed, its relatively high output power makes the push-push oscillator a good compromise between output power and oscillation frequency. However, with this kind of architecture, the oscillation frequency is limited to twice the cut-off frequency of the active device. To reach higher frequency, topologies with a higher number of stages are required.

Triple-push oscillators

The three stages harmonic recombination oscillator is named *triple-push* oscillator. After the push-push oscillator, it is the second most used architecture for mm-wave and THz frequency generation. This topology allows to reached frequencies up to three time the active device cut-off frequency. Nevertheless, this high output frequency is provided at the expense of output power which is reduced by a factor of 1/4.

A triple-push oscillator architecture is presented in figure 1.8. As for the push-push version, the triple-push oscillator output is located at the common node beyond the three inductances. Here again, a $\lambda/4$ (@ f_{out}) transmission line performs an AC isolation between the supply node and the output node. The three transistors are connected in an inductive-load ring oscillator. Thus, the ring loop oscillates at a frequency of $f_0/3$ and each drain voltages are phase-shifted by 120 degrees one respective to the others.

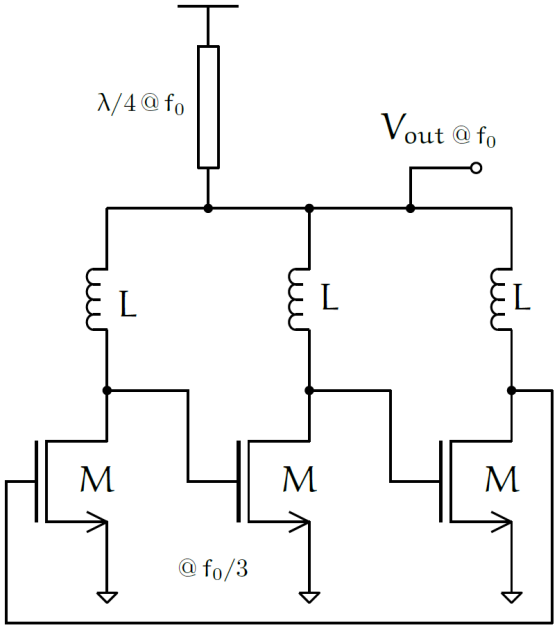


Figure 1.8 – Triple-push oscillator architecture.

Triple-push oscillators have been used in a lot of recent works [22–26]. Indeed, even if the output signal level is relatively low, the very high frequency reachable by this kind of architecture makes the triple-push a very attractive topology for mm-wave and THz frequency generation.

1.3 State-of-the-art in mm-wave and THz sources

To well understand the technological issues to tackle in mm-wave and THz frequency generation, a state-of-the-art study is necessary. This study will begin by focusing on oscillators state-of-the-art. Then, we will discuss locked frequency synthesizers.

1.3.1 State-of-the-art in mm-wave and THz oscillators

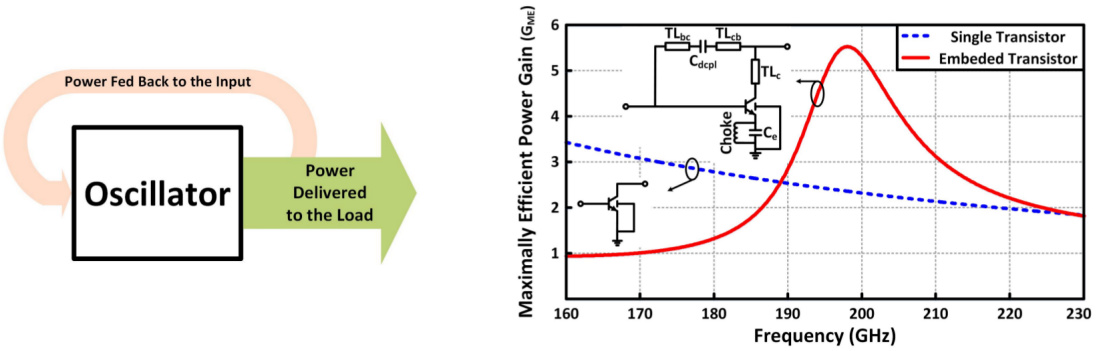
Fundamental mode oscillators

Silicon based fundamental oscillators with output frequency above 100 GHz started being published by 2006-2007 [13, 27]. When operating very close to active component cut-off frequency, the challenge is to maximize output power and DC-to-RF efficiency. At the beginning of this thesis work, mm-wave and THz fundamental generation were very rare because transistor performances of theses frequency were very limited.

Nevertheless, very recent works have demonstrated excellent performances near the transistors f_T/f_{max} [28, 29].

Let us focus on the one which presents, today, the best performances: [29] published in 2017 by Khatibi *et al.*.

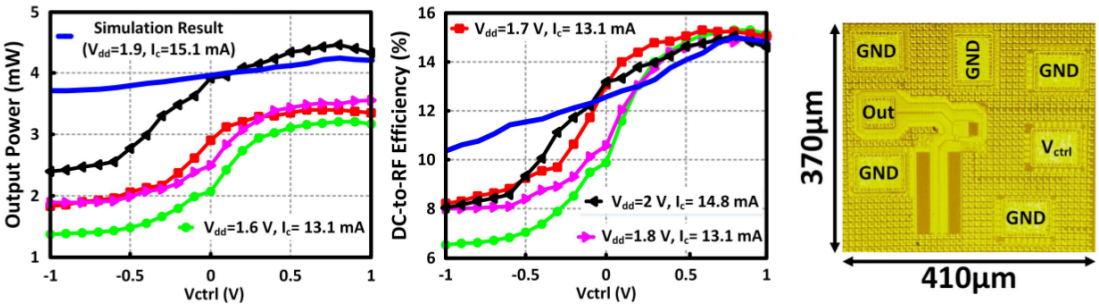
As presented in figure 1.9(a), in this work the oscillator is seen as a power amplifier which feeds part of its output power back to its own input and which delivers the excess power to the load. From this point of view, to design a high output power and high-efficiency oscillator the authors choose to maximize the *Maximally Efficient Power Gain* (see figure 1.9(b)).



(a) (b)

Figure 1.9 – (a) Oscillator seems as a looped back power amplifier. (b) Maximally Efficient Power Gain optimization. [29]

Using this new approach, [29] presents a 195 GHz fundamental oscillator with 6.5 dBm output power and a very high DC-to-RF efficiency of 15.3%, as depicted in figure 1.10. This work was designed in a 55 nm SiGe BiCMOS technology from ST Microelectronics which exhibit a f_{max} of $\approx$ 340 GHz. It is important to note that in this technology the active component has excellent performances at high frequencies. Such performances are not comparable to CMOS transistor performances at these frequencies.



(a) (b) (c)

Figure 1.10 – Simulated and measured (a) output power and (b) DC-to-RF efficiency under different bias condition. (c) Die photomicrograph. [29]

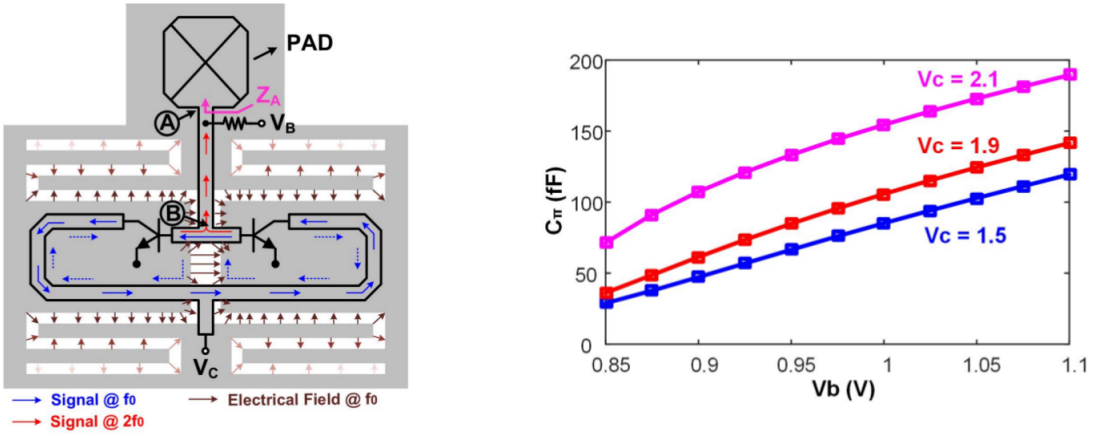
Push-push oscillators

As explained in the previous section, push-push architectures have been widely used to overcome cut-off frequency limitation. This kind of architecture has allowed output frequency of almost 200 GHz since 2005 in both BiCMOS and CMOS technologies [16, 19]. Later, in 2008, Seok *et al.* have proposed the very first oscillator beyond 300 GHz in a CMOS technology [18].

The main limitation of the push-push oscillator is its low DC-to-RF efficiency and its medium output power level coming from the second harmonic extraction. Since the beginning of this thesis work, mm-wave and THz push-push oscillators with good performance have been proposed [20, 21].

Let us focus on one of them which proposed an innovative architecture: [20] which was published in 2017 by Jiang *et al.*.

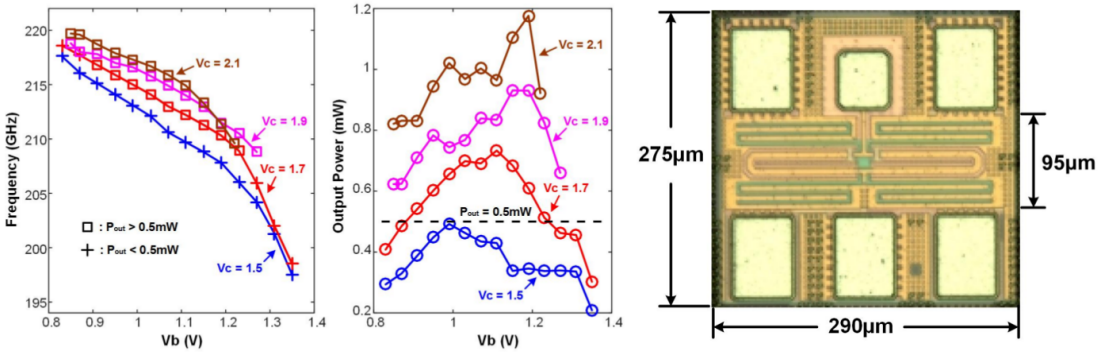
This oscillator is based on two self-feeding oscillator structures which are looped through a Return-Path Gap (RPG) in order to perform both DC isolation and second harmonic isolation, as shown in figure 1.11(a). The authors also used the bipolar base-emitter parasitic capacitance C_π (which is highly sensitive to bias point, as depicted in figure 1.11(b)) as a varactor to allow large frequency tuning range.



(a) (b)

Figure 1.11 – (a) Schematic of the presented push-push oscillator. (b) Bipolar base-emitter parasitic capacitance C_π at different bias points. [20]

Using this technique, [20] presents a 10.6% tuning range 210 GHz push-push oscillator with 1.4 dBm maximum output power and 2.4% maximum DC-to-RF efficiency, as shown in figure 1.12(a-b). This work was designed in a 130 nm SiGe BiCMOS technology from ST Microelectronics with a chip area of $290\times275\mu m^2$, as presented in figure 1.12(c).



(a) (b) (c)

Figure 1.12 – Measured (a) frequency and (b) output power under different bias point. (c) Die photomicrograph. [20]

Triple-push oscillators

Triple push oscillators have been also widely used in literature [24,26]. In 2011, Momeni and Afshari have proposed a systematic approach to design optimized triple-push oscillator [26]. Since this date, numerous works have proposed techniques to increase the output signal

power which is the main drawback of this kind of architecture.

As a matter of example, [23–25] proposed to couple several triple-push oscillators to extract a recombination of them and thus increase the output power. Nevertheless, these architectures still suffer from low DC-to-RF efficiency since DC consumption still increases with output power.

Triple-push oscillators have been also used in several locked frequency synthesis architectures, as presented in the next section.

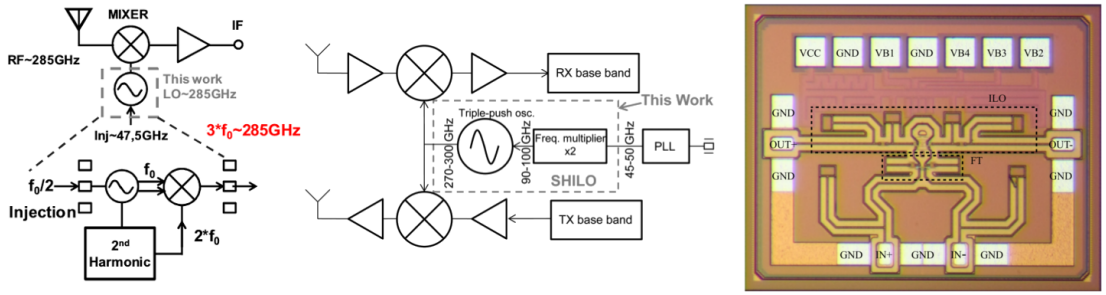
1.3.2 State-of-the-art in mm-wave and THz synthesis

Two main approaches are privileged for silicon-based integration of mm-wave and THz sources.

Frequency synthesis based on injection locked oscillators

The first one is based on sub-harmonic injection locked oscillator (ILO). As a matter of example:

- In [30] Guerra *et al.* present a push-push ILO follows by a mixer which takes the extracted second harmonic and multiplies it with the ILO fundamental. It results in a frequency multiplication by 6, as presented in figure 1.13(a). Nevertheless, output power (-19 dBm) and DC-to-RF efficiency (0.018%) are here very low.
- In [31], authors present an injection locked triple-push oscillator following a self-mixer to perform a frequency multiplication by 6, as shown in figure 1.13(b). But,



(a) (b) (c)

Figure 1.13 – (a) Push-push ILO based design proposed in [30]. (b) Triple-push ILO based design presented in [31] and (c) layout of the cascaded ILO introduced in [32].

the output power of -9 dBm and DC-to-RF efficiency of 0.25% are still low.

- In [32], more recently (in 2018), Li *et al.* presents a 200 GHz ILO based on differential Colpitts oscillator cascaded with a frequency tripler, performing a frequency multiplication by 3 as depicted on figure 1.13(c). This solution presents a good output power of 0 dBm for an Efficiency of 3.5%.

Frequency synthesis based on phase locked loops

The second approach performing silicon-based frequency synthesis at mm-wave and THz frequency ranges is based on a full phase locked loop (PLL). There are only two examples of silicon integrated PLL above 200 GHz in literature:

- The first one, introduced in 2014 by Chiang *et al.* in [33] proposed a classical PLL architecture using a 100 GHz voltage controlled oscillator (VCO). The VCO architecture is a three-stages inductively loaded ring oscillator. Thus, using a triple-push technique, the 300 GHz output frequency is probed at the common node of the ring stages which is isolated from supply thanks to a λ/4 TL. The figure 1.14 presents the architecture proposed in this work.

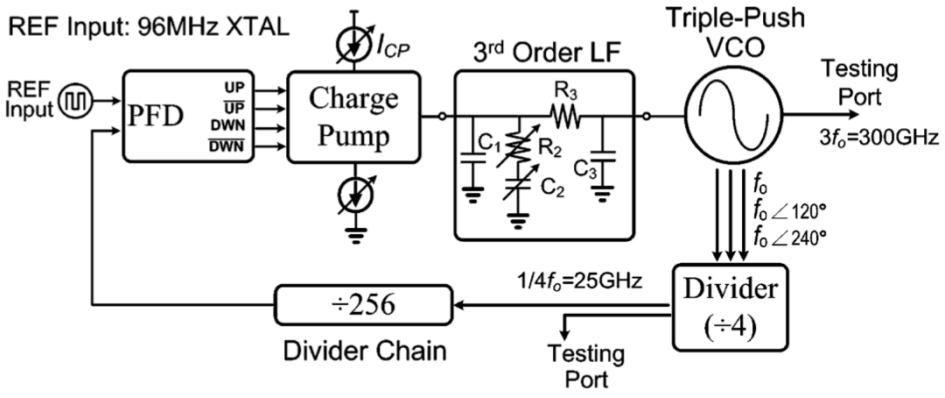


Figure 1.14 – Architecture of the 300 GHz frequency synthesis proposed in [33].

This work was the first silicon-based frequency synthesis published above 200 GHz with a center frequency of 290 GHz and a 7.9% locking range. The output power is -14 dBm for a 376 mW DC consumption resulting in a DC-to-RF efficiency of 0.01%. Finally, the phase noise was measured at -77.8 dBc/Hz at 100kHz offset and -82.5 dBc/Hz at 1MHz offset.

- The second example of silicon integrated PLL above 200 GHz was published in 2015 by Han *et al.* in [34] (and reused in 2016 by Jiang *et al.* in [35]). In this work,

the authors proposed a PLL architecture using four coupled 80 GHz VCOs. The VCOs architecture is based on a push-push oscillator to extract its second harmonic at 160 GHz. The locked signal at 160 GHz is then used to synchronize (locked by injection) four rows of four coupled 320 GHz oscillators (*i.e.* a 4×4 oscillator array). The 320 GHz oscillators are based on a push-push architecture similar to the one presented in [20] (see figure 1.11 in previous section). The architecture of the 320 GHz frequency synthesis is presented in figure 1.15.

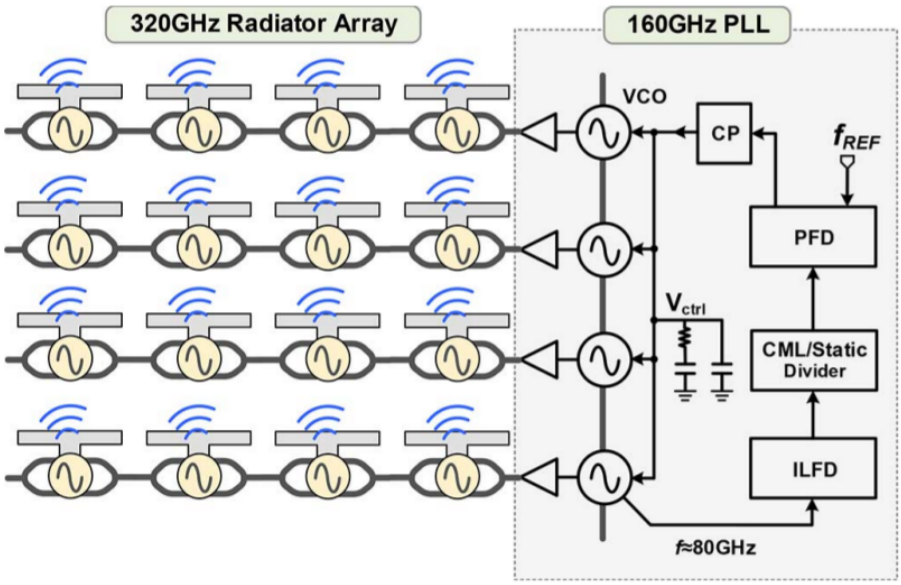


Figure 1.15 – Architecture of the 320 GHz frequency synthesis proposed in [34].

This work exhibits the best performances above 320 GHz in terms of output power (5.2 dBm) for a 610 mW DC consumption resulting in a DC-to-RF efficiency of 0.54%. The output signal center frequency is 317 GHz and its phase noise was measured at -79 dBc/Hz at 1MHz offset. The only limitation of this work is its tuning range which is limited to 200 MHz at 320 GHz (corresponding to 0.06%).

1.3.3 Challenges for future THz applications

The tables 1.1 and 1.2 summarize the state-of-the-art of silicon based mm-wave and THz frequency sources. It is notable that the main challenge in mm-wave frequency generation is to reach high DC-to-RF efficiency and high output power near or beyond the cut-off frequency.

Structures like triple-push (or more quad.) allow oscillating at very high frequency but

Ref.	Freq. (GHz)	P_{out} (dBm)	P_{DC} (mW)	DC-to-RF Efficiency	$PN_{@1MHz}$ (dBc/Hz)	Tuning Range	Technology	Year	Type	Phase Locked?
[13]	140	-19	9.6	0.13 %	-93**	0.86 %	90nm CMOS	2006	Fund.	No
[26]	104	-2.7	28	1.92 %	-93.3	N/A	130nm CMOS	2011		
[26]	121	-3.5	21	2.13 %	-88	N/A	130nm CMOS	2011		
[14]	219	-3.0	24	2.08 %	-77.4	N/A	65nm CMOS	2016		
[28]	176	4.8	25.8	11.7 %	-101.7	0.34 %	130nm SiGe	2017		
[29]	195	6.5	29.2*	15.3 %	-98.6	1.1 %	55nm SiGe	2017		
[19]	190	-4.5	215	0.16 %	-73	3.8 %	140nm SiGe	2005	Push push	
[16]	192	-20	16.5	0.06 %	-100**	0.68 %	130nm CMOS	2006		
[17]	202	-7.2	30	0.64 %	-87	3.5 %	130nm SiGe	2013		
[17]	212	-7.1	30	0.65 %	-92	2.8 %	130nm SiGe	2013		
[20]	210	1.4	56.5*	2.40 %	-87.5	10.6 %	130nm SiGe	2016		
[21]	215	5.6	79	4.60 %	-94.6	0.65 %	65nm CMOS	2017		
[26]	256	-17	71	0.03 %	-88	N/A	130nm CMOS	2011	Triple push	
[26]	482	-7.9	61	0.27 %	-76	N/A	65nm CMOS	2011		
[26]	482	-9.0	27.5	0.46 %	-76	N/A	65nm CMOS	2011		
[24]	288	-1.5	275	0.26 %	-87	1.4 %	65nm CMOS	2013		
[22]	200	-8.8	28.8	0.46 %	N/A	N/A	65nm CMOS	2016		
[25]	298	0.9	235	0.51 %	-79	1.7 %	65nm CMOS	2016		
[23]	210	-6.0	28.6	0.88 %	-88	5.1 %	90nm CMOS	2018		
[15]	290	-1.2	325	0.23 %	-78	4.5 %	65nm CMOS	2012	Quad.	
[15]	320	-3.3	339	0.13 %	-77	2.6 %	65nm CMOS	2012		

* Estimated from provided data, ** @10MHz offset.

Table 1.1 – State-of-the-art of silicon based mm-wave and THz oscillators per type of oscillator, the references are reported upon their publication year.

Ref.	Freq. (GHz)	P_{out} (dBm)	P_{DC} (mW)	DC-to-RF Efficiency	$PN_{@1MHz}$ (dBc/Hz)	Tuning Range	Technology	Year	Type	Phase Locked?
[30]	285	-19	71	0.02 %	-80.5 †	1.7 %	65nm CMOS	2013	ILO	Yes
[31]	285	-9.0	52	0.24 %	-105 †	10.8 %	55nm SiGe	2015		
[32]	195	0.0	28.8	3.50 %	-117.5*†	5.4 %	130nm SiGe	2018		
[32]	195	-3.7	21.6	2.00 %	-117.5*†	12.3 %	130nm SiGe	2018		
[33]	290	-14	376	0.01 %	-82.5	7.9 %	90nm SiGe	2014	PLL	
[34]	317	5.2	610	0.54 %	-79	0.06 %	130nm SiGe	2015		

* Estimated from provided data, † Depends on reference phase noise.

Table 1.2 – State-of-the-art of silicon based mm-wave and THz frequency synthesis solutions.

always at the expense of a huge DC consumption and thus a very low DC-to-RF efficiency. Moreover, phase noise performances of this kind of structures are not very good.

Push-push structures have suffered from the same problems during a long time. Nevertheless, very recent works exhibit several alternatives with improved performances. Indeed, today's best CMOS push-push oscillator ([21], published in 2017) exhibits a very high output power of 5.6dBm for a 4.6% efficiency. This with the measured -95 dBc/Hz at 1MHz from the carrier makes this topology still very interesting for frequency generation above 200 GHz. These results were obtained thanks to optimizations of large-signal transistor behavior to boost harmonic extraction.

Finally, fundamental oscillators helped by recent sub-micron silicon technology improvements, present the best today's output power and efficiency. Indeed, [29] proposed in 2017 a single transistor oscillator achieving 6.5 dBm output power for a 15.3% DC-to-RF efficiency and a phase noise of -98.6 dBc/Hz at 1MHz offset. These excellent results were obtained thanks to an innovative approach. Indeed, by considering the oscillator as a looped back unstable power amplifier, authors choose to maximize an old figure of merit: the Maximally Efficient Power Gain (G_{ME}). Unlike the maximum available gain (G_{MA}), which is defined only for stable network, G_{ME} is defined in order to have a power gain which remains finite and well-behaved for both stable and unstable network.

Regarding these results, it appears clear that to design high efficiency and high output power oscillators at mm-wave and THz frequencies the most efficient way is to optimize the active part as a looped back power amplifier as in [20, 28, 29]. Moreover, large-signal transistor behavior must be fully understood to allow an optimized power extraction and hence maximized the output power and the efficiency [21]. These design techniques helped by recent sub-micron technologies improvements should allow reaching excellent performances at mm-wave and THz operation frequencies.

Concerning the phase locked systems, the same limitations appear. Injection-locked oscillators have presented very interesting behavior for this kind of systems and must be investigated. But to guarantee good locked system performances (especially in terms of output power and efficiency) it appears evident that research must first focus on good oscillator performances.

It is important to note that, depending on the targeted application, different parameters must be optimized. Indeed, in some mm-wave/THz applications, especially for sensing, sources do not need to be locked as the phase noise is not critical. For this kind of systems, only the output power and the efficiency have to be maximized. On the other hand, for very high data rate communications with complex modulations, the phase noise is critical and locked sources are mandatory.

1.4 Chapter conclusion

This chapter has introduced the context of silicon-based mm-wave and THz applications, from imaging to high data rate application. Several mm-wave and THz oscillator topologies have been introduced and intrinsic limitations have been highlighted.

Following the state-of-the-art analysis, it appears that to guarantee good system performances at mm-wave and THz operation frequencies (especially in terms of output power and efficiency) research must first focus on oscillator performances.

Recent techniques based on the large-signal optimization of the oscillator active part (seen as a loop power amplifier) provide good results at mm-wave and THz operation frequencies. These new design techniques must be investigated to take full advantage of sub-micron technologies possibilities.

Finally, for some applications like very high data rate communications with complex modulations, the source phase-noise performances are very critical. Thus, phase-noise optimization techniques must be investigated.

In this work, we proposed to focus on the realization of a fundamental distributed oscillator. This oscillator is aimed to be synchronized as an injection-locked oscillator. Thus, in the next chapter, injection-locked oscillators will be studied in detail.

2 An Alternative: The Injection Locked Distributed Oscillator

Injection-Locked Oscillators (ILO) take advantage of synchronization phenomenon to realize innovative frequency synthesis architectures. A good understanding of the injection phenomenon is essential to properly predict the ILO behavior. Its properties make Distributed Oscillators (DO) good candidates for mm-wave and THz frequency generation for advanced CMOS technologies.

After a presentation of the ILO and its properties, this chapter will present a methodology to fully optimize an ILO by taking into account its architecture specificity. Finally, DO for operation close to f_{max} will be presented and previous theory will be extended to the study of Injection-Locked Distributed Oscillators.

2.1 The injection locked oscillator

A classic oscillator is a circuit which produces a periodic signal without any input signal. The Injection-Locked Oscillator (ILO) is a particular case of oscillator since it has a synchronization input, as depicted in Figure 2.1.

In the absence of an input locking signal, the ILO behaves like a classic oscillator and oscillates at its free-running frequency f_0. If a small-amplitude periodic signal is applied to the synchronization input, and if its frequency f_{inj} is close to f_0, then the ILO starts to oscillate at the injected signal frequency. This is the injection locking phenomenon.

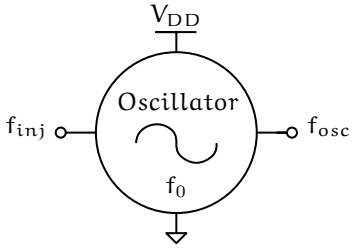


Figure 2.1 – Oscillator with a synchronization input.

2.1.1 Presentation of the injection locking phenomenon

The injection locking (or oscillators synchronization) is a property common to all oscillators whether mechanical, electrical or even biological [36]. This phenomenon was discovered by Christiaan Huygens in the 17th century when he noticed that clocks which did not beat the second at same moment can be synchronized if they are fixed on the same wall [37, 38]. Another example of synchronized oscillator is the human. Indeed, it has been demonstrated that the proper life cycle of human is 25 to 27 hours depending on the individual. However, the rotation of the earth forces our life cycle to have a period of about 24 hours [39].

The injection locking is a phenomenon well-known by Radio Frequency (RF) and Millimeter-Wave (mm-wave) communities. Indeed, this property can be an obstacle for the realization of some RF systems. For example, in the broadband transceiver depicted in Figure 2.2a, the transmitter local oscillator (LO) is locked by a local crystal while the receiver LO is locked by the incoming data and hence potentially at a slightly different frequency. Thus, pulling between the two LOs may appear due to substrate coupling. Similarly, the power amplifier (PA) output of the RF transceiver presented in Figure 2.2b contains large spectral components close to the carrier ω_{LO}. Thus, leakage through the substrate may cause pulling with the LO.

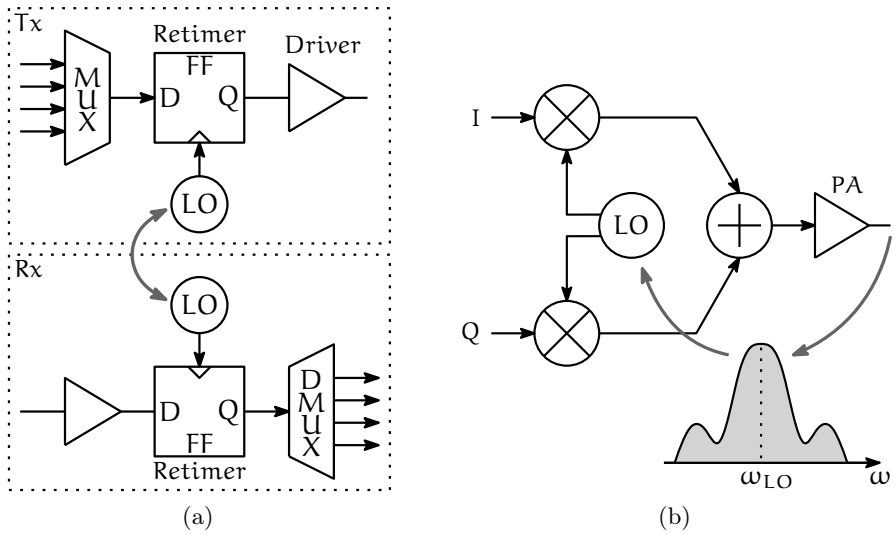


Figure 2.2 – Oscillator pulling in (a) broadband transceiver and (b) RF transceiver.

ILOs are attractive for the design of several RF integrated circuits like: Sub-Harmonic ILOs (SHILO) [31, 40–43], Injection Locked Frequency Dividers (ILFD) [44–48] or Coupled Oscillators Array (COA) [34, 49–51]. Moreover, ILOs properties offer alternatives to classical Phase Locked Loop (PLL) solutions for frequency synthesis under certain operation frequency and phase-noise/jitter constraints [52–56].

2.1.2 ILO properties and their utilization in frequency synthesis

The ILOs have many interesting properties. Here we draw a non-exhaustive list, focused on the most important properties for frequency synthesis design:

- As explained at the beginning of this chapter, an ILO is able to be synchronized by a periodic signal if its oscillation frequency is close to the ILO's free-running frequency ($f_0 \approx f_{inj}$). This is the "synchronization on fundamental".
- An ILO is also able to be synchronized by a periodic signal whose oscillation frequency is close to one of the ILO's harmonics. This means that an ILO is able to perform frequency divisions by an integer ($f_0 \approx f_{inj}/n$). This is the "harmonic synchronization".
- Furthermore, an ILO is able to be synchronized by a periodic signal of which one of the harmonics is close to the ILO's free-running frequency. This means that an ILO

is also able to perform frequency multiplication by an integer ($f_0 \approx n \cdot f_{inj}$). This is the "sub-harmonic synchronization".

- The acquisition time of an ILO is significantly lower than that of a classic PLL [57–59]. This means that an ILO is able to follow complex frequency/phase modulations.

- Last but not least, in its locking range (LR), the ILO copies the injected signal phase-noise (within a multiplication or division factor) [57, 59].

All its properties make the ILO a key circuit of innovative frequency synthesis architectures. Thereafter, we will see three possible ILO use cases in frequency synthesis upon the different ILO properties.

Synchronization on fundamental use case

Recent wireless communication systems use transceiver array with beamforming techniques to reach very high data rate performances [34, 49–51]. Beamforming requires controllable identical phase-shift between adjacent RF paths in the array. However, phase-shifters at mm-wave frequencies suffer from their low performances in terms of frequency range, losses, and linearity. To overcome these issues, [49] proposed to use injection locked COA.

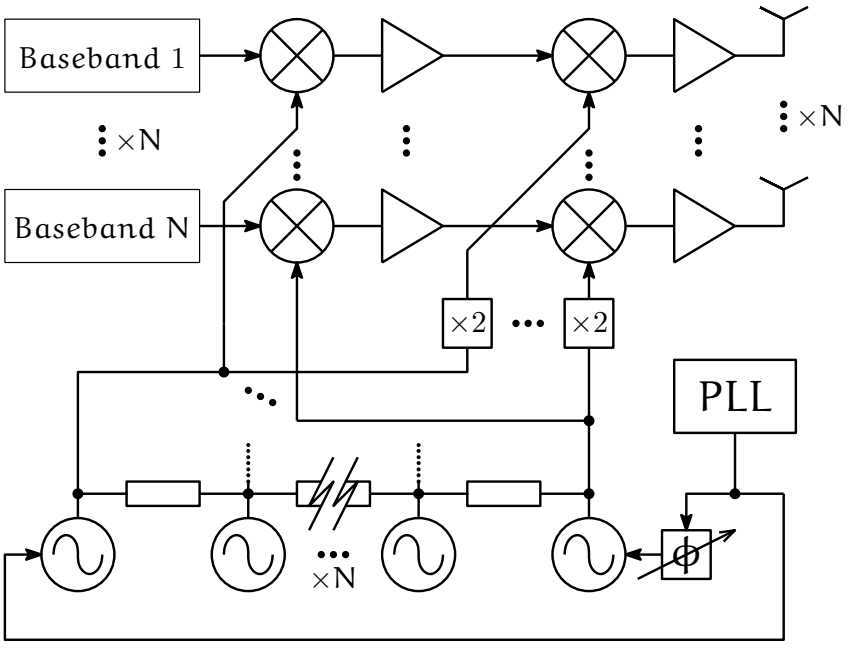


Figure 2.3 – Beamforming transmitter using injection locked COA.

The Figure 2.3 depicts the transceiver used in [49]. The oscillators at both ends of the array are synchronized to respectively the local oscillator and its phase-shifted ϕ copy. The resulting phase-shift between the N adjacent oscillator outputs is given by $\Delta\phi = \frac{\phi}{N-1}$. This technique has the big advantage of using only one phase-shifter instead of $N-1$. Moreover, the COA provides a continuous tuning of phase shift value whereas classic beamforming systems perform only discrete values.

Harmonic synchronization use case

The need for high-frequency synthesis in recent systems involves many challenges, in particular with the PLL feedback loop frequency dividers (FD). Broadband nature of FDs makes them huge energy consumers, especially at high operation frequency [44]. Furthermore, classic flip-flop like digital FDs cannot be used beyond a certain frequency.

A possible solution is to use an ILO locked on one of its harmonics as an FD. This kind of circuit is named Injection-Locked Frequency Divider (ILFD).

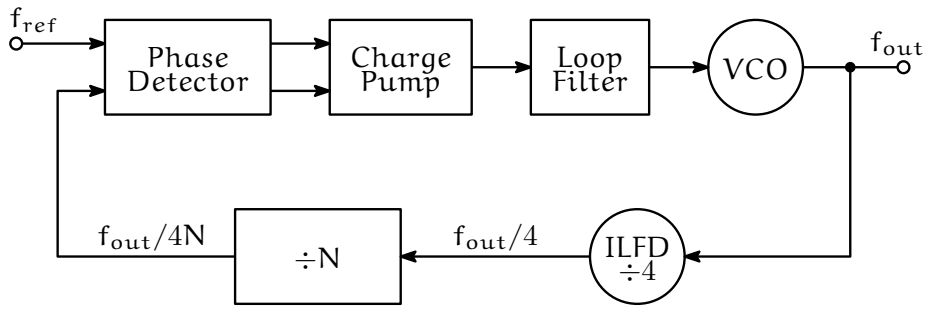


Figure 2.4 – Frequency synthesis using an ILO as divider by 4.

The Figure 2.4 represent a frequency synthesis structure using an ILFD. The advantage of this kind of structure was demonstrated in several works such as [44–48]. As a matter of example, in [44], the first stage of frequency division, (which is ILO based) has a power consumption equal to 1/8 of the second stage consumption (flip-flop based).

Nevertheless, to ensure a good behavior of the ILFD, the VCO frequency range and the LR of the ILO must coincide. Which means that the LR of the ILFD is a key parameter and must be totally controlled. Finally, the VCO of this kind of typology sustains the major part of constraints linked to frequency synthesis. This makes difficult to optimize the phase-noise/consumption tradeoff for high-frequency synthesis.

Sub-harmonic synchronization use case

The sub-harmonic synchronization allows stable frequency synthesis driven by a low-frequency PLL. The Figure 2.5 depicted a frequency synthesis using a SHILO. The harmonic 4 of the PLL output signal locks the ILO and thus performs a multiplication by 4.

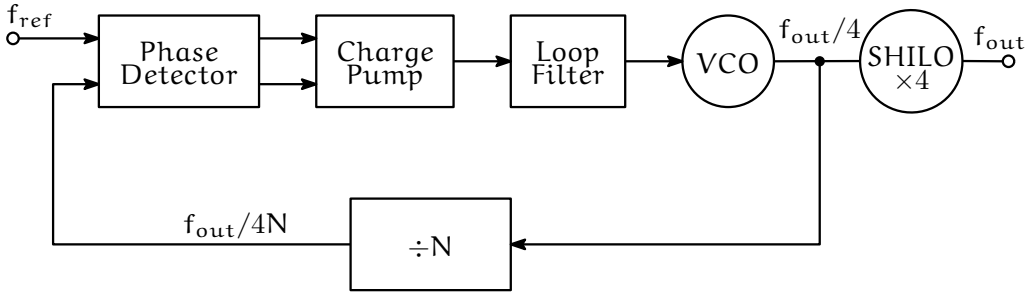


Figure 2.5 – Frequency synthesis using a SHILO.

This frequency synthesis structure has several advantages. First, global power consumption is reduced. Indeed, the low operating frequency of the PLL reduces the constraints in all its blocks. In addition, the ILO copies the injected signal phase-noise (within a multiplication factor $20\log(N)$), which means that the phase-noise constraint is reported to a lower frequency PLL. And, as demonstrated by Lesson [60], VCO phase-noise is proportional to the frequency squared. Thus, it is easier to optimize low-frequency oscillator phase noise than higher frequency ones. However, the VCO tuning range must be included in the ILO locking range to ensure correct operation. Thus, the LR remain critical for this kind of synthesis.

In sum, this topology is very attractive for very high-frequency synthesis. The reduced power consumption and the phase noise copy property makes the SHILO an excellent candidate for mm-wave and THz frequency source. Nevertheless, the LR of the ILO must be totally controlled. Consequently, a theoretical study is essential to anticipate the LR and the dynamic behavior of the oscillator under injection.

2.1.3 Previous ILO theory studies

The main design challenge in ILOs is the LR (i.e. the range of injected frequency across which injection locking holds). To improve LR, several theoretical approaches can be found in literature [59, 61–70]. The two commonly used are the Adler's theory [61] (developed in 1946 and nicely reviewed by Paciorek in 1965 [63] and Razavi in 2004 [66]) and the Huntoon-Weiss theory [62] (introduced in 1947 and revisited by Badets in 2000 [59]).

Adler's theory and its reviewed versions

The Adler's theory [61] is an intuitive approximation in the case of LC oscillators. It is based on the equation of the phase difference between the synchronization signal and the system response. In this analysis, the three following assumptions are made:

1. The locking signal frequency must be close to the oscillator free-running frequency.
2. The time constant involved in the amplitude control mechanism must be short compared to one beat cycle.
3. The locking signal amplitude must be small compared to the output voltage amplitude.

Adler then presents a model based on differential equations and used it to investigate pulling effect which appears out of the ILO locking range.

In 1965, Paciorek proposed a modification of Adler's theory by keeping only the two first assumption [63]. Thus, this new approach extends the theory to the case where locking signal amplitude is close to the oscillator output amplitude.

Finally, in 2004, Razavi proposed a graphical interpretation of the extended Adler's theory [66]. Let us develop here this study by considering the conceptual oscillator shown in Figure 2.6a. The tank operates at the resonance frequency $\omega_0 = 2\pi f_0 = \frac{1}{\sqrt{LC}}$. A total feedback loop phase-shift of 2π is achieved thanks to an ideal inverter following the tank.

If, as depicted in Figure 2.6b, an additional phase-shift ϕ_0 is inserted in the loop, the circuit can no longer oscillate at ω_0. Thus, the oscillation frequency must change to a new value ω_1 to cancel the effect of ϕ_0, as illustrated in Figure 2.6c.

Now let's suppose that ϕ_0 is obtained by adding a sinusoidal current I_{inj} to the drain current of M1. If the amplitude and phase (θ) of I_{inj} are chosen properly, the circuit starts to oscillate at ω_{inj}. This is the injection locking. In order to determine the LR we examine the phase diagram of Figure 2.6e. It can be shown that

$$\sin(\phi_0) = \frac{I_{inj}}{I_T}\sin(\theta) = \frac{I_{inj}\sin(\theta)}{\sqrt{{I_{osc}}^2 + {I_{inj}}^2 + 2\,I_{osc}\,I_{inj}\cos(\theta)}} \tag{2.1}$$

, where I_{osc} and I_T represents the tank current in the free-running and when locked, respectively. This equation reaches a maximum of $\sin(\phi_{0,max}) = \frac{I_{inj}}{I_{osc}}$, if $\cos(\theta) = -\frac{I_{inj}}{I_{osc}}$, as represented in Figure 2.6f. To determine the value of ω_{inj} corresponding to this case,

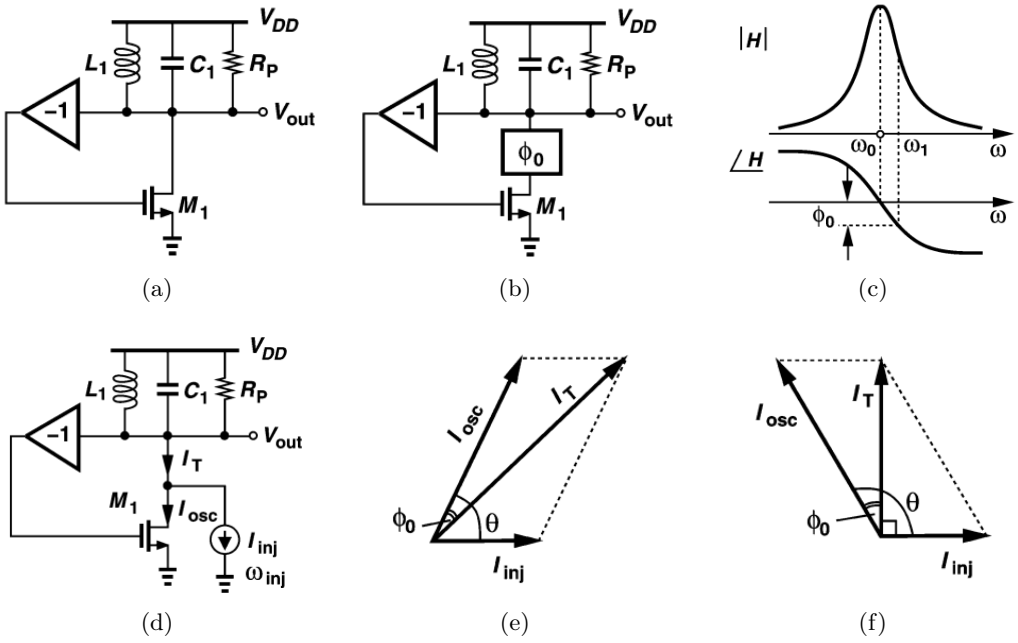


Figure 2.6 – (a) Conceptual oscillator. (b) Frequency shift due to additional phase-shift. (c) Open-loop characteristics. (d) Frequency shift by injection. (e) and (f) Phase difference between input and output for two values of $|\omega_{inj} - \omega_0|$. (Figures from [66])

we recognize from Figure 2.6f that

$$\tan(\phi_0) = \frac{I_{inj}}{I_T} = \frac{I_{inj}}{\sqrt{{I_{osc}}^2 - {I_{inj}}^2}}. \tag{2.2}$$

Moreover, the LC tank impedance can be written as:

$$Z(j\omega) = \frac{R}{1 + jQ\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)}.$$

Thus an approximate expression of the tank phase-shift near resonance is given by

$$\tan(\phi) = -Q\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right) \underset{\omega_0}{\sim} 2Q\left(\frac{\omega_0 - \omega}{\omega_0}\right). \tag{2.3}$$

From equations (2.2) and (2.3) follows that

$$(\omega_0 - \omega_{inj}) = \frac{\omega_0}{2Q}\frac{I_{inj}}{I_{osc}}\frac{1}{\sqrt{1 - \frac{{I_{inj}}^2}{{I_{osc}}^2}}}. \tag{2.4}$$

Equation (2.4) is the result obtain by Paciorek using a different approach. Note that (2.4) is the "one-side" LR. The "full" LR is then given by $\Delta\omega = 2\left(\omega_0 - \omega_{inj}\right)$.

If $I_{inj} \ll I_{osc}$, as in Adler's original work, then (2.1) is reduces to

$$\sin\left(\phi_0\right) \approx \frac{I_{inj}}{I_{osc}} \sin\left(\theta\right) \tag{2.5}$$

implying that ϕ_0 is small and $\sin\left(\phi_0\right) \approx \tan\left(\phi_0\right)$. Equations (2.3) and (2.5) therefore give

$$\sin\left(\theta\right) \approx \frac{2\,Q}{\omega_0} \frac{I_{osc}}{I_{inj}} \left(\omega_0 - \omega_{inj}\right).$$

From Figure 2.6f it is evident that if $I_{inj} \ll I_{osc}$, then $\theta \to \frac{\pi}{2}$. Then the phase difference in this case can be given by

$$\left(\omega_0 - \omega_{inj}\right) = \frac{\omega_0}{2\,Q} \frac{I_{inj}}{I_{osc}}. \tag{2.6}$$

Equation (2.6) is the result obtained by Adler in 1946.

The main limitation of this theory is that it applies only to LC oscillators. Nevertheless, as Razavi showed in the second part his publication, this theory is very interesting to study the ILO pulling effect.

Huntoon-Weiss theory

The Huntoon-Weiss theory [62] is the second commonly used approach to optimize the LR. Presented in 1947, this theory emerges by the simplicity of its calculations and its general character. Let's consider the oscillator shown in Figure 2.7 with free-running frequency f_0 and loaded by the impedance Z. The voltage source V_{inj} represents a sinusoidal injection source oscillating f_{inj} in series with Z.

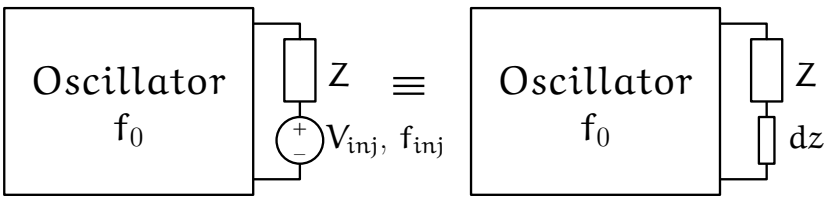


Figure 2.7 – Representation of oscillator for Huntoon-Weiss theory.

This theory is based on two fundamental assumptions:

1. all oscillators that have frequency and amplitude as continuous functions of the load are likely to experience the synchronization phenomenon,
2. if the disturbance is low and its frequency is close to f_0, then the synchronization source can be replaced by a small variation of the load impedance.

In their seminal publication, Huntoon and Weiss showed that it is possible to determine the ILO parameters based on elasticity coefficients defined as small variation of amplitude A and frequency f for a small change of the load impedance $dz = r + j\,x$:

$$A_r = \left.\frac{\partial A}{\partial r}\right|_{dz=0} \qquad A_x = -\left.\frac{\partial A}{\partial x}\right|_{dz=0}, \tag{2.7}$$

$$f_r = \left.\frac{\partial f}{\partial r}\right|_{dz=0} \qquad f_x = -\left.\frac{\partial f}{\partial x}\right|_{dz=0}. \tag{2.8}$$

Complex amplitude and frequency elasticity coefficients, (respectively E_A and E_f) are defined as:

$$E_A = |E_A|\, e^{j\alpha} = A_r + j\,A_x = \sqrt{A_r + A_x}\, e^{j\alpha}, \tag{2.9}$$

$$E_f = |E_f|\, e^{j\beta} = f_r + j\, f_x = \sqrt{f_r + f_x}\, e^{j\beta}. \tag{2.10}$$

Amplitude A and frequency f 1st order Taylor's development for small variation of the load impedance give relations between amplitude (respectively frequency), elasticity coefficients and impedance variations:

$$A - A_0 = r\,A_r - x\,A_x = Re\,(E_A\, dz)\,, \tag{2.11}$$

$$f - f_0 = r\, f_r - x\, f_x = Re\,(E_f\, dz) \tag{2.12}$$

, where A_0 and f_0 are respectively the oscillator free-running amplitude and frequency.

The locking signal V_{inj}, oscillating at f_{inj}, can be expressed as:

$$V_{inj} = \left|V_{inj}\right|\, e^{j\,2\pi\, f_{inj}\, t}. \tag{2.13}$$

The current I through the load and the injection source is given by:

$$I = |I|\, e^{j\,\phi_{osc}(t)}, \text{ with } \phi_{osc}(t) = 2\pi \int_{-\infty}^{t} f(u)\, du \tag{2.14}$$

, with f the instantaneous ILO oscillating frequency. By taking the second assumption, the injected signal amplitude is considered small enough not to result in significant changes in current amplitude. Under these conditions we can , with sufficient accuracy, represent I by its initial values I_0. The expression of the impedance dz is therefore given by:

$$dz = \frac{V_{inj}}{I} = \frac{|V_{inj}|}{|I_0|} e^{j\,\phi} = r + j\,x \tag{2.15}$$

$$\phi\,(t) = 2\pi \left(f_{inj}\,t - \int_{-\infty}^{t} f\,(u)\ du \right). \tag{2.16}$$

From (2.11), (2.12) and (2.15) we may thus write:

$$A - A_0 = \frac{|E_A|\,|V_{inj}|}{|I_0|} \cos\,(\phi + \alpha)\,, \tag{2.17}$$

$$f\ -\ f_0 = \frac{|E_f|\,|V_{inj}|}{|I_0|} \cos\,(\phi + \beta)\,. \tag{2.18}$$

It is notable here that in typical oscillators $A_x \ll A_r$, while $f_x \ll f_r$. Thus, α is usually very small, and β is nearly $\frac{\pi}{2}$.

In order to establish the locking equation, let's take the time derivation of (2.16):

$$\frac{1}{2\pi}\frac{d\phi}{dt} = f_{inj} - f = \left(f_{inj} - f_0\right) - \left(f - f_0\right). \tag{2.19}$$

By substituting (2.18) in previous equation it follows:

$$\frac{1}{2\pi}\frac{d\phi}{dt} = \left(f_{inj} - f_0\right) - \frac{|E_f|\,|V_{inj}|}{|I_0|} \cos\,(\phi + \beta)\,. \tag{2.20}$$

This differential equation gives the evolution of the oscillator signal phase during the synchronization process simply as a function of the frequency compliance coefficient E_f modulus and phase.

When the oscillator is locked, its phase follows the injected signal phase. So, since ϕ is defined as the difference between the injected signal phase and the oscillator instantaneous phase, $\frac{d\phi}{dt} = 0$ and then (2.20) gives:

$$\left(f_{inj} - f_0\right) = \frac{|E_f|\,|V_{inj}|}{|I_0|} \cos\,(\phi + \beta)\,. \tag{2.21}$$

Considering that the cosine function varies between -1 and 1, the oscillator frequency

locking range is given by:

$$\Delta f = 2\frac{|E_f|\left|V_{inj}\right|}{|I_0|}. \tag{2.22}$$

Starting from this result, Huntoon and Weiss demonstrate that it is possible to find the ILO parameters as a function of LR and elasticity coefficients. As a matter of example, the locking time is therefore given by:

$$\tau = \frac{1}{2\pi\sqrt{\left(\frac{\Delta f}{2}\right)^2 - \left(f_{inj} - f_0\right)^2}} \tag{2.23}$$

, and the amplitude variation in the LR is given by:

$$A - A_0 = \frac{|E_A|\left|V_{inj}\right|}{|I_0|}\cos\left(\arccos\left(\frac{2\left(f_0 - f_{inj}\right)}{\Delta f}\right) - \pi + \alpha - \beta\right). \tag{2.24}$$

The Huntoon-Weiss theory is interesting because all ILO parameters are function of the LR, elasticity coefficients and oscillator quiescent point. In other words, the study of injection locking is reduced to the examination of the frequency and amplitude variations as a function of load impedance change.

In 2000, Badets proposed a modification of Huntoon-Weiss theory by applying this study for the case of locking signal amplitude close to the oscillator output amplitude [59].

2.2 Theoretical consideration for harmonic ILOs

2.2.1 Parallel injection versus series injection

The main drawback of Huntoon-Weiss theory is that it does not provide a clear correlation between its principal parameters and ILO circuit parameters. In this section, a modification of this theory will be presented. This new approach is based on three following assumptions:

1. All harmonic oscillators are likely to experience synchronization phenomenon.
2. The injection source does not have to be applied on the load, which is the case in Huntoon-Weiss theory, but anywhere in the oscillator tank.
3. If the injection source amplitude is low and its frequency is close to f_0, then its influence can be modeled as a small signal variation of the impedance, or respectively admittance, which is presented as a load to the injection source.

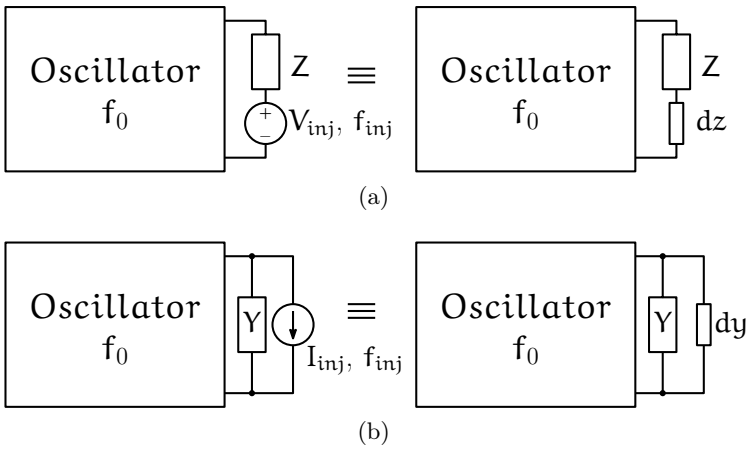


Figure 2.8 – Representation of oscillator for (a) proposed series injection, (b) proposed parallel injection.

Two practical cases are then possible and will be analyzed. The first case, a voltage injection source in series with an oscillator element Z will be replaced by a small impedance variation $dz = r + jx$ of this element. Figure 2.8a shows the equivalent schematic in the case of series injection. In the second case, illustrated in Figure 2.8b, a current injection source is connected in parallel with an oscillator element Y. Its influence will be modeled as a small variation $dy = g + jb$ of the oscillator element admittance.

For both cases, new elasticity coefficients are defined as small variation of amplitude A and frequency f for small change of Z impedance dz (respectively Y admittance, dy). For series injection case, equations (2.7) and (2.8) can be used, assuming that Z is no longer the load but an oscillator element. For parallel injection case, elasticity coefficients are given by:

$$A_g = \left.\frac{\partial A}{\partial g}\right|_{dy=0} \qquad A_b = -\left.\frac{\partial A}{\partial b}\right|_{dy=0}, \tag{2.25}$$

$$f_g = \left.\frac{\partial f}{\partial g}\right|_{dy=0} \qquad f_b = -\left.\frac{\partial f}{\partial b}\right|_{dy=0}. \tag{2.26}$$

Thus, complex elasticity coefficients are defined as E_{A_s} and E_{f_s} for series injection and E_{A_p} and E_{f_p} for parallel injection. Using an approach similar to that presented in previous section, one can demonstrate that the LR Δf_s and Δf_p (respectively for series and parallel injection) are given as:

$$\Delta f_s = 2\frac{|E_{f_s}|\,|V_{inj}|}{|I_0|} = 2\frac{|V_{inj}|}{|I_0|}\sqrt{{f_r}^2 + {f_x}^2}, \tag{2.27}$$

$$\Delta f_p = 2\frac{|E_{f_p}|\,|I_{inj}|}{|V_0|} = 2\frac{|I_{inj}|}{|V_0|}\sqrt{{f_g}^2 + {f_b}^2} \tag{2.28}$$

, where $|I_0|$ (respectively $|V_0|$) is the amplitude of the current through (respectively the voltage across) the synchronization source in the free running oscillator.

Equations (2.27) and (2.28) give the LR of the ILO in both, series and parallel, injection cases. In the next sections, proposed modified theory will be used to determine the LR expressions for harmonic ILO as a function of circuit elements in both practical cases.

2.2.2 Parallel injection – example of Colpitts oscillator

This section is based on the compliance factors calculation methodology which has been developed by F. Badets in [59].

Consider the Colpitts oscillator shown in Figure 2.9a, where a parallel-injection current source I_{inj} is replaced by a small admittance variation $dy = g + jb$.

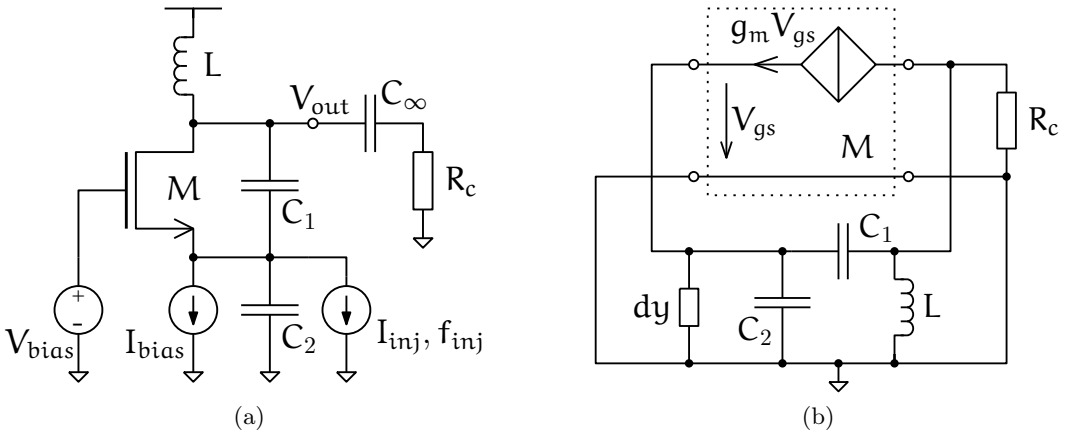


Figure 2.9 – Colpitts oscillator loaded with resistance R_c (a) schematic with parallel-injection source, (b) small-signal equivalent circuit.

The [Y]-matrix of the small-signal equivalent quadripole given in Figure 2.9b is:

$$[Y] = \begin{bmatrix} g + g_m + j\,(b + (C_1 + C_2)\,\omega) & -j\,C_1\omega \\ -(g_m + j\,C_1\omega) & \frac{1}{R_c} + j\,\left(C_1\omega - \frac{1}{L\omega}\right) \end{bmatrix} \tag{2.29}$$

The Barkhausen criterion, $\det[Y] = 0$, describes the behavior of the oscillator and will be used as a starting point to obtain relation between circuit parameters, elasticity coefficients and locking range.

By substituting g_m from the imaginary part of $\det[Y] = 0$ to the real part of $\det[Y] = 0$ one can obtain equation:

$$\omega^3 \left(\frac{L^2}{{R_c}^2} - \frac{L\,C_1 C_2}{C_1 + C_2} + \frac{g\,L^2\,C_1}{R_c\,(C_1 + C_2)} \right) + \frac{\omega^2\,b}{C_1 + C_2} \left(\frac{L^2}{{R_c}^2} - L\,C_1 \right) + \omega + \frac{b}{C_1 + C_2} = 0. \tag{2.30}$$

In case of the free-running oscillator $g = b = 0$ thus reducing (2.30) to already well-known equation:

$$\omega_0 = \frac{1}{\sqrt{L\frac{C_1 C_2}{C_1 + C_2} - \frac{L^2}{{R_c}^2}}}. \tag{2.31}$$

The frequency elasticity coefficients f_g and f_b are obtained by taking derivative of (2.30) by g and b, respectively, followed by equating to zero dy ($g = b = 0$) in the resulting

expressions:

$$f_g = \frac{1}{2\pi}\frac{\partial\omega}{\partial g}\bigg|_{dy=0} = \frac{1}{4\pi}\frac{L^2 C_1 \omega}{(C_1 + C_2)\, R_c}, \tag{2.32}$$

$$f_b = -\frac{1}{2\pi}\frac{\partial\omega}{\partial b}\bigg|_{dy=0} = -\frac{1}{4\pi}\frac{1 + {\omega_0}^2\left(\frac{L^2}{{R_c}^2} - L\,C_1\right)}{C_1 + C_2}. \tag{2.33}$$

The oscillator frequency LR is thus obtained by substituting (2.32) and (2.33) in (2.28), given as:

$$\Delta f_p = \frac{1}{2\pi}\frac{|I_{inj}|}{|V_0|}\sqrt{\left(\frac{L^2 C_1 \omega}{(C_1 + C_2)\, R_c}\right)^2 + \left(\frac{1 + {\omega_0}^2\left(\frac{L^2}{{R_c}^2} - L\,C_1\right)}{C_1 + C_2}\right)^2}. \tag{2.34}$$

Equations (2.31)–(2.34) allow ILO optimization and a practical way of simplifying them is to assume an open circuit as a load ($R_c \to \infty$):

$$\omega_0 = \frac{1}{\sqrt{L\frac{C_1 C_2}{C_1 + C_2}}}, \tag{2.35}$$

$$f_g = 0, \tag{2.36}$$

$$f_b = \frac{1}{4\pi}\frac{C_1}{C_1 + C_2}\frac{1}{C_2}. \tag{2.37}$$

Here, ω_0 is the frequency of free-running oscillations in a Colpitts oscillator. The term f_g shows that, in the first approximation, variations of the admittance Y real part does not impact the oscillation frequency. Parameter V_0 is the voltage across the free running oscillator nodes where the injection source will be applied in the ILO. Thus, it is given as $V_0 = V_{out}\frac{C_1}{C_1 + C_2}$. Now (2.34) can be expressed as:

$$\Delta f_p = \frac{1}{2\pi}\frac{|I_{inj}|}{|V_0|}\frac{C_1}{C_1 + C_2}\frac{1}{C_2} = \frac{1}{2\pi}\frac{|I_{inj}|}{|V_{out}|}\frac{1}{C_2}. \tag{2.38}$$

Equation (2.38) shows that to increase the locking range of the ILO the capacitance C_2 should be minimized. In this case the influence of dy and injection locking source on ILO is higher when the imaginary part of Y is smaller.

2.2.3 Series injection – example of Colpitts oscillator

Consider the Colpitts oscillator shown in Figure 2.10a, where a series-injection voltage source V_{inj} is replaced by a small impedance variation $dz = r + jx$.

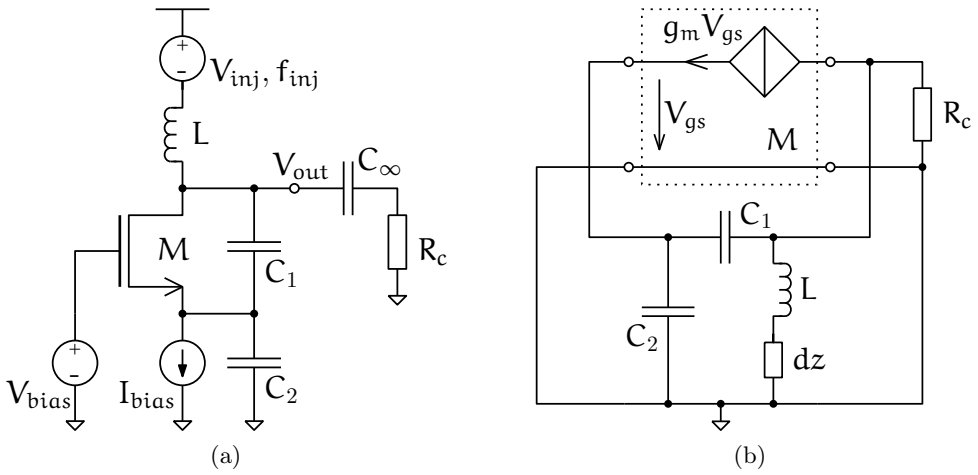


Figure 2.10 – Colpitts oscillator loaded with resistance R_c (a) schematic with series-injection source, (b) small-signal equivalent circuit.

The [Y]-matrix of the small-signal equivalent quadripole given in Figure 2.10b is:

$$[Y] = \begin{bmatrix} g_m + j\,(C_1 + C_2)\,\omega & -j\,C_1\omega \\ -(g_m + j\,C_1\omega) & \frac{1}{R_c} + j\,C_1\omega + \frac{1}{r + j\,(x + L\,\omega)} \end{bmatrix} \tag{2.39}$$

Starting again from the Barkhausen criterion, $\det[Y] = 0$, and substituting g_m from the imaginary part of $\det[Y] = 0$ to the real part of $\det[Y] = 0$, similarly to parallel injection, one can obtain the following equation:

$$\omega^2 \left(\frac{L\,C_1C_2}{C_1 + C_2} - \frac{L^2}{{R_c}^2} \right) + \omega\,x \left(\frac{C_1C_2}{C_1 + C_2} - \frac{2\,L}{{R_c}^2} \right) - \frac{x^2}{{R_c}^2} + \frac{(r + R_c)^2}{{R_c}^2} = 0. \tag{2.40}$$

In the free-running oscillator, $r = x = 0$ resulting in equation (2.40) reduction to (2.31).

The frequency elasticity coefficients f_r and f_x are obtained by taking derivative of (2.40) by r and x respectively, followed by equating to zero dz ($r = x = 0$) in the resulting expressions:

$$f_r = \frac{1}{2\pi} \frac{\partial\omega}{\partial r}\bigg|_{dz=0} = \frac{1}{4\pi} \frac{2\,\omega_0}{R_c}, \tag{2.41}$$

$$f_x = -\frac{1}{2\pi}\frac{\partial\omega}{\partial x}\bigg|_{dz=0} = -\frac{1}{4\pi}{\omega_0}^2\left(\frac{C_1C_2}{C_1+C_2} - \frac{2L}{{R_c}^2}\right). \tag{2.42}$$

The oscillator frequency LR is then obtain by substituting (2.41) and (2.42) in (2.27):

$$\Delta f_s = \frac{1}{2\pi}\frac{|V_{inj}|}{|I_0|}\sqrt{\left(\frac{2\omega_0}{R_c}\right)^2 + \left({\omega_0}^2\left(\frac{C_1C_2}{C_1+C_2} - \frac{2L}{{R_c}^2}\right)\right)^2}. \tag{2.43}$$

By considering an open circuit as a load ($R_c \to \infty$) we can simplify (2.41)–(2.43):

$$f_r = 0, \tag{2.44}$$

$$f_x = \frac{1}{4\pi}\frac{1}{L}, \tag{2.45}$$

$$\Delta f_s = \frac{1}{2\pi}\frac{|V_{inj}|}{|I_0|}\frac{1}{L}. \tag{2.46}$$

Equation (2.46) shows that to increase the LR of the ILO the inductance L should be minimized. Again, the influence of dz and injection locking source on ILO is higher if imaginary part of Z is smaller.

2.2.4 Generalization

With the modified Huntoon-Weiss theory, one can fully optimize the ILO design by taking into account its topology specifications. Moreover, with first order approximations, as in (2.38) and (2.46), this approach can lead to first order ILO trade-offs.

A comparative study of harmonic oscillator architectures like Hartley or Cross-Coupled oscillators was performed. For each case, the LR equation as a function of circuit parameters was derived using the previously introduced methodology. This study showed that as a first approximation the ILO frequency LR can always be approximated using equations (2.38) or (2.46) depending on the nature of the injection source. In other words, the first way to increase the ILO frequency LR is by minimizing the impedance or the admittance presented to the synchronization source.

This can be easily explained: by definition the frequency elasticity coefficients are an image of the oscillator frequency sensitivity according to the variations of the impedance (or the admittance) of the phase shifting network. It is normal, *a posteriori*, that more the impedance (or the admittance) presented to the synchronization source is reduced, the larger the influence of the disturbance is felt on the equivalent component, and therefore on the operation frequency.

Another important observation appears by rewriting equations (2.38) and (2.46) and by comparing the dimensions of each term.

$$\Delta f_p = \frac{1}{2\pi} \frac{|I_{inj}|}{|V_{out}|} \frac{1}{C_2} \equiv \frac{[mA]}{[V]} \frac{1}{[pF]} \propto [GHz], \tag{2.47}$$

$$\Delta f_s = \frac{1}{2\pi} \frac{|V_{inj}|}{|I_0|} \frac{1}{L} \equiv \frac{[mV]}{[mA]} \frac{1}{[nH]} \propto [GHz]. \tag{2.48}$$

To obtain a locking range of a few gigahertz one has to apply either few milliamps at the synchronization input in the case of parallel injection or only few millivolts in the case of series injection. If other parameters are in the usual range of values for common RF/mm-wave oscillators, equations (2.47) and (2.48) illustrate an oscillator easier to be synchronized in a large range of frequency by using a series injection architecture.

2.2.5 Simulation results

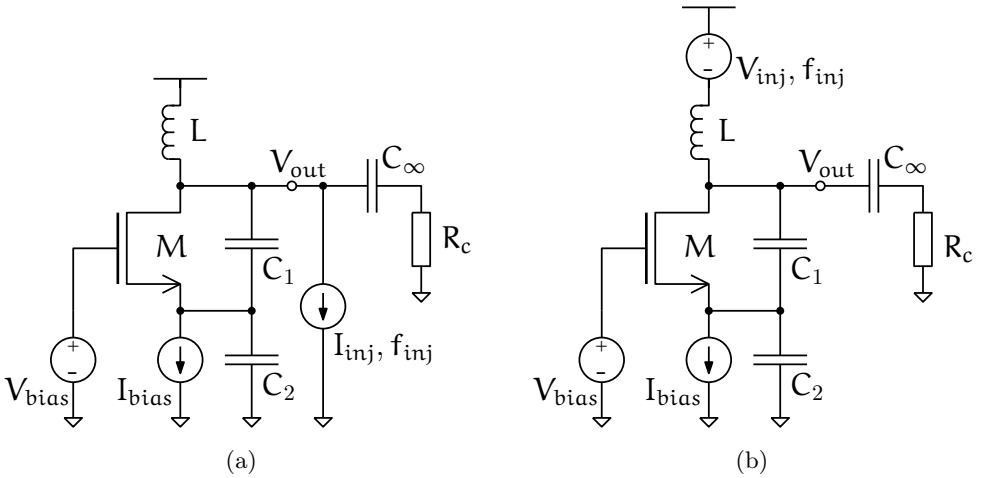
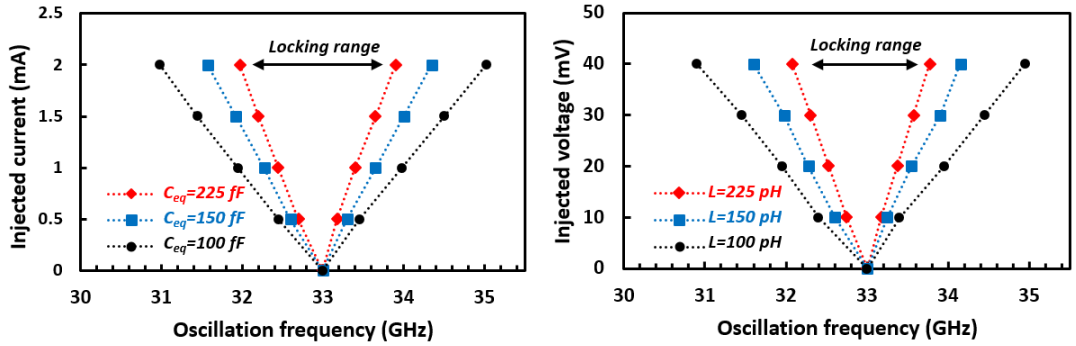


Figure 2.11 – Simulated schematics of (a) parallel synchronized and (b) series synchronized Colpitts oscillators.

The proposed theory has been verified on several circuit topologies implemented in ST Microelectronics 28nm UTBB FDSOI CMOS technology. Figure 2.11 represents the simulated oscillator schematics, where I_{inj} and V_{inj} are the parallel and the series injection sources respectively. In the aim of LR increase, the injection source of the Figure 2.11a was moved to the minimum capacitance point of the architecture.

In order to focus this analysis on first order behavior, all passive components are taken here as ideal and parasitic capacitances introduced by the transistors are also considered.



(a) (b)

Figure 2.12 – Simulated oscillation frequency and locking range for the (a) parallel synchronized and (b) series synchronized Colpitts oscillators.

The ILO LRs were simulated as a function of the injected signal amplitude for different values of passive elements (C_1, C_2 and L). In each case the free-running frequency is 33GHz and DC biasing conditions are identical.

The LR is defined, with respect to this theory, as the range of frequency in which: 1– the oscillator will be locked by the injected signal. 2– the amplitude of the output signal is at least equal to the free-running oscillator amplitude (i.e. the injected signal does not affect significantly the amplitude of the output signal).

Figures 2.12(a-b) present the simulation results of the oscillation frequency as a function of the injected signal amplitude for the parallel synchronized and the series synchronized Colpitts oscillator respectively. As predicted by the theory, the LR is increased by decreasing C_{eq} and L for parallel and series injection respectively. Moreover, the LR increases linearly with the injected signal amplitude.

It is noteworthy that it is possible to reach an LR larger than 4 GHz (which means approximately 12% of the free-running frequency) using $C_{eq} = 100\mathrm{fF}$, $I_{inj} = 2\mathrm{mA}$ and $L = 100\mathrm{pH}$, $V_{inj} = 40\mathrm{mV}$ for the parallel and series injection respectively.

In each case the free-running amplitude is respectively $|I_0| = 15.8\mathrm{mA}$ and $|V_0| = 785\mathrm{mV}$. This means that to obtain the same 4 GHz (12%) LR, the injected signal amplitude has to be 12.7% of the free-running signal amplitude for parallel injection and only 5.1% for series injection.

Figure 2.13 presents the normalized injected signal amplitude as a function the normalized LR in these two cases. These results confirm the previously derived conclusion that it is

more practical to obtain a large LR with a series injection source than a parallel one.

The theoretical LR values are compared to simulated ones in Figure 2.14. It can be seen that as a first approximation (i.e. by considering ideal passive devices) the theory developed in this paper predicts accurately the ILO LR. The normalized errors between theory and simulations are lower than 1.5% for both analyzed cases, shown in Figure 2.15.

Finally, two remarks have to be added. First, the theory presented in [62] and in this work too makes the assumption that the injected signal does not modify significantly the amplitude of the output signal. However, in the case of strong injection, the output signal amplitude decreases and the locking range can be significantly larger than estimated by

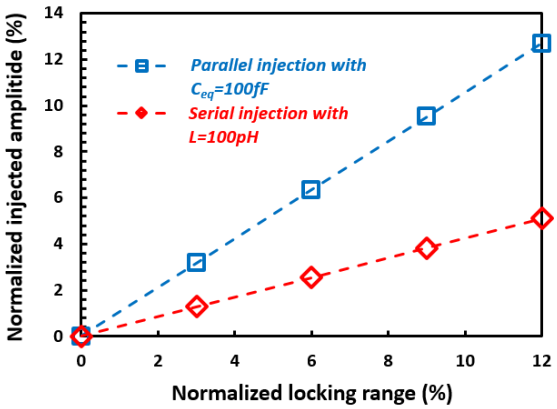
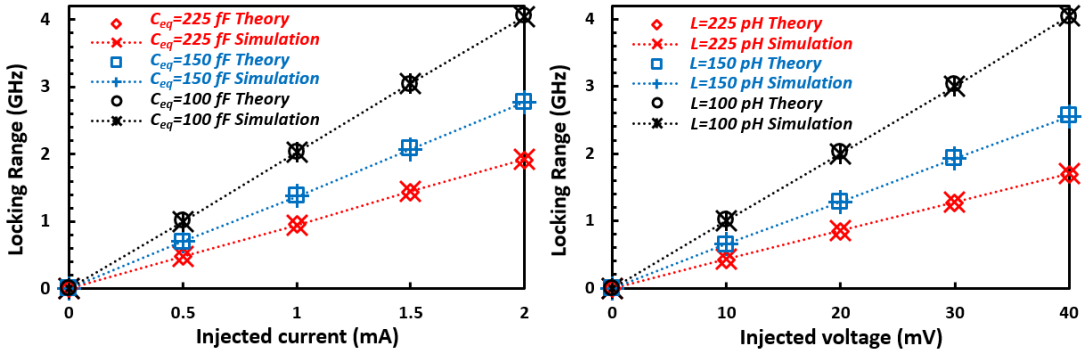
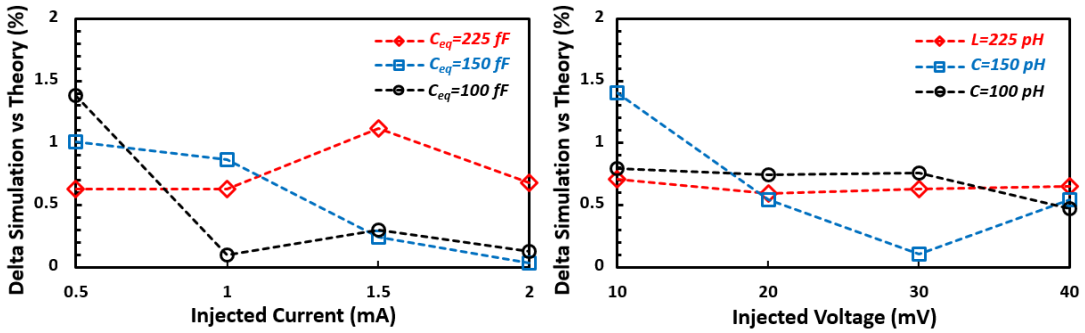


Figure 2.13 – Colpitts ILO normalized injected signal amplitude as a function of the normalized locking range.



(a) (b)

Figure 2.14 – Simulation versus theory of the locking range for the (a) parallel synchronized and (b) series synchronized Colpitts oscillator.



(a) (b)

Figure 2.15 – Normalized error between theory and simulation for the (a) parallel synchronized and (b) series synchronized Colpitts oscillator.

the first order theory. This variation can be calculated by using the theory developed by Badets in [59] and adjusting the LR formula accordingly.

The second remark is that in this example all passives are considered ideal. However, it is possible to accurately predict the LR of the ILO in a non-ideal case by using the matrix approach presented in this chapter (see section 2.2.2) and including all the parasitic elements of passive components.

2.3 The injection locked distributed oscillator

2.3.1 Overview of the distributed oscillator and its properties

Distributed oscillators originate from distributed amplifiers (DA, or traveling wave amplifiers, TWA). Firstly introduced in 1948 by Ginzton *et al.* [71], DA can achieve a higher gain-bandwidth product than classic amplifier circuits [72]. Thus, DA have been widely used for wide-band amplification [73–76].

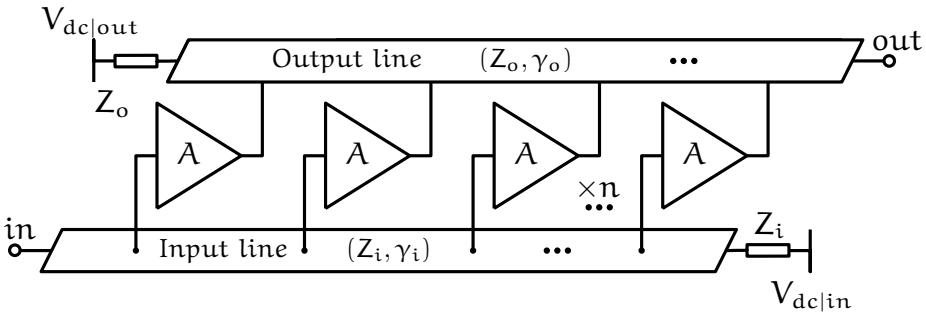


Figure 2.16 – Simplified n-stage distributed amplifier.

The Figure 2.16 presents a simplified n-stage distributed amplifier schematic in which n identical amplifiers are cascaded. Amplifier inputs and outputs are connected to a transmission line (TL) with a constant spacing. The propagation constants physical and lengths of the input and output lines are chosen for constructive phasing of the output signals. The two TLs are ended by loads to absorb incident and retrograde waves and thus ensure signal integrity.

In 1992, Skvor *et al.* [77] proposed to build an oscillator by looping-back a DA with the

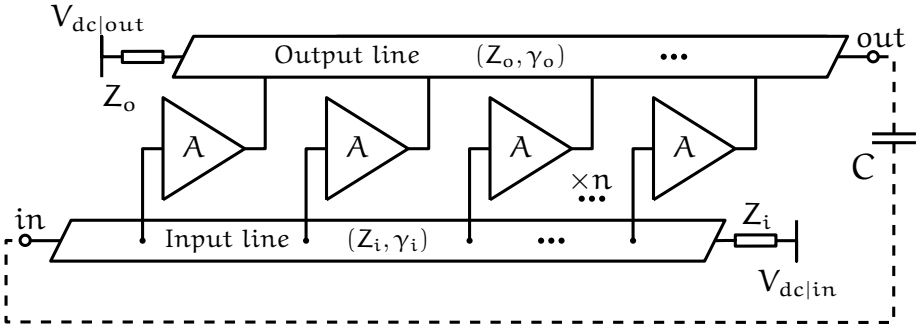


Figure 2.17 – Simplified n-stage distributed oscillator.

required phase inversion, as depicted in Figure 2.17. Intuitively, the oscillation frequency is determined by the loop propagation time delay, *i.e.*, the time the wave takes to travel through the TLs and then gets amplified by one of the amplifiers. The speed on the wave through the TL is given by $v = c/\sqrt{\epsilon_{eff}}$, with c the speed of light in vacuum and ϵ_{eff} the effective permittivity of materials surrounding the line. Thus, the oscillation frequency is linked to the wave velocity as: $f_{osc} = v/\lambda$, in which λ represents the wavelength and thus the total line length.

The DOs have many interesting properties mainly due to the distributed nature of the passive components.

- First of all, the oscillation frequency is mainly function of the TL equivalent lumped component which depends only on the TL dimension [78, 79]. This means that the oscillation frequency has a very low dependence on the technological dispersion of active components.
- Due to the distributed structure, the transistors' parasitic capacitances are absorbed into the TLs [78]. This allows better open loop gain-bandwidth product and thus farther close loop operation frequency compared to a lumped harmonic oscillator.
- The TL exhibit better high-frequency quality factor than lumped components [72], thus the frequency phase noise of a mm-wave/THz DO will be better than a classical harmonic oscillator.
- By choosing the adequate number of amplification stages, it is possible to generate low-noise quadrature signals [78].

All these properties make the DO a good candidate for mm-wave and THz frequency generation on advanced CMOS technology. Nevertheless, a good understanding of DO behavior is essential. Consequently, a theoretical study is necessary.

2.3.2 Distributed oscillator for operation frequencies close to f_{max}

Let us consider the DO presented in Figure 2.18. The gates and drains of the n identical transistors are connected to TLs with a constant spacing of l. Each transistor has a large signal transconductance of G_m. The TLs have a characteristic impedance Z_c and a complex propagation constant $\gamma = \alpha + j\beta$, in which α and β are the attenuation and phase constant of the transmission lines, respectively. We assume here that the TLs are terminated to a matched load of Z_c. According to DO theory [78], the oscillation

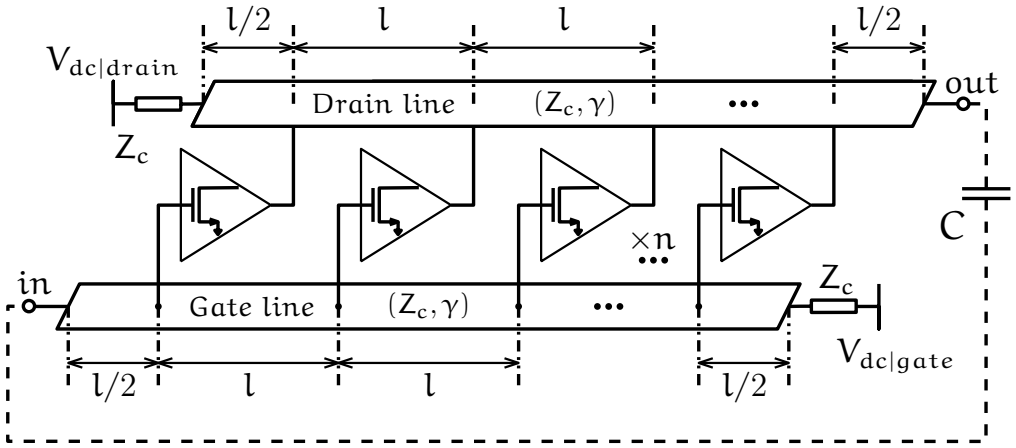


Figure 2.18 – Distributed oscillator architecture used in the theory.

condition in an ideal behavior is given by:

$$G_m n (Z_c/2) e^{-\alpha n l} e^{-j\beta n l} = -1. \tag{2.49}$$

Assuming purely real characteristic impedance Z_c, (2.49) gives the Barkhausen amplitude and phase criteria:

$$\left| G_m n (Z_c/2) e^{-\alpha n l} \right| = 1, \tag{2.50}$$

$$e^{-j\beta n l} = -1 \Leftrightarrow \beta n l = \pi. \tag{2.51}$$

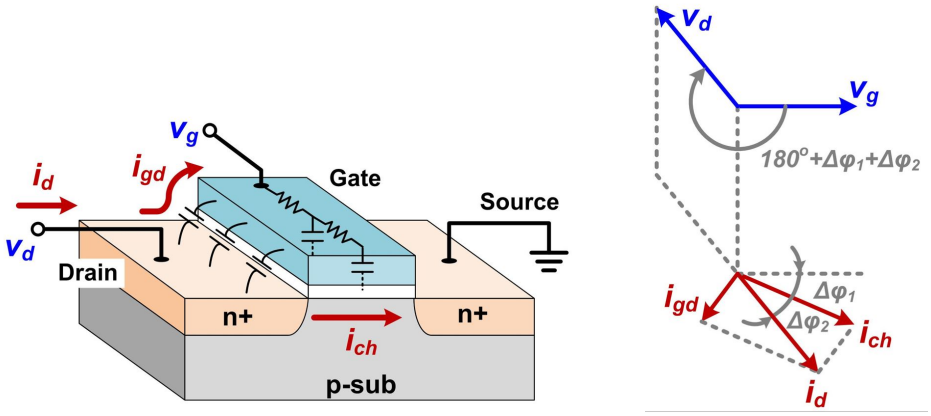
Noting that $\beta = \frac{2\pi f}{v_\phi}$ and $v_\phi \approx \frac{1}{\sqrt{L_u C_u}}$ [72], (2.51) gives the oscillation frequency:

$$f_{osc} = \frac{1}{2 n l \sqrt{L_u C_u}} \tag{2.52}$$

, where L_u and C_u are TLs inductance and capacitance per unit length, respectively. It is noteworthy that (2.52) can be written as $f_{osc} = \frac{1}{\sqrt{L_{tot} C_{tot}}}$ where $L_{tot} = 2nlL_u$ and $C_{tot} = 2nlC_u$ are the total inductance and capacitance of the entire loaded line. Thus, the oscillation frequency given by (2.52) is approximately 2π times larger than that of a lumped oscillator with a tank inductance and capacitance of values L_{tot} and C_{tot}.

Equations (2.49) to (2.52) assume an ideal transistor phase shift of π which is never the case at RF and mm-wave frequencies given the limited values for transistors' f_T/f_{max} [79, 80].

Indeed, when we apply a voltage on the gate to source junction of a standard CMOS transistor, as depicted in Figure 2.19a, it induces a current i_{ch} in the channel with a delay



(a) (b)

Figure 2.19 – (a) Standrad CMOS transistor and (b) its gate/drain phase relationship. (Figures from [80])

(inducing a fist added phase shift $\Delta\varphi_1$). This is because it takes time for the gate signal to travel along the gate RLC network. Moreover, due to parasitic capacitance between the gate and drain, the gate voltage also causes a feedforward current from the drain i_{dg} (inducing a second added phase shift $\Delta\varphi_2$).

The transistor gate to drain phase relationship is illustrated in Figure 2.19b. The total drain current i_d is the vector sum of i_{ch} and i_{dg}. Since the drain current is delayed, the drain voltage should also be delayed on top of the conventional inversion behavior of the CMOS transistor. Thus, a total transistor phase shift correction $\Delta\varphi$ is introduced as $\Delta\varphi = \Delta\varphi_1 + \Delta\varphi_2$. Such effect is normally neglected in RF design, but in mm-wave and THz frequency ranges, it becomes very significant.

When applying this phase shift correction to the DO theory, the oscillation condition for operation frequencies close to f_{max} becomes:

$$G_m n\,(Z_c/2)\,e^{-j\Delta\varphi}\,e^{-\alpha n l}\,e^{-j\beta n l} = -1. \tag{2.53}$$

Assuming purely real characteristic impedance Z_c in the oscillation frequency vicinity, (2.53) gives the Barkhausen amplitude and phase criteria:

$$\left| G_m n\,(Z_c/2)\,e^{-\alpha n l} \right| = 1, \tag{2.54}$$

$$e^{-j(\beta n l+\Delta\varphi)} = -1 \;\Leftrightarrow\; \beta n l + \Delta\varphi = \pi. \tag{2.55}$$

As previously said, $\beta \approx 2\pi f\sqrt{L_u C_u}$, therefore the equation (2.55) gives the oscillation

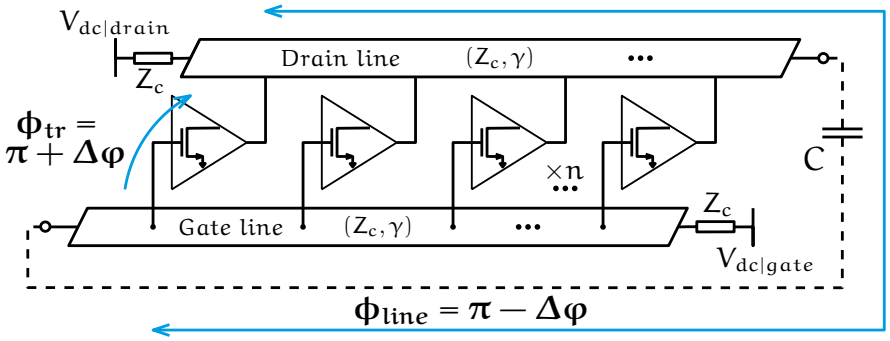


Figure 2.20 – Distributed oscillator for operation frequency close to f_{max}.

frequency:

$$f_{osc} = \frac{1 - \Delta\varphi/\pi}{2\,n\,l\,\sqrt{L_u C_u}}. \tag{2.56}$$

It is noteworthy that, for a given TL length, the phase-shift correction involves a reduction of the oscillation frequency. In other words, to oscillate at a given frequency the phase-shift correction involves a reduction of the TL length and hence of the circuit surface.

The results of (2.56) can be found by considering the Figure 2.20. Indeed, intuitively the phase-shirt induce by the TL between the same transistor drain and gate have to be equal to $\pi - \Delta\varphi$. As the TL length between one transistor drain and gate is always equal to nl, this gives $\beta nl = \pi - \Delta\varphi$ which is the result of (2.55).

2.3.3 Theory of injection locked distributed oscillator

In this section, we propose to extend the ILO theory introduced in section 2.2 to the study of injection-locked-distributed-oscillators (ILDO). The theory will be applied for the case of a series injection, following the conclusion from the section 2.2.4.

Let us consider the DO previously presented and the TL unit length element equivalent circuit shown in Figure 2.21a. The series inductance L_u represents the total self-inductance of the TL, and the parallel capacitance C_u is due to the proximity between TL and return path ground. The series resistance R_u represents the resistance due to the finite conductivity of the conductors, and the parallel conductance G_u is due to dielectric loss in the material between TL and ground. R_u and G_u therefore represent losses.

By writing and transposing the *telegrapher equations* in frequency domain for the sinusoidal

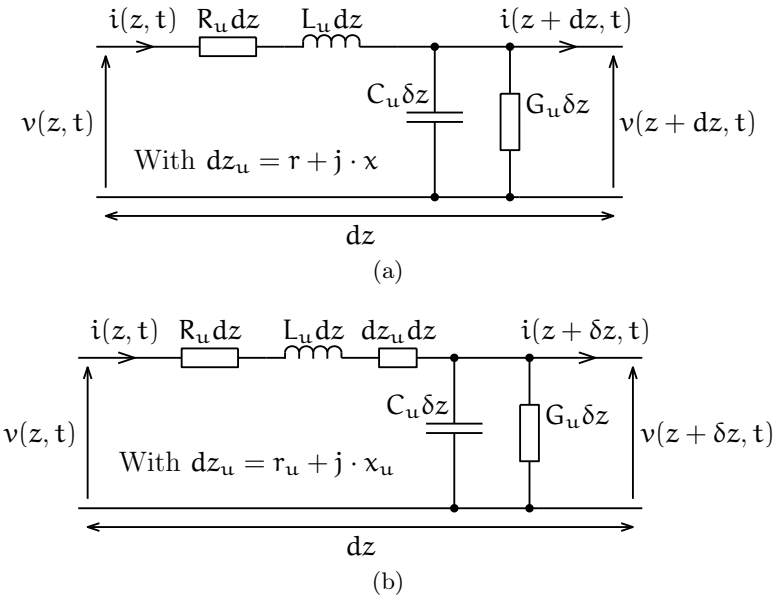


Figure 2.21 – Unit length element equivalent circuit of (a) classic TL and (b) TL under series injection.

steady-state condition [72], we obtain:

$$\frac{d\,V(z)}{dz} = -\,(R_u + j\,L_u\,\omega)\,I(z)\,, \tag{2.57}$$

$$\frac{d\,I(z)}{dz} = -\,(G_u + j\,C_u\,\omega)\,V(z)\,. \tag{2.58}$$

Now let's suppose, like in series synchronization theory, that if the injection amplitude is low and its frequency close to f_0, then a synchronization source in series with the line can be replaced by a small variation of its impedance per unit length dz_u, as depicted in Figure 2.21b. In this case r_u and x_u are unit length parameters. In these conditions, (2.57) can be rewritten as follows:

$$\frac{d\,V(z)}{dz} = -\,((R_u + r_u) + j\,(L_u\,\omega + x_u))\,I(z)\,. \tag{2.59}$$

Equations (2.58) and (2.59) can be solved to give wave equations for $V(z)$ and $I(z)$ [72]:

$$\frac{d^2\,V(z)}{dz^2} = -\gamma^2\,V(z)\,, \tag{2.60}$$

$$\frac{d^2\,I(z)}{dz^2} = -\gamma^2\,I(z) \tag{2.61}$$

, where the complex propagation constant γ is:

$$\gamma = \alpha + j\,\beta = \sqrt{((R_u + r_u) + j\,(L_u\,\omega + x_u))\,(G_u + j\,C_u\,\omega)}$$
$$= \sqrt{\begin{array}{l}((R_u + r_u)\,G_u - (L_u\,\omega + x_u)\;C_u\,\omega) \\ \quad + j\,((R_u + r_u)\;C_u\,\omega + (L_u\,\omega + x_u)\;G_u)\end{array}}\,. \tag{2.62}$$

The phase Barkhausen criterion, $\beta\,n\,l + \Delta\varphi = \pi$ (Equation (2.51)), describes the frequency behavior of the oscillator and will be used as a starting point to obtain a relation between circuit parameters, elasticity coefficients and locking range in the case of ILDO.

If $\gamma = \sqrt{a + j\,b}$ and $b > 0$, then its imaginary part β can be written as:

$$\beta = \frac{1}{2}\sqrt{2\sqrt{a^2 + b^2} - 2a}\,. \tag{2.63}$$

By combining (2.62) and (2.63), the phase constant β can be rewritten as:

$$\beta = \frac{1}{2}\cdot\sqrt{\begin{array}{l}2\cdot\sqrt{\begin{array}{l}((R_u + r_u)\,G_u - (L_u\,\omega + x_u)\;C_u\,\omega)^2 \\ \quad + \;((R_u + r_u)\;C_u\,\omega + (L_u\,\omega + x_u)\;G_u)^2\end{array}} \\ \quad - 2\;((R_u + r_u)\,G_u - (L_u\,\omega + x_u)\;C_u\,\omega)\end{array}}\,. \tag{2.64}$$

By rewriting this equation one can obtain the general equation describing the frequency variation as a function of circuit parameters:

$$\omega^2\,\frac{4\,\beta^2\,L_u\,C_u + ((R_u + r_u)\;C_u + L_u\,G_u)^2}{4\,\beta^2\,(\beta^2 + (R_u + r_u)\;G_u)}$$
$$+\;\omega\,x_u\,\frac{4\,\beta^2\,C_u + 2\,G_u\;((R_u + r_u)\;C_u + L_u\,G_u)}{4\,\beta^2\,(\beta^2 + (R_u + r_u)\;G_u)}$$
$$+\;\frac{{x_u}^2\,{G_u}^2}{4\,\beta^2\,(\beta^2 + (R_u + r_u)\;G_u)} - 1 = 0\,. \tag{2.65}$$

In case of the free-running oscillator, $r_u = x_u = 0$ and (2.65) is reduced to:

$$\omega_0 = \sqrt{\frac{4\,\beta^2\,(\beta^2 + R_u\,G_u)}{4\,\beta^2\,L_u\,C_u + (R_u\,C_u + L_u\,G_u)^2}}\,. \tag{2.66}$$

The frequency elasticity coefficients over the total line length (noted $2nl$), f_r and f_x, are obtained by tacking derivative of (2.65) by r_u and x_u, respectively, followed by equating to zero dz_u ($r_u = x_u = 0$). The resulting expressions are:

$$f_r = \frac{1}{2\pi}\frac{1}{2nl}\frac{\partial\omega}{\partial r}\bigg|_{dz_u=0} = \frac{4\beta^2 G_u \omega_0 + 2C_u(R_u C_u + L_u G_u)\,{\omega_0}^3}{4\pi\cdot 2nl\cdot 4\beta^2(\beta^2 + R_u G_u)}, \tag{2.67}$$

$$f_x = -\frac{1}{2\pi}\frac{1}{2nl}\frac{\partial\omega}{\partial x}\bigg|_{dz_u=0} = \frac{{\omega_0}^2\left(4\beta^2 C_u \omega_0 + 2G_u(R_u C_u + L_u G_u)\right)}{4\pi\cdot 2nl\cdot 4\beta^2(\beta^2 + R_u G_u)}. \tag{2.68}$$

The oscillator frequency LR is obtained by substituting (2.67) and (2.68) in (2.27), which is the LR equation for the case of series injection which was introduced in section 2.2. It follows:

$$\Delta f = \frac{1}{2\pi}\frac{1}{2nl}\frac{|V_{inj}|}{|I_0|}\sqrt{\left(\frac{4\beta^2 G_u \omega_0 + 2C_u(R_u C_u + L_u G_u)\,{\omega_0}^3}{4\beta^2(\beta^2 + R_u G_u)}\right)^2 + \left(\frac{{\omega_0}^2\left(4\beta^2 C_u \omega_0 + 2G_u(R_u C_u + L_u G_u)\right)}{4\beta^2(\beta^2 + R_u G_u)}\right)^2}\,. \tag{2.69}$$

Equations (2.66) to (2.69) allow ILDO optimization. As proceeded in sections 2.2.2 and 2.2.3, we can simplify them assuming low losses in the TL ($R_u, G_u \to 0$) and then obtain:

$$\omega_0 = \frac{\beta}{\sqrt{L_u C_u}} = \frac{\pi - \Delta\varphi}{nl\sqrt{L_u C_u}}\,, \tag{2.70}$$

$$f_r = 0\,, \tag{2.71}$$

$$f_x = \frac{1}{4\pi}\frac{1}{2nl}\frac{1}{L_u}\,. \tag{2.72}$$

It can be seen that ω_0 is the already known equation of a DO free-running oscillation frequency which was previously presented in section 2.3.2. The term f_r shows that assuming low losses, variations of the impedance Z_c real part do not impact the oscillation frequency. Now (2.69) can be expressed as:

$$\Delta f = \frac{1}{2\pi}\frac{|V_{inj}|}{|I_0|}\frac{1}{2nl}\frac{1}{L_u} = \frac{1}{2\pi}\frac{|V_{inj}|}{|I_0|}\frac{1}{L_{tot}} \tag{2.73}$$

, where $L_{tot} = 2nlL_u$ is the total inductance of the entire loaded line. Equation (2.73) shows that to increase the locking range of the ILDO the TL unit length equivalent inductance L_u should be minimized.

2.3.4 Simulation results

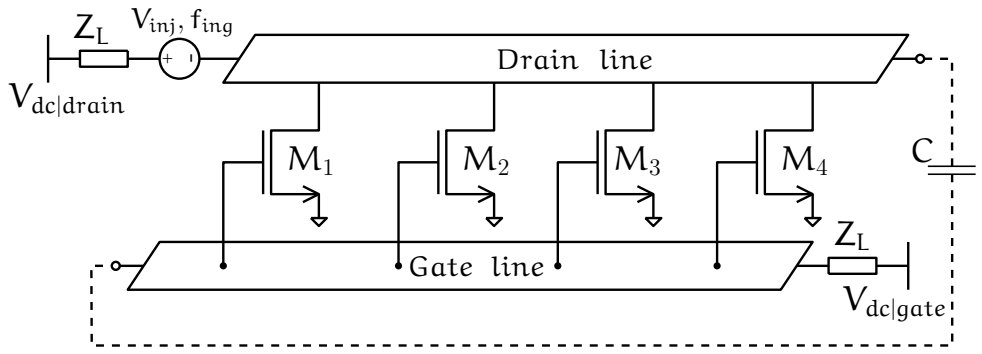


Figure 2.22 – Simulated schematics of the series synchronized distributed oscillators.

This proposed theory has been verified on a topology implemented in STMicroelectronics 28nm UTBB FDSOI CMOS technology. Figure 2.22 represents the simulated oscillator schematic, where V_{inj} is the series injection source.

In order to focus this analysis on first order behavior, all passive components are considered here as ideal and parasitic capacitances introduced by the transistors are also considered. Dielectric losses are neglected, which means that G_u is equal to 0. Nevertheless, to guaranty a good oscillator behavior, the unit length resistance is taken into account.

The ILDO LRs were simulated as a function of the injected signal amplitude for two different values of unit length inductance L_u. In each case the free-running frequency is 33GHz and DC biasing conditions are identical. Unlike what was done in section 2.2.5, only two values of unit length inductance are presented because in this particular example a smaller inductance per unit length would be physically unrealizable with the given conditions.

Like in section 2.2.5, the LR is defined as the range of frequency in which: 1– the oscillator will be locked by the injected signal. 2– the amplitude of the output signal is at least equal to the free-running oscillator amplitude (i.e. the injected signal does not affect significantly the amplitude of the output signal).

Figure 2.23 presents the simulation results of the ILDO oscillation frequency as a function of the injected signal amplitude. As predicted by the theory, the LR is increased by decreasing the unit length inductance L_u. And again, the LR increases linearly with the injected signal amplitude, as predicted.

The theoretical LR values are compared to simulated ones in Figure 2.24a. It noteworthy that as a first approximation (i.e. by considering ideal passives and low TL losses) the

theory developed in this chapter predicts accurately the ILDO LR. The normalized errors between theory and simulations are lower than 2% as shown in Figure 2.24b. It can be seen that a systematic error appears. It is due to the simulated transmission lines model which is not fully simplified. Indeed, a distributed oscillator behavior implies that the resistive losses of any TL have to exist even for a conceptual simulation like here.

Finally, remarks made in section 2.2.5 are still valid here. Indeed, this theory is limited to the study of low amplitude injection to guaranty that the injected signal does not modify significantly the amplitude of the output signal. However, in the case of strong injection, it is possible to calculate the LR using the theory developed by Badets in [59]. In any way, since in strong injection case the output signal amplitude decreases near the LR limits, the effective LR must be at least significantly larger than estimated by the first order theory introduced here.

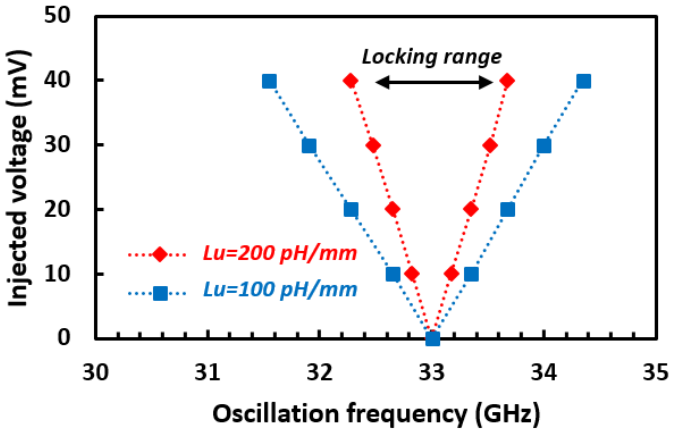
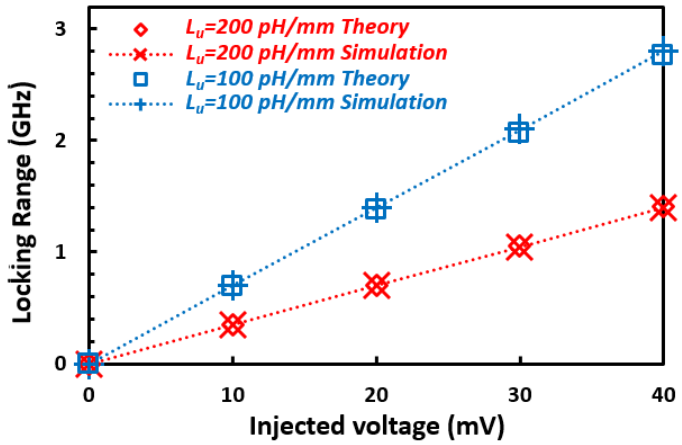


Figure 2.23 – Simulated ILDO oscillation frequency and locking range.

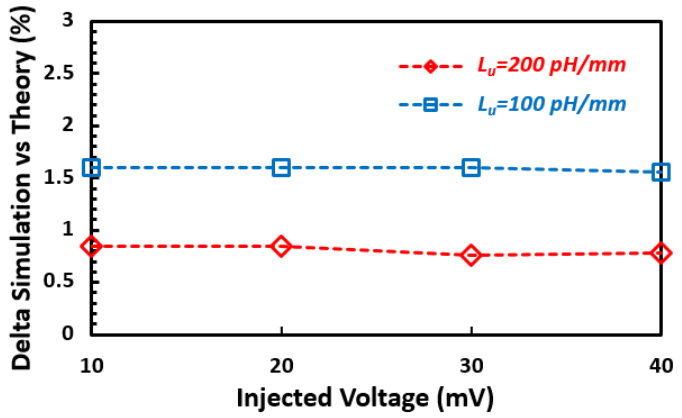
2.4 Chapter Conclusion

This chapter has presented the injection locking phenomenon and how ILOs can be used in frequency synthesis. The mainly used oscillator synchronization theories have been quickly described and a new methodology for the case of harmonic oscillators was introduced.

This theoretical approach allows to fully optimize an ILO design by taking into account its topology specifications. Moreover, with first order approximation, this approach gives simple equations for the locking range as a function of circuit parameters. This analysis



(a)



(b)

Figure 2.24 – (a) Simulation versus theory of the ILDO locking range and (b) Normalized error between theory and simulation.

has shown that a series injection approach is the most efficient way to increase the locking range of an ILO.

Thereafter, the distributed oscillator has been presented and theory for operation frequency close to transistor f_{max} has been introduced. Finally, the ILO theory previously introduced in this chapter has been extended to the study of ILDO.

To conclude, this chapter has shown that ILDO is one of the most relevant choices for mm-wave and THz frequency synthesis. Moreover, the theory presented in this chapter guarantees an excellent ILDO behavior prediction, allowing its use for the realization of mm-wave and THz frequency sources in advanced CMOS technology.

3 Mm-wave and THz Sources Design in 28nm FD-SOI Technology

This chapter will present the design of mm-wave and THz sources in advanced silicon technology.

First, we will provide an overview of the 28nm FD-SOI technology from ST Microelectronics for high-frequency applications. Then, a distributed oscillator design methodology will be presented.

Finally, the introduced design methodology will be used to design two distributed oscillators at 135 GHz and 200 GHz. Starting from amplification stages and transmission lines design up to chip finishing.

3.1 Overview of the 28nm FD-SOI technology for mm-wave THz applications

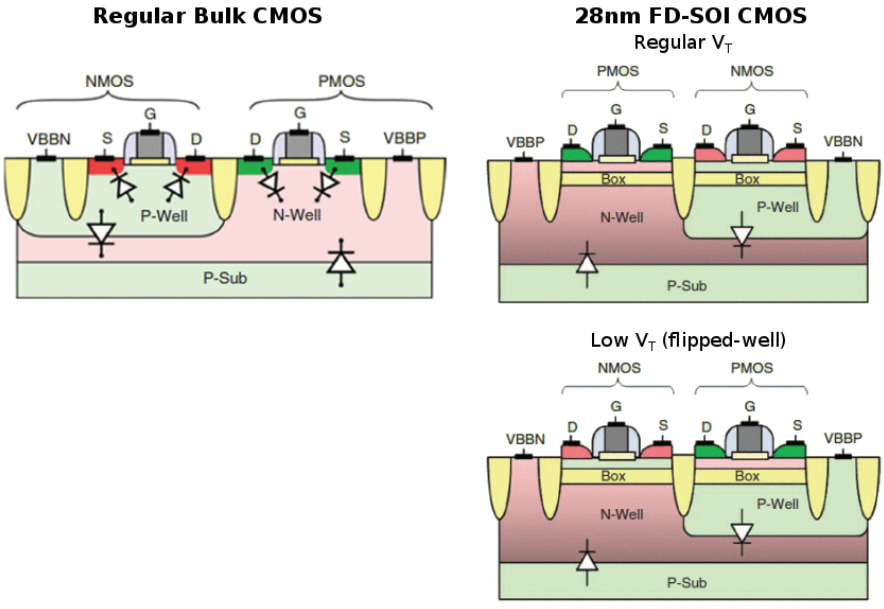
The constraints linked to today's and tomorrow's electronic systems involve the use of cost-optimized technologies that allow the integration of complex reconfigurable systems.

With advanced technologies such as CMOS FD-SOI, it is possible to integrate both high-speed digital and RF components to take advantage of system-on-chip (SOC) integration and thus reduce the production costs of complex systems.

This section provides an overview of the 28 nm FD-SOI technology from ST Microelectronics which is used in this work.

3.1.1 Active devices

Compared to conventional bulk CMOS, FD-SOI technology uses an ultra-thin silicon layer covering a very thin buried oxide (BOX). In the 28-nm FD-SOI technology, the implementation of the BOX isolates the channel from the substrate and limits the electrons circulating therein. Thus, the leakage between the channel and the substrate are reduced.



(a) (b)

Figure 3.1 – Cross-section of (a) regular Bulk CMOS technology and (b) 28nm FD-SOI CMOS technology transistors [81].

In addition, the presence of the buried oxide under the source and the drain eliminates the junction diodes of the source and the drain to the substrate. Thus, it allows large body-biasing and reduces the source-substrate and drain-substrate parasitic capacitances compared to a bulk CMOS technology. The transistors of the CMOS Bulk and FD-SOI technologies are presented and compared in Figure 3.1.

I-V characteristic measurements of 28nm FD-SOI LVT NMOS are depicted in Figure 3.2 from [82] and compared with 28nm bulk technology. It is noticeable that thanks to its isolated channel, the 28nm FD-SOI technology exhibit a better transistor effect. Indeed, R_{DS} appears noticeably higher thus analog gain (G_m/G_{DS}) is improved.

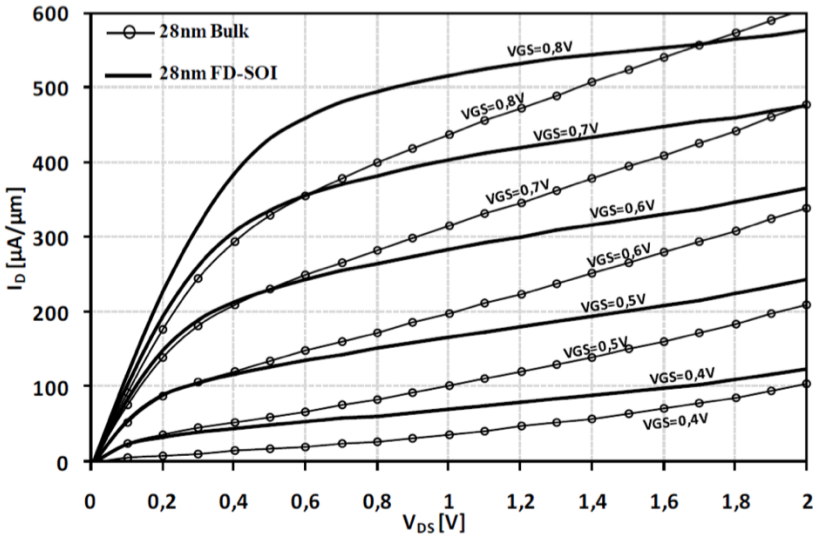
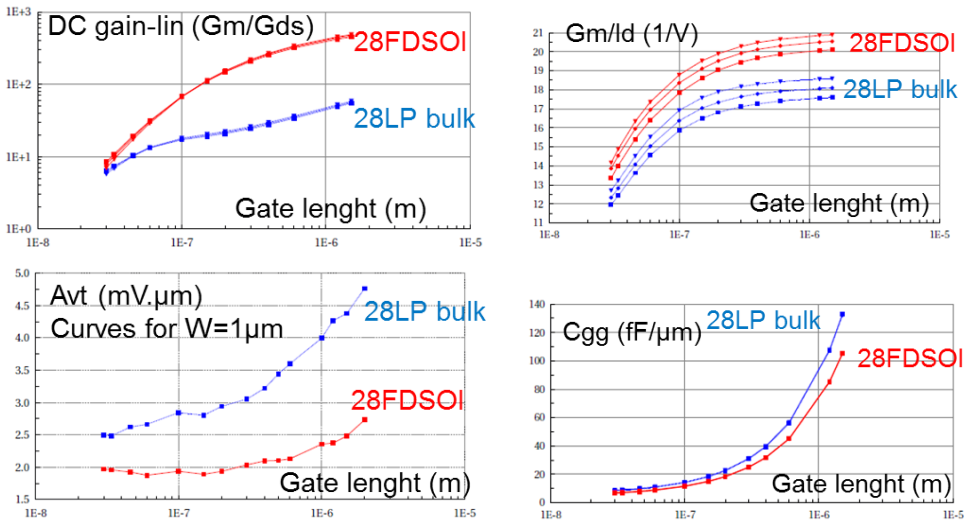


Figure 3.2 – I-V characteristic measurement comparison between 28nm Bulk and FD-SOI technology. [82].

In order to present more in detail the advantages of the FD-SOI technology, in the following figures, different analog parameters will be compared between the 28nm FDSOI technology with its equivalent 28nm LP bulk technology from ST Microelectronics.

The Figure 3.3(a) presents major improvements of FD-SOI solution regarding analog gain and VT matching parameter. For example, in 28nm FDSOI, a Low V_T (LVT) NMOS device of size 1µm/100nm can show an excellent analog performance of DC gain of 80 and a sigma(VT) of only 6mV.

The Figure 3.3(b) shows that an FD-SOI device provides higher Gm for a given current, with respect to its equivalent in 28nm Bulk technology. This, combined with the low parasitic capacitance presented before, allow achieving higher gain-bandwidth product for a given current consumption, or lower power consumption for a given gain and bandwidth.



(a) (b)

Figure 3.3 – Improved analog performance ((a) Analog gain (Gm/Gds) and matching (AVT) and (b) Gm/Id and total gate capacitance Cgg) for NMOS LVT devices in 28nm FDSOI technology (red) and comparison with 28nm LP bulk (blue) [81].

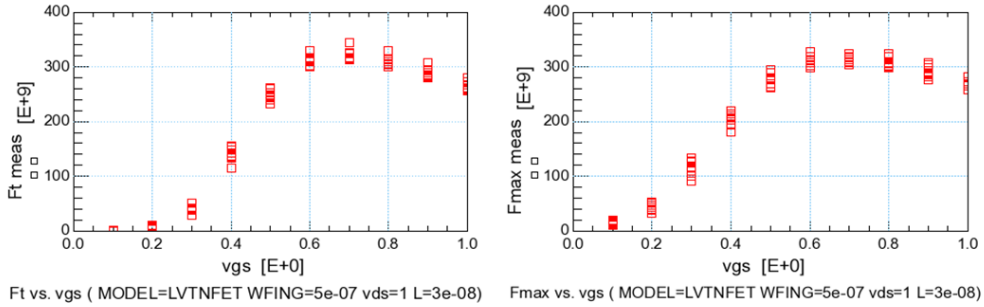


Figure 3.4 – High frequency behavior (f_T and f_{max}) of LVT NMOS with 0.5µm/30nm finger size in 28nm FDSOI CMOS [81].

Moreover, high values of f_T/f_{max} are reported in 28nm FD-SOI technology. The intrinsic devices (Front-End-of-Line (FEOL) plus Metal1 contact) in the NMOS LVT show f_T and f_{max} superior to 300GHz as presented in Figure 3.4.

3.1.2 Body-Biasing

In order to get a good understanding of the unique body-biasing feature of 28nm FD-SOI, let's start with a small reminder from Bulk CMOS transistors.

In a regular Bulk CMOS technology, a V_T modulation can be obtained by the application of a voltage on the transistors' body ties. But, in such technologies, the V_T of the parasitic source/drain diodes towards the transistors' body limit this effect. Indeed, the body-biasing voltage range is typically only from 0 to 0.3V (modulus) in classic Bulk technology.

In FD-SOI CMOS technology, the thin BOX isolates the front-side transistor from its body. Thus, regarding the V_T modulation through body biasing, the only limiting parasitic diodes are those between deep NWell to P-substrate for NMOS and respectively embedded PWell to deep N-well for PMOS devices. These diodes have opening voltage around 3V (modulus) and thus allow a unique huge range of body-biasing.

Depending on the flavor of the transistors, two type of body biasing can be applied to the active devices. Forward body biasing (FBB) is used to reduce the V_T and, in the opposite way, reverse body biasing (RBB) gives higher V_T level. The Figure 3.5 summarize the biasing mode with respect to transistor flavor.

Transistor Type	Biasing mode and limits (V)	Nominal body biasing
LVT NMOS	FBB: -3 to -0.3	GND
LVT PMOS	FBB: -3 to +0.3	GND
RVT NMOS	RBB: -3 to $\frac{V_{DD}}{2}+0.3$	GND
RVT PMOS	RBB: $\frac{V_{DD}}{2}-0.3$ to +3	VDD

Figure 3.5 – 28nm FD-SOI CMOS technology transistors body biasing mode, limits and nominal voltage.

As depicted in Figure 3.6 for an LVT NMOS, the body factor of both FD-SOI transistor family, LVT and RVT (Regular V_T), is larger than in equivalent Bulk technology. This, with the large body-biasing range, enables a unique wide variation of V_T of around 250mV compared to typically 15mV in Bulk technology.

The figure 3.7 presents the V_T variation range with respect to body-biasing voltage for RVT and LVT devices in 28nm FD-SOI technology.

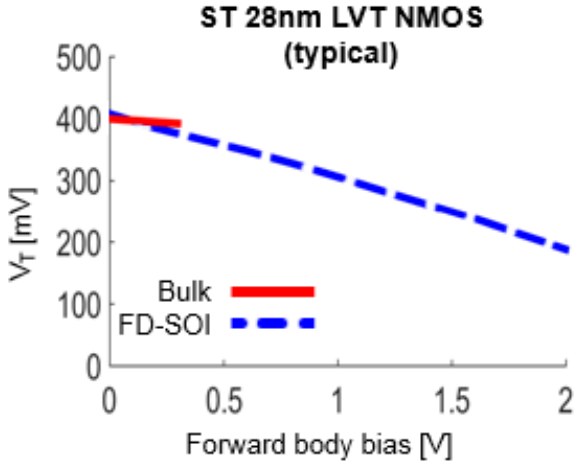


Figure 3.6 – V_T variation comparison between regular Bulk NMOS (in red) and FD-SOI LVT NMOS (in blue).

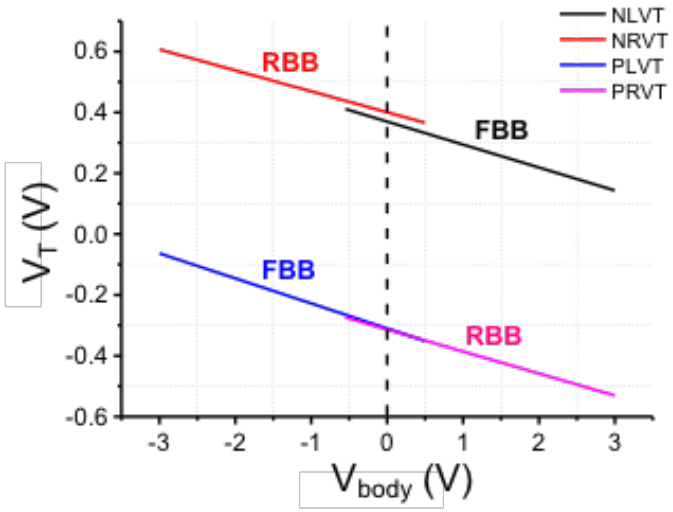


Figure 3.7 – V_T variation range with respect to body-biasing voltage for RVT and LVT devices in 28nm FD-SOI technology [81].

3.1.3 Back-end-of-line

In addition to its active devices, the potential of the 28nm FD-SOI technology for mm-wave and THz application come from its back-end-of-line (BEOL).

Indeed, two different BEOL are actually available in the 28nm FD-SOI technology. One,

which features 8 metal layers (8ML), is ideal for applications from Analog/RF to uW. It is composed by:

- 6 thin copper metal layer of the same thickness. (M1 to M6)
- 2 thick copper metal layer. (IA and IB)
- A thick aluminum metal layer (LB, sometimes named AluCap)

The thin metal layers are principally used for routing of digital part of systems. Indeed, the very small thickness of these metal layers induces high losses at high frequency.

The second BEOL is featuring 10 metal layers. The two additional layers, named B1 and B2, are located between M6 and IA and have intermediate thickness. The 10ML BEOL option is more adapted for complex systems and circuits operating from RF to THz frequencies. Indeed, thanks to the addition of two layers, the two last copper layers and the alucap are farther from the substrate and hence allow lower losses and higher Q factor passive devices.

For all these reasons, the circuits implemented in this thesis are designed in the 10ML BEOL 28nm FD-SOI CMOS technology from ST Microelectronics. This BEOL is depicted in Figure 3.8.

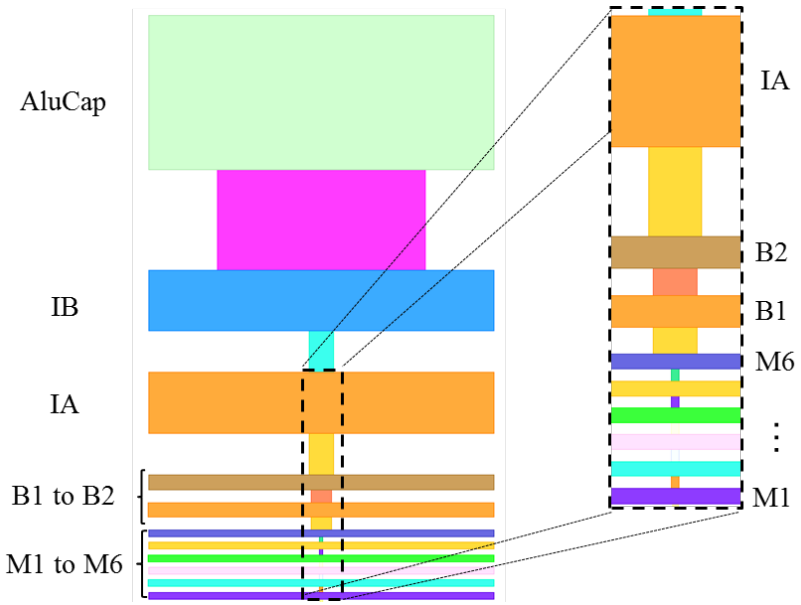
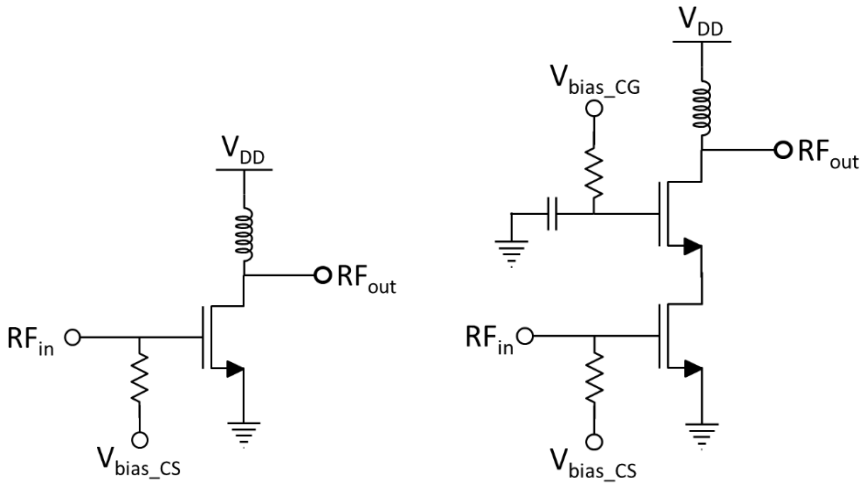


Figure 3.8 – 10 metal layers back-end-of-line of 28nm FD-SOI CMOS technology from ST Microelectronics.

3.2 Distributed oscillator design methodology

3.2.1 Amplification stage

The first step to design a distributed oscillator is to make a choice for the amplification stage topology. The most used one is the common source topology. Indeed, this topology, depicted in figure 3.9(a), allows a fast and easy implementation. It offers an excellent linearity thanks to the high voltage swing achievable at the output and thus allows a good phase reconstruction between the stages.



(a) (b)

Figure 3.9 – (a) Common source topology and (b) cascode topology scheme.

However, this topology can suffer from parasitic elements. The drain-to-source capacitance can reduce the stage gain due to the decrease of the output impedance. The gate-to-drain capacitance is another drawback. In fact, coupled with Miller effect, this capacitance can significantly reduce the stage bandwidth.

Others topologies are possible. As a matter of example, the cascode topology which is presented in figure 3.9(b) can be an option to reduce the Miller effect and thus resulting in higher output power level and wider bandwidth. A higher output power level is also achievable thanks to a possible higher power supply.

Nevertheless, with this structure, the use of high power supply results in high power consumption. Moreover, the parasitic elements introduced between the common-source and the common-gate transistors can significantly reduce the performances.

The most important parameters for the amplification stage are transistor's f_T and f_{max}.

From the S parameters of the 4-ports amplification stage, it is possible to extract these two parameters.

The cutoff frequency f_T is, by definition, the frequency at which the current gain is unity. The current gain H21 can be express from S parameters by:

$$H21 = \frac{-2 \cdot S21}{(1 - S11)(1 + S22) + S12\,S21} \ . \tag{3.1}$$

The maximum oscillation frequency is defined as the frequency at which the maximum stable power gain is equal to unity. The maximum stable power gain can be expressed from S parameters by:

$$G_{MAX} = \left(K - \sqrt{K^2 - 1}\right) \frac{|S21|}{|S12|}, \text{ for } K > 1 \ . \tag{3.2}$$

The K-factor is named Rollett's stability factor. If $K > 1$ then the quadripole is stable. The K-factor can be express from S parameters as:

$$K = \frac{1 - |S11|^2 - |S22|^2 + |\Delta|^2}{2\ |S21\,S12|} \tag{3.3}$$

, with

$$\Delta = S11\,S22 - S21\,S12 \ . \tag{3.4}$$

The f_{max} is also achievable by taking the frequency at which Mason's gain is equal to unity. Mason's gain function U can be express from the Y-parameters of a quadrupole as:

$$U = \frac{|Y21 - Y12|^2}{4\,[Re\,(Y11)\ Re\,(Y22) - Re\,(Y12)\ Re\,(Y21)]} \ . \tag{3.5}$$

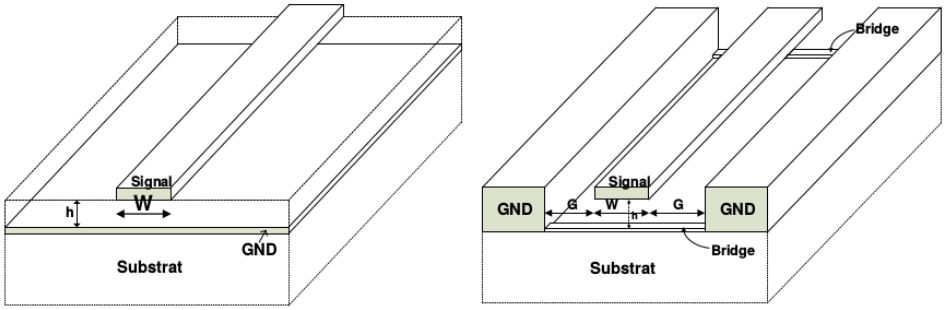
In a distributed oscillator, the theoretical maximum oscillation frequency can be expressed as function of f_T [83] as :

$$f_{max} = \frac{\pi}{2} \cdot f_T \ . \tag{3.6}$$

It is important to keep in mind that this equation is true only in an ideal case with a loop gain exactly equal to one.

3.2.2 Transmission line

After the amplification stage topology choice, the next step is the transmission line (TL) topology choice. Several line topologies exist: microstrip (MS), coplanar (CPW), slotline, stripline, etc... The two most used structures in millimeter-wave integrated circuits are the microstrip line and the coplanar line, as shown in Figure 3.10.



(a) (b)

Figure 3.10 – (a) Microstrip topology and (b) coplanar topology scheme.

- The microstrip line consists of a grounded conductive ribbon. The line and its ground plane are separated by a dielectric material. The main drawback of this topology is the low range of characteristic impedance achievable in standard embedded technology. Indeed, a MS line has only two degrees of freedom, the conductor width (W) and the dielectric thickness (h). Nevertheless, the major part of the electric field is concentrated between the conductor and the ground plane. This makes this solution attractive for low resistivity substrate technology.

- The coplanar line consists of a central conductor ribbon and a ground plane on each side of the ribbon. The new degree of freedom offered by the distance between the ground plan and the line (G) allows reaching a wider range of characteristic impedances. The electric field is largely concentrated between the conductor line and the ground plane. However, part of the electric field penetrates the substrate, which makes this topology extremely sensitive to substrate resistivity. Bridges are distributed at regular intervals to ensure that the ground plane homogeneity.

The TL topology choice depends on the constraints of the intended application and of the constraints of the used technology. In a dense very large scale integration (VLSI) CMOS technology, as the 28nm FD-SOI technology, the layout constraints coming from the density rules make that MS topology has always lateral grounded walls. It is thus important to take these walls into account from the beginning of the design. These lateral walls must be far enough from the TL to ensure that the major part of the electric field is concentrated between the line and the ground plane and thus have no significant impact

on the TL properties if this distance change due to layout constraint. For a high efficiency distributed oscillator design, the TL width must be sufficient to reduce transmission losses. In addition, the return path must be perfectly mastered with a uniform ground plane.

The first step in transmission line characterization is to determine the characteristic impedance Z_c and the complex propagation constant γ. To do this, it is possible to exploit the S parameters coming from an electromagnetic simulation.

Indeed, the characteristic impedance can be written as:

$$Z_c = 50 \cdot \sqrt{\frac{(1+S11)(1+S22) - S12\,S21}{(1-S11)(1-S22) - S12\,S21}} \ . \tag{3.7}$$

And the complex propagation constant is obtained from:

$$\gamma = \frac{1}{l} \cdot \operatorname{acosh}\left(\frac{(1+S11)(1-S22) + S12\,S21}{S12+S21}\right) \tag{3.8}$$

, with l the length of the transmission line. The complex propagation constant can be rewritten as:

$$\gamma = \alpha + j \cdot \beta \ . \tag{3.9}$$

The real part α represents the attenuation constant. It is usually expressed in dB/m. The imaginary part β is the phase constant. It represents the phase-shift per unit length in rad/m. The effective permittivity ϵ_{eff} of the dielectric material is reduced from β by:

$$\epsilon_{eff} = \left(\frac{\lambda_0 \beta}{2\pi}\right)^2 \ . \tag{3.10}$$

Finally, the quality factor of the transmission line is given by:

$$Q_{TL} = \frac{\beta}{2\alpha} \ . \tag{3.11}$$

A transmission line can be modeled with an RLCG model as depicted in figure 3.11. The model parameters R, L, C and G are respectively the unit length resistance, inductance, capacitance and conductance. They can be express from the equations (3.12) to (**??**).

$$R = Re\,(Z_c \cdot \gamma) \ \ [\Omega/m] \ , \qquad L = \frac{Im\,(Z_c \cdot \gamma)}{2\pi f} \ \ [H/m] \ , \tag{3.12}$$

$$C = \frac{Im\,(\gamma/Z_c)}{2\pi f} \ \ [F/m] \ , \qquad G = Re\,(\gamma/Z_c) \ \ [S/m] \ . \tag{3.13}$$

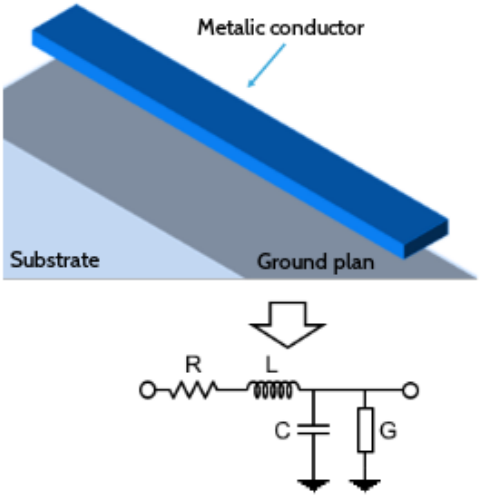


Figure 3.11 – Equivalent RLCG model of a transmission line.

This RLCG model is correct for line length smaller than λ/20. Otherwise, it is necessary to divide the line into several stages to improve the modeling accuracy, as illustrated by the figure 3.12.

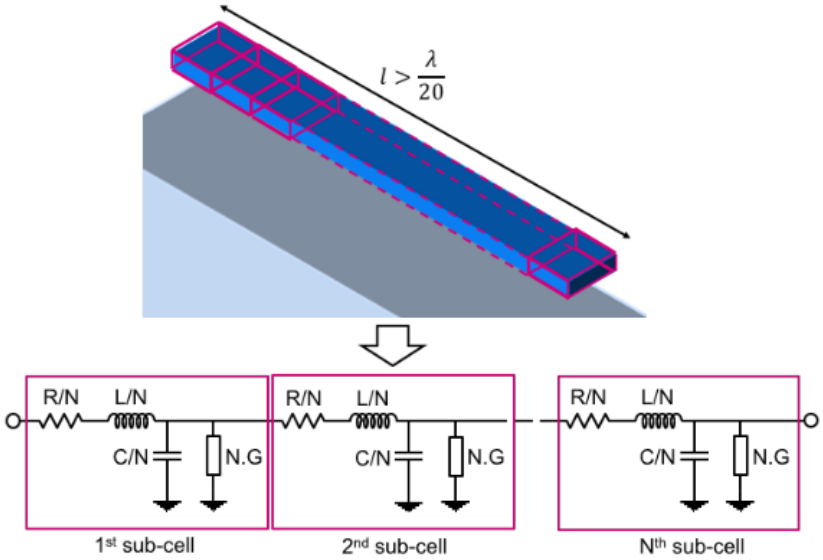


Figure 3.12 – Equivalent RLCG model of a transmission line with length over λ/20.

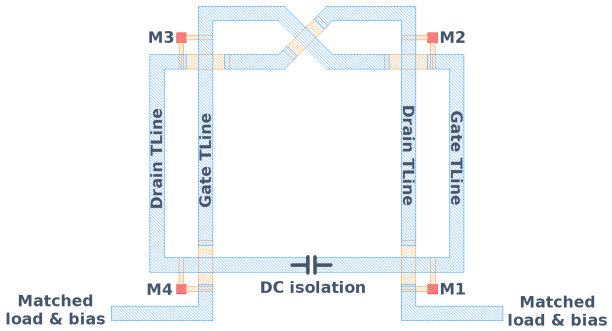
In advance silicon technology, a transmission line generally presents a low quality-factor and high losses. This is mainly due to the low substrate resistivity, the low distance to the substrate and the limited line width.

3.2.3 Form factor and stage number

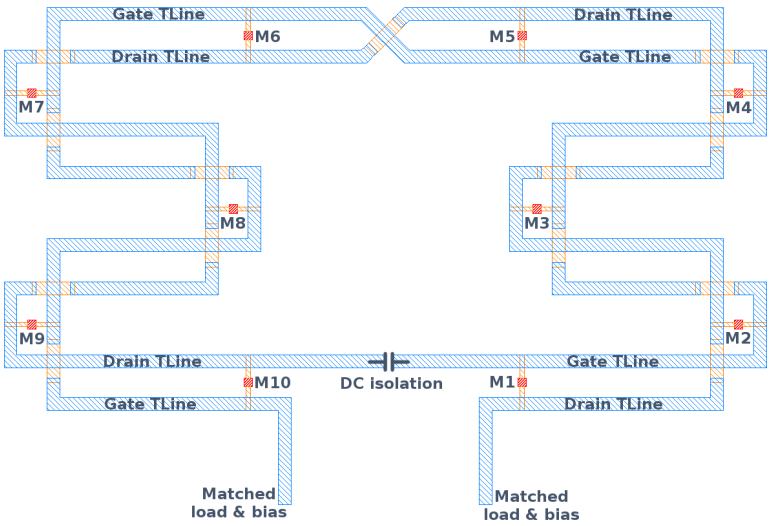
Knowing the transmission line parameters, the next step is to define the number of amplification stages and to choose the distributed oscillator form factor.

The number of amplification stages and the form factor are linked. They depend on the available space, the total length of the line, the transmission line losses and the amplification stage gain.

It is important that the drain and gate electrical length stay equal between two amplification stages. This guarantees a good phase reconstruction of the signal through the



(a)



(b)

Figure 3.13 – Distributed oscillator form factor examples with (a) 4 stages in square shape and (b) 10 stages in boustrophedon shape.

transmission line. Thus, the form factor must respect some symmetries. The figure 3.13 present some form-factor example schemes.

With a given form factor and amplification stage number, the distributed oscillator will maintain oscillation if the total loop gain is higher than the transmission line losses. If this oscillation is maintained, the final step is to check all wanted specifications.

Through this section, we provided a methodology to design a mm-wave distributed oscillator. The figure 3.14 synthesize this methodology, highlighting all the important steps in distributed oscillator design. This methodology has been used to design the distributed oscillators presented in the next section.

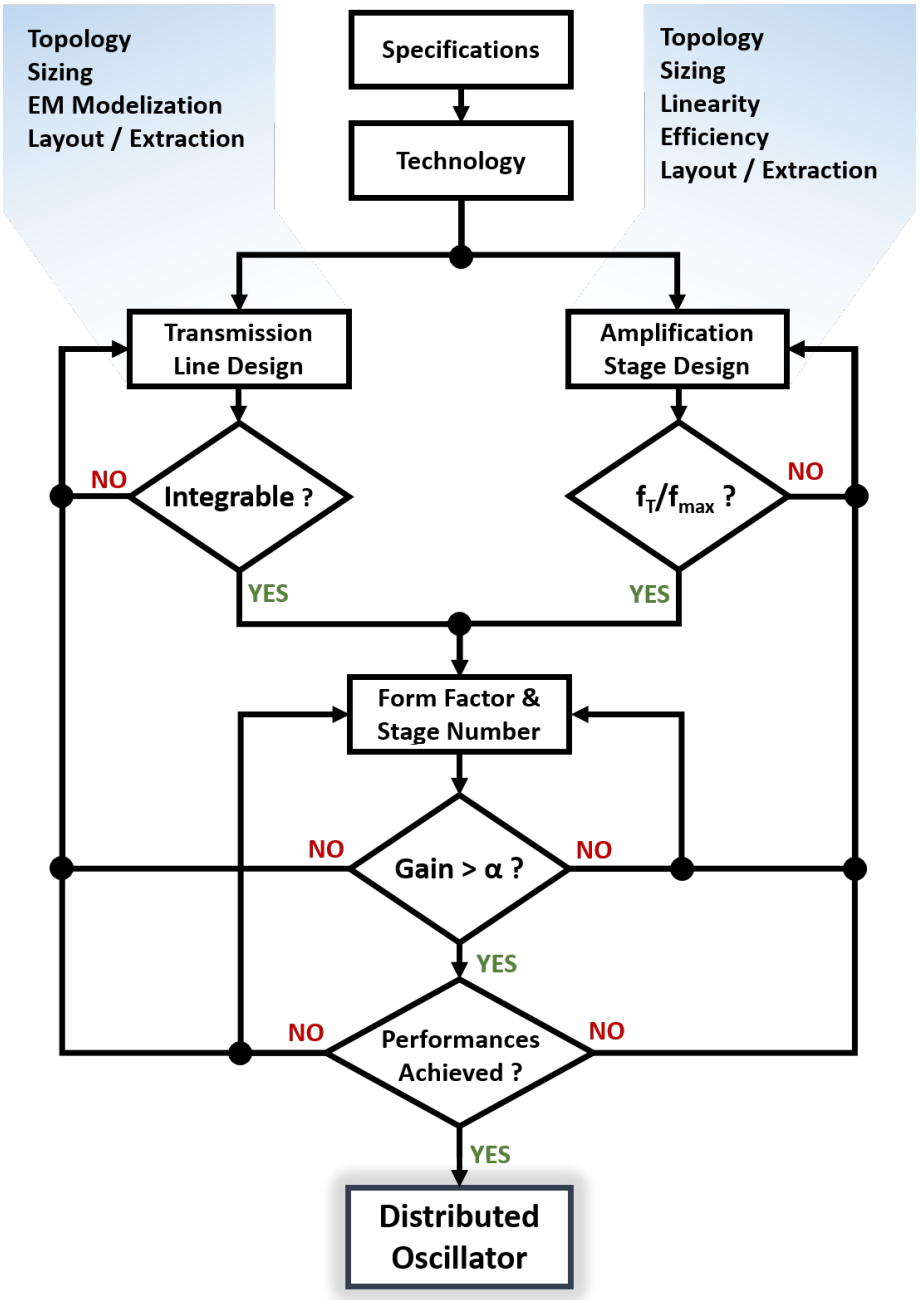


Figure 3.14 – Distributed oscillator design methodology diagram.

3.3 Energy efficient 135 and 200 GHz distributed oscillators design

The design specifications are resumed in table 3.1

Oscillator Topology	Distributed Oscillator
Oscillation Frequency	$\tilde{1}$35Ghz and $\tilde{2}$00GHz
Output Power	Higher than 0dBm
DC-to-RF Efficiency	Higher than 5%
DC Power Consumption	20mW (On 1V supply)
Phase Noise @ 1MHz	Lower than -90 dBc/Hz

Table 3.1 – Distributed oscillators design specifications.

3.3.1 Amplification Stage Design

The circuits have been implemented made in 28nm FD-SOI CMOS technology from ST Microelectronics. In these designs, only L-min LVT NMOS transistors have been used. Indeed, LVT transistors provide higher performances in terms of f_T/f_{max}.

To realize the amplification stages, a common source topology was chosen. Indeed, as said in the previous section, this topology allows high efficiency, high linearity, and a good output power.

A transistor with a total width of W_{tot} is composed of several fingers of with a width W_f (3.14).

$$W_{tot} = N_f \cdot W_f \ , \tag{3.14}$$

The finger width W_f is critical for millimeter applications. It is indeed directly connected to the gate resistance responsible for the f_{max} degradation. Charts have been published in [84] (figure 3.15(a)) in order to select the appropriate gate width W_f according to the technological node.

Even if the 28nm technology node is not reported, this chart allows making the projection that the optimum gate finger width is around 0.8µm. This value has been confirmed by early simulations with the 2.5f design kit version of 28nm FD-SOI technology, as shown in figure 3.15(b).

A transistor with a total width W_{tot} can be composed of one or several cells, as presented in figure 3.16

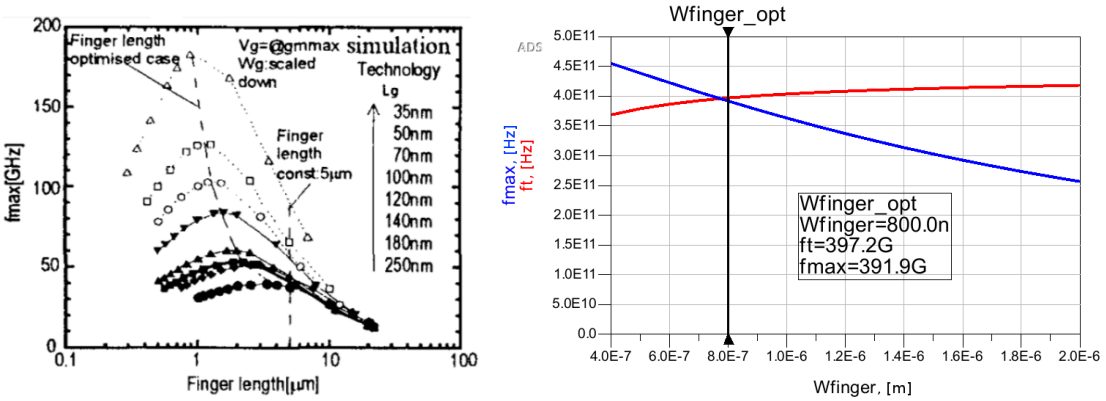
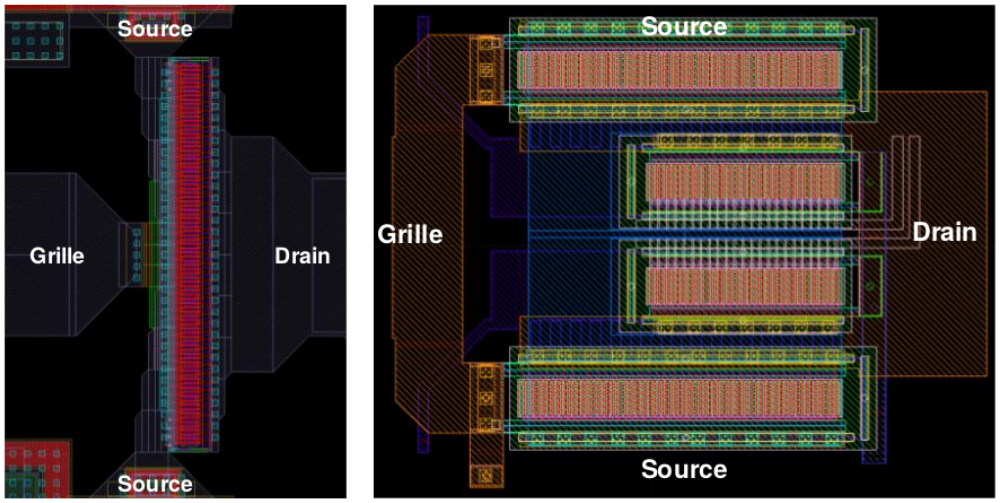


Figure 3.15 – Finger width determination: (a) charts proposed in [84] and (b) 28nm FD-SOI NMOS f_T/f_{max} simulations as a function of finger length at a constant current density.



(a) (b)

Figure 3.16 – Example of transistor layout from [82]: (a) single cell transistor and (b) multiple cells transistors (The topology on the right contains two different sizes transistors split each into two other ones).

The layout in figure 3.16(a) is suitable for small transistors with only one gate access. The layout in figure 3.16(b) allows two gate accesses on each transistor sub-cells. This highly improves the reliability of the component by limiting its stress.

The total transistor width is estimated according to the desired output power and the current density in the transistor. The optimal current density $J_{DS|opt}$ is around 0.3mA/µm. This value is independent of the technology as it as been demonstrate by [85].

In our case, the specification is to have a total power consumption of 20mA. Thus, assuming 4 amplification stages, each stage has to be biased at around 5mA. From this and the optimal current density, the optimal total transistor width $W_{tot|opt}$ of each amplification stage is deduced using (3.15).

$$W_{tot|opt} = \frac{I_{DC|stage}}{J_{DS|opt}} \approx 16\mu m \ . \tag{3.15}$$

Our amplification stage transistor is finally sized. The total width is equal to 16µm and the optimal finger width is 0.8µm, with 20 fingers.

The next step is to layout specific access in order to minimize the effect of the full BEOL on the f_T/f_{max}. The small-signal model of a MOS transistor with its interconnection parasitic elements is depicted in figure 3.17.

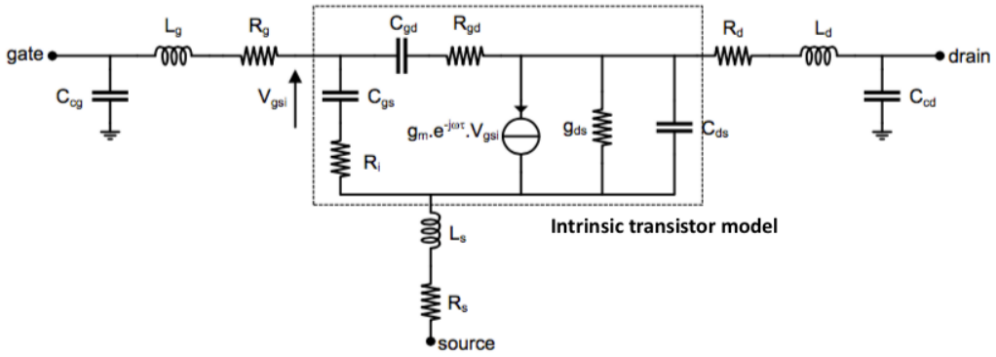


Figure 3.17 – Small-signal model of MOS transistor with its interconnections [86].

Equations (3.16) and (3.17) present respectively the f_T and f_{max} equations deduced from the small-signal schematic.

$$f_T \approx \frac{g_m}{C_{gs}\sqrt{1+2\frac{C_{gd}}{C_{gs}}}} \ . \tag{3.16}$$

$$f_{max} \approx \frac{g_m}{4\pi C_{gs}\sqrt{(R_g+R_s+R_i)\left(g_{ds}+g_m\frac{C_{gd}}{C_{gs}}\right)}} \ . \tag{3.17}$$

From (3.16) and (3.17) it is obvious that f_T/f_{max} performances are degraded by the parasitic interconnections. Several techniques have been used here to reduce the effect of the BEOL interconnection and thus optimize the overall transistor performances.

First of all, to reduce parasitic capacitance, it is possible to use thin staircase accesses for the drain and the source as shown in figure 3.18. These accesses allow low drain-to-source parasitic capacitances, as well as the drain and source surface facing the gate is reduced. Using these techniques, [82, 86] reports f_{max} amelioration of almost 20% comparing to classic layout method for the full BEOL layouted transistor.

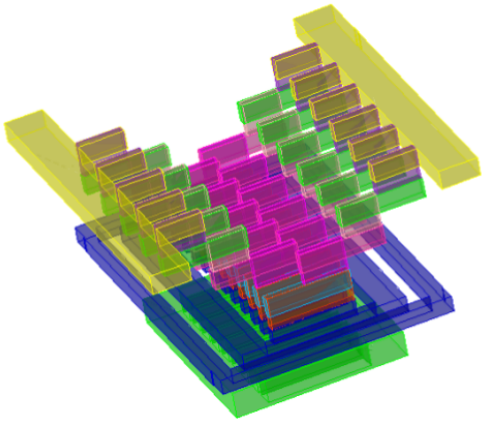


Figure 3.18 – Example of layout with thin staircase accesses for drain and source [82].

A second optimization is the use of a dual gate access. As reported in [87], the use of dual gate accesses reduces the gate access resistance. In [82, 86], the author report an f_{max} amelioration of approximately 8% comparing single gate access transistor, as shown in figure 3.19.

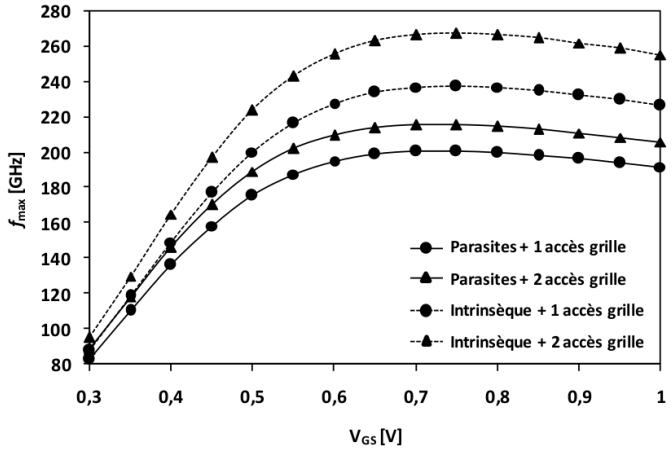


Figure 3.19 – Impact of dual gate access on f_{max} [82].

The figure 3.20 present the optimized BEOL of the amplification stage transistor. A 3D view is also available in figure 3.21(a), while figure 3.21(b) presents a cross sections through the plane A.

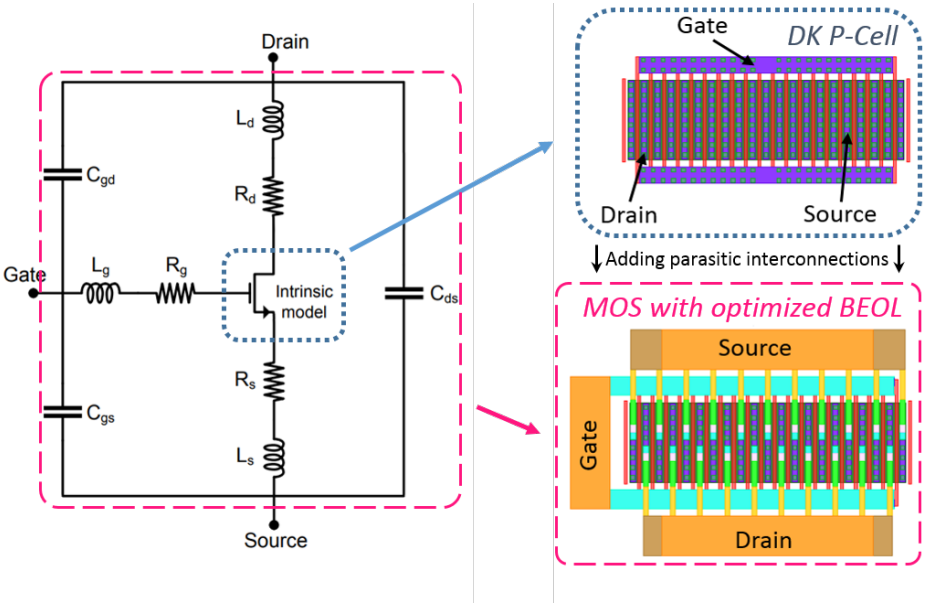
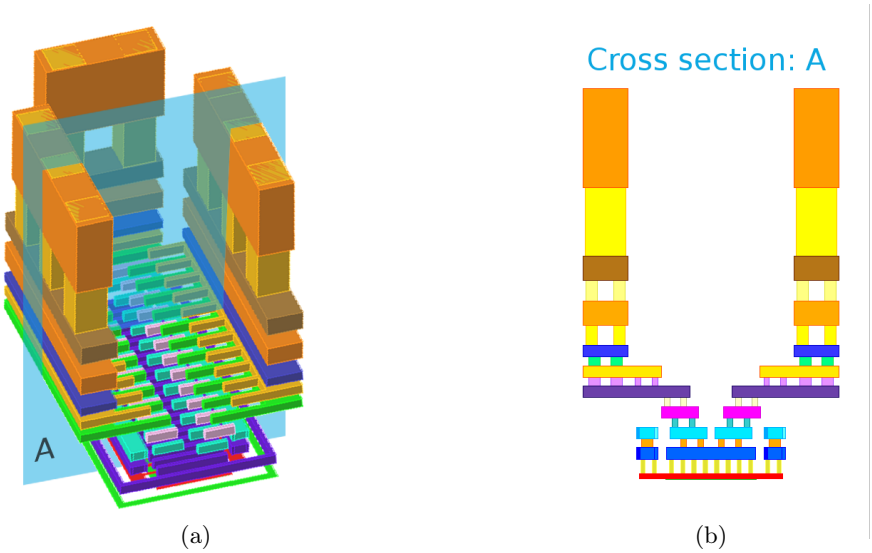


Figure 3.20 – BEOL layout optimization of the amplification stage transistor.



(a) (b)

Figure 3.21 – Transistor layout with optimized BEOL (a) 3D view and (b) cross section on the plane A.

At this point, post-layout simulations must be made to evaluate the impact of the full BEOL on the f_T/f_{max} performances. To extract the parasitic capacitances and resistance RCc extraction was performed using StarRCXT tool [88].

The parameters f_T/f_{max} are calculated using (3.1) and (3.2) times the frequency. The figure 3.22 presents the f_T/f_{max} results with and without BEOL.

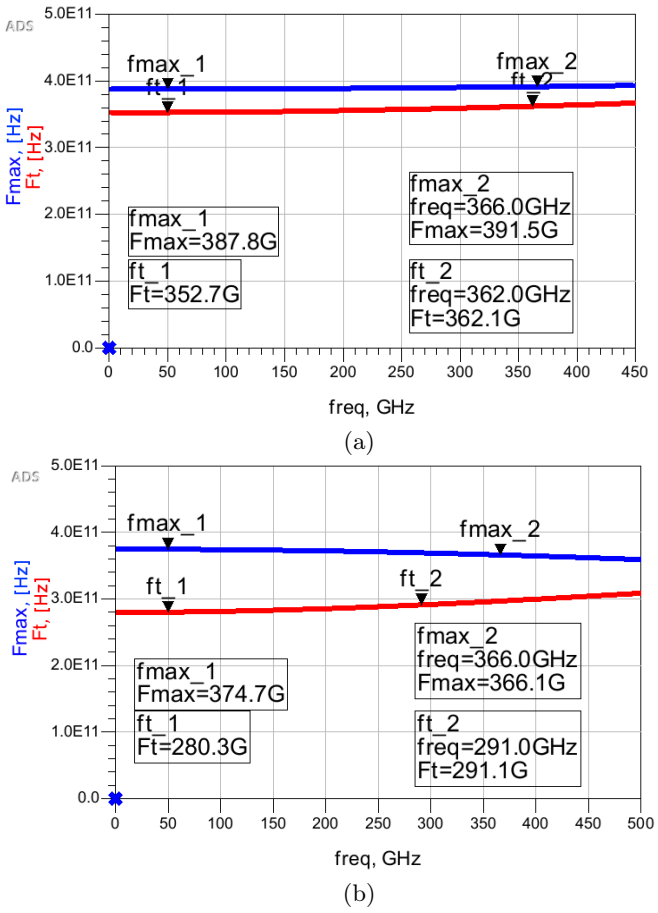


Figure 3.22 – f_T/f_{max} performances of (a) the Design kit PCell up to M1 and (b) PCell with full BEOL.

As expected, the gate access optimization permits a very small degradation of f_{max} with the full BEOL. The design kit P-Cell, which is up to metal 1, was simulated with an f_{max} of approximately 390GHz while this value is near 370GHz with the optimized BEOL.

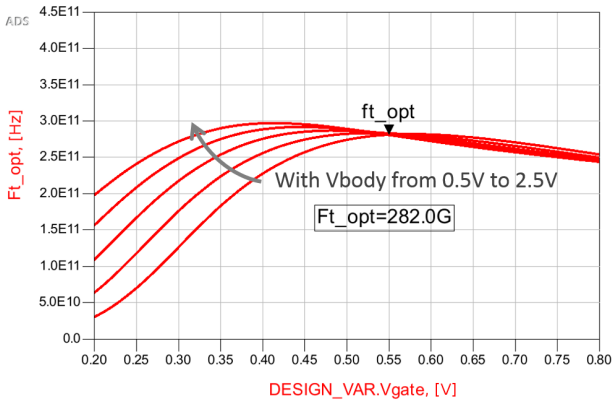
The P-Cell f_T was simulated at 360GHz. With the proposed BEOL, this value rushed approximately 280GHz. The table 3.2 resumes theses values.

As explained at the beginning of this chapter, it is possible to modulate the NMOS V_T

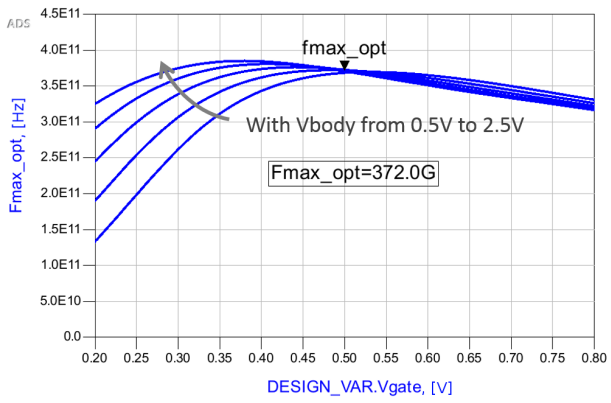
	Simulation with DK P-Cell	Simulation with P-Cell + BEOL
f_T	360 GHz	280 GHz
f_{max}	390 GHz	370 GHz

Table 3.2 – f_T and f_{max} simulations with and without BEOL parasitic interconnections.

using the transistor body-bias feature. To ensure that the transistor always works at its optimum, it is important to study the effect of body-bias on the f_T/f_{max}. Figure 3.23 presents the f_T/f_{max} as a function of gate voltage for several body voltages. The body voltage is here sweep from 0.5V to 2.5V by 0.5V steps.



(a)



(b)

Figure 3.23 – Effect of the body-biasing on f_T/f_{max}. (a) f_T and (b) f_{max} as a function of Vgate for sevegal Vbody.

It is noteworthy that the optimum bias point (i.e. the optimum gate voltage) is not necessary at maximum f_T, respectively f_{max}. Indeed, as visible in figure 3.23, it provides the gate voltage at which f_T, respectively f_{max}, does not change with body biasing. This

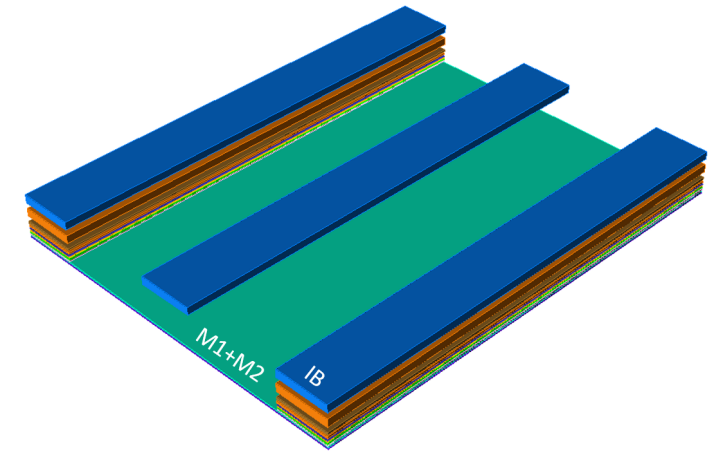
gate voltage is equal to 0.55V for f_T and 0.5V for f_{max}. Thus, it appears judicious to choose a gate voltage optimum point between 0.5V and 0.55V.

3.3.2 Transmission Line Design

To choose the transmission line topology, it is important to take into account the distributed oscillator operating environment from the beginning. Indeed, a distributed oscillator transmission line must be loaded with a matched load. Thus, the transmission line characteristic impedance must be chosen accordingly.

To simplify our design, we choose to load the distributed oscillator with the measurement spectrum analyzer. As this kind of test equipment has usually 50 Ohm ports, we choose to design a 50 Ohm transmission line.

To reduce at maximum the substrate losses, we chose to use a microstrip (MS) line with a ground plane on metal 1 and metal 2. Nevertheless, due to layout density rules, it is almost impossible to have a perfect MS line. Thus, as presented in figure 3.24, the implemented structure was a microstrip with grounded all levels metal walls.



(a)

(b)

Figure 3.24 – Proposed transmission line topology.

This kind of topology is usually called grounded coplanar lines (CPW-G). Nevertheless,

in our case, the grounded walls are far enough from the line to ensure that the major part of the electric field is still concentrated between the line and the ground plane.

As explained in the previous section, the first step in transmission line characterization is to determine the characteristic impedance Z_c and the complex propagation constant γ. Using the Momentum electromagnetic (EM) tool, it is possible to extract the transmission line S parameters.

The figure 3.25 presents the extracted Z_c and γ of the proposed transmission line over 1mm by using equations (3.7) and (3.8). It is noteworthy that our 50 Ohm 1mm length transmission line corresponds to a full wavelength at around 171 GHz.

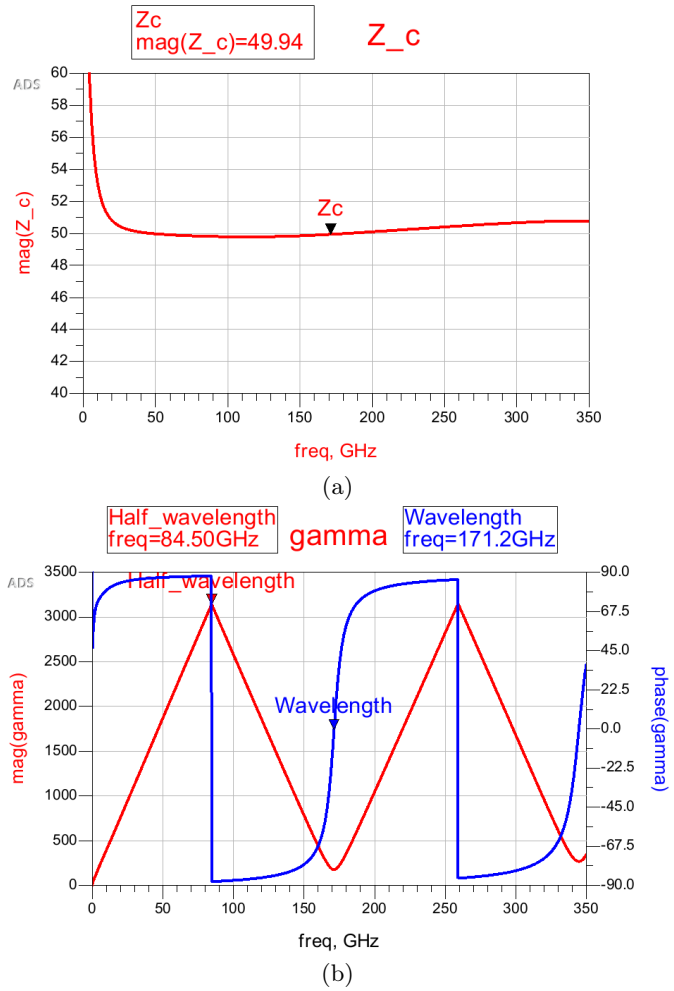


Figure 3.25 – Electromagnetic extraction of transmission line (a) characteristic impedance Z_c and (b) complex propagation constant γ over 1mm.

From the real part of γ (see equation (3.9)), it is possible to extract the attenuation constant α, presented in figure 3.26(a). From these results, it is possible to determine the losses per millimeter. For example, our transmission line exhibits around 1.7dB/mm losses at 200GHz.

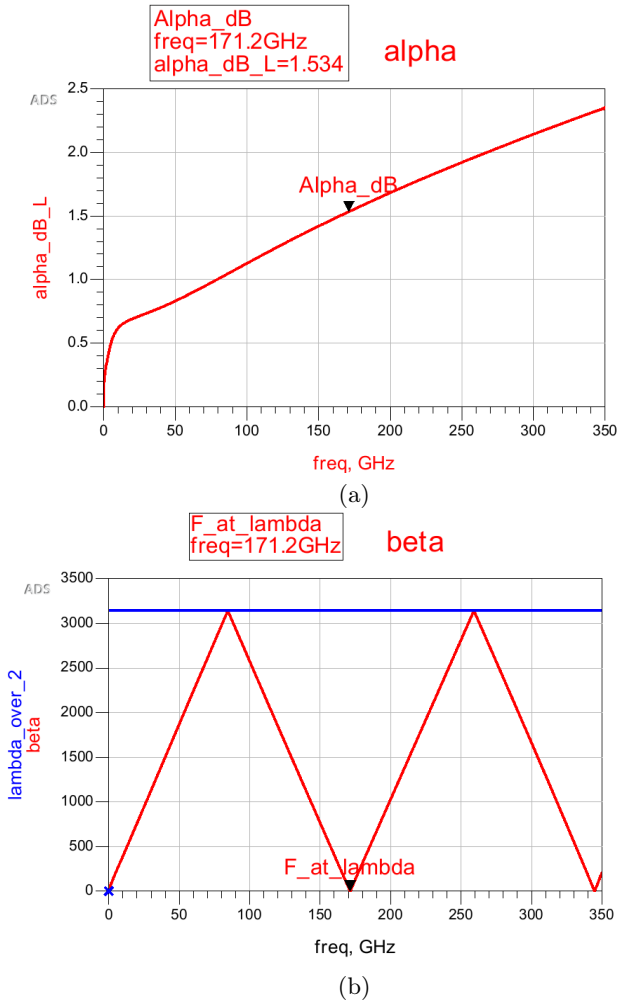


Figure 3.26 – Electromagnetic extraction of transmission line (a) attenuation constant α and (b) phase constant β over 1mm.

The imaginary part of γ is the phase constant β, presented in figure 3.26(a). It represents the phase-shift per unit length in rad/m. Thus, it increases until a maximum at which the wavelength is equal to $\lambda/2$ (modulus λ). Then, since the phase-shift have a modulus of 2π, the phase-shift will decrease to zero. At zero, it corresponds to a full wavelength phase-shift. Thus, if one looped back a transmission line of 1mm and assuming no losses in the transmission line, oscillations must appear at around 171.2 GHz.

By considering a small part of the transmission line, typically smaller than $\lambda/20$, it is now possible to extract an RLCG model to use it to size our distributed oscillator. Figures 3.27(a-d) present respectively the resistance R_u, inductance L_u, capacitance C_u and conductance G_u per unit length of our transmission line.

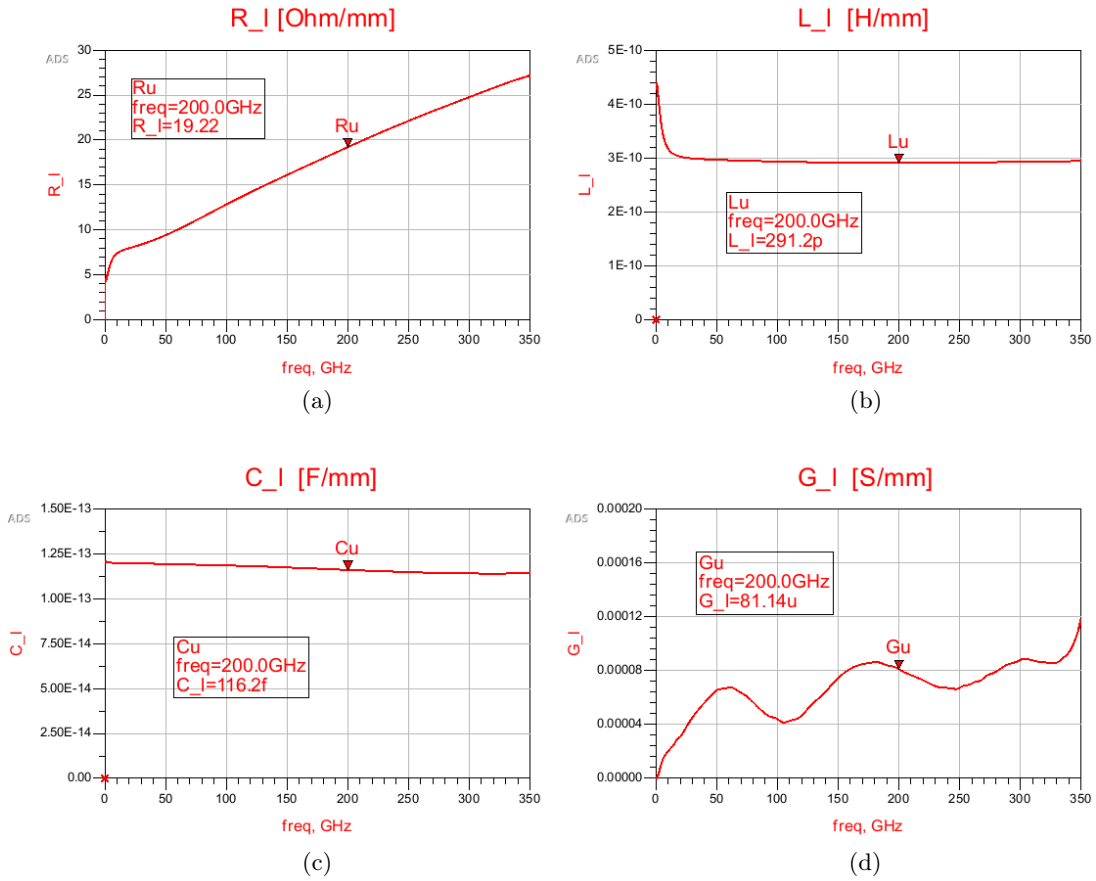


Figure 3.27 – Extracted RLCG model of proposed transmission line. (a) Resistance R_u, (b) inductance L_u, (c) capacitance C_u and (d) conductance G_u per unit length.

By substituting L_u and C_u in equation (2.56) (see section 2.3.2 of Chapter 2) and by rewriting this equation, it is now possible to calculate the total line length l_{tot} needed to oscillate at a given frequency.

$$l_{tot} = 2nl = \frac{1 - \Delta\varphi/\pi}{f_{osc}\sqrt{L_u C_u}} \ . \tag{3.18}$$

At this point, the only unknown parameter is $\Delta\varphi$. As presented in section 2.3.2 of Chapter 2, this parameter represents the amplification stage additional phase-shift due to parasitic effect at mm-wave and THz frequencies.

To calculate this added phase-shift, it is necessary to know the distance between the drain and gate lines. Indeed, the connection accesses between the TL and the amplification stage will also influence this parameter.

A way to do this is to fix the distance between the drain and gate lines and calculate the added phase-shift in this configuration. Then calculate l_{tot} using equation (3.18) and check if it exists a form factor allowing this line spacing and this line length. Several iterations can be necessary to find a solution.

To fix the distance between the drain and gate lines, a trade-off appears. Indeed, the two lines have to be far enough to not significantly impact each other. But, they also have to be close enough to minimize the added phase-shift and to allow to close the loop. In our cases, the simulated added phase-shift are 0.37π at 135 GHz and 0.48π at 200GHz. Corresponding to a total TL length of approximately $800\mu m$ for the 135 GHz DO and $450\mu m$ for the 200GHz DO, as resumed in table 3.3.

Assuming a linear approximation for the added phase-shift, it is possible to draw the TL total length as a function of the targeted oscillation frequency, as depicted in figure 3.28.

Targeted frequency	135 GHz	200 GHz
Added phase-shift	0.37π	0.48π
Corresponding TL length	$800\mu m$	$440\mu m$

Table 3.3 – Determination of the transmission line total length as a function of targeted oscillation frequency.

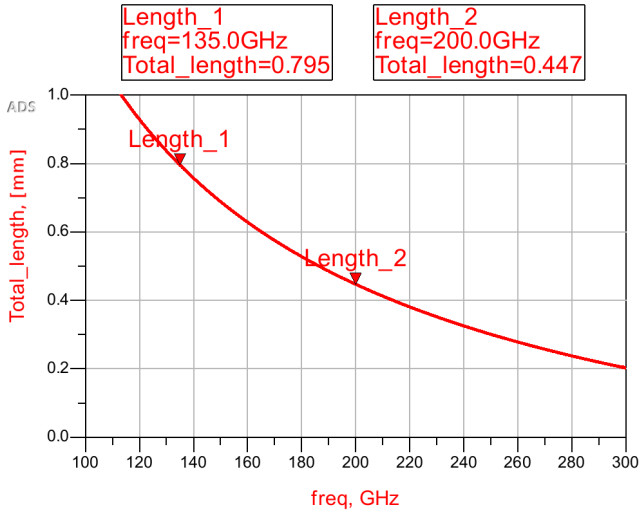


Figure 3.28 – Transmission line totel length as a function of targeted oscillation frequency.

3.3.3 Other passives design

To perform the DC isolation between gate and drain lines, an *ad-hoc* MoM capacitance has to be designed. To reduce insertion losses and to minimize parasitic capacitance to ground, we choose to draw this capacitance only on the top metal layer. Figure 3.29 illustrate this capacitance.

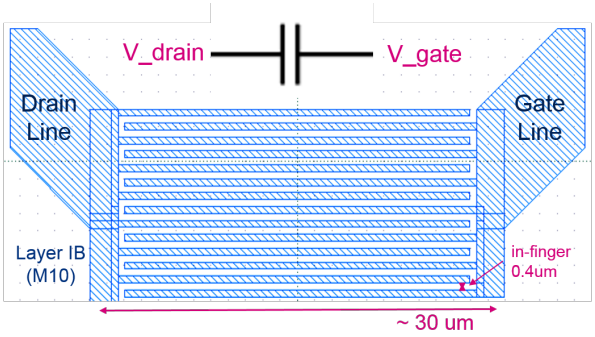


Figure 3.29 – DC isolation *ad-hoc* MoM capacitance drawn on IB layer (metal 10).

Finally, the RF pads have to be carefully considered. Indeed, they add parasitic capacitance to ground at mm-wave and THz frequencies. In our case, the GSG RF pads (Ground Signal Ground) have to be compatible with both 100µm and 50µm pitch probes. (Depending on the bench, the used probes are: Infinity Waveguide Probes from Cascade [89] and Microwave Testing Waveguide probes from Picoprobe [90].)

We proposed a new RF pad design to minimize the parasitic capacitance and allow compatibility with both 100µm and 50µm pitch probes. The designed RF pad is presented in figure 3.30. It is noteworthy that the central pad is only 40.5x22.5μm^2 (taking into account the 0.9 shrink factor) which is the minimum allowed for the used 100µm probes. The extracted parasitic capacitance of this RF pad is presented in figure 3.31.

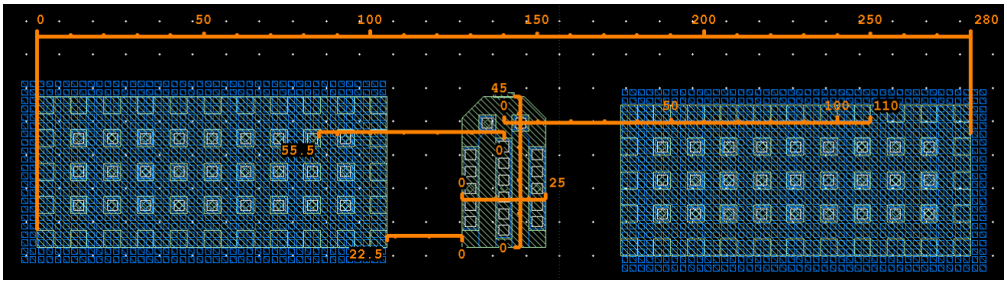


Figure 3.30 – Designed RF pad with 100µm and 50µm pitch probes compatibility.

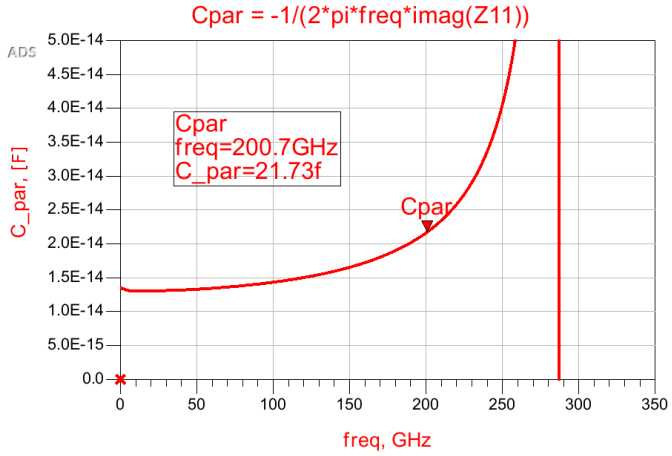
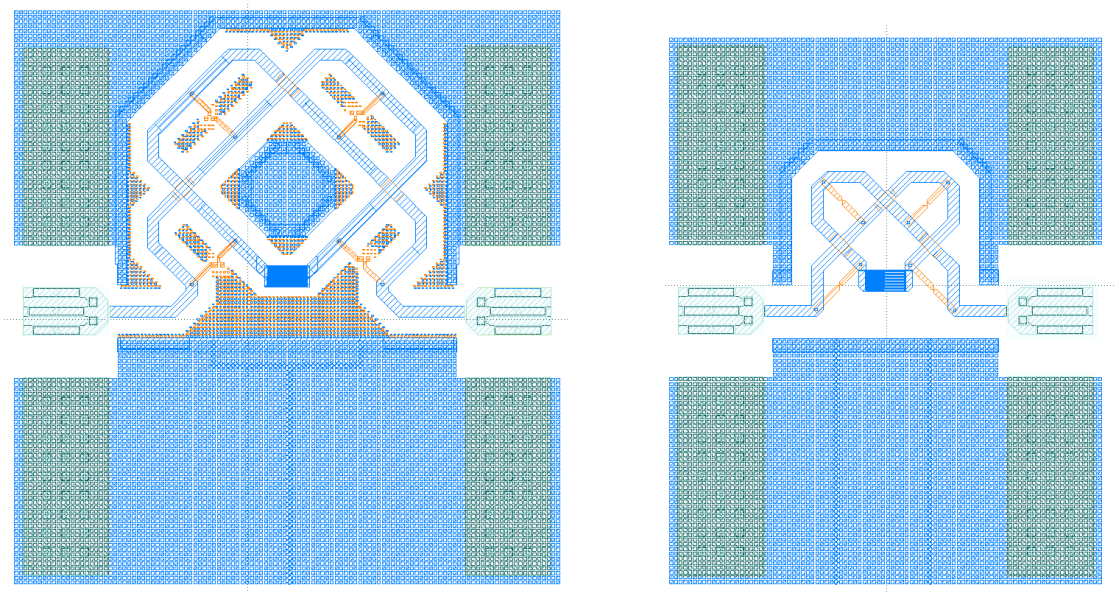


Figure 3.31 – Extracted parasitic capacitance of designed RF pad.

3.3.4 Final layout

Figures 3.32 present the layout views of the two designed distributed oscillators at 135 GHz and 200 GHz, at the same scale factor. On the figure 3.32(a), several metal dummies are visible. This tiling has been performed by hand to ensure good placement and minimum degradation on the distributed oscillation behavior.



(a) (b)

Figure 3.32 – Layout views of the (a) 135GHz and (b) 200GHz distributed oscillators.

Several versions of the two oscillators have been fabricated. It is noteworthy that in the last version of the 200GHz (which is presented in figure 3.32(b)) metal dummies have been removed thanks to ground plan density optimization and chip placement optimization. Indeed, the design rules density check is performed by sliding a square check windows with fixed width and applying rules in the windows at each iteration. Thus, by optimizing the chip placement and the border ground plane density, it is possible to clean density rules without metal dummies.

3.4 Chapter conclusion

This chapter has presented the design of mm-wave and THz sources in advance silicon technology. After a brief introduction of the 28nm FD-SOI technology from ST Microelectronics for mm-wave applications, a distributed oscillator design methodology has been proposed.

This methodology is largely based on electromagnetic simulations. This work has helped to redefine the STMicroelectronics mm-wave design flow by centralizing the use of electromagnetic extraction tools such as Momentum. In addition, very particular attention has been paid to post-layout simulations which, at these operating frequencies, are the only ones guaranteeing a proper circuit operating.

Two energy efficient mm-wave and THz distributed oscillators have been designed following the introduced design methodology. These two distributed oscillators take advantage of the high-frequency performances of the 28nm FD-SOI technology and have contributed to validate the mm-wave design flow.

In the next chapter, experimental results of these two oscillators will be presented and injection-locked capability of such of oscillators will be demonstrated.

4 Experimental results

This chapter will present the experimental results of this thesis work. First, a study will be performed on a standalone transistor in order to well understand its behavior at mm-wave and THz operation frequency.

Then, the two distributed oscillators presented in the previous chapter will be tested. A variability study is presented highlighting the very low process variability of such of architecture. Then, phase noise shaping feature of our oscillators is presented, allowing fine-tuning of the oscillator phase noise using the FD-SOI body bias feature.

Finally, injection trials are presented in order to demonstrate the injection locked capability of such of oscillators.

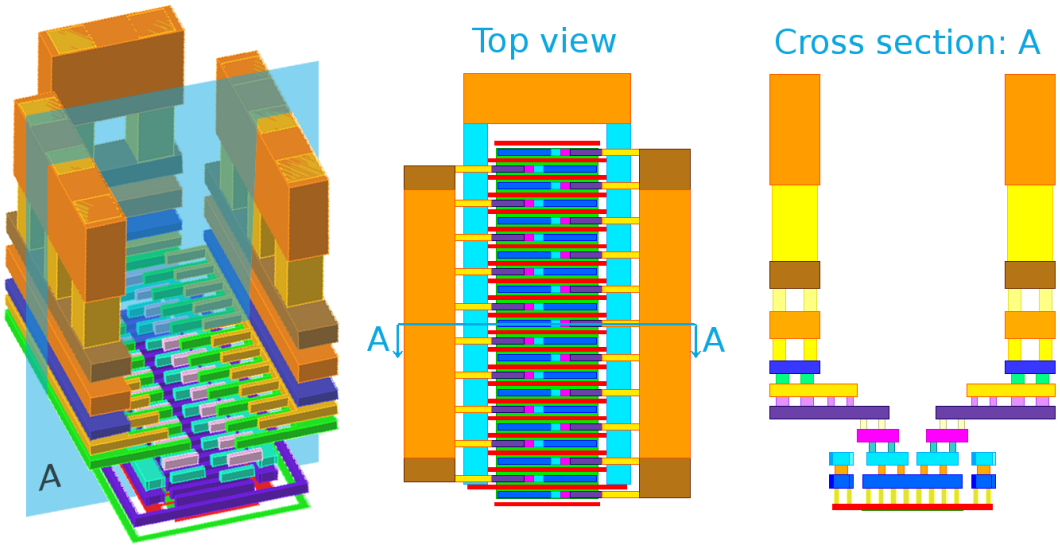
4.1 Standalone transistor

In order to well understand the transistor behavior at mm-wave and THz frequencies, a standalone transistor and some test structures have been embedded on the side of our first test-chip.

4.1.1 De-embedding

When measuring a structure on-wafer, the measurement reference plan is usually defined at the tip of the probes. Therefore, it is necessary to evaluate and remove the BEOL contribution. Thus, only the device under test (DUT) contribution is kept. To do this, one must perform a step called de-embedding. This is equivalent to modifying by calculation the reference plane from the measuring probes up to the intrinsic component to be characterized.

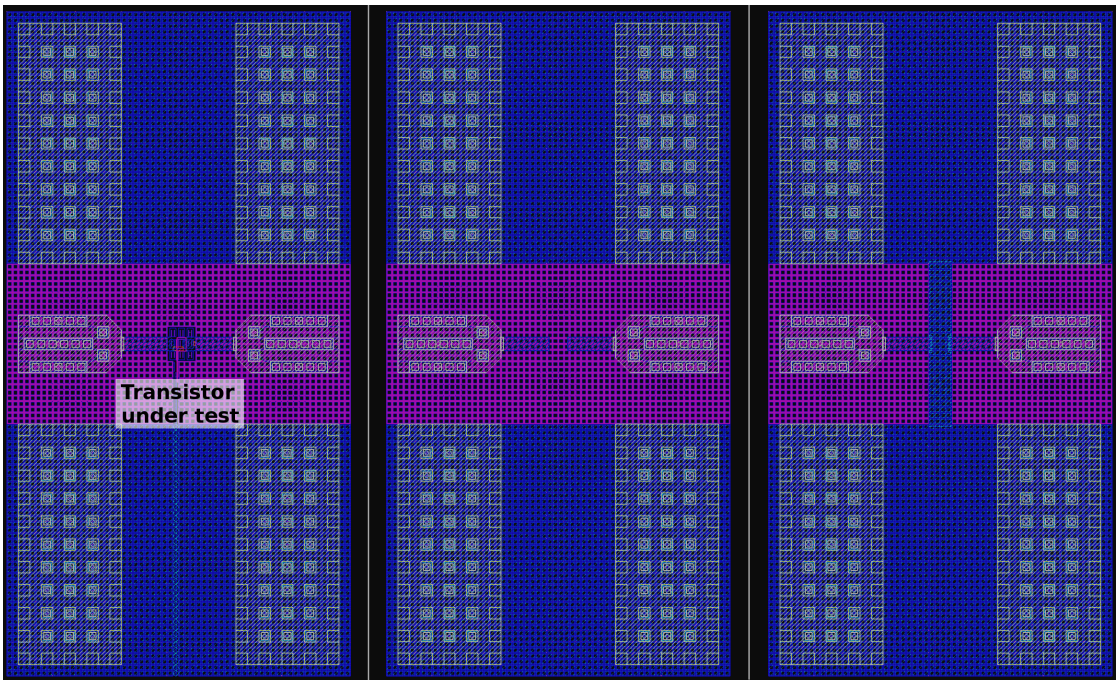
There are several methods to perform de-embedding [91] depending on the complexity of the BEOL access. In our case, we will consider that the device under measurement is a transistor with its BEOL accesses up to metal IA, as depicted in Figure 4.1. Thus, the de-embedding step aim is to remove pads and IB access lines contribution. This simple de-embedding can be performed with a classic Open/Short de-embedding method.



(a) (b) (c)

Figure 4.1 – Standalone transistor under test (a) 3D view, (b) top view and (c) cross section on the plane A.

The classic Open/Short de-embedding method used here is based only on two steps named "Pad-Open" and "Pad-Short". Indeed, as our IB access lines are very small they are supposed to be localized elements. To perform these steps, two structures have been added on the wafer, as presented in Figure 4.2.



(a) (b) (c)

Figure 4.2 – On-wafer test structures: (a) standalone transistor, (b) open and (c) short.

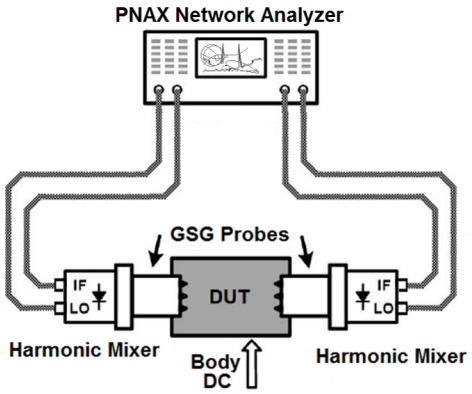
Thus, after having calibrated the measuring apparatus in order to place the reference plane at the ends of the probes, the S parameters of the two structures (Pad-Open and Pad-Short) and of the DUT are measured.

Then, these S parameters are converted into Y parameters. The Y parameters of the Pad-Open structure are then subtracted from the Y parameters of the Pad-Short and the DUT. This step removes the pads' capacity.

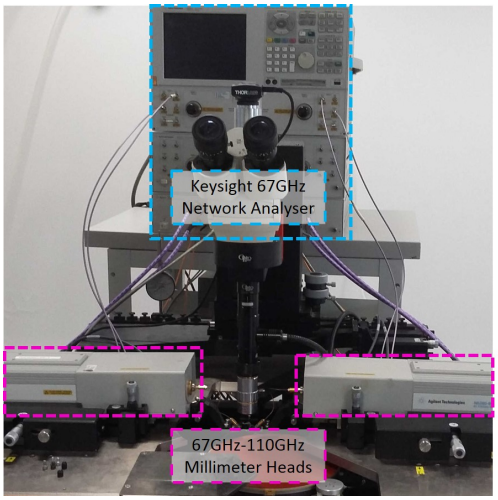
The remaining Y parameters are then converted to Z parameters and the Z parameters of the Pad-short structure are subtracted from the Z parameters of the DUT. This removes the inductive contribution of the pads as well as the inductance of the access line.

The conversion of the DUT Z parameters into S parameters finally makes possible to obtain the S parameters of the intrinsic DUT.

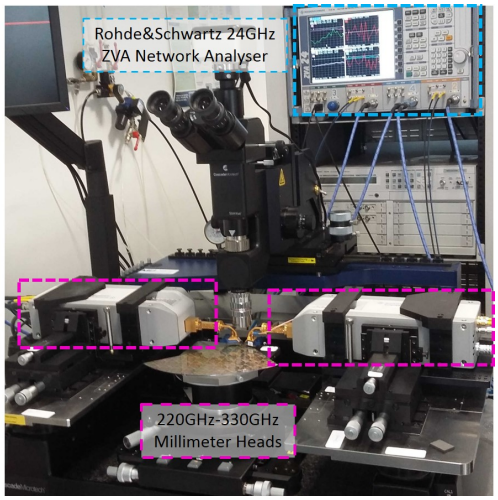
4.1.2 Measurement setup



(a)



(b)



(c)

Figure 4.3 – (a) Measurement setups schematic, (b) first bench from DC to 110 GHz picture and (c) second bench from 220 to 330 GHz picture.

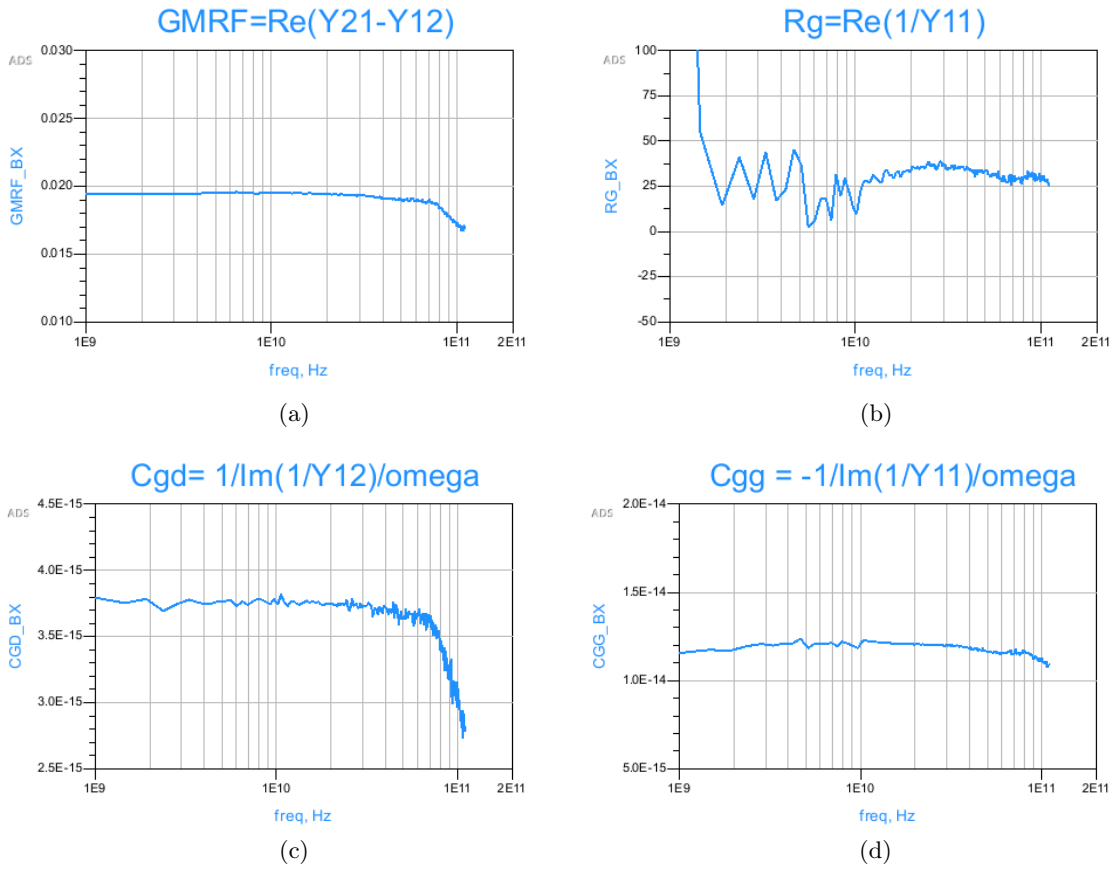
The on-wafer measurement setup is depicted in Figures 4.3. For these measurements two benches were used to cover two frequency bands:

- The first one performing measurements from DC to 110GHz. It consists of: a Keysight 67GHz network analyzer followed by two 67-110GHz millimeter test "heads" (i.e. two harmonic mixers) and two 100µm Picoprobe GSG probes.
- The second one covering the range from 220GHz to 330GHz. It consists of: a Rohde&Schwartz 24GHz ZVA network analyzer followed by two 220-330GHz millimeter test "heads" and two 50µm Picoprobe GSG probes.

The body bias is provided through a DC-pad not visible in Figure4.2.

4.1.3 Measurement results

First of all, in the following figures, some analog transistor parameters measurements up to 110GHz will be presented. The Figures 4.4(a-b) present the RF transimpedance ($G_{m|RF}$) and the gate resistance (R_g) while the parasitic capacitances C_{gd} and C_{gg} are presented in figure 4.4(c-d).



(a) (b) (c) (d)

Figure 4.4 – Standalone transistor measurement up to 110GHz: (a) RF transimpedance, (b) gate parasitic resistance, (c) gate to drain parasitic capacitance and (d) gate to substrate parasitic capacitance.

The cutoff frequency (f_T) is, by definition, the unity current gain frequency. To measure it, one can plot the H21 of the DUT and spot the zero crossing. Nevertheless, most of the time the measurement apparatus does not reach this frequency and H21 must be extrapolated. H21 is decreasing with a slope of 20dB/dec so it is possible to extrapolate

it by taking the asymptote of H21 and extending it to zero.

In the same way, the maximum oscillation frequency f_{max}, which is the frequency at which the maximum power gain is equal to 1, is measurable by taking the crossing of Mason's gain function U with zero. The only difference is that U is decreasing with 40dB/dec.

The figures 4.5 show in blue lines the H21, U, f_T and f_{max} measured on the standalone transistor with the first bench, up to 110GHz.

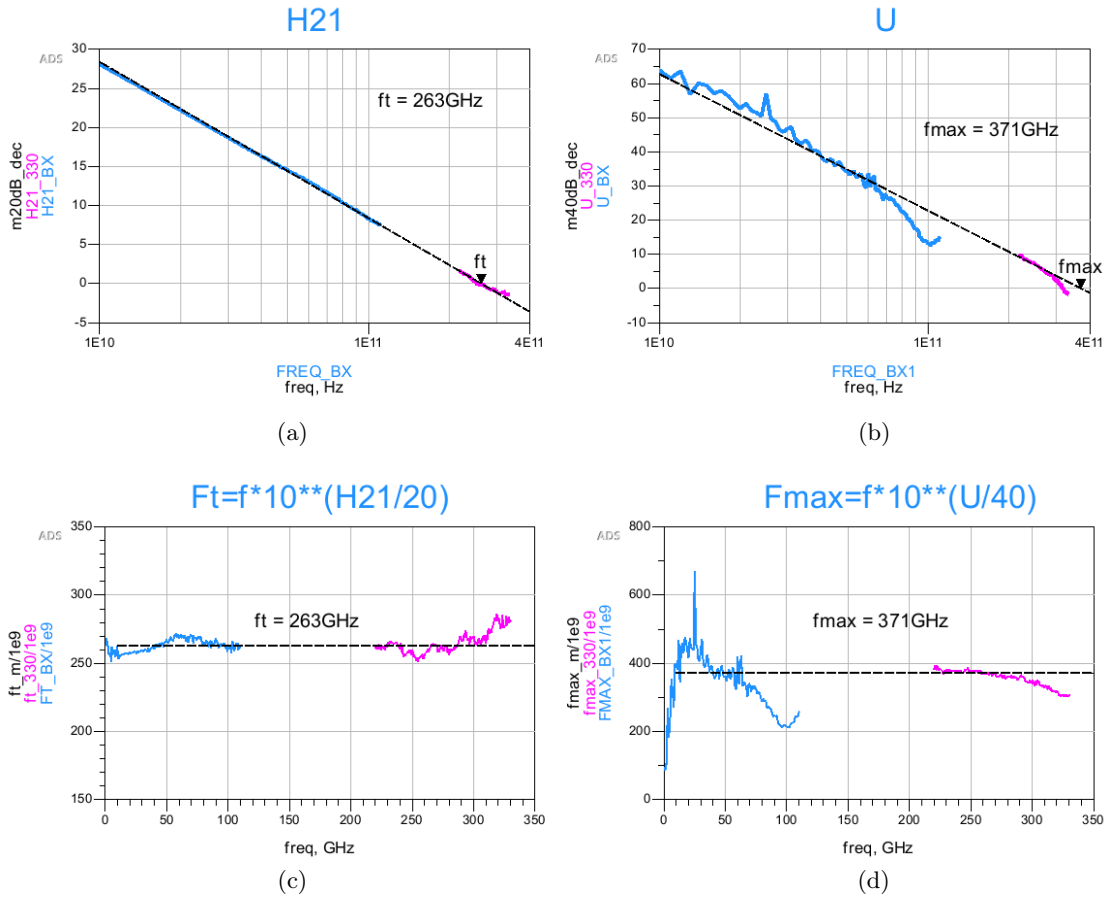


Figure 4.5 – Standalone transistor measurement up to 110GHz in blue lines and from 220GHz to 330GHz in pink lines: (a) Current gain H21, (b) Mason's gain U, (c) cutoff frequency f_T and (d) maximum oscillation frequency f_{max}.

Thanks to our second bench, from 220GHz to 330GHz, it becomes possible to plot H21 and U until the zero crossing. The figures 4.5 show in pink lines the H21, U, f_T and f_{max} measured on the standalone transistor with the second bench, from 220GHz to 330GHz.

It is remarkable that for both f_T and f_{max} the continuity between the two frequency bands seems to be respected. Thus, for our transistor featuring a gate length of 30nm and 20 fingers of 800nm width and including an optimized BEOL, measurements gives 263GHz of f_T and 371GHz of f_{max}.

The figure 4.6 and the table 4.1 present the comparison between simulations (*c.f.* chapter 3, section 3.3.1) and measurements for f_T and f_{max}. It can be seen that we obtain an excellent correlation. This confirms the very accurate models of the design kit P-Cell.

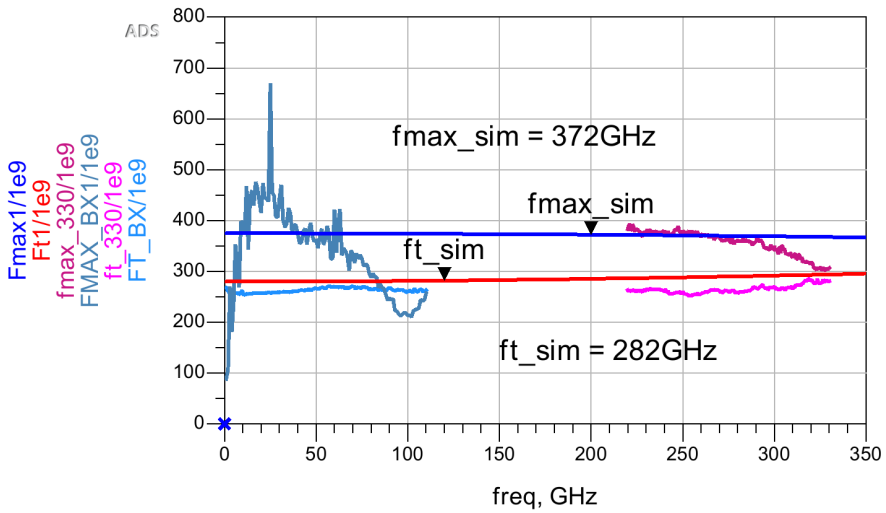


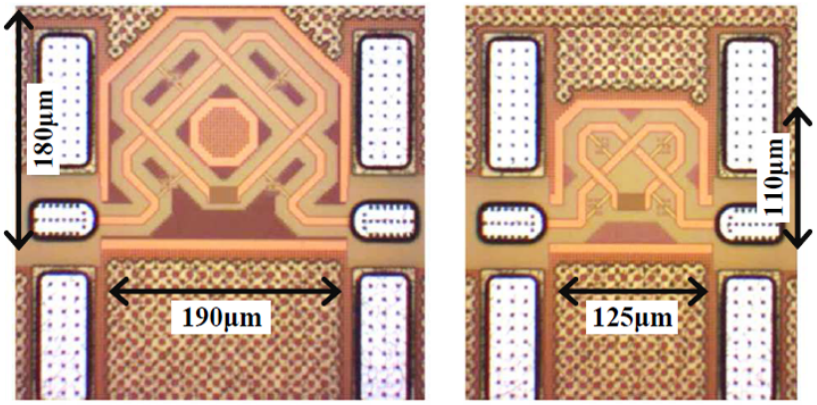
Figure 4.6 – Standalone transistor measurement versus simulation results for cutoff frequency f_T and maximum oscillation frequency f_{max}.

	Simulation with DK P-Cell	Simulation with P-Cell + BEOL	Measurement
f_T	360 GHz	280 GHz	260 GHz
f_{max}	390 GHz	370 GHz	370 GHz

Table 4.1 – f_T and f_{max} simulations with and without BEOL parasitic interconnections versus measurement.

4.2 Distributed oscillators

The microphotographs of the two distributed oscillators manufactured in 28nm FD-SOI CMOS technology from ST Microelectronics are presented in Figure 4.7. The core areas are respectively 0.034mm^2 and 0.014mm^2 without pads for the 134GHz and the 202GHz topologies.



(a) (b)

Figure 4.7 – Microphotograph of the (a) first (134GHz) and (b) second (202GHz) distributed oscillator. (same metric scale).

4.2.1 Measurement setup

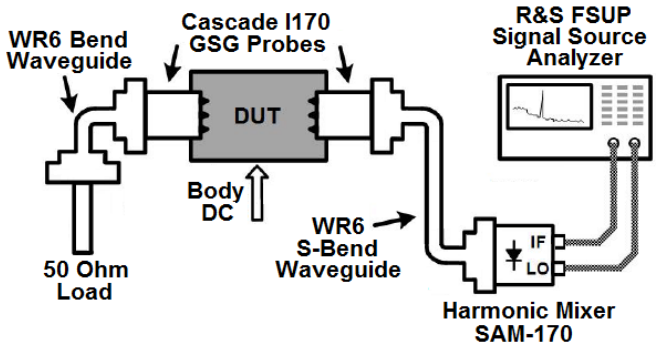


Figure 4.8 – Measurement setup.

The on-wafer measurement setup is depicted in Figure 4.8. It consists of: a 100µm Cascade I170 GSG probe followed by an S-bend waveguide, a SAM-A70 harmonic mixer and a Rohde & Schwarz signal source analyzer on the drain pad. Another Cascade GSG probe is followed by a bend waveguide and a 50Ω load, connected to the gate pad. The

DC gate and drain voltages are directly provided through the bias-tees included in the probes. The body bias is provided through a DC-pad not visible in Figure4.7.

4.2.2 Measurement results

The first distributed oscillator was measured at a frequency of 134.3GHz with a power consumption of 20mW (Vdrain=1V), as shown in Figure 4.9. The measured phase-noise is depicts in Figure 4.10 with -99.6dBc/Hz at 1MHz offset from the carrier.

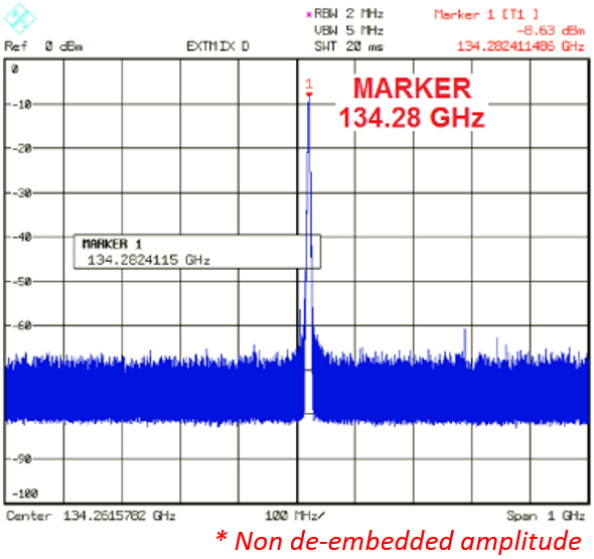


Figure 4.9 – Measured output spectrum of the first (134GHz) distributed oscillator.

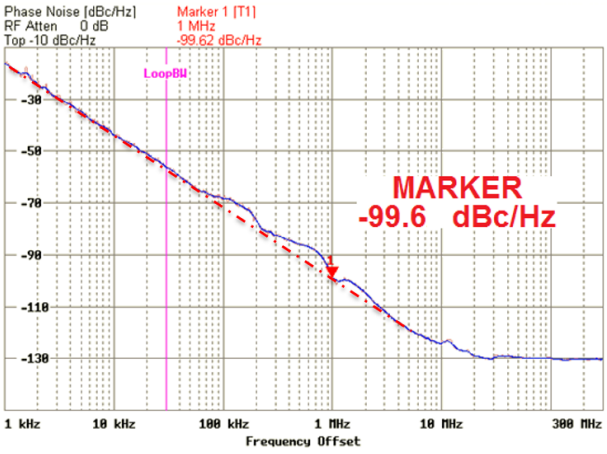
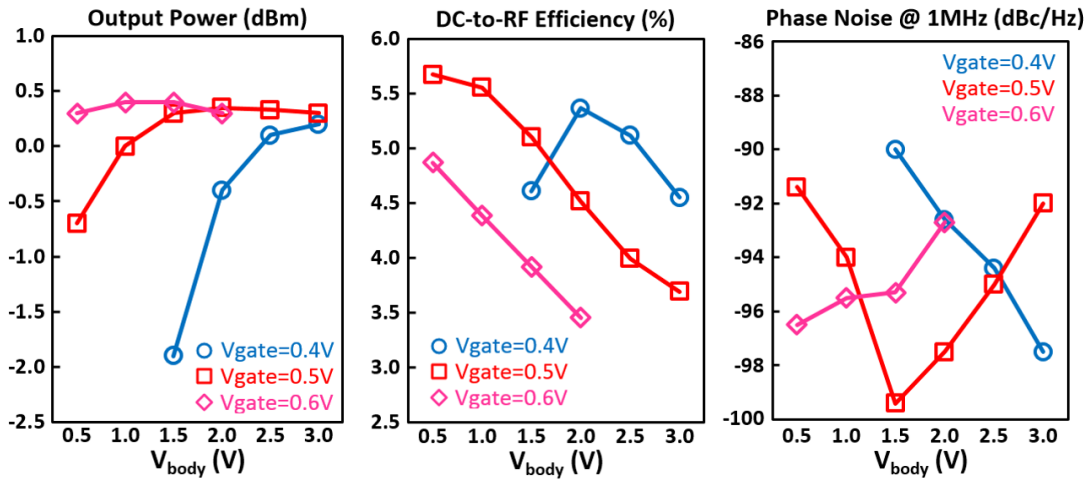


Figure 4.10 – Measured phase noise of the first (134GHz) distributed oscillator.

The de-embedded output power is 0.4dBm (1.1mW) corresponding to a remarkable DC-to-RF efficiency of 5.48%. The measured output power, DC-to-RF efficiency and phase noise at 1MHz offset are shown in Figure 4.11 for different gate (Vgate) and body (Vbody) voltages.



(a) (b) (c)

Figure 4.11 – Measured (a) output power, (b) DC-to-RF efficiency and (c) phase noise at 1MHz offset for different Vbody and Vgate, for the first (134GHz) oscillator.

As expected, increasing bias condition increase the output power until a compression. After this compression, increasing bias voltages result logically on a reduction of DC-to-RF efficiency. This behavior is easily understandable since the DO can be seen as a looped back distributed power amplifier. Indeed, increasing Vbody is equivalent to boost the transistors' gain (since the trans-conductance g_m is inversely proportional to V_T). Nevertheless, as for power amplifier, when operating in large-signal the gain compresses and thus the efficiency decreases.

Moreover, as predicted by the theory the phase noise changes positively with the body bias voltage change until the output power compression. A remarkable result here is that thanks to the FD-SOI unique wide range of body bias control, a large range of phase noise values can be covered and hence a minimum phase noise operating point can be found.

Finally, the oscillation frequency variation over bias voltages' variation is only 60MHz. This represents a very small frequency variation of 0.045% thanks to its low sensitivity to active component parameters.

As shown in Figure 4.12, the second distributed oscillator was measured at a frequency of 202.2GHz with a power consumption of 20mW. The optimum phase noise at 1MHz offset is -100.4dBc/Hz, as presented in Figure 4.13.

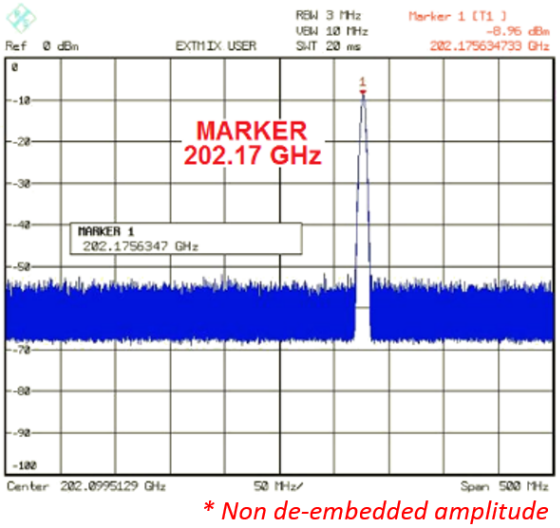


Figure 4.12 – Measured output spectrum of the second (202GHz) distributed oscillator.

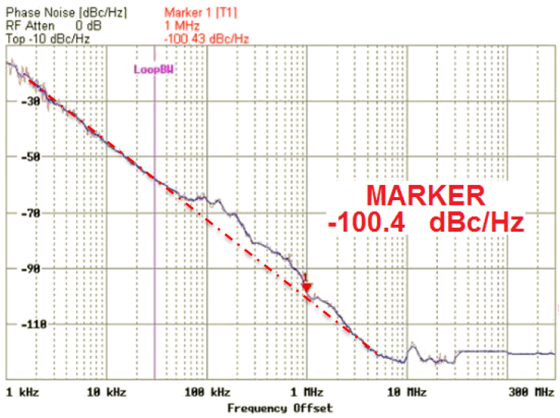
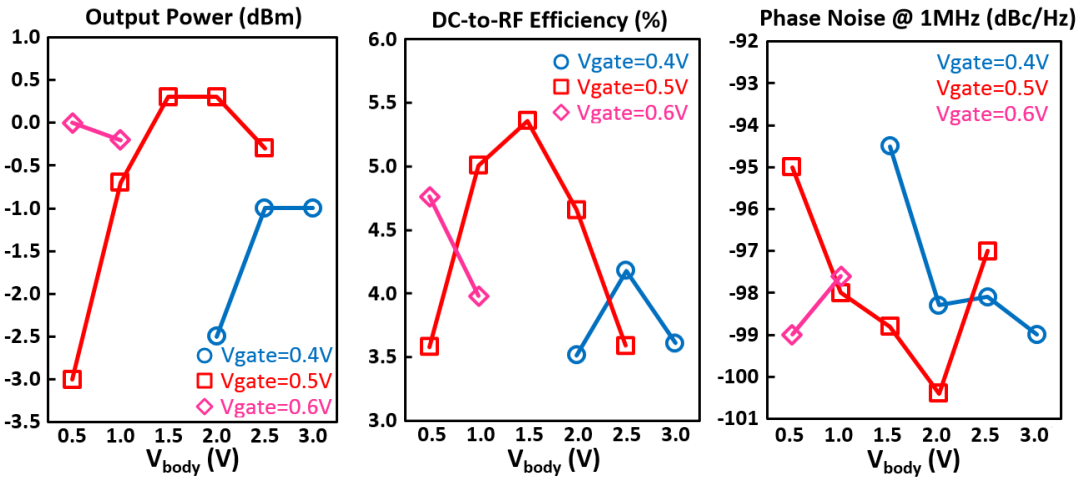


Figure 4.13 – Measured phase noise of the second (202GHz) distributed oscillator.

The oscillation output power is measured at 0.3dBm (1.07mW) corresponding to a DC-to-RF efficiency of 5.38%. The measured output power, DC-to-RF efficiency and phase noise at 1MHz offset are presented in Figure 4.14 for different gate (Vgate) and body (Vbody) voltages.

Similarly to precedent results, a phase noise optimum point can be reached by tunning the body bias voltage. The oscillation frequency variation over bias change is 50MHz, representing a variation of only 0.025%.

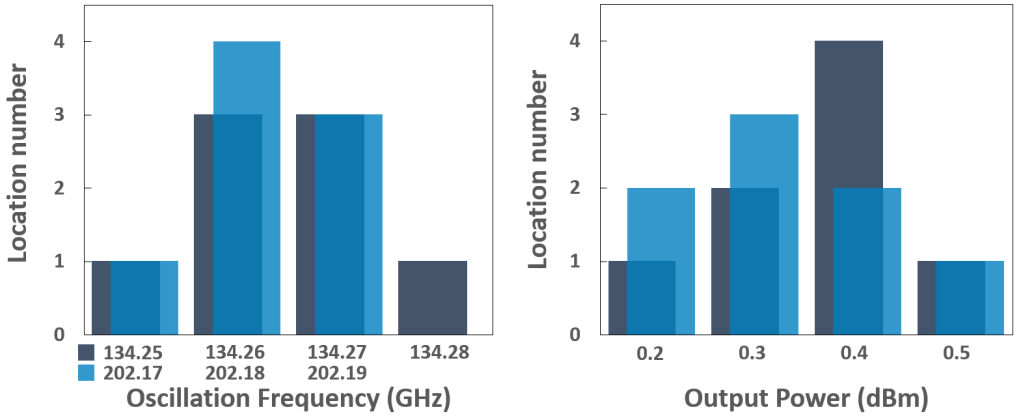


(a) (b) (c)

Figure 4.14 – Measured (a) output power, (b) DC-to-RF efficiency and (c) phase noise at 1MHz offset for different Vbody and Vgate, for the second (202GHz) oscillator.

4.2.3 On-wafer mapping measurement for variability study

For each circuit implementation, several circuits at different locations (#8) on the same wafer have been measured in order to provide information on the potential variability.



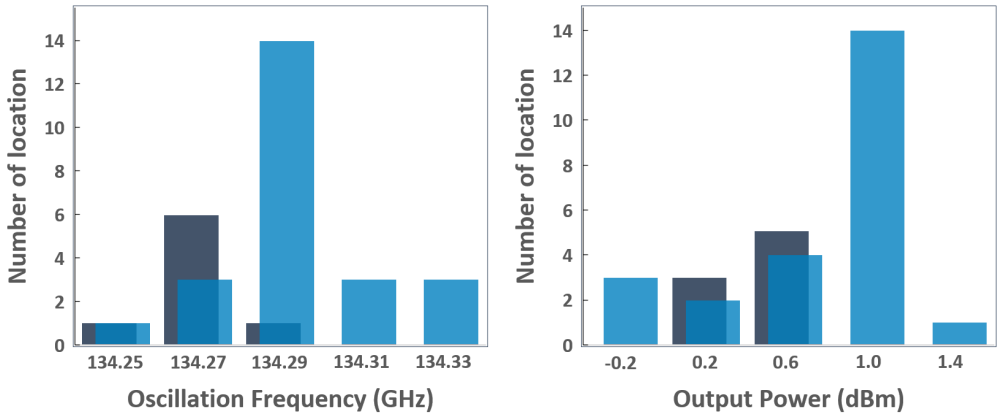
(a) (b)

Figure 4.15 – Distribution histograms for the (a) oscillation frequency and (b) output power as a function of on-wafer location. (8 different locations measured on a same wafer for each topology. Dark bar for the first (134GHz) and blue bar for the second (202GHz) oscillator).

Using the same Vgate and Vbody biasing operation point, the oscillation frequency shows variations of only around 0.01%. Similarly, the output power level shows a standard deviation of less than 0.1dBm. This demonstrates the low variability feature of such DO architectures, as shown in Figure 4.15.

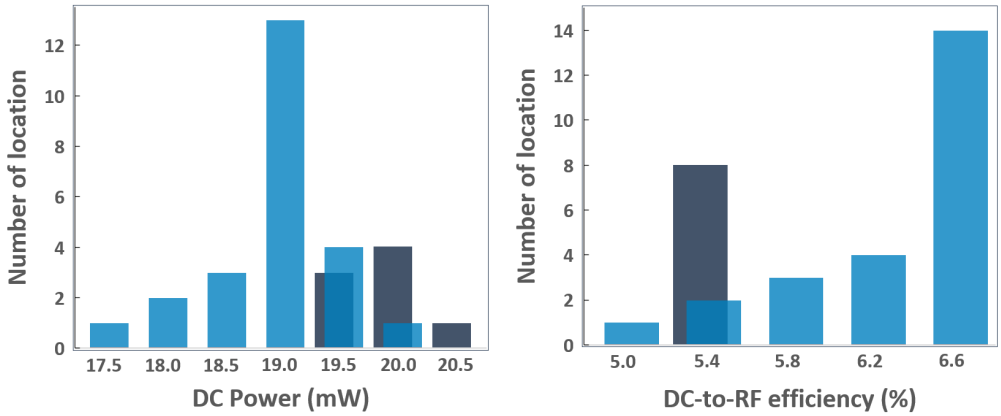
In order to have a better representative sample, for the first (134GHz) oscillator, a second wafer from another tape-out has been tested and 24 other locations have been measured. Slight layout modifications have been made to reduce losses in TL and in transistor accesses, and hence increase DC-to-RF efficiency. These modifications include metal dummies removal (one row of dummies was removed thanks to ground plan density optimization) and transistors' source access reduction (source access was reduced to dive more quickly to the ground plane).

Using the same Vgate and Vbody biasing operation point, the oscillation frequency shows a standard deviation of around 0.015%. The output power level shows a standard deviation of 0.4dBm. Distribution histograms for the oscillation frequency and output power are presented in Figure 4.16 (in blue bar). Standard deviations are calculated only from the 24 new locations. Nevertheless, the 8 previous locations are also presented (in dark bar) in order to compare results. These results confirm the low variability feature of such DO architectures. Moreover, the very low variation of the center frequency confirms that the DO oscillation frequency is mainly defined by the TL total length and does not depend on active components variations.



(a) (b)

Figure 4.16 – Distribution histograms for the (a) oscillation frequency and (b) output power as a function of on-wafer location. 32 different locations on two different wafers. (Dark bar for the first wafer and blue bar for the second wafer).



(a) (b)

Figure 4.17 – Distribution histograms for the (a) DC power consumption and (b) DC-to-RF efficiency as a function of on-wafer location. (32 different locations on two different wafers. (Dark bar for the first wafer and blue bar for the second wafer).

Distribution histograms for the DC power consumption and DC-to-RF efficiency are depicted in Figure 4.17 (Dark bar for the first wafer and blue bar for the second wafer). As predicted, the reduction of parasitic losses allows to rushed better output power with lower power consumption on the second wafer. Thus, the DC-to-RF efficiency is logically improved as shown in figure 4.17b. Power consumption presents a standard deviation of 0.57mW and DC-to-RF efficiency exhibits a standard deviation of only less than 0.5%.

All these low process variability results enabled the use of such Distributed Oscillators as unlocked frequency reference for a certain category of sub-THz applications.

4.2.4 Phase noise optimization through body-bias control

For the phase noise, the measured variation for a constant Vbody and Vgate is around 6% for a standard deviation of approximately 1.4dBc/Hz, as shown in the distribution histogram Figure 4.18.

Nevertheless, phase noise is inversely proportional to output voltage level [92] and in our topology output voltage is proportional to overdrive voltage and hence to the threshold voltage. Thus, the FD-SOI large V_T variation range allows a wide range of phase noise tuning and hence permits to find a minimum phase noise operating point.

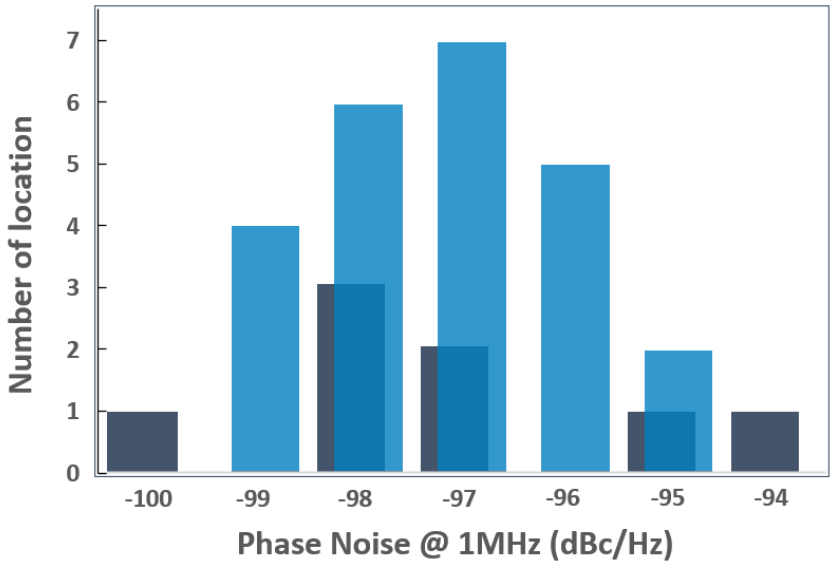


Figure 4.18 – Distribution histograms for the phase noise at 1MHz offset as a function of on-wafer location. (32 different locations on two different wafers. (Dark bar for the first wafer and blue bar for the second wafer).

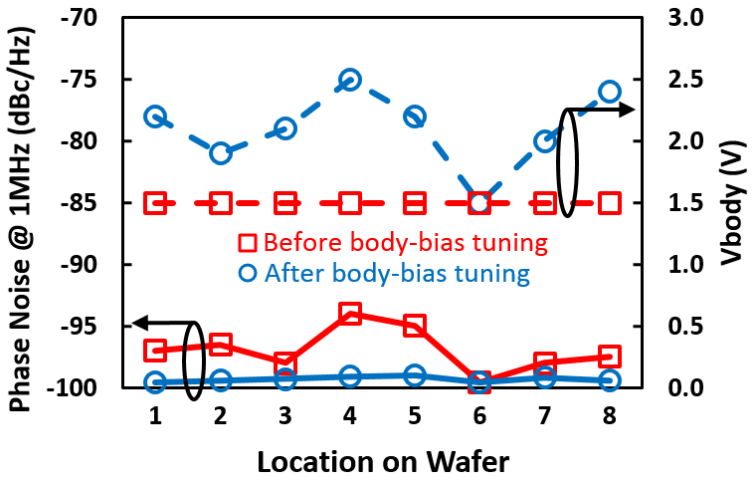


Figure 4.19 – Phase Noise optimization by body-biasing; measurement over 8 locations on wafer, for the first (134GHz) oscillator.

This feature is depicted in Figure 4.19, where the phase noise at 1MHz offset of the 8 locations on the first wafer was measured for a constant Vbody in square symbol lines. The circle symbol lines present the phase noise after optimization through body biasing.

Finally, the phase-noise of all location can be reduced between -99dBc/Hz and -100dBc/Hz.

This phase noise optimization is made at the expense of a power consumption variation between 20mW and 25mW and thus DC-to-RF efficiency reduction down to around 4%.

Moreover, for some applications which require low power consumption but less optimized phase noise, the body biasing can be used to reduce the consumption (as the transistors are biased at constant Vgate condition, body bias changes involved V_T changes and hence bias and g_m variation) at the expense of less performant phase noise.

4.2.5 State-of-the-art comparison

Measurement results are summarized and compared to state-of-art in Table 4.2 using the classic oscillator FoM:

$$FoM = PN(\Delta f) - 20\log\left(\frac{f_0}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1mW}\right). \tag{4.1}$$

Ref.	Freq. (GHz)	P_{out} (dBm)	DC-to-RF Efficiency	$PN_{@1MHz}$ (dBc/Hz)	P_{DC} (mW)	|FoM|	Techno.
[26]	121	-3.5	2.07 %	-88	21.6	176.3	130nm CMOS
[29]	195	6.5	15.2 %	-98.6	29.2*	189.7*	55nm SiGe
[20]	210	1.4	2.44 %	-87.5	56.5*	176.4*	130nm SiGe
[17]	212	-7.1	0.65 %	-92	30	183.8*	130nm SiGe
[14]	219	-3	2.09 %	-77.4	24	170.4	65nm CMOS
This Work	134	0.4	5.48 %	-99.6	20	188.9	28nm FDSOI CMOS
This Work	202	0.3	5.38 %	-100.4	20	193.5	28nm FDSOI CMOS

* Calculated from provided data. / Work published in [79].

Table 4.2 – Comparison with Previous State-of-the-Art.

To our knowledge, this work presents for the very first time oscillators at mm-wave and THz frequencies integrated in a 28nm CMOS technology. The advantages coming from the high f_T/f_{max} performances for the active devices are, for these processes, counter-

balanced by the limited back-end performance in such very dense nodes. This work compares positively with the state of the art, showing good DC-to-RF efficiency for a very compact solution, despite the potential VLSI integration style 10ML BEOL. Performant phase noise values have been measured taking advantage of the body-bias enabled phase noise optimization. And, the numerous locations measurements on wafer demonstrate the robustness of such integrated DO solution.

Another remarkable result appears when comparing these values with respect to post-layout simulated values and with theoretical value coming-out from the DO theory developed in Chapter 2 (section 2.3.2). Indeed, as depicted in figure 4.20, an excellent correspondence is obtained demonstrating the accuracy of the proposed mm-wave design flow and confirming the good precision of the DO theory. Indeed, all the presented numbers (simulation, theory, statistical measurement) are within less than 0.1% precision.

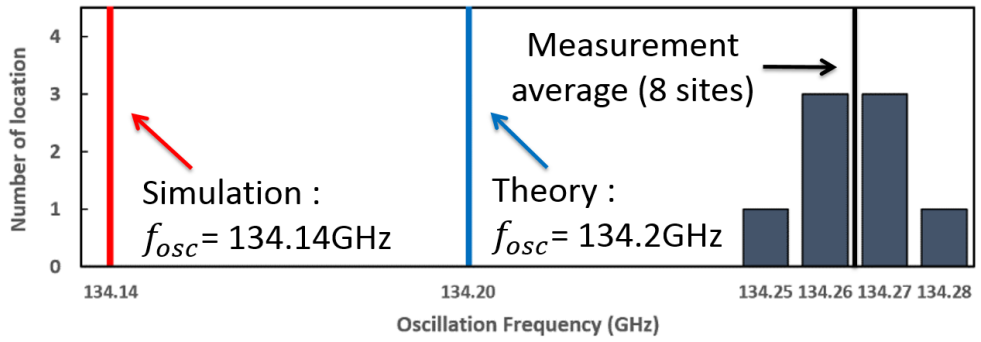


Figure 4.20 – Oscillation frequency comparison between measurements over the 8 locations of the first wafer, post-layout simulation and theoretical value. (precision less than 0.1%)

4.3 Injection locked distributed oscillator

In order to demonstrate injection locked capability of such of oscillator, experimental injection trials have been performed on the 200GHz distributed oscillator. The microphotograph of the structure made in 28nm FD-SOI CMOS technology is presented in Figure 4.21. The core area of this oscillator is 0.065mm^2 and 0.014mm^2 with and without pads respectively.

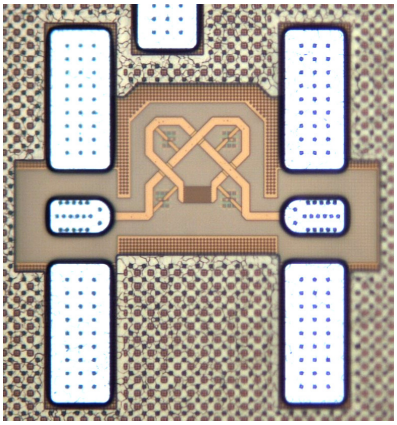


Figure 4.21 – Microphotograph of the tested distributed oscillator.

4.3.1 Measurement setup

The injection locking capability was demonstrated experimentally on this CMOS integrated oscillator by carefully locking on an externally injected signal. The test fixture is given in Fig. 4.22(a).

It consists of: a 100µm GSG probe followed by an S-bend waveguide, a harmonic mixer and a signal source analyzer on the drain pad. Another GSG probe followed by an S-bend waveguide, a ×24 mixer and an RF source is connected to the gate pad. The DC gate and drain voltages are directly provided through the bias-tees included in the probes. The equivalent schematic under injection is depicted in Fig. 4.22(b).

4.3.2 200 GHz ILDO measurement results

The free-running oscillator was first measured at a frequency of 197.1GHz with a power consumption of 21mW (Vdrain=1V) as shown in Fig. 4.23(a). The free-running phase-noise was measured at -100dBc/Hz at 1MHz offset from the carrier. The de-embedded output power is 2dBm (1.6mW) corresponding to a DC-to-RF efficiency of 7.62%.

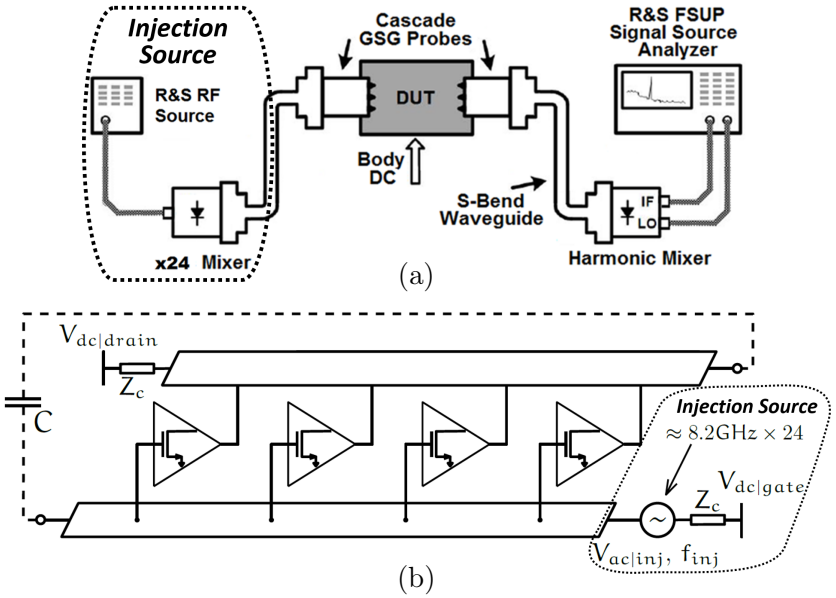


Figure 4.22 – (a) Measurement setup and (b) equivalent schematic under injection.

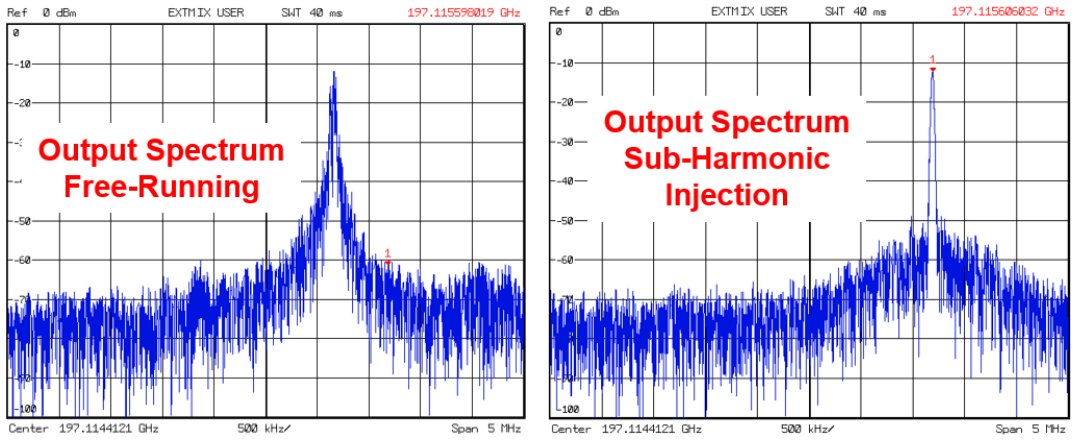


Figure 4.23 – Output spectrum of (a) free-running DO and (b) locked SHILDO.

The external RF source generates a signal around 8.213GHz up-converted through an external ×24 mixer. The THz oscillator output spectrum under injection is presented in Fig. 4.23(b).

The locked phase-noise was measured at -106dBc/Hz at 1MHz offset. Fig. 4.24 presents respectively the phase-noise curves for the free-running oscillator, the low-frequency reference, and the injection locked oscillator. As predicted by the ILO theory, the phase-noise of the locked oscillator follows the phase-noise of the reference within the

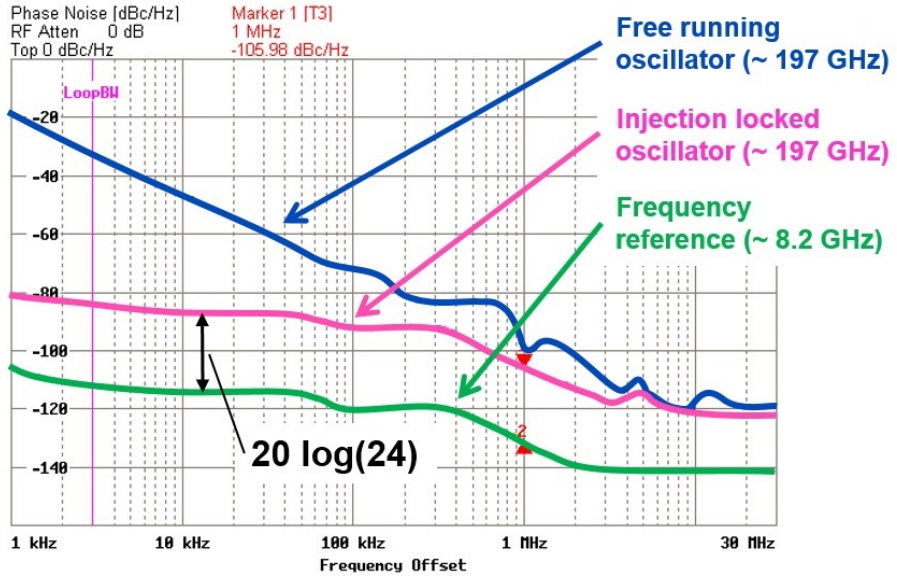


Figure 4.24 – Measured phase-noise of the free-running oscillator, the low frequency reference and the injection locked oscillator.

multiplication factor ($+20\log(24)$).

The $\times 24$ instrumentation mixer used here only allows a constant output power of -47dBm at 197GHz. At this injected power level, the theoretical LR coming from Chapter 2 theory should be 216MHz. Nevertheless, the measured LR is only 9.2MHz. This difference can be explained by the injection technique used in this measure.

Indeed, the main assumption of the presented theory is that the effect of the injection is considering distributed (with distributed impedance variation r_u, x_u across the TL, see Figure 2.21), and in the implemented circuit all the phase shift induced by the injection source is concentrated at the input port. A possible modification to apply presented theory is to inject signal through a line coupled to the DO transmission line.

Nevertheless, it is possible in our case to apply Adler theory to deduce an equivalent Q-factor of the ILDO and extrapolate the locking range for higher injected amplitude.

To tune the injected signal amplitude, a variable attenuator is added at the mixer output. By using this attenuator, the injected power is tunable between -47dBm and -70dBm. Fig. 4.25(a) depicts the measured LR as a function of injected signal amplitude (crosses) versus the theoretical prediction using Adler theory. By extrapolation, the LR of the ILDO for larger amplitude is presented in Fig. 4.25(b).

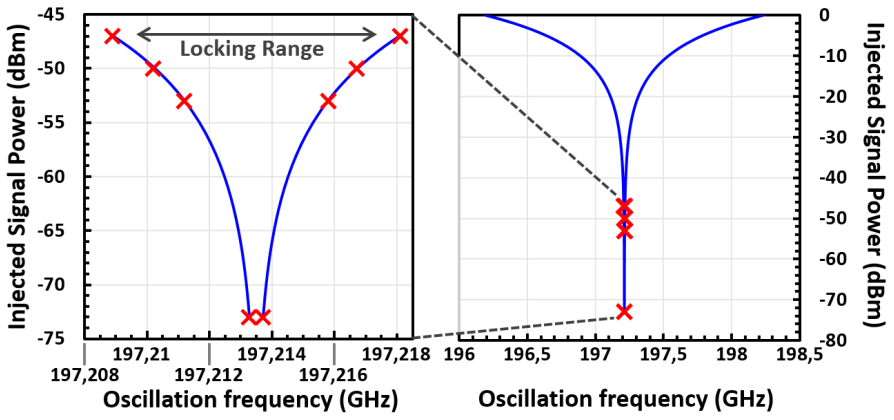


Figure 4.25 – ILDO locking range (a) measurement (crosses) versus Adler theory (solid line) and (b) extrapolation as a function of injected amplitude.

4.3.3 State-of-the-art comparison

Measurement results are summarized and compared to the state-of-art in Table 4.3.

Ref.	Locked by ?	Freq. (GHz)	P_{out} (dBm)	DC-to-RF Efficiency	$PN_{@1MHz}$ (dBc/Hz)	P_{DC} (mW)	Techno.
This Work	ILO	197	2	7.62 %	-106†	21	28nm FDSOI CMOS
[32]	ILO	195	0.0	3.47 %	-117.5*†	28.8	130nm SiGe
[31]	ILO	285	-9	0.24 %	-105†	52	55nm SiGe
[33]	PLL	290	-14	0.01 %	-82.5	376	90nm SiGe
[34]	PLL	317	5.2	0.54 %	-79	610	130nm SiGe

* Estimated from provided data, † Depends on reference phase noise.

Table 4.3 – Comparison with Previous State-of-the-Art.

This work compares positively with the state of the art, pointing out the potential advantages of such a solution for mm-wave/THz signal generation with improved energy efficiency and a very performant phase noise behavior.

Nevertheless, the locking range is too narrow for classic applications and still needs to be improved. A possible way to do it is to explore injection technique possibilities with for example coupled transmission lines.

4.4 Chapter conclusion

This chapter has presented the experimental results of this thesis.

First, a study has been performed on a standalone transistor highlighting the excellent performances of the 28nm FD-SOI transistors at mm-wave and THz operation frequency.

Then, the two distributed oscillators presented in the previous chapter have been tested. These two oscillators compare positively with the state of the art with excellent DC-to-RF efficiency, good output power level, and remarkable phase noise performances.

A variability study has been presented highlighting the very low process variability of such of architecture thanks to the low contribution of active components on the oscillation frequency. And phase noise shaping feature was for the first time demonstrated taking advantage of the FD-SOI body-bias.

Finally, injection locked capability of such of oscillator has been demonstrated. The injection-locked distributed oscillator exhibit very performant output power and DC-to-RF efficiency as well as excellent phase noise behavior. Nevertheless, locking range still needs to be improved and thus future works are needed to take full advantage of this kind of architecture.

Conclusion and perspectives

Conclusion

In this thesis, silicon-based mm-wave and THz source challenges induced by limited f_T/f_{max} and dense BEOL of VLSI technologies have been identified and addressed. The promising applications of such mm-wave and THz systems have made the signal generation in this frequency range a new trend, especially in cost-optimized processes such as CMOS FD-SOI. The most challenging specifications in these frequency bands are the energy efficiency, the output power level and, for some applications, the phase-noise performances.

While these specifications and challenges have been highlighted in Chapter 1, the second chapter has introduced an alternative for mm-wave and THz frequency generation in CMOS technology: the injection locked distributed oscillator (ILDO). Thanks to its ability to provide efficient and high-level output signal close to transistors' f_{max}, the distributed oscillator appears as an excellent candidate for mm-wave and THz frequency generation in advanced CMOS technology. A theoretical study of distributed oscillator under injection has been proposed allowing to fully optimize the ILDO design taking into account its topology specifications. This study has shown that ILDO is one of the most relevant choices for mm-wave and THz frequency synthesis.

In the third chapter, a specific design methodology for silicon integration of mm-wave and THz distributed oscillator has been introduced. The 28nm FD-SOI CMOS technology for mm-wave applications has been presented and two mm-wave/THz distributed oscillators have been realized in this technology validating this mm-wave design flow.

The final chapter is dedicated to the experimental results of this thesis. Standalone transistor measurements have been presented demonstrating the excellent high-frequency performances of the 28nm FD-SOI technology NMOS transistors. Then, the two designed distributed oscillators have been measured exhibiting excellent performances in terms of output power, DC-to-RF efficiency, and phase-noise. The presented oscillators exhibit

the measured highest oscillation frequency for an integrated CMOS oscillator in a 28nm node, upon the state-of-the-art at the date this manuscript is proposed.

On-wafer probing measurements have been conducted highlighting the very low variability feature of such distributed oscillator architectures. Comparisons between measurements, simulations, and theory have demonstrated the remarkable accuracy of the used design flow. Moreover, a new phase-noise optimization feature has been proposed taking advantage of FD-SOI uniquely wide body-bias tuning range.

Finally, the injection locked capability of such distributed oscillators has been experimentally demonstrated paving the way for future high efficiency and high output power locked THz sources fully integrated in a VLSI CMOS technology.

The original contributions presented in this manuscript are the following:

- An innovative architecture proposal for silicon-based frequency generation at mm-wave and THz frequencies.
- The introduction of a new theoretical approach for distributed oscillators operating close to transistors' f_{max}.
- The generalization of the Huntoon-Weiss/Badets theory for injection locked harmonic oscillators and its extension to the study of injection locked distributed oscillators.
- The participation in the optimization of the STMicroelectronics mm-wave design flow.
- The proposal of a new design methodology for mm-wave distributed oscillator in VLSI CMOS technologies.
- The silicon physical implementation of two demonstrators of mm-wave distributed oscillators presenting the measured highest oscillation frequency in a 28nm CMOS node.
- The demonstration of the injection locked capability of such mm-wave distributed oscillators opening the way for future CMOS-integrated THz locked signal generation.

Perspectives

Through this thesis, it has been demonstrated that high output power and energy efficient sources are achievable in VLSI 28nm CMOS technology. Nevertheless, future work should

be tackled in order to take full advantage of the excellent high-frequency performances of the 28nm FD-SOI technology. Some research perspectives are here proposed:

Perspective 1: Boosted gain DO amplification stage

Recent publications have demonstrated that it is possible to boost the output signal level very close to f_{max} by considering the amplification stage as a looped back unstable power amplifier [20, 28, 29]. It is possible to apply this technique to distributed oscillators by optimizing the amplification stage design to reach its maximum achievable gain as it has been demonstrated firstly for power amplifiers in [93, 94]. To do this, a local feedback is employed to boost the amplification stage gain. Figure 4.26 presents a proposed implementation of this technique in a distributed oscillator. The curve presented in this figure is an example of the gain-boost achieved with this technique in [93].

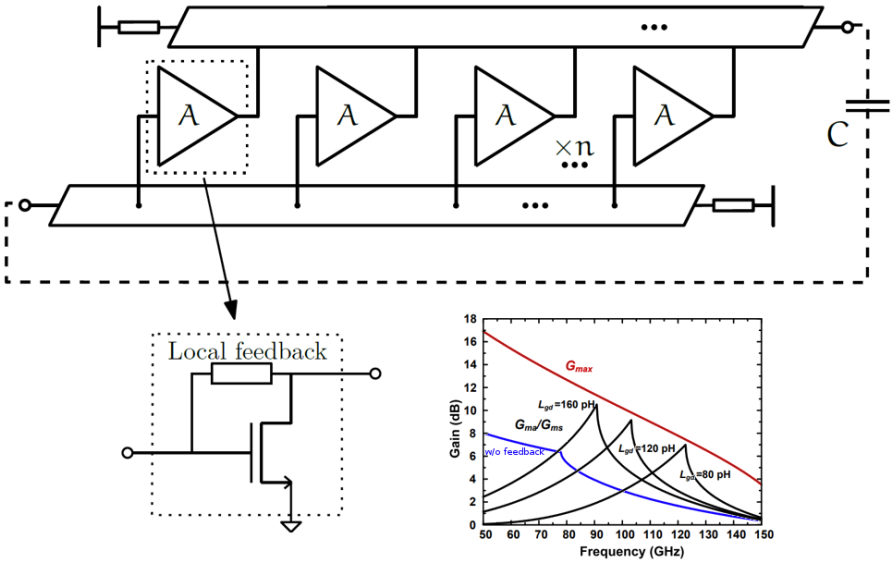


Figure 4.26 – Proposed architecture of a DO with boosted gain amplification stages and example of gain boost achieved with this technique in [93].

The main challenges for this kind of architecture coming from the boosted-gain frequency band and the layout. Indeed, it is essential to guarantee that the boosted gain center frequency coincides with the DO frequency bands to permit oscillations. Moreover, the local feedback must be as small as possible to be implementable in the already compact distributed oscillator.

Perspective 2: ILDO injection techniques

In this thesis, injection locked capability of such distributed oscillators has been experimentally demonstrated. Nevertheless, the locking range is too small for classic applications and still needs to be improved.

It is hence needed to explore new injection techniques. As a matter of example, a possible way is to use a transmission line coupled all along the DO line, as depicted in figure 4.27. Indeed, with this technique the ILDO theory presented in Chapter 2 is applicable as the injection is distributed all along the line. Hence, following the developed theory, the locking range should be highly improved.

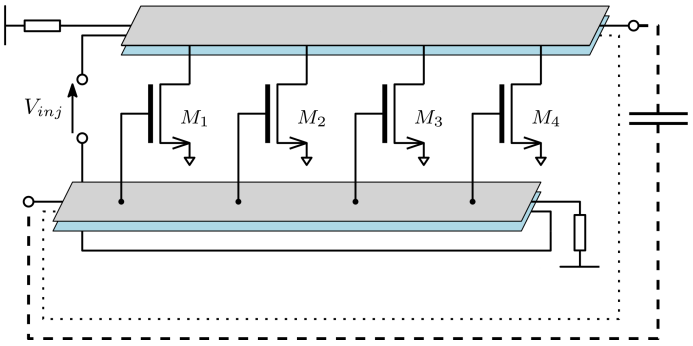


Figure 4.27 – Proposed injection technique using a TLine coupled all along the DO line.

The main challenges of this injection technique are the coupled-line induced losses and the layout. Indeed, the coupled-line must not impact significantly the DO transmission line attenuation constant to ensure that the oscillations are maintained. Regarding the layout, it is obvious that such coupled-line is a layout challenge since a DO is based on a looped TL which is very compact.

Perspective 3: Fully integrated THz locked signal generation

Assuming an improved ILDO locking range, it is possible to consider the design of a fully integrated THz locked signal generation in a VLSI CMOS technology. The proposed mm-wave architecture is presented in figure 4.28.

This proposed architecture is based on two cascaded ILOs. The last stage is an ILDO providing an efficient and high-level output signal. For the intermediate stage, a triple-push injection locked oscillator is a good choice. Indeed, the amplitude is not critical here and its structure guarantees an efficient third harmonic extraction and thus, allows an optimal frequency multiplication. This intermediate ILO is synchronized by a lower

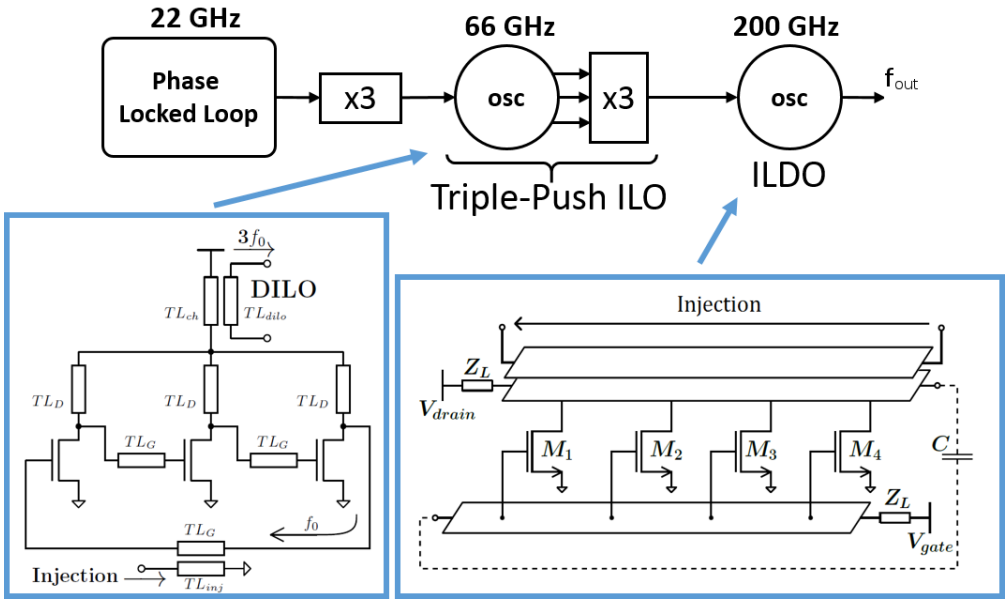


Figure 4.28 – Proposed architecture for fully integrated THz locked-source in a VLSI CMOS technology.

frequency PLL after a synchronization network which is aimed to extract the third harmonic of the PLL signal. The use of a lower frequency PLL permits an optimized power consumption with better phase-noise performances for the initial signal generation.

The main challenge to realize this THz locked-source is to ensure that the two ILO locking ranges are wide enough and well centered to guarantee that the system could be locked in a sufficient frequency range. Indeed, the full system relative locking range is intrinsically equal to the intersection of each ILO relative locking range[1]. Another challenge is the synchronization network between the PLL and the intermediate ILO. Indeed this bloc must extract efficiently the PLL output signal third harmonic. At this frequency, a triple-push structure is not implementable thus other solutions must be investigated. Finally, numerous layout aspects coming from on-chip coupling among the different oscillation structures will have to be carefully tackled.

[1]For a locking range LR around a central frequency f_0, the relative locking range is: $LR_{\%} = LR/f_0$

Bibliography

[1] P. H. Siegel, "Terahertz technology," *IEEE Trans. Microw. Theory Techn.*, vol. 50, no. 3, pp. 910–928, Mar. 2002.

[2] H. Sherry, "Terahertz circuits and systems in cmos," Theses, Université de Lille, 2013. [Online]. Available: http://www.theses.fr/2013LIL10049

[3] J. M. Guerra, "Design of sub-thz heterodyne receivers in 65 nm cmos process," Theses, Université de Lille, 2014. [Online]. Available: http://www.theses.fr/2014LIL10053

[4] U. R. Pfeiffer and E. Öjefors, "Terahertz imaging with CMOS/BiCMOS process technologies," in *2010 Proceedings of ESSCIRC*, Sep. 2010, pp. 52–60.

[5] F. Schuster *et al.*, "A broadband THz imager in a low-cost CMOS technology," in *2011 IEEE International Solid-State Circuits Conference*, Feb. 2011, pp. 42–43.

[6] Teraview. [Online]. Available: http://www.teraview.com/

[7] I. F. Akyildiz, J. M. Jornet, and C. Han, "Terahertz band: Next frontier for wireless communications," *Physical Communication*, vol. 12, pp. 16–32, Sep. 2014. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1874490714000238

[8] C. Wang *et al.*, "0.14thz high speed data communication over 1.5 kilometers," in *2012 37th International Conference on Infrared, Millimeter, and Terahertz Waves*, Sep. 2012, pp. 1–2.

[9] S. Koenig *et al.*, "Wireless sub-THz communication system with high data rate," *Nature Photonics*, vol. 7, no. 12, pp. 977–981, Dec. 2013. [Online]. Available: https://www.nature.com/articles/nphoton.2013.275

[10] M. Shur, "Silicon and Silicon Germanium Terahertz Electronics," in *2018 IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*, Jul. 2018, pp. 1–3.

[11] Y. Chen *et al.*, "22.2 A 25gb/s hybrid integrated silicon photonic transceiver in 28nm CMOS and SOI," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, Feb. 2015, pp. 1–3.

[12] Y. Ye, B. Yu, and Q. J. Gu, "A 165-GHz Transmitter With 10.6% Peak DC-to-RF Efficiency and 0.68-pJ/b Energy Efficiency in 65-nm Bulk CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 12, pp. 4573–4584, Dec. 2016.

[13] C. Cao and K. K. O, "A 140-GHz fundamental mode voltage-controlled oscillator in 90-nm CMOS technology," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 10, pp. 555–557, Oct. 2006.

[14] H.-T. Kwon, D. Nguyen, and J.-P. Hong, "A 219-GHz fundamental oscillator with 0.5 mW peak output power and 2.08% DC-to-RF efficiency in a 65 nm CMOS," in *2016 IEEE MTT-S International Microwave Symposium (IMS)*, May 2016, pp. 1–3.

[15] Y. M. Tousi, O. Momeni, and E. Afshari, "A Novel CMOS High-Power Terahertz VCO Based on Coupled Oscillators: Theory and Implementation," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3032–3042, Dec. 2012.

[16] C. Cao, E. Seok, and K. K. O, "192 GHz push-push VCO in 0.13 /spl mu/m CMOS," *Electronics Letters*, vol. 42, no. 4, pp. 208–210, Feb. 2006.

[17] P. Y. Chiang, O. Momeni, and P. Heydari, "A 200-GHz Inductively Tuned VCO With -7-dBm Output Power in 130-nm SiGe BiCMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3666–3673, Oct. 2013.

[18] E. Seok *et al.*, "A 410ghz CMOS Push-Push Oscillator with an On-Chip Patch Antenna," in *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*, Feb. 2008, pp. 472–629.

[19] R. Wanner, R. Lachner, and G. R. Olbrich, "A monolithically integrated 190-GHz SiGe push-push oscillator," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 12, pp. 862–864, Dec. 2005.

[20] C. Jiang, A. Cathelin, and E. Afshari, "An efficient 210GHz compact harmonic oscillator with 1.4dBm peak output power and 10.6% tuning range in 130nm BiCMOS," in *IEEE RFIC Symposium*, May 2016, pp. 194–197.

[21] R. Kananizadeh and O. Momeni, "High-Power and High-Efficiency Millimeter-Wave Harmonic Oscillator Design, Exploiting Harmonic Positive Feedback in CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 10, pp. 3922–3936, Oct. 2017.

[22] H. Rashtian *et al.*, "A 200-GHz triple-push oscillator in 65-nm CMOS with design techniques for enhancing DC-to-RF efficiency," in *2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2016, pp. 77–80.

[23] C. S. Hsieh and J. Y. Liu, "A Low Phase Noise 210-GHz Triple-Push Ring Oscillator in 90-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 4, pp. 1983–1997, Apr. 2018.

[24] J. Grzyb, Y. Zhao, and U. R. Pfeiffer, "A 288-GHz Lens-Integrated Balanced Triple-Push Source in a 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 7, pp. 1751–1761, Jul. 2013.

[25] A. H. M. Shirazi *et al.*, "A quad-core-coupled triple-push 295-to-301 GHz source with 1.25 mW peak output power in 65nm CMOS using slow-wave effect," in *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, May 2016, pp. 190–193.

[26] O. Momeni and E. Afshari, "High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 3, pp. 583–597, 2011.

[27] S. T. Nicolson *et al.*, "Design and Scaling of W-Band SiGe BiCMOS VCOs," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 9, pp. 1821–1833, Sep. 2007.

[28] H. Khatibi, S. Khiyabani, and E. Afshari, "An Efficient High-Power Fundamental Oscillator Above $f_\max /2$: A Systematic Design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 11, pp. 4176–4189, Nov. 2017.

[29] H. Khatibi *et al.*, "A 195 GHz single-transistor fundamental VCO with 15.3% DC-to-RF efficiency, 4.5 mW output power, phase noise FoM of -197 dBc/Hz and 1.1% tuning range in a 55 nm SiGe process," in *IEEE RFIC Symposium*, Jun. 2017, pp. 152–155.

[30] J. M. Guerra *et al.*, "A 285 GHz sub-harmonic injection locked oscillator in 65nm CMOS technology," in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, Jun. 2013, pp. 1–3.

[31] A. Siligaris *et al.*, "A 270-to-300 GHz Sub-Harmonic Injection Locked Oscillator for Frequency Synthesis in Sub-mmW Systems," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 4, pp. 259–261, Apr. 2015.

[32] S. Li *et al.*, "A 200-GHz Sub-Harmonic Injection-Locked Oscillator with 0-dBm Output Power and 3.5% DC-to-RF-Efficiency," in *2018 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2018, pp. 212–215.

[33] P. Y. Chiang *et al.*, "A Silicon-Based 0.3 THz Frequency Synthesizer With Wide Locking Range," *IEEE J. Solid-State Circuits*, vol. 49, no. 12, pp. 2951–2963, Dec. 2014.

[34] R. Han *et al.*, "A SiGe Terahertz Heterodyne Imaging Transmitter With 3.3 mW Radiated Power and Fully-Integrated Phase-Locked Loop," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2935–2947, Dec. 2015.

[35] C. Jiang *et al.*, "A Fully Integrated 320 GHz Coherent Imaging Transceiver in 130 nm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2596–2609, Nov. 2016.

[36] A. Pikovsky, M. Rosenblum, and J. Kurths, *Synchronization: A Universal Concept in Nonlinear Sciences*. Cambridge University Press, Apr. 2003.

[37] C. Huygens, Hollandsche Maatschappij der Wetenschappen, and J. A. Vollgraff, *Oeuvres complètes de Christiaan Huygens*. La Haye : M. Nijhoff, 1888.

[38] J. Peña Ramirez *et al.*, "The sympathy of two pendulum clocks: beyond Huygens' observations," *Nature, Scientific Reports*, vol. 6, p. 23580, Mar. 2016.

[39] R. Ward, *Living Clocks*. New York: Alfred Knopf, 1971.

[40] Y. Deval *et al.*, "HiperLAN 5.4-GHz low-power CMOS synchronous oscillator," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 9, pp. 1525–1530, Sep. 2001.

[41] H. Lapuyade *et al.*, "A Radiation-Hardened Injection Locked Oscillator Devoted to Radio-Frequency Applications," *IEEE Transactions on Nuclear Science*, vol. 53, no. 4, pp. 2040–2046, Aug. 2006.

[42] C. Jany *et al.*, "A Programmable Frequency Multiplier-by-29 Architecture for Millimeter Wave Applications," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 7, pp. 1669–1679, Jul. 2015.

[43] G. Mangraviti *et al.*, "Design and Tuning of Coupled-LC mm-Wave Subharmonically Injection-Locked Oscillators," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 7, pp. 2301–2312, Jul. 2015.

[44] H. R. Rategh and T. H. Lee, "Superharmonic injection-locked frequency dividers," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 6, pp. 813–821, Jun. 1999.

[45] A. Mirzaei *et al.*, "Multi-Phase Injection Widens Lock Range of Ring-Oscillator-Based Frequency Dividers," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 3, pp. 656–671, Mar. 2008.

[46] X. Gui, Z. Chen, and M. M. Green, "Analysis of Nonlinearities in Injection-Locked Frequency Dividers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 3, pp. 945–953, Mar. 2015.

[47] S. Liu *et al.*, "Ring Oscillator Based Injection Locked Frequency Divider Using Dual Injection Paths," *IEEE Microwave and Wireless Components Letters*, vol. 25, no. 5, pp. 322–324, May 2015.

[48] J. H. Cheng, J. H. Tsai, and T. W. Huang, "Design of a 90.9 % Locking Range Injection-Locked Frequency Divider With Device Ratio Optimization in 90-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 1, pp. 187–197, Jan. 2017.

[49] M. Egot *et al.*, "A 20–23ghz Coupled Oscillators Array in 65nm CMOS for HDR 60ghz beamforming applications," in *2011 Proceedings of the ESSCIRC (ESSCIRC)*, Sep. 2011, pp. 463–466.

[50] A. Valdes-Garcia *et al.*, "A SiGe BiCMOS 16-element phased-array transmitter for 60ghz communications," in *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb. 2010, pp. 218–219.

[51] N. Ebrahimi *et al.*, "A 71–86-GHz Phased Array Transceiver Using Wideband Injection-Locked Oscillator Phase Shifters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 65, no. 2, pp. 346–361, Feb. 2017.

[52] J. Lee and H. Wang, "Study of Subharmonically Injection-Locked PLLs," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 5, pp. 1539–1553, May 2009.

[53] I. T. Lee *et al.*, "A divider-less sub-harmonically injection-locked PLL with self-adjusted injection timing," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2013, pp. 414–415.

[54] Y. C. Huang and S. I. Liu, "A 2.4-GHz Subharmonically Injection-Locked PLL With Self-Calibrated Injection Timing," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 2, pp. 417–428, Feb. 2013.

[55] D. Shin, S. Raman, and K. J. Koh, "2.8 A mixed-mode injection frequency-locked loop for self-calibration of injection locking range and phase noise in 0.13um CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, Jan. 2016, pp. 50–51.

[56] D. Shin *et al.*, "A subharmonically injection-locked PLL with 130 fs RMS jitter at 24 GHz using synchronous reference pulse injection from nonlinear VCO envelope

feedback," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 100–103.

[57] V. Uzunoglu and M. H. White, "The synchronous oscillator: a synchronization and tracking network," *IEEE Journal of Solid-State Circuits*, vol. 20, no. 6, pp. 1214–1226, Dec. 1985.

[58] ——, "Synchronous and the coherent phase-locked synchronous oscillators: new techniques in synchronization and tracking," *IEEE Transactions on Circuits and Systems*, vol. 36, no. 7, pp. 997–1004, Jul. 1989.

[59] F. Badets, "Contribution à l'étude de la synchronisation des oscillateurs : intégration des oscillateurs synchrones dans les systèmes radiofréquences en technologie silicium," phdthesis, Universite Bordeaux 1, Jan. 2000.

[60] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, no. 2, pp. 329–330, Feb. 1966.

[61] R. Adler, "A Study of Locking Phenomena in Oscillators," *Proceedings of the IRE*, vol. 34, no. 6, pp. 351–357, Jun. 1946.

[62] R. D. Huntoon and A. Weiss, "Synchronization of Oscillators," *Proceedings of the IRE*, vol. 35, no. 12, pp. 1415–1423, Dec. 1947.

[63] L. J. Paciorek, "Injection locking of oscillators," *Proceedings of the IEEE*, vol. 53, no. 11, pp. 1723–1727, Nov. 1965.

[64] L. W. Couch, "A Study of a Driven Oscillator with FM Feedback by Use of a Phase-Lock-Loop Model," *IEEE Transactions on Microwave Theory and Techniques*, vol. 19, no. 4, pp. 357–366, Apr. 1971.

[65] J. J. Lynch and R. A. York, "Synchronization of oscillators coupled through narrow-band networks," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 2, pp. 237–249, Feb. 2001.

[66] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 9, pp. 1415–1424, Sep. 2004.

[67] P. Bhansali and J. Roychowdhury, "Gen-Adler: The generalized Adler's equation for injection locking analysis in oscillators," in *2009 Asia and South Pacific Design Automation Conference*, Jan. 2009, pp. 522–527.

[68] C. J. Li *et al.*, "A Rigorous Analysis of a Phase-Locked Oscillator Under Injection," *IEEE Transactions on Microwave Theory and Techniques*, vol. 58, no. 5, pp. 1391–1400, May 2010.

[69] Q. Béraud-Sudreau *et al.*, "VHDL-AMS model of an injection locked VCO," in *10th IEEE International NEWCAS Conference*, Jun. 2012, pp. 25–28.

[70] A. Buonomo and A. L. Schiavo, "Remarks on the Adler's equation," in *2015 European Conference on Circuit Theory and Design (ECCTD)*, Aug. 2015, pp. 1–4.

[71] E. L. Ginzton *et al.*, "Distributed Amplification," *Proceedings of the IRE*, vol. 36, no. 8, pp. 956–969, Aug. 1948.

[72] D. M. Pozar, *Microwave Engineering, 4th Edition*. Wiley, Nov. 2011.

[73] P. Gamand, Y. Crosnier, and P. Gelin, "Large-signal capabilities and analysis of distributed amplifiers," *Electronics Letters*, vol. 20, no. 8, pp. 317–319, Apr. 1984.

[74] J. Kim and J. F. Buckwalter, "A 92 GHz Bandwidth Distributed Amplifier in a 45 nm SOI CMOS Technology," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 6, pp. 329–331, Jun. 2011.

[75] D. Fritsche *et al.*, "A Trimmable Cascaded Distributed Amplifier With 1.6 THz Gain-Bandwidth Product," *IEEE Transactions on Terahertz Science and Technology*, vol. 5, no. 6, pp. 1094–1096, Nov. 2015.

[76] P. V. Testa *et al.*, "Analysis and Design of a 30- to 220-GHz Balanced Cascaded Single-Stage Distributed Amplifier in 130-nm SiGe BiCMOS," *IEEE Journal of Solid-State Circuits*, vol. PP, no. 99, pp. 1–11, 2018.

[77] Z. Skvor, S. R. Saunders, and C. S. Aitchison, "Novel decade electronically tunable microwave oscillator based on the distributed amplifier," *Electronics Letters*, vol. 28, no. 17, pp. 1647–1648, Aug. 1992.

[78] H. Wu and A. Hajimiri, "Silicon-based distributed voltage-controlled oscillators," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 493–502, Mar. 2001.

[79] R. Guillaume *et al.*, "Energy efficient distributed-oscillators at 134 and 202ghz with phase-noise optimization through body-bias control in 28nm CMOS FDSOI technology," in *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, Jun. 2017, pp. 156–159.

[80] R. Han and E. Afshari, "A CMOS High-Power Broadband 260-GHz Radiator Array for Spectroscopy," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 3090–3104, Dec. 2013.

[81] A. Cathelin, "Fully Depleted Silicon on Insulator Devices CMOS: The 28-nm Node Is the Perfect Technology for Analog, RF, mmW, and Mixed-Signal System-on-Chip Integration," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 18–26, 2017.

[82] A. Larie, "Design of highly linear 60GHz power amplifiers in nanoscale CMOS technologies," Theses, Université de Bordeaux, Oct. 2014. [Online]. Available: https://tel.archives-ouvertes.fr/tel-01142532

[83] N. Seller, "Contribution à l'Étude, au Développement et à la Réalisation d'Oscillateurs à Controle Numérique en Technologie Silicium Avancée," Theses, Université de Bordeaux, 2008. [Online]. Available: http://www.theses.fr/2008BOR13648

[84] E. Morifuji *et al.*, "Future perspective and scaling down roadmap for RF CMOS," in *1999 Symposium on VLSI Technology. Digest of Technical Papers (IEEE Cat. No.99CH36325)*, Jun. 1999, pp. 163–164.

[85] T. O. Dickson *et al.*, "The Invariance of Characteristic Current Densities in Nanoscale MOSFETs and Its Impact on Algorithmic Design Methodologies and Design Porting of Si(Ge) (Bi)CMOS High-Speed Building Blocks," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, pp. 1830–1845, Aug. 2006.

[86] B. Martineau, "Potentialités de la technologie CMOS 65nm SOI pour des applications sans fils en bande millimétrique," thesis, Lille 1, May 2008. [Online]. Available: http://www.theses.fr/2008LIL10041

[87] B. Martineau *et al.*, "80 GHz low noise amplifiers in 65nm CMOS SOI," in *ESSCIRC 2007 - 33rd European Solid-State Circuits Conference*, Sep. 2007, pp. 348–351.

[88] "Parasitic Extraction - StarRC." [Online]. Available: https://www.synopsys.com/implementation-and-signoff/signoff/starrc.html

[89] "Infinity Waveguide Probe." [Online]. Available: https://www.formfactor.com/product/probes/infinity/infinity-waveguide-probe/

[90] "GGB Industries, Inc. Home Page." [Online]. Available: http://www.ggb.com/index.html

[91] M. Potéreau, "Contribution on the characterization of sub THz components," Theses, Université de Bordeaux, Nov. 2015. [Online]. Available: https://tel.archives-ouvertes.fr/tel-01269635

[92] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[93] O. Momeni and E. Afshari, "A high gain 107 GHz amplifier in 130 nm CMOS," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, Sep. 2011, pp. 1–4.

[94] O. Momeni, "A 260ghz amplifier with 9.2db gain and -3.9dbm saturated power in 65nm CMOS," in *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2013, pp. 140–141.