Caractérisations électriques et modélisation des phénomènes de piégeages affectant la fiabilité des technologies CMOS avancées (Nanofils) 10nm

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THÈSE

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Spécialité : **Nano électronique et Nano technologie**

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Présentée par

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codirigée par **Dr. Xavier Garros, CEA-LETI**

préparée au sein du **CEA-LETI et de l'IMEP-LAHC**
dans **l'École Doctorale Electronique, Electrotechnique, Automation et Traitement du Signal**

Electrical characterization & modeling of the trapping phenomena impacting the reliability of nanowire transistors for sub 10nm nodes

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To my grandparents, Artemisia and Petros

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Glossary

Abbreviation	Description
AVGP	Arbitrary VG Pattern
BL	Bottom-Level
BOX	Buried Oxide Layer
CCDF	Complementary Cumulative Distribution Function
CDF	Cumulative Distribution Function
CET	Capture and Emission Time
CMOS	Complementary Metal Oxide Semiconductor
CNF	Carrier Number Fluctuations
CNF/CMF	Carrier Number Fluctuation/ Correlated Mobility Fluctuation
CNT	Carbon nanotubes
CP	Charge Pumping
CV	Capacitance-Voltage
DCM	Defect Centric Model
DF	Duty Factor
DIBL	Drain-Induced Barrier Lowering
DV	Dynamic Variability
EOT	Equivalent Oxide Thickness
ESR	Electron Spin Resonance
FDSOI	Fully Depleted Silicon-On-Insulator
FEOL	Front End of the Line
FFT	Fast Fourier Transform
GAA	Gate-All-Around
HCI	Hot Carrier Injection
HK/MG	High-k/Metal Gate
HMF	Hooge Mobility Fluctuations
HRTEM	High-Resolution Transmission Electron Microscopy
HT	High Temperature
IL	Interface Layer
ITRS	International Technology Roadmap for Semiconductors
LFN	Low Frequency Noise
LT	Low Temperature
MC	Monte Carlo
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSM	Measure-Stress-Measure
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
PDSOI	Partially Depleted Silicon-On-Insulator

PNA	Post Nitridation Anneal
PSD	Power Spectral Density
R-D	Reaction-Diffusion
RSU	Remote-sense and Switch Unit
RTN	Random Telegraph Noise
S/D	Source/Drain
SCE	Short-Channel Effects
SMS	Stress-Measure-Stress
SOI	Silicon-On-Insulator
SW	Side Walls
TB	Thermal Budget
TDDB	Time Dependent Dielectric Breakdown
TDDS	Time Dependent Defect Spectroscopy
TEM	Transmission Electron Microscopy
TL	Top-Level
TS	Top Surface
TSV	Through Silicon Via
TTF	Time-To-Failure
WF	Work Function
WGFMU	Waveform Generator Fast Measuring Unit

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General context

Around 70 years ago, at the end of 1947, three colleagues - W. Shockley, J. Bardeen and W. Brattain - made an invention that was about to change the world of solid-state electronics. It was the first working bipolar point junction transistor in Bell laboratories. A few years later, the most commonly used transistor up to this date was fabricated, the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) with Gordon Moore making the prediction that the number of transistors per chip would double every two years [1] and the integrated circuits (ICs) would become smaller, faster and cheaper. In order to continue the frantic chase of these three characteristics, we kept on scaling our devices. It is possible to divide the different ages of scaling in three categories [2]:

- Geometrical scaling (1975-2003): During this period, we experienced the reduction of the physical dimensions which, in turn, improved the transistors' performance.
- Equivalent scaling (2003~2024): Here we not only have the geometrical scaling, but also the introduction of new materials either in the gate stack or incorporated in the channel, even though the silicon remains the top candidate in terms of performance and cost. In addition to that, new architecture designs, like Fully Depleted Silicon-On-Insulator (FDSOI), FinFETs and Trigate Nanowires, have been proposed to replace the standard planar MOSFETs.
- 3D power scaling (2024~203X): Alternatively known as "More than Moore", in which we will have heterogeneous integration (MEMS, Photonics, Biochips, etc.) and reduced power consumption with the help of vertical structures.

However, along with the advancements in the semiconductor industry targeting an improved performance, additional reliability issues have emerged. Reliability, which is defined as "The probability that an item will perform a required function under stated conditions for a specific period of time" is impacted by the microscopic defects that are induced by the fabrication process or the ageing of the device under electrical stress. It is essential to be confident that the designed everyday used products will not fail after a short time, like the processor of our computer or the battery in our mobile. Since this aspect of CMOS technology becomes more and more important nowadays, it is necessary to study the degradation mechanisms that take place in the above scaling categories which is the purpose of this thesis.

In the first chapter, we will see an introduction on new generation devices, having novel architectures or newly introduced materials, as well as an introduction to a cutting-edge integration process; the 3D sequential integration (CoolCube^{TM}). In addition to that, we will describe the meaning of reliability and the trapping phenomena that occur on CMOS transistors along with a review of the existing models that help us describe the physical mechanisms behind them. Finally, we will have an analytical report of the measurement methods that were used during this thesis.

In the second chapter, we will focus on the 3D architectures that have been studied (Trigate nanowires) and their channel size dependence on t_0 reliability, due to pre-existing defects, compared to previously reported works w.r.t. the results from Monte Carlo simulations. After

that we will see how the already known methods for trap extraction can be applied in 3D architectures and compare the two most popularly used at this time.

The third chapter will show a study concerning the impact of 3D sequential integration on reliability. At first, “simulating” the behavior of a Top-Level transistor and providing a set of guidelines with all the important process steps that can be improved. And at the end of the chapter, we will present, for the first time, a complete study of a fully integrated 3D sequential technology concerning performance reliability of both levels.

For the fourth, and final, chapter, we will see how new high mobility materials incorporated in the channel (Germanium in particular) are affecting NBTI reliability and we will provide a new insight regarding the physical mechanisms that are repeatedly reported to be improving the degradation in SiGe channel planar PMOSFETs. To do so, we will present an extensive set of reliability measurements on large and smaller transistors, having a thin or thick gate oxide and conclude on which are the defects that are responsible for this improvement or not.

Chapter 1. Introduction

1.1 Issues on conventional planar technologies

We already live in the era of technological breakthroughs, where we can fit in the palm of our hand the power, the speed and the performance of a supercomputer that a few years ago would fit in a room. Surely, none of the transistor's inventors would imagine that the impact of their research, 70 years later, still plays the most important role in the digital revolution. The building block of every electronic device that we use is the MOSFET, but as we try to make it smaller and reduce the cost of fabrication at the same time, we face different challenges. Standard bulk planar MOSFETs are particularly susceptible to two phenomena: the so-called Short-Channel Effects (SCE) (Figure 1.1) and Drain-Induced Barrier Lowering (DIBL) (Figure 1.2). During the first one, the gate loses the electrostatic control of the channel as the electric field lines propagate through the depletion regions of the source and drain, as they move closer to one another on shorter gate lengths. The second one is due to the lowering of the potential barrier between the drain and the source caused by the drain polarization. The lowering of the source barrier causes an injection of extra carriers which, in turn, increases the current substantially. This increase of current shows up in both, above-threshold and subthreshold regimes. As a result from SCEs we have a decrease of the threshold voltage which, finally, is calculated as [3]:

$$V_{T,short} = V_{T,long} - SCE - DIBL \qquad \text{Eq. 1.1}$$

with DIBL to be defined as:

$$DIBL = V_T\ (high\ V_D) - V_T\ (low\ V_D) \qquad \text{Eq. 1.2}$$

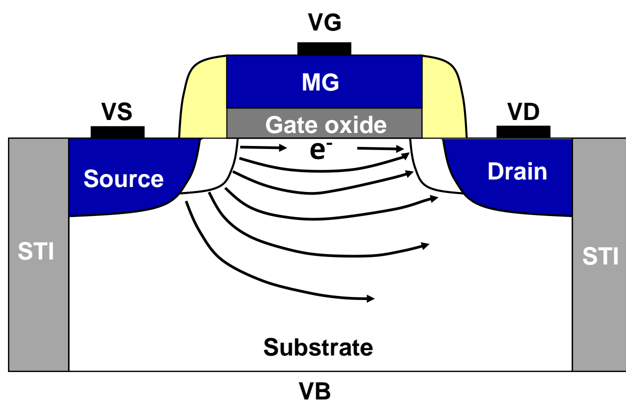


Figure 1.1 Schematic of a Bulk transistor suffering from Short-Channel Effects (SCE), reproduced from [4].

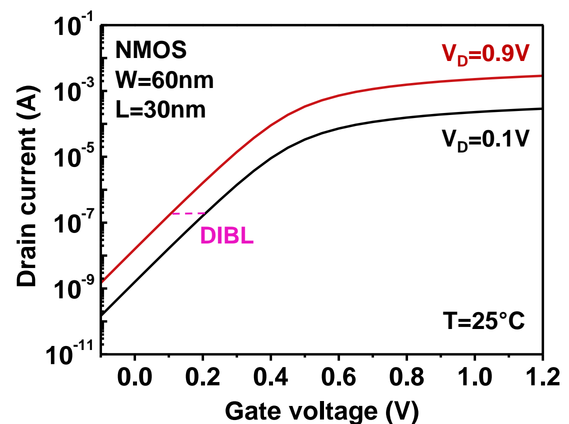


Figure 1.2 Increase of drain current and shift of threshold voltage due to Drain-Induced Barrier Lowering (DIBL).

1.1.1 Equivalent scaling opportunities

As was presented before, two decades ago it became quite obvious that the requested performance improvement could not be easily reached and the technology optimization for

very short gate lengths (<30nm) had to be done in a different way in order to avoid parasitic effects and for the gate to maintain the control of the channel. At this very moment we are living the "Equivalent scaling era", so in the next part, we will present the major technological advancements over the past few years to meet the expectations of ITRS concerning the aggressive gate dimensions.

1.1.2 SOI process

In order to avoid the aforementioned issues with planar transistors, the industry turned to a new type of process technology, called SOI (Silicon-On-Insulator). The difference from the standard MOS is that now we have a Buried Oxide Layer (BOX), constituting of Silicon Dioxide (SiO_2) providing an extra isolation to the body from the substrate with the silicon film that is used to form the channel to be a single crystal, very thin and undoped (typical doping value $N_A=10^{15}$ cm^{-3}).

The fabrication process that has changed the SOI production is called SmartCut™ [5] and was developed by Soitec in collaboration with CEA-Leti. In Figure 1.3, we can see a simplified description of the followed procedure. The whole process starts with wafer A acting as a donor that becomes thermally oxidized to develop the SiO_2 layer that will be used as BOX of the final wafer. Hydrogen implantation through cleavage layer creation is applied to settle the transferred Si thickness. After that, the surface is cleaned and the two wafers are bonded, while the cleavage layer is split. As a result, we have structures with a thin silicon film on BOX with two additional parameters to consider: the silicon thickness, t_{Si}, and the thickness of the BOX, t_{BOX}. According to them, the SOI devices can be separated in two categories:

- Partially Depleted SOI (PDSOI): If $t_{Si} > W_D$ (thickness of the depletion zone), the silicon film has a non-depleted neutral zone and avalanche ionization at the drain can lead to accumulation of charges in the partially depleted zone, what we call floating body effect
- Fully Depleted SOI (FDSOI): when the t_{Si} is smaller than the depletion zone and there is no floating body effect.

In the thesis, only the second category, the FDSOI structures, has been studied with the silicon thickness to vary from 7nm for planar transistors to 24nm for Trigate MOSFETs.

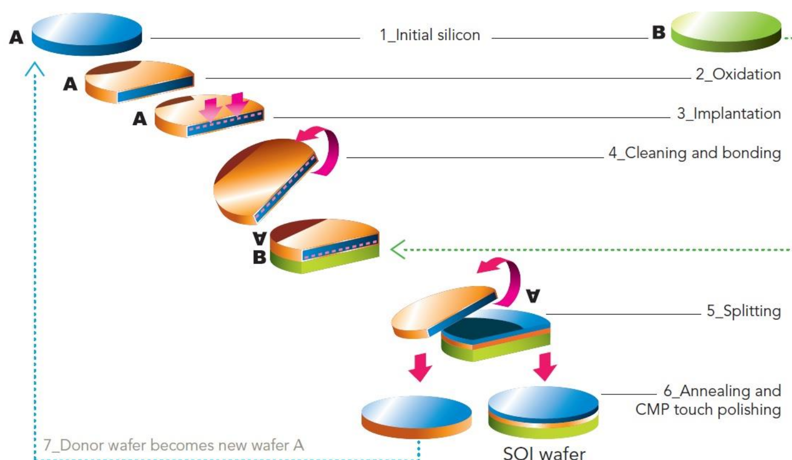


Figure 1.3 SmartCut™ fabrication process [5] for the manufacturing of SOI wafers.

1.1.3 3D architectures

Along with FDSOI, there have been other technologies that have pushed the equivalent scaling area into new limits giving, also, solutions for decreasing SCEs. By introducing 3D architectures [6]–[8] as alternative candidates to the conventional planar ones, it is possible to increase the gate area without increasing the total surface of the transistor and continue obey the scaling law. In that way, we can achieve the requested electrostatic control [9], [10], shielding of the channel from parasitic electric fields, lower gate leakage current, higher gate-drive current and lower DIBL.

These architectures, shown in Figure 1.4 [7], are characterized by the number of gates that they have, like double, triple or even all around. The first multi-gate device (double-gate), in Figure 1.4 (a), was introduced in the late '90s [6], [11] , having a thick dielectric, called 'hardmask' that prevented the formation of the inversion channel on the top surface, so only the two sides were used for conduction. Regarding Trigate structures, we can find them in the literature implemented either on an SOI or a Bulk wafer ((b) and (f) in Figure 1.4) and the three conduction surfaces help us towards the advantages that we reported before. Two other possible design are Π-gate and Ω-gate FETs ((c) and (d) in Figure 1.4), which improve the gate control compared to Trigate due to the lateral electric field at the bottom and, of course, the increased channel surface. For the second one the use of H_2 anneal helps us smooth the fin surfaces and round the corners, improving the mobility and reducing even more the gate leakage. The same procedure is followed for processing a Gate-All-Around (GAA) FETs (Figure 1.4 (e)), devices in which the gate is completely wrapped around the channel and that they have shown to be able to maintain the electrostatic control for dimensions down to 3nm [12].

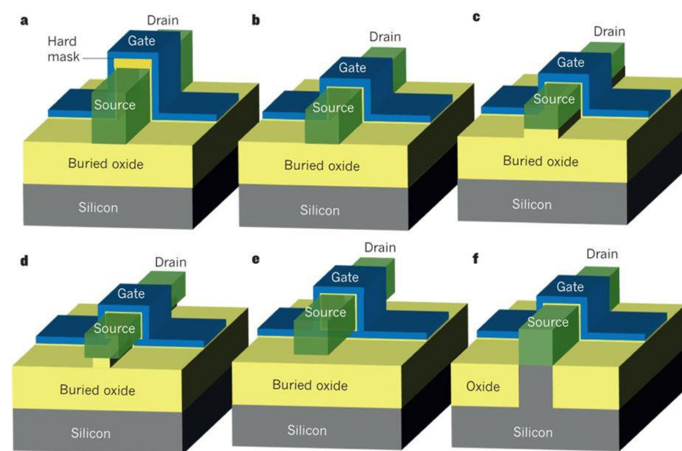


Figure 1.4 Overview of the existing 3D MOSFET architectures (a) SOI FinFET, (b) SOI Trigate, (c) SOI Π-gate, (d) SOI Ω-gate, (e) SOI GAA, (f) Bulk Trigate [7].

1.1.4 New materials

Along with the width, length and height, W, L and t_{Si} respectively, there is another dimension that has to decrease on this scaling "game": the thickness of the oxide, according to Eq. 1.3,

$$C_{OX} = \frac{\varepsilon_{OX}}{T_{OX}} \quad \text{Eq. 1.3}$$

where C_{OX} is the gate oxide capacitance, ε_{OX} the dielectric constant and T_{OX} the oxide thickness. Having a small oxide thickness leads to an increased gate capacitance and as consequence to reduce SCEs. For some years, SiO_2 was scaling proportionally to the gate length, down to an Equivalent Oxide Thickness (EOT) equal to 1.1nm in 2006 when it reached its lowest limit. After that, the known problem of leakage current emerged again due to the direct tunneling of carrier phenomena and lifetime prediction as well as power consumption became an issue. Everyone wanted to avoid these phenomena, so the research community started looking for other materials that could replace SiO_2 and since,

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{OX}} * T_{OX} \quad \text{Eq. 1.4}$$

with ε_{SiO2} the relative permittivity of SiO_2 equal to 3.9 and ε_{OX} the permittivity of the new dielectric, it was clear that we needed something with a high dielectric constant to do so.

In Figure 1.5, we can see a list of studied high-k materials towards this goal which had to be evaluated according to four criteria [13]:

1) to be able to scale to lower EOTs
2) to limit the loss of carrier mobility in the Si channel
3) to stop the gate threshold instabilities caused by the high defect densities of the poor-quality interface between the channel and the high-k
4) and to control the gate threshold voltage, which led to the need of metal gates.

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si
SiO_2	3.9	8.9	3.2
Si_3N_4	7	5.1	2
Al_2O_3	9	8.7	2.8[a]
Y_2O_3	15	5.6	2.3[a]
La_2O_3	30	4.3	2.3[a]
Ta_2O_5	26	4.5	1–1.5
TiO_2	80	3.5	1.2
HfO_2	25	5.7	1.5[a]
ZrO_2	25	7.8	1.4[a]

Figure 1.5 Electrical properties of the most researched high-k materials [13].

Nowadays, most of the HK/MG stacks consist of HfO_2 or middle solutions, like Hafnium-based oxides (HfSiON) to lower the defect density. An alternative way that is widely used is a combination of HfO_2, on top, and SiO_2, next to the silicon, to improve the interface quality. In both cases, we need to be compatible with the applied metal gate, for example TiN, whose workfunction can be adjusted using different deposition process or thickness.

Besides the gate stack material, we have been looking for different channel materials as well. Germanium incorporation [14] in the channel of PMOSFETs has improved, not only the mobility [15]- aka performance of transistors, but has also given an improved reliability [16], [17]. This part will be presented extensively in the last chapter of the thesis. Alternative materials, such as III-V semiconductors (GaAs, InGaAs, InAs, InP) [18] which are the number one choice for NMOSFETs' advancement, are investigated for the next generation CMOS technology as well as 2D materials (Graphene, MoS_2, etc.) [19]–[21] or Carbon nanotubes (CNT) [22]. Even though, the most important part is to find ways to obtain high interface quality, low access resistance and, of course, low cost CMOS integration methods, they appear as very promising candidates for future flexible and transparent devices.

1.1.5 3D sequential integration

The last, and apparently final, report of ITRS [23], [24] was published in 2015 reporting that Moore's law will not continue in the traditional dimensional scaling way that we know so far and will reach its final limit at 2021. So the electrical performance and current limit will no longer be the primary target, but the focus will now be on how we can take advantage of the existing technology and adapt it to the needs of the market [25], [26] and the world, like the use of GPS, clinical wearables and biosensors. Even from the economical aspect of view [27], the fabrication of a new scaled node becomes more and more expensive due to the necessity of high-precision equipment and design tools. So, it is quite obvious that we march, or better run, towards the 3D power scaling era, with the 3D integration to be one of the frontrunners in "More than Moore" (r)evolution.

The whole concept of this integration is to fabricate one transistor on top of another to achieve a high density of components which results in high performance and reduced scaling for lower cost [27], using its unique 3D contact characteristics towards the new age [28], [29]. Depending on the requested application, it can feature the different technologies described before, like FDSOI on FDSOI structures [30] or FinFET on FinFET [31] in order to achieve the best possible outcome each time. Towards this road, we can distinguish two types of 3D integration: the parallel and the sequential.

In the parallel one, the wafers are processed separately and the two levels are connected at the end using Through Silicon Vias (TSVs) which limit substantially the alignment precision. Another drawback is that the TSVs are quite large and as a result we have higher parasitic impedances.

In the sequential integration (Figure 1.6 & Figure 1.7), the process is done continuously, with the Top-Level using the previous alignment marks from the bottom one. In that way, the two transistors are fully aligned which in turn, favors the increase of 3D contacts density. But the Top-Level device has to be processed in a certain way, so that the bottom transistor remains unaffected, which means that the thermal budget must be decreased [32], [33]. Additionally to the temperature limitation, the integration itself is particularly complex and all the processing steps have to be evaluated at the same time [34], [35].

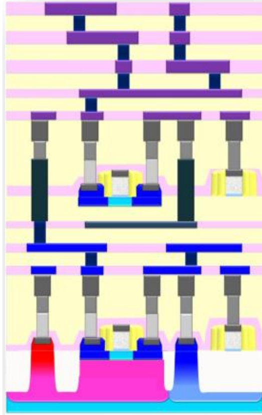


Figure 1.6 CEA-Leti's CoolCube^{TM} sequential integration.

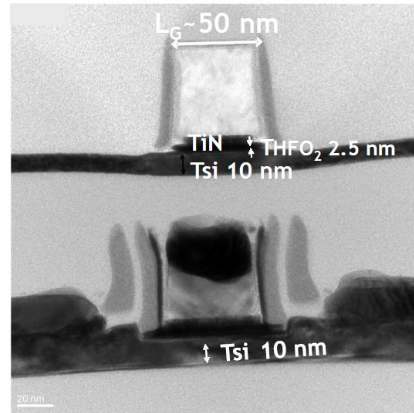


Figure 1.7 3D sequential stacked transistors with process secured alignment [36].

The pioneer towards this concept is CEA-Leti with several groups around the globe becoming attracted by the idea and working towards this kind of integration (like IMEC [37], NDL [38] and Stanford [39]). Even though, there is a lot of research regarding the processing procedure that has to be followed to reach a high Top-Level performance, there are limited results regarding the reliability of the integration [40], an issue that we will try to address fully in Chapter 3.

1.2 Oxide defects overview

Until now, we have only talked about the advancements on CMOS technology from the performance point of view. Of course, it's great to have a fast computer or a high-resolution camera on your smartphone, but you have to be sure that it will continue doing its job for a long time. This is where reliability comes and since MOSFET is the building block of all electronic devices, it is important to know and understand the degradation mechanisms that take place due to an increased gate voltage application, a transistor's operation under an elevated temperature (Reliability) or even the ones that are due to the manufacturing process (Yield).

Whether a device is reliable or not, there is one thing to blame: the defects that exist in the gate oxide of the transistor [41], [42]. For many years, the CMOS technology has been successful due to the advantageous properties of SiO_2 [43]: high energy band, low defect density, easy to become process integrated etc. But the introduction of the high-k materials that we saw before, introduced also additional problems. In this part, we will present an overview of the different oxide defect categories and try to see how each one is affecting both Yield and Reliability.

1.2.1 Fixed oxide charge

Fixed oxide charges were one of the first observed defects since the beginning of CMOS production. They are located near the Si/SiO_2 interface and are directly related to the fabrication process, specifically from the Si oxidation step and the used temperature. The good news is that there is no electrical communication with the silicon channel, therefore it belongs to the pre-existing defects category and only affects the initial MOSFET parameters, like a static shift on the flatband voltage.

1.2.2 Mobile oxide charge

The mobile oxide charge is mainly caused by the ionic impurities of sodium (Na+), lithium (Li+) and potassium (K+). They are also related to the processing techniques, so the yield part, and are causing threshold voltage instabilities when positive gate bias is applied, with sodium being the first impurity to be related to this gate bias instability [44]. In order for them not to become an oxide reliability problem, the density should be kept low, around $10^9 cm^{-2}$.

1.2.3 Oxide trapped charge

Moving now to a more serious category of oxide defects, the oxide trapped charge. This charge can be either positive or negative, in the bulk of the oxide, and is due to the filling of the defects by holes or electrons, with the electron traps being distributed through the oxide and the hole traps located near the Si/SiO_2 interface. This too, can originate from the processing after the oxide growth but also from the defects that are generated when the transistor is under operation, like during electrical stress in a high field. As we will see later, this type of defects plays an important role during Positive Bias Temperature Instability (PBTI), on NMOS, during which the traps in the high-k prevail.

1.2.4 Interface trapped charge

The number one danger for the gradual, or even without return, degradation is the interface trapped charge. They are next to the silicon channel and can be either acceptors or donors, depending on their position w.r.t. the bandgap, upper or lower half respectively. The number of caused effects are numerous: impact on capacitance, leakage current, noise level and, of course, on the Negative Bias Temperature Instability (NBTI) that we will see later on. They are originally created by the dangling bonds at Si/SiO_2 interface, with their density (D_{IT}) to be depending on the surface orientation. When they were first identified by Electron Spin Resonance (ESR) [45], they were called P_b centers and were divided into two types (Figure 1.8):

- P_{b0}, for •Si ≡ Si_3 bonds and
- P_{b1}, for the Si_2 = Si •−Si ≡ Si_2O ones,

with the latter having a minor impact compared to the first one [46].

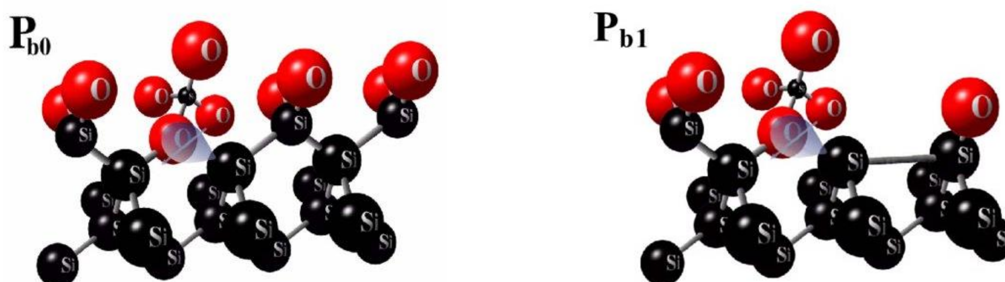


Figure 1.8 The two types of interface charge [47].

Regarding the occupying states at flatband, each time, they can be distinguished in three categories:

- Neutral: states at the lower half of the bandgap when the electron occupied states are below the Fermi level (occupied donors) or above the Fermi level (unoccupied acceptors)
- Negative: states between the midgap and the Fermi level (occupied acceptors)
- Positive: when a PMOSFET is inverted, the interface traps between midgap and Fermi level are unoccupied donors and as a result we have positively charged interface traps which lead to negative threshold voltage shifts (NBTI mentioned before).

A way to decrease the density of interface traps and avoid, at some part, the detrimental impact of these defects is the use of H_2 anneal [48]. The hydrogen atom will fill the dangling bond and neutralize it, the so-called passivation. However, the hydrogen chemistry is very important since it can go sideways and depassivate again the bond, especially under the application of electrical stress.

1.2.5 Border traps

Around 24 years ago, D. Fleetwood [49] suggested an extension of the, already long, list of gate oxide defects by introducing the border traps, positively charged oxide traps passivated with hydrogen. The most common border traps are oxygen (O) vacancies and/or defects that contain hydrogen (Hydrogen bridge & Hydroxyl E' center). They are characterized as near-interfacial oxide traps and can communicate by tunneling from the semiconductor to the traps and back having larger emission and capture time constants than the interface or oxide traps. Recent studies have shown that this "communication", in PMOSFETs, can happen not only through tunneling but also through trap-assisted tunneling or even thermal activation [50], [51]. All these sound familiar since they are similar processes occurring during the recovery part of a fast NBTI measurement [52], whose modeling we'll see in the next section.

For quite some time, it was difficult to distinguish the impact of border and interface traps with the key point being the measurement speed. In the chase of border traps' identification, we have some measurement methods as allies, like Charge Pumping, Low Frequency Noise and Time Dependent Defect Spectroscopy. Details for all of them will be presented in the next sections.

1.3 Bias Temperature Instability

Now that we have a general idea regarding the defects in the gate oxide, let's discuss about how they affect the electrical parameters of MOSFETs, unfortunately always in a negative way: the widely known reliability.

Maybe the most recognized illustration among reliability engineers is the one in Figure 1.9, the bathtub curve. It indicates the lifecycle of an electronic component, or a transistor in our case, and is composed of three parts: the infant mortality, the useful life and the wearout. We all want to avoid the first one and stay as much as possible in the second one. Regarding the third part, we would all wish to never go there, but that's not how it works! The infant mortality

is related to pre-existing defects and is correlated to the yield that we mentioned before. During the useful life, there are only some random defects in the transistor, now necessarily affecting it. Eventually, we arrive in the wearout part, caused usually by accelerated testing and characterization in extreme conditions of voltage, current or temperature. The questions that emerge in this part are: why, when and how this failure has occurred. In the case of the CMOS technology, specifically the Front End of the Line (FEOL) reliability, there are three degradation mechanisms: one that describes the sudden failure of transistors, called Time Dependent Dielectric Breakdown (TDDB) or the gradual one, as it is the case with the Bias Temperature Instability (BTI) and the Hot Carrier Injection (HCI).

In this section and, in general in this thesis, we will focus only on the second type of failure and specifically the BTI.

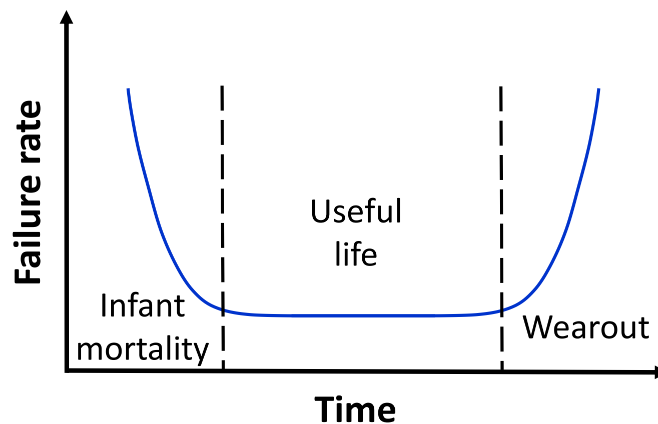


Figure 1.9 Bathtub curve showing the lifecycle of a product.

1.3.1 BTI degradation

The principle of BTI is to force a stress voltage on the gate by keeping, at the same time, the drain and the source at 0V as it appears in Figure 1.10. In that way, there is no drain current flowing in the channel and makes it possible to record the threshold voltage drift that occurs with time. Since it is an acceleration test, part of the wearout period, it is typically performed at a high temperature of 125°C. When this method is implemented on NMOSFETs the V_G stress is positive (PBTI) which causes a negative oxide charge that leads to a positive V_{TH} shift. The opposite applies on PMOSFETs (NBTI): the $V_{G,\ stress}$ is negative which induces a positive oxide trapping that results to a negative V_{TH} shift (Figure 1.11). But this time, there is an additional impact: the creation of interface states, as well, impacting the mobility, transconductance and subthreshold slope degradation. Historically, it’s the NBTI that constitutes the major reliability problem, since PMOSFETs are subjected to a degradation almost four times higher than the corresponding NMOS. For that reason, the research for a model suitable for NBTI prediction and description is of an imperative need.

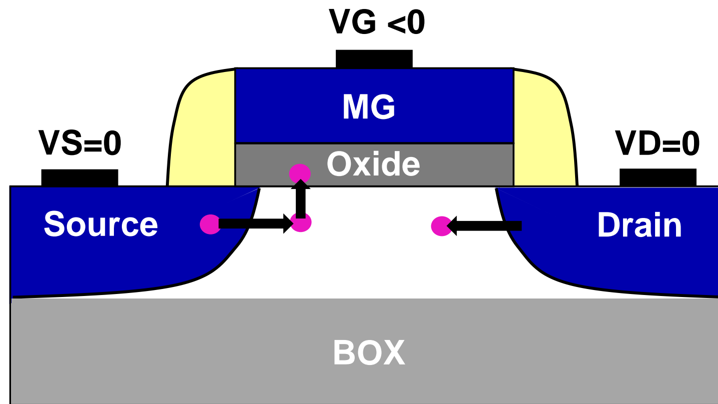


Figure 1.10 FDSOI MOSFET under BTI stress.

Even though NBTI is a problem that is bothering the reliability community for more than 50 years, there are still some blank spots regarding its origin which, consequently, has emerged disputes for its modeling [53], [54]. Especially, with the CMOS advancement on oxides (high-k), process (i.e. nitridation) or structures (Trigate), it has become an important concern will trying to ensure the lifetime of a transistor. We'll see now an overview of the existing models, separated in two different approaches, and the recent progress regarding the physical explanation of this reliability concern.

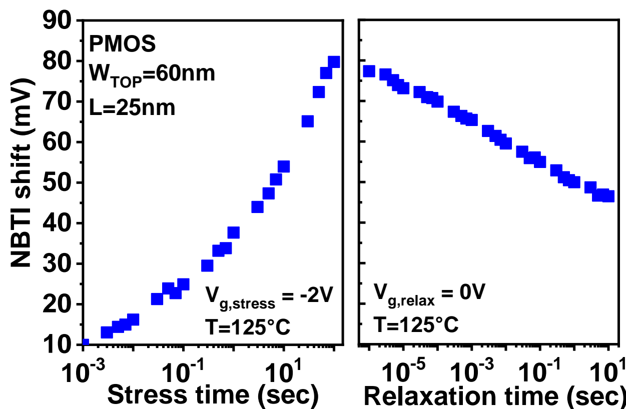


Figure 1.11 Typical V_{TH} shift of stress and recovery in FDSOI MOSFET.

1.3.2 Reaction-Diffusion model

The first attempted try, to describe the creation of interface traps during a NBTI stress was called Reaction-Diffusion (R-D) model [55], [56]. This model is based on the breaking of the Si-H bonds at the Si/SiO_2, forming dangling bonds, and the diffusion of the charged hydrogen atoms into the gate oxide. The free hydrogen can then recombine with other available atoms forming molecular H_2 that can also diffuse into the gate oxide (Figure 1.12). Nonetheless, several process knobs tend to improve this situation, like with the use of forming gas (H_2) or high-pressure deuterium anneal that seems to “cure” the dangling bonds which means that the NBTI degradation is mainly related to the interface states. This worked really well during that time, since everyone was mostly concerned about the kinetics of interface traps to explain the degradation.

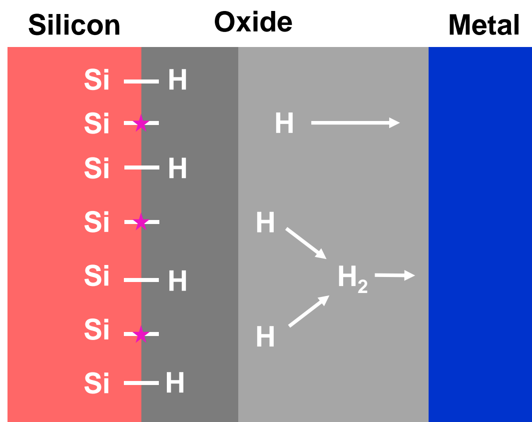


Figure 1.12 Reaction-Diffusion model principle.

But, the development of fast measuring techniques, over the past decade, has revealed the limitations of the model. Specifically, it has proven difficult for the R-D to fully describe experimental results [57], especially in the relaxation part [58], [59], [60]. The recovery part starts as soon as the stress is removed and it is globally uniform over the entire relaxation period. The R-D model could only predict a relaxation during 4 decades of time while the recovery should be relatively slow. In addition, the relaxation predicted by the R-D model is due to the back scattering of the neutral H_2 species to the substrate. Since they are neutral, they should not be influenced by the gate bias during relaxation, but experiments have shown that the relaxation is highly dependent on the applied $V_{G,\ relax}$ [60]. Finally, while the R-D model predicts that the relaxation depends on the initial hydrogen concentration, it has been shown that is independent of the Si/SiO_2 interface passivation [58], [61].

1.3.3 Huard's model

It was not until 2006 that a new interpretation of the NBTI physical mechanisms appeared [61]–[63]. Huard this time considered two different components of NBTI degradation, independent from one another, the permanent and the recoverable. The recoverable part that is due to the hole trapping occurring mostly in pre-existing defects with long capture and emission time constants, which can be reversible since the holes can be re-emitted into the channel or the gate. This means that this part of degradation is exclusively related to the fabrication process of the device. On the other hand, the permanent part, attributed to the aforementioned dangling bonds created by stress. This time, we are talking about very fast defects with short time constants which are very difficult to be repassivated with the process steps that we saw before.

1.3.4 Grasser's model

A few years later, in 2009 [64], Grasser proposed a different version of Huard's model where the permanent and recoverable phenomena are related. The creation of interface states may be justified from the R-D model but not only, while it predicts the hole trapping taking place in stress-driven gaps. It is now called a quasi-permanent phenomenon since it can have long recovery times, longer than the experimental timescale. The recoverable part, at the same time, is considered to be explained by the capture of holes in oxygen deficiencies through Multi Phonon Field Assisted Tunneling. Even though this model, can reproduce experimental data of stress and relaxation, it faces some difficulties when it comes to other gate oxides or processing steps, since it cannot consider deficiencies other than the oxygen ones. This led to an update

of the existing model in 2014 [65], indicating that the recovery is more reaction-limited than diffusion-limited.

Right now, we are still considering two different components of the NBTI degradation, but there are some updates regarding the microscopic defects that are responsible for each one [66], [67]. For the hole trapping and the recoverable part, it is assumed that it is due to hydroxyl E' center created by the attachment of the released atomic hydrogen to strained bridging oxygen centers. In the meantime, the quasi-permanent kinetics, of the interface states, are still following a power law dependence, but there is an extra consideration. Apart from the dangling bonds in Si/SiO_2 we may have hydrogen diffusing from the gate that could create additional border traps. In both cases, the repassivation or redistribution of H is possible, but has very long recovery times.

In general, there are some parts of common agreement among the researchers, like the role of hole trapping/detrapping and the creation of defects during stress, but there is still no consensus and, most importantly, no predictive physical model that allows simulation under different circuit conditions [53].

1.4 Characterization of averaging effect

To identify and characterize the defects that cause the CMOS devices to degrade over time, we need some techniques to help us do that. In the next sections, we'll see an overview of the used characterization methods in this thesis, starting with the ones that show the averaging effect of traps.

The first reliability characterization technique that has been used in this thesis, is the Bias Temperature Instability: a method to stress both N&PMOSFETs, called Positive (PBTI) and Negative (NBTI) respectively. The main ageing feature, as we saw before, is the shift of the threshold voltage with time while the transistor is on standby mode, there is no drain current flowing in the channel (V_D=0V). It is an indicator of the gate oxide quality and helps towards the optimization of the gate oxide or the channel material depending on the results each time. It can be applied in two forms: the DC and the AC that we'll describe separately.

1.4.1 DC stress

The BTI application has two different stages, the stress and the relaxation. BTI is strongly activated by temperature and so it's globally measured at 125°C. At the beginning of the technique, we perform an initial I_D-V_G to characterize the device and evaluate its V_{TH}. During stress, a high gate voltage is applied for a specific time period, followed by the measurement itself during which we observe the degradation of the transistor's parameters. The whole sequence is repeated several times over the total stress period, that's why it is often referred to Stress-Measure-Stress (SMS) or Measure-Stress-Measure (MSM) in the literature (Figure 1.13). The only difference between NBTI/PBTI is the application of negative/positive $V_{G,\,stress}$. However, once the stress stops the degraded electrical characteristics tend to return in their original state, called relaxation.

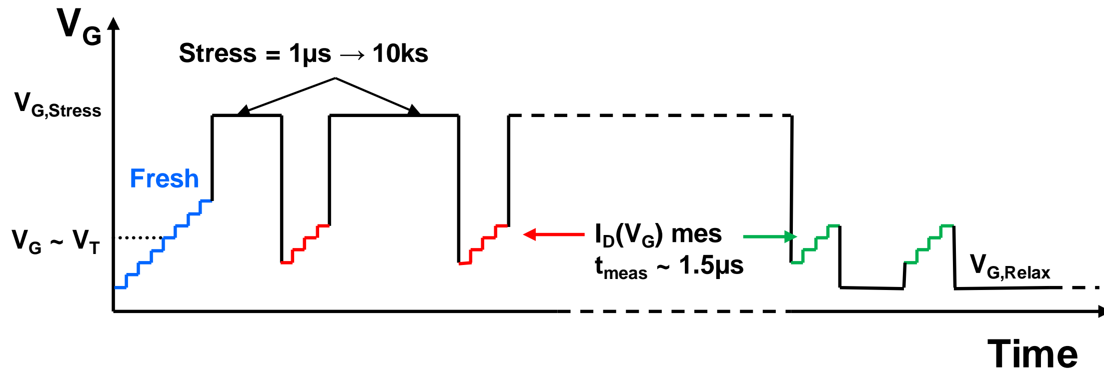


Figure 1.13 Time chart of the applied gate voltage during an DC BTI stress.

Depending on the stress time, the degradation is not the same each time and since the recovery is quite strong, it is possible to overestimate/underestimate the reliability/degradation as it is evident in Figure 1.14. Due to that, it is suggested, if not imposed, to use a fast measurement methodology to limit the relaxation and along with a shorter measuring time after stress (fewer I_D-V_G points for example) we can have a clear aspect of the actual degradation.

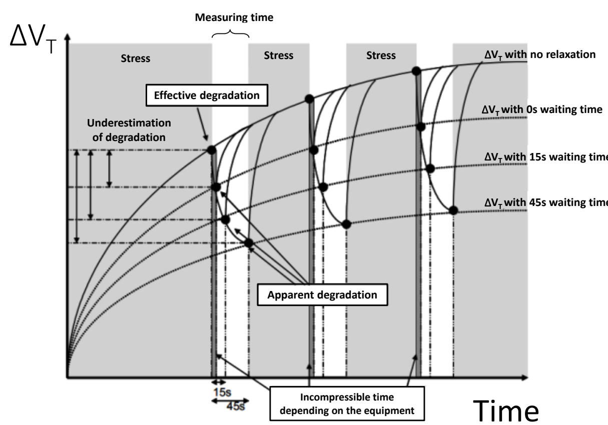


Figure 1.14 Impact of BTI relaxation in the final degradation level, reproduced from [68].

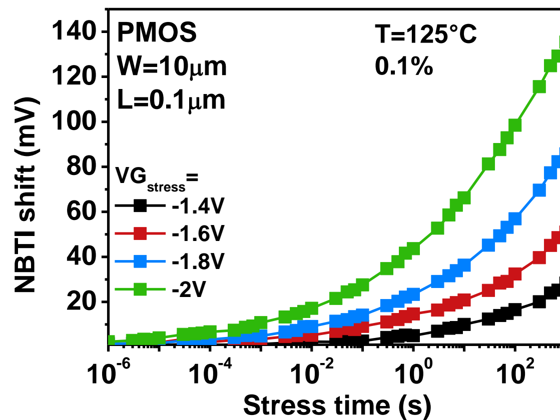


Figure 1.15 Threshold voltage drifts with time for different $V_{G,\ stress}$ during a fast range NBTI.

The difference between conventional and fast range methodology lies in the measuring tools. Typically, the $V_{G,\ stress}$ is applied through a System Measuring Unit (SMU) which, unfortunately, has settling time in a millisecond range. So, in our case, it has been replaced by a Waveform Generator Fast Measuring Unit (WGFMU) connected to a Remote-sense and Switch Unit (RSU), placed in a B1530A Keysight module. An extra advantage is that we are able to watch the degradation for over 9 decades of time, from 1μs to 1ks (Figure 1.15). However, there is a trade-off between accuracy and speed. For a device with a large width (common in BTI measurements) we reach a current range of 100μA which means we can have an accuracy/speed of 1μs in our results. On the contrary, if we move to smaller gate width, like in the case of nanowires (used in TDDS measurements in next section), we acquire an I_D~10μA which forces us to measure with a speed of 100μs.

As a result of the two aforementioned advantages, we are able to extract the real lifetime for our devices using this fast range methodology. The reliability criterion, in CMOS technology, is to establish a V_{TH} shift of 50mV after a 5-year operation at the circuit operating voltage, so for a V_{DD}=0.945V in our technology (Figure 1.16). An extra consideration has to be the variability, which is enhanced in advanced MOSFETs. Just like one transistor is not identical with another one, so is their reliability. NBTI shifts differ from one device to another due to the fluctuation of the number of traps per device. Consequently, the level of degradation is not the same, so the extrapolation is better to be made within a 3-sigma deviation (3σ) in order to include the variability and have rock evidence about the reliability each time. By measuring the ΔV_{TH} through a range of $V_{G,\ stress}$ and scaling it to the supply voltage, it is possible to extract the shift at 5 years lifetime and also the Time-To-Failure for the 50mV criterion (Figure 1.16 & Figure 1.17).

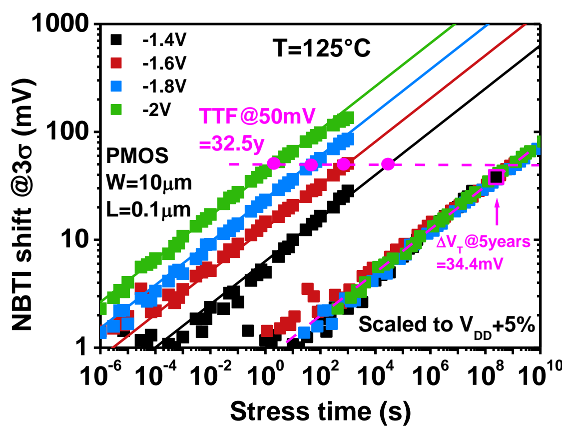


Figure 1.16 Log-log plot of Figure 1.15 scaled at V_{DD} to extract the V_{TH} shift after a 5-year operation.

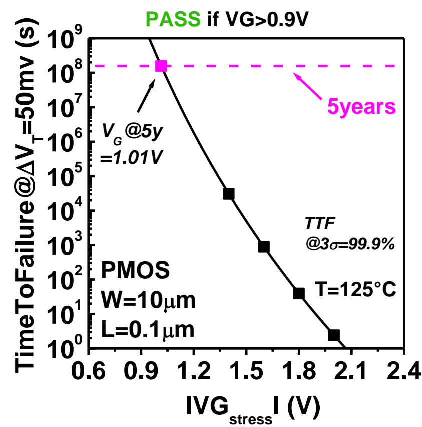


Figure 1.17 Demostration of successful technology validation, reaching and exceeding the reliability criterion for a V_G>0.9V.

Using the following power law model (Eq. 1.5), we can estimate the maximum applied voltage, in order not to pass the ΔV_{TH}=50mV, and which has to be higher than the supply voltage in order to validate each technology.

$$\Delta V_{TH}(t, V_G, T) = C \cdot V_G^{\gamma} \cdot e^{-\frac{E_a}{kT}} \cdot t^n \qquad \text{Eq. 1.5}$$

where:

- C: a constant depending on the technology, specifically on the gate stack
- T: the used temperature (125°C at BTI setups)
- V_G: the stress voltage applied at the gate
- γ: the voltage acceleration factor
- E_a: the activation energy of the generated traps
- k: Boltzmann's constant
- n: a time acceleration constant
- t: the total stress time

As a result, and as we continue scaling and reducing the supply voltage even more, it is essential to measure the degradation as fast as possible, in order to correctly evaluate the

lifetime duration of the transistors and, eventually, of the circuits. In addition to the proper equipment, it is important to understand the physical mechanisms lying behind the measured degradation and build correctly calibrated models to help us predict the behavior of our devices during long operating times.

1.4.2 AC stress

Like the name indicates, there is an alternative way to apply BTI stress in a transistor, this time using the AC method. In that case, we better reproduce the circuit operation for which the stress voltage is not applied constantly. Like a circuit oscillates between 0V and the supply voltage V_{DD}, the applied stress switches from 0V to $V_{G,\,stress}$. Again, there is a series of stress and relax events, called cycle, and the measuring principle is the same, a Measure-Stress-Measure sequence, recording the I_D-V_G characteristic to extract the V_{TH} shift, similar to the DC BTI (Figure 1.18).

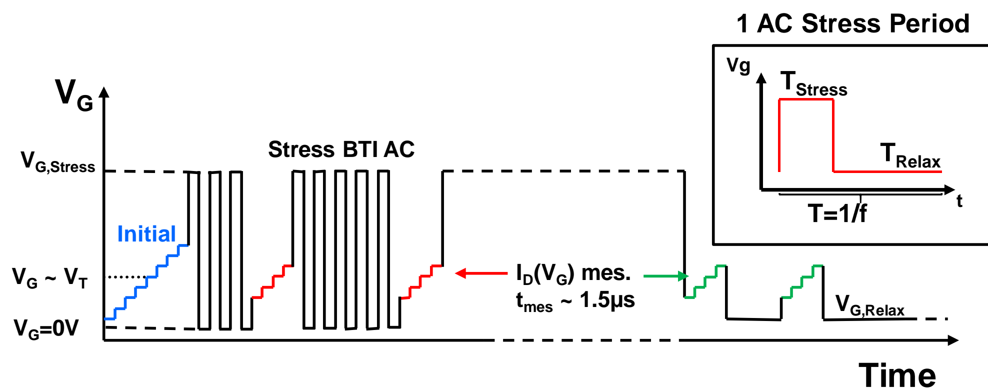


Figure 1.18 Time chart of the applied gate voltage during an AC BTI stress with the inset showing a single period of it, taken from [69].

Using the AC technique, we have to identify two parameters: the frequency and the Duty Factor (DF), described by:

$$f = \frac{1}{T} \qquad \text{Eq. 1.6}$$

$$DF = \frac{T_{stress}}{T_{stress} + T_{relax}} \cdot 100\% \qquad \text{Eq. 1.7}$$

The frequency is describing the operation speed of the circuit while the duty factor reveals the percentage of the period that the circuit is “on”. For example, during a 10% AC BTI application, the transistor is stress during 10% of the defined period and the rest 90% is under relaxation. We can perform tests from a duty cycle of 1% up to 100% (Figure 1.19), with the maximum percentage being the DC BTI that we saw before, and over a wide range of frequencies from 100Hz up to 1MHz. Each time the AC degradation will be lower than the DC one. This is due to the fact that the end of AC signal has a 0V state which means relaxation. So again in this type of measurement, it is necessary to have a fast range setup to avoid any

relaxation phenomena. In our case, we have used a previously developed fast methodology, operating under the "Arbitrary VG Pattern" (AVGP) method, described in details in [70].

The best way to exploit AC BTI data, is to build the Capture and Emission Time (CET) maps [71] (Figure 1.20). Using this method, we can identify two trap populations, the permanent and the recoverable. The first one has a very high emission time compared to the capture ones and is related to the interface traps while the latter experiences a strong correlation between capture and emission and is mostly due to the traps deeper in the oxide.

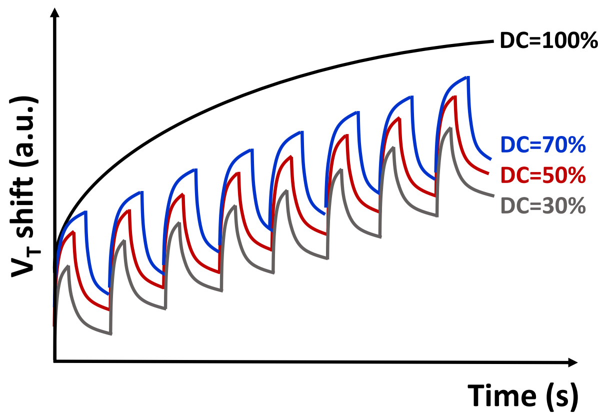


Figure 1.19 . Illustration of a PMOSFET V_{TH} degradation under DC and AC stress conditions.

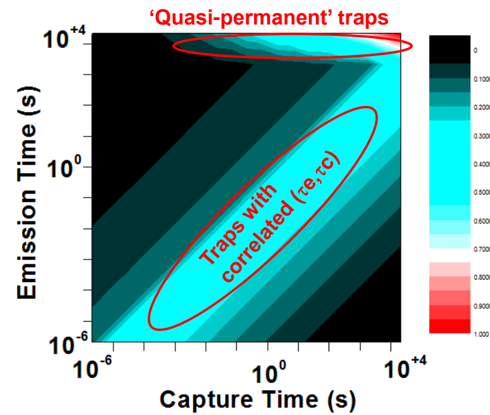


Figure 1.20 CET map revealing the two populations according to their time constants [70].

Of course, the next step is to have a model that is able to describe the experimental results and predict the degradation for AC and AVGP stress. The model that has been used to reproduce the V_{TH} shift in combination with the CET maps, is the RC model [70], [72] (Eq. 1.8).

$$\Delta V_{TH}(t) = K \cdot \sum_{i=1}^{N} g(\tau_c^i, \tau_e^i) \cdot U^i(t) \qquad \text{Eq. 1.8}$$

where K is a technological constant, $g(\tau_c, \tau_e)$ the local density of capture and emission time constants and U the voltage after n stress cycles: all of them individual parameters for each "i" trap. In this model, each trap can be seen as a lumped RC element with given resistance and capacitance. Taking the local trap density extracted from Figure 1.20, we are able to successfully fit our data, like the ΔV_{TH} recovery for different AC stress periods, the normalized stress and recovery for different frequencies or w.r.t. the duty factor.

1.5 Characterization of individual defects

Besides the characterization methods used for large devices to record the averaging effect of traps, as we move on to deeply scaled devices, we are witnessing the impact of only a handful of random defects. For that, it becomes imperative to have reliable techniques to characterize the individual traps.

1.5.1 Random Telegraph Noise – Low Frequency Noise (stationary method)

One of the first applied techniques for trap detection method is the Random Telegraph Noise (RTN), a method suitable for small gate areas. When a trap inside the oxide randomly captures and emits a carrier from the conduction channel, it causes a fluctuation of the electrical parameters of the transistor, especially in the drain current. This appears like discrete switching between two current levels in the time domain. Two current levels correspond to one trap, four levels to two traps etc. Each trap has three specific characteristics that make it unique: the capture time constant τ_c, the emission time constant τ_e and the drain current variation ΔI_D that eventually has an impact on the threshold voltage. These type of fluctuations have been observed for quite some time and are evident in devices with surface smaller than $0.1\mu m^2$ [73], [43], where it is easier to be detected due to the smaller existing number of traps.

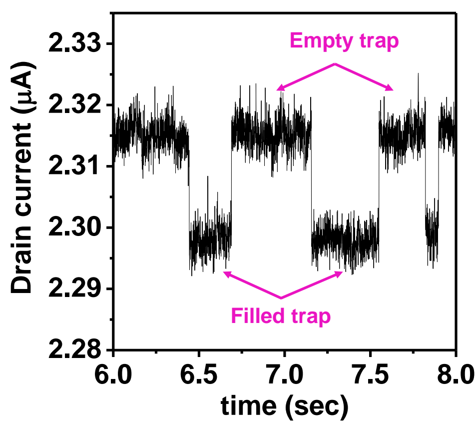


Figure 1.21 RTN of a FDSOI PMOSFET transistor during a $V_{G,\,bias}$ of -0.5V.

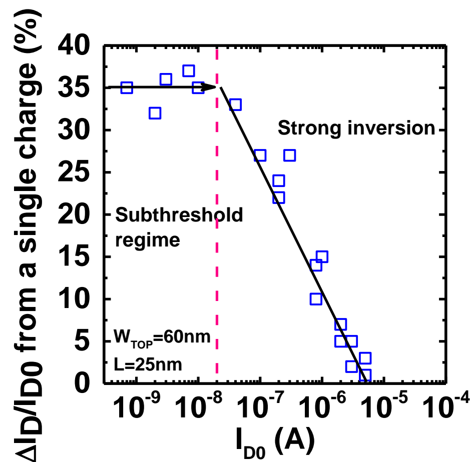


Figure 1.22 Impact of a single trap in the drain current

The usually applied gate voltage is part of the subthreshold region. Figure 1.22 shows the reason for this choice. Applying different gate bias on a MOSFET, we can identify two different zones of the trap. The left part in which the impact on the drain current reaches a maximum and constant value and the right part during which this effect decreases with the increasing operating drain current. The decrease in the strong inversion regime results from the screening of the oxide layer by mobile carriers of the inversion layer [43]. It is therefore related to the current flowing across the transistors through the equation [74]:

$$\frac{\Delta I_D}{I_D} = \frac{G_m}{I_D} \cdot \frac{q}{W \cdot L \cdot C_{OX}} \qquad \text{Eq. 1.9}$$

During the bias application, we keep the device in quasi-thermal equilibrium and we see the multiple captures and emission of the same defect. This means that we can see and detect only a small portion of the existing oxide traps, depending on the setup each time, like the bias conditions and the experimental measuring window. Figure 1.23 shows the current transients of the same PMOSFET, having a constant sampling time, but a different applied gate voltage. It

is obvious that the number of detected traps is directly related to the applied V_G and such, we can see from zero up to two current fluctuations.

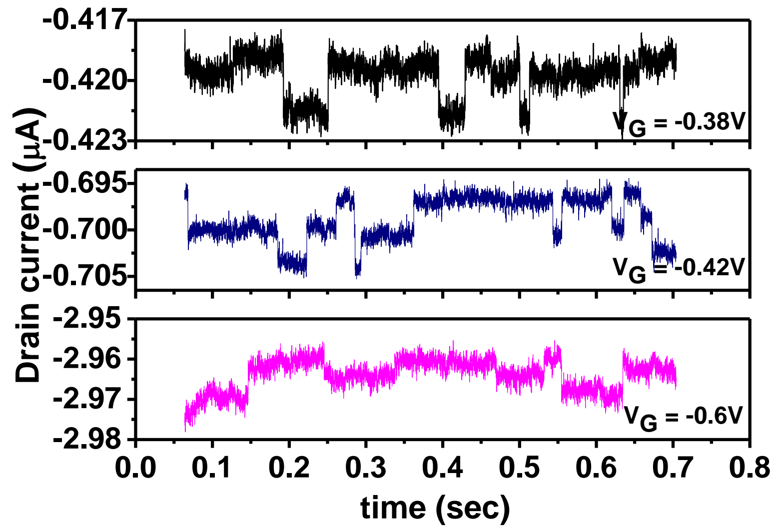


Figure 1.23 Current fluctuations of one transistor under different bias application.

Besides the voltage, it is also the experimental window that affects our results. In Figure 1.24, it is evident that the sampling rate plays an important role in the measurements. We can see that, under a fixed pair of (V_G, V_D) there are some differences: in the first "window", there is no discrete switching visible while one the second and the third one, there are two and even four witnessed current levels, meaning that we have slower traps. In addition to that, the need of a large number of points [75], like here the selected 20.480, makes it more complicated to analyze the data after, especially when it comes to the determination of their characteristic capture and emission times.

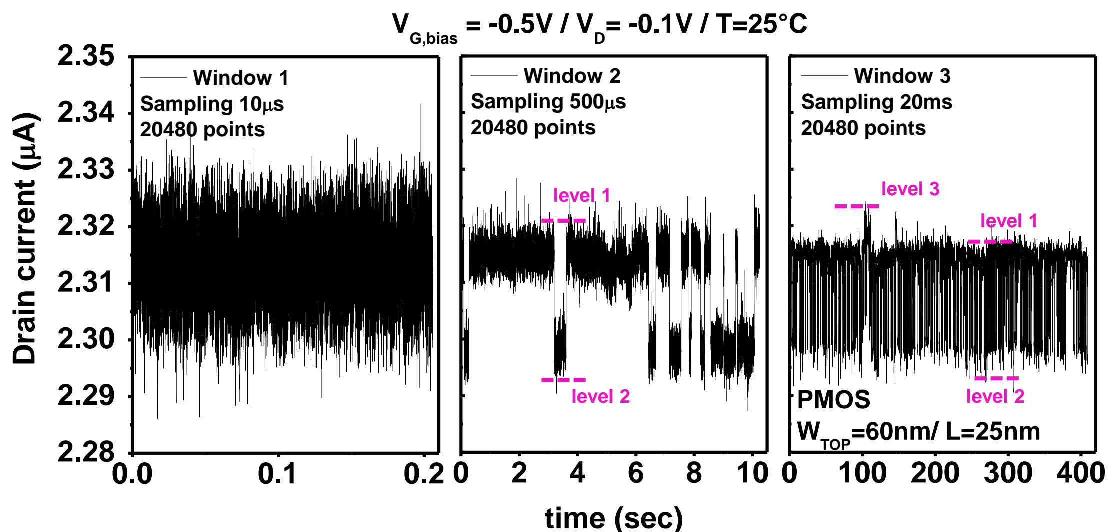


Figure 1.24 Three experimental measuring windows with different sampling rates showing the complexity of RTN method for trap detection.

A relatively easier way to exploit the RTN data is to construct the drain current histograms (Figure 1.25) [76]. Even with a first glance, we can be more confident on the current fluctuations that have been measured and the existence (or not) of a defect. If we observe window 1, we see that the current is drifting around a specific level; one that is directly illustrated on the left histogram (~2.31μA). On the contrary, in the two other windows/histograms, there are two or even three different I_D levels, showing a series of capture/emission events that correspond to one or two traps respectively.

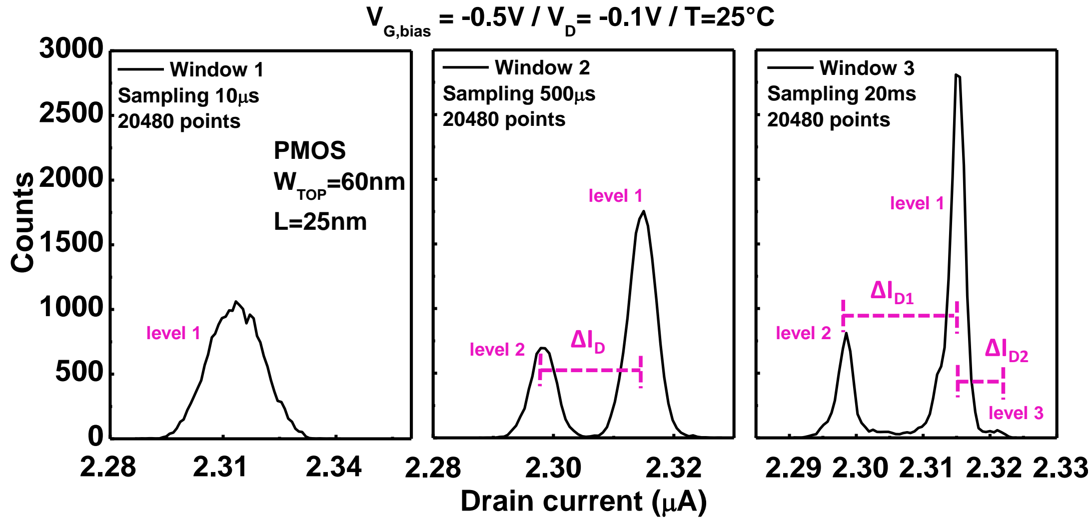


Figure 1.25 Respective drain current histograms of Figure 1.24.

Now, we also have the option to switch from the time domain to the frequency domain and use the Low Frequency Noise as a diagnostic approach for the detection of defects. To do so, we take the raw data of I_D-t and use Welch's method [77] to make this transformation resulting to use the Power Spectral Density (PSD [A^2/Hz]) as a tool.

The method is based on the following concept: The original time signal is split in 1024 overlapping subparts, in our case, defining like this the averaging in the calculating periodograms, an important factor that reduces the variance of the individual power spectral results. Then, these overlapping segments have a window applied to them, in the time domain: we selected the Hanning window which is most commonly used in noise analysis due to its good frequency resolution.

After, we take the difference between the timestamps:

$$\Delta T = t_2 - t_1 \qquad \text{Eq. 1.10}$$

and calculate the minimum and the maximum frequency of our segment using the previously mentioned number of points per window (here 1024):

$$f_{min} = \frac{1}{\Delta T \cdot 1024} \qquad \text{Eq. 1.11}$$

$$f_{max} = \frac{1}{\Delta T}$$ Eq. 1.12

continuing with their difference, which will serve as our sampling frequency in the PSD:

$$\Delta f = \frac{f_{max} - f_{min}}{1024}$$ Eq. 1.13

The corresponding periodogram (PSD) is calculated for each window using Fast Fourier Transform (FFT) and finally, we average the calculated periodograms, with the previous value.

$$PSD = \frac{FFT^2}{\Delta f}$$ Eq. 1.14

The PSD shape of RTN has a $1/f^2$ dependence, called Lorentzian and as we scale down we experience a strong noise dispersion (Figure 1.26). The PSD is described by [78]:

$$S_{ID} = 4 \cdot A \cdot \Delta I_D^2 \cdot \frac{\tau}{1 + (2\pi f)^2 \tau^2}$$ Eq. 1.15

where ΔI_D is the average RTN amplitude (Eq. 1.9), τ is the time constant of transitions given by:

$$\tau = \left(\frac{1}{\tau_c} + \frac{1}{\tau_e}\right)^{-1}$$ Eq. 1.16

with τ_c and τ_e, the capture and emission time, respectively and A the space mark ratio described by:

$$A = \left(\frac{\tau}{\tau_c + \tau_e}\right)$$ Eq. 1.17

This method can be applied on both large and small area devices with the difference lying on the shape of PSD. On larger transistors, there is an increased number of traps, each one with a distinguished Lorentzian spectrum. As they are averaging, the new spectrum will fit the $1/f^\gamma$ form, the so-called flicker noise (Figure 1.27). Depending on the γ value, we can identify the position of the traps in the oxide ($0.7 < \gamma < 1.3$) [79]. For a value lower than 1 the traps are located near the interface while when the value is higher than 1 the traps are positioned deeper in the oxide. If γ=1, then we have a uniform trap distribution near the interface.

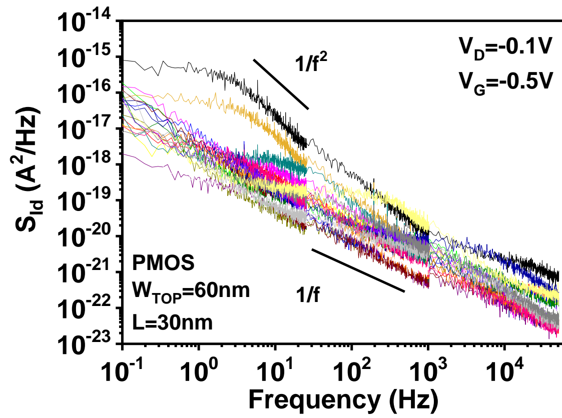


Figure 1.26 Strong PSD dispersion in deeply scaled transistors, here showing Trigate PMOSFETs.

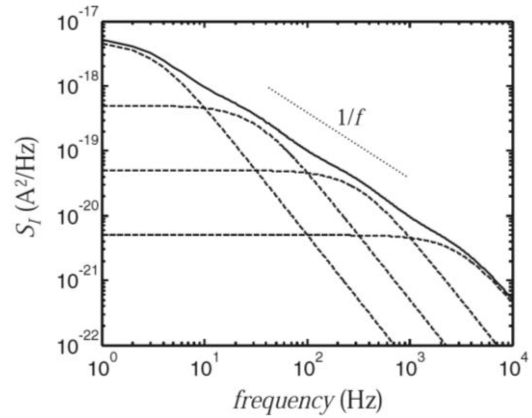


Figure 1.27 Superposition of Lorentzian spectra creating a 1/f dependence on a large device [80].

Even after all the years of LFN studies, there is still a debate regarding the physical mechanisms that are responsible for the origin of flicker noise in semiconductors, especially in MOSFETs where the PSD spectrum is a combination of Lorentzian and flicker. There are two major "schools": the Carrier Number Fluctuations (CNF) and the Hooge Mobility Fluctuations (HMF) [81]. But, it seems that a combination of both (Carrier Number Fluctuation/ Correlated Mobility Fluctuation-CNF/CMF) is more suitable to describe this more complex PSD (Eq. 1.18 [82], [83]).

$$S_{Id} = g_m^2 \cdot S_{Vfb} \left(1 \pm \alpha_{sc}\mu_{eff}C_{ox}\frac{I_d}{g_m}\right)^2 \quad \text{Eq. 1.18}$$

where μ_{eff} is the effective mobility, α_{sc} the Coulomb scattering coefficient and S_{Vfb} the flatband voltage that is described by (Eq. 1.19) if the carrier trapping-detrapping takes place through a tunneling process:

$$S_{Vfb} = \frac{q^2\lambda kTN_t}{f^\gamma WLC_{ox}^2} \quad \text{Eq. 1.19}$$

with N_t being the oxide trap surface state density.

To have a complete study, it is necessary to perform the noise measurements in a large range of $V_{G,\,bias}$, always at a small V_D and, at least, one decade above the equipment noise level. In that way, we can extract some useful information regarding the oxide/channel interface properties. Plotting the normalized PSD w.r.t. the drain current for a specific frequency, usually at 10Hz, and fitting the data with the CNF/CMF model, we are able to extract the two major parameters: N_t and the correlated mobility fluctuations factor, $\Omega = \alpha_{sc}\mu_{eff}C_{ox}$ [84]. The first one indicating the quality of the oxide depending on different technological aspects, like the various processing steps [85], or the impact of electrical stress and the second one to characterize the scattering rate induced by the interface charge fluctuations.

1.5.2 Time Dependent Defect Spectroscopy

Another technique, very similar to RTN and also qualified for small area transistors, like the Trigate nanowires in this thesis, is the Time Dependent Defect Spectroscopy (TDDS) [86], [87]. Several studies have shown that the recoverable component of BTI degradation and the Random Telegraph Noise (RTN) are caused by the same oxide defects having a match between their extracted characteristics, like the carrier-emission constants or the characteristic step height. Even though TDDS and RTN study the same phenomenon [87]–[89], there are still some differences between them. Just like BTI, the TDDs technique is also divided in two parts, the filling (called stress in BTI) and the recoverable.

To begin with, the basic difference with RTN is that the TDDS method is identified as a transient effect (Figure 1.28). We apply a high enough charging gate voltage ($V_{G,\ charge}$) in order to fill the traps and have an almost 100% occupancy of them, but without stressing our device. So, for a single-channel transistor the usual value for N/PMOSFETS is ±1.2V, respectively, in order to charge in strong inversion and characterize the pre-existing defects without creating new ones. The filling time is set to 10s in all our tests during which we do not make any drain current measurements. After that we switch to a lower discharging voltage ($V_{G,\ relax}$), choosing a value close to the threshold voltage and recording directly the relaxation drain current transient for a period of 11sec using 3.000 timestamp points. During that time, the filled traps are emptying and we can measure the carrier emissions from single defects that appear as steps. Considering that we are in linear operation and the current degradation is due to the V_{TH} degradation [90], we transform the ΔI_D into ΔV_{TH} as shown in Figure 1.29. We perform an initial I_D-V_G measurement, before the filling of the traps and compare it with the recorded jumps after the relaxation part (ΔI_D (n)). Like that, we can obtain the equivalent V_{TH} shift of a single defect (ΔV_{TH} (n)).

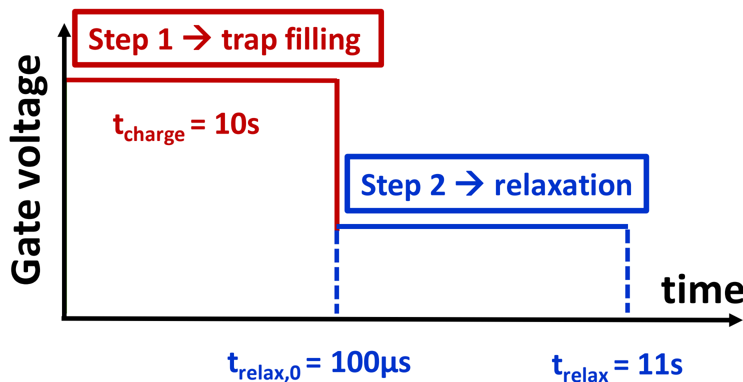


Figure 1.28 Experimental setup of Time Dependent Defect Spectroscopy.

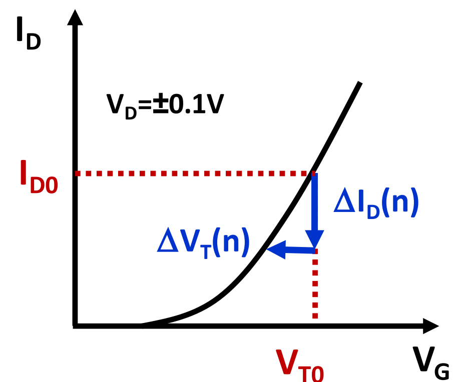


Figure 1.29 Transformation of individual ΔI_D jumps to a V_{TH} shift.

There are two attention points in this method: Firstly, in order to be sure that we are measuring above the equipment noise level, the minimum step height limit is set to 1mV. After that, depending on the measurement conditions, we can set it to 2 or 2.5mV, but always keeping in mind the 1mV minimum limitation. Secondly, when there is a comparison between different geometries, it is advisable to choose the $V_{G,\ sense}$ correctly so that the same current level is reached each time, hence the same oxide field. The fact that TDDS is applied in deeply

scaled devices, makes it understandable that the variability, even between the same geometry transistors, is increased (Figure 1.30). For this reason, it is an imperative need to acquire a statistical interpretation of the results, using a minimum of 60 tested devices each time.

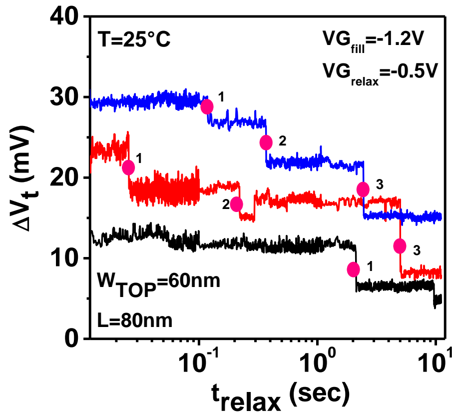


Figure 1.30 Typical TDDS relaxation transients of different devices having the same geometry.

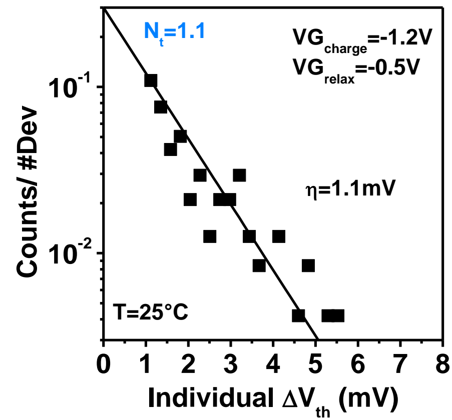


Figure 1.31 Histogram of the recorded jumps after applying the TDDS method on 60 devices.

So, now the question is how we can obtain some useful information from this procedure. The first “easy” statistical representation of these steps is to plot their histogram (Figure 1.31) from which itis clear that they follow an exponential law and we’ll see now what kind of parameters can help us characterize their impact on a decananometer device. In this direction, we use the above results and plot two different figures, the Cumulative Distribution Function (CDF) of the total V_{TH} shift per device measured just after the filling step and the Complementary Cumulative Distribution Function (CCDF) of the individual steps (Figure 1.32). We’ll look at both separately regarding the qualitative information that we can extract from them and then make a comparison of the parameters.

Starting from the Cumulative Distribution of the total ΔV_{TH}, measured at the first relaxation point, fitting the raw data with the Defect Centric Model (DCM). The DCM was, firstly, introduced by in 2010 [91] in order to obtain the needed statistics for deeply scaled devices and it is based on two assumptions. Firstly, that the ΔV_{TH} distribution of individual devices is exponentially distributed. And secondly, that the mean number of defects that are present in the gate oxide is Poisson distributed (Eq. 1.20 - Eq. 1.22).

Combining both distributions, the number of traps and the impact of each one of them, we conclude to these forms allowing us to express the two parameters in terms of mean value and variance and have a technological or geometrical independent calculation of them.

$$F_n(\Delta V_{th},\eta) = \sum_{n=1}^{\infty} \frac{e^{-N} * N_{trap}^{n}}{n!} * \left[1 - \frac{\Gamma(n, \frac{\Delta V_{th}}{\eta})}{(n-1)!}\right] \quad \text{Eq. 1.20}$$

with η being the average V_{TH} shift from a single defect, equal to:

$$\eta = \frac{\sigma\Delta V_{th}^{2}}{2 * mean\Delta V_{th}} \qquad \text{Eq. 1.21}$$

and N_T, the average number of charged defects calculated from:

$$N_{Trap} = 2 * \left(\frac{mean\Delta V_{th}}{\sigma\Delta V_{th}}\right)^{2} \qquad \text{Eq. 1.22}$$

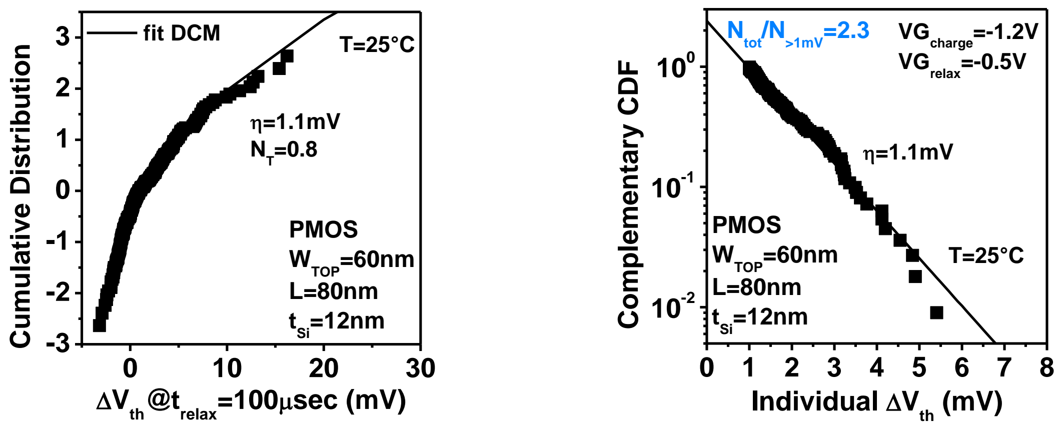


Figure 1.32 (left) CDF of the total V_{TH} shift per device at the first relaxation point and (right) CCDF of all the recorded individual steps.

At the same time, there is the CCDF plot, constructed using the carrier emissions from single microscopic defects and as the histogram before, it appears exponentially distributed. It originates from the random position of the trapped charged in the gate oxide, an observation already made on FDSOI devices [92]–[94]. Fitting the data helps us extract two parameters: the reverse of the slope gives us the η parameter and as presented by many works, the N_T is considered to be the intercept with y-axis. Experimentally, it is also necessary to fix a threshold on ΔV_{TH}^{ind} to distinguish a true emission event from the system noise level. It is fixed to 1mV in all our experiments. Such a threshold implies that the defects with ΔV_{TH}^{ind} below 1mV cannot be detected properly by the technique. In order to know how this limitation can affect the extraction of the trap parameters, we simulate the ΔV_{TH}^{ind}s of 10.000 defects exponentially distributed through a Monte Carlo drawing. Amongst the 10^4 traps, only the $N_{>1mV}$ defects, which exhibit a V_{TH} shift above 1mV, can be detected experimentally. The histogram and CCDF of the total number of defects N_{tot} are then compared to the ones of detectable traps $N_{>1mV}$ in Figure 1.33. For the simulation, η is fixed to 1.1mV. We first notice that both histograms are very similar and lead to the same η extraction. This proves that the method is effective to

extract η even if some trapping events cannot be recorded experimentally. Once η has been extracted, N_{tot} can also be easily deduced from the y-intercept of the same histogram, which is simply given by $N_{tot}.dV_{TH}/\eta$ where dV_{th} represents the class of the histogram. Looking now at the CCDFs, we note that both N_{tot} and $N_{>1mV}$ distributions again exhibit the same slope η. Therefore, as for PDF, measuring only a fraction of traps by TDDS does not impact the η extraction. η parameter can always be obtained by a simple fit of the measured CCDF. Nevertheless, we also observe that the two CCDFs are not identical this time, but, are shifted from a constant value along the y axis. The shift, that is directly given by the y intercept of the $N_{>1mV}$ distribution, actually corresponds to the ratio of “detectable” traps $N_{>1mV}$ over the total defect number N_{tot}, and, not to N_{tot} itself as reported in [95], [96].

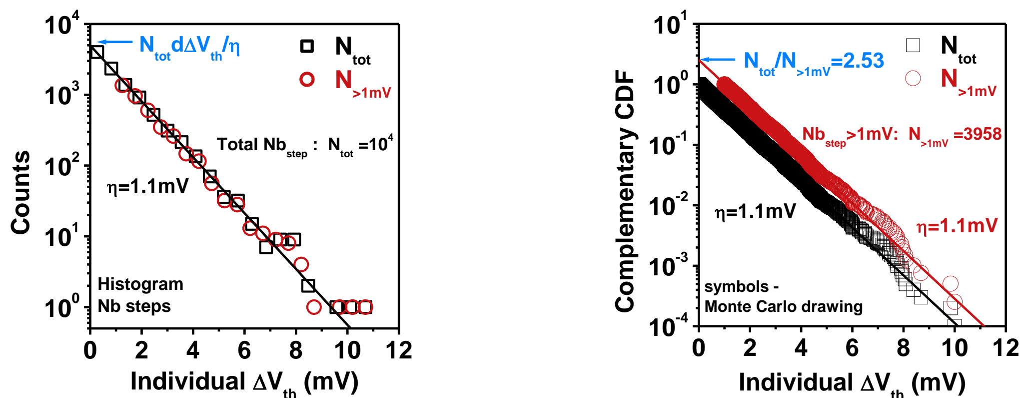


Figure 1.33 Simulated (left) histogram (right) CCDFs of a sampling of exponentially distributed V_{TH} shifts with a mean value of 1.1mV. A total number of 10.000 simulated steps is then compared to the recorded experimental results above 1mV.

Now that we have an idea regarding the parameter extraction each time, it is possible to make a comparison between them. The good news is that the η can be extracted for both distribution types. The bad news is that it is not the same for the N_T. It is an often phenomenon that there is a miscalculation or, more correctly, an overestimation of N_T when it comes to CDF. This results from the uncertainty of the fit due to a higher N_T value which leads to a computational error on the calculation of the trap number. On the other hand, the CCDF plot is direct and more accurate, but as we saw before we have a loss of information due to the minimum step height each time.

To conclude, there is no black and white for the data treatment of TDDS and in the chapters to come, we present both methods each time and compare their results. There is a question though, about if and how these results are affected. Just like in the NBTI case, there are two factors that could have an impact on the η and N_T extraction: the filling time and the temperature.

It has been already shown [69] that whatever the filling time, the average impact of a single trap does not change: a constant η value is extracted which is not the case with N_T where the number of filled traps is increasing with the filling time. From the temperature point of view, will be presented later that we acquire similar results, the η remains unimpacted while the N_T is changing, in agreement with the fact that NBTI is temperature activated. The reason for this is that when using different temperatures, having a constant measurement window, modifies

the emission time constant of each trap, since they empty faster when the temperature is increasing [96].

1.5.3 Correlation between standard NBTI tests and TDDS

Combining Eq. 1.21 and Eq. 1.22, we can easily deduce that

$$mean\Delta V_{TH} = \eta . N_{Trap} \quad \text{Eq. 1.23}$$

This makes a direct correlation between the mean V_{TH} shift measured during standard DC NBTI tests and η & N_{Trap} parameters given by TDDS. In the charge sheet 1D approximation, the same mean V_{TH} shift is related to oxide parameters and mean trap density D_{Trap} through:

$$mean\Delta V_{TH} = \frac{q.EOT}{\epsilon_{ox}} . D_{Trap} = \eta_0 . N_{Trap} \quad \text{Eq. 1.24}$$

with

$$\eta_0 = \frac{q.EOT}{\epsilon_{ox} W_{eff} L} \quad \text{Eq. 1.25}$$

η_0 represents the mean V_{TH} shift due to a single oxide charge in an ideal 1-dimensional approximation. It can be directly compared to η parameter extracted from TDDS measurements. In a 1D transistor i.e. large and wide planar device, η is very close to η_0 and scales as the reverse of the device area $W_{eff} \cdot L$. This is an important result that will be checked experimentally in the next chapter. In a 3D structure like a FinFET, η does not follow anymore this scaling because of the mitigated effects of sidewalls and top surface. This deviation from 1D model will be also further analyzed in the next chapter.

We have finished with the introduction of the trapping phenomena and the techniques that are commonly used to characterize the defects responsible for the reliability degradation. In the following chapters, we will see how all these can be applied to advanced 3D transistor architectures, to novel 3D integration schemes and to newly introduced high mobility channel materials.

Chapter 2. Impact of 3D architectures on BTI/RTN reliability

2.1 Introduction

In the first Chapter, we saw how the evolution of scaling has progressed over the past years up until today. Especially in the last decade there has been a tremendous innovation in transistor architectures and one of the best candidates to continue Moore's scaling law is the use of 3D technologies. By using Trigate or FinFETs we can achieve an improved electrostatic control, better scalability and lower variability, but meeting the reliability requirements becomes more and more challenging. Many studies have shown that BTI trapping is more complex since it takes place not only at the top surface, but also at the sidewalls (SW) of the transistor. In addition to that the different carrier mobilities due to the conduction plane enhance even more the degradation. Two of the questions that emerge is how all this is affecting the dynamic variability of nanoscaled devices and, of course, how the already known methods for trap extraction can be applied to 3D architectures.

2.2 Tested structures

For our study, we used single-channel Trigate nanowires processed on 300mm FDSOI wafers with a 145nm BOX thickness, fabricated at CEA-Leti [8]. As it is shown on the cross-sectional Transmission Electron Microscopy (TEM) image (Figure 2.1), the effective width W_{EFF} of a nanowire is defined as its perimeter $2.t_{Si}+W_{TOP}$ where t_{Si} is the silicon thickness and W_{TOP} is the top-view, while the gate stack is made of a high-k oxide (HfSiON) and a TiN metal gate.

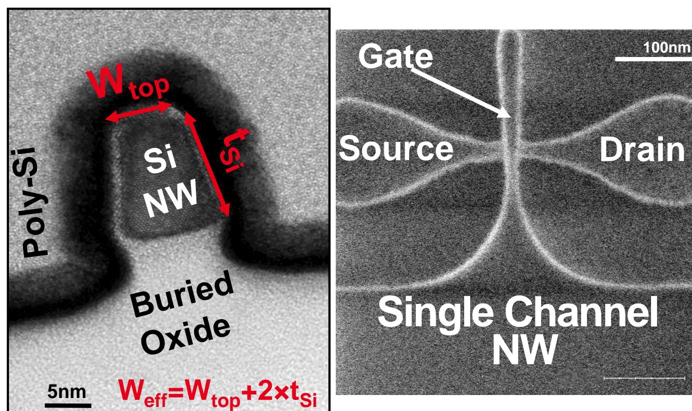


Figure 2.1 (left) Cross-sectional TEM image of silicon nanowires and (right) top view of the tested single-channel devices.

2.3 3D electrostatic simulation of the impact of one charge on V_{TH}

In order to give theoretical background on experimental results, we propose a methodology shown in Figure 2.2 to address theoretically how a single charge impacts the transistor V_{TH} [97], [98]. The technique allows us to extract the η parameter due to one single charge distributed all over the gate oxide surrounding the transistor channel. The process consists in (1) simulating using FlexPDE, a 3D finite element simulator, the impact of a charge on V_{TH} depending on its position (x_0, y_0, z_0) on the gate oxide for a given device geometry W·L, (2) randomizing this position using uniform distribution along the three axis to build the histogram of given number of transistors N and (3) finally extracting corresponding η values for the given geometry. This process is used hereafter to extract the η of different 3D transistors with different aspect ratios between t_{Si}, W_{TOP} and L.

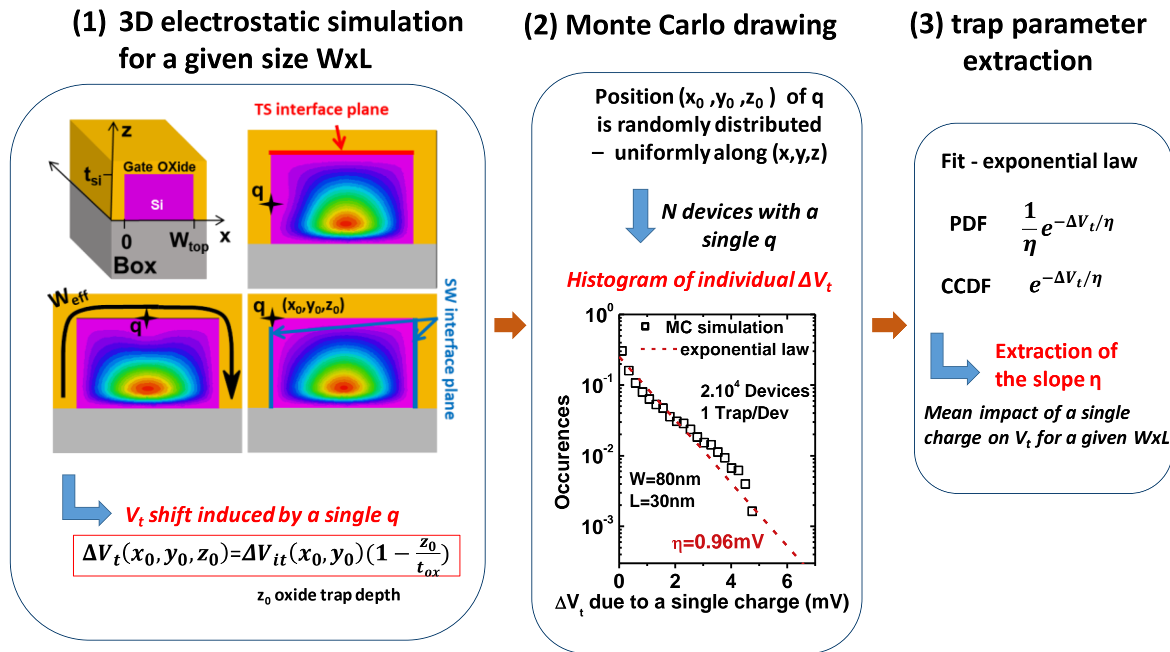


Figure 2.2 Monte Carlo process to simulate the V_{TH} shift induced by a single charge

2.4 Reliability of PMOS transistors

Depending on the tested structures we can classify our devices in three categories: ΠFETs if the ratio t_{Si}/ W_{TOP} ≈1, FinFETs if t_{Si}/ W_{TOP} >2 or Planar transistors if W_{TOP} >100nm. The goal is to see how the dynamic variability of pre-existing defects is impacted by the different geometrical aspects (top width, gate length and silicon thickness) using the TDDS method and, also, the agreement between statistical data and Monte Carlo simulations that have been conducted at the same time and are presented extensively in [97], [99].

2.4.1 Effect of top width

Since we will use Time Dependent Defect Spectroscopy as a characterization method, it is necessary to use small enough transistor area to apply this technique. We will start by looking at the difference between three top gate widths of 240, 60 and 30nm respectively. The silicon thickness is 12nm and the gate length is limited to 40nm while the applied filling voltage is modified in order to achieve the same level of current for all W_{TOP}. Performing TDDS in, approximately, 200 individual devices we plot the Complementary CDF, as usual, and using the reverse of the slope we extract the average V_{TH} shift per defect (Figure 2.3).

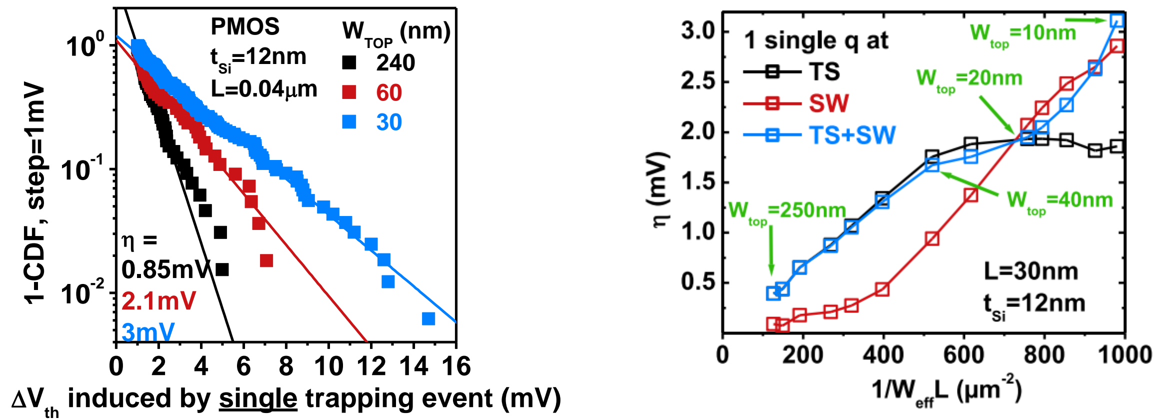


Figure 2.3 (left) Experimental Complementary CDF of W_{TOP} 60 and 30 nm, showing the impact of geometry on t_0 reliability and (right) 3D simulations of η values versus the reverse of the total device area $(W_{eff} \cdot L)^{-1}$ for variable top width W_{TOP} and a fixed t_{Si}.

It is clear that as we decrease the W_{TOP}, the η value increases in agreement with the qualitative law that wants it reversely proportional to the total transistor area. This is in agreement with the scaling law established in 1.5.3 for η_0 and recovered here using the MC simulation process described in 2.3. Indeed, we notice that η_{TS+SW} increases linearly with the reverse of the area till W_{TOP}=40nm before saturating and increasing again for the narrower widths. The inflexion occurs for W_{TOP}~20nm. Basically, in these 3D devices, the scaling of the total η is similar than the one observed for pure 2D planar devices until the effect of the sidewalls, SW, remains negligible w.r.t. the impact of the top surface, TS. However, for the narrower devices, both contributions of SW and TS must be considered to explain the behavior of η. This makes the scaling of Dynamic Variability (DV) more difficult to predict for these specific Trigate nanowire devices compared to their planar counterparts.

2.4.2 Effect of gate length

In the same way, we will compare now different gate lengths of transistors with a constant top gate width and silicon thickness, of 60nm and 12nm respectively. Three different gate lengths were tested, this time, L=80/50/30nm under the same conditions and on over 100 devices. Figure 2.4 shows the CCDF for all of them, with a common extracted η=1.1mV for the main part of the distributions. But, for the band tail, the effect of scaling is more obvious: shorter channel lengths exhibit higher η values. In addition, MC simulations were also performed to address the impact of L scaling on η. Like for W_{TOP}, η is expected to increase linearly when L is scaled down, for a value down to 10nm. The mismatch between simulations and experimental data on the main distribution part might be explained by uncertainties on the experimental η extraction due to sensitivity (η values are very low in this domain) combined with uncertainties on true device gate lengths.

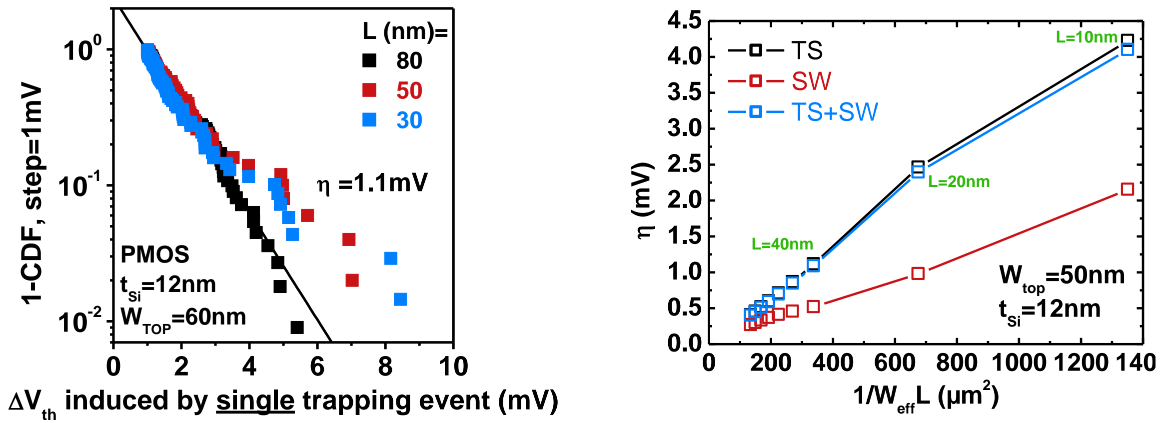


Figure 2.4 (left) Complementary CDF of different gate lengths showing a common slope for a given W_{TOP}=60nm and (right) Simulated variation of η versus $1/W_{eff}\cdot L$.

2.4.3 Effect of Silicon thickness (Height - H)

The last part of the geometry evaluation on t_0 reliability, with the help of TDDS, is the silicon thickness consideration of 12 and 23.9nm. Since we saw that the gate length has a uniform behavior, we tested two different top gate widths in order to see if indeed it is the most dominant dimension impacting the dynamic variability. For this reason, we selected wider PMOSFETs of W_{TOP}=60nm and narrower ones with a W_{TOP}=30nm. With a first glance at the threshold voltage distributions (Figure 2.5) of all devices, it seems that there is an impact of the silicon height on the larger W_{TOP}, while the narrowest one remains unaffected. Due to that, it is necessary to adjust the $V_{G,\ sense}$ of TDDS to sense at the same level of current for a direct comparison.

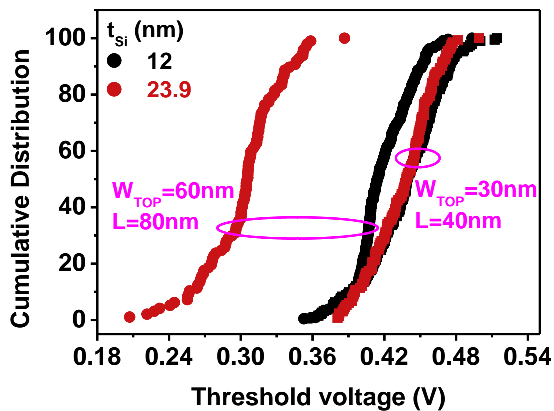


Figure 2.5 Cumulative Distribution of threshold voltage for the different structures.

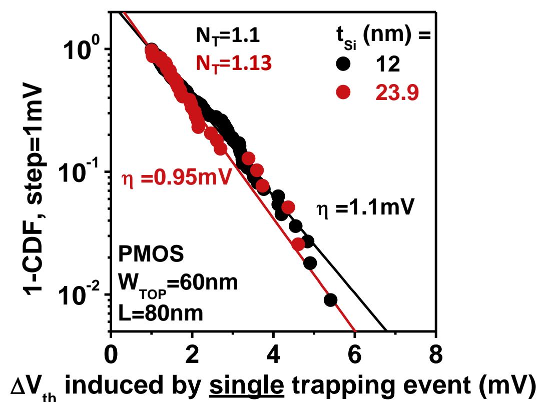


Figure 2.6 CCDFs of two t_{Si} on wide PMOSFETs reveal an almost equal η value.

For the wider transistors (Figure 2.6) we see that there is no impact of the t_{Si}, on t_0 reliability, and we are able to extract a similar η value, around 1mV. In addition to that, the extract average number of defects per device is also the same. On the contrary, when we look at the narrower devices, at Figure 2.7, the t_{Si} impact is more dominant with an almost doubled η for the smaller height. We confirmed this effect by performing Monte Carlo simulations on 50.000 devices, with the model developed in CEA-Leti and described extensively in [97], [100]. By placing a

single interface charge along the oxide, we extract the same ratio between the short and taller Si height which verifies our experimental results acquiring the same ratio.

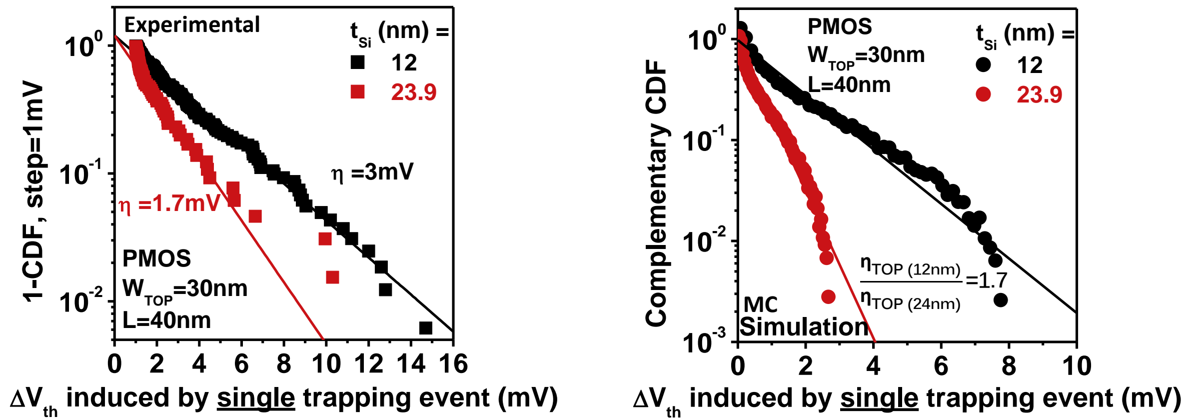


Figure 2.7 (left) The top gate width has a higher impact on the dynamic variability than the silicon thickness with an almost double η value and (right) MC simulations verify the ratio between the extracted η values.

In addition to TDDS, we performed Low Frequency Noise measurements for a range of 1Hz up 10 kHz and for various $V_{G,\ bias}$ from the subthreshold region to strong inversion, for both top gate widths and Silicon heights (Figure 2.8 and Figure 2.9). This will be used to extract the t_0 density of border traps in the several structures. For the larger PMOSFETs having a W_{TOP}=60nm and L=80nm, we plot the normalized PSD, averaged for 40 devices, for the two silicon heights. The higher PSD values for the 12nm are due to the low current that we obtain at lower $V_{G,\ bias}$ (see Figure 2.5). But, for both 12nm and 24nm we, clearly see a 1/f dependence. At the same time, we take the corresponding values at 10Hz w.r.t. the drain current and fit the data with the CNF/CMF model to extract the necessary parameters. This gives us two very close volumetric trap densities with a slight decrease of the N_t as W_{eff} decreases as well [101]. At the same time, there is a variation between the correlated mobility fluctuations factor (Ω), which is due to the different effective mobilities [102].

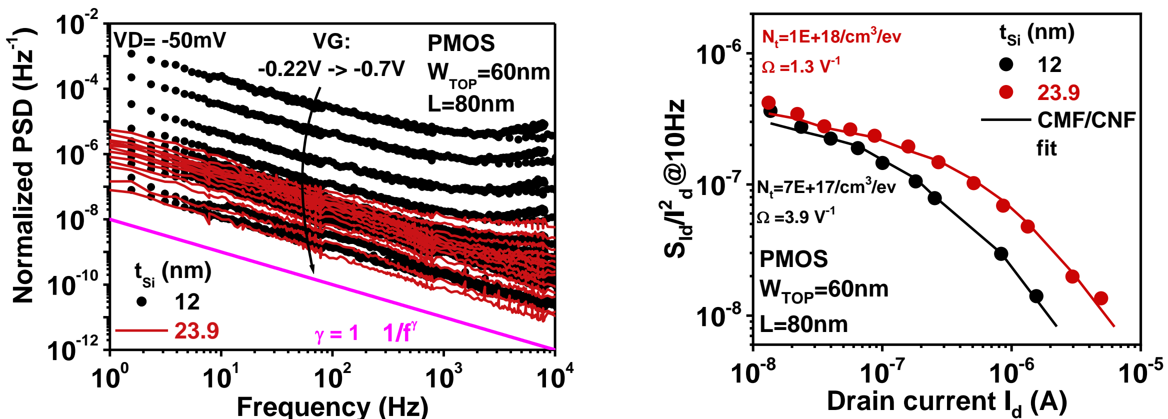


Figure 2.8 (left) Average normalized PSD of W/L=60/80nm PMOSFETs for two different silicon heights. Both showing a 1/f dependence (right) Normalized PSD extracted at 10Hz and fit with the CNF/CMF model for parameter extraction.

From Eq. 1.18, it is clear that the difference in the mobility can have an impact in the extracted factor $\Omega = \alpha_{sc} \cdot \mu_{eff} \cdot C_{ox}$ [84] that consequently impacts the drain current level noise. The fact that there are a few points that do not fit the model is due to the fact that the drain current is very low in that particular bias condition, so the normalized PSD becomes very high.

Following the same procedure for the smaller top gate width (W_{TOP}=30nm), this time we see a small variation regarding the γ exponent of the average normalized PSDs (Figure 2.9). Even though for the 12nm the value is 1, for the 24nm height we obtain a value of 0.9 that does not modify the 1/f dependence. At the same time, the volumetric trap density increases again with an increasing total width giving, nonetheless, state-of-the-art values, just like for the wide PMOSFETs. Again, the variation of the Ω factor is due to the mobility difference between the two device types and the difference in the negative or positive sign depends on the mobility increase or decrease upon trapping a charge [103]. As a general comment, if we look at each geometry individually, it is obvious that the gate oxide trap density is not significantly altered by the silicon thickness and very good Hafnium-based HK/MG values are obtained. So, it is not the number of defects that impacts the reliability. On the contrary, the difference between the Ω factor may indicate a dependence on the distance of the centroid from the interface, in agreement with the η values that suggest defects closer to the IL for the small t_{Si} and the narrower top width.

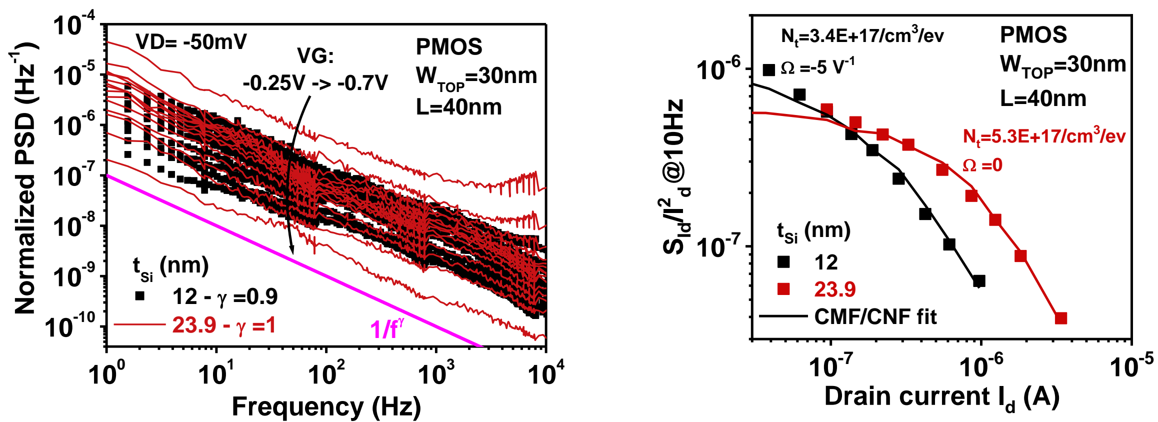


Figure 2.9 (left) Average normalized PSD of W/L=30/40nm PMOSFETs for two different silicon heights. For t_{Si}=12nm we see an exponent of 0.9 compared to t_{Si}=24nm (right) Normalized PSD extracted at 10Hz and fit with the CNF/CMF model for parameter extraction.

Closing this part, we had a first taste regarding the impact of Trigate nanowires on the dynamic variability, looking at their geometry dependence. The gate width appears to be the most important variable on the results, when the gate length shows uncertain conclusions and the silicon thickness insignificant effect. Specifically, for the gate length and due to its doubtful results, an extensive study with the most widely used trap extraction techniques will be presented in the next section.

2.5 Comparison of TDDS and RTN

We have already discussed that advanced CMOS technology is very sensitive to the generation of individual defects [104] that degrade the performance of the transistors. In addition to that, the characterization techniques that have been used, through all these years

must now be adapted to 3D architectures. This section is dedicated to a comparison between the two most popular methods for defect detection, i.e. Random Telegraph Noise (RTN) and Time Dependent Defect Spectroscopy (TDDS) measurements (see Section 1.5), applied, specifically, on short channel Trigate nanowires.

2.5.1 Setup procedure

For our goal, we used small PMOS single-channel transistors that were described in Section 2.2, with a fixed top gate width of 60nm, gate length of 50/30/25nm and a silicon thickness of 12nm. In order to make a statistical study, approximately 100 devices per geometry were tested, at room temperature, following the experimental setup of Figure 2.10.

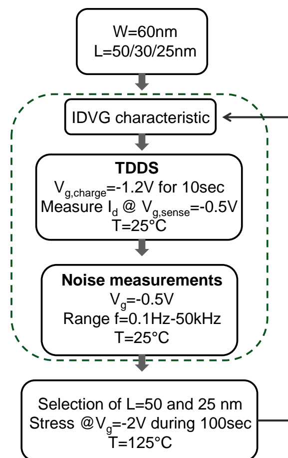


Figure 2.10 The measurement setup divided in two stages. The first describes the TDDS and noise methods for all dimensions. For the second one we select two geometries, we stress them and repeat the measurement sequence from part one.

In the first part of the study, we performed the TDDS measurements at a constant V_D=-0.1V, while we applied a V_G=-1.2V for 10 sec to fill the traps. We know that the gate voltage must be chosen to be high enough, in the strong inversion regime, in order to have a high occupancy level of the traps (almost 100%). Then, we switched to a lower $V_{G,\,sense}$=-0.5V and measured the drain current transient during relaxation with an Agilent 1530 unit, for a period of 11 seconds. Instantly after, we performed the Low Frequency Noise measurements at the same $V_{G,\,sense}$ in weak inversion, by using the same equipment and setup. The raw data of the drain current versus time are acquired by using three different "windows", each one with a different sampling rate, 1e-05s, 0.0005s, 0.02s, but with a constant number of 20480 sampling points [75]. In that way, we are able to detect the slow, as well as the faster traps. We estimated the Power Spectral Density (PSD) of the drain current by using Welch's method [77], described in Chapter 1. At the same time, with the help of a Hanning window, we obtain the PSD of the drain current SI_D (A^2/Hz) in a frequency range of 0.1Hz-50 kHz.

For the second part of the experimental setup, we selected the largest and smallest gate length (L=50 and 25 nm respectively) and stressed them under NBTI condition, at 125°C, for a $V_{G,stress}$=-2V during 100sec. Right after the stress, we repeated the TDDS and RTN measurements from part one to see the impact of stress in both cases.

2.5.2 Comparison method

It is useful to remember, at this point, that RTN and TDDS study the same phenomenon, but there are still some differences between them. The basic one is that when we talk about

RTN, we have stationary method meaning we detect multiple capture and emission events of the same defect. On the contrary, TDDS is a transient (non-stationary) method during which only the emission part is recorded.

We already know that in TDDS, the drain current variation is, usually, transformed into a voltage shift, as shown in 1.5.2, and the minimum step height for reliable results is the 1mV. Above that, we can detect a carrier emission from a single defect and be confident that we measure above the equipment noise level. However, RTN is a technique that needs a larger number of points and their transformation in voltage is more complex. So, for this study the comparison was made in terms of current for both of them, using the directly measured raw data I_D w.r.t. time, setting the minimum jump height to 10nA.

To have a more visual example of how this comparison will work, in Figure 2.11, we plot, for the same transistors, the relaxation current recorded in TDDS next to the RTN histogram created by the raw data I_D -t. It is clear that with both methods we obtain the same ΔI_D as well as the same number of traps, which is one in this case.

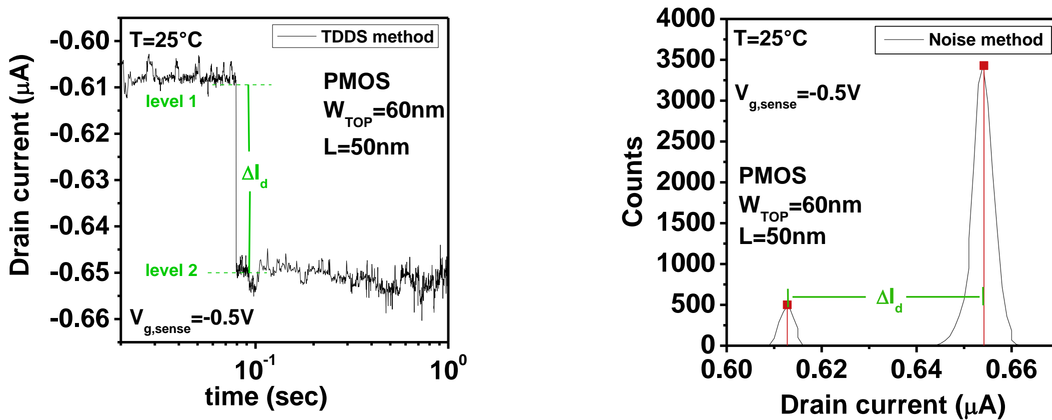


Figure 2.11 Direct comparison of the two methods for a PMOSFET of W=60nm and L=50nm. (left) For a step larger than 10nA, in TDDS, we can detect a carrier emission from a single trap. (right) The same ΔI_D is observed in the histogram of the raw current data in the noise measurements. In both cases, the trap number is one.

Regarding the RTN data treatment, we are already familiar with a method commonly used for defect identification which is the histogram of I_D [76] and was described in 1.5.1. Here, we will also apply it to the TDDS data to have a straight comparison between them so that we can divide the recorded defects in three categories (see Figure 2.12).

In Category A, we have the same number of defects detected in both methods for each transistor. Two histogram peaks correspond to one defect, three or four peaks to two defects and so on, with the noise analysis becoming more complicated if there are several traps involved that generate RTN so that there are more than two levels. Besides the number of defects, we, also, identify the same drain current level ΔI_D so that we are sure we are talking about the same traps. Category B describes the case where we have at least one defect match between the techniques but in terms of numbers, with TDDS there are more traps detected. Finally, Category C is about the carrier emissions found only in TDDS, while, at the same time, we observe no RTN fluctuations of the drain current during the noise test.

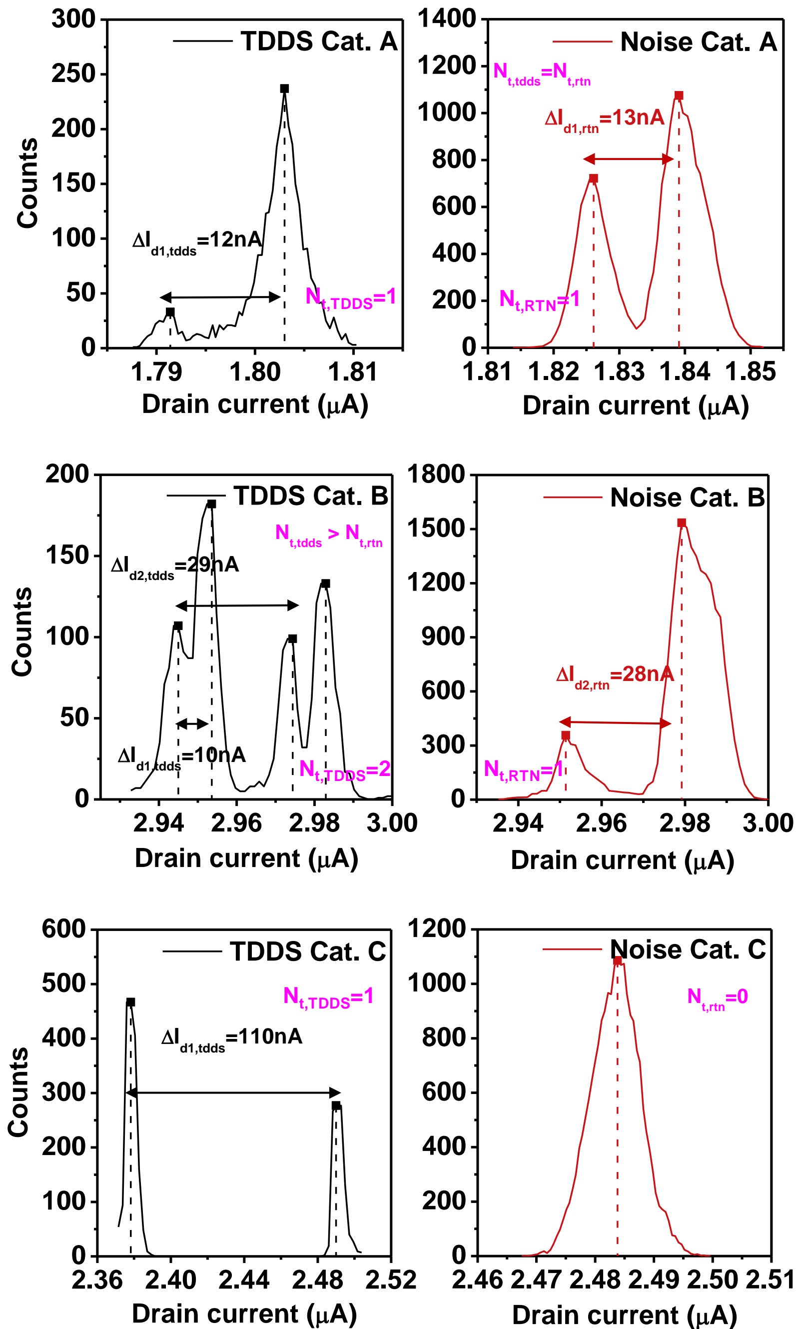


Figure 2.12 Illustration of defect categories according to the histogram, of drain current, for both measurement methods, TDDS in black color and Noise in red.

2.5.3 Fresh devices

Using the comparison method described before, we extract the individual ΔI_D steps, for both TDDS and RTN. Using that, we plot as usual the Complementary Cumulative Distribution Function (CCDF) of these data (see Figure 2.13). The CCDFs, were expected to appear as exponentially distributed.

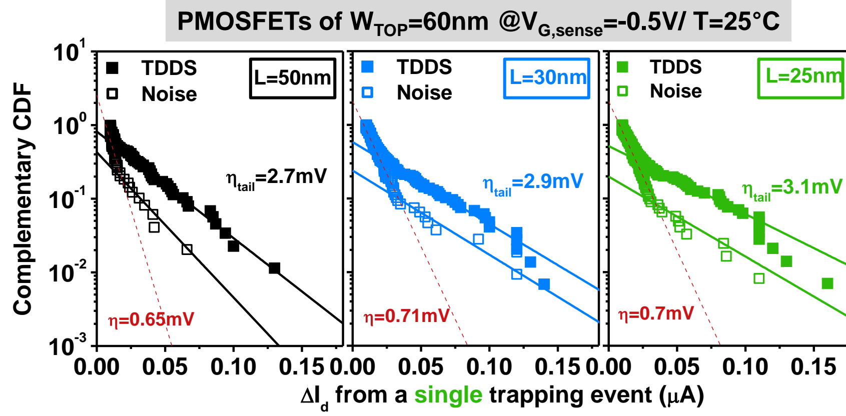


Figure 2.13 Complementary Cumulative Distribution Function (CCDFs) of individual ΔI_D induced by a single trapping event for the tested PMOS geometries. Two slopes are observed for the two types of measurements.

However, for all gate lengths, we are able to see a bimodal distribution. So far, bimodal distributions have been seen in the literature in two cases. The first one, for NMOS planar devices in which the two slopes are attributed to two different kinds of defects, those in the HK region (small η value) and the ones closer to the dielectric/channel interface (higher η) [95]. The second one, is in FDSOI transistors and is related to the traps that are present in the Buried Oxide (BOX) [92]. Our simulation studies confirm the second hypothesis (Figure 2.14) that for 3D FDSOI nanowires even a low density of defects in the BOX (~5% of the total trapping population) can have detrimental impact on the Cumulative Distribution.

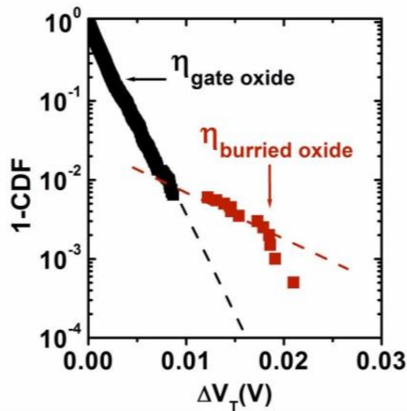


Figure 2.14 Simulation results on PMOS Trigate nanowires show the effect of defects inside the BOX in agreement with previous results on planar transistors.

Now, looking closely at Figure 2.13, and using the slopes we can evaluate the average threshold voltage shift (η) for each geometry, with the equation $\eta = \Delta I_D/g_m$, g_m being the transconductance, in order to transform it into voltage and easily understand the impact on the V_{TH}. The main part of the distribution is described by a small slope, common for both methods, and is evident for all different gate lengths exhibiting a small increase as we scale down. This is consistent with literature which predicts a scaling of η with 1/W·L in qualitative agreement. In addition to that, they have the same intercept with the y-axis, which indicates the same ratio R between the detected and the total number of recorded traps. The second slope is associated to the tail and has a higher η value for the two types of measurements. Again, as the gate length becomes shorter there is a small increase of the η tail value from 2.7 to 3.1mV. Besides that, the intercept of the tail slopes points out that there is a higher ratio of

detected traps (over their total number that exists in the gate oxide) in TDDS than in RTN. This is anticipated, since TDDS, which is a non-stationary process, is able of detecting a larger number of defects after their filling at -1.2V, whereas RTN technique detects traps under stationary condition and is limited by the setup conditions each time.

We want to move on and make the correlation between the detected traps of both techniques, in each of the 100 tested PMOSFETs. In the CCDFs, we see that the majority of the individual trapping events have a step height, ΔI_D, smaller than 30nA. Almost 70% of the TDDS and 90% of the noise results are included in this part. Making the comparison per device, we notice that there is a global agreement for all geometries (see Figure 2.15). Having an exact match between the two methods is higher than 55% which slightly increases with the device scaling. The part where we have more traps with TDDS, has no clear trend/variation with the tested geometries. Finally, the last category of having no match of the techniques is decreasing as we move on to shorter gate lengths. The results of the correlation are verified by calculating the effective trap density per geometry, as shown in Table 2.1, and indicate the global agreement between the tested gate lengths.

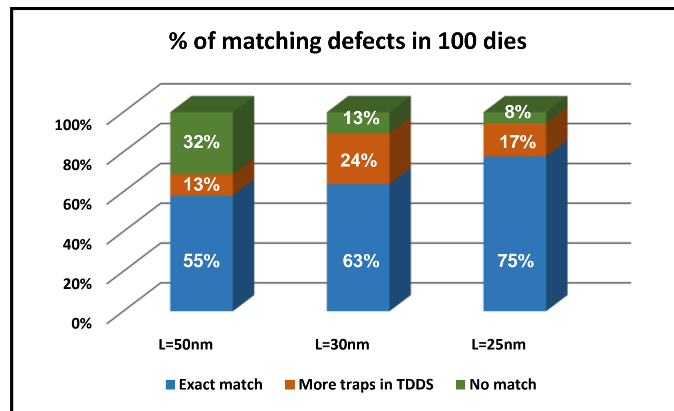


Figure 2.15 Correlation of the individual defects detected by the TDDS and RTN measurements per gate length. Better agreement between the methods with scaling.

W=60nm	TDDS	RTN
L=50nm	$3*10^{10}$	$1.6*10^{10}$
L=30nm	$8*10^{10}$	$6*10^{10}$
L=25nm	$9.5*10^{10}$	$8*10^{10}$

Table 2.1 Effective trap density per device area (/cm^2), recorded with TDDS and noise measurements, for three different geometries.

2.5.4 "After stress" comparison

For the second part of the study, we stressed the PMOSFETs with top gate width W_{TOP}=60nm and gate length L=50 and 25 nm, under standard, fast range NBTI setup, at 125°C and for a $V_{G,\,stress}$=-2V for 100s. Plotting the typical NBTI ΔV_{TH} evolution with time (Figure 2.16) we observe a shift of almost 80mV for both gate lengths, while the relaxation is equally fast for the two device areas.

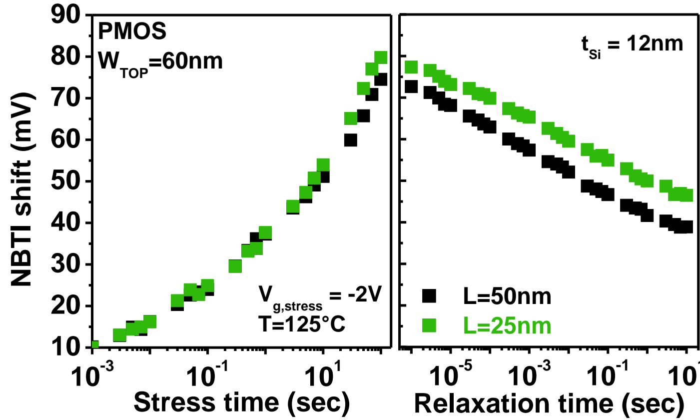


Figure 2.16 Typical V_{TH} shift during stress (left) and relax (right) for two gate lengths, L=50nm and L=25nm.

The above conclusion can be verified by plotting the Cumulative Distribution of V_{TH} shift, just after 100s of stress and after the end of relaxation for the smaller gate length (Figure 2.17). Fitting the data with the DCM model, we see that the average number of defects is decreased, from 25 to 13 for L=50nm and from 47 to 27.5 for L=25nm, by the end of the relaxation measurement (10sec).

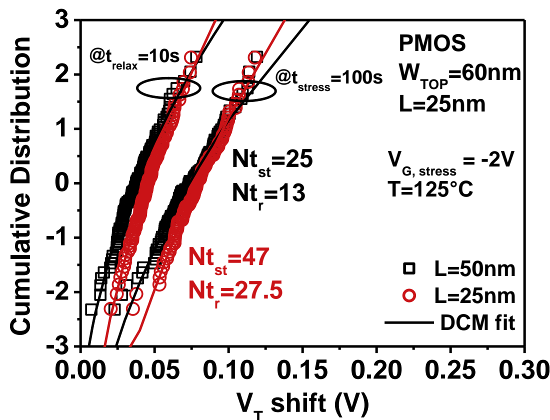


Figure 2.17 Cumulative distribution of ΔV_{TH} after stress of 100sec and after the end of 10sec relaxation for L=25nm.

After the stress, we return at room temperature and repeat the procedure of the previous section using the same settings and equipment to extract the ΔI_D and plot the CCDFs like before (Figure 2.18). Again, we see two different slopes in the distributions for both methods and gate lengths. In all the cases, there is no difference between the extracted η values before and after stress, a value that is consistent with previous results that place the defects close to the Interface Layer (IL). As we reported in 1.5.2, η has proven independent of the filling time as well as the temperature increase. This means that there is no modification of their depth. For the TDDS results we see, also, that the intercept with the y-axis remains the same after stress showing that the ratio of detected defects is not impacted. However, regarding RTN results, this time we have a shift of the intercept, a higher R, regarding the tail distributions meaning

that we are able to detect fewer traps, a behavior that can be attributed to the fast relaxation that occurs for both gate areas and to the stochastic nature of defects in deeply scaled devices which are no more detectable in our experimental window [105], [106].

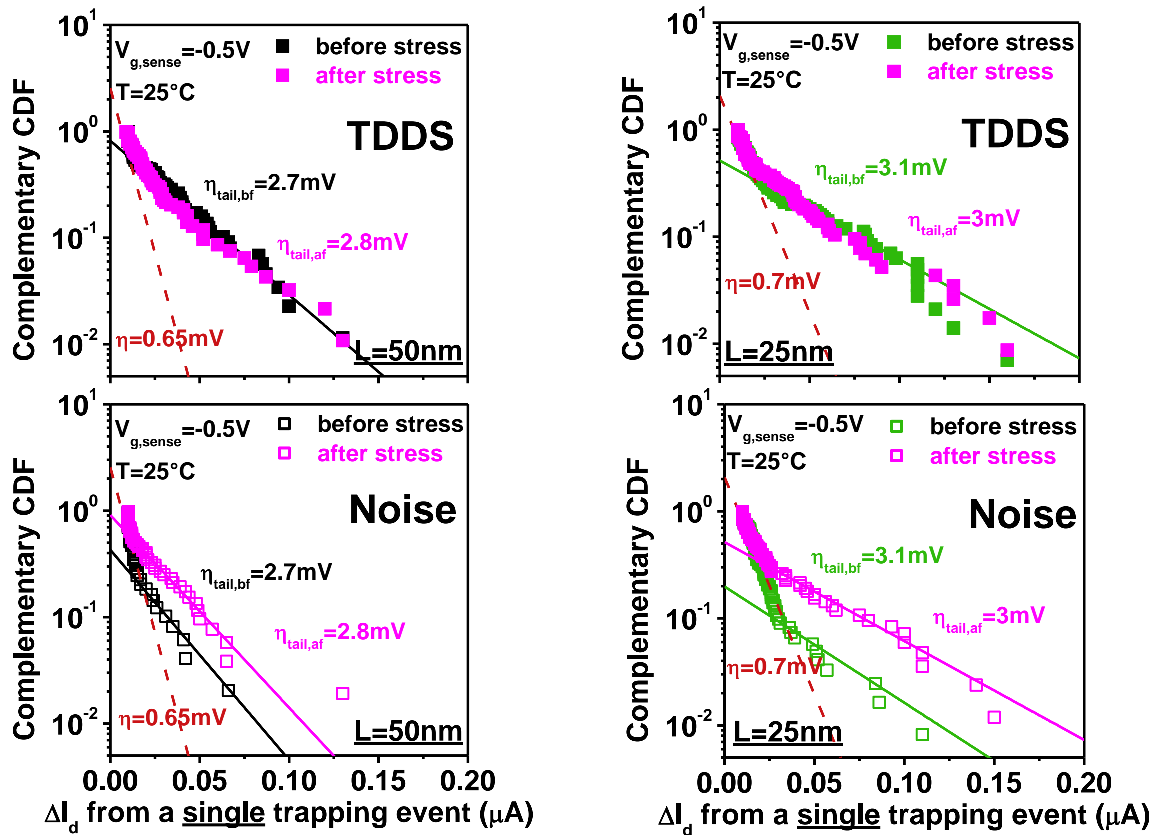


Figure 2.18 CCDFs of individual traps recorded after the stress, for PMOSFETs with W=60nm and L=50nm (left) L=25nm (right).

Moving a step forward, we investigate the correlation of traps, individually for each method, and both geometries before and after stress. To do so, we determine three similar categories using the histograms as before (Figure 2.19). Category 1 represents the condition of having a larger number of defects after applying NBTI. For example, we can see three peaks after stress instead of two at the beginning of the experiment. This means that we have an additional trap detected. Category 2 describes the detection of the same trap(s) before and after stress, both in terms of numbers and current level. Finally, in Category 3 we record a smaller number of traps after the stress application which means there are fewer current fluctuations, mostly due to the relaxation that was discussed before.

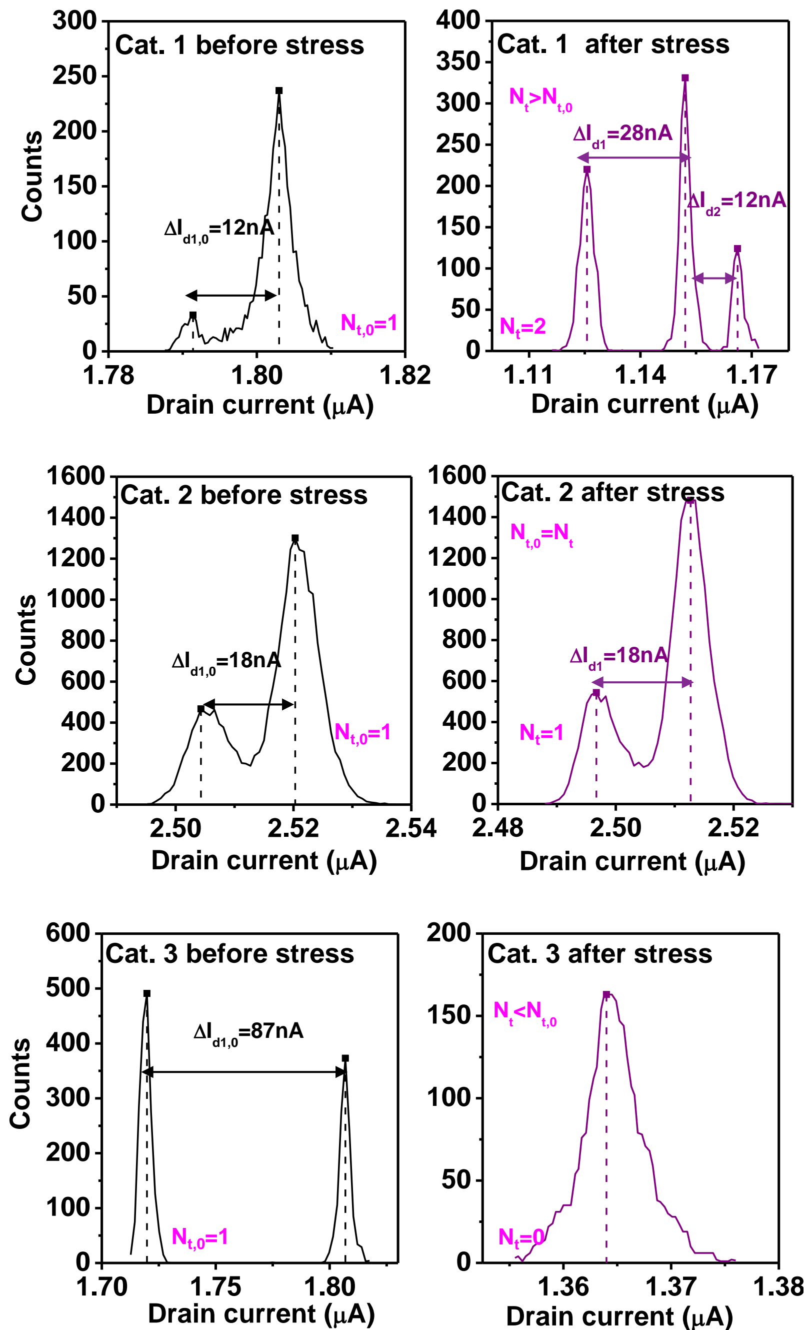


Figure 2.19 Definition of defect categories describing the agreement of traps, before and after stress, for TDDS and Noise measurements in both tested geometries.

By making, the comparison of the individual defects detected by the TDDS and RTN measurements (Figure 2.20) we can see that, for the larger gate length, the majority of recorded steps is in agreement before and after stress. At the same time, the impact of NBTI and the “disappearing” of traps hold a small percentage (≈24%) for both methods. For the short channel PMOSFETs, again, the stress effect is not evident and the data are equally divided between looking at the same defects or no defects at all (> 40%). This last assumption can be attributed to the stochastic nature of trapping on scaled transistors and in order to have reliable results, the need of repeated measurements in each device is necessary. However, using here our statistical results we can see a general trend of the method comparison and their application to 3D architectures.

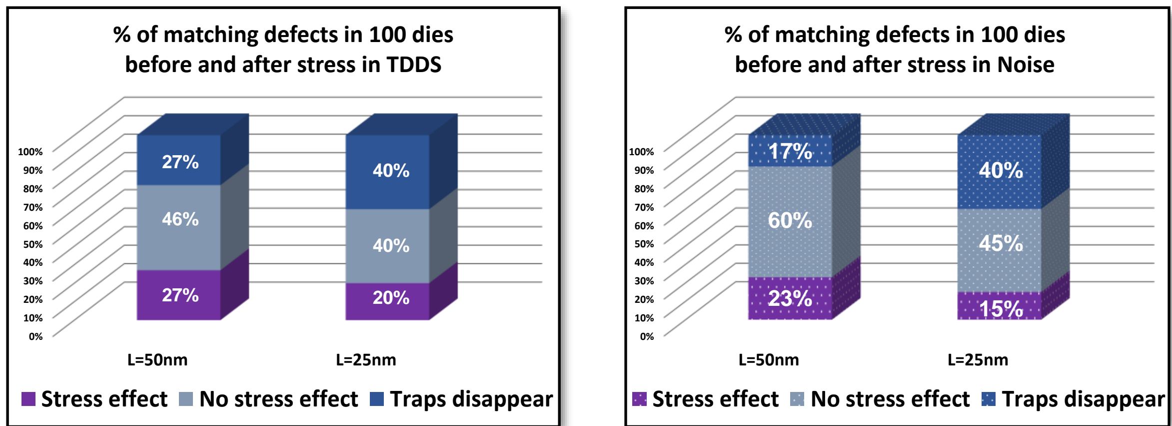


Figure 2.20 Correlation of the individual defects detected by the TDDS (left) and noise (right) measurements per gate length, before and after stress.

Summarizing the results of this Chapter, the novel Trigate nanowire architecture was introduced. At the beginning, we studied their impact on the dynamic variability, looking at their geometry dependence. The gate width appeared to be the most critical factor on the results and the t_{Si} *having minor effect, when the gate length showed uncertain conclusions. For this reason, a detailed study with the most widely used trap extraction techniques was presented. The trap extraction in Trigate PMOSFET nanowires was performed by using TDDS and RTN, two very similar but also very different methods. Before stress, a first-time bimodal distribution has been witnessed for all tested FDSOI geometries, an indication of the existing defects inside the Buried Oxide. Furthermore, the correlation of the traps recorded for each technique, shows a very good agreement for all gate lengths, with a minimum consistency of 55%. After stress, the bimodal distribution remains but with fewer defects detected with RTN, possibly due to the insufficiency of our measuring window. Comparing each method separately, in both cases the large area transistors do not seem to be impacted by stress while for the shorter L, there is a split of the results between the no stress effect and the no trap recording. Nevertheless, it is interesting to see how these well-known techniques can be applied to 3D architectures, specifically to Trigate nanowires and what kind of information we can acquire from them.*

Chapter 3. Impact of 3D sequential integration on BTI/RTN reliability

3.1 Introduction

As the Equivalent Scaling era comes to an end, we keep searching for alternative approaches to continue the advancements in semiconductor industry, moving closer to the "More than Moore" era. In this 3D power scaling period, we have heterogeneous integration schemes and reduced power consumption with the help of vertical structures. One of the most promising candidates towards this target is the 3D sequential integration. The main benefits of this particular design are that we can achieve a high density for high performance and reduced scaling for lower cost [27], at the same time. Its unique 3D contact characteristics offer a large set of applications and opportunities for smart and scaled sensors [28], [107], [108]. The concept is to develop a Top-Level device fully aligned with the bottom one (Figure 3.1), and although it sounds relatively "easy", the fabrication of the two-level transistors faces many process integration challenges [32]–[34], [109].

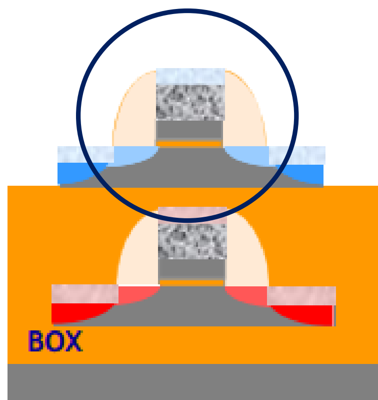


Figure 3.1 Schematic design of 3D sequential technology with fully aligned two-level transistors.

The most important one is that the top MOSFET must be processed at low temperature (500-600°C) in order to preserve the integrity of Bottom-Level silicided contacts. But reducing the thermal budget may be detrimental for the Top-Level device, as well, in terms of performance and reliability [110], [111]. Having that in mind, in Sections 3.2-3.3 we will try to "simulate" the behavior of a Top-Level transistor and provide a set of guidelines with all the process steps that can be improved in order to achieve the desired performance and reliability. Finally, at the end of this chapter, in Section 3.4, we will present a complete study of a fully integrated 3D sequential technology.

3.2 Impact of low temperature process

The first, and most important, step that will be addressed, towards a 3D sequential integration is the temperature decrease during process. As we saw before, it is essential to secure the electrical properties of the transistor and, at the same time, to achieve low degradation.

3.2.1 Quality of thin gate stack oxide

In order to evaluate the quality of the gate oxide of a low temperature process, we studied its impact on N&PMOSFETs silicon nanowires (described in previous Chapter) with 10 fingers in parallel (Figure 3.2) in addition to the standard single-channel ones that have been presented

so far. The multi-finder device's top gate width is W_{TOP}=30nm and the gate length L is 100nm, with a silicon thickness of 12nm while the single-channel ones feature a geometry of W_{TOP}/L=60/80nm.

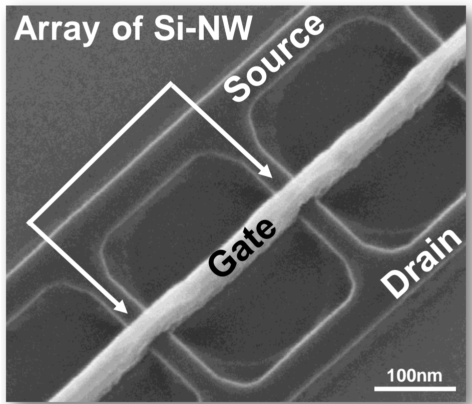


Figure 3.2 Top view of tested arrays with 10 parallel fingers.

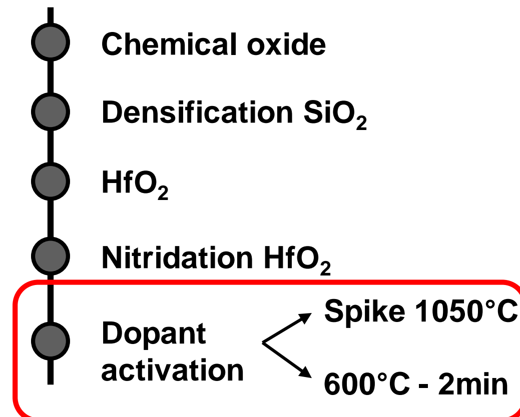


Figure 3.3 Process flow of the tested structures having as a variant the temperature of dopant activation.

Four processes with different thermal budgets were compared (see Table 3.1) for long and short channel devices. For the first split, that was used as a reference, a high dopant activation temperature was applied at 1050°C (HT), while the other three have a lower activation temperature at 600°C (LT). The LT splits also feature differences concerning a different Interfacial Layer (IL) preparation and a different nitridation of the HK layer. In general, integrating a high-k material requires the formation of an IL, mostly, to obtain a better interface with the Si channel. In the reference case, it is the high temperature that plays that part and leads to a thin and qualitative SiO_2. But, when the temperature decreases (here to 600°C), it is necessary to add another step in the process flow, which is the densification (splits HT and LT3). Finally, all of them have a common gate stack of HfO_2/TiN.

	Split HT	Split LT1	Split LT2	Split LT3
Chemox	●	●	●	●
Densification 8Å-SiO_2	●			●
HfO_2	●	●	●	●
Nitridation HfO_2	●		●	●
Activation dopants 600°C- 2min		●	●	●
Activation dopants Spike 1050°C	●			

Table 3.1 Tested splits evaluated for the temperature study.

Starting our study by performing C-V and leakage current measurements, on large area devices, us evaluate how the electrical properties change with thermal budget (Figure 3.4). Fitting the capacitance results, for a frequency of 90 kHz, with an in-house developed model, we extract the Equivalent Oxide Thickness (EOT) for all tested splits. Looking at the extracted value in the inset, we observe that the difference between the dopant activation temperatures is less than 1 Angstrom (Å) and, along with the leakage current results it is safe to conclude that there is no significant change in the macroscopic properties of the gate stack for low TB. The drop of the experimental value of the capacitance at high V_G is could be due an excessive leakage current, only that it is usually smaller. However, in our case it is quite enhanced and the leakage current data show that this is not the reason. So, it should be due to a higher series resistance (process dependent) that leads to a problem in the gate activation.

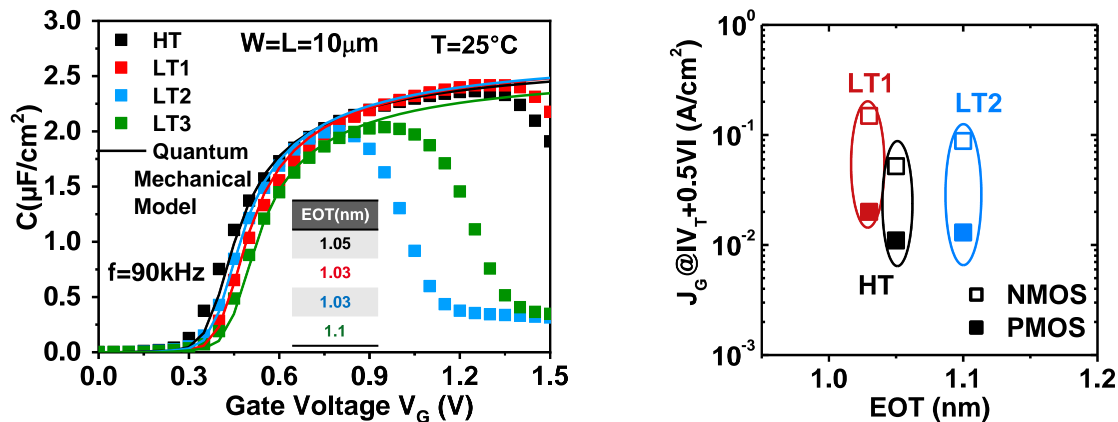


Figure 3.4 (left) Comparison of NMOS C-V characteristics measured on large devices L=10µm, (right) Gate leakage current Jg vs EOT from C-Vs for each split

Having established that, the next step is to see the impact of pre-existing defects that are responsible for the Random Telegraph Noise (RTN), known as t_0 reliability. For that reason, we used the TDDS method, described in Chapter 1, to analyze the oxide defects. NMOS and PMOS results will be presented separately because traps responsible for trapping are not necessary the same in two kinds of devices.

NMOSFETs

Starting with the NMOSFETs, we compare TDDS results for both single and multi-channel transistors. By plotting the total V_{TH} shift, just after the filling step, at 100us (Figure 3.5), it is clear that the low thermal budget (TB) slightly affects the NMOSFETs, they experience a shift less than 10mV for the multi-channel arrays and even smaller for the single-channel. Easily, we fit the distribution with the DCM model and extract the η and the N_T for each case. Since we have no variation in the V_{TH} shift, it is only natural that we obtain the same η as well. The average number of charge defects has a small increase in the 10-array transistor and a very small variation in the 1-array. The difference between these results is due to the fact that in the first case, we have a larger gate area, hence more defects compared to the single-channel ones.

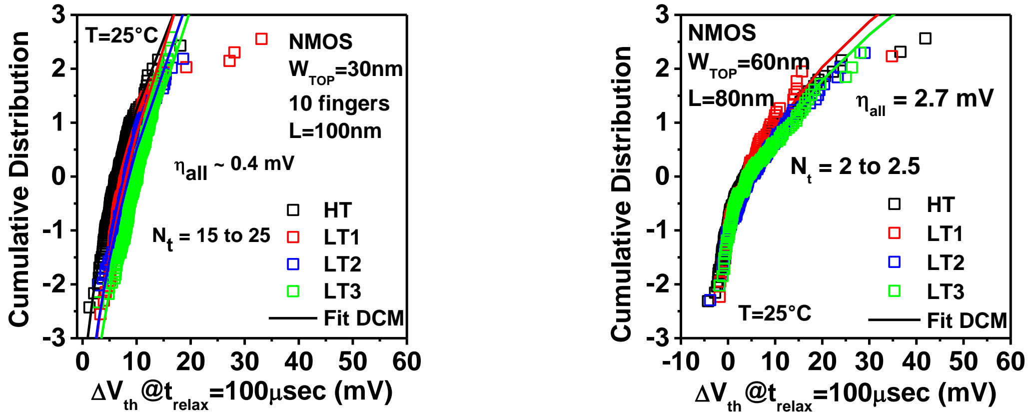


Figure 3.5 Cumulative distribution of total V_{TH} shift measured on 100 devices, 100µs after the end of the filling step stage for (left) multi-channel and (right) single-channel NMOSFETs.

Taking, now, the single trapping events recorded during the relaxation period and plot the CCDFs (Figure 3.6). For the multi-channel devices, the average V_{TH} shift from a single defect is estimated to be less than 1mV in all splits, with a value varying slightly from 0.35mV to 0.43mV, almost superimposing one another. However, in this case, the sensitivity of the technique is rather poor because of the large total effective width of the devices, 10·W_{TOP}. This low sensitivity was shown in [112]. Therefore, while it is preferable to use these transistors for the N_T extraction, due to the averaging effect on large surfaces, it is advisable to use single-channel devices for a reliable η extraction. This is done in the right Figure 3.6. For the single-channel transistors, there two sets of distributions. The first set includes the LT1 and LT2 for which η is found higher than for the second set LT1 <2. In both cases, traps are expected to be located in the high-k layer in these NMOS devices. But, the difference in the two families lies in an extra process step to densify SiO_2 interfacial oxide for both HT and LT3 variants (see Table 3.1). Therefore this increase of η, for set 1, may be explained here either by a change of the charge centroid (closer to the channel interface) induced by the IL densification process [93] or by a variation of the dielectric constant of the IL induced by the same process, which, would modify η in the way.

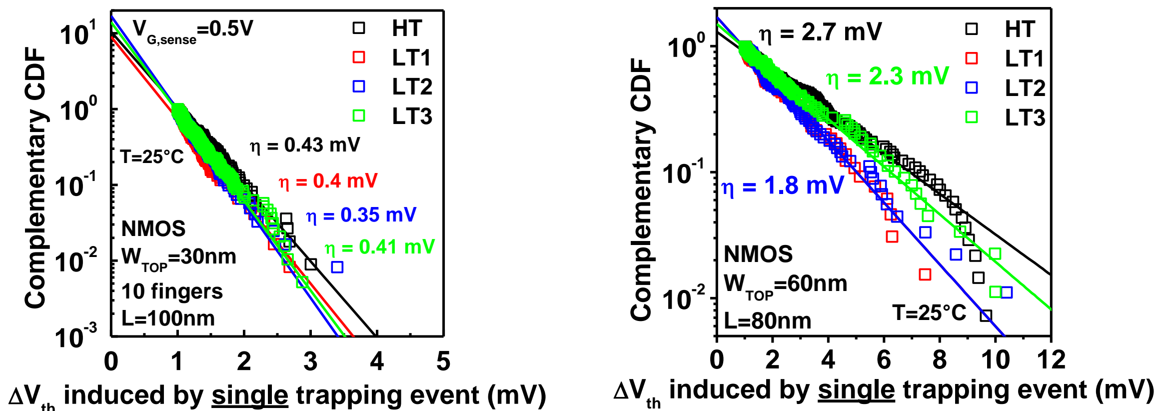


Figure 3.6 Complementary Cumulative Distribution Function (CCDF) of individual ΔV_{TH} induced by single trapping event measured on NMOSFETs with (left) 10 parallel arrays and (right) one array.

PMOSFETs

The next step is to look at the impact of the TB on PMOSFETs, again single and multi-channel ones. The first indication that we get from the CDFs, is the impact of the low temperature on the IL and the total V_{TH} shift after the filling step (Figure 3.7). On multi-channel transistors, there is a strong degradation of almost 45mV for the LT splits compared to the 20mV of the HT reference. Even though the difference between HT and LT of single-channel devices, regarding the total V_{TH} shift seems smaller, it actually doubles again, from 9.4mV for the HT to 18.4 for the LT splits. For the single-channel data, it is possible to fit the distributions with the same η and watch that the average number of defects increases with the decreased temperature. On the contrary, for multi-channel transistors it is only possible to fit the model for the HT reference split. This is due to the fact, that there is a higher number of defects in the LT devices that leads to a computational error. A problem that does not exist in the single-channel devices due to the reduced number of defects on their smaller surface. For this reason, we will need the help of CCDFs to extract some meaningful information for PMOSFETs.

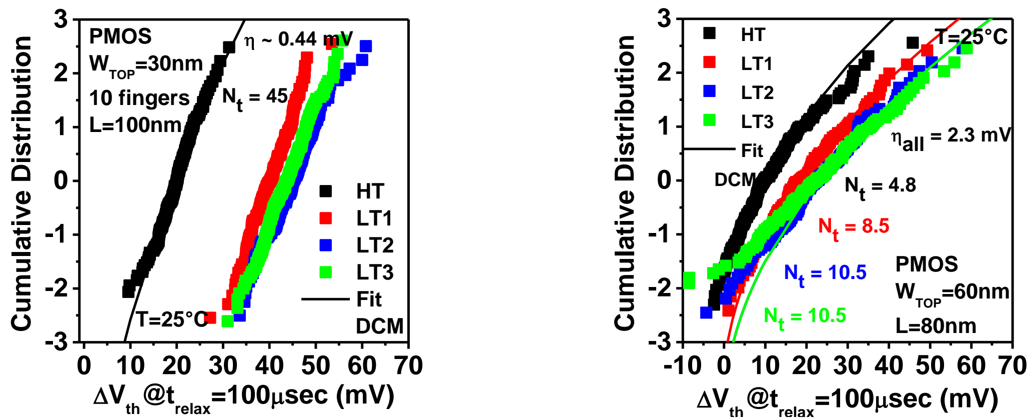


Figure 3.7 Cumulative distribution of total V_{TH} shift measured on 100 devices, 100µs after the end of the filling step stage for (left) multi-channel and (right) single-channel PMOSFETs.

Using again the recorded step heights, larger than 1mV, we plot the exponentially distributed CCDFs (Figure 3.8). For PMOSFETs, we see the opposite behavior that in NMOSFETs: the multi-finger devices vary regarding the average V_{TH} shift, that increases with low TB, when the single-channel ones have the same η value. Aforementioned, the issue on multi-channel transistors is the lack of sensitivity [112] that can lead to an underestimation on the average V_{TH} shift caused by a single defect. However, the extracted N_T values can be used to give an indication of the average number of charged defects without any variability issues due to their large gate area.

On the contrary, single-channel PMOSFETs appear to have the same average V_{TH} shift per defect despite the variations of the processing. Unlike NMOSFETs, all splits show a constant average V_{TH} shift of 2.3mV. This is due to the fact, that, in PMOSFETs, the V_{TH} shift originates from trapping in IL defects and not to HK traps. And it seems that the thermal budget does not modify the nature of these hole traps: their average depth is not changed since η is unchanged. Using this extracted η values and Eq. 3.1 to fit the DCM, we can see that the N_T is increasing for the LT splits, for both single and multi-channel PMOSFETs (see Table 3.2).

$$N_t = \frac{mean\Delta V_{th}}{\eta} \qquad \text{Eq. 3.1}$$

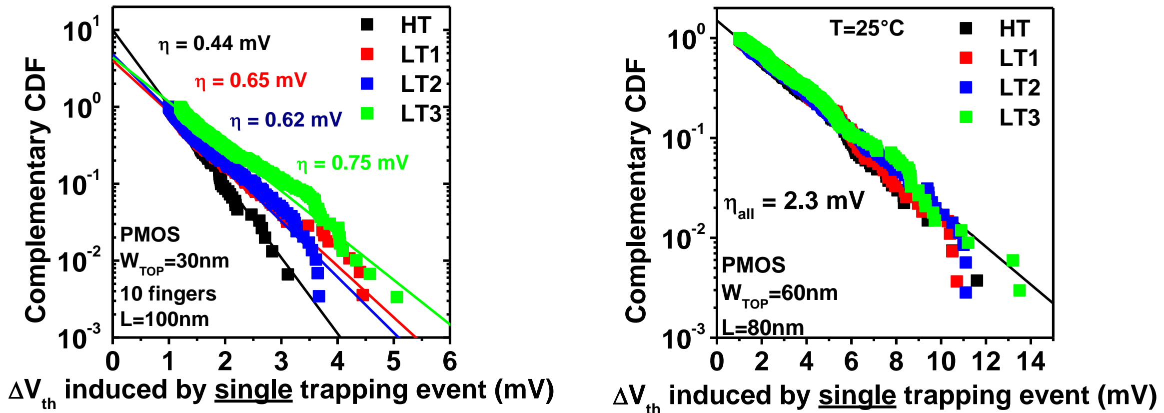


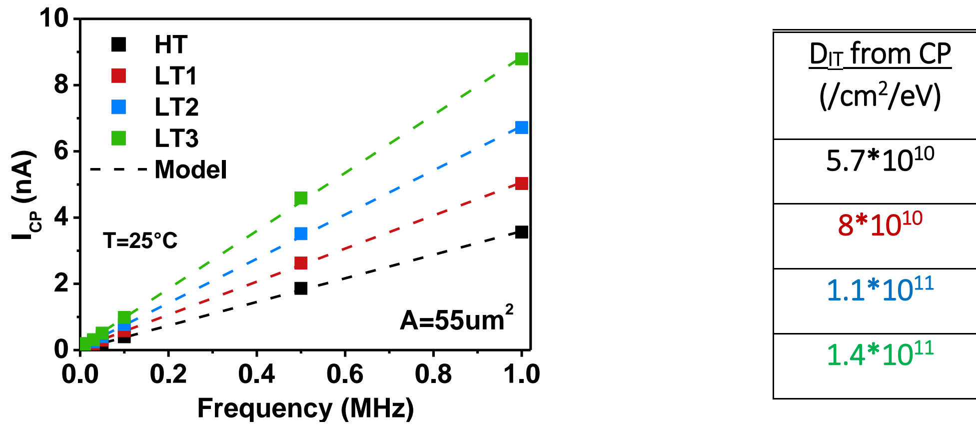
Figure 3.8 Complementary Cumulative Distribution Function (CCDF) of individual ΔV_{TH} induced by single trapping event measured on NMOSFETs with (left) 10 parallel arrays and (right) one array.

Looking at the extracted mean value of defects in each case, it is clear that either in 10 or 1-array PMOSFETs, the impact of low TB is severe when it comes to IL. The lack of HT is crucial for curing the process-correlated pre-existing defects and the need of low temperature seems to be the most challenging step for the 3D sequential integration, specifically for PMOSFETs.

PMOS single-channel	Split HT	Split LT1	Split LT2	Split LT3
N_T	4.2	7.7	9.9	9.3
η	2.3	2.3	2.3	2.3
PMOS multi-channel				
N_T	45	62	73	58
η	0.44	0.65	0.62	0.75

Table 3.2 Mean value of defect number and η for all tested splits on multi and single-channel PMOSFETs.

Moreover, performing Charge-Pumping measurements (Figure 3.9), from 100 Hz to 1MHz, we notice an important increase in the density of interface states ($D_{IT} \sim 8*10^{10}$ to $1.4*10^{11}$ /cm² /eV) in the case of LT devices which may be due to an interfacial SiO_2 whose thickness is less than the 6-7Å required to obtain the optimal insulating properties of SiO_2 [113]. The reduction of D_{IT} when using a HT budget (1050°C) has been observed before in the literature and can be attributed to a healing effect of the defects at high temperature [114]. Even if we look the LT splits separately, there are still some variations due to the different process steps between them improving or not the oxide quality, but still far from the high temperature reference. These results come in agreement to our observation on PMOSFETs, from the TDDS measurements, showing an increase in the number of IL defects for lot TB.



D_{IT} from CP (/cm²/eV)
5.7*10¹⁰
8*10¹⁰
1.1*10¹¹
1.4*10¹¹

Figure 3.9 Charge pumping current versus frequency shows an increased D_{IT} for LT devices.

Finally, all these results, for single and multi-channel transistors, are consistent with standard BTI measurements. Large area devices, both NMOS&PMOSFETs were stressed for 1000sec at 125°C (Figure 3.10). The new defects that were created due to BTI stress, in both types of devices, follow the same trend as the pre-existing traps. Regarding PBTI, we can achieve a very low degradation (less than 40mV) regardless the applied $V_{G,\,stress}$, which indicates that the HK defects responsible for it, will not be a problem for a 3D scheme. On the contrary when it comes to NBTI, the gap between HT and LT splits is quite big, verifying the temperature limit of 800°C to obtain a good enough reliability [115]. Even with a thicker interfacial SiO_2, like in the case of LT3, it is not enough to see an improvement in NBTI reliability, due to the low temperature.

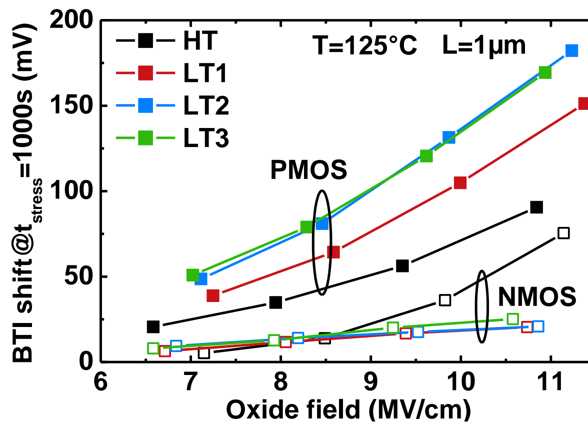


Figure 3.10 Corresponding BTI shifts versus oxide field measured on larger devices at T=125°C. BTI stresses in PMOS confirm that LT process degrades the quality of the IL oxide (larger number of defects).

3.2.2 Quality of thick gate stack oxide

One of the opportunities that open with a 3D sequential technology is the sensing applications, as was presented at the beginning of the Chapter. For this reason, the need of analog devices is increased with their performance criteria to be quite different from those of digital ones. Even if the main issue is not the short channel effect control, since the typical gate

length is L=300nm for a V_{DD}=3.3V, the gate oxide still needs to be optimized in terms of reliability requirements.

In our study, we tested thick oxide N&PMOSFETs, fabricated on 28nm FDSOI wafers, having as a reference a HT process with a spike anneal at 1050°C compared to LT Source-Drain junctions annealed at 600°C for 1min. The device gate width is 0.21µm and the gate length is the typical one, 0.3µm.

Again we start with by looking at the performance of our devices through Drain current – Gate voltage (I_D-V_G) and C-V measurements to see if and how the electrical properties change with thermal budget (Figure 3.11).

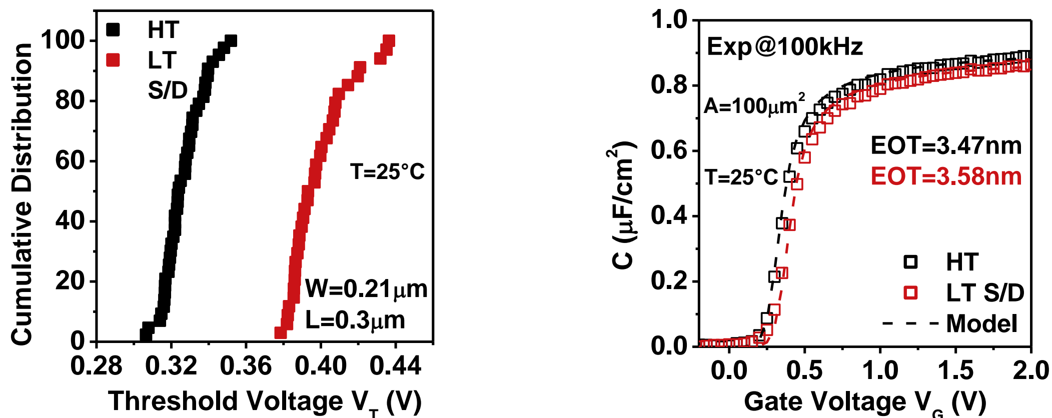


Figure 3.11 (left) Cumulative distribution of the extracted threshold voltage for both HT and LT splits of a gate length L=0.3µm and (right) C-V data at 100kHz and EOT extraction through Quantum-Mechanical simulations.

Extracting the threshold voltage, for a gate length of 300nm, shows that the LT transistors have a lower V_{TH} value, an effect of the lack of spike anneal in their process due to the positive shift of the TiN work function with temperature [116]. The results from C-V measurements, in large area MOSFETs of 100µm^2, reveal a higher EOT value for the LT Source/Drain junction wafer. Both are in the oxide thickness requirements (3.4-3.6nm) and allow us to continue with the reliability tests equally comparing them.

We performed a standard fast BTI measurements on both N&PMOSFETs devices, having a W=0.16µm and an L=0.3µm. This time using a higher stress voltage compared to the thin oxide transistors, from ±2.4 to ±3.2V, at 125°C and for 1000sec of stress time. Plotting the Fast BTI shift at the maximum stress time w.r.t the used stress voltage (Figure 3.12) reveals again what we have seen for the thin oxides. In PBTI, we can achieve an even lower degradation than before, due to the thick oxide (less than 20mV shift) regardless the applied $V_{G,\ stress}$, since the origin of PBTI is due to the HK oxide traps. On the contrary, for PMOSFETs the NBTI difference between HT and LT splits doubles again, even for an EOT larger than 3nm, verifying that a LT process degrades the quality of the IL regardless the thickness.

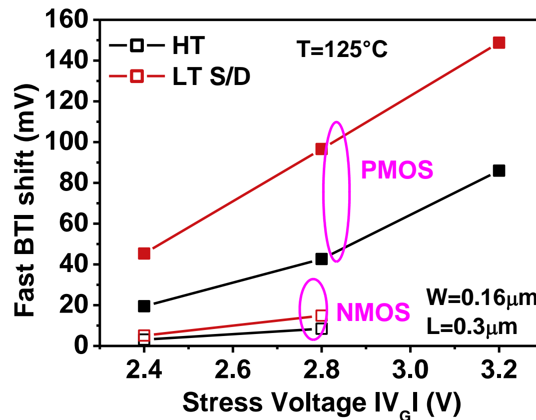


Figure 3.12 Fast BTI shifts w.r.t. applied stress voltage at 125°C. Once more, even for thicker oxide, the LT process degrades the quality of the IL oxide on PMOSFETs.

Different studies on thin and thick gate oxide stacks have shown us the principle issue for the future 3D sequential integration: the quality of IL. For NMOFETs, the impact of a low TB is negligible and each time passes the reliability criteria. On the contrary, for PMOSFETs the IL, either thin or thick, is severely degraded for lower temperatures and it is necessary to optimize the rest of the process flow steps in order to achieve the desirable performance and reliability.

3.3 Impact of different process steps

Besides the temperature which is the main issue when it comes to a 3D integration scheme, there other process steps that must be taken under consideration for a successful and reliable process flow. Steps like nitridation of the HK layer, the Post Nitridation Anneal temperature and, finally, the back end forming gas will be reviewed in this section. These steps are already known and evaluated in the literature for a high thermal budget [117]–[119], but we will address them now to a low temperature processing. The goal is to "simulate" the behavior of the Top-Level device and ensure a good reliability of the sequential integration as a total.

3.3.1 Tested structures

In Section 3.2, we saw that a low temperature integration hardly affects NMOSFETs while the impact on PMOSFETs is quite high. So, for our study, we only tested small PMOS single-channel Trigate nanowires with a top gate width of 60nm and a gate length of 80nm and a silicon thickness of 12nm. All of them have the same gate stack as before (HfO_2) and a low temperature dopant activation at 600°C for 2 minutes. The different variations between the splits are shown in Figure 3.13.

The study will be divided in three parts, as it appears in the flow diagram. In part A, we will evaluate the impact of the high-k nitridation step that takes place after the high-k deposition. Three different variations take place, a N_2, N_2/H_2 and a non-nitrided split. Part B will study the impact of the step right after nitridation, the Post Nitridation Anneal for two different temperatures. Finally, part C will investigate the impact of the back end forming gas, the last step during the processing of the gate stack of a transistor.

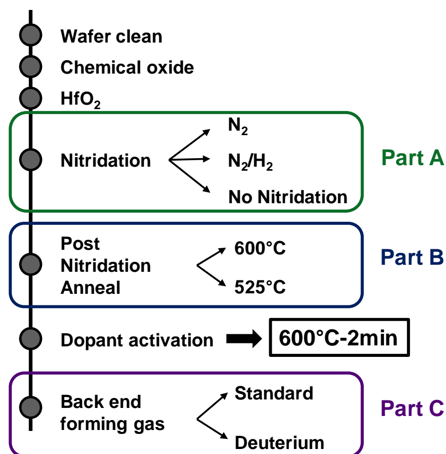


Figure 3.13 Variations of the tested splits evaluated for this study. All of them with HfO_2 and a low temperature dopant activation at 600°C for 2 min.

As previously, we will start by evaluating the electrical properties of the gate stack (I_D-V_G, C-V) and then move on to the reliability part (TDDS, NBTI).

3.3.2 Nitridation

The first process step (Part A), that will be evaluated, is the Nitridation of the HfO_2. As it is known, the nitrogen incorporation at the gate oxide has many advantages. It increases the SiO_2 permittivity or the crystallization temperature of the HfSiO or HfO_2 [120]. However, at the same time it seems to degrade even more the transistor's reliability. In our case, we tested three different splits, with an N_2, N_2/H_2 or no nitridation at all. From the average I_D-V_G of 200 devices, we observe no difference between the subthreshold slope values but, only a shift of the V_{TH} for the non-nitrided split (Figure 3.14) that can be attributed to the EOT roll-off already reported in [121] on capacitors where the variability is significantly lower.

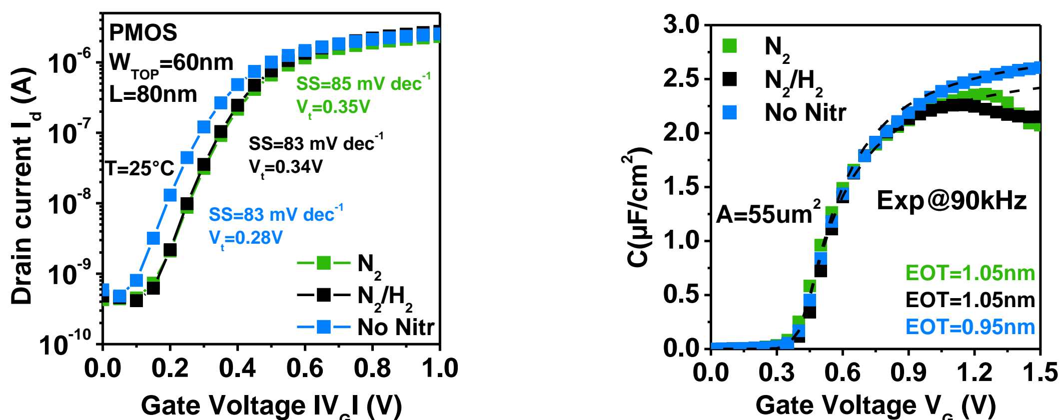


Figure 3.14 (left) Average I_D-V_G curves from 200 devices indicates a V_{TH} shift for the non-nitrided devices (right) Fit of the Capacitance-Voltage measurements indicate a higher EOT for the splits with both types of nitridation.

The C-V analysis, at 90 kHz, shows an additional advantage in terms of performance. Fitting the data with our Quantum-Mechanical model, we can reach a smaller EOT value for the non-nitrided devices. However, this comes in contradiction to the "normal" effect of Nitrogen which is the decrease of EOT [122]. At the same time, the small drops of the capacitance at higher V_G values prevent the capacitance in the nitrided splits from saturation. This leads to an

uncertainty in the EOT extraction. In addition to that, we acquire the same EOT values, even though the N_2/H_2 nitridation type is a lower incorporated nitrogen dose compared to N_2. The shown C-V drops indicate a higher leakage current for the two nitrided splits, verified by the leakage current results, on larger surface devices, in Figure 3.15. All these observations are likely to affect the next part of the analysis.

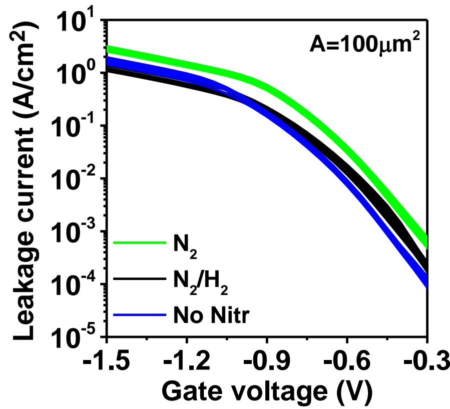
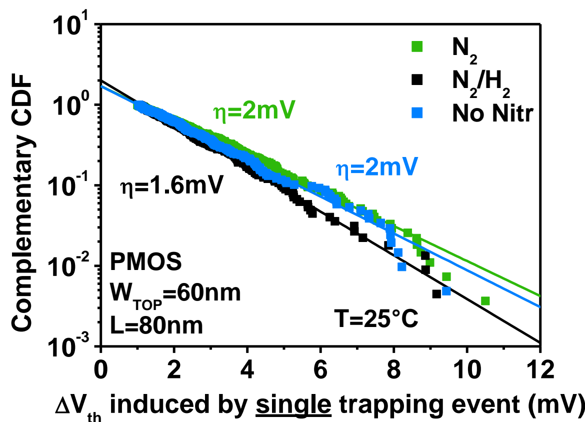


Figure 3.15 Leakage current measurements on large area transistors for the nitridation part.

For the evaluation of t_0 reliability we used again the TDDS method and a V_G=-1.2V to fill the traps. Recording the single trapping events, we plot the CCDF (Figure 3.16) shows a variation between the splits regarding the extracted η value. Specifically, a 1.6mV average V_{TH} shift of a single defect, for the N_2/H_2 nitridation on the contrary to the other two splits. One possible explanation is that the nitridation forms N-O bonds that can be broken due to upcoming annealing and release oxygen that prevents the regrowth of SiO_2, an oxygen diffusion barrier limiting the impact of anneal [121]. In the case of N_2/H_2 type, the use of hydrogen reacts with the oxygen to form O-H bonds which allows the nitrogen part to diffuse deeper in the gate oxide. For this reason, the detected defects in the case of N_2/H_2 type are located deeper in the oxide compared to the other two that remain closer to the IL, that justifies the difference in the extracted η value. In addition to that, the average number of charged defects found through the DCM is almost the same for the non-nitrided devices and the one with the lower dose of incorporated Nitrogen (N_2/H_2) showing that the additional H_2 can “cure” some of the pre-existing defects.



N_T from DCM
15
12
11

Figure 3.16 CCDF shows no significant difference between the splits, only a small variation of 0.4mV, showing that the t_0 reliability is not affected by the nitridation step. N_T values found from DCM are very close too.

However, after performing NBTI stress on larger devices, with W=240nm and L=10μm, we observe that the non-nitrided transistors show better reliability compared to both types of nitridation (Figure 3.17). Due to the uncertainty of EOT, we make a direct comparison through the applied stress voltage. The enhanced degradation of the nitrided splits is attributed to the creation of traps in the IL from the nitrogen, as it has been reported before for processes with a HT budget [117] and that apparently is valid in our case too.

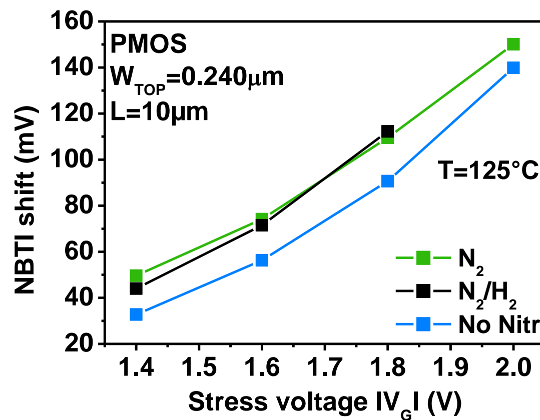


Figure 3.17 NBTI shift shows an enhanced degradation for the PMOSFETs with a nitridation process. Best compromise for the non-nitrided devices that combine a low degradation and a small EOT.

Apparently, we benefit from a lower degradation and a smaller Equivalent Oxide Thickness (EOT) for the non-nitrided split, but there is a doubt on the EOT extraction. The sure thing is that the degradation is much more important when nitridation is included in the gate stack and that it is important to prevent nitrogen from reaching the interface during the CMOS process. Like that, we decrease the formation of Si-N bonds near the IL that leads to carrier scattering effects [123]. One of the optimizations that can be made to improve this phenomenon is to control the nitrogen profile and limit its diffusion, e.g. by decreasing the Post Nitridation Anneal temperature, as we will see in the next section.

3.3.3 Post Nitridation Anneal

After the nitridation step, we have the Post Nitridation Anneal which is necessary to stabilize the Hf-O-N bonds. This step has been made at two different temperatures, 600°C or 525°C (Part B). We tested splits with no nitridation and with a N_2/H_2 nitridation. Of course, for the non-nitrided splits it is not necessary to have PNA, but it was interesting to see if there is any impact in that case too. Checking the electrical properties of both sets (Figure 3.18), we observe the same SS and V_{TH} values, for each type of splits, without any difference between temperatures.

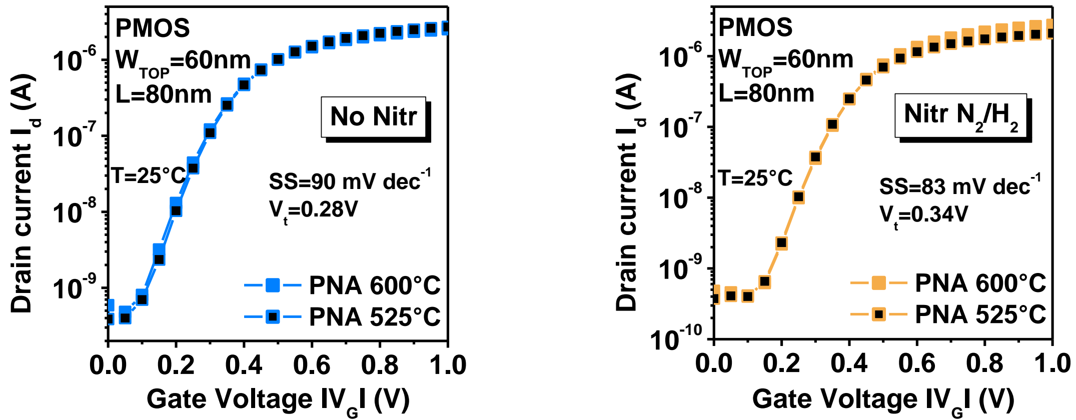


Figure 3.18 (left) Average I_D-V_G curves from 200 devices show no difference for the two post-nitridation anneal temperatures, either for non-nitrided or (right) nitrided splits.

Regarding the gate stack properties and the C-V analysis (Figure 3.19), at 90 kHz, we obtain the same EOT value for the transistors with no nitridation, no matter the PNA temperature. On the contrary, the splits with N_2/H_2 nitrogen incorporation have differences in terms of performance, a smaller EOT value for the lower PNA, at 525°C. In addition to that, we see again a drop of the capacitance at a high V_G, as before possibly to an excess leakage current.

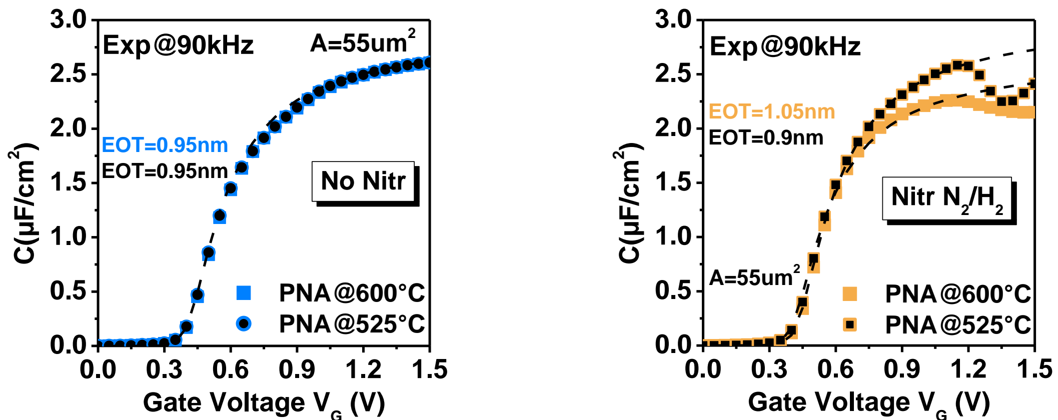


Figure 3.19 EOT extraction, from fitting with the in-house developed Quantum Mechanical Model, indicate the same value of 0.95nm for the non-nitrided devices (left), while there is a 1.5Å difference for the N_2/H_2 nitrided splits (right).

Indeed, this is confirmed by the current measurements (Figure 3.20). The results show that there is no shift on the gate leakage curves between the two PNA temperatures if we look each set of splits separately. Globally, it is clear that the devices that have “suffered” a N_2/H_2 nitridation are subjected to higher J_G levels.

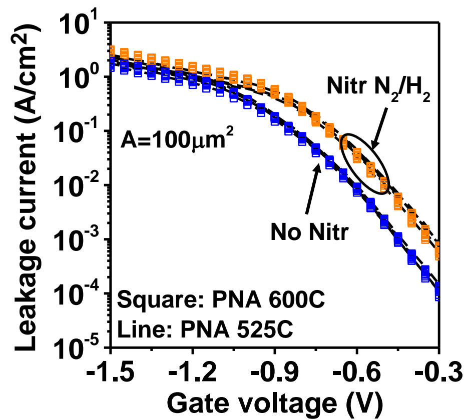


Figure 3.20 Leakage current data for both sets of splits showing that the nitridation is responsible for the J_G increase regardless of the PNA temperature used after.

Following the same procedure, as before, and looking at the impact of pre-existing traps (Figure 3.21), it is clear that there is no difference between the two used PNA temperatures, for each split type. The same average V_{TH} shift per defect as well as the same, extracted from the DCM, N_T for 600°C and 525°C.

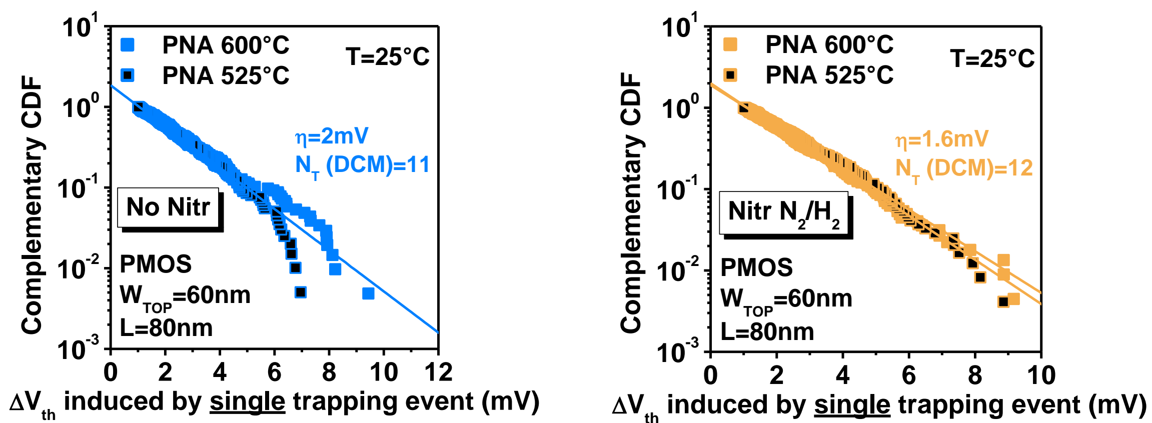


Figure 3.21 CCDFs for both PNA temperatures indicate the same t_0 reliability impact, regardless the previous process step.

Moving to the NBTI measurements, on large devices, for $V_{G,stress}$=-1.4V/-1.6V/-1.8V/-2V and at 125°C as usual, we see the same level of degradation for both used temperatures (Figure 3.22). The fact that PNA is an additional anneal, during the process flow, does not seem to improve the reliability, an indication that the dopant activation temperature is the main issue when it comes to the degradation caused by temperature, as shown in Section 3.2. In combination with the lower EOT that was extracted for the 525°C, we can achieve a very good trade-off between performance and reliability for the lower PNA temperature, an argument that is beneficial for the previous process step as well as for the continuous decrease of temperature in the 3D sequential integration.

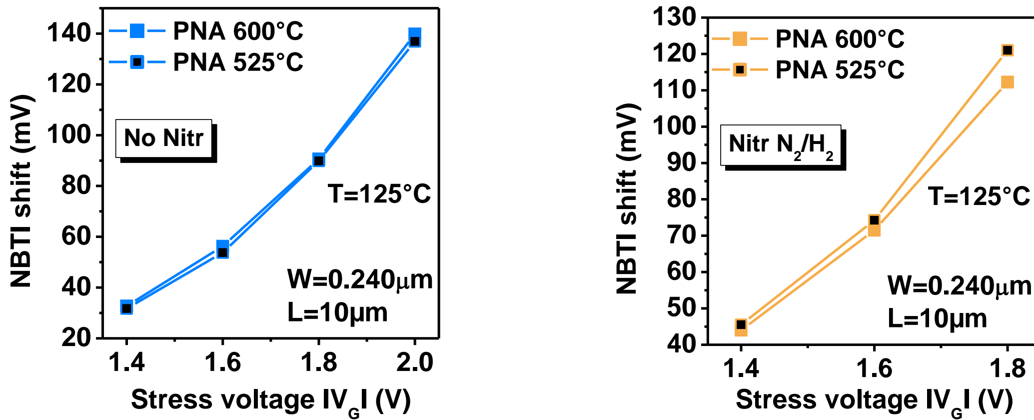


Figure 3.22 After NBTI: V_{TH} shift shows no difference between them, which allows us to choose the lowest temperature possible.

3.3.4 Forming gas anneal

The final step in a CMOS process is the back end forming gas. It is necessary to passivate the dangling bonds of the SiO_2/Si interface and improve the interface state density. Its most commonly used form is the N_2/H_2 at 400°C [48]. However, in our case, the Deuterium will be investigated as an alternative (Part C) which has to be annealed at high pressure in order to diffuse the atom to the IL. It is not a newly introduced method [124], but it will be addressed this time in an LT integration, just like the previous process steps. We will start again with the performance measurements on small area PMOSFETs (Figure 3.23). Our results show no difference in the, average of 200 devices, I_D-V_G characteristics, but C-V measurements reveal a lower EOT when the Deuterium is used. At the same time, we see no "drop" effect of the leakage current in the C-V compared to the standard gas, shown before in Figure 3.15 in black color. An effect already reported in [125] showing that the use of deuterium anneal is strongly favored to passivate the latent damage.

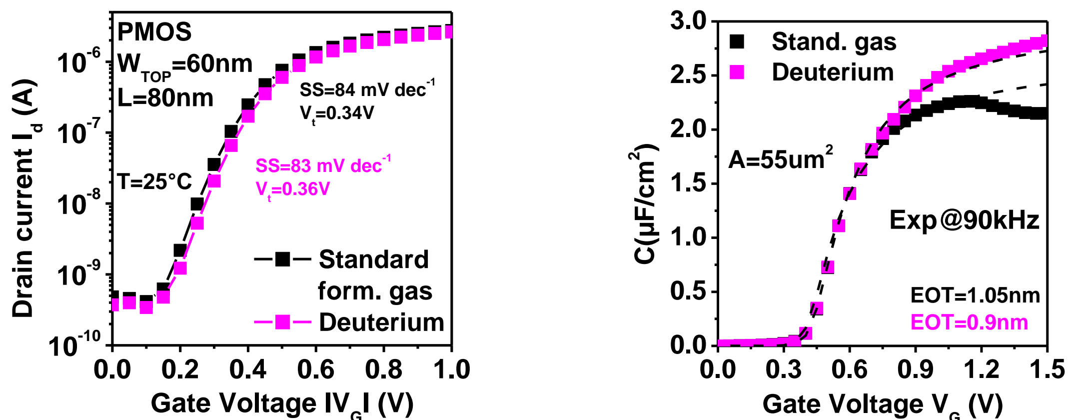
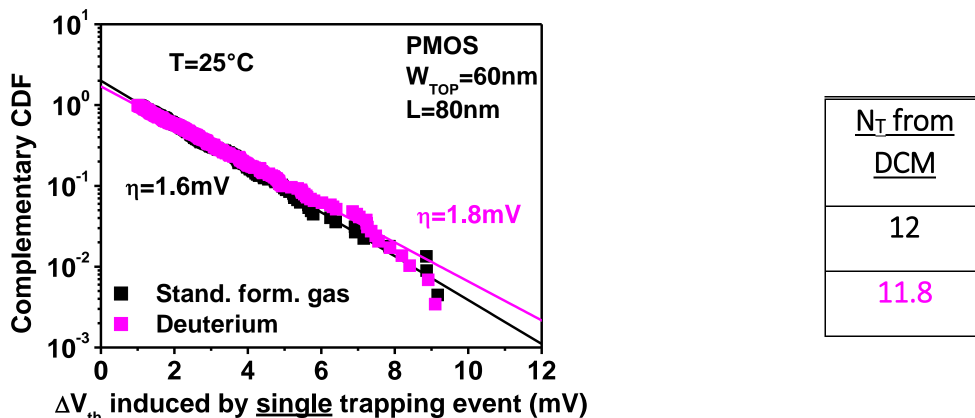


Figure 3.23 (left) Same SS and V_{TH} values for the two types of forming gas along with (right) a 1.5Å smaller EOT value when the Deuterium is used.

Applying TDDS to study the t_0 reliability (Figure 3.24), we observe no major difference of the average V_{TH} shift, from a single defect, in both cases. There is only a minor shift of 0.2mV, probably originated from the H_2 included in the nitridation process and which does not affect the extracted N_T from DCM. The fact that, N_T is found almost identical shows that average

defect density is not affected by the change in the forming gas, which is the last step of the gate stack flow.



N_T from DCM
12
11.8

Figure 3.24 Extracted η values have only a minor difference of 0.2mV which reveals the same degradation due to pre-existing defects.

Finally, looking at the NBTI results (Figure 3.25), we obtain a similar degradation for both, the difference for a high $V_{G,\,stress}$=-1.8V is only 6mV. This means that the deuterium passivated dangling bonds appear to be quite stable even though the EOT is less than 1nm. In the literature, there are some controversial results, for example in [126] there is no influence of deuterium passivation on NBTI reliability, while in [127] we see an improvement on NBTI. These opposed results show that the phenomena related to hydrogen and/or deuterium are still under study and, of course, one of the main factors that impact the conclusions is the different process followed each time. In our case, based on the similar degradation and the lower achieved EOT, we can say that by using a high-pressure Deuterium anneal, we have the best compromise between performance and reliability.

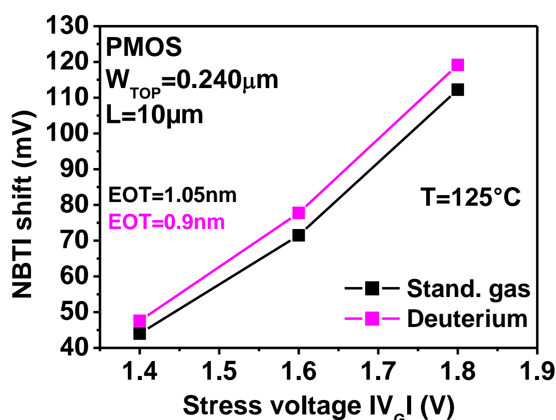


Figure 3.25 NBTI shift shows similar degradation (≈6mV) for the devices with Deuterium as back end forming gas, along with a small EOT. This is verified by an additional study that resulted in lower D_{IT} values when HPD2 was used.

It has already been established that developing a high-performance and reliable gate stack when it comes to the 3D sequential integration can be very challenging. Even though the NMOSFETs appear reluctant, we cannot say the same for PMOSFETs. The Nitridation of the HK has a major impact on the performance and reliability despite its many advantages. The Post

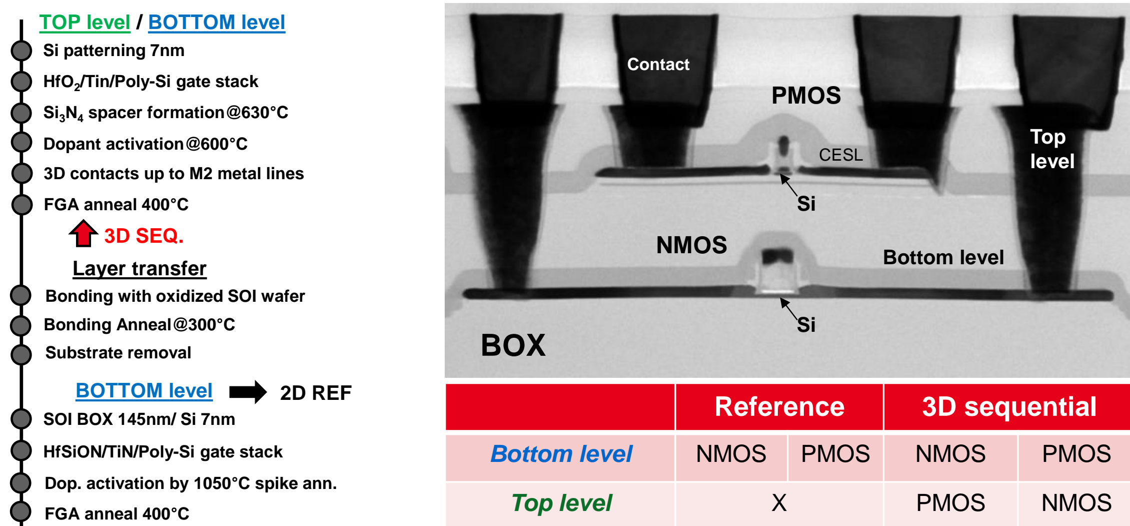
Nitridation Anneal temperature can be chosen to be low enough, at 525°C, a positive outcome towards the goal of low temperature sequential integration. Finally, with the High-Pressure Deuterium anneal showing very promising results, we summarize a set of guidelines for the future improvement of the 3D scheme process flow.

3.4 Fully integrated 3D sequential technology

Having studied, in the previous sections, all the necessary steps needed to have a reliable 3D integration scheme, we will present now for the first time, performance and reliability of a full integrated 3D sequential technology. Several groups during the last few years have been working on the development of this 3D sequential integration scheme, using different structures, like FinFET on FinFET [128] or FinFET on bulk CMOS [129]. The key point in all of them is the performance of the top transistor, but a key feature is the impact of the Top-Level on the bottom one and what happens with the reliability on both levels. So, these are the questions we will try to answer in this section.

3.4.1 Description-Devices

We will start with some details regarding the process fabrication of the devices (Figure 3.26) [30]. The reference transistors have a standard gate-first CMOS FDSOI route. They consist of a 7nm Si channel thickness and a gate stack of Nitrided Hafnium Silicate (HfSiON). They have undergone a dopant activation temperature at 1050°C and a forming gas anneal at 400°C steps with the last one used, as mentioned before, for the passivation of interface stack defects. This process route will serve as the basis of the Bottom-Level of our 3D scheme. In the next part, we will refer to the reference wafer as REF and the Bottom-Level of the 3D scheme as 3D SEQ.



	Reference		3D sequential	
Bottom level	NMOS	PMOS	NMOS	PMOS
Top level	X		PMOS	NMOS

Figure 3.26 (left) TEM image of 3D integration scheme. N&PMOSFETs are fabricated on BOTTOM and TOP layers. For the 2D planar references that we present, only CMOS Bottom-Level is processed, (right) Process flow of 3D sequential scheme with a max temperature of 630°C for the Top-Level.

Next, we developed a low-temperature sequential integration process in order to fabricate NMOS & PMOS transistors on a top tier as you can see in the cross-sectional TEM image. The Top-Level also features a 7nm thick Si channel, but this time with a Hafnium Oxide used as a

gate stack. The maximum temperature of the TL process is fixed by the formation of the SiN spacers at 630°C and the dopant activation was done at 600°C. The Top-Level also has a 400°C forming gas anneal, just like the Bottom-Level. In this 3D integration scheme, it is possible to have two types of contacts between the two-level transistors. Either independent as we have in this TEM image or with a shared drain contact (see later in Section 3.4.6).

3.4.2 Performance Bottom level

Initially, we wanted to investigate how a Top-Level process impacts the performance of the Bottom-Level transistor. In Figure 3.27, we can see a summary of the electrical performance on long channel N&PMOSFETs (W=L=10µm). We performed Capacitance-Voltage (C-V) measurements and fitted the experimental data with a Quantum-Mechanical model. From this fit, we extracted as usual the Equivalent Oxide Thickness (EOT) and the Work Function (WF), equal to 1.12nm and 4.51eV respectively, for both the reference devices and the BL of the 3D scheme. An indication that the gate stack properties remain unchanged after the Top-Level processing.

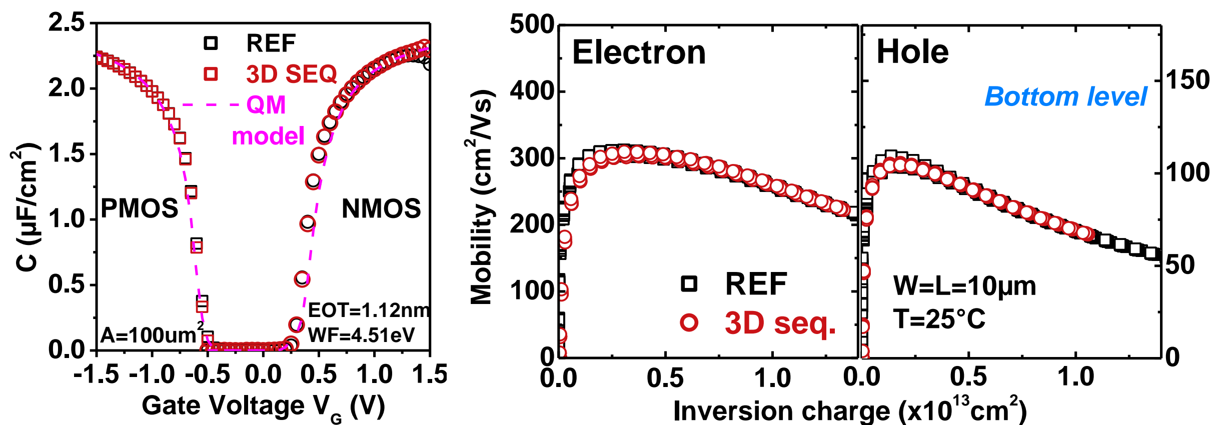


Figure 3.27 (left) C-V characteristics measured on long channel N&PMOS of BL transistors of 3D seq. tech., 2D REF and TL. EOT is 1.12nm in all cases, (right) Electron and hole mobility for 2D reference and bottom transistors of a 3D seq. technology show that mobility is unchanged after Top-Level processing.

Extracting, also, the electron and hole mobility on large area Bottom-Level N&PMOSFETs we see that it remains the same, there is no impact of the low temperature sequential integration. So, from these results, we can be confident that the transport properties are not affected by the Top-Level.

However, if we look on the performance of short-channel NMOSFETs, at a high V_{DD}=0.9V (Figure 3.28), we notice a small degradation of the saturated current I_{on} of the Bottom-Level transistors after processing the Top-Level. This can be due to a Top-Level processing that impacts the Drain-Induced Barrier Lowering (DIBL) or the threshold voltage (V_{TH}) of the transistors.

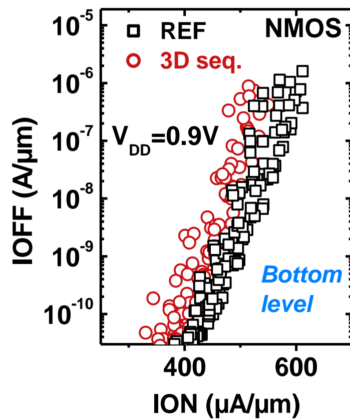


Figure 3.28 I_{on}/I_{off} for NMOS Bottom-Level devices show a small I_{on} degradation after the Top-Level process

Checking the DIBL and the threshold voltage extraction (Figure 3.29), for different gate lengths, we see that this is not the cause of the current degradation, there is no shift on the Bottom-Level devices. Looking at the sheet resistance of the Source/Drain contacts, before and after the Top-Level processing, we notice a small increase. This is consistent with previous observations and can be related to a structural change of the silicide layers due to agglomeration, phase change and Ni diffusion or NiSi regrowth, all for temperatures above 550°C [36], [109] that eventually affects the I_{ON} current.

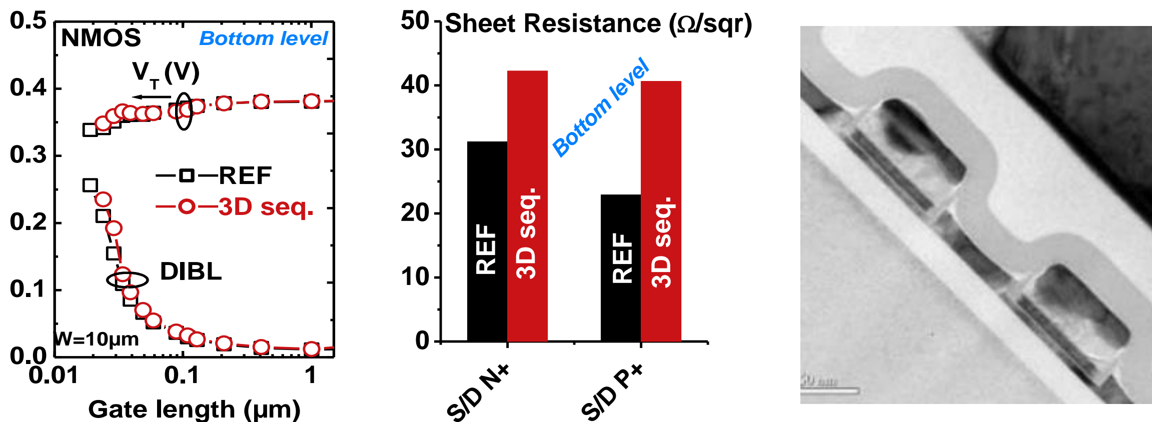


Figure 3.29 (left) V_{TH} & DIBL versus gate length for 2D REF & BL 3D seq. Both parameters are not affected by the TL process, (middle) Sheet resistance of N+ & P+ Source/Drain regions is increased after the TL process which explains the I_{on}/I_{off} degradation and (left) TEM showing the structural changes of the silicide layers [109].

Moving on with the study, it is essential to examine the variability which tends to increase as technology advances. For this reason, we plot Pelgrom's Figure of Merit of the matching results (Figure 3.30). By fitting the data, we could extract an excellent A_{VT} value of 1mV.µm measured for both planar REF transistors and BL devices of 3D sequential wafers. This value confirms the benefit of undoped FDSOI films to reduce variability [130], as well as that top processing has only minor impact on BL performance.

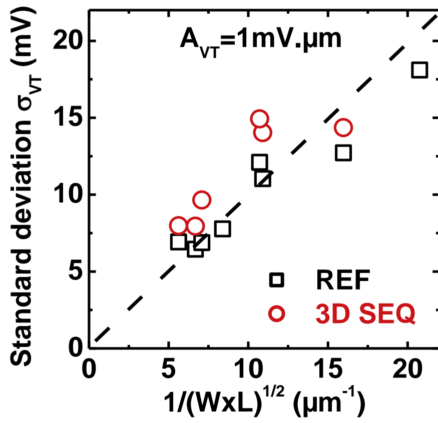


Figure 3.30 Pelgrom FOM for REF and BL 3D seq. technology shows excellent A_{VT} value even after the TL fabrication.

The next step is to evaluate the quality of the interface layer after the Top-Level processing (Figure 3.31). To do that, we used the Charge Pumping (CP) technique applied at different frequencies, from 1 kHz to 1 MHz. The density values that are found by fitting the model, are very low around $2*10^{10}$/cm^2/eV for both the reference and the Bottom-Level of the 3D scheme. These values prove that the excellent Si interface passivation that is achieved for REF FDSOI technology and can be preserved after the TL processing.

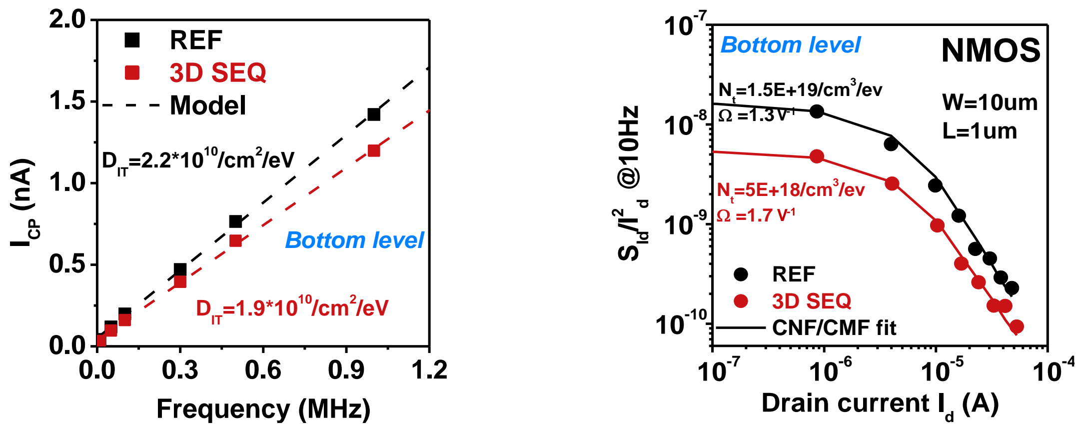


Figure 3.31 (left) Charge pumping current vs frequency extracts a very low D_{IT} value for both 2D REF and BL 3Dseq transistors, (right) Normalized PSD@ 10Hz fitted with CNF/CMF model helps us obtain the bulk trap density Nt which is strongly reduced after 3D integration.

Another excellent experimental tool, for the detection of defects in the dielectric interface, is the Low frequency Noise. We selected long channel transistors in order to avoid the Lorentzian spectrum that is observed on short channel transistors, as we saw in Chapter 1 and performed the measurements at different bias conditions, from 0.16V to 0.8V, all at linear regime with a V_{DD}=30mV. By fitting the normalized Power Spectral Density at 10Hz with the CNF/CMF model [83], we are able to extract the bulk oxide trap density (N_t) and the correlated mobility fluctuations factor (Ω). As we can see, Ω is almost the same since it mainly depends on the centroid of the carriers with the channel. However, N_t is divided by 3 after the TL processing. This suggests that the additional anneal used for the TL processing favors defect curing in the BL gate oxide. The difference with the Charge Pumping is due to the fact that the methods sense different traps, so even though the interface density is almost the same, the bulk oxide one is decreased after the Top-Level processing.

Summarizing the above results, it is safe to conclude that the performance of the Bottom-Level, N&PMOSFETs, is not affected by the Top-Level processing.

3.4.3 Performance of Top Level

After finishing with the Bottom-Level devices, we continue this study with the Top-Level N&PMOSFETs. Starting again with large channel devices (W=L=10μm), we perform the same C-V measurements as for the Bottom Level transistors which result in the same EOT and WF values as before (Figure 3.32) despite the change of the HK layer. Along with that, the Leakage current seems unaffected using HfO_2 as gate stack and, at the same time, without having any sacrifice in the EOT.

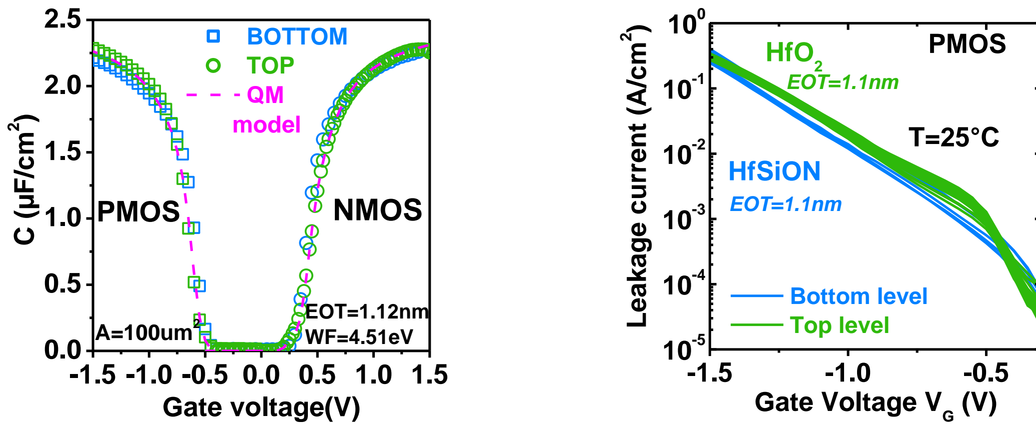


Figure 3.32 C-V measurements for Top-Level N&PMOSFET long channel transistors. EOT and WF match the Bottom Level devices.

However, this time we observe a degradation of the mobility of the TL devices, for both electron and hole (Figure 3.33). A drop of 42% for the first one and even higher for the latter (~80%). If we look at the conductance measurements performed at different frequencies: 10 kHz/ 30 kHz/ 90 kHz/ 300 kHz, we observe a more than 2x higher interface trap density for both N&PMOSFETs, compared to the Bottom-Level that we saw before. These high D_{IT} values result in an enhanced Coulomb scattering which in turn degrades the mobility [131].

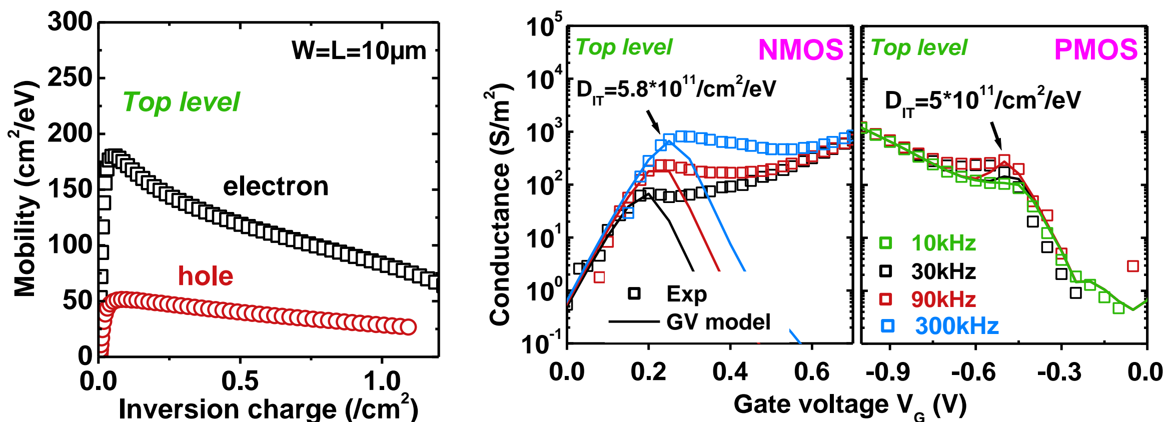


Figure 3.33 (left) Electron & hole mobility for Top-Level extracted on long channel N&PMOS from C-V split is degraded compared to the BL, (right) Conductance-Voltage GV characteristics for Top-

Level N&PMOS. A high D_{IT} value is extracted to ≈$5*10^{11}/cm^2/eV$ by GV peak modeling that explains the degraded mobility.

There are several process knobs under study to improve the Si interface passivation and turn, the mobility. One of these is the High-Pressure Deuterium Anneal, studied before. Figure 3.34 shows that inserting HPD2 into the process route helps us achieve D_{IT} levels found in the high temperature Bottom-Level devices. Moreover, this significant reduction of one order of decade, does not modify the leakage current and EOT demonstrating that the gate stack properties remain unchanged [34].

The performance of the Top-Level transistor, in an actual 3D sequential integration, has been studied, with results showing that despite the fact that it is still in a preliminary stage of research, it is good enough. The impact of low temperature TB is, of course, still evident but with much room for improvement.

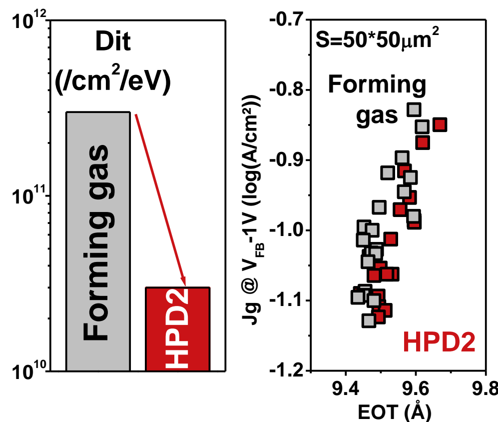


Figure 3.34 Investigation of Deuterium as back end forming gas seems to improve D_{IT} values and does not degrade the leakage current.

3.4.4 Reliability Bottom level

The second part of this 3D integration scheme study concerns the impact of the Top-Level process on the reliability of the Bottom Level transistor. For this reason, we applied fast (1µs range) BTI stress on N&PMOSFETs, at 125°C, for 1000sec and relaxation of 10sec. The exact same setup was used for the reference devices and the Bottom-Level of the 3D integration.

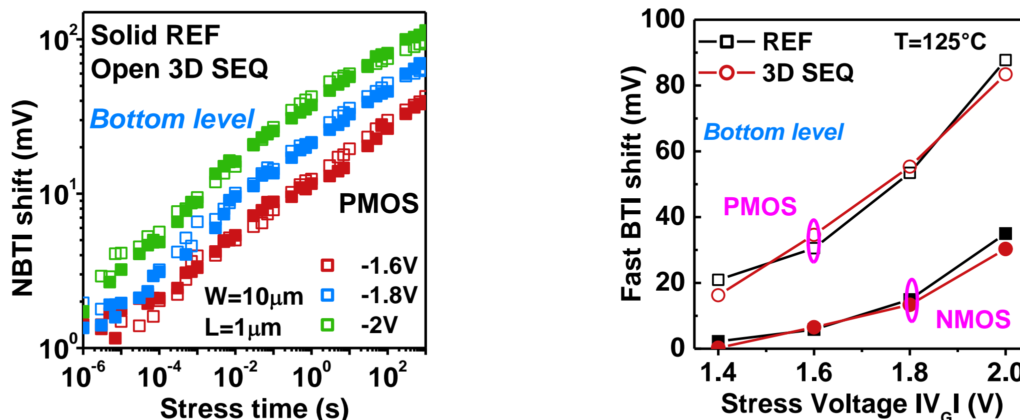


Figure 3.35 (left) NBTI shift vs time measured on 2D REF and BL PMOS of 3D seq. using fast methodology (1µs range) at T=125°C and, (right) BTI shifts for N&PMOS transistors show no additional degradation due to the Top-Level process.

Looking at the typical NBTI ΔV_{TH} evolution (Figure 3.35) with time we can see clearly no difference on the BTI amplitudes regardless the $V_{G, stress}$ for N&PMOSFETs. Plotting the fast BTI shift w.r.t. stress voltage, for both types of transistors, no difference is observed due to the Top-Level processing.

In addition to BTI, the next step is to evaluate Hot Carrier (HC) reliability, in short channel NMOS, with a gate length of 30nm. Again, a high acceleration temperature was used, at 125°C and the applied stress is performed under the worst-case conditions, V_G=V_D to have the maximum impact ionization.

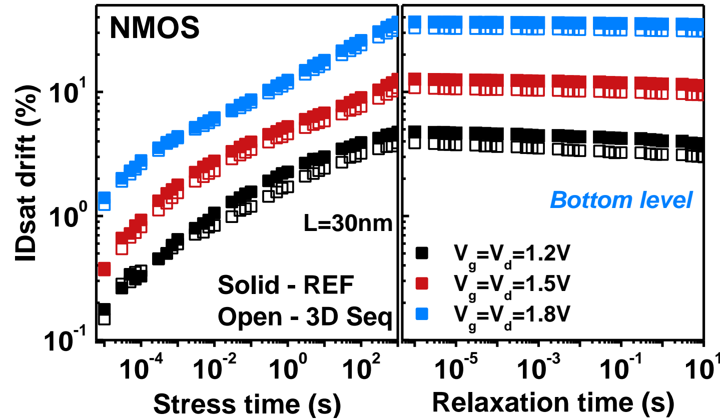


Figure 3.36 HC drift in short channel BL NMOS for various stress conditions of V_G=V_D. Again, no difference is seen between 2D REF and BL 3Dseq.

Figure 3.36 shows that the saturation current drift is almost the same whatever the stress level, before and after the Top-Level processing. Furthermore, a negligible recovery is observed during the relaxation ($V_{G, stress}$=0V) for both reference and Bottom-Level of the 3D scheme, confirming that the interface state generation is responsible for HC degradation, in both cases. This is in agreement with previously published results for Bulk [132], [133] and FDSOI technology [134], [135]. This last result, also, suggests that the integrity of dielectrics over the channel/drain junction is preserved after the TL processing and that Self Heating, which can enhance HC degradation, is not higher in the 3D integration scheme despite the presence of the Top-Level [136].

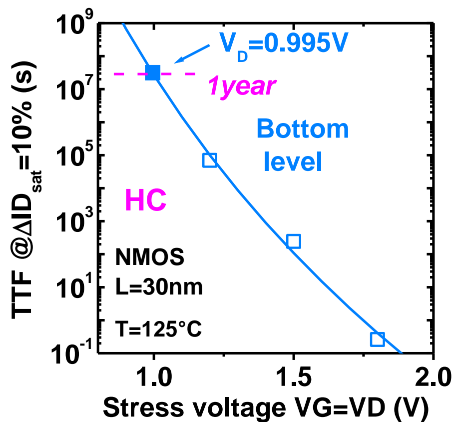


Figure 3.37 HC extrapolation, of L=30nm BL NMOS, of Time-To-Failure for different stress voltage, passes the criterion of V_D > 0.9V.

Next, we plot the Time-To-Failure, for a 10% drive current degradation, versus the applied stress voltage for the reference and the BL devices (Figure 3.37). Looking at the V_D, for a 1-year

operation, it is estimated to 0.995V; a value that satisfies this technology's requirements (V_D=0.9V).

From the above results, we can conclude that the Bottom-Level can, therefore, sustain a 630°C Top-Level process integration without affecting the gate oxide reliability of the Bottom-Level CMOS transistors.

3.4.5 Reliability Top level

Taking a step further, we wanted to study, for the first time, the reliability of a TL device. For this reason, N&PBTI reliability technique was applied under the same conditions as for the Bottom-Level. N&PMOSFETs were stressed, at various $V_{G,\,stress}$ during 1000sec. We plot, after, the Time-To-Failure, for a 5-year lifetime and extract the operating voltage at this point (Figure 3.38). Regarding PMOSFETs, the minimum V_G equivalent to their BL counterparts and over 1V. For NMOSFETs, there is a small decrease after the Top-Level processing, but still passes the reliability criterion (V_G>0.9V).

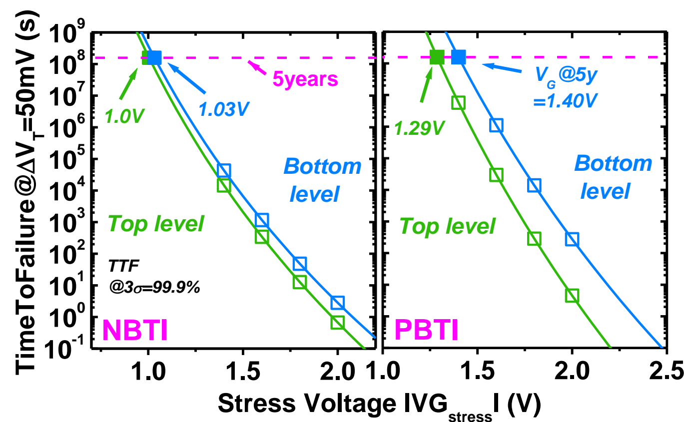


Figure 3.38 NBTI/PBTI Time-To-Failure extrapolation for TL N&PMOS compared to the BL counterparts. Both levels meet the lifetime requirements at 5 and 10 years.

Additionally, both types of transistors meet the reliability requirements, for a 10-year lifetime prediction as well, a timeframe that is used by several groups. Their values that are presented in Table 3.3 show that even in this case, the Top-Level N&PMOSFETs of a 3D sequential integration can achieve a minimum V_G of 0.98V and 1.26V respectively. Along with the Bottom-Level results, this is a first demonstration that we can have a functional and reliable 3D scheme.

BTI@T=125°C/ Criterion=50mV	V_G@10y/3σ PASS if V_G>0.9V
PMOS (TL/BL)	0.98V/ 1.01V OK
NMOS (TL/BL)	1.26V/ 1.37V OK

Table 3.3 Extracted V_G of Top-Level N&PMOSFETs, for a 10-year lifetime and a 50mV V_{TH} shift.

A complete benchmark (Figure 3.39) of performance and reliability, of published results [31], [38], [128], [129], [137], including this work, summarizes the work that has been done during the last years on a 3D integration scheme. Depending on the group different configurations have been used each time. Starting with the channel material and the silicon that remains the main candidate, but in different forms according to the need and targeting on different thicknesses. For the metal gate, it seems the research community is divided between TiN and TaN, in everyone's attempt to achieve the desired threshold voltage. Besides the chosen materials, there are also variations regarding the used structures, going from FinFET or Ultra-Thin Body (UTB) on bulk CMOS to FDSOI on FDSOI, in our case. The key point in all the groups is the outcome of a high performance Top-Level transistor, with a small enough EOT and high I_{ON} current. No actual work has been done in the reliability part, besides the study on low temperature capacitors, a similar concept to the one presented in Sections 3.2-3.3, the "simulation" of the behavior of the TL. With the extensive study shown here, in both aspects of performance and reliability of a 3D scheme, we provide useful information for future work towards the optimization of the 3D sequential integration.

		This work	IEDM'16[13]	IEDM'15[14]	IEDM'14[15]	IEDM'13[16]	IRPS'17[17]
Performance	Channel	Si mono	Epi-like Si	Epi-like Si	Poly-Ge	Si LC	Si
	Gate	TiN	TaN	TaN	TaN	TiN	TiN
	Structure 3D seq.	FDSOI on FDSOI	FinFET (TL&BL)	NWFET on bulk FinFETs	FinFET on bulk CMOS	UTB on bulk MOSFETs	Planar capacitors
	T_{si} (nm)	7	53.4	16	47	14	-
	EOT (nm)	1.12	-	-	-	2.1	1
	TOP level I_{on}/W_{eff}	P: 250 (I_{off}=40nA/µm V_{DD}=-0.9V)	P: 352 (I_{off} unknown V_{DD}=-1V)	P: 220 (I_{off} unknown V_{DD}=-1V)	P: 311 (I_{off} unknown V_{DD}=-1V)	P: 62 (I_{off} unknown V_{DD}=-1V)	-
Reliability	BTI@T=125°C Crit=50mV	VG@10y/3σ, PASS if VG>0.9V	X				V_{ov}@10y/ 30mV, T=25°C
	PMOS (TL/BL)	0.98V/1.01V OK					-
	NMOS (TL/BL)	1.26V/1.37V OK					TL: V_{ov}=0.7V BL: V_{ov}=1.05V
	HCI@T=125°C ΔId_{sat}=10%	VD_{max}@1y, PASS if VD>0.9V	X				X
	NMOS	BL: 0.91V OK					

Figure 3.39 Benchmarking performance and reliability of published results for 3D sequential technology.

3.4.6 Circuit level

In order to have a complete study, we moved on to the circuit operation of a two-level inverter, fabricated using this 3D sequential integration scheme. The inverter is made of a PMOS fabricated on the top of a Bottom-Level NMOS with two different configurations, independent or shared crossing drain contacts, as was discussed on Section 3.4.1.

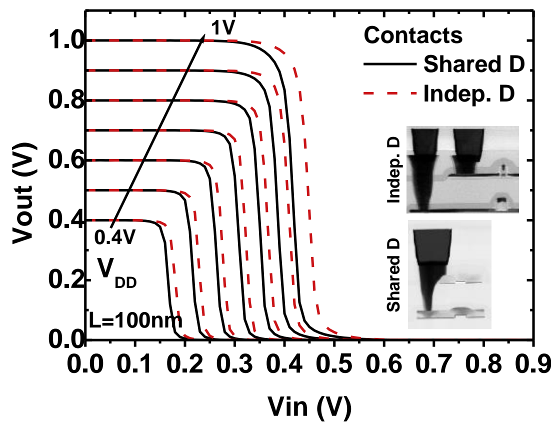


Figure 3.40 V_{IN}-V_{OUT} characteristic of an inverter integrated at 3D sequential scheme for different V_{DD} and two configurations.

In Figure 3.40, we can see the V_{IN}-V_{OUT} characteristics of short channel transistors, having a gate length of L=100nm, for both types of configurations and for a V_{DD} range from 0.4V to 1V. Both inverters show good functionality, but the shared drain contact inverter has a faster transition due to a higher level of drain current of the top PMOSFET. This was expected, since the additional contact that exists in the individual configuration, inserts an extra parasitic capacitance that lowers the drain current of the transistor and by consequence, the transition speed.

In addition to the good performance of the inverter and having measured the individual characteristics of both transistors (I_D-V_G-V_D), we were able to build and calibrate an in-house developed SPICE-like model. In that way, we perfectly reproduced the experimental data, for all tested V_{DD}, as it is shown in Figure 3.41, for the shared drain setup.

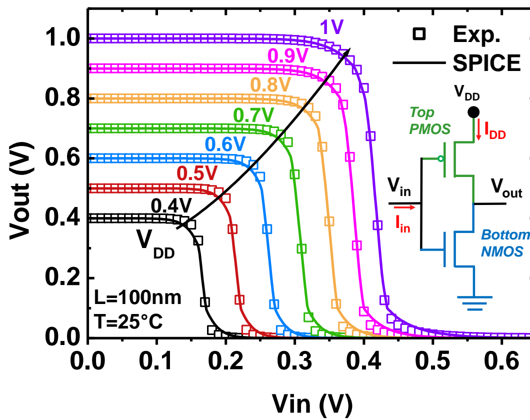


Figure 3.41 Fit of the experimental data with a SPICE-like model for the common drain setup at different V_{DD}.

At the same time, we measure the I_{IN} and I_{DD} currents, as presented in the inset. Using the same model, we can also fit the measured current data against the full used V_{DD} range as before and predict the inverter consumption, $P=I_{DD} \cdot V_{DD}$ (Figure 3.42).

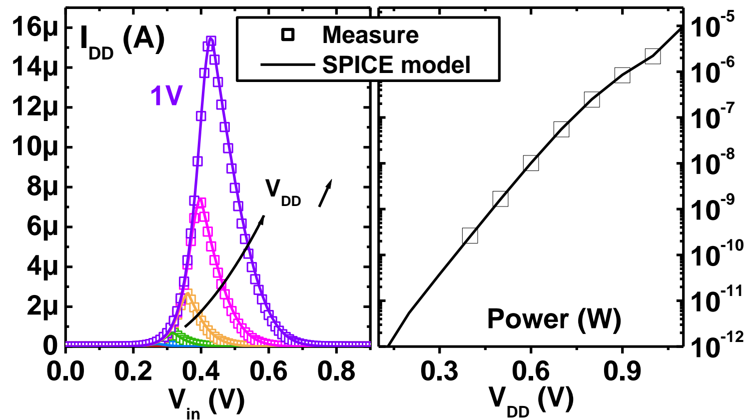


Figure 3.42 Very good agreement between simulated and measured I_{DD} current for different V_{DD} and fit of the calculated consumption.

With the help of the model we can tune our technology and use the right threshold voltage, for the bottom NMOS and top PMOS transistor, in order to achieve the desirable inverter performance in terms of switching bias and dissipated power as you can see in the simulated results, in Figure 3.43.

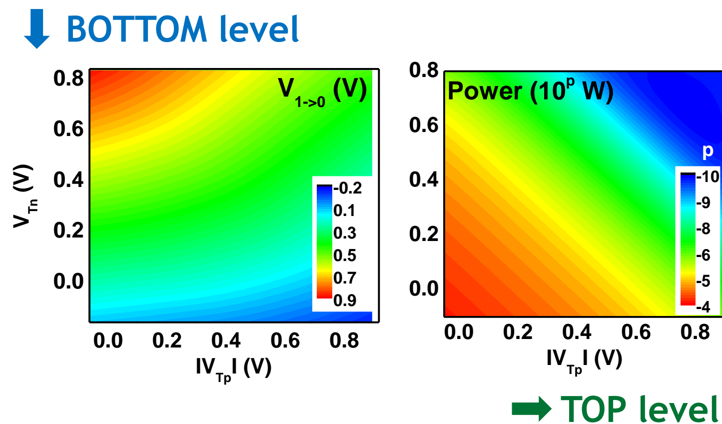


Figure 3.43 Simulated switching voltage (left) and dissipated power (right) of the inverter w.r.t. N&PMOS $V_{TH,n}$ &$V_{TH,p}$.

The same inverter is now stressed under NBTI condition using fast measuring units (WGFMU) and a digital scope to capture the V_{OUT} (V_{IN}) characteristic after stress. Here in the setup, we used a standard Measure-Stress-Measure technique with a $V_{G,\ stress}$ of -2V for 100s of stress at 125°C and a 10s relaxation period (Figure 3.44).

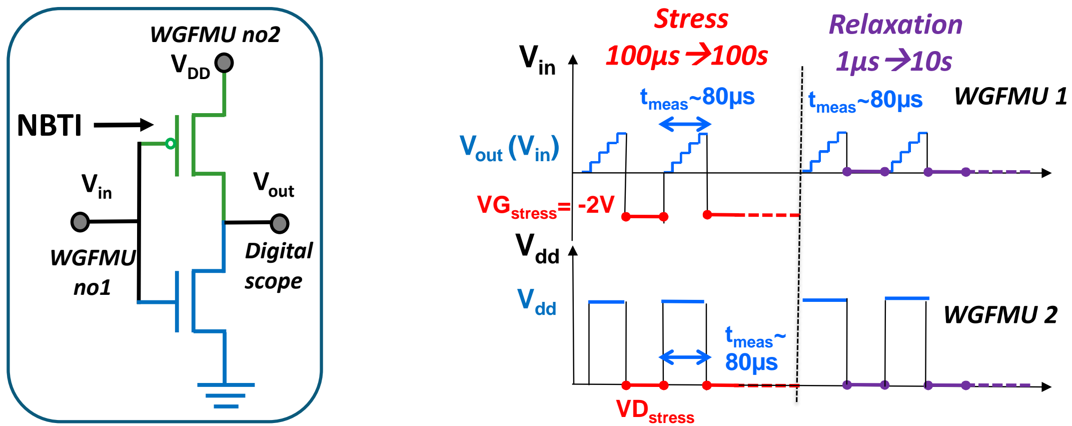


Figure 3.44 Experimental setup for NBTI application on integrated inverters in this 3D scheme.

In order to reproduce the data acquired during stress, we used a combination of the standard BTI modeling described in Chapter 1, for the top PMOS and bottom NMOS transistors individually, along with the SPICE-like modeling that was used before. The only difference is that the V_{TH} shift was added in the initial threshold voltage of each device type, so the V_{OUT} and I_{DD} were modelled w.r.t. to the final V_{TH}, after stress, and the V_{IN} (Figure 3.45).

Model description:

1) NBTI V_T shift of individual **TOP** pmos/ **BOTTOM** nmos

2) SPICE-modeling of V_{out} and I_{DD} w.r.t. $V_T+\Delta V_T$ and V_{in}

Predict ageing of 3D sequential circuits

Figure 3.45 Schematic of the used model to reproduce the V_{IN}-V_{OUT} characteristics of the-two level inverter that can be used to predict the ageing of 3D seq. circuits.

Looking at the experimental V_{IN}-V_{OUT} drifts and the current degradation during stress and comparing them to the modeled data, we can see that we have a very good agreement between them (Figure 3.46) and are able to reproduce the current and voltage drifts with stress time. With these results, we can validate our approach that combining a SPICE-like and NBTI modeling, we are able to predict the ageing of 3D sequential circuits.

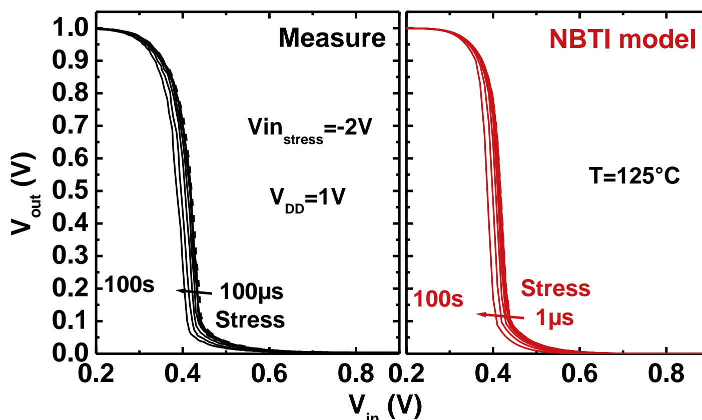
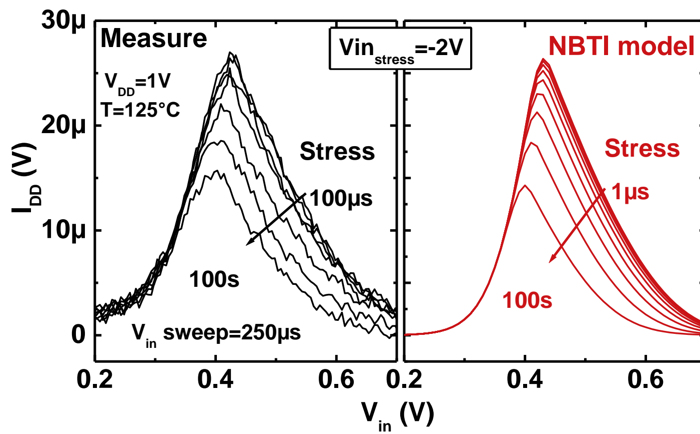


Figure 3.46 (up) Measured and simulated drifts of V_{IN}-V_{OUT} characteristic of the two-level inverter under NBTI stress at $V_{IN,stress}$=-2V and 125°C, (down) Current drifts at V_{DD}=1V, under NBTI stress of an inverter integrated at 3DSI in very good



agreement with the simulated characteristics.

In this Chapter, the 3D sequential integration was presented in detail regarding performance and reliability. An evaluation of all the major process steps has been made, regarding the dopant activation temperature, the HK Nitridation, the Post Nitridation Anneal temperature and the Forming gas anneal, providing a set of guidelines for a Top-Level device integration on the standard CMOS route. Furthermore, in the last part of the chapter, an actual 3D scheme was studied in terms of performance and reliability showing the promising results towards the More than Moore era.

Chapter 4. Impact of high mobility materials on NBTI reliability

4.1 Introduction

At the continuous struggle of scaling, different approaches have been used as described in Chapter 1. The last one that will be presented here, is the use of high mobility materials in the channel, specifically the use of Germanium on PMOSFETs. Due to the, by default, lower mobility of holes compared to electrons, an idea came up in order to boost the performance of the former and at the same time to tune the threshold voltage of the transistor, the use of SiGe alloys [98], [138]–[140]. Besides the continuous verification of it, several studies and groups have shown, that, along with performance boost, the integration of a SiGe channel can significantly improve the Negative Bias Temperature Instability (NBTI) reliability of these transistors. Regarding the origin of this improved reliability, one of the most popular assumptions is that it may be explained by a more favorable alignment, in the case of SiGe channel, of the Fermi level with respect to the energy levels of the oxide defects [141], [142]. It is true that the bandgap reduction caused by the Germanium incorporation makes the Fermi level move upwards and reduces the number of defects that can capture holes accumulated in the thin SiGe layer. Moreover, the traps involved in the trapping process are supposed to be localized both within the Interfacial Layer (IL) and the high-k (HK). However, not everything is clear regarding the physical mechanisms that lead to this result, like the exact spatial position of the traps involved in the trapping. For the moment, there is no experimental evidence that proves the contribution of HK traps in the improved reliability of PMOSFETs [143]–[145]. The goal of this chapter is to confirm or not this hypothesis by analyzing results from individual traps as well as NBTI data, in thin and thick interfacial layer oxides, providing useful insight for future integration using Germanium content in the channel.

4.2 Tested structures

For our study, we used single-channel PMOS planar devices, with different Ge content incorporation. The content starts from 0%, which is the Si reference, and having as a maximum the 38%. The transistors are fabricated on 28nm FDSOI wafers (BOX thickness 25nm) using a gate first integration scheme and provided by STMicroelectronics. A cross-sectional TEM image and a sketch of the used devices are presented in Figure 4.1.

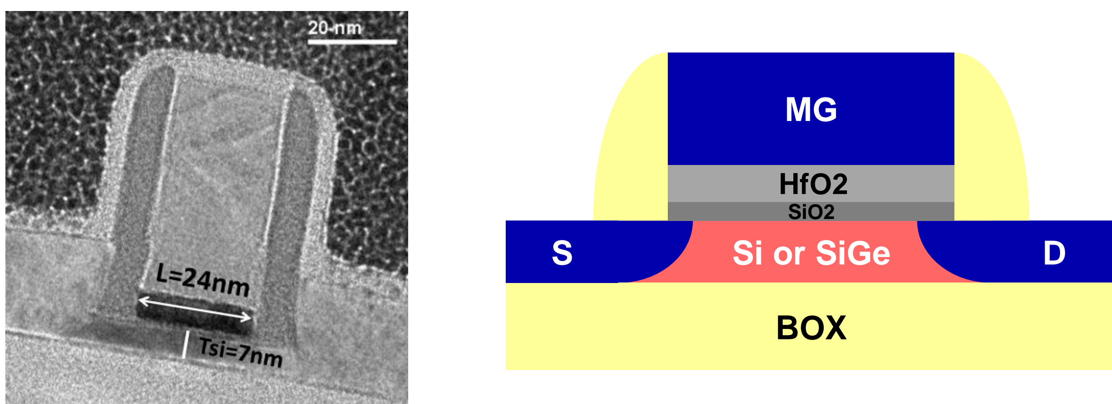


Figure 4.1 Cross-sectional TEM image and structure description of the tested devices.

The gate stack consists of a SiO_2 interfacial layer and a thin HfO_2 layer capped by a TiN metal gate. The gate oxide is directly formed on the top of the SiGe channel which means that we have no Si capping. For standard devices, called GO1, the nominal gate length is 28nm and the interfacial layer is thin (<1nm), while for GO2 transistors, the nominal gate length is 150nm for a V_{DD}=1.8V with the IL being much thicker (>2nm). To verify the integrity of HfO_2 after the Ge incorporation, we need to check the gate oxide using the HRTEM (High-Resolution TEM) method. Indeed, Figure 4.2 shows that the gate stack remains unaffected and confirms the presence of a thicker IL in GO2 devices.

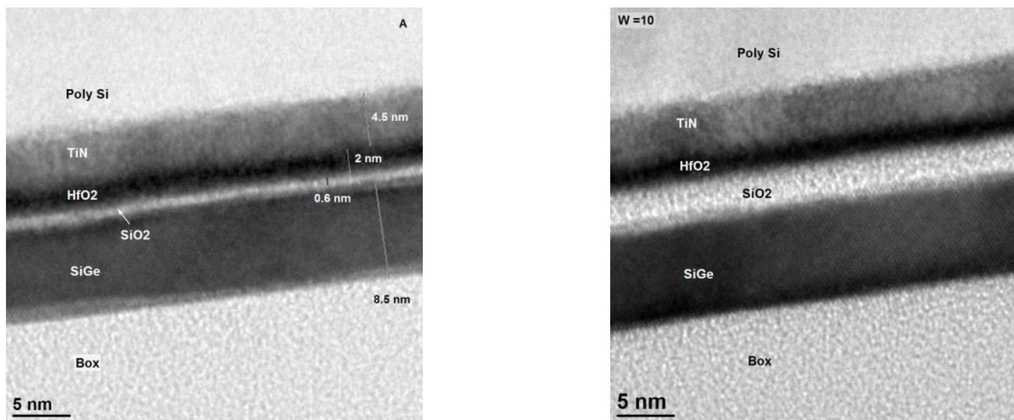


Figure 4.2 HRTEM results for (left) GO1 and (right) GO2 PMOSFETs showing their different process levels and the difference between the IL thickness.

Beside the two different device types, we also used two different types of nitridation standard and high, as we can see in Table 4.1 with the high one having an elevated nitrogen concentration as the name indicates.

Type	Channel Type	Type of Nitridation
Thin Oxide (GO1)	Ge: 0% - 17% - 27% - 31%	Standard
	Ge: 0% - 17% - 27% - 38%	High
Thick Oxide (GO2)	Ge: 0% - 17% - 27% - 31%	Standard
	Ge: 0% - 17% - 27% - 38%	High

Table 4.1 Different channels and Nitridation used for this study.

Starting as usual with the Capacitance-Voltage measurements, we want to verify the superior performance of Germanium for both thin and thick oxides. Plotting the C-V results of our measurements (Figure 4.3 & Figure 4.4), we first notice that the increase of Ge concentration causes a decrease of the threshold voltage, just as expected, with the highest value being up to 300mV for the 38% content, a consistent observation for the two device types. Later, we will see what this positive V_{TH} shift means. Fitting the data with Quantum-Mechanical modeling, we are able to extract the Equivalent Oxide Thickness (EOT), for both types of PMOSFETs. The EOT varies between 1 and 1.1nm for the GO1 and from 3 to 3.3 for the

GO2 transistors. The same model will be used in a next section of this Chapter to help us build the real band diagram of each structure, for the different Germanium concentrations.

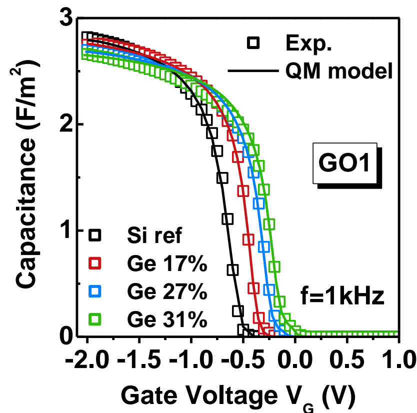


Figure 4.3 Capacitance-Voltage measurements and Quantum-Mechanical model fit for GO1 devices.

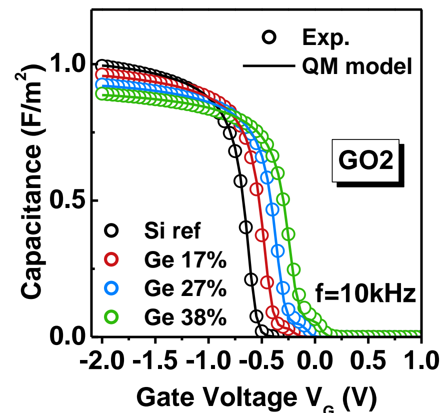


Figure 4.4 Capacitance-Voltage measurements and Quantum-Mechanical model fit for GO1&GO2 devices.

In addition to that, we use the Conductance-Voltage (GV) characteristics, modeled by our CV-GV simulator reported previously [146], to extract the interface state density (D_{IT}) on fresh devices. At this point, we have to mention that the estimated threshold voltage shift from the D_{IT} measurements assume a constant level throughout the bandgap which means that the conductance method evaluates the D_{IT} at a certain energy that could lead to an overestimation of the extracted, extrapolated to the entire bandgap, values. These values illustrated in Figure 4.5 show the increase of interface traps density with the Ge concentration [147]. Concerning the different nitridation types, the higher one seems to increase the interface state density as well. At the same time, comparing the thin and thicker oxides for the same Ge content and the same type of nitridation, we see a better interface quality for GO2 devices.

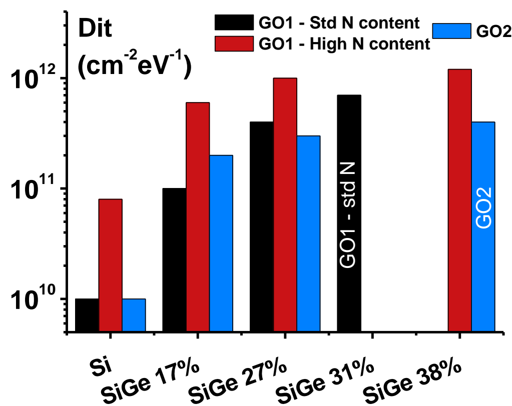


Figure 4.5 D_{IT} values extracted from the modeling of GV characteristics for Si and SiGe GO1 and GO2 PMOSFETs.

Since we have finished with the performance evaluation, we will move on to the reliability part. Two different test methodologies were applied for our investigation. For the first part, Time Dependent Defect Spectroscopy (TDDS), was used, on short channel devices at 125°C, to help us determine the impact of Ge on the individual traps. Over the years, studies have shown that transistors having a SiGe channel experience a particularly fast relaxation [148]. The Interface Layer (IL) traps have a very short emission time which makes them difficult to detect, so we must slow down the emission by performing the tests at a higher temperature than 25°C.

We performed this measurement with more than 60 devices per type tested, to obtain a statistical analysis of the results. After that, we will extend our study on long channel transistors by using fast Negative Bias Temperature Instability (NBTI) of 1µs range for 1ks, at different $V_{G,stress}$ and at T=125°C as before, in DC mode. The same fast technique (1us) was also used to avoid any relaxation in our transistors and to allow a cross-comparison between the different devices. Finally, for confidentiality reasons, some of the experimental results of this part will be presented in Arbitrary Units (A.U.).

4.3 Study on GO1 and GO2 short channel devices

We will begin the report of the experimental observations by the standard nitridation called ISSG (In Situ Steam Generator) and then, we will continue with the results of the higher one. Since we want to see if the extra layer that exists in GO2 is important or not for our conclusions, we will be discussing the results, for GO1 and GO2 PMOSFETs, at the same time from now on.

4.3.1 Standard nitridation

The Time Dependent Defect Spectroscopy (TDDS) method was used to help us evaluate the impact of Germanium on short channel transistors having the following dimensions: W=80nm/L=30nm for GO1 and W=160nm/L=100nm for GO2. A charging voltage is applied, at a constant V_D=-0.1V, for the filling of traps and then a switch to a lower discharging voltage to record the relaxation current. Since we know that the Ge incorporation will modify the threshold voltage of the PMOSFETs, compared to the Si reference, the selection of the discharging voltage was made according to the V_{TH} of each transistor type, in order to have the same current level (≈1µA) and, thus, an equivalent oxide field dependence. For the used setup conditions, we decided to set the minimum step height at 2.5mV. Already from the relaxation transients (e.g. for GO2) we can see the impact of Germanium on our devices. Looking at the current relaxation over time it is obvious that we have a decrease on the number of traced steps as we increase the fraction of Germanium in the channel (Figure 4.6).

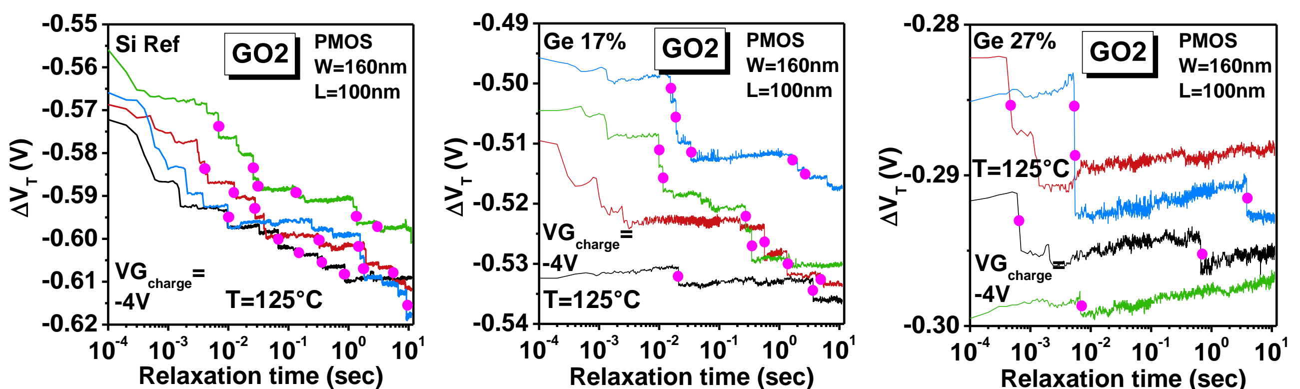


Figure 4.6 Relaxation transients of GO2 PMOSFETs for different Ge fractions (left) 0% (Si reference), (middle) 17% and (right) 27%.

We use these steps from the current transient to plot the Complementary Cumulative Distribution Function (CCDF), just like in the previous chapters, from which we obtain exponential distributions for all Ge contents and oxide thicknesses (Figure 4.7 & Figure 4.8). We

already know from previous publications [92]–[94] that, in FDSOI devices, this type of exponential distribution originates from the random position of the trapped charge within the gate oxide, from which we can extract the two aforementioned variables, η and N_T.

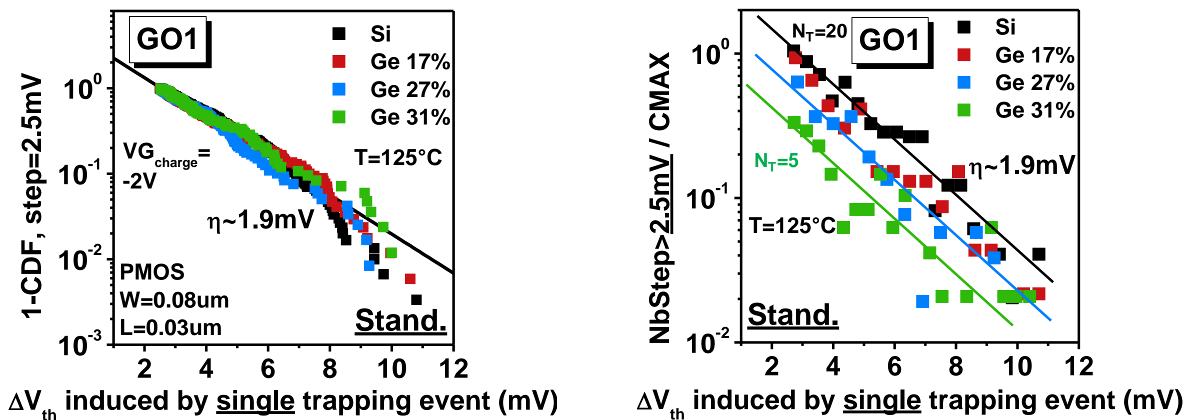


Figure 4.7 (left) Complementary Cumulative Distribution Function and (right) Histogram of the recorded steps for GO1 PMOSFETs on standard nitridation.

With a first glance, we see that the extracted η values agree, at a value of 1.9mV and 1.3mV for GO1 and GO2 respectively. In addition, this is obvious for all tested Ge contents in both device types. This indicates that the nature of the microscopic oxide defects remains the same and that the centroid of the trapped charge is not modified when we switch from Si to SiGe, even increasing the incorporation.

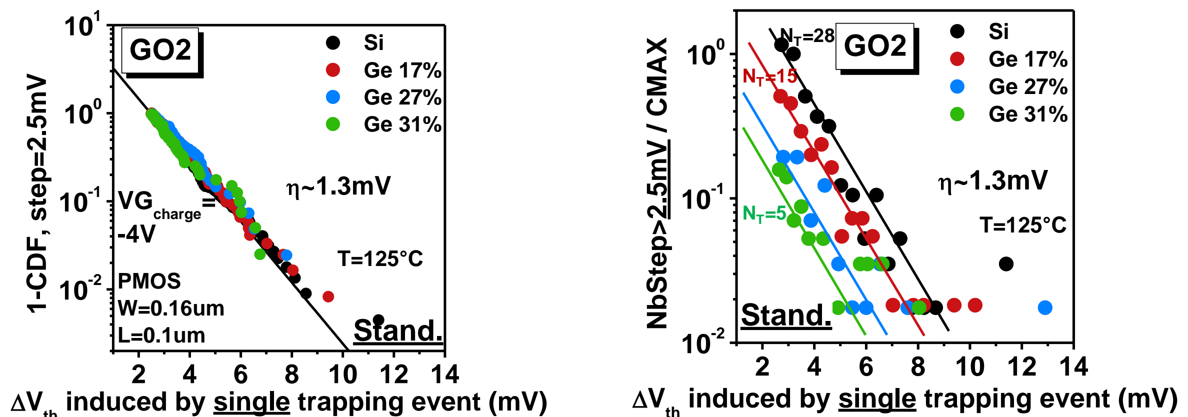


Figure 4.8 (left) Complementary Cumulative Distribution Function and (right) Histogram of the recorded steps for GO2 PMOSFETs on standard nitridation.

On the contrary the N_T values, extracted from the histograms, are impacted even by the lowest Ge content. N_T keeps decreasing as we increase the Ge incorporation, similarly for thin and thick oxides, a behavior already seen on thin oxides with Si capping and a SiGe channel [148], [149], but first time observed on thick oxide devices. An important hint that the traps responsible for NBTI trapping are very similar between GO1 and GO2 transistors.

4.3.2 High nitridation

The same data treatment and results evaluation are followed for the highest concentration of nitrogen, high nitridation as we will call it.

Although the average V_{TH} shift from a single defect seems unaffected by the higher nitridation (η remains the same), for the thin oxide transistors, plotting the histogram of traced steps shows otherwise (Figure 4.9). The use of nitrogen has increased the number of traps that caused a larger ΔV_{TH} (≈15 to 18mV), the tail of the distribution as it is known. Nonetheless, the positive impact of Ge incorporation remains intact and reduces again the average N_T.

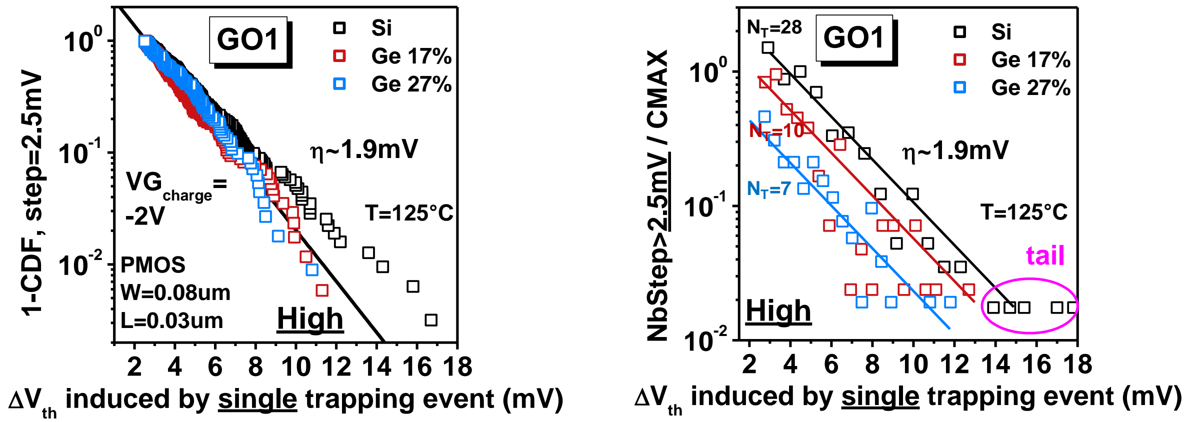


Figure 4.9 (left) Complementary Cumulative Distribution Function and (right) Histogram of the recorded steps for GO1 PMOSFETs under high nitridation.

To have a direct comparison of the η values between GO1 and GO2 devices, we normalize the raw η data by the charge sheet approximation value η_0 given by:

$$\eta_0 = \frac{q \cdot EOT}{\varepsilon_{ox} \cdot W \cdot L} \quad \text{Eq. 4.1}$$

with q being the electron charge, ε_{ox} the SiO_2 permittivity and W&L are the device width and length respectively (Figure 4.10). This is necessary, so that we take the EOT change into account as well as the device geometry. The fact that the ration η/η_0 is independent of the Ge concentration and close to 1, for both thin and thick IL oxides, suggests that the defects responsible for NBTI are identical regarding the nature and the spatial location in both types of gate stacks. The extracted N_T values that are also shown as a function of the Ge content, reveal the same decreasing trend with an increasing Germanium concentration for both standard and high nitridation.

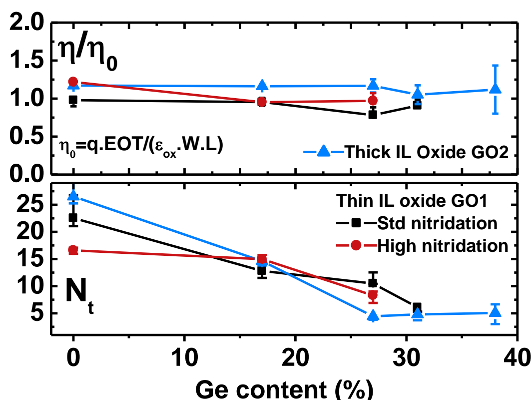


Figure 4.10 Extracted N_T (bottom) and η normalized by charge sheet approximation η_0 (top) as a function of Ge content for GO1 and GO2 PMOSFETs and both types of nitridation.

4.4 Study on GO1 and GO2 long channel devices

The next step is to evaluate the impact of Germanium on long channel GO1&GO2 PMOSFETs through standard DC NBTI measurements. Similar to the short channel part, we will first address the results for the standard nitridation and move on to the higher type, always making the comparison between thin and thick oxide devices.

4.4.1 Standard nitridation

We perform our standard fast range NBTI technique, already described before, using four different stress voltage for a period of 1000sec followed by the recovery part of 100sec at zero gate or drain bias voltage. Regarding GO1, we used the usual values of -1.4V /-1.6V /-1.8V /-2V, while for the GO2 it is necessary to rise the $V_{G, stress}$ (-3.4V /-3.6V /-3.8V /-4V) due to the thicker IL that exists in these devices. To have a straight comparison of the degradation, we compared the same gate length in both cases, L=1μm since it is the main factor that impacts the NBTI results when we talk about planar transistors [70], [92], [94].

Starting from the lowest Ge content (17%), we plot its NBTI dynamics compared to the Si reference (Figure 4.11 & Figure 4.12). The first obvious comment to make is that even this small amount of Germanium is sufficient enough to decrease the degradation on both thin and thick IL oxides. A behavior that is consistent with our results on short channel devices. Especially in the case of GO2, the obtained V_{TH} shift is almost half of the reference one. So, regardless the additional part that essentially "isolates" the HK layer, we have the same trend which could be an indication that we are talking about the same traps, the ones located in the IL.

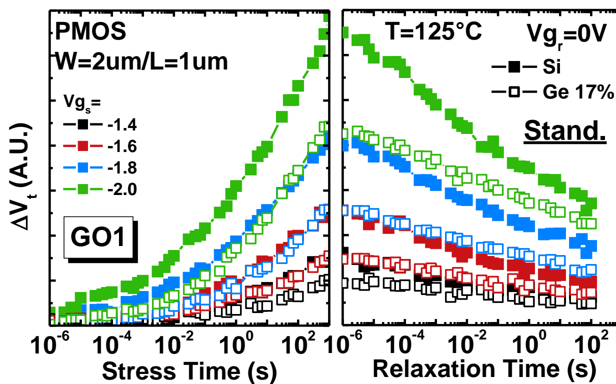


Figure 4.11 Stress and relaxation dynamics for the reference Si *thin* oxide PMOSFETs compared to the lowest Ge fraction (17%) with standard nitridation.

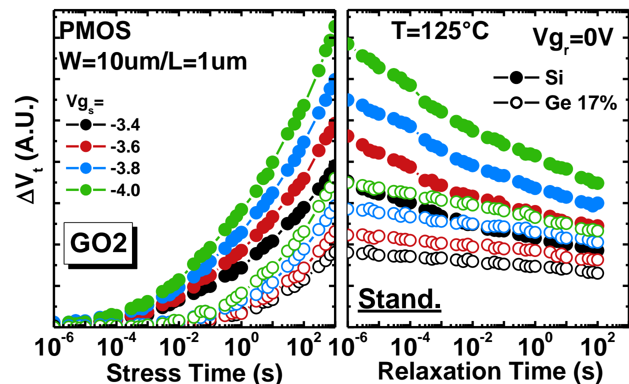


Figure 4.12 Stress and relaxation dynamics for the reference Si *thick* oxide PMOSFETs compared to the lowest Ge fraction (17%) with standard nitridation.

As we did in the TDDS on short channel devices, it is better to observe the oxide field dependence of NBTI, instead of $V_{G,\ stress}$, since the Germanium incorporation affects the threshold voltage of the transistors. Having that in mind, we confirm the previous results, by looking the oxide field dependence for the normalized NBTI shift. We divide the ΔV_{TH} values, of the different Ge contents, with the V_{TH} shift values obtained from the Si reference and observe that it remains constant for each Ge fraction (Figure 4.13) proving that we have the same oxide field dependence for GO1 and GO2. A proof that the additional thickness of GO2 PMOSFETs has no impact on the results. In the next part, we will also see the NBTI improvement at a specific oxide field value, for both types of transistors.

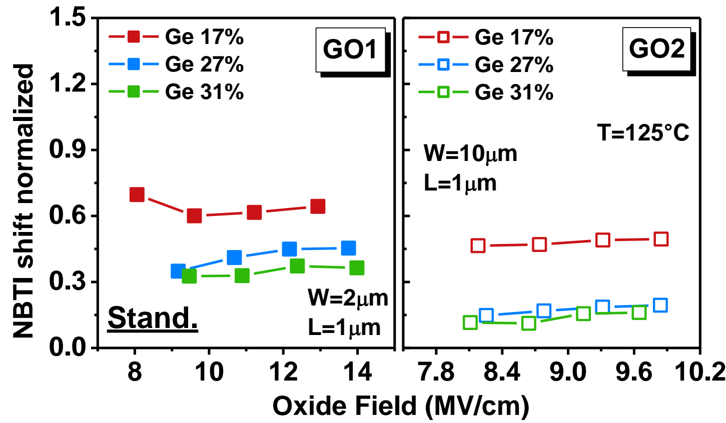


Figure 4.13 Normalized NBTI shift for GO1&GO2 transistors for different % of Ge having a standard nitridation.

4.4.2 High nitridation

For the Rapid Thermal Nitridation part, we will follow the same procedure as before studying the impact of a stronger type of nitridation (higher nitrogen content) on long channel transistors, again for different fractions of Germanium.

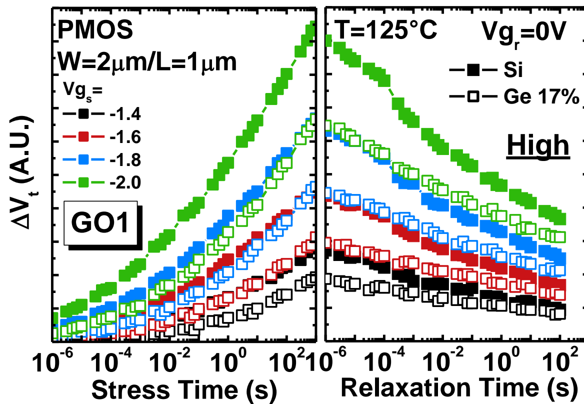


Figure 4.14 NBTI components of reference Si *thin* GO1&GO2 PMOSFETs compared to the lowest Germanium fraction (17%) having a strong nitridation.

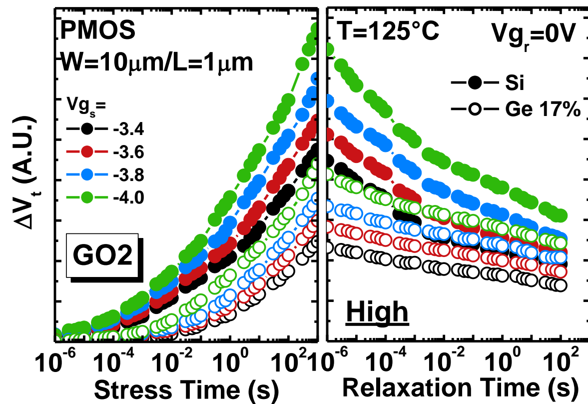


Figure 4.15 NBTI components of reference Si *thick* GO1&GO2 PMOSFETs compared to the lowest Germanium fraction (17%) having a strong nitridation.

We take a look at the typical NBTI evolution with time, for thin and thick oxide PMOSFETs (Figure 4.14 & Figure 4.15), and we see that SiGe shows, again, the same trend as for the standard nitridation. Incorporating even a small amount of Ge in the channel, improves significantly the V_{TH} shift during stress while the Si reference devices show a larger sensitivity to NBTI. This is verified for both thin and thick oxides being in agreement with the results on nanoscale transistors.

Plotting, again, the normalized NBTI shift w.r.t. the oxide field, the constant behavior for each fraction of Ge remains the same just like before (Figure 4.16). Of course, having a 38% of Ge in the channel improves even more the NBTI reliability which is obvious by the lower level of the shift, but again the same oxide field dependence is obtained.

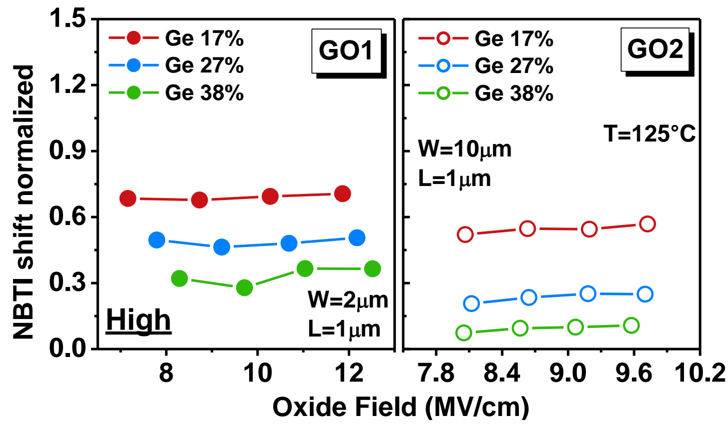


Figure 4.16 Normalized NBTI shift for GO1&GO2 transistors for different % of Ge having a high nitridation.

As mentioned before, we will compare the NBTI improvement for each type of nitridation w.r.t. the Germanium, always for both thicknesses. We make the comparison at the same oxide field chosen here at 9MV/cm, and we see that it is possible to achieve the same reliability boost as we increase the Ge in the channel following the same trend for both standard and high nitridation (Figure 4.17). The fact that the values are almost the same between GO1 and GO2, proves that the same type of traps are responsible for the existing degradation.

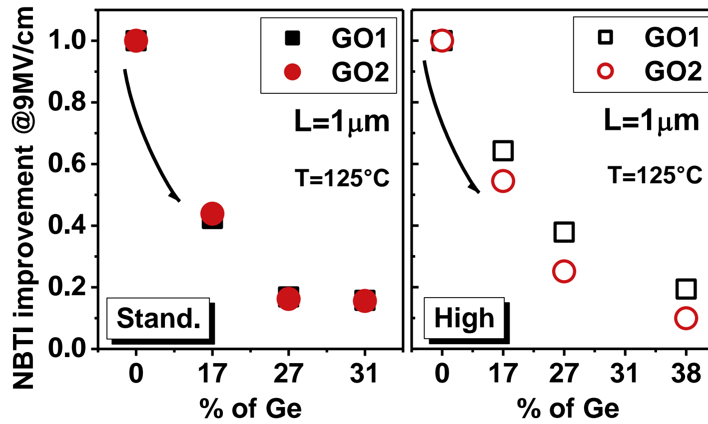


Figure 4.17 NBTI improvement at a constant oxide field (9MV/cm) for GO1&GO2 transistors and for both types of nitridation.

Fitting the Time-To-Failure for a V_{TH} shift of 50mV and a 10-year lifetime, we are able to extract some variables as we have seen before. One of them is the γ variable, the oxide field acceleration factor. Plotting the extracted values for all devices, as we can see in Figure 4.18, the value remains almost constant, varying from 5.4-5.6, with the exception of GO1 devices having a higher nitridation and where the value is around 5.2. The above observation indicates that despite the reduced level of degradation for the SiGe devices, the similar oxide field dependence shows the same interface bond breaking process regardless the use of Ge or not.

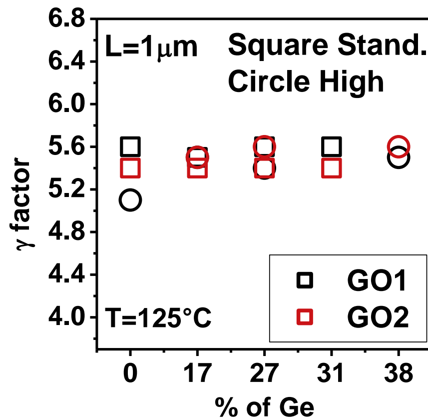


Figure 4.18 Extracted γ factor after Time-To-Failure fit compared for thin and thick oxides and both types of nitridation.

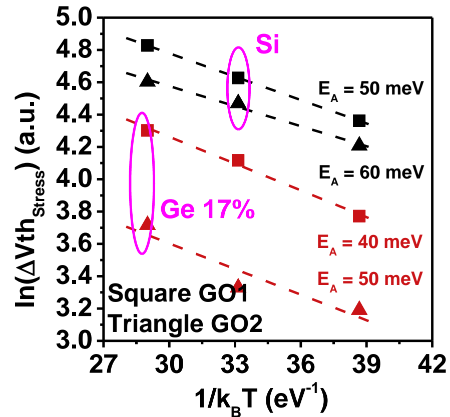


Figure 4.19 Activation energy extraction for thin and thick IL oxides and two types of nitridation.

An extra step to verify our theory is to perform the same NBTI measurements, using the same parameters, but for different temperatures: 25°C and 75°C in addition to the 125°C already shown. This will allow us to extract the activation energy for the highest used $V_{G,\ stress}$ in each case: -2V for the GO1 and -4V for the GO2 PMOSFETs (Figure 4.19). Comparing the resulting values, it is evident that the difference between thin and thick oxide, comparing the two different channel materials, is low around 10meV. At the same time, their individual values are very close to the typically reported range [63]. We already know that NBTI degradation is activated with temperature, finding similar values adds an extra proof that we are talking about the same traps.

From the C-V data of Section 4.2, we obtained not only the Equivalent Oxide Thickness (EOT), but also the flatband voltage shift (ΔV_{fb}) for all devices. Along with the extracted interface trap density (D_{IT}) of each transistor type, we are able to build the band diagrams for the reference Si (GO1&GO2 devices) and compare them with the higher fraction of Ge (38%) (Figure 4.20). For consistency, we choose again the oxide field of 9MV/cm, just like for the NBTI. If we look at the Fermi level difference between Si an SiGe devices, we see that the same value is obtained, 0.2294eV, for both thin and thick oxide. This confirms our approach that we are looking at the same traps, in both cases, despite the additional layer of GO2 transistors and that the possible favorable alignment of the Fermi level with respect to the energy levels of the oxide defects, of the Germanium, does not include the HK defects.

So, if it is not the HK defects that improve the NBTI reliability, what is? It was shown before that the Germanium incorporation causes a positive shift of the V_{TH} that reaches a maximum of 300mV for the highest fraction (Figure 4.3 & Figure 4.4). At the same time, as we move from 17% to 38% there is an increase in the interface state density (Figure 4.5) for the thin and thick transistor types. This indicates that besides the bandgap narrowing, there could be negatively charged traps that contribute to the robustness of SiGe PMOSFETs [150] as has been seen in the literature. Their high density and the fact that they are close to the valence band, cause a lowering of the oxide field that reduces the NBTI degradation, despite the poor interface quality

when it comes to Ge incorporation. Published simulation results [151] have shown that these acceptor-like traps develop a large buildup of negative charges that shift positively the transistors, just like in our case.

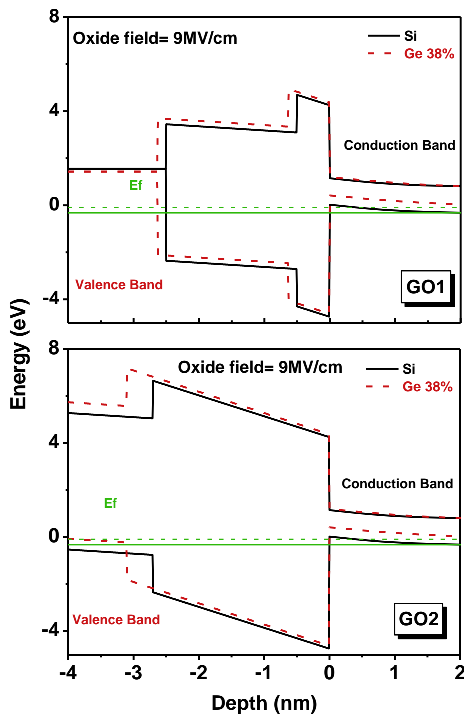


Figure 4.20 Energy band diagrams for GO1 (top) and GO2 (bottom) constructed according to the individual transistor characteristics (EOT, ΔV_{fb}, D_{IT} etc.) under the same oxide field.

Both of these indications have not been taken into account in previously related works [148], [152]. The fact that we acquire the same trends for GO1&GO2 PMOSFETs are a clear suggestion that this effect occurs regardless the IL thicknesses, so the same acceptor-like traps are responsible for the improved reliability. Even though, this additional amount of fixed charges is impacting the mobility, hence the performance, the NBTI tolerance is worth taking this risk if it is to overcome reliability limitations in the CMOS journey.

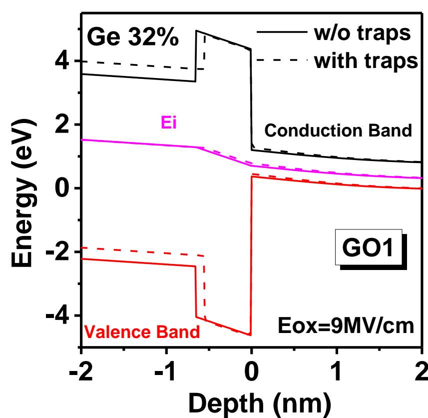


Figure 4.21 Impact of channel trap density in the energy band diagram of a *thin* oxide transistor with a high Ge concentration.

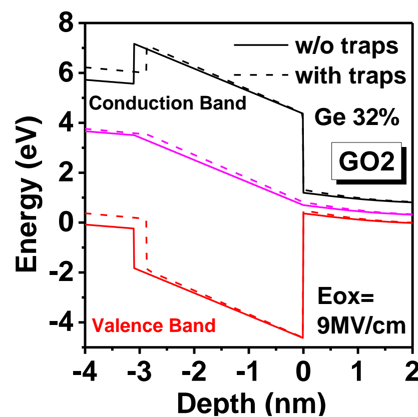


Figure 4.22 Impact of channel trap density in the energy band diagram of a *thick* oxide transistor with a high Ge concentration

Summarizing the results of the chapter, the advantages of Ge incorporation in the channel in terms of reliability have been studied, trying to identify the defects that are responsible for it. Comparing thin and thick IL PMOSFETs through different characterization techniques reveal the same trends despite the increased thickness of the GO2 that helps us isolate the HK. This confirms our feeling that in both transistor types, the same traps are involved in the degradation mechanisms impacting the reliability of the devices. This comes in contradiction to the popular belief that it is due to HK defects, but in consensus with the presence of acceptor-like traps near the valence band.

General conclusions

In Chapter 1 of this thesis, an overview of the advancements in semiconductor industry has been presented. New channel materials, 3D architectures and integration schemes have been introduced towards the “More Moore” and “More than Moore” era, trying at the same time to solve the problems created by the scaling. The advancements in the CMOS route come with the price of additional defects that need the proper techniques to be characterized, described in detail there. Revealing the physical mechanisms behind these trapping phenomena and with the help of models, we are able to set the reliability requirements for each technology.

In Chapter 2, we focused on the 3D architectures, specifically the Trigate nanowires. At the beginning, we studied their impact on the dynamic variability, looking at their geometry dependence. The gate width appeared to be the most critical factor on the results and the t_{Si} having minor effect, when the gate length shows uncertain conclusions. In addition to that, for the gate length and due to its doubtful results, an extensive study with the most widely used trap extraction techniques was presented. Comparing RTN and TDDS, on short channel PMOSFETs, we saw a trap detection agreement of a minimum 55%, with both methods revealing also a bimodal distribution coming from the impact of defects in the Buried Oxide. After stress, comparing each method individually with the before stress results, the TDDS appears less impacted by the applied stress time and voltage while RTN even experiences a loss of information, possibly due to the stochastic nature of defects in deeply scaled transistors that are dependent on the experimental window each time. Even though both techniques can be used to study the same phenomena, TDDS has proven to be more advantageous in terms of measurement time, flexibility and data treatment, verifying its already known leverage even for this type of advanced structure.

In Chapter 3, the 3D sequential integration study was presented in two parts. In the first one, the effort to “simulate” the Top-Level device, has led to a lower thermal budget that appears to be the main concern in the reliability part. For PMOSFETs, the Interfacial Layer of both thin and thick oxides is degrading for lower temperatures. On the contrary, NMOSFETs remain less affected by the low thermal budget and each time the reliability criteria are passed. But the 3D sequential integration does not only include the low TB, there are also different process steps that need evaluation and optimization. The HK Nitridation, the Post Nitridation Anneal temperature and the Forming gas anneal are the three major process steps that have been studied on PMOSFETs. All of them are already known in the standard high temperature process, but evaluated, now, for low TB. The Nitridation shows no significant gain in the performance of the transistors and degrades more their reliability, whether it is in N_2 or N_2/H_2 form. The Post Nitridation Anneal temperature variation shows no difference between 600°C and 525°C. The fact that PNA is an additional anneal, during the process flow, does not seem to improve the reliability, an indication that the dopant activation temperature is the main issue when it comes to the degradation caused by temperature. This gives us the opportunity to lower even more the thermal budget of the 3D sequential integration. The last process step, the Forming gas anneal using high-pressure deuterium appears very promising regarding both performance and reliability, with the phenomena lying behind it to be still in debate around the

research community. In the second part of this chapter, both levels of an actual 3D scheme were studied for the first time. In terms of performance, after a set of extensive measurements, it is clear that the Bottom-Level N&PMOSFETs are not impacted by a Top-Level processing verifying the stability and superiority of the existing and mature technology. The Top-Level transistors appear to have a good enough performance that can be improved using the aforementioned process steppingstones. For the reliability part, again the Bottom-Level shows no additional degradation due to the TL processing and at the same time, the Top-Level devices are very close to the BL counterparts, passing the reliability requirements for the first time. Finally, the 3D scheme was evaluated in a circuit level, testing an inverter fabricated with a PMOSFET on the top and a NMOSFET on the bottom level with separate contact and a common drain configuration. Using the characteristics of the individual devices, we were able to build a SPICE-like model to reproduce it V_{IN}-V_{OUT} characteristics for different V_{DD}. The model allows us to tune our technology and use the right threshold voltage, for the bottom NMOS and top PMOS transistor, in order to achieve the desirable inverter performance in terms of switching bias and dissipated power each time. Furthermore, stressing the inverter and introducing the resulted threshold voltage shifts of both transistors to the model, we can perfectly fit the voltage and current drifts over time. This confirms our approach that by combining a SPICE-like and NBTI modeling, we are able to predict the ageing of 3D sequential circuits.

In the last part of the thesis, Chapter 4, the impact of Ge incorporation in the channel regarding reliability was presented. It has already been verified by many publications that when it comes to germanium there is an improved degradation on PMOSFETs and here, we went to an in-depth reliability characterization of the traps responsible for it, comparing thin and thick IL planar devices through a series of measurement methods, both on large and small area devices and for two types of nitridation. Regarding performance, even though there are no large variations in the EOT extraction, the C-V and conductance results show a positive shift of the threshold voltage and an increasing value of interface state density, respectively, w.r.t. the increasing Ge concentration. A result verified for GO1&GO2 as well as Standard and High type of nitridation. For the t_0 reliability, on short channel devices, there is no modification of the traps' depth, only a decrease of the extracted average number of defects, for the different Ge contents. Again, showing the same trend for thin and thick IL PMOSFETs and the two nitridation types. Performing DC NBTI measurements for different temperatures, on long channel devices, we verify the improved degradation with an increasing Ge concentration and are able to calculate the activation energy in each case showing the agreement of results between GO1&GO2 transistors. Building the band diagrams for both of them at a high oxide field (9MV/cm), using the results of the performance part, indicate the same Fermi level difference between Si and SiGe devices on both thicknesses. The fact that there is a global consistency, for thin and thick ILs, confirms our approach that we are looking at the same traps in both transistor types and that the additional layer of GO2 transistors is not affecting the results. The HK defects are not contributing to the improved reliability of SiGe channels. Based on our results and previously reported evidence, the explanation tends to be more on the existence of high-density acceptor-like traps near the valence band that lower the oxide field causing a more robust reliability for SiGe transistors, verifying also the positive V_{TH} shift due to the buildup of negative charges.

As a general conclusion, the Front End Of the Line (FEOL) reliability is the major concern to ensure the long-lasting operation of modern electronics that has just started to be explored. With the continuous scaling, each technology "suffers" from newly created defects that degrade the transistors' performance along with the increased variability that has to be considered in the existing or future prediction models. Moreover, the lack of inclination concerning the origin of BTI shows that there still a lot to be understood from the physics point of view and the need for accurate characterization methods to be followed towards it.

Future work

Regarding the continuation of this work in the near future, we suggest, first of all, the investigation of the Time Dependent Defect Spectroscopy (TDDS) versus Random Telegraph Noise (RTN), presented in Chapter 2, on different $V_{G,\,sense}$ and temperatures in order to extend the existing study and acquire more knowledge on their comparison. In the same way, the correlation of their emission time constants will provide a deeper insight on the characteristics of recorded traps each time, as well as the application of longer stress times can reveal a different stress impact, mainly, on the number of detectable traps but also on the extracted drain current fluctuation level.

As has been described in Chapter 3, there are several process knobs under study in order to improve the performance of the 3D sequential integration. All these different processing steps should be also evaluated in terms of reliability, pushing this technology on becoming more mature and eventually being integrated into everyday electronics.

Finally, in addition to the 3D sequential integration, stacked nanowires and alternative channel materials, such as III-V semiconductors, 2D materials or Carbon nanotubes (CNT), are currently being investigated for the next generation of transistors. For all of them, reliability is still an uncharted territory and the application of the described characterization methods in this thesis, should be a first step towards its preliminary results.

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Caractérisations électriques et modélisation des phénomènes de piégeages affectant la fiabilité des technologies CMOS avancées (Nanofils) 10nm

Dans les technologies CMOS avancées, les défauts microscopiques localisées à l'interface Si (N_{it}) ou dans l'oxyde de grille (N_{ox}) dégradent les performances des transistors CMOS, en augmentant le bruit de basse fréquence (LFN). Ces défauts sont généralement induits par le processus de fabrication ou par le vieillissement de l'appareil sous tension électrique (BTI, porteurs chauds). Dans des transistors canal SiGe ou III-V, leur densité est beaucoup plus élevée que dans le silicium et leur nature microscopique est encore inconnue. En outre, en sub 10 nm 3D comme nanofils, ces défauts répartis spatialement induisent des effets stochastiques typiques responsables de la “variabilité temporelle” de la performance de l'appareil. Cette nouvelle composante dynamique de la variabilité doit maintenant être envisagée en plus de la variabilité statique bien connu pour obtenir circuits fonctionnels et fiables. Aujourd'hui donc, il devient essentiel de bien comprendre les mécanismes de piégeage induites par ces défauts afin de concevoir et fabriquer des technologies CMOS robustes et fiables pour les nœuds de sub 10 nm.

Mots - clés: Nanofils, bruit, piégeages, CMOS avancés, intégration 3D séquentielle

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Electrical characterization & modeling of the trapping phenomena impacting the reliability of nanowire transistors for sub 10nm nodes

In advanced CMOS technologies, microscopic defects localized at the Si interface (N_{it}) or within the gate oxide (N_{ox}) degrade the performance of CMOS transistors, by increasing the low frequency noise (LFN). These defects are generally induced by the fabrication process or by the ageing of the device under electrical stress (BTI, Hot Carriers). In SiGe or III-V channel transistors, their density is much higher than in silicon and their microscopic nature still is unknown. In addition, in sub 10nm 3D like nanowires, these spatially distributed defects induce typical stochastic effects responsible for “temporal variability” of the device performance. This new dynamic variability component must now be considered in addition of the well-known static variability to obtain functional and reliable circuits. Therefore, today it becomes essential to well understand the trapping mechanisms induced by these defects in order to design & fabricate robust and reliable CMOS technologies for sub 10nm nodes.

Key words: Nanowires, noise, traps, advanced CMOS, 3D sequential integration

Résumé en français

Au Chapitre 1 de cette thèse, un aperçu des progrès de l'industrie des semiconducteurs a été présenté. Les nouveaux matériaux utilisés pour les canaux, les architectures 3D et les schémas d'intégration introduits vers les ères «More Moore» et «More than Moore», ont été décrits. Les progrès réalisés dans la voie CMOS vont de pair avec l'apparition de nouveaux défauts dont l'étude nécessite l'utilisation de techniques avancées, décrites en détail dans cette section. En dévoilant les mécanismes physiques responsables de ces phénomènes de piégeage, nous pouvons définir, à l'aide de modèles de dégradation, les exigences de fiabilité pour chaque technologie.

Au Chapitre 2, nous nous sommes concentrés sur les architectures 3D, en particulier les nanofils de type Trigate. L'impact des nanofils sur la variabilité dynamique a été étudié en termes de variations géométriques. La largeur de la grille semble être le facteur le plus critique alors que l'épaisseur du silicium a un effet mineur. Enfin, l'impact de la longueur de la grille est incertain. Une étude approfondie des pièges par les méthodes RTN et TDDS est également présentée. En comparant ces méthodes sur les PMOSFET au canal court, nous avons constaté un accord de détection des pièges de 55% minimum. Ces deux méthodes révélant également une distribution bimodale provenant de l'impact des défauts dans l'oxyde enterré (BOX). En appliquant du stress électrique pour comparer chaque méthode individuellement avec les résultats initiaux, la TDDS apparaît moins impactée par le temps de stress appliqué et la tension. A l'opposé, la méthode RTN subit même une perte d'informations, probablement due à la nature stochastique des défauts dans les transistors dont la détection dépend de la fenêtre expérimentale. Même si les deux techniques peuvent être utilisées pour étudier les mêmes phénomènes, la TDDS s'est avérée plus avantageuse en termes de temps de mesure, de flexibilité et de traitement des données, vérifiant son effet de levier déjà connu, même pour ce type de structures avancées.

Au Chapitre 3, l'étude d'intégration séquentielle 3D était présentée en deux parties. Dans le premier cas, l'effort de «simulation» du transistor du niveau supérieur a entraîné une réduction du budget thermique, ce qui semble être la principale préoccupation de la partie fiabilité. Pour les PMOSFET, la couche interfaciale d'oxydes minces et épais se dégrade aux températures plus basses. Au contraire, les NMOSFET sont moins affectés par le faible budget thermique et à chaque fois les critères de fiabilité sont satisfaits. Mais l'intégration séquentielle 3D n'inclut pas seulement le faible budget thermique mais également différentes étapes de process qui nécessitent une évaluation et une optimisation. Pour les PMOSFET, la nitruration du diélectrique high-k, la température de recuit après la nitruration et le recuit sous gaz de formage sont les trois principales étapes du process qui ont été étudiées. Toutes sont déjà connues dans le procédé standard à haute température, mais sont maintenant évaluées pour un budget thermique bas. La nitruration ne montre aucun gain significatif par rapport à la performance des transistors et dégrade davantage leur fiabilité, que ce soit sous forme N_2 ou N_2/H_2. La variation de température après le recuit de nitruration ne montre aucune différence entre 600°C et 525°C. Le fait que le recuit post nitruration soit un recuit supplémentaire au cours du processus ne semble pas améliorer la fiabilité, ce qui indique que la température

d'activation du dopant est le principal problème en ce qui concerne la dégradation causée par la température. Cela nous donne la possibilité de réduire encore plus le budget thermique de l'intégration séquentielle 3D. La dernière étape du process, le recuit de gaz de formage utilisant du deutérium à haute pression, semble très prometteuse en termes de performances et de fiabilité mais nécessite une étude approfondie afin de conclure définitivement. Dans la deuxième partie de ce chapitre, les deux niveaux d'un schéma 3D réel ont été étudiés pour la première fois. En termes de performances, après un ensemble de mesures poussées, il est clair que les transistors N&PMOSFET de niveau inférieur ne sont pas affectés par l'integration du niveau supérieur, vérifiant la stabilité et la supériorité de la technologie existante. Les transistors du niveau supérieur semblent avoir une performance suffisante qui peut être améliorée en optimisant les étapes de process mentionnées précédemment. Pour ce qui concerne la fiabilité, encore une fois, le niveau inférieur ne montre aucune dégradation supplémentaire due à l'intégration du niveau supérieur. Dans le même temps, les dispositifs de niveau supérieur sont très proches de leurs homologues du niveau inférieur, satisfaisant ainsi les exigences de fiabilité pour la première fois. Enfin, le schéma 3D a été évalué au niveau du circuit, en testant un inverseur fabriqué avec un PMOSFET intégré au-dessus d'un NMOSFET, avec un contact séparé et une configuration de drain commun. En utilisant les caractéristiques des dispositifs individuels, nous avons pu créer un modèle de type SPICE afin de reproduire les caractéristiques V_{IN}-V_{OUT} pour différents V_{DD}. Ce modèle nous permet d'ajuster notre technologie et d'utiliser la tension de seuil appropriée pour le transistor NMOS inférieur et le transistor PMOS supérieur, afin d'obtenir les performances optimales de l'inverseur en termes de polarisation et de puissance dissipée. De plus, en stressant l'inverseur et en introduisant les décalages de tension de seuil résultants des deux transistors dans le modèle, nous pouvons parfaitement adapter la dérive en tension et en courant en fonction du temps. Cela confirme qu'avec notre approche combinant une modélisation SPICE et une modélisation NBTI, il est possible de prédire le vieillissement des circuits séquentiels 3D.

Dans la dernière partie de la thèse, le Chapitre 4, l'impact de l'incorporation de Germanium dans le canal en matière de fiabilité a été présenté. De nombreuses publications ont déjà vérifié que, dans le cas du germanium, la fiabilité des PMOSFET était améliorée. Dans notre cas, nous avons procédé à une étude détaillée des pièges qui sont responsables pour la dégradation, en comparant les dispositifs planaires d'un couche d'oxyde interfaciale IL mince (GO1) et épais (GO2) au travers d'une série de techniques de caractérisation; à la fois sur des dispositifs de grande et de petite superficie et sur deux types de nitruration. En ce qui concerne les performances, bien qu'il n'existe pas de variations importantes dans l'extraction EOT (pour Equivalent Oxide Thickness), les résultats C-V et de conductance montrent un décalage positif de la tension de seuil et une valeur croissante de la densité d'états de l'interface, pour une concentration croissante de Ge. Un résultat vérifié pour GO1 et GO2 ainsi que pour le type de nitruration standard et pour la plus forte concentration d'azote. Concernant la fiabilité t_0, sur les dispositifs au canal court, il n'y a pas de modification de la profondeur des pièges, mais seulement une diminution du nombre moyen de défauts extraits, pour les différentes concentrations en Ge. Encore une fois, montrant la même tendance pour les PMOSFET IL minces et épaisses et les deux types de nitruration. En effectuant des mesures DC NBTI à différentes températures, sur des dispositifs au canal long, nous observons que la dégradation

est améliorée pour une concentration croissante en Ge et il est possible de calculer l'énergie d'activation dans chaque cas en montrant la concordance des résultats entre les transistors GO1 et GO2. La construction des diagrammes de bande pour les deux dispositifs à un champ d'oxyde élevé (9MV/cm), en utilisant les résultats de la partie performance, indique la même différence du niveau de Fermi entre les dispositifs Si et SiGe sur les deux épaisseurs. Le fait qu'il y ait une cohérence globale, pour les oxydes interfaciales, minces et épaisses, confirme que les mêmes pièges sont observés dans les deux types de transistors et le fait que la couche supplémentaire de transistors GO2 n'affecte pas les résultats. Les défauts de HK ne contribuent pas à l'amélioration de la fiabilité des canaux SiGe. Sur la base de nos résultats et des preuves rapportées précédemment, l'explication tend à être davantage basée sur l'existence d'une forte densité de pièges de type accepteur près de la bande de valence qui abaissent le champ d'oxyde, ce qui entraîne une amélioration de la fiabilité pour les transistors SiGe, expliquant également le décalage V_{TH} positif en raison de l'accumulation de charges négatives.

En conclusion générale, la fiabilité est un aspect très important pour assurer le fonctionnement durable de l'électronique moderne qui vient d'être explorée. Avec la diminution des dimensions qui continue, chaque technologie «souffre» de nouveaux défauts créés qui dégradent les performances des transistors, ainsi que de la variabilité accrue à prendre en compte dans les modèles de prévision existants ou futurs. De plus, le manque d'accord concernant l'origine du BTI montre qu'il reste encore beaucoup à comprendre du point de vue physique et qu'il est nécessaire de suivre des méthodes de caractérisation précises.

Perspectives

En ce qui concerne la poursuite de ces travaux dans l'avenir proche, on suggéra tout d'abord d'étudier la technique du TDDS par rapport au RTN en fonction du temps, présentée au Chapitre 2, avec des variations des paramètres $V_{G,\ sense}$ et de la température, afin d'étendre l'étude existante et d'acquérir plus de connaissances pour leur comparaison. De la même manière, la corrélation de leurs constantes de temps d'émission fournira un aperçu plus détaillé des caractéristiques des pièges détectés, alors que l'application de temps de stress plus longs pourra influencer le nombre de pièges détectables, mais aussi le niveau de fluctuation du courant de drain extrait. Comme cela a été décrit au Chapitre 3, plusieurs étapes de process sont à l'étude afin d'améliorer les performances de l'intégration séquentielle 3D. Toutes ces différentes pistes de traitement doivent également être évaluées en termes de fiabilité, ce qui poussera cette technologie à devenir plus mature et à être éventuellement intégrée à l'électronique quotidienne. Enfin, outre l'intégration séquentielle 3D, des nanofils empilés et des matériaux de canaux alternatifs, tels que des semi-conducteurs III-V, des matériaux 2D ou des nanotubes de carbone (CNT), sont actuellement à l'étude pour la prochaine génération de transistors. Pour tous, la fiabilité reste un territoire inconnu et l'application des méthodes de caractérisation décrites dans cette thèse devrait constituer un premier pas vers ses résultats préliminaires.