Contribution to the study of the SiC MOSFETs gate oxide

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Abbreviations and Acronyms

3-C 3-C SiC polytype.

4-H 4-H SiC polytype.

6-H 6-H SiC polytype.

ABS Antilock Braking System.

AC Alternative Current.

BFM Baliga Figure of Merit.

BHFFM Baliga High Frequency Figure of Merit.

BJT Bipolar Junction Transistor.

BPD Basal Plane Dislocation.

BTI Bias Temperature Instability.

C Cubic.

CMB Chopper Mode Bias.

CVD Chemical Vapor Deposition.

DC Direct Current.

DLTS Deep Level Transient Spectroscopy.

DMOSFET Double-Implanted Metal Oxide Semiconductor Field-Effect Transistor.

DUT Device Under Test.

ED Edge Dislocation.

EHA Electro-Hydraulic Actuator.

EMA Electro-Mechanical Actuator.

EMC Electromagnetic Compatibility.

EMI Electromagnetic Interference.

ESP Electronic Stability Program.

EV Electric Vehicle.

FoM Figure of Merit.

GaN Gallium Nitride.

Gen1 1st Generation.

Gen2 2nd Generation.

Gen3 3rd Generation.

Gen4 4th Generation.

GTO Gate Turn-off Transistor.

H Hexagonal.

HTGB High Temperature Gate Bias.

HTGS High Temperature Gate Switching.

HTRB High Temperature Reverse Bias.

HV High Voltage.

HVDC High Voltage Direct Current.

IGBT Insulated Gate Bipolar Transistor.

JEDEC Joint Electron Device Engineering Council.

JFET Junction Field-Effect Transistor.

JFM Johnson Figure of Merit.

KFM Keyes Figure of Merit.

LPE Liquide-Phase Epitaxy.

MEA More Electric Aircraft.

MOSFET Metal Oxide Semiconductor Field-Effect Transistor.

MP Micropipe.

NBTI Negative Bias Temperature Instability.

PBTI Positive Bias Temperature Instability.

PCB Printed Circuit Board.

R Rhomboidal.

ROHM ROHM Semiconductorg.

SCR Silicon Controller Rectifier.

SF Stacking Faults.

SiC Silicon Carbide.

SOFC Solid Oxide Fuel Cell.

ST STMicroelectronics.

TDDB Time Dependent Dielectric Breakdown.

TED Threading Edge Dislocation.

TRIAC Triode for Alternating Current.

TSD Threading Screw Dislocation.

TSP Thermo-sensitive Parameter.

U-MOSFET Trench gate MOSFET.

VD-MOSFET Vertical Diffused MOSFET.

VJFET Vertical JFET.

VPE Vapour-Phase Epitaxy.

ZVS Zero Voltage Switching.

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Résumé

Les MOSFET en SiC sont appelées à remplacer les IGBT en silicium pour des applications demandant une plus forte vitesse de commutation. Cependant, les MOSFET en SiC ont encore quelques problèmes de fiabilité, tels que la robustesse de la diode interne ou bien la robustesse de l'oxyde de grille. Cette dernière est liée à l'oxyde de grille des composants de type MOSFET. Des instabilités de la tension de seuil sont aussi signalées. Cette thèse aborde ces deux sujets sur les MOSFET commerciaux 1200 V.

L'étude de la diode interne met en évidence que les caractéristiques I-V (de la diode intrinsèque) demeurent stables après l'application d'un stress. Cependant, une dérive surprenante de la tension de seuil apparaît. Des tests complémentaires, en stressant le canal à la place de la diode, avec les mêmes contraintes n'ont pas montré de dérive significative de la tension de seuil. Donc, l'application d'un stress en courant quand le composant est en mode d'accumulation semble favoriser l'apparition des instabilités de la tension de seuil.

La robustesse de l'oxyde de grille concerne les instabilités de la tension de seuil, mais aussi l'estimation de la durée de vie dans des conditions de fonctionnement nominales.

Les résultats obtenus montrent que la durée de vie de l'oxyde de grille n'est plus un problème. Pourtant, le suivi du courant de grille pendant les tests ainsi que les caractérisations de la capacité de grille mettent en évidence des déplacements de la courbe C(V) à cause de phénomènes d'injection des porteurs et de piégeage, mais aussi la possible présence d'ions mobiles.

L'analyse des dégradations et dérives liées à l'oxyde de grille doit être poursuivie plus profondément.

Abstract

SiC power MOSFETs are called to replace Si IGBT for some medium and high power applications (hundreds of kVA). However, even if crystallographic defects have been drastically reduced, SiC MOSFETs are always concerned by some robustness issues such as the internal diode robustness or the robustness of the gate oxide. The last one especially affects MOSFETs devices and is linked to the apparition of instabilities in the threshold voltage. This thesis focuses on these two issues.

The study of the internal diode robustness highlighted that the I-V curve (of the intrinsic diode) remains stable after the application of a current stress in static mode, but also with the DUT placed in a converter with inductive switchings. These are the most stressful conditions. However, a surprising drift in the threshold voltage has been observed when some devices operates under these conditions; in static mode or in a converter. Complementary tests stressing the channel instead of the internal diode in the same temperature and dissipated power, have not resulted in a drift of the threshold voltage. Thus, the application of a current stress when the device is in accumulation regime could favour the apparition of instabilities in the threshold voltage.

The study of the gate oxide focus in the instabilities of the threshold voltage, but also on the expected lifetime of the oxide at nominal conditions.

Results obtained shown that the expected lifetime (TDDB) of the oxide is no longer a problem. Indeed, tests realized in static mode, but also in a converter under inductive switching conditions resulted in expected lifetimes well above 100 years. However, the monitoring of the gate current during the test and gate capacitance characterizations C(V) highlighted a shift in the capacitance due to carrier injection and trapping phenomena and probably to the presence of mobile-ions.

Still regarding the instabilities of the threshold voltage, classic tests resulted in no significant variations of the threshold voltage at 150 °C. However, at 200 °C the drift observed for some manufacturers is higher than +30%. This is unacceptable for high-temperature applications and evidence that the quality of the gate oxide and the SiC/SiO_2 interface must continue to be improved, together with the manufacturing methods to minimize the presence of mobile ions in the substrate.

General Introduction

Human societies and electricity have evolved together since the end of 19^{th} century. Inventions such as the telephone by Graham Bell in 1876, the lamp bulb by Joseph Wilson Swan in 1878 [1] or the work of Nikola Tesla on electric machines provoked a real change on the live of their contemporaries. Since then, electricity usage has not ceased to increase as more powerful and complex devices and machines have been introduced.

In this way, power electronics appeared at the beginning of the 20^{th} century. Power electronics is charged to adapt an electrical input to the characteristics of an electrical receptor and to control its parameters using power electronic devices.

The first power electronic device was the mercury-arc valve (1902), invented by Peter Cooper Hewitt. After this, devices such as the ignitron, the phanotron, the thyratron and especially the vacuum valve dominated power electronics until the 50's [3].

In 1947 the first Germanium transistor was invented by Bell Telephone Laboratories [4]. This discovery would change electronics forever. In 1956 the first thyristor or SCR (silicon controlled rectifier) was developed, also by Bell Laboratories. This device was used exclusively in power electronics applications. After that, other power devices such as the GTO, the

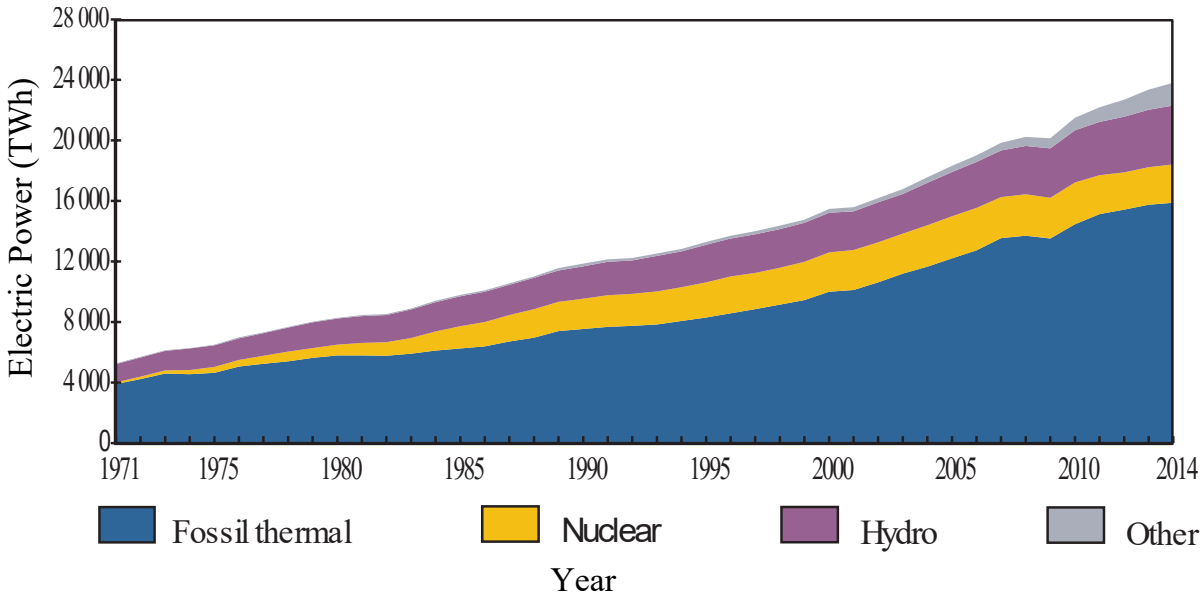


Figure 1 – World electricity generation from 1971 to 2014 by fuel (TWh) [2].

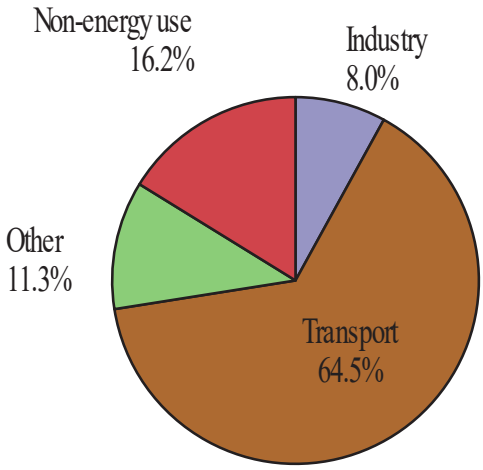


Figure 2 – 2014 world oil consumption (3761 Mtoe) [2].

TRIAC, MOSFET and JFET devices or the IGBT were introduced, resulting in more powerful, integrated and efficient systems.

Today, a major change on semiconductor devices is happening. It is based on wide band gap semiconductor materials, mainly silicon carbide and gallium nitride. It seems that these technologies will be widely used in the next years in power applications. Other semiconductors, such as diamond, boron nitride or gallium trioxide are under study, but they are far away from industrialization.

Today, one of the most important issues for the society is to reduce its dependence of fossil energy and its CO_2 emissions, which cause global warming. Indeed, fossil resources provide more than 80% of the world primary energy [2].

Among many other actions, this requires a transition towards more electric systems. However, this would not be a real solution without an important reduction of fossil resources proportion on the energy mix. One of the main activities consuming fossil resources, specially oil, is transport. As showed in fig. 2, near 64.5% of world oil consumption is used for this activity [2].

Thus, transport activities are turning towards more electric, efficient and ecological vehicles. This concerns automotive, railway and aeronautical industries.

Even if other sectors of activity are concerned about CO_2 emissions and fossil resources dependence, we will focus our discussion on transport and more specifically on the aeronautics industry.

More Electric Vehicles

Automotive

Although if currently receives a lot of attention, the electric car actually exist since the middle of the XIX^{th} century [5]. Nevertheless, competitive gasoline prices as well as some improvements on combustion unit, better autonomy and lower fabrication cost contributed to internal combustion hegemony we see today.

The interest on electric cars restarted at the end of s. XX, when General Motors introduced its EV (electric vehicle) concept [6]. Since then, manufacturers made several attempts, but

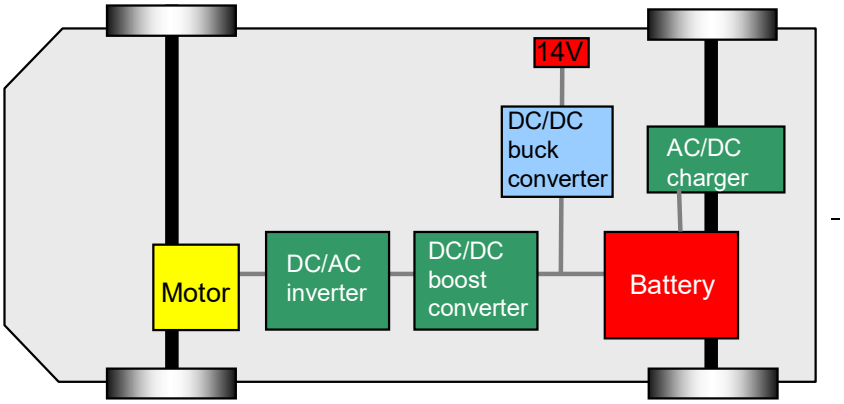


Figure 3 – Schematic diagram of typical EV configuration [9].

autonomy has always been a limitation. Fuel cell vehicle concept was introduced by Honda (Honda FCX) [7] and some cities have fuel cell demonstration buses [8]. Even if fuel cell cars have a competitive range (about 500 km), hydrogen distribution remains a key issue for its expansion.

Currently, it seems that most suitable concept would be based on a HV (high voltage) battery (near 600 V)[9]. Usual 12 V battery would be eliminated and a buck converter will provide the energy to a low voltage bus in order to supply auxiliary systems as ABS, ESP or illumination. Connexion between battery, low voltage bus, and different car systems would be done using power electronic converters as shown in fig. 3.

Vehicle components experience harsh environment conditions due to vibrations, extreme temperatures and thermal cycling. Temperature requirements in automotive are -40/150 °C(Grade 0, AEC Q100). Then, silicon semiconductors have a very slight margin in order to avoid working above their specifications (usually their maximum junction temperature is limited to 150 or 175 °C). This, together with high voltages and power density predicted on electrical cars leads silicon technology to its limit and wide band gap devices are required.

Railway

In the late XIX^{th} and in the early XX^{th} century [10, 11], railway electric grids used continuous voltage and motors used for the locomotives were DC motors[11]. Nevertheless, reduced lifetime of mechanical contactors as a result of electric arcs was a handicap and transition to AC grids started[12].

In the 60's, semiconductor devices appeared on locomotives to be used on Graetz bridges. Controlled rectifiers and inverters were then introduced thanks to the evolution of power semiconductor devices. The next improvement on railway evolution was the replacement of DC motors by induction motors, with a great gain in weight and integration.

The last huge improvement arrived with the IGBT, in the 90's. With its better switching performances compared to the GTO and its easier control (the GTO is a current controlled device while the IGBT is a voltage controlled device), the IGBT become the reference device for all energy conversion systems (see fig. 4).

Indeed, other silicon devices such as JFETs or MOSFETs were not suited to the voltage and current requirements of the railway industry [14]. Today, with the apparition of new wide

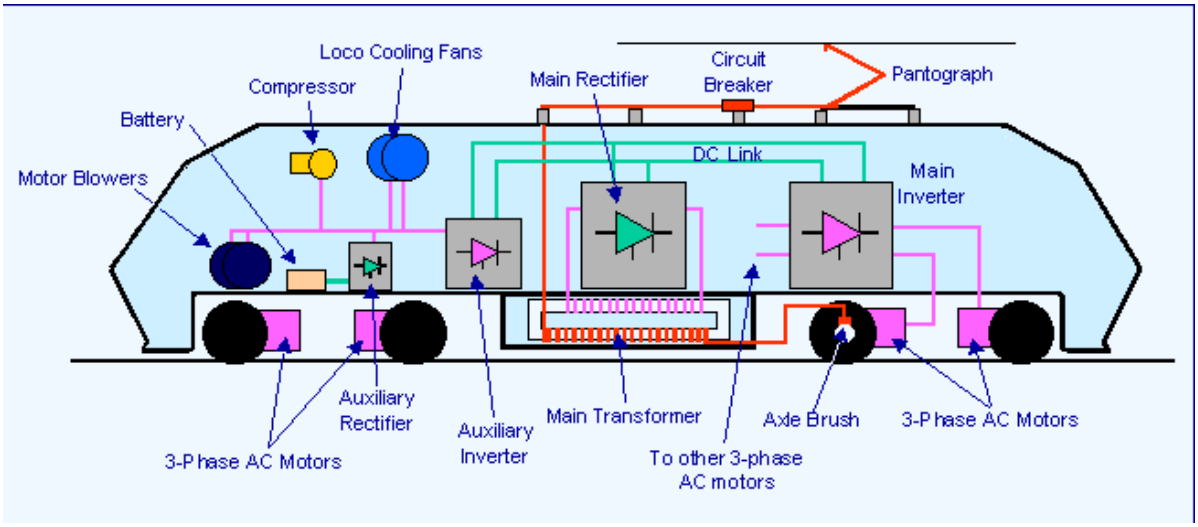


Figure 4 – Block diagram of a modern Electric Locomotive [13].

band gap devices, siicon IGBTs may be replaced by SiC MOSFETs [15]. The goal, as always, more integrated systems and more reliability.

Aeronautics

As for the railway and automotive sectors, aeronautics is turning towards a more electrical aircraft (MEA). In fact, this transition is not new and successive aircraft models have always used more electric power.

At the end of second world war, aircraft technology had greatly improved. The firsts civil jet airliners models arrived in the 50's, incorporating also more complex systems. Havilland Comet (1952), Tu-104 (1956) or french Caravelle (1959) were the first jet airliners.

As an example, the Caravelle has an installed electric power about 27 kW, using a 28 V_{dc} bus. All driving systems were pneumatic or hydraulic. In the early 70's, the Airbus A300 was consuming around 250 kVA, incorporating a new electric architecture.

Its electrical system was based on a 115 V 400 Hz AC bus, while maintaining the 28 V_{dc} bus. The 400 Hz frequency was chosen as it made possible to significantly reduce alternator weight for the same power compared to a lower frequency.

Power requirements continued increasing as new aircraft models were introduced. As an example, the Airbus A320 (300 kVA) includes the system "Fly by Wire". In other words, the control stick was replaced by a simple joystick with electrical signal transmission. Other examples followed, such as electrical sensors and actuators, electric brake system or anti-ice system (see fig. 5).

Recently, with the apparition of the A380 in 2007 with its 600 KVA a big step toward the MEA was accomplished. It incorporates electromechanical (EMA) and electro-hydraulic (EHA) actuators. In 2011, another aircraft appeared largely doubling on A380 electric power capacity. It was the Boeing B787, with a power electric capacity of 1.5 MVA.

The Boeing 787 is the first modern aircraft without pneumatic systems. Its electric architecture is shown in fig. 6. It has six power generators (4x250 kVA, 2x225 kVA) and four electric buses at different voltages (230 Vac, 115 Vac, ± 270 V_{dc}C and 28 V_{dc} [17, 18]).

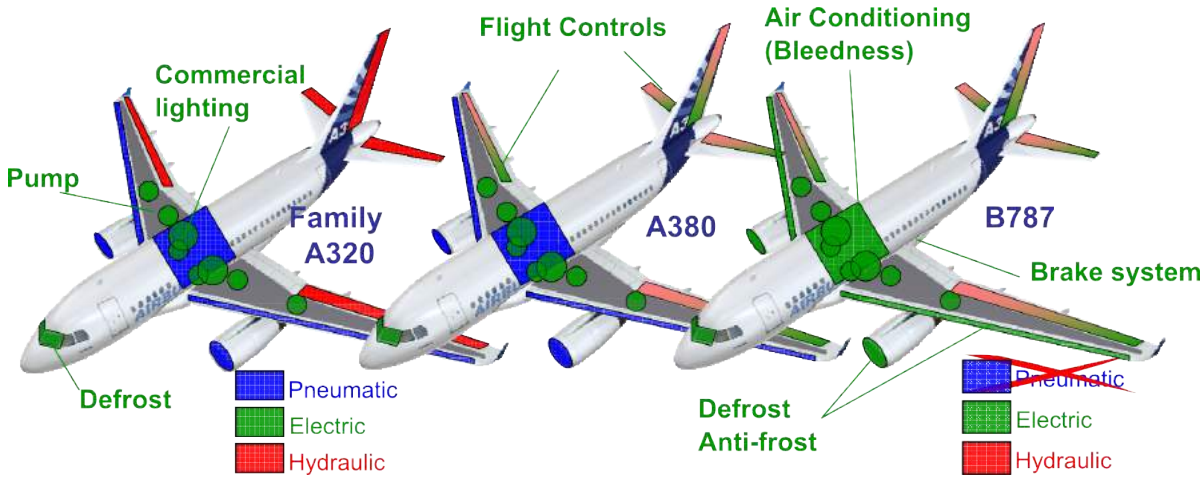


Figure 5 – Evolution of aircraft systems towards MEA [16].

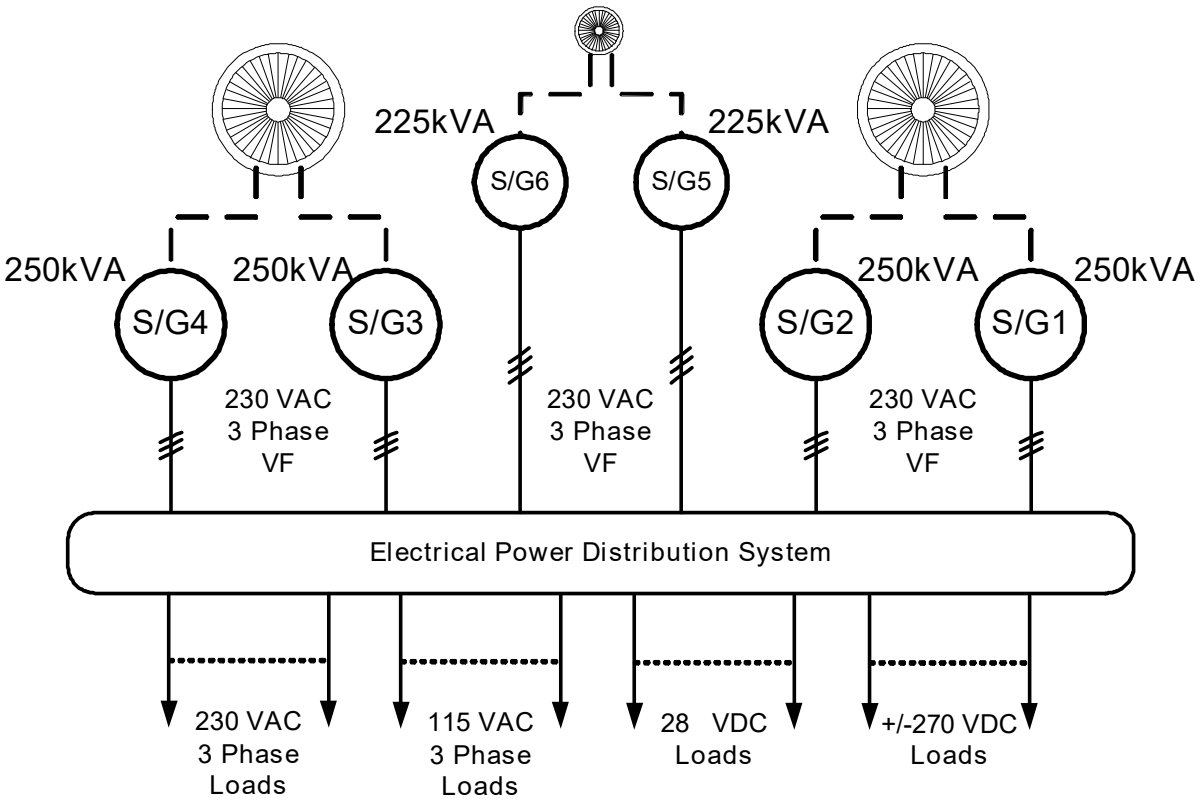


Figure 6 – Electrical structure on Boing 787 [17, 18].

The MEA concept is still in progress, with the development of reliable and efficient electric systems. In this particular, wide band gap devices should allow to operate at higher voltages and temperatures enabling further weight reduction. As in the Boeing 787, it is expected that new models will incorporate a HVDC bus 540 V ($\pm$ 270 V_{dc}) [19]. Using higher voltages, wire sections can be reduced. Also, cooling systems size and weight could be reduced by using devices which can operate at higher temperatures.

One of the most promising wide band gap materials is SiC. As it will be detailed further in chapter 1, MOSFET structure has become the main SiC device for power applications because

it is a voltage controlled and normally-off device. Among the benefits of SiC devices, there is a drastic loses reduction thanks to SiC lower resistivity, but also due to their capability to switch faster than silicon devices, minimizing commutation times. Moreover, they can drive much higher voltages than silicon devices for a given temperature and even it is envisaged to use SiC devices for high-temperature applications (>200 °C).

This PhD thesis is involved in the project GENOME-PREMICES, which focuses in the MEA concept. In the first chapter we describe the state of the art on SiC semiconductor properties, power electronics semiconductor devices and their reliability. In a second time, chapters 2 and 3 analyses two of the main reliability issues in SiC MOSFETs which limits their utilisation in aeronautics applications; the intrinsic diode and the gate dielectric robustness.

Chapter 1

State of the art in SiC devices

Contents

1.1 SiC semiconductor properties

Since the apparition of the first commercial silicon devices (grown junction) in 1954 [20], silicon technology has become hegemonic. Indeed, silicon proprieties allow to be used over a wide applications range. With a bandgap energy of 1.1 eV [21], manufactured silicon devices can reach temperatures near 200 °C at 1000 V [22].

Nevertheless, the critical junction temperature follows an inverse relation with the breakdown voltage. Then, developing devices for high temperature (>200 °C) and high voltage (>600 V), silicon material is the principal limiting factor.

A wide type of applications, specially harsh environment applications, are requiring more powerful systems and more performant semiconductor devices. As a result, the semiconductor industry is turning towards wide band gap materials. Among these materials, SiC and GaN seems to be the most interesting in the short-term. Indeed other semiconductor materials, such as diamond, are a long way from maturity.

In this thesis, we will focus on SiC. GaN is a promising semiconductor material, but for high power applications, SiC is more interesting for the following reasons:

- It is a massif material, thus it will allow to develop vertical devices. This will result in higher voltage devices (>1200 V). Today GaN devices are limited to 650 V.
- SiC technology is more mature than GaN technology. First SiC commercial devices appeared in early 2000's.
- There are many elementary reliability issues which must to be solved in GaN until to be introduced on industrial applications.

1.1.1 SiC Crystal Structure

SiC was discovered accidentally by *J. Berzelius* [23] in 1824, but industrial fabrication process was not achieved until 1891 by *E.G. Acheson* [24]. In the first half of the 20th century, SiC was only considered for its mechanical and chemical properties [25].

In 1955, a patent from *J.A. Lely* [26] concerning SiC mono-crystal manufacturing by sublimation opens the door to the first semiconductor devices based on SiC substrates [27, 28, 29, 30]. Silicon and Carbon, both elements of IV group of the periodic table of elements, form covalent bonds [31] resulting in tetrahedral structures as shown in fig. 1.1.

The actual crystal structure can differ in function of the tetrahedral stacking sequence, which can be symmetric or asymmetric. As a result, more than 200 types of crystal structures, called polytypes, have been mentioned in the literature [33]. Among them, there are the main structures used in electronics, which are listed in table 1.1 using Ramsdell notation [34] and represented in fig. 1.2. In Ramsdell notation, the letter indicates the crystal structure of the polytype (cubic, hexagonal or rhomboidal) and the number indicates the number of bilayers on the stack sequence.

6-H was used first for power electronics [36]. Even if its fabrication processus is more complicated, 4-H has replaced it, as it presents better electrical characteristics. The 3-C cubic structure was used for photonics applications in the past, but it has been remplaced by GaN which shows brighter emission [37] due to GaN direct bandgap insted of the indirect one of SiC. However, 3-C is still investigated for several applications, such as biosensors [38].

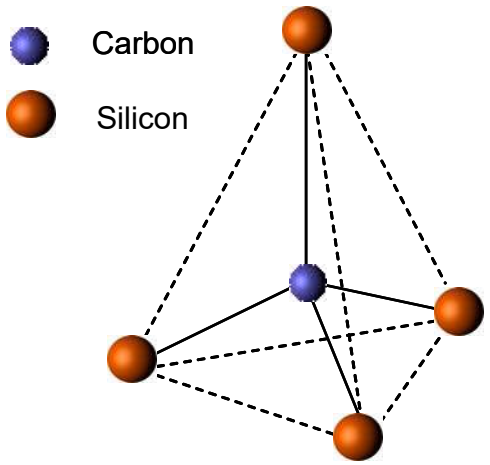


Figure 1.1 – SiC base tetrahedron. A carbon atom is bounded to four silicon atoms [32].

Ramsdell Notation	Structure	Sequence
SiC-3C	Cubic	ABC
SiC-4H	Hexagonal	ABCB
SiC-6H	Hexagonal	ABCACB

Table 1.1 – Notation of most common SiC polytypes used in electronics [35].

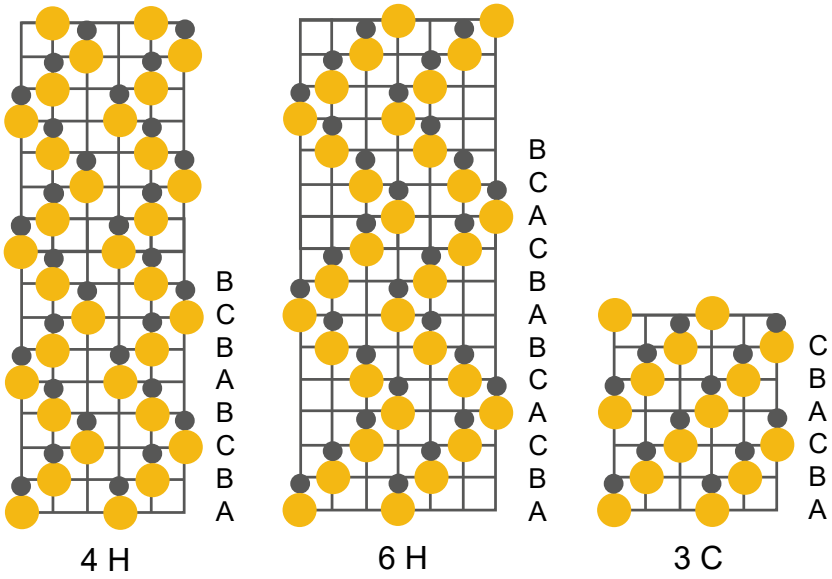


Figure 1.2 – Cristalline structure of polytypes 4-H, 6-H and 3-C [35].

1.1.2 Electric Properties

The different nomenclatures used in this section are summarized in table 1.2.

1.1.2.1 Intrinsic Carrier Concentration n_i

The intrinsic carrier concentration is determined by the quantity of electrons and holes that participate in conduction [21]. Its concentration depends on temperature (T), bandgap energy of the material (E_G) and the density of states in the valence band (N_V) and in the conduction band (N_C) as specified by eq. (1.1).

$$n_i = \sqrt{N_C \cdot N_V} \cdot e^{E_G/2kT} \tag{1.1}$$

where k is the Boltzmann's constant ($1.38 \cdot 10^{-23} J/K$) and T is the absolute temperature (K). The intrinsic carrier concentration of silicon and silicon carbide (4H) are given by eq. (1.2) and (1.3) respectively [21]. These equations are plotted in fig. 1.3.

$$n_i = 3.87 \cdot 10^{16} \cdot T^{3/2} \cdot e^{-7.02 \cdot 10^3/T} \qquad [cm^{-3}] \tag{1.2}$$

$$n_i = 1.70 \cdot 10^{16} \cdot T^{3/2} \cdot e^{-2.08 \cdot 10^4/T} \qquad [cm^{-3}] \tag{1.3}$$

Nomenclature	Parameter	Units
α	Impact ionization coefficient	cm^{-1}
α_n	Impact ionization coefficient for electrons	cm^{-1}
α_p	Impact ionization coefficient for holes	cm^{-1}
μ	Carrier mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$
μ_0	Electron mobility at low electric fields	$cm^2 \cdot V^{-1} \cdot s^{-1}$
μ_n	Electron mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$
μ_p	Holes mobility	$cm^2 \cdot V^{-1} \cdot s^{-1}$
ρ	Intrinsic resistivity	$cm \cdot \Omega$
ε_S	Semiconductor dielectric constant	-
E	Electric field	$V \cdot cm^{-1}$
E_c	Critical electric field	$V \cdot cm^{-1}$
E_G	Bandgap energy	eV
k	Boltzmann's constant	J/K
N	Doping concentration	cm^{-3}
N_A	Acceptor concentration	cm^{-3}
N_C	Density of states in the conduction band	cm^{-3}
N_D	Donor concentration	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
N_V	Density of states in the valence band	cm^{-3}
Q	Electric charge	C
q	Electron charge	C
$R_{on,sp}$	Specific on-resistance	$\Omega \cdot cm{-}3$
T	Temperature	K
V_{bi}	Built-in potential	V
V_{br}	Breakdown voltage	V
v_{sat}	Saturated drift velocity	$cm \cdot s^{-1}$
V_a	Applied bias	V
v_D	Carrier velocity	$cm \cdot s^{-1}$
W_D	Depletion region width	cm

Table 1.2 – Table of symbols.

As shown in fig. 1.3, n_i increases with temperature, but remains much smaller for SiC than that for Si, as a result of its larger energy bandgap. At 300 K, 4H-SiC intrinsic carrier concentration is $6.7 \cdot 10^{-11}\ cm^{-3}$, compared to $1.4 \cdot 10^{10}\ cm^{-3}$ for Si. As a consequence, SiC devices offer a lower leakage current (bulk generation current is negligible) and a capability to operate at higher temperature.

1.1.2.2 Built-in Potential V_{bi}

The built-in potential (V_{bi}) in a semiconductor is defined as the potential across the depletion region which occurs around an abrupt PN junction in thermal equilibrium and is given by eq. (1.4) [21].

$$V_{bi} = \frac{k \cdot T}{q} \cdot ln\left(\frac{N_A^- \cdot N_D^+}{n_i^2}\right) \tag{1.4}$$

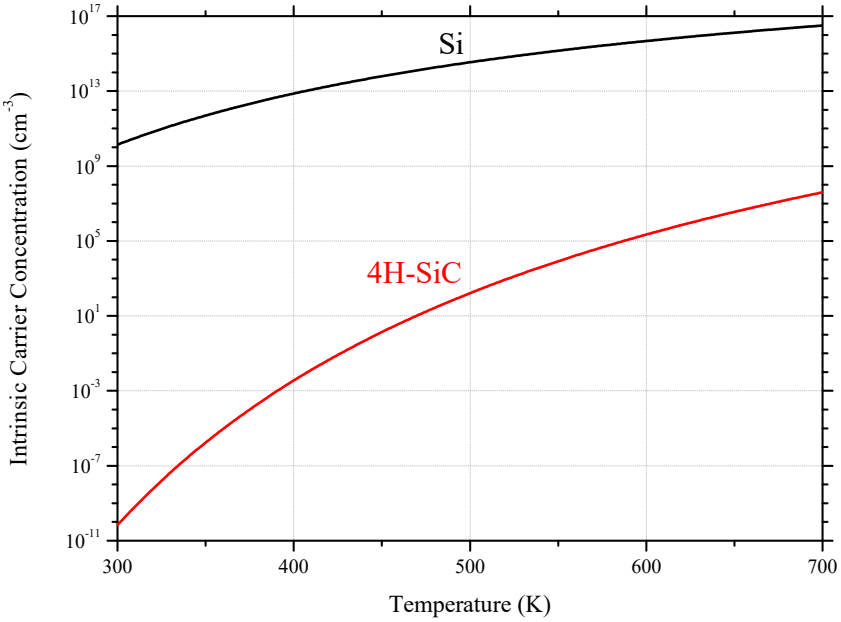


Figure 1.3 – Si and 4H-SiC intrinsic carrier concentration (based on [21]).

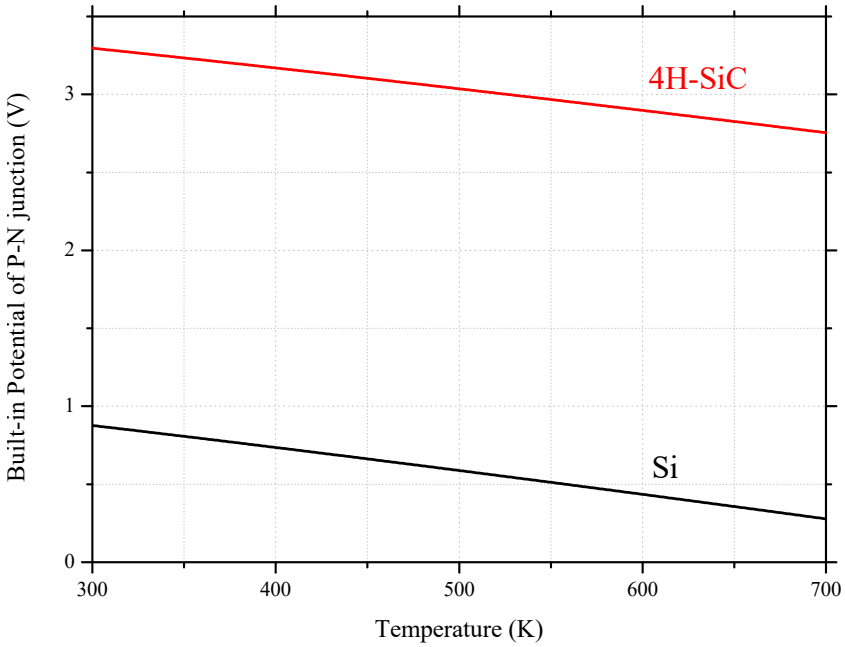


Figure 1.4 – Si and 4H-SiC built-in potential (based on [21]).

where q is electron charge ($1.6 \cdot 10^{-19}\ C$) N_A^- and N_D^+ are the ionized impurity concentrations (cm^{-3}) on the two sides of the P-N junction.

Fig. 1.4 shows the built-in potential as a function of temperature for 4H-SiC and Si according to (1.4), using (1.3) and (1.2) for n_i. It was assumed that $N_A = 10^{16}$ and $N_D = 10^{19}\ cm^{-3}$ as typical doping concentrations.

As can be seen from fig. 1.4, 4H-SiC built-in potential is much higher than for Si. This results from lower intrinsic carrier concentration on SiC ($6.7 \cdot 10^{-11}\ cm^{-3}$ vs $1.4 \cdot 10^{10}\ cm^{-3}$ on Silicon) derived from its higher band gap energy. Even if doping concentrations can be higher

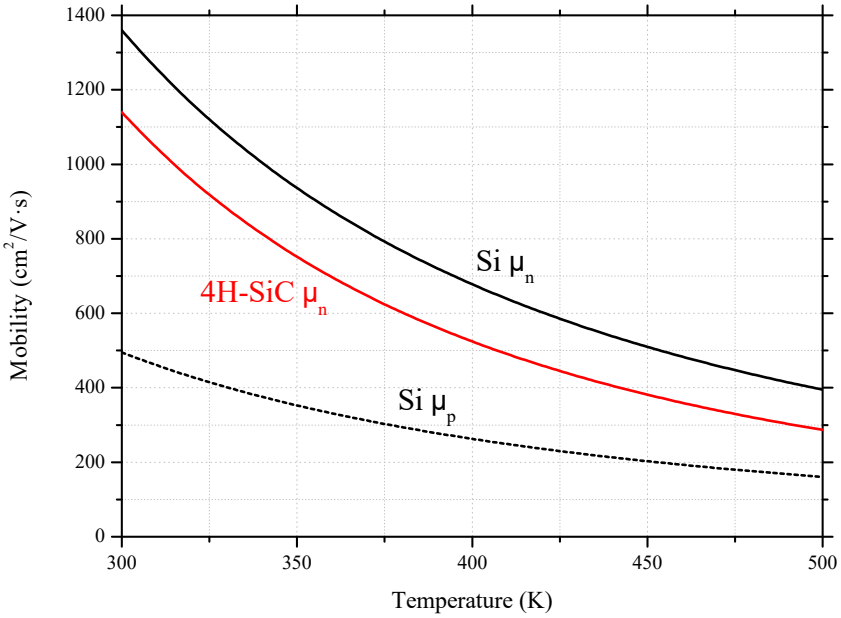


Figure 1.5 – Si (electron and holes) and 4H-SiC (electron) mobility dependence on temperature (based on [21]).

for SiC (about 100x those of a Si junction with the same breakdown voltage) [21], these have a low impact in the built-in potential due to the magnitude of n_i.

1.1.2.3 Carrier Mobility μ

One of the main physical quantities in semiconductor physics is the mobility (μ), which refers to the relation between the average carrier velocity (v_D) and the electric field (E) as eq. (1.5) shows [21]. Indeed, carriers are accelerated by electric field and reach an average velocity v_D.

$$\mu = \frac{v_D}{E} \tag{1.5}$$

For higher electric fields, the velocity converges to a constant value called *saturated drift velocity*. It is worth noting that mobility is not only dependent on the electric field, but also on the temperature and doping concentration.

Temperature dependence

The temperature dependence of electron mobility at low doping concentrations has been empirically described by eq. (1.6) and eq. (1.7) [21] for silicon and 4H-SiC respectively.

$$\mu_n(Si) = 1360 \cdot \left(\frac{T}{300}\right)^{-2.42} \qquad \left[cm^2 \cdot s^{-1} \cdot V^{-1}\right] \tag{1.6}$$

$$\mu_n(4H-SiC) = 1140 \cdot \left(\frac{T}{300}\right)^{-2.7} \qquad \left[cm^2 \cdot s^{-1} \cdot V^{-1}\right] \tag{1.7}$$

Figure 1.5 summarizes temperature dependence of mobility for 4H-SiC electrons (μ_n) and Si electrons and holes (μ_p) for the case of low doping concentrations (below 10^{15} cm^{-3}). As seen, the temperature dependence of mobility is significant, with a reduction by a factor 2

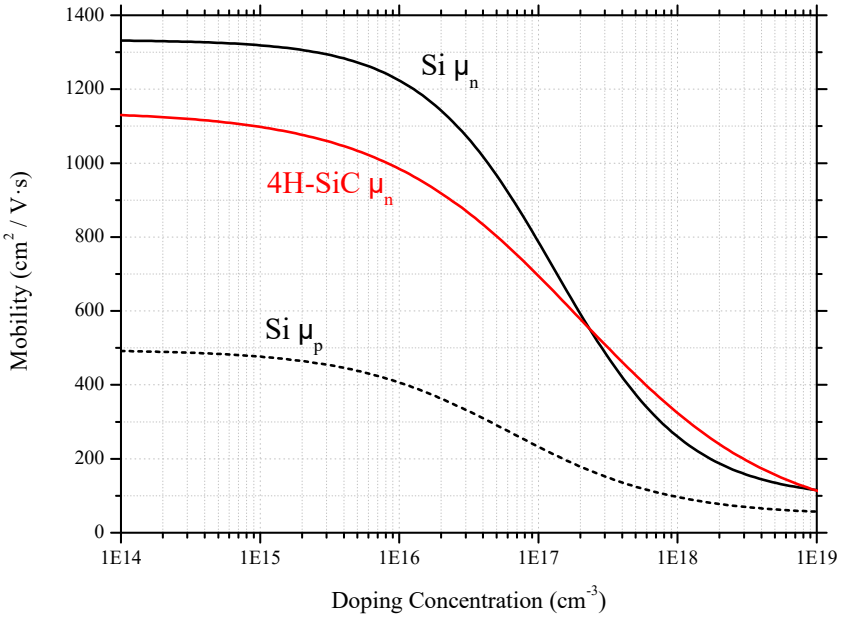


Figure 1.6 – Si (electron and holes) and 4H-SiC (electron) mobility dependence of doping concentration (based on [21]).

between 300 and 400 K which is the usual temperature range of operation for power devices. The mobility plays a major role in the resistivity of the semiconductor material, as described by eq. (1.8), where ρ is the resistivity and N is the doping concentration.

$$\rho = \frac{1}{q \cdot \mu \cdot N} \tag{1.8}$$

Doping concentration dependence

At low doping concentrations (below 10^{16}), mobility remains near constant and phonon scattering is the principal limiting phenomenon. At higher doping concentrations Coulombic scattering becomes important, reducing mobility. This is due to ionized impurity scattering with ionized doping atoms [39]. This behaviour, was empirically modelled by eq. (1.9)[39].

$$\mu = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N}{N_r}\right)^{\alpha}} \tag{1.9}$$

where N is the donor/acceptor concentration, μ_{min} and μ_{max} are the minimal and maximal mobility. N_r and α are fitting parameters. For 4H-SiC the eq. becomes [21]:

$$\mu_n(4H - SiC) = \frac{4.05 \cdot 10^{13} + 20 N_D^{0.61}}{3.55 \cdot 10^{10} + N_D^{0.61}} \qquad \left[cm^2 \cdot s^{-1} \cdot V^{-1}\right] \tag{1.10}$$

Electric field dependence

Electron and holes mobility in silicon is considered independent from the electric field below $10^3\ V \cdot cm^{-1}$. For higher electric fields, carrier velocity increases sub-linearly until it reaches the saturated drift velocity which is also temperature-dependent.

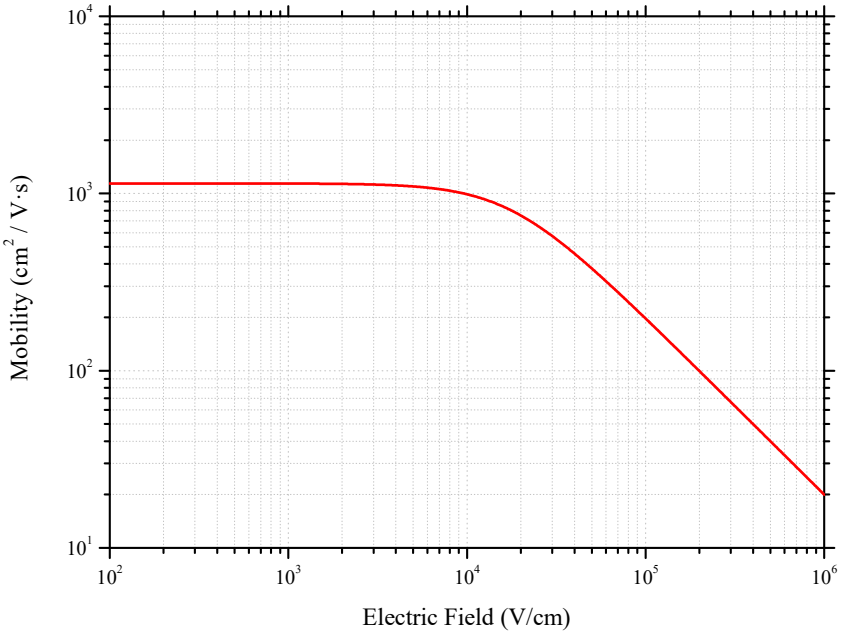


Figure 1.7 – 4H-SiC electron mobility dependence of electric field (based on [21]).

At low doping concentrations, mobility of SiC electrons can be defined by eq. (1.11) [40], where μ_n is the electron mobility, μ_0 is electron mobility at low electric fields ($1140\ cm^2 \cdot V^{-1} \cdot s^{-1}$ for 4H-SiC), E is the electric field in $V \cdot cm^{-1}$ and $v_{sat,n}$ is the saturated drift velocity for electrons ($2 \cdot 10^7\ cm \cdot s^{-1}$ for 4H-SIC). Eq. (1.11) is plotted in fig. 1.7.

$$\mu_n(SiC) = \frac{\mu_0}{\left[1 + \left(\frac{\mu_0 \cdot E}{v_{sat,n}}\right)^2\right]^{0.5}} \tag{1.11}$$

1.1.2.4 Breakdown Voltage V_{br}

One of the principal characteristics of power semiconductor devices is their capability to block high voltages in their off state.

This blocking voltage is limited by the avalanche breakdown phenomenon. For high electric fields, impact ionization phenomena appears (see fig. 1.8), producing the generation of electron-hole pairs with a multiplicative effect (avalanche) which may result in device destruction.

Some notions about impact ionization coefficients and avalanche breakdown voltage are presented bellow for an abrupt P-N junction.

Impact ionization coefficient

Impact ionization coefficient for electrons (α_n) is defined by *Baliga* as "the number of electron-hole pairs created by one electron traversing 1 cm through the depletion layer along the direction of the electric field [21]." Impact ionization coefficient for holes (α_p) can be defined analogously.

$$\alpha = a \cdot e^{-b/E} \qquad \left[cm^{-1}\right] \tag{1.12}$$

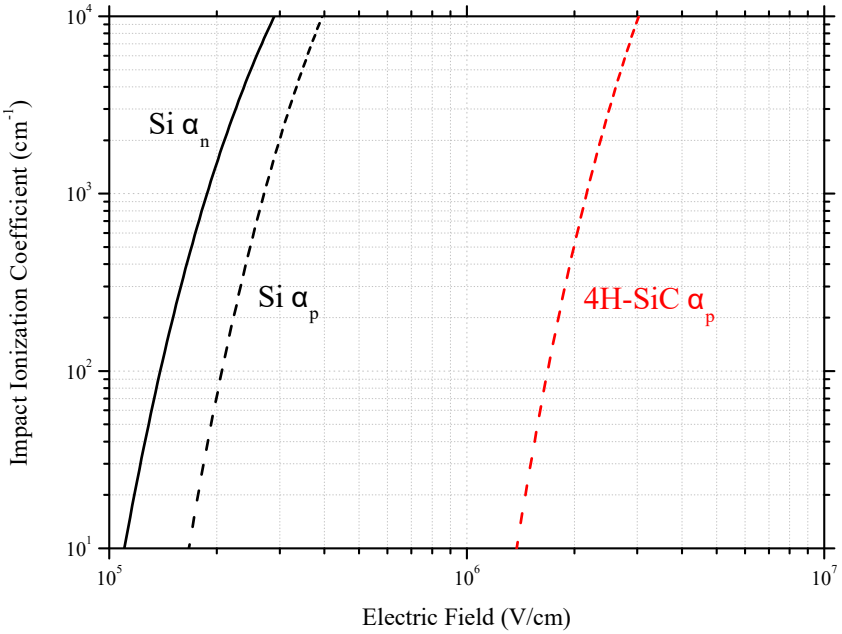


Figure 1.8 – Si (electron and holes) and 4H-SiC (holes) electric field dependence of impact ionization coefficient.

A.G. Chynoweth determined by Chynoweth's Law [41, 42] that impact ionization coefficients for semiconductors were electric field dependent in agreement with eq. (1.12), where α is the impact ionization coefficient, a and b are constants that depend of the semiconductor material and E is the electric field. In agree with [21], fig. 1.8 shows electric field dependence of impact ionization coefficient at room temperature. 4H-SiC impact ionization coefficient for holes (α_p) and Si impact ionization coefficients for holes and electrons (α_n) are plotted.

As it can be seen in fig. 1.8, impact ionization coefficient have a strong dependence of electric field which will limit power device breakdown voltage. It is evident that significant generation of carries by impact ionization occurs at higher electric fields for 4H-SiC than for Si, implying a larger breakdown voltage (near one order of magnitude).

Avalanche breakdown for an abrupt P-N junction

An abrupt PN junction is defined as a junction where doping type changes over a very small distance compared to the width of the depletion region. This can be considered as a suitable model for a junction where one side is highly doped compared to the other one. In this case it can be considered that electric field supported in the highly doped region can be neglected and that depletion region extends only on the lightly doped region. Then, using Poisson's equation [43] for the lightly doped region (N) and in agreement with fig. 1.9, eq. (1.13) is obtained.

$$\frac{d^2V}{dx^2} = -\frac{dE}{dx} = -\frac{Q(x)}{\varepsilon_S} = -\frac{q \cdot N_D}{\varepsilon_S} \tag{1.13}$$

where ε_S is the semiconductor dielectric constant

Integrating eq. (1.13), it is possible to obtain the electric field distribution:

$$E(x) = -\frac{q \cdot N_D}{\varepsilon_S} \cdot (W_D - x) \tag{1.14}$$

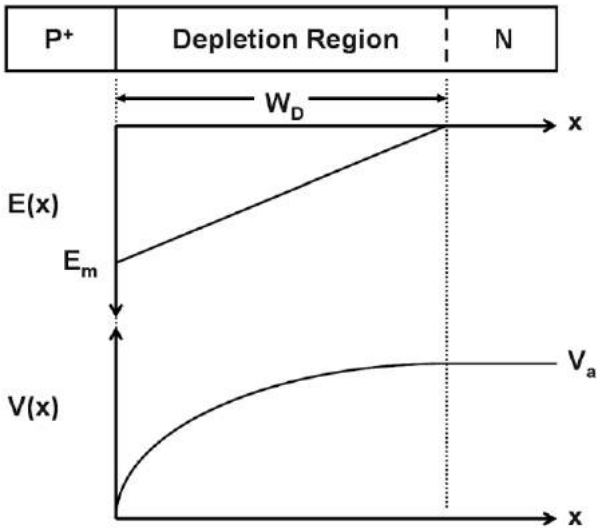


Figure 1.9 – Electric field and potential distribution for an abrupt parallel-plane P^+-N junction [21].

Integrating eq. (1.14) and assuming that electric field is zero at the end of the depletion region ($x = W_D$), yields the electric potential distribution:

$$V(x) = \frac{q \cdot N_D}{\varepsilon_S} \cdot (W_D \cdot x - \frac{x^2}{2}) \tag{1.15}$$

The maximal value of the electric field and potential are expressed by eq. (1.16) and eq. (1.17) respectively.

$$E(x)_{max} = \frac{q \cdot N_D \cdot W_D}{\varepsilon_S} \tag{1.16}$$

$$V(x)_{max} = \frac{q \cdot N_D \cdot W_D^2}{2 \cdot \varepsilon_S} \tag{1.17}$$

Considering an applied bias V_a as the maximal potential, it is possible to rewrite eq. (1.17) to obtain the thickness of the depletion region:

$$W_D = \sqrt{\frac{2 \cdot \varepsilon_S \cdot V_a}{q \cdot N_D}} \tag{1.18}$$

For 4H-SiC, *Baliga* [21] provides equations (1.19) and (1.20) expressing respectively the breakdown voltage and the depletion region thickness as a function of the doping concentration. These are plotted in figures 1.10 and 1.11 and compared to Silicon. It is considered [21] that breakdown phenomena occurs when the integral of the impact ionization coefficient on the depletion region becomes equal to unity.

$$V_{br} = 3.0 \cdot 10^{15} \cdot N_D^{-3/4} \qquad [V] \tag{1.19}$$

$$W_{D_{max}} = 1.82 \cdot 10^{11} \cdot N_D^{-7/8} \qquad [cm] \tag{1.20}$$

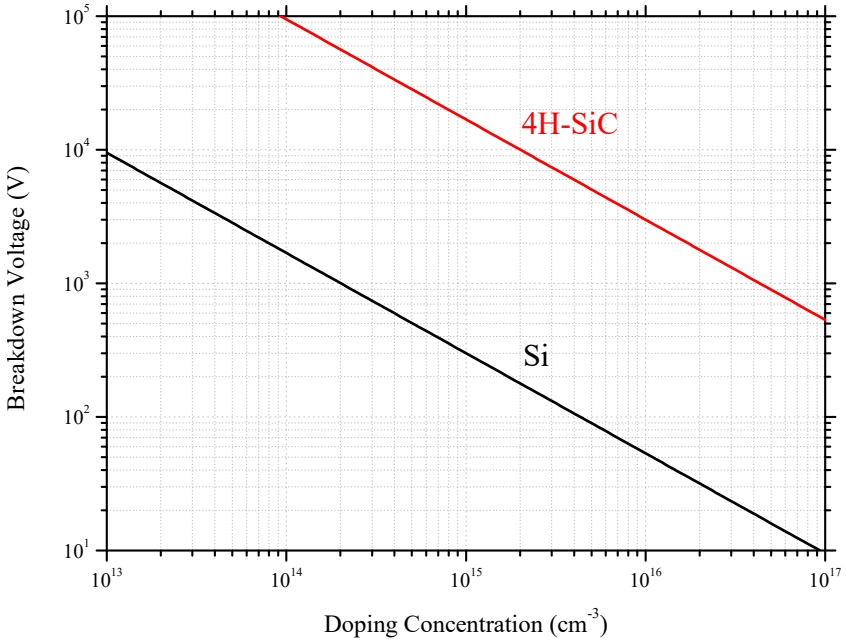


Figure 1.10 – Voltage breakdown of a PN junction as a function of the N-region doping, for Si and 4H-SiC (based on [21]).

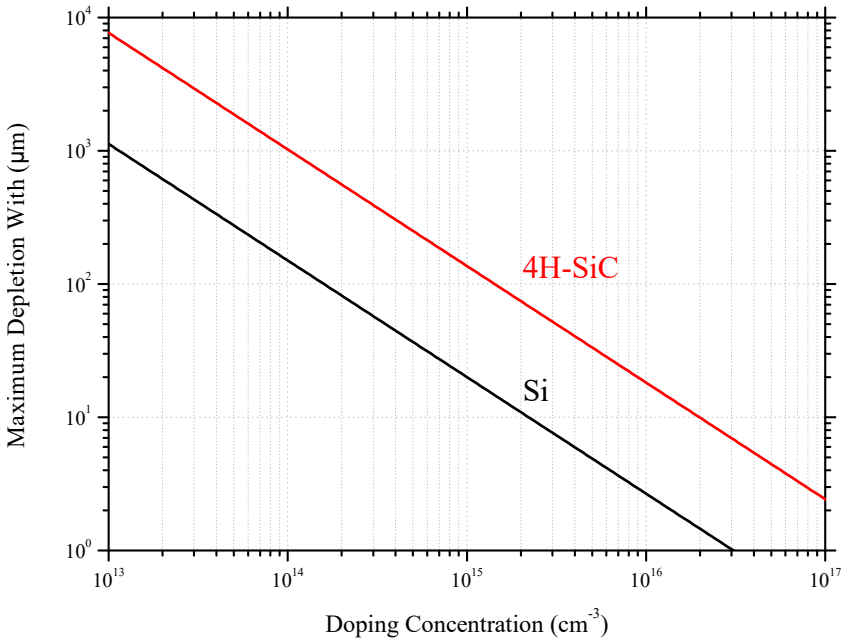


Figure 1.11 – Maximum depletion width of a PN junction as a function of the N-region doping, for Si and 4H-SiC (based on [21]).

As it can be seen on fig. 1.10, the breakdown voltage decreases with the doping concentration, but remains much higher for SiC than for silicon, permitting higher doping concentrations for a given breakdown voltage. For a given breakdown voltage, the depletion width is thinner for 4H-SiC than for silicon devices. Both parameters result in a much lower specific-on resistance as will be showed in section 1.1.2.5.

One of the principal physical properties used to compare semiconductor materials is the

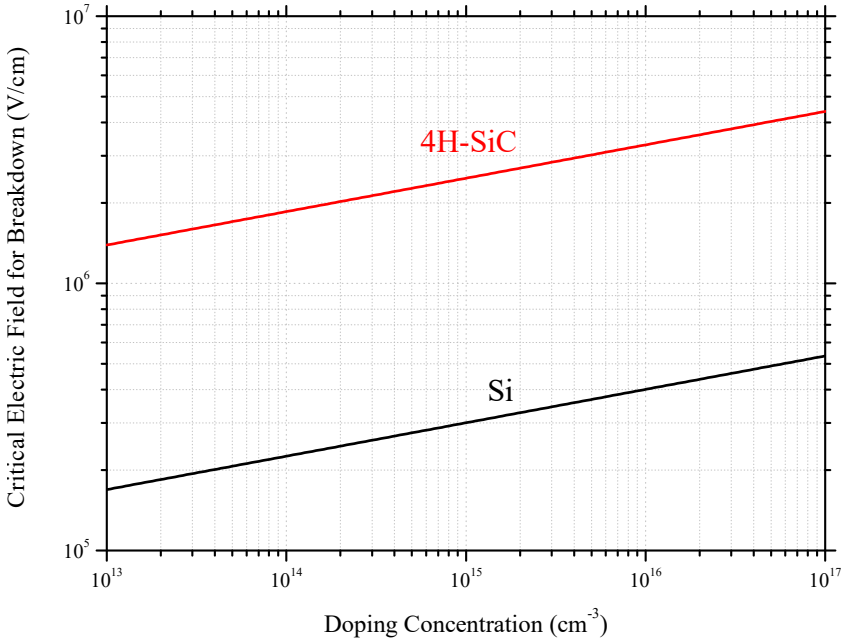


Figure 1.12 – Critical electric field for breakdown in Si and 4H-SiC (based on [21]).

critical electric field. For example, this term is present in figures of merit (FoM) such as Baliga's [21] or Johnson's [44]. Combining eq. (1.16) and (1.18) it can be calcultaded the maximal electric field at the junction, which is expressed by eq. (1.21). Combining this with eq. (1.19) allow to describe the critical electric field (E_c) dependence on doping concentration by eq. (1.22) [21]. This is plotted on figure 1.12 and compared to silicon.

$$E_{max} = \sqrt{\frac{2 \cdot q \cdot N_D \cdot V_{br}}{\varepsilon_S}} \tag{1.21}$$

$$E_c = 3.3 \cdot 10^4 \cdot N_D^{1/8} \qquad [V \cdot cm^{-1}] \tag{1.22}$$

It is seen in fig. 1.12 that the critical electric field increases slightly with doping concentration. 4H-SiC has a critical electric field 8.2 times larger than silicon for the same doping concentration. This is a key parameter to design high voltage devices and has a special relevance on specific on-resistance reduction.

1.1.2.5 Specific On-Resistance $R_{on,sp}$

The specific on-resistance is defined as the resistance per unit area of the drift region and is expressed in $\Omega \cdot cm^2$. It is related to the breakdown voltage V_{br} by eq. (1.23).

$$R_{on,sp} = \frac{4V_{br}^2}{\epsilon_S \cdot \mu_n \cdot E_c^3} \tag{1.23}$$

Replacing V_{br} and E_c by their expressions (eq. (1.16) and eq. (1.17)) yields:

$$R_{on,sp} = \frac{W_D}{q \cdot \mu_n \cdot N_D} \tag{1.24}$$

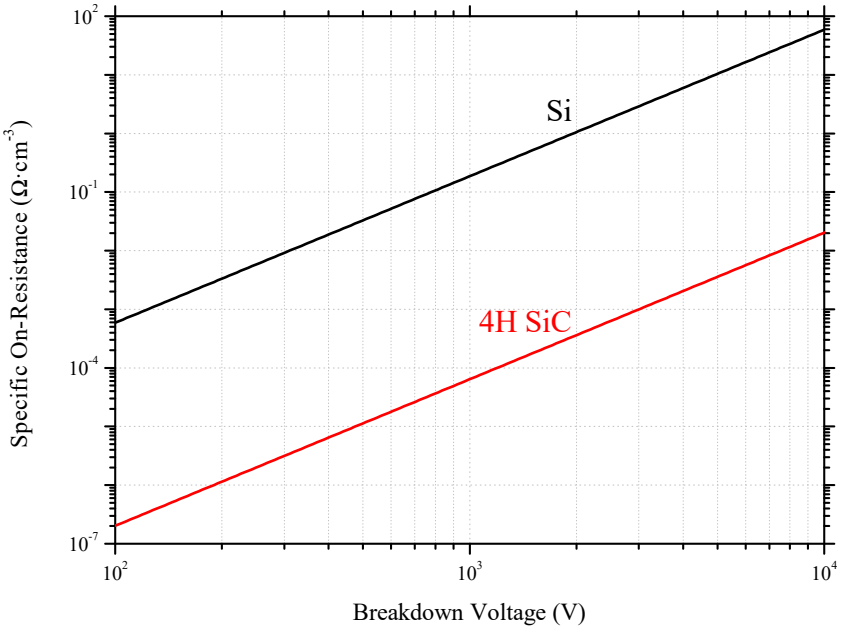


Figure 1.13 – Specific on-resistance versus breakdown voltage for 4H-SiC and Si (based on [21]).

The projected specific on-resistance as a function of breakdown voltage is plotted in fig. 1.13 for 4H-SiC and Si substrates. It can be seen that the specific on-resistance on 4H-SiC is about 2500 times lower than that of silicon. This represents a real advantage for 4H-SiC devices, allowing more efficient devices.

1.1.3 Comparative Properties

Table 1.3 summarizes principal electrical and physical properties for Si and 4H-SiC. The larger band gap, near three times higher for 4H-SiC than for Si, results in a drastic reduction of intrinsic carrier concentration. Thus, the leakage current of a reverse-bias junction is dramatically reduced. Consequently, it is possible to develop new devices working at higher voltages and temperatures.

Most of the properties presented in table 1.3 show the better performances of the 4H-SiC. With a saturation drift velocity doubling that of Si and a critical electric field near to 8 times higher, 4H-SiC is one of the best performing semiconductor materials. 4H-SiC has a thermal conductivity higher than twice that of Si. Only the mobility is lower. Figure 1.14 summarizes a comparison between some properties of the main semiconductor materials.

In order to compare semiconductors properties, several figures of merit have been defined. The most common are Johnson FoM [44], Keyes FoM [46] and Baliga FoM [21]. It is worth noting that every FoM focuses on a type of application. In this way, Johnson's and Baliga's focus on power applications, but the first one on high frequency and low voltage applications and the second one on low frequency applications, assuming that conduction losses are dominant. There is another FoM defined by Baliga, called BHFFM [47] (Baliga High Frequency FoM) which is focused on high frequency power applications. Keyes FoM has the particularity of incorporating thermal parameters and is also focused on high frequency applications, but for transistors used on integrated circuits.

Properties[a]	**Si**	**4H-SiC**
Relative Dielectric Constant ε	11.7	9.7
Energy Band Gap $E_G\ (eV)$	1.1	3.26
Carrier Concentration $n_i\ (cm^3)$	$1.4 \cdot 10^{10}$	$6.7 \cdot 10^{-11}$
Electron Mobility $\mu_n\ (cm^2 \cdot V^{-1} \cdot s^{-1})$	1320	1100
Saturated Drift Velocity $v_{sat}\ (cm \cdot s^{-1})$	$1 \cdot 10^7$	$2 \cdot 10^7$
Critical Electric Field $E_c\ (V \cdot cm^{-1})$	$3.01 \cdot 10^5$	$2.47 \cdot 10^6$
Thermal Conductivity $\lambda\ (W \cdot cm^{-1} \cdot K^{-1})$	1.5	3.7

Table 1.3 – Electro-physical properties for Si and 4H-SiC semiconductors materials [21, 45].

[a] Assuming a doping concentration $N_A = N_D = 10^{15}$

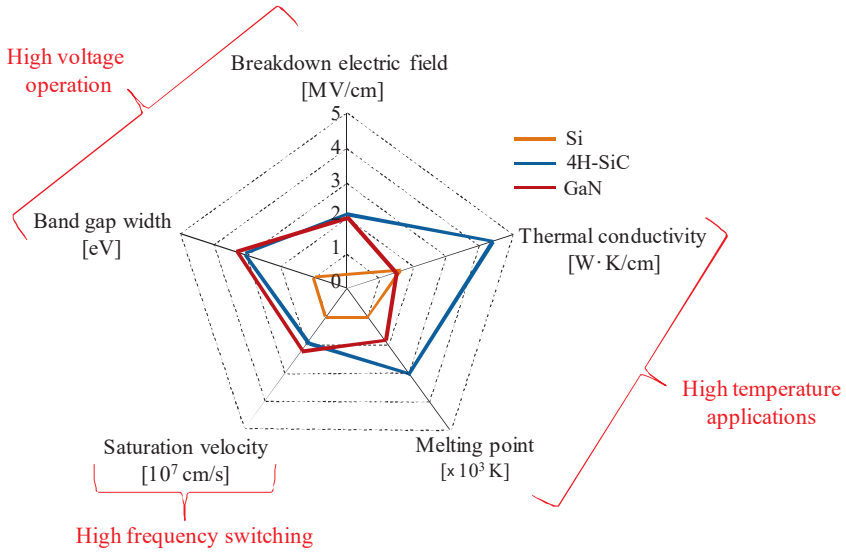


Figure 1.14 – Summary of Si, SiC and GaN relevant material properties [48].

Table 1.4 summarizes these FoMs, including a comparison between Si (reference) and 4H-SiC, highlighting the better performances of 4H-SiC.

In conclusion, 4H-SiC offers the following advantages:

- Lower conduction losses due to its lower specific on-resistance. This is due to its higher doping concentration and to its thinner drift region for a given V_{br}.

FoM	Equation	Si	4H-SiC
Johnson JFM	$\frac{E_c^2 \cdot v_{sat}^2}{4 \cdot \pi^2}$	1	410
Keyes KFM[a]	$\lambda \cdot \sqrt{\frac{c \cdot v_{sat}}{4\pi \cdot \epsilon}}$	1	5.1
Baliga BFM	$\epsilon \cdot \mu \cdot E_c^3$	1	290
Baliga HF BHFFM [b]	$\frac{\mu \cdot E_c^2}{2} \cdot \sqrt{\frac{V_g}{V_{br}^3}}$	1	34

Table 1.4 – FoM summary and comparative between 4H-SiC and Si [44, 21, 46, 47, 49, 45].

[a] c is light speed in vacuum.
[b] V_g is gate voltage.

- Higher voltage devices can be designed thanks to the higher critical electric field of 4H-SiC. Its lower carrier concentration minimizes leakage current in the off-state.
- Its better thermal performances, could open the way towards high temperature and more integrated devices, particularly on devices without gate oxide.

1.2 Impact of crystallographic defects in SiC

Electronic devices manufacturing involves many steps which have to be realised carefully. Any defect introduced during the different manufacturing phases or material finishing could result in a failure of the device.

One of the critical process step is the growth of SiC on a SiC substrate (epitaxy).

The most common method to grow SiC crystal is VPE (Vapour-Phase Epitaxy). This process is capable to produce high quality material. In spite of the high crystal quality, improvements are required in order to minimize material defects. In this way, different approaches on CVD (chemical vapor deposition) [50] have been presented, showing as micropipes defects where properly closed. Also, LPE (liquide-phase epitaxy) technique has been studied [51], repporting a defect number reduction.

Even if further description of epitaxy techniques are not the focus of this document, a description of the principal material defects is necessary. This is described and summarized below.

1.2.1 Main SiC crystallographic defects

The most important defect encountered in SiC crystals are micropipes. These are thermodynamically stable hollow core screw dislocations [52]. On a wafer, they consist on a hole about 1 μm diameter in size [53]. Thus, a device with a micropipe defect is no longer capable to support a high electric field. It is considered as a critical defect which manufacturing companies try to eliminate. Commercial SiC wafers are usually classified by the rate of defects [54].

Today, it is possible to produce 150 mm diameter 4H-SiC wafers without any micropipe defect [54].

Unfortunately, micropipes are not the only type of defect which can be found in SiC crystals. There are several other types of defects which can be classified in two sets:

- SiC wafer defects.
- Epitaxial defects.

A type of defect, called stacking fault (SF) could be classified in the wafer defect category. But, as it can propagate through the epitaxial layer and because it is of high importance on SiC devices, a special section is dedicated to it.

1.2.1.1 SiC wafer defects

The principal defects relative to wafer substrate are the following:

- Basal plane dislocations (BPD).
- Edge dislocations (ED).
- Core screw dislocations.

Basal plane dislocations are planar defects of the crystal, which perturb its periodicity. This type of defect can spread to the substrate surface, where the epitaxy has to be realised. Then, this can result in a defect in the epitaxy layer. Due to its unstable nature, BPD can evolve to another kind of defect called staking fault (SF) under conditions of bipolar injection [55]. As SF and BPD can be potentially critical, it is usual to use advanced epitaxial growth and engraving techniques [56] to transform this type of defect into TED (Threading Edge Dislocation) defects, which are considered as not critical [53, 57].

Edge dislocations are usually one-dimension defects on the surface of the wafer that get annealed during the epitaxial growth [53]. An edge dislocation defect is caused by the absence of an inter-atomic bonding. This kind of defect rarely affects devices operation.

Core screw dislocation is a type of defect similar to micropipes, which evolves over the thickness of the SiC wafer. This defect might continue over the epitaxy layer depending of several factors such as epitaxial growth techniques. It is known that this kind of defect results in a lower critical electric field [58] and lower carrier lifetime of the epitaxial layers grown over them [53, 59]. Some studies show that is possible to properly close core screw dislocations, limiting the reduction of the critical electric field to around 10% [60].

Finally, other defects such as low angle boundaries or defects due to polishing processes [53] are presents on commercial wafers and cause a leakage current augmentation when devices are under reverse bias conditions.

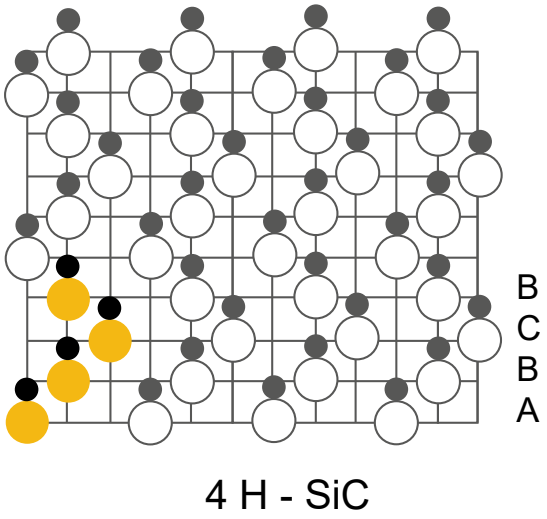


Figure 1.15 – 4H-SiC crystal structure (based on [61].

1.2.1.2 Epitaxial defects

Epitaxial defects are related to the epitaxial growth techniques. The principal defects relative to epitaxial growth are the following: [53, 59]:

- Small growth pits.
- Triangular inclusions of different polytype.
- Carrot and comet tail.

Small growth pits are usually related to closed core screw dislocations, wafer preparation or epitaxial growth steps. In spite of epilayer processes advances, it seems that closed core screw dislocations density will be the limit of small growth pits defect reduction [59].

Triangular 3C inclusions are due to wafer preparation and epitaxial groth process. Concretely, non-uniform temperatures during the epitaxial grown will cause these defect to appear [53]. They have a critical impact on high voltage devices, with a leakage current augmentation and a reduction in breakdown voltage by 50% [59]. Densities of these defects are not so large and they are improving.

Carrot defects result from wafer defects that create adverse conditions for the realization of a perfect crystal structure during epitaxial growth [53]. Comet tail are caused by a poor management of impurities or premature nucleations of SiC particules [53]. Both defects are not critical, but produces a slight augmentation in current leakage at reverse bias as well as a small reduction in breakdown voltage [59].

1.2.1.3 Stacking Faults

As presented in the precedent section, SiC polytypes are defined by their structure (cubic (C), hexagonal (H) or rhomboidal (R)) and by their periodicity. Then, 4H-SiC is an hexagonal structure with a periodicity of 4. As represented in figure 1.15, the atomic plans follows a pattern of two displacements to the right followed by two displacements to the left [57]. When one or more atomic plans do not follows this pattern, a stacking fault defect appears.

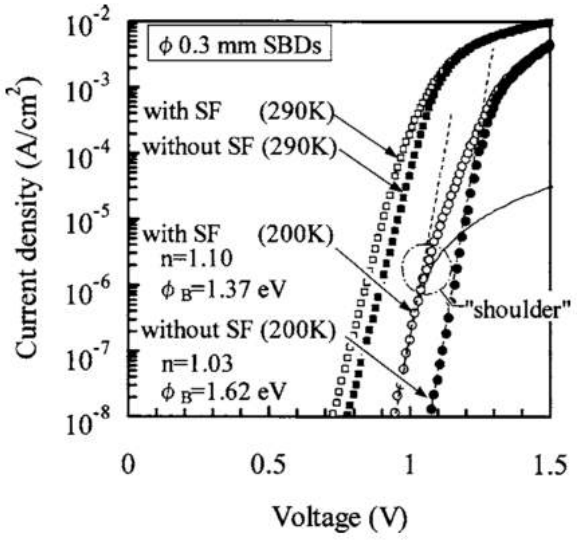


Figure 1.16 – Double barrier apparition on schottky contacts due to SF defects [64].

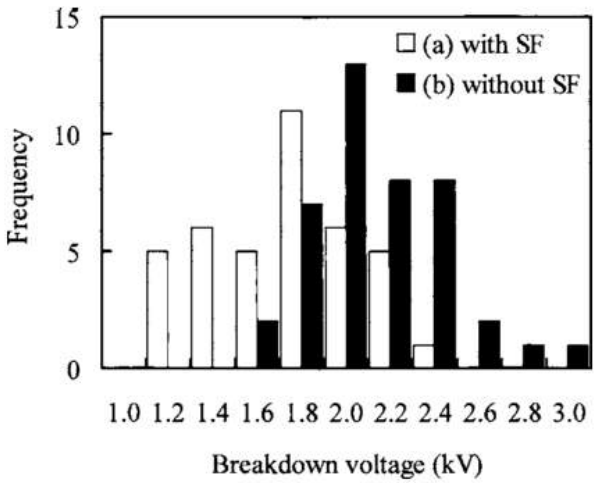


Figure 1.17 – Influence of SF defects over breakdown voltage [64].

As mentioned in 1.2.1.1, SF can result from other defects such as basal plane dislocations and tends to progress through the whole epitaxial layer thickness. In 2001, *Bergman et al.* considered that SF acts as recombination centers, reducing the recombination emission intensity and carrier lifetime [62], and resulting in forward voltage increase on PN junctions. This hypothesis seems to be contested by more recent studies which suggest that the increase of forward voltage is due to a reduction of the conduction area by SFs [53]. In [63], *Jung et al.* shows a relation between on-resistance and SF density.

A consequence of SFs in Schottky diodes is the decrease of the barrier height and the breakdown voltage [64, 65]. This results in an augmentation of the leakage current at reverse bias, as demonstrated by several studies [64, 66, 65]. Fig. 1.16 and fig. 1.17 shows respectively the apparition of a double barrier height on devices with SF defects and the difference of voltage breakdown between devices with SF defects and devices free from SF.

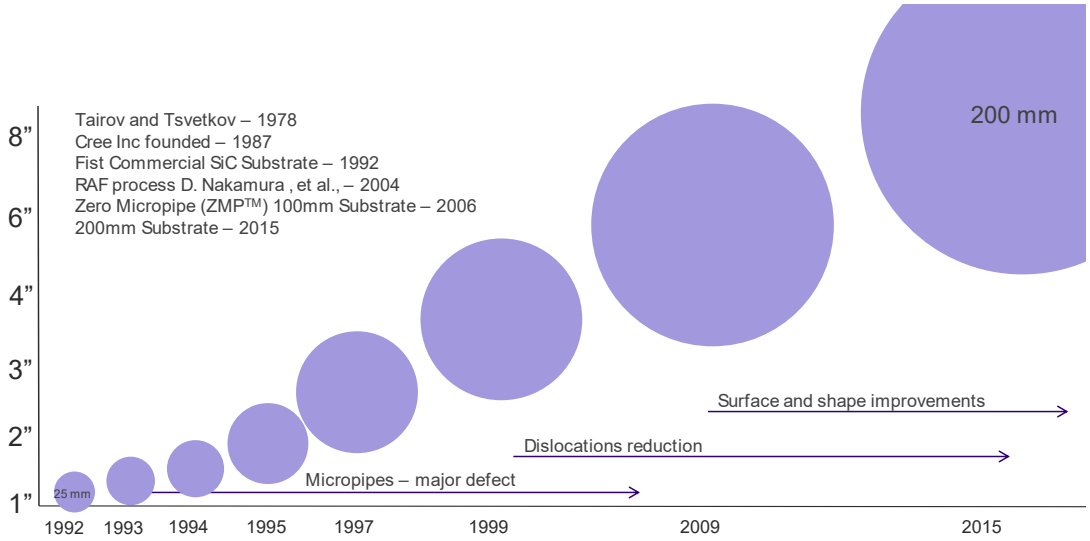


Figure 1.18 – Evolution of SiC Wolfspeed wafers from early 90's to present [54].

It is worth noting that SFs propagation incidence can be augmented under conditions of high current density or high temperature operation [53].

1.2.2 SiC defects summary

Difficulties to reach high crystal quality has long limited SiC development and expansion. Improvements on crystal growth techniques proposed by *Tairov et al.* [67] in 1978 represented an important step on SiC devices evolution. Semiconductor industries have focused on SiC devices development at the end of the 80's.

Defect	Density (cm^{-2}) Year 2012 [68]	Density (cm^{-2}) Year 2016 [69]	Yield effect	Reliability effect
MP	<2	<0.3	minor	critical
TSD	10^3	200	medium	medium
TED	$< 10^4$	3100	none	none
BPD	$< 10^3$	800	none	critical (bipolar)
SF	1	-	minor	critical
Additional Epitaxial defects	$1 - 10$	-	medium	medium
Technology defects	$1 - 10$	-	medium	medium

Table 1.5 – Overall defect situation on state of the art wafers.

A lot of efforts have been dedicated to reduce and minimize defects. Fig. 1.18 illustrates SiC wafer development and evolution. In the early 90's, SiC wafers had 25 mm diameter size. In early 2000's, wafer size reached 100 mm size in diameter. Nevertheless, defects density was still too high to develop reliable power devices. CREE developed its first 100 mm substrate with zero micropipes defect (ZMP) in 2006 [54]. One of the main objectives was reached.

However, other defects types such as BPD, TSD or SF were still important issues to solve. At the same time that quality improvement was required, wafers needed to grow in size to manufacture cost-competitive devices. The focus was on dislocation reduction and 150 mm diameter size wafers. Today, after important efforts on SiC crystal grown technology, a certain technology maturity has been acquired. Wolfspeed (CREE) is working towards 200 mm diameter size wafers development.

Table 1.5 summarizes the most important defect types, as well as their density, their impact on device efficiency and their impact on reliability. Defect density values are reported from [68] and [69], published in 2012 and 2016 respectively. Thus, this illustrates defect reduction over last years.

It is seen that critical defects such as MP, BPD or SF have been highly reduced. As a result, it is now possible to design devices with a larger surface. Then, devices operating at higher current and voltage ratings are possible. MP and SF defect seems to be near to eliminated. Nevertheless, BPD could result in SF defect during bipolar current recombination, seriously affecting device performance and reliability. To limit their impact, techniques to transforming BPD defects into TSD defects [56] have been developed.

1.3 SiC Power Electronic Switches

One of the main elements in power electronics are the switches. Their function is to allow or block the current flow. They can be divided in two categories: natural and controlled switches. The main uncontrolled switch is the rectifier diode, which allows current flow in only one direction (anode-cathode). Among the controlled switches (externally controllable), are the transistors which can be further separated into BJTs, MOSFETs, JFETs and IGBTs. MOSFETs and JFETs are current bidirectional switches, which allow the forward and reverse current to flow as a function of a voltage level applied to their gate. BJTs are voltage bidirectional switches and their current flow is a function of their base current. The IGBT is an unidirectional device combining some of the MOSFET and the BJT caracteristics. The ideal behaviour of these switches is illustrated in fig. 1.19 .

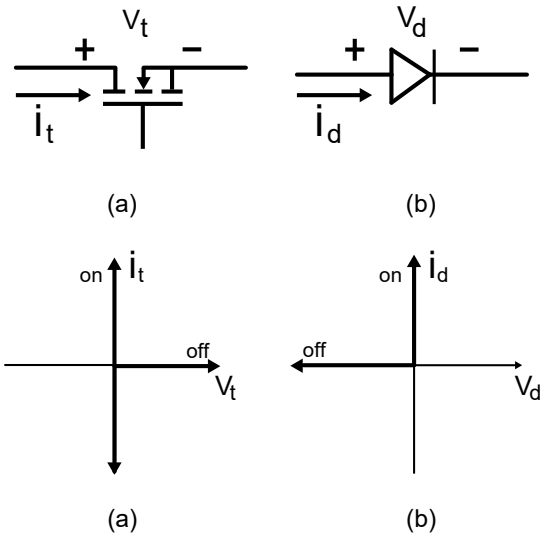


Figure 1.19 – Ideal behaviour of a MOSFET transistor (a) and a diode (b) (based on [70]).

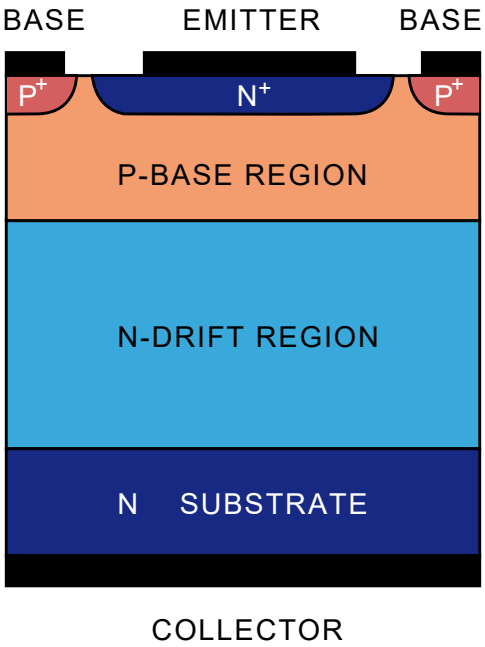


Figure 1.20 – Power bipolar NPN transistor cell (silicon) [21].

In the sections 1.3.1 to 1.3.4, we will present the main power transistor structures (BJT, JFET, MOSFET and IGBT), regardless of the semiconductor material they are based on. Then, we will focus on SiC devices, highlighting their maturity and performance.

1.3.1 BJT

The Bipolar Junction Transistor (BJT), invented in 1947 by Bell Laboratories [71], is a device controlled by injecting current in its base. As its name implies, the bipolar transistor uses both types of charge carriers (electrons and holes).

A BJT is constituted by three regions (N-P-N or P-N-P, depending on the majority carriers type). The structure of a NPN bipolar transistor is illustrated in fig. 1.20, where collector and emitter are highly-doped N^+ regions. In fig. 1.20, a lightly-doped region N^- is grown over the collector to support high blocking voltages in the off-state. The base region (P^-) is grown over this lightly-doped region N^-.

When a positive bias is applied to the collector terminal, the collector-base PN junction is reverse-biased and supports the voltage. By applying a positive voltage to the gate (with respect to the emitter), injected electrons diffuse through the P region up to the collector-base junction, allowing collector-emitter current flow.

Since the beginning of the XXI^{th} century, several industrial and academic groups have shown interest in the SiC BJT, which theoretically has the lowest specific on-resistance of all SiC transistors. Besides, power SiC BJTs have a higher gain than Si BJTs, which was one of its main limitations [72, 73, 74]. In 2005, *Krishnaswami et al.* [75], presented a 1000 V 30 A SiC BJT incorporating some improvements, such as a lower forward voltage drop, and better gain that previous devices. It is worth noting that for the same die size, *Krishnaswami et al.* reported a forward voltage drop of $V_{CE} = 2\ V$ and a gain $\beta = 40$ at 30 A, whereas *Agarwal et al.* [76] reported a $V_{CE} = 2\ V$ and a gain $\beta = 11$ at 17 A. In 2013, *Sundaresan et al.* [77]

presented a 10 kV SiC BJT, which reached 91% of the theorical 4H-SiC voltage breakdown limit.

Today, industrial SiC BJT production has been progressively abandoned in favour of SiC MOSFETs, because they are easier to drive. Only GeneSiC continues to produce a bipolar device called SJT [78], which I-V curve differs of that of a classic BJT (resistivity modulation between linear and saturation region is very low, obtaining a I-V curve similar to that of a MOSFET). Nevertheless, academic interest on the BJT continues, and it is seen as a promising device for protection or high temperature applications.

1.3.2 JFET

The Junction Field Effect Transistor (JFET) was invented in 1952 in the Bell Laboratories by W. Schockley [79]. It is a power device controlled by a gate bias voltage. Contrary to the BJT, the JFET only uses majority carriers, so it is an unipolar device. It is worth noting, that a JFET may be a normally-on device, i.e. it is conducting current in the absence of a gate bias.

The basic internal structure of a JFET is quite simple. A JFET is constituted by a semiconductor bar, with ohmic contacts at both ends (corresponding to drain and collector terminals). For a N-type JFET, the semiconductor bar would be N-type material and the gate would be grown with P-type material. Gate regions are heavily doped P^+ type and are situated on both sides of the bar. Several examples are depicted in figures 1.21 and 1.22.

In a normally-on JFET, when V_{gs} is higher than the threshold voltage the current can flow through the channel. When applying a slight negative voltage to the gate, the depletion zones around the P regions grow, constricting the channel, and increases the device resistance. For more negative gate-source potentials, the depletion regions continue to expand until they occupy all the channel when the device is blocked.

While Si power JFETs have never been significantly used, because they offer no advantage over Si MOSFETs, SiC JFETs attracted a lot of interest. During a few years, SiC JFET were commercialized by several manufacturers such as Infineon or Semisouth, but they were withdrawn, probably in favour of the SiC MOSFET. Today only the USCi company is providing SiC JFETs.

Peter Friedrichs, from SiCED, studied several SiC JFET structures [80]. The lateral-vertical structure, shown in fig. 1.21 (a), presents a lower on-resistance as the currents flows directly from the source to the drift region. However, the surface area of the gate is large resulting in higher miller capacitance and limiting the switching frequency. The structure in fig. 1.21 (b), has a lower Miller capacitance, as the gate-drain area is smaller, improving switching performances as the expenses of a higher on-resistance [81].

One of the main issues regarding the JFET has been to develop normally-off devices. Several attempts and researches have been done [83, 84, 85]. In [84], a 4H-SiC 1.7 kV vertical JFET with a specific on-resistance of 3.6 $m\Omega \cdot cm^2$ is reported. Also a 11 kV normally off 4H-SiC vertical JFET with a specific on-resistance higher than 130 $m\Omega \cdot cm^2$ is proposed by *Zhao et al.* [85]. To design a normally-off JFET, the depletion region has to be large enough to block the channel when the voltage between gate and source is null. This results in a reduced channel width and requires a low doping concentration. Consequently, the on-state resistance of the transistor could be increased and the saturation current decrease [86]. Fig. 1.22 illustrates a normally-off JFET structure.

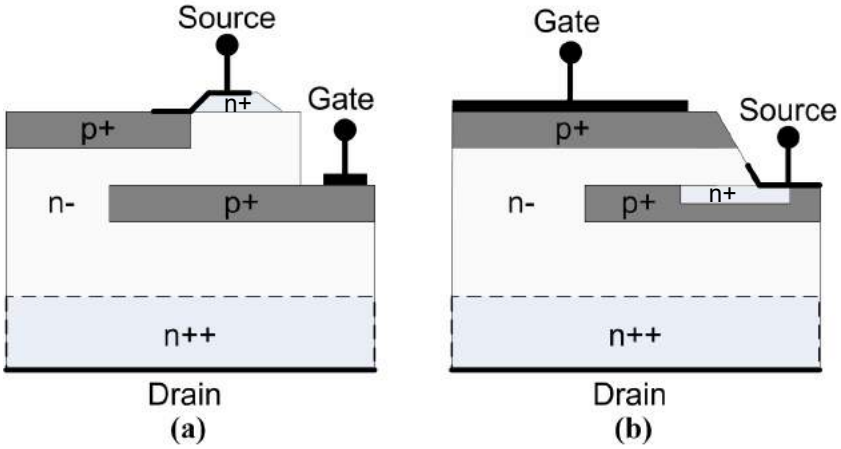


Figure 1.21 – Two different vertical JFET structures [81].

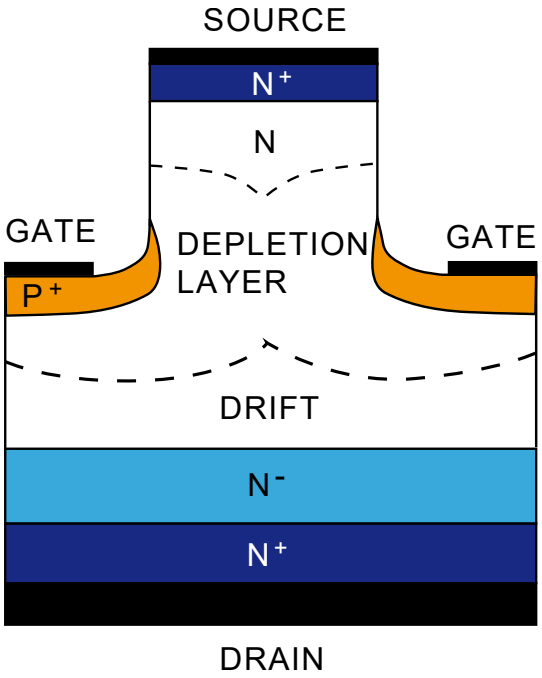


Figure 1.22 – Structure of a vertical normally-off JFET (based on [82]).

1.3.3 MOSFET

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor), is a unipolar, normally-off device. It was patented by *Lilienfeld* in 1927 [87]. As high-purity semiconductor were not available, the development of this device was not achieved until 1960, when *Dawon and Kahng* developed it at Bell Laboratories [88].

The basic MOSFET structure has four terminals, as it is shown in fig. 1.23. Usually, the bulk and source terminals are short-circuited. On a P-type semiconductor, N^+ contact regions are grown for the drain and source terminals. The gate terminal is placed between these terminals and isolated from the P-type semiconductor. The most commonly used electric insulator is SiO_2. For a negative or null voltage applied between gate and source, this device blocks the drain-source current. Applying a positive voltage to the gate, an electric field

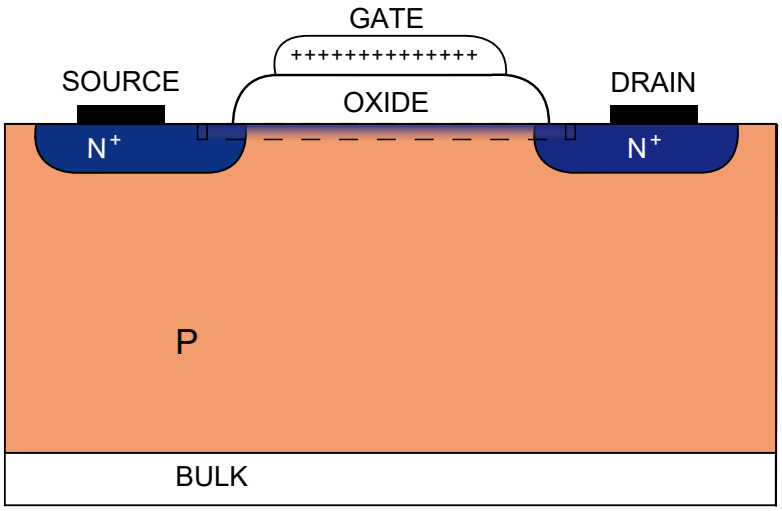


Figure 1.23 – Basic Silicon MOSFET structure (based on [21]).

is created, causing a concentration of negative charges just underneath the gate terminal. For a given electric field, a channel is created, and drain and source terminals are connected electrically. Then, the device allows the current flow.

The structure of a power MOSFET differs from that in fig. 1.23. The first high-voltage power MOSFETs were developed using a V-groove structure [21]. Nevertheless, due to technical difficulties, the V-groove structure was abandoned. Today, two types of power MOSFET structure are predominant: Vertical-Diffused (VD) and trench-gate (U).

1.3.3.1 VD-MOSFET

The cross section of a VD-MOSFET structure is shown in fig. 1.24 (a). This structure is based on a heavily-doped substrate N^+. Over this, a N^- type layer is grown. Two ion implantation processus are used to form the P-well and N+ doped regions, situated at each side of the gate terminal. The channel is formed by the difference in lateral extension of the P-well and N+ source regions produced by their diffusion cycles [21].

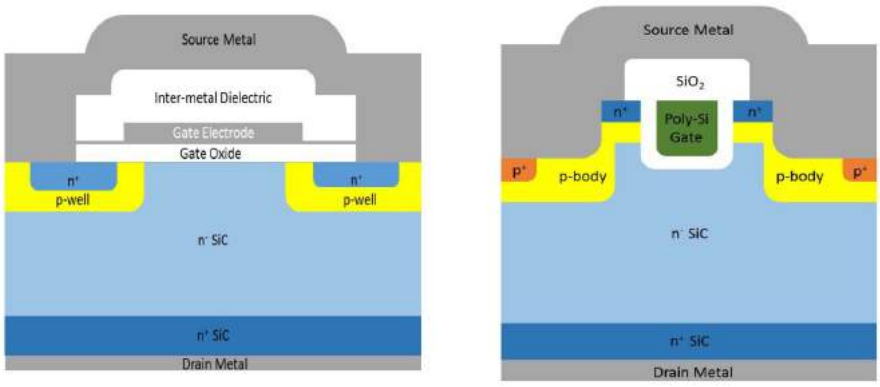
One of the inconvenient of this structure is the higher on-state resistance. When conducting, electrons circulate from the source to the drain. First, they flow through the channel. After, they enter in the JFET region and finally they reach the drain through the drift region. The higher on-state resistance is due to JFET region. This region is located where the P-well zones restrict the current flow, and care must be taken to reduce its effect. One possible solution is to increase the doping concentration in the JFET region.

1.3.3.2 U-MOSFET (Trench)

In the 90's, the U-MOSFET structure was developed to eliminate the JFET resistance.

A U-MOSFET structure is showed in fig. 1.24 (b). The trench extends from the upper surface of the structure through the N+ source and P-body regions into the N-drift region [21].

Using this structure, when the MOSFET is in the on-state, a vertical channel appears around the trench and the internal on-resistance is significantly reduced, as there is no JFET resistance. One problem of this structure is that the high electric fields which occurs in the



(a) (b)

Figure 1.24 – Silicon MOSFET structure of a VD-MOSFET (a) and a U-MOSFET (b) [89].

trench corners can cause reliability problems. In order to reduce this, the geometry has to be designed carefully and the corners are usually rounded.

1.3.3.3 SiC MOSFETs

The first SiC power MOSFET was presented in 1993 by Cree Research [90], based on a U-MOS structure, using 6-H SiC. Research advanced quickly, increasing the voltage blocking capability and reducing the internal on-resistance. A good set of references showing this improvement is given in [91]. In the same paper, one of the firsts 4-H SiC MOSFETs is presented. With a voltage blocking capability of 1400 V and based on a U-MOSFET structure, its $R_{on_{sp}}$ was much lower than the first 4-H 1400 V SiC U-MOSFET presented just one year earlier [92] ($R_{on_{sp}}$=15.7 $m\Omega{\cdot}cm^2$ vs $R_{on_{sp}}$=125 $m\Omega{\cdot}cm^2$).

In 2011, the first SiC MOSFET was commercialized by CREE,[1] providing blocking voltages up to 1200 V [93]. Its main conpetitor, ROHM, introduced a 1200 V SiC MOSFET shortly after. However, the technical solutions were not identical, but both based in a planar structure. In this way, *Shenai* showed [89] that the specific on-resistance of CREE SiC MOSFETs was 1.42 times greater than that of ROHM´s ($R_{on_{sp}}$=3.7 $m\Omega{\cdot}cm^2$ and $R_{on_{sp}}$=2.6 $m\Omega{\cdot}cm^2$ respectively).

Today, research continues on SiC MOSFETs in order to increase their blocking capability, focusing on the thickness of the drift layer which could result in a prohibitive resistivity. In this way *Pala et al.*, from CREE, presented [94] a MOSFET with a blocking capability of up to 15 kV with a $R_{on_{sp}}$=204 $m\Omega{\cdot}cm^2$. The semiconductor industry is working towards providing competitive SiC MOSFETs for a voltage range until now reserved to IGBTs. The limit between SiC MOSFETs and SiC IGBTs in unclear, but *Millan et al.* suggested that above 9 kV the IGBT should be preferable [95]. However, on a study focused on microgrids, *Zhang et al.* considered that SiC MOSFETs could dominate the applications below 15 kV.

1.3.4 IGBT

In 1968, *Yamagami and Akagiri* [96] from Mitsubishi Electric introduced the idea of the IGBT as a four semiconductor layers P-N-P-N device. First developements of IGBT were reported

[1] In September 2015 CREE announced the creation of Wolfspeed, a new division of the company for power and radio frequency devices.

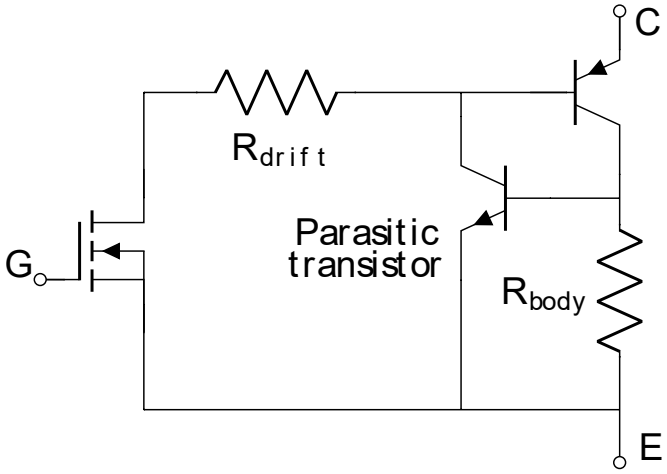


Figure 1.25 – Principle schematic of an IGBT (based on [21]).

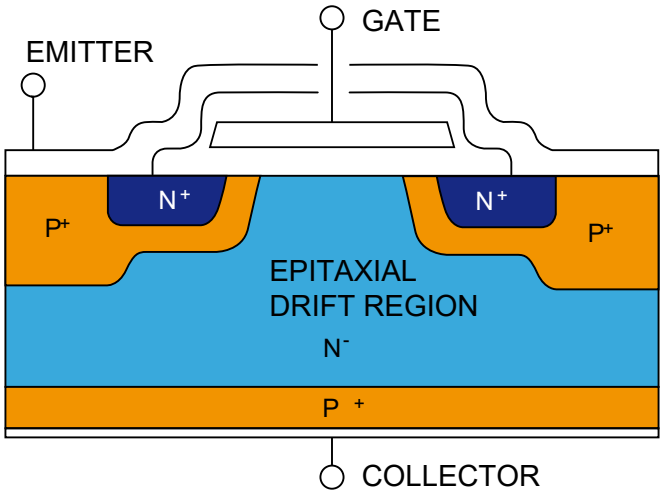


Figure 1.26 – Structure of an IGBT.

at the end of 1970s by *Sharf and Plummer* [97] and *Baliga* [98]. It is a bipolar, normally-off device.

The first IGBT with a signifiant power level appeared in 1982 and had current and voltage ratings of 10 A and 600 V respectively [99]. It has rapidly been scaled up and adapted to higher current and voltage ratings, reaching more than 1300 A and 6.5 kV [21]. The IGBT has displaced the BJT for medium power applications, but also gate turn-off thyristiors (GTO) for high power applications such as railway [21].

The electric schematic of the operating principle of an IGBT is represented in fig. 1.25. It incorporates some advantages from MOSFETs and BJTs. In this sense, as a MOSFET device, it is voltage-controlled, presenting a high input impedance. It also has the high current capability of the BJT. The IGBT structure has a notably higher current capability than MOSFETs due to the bipolar structure of the IGBT, as well as to the high level injection of free carriers into the drift region. Moreover, the IGBT has inherent forward and reverse-blocking capability.

The IGBT structure, shown in fig. 1.26, is formed by four alternative (N-P-N-P) layers, like a thyristor. This thyristor operation is suppressed by including a deep P+ region and by short circuiting the P-well and N+ emitter regions.

For a null gate-emitter voltage, the IGBT is blocked. Applying a voltage higher than the threshold voltage, a channel appears between the N+ and N drift regions, allowing current to flow from the P-N-P bipolar structure. Therefore, the collector-emitter current is the sum from that of the bipolar P-N-P structure and of the unipolar MOSFET structure.

Even if SiC IGBTs are not commercially available yet, they attract a lot of research effort. They are not competitive against SiC MOSFETs for relatively low-medium voltages (<9 kV) due to the collector-emitter voltage drop in the saturation region. *Ruy et al.*, from Cree, reported on 2012 a 4-H SiC N-IGBT with a voltage blocking capability of 12.5 kV with a $V_{ce_{sat}}$=6.1 V for a current of 32 A and V_{ge}=20 V [100]. In 2014, *Van Brunt et al.* reported the IGBT with the higher blocking capability in our knowledge, reaching 27 kV [101] with a $V_{ce_{sat}}$=11.8 V for a current of 20 A and V_{ge}=20 V.

1.3.5 Comparison of SiC devices

Until today, the IGBT has been the principal device for high power applications due to Si technology limitations. With the apparition of SiC devices, BJT, JFET or MOSFET role has to be re-evaluated as they can be good alternatives for relatively high power applications (in the hundreds of kVA) such as railway or aeronautics. Besides, the Si IGBT is the more complex and expensive of all those devices and presents frequency limitations (few tens of kHz).

Among SiC devices, BJT is an interesting low cost alternative, as it has the lower specific on-resistance, and can operate at relatively high frequencies (commutation time in the order of 100 ns [102]). Nevertheless, it has some drawbacks. It requires a permanent base-current excitation. This is contrary to industries preferences for high input impedance (voltage-controlled devices). This would require to develop specific drivers. Moreover, current gain presents important limitations mainly due to SiC substrate defects and surface recombination centers, which increase the device resistance limiting its gain [103, 104]. Today, oxide passivation is limiting the gain current on SiC BJT [105].

JFETs and MOSFETs are medium-cost alternatives, capable to operate at high frequencies (near 1 MHz). They are voltage controlled devices, thanks to their high gate input impedance. JFETs, as explained early are normally-on devices. Then, a loss of a gate driver signal could result in a system damage. For this reason, the MOSFET is preferred for most of the power electronic applications in its power range.

However, the MOSFET is a more complex device than the JFET and presents some additional reliability issues relative to the gate oxide insulator (SiO_2). These reliability problems, presented in detail in the following sections, are basically due to threshold voltage instability and oxide degradation or even failure under conditions of high electric fields and temperature [106]. In this case, electric charges can be injected in or through the $Si/SiO2$ interface, accelerating its degradation or causing voltage threshold instability and result in a change in the a operation conditions.

Therefore, as the SiC MOSFET is the preferred controlled switch for applications which were until today reserved to the Si IGBT, a special care has to be given to the MOSFET reliability to insure industry quality standards and systems lifetime requirements [107].

1.4 SiC MOSFET robustness issues

The objective of this thesis is to study the robustness of SiC MOSFETs under several conditions of operation. Due to the defects, SiC devices reliability has been highly discussed for a long time. As presented in section 1.2, the defect density has drastically reduced in the wafer. Thus, it is time to evaluate if present SiC devices are reliable, and if they are ready to be used on industrial applications.

On the following pages, a review of the most important reliability issues remaining associated with SiC devices is shown:

- Gate MOSFET robustness.
- Internal diode robustness.
- Robustness under avalanche breakdown phenomenon.
- Robustness under short-circuit conditions.

1.4.1 Gate robustness

Gate robustness is probably the most important reliability issue for SiC MOSFETs devices. Indeed, this issue concerns specially MOSFETs because it is mainly related to the SiO_2 gate insulator. Other devices, such as JFETs or BJTs, do not have this gate oxide and are not concerned by this issue.

The physical phenomenon associated with gate reliability are presented in section 1.4.1.1. The main measurements to evaluate the gate oxide degradation are described in section 1.4.1.2 and 1.4.1.3. They are:

- Time Dependent Dielectric Breakdown - TDDB
- Bias Temperature Instability - NBTI/PBTI

1.4.1.1 Energy band and carrier injection phenomenons

Energy band diagrams are common representation of semiconductor structures where conduction and valence band are defined. Electrons are filling the valence band and only a few are located in the conduction band. Only the electrons of the conduction band participate in the conduction of the device. Electrons placed in the valence band can reach the conduction band, providing they a level of energy equivalent to the energy bandgap, which is the difference between the energy levels of the conduction and valence bands. This is possible through various excitations as heat (phonon) or light (photon) excitations. Electrons can not be placed in-between the valence and the conduction bands except for deep traps.

As every semiconductor has different electrical properties, its energy band diagram it is also different. Fig. 1.27 shows the energy bands for different semiconductor materials and dielectrics. It can be seen that SiO_2 bandgap is 9 eV and 3.2 eV for 4H-SiC. Si has a much lower bandgap, at 1.1 eV. Therefore, the barrier height between 4H-SiC and SiO_2 conduction bands is lower and results 2.7 eV for 4H-SiC (in comparison with 3.2 eV for Si).

In fig. 1.28, a schematic energy band diagram is represented with a 4H-SiC (blue) semiconductor and SiO_2 interface. Moreover, silicon energy bands (brown) and the main carrier

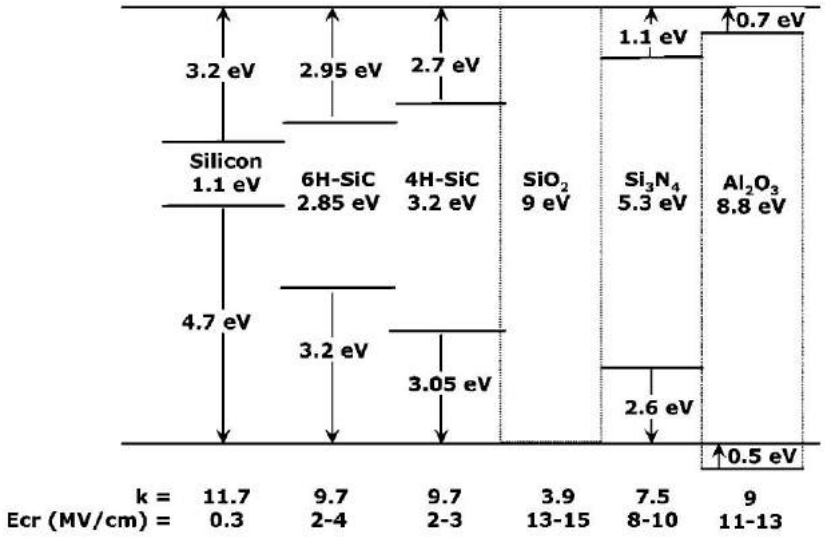


Figure 1.27 – Dielectric constants, and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3).Conduction and valence band offsets of these are also shown with respect to SiO_2 [53].

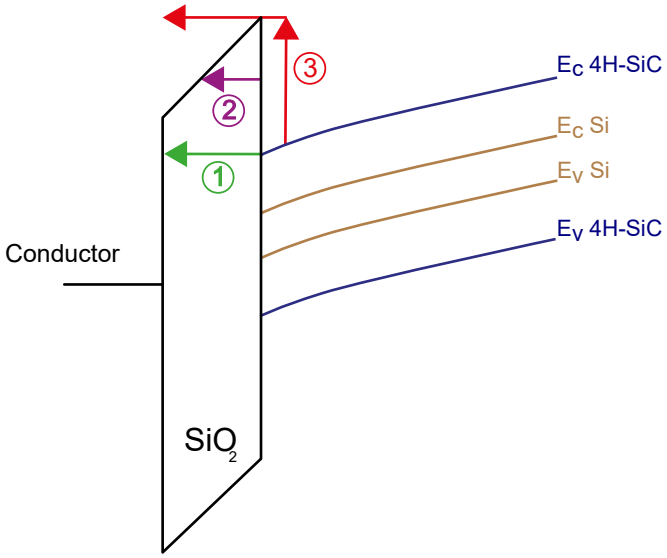


Figure 1.28 – Energy Band diagram and principal carrier injection phenomenon to interface semiconductor/SiO_2. 1) Tunnel Effect 2) Injection Fowler-Nordheim 3) Hot carrier injection.

injection phenomena are also represented. The main injection phenomena are: direct tunnel effect, Fowler-Nordheim injection and hot carrier injection.

For direct tunnelling, electrons pass through the whole SiO_2 energy barrier. Fowler-Nordheim tunnelling is a special case of direct tunnelling. Electrons do not tunnel directly to the other side of the barrier. Instead, they tunnel from the semiconductor inversion layer to the conduction band of the SiO_2 layer from where they are transported to the gate contact [108]. Injection by hot carrier is quite different. Hot carriers are particles which acumulated a very high kinetic energy from being accelerated by a high electric field. This energy permits particles to go over the SiO_2 conduction band. As a result, these particles can get trapped in

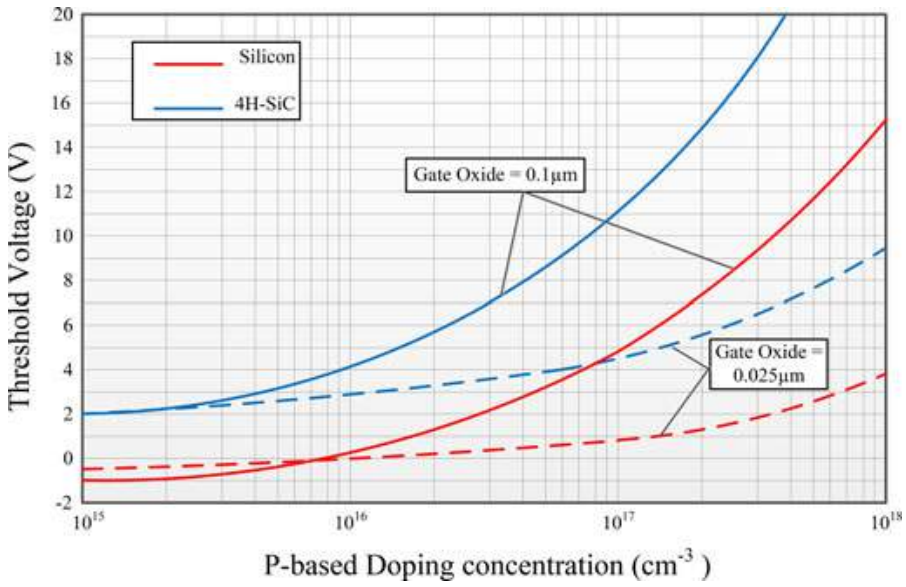


Figure 1.29 – Threshold voltage of SiC MOSFET compared to Si MOSFET (includes impact of N^+ Polysilicon gate and an oxide fixed charge of $2 \cdot 10^{11}$ cm^{-2} [111].

the SiO_2 or cause interface state to be generated [108, 109, 110].

Carrier injection phenomenons are more important in 4H-SiC than in Si devices due to their lower barrier height, but also to their thinner dielectric layer: as shown in fig. 1.29, for the same SiO_2 thickness and doping concentration, the threshold voltage of a 4H-SiC MOSFET is much higher than that of Si MOSFETs [111]. Therefore, as compatible drivers for both technologies are mandatory, 4H-SiC and Silicon MOSFETs must have similar threshold voltages. As a consequence, SiO_2 dielectric thickness is near to three times thinner in 4H-SiC MOSFETs than in Si MOSFETs. This result in much higher electric field in the dielectric, and carrier injection becomes a major issue.

Finally, carrier injection has important consequences on reliability. Carrier trapping or generation of interface states [108, 109, 110] may cause threshold voltage instabilities or even dielectric breakdown. This two issues will be detailed below.

1.4.1.2 TDDB

TDDB (Time Dependent Dielectric Breakdown) estimates how long the dielectric can operate until failure. TDDB is temperature and electric field dependent. Temperature and oxide electric field are acceleration factors of dielectric degradation and usually increased to accelerate testing. The estimated TDDB at nominal conditions is then extrapolated from these accelerated tests.

Different acceleration models for TDDB are largely studied by *Kimura* on [112], such as the thermochemical breakdown (linear field dependence) model, the hole-induced breakdown (reciprocal field dependence) model and the modified hole-induced breakdown model for different gate bias stress and temperatures. Tested samples were based on Silicon substrates with oxide thickness between 2.75 and 18.1 nm. It is concluded that thermochemical breakdown model is the most suitable [112].

Fig. 1.30 shows predicted TDDBs for different temperatures, depending on the applied electric field. Even if [112] presents a large study about SiO_2 reliability on silicon substrates,

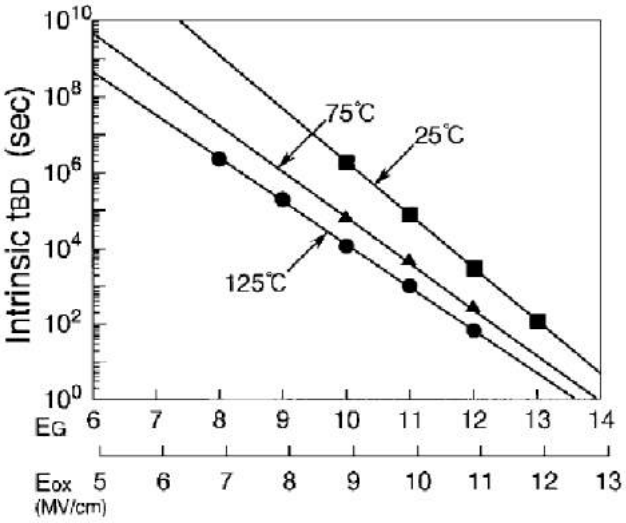


Figure 1.30 – The electric field versus the intrinsic TDDB (t_{BD}) for temperatures of 25, 75 and 125 °C for silicon MOSFETs [112].

some differences must be considered for SiC MOSFETs. First of all, the substrate is obviously SiC, and defects on the substrate could have implications on the oxide reliability. Moreover, as it is expected to use SiC devices at greater temperatures than silicon ones, the oxide reliability must be studied at higher temperatures. A paper presented by *Yu*, focuses on these two issues: higher temperature and SiC substrates [113].

In [113], it is also suggested that substrate material should not affect the dielectric reliability if carrier injection conditions are the same. As the barrier heigh (Φ_b) is lower for SiC than for Si [111], in agreement with the expression (1.25), the electric field applied in the SiC oxide (E_{ox}) should be lower to be in the same carrier injection conditions (J_{FN} is the current density by Fowler-Nordheim injection). Nevertheless, it is known that the electric field applied in SiC devices is higher, as demonstrated by eq. (1.26), where V_{gs} is the applied gate bias, V_{FB} is the flat-band voltage and t_{ox} is the oxide thickness. This is due to the thinner dielectric layer used in order to have the same driving voltages as silicon devices.

$$J_{FN} \propto e^{-\Phi_b^{3/2}/E_{ox}^2} \tag{1.25}$$

$$E_{ox} = \frac{V_{gs} - V_{FB}}{t_{ox}} \tag{1.26}$$

TDDB measurements were performed on 4H-SiC MOS capacitors and DMOSFETs (Double-Implanted Metal Oxide Semiconductor Field-Effect Transistor) between 225 and 375 °C [113]. The applied electric field ranged from 6 to 10 MV/cm. It was found that the field-acceleration factor is around 1.5 dec/(MV/cm) for all temperatures. For a lifetime projection of 100 years, it has been estimated a maximum operating electric field of 3.9 MV/cm and 375 °C, as illustrated in fig. 1.32. It is noticeable that the Weibull slopes (fig. 1.33) are significantly poorer for SiC DMOSFETs than for MOS capacitors, because of the additional processing steps.

In conclusion, SiC MOSFETs structures show good reliability as demonstrated in [113] (e.g. 100 years at $4MV/cm^2$ expected in TDDB, in fig. 1.32). However, further studies are still needed to assess the actual reliability of commercial SiC devices for industrial applications.

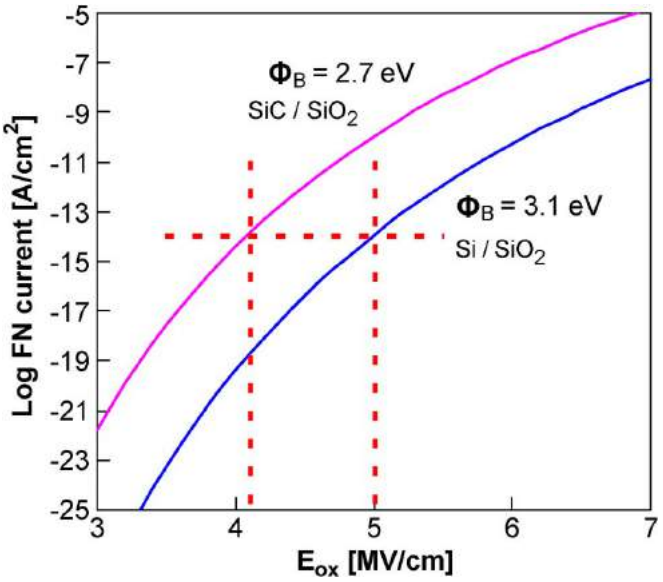


Figure 1.31 – Theorical FN tunneling current at $\Phi_B = 2.7$ and $\Phi_B = 3.1$ ev for SiC/SiO_2 and Si/SiO_2 systems, respectively [113].

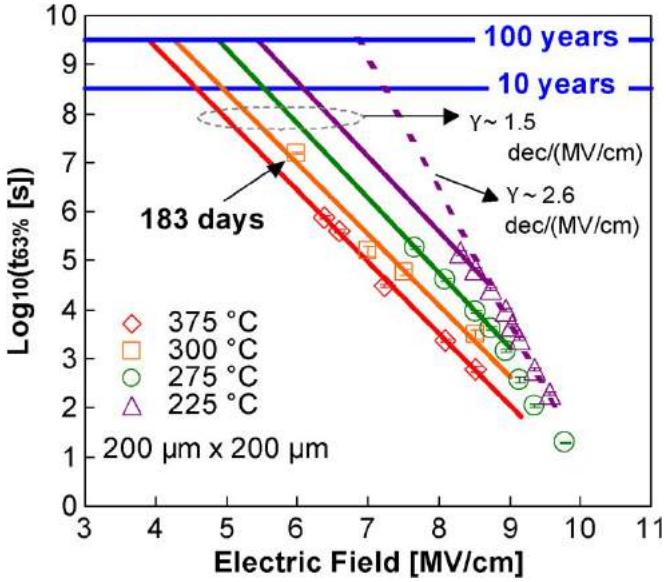


Figure 1.32 – Projection of lifetime based on data measured below 9 MV/cm using the E model [112] and $t_{63\%}$ [113].

1.4.1.3 Bias Temperature Instability

On MOSFETs devices, bias temperature instability (BTI) causes a shift of the threshold voltage, but also of the capacitance as shown in fig. 1.34. This is due to a change in the electrical charge of the oxide or in the SiC/SiO_2 interface. This could be critical for these kind of devices, because an increase in threshold voltage will result in higher conduction losses and eventually in a device thermal runaway. On the contrary, a decrease in threshold voltage may eventually result in a normally-on device.

As explained in section 1.4.1.1, carrier injection and near-interfacial oxide traps generation are the main causes of these instabilities and are temperature and electric field dependent.

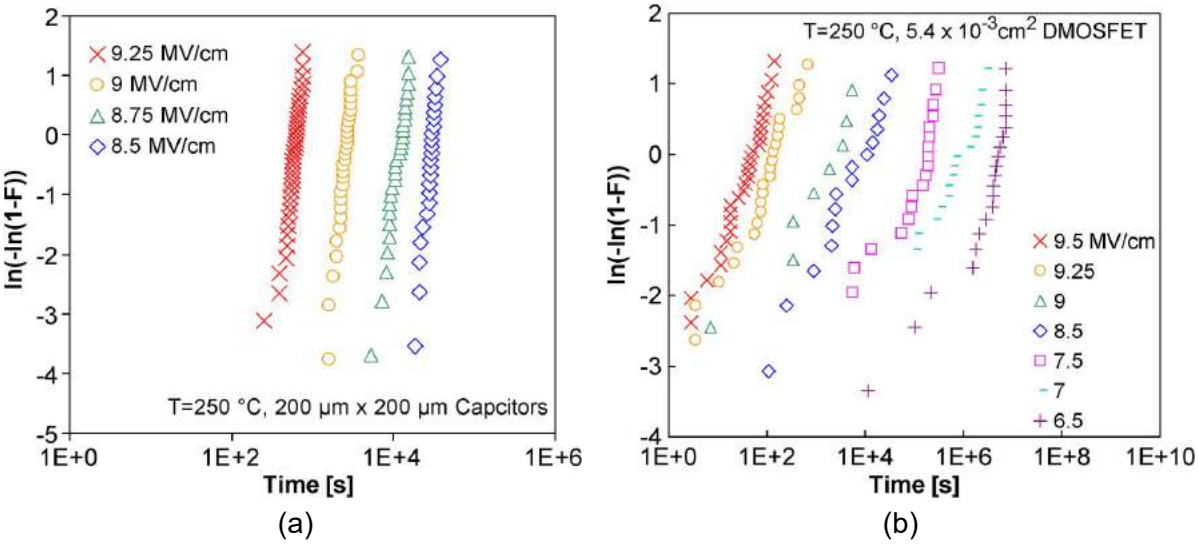


Figure 1.33 – Weibull distributions at 250 °C and different electric fields for (a) MOS capacitors and (b) SiC DMOSFETs [113].

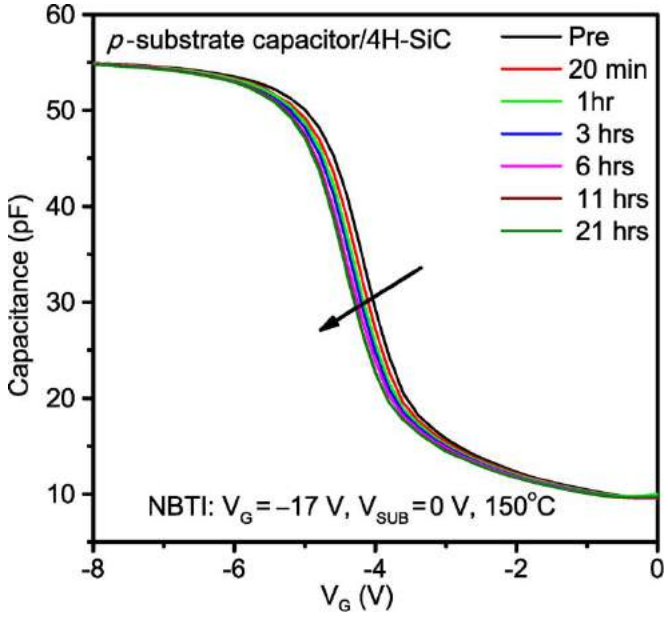


Figure 1.34 – Capacitance as a function of gate voltage stress and stress time for a 300x300 μm p-substrate 4H-SiC capacitor. Stress bias is -17 V on the gate and the temperature is 150 °C [114].

BTI is largely aborded by *Grasser et al.* [115], where it is concluded that classical Reaction-Diffusion models [116, 117] can not explain completely BTI. Moreover, it is found that BTI up at least 1 ks is dominated by inelastic exchanges between prexisting defects and the substrate. Besides, it is suggested that charge trapping creates switching oxide traps, affecting the Fermi level in the substrate, thereby introducing a density of states into silicon band gap.

In [118], an experiment applying negative stress bias at 200 °C results in an important threshold voltage shift for Silicon MOSFETs and voltage flatband shift in MOS capacitors. Nearly all intrinsic trap states existed in Si-MOS structures were identified as Si dangling

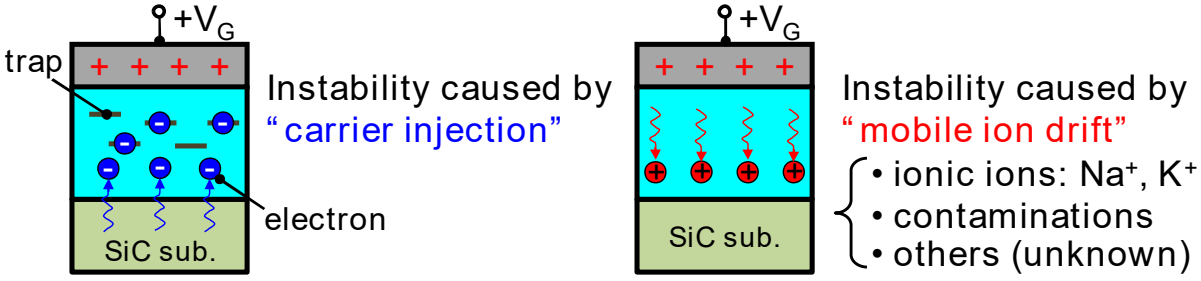


Figure 1.35 – Schematic illustration of BTI in SiC-MOS devices. The two main origins for BTI are carrier injection (left) and mobile ion drift (right) at high temperature, which change the distribution and amount of charge density in the oxides [119].

bonds. They can be passivated by hydrogen annealing, but operation at high temperatures leads to the regeneration of the oxide and interface traps due to hydrogen dissociation [108].

Nevertheless, *Chanthaphan* on [119] suggests that charge trapping and carrier injection would not be the only phenomenons. Indeed, mobile ions would also be responsable of BTI. This phenomenon has also been largely studied for Silicon devices. Typical mobile ions are alkaline ions (K^+, Na^+), hydrogen ions (H^+) and some organic contaminats [120, 121]. Depending on the mobile ions concentration inside the oxide, the threshold voltage might shift dramatically. Moreover, mobile ions concentration is difficult to predict. In this way, as has been done for Si technology, suitable methods to prevent mobile ions on SiC must be developed. Fig. 1.35 shows a schematic illustration about BTI phenomenons in SiC-MOS devices.

A study on SiC MOSFETS [122] realized by *Santini* on commercial devices shows an important threshold voltage augmentation during a positive gate bias stress ($V_{gs} = 30\ \ V$) at 100 °C. As can be seen in fig. 1.36, the threshold voltage increases by up to 25% after 300 hours. This results are in agreement with other results reported by *Yang* [123]. As such, this is unacceptable for industrial applications and further investigations are required.

1.4.2 Internal diode robustness

It is commonly accepted that degradations in PiN junctions are induced by the presence of SF. This is presented in [124, 125] for high voltage SiC PiN diodes, where a forward voltage (V_f) increase is reported under high current density conditions. It was accepted that this degradation phenomenon only affects bipolar devices. However, in 2007, a new degradation phenomenon reporting an increase on the V_f was also reported for the first time on unipolar devices [126].

The robustness of the intrinsic MOSFET diode has been a recurrent research issue for the last years. *Agarwal et al.* reported this degradation phenomenon [126] on high-voltage MOSFETs. The authors deduced that as a result of internal diode forward biasing, recombination-induced SF reduces the majority carrier conduction current and increases the leakage current in blocking mode. This is illustrated in fig. 1.37, where it is shown that these effects evolve in function of stress time (reduction of the majority carrier conduction current can be observed in fig. 1.37 (a) and (b), whereas the leakage current increase can be observed in fig. 1.37 (c)). The devices under test in [126] are 10 kV 4H-SiC DMOSFET. It worth noting that this effect is more noticeable for high-voltage devices, which have a thick epitaxy layer. It is not expected to affect 600-1200 V devices.

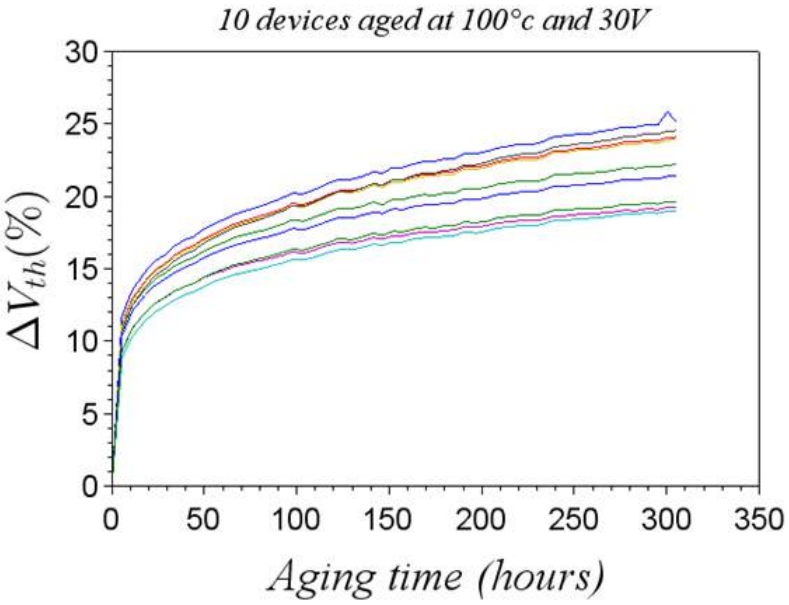


Figure 1.36 – threshold voltage instability for 10 SiC MOSFETs under stress conditions of $V_{gs} = 30\ V$ and 100 °C [122].

While this degradation phenomenon has been observed on MOSFET devices, other unipolar devices such as Schottky diode or JFET may be concerned. At Ampère Laboratory, *Mr. Younes Hamieh* investigated the degradation associated with the biasing of the body diode of a JFET [86]. A 8 A forward intrinsic diode stress was applied on a 1200 V 15 A rated SiC JFET for 64 hours. During the test, the JFET device was in the off-state. As a result, no noticeable augmentation of internal resistance or current saturation was reported. 64 hours correspond to more than 4,500 hours of operation for the diode in a 10 kHz inverter (assuming a dead-time of 500 ns).

Similar studies were carried on commercial Wolfspeed SiC MOSFETs [128, 127]. In [128], the internal diode of 20 4H-SiC 1200 V MOSFET were submitted to a 22 A forward current stress for 1000 hours. As a result, characterizations realized after stress, showed a forward voltage increse of 0.8% . Thus, this parameter can be be considered close to stable. A similar experience was carried in [127], also 4H-SiC 1200 V MOSFETs, from CREE (Generation 2, 20 A rated). As reported by [128], results presented in [127] shows that the internal diode forward voltage remains stable after being stressed at 10 A for 1000 hours. This is illustrated by fig. 1.38.

In conclusion, it seems that the PN junctions of present commercial SiC 1200 V MOSFETs have a good robustness. As shown in [126], higher voltage devices may be more sensitive to SF defects due to their thick epitaxial layer. For such devices, the robustness of the intrinsic diode remains an important reliability issue. However, even for low voltage devices, there are questions about the reliability of the intrinsic diode which have not been addressed yet. One of the objectives of this thesis is to investigate the behaviour of the intrinsic diodes of MOSFETs, in particular to analyse their robustness under inductive switching conditions.

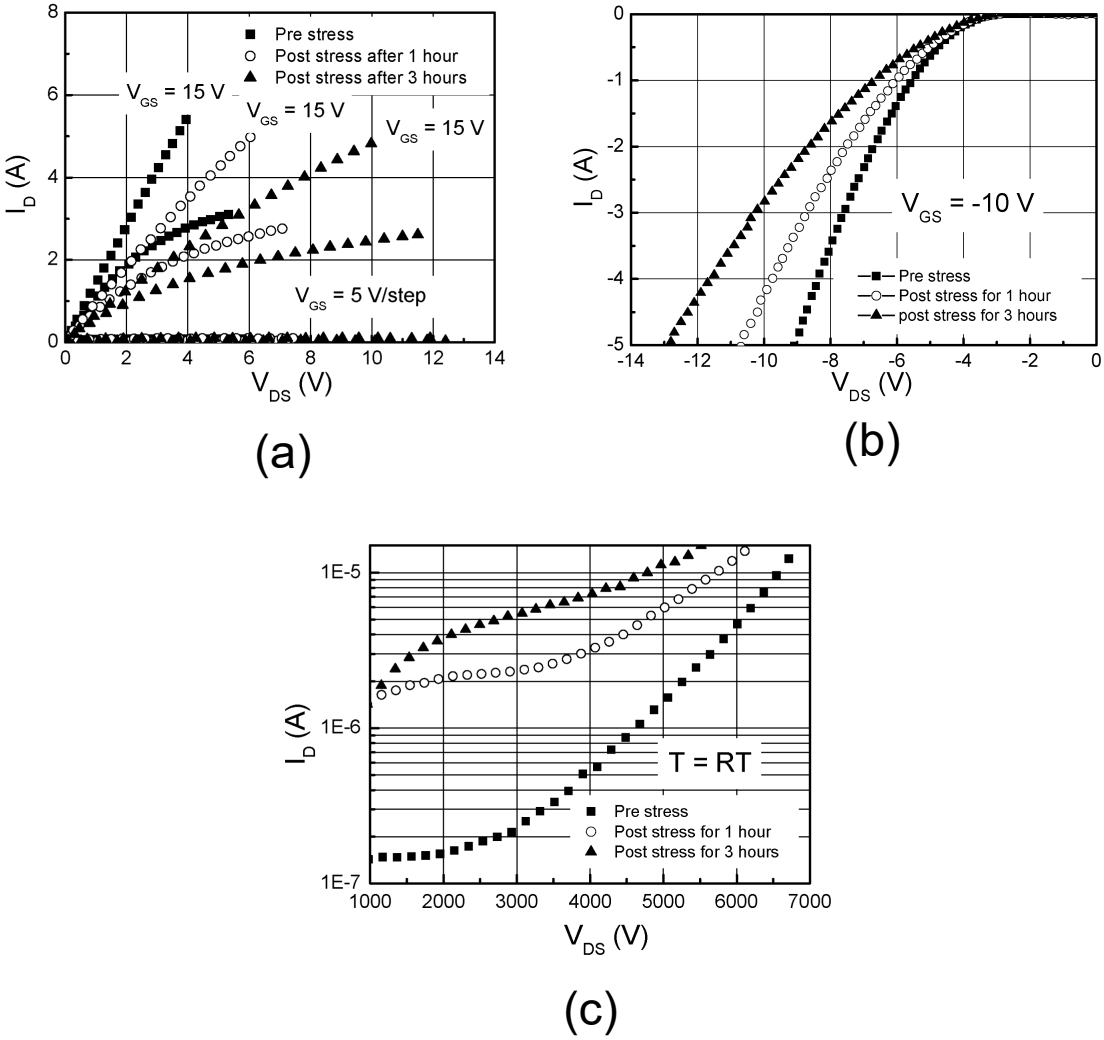


Figure 1.37 – (a) Forward I-V characteristics of a 10 kV DMOSFET before and after stressing the body diode at 5 A. Curves with gate voltage of 0, 5, 10 and 15 V are shown. Curves with gate voltage of 0 and 5 V are overlapping. (b) Degradation of the forward I-V characteristics of the built-in body diode before and after stress of 5 A. (c) Forward leakage current of the 10 kV DMOSFET at room temperature before and after stress of the body diode at 5 A [126].

1.4.3 Robustness under avalanche breakdown phenomenon

One of the SiC devices advantages is their capability to switch faster than Si devices. A short (on the order of 10-20 ns) transition time between on-off states reduces switching losses. However, fast switching causes the apparition of large voltage oscillations between drain-source terminals, which are accentuated by inductive loads. This, results in voltage levels much higher than the nominal bus voltage, and eventually well above the rated device voltage. In this case, the breakdown voltage phenomenon appears. Therefore, it is necessary to study the reliability of SiC devices in the case of avalanche events.

It is known that MOSFET devices have two failure modes under avalanche conditions [129]. The first one is parasitic BJT latch-up due to high avalanche energy over a short time [21]. Par-

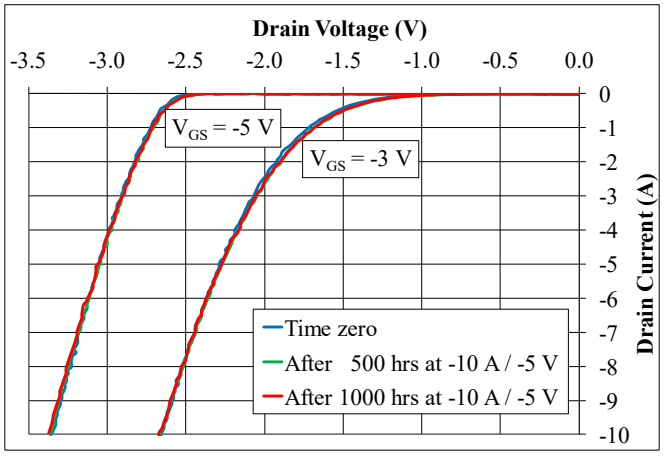


Figure 1.38 – Typical body diode characteristics of 1200 V MOSFETs at time-zero and after 500 hours and 1000 hours of third-quadrant stress (10 A current and -5 V gate bias) [127].

asitic BJT latch-up occurs due to a voltage drop between source and p-body regions, resulting in the forward voltage biasing of the emiter-base junction. This phenomenon can be aggravated by non-uniform distribution over the different cells of the device, resulting on current and temperature focusing (hot spot) [129, 130]. The second failure more is related to intrinsic temperature limitations of the device in the case of low avalanche current maintained over a long time [131]. This corresponds to the case of large inductive loads.

For JFET devices, once avalanche occurs, the current flows initially into the gate-drain diode, increasing the gate voltage (due to internal and external gate resistance). When the threshold voltage is reached, the device turns on in saturation mode, so the avalanche current is diverted to the channel [132]. This results in an important increase of the junction temperature. Nevertheless, as opposed to MOSFET devices, the JFETs do not have any BJT parasitic structure nor any gate oxide layer. This results in a better exploitation of the SiC material characteristics and it is expected to be more reliable to avalanche events than devices such as the MOSFET.

In the case of BJT devices, the breakdown mechanism is quite similar to that of p-n junctions [39]. A high electric field in the base-collector depletion region causes carrier multiplication due to impact ionization. This phenomenon is not destructive by itself, but as a result temperature can increase dangerously, provoking device failure.

It is worth noting that for BJT devices, the avalanche phenomenon is dependent of device configuration. There are two possible configurations, common-base mode or common-emitter mode [39]. In power electronics, the usual configuration is common-base mode and breakdown voltage usually refers to this configuration. The breakdown voltage in common-emitter mode is much lower. In addition, for bipolar devices such as BJTs, another phenomenon called second breakdown voltage appears [21]. This can cause local high-current densities in the device, resulting in thermal runaway and device failure.

The literature regarding BJT avalanche robustness is not so rich, but some studies have been carried. An interesting work, presented by *Cheng* [133], compares BJT, JFET and MOSFET devices under avalanche conditions. In fig. 1.39, it is shown a destructive avalanche event on a BJT. With a bus voltage of 400 V and a collector current of 11 A, an avalanche event appears

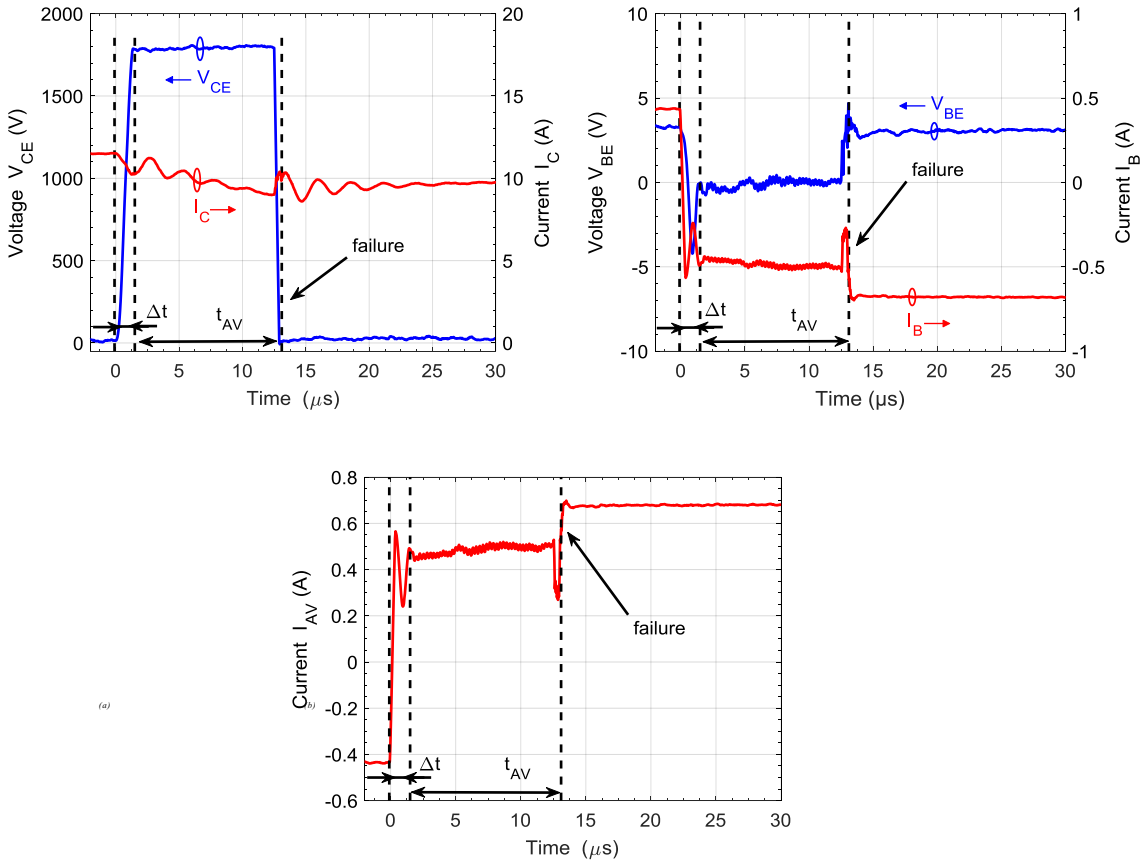


Figure 1.39 – Destructive test of BJT (a) Drain voltage/current, (b) Gate voltage/current, (c) avalanche current for $U_{dc} = 40\ V$, $R_g = 22\ \Omega$, $T_{case} = 25\ °C$[133].

when the transistor turns off, resulting in a collector-emitter voltage of 1800 V. Under these conditions, the device fails after 12 μs, for a dissipated energy of 217.8 mJ.

The behaviour of BJTs and JFETs until failure seems to be very similar, and both devices fail at comparable dissipated energy level due to a thermal stress [133]. In the case of JFETs, failure occurs after 8-9 μs and near to 200 mJ for a bus voltage of 400 V and a maximal drain current of 24 A. During the avalanche event, the drain-source voltage was near 1800 V. This result is slightly lower than that repported by *Friedrichs* in [134], where the study of a VJFET robustness during to avalanche events is presented. Concretely, it is reported a dissipated energy of 350 mJ during near to 17.5 μs. However, even if the voltage was similar, source-drain current was much lower (near to 5 A in [134] vs near 25 in [133]). Thus, it seems evident that in [134], device thermal stress was not so demanding.

Concerning SiC MOSFETs, *Cheng* suggest that the failure mode is due to the activation of the parasitic BJT and not to thermal stress [133]. As a result, SiC MOSFET failure appears after 1.5-2 μs for a low dissipated energy level (8-9 mJ). Reported experience is illustrated in fig. 1.40. Anyway, there is no consensus about the failure mode. In [135], *Fayyaz* finds that failure is due to temperature increase, reaching a junction temperature of 510 °C. In this case, different avalanche event durations and different current levels are used, but the dissipated energy is always found to be 1.2 J. Avalanche event duration goes from 38 μs to 48 μs until failure, depending on case temperature, current level and inductance value. In fig. 1.41, a unclamping inductive switching test is shown [135]. It is noticeable, that in [135], an

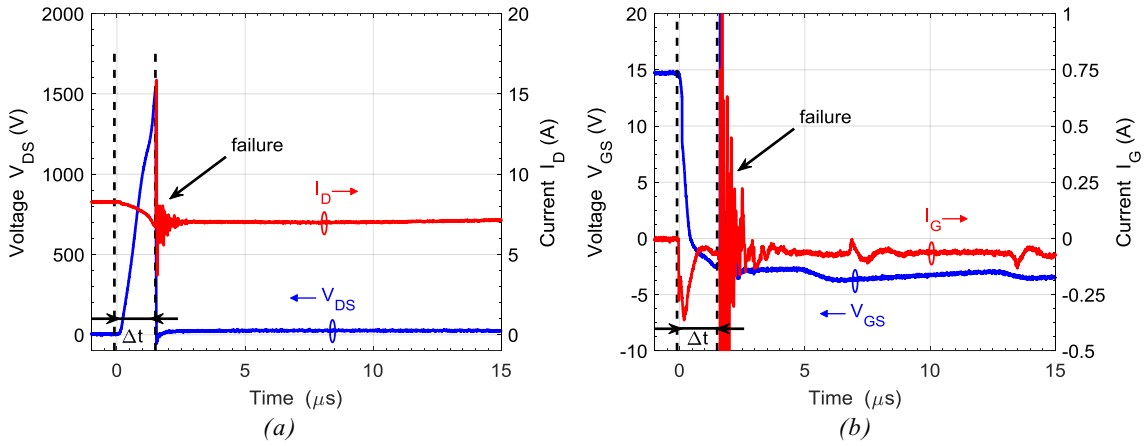


Figure 1.40 – Destructive test of MOSFET SCT2080KE (a) Drain and (b) Gate waveforms for $U_{dc} = 40$ V and $T_{case} = 25$ °C [133].

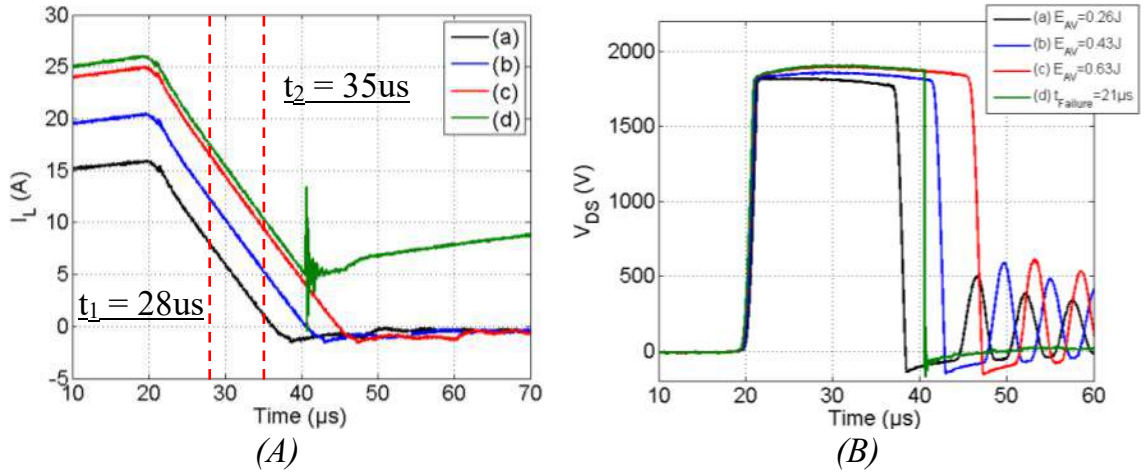


Figure 1.41 – Tests under unclamping inductive switching. (a) Load current I_L (b) Drain-source voltage V_{ds}. $T_{case} = 27$ °C [135].

important threshold voltage shift is reported after repetitive avalanche tests. This results in a threshold voltage increase, which in agreement with [135] would be due to the interfacial charge (electrons for n-channel) trapped at and near the $SiO_2 - SiC$ interface and therefore leading to a significant degradation of device performances.

Differences between [133] and [135] could be related to several factors. Even if in all cases devices are 1200 V rated, device structure, manufacturer or even device generation can differ, resulting on different results.

In order to compare the robustness of different devices under an avalanche event, table 1.6 summarizes time and critical energy for different devices until failure. In order to compare device robustness under the same test conditions, only the results presented on [133] are summarized. Concerning SiC MOSFETs, even if energy and duration events presented in [135] show a very good robustness, the poor results presented on [133] remind us that SiC MOSFETs technology is not mature. Comparably, it seems that JFET and BJT devices have a relatively good robustness to avalanche events.

Device structure	Time until failure (μs)	Dissipated Energy (mJ)	Failure mode
SiC MOSFET	1.5 - 2	6.9 - 8.1	Parasitic BJT latch-up
SiC BJT	12	217.8	Thermal stress
SiC JFET	8 - 9	199 - 212	Thermal stress

Table 1.6 – Summary of robustness for MOSFET, BJT and JFET devices under avalanche tests at $U_{dc} = 40\ V$, $T_{case} = 25\ °C$ [133].

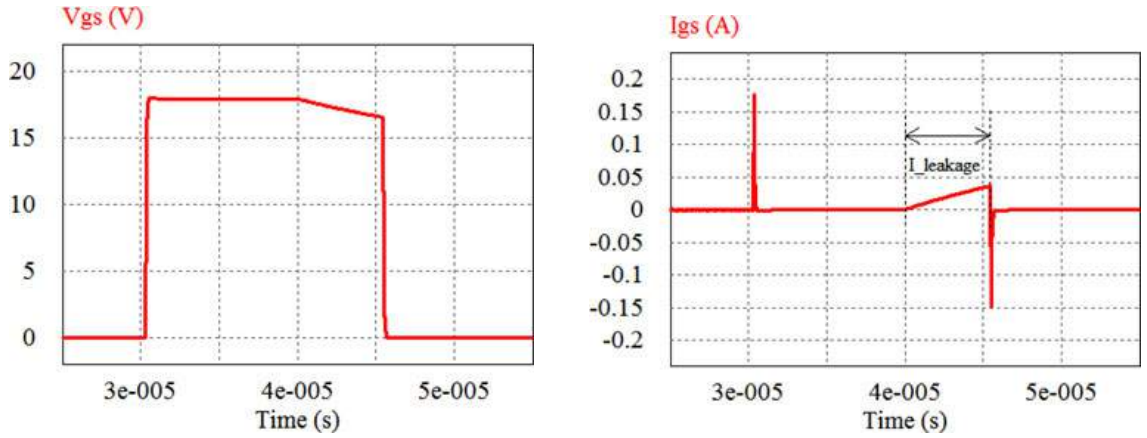


Figure 1.42 – Simulation of the gate-source voltage V_{gs} and gate-source current I_{gs} behaviour under short circuit event [111].

1.4.4 Robustness under short-circuit conditions

Another condition affecting power device reliability is its robustness to transient short circuit events. This type of event takes place regularly in power electronics applications such as inverters. Thus, study and comparison of different power devices and technologies is required to protect the system [111].

The literature shows that SiC MOSFETs robustness towards short-circuit events is lower than that of silicon MOSFETs. This could be related to the gate oxide [111, 136]. Even if SiO_2 is used in both technologies, its thickness is about three times smaller for SiC MOSFETs (see section 1.4.1.1) because of industry requirement to be voltage compatible with silicon based devices and their gate drivers.

This means that the electric field in the oxide tends to be significantly higher for SiC devices. This impacts gate oxide reliability, because the electric field, together with the temperature, was found to be an accelerator factor of the oxide failure, as was explained in section 1.4.1.2.

Under short-circuit conditions, a high power density is dissipated in a short time. This locally provokes a dramatic rise of the junction temperature. The Fowler-Nordheim current increases with temperature and electric field. Then, under short-circuit conditions, the gate leakage current increases, favouring gate oxide degradation. This is not observed with Si based MOSFETs because of the lower electric field in their oxide layer. Fig. 1.42 illustrates this phenomenon. The short-circuit event starts when the driver triggers the MOSFET gate at 30 μs. After 10 μs, it is observed that the gate voltage starts to decrease and simultaneously

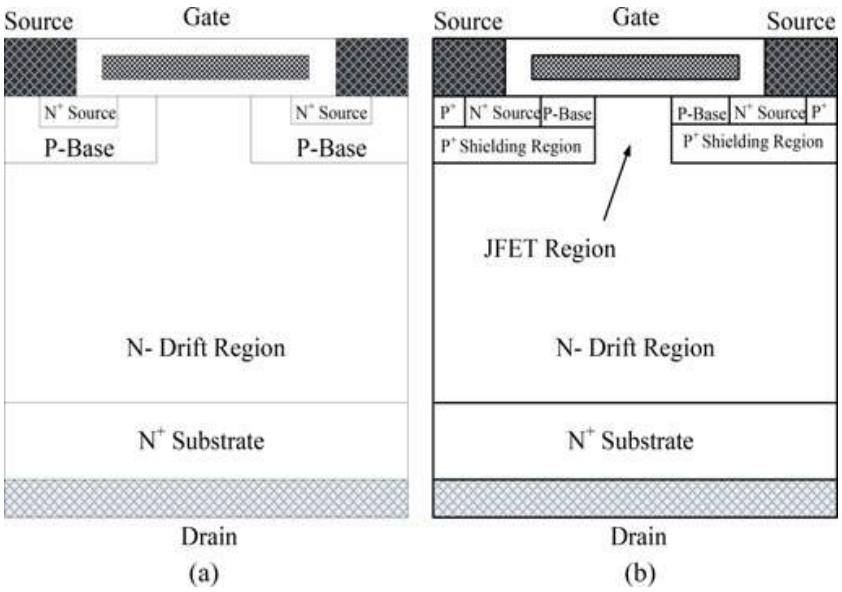


Figure 1.43 – Structures of Si and SiC MOSFETs (a) Planar MOSFET structure (b) Shielded planar MOSFET structure [111].

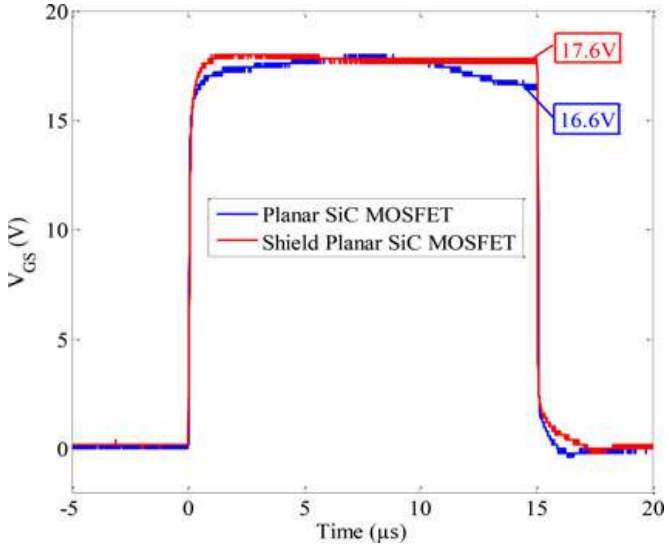


Figure 1.44 – Reduction in gate-source voltage for planar SiC MOSFET and Shield planar SiC MOSFET [111].

the gate current increases until the end of the short-circuit event.

However, this phenomenon differs depending on the device structure, as was shown by *Nguyen et al.* in [111]. Concretely, this paper compares oxide reliability between a planar MOSFET structure and a shielded planar MOSFET structure. Both structures are illustrated in fig. 1.43. Fig. 1.44 shows waveforms of the gate voltage for both structures under a short-circuit event. As it can be seen, the shielded planar structure remains stable during the whole short-circuit event. It is not the case of the MOSFET designed using a planar structure, which shows a relaxation of the gate voltage after 10 μs.

At lower gate-source voltages, this phenomenon is less important. It is showed that for the same planar MOSFET, when the gate-source voltage is reduced to 15 V, it remains practically

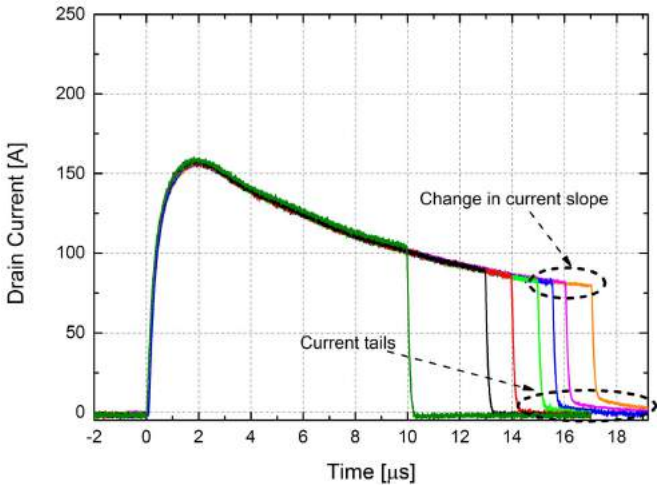


Figure 1.45 – I_d short-circuit waveforms ($V_{ds} = 400\ V$, $V_{gs} = 18\ V$, $T_{case} = 27$ °C, CREE) [137].

stable during the entire short-circuit event [111]. This is due to two reasons. First, the saturation current is reduced, limiting the power dissipation of the device and consequently the maximal temperature reached during the short-circuit. Second, as the gate-source voltage is lower, so is the electric field of the oxide. This results in a lower gate-source leakage current.

Nguyen et al. also studied the effect of repetitive, non-destructive short-circuit events [111]. Concretely, a sequence of 15 μs short-circuit events with a drain-source bus voltage of 500 V and gate-source voltage of 18 V is repeated for 50 times. It is shown that the gate-source voltage decreases slightly after 50 sequences and that the leakage gate current increases. The authors suggest that repeated sequences of FN injection through the gate oxide create some defects in the insulator, resulting in a leakage current increase and eventually in device failure.

Regarding destructive short-circuit test, it has been shown that SiC MOSFET devices can sustain short-circuit condition for a few μs only. This duration depends on the gate and bus voltage. In this way *Romano et al.* [137] present a study at different bus voltages with several short-circuit durations. It is shown that for low voltage (below 200 V), the devices are capable to sustain a short-circuit for a relatively long time. Concretely, failure occurs after 85 μs. Nonetheless, time until failure is drastically reduced at higher voltages: for a bus voltage of 400 V, it is down to 17 μs. This time is reduced to 5.5 μs with a bus voltage of 800 V. These tests results are supported by thermal simulations, which indicate a dramatic temperature rise, far higher than the aluminium melting point. Tests at at 400 V are illustrated by fig. 1.45, were current tails phenomena indicate that in the off state an important leakage current remains for short-circuits durations greater than 15 μs, because of the temperature increase [137].

A recent study was carried by *Cheng* [133] in the course of his PhD thesis. Several types of 1200 V SiC MOSFETs from two different manufacturers were studied under short-circuit conditions with a bus voltage of 600 V. Short-circuit event duration until failure was found to be comprised between 12.5 μs and 19 μs. These results are in agreement with [137] and other studies such as [138]. In [133], the energy dissipated during the short-circuit events was calculated. It is comprised between 0.7 and 1.78 J.

In the same study, BJT SiC devices were also studied under the same conditions reporting a dissipated energy until failure between 0.25 J and 0.32 J depending on the base current. Time

until failure can be very variable depending on the base current, more concretely, reported times before failure in [133] were comprised between 9 and 32 μs for gate current levels of 0.6 and 0.2 A respectively. This failure times are in the same order of magnitude than reported by other publications such as [139, 140] for similar test conditions (20 and 10 μs) respectively.

The SiC device presenting the best short-circuit robustness is the JFET. It is shown in [141] where the author compares SiC MOSFETs and JFETs. Presented tests exhibits a time before failure of 1.4 ms for JFETs and 13 μs for SiC MOSFETs ($V_{gs} = 18\ V$), always using a bus voltage of 600 V. In spite of this, the critical energy per surface for every device is relatively similar: 10.01 J/cm^2 for the JFET, compared to 6.8-12.8 J/cm^2 for the MOSFET. This is in agreement with [142], where a time before failure of 1.4 ms was also reported for a JFET. As is suggested in [142], the better performances of the JFET in the case of short-circuits are due to its higher channel mobility and its negative temperature coefficient, resulting in lower internal resistance and saturation current.

The short-circuit behaviour of different SiC is summarized in table 1.7. Thanks to its low saturation current, the JFET is able to sustain short-circuit over a much longer time (1.4 ms vs. tens of μs for the other devices), while dissipating a low power. This results in a low critical energy for the JFET despite the long duration of the short-circuit.

The BJT was also expected to be robust in short-circuit conditions, because it has no oxide layer and because it is supposed to have a coarser die layout. This is not confirmed by the experiments reported in the literature, with critical energies and failure time lower than those of MOSFETs.

SiC MOSFETs are capable to sustain a short-circuit for some μs (12-18 μs). Results of table 1.7, shows that the dissipated energy par surface is between 6.8-12.8 J/cm^2.

Device structure	Device	Rated current (A)	Die size (mm^2)	Time before failure	Dissipated energy (J)	Dissipated energy per surface (J/cm^2)
MOSFET	CMF20120D	42	12	16 μs	1.15	6.95
MOSFET	C2M0080120	31.6	10.4	12.5 μs	0.71	6.82
MOSFET	SCT2080KE	40	12.58	18 μs	1.61	12.79
BJT	FSICBH057A120	31.6	3.6	9 - 32 μs	0.25 - 0.32	3.39 - 4.81
JFET	SJEP120R063	30	4(x2)	1.4 ms	0.8[a]	10.01

Table 1.7 – Times and energy until failure for different types of SiC 1200 V devices for a bus voltage of 600 V[141, 133, 143].

[a] Energy dissipated after 800 μs without faiure. Failure occurs after 1.4 ms, but author does not reports the energy. Idem for energy density.

This energy par surface is comparable to that of 1200 V Si IGBTs, which for similar short-circuit conditions (540 V) exhibits a critical energy par surface of 10.25 J/cm^2 [144]. Thus, also from a robustness point of view the SiC MOSFET could be in concurrence with Si IGBT.

1.5 Conclusions

In this chapter the main properties of SiC were presented and compared to those of Si (see section 1.1). As a result, we highlighted the advantages of SiC for power devices. However, SiC substrates still show some reliability issues related to crystallographic defects, as related in section 1.2. These defects have been delaying SiC power devices development for long time, restricting it to academic research. Recently, most of these issues have been overcome, and many academic studies now focus on evaluating the performance of SiC power device structures. These structures are presented in section 1.3, and they are BJT, JFET, MOSFET and IGBT.

Among these devices, BJTs and JFETs present some drawbacks for the industry. The first one is a current controlled device, while the second is a normally-on device. These characteristics are in opposition with industry standards, which prefer devices with high input impedance (voltage controlled) and which remain in the off state in the case of driver failure. As a result, the MOSFET is the most attractive device structure, and seem to be the alternative being considered by the industry for applications below 10 kV. SiC IGBTs would be an alternative only for higher voltages, but they are currently under development, and no commercialization is expected in the short term.

However, the manufacturing process of SiC MOSFETs is complex, and some reliability issues remain. They are presented in section 1.4, and are related to the gate oxide, the intrinsic diode and to the behaviour under avalanche and short-circuit conditions. Short-circuit and avalanche phenomena are common reliability issues of all the presented devices. A brief state of the art regarding these devices has been presented.

This thesis will focus on two intrinsic reliability issues of the SiC MOSFET: intrinsic diode degradation and the reliability of the gate oxide. They are presented in chapters 2 and 3 respectively.

Chapter 2

Robustness of the MOSFET internal diode

Contents

2.1 Introduction

SiC devices are especially attractive for power applications. For example, replacing Si IGBTs with SiC MOSFETs, allows important loss reduction, which, associated with better thermal and frequency performances, may yield to a reduction of the system dimensions.

However attractive the material is, the commercial development of SiC devices faces technological challenges about defect elimination. Among them, dislocation issues and micropipes have limited for a long time the forward-blocking capacity of SiC devices at high voltages, one of SiC most promising applications. Besides, the electron mobility in the SiC MOSFETs channel is limited because of the presence of crystal defects and interface states.

Although manufacturers have considerably minimised these defects for the last commercialised SiC devices, these are not fully controlled yet and some reliability problems remain, as presented in chapter 1. Among these issues, there is the degradation of the internal diode.

In this chapter, the robustness of the internal diode of SiC MOSFETs is assessed under static, but also under realistic (switching) operating conditions. This work is oriented towards aeronautical applications (inductive switching and a bus voltage of 540 V, corresponding to the future aircraft HVDC network). The objective is to study whether current commercial SiC MOSFET devices could be used in diode-less applications.

An example of such application is an inverter where the transistors are mounted without antiparallel diodes. Diode-less converters require fewer components and may reduce losses, hence a more compact,efficient and cheaper system. In such conditions, [145] reported a drift

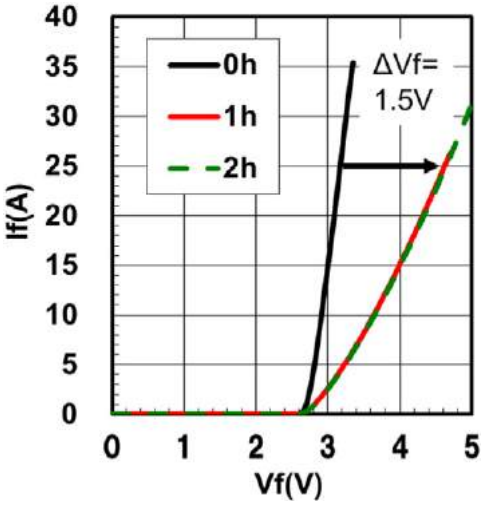


Figure 2.1 – Typical forward current-voltage characteristics of pn-junction-based body diode in a conventional SiC MOSFET after applying forward current of 15 A [145] (2016).

in the voltage threshold of some MOSFETs. We also monitor this parameter, which is especially important, as it has consequences on the gate drive circuit design.

To evaluate the robustness of the internal diode of SiC MOSFETs, some tests are presented in this chapter. Firstly, several static test stressing the internal diode are realized, with regular MOSFET characterizations to evaluate possible degradations.

Secondly, we focus on a more realistic case. The MOSFETs are placed in a real converter, with inductive switching conditions, a bus voltage of 540 V and at their maximal operation temperature. The influence of MOSFET switching and operation duty cycle is analysed.

2.2 Context

As it has been presented in chapter 1, MOSFET internal diode stresses could result in two principal reliability issues. The first one, an increase in the diode forward voltage, increasing losses. The second is a shift in the voltage threshold of the MOSFET. This could result in more resistive devices due to a voltage threshold increase. In this case, thermal runaway could be the principal risk. In the case of a negative voltage threshold shift, the MOSFET could become a normally-on device or simply more sensitive to EMI (Electromagnetic interference). In either case, it might cause dramatic failures.

A commonly used solution to avoid any P-N junction degradation is to use a Schottky diode in an antiparallel configuration. This solution also offers advantages such as faster recovery time and perhaps lower losses. However, it has the downside of requiring more components. An intermediate solution is a structure integrating a Shottky diode in the MOSFET die [146, 145].

When no schottky diode is used, *Kusumoto et al.* showed [145] a forward voltage shift in the case of an internal diode stress at 15 A. This is illustrated by fig. 2.1, where there are no changes in the built-in voltage V_{bi}, but in the series dynamic resistance; probably due to a degradation of the source metallization. In addition, a threshold voltage drift of the channel was also observed in two different cases (both at 150 °C): the first one, for a gate bias of 20 V, and the second one at V_{gs} =-10 V. These two cases are illustrated in fig. 2.2. Finally, it was

shown [145] that integrating an antiparallel diode in the MOSFET die within epitaxial grown improvements these two issues could be avoided.

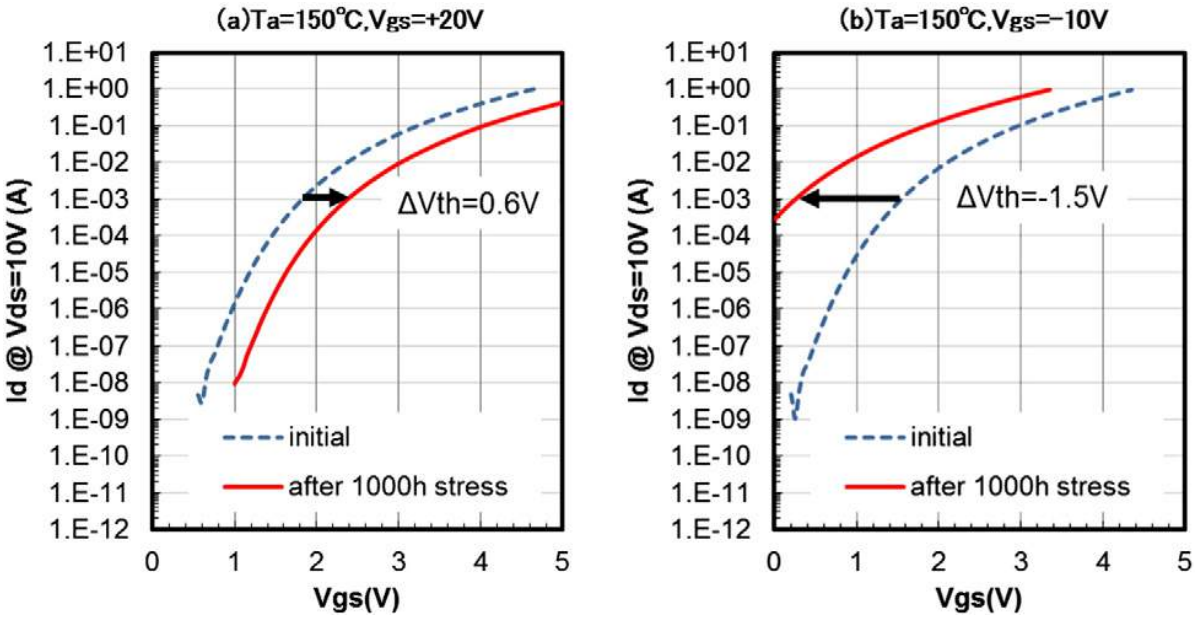


Figure 2.2 – Typical data of Vth shift after the application of an HTGB test (a) positive bias stress V_{gs}=20 V (b)negative bias stress V_{gs}=-10 V over 1000 hours at 150 °C [145] (2016).

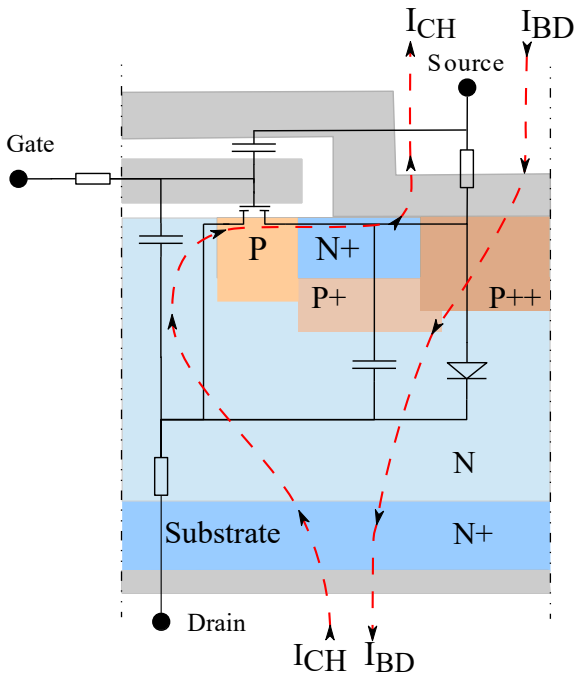


Figure 2.3 – Typical SiC NMOSFET cross section and its parasitic elements. I_{BD} and I_{CH} refers to current flowing through the body diode and channel paths, respectively.

It is worth noting that most of the papers studying body-didode focus on diode forward voltage evolution and the threshold voltage of the MOSFET is not characterized [145, 147].

Thus, this issue requires further investigation and results presented in sections 2.3 and 2.4 will show that body-diode stress may cause a shift in voltage threshold.

Figure 2.3 shows a typical MOSFET structure and the current paths I_{CH} when the current flows through the channel and I_{BD} when it flows through the internal diode. As it can be seen, the structure of a SiC MOSFET is comparable to that of a Silicon MOSFET. Moreover, as in silicon the body diode current does not flows near to the gate oxide. Thus, voltage threshold shift was an unexpected phenomenon.

2.3 Static tests

As introduced, several preliminary static test are realized in order to be used as a reference. The results are compared later with those obtained from inductive commutation tests, in order to draw some conclusions about the degradation phenomenons.

The main JEDEC standard tests [148] are summarized in annex A.1 alongside with some non-standard tests. In all cases, devices under test are Wolfspeed SiC MOSFETs (C2M008012D) [149]. It is noticeable that devices were purchased in two batches: a first (Ref. W14514, year 2014) for HTGB test and a second (Ref. W10116 and W10216, year 2016) for Q1,Q3 and Q4 tests.

Characterizations are realized using an Keysight B1505B curve tracer as described in annex A.2. Special attention requires the characterisation of the threshold voltage. In this way, devices are blocked initially at $V_{gs} = -8\ V$and the gate-source voltage is increased progressively until to reach the conditions chosen to define the threshold voltage (I_{ds}=100 μA at V_{ds}=1 V). The fact to block the device initially at $V_{gs} = -8\ V$assures the measure repeatability, as shown in annexe A.2.

Initially, the only static test we intended to perform was a HTGB (High Temperature Gate Bias) test, which is presented in section 2.3.1.2. However, the results of the inductive switching tests, which are presented in section 2.4, forced us to investigate further the effects of static stresses. Thus, three different static tests are run. One with a negative gate bias and a source drain current flowing through the internal diode (Q3); the other two tests are run at positive gate bias in the two current directions, drain to source (Q1) and source to drain (Q4). These are described in section 2.3.1.3. All the data of the different tests are summarized in annexe A.6.

In some of these tests, the device under test dissipates a significant amount of power. A method is developed to estimate the junction temperature of the DUT during these tests. Its principle is described in section 2.3.1.1, and more details are given in annexe A.4, together with an uncertainty calculation of the junction temperature.

2.3.1 Description of the set-ups for static tests

2.3.1.1 Junction temperature estimation

Estimation of junction temperature using thermosensitive parameters (TSP) has been largely discussed in the litterature [150, 151]. An accurate estimation of the junction temperature is important in order to test the devices without exceeding their maximal junction temperature, as it could trigger the apparition of some other degradation mechanism.

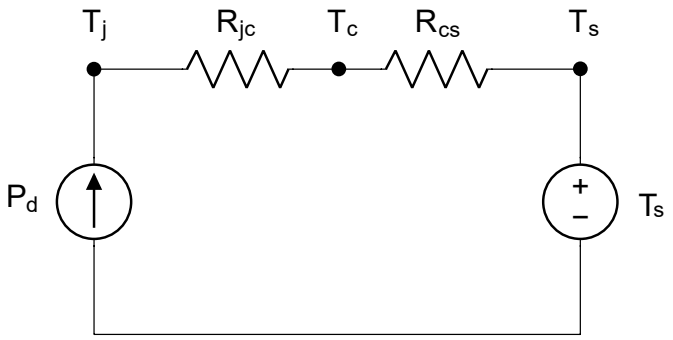


Figure 2.4 – 1st order MOSFET steady-state thermal model

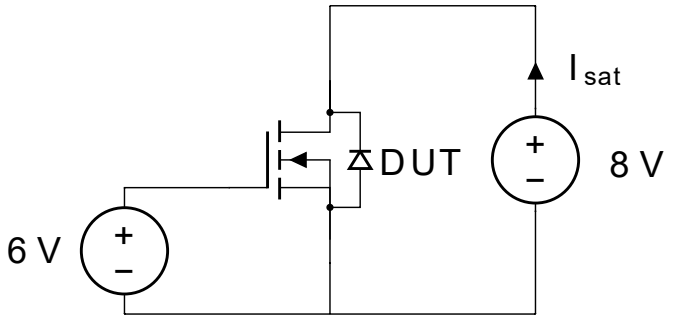


Figure 2.5 – Biasing conditions for the measurement of $I_{sat} = f(T)$ characterization.

A simple thermal model at steady-state is given in fig. 2.4. The corresponding junction temperature can be calculated using equation (2.1). T_j and T_s are respectively the junction and hot-plate temperature, P_d is the power dissipated by the device under test, and $R_{th_{jc}}$ and $R_{th_{cs}}$ are respectively the junction-case and case-sink thermal resistances.

$$T_s = T_j - P_d \cdot (R_{th_{cs}} + R_{th_{jc}}) \tag{2.1}$$

In our test setup, T_h is regulated at a constant value, and $R_{th_{jc}}$= 0.65°C/W in agreement with the datasheet [149].

To determine $R_{th_{cs}}$, the saturation current (I_{sat}) is characterized (using an Keysight B1505B curve tracer in pulsed mode and a Thermonics T-2500E/300 thermal conditioner) over a temperature range from 60 °C to 150 °C (with 10 °C steps), in agreement with fig. 2.5. The resulting I_{sat} characteristic can be fitted using a second order polynomial by equation (2.2) and be used as a thermo-sensitive parameter for the estimation of T_j.

$$I_{sat}\Big|_{V_{gs}=6\ V\ V_{ds}=8\ V} = 6.10^{-5}\ T^2 + 6.6.10^{-3}\ T + 0.5536 \qquad [A] \tag{2.2}$$

Once the MOSFET is characterized, it is assembled on the hot plate (see fig. 2.6) together with a Thermal Interface Material (TIM) layer (SIL-K10 from Bergquist). The device is excited at the same operating point used for the characterization (V_{gs}=6 V, V_{ds}=8 V). Using eq. (2.2), it is then possible to calculate the junction temperature from the measured I_{sat} value at equilibrium (I_{sat}= 2.11 A, corresponding to a junction temperature T_j= 117 °C). As the dissipated

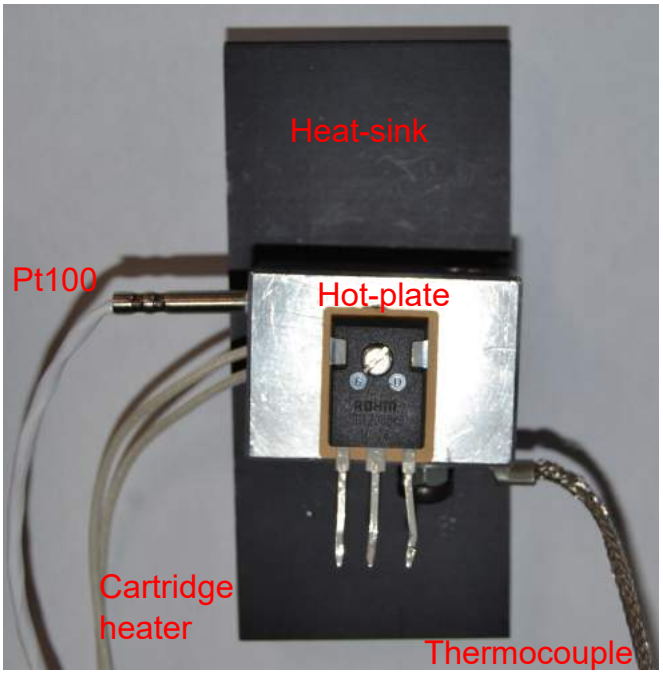


Figure 2.6 – DUT assembled within the hot-plate.

power is the product of I_{sat} and V_{ds}, T_s= 80 °C, and $R_{th_{jc}}$= 0.65 °C, $R_{th_{cs}}$ is calculated using equation (2.3).

$$R_{th_{cs}} = \frac{T_j - T_s}{V_{ds} \cdot I_{sat}} - R_{th_{jc}} = \frac{117 - 80}{16.88} - 0.65 = 1.54 \qquad [\,°C/W] \tag{2.3}$$

Thus, using equation (2.1) and measuring the dissipated power, it becomes possible to determine the required heat-sink temperature to maintain the junction temperature of the DUT under the maximum value specified in the datasheet [149].

2.3.1.2 HTGB Test

In the literature, several studies based on JEDEC tests [148] (static conditions of operation) report a threshold voltage drift [123]. For the sake of comparison, we also perform a HTGB test (see fig. 2.7) on 10 devices. Test conditions are the same as for the CMB (Chopper Mode Bias) test bench ($V_{dd} = 540\ V$, $V_{gs} = -8\ V, T_j = 150$ °C), which is be presented in section 2.4. This HTGB test[1] is run for 400 hours.

Devices are initially characterized (using a Agilent B1505 curve tracer) and placed in a forced-convection oven VENTICELL E09524 for 400 hours (dissipated power by the devices is negligible during the HTGB test, so no heatsink is necessary). They are characterized every 100 hours (and after the first 10 hours) after a cooling-down time of 1 hour. Characterizations

[1] There are some ambiguities between HTGB and HTRB tests (see annexe A.1). HTRB test is used to stress major power junctions and HTGB is used to stress gate oxide junctions. The test shown here, applies a stress in both; gate oxide and major power junctions. As the only criteria given by JEDEC standards [148] is that junctions must be stressed near their maximal voltage rating (>80%), it is chosen to classify this experiment as an HTGB test. Indeed, gate oxide junction is stressed at 80% of their maximal rating whereas the stress applied to the power junction is much lower. Although in most of the publications drain and source terminals are short-circuited for HTGB tests, this condition is not required by JEDEC procedures.

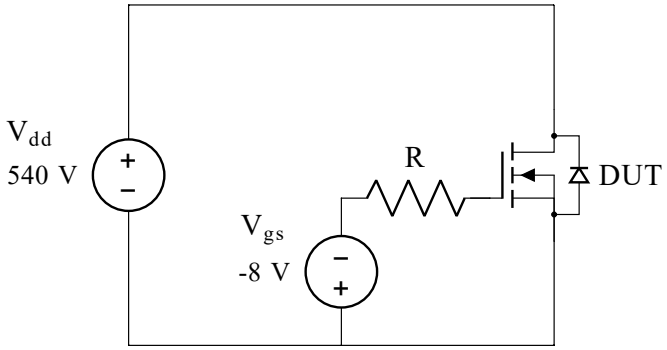


Figure 2.7 – HTGB JEDEC Test

are realized at room temperature, internal on-resistance R_{ds}, diode forward voltage V_f and threshold voltage V_{th} are measured.

Our results are compared to the results presented in the literature for similar tests. In section 2.4, they will be compared to the threshold voltage drift observed for the CMB test bench.

2.3.1.3 Static Tests with Current Biasing

The tests set-ups presented here are designed to provide reference points for the results presented in section 2.4. Even if the aim of this chapter is to study the internal diode robustness, some test are realized at positive gate bias (i.e. with current flowing through the channel of the MOSFET and not through the body-diode) in order to clarify if degradation phenomenons, especially on threshold voltage, are due to internal diode stress or not. The various test set-ups used are represented in fig. 2.8. Each test is performed on 3 samples. In all cases, the junction temperature is regulated to $T_j = 150$ °C using a hot plate and a thermal controller, according to the method described in section 2.3.1.1.

As it can be seen in fig. 2.8, there are four "quadrants" of operation in the plane (I_{gs}, V_{ds}). The third quadrant test is intended to stress the internal P-N junction, as in the case of a diode-less inverter. Nevertheless, in this case the current flow is continuous and no switching occurs. Defined test conditions are $V_{gs}= -8\ V$, $I_{sd} = 10$ A and $T_j = 150$ °C. Current level and gate-source voltage are chosen in accordance with test realized later on section 2.4. Due to the surprising results, showing an important voltage threshold drift, the same test is also run at $V_{gs} = -5\ V$ (see table 2.1).

The two other tests (first and fourth quadrant, fig. 2.8), stress the device forcing the current to circulate through the channel for comparison purposes. Circulating through the channel, the current will pass really near to the gate and it could be interesting to study if this affects the threshold voltage drift. For these tests, the conditions are $V_{gs} = 20\ V$, $I_{ch} = 16$ A and $T_j = 150$ °C. The current level is chosen in order to dissipate the same power than in the third quadrant test.

It is worth noting that the tests are realized at two different current levels: 10 A for the third quadrant test, while it is 16 A for the other two tests. These current choices allows to dissipate about the same power in all the cases. V_f is measured for a 10 A current after temperature stabilization (near the same value is measured for $V_{gs} = -8\ V$ and for $V_{gs} = -5\ V$). Power

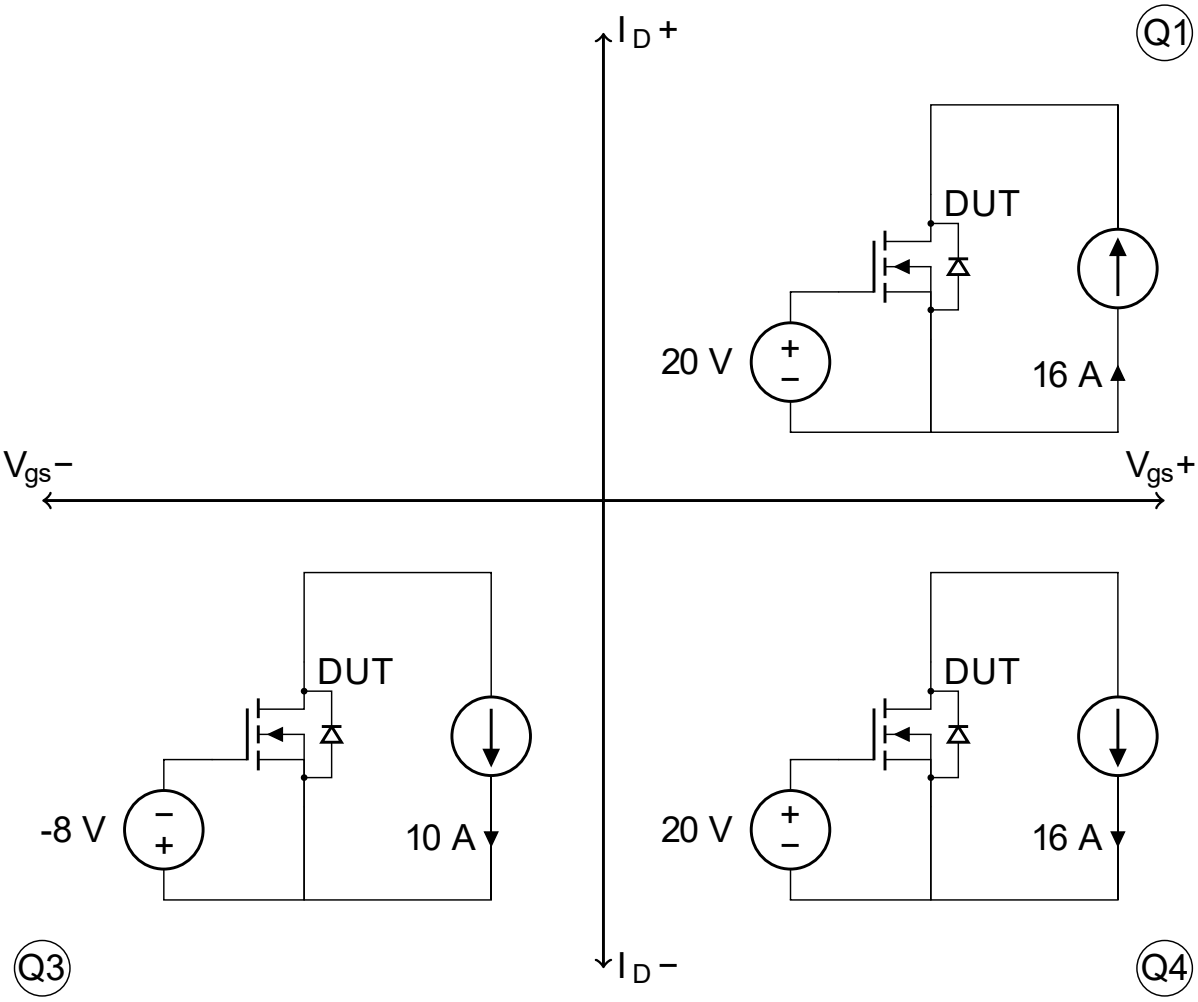


Figure 2.8 – Set of realized static tests

dissipation is calculated in agreement with eq. (2.4). To achieve the same power dissipation, a current of 15.93 A is determined for the other two cases using eq. (2.5) after device R_{ds} characterisation at 150 °C (see fig. 2.9). Finally, it is verified that dissipated power is the expected measuring drain-source voltage and current using two multimeters. As it was slightly lower, current has been adjusted to 16 A.

$$P_{d3} = V_f \cdot I_f = 3.73 \cdot 10 = 37.3 \qquad [W] \tag{2.4}$$

$$I_{ch} = \sqrt{\frac{P_{d1|4}}{R_{ds}}} = \frac{37.3}{0.147} = 15.93 \qquad [A] \tag{2.5}$$

The hot plate temperature is fixed in order to reach a junction temperature of 150 °C. According to equation. (2.1), the hot plate temperature is calculated as:

$$T_s = T_j - P_d \cdot R_{th_{js}} = 150 - 37.3 \cdot 2.19 = 68.3 \qquad [°C] \tag{2.6}$$

The devices are characterized initially and then regularly during the tests, after a cooling-

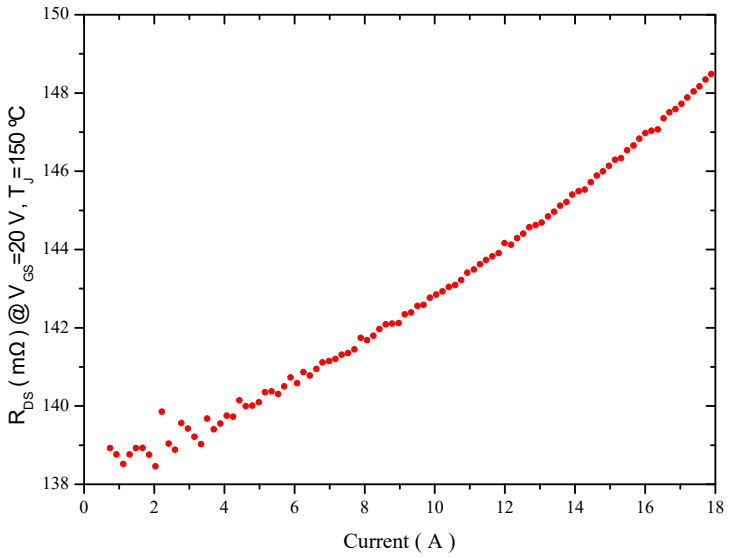


Figure 2.9 – R_{ds} characterization at 150 °C on a Wolfspeed C2M008012D MOSFET

Test	samples [a] (N)	V_{gs} (V)	I_{ds} (A)	V_{ds} (V)	T_j (°C)	Power (W)
HTGB	10	-8	0	540	150	0
1st quadrant	3	20	16	0	150	37.3
3rd quadrant	3	-8	-10	0	150	37.3
3rd quadrant	3	-5	-10	0	150	37.3
4th quadrant	3	20	-16	0	150	37.3

Table 2.1 – Summary of the static tests run on Wolfspeed C2M008012D MOSFETs.

[a] Devices were purchased in two batches: a first (Ref. W14514, year 2014) for HTGB test and a second (Ref. W10116 and W10216, year 2016) for Q1,Q3 and Q4 tests.

down time of 1 hour. At the beginning, characterizations are performed after a few stress hours. The following characterizations do not follow a fix stress period because it is preferable to realize device characterization just after the test is stopped as relaxation effects could take place. Characterizations are realized at 150 °C. Tests are run for 100 hours, but due to a failure on the curve tracer[2], the third quadrant test is stopped after 80 hours. The characterization includes internal on-resistance R_{ds}, diode forward voltage V_f and threshold voltage V_{th}.

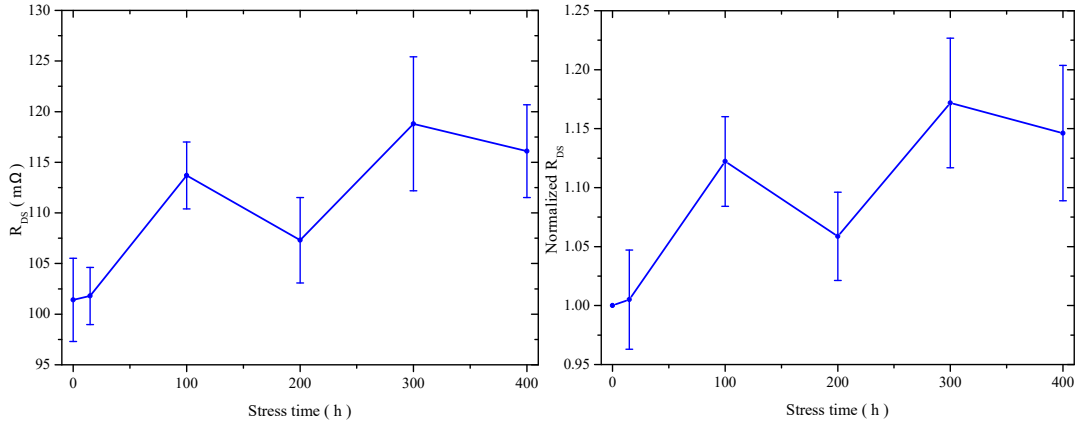
2.3.1.4 Static Tests Summary

To summarize, five different static tests are run. A HTGB test and four tests with current biasing. All these tests are summarized in table 2.1.

2.3.2 Experimental Results

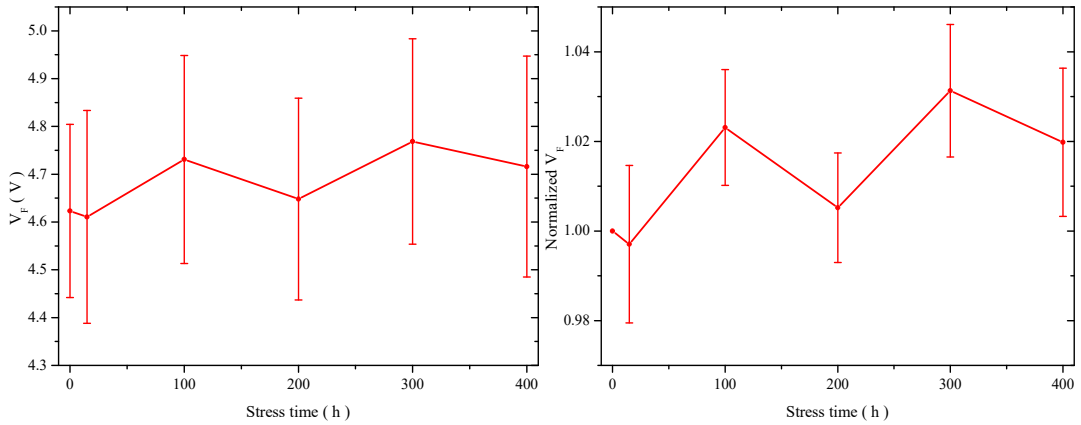
On the following pages, the experimental results obtained from the static tests are presented.

[2] Requiring the shipment of the curve tracer to Keysight for reparation.



(a) Rds-on resistance (b) Normalized Rds-on resistance

Figure 2.10 – Rds-on evolution for HTGB test. Characterised at room temperature, $I_{ds} = 10$ A and $V_{gs} = 20\ V$.



(a) Diode forward voltage (b) Normalized diode forward voltage

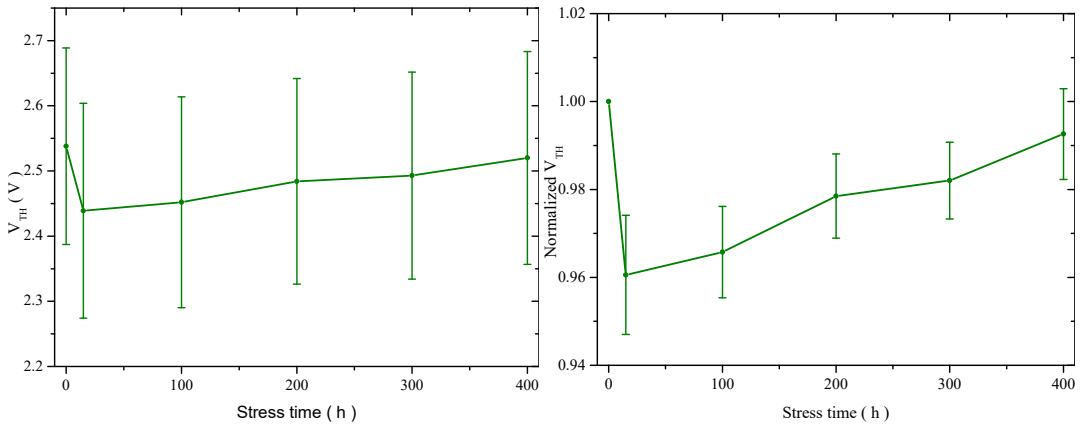
Figure 2.11 – Intrinsic diode forward voltage evolution for HTGB test. Characterised at room temperature, $I_f = 10$ A and $V_{gs} = -8\ V$.

2.3.2.1 HTGB Test

The HTGB test ($V_{dd} = 540\ V$, $V_{gs} = -8\ V$, $T_j = 150$ °C) shown in fig. 2.7 is performed on 10 devices. As mentioned earlier, characterized parameters are internal on-resistance R_{ds}, diode forward voltage V_f and threshold voltage V_{th}. The evolution of these parameters over 400 hours is given in figures 2.10 to 2.12. In all cases, the measured and normalized parameter values are represented. Normalized value is defined as the relation between the measured value at any given time (t_i) and its initial value (at t_0) (before starting the test):

$$Normalized\ parameter(t_i) = \frac{Measured\ parameter(t_i)}{Measured\ parameter(t_0)} \tag{2.7}$$

Fig. 2.10 shows the evolution of the internal on-resistance over the test at $V_{gs} = 20\ V$ and $I_{ds} = 10$ A. This shows an upward trend of the resistance, increasing by around 15% (≈15 $m\Omega$) after 400 hours. However, it is unclear if this evolution should be attributed to the SiC die or to its packaging. In our test setup, a 4-wire connexion is used on most of the cabling, but



(a) Threshold voltage (b) Normalized threshold voltage

Figure 2.12 – Threshold voltage evolution for HTGB test. Characterised at room temperature, $I_{ds} = 100\ \mu A$ and $V_{ds} = 1\ V$.

the actual connexion to the DUT leads is 2-wires only (see A.2). Therefore, effects such us oxidation of the leads could cause such R_{ds} change. Other effects such as the degradation of the die metallization cannot be ruled out either.

The evolution of the diode forward voltage V_f over the HTGB test stress is depicted in fig. 2.11. Characterization is realized at $V_{gs} = -8$ and $I_{sd} = 10$ A. As it can be seen in fig. 2.11b, V_f remains near to stable under the HTGB stress. The voltage forward increases by about 2% on average.

The increase of these two parameters, R_{ds} and V_f, could be related. Regarding fig. 2.11a, we can see that the forward voltage increase is about 0.1 V. It can be also seen from fig. 2.10a that the internal on-resistance increases by about 0.015 Ω. If we consider that this change in R_{ds} is due to an increase of the drift region resistance, or of any resistance which belongs to both the I_{CH} and I_{BD} paths (fig. 2.3), this could represent an increase of about 0.15 V on the V_f ($I_{sd} = 10\ A$). The measured forward voltage increase is slightly lower (about 0.1 V), but both values are comparable when measurement error is considered. This increase in the internal-on resistance is not due to a variation in the threshold voltage. Both parameters are related in agreement with eq. (2.8), where b is a constant related to the material. However, taking in account the initial measured values from fig. 2.10a and 2.12a (R_{ds}=102 $m\Omega$, V_{th}= 2.54 V) and a V_{gs}=20 V, the sensibility of R_{ds} versus a variation in the threshold voltage would be around 6.2 $m\Omega{\cdot}V^{-1}$ in agreement with eq. (2.9) and (2.10). Thus, the observed increase in the R_{ds} (around 15 $m\Omega$) should require an increase greater than 2 V in the V_{th}, which is not the case.

$$R_{ds} = \frac{b}{(V_{gs} - V_{th})} \tag{2.8}$$

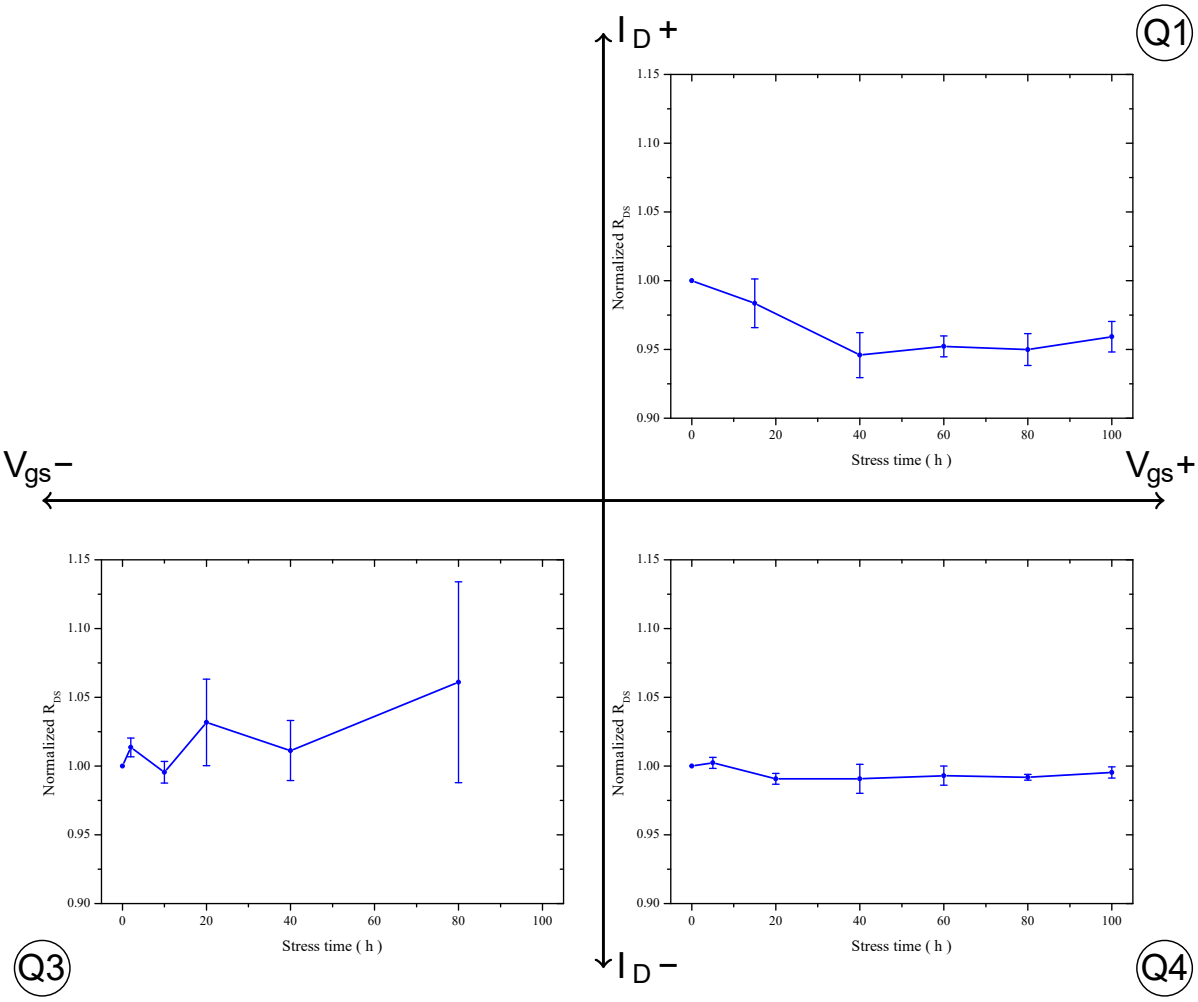


Figure 2.13 – R_{ds} evolution (3 samples). Test conditions (table 2.1): 1Q and 4Q ($I_{CH} = 16\ A,\ V_{gs} = 20\ V$); 3Q ($I_{BD} = 10\ A,\ V_{gs} = -8\ V$). Characterised at 150 °C, $I_{ds} = 10$ A and $V_{gs} = 20\ V$.

$$R_{ds} + \Delta R_{ds} = \frac{b}{(V_{gs} - V_{th} - \Delta V_{th})} \tag{2.9}$$

$$\frac{\Delta R_{ds}}{\Delta V_{th}} = \frac{(20 - 2.54) \cdot 102}{(20 - 2.54 - \Delta V_{th})} - 102 \Big|_{\Delta V_{th}=1V} = 6.2 \qquad \left[m\Omega \cdot V^{-1}\right] \tag{2.10}$$

The evolution of the threshold voltage can be seen in fig. 2.12. V_{th} is measured for $V_{ds} = 1\ V$ and $I_{ds} = 100\ \mu A$. A drop in the threshold voltage is observed after the first 10 hours of operation, followed by a slow recovery to the initial value. However, the initial V_{th} drop is small (< 5 %). These results are reassuring, as previous articles [123, 145] reported much larger V_{th} drifts. Nevertheless, devices used in these publications could be of older generations than those considered here. Particularly, in [123], the V_{th} drift is larger than 20 % of the initial value for an HTGB test performed at $V_{gs} = -5\ V$. In the case where $V_{gs} = 20\ V$, the V_{th} drops dramatically according to [145]. It is also worth noting that, contrary to our configuration, in

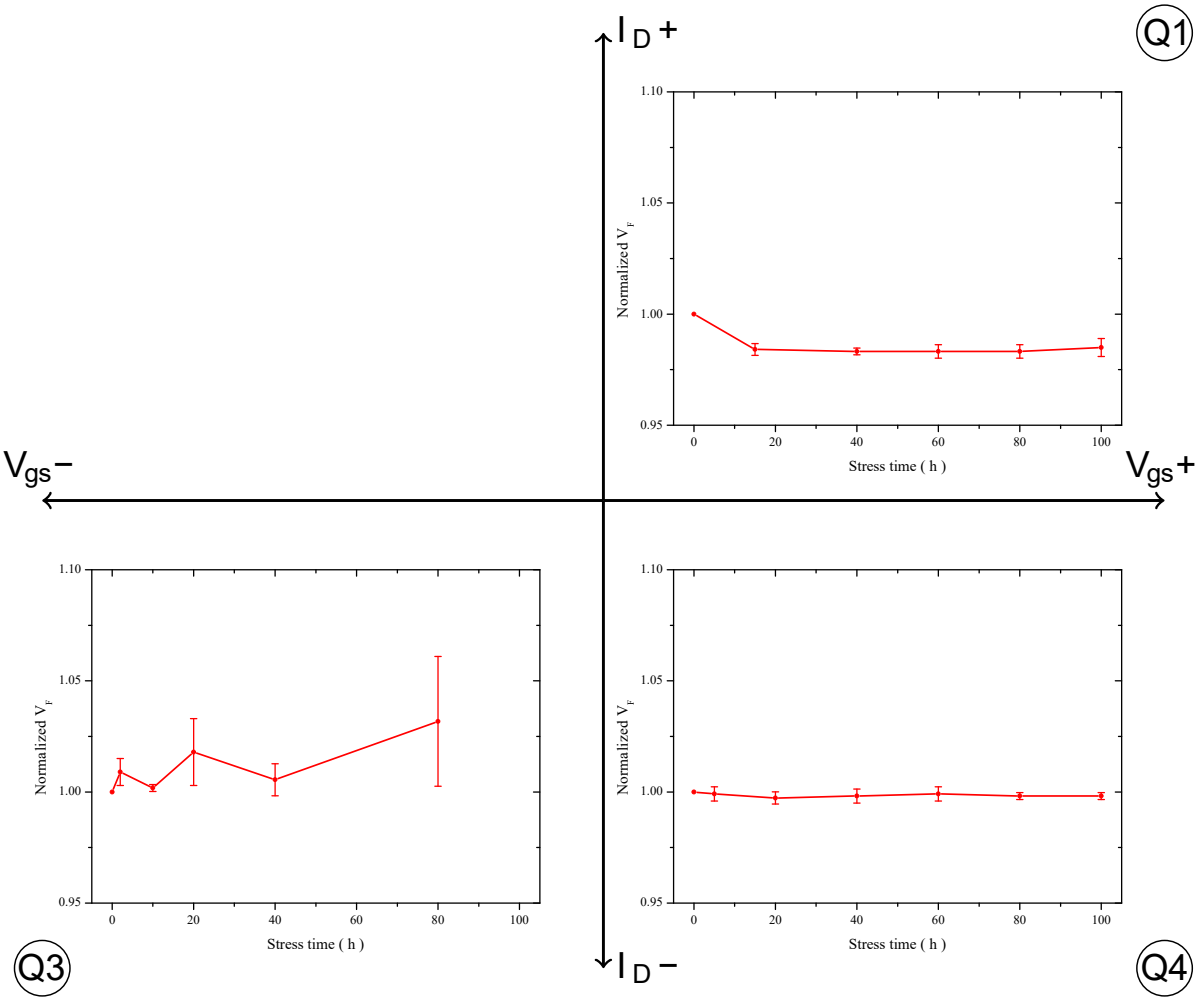


Figure 2.14 – V_f evolution (3 samples). Test conditions (table 2.1): 1Q and 4Q ($I_{CH} = 16\ A,\ V_{gs} = 20\ V$); 3Q ($I_{BD} = 10\ A,\ V_{gs} = -8\ V$). Characterised at 150 °C, $I_f = 10$ A and $V_{gs} = -8\ V$.

these experiments the drain and source terminals of the DUT are connected together during the HTGB test (V_{ds}= 0) and it might have an effect on the threshold voltage drift.

2.3.2.2 Static Tests with Current Biasing

In this section the results from the different tests with current biasing (see section 2.3.1.3) are presented. Fig. 2.13, 2.14 and 2.15 show the evolution of parameters R_{ds}, V_f and V_{th} respectively over the tests. All parameters are measured at 150 °C and at the same point of operation than in section 2.3.2.1; this is $\{V_{gs} = 20\ V,\ I_{ds} = 10$ A$\}$ for R_{ds}, $\{V_{gs} = -8\ V$and $I_{sd} = 10$ A$\}$ for V_f, and $\{V_{ds} = 1\ V,\ I_{ds} = 100\ \mu A\}$ for V_{th}.

Regarding the evolution of R_{ds} (fig. 2.13), no large variation is observed when the current circulates through the channel (first and fourth quadrant of operation). One can only notice a small initial decrease by about 3% of R_{ds} in the first quadrant. What was expected, if anything, was an increase in R_{ds} because the applied gate-source bias in the first quadrant is positive ($V_{gs} = 20\ V$), which could result in a positive shift in the threshold voltage, which should

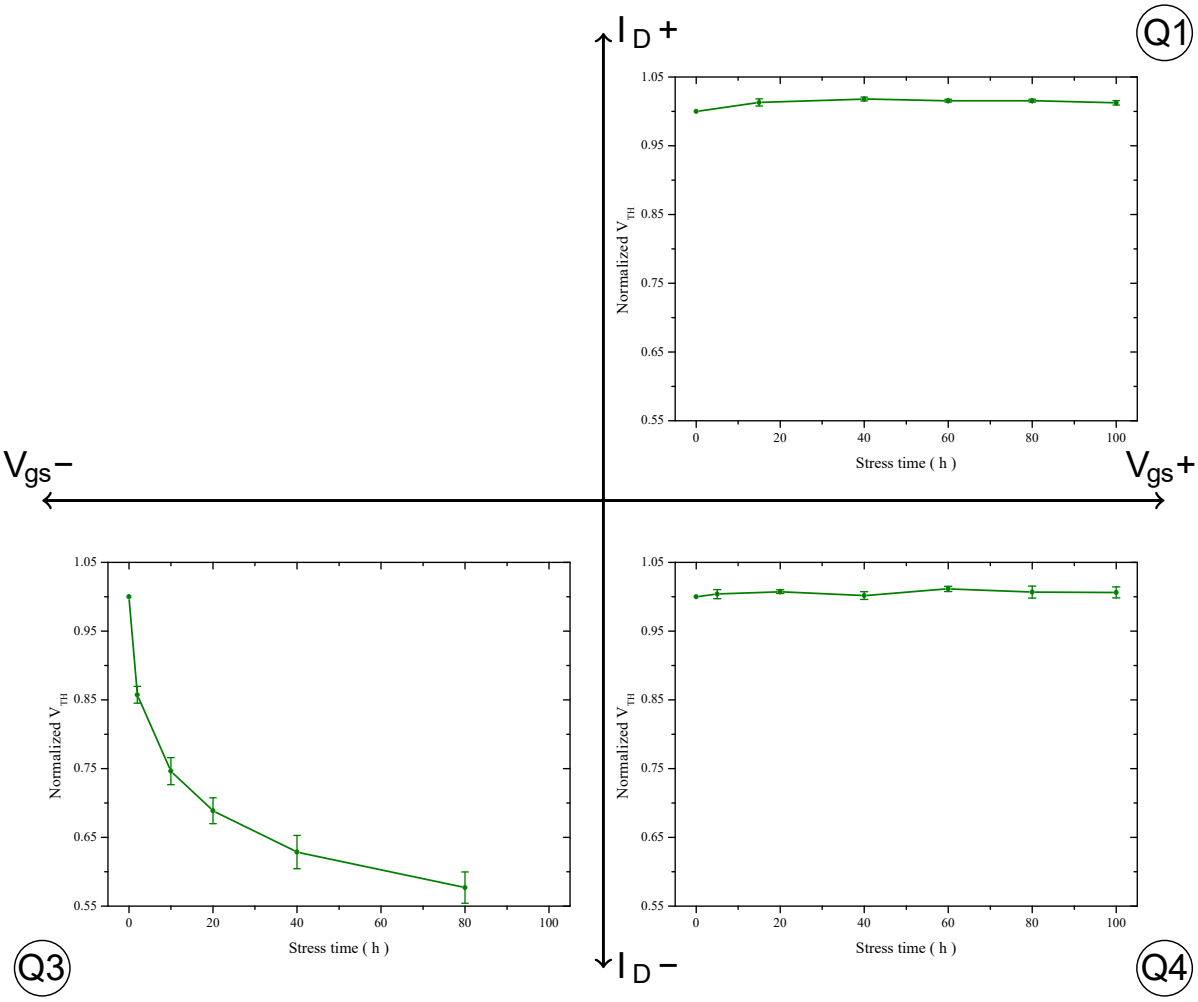


Figure 2.15 – V_{th} evolution (3 samples). Test conditions (table 2.1): 1Q and 4Q ($I_{CH} = 16\ A,\ V_{gs} = 20\ V$); 3Q ($I_{BD} = 10\ A,\ V_{gs} = -8\ V$). Characterised at 150 °C, $I_{ds} = 100\ \mu A$ and $V_{ds} = 1\ V$.

provoke an increase in the on-resistance. For the fourth quadrant, R_{ds} variation over 100 hours is lower than 1%.

Working at the third quadrant, one of the devices shows a relatively large increase in R_{ds} (almost 15%). However, this is not observed on all devices, with one even exhibiting a 1% decrease over the test duration (hence the large error bars in fig. 2.13 for Q3). Because of this experimental scattering, no obvious explanation can be proposed for this little change in R_{ds}.

The behaviour of the diode forward voltage is shown in fig. 2.14. For the first and fourth quadrants, it is shown that this parameter remains almost stable and only some slight variations are observed (especially for the 1st quadrant, at the beginning of the tests). On the third quadrant of operation, as for R_{ds}, a significant increase after 80 hours is observed on some samples. This differs for each sample and it is comprised between 0.25 and 6.1 %. In all cases, results are coherent with the evolution of the internal on-resistance observed in fig. 2.13. Besides, results allows to confirm that the presence of SFs has been drastically reduced (there is any important increase of V_f), as indicated by the manufacturers [54].

The evolution of the threshold voltage shows the most interesting behaviour. For the first

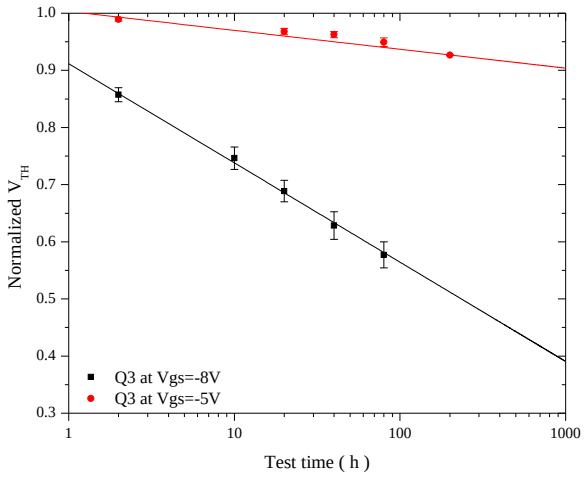


Figure 2.16 – V_{th} evolution and extrapolation for 3 samples operating in the 3Q:($I_{BD} = 10\ A$) for $V_{gs} = -5$ and $V_{gs} = -8\ V$. Characterised at 150 °C, $I_{ds} = 100\ \mu A$ and $V_{ds} = 1\ V$.

and the fourth quadrants of operation, it remains almost stable and V_{th} increase remains lower than 2 % after 100 hours in both cases. However, for the third quadrant of operation, it shows an abnormal behaviour with a dramatic drop down to 58 % of its initial value after a 80 hours stress. This behaviour is common to all three samples, with final threshold voltage values comprised between 0.55 and 0.6 of their initial value.

To further analyse the extend of the issue, an additional test is run in the third quadrant of operation, but this time applying a lower gate-source voltage ($V_{gs} = -5\ V$) for 200 hours. In this case the threshold voltage drift is much lower than for $V_{gs} = -8\ V$ and V_{th} remains close to 92% of its initial value after 200 hours.

To better understand the evolution of the threshold voltage in the third quadrant of operation, these data (at $V_{gs} = -5$ and $V_{gs} = -8\ V$) are plotted using a semi-logarithmic scale in fig. 2.16. The least square method is used to extrapolate its behaviour to 1000 hours of operation. At this point, the threshold voltage would only be of 38.5 % of its initial value for the case where $V_{gs} = -8\ V$. Nevertheless, in the case where $V_{gs} = -5\ V$, the V_{th} is expected to remain near the 90 % of its initial value after 1000 hours.

2.3.3 Discussion

Some conclusions can be deduced from the presented static tests. These tests are a HTGB test, where the dissipated power is negligible, and three different tests in which the MOSFETs are operating in different quadrants. In all these three later cases, the same power is dissipated. This allows to eliminate temperature uncertainties and to obtain comparable results. Nevertheless, with this approach, the current density is not the same in all three tests, which might have an effect.

From HTGB test, an increase in the internal on-resistance (about 15 $m\Omega$) and a slight increase in the diode forward voltage (about 0.1 V) has been observed. As both changes are comparable when considering a current of 10 A, it would be possible that they would be due to an increase in resistance of the regions which are common to both current path (i.e. the drift

region, the metalization in the packaging). However, these hypotheses have not been confirmed by the other static test (Q1,Q3,Q4). These tests, contrary to HTGB, do not show any consistent internal on-resistance increase. The most probable reason for this different behaviour is that although all devices under test are Wolfspeed SiC MOSFETs C2M008012D [152], they were purchased separately and those used for the HTGB test [149] are older[3]. More recently devices had probably been improved. We consider that the test realized at the third quadrant of operation has to be almost as demanding as the HTGB test, as in both cases $T_j = 150$ °C and $V_{gs} = -8$ V, but besides it incorporates a current flow which stresses the drift region but not the channel.

Tests realized in the first and fourth quadrant of operation do not show any remarkable phenomenon, and in all cases R_{ds}, V_f and V_{th} remain essentially stable. However, when devices operate in the third quadrant, a significant increase in the internal on-resistance is reported in some cases as well as an important decrease of the V_{th}.

For one of the samples, the R_{ds} increase reaches close to 14 % of the initial value (about 150 $m\Omega$ at 150 °C for $V_{gs} = 20$ V and $I_{ds} = 10$ A). This increase is comparable with that reported in the diode forward voltage, which in one sample reaches 6 % (the typical V_f value is about 3.7 V at 150 °C for $V_{gs} = -8$ V and $I_{ds} = 10$ A). A sensibility calculus of $\Delta R_{ds}(\Delta V_{th})$ (see eq. (2.8) to (2.10)) reported that it should be necessary a change of about 1 V in the V_{th} to obtain a variation about 6 $m\Omega$. As obtained results are inconsistent with this order of magnitude, it is not possible to associate the change in the R_{ds} to that of the V_{th}, and consequently to a variation of the channel resistance.

From the V_f and V_{th} behaviour, two main conclusions can be drawn from the devices tested in the third quadrant of operation:

Stacking Fault (SF) defects have been drastically reduced. As introduced in section 2.2, it has been reported that the use of the internal diode can cause the apparition of basal plane dislocation which could result in stacking faults (SF) defects [153, 154]. Thus, as the diode voltage forward increase after stress is not significant (<6 %) compared with results reported on the literature (see fig. 2.2 [145]), it can be concluded that crystal quality has been improved, significantly reducing SF.

An unexpected and dramatic threshold voltage drop occurs. It shows a decreasing exponential behaviour, reaching between 55 and 60 % of the initial value after a stress of 80 hours in all cases. Extrapolating this behaviour to 1000 hours, it is found that the threshold voltage would drop to 38.5 % of its initial value, as shown in fig. 2.16. This would make the device less robust to electromagnetic perturbations. Thus, the probability of a short-circuit event or failure would increase. Even, in an extreme case, the device could become normally-on.

As shown, to minimize this drop in the threshold voltage, it is possible to apply a different V_{gs} (-5 V instead of -8 V). Again, this results in lower EMC immunity, requiring a very good setup of the converter to avoid spurious turn-on.

As the threshold voltage has drastically decreased only for the Q3 test, some differences between the different tests must be considered. For Q1 and Q4 test, the device is under conditions of high inversion. In these conditions, with a positive electric field applied between

[3] Wolfspeed has been found to modify its devices without reflecting the changes in the part reference number, which remained identical.

gate-source terminals it could be possible to inject electrons into the interface SiC/SiO2 near the channel zone, provoking an increase of the V_{th} which in these tests has not been observed. However, for the Q3 and HTGB tests, devices are operating under accumulation regime. Thus, in this case, the carriers are holes which could be injected into the interface SiC/SiO2. Contrary to the precedent case, this would result in a decrease of the V_{th}.

Focusing in the differences between HTGB and Q3 cases, at least one seems evident. For the HTGB test, as dissipated power is negligible, it is possible to assume that temperatures of the different regions of the device are very similar. However, in the case of Q3, a considerable amount of power is dissipated in the device. This could result in an important temperature gradient between the drift region and the top level of the device (near the oxide, see fig. 2.3), favouring carrier (holes) injection and the V_{th} drift.

2.4 Testing SiC MOSFET internal-diode for an inductive switching application

In the last section, several static tests have been presented. These tests were realized under continuous operation at the maximal junction temperature allowed by the manufacturer. The objective was to show the main weakness of the MOSFET internal-diode. However, stress conditions would be very different in a real case, with two main differences:

- Non-continuous diode stress.
- Inductive switching.

To realize the tests under these two conditions, a new test-bench is designed. In this way, a converter with an inductive load is described in section 2.4.1. Stress duration is determined by the state of the other switches, but this time, the stress is discontinuous, with pulses at 20 kHz. The aim of this experiment is to study the drift in threshold voltage for SiC MOSFETs reported in 2.3. Moreover, it is studied if inductive switching condition causes any degradation of the P-N junction or if it has additional effects on the threshold voltage drift.

Tested devices are Wolfspeed C2M008012D SiC MOSFETs, 1200 V, 80 $m\Omega$, in a TO-247 package. The devices were purchased in two batches: a first (Ref. W14514, year 2014) for CMB1 tests and a second (Ref. W10216, year 2016) for CMB2 tests. It is worth noting that fresh devices are used for each test. Devices are attached to a temperature-regulated hot plate to operate near their maximum junction temperature of 150 °C [149].

Different experimental protocols are presented in 2.4.1.1 and 2.4.1.2, whereas tests results are presented in section 2.4.2. All the data of the different tests are summarized in annexe A.6.

2.4.1 Test-bench description

Devices under test (DUT) are required to conduct in reverse mode (internal-diode stress) and under inductive switching conditions. Thus, the designed test-bench is based on a back-to-back structure, which is composed by a buck converter followed by a boost converter (see fig. 2.17). In this memory, this test-bench will be referred to as "Chopper Mode Bias" (CMB). As two versions of the test-bench are developed, we will use CMB1 to refer to the first one and CMB2 for the second version.

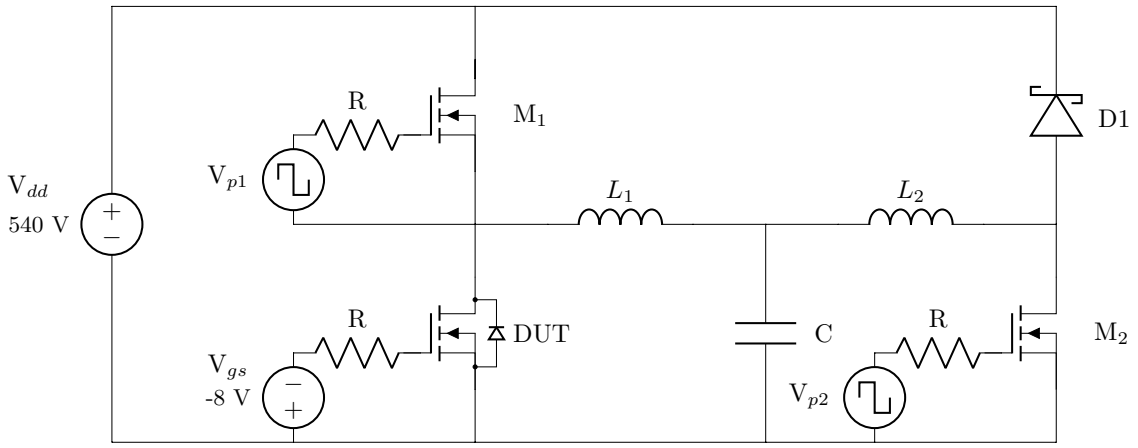


Figure 2.17 – Schematic of the back to back test-bench (CMB).

The current in the boost converter inductor (L_2) is regulated to 10 A by the duty cycle of M_2. This imposes the same current to the buck inductor (L_1), and therefore to the DUT when it is involved. Both inductors L_1 and L_2 have a value of 80 mH. This high inductance value will assure a low current ripple for the chosen frequency (f=20 kHz), but also guarantees highly inductive commutations. Moreover, a capacitor of 27 μF is placed between these two inductors to minimize perturbations and to simplify the control of the system.

To illustrate the amplitude of the current ripple, we can consider a duty cycle (D) of M_1. During the time when this switch is conducting (50% of the period), the inductor current increases. Considering that capacitance voltage (V_c) is stable at 50% of the input voltage (540 V), current will increase by 0.084 A in agreement with (2.11). When the state of the switches changes, the current decreases by the same value. Thus, the current ripple is small enough to be neglected.

$$\Delta I_{pp} \simeq \frac{V_{dd} - V_c}{L} \cdot \frac{D}{f} = \frac{540 - 270}{80 \cdot 10^{-3}} \cdot \frac{0.5}{20 \cdot 10^3} = 0.084\ A \tag{2.11}$$

Fig. 2.18 shows a simplified circuit diagram of the CMB test-bench, where the boost converter is modelled as a 10 A continuous current source (I_{sw}). The chosen input voltage is $V_{dd} = 540\ V$ because this is the voltage chosen for the more electric aircraft high voltage DC bus (HVDC) [17, 18]. Thus, it allows to test the device in the same conditions of operation as in a real avionic application.

Using the same test-bench, two different tests are realized. These are presented in sections 2.4.1.1 and 2.4.1.2. For the first one, the channel of the DUT remains always blocked and the current only flows through the internal diode. For the second test, the DUT is periodically turned-on and the current also flows through the channel, depending of the applied duty cycle. The objective is to determine if the duty cycle has any impact on the threshold voltage drift.

2.4.1.1 CMB Test -Channel always blocked-

The aim of this test is to assess an eventual degradation of the P-N junction, as well as a threshold voltage drift. The gate voltage is fixed at a constant negative voltage, forcing the MOSFET in the off-state and the current to flow through the intrinsic diode. As the converter

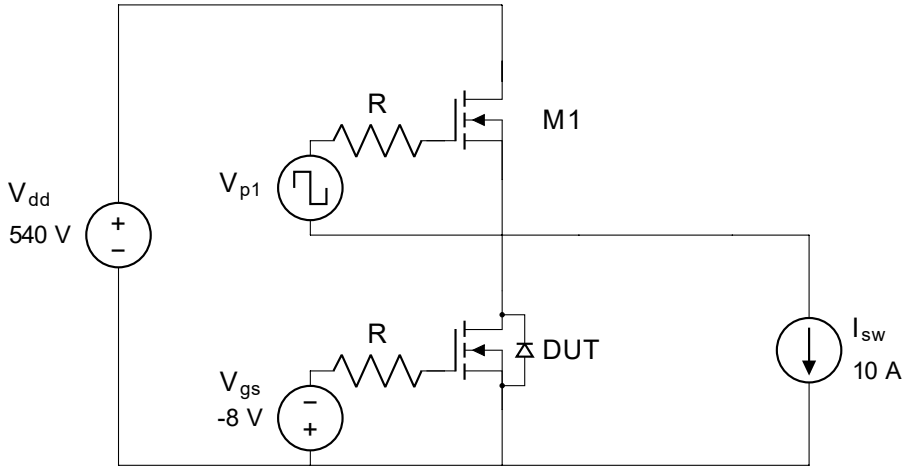


Figure 2.18 – Simplified CMB schematic, modelling the boost converter as a continuous current source.

is working in continuous conduction mode, there are different circuit configurations depending on the state of switches (M_1 and DUT). These are detailed below together with the junction temperature estimation.

Some first measurements are performed at $V_{gs} = -5\ V$ and show important perturbations on the gate-source voltage. Thus, gate-source DUT voltage is fixed to $V_{gs} = -8\ V$ to ensure that EMC perturbations are not capable to cause a short-circuit event. It is worth noting that the datasheets [149, 152] mention an absolute minimal $V_{gs} = -10\ V$. However, the latest datasheet version [152] recommends a $V_{gs} = -5\ V$ for applications involving the internal diode. Nevertheless, this is not mandatory and the absolute minimal V_{gs} level remains -10 V.

A complete characterization of the devices under test at room temperature is realized every 20 hours after a cooling-down time of 1 hour. Devices are also characterized after the first 10 hours. Total test duration is 100 hours. As a threshold voltage drift is observed, the test has been prolonged up to 400 hours for four components.

Moreover, to study deeply this drift of the threshold voltage, the test is run on SiC MOSFETs from two additional manufacturers, with the same voltage and similar current range. Chosen devices are SCT2080KE from ROHM[4] [155] and SCT30N120 from ST[5] [156]. In both cases, the test is run on three samples. It is noticeable that ROHM MOSFET is blocked at $V_{gs} = -5\ V$, as its datasheet limits the minimal V_{gs} to -6 V [155]. For the ST MOSFET, test is run at $V_{gs} = -8\ V$, as for the Wolfspeed devices (it is limited at -10 V [156]).

Finally, a second test-bench (CMB2) has been developed to minimize gate-source voltage perturbations. It is based on the same circuit structure, but parasitic inductances and capacitances on the power and driver PCBs have been minimized. This better EMC design, allowed to reduce significantly the perturbations, especially on the gate-source voltage. Using this test-bench, two additional test runs are performed. The first one at $V_{gs} = -8\ V$ and the second one at $V_{gs} = -5\ V$. In both cases, the test are run on three samples. Unfortunately, in spite of the perturbation reduction, in the case where $V_{gs} = -5\ V$, two samples have fail during the test. Anyway these first characterization points indicate a trend. All details about both CMB test-benches are presented in annexe A.5.

[4]ROHM refers to ROHM Semiconductor
[5]ST refers to STMicroelectronics

Junction temperature and losses estimation

Device	D_{DUT}	Channel losses (W)	Intrinsic diode losses (W)	Total losses (W)	Hot plate temperature (°C)
SCT30N120[a]	0 %	0	16.25	16.25	114
SCT2080KE[b]	0 %	0	28.15	28.15	90
C2M008012D[c]	0 %	0	19.2	19.2	108

Table 2.2 – Losses and hot plate temperature for every device tested.

[a] $V_f = 3.25\ V$ ($T_j = 150$ °C,$I_{sd} = 10$ A, $V_{gs} = -8\ V$), $R_{jc} = 0.65°C/W$
[b] $V_f = 5.63\ V$ ($T_j = 150$ °C,$I_{sd} = 10$ A, $V_{gs} = -5\ V$), $R_{jc} = 0.57°C/W$
[c] $V_f = 3.84\ V$ ($T_j = 150$ °C,$I_{sd} = 10$ A, $V_{gs} = -8\ V$), $R_{jc} = 0.65°C/W$

As said, the test is done at $T_j = 150$ °C. To achieve this junction temperature it is necessary to estimate the losses to regulate the hot plate temperature.

The switching losses of the DUT could be neglected if the MOSFET channel always remains blocked, as these are not important for the internal diode of a SiC MOSFET [157] (f=20 kHz). The forward voltage drop of the diode at the CMB operating point ($T_j = 150$ °C, $V_{gs} = -8\ V$, I_f=10 A) was measured as V_f=3.84 V for Wolfspeed MOSFETs. As the current has a low ripple, the diode current is assumed to have a square waveform. Then, the power dissipated by the DUT can be calculated using equation (2.12). Finally, using equation (2.1) and the values calculated above ($R_{js} = 2.19\ °C/W$), one can estimate that a junction temperature $T_j = 150$ °C is achieved for a heat-sink temperature T_S=108 °C (eq. (2.13)).

When $V_{gs} = -5\ V$ is applied to the DUT, the forward voltage is the same as when $V_{gs} = -8\ V$. Thus, for both tests realized on the CMB2 test-bench, heat-sink temperature is also 108 °C.

$$P_D = V_f \cdot I_f \cdot D = \frac{3.84\ V \cdot 10\ A}{2} = 19.2\ W \tag{2.12}$$

$$T_S = T_j - P_d \cdot R_{js} = 150 - 19.2 \cdot 2.19 = 108°C \tag{2.13}$$

For the case where the test is run on MOSFETs from ROHM or ST, heat-sink temperature is calculated in the same way and in agreement with its characterized V_f and its thermal resistance [155, 156]. Losses and hot-plate temperature for each device tested are summarized in table 2.2. In all cases, heat-sink temperature is determined to achieve a junction temperature of 150 °C.

2.4.1.2 CMB Test -Channel sometimes conducting-

In the section above, the MOSFET is always in the blocking state, using only the intrinsic diode. This is not representative of most application cases, where the diode is used during the dead-time, before the MOSFET channel is turned on. Another test is therefore proposed to study if there is an impact of the diode duty cycle on the DUT degradation, particularly on the

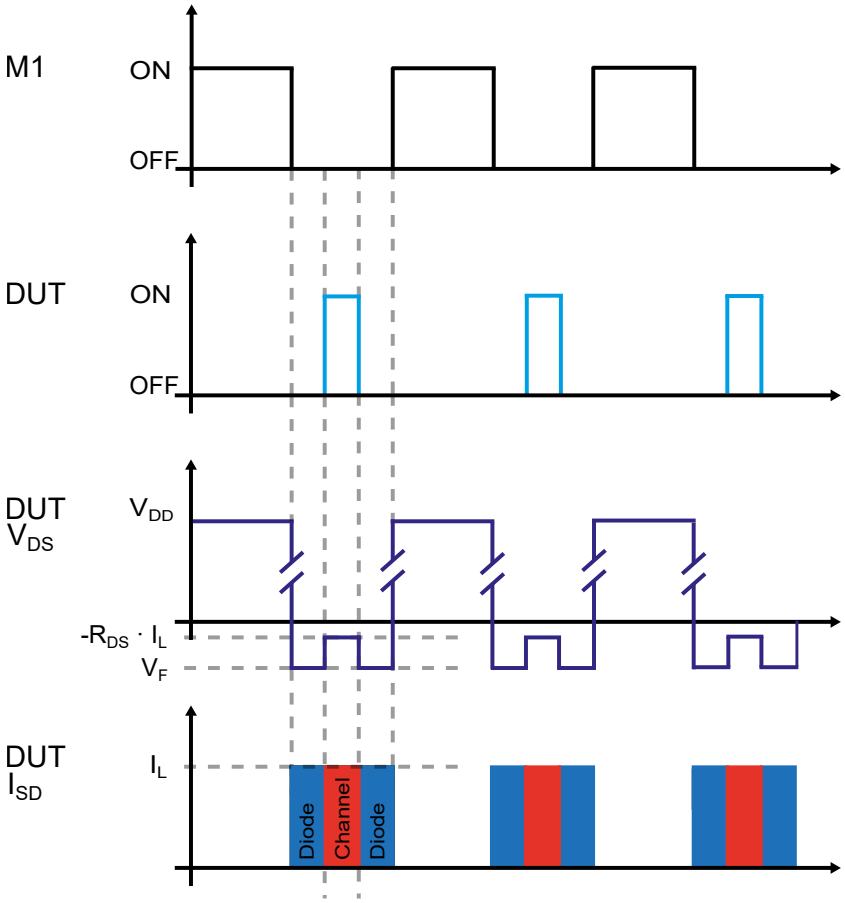


Figure 2.19 – Qualitative waveforms of current and voltage for the DUT, as well as the logic states for switches M_1 and DUT. Body diode current is plotted in blue. When it flows through the channel, it is plotted in red.

threshold voltage. It is noticeable that all these tests are run on the first designed test-bench (CMB1).

To submit the internal diode to the same stress as in the test presented in section 2.4.1.1 (internal diode stressed during 50% of the period), the duty cycle of M1 (see fig. 2.18) is varied. This, in combination with the signal control applied to the DUT gate ($V_{gs} = +20/-8\ V$), allows to modulate the channel and the P-N junction conduction time depending on the chosen duty cycles. Figure 2.19 illustrates the current and voltage waveforms of the DUT depending of the switches states.

Table 2.3 shows the duty cycle for devices M1 and DUT. The DUT conduction time is divided between intrinsic diode and channel conduction durations and expressed as a percentage. Obviously, there is one case where is not possible to have the current flowing though the intrinsic diode for 50% of the switching period (when D=85 %). In this case the internal diode is only solicited during the dead-time, which represents a 1.6% of the period.

This test is only run on one Wolfspeed sample for each case, as the objective is just to observe if there is any impact of the duty cycle on the threshold voltage. A further study on more samples should be required to properly quantify this impact.

Junction temperature and losses estimation

D_{M1}	D_{DUT}	Conduction time of DUT intrinsic diode	Conduction time of DUT channel
50 %	0 %	50 %	0 %
45 %	5 %	50 %	5 %
35 %	15 %	50 %	15 %
13.4 %	85 %	1.6 %	85 %

Table 2.3 – Configurations used for the CMB test with partial channel conduction.

The junction temperature is calculated in the same way as in section 2.4.1.2. As the channel is turned-on when the current is flowing through the internal P-N junction, switching losses can be also neglected (Zero Voltage Switching "ZVS" conditions, f=20 kHz). However, losses differs depending on the channel time conduction. Thus, it is necessary to estimate this for all cases in order to determine the required hot plate temperature.

Device	D_{DUT}	Channel losses (W)	Intrinsic diode losses (W)	Total losses (W)	Hot plate temperature (°C)
C2M008012D[a]	5 %	0.72	19.2	19.92	106
C2M008012D	15 %	2.15	19.2	21.35	103
C2M008012D	85 %	10.73	0.61	11.34	125

Table 2.4 – Losses and hot plate temperature for every duration of the DUT duty cycle.

[a] R_{ds}=0.143 Ω (T_j = 150 °C,V_{gs} = 20 V,I_{ds} = 10 A see fig. 2.9)

In this sense, eq. (2.14) and eq. (2.15) refer respectively to the channel and body diode losses depending on the applied duty cycle.

$$P_{ch}(D) = R_{ds} \cdot I_{sd}^2 \cdot D \tag{2.14}$$

$$P_{bd}(D) = V_f \cdot I_{sd} \cdot (1 - D_{M1} - D_{DUT}) \tag{2.15}$$

Adding body-diode and channel losses, we obtain the total losses :

$$P_d(D) = P_{ch}(D) + P_{bd}(D) \tag{2.16}$$

To achieve a junction temperature T_j = 150 °C, the hot plate temperature can be calculated for each duty cycle using equation (2.1) ($R_{cs} = 1.54\ °C/W$).

Table 2.4 summarizes the required hot plate temperature and the calculated losses for each DUT duty cycle. For conduction times, refers to table 2.3.

2.4.1.3 CMB Test Summary

The objective of this section is to stress the devices under more realistic conditions than in section 2.3. The internal P-N junction of the DUTs is stressed under inductive switching

conditions. Depending of the duty cycle applied to the complementary switch of the DUT, the duration of the stress pulse can be defined.

In the first case (section 2.4.1.1), the DUT remains always blocked and the current flows 50% of the period through the internal diode ($D_{M1} = 0.5$). This test is run on Wolfspeed ROHM and ST MOSFETs, comparing the results. A second version of the test-bench (CMB2) has been developed to minimize EMC perturbations. However, only Wolfspeed MOSFETs are tested in CMB2 testbench.

In the second case (section 2.4.1.2), DUT is turned-on during part of the period, so the current also flows through the channel.

The objective of this second test is to study if there is an impact of the duty cycle, especially on the V_{th} drift observed in section 2.3. Thus, three different duty cycle values are applied (D_{DUT}=5%, 15% and 85%).

Table 2.5 summarizes the tests realized, detailing DUT losses, hot plate temperature, the number of samples and the used test-bench. Results are presented in the following section.

Device	D_{DUT}	Total losses (W)	Hot plate temperature (°C)	Number of samples	Test
SCT30N120[a]	0 %	16.25	114	3	CMB1
SCT2080KE[b]	0 %	28.15	90	3	CMB1
C2M008012D[c]	0 %	19.2	108	10	CMB1
C2M008012D[d]	0 %	19.2	108	6	CMB2
C2M008012D[c]	5 %	19.92	106	1	CMB1
C2M008012D[c]	15 %	21.35	103	1	CMB1
C2M008012D[c]	85 %	11.34	125	1	CMB1

Table 2.5 – Summary of body diode stress tests under inductive switching conditions.

[a] Ref. CHN-GK-552, year 2015.
[b] Ref. 15-04, year 2015.
[c] Ref. W14514, year 2014.
[d] Ref. W10216, year 2016

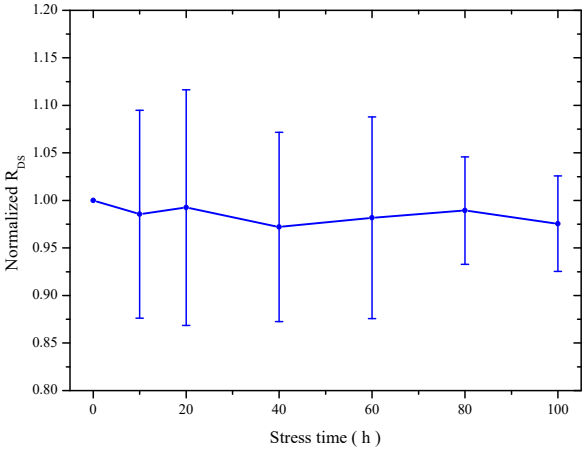
2.4.2 Experimental Results

2.4.2.1 CMB Test Results -Channel always blocked-

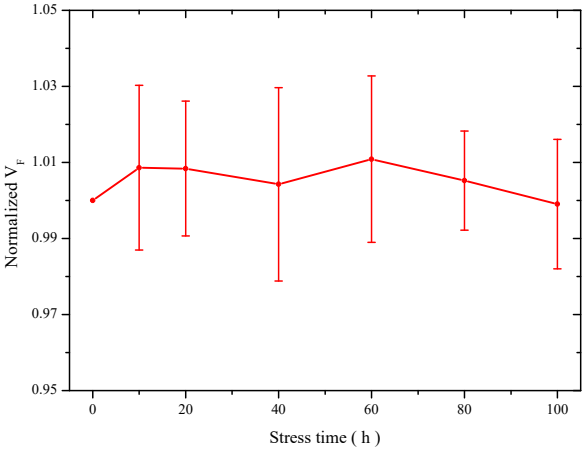
CMB test is performed on 10 devices on CMB1 test-bench. Unfortunately, for one of these devices an important threshold voltage drop ($V_{th} = 0.47\ V$) is detected after 10 hours of operation. This device[6] is removed from the test, so the final group under study is composed of only nine samples.

Fig. 2.20 shows the evolution of the normalized value of V_{th}, R_{ds}, and V_f. Fig. 2.20c shows a noticeable V_{th} drop (about 20 % after 100 hours of operation). However, the degradation rate

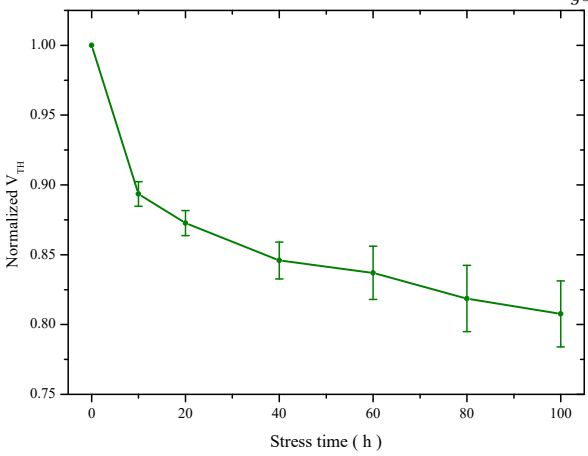
[6] The gate leakage current of this device remains acceptable (Igs=500 pA at $V_{gs} = 22\ V$), but it is necessary to notice that its threshold voltage was in the lower range allowed by the manufacturer [149] ($V_{th} = 1.97\ V$ at $V_{ds} = 1\ V$, $I_{ds} = 100\ \mu A$) when it has been characterised initially at room temperature.



(a) Normalized R_{ds}. Characterized at $I_{ds} = 10$ A and $V_{gs} = 20$ V.



(b) Normalized V_f. Characterized at $I_f = 10$ A and $V_{gs} = -8$ V.



(c) Normalized V_{th}. Characterized at $I_{ds} = 100$ μA and $V_{ds} = 1$ V.

Figure 2.20 – Normalized evolution of R_{ds}, V_f and V_{th} for CMB test (DUT always blocked at $V_{gs} = -8$ V). Characterizations realized at room temperature.

decreases over time. It is therefore necessary to continue the tests over a longer period of time in order to assess if there is some stabilization.

In fig. 2.20b, one can observe that the forward voltage drop of the intrinsic diode remains constant. This suggests that there is no noticeable degradation of the P-N junction, contrary to previously reported in the literature [146, 145]. This is consistent with the static test from section 2.3. The on-state resistance (see fig. 2.20a) of the MOSFETs also remains stable, even if a larger experimental scattering is observed on this parameter among the samples.

Fig. 2.21 shows the V_{th} degradation extrapolated to 10,000 hours of operation. Curve fitting has been performed using the least squares method (and including some data points acquired for 4 samples up to 400 h). After 10,000 hours of operation, one can predict a 35 % drop in V_{th}.

Fig. 2.22 shows the evolution of the parameters R_{ds}, V_f, and V_{th} over 100 hours for the MOSFETs of ST, ROHM (3 samples of each rreference) and Wolfspeed (9 samples), as well as the results obtained on Wolfspeed MOSFETs. The applied gate-source voltage is chosen close to 80% of the absolute maximum rating for V_{gs} in the off state (quoted at -10 V for ST

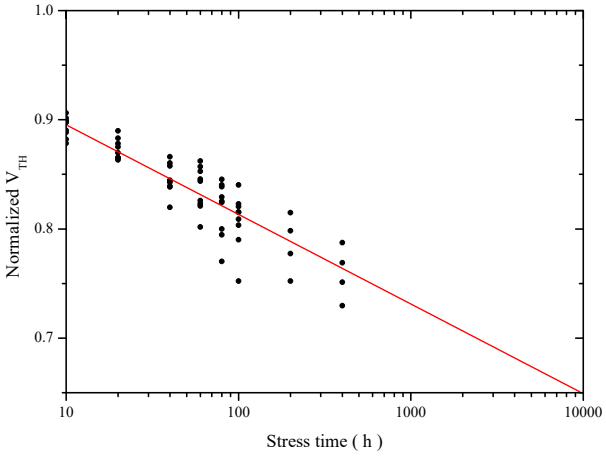


Figure 2.21 – Evolution and extrapolation of normalized V_{th} over CMB test stress. Characterization at ambient temperature, $I_{ds} = 100\ \mu A$, $V_{ds} = 1\ V$.

and Wolfspeed, and -6 V for ROHM). Thus, for ROHM samples $V_{gs} = -5\ V$ and for ST and Wolfspeed samples $V_{gs} = -8\ V$.

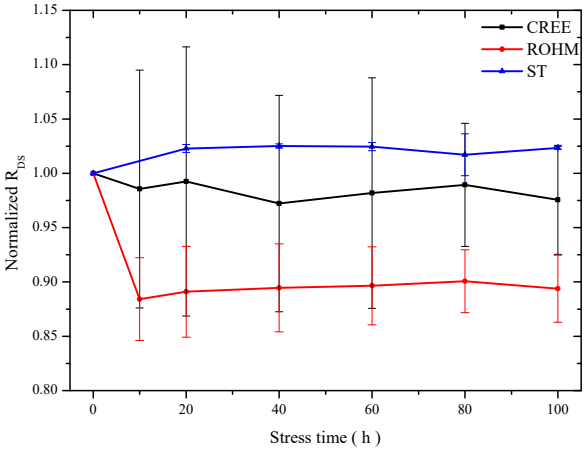
Fig. 2.22a and fig 2.22b shows the evolution of the internal on-resistance and the forward voltage for all three manufacturers. It can be seen that even if there is an initial reduction in R_{ds} for ROHM devices, it leads to stabilize and remains lower than 15%. ST MOSFETs remains stable throughout the test. The same behaviour is seen on the forward voltage. Thus, there is no noticeable difference with Wolfspeed MOSFETs on the regard.

However, fig. 2.22c shows a very remarkable difference on the threshold voltage behaviour. While Wolfspeed MOSFETs shown a very important drift in their threshold voltage (by about 20%), whereas devices of the two other manufacturers remain relatively stable, with a maximum change in V_{th} of $<$5% of its initial value.

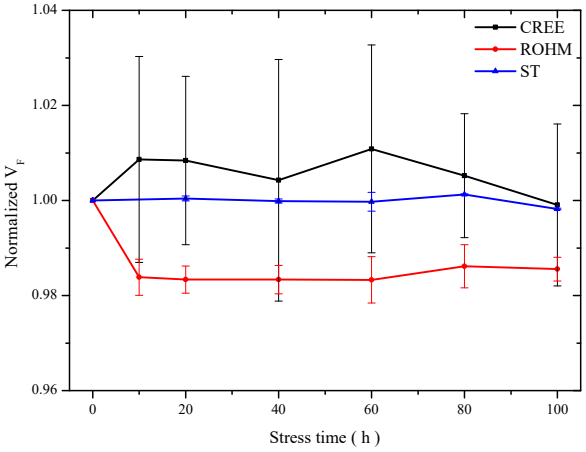
On CMB1, perturbations on the DUT V_{gs} are important, reaching peaks at V_{gs}=-11.4 V(see annex A.5). This exceeds the maximal value allowed by the manufacturer [149], which is V_{gs}=-10 V. As this could damage the devices or cause a V_{th} drop, a second test-bench (CMB2) version has been designed to reduce EMC perturbations, especially on the gate-source voltage of the DUT.

Even if EMC perturbations and gate-source voltage peaks are dramatically reduced on the second test-bench (CMB2) (see annexe A.5), it produces unexpected results: a higher V_{th} drop is observed with CMB2 than on CMB1. The results obtained on CMB2 for three samples are shown in fig. 2.23, were they are compared with the results obtained on CMB1. In both cases, the test conditions are identical($V_{gs} = -8\ V$, $I_{sd} = 10$ A, $T_j = 150\ ^\circ$C) and devices are characterized at the same point of operation. Looking at CMB2 results, it can be seen that the threshold voltage drops by between 37% and 48% after 100 hours of stress. This V_{th} drop is near twice that observed on CMB1.

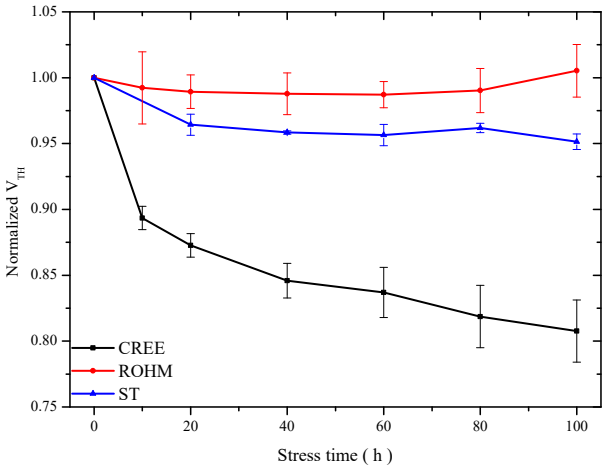
A second test is run on CMB2 in order to asses if the gate-source voltage impacts the V_{th} drift. Thus, gate-source voltage is fixed at $V_{gs} = -5\ V$ and the test is run on three samples (Wolfspeed). Fig. 2.24 shows the obtained results for this test. Devices are characterized before the test and every 20 hours of stress. An additional characterization is performed after 5 hours of stress. Unfortunately, two of the three devices under study have failed within a few hours.



(a) Normalized R_{ds}. Characterized at $I_{ds} = 10$ A and $V_{gs} = 20$ V.



(b) Normalized V_f for $I_f = 10$ A, $V_{gs} = -8$ V (Wolfspeed, ST) and $V_{gs} = -5$ V (ROHM).



(c) Normalized V_{th}. Characterized at $I_{ds} = 100$ μA and $V_{ds} = 1$ V.

Figure 2.22 – Comparison of normalized R_{ds}, V_f and V_{th} evolution for CMB1 test for different manufacturers (ROHM, ST, Wolfspeed). Characterizations realized at room temperature.

The most probably cause of the failure is a short-circuit event provoked by a perturbation on the gate-source voltage.

Anyway, fig. 2.24 shows that a lower gate-source potential minimizes the V_{th} drift. After 5 hours of stress, the most important part of the V_{th} drop has occurred, but it does not exceeds a 5% of the initial value. For the two devices which failed during the test, V_{th} drop is about 5% on its last characterization (40 hours for CMB26 and 60 hours for CMB24). The test on sample CMB25 is run for 100 hours without failure, showing a the V_{th} drop of nearly 7%. It is found to be stabilized after 60 hours. This contrasts with the threshold voltage drop shown in fig. 2.23 for the devices tested at $V_{gs} = -8$ V on the same test-bench (CMB2), with a V_{th} drop between 37% and 48% after 100 hours of stress.

2.4.2.2 CMB Test Results -Channel sometimes conducting-

In this case, the switching pattern is more complex (and more realistic): during the switching cycle, the current flows either through the internal diode or through the channel of the DUT

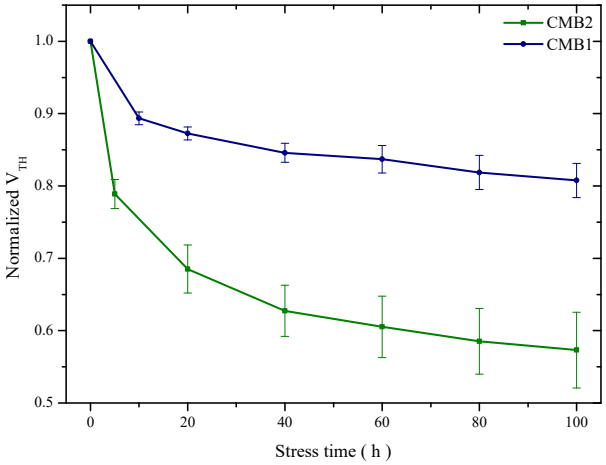


Figure 2.23 – Evolution of normalized V_{th} over CMB test stress for CMB1 and CMB2 test-bench ($V_{gs} = -8\ V$). Characterization at ambient temperature, $I_{ds} = 100\ \mu A$, $V_{ds} = 1\ V$.

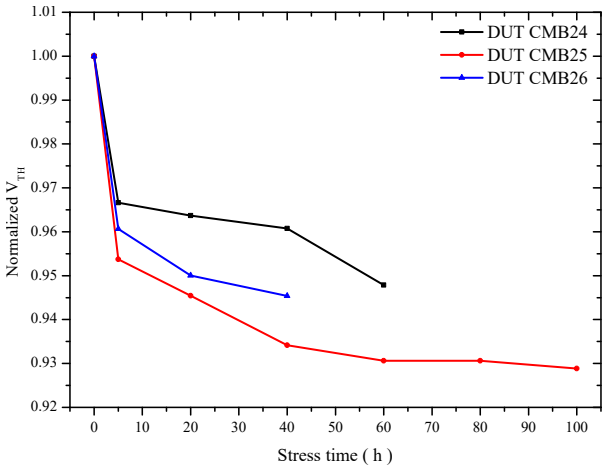
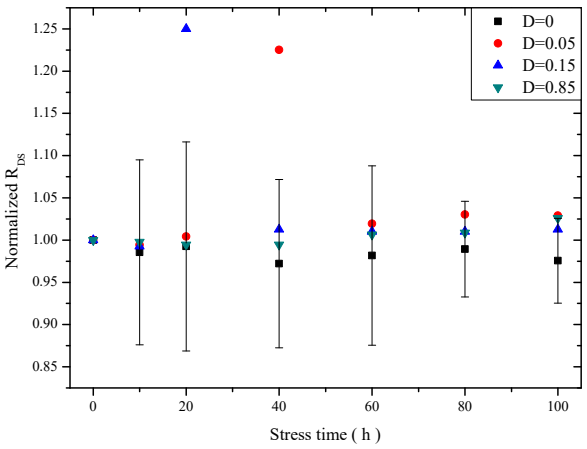


Figure 2.24 – Evolution of normalized V_{th} over CMB test stress (test-bench CMB2, $V_{gs} = -5\ V$) for three samples. Characterization at ambient temperature, $I_{ds} = 100\ \mu A$, $V_{ds} = 1\ V$.

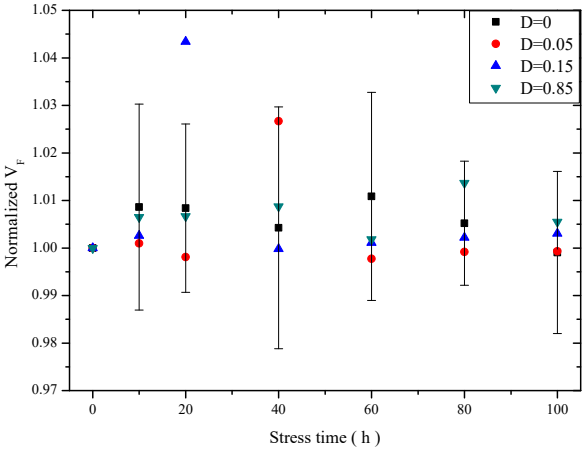
(see table 2.3 and fig. 2.19). The test is run on only one sample for each test condition (D=0.05, D=0.15 and D=0.85), but it clearly shows a different V_{th} drift for the different duty cycles. Further studies may be realised for more accurate results. The test is performed using the first version of the test-bench, not on the improved one (see annexe A.5) and at $V_{gs} = +20/-8\ V$.

Fig. 2.25 shows the evolution of R_{ds}, V_f and V_{th} for different duty cycles (D). Internal on-resistance (fig. 2.25a) and forward voltage (fig. 2.25b) remain almost stable with changes of less than 3% and 1% respectively after 100 hours of stress. Measurement points after 20 hours for D=0.15 and after 40 hours for D=0.05 presents aberrant errors.

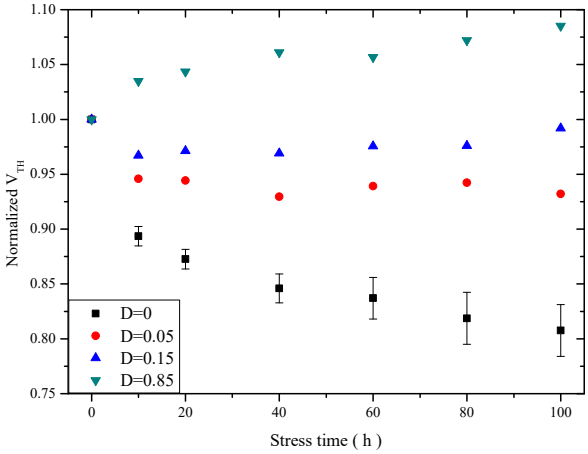
The most remarkable is the influence of the duty cycle (D) on the threshold voltage degradation, which is shown in fig. 2.25c. The cases where D=0 (which corresponds to the tests presented in the previous section), D=0.05 and D=0.15 are fully comparable with each other, as the conduction time through the intrinsic diode remains at 50% of the switching cycle (20 kHz). It is observed that for a low duty cycle (5 or 15 %), the threshold voltage shows a weak negative drift and seems to stabilize rapidly.



(a) Normalized R_{ds}. Characterized at $I_{ds} = 10$ A and $V_{gs} = 20$ V.



(b) Normalized V_f. Characterized at $I_f = 10$ A and $V_{gs} = -8$ V.



(c) Normalized V_{th}. Characterized at $I_{ds} = 100$ μA and $V_{ds} = 1$ V.

Figure 2.25 – Normalized evolution of R_{ds}, V_f and V_{th} for CMB1 test for different duty cycles (D). Characterizations realized at room temperature.

For larger duty cycle (D=85 %), the threshold voltage presents a positive drift of about 9 %. Further investigation is necessary in order to assess whether this augmentation could result in a higher internal resistance of the device, and therefore higher conduction losses. Indeed, on the tested device, a R_{ds} increase of 2.6 % is measured (see fig. 2.25a). Also, further analysis would be required in order to determine the influence of additional parameters such as applied V_{gs} or dV/dt.

2.4.3 Discussion

The aim of this set of experiments was to study the phenomenons observed in section 2.3 in more realistic conditions. For this, the DUT has been tested in a DC/DC converter, stressing its internal diode in inductive switching conditions. Initially, the devices under test have remained always blocked, with current flowing through their internal diode. On a second test, different duty cycles have been applied to the DUT in order to analyse if its duration has any impact on the voltage drift observed in section 2.3.

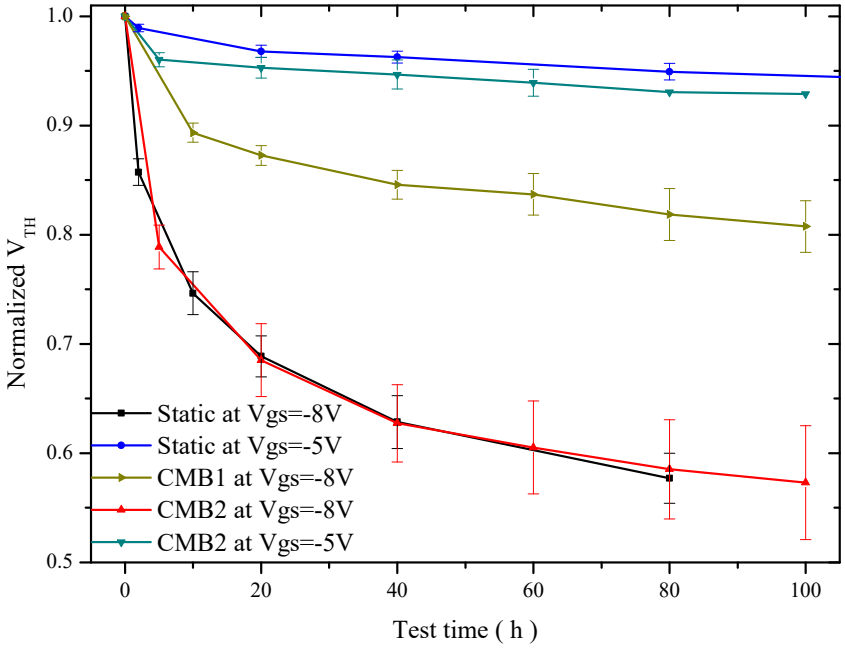


Figure 2.26 – Comparison between results obtained from CMB tests stress and from static test (3rd quadrant) for two different gate-source voltages ($V_{gs} = -8\ V$ and $V_{gs} = -5\ V$). For CMB tests, the internal diode is only biased 50% of the test time.

In all cases, no significant increase of the forward voltage or the internal on-resistance is observed, as shown in figures 2.20 and 2.25.Overall, the increase of R_{ds} and V_f after 100 hours of stress is always lower than 8% and 2% respectively. This is consistent with the findings of section 2.3 (static tests). Thus, we can conclude that SF defects in the substrate have been significantly reduced.

However, as observed in section 2.4.2.1, an important threshold voltage drift is observed. It is possible to estimate a V_{th} drop of 35% after 10,000 hours of stress for the case where the channel remains always blocked with $V_{gs} = -8\ V$. But the most surprising result is that this V_{th} drop can be even higher in a test-bench with lower EMC perturbations and where the gate-source voltage is more stable (CMB2). This is clearly shown in fig. 2.23, where it can be seen that the V_{th} drop can reach nearly 50% after 100 hours of stress.

This threshold voltage drop is consistent with results obtained in section 2.3.2.2, where the static test on the third quadrant of operation at $V_{gs} = -8\ V$ reports a comparable drop of the V_{th} (about 45%) and where the threshold voltage after 1000 hours of stress has been extrapolated to 38.5% of its initial value.

Equally, results obtained in section 2.3.2.2 for the third quadrant of operation, but at $V_{gs} = -5\ V$ are consistent with the results obtained on the CMB2 test-bench for the same gate-source voltage. In all cases, the threshold voltage drop does not exceeds 8%.

The observed threshold voltage drift may be due to to carrier injection phenomenon and trapping at the SiO_2/SiC interface, or in the oxide. The fact that lower perturbations on the gate-source potential induces a higher threshold voltage drop, could be due to a de-trapping phenomenon which would occurs when an important reduction of the potential takes place. Chapter 3 will focus in the MOSFET gate oxide.

Further analysis, applying different duty cycles to the DUT, are realized. It shows that the duty cycle has an important impact on the threshold voltage stability.

On the one side, for a small duty cycle (5 or 15%), threshold voltage decreases weakly during the first hours of stress and then remains stable. The maximum V_{th} drop is 8% after 100 hours for the case where D=0.05. On the other side, for a relatively high duty cycle (D=0.85), V_{th} shows a increase of about 9% after 100 hours of stress. It is noticeable that according to table 2.3, in this last case the internal P-N junction is stressed for a very short time.

The weak threshold voltage drop in the cases where a the duty cycle is no longer 0, but it remains small (5 or 15%), could be explained by the same de-trapping phenomenon as in the case where important perturbations appears on the gate-source voltage (reducing the applied gate-source potential).

Further studies should investigate the case where a large duty cycle is applied, as for the case where D=0.85, which reports an increase of about 9% on the threshold voltage. It could be thought that this is due to a trapping phenomenon when a high electric field is applied for a long time, but this has not been observed with the static tests (1st and 4th quadrant) presented in section 2.3.2.2.

2.5 Conclusions

The main objective of this chapter was to study the robustness of the internal P-N junction of SiC MOSFETs, for their posible utilisation in diode-less applications. Obtained results highlighs that the intrinsic diode does not show any a significant degradation when it is used. This differs from previous reports in the literature, and may indicate an improvement in the SiC substrate quality, with a reduction of its defect density as reported in recent years [158, 159]. Among these defects there are the basal plane dislocations or stacking faults, which would cause degradation of the P-N junction.

However, an unexpected drift of the threshold voltage has been observed. Presumably, it is due to carrier injection and trapping at the SiO_2/SiC interface, or in the oxide. This injection depends on the polarity of the voltage applied at the gate, as well as on the application time (i.e. the duty cycle).

Carrier injection phenomenon are related to the electric field as well as to the barrier height. We find that when the device is blocked at $V_{gs} = -5\ V$ the V_{th} drift is much lower than when it is blocked at $V_{gs} = -8\ V$. Thus, a threshold factor appears. In fig. 2.26 it can be seen that there is no significant difference between the V_{th} drift observed on the CMB2 test stress and on the static tests (3rd quadrant of operation). Thus, repetitive inductive switching does not cause a noticeable degradation.

However, this degradation of the threshold voltage has not been observed during the static tests where the internal diode is not solicited (1st and 4th quadrant of operation), nor during the standard HTGB test. Thus, further study is required about this, especially taking in account that a positive V_{th} drift has been observed in CMB test stress in the case when a high duty cycle is applied (D=0.85).

Another remarkable issue is that perturbations on the gate-source voltage may induce a de-trapping phenomenon, due to a temporary lower potential applied between the gate-source terminals. This minimizes the observed V_{th} drift, as it has been shown in fig. 2.23. In the same

way, as soon as the duty cycle is not zero, there is a gate-source polarity inversion which will trigger this de-trapping phenomenon. Thus, also in this case V_{th} drift is minimized.

In a real application case, the diode is only used during a small fraction of the overall switching cycle (during dead-times). Therefore, and taking in account that gate-source polarity will not be always negative, we can conclude that it is possible to use the internal diode instead of adding an external diode ("diode-less" applications). Anyway, Wolfspeed MOSFETs C2M0080120D seem to be more sensitive to this phenomenon that their competitors and require further tests, especially at extremes duty cycle.

The experiments presented here show that the standard JEDEC tests used on silicon IGBT and MOSFETs are not fully suited to SiC devices. The degradation observed of the gate oxide, both on static and CMB tests is indeed not revealed by standard HTGB tests. Thus, standard tests must be revised or new tests must be added to the qualify procedures.

Regarding the driving circuit, and to prevent short-circuit problems which may arise from a reduction in threshold voltage, the use of a negative voltage to block the device is recommended. However, care must be given in the choice of the negative V_{gs} level, as a larger value, although it would give a better EMI immunity, may cause V_{th} to drift faster. In the case of Wolfspeed MOSFETs, it was found that $V_{gs} = -5\ V$ is more suitable than $V_{gs} = -8\ V$. This finding is confirmed by the most recent datasheet from Wolfspeed, where a $V_{gs} = -5\ V$ is recommended for applications where the body diode is used.

Future work should include a larger number of samples to obtain more reliable results, based on samples from several manufacturers as well as on the newest generations of devices, as they tend to improve rapidly. Furthmore, as shown by the different results acquired from both versions of the CMB setup, V_{gs} itself is not the only parameter which has an influence on the V_{th} drift. $\Delta V_{gs}/\Delta t$ or EMI transient also may have an effect which must be assessed in future studies.

Chapter 3

Robustness of the MOSFET gate oxide

Contents

3.1 Introduction

In spite of the better properties of SiC versus Si, which were shown in chapter 1, SiC power MOSFETs are just penetrating into industrial applications. This is due to their lack of maturity and some reliability issues which were also introduced in that same chapter. One of these issues is related to the oxide layer and more particularly to the SiC/SiO_2 interface, as it was highlighted in chapter 2. This chapter focuses on the behaviour of this oxide layer, which even if it is identical in chemical composition as the oxide used in Si MOSFETs (SiO_2), is weaker due to its smaller thickness (thus, supporting a higher electric field) and lower energy band difference with SiC.

As it was presented in chap. 1, gate robustness is related to the SiO_2 insulator layer located between the gate terminal and the drift region. In this chapter, we focus on the two main measurements used to asses the degradation of the gate oxide:

- Bias Temperature Instability - BTI
- Time Dependent Dielectric Breakdown - TDDB

In a first time, we study bias temperature instabilities on commercial SiC MOSFETs. The objective of this study is to asses if the V_{th} drift observed in some cases in chapter 2, is reproduced here. Moreover, the gate leakage current is measured in order to evaluate if this parameter can be used to assess the gate oxide degradation.

In a second time, a study of TDDB is realized with the same commercial SiC MOSFETs. The objective is to assess if this devices can run for over 100.000 hours as required in industrial applications. In this case, the gate leakage current is monitored over the duration of the test, in order to study if there is any common behaviour which could indicate that the oxide is near to fail. This test is run also for some samples under inductive switching conditions in order to evaluate if this could impact TDDB estimation.

3.2 Degradation of the Gate Oxide

BTI and TDDB measurements, as well as some physical notions about these phenomena, were detailed in chap. 1. Here, some basic issues are remembered to provide grounds for comparison with our study, which is presented in the following sections.

3.2.1 Bias Temperature Instability - BTI -

The instability of the threshold voltage, or bias Temperature instability (BTI [148]), is a phenomenon which results in a gradual variation of the threshold voltage (V_{th}) when a voltage is applied between the gate and source terminals of a MOSFET. The temperature is an acceleration factor of this phenomenon. V_{th} instability can result in a positive shift (PBTI) or negative one (NBTI), depending on the applied electric field between the gate-source terminals. In the PBTI case, this could lead to a higher on-state resistance. In the NBTI case, this can lead to a higher I_{ds} leakage current and to a lower immunity towards EMI.

Several papers, such as [123], study this phenomenon. Fig. 3.1 shows the evolution of the V_{th} for devices biased at V_{gs}=20 V, V_{gs}=-5 $V$and V_{gs}=-10 V, at 150 °C. It can be seen that

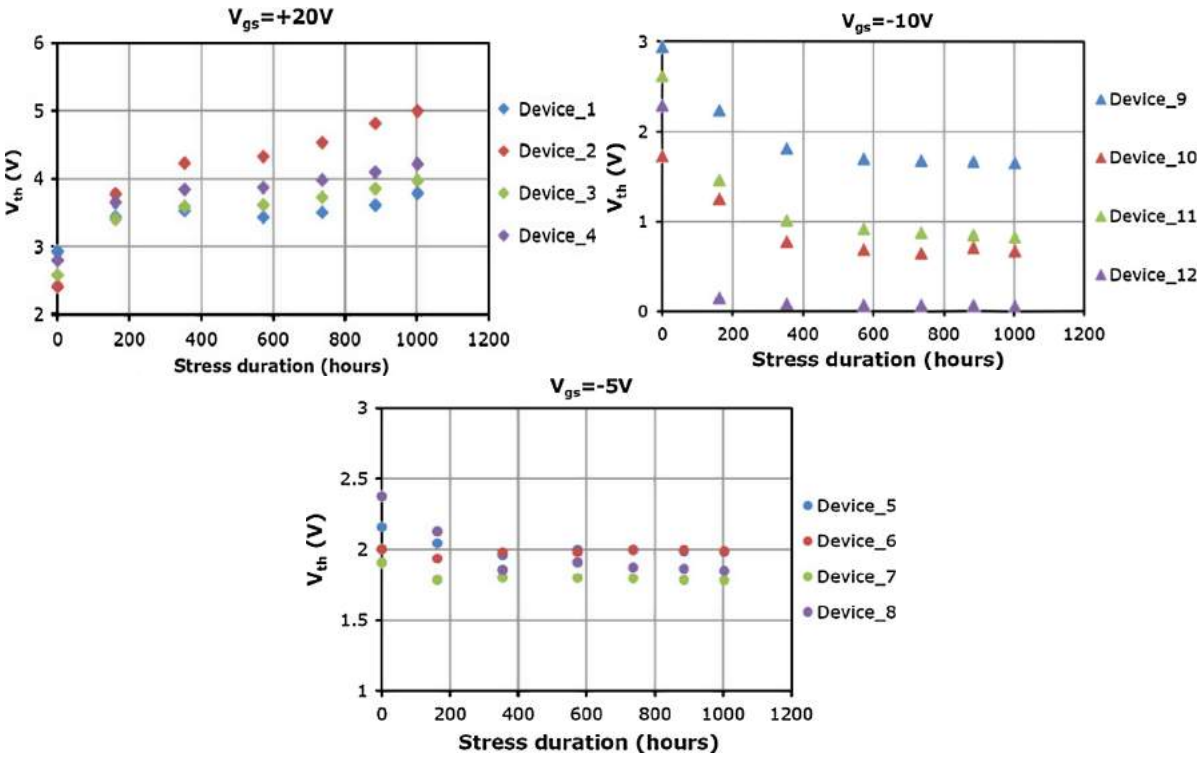


Figure 3.1 – Evolution of V_{th} for HTGB tests at V_{gs}=20 V, V_{gs}=-10 $V$and V_{gs}=-5 V[123].

for a positive gate bias stress (V_{gs}=20 V), the value of the voltage threshold at the end of the test can double with regards to the initial value. In the case of a negative gate bias stress, a slight reduction of the V_{th} is observed when the gate-source terminals are biased at -5 V, but when they are biased at -10 V, this can result in a dramatic failure, with devices becoming normally-on. This highlights the importance of the applied voltage values in BTI apparition.

To our knowledge, the evolution of the gate leakage current (I_{gs}), which could indicate a degradation of the gate insulator, has not been studied deeply. Only in a few papers, as [82], a measurement of this parameter is realized, but presented tests do not correspond to standard JEDEC HTGB (High Temperature Gate Bias) tests [148]. As HTGB test is defined specifically to stress the insulator, we realize HTGB tests at different temperatures, stopping the test and measuring the evolution of the main parameters, including the gate leakage current.

However, other test circuit configurations are tested in order to verify that HTGB test is the most stressfull one or adapted to SiC devices. *Fayyaz et al.* reported in [160] an interesting study about the electric field applied on the oxide for several cases. Some of them are depicted in fig. 3.2.

As it can be seen, the case where the electric field in the gate oxide is lower (fig. 3.2c) is when drain-source terminals are short-circuited and $V_{gs} = -5\ V$. However, if a drain-source voltage (600 V) is applied, the electric field in the oxide increases significantly, as can be seen in (fig. 3.2a). In this last case, the electric field is very similar but slightly higher (especially near the P-N junction) to that presented in fig. 3.2b, where V_{ds}=600 $V$and gate-source terminals are short-circuited. Of all presented cases, the one which shows the higher electric field in the oxide is when drain-source terminals are short-circuited and $V_{gs} = 20\ V$ (fig. 3.2d). However, in some cases, differences are not very important, and calculated electric field values remains in the same order of magnitude. It is remarkable that in all cases, the most important zone relative to a V_{th} drift is located near the channel P-well.

3.2.2 Time Dependent Dielectric Breakdown - TDDB -

TDDB is the lifetime estimation of the dielectric for a given electric field and temperature. In the SiC MOSFETs, the dielectric used to insulate the gate terminal is SiO_2. Both parameters, the electric field and the temperature, are accelerator factors of the oxide degradation.

During gate bias stress, electrical charges can tunnel into the oxide and remain trapped. This results in an increase of the electric field. When the electric approaches its critical value, an increase of the leakage current or even a short-circuit between gate and source terminals occurs. Then, the TDDB can be defined as the time that the gate oxide takes to fail under a given electric field and temperature conditions.

There are few studies in the literature regarding TDDB on commercial SiC MOSFETs. Most studies are based on MOS capacitor structures or research MOSFETs, as in [113]. In its scientific publications, Wolfspeed has shown an estimation of TDDB for its Gen2[1] MOSFETs, and reports an expected lifetime of $8 \cdot 10^6$ hours at V_{gs}=20 V [127], as it is depicted in fig. 3.3. Nevertheless, in our knowledge, there is no similar data from authors not related with the manufacturer.

[1]Wolfspeed differences [161] between "Generation 1" (Gen1, launched in 2011) and "Generation 2" (Gen2, launched in 2013) MOSFETs. Both Generations are based on planar technology, as well as Gen3 SiC MOSFETs (900V, year 2016). The Gen4 is expected to be based in trench gate technology.

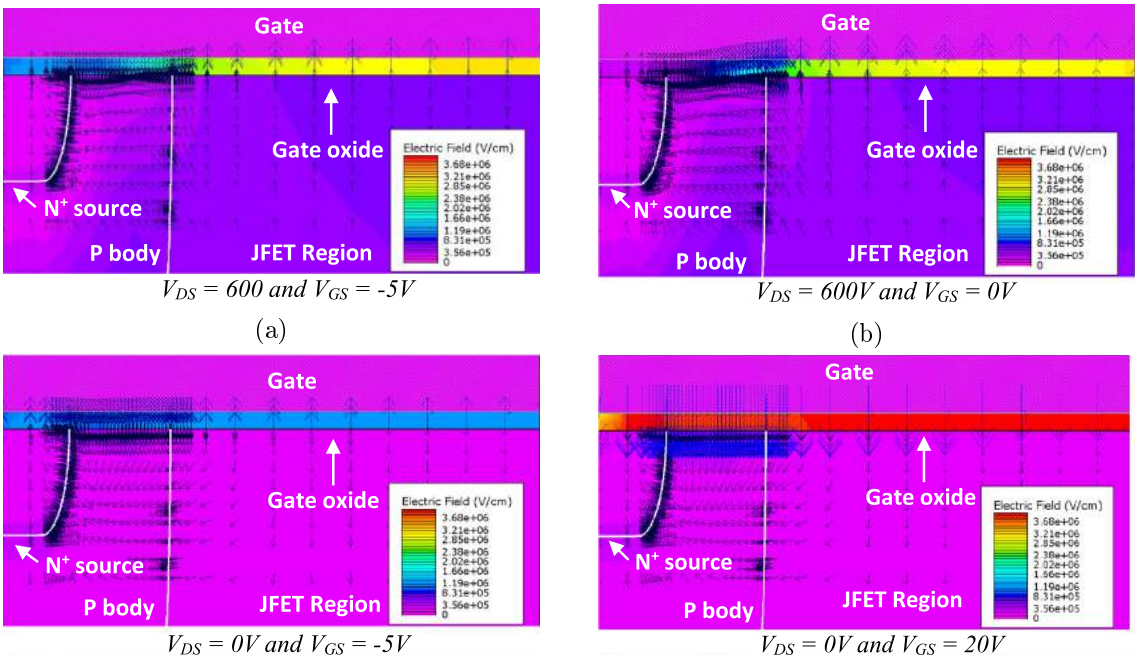


Figure 3.2 – Electric field in the gate oxide depending on the gate-source and drain-source voltage [160].

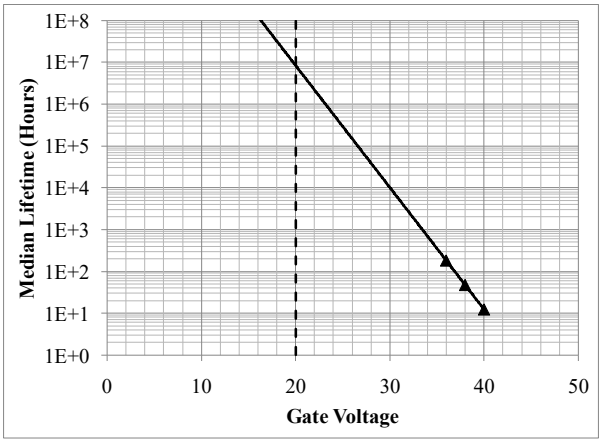


Figure 3.3 – Estimation of TDDB at 150 °C for Gen2 CREE MOSFETs [127].

Ouaida, in his thesis manuscript [82], realized an extrapolation of the TDDB as a function of the temperature. This is shown in fig. 3.4. This experiment presents a particularity, because contrary to [127] where the devices were biased in a static mode, here the devices are constantly switching over a resistive load and gate-source terminals are biased successively at +20 and -5 V(f=10 kHz).

In this chapter, a static mode TDDB, as well as on the corresponding failure mechanisms are studied. Moreover, some experimental data points are extracted in order to estimate the TDDB of devices placed in a real converter, driving an inductive load. Obtained results are compared in order to determine if this condition could impact the expected lifetime of SiC MOSFETs.

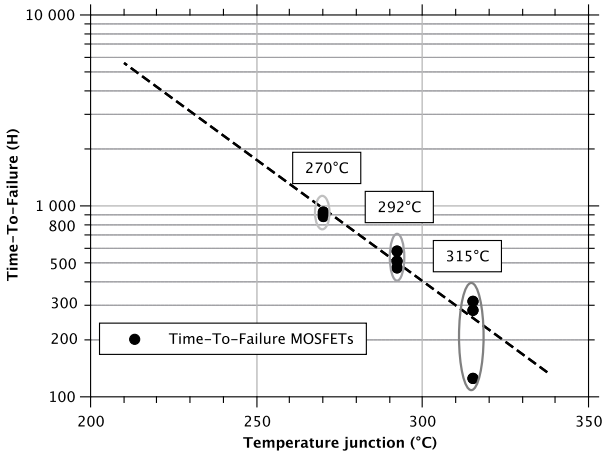


Figure 3.4 – Estimation of TDDB depending on temperature for Gen1 CREE MOSFETs commanding a resistive charge [82].

3.3 Study of the bias temperature instability -BTI-

HTGB tests are realized in order to study if there is a V_{th} drift and an increase of the leakage current I_{gs}. An increase of I_{gs} could indicate a degradation of the gate oxide and eventually, it would allow to implement a health monitoring system.

Devices under study are Wolfspeed C2M0080120D SiC MOSFETs [152] and characterizations are realized using an Keysight B1505B curve tracer to determine the V_{th}. The measurement of I_{gs} requires a high accuracy (in the order of 100 fA), thus a measurement test-bench has been built using an Keithley SMU 2636B. This is described in annexe A.2, within the protocol used to measure V_{th}.

A preliminary set of tests (section 3.3.1.1) is run in order to determine the set-up configuration to stress the devices. Several configurations are compared in a test where the temperature is increased every 24 hours in order to accelerate the degradation. As a result, retained configuration is the standard HTGB test with a positive gate bias (see annexe A.1).

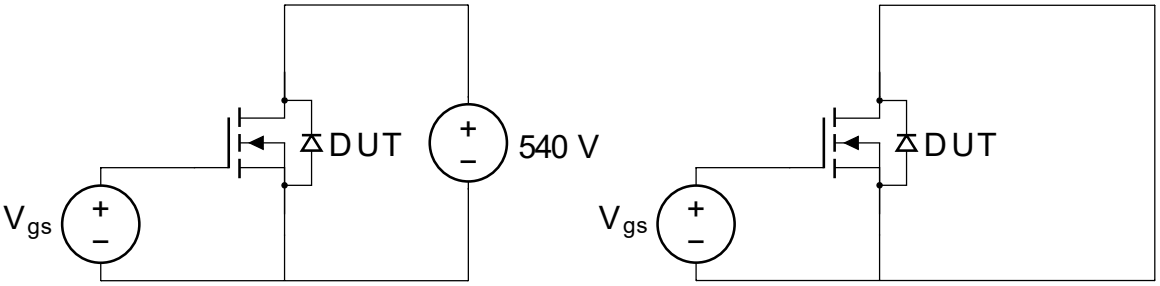
Tests are run at 150 °C (the maximal junction temperature allowed by the manufacturer [152]) and 200 °C. The test run at 200 °C ensures the apparition of an important V_{th} drift. The objective is to study if an I_{gs} increase occurs, and if there is a correlation between the V_{th} drift and the leakage current I_{gs}.

Finally, results at 200 °C are compared with MOSFETs from other manufacturers (ST, ROHM) in order evaluate if the same V_{th} drift appears. As described in chapter 2, Wolfspeed MOSFETs shown a much larger drift in their threshold voltage than that observed on devices from the other manufacturers.

3.3.1 Experimental Methodology

3.3.1.1 Preliminary tests

As introduced in section 3.2.1, test circuit configuration as well as applied voltage values, can impact instabilities magnitude. Thus, before to run our test, it is considered necessary to realize some preliminary investigations using different configurations and V_{ds} and V_{gs} magnitudes. Fig. 3.5 shows the two main configurations for these preliminary tests.



(a) (b)

Figure 3.5 – Main circuit configurations for the preliminary tests.

Test	Device	samples (N)	V_{gs} (V)	V_{ds} (V)	T_j (°C)
Config 1	C2M008012D[a]	1	0	540	150..200
Config 2	C2M008012D[a]	1	-8	540	150..200
Config 3	C2M008012D[a]	1	22	0	150..200
Config 4	C2M008012D[a]	1	-8	0	150..200
Config 5	C2M008012D[a]	1	-5	0	150..200

Table 3.1 – BTI tests summary.

[a]Ref. W10216, year 2016.

Obviously, one test is realized with relatively high gate-source voltage (22 V) and with drain and source terminals short-circuited. Additionally, two different tests are realized with a bus voltage of 540 V; one with $V_{gs} = -8\ V$, and the other one with the gate-source terminals short-circuited. It is noticeable that the first one is the same HTGB test presented in chapter 2, where it was run at 150 °C only (200 °C here).

Moreover, even if the electric field in the oxide is not expected to be so high, two other tests are realized with the drain and source terminals short-circuited. In one case the applied voltage is $V_{gs} = -5\ V$and in the other one it is $V_{gs} = -8\ V$. The reason to realise these tests is that these voltages were used in the third quadrant static test in the chapter 2, where an important drift of the threshold voltage was reported.

Table 3.1 summarizes all realized preliminary tests. Used devices for these tests are in all cases C2M0080120D Wolfspeed MOSFETs, which are previously characterized. Tests are run for one week at 150 °C. After that, temperature is increased by 10 °C every 24 hours up to 200 °C, when the temperature is maintained for 4 days until the end of the test. Devices are characterized at the end of the first week before starting the temperature steps and at the end of every temperature step. In the case when the temperature is 200 °C, a characterization is realized after 24 hours, as well as a final one when the test is finished. The corresponding temperature profile is depicted in fig. 3.6.

All characterizations are realized at room temperature and in agreement with measurement protocols presented in annexe A.2, and after a cool-down time of 1 hour.

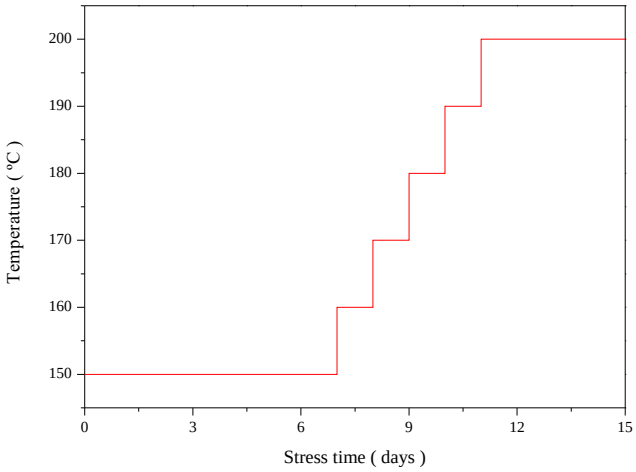


Figure 3.6 – Temperature profile used for the preliminary tests.

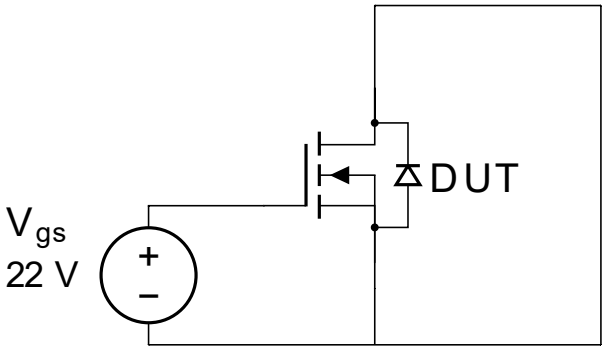


Figure 3.7 – Configuration used for HTGB tests over 1000 hours (Config 3).

3.3.1.2 HTGB Tests

As described later in section 3.3.2, results from the preliminary tests shown that the most stressful configuration for the BTI is when drain and source terminal are short-circuited and a relatively high gate-source voltage is applied. This is in agreement with the results reported by *Fayyaz et al.* [160] and which have been presented earlier.

This configuration, depicted in fig.3.7, also corresponds to the HTGB tests, described in JEDEC standards [148]. These standards specify that the voltage applied between gate and source must be close to the maximal V_{gs} allowed value, and in any case higher than 80% of the maximal value. Thus, the applied V_{gs} is defined in agreement with devices datasheets (see below).

The HTGB test is run for devices from three different manufacturers. Wolfspeed C2M0080120D devices are tested at two different temperatures: 150 °C, which is the maximum temperature allowed by the datasheet [152], and 200 °C. For ST SCT30N120 and ROHM SCT2080KE devices, the test is run only at 200 °C. It is noticeable that for the ST SCT30N120 the maximum junction temperature specified by the manufacturer is 200 °C [156], and for the ROHM SCT2080KE it is 175 °C [155].

Even if this temperature value is out of the specifications, the objective is not to realize

Test	Device	samples (N)	V_{gs} (V)	V_{ds} (V)	T_j (°C)
Config 3	C2M008012D[a]	4	22	0	150
Config 3	C2M008012D[a]	4	22	0	200
Config 3	SCT2080KE[b]	4	22	0	200
Config 3	SCT30N120[c]	4	22	0	200

Table 3.2 – HTGB tests summary.

[a] Ref. W10216, year 2016.
[b] Ref. CHN-GK-552, year 2015.
[c] Ref. 15-04, year 2015.

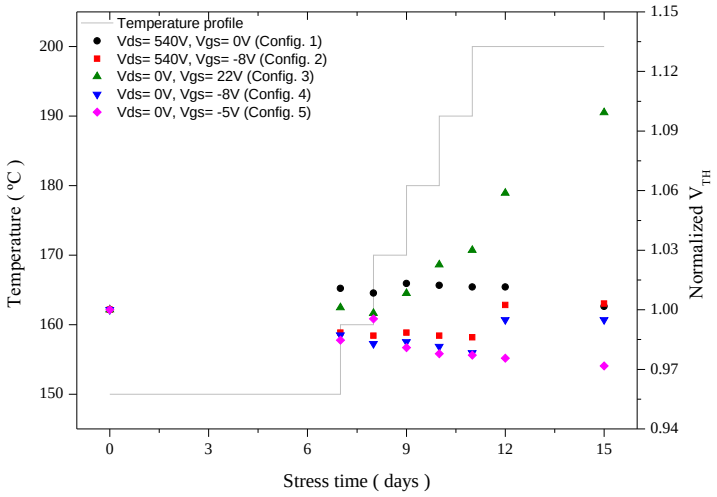
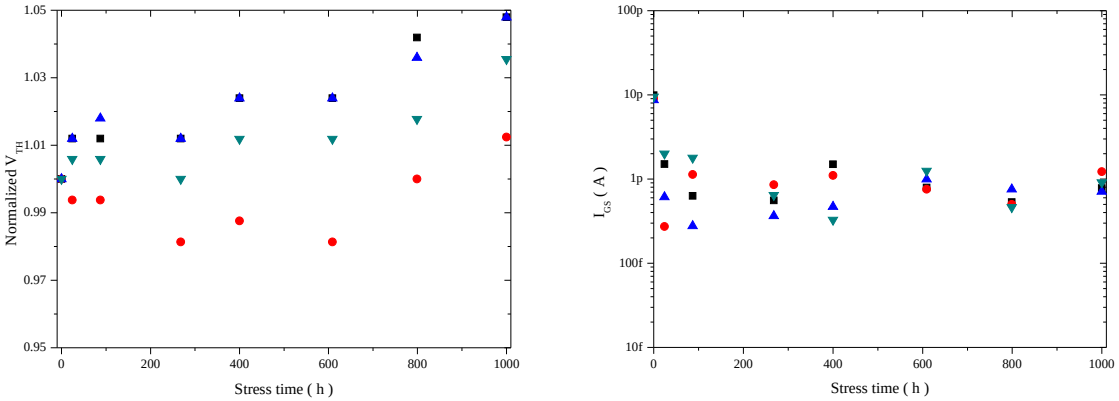


Figure 3.8 – Evolution of V_{th} for realized preliminary tests and the used temperature profile.

a standard HTGB test which can be easily found in the literature, but to accelerate the BTI phenomena in order to observe if an increase in the gate-source leakage current is associated to it.

The chosen gate-source voltage is V_{gs}=22 V, because this is the maximum V_{gs} allowed for ST SCT30N120. For the Wolfspeed C2M008012D, the maximal allowed V_{gs} is 25 $V$and for the ROHM SCT2080KE it is 26 V. Thus, at V_{gs}=22 V, in all cases the applied V_{gs} is higher than 0.8 times the maximum allowed value.

All tests are summarized in table 3.2. They are run for 1000 hours using 4 samples in each case. All devices are initially fully characterized at room temperature. The leakage current I_{gs} is also measured at 150 °C. All characterizations are realized according to the the protocols presented in annexe A.2 and A.3. The tests are regularly interrupted in order to characterize the devices, after a cool-down time of 1 hour. Time intervals between successive characterizations in not strictly constant for two main reasons: to better observe if a large effect is occurring during the first hours of tests, and for practical reasons (characterizations are performed during standard laboratory hours, 1 hour after cooling-down).



(a) Normalized V_{th}. Characterized at room temperature for $I_{ds} = 100\ \mu A$, $V_{ds} = 1\ V$.

(b) Leakage current I_{gs}. Characterized at $T_j = 150$ °C for V_{gs}=22 V, V_{ds}=0 V.

Figure 3.9 – Evolution of normalized V_{th} and I_{gs} for HTGB test conditions (V_{gs}=22 V, V_{ds}=0 V, $T_j = 150$ °C) for 4 Wolfspeed C2M0080120D samples.

3.3.2 Experimental Results

3.3.2.1 Preliminary tests

The results obtained from the preliminary tests shows that BTI is significant only in one of the cases, as it can be seen in fig. 3.8. Indeed, only in the case where a relatively high gate-source voltage (22 V) is applied and drain and source terminals are short-circuited, an increase in the threshold voltage of about 10% appears.

For this case, the voltage threshold remains almost stable for the characterizations realized after the stresses at 150 °C and 160 °C. Indeed, V_{th} starts to increase only after the temperature step stress at 170 °C. V_{th} drift seems to accelerate at 200 °C.

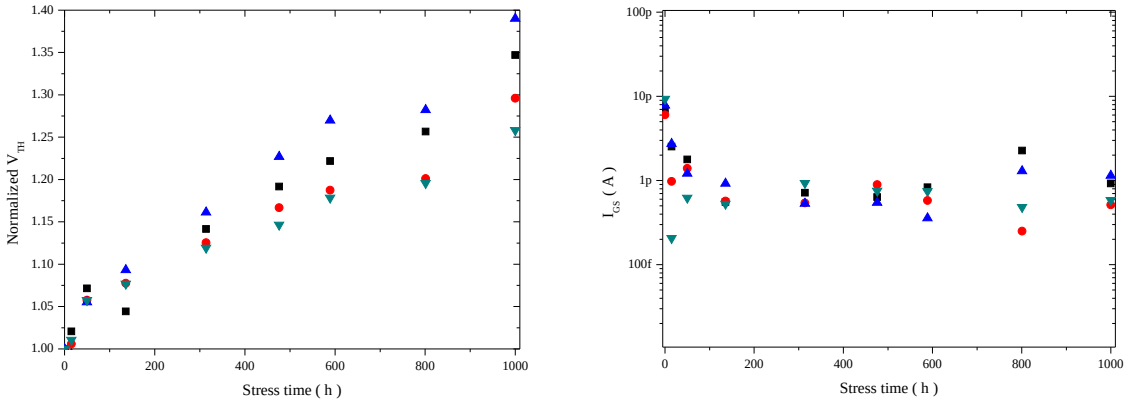
For all the other cases from table 3.1, there are some differences between the initial V_{th} characterization and the measurement realized after the stresses, but they are always lower to 3% (even at 200 °C). Thus, there is no obvious trend.

In any case, it seems evident that the most suitable configuration to stress the devices is for V_{gs}=22 V and V_{ds}=0 V (fig. 3.7). Moreover, this is consistent with the electric field simulations realized by *Fayyaz et al.* and presented earlier.

3.3.2.2 HTGB Tests

Here, obtained results of HTGB tests at 150 °C and 200 °C are presented. Fig. 3.9 shows the evolution of V_{th} and I_{gs} over the test realized at 150 °C, showing a slight increase in V_{th} (fig. 3.9a. This is in any case lower than 5% of the initial value after 1000 hours of test. The leakage current, as it can be seen in fig. 3.9b, shows an initial decrease from about 10 pA to near 1 pA, where it remains almost stable until the end of the test. The initial decrease could be related to an internal electric stabilization of the device.

Thus, we can consider that device characteristics remains almost stable under these test conditions ($T_j = 150$ °C), and that even if there is a slight increase in the V_{th}, the device does not present any additional risk of failure.



(a) Normalized V_{th}. Characterized at room temperature for $I_{ds} = 100\ \mu A$, $V_{ds} = 1\ V$.

(b) Leakage current I_{gs}. Characterized at $T_j = 150$ °C for V_{gs}=22 V, V_{ds}=0 V.

Figure 3.10 – Evolution of normalized V_{th} and I_{gs} for HTGB test conditions (V_{gs}=22 V, V_{ds}=0 V, $T_j = 200$ °C) for 4 Wolfspeed C2M0080120D samples.

A different behaviour is observed for the test realized at $T_j = 200$ °C, as is depicted in fig. 3.10. Even if the leakage current (see fig. 3.10b) shows a very similar behaviour from that observed in the tests realized at 150 °C, V_{th} shows a remarkable increase, comprised between 25 and 40% of its initial value. Indeed, this increase seems to evolve almost linearly with the stress time, and no stabilization or slow-down of the V_{th} drift is observed.

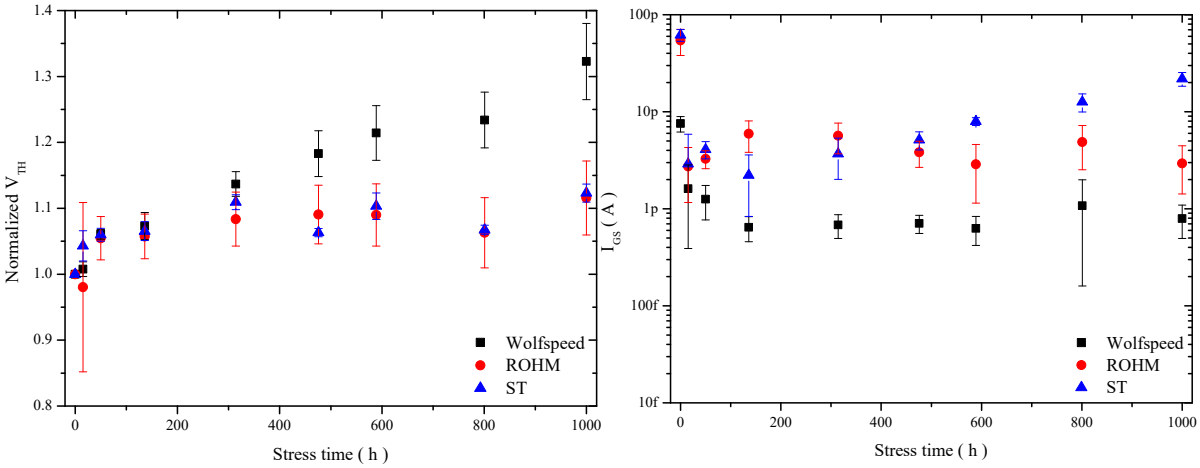
Fig. 3.11 shows the evolution of V_{th} and I_{gs} over the same HTGB test, comparing three different manufacturers (Wolfspeed, ROHM and ST). As it can be seen in fig. 3.11a, the V_{th} drift is much larger for Wolfspeed devices. On the contrary, the devices from ST and ROHM show an increase of V_{th} by about 12%, with an initial increase which tends to stabilise after some hours of stress. Regarding the leakage current I_{gs} (fig. 3.11b), all devices show an initial reduction of the leakage current after the first hours of stress. While the I_{gs} of ROHM and Wolfspeed devices remains almost stable after some hours of stress, it seems to increase slightly during the test for ST devices. However, even after 1000 hours of test, this I_{gs} leakage remains lower than its initial value.

3.3.3 Discussion

The preliminary tests demonstrates that some configurations are more stressful than others. Among all tested configurations, the typical PBTI/HTGB configuration where source and drain terminals are short-circuited and a positive gate-source voltage (>80% of the maximum value allowed) is applied, is found to be the most stressing one.

Using this configuration, Wolfspeed devices are stressed at their maximum allowed temperature ($T_j = 150$ °C). Device characterization reports only a slight increase in the V_{th}, lower than 5%, whereas I_{gs} remains almost constant once internal electric charges are stabilized.

The same test configuration, but this time at $T_j = 200$ °C (also on Wolfspeed samples) results in a large increase in the V_{th}. Nevertheless, as I_{gs} remains almost stable over all the tests, this parameter can not be considered as an indicator of the BTI. Moreover, the test



(a) Normalized V_{th}. Characterized at room temperature for $I_{ds} = 100\ \mu A$, $V_{ds} = 1\ \ V$.

(b) Leakage current I_{gs}. Characterized at $T_j = 150$ °C for V_{gs}=22 V, V_{ds}=0 V.

Figure 3.11 – Evolution of normalized V_{th} and I_{gs} for HTGB test conditions (V_{gs}=22 V, V_{ds}=0 V, $T_j = 200$ °C) over samples of three different manufacturers (ST, ROHM, Wolfspeed).

realized on ST devices under the same stress conditions is the only that has resulted in a slight increase in the leakage current, but without any correlation with the threshold voltage drift.

Comparing the three tested manufacturers, it is found that Wolfspeed devices shows lower robustness (increase in V_{th} over time, with a 40% drift over 1000 hours) than their competitors (ROHM and ST), which report similar behaviours with an increase in the V_{th} by about 12%, and a slowing-down of this increase over time.

While the leakage current should be monitored to detect the onset of some failure modes [162], it is not a good indicator of the oxide degradation or of the BTI phenomenon. This leads to consider that to evaluate the state of health of a SiC MOSFET it would also be necessary to study several additional parameters.

The most obvious should be the internal on-resistance, but unfortunately the results obtained in chapter 2 do not go in this direction. Thus, more complex alternatives such as the evolution of the internal capacitances or the threshold voltage have to be considered. In this way, *Hologne* shows in [163] some preliminary results to determine the state of health of a SiC module by measuring the Miller capacitance and its V_{gs} voltage during the Miller plateau.

3.4 Estimation of gate oxide breakdown time -TDDB-

As introduced in section 3.2.2, only a few studies focus on assessing the TDDB of commercial SiC MOSFET. Among these, some static tests provided by Wolfspeed on their own MOSFETs [127], and the PhD thesis of *R. Ouaida* [82], where the TDDB is estimated for a MOSFET placed in a real converter connected to a resistive load.

In this section, two different tests are presented. The first one is a static test which provides some data points, allowing to extrapolate the expected TDDB value at nominal conditions. In the second one, the MOSFET under study is placed in a DC/DC converter. However, contrary to the work of *R. Ouaida*, here the converter is driving a highly inductive load.

To realize the extrapolation to nominal conditions, the electric field is used as a acceleration factor. The main models used in the literature are the thermochemical breakdown model [164] and the hole-induced breakdown model [165]. From both models, the most conservative is the thermochemical breakdown model. Indeed *McPherson et al.* showed that for a low electric field the thermochemical model fits better [166]. Thus, the extrapolation to nominal conditions is achieved using this latter model, which is described by eq. (3.1) and where t_{BD} is the time before breakdown, A_0 is a constant relative to the substrate, γ is the acceleration factor and E_{ox} the electric field in the oxide.

$$t_{BD}(E_{ox}) = A_0 \cdot e^{-\gamma \cdot E_{ox}} \tag{3.1}$$

The devices under study are Wolfspeed C2M008012D SiC MOSFETs [152]. They are characterized (see annexe A.2) before the test, in order to verify that no DUT shows any anomaly. All the tests are run at $T_j = 150$ °C.

The results obtained from the static test are compared to those obtained from the devices placed in a DC/DC converter, working under inductive switching conditions. The objective is to study if a major degradation of the MOSFET gate oxide can occur due to hard-switching conditions.

The results of the static tests, which are shown in section 3.4.2.1, together with our desire to find and indicator of the gate oxide health (as was discussed in sec. 3.3.3), lead us to analyse the degradation phenomena further. Some additional tests are run for a better understanding of the failure mechanisms, as well as to study if the internal capacitances could be used for health monitoring applications. These tests and their results are presented in sections 3.4.1.2 and 3.4.2.2 respectively.

3.4.1 Experimental Methodology

The different tests described in sections 3.4.1.1 and 3.4.1.3 requires a previous characterization of the leakage current $I_{gs}(V_{gs})$. This allows to determine the voltage range where the Fowler-Nordheim injection phenomena is predominant, showing a linear behaviour in agreement with the thermochemical model, which allows to extrapolate the obtained results to the nominal conditions of use.

The characterization of I_{gs} requires some care: it is characterized at $T_j = 150$ °C for 10 different samples which had never been used before; using a Keithley SMU 2636B with triaxial connections, and the device is placed in a metal enclosure to achieve good sensibility to low currents (pA range). This is described in annex A.3 (see fig. A.12).

The test conditions are: V_{gs} ramping from from 20 V to 50 V, with a compliance (maximum current delivered by the source) of 100 mA. Very small steps are used (50 mV, with a delay before measurement of 1 second). These conditions are set using the control software embedded in the instrument (TSP Express).

This setting allows to minimize the measurement of capacitive currents (i_c) in agreement with eq. (3.2), where the value of C_{gs} is extracted from de component's datasheet [152].

$$i_c = C_{gs} \cdot \frac{dv}{dt} \simeq 950 \cdot 10^{-12} \cdot \frac{50 \cdot 10^{-3}}{1} = 47.5\ pA \tag{3.2}$$

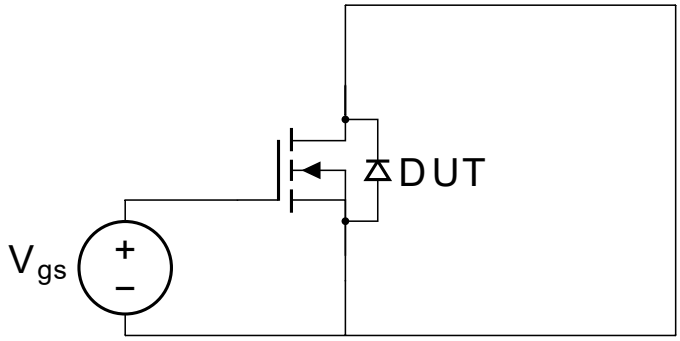


Figure 3.12 – Circuit configuration used for the static stress of the gate oxide.

Device	Samples (N)	V_{gs} (V)	V_{ds} (V)	T_j (°C)
C2M008012D[a]	7	40.5	0	150
C2M008012D[a]	7	41.5	0	150
C2M008012D[a]	7	42.5	0	150

Table 3.3 – TDDB static tests summary.

[a]Ref. W10216, year 2016.

3.4.1.1 Gate oxide lifetime estimation under static stress

A first static TDDB test is run to assess the gate oxide quality of Wolfspeed's SiC MOSFETs. The circuit diagram of this test is depicted in fig. 3.12. Three levels of stress are considered (see table 3.3).

The results of the $I_{gs}(V_{gs})$ characterization (presented in section 3.4.2), show that the final stress bias should be placed below 45 V. As the lifetime is expected to have an exponential dependence with the inverse of the applied V_{gs}, a good equilibrium must be found between test duration and the distribution of the biasing conditions. The chosen test conditions are summarized in table 3.3.

The oxide lifetimes measured with these tests allows to estimate the actual oxide lifetime at the maximum allowed V_{gs} (25 V [152]), in agreement with the thermochemical model which is described by eq. (3.1). It is noticeable that I_{gs} is monitored regularly and that the condition $I_{gs} > 1\ mA$ is adopted to determine device failure. Further details about the monitoring system are given in section 3.4.1.2, where I_{gs} evolution and failure are analysed.

3.4.1.2 Evolution of the gate oxide behaviour during static stress

In this section, we focus on what occurs during the gate oxide stress, as well as on how failure appears. Indeed, during the static tests, some peculiarities in the I_{gs} evolution attracted our attention.

As explained earlier, the current I_{gs} is monitored during the static tests. The monitoring system allows to set the sampling period (t_s) which normally is set to 60 seconds. The system, which is detailed in annex A.3, realizes all measurements and communications between the SMU and the PC, saving all the data through a Labview application.

Device	Samples (N)	V_{gs} (V)	V_{ds} (V)	T_j (°C)
C2M008012D[a]	1	41.5	0	150
C2M008012D[a]	1	42	0	150
C2M008012D[a]	1	42.5	0	150
C2M008012D[a]	1	43	0	150
C2M008012D[a]	1	43.5	0	150

Table 3.4 – Tests realized to compare I_{gs} evolution depending on the applied V_{gs}.

[a]Ref. W10216, year 2016.

After the first tests, an initial increase of the leakage current is observed. Thus, the Labview programme is modified in order to incorporate the possibility to acquire data at a much higher rate. The objective is to study the initial behaviour of I_{gs}.

To avoid bottleneck due to the communication between the PC and the SMU, the new routine allows to program the SMU in order to perform rapid bursts of measurements (up tp t_s=0.2 s in High-Accuracy acquisition mode [167]) saving the data into the internal SMU memory. Once a determined number of measurements has been realized (about 1000 points), all measured data is sent to the PC. After that, the Labview program continues to measure the current I_{gs}, but with the slow mode where t_s is setted to 60 s (as performing measurements at high time rate would result in very large amount of data).

To study the evolution of I_{gs} during the first phases of the stress, five devices are tested at different gate-source voltages. These tests are summarized in table 3.4. Moreover, as these tests are run until the oxide failure, it is possible to observe how I_{gs} evolves just before the failure and therefore if any element could predict it.

The charge injected into the oxide is calculated using the trapezoidal integration method with the aim to verify if the different devices fails for a similar amount of injected charge. Eq. (3.3) is used to calculate the total injected charge at the time of failure ($Q_{injected}$), where N is the total number of measurements before failure, and t is the stress time for each measurement.

$$Q_{injected} = \int_{t=0}^{t_{failure}} I_{gs}(t) \cdot dt \approx \sum_{k=1}^{N} \frac{I_{gs}(k-1) + I_{gs}(k)}{2} \cdot (t_k - t_{k-1}) \tag{3.3}$$

An additional test is realized using a fresh device to analyse further the evolution of its characteristics during the static test stress. Thus, the DUT is characterized initially and then repetitively (9 times over 8 hours), tacking special care in the V_{th} and the gate input capacitance C_{gs}. As discussed in section 3.3, both parameters could be linked to a possible degradation of the dielectric. For further details about C_{gs} characterization, see Annex A.2.

Once the DUT has been characterized, it is stressed at V_{gs}=42.5 V for 15 minutes and characterized again. Successive stress stages (always at 42.5 V) are realized, followed by characterization until the apparition of a dramatic failure in the oxide. The duration of the stress stages is increased gradually, because the main evolution of the parameters is observed during the first hours of stress. The current I_{gs} is monitored during all the test.

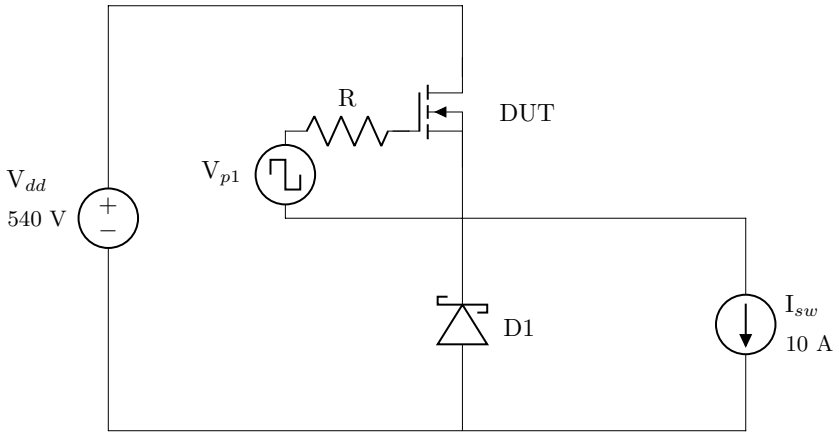


Figure 3.13 – Simplified schematic of the test-bench used for the inductive switching stress test of the gate oxide.

3.4.1.3 Gate oxide lifetime estimation for an inductive switching application

Operation conditions in a real application, such as a DC/DC converter or an inverter are very different that those experienced by the component in a static stress. One of the main differences is that the MOSFET is switching its state, allowing or preventing the current flow. At the instant where the device is switching from a state to another, some perturbations appear, both in the gate-source voltage and in the drain-source voltage. This is because the commutation is not instantaneous, but also because of the inductive nature of most circuit elements. In many actual applications, SiC MOSFETs are used to drive very inductive loads, such as motors, causing greater perturbations and favouring carrier injection phenomena. Indeed, most favourable conditions for the injection of carriers into the oxide (or in the interface SiC/SiO2) occurs when there is a cross electric field in the oxide, a current traversing the channel and a longitudinal electric field at the end of the channel (operating in the saturation region). All these conditions occurs in an inductive switching.

These perturbations could cause several undesired phenomena. The most evident examples are avalanche phenomenon in the case of a great increase in V_{ds}, or a short-circuit event in the case where V_{gs} would become high enough to turn-on an otherwise blocked transistor. Besides, both types of perturbations carrier injection phenomena in the gate oxide, which were introduced in section 1.4.1; tunnel-effect, Fowler-Nordheim and hot-carrier injection.

The gate bias values selected in section 3.4.1.1 for the static tests corresponds to the zone where the Fowler-Nordheim injection is predominant. However, in a real application, other phenomena such as hot-carrier injection could have a more relevant role (e.g. due to local heating or to inductive loads). For this reason, it is interesting to realize tests under switching operation conditions to analyse if this could have a repercussion on the oxide lifetime.

The test-bench used for this test is based on the same converter topology as that used to test the internal diode, and which is described further in annexe A.5. It can be modelled as shown in fig. 3.13, where the DUT is the high-side switch.

The DUT is placed on a hot-plate to achieve a $T_j = 150$ °C. It is driven with a duty cycle D=0.5 at 20 kHz for different V_{gs} levels. During the test I_{ds} is set to 10 A. The gate current is not monitored, and the measured lifetime corresponds to the moment when a catastrophic

Device	Samples (N)	V_{gs} (V)	V_{ds} (V)	D	T_j (°C)
C2M008012D	1	40/-8	0/540	0.5	150
C2M008012D	1	42.5/-8	0/540	0.5	150
C2M008012D	1	43.5/-8	0/540	0.5	150
C2M008012D	1	45/-8	0/540	0.5	150

Table 3.5 – Summary of TDDB tests realized in a DC/DC converter.

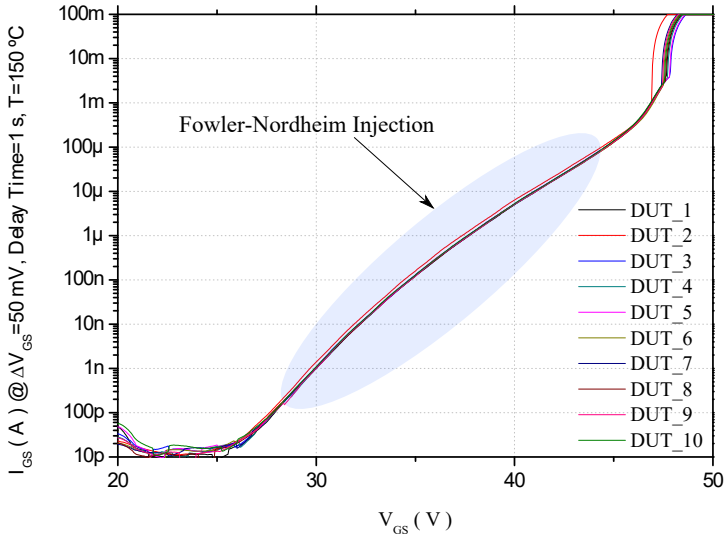


Figure 3.14 – I_{gs} (V_{gs}) characterization on 10 C2M0080120D Wolfspeed samples.

failure occurs. This is detected by a current sensor which stops a time counter when a anomalous drain-source current is measured. As a consequence, results could differ from those obtained for the static test, where a I_{gs} threshold of 1 mA is defined to determine when a device failure occurs.

Table 3.5 summarizes the different tests. The test points are defined in agreement with the characterization of $I_{gs}(V_{gs})$. Here again, the actual bias values are chosen to minimize the test time. Initial points of measure were 40, 42.5 and 45 V. Unfortunately for V_{gs}=45 V, an unexpected failure occurred after a few minutes only. Thus, an accelerating phenomenon of the gate oxide degradation appeared. As a result, it is chosen to realize a test at a lower V_{gs}, in this case 43.5 V, to avoid the apparition of other degradation phenomena in the gate oxide.

Finally, the estimation of the oxide lifetime is realized from the obtained lifetime values at 40, 42.5 and 43.5 V. This estimation is realized, as for the static tests, using the thermochemical model (eq. (3.1)) and extrapolating to the maximal conditions of utilisation (25 V [152]).

3.4.2 Experimental Results

Before to start the static set of tests, the characterization of $I_{gs}(V_{gs})$ was realized. The 10 curves obtained from the different samples are plotted in fig. 3.14. As it can be seen, above about 26 V, the current starts to increase exponentially. This behaviour corresponds to the zone where the Fowler-Nordheim injection mechanism is predominant [168, 169]. There are two noticeable considerations. First, that the initial measurements (<26 V), are in a range of

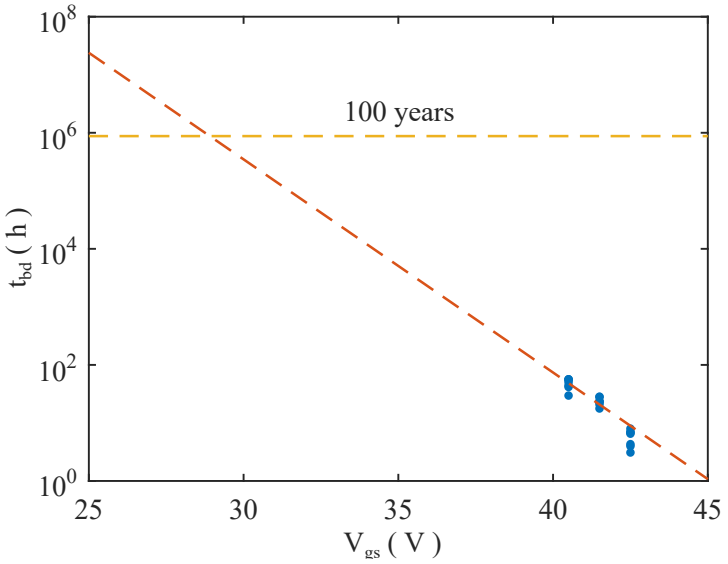


Figure 3.15 – TDDB estimation for static tests at $T_j = 150$ °C.

V_{gs} (V)	$t_{bd}(N_1)$	$t_{bd}(N_2)$	$t_{bd}(N_3)$	$t_{bd}(N_4)$	$t_{bd}(N_5)$	$t_{bd}(N_6)$	$t_{bd}(N_7)$
40.5	29.62	41.59	44.28	50.43	55.81	56.36	56.47
41.5	17.72	20.85	22.96	23.24	23.79	27.92	28.35
42.5	3.09	3.98	4.31	6.52	6.81	7.06	7.98

Table 3.6 – Measured lifetime (in hours) of the samples ($N_{1:7}$) under static stress.

current where can be highly impacted by a measurement of a capacitive current, as shown by eq. (3.2). Second, that for a V_{gs} of about 46 V, the current increases much faster and rapidly reaches the current limit of 100 mA.

This characterization contributes to the selection of the bias points used for the tests shown in this section.

3.4.2.1 Gate oxide lifetime estimation under static stress

As introduced in section 3.4.1, the chosen V_{gs} levels to realize the different oxide lifetime measurements are: V_{gs}=40.5 V, V_{gs}=41.5 $V$and V_{gs}=42.5 V. Table 3.6 summarizes the test results for all 21 samples.

In fig. 3.15, oxide lifetime is extrapolated to 25 V, in agreement with the thermochemical model described in eq. (3.1). The thermochemical model depends on the electric field in the oxide (E_{ox}), which can be estimated using eq. (3.4), where V_{FB} is the flat-band voltage, V_S is the surface potential and t_{ox} is the oxide thickness. This equation assumes a uniform field distribution.

$$E_{ox} \approx \frac{V_{GS} - V_{FB} - V_S}{t_{ox}} \tag{3.4}$$

In our case, it is also assumed that the flat-band voltage and the surface potential are negligible in order to simplify the calculation. Due to the large lifetime estimated, much higher than required for any industrial application, a further approximation of these parameters is

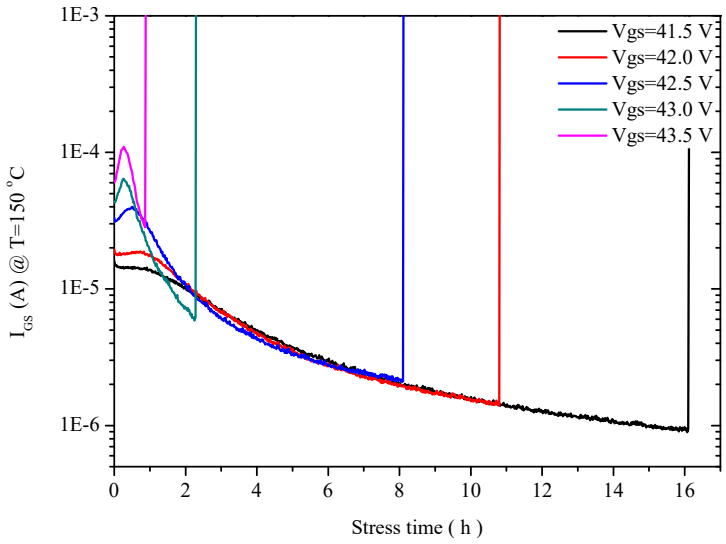


Figure 3.16 – Evolution of I_{gs} at $T_j = 150$ °C during the static tests for several V_{gs} levels.

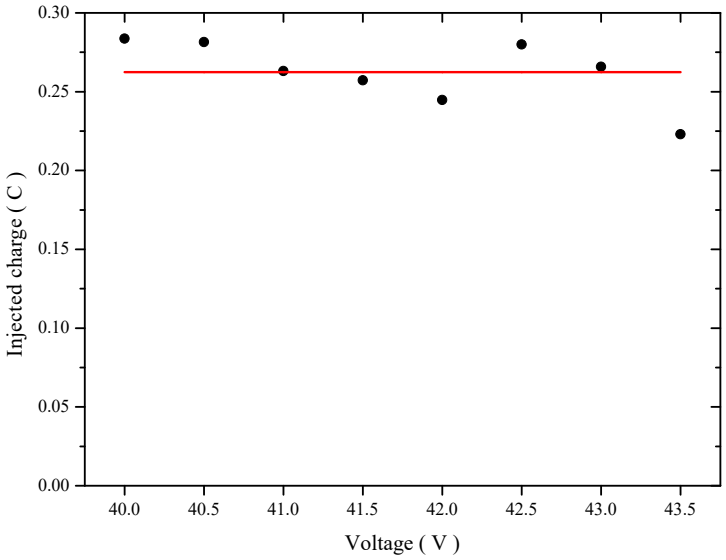


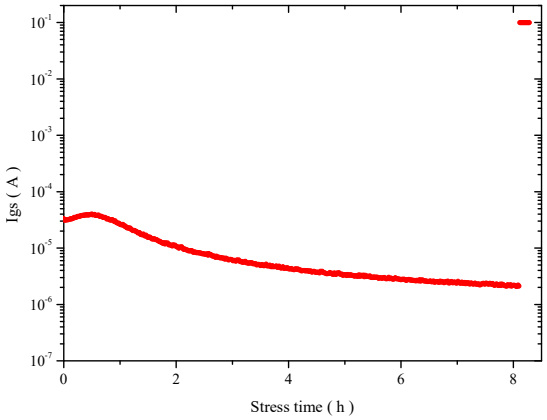
Figure 3.17 – Injected charge during the static tests for several V_{gs} levels, $T_j = 150$ °C.

not required in this case. This allows to rewrite the thermochemical model expression, as a function of the applied V_{gs}, as expressed in eq. (3.5), where $b = -\gamma/t_{ox}$.

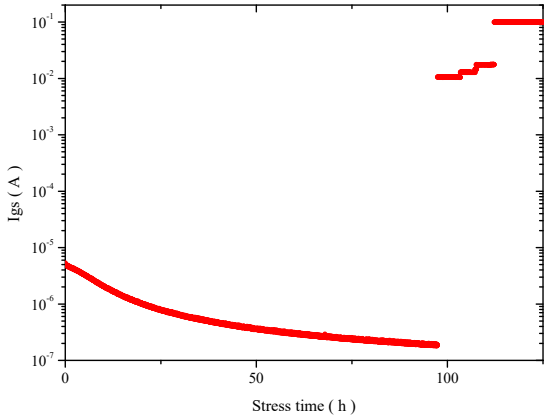
$$t_{BD}(V_{gs}) = A_0 \cdot e^{-b \cdot V_{gs}} \tag{3.5}$$

Using a least-square fitting of eq. (3.5) with the data in table 3.6 allows to estimate an oxide lifetime of $2.4 \cdot 10^7$ hours at 25 V. The parameters of eq. (3.5) are found to be:

$$A_0 = 3.646 \cdot 10^{16}\ h$$
$$b = 0.8458\ V^{-1}$$



(a) Evolution of I_{gs} during a static test at V_{gs}=42.5 V. A dramatic failure appears suddently.



(b) Evolution of I_{gs} during a static test at V_{gs}=40 V. The failure appears progressively with I_{gs} progressing by steps of a few mA.

Figure 3.18 – Comparison between the two failure types (suddent and progressive) at 150 °C.

3.4.2.2 Evolution of the gate oxide behaviour during static stress

The monitoring of I_{gs} reports some surprising results. In fig. 3.16, the evolution of this parameter is depicted for five different devices with V_{gs} ranging from 41.5 to 43.5 V. As it can be seen, for the lower voltage level (41.5 V) the current I_{gs} remains almost stable initially (about 1 hour), and then decreases logarithmically before a dramatic failure at t=16 h.

For higher voltages levels, it is noticeable that during a first phase the current increases significantly. In example, for V_{gs}=43.5 V, the current increases by about 70%. This initial increase was unexpected, and could be explained by the electrical stabilisation of the device, together with the apparition in a first time of intrinsic material defects or trapping phenomena.

After this first phase, the current starts to decrease until the sudden apparition of a failure. During this second phase, the main phenomena involved may be charge trapping, leading to a failure when a determined amount of charge is injected into the oxide. This hypothesis is supported by the literature, where it is shown that several devices fail for a similar injected charge level [170].

Using some preliminary results obtained on the static test, I_{gs} is integrated over time until the apparition of a failure for different V_{gs} levels. The obtained results are shown in fig. 3.17. As it can be seen, all devices fails for a injected amount of charge of about 0.26 C, with a maximal deviation of 15%.

Focusing at the failure instant, there are two different types of failure. Both are compared in fig. 3.18, where the current I_{gs} is monitored until failure. This corresponds to a measured I_{gs} of 100 mA because of the current limitation from the power source.

The first one, is a dramatic failure where the device becomes short-circuited between the gate and source terminals (see fig. 3.18a). However, a second failure mode is observed in some devices. This one shows gradually increase in I_{gs}, with jumps of a few mA as it can be seen in fig. 3.18b. In this case the device continues to work, despite the damage of the oxide layer (which allows a high leakage current). A higher gate-source voltage is then required to turn the device on because of the greater leakage current. This would result in an losses increase.

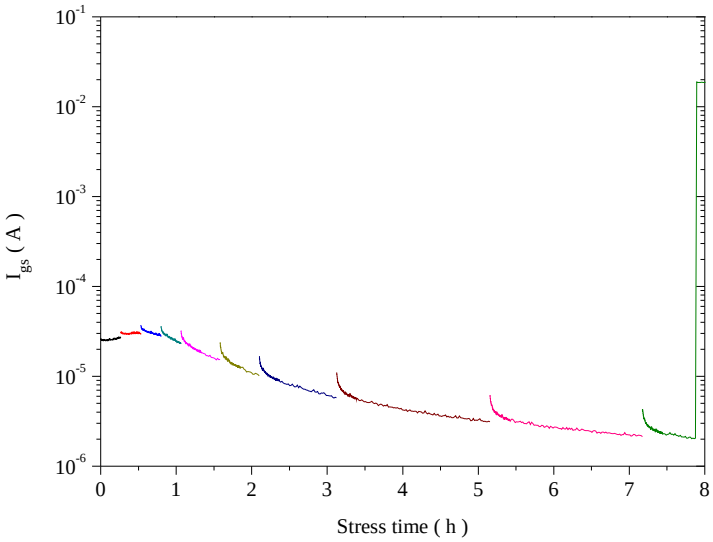


Figure 3.19 – I_{gs} measurement until failure apparition at V_{gs}=42.5 V during a static stress at $T_j = 150$ °C, which is interrupted regularly to re-characterize the device.

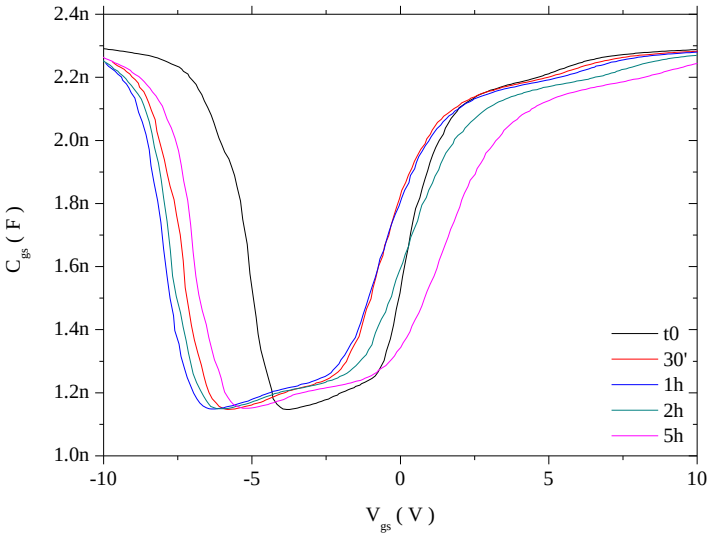


Figure 3.20 – C_{gs} evolution during the static stress at V_{gs}=42.5 V. Characterized at room temperature.

For a better understanding about what is internally happening in the device, fig. 3.19 shows the evolution of I_{gs} over time for a static stress at V_{gs}=42.5 V. This test is realized by steps, with regular (not periodical) characterization of the DUT. The device characteristics considered here are C_{gs}(Vgs), Ids(Vds), and Ids(Vgs).

The evolution of C_{gs} is shown in fig. 3.20. The curve exhibits a significant drift, moving towards the left during the first hour of stress. Moreover, a great increase of the depletion region width is observed. After that, the drift changes in direction, moving towards the right side (greater gate-source values). This move to the right side is especially noticeable for the inversion region, whereas the accumulation region remains more stable, and the width of the depletion region continues to increase. These translations of the C_{gs} curves are consistent with the initial behaviour of the I_{gs} current, as it is discussed later in section 3.4.3.

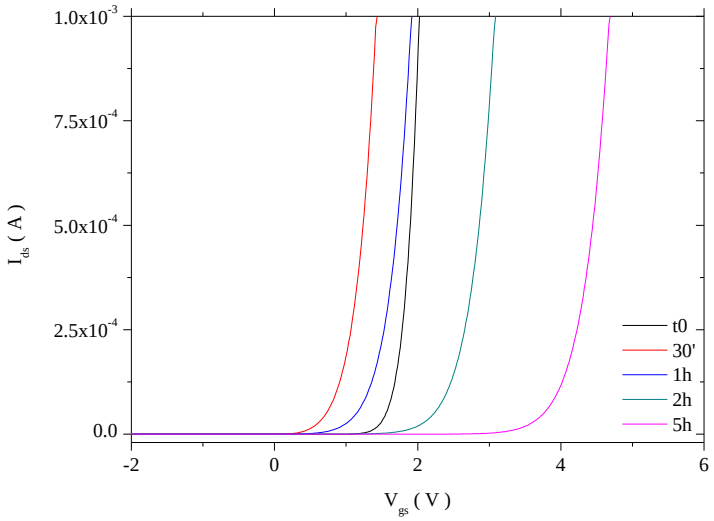


Figure 3.21 – $I_{ds} - V_{gs}$ evolution during the static stress at V_{gs}=42.5 V. Characterized at room temperature and V_{ds}=1 V.

The observed evolution of the C_{gs} capacitance is also consistent with the evolution of $I_{ds}(V_{gs})$, which is shown in fig. 3.21. Indeed, looking at the inversion region in fig. 3.20, for the first two measurements (30' and 1 hour) there is a translation to the left side which is also observed for the curves $I_{ds}(V_{gs})$, thus in the V_{th}. However, from fig. 3.20 it can be observed that the inversion regions shapes in these two cases are almost superposed, which should result in very similar $I_{ds}(V_{gs})$ characteristics, but it is not the case. The other two $I_{ds}(V_{gs})$ measurements (after 2 and 5 hours), shows a translation to the right side, reaching higher values than the initial measurement, as expected in agreement with C_{gs}.

3.4.2.3 Gate oxide lifetime estimation for an inductive switching application

In the case where the DUT is placed in a DC/DC converter with a high inductive load, the test is repeated for four different operating points. The corresponding lifetimes, are summarized in table 3.7. As introduced earlier, the test realized at V_{gs}=45 V resulted in a much faster failure than expected. It could be because this voltage is close to the zone where the behaviour of I_{gs} starts to change (see fig. 3.14). Thus, this point is discarded and the estimation of the oxide lifetime at 25 V is realized using the results obtained from the remaining three points. It is noticeable, that the oxide lifetime (t_{bd}) results shown in table 3.7, are the total time elapsed before failure. Thus, as a duty cycle D=0.5 is applied during the test, the dielectric layers were actually exposed to a high voltage stress for only half of this time. Hence, on the following calculations and graphics t_{bd} is divided by 2.

To estimate the oxide lifetime at 25 V, the calculus are analogue to those realized in section 3.4.2.1. The oxide lifetime estimation depending on V_{gs} is plotted in fig. 3.22, and the corresponding parameters are:

$$A_0 = 2.046 \cdot 10^{13}\ h$$
$$b = 0.6219\ V^{-1}$$

V_{gs} (V)	40/-8	42.5/-8	43.5/-8	45/-8
t_{bd} (h)	642.8	130.8	79.4	0.1

Table 3.7 – Measured oxide lifetime (in hours) for the tests realized in a DC/DC converter with a duty cycle D=0.5.

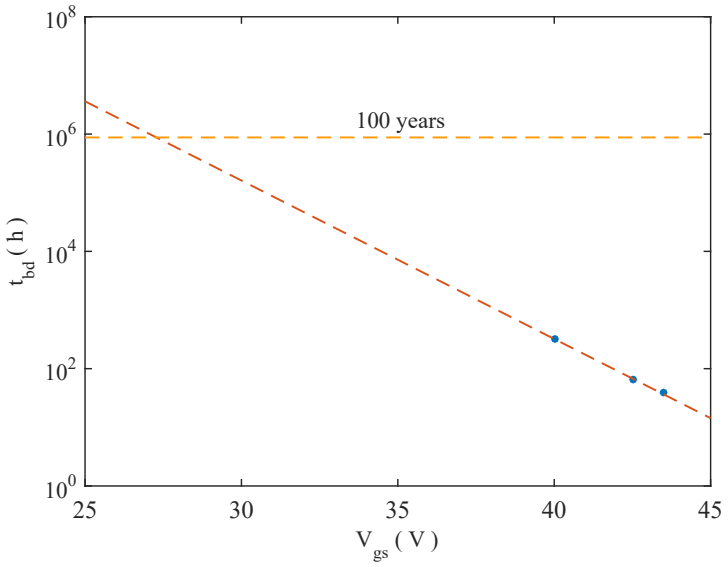


Figure 3.22 – TDDB estimation for a SiC MOSFET placed in a DC/DC converter at $T_j = 150$ °C.

This allows to estimate an oxide lifetime of $3.6 \cdot 10^6$ hours at 25 V. Obviously, additional tests would be required in order to give a confident estimation for the oxide lifetime. However, in this case the aim is to evaluate it there is a remarkable difference between a static test and a more realistic one. In both cases, the obtained dielectric lifetime is very high (more than 100 years). Thus it is considered unnecessary to continue this test which requires a high amount of time and human resources.

3.4.3 Discussion

The different TDDB tests, both in static stress and for devices placed in a real converter, have reported an expected oxide lifetime well above 100 years. A comparison among the expected lifetime obtained from the different tests (static and under inductive switching) and the data provided by the manufacturer is shown in fig. 3.23.

Results obtained when the device is placed in a converter, driving a high inductive load, shows an expected lifetime about 6.6 times lower than that reported by the static tests ($3.6 \cdot 10^6$ *vs* $2.4 \cdot 10^7$ hours). However, as in both cases the expected oxide lifetime is much greater than what could be required for any application, the tests are stopped due to the high human resources and time that they required.

Nevertheless, with only 3 samples it is not possible to determine if inductive switching conditions could impact the oxide lifetime, and additional tests would be required to verify whether the difference in lifetime between static and switching test is significant. At the moment, all we can conclude (and it was the objective of these tests) is that switching operation

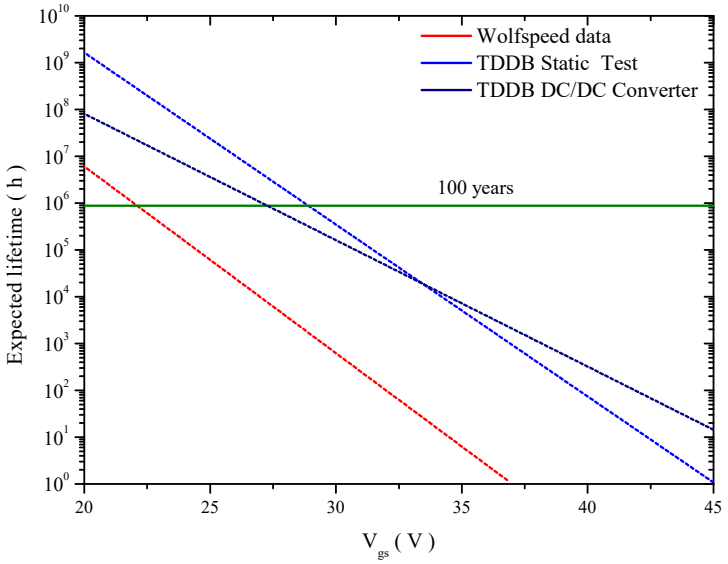


Figure 3.23 – Expected lifetimes depending on V_{gs}. Comparison between Wolfspeed data and the experimental data (obtained from inductive commutation tests as well as static tests.

does not have such a radical effect in oxide lifetime that it would become a problem in real applications.

From an industrial point of view, this issue could only become relevant if the oxide thickness of the SiC MOSFETs is reduced further or if these devices are used at high temperature, reducing the expected oxide lifetime.

However, the surprising behaviour of the leakage current I_{gs} during the static tests, has attired our attention. Indeed, an initial increase in the gate current is observed when a high electric field is applied to the oxide. This is followed by a decrease until failure occurs. This failure can result in a short-circuit between gate and source terminals or an increase in the I_{gs} by some mA.

To understand the initial evolution of this leakage current, a C(V) analyse of C_{gs} revealed an initial drift of this capacitance towards lower voltages. This is usually associated with the injection and trapping of positive charges into the oxide or near the SiC/SiO_2 interface or ion-diffussion phenomena [115, 119]. As an hypothesis, this can be associated with substrate contamination or ionic ions such as H^+, which as in the case of SOFC (Solid Oxide Fuel Cell) [171] could move through the oxide in some cases. A similar phenomenon involving H^+ migration was reported by *Gale et al.* in 1983 [172] in Silicon MOS capacitors.

As the number of ions at the interface is limited (because they are related to the manufacturing process), this phenomena would gradually slow down hence the reduction in leakage current over time. The I_{gs} current decreases and the C_{gs}(V) characteristics shifts towards higher voltages could then be associated with carrier injection phenomena and trapping, introducing negative charges into the oxide or near the interface.

These phenomena, could induce the apparition of conductive paths in the oxide layer due to ions displacement and/or to the breakage of molecular bonds [173]. In the case of a conductive path running throughout all the oxide, this could lead to a dramatic failure of the oxide.

3.5 Conclusions

The objective of this chapter is the study the robustness of the gate dielectric (SiO_2) and to verify if its expected lifetime is in agreement with the industry requirements. The study is focused on two main measurements of the gate oxide degradation: BTI and TDDB.

For BTI, it has been verified in agreement with [160], that the most stressful configuration is when drain and source terminals are short-circuited, and a positive V_{gs} (close to the maximum value) is applied. This configuration corresponds to the classic HTGB test. For this case, firsts BTIs appears at about 170-180 °C (for V_{gs}=22 V).

Tests realized on Wolfspeed MOSFETs at 150 °C have shown no significant BTIs over 1000 hours of stress, with a maximal increase in the V_{th} of 5%. However, the tests realized at 200 °C (V_{gs}=22 V), have shown a great increase in the V_{th}. In both cases, the I_{gs} current remained stable. Thus, it is not a good indicator of BTIs, even if its monitoring could be required regarding other undesired phenomena such as short-circuit [162].

Finally, regarding BTIs, it is noticeable that Wolfspeed MOSFETs are found to be the most sensitive to this phenomena, whereas ROHM and ST SiC MOSFETs do not show a significant degradation, with a V_{th} increase of about 12% over 1000 hours, without showing a clear tend. As for Wolfspeed MOSFETs, the leakage I_{gs} current has not been found to be an indicative parameter of the oxide degradation.

With TDDB tests, the expected oxide lifetime has been found to be well above 100 years in the two cases under study: under static stress ($3.6 \cdot 10^6$ hours)and when the device is placed in a real converter driving an inductive load ($2.4 \cdot 10^7$ hours). In this latter case, only three samples have been stressed. While this small sample size is too small to allow for an accurate comparison with the static tests, it is sufficient to demonstrate that oxide lifetime should not be an issue in real operating cases.

The most significant issue related to the TDDB is the observed mode of failure, where the current I_{gs} shows a great increase, leading to a dramatic failure (gate-source short-circuit) or increasing to some mA. In this last case, the device is still capable to work, even if the loses should increase notably. Regarding the behaviour of I_{gs} and the capacitance C_{gs}, our conclusion is that during the tests two phenomena are involved. A first one which would be predominant at the beginning (at least when high electric field is applied to the oxide) moving positive charges into the oxide or in the interface. This phenomena could be related to the presence of contamination or ionic ions, such as H^+. After that, another phenomena becomes predominant, moving negative charges into/near the oxide. This phenomena might be related to carrier injection and trapping.

It is concluded that the SiC MOSFETs show a good robustness of the gate oxide, allowing their use for industrial applications at temperatures of T_j = 150 °C. Nevertheless, before exploring their use in high temperature applications, some issues should be addressed. This is the case of BTI apparition for temperatures above 170 °C (Wolfspeed) or the presence of mobile ions in/near the interface. These two issues are probably related.

Conclusions

In this thesis, the main robustness issues concerning SiC MOSFETs have been studied. Contrary to some years ago, where the main problems concerned SiC epitaxy, today the main issues focus on device characteristics and their robustness in different operation modes.

In this thesis, two different issues have been addressed on 1200 V SiC MOSFETs:

Intrinsic diode degradation, which may be due to the presence of SFs inducing a shift of the diode forward voltage (V_f).

Gate oxide reliability, which can be divided in two different aspects:

1. Oxide or dielectric expected lifetime (estimated by TDDB test).
2. Threshold voltage (V_{th}) drift (evaluated by BTI tests).

Other aspects concerning the robustness of SiC MOSFETs are linked to the operation mode of the devices, such as the occurrence of short-circuit or avalanche events. These issues are not been addressed in this thesis because they were studied in the same project by a complementary thesis [133].

The robustness of the intrinsic diode has been addressed in chapter 2 with the objective to validate if SiC MOSFETs could be used for diode-less applications (e.g. in an inverter). In this kind of applications, the internal diode is typically solicited during the dead-times. In this way, tests have been addressed in static mode, but also placing the DUT in an inductive switching converter (which are the most stressful conditions of operation).

In both cases, no significant drift of the V_f has been observed. This matches with recent publications of the manufacturers indicating an important reduction of the SFs and BDP defects in the substrates [158, 159].

However, with a current stress of the internal diode, an important V_{th} drift appears in some cases. This could probably be related to carrier injection phenomena and trapping at the SiO_2/SiC interface, or in the oxide. This drift of the V_{th} appears in both modes of operation (static and in a converter). Moreover, for the same gate-source voltage (i.e. $V_{gs} = -8\ V$), this drift is very similar in both cases. For lower gate-source potentials, the V_{th} drift is drastically minimized (i.e. $V_{gs} = -5\ V$). Thus, this V_{th} drift depends of the applied gate-source potential, or as some tests introduced, on the duty cycle (by de-trapping phenomenon).

Complementary tests, stressing the channel instead of the body diode for $V_{gs} = 20\ V$ the same temperature (150 °C) and dissipated power than for the third quadrant tests, does not results in significant V_{th} drift.

Thus, a significant V_{th} drift only appears (at 150 °C) in the case where the P-N junction is stressed (in HTGB tests, a V_{th} drift is observed at higher temperatures). Then, the accumulation regime could favour this degradation of the V_{th} (only observed for Wolfspeed devices).

To observe a V_{th} drift (at 150 °C), even in accumulation regime, a stress of the P-N junction is required. An hypothesis that we can formulate is that due to the significant amount of power dissipated in the device during the test, an important temperature gradient appears between the drift region an the top of the device, favouring hole injection in the oxide or near the interface SiC/SiO_2 and resulting in a V_{th} drift. To validate this hypothesis, thermal and electric simulations of the device are required.

It is necessary to note that these results are obtained for Wolfspeed MOSFETs. ST and ROHM devices have also been also tested (only placed in the converter test-bench). Devices from these manufacturers do not exhibit any significant degradation of the V_f, nor in the V_{th} for the same conditions of operation.

Thus, the utilisation of the internal diode for diode-less applications is possible with the actual technology. In the case of Wolfspeed SiC MOSFETs, it should be possible taking some precautions regarding the V_{th} drift and spurious turn-on of the device. Indeed, even if Wolfspeed MOSFETs show a significant drift of the V_{th} in some tests, in a real application the P-N junction is only solicited during a small fraction of the overall period. This fact, together with the slight drift observed in more realistic cases ($0.05 <$ duty cycle < 0.85) seem to validate their utilisation for industrial applications.

Regarding gate oxide robustness, the different test realized in chapter 3 indicate that expected lifetime (TDDB measurement) is no longer a main issue for SiC MOSFETs. TDDB measurements are realised. One in static mode, applying a gate-source voltage high enough to accelerate the oxide degradations. Another one, placing the devices in a real converter to stress further the device. The obtained oxide lifetime from our tests is higher than that provided by the manufacturer (x10) [161], which assures 10 years at 25 V, and well above 100 years at $V_{gs} = 20\ V$, which is the recommended V_{gs}.

BTIs probably remains as main robustness issue for SiC MOSFETs. HTGB test in Wolfspeed MOSFETs resulted in the apparition of V_{th} drift after some hours about 170-180 °C and V_{gs}=22 V. This instability is not significant for ROHM and ST MOSFETs, even at 200 °C. Contrary what we expected, I_{gs} current is not found to be an indicative parameter of this V_{th} drift, as measurement results in similar values during overall the test, whereas the V_{th} drift (positive) could be about 30% after 1000 hours (test conditions V_{gs}=22 V at 200 °C).

With the aim to evaluate the behaviour of the oxide and trapping injection phenomena which may occur, the I_{gs} current has been monitored during some TDDB tests. From these tests we observed two surprising phenomena.

1. A great and progressive increase of the I_{gs} current during the first minutes of the TDDB test.

2. In some cases, device resulted in partial failure(s), with currents around some mA and increasing progressively by current steps.

With a further study, stopping TDDB test and characterizing the gate-source capacitance regularly, it is observed that the C(V) characteristics shift to the left side during the phase where the I_{gs} current increases and to the right side when it starts to decrease. An hypothesis

that could explain this phenomena is that the injection of positive charges in the oxide or in the interface during a first time. These positive charges could be mobile ions such as H^+. As the number of this type of charges is limited (they are associated to the manufacturing process), once they are moved the current starts to decrease (as initially expected). In this second time, the main phenomena may be associated to carrier injection electrons and trapping.

In the case that ions would diffuse into the oxide, due to their size it could result in a great increase of the leakage current (as leakage current steps observed during the tests). However, it is not possible to explain if these current steps should be related to a perforation through all the oxide layer, which becomes larger, or perhaps to multiples and locate degradations of the oxide resulting in a local thinner layer.

Regarding industrial applications, gate robustness is no longer an impediment. The only degradations observed in this thesis regards Wolfspeed MOSFETs operating well above 150 °C. ST and ROHM MOSFETs do not shows important V_{th} drifts (about 12% at 200 °C over 1000 hours). However, it seems obvious that before to explore the use of SiC MOSFETs in high temperature applications, further studies should be carried out.

In GENOME project, it has also been studied by *M. Cheng* [133] the robustness of SiC MOSFETs under short-circuit and/or avalanche conditions. It is concluded that SiC MOSFETs are very vulnerable in these operation modes. Thus, it is required to evaluate if the protection systems used until now for silicon MOSFETs are adapted to SiC devices or if it is required to redesign them for a faster protection.

Future Work

As the results obtained in this thesis highlight that the robustness issues regarding the internal diode have been overcome, future work should focus in the gate oxide robustness. The main issues for power electronics applications are the following:

- **Apparition of BTI during forward current stress of the intrinsic diode.** This type of degradation requires some complementary investigations and tests. This involves developing a thermal and electrical model of the device to evaluate the apparition of temperature gradients during a stress of the internal diode. Some tests should quickly indicate if this V_{th} drift is associated with the apparition of temperature gradients in the device structure. Among them, tests stressing the internal diode at different currents levels and temperatures, and eventually a set of tests applying different duty cycles in the case of CMB tests (a larger experiment set). To study this issue further, the identification of the defects causing this degradation of the V_{th} could be studied by techniques such as DLTS and reproduced by simulation tools.

- **BTIs at higher temperatures.** This requires, as above, the improvement of the gate oxide quality and of the SiC/SiO_2 interface. HTGB test will continue to be required to evaluate the new generation of devices for temperatures above 200 °C. Today (as reported in this thesis), 1200 V MOSFETs can operate without the apparition[2] of significant instabilities in the threshold voltage up to 170 °C.

- **Evaluation of the impact of short-circuit and avalanche events in the expected lifetime.** In this thesis, the TDDB tests resulted in great expected lifetime for 1200 V SiC devices (>100 years; in static mode, or under conditions of inductive switching). However, the apparition of some operation modes such as short-circuit or avalanche is very stressful for the devices because of the high power dissipated, causing great temperature increase in the device and accelerating their degradation. Many applications incorporate protection systems for these operation modes, but they are based on the "know-how" accumulated from silicon devices. Thus, TDDB tests should be carried on SiC devices stressed repetitively in these modes of operation. Results should be compared with the duration of the stress events, in order to evaluate the corresponding gate oxide degradation and to supply data for the design of protection systems.

[2] Except for the case where the internal diode is stressed.

Appendix A

ANNEXES

Contents

A.1 Main Bias Tests

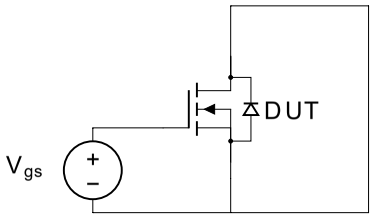
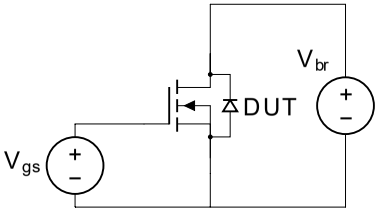
Acronym	Test full name	Test Conditions	Performed here?	Schema
HTGB	High Temperature Gate Bias	$T = T_{max}$ $V_{gs} = +V_{gs_{max}} / -V_{gs_{min}}$ V_{gs} cst V_{ds} undefined	Yes, see ch.3	
HTRB	High Temperature Reverse Bias	$T = T_{max}$ $V_{gs_{min}} < V_{gs} < 0\ V$ $V_{ds} = V_{br}$ or near	Yes, see ch.2 and 3	

Table A.1 – JEDEC tests used on gate bias and voltage threshold instability.

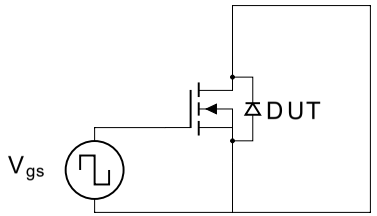
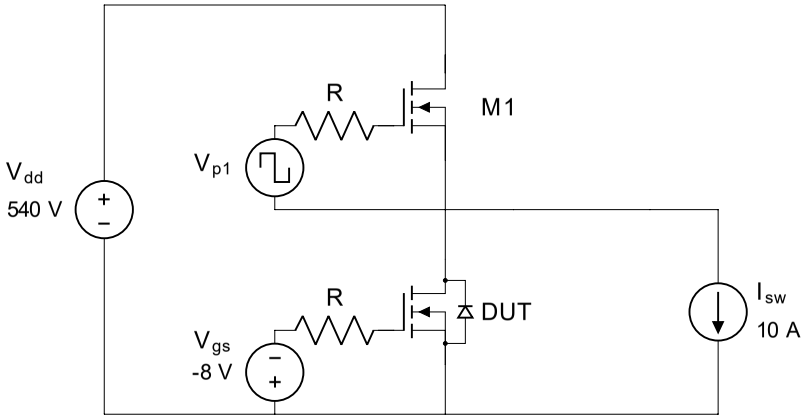
Acronym	Test full name	Test Conditions	Performed here?	Schema
HTGS	High Temperature Gate Switching	$T_{amb} = T_{max}$ $V_{gs} = +V_{gs_{max}} / -V_{gs_{min}}$ or near Pulsed excitation Frequence and Duty Cycle no explicitly defined $V_{ds} = 0\ V$	No	
CMB	Chopper Mode Bias	$T = T_{max}$ $V_{gs} = -8\ V$ $V_{ds} = 540\ V$ $f = 20\ kHz$ $D = 0.5$	Yes, see ch.2	

Table A.2 – Non-standard tests used on gate bias and voltage threshold instability.

A.2 Device Characterization

In this work, five different parameters are characterized in order to evaluate if there is any degradation of the power device. These four parameters are the following:

- Drain-source current vs drain-source voltage $I_{ds} - V_{ds}$.
- Diode forward voltage $V_f - I_{ds}$
- Threshold Voltage V_{th}
- Gate-source capacitance C_{gs}
- Gate-source leakage current I_{gs}

To realize the characterization of the first three parameters, a power device curve tracer Keysight B1505B is used. To measure C_{gs}, a Keysight B1506A curve tracer is used. Details about characterizations and some recommendations are given below. Moreover, an entire appendix is dedicated to the measurement of the leakage current I_{gs} (see. Appendix A.3).

Fig. A.1 shows the connection box used to characterize $I_{ds} - V_{ds}$, V_f and V_{th} with the B1505B curve tracer. As it can be observed, the measurement is realized with 4-wire connexions. However, this 4-wire configuration is maintained up to the ceramic connexion block (the white block in fig. A.1) only. Thus, the realized measurements are sensitive to phenomenon such as the oxidation of the leads of DUT, which could cause a R_{ds} change.

Nevertheless, this is not the only error which could impact the characterizations. One of the most common errors is related to self-heating phenomenon. Indeed, if the characterization setup is not properly defined, it can induce to measurement errors due to the increase in the device temperature. This could be especially important when the device is operating in the saturation

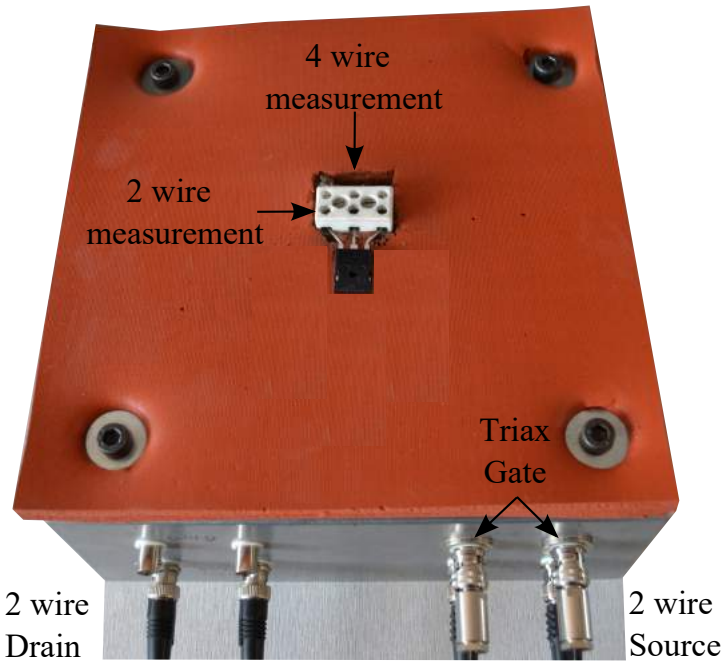


Figure A.1 – Connection box used for the characterization of $I_{ds} - V_{ds}$, V_f and V_{th} curves.

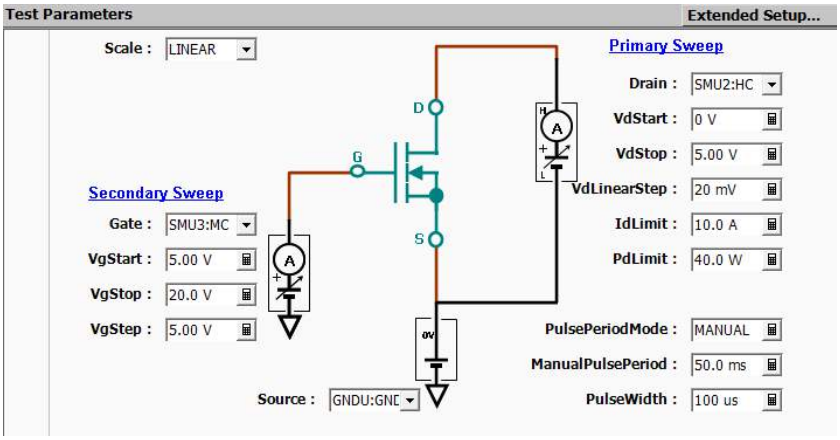


Figure A.2 – Setup used for the measurement of $I_{ds} - V_{ds}$ characteristics.

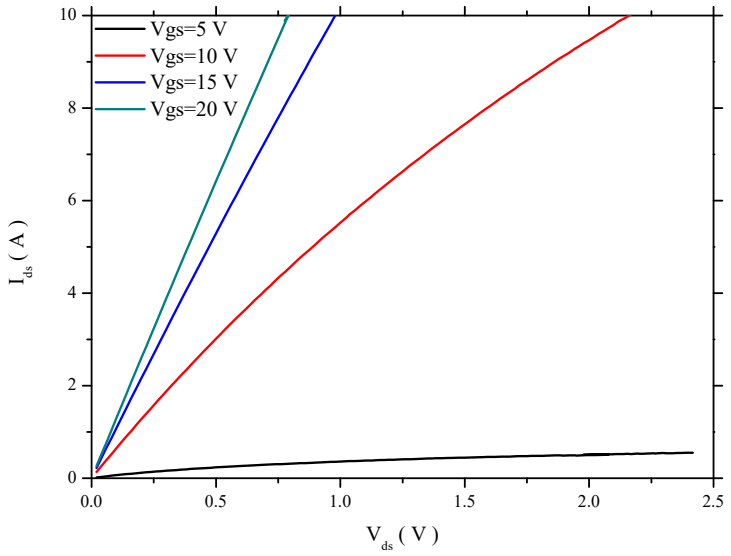


Figure A.3 – Typical $I_{ds} - V_{ds}$ characteristic curves of a SiC MOSFET for different gate-source voltages.

region. For this reason, the characterization program proposed with the curve tracer requires a duty cycle lower than 1%. This duty cycle is related to the pulse time over the pulse period (parameters located on the low side of picture A.2 at right). Anyway, this does not warranties that self-heating will not occur, and it is recommendable to realize some preliminary repetitive measurements tests to define measurement protocols.

Drain-source I-V $I_{ds} - V_{ds}$

Fig A.2 shows the chosen parameters for $I_{ds} - V_{ds}$ characterization. To minimize a possible self-heating of the device, time between measures is set to 50 ms, with a measurement pulse width of 100 μs. This is duty cycle of 0.2%. Characterization is realized at four different gate-source voltage, starting at $V_{gs} = 5\ V$ up to $V_{gs} = 20\ V$ by steps of 5 V. Drain current has been limited to 10 A. Obtained curves are plotted on fig. A.3.

From this characterization, it is possible to obtain the internal on-resistance R_{ds} of the power

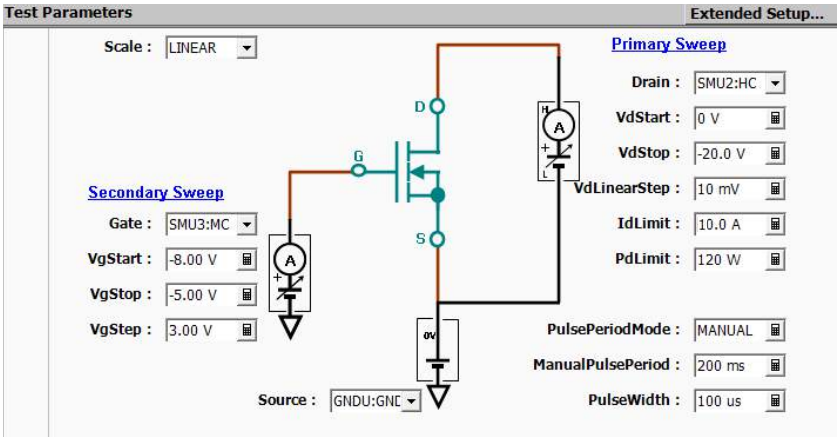


Figure A.4 – Setup used for the measurement of V_f-I_{ds}.

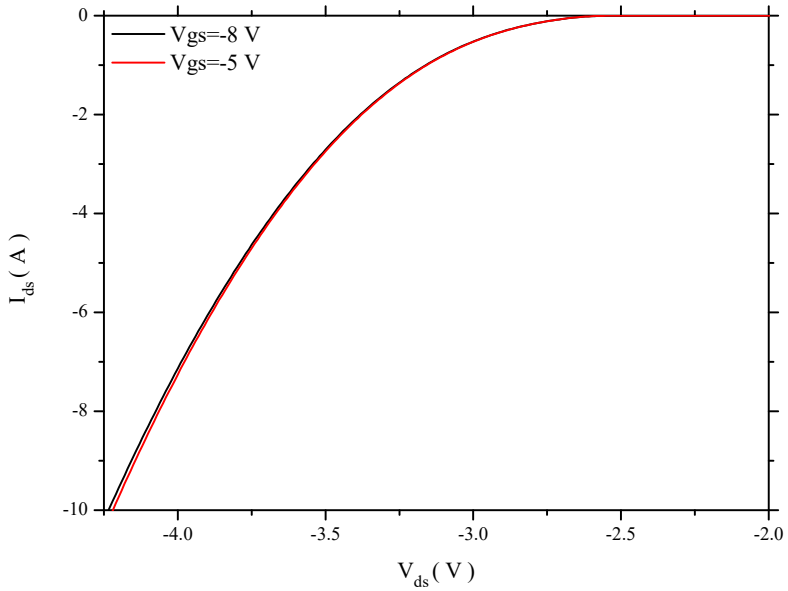


Figure A.5 – Typical V_f (-V_{ds}) characteristic of a SiC MOSFET for different gate-source voltages.

device for a given operation point (V_{gs}, I_{ds}).

Diode forward voltage V_f−I_{ds}

The diode forward voltage and $I_{ds} - V_{ds}$ characteristics are similar, with the difference that the device channel is blocked. Thus, for a negative value of V_{ds} the current flows through the internal diode. The characterization setup is shown in fig. A.4, and obtained curves are plotted in fig. A.5.

As operating voltage drop on the internal P-N junction is much higher on SiC MOSFETs than on Si MOSFETs and to avoid self-heating, the applied duty cycle is reduced to 0.05% (time between measures is setted to 200 ms, with a measurement pulse of 100 μs). Characterizations are realized at $V_{gs} = -8\ V$ and $V_{gs} = -5\ V$. Applied V_{ds} starts at 0 V and decreases until reaching a diode forward current I_f=10 A.

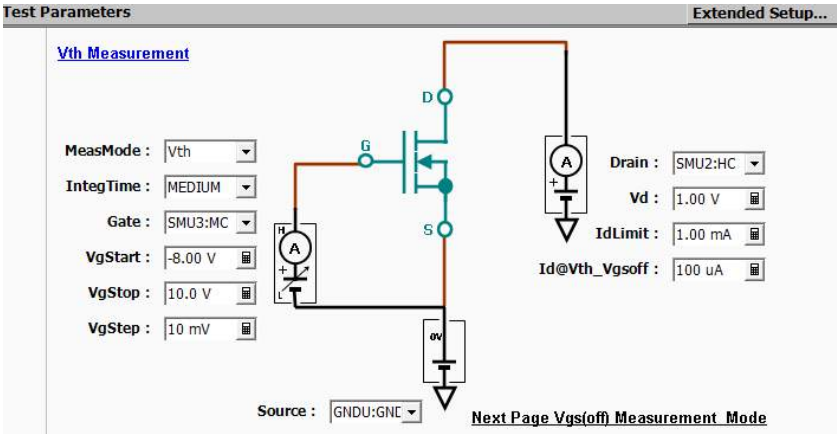
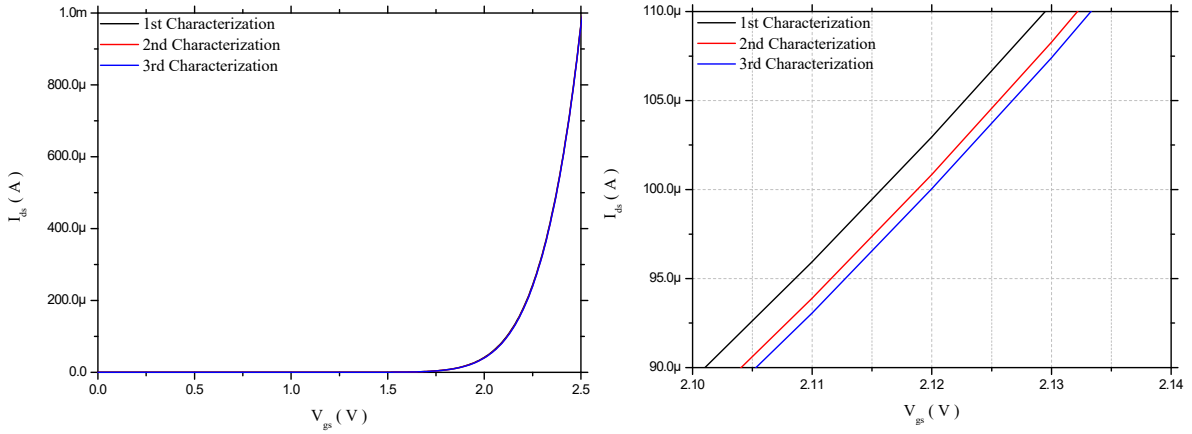


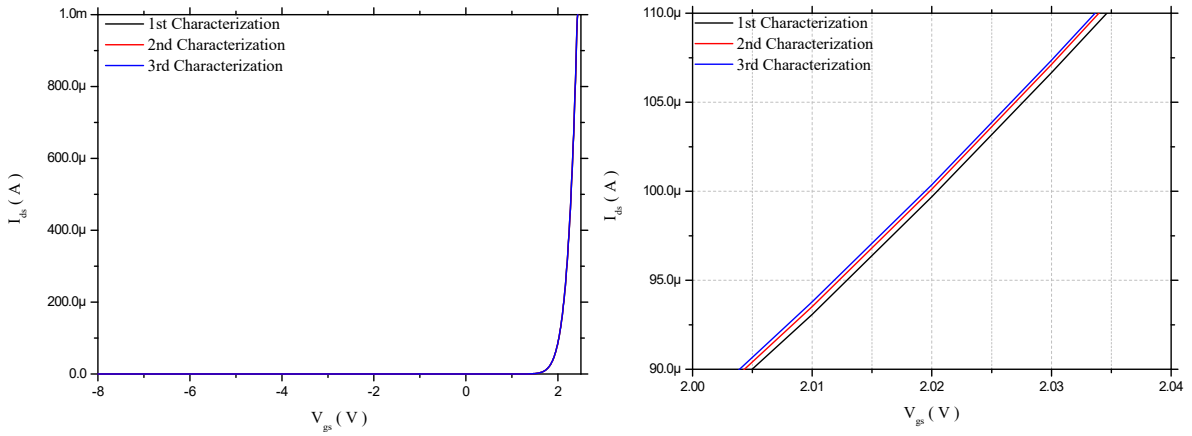
Figure A.6 – Setup used for the measurement of V_{th}.



(a) I_{ds}–V_{gs} characteristics curve for a V_{gs} starting at 0 V.

(b) Zoom of $I_{ds} - V_{gs}$, around the point of V_{th} measurement ($I_{ds} = 100\ \mu A$).

Figure A.7 – $I_{ds} - V_{gs}$ characterization of a SiC MOSFET. Initial V_{gs}=0 V, $V_{ds} = 1\ V$, V_{th} measured at 100 μA. Three successive measures have been realized.



(a) I_{ds}–V_{gs} characteristics curve for a V_{gs} starting at -8 V.

(b) Zoom of $I_{ds} - V_{gs}$, around the point of V_{th} measurement ($I_{ds} = 100\ \mu A$).

Figure A.8 – $I_{ds} - V_{gs}$ characterization of a SiC MOSFET. Initial V_{gs}=-8 V, $V_{ds} = 1\ V$, V_{th} measured at 100 μA. Three successive measures have been realized.

Threshold voltage V_{th}

From the $I_{ds} - V_{gs}$ characteristic, it is possible to determine the voltage threshold, which is measured for a given I_{ds} current. This current level is fixed arbitrarily and in this work V_{th} is measured at I_{ds}=100 μA for a constant drain-source voltage V_{ds}=1 V.

The corresponding configuration is showed in fig. A.6. As it can be seen, the characterization starts for a $V_{gs} = -8\ V$. Even if it could seems unnecessary, it has consequences on the final result.

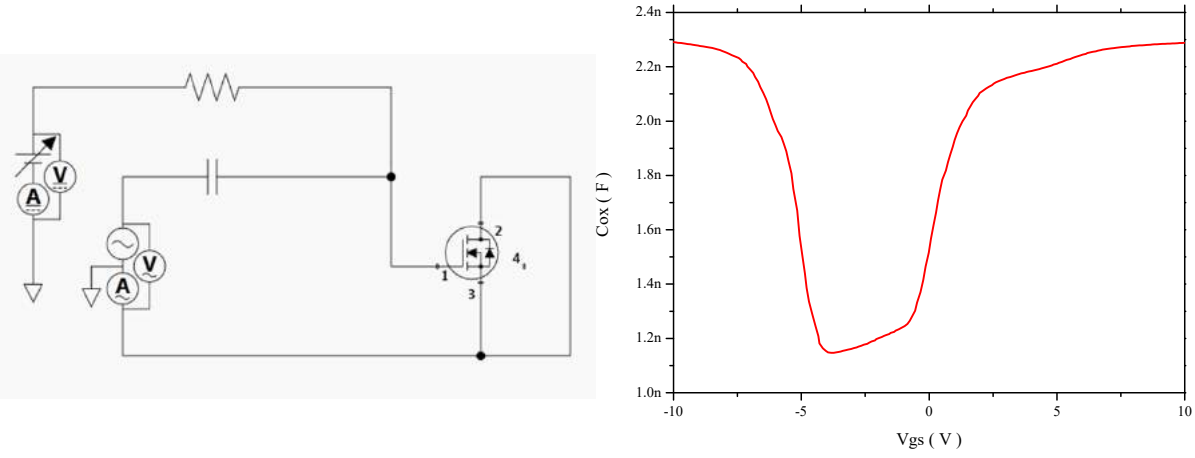
Fig. A.7a shows a typical $I_{ds} - V_{gs}$ curve for an initial V_{gs}=0 V. Zooming near the point where I_{ds}=100 μA it can be seen that over three successive measures, the resulting V_{th} differs by about 5 mV and that the $I_{ds} - V_{gs}$ characteristics is moving towards the right side. In this case, V_{th} should be between 2.115 V and 2.12 V.

In the case of a characterization of $I_{ds} - V_{gs}$ (same device) starting at $V_{gs} = -8\ V$ (see fig. A.8), it can be seen that I_{ds} starts to increase earlier. Moreover, successive measures are much repeatable (fig. A.8b), even if one can observe some left-side drift.

The protocol used to measure V_{th} starts by applying $V_{gs} = -8\ V$ (for Wolfspeed and ST MOSFETs; for ROHM MOSFETs it starts to $V_{gs} = -5\ V$). This blocking voltage, $V_{gs} = -8\ V$, has been chosen because it leads to a more repetitive characterization. In our case, the same characterization procedure is repeated over the duration of the ageing tests, therefore a repeatable measurement is more important than absolute values.

Capacitance C_{gs}

An example of C_{gs} characteristic acquired for a Wolfspeed C2M0080120D MOSFET is shown in fig. A.9.The measurement of the gate-source capacitance (C_{gs}) is realized in agreement with the figure A.10 (Keysight calls C_{gs} as C_{ox}). The AC voltage component is setted to a frequency of 100 kHz and 25 mV in amplitude. The measurements are realized for gate-source voltages



(a) (b)

Figure A.9 – Measurement schema for C_{gs}(fig. A.10) and C_{gs} measurement of a Wolfspeed SiC MOSFET (fig. A.9b) at room temperature.

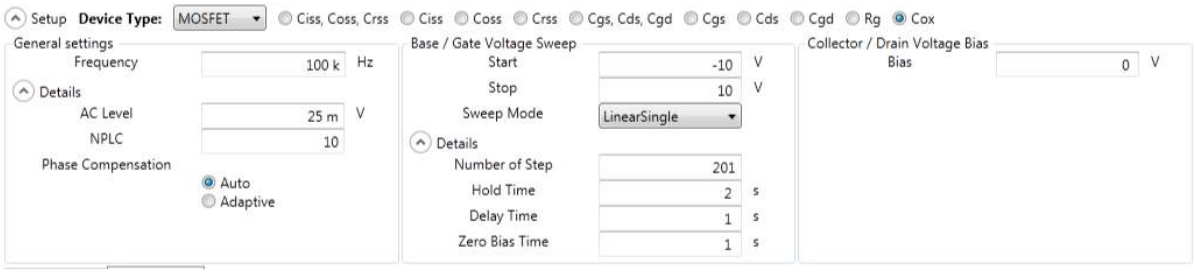


Figure A.10 – Setup used for the measurement of C_{gs}.

comprised between -10 and 10 V with voltage increases of 100 mV (201 measurements) and a delay time of 1 s (see fig. A.10).

A.3 Measurement of the leakage current I_{gs}

In some cases, an additional parameter is characterized. This is the gate-source leakage current. Ideally, the oxide layer should block any current flow. However, it is not perfect and a very low current exists. It depends on the applied voltage between gate-source terminals, as well as on the device temperature.

A special test-bench has been designed to measure this current which could be in the fA range. This test-bench is developed using a Keithley 2636B SMU which communicates with a PC. Using a Labview interface, it is possible to perform two types of measurements: either monitor the leakage current as a function of time, over potentially long periods of time (hundreds to thousands of hours), or to measure the leakage current as a function of gate-source voltage. This interface allows also to define the precision parameters, measurement range, the compliance current or even to realize a fast acquisition (up to t_s=200 ms in High-Accuracy [167] mode) when the measurement starts (to observe transient behaviour). The Labview interface is depicted in fig.A.13, and the test-bench set is shown on fig A.12.

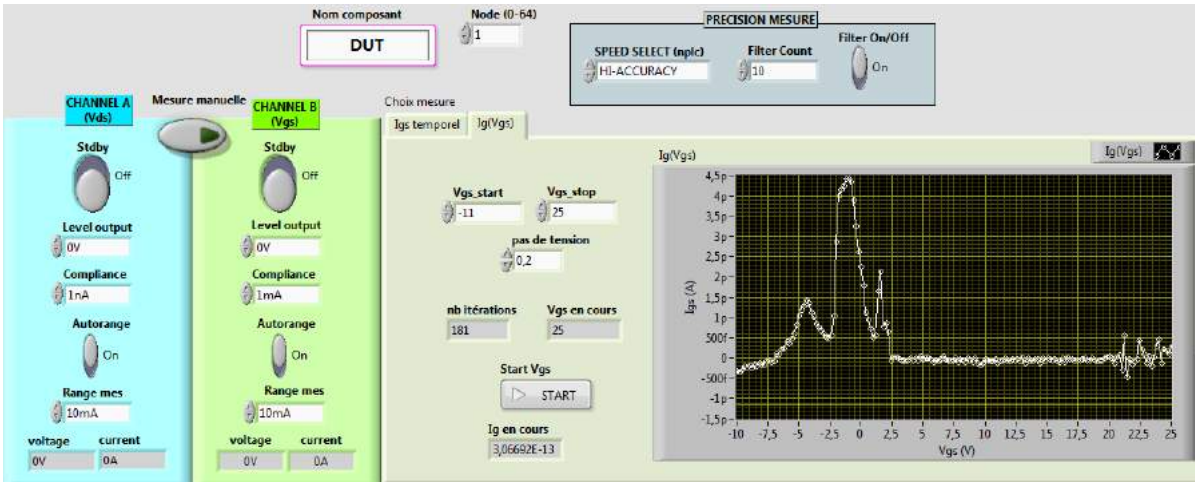


Figure A.11 – Labview interface used to measure gate-source leakage current.

(a) Test-bench used to measure gate-source leakage current.

(b) Measurement box of gate-source leakage current.

Figure A.12 – I_{gs} measurement test-bench.

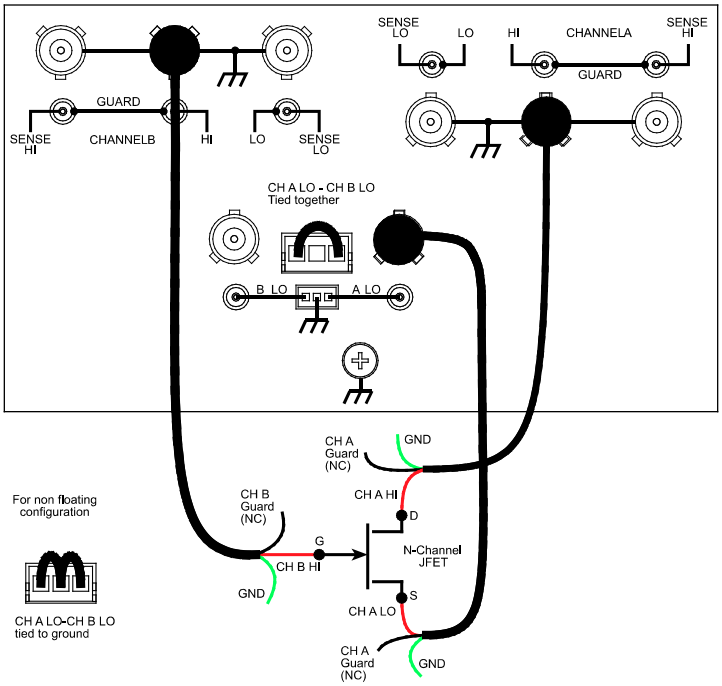
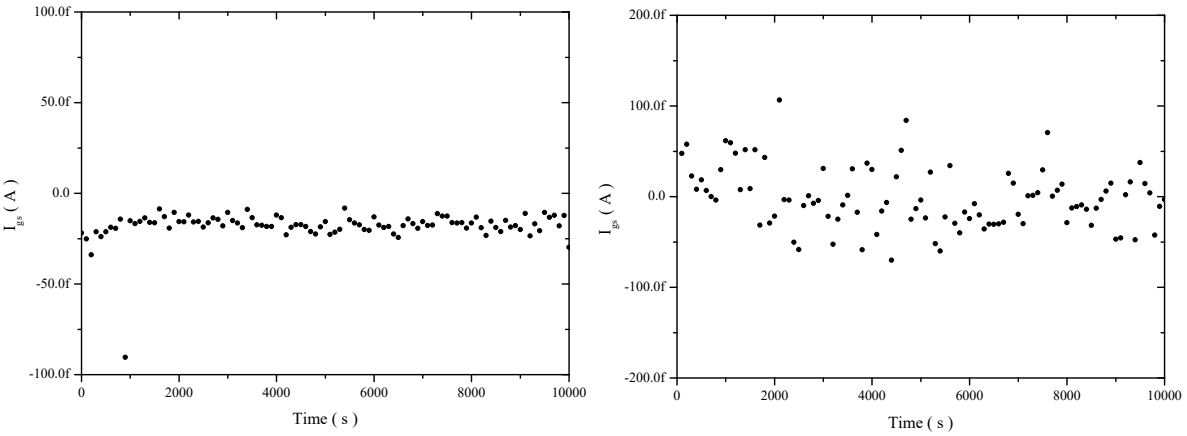


Figure A.13 – Schema of two SMUs (Model 2636A) connected to a 3-terminal MOSFET device for I_{gs} measurement [167].



(a) Measurement of the leakage current of the test-bench (without placing any device).

(b) Measurement of the leakage current I_{gs} on a SiC MOSFET.

Figure A.14 – Tests realized on the I_{gs} measurement test-bench at room temperature.

As it can be seen in fig A.12, the MOSFET under measure is placed in a metallic box to minimize EMI perturbations. A socket is placed on a plastic support in order to limit measurement noise. The three terminals of the socket are connected to the 2626B SMU using triaxial cables. This allows to realize measurements with an error lower than 100 fA. As the gate-source leakage current is really low at ambient temperature, a hot-plate is used to heat the device under measure (to $T_{j_{max}}$). As a result, the measured leakage current is in the order of some pA. Working in this current range, it is easier to identify any trend or degradation on the gate-source current.

Some tests are shown in fig. A.14 and A.15. Fig. A.14a shows the measurement obtained

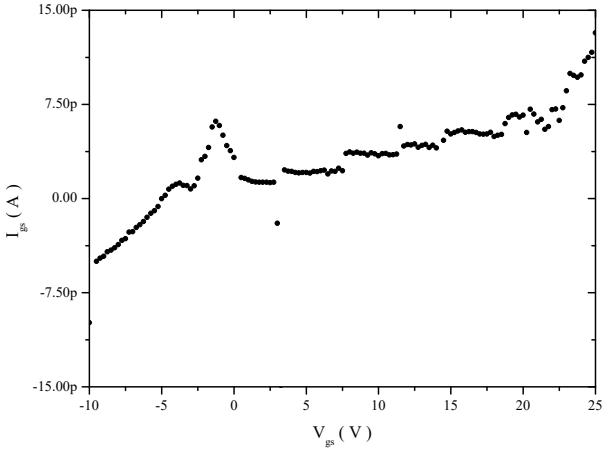


Figure A.15 – I_{gs} measurement depending on V_{gs} for a SiC MOSFET at 150 °C.

when no device is placed into the connector. The aim was to measure if there was a leakage current which could be attributed to the test-bench and if measurements were repetitive. This is the case and measurements are all about -25 fA, which could be attributed to an offset error. Fig. A.14b shows the measured I_{gs} when a pristine SiC MOSFET is placed into the connector and 20 V are applied between gate and source terminals. In this case, the hot plate is not used and device is at room temperature. The measurements are lower than 100 fA, but an important scattering is observed. Finally, fig. A.15 shows the measured leakage current for a SiC MOSFET at 150 °C for V_{gs} ranging from -10 V to 20 V.

A.4 Estimation of the junction temperature

In order to accelerate the tests, they must be performed as close as possible to the maximum rated junction temperature of the device. A key issue is the estimation of T_j. Thus, the thermal resistance of the cooling system has to be determined. In this case, the system includes a hot plate, an electrical insulator (Sil-Pad K10 from Bergquist) and finally the power device. A clip [174] mounted by a screw is used to press the power device against the hot plate. As the hot plate temperature (t_s) is stable and regulated by a thermal controller, there is no need to consider the heat exchange with the environment.

Estimation of the thermal impedance of power devices is a recurrent subject in the literature [150, 151]. Both authors consider that one of the most suitable thermosensitive parameters (TSP) for a MOSFET is the saturation current. However, there are other parameters which depend on the temperature such as the voltage drop of the internal diode or the on-resistance.

First of all, thermosensitive parameters have to be characterized as a temperature-depending function. This stage requires to chose characterization parameters carefully. For example, as explained in annexe A.2, a measurement time so high could lead to a self-heating phenomenon, which would increase the junction temperature we want to measure.

In fact, on our first setup, the characterization protocol was not sufficiently precise and yielded to confusing temperature estimations using TSPs such as on-resistance and internal diode voltage drop.

Characterization setup is improved, using a transistor curve tracer B1505B (setup is described in annexe A.2) within a temperature forcing system (Thermonics T2500E/300).

As the on-resistance of these devices is low (80 $m\Omega$), it leads to some inaccuracies which make difficult the estimation of the temperature. Thus, it is chosen to focus only on the two other parameters (V_f and I_{sat}).

Below, two different estimations using the saturation current and the diode forward voltage are presented. Results are compared to the theoretical thermal resistance obtained from the manufacturers datasheets.

Characterization

The saturation current is characterized over a large range of junction temperatures using the curve tracer B1505B and the temperature forcing system. Obtained results are shown in table A.3 and plotted in fig. A.16, where the dashed-line represents the extracted polynomial regression which is defined by eq. (A.1).

$$I_{sat}(T) = 5.695E^{-5} \cdot T^2 + 6.57E^{-3} \cdot T + 0.55364 \qquad [A] \tag{A.1}$$

T_j (°C)	60	80	100	120	130	140	150	160	170	180
I_{sat} (A)	1.126	1.489	1.834	2.137	2.376	2.573	2.831	3.027	3.401	3.575
V_f (V)	2.909	2.874	2.838	2.808	2.788	2.773	2.758	2.743	2.728	2.713

Table A.3 – Characterization of I_{sat} (V_{gs}=6 V and V_{ds}=8 V) and V_f ($V_{gs} = -8\ V$ and $I_f = 5$ A) between 60 and 180 °C. For a Wolfspeed C2M008012D SiC MOSFET.

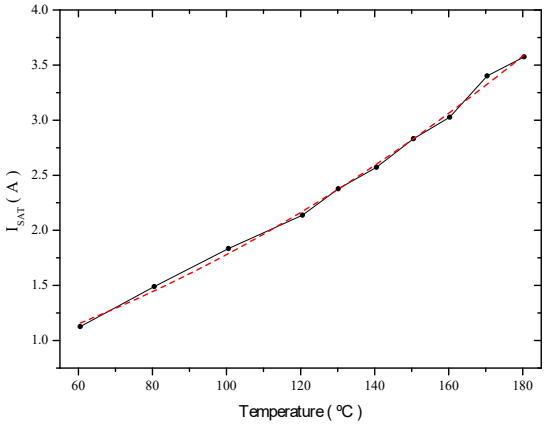


Figure A.16 – Saturation current characterization and its polynomial regression (V_{gs}=6 V and V_{ds}=8 V). For a Wolfspeed C2M008012D SiC MOSFET.

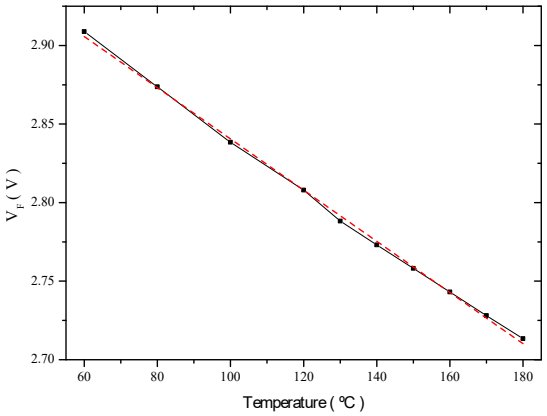


Figure A.17 – Characterization of the internal diode forward voltage and its linear regression ($V_{gs} = -8$ V and $I_f = 5$ A).

The diode forward voltage is characterized in the same way ($V_{gs} = -8$ V, $I_f = 5$ A), as it is shown in the same table A.3. V_f is plotted in fig.A.17 and its behaviour can be described using eq. (A.2).

$$V_f(T) = 3.0034 - 1.6E^{-3} \cdot T \qquad [V] \tag{A.2}$$

Then, from the obtained I_{sat} and V_f characterizations it is possible to determine the junction temperature for the same operation point. As the hot plate temperature is known, it is possible to determine the thermal resistance from the junction of the device to the hotplate.

Thermal resistance of the device and its thermal management system

Saturation current

The operating point is the same as the one used for the parameter characterization. That is, V_{gs}=6 V and V_{ds}=8 V. The chosen temperatures for the hot plate are 80 °C and 110 °C.

For a hot plate temperature of 80 °C, the measured saturation current is 2.11 A. In agreement with eq. (A.1), this matches a junction temperature of 117.1 °C. Then, the junction to

T_s (°C)	I_{sat} (A)	T_j (°C)	P_d (W)	$R_{th_{js}}$ (°C·W^{-1})
80	2.11	117.1	16.88	2.19
110	2.94	155.5	23.51	1.94

Table A.4 – Measured I_{sat} and estimation of T_j and $R_{th_{js}}$ for different hot-plate temperatures (V_{gs}=6 V V_{ds}=8 V).

hot-plate thermal resistance (T_{js}) is calculated by eq. (A.3), where T_j and T_s are the junction temperature and the hot-plate temperature respectively.

$$R_{th_{js}} = \frac{T_j - T_s}{V_{ds} \cdot I_{sat}} = \frac{117.1 - 80}{16.88} = 2.19 \qquad \left[°C \cdot W^{-1}\right] \tag{A.3}$$

For a hot-plate temperature of 110 °C, the measured saturation current is 2.938 A, corresponding to a junction temperature of 155.5 °C in agreement with eq. (A.1). Thus, the thermal impedance should be 1.94$°C/W$.

$$R_{th_{js}} = \frac{T_j - T_s}{V_{ds} \cdot I_{sat}} = \frac{155.5 - 110}{23.51} = 1.94 \qquad \left[°C \cdot W^{-1}\right] \tag{A.4}$$

It seems that the thermal resistance could change depending on several factors, such as dissipated power or hot-plate temperature. The following experiment, based on the diode voltage forward characterization, is realized at three different hot-plate temperatures. The goal is to determine if the hot-plate temperature plays a role in the evolution of $R_{th_{js}}$.

Forward Voltage

The forward voltage is measured at the same point of operation than during the characterization, this is $V_{gs} = -8\ V$ and $I_f = 5$ A. As said, this test is realized at three different hot-plate temperatures (85 °C, 100 °C and 115 °C). The measures, as well as the estimation of T_j and $R_{th_{js}}$ are shown on table A.5. Eq. (A.2) and (A.5) have been used to calculate T_j and $R_{th_{js}}$ respectively.

$$R_{th_{js}} = \frac{T_j - T_s}{I_f \cdot V_f} \tag{A.5}$$

Obtained results for all three hot-plate temperatures are very similar, and the obtained $R_{th_{js}}$ is around 1.84 $°C/W$. As the dissipated power is always near 14 W, it can be concluded that the hot-plate temperature does not have a significant impact on $R_{th_{js}}$.

However, it is no possible to conclude if the dissipated power has a significant effect on $R_{th_{js}}$. The highest values of $R_{th_{js}}$ using the saturation current (2.19 $°C/W$) corresponds to a dissipated power of 16.88 W. This power is relatively close to the 14 W dissipated using the internal diode, and one could expect similar results. Furthermore, for the case where the dissipated power is 23 W, the obtained $R_{th_{js}}$ (1.94 $°C/W$) is relatively close to that obtained using the parameter V_f.

To verify the results, a theoretical calculation of $R_{th_{js}}$ is presented below. This is based on the insulator film, the clip and the MOSFET datasheets [175, 174, 152].

T_s (°C)	V_f (V)	T_j (°C)	P_d (W)	$R_{th_{js}}$ (°C·W^{-1})
85	2.826	111.0	14.13	1.84
100	2.803	125.4	14.01	1.81
115	2.778	141.0	13.89	1.87

Table A.5 – Measured V_f and estimation of T_j and $R_{th_{js}}$ for different hot-plate temperatures ($V_{gs} = -8\ V$ and $I_f = 5$ A). T_j is calculated by eq. (A.2). $R_{th_{js}}$ is calculated in agreement with eq. (A.5).

Pressure (psi)	10	25	50	100	200
Thermal resistance (°C· in^2/W)	0.86	0.56	0.41	0.38	0.33

Table A.6 – Thermal resistance dependence of pressure for Sil-Pad K-10 from Bergquist [175].

Theoretical Estimation

The insulator manufacturer provides a set of values of the Sil-Pad K10 thermal resistance depending on the applied pressure. This parameter is very important, because as it can be seen on table A.6, the thermal resistance is highly dependent on the pressure. A clip is used to press the device. This clip [174] datasheet indicates that it is capable to apply a force of 60 N. This, combined with the device metallic area (0.263 in^2) [152], leads to a pressure slightly higher than 50 psi, which we will consider uniform over the device area.

Fig. A.18a is based on the data provided by Bergquist. The black line is the thermal resistance of a TO-220, in agreement with the thermal impedance of the insulator film and the metallic area of a TO-220 (0.18 in^2). The red line is based on a measurement of the thermal resistance of a TO-220 package, which is provided in the insulator film datasheet [175]. It is noticeable that the red line is always below than the calculated values.

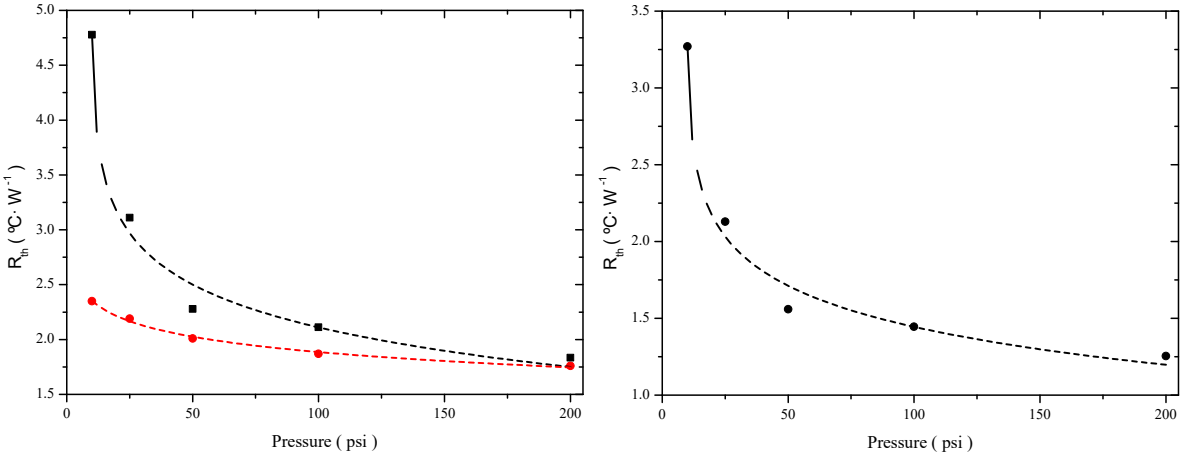
Fig. A.18b is similar to the last one, but only the calculated values are plotted because no information is provided in [175] for a TO-247 package. However, at 50 psi, the calculated thermal resistance of the insulator film is 1.56 $°C/W$. Adding this thermal resistance to the junction-case thermal resistance of the MOSFET (0.65 $°C/W$ [152]), leads to a $R_{th_{js}}$=2.21 $°C/W$.

The real $R_{th_{js}}$ value is expected to be smaller in the same way that measured TO-220 thermal resistance is lower than the calculated one. Insulator film datasheet, as well as device datasheet gives the maximal value, but normally it should be lower.

Calculation of the uncertainty error

Some divergences have been observed in the calculation of the thermal resistance. Here, a calculus. As a reminder, the junction temperature is calculated in agreement with equation (A.6). Thus, the absolute error of the junction temperature (ΔT_j) can by defined by eq. (A.7), where ΔT_s is the hot-plate temperature error and ΔT_{js} is the junction to hot-plate temperature error.

$$T_j = T_s + P_d \cdot R_{th_{js}} \tag{A.6}$$



(a) In black- Calculated thermal resistance based on SilPad K-10 thermal impedance [175] and TO-220 measured metallic area (0.18 in^2). In red- Thermal resistance for a TO-220 package mesured by Bergquist [175].

(b) Calculated thermal resistance based on SilPad K-10 thermal impedance [175] and TO-247 measured metallic area (0.263 in^2). No measurement on a TO-247 of thermal impedance is provided by the manufacturer.

Figure A.18 – Thermal resistances for TO-220 (a) and TO-247 (b) packages depending on applied pressure.

$$\Delta T_j = \Delta T_s + \Delta T_{js} \tag{A.7}$$

The temperature of the hot-plate is measured with a thermocouple just under the device (through a hole in the hot-plate). The temperature regulation has an hysteresis slightly higher than 1 °C. Thus, to be conservative, an absolute error of 2 °C is assumed for the hot-plate temperature.

The estimation of the junction to hot-plate absolute error is based on the thermal resistance estimations for the thermal management system, which have been described above. In this way, the absolute error of the junction to hot-plate thermal impedance is defined as the product between the dissipated power (P_d) and the subtraction between the maximum and the minimum value estimated for the thermal resistance ($\Delta R_{th_{js}}$):

$$\Delta T_{js}(P_d) = \pm P_d \cdot \Delta R_{th_{js}} \tag{A.8}$$

Then, in agreement with eq. (A.7), the absolute error of the junction temperature can be calculated as a function of the dissipated power as follows:

$$\Delta T_j(P_d) = \pm 2 \pm P_d \cdot (2.19 - 1.81) = \pm 2 \pm 0.38 \cdot P_d \tag{A.9}$$

In this thesis, the case where a higher power is dissipated (37.3 W) corresponds to the static tests run in chapter 2. The error associated with the P_d measurement is neglected because measurement instruments have accuracies better than 0.5%, which in any case would result in estimation error lower than 0.4 °C. Thus, in agreement with eq. (A.10), we estimate that in all cases the temperature uncertainty is lower than 10 °C.

$$\Delta T_j(P_d = 37.3W) = \pm 2 \pm 0.38 \cdot 37.3 = \pm 9.6 \qquad \left[°C \cdot W^{-1}\right] \tag{A.10}$$

Conclusions

Theoretical and experimental calculations of $R_{th_{js}}$ have been presented in this annexe. Experimental values of $R_{th_{js}}$ range between 1.81 and 2.19°C/W.

Results using the diode forward voltage as a thermosensitive parameter are more consistent than those using the saturation current. Some test have been realized using R_{ds} as a thermosensitive parameter, but results were poor and not detailed here.

Test studying the effects of hot-plate temperature and dissipated power on $R_{th_{js}}$ have reported that hot-plate temperature does not have a significant impact. Data about dissipated power are not consistent.

The theoretical estimation has found that for a TO-247, the thermal resistance should be $R_{th_{js}}$=2.21°C/W. As this calculation is based on the datasheets which includes some safety margins, it is expected that the actual thermal resistance will be lower. We estimate that the values obtained experimentally using the internal diode as a thermosensitive parameter seems more realistic (about 1.84°C/W).

In spite of this, in order to avoid device overheating during our tests, it is preferred to be conservative. Thus, in this thesis the $R_{th_{js}}$ value used to estimate the junction temperature is the highest value obtained experimentally, this is 2.19°C/W. In addition, a calculation of the uncertainty error (assuming steady-state model) is realized in this annexe, resulting in an error of the junction temperature lower than 10 °C.

A.5 CMB Test-Bench Description

The test-bench presented here is designed to test power MOSFET devices under realistic conditions. As the aim of the research project is to study the possible use of these devices for aeronautical applications, there are two basic requirements:

- Use of the same voltage than in the aeronautics HVDC, 540 V.
- Use of an inductive load.

To realize that, two options are on the table. The first one is simplest, but thermally and environmentally undesirable. It is a simple architecture with two MOSFET devices transferring power from a source to a load where all power is dissipated (2.7 kW). As the converter works permanently for weeks, this possibility is discarded.

The chosen architecture is a "back-to-back" converter, where the energy is provided by a power source. Its principle diagram can be seen in fig. A.19. The converter can be separated in two different stages. The first one is a buck converter, and the second one a boost converter. In the middle of this two stages, a capacitor is placed in order to minimize perturbations. The boost converter re-injects the energy to the power source. Thus, the losses are limited to the power energy dissipated in the inductors and MOSFETs (around 200 W), and are independent from the apparent power managed by the MOSFETs.

Description of operation modes

Fig. A.20 shows the circuit diagram of the test-bench. As introduced in chapter 2, two different tests are run. The first one, when the DUT remains always blocked, and the second one when the conduction time of the DUT is divided between the PN junction and the channel. These two modes of operation are detailed bellow.

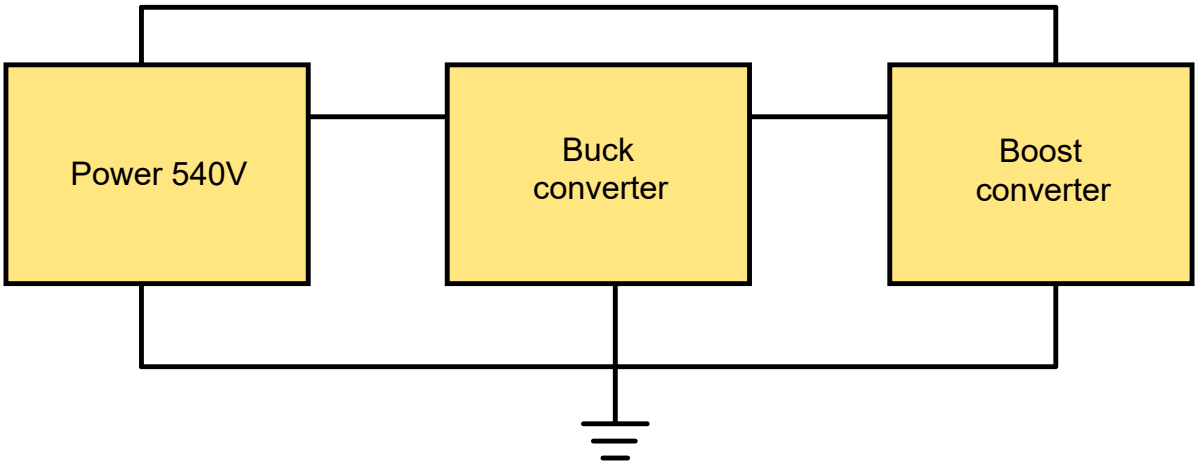


Figure A.19 – Principle diagram for the back to back structure.

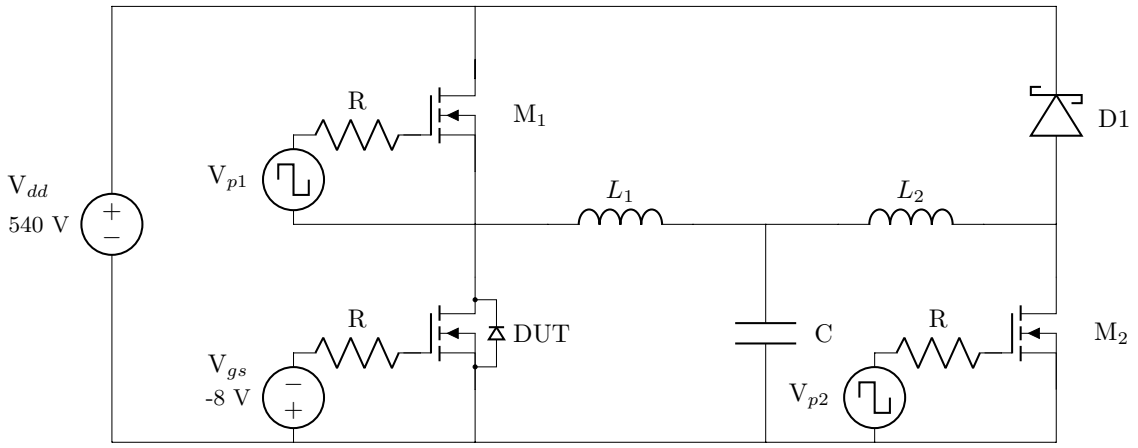


Figure A.20 – Schematic of the back to back test-bench (CMB).

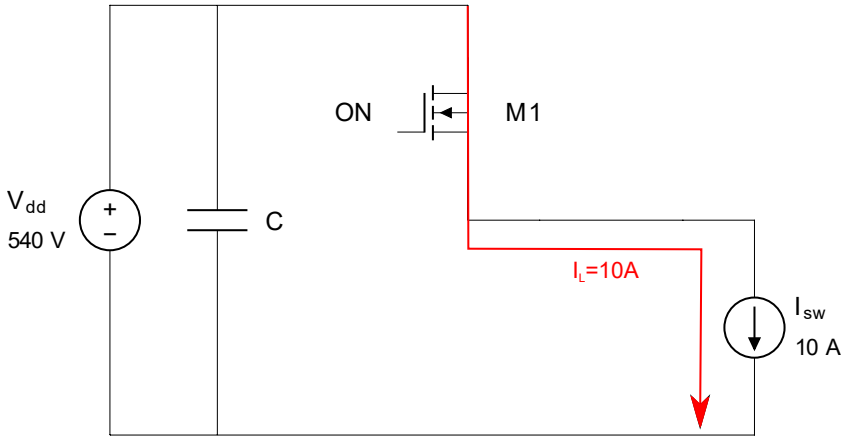


Figure A.21 – Equivalent circuit diagram and current path when switch M_1 is in the on state and the DUT remains blocked.

CMB test-bench - Channel always blocked -

Circuit configuration M1 On - DUT Off

In this case (see fig. A.21), the DUT is in the off state (modelled as an open circuit) and the MOSFET M_1 is conducting. Its duty cycle (M_1) is 0.5. The voltage source supplies energy to the inductor and I_L increases, remaining always near 10 A due to the high inductance value. This ensures that the inductor energy is enough for when the switch M_1 is blocked and this has to supply the required current to stress the DUT.

Circuit configuration M1 Off - DUT Off

In this case (see fig. A.22), as M_1 is blocked (modelled as an open circuit), the inductor supplies the energy. The DUT also remains blocked. The current flows through the DUT P-N junction, which becomes forward biased at near 10 A.

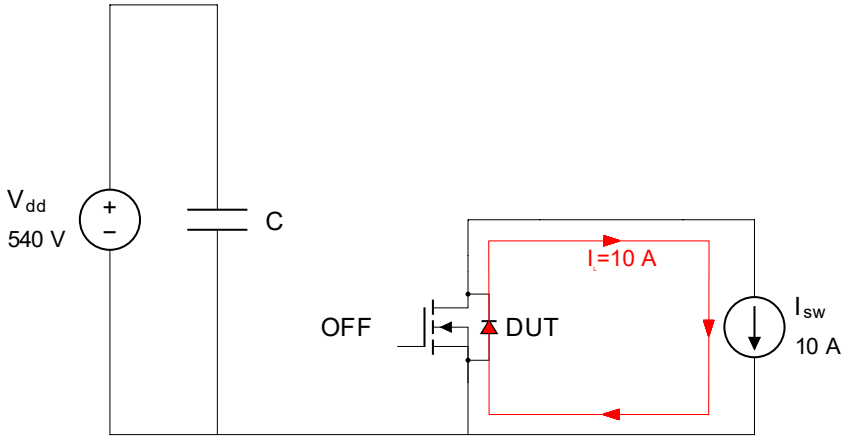


Figure A.22 – Equivalent circuit diagram and current path when the switch M_1 and the DUT are in the off state. The DUT is conducting through the internal diode.

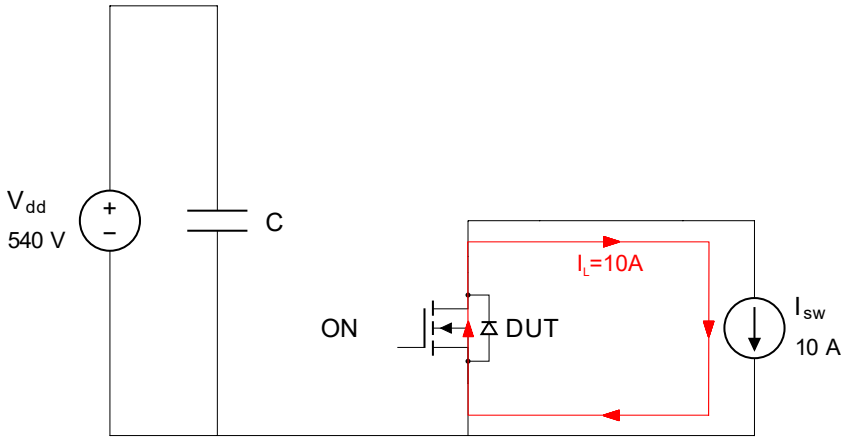


Figure A.23 – Equivalent circuit diagram and current path when switch M_1 is the off state and the DUT on the on state (conducting through the channel).

CMB test-bench - Channel sometimes conducting -

Circuit configuration M1 On - DUT Off

As described above, the voltage source supplies energy to the inductor. No current flows through the DUT which is blocking the input voltage (540 V).

Circuit configuration M1 Off - DUT Off

As described above, the inductor supplies energy and the current flows through the internal P-N junction. M_1 is in the off state blocking the voltage $V_{dd} - V_f$.

Circuit configuration M1 Off - DUT On

In this third case of operation, M_1 remains blocking the V_{dd} voltage.

Then, the gate is positively biased, and the DUT turns on. Thus, the current path gradually changes from the P-N junction to the channel. This mode of operation is represented in fig. A.23. The DUT remains conducting through the channel for a period which depends on the desired duty cycle before to return to the case where both switches are in the off state.

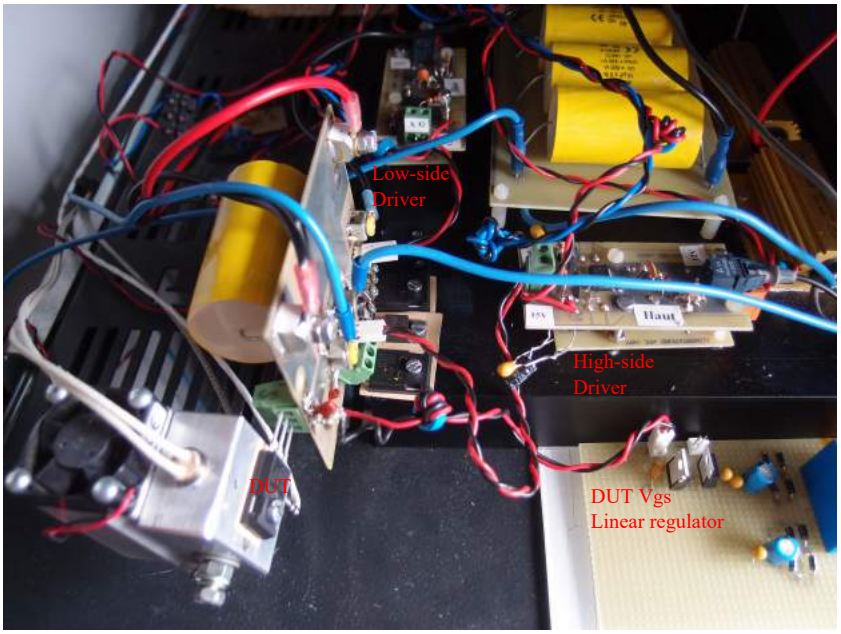


Figure A.24 – CMB1 test-bench.

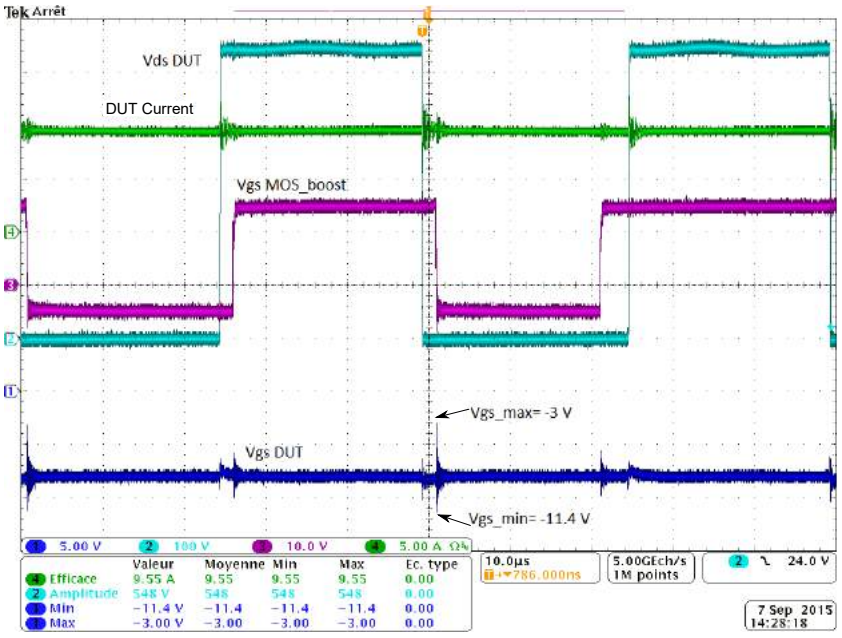


Figure A.25 – Measured waveforms on CMB1 test-bench.

Experimental test-bench setup

As introduced in chapter 2, two versions of the test-bench have been developed. The first one (CMB1) is shown in fig. A.24. The main waveforms are depicted in fig. A.25. However, this test-bench is far to have an optimum design and important perturbations are observed in the DUT gate-source voltage (A.25).

Thus, a second test-bench is designed taking special care about EMI perturbations and the drivers output signals. This test-bench is shown in fig. A.26. As it can be seen, in this second test-bench several improvements are realized to minimize EMI perturbations; the heat-sinks

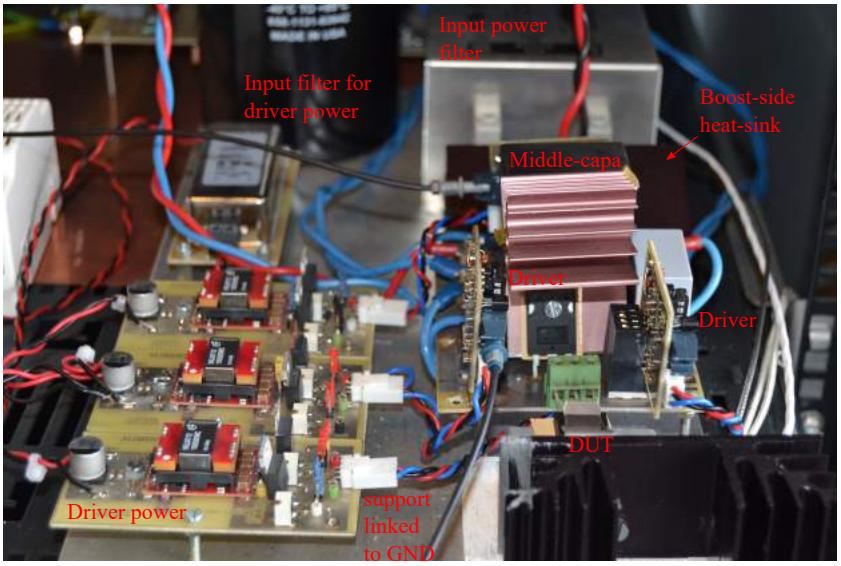


Figure A.26 – CMB2 test-bench.

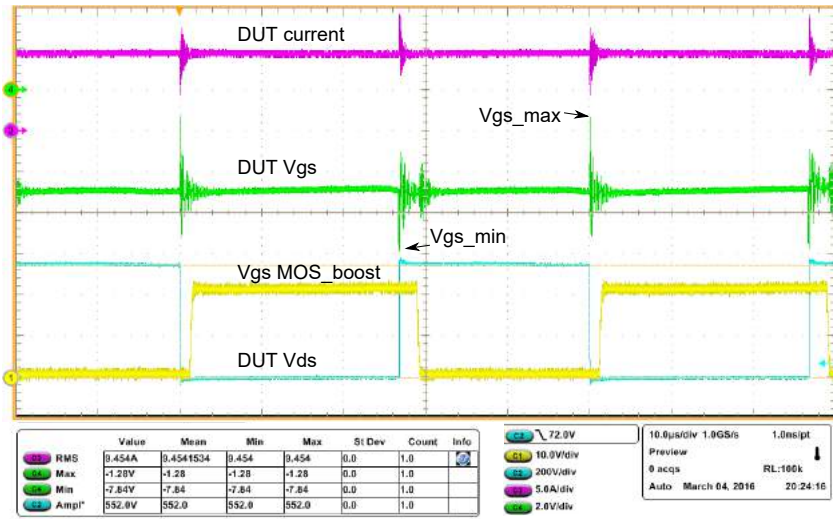


Figure A.27 – Measured waveforms on CMB2 test-bench.

for the boost and buck converters are independents, input filters (power and drivers) are added and a metallic support connected the different stages to the ground. In addition, the drivers are situated very close to the power switches, reducing parasitic inductances.

Some waveforms for this test-bench (CMB2) are depicted in fig. A.27. Even if some important perturbations remain visible on the gate-source voltages, thanks to the improvements in the test-bench it is possible to remove two 0.47 Ω resistors (not shown in fig. A.24, but placed in series with L1 and L2) which are added in the first test-bench to stabilize the system.

Regarding EMI perturbations, these are successfully minimized for the CMB2 test-bench as it is shown in fig. A.28 and A.29.

Fig. A.28 shows the common mode current (IMC) measured at the power input for the two test-bench; CMB1 and CMB2. Obtained results are compared with the different categories of the RTCA DO-160E standard [176], which addresses aeronautics. It can be seen that there remains a peak at the frequency of 1 MHz, that could be minimized with the addition of a

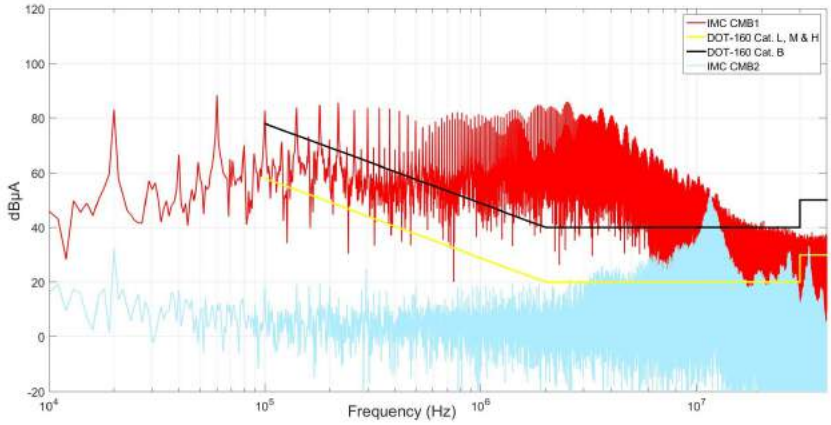


Figure A.28 – Comparison of measured common-mode interferences in CMB1 and CMB2 test-benches and DO-160 standard [176].

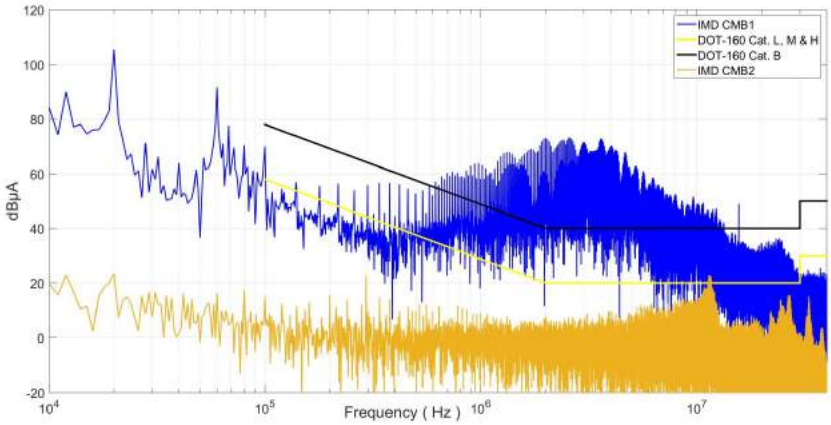


Figure A.29 – Comparison of measured differential-mode interferences in CMB1 and CMB2 test-benches and DO-160 standard [176].

filter in the input.

The same comparison is shown in fig. A.29, but this time measuring the differential mode current (IMD), also measured at the power input.

A.6 Internal diode robustness data

HTRB Test

	DUT 1	DUT 2	DUT 3	DUT 4	DUT 5	DUT 6	DUT 7	DUT 8	DUT 9	DUT 10
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
15 h	1.02	1.00	0.98	0.95	1.01	0.96	1.03	1.06	0.96	1.07
100 h	1.16	1.14	1.07	1.09	1.18	1.08	1.15	1.11	1.09	1.15
200 h	1.11	1.03	1.04	1.03	1.11	1.04	1.09	1.07	1.00	1.08
300 h	1.28	1.19	1.17	1.10	1.21	1.12	1.22	1.16	1.16	1.12
400 h	1.23	1.13	1.13	1.07	1.19	1.09	1.11	1.11	1.20	1.22

Table A.7 – Normalized R_{ds} evolution over stress time for HTRB tests on Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

	DUT 1	DUT 2	DUT 3	DUT 4	DUT 5	DUT 6	DUT 7	DUT 8	DUT 9	DUT 10
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
15 h	1.01	0.97	1.00	0.98	1.01	0.98	1.01	1.02	0.99	1.02
100 h	1.03	1.03	1.02	1.01	1.04	1.00	1.03	1.02	1.01	1.03
200 h	1.02	1.00	1.00	0.99	1.02	0.99	1.019	1.02	0.99	1.01
300 h	1.05	1.04	1.04	1.00	1.04	1.02	1.04	1.03	1.02	1.02
400 h	1.04	1.02	1.03	0.99	1.04	1.00	1.01	1.02	1.02	1.03

Table A.8 – Normalized V_f evolution over stress time for HTRB tests on Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

	DUT 1	DUT 2	DUT 3	DUT 4	DUT 5	DUT 6	DUT 7	DUT 8	DUT 9	DUT 10
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
15 h	0.99	0.96	0.97	0.96	0.96	0.96	0.95	0.96	0.96	0.93
100 h	0.98	0.97	0.97	0.97	0.98	0.97	0.96	0.96	0.96	0.94
200 h	1.00	0.98	0.97	0.98	0.98	0.97	0.97	0.98	0.99	0.96
300 h	1.00	0.98	0.99	0.99	0.98	0.98	0.98	0.98	0.98	0.96
400 h	1.01	0.99	1.00	1.00	1.00	0.99	0.99	1.00	0.99	0.97

Table A.9 – Normalized V_{th} evolution over stress time for HTRB tests on Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

Active Static Tests

	DUT 1	DUT 2	DUT 3	DUT 4	DUT 5	DUT 6	DUT 7	DUT 8	DUT 9
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
2 h	-	-	-	1.02	1.01	1.01	-	-	-
5 h	-	-	-	-	-	-	1.00	1.00	1.01
10 h	-	-	-	1.00	0.99	1.00	-	-	-
15 h	0.96	0.99	1.00	-	-	-	-	-	-
20 h	-	-	-	1.07	1.01	1.01	0.99	0.99	0.99
40 h	0.94	0.96	0.94	0.99	1.03	1.02	0.98	0.99	1.00
60 h	0.94	0.96	0.96	-	-	-	0.99	0.99	1.00
80 h	0.94	0.96	0.96	1.04	1.00	1.14	0.99	0.99	0.99
100 h	0.95	0.97	0.96	-	-	-	0.99	0.99	1.00
Test	Q1	Q1	Q1	Q3	Q3	Q3	Q4	Q4	Q4

Table A.10 – Normalized R_{ds} evolution over stress time for Q1 ($V_{gs} = 20\,V$), Q3 and Q4 ($V_{gs} = -8\,V$) tests on Wolfspeed devices (C2M008012D), lot 2 (Ref. W10116 and W10216, year 2016).

	DUT 1	DUT 2	DUT 3	DUT 4	DUT 5	DUT 6	DUT 7	DUT 8	DUT 9
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
2 h	-	-	-	1.02	1.01	1.01	-	-	-
5 h	-	-	-	-	-	-	1.00	1.00	1.00
10 h	-	-	-	1.00	1.00	1.00	-	-	-
15 h	0.98	0.99	0.98	-	-	-	-	-	-
20 h	-	-	-	1.03	1.01	1.01	1.00	0.99	1.00
40 h	0.98	0.98	0.98	1.00	1.01	1.01	1.00	0.99	1.00
60 h	0.98	0.99	0.98	-	-	-	1.00	1.00	1.00
80 h	0.95	0.96	0.96	1.03	1.01	1.6	1.00	1.00	1.00
100 h	0.98	0.99	0.98	-	-	-	1.00	1.00	1.00
Test	Q1	Q1	Q1	Q3	Q3	Q3	Q4	Q4	Q4

Table A.11 – Normalized V_f evolution over stress time for Q1 ($V_{gs} = 20\ V$), Q3 and Q4 ($V_{gs} = -8\ V$) tests on Wolfspeed devices (C2M008012D), lot 2 (Ref. W10116 and W10216, year 2016).

	DUT 1	DUT 2	DUT 3	DUT 4	DUT 5	DUT 6	DUT 7	DUT 8	DUT 9
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
2 h	-	-	-	0.84	0.86	0.86	-	-	-
5 h	-	-	-	-	-	-	1.01	1.00	1.00
10 h	-	-	-	0.72	0.76	0.76	-	-	-
15 h	1.01	1.02	1.01	-	-	-	-	-	-
20 h	-	-	-	0.67	0.70	0.70	1.01	1.00	1.01
40 h	1.02	1.02	1.02	0.60	0.64	0.64	1.00	1.01	1.00
60 h	1.02	1.02	1.01	-	-	-	1.01	1.02	1.01
80 h	1.02	1.02	1.01	0.55	0.59	0.59	1.00	1.02	1.00
100 h	1.02	1.01	1.01	-	-	-	1.00	1.02	1.00
Test	Q1	Q1	Q1	Q3	Q3	Q3	Q4	Q4	Q4

Table A.12 – Normalized V_{th} evolution over stress time for Q1 ($V_{gs} = 20\ V$), Q3 and Q4 ($V_{gs} = -8\ V$) tests on Wolfspeed devices (C2M008012D), lot 2 (Ref. W10116 and W10216, year 2016).

	R_{ds}			V_f			V_{th}		
	DUT D4	DUT D5	DUT D6	DUT D4	DUT D5	DUT D6	DUT D4	DUT D5	DUT D6
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
2 h	1.20	0.99	0.98	1.08	0.99	0.99	0.99	0.99	0.99
20 h	0.97	0.89	0.89	0.98	0.96	0.96	0.96	0.97	0.97
40 h	0.97	0.88	0.89	0.98	0.96	0.96	0.96	0.97	0.97
80 h	0.97	0.90	0.88	0.98	0.96	0.96	0.94	0.95	0.96
200 h	0.95	0.87	0.88	0.98	0.96	0.96	0.93	0.93	0.93

Table A.13 – Normalized values evolution of R_{ds}, V_f and V_{th} over stress time for Q3 test ($V_{gs} = -5\ V$). Wolfspeed devices (C2M008012D), lot 2 (Ref. W10116, year 2016).

CMB Test -Channel always blocked-

	DUT C4	DUT C5	DUT C6	DUT C7	DUT C8	DUT C9	DUT C10	DUT C11	DUT C12	DUT C13
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
10 h	0.6	1.06	1.20	1.12	0.85	0.82	0.92	0.94	0.98	0.98
20 h	-	1.10	1.22	1.16	0.84	0.82	0.90	0.95	0.97	0.98
40 h	-	1.15	1.11	1.05	0.83	0.83	0.91	0.94	0.97	0.96
60 h	-	1.22	1.12	0.99	0.89	0.84	0.90	0.93	0.98	0.96
80 h	-	1.08	1.08	1.00	0.88	1.01	0.94	0.95	0.98	0.98
100 h	-	1.01	0.89	0.91	1.07	1.00	0.95	0.94	0.99	1.01

Table A.14 – Normalized R_{ds} evolution over stress time for CMB1 tests on Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

	DUT C4	DUT C5	DUT C6	DUT C7	DUT C8	DUT C9	DUT C10	DUT C11	DUT C12	DUT C13
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
10 h	0.86	1.03	1.05	1.02	0.96	0.99	1.00	1.02	1.01	1.00
20 h	-	1.02	1.04	1.03	0.97	0.99	1.00	1.01	1.01	1.01
40 h	-	1.03	1.03	1.03	0.96	0.95	1.00	1.02	1.01	1.01
60 h	-	1.06	1.03	1.00	0.98	0.99	1.00	1.02	1.01	1.01
80 h	-	1.03	1.01	1.00	0.98	1.01	0.99	1.01	1.01	1.01
100 h	-	1.00	0.98	0.97	1.02	1.01	0.98	1.02	1.01	1.00

Table A.15 – Normalized V_f evolution over stress time for CMB1 tests on Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

	DUT C4	DUT C5	DUT C6	DUT C7	DUT C8	DUT C9	DUT C10	DUT C11	DUT C12	DUT C13
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
10 h	0.25	0.91	0.89	0.89	0.90	0.90	0.88	0.90	0.90	0.88
20 h	-	0.86	0.87	0.88	0.88	0.88	0.86	0.87	0.89	0.86
40 h	-	0.84	0.84	0.86	0.86	0.84	0.82	0.84	0.87	0.84
60 h	-	0.84	0.82	0.85	0.85	0.83	0.80	0.86	0.86	0.82
80 h	-	0.82	0.80	0.83	0.85	0.79	0.77	0.84	0.84	0.83
100 h	-	0.82	0.82	0.81	0.82	0.79	0.75	0.84	0.82	0.80

Table A.16 – Normalized V_{th} evolution over stress time for CMB1 tests on Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

	DUT R1	DUT R2	DUT R3	DUT ST1	DUT ST2	DUT ST3
0 h	1.00	1.00	1.00	1.00	1.00	1.00
20 h	0.86	0.94	0.88	1.03	1.02	1.02
40 h	0.86	0.94	0.88	1.03	1.02	1.02
60 h	0.88	0.94	0.87	1.03	1.02	1.03
80 h	0.91	0.93	0.87	0.99	1.03	1.03
100 h	0.87	0.93	0.88	1.02	1.02	1.02
Manufacturer	ROHM	ROHM	ROHM	ST	ST	ST

Table A.17 – Normalized R_{ds} evolution over stress time for CMB1 tests on ROHM SCT2080KE (Ref. 15-04, year 2015) and ST SCT30N120 (Ref. CHN-GK-552, year 2015) devices.

	DUT R1	DUT R2	DUT R3	DUT ST1	DUT ST2	DUT ST3
0 h	1.00	1.00	1.00	1.00	1.00	1.00
20 h	0.98	0.99	0.98	1.00	1.00	1.00
40 h	0.98	0.99	0.98	1.00	1.00	1.00
60 h	0.98	0.99	0.98	1.00	1.00	1.00
80 h	0.98	0.99	0.98	1.00	1.00	1.00
100 h	0.99	0.99	0.98	1.00	1.00	1.00
Manufacturer	ROHM	ROHM	ROHM	ST	ST	ST

Table A.18 – Normalized V_f evolution over stress time for CMB1 tests on ROHM SCT2080KE (Ref. 15-04, year 2015) and ST SCT30N120 (Ref. CHN-GK-552, year 2015) devices.

	DUT R1	DUT R2	DUT R3	DUT ST1	DUT ST2	DUT ST3
0 h	1.00	1.00	1.00	1.00	1.00	1.00
20 h	1.00	0.98	0.99	0.97	0.96	0.97
40 h	1.01	0.98	0.98	0.96	0.96	0.96
60 h	0.99	0.98	1.00	0.96	0.95	0.96
80 h	0.97	1.00	1.00	0.96	0.96	0.96
100 h	1.01	0.99	1.03	0.96	0.95	0.95
Manufacturer	ROHM	ROHM	ROHM	ST	ST	ST

Table A.19 – Normalized R_{ds} evolution over stress time for CMB1 tests on ROHM SCT2080KE (Ref. 15-04, year 2015) and ST SCT30N120 (Ref. CHN-GK-552, year 2015) devices.

	DUT CMB21	DUT CMB22	DUT CMB23	DUT CMB24	DUT CMB25	DUT CMB26
0 h	1.00	1.00	1.00	1.00	1.00	1.00
5 h	0.81	0.79	0.77	0.97	0.95	0.96
20 h	0.71	0.69	0.65	0.96	0.95	0.95
40 h	0.65	0.64	0.59	0.96	0.93	0.95
60 h	0.63	0.63	0.56	0.95	0.93	-
80 h	0.62	0.60	0.53	-	0.93	-
100 h	0.61	0.60	0.51	-	0.93	-
CMB V_{gs}	-8 V	-8 V	-8 V	-5 V	-5 V	-5 V

Table A.20 – Normalized V_{th} evolution over stress time for CMB2 tests on Wolfspeed C2M008012D devices, lot 2 (Ref. W10216, year 2016).

CMB Test -Channel sometimes conducting-

	R_{ds}			V_f			V_{th}		
	DUT 005	DUT 015	DUT 085	DUT 005	DUT 015	DUT 085	DUT 005	DUT 015	DUT 085
0 h	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
10 h	0.99	0.99	1.00	1.00	1.00	1.01	0.95	0.97	1.03
20 h	1.00	1.25	0.99	1.00	1.04	1.01	0.94	0.97	1.04
40 h	1.23	1.01	0.99	1.03	1.00	1.01	0.93	0.97	1.06
60 h	1.02	1.01	1.01	1.00	1.00	1.00	0.94	0.98	1.06
80 h	1.03	1.01	1.01	1.00	1.00	1.01	0.94	0.98	1.07
100 h	1.03	1.01	1.03	1.00	1.00	1.01	0.93	0.99	1.09
Duty cycle	0.05	0.15	0.85	0.05	0.15	0.85	0.05	0.15	0.85

Table A.21 – Normalized values evolution of R_{ds}, V_f and V_{th} over stress time for CMB1 tests in the case where the channel is used. Wolfspeed devices (C2M008012D), lot 1 (Ref. W14514, year 2014).

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National Conference papers

O. Avino-Salvado, H. Morel and C. Buttay (2017). Étude de la robustesse de l'oxyde de grille pour des applications aéronautiques. *Jeunes Chercheurs en Génie Électrique, JCGE 2017*, Arras (France), May 2017.

O. Avino-Salvado, C. Cheng, C. Buttay, H. Morel, D. Labrousse, S. Lefebvre, M. Ali (2016). Analyse de la robustesse des MOSFET SiC pour les applications "Diode-less". *Symposium de Génie Électrique 2016 (SGE)*, Grenoble (France), July 2016.

FOLIO ADMINISTRATIF

THESE DE L'UNIVERSITE DE LYON OPEREE AU SEIN DE L'INSA LYON

NOM : Aviñó Salvadó

DATE de SOUTENANCE : 14/12/2018

Prénoms : Oriol

TITRE : Contribution à l'étude de la robustesse de l'oxyde de grille des MOSFET en SiC

NATURE : Doctorat

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Ecole doctorale : EEA 160

Spécialité : Génie Électrique

RESUME :

Les MOSFET en SiC sont appelées à remplacer les IGBT en silicium pour des applications demandant une plus forte vitesse de commutation. Cependant, les MOSFET en SiC ont encore quelques problèmes de fiabilité, tels que la robustesse de la diode interne ou bien la robustesse de l'oxyde de grille. Cette dernière est liée à l'oxyde de grille des composants de type MOSFET. Des instabilités de la tension de seuil sont aussi signalées. Cette thèse aborde ces deux sujets sur les MOSFET commerciaux 1200 V.
L'étude de la diode interne met en évidence que les caractéristiques I-V (de la diode intrinsèque) demeurent stables après l'application d'un stress. Cependant, une dérive surprenante de la tension de seuil apparaît. Des tests complémentaires, en stressant le canal à la place de la diode, avec les mêmes contraintes n'ont pas montré de dérive significative de la tension de seuil. Donc, l'application d'un stress en courant quand le composant est en mode d'accumulation semble favoriser l'apparition des instabilités de la tension de seuil.
La robustesse de l'oxyde de grille concerne les instabilités de la tension de seuil, mais aussi l'estimation de la durée de vie dans des conditions de fonctionnement nominales.
Les résultats obtenus montrent que la durée de vie de l'oxyde de grille n'est plus un problème. Pourtant, le suivi du courant de grille pendant les tests ainsi que les caractérisations de la capacité de grille mettent en évidence des déplacements de la courbe C(V) à cause de phénomènes d'injection des porteurs et de piégeage, mais aussi la possible présence d'ions mobiles.
L'analyse des dégradations et dérives liées à l'oxyde de grille doit être poursuivie plus profondément.

MOTS-CLÉS :

MOSFET, SiC, Gate Oxide, SiO2, SF, BTI, TDDB, Threshold Voltage

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