Investigation into trapping mechanisms and impact on performances and reliability of GaN HEMTs through physical simulation and electro-optical characterization

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INVESTIGATION INTO TRAPPING MECHANISMS AND IMPACT ON PERFORMANCE AND RELIABILITY OF GaN HEMTS THROUGH PHYSICAL SIMULATION AND ELECTRO-OPTICAL CHARACTERIZATION

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For Baba, and Ma

…and Rishab.

One sees great things from the valley,

Only small things from the peak.

Gilbert. K. Chesterton

From error to error,

One discovers the entire truth.

Sigmund Freud

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Abstract

Gallium Nitride has emerged as a terrific contender to lead the future of the semiconductor industry beyond the performance limits of silicon.

The immense potential of the AlGaN/GaN HEMT device derives from the high density, high mobility electron gas formed at its hetero-structure. However, frequent subjection to high electric field, temperature and stress conditions makes the device vulnerable to reliability issues that restrict its efficiency and lifetime. A dominant contributor to several parasitic and reliability issues are traps present within the semiconductor structure which restrict the channel density and aggravate the static and dynamic device response. As the GaN industry addresses an increasing demand for superior devices, reliability analysis is of critical importance. There is a necessity to enable advancements in trap inhibition which would allow the realization of stronger, efficient devices.

The motivation of this work is to recognize distinct ways in which various traps affect the performance and reliability metrics of 0.25 μm GaN HEMTs through a study of devices of the GH-25 process optimized for high power applications up to 20 GHz. The investigation employs physical TCAD simulations to provide insight and perspective to electrical and optical characterizations. Detailed analysis into independent and interrelated effects is performed to identify the relative impact of traps in circumstances presenting notable deviations from the ideal device response.

The methodology to develop a representative TCAD model derived closely from internal physics is described with special focus on the sensitive gate leakage characteristic which reflects the influence of fundamental physical processes as well as parasitic effects commonly encountered in GaN HEMTs. Targeted simulations provide a pivotal link between the observation of a reliability issue and its underlying origin in trapping phenomena. Establishing associations between the spatial location of traps and the degradations they could trigger is an important objective of this thesis.

Several simulation strategies that explore trapping behavior in various steady state and transient environments are discussed which allow detailed perception into the manner and extent to which trap attributes affect operational considerations. Approaches to distinguish disparate trap interactions are also described. The central case study in this thesis is an abstruse parasitic leakage phenomenon, identified in the GH 25 process as a consequence of aging stress. Referred to as the "belly shape", it presents an interesting example of how the developed strategies can be applied to discern the causality, impact and evolution of the responsible traps. In order to take a deeper look into trapping modes, further aging and LASER characterizations are performed to alter the general occupational dynamics and observe the modulation of trap control over device response.

Résumé

Le Nitrure de Gallium est devenu un matériau incontournable pour le développement de dispositifs semi-conducteurs aux performances très supérieures aux composants silicium.

L'immense potentiel du dispositif HEMT AlGaN / GaN provient du gaz d'électrons à haute densité et à forte mobilité formé au niveau de son hétéro-structure. Cependant, le fonctionnement sous champ électrique, température et conditions de stress élevés rend le dispositif vulnérable aux problèmes de fiabilité qui limitent son efficacité et sa durée de vie. Les pièges présents dans la structure, qui limitent la densité porteurs du canal et pénalisent la réponse du dispositif, constituent le facteur majeur déterminant plusieurs effets électriques parasites et la fiabilité du dispositif. L'industrie du GaN est confrontée à la nécessité de disposer de dispositifs de haute fiabilité si bien qu'il est nécessaire de faire des progrès dans l'analyse de l'impact des pièges pour en déduire des solutions technologiques permettant leur inhibition.

La motivation de ce travail est d'identifier les signatures électriques associées à l'activité de différents pièges ainsi que leurs conséquences sur les performances et la fiabilité des HEMT GaN grâce à une étude dédiée des dispositifs de la technologie GH-25 conçue pour des applications RF de puissance fonctionnant jusqu'à 20 GHz. L'étude utilise des simulations physiques TCAD. Une analyse détaillée des effets indépendants et interdépendants est réalisée afin d'identifier l'impact relatif des pièges pour des études de cas où les caractéristiques électriques présentent des écarts importants par rapport à la réponse idéale du dispositif.

La méthodologie utilisée pour développer un modèle TCAD représentatif et dérivé de la physique interne est décrite en accordant une attention particulière au courant de fuite de grille qui reflète l'influence de processus physiques fondamentaux ainsi que les effets parasites couramment rencontrés dans les dispositifs GaN. Les simulations ciblées établissent un lien entre l'observation d'un problème de fiabilité et son origine sous-jacente dans les phénomènes de piégeage. L'établissement d'associations entre la localisation spatiale des pièges et les dégradations qu'ils pourraient provoquer est un objectif important de cette thèse.

Plusieurs stratégies de simulation sont présentées, permettant d'explorer le comportement des pièges en régime permanent et en régime transitoire et donnant une perception détaillée de la manière dont les paramètres des pièges affectent les caractéristiques opérationnelles. Des approches pour distinguer les interactions de pièges différents sont également décrites. L'étude centrale de cette thèse est un phénomène de courant de fuite parasite complexe, identifié dans le procédé GH 25 comme conséquence du vieillissement accéléré. Connu sous le nom de «belly-shape», il représente un

exemple intéressant de la façon dont les stratégies développées peuvent être appliquées pour discerner la causalité, l'impact et l'évolution des pièges responsables du phénomène. Afin d'approfondir l'analyse des modes de piégeage, nous avons procédé à des tests de vieillissement accéléré et des caractérisations électro-optiques afin de modifier la dynamique générale du mécanisme de piégeage et d'observer la modulation du mécanisme du piégeage sur la réponse du dispositif.

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INTRODUCTION

Primarily rooted in its superior material characteristics, extensive and diverse research is being targeted at viability of GaN based systems for not only commercial or industrial requirements, but also for niche consumer-specific demands. GaN is exceptionally robust, with high tolerance to temperatures and voltages in addition to being highly relevant in high power and frequency domains. GaN based systems are predicted to occupy a significant share of the semiconductor market over the next decade and promises huge economic advantages with continued development.

Large-scale investments, for e.g. by Google and BMW, have been undertaken into optimizing GaN based technologies for implementation into varied circuit architectures and packaging solutions that could set qualification criteria for the next phase of research and manufacturing chain roadmap towards exciting and novel objectives.

The AlGaN/GaN HEMT has exceptional possibilities for different applications owing to the AlGaN/GaN hetero-structure which enables a high mobility and high density channel. Because of the piezoelectric and spontaneous polarization charges at the interfaces, the two-dimensional electron gas can reach high densities without requiring external bias or doping. The prospects of the GaN HEMT are however threatened by degradation mechanisms that limit performance and worsen the reliability and lifetime. The distinctive physical features that enable the advantages of these devices also complicate reliability investigations of GaN HEMTs because of singular reliability issues that do not affect other semiconductor technologies such as Si-based processes. Currently, a central focus of GaN research is to better understand inconsistencies or weaknesses that plague GaN systems to then develop apropos counteractive techniques.

A dominant contributor to several parasitic and reliability issues are traps present within the semiconductor structure which restrict channel density and aggravate the device response. At this juncture of the GaN industry, addressing an increasing demand for better devices, efficient reliability analysis is of critical importance. Significant advances in performance figures of HEMTs have been made by research institutions and industrial corporations despite trap induced limitations which have well-demonstrated the promise of GaN-based devices. To sustain the acceleration in GaN markets however, there is a need to build transistors capable of capitalizing on the true potential of III-N materials. This necessitates advancements in understanding and inhibiting trap effects.

This work addresses the impact of trapping phenomena on device performance and reliability through multiple outlooks at major factors such as spatial location, energy and density that control the relevance of traps within the HEMT structure at specific conditions.

Chapter 1 is an introduction to the GaN material, the AlGaN/GaN HEMT and the degradation issues that weaken the device efficiency. It summarizes briefly the current trends in the GaN market and its major application areas. Then the basic features of the III-N semiconductors and their advantages over conventional semiconductor systems are discussed. The polarization charges which are one of the most important physical features of the lateral GaN HEMT is reviewed in detail. The general structure, fundamental operation and conduction mechanisms of the AlGaN/GaN HEMT are presented including constraints governing the composition and thickness of the barrier layer. The GH-25 process details and basic performance results are presented as an introduction to the subject devices of this work. Then, the different origins of degradation in GaN HEMTs and the reliability issues that manifest as a consequence are introduced. Finally, reliability issues more relevant to the GH-25 process devices are introduced, including the belly shape effect.

Development of accurate design methodologies for device processes involves diverse approaches to account for variability, robustness and operational or environmental boundaries. Testing and modeling are both critical to this often iterative process of device development, to ensure standards of quality and performance as a viable technology. Many semiconductor companies rely on TCAD to explore process variations and design choices to maximize productivity and performance metrics through intensive and accurate modelling instead of lengthy and abstract tests. Thus, it is a highly efficient and inexpensive method to set parameter standards, and development targets. Simulations that provide an in-depth look at the internal physics of modelled devices under varying constraints are highly useful in recognizing factors that might exacerbate device weaknesses.

Chapter 2 explains the general TCAD simulation approach that has been adopted in the work towards study of the GaN HEMT devices. The essential steps to building a physics based 2D drift diffusion based model that reproduces the behavior of a real device are described based on parameter-induced modulations of the leakage characteristic which precisely reflects the individual impacts of each model parameter. In addition to identifying thresholds and valid ranges for fundamental parameters that are mandatorily required to build a GaN HEMT model, a detailed study of tunneling and trap effects is also performed, with special focus on the recognition of the relative impact of each trap type on the gate current. The consistency of the methodology is verified through the simulation of different versions of the GH 25 process. This also serves to demonstrate the capability of the extracted model parameter sets to allow effective performance comparisons through

the distinctive features of each dedicated set. Finally, a brief comparison between hydrodynamic and drift diffusion model is performed, substantiating the choice of the drift diffusion transport model.

Chapter 3 continues the discussion into simulation methodologies, but on an improved model structure that better represents the GH-25 process. Two major transient simulation approaches are discussed which investigate the capacitance-voltage and on-resistance characteristics. The gate capacitance characteristic is classified into four regions and the relative impact of each kind of trap on different regions of the characteristic is compared to the ideal device response to link possible degradations with individual trap impacts. For the on-resistance study, the changes in trap control when pulsing parameters are varied to alter the device's response capability are reported. Thus, the focus is on recognizing and more importantly, distinguishing disparate trap interactions that lead to worsening characteristics. Such correlations help to extricate the primary root from often superimposed trap effects and allow directed strategies to minimize their impact, dependent on relative significance with respect to the constraints of specific application scenarios. It also provides information on the physics of trapping occurrences and interpretation of experimental observations.

Chapter 4 is a detailed study into the belly shape effect, which is a gate leakage artifact observed in the GH-25 process devices after aging tests. It introduces the unique attributes of this anomaly, a review of previous characterizations and builds initial hypotheses that form the core of simulations performed to reproduce this phenomenon for the first time. Based on simulation results and re-characterizations on belly shape devices after 3 years of inactivity, an explanation for underlying causes of this effect is proposed. The hypotheses are further supported by simulations that interpret unpredictable evolution of the belly shape magnitudes during aging tests. The techniques developed in Chapter 3 are applied to add to the discussion of possible impacts of the causal mechanisms behind belly shape. A second round of aging tests is performed to stress the devices further and observe associated responses, reflective of the damage potential of belly shape.

Chapter 5 presents electro-optical measurements that utilize laser beams to trigger trappings or de-trappings in belly shape devices. The approaches include applying the laser with increasing energy content in order to allow a gradual de-trapping in trap constituents with shallower energies towards deeper energy locations. It details the effects of applying trap filling stresses prior to laser application which boost the strength of the de-trapping transient but also activate shallow traps with very small time constants. Optical beam induced current (OBIC) technique is used to image some of the test devices to visualize defect locations. This discussion provides insight into occupational dynamics of trapping phenomena under steady state and stressed conditions and acts as a corroborating tool towards hypotheses to interpret device characteristics.

CHAPTER 1

GaN Industry and Reliability

STATUS AND TRENDS

Exceptional performance advances of GaN based devices are being reported across market-driven fields such as high frequency communications, photonics, RF power devices, high power conversion and control, which aids corporations and commerces in sustaining the rapidly evolving demands for higher metrics. The inherent robustness capably addresses modern markets for compact, rugged and highly reliable devices such as in automotive, defense and space applications. GaN engineering is promising not only in meeting key performance needs, but also for the potential for sustained economic rewards on maturity.

The RF GaN market has continued to grow with high momentum reaching mainstream status with a market estimation of US$ 380 million at the end of 2017 [1.1]. 5G network operations should prompt another breakout boost by 2020 which leads the way to a forecasted value of US$ 1.3 billion by 2023. The GaN power device segment is crucial with a worth of US$ 12 million in 2016 which is projected to reach an explosive US$ 460 million by 2022 [1.2]. The global GaN market is estimated to reach US$ 4 billion by 2024 [1.1-1.5] according to several market analyses.

The first depletion mode radio frequency (RF) GaN HEMT was introduced around 2005 by Efficient Power Conversion Corporation (EPC) [1.6]. The first commercial 200 V e-mode GaN devices were released in 2010 followed by the first devices for 650 V in 2014 [1.5]. The current GaN device market is still controlled by < 200 V applications but 600 V devices are slowly becoming relevant, estimated to be valued higher than US$ 200 million and US$ 50 million respectively as MOSFET devices progressively start being substituted [1.7]. 1.2 kV and higher voltage devices are also expected to contribute significantly to the market share in the next few years.

This chapter addresses the current state of the GaN industry centered on the major players and applications in the RF and power domains. Fundamental physics of III-N materials, especially polarization effects, and operational basics and relevance of the GaN-based high electron mobility transistor are discussed. The UMS GH-25 technology is introduced to describe the key attributes of the devices that form the subject of this work. Finally, the primary reliability issues plaguing GaN HEMTs are reviewed, with special focus on effects associated directly with the GH-25 technology.

1.1 Growth of Industry

A. POWER DEVICE MARKET

Core necessities for a successful power semiconductor technology are efficiency, reliability and cost efficiency. In 2009, EPC launched the first enhancement-mode GaN (eGaN) field effect transistor (FET) intended for power MOSFET replacements [1.6]. The market for GaN has since grown tremendously. Figure 1.1 presents the current distribution and projection of the power market. The key organizations leading the first generation of reliable power GaN production towards innovative territories are Transphorm, Infineon, EPC, Navitas, Dialog and GaN Systems [1.2, 1.5].

They display impressive specifications and notable improvements over silicon in regard to current handling, switching frequencies and breakdown voltages while having varied outlooks for manufacturing process and design.

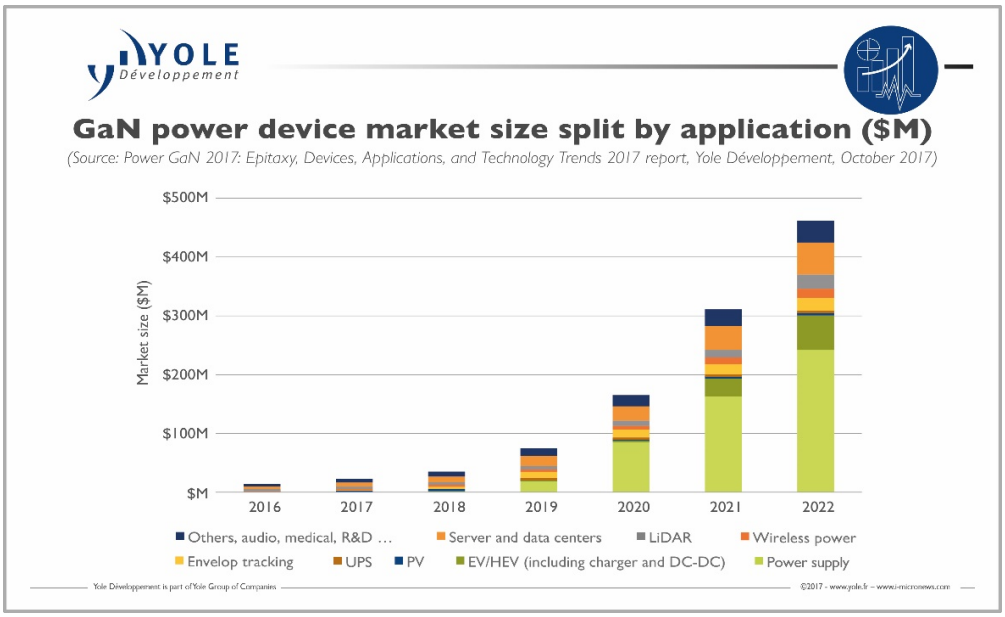

Figure 1.1: Predictive GaN power market breakdown [1.2] compiled in 2017 for contributive applications including power supply, wireless power, Electric/Hybrid Electric Vehicles (EV/HEV), uninterruptible power sources (UPS), Photovoltaics (PV), data centers and others.

Power supply is expected to remain a major player driving the growth into 2022. LIDAR (light detection and ranging) along with wireless power and envelope tracking are profitable additions to low/medium voltage segment since GaN is uniquely suited to managing their specific needs. Velodyne LIDAR is accelerating the development of 3D sensors for manufacturing and wireless charging solutions are being proposed from companies like EPC, Apple and Starbucks. Not just as power converters for general automobiles, the GaN market for the Electric and Hybrid Electric Vehicle (EV/HEV) could be highly relevant in the near future due to the high speed switching efficiency strengths of GaN. As the EV segment expands, vehicle-charging needs will open up needs for intelligent switching in local power distribution grids. By extension, the huge software framework required to support autonomous driving again will demand highly efficient power conversion. Transphorm with its automotive qualification could lead the way for GaN production in this sector. For data centers, EPC and Texas Instruments offer great products. GaN power IC implementations are also promising for laptops or smartphones.

The performance advantages of GaN provide opportunities for high return of initial investment as well as running profits, which is prioritizing research into the next phase of manufactured devices as can be seen from Figure 1.2.

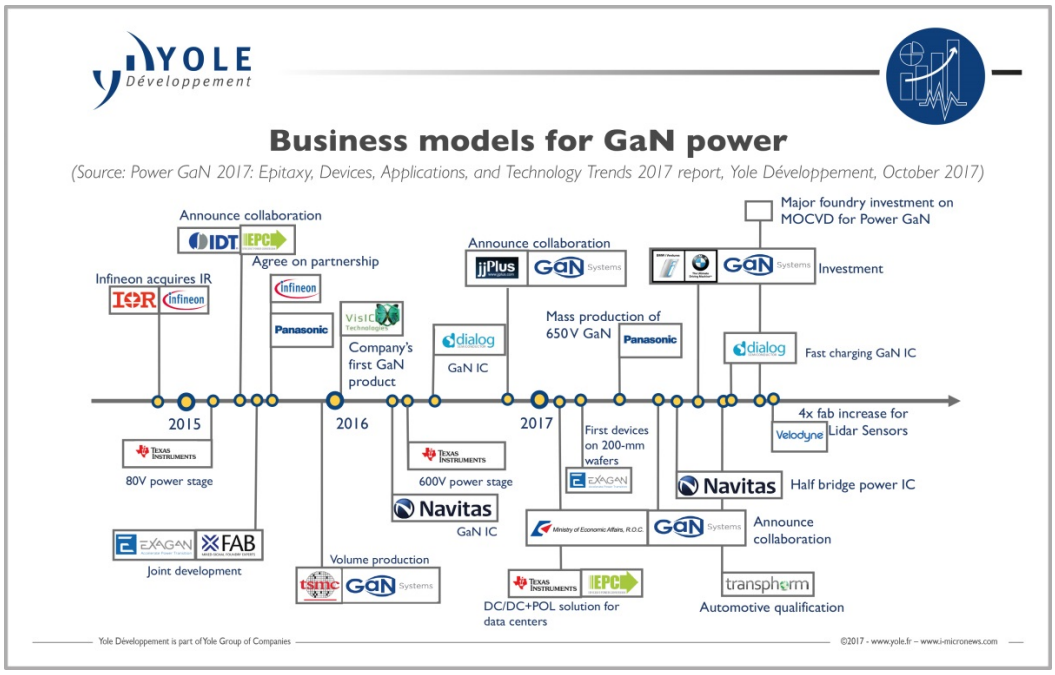

Figure 1.2: Business investments into GaN power by corporations compiled in 2017 [1.2].

Commercially viable large area substrates are very close to being launched for power conversion applications. Foundries are optimistically pursuing mass production of GaN devices by

undertaking huge investments into handling and fabrication capacity such as the recent Navitas partnership with TSMC and Amkor. Panasonic has announced large scale production of its 650 V devices while several other companies are in final R&D stages, expected to soon be ready for debut. In collaboration with GaN Systems, which recently secured an investment from BMWi Ventures, the Taiwan's Ministry of Economic Affairs is encouraging GaN applications for green energy.

B. RF DEVICE MARKET

The RF market has been central to initial interest and research into GaN development and continues to flourish with novel industrial solutions. Both established and upcoming corporations are involved in production, such as Sumitomo Electric, Infineon, Wolfspeed, Qorvo, NXP Semiconductors, Mitsubishi Electric, GaN Systems, United Monolithic Semiconductors (UMS), M-A/COM, Ampleon, RFHIC, Northrop Grumman, and Anadigics [1.1, 1.8].

As presented in Figure 1.3 telecommunications and military are central markets of RF GaN technology. GaN can sustain very high power to efficiency levels; much superior to existing Si laterally diffused metal oxide semiconductor (LD MOS) or GaAs solutions, which offers a critical advantage for high frequency telecom networks.

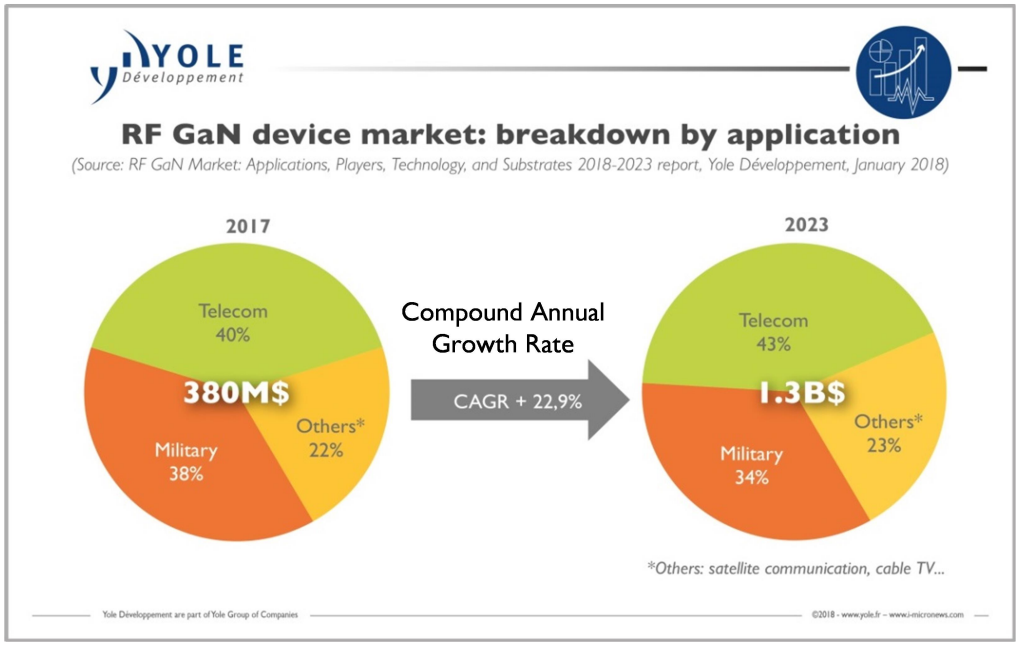

Figure 1.3: GaN RF market breakdown by application compiled in 2018 [1.1] including contributions from the major telecom and military sectors predicting an annual growth rate of 23% to reach an estimated worth of 1.3 billion dollars by 2023.

The different sectors of RF power are wireless infrastructure, wired broadband, satellite communications, coaxial and fiber cable, military and aerospace. In the near future, GaN is ideal for

power macro base station amplifiers, requiring high frequencies, thus disadvantaging LDMOS, and high power, which is detrimental to GaAs operation. Its high bandwidth offers broadband capacities towards novel application genres like multi-band carrier aggregation. Mass production is crucial with a need for more transistors at higher frequencies, due to reduction in unit coverage of base stations. In addition, scientific and medical radio band applications are also relevant.

Devices have already been implemented for utilization in Cable TV, base transceiver stations and very small aperture terminal (VSAT) satellite ground stations. Next generation aerial and terrestrial radars under US Department of Defense have incorporated GaN devices supporting better resolution and longer detection ranges. They are also being used for anti-improvised explosive device or anti-IED systems [1.8].

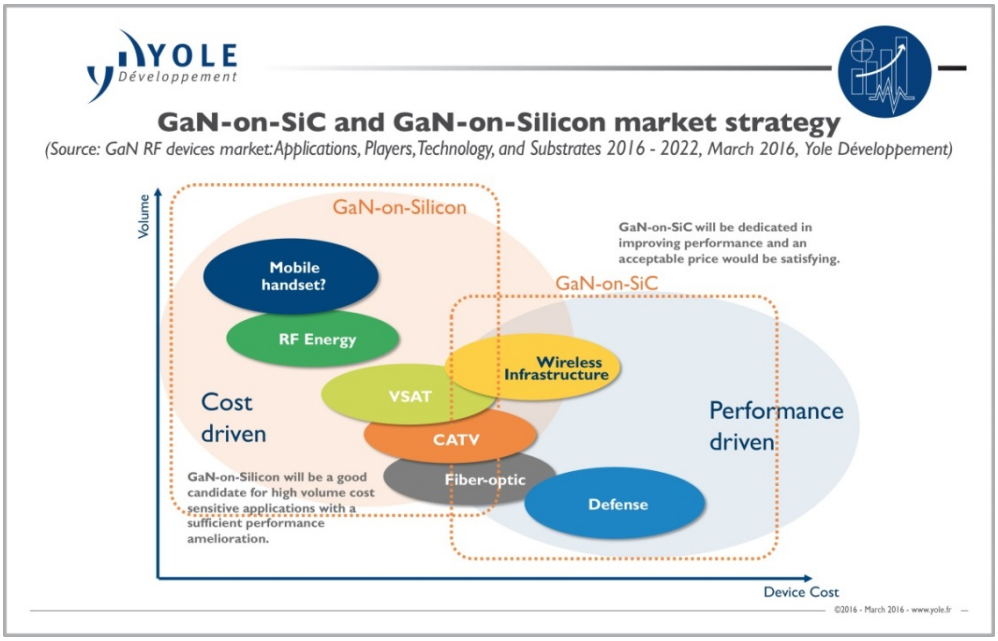

Figure 1.4: GaN RF application breakdown by substrate markets as compiled in 2016 [1.9]

As demonstrated in Figure 1.4, two major technologies GaN-on-SiC and GaN-on-Si, cater to differing sectors. GaN-on-SiC is used in the majority (> 95 %) of commercial GaN infrastructure [1.8]. It has matured rapidly, and provides higher performance standards, though cost continues to be a limiting factor. Packaging issues contribute to cost drawbacks of implementation.

Qorvo and GaN Systems amongst others are dominantly pursuing GaN-on-SiC for further innovations while M/A-COM has launched their Gen4 GaN-on-Si for highly cost efficient base stations. These devices will have access to the widespread low cost, wide wafer Si and CMOS foundries. Pending further improvements however, GaN-on-Si will remain a minor challenger to SiC substrate processes.

1.2 Introduction to GaN Physics

A. MATERIAL ADVANTAGES

Nitrides of III group-semiconductors exhibit some fascinating properties giving AlN and GaN huge advantages towards high power and high frequency applications. Figure 1.5 presents inherent properties of the III-N semiconductors enabling specific advantages.

Property	Si	GaAs	SiC	GaN
Bandgap E_g (eV)	1.12	1.42	3.25	3.4
Intrinsic Carrier Density n_i (cm^{-3})	1.45×10^{10}	1.79×10^{6}	1.16×10^{-8}	1.67×10^{-10}
Breakdown Field E_{BR} ($MV\ cm^{-1}$)	0.3	0.4	3.5	4.0
Separation energy (eV)	Indirect	T-L 0.29	Indirect	T-T' 1.9, T-M 2.1
Johnson's figure of merit (~ Si)	1.0	2.7	20	27.5
Baliga's figure of merit (@ E= 500 kV/cm)	1.0	9.6	3.1	24.6

Direct, Wide Band-Gap

- High temperature tolerance and radiation hardness
- High breakdown voltages (αE_g^2) » High efficiency
- High density of optical storage ($\alpha \lambda^{-2}$)

High Power/ Unit Width

- Simpler matching circuits
- Smaller devices » no power combining » lower chip and system costs

	Si	GaAs	SiC	GaN
Saturated Drift Velocity v_d ($\times 10^7$ cm s^{-1})	1.0	2.0	2.0	3.0
Electron Mobility μ ($cm^2V^{-1}s^{-1}$)	1350	6000	650	1000-2000
Thermal conductivity κ ($W\ cm^{-1}\ K$)	1.5	0.5	4.9	1.7

Wurtzite Lattice → High Bond Strength → Stronger Ionicity

- Chemical stability at higher temperatures
- High thermal conductivity » Better heat dissipation
- Better electron transport properties, high gain and polarization charges
- High electron velocity » High *f* operation, high bandwidth, low noise

	Si	GaAs	SiC	GaN
Supports hetero-structure formation	No	Yes	No	Yes

Enabling of AlGaN/GaN Heterostructure

- Simultaneous high I, high V and low R_{on} operation owing to 2-DEG
- High operating voltage » No voltage conversion & high efficiency
- High Efficiency » Less power consumption » Simpler cooling systems

Figure 1.5: Properties and advantages of III-Nitride semiconductors in comparison to other semiconductor candidates at room temperature [data taken from 1.10-1.12]

GaN, being a direct bandgap semiconductor, has an explicit relevance in optoelectronics allowing for luminescence at high intensities. The wide energy bandgap (E_G) supports high density optical storage technologies (≥20 GB) thus allowing full color display while reducing power consumption by 10 to 20 times. Blue (or ultraviolet) GaN lasers reinforce storage capacity by 4 times in comparison to GaAs infrared radiance [1.11-1.12]. About detectors, E_G maintains efficiency in the ultraviolet spectrum while blocking visible radiation, which enables UV imagery.

Because of the wide E_G (GaN= 3.4 eV, AlN= 6.2eV), these materials have low intrinsic carrier concentrations until 1000^0C making them rugged and reliable with very high temperature and voltage tolerances. Associated systems can thus withstand higher junction temperatures and present breakdown voltages V_{BR} beyond 1 kV. The Wurtzite lattice structure comprises of strong bonds which further promotes high robustness and long term stability. This promotes several automotive and aircraft applications such as high power and high voltage rectifiers or converters.

A critical tradeoff exists between the breakdown voltage V_{BR} of the transistor and the cut off frequency f_T. This stems from increase in the electric field E as the carrier transit time τ is shortened, thus requiring a corresponding lowering of the applicable voltage. The derivation of this tradeoff [1.12] is described where E_C is the critical electric field and the electron path is represented by l.

$$V_{BR} = E_C \times l \tag{1.1}$$

$$f_T = \frac{1}{2\pi\tau} = \frac{v_{sat}}{2\pi l} \tag{1.2}$$

$$V_{BR} \times f_T = \frac{E_C v_{sat}}{2\pi} = const. \tag{1.3}$$

Hence, the product is a constant, referred to as the Johnson's figure of merit (JFM). To create electron hole pairs for impact ionization, hot carriers need to obtain an energy equivalent to E_G. The wide bandgap of GaN thus, similar to SiC, enables a very high E_C. In addition, the saturation velocity v_{sat} is also substantially higher for GaN because of the large energy separation between the conduction band valleys, which restricts inter-valley transitions under high electric fields [1.12]. Thus, this gives GaN superior JFM values in comparison to Si and GaAs. The Baliga's Figure of Merit [1.10] for resistive losses is defined as BFOM= $\varepsilon\mu_e E_C^3$ where GaN again excels unlike SiC which suffers due to low electron mobility [1.6].

Thus, GaN devices have the potential to dominate the power electronics market because of their ability to operate at high frequencies and high power [1.13-1.14]. The material power density itself is 10 times that of GaAs devices [1.11]. The associated high power per unit width translates into easier fabrication and smaller devices with high impedance, in turn making them easier to match into

the system. In comparison, a matching ratio 10 times higher might be necessary for a GaAs transistor [1.11]. In addition the need for voltage and power conversion is also obviated. The high thermal conductivity helps with reducing the need for expensive and complex cooling systems. This is especially significant because the cost and weight of cooling systems constitute an important portion of the building costs of a high power microwave transmitter. The achieved overall compactness of weight, volume and cost is also crucial for space-targeted devices. Also, this makes GaN strategically competent to counteract global warming through utilisation in major production systems.

The high E_C in association with the ability to form a hetero-structure and a conducting two dimensional electron gas (2DEG) channel at V_G= 0V due to polarization charges, provides simultaneous high current, high voltage operation and low R_{on} (< 50 mΩ @ 30 A) [1.12]. It is possible to build greatly efficient (> 99%) and smaller, cost effective systems with high breakdown voltages ensuring high working voltage under off conditions.

The high electron velocity v_d provides higher efficiency, bandwidth and linearity, substantiating the RF and microwave performance of III-N devices through superior cut-off frequencies. Because of high gain coupled with v_d, GaN based systems also have low noise figures. Minimal carrier scattering and the low R_{on} × gate charge product leads to reduced RF and switching losses for applications in the low to medium voltage ranges [1.12]. Due to superior R_{on} to V_{BR} ratios under identical on-resistance R_{on} conditions, the superior switching capability of GaN will yield significantly lower losses than a Si device [1.6]. Thus, the driving needs of RF power applications such as the ever-expanding wireless communication field are well achieved. This domain is also strategic for military, civil and space applications such as C band satellite communications, Ku-K small aperture terminal, and digital radio and radar systems [1.10].

B. SUBSTRATES

There are three dominant substrate choices for GaN epitaxy processes each with its set of tradeoffs and advantages. Figure 1.6 presents the salient advantages and disadvantages of each.

Sapphire

Sapphire which is single crystal aluminum oxide was the first substrate used in the pioneering work by Maruskas and Tietjen in GaN epitaxy in 1969 [1.15]. Its large lattice constant mismatch (+16%) with GaN leads to high dislocation density (10^{10} cm^2) [1.16] in the epitaxial film reducing carrier mobility, minority carrier lifetime and thermal conductivity. Further, due to a high coefficient of thermal expansion (greater than GaN by 30%) biaxial compressive stress develops in the grown layer as it cools from deposition temperatures, which can lead to cracking. Owing to low thermal

conductivity (about 0.25 W/cm. K at 100°C), heat dissipation is not optimal, making sapphire unfit for power applications [1.13]. However, a lot of research was undertaken into developing sapphire as a substrate, which led to its initial success. GaN is usually grown on the c-plane of sapphire resulting in c-plane oriented films but with the [0001] plane of GaN rotated by 30° relative to the sapphire. This reduces the lattice mismatch from 30% to 14% [1.14]. A drawback is that cleavage planes of epitaxial GaN are not parallel to sapphire, inhibiting laser facet formation. Also, because sapphire is insulating, only front side electrical contacts are feasible, reducing the area available for device structures and complicating device fabrication. In addition, oxygen from sapphire could be a source of unintentional doping in GaN [1.18].

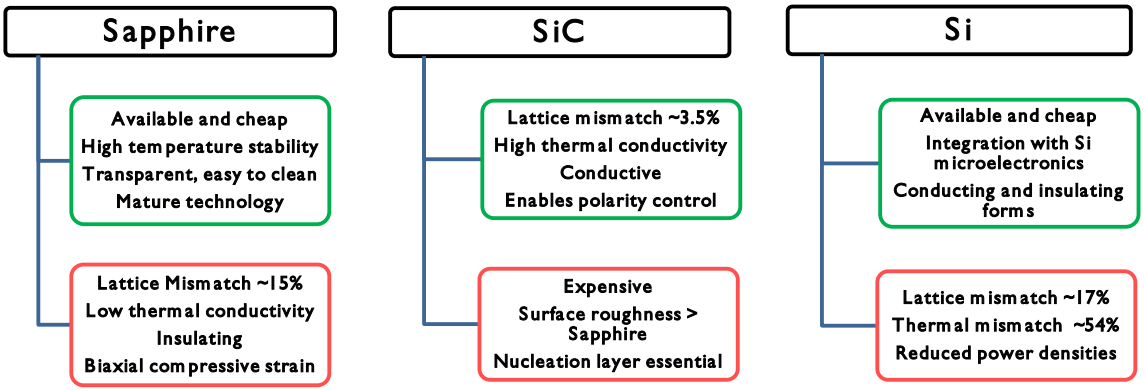

Figure 1.6: Advantages and disadvantages of substrate choices for GaN epitaxy

Silicon Carbide

The SiC material has over 250 different poly-types, which represent one-dimensional variations in the stacking sequence of close-packed bi-atomic planes [1.19]. For epitaxial growth of GaN however, the 4H and 6H poly-types are commonly used. "H" stands for hexagonal crystal symmetry and the numbers refer to the number of layers of Si and C atoms before the atomic arrangement is repeated. SiC is a polar material and hence advantageously available in both polarities affording more control. Generally speaking, Si terminated SiC results in Ga-face polarity of the GaN film and C-terminated SiC gives N-face polarity [1.20].

The roughness of the SiC substrate (generally ~ 1nm root mean square (RMS) compared to 0.1nm for sapphire), couples with damages during the polishing process (propagating into the epitaxial film from the surface) as well as strain and dissimilarities in thermal expansion. Hence, despite the lattice mismatch of only 3%, high dislocation densities in the order of $10^9 - 10^{10}/cm^2$, similar to GaN films on sapphire [1.13-1.14] is formed. Different pre-treatments like wet/dry etching or annealing are now being used to counter these effects. Furthermore, GaN and AlN nucleation

layers are being used to improve the quality of the epitaxial film though it increases the device to substrate resistance. Because the thermal expansion coefficients of SiC are smaller than those of GaN, most epitaxial films grown are under tensile strain. However, the amount of strain and sometimes even its sign can be strongly controlled by adjusting the nucleation layer. Its high thermal conductivity (3.8 W/cm. K) makes SiC an optimal choice for high-power applications although it is expensive. Semi-insulating, n and p-type substrates are available and preferred for SiC and AlGaN based power microwave devices. Conductive substrates make electrical contacts to the backside of the substrate possible, thereby simplifying the device structure compared to sapphire substrates. The crystal planes in epitaxial GaN parallel to those of the SiC substrate, making facet formation through cleaving much more practical.

Silicon

Silicon is a low cost and well-established technology, which brings the advantages of precise doping, thermal stability and the history of experienced research into its viability for GaN [1.10]. The crystal perfection and surface finish quality is better than any other substrate competitor for GaN. However, GaN epitaxial layers on Si have substantial drawbacks to quality arising from large variations in lattice constant (-17%) and thermal expansion coefficients (+50%) with dislocation densities ranging around 10^{10} cm^{-2} [1.21]. Further, Si tends to form amorphous layers of silicon nitride on exposure to atomic nitrogen. Buffer layers deposited on Si substrates alleviate the lattice constant mismatch while improving wetting and reducing Si reactivity. Both zincblende and wurtzite GaN epilayers [1.22] have been grown on the Si (001) by different growth techniques and several applications including HEMTs and detectors [1.10, 1.21-1.24] have Si substrates, especially Si (111).

Gallium Nitride

Gallium nitride itself would be the ideal substrate for homo-epitaxial device fabrication, since that would automatically obviate heteroepitaxy related issues [1.25, 1.13]. Using GaN would enable stronger and easier control of crystal polarity, dopings and stress quantities. The associated mismatches in lattice constants and thermal expansion coefficients would be negligible thus obviating the need for buffer layers or nitridation as required for hetero-epitaxy.

However, GaN still needs substantial optimization before the other substrates can be replaced. The process to synthesize GaN in bulk is complicated, because of the very high melting point of GaN ~ 2800°C [1.26]. At high temperatures, the vapor equilibrium pressure of nitrogen is very high and high pressures are needed (2000 bar) to incorporate N and finally grow GaN. The technique is to grow very thick (>100 μm) layers by Hydride Vapor Phase Epitaxy (HVPE) and to

use them as "quasi" substrates [1.27]. While other techniques are employed for producing bulk GaN crystals, only high-pressure growth from solutions such as HVPE have produced large area crystals. The ammono-thermal method is however proving to be a good contender to HVPE [1.28]. Despite the low quality and defect densities that would eliminate other technologies, the power and reliability metrics make GaN still promising for the future pending further research.

C. III NITRIDES LATTICE STRUCTURE AND POLARIZATION

Group III nitrides are compound semiconductors consisting of a group III element (Al, Ga, In) and Nitrogen (N) as well as the associated alloys. Though InGaN is promising to FET applications, its potential is limited by technological issues due to a considerable difference in ion sizes of In and N. GaN and AlGaN thus dominate the research and market of the III-N industry.

The group III-nitrides AlN, GaN and InN crystallize in three crystal structures. However, Wurtzite is the thermodynamically stable phase under ambient conditions. It consists of two interpenetrating hexagonal close packed lattices [1.29-1.30] shifted ideally by $3/8.c_0$ with respect to each other where c_0 is the lattice cell height. N, being the smallest and most electronegative Group V element, is what makes III-N devices unique among the other III-V compounds. Because of the N atom electronic configuration with a lack of electrons in the outer orbitals, the metal to nitrogen covalent bond electrons feel a strong attraction toward the N atomic nucleus due to Coulomb potential. Hence, although predominantly covalent with tetrahedral bonding; the large difference in electronegativity of Ga and N atoms gives an ionic (significant compared to other III-V compounds) nature to the Ga-N (III-N) chemical bond leading to a strong cohesive structure.

Spontaneous Polarization

The unit Wurtzite lattice has four atoms, two of each kind. However, there is no inversion symmetry in the lattice along [0001] direction (c-axis). This means that all the atoms on the same plane on either side of the bond are the same. Hence, grown GaN has two characteristic crystal structures: Ga-face and N-face. In addition, the discussed ionicity, inherently a microscopic polarization, results in a strong macroscopic polarization (along [0001] axis) when the crystal lacks inversion symmetry. The analogous effect in [111] direction of GaAs and Indium Phosphide (InP) is less relevant since the covalent bonds are less ionic. This kind of polarization effect occurs within the equilibrium lattice without any strain or bias. Hence, it is called spontaneous polarization P_{SP} [1.29].

The orientations of P_{SP} are presented in the following Figure 1.7 where c_0 and a_0 are the height and edge length of the equilibrium lattice. Ideally (for a Wurtzite lattice) $c_0/a_0 = 1.633$. The degree of non-ideality determines the strength of polarization in III-Nitrides [1.31-1.32]. Although

the covalent bond parallel to c-axis is strongly ionic and primarily responsible for P_{SP}, the other three covalent bonds in the tetrahedral structure are also ionic and their resultant spontaneous polarization aligned in the opposite direction serves to counteract the polarization of the other bond.

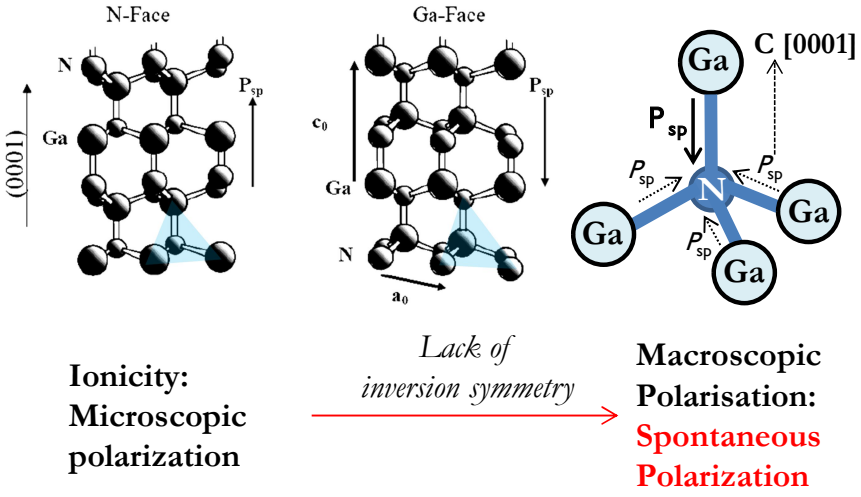

Figure 1.7: Tetrahedral bond-structure of Ga-face and N-face hetero-structures and the alignment of P_{SP}

When c_0/a_0 decreases, c_0 decreases and a_0 increases, the three covalent bonds are spread wider from the c-axis and the resultant compensation polarization decreases. Hence, the macroscopic dominant P_{SP} increases. Table 1.1 shows that c_0/a_0 for GaN is closest and for AlN farthest from the ideal value. As c_0/a_0 ratio moves away from 1.633 of the ideal lattice, the value of P_{SP} increases from GaN to InN to AlN [1.29]. Also, as seen above, the directions of P_{SP} in the N-face GaN Wurtzite structure and Ga-face GaN Wurtzite structure are opposite. The orientation of polarization is defined assuming that the positive direction is from the metal i.e. cation to the nearest neighboring nitrogen atom i.e. anion along the c axis. Hence, the resultant spontaneous polarization P_{SP} for III-N materials with the orientation as displayed in Figure 1.7 is always negative [1.32].

Table 1.1: Lattice parameter c_0/a_0 and P_{SP} variations across the Group III Nitrides [1.29]

Parameter	Ideal Wurtzite	AlN	InN	GaN
c_0/a_0	1.633	1.6010	1.6116	1.6259
P_{SP} (C/m^2)	--	-0.081	-0.032	-0.029

Piezoelectric Polarization

If the non-ideality of the lattice is altered externally thus triggering a change in c_0/a_0, the strong ionicity of the GaN bond can generate large changes in crystal polarization. When stress is applied to the III-nitride lattice, c_0 and a_0 of the unit crystal are compelled to change accordingly.

Correspondingly, the polarization strength changes as well. This additional polarization in strained III-nitrides is called piezoelectric polarization P_{PE} [1.29]. Under biaxial compressive stress, the in plane lattice constant a_0 decreases and the vertical lattice constant c_0 increases. Hence, c_0/a_0 increases towards the ideal value of 1.633 and total polarization strength of the crystal decreases as the P_{PE} and P_{SP} act in opposite directions. Conversely, if tensile stress is applied to the crystal, total polarization increases as P_{PE} and P_{SP} act in the same direction [1.11, 1.29].

To elaborate mathematically, the relationship between stress S and strain T can be represented in C_{6v} point group as follows where C_{ijkl} are stiffness constants [1.33].

$$T_{ij} = C_{ijkl}S_{kl} \quad , T_j > 0: tension, T_j < 0: compression \tag{1.4}$$

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} = \begin{bmatrix} c_{11} & c_{12} & c_{13} & & & \\ c_{12} & c_{11} & c_{13} & & 0 & \\ c_{13} & c_{13} & c_{33} & & & \\ & & & c_{44} & 0 & 0 \\ & 0 & & 0 & c_{44} & 0 \\ & & & 0 & 0 & \frac{c_{11}-c_{12}}{2} \end{bmatrix} \begin{bmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \\ S_5 \\ S_6 \end{bmatrix} \tag{1.5}$$

$$T_3 = C_{13}S_1 + C_{13}S_2 + C_{33}S_3 \tag{1.6}$$

For a Wurtzite lattice with tetrahedral coordination and a hexagonal Bravais lattice, assuming linear theory is applicable according to Hooke's law, the piezoelectric tensor has three independent components, two of them $c_{13}S_1$ and $c_{13}S_2$ represent the in plane strain and one is across the c axis of the hexagonal lattice $c_{33}S_3$. If a free top surface can be assumed, then $T_3=0$ due to the isotropic nature of the material, the first two terms are equivalent ($S_1= S_2$). Hence, S_3 across the c axis can now be expressed as a function of the in plane strain component:

$$2C_{13}S_1 + C_{33}S_3 = 0 \tag{1.7}$$

The piezoelectric tensor for a tensile strained AlGaN layer on the bulk GaN layer can be represented as a combination of three independent components:

$$P_{PE} = e_{31}u_{xx} + e_{31}u_{yy} + e_{33}u_{zz} \tag{1.8}$$

The e_{ij} terms represent piezoelectric coefficients and u_{ii} are the strains corresponding to the mechanical displacement in the lattice along the x, y and c axes. Since AlGaN layers grown pseudomorphically on GaN are under tensile biaxial strain, $u_{xx} = u_{yy}$ and given as:

$$u_{xx} = u_{yy} = \frac{a - a_0}{a_0} = \frac{a_{AlGaN} - a_{GaN}}{a_{GaN}} \; and \; u_{zz} = \frac{c - c_0}{c_0} \tag{1.9}$$

where a and c are strained lattice constants. Assuming the top surface of the grown AlGaN is free, we can use the previous relationship to express u_{zz} in terms of u_{xx} where C_{13} and C_{33} are the elastic stiffness constants [1.33].

$$u_{zz} = -\frac{2C_{13}}{C_{33}} u_{xx} \tag{1.10}$$

Thus, the piezoelectric polarization of the AlGaN layer can hence be expressed as [1.32-1.33]:

$$P_{PE} = 2u_{xx}\left[e_{31} - \frac{C_{13}}{C_{33}} e_{33}\right] \tag{1.11}$$

The above is valid for small strains or small Al content in the linear regime derived from polarization components as induced by changes in a and c. There is a dimensionless parameter u which represents the length of the bond parallel to the c-axis. At the microscopic level, an additional component of P_{PE} exists due to strains parallel or perpendicular to the c-axis which cause changes in u due to internal dislocations between the metal and nitrogen sub-lattices [1.32]. The total calculated values of piezoelectric constants for III-nitrides are presented in Table 1.2 [1.10, 1.29, and 1.32-1.40].

Table 1.2: Lattice constants and piezoelectric constants of AlN, GaN, InN Wurtzite

Wurtzite	AlN	GaN	InN
a_0 (Å)	3.112	3.189	3.54
c_0 (Å)	4.982	5.185	5.705
c_0/a_0	1.601/1.619	1.627/1.634	1.612/1.627
u	0.380	.376	0.377
e_{33} (C/m^2)	1.46/1.55/1.29	0.73/1/0.65	0.97
e_{31} (C/m^2)	-0.60/-0.58/-0.38	-0.49/-0.36/-0.33	-0.57
u_{xx}	9.0	9.5	
u_{zz}	10.7	10.4	14.6

The piezoelectric constants of III-N compounds are negative in contrast to other III-V materials and 10 times larger [1.29] than obtained with GaAs crystals. P_{PE} increases with strain and from GaN to InN to AlN. Irrespective of the AlGaN composition, $e_{31} - {}^{C_{13}}/_{C_{33}}\, e_{33} < 0$, and since u_{xx} is positive, the value of P_{PE} in III-nitrides is always negative for layers under tensile stress ($a > a_0$) and positive for layers under compressive stress ($a < a_0$). Hence, for layers under tensile stress, P_{SP} and P_{PE} orientations are parallel, and for layers under compressive stress, the two polarizations are anti-parallel [1.32]. This is why, generally, AlGaN barrier layers are grown over GaN buffer layers to activate tensile strain and maximize the polarization charge density. Figure 1.8 illustrates the directions of P_{SP} and P_{PE} vectors for an undoped Ga-face and N-face AlGaN/GaN heterostructure where a thin AlGaN layer is grown under tensile stress.

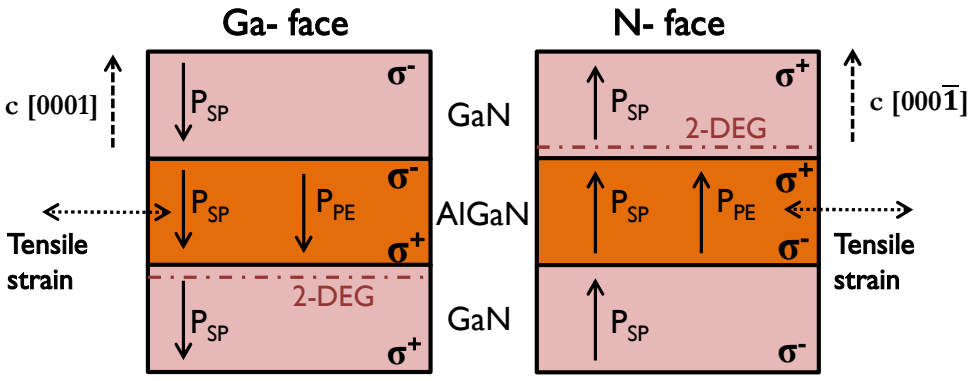

Figure 1.8: Directions of polarization vectors in an un-doped GaN/AlGaN/GaN heterostructure

Polarization charges exist at each interface of the structure. P_{PE} is insignificant in thick GaN layers since the lattice mismatch between GaN and substrate releases through defects or dislocations at the bottom of GaN buffer layer breaking the strain [1.41]. The polarization induced sheet charge σ is positive for AlGaN on top of GaN with Ga/Al-face polarity and for GaN on top of AlGaN with N-face polarity. The negative P_{SP} of GaN and AlGaN, as well as the negative P_{PE} of the AlGaN layer, point from the nitrogen towards the nearest neighbor Ga or the Al atom along the c axis. As a consequence, total polarization of both layers is directed towards the substrate for Ga-face and towards the surface for N-face polarity crystals. Since values of the piezoelectric constants and P_{SP} increase from GaN to AlN [1.29, 1.32], the total polarization of a strained (or even unstrained) AlGaN layer is larger than a relaxed GaN buffer layer. The polarization induced charge density at an abrupt hetero-structure interface [1.32] can be defined as:

$$\begin{aligned} \sigma\,(P_{SP} + P_{PE}) &= P(bottom) - P(top) = \\ \{P_{PE}(bottom) - P_{PE}(top)\} &- \{P_{SP}(bottom) - P_{SP}(top)\} \\ &= \sigma(P_{SP}) + \sigma(P_{PE}) \end{aligned} \tag{1.12}$$

Therefore, a net positive polarization charge is present at the lower AlGaN/GaN interface for Ga-face structure (Figure 1.8 left), and at the upper GaN/AlGaN interface for the N-face structure (Figure 1.8 right)). The electron density developed in response to this positive charge forms a two dimensional electron gas (2-DEG), presuming that the triangular quantum well at the AlGaN/GaN interface drops below the Fermi level E_F.

Thus, in Ga face heterostructures, the 2-DEG is formed close to the lower AlGaN/GaN interface, and for N face, close to the upper interface. Likewise, a negative polarization sheet charge density can cause an accumulation of holes at the interface, if the valence band edge of the AlGaN/GaN heterostructure crosses the Fermi level.

In fact, P_{SP} and P_{PE} components are large enough to produce a 2DEG with high electron concentration even without intentional doping of the barrier (P_{PE} (GaN) = 5 × P_{PE} (GaAs)) [1.32], in contrast to remote doping employed for AlGaAs/GaAs structures. The piezoelectric constants for $Al_xGa_{1-x}N$ can be obtained from linear interpolation as:

$$e_{ij}(x) = \left[e_{ij}(AlN) - e_{ij}(GaN)\right]x + e_{ij}(GaN) \tag{1.13}$$

The nature of piezoelectric constants is shown in Figure 1.9. It can be observed that $|e_{33}(x)|$ tends to strongly increase with Al x and $|e_{31}(x)|$ has a slight increase. However, at higher strains, changes in e_{ij} appear due to an internal strain component originating from changes in the bond parameter u becoming increasingly relevant. As can be seen from the dashed lines [1.37-1.38], u related reductions in e_{ij} at higher x for AlGaN grown on GaN renders the increase in $|e_{33}(x)|$ negligible. The rise in $|e_{31}(x)|$ is more evident. This causes a non-linear P_{PE} in a pseudomorphically grown AlGaN/GaN heterostructure.

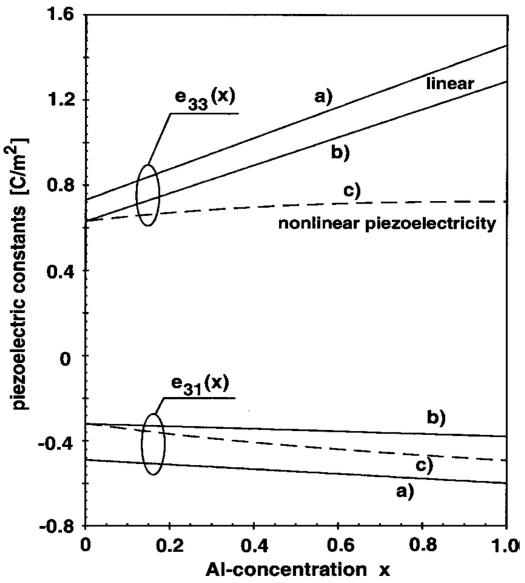

Figure 1.9: Piezoelectric constants of AlGaN determined by linear interpolation between GaN and AlN constants from literature [1.29, 1.37-1.38]. Dashed lines show piezoelectric constants of a pseudomorphic AlGaN layer grown on GaN vs alloy composition calculated by taking strain induced nonlinear effects.

The bound sheet charge associated with P_{PE} is σ (P_{PE}) /e which increases more than linearly with mole fraction x. The following linear interpolations can be used to obtain AlGaN properties and calculate the actual polarization induced charge densities [1.32, 1.42].

Spontaneous Polarization:

$$P_{SP}(x) = (-0.052x - 0.029)\ C/m^2 \tag{1.14}$$

Alternatively, a bowing parameter b might be used for accurate interpolation [1.43]

$$P_{SP}(x) = (xP_{SP}(AlN) + (1-x)\,P_{SP}(GaN) + bx(1-x)) \tag{1.15}$$

Lattice constants:

$$a_0(x) = (-0.077x + 3.189) \times 10^{-10}\ m \tag{1.16}$$

$$c_0(x) = (-0.203x + 5.189) \times 10^{-10}\ m \tag{1.17}$$

Elastic constants:

$$C_{13}(x) = (5x + 103)\ GPa \tag{1.18}$$

$$C_{33}(x) = (-32x + 405)\ GPa \tag{1.19}$$

Still, due to increases in $|e_{ij}|$, it would appear that the polarization charge density in eq. 1.11 could be continually maximized by increasing x. However, above a critical growth thickness or Al mole fraction (> 0.14) [1.44-1.45], a reduction in the total polarization charge density due to strain relaxation effects needs to be taken into account [1.32] as the growth ceases to be pseudomorphic. The degree of relaxation for x is given by $r(x)$ and the modified equation for P_{PE} taking into account partially relaxed barriers can be considered as:

$$r(x) = \frac{a(x) - a(GaN)}{a_0(x) - a(GaN)} \tag{1.20}$$

$$P_{PE} = 2\{r(x) - 1\}\left\{\frac{a_0(x) - a(GaN)}{a_0(x)}\right\}\left[e_{31} - \frac{C_{13}}{C_{33}}e_{33}\right] \tag{1.21}$$

For an AlGaN barrier with fixed composition, polarization and the associated sheet charge (taking into account P_{SP} differences) decreases linearly with increasing relaxation degree. Thus strain relaxation limits the maximum possible P_{PE} and the associated charge density.

1.3 Basics of GaN HEMTs

High electron mobility transistors or HEMTs address the major application sectors in the overall GaN market and are highly suited for high power and high efficiency amplifiers. It also addresses the mm wave market requisites of low dispersion with high speed and high breakdown. While commercialization of GaN HEMTs was initiated around 2005, the premier AlGaN/GaN HEMT on Sapphire with a 14 % Al content was proposed by Khan et al. in 1993 [1.46] with channel densities around 10^{11} cm^{-2}. They also reported a small signal performance of f_T =11 GHz and f_{max} =35 GHz in 1994 [1.47]. Wu et al. [1.48] then reported RF power densities of 1.1 W/mm around 1996 which clearly outperformed GaAs and InP technologies. Around 1999-2001, HEMTs with

good power densities ~9 W/mm were produced though they suffered from nonlinearity issues. [1.49-1.50]. Improvements in fabrication strategies and epitaxial growth greatly contributed to boost the large-signal characteristics to simultaneously reach mobilities around 1500 $cm^2/V.s$, channel densities ~ 10^{13} cm^{-2}, V_{BD} > 80V and power densities ~10 W/mm [1.11]. Palacios et al. [1.51] in 2005 demonstrated Ka band power density of 10.5 W/mm at 40 GHz and 33 % PAE.

Huge growth has occurred across performance levels of AlGaN/GaN transistors with typical output current levels ~1 A/mm and power densities around 12 W/mm. Power amplifiers with P_{out} ~ 1kW in the L~S band and 81 W in the X band have been reported [1.52-1.53]. Sun et al. [1.54] demonstrated f_T= 90 GHz with a current density of 750 mA/mm with 100 nm transistors. Kimura et al. [1.55] and Yamasaki et al. [1.56] have reported 43% PAE with P_{out}= 60 W and 68% PAE with P_{out}= 100 W respectively. Micovic et al. [1.57], reported on GaN performances in the W band with a power density of 2.1 W/mm. Breakdown voltages exceeding 1500 V and 1700 V [1.58-1.59] on Si and Sapphire respectively has already been achieved. In 2013, f_T and f_{max} values of 100 and 206 GHz were reached by Bouzid-Driad et al. [1.60] while Denninghoff et al. [1.61], achieved current densities of 4A/mm and f_T and f_{max}= 204 and 405 GHz respectively on MIS-HEMTs.

A. STRUCTURE AND ENERGY BAND PROFILE

The basic HEMT structure based on the AlGaN/GaN heterostructure [1.6, 1.11] is shown in Figure 1.10. A heterojunction is formed when two semiconductors of differing bandgaps are grown on each other. Similar to other FET structures, there are three electrodes: gate, source and drain.

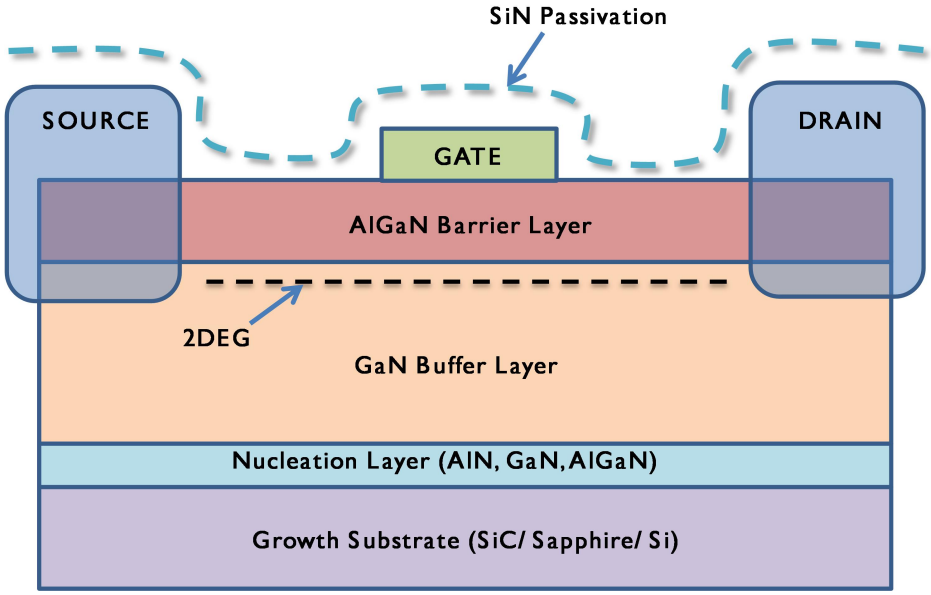

Figure 1.10: Basic AlGaN/GaN HEMT structure with metal/semiconductor contacts

Because GaN substrates cannot be grown viably, hetero-epitaxy on SiC or other substrates is used to grow a thick GaN buffer layer. The nucleation layer is critical to reduce the lattice mismatch for growth and thus improve surface quality. Sometimes, it aids in suppressing the growth of mixed polarity GaN. In some cases, an undoped AlGaN spacer might be present. Its thickness is modulated to separate dopants from the channel region to reduce scattering and boost mobility.

Since the lattice constant of AlGaN is smaller than GaN, the AlGaN is grown with a certain amount of tensile strain depending on the mole fraction. A GaN cap may or may not be present. The band gap discontinuity results in the formation of a notch in the conduction band E_C adjacent to the AlGaN/GaN interface [1.32, 1.62]. As previously discussed, due to the discontinuities in polarizations and the resultant net positive polarization charge existing at the AlGaN/GaN interface, electrons tend to accumulate in the notch to form a 2-DEG well, a typical characteristic of the isotype junction [1.63-1.64]. The energy of an electron contained in a potential well is quantized. The phrase "two-dimensional electron gas" refers to the accumulated electrons with quantized energy levels in one spatial direction (perpendicular to the interface), but free to move in the other two spatial directions.

The central objective of an HEMT is to maximize the electron channel density in the 2-DEG which could be affected by roughness, interactions between polarities of Ga- and N- face, traps and scatterings. As discussed in the previous section, for GaN devices the 2-DEG potential well is formed naturally with no external doping, allowing the increase of carrier concentration with reduced impurity scattering. This generates the term "high mobility" transistor since even for undoped or lightly doped GaN, the electron concentration is very high, and the channel electrons are separated from the ionized donors enabling high mobilities and low noise operation. In some cases, doped AlGaN structures demonstrate superior DC operation but associated worsening of scattering phenomena might degrade the RF performance [1.65].

The source and drain usually composed of Ti/Al/Au alloys [1.66] extend through the AlGaN barrier to reach the 2DEG forming ohmic contacts through thermal annealing. Thus, this is a normally on or depletion mode transistor since the 2-DEG maintains a direct connection between the source and the drain even at zero gate voltages [1.32]. The 2-DEG needs to be externally depleted before the semi-insulating GaN stops the current flow. The gate electrode forms a Schottky contact to the surface AlGaN which needs to be reverse-biased beyond a certain threshold voltage to completely deplete the electrons, pinch-off the channel and turn off the device. Usually made out of Ni/Au or Pt/Au, the Schottky gate also prevents parasitic conductions parallel to the channel between the source and drain.

The energy band diagram of the HEMT device, with the formation of the triangular potential well as the two semiconductors make contact is shown in Figure 1.11 [1.62, 1.67].

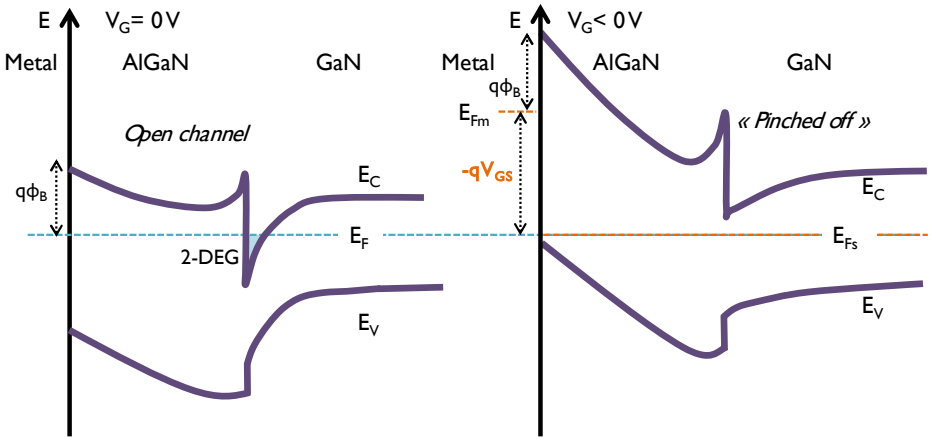

Figure 1.11: Electronic band diagram underneath gate electrode of AlGaN/GaN HEMT in thermal equilibrium under zero gate voltage and under negative gate bias

AlGaN has a wider bandgap than GaN. Hence, two interface parameters controlling the band diagram on contact are the conduction and valence band discontinuities and the built in potential. The Fermi level E_F is aligned across the layers under no external voltages. The conduction band energy directly reflects the presence and manipulation of the 2DEG layer. The offset in the conduction band ΔE_C is the difference in the electron affinities χ of GaN and AlGaN. It varies depending upon the chosen x.

$$\Delta E_C = \chi_{GaN} - \chi_{AlGaN} \tag{1.22}$$

The corresponding valence band discontinuity can be obtained as:

$$\Delta E_V = (\chi_{GaN} + E_{G,GaN}) - (\chi_{AlGaN} + E_{G,AlGaN}) \tag{1.23}$$

The negative piezoelectric charges at the top AlGaN/metal surface contribute to the peak of E_C at the metal contact. The Schottky barrier Φ_B at the gate contact is defined as follows in terms of the metal work function and the electron affinity:

$$q\Phi_B = q\Phi_m - \chi \tag{1.24}$$

The 2DEG in the triangular potential well at V_G= 0V is formed as E_C at the AlGaN/GaN interface bends in response to the positive polarization interface charge. For AlGaN/GaN at equilibrium, the band bending due to the bound polarization is high enough to cause the edge of E_C to fall below fermi level E_F adjoining the interface. Electrons accumulate to populate quantized energy levels in the well below the E_F.

At this point of V_{GS}= 0 V, on application of a positive drain voltage V_{DS}, conduction would be initiated due to a potential drop between the source and drain. Transistor action is activated as an applied gate voltage V_{GS} shifts E_F on the gate metal E_{Fm} with respect to its value deep in the GaN buffer layer. On varying V_{GS}, the E_F on the gate side shifts upward or downward depending on the polarity while the Fermi level in the semiconductor bulk remains relatively constant. Under forward bias, the position and shape of the potential barrier on the AlGaN side of the interface remain relatively similar and the drop is concentrated in the GaN. Under reverse V_{GS}, E_C edge at the GaN channel rises away from E_F proportionally as the channel density and hence the current levels drop [1.62]. Due to the significant depletion just under the gate, most of the applied bias drops across the AlGaN layer, creating a barrier between the Schottky gate and the 2-DEG as the depletion width extends. When reverse V_{GS} crosses V_{th} defined as the threshold voltage, E_C crosses E_F and the channel is pinched off.

B. BARRIER CONTROL ON 2-DEG CONCENTRATION

The origin of electrons in the channel is normally surface donor states unless there is intentional doping in the AlGaN barrier. These surface states exist within the band-gap of the semiconductor created by dislocations, impurity species or crystalline defects. When trap energies are below E_F, acceptor-like traps hold a negative charge on occupation. However, it is the donor like surface traps present above E_F that are the source of the 2-DEG. To support 2-DEG formation, donor-like traps need to be empty of electrons, and holding a positive charge as these traps are neutral when occupied. The formation and concentration of the 2-DEG are closely linked to the thickness and composition of the AlGaN barrier [1.68-1.71] as illustrated in Figure 1.12.

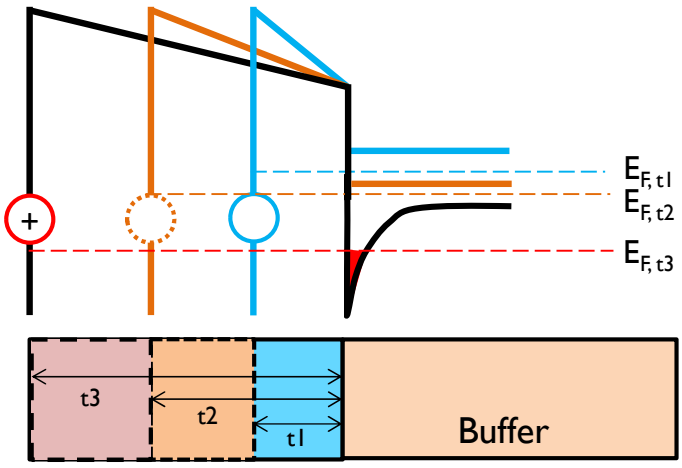

Figure 1.12: Schematic diagram illustrating the changes in the band diagram with the thickness of the AlGaN barrier layer

Donor like traps deep within the AlGaN bandgap of a thin barrier layer t_1 can be assumed to be completely occupied and the surface field is controlled solely by polarization charges. Thus, they are neutral and cannot support the formation of the 2-DEG. However, as the barrier thickness increases and the conduction band stretches, the E_F starts sliding down and begins to approach the donor trap level. At a critical thickness $t_C \sim t_2$, the donor trap and E_F levels coincide. At this point, the electrons occupying the traps are instantly drawn to the channel owing to the strong polarization-induced electric field and the surface traps become empty i.e. positively charged. A finite 2-DEG density is thus achievable as the electric field within the barrier reduces.

For higher thicknesses, the 2-DEG density increases until it begins to saturate, limited by the polarization induced charges or complete depletion of the surface states. Also, above the AlGaN critical growth thickness [1.32, 1.68-1.71] relaxation could set in, which would create defects and severely restrict the attainable channel density. This is where the chosen AlGaN mole fraction becomes a critical factor. For high x, the grown AlGaN barrier has higher spontaneous polarization (P_{SP} (AlGaN) > P_{SP} (GaN)) and carries a higher strain, thus creating stronger piezoelectric polarization charge densities. This would mean an almost linear increase in the achievable 2-DEG channel density with x, though mobility will suffer due to higher roughness, alloy disorderings and associated scatterings. However, other factors constrain the advantages of higher x values.

At a critical x value ~ 0.4, the piezoelectric strain would cross the elastic energy threshold resulting in the relaxation of the AlGaN barrier. The associated fall in the piezoelectric polarization would be significantly stronger than the increase in P_{SP} and the device performance, and especially the channel density will suffer. For smaller x, the available polarization charge will be smaller, but the critical AlGaN growth thicknesses are higher, increasing the probability to reach the maximal channel density, limited in this case, only by the bound polarization charges. Relaxation would then occur much later and generally not be an issue. Hence, a tradeoff exists in choosing a suitable x.

C. FUNDAMENTAL CONDUCTION THEORY

Gate Current

The quality and robustness of the Schottky contact with low leakage currents are essential to high performance GaN HEMTs. The Schottky barrier height is the key parameter of the junction, which controls both the width of the depletion region and the electron flow across the interface. In contrast to p-n junctions, the Schottky current transport is due to majority carriers with fast response rates. For HEMTs, general current transport is defined through thermionic emission TE theory [1.72-1.73] wherein electrons have to cross over the potential barrier between the metal and

semiconductor to initiate transport. Thus, according to standard TE, the gate current is solely controlled by the barrier height and independent of the barrier profile. The following assumptions hold: (a) the barrier height is higher than the thermal voltage, (b) thermal equilibrium exists at the emission interface and (c) a net current flow does not alter the equilibrium. Hence, for a fixed depletion layer, the TE current flowing from the GaN to the metal can be written as:

$$I_G = I_0\left\{exp\left[\frac{q(V_{GS}-I_GR_S)}{\eta kT}\right]-1\right\} \approx I_G = I_0\left\{exp\left(\frac{qV_{GS}}{\eta kT}\right)\right\} \; for\; V_{GS} \gg I_GR_S \tag{1.25}$$

Here, k is the Boltzmann constant (1.38 x 10^{-23} J/K. s^2), V_{GS} is the gate bias, η is the ideality factor realated to the current slope, R_S is the series resistance of the diode, T is temperature, q is electronic charge (1.602 x 10^{-19} C). I_0 is the reverse saturation current which can be calculated from the straight line current intercept at zero bias as follows:

$$I_0 = AA^*T^2exp\left(\frac{-q\Phi_B}{kT}\right) \tag{1.26}$$

Where A: effective diode area, A^*: effective Richardson's constant = 32 A/cm^2.K^2 for undoped $Al_{0.23}Ga_{0.73}N$ and 34.2 A/cm^2. K^2 for $Al_{0.25}Ga_{0.75}N$ and Φ_B : zero-bias barrier height

The ideality factor for thermionic emission is 1. In actual devices however, η varies significantly. Thus, η reveals how close the observed on-state characteristic is to ideal thermionic emission and thus, the contributions of alternate conduction mechanisms such as tunneling.

Channel Density

The electronic band diagram in Figure 1.13 presents the schematic to understand the 2-DEG density considerations which are ~ 10^{13} cm^{-2} in AlGaN/GaN heterostructures [1.32, 1.69 and 1.74].

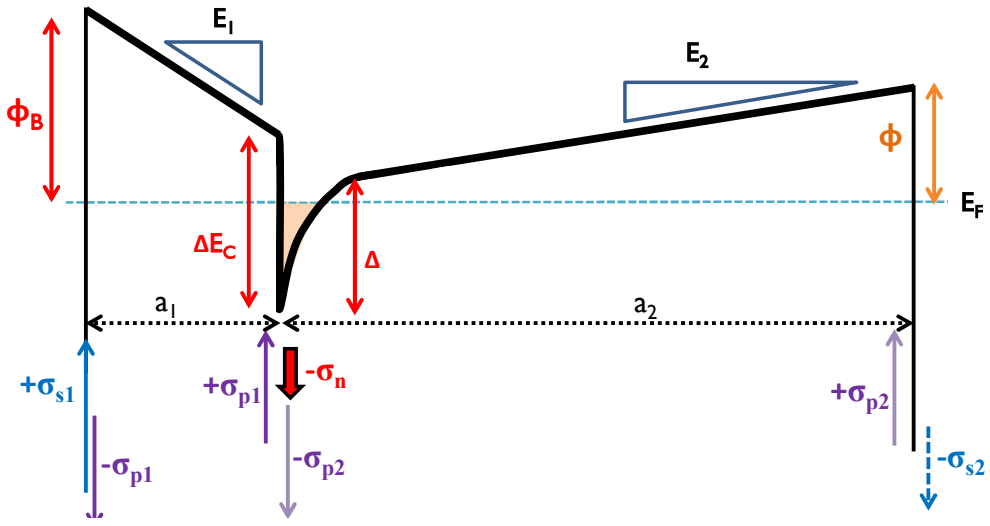

Figure 1.13: Schematic for the computation of the channel density

The net channel density in the 2DEG is proportional to the net polarization charges at the interfaces and diminished by the electric fields

$$\sigma_n = \sigma_{p1} - \sigma_{p2} - \epsilon_1 E_1 - \epsilon_2 E_2 \tag{1.27}$$

To represent the stored charges, the capacitance representing the front depletion is considered which arises from the electric field across the AlGaN barrier. The field in the buffer layer is significantly reduced since $a_2 >> a_1$. Hence, the backside depletion term can be neglected and the channel density n_s ($=\sigma_n/q$) can be represented as a function of the applied voltage as:

$$n_s(x,d) = \frac{\sigma_b(x)}{q} - \frac{\epsilon_0 \epsilon(x)}{q^2 t_{AlGaN}}(q(\phi_B(x) - V_G) + \Delta(x) - \Delta E_C(x) \tag{1.28}$$

where

$n_s(x,d)$: Electron density

σ_b : Sheet charge density

ϵ : Dielectric constant of the barrier layer

ϕ_B: Schottky barrier height of the gate contact

V_G: Gate voltage

ΔE_C: Conduction band discontinuity at interface

Δ: Penetration of conduction band below the Fermi level

Assuming that all electrons in the channel occupy the lowest subband, Δ can be approximated as:

$$\Delta = \frac{\sigma_n}{q^2 N_S} \tag{1.29}$$

where N_S is the effective density of states.

The sheet carrier concentration will be lower with increasing height of the Schottky barrier and decreasing thickness of the barrier layer. In the normal on state, the 2-DEG is well below the Fermi level and n_s remains high. As V_{GS} becomes increasingly negative, the electron density decreases as Δ reduces. Near the threshold V_G value, n_s tends to zero.

Threshold Voltage

The minimum voltage at the gate necessary to empty the potential well and elevate the conduction band to the Fermi level is the threshold voltage. The carrier density $n_s = n_{2DEG}$ in the potential well can be expressed in terms of the Fermi level as follows [1.75]

$$E_F = kT\, ln\left(\frac{n_{2DEG}}{2\frac{m_e kT}{\pi h^2}}\right) \tag{1.30}$$

The potential difference between the gate and the channel for $V_{GS}= V_{th}$ must balance the net residual potential difference in the structure. Thus V_{th} needs to compensate for ΔE_C, the potential difference due to net interface charge Q_{int} as well as the surface donor charge N_{Surf} that maintains the 2-DEG density. The doping effects can be neglected since most devices are not doped. If a maximal nonintentional n-doping of 10^{18} is considered, the change in V_{th} would be around 60 mV which is irrelevant.

Thus, V_{th} can be expressed as [1.76-1.77]:

$$V_{th} = \phi_B - \frac{\Delta E_C}{q} - \frac{t_{AlGaN} Q_{int}}{\varepsilon_{AlGaN}} - \frac{q t_{AlGaN} N_{Surf}}{\varepsilon_{AlGaN}} \tag{1.31}$$

Q_{int} is essentially the sum of P_{SP} and P_{PE} charges of AlGaN and GaN. It can be written as:

$$Q_{int} = P_{SP+PE}(AlGaN) + P_{SP}(GaN) \tag{1.32}$$

Since N_{2DEG} is supported by the surface charge N_{Surf} and the gate bias, we can write:

$$N_{surf} = \frac{\varepsilon_{AlGaN}}{q t_{AlGaN}} [V_{GS} - V_{th}] \tag{1.33}$$

Drain Currents

The drain current I_{DS} localized in the 2-DEG channel is expressed in terms of the drift current controlled by the lateral electric field as follows [1.75, 1.77]:

$$I_{DS}(x) = W Q_{2DEG}(x) v(x) \tag{1.34}$$

Where $v(x) = \mu_n E(x)$ and $Q_{2DEG}(x)$ can be expressed as

$$Q_{2DEG} = q n_{2DEG}(x) = \frac{\varepsilon_{AlGaN}}{t_{AlGaN}} (V_{GS} - V_{th} - V(x)) \tag{1.35}$$

I_{DS} can be obtained by integrating this equation along the length of the gate

$$I_{DS} = \frac{W \mu_n}{L} \int_0^L Q_{2DEG}(x) \frac{dV(x)}{dx} \tag{1.36}$$

Since the channel density is proportional to the effective gate bias V_{GS}- V_{th}, I_{DS} can be expressed as a function of the gate bias, the electron mobility as well as V_{th} which accounts for the polarization charge dependence for the linear and saturation regimes of operation.

$$I_{DS,Lin} = \frac{\varepsilon_{AlGaN}}{t_{AlGaN}} \frac{W \mu_n}{L} [(V_{GS} - V_{th}) V_{DS}] \qquad V_{DS} \ll V_{D,sat} \tag{1.37}$$

$$I_{DS,Sat} = \frac{\varepsilon_{AlGaN}}{t_{AlGaN}} \frac{W\mu_n}{L} \left[\left(V_{GS} - V_{th} - {}^{V_{D,sat}}/_{2} \right) V_{DS} \right] \qquad V_{DS} \gg V_{D,sat} \tag{1.38}$$

HEMTs are essentially voltage controlled current sources; hence the transconductance is given as:

$$g_m = \frac{\delta I_{DS}}{\delta V_{GS}} = \frac{W\mu_n}{L} (V_{GS} - V_{th}) \tag{1.39}$$

1.4 UMS GH25 GaN HEMT Technology

United Monolithic Semiconductors is a European corporation specialising in RF, microwave and millimetre wave devices. Their GH25-10 MMIC GaN HEMT technology is ideally designed for robust low noise amplifier and low power MMICs, switching applications, and multi-stage, high power, high efficiency amplifiers up to 20 GHz [1.78-1.80]. UMS has been a partner in multiple projects based on GaN products through contribution of the GH-25 devices. This process has successfully achieved space evaluation and belongs to the European Preferred Parts list (EPPL) organized by the European Space Agency (ESA). GaN power amplifiers for space were also provided by UMS for the Slogan project. UMS is also partnering with Tesat and Schott to develop RF power GaN devices for BIOMASS earth observation satellites slated for launch in 2021 [1.80].

A. FEATURES AND STRUCTURE

As presented in the schematic cross section of Figure 1.14, the GH25-10 technology [1.78] is based on AlGaN /GaN HEMTs with a gate length of 250 nm and a slanted T-shaped profile. This gate dimension has been found to yield a reliable process with low leakage which is essential to realize an electrically robust contact. The T-profile lends first order field plate effects and has been carefully tailored to widen frequency boundaries.

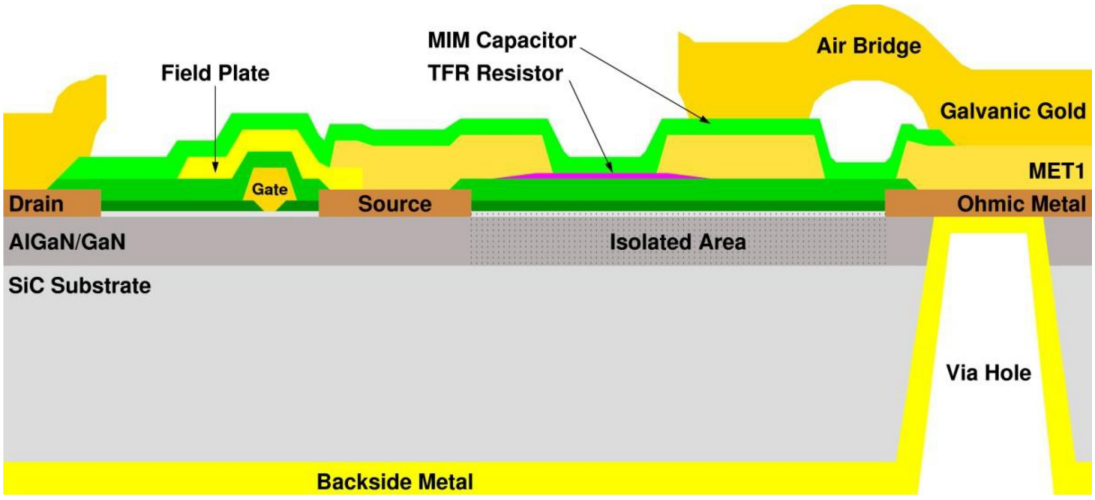

Figure 1.14: GH25-10 process schematic cross section [1.78]

The asymmetry in the gate is customized to support higher breakdown voltages, a critical requirement in the power amplification mode. The devices have an average V_{th}= -3.5 V.

The process was built on semi-insulating SiC-6H substrate with a diameter of 4 inches using a MOCVD (Metal Organic Vapour Phase Epitaxy) active layer. The wafer is thinned down ~ 100µm followed by a via-hole process to ground the source before the final metallization on the back side. The front side of the wafer is protected with SiN.

The major processes including epitaxial deposition of AlGaN, GaN and passivation layers have been controlled to achieve the optimal current and power densities. Source and the drain ohmic contact resistances are low ~ 0.2-0.3 Ohm.mm to enable better RF performances. The recommended V_{DS} bias for operation is 30 V. The sequence of passivation deposition has been improved to achieve median leakage current of 20 µA/mm at V_{DS}= 50 V. Moderate Al mole fraction is chosen to suppress the reverse gate and drain leakage currents while obtaining a competent maximum current level.

Significant thought into reducing the parasitic capacitances, in particular between the gate and source has contributed to design flow. Source-terminated field plate is employed to reduce the gate-drain capacitance under high voltages. However, for power switch applications, the gate is centred between the source and drain ohmic contacts with no field plate.

Two gate-drain distances L_{GD} were chosen = 1.7 µm and 2.7 µm to have flexibility in power, efficiency and bandwidth trade-offs. For L_{GD}= 2.7 µm, the source-drain breakdown voltage V_{BDS} exceeds 150 V defined at a drain current level I_D= 1 mA/mm.

Air bridges have been designed to isolate device topography and enable integrated inductors in addition to MIM capacitors, diodes and metallic resistors. For interconnects, 1.8 µm evaporated and 7 µm electroplated Au has been used. Taking into account the thermal variations and to sustain maximum temperature of 200°C, a gate to gate pitch of 40µm is chosen.

B. RF PERFORMANCE

Table 1.3 presents the main attributes of this technology [1.78]]. A power density ~ 4.5W/mm has been achieved during load-pull characterization by optimizing the biasing to a standard V_{DS}= 30 V. Load and source pull matchings, preferably in continuous wave CW mode, help extract the ideal load conditions with respect to obtaining the maximum power and efficiency.

Relevant to receiver applications, a general noise equivalent to 1.5 to 1.7 dB has been measured at 10 GHz when the bias is reduced to a 10-15 V range, for a current density value of 100 mA/mm.

Table 1.3: Main performance attributes of the UMS GH-25 technology [1.78]

Element	Value
Power Density	4.5 W/mm
Threshold Voltage	-3.5 V
I_{DSS}	0.86 A/mm
I_{DS+}	1 A/mm
g_M	290 S/mm
V_{BDS}	> 100 V
DCV_{DS}	25 V (for CW) 30 V (Pulsed)
f_T	25 GHz
f_{max}	> 50 GHz
MIM Density	255 pF/mm^2
Metallic Resistors	28 and 1000 Ω/sq

Relevant to receiver applications, a general noise equivalent to 1.5 to 1.7 dB is measured at 10 GHz, when bias is reduced to a 10-15 V range and a current density equal to 100 mA/mm. Figure 1.15 presents the output power P_{out}, gain, I_D and power added efficiency (PAE) distributions of a 4 inch wafer at 10 GHz, V_{DS}= 30 V and quiescent I_D= 100 mA/mm on a 0.6 mm transistor with identical loads on all transistors.

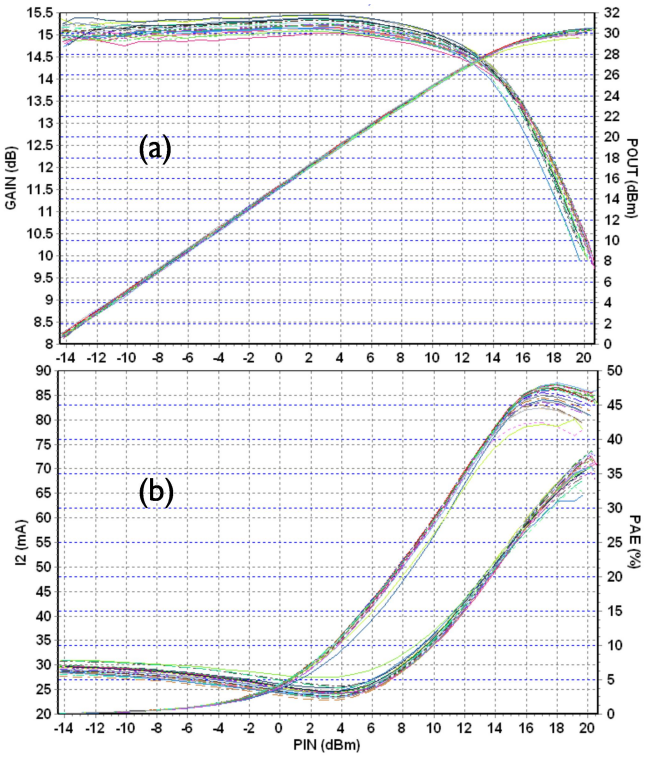

Figure 1.15: (a) Gain & output power and (b) drain current and PAE spreads for a frequency = 10GHz. CW condition and a transistor size of 0.6mm (8x75μm) [1.78]

C. RELIABILITY QUALIFICATION

Significant qualification tests have been carried out to validate the reliability performance of the GH 25 technology whose lifetime expectancies exceed 20 years at 230 °C peak channel temperature [1.78-1.80]. The criteria for tests included effects of wear out mechanisms, environmental factors and the evaluation of failure lifetimes.

The qualification included temperature cycling, storage tests for 1000 hours, High Temperature Reverse Biased (HTRB) tests for 2000 hours and High Temperature Operating Life (HTOL) tests up to 4000 hours as well as DC and RF stress tests to estimate Safe Operating Area (SOA). Significant research has gone into space optimization and associated reliability and compatibility validation of the GH-50 and GH-25 technology.

4000 hours of accelerated RF life tests were performed on GH-25 MMIC samples for channel temperatures of 300°C and 325°C and a constant RF input power at 8.5 GHz. The devices were driven at 7-8 dB of gain compression while P_{out} corresponded to the max PAE condition. V_{DS} was set to 30 V and initial output power was ~ 40dBm [1.79]. Figure 1.16 shows the loss in the output power at both temperatures.

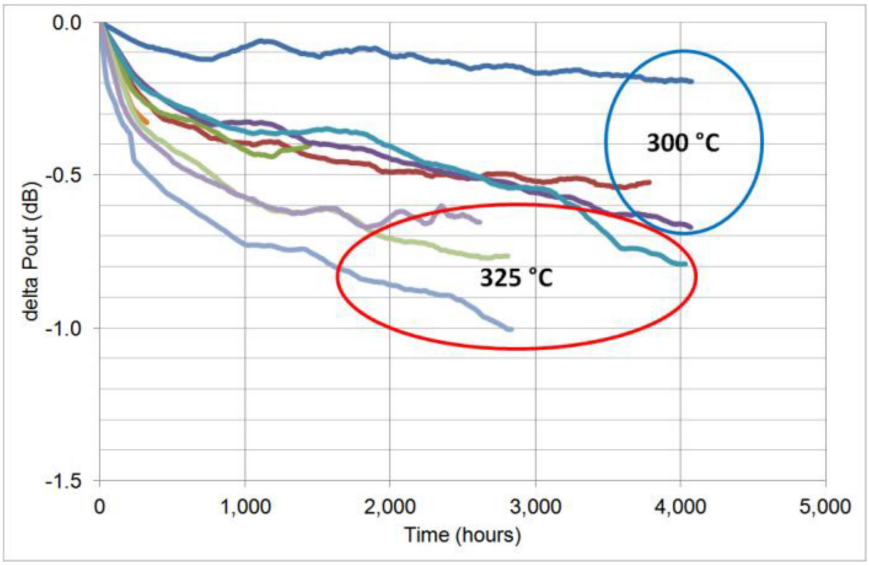

Figure 1.16: GH25-10 MMIC P_{out} degradation at 300 °C and 325 °C channel temperatures [1.79]

A lifetime extrapolation of the MMICs for a failure criterion of 0.5 dB output power degradation is demonstrated in Figure 1.17.

A mean time to failure (MTF) of 23000 hours was achieved at a channel temperature equal to 230°C (nominal operation) and a confidence level ~ 60%. For a 1 dB power degradation criterion, estimated MTF is significantly higher at ~ 2 x 10^5 hours.

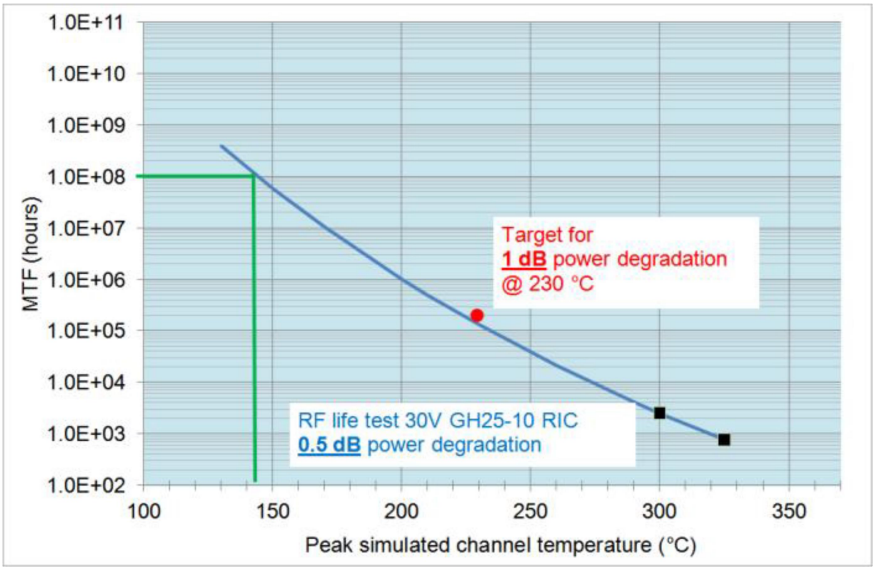

Figure 1.17: GH25-10 GaN-MMIC life time extrapolation for wear-out failure mode (failure criterion: 0.5 dB RF output power degradation) [1.79]

1.5 Reliability of GaN HEMTs: Issues and Mechanisms

A. ORIGINS OF DEGRADATION

For widespread acceptance in existing and future markets, as well as fulfil the core requirements for mass production, reliability is the major concern after performance. The relatively new GaN technology, while providing innovative and powerful solutions, unavoidably also faces the challenges brought by each stage of material and device development. Parasitic effects can be generally observed even on unaged GaN HEMTs, which reduce the performance metrics but do not severely affect reliability. However, degradation mechanisms which strengthen over time or aging stresses, steadily deteriorate not just the electrical response but also device robustness and reliability leading to failure and shorter lifetimes. Research into improving the reliability and suppressing undesirable parasitic effects is thus a central priority for the GaN industry.

In addition to failure or performance limiting mechanisms faced by other similar compound semiconductor devices, GaN devices suffer further degradation issues that are innately linked to the material itself such as polarization effects, heteroepitaxy and thermal mismatches with the substrate. AlGaN/GaN HEMTs also operate under very high bias, electric field and temperatures as compared to other common technologies. This can be better understood from Figure 1.18 which lists the different kinds of degradations affecting AlGaN/GaN HEMTs and the factors that control them [1.12, 1.81-1.82].

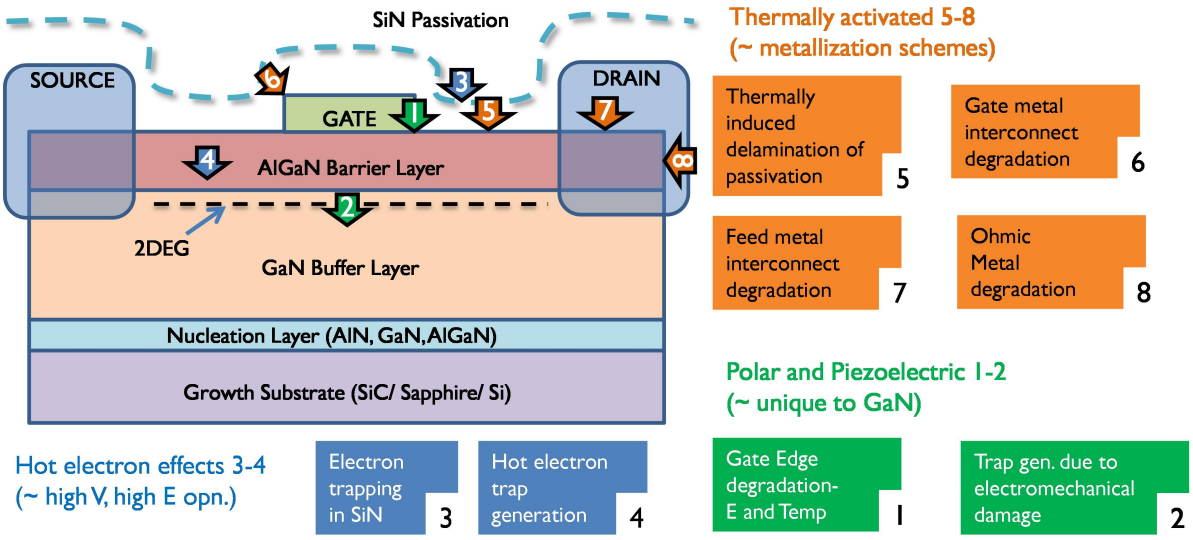

Figure 1.18: Various degradation issues of AlGaN/GAN HEMTs and their origins [81]

Issues 5-8 refer to thermally activated degradation mechanisms, which have been previously observed in other semiconductors systems (Si, GaAs, InP, SiC, etc.). Hence, these failure mechanisms are easier to comprehend and proprietary of the metallization scheme employed. Mechanisms 3 and 4 are related to the presence of hot electrons, which are again a common issue faced by high-voltage field-effect-transistors. Hot-electrons related degradation has been found in all other semiconductor devices (Si, GaAs, InP, etc.) and thus, these failure mechanisms have been studied before in detail. However, mechanisms 1-2 are peculiar to GaN devices due to the polar and piezoelectric nature of this semiconductor material, which is why these mechanisms have never been clearly identified or previously analyzed. This makes the reliability analysis of GaN HEMTs a truly unique subject requiring dedicated and deeply physics-based research.

Alternatively, degradation mechanism genres for GaN HEMTs for RF applications can be broadly categorized [1.83]. Under severe operational or environmental conditions or immature technologies, the discussed effects might be relevant even within a couple hundred hours of tests.

Gate Edge Degradation

A significant portion of the damage to an AlGaN/GaN system is concentrated at the gate edge accelerated dominantly by high electric fields. Especially important in the off state with high reverse voltages [1.84-1.87], it contributes to high leakage currents and can have origins in several physical mechanisms:

1. **Inverse piezoelectric effect (IPE)**: This effect was researched extensively by Joh and Alamo [1.85-1.86] and Ando et al. [1.88], hypothesizing a voltage-controlled failure

mechanism in contrast to the general hot electron based current-critical degradation process. The AlGaN/GaN heterostructure, which is the backbone of the HEMT, has a strained Al layer grown on top of the GaN buffer and thus inherently stores a significant amount of elastic energy. In addition, for strongly piezo-electric materials such as GaN/AlGaN, high voltages can induce large stresses resulting in the appearance of a strong vertical electric field across the AlGaN barrier close to the gate edge. This creates a region in the AlGaN barrier with a high concentration of mechanical stress. Once the total elastic energy crosses a critical value, the AlGaN strained layer relaxes and crystallographic defects are formed. These defects are electrically active and hence significantly affect device behavior such as observed shifts of threshold voltage.

A characteristic critical voltage can be identified at which the threshold elastic energy is reached and a deterioration of all figures of merit is observed. This voltage is a function of the initial stored elastic energy and thus dependent on thickness and composition of the AlGaN barrier. The elastic energy in the AlGaN barrier layer is proportional to strain squared, and strain is linearly proportional to the vertical electric field which is a function of voltage hence the existence of a critical voltage for electrical degradation supports the idea that lattice damage would not occur until elastic energy reaches its critical value [1.85-1.86]. Beyond this voltage, the traps formed in the AlGaN adjacent to the gate edge could form an electron pathway for leakage currents across the gate to channel.

2. **Schottky barrier degradations**: GaN systems in contrast to silicon devices are vulnerable to creation of traps and conductive leakage paths between gate and channel. This phenomenon of gate current rise has been found to be a time dependent degradation with behavior similar to MOS dielectric breakdown [1.89-1.90] Voltage dependent barrier heights have been observed due to defective contacts. Lateral inhomogeneities in the Schottky barrier height can lead to variations in experimental derivations of effective barrier height and ideality factors [1.72, 1.91-1.93].
3. **Electrochemical formation of pits**: Dissolution of GaN at the gate-drain edge can provoke the formation of pit and grooves composed of Ga or Al oxides, which gradually worsen the structural robustness. A chain of electrochemical reactions cause these defects, requiring the presence of holes generated by band-to-band tunneling in addition to agents such as water or oxygen [1.10, 1.94-1.95]. Some have also observed interfacial layers of amorphous aluminum oxide under the gate [1.96].

4. **Extended cracks**: Across the semiconductor epitaxial layers, devices subjected to on-state accelerated tests have been found to develop long cracks and general surface deterioration because of high current density and channel temperature. Greater formation of pits is triggered by high junction temperatures leading to some researchers [1.97] referring to this as the onset of the true temperature-activated inverse piezoelectric effect. Unlike the previous three mechanisms which only increase gate currents, this would also cause an irreversible and noticeable degradation of drain current.

Trapping and Detrapping

Traps in different parts of the structure may be formed during the fabrication process steps prior to being formed during on state or off state stresses [1.81-1.82]. Transient or permanent trapping and detrapping mechanisms with short or long time constants may trigger substantial drifts in device performances such as shifts in threshold voltage or a lowering of transconductance. The spatial and energetic distribution of trap mechanisms is associated with the appearance of several reliability issues. The charge generation in the 2DEG is directly dependent on surface states and hence essential to high power operation. Material imperfections could be manifested as deep-level surface and interface traps. Traps in the bulk barrier or buffer layers could be linked to process variations, which introduce contaminants such as hydrogen, fluorine and oxygen, or compensating species such as iron or carbon into the structure [1.99]. Traps located within the barrier height of AlGaN acts as facilitators to barrier tunneling and threading dislocations extending from the GaN layer [1.92-1.93]. Hence, gate leakage currents are often substantially higher than theoretical predictions due to trap and defect-assisted tunneling, barrier thinning caused by trapping, and hopping through dislocations [1.97-1.100].

Hot Electron Effects

"Hot electrons" refer to highly energetic non-equilibrium electrons, which are capable of crossing potential energy barriers through accumulation of adequate kinetic energy. They can thus penetrate into different structural layers and with sufficient force to break atomic bonds i.e. impact ionization. They can activate as well as create new deep level trap states. Dependent on experimental conditions as well as specific device vulnerabilities, hot electrons cause gradual recoverable and non-recoverable worsening of device metrics as well as contribute as accelerants to electric field induced issues [1.74, 1.98, 1.101-1.102]. They are more relevant under semi-on and on state conditions often accompanied by trapping effects and especially detrimental near the gate-drain access regions.

Metal-Metal and Metal-Semiconductor Inter-Diffusion

During annealing processes, Nickel has been found to form nitrides and oxides from temperatures around 200°C, which reduce the Schottky barrier height. Thermal mismatches, defects or strain can cause occasional inter-diffusion problems such as Au diffusion in the Ni/Au metallization schemes [1.91, 1.100, 1.103 and 1.104]. However, GaN contacts are extremely stable in most cases, capable of tolerating long periods of > 300°C extreme temperature conditions [1.103].

B. RELIABILITY ISSUES

Damage to the AlGaN/GaN system manifests in the form of various degradation issues with specific electrical signatures that are distinctly identifiable as changes in the device response. The origins of these issues are interactions of multiple physical mechanisms, which trigger a certain nature of device deterioration under specific conditions.

Figure 1.19 illustrates the spatial distribution of the following contributing mechanisms which could be the causes of a given reliability issue.

a. Surface states and charge injection to form a virtual gate
b. Traps in the AlGaN barrier
c. Traps in the GaN buffer
d. Traps at the AlGaN/GaN heterointerface
e. Inverse piezoelectric effect
f. Tunneling near the Schottky gate contact
g. Hot electrons

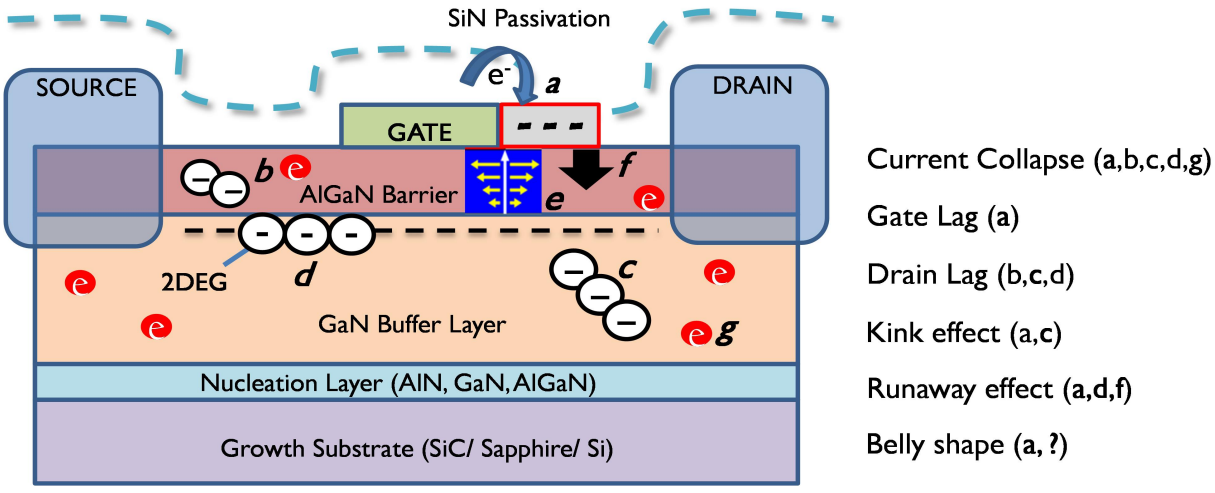

Figure 1.19 : Contributing mechanisms of commonly observed degradation issues in GaN HEMTs

Current Collapse

Current collapse is a parasitic phenomenon referring to the commonly observed reduction in maximum output I_D on successive measurements, especially when driven to reverse voltages, due to trap filling in the first sweep, as well as a noticeable DC to RF dispersion [1.11, 1.48, 1.82-1.84, 1.100-1.110]. When the device is driven at high frequencies and the detrapping time constants cannot respond to the fast signal, there is a discrepancy between steady state IV and the RF frequencies reducing the max I_D and increasing knee voltage, which in turn reduces PAE, and maximum available power. Hence, it can also be quantified as the difference in output power measured from DC I-V and load pull power measurements. Surface traps under the gate are believed to be the major cause though it might also be supported by barrier or buffer traps [1.105]. It is inherently linked to the concept of a virtual gate formation, which we can understand from Figure 1.20.

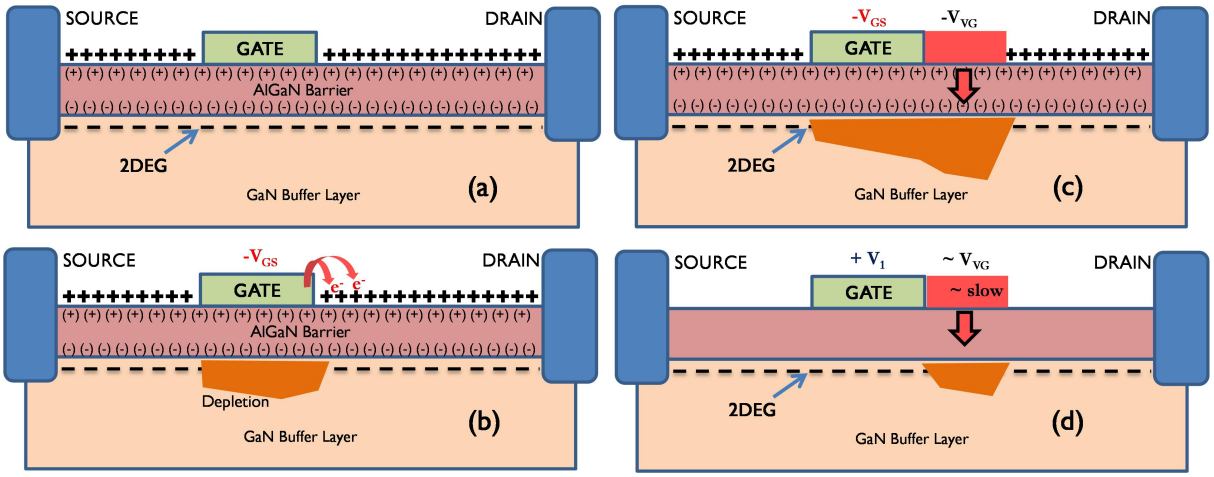

Figure 1.20 : Schematic representation of the formation of virtual gate

The donor states at the top surface are required to maintain the 2-DEG channel charge in the presence of the interface polarization charges to maintain an overall charge equilibrium (Figure 1.20 (a)). When the gate is first reverse biased beyond the pinch-off voltage, the peak electric field appears across the drain edge of the gate. Leakage electrons are injected from the gate into the adjacent free surface donor states (Figure 1.20 (b)). As the donor density is reduced, the region adjoining the gate seems to be an extension of the negatively charged gate [1.110], in effect a "virtual gate" (Figure 1.20 (c)). In accordance with the surface potential, the 2-DEG falls accordingly responding to lowering in the net positive charge [1.81-1.84].

The potential on this "virtual gate" now determines the available current and hence the device responds slowly. On a successive measurement, when the gate voltage just turns positive, most of the depletion under the gate disappears as the mobile charges respond and the channel

density builds. However, the trapped fixed charges respond slowly but contribute to the charge equilibrium. Hence, the negative charge on the virtual gate is sustained longer and the output drain current stays low due to lower mobile carriers [1.12] (Figure 1.20 (d)). The highly resistive access region ~ virtual gate absorbs most of the applied potential, which causes the knee voltage shift to higher voltages. The effect can be clearly seen in Figure 1.21 by Mizutani et al. [1.107], where the drain undergoes significant collapse following the application of a reverse bias.

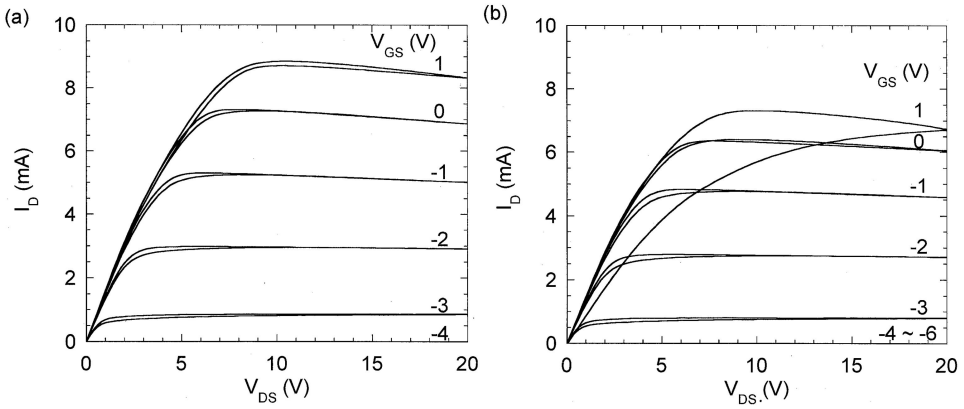

Figure 1.21 : I-V characteristics measured at gate voltage of (a) 1 to -4 V and (b) 1 to -6 V [1.107]

Steady state electron population of the virtual gate is determined by the time constants of detrapping processes; the lateral transport of the electrons to the traps and the frequency of the applied signal. To forward bias the virtual gate and restore the original I_D, V_G needs to be more positive or photons might be introduced to generate electron hole pairs to compensate the charge deficit. The current collapse phenomenon alternatively has characteristic time dependence. After sufficient time, normal I_D characteristics are restored through thermal emission of the trapped charge. However, under AC drive, the failure of the electrons to respond to the high frequency signal is a major issue. Thus, current collapse, expressed as an increase in dynamic on-resistance can substantially affect dynamic RF output as well as efficiency of high power switching applications.

Approaches to reduce collapse include reducing the electric field for injection, limit the absolute number of traps available and increase the pathway resistances between electrons and traps [1.12]. Surface passivation can prevent the formation of the virtual gate though it might decrease the breakdown voltage of the device. However, since the surface states are indispensable to the system, passivation is essential to reduce current collapse. The passivant might make surface donors inaccessible to electrons leaking from the gate metal or the process of depositing silicon nitride passivant causes Si to incorporate as a shallow donor at the AlGaN surface in sufficiently large quantities to replace the surface donors and prevent current collapse.

However, if the AlGaN/passivant interface or bulk of the passivant contains charge-trapping sites, then electrons leaking from the gate metal under the influence of large electric fields during high power operation can get trapped. The trapped negative charge can cause a negatively charged virtual gate to develop in a manner similar to that on an unpassivated surface. This can negatively influence long time stability and reliability of the device characteristics. Compression of gate current could lead to signal distortion and reduction of efficiency. In addition, impurities such as C or Fe that are added to increase buffer layer resistance could also introduce more traps. The doping, nucleation layer and substrate choices are being continually optimized in coordination with understanding and improving epitaxial growth techniques [1.5, 1.12 and 1.91].

Field plate technology [1.74, 1.111-1.112] is an innovation that has tackled this problem by reducing the absolute peak and laterally distributing the electric field near gate and drain, thus suppressing surface high field trapping effects.

Gate Lag and Drain Lag

In modern devices usually built with passivation and field plates, DC current collapse is usually measured as changes in drain current before and after certain quiescent gate and drain biases are applied inducing specific kinds of trapping in the device [1.106, 1.109]. Abrupt changes in gate and drain biases induce slower current transients that lag behind the applied voltage, phenomena individually referred to as gate-lag and drain lag respectively [1.49, 1.105-1.106, 1.109]. These lags in combination translate to current collapse in microwave devices since pulsed or RF drain currents obtained are notably lower than predicted from DC operation. Ghosh et al. [1.106] in Figure 1.22 studied the collapse magnitudes near the knee and saturation voltages for 3 sets of devices and 4 quiescent biases showing that the collapse significantly degrades the response near the knee voltage.

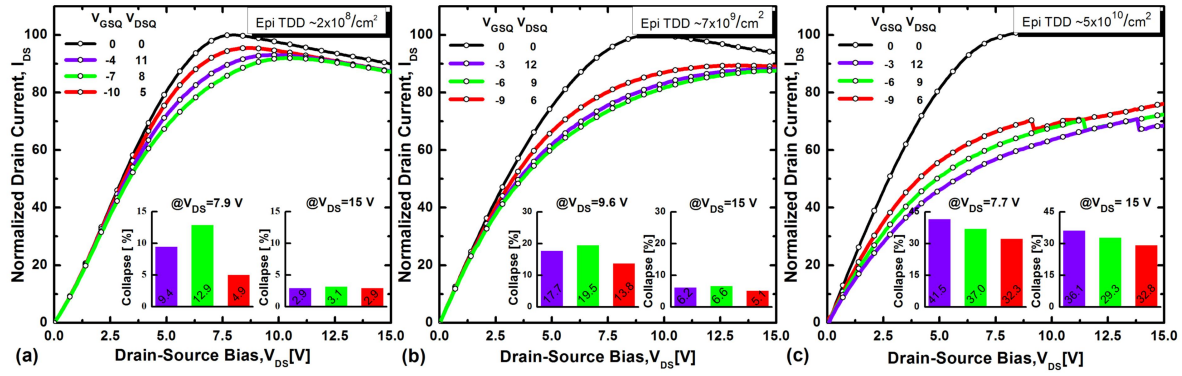

Figure 1.22 : Normalized pulsed I–V for (a) V_{th}=−4 V, (b) V_{th}=−3 V, (c) V_{th}=−3 V, for varying static or dynamic quiescent biases (with identical cumulative reverse V_{DG}). For different bias schemes, the collapse magnitudes in the knee and in the saturation region are shown in the insets [1.106].

Gate lag measurements compare the prompt and steady state I_D at a constant low field drain voltage (avoid self-heating contributions) while the gate bias is modulated from a quiescent point usually below the pinch off voltage ~ V_G= -6 V to an open channel condition such as V_G= 0 V. At pinch-off, a high amount of channel electrons are trapped in bulk or surface states, which do not immediately feed back into the channel instantaneously when the gate turns on. With large-signal recovery time constants up to the order of seconds, the responsible traps must have a significantly large activation energy and/or they must be fed by a "slow" conducting mechanism (like hopping), in order to explain the long time constants. Surface states are believed to be dominant in gate lag since passivation significantly improves the current response.

For drain lag measurements, the gate voltage is kept constant around 0V while the drain voltage is shifted from an equilibrium low value ~10-100 mV to a higher value 15-30 V. Buffer traps are reported to be dominant here since devices with higher buffer layer conductivities display lower drain lag ratios. High drain biases inject electrons into the buffer where they stay trapped. Passivation has minimal effect and hot electrons can be a major contributing factor. The recovery time is often in minutes and the reduction in knee voltages and $I_{D,max}$ is amplified. Threshold shifts associated with current collapse are also accounted to the drain lag effect.

Faqir et al. [1.108] and Brunel et al. [1.113] individually studied current collapse in the UMS GH50 technology as presented in Figure 1.23. In the first case, gate lag components due to traps presumed to be in the barrier/surface were found to be dominant. Drain lag presumably due to buffer traps was found to be less relevant. In the second case study however, drain lag seems to be the dominant contributor to current collapse.

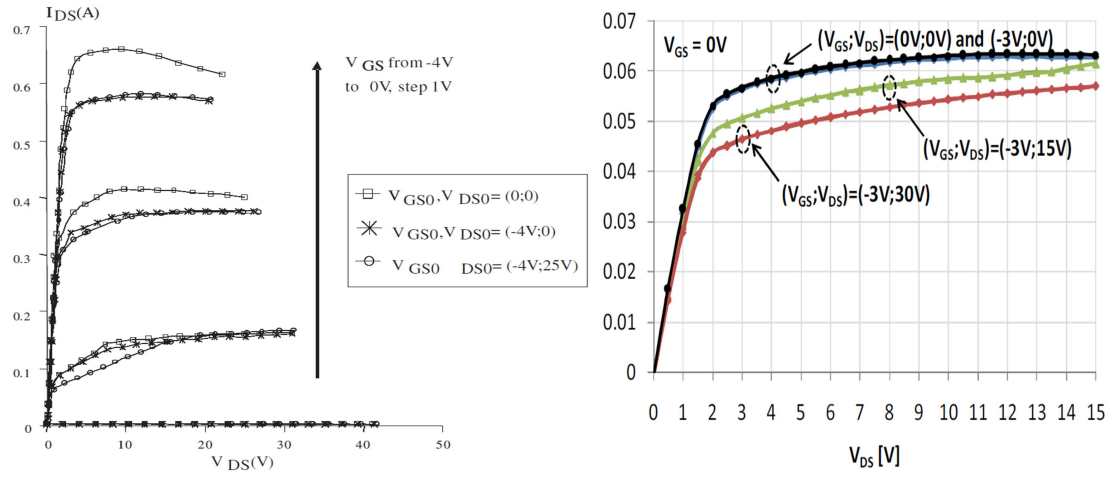

Figure 1.23 : (left) Pulsed I_D-V_{DS} characteristics measured for V_{GS}= -4 to 0 V and for three quiescent biases (V_{GS}, V_{DS}) = (0, 0), (-4V, 0V) and (-4V, 20 V) [1.108] and (right) Output characteristics in pulsed mode at V_{GS}=0V and 300K for 4 quiescent points [1.113]

Kink effect

The phenomenon of an undesirable change in the output I-V characteristics due to alterations in the drain conductance is referred to as the kink effect [1.14, 1.110 and 1.113], which depends on the device operating point, current, voltage and temperature. This is observable when we compare output characteristics obtained with upward and downward pumping of V_{DS} with long integration times as observed in Figure 1.24.

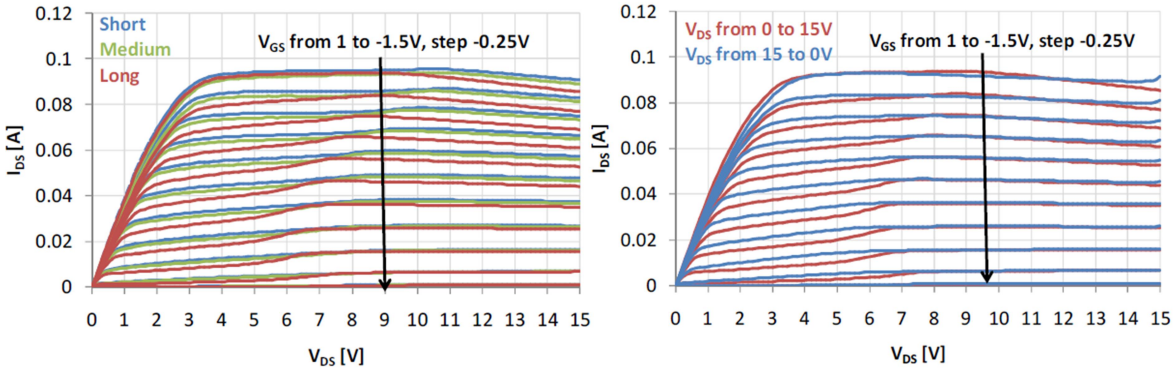

Figure 1.24 : (left) Static $I_{DS}(V_{DS})$ characteristic at 300K and (right) comparison between upward (V_{DS} from 0-15V) and downward (V_{DS} from 15-0V) pumping in long integration time configuration [1.113]

A lowering in the drain current near a $V_{DS,kink}$ position is observed for upward pumping while it disappears when V_{DS} is pumped down from a high value. Hence, it is linked to the electric field between the drain and source and the lowered g_d can be accounted to trapping states. This is also derivable from the kink magnitude being independent of the operating V_{GS} value, thus showing that a high drain current is not essential to trap filling. Since the kink magnitude (~ change in g_d) changes with temperature, the phenomena are thermally activated [1.113]. The traps responsible are assumed to be in the GaN buffer below the gate since the associated time constants are long and the effect being unidentifiable in pulsed mode operation. Since a downward pumping (V_{GS}=0V and V_{DS} from 15 to 0V) leads to partial recovery of the drain current, de-trapping processes could be faster when the device is biased at low or decreasing electric field conditions.

Kaushik et al. [1.110] proposed the kink mechanism to be a consequence of the virtual gate phenomenon. A high resistance region of 20-80 nm formed below the virtual gate in the channel region would be very sensitive to electric field and temperature. At low V_{DS}, the field is high enough to initiate the tunneling of electrons to surface states while the device temperature remains relatively constant. As V_{DS} increases further, the temperature of the channel starts rising due to self-heating which restricts further lengthening of the virtual gate at higher V_{DG}. Thus, the channel resistance stops rising. The dynamic balance between channel current and V_{DG} is achieved at a particular

temperature resulting in the collapsed kink-like feature. The I_{DS} in this region is very sensitive to change. When V_{DS} crosses a critical $V_{DS,Kink}$, I_{DS} suddenly increases and approaches saturation level since the dynamic resistance region under the virtual gate reduces suddenly, resembling the cut-in point of an "n+-n−-n+ diode" with very small cross-sectional area. When the device temperature increases, the cut-in voltage decreases, the resistance can be overcome at lower voltages until the kink becomes almost negligible (>500 K).

Runaway effect

The runaway effect is a parasitic phenomenon that has been observed in the UMS GH-25 technology devices [1.114-1.115] and characterized as a simultaneous increase in gate and drain currents when the drain voltage is increased in the saturation regime. Normally, the gate leakage is dominated by the gate-drain diode component hence increases with V_{DS} near threshold conditions. As $|V_{GS}|$ is lowered, the gate leakage is expected to reduce. However, in runaway mode the absolute gate current is higher for lower $|V_{GS}|$ values as demonstrated in Figure 1.25. This affects RF performance of the devices since higher gate leakage reduces the available RF output power under high compression.

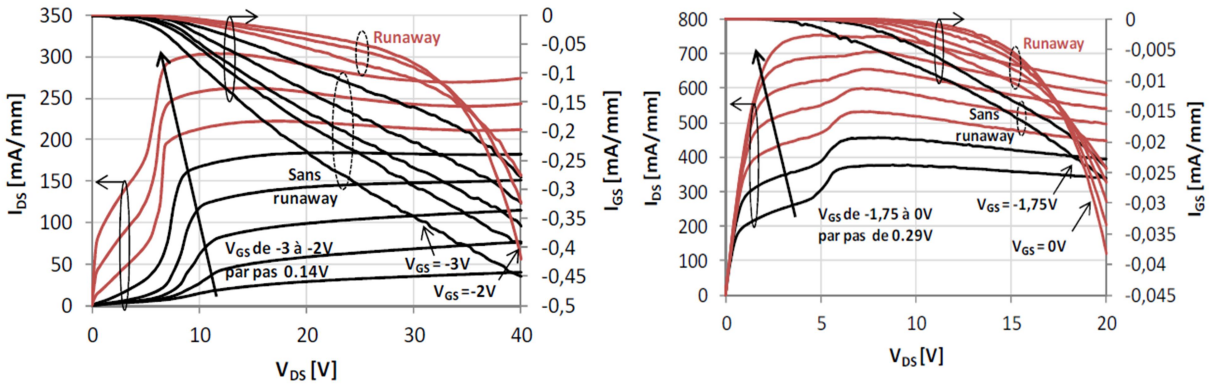

Figure 1.25 : Measurements illustrating the runaway effect for two gate voltage ranges [1.114]

It could be especially detrimental to perform reliability characterizations after runaway-inducing aging tests since the continual increase in I_G and I_D might lead to catastrophic failure essentially making runaway an end of life mechanism. There is a critical gate and drain voltage for runaway to be observed. In open channel conditions, the runaway is shifted to lower V_{DS} values and more negative values of V_G. Higher temperatures and longer aging times also promote lower activation voltages. The study of conduction mechanisms seems to suggest a connection of runaway with the Fowler-Nordheim tunneling mechanism. Brunel et al. [1.114] have proposed a mechanism for the runaway phenomenon, which has been summarized in the following Figure 1.26 .

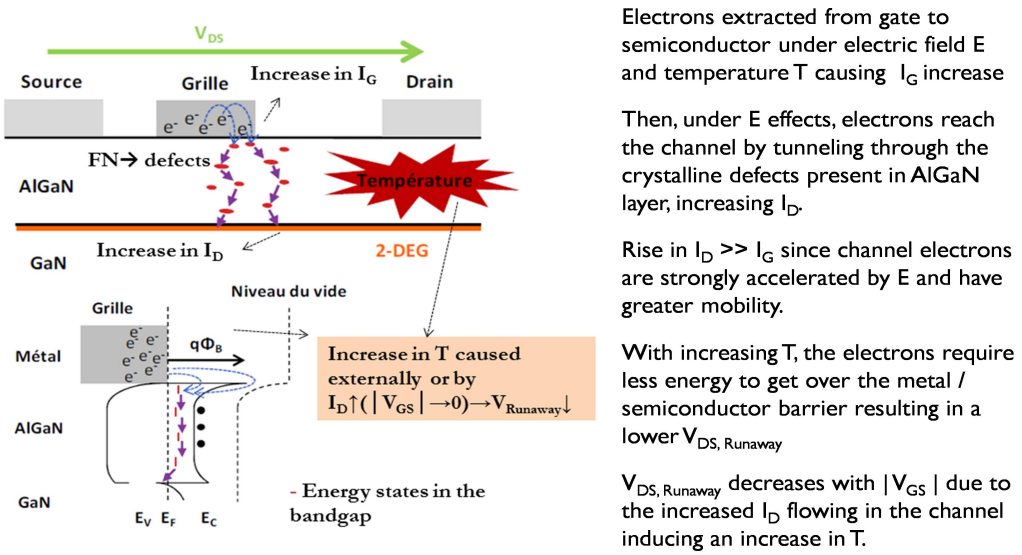

Figure 1.26 : Mechanisms of the runaway effect as proposed by Brunel et al. [1.114]

Belly Shape Effect

The belly shape effect (BS) is an electrical parasitic phenomenon that was recently discovered in UMS GH 50 and GH 25 technologies by Brunel et al. [1.116-1.117] where an excess of gate leakage current resembling a "belly shape" feature is observed on Schottky forward characteristic after HTOL or HTRB reliability tests. A typical belly shape characteristic is displayed in Figure 1.27.

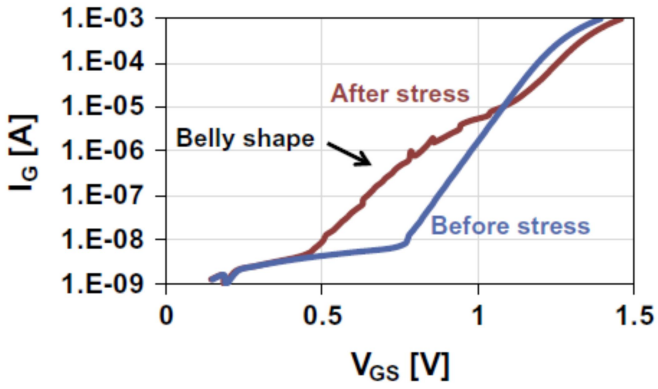

Figure 1.27 :Schottky diode forward characteristics with drain and source shorted to the ground of a HEMT with BS before (blue) and after (red) 4000 h of HTRB stress [1.116]

BS appears after only few hours of aging with unpredictable magnitudes during the aging time suggesting degradations induced by changes in metal, epitaxial layers or surface states.

However, its origin mechanisms remain unclear and require further analysis to address reliability manifestations. It provides an interesting case study into internal physics and circumstances that could lead to such excessive leakage currents without significantly worsening overall reliability.

1.6 Conclusion and Perspectives

The GaN HEMT is a promising device for the near future of the semiconductor market due to its material and functional advantages. The current state of demand and predicted growth rates for GaN based products are summarized for major RF and power markets. The physics and advantages of III-N materials are discussed to build an understanding into the superior potential of the GaN based devices. The theory of spontaneous and polarization effects are explored in detail since they are responsible for the high channel density at the AlGaN/GaN hetero-interface.

The operation and the control factors in the performance of AlGaN/GaN HEMTs are discussed including the composition and thickness of the pivotal AlGaN layer. The origins of physical degradation mechanisms in these devices because of various stress factors are discussed. The major reliability issues observed in GaN HEMTs as a consequence of trap effects such as current collapse, gate and drain lag are discussed briefly.

The UMS GH-25 process provides a good device platform to investigate widely prevalent trapping phenomena, which enables further insight into specific manifestations of such trap-limited behaviour such as the runaway mechanism or the recent belly shape effect. The structural, operational and reliability characteristics of this process are briefly summarized.

Reliability studies tackling operational drawbacks of GaN HEMTs are important in ensuring the growth and success of its application areas. Chapter 2 and Chapter 3 deal with understanding and simulating the trap limited behaviour through study of the gate leakage current and transient simulations respectively. They capture not just evident trap impacts but also more sensitive device responses under varying constraints. In addition to further investigations into the belly shape nature, Chapter 4 also employs techniques developed in the previous chapters to supplement dedicated research into belly shape trigger or support mechanisms.

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CHAPTER 2

Simulation Fundamentals and Gate Leakage Analysis

MODELS AND APPROACH

2.1 Introduction to T-CAD Environment

Physics based modelling is essential alongside electrical characterization techniques to understand and predict potential issues or advantages as well as structural and behavioral optimization of given configurations.

Technology Computer-Aided Design (T-CAD) [2.1-2.4] provides a framework for design automation to model and describe the processes of semiconductor development, fabrication and operation with the aid of computer solutions. Solving fundamental differential equations that describe the device, the software can reproduce and envision the electrical behavior to develop a model for a particularly designed structure. The aim of TCAD is to enable a quantifiable link between structural description and electrical response to identify which physical phenomena and associated electrical model parameters are most relevant or crucial within a defined setting. In conjunction with electrical data, it provides a deep physical understanding that might not otherwise be discernible even after several additional costly and demanding test runs.

Sentaurus [2.1] is one such T-CAD software developed by Synopsys based on finite element analysis. The system numerically analyzes equations with respect to boundary conditions to obtain approximations for essential parameters at discrete points i.e. finite elements. Over the entire domain, this is a bottom-up problem solving approach to assemble the results of each point into a complete model for a given system. It is a fast and efficient method to explore varying constraints in a given scenario. Figure 2.1 summarizes major blocks of the Sentaurus environment [2.1].

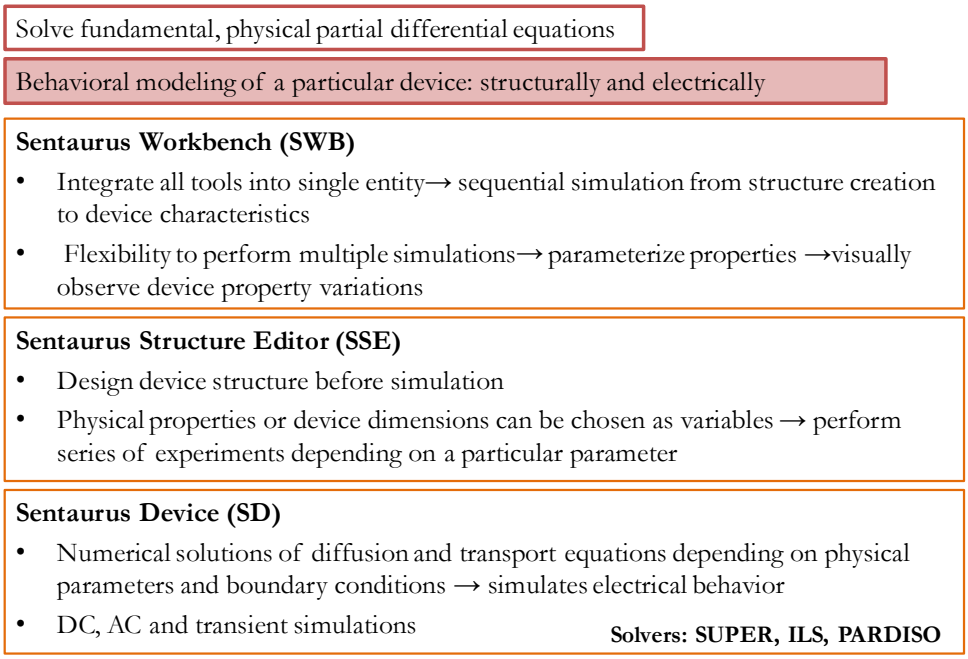

Figure 2.1 Different blocks of the Sentaurus environment

Sentaurus Workbench (SWB) is the central tool that integrates the other tools into a single sequential setup. There is a visual and functional simulation flow from creating the structure to device biasing and operation. It can simultaneously run multiple simulations on a single device by parameterizing the structural and physical properties. This allows comparing the effect of parameter choices on device behavior within a single project, but for different experimental scenarios.

Sentaurus Structure Editor (SSE) designs the device structure, the first step of model development. Due to the inherent flexibility, the user can set as variable, any physical property or device dimension, to compare operational advantages or sensitivity to modifications thus aiding in fabrication choices. It is responsible for creating the mesh by dividing the built structure into a tight network of discrete points. The physical equations are solved for each of the meshing points and the output contains geometrical and material details in addition to contact and doping definitions. This defines the input framework for all successive simulations, which capture device operation.

Sentaurus Device (SD) solves the activated set of diffusion and transport equations based on user-defined physical parameters and boundary conditions, to simulate the virtual device. This tool utilizes models to reproduce the physics as well as account for specific operational conditions. It can be used to perform DC, AC and transient simulations and the output provides information on quantities such as carrier densities, electric fields, potentials, energy levels and temperatures inside the device at various times during the simulation. Visualization tools such as Tecplot SV and Inspect allow us to observe the 3D and 2D variations respectively, within the device.

A. SENTAURUS TRANSPORT MODELS

As derivations of the Boltzmann transport equation, Sentaurus provides three general carrier transport models for varying modeling requirements or conditions, and control current flow. The models are: Drift-diffusion (DD), Thermodynamic (TD) and Hydrodynamic (HD) [2.1].

Drift-Diffusion

The default model is based on the drift diffusion current transport hypothesis, which approximates that the flow of carriers within a device occurs due to a combination of diffusion and drift under the influence of an external field. It also assumes a concurrent recombination and generation of carriers, which controls the carrier density. The electron and hole current densities under this model are derived directly from semiconductor theory. For the drift current component controlled by the electric field E, the charge movement is expressed as the product of electron and hole volume densities and the average drift velocity v_d as follows:

$$J_{Dr} = \rho v_d = J_{n,Dr} + J_{p,Dr} = (-en)(-\mu_n E) + (ep)(\mu_p E) = e(\mu_n n + \mu_p p)E = \sigma E \tag{2.1}$$

When a particle accelerates in a crystal the velocity increases with the electric field. If the charged carrier collides with an atom within the crystal, most of the particle energy is lost. The particle then recommences to gain energy and accelerate until it suffers another scattering process. While this process repeats, the particle possesses an average drift velocity which, for low electric field, is directly proportional to the field. We may then write (2.1, 2.6):

$$v_{dr,p} = \mu_p E \; and \; v_{dr,n} = \mu_n E \tag{2.2}$$

The following can be obtained from derivation for a hole with effective mass m_p under an external force F:

$$F = m_p \frac{dv}{dt} = eE \tag{2.3}$$

On integration, we obtain the drift velocity as

$$v_{dr,p} = \int \frac{eE}{m_p} dt \;\; hence \; \mu_p = \frac{v_{dr,p}}{E} = \frac{e\tau_{co,p}}{m_p} \; and \; \mu_n = \frac{v_{dr,n}}{E} = \frac{e\tau_{co,n}}{m_n} \tag{2.4}$$

where, $\tau_{co,n}$ and $\tau_{co,p}$ are mean times between particle collisions of electrons and holes.

For diffusion transport, the movement describes the flow of electrons or holes from high concentration to low concentration which is proportional to the free density of carriers. If the flux of electrons is flowing in the negative x direction, then the current flow is conventionally in the positive x direction. The diffusion current components are given as:

$$J_{n,Di} = -eR_f = +ev_t l\frac{dn}{dx} = eD_n\frac{dn}{dx}\ and\ J_{p,Di} = -eD_p\frac{dn}{dx} \tag{2.5}$$

Where $\mathrm{D_n}$ and $\mathrm{D_p}$ are diffusion coefficients which take into account the average distance between collisions. Equating n and p with Φ, the quasi fermi potentials where Ψ represents the electrostatic potential, the current density equations can be formulated as a combination of the drift and diffusion components as follows:

$$J_n = -nq\mu_n\nabla\Phi_n \qquad\qquad J_p = -pq\mu_n\nabla\Phi_p \tag{2.6}$$

$$n = n_{i,eff}\ exp\left(-\frac{q(\Phi_n - \Psi)}{kT}\right) \tag{2.7}$$

$$p = p_{i,eff}\ exp\left(-\frac{q\left(\Phi_p - \Psi\right)}{kT}\right) \tag{2.8}$$

Thus,

$$\overrightarrow{J_p} = qp\mu_p\,\vec{E} - qD_p\nabla p \tag{2.9}$$

$$\overrightarrow{J_n} = qn\mu_n\,\vec{E} + qD_n\nabla n \tag{2.10}$$

The drift and diffusion constants are related by the Einstein's equation:

$$D_{n,p} = \frac{kT}{q}\mu_{n,p} \tag{2.11}$$

This approach offers high speed and good accuracy for most device conditions in low to medium stress conditions and supports versatility in simulation approaches.

Thermodynamic Model

The Thermodynamic Model is a non-isothermal model which extends the drift-diffusion model by incorporating additional terms to consider electro-thermal effects [2.1, 2.7-2.8]. This model assumes a state of thermal equilibrium between the charges and the lattice which allows a unified expression of carrier and lattice temperatures.

Hence, extra lattice temperature gradients derived from the lattice heat flow equation are inserted within the continuity equations:

$$\overrightarrow{J_n} = -nq\mu_n(\nabla\Phi_n + P_n\nabla T) \tag{2.12}$$

$$\overrightarrow{J_p} = -pq\mu_p(\nabla\Phi_p + P_p\nabla T) \tag{2.13}$$

Where P_n and P_p are defined as the absolute thermoelectric powers.

This approach is important if modeling requirements extend to very high current or voltage operation regimes where self-heating is dominant.

Hydrodynamic Model

A deeper look at temperature effects on carrier transport requires the hydrodynamic model based on the principle of energy balance [2.9-2.12]. In this approach, the energy of each carrier is dependent on lattice and its own carrier temperature. In addition, current densities have contributions from spatial variations of electrostatic potential, electron affinities and band-gap [2.1]:

$$\overrightarrow{J_n} = q\mu_n(n\nabla E_C + kT_n\nabla n + f_n^{td}kn\nabla T_n - 1.5nkT_n\nabla lnm_n) \quad (2.14)$$

$$\overrightarrow{J_p} = q\mu_p(p\nabla E_V - kT_p\nabla p - f_p^{td}kp\nabla T_p - 1.5pkT_p\nabla lnm_p) \quad (2.15)$$

The final three terms represent concentration gradient, carrier temperature gradient and spatial variation of the carrier effective mass. This model is a better substitute to the DD approach in simulations at high electric fields, especially when dealing with hot electrons, velocity overshoot and impact ionization effects. However, its relevance trades off with the associated increase in simulation time and computational complexity.

B. STRUCTURE DETAILS

The first 2D virtual structure employed for simulation studies on UMS GH-25 technology is presented in Figure 2.2. It is a slightly simplified version of the UMS AlGaN/GaN HEMT without the gate detail and field plates, but otherwise representative of the internal dimensions and properties of the GH-25 process. The gate is defined as a Schottky contact. The gate-source and gate-drain passivation lengths are L_{SG}= 0.8 µm and L_{GD}= 1.7µm respectively. An area factor of 1000 µm is defined to represent width of the 2D device and obtain output currents normalized to A/mm. The source and the drain regions are defined in Sentaurus as "modified ohmic" contacts [2.1].

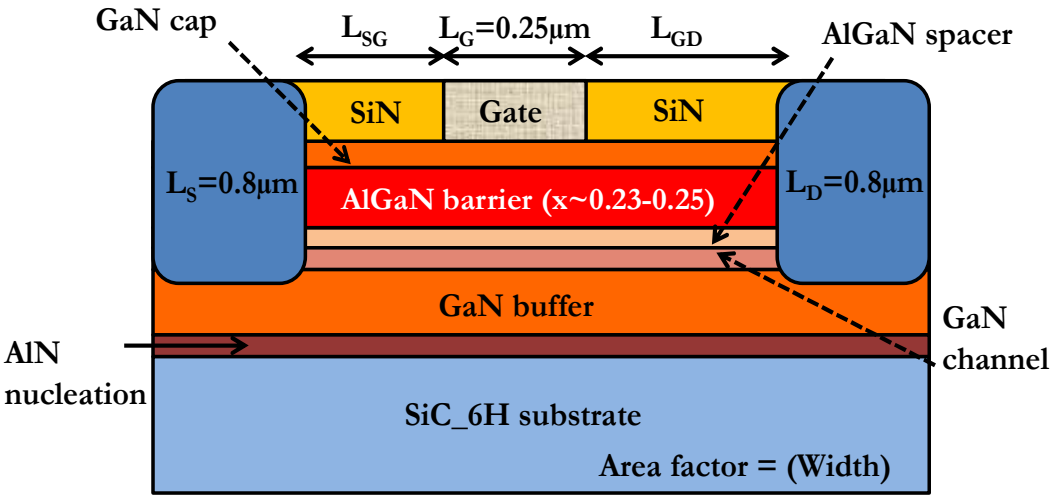

Figure 2.2: Initial 2D TCAD simulation structure for the UMS GH 25 technology

This definition reproduces the electrical behavior of an ohmic contact without imposing the charge neutrality condition at contact vertices. This helps to prevent inaccurate simulations around charged depletion regions. A thin AlGaN spacer separates the AlGaN barrier (x= 0.25) from the GaN buffer but all the layers are minimally doped ~1-2 x 10^{15} cm^{-3}. Only the 2 nm GaN cap is n-doped with N_A= 10^{18} cm^{-3}. The SiC (6H) substrate of 100 µm is defined with a thin layer of AlN nucleation. The default numerical Sdevice solver SUPER that is quite robust and accurate for multipurpose 2 D simulations is used for all simulations.

Mesh Considerations

The built device as presented in-scale in Figure 2.3 (left) then needs to be distributed into finite elements to discretize its physical properties by an efficient meshing strategy (Figure 2.3 (right)) which enables the numeric simulation of the defined structure.

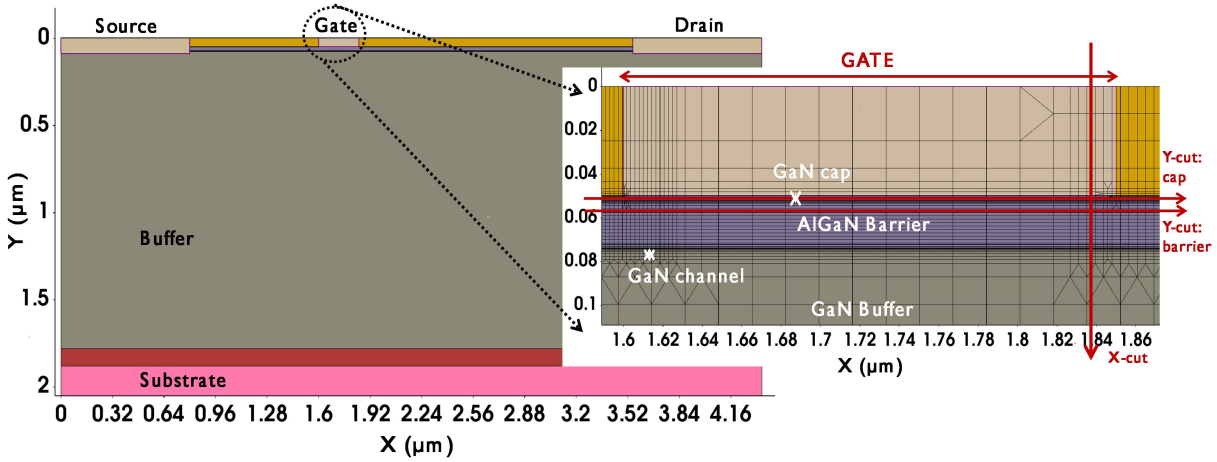

Figure 2.3: Sentaurus 2D-TCAD structure displaying mesh strategy close to the gate

A non-uniform mesh is needed to balance simulation accuracy and time. It should be denser near critical or sensitive regions and interfaces of the device where more meshing points need to be compiled to capture the internal changes in the distribution of quantities such as electric fields or current densities. To save on computational time, the mesh can be wider in regions with lower current, field or potential gradients.

In this structure, the mesh is notably finer at gate edges, especially at the gate-drain, and all semiconductor interfaces, to ensure both robust and efficient simulation. It is also finer around the channel layer where electron densities are high. To observe distributions of physical quantities within the structure, usually an X-cut or Y-cut in Sentaurus is employed as shown in Figure 2.3 (left). Unless otherwise stated, all X positions are chosen close to the critical gate-drain edge. Y positions could be chosen in the cap or buffer to visualize the behavior close to the surface.

2.2 Foundation of GaN HEMT Simulations

The next step after defining the structure is to introduce fundamental physical models [2.1, 2.5] that need to be activated to reproduce GaN HEMT operation.

The Drift-Diffusion model for carrier densities is first activated. Realistic Fermi statistics [2.13] is employed for its importance to the GaN HEMT with high carrier densities ~ 10^{19} cm^{-3}, as obtained in the 2-DEG channel. Thermionic model [2.14-2.15] is used to reproduce the gate current characteristics in regard to the hetero-interfaces. For the bandgap model, the BennettWilson [2.16] approach is used. Band gap narrowing has been turned off in the simulations since there is minimal doping within the structure. The Anisotropic [2.1] model is activated within the Poisson equation to represent the anisotropic dielectric properties associated with GaN. For the recombination-generation of carriers, the Shockley-Read-Hall (SRH) and Auger models [2.1] have been activated for their relevance at high carrier densities.

A. MODEL IMPLEMENTATIONS

Carrier Mobility and Velocity

The higher peak velocity and saturation velocity is what makes GaN ideal for power applications, despite the higher 2DEG mobility obtained with GaAs. At low electric fields, the carrier velocity can be described as a function of the applied electric field with its dependence being the low field mobility i.e. $v(E) = \mu_{low}E$. The constant mobility model is activated by default and accounts for phonon scattering as a function of lattice temperature [2.17].

$$\mu_{const} = \mu_L \left(\frac{T}{300K}\right)^{-\zeta} \tag{2.16}$$

where μ_L is the mobility corresponding to bulk phonon scattering. The values activated for GaN are μ_L (electron, hole) = 1700, 20 $cm^2/V.s$ and ζ= (1, 2.1).

To improve the preciseness, Arora's doping dependence [2.18] model using Arora parameters to account for total and effective doping influences is also activated for GaN

$$\mu_{dop} = \mu_{min} + \frac{\mu_d}{1 + \left(\frac{N_{total}}{N_0}\right)^{A*}} \tag{2.17}$$

The accurate value for μ_{low} can be obtained according to Matthiessen's rule [2.1].

$$\frac{1}{\mu_{low}} = \frac{1}{\mu_{const}} + \frac{1}{\mu_{dop}} + \cdots \frac{1}{\mu_n} \tag{2.18}$$

At high electric fields however, the electron velocity saturates leading to a constant v_{sat}, while the simple proportional relation in eq. [2.16] is no longer valid. For wide bandgap materials which often operate at high electric fields, velocity saturation modeling becomes important i.e. $\mu = f(\mu_{low}, F_{hfs})$ where F_{hfs} is the driving force. The extended Canali model is activated [2.19-2.20] to model velocity saturation with α and β as adjustment parameters as:

$$\mu(F) = \frac{(\alpha+1)\mu_{low}}{\alpha + \left[1 + \left(\frac{(\alpha+1)\mu_{low}F_{hfs}}{v_{sat}}\right)^{\beta}\right]^{1/\beta}} \tag{2.19}$$

For materials such as GaAs and GaN where inter-valley carrier transfer is probable at high fields, the mobility also has a representation according to the Transferred Electron Model [2.21] applicable to all transport models. Simulating this effect is complicated but physically suitable for GaN and hetero-junction devices where high electric field could induce negative differential electron mobilities. It takes into account the transfer of electrons into energetically higher side valleys of higher effective mass. The Transferred Electron Model 2 (TEM2) [2.1] is chosen where the mobility is written as a unification of two different models as:

$$\mu = \frac{\mu_{low} + \mu_1\left(\frac{F_{hfs}}{E_0}\right)^{\alpha} + v_{sat}\frac{F_{hfs}^{\beta-1}}{E_1^{\beta}}}{1 + \gamma\left(\frac{F_{hfs}}{E_0}\right)^{\alpha} + \left(\frac{F_{hfs}}{E_1}\right)^{\beta}} \tag{2.20}$$

Here, E_0 is the critical electric field at which velocity overshoot occurs. α has a maximum value of 4 when implemented in Sentaurus. F_{hfs} is computed as a gradient of the electron quasi Fermi level. This model however causes convergence issues. Because α is the exponent, it cannot be included as a model parameter and is unmodifiable in the overshoot region. E_0 gets overestimated as overshoot occurs at lower electric field than predicted accurately by Monte Carlo simulations. The parameters for TEM-2 need optimization from the default GaAs values to minimize the error due to Canali model. The general parameter values for AlGaN/GaN structures are presented in Table 2.1.

Table 2.1: TEM 2 Model parameters for AlGaN/GaN heterostructures [2.1]

Material	μ_1 (cm^2/Vs)	$E_0 = E_1$ (V/cm)	α	β	γ
GaN	0	220893.6	0.7857	7.2044	6.1973
$Al_{0.2}Ga_{0.8}N$	0	245579.4	0.7897	7.8138	6.9502
AlN	0	447033.9	0.8554	17.3681	8.7253

Polarization Effects

Proper representation of polarization charges is a critical concern in correctly simulating the GaN based HEMT. The Piezoelectric Polarization [2.1] model is activated which internally calculates the spontaneous and piezoelectric polarization charges at each interface of the structure.

The default elastic and stiffness coefficients defined for GaN and AlGaN in Sentaurus are defined in Table 2.2.

Table 2.2: Elastic and stiffness coefficients as defined in Sentaurus parameter files

Parameter	GaN	AlN	AlGaN
P_{SP} (C/m^2)	0.029	0.081	0.042
e_{31} (C/m^2)	-0.35	-0.5	-0.387
e_{33} (C/m^2)	1.27	1.79	1.4
C_{13} (Gpa)	106	108	106.5
C_{33} (Gpa)	398	373	391.75
a_0 (Å)	3.189	3.112	3.17
c_0 (Å)	5.185	4.982	5.134

The model computes the charges as a function of strain as well as an additional contribution dependent on the gate [2.1, 2.22-2.23].

The polarization vector in Sentaurus is written as:

$$\begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} P_x^{sp} \\ P_y^{sp} \\ P_z^{sp} + 2d_{31}.strain.\left(c_{11} + c_{12} - 2c_{13}^2/c_{33}\right) \end{bmatrix} \tag{2.21}$$

To account for the inverse piezoelectric effect, the gate-dependent additional term is added:

$$P_{add} = \frac{e_{33}^2}{c_{33}}(E_z) \tag{2.22}$$

where E_z is the vertical component of the electric field and has been calculated from results as $E_Z = 0.68 \times 10^6$ V/cm. The value of polarization charge at the AlGaN/GaN interface obtained with Sentaurus defaults is $P_{PE} = 5.07 \times 10^{-6}$ C/m^2. The gate component is an additonal $P_{add} = 0.34 \times 10^{-6}$ C/m^2 to have a total value of $P_{PE,Tot} = 5.41 \times 10^{-6}$ C/m^2. This value is in close correspondence with

other works that calculate P_{PE} without consideration of P_{add} ([2.4] with $P_{PE,Tot} = 5.2 \times 10^{-6}$ C/m^2), ([2.6] with $P_{PE} = 5.15 \times 10^{-6}$ C/m^2) and ([2.23] with 5.008×10^{-6} C/m^2].

To have a complete representation of polarization effects, in addition to specifying the Piezoelectric Polarization model, it is essential to define a surface donor density corresponding to the traps at the top interface responsible for supporting 2-DEG formation as discussed in Chapter 1. The definition of concentration and energy position of these traps will be explored in the Section 2.3.

Density Gradient Model

The 2-DEG in a GAN HEMT exists in the triangular potential well as a result of band discontinuity with a quantization of energies. Thus, electron distribution within the 2DEG is different from normal bulk distributions. By default, the quantization effects are ignored. Ideally, the Schrodinger equation should be solved. But this option only exists for one dimensional simulation.

The density gradient model allows a good compromise with medium addition of simulation time and effort. It changes the conduction and valence band distribution into discrete-like states that represent quantization.

Mathematically, an additional term $\boldsymbol{\Lambda_n}$ is added to the conduction band energy equation with γ as a fitting parameter [2.1, 2.24-2.25]:

$$n = N_C F_{1/2}\left(\frac{E_{F,n} - E_C - \boldsymbol{\Lambda}_n}{kT_n}\right) \; where \;\; \boldsymbol{\Lambda}_n = -\frac{\gamma h^2}{6m_n}\frac{\nabla^2\sqrt{n}}{\sqrt{n}} \tag{2.23}$$

It does not significantly affect the I-V characteristics of the device but it does improve channel density representation and calculations as can be seen, from the electron density simulation for a X-cut close to the GD edge for V_D= 0 V, 20 V in Figure 2.4.

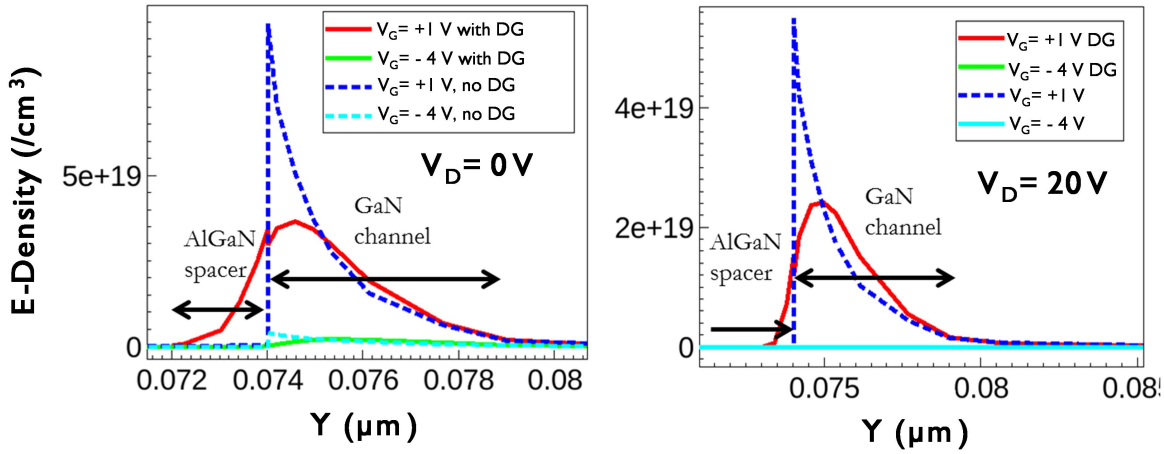

Figure 2.4: Channel density simulation comparisons with and without density gradient (DG) model

The peak of the 2-DEG is rounded and lower. The spread of electron distribution into adjacent layers instead of being sharply confined at the defined channel region interface presents a more realistic approach towards modelling the electron gas.

B. DATA FLOW

After the basic physical models have been defined in the central command file and the material parameter values for all relevant III-N semiconductors included in the parameter file, the system needs to be solved for DC analysis at varying bias conditions.

As illustrated in Figure 2.5, the framework to obtain gate and drain characteristics is established across a single SSE (for structure and mesh) and multiple SD nodes.

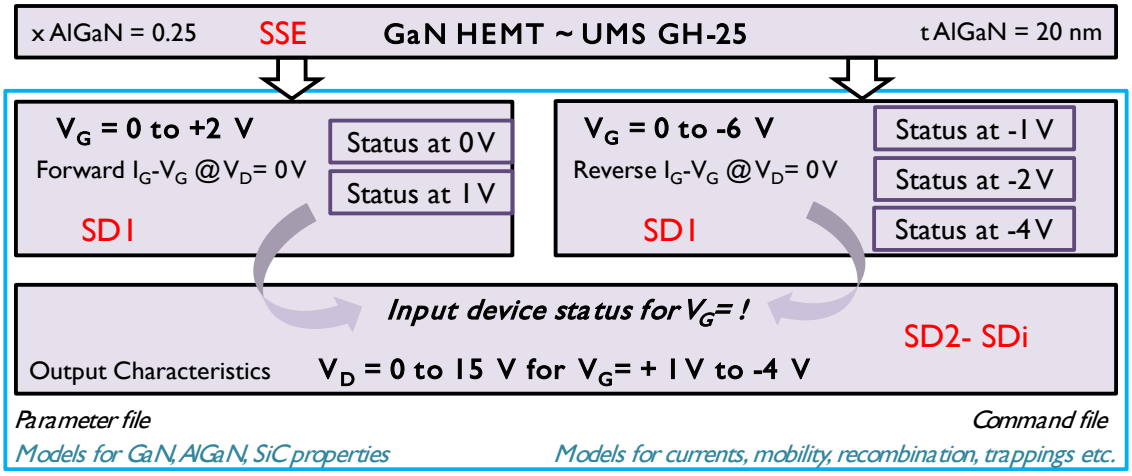

Figure 2.5: Description of the simulation result compilation

First the equilibrium solution of the device is computed by solving the Poisson and continuity equations at zero gate and drain biases.

In the next SD node, V_G is ramped in quasi-stationary mode in positive and reverse directions to obtain the forward and reverse gate current characteristics at V_D= 0V.

During the V_G sweeps, the state of the virtual device is saved at different points to obtain the solved characteristic at each V_G bias condition. This avoids re-computing the starting point in the next set of output I_D-V_D characteristic solutions where V_D is swept for constant V_G values. Instead, the saved file for each V_G is imported from the previous node thus saving simulation time.

Different output files at a chosen V_D can also be saved during the I_D-V_D sweep which could then be used to plot trans-conductance curves. Different SVisual modules fed from the previous SD node outputs could be added to automatically plot output or trans-conductance curves once the line of simulation finishes running.

2.3 Leakage Controlled Modeling

The model of a defined structure, with fundamental physics enabled, is now an ideal foundation to understand the models and approaches needed to accurately simulate the core of a representative GaN HEMT technology. TCAD has proven beneficial towards investigation of reliability concerns in several previous works [2.26-2.28]. The simulation of an III-N HEMT with its unique properties presents the research challenge of finding a modeling approach capable of isolating inherent correlations within factors controlling and modulating device behavior while developing the best representation of the technology under study. Defining reference values for major parameters that control the applicability of defined physical models is an important step.

The gate leakage current illustrates the robustness of the pivotal Schottky gate-drain region and is linked to many reliability issues. Reverse gate leakage is often substantially higher than predicted by thermionic emission which deteriorates high voltage operation and standby power dissipation [2.29-2.30]. Significant research has been performed to interpret gate leakage mechanisms [2.31-2.36]. Many works have confirmed the contribution of tunneling through the Schottky barrier to the increased leakage [2.32-2.34]. While Poole-Frenkel emission could assist conduction at high temperatures [2.34-2.35], surface trap related hopping conduction [2.36] and trap assisted tunneling mechanisms [2.32, 2.35-2.36] have also been reported.

Gate leakage still requires improved modeling, probably because it is susceptible to various factors or degradations that could be undiscernible or indistinguishable in other outputs. The I_D-V_D characteristic of slightly differing technologies might often be alike, but the I_G-V_G characteristic is more reflective of small contrasts and thus, more unique. From a simulation point of view, there could be several ways to fit an experimental I_D-V_D characteristic, while reproducing the I_G nature requires a deeper physical outlook, thus limiting the range of parameter variation. This is why modeling motivations behind the choice of certain parameter values for calibration of output characteristics are often unclear, even if a good fit is obtained.

This work aims to exploit the gate current sensitivity towards small variations as an advantage. Hence, the impact of dominant device simulation parameters is understood through their control over different regions of the gate leakage characteristic. Using the gate characteristic at the core of optimization offers a physics-based design approach to improve the accuracy of gate leakage simulations and simultaneously build a representative parameter set for a technology. Over the next sections, simulation parameters that primarily contribute to leakage current are identified and the process to correctly simulate these parameters while recognizing their physical limits is discussed.

Tunneling and traps, being two critical issues affecting leakage performance are carefully simulated through studying the parameters that describe them. A methodology is proposed to recognize the relative control of parameters on distinct regions of the I_G-V_G curve, aiding to distinguish parameters most relevant to performance optimization across different operational conditions or technologies.

A. IDEAL DEVICE PARAMETERS

Each parameter that needs a reference value for simulation of elemental device function is studied individually to determine a physically viable operational range through its impact on global I_G-V_G. These parameters define and control the simulated virtual device. To enable unambiguous inferences, the parameter variations are performed under degradation-free initial conditions. The activated thermionic emission model dominantly controls gate current response in this ideal model.

Schottky Gate: Metal Work Function

An essential step and a primary concern is the simulation of the gate current. The physics of the Schottky barrier was discussed in Chapter 1. The metal work function is a parameter that is to be chosen purely from device manufacturing constraints. Standard thermionic emission theory can be applied to extract the effective Schottky barrier height $\Phi_{B,eff}$ directly from the forward gate current I_{Forw} of the GH 25 device using the equation:

$$I_0 = AA^*T^2 exp\left(\frac{\Phi_{B,eff}}{\eta kT}\right) \tag{2.24}$$

I_0 is the saturation current obtained as the zero-bias intercept through extrapolation of the linear region of the forward gate current. A is the contact area, A* is the effective Richardson's constant, T is the absolute temperature and η is the ideality factor.

An $\Phi_{B,eff}$ ~ 0.9 eV has been previously extracted from UMS GH-25 measurements in [2.6], and also reported in other works [2.27, 2.37-2.39]. Schottky barrier Φ_B at the surface is theoretically defined as the difference of the gate metal work function Φ_{ms} and the electron affinity χ of the semiconductor. It is a preferable simulation technique to choose Φ_{ms} as a parameter instead of directly specifying Φ_B for Schottky contacts on semiconductors such that the $\Phi_{B,eff}$ is calculated internally. For the mole fraction range of x = 0.235–0.25 for the GH 25 device, a χ_{GaN} value of 3.9 eV and χ_{AlGaN} of 3.425–3.45 eV are considered in material parameter files [2.1].

A gate contact with Φ_{ms} = 4.4 eV thus well approximates the measured I_{Forw} current levels, resulting in an effective gate to channel barrier of ~ 0.9- 1 eV. Hence, it is chosen as reference for investigating the next parameters.

Schottky Gate: Gate Resistance

A distributed gate resistance (R_G) is the other major parameter defining a Schottky gate. As observed in Figure 2.6 , an increase in R_G reduces I_{Forw} in the high current regime (V_G > 1 V).

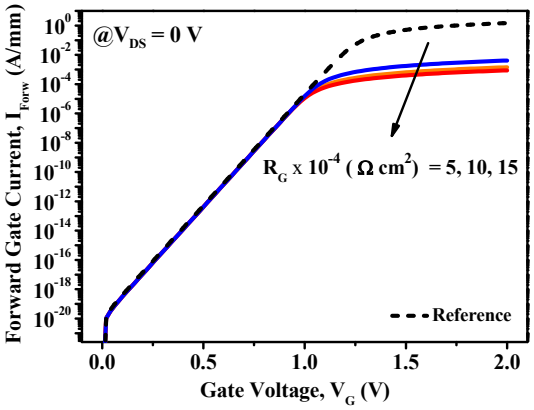

Figure 2.6: Forward I_G-V_G characteristics for varying R_G

However, as can be expected, the activation of R_G has no influence on simulated reverse gate characteristics (I_{Rev}). No R_G is defined in the reference to better isolate the effects of parameters described in the following sections.

Surface Donors

The GaN HEMT is singular because of the piezoelectric and spontaneous polarization charges at device interfaces, which require detailed modeling. The polarization charges at the interfaces are calculated by the Piezoelectric Polarization model. In addition, surface-donors which are inevitable and indispensable to GaN systems need to be defined at the top SiN/GaN cap interface to support and control the 2-DEG concentration formed in the quantum well at the AlGaN/GaN hetero-interface. Both S-D density ($N_{S\text{-}D}$ in cm^{-2}) and energy ($E_{S\text{-}D}$ in eV) need careful optimization for a given structure to sustain the complete activation of 2-DEG, and thereby achieve maximal device performance. Works on simulation of GaN HEMTs [2.37-2.38] generally choose surface donors based on fits to experiments, or previous literature.

However, reasons for which specific $N_{S\text{-}D}$ or $E_{S\text{-}D}$ values might be physically more suitable than others remain obscure. I_G-V_G characteristics offer a coherent approach towards interpreting the physical origin of changes due to variations in $N_{S\text{-}D}$ or $E_{S\text{-}D}$.

Surface Donor Concentration (N_{SD})

The primary factor governing $N_{S\text{-}D}$ validity at a given $E_{S\text{-}D}$ is the surface electric field E_{Surf}. Reverse gate I_{Rev} currents for varying $N_{S\text{-}D}$ at $E_{S\text{-}D}$ = 0.4 eV from MidBand (1.3 eV from E_C) are presented in Figure 2.7.

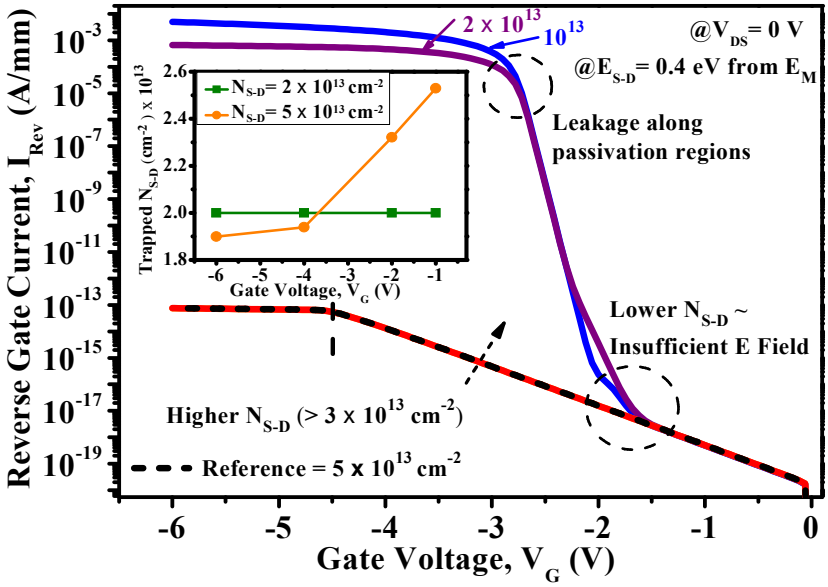

Figure 2.7: Reverse I_G-V_G Characteristics for varying N_{S-D}. Inset: Trapped N_{S-D} as a function of reverse V_G.

Figure 2.8 presents the corresponding surface donor occupation I_D behavior compared between N_{SD} values below and above the threshold.

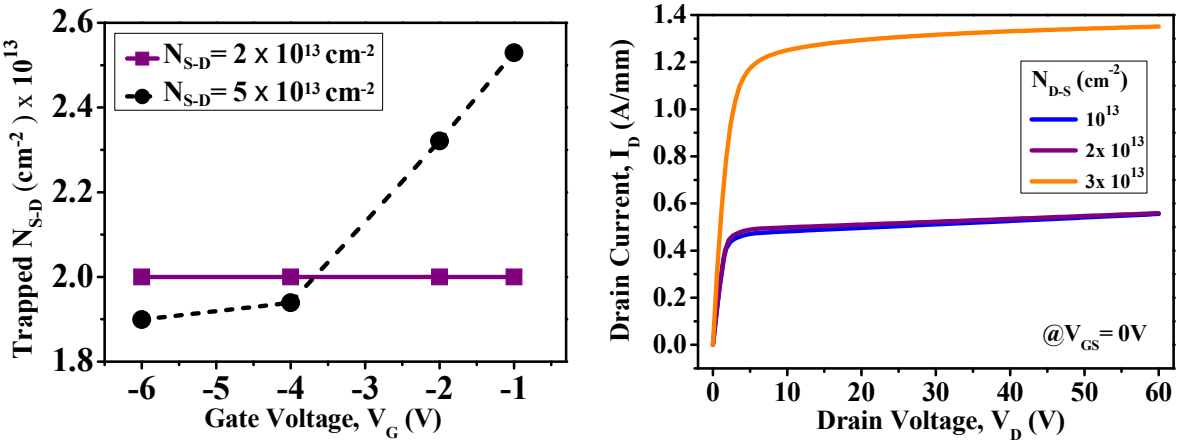

Figure 2.8: (Left) Trapped N_{S-D} as a function of reverse V_G for 2×10^{13} cm^{-2} (below the threshold) and 5×10^{13} cm^{-2} (above the threshold) (Right) I_D-V_D Characteristics for N_{S-D} : 1×10^{13} cm^{-2} to 3×10^{13} cm^{-2}.

A rapid growth in I_{Rev} can be observed for $N_{SD} < 3\times10^{13}$ cm^{-2} at low $|V_G|$ values. These N_{S-D} values are also associated with uncharacteristically low I_D levels as can be seen from (right) of Figure 2.8. Relative occupation of the defined N_{S-D} can be perceived from Figure 2.8 (left) through the evolution of the trapped (occupied) N_{S-D} with V_G bias. For N_{S-D} = 2 × 10^{13} cm^{-2}, trapped N_{S-D} remains fixed at the defined value and shows no evolution with higher $|V_G|$.

Figure 2.9 presents the color map for the simulated electric field and surface leakage distribution close to the gate-drain (GD) edge.

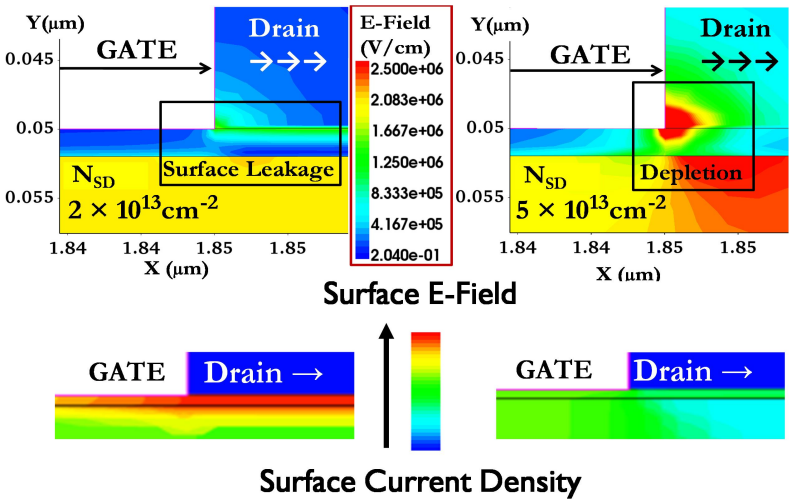

Figure 2.9: Surface field and density distributions in the structure near the gate-drain edge for 2 × 10^{13} cm^{-2} and 5 × 10^{13} cm^{-2} (lines) respectively.

From Figure 2.9 we notice that despite the peak of E_{Surf} at the GD edge, significant surface leakage exists along the gate-drain passivation interfaces for $N_{S\text{-}D}$= 2×10^{13} cm^{-2}.

For a defined N_{SD} > 3×10^{13} cm^{-2}, I_{Rev} growth is more gradual. They finally saturate beyond the threshold voltage V_{th} > −4 V. For N_{SD} = 5×10^{13} cm^{-2} in Figure 2.9, we observe that the E_{Surf} peak is much stronger at the GD edge and the surface current is substantially lower in passivated regions.

To understand this clearly, Figure 2.10 provides the evolution of E_{Surf} as well as total electron density along the device length, 1 nm below the GaN cap for both N_{SD} cases.

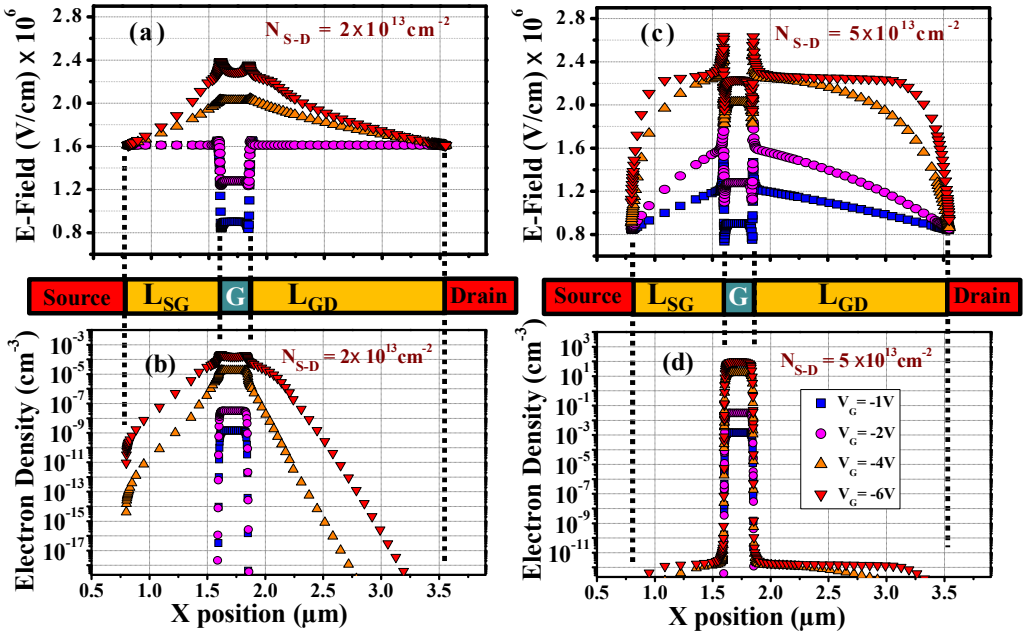

Figure 2.10: Abs(E_{Surf}) and E-density for a X-cut position 1 nm under the GaN cap/AlGaN barrier interface for N_{SD}= (a), (b) 2 × 10^{13} cm^{-2} and (c), (d) 5 × 10^{13} cm^{-2} (lines) respectively.

For N_{SD} = 2×10^{13} cm^{-2}, an insufficient E_{Surf} at gate edges (Figure 2.10(a)) allows electrons to leak and spread into the passivated gate-source and gate-drain regions (Figure 2.10 (b)). This promotes surface leakage, which further aggravated by higher $|V_G|$, induces a higher I_{Rev}. Thus, the presence of a minimum threshold in N_{S-D} can be identified which defines an adequate E_{Surf} at the gate edge. Here, the threshold is found at 3×10^{13} cm^{-2} for which normal I_{Rev} and I_D-V_D characteristics are obtained. An N_{S-D} of 3 × 10^{13} cm^{-2} was also chosen in [2.37] for modeling a GaN capped HEMT.

The corresponding E_{Surf} for N_{SD} = 5×10^{13} cm^{-2} is stronger and creates depletion regions at the gate edges (Figure 2.10 (c)), restricting electrons to only under the gate (Figure 2.10 (d)), and effectively suppressing surface leakage along the passivation. Any gate leakage is now confined to immediately under the gate and much better controlled.

In this condition, the I_{Rev} slope corresponds to electrons that steadily compensate or de-trap the initial trapped N_{S-D} due to the stronger E_{Surf} (Figure 2.10 (c)) along L_{GS} and L_{GD} accompanying a higher $|V_G|$ (Figure 2.8 (left)), until $|V_G| = V_{th}$ when N_{S-D} reaches its minimum and the 2-DEG is completely depleted. However, this threshold effect in almost unobservable in the forward gate characteristic as displayed in Figure 2.11. A trivial increase in I_{Forw} can be noticed when N_{S-D} is changed from 10^{13} cm^{-2} to > 3 ×10^{13} cm^{-2} and the increase beyond that is imperceptible.

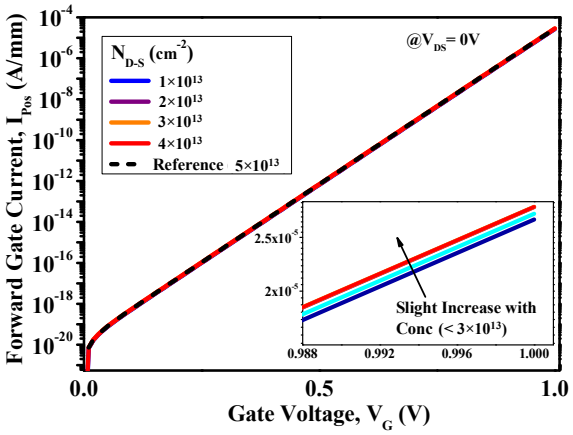

Figure 2.11: Forward I_G-V_G characteristics for variation in surface donor concentration (N_{S-D})

For I_{Forw} too, N_{S-D} values higher than 3 ×10^{13} cm^{-2} only marginally raise the final I_{Rev}. Hence, the choice of N_{S-D} is minimally relevant as long as it is defined higher than the threshold for the modelled device. We choose to set a reference N_{SD} = 5×10^{13} cm^{-2} for the following investigations.

Energy Position of Surface Donors (E_{S-D})

Energy positions above the Fermi level and closer to the conduction band energy E_C have a higher probability (≥50%) of being occupied by a hole. Hence, at a defined N_{S-D}, S-D charges have a greater chance of being occupied for E_{S-D} values defined closer to the conduction band. B. Jogai in

[2.40] indicated an E_{SD} of 1.5 eV, pinning the surface Fermi level E_F close to the mid-band. However, Gladysiewicz et al. [2.41] reported that the E_F is pinned at 0.55 eV below the CB for GaN/AlGaN/GaN structures, based on theoretical and experimental findings. Other works [2.34, 2.37 and 2.42] also support and validate $E_{S\text{-}D} \approx 0.5$ eV in their studies. For our study into impact of $E_{S\text{-}D}$ on the gate curves, Figure 2.12 (a) and (b) displays the I_{Rev} and I_{Forw} characteristics for an $E_{S\text{-}D}$ range of 0.6 eV–0.9 eV from E_C, compared to an $E_{S\text{-}D} = 1.3$ E_V from E_C, close to the mid band-gap.

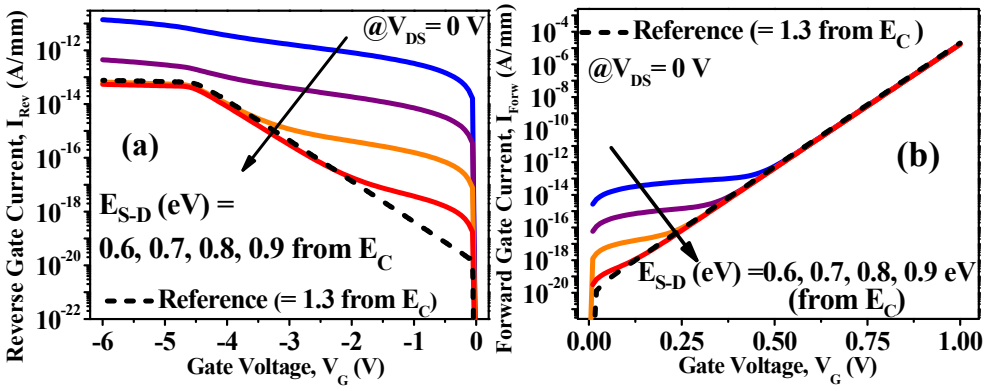

Figure 2.12: (a) I_{Rev} and (b) I_{Forw} curves for varying $E_{S\text{-}D}$ and $N_{S\text{-}D}= 5\times10^{13}$ cm^{-2}

An initial rise followed by a gentle saturation in both I_{Rev} and I_{Forw} is observed at low $|V_G|$, for $E_{S\text{-}D}$ values lower than an observed threshold $E_{S\text{-}D} \approx 0.9$ eV. The effect gets stronger for $E_{S\text{-}D}$ defined closer to E_C. For an $E_{S\text{-}D} < 0.8$ eV, overall I_{Rev} is higher for $|V_G| > V_{th}$ conditions.

Figure 2.13 (a) and (b) presents the distribution of the absolute values of E_{Surf} and current density J_{Surf} along the device length, obtained just under the GaN cap for $V_G=-1$ V.

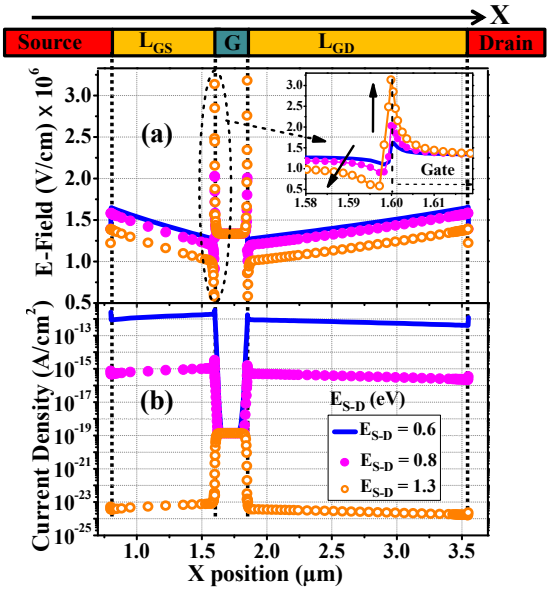

Figure 2.13: (a) Abs (E_{Surf}) and (b) Abs (J_{Surf}) at $V_G=-1$ V along the device 1 nm below the GaN cap/AlGaN barrier interface for varying surface donor energy from E_C.

For an $E_{S\text{-}D}$ =1.3 eV from E_C, simulations reveal a high E_{Surf} at the both gate edges and a low E_{Surf} along the passivation lengths, which produces the general I_{Rev} curve as previously discussed.

In contrast, for $E_{S\text{-}D}$ = 0.6 eV, E_{Surf} at the gate edges are lowest, allowing electrons to flow into passivated regions. This, combined with the higher E_{Surf} along L_{GS} and L_{GD}, spikes the current flow illustrated by J_{Surf}, and I_{Rev} is also increased. At low $|V_G|$, surface donors de-trapped by the incoming electrons can get re-trapped owing to their proximity to the E_C, triggering an even higher I_{Rev} in response. Once the gate is reverse-biased enough, E_{Surf} at the gate edges is high enough to block electrons from leaking into the surrounding regions. This is when I_{Rev} softly saturates and then merges into the general curve. For the following reliability section, a reference $E_{S\text{-}D}$ =1.3 eV has been chosen since it doesn't modify the leakage characteristics considerably and hence helps to isolate other degradation effects from behavior induced due to $E_{S\text{-}D}$.

B. REAL DEVICE PARAMETERS: RELIABILITY ISSUES

A real device is vulnerable to several electrical degradations that cannot be modelled by adopting ideal device considerations. To obtain an accurate representation, it's necessary to also account for major reliability issues that are unavoidable in even mature GaN technologies. Two major phenomena, unavoidable in a real device, are tunneling through the Schottky contact and spatially distributed trap defects within the structure. Gate leakage simulations can clearly reflect these parasitic effects. We can also draw inferences about their relative potential towards disrupting device performances through precisely modeling their modulations of the I_G-V_G characteristic.

Schottky Gate Tunneling

The phenomenon of tunneling is inherently a non-local process. This is because tunneling current (I_{Tun}) is inherently dependent on the E_C edge profile along the entire tunneling path connecting any two points. Hence, specific models for tunneling such as Fowler-Nordheim (F-N) tunneling are not completely representative of the entire tunneling process. "Non-Local Tunneling" is the most powerful model to capture the tunneling nature proposed by Sentaurus and recommended for modeling tunneling through Schottky contacts and through hetero-structure interfaces [2.1].

It accurately computes the complex band edge profile from the Poisson and transport equations completely, for each node along the tunneling path, instead of assuming a generic barrier shape. As such, this model is inclusive of specific tunneling cases such as F-N or direct tunneling. The physics of N-L tunneling is based on the concepts described in [2.43] with several

augmentations as presented in [2.1]. The probabilities for tunneling to the conduction band or valence band at contacts are calculated from WKB Wentzel–Kramers–Brillouin approximation [2.1].

To use Non-Local tunneling, a customized non-local mesh needs to be constructed overlapping the background original mesh, which establishes the tunneling regime. This is essential to limit simulation time, since tunneling computations severely complicate the solution of linear systems. It needs to be restricted only to areas of interest, close to the contact or interface where tunneling is to be modelled. The primary parameter for building a non-local mesh is the tunneling length L_{Tun}. For an L_{Tun} defined in association to the gate contact, all semiconductor vertices (nodes of the N-L mesh) within a radius of L_{Tun} are connected to the gate. These connections are the focal points of non-local lines which essentially represent the tunneling paths for carriers.

In Figure 2.14 (left), a schematic band diagram of the HEMT illustrates the N-L tunneling mechanism under variations of L_{Tun} and bias. For a low $L_{Tun}= L_1$, the tunneling is restricted only to the GaN cap. A higher $L_{Tun}= L_2$ however allows the electrons to tunnel deeper, reaching into the AlGaN barrier. A higher $|V_G|$ supports leakage by shifting the E_C higher which weakens the width of the tunneling barrier, thus potentially increasing I_{Rev} substantially. In Figure 2.14 (right) displaying the device current density, we can see how a higher L_{Tun} can strengthen the current leakage considerably around the gate for reverse biased conditions.

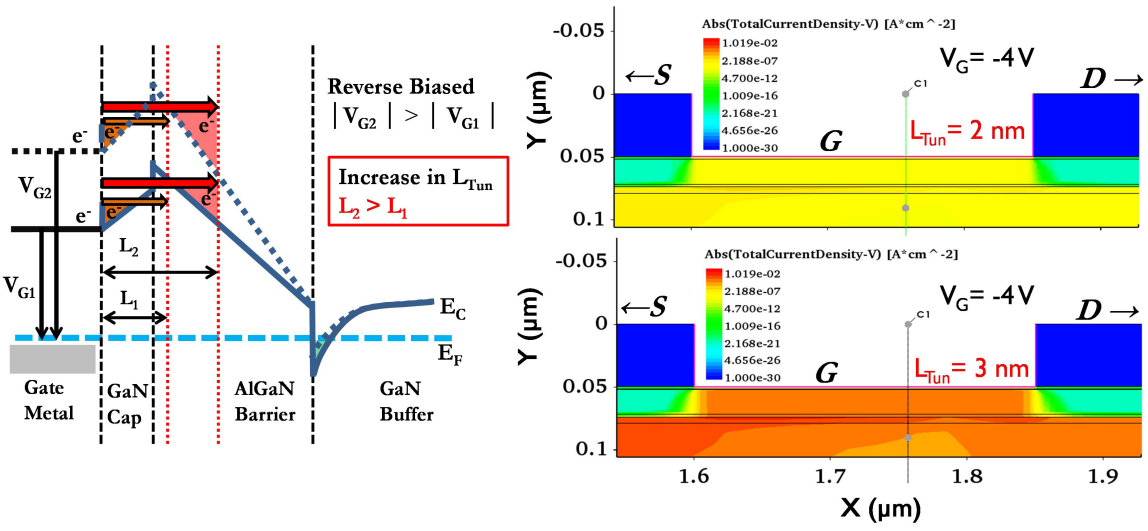

Figure 2.14: (left) Band-diagram schematic for reverse V_{GS} to illustrate the N-L tunneling model and (right) total current density comparison for L_{Tun}= 2nm and 3 nm at V_D= 0 V.

The non-local mesh can be visualized through the vector quantity Non-Local Direction as presented in Figure 2.15 (left) for L_{Tun} = 10nm. For a non-local line, this vector field constitutes vectors pointing from each vertex of the background device mesh towards the end of the non-local line following the direction of the contact in X and Y directions for which tunneling is defined.

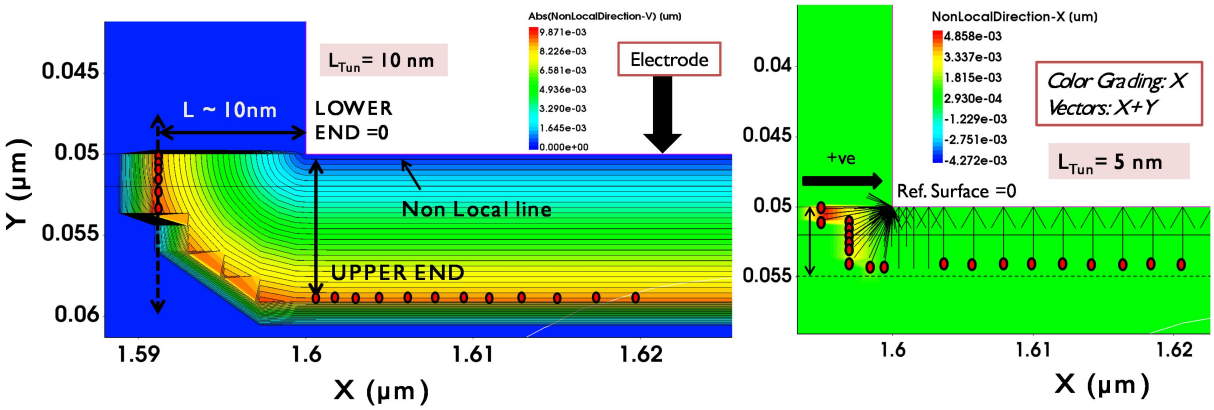

Figure 2.15 : Quantities to visualize non-local tunneling (Left) Abs (NonLocalDirection) for L_{Tun}= 10 nm. (Right) NonLocalDirection-X color map and NonLocalDirection (X+Y) vectors for L_{Tun} = 5nm

Thus, the original meshing of the structure needs to be tight enough in the tunneling region for the development of a well-formed non-local mesh and thus, accurate representation of the tunneling currents. The color map for the NonLocalDirection quantity describes the length of the vectors as can be understood from Figure 2.15 (right) obtained for L_{Tun}= 5nm. It illustrates the non-local vectors in both X and Y directions but the color map for only X vectors. Shorter vectors from vertices closer to the contact are superimposed on the longer vectors but can be visualized through their corresponding colors which fall lower in the scale. Red corresponds to vectors for vertices positioned ~ 9.87 (left) and ~4.86 nm (right) away from the contact. This is the highest length for which vertices in the original mesh fall within the defined L_{Tun}= 10nm and L_{Tun} = 5 nm constraints.

To visualize the non-local tunneling process, Figure 2.16 (left) presents the simulated eBarrierTunneling quantity along the device for Y cross section close to the gate-drain edge. This describes the rate at which electrons or holes are generated or recombined during the tunneling process averaged over the semiconductor volume.

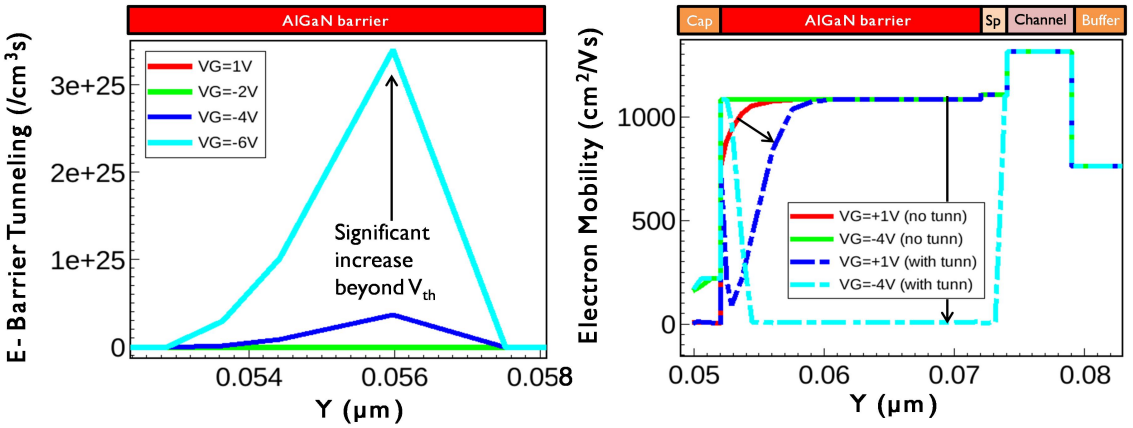

Figure 2.16: (left) E barrier tunneling, and (right) electron mobility distribution compared with and without tunneling, for an X position close to the gate on the drain side at V_D= 0V

Although the value itself is dependent on mesh spacing, the relative strength can be easily inferred to be much higher once V_G is reverse biased beyond threshold voltage, where tunneling currents are at maximum. The high tunneling current and leakage of electrons is accompanied with the fall in mobility observed at high reverse voltages. Figure 2.16 (right) compares the mobility distribution with and without tunneling effects along the device cross-section.

Generally, at V_G= +1V, the mobility remains high except in the highly doped GaN cap, with the highest value obtained in the 2-DEG channel. A slight drop is observed in the beginning of AlGaN due to the carrier flow under forward bias. When tunneling is activated, the drop in surface mobility can be easily seen and the loss is recovered only after a significant distance into the barrier layer, which would depend on L_{Tun}. This loss corresponds to the greater active carriers in the region.

For the reverse bias with no-tunneling condition, due to absence of carriers, mobility is high in the AlGaN barrier. However, with tunneling, higher $|V_G|$ equals much stronger barrier tunneling and hence the mobility sharply drops, slightly away from the surface. Then, it remains low throughout the AlGaN barrier until the curves meet at the peak of the 2-DEG well. Immediately adjacent to the surface, the negative V_G would have a slight repelling effect to carriers.

The effect of tunneling is hardly observable on output device characteristics for open channel conditions at V_D> 0 V. However, as presented in Figure 2.17 for V_G= -3 V to -2 V, the I_G-V_D characteristics reflect the presence of tunneling, which manifests as several orders of higher gate leakage though the inherent characteristic remains similar. The tunneling curves are observed to have a slightly higher slope close to 0< V_D< 3 V conditions.

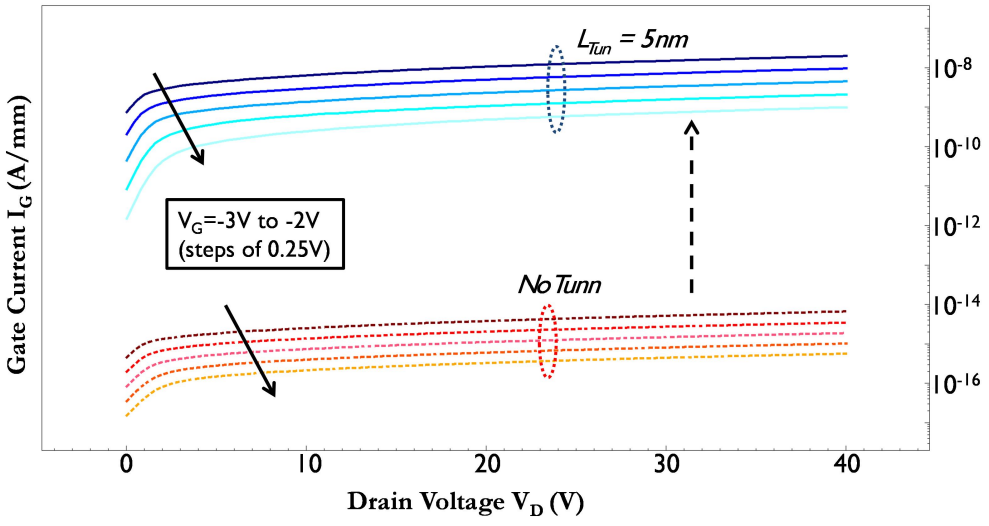

Figure 2.17: Comparison of I_G-V_D characteristics for V_G= -3 V to -2 V with and without tunneling.

Effect on Gate Characteristics

The I_{Rev} characteristics for L_{Tun} ranging from 1 nm–10 nm are presented in Figure 2.18 (a). The reference curve (L_{Tun}=0) is primarily governed by the thermionic emission model.

For L_{Tun} = 1 nm or 2 nm, tunneling occurs within the highly doped cap, hence only a slight I_G rise is observed compared to the reference. For L_{Tun}=2.1 or 2.5 nm, the stronger vertical electron E-field component causes a higher I_{Rev}. V_{th} is however still preserved around -4V.

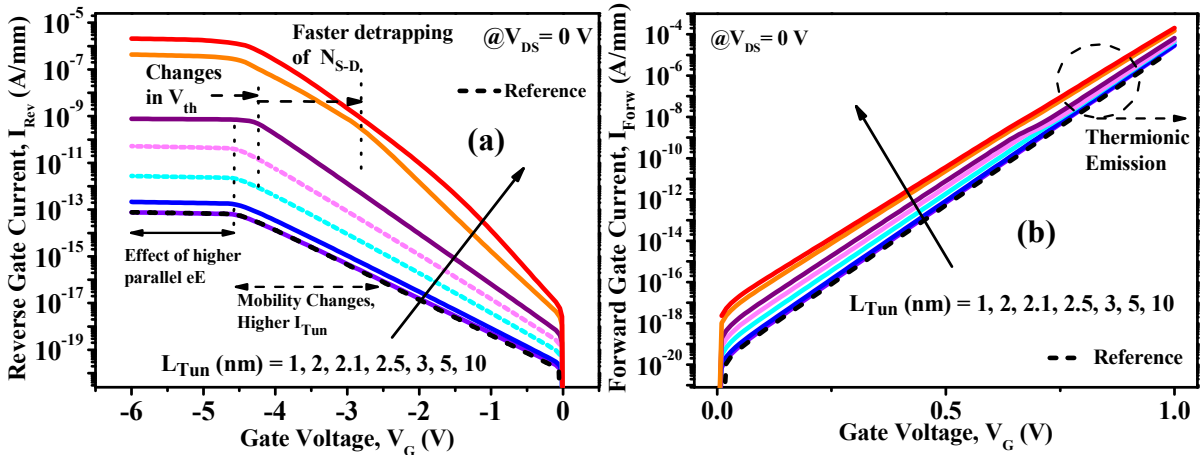

Figure 2.18: (a) I_{Rev} and (b) I_{Forw} for variation in L_{Tun}

Higher L_{Tun} curves however, begin displaying earlier saturation (lower V_{th}) due to faster de-trapping of the surface donors while the stronger leakage flow now reaches deeper into the barrier layer. This also results in reduction of mobility in the GaN channel. For L_{Tun} higher than 5 nm, the tunneling field is strong enough to promote a rise in I_{Rev} even for $V_G \geq V_{th}$ conditions. However, the relative I_{Rev} rise for higher L_{Tun} values reduces beyond L_{Tun} > 5 nm, since the additional tunneling area that is activated lies too far from the gate to make a notable impact.

Figure 2.18 (b) demonstrates that a higher L_{Tun} also increases I_{Forw} for lower $|V_G|$ conditions, though the relative change is less pronounced than for I_{Rev} as expected. At higher V_G, tunneling becomes less significant [2.44], and even curves with high L_{Tun} start merging into the reference, corresponding to just thermionic emission. Choosing an L_{Tun} for a technology depends on the Schottky robustness and any corresponding surface degradations in the modelled device.

Trapping Effects

In Sentaurus, traps can be introduced with various specifications [2.1]. The first is the location of the trap which can be defined in bulk regions or materials as well as material or region interfaces. Acceptor or donor traps defined in Sentaurus are uncharged when they are unoccupied

and negatively or positively charged when they are occupied respectively. They can be defined to have a single energy level, uniform, exponential, Gaussian or user-defined distributions.

The energy of the center of trap distribution can be written as E^0_{Trap} and derived from a chosen E_0 and a reference point within the bandgap as expressed below:

$$E^0_{Trap} = E_C - E_0 - E_{shift} \quad from\ Conduction\ Band \tag{2.25}$$

$$E^0_{Trap} = [E_C + E_V + kt\ ln(N_V/N_C)]/2 + E_0 + E_{shift} \quad from\ Mid\ Band\ Gap \tag{2.26}$$

$$E^0_{Trap} = E_V + E_0 + E_{shift} \quad from\ Valence\ Band \tag{2.27}$$

E_{Shift} is a physical model interface parameter dependent on electric field or temperature which can be defined or computed from energy shift models within Sentaurus [2.1]. In our simulations and by default, it is zero.

Different kinds of trap combinations have been simulated to understand their general impact and verify the validity for comparison with experimental scenarios. Acceptor traps substantially affect leakage and device performance as illustrated in Figure 2.19 for barrier traps under forward and reverse gate biases at V_D= 0 V.

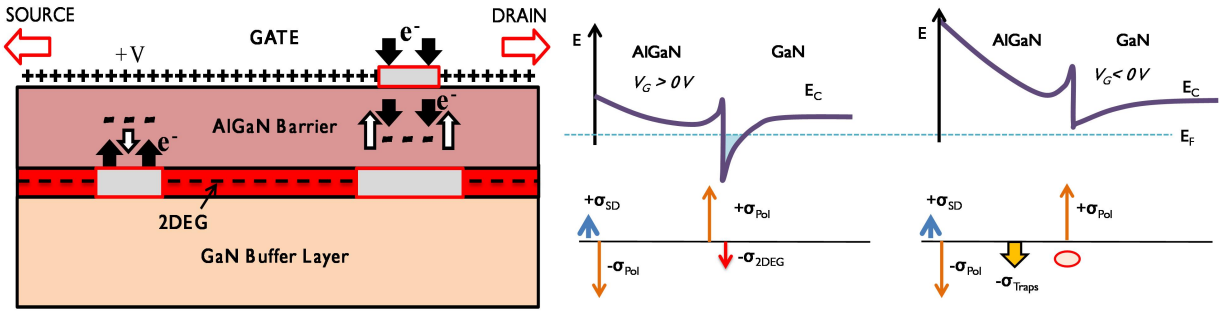

Figure 2.19: Schematic illustration of AlGaN barrier acceptor trap effects under varying V_G

Traps need to capture an electron to hold a negative charge and thus, affect the charge equilibrium in the structure. When a positive V_G is applied in the absence of drain bias, electrons from the lower structure try to flow to the top surface attracted by the positive voltage. When the barrier traps encounter these electrons, they get occupied. Once trapped, the build-up of negative charge starts repelling the flow of electrons hence reducing forward leakage currents.

Next, we assume a reverse gate voltage. Electrons flow from the top interface through tunneling and driven by repulsion from the negative V_G near the surface, start flowing down. In the process, these electrons first neutralize some surface donors which directly deplete the 2DEG density. Then, they similarly encounter the barrier traps and get trapped. Yet again, these negative charges now start repelling the flow of electrons and current drops. Hence we see that acceptor traps act to reduce both forward and reverse leakage currents in the device. In addition, the presence of

these negative charges also compensate for some surface donor charge, hence further depleting the corresponding concentration of 2-DEG in the channel. Thus, reverse bias conditions suffer greater worsening in the presence of acceptor traps.

Donor traps have similar but contrary effects since they would support conduction through replenishing the surface donor concentration. The comparative effects of donor and acceptor traps in the AlGaN barrier are observable in the example presented in Figure 2.20 displaying the simulated E_C distribution for a model device (with V_{th}> 4 V) at V_D= 0 V for varying V_G conditions.

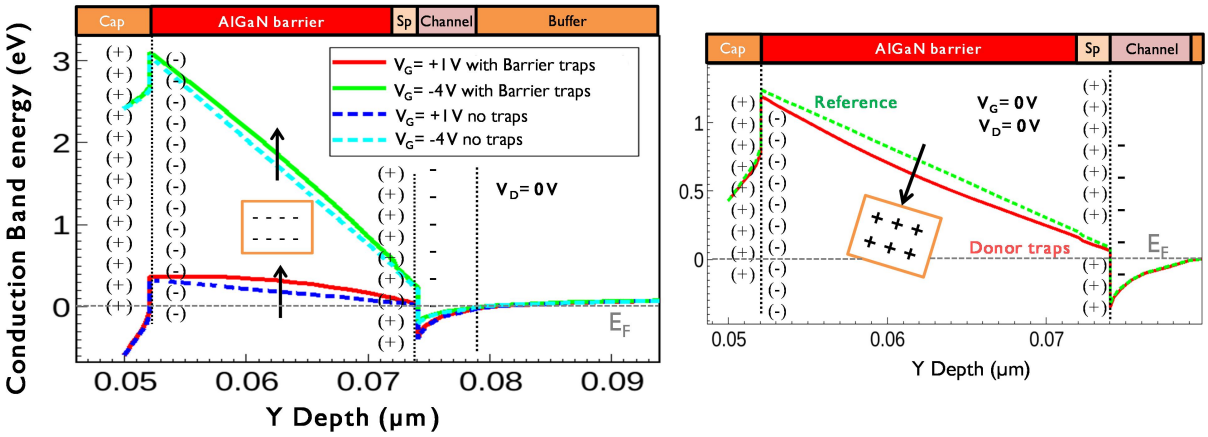

Figure 2.20: Conduction band energy distribution with V_{th} > 4 V for (left) acceptor traps in the barrier at V_G= +1 V and -4 V (right) barrier donor traps at V_G= 0 V and V_D= 0 V respectively.

The conduction band shape is controlled by the fixed polarization charge field, doping changes and free carrier densities. A higher $|V_G|$ bias shifts the peak higher. The falling slope of E_C going away from the cap/barrier interface represents the lowering of Schottky barrier height and thus higher charge flow towards the positive polarization charges. Acceptor trapped charges cause an upward bending of E_C in the barrier thus indicating a fall in current capability (Figure 2.20 (left)).

Donor traps in contrast, cause a downward shift in E_C shape within the barrier region indicating a lower barrier to current flow thus supporting conduction. However, even if defined with identical concentrations, their influence on the device characteristic is not equivalent to acceptor traps, since the occupational dynamics are different. The relative impact is thus dependent upon defined trap specification scenarios. In most cases, the presence of donor traps cannot act as compensation for the effect of electron traps, which are generally dominant.

For positive V_D, acceptor traps can substantially impact V_{th} as displayed in Figure 2.21 for V_D= 20 V. Negative trapped charge worsens E_C considerably at the notch near V_{th}. From Figure 2.21 (right) with I_D-V_G plots, we see that with acceptor traps in high quantities depleting channel density, it is easier to pinch off the channel since charge neutrality with the surface donors is achieved earlier.

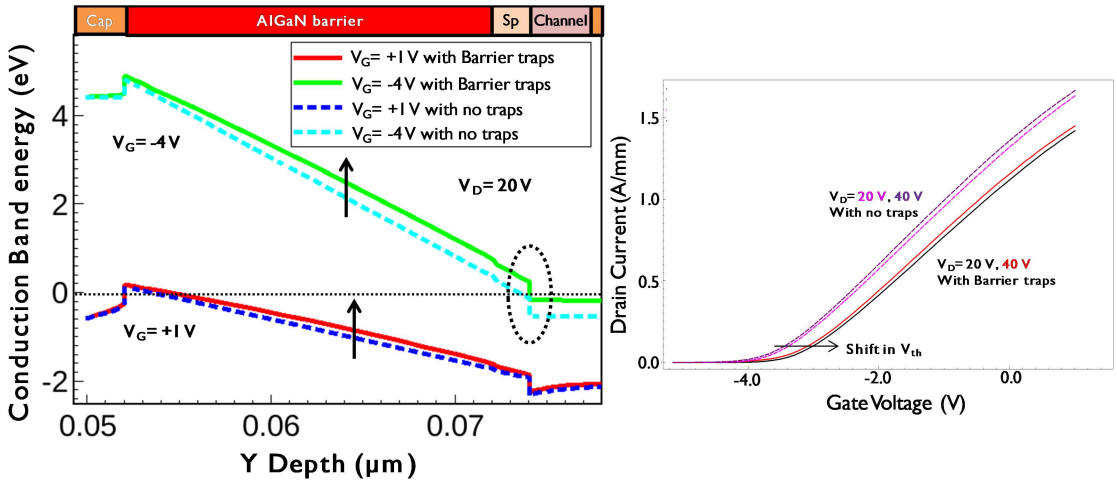

Figure 2.21: (left) Conduction band energy distribution at V_D= 20 V and I_D-V_G characteristics at V_D= 20V and 40V comparing the device response with and without barrier traps.

From Figure 2.21 (right) with I_D-V_G characteristics, we see that with acceptor traps in sufficient quantities depleting the channel density, it is easier to pinch off the channel since charge neutrality with the surface donors is achieved earlier. This is why V_{th} is less negative in the presence of acceptor traps. Donor traps, conversely induce slightly higher $|V_{th}|$ values.

Effect on Gate Characteristics

Though different traps impair the device reliability in distinct ways, their effect on output characteristics could often be similar as we shall see in detail later in Section C. Traps of different concentrations with different energy and spatial locations could cause equivalent I_D degradation or V_{th} shifts, making it difficult to distinguish the presence of specific traps within the device. I_G-V_G characteristics, however, are uniquely affected by each trap type which aids in identifying individual trapping phenomena, for simple V_D= 0V conditions. For our study, traps at relevant locations have been simulated assuming a level constant distribution, with the details as specified in Figure 2.22.

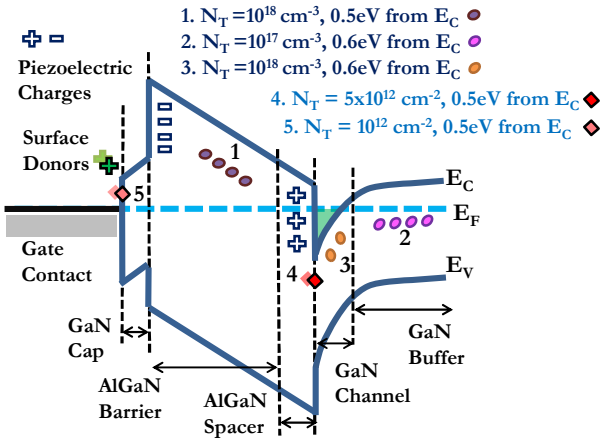

Figure 2.22: Schematic band diagram illustrating simulated trap details close to conduction band

Bulk acceptor traps in the AlGaN barrier, the GaN buffer and the GaN channel, and interface traps at the AlGaN/GaN hetero-interface and passivation/GaN cap interface are investigated. Numerous works have substantiated the presence of bulk traps in the AlGaN barrier [2.30, 2.38, and 2.45-2.46] and in the GaN buffer [2.26-2.27, 2.37-2.38, and 2.45]. Research also corroborates the importance of traps close to the AlGaN/GaN hetero-interface [2.30, 2.46-2.47] and at the top SiN passivation/cap surface [2.26, 2.30 and 2.38]. Chosen bulk trap concentrations usually range from ≈ 10^{16} cm^{-3} to 10^{18} cm^{-3} while interface trap concentrations of 3×10^{12} to 9×10^{12} cm^{-2} have been studied in [2.38]. The concentrations chosen for this work agree with literature while best reflecting the trapping influence on the leakage curve.

Traps defined close to E_C

For UMS devices, trap activation energies of 0.48 eV and 0.66 eV [2.48] have been identified by Drain Current Transient Spectroscopy (DCTS). Numerous works have reported similar trap energy of 0.5 eV [2.26-2.27, 2.30, 2.37, and 2.46-2.47] or 0.6 eV [2.38, 2.45] relative to E_C. Hence, all considered traps are located 0.5/0.6 eV from E_C. Each trap type has its own signature impact on the I_G-V_G when compared to the reference (no trap condition) as observed from Figure 2.23.

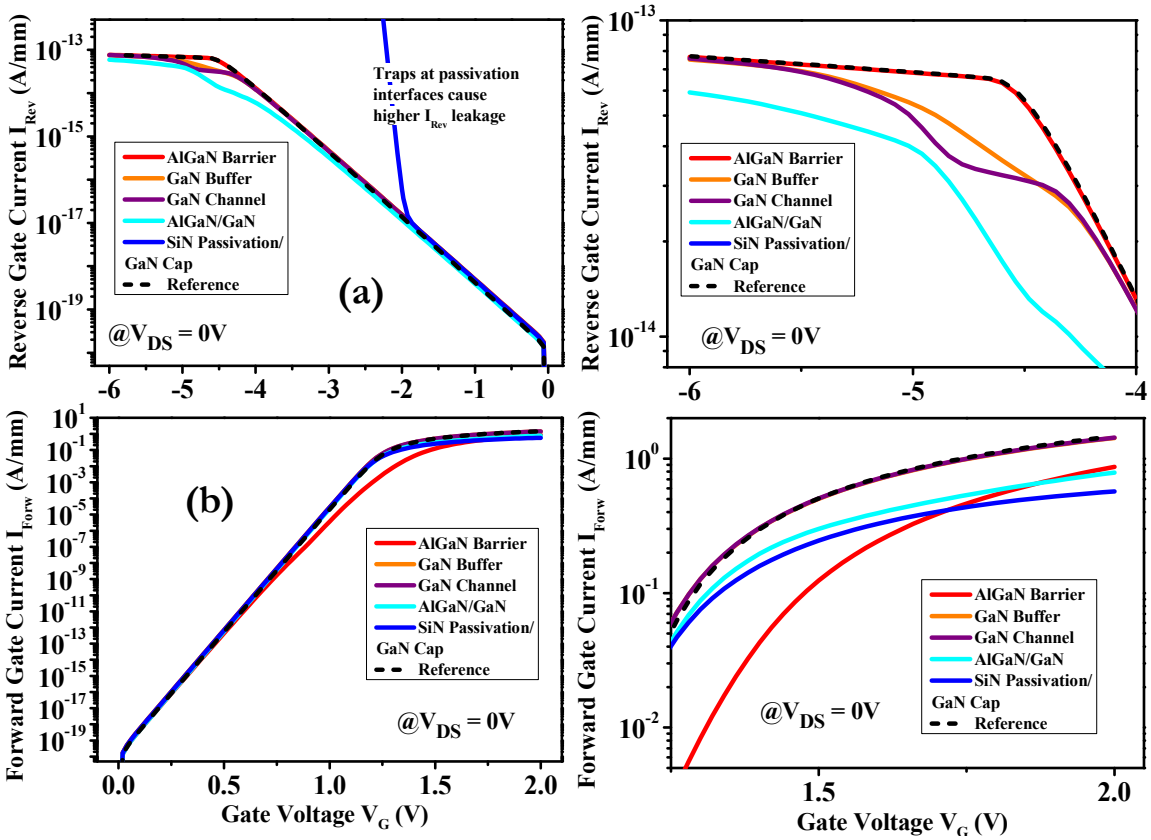

Figure 2.23: (a) I_{Rev} and (b) I_{Forw} characteristics for variation in traps defined close to E_C

Traps dominantly affect I_{Rev} (Figure 2.23 (a)) for $|V_G| \geq Vth$. This is probably because for low $|V_G| < V_{th}$, the rise in I_{Rev} due to de-trapping of N_{S-D} at the surface makes electron availability for trapping low in deeper structural positions. The impact on I_{Forw} (Figure 2.23 (b)) is important only at high $V_G \geq 1$ V conditions.

Barrier traps do not noticeably modify I_{Rev} characteristics but are found to significantly reduce the I_{Forw} slope for 0.8 V $\leq V_G \leq$ 1.7 V resulting in lower I_{Forw} levels than the reference. The effects on I_{Rev} would be noticeable however if energetically deeper traps were chosen. Buffer and channel traps can be observed to change the current slope near V_{th}, causing a slow I_{Rev} rise beyond V_{th} to finally reach the reference current level at $V_G = -6$ V (see Figure 2.23 (a)). Channel traps display a small saturation before a second rise while the growth in the buffer trap characteristic is more gradual. However, both traps have essentially negligible effects on I_{Forw}. Traps at the AlGaN/GaN interface also display a similar slight rise in I_{Rev} slope after V_{th}, but they start deviating from the reference much earlier, causing a noticeable reduction in overall I_{Rev} current levels and slope for $|V_G| \geq 2$ V. The corresponding change in I_{Forw} is minor in comparison, but observable as a minor decrease once V_G crosses 1 V. Traps at the passivation interfaces increase I_{Rev} due to surface leakage as previously discussed and decrease final I_{Forw} levels beyond $V_G \geq 1$ V.

Traps defined close to E_V

To gain further understanding into the impact potential of trap locations, each kind of trap is defined close to E_V as described in Figure 2.24 and their effects on the gate characteristic are compared in Figure 2.25. Traps close to E_V suffer very little modulation with bias conditions and thus have maximal and consistent occupancy since electron availability remains high as long as the trap energy remains below E_F. Such trap energies have been studied in [2.57-2.58, 2.62]. The corresponding characteristic represents the highest potential for damage in a given trap region.

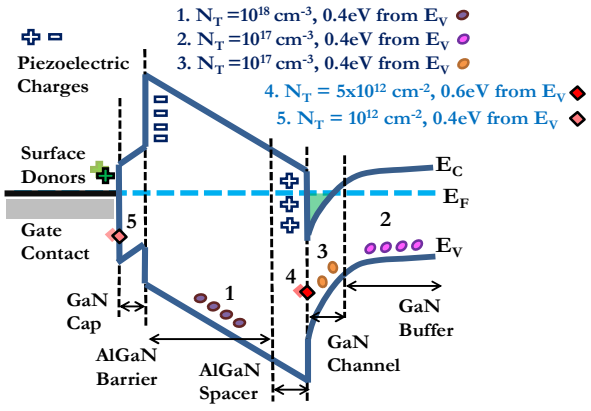

Figure 2.24: Schematic band diagram illustrating simulated trap details close to the valence band

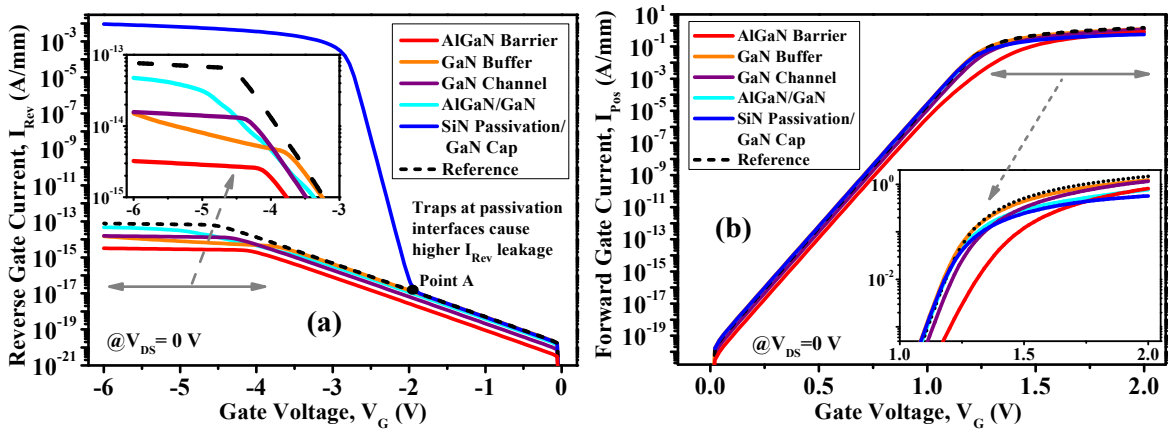

Figure 2.25: (a) I_{Rev} and (b) I_{Forw} comparison for variation in traps defined close to E_V

When defined energetically closer to E_V, most traps similarly affect I_{Rev} dominantly for $|V_G| \geq V_{th}$, but the absolute change relative to reference is markedly amplified. Barrier traps are observed to cause a constant decrease in I_{Rev} but induce no real change in its nature which is similar to trap definitions close to E_C although now, they cause a shift in V_{th}. Effect on I_{Forw} however remains identical. Channel traps are now mostly occupied and thus are powerful enough to cause a reduction in overall I_{Rev} as well as I_{Forw} accompanied by a shift of V_{th} to lower values, all indicative of a direct reduction in channel density. The small initial saturation that was observed close to V_{th} in Figure 2.23 (a) is sustained when the traps are close to E_V. Thus, I_{Rev} fails to recover to approach the reference levels. This is because, previously, reverse voltages beyond V_{th} could induce some de-trapping but they are not high enough to reduce the trap occupancy close to E_V.

The buffer trap I_{Rev} impact remains similar in that it doesn't deviate from the reference until pinch-off when the depletion region reaches the deeper buffer region. Similar to channel trap behavior, the gradual rise in I_{Rev} triggered by further rise in $|V_G|$ beyond V_{th} is insufficient to reach the reference level as I_{Rev} saturates at the lower current level. Continued increase in $|V_G|$ could potentially improve this discrepancy as buffer traps continue to slowly detrap.

AlGaN/GaN and surface trap effects are almost identical and relatively independent of E_A. This is probably since electrons are readily available for trapping adjacent to the 2-DEG and gate contact. I_{Forw} characteristics are also found independent of E_A within 0.4 to 0.6 eV from E_C except channel traps which, when occupied, impact charge balance directly by changing the 2-DEG density.

C. MODEL OPTIMIZATION

The above discussion recognizes the impact of critical parameters on the I_G-V_G characteristic. Based on careful assessment, a simulation methodology can proposed to achieve an optimal set of

simulation parameters for a given technology through recognition of the relative control of individual parameters on distinct regions of the leakage characteristic. We can customize the principal parameters, within their identified thresholds, to govern the low and high current regimes to build a representative I_G-V_G curve.

Measurement Set-Up

All DC characterizations on the packaged devices from UMS have been performed using a setup composed of the HP 4142 B Modular DC Source/Monitor (Figure 2.26 (a)) controlled by the Agilent IC-CAP software tool. A specific package fixture specially designed to hold the device as displayed in Figure (b) and (c), connects the gate and drain terminals to the instrument's medium power and high power source-monitor units respectively.

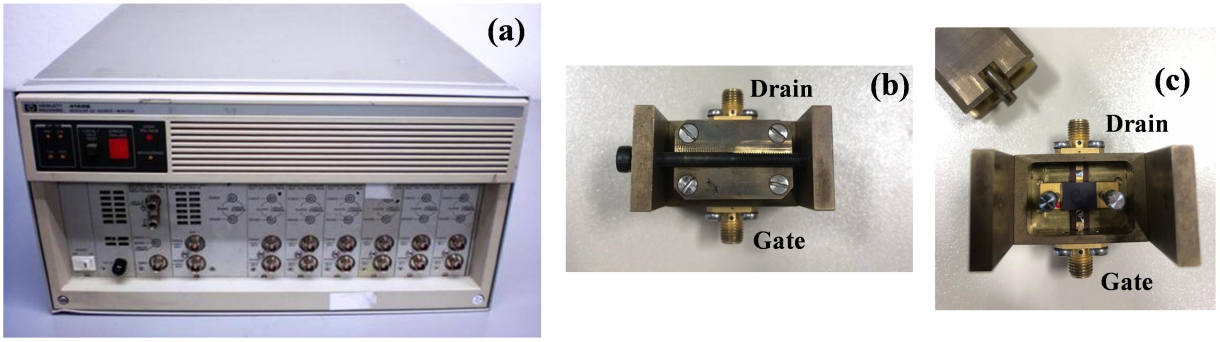

Figure 2.26: (a) HP 4142B source monitor and (b) closed and (c) open images of the device holder

Table 2.3 summarizes parameter effects on I_G levels in two regions for each curve: Region 1 (I_{Rev}: V_G = -2 V to 0 V; I_{Forw}: 0 V to 0.3 V) and Region 2 (I_{Rev}: V_G = -6 V to -3 V; I_{Forw}: 0.8 V to 1 V).

Table 2.3: Relative control of parameters on I_G-V_G curve

Impact	Φ_{ms}	L_{Tun}	N_{S-D}	E_{S-D}	Traps	R_G
Region 1, I_{Rev}	High	Medium	Low	High	Low	Trivial
Region 2, I_{Rev}	Medium	High	Low	Low	High	Trivial
Region 1, I_{Forw}	High	Low	Trivial	Medium	Low	Trivial
Region 2, I_{Forw}	High	Trivial	Trivial	Trivial	Low	Medium

The I_{Forw} characteristic is majorly controlled by TE [2.35] and hence is less susceptible to modification by parameters other than Φ_{ms}. An E_{S-D} closer to E_C and a higher L_{Tun} moderately increases I_{Forw} in Region 1, while R_G can moderately reduce the level and slope of I_{Forw} in Region 2. Traps can affect Region 2 in small amounts, but could be important in Region 1 too when present in high concentrations. In contrast, I_{Rev} can be well controlled by the discussed parameters.

For demonstration, I_{Rev} and I_{Forw} characteristics of an UMS GH-25 process are compared to their representative simulations in Figure 2.27 (a) and (b) respectively, based on the illustrated nature of control exercised by each parameter over the four distinct segments of the leakage characteristic.

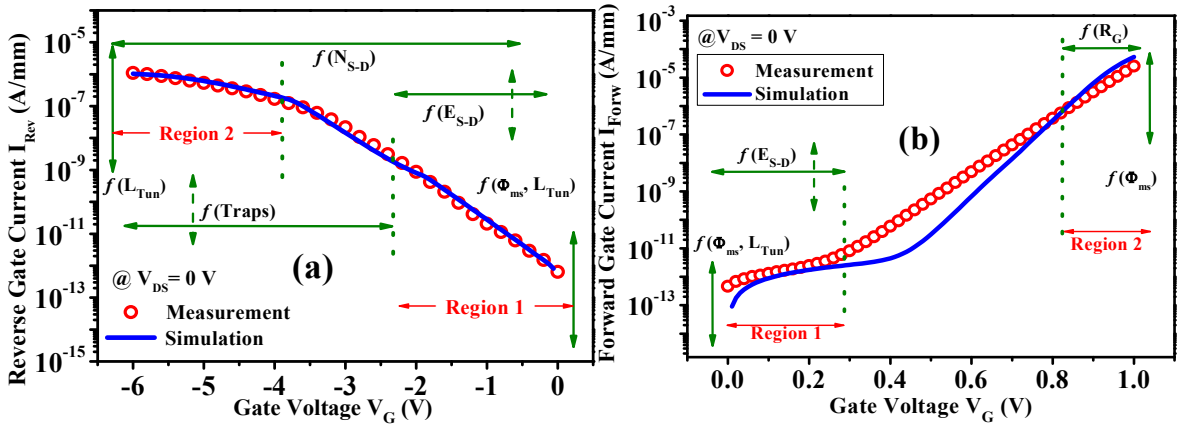

Figure 2.27: Model comparison of (a) I_{Rev} and (b) I_{Forw} with UMS GH-25 measurements

Φms and L_{Tun} define the initial value in Region 1. L_{Tun} however can also potentially alter the level and nature of I_{Rev} quite significantly in Region 2. While E_{S-D} is relevant in obtaining a weak initial slope in Region 1 (as for I_{Forw}), the effect of N_{S-D} though small, extends over the entire V_G range. Except in Region 1, traps can alter the I_{Rev} nature and final levels to a moderate extent.

Final I_G-V_G simulations show good agreement excepting a mismatch in I_{Forw} for medium V_G range. This issue has been discussed later in the section. Using $\eta = 1$ and $A^* = 23.2$ A/cm^2. K^2 [2.49] in Eq. 2.25 for Figure 2.27 (b), a $\Phi_{B,eff}$ of 0.88 eV and 1.06 eV is extracted from I_0 intercepts of 10^{-11} A/m and $10^{-14.2}$ A/m for the measured and simulated curves respectively. This disparity could potentially be due to barrier height modulations [2.35, 2.50] caused by transient trap effects, hopping mechanisms or trap assisted tunneling (TAT), effects that have not been considered.

The means of using the information summarized in Table 3 to build the parameter set corresponding to the simulation curves in Figure 2.27, to represent the device set of the UMS GH-25 technology, is a careful optimization process subject to several constraints. Φ_{ms} is chosen to approach I_{Forw} levels. The nature of the initial slope in measured I_{Forw} suggested an E_{S-D} value close to E_C and E_{SD}= 0.53 eV provided good agreement, similar to findings in [2.41]. Beyond these fundamental parameter choices, close representation of a technology relies on the realistic parameters describing tunneling and traps. While selecting these parameters, an integrated approach that simultaneously verifies the impact on simulated I_D-V_D is better suited. This also serves as a second validation of the parameter set validity under active operation. The results describing I_D-V_D control that contributed to parameter preferences are discussed in detail later in the section.

Continuing the discussion specific to the studied device set, simulated I_{Rev} levels were found lower in comparison to the reference for both Region 1 and Region 2, corresponding to an ideal device response. A higher L_{Tun} could account for a higher I_{Rev} in Region 2 but is not enough for the increase required in Region 1. This indicated the presence of not just appreciable tunneling, but also donor-like traps. Simulated I_D-V_D curves, however, were higher than measurement levels, thus reflecting the impact of acceptor traps. Since the measured I_{Rev} exhibits a small slope beyond V_{th}, buffer and AlGaN/GaN interface acceptor traps (as discussed for Figure 2.23 (a)) were considered which exhibit such a nature. Also, since L_{Tun} is irrelevant to I_D-V_D nature, while traps significantly control I_D levels, I_D-V_D considerations helped determine the relative impact of tunneling versus traps.

Optimization of L_{Tun} and AlGaN/GaN interface trap parameters completes the dedicated parameter set, as specified in Table 2.4. The corresponding I_D-V_D results are displayed in Figure 2.28.

Table 2.4: Relative control of parameters on I_G-V_G curve

SWF	L_{Tun}	N_{S-D}	E_{S-D}	Traps : Donors N_D , E_D	Traps : Acceptors N_A , E_A
4.24 eV	4.5 nm	6×10^{13} cm^{-2}	0.53eV from E_C	AlGaN barrier: 5×10^{18}cm^{-3}, 1.2eV from E_C	AlGaN/GaN: 10^{12} cm^{-2}, 0.1eV from E_C

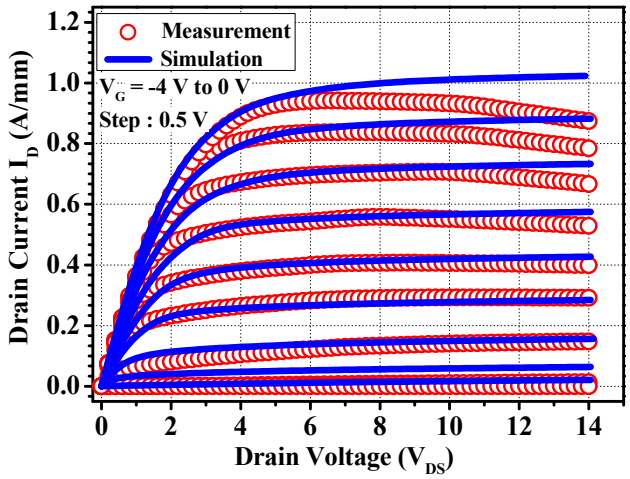

Figure 2.28: Model comparison to I_D-V_D for the ASAP process of the GH-25 technology

Understandably, I_D-V_D simulations slightly deviate for high V_G conditions, since self-heating induced I_D lowering is not taken into account by the adopted DD model. A hydrodynamic model while allowing simulation of self-heating effects would require sacrificing simulation speed and simplicity, which are important considerations when building the primary fit to measurements.

In contrast, this methodology based on modeling I_G-V_G behavior operates at V_{DS} = 0 V and low I_D values, where self-heating effects are insignificant and do not affect the accuracy of any inferences drawn under these conditions. Therefore, the good global accuracy validates the chosen parameter set.

I_D-V_D Considerations

Figure 2.29 compiles the effect of variation in concentration and energy positions of barrier, buffer, AlGaN/GaN and surface interface traps on output characteristics for V_G= 0 V and V_G= -2V. The reference is defined with N_{S-D}= 3× 10^{13} cm^{-2}, E_{S-D}= 0.55 eV, Φ_{ms}=4.25 eV and no traps.

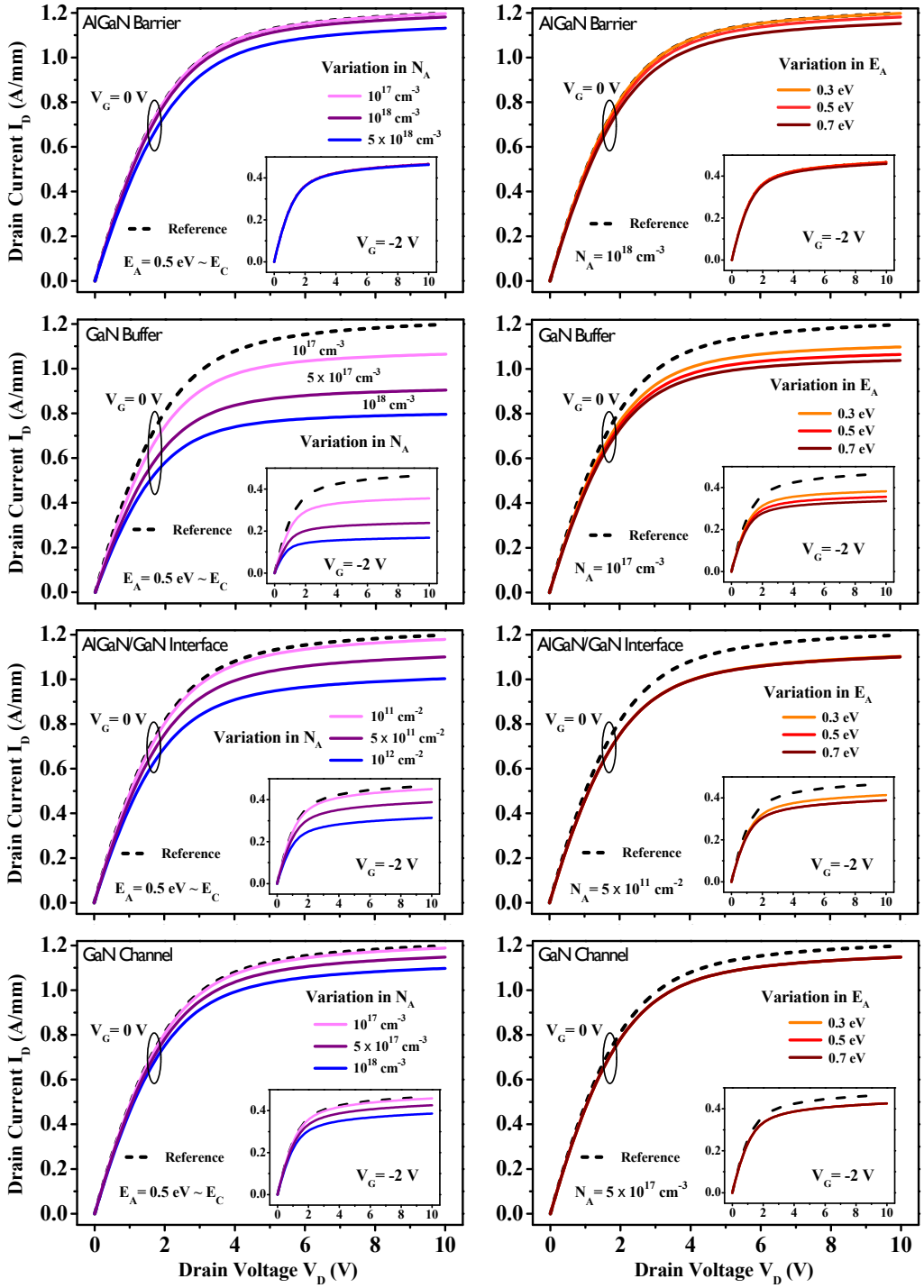

Figure 2.29: I_D-V_D characteristics for changes in concentration and energy position of AlGaN barrier, GaN buffer, AlGaN/GaN interface and GaN channel traps

For successful application of the methodology to extract specific parameter sets that directly facilitate reliability or performance comparisons across different technologies, it is important to understand the possible effects on I_D-V_D caused by parameters introducing non-idealities.

Tunneling parameters have negligible impact on I_D-V_D under open channel conditions. So the choice of tunneling parameters is entirely motivated by the gate characteristics. Traps however, in varied spatial or energetic locations, influence notable changes in I_D. Hence, these effects need to be simultaneously reviewed when deriving the best fit to model I_G-V_G and I_D-V_D characteristics.

All N_A variations are performed at a constant E_A= 0.5 eV while moderate concentrations are chosen to investigate E_A impacts. At V_G= 0V, AlGaN barrier traps have negligible effects on I_D unless present in high N_A values. Deeper traps for $E_A \geq 0.5$ eV causes small falls in I_D. The effects are trivial at V_G=-2V. For traps in the larger GaN buffer, N_A has a major impact in the potential worsening of I_D. Significant lowering in I_D is observed even for small N_A values. Energetically deeper buffer traps moderately degrade the I_D levels. The effects at V_G= -2V are equivalent.

AlGaN/GaN interface traps are important to I_D degradation at moderate to high N_A values. Shallow E_A values produce smaller changes around V_G=-2 V, but at V_G= 0 V, the worsening is significant, and essentially independent of E_A. This is in agreement with the results obtained in Figs. 2.22 and 2.24, since the presence of traps near the channel guarantees a high level of occupancy. Channel traps have similar effects to AlGaN/GaN traps, and are immune to E_A and V_G variations.

Here, from a summary observation of Figure 2.29, it is easy to see how multiple trap combinations might result in the same resultant I_D-V_D characteristic. This demonstrates the relevance of using an alternate characteristic such as gate leakage to separate trap contributions.

Consistency of Methodology

The UMS GH-25 technology has several process versions due to varied fabrication steps in the process flow yielding moderately different device characteristics. The previously discussed process is one of these technology versions.

Three other technology versions designated as P1, P2 and P3 and have been modelled using the gate control methodology supplemented with I_D-V_D information on trap effects to generate their representative parameter sets. AlGaN/GaN and AlGaN barrier traps have been considered, which well modulate the I_D-V_D levels and I_{Forw} slope respectively depending on chosen N_A.

The corresponding I_G-V_G and I_D-V_D results are presented in Figure 2.30 and Figure 2.31 respectively. The parameter sets have been assembled in Table 2.5. Comparison of parameter values from one process version to another helps to recognize relative vulnerabilities or advantages.

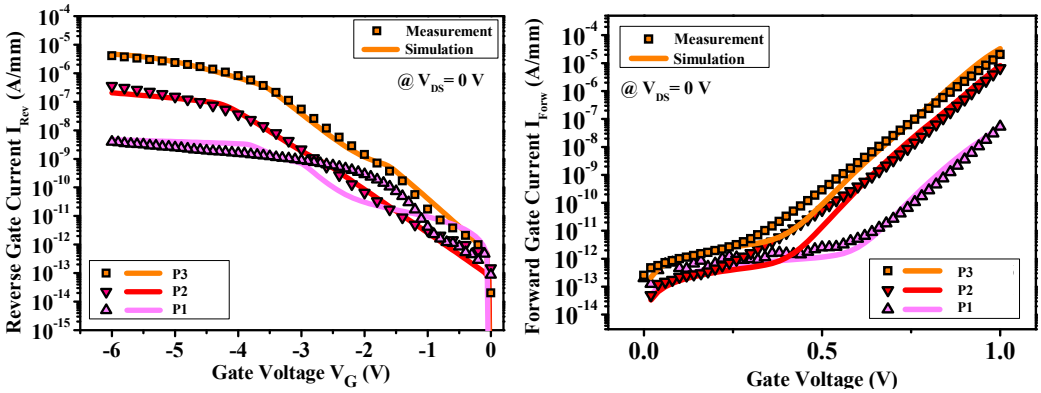

Figure 2.30: Model comparisons for the P1, P2 and P3 UMS GH-25 processes

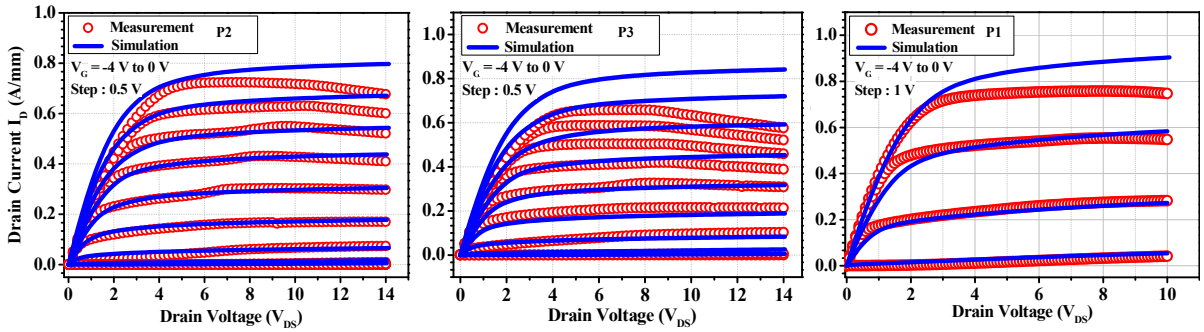

Figure 2.31: Measured and simulated I_D-V_D characteristics for the P1, P2 and P3 device processes.

Table 2.5: Parameter sets for the GH-25 process technologies

Tech.	SWF	L_{Tun}	N_{S-D}	E_{S-D}	Traps : Donors N_D , E_D	Traps : Acceptors N_A , E_A
P2	4.29 eV	3.8nm	5×10^{13} cm^{-2}	0.54 eV	AlGaN barrier: 1×10^{17} cm^{-3}, 0.8 eV from E_C	AlGaN/GaN: 2×10^{12} cm^{-2}, 0.3 eV from E_C AlGaN: 2×10^{18} cm^{-3}, 0.55 eV from E_C
P3	4.31 eV	6.5 nm	5×10^{13} cm^{-2}	0.52 eV	AlGaN barrier: 5×10^{17} cm^{-3}, 1.0 eV from E_C	AlGaN/GaN: 3×10^{12} cm^{-2}, 0.2 eV from E_C AlGaN: 5×10^{17} cm^{-3}, 0.4 eV from E_C
P1	4.41 eV	4 nm	4×10^{13} cm^{-2}	0.55 eV	-	AlGaN/GaN: 1×10^{11} cm^{-2}, 0.4 eV from E_C AlGaN: 1.8×10^{18} cm^{-3}, 0.65 eV from E_C

For example, if we compare the P3 and P2 devices, we see that P3 is more susceptible to tunneling since it has higher I_{Rev} in Region 2. E_{SD} is chosen based on Region 1 I_{Forw} saturation levels. Measurements for both devices had a larger I_{Forw} slope than initial simulations, indicating the presence of AlGaN barrier traps which bend the I_{Forw} curve close to E_A=0.4-0.5 eV from E_C (Figure 2.23 (b)). The high L_{Tun} for P2 moderately compensates this difference, and yields the final fit with minor Φ_{ms} and AlGaN/GaN trap adjustments. P3 however presents a lower L_{Tun} and thus, requires higher barrier acceptor traps to enable a better fit to the slope and I_D levels. Interestingly, both devices have similar levels of measured I_D-V_D at low V_G, which would make the above distinctions difficult to detect without the gate curves. Self-heating seems to be more important in the P3 process which leads to a mismatch with simulations at high V_G. For the measured P1 device, I_G-V_G levels are lower indicating a higher Φ_{ms}. a long saturation exists until V_G= 0.7 V before the rise in I_{Forw}. With a high Φ_{ms}, an E_{S-D} close to the E_C approaches the level in Region 1, but cannot extend it to higher V_G.

Deep AlGaN traps at high N_A cause I_{Forw} shifts similar to traps close to E_V in Figure 2.25(b). Hence, the addition of these traps was necessary to approach the measurement nature.

As observed, obtained parameter sets provide reasonably good fits except for the I_{Forw} slope around $0.3 < V_G < 0.5$ V, similar to the deviation obtained with the previous process as well. This region of the I_{Forw} has been reported to be susceptible to surface trap and TAT mechanisms [2.35, 2.51]. Drawing from this and other analyses, the TAT effect has been simulated in detail on the complete GH-25 structure for a different UMS process in Chapter 3, dedicated to the study of the forward leakage behavior. Based on the study, TAT has indeed been found to be capable of manipulating the slope in the region of discrepancy and hence is potentially the missing mechanism. Donor traps adjacent to the gate edges can also influence this I_{Forw} slope. However, in contrast to the GH-25 process studied in Chapter 3, there is no information on the currently studied process versions that could establish or validate a link to TAT or accompanying degradation phenomena. As such, it is impossible to conclude on the root of this mismatch.

Hence, in the interest of maintaining the simplicity and optimization efficiency of the methodology, we don't add TAT as a governing parameter. Nonetheless, incongruity in the I_{Forw} description is a potential drawback of a guiding methodology drawn on only six control parameters.

Concluding Remarks: Methodology Capability and Limitations

The detailed leakage current analysis advances the discussion on identifying possible contributions of degradation mechanisms plaguing the GaN HEMT. The D-D model is found sufficiently capable of illustrating the behavior and relative impact of all considered parameters including gate tunneling and traps. Thus, the model is found powerful enough to viably model reliability concerns of GaN HEMTs.

Since the investigated I_G-V_G characteristic, in contrast to I_D-V_D, is unique to each technology, precise physics based optimization of the dominant parameters for each region of the I_G-V_G curve using chronological steps of the defined methodology improves the validity of device simulation parameters. However, because of non-negligible dispersion within process devices, consideration of a simpler initial structure, and absence of deeper information into process conditions, the achieved parameter set while being unique and representative is not necessarily exclusive. More information that could conclusively restrict the tuning range of certain parameters such as Φ_{ms} further, could in turn change other not so easily verifiable parameters such as L_{Tun}, resulting in a slightly modified but still physically-meaningful set. Thus, even though parameter sets are built through careful and detailed optimization, they might not be the only possible combination.

The work does not claim to always yield the closest fit to measurements, which might require substantial device-specific data in addition to a high level of proficiency in navigating Sentaurus numeric solvers. The existence of an exclusive, perfect parameter set, even after relevant validation, might be difficult to prove, especially since GaN device concepts are based on hypotheses that are still evolving. Many other design, condition or application specific models and parameters might be needed to produce the final match for a particular technology, such as the TAT mechanism which needs incorporation for the GH-25 forward gate curves.

2.4 Comparison with Hydrodynamic Simulations

Preliminary investigations were carried out in hydrodynamic mode to explore its applicability to our case studies. Some changes to the general simulation technique enabled the hydrodynamic model. The driving force for electron mobility is changed to carrier temperature [2.1, 2.52]. The substrate is thinned to 10 μm to save simulation time. A single thermode is defined at the bottom substrate interface for heat dissipation which defines environmental temperature at 300 K.

Most importantly, the Piezoelectric Polarization model for interface charges was found unable to well-support hydrodynamic operation since the convergence issues could not be solved. It proved necessary to instead directly define the polarization through fixed interface charges. The output characteristic comparison between the DD and HD model is presented in Figure 2.32.

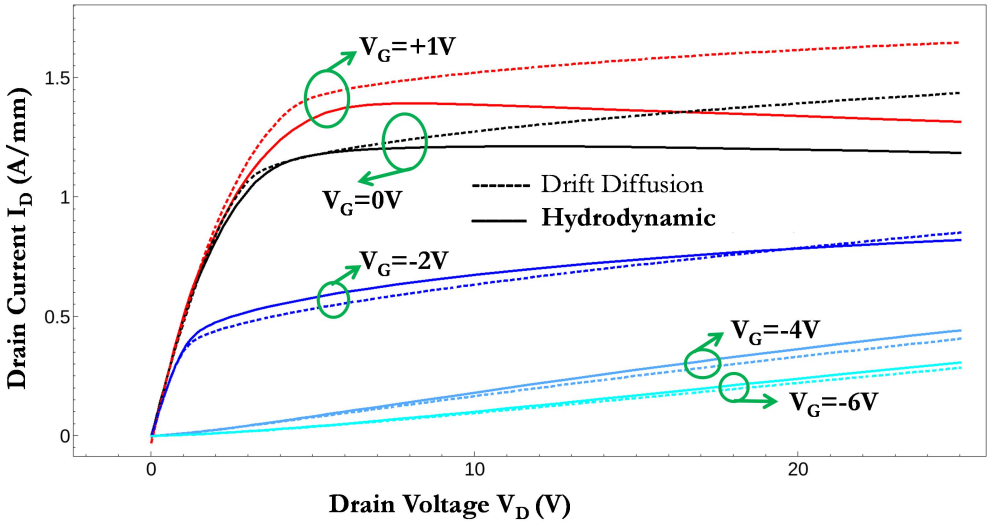

Figure 2.32: Initial comparison of drift-diffusion and hydrodynamic approaches

The charge at the AlGaN/GaN hetero-interface is defined equal to 9×10^{12} cm^{-2} [2.23, 2.53] which is lower than the theoretical value to account for relaxation effects, similar to approaches used in other works on GaN interface charge or hydrodynamic models [2.52-2.56].

An equivalent drift diffusion model with identical interface polarization charges was built to enable a clearer comparison. Significant deviation owing to self-heating [2.59-2.61] caused by an increase in the average lattice and electron temperatures is quite noticeable for high V_G, while the lower V_G curves are quite similar to the DD model. To study the origins further, we can visualize the lattice and electron temperature distributions within the structure at different operational conditions.

A. TEMPERATURE DISTRIBUTIONS

Lattice Temperature

Figure 2.33 presents the lattice temperature variations around the gate for V_{DS}= 10 V.

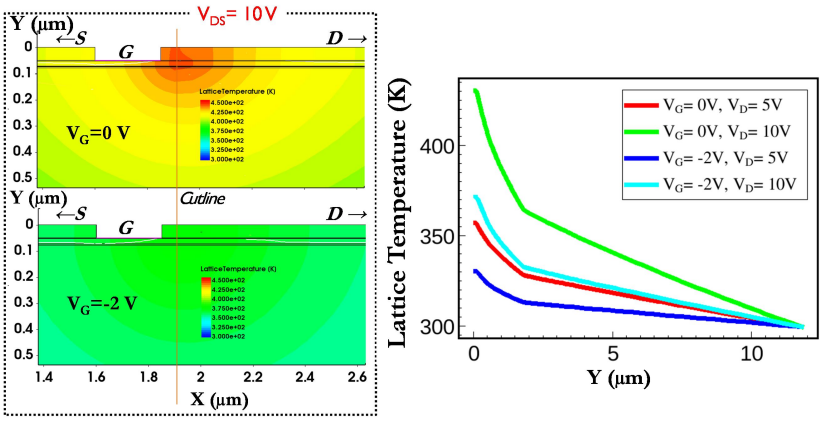

Figure 2.33: Lattice temperature distributions at V_D= 10 V for different V_G conditions for the cutline shown in (left).

At V_{DS}= 0V in the absence of current flow in the channel, the lattice temperature maintains close to 300 K with minor perturbations. When V_{DS}= 10 V, current flow is enabled and a high electric field appears at the gate-drain edge. This then becomes the center of heat concentration with the highest temperature extending from the surface to the channel [2.59, 2.62]. At V_{GS}= 0 V, it rises rapidly for higher V_{DS} values. Close to the threshold, current flow is limited and this leads to lower temperatures and a slower lattice temperature rise with V_D. The heat distribution is also observed to be more uniform, with a smaller difference between surface and bulk temperatures.

Electron Temperature

Carrier temperatures are strongly linked to electric fields which accelerate electrons and increase their kinetic energy. Electrons and phonons have very strong coupling in GaN HEMTs [2.63] hence higher electron energies lead to the formation of hot electrons and localized hot-spots under normal operating conditions in addition to rising lattice temperatures [2.29, 2.59, 2.62-2.65]. Figure 2.34 presents the color map for electron temperatures within the structure for V_{DS}= 0V, V_{GS}=

0V and V_{DS}= 10 V. Figure 2.35 depicts the corresponding values at the cutline in Figure 2.34 for some of the conditions.

In all cases, the observed hotspots seem to follow the electric field peaks [2.62, 2.64]. At V_{DS}= 0 V (Fig. Figure 2.35 (left)), high reverse biases develop a high electric field region around the gate. Maximal electron temperatures are observed as leakage from the gate approaches the high electron density channel (Figure 2.35 (left)). Leakage currents at V_G= +1 V also induce small rises in electron temperature, but the smaller electric field limits the peak values.

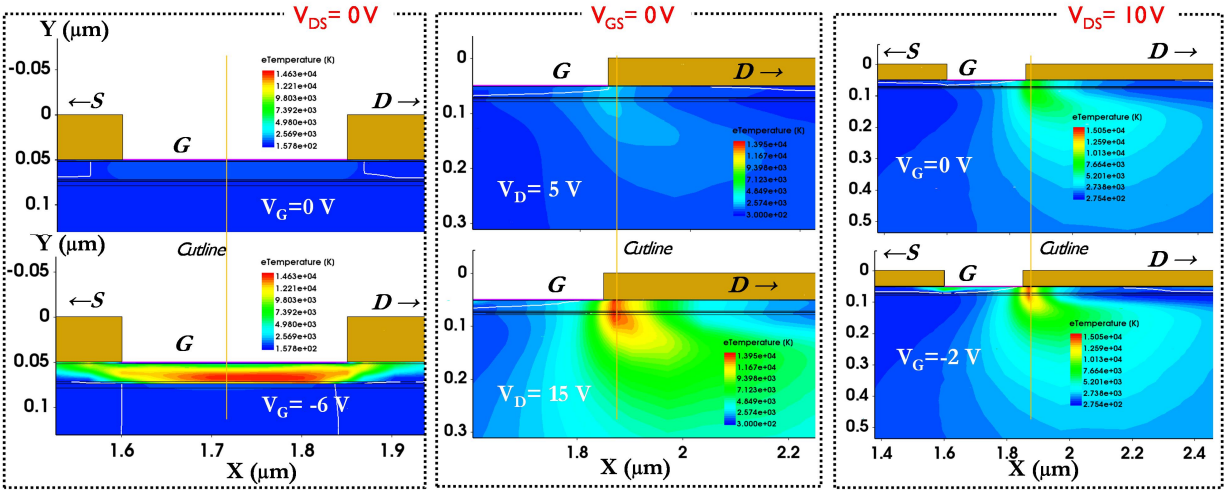

Figure 2.34: Electron temperature distribution at different V_G and V_D bias conditions

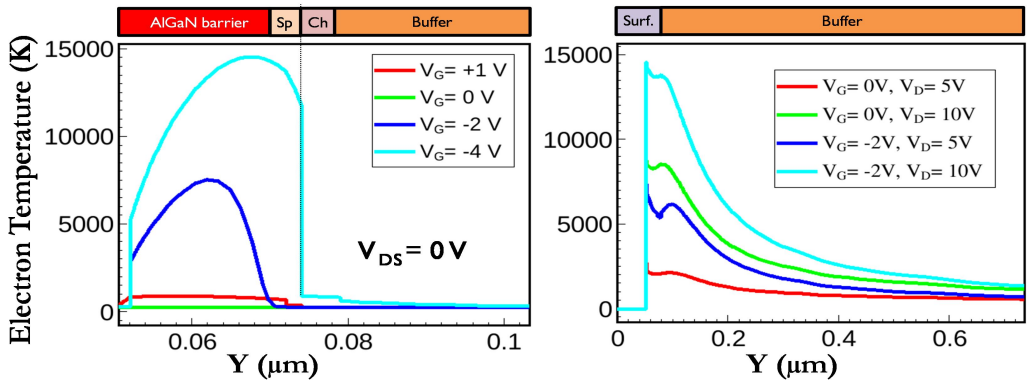

Figure 2.35: Electron temperatures for (left) varying V_G at V_{DS}= 0 V and (right) varying V_G and V_D.

Under on-state operation, at a constant V_G= 0 V, electron temperature rapidly rises with higher V_{DS} values and the hotspot localized near the gate-drain edge where the V_{DG} field is maximum. The region of high temperature extends from the surface to the channel [2.63, 2.66] and falls away slowly, deeper in the buffer. For V_G= -2 V, the associated electric field peak is correspondingly higher leading to higher temperatures. Hence, electron temperature peaks near the surface are greatest at high V_D and $|V_G|$ conditions as could be expected.

B. EFFECT OF TRAPS

To compare the effects of traps in drift-diffusion or hydrodynamic implementations, Figure 2.36 presents the I_D-V_D at V_G= +1 V with and without traps. It also illustrates the associated increase in electron and lattice temperatures with respect to V_D for the hydrodynamic case. Acceptor traps have been introduced in the AlGaN barrier (N_A= 5× 10^{16} cm^{-2}, E_A= 0.5 eV) and the GaN buffer (N_A= 10^{16} cm^{-2}, E_A= 0.4 eV).

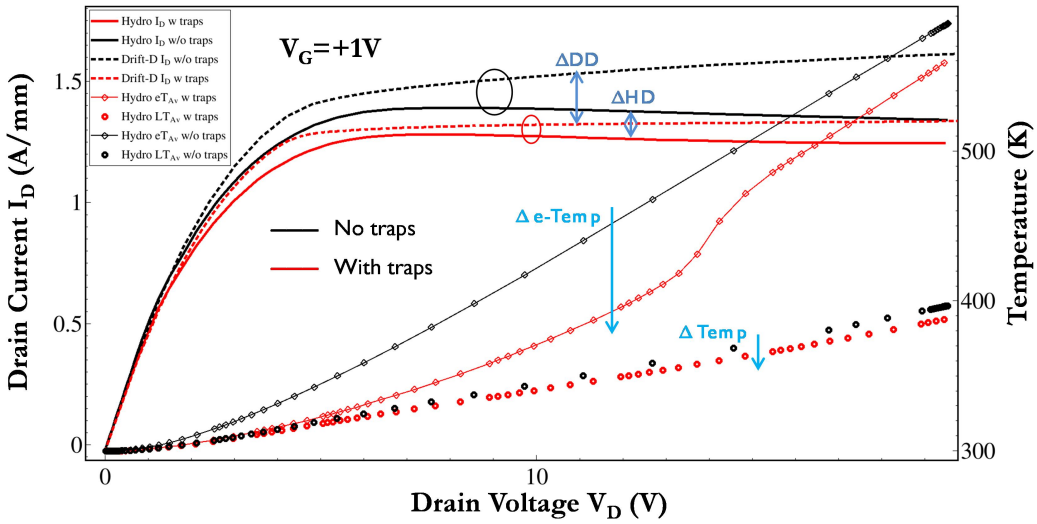

Figure 2.36: Effect of traps in drift-diffusion and hydrodynamic implementations

If the response with and without traps are compared, the variation is substantially higher in the DD case. Hence, the hydrodynamic model lessens the effect of traps on the device response, especially at high V_D where self-heating dominates. With activation of traps in the HD model, free electrons which could otherwise reach high energies get trapped. Hence the build-up of electron temperature and lattice temperature is also reduced. Thus, the temperature and trap mechanisms have a moderating influence on each other.

HD cases are observed to have a higher knee voltage, and hence a delayed saturation when compared to the DD curves. Self-heating is evident between both sets of HD and DD curves. However, the magnitude of I_D fall going from DD to HD is smaller in the presence of traps. This means that the contribution of self- heating to the worsening of device response at high V_D is relatively lower in the presence of traps.

Based on this discussion, it can be inferred that the investigation of traps is more sensitive with the DD model where self-heating would not impact the observations. In addition, traps also reduce the disparity between HD and DD representations. This suggests that the study of individual trap effects which is the motivation of this work could be well performed using the DD model.

Remarks on the hydrodynamic model

For the GaN HEMT with its material and design peculiarities, building a hydrodynamic model appreciably increases simulation time and complexity. It is often subject to convergence issues that are difficult to troubleshoot and require substantial effort into optimizing the mathematical parameters of Sentaurus solvers. Despite attempts with several interface charge combinations derived from literature, a good approximation of the leakage current behavior could not be obtained. It was unclear whether the higher currents are indicative, or possibly due to technical simulation inaccuracies. Our study of gate currents is based on characteristics at V_D= 0 V or low V_D conditions where temperature effects would not have significant impact. Hence, to avoid convergence instabilities and potential misinterpretations, the DD model using the Piezoelectric Polarization model is sufficient and optimal to perform the deeper trap-focused studies into device behavior.

2.5 Conclusions and Perspectives

Fundamental quantities like surface donors as well as performance limiting factors such as tunneling and trap occurrences need to be addressed together in order to obtain a physically intuitive simulated characteristic. A detailed discussion into trap and tunneling impacts on the gate current clarifies how each phenomenon affects the device leakage performance in distinguishable ways. Especially, the trapping contributions from varying spatial locations provide important insights into relative impact. This approach is valid when complemented with output characteristic considerations.

The methodology for building a representative model using the gate leakage current primarily serves as a guideline to build a physically intuitive and functional calibration, based on physical models that are absolutely imperative when simulating a GaN HEMT device. It is meant to act, along with the insight gained into physical boundaries, as the foundation towards more extensive or complicated investigations specific to the designer's purpose. The transient simulations performed in Chapter 4 present an example of how a well-derived fundamental model can be reoriented to be applicable in evolving conditions, with minor redesigns to capture the constrained device response.

Further, this modeling approach as demonstrated can be applied to perform fast and efficient relative comparisons between process or design alternatives targeted at handling specific reliability phenomena. Recognizing comparative device performances can aid fabrication, process or design choices aiming to improve leakage performance criteria of GaN technologies. This validates TCAD simulation to be an effective tool in reviewing and interpreting GaN HEMT reliability performance.

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CHAPTER 3

Simulation Approaches for Transient Analysis

CAPACITANCE VOLTAGE AND ON-RESISTANCE

3.1 Introduction

Material defects manifested in the form of traps limit charge transport and degrade the 2-DEG. These effects often worsen under high frequency conditions. The charge distribution within the structure can be substantially altered in the presence of slow discharging traps, effects that are observable from capacitance-voltage characteristics.

Robust device operation under off-on transitions [3.1-3.2] is critical for switching applications, which renders traps with slow de-trapping time constants a crucial reliability concern. The switching efficiency is impeded by carrier trapping, which limits the charge transport efficiency.

This chapter investigates trap effects under transient conditions, through illustrating how specific traps can modulate the capacitance voltage profiles and resistances of a modelled device.

Changes in Method

Prior to continuation of the simulation studies, the primary model has been improved to attain a more versatile and stronger representation of the GH-25 process. We apply the approach described in the last chapter to build a physics based model for a second device structure more carefully tailored to closely replicate the distinct features of the GH-25 structural process. This allows us to draw meaningful inferences regarding issues specific to this technology.

The device schematic is displayed in Figure 3.1, with the slanted, T-shaped Schottky gate and the source terminated field plate (FP) being the major additions. These extensions help with better distribution of electric field gradients, which improves lifetime and breakdown performances. The structure is minimally doped throughout, with background doping concentration set to 1×10^{15} cm^{-3}.

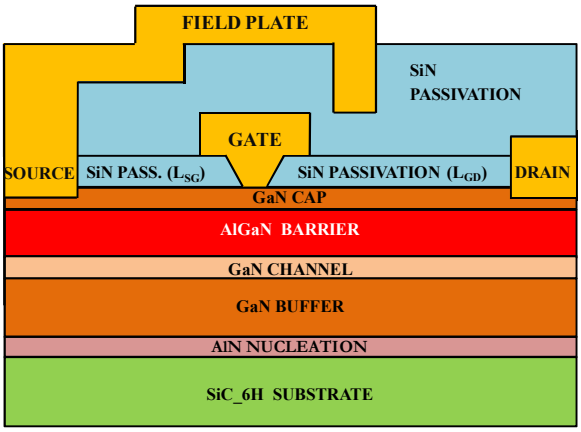


Figure 3.1: Virtual device schematic for the UMS GH-25 technology

To control the leakage current among other considerations [3.3, 3.4], iron doping is present in the device. Deep buffer acceptor traps with a concentration of 5×10^{17} cm^{-3} are introduced to simulate its effects [3.3]. The surface donor density is defined with 4×10^{13} cm^{-2} energetically located at 0.55 eV from the E_C to support the 2-DEG at the AlGaN/GaN interface.

To consider the unavoidable fallibilities of a real device, a gate current tunnelling component is activated at the gate/GaN cap interface in addition to traps in the AlGaN barrier. The Schottky barrier is maintained at 1eV. Table 3.1 summarizes the key changes in simulation parameters for the new model. It also includes changes limited to the transient simulation approach.

Table 3.1: Difference in simulation approach for following discussions

Previous Model	New Model
No field plates	Source terminated field plates
Rectangular gate	T shaped slanted gate
Highly doped GaN cap	Undoped throughout the structure
No buffer doping	Deep buffer traps to compensate for Fe doping
TRANSIENT SIMULATIONS	
Sdevice Solver: SUPER	Sdevice Solver: ILS
Driving force F_{hfs} for electron mobility [eq. 2.20] Gradient of quasi fermi level	Driving force F_{hfs} for electron mobility [eq. 2.20] Electric field parallel to closest semiconductor interface

Transient simulations begin after an initial solution has been obtained for the modelled device. Then, the time is incremented in steps and the device is re-solved. To perform discretization of the non-stationary equations, the stable Backward-Euler (BE) [3.5] method is chosen. For each iteration of the BE solution at an analysis frequency, circuit equations and contact equations are solved in addition to Poisson and electron, hole equations. To further facilitate simulation efficiency, the iterative linear solver –ILS from Sentaurus especially suitable for wide-bandgap materials [3.6] is utilized and optimized to perform all computations.

Because of the un-doped and the wide-bandgap structural details, the driving force for high electric field saturation is changed to the electric field parallel to the closest semiconductor interface. The general force field as calculated from the gradient of the quasi Fermi level makes the simulation unstable in regions with very low carrier densities [3.5, 3.7].

3.2 Transient Simulation of C-V Characteristics

A. TESTING APPROACH

The devices under study are packaged devices with gate section of $1000 \times 0.25\ \mu m^2$. As such, attempted C_g-V characterizations have proved unreliable due to very small C_g magnitudes which were indifferentiable from measurement noise. Hence, a simulated model is very useful to explore charge modifications that could be expected due to BS under transient conditions in conjunction with frequency effects. Transient capacitance voltage (C-V) simulations at multiple frequencies performed on the developed GaN HEMT model can provide detailed insight into acceptor trap behavior localized at the four critical device regions.

C-V profiles reflect carrier distribution in the device and are used to extract the 2-DEG sheet carrier concentrations [3.8-3.9]. Hence, AC small signal C-V profiles extracted at different V_D can capture trapped charge distributions and illustrate individual and relative effects of each trap type at different stages of operation [3.8- 3.10]. The comparative trap impact under low and high frequency conditions is also advantageous to identifying sensitive or trap-susceptible operational environments.

Bias Definition for AC analysis

AC transient analysis is performed in a mixed-mode environment to extract the device C-V profiles. Each device contact drain, gate and source is defined as a voltage source acting as a circuit node. The coupled solving of the drift diffusion equations is extended to allow small signal AC analysis and compute the frequency dependent admittance matrix Y between defined nodes. The equivalent small signal model is defined in terms of voltage and current excitation vectors:

$$\delta I = Y \delta V \tag{3.1}$$

At a given excitation frequency f, the admittance matrix can be represented as:

$$Y = A + i2\pi f\ C \tag{3.2}$$

Where A is the conductance matrix and C is the capacitance matrix.

Hence, by calculating the current response of a chosen contact node when a small voltage signal is applied to another, the small signal capacitances can be extracted for a chosen constant frequency or for a defined frequency range.

AC simulations are first performed with no traps to obtain the reference profile and visualize the initial response. The drain and gate voltage sources in the system are defined as piecewise linear functions as described in Figure 3.2. The source is grounded.

V_D is pulsed to reach a constant value of 2, 5 or 10 V at 1s. After 1s to stabilize V_D, V_G is pushed to a reverse bias of -6 V in deep pinch-off, and then pulsed to a forward bias of +2 V. During this off to on transition, we carry out coupled AC analysis to extract the capacitance profiles. A longer transition period of 2 s (4s - 6 s) is allowed to capture the gradual response. Hence, the gate and drain node voltages define the timing transient. All three power supplies however need to be excluded from the coupled AC analysis, to avoid short circuiting the AC analysis.

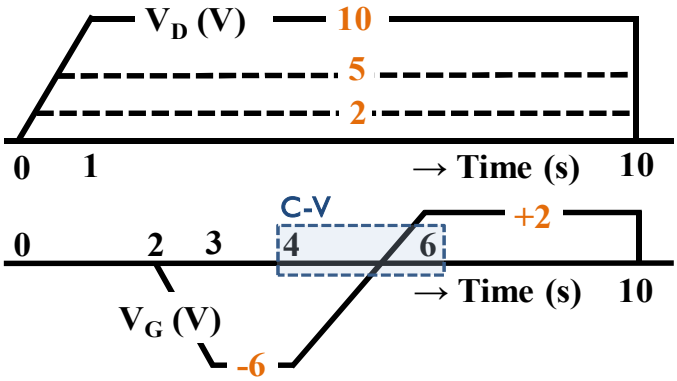


Figure 3.2: Defined gate and drain voltage sources for C-V analysis

The associated data flow for the transient analysis approach is described in Figure 3.3.

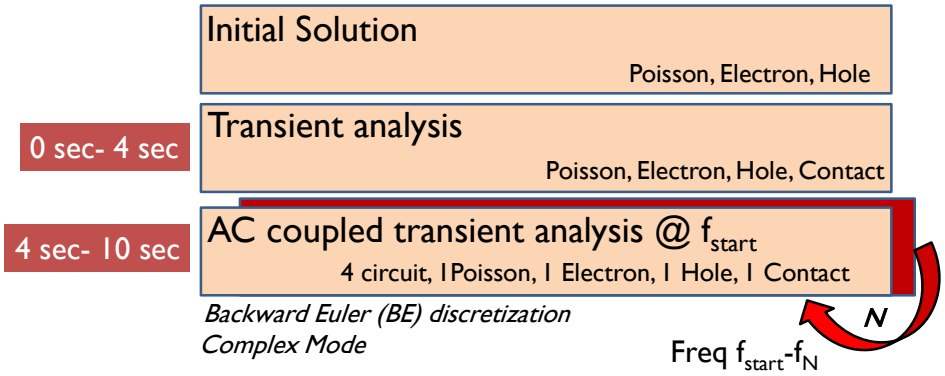


Figure 3.3: Data flow for the transient analysis in Figure 3.2

Just a normal transient analysis with respect to time is performed for the first four seconds when the biases reach the initial conditions for C-V analysis. Then, during the extraction of the capacitance profiles, the coupled AC transient approach is used, which computes the response for each frequency specified through the frequency range and number of frequency points.

Reference C-V characteristics

The gate capacitance C_g represents modifications in the gate charge controlled by the thickness of the effective barrier. The typical C_g-V profile for V_D = 5 V and frequency of 1 GHz is illustrated in Figure 3.4.

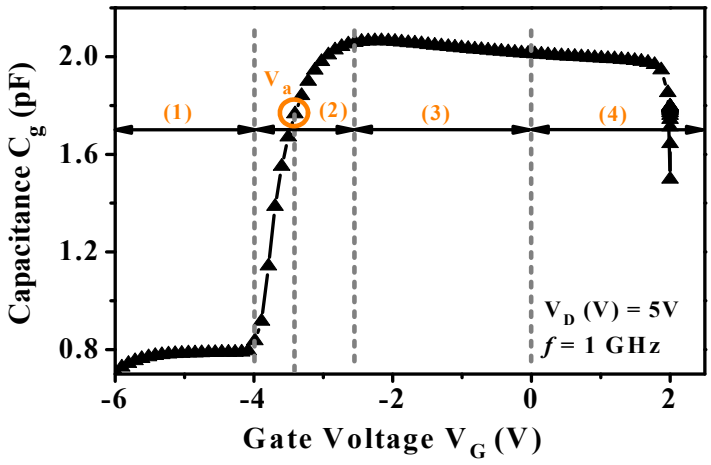


Figure 3.4: Typical reference C-V profile at V_D = 5V

Four stages of device action, as a function of applied gate voltage V_G, can be identified from the simulated C_g. The GaN HEMT at zero bias has a high 2-DEG density due to the interface polarization charges supported by the surface donors. In Region 1: when $V_G < V_{th}$, the 2-DEG is pinched off and has only a trivial channel density (n_s). Thus, the vertical depletion width is relatively constant and the effective barrier extends deep into the GaN buffer. The effective C_g is the serial combination of the barrier, channel and buffer capacitance contributions. Hence C_g is low, and displays minimal change with V_D.

The horizontal depletion slowly extends further for higher $|V_G|$ biases, thus decreasing C_g slightly. Region 2 depicts the device turning on in response to higher V_G as n_s starts to grow. The rise of C_g represents the channel building up from the pinch-off point to respond to the applied V_D while the effective barrier reduces. At this time, the edge of the depletion width gradually moves up to the AlGaN/GaN hetero-interface. This is when the effective barrier is minimal, and C_g is derived between the gate and the channel.

The V_a point is critical corresponding to when the channel density becomes equivalent to background doping. This condition also coincides with V_{th}, a $V_{th} \sim V_a \sim$ -3.5V. Hence, the initial C_g slope is a function of defined material properties. A higher C_g at the end-point of Region 2 indicates stronger channel conduction. Region 3 exhibits a slight decrease in C_g with increased V_G, as the depletion region grows towards the source and the 2-DEG electron density saturates.

In Region 4, the gate is forward-biased. As such, the gate now requires electrons within the previously depleted AlGaN barrier to support this positive voltage. Since the AlGaN layer is minimally doped, and the channel is already saturated, the device cannot respond to the forward potential and there is an abrupt fall in C_g [3.11].

The GH-25 technology is meant for applications until 20 GHz [3.4]. For our study, Figure 3.5 investigates the effect of f variation between 10 kHz-15 GHz on C_g profiles for V_D= 2 to 10 V.

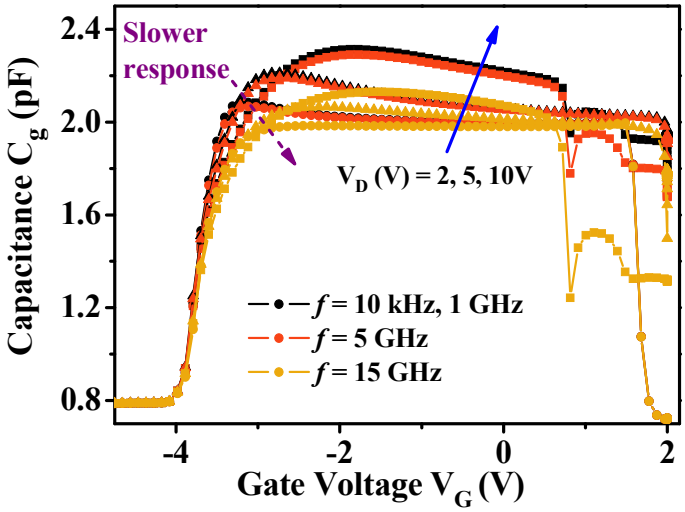


Figure 3.5: Variation in C_g profiles for V_D= 2, 5 and 10 V at different frequencies

The C_g characteristic reflects the effect of bias and frequency over the four defined regions. With a higher V_D requiring a higher drain current I_D and a greater supporting channel density, the device needs longer to reach the higher corresponding C_g level. Thus, Region 2 is wider and displays a smaller slope for a greater V_D. The decrease in Region 3 is also more pronounced at a higher V_D which is due to broadening of the depletion near the drain edge, effectively screening the channel from V_G variations, and reducing C_{gd} strongly [3.12]. Thus C_g falls, despite the improvement in C_{gs}. The C_g at V_D = 10 V has a narrow Region 3, and merges with Region 4 (V_G > 0 V). The C_{gs} fall in Region 4 sets in earlier for the high V_D = 10 V because of wider horizontal depletion.

For $f \approx$ 15 GHz, approaching the GH-25 technology limits, a significant drop in C_g is observed in Region 3 due to background trapped charges failing to follow the signal and slowing the response. This falling section of the C_g characteristic is due to a decrease in C_{gs}, and is more important at higher V_D which supports higher trap occupancies. The C_{gd} however remains unchanged, controlled dominantly by the horizontal depletion width. These observations agree with C-V measurements performed in [3.11]. The effect of f is strengthened at higher V_D as can be inferred from the C_g-V characteristics in Figure 3.6 for a range of f at different V_D voltages.

The characteristics remain identical for frequencies between 10 kHz and 3 GHz. Deviation begins from a threshold frequency of 3-5 GHz at which C_g just starts weakening.

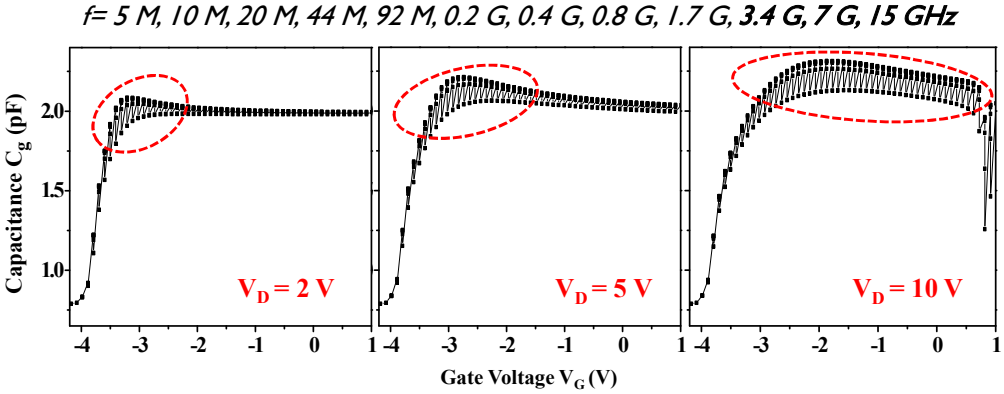


Figure 3.6: C_g-V characteristics for frequencies between 5 MHz and 15 GHz for V_D= 2, 5 and 10V

For V_D= 2 V and 5 V, the *f*-induced variation is closely restricted to the end of the Region 2 slope, due to a portion of charges responding slowly to the device turning-on. This limits the maximal achieved C_g. Bias dominates the rest of the characteristic except for V_D= 10 V when higher f is seen to reduce C_g levels considerably in Region 3 as also presented in Figure 3.5. This compensates for the rise in C_g that a higher V_D would normally support at lower defined *f*. Hence, as seen in Figure 3.5, the control of V_D on the Region 2 slope is quite diminished at *f* = 15 GHz and the three curves are almost identical on reaching Region 3. Further, the C_g collapse under forward bias in Region 4 is notably worsened under high *f*, due to a heightened inability of trapped electrons to respond to the AC signal.

B. GENERAL IMPACT OF TRAP SPATIAL LOCATION

In the previous Chapter 2, we have observed that the spatial location of traps affect the severity of the degradations they could potentially induce in the GaN HEMT. The interface traps at the surface or at the AlGaN/GaN heterointerface are direct limiting factors for the achievable channel density hence they have substantially higher impact. Buffer traps could be important because they comprise a notable section of the GaN structure. AlGaN barrier traps could be an extension of surface degradations or arise due to piezoelectric stresses. The traps defined in these regions could become significant constraints under certain conditions.

To enable a general outlook into relative trap impact, and physical changes that could accompany possible shifts in C_g characteristics, Figure 3.7 displays the changes in (left) conduction band energy (E_C) and (right) space charge distributions due to AlGaN and AlGaN/GaN traps for a cutline close to the gate-drain edge (along the device vertical axis) at V_G = -3 V for V_D= 2 and 10 V.

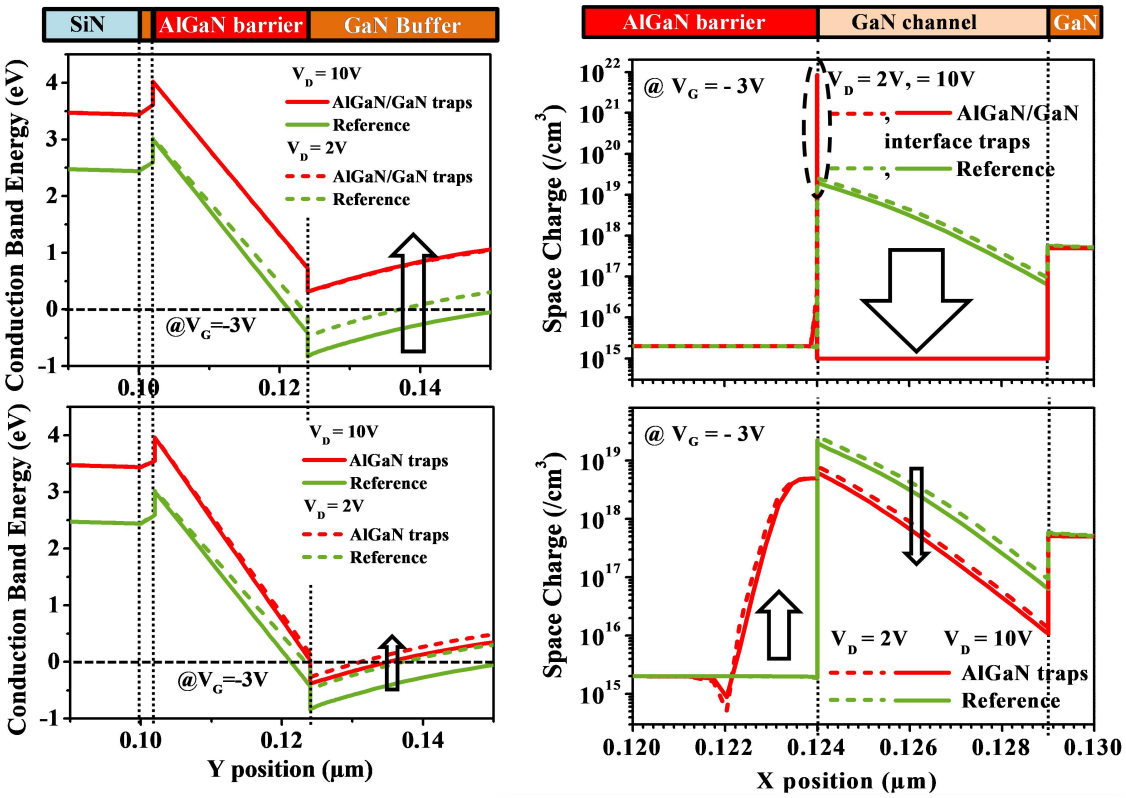


Figure 3.7: (Left) Conduction Band Energy and (right) space charge distribution for bulk AlGaN and AlGaN/GaN interface traps at V_G = -3V

Trapped charges in the AlGaN raise E_C higher, increasing barrier height. However, E_C at the 2-DEG though degraded still remains negative (below the E_F) thus retaining an active concentration of channel charge. In contrast, E_C in presence of AlGaN/GaN traps shifts notably higher such that the entire notch at AlGaN/GaN interface is above E_F, rendering channel density minimal.

From the space charge comparison, it is evident that occupied AlGaN/GaN traps substantially increase the hetero-interface charge. These trapped charges not only increase the electric field across the AlGaN barrier but also cause a field spike bordering the channel, which triggers a fall of charge density in the 2-DEG. For the less severe scenario involving just AlGaN traps in the barrier, we notice an accumulation in trapped charge within the AlGaN barrier and a moderate drop in space charge within the channel.

Hence, based on these and previous discussions, we can expect the C_g characteristics to display substantially high vulnerability to change in the presence of interface traps. However, which regions of the C_g nature are affected the worst, as well as a comparison of the trap response to a slow turn-on of the device gate remains to be studied. The frequency effects also add a different level of insight towards gauging the region or interface trap-limited response to a rapid change in signal.

C. TRAP EFFECTS ON C-V CHARACTERISTICS

Acceptor traps have been introduced into the reference model at the four device locations of the AlGaN barrier, GaN buffer, and AlGaN/GaN hetero-interface and at the surface. The simulated trap parameters are chosen in accordance with previous discussions in Chapter 2 according to reports in literature. Identical energy positions located 0.5 eV from E_C are defined to enable discussion of relative impact of the trap spatial location.

Effects of introduced traps on each region of the C-V profile are studied independently, in comparison to the reference profiles for a low (1 GHz) and a high frequency (15 GHz).

AlGaN Barrier Traps

Figure 3.8 presents the simulated C_g-V profile at 1 GHz and 15 GHz for uniform distribution of traps introduced in the barrier layer with a concentration $N_A = 5\times10^{18}$ cm^{-3}. At 1 GHz, we observe only a slight decrease in the Region 2 slope while C_g levels in region 3 are preserved.

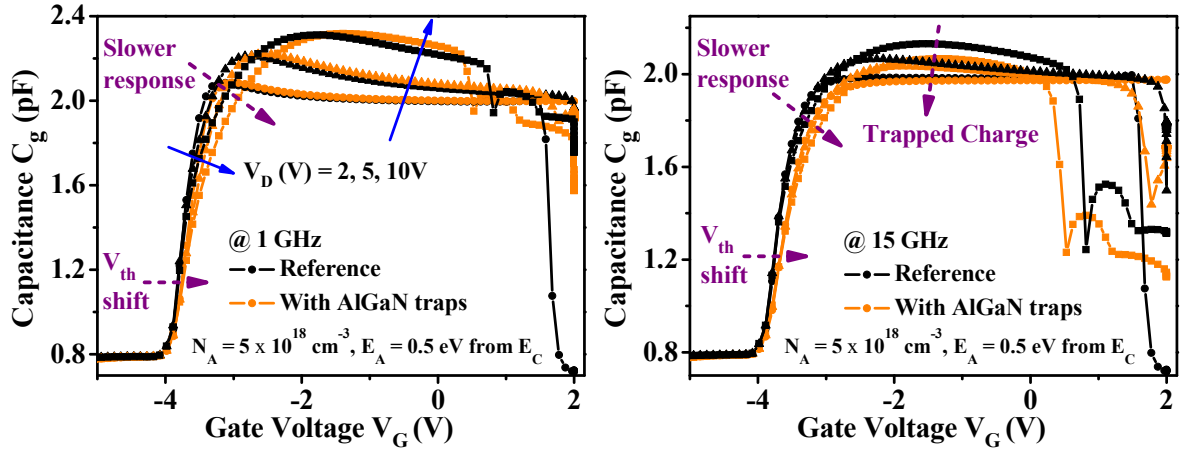


Figure 3.8: C-V profile for AlGaN traps at 1 GHz, 15 GHz

At f = 15 GHz, a small shift in V_{th} is observable. Also, C_g is appreciably reduced in Region 3 due to the presence of trapped charges in the barrier causing a reduction in C_{gs}. With the traps, the C_g fall in Region 4 is greater at higher f.

Thus, we can conclude that the effect of barrier traps is more important at higher frequencies, where the worsening in C_g is higher. This bias region and frequency inter-dependence is demonstrated in Figure 3.9 that plots the barrier trap-induced change in C_g ($\Delta C_g = C_{g,\,ref} - C_{g,\,trap}$) for 12 frequency values at V_D= 2, 5 and 10 V.

Irrespective of bias or f, maximum change in C_g is induced in Region 2 around the V_{th} value. For higher V_G, ΔC_g reduces gradually, but the roll-off slope is slower for higher V_D conditions, which sustain high ΔC_g values longer into Region 3.

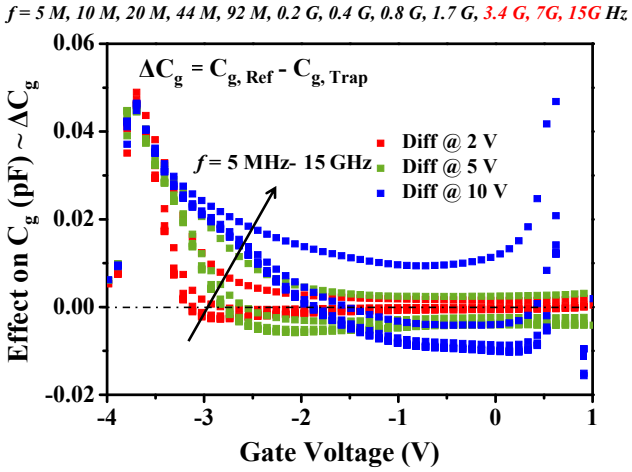


Figure 3.9: Bias and frequency dependence of barrier trap effects on C_g

The curves corresponding to initial range of low frequencies are superimposed on each other. They also display negative ΔC_g values in Region 3, which implies the presence of an overshoot above reference C_g. This corresponds to the eventual de-trapping of trapped charges in response to the applied bias, causing a delayed growth in current and thus C_g.

The curve obtained at 3.4 GHz is the first to show deviation, with the two higher frequencies displaying stronger tendencies towards high ΔC_g. For f= 15 GHz, the overshoot tends to disappear as f is too high to allow even the delayed response to occur within the 2 s transient window (see Figure 3.2). This is further worsened at higher V_D resulting in significant dispersion from reference.

GaN Buffer Traps

Figure 3.10 presents simulated C_g-V profiles at 1 GHz and 15 GHz for traps introduced in the GaN buffer with $N_A = 10^{18}$ cm^{-3}. In comparison to the AlGaN traps, the shift in V_{th} to a less negative V_G is more noticeable even with the lower concentration, for both f = 1 GHz and 15 GHz.

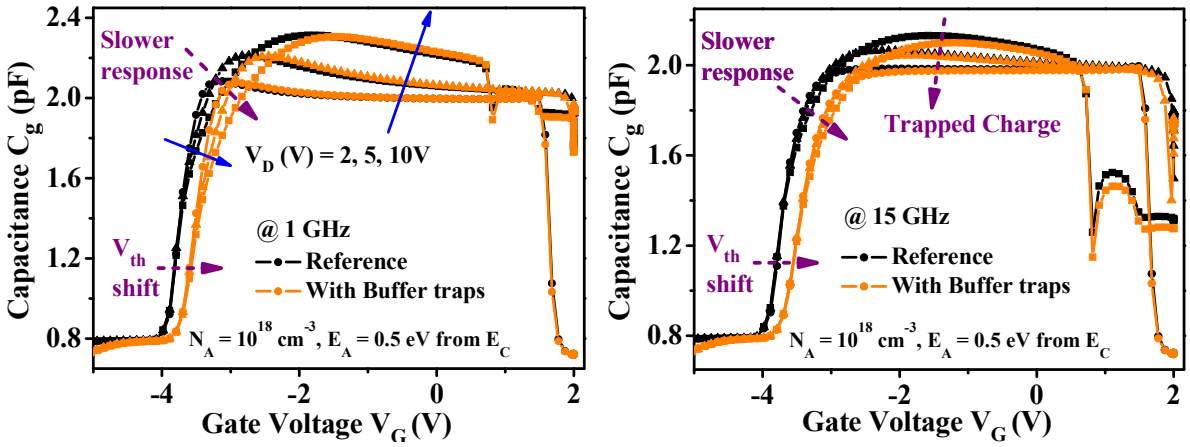


Figure 3.10: C-V profile for GaN buffer traps at 1 GHz, 15 GHz

Since the buffer layer is wide and deep, located just below the channel, the trapped charges are capable of changing V_{th} significantly.

However, they barely affect the charge density and barrier width between the gate and channel. When the device is on, the channel defines the end of the effective barrier seen by the gate capacitance. Hence, the effects of changes in the buffer charge component is screened by the 2-DEG channel. Even at high f= 15 GHz, the reduction in C_g levels in Region 3 is marginal.

The ΔC_g dependence for buffer traps is shown in Figure 3.11.

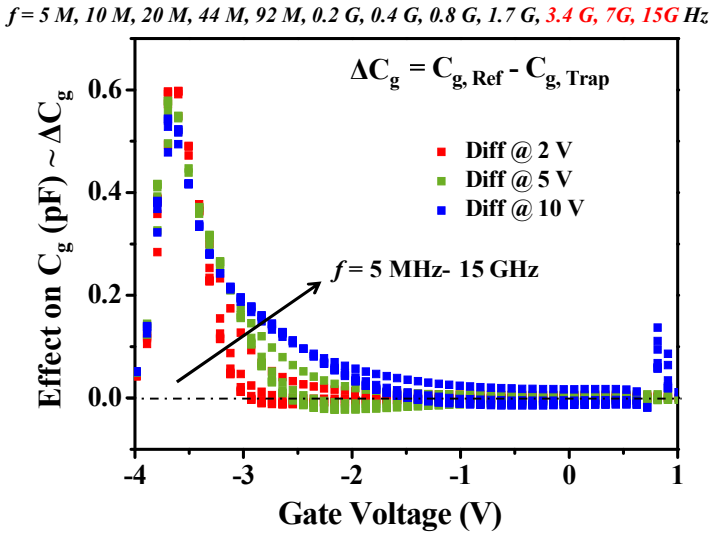


Figure 3.11: Bias and frequency dependence of buffer trap effects on C_g.

The buffer trap degradation is controlled mainly by its position and thus quite constant, with no exacerbation at higher *f*. The relative increase in ΔC_g from low to high *f* is nominal. Here too, the general trap effect is maximal near V_{th} similar to barrier traps, but absolute ΔC_g magnitudes are notably higher across the V_G range.

For lower V_D= 2 V or 5 V values, we observe an earlier rise in ΔC_g for f > 3.4 GHz in Region 2. Comparative to positive ΔC_g levels, the overshoot observed for low V_D, low f conditions is quite small indicating that buffer traps are not only more damaging but also take longer to de-trap, which contributes to the V_{th} shift.

AlGaN/GaN Interface Traps

As discussed earlier, interface traps directly influence piezoelectric charges and channel density, and hence can seriously aggravate charge distribution in the device. Figure 3.12 illustrates the C_g-V profile at 1 GHz and 15 GHz simulated for traps defined at the AlGaN barrier/GaN channel interface with N_A= 5×10^{12} cm^{-2}. The degradation in C_g characteristics in the presence of AlGaN/GaN traps is distinguishably higher than for buffer or barrier traps.

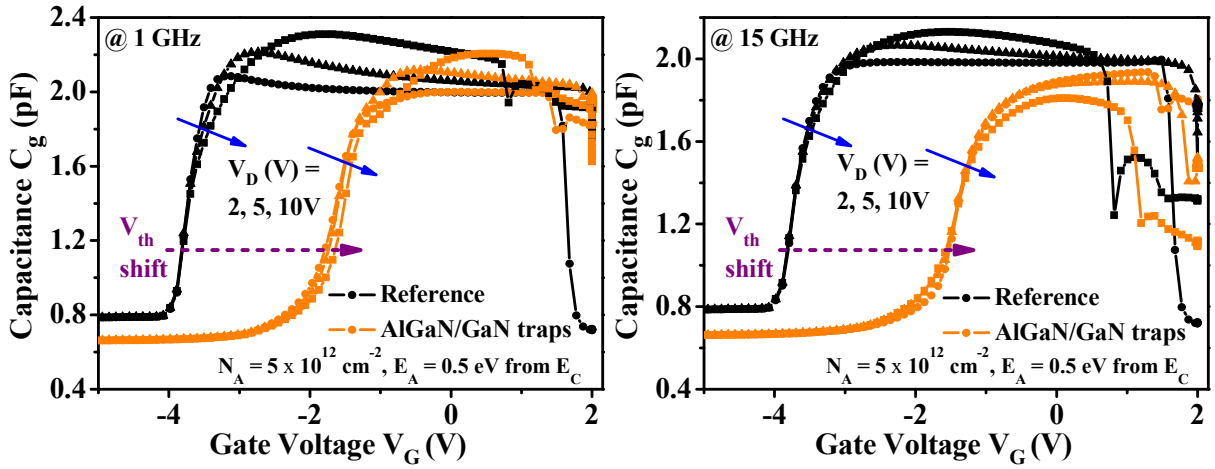


Figure 3.12: C-V profile for AlGaN/GaN hetero-interface traps at 1 GHz, 15 GHz

At the chosen N_A, V_{th} is significantly degraded by around 2 V at both f= 1 GHz and 15 GHz since the negatively charged interface traps considerably restrict the density of the 2DEG channel. Lower trap concentrations might diminish the magnitude of degradation. In Region 4, with the device still attempting to respond with charges to compensate for the applied bias, C_g remains stable until a higher V_G before it collapses.

Importantly, at 1 GHz, in the delayed Region 3, trapped C_g curves still approach reference curve magnitudes. At high f =15 GHz however, final C_g levels in Region 3 are notably lower, indicating a substantial trapped charge which fails to respond to the rapid change in signal. This is also illustrated in the ΔC_g profiles plotted for AlGaN/GaN traps in Figure 3.13.

It is noticeable that the ΔC_g nature is quite dissimilar to barrier or buffer traps and appreciably higher in magnitude.

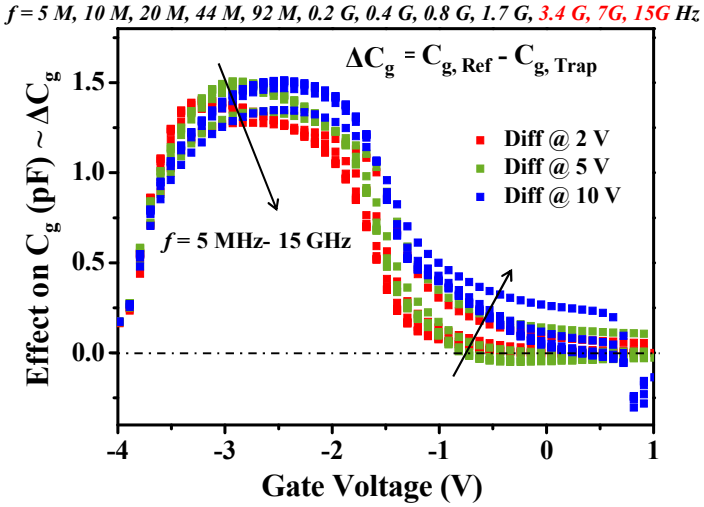


Figure 3.13: Bias and frequency dependence of AlGaN/GaN trap effects on C_g

The maximum change is concentrated around a range of -3 V to -2 V, after the reference V_{th} values and before the shifted V_{th} value ~-2V. Variations due to bias and frequency are not monotonic. In Region 2 at higher V_D, the ΔC_g peak is delayed but eventually higher, indicating that the trapped charge build-up as V_G rises to try to turn the channel on, is slow but elevated. The associated depletion in the AlGaN barrier also extends deeper, as ΔC_g at greater V_D remains higher throughout Region 3 and Region 4.

The lower V_D values have closer curves and lower disparity in Region 3. The overshoot that expresses de-trapping within the 2 s time duration, occurs much later towards the end of Region 3 and is essentially negligible. The distinction due to *f* occurs only after 7 GHz, all previous curves being dominated by the bias-induced trapping dynamic. For *f* = 15 GHz, ΔC_g is lower in Region 2 but higher in Region 3/4 demonstrating that higher frequencies impact both charging and discharging efficiency of the hetero-interface traps.

Surface Traps

Traps were introduced at the top SiN passivation to GaN cap interface with $N_A = 10^{12}$ cm^{-2} to investigate their effects on the C_g characteristics as displayed in Figure 3.14. Since surface acceptor traps act to deplete the surface donor density, occupied acceptors at the surface considerably deteriorate the device response.

The device response is observed to clamp to a low C_g, independent of applied V_D. Region 2 is wider and there is no detectable Region 3 since the device is still attempting to respond to the applied signal when the gate becomes forward biased. However, the beginning of Region 2 is identical to the reference before continued response is blocked, prior to the threshold voltage point. Since the response is constant, it is irrelevant to compare the ΔC_g distribution for surface traps.

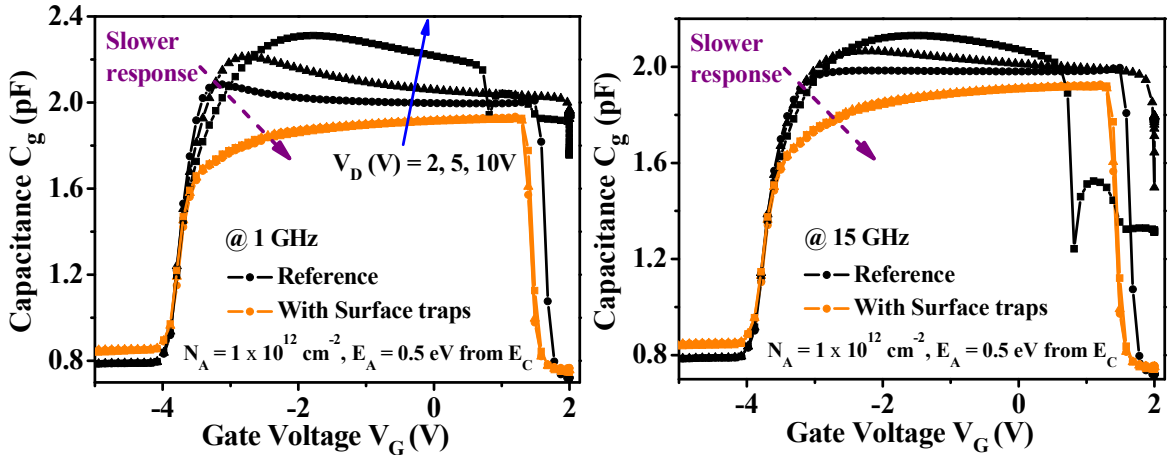


Figure 3.14: C-V profile for SiN/GaN surface traps at 1 GHz, 15 GHz

D. DISCUSSION: RELATIVE IMPACT OF TRAP LOCATION

Current Transient Response

A closer look at the I_D response to the applied timing function (see Figure 3.2) under V_D = 10 V and 2 V is presented in Figure 3.15. As V_G is pulsed from -6 V to +2 V, it traverses the point when the device just turns on beyond V_{th}= -3.5 V.

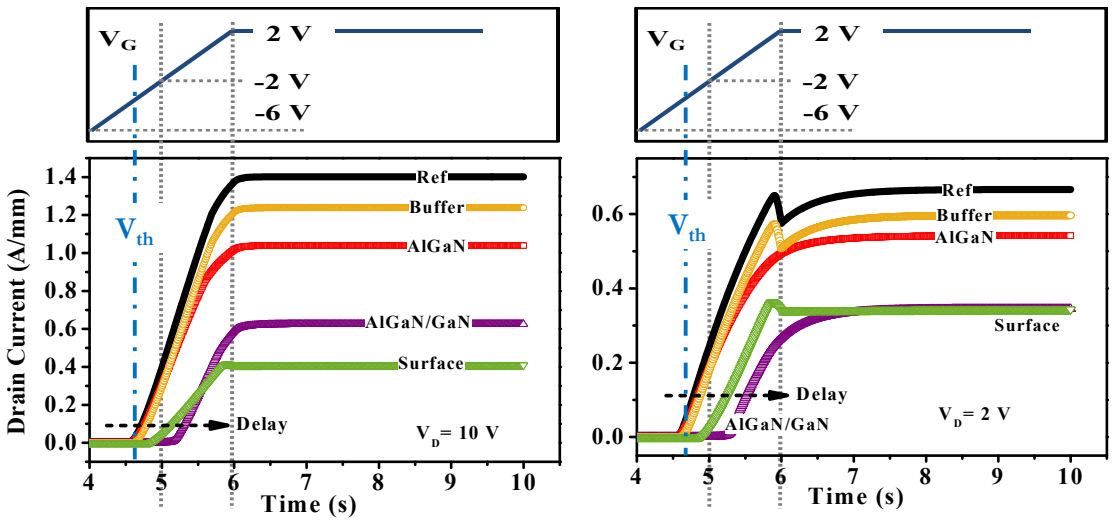


Figure 3.15: I_D response to defined time pulse for the barrier, buffer, AlGaN/GaN and surface traps for V_D= 10 V (left) and 2 V (right)

At V_D = 10V, I_D simulated with barrier or buffer traps closely follows the reference from t = 4.5 s when the V_G pulse crosses V_{th}. These curves reach similar levels by t = 5 s. The I_D corresponding to surface traps begins to respond just before t = 5s but fails to rise since the device is unable to supply sufficient charge to support the applied V_D.

With AlGaN/GaN traps, the initial response is markedly delayed starting only at around t = 5.2 s. However, it grows faster due to rapid detrapping, displaying a higher slope and greater I_D than the surface traps.

At V_D = 2V, both reference and buffer traps display a kink-like feature before achieving stable response. Since the reference model also has background buffer traps, this indicates that device response with traps located deep in the buffer layer, while rapid initially, fails to maintain the requisite current. Delayed trapping abruptly reduces the stable current. Response of AlGaN traps is slower and smoother. Difference in I_D between reference, AlGaN and buffer traps is now reduced at V_D = 2 V. Surface trap response remains low with a similar I_D as for V_D = 10 V, and also displays a small kink due to an unsustainable initial rise. Hence the AlGaN/GaN associated response is considerably delayed and I_D levels are lower than the surface trap response in contrast to V_D = 10V.

Figure 3.16 studies the I_D-V_G response at V_D = 2 V, 10 V under influence of different traps.

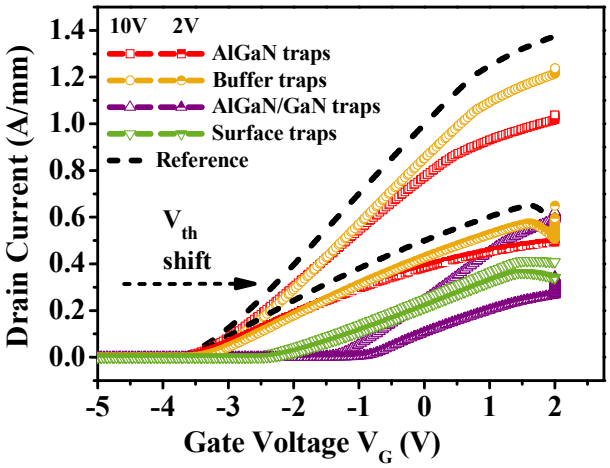


Figure 3.16: I_D -V_G characteristics for the barrier, buffer, AlGaN/GaN and surface traps for V_D= 10 V and 2 V during the transient analysis from V_G=-6 V to V_G=+ 2 V

A V_{th} ≈ -3.5 V is clearly identifiable in the reference curve. AlGaN/GaN traps induce the greatest V_{th} shift while both interface trap responses are severely degraded. With buffer traps, despite a small V_{th} shift, the trap response improves greatly as V_G rises. The AlGaN trap response in contrast is initially favorable and starts worsening as V_G rises, and the device is driven deeper into conduction.

Inferences from Transient Response of Traps

Based on the observations from Figure 3.15, Figure 3.16 and the previous ΔC_g plots for each trap, the following inferences are made.

AlGaN/GaN traps have slow initial responses and are generally quite damaging inducing strong V_{th} shifts and heavily diminished currents. They cannot de-trap under low V_D conditions (Figure 3.15) while electron mobility stays low due to scattering. However, they rapidly discharge or detrap under high V_D conditions. Thus, the trap response emulates the reference quite well in following the changes in V_G at high V_D, despite the absolute reduction in magnitudes (Figure 3.16). They charge slowly and hence, high *f* conditions would lower the degradation at reverse V_G. However, high *f* also worsens detrapping in on-state conditions, in which case, a longer interval to respond might lessen its absolute impact. Surface traps induce lower V_{th} shifts than AlGaN/GaN traps and a high V_D induces a marginally better response to V_G bias changes (Figure 3.16). Their effects are generally constant and extremely damaging irrespective of operational conditions since they define the charge distribution in the rest of the structure.

Buffer traps induce moderate V_{th} shifts but the de-trapping response significantly improves at higher V_G and V_D. Beyond the initial delay, the traps respond well to V_G changes (Figure 3.16), close to the reference levels and slope, irrespective of V_D bias. The discharging process might be slightly

faster initially at low V_D, which is why the initial response to the device turning on might be more favorable until V_G becomes constant. A low V_D is not enough to sustain continued de-trapping and the traps might get reoccupied, which results in the current abruptly falling to a lower value before stabilizing (Figure 3.15). These traps, located deep in the structure would not de-trap unless bias conditions were changed, even if more time were available to respond. Hence, *f* has minimal impact, especially at high V_D.

AlGaN traps in high concentrations are slightly more damaging at high V_D conditions while the initial or low V_G response could be close to ideal with no V_{th} shifts. In the on state, the response is favorable until V_G is forward biased (Figure 3.16), then the de-trapping response worsens considerably, resulting in slower I_D growth and a wider difference from the reference. They de-trap quite fast unless the time available to respond is very small. Hence, their effect while moderate for low to medium frequencies might become important at very high frequencies.

Learnings: Region-wise C_g-V control factors

To better visualize the relative impact of different factors on the C_g characteristics, Figure 3.17 presents the typical C_g profile demonstrating the impacts that individual traps can have on each region of the C_g curve. The variation with frequency is also illustrated. This discussion helps us identify and correlate the contribution of specific traps with observed irregularities in C_g behavior.

A lowering of the stable C_g level in Region 3 is induced in presence of trapped charges within the effective barrier. The strongest factor is surface traps with higher worsening at high frequencies. AlGaN and AlGaN/GaN traps also worsen at high frequency. A smaller slope in Region 2 indicates a slower initial response when the device is turning on from pinch-off to V_{th}.

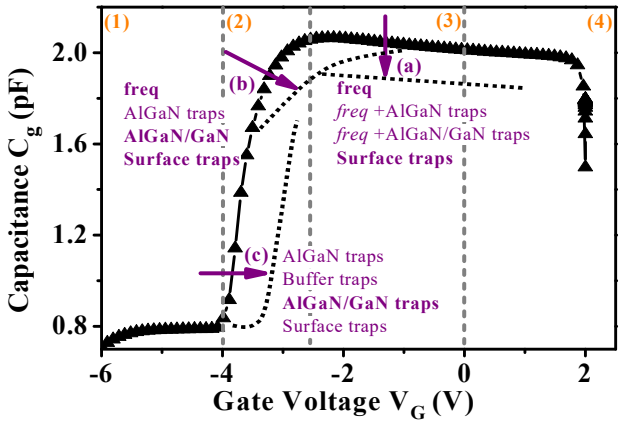


Figure 3.17: Relative impact of frequency and traps on the C_g-V characteristic

AlGaN traps cause small slope bends as V_G rises. This effect increases with high frequencies and is extreme under the influence of AlGaN/GaN and surface traps.

A shift in V_{th} (shift in Region 2) indicates a significant lowering of the available channel density. AlGaN traps create only slight V_{th} shifts, only if present in very high densities. Buffer traps and especially AlGaN/GaN traps significantly worsen V_{th}, the effect being higher at lower V_D. For surface traps, the shift is found to be independent of bias conditions.

Summary and Perspective

Associated changes in the effective barrier and space charge distribution due to trapped charges at varying frequencies are discussed. The specific degradation each kind of trap causes within the C_g profile such as a shift in V_{th} and a lower C_g in Region 2 and 3 is studied to enable identification of relative trap effects on device response during transient analysis. The impact is found to be generally strengthened under high *f* operation and for interface traps, which affect all regions of C_g. Expectedly, the coupling of high bias and frequency conditions are found to be generally detrimental to device response. Surface traps alter the charge equilibrium directly and are equally damaging in all possible conditions. Hence, minimization through improved processes or surface treatments is an essential strategy. AlGaN and AlGaN/GaN traps present a higher threat for high frequencies and worsen the peak C_g in the on-state which can be directly equated to a loss in current and power performance.

3.3 Transient Analysis of R_{on} Performance

This section studies and interprets the turn-on response of a GaN HEMT, impacted by traps in the AlGaN barrier, GaN buffer and at the AlGaN/GaN hetero-interface. The relative potential of each trap is identified through comparing the output response immediately after a transition from a high voltage-off to a low voltage-on state. This approach analyses the fundamental root of current collapse, a combination of bias factors that induce a device state highly vulnerable to trapping. Despite bias levels being restored to normal, low-stress conditions, the subsequent device response continues to be susceptible to trapping dynamics and fails to reach expected GaN performance. The obtained results reflect instead, the trap-limited current response. Discussion into biasing factors for a chosen transient pulse that manipulate these trap-induced delays is performed.

Definition of Pulse Parameters

Four pulse parameters are varied to detect dominant delay-inducing factors to extract information into trapping physics. Changes in the extent of each trap's contribution to device response under varied pulsing conditions are studied. Correlating deviations from the expected response with spatially confined trapping-detrapping instances provides perception into conditions

that promote on-resistance (R_{on}) changes and fall in output drain current (I_D) levels. Transient analysis is performed along with ac analysis at a frequency of 5 GHz, close to the threshold value for which device response just begins to degrade, as obtained in the previous Section 2.5.

Figure 3.18 presents the timing methodology of pulses which define the drain (V_D) and gate (V_G) piecewise linear sources, illustrating investigated parameters. Timing intervals are in the order of seconds to focus on trap effects with longer time constants, unavoidable in any switching instance.

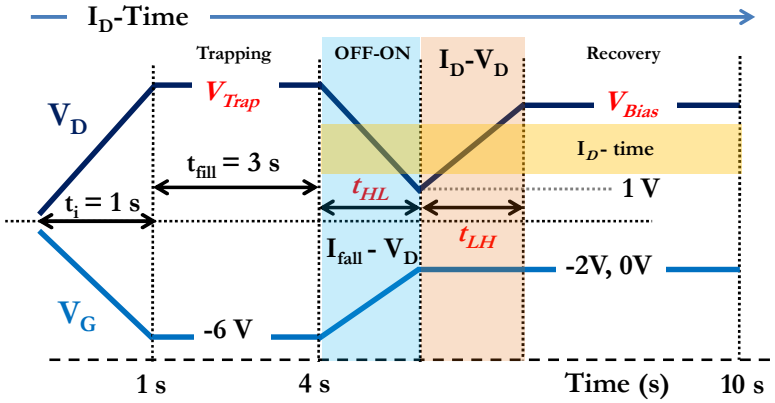


Figure 3.18: Defined drain and gate pulses for transient analysis during 10s. Parameters to be varied are: V_{Trap}: trapping voltage, t_{HL}: t (High to Low), t_{LH}: t (Low to High) and V_{Bias}: Final drain bias

The maximal trapping state t_{fill} is of 3 s duration, where V_G= -6 V maintains the device in deep pinch-off while the quiescent drain bias V_{Trap} is varied. The second studied parameter is the transition time t_{HL} to reach "on" state at V_D = 1V and V_G= -2V and 0V. The resultant current growth is monitored through the I_{fall} characteristic. Immediately following the device's turn-on transition, V_D is swept to V_{Bias} (varied parameter) in a chosen rise time t_{LH} (varied parameter) to provide an I_D-V_D output response at a defined constant V_G. This is followed by recovery at constant bias conditions until 10s.

A. TRAP ENERGY POSITION

Traps have been individually defined in three spatial locations to observe the impact on reference state. Acceptors in AlGaN barrier and GaN buffer have trap densities N_A= 10^{18} cm^{-3} while N_A is 10^{12} cm^{-2} at the AlGaN/GaN heterojunction interface in accordance with previous sections and Chapter 2. Capture cross sections are defined in simulations as 10^{-16} cm^2. Before studying the effects of pulse parameter variations on traps, the consideration of the trap energy positon E_A is vital.

To demonstrate the changes in trap behavior for E_A= 0.3, 0.5 and 0.7eV from E_C, Figure 3.19 presents the I_D-V_D response acquired during t_{LH} for parameters defined as: V_{Trap}= 30V, t_{LH} =1 s and t_{HL}= 1s for V_G= 0 V and -2 V.

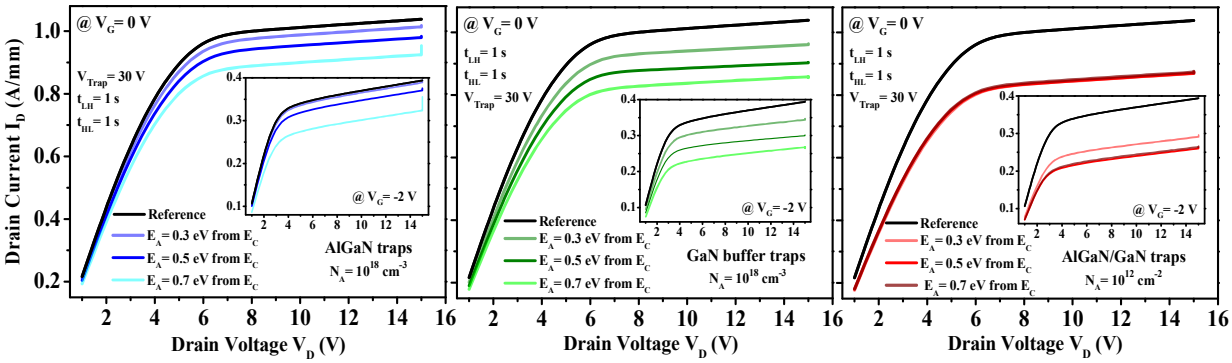


Figure 3.19: I_D-V_D comparison with barrier, buffer and heterojunction traps for a variation in trap energy E_A and trapping voltage V_{Trap}= 30 V, t_{LH}= t_{HL}= 1s

The corresponding R_{on} values are extracted from the linear part of the curves between V_D= 1 to 4 V and summarized in Figure 3.20. The absolute impact relative to reference gets progressively higher from barrier to buffer to AlGaN/GaN traps. The influence of the trap energy positon appears slightly higher for buffer traps at V_G= -2 V.

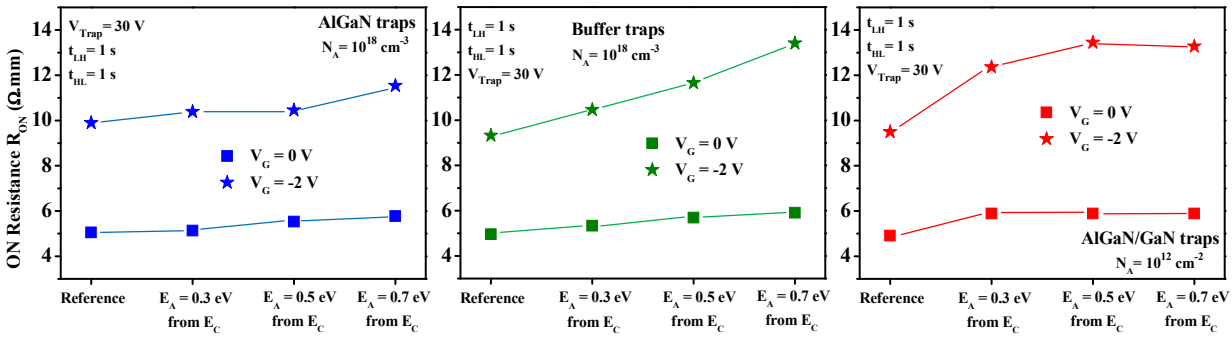


Figure 3.20: Extracted R_{on} comparisons for barrier, buffer and heterojunction traps for variation in E_A

Failure to de-trap within the defined t_{LH} leads to greater I_D loss and R_{on} degradation. Traps further away from E_C have greater de-trapping constants and are observed to have a greater impact.

Barrier and buffer traps induce moderate variation of R_{on} with E_A for V_G= 0V. To enable a clearer view of the associated effects, Figure 3.21 investigates the relative difference (Diff) between the reference and trapped response for the different E_A values at three essential bias points: V_D= 1V representing the start values, V_D= 4 V around the R_{on} sensitive knee voltage region and V_D= 15 V, representing the final degradations in I_D levels. Diff is calculated for each V_G bias as:

$$Diff_{0V/-2V} = \frac{I_{D,Ref} - \left(I_{D,Trap}@E_{Trap}\right)}{I_{D,Ref}} \times 100 \tag{3.3}$$

For AlGaN traps, Diff is generally higher at V_G= -2V except for the shallow E_A = 0.3 eV which easily de-traps under the reverse bias, with negligible deviation from the reference. For E_A= 0.5 eV, Diff is higher but only slightly dependent on V_G.

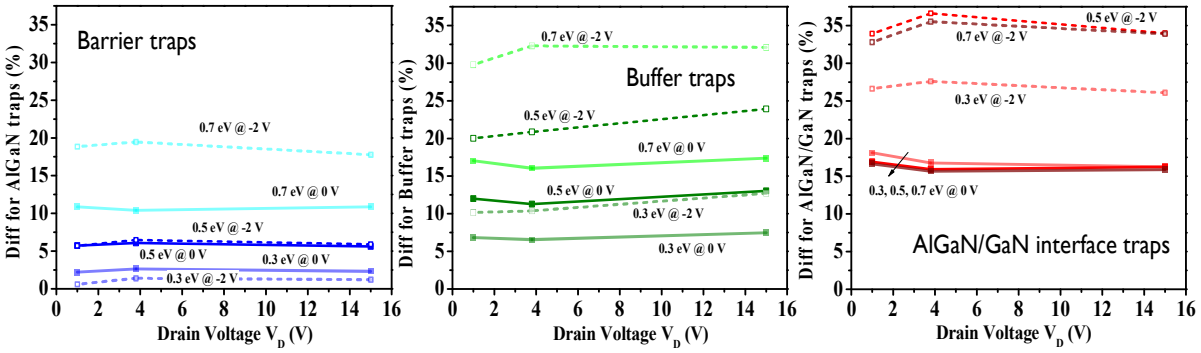


Figure 3.21: Relative difference respective to the reference for barrier, buffer and heterojunction traps varied in trap energy E_A and V_{Trap}= 30 V, t_{LH}= t_{HL}= 1s

For the deeper E_A= 0.7 eV, it is notably higher, with enhanced dispersion from reference occurring at V_G= -2 V. The highest Diff is generally obtained at V_D= 4 V, indicating that trap contribution toward R_{on} degradation is stronger. De-trapping at higher V_D lessens the final I_D loss.

For buffer traps, absolute Diff is higher with peaks at the final V_D, indicating that buffer trap impact is more relevant for I_D losses. The relative escalation in Diff from V_G= 0 V to V_G= -2 V is higher than for barrier traps, making them more significant under reverse bias conditions. In fact, shallower traps at V_G=-2 V cause higher deviations from the reference response than deeper traps during on-state V_G= 0V conditions.

For AlGaN/GaN traps, the maximum Diff values are closer to buffer and much higher than barrier traps. When the channel is on for V_G= 0 V, AlGaN/GaN traps have high occupations irrespective of the energy level, and display constant Diff ~15-20 % in the beginning of the V_D sweep. The dispersion gets lower as V_D rises and the electrons are pulled to the drain. Under reverse gate bias, energetically deep traps present markedly higher Diff values. In the beginning of the V_D sweep, trapping is enabled and Diff peaks around V_D= 4V indicating serious R_{on} degradation.

We choose an E_A=0.5 eV to investigate the evolution of trap contributions to degradations in output I_D or R_{on} response with variation in pulsing parameters.

B. VARIATION OF PULSE PARAMETERS

Variation of V_{Trap}

The I_D-time response at V_G= 0 V, -2 V for the trap filling bias V_{Trap}= 10 V and 30 V is displayed in Figure 3.22 (left) for t_{HL}, t_{LH}= 1s and V_{Bias}= 15V. As the device turns on beyond 4 s, I_D while the voltage V_D returns to 1 V is naturally higher coming down from a higher V_D (V_{Trap}). Figure 3.22 (right) compares the consequent I-V during t_{LH} (growth of I_D as V_D rises from 1 V to V_{Bias}= 15 V during t= 5 s to 6 s, see Figure 3.18).

It is apparent that a higher V_{Trap} promotes higher trap occupation which fail to de-trap during t_{LH} thus degrading R_{on} and I_D response. The change in final I_D is higher for AlGaN and AlGaN/GaN traps, especially at V_G= -2 V closer to the threshold value (V_{th} ~ -3.5 V) where de-trapping is lower.

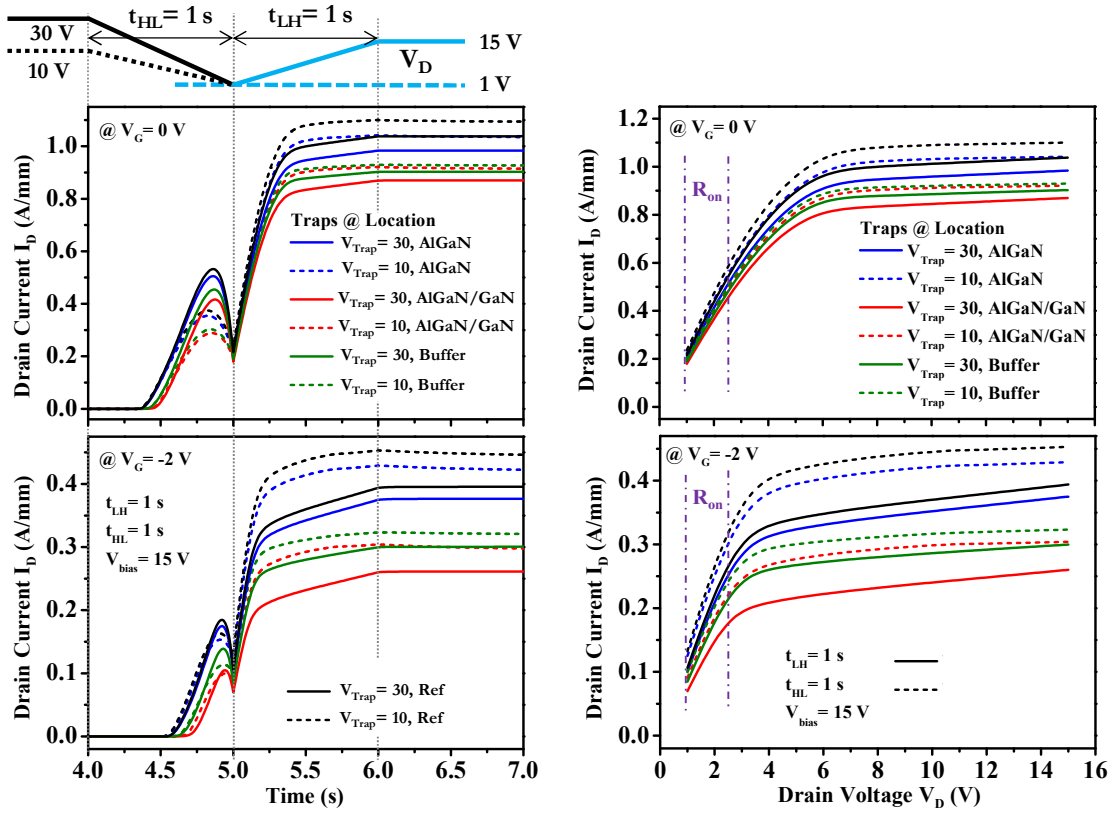


Figure 3.22: I_D-time and I_D-V_D response for V_{Trap}= 10, 30 V at V_G=0 V and -2 V

The R_{on} values are extracted from I_D-V_D characteristics (see. Figure 3.22 (right)) in the linear region of V_D= 1 V to V_D= 2.5 V and plotted in Figure 3.23.

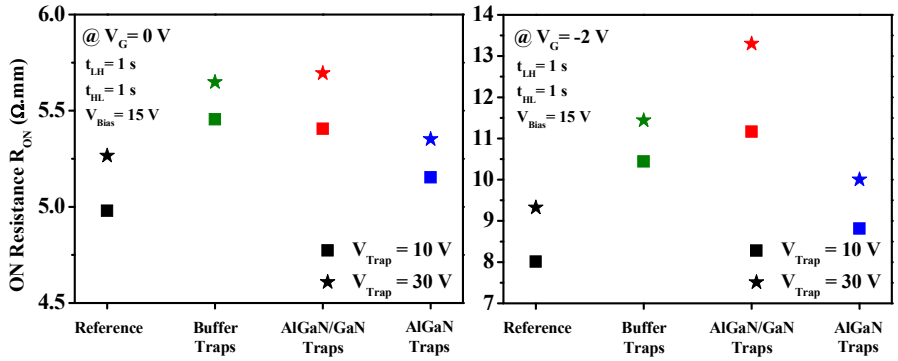


Figure 3.23: R_{on} extracted from Figure 3.22 (right) for V_{Trap}= 10, 30 V at V_G=0 V and -2 V.

R_{on} increase is highest for AlGaN/GaN traps for both V_G, which are the most deleterious on device behavior. At V_G= 0 V, V_{Trap} has similar effects on R_{on} for all three traps and the reference.

However, high V_{Trap} causes stronger R_{on} increase at V_G=-2 V for AlGaN traps, and especially for AlGaN/GaN traps. The detrimental effects of a stronger V_{Trap} appear to be minimal for buffer traps.

Variation of t_{HL}

Figure 3.24 (left) shows the I-V response for V_G= 0 V and V_G= -2 V during t_{HL} (the fall of V_D from V_{Trap} = 30 V to 1 V, referred to as I_{fall}-V, see. Figure 3.18) for varying t_{HL}= 1s and 2 s.

The corresponding I-V responses during t_{LH} (the rise of V_D from 1 V to V_{Bias}= 15 V) are obtained from t=5 to 7 s (t_{HL}= 1s) and t= 6 to 8 s (t_{HL}= 2s) and plotted in Figure 3.24 (right).

A longer t_{HL} interval allows a larger amount of traps to respond to the turning-ON pulse, thus displaying a higher corresponding I_{fall}.

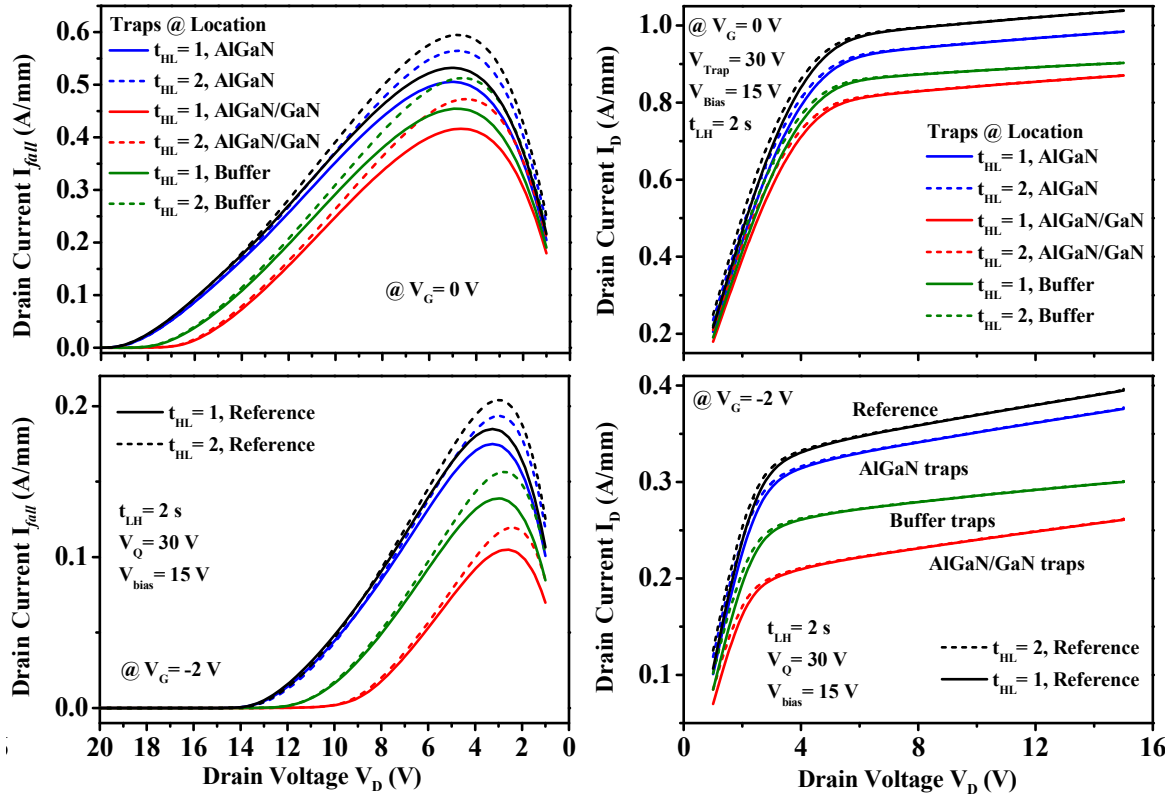


Figure 3.24: (left) I_{fall}– V and (right) I_D- V_D response for t_{HL}= 1s and 2 s at V_G=0 V and -2 V

During the subsequent V_D sweep from 1 V to 15 V, the higher concentration of free carriers slightly improves R_{on} similarly for all the trapped curves. Concurrent behavior is observed at V_G= -2V. Final I_D levels are unaffected.

The improvement for a higher t_{HL} is of similar magnitudes for all traps. To extend the range of discussion further, we have drastically reducing t_{HL}.

Figure 3.25 presents the I_{fall}- V characteristics for t_{HL}= 0.1s and 0.2 s.

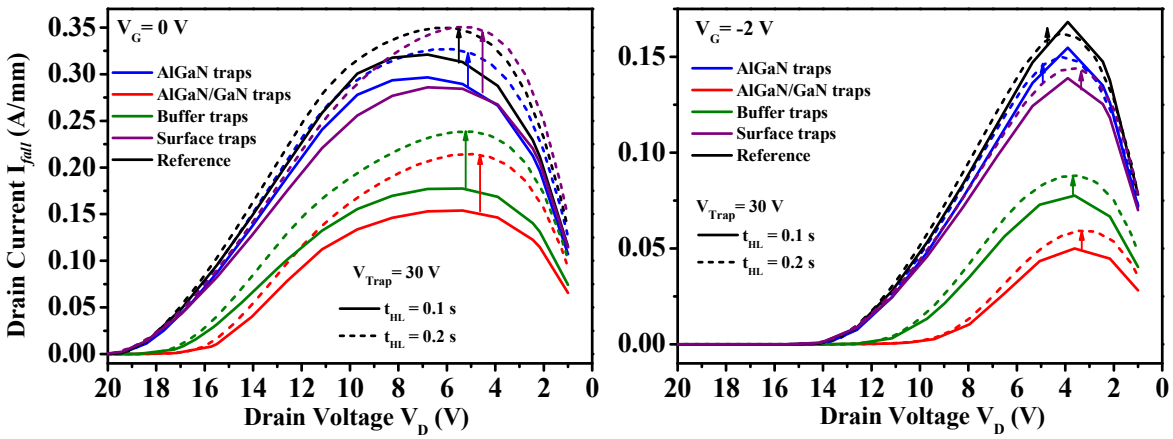


Figure 3.25: I_{fall}-V characteristics for variation in t_{HL}= 0.1s and 0.2 s for different traps

It is noticeable that the general behavior of inducing an increase in the current response under a longer t_{HL} is sustained even at low t_{HL} levels. The achieved I_{fall} levels for t_{HL}= 0.1 s/0.2 s are significantly lower for V_G= 0 V compared to t_{HL}= 1 s/2 s in Figure 3.24 (left). This is because the low t_{HL} values are small in comparison to de-trapping time constants of the defined traps with an E_A= 0.5 eV leading to a smaller current response. AlGaN/GaN and buffer traps however induce lower R_{on} changes accompanying the t_{HL} increase from 0.1 s to 0.2 s, while the behavior of surface trap, barrier trap and reference curves is similar and smaller.

Variation of t_{LH}

t_{LH} controls the time available to trapped charges to dynamically respond to the applied V_D sweep and generate the steady-state I_D. Hence, this would be an important parameter controlling the trap-limited response.

Figure 3.26 presents the I_D-time and I_D-V_D response for t_{LH} sweep times of 0.5 s and 2 s.

In Figure 3.26 (left) the I_D transient versus time is presented, which includes the region of rise in V_D from V_D= 1 V to V_{Bias}= 15 V during 5 s to 5.5 s (t_{LH}= 0.5 s) or 5 s to 7 s (t_{LH}= 2 s).

In Figure 3.26 (right), the associated I_D-V_D calculated during the same time intervals is plotted. The R_{on} values extracted from the I_D-V_D (Figure 3.26 (right)) curves between V_D= 1 V and V_D= 2.5 V are presented in Figure 3.27 for t_{LH} values of 0.5 s, 1 s and 2ss.

Due to insufficient de-trapping at low t_{LH}, a vital portion of the trapped density fails to respond until higher $V_D \geq 8$ V (V_G= 0 V) explaining why a slight I_D overshoot is observed at high bias in Figure 3.26. Substantial R_{on} degradation is observed for all trap locations, proportional to the t_{LH} decrease while the absolute degradation is still higher for the AlGaN/GaN interface traps.

The AlGaN/GaN trap induced R_{on} worsening is the most aggravated by lower t_{LH}, especially when it is decreased from 1 s to 0.5 s for both V_G= 0 V and -2 V (Figure 3.27 (right)).

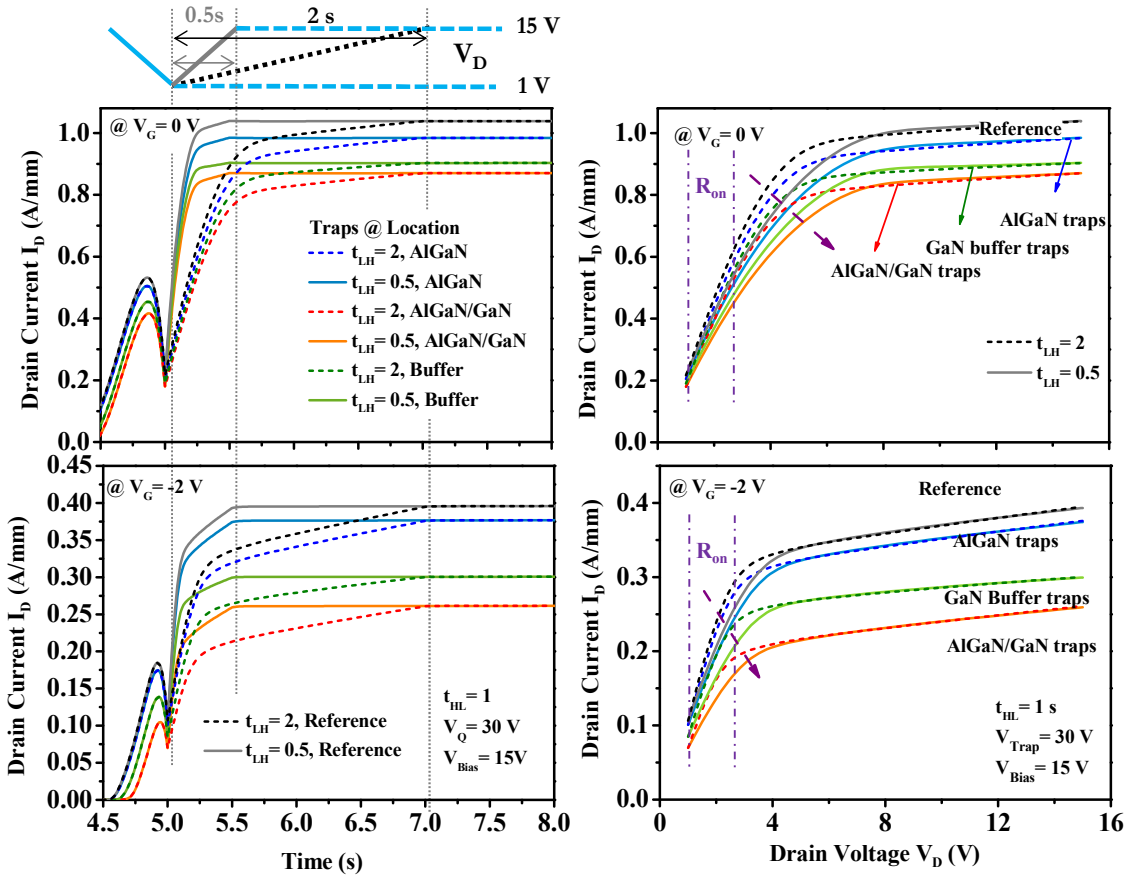


Figure 3.26: (left) I_D-V_D and I_D-time response for t_{LH}= 0.5 s, 1 s and 2 s at V_G= 0 V and -2 V

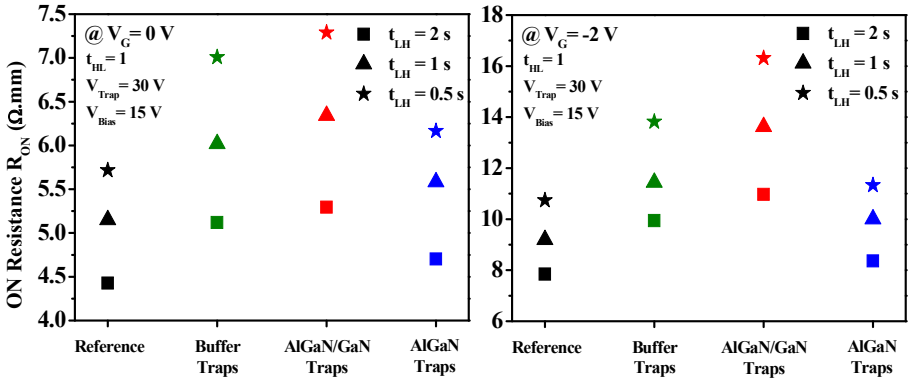


Figure 3.27: R_{on} extracted from Figure 3.26 (left) for t_{LH}= 0.5, 1 and 2 s at V_G=0 V and -2 V

The associated changes in buffer trap-induced response are moderate. The reference and AlGaN trap responses are similarly and least affected by t_{LH} variations in comparison.

For traps defined in the GaN buffer, Figure 3.28 depicts the change in E_C distribution along the Y-axis for t_{LH}= 0.5 s and 2 s for two identical bias states during each t_{LH} sweep. E_C is notably lower corresponding to the higher t_{LH} case, indicating higher I_D, especially around V_2=4 V, the bias region that reflects R_{on} variations.

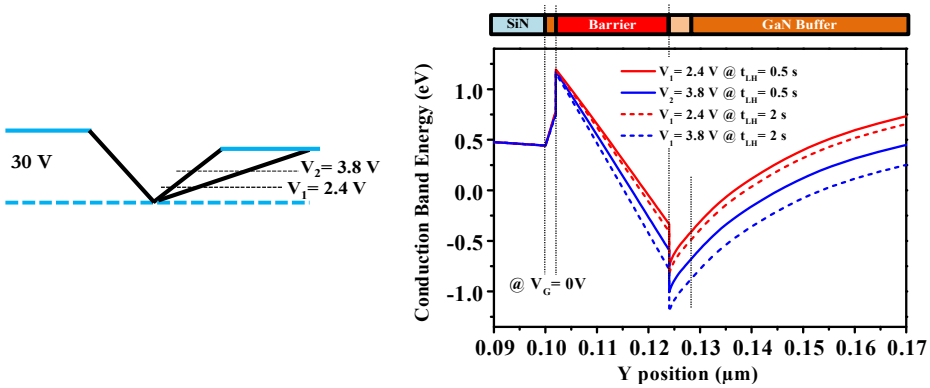


Figure 3.28: Conduction band energy distribution for t_{LH}= 0.5s and 2s for two time instants at identical voltage levels and V_G= 0 V

Variation of V_{Bias}

Finally, the endpoint of the I_D-V_D sweep is modified by changing V_{Bias} from 15 V to 10 V. V_{Trap} is kept low at 10V, and t_{HL}= t_{LH}= 1s. The I_D-time from 4.5 s to 7 s and I_D-V_D (calculated during 5 s to 6 s in Figure 3.18, as V_D rises from 1 V to V_{Bias}= 10/15 V) current responses are displayed in Figure 3.29 for V_G= 0 V and V_G= -2 V. For a low V_{Bias}, the requisite charge density to support the applied voltage is lower hence we see minor improvements in R_{on}. The corresponding changes at V_G= -2 V are observed to be analogous.

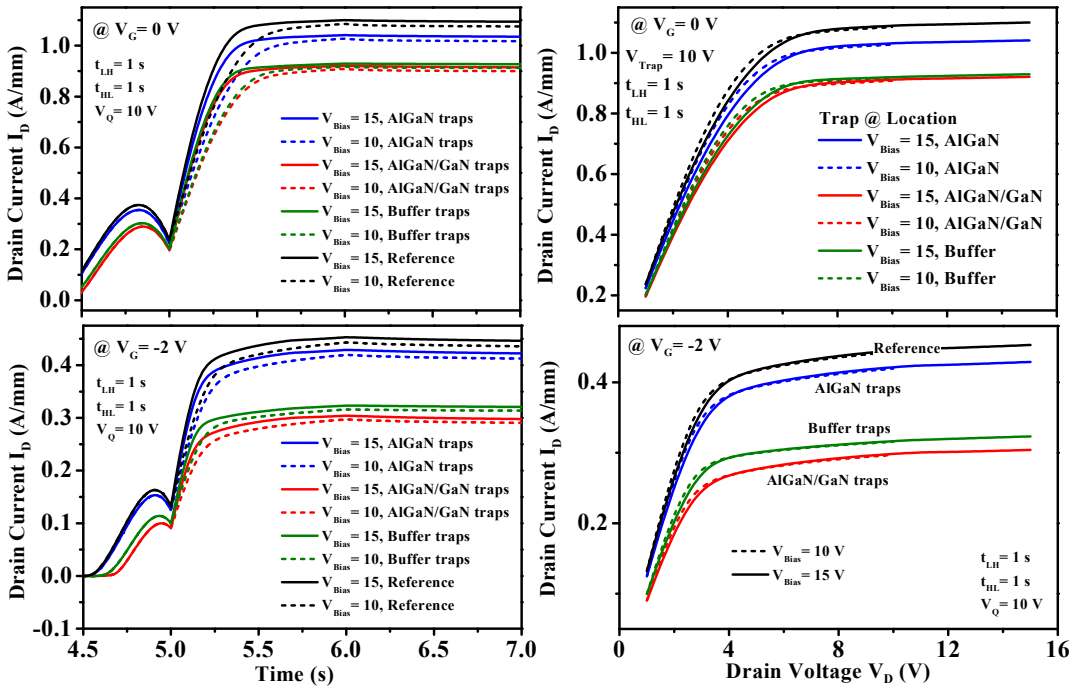


Figure 3.29: (left) I_D-time and (right) I_D-V_D response for V_{Bias}= 15 V and 10 V at V_G=0 V and -2 V.

This parameter seems to equally affect the different traps, and the degradations do not extend to significant changes in currents between V_D= 5 V and V_D= 10 V when both sets of curves

are superimposed. The lower levels of I_D at the end of the sweep caused by the lower end-point voltage are reflected better in the I_D-time characteristics.

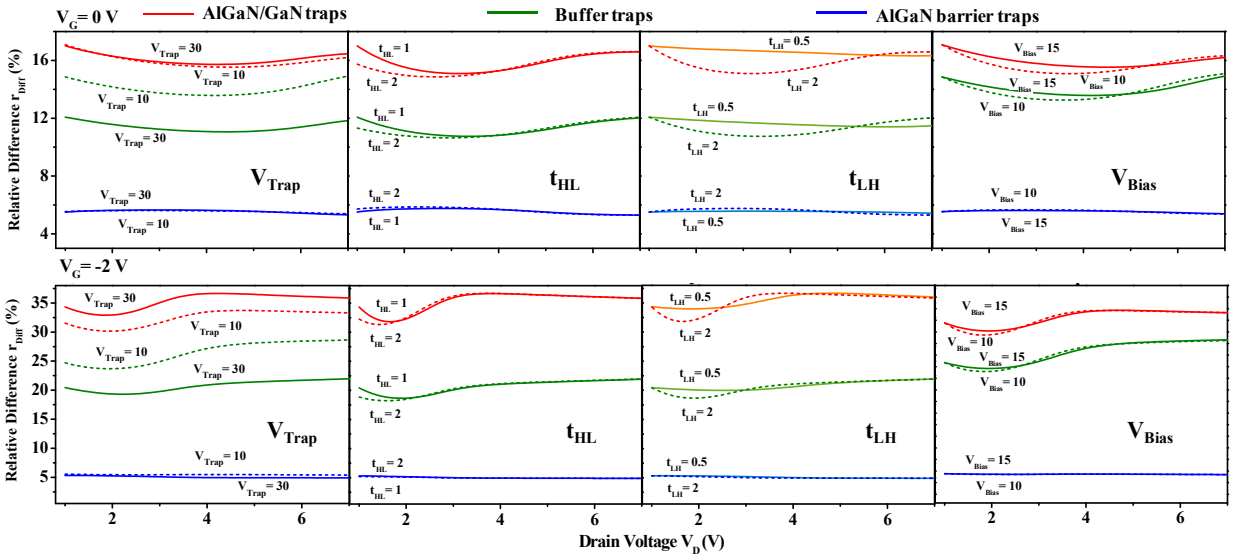
C. PULSE PARAMETER IMPACT ON TRAP EFFECTS

Since the changes in pulsing parameters also affect the reference state owing to its background traps, it is useful to obtain an idea into relative trap impact on the general response isolated from similar changes in the reference characteristic. Figure 3.30 ascertains the effects of V_{Trap}, t_{HL}, t_{LH} and V_{Bias} on traps compared to the reference for a part of the I_D-V_D sweep (V_D < 7 V) during t_{LH} by calculating r_{Diff} as:

$$r_{diff}(\%) = \left(I_{D,Ref} - I_{D,Trap}\right)/I_{D,Ref} \times 100 \tag{3.4}$$

As such, r_{Diff} represents the pulse parameter induced changes in trap impact. The associated table summarizes the effects of each pulse parameter on individual trap induced R_{on} or I_D degradations (relative to the reference) as high, moderate or low.

r_{Diff} is generally higher at V_G= -2 V closer to V_{th}. At V_G= 0 V, traps have a stronger impact at V_D < 2 V and V_D> 5 V. For V_G= -2 V, effects are higher for 3 V< V_D <5 V.



Trap	Density	Energy (eV)	Degradation of	V_{Trap} (V)	t_{HL} (s)	t_{LH} (s)	V_{Bias} (V)
AlGaN Barrier	10^{18} cm^{-3}	0.5 eV from E_C	R_{on}	Low	Low	Low	Low
			I_D	Low	Low	Low	Low
GaN Buffer	10^{18} cm^{-3}	0.5 eV from E_C	R_{on}	+ve (High)	Moderate	High	Moderate
			I_D	+ve (High)	Low	Low	Low
AlGaN/GaN heterointerface	10^{12} cm^{-2}	0.5 eV from E_C	R_{on}	High	Moderate	High	Moderate
			I_D	High	Low	Low	Low

Figure 3.30: Relative trap impact relative to the reference for variations in V_{Trap} (V), t_{HL} (s), t_{LH} (s) and V_{Bias} (V) for V_G= 0V and V_G= -2V along with table summarizing the effects

AlGaN barrier traps closely mirror changes in reference state due to parameter variations; thus associated r_{Diff} remains consistently low. For traps at AlGaN/GaN, a higher V_{Trap} worsens the disparity in both I_D and R_{on} strongly at low V_G. Buffer trap impact however appreciably weakens, indicating that a high OFF-state bias reduces its trapping contribution.

This is illustrated in Figure 3.31 comparing the trapped charge distribution for an X-cut extracted in the middle of t_{HL} for V_{Trap}= 10 V, 30 V.

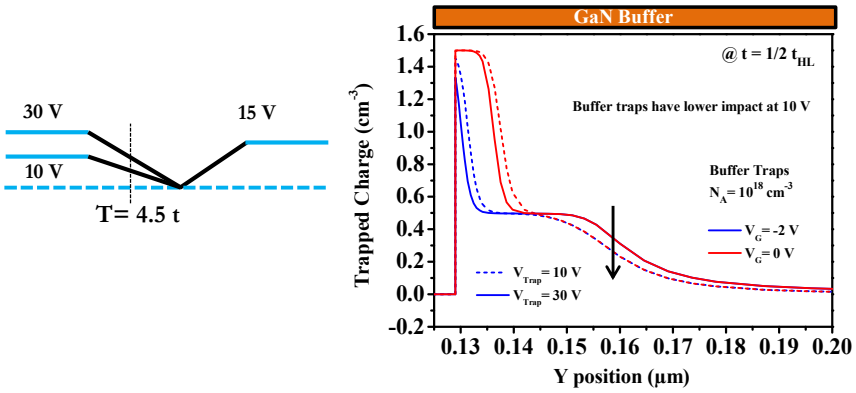


Figure 3.31: Distribution of trapped charge in the presence of buffer traps for a variation in V_{Trap}

It can be observed that while a lower V_{Trap} induces higher trap occupations just adjacent to the interface, average occupancy in the rest of the buffer region is reduced leading to better response. R_{on} ($V_D \leq 4$ V) degradations due to buffer or hetero-interface traps are generally mitigated by increasing t_{HL} especially at V_G= 0 V. Trap control on device response is strengthened at a lower t_{LH}, especially at V_G= 0 V. Due to a failure to de-trap, r_{Diff} nature is altered, with highest r_{Diff} at low V_D and linearly decreasing at high V_D. At V_G= -2 V, r_{Diff} increases with higher V_D. For a lower V_{Bias}, the comparative effect of both traps uniformly reduce for V_D< 5V.

AlGaN/GaN traps display highest divergence and maximal susceptibility to an aggravated response due to unfavorable pulsing conditions. The change in buffer trap responses due to pulse parameters is similar to those for AlGaN/GaN, but the effect magnitude is weaker. Insight into V_{Trap} and t_{LH} is important, which dominantly influence the trap-triggered switching response and thus define the maximal damage scenarios.

3.4 Conclusions and Perspectives

The methods to use transient simulations to understand trap-controlled devices responses to bias transitions have been described.

In the absence of suitable wide devices for performing C-V measurements, the availability of a representative TCAD model allows detailed discussion into comparison and correlation of existing

hypotheses specific to trap locations to obtain a deeper understanding of the critical factors that drive trap-induced degradations under specific bias or f conditions. The C_g characteristic is extremely sensitive to small changes in charge distributions and such presents a valuable technique to predict the presence or quantify the impact of phenomena that might not be otherwise be observable in other characteristics or simply unrecognizable due to suppression by predominant factors. Finally, this analysis can be a diagnostic tool to directly interpret channel density or space charge region transitions and validate trap-related information extracted from C_g measurements.

Careful optimization of the on-resistance is crucial for low voltage RF applications. The discussion into trap-induced changes in R_{on} following an off-on transition enables an understanding into which pulsing conditions cause certain kinds or locations of trapping phenomena to gain higher significance. Expectedly, AlGaN/GaN traps were observed to clearly cause the highest degradation, especially when the defined pulse parameters are restrictive. The most relevant pulse parameters are the trap filling voltage and the time allowed for the traps to respond to a rising bias, just after subjecting the device to an off-on transition.

In both the C_g-V and R_{on} approaches to understand trap behavior, the device is subjected to transient analyses that drive the device from a high trapping state or off state to a state favorable to detrapping, i.e. as the device turns on. Hence, both these characteristics reflect the individual trap induced limitations on the switching performance of the device. While the C-V characteristics in Section 3.2 take a closer look at charge modulations during the off-on transition itself alongside frequency effects, the R_{on} section in 3.3 investigates not only the transition, but the effects of pulsing parameters that precede, define and follow this off-on transition to offer a larger viewpoint of how the trapped charges respond surrounding a switching instance.

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CHAPTER 4

Investigation into "Belly Shape" Degradation

CAUSAL MECHANISMS AND AGING EFFECTS

4.1 Introduction

Gate leakage mechanisms are actively researched in reliability investigations of GaN based HEMTs. They are subject to various effects and constraints, such as discussed in Chapter 2, that are often difficult to interpret, and are aggravated by high electric fields and stress conditions. Several works have explored high electric field activated processes of degradation such as surface pitting [4.1- 4.3], the formation and distribution of epitaxial traps [4.4- 4.8], trap-assisted tunneling mechanisms [4.9- 4.10], and the inverse piezoelectric effect [4.8, 4.11]. Some works [4.12- 4.14] reported on an atypical parasitic leakage phenomenon observed in Schottky GaN HEMTs, and importantly in the UMS GH-25 technology, after aging tests. The effect is characterized by a strong parasitic surge in forward gate current for $V_G < 1$ V, resulting in a "belly-shape" [4.13] (BS) like characteristic of arbitrary magnitude.

Despite considerable analysis, primarily indicative of surface leakage [4.13-4.15], a complete description of its causation or trigger factors is yet to be achieved. Further, observed irregularities in BS magnitudes and the erratic, unpredictable evolution of the gate current during the aging process make it an interesting case study. These issues merit further research. Although BS has not been associated with adverse impacts on device lifetime, insight into its origin is essential to recognize the interactions among critical mechanisms linked to Schottky gate degradation and leakage performance under stress-induced high electric field conditions. This work investigates fundamental mechanisms governing this anomaly, based on a comprehensive study of electrical characterization, TCAD

simulation and review of previous analyses. Each approach attempts to identify and understand mechanisms that play a role in the belly shape effect.

Basics of Aging Tests

For reliability or lifetime performance predictions, accelerated life tests provide a realistic evaluation of the impact of defects or degradation mechanisms under normal or stressed operational conditions within a controlled environment. The test conditions must be carefully chosen to aggravate the bias or heat conditions that would accelerate the appearance and escalation of existing degradations, while ensuring that new failure mechanisms are not introduced. In order to minimize the design to product qualification times, this is an essential step to activate or analyze possible failure modes of devices and estimate their applicability to long term or high-stress requirements. For GaN HEMTs, this is especially significant since its applications involve high levels of robustness such as for automobiles and high temperature and time stability such as for space applications.

The devices under study were provided by UMS who performed HTOL tests in the first stage of investigation into the device set. HTRB aging was carried out in the course of this study as well. These two kinds of aging tests relevant to this study are briefly described as follows:

High Temperature Operating Life (HTOL) Tests: This kind of test involves medium electrical stress at low levels of I_{DS} and intermediate V_D biases, at high temperatures (~ 250°C - 300°C) over long time periods (~100s of hours) to accelerate the physical degradations or induce failure. They can activate wear-out mechanisms due to steady long term application of stress. In short durations, "burn-in" tests with similar conditions are employed to detect early failures or enable a stable and reproducible electrical state before further tests.

High Temperature Reverse Bias (HTRB) Tests: For a targeted study into the durability of the Schottky contact, this kind of test subjects the device to a deep reverse bias ($V_{Test} < V_{th}$) and high V_D bias for long durations under medium to high temperatures. Since the channel is pinched off, the channel temperature is close to applied temperatures. These tests are important in analyzing high electric field induced leakage or defect mechanisms.

A. BS FUNDAMENTALS AND ANALYSIS APPROACH

"BS" Gate Characteristic

The belly-shape effect is defined as the appearance of a high forward gate leakage that occurs after devices are subjected to aging tests. Figure 4.1 (a) shows a typical example of a device displaying the Belly shape effect compared to unaged reference device of the same device set. BS can be

identified in the swell or ballooning of I_G for low to medium gate bias ($V_G \leq 0.8$ V). This kind of gate feature, 5 or 6 orders higher than expected, presents a striking contrast compared to the reference characteristic. |BS| represents the magnitude of the associated leakage growth. At high bias ($V_G >$ 0.8V) the BS current usually declines; and $I_{G,f}$ falls slightly lower than the reference.

In a given set of aged devices, the belly shape appears in most but not all of the devices. In some devices, no belly shape is observed and a decrease in absolute $I_{G,f}$ is induced. This is referred to as the No-BS characteristic as presented in Figure 4.1 (b). In this case, the inherent nature of the $I_{G,f}$ curve remains unaltered.

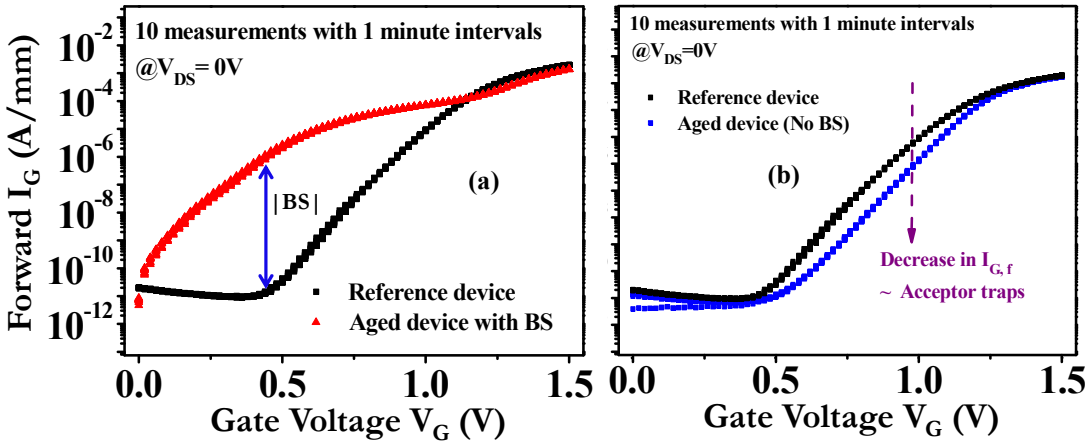


Figure 4.1: (a) A measured Belly-Shape aged characteristic and (b) a measured No-BS aged characteristic in comparison to a reference unaged device

Flow of Analysis

The complete analysis approach for investigation into the belly-shape nature is illustrated in Figure 4.2 which will be discussed chronologically in following sections. The devices under study are UMS devices from the GH-25 device process technology. A given set of 12 devices were subjected to HTOL testing for 7000 hours and a second set of 10 devices were subjected to HTRB testing for 4000 hours in 2014 [4.13]. Reference devices from each set were kept unaged for comparison. Majority of devices from both these sets were observed to display the belly shape effect after aging.

Following analyses was carried out for both these sets which provided information into the appearance and behavior of BS. For the HTRB set, electroluminescence tests were also performed [4.15]. A review of all these observations comprised the first step of this work. Experimental data about the long term effect of BS was however missing. Since the HTRB set was subjected to destructive testing, a re-characterization of the first set of HTOL-aged devices was carried out after 3 years of inactivity to examine recoverability of BS. However, even with all experimental data combined, only speculative hypotheses could be made about the mechanisms responsible for BS.

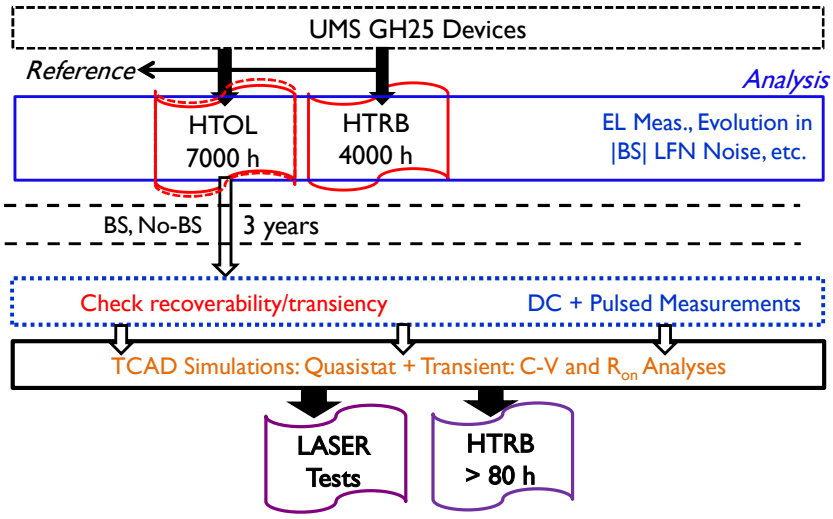


Figure 4.2: Schematic flow of analysis into Belly shape effect.

To validate the assumptions, TCAD device modeling was performed to reproduce the behavior of the aged devices and the circumstances that could induce BS and No-BS characteristics.

In the second phase of analysis, AC transient simulations were performed to obtain further insight into how BS affects device performance. With the new understanding into its causation, the studied device set was split into two for the next steps of the investigation. One half of the devices were studied through laser techniques in an attempt to visualize trap contributions to BS. Then, BS effects on sustained reliability were assessed by subjecting the other half of devices to a second round of aging, but in HTRB mode, for more than 80 hours.

B. REVIEW AND POSSIBLE CAUSAL MECHANISMS OF BS

To review the information that can be inferred about BS based on previous works, Figure 4.3 describes how the presence of certain mechanisms can be linked to BS from different observations.

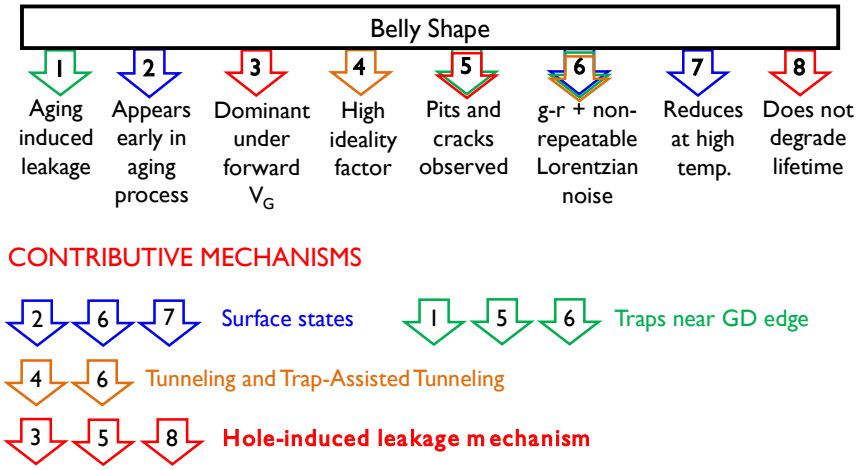


Figure 4.3: Possible mechanisms that could contribute to BS based on observations

Firstly, BS can be associated with surface states since it starts appearing quite early in the aging process [13], within a couple of hours. It can also be linked to trapping-detrapping mechanisms around the gate since BS devices have been associated with high components of generation-recombination noise [4.14]. Further, BS magnitudes have been observed to decrease at high temperatures up to 100 ^{0}C [4.15] which could correspond to de-trapping of shallow surface states.

BS manifests in the devices only after they have been subjected to aging tests. Since aging primarily affects the area surrounding the drain side of the gate edge where the maximum electric field induced stress develops, the traps or defects that would be associated with the appearance of BS could also be assumed to be concentrated around the gate edge.

BS has also been correlated to a high ideality factor (η >2) [4.15], often indicative of the presence of trap assisted tunneling mechanisms. Hence, the role of tunneling and traps coupled to tunneling need to be considered.

Since Ando et al. in [4.12] observed a suppression of BS on devices having an improved epi-layer, the 'No-BS' behaviour could be linked to better surface quality. Then, BS could arise from localized non-uniformities near the surface, due to small inconsistencies in initial fabrication processes, which are activated by aging. However, despite the surface degradation and leakage, BS does not significantly degrade threshold voltage V_{th}, output power or aggravate long-term reliability. In fact, electron redistribution tests [4.15] failed to reduce the BS magnitudes, thus indicating a lack of electron trapping accompanying BS instances.

Hence, based on all these observations, we propose that BS is primarily a hole-induced leakage mechanism involving donor-like surface states at the metal/semiconductor interfaces, presumably near the gate-drain edge. Moreover, this would explain why the BS effect is dominant under forward V_G conditions, and the corresponding impact during active device operation (V_D > 0 V) is minor in comparison.

4.2 Characterization after 3 years of storage

There were two motivations to perform a characterization of the HTOL aged devices after 3 years of storage at room temperature. The first was to verify whether the BS effect is recoverable, in which case the responsible traps would have all been de-trapped in the storage period. The second was to capture the random variability in BS magnitudes. Hence, measurements were repeated 10 times with 1 minute intervals.

Figure 4.4 presents the $I_{G,f}$ measurements for three BS devices compared to the reference for 10 consecutive characterizations in 1 minute intervals.

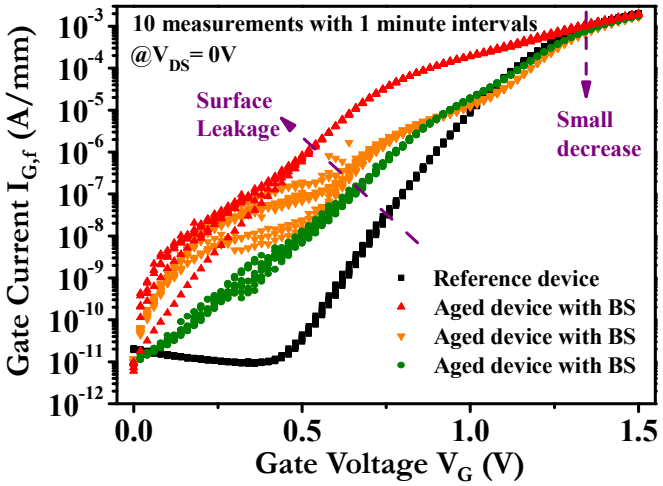


Figure 4.4: Forward gate current characteristics for 3 BS devices after 3 years of storage

The curves display noticeable deviation in |BS| magnitudes, especially at low V_G conditions. Fluctuations between different devices and within such short intervals of time, suggests the role of transitional mechanisms in producing BS-like features. We have previously discussed that the presence of surface trap states can be assumed accompanying BS. This, along with correlation of transient mechanisms with BS curves leads us to propose the influence of shallow donor-like states near the gate-drain edge as a contributing mechanism.

Figure 4.5 presents the $I_{G,f}$ comparison of 4 BS devices before and after the storage period.

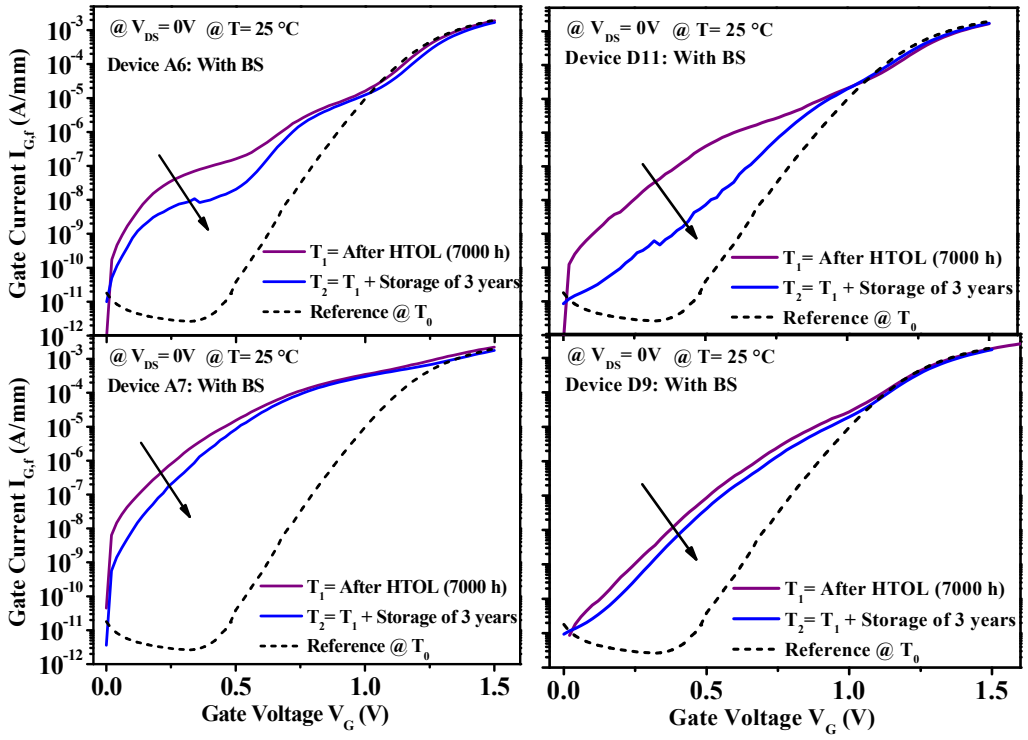


Figure 4.5: Forward gate current characteristic for 4 BS devices before and after storage

An important observation here is that all of the devices that previously displayed the BS nature, following an aging process, were still found to display substantial BS magnitudes. Hence, it could be asserted that the BS is an enduring effect and not fully recoverable, and thus probably linked with permanent device degradation. However, a general reduction in |BS| indicates some amount of restoration in the underlying mechanisms, resulting in a less severe BS occurrence. The decrease is observed to be significant for some of the devices while quite trivial in others.

Hence, an attempt to better understand the effects of storage on BS needs to be pursued. This would of course be inherently linked to the nature of the responsible degradation mechanisms, variations in which induce the shifts in observed BS curves. Hence, this discussion will be continued later once the principle mechanisms have been identified in the following sections.

No-BS or un-aged reference device natures remain essentially unaltered after the storage interval, in contrast to the BS devices, as can be observed from Figure 4.6. Only a weak reduction in I_G is observed at low V_G for the No-BS device which could indicate small de-trappings. However, it could also simply be a consequence of dispersion or measurement setup dissimilarities.

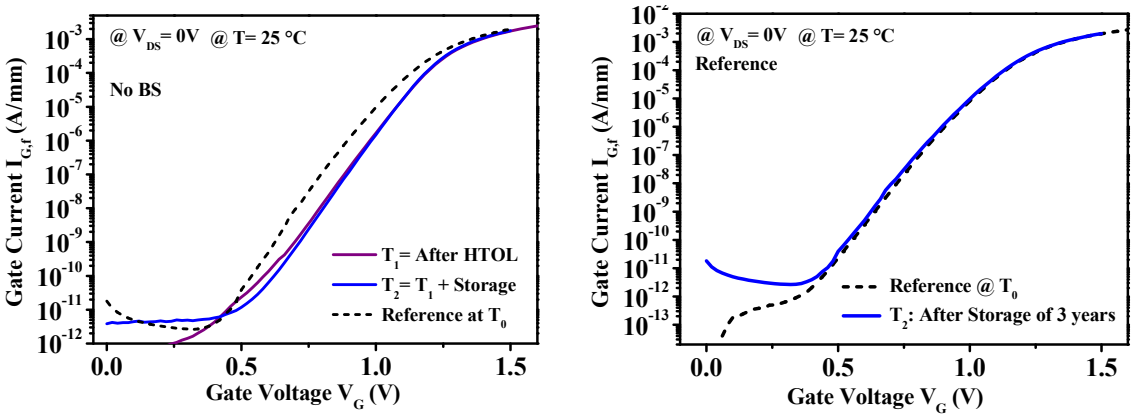


Figure 4.6: Effect of storage on No-BS and reference devices

4.3 Simulation of the Belly Shape Effect

The hypotheses developed from the discussion into experimental observations form the basis of the TCAD simulations to reproduce and understand the BS effect. A reference $I_{G,f}$ characteristic is simulated on the complete device structure presented in Chapter 3 to closely resemble the non-aged device states in [4.13- 4.14].

A. SURFACE DONORS

Donor traps, which we shall refer to as D_t were introduced at the top surface (SiN passivation/GaN cap interface) of the reference model. Since aging tests have been found to

primarily generate defect sites near the high electric field gate-drain edge region [4.8, 4.13 and 4.17], D_t is activated within a length L_{ext} extending from the gate-drain edge (see Figure 4.7 (left)). Figure 4.7 (right) demonstrates the change in electric field and current density distributions caused in the presence of D_t for a X-cutline C in the GaN cap at V_G= 0.8 V.

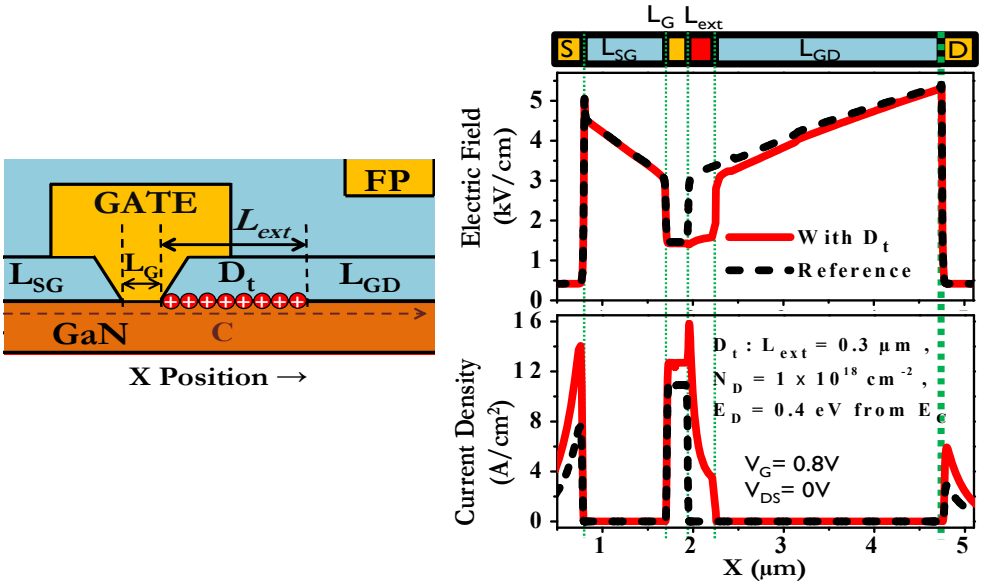


Figure 4.7: (Left) Schematic of surface donor traps D_t defined at the SiN passivation/GaN cap interface within a length L_{ext} from the gate-drain edge and (Right) comparison of the electric field and current density distributions with and without D_t at V_G= 0.8V for the cutline C.

Under forward V_G, holes are introduced in the device. Due to the associated increase in donor trap occupancy, a localized positive charge develops, prompting a lowering in the electric field near the gate edge [4.18]. It remains low within L_{ext} as the peak of the electric field shifts from the gate edge to the right of L_{ext}. The associated spike of current at the drain side of the gate edge, which then spreads further in the L_{ext} region, is essentially the origin of the surface leakage triggering the peculiar growth of $I_{G,f}$ which manifests as the BS-like characteristic. The increase in surface donors also causes a current rise adjacent to the source and drain.

Figure 4.8 investigates the impact of variation in the simulated D_t parameters: L_{ext}, trap concentration (N_D) and trap energy (E_D) respectively on $I_{G,f}$. It is evident that the rise in $I_{G,f}$ caused due to D_t bears a definite resemblance to the BS characteristic.

The curves noticeably diverge at low V_G and merge with the reference beyond V_G > 1V. The variation of L_{ext} from 0.2 to 0.4 µm (Figure 4.8 (a)) causes only a small $I_{G,f}$ rise, indicating that BS inducing donor traps are dominant in a very small area in the gate-drain region. This observation could be strongly linked to creation of dislocations close to the gate edge due to the high electric field accompanying the aging tests, which then act as trapping sites for holes.

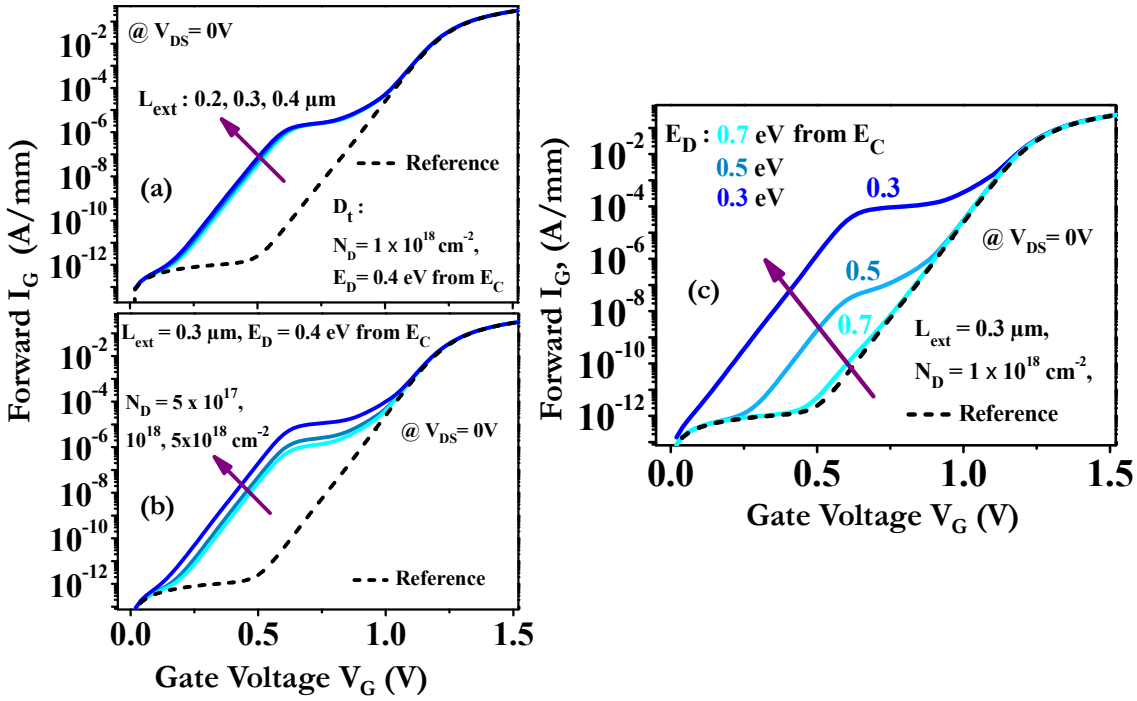


Figure 4.8: Simulated forward I_G-V_G characteristics for variation in (a) L_{ext} (b) Concentration N_A and (c) energy position E_A of surface donor traps D_t.

While a higher N_D supports a slightly higher BS as shown in Figure 4.8 (b), the critical parameter which controls the appearance and strength of BS is found to be E_D (Figure 4.8 (c)). In [4.10] and [4.19], surface states with shallow energy levels ~ 0.2 eV and 0.3 eV have been associated with gate leakage, while [4.20] considered a donor trap level close to 0.4 eV.

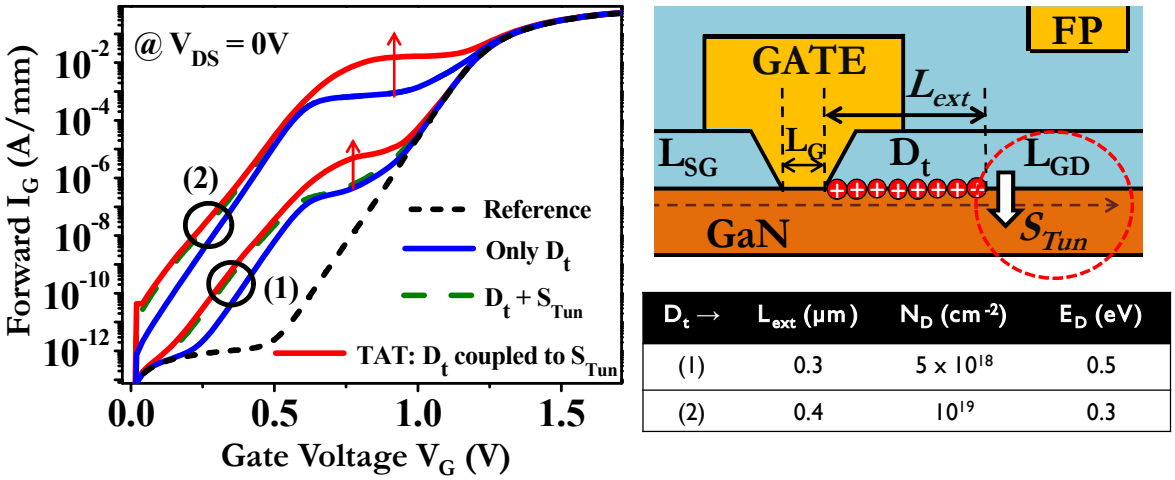
A threshold donor trap energy E_D of 0.7 eV from E_C can be identified, beyond which the BS effect is found to be trivial. The influence of deeper traps appears at medium V_{GS} (> 0.5 V) conditions where they cause an earlier onset of the $I_{G,f}$ slope, while traps with lower E_D, with the highest occupation probability are responsible for the ballooning of the $I_{G,f}$ curve, even under very low V_G. High BS magnitudes such as the cases in Figure 4.1 or Figure 4.4 can hence be observed only in the presence of shallow traps. Although deep traps might contribute, a definite amount of shallow surface traps are essentially requisite for a significant BS. Strong deviation from reference $I_{G,f}$ at low V_G biases can hence be attributed to shallow D_t traps located in proximity to the gate edge.

Simulation of Trap-assisted Tunneling

The Non-Local (NL) tunneling model in Sentaurus that simulates tunneling effects has been described in Chapter 2. A specialized NL mesh establishes tunneling paths as a function of two model parameters: tunneling length $L_{Tun,}$ and a second quantity defined as the permeation p. To achieve tunneling between vertices on different sides of an interface, the connections are extended

by the defined p beyond the interface boundary. TAT is activated by coupling defined traps to NL tunneling at adjacent interfaces, as a combination of inelastic, phonon-assisted and elastic processes [4.16]. Tunneling paths are defined between trap vertices and each coupled interface through individual NL meshes. Band to band tunneling is activated by tuning simulation parameters of TAT.

We investigate the interplay of D_t with the presence of tunneling across the GaN cap/AlGaN barrier interface, henceforth referred as the surface tunneling component S_{Tun} in Figure 4.9.



$D_t \rightarrow$	L_{ext} (µm)	N_D (cm^{-2})	E_D (eV)
(1)	0.3	5×10^{18}	0.5
(2)	0.4	10^{19}	0.3

Figure 4.9: Effect of introducing tunneling at the GaN cap/AlGaN barrier interface (S_{Tun}) in addition to donor traps D_t, and coupled to D_t, with two kinds of surface trap specifications.

Two D_t specifications produce $I_{G,f}$ curves with medium (D_{t1}, N_{D1}, E_{D1}) and high (D_{t2}, N_{D2}, E_{D2}) BS magnitudes. First, we activate S_{Tun} (L_{Tun}= 3nm, p= 2nm) in addition to D_t, and then, couple the defined D_t to S_{Tun} to activate TAT. While S_{Tun} itself strengthens BS slightly at V_G<0.8 V, TAT further prolongs the presence of BS in the gate characteristic to a higher bias. With TAT, the simulated curve closely resembles measured curves such as (1) in Figure 4.1 (a).

B. ALGAN BARRIER TRAPS

Surface donor traps are the dominant cause of BS at low to medium V_G, regions governed by thermionic emission. As observed, the simulated BS due to D_t merges with the reference at high V_G. For V_G> 1V, $I_{G,f}$ is generally controlled by the series resistance, and effect of D_t is marginal as trap occupancy declines. In the presence of acceptor traps however, the current for V_G >1V is susceptible to change. Based on the pits and cracks revealed by EL tests [4.13] in BS and No-BS devices near the gate-drain edge possibly corroborated with the inverse piezoelectric effect (IPE), acceptor traps in the barrier due to defects associated with aging induced strain relaxations need to be considered. Thus, even if not a direct cause to BS, the presence of electron traps in both BS and No-BS devices after aging cannot be disregarded in the simulations.

Generally, high density traps within the barrier might severely reduce $I_{G,f}$ or I_D, dominating the device response. However, aging-induced trap activity, especially formed due to barrier relaxation would be localized (as for D_t), near the gate edge, with the highest electric field.

Hence, A_t is defined as a uniform concentration (N_A) of acceptor traps in the AlGaN barrier localized within a length $L_{ext,A}$ = 2µm around the gate edge as illustrated in Figure 4.10 (right).

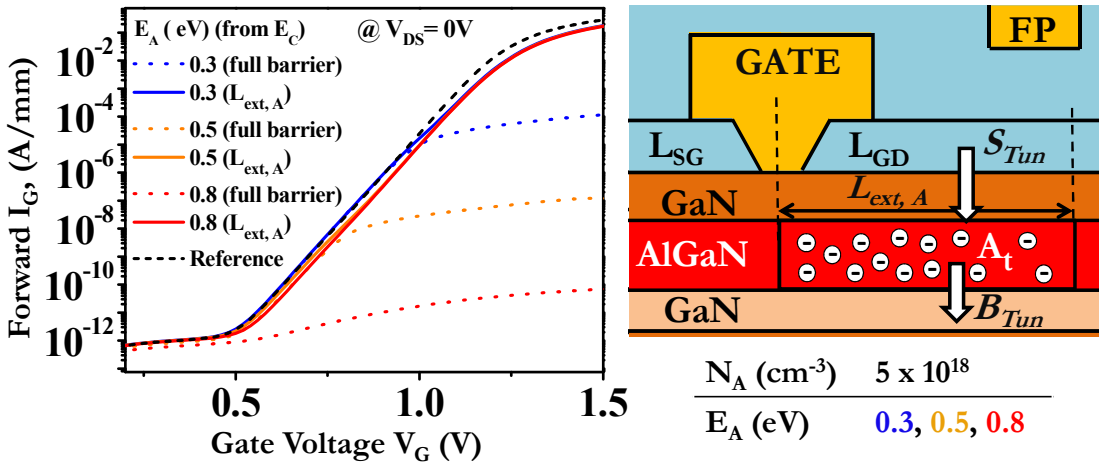


Figure 4.10: Schematic presenting definition of acceptor traps A_t in the AlGaN barrier for a length $L_{ext,A}$ around the gate-drain edge (b) simulated forward I_G-V_G characteristics for varying energy positions of A_t.

The consequence of defining traps in $L_{ext,A}$ instead of the entire AlGaN barrier is illustrated in Figure 4.10 (left) for N_A= 5x10^{18} cm^{-3} and different trap energy positions (E_A= 0.3, 0.5 and 0.8 eV) typically reported for GaN HEMTs [4.4-4.8]. Activation energies of 0.48 eV and 0.66 eV have been previously identified in [4.7] for UMS devices. Traps in the full barrier are found to cause huge reductions in $I_{G,f}$. The drop is stronger for traps energetically further from E_C. However, restricting A_t within $L_{ext,A}$ moderates the impact on $I_{G,f}$. Shallow acceptors cause a lowering in $I_{G,f}$ at high V_G bias beyond 0.8 V. Deeper acceptor traps, however, effect an overall decrease of $I_{G,f}$ compared to the reference, emulating the behavior of the No-BS devices in Figure 4.1 (b).

Effect of Trap Assisted Tunneling and Barrier Lowering

In addition to the tunneling across the surface (S_{Tun}), an additional tunneling component can be introduced across the barrier/channel interface B_{Tun} (L_{Tun}= 4nm, p= 3nm). In combination, these tunneling components activate a leakage path from the gate until the channel. Barrier height irregularities often accompany surface degradation in devices [4.21-4.22], which lead to I_G variations. Since the BS occurrence is a consequence of aging-induced surface deterioration, we study the effects of Schottky barrier lowering $\Delta\varphi$ on the simulated BS characteristic.

For the same A_t parameter values, $I_{G,f}$ can approach BS-like behavior when combined with trap assisted tunneling as presented in Figure 4.11(left) for E_{A1}= 0.3 eV and E_{A2}= 0.5 eV. As observed previously for D_t, here again, activating TAT by coupling A_t to S_{Tun} and B_{Tun} slightly enhances $I_{G,f}$. The characteristic fall in $I_{G,f}$ beyond V_G=1 V, lower than the reference as observed in measured BS, is now also discernible in the simulated curves. Thus, shallower A_t (0.3-0.5eV), when reinforced with tunneling, can directly resemble $I_{G,f}$ measurements with small |BS|.

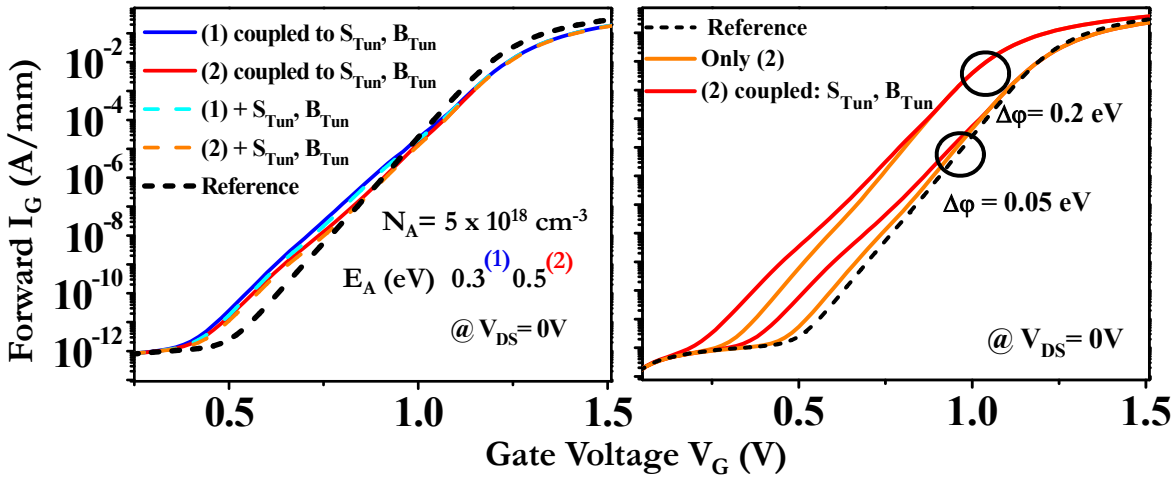


Figure 4.11: (left) Effect of (left) tunneling components S_{Tun}, at the surface and B_{Tun} at barrier/ channel interface and (right) barrier lowering, when coupled to acceptor traps A_t in a section of the AlGaN barrier around the gate–drain edge ($L_{ext,A}$), on forward I_G-V_G characteristics for varying E_A.

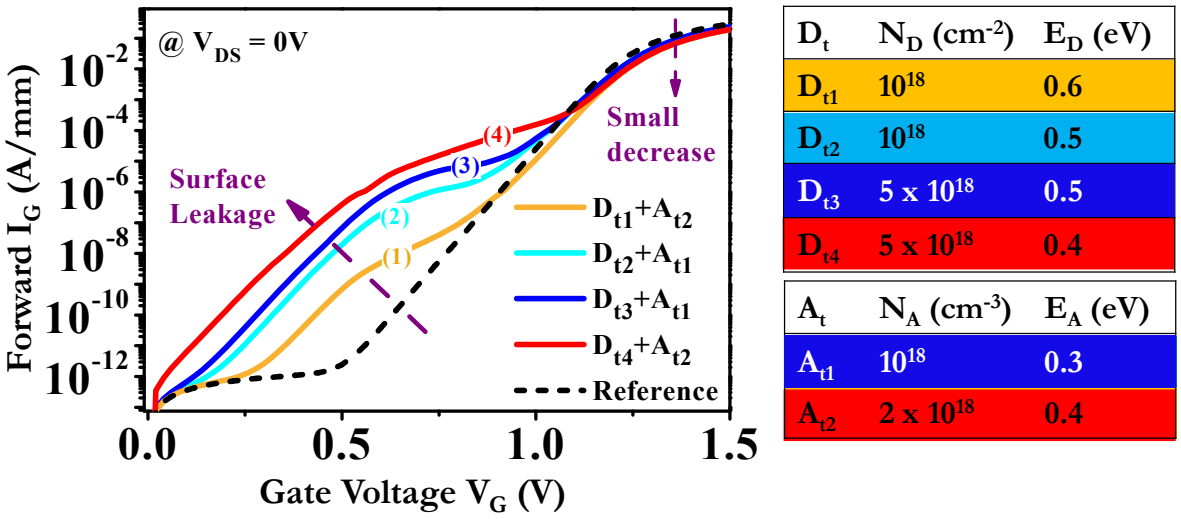
However, as observed, aged devices display significantly stronger BS than obtained with just A_t traps coupled to TAT. Figure 4.11(right) describes the impact on $I_{G,f}$, with A_t when the barrier height is lowered by $\Delta\varphi$ = 0.05 and 0.2 eV.

By defining a higher $\Delta\varphi$, deviation from the reference can start earlier and BS magnitudes are distinctly larger, even beyond V_G= 1 V. This attests to the role of barrier height degradations in the triggering of BS leakage in $I_{G,f}$ of aged devices.

C. MODELING THE "BS" CHARACTERISTIC

The above discussion identifies principal trapping mechanisms driving the belly shape effect: donor traps at the SiN/GaN cap interface (simulated as D_t) causing growth in $I_{G,f}$ for V_G< 0.8 V and acceptor traps in the AlGaN barrier (simulated as A_t) effecting a reduction in $I_{G,f}$ at high forward V_G. TAT plays an important role in coupling these traps with tunneling components (S_{Tun} and B_{Tun}) to trigger leakage current flow across the gate to channel.

Figure 4.12 simulates $I_{G,f}$ as a function of D_t coupled to S_{Tun}, and A_t coupled to S_{Tun} and B_{Tun}, for a set of D_t and A_t definitions.



D_t	N_D (cm^{-2})	E_D (eV)
D_{t1}	10^{18}	0.6
D_{t2}	10^{18}	0.5
D_{t3}	5 x 10^{18}	0.5
D_{t4}	5 x 10^{18}	0.4

A_t	N_A (cm^{-3})	E_A (eV)
A_{t1}	10^{18}	0.3
A_{t2}	2 x 10^{18}	0.4

Figure 4.12: Simulated forward I_G-V_G characteristics to represent four BS cases as a conjunction of surface donor traps D_t (coupled to S_{Tun}) and acceptor traps in the barrier A_t (coupled to S_{Tun} + B_{Tun}).

The distinctive BS is recognizable and conforms to the measured shape. At low to medium V_G, D_t-activated leakage dominates and $I_{G,f}$ is high, which also represents the reduction in barrier height [4.8, 4.20]. This obviates the need to explicitly define a $\Delta\varphi$ to simulate high BS values. Curves (2) and (3) have the same A_{t1}, hence they merge beyond V_G> 1 V, slightly below the reference. Since (3) has a higher N_D (N_{D3}>N_{D2}) but the same E_D= 0.5 eV, the associated BS is only a little greater. Curves (1) and (4) have stronger A_t (higher N_A, deeper E_A) than (2) and (3), and hence a deeper decline than (2) and (3) for V_G>1V. However, the BS magnitude for (4) is notably higher owing to the D_t definition with higher N_D (N_{D4}> N_{D1}) and shallower E_D (E_{D4}=0.4eV, E_{D1}= 0.6eV).

Figure 4.13 visualizes the (a) electric field and (b) current distribution of a representative BS simulation (D_t and A_t: $N_{D,A}$= $10^{18}cm^{-3}$, $E_{D,A}$= 0.4 eV, L_{ext}= 0.3µm) compared with the reference, close to the gate-drain edge at V_G= 0.8 V.

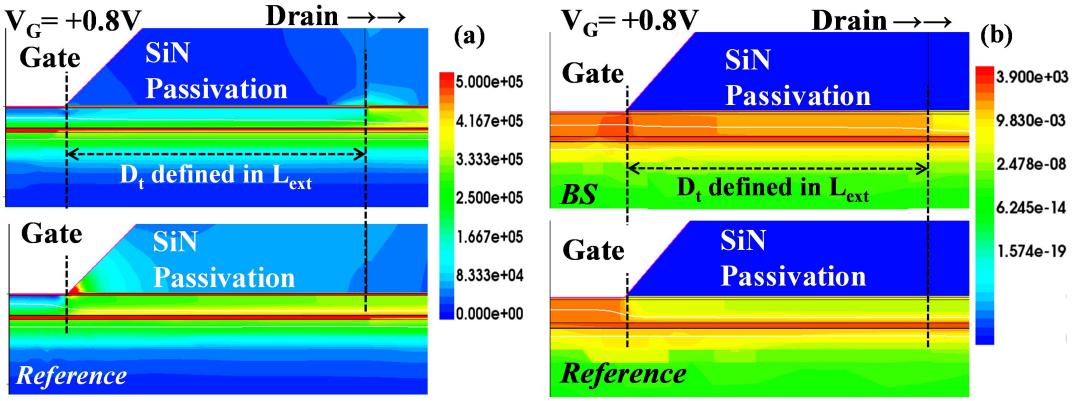
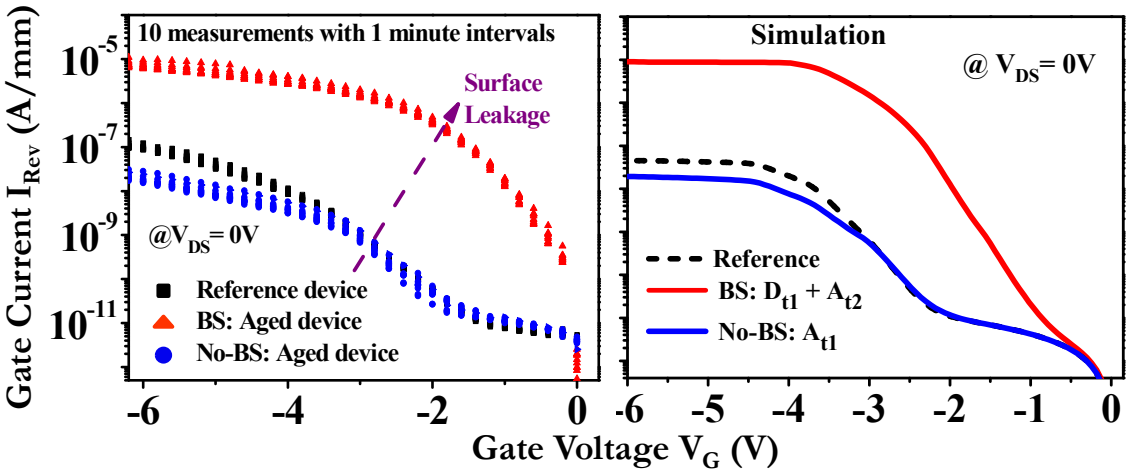


Figure 4.13: Comparison of the simulated (a) electric field and (b) current density distribution (A/cm²) at V_G= 0.8 V for BS and reference case.

The lowering in the electric field peak in the region surrounding the gate edge, in the presence of donor traps, is observable from the color map. In comparison to the reference, BS-linked current densities in the cap and barrier layers below the gate drain passivation are appreciably higher within L_{ext}. This leakage is reflected in the forward gate characteristic as the BS effect.

Reverse Gate Leakage and Output Currents

To substantiate the described hypotheses and corroborate the trap parameters, reverse bias simulations for the reference, No-BS and BS scenarios are illustrated in Figure 4.14.



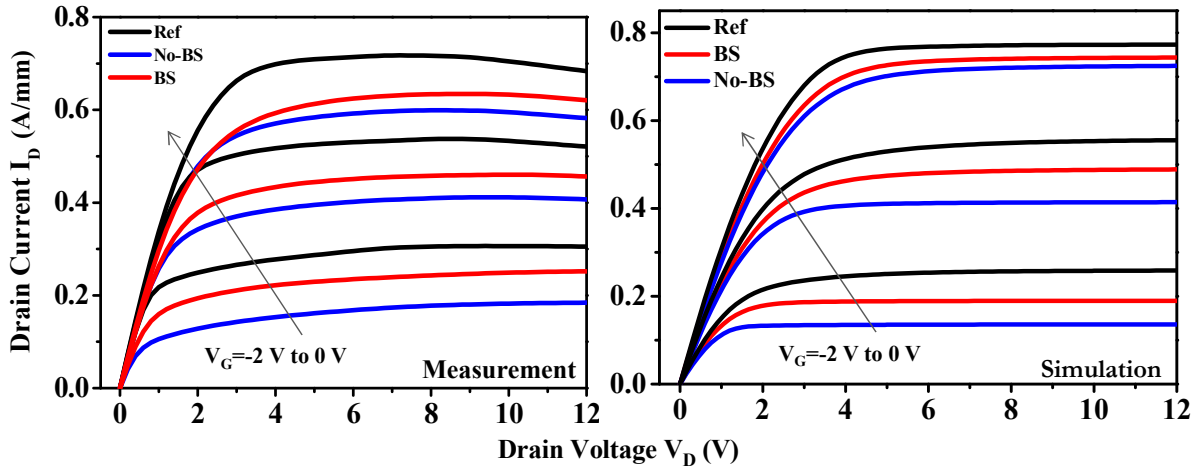
D_t	N_D (cm^{-2})	E_D (eV)	A_t	N_A (cm^{-3})	E_A (eV)
D_{t1}	5 x 10^{17}	0.35	$A_{t1, t2}$	5, 2 x 10^{18}	0.7, 0.4

Figure 4.14: Measured and simulated reverse bias characteristics for reference, BS and No-BS cases

The No-BS curve is simulated with deep (E_A= 0.7 eV) A_t traps coupled to S_{Tun} and B_{Tun} while the BS case has shallower A_t (E_A= 0.4 eV) traps and D_t traps with N_D=1×$10^{18}$$cm^{-3}$ and E_D= 0.4 eV. They are compared to the reverse bias gate characteristics (I_{Rev}) of a reference device and aged devices with and without BS. Here too, I_{Rev} is several orders higher for BS devices, however, the inherent characteristic appears less divergent. For No-BS devices, current levels begin to deviate close to V_G=-3 to -4 V which could be attributed to the presence of acceptor traps, in accordance with our previous inferences.

Output characteristics are also compared to simulations in Figure 4.15 while retaining the simulation parameter values that have been chosen for our discussion so far.

For both BS and No-BS cases, we observe a decrease in I_D. The fall is stronger in the No-BS case due to the deep acceptors. Hence, donor traps present in conjunction with other BS inducing factors, in addition to increasing gate leakage, are recognized to normally contribute to a lowering of output currents.



BS: D_t + A_{t2}	D_t	N_D (cm^{-2})	E_D (eV)	A_t	N_A (cm^{-3})	E_A (eV)
No-BS: A_{t1}	D_t	5 x 10^{17}	0.3	$A_{t1, t2}$	2 x 10^{18}	0.7, 0.4

Figure 4.15: Measured and simulated output characteristics for reference, BS and No-BS cases

The simulated I_{Rev} and I_D-V_D behavior is found consistent with the measured characteristic behavior, hence validating the discussed presumptions on BS mechanisms.

D. EVOLUTION OF "BS" DURING AGING PROCESS

Brunel et al. in [4.13] reported on unpredictable changes in the BS magnitude of devices measured at different times in the course of 4000 hours of aging. The "belly" first grows until 1000 hours of aging and then declines. This abstruse behavior can be presumed to be a consequence of complex interactions between mechanisms influencing device behavior.

To achieve further understanding of aging dynamics, the impact of two specific phenomena on manipulation of the BS effect need to be studied.

Effect of Strain Relaxation on BS

The tensile strain in AlGaN barrier relaxes when the HTRB induced electric field building around the gate-drain edge causes the effective strain to cross the IPE threshold [4.8, 4.11]. Hence, relaxation is a phenomenon which might become important at latter stages of the aging process, contributing to variations in |BS|. The model parameter "relax" (r) is modified within the AlGaN parameter file to simulate relaxation effects within the device model. Piezoelectric charges at device interfaces linearly decrease with a higher degree of strain relaxation [4.23]. Figure 4.16 presents changes in $I_{G,f}$ for r = 0, 0.02 and 0.1 (0, 2 and 10% of strain relaxation). However, the impact of r on BS appears to be small. As observed for r = 0.1 equivalent to 10 % strain relaxation, BS impact is sustained until a slightly higher V_G, and the magnitude displays a minor rise with partial relaxation.

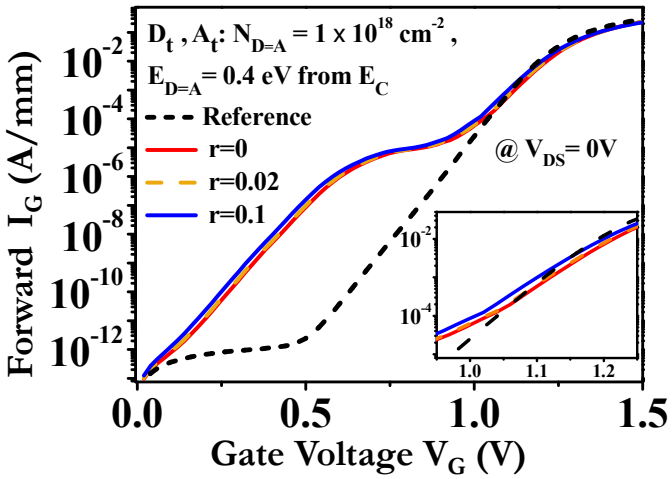


Figure 4.16: Effect of parameter relax (r) on simulated forward I_G-V_G characteristics for a BS case with surface donor traps.

Effect of Defects near Field Plate on BS

The second factor to consider is the shift in defect formation from the gate drain edge towards the field plate near the final stage of aging. Localized changes in strain or electric field distributions and consequently in piezoelectric polarization might cause the peak field to shift away from the gate-drain edge. This shift would alter the donor trapping dynamics. To investigate the associated effect on BS magnitudes, we simulate a donor trap density DF_t, at the GaN cap/passivation interface similar to D_t, but in a region $L_{ext,F}$ = 0.6 µm located away from the gate edge and underneath the FP, as illustrated in Figure 4.17 (left).

The simulated $I_{G,f}$ characteristics when A_t is supplemented with DF_t instead of D_t, are presented in Figure 4.17 (right), for a donor density N_{DF}=1×10^{18} cm^{-2} and different energy values.

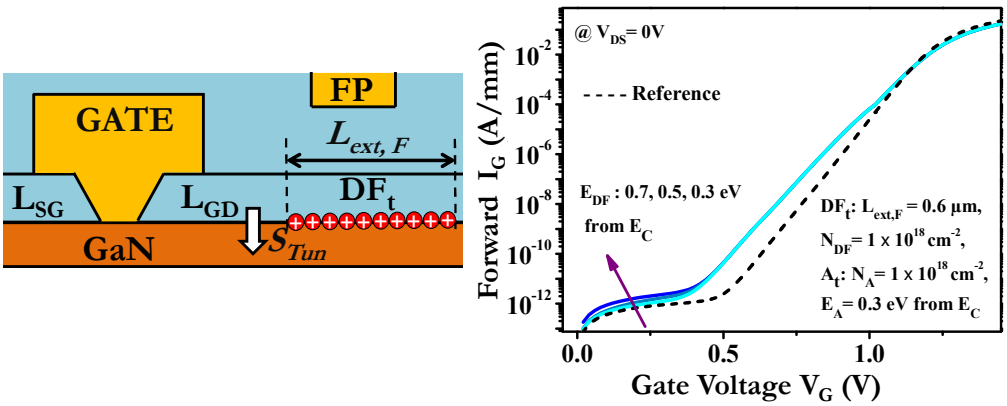


Figure 4.17: (left) Schematic defining donor traps DF_t at the surface SiN passivation/GaN cap interface for an extended length $L_{ext,F}$ around the field plate and (right) simulated forward I_G-V_G characteristics for varying energy positions (E_{DF}) of DF_t and acceptor traps A_t in the AlGaN barrier.

It is apparent that BS magnitudes are distinctly reduced for DF_t traps in contrast to BS caused by D_t (see Figure 4.17 (right)). BS manifests only at bias conditions V_G > 0.4 V, thus

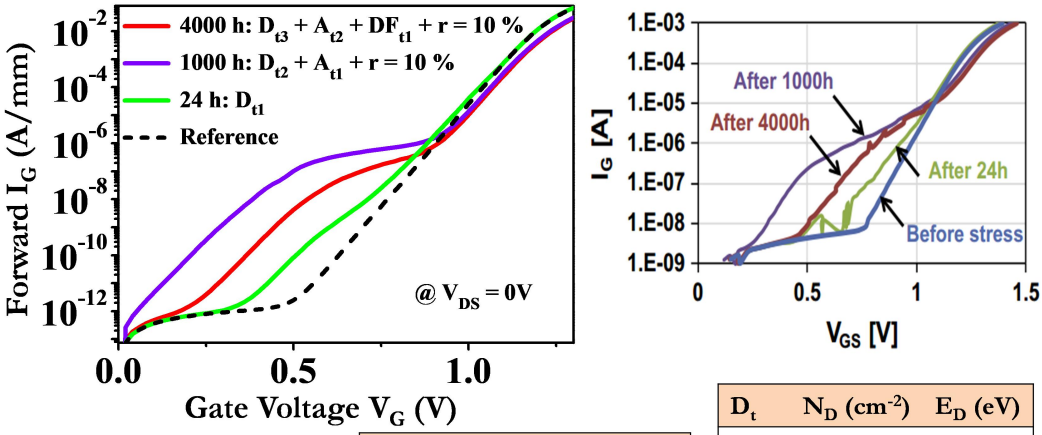
resembling simulated curves produced by deep ($E_D \geq 0.4$ eV from E_C) D_t traps. Further, BS magnitude owing to DF_t is found to be relatively constant, displaying only a weak dependence on E_{DF} for low $V_G < 0.3$ V bias.

Discussion on BS evolution with Aging Stages

Based on the analysis of BS control factors, it is possible to propose a hypothesis addressing the evolution of measured BS during the HTRB aging in [4.13]. Devices subjected to the high electric field during aging tests suffer surface degradation leading to development of numerous defect sites near the gate in the gate-drain region. Existing non-homogeneities initiated from process defects might be activated. In the presence of holes, these sites act as traps. Under the strong electric field accompanying aging tests, holes could be generated within the barrier [4.24], or originate from trap assisted band to band tunnelling [4.1] [4.3] [4.24].

When occupied, they cause random local variations in barrier height, promoting surface leakage. The lower barrier height is also reflected in the shifts in field due to occupied donor trap states close to the surface. These traps can also be expected to participate in TAT as tunneling across the top surface could be significant under high fields [4.9].

The change in BS with aging, reported in [4.13], has been reproduced in Figure 4.18. Simulated curves that reproduce the measured behavior at three different aging time instants are displayed in Figure 4.18 (left).



DF_t	N_D (cm^{-2})	E_D (eV)
DF_{t1}	3×10^{18}	0.4

A_t	N_A (cm^{-3})	E_A (eV)
A_{t1}	3×10^{18}	0.4
A_{t2}	8×10^{18}	0.4

D_t	N_D (cm^{-2})	E_D (eV)
D_{t1}	7×10^{16}	0.6
D_{t2}	5×10^{16}	0.25
D_{t3}	5×10^{17}	0.55

Figure 4.18: (left) Simulations reproducing the evolution of measured BS at different aging times through surface donor traps Dt (coupled to S_{Tun}) adjacent to GD, surface donor traps near the field plate DF_t, AlGaN barrier traps At (coupled to S_{Tun}, B_{Tun}) and piezoelectric relax parameter r. (right) Evolution of the Schottky diode forward characteristic with drain and source shorted to the ground during the HTRB test, reproduced from [4.13].

The first measured gate current curve at 24 hours has a small BS magnitude, and is only observable for V_G> 0.4 V, indicating energetically deep traps probably activated by the aging stress. Further, it completely merges with the reference. This can be modeled by activating D_{t1} traps coupled to S_{Tun} with a low N_D and deep E_D.

With continued aging and the escalating field, dislocations grow and further extend from the gate edge [4.2] while the surface quality worsens, possibly exacerbated by inter-diffusion [4.10] [4.25] and migration of chemical species. More voids and sites for shallower donor sites are created, boosting surface leakage. Once the IPE strain threshold is crossed, the AlGaN barrier relaxes, creating substantial defects near the gate drain region [4.8] and acceptor like traps within the AlGaN barrier. Tunneling is stronger spreading across the AlGaN, and TAT effects intensify. The appearance of surface pits and cracks near the gate foot, as confirmed by electroluminescence (EL) studies of BS devices in [4.13], substantiates the presence of sufficient holes near the gate edge to support aging degradations. This is because several works [4.1-4.3] propose that pits are formed by an electrochemical reaction with hydroxyl groups originating from moisture or oxygen, which are diffused through degraded passivation surfaces. According to this theory, holes would be essential to the AlGaN or GaN near the gate to be then oxidized and create pits composed of Al_2O_3 or Ga_2O_3. With the evidence of relaxation and trap formation, also accompanied by a shift in V_{th}, this state corresponds to the second measured curve at 1000 hours.

This is modeled by adding shallower D_{t2} traps with E_D= 0.25 eV [4.10], coupled to S_{Tun}, A_{t1} coupled to S_{Tun}, B_{Tun} and a 10% relaxation (r= 0.1) of piezoelectric charges within the barrier.

After relaxation, the electric field locally weakens near GD, decreasing leakage as aging progresses. The reduced strain causes the field peak to shift towards FP, subsequently creating defects, or trap sites (DF_t) under FP. Continued defect formation promotes formation of additional traps in the AlGaN barrier. At the same time, high hotspot temperatures near the GD edge can be believed to further de-trap shallow D_t states reducing BS. This is supported by experiments [4.15] that confirm that BS reduces at higher temperatures.

However, the damaged surface can still be assumed to have significant deep D_t sites which do not de-trap. Indeed, the measurement at 4000 hours displays a generally lower BS magnitude, and also a lower $I_{G,f}$ at high V_G, compared to the 1000 hours state. This final state is modeled by introducing traps DF_{t1} around the FP edge in addition to D_{t3}, which produce only a small BS as previously discussed. Here, despite the high concentration of deep D_{t3} traps, the BS magnitude remains low due to the absence of shallow D_t states. A higher N_{A2} is used to model the slight drop in $I_{G,f}$ beyond V_G= 0.8V.

Conclusions from simulation of the BS characteristic

Underlying mechanisms of "belly-shape" are carefully identified through a dedicated measurement and TCAD device simulation study. BS is found to have non-recoverable as well as transient impacts on gate current behavior as a consequence of aging-induced Schottky contact damage and surface degradation surrounding the gate drain region, leading to formation of trap sites. The appearance of BS on aging is reliant on the development of dominantly shallow donor trap sites near the surface. Hence, its occurrence is conditional, and dependent on initial epitaxial quality.

The dedicated TCAD physical simulation of BS is an efficient approach to visualize, reproduce and thus validate the role of the contributing donor traps at the surface and acceptor traps in the AlGaN barrier. Associated tunnelling mechanisms across the surface and the AlGaN/GaN interface are also incorporated.

Trapping-detrapping dynamics of energetically shallow donor-states are affirmed to be the cause of random variations in BS magnitudes. A proposed hypothesis ascribes the distinctive BS characteristic to donor trap induced surface leakage and acceptor traps in the AlGaN barrier, coupled with trap-assisted tunneling across the cap and barrier layers. These inferences are validated through successful reproduction of the BS nature using device simulation.

A detailed discussion recognizes the physical interplay between fundamental trapping mechanisms and auxiliary mechanisms of IPE induced relaxation and associated electric field variations. An interpretation is then derived for the vacillating BS response measured at progressive aging intervals, and justified through corresponding simulations.

4.4 Interpretation for Storage Effects on BS

A. IMPACT OF STORAGE AT ROOM TEMPERATURE ON I_G-V_G

The reduction in BS magnitudes after storage can be considered to be dependent on the relative composition of shallow and deep donor and acceptor traps in each aged device. 4 BS cases are identified as representative, depending on the amount and nature of BS displayed by the devices at T_1, when they were first aged, as displayed in Figure 4.19. All of them displayed a reduction in BS magnitudes after long term storage.

To quantify the fall in $I_{G,f}$, we can calculate the percentage drop in forward I_G (P_f) as follows between T_1 and $T_2 = T_1 + 3$ years:

$$P_f = \frac{I_{G,f}(T_1) - I_{G,f}(T_1 + 3\ years)}{I_{G,f}(T_1)} \times 100$$

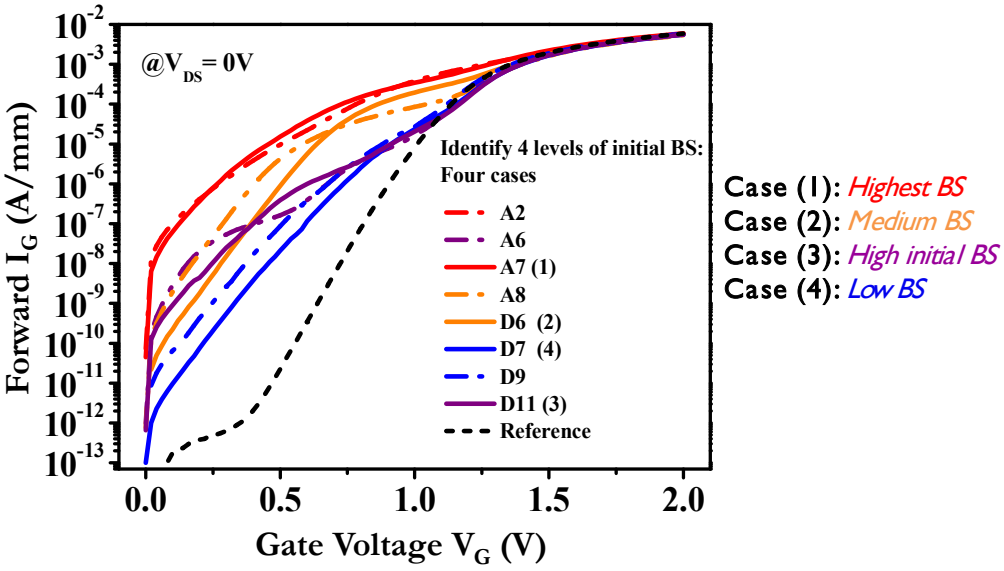


Figure 4.19: Identification of 4 representative BS cases from $I_{G,f}$ measured (at T1) after HTOL aging

P_f characteristics for the four BS cases have been extracted from the measurements at T_1 and the first measurement carried out at T_2. Their natures are summarized in Figure 4.20 to understand how storage affects the gate leakage in forward V_G conditions.

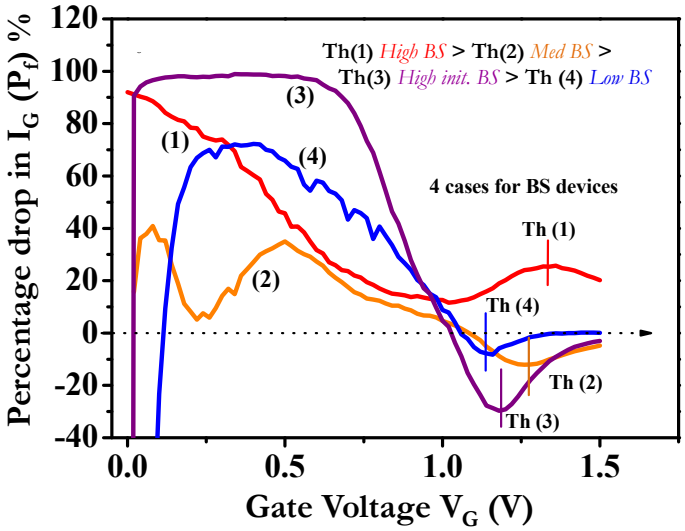


Figure 4.20: Comparison of percentage drop in $I_{G,f}$ (P_f) after storage for four representative BS cases

All four cases display a high positive P_f for low to medium V_G conditions; due to storage-induced reduction in $|BS|$. The general characteristic in each case is distinctly distinguishable from the others but they all converge towards P_f=0 at high V_G. At V_G> 1 V, BS or time effects are marginal and thermionic nature of the curve dominates.

Hence, the changes in $I_{G,f}$ between T_1 and T_2 can be associated to BS related effects only until an identified threshold V_G = Th**.** The value of Th varies with the case studied.

Case 1 has the highest measured BS at T_1 (see Figure 4.19) hence it can be assumed that a high amount of shallow and deep surface donors existed, which indicates significant physical degradation caused during aging. This in turn signifies the presence of high barrier acceptor traps as well. Also, the high magnitude of BS could be enough to mask the acceptor induced fall in $I_{G,f}$, even when close to V_G=1 V.

After storage, de-trapping of a high concentration of shallow surface donors could have taken place, which would explain the high +ve P_f for low V_G and the lower BS at T_2. For 0.5 < V_G < 1 V, the amount of deep donor de-trapping is comparatively lower. Thus, the falling slope of P_f reaches a minimum around 1 V. Beyond V_G= 1 V, effect of barrier acceptor traps is important. At T_1, acceptor trap induced lowering of $I_{G,f}$ was compensated because of the high BS magnitude. At T_2 however, substantial donor-like states have detrapped. This de-masks the lowering of $I_{G,f}$ due to acceptor traps, and corresponds to the small rising peak of P_f. It could presumably be even higher, but some acceptor traps should have likewise de-trapped during the storage time, restricting the associated fall. Since this rise in P_f is still BS-linked, Case 1 threshold Th (1) is identified at the small P_f peak. Beyond Th (1), thermionic emission dominates and the effect of storage time is minimal.

Case 2 displayed medium BS at T_1 hence it can be assumed that the existing shallow and deep surface donors would be lower in concentrations than Case 1. Analogously, formation of barrier traps would also be reduced from Case 1. Correspondingly, after storage, the initial P_f due to detrapping of shallow traps is not so high. For 0.5<V_G< 1 V, deeper donors de-trap as the falling slope of P_f reaches a minimum. The P_f response in this region is similar to Case (1). Beyond V_G= 1 V, most of the acceptor traps that caused a reduction of $I_{G,f}$ at T_1 would have de-trapped hence making $I_{G,f}$ at T_2 higher. P_f is thus negative in this region. Th (2), is obtained at the center of the negative P_f peak. Beyond this point, trap effects cease to control the response.

Case 3 devices had a high BS for low V_G at T_1. Thus, we assume a greater contribution of shallow surface traps and relatively reduced concentration of deeper donor traps. High formation of new surface states corresponding to shallow traps indicates aging-induced surface degradation and hence a high barrier acceptor trap density is probable.

As discussed for Case (1) shallow donor traps present at T_1 strongly detrap during the storage time. Hence, at T_2, Case (3) shows good recovery from BS as P_f is very high and positive initially. For 0.5< V_G< 1V, the amount of deeper donor de-trapping is quite low resulting in a rapidly falling P_f slope. The minimum is obtained near 1 V similar to cases (1) and (2). With the detrapping of high densities of acceptor traps at T_2, $I_{G,f}$ rises. P_f is strongly negative in this region. Hence, Case

(3) shows good recovery after storage respective to both donor and electron trapping. Th (3), the Case (3) V_G threshold occurs earlier, indicating that BS effects are limited within a smaller V_G region.

Case (4) had the lowest BS at T_1 indicating that shallow trap concentrations are considerably smaller. Low densities of deep donors and barrier traps are also expected. These devices are the most robust within the BS device set. The de-trapping of shallow donor states during the storage time yields a high positive P_f for $V_G < 0.5V$. For $0.5 < V_G < 1$ V, deep donor de-trapping is quite low. P_f converges close to the other curves near $V_G = 1$ V as the donor trap impact weakens. Th (4) can be identified in the middle of the negative P_f region.

It is clear that the threshold until which BS effects are sustained in the gate current response decreases progressively from cases (1) to (4). Devices with BS owing to higher shallow donors improve the most after the long storage interval. However, subsequent or repeated characterizations might allow these surface states to be partially re-trapped, reducing the absolute recovery.

B. IMPACT OF STORAGE AT ROOM TEMPERATURE ON I_D-V_D

With the information obtained into BS attributes, we can now take a closer comprehensive look at the storage-induced changes observed in overall device behavior manifested through alterations in I_D-V_D characteristics in addition to I_G-V_G for aged devices.

Instance A: Low variation in I_D

Figure 4.21 presents the effects of the storage time on the I_G-V_G and I_D-V_D characteristics of a particular BS device D11 as an example of the behaviour observed for several BS devices. In this case, in addition to the reduction in $|BS|$ leakage, the I_D nature is moderately affected. For high V_G values, a decrease in I_D at high V_D is noticed. For lower V_G values however, the I_D values are slightly higher than characteristics before storage. We refer to this behaviour as Instance A.

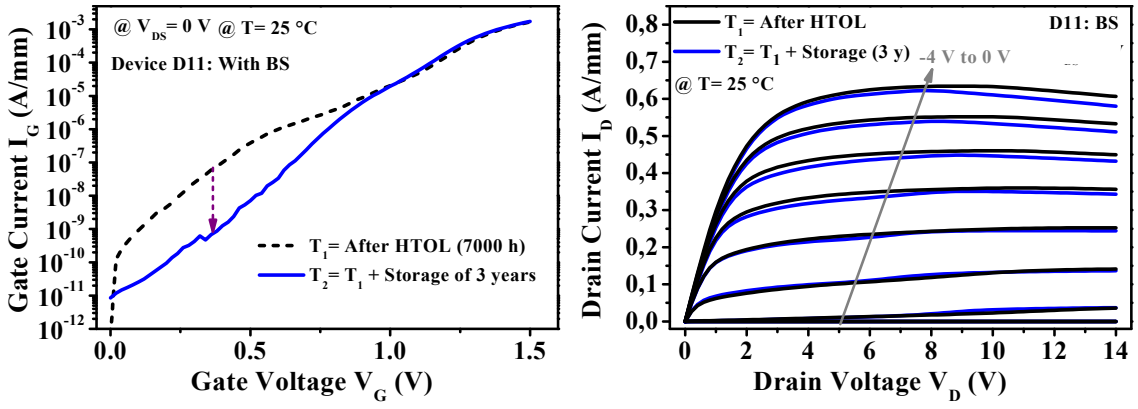


Figure 4.21: I_G-V_G and I_D-V_D characteristics of a BS device displaying a low decrease in I_D-V_D at high V_G after the storage time

In a special case, a device that had been previously identified as a No-BS device after it was aged underwent a noticeable change following the storage interval, as presented in Figure 4.22.

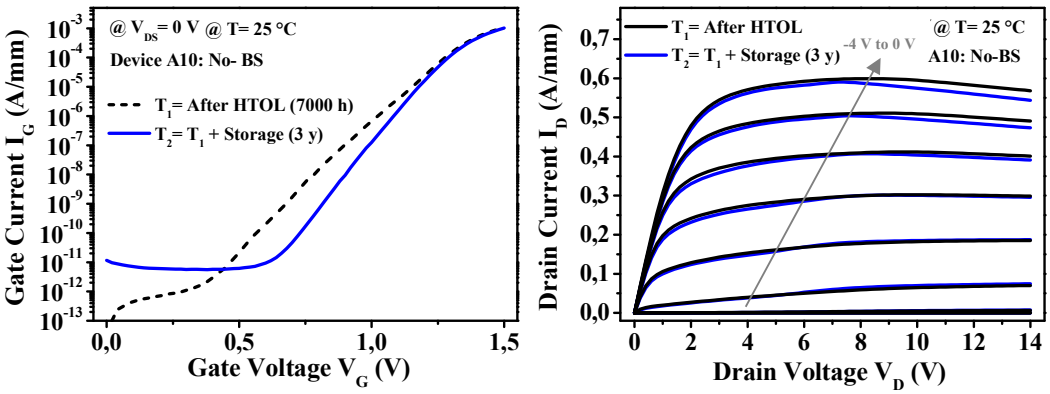


Figure 4.22: I_G-V_G and I_D-V_D characteristics of a device previously identified as No-BS displaying a low decrease in I_D-V_D at high V_G after the storage time

The decrease in I_G between V_G= 0.4 V and 0.7 V shows that the curve initially did display a small amount of belly shape. It was unrecognizable as BS, since the distortion in the I_G shape was weaker compared to the other BS devices and the I_G levels were still lower than the reference. Hence, it resembled a general lower I_G, and thus was recognized as a No-BS device. As previously discussed, this kind of a small |BS| could be a consequence of trap assisted tunneling induced leakage, possible supported by a low concentration of deep donor traps due to intrinsic defects.

After storage, the gate leakage recovers similar to other BS devices. The change in I_D characteristics following storage is also found to be similar to the Instance A scenario.

Instance B: High variation in I_D

For some of the BS aged devices, the effect on I_D characteristics is different as displayed in Figure 4.23. Accompanying the lower gate leakage, a monotonic decrease in I_D levels is observed, behavior we can refer to as Instance B. Further, in the I_G-V_G characteristic at high V_G, we can see a lowering in the gate current. This is in contrast to Instance A behavior where the I_G levels for V_G> 1 V are almost unaffected by storage. While this could be linked to the BS induced I_G decrease, at V_G> 1 V, changes mostly originate from acceptor densities. An increase in shallow acceptors could explain the slight fall in I_G and the uniform decrease in I_D after the storage times. However, an increase in trap densities after a period of inactivity is uncommon. Hence, other possibilities to explain this kind of behavior should also be considered.

We have seen from Section 4.3.C for output currents, that both BS and No-BS trap definitions lead to a substantial decrease in I_D levels due to the shallow and deep acceptor trap contributions respectively.

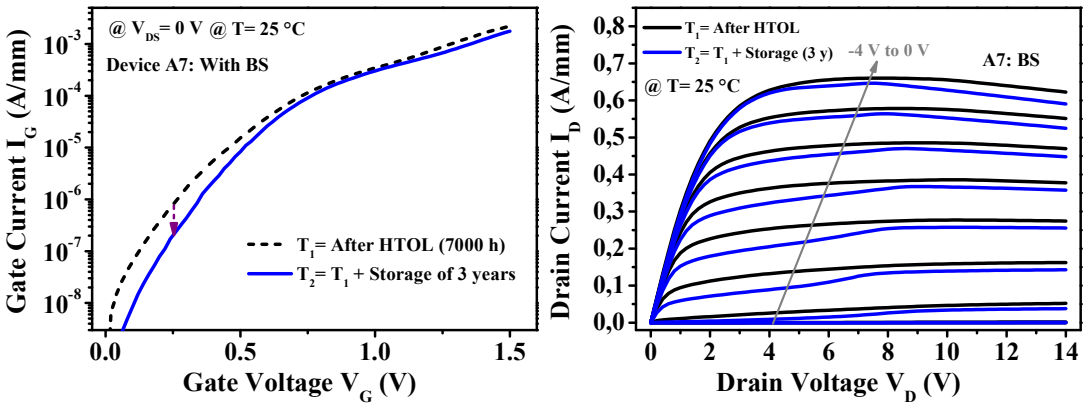


Figure 4.23: I_G-V_G and I_D-V_D characteristics of BS device A7 before and after storage displaying a high decrease in I_D-V_D at high V_G after the storage time

If an initial prediction were to be made, storage might have been expected to improve I_D levels in association with the lower BS observed in I_G-V_G characteristics. However, the observed I_D-V_D behavior for both Instance A and B is quite different. This implies complex trap interactions since it is impossible to attest this variation to any one particular trap. Understanding trap interactions that could be responsible for divergent I_D behavior while presenting similar effects on I_G requires a more detailed study. TCAD simulations are used to help in understanding trap occupational tendencies that could have been responsible for such observations.

Simulating Tendencies

The experimental observations could be the culmination of several device mechanisms that could be impossible to recreate. However, we explore possible scenarios based on trapping dynamics of four contributions: shallow donor traps $\mathbf{N_{DS}}$ with E_D= 0.3 eV, deep donor traps $\mathbf{N_{DD}}$ with E_D= 0.6 eV, shallow acceptor traps $\mathbf{N_{AS}}$ with E_A= 0.4 eV and deep acceptors $\mathbf{N_{AD}}$ with E_A= 0.7 eV from E_C. Donors and acceptors are defined within L_{ext} and $L_{ext,A}$ in continuation with previous discussions.

The effect of acceptor traps on the I_D characteristic is generally stronger, and can be expected to dominate I_D changes compared to the influence of donor traps. We consider two conditions to understand how changes in acceptor densities may influence the drain current characteristic in the presence of donor traps. We consider a high trap concentration N_1= 5×10^{18} cm^{-3} and a low concentration N_2= 1×10^{16} cm^{-3}. We adopt two ways of looking at occupational changes. In Figure 4.24 (left), the I_D characteristic for all traps (N_{DS}, N_{DD}, N_{AS}, N_{AD}) with high densities = N_1 is compared to when N_{AS} and N_{AD} are individually reduced (~ de-trapping) to N_2. In Figure 4.24 (right), the contrary is presented where the curve obtained for all traps (N_{DS}, N_{DD}, N_{AS}, N_{AD}) with low densities = N_2 is compared to characteristics with only a high concentration of N_{AS}= N_1 or a high concentration of N_{AD}= N_1 (~ trapping) while the rest of the trap densities remain low.

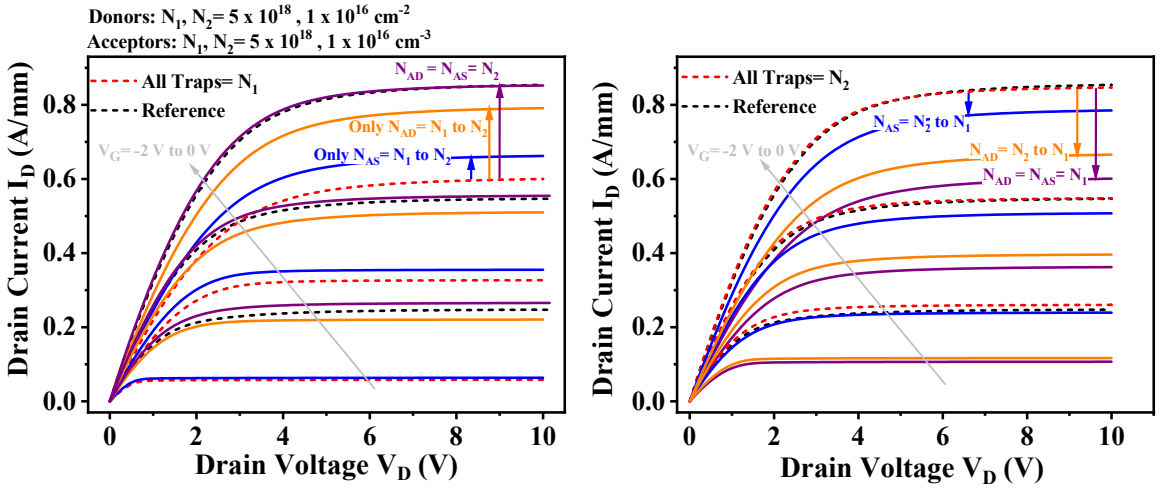


Figure 4.24: I_D-V_D characteristics for changes in shallow and deep acceptor concentrations from an initial condition of all traps (left) : N_1=5×10^{18} cm^{-2} (donors), N_1=5×10^{18} cm^{-3} (acceptors) and (right) : N_2=1×10^{16} cm^{-2} (donors), N_2=1×10^{16} cm^{-3} (acceptors)

For Figure 4.24 (left), the donor traps (N_{DS} and N_{DD}) are fixed at high concentrations. We observe that just the de-trapping of shallow acceptors (N_{AS}) moderately improves I_D while the de-trapping of deep acceptors (N_{AD}) substantially improved I_D levels. This can be directly attributed to the higher impact of deeper energy positions. However when both shallow and deep acceptor traps are de-trapped to a low concentration, we see that the I_D characteristic (for N_{DS}=N_{DD}= high and N_{AS}=N_{AD}= low) is slightly improved over the reference. This implies that when acceptor concentrations are low, the presence of donor traps acts to support and increase the I_D levels.

For Figure 4.24 (right), we begin with donor traps and acceptors fixed at low concentrations. We can observe that this condition (N_{DS}=N_{DD}= N_{AS}=N_{AD}= low) corresponds to a slightly improved I_D at V_G= -2 V and a slightly lower I_D at V_G= 0 V in comparison with the reference. This is similar to the change in I_D observed for BS devices after the storage interval. Hence, this is an important observation. Continuing the discussion however for Figure 4.24 (right), as can be expected, the shift from N_{AS} from low to high concentrations degrades I_D moderately while the decrease for N_{AD} transitioning from low to high is stronger.

Based on these and previous observations, we can recognize that acceptor trap impact on I_D remains conventional even in the presence of donors. Any increase or decrease in densities will cause a corresponding lowering or increase in I_D levels, irrespective of energy. It is the impact of the donor traps on the I_D characteristic that is subject to variation depending on the acceptor trap densities.

Based on transitions in these traps corresponding to "before storage" and "after storage" conditions, we can try to identify circumstances that could lead to Instance A (fall in I_D at high V_G, rise at low V_G) or Instance B (uniform decrease in I_D) behavior.

The first step is to identify constraints that limit the number of trap transitions from all possible cases to only those valid for the storage scenario. It can be assumed that a long period of inactivity would induce de-trappings and hence a lowering in trap densities, presumably near the surface. From previous discussions, we can assume that a decrease in $I_{G,f}$ should, in fact, be associated with a de-trapping of shallow donor traps. Since No-BS devices show little to no change due to storage we can assume that deeper acceptors do not de-trap during the storage period. Hence, barring minor de-trappings, the lowering of acceptor densities in BS devices is not considered since it would have induced a clear improvement in I_D characteristics. Based on these assumptions, Figure 4.25 compiles the results based on acceptor trap preconditions that correspond to the presence of BS, to summarize which combinations have been found to induce Instance A or Instance B like variations. The trap concentrations $N_1 = 5\times10^{18}$ cm^{-3} and $N_2 = 1\times10^{16}$ cm^{-3} have been referred to as high and low respectively.

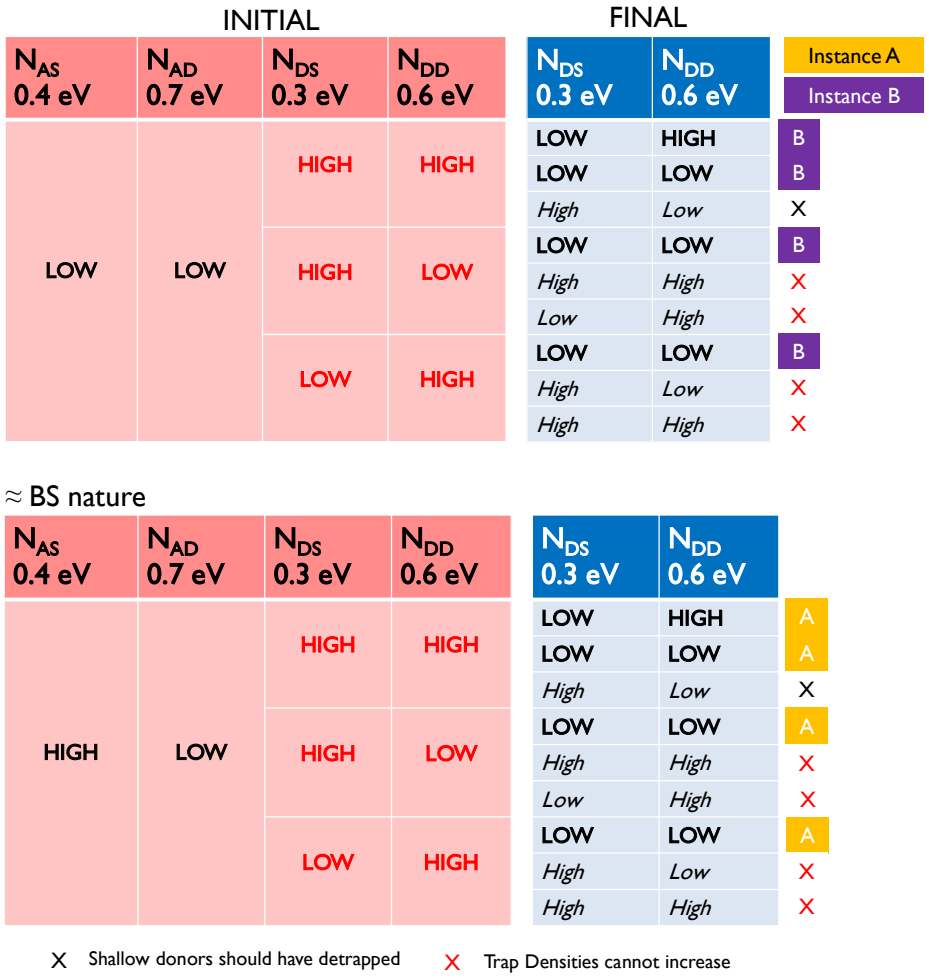


Figure 4.25: Possible trapping transitions to explain the effect of storage for two acceptor trap preconditions (low N_{AS}= N_{AD} and high N_{AS} and low N_{AD}) associated with causing the belly shape

The combinations incompatible with storage-related changes have also been indicated. The shallow donor trap contribution to variation of I_D is found to be quite significant. For the condition most representative of BS: a high N_{AS} and low N_{AD}, detrapping of donor traps has been found to be consistent of observed Instance A behavior.

Figure 4.26 presents the three major transitions that could have occurred during storage for devices that display a conditional decrease in I_D following the storage time. These simulated cases represent devices that suffered from a high shallow acceptor concentration following the aging tests.

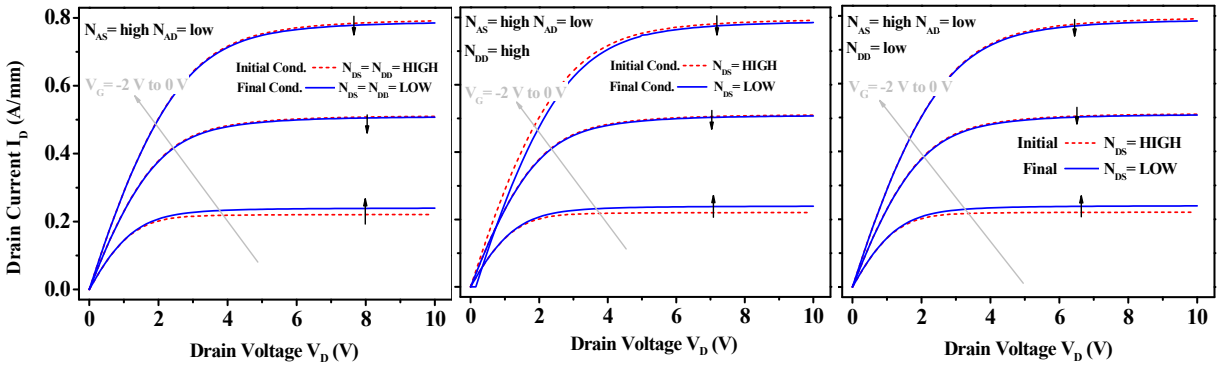


Figure 4.26: I_D-V_D donor detrapping transitions for acceptor trap precondition: high N_{AS} and low N_{AD}

Changing the initial condition to low densities for both acceptor traps, the Instance B behavior is obtained when donor densities are reduced, wherein the I_D is lower for all associated donor detrappings. This behavior would then correspond to devices for which a substantial concentration of acceptors was not formed during the aging process. The BS in these devices majorly stemmed from surface degradation and hence, the donor traps. Figure 4.27 presents the two major detrapping transients that correspond to storage effects under these conditions.

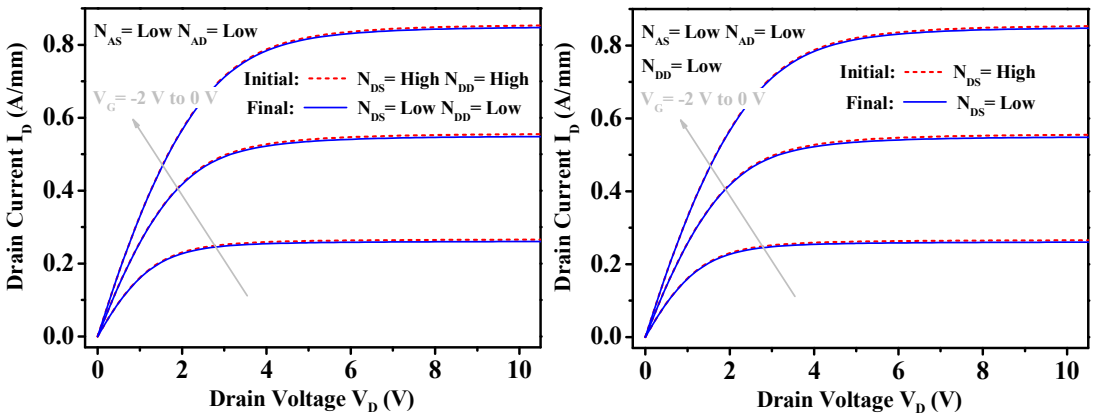


Figure 4.27: I_D-V_D donor detrapping transitions for acceptor trap precondition: low N_{AS} and low N_{AD}

Although the absolute magnitude of variation is low compared to measurements, the tendency is consistent with the observations and helps to interpret the core of incongruence in I_D

characteristics within the same set of devices with BS. These results reiterate that in the absence of deep acceptors, the presence of donors is advantageous to I_D levels, especially at high V_G. This is why de-trapping of donors effects a decrease in I_D levels. With stronger shallow acceptors, higher donor traps tend to decrease I_D for lower V_G.

In the presence of deeper acceptor traps and substantial donor traps, the storage interval would induce an improvement in I_G levels as has been simulated and compiled in Figure 4.28 for the two remaining preconditions with high densities of energetically deep acceptors.

≈ Tending towards No-BS nature

N_{AS} 0.4 eV	N_{AD} 0.7 eV	N_{DS} 0.3 eV	N_{DD} 0.6 eV
LOW	HIGH	HIGH	HIGH
		HIGH	LOW
		LOW	HIGH

N_{DS} 0.3 eV	N_{DD} 0.6 eV	
LOW	HIGH	Better I_D
LOW	LOW	Better I_D
High	*Low*	X
LOW	LOW	Better I_D
High	*High*	X
Low	*High*	X
LOW	LOW	Better I_D
High	*Low*	
High	*High*	

≈ No-BS nature

N_{AS} 0.4 eV	N_{AD} 0.7 eV	N_{DS} 0.3 eV	N_{DD} 0.6 eV
HIGH	HIGH	HIGH	HIGH
		HIGH	LOW
		LOW	HIGH

N_{DS} 0.3 eV	N_{DD} 0.6 eV	
LOW	HIGH	Better I_D
LOW	LOW	Better I_D
High	*Low*	X
LOW	LOW	Better I_D
High	*High*	X
Low	*High*	X
LOW	LOW	Better I_D
High	*Low*	
High	*High*	

Figure 4.28: Possible trapping transitions to explain the effect of storage for two acceptor trap preconditions (high N_{AS}= N_{AD} and low N_{AS} and high N_{AD}) associated with No-BS

Devices containing this kind of acceptor densities due to the aging process would be closer to displaying a No-BS like characteristic i.e. a lower I_G due to the deep acceptors. If in addition to acceptors, substantial donor traps were also formed, their detrapping in the storage time would increase I_D levels. Hence, we can infer that in the presence of deep acceptors, donor traps are an additional aggravating factor that further degrades I_D.

Hence, their de-trapping would be accompanied by a corresponding rise in I_D levels.

If the No-BS devices in our device set had significant donor traps which had subsequently detrapped, we should have seen an improvement in I_D characteristics following storage. Since no such change in I_D was observed, it can be concluded that the No-BS devices in this device set had negligible donor traps after the first round of aging.

Perspective on Storage effects

The primary inferences from this section relate to understanding how storage has affected the device characteristics for BS devices in different ways within the same device set. This discussion was facilitated by the knowledge acquired from the BS simulations which highlight the fundamental mechanisms that governs and manipulates this effect. Donor traps are recognized to increase gate leakage in all conditions, while they can be beneficial or detrimental to output current levels, depending on whether the acceptor trap densities for the same devices are low or high respectively. The inferences are also helpful in understanding the effects of a second round of aging on these devices, described in a later section. The change in device characteristics from first round of aging to storage and finally after the second round of aging will be compared which allows further insight into trap density formation and redistribution.

4.5 Turn-on Response of BS-Inducing Trap Contributions

A. RESPONSE OF BS CASES TO AN OFF-ON PULSE TRANSITION

To investigate effects and changes in the belly-shape output characteristic induced by off-on pulsing considerations, we adopt the approach detailed in Chapter 3 and apply it to BS, No-BS and reference cases. The pulse parameters chosen are constant and as described in Figure 4.29.

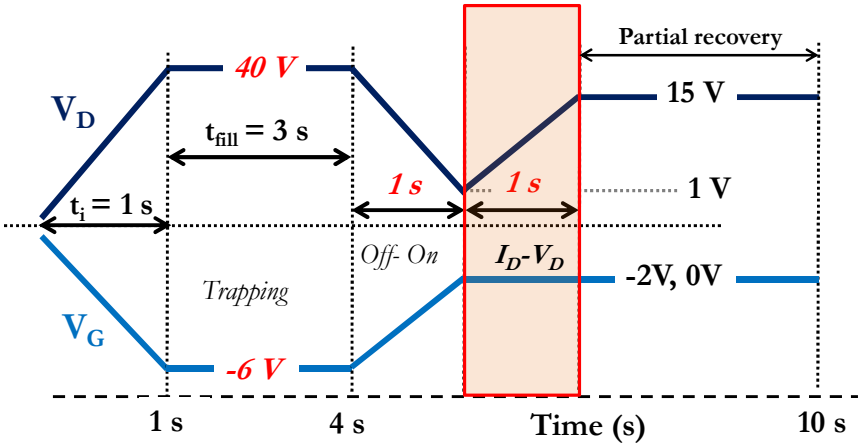


Figure 4.29 : Pulse parameters for transient analysis into belly shape

The trapping duration with a trapping voltage of V_{Trap}= 40 V is fixed at 3 s with fall and rise times of t_{HL}=t_{LH}=1 s. The I_D-V_D response is obtained by a ramp up to V_{Bias}= 15 V immediately after the off-on transition.

The output characteristics for donor and acceptor trap responses at V_G= 0V are compared in Figure 4.30.

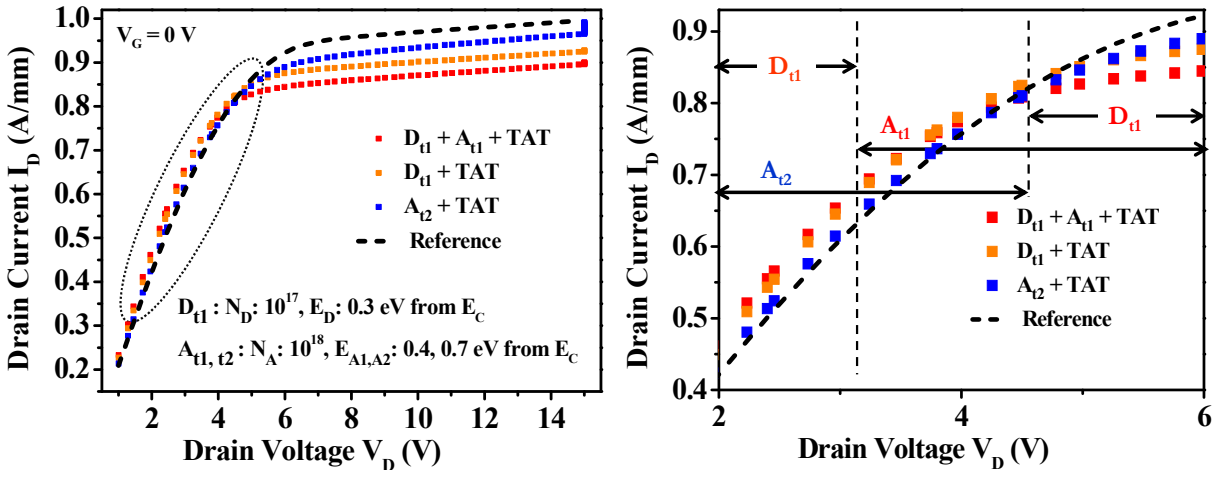


Figure 4.30 : Output characteristics obtained through transient simulation of BS (D_{t1}+ A_{t1}+TAT) and No-BS (A_{t2}+ TAT) scenarios for V_G= 0 V.

The BS case is, as previously discussed, represented as a combination of shallow donors (D_{t1}) defined in a L_{ext}= 0.3 µm close to the gate to drain regions and medium acceptors (A_{t1}). The individual D_{t1} response is also plotted for contrast.

Both cases have trap-assisted tunneling activated. The No-BS response is a consequence of deep acceptors A_{t2} with TAT activated. Equivalent curves are compiled in Figure 4.31 for V_G= -2 V.

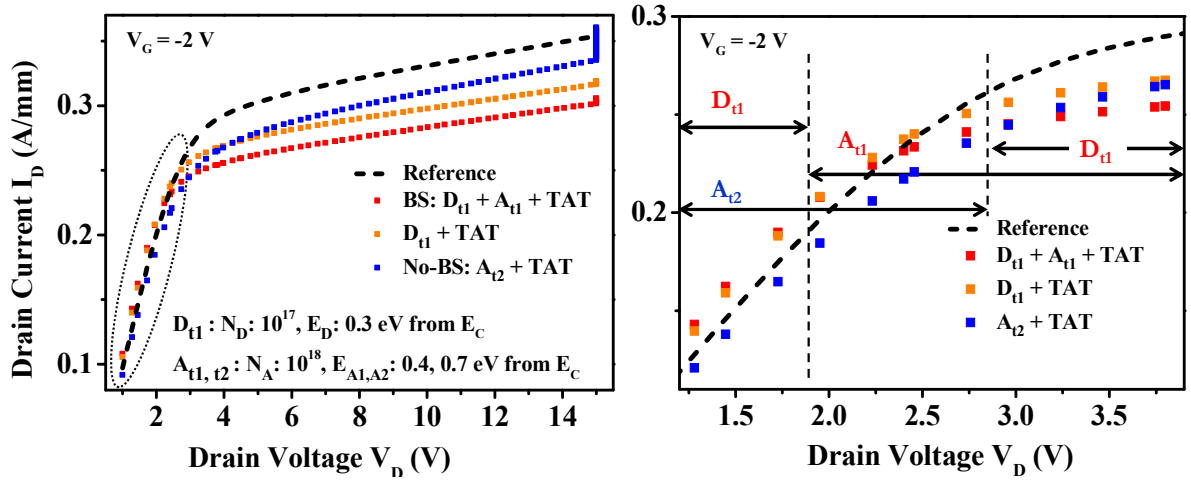


Figure 4.31 : Output characteristics obtained through transient simulation of BS (D_{t1}+ A_{t1}+TAT) and No-BS (A_{t2}+ TAT) scenarios for V_G= -2 V.

It is easily discernible that the I_D levels beyond 4 V suffer greater damage for the cases with donor traps. The BS case is the worst affected in this region, with the presence of medium energy acceptors A_{t1} in addition to shallow donors D_{t1}. With deeper acceptor traps A_{t2}, the degradation in I_D is slightly higher in the presence of TAT.

The linear region of the output curve is closely inspected to detect alterations in R_{on}. The regions where each kind of trap maximally affects the response are marked in Figure 4.30 and Figure 4.31 (right). Until V_D= 2.5 to 3 V, all the curves show a slight improvement in the R_{on} slope. This is a consequence of the donor traps D_{t1} and the TAT leakage.

From Figure 4.30 (right), we see three distinct regions displaying the changes in the case responses as V_D slowly rises. The acceptor trap responses are almost identical, and hence it's the deep trap energy that controls the associated response. Initially, BS response is highest followed closely by the D_{t1} trap response. In this first interval, the shallow donor trap impact is dominant. In the second interval from 3 V- 4.5 V, the BS response begins to fall below the D_t-only response, indicating the influence of acceptor traps in reduction of I_D. For the final interval from 4.5 V to 6 V, we see both curves with D_{t1} decrease to levels lower than the A_t-induced responses. In this region therefore, donor traps are dominant again, contributing further to I_D degradation. This behavior is still consistent at V_G=-2 V in Figure 4.31 (right), with small shifts in the bias ranges for each interval.

As previously discussed, the BS magnitude is substantially lower when donor traps DF_t are defined away from the gate, which corresponds to a reduced BS (BS_{Red}) scenario. Figure 4.32 presents the I_D-V_D comparison at V_G=0 V between donor trap definitions close to the gate edge compared to donors DF_t defined under the field plate.

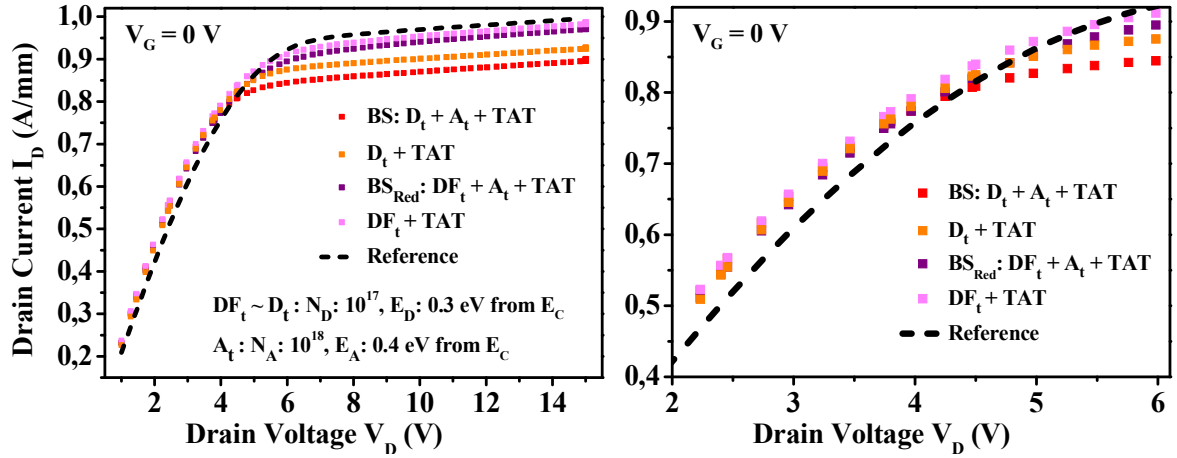


Figure 4.32 : Output characteristics obtained through transient pulses for donor traps at V_G= 0 V.

The chosen trap concentrations and energy positions are otherwise identical. The corresponding characteristics at V_G= -2 V are presented in Figure 4.33.

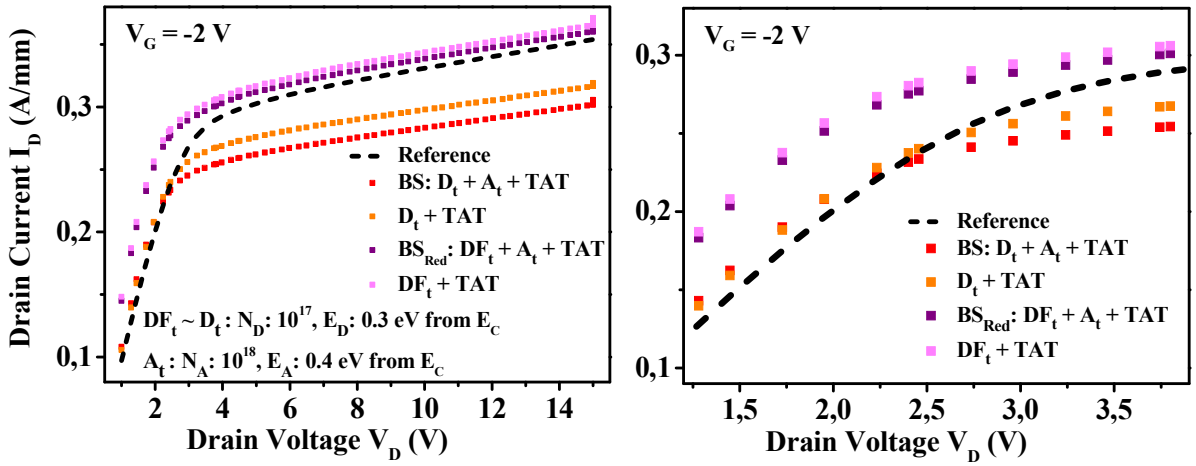


Figure 4.33 : Output characteristics obtained through transient pulses for additional donor traps DF_t away from the gate at V_G= -2 V.

The device response for donor traps defined close to the field plate is substantially improved with better R_{on} and I_D values. The BS_{Red} case displays slightly lower levels than with just DF_t due to the additional acceptor traps. Both display a better R_{on} in the linear region and suffer the least degradation in current levels at higher V_D for V_G= 0 V. In fact, at V_G=-2 V, the responses with DF_t are considerably enhanced over the reference curve over the entire V_D range, since the associated improvement in channel densities is more critical closer to V_{th}.

Intermediate Conclusions: Donor control over BS Impact

We can conclude that causal scenarios for BS, especially the presence of donor traps close to the GD edge are quite detrimental to transient response following switching or off-on transitions. The deterioration is more critical at high V_D conditions. However, R_{on} values do not degrade because of the fast response from the additional donor-induced currents. Despite the better initial current levels, BS cases have the potential to prove more damaging than deep acceptors towards sustenance of I_D performance following a switching event. Donor traps near FP have favorable effects on device behaviour especially when accompanying acceptor trapping occurrences are low.

4.6 HTRB Aging of the BS Devices

Some of the devices from the HTOL aged device that were re-measured after three years of inactivity were next subjected to a second round of aging tests.

Since the devices had been previously aged under HTOL conditions, to activate a different mode, the aging mechanism was changed to HTRB testing which involves biasing the device with a high reverse gate bias and moderate drain voltages at high temperatures.

The aging test bench involved the Lakeshore 336 Temperature Controller and the software controlled BILT Modular Test system (Figure 4.34 (c)) to apply the stress bias. The 40 V/200 mA port was used for the gate and the high power 60 V/2 A port was used for the drain. To ensure that the device is stressed within a temperature controlled enclosure, the TTPX Lakeshore Probe station was employed. The package holder was sealed within the station as shown in Figure 4.34 (a) and (b) and the probes were replaced with SMA (Sub Miniature version A) connections. I_G-V_G, I_D-V_D, I_D-V_G measurements were performed under different conditions. The aging process was paused at multiple intervals to observe induced changes in gate leakage and output characteristics.

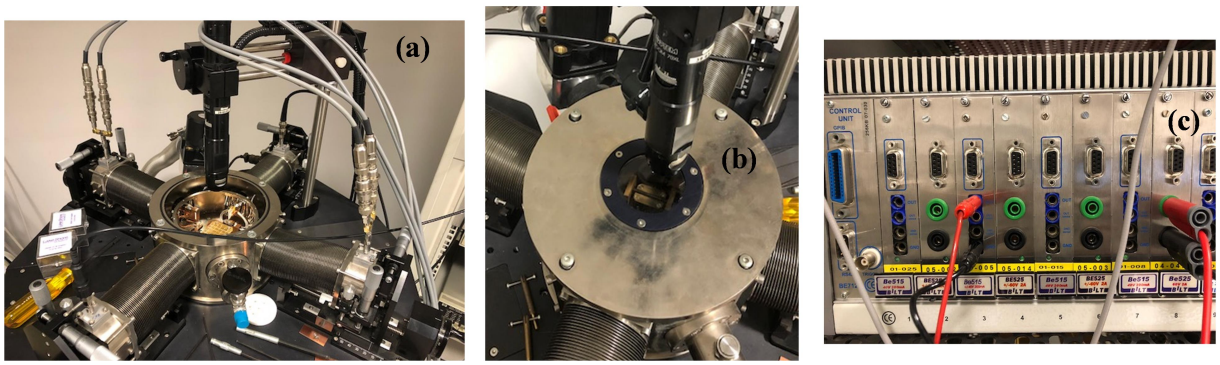


Figure 4.34 : a) the Lakeshore probe station setup (b) the device fixture fixed within the compartment and (c) the BILT test system for application of aging stress

The gate and drain biases were fixed at -7 V and 30 V respectively. Since these devices were once aged, care was taken to find an appropriate temperature for further aging to prevent immediate device failure. Generally a temperature of 175 °C is found suitable for virgin devices. Hence, the first test for these devices was carried out with a lower 125°C. This however did not yield any significant change in parameters over several days, indicating that the stress under given bias conditions wasn't strong enough. A temperature of 140°C was finally chosen as a good compromise to induce aging stresses within the device. The aging tests were performed over a period of 70-80 hours.

Some of the devices suffered an irreversible increase in leakage currents for longer aging times resulting in device breakdown.

A. DEVICES WITH BELLY SHAPE

Figure 4.35 and Figure 4.36 presents the characteristics of a couple of BS device after 78 and 70 hours of aging (T_3) compared with its behaviour after the storage (T_2) and prior to aging, and finally before the storage period (T_1) which is just after the first round of HTOL aging. From the I_G-V_G characteristics of Figure 4.35 (left), it is found that the magnitude of belly shape has been reamplified due to the aging stress.

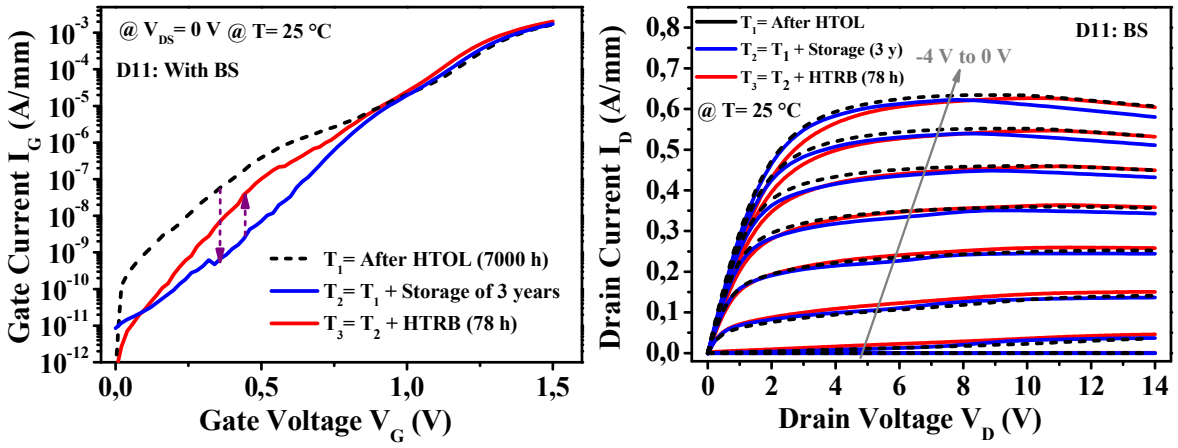


Figure 4.35 Effects of aging on the I_G-V_G and I_D-V_D characteristics of a BS device D11

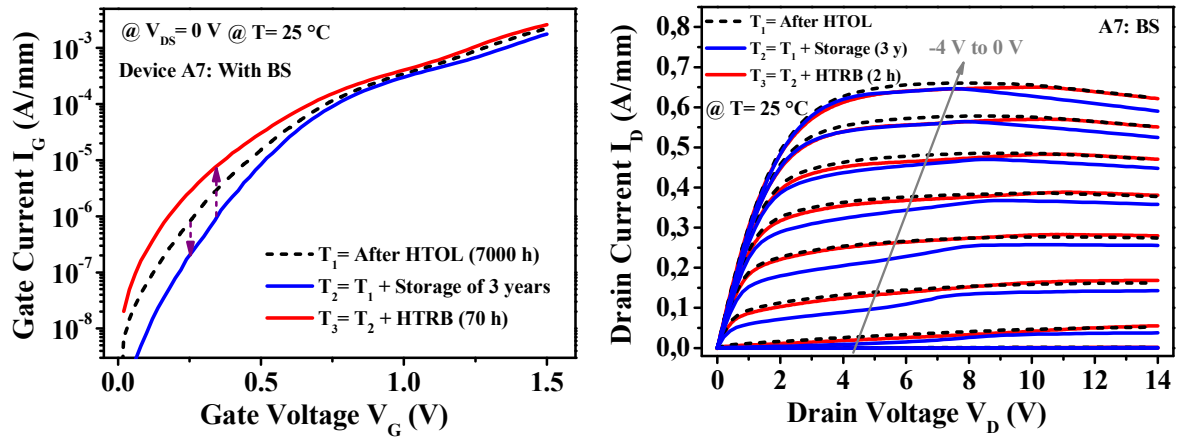


Figure 4.36 Effects of aging on the I_G-V_G and I_D-V_D characteristics of a BS device A7

The recovery in BS that occurred due to the storage time is compensated by the second aging test. In fact, for some devices (see Figure 4.36 (left)), the BS is strengthened beyond the magnitudes initially observed after 7000 hours of the first HTOL aging. This is an important observation. After long aging tests such as the first HTOL aging of these devices, aging effects usually saturate and the device reaches a stable state with a certain amount of physical degradation. With a second round of aging, it is often difficult to induce further change. However, the I_G response suggests that not only have the available surface sites been reoccupied by holes, further surface degradation has occurred during the second aging, which allows the |BS| to overshoot the leakage after the first aging test. This could be attributed to the change in the mode of aging. HTRB is a stronger stressing method, and especially important near the gate contact due to the high electric field from the reverse bias.

On comparison of the I_D-V_D characteristics for both devices in Figure 4.35 and Figure 4.36, the aging stresses (T_3) are seen to counterbalance the storage induced lowering in I_D (state T_2) at moderate to high V_D and approach the initial I_D levels of T_1. Following with the previous discussion

which links the storage effects to donor detrapping transitions, this aging-induced compensation can be directly ascribed to a retrapping of the donor traps which had detrapped during the inactive 3 year interval. However, a second effect of the aging tests seems to be a severe increase in R_{on}, especially discernible in Figure 4.35. Another observable effect is an increase of I_D levels from T_2 to T_3, minor for low V_G values in Figure 4.35 and notably strong for Figure 4.36. At high V_G and low V_D conditions, this rise is offset by the R_{on} decrease.

To better understand the development of these changes, Figure 4.37 compares the I_G-V_G and I_D-V_D characteristics of a BS device at aging timings of 58 hours and 77 hours.

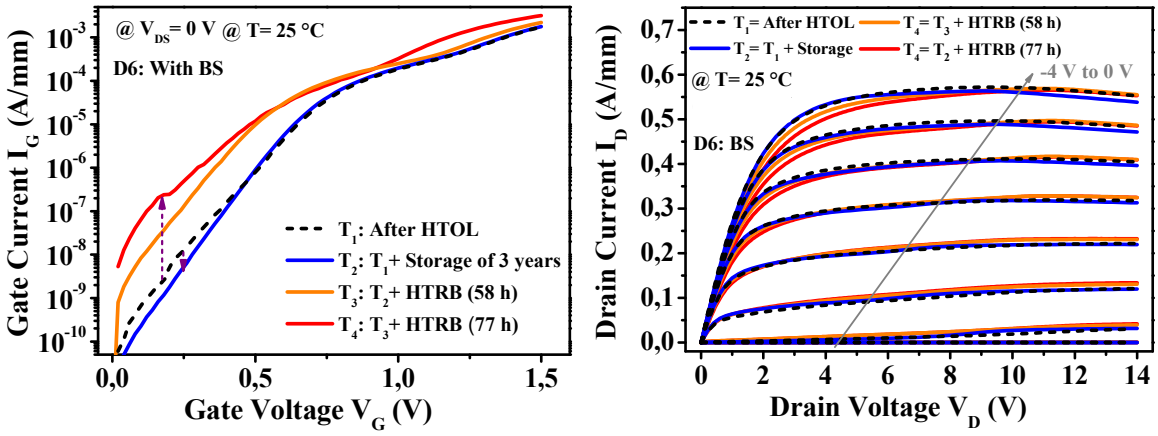


Figure 4.37 Effects of aging on the I_G-V_G and I_D-V_D characteristics of a BS device D6

The major changes that occur on prolongation of aging is a worsening in R_{on} and a rise in I_G at high V_G. This increase in I_G is also observable in Figure 4.35 and Figure 4.36 compared to the storage characteristics. The increase in |BS| between 58 and 77 hours is quite minor in comparison, attributable to small changes in shallow donors. Hence, the increase of belly shape is not directly linked to the mechanism responsible for the other results.

Another observation from Figure 4.37 is a small increase in I_D for low V_G values from 58 hours to 77 hours, accompanying the higher R_{on} and a higher I_G for $V_G > 1.0$ V. From Figure 4.24 which discusses the effects of changes in acceptor trap densities, it was established that deep acceptors induce much stronger reductions in I_D at low V_G compared to shallow acceptors.

All these changes are indicative of a redistribution of the shallow acceptor trap densities, triggered by the aging process. A transition towards higher shallow acceptors and reduction in density of deep acceptors could explain these observations. It would explain the general recovery in I_D, especially at low V_G due to the fall in deep donor density. From BS simulations, the higher I_G for $V_G > 0$ V would correspond to a shift of the contributing acceptors to shallower energies or lower densities. The R_{on} degradation could be a consequence of the higher density of shallow acceptors.

Their impact on I_D-V_D would be limited to low V_D since the occupancies will decrease as the V_D rises. However, further support factors could possibly be present which contribute to the substantial stress-induced R_{on} increase.

B. DEVICES WITH TRIVIAL INITIAL BS

Figure 4.38 presents the effects of 80 hours of aging on the device that was previously identified as No-BS but was found to display a lowering of I_G following the storage interval as previously discussed in Section 4.4.B.

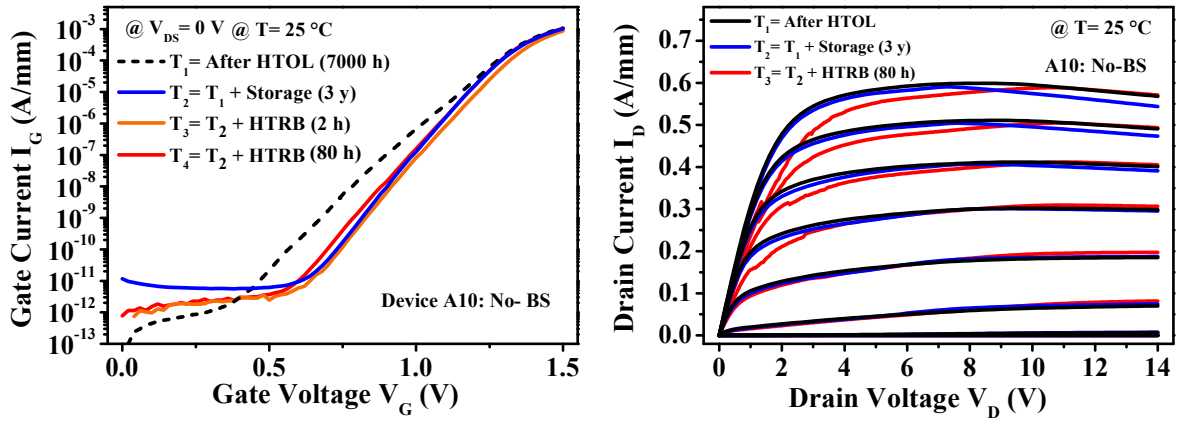


Figure 4.38 Effects of aging on the I_G-V_G and I_D-V_D characteristics of a BS device A10 previously identified as a No-BS device at T_1.

This is the only case in which the effects of storage on I_G have not been reversed by application of the HTRB aging stress. We see that the gate current is maintained close to the characteristic measured at T_2, 3 years after the device was first aged. The small amount of BS originally present in the device seems to have completely recovered and no traces of BS reappear even after 80 hours of aging.

The I_D characteristics however, display a strong R_{on} worsening similar to other aged devices. In fact, it is more severe and extends to lower V_G values. This is further evidence that the BS effect or more specifically donor traps, is highly unlikely to be the causal mechanism behind the R_{on} changes. Initially recorded as a No-BS device at T_1 since the I_G level was lower than the reference, this device should contain a high density of acceptors. Hence, the stronger R_{on} worsening in this device emphasizes the role of acceptors.

4.7 Conclusions and Perspectives

The belly shape effect is a combination of aging induced transient and enduring mechanisms because of degradations in the physical structure close to the gate edges in areas of high fields.

The appearance of BS is dependent on initial as well as aging-induced alterations in surface and epitaxial quality. Its dominant causal mechanisms are shallow donor surface traps (E_D= 0.2-0.4 eV) coupled with acceptors in the AlGaN barrier energetically located between 0.3 and 0.5 eV. Substantial evidence suggests energetically variable trap processes with complex interactions.

DC measurements performed to ascertain the long term impact and variability of this effect allow the discussion of storage-induced detrapping transients of the trap components. The BS is recognized to be partially recoverable with long times due to a fall in trap occupation but the physical surface degradation is irreversible, and thus the surface defects that act as shallow trap sites allow retrapping and random fluctuations in BS magnitudes subject to stress or biasing considerations.

A detailed TCAD simulation study, reproduces the anomalous gate leakage as the consequence of donor state induced surface leakage defined near the drain edge of the gate, coupled with trap assisted tunneling across the AlGaN barrier allowing a leakage path from the gate to the channel. A proposed hypothesis further corroborates experimental observations with inferences drawn from physical simulations to interpret the unpredictable evolution of gate current during the course of the first round of aging responsible for triggering the BS effect.

BS reduces for shifts in donor trap locations away from the gate edge, and towards the field plate edge. However, the turn on response is much better for traps defined closer to the gate. BS causal scenarios i.e. shallow energy donor traps and medium energy acceptors, even with the improvement in R_{on} could be more detrimental than deep acceptors to I_D following a switching event, and worsened at higher frequencies. Donors under the field plate are found to have favorable impacts on steady state performance, but degrade the switching efficiency.

On a second round of aging under HTRB conditions, BS magnitudes increase considerably, negating and exceeding storage induced recovery in the leakage magnitudes. The I_D impact too is compensatory to detrappings during storage. A substantial R_{on} degradation is also observed for both BS and No-BS devices. Since it appears in all of the aged devices and has been found to be generally non-recoverable, it is probably linked to field induced alterations in acceptor densities or irreversible structural deteriorations. Detailed investigation and a wider sample set are essential to understand the origin, and thus, the extent of vulnerability of BS devices to this effect.

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CHAPTER 5

Laser Characterization towards Trap Analysis

STRESS AND TRAPPING DYNAMICS

5.1 Introduction

A laser source is produced from stimulated emission of electromagnetic radiation with very high levels of spatial and temporal coherence [5.1]. As such, lasers can produce very short pulses containing high amounts of a specific energy i.e. a particular wavelength, within a small focused spot area. General luminescence techniques have proved effective in different approaches towards trap and defect analysis [5.2-5.3] of GaN HEMTs. Bouya et al. in [5.3] used illumination to study the effects of traps with high energies (1.4 eV to 2.3 eV) on AlGaN/GaN HEMTs.

If a laser beam provides trapped states with enough energy to induce a detrapping, it allows us to monitor and extract detrapping transients dependent on the wavelength of the laser beam. The work is an attempt to develop techniques towards understanding trap constraints. By combining stress conditions and laser, the trapping state of the device can be altered. Trap contributions to the device behavior and their kinetics under various circumstances can thus be captured.

Since the devices under test are from the belly shape set discussed previously in Chapter 4, this study is also an endeavour to achieve an alternate understanding into the trapping dynamics that lead to the appearance and strengthening of the belly shape. Optical Beam Induced Photocurrent or OBIC is a technique that can be used for defect imaging and failure analysis [5.4-5.6] by the excitation of carriers through photon absorption. For wide bandgap structures, instead of single photon absorption, two-photon excitation is usually adopted since it allows better resolution, focus and reduced power loss. We employ two photon OBIC on the test devices to visualize the degradations surrounding the gate fingers in the active device area.

5.2 Details of the Test Environment

A. SAMPLE PREPARATION

Because of the metal layers and field plates blocking the active device area from the top, the laser tests need to probe the device from the backside. To enable access for the laser beam however, backside sample preparation needs to be done to open a window to the device chip area. The sample preparation is done in several careful steps.

Figure 5.1 displays the front and backside of a test device before the sample preparation process commenced.

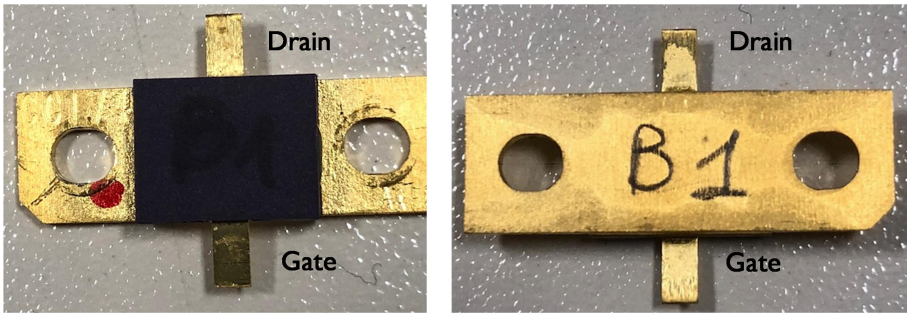

Figure 5.1: Front and backside views of a test sample before sample preparation

The first step was the removal of the top ceramic cover. The devices have a continuous backside source metal contact. Since the back layers need to be removed in order to enable the laser tests, the source contact would be destroyed. Hence, to preserve access to the source contact during the tests, alternate bondings needed to be made directly from the device chip on the front side. After this step, the front is sealed off with resin to protect the contacts and provide mechanical stability to the backside treatments.

Figure 5.2 (left) displays the exposed front side chip after the top ceramic cover was detached and (right) front side with resin after additional bondings were formed.

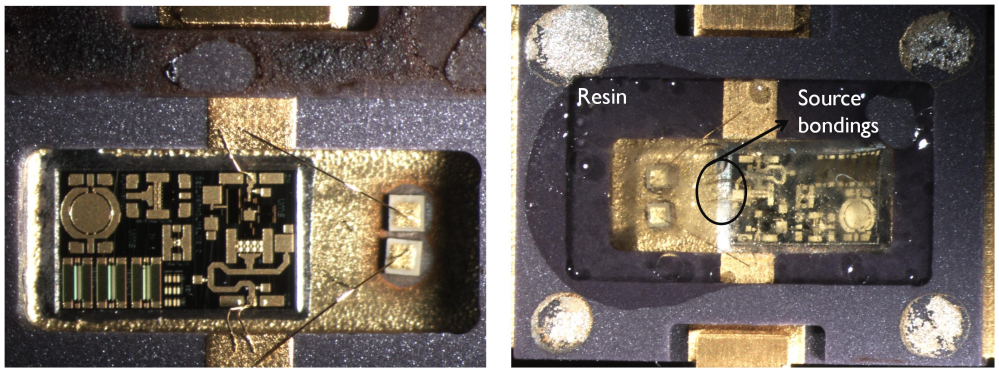

Figure 5.2: Front views of the device chip area (left) after the top ceramic cover is removed and (right) after additional bondings and resin are deposited

To attain an even, stable surface, the resin at the top was carefully rid of small bubbles and smoothed out carefully. From the backside, each layer needs to be removed gradually to reach the chip. A schematic of the different layers is presented in Figure 5.3.

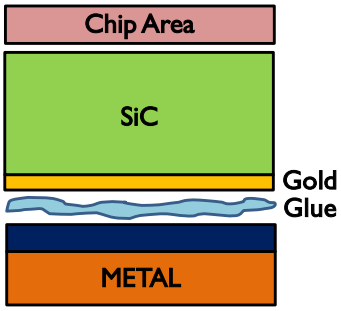

Figure 5.3: Schematic of the backside layers that required treatment during sample preparation

First, meticulous measurements of dimensions were taken to estimate the position of the chip, so that the drilling window is chosen accurately with the chip at its focus. The size of the window is a key concern: a bigger window minimizes mechanical constraint near the chip but drilling near the edges should be avoided as well to avoid edge cracking.

After the thick metal layer is removed, a thin and very hard layer comes next. Removing this layer while keeping the tool centered on the component is again a critical step because even slight mismatches in pressure produces cracks in the underneath chip. This is followed by glue, and then a thin gold layer, which is removed through careful polishing. Finally, the SiC substrate is reached which is thoroughly polished until the chip outlines are observed. The sample needs to be cleaned thoroughly after each step. Acetone and ultrasound cleaning is employed. Some attempts resulted in cracking of the chip area, which damaged the devices. However, comparisons on devices with successful sample preparations did not reveal any non-trivial changes in the electrical characteristics.

Figure 5.4 presents the (left) reconstructed image of the device package and (right) the backside view of a test device after sample preparation is complete.

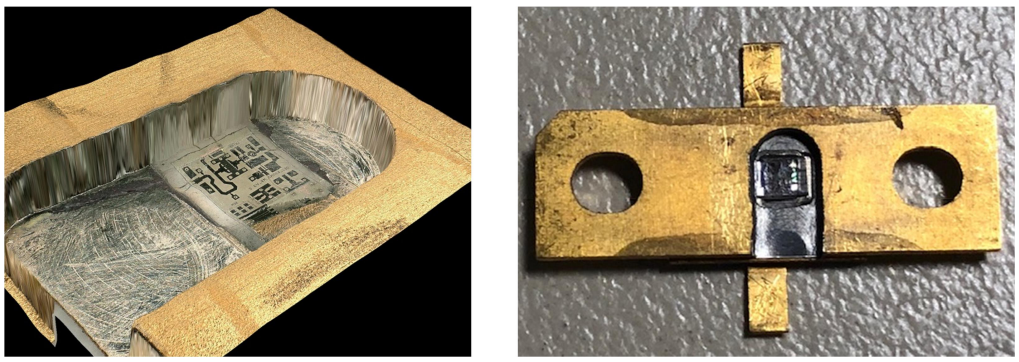

Figure 5.4: (Left) Reconstructed image of the sample after backside preparation and (right) Top view of the test device

B. BOARD FOR DEVICE CHARACTERIZATION

After the sample preparation, the board needs to be constructed to build biasing connections for possible test scenarios. Figure 5.5 illustrates the details of the board designed for the experiment with the equivalent circuit connections on the right. An image of the backside (in accordance with Figure 5.5) and front side views of the fabricated board is displayed in Figure 5.6.

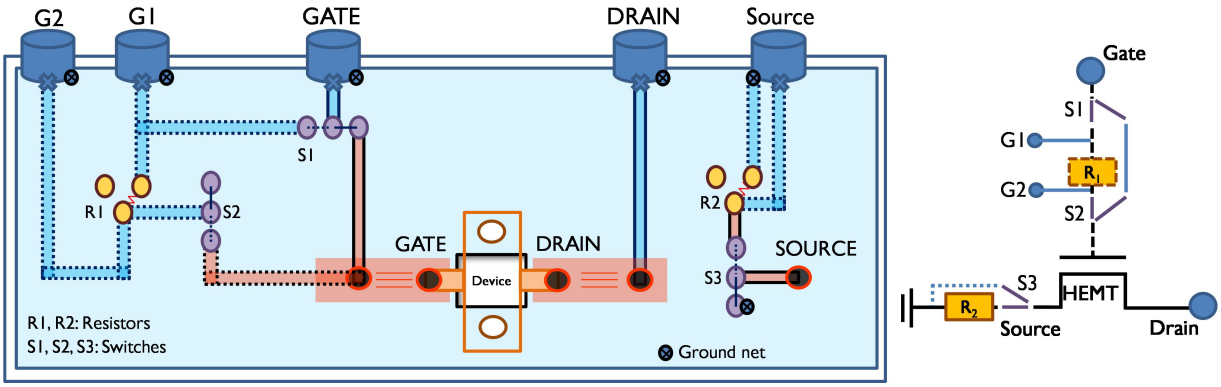

Figure 5.5: Schematic of the build test board

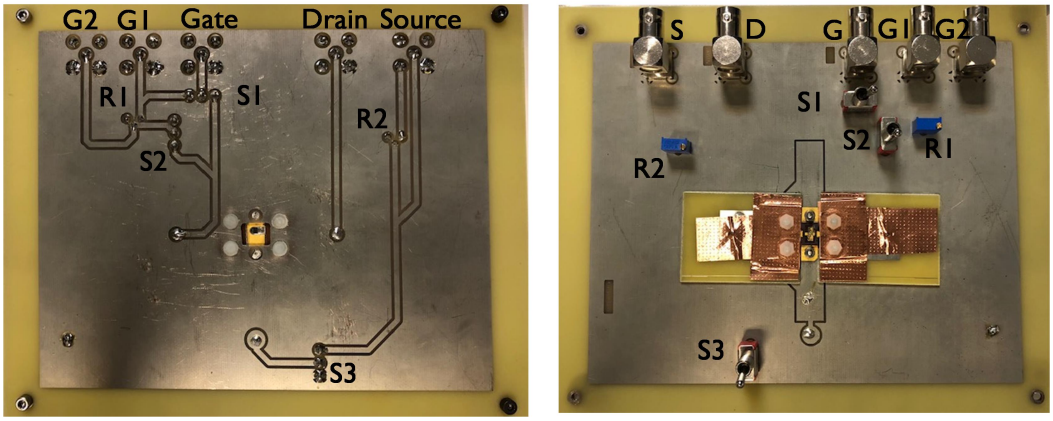

Figure 5.6: Backside and front side top views of the developed board

A hole is made in the printed circuit board to retain an opening on the device backside for entry of the laser beam. Screws and conductive tape are used to establish a good contact with the gate and drain metallic extensions protruding from the package (see Figure 5.4). The screw heads on the backside are flattened out to maximize the adjustable distance between the chip and the microscope objective that focuses the laser beam onto a chosen section of the active device area.

Coaxial connectors connect the device drain and gate terminals to the two source-measure inputs of the Keithley Sourcemeter 2612B. There is a common ground plane which connects all the coaxial grounds together as a net, and the source too when it is directly connected to the ground. Switch S3 creates an alternate pathway for the source contact to go through a resistor R2 before

reaching ground. Two switches S1 and S2 create an alternate path for the gate current to flow through a resistor R1 which enables G1 and G2 to serve as inputs to the oscilloscope during the OBIC tests. For the detrapping tests, the general connections are chosen wherein the gate and the drain outputs from the device are connected directly to the sourcemeter and the source is grounded.

C. ORGANIZATION OF LASER COMPONENTS

Though we explore different approaches to capture the trap effects, the fundamental set up for the coupled electro-optical characterization is constant and thus needs to be carefully assembled. There are several considerations in building a reliable, flexible system that can enable testing the board in an efficient manner, with special care on minimising the need for manual interference during the course of a particular test. The automation of the sequential electrical or optical characterizations is important since the time constants of the investigated traps are a crucial concern, especially for traps with very shallow energies.

The schematic in Figure 5.7 describes the building blocks of the central laser source. This is also the first block of the overall test bench.

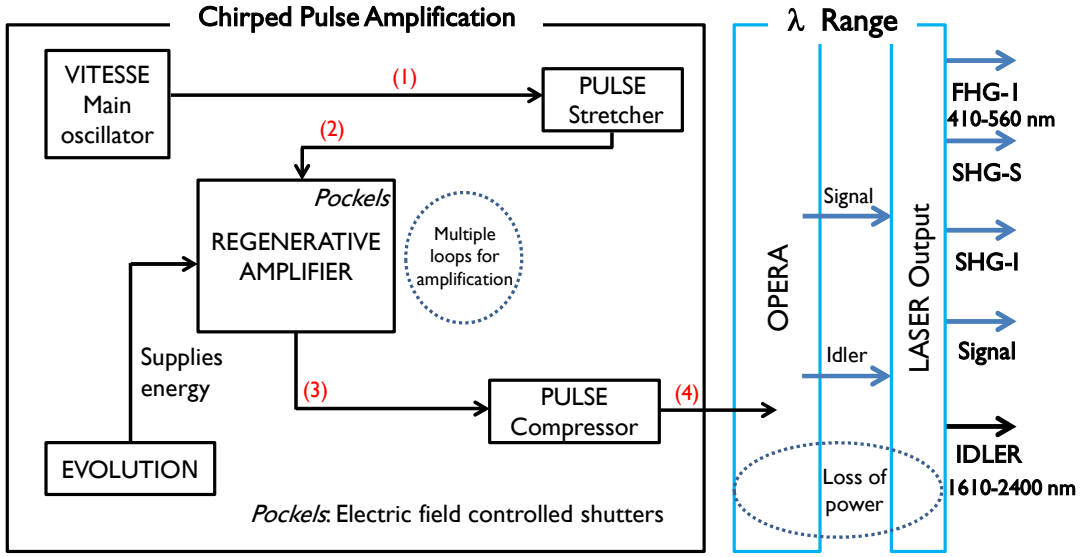

Figure 5.7: Schematic of the central block of laser generation which amplifies the power and chooses the wavelength of the emitted laser source.

A combination of several components forms the basis of the power amplification of the LASER source based on the principle of chirped pulse amplification [5.7]. This technique allows the generation of high power femtosecond pulses within reasonable peak intensities through temporal stretching of the LASER pulses before the amplification stage.

As displayed, the VITESSE block is the main oscillator which generates short laser pulses of high frequency. At this stage, the output power is very low. Before inputting the pulses to the regenerative amplifier which is fed energy from the EVOLUTION, the pulse stretcher increases the pulse widths. After the compressor restores the original pulse widths, we have high energy pulses of 1 kHz repetition rate at the output. The next couple of stages allow splitting the laser output into distinct ranges of wavelengths. For our trapping-detrapping tests, we use the infrared IDLER output with the chosen wavelength varying within 1610nm -2200 nm. For the OBIC tests (Section 5.4) performed at 550 nm, we use the FHG-I output.

Figure 5.8 describes the assembly of different components which represent the organization and control of the test system.

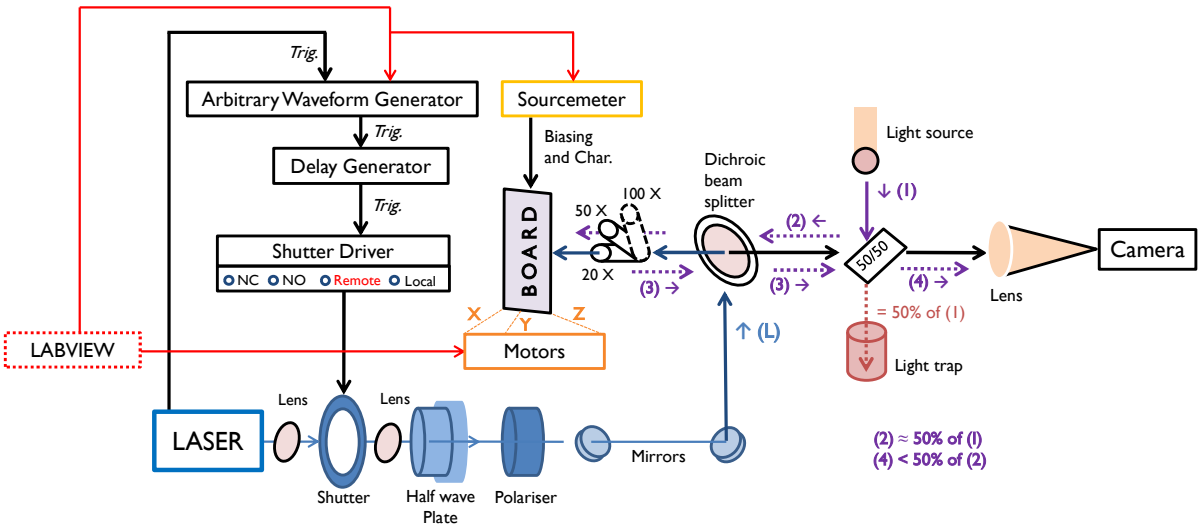

Figure 5.8: Schematic describing the mechanical assembly of the electrical and optical components that build the device test bench

The laser output of a particular wavelength travels to the shutter which is normally closed. When the shutter is open, the laser beam travels through the lenses before and after, which focus and collimate the beam. Next, it passes through the half wave plate and then the polariser which only has one axis to transmit the beam. The half wave plate [5.8], by rotation, alters the power of the linearly polarised beam at the input by changing its polarization state. The amount of transmitted power depends on the angle between the plate's axis and the polarization of the input beam, according to which it distributes the electric field. To reach the beam splitter, the light is manipulated through a set of mirrors which are optimised for the utilised wavelengths.

An internal signal from the OPERA block in Figure 5.7 acts as the trigger to the arbitrary waveform generator which then generates a pulse train locked in phase with the laser signal. This, in turn trigs the delay generator which drives the shutter.

The pulses are synchronized such that the shutter opens for just long enough to allow a single laser pulse to reach the device during tests. The shutter can also be driven to allow several laser pulses within a single opening window.

Labview also remotely controls the Keithley sourcemeter which comprises the electrical biasing and characterisation section of the setup. It is directly attached to the sample board which is set up for backside analysis. A separate Labview program controls the X, Y and Z motors connected to the mount to facilitate adjustment of the board and allow scanning of the device.

In order to focus the laser beam on the active area of device, we need to image and focus the microscope objective onto the device manually using the camera. The light source wavelength has to be chosen based on the laser wavelengths that are being employed.

The dichroic beam splitter needs to maximally reflect the laser beam coming from the mirrors, while being transparent to the light source that allows illumination of the device. On reflection, the laser spot size on the chip is 70-80 μm. Using a 20X microscope objective, we obtain an 80 μm diameter laser spot covering around 1/5 of the active device area. The power available at this stage depends on the chosen and lies within a range of 1.2 mW to 2 mW.

The imaging light source ((1) in Figure 5.8) first incidents on a 50/50 splitter which reflects 50% of the light onto the dichroic beam splitter (see (2) in Figure 5.8) and transmits the other 50 % onto a light trap to prevent parasitic light into the camera. The light passes through the dichroic splitter, through the objective and on the device. As the light returns (3) and is incident on the 50/50 splitter again, some power loss is to be expected. Finally, 50 % of (3) i.e. (4) is transmitted onto the camera to allow imaging, while the rest is reflected onto the light trap.

For the sets of detrapping tests, the employed laser wavelengths are 1610 nm and higher. The dichroic beam splitter is chosen to have high reflectivity beyond 1610 nm but has high transmission around 1000 nm. Hence, an infrared light source can be employed between 1100-1200 nm. For the OBIC tests, the employed laser wavelength is 550 nm. In this case, source light is also infrared. The beam splitter is changed, though some power loss is unavoidable in order to allow some transparency in the infrared range to the light source.

5.3 Laser Application: Modulation of Trapping Dynamics

In this section, the tests involving laser beam interactions with the active device, and their effects on trapping phenomena is described. On application to the device under test, the laser beam supplies energy by providing photons of a specific energy E_1 depending on its wavelength λ. Occupied traps that are energetically away from the conduction band E_C by an amount E_1 or less can

detrap if they absorb a single photon. Hence, by absorption of photon energies, we can induce detrapping in devices under test. By altering the wavelength or the initial electrical condition before the laser pulses are applied, the trapping phenomena within the device can be modulated to better comprehend the trap behavior in a given device.

A. ELECTRO-OPTICAL TESTING SYNCHRONISATION

The temporal synchronisation between the laser and electrical sections of the test set up are of critical importance. This section details how these characterisations are organized in order to best capture the effect of the incident laser beam on the test device.

Figure 5.9 presents the Labview program and the schematic of the electrical and optical sections in the basic sequence of activation. The core characterization occurs automatically as soon as the Labview program is hit to run.

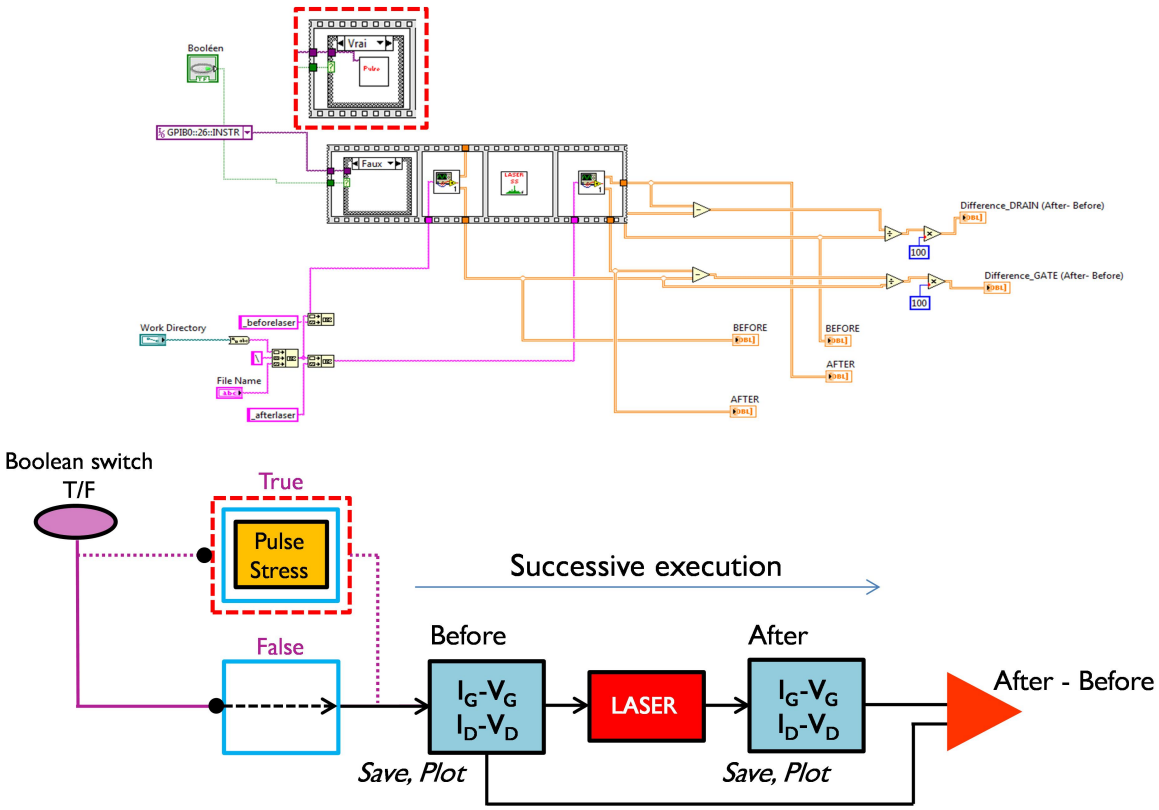

Figure 5.9: Basic flow of electro-optical characterization for the detrapping test methods

An I_G-V_G (V_G= 0 V to 1.5 V at V_D= 0 V) and I_D-V_D (V_D: 0 V to 6 V, V_G=-4 V to 0 V) pulsed characterization of the device is first performed by the Sourcemeter. This is the "Before" state of the sample device. Since the device after sample preparation is very thin and fragile, we limit exposure to high voltages. The pulse widths are 250 µs and 200 µs for the gate and drain bias.

These are the smallest pulse widths that could be supported by the sourcemeter for reliable results. The off-time for the pulses is 2 ms. With an effective biasing pulse time of 2.2 ms, the total time for a single iteration of an I_D-V_D and I_G-V_G characterisation takes approximately 0.5 s. The delay for the total "Before" block, including initializations and save operations is closer to 1s.

It is followed by laser application which involves opening and closing the shutter in Figure 5.8 for precisely long enough for a laser pulse to pass through and be incident on the device. The average delay for the laser block is 0.8 ms. In continuation of sequential execution, a second iteration of the identical I_D-V_D and I_G-V_G block is activated which takes measurements comprising the "After" state of the device. Both results are automatically exported and recorded in files. After the final characterization, any changes in device response owing to the laser pulse reflects in the "After-Before" data sets. By changing the laser wavelength, we obtain the device response for exposure to a certain photon energy that defines that particular wavelength.

The Boolean switch controls whether an initial stress is applied to the device under test before the first characterization. As we shall see for Section 5.3.B, when the switch set to False, no stresses are employed. The "After-Before"= ΔI_D or ΔI_G in this case is purely a response of the steady state device to an applied laser pulse. When the switch is set to true, there is an additional block before the first characterizations are performed. This block applies a stress pulse at V_G= - 10 V and V_D= 20 V. The pulse width is 200 μs. Single or multiple stresses can be applied to change the initial trapping state before the first characteristics are performed. The following LASER pulse then reflects the device response to available laser energy, but under a different transient state of trapping.

B. BASIC RESPONSE

The general response of the device when a laser pulse is applied in described in Figure 5.10. The setup is identical to Figure 5.9 with the Boolean switch set to false. For ease of comparison, the difference in I_D is shown at V_G= 0 V. At lower V_G values, the effect is similar but smaller. Sometimes the low V_G measurements also display random fluctuations which harm the integrity of the achieved signal. The measurements at V_G= 0 V are the most stable and representative of the device response.

From Figure 5.10 (left) we can observe that for a laser pulse at λ= 1700 nm (E= 0.72 eV), a detrapping occurs in the device, reflected in the higher I_D in the "After" state. The inset displays ΔI_D equal to the "After" laser – "Before" laser response (see. Figure 5.9), which is positive.

$$\Delta I_D = I_D(After\ laser) - I_D(Before\ laser) \tag{5.1}$$

This is a characteristic response when laser energy induces a detrapping within the device. Figure 5.10 (right) shows the ΔI_D response for λ= 2200 nm (0.56 eV). In this case, ΔI_D is negative.

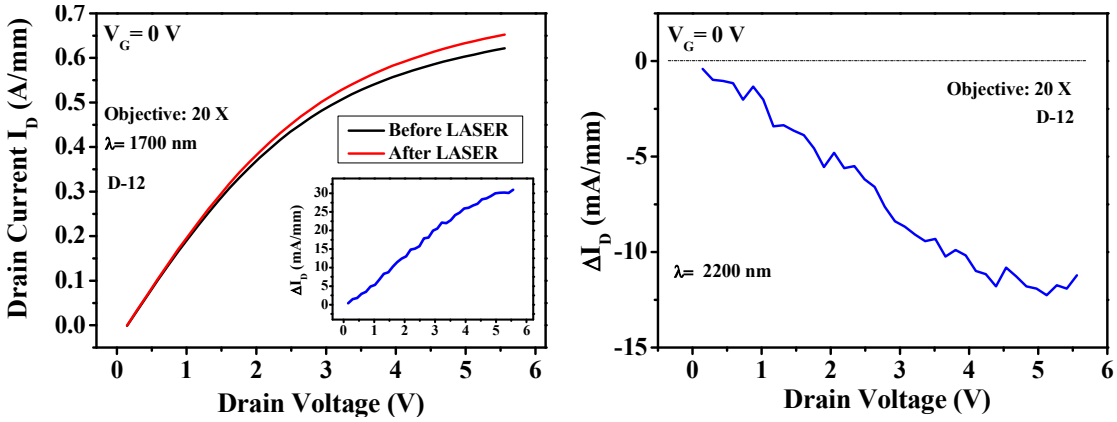

Figure 5.10: (left) A typical device response at λ= 1700 nm showing a detrapping in I_D-V_D at V_G= 0V, and a positive ΔI_D. (right) Typical ΔI_D for a no-detrapping scenario, here for λ= 2200 nm.

Thus, in this case, the laser triggers no detrapping. The "After" characterization is only a sweep which induces additional trapping in the device leading to the negative ΔI_D.

Since each characterization of the device introduces some amount of trapping, this implies that the observed positive ΔI_D (obtained by the "After" measurements) for a laser induced detrapping response could be lower than the real detrapping magnitude. Unavoidably, the quantifiable ΔI_D is equal to (actual laser-detrapping)-(retrapping due to the "After" characterization). In Figure 5.10 (left) therefore, the "After" state I_D due to the detrapping occurrence at 1700 nm is around 30 mA (observed maximum ΔI_D at 1610 nm) + 14 mA (negative ΔI_D for no detrapping in Figure 5.10 (right))= 44 mA higher than what it would have been in absence of the laser.

Laser Application with 20 X Objective

The chosen microscope objective for focusing the laser on the device is generally 20 X since it allows visualization of the active device area and does not appear to degrade the device. Laser applied at 50 X or higher puts a high intensity in a very small device area, and was observed to cause small damages to the sample structure. Using a 5 X microscope would have allowed the laser spot to cover a larger portion of the device area. However, the laser power density (photons per unit area) near the active device region is quite low at 5 X. Hence the responses are not strong enough to be conclusive.

Thus, in the following sections, a 20 X objective was the effective choice. Figure 5.11 presents a view of the device imaged at 20 X (left) and the usual laser spot size which is incident on the sample. This is the area of maximum laser intensity, although the laser effects occur in surrounding areas as well. The spot location is occasionally changed, but is always focused near the edges of the gate fingers as shown in Figure 5.11 (right) to enhance trap response.

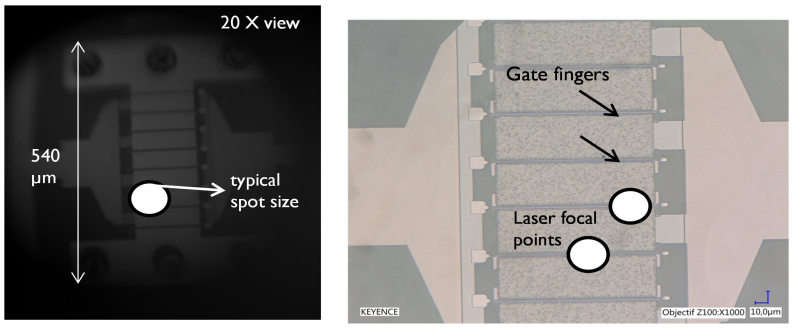

Figure 5.11: Imaging of a test device at 20 X (left) and (right) a typical laser spot size and location.

C. RESULTS: EXTRACTION OF DETRAPPING ENERGIES

GaN HEMTs are often vulnerable to small dispersions in output characteristics over periods of time. Before laser pulses were applied on the device, some consecutive characterizations were performed in an attempt to stabilise the initial electrical response before the laser pulses are applied.

By observation of the device response to the application of laser pulses for a range of wavelengths, it is possible to identify the photon energies that induce a detrapping response (i.e. a positive ΔI_D). A negative ΔI_D indicates an absence of trap energies close to the applied wavelength. Several iterations of laser pulses, as illustrated in Figure 5.12 are applied at any given wavelength to verify whether any observed detrappings are reproducible and not a consequence of random changes in laser power levels or other setup constraints.

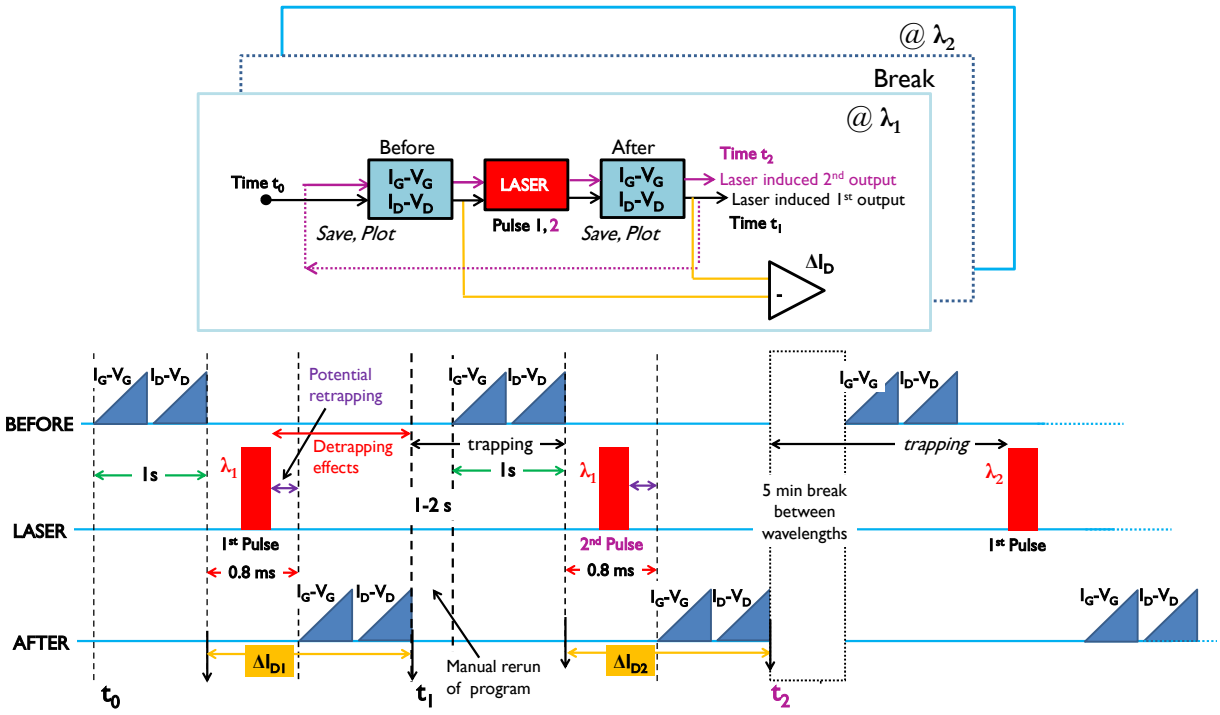

Figure 5.12: Description of the sequence in which laser pulses are applied to the test device illustrated by a block schematic and the corresponding chronograph

During drain current spectroscopy studies on GH-25 devices, trap energies at 0.48 eV and 0.66 eV were identified [5.9]. This work was performed for a wavelengths ranging from 2300 nm (0.53 eV) to 1610 nm (0.77 eV). The impact of a particular laser pulse on I_D is estimated by ΔI_D, as illustrated in Figure 5.12. Several loops of the basic characterisation sequence are activated. When the first "After" output is obtained at time t_1, the program is hit to rerun as soon as possible (1-2 s) to obtain another response to a second laser pulse at time t_2. Since each I_G-V_G+ I_D-V_D block requires 1 s to finish execution, the minimum time elapsed between two consecutive laser pulses (Pulse 1 and Pulse 2 in Figure 5.12) is in the order of 5-6 s. The time between the end of a laser pulse and the beginning of the "After" characterization is set by minimum communication delays between the setup and the computer. This is the limiting factor to observable trapping constants. Traps that might retrap within this time interval (≈ 0.4 ms) cannot be detected by this setup.

After the response is obtained for the initial wavelength, there is break of 5 minutes before characterisation is repeated at the next λ (see Figure 5.12). The break duration was chosen to allow the device to somewhat return (retrap) to a steady state condition, and allow the "Before" condition for the following wavelength to be isolated from changes (detrappings) produced in response to previously tested wavelengths. However, as will be discussed at the end of this section, this duration might not be enough to obtain independent wavelength responses, and a strong retrapping of the device should be performed before a new laser wavelength is tested.

As laser wavelengths become shorter, corresponding photon energies are higher and the detrapping response should get stronger. For example, when a laser at 1610 nm i.e. 0.77 eV is applied: in addition to a trap energetically located at 0.77 eV, a trap located at 0.35 eV might also get detrapped if it absorbs a photon of 0.77 eV. This is why the characterisation was started at higher wavelengths, and gradually moved towards lower wavelengths to identify trap contributions with shallower energies. Figure 5.13 summarises the response of a device to varying wavelengths between 2100 nm and 1610 nm by plotting ΔI_D at V_G= 0 V.

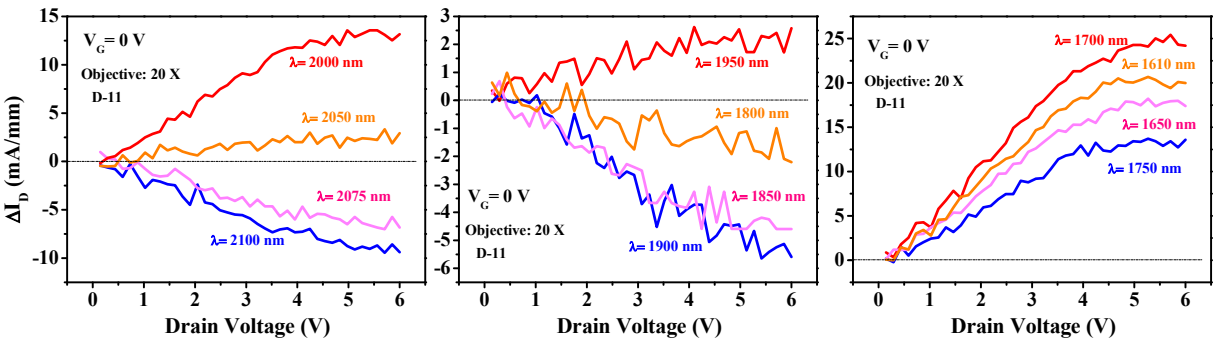

Figure 5.13: Device response to applied laser wavelengths between 2100 nm and 1610 nm

Strong detrapping occurrences in Figure 5.13 are observed at energies of 0.6 eV (λ= 2050 nm), 0.62 eV (λ= 2000 nm), 0.7 eV (λ= 1750 nm), 0.73 eV (λ= 1700 nm) to 0.75 eV (λ= 1650 nm) and 0.77 eV (λ=1610 nm). No detrapping responses are seen for λ= 2100 nm, 2075 nm, 1900 nm, 1850 nm and 1800 nm. The responses at λ= 1950 nm and 1800 nm are too weak to be conclusive.

It is interesting to note that the detrapping response at 2050 nm (0.6 eV) and 2000 nm (0.62 eV) is higher than for wavelengths between 1900 to 1800 nm (0.65 eV to 0.69 eV) which have higher energies. It could be because of the presence of specific trap energies at 0.6 eV and 0.62 eV which display a stronger response to the exact photon energy. Since the laser has a very small pulse width and hence incident on the device for a very short time, possibility of detrapping responses for photon energies varying from respective trap energies could be lower, even if the available photon energies are slightly higher. The laser power at these energies is also low, around 1.2 mW maximum. For this particular case, the photon energy could be 0.09 eV higher at 1800 nm than at 2050 nm, which might not be high enough to de-occupy traps with a different time constant. This would not be the case in luminescence studies, where the wavelengths of the light source are not as precise, and the light energy is applied for longer durations.

However, detrapping magnitudes do get stronger at lower wavelengths around 1700 nm to 1610 nm for all the tested devices. At these λ, when energies are significantly higher, accompanied by an improvement in laser power (closer to 1.8 mW), the detrapping response should be a combination of detrappings with the specific (corresponding to λ) as well as shallower trap energies. The detrapping (ΔI_D) is seen to be slightly weaker going from 1700 nm (0.73 eV) to 1650 nm (0.75 eV) and then rises slightly at 1610 nm (0.77 eV). This might indicate probable trap energies present at 1700 nm and 1610 nm, since the contribution from shallower traps would also affect 1650 nm.

Multiple Laser Pulses

As illustrated in Figure 5.12, multiple laser pulses were applied to check reproducibility of observed detrappings at the tested wavelengths. Figure 5.14 compares the ΔI_D responses for (left) some wavelengths with no detrapping responses and (right) with significant detrapping occurrences for two successive laser pulses (Pulse 1 and Pulse 2 in Figure 5.12).

For the no-detrapping wavelengths, only the performed gate and drain characterizations have an effect, and the laser has no effect. The trapping due to the first sweep induces the maximum negative ΔI_D. For successive characterizations, the effect degrades and saturates over time. For the detrapping wavelengths, the output after the second laser pulse is usually found to be smaller than the first. For some cases however (for 2050 nm in Figure 5.14), the difference is quite nominal.

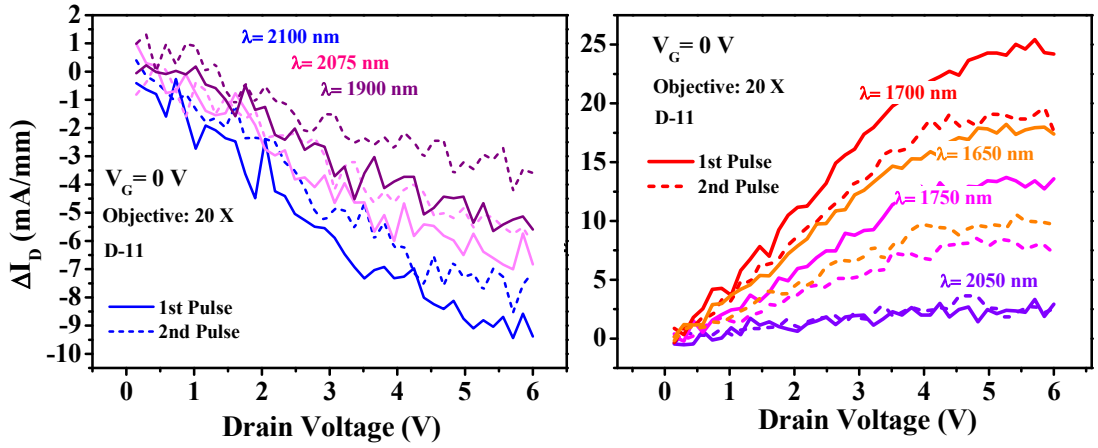

Figure 5.14: Comparison to response deviations for successive laser pulses at λ= 1700 nm, 2050 nm

For λ= 1750-1650 nm, the detrapping response to the second pulse (ΔI_D), although still positive, is noticeably reduced. This indicates that the trap dynamics in the time between consecutive laser pulses (time difference of 5-6 s) is variable, and dependent on λ.

Figure 5.15 presents how trap charging times can influence the intermediate state of I_D between the two laser pulses, and thus control the final ΔI_D values.

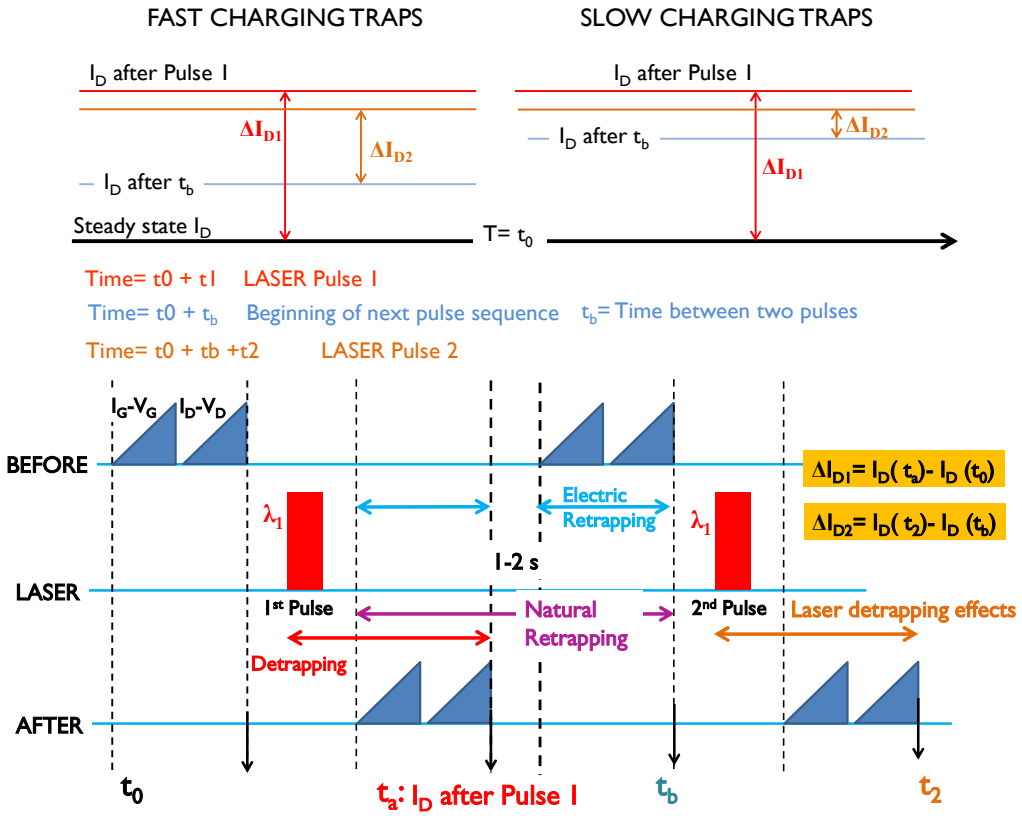

Figure 5.15: Schematic illustrating the difference in ΔI_D for consecutive laser outputs when detrapping (left) fast or (right) slow charging traps.

Since there are delays within and between the blocks (see. Figure 5.12), the "After" device state at time t_a (Figure 5.15) is slightly different from the "Before" state at the start of the next iteration. A portion of traps that were detrapped by the first laser pulse might naturally retrap before the next iteration, starting just after the laser. In addition, the two I_D-V_D+ I_G-V_G sweeps induce electrical retrapping as well. Hence, I_D falls to an intermediate state between the two laser pulses. When the second laser pulse again detraps the associated traps, I_D recovers again as well. Usually, the first pulse would be associated with the highest ΔI_D (as can be observed from Figure 5.14), which quantifies the maximum amount of detrapping from the steady state of the device. The magnitude by which the second laser pulse response varies from the first is thus linked to whether the detrapped traps are slow or fast charging traps.

Let's assume for Figure 5.15, similar densities of traps, and that the applied laser wavelength is capable of detrapping the corresponding slow or fast charging trap. If the first laser pulse results in detrapping of fast charging traps, these traps are susceptible to immediate retrapping. Hence, I_D would again fall to a low value before the next pulse is applied. This is the I_D state at t_b in Figure 5.15 (left). The next laser pulse will again detrap these traps to reach a high current state close to the I_D output after Pulse 1. In this case, ΔI_{D2} is not so different from ΔI_{D1}.

In the second case, (see. Figure 5.15 (right)) if the traps detrapped by the first pulse have longer charging constants, the fall in I_D at the intermediate state is very small. In this case where I_D after the first pulse is stable (I_D at $t_b \approx I_D$ after pulse 1), detrapping due to the second laser pulse will be very limited, since occupied trap densities will still be quite low. Hence the second $\Delta I_{D2} << \Delta I_{D1}$.

Generally, shallow traps could be expected to have low charging time constants. However the spatial location of the traps contributing to the detrapping response could also be significant. Traps at the surface or close to the channel might retrap faster than buffer traps.

Since, the detrapping response at low wavelengths (λ= 1700-1610 nm) is usually a combination of excitation of several traps, it is reasonable to expect that at least some amount of these traps will be slow charging. This could explain why the deviation between output responses of consecutive laser pulses is usually substantial at low λ.

The ΔI_D results, such as in Figure 5.13, are compiled for a second device subjected to a similar test scenario (application of two laser pulses for each wavelength followed by a change in wavelength) between λ of 2050 nm to 1610 nm. The responses are displayed in Figure 5.16.

Detrappings are observed at energies of 0.62 eV (λ= 2000 nm), 0.73 eV (λ= 1700 nm), 1650 nm (0.75 eV) and 1610 nm (0.77 eV). No detrapping responses are seen for λ=1900 nm -1800 nm.

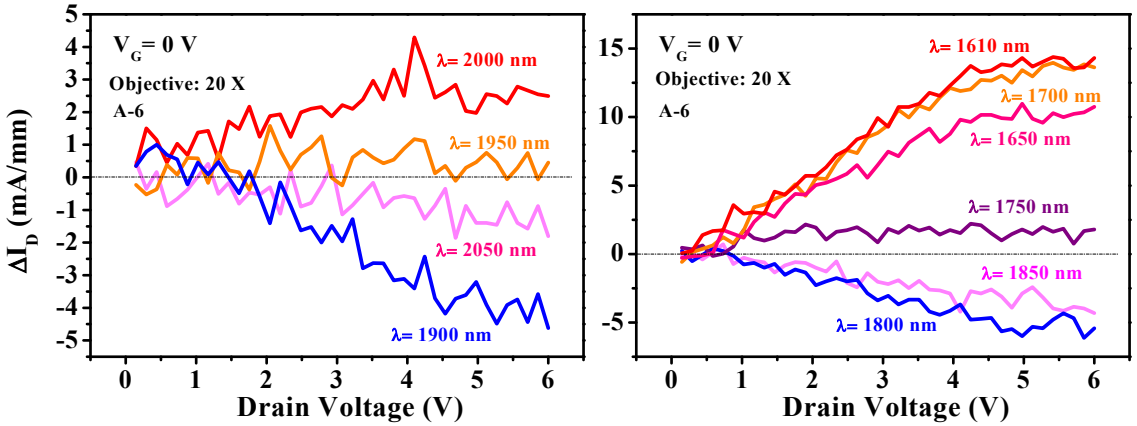

Figure 5.16: Device response to applied laser wavelengths between 2000 nm to 1610 nm

The responses at λ= 2050 nm, 1950 nm and λ= 1750 nm are inconclusive. For this device too, the deviation between the first and second laser pulse outputs has been generally found to be higher for lower tested wavelengths.

Verifying the detrapping response

In the discussed laser application approach (as illustrated in Figure 5.12), unavoidably, there is a notable time interval between the first characterisation at ≈ 2200 nm to the final characterisation at ≈ 1610 nm. Though the power of the laser beam is measured at the beginning, it cannot be monitored at small intervals since power measurements involve changing the setup and takes considerable time. A high ΔI_D was observed for all the tested devices close to 1610 nm.

To ensure that the detrappings at the lower wavelengths are not occurring due to random temporal changes in laser power levels, we can alter the sequence of applied wavelengths. A higher laser wavelength could be applied to the device after a low wavelength to verify if the detrapping response is still stronger for the low λ value. Another approach to ensure that I_D changes are not due to setup induced spikes in current is to perform a normal characterisation just prior to the laser application. Since, this would definitely be a trapping response, the contrast should be clearer. This is observable from the schematic for (no-laser) sweeps followed by (with-laser) sweeps in Figure 5.17.

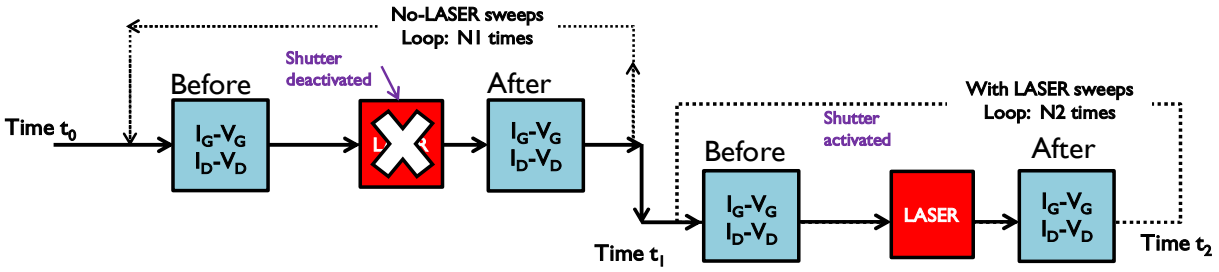

Figure 5.17: Schematic illustrating the concept of applying no-laser sweeps (repeated N1 times) prior to the actual laser application (repeated N2 times, if multiple laser pulses are applied)

A No-Laser sweep comprises a "Before" and "After" characterization as in Figure 5.9 except that the shutter is kept closed during the laser application block. These sweeps can be repeated multiple times (N_1 in Figure 5.17).

When the shutter is activated again at time t_1, the following laser characterisations (With-Laser) verify that setup or environmental constraints remain identical and the difference between no-laser and with-laser outputs (obtained at time t_2) is entirely attributable to the laser application.

Figure 5.18 (left) presents the ΔI_D results when the device was tested at 1610 nm and then followed by a change in wavelength to 1780 nm (λ_1 = 1610 nm and λ_2= 1780 nm, in Figure 5.12). Figure 5.18 (right) presents ΔI_D when a no-laser characterisation (N_1=1 in Figure 5.17) precedes a single laser pulse application at 1700 nm (N_2=1 in Figure 5.17).

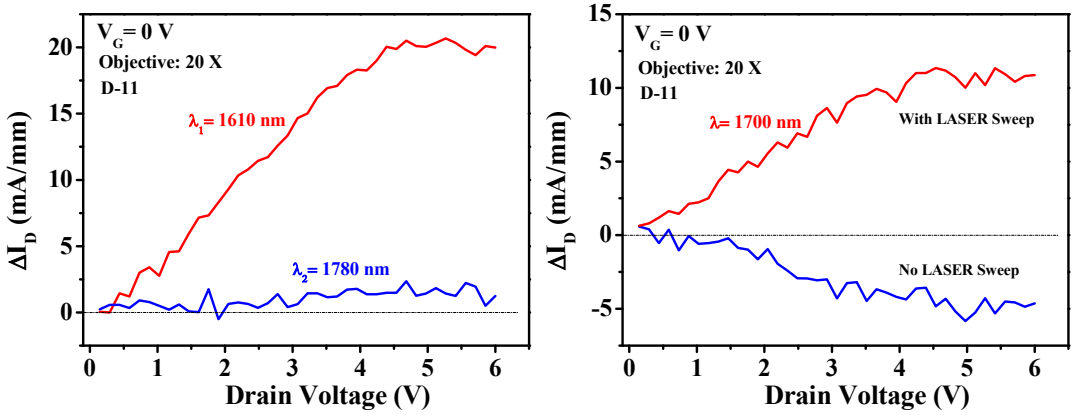

Figure 5.18: Approaches to verify laser-induced effects: (left) a change in wavelength from low to high and (right) a no-laser sweep preceding a with-laser sweep

The low ΔI_D observed at 1780 nm is similar to the response obtained earlier for the device in Figure 5.13 for λ = 1800 nm when λ was being decreased from 2200 nm to 1610 nm. The equivalence validates that the stronger detrapping response (transient from a trapped to a detrapped state) obtained around 1610 nm is due to changes in trap occupations. In Figure 5.18 (right), we see that the ΔI_D response for the no-laser sweep is negative. This again validates the positive ΔI_D observed immediately after at λ = 1700 nm, since the rest of the setup remains identical.

Change in Approach: Application of No-Laser sweeps prior to Laser Pulses

As we have been discussing, the no-laser sweep acts similar to a trapping occurrence. Thus, multiple bias sweeps act as a kind of stress to the device. Since the application of different laser wavelengths in succession could be changing the initial trapped state, applying no-laser sweeps is an effective way to make sure that the device is in a substantially trapped condition prior to application of the laser pulses at a particular wavelength.

In this way, the "Before" condition of the tests at each wavelength could be very similar. The associated detrapping response obtained is thus stronger and more distinctive. Hence, a change in the approach can be made to apply multiple no-laser pulses (N_1= 3 in Figure 5.17) then apply multiple with-laser pulses (N_2= 3 in Figure 5.17). The chronogram for the process is demonstrated in Figure 5.19.

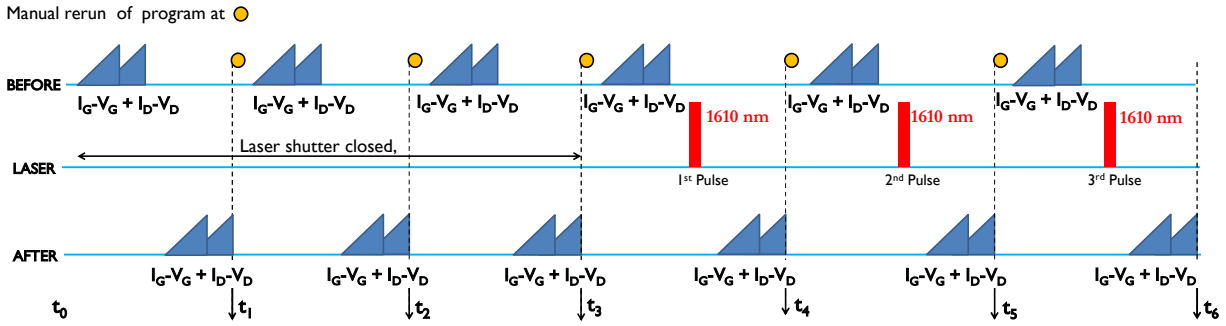

Figure 5.19: Schematic for application of three no-laser sweeps before three laser pulses

Three iterations of the basic "Before and "After" characterizations are performed to get the no-laser outputs at t_1, t_2 and t_3. Then, the laser shutter is activated so that it will open during the laser block in Figure 5.17. Three (with-laser) iterations are performed at a particular wavelength, outputs of which become available at t_4, t_5 and t_6. The entire sequence shown in Figure 5.19 would have to be repeated for a different wavelength, after a break period. The results for device A4 are presented in Figure 5.20 for λ = 1610 nm.

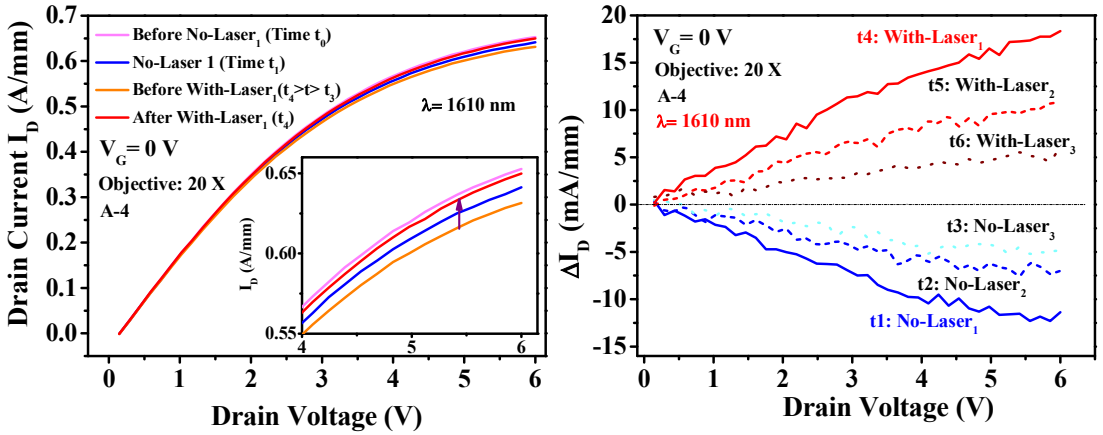

Figure 5.20: Device response on application of three characterizations with no-laser followed by three laser pulses at λ= 1610 nm (schematic in Figure 5.19)

On the left, we can visualize the change in I_D as the characterisation progresses. The first no-laser sweep decreases the I_D substantially. The next two no-laser sweeps slightly add to the overall trapping although some amount of natural detrapping might also be occurring during this interval (t_1<t<t_3), acting as a limit to the decrease in I_D, and hence total negative ΔI_D.

From Figure 5.20, we can see that the device is in a high trapped state (Curve: Before With-Laser$_1$) just prior to the application of the first laser pulse. At this point, I_D is at its lowest.

On the first laser pulse, most of the fall in I_D is immediately recovered (at time t_4). ΔI_D for the first laser pulse is thus quite high. For the second and third laser pulses, the effect slowly degrades. This is reflected in the ΔI_D characteristics on the right obtained at t_4, t_5 and t_6.

With this new approach, the device measured in Figure 5.16 is re-characterised. The ΔI_D results for wavelengths of 1800 nm, 1750 nm and 1610 nm are presented in Figure 5.21, compared with the previous responses obtained (from Figure 5.16) without employing no-laser sweeps.

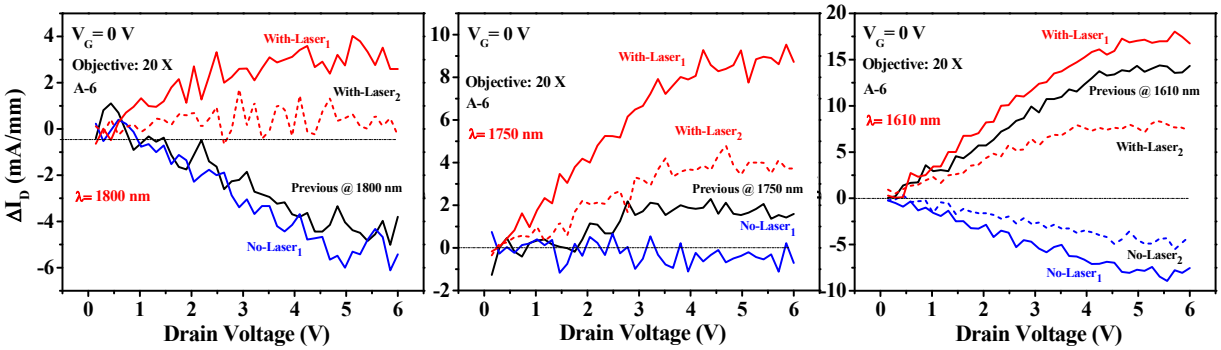

Figure 5.21: Re-characterization of the device from Figure 5.16 with the (no-laser) followed by (with-laser) approach for the wavelengths of 1800 nm, 1750 nm and 1610 nm

It is clear that the responses for 1800 nm (0.69 eV) and 1750 nm (0.71 eV) have improved and ΔI_D values are higher. From the earlier analysis, the response at 1800 nm (0.69 eV) yielded a negative ΔI_D. Now however, it displays a weak detrapping. The application of the no laser sweep to bring the device into a trapped state just prior to obtaining the laser response might have unmasked a detrap contribution from shallower traps. Or, the positive ΔI_D could be due to the appearance of a new trap activated only due to the prior no-laser sweeps.

For λ = 1750 nm, earlier results were inconclusive since ΔI_D was close to zero. Due to the strengthened response with no-laser sweeps, this wavelength can now be assuredly associated with a detrapping response. For λ = 1610 nm, the results are consistent with the previous one. Overall, the application of no laser sweeps is found to be a better approach since it enables a clearer demarcation.

Intermediate Perspectives

The above approach can be useful to gain an idea of the dominant trap energies present in GaN HEMTs. Since the study is carried out for a stable device state, the responses are reflective of traps that are generally occupied for normal device operation. For the entire device set, we observed strong detrappings at high energies (0.72 eV-0.77 eV) for all the investigated devices. The laser

powers available at lower wavelengths is usually higher, so a portion of the ΔI_D magnitude could possibly be due to a more active laser application. A contribution from traps having shallower energies is also expected. However, the general nature of ΔI_D well-reflects the existing trapping components. The responses at lower energies (higher wavelengths) were variable and unique to each device. For the next section, stresses that activate higher trapping occurrences are used to further study the laser-induced detrapping transients.

D. LASER INDUCED DETRAPPING AFTER ELECTRICAL STRESS PULSES

In this section, two kinds of stresses are employed to alter the initial trapped state of the test device preceding the laser pulses. Here onwards, gate characteristics are also compared along with changes in I_D to capture any insight into the trap mechanisms responsible for the belly shape.

The first kind of electrical stress applied is a trapping pulse of 200 μs with the device biased beyond pinch-off at V_G= -10 V and V_D= 20 V. With the reverse biased gate, the pulse activates an instantaneously higher probability of trap occupation, meaning that the "Before" state of each characterisation will have greater and more varied trap contributions. This is referred to as the application of pulse stresses. Repeated no-laser sweeps are also considered as valid stressing conditions, though trapping capability in this case is expected to be limited. These are called sweep stresses, as previously introduced, and discussed in detail in the next section.

So far, the laser detrapping approach was performed at a steady initial device state. Thus, the responses were due to traps that were occupied in steady state with dominantly long time constants. It required a laser pulse to change their occupations, and induce a detrapping. Stress causes an increase in the trapping probability for traps with lower time constants, which then allows us to study the effect of laser in such conditions. ΔI_D is calculated relative to the stressed characteristic in these new scenarios, and is specifically defined in each case. It is calculated in variable ways to best capture and understand the detrapping transient for a given condition. Also, devices are subjected to characterisations in certain chronologies to extend the discussion on particular observations. These factors are explained along with other relevant details for each subsection independently.

Time induced Recovery from Stress Pulses

Before observing the effects of laser following stress application, it is essential to understand how these electrical stress pulses (pulse width: 200 μs, V_D= +20 V, V_G= - 10V) affect the trapping state of the test devices. The following schematic in Figure 5.22 describes the general process of applying pulse stresses to induce greater trapping, followed by a time based recovery process.

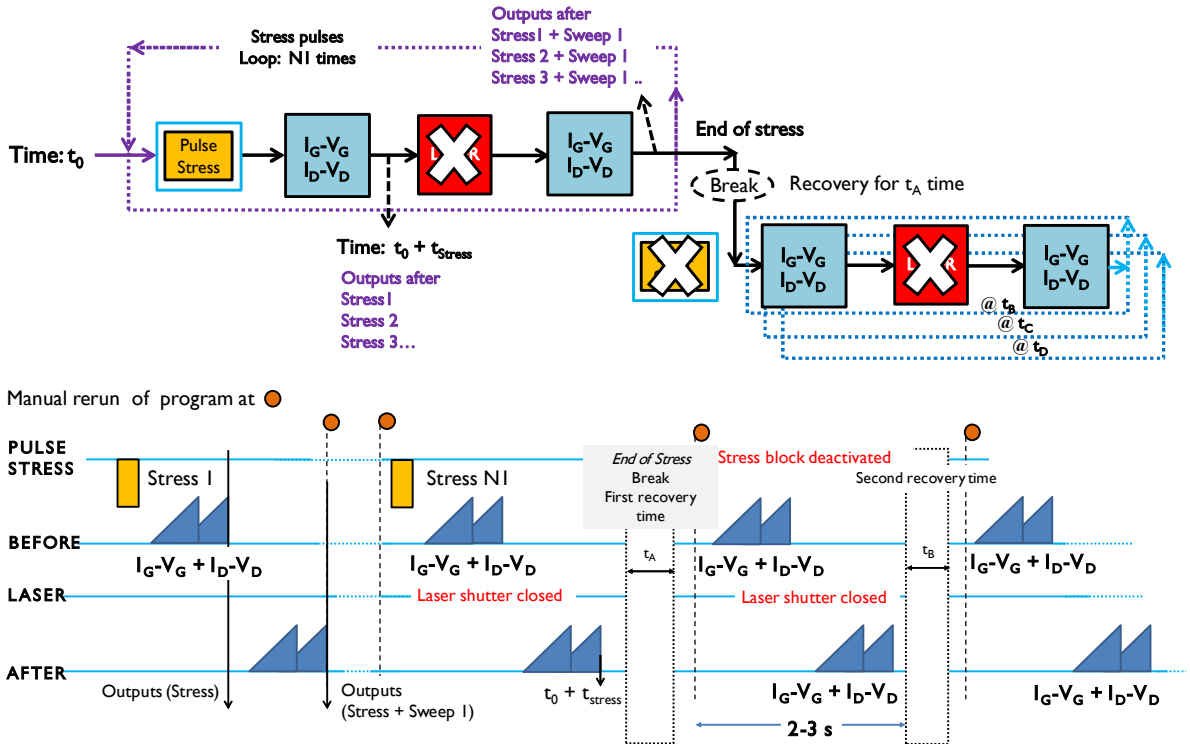

Figure 5.22: Schematic describing activation of stress pulses to induce trapping followed by time-based recovery, along with the process chronogram

Throughout the whole process, the laser shutter is kept closed. First, a number of stress pulses are applied (N_1 times) to get the responses of each stress after the first I_G-V_G + I_D-V_D block. The stressed response after a second I_G-V_G + I_D-V_D characterisation can also be obtained (Stress + Sweep 1) as demonstrated in Figure 5.22.

When the stress application is complete, the pulse stress block is deactivated and the execution is begun from the first I_G-V_G + I_D-V_D after waiting for the first recovery interval t_A. The two I_G-V_G + I_D-V_D blocks characterize the device again after further waits of t_B, t_C and so on to capture the gradual recovery in the trapped device I_D with time.

Figure 5.23 describes I_D variations that occur during three stress pulses on a test device. Hence, only the first (until "end of stress") section of the process in Figure 5.22 is discussed.

The first pulse stress notably reduces I_D by activating traps (Stress 1). This is followed by a second sweep which slightly reduces I_D further. After the pulse stress block, the process essentially constitutes a no-laser sweep since the laser is blocked. On application of pulse stress 2, I_D falls further. However, after the sweep in continuation of Stress 2 and before the third pulse stress can be applied, a small delay is present and the device state shows a minor recovery as seen in the inset for the condition Stress 2 + Sweep 1. This indicates that the traps activated by Stress 2 onwards have very small trapping time constants.

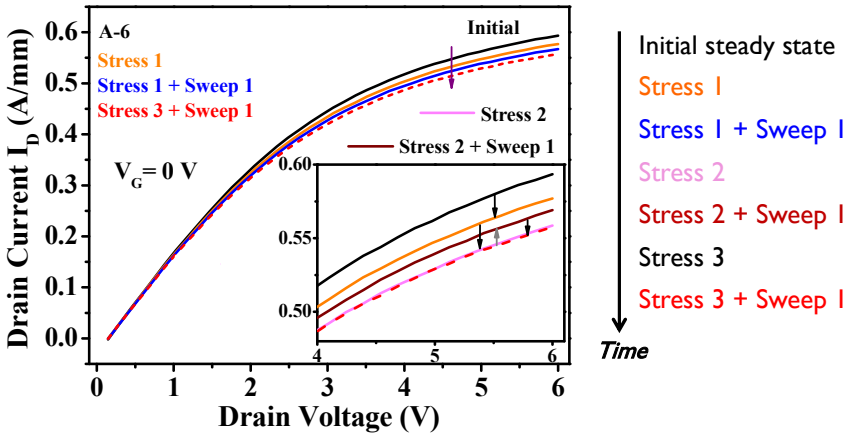

Figure 5.23: Variation of I_D after application of three stress pulses on a test device

On the third pulse stress, these traps are retrapped as I_D falls again to the lowest value (also achieved after Stress 2) achievable with these pulse parameters. This value seems to be stable, since further stresses do not notably cause any further worsening in I_D.

In the device of Figure 5.23 , there is an observable trap presence with very small recovery times. The trap components differ however in different devices. For example, Figure 5.24 presents the recovery in a test device, represented by ΔI_D for recovery times between 3 minutes and 24 hours following four stress pulses (N_1= 4 in Figure 5.22).

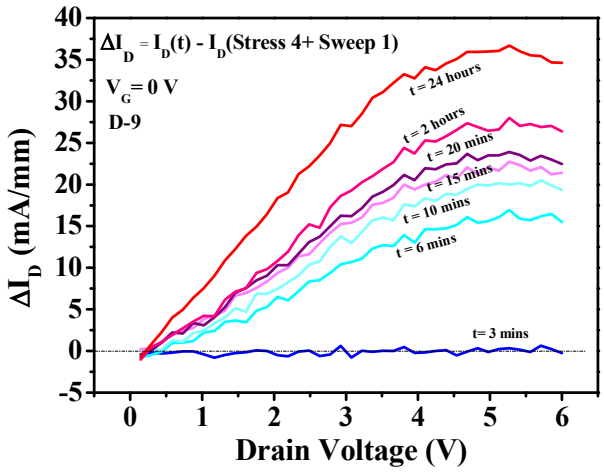

Figure 5.24: Recovery time constants of stress pulse activated traps with respect to the initial curve

This discussion now deals with the second part (right of "end of stress") of the process described in Figure 5.22. ΔI_D is the difference in response at a given recovery time with I_D state at the end of four stress pulses (Stress 4+ Sweep 1). In the device of Figure 5.24, a very small fraction detraps naturally within three minutes. A laser pulse would detrap most of the traps within a 3-4 s interval. A major amount of traps display time constants between 3 and 6 minutes. If we were testing laser responses at different wavelengths in turns, it would take around 6 mins to change from one

wavelength to another. In the absence of no-laser sweeps/stresses before each laser application, these traps (discharging by 3-6 minutes) might have detrapped automatically before we found the correct wavelength to detrap them. Hence, it is important to maintain the traps in their occupied states when each laser beam is incident, irrespective of wavelength. Beyond 6 minutes, I_D levels then improve slowly (Figure 5.24). Energetically deeper traps are expected to be the contributions behind the detrapping between 2 to 24 hours. After 24 hours, the device is almost recovered. Thus, without no-laser sweeps or stress pulses to re-activate the saturated trapping state of the device, an accurate technique would be to wait for 24 hours after a laser test, before a second laser wavelength is employed. This would ensure that this device is always in its initial, stable state when the laser attempts to induce a change.

On application of a high energy laser pulse, such as λ= 1610 nm, all the trap components activated during the stress pulses should be expected to detrapped together. Hence, the insight into the detrapping time constants of these stress pulse activated traps helps to understand how the laser detrapping alters the trapping dynamics in a device. If a laser pulse were to immediately follow the final stress pulse, instead of allowing it to recover naturally, the potential of the chosen laser wavelength to detrap the complete set of trap contributions could be captured (except natural detrapping effects that occur within 2-3 s: the time a laser pulse needs to reach the device after the last stress application)

Laser induced Recovery from Stress Pulses

Figure 5.25 illustrates the process used in this section to follow the stress pulses with one or more laser pulses and observe the associated responses. The approach is similar to Figure 5.22, except that the time based recovery section loop is replaced with incident laser pulses (number of laser pulse iterations: N_2) at the end of the stress pulses (number of pulses: N_1). The corresponding chronogram describing the timing of this process is presented in Figure 5.26.

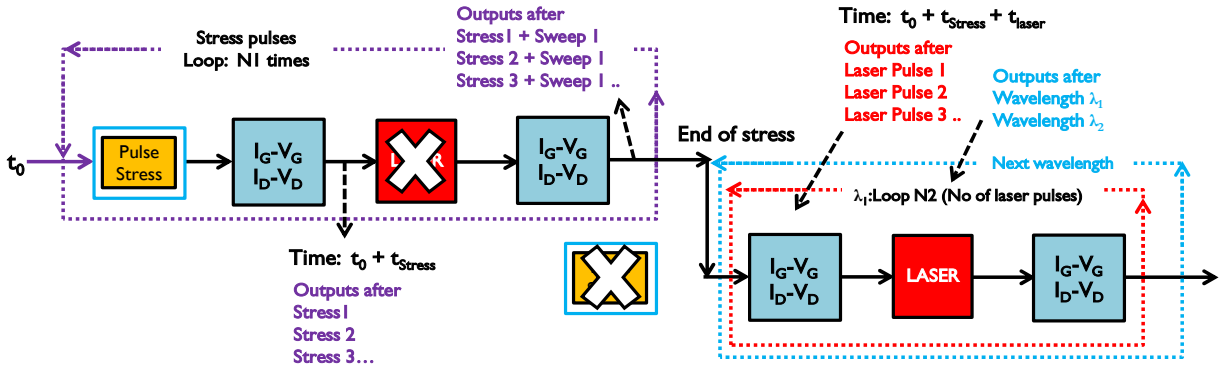

Figure 5.25: Schematic of the stress pulses followed by laser application approach

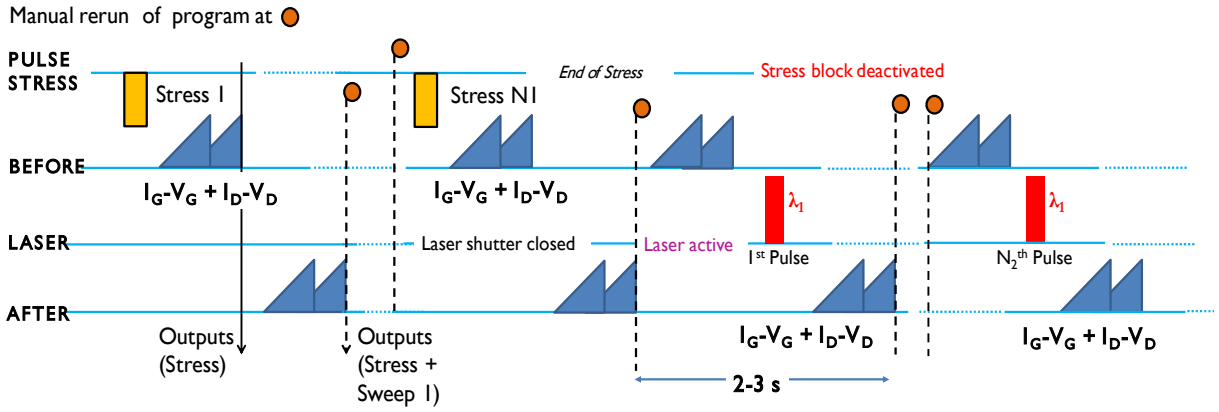

Figure 5.26: Timing diagram that explains the process flow described by the schematic in Figure 5.25

The approach is similar to Figure 5.22, except that the time based recovery section loop is replaced with incident laser pulses (number of laser pulse iterations: N_2) at the end of the stress pulses (number of pulses: N_1). The following cases explore laser effects of different λ on trapping-detrapping transients, interactions with stresses and natural, constantly occurring recovery with time.

Device 1, Test 1: 4 Pulse Stresses, then 2 Laser Pulses at λ= 1610 nm

Figure 5.27 (left) presents the characteristics obtained for two (N_2=2 in Figure 5.25) consecutive laser pulses at λ= 1610 nm after the device of Figure 5.16 is subjected to four stress pulses (N_1=4). Figure 5.27 (right) displays the corresponding ΔI_D curves. ΔI_D after identical tests at λ= 1700 nm (also dominant for this device) is presented as well. Here, ΔI_D represents the absolute difference between the I_D after a laser pulse (1, 2 etc.), and the measurement at the end of Stress 4. The (Stress 4+Sweep 1) state represents the maximal trapped state of the device.

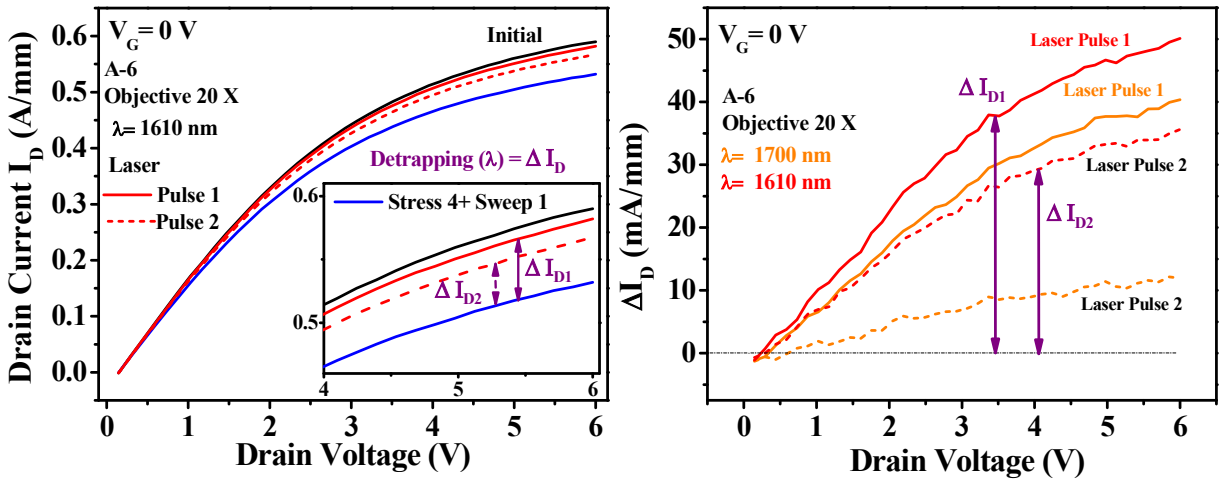

Figure 5.27: (left) I_D-V_D characteristics for laser application at λ= 1610 nm after four stress pulses (right) ΔI_D characteristics for the tests carried out at λ= 1610 nm and λ= 1700 nm.

From Figure 5.27 (left), we can see that the first laser pulse almost completely recovers the substantial stress-induced fall in I_D. Hence, a very strong detrapping transient is observed with high values for ΔI_D. In absence of laser pulses, this amount of detrapping could have taken several hours as observed in Figure 5.24. A normal "Before" sweep (I_G-V_G + I_D-V_D block preceding the Laser block) occurs before the second laser pulse of 1610 nm is applied. Retrapping (of traps detrapped by the first laser pulse) and detrapping (time based detrapping of trappings induced by the four stress pulses) occur simultaneously. The response after the second laser pulse is close but slightly lower than the I_D level after the first.

After an identical test, the behaviour is found to be similar for λ= 1700 nm (0.73 eV) (see Figure 5.27 (right), but the absolute ΔI_D is lower. Here, the ΔI_D for the second laser pulse is however notably lower, indicating that for traps with energies lower than 0.73 eV, retrapping after the first pulse is substantially more dominant than the detrapping due to the second. Since the ΔI_D for the two pulses at 1610 nm (0.77 eV) were much closer, it would follow that there are trap components present between 0.73 eV and 0.77 eV that have much slower retrapping constants. According to the discussion based on Figure 5.15, this would explain the close ΔI_D values for 1610 nm.

To study comparative effects of stress pulses on I_D and I_G, Figure 5.28 presents the ΔI_D and ΔI_G characteristics for the four stress pulses (N_1=4 in Figure 5.25) during the start of Test 1 (Figure 5.27) until the end of the stress section. In this case, ΔI_D or ΔI_G is defined as the difference between the steady state and stressed condition as illustrated in Figure 5.28 for an e.g. Stress 1.

While each stress pulse worsens the I_D fall, and ΔI_D is higher, the effect on I_G appears to be constant. Although the resolution specifics for the sourcemeter should be good until 100 nA, it is in fact found to be quite limited, which affects I_G readings. A small positive ΔI_G for low V_G might represent an increase in donor trap occupation resulting in slightly higher |BS|. However, ΔI_G is dominantly negative for medium to high V_G, which indicates a trapping of acceptors in BS devices.

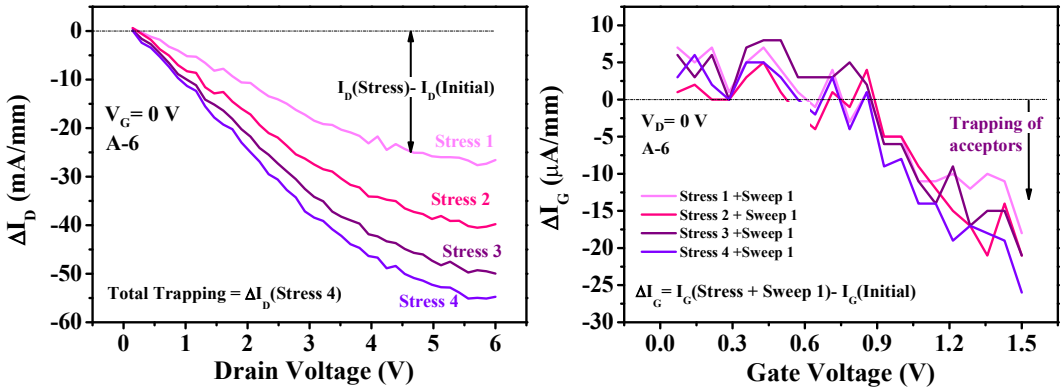

Figure 5.28: Effect of pulse stresses on drain and gate currents during the first section of Test 1

Hence, both characteristics reflect an increase of trapping phenomena, acceptor traps presumably, on application of stress pulses.

When the laser pulses are applied, the corresponding gate current characteristics in direct correlation with Figure 5.27 are displayed in Figure 5.29.

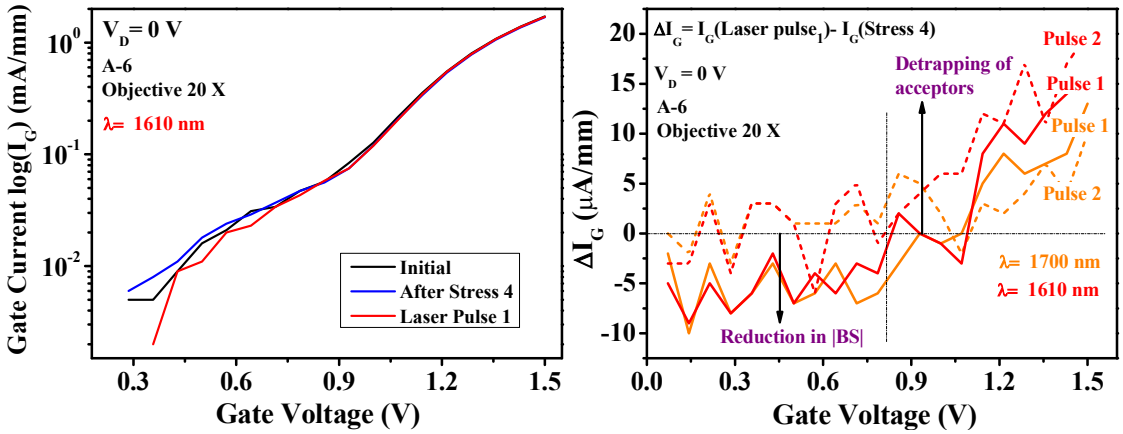

Figure 5.29: (left) I_G-V_G characteristics for laser application at λ= 1610 nm after four stress pulses (right) ΔI_G characteristics for the tests carried out at λ= 1610 nm and λ= 1700 nm.

The difference in I_G between the first laser pulse and Stress 4 is better represented in Figure 5.29 (right). The behaviour is opposite to the application of stress in Figure 5.28. Here, ΔI_G is initially negative and then moves onto positive values. It represents a small reduction in belly shape for low V_G, presumably due to detrapping of some donor traps. At high V_G, the fall in I_G due to detrapped acceptors is similar to the laser induced recovery of I_D.

Laser on Device 1, Test 2: 4 Pulse Stresses, then 2 Laser Pulses at λ= 2000 nm

Test 2 has characterizations similar to Test 1 on the same device but the laser wavelength is changed to λ= 2000 nm. Figure 5.30 presents associated effects on I_G for 2 consecutive laser pulses.

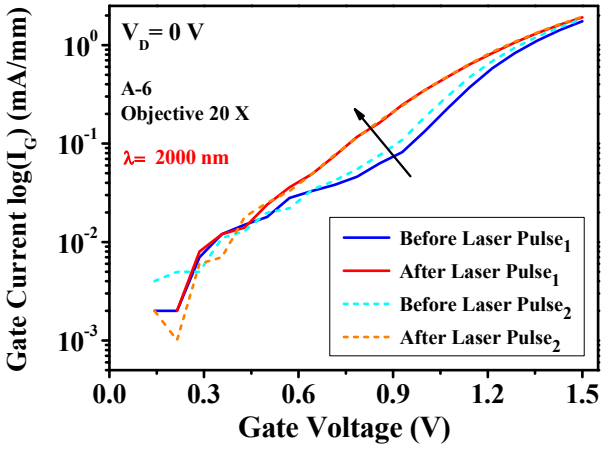

Figure 5.30: I_G-V_G characteristics for two WL pulses at λ= 2000 nm

The "Before" and "After" characterizations are obtained from the I_G-V_G + I_D-V_D blocks preceding and following the laser block respectively in Figure 5.25. It is clearly observable that the laser pulses induced an increase in the belly shape between V_G= 0.6 to 1.2 V. This is unexpected since it points towards an increased donor trap occupation. Since it has not been observed at λ= 1610 nm in Figure 5.29, it is probable that laser beam at λ= 2000 nm is somehow feeding energy for surface donors to tend towards higher occupations, thus supporting a higher |BS|.

Laser on Device 1, Test 3: 3 Stress Pulses, 1 Laser pulse at 2000 nm, 12 hr recovery

To verify if the results are consistent or reversible, the same device is subjected to Test 3 at λ= 2000 nm. The device is subjected to 3 stress pulses, followed by a single laser pulse, and finally left to recover for 12 hours. Figure 5.31 presents the associated I_G-V_G and I_D-V_D characteristics. The ΔI_G values are calculated and displayed in inset of Figure 5.31 (left).

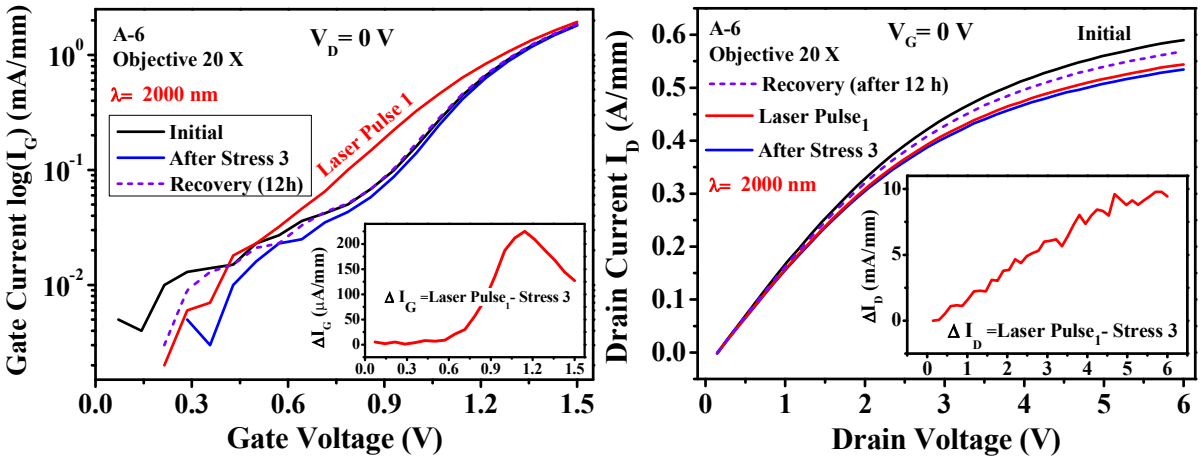

Figure 5.31: I_G-V_G and I_D-V_D characteristics for Test 3: laser application at λ= 2000 nm, and recovery for 12 hours, after 3 stress pulses are used to stress the device.

Here too, the application of the first laser pulse itself triggers an increase in the belly shape. Even at high V_G, the gate current is higher which could partially be due to acceptor detrapping. For lower V_G however, the donor traps seem to getting stronger due to the laser. Since a source of energy such as a laser should ideally induce detrapping and not trapping, an explanation could be that repeated laser bombardment on the device might have triggered some amount of physical damage.

Since the microscope objective is 20 X, the damage would be small but could have built up over several laser pulses. As such, some very shallow donor sites might have been created near the already degraded surface of the belly shape device, leading to stronger |BS|. The application of repeated stress pulses could also be a further contributor to extended surface worsening. This could also explain why initial tests on the device do not show this kind of I_G nature.

The effects of stress on the devices are still consistent with previous results. The effect of the laser pulse on the I_D behaviour still presents effects of acceptor detrapping with a ΔI_D close to 10 mA. Hence, at this point, any device degradation is only reflected in the leakage characteristic. After 12 hours of recovery time, the increase in belly shape as well as effects of the stress pulses are observed to disappear and I_G is quite close to its initial state. Since detrapping at λ= 2000 nm only partially improves the stress-induced fall in I_D, the recovery time further improves the current levels.

Laser on Device 1, Test 4: 4 Stress Pulses, 1 Laser pulse at 2000 nm, 24 hr recovery

If the laser induced rise in BS originated from physical degradation, further tests should show similar or aggravated trends in I_G. To validate this, Test 4 is performed with similar conditions: four stress pulses, a single laser pulse at 2000 nm and then recovery for 24 hours. The corresponding I_G-V_G and I_D-V_D plots are presented in Figure 5.32.

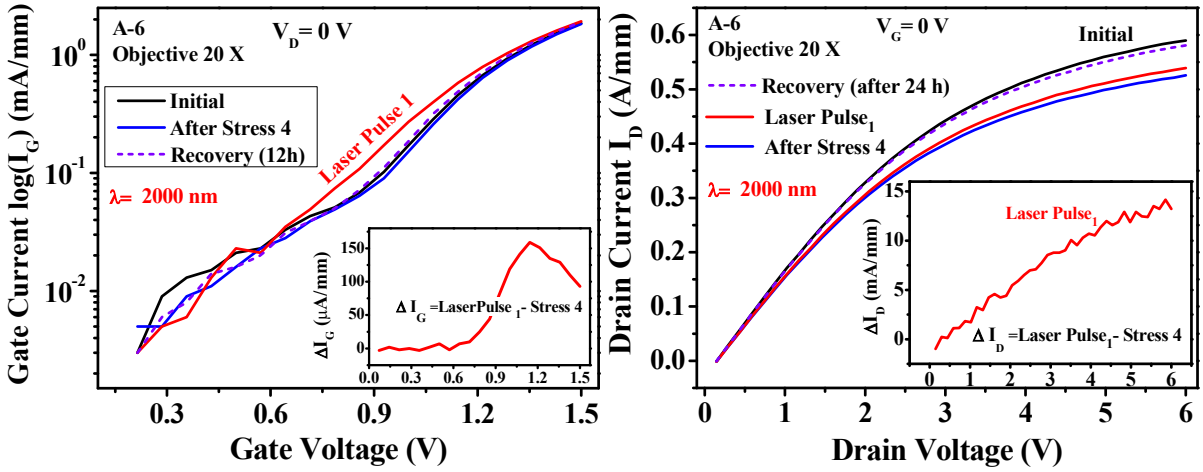

Figure 5.32: I_G-V_G and I_D-V_D characteristics for Test 4: laser application at λ= 2000 nm, and recovery for 24 hours, after 4 stress pulses are used to stress the device.

Similar behaviour to Test 3 is observed. The I_D behaviour is similar. The laser pulse again triggers a local rise in |BS|. The laser energy appears to activate the donor sites increasingly formed due to laser and pulse stresses. However, it recovers completely after 24 hours. The 24 hr recovery in I_D is also observed to be better than for the 12 hours in Test 3 (Figure 5.31 and Figure 5.32 (right)).

Laser on Device 1, Test 5: 4 Stress Pulses, 4 laser pulses at 2000 nm, No recovery

In Test 5, the device is similarly subjected to four stress pulses. Now however, multiple laser pulses at λ= 2000 nm are applied to observe the effect on I_G without any recovery intervals. Figure 5.33 presents the change in I_G for four consecutive laser pulses. Corresponding effects on I_D are displayed in Figure 5.33 (right). On the first laser pulse, I_G is only marginally higher. The second and

third pulses significantly increase the I_G leakage, observable especially at low V_G. The I_D behavior during these pulses still resembles the general detrapping response for a laser pulse of 2000 nm.

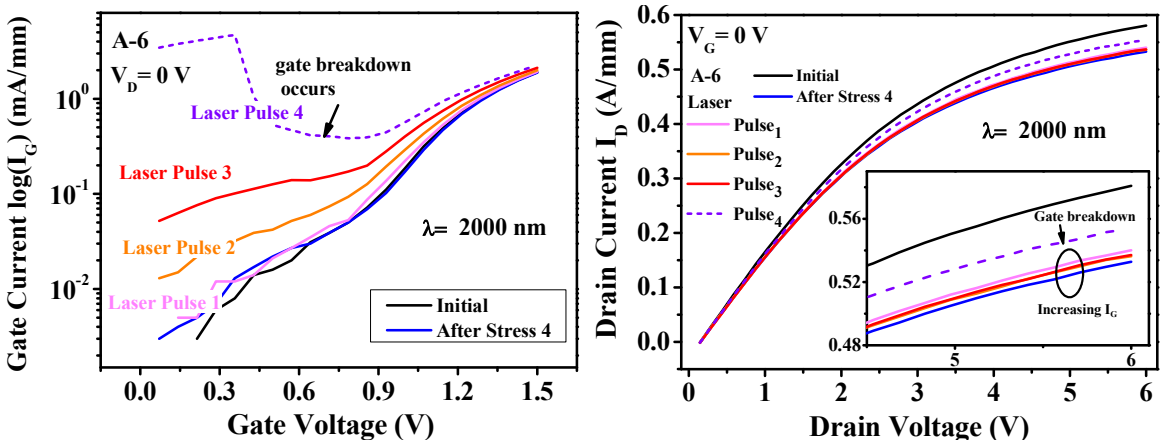

Figure 5.33: I_G-V_G and I_D-V_D characteristics for Test 5: repeated laser application at λ= 2000 nm following 4 stress pulses

Finally, when a fourth laser pulse is applied, the gate current increases uncontrollably leading to gate breakdown. At this point, the I_D currents abruptly rise due to the gate leakage and the device loses gate control over current levels, as shown in Figure 5.34.

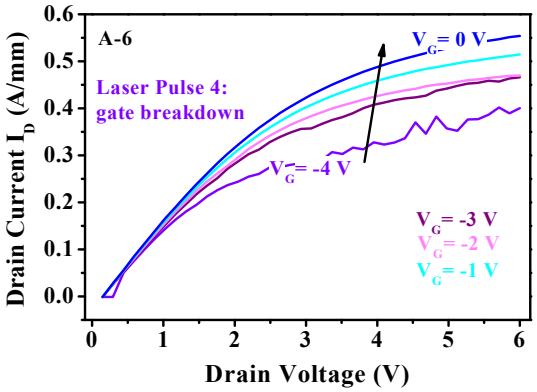

Figure 5.34: Loss of gate control over the device characteristic after 4 WL pulses at λ= 2000 nm

Stress Induced BS Rise: Device 2, Test 1: 2 Stress Pulses followed by 4 Stress Pulses

On a second device, the impact of stress pulses was found to present interesting results that add to the discussion about laser effects on the previous device. Stress pulses were applied to this device in two sets with 2 and 4 stress pulses each.

Their ΔI_G characteristics are presented in Figure 5.35. For Set 1, the stress pulses create an increase in |BS| with a ΔI_G nature very similar to the ΔI_G in Figure 5.31 and Figure 5.32 for the laser pulse induced rise in |BS|. No amount of acceptors detrapping can produce such a rise in BS. Even more, stress pulses with a reverse bias would not support a detrapping in acceptors.

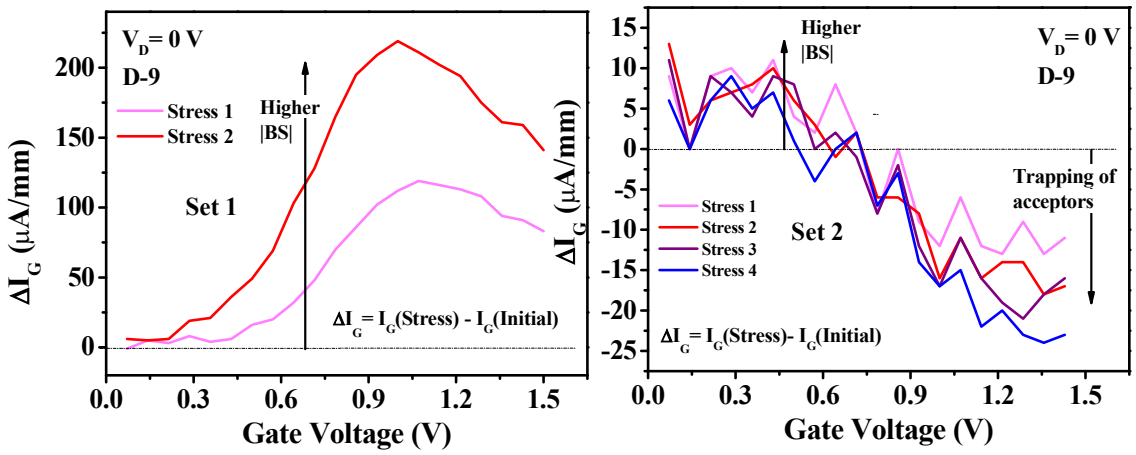

Figure 5.35: ΔI_G characteristics for two sets of stress pulses on device D9

As such, an increase in donor traps due to stress pulses is a reasonable explanation. This observation implies that the laser triggered rise in BS, which closely resembles the stress-induced rise, could also be due to a trapping of donors or activation of donors, rather than a detrapping related response.

During Set 2 stresses however, this effect disappears and ΔI_G agrees with the general stress response similar to Figure 5.28 (right). This further attests to the low energies of the shallow surface traps, activations of which are highly transient and unpredictable at varying times or conditions.

E. LASER SCANNED OVER ACTIVE AREA AFTER ELECTRICAL STRESSES

As illustrated in Figure 5.11, the central laser spot is usually incident on a small part of the device area. Though the position is changed between different tests across different gate fingers, only a single laser spot is responsible for the observed detrapping response. It is reasonable to study the detrapping effects if multiple laser spots were employed, over the entire active device area including the gate fingers. This is a different technique of laser application, as illustrated in Figure 5.36.

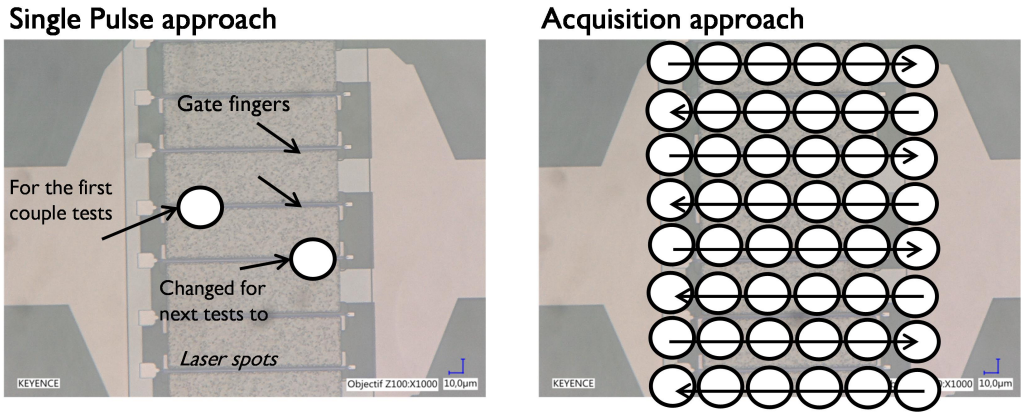

Figure 5.36: Comparison of single laser spot approach compared to the acquisition approach

Instead of a single pulse during the Laser block in Figure 5.25, the "Before" characterization is followed by an acquisition labview program which moves the board gradually in X and Y directions such that single laser pulses are applied at distributed points, eventually scanning the entire device. This is a more comprehensive approach to ensure each part of the device receives laser energies, and can contribute to the corresponding detrapping transient. The application of the stress block or sweep stresses remains identical.

However, since the process takes 2-3 minutes to complete, effects of natural detrapping could accompany the laser acquisition response when following stress pulses or sweep sets. Hence, a stronger response due to this new technique might in addition to laser effects, contain a contribution from time-induced detrapping.

Sweep as a Stress Condition

As previously discussed for no-laser sweeps or general "before" and "after" characterisations (see Figure 5.17 and Figure 5.19), repeated characterizations of the device have been found to create trapping-like effects on the device. As such, a sufficiently high number of sweeps could be a valid stressing condition for the device, as illustrated in Figure 5.37. The effect of sweep stress on ΔI_G, in comparison to ΔI_D, is presented in Figure 5.38.

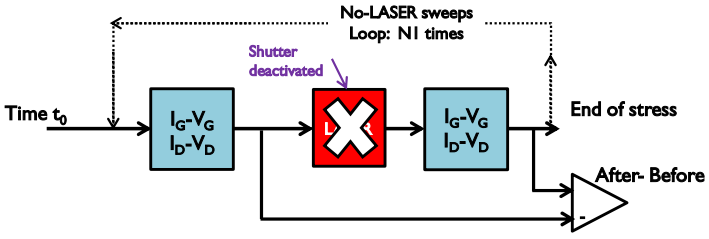

Figure 5.37: Schematic of the no-laser/sweep stress approach

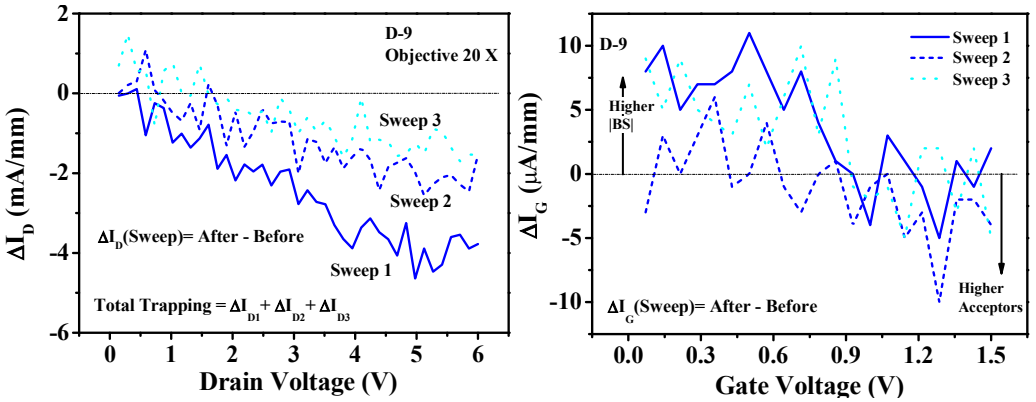

Figure 5.38: Sweeps as a stress condition: effects on ΔI_D and ΔI_G for three consecutive sweeps

Here, the differences are directly taken as "After"-"Before" so the trapping effects are accumulative over the applied sweeps. The behaviour in Figure 5.38 clearly reflects that the effect of

sweeps is similar to the effect of pulse stresses, though the absolute magnitude of induced trapping is lower. This is to be expected since the pulse stress induces trap filling at a much more potent reverse biased condition with a high electric field. The effect of sweeps, similar to pulses, also appears to decrease at higher instances as the response stabilises.

Time-induced Recovery of Sweep and Pulse Stresses

Similar to the analysis of stress pulses (for example Figure 5.25), it is necessary to understand how the device recovers after sweep stress induces changes in gate or drain currents. Figure 5.40 compares the ΔI_D for (left) two sets of 7 sweeps and (right) three sets of 4 stress pulses, according to the illustrated schematic in Figure 5.39. The changes in gate current have been found to be too trivial for discussion. The ΔI_D is calculated between the maximal stressed state and after 5 mins of recovery time. Then a break of 3-4 hours is taken, before commencing a second set.

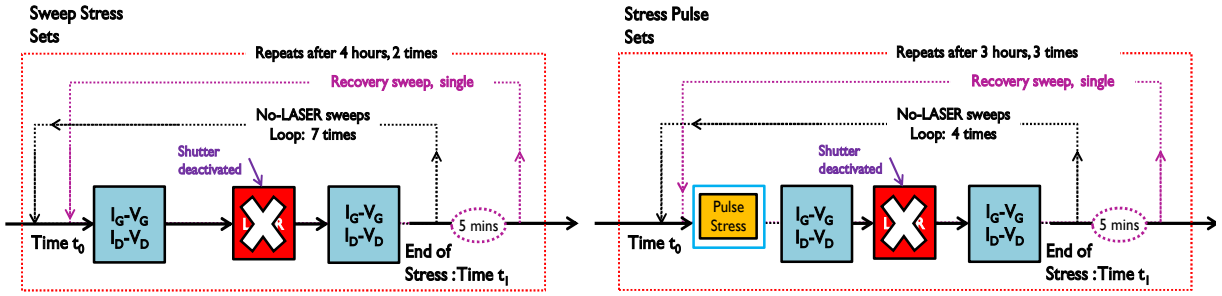

Figure 5.39: Schematic for the time-based recovery tests of (left) sweep and (right) pulse stresses

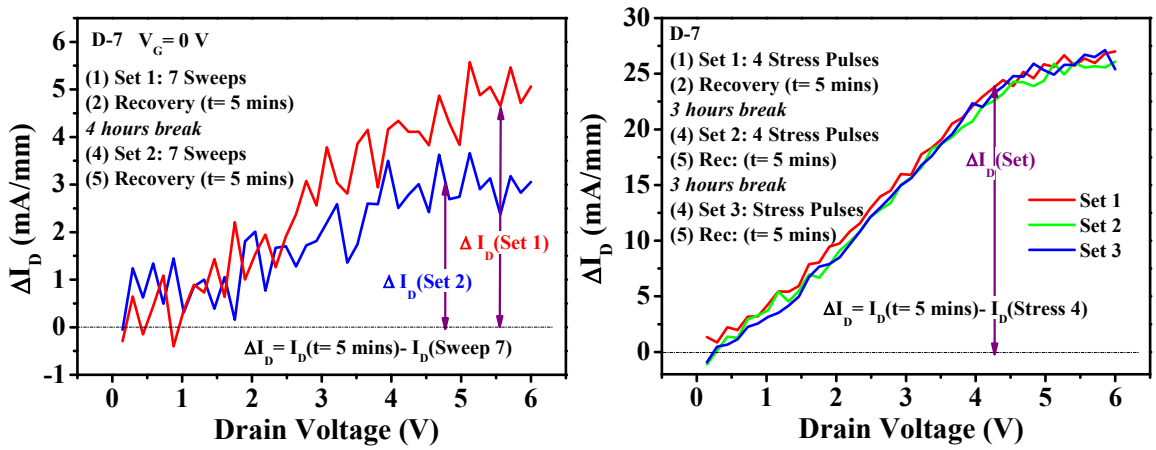

Figure 5.40: ΔI_D for 5 mins of recovery after (left) 2 sweep stress sets and (right) 3 pulse stress sets

The sweep sets show medium recovery for both sets for the 5 minute window. Since sweeps only activate a moderate amount of traps, it is reasonable to observe low ΔI_D levels within a five minute interval. Pulse stresses however activate significant traps with very short time constants. Hence, the recovery time of 5 mins is sufficient to detrap most of the stress-induced trap density.

The pulse stress induced ΔI_D magnitudes are also significantly higher than for sweep stresses. This behaviour is found similar for several devices, which validates the heightened effect of pulse stresses in comparison to sweep stresses.

Laser Induced Recovery of Sweep and Pulse Stresses

To extend the discussion into the nature of traps that are activated by the two stressing techniques, Figure 5.42 plots the responses of the same device subjected separately to trapping pulses and sweep tests followed by a single laser pulse at 1610 nm. The change in the device state, 5 mins and 10 mins after the laser, for the pulse and sweep cases respectively, is also demonstrated. The chronogram describing the experimental flow is presented in Figure 5.41 for the sweep and pulse stress cases.

Following the stress pulses, the laser pulse detraps a substantial amount of traps that were activated due to the trapping pulses. Within 5 mins, the I_D falls however to a lower value, with ΔI_D fall of 10 mA. Thus, we can assert that a portion of the traps activated by stress pulses have trapping constants smaller than 5 mins.

However, a significant ΔI_D still exists beyond the 5 min period. This accounts for slow recharging traps. The behavior after sweep stresses is similar except that the fall in I_D is similar even though the recovery period is longer. This would mean that sweep tests activate a lower density of traps with fast charging constants, for energy positons lower than 0.77 eV (≈ 1610 nm) from the E_C.

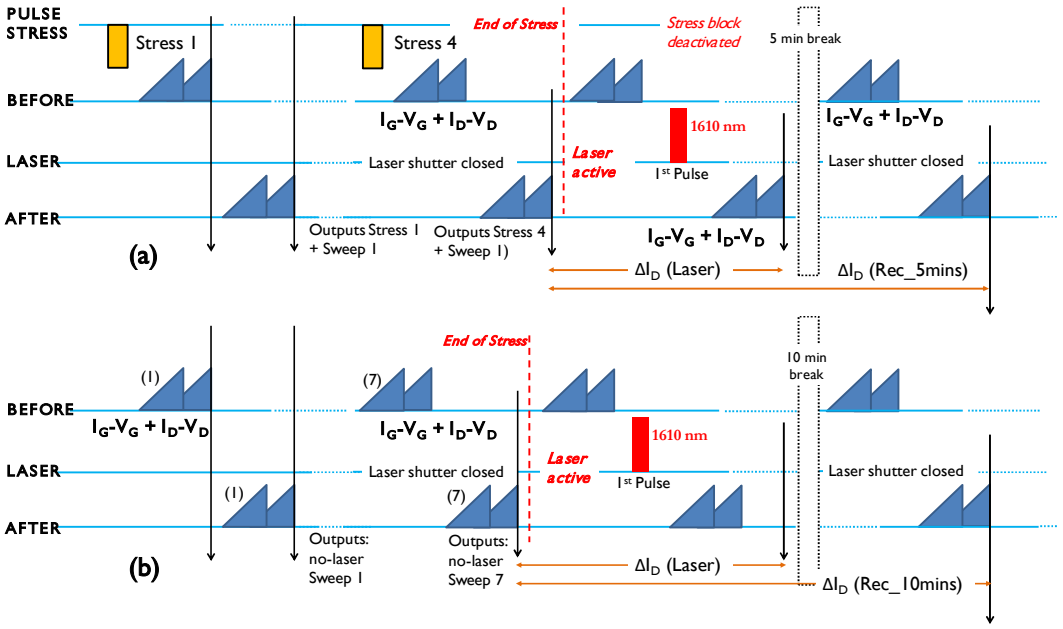

Figure 5.41: Timing diagrams to describe the stress and recovery process followed for the results in Figure 5.42 for (a) pulse stresses and (b) sweep stresses

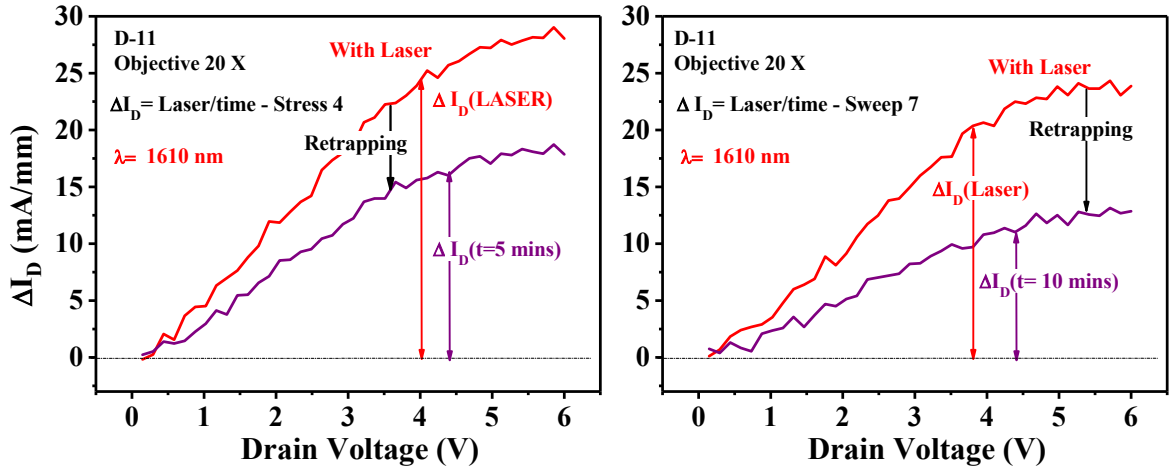

Figure 5.42: ΔI_D characteristics for a laser pulse at 1610 nm and recovery following (left) four stress pulses and (right) seven sweep stresses

We compare the amount of retrapping occuring after the laser-induced detrapping, by plotting the difference between the response after the 5/10 mins of recovery time and the response immediately after the laser in Figure 5.43. The response to a 2000 nm (0.62 eV) laser pulse and 5 minutes of recovery time after stress pulses is also shown for comparison.

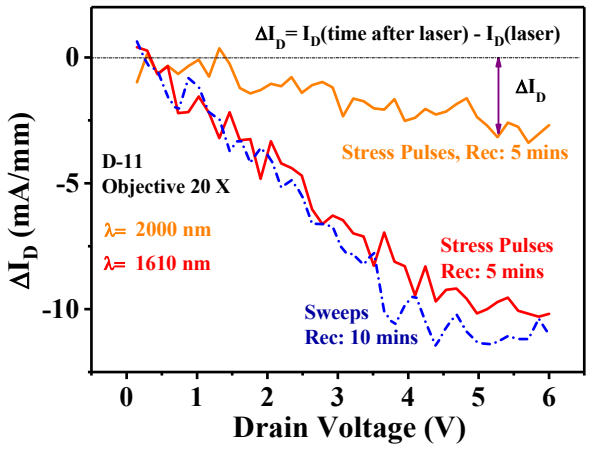

Figure 5.43: Comparison of retrapping during recovery intervals after laser pulses at 1610 nm and 2000 nm for pulse stresses and 1610 nm for sweep stresses.

Clearly, stress-activated trap components exist that have energies below 0.61 eV (2000 nm) and display recharging time constants smaller than 5 minutes. These traps however, are not the dominant stress induced traps. The dominant traps with energies between 0.61 eV and 0.77 eV are present in higher densities and are mostly fast recharging traps, since the difference between the 2000 nm and 1610 response, both for 5 minutes of available natural retrapping time is quite substantial. Sweep activated traps however require a longer 10 minute interval to reach the same amount of

retrapping that occurred after 5 mins in the stress pulse case. As seen in Figure 5.42, the initial ΔI_D for (laser)-(7 sweeps) and (laser)-(4 stresses) were quite similar. Hence it is fair to assert that sweep activated traps generally have longer recharging constants than those activated due to the reverse biased stress pulses. Since the consecutive laser pulse responses at 1610 nm are usually close, in contrast to 1700 nm responses (as discussed previously in Figure 5.27), the fast charging traps can be further localised between 0.73 eV (1700 nm) and 0.61 eV (2000 nm).

Laser Acquisition Tests after Stress Pulses

Device 1, Test 1: 5 Stress Pulses, Laser at 2000 nm, 33 mins recovery, Laser at 1610 nm

In Test 1, the comparative effects of the chosen laser wavelength, stress and recovery times are considered. The process schematic is displayed in Figure 5.44.

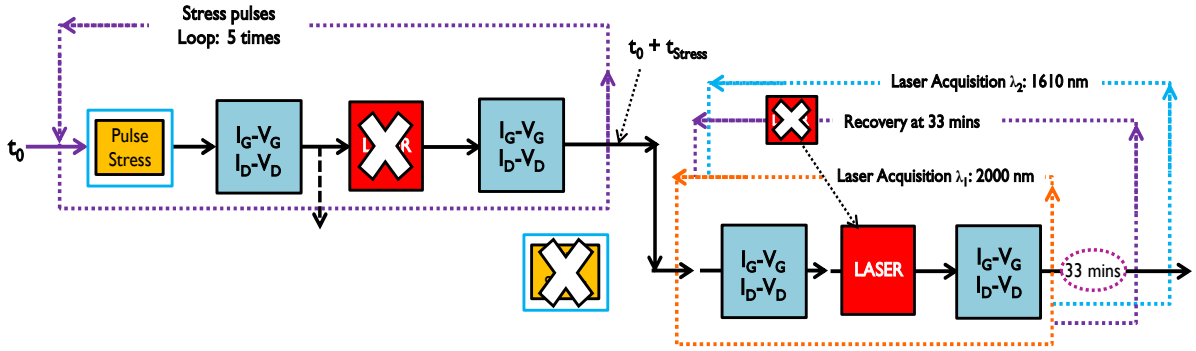

Figure 5.44: Schematic describing the experimental process for Test 1: 5 stress pulses followed by an immediate laser acquisition at 2000 nm, then a 33 minute recovery, and acquisition at 1610 nm.

Five stress pulses are applied to the device. The stress-induced changes in I_D and I_G were found consistent with general stress behaviour. No increase in BS was observed. Then a laser acquisition was performed at λ= 2000 nm with single laser spots applied at different parts of the active device region. This was followed by a recovery interval of 33 minutes. Then, a second laser acquisition at λ= 1610 nm was employed. The corresponding ΔI_D and ΔI_G are shown in Figure 5.45.

The first laser acquisition (at 2000 nm) prompts a medium recovery in I_D levels. The BS magnitude, here too is significantly enhanced after the laser is applied. Within 3 mins, we see that ΔI_D falls, indicating rapid retrapping. Between the 3 mins and 33 mins time window, retrapping of traps after laser-induced detrapping, and detrapping after the stress-induced trappings are occurring simultaneously hence we see a small rise in ΔI_D. Then, a second laser beam at 1610 nm is applied in an attempt to detrap the remaining traps, which have time constants higher than 33 minutes. An additional 10 mA of detrapping is obtained as indicated in Figure 5.45 (left). The belly shape however worsens considerably on application of the second laser instance.

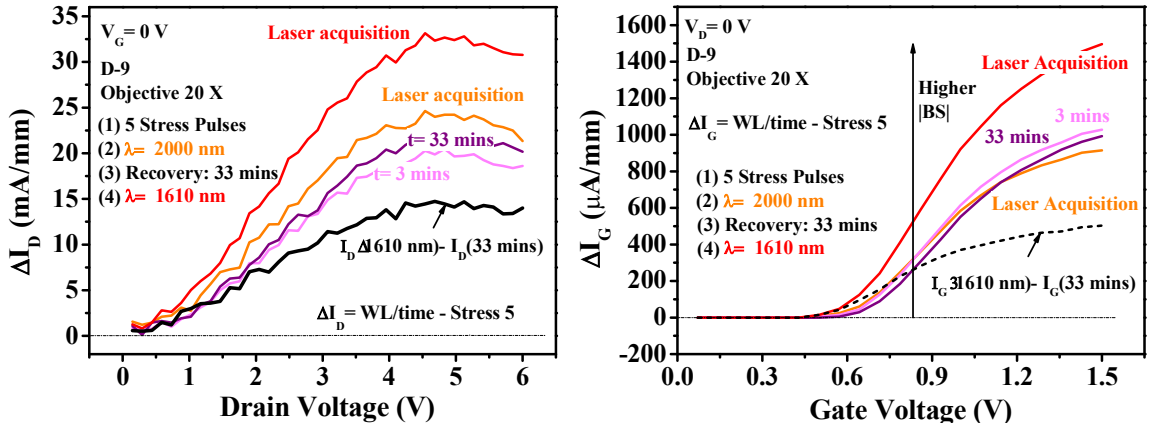

Figure 5.45: ΔI_D and ΔI_G behavior for Test 1 scenario with five stress pulses, laser acquisition at λ= 2000 nm, a 33 min recovery and finally acquisition at λ= 1610 nm

The acquisition approach has not been found to substantially promote higher ΔI_D levels compared to the single laser spot approach (Figure 5.45 compared to Figure 5.27 for λ=1610 nm following stress pulses). However, ΔI_D is greatly dependent on trap instances in different devices, and the amount of additional trappings generated by stress pulses, so it's difficult to make a direct comparison. Due to the acquisition approach however, the degradation in gate characteristics (ΔI_G) seems to have been intensified (Figure 5.45 (right) compared to Figure 5.31/Figure 5.32 for λ=2000 nm following stress pulses). This is probably linked to the bombardment from the additional laser pulses applied during the acquisition.

Device 1, Test 2: 4 Stress Pulses, Laser acquisition at 1610 nm, Recovery for 3 mins

As illustrated in Figure 5.47 comparing the I_G behaviour for Test 1 and Test 2, the gate characteristic was already degraded during Test 1. In Test 2 on the same device, four stress pulses are applied. Then, an acquisition at 1610 nm is performed. After a recovery time of 3 mins, the device is re-characterized. The schematic is in Figure 5.46.

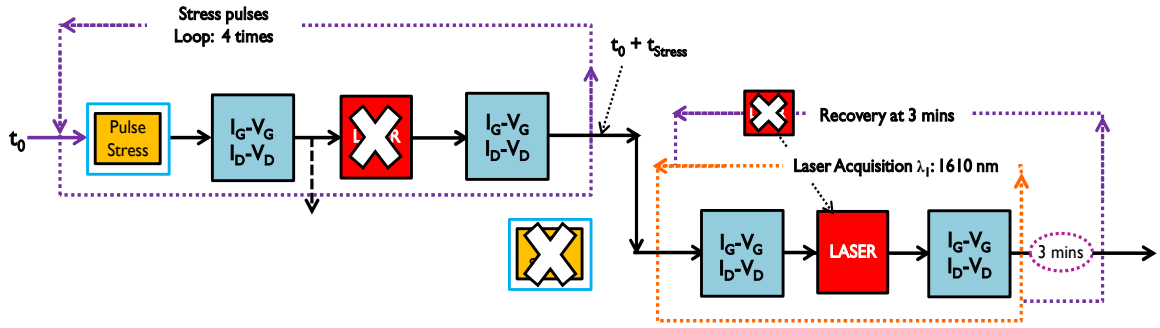

Figure 5.46: Schematic for Test 2: 4 stress pulses, laser at 1610 nm, followed by a recovery of 3 mins

In the beginning of Test 2 during a significant time after the second acquisition induced I_G rise in Test 1, the gate characteristics were comparatively normal.

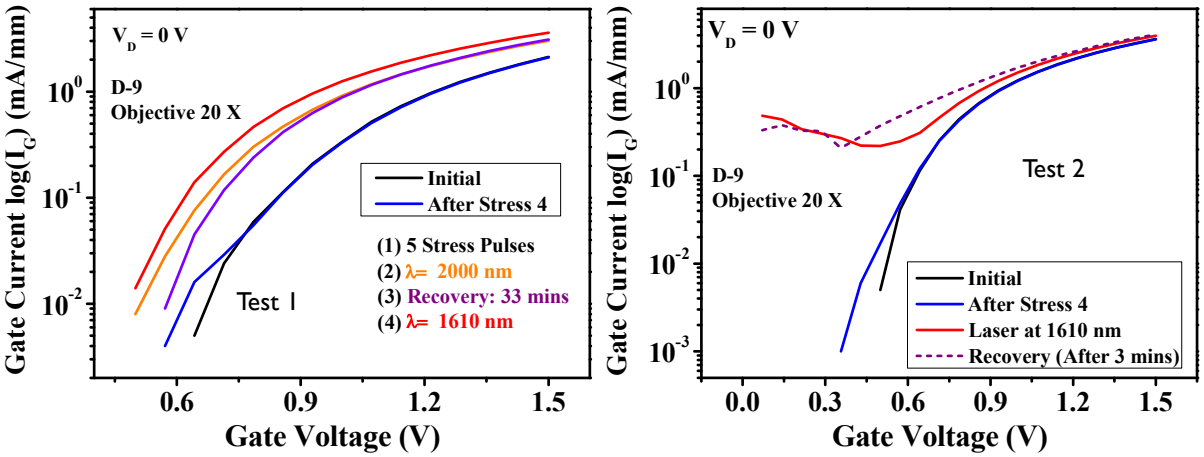

Figure 5.47: I_G- V_G characteristics on laser acquisition during (left) Test 1 and (right) Test 2 following stress pulses

This is probably because even though the new trap sites existed due to degradation, they were unoccupied. Once the laser is applied, immediately, the gate leakage catastrophically increases. Recovery times were found to no longer be helpful. On the next biasing sweep, the device loses gate control, similar to Figure 5.34.

Laser Acquisition Tests after Sweep Stress

Device 2, Test 1: 7 Sweeps, 2 Laser acquisitions at 2000 nm, 1800nm, 1610 nm

On attempting the extraction of laser acquisition based detrapping transients on a different device, after stressing the device using sweeps instead of pulses, similar behaviour was observed leading to gate breakdown after several laser applications.

Two acquisitions were performed for each wavelength. The process schematic for Test 1 on this device is displayed in Figure 5.48.

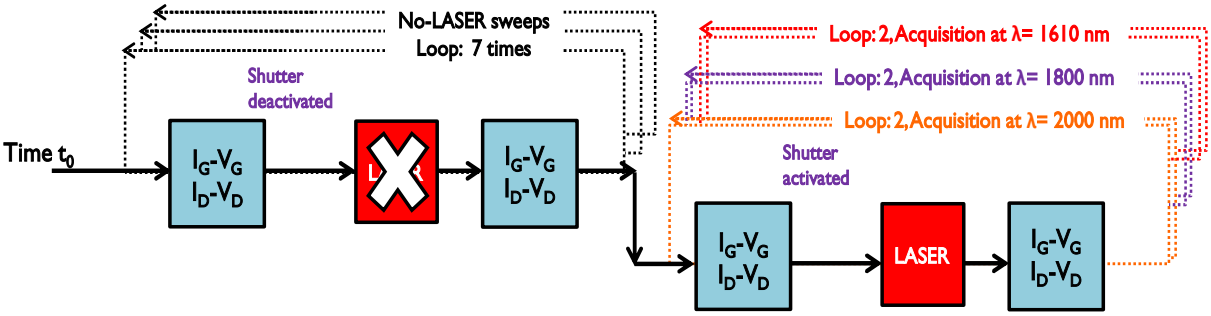

Figure 5.48: Schematic for test 1: 7 sweep stresses followed by 2 laser acquisitions each at 2000 nm, 1800 nm and 1610 nm sequentially.

Figure 5.49 illustrates the relevant ΔI_D and I_G behavior for the three wavelengths. The second laser acquisitions at each wavelength cause a slight recovery in the |BS|.

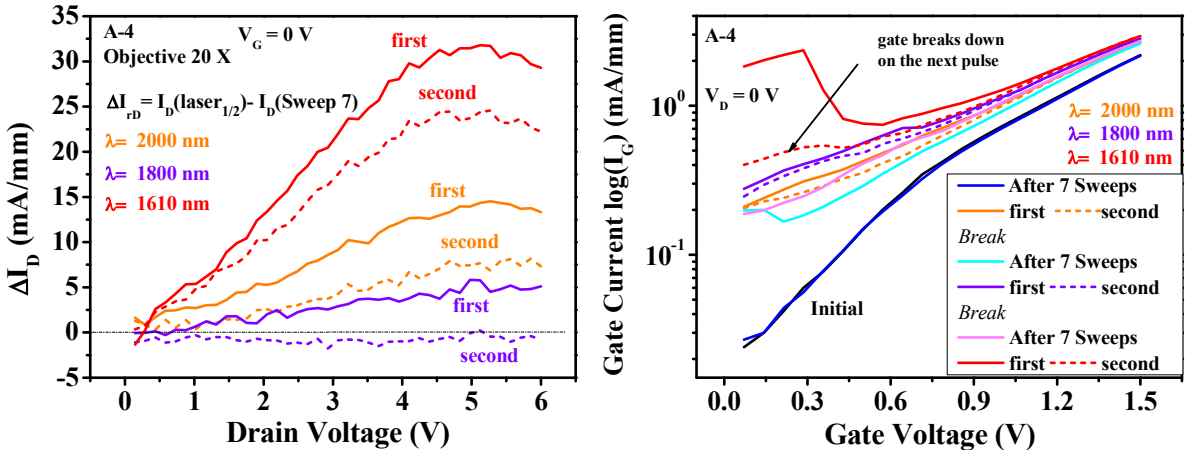

Figure 5.49: (left) ΔI_D characteristics for Test 1 acquisitions at 2000 nm, 1800 nm and 1610 nm and (right) I_G-V_G characteristics during stresses and the two acquisitions each of Test 1 (Figure 5.48)

Eventually however, gate breakdown occurs beyond the second laser acquisition at 1610 nm. Here too, however, until the point of gate breakdown, the degradation of the gate is unnoticeable from the ΔI_D measurements which continue to display acceptor trap induced detrapping transients As a side note, stress and acquisition effects substantially increase this device's detrapping magnitudes, compared to Figure 5.20 for laser pulses applied in steady state.

5.4 OBIC Imaging of Devices under Test

After the gate breakdown of the devices, the optical beam induced current (OBIC) technique was employed to scan and image the active device area. Normally, it would indicate the vulnerable or defective structural regions. For this work, it enables a visualization of the high defect densities expected around the gate fingers associated with the catastrophic increase in leakage currents. The technique employs the gate resistor to obtain the current response between the gate and source when the drain is grounded.

On applying a laser beam with energy higher than the semiconductor bandgap, e-h pairs or excess carriers are generated due to absorption of individual photons as carriers are excited into the conduction band. The electric field separates the generated carriers, and the photocurrent is measured and analyzed to detect defects or system anomalies. Considering the large GaN bandgap (E_G= 3.4 eV) and thus, the requirement for UV wavelengths to realise single photon OBIC, the two-photon OBIC method was found to be better suited for this work. The two photon absorption or T-OBIC uses photon energies lower than the band gap of the semiconductor, but greater than half of the band gap. This is a non-linear form of absorption, with a reduced probability for carrier generation. Using ultra short laser pulses (≈ 100 fs), photons can be concentrated in both space and

time to maximize impact in a small section at a time. T-OBIC reduces the absorption of the illuminating light by the substrate or overlayers while allowing an efficient generation of photo-excited carriers in the active layer. We use a laser with λ= 550 nm i.e. energy = 2.25 eV. Gate voltage was biased at -10 V to have high electric field present within the device and obtain the photocurrent. Mapping step sizes were between 4 to 6 μm.

The oscilloscope connected across the gate resistor plots equivalent voltages for the gate current component. Across the source resistor, we obtain the I_D+I_G response. Obtained for each scan position, these signals in contrast scale build an image of the scanned area. The technique detects variation in electric fields across the area scanned. Any difference in signal amplitudes between an ideal device and a stressed or aged device at specific regions or spots of the device is indicative of a deviation. Hence higher voltage transients are indicative of defects.

Device 1: Reference device

For reference, T-OBIC imaging of a device that was unstressed by the aging tests in Chapter 4 or the laser experiments in Chapter 5 was performed, as illustrated in Figure 5.50.

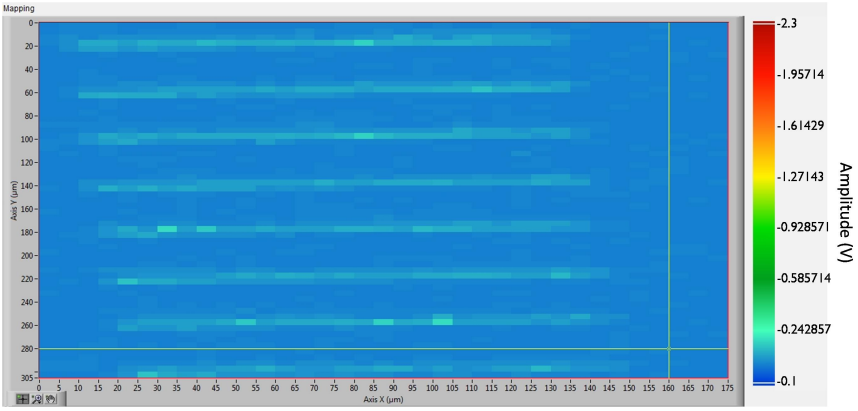

Figure 5.50: Example of an OBIC mapping for an unstressed device

The signals are higher near the gate fingers, and are uniform in magnitudes. This is to be expected since, under the applied reverse bias, the electric field is highest across the region surrounding the gate-drain edge. Very minor discontinuities are detected and they are distributed across the different gate fingers. There is a shift observed in the image towards the lower gate fingers, probably arising out of minor hysteresis within the motors controlling the scan of the board.

Device 2: Gate breakdown after laser acquisition

The test device suffered from gate breakdown following repeated iterations of stress and laser acquisition tests (Section 5.3.E), where the laser beam was scanned across the active device area. Figure 5.51 presents the device images after it was subjected to the T-OBIC imaging technique.

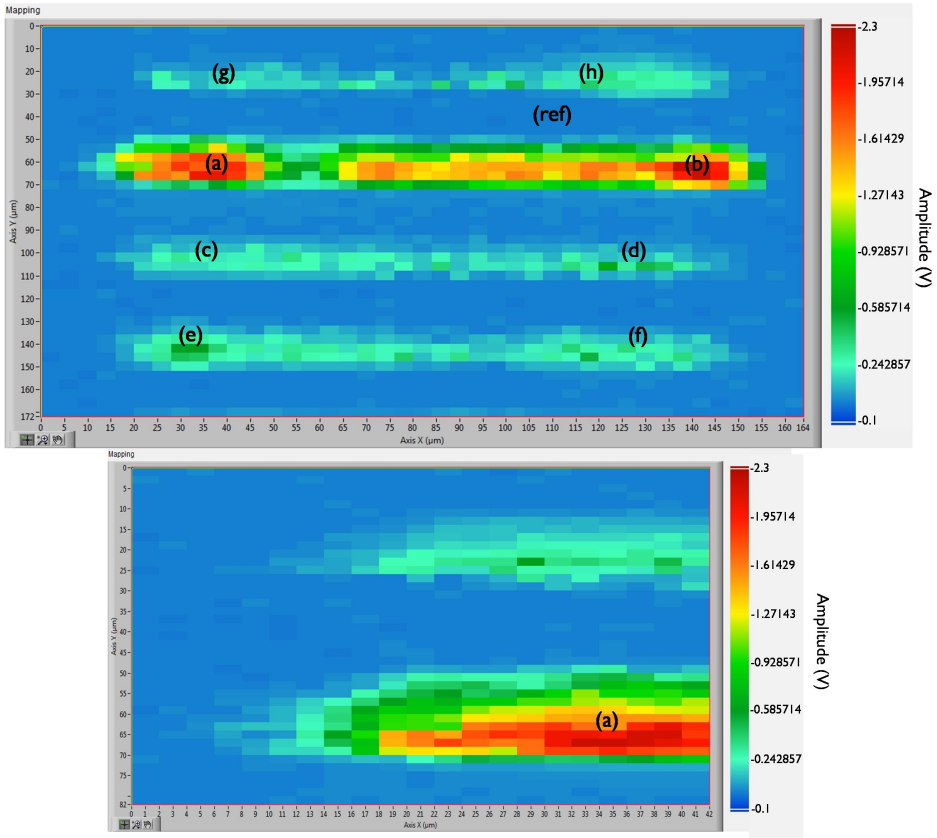

Figure 5.51: Example of an OBIC mapping for a device after gate breakdown with a closer left scans for the defective gate finger.

The amplitude of the obtained T-OBIC signals, in comparison to the reference Figure 5.50, indicates the level of physical degradation existing in the device. Figure 5.51 displays the image covering four out of the eight gate fingers of the device. By changing the X and Y step size of the scan, it is possible to obtain a closer zoom in to the left (shown in Figure 5.51) or right edges of the relevant gate finger where the signal contrast is highest. Now, it is clearer that the signals appear to be higher towards the lower end of the gate finger, which could be because of proximity towards the drain side with higher electric fields.

The voltage amplitudes are up to 10 times higher than obtained for the reference of Figure 5.50. It is easy to discern that the maximal deviation is concentrated on a single gate finger, which could presumably be the location of breakdown. This finger might have been bearing most of the heat generated from transistor operation, which usually is concentrated towards the central gate fingers in the middle of the active area. Thus, it would be the first gate finger to suffer damage. Once the breakdown occurs, the device leakage is uninterrupted and further defects are less probable.

The T-OBIC transients were extracted from different points of the image, as illustrated in Figure 5.51 and plotted together in Figure 5.52 (left).

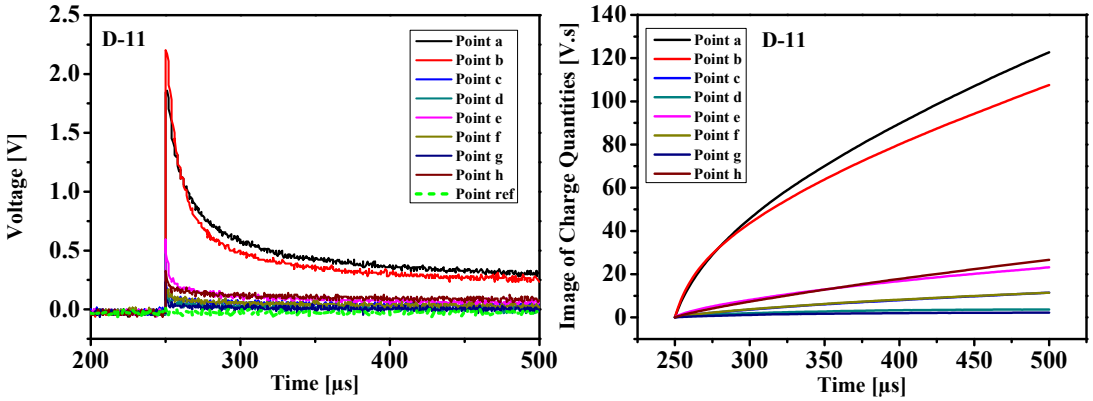

Figure 5.52: (left) OBIC signals for device 1 at different points of the scanned device area and (right) integral of the voltage signals to represent associated charge quantities

The (ref) point in Figure 5.51 is the zero contrast point where signal amplitudes are minimal. The voltage signals integrated over the time interval provide the comparative charge contributions associated with each signal since the resistance is constant (see Figure 5.52 (right)).

It is observable that the peak signal points (a) and (b) on the left and right edge of the gate finger corresponds to highest charge levels associated with T-OBIC induced photocurrent. This indicates that the primary defects are present at these edges. Stress or aging tests generally bias the device at high reverse gate voltages which would be focused at the gate finger biasing edges.

The breakdown could have originated there, though the entire gate finger would still substantial defects as can be seen from Figure 5.51. From Figure 5.52 (right), the next highest charges after (a) and (b) appear at points (e) and (h) which could be smaller defects on the surrounding gate fingers. Here too, defects have appeared at the edges of the gate finger.

Device 3: Gate breakdown after single shot laser pulses

A second device that suffered from gate breakdown after several stress pulses and the associated laser application in Section 5.3.D was imaged using T-OBIC. The obtained image is displayed in Figure 5.53 with the same color scale as for Figure 5.50 and Figure 5.51.

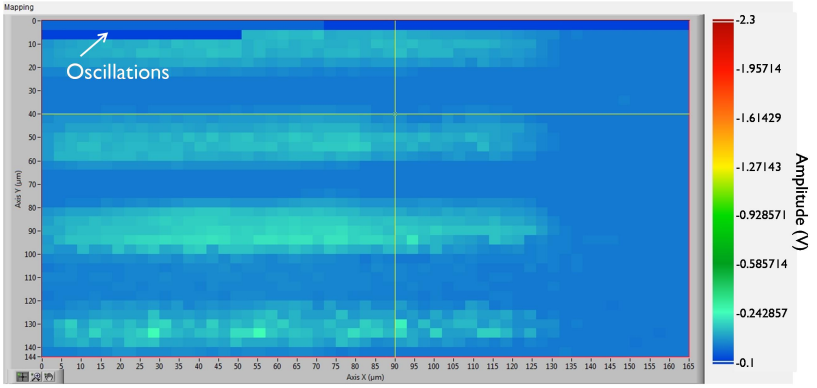

Figure 5.53: Example of an OBIC mapping for a device after gate breakdown

Though several lighter spots can be observed, the magnitudes of the voltage transients are substantially lower than obtained for Device 2. This could be indicative of a lower level of damage since Device 1 was subjected to a higher number of laser pulses during each acquisition process, in comparison to the single laser pulse applied during a test on Device 3.

Towards the end of the scan (top left of Figure 5.53), the signal readings were disrupted due to the onset of laser induced oscillations. The transient on the oscilloscope observed in such conditions is displayed in Figure 5.54. The time per division scale is optimised for the expected signals, and hence fails to accurately capture the shape of the oscillations.

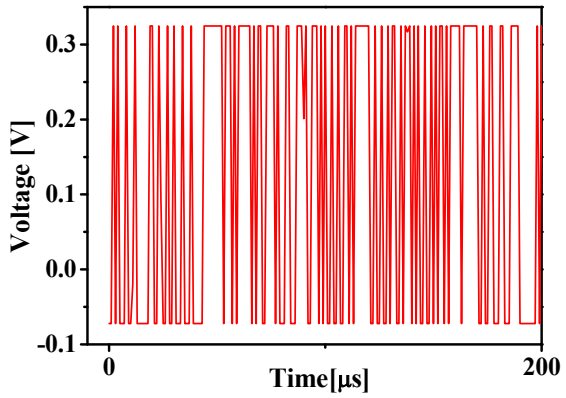

Figure 5.54: Signals on the oscilloscope when laser induced oscillations occur during a T-OBIC scan

This is a potential issue with the T-OBIC scan process and must be monitored to maintain the fidelity of the scan. To better understand the defect occurrences in this device, Figure 5.55 presents the image in a tighter magnitude range.

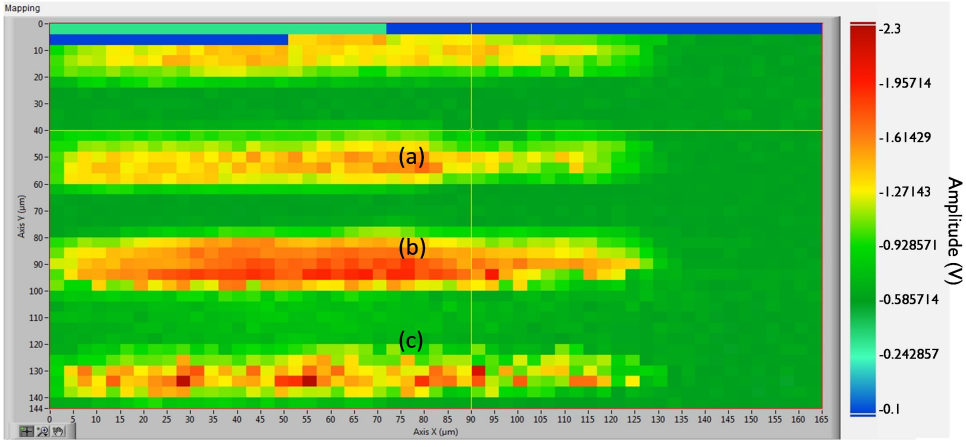

Figure 5.55: OBIC mapping of device 3 after reducing the contrast range from Figure 5.53

In Figure 5.55, the points of damage are observable and appear to be distributed across the different gate fingers. The signals are quite high in the surrounding region of each gate finger as well. It is difficult to conclude however on which of these fingers is at the center of the gate breakdown

since they have similar magnitudes. Being belly shape devices, they were expected to show significant degradations surrounding the gate edges where the donor trap sites form and spread. Here too, oscillations appear towards the end of the scan. However, they do not seem to result in immediate destruction of the gate contact, since subsequent scans have been viably obtained, even after the oscillations appeared.

Figure 5.56 compares the voltage transients for the scan points (a), (b) and (c) as marked in Figure 5.55. To study if the defects have a directional dependence relative to the gate surroundings, a closer look at the gate finger corresponding to point (a) is imaged as shown in Figure 5.57.

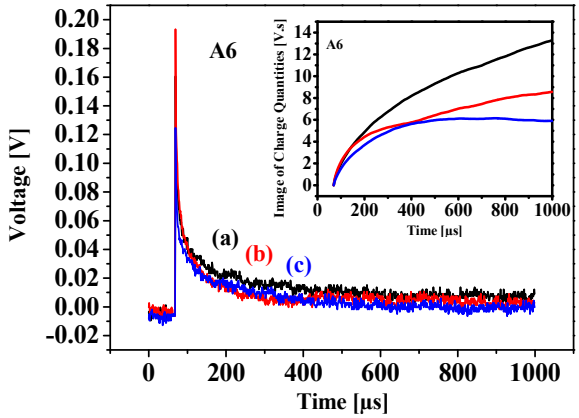

Figure 5.56: Comparison of OBIC transients at different scan points (inset) relative charge content

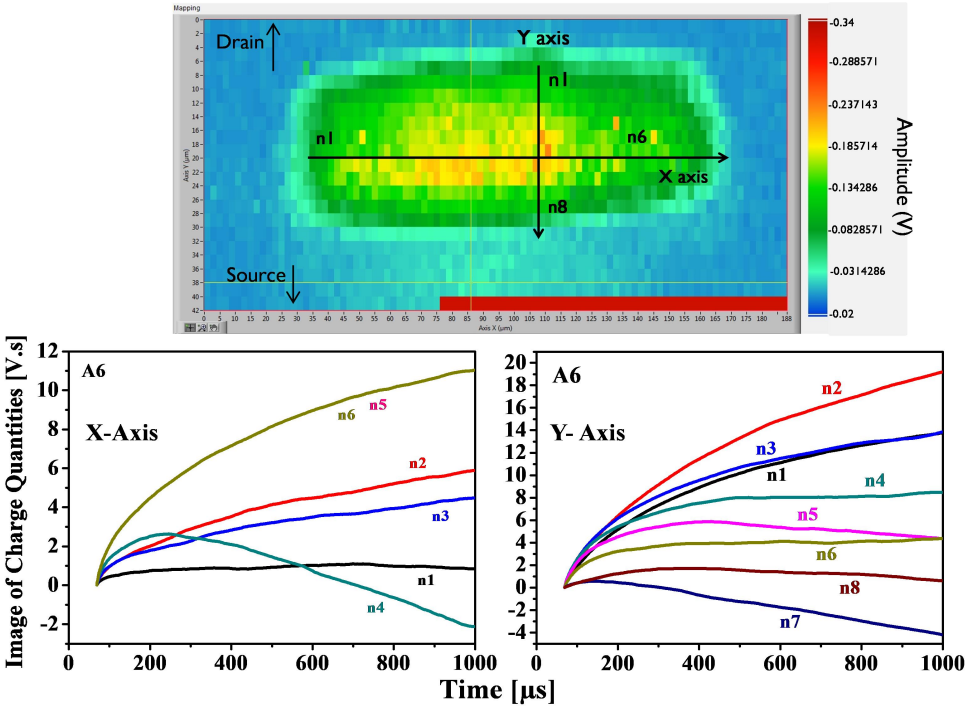

Figure 5.57: Computation of charge contributions for scan points distributed along the X and Y directions of a gate finger.

Here too, oscillations appear in the scan, but at the lower part of the scan, i.e. the beginning. The oscillations in Figure 5.53 and Figure 5.55 appear at gate finger edges, while away from it in Figure 5.57. Thus, the oscillations cannot be attributed to compositional factors. Rather, susceptibility to oscillations seems to appear at the beginning or the end of scans.

By a comparison of the charge contributions from each of the three scan points with the highest transients, point (a) seems to be the point of maximum damage. Several scan points are chosen along the X axis (left to right) and the Y axis (top to bottom). While no real dependence is observed on X position in this particular device, the transients are stronger towards the top of the gate finger. This could be attributed to defects being more prevalent close to the gate-drain edge.

Remarks

Two photon OBIC has proved to be an efficient method to visualize and quantify the damage caused to the belly shape devices subjected to stress laser tests. The large distribution of defects surrounding the gate fingers attests to the role of various surface trap sites near the gate edges responsible for the appearance of the belly shape. In addition, the point of gate breakdown or onset of breakdown could be identified through OBIC imaging as well. For defect points with similar contrast display, computing the charge components associated with the photo transients could be helpful during OBIC measurements interspersed with stress tests to observe the accumulation or deepening of defects states in test devices.

Since most of the devices were already highly degraded, there were some issues with obtaining an image of the device active area. After the observed gate breakdown during the detrapping tests, some control over the gate was still required to allow measuring the photocurrent using the reverse biasing of the gate. However, for several devices, the gate was found to be too damaged and there was a steady flow of leakage which made it impossible to obtain a contrast image. In future endeavours, OBIC tests would be more efficient if performed once the gate leakage begins to irreversibly increase, but before the catastrophic gate breakdown.

5.5 Conclusions and Perspectives

We can infer from the different studies that laser application is an efficient and generally accurate method of detrapping trap components present within the device. Supplementing the device trapping phenomena with additional stress pulses or repeated sweeps enhance the laser effect and allows access to trap contributions not normally observable under steady state conditions. Adding a no-laser sweep prior to the change in laser wavelength or test scenario is an effective method to preserve the initial conditions and activate the traps that might still be unoccupied due to previous

laser-triggered detrappings. However, when dealing with belly shape devices which are already vulnerable to a substantial amount of surface degradation, a very careful approach is needed to minimise further laser-induced damage to the physical quality. Some results point to the possibility of detrapping BS causing traps by laser, which results in a reduced BS. More commonly, the laser serves to activate the growing donor sites which then begin to strengthen the BS. This process is recoverable initially, but causes irreparable damage to the gate characteristic on repeated measurements. The acquisition approach is not effective in these scenarios since they involve multiple laser pulses and thus, hasten the degradation and the eventual breakdown of the gate. The OBIC method is useful in visualization of the defect densities around the gate fingers after device breakdown. Due to the fragility of aged and stressed devices however, it was impossible to continue with this particular device set. Though the results are just the inception, the developed approaches can be directly applied to other device sets to continue the discussion as well as serve as a tool to achieve valuable insight into trapping mechanisms and their occupational transitions.

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CONCLUSION

The GaN based HEMT technologies are leading contenders for the RF, power and optoelectronic markets. The reliability issues that hinder its prospects are being actively researched to allow the GaN systems to utilize its inherent advantages towards widespread applications. Trapping sites, originating from structural non-uniformities during fabrication processes, can be activated or aggravated during small term stresses or long term aging tests. Distributed within the structure, the trapping phenomena obstruct ambitious device development and set limits for power handling or current capability metrics. Further study is essential to address and circumvent trap induced degradations. For this, a deep understanding of trapping physics and occupational dynamics is vital.

During the course of this work, the focus of the analysis into GaN HEMT operation is to recognize the different ways in which traps can affect the device behavior, and how these observations can validate associations between the spatial, energetic, or density distribution of traps with particular occurrences of deviation from an ideal response.

Physical TCAD simulation strategies that support and interpret electrical characterizations is the central method used to investigate the variations in trap processes under constrained environments. Laser characterization is the third axle that attempts to quantify and visualize the trapped states that control the device. The devices used for the study were GH-25 process devices from UMS, built for applications up to 20 GHz.

The core physical attributes of the GaN material and the GaN HEMT have initially been discussed as an overview into the unique merits of this technology, especially the formation and control of the high density two dimensional electron gas. A broad summary of major trap induced reliability and parasitic effects, which deteriorate the device response under different biasing conditions has been presented.

Electrical analysis and numerical simulation methods have been coupled to demonstrate the advantages of a physically derived representative model. Steps to build such models are defined by highlighting the importance of choosing simulation parameters dependent on physical limits, identified by their impact on the sensitive gate leakage characteristic. It serves as a methodology to achieve a stable initial calibration in addition to facilitating better simulation of gate currents.

The six central parameters: metal work function, gate resistance, surface donor concentration, surface donor energy, gate tunneling and spatially distributed traps account for both fundamental as well as parasitic effects present in real devices. Each parameter is individually analyzed, while the other parameters maintain other interactive mechanisms in ideal or dormant states. The choice of the metal work function and gate resistance depend closely on the device's structural composition. Surface donor energy should be chosen according to the pinned Fermi level. The surface donor density needs to be above a threshold value that supports a high enough electric field at gate edges. This prevents gate leakage from spreading in surrounding passivated regions.

The tunneling mechanism is viewed in detail, an essential tool to model Schottky robustness, and comprising a crucial part of both forward and reverse gate leakage. The traps are activated separately in the AlGaN barrier, the GaN buffer, the AlGaN/GaN hetero-interface and at the surface to identify their specific impact on the gate current, which is generally unique to each trap location. This allows the capture of the true effect of a given parameter, untangled and isolated from other mechanisms that might influence or mask its effect. The effects are slightly different for traps defined close to the conduction or valence band. Since the occupations of electron traps close to the valence band are quite constant, they represent the maximal trap effect at a particular density. Traps defined to the conduction band, dominantly captured through measurements, are more sensitive to biasing considerations. The surface traps harm the charge equilibrium and need to be minimal. In the presence of the passivated surface however, we expect the surface traps to be quite low.

The detailed modeling is used to create a methodology that specifies how the simulations of low (I_{Rev}: $V_G = -2$ V-0 V; I_{Forw}: 0V-0.3V) and high bias regions (I_{Rev}: $V_G = -6$V to -3V; I_{Forw}: 0.8 V-1 V) of the forward and reverse gate current can be manipulated through controlling one or more of these six parameters. The gate resistance expectedly controls the forward gate current level for high bias ($V_G > 0.9$ V). The surface donor density, when defined above its necessary threshold has low control otherwise. The surface donor energy dominantly controls the current levels in the lower bias regions of the forward and reverse gate characteristic. The tunneling contribution can dominate the reverse gate current levels. While increasing the forward gate current in the low bias region, it does not affect the currents for $V_G > 0.8$ V thus effecting a change in the current slope. Traps affect the mid to high bias regions of the reverse gate characteristic in distinct ways, but effects on the forward gate is limited to very high bias. An exception is AlGaN barrier traps, which in high densities can alter the slope of the forward gate curve. Since each parameter choice is physically constrained, this automatically allows a deeply physical parameter set while obtaining the best fit to measurements.

To obtain the final fit, validation and slight readjustments within the parameters are required based on output current characteristics. Hence, when we recognize how a certain change in gate current can be linked to a higher tunneling occurrence, or perhaps to traps in the buffer, a comparison with output currents might identify buffer traps as being more probable. This information and the fitting methodology are used to obtain models for four variations of the GH 25 process. This knowledge into individual impact can be very helpful in understanding experimental observations, which are almost always the consequence of a combination of these effects.

The simulation study is then extended from quasi-static simulations to present an alternative outlook towards a deeper, predictive understanding into the origin and extent of trap-induced degradations and their driving factors, but under transient conditions. At the same time, the modelled structure is improved to take into account, the source terminated field plate and the slanted T-shaped gate, key attributes of the UMS technology. Simulations of the gate capacitance variations corresponding to variations in trap location or energy are used to develop links between traps and associated effects. Here too, interface traps pose the greatest threat, especially in the presence of high V_D or high frequency. Three major variations from an ideal C_g characteristic are described in three biasing regions in order to identify how traps might impact the charge distribution within the structure. The effects of frequency on the C_g deviations are also explained. The threshold frequency for which the characteristic begins to deviate is identified around 3.5 GHz.

The first is a fall in the stable C_g peak level while the device is in the on-state, and the effective barrier thickness is between the gate and the channel. This is observed especially at high frequencies. Surface traps are major contributors to this effect. High frequencies additionally strengthen the contributions from barrier and AlGaN/GaN trap. The second effect is a smaller slope when the device is switched from an off (biased beyond the threshold voltage) to on condition. This represents significant lag in the device response, with heterojunction and surface traps being the major limiting factors. AlGaN barrier traps also contribute at high frequencies. Finally, a shift in threshold voltage shifts the entire C_g characteristic towards the right. Buffer and AlGaN/GaN traps are primary causes of this deviation, especially noticeable under low drain biasing conditions.

Based on an analysis into the transient time response under different bias conditions, AlGaN/GaN traps are found to substantially restrict the initial response. Their detrapping is weak under low V_D conditions. However, the detrapping is fast under high V_D, under which circumstances the trapped charges can follow the changes in V_G. Since high frequencies contribute to delay in detrapping under on-state conditions, longer response times weaken the magnitude of its impact.

The impact of surface traps on V_{th} is lower than AlGaN/GaN traps. For surface traps too, high V_D conditions allow better responses to V_G bias. Their effects are however generally high and extremely damaging irrespective of operational conditions.

The detrapping of buffer traps is especially improved under high V_G and V_D conditions. Beyond the V_{th} shift, traps respond well to continued changes in V_G bias, irrespective of V_D. These traps, by virtue of their deep location in the structure only de-trap when bias conditions are changed, and thus are independent of response times. Hence frequency effects are limited.

Barrier traps are damaging in high concentrations and high V_D conditions. Their impact is high when V_G is forward biased and detrapping is much slower. Hence the dispersion from the reference characteristic is amplified. Usually, discharging is fast, unless the response time is very limited, such as with very high frequencies.

The on-resistance analysis deals with the impact of four pulse parameters on trap-induced delay and degradation in the off-on switching response of the modelled device. The bias in the trapping state prior to the on-off transition, the time interval for the transition, and the time and bias for a V_D bias sweep immediately following the transition are considered. Most of the deviation is concentrated in the on-resistance region while the stable drain current levels are not notably altered due to changes in the pulse shape. The major two factors are identified as the trapping voltage before the transition and the time for the current to respond in the V_D bias sweep after the transition. These parameters dominantly control the trap-limited device response, and can dictate the scenarios which would produce heightened performance degradation. The heterojunction traps display substantial increases in on-resistance, when the pulsing conditions are strained. Buffer and barrier trap impacts are similarly affected by pulsing variations.

To apply the developed techniques and information gained into recognizing and characterizing trap effects, the belly shape (BS) parasitic effect is chosen as the case study. It is an increase in the forward gate leakage current, shaped like a "belly", developed after aging tests in GH 25 devices. The objective was to investigate the mechanisms behind this anomalous degradation, as well as understand how the mechanisms are interlinked, to strengthen or weaken the BS magnitude.

The scope of investigation into this effect included initial characterizations performed by UMS that led to the awareness about this effect, developing working hypotheses to serve as foundation to TCAD simulations, re-characterization of BS device after 3 years of room temperature storage, and finally a second round of HTRB aging tests on the previously HTOL aged BS devices.

The first major mechanism that triggers and controls BS is found to be donor –like traps at the surface close to the gate edges. They act to shift the electric field peak from the gate edge

towards the end of the donor region, which supports extensive surface leakage concentrated in the donor area. They are located in sites and defects formed at the degraded surface, due to the high electric field during aging tests. Holes to feed the donor traps could originate from band to band tunneling and are verifiably present in this region since pits and grooves observed in BS devices require holes to fuel the electrochemical reaction that creates these pits in the first place. The location and energy of these donor traps are important. They have maximum impact when defined in a virtual-gate like extension adjoining the drain side of the gate. In this location they are highly dependent on the energetic location. Shallow traps (0.2-0.4 eV from E_C) are essential to obtain high BS magnitudes, especially in the low forward gate bias region. Deeper donor traps (0.5-0.7 eV) too contribute to BS, but their effect is weaker. When the traps are located away from the gate, and closer to the field plate, their impact is considerably weakened, and found to be generally independent of the trap location.

From long term storage results, a part of the shallow donor contribution has been found to be recoverable, but they are liable to be reactivated even on small stresses. The shallow donors are also susceptible to occupational variations, giving rise to random changes in BS magnitudes between a span of minutes or varying measurement sequences. The BS effect is however, rarely fully recoverable. This can be expected since the appearance of belly shape is linked to an irreversible physical surface degradation, which enhances initial device discontinuities in addition to creating further defects, depending upon the severity and duration of aging tests.

Through C_g simulations, causal shallow donor traps near the gate edge are found to trigger faster channel saturation and degrade stable C_g levels following a switching transition by restricting the charge available for $V_G > V_{th}$. They do however support a better turn-on slope. When dominant, shallow donors are found to be equally, if not more, threatening to device performance as acceptor traps, in limiting current response of the devices. Donor traps near the field plate, in contrast are actually beneficial to the charge response, since donors support higher charge levels in the on-state except a small delay in the turn-on transient of the device. As can be predicted, impact of shallow donors close to the gate is more susceptible to high frequency and high bias effects than deep donors. Frequency effects on donors under the field plate are moderate in comparison. They reduce the donor (close to the field plate) induced rise in C_g in the on-state which limits its advantage. The exact energetic location for donor traps to trigger BS is also identifiable for different donor densities using C_g characteristics. Close to these thresholds, the donor impact is minimal. On either side of the energy position however, the steady state C_g level worsens, though moving towards shallower energies does help in a faster turn-on (off-state to on-state) response.

The second fundamental mechanism of the belly shape phenomenon is acceptor traps located in a region of the AlGaN barrier surrounding the gate drain edge, with energies between 0.3 and 0.5 eV. This controls the high bias region of the forward gate curve, where BS current is usually lower than the reference unaged device. These traps are unavoidable in the high stress aging tests which not only strain the barrier layer, but might induce strain-induced defect sites. Some of the BS devices have V_{th} shifts. The aged devices that do not display BS (No-BS) present a uniform decrease in gate current. These observations point towards aging induced acceptor traps. Shallow to moderate acceptor traps are found to be associated to BS, while deeper barrier traps (0.7 eV) are most likely to be responsible for the gate current decrease associated with No-BS devices.

A BS scenario can thus be defined as the combination of shallow and/or medium donors, shallow and/or medium acceptors in addition to a trap assisted tunneling component coupled to both these trap elements allowing the propagation of gate-triggered leakage to the channel. Using simulation, shifts in trap densities as well as formation of new donor trap sites close to the field plate towards final stages of aging can explain the evolution of BS magnitudes through different stages of the aging process.

BS trapping scenarios are detrimental to steady state C_g levels, but support a slightly improved off-on slope. No-BS scenarios show marked deteriorations in both turning-on slope and on-state C_g levels. However, steady C_g levels are better than for BS cases. The BS scenario does not negatively affect R_{on} characteristics following a switching transition, but rather worsens the response at high V_D conditions. For the No-BS case too, when supplemented with trap assisted tunneling, R_{on} degradation is minimal, effects being more important at high V_D. The BS case with donors close to the gate show worst digressions, while with donor traps close to field plate, the impact is contained. For V_G close to the threshold however (V_G=-2 V), donor traps under the field plate are the only traps to display better current levels over the reference for the entire bias range. Above V_D= 2 V, cases with donor traps near the gate edge show high deviations from the reference. With weakening impact of trap-assisted tunneling, the No-BS case presents consistently lower current levels, even in the R_{on} region, with maximum deviation from the reference observed around V_D=2-5 V.

Though three years of room-temperature storage decreased BS magnitudes from the first aging test, a second round of aging was found to boost these amplitudes, even beyond their initial levels, indicating further worsening of the surface quality. Donor traps are found to improve output current levels in the presence of low acceptor traps in the barrier layer. However, they further worsen acceptor induced lowering in output currents, if the acceptor traps are present in high densities. These interactions govern the I_D-V_D response of BS devices after the storage, and after the second

HTRB aging test. The second aging test also introduces substantial unrecoverable R_{on} degradation, which evidence suggests, is unrelated to the donor trap dynamics or even restricted to belly shape scenarios. Some devices also displayed breakdown beyond 80 hours of aging. Both of these could be a result of increased electric field triggered degradations that devices with belly shape might be vulnerable to, owing to their weakened physical character.

Since the appearance of BS or No-BS characteristics is inherently linked to epitaxial quality, BS could be controlled through improved surface and contact engineering, thus restricting trap formation. Further, BS could prove to be a useful reliability indicator to gain insight into surface quality and gate current performance, and help in development of better fabrication processes. However, further detailed investigation and more tests on a wider sample set are essential to understand the susceptibility of BS devices to continued stresses or aging.

The laser techniques applied to a portion of the BS devices have been found to be an efficient and viable method to induce detrapping of trap components with varying energies and time constants. Sample preparation to allow backside laser probing makes the devices fragile however, and hence pulsing parameters were carefully chosen to avoid damaging the device while making simple characterizations. This restricts the biasing and stressing scope of the tests.

Manipulating the chosen laser wavelengths can provide precise information on the trap energies. This process can be strengthened by subjecting the devices to trap filling pulses or repeated characterizations that activate a higher and varied distribution of traps available for response to the laser pulses. Comparing time and laser based recovery provides information into the kind of traps present in each device. Each device has small variations in detected trap energies. All devices displayed a strong detrapping response between the λ= 1610 nm-1700 nm range which is expected to include shallow trap energy contributions in addition to a dominant trap energy close to 0.7-0.77 eV. However, since the studied belly shape devices have already been subjected to repeated stresses, a very careful approach was needed to minimise further laser-induced damage to the physical quality, and ensure that the results were exclusively dependent on trap responses. Despite this, some devices abruptly suffered breakdown during the sample preparation, initial characterizations or laser stresses which restricted the statistical range of the observations from different devices. One of these devices was the No-BS sample, because of which, we were unable to make a direct correlation between BS and No-BS responses to the laser.

Nevertheless, some results point to the possibility of detrapping BS causing traps by laser, which results in a reduced BS. More often however, the laser pulses seem to feedback energy to the donor sites which then begin to strengthen the BS. Repeated several times to visualize the extent of

this degradation, irreversible damage to the gate characteristic is observed, which makes the device prone to sudden gate breakdown within the next couple characterizations. The acquisition approach, with multiple laser pulses that scan the entire device is not as effective in these scenarios since they hasten the degradation. The laser testing methods should be employed on a wider device set, to allow stronger and varied initial device states to trigger specific detrapping modes in response to laser pulses of definite energies. The two photon OBIC method is useful in visualizing the point of breakdown in such devices as well as defect densities around the gate fingers after device breakdown. It would be very interesting to perform T-OBIC comparisons between successive tests to gauge the extension of defects. There is a good potential for further studies on these observations, especially the laser interaction with the traps responsible for BS. In addition, twice aged BS and No-BS devices could also be compared through laser techniques to understand what nature of stress makes BS devices susceptible to breakdown. These tests could offer conclusive evidence regarding the threshold of degradation beyond which BS devices become highly probable to suffer catastrophic gate breakdown. Developed testing approaches can be directly applied to the next sets to continue a comprehensive investigation into occupational transitions and trap dynamics.

APPENDIX

Capacitance Voltage Characteristics for BS Scenarios

A. DEPENDENCE ON DONOR TRAP POSITION

The magnitude of the observed belly shape has been found to be dependent on the region in which the donor traps are defined at the surface interface. Close to the gate-drain edge with maximal electric field, they have stronger impacts and show substantial modulation with the chosen energy position. When defined under the field-plate, the BS is greatly reduced and independent of the energy position of the donor traps.

Donors near the Gate-Drain edge

The BS response obtained due to shallow donors near the gate edge with a L_{ext}= 0.3 µm and medium acceptor traps in the barrier (defined in $L_{ext,A}$= 0.6 µm around the gate-drain edge) is first considered while the No-BS response is due to deeper acceptor traps. The corresponding C_g curves are presented in Figure 1 for a moderate frequency of 5 GHz for V_D= 2, 5 and 10 V.

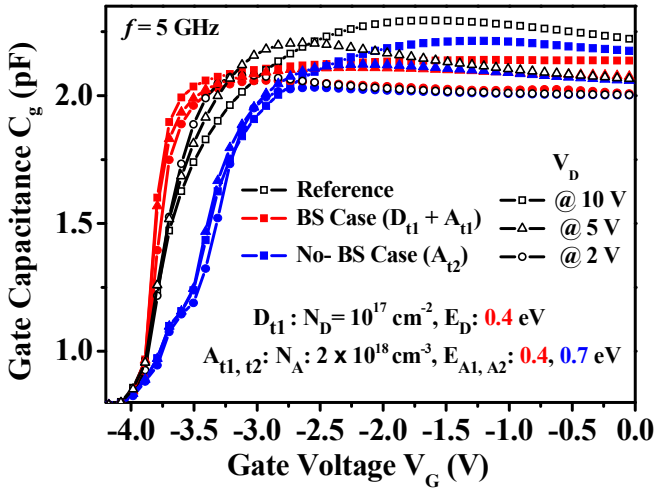

Figure 1: C_g-V characteristics for reference, BS and No-BS scenarios at V_D= 2, 5 and 10 V

Shallow donors are observed to hasten the turn-on in Region 2 which reflects faster channel saturation. However, the BS case at high V_D fails to sustain the required charge at higher V_G which

results in significant lower C_g levels in Region 3. With the deeper acceptors in the No-BS case, the Region 2 slope deteriorates significantly due to slower de-trapping.

While the response in Region 3 at V_D= 2 or 5 V is similar to the BS case, the recovery at higher V_D is better in the No-BS case with a smaller deviation from reference C_g levels.

The electric field distribution along the lateral device length is demonstrated in Figure 2 for the key bias points of V_G= -3.5 V (left) and V_G= -2 V (right) in the center of Region 2 and Region 3 respectively. Close to V_G= -3.5 V close to V_{th}, the electric fields are higher surrounding the gate. The low electric field within L_{ext} for the BS case induces the leakage current. The field recovers rapidly and overshoots for lengths beyond L_{ext}.

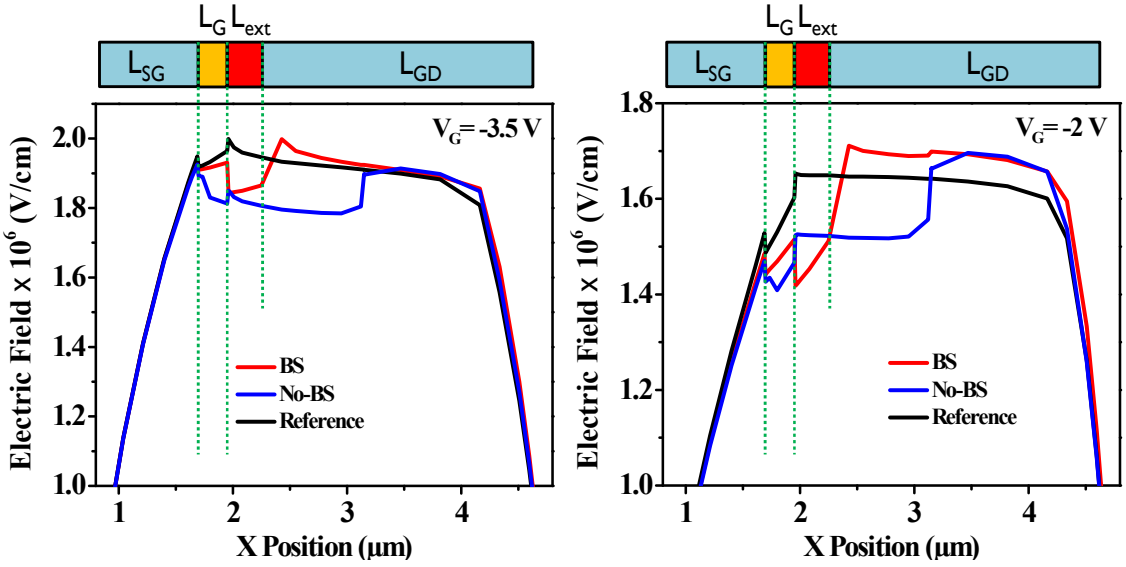

Figure 2: Electric field distribution for reference, No-BS and BS cases at V_G=-3.5 V and V_G=-2V

Eventually, as we move away from the gate, the BS and reference curves become similar. The No-BS curve due to deep acceptors in the barrier displays a significantly lower field and thus suffers from reduced charges until very deep into the gate-drain passivation length, away from the gate, where it finally recovers and approaches the reference values.

At V_G= -2 V, the disparity between the three cases is amplified, however the tendency remains similar. Within L_{ext}, the field for the BS case is lowest, falling below the No-BS curve. Deeper within L_{GD}, the BS and No-BS fields are similar and higher than the reference leading to the general reduction in C_g levels as previously observed in Figure 1.

The conduction band energy E_C distribution at V_D= 10 V is also compared along the device Y axis in Figure 3 for V_G= -3.5 V (left) and V_G= -2 V (right).

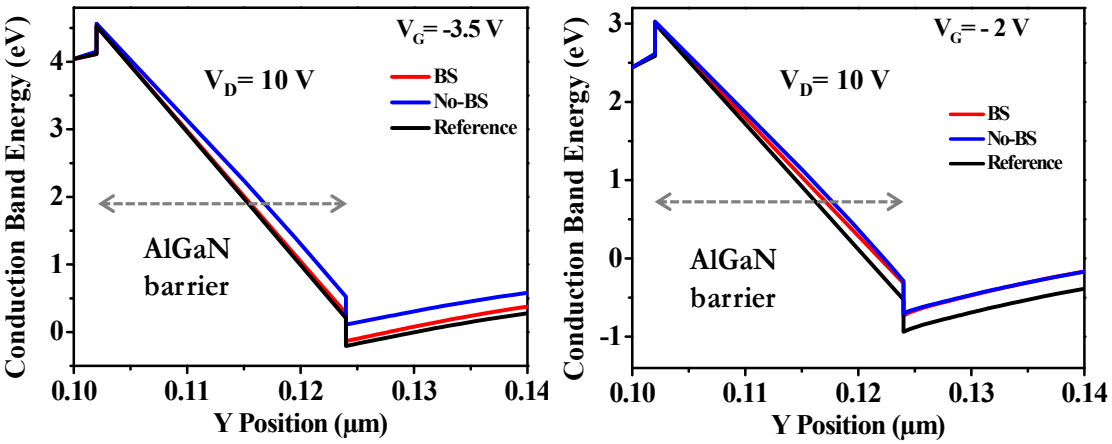

Figure 3 Conduction band energy for reference, No-BS and BS cases at V_G=-3.5 V and V_G=-2V

Charge near the channel for the BS case is lower than the reference for V_G=-3.5 V as reflected in the higher E_C near the AlGaN/GaN interface. However the surge in gate leakage for greater V_G compensates, resulting in the faster turn-on response in Region 2 (Figure 1). The No-BS E_C levels are noticeably higher indicating the presence of substantial trapped charges and reduced current levels. At V_G= -2V, it is apparent that the BS and No-BS scenarios are very close and display a higher E_C near the channel, indicating the loss of available charge and thus current. Thus, the BS occurrence could prove to be quite detrimental to the device response for on-state conditions.

Donors near the Field Plate

Figure 4 displays C_g for donors defined under FP with otherwise identical parameters. The donor trap response is markedly different from the previous characteristic obtained for donors near the GD edge in Figure 1. While donors near the gate-drain edge are dominant near V_{th} and degrade the saturated C_g levels, donors near the FP have a contrasting effect.

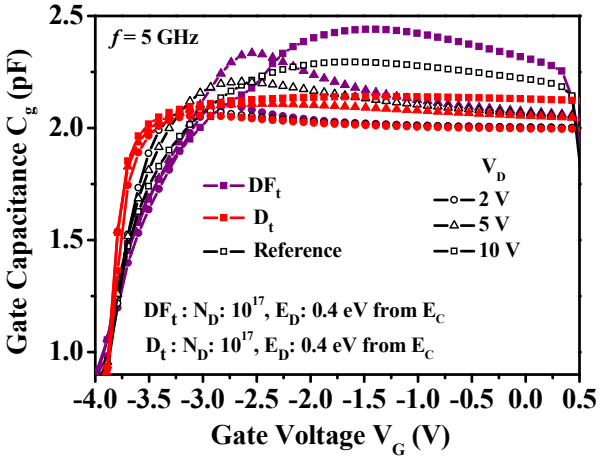

Figure 4 C_g-V characteristics for donor traps near the GD and FP edge at V_D= 2, 5 and 10 V.

They cause a delayed turn-on response, with C_g levels in Region 2 lower than the reference. The delayed de-trapping however produces a boost in current for higher V_G where the additional donors support greater conduction. A significant charge overshoot over reference levels is observed at the end of Region 2, especially for higher V_D values. Stable C_g levels in Region 3 remain higher than the reference for V_D= 10 V, with an additional channel density component due to the donor support. Thus, donor traps away from the gate-drain edge are far less detrimental with respect to leakage and under steady state conditions.

B. TRAP ENERGY THRESHOLDS FOR BS OCCURRENCE

The C_g-V characteristic is very sensitive to small changes in the charge distribution within the structure. It reflects changes that might not be identifiable from the I_G-V_G characteristic. Hence, it's an ideal tool to take a closer look into the impact of donor density and energy on the device behavior. Especially, precise thresholds for E_D might be identified when BS just becomes apparent.

Figure 5 presents how E_D thresholds can be extracted for two donor trap concentrations = 10^{16} cm^{-2} and 10^{17} cm^{-2} defined near the gate-drain edge by recognizing the point of transition from general to belly shape nature. It also compares effects of strengthening or weakening of BS as the energy positions are pushed further from the identified thresholds. For N_D= 10^{16} cm^{-2}, the E_D threshold is 0.71 eV for which the C_g curves are just above the reference in Region 2, and just below in Region 3. At this condition, I_G and I_D characteristics would remain unaffected. As we move E_D further away from E_C, the BS induced leakage should be weakening. However, C_g levels continue to uniformly degrade in Region 3, which is further magnified at higher V_D. This manifests as a loss of V_D control on the C_g response.

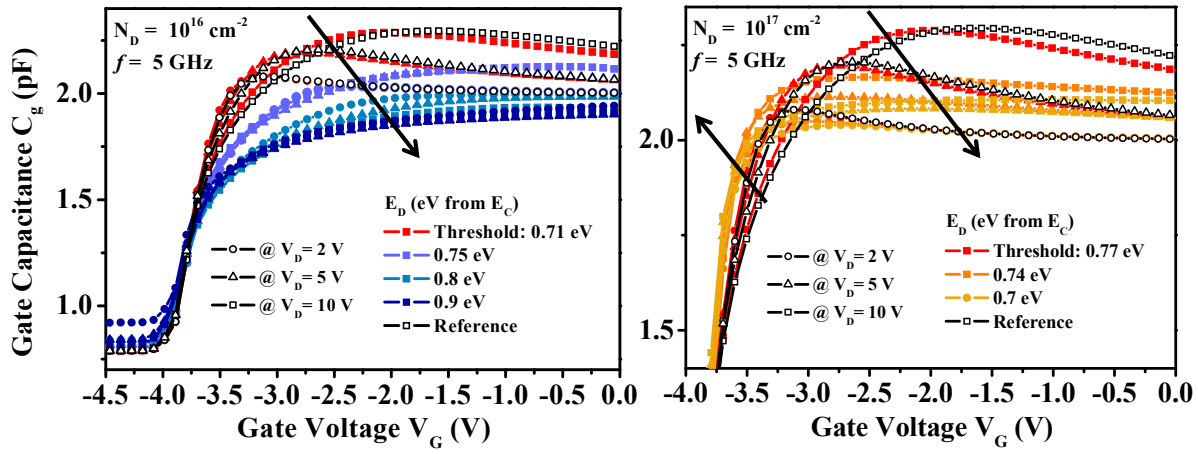

Figure 5: C_g characteristics for (left) N_D=10^{16} cm^{-2} and weakening BS conditions and (right) N_D=10^{17} cm^{-2} and strengthening BS conditions

The Region 2 peaks are lower as the slope progressively increases for deeper traps, similar to the impact of acceptor traps. Thus, the presence of deeper donor traps, while limiting BS-induced leakage, limits the maximal available charge, affecting steady state I_D-V_D levels considerably.

For N_D= 10^{17} cm^{-2}, the E_D threshold is identified as 0.77 eV. In this case, the E_D values are brought closer to E_C to study the impact of aggravating BS induced effects. The Region 2 slope expectedly improves due to the gate current build-up, however, the peaks at the end of Region 2 start declining. C_g levels in the beginning of Region 3 are substantially worsened, resembling again, the effect of acceptor traps. In contrast to Figure 5 (left) for deeper traps, C_g levels near V_G= 0 V show good recovery for V_D= 2 or 5 V with nominal dispersion from reference, although all donor trap induced responses are noticeably diminished for V_D= 10 V. Hence, the presence of stronger BS, in addition to promoting gate leakage, negatively disturbs on-state device operation.

Similarly, E_D thresholds are extracted for N_D =10^{15} and 10^{18} cm^{-2} as shown in Figure 6.

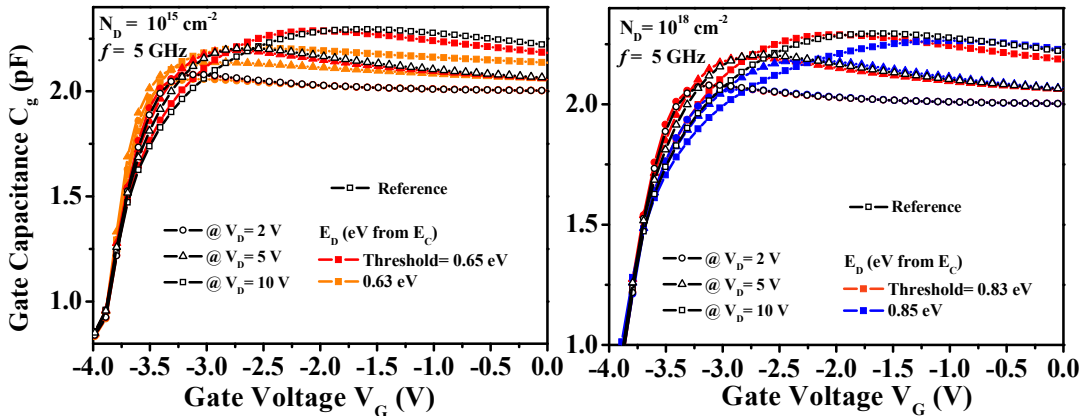

Figure 6: C_g characteristics with E_D thresholds for (left) N_D=10^{15} cm^{-2} and (right) N_D=10^{18} cm^{-2}

The extracted E_D thresholds are located 0.65 eV and 0.83 eV away from the E_C for N_D= 10^{15} and 10^{18} cm^{-2} respectively. Close to these values, C_g deviations are limited, and restricted to changes around Region 2.

From these results, we find that for every order of increase in N_D, the E_D threshold shifts away from E_C by 0.06 eV. This value describes the importance of the trap position relative to stress or bias induced changes in donor trap densities. For comparison, Figure 7 displays the change in simulated C_g response for an identical trap energy E_D= 0.4 eV when the trap density N_D is increased from 10^{17} to 10^{18} cm^{-2}. At a higher N_D, the Region 2 slope improves and a higher peak is observable at the end of Region 2. This corresponds to a better turn-on characteristic for the device. The changes in Region 3 are negligible. Thus, for a given E_D, a higher N_D produces a slightly better C_g response.

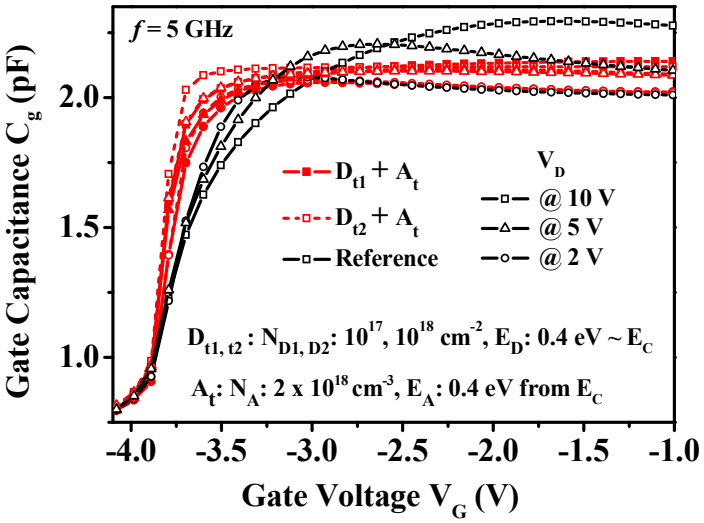

Figure 7 C_g response for surface donor traps close to the gate-drain edge with E_D= 0.4 eV and varying N_D

Perspective

We can conclude that close to the E_D thresholds inducing BS at a given N_D, the impact on C_g is nominal and the effects on I_G or I_D might be unidentifiable. For small deviations around the threshold E_D, recovery is possible under favorable biasing conditions. However, the associated issues while latent are nevertheless present owing to physical device configurations, and can become important under alteration of trap occupational conditions.

The damage potential of surface traps is majorly controlled by the energy position. Energetically deeper traps cause severe detrapping delays that affect efficiency and performance. Shallower traps, the major contributor to BS, have a slightly better impact on C_g, since the charge degradation in Region 3 is at least accompanied by a favorable Region 2 response. In higher concentrations, the enhancement in Region 2 is reinforced. However, their impact is not just limited to I_G-V_G and augmentation of the BS feature. The diminished C_g saturation levels can be expected to create issues in various operational circumstances.

C. FREQUENCY EFFECTS ON C-V RESPONSE OF BS CASES

To investigate how frequency affects the contributing mechanisms of the BS effect, the C_g characteristics of surface traps for variations in frequency is simulated.

Figure 8 presents C_g-V curves for shallow donor traps located E_D= 0.3 eV from E_C for a frequency range from 5 MHz to 15 GHz at V_D= 5 V and V_D= 10 V.

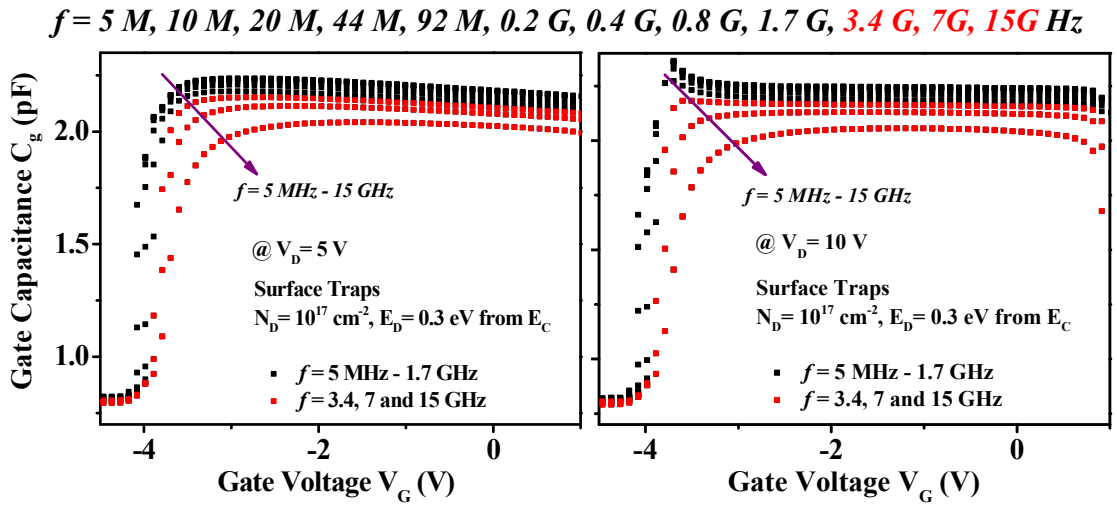

Figure 8: C_g-V behavior for shallow donors at different frequencies at (left) V_D= 5 V (right) 10 V

The benefit of donor traps on the C_g characteristic is a rapid Region 2 response. However, starting from moderate to high frequencies, this advantage weakens as the peak of Region 2 deteriorates. The general trap-induced reduction in Region 3 is also worsened further due to the high sensitivity to frequency. At higher V_D, effects are similar but heightened.

Similarly, the C_g-V nature with deep donor traps located E_D= 0.7 eV away from the E_C is plotted in Figure 9 for varying frequencies.

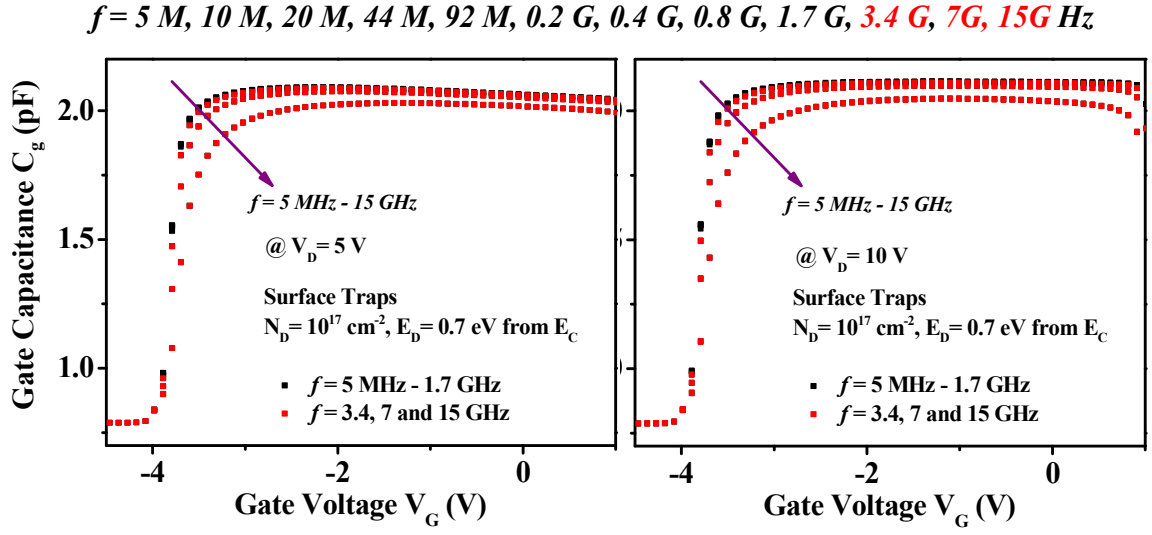

Figure 9: C_g-V behavior for deep surface donor traps at different frequencies for (left) V_D= 5 V and (right) V_D= 10 V

In this case, compared to Figure 8, trapped charges display a substantially reduced sensitivity to frequency. De-trapping is dominantly controlled by the energy position and hence the frequency threshold for deviation is much higher at f= 3.4 GHz.

The effects, while small, lead to a worsening of C_g surrounding the threshold voltage near the transition from Region 2 to 3. For a frequency of 15 GHz, a slight reduction in the Region 3 levels is also observed.

D. RELATIVE IMPACT OF BS INDUCING TRAPS ON C-V

To take a deeper look at trap induced dispersion from the reference C_g nature, Figure 10 plots the relative impact of shallow and deep donor traps on device behavior for the range of frequencies, obtained as follows for V_D= 5 and 10 V:

$$\Delta C_g(\%) = \left(C_{g,Ref} - C_{g,Trap}\right)/C_{g,Ref} \times 100$$

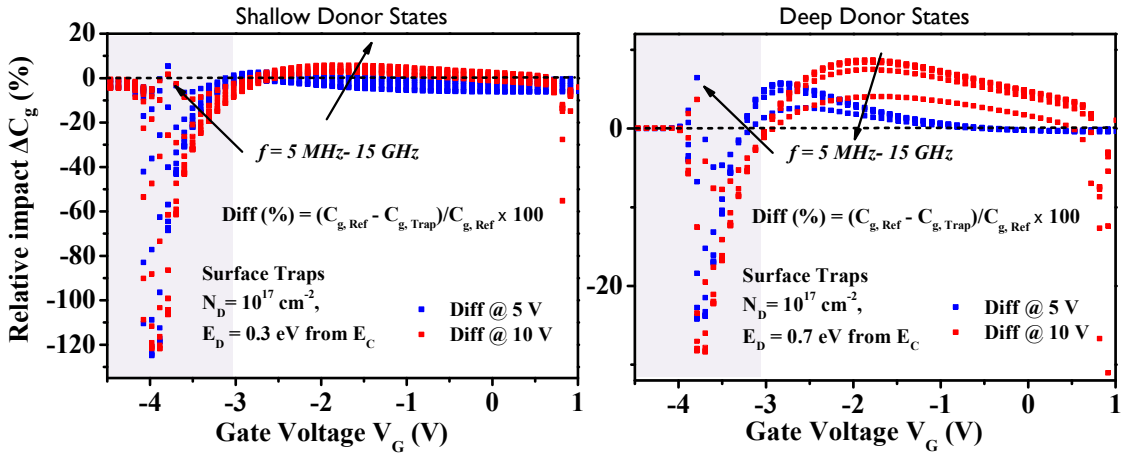

Figure 10: Relative impact of shallow and deep donor states compared to reference C_g response

The major extent of dispersion is confined to V_G= -4 V to -3 V as the device turns on in response to V_G exceeding the threshold voltage. Shallow donors cause an appreciably higher C_g in region 2 and hence a greater deviation from the reference. An increase in frequency however limits the maximal ΔC_g. For deeper traps, the nature is similar but ΔC_g levels are much smaller. Effect of drain voltage is minimal in this region for both trap energies.

Beyond V_G= -3 V, a comparative study can be made based on Figure 10 which concentrates on the changes in Region 3. Shallow traps at the lower V_D show good recovery for most of the frequency range, where deviation from the reference is minimal. In fact, despite the lower C_g peaks at the end of Region 2, ΔC_g remains negative in most of Region 3, which indicates favorable charge levels and a higher C_g compared to reference. Shallow traps at the lower V_D show good recovery for most of the frequency range, where deviation from the reference is minimal. In fact, despite the lower C_g peaks at the end of Region 2, ΔC_g remains negative in most of Region 3, which indicates favorable charge levels and a higher C_g compared to reference.

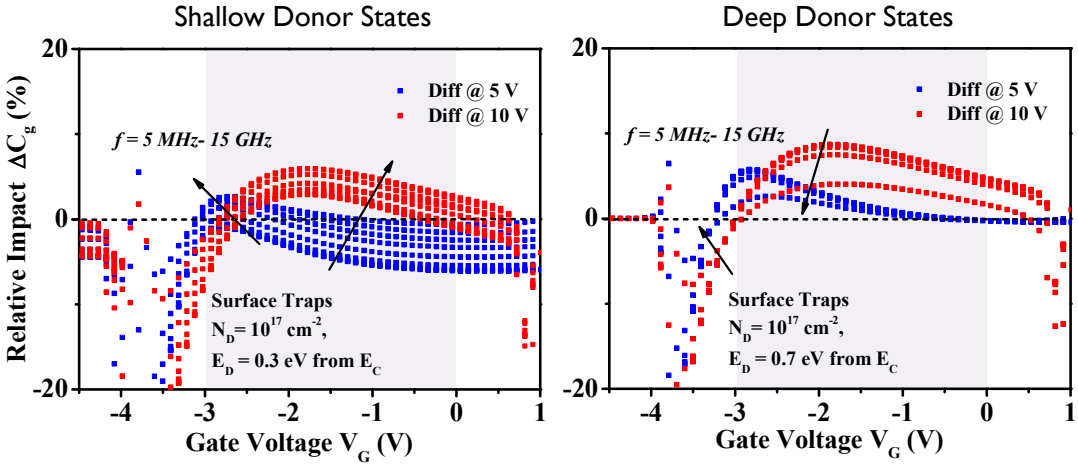

Figure 11: Closer look at relative impact of shallow and deep donors on C_g behavior in Region 3

For frequencies higher than 100 MHz, ΔC_g for shallow traps is observed to steadily worsen as the advantageous dispersion for V_D= 5 V is minimized and the detrimental deviation for V_D= 10 V grows higher.

Deeper traps present positive ΔC_g levels for both V_D values illustrating the general depreciation in C_g magnitudes in Region 3. Frequency effects are relevant only beyond 4 GHz and actually act to decrease the disparity since deeper trap occupancies are restricted at very high frequencies. At V_D= 5 V, the loss in Region 2 peaks are higher than for shallow traps and no favorable overshoot above the reference is observed.

However, ΔC_g is trivial at higher V_G, where the C_g values coincide with reference levels. For V_D= 10 V, ΔC_g is higher and remains strongly positive even for $V_G \approx 0$V.

Donor traps under the field plate and away from the GD edge have also been studied similarly. Figure 12 and Figure 13 present the C_g characteristics for varying frequencies and the corresponding ΔC_g nature for traps with N_D= 10^{17} cm^{-2} and E_D= 0.4 eV from E_C.

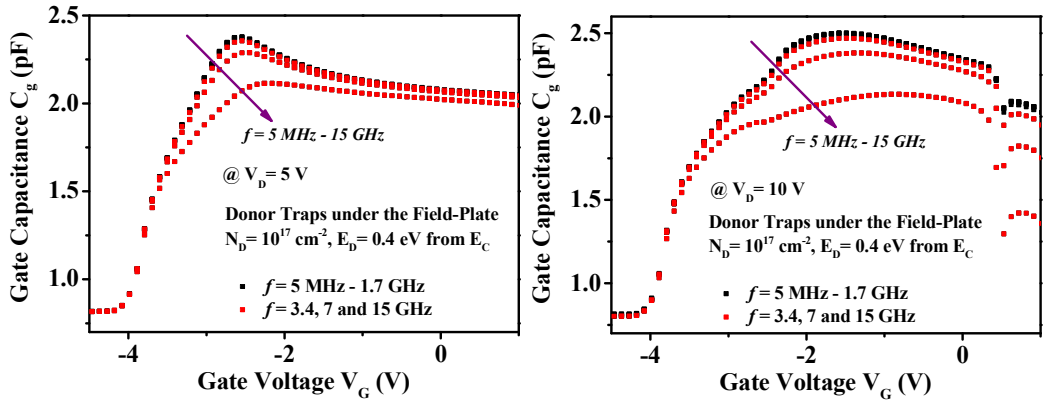

Figure 12: C_g-V behavior for shallow donor traps under the FP at different frequencies for (left) V_D= 5 V and (right) V_D= 10 V

It is noticed that similar to energetically deeper traps, traps spatially located away from the GD edge have frequency threshold near 4 GHz. For f= 7 GHz or 15 GHz, the Region 2 response worsens considerably for V_D= 5 V. For V_D= 10 V, the fall in the C_g peak extends into substantially lower C_g values throughout the V_G= -3 V to 0 V regime.

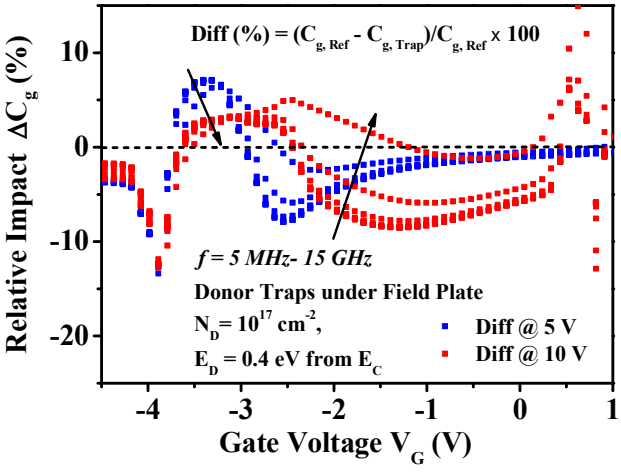

Figure 13: Relative impact of shallow donor states under the FP on C_g behavior

As observed from Figure 13, the initial favorable deviation from reference in Region 2 is smaller for traps under FP since they do not significantly influence the gate leakage responsible for a faster device response in this area. The positive ΔC_g region of degradation is restricted to the overshoot around V_{th} near the end of Region 2. The peak positive ΔC_g is higher at V_D= 5 V but recovers fast as V_G rises. For V_D= 10 V, ΔC_g peak is lower but extends over a wider V_G range. For most curves, delayed detrapping results in a favorable recovery deeper in Region 3 where C_g levels are higher than the reference until high V_G when ΔC_g tends to zero. High frequencies reduce the dispersion in both Region 2 and Region 3, as especially noticeable for f= 15 GHz at V_D= 10 V.

Perspective

The BS trap combination is found to severely affect Region 3 charges, while the Region 2 response is slightly faster. The No-BS scenario causes a strong deterioration in Region 2 though the fall in Region 3 is less critical compared to BS. Donor traps near the gate drain edge, which is the main contributor to the belly shape, has been found to be significantly detrimental to the charge response of the simulated device, as reflected in the C_g-V characteristic. Donor traps near the field plate, in contrast are actually beneficial to the charge response, barring a small delay in the turn-on response of the device. As V_G rises, and the device moves deeper in the on-state, the donor traps near the GD edge degrade the C_g response similarly to acceptor traps which implies that they similarly limit the current performance of the device. Precise E_D thresholds have been identified

through C-V comparisons which have demonstrated the importance of the donor energy position. Near its threshold, the induced BS is the least detrimental to C_g. Other energy positions, shallower or deeper negatively impact the charge available within the device, though shallower energies help the Region 2 response. As expected, shallow donors near the gate are found to be more susceptible to frequency effects than deep donors. Donors under the FP are moderately affected. For high V_D and high frequencies, the effects of shallow donor states worsen. Higher frequencies also reduce relative difference in C_g for donors under the FP, which limits its favorable effects in Region 3.

LIST OF PUBLICATIONS

Peer Reviewed Journals

K. Mukherjee, F. Darracq, A. Curutchet, N. Malbert and N. Labat, "Transient Simulation Strategies for Insight into Gate Leakage Artefact observed in GaN HEMTs", IEEE Transactions on Microwave Theory and Techniques. (Submitted)

K. Mukherjee, F. Darracq, A. Curutchet, N. Malbert and N. Labat "TCAD simulation capabilities towards gate leakage current analysis of advanced A1GaN/GaN HEMT devices" Microelectronics Reliability Vol. 76-77, pp. 350-356, 2017. doi. https://doi.org/10.1016/j.microrel.2017.07.049

Peer Reviewed Conferences

K. Mukherjee, F. Darracq, A. Curutchet, N. Malbert and N. Labat, "Investigation of the trap-limited transient response of GaN HEMTs," *2018 International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMIC)*, Brive La Gaillarde, 2018, pp. 1-3. doi: 10.1109/INMMIC.2018.8430007

K. Mukherjee, A. Curutchet, F. Darracq, N. Malbert and N. Labat, "Investigation of trapping behaviour in GaN HEMTs through physical TCAD simulation of capacitance voltage characteristics," *2018 19th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE)*, Toulouse, 2018, pp. 1-7. doi: 10.1109/EuroSimE.2018.8369924

K. Mukherjee, F. Darracq, A. Curutchet, N. Malbert and N. Labat, "Comprehensive study into underlying mechanisms of anomalous gate leakage degradation in GaN high electron mobility transistors," *2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA, 2018, pp. 4B.4-1-4B.4-9. doi: 10.1109/IRPS.2018.8353581

K. Mukherjee, F. Darracq, A. Curutchet, N. Malbert and N. Labat, "Advantages of T-CAD Simulation towards investigation of reliability concerns in GaN HEMTs for RF Power Applications", *BEE Week at IEEE IMS and MTT-S Day*, IEEE Student Branch, France Chapter, Nov 2017.