Analysis of single event radiation effects and fault mechanisms in SRAM, FRAM and NAND Flash : application to the MTCube nanosatellite project

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Application to the MTCube nanosatellite project

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Abstract

Space radiation is a harsh environment affecting all electronic devices used on spacecraft, despite the presence of Earth's protective magnetic field in Low Earth Orbit (LEO). Although particles inducing total ionizing dose (TID) can be effectively shielded against in LEO, particles responsible for Single Event Effects (SEEs) remain an issue for the reliability of electronics. This is particularly of concern considering the increasing use of Commercial-Off-The-Shelf (COTS) components, not designed for space applications. In the frame of this thesis, the SEE response of three commercial memory types are explored: SRAM, FRAM and NAND Flash. Based on SEE test results, the possible fault mechanisms induced by SEE particles on those devices are analysed. In order to study and compare the devices' response with actual in-orbit measurements, the RES (Radiation Effect Study) science experiment was developed and is presented. The RES experiment will be the payload of the MTCube (Memory Test CubeSat) nanosatellite, which is being developed at the University of Montpellier as a joint project between the University Space Center (CSU Montpellier-Nîmes), as well as the LIRMM and IES laboratories. The MTCube project is financed jointly by the European Space Agency (ESA) and the Van Allen Foundation (FVA).

Résumé

L'environnement radiatif spatial est un environnement sévère qui agit sur tout composants électroniques embarqués sur des engins spatiaux, y compris sous le bouclier naturel que nous procure le champ magnétique terrestre en orbite basse. Bien qu'il soit possible, en particulier à ces orbites, de se protéger efficacement contre les particules créant de la dose totale ionisante, cela pose plus de difficultés pour les particules générant des effets singuliers. Cela est d'autant plus un problème que l'utilisation des composants commerciaux (dits « COTS »), non conçus pour de telles applications, sont de plus en plus utilisés. Dans le cadre de cette thèse, les effets singuliers sur trois types de mémoires sont étudiés: SRAM, FRAM et NAND Flash. En se basant sur l'analyse des résultats de tests, les mécanismes d'erreurs induits par des particules générant des effets singuliers sont analysés. Avec pour objectif d'étudier et comparer la sensibilité de ces mémoires directement en orbite, l'expérience RES (Radiation Effect Study) a été développée et est présentée dans ce manuscrit. Cette expérience scientifique constituera la charge utile du nanosatellite de type CubeSat nommé MTCube (Memory Test CubeSat) developpé à l'Université de Montpellier en collaboration entre le Centre Spatial Universitaire Montpellier-Nîmes, et les laboratoires LIRMM et IES. Le projet MTCube est financé conjointement par l'Agence Spatiale Européenne (ESA) et la Fondation Van Allen (FVA).

To my Mum,
Yasmeen Kapadia,
that we still miss so much everyday
but who keeps inspiring me!

माँ,
मैं तुम्हें प्यार किया,
तुम्हें प्यार करता हूँ,
और तुम्हें हमेशा प्यार करूंगा !

« (Si)[1] *j'ai fait un peu de bien ; c'est mon meilleur ouvrage »*
Voltaire, Epîtres à Horace

[1] *(phrase légèrement modifiée avec l'ajout de la conjonction de subordination)*

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List of Abbreviations

amu	Atomic Mass Unit
AOCS	Attitude and Orbit Control System
BL	Bit Line
BOL	Beginning Of Life
bps	bits per seconds
CAN	Controller Area Network
CERN	Centre Européen de Recherche Nucléaire (European Nuclear Research Centre)
CME	Coronal Mass Ejection
CMOS	Complementary Metal Oxide Semiconductor
CNES	Centre National d'Etudes Spatiales (French Space Agency)
COTS	Commercial Off The Shelf
CSU	Centre Spatial Univeristaire (University Space Centre) Montpellier-Nîmes
DD	Displacement Damage
DR	Data Rate
GCR	Galactic Cosmic Ray
GEO	Geostationary orbit
ECC	Error Correcting Code
EDAC	Error Detection And Correction
EEE	Electrical, Electronic and Electro-mechanical
ELDRS	Enhanced Low-Dose Rate sensitivity
EMC/EMI	Electromagnetic Compatibility/Electromagnetic Interference
EOL	End Of Life
EPS	Electrical Power Subsystem
ESA	European Space Agency
FPGA	Field Programmable Gate Array
FRAM	Ferroelectric Random Access Memory
FSM	Finite-State Machine
FWF	Full Word Failure
HK	Housekeeping
IC	Integrated Circuit
IWF	Intermittent Word Failure
JPL	Jet Propulsion Laboratory
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LIRMM	Laboratoire d'Informatique, Robotique et Microélectronique de Montpellier (Computer Science, Robotic and Microelectronic Laboratory of Montpellier)
MTCube	Memory Test CubeSat
MCU	Multiple Cell Upset
MBU	Multiple Bit Upset
MLAN	Mean Local Time of the Ascending Node
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
NASA	National Aeronautics and Space Administration
OBC	On-Board Computer
OBDH	On-Board Data Handling Subsystem
OSL	Optically Stimulated Luminescence
PCB	Printed Circuit Board
PL	Plate Line
RADIAC	Radiation et Composants (Radiation & Components research group)
RBF	Remove Before Flight
RES	Radiation Effects Study by SEE Experiment on CubeSat
radhard	Radiation-Hardened

SEB	Single Event Burnout
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SSO	Sun Synchronous Orbit
SEP	Solar Energetic Particles
SSR	Solid-State Recorders
SRAM	Static Random Access Memory
SV	Sensitive Volume
TC	Test Campaign
TID	Total Ionizing Dose
TNID	Total Non Ionizing Dose
TRL	Technology Readiness Level
TTC	Telemetry, TeleCommand Subsystem
VL	Vertical Lines
WL	Word Line

Introduction

Curiosity, the most recent Mars rover, experienced in February 2013 an issue with its 2 GB Flash memory (used for addressing memory files) leading to an automatic switch from the nominal on-board computer to the redundant one [JPL, 2016]. This major safety action usually happens when a major error occurs in the nominal functionality of a space system. As mentioned by Richard Cook, the Curiosity project manager at JPL and reported in [Arstechnica, 2016]: "*The hardware that we fly is radiation tolerant, but there's a limit to how hardened it can be. (...) You can still get high-energy particles that can cause the memory to be corrupted. It certainly is a possibility and that's what we're looking into*". Figure 1 shows an auto-portrait of this rover on Mars.

Figure 1: Curiosity rover auto-portrait on the Martian surface which suffered from glitches on its Flash on-board memory potentially due to radiation effects.

As can be seen through this recent example, the sources of failure are numerous for components used in space applications, one of them being radiation against which mitigation technics may not necessarily be enough. In fact, since the dawn of the space era, radiation has been an issue for space electronics leading to minor glitches up to major issues. This is even more of a concern on non-radiation-hardened by design components, such as Commercial Off The Shelf components (COTS) which are increasingly used in space applications, as well as new components with very little or no flight heritage.

In this context, the current work addresses the radiation effects of different memory technologies focusing on a particular type of radiation effect: Single Event Effects (SEE). Due to the miniaturisation of electronic components, SEEs are becoming an increasing threat to electronic components even more than Total Ionizing Dose (TID) effects. Memories, due to their nature of storing binary information, are able to record and keep track of some of the effects induced by single

events. Besides, relatively recent memory technologies require more flight heritage for potential use in future space applications. In this work, are presented memory radiation test results; and analysing those results, the potential source of failure mechanisms are investigated based on test methods previously developed in our research group. These analyses may be useful to better understand the impact of single events on these components, understand the impact on various memory technologies and even be used in order to further harden devices.

This work will be used in order to prepare the scientific output of the MTCube nanosatellite CubeSat project. This 1-Unit CubeSat's scientific goal is to collect real in-orbit data on the tested memories and analyse the SEEs occurring during the two-year mission. Hence, parallel activities were undertaken in order to start the MTCube project, estimate the type of scientific data collected by the science experiment of the mission, design, build and test the science experiment. Currently, the project is on track for an expected launch in 2018 in a low earth polar orbit.

The undertaken work will be presented as follows: in chapter 1 will be presented the space radiation environment in order to understand where radiation comes from and how components may be impacted by them. Considerations of the shielding impact of the overall spacecraft will also be briefly discussed. Examples will be provided of actual missions which were impacted by radiation effects with the objective of showing that any type of mission is at risk. The use of COTS components in space projects will be introduced and then, the MTCube mission will be presented, first focusing on its objectives, then on the mission analysis, which was initially performed to ensure the feasibility of the mission.
Chapter 2 will then briefly present the main mechanisms inducing SEE in electronic components, which will allow a better understanding of the parameters and concepts used to assess the sensitivity of a memory. The various test campaigns performed in the frame of this work, as well as the test bench, test methods and facilities will be introduced.
Chapter 3 will then focus on the test results focusing on SRAM volatile memories. First, the components selected for the MTCube mission will be described. Then, a general overview will be provided regarding the radiation effects on those components (not necessarily focusing here on SEE). Test results will then be presented and types of errors and their occurrence will be studied.
Similarly to chapter 3, chapters 4 and 5 will be dedicated to two non-volatile memories, respectively FRAM and NAND Flash memories. After a general overview of the radiation effects occurring on these types of memories, the test results and analysis for these memories will be presented.
This will then lead to chapter 6, where will be shown how the current experimental work undertaken on these memories is used to prepare the scientific experiment of the MTCube project. It should be noted that the current work can also be used for other missions. Based on the experimental data, the expected in-orbit average error rate for each memory will be estimated using available tools commonly used for space applications. This information will be valuable in order to compare the experimental results with those collected when the actual mission will begin. The in-orbit acquired data may be directly compared with the work described here to provide more insights into the failure mechanisms occurring in a real space environment.

Chapitre 1

Context of the current study

1.1 Near Earth space radiation environment

In order to ensure the good functionality of satellites for the duration of their mission, the harsh space radiation environment has been and remains an important aspect to be considered during the design phase for all types of missions, from low earth orbit (LEO) to interplanetary missions. Radiation designates a field of particles (or electromagnetic waves), which can be ionizing or non-ionizing.

Other environmental aspects such as vacuum, thermal, atomic oxygen in upper atmosphere, micrometeorites, charging due to plasma of electrons and protons have to be considered as well, but they are out of the scope of this work. According to [Ecoffet, 2011] based on studies from [Bedingfield, 1996], 45% of spacecraft anomalies related to the space environment are due to radiation, and 29% are due to plasma. This proves that not only radiation was of concern since the very early ages of the space era, but is still of concern in current space missions, increasing the risk of jeopardising partially, or even worse, an entire mission.

The Earth's space radiation environment can be divided in three major groups which will be further discussed below [Adams, 1981]:

- The particles originating from the Sun consisting of protons, electrons and heavy-ions;
- The Galactic Cosmic Rays (GCRs) consisting of protons and heavy-ions;
- The trapped particles in the Earth's magnetic field, also referred to as the radiation belts or Van Allen belts, consisting mainly of electrons and protons.

1.1.1 Solar particles

The Sun contributes in three different ways to the radiation environment of the solar system. The three main solar sources of particle ejection are: the solar wind, the solar flares and the CMEs (Coronal Mass Ejections).

The solar wind is a constant plasma flow of electrons, protons, and alpha particles coming from the Sun at speeds between 300 to 900 km/s, constituted of particles with low energies. Most of the solar wind particles are deviated or trapped by the Earth's magnetic field and are usually not of concern for components inside the spacecraft as they do not have enough energy to penetrate spacecraft shielding.

Solar flares are randomly occurring events. However, the mean solar activity is periodic and modulated by the solar cycle Sun's. They release mostly electrons [Petersen, 2011], but also energetic protons, alpha particles and other heavy-ions, along with electromagnetic radiation in all wavelengths.

CMEs are larger events in which electromagnetic radiation as well as mainly highly energetic protons, but also alpha particles and heavy-ions are released (at speeds varying between 50 to 2500 km/s); CMEs are richer in protons and poorer in heavy-ions with respect to solar flares [Reames, 1995]. High-energy solar particles can affect spacecraft in the interplanetary solar system, but also spacecraft protected by the Earth's magnetic field with high enough energetic particles able to pass through it, especially at high inclinations (above approx. 60°) and/or high altitudes, where the protection provided by the Earth's magnetic field is attenuated (geomagnetic rigidity cut-off value is smaller). Solar flares

and/or CMEs lead to the release of SEPs (Solar Energetic Particles) that span from proton to uranium and with energies up to 100 MeV/nucl.

Solar flares and CMEs can occur simultaneously with a total flux increased above three orders of magnitude compared to the GCR fluxes [Reed, 2008].

The dynamic interaction between the Sun and the Van Allen belts, modulated by the Sun's own 11-year activity (seven years of maximum activity and four years of minimum activity; 22-year cycle if the magnetic polarity of the Sun is considered) as well as the short storm bursts, has a direct impact on the number of errors, malfunctions or even destructions of electronic components. It is hence important to take into account where and when the mission will take place, as well as the duration of the mission.

1.1.2 Galactic Cosmic Rays (GCR)

The second source of radiation is due to GCRs originating most likely from supernovae and other violent events in the distant Universe although their origin is not fully understood [Bourdarie, 2008]. They make up an isotropic field of protons (85%), alpha particles (14%) and heavy-ions (1%) at very high energies (in the order of 10s of MeV/nucl. to 100s of GeV/nucl. and above). According to [Reed, 2011] GCRs are also constituted of electrons (3% electrons, 83% protons, 13% alpha particles, 1% heavier ions up to Uranium having a Z=92). The relative abundance of ions significantly drops after iron (Fe), this is the reason why, most of the time, only GCR protons and heavy-ions lighter than Fe are considered as depicted in Figure 2. In fact, the main direct ionization contribution in GCR are the following 5 ions: H, He, C, N, O and Fe [Reed, 2011] with Fe having at the same time a relatively high intensity (or flux), high energies (to penetrate deep inside a spacecraft) and high LET (Linear Energy Transfer). LET it is a physical value giving the energy transferred from the impinging particle to the target material inducing ionization; this aspect will be further discussed in chapter 2. Fe ion is contributing to a larger proportion (in the order of 50% in the LET region inducing SEE roughly between a LET of 1 to 30 MeV.cm²/mg) to SEE due to GCRs heavier than hydrogen (H) [Petersen, 2011]. The integral LET spectrum considerably drops above 30 MeV.cm²/mg (mainly contribution of Iron). Although it may be possible to consider negligible the effect of higher LET on SEE compared to the SEE due to LET below 30 MeV.cm²/mg (the GCR flux being much lower above 30 MeV.cm²/mg), it shall not be neglected when considering SEE devices allegedly radiation hardened in LEO particularly at low inclinations in order to ensure that those component are fully latch-up free [Petersen, 2011].

Some of the GCRs penetrate the Earth radiation belts and affect spacecraft in low earth orbit; this is especially true at the Earth's poles. Nevertheless, the flux of GCRs remains very low, in the order of 1 part./m²/s around 1 GeV/nucl. at solar minimum (worse case for GCR) [Weulersse, 2011]. In GEO or at higher altitude, outside the Van Allen belts, the heavy-ion flux may lead to daily upset for very sensitive devices with a flux of about 100 part./cm²/day [Petersen, 2011]. At 500 km, above 40° inclination, the LET spectrum of GCR becomes more intense at high LET (approximately above 20 MeV.cm²/mg) with a large increase between 40° and 50° [Petersen, 2011].

The highest values of GCR energies taken aside, the GCR energy spectrum on a given LEO orbit is modulated by the Sun's activity: the higher the Sun's activity, the lower the GCR intensity is for a given LEO orbit. This is due to the fact that as the Sun's activity increases, the solar wind intensity increases and better shields the low Earth environment from incoming GCRs [J. D'Aleo, 2011]. This fluctuation is also dependent on the Sun's magnetic polarity, which has an 11-year cycle.

Heavy-ions and GCR (and solar) protons that reach the Earth's atmosphere interact essentially with the oxygen and nitrogen atoms and generate a cascade of events creating the radiation environment experienced at different atmospheric altitudes and at ground level. Such secondary particles include: neutrons, protons, electrons and muons, pions, photons and gamma.

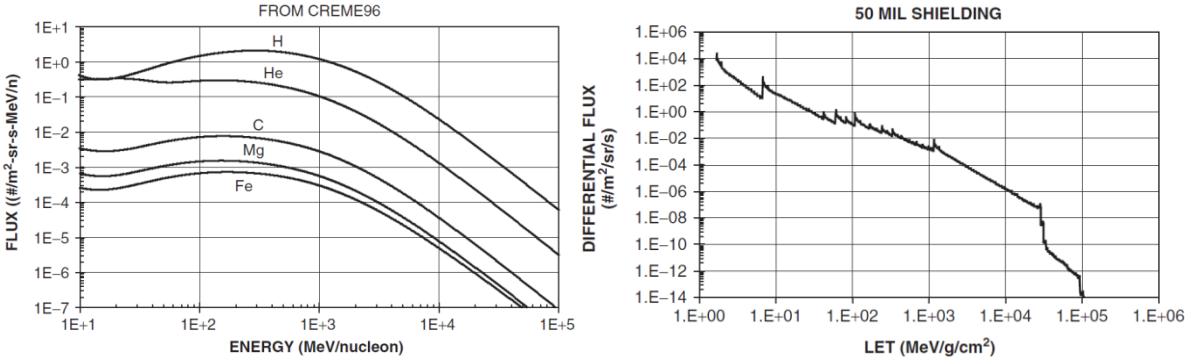


Figure 2: (left) GCR energy spectra of the five most abundant particles; (right) Differential flux LET spectrum of GCRs behind 50 mil of Al shielding (1.27 mm).

1.1.3 Earth Trapped ionizing particles

The last source of radiation only affects earth-orbiting spacecraft. Since the Earth generates its own magnetic field, particles, mainly originating from the Sun and GCR, were trapped and progressively enabled the formation of the radiation fields surrounding the Earth. These fields are commonly known as radiation belts due to their shape (or also known as the Van Allen belts as they were discovered by James Van Allen in 1958): the internal belt is mainly composed of protons and electrons whereas the external belt is mainly constituted of electrons. The particles in the radiation belts are considered to be isotropic. Alpha particles and heavy-ions are also present in these belts, but their proportion remains negligible as well as their energies (in the order of 10s of MeV/nuc), which are not sufficiently high to penetrate thin shielding [Reed, 2008] in the order of a few millimeters. These particles come from external sources (e.g. Sun, GCR) and are trapped by the Earth's magnetic field. Figure 3 depicts the extent of the radiation belts with respect to the Earth's radius as well as their fluxes: the left part shows the proton contribution and the right part, the electron contribution. In fact, not only the flux, but also the energy of the particles in the Van Allen radiation belts depends on the altitude and inclination: particles' energy can reach a few GeV [O'Brien, 2013].

The internal belt comprises of electrons (up to several MeV) and protons (up to 600 MeV). The highest proton flux is found around 3 000 km altitude regardless of the inclination [Petersen, 2011]. At this altitude, the proton flux with energies above 30 MeV reaches between $4x10^8$ protons/cm²/day near the poles (inclination of 90°) and $2x10^9$ protons/cm²/day near the equator (inclination of 0°). The proton belt extends up to about 3.8 Earth radii[2] (corresponding to an altitude of ~18 000 km). Besides, high electron fluxes can also be encountered in LEO especially near the polar cusps ("polar horns"). The inner electron belt extends to about 2.4 earth radii (altitude of ~9 000 km). The max electron flux in LEO above 1 MeV occurs around 1.5 Earth Radii (altitude of ~3 000 km altitude) similarly to trapped protons.

The external belt, on the other hand, comprises mainly of electrons of energies up to 7 MeV [Holmes, 1994]. The max flux occurs between 4 and 5 Earth radii (~19 000 to 25 500 km) with flux reaching up to $2x10^6$ electrons/cm²/s above 1 MeV. The outer electron belt extends mainly between 2.8 (~11 500 km) to 12 (~70 000 km) Earth radii [Holmes, 1994].

The region between the inner and outer belt is referred to as the "slot region". Besides, the belts are not static but rather dynamic as they are distorted by the solar wind, solar magnetic field especially the outer belt, affected by the Sun cycles and the Earth's rotation [Dyer, 2001] [NASA, 2014] as well as magnetic storms [O'Brien, 2013]. As relayed in [O'Brien, 2013], transient proton belts may also

[2] The Earth radius is around 6380 km.

appear due to SEP (Solar Energetic Particles) events but also geomagnetic storms [Lorentzen, 2002] leading to high SEE (Single Event Effect) rates in the slot region and affecting high sensitive systems (for example: electronic components, solar panels). During the period of solar maximum, the trapped proton fluxes in LEO decreases and the trapped electron fluxes increases. The opposite occurs at solar minimum [Petersen, 2011].

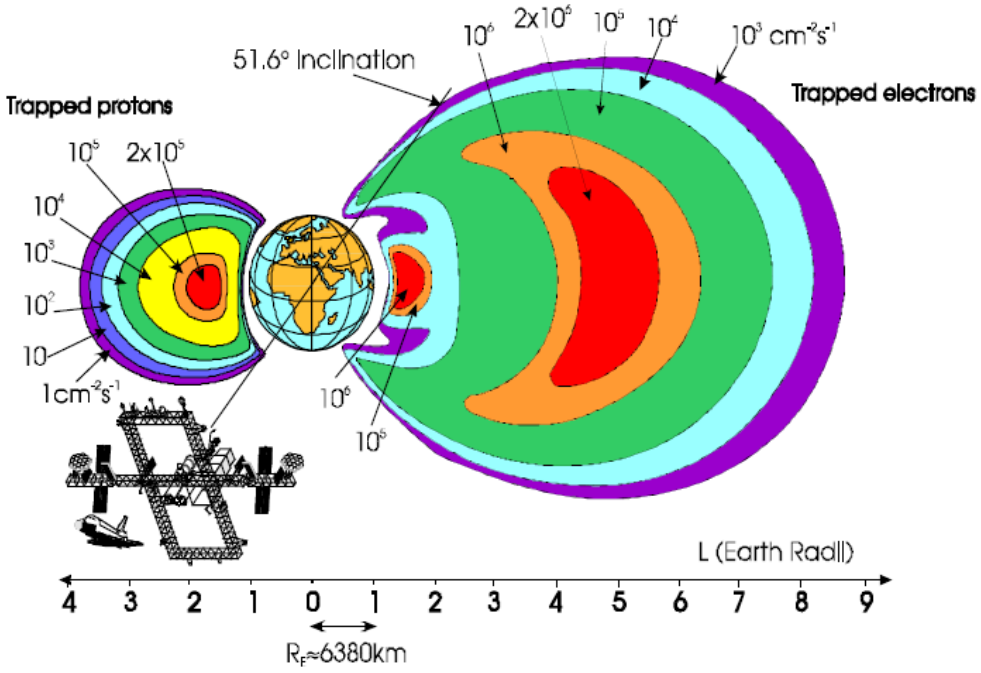


Figure 3: Location of the two Van Allen radiation belts. The internal belt mainly made of protons and electrons, external belt mainly made of electrons [Dyer, 2001]

One particularity of the inner proton radiation belt is the region called the South Atlantic Anomaly (SAA). This region, which spreads about the east-side of the South Atlantic subcontinent, presents a higher flux of energetic protons (for a given altitude) w.r.t. other regions at the same altitude. From about 1000 km [Petersen, 2011] down to approximately 200 km altitude, spacecraft may be exposed to the SAA and the radiation effects may be felt up to 2 000 km [O'Brien, 2013]. The SAA is due to the inclination of the Earth's magnetic axis with respect to its rotational axis (11 degrees) and the fact that the intersection of those two axes is several hundred kilometres north from the Earth's centre.

As mentioned in [Barth, 2003], the space radiation environment is still being investigated and models are constantly being improved to reflect new advances in the field.

1.2 Radiation effects in spacecraft

Several episodes show that radiation is a concern since the dawn of the space era. Critical errors occurred due to GCRs in the Pioneer (launched in 1972 and 1973) and Voyager (launched in 1977) probes [Petersen, 2011]. The Galileo mission targeting a mission to Jupiter and its moons, suffered from the extremely intense radiation environment of Jupiter. Over 20 anomalies were due to the severe radiation environment. Safe mode was activated due to current leakage in the power bus, cameras were deactivated after radiation damage in 2002 and the tape recorder was damaged due to proton induced displacement damage on GaAs LEDs that were partially fixed thanks to annealing sessions. Closer to Earth, the Hubble space telescope in LEO had his guidance system affected by the SAA, which required frequent scrubbing and reloading of the program [Petersen, 2011]. The Cassini

spacecraft orbiting Saturn experienced MBUs (Multiple Bit Upset, a type of effect due to a single particle strike, discussed more in-depth in section 1.2.2), Mars Odyssey's alarm was switched on due to a SEU (Single Event Upset, see section 1.2.2). But for all these missions, the effects were not lethal to the mission and workaround solutions were found. In the case of the Japanese "Superbird" mission [Petersen, 2011], faith had it such that the mission was lost due to the combination of an SEU and an operator error.

After having reviewed in section 1.1 the sources of space radiation, in this section will be briefly reviewed the main radiation effects affecting spacecraft electronics followed by how particles are affected by the shielding of a spacecraft in order to better understand the radiation environment inside the spacecraft where most of the electronic equipment is housed.

1.2.1 Types of radiation effects

The space radiation environment affects microelectronics in two different ways: via cumulative effects (Total Ionizing Dose, Displacement Damage) and Single Event Effects (SEEs). Effects of the particles mentioned in the previous section (protons, electrons and heavy-ions) on semi-conductors are summarised in Figure 4.

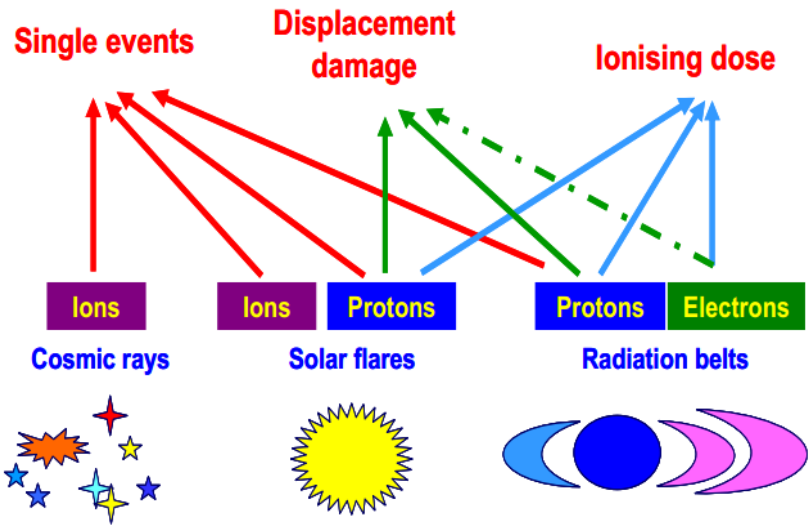


Figure 4: Comparison between radiation sources and effects [Ecoffet, 2013].

Electrons are responsible of surface charging (below 100 keV) and internal spacecraft charging (between 100 keV and 10 MeV) [O'Brien, 2013]. Spacecraft charging issues are out of the scope of the current work but standards and handbooks are available to understand and prevent those effects such as NASA-HDBK-4002A and NASA-HDBK-4006 and ECSS-E-ST-20-06C standards and handbooks. Besides, electrons are able to induce surface dose (0.5 to 100 keV) and ionizing dose (above 100 keV) as well as displacement damage dose (above few MeV) [O'Brien, 2013]. The latter two effects being the main concern of a radiation engineer whereas surface charging is the activity of the EMC/EMI (Electromagnetic Compatibility/Electromagnetic Interference) engineer.

Similarly to electrons, protons may be responsible of surface dose (0.5 to 100 keV), ionizing dose (above 100 keV) and displacement damage (above 10 MeV). Besides, protons may also induce Single Event Effects (above 10 MeV, though recent technologies appear to be sensitive to even lower proton energies in the order of hundreds of keV) and nuclear activation (above 20 MeV) [O'Brien, 2013]. In order to give an idea of the penetration depth of protons a table was extracted from the SRIM 2013 software tool [SRIM, 2013] and is shown in Table 1.

Energy (MeV)	Penetration depth in Silicon (µm)	Penetration depth in Aluminium (µm)
0.5	6	5
1	16	14
2	48	42
3	92	80
5	216	222
10	709	623
20	2 390	2 110
30	4 910	4 330
40	8 190	7 230
50	12 180	10 750
100	41 620	36 790
200	138 630	122 620
250	202 080	178 770

Table 1: Penetration depth of protons for various incident energies simulated with SRIM 2013 in Silicon and Aluminium. Protons with energies above 20-30 MeV are able to penetrate usual spacecraft shielding (few mm). Protons with energies above 5-10 MeV are able to penetrate component packaging.

Heavy-ion may generate single event effects (above 10 MeV/amu) usually, though very sensitive components may be sensitive to lower energies. Finally, secondary neutrons generated by primary protons or heavy-ions colliding with atoms of the external spacecraft walls and other material may also generate radiation effects such as displacement damage (above 10 MeV) or nuclear activation similarly to protons (above 50 MeV) [O'Brien, 2013].

1.2.2 Single event effects

Single events effects (SEEs) are a class of effects that are due to a single particle strike on a component with respect to cumulative effects, which considers the effects of several particles. Hence, SEEs occur almost instantaneously after a particle strike, whereas cumulative effects have the effect of degrading over time the components. Within the SEE group, there is a distinction between reversible (soft error) and non-reversible effects (hard error). Soft errors are able to be mitigated for example by a reset, an erase operation, or a power cycles.

The different types of SEE are summarized below:

1. **SET (Single Event Transient)** [soft] ➔ An ionizing particle will generate free carriers along its path. Those carriers may be collected at sensitive node in the circuits generating a current transient or voltage transient that may lead to unexpected effects in digital (especially combinatory logic) or analog circuits;
2. **SEU (Single Event Upset)** [soft] ➔ Single event upset is due to a transient event occurring at a specifically sensitive area of a logic cell inducing a change of the store information (bit flip);
3. **MCU/MBU (Multiple Cell Upset/Multiple Bit Upset)** [soft] ➔ MCU are bit flips (or SEUs) occurring in neighbouring cells due to a single particle. MBU are bit flips occurring in the same word often constituted of 8, 16 or more bits. MBUs are problematic: their multiplicity is important to consider the efficacy of EDAC to correct a word in error. EDAC can only detect and correct a limited number of bit flips per word;
4. **SEFI (Single Event Functional Interrupt)** [soft] ➔ A SEFI is due to a particle strike in the control logic of a device, which results is several tens or even hundreds/thousands apparent bit flip. In reality, in that case, the logic cells are not affected by ionized particles but the access,

the read or the write operations, for example, were not correctly performed due to the malfunctioning control logic and results in apparent fault read information;

5. **SEL (Single Event Latch-up)** [soft/hard] ➔ Latch-up occur in CMOS technologies when a particle strike triggers a parasitic PNPN or NPNP thyristor essentially generating a self maintained short-circuit and requiring a power cycle without which the component may burn due to thermal dissipation of large current;
6. **SEGR (Single Event Gate Rupture)** [hard] ➔ A SEGR is due a particle strike breaking the gate oxide of a MOS transistor;
7. **SEB (Single Event Burnout)** [hard] ➔ Finally, a SEB affects power MOSFETs and occurs when a strike induces the activation of a parasitic transistor which may results in the component burning due to high current and Joule effects.

Another type of effect due to a single particle but having similar effects as those due to dose are called microdose effects. Microdose effects are increasingly becoming important as the transistor size is reducing along with the level of parasitic charge able to generate malfunctions (dose or SEE related); one particle having enough energy to generate this parasitic charge.

For space systems SEEs have become increasingly important over the last fifteen years and are likely to become the major radiation effects problem of the future. For avionic applications, SEEs are the main radiation concern but total dose is relevant for aircrew (although the latter is in fact an accumulation of SEE in tissue). SEL is dependent on temperature, the occurrence of SEL can increase as temperature goes higher.

The current work is dedicated to the study of SEE effects on different memories. As seen in section 1.1, there are two types of particles able to generate SEE in the space radiation environment as summarised in Figure 5:

1. Heavy-ions are able to induce upsets via direct ionization: when passing through a material, the particle itself ionizes the material along its track;
2. Protons mainly generate SEE via indirect ionization: the particle itself is not able to ionize sufficiently the material but interacts through nuclear reactions generating heavy-ion recoils that are able to generate SEE. Nevertheless, very integrated technologies are also sensitive to direct ionization due to protons, which is exacerbated at low proton energies.

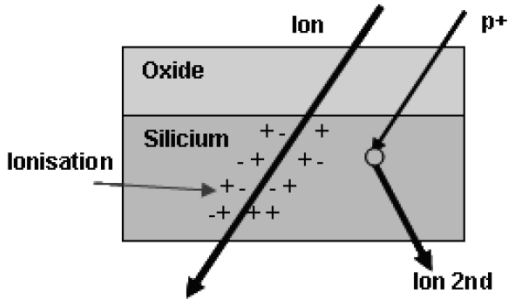


Figure 5: Simplified schematic showing the two mechanisms responsible for generating parasitic charge within a transistor that may lead to SEEs [Ecoffet, 2011].

1.2.3 Impact of shielding

Most of the time, the internal components inside a spacecraft are shielded at the minimum by the sidewalls of the spacecraft, which usually support solar panels, radiators, antennae, and so on. Hence, the radiation environment inside a spacecraft is expected to be different from the external radiation environment. One may consider that if thick enough shielding is used, it may reduce or cancel at least some of the ionizing particles. In reality, this is not necessarily true since it depends on the particle type, energy, shielding material and thickness. Moreover, it is not realistic to launch a spacecraft with a large mass dedicated to shielding, which increases the launch mass and hence the cost. It is therefore

necessary to understand how particles are affected by shielding and whether it is realistic, from a physical but also financial point of view, to use shielding and/or whether it is useful to find other means to prevent malfunctions or degradation due to the radiation environment.

As it will be explained in chapter 2, a charge particle (proton, heavy-ion, and electron) passing through a material will interact with it by transferring some of its initial energy to the material via two ionization processes: direct and indirect ionization. In the direct ionization process, the particle losses energy while generating electron/hole pairs (Coulomb interaction) while in the indirect ionization process, the particle may transfer the total or part of its energy to a target atom (inelastic or fission reaction). If the target atom (or recoil) has enough energy, it can itself generate direct/indirect ionization, leading to cascade of by-products through the material.

Figure 6 illustrates electron dose deposition (top) and proton energy deposition (bottom). Both particles have different energy deposition profiles: protons energy deposition is higher at the end of the particle range whereas the electron deposition is more spread out within the material. It is also possible to observe that low energy electrons (such as those present in the inner and outer radiation belts) and protons can be stopped by enough shielding material. On the other hand, higher energy protons (> 20-30 MeV) are able to penetrate usual shielding thicknesses similarly to the very high-energy heavy-ions from GCR or SEP events.

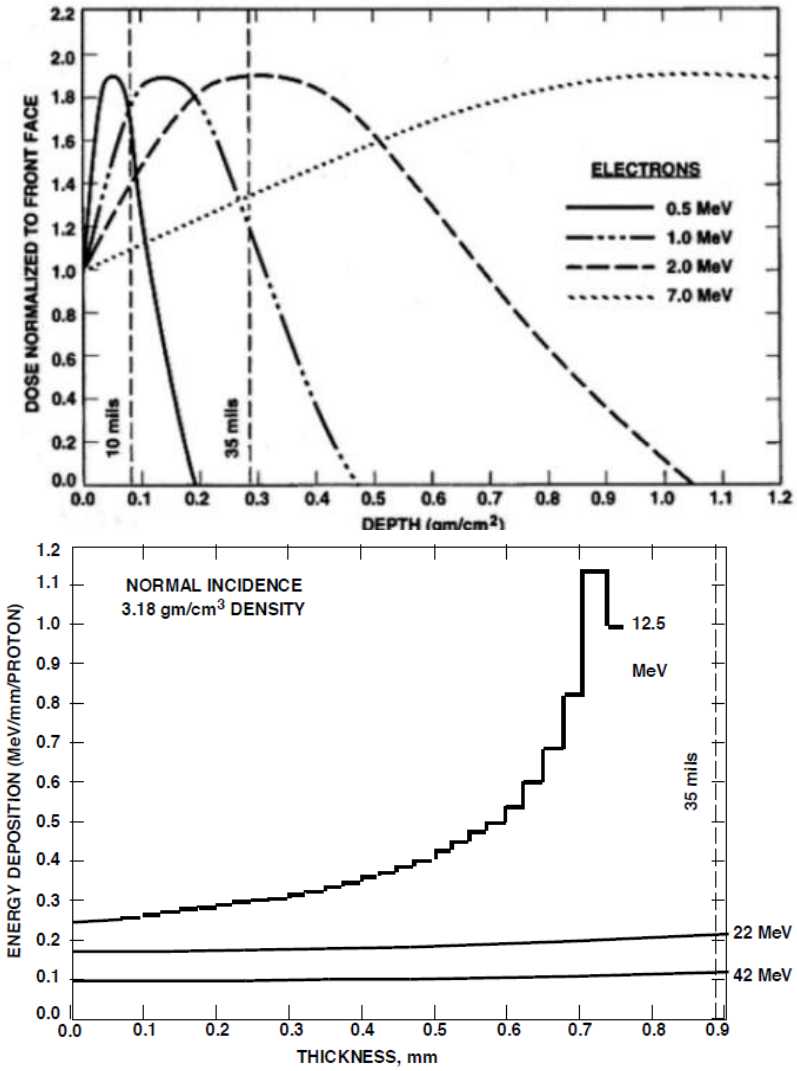


Figure 6: (top) Electron dose deposition and (bottom) proton energy deposition [Garrett, 2011].

Hence, shielding is an effective solution for reducing dose levels inside a spacecraft but highly energetic particles, those mainly responsible for SEEs, have their energies marginally reduced passing through the shielding material. For highly energetic heavy-ions such as those present in GCR, as the effect of shielding is very little, the internal heavy-ions spectra is traditionally given after 2.54 mm (100 mils) of aluminium shielding [Petersen, 2011]. The shielding enables to remove the low energy part of the heavy-ions flux, which, although constitute the highest LET particle population (Figure 7 top), has a small enough range not sufficient to penetrate usual spacecraft aluminium sidewalls. The increase of the shielding thickness does not sensibly impact the modified heavy-ion spectrum (Figure 7 bottom). At low inclination and low orbit altitude, the magnetic shielding naturally removes the low-energy-high-LET component of the spectrum.

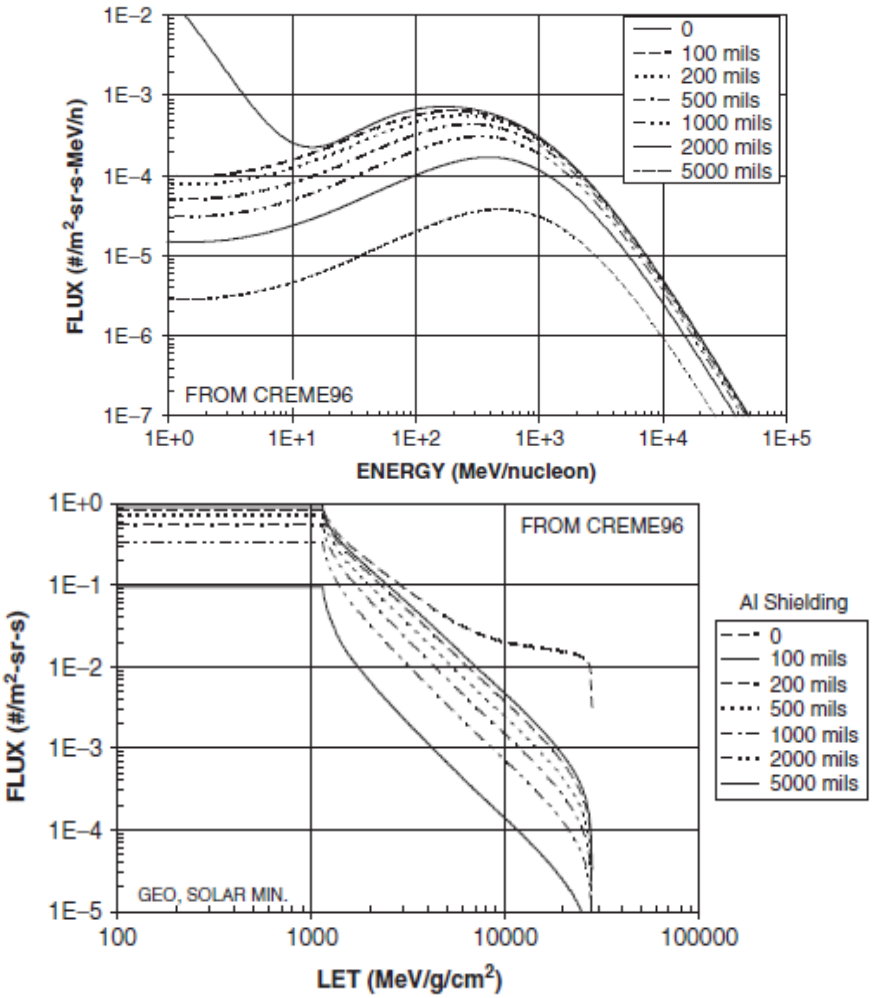


Figure 7: (top) Cosmic Iron Energy and (bottom) LET spectra behind different aluminium shielding thicknesses [Petersen, 2011].

Regarding protons, the shielding enables as well to reduce the proton low energy spectrum, nevertheless, the high-energy component remains unaffected by shielding regardless of the shielding thickness (Figure 8). Nevertheless, as some components have increased sensitivity to low energy proton's direct ionization, the remaining low energy spectrum able to penetrate shielding shall not be neglected for SEE rate considerations.

At solar minimum the peak flux of GCR is around 1 GeV/nucl. In [Reed, 2011] the author shows that, considering a commonly used shielding thickness of 0.254 cm (100 mils) of aluminium, the flux peak shifts around 100 MeV/nucl. for all heavy-ions as shown in Figure 9.

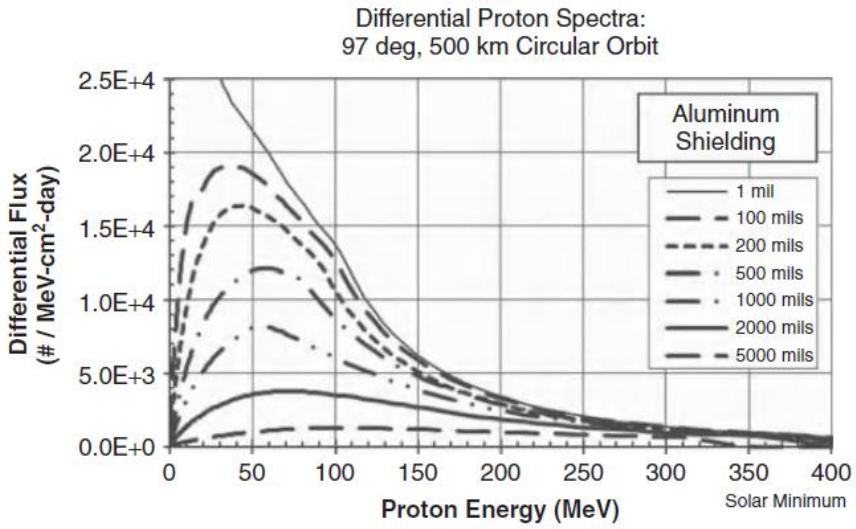


Figure 8: Effect of shielding thickness on the proton energy spectra [Petersen, 2011].

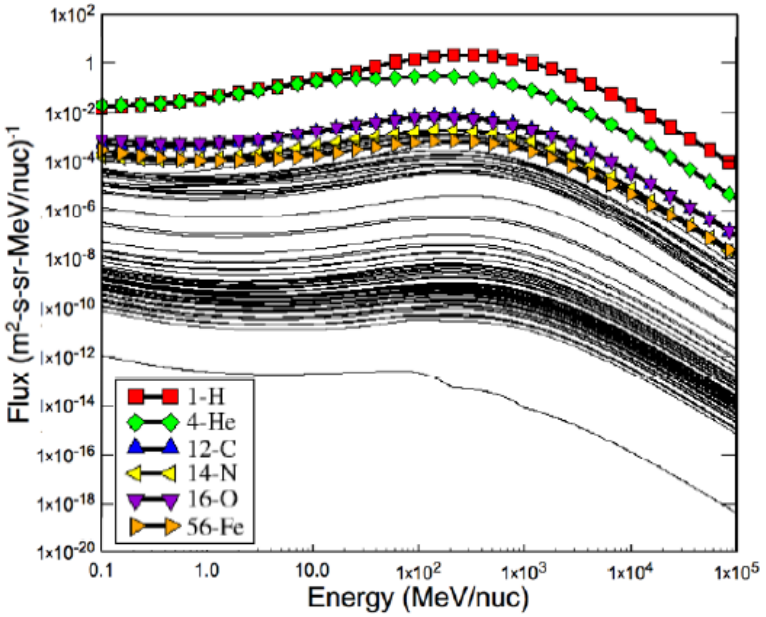


Figure 9: GCR energy spectra behind 100 mils (2.54 mm) [Reed, 2011].

The higher the material is constituted of high-Z atoms (Z being the atomic charge), the more the incident particle will interact and loose energy in the form of ionization (other important parameters are the incident particle energy, Z of the incident particle). However, the ionization energy (electronic stopping power or LET) increases for high-energy particles, when the energy of the incident particle reduces (this is not true for low energies, approximately below 1 MeV/nucl. for high Z heavy-ions and below 0.1 MeV for proton in silicon), as seen on Figure 10. This important fact shows that, in some cases, adding shielding may increase the ionization energy of a given particle inside a spacecraft, thus thus increasing the occurrence of SEEs.

Hence, not only shielding has to be taken into account when considering the probability of SEE of a component in a given orbit, but particular care must be taken to design the shielding in order to avoid worsening the SEE radiation environment inside a spacecraft. The shape of the shielding material is also an important aspect to be considered not only for SEE but also for dose consideration as illustrated in Figure 11, where is can be seen that the thickness combined with the natural scattering of the electron inside the target material can result in more or less backscattering.

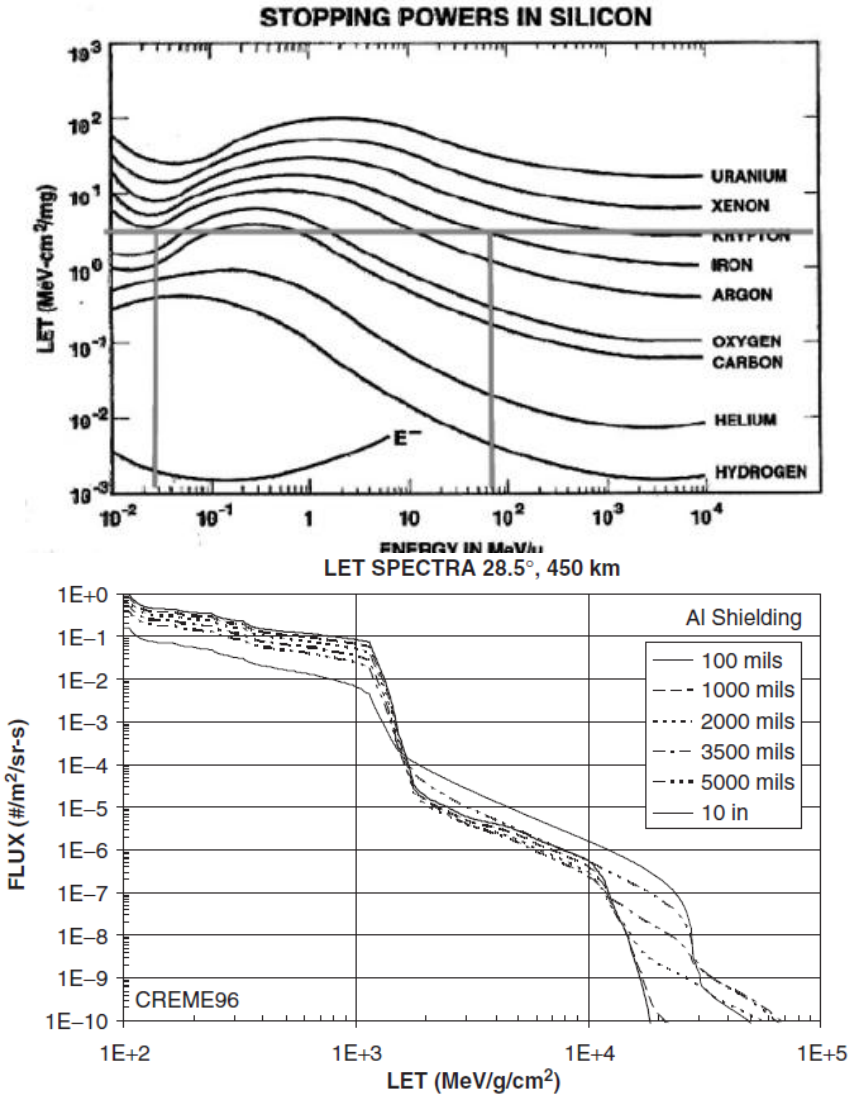


Figure 10: (top) LET vs. Energy for different particles in silicon [Adam, 1983]; (bottom) Illustration of the worsening effect of shielding in the LET spectra seen by component in a LEO orbit (450 km altitude, 28.5°) [Petersen, 2011].

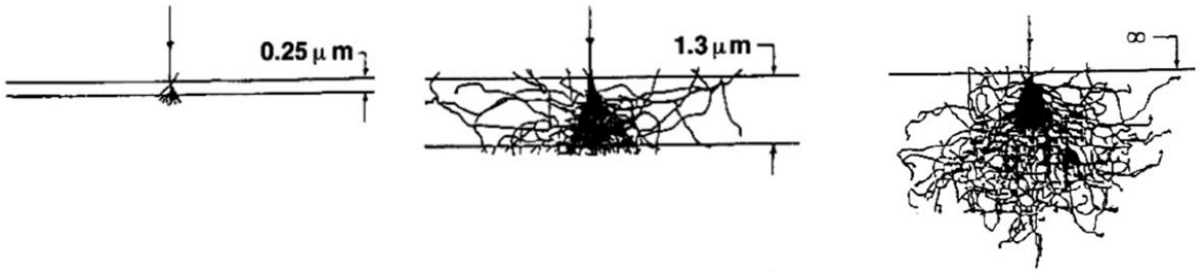


Figure 11: 20 keV incident electron scattering in aluminium of different thicknesses [Brown, 1990].

Design of shielding can be optimised in order to prevent as much as possible particles from penetrating inside spacecraft shielding, while keeping the mass as low as possible.

1.3 Electronic component reliability

1.3.1 Examples of radiation induced failures of spacecraft

In order to provide with concrete examples (besides those briefly mentioned in section 1.2) of effects at subsystem, or even satellite, level of the radiation impact on electronic components, in this section will be presented a few cases of radiation related events on famous space missions. The focus will be on SEE related errors but many more mission failures and causes (also due to TID and DD) are listed in [Ecoffet, 2011] and [NASA, 1996].

TDRS-1 (Tracking and Data Relay Satellite) is a US communication satellite launched in April 1983 to GEO. Since launch, SEU were detected on-board [Ecoffet, 2011], [Wilkinson, 1991], [Croley, 1995]. The AOCS (Attitude and Orbit Control System) is responsible for properly orienting the spacecraft as well as maintaining the satellite on its defined orbit. It is constituted of bipolar SRAM memories (93L422) that were in fact very sensitive to SEE and could lead to spacecraft tumbling unexpectedly. Analyses by [Wilkinson, 1991] and [Croley, 1995] showed that this memory was sensitive to proton in the lower belt during the transfer phase, then GCRs in GEO but also solar particles especially during solar flares.

In October 1997, the Cassini-Huygens spacecraft was launched as a NASA-ESA mission to study Saturn and its moons. The Huygens probe landed on the Titan moon and accomplished its mission objectives, whereas the Cassini spacecraft is still operational (at the time of writing). Soon after launch, errors were recorded in the two SSR (solid-state recorders) for science data storage when the satellite was still in LEO. This was due to high solar flares resulting in several MBUs due to a bad EDAC architecture [Swift, 2000], which exceeded the MBU error rate predictions. MBUs are critical errors that cannot be easily corrected using ECCs especially when errors in more than two bits in a word occur.

Closer to us, as briefly mentioned in the introduction, the Curiosity rover (Mars Science Laboratory) landed safely on Mars in August 2012. The rover is constituted of 2 Gb of Flash memory to be used with the main on-board computer. In February 2013, the operators detected some issues since continuous reboots occurred in the main computer and the rover was put in safe mode while the redundant computer was being activated. The reason was a corrupted file in the Flash memory that could be due to high-energy particles [MSL1, 2016][MSL2, 2016]. The opportunity rover also experienced several issues with its Flash memory since 2004. Figure 12 depicts the three above-mentioned satellite, probe and rover.

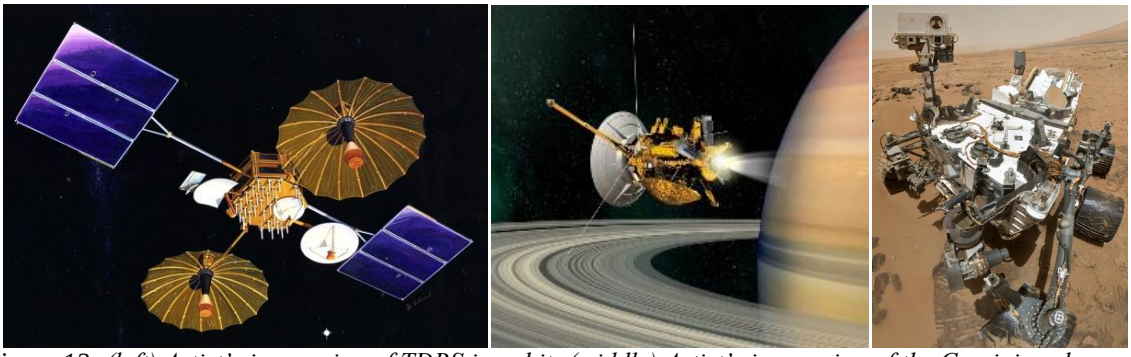


Figure 12: (left) Artist's impression of TDRS in-orbit; (middle) Artist's impression of the Cassini probe near Jupiter; (right) Auto portrait of the MSL rover on Mars.

1.3.2 Radiation testing of COTS components

The miniaturisation, improvement and development of Electrical, Electronic and Electro-mechanical (EEE) components as well as electronic circuits have been advantageous to the development of spacecraft and the increase in mission complexity. However, this miniaturisation has generally led to the increase of these components' vulnerability to the space radiation environment, which was presented in the previous sections and this is particularly true when considering SEEs.

Radiation-Hardened (RadHard) components are available, and are designed specially to cope with the space radiation environment. Electronic components used in space applications have been radiation-hardened by design, by using schemes such as guard rings or triple wells among others possible technics. Silicon-on-Insulator (SOI) technology is used instead of bulk CMOS in order to reduce latch-up events [Weste, 2010]. Nevertheless, their cost is rather high, especially for modest or low-cost space missions. Space companies but also space agencies are starting to use COTS (Commercial Off-The-Shelf) components, which represent an increasingly appealing alternative in satellite component selection, as they are readily available, usually lower in mass, with power consumptions lower than their RadHard counterparts and they are much cheaper. But as those components have not specifically been designed for space applications, it is necessary to ensure that their functionality is compatible with the satellite system and subsystem requirements, one way of achieving this is by means of testing.

Several ground-level testing means are available to evaluate the SEE susceptibility of components: laser testing, micro-beam testing, proton and heavy-ions beams testing with either mono-energetic or mixed field spectrum using particle accelerator facilities. Those test means are used for different purposes, but can also complement each other depending on the radiation environment under study. Laser and micro-beams allow the testing of a very small region of the component in order to investigate SEE at a relatively precise locations closer to the transistor-size level. This precision can result into the triggering of an SEE and thus the study of sensitive regions of the component and their overall contribution to the system's functionality. This may allow discovering specific sensitive regions in a chip in order to find suitable mitigation techniques.

Proton and heavy-ion testing allows the testing of the entire component or even an entire electronic system (possible in some proton beam facilities). In those facilities, ions (confined using magnetic field) are accelerated using electric fields allowing the particle to gain the required energy. Testing under proton and heavy-ion are the preferred choice of guaranteeing good functionality of a given device for space applications. Space standards of ESA or NASA may be followed, such as [ESCC25100, 2012] or [JEDEC57, 1996] for SEE testing under heavy-ion or proton irradiation. Characterisation of the functionality of an electronic component (e.g. memory devices) for each particle type and energy is made possible using mono-energetic beams. On the other hand, the radiation environment of a mission can be simulated using a mixed field spectrum in order to assess the global functionality of an electronic board, emulating the radiation environment closer to the one that will be experienced by the satellite. An example of such a facility is the CHARM facility at CERN [Mekki, 2015]. Nevertheless, it is important to remember that the space radiation environment cannot be fully reproduced for certain particles and energies, such as the very highly energetic heavy-ions or protons.

Thanks to previous testing experiments, it is possible to calculate the different SEE cross-sections, which provide an insight on the reliability of a component. The SEE cross-section of an electronic component quantifies the likelihood that a particle at a given energy will induce an SEE, and more specifically, whether it will be an SEU, MCU, SEL event and so on.

Usually, for proton testing, the cross-section is evaluated as a function of the energy (in MeV) of the proton, whereas for heavy-ions, it is evaluated as a function of the ionizing energy transmitted by the ion to the material per unit length and divided by the density of the material. This quantity is called LET (Linear Energy Transfer) and is given in $MeV.cm^2/mg$. Then, with environment simulator

software such as OMERE [OMERE, 2016] and SPENVIS [SPENVIS, 2016], which provide the average ionizing energy spectrum of the different particles encountered on a given orbit or trajectory, it is possible to calculate the expected error rate occurring during the mission. Based on those results, if necessary, mitigation technics may be implemented to reduce the error rate. Solutions may be hardware or software based. Several solutions may be implemented such as:

- Error Correction Codes (ECC);
- Software or Hardware redundancy (e.g. TMR);
- Using several smaller components instead of one main component;
- Periodical restarts of systems and sub-systems;
- Optimizing the placement of components, using the least sensitive components to shield the most sensitive ones for example;
- Combinations of the above solutions.

Nevertheless, SEE ground testing is not fully representative of the actual environment that will be experienced in space by the component. For example:

- Particle accelerators cannot reach the high energy levels found in space (always as a function of the environment the component is meant to operate in) [Ferlet-Cavrois, 2012];
- Synergetic effects (dose effects and SEE combined) may be not tested due to time and/or cost constraints;
- Often due to limited beam diameter only parts of the integrated components can be tested at once, and not the entire system;
- Most of the time, radiation testing is performed with the beam perpendicular to the surface of the component and only occasionally studies are made to study the angular dependency of the component's response to the radiation environment [Tipton, 2008], whereas space radiation is often omnidirectional;
- Due to time/cost constraints, radiation testing is performed at high fluxes that may not be representative of the space environment;
- Moreover, electrical degradation and temperature impact on the component after several years of mission in the space environment is difficult to apprehend.

Besides the limited representativeness of testing under particle beam, environmental models used to then estimate the error rate may not be fully accurate, several assumptions/simplifications are thus also considered as well in the calculation of the final error rate in orbit.

Hence, due to all these approximations, it is of high interest to confirm the ground-based predictions with actual in-orbit data. This is especially true for components that have not yet been sent to space, allowing raising their TRL (Technology Readiness Level) to acceptable levels for use in future missions. This also provides valuable feedbacks to compare with accelerated testing results as well as simulation results, in order to evaluate how representative these tests are of the actual mission radiation environment.

1.4 The MTCube mission

The objective of comparing SEE radiation testing with actual in-orbit data is at the heart of the MTCube project. The aim of the project is to fly a 1-Unit CubeSat, named MTCube, which will fly the RES (Radiation Effects Study) Experiment consisting in flying different types of commercial memories in order to assess their sensitivity against the LEO radiation environment. This data will be compared with ground-based accelerated testing (presented in chapters 3, 4 and 5) and SEE error rate estimations (presented in chapter 6). Not only such types of missions are useful to compare ground based and in-orbit data, but, as mentioned above, it is also ideal for testing components produced with new/emerging technologies and that have little or no flight experience. For this reason, several types of memories with different technologies, architectures and flight heritage will be part of the MTCube payload. These memories will be presented in section 1.4.3.

1.4.1 MTCube partners

In Figure 13 the logos of the main actors of the MTCube project are depicted. MTCube stands for Memory Test CubeSat. In this section, the partners of the MTCube project will be briefly presented.

The "Centre Spatial Universitaire" (CSU) was created by the RADIAC research group, one of the world leading groups in the field of radiation effects on electronics and part of the IES research entity formed by the collaboration between the University of Montpellier and CNRS (Centre National de la Recherche Scientifique). For more than 25 years, RADIAC has been providing support to industries and agencies in the field of radiation effects by investigating basic mechanisms and providing them with accelerated testing methodologies. The CSU was born thanks to the collaboration between the RADIAC group and the IUT of Nîmes. The CSU is developping the Robusta platforms (1U and 3U), which follow the CubeSat standard [CDS, rev13].

The Van Allen Foundation, aims at supporting nanosatellite activities in France, with corporate sponsorship of prestigious partners such as the University of Montpellier, Astrium, Intespace, 3D Plus, ESA and CNES. Both ESA and the Van Allen Foundation (FVA) are currently financing the MTCube project.

MTCube will fly different types of memories that may be used for future space applications. The selected memories will constitute the RES (Radiation Effect Study by SEE) experiment payload of MTCube, which will be built under an ESA collaboration contract.

The payload has been conceived and designed within the TDH (Test and Design of electronics for space and Harsh environments) group of LIRMM, Laboratoire d'Informatique, de Robotique et de Microélectronique de Montpellier, which is a joint research laboratory between the University of Montpellier and CNRS.

The RADEF radiation facility of the University of Jyväskylä offers the use of their heavy-ion and proton beams. Most of the radiation test campaigns performed on the payload memories were conducted there.

Figure 13: The main actors of the MTCube project along with the logo of the project.

1.4.2 MTCube mission objectives

The primary objective of MTCube is hence to develop, test and fly the RES Experiment and gather data for 2 years (nominal mission duration). During the development phase, a set of COTS memories was selected for the experiment. The RES Experiment will use the Robusta 1U CubeSat platform [Deneau, 2010], [Perez, 2010] with several upgrades included for this mission. A CAD overview of the 1U CubeSat is shown in Figure 14.

The main objectives of the MTCube mission are:

- ⇨ to assess the in-orbit radiation sensitivity (SEE) of various state-of-the-art memory devices (SEU and SEL);
- ⇨ to geolocalise the SEE occurrence in these memories along the orbit;
- ⇨ to compare ground-based Radiation Hardness Assurance (RHA) processes with in-flight radiation data;
- ⇨ to develop and provide a technology test bed for novel memory devices;
- ⇨ to measure the on-orbit radiation dose by the use of an in-house built OSL-based dosimeter.

The MTCube platform and payload are developed, built and tested by the CSU and LIRMM as a student project implying a strong education aspect. Students from all level and several disciplines are involved and trained under the supervision of a team of researchers and professors.

1.4.3 Description of the RES Experiment

Memories are used for different tasks depending on their performances and features. Generally, memories are used as storage devices for software boot, memory cache for microprocessors but also storage devices for telemetry/telecommand and scientific data. In this section, we will briefly review the types of memories that will be part of the MTCube payload and briefly explore the main SEE sources for each type of memory.

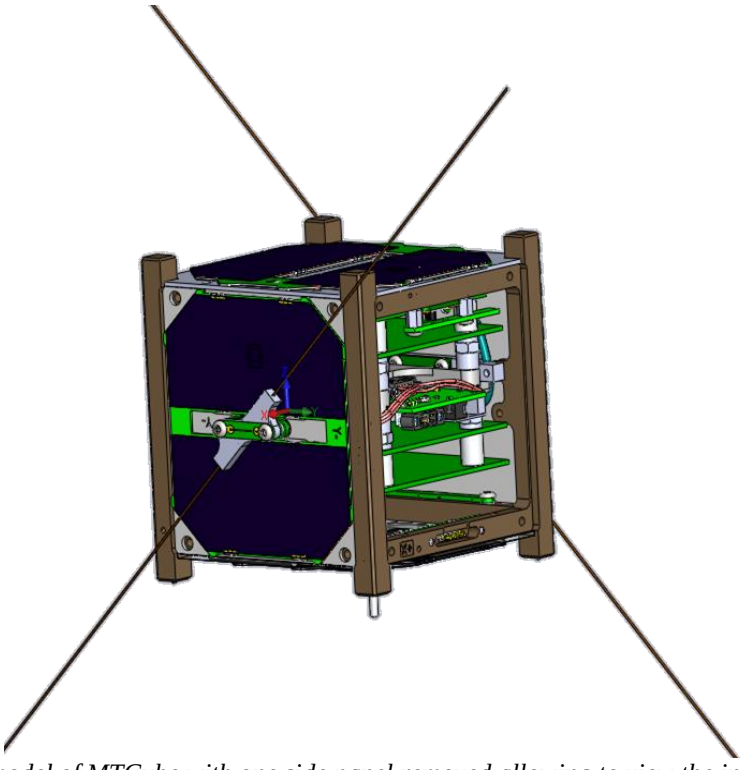


Figure 14: CAD model of MTCube with one side panel removed allowing to view the internal configuration.

SRAM (Static Random Access Memory) is a type of memory that has high performance in terms of access time. Besides, it is a volatile memory: the data is lost if the power supply voltage drops below a certain level. The most common SRAM memory cell design is based on 6 transistors (6T). The bit, either '0' or '1', is stored thanks to 4 MOS transistors connected in order to form two cross-coupled inverters; the other two transistors are used to access the memory cell during read/write operations [Baumann, 2005]. The miniaturisation trend makes it necessary to test the sensitivity to radiation of new technology nodes, as new types of effects may appear. For example, direct proton ionization due to low energy protons is a new source of error, due to the increased sensitivity and high-density of memory cells [Lawrence, 2009]. The number of cells affected during the occurrence of MCUs (Multiple Cell Upsets) also considerably increases [Cannon, 2008] with miniaturisation. The SEE test results of the selected SRAM memory are presented in chapter 3.

The MRAM and FRAM provided by the partner company 3D Plus have also been chosen to observe the effects of the space radiation environment on these different commercial non-volatile memories. MRAM cells are based on two ferromagnetic layers sandwiching a thin insulating barrier with one reference layer and another free layer which can see its magnetic orientation changed based on magnetic field created by large amounts of current [Senni, 2015]; controlling the magnetic orientation induces a change in the overall electrical resistance of the sandwiched layers (also called MJT – Magnetic Tunnel Junction). FRAM memories use ferroelectric materials, which allow changing their state thanks to electrical field inducing a change in the apparent stored charge. The particularity of those two types of non-volatile memories is that they are stacked memories, each component consisting of 4 layers of memory dies. MRAM or FRAMs memories appear to be interesting candidates for future space missions, since they present high radiation resilience and low access times when compared to other non-volatile memories. Their cells' data storage mechanisms provide inherent radiation robustness according to literature such as in [Nuns, 2008], while most of the potential errors may arise from the CMOS-based peripheral circuitry. As those memories are rather new on the commercial market, characterising their behaviour is essential to assess their suitability for future space missions. In the current study, amongst those two memories, solely the test results from the FRAM memory will be presented in chapter 4.

Finally, two Flash memories, selected by ESA, will be part of the memories to be tested. Flash memory cells are made by a transistor that presents an additional floating gate sandwiched between two oxides on top of which is placed the actual transistor's gate: charges may be stored in the floating gate allowing changing the characteristics of the transistors (shift of the threshold voltage). Flash memory cells are less sensitive to the radiation environment than SRAM memory cells, but they may still be affected, not only at cell level but also in their control circuitry. Faulty control logic may produce large clusters of errors, for example during the occurrence of SEFI (Single Event Functional Interrupt). [Bagatin, 2008] provides a comprehensive list of potential effects of heavy-ion radiation on Flash memories. Flash memory test results will be presented in chapter 5.

All candidate memories are listed in Table 2.

Type of memory	Nb	Manufacturer	Reference
32 GB NAND Flash	2	Micron	MT29F32G08ABAAA
90nm SRAM	1	Cypress	CY62177EV30
65nm SRAM	1	Cypress	CY62167GE
FRAM 3D (3 layers)	1	3D plus	3DMR64M08VS4476
MRAM 3D (4 layers)	1	3D plus	3DFR16M16VS4315

Table 2: Selected memories for the RES Experiment. One of the FRAM layers will be used as the experiment temporary data storage memory unit.

In addition to the considered memories, a radiation dose monitoring system based on an OSL (Optically Stimulated Luminescence) dosimeter developed by the RADIAC group will be hosted in the satellite as additional payload. This OSL-NG is based on a previous OSL technology that flew on the ICARE instrument of the CARMEN-2 payload on board the JASON-2 CNES satellite [Deneau,

2012]. The OSL will be located on the OBDH electronic board as spare space is available on this board.

The RES Experiment board has been designed to work fully autonomously during the nominal mission. The memory testing experiments will be run using Finite-State Machines (FSM) implemented on a Microsemi IGLOO NANO FPGA, which will also be responsible for the communication with the other satellite subsystems through a CAN bus. Sequences of dynamic and static tests will be performed on the studied memories, in order to compare their SEE sensitivity in various test modes and conditions.

To prevent permanent damages due to particle triggered over-currents, anti-latchup circuits will be placed on the power supply rails, moreover logic hardening methods will be implemented on the FPGA and data buffer. The data buffer will be hardened by using error detection and correction routines. This buffer will store information about the error events detected on the memories. This information is regularly transmitted to the main on-board computer subsystem that will take care of its transmission to ground. The buffer needs to be hosted in a non-volatile memory, since it has to retain the data in the unlikely event of a payload power shutdown or for the regular resets of the payload system performed to prevent possible fault accumulations.

The following information will be gathered on orbit: data of the corrupted words, along with their addresses, the timestamp and all additional information necessary to know in which conditions exactly the events occurred. There will also be a record of the occurring latch-ups, specifying the devices to which it occurred as well as the timestamp of the event.

Figure 15 presents a picture of a prototype of the RES Experiment that will be used for high-energy radiation testing. The FPGA is directly connected to each memory via a shared bus, while the Flash memories will have their own separate bus connected to the FPGA. In Figure 15, the MRAM and FRAM memories show a gold colored package, and their stacked configuration can be easily spotted (bulky shape). The remaining memories (the second Flash and SRAM memories) and other components are located on the bottom part of the board.

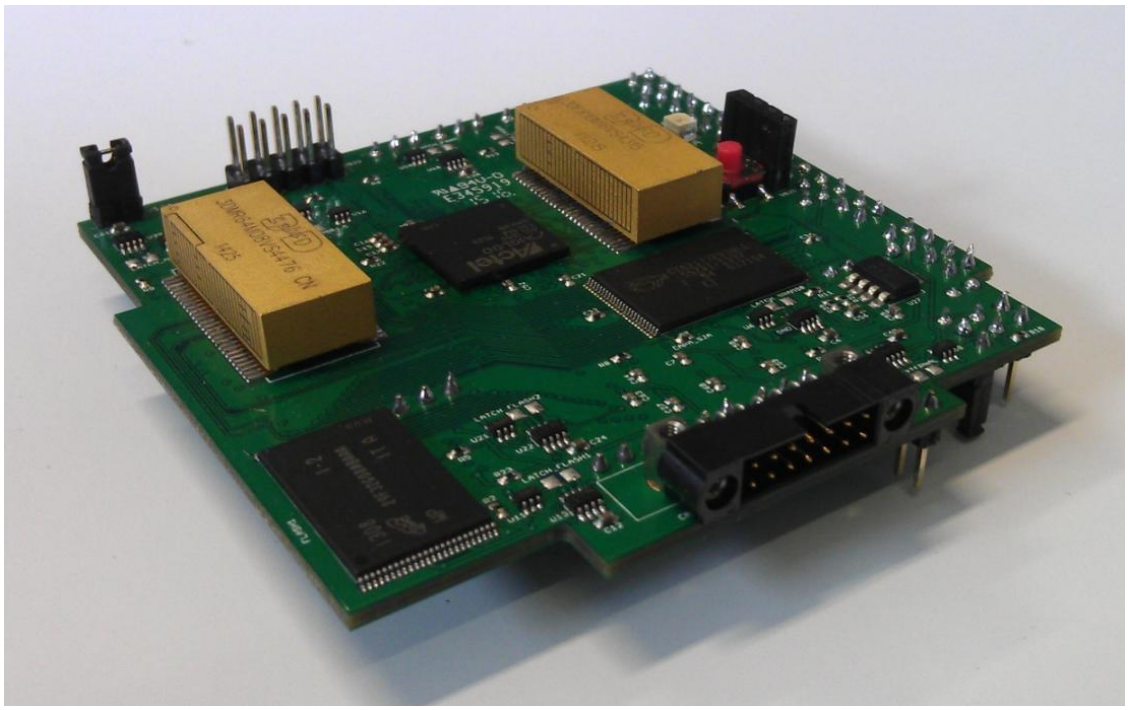


Figure 15: Picture of the second RES Experiment prototype to be used for high-energy proton radiation testing.

1.4.4 Mission feasibility

1.4.1.1 Introduction

After introducing the objectives of the MTCube mission and after presenting how the science experiment will be conducted, it is crucial to understand whether the mission is feasible or not. First, a study orbit shall be selected in order to perform the preliminary calculations as the final orbit will be fixed at a later stage. Then, the overall mission profile will be briefly described as well as the foreseen spacecraft system modes and ground coverage based on the selected orbit. The main parameters concerning the consumption/mass/data of each subsystem is estimated and motivated. All these assumptions will provide inputs in order to assess the feasibility with respect to the most critical mission budgets, which are the total mass, power and communication link budgets.

MTCube will comply with the requirements of a 1U (Unit) CubeSat [CDS, rev13]. The platform, built by CSU, is an improved version of the previous experience including Robusta 1A and Robusta 1B. These two 1-Unit CubeSats were built with the objective of studying the ELDRS effect on bipolar devices in order to compare with a methodology developed by J. Boch [Boch, 2011]: Robusta 1A, launch in February 2012 suffered from malfunctions; Robusta 1B is expected to be launched in the very near future (at the time of writing). Several improvements were implemented on MTCube during the design phase and are still being made at the time of writing.

1.4.1.2 MTCube initial feasibility study

Part of the initial work carried for this study first involved performing an initial assessment of the feasibility of such a mission. Based on initial assumptions and previous mission data, a mission feasibility was performed. In an attempt to avoid overloading this section, more oriented towards radiation studies, this feasibility of the mission is presented in Annex A.

1.4.5 Radiation environment study

In order to estimate the SEE error rate of the payload memories, besides the required experimental data that will be presented in section 3, it is necessary to know the radiation environment that will be experienced by the satellite. As the launch parameters remain uncertain at this stage of the project, an assumption was made to estimate the most probable radiation environment. Most common used LEOs are in the range of 500 to 700 km in Sun Synchronous Orbits (SSO). Hence it was assumed that the orbit will likely be around 600 km circular orbit in SSO. This altitude clearly is compatible with French and ESA space regulations for end-of-mission lifetime. Of course, in the case of radiation experiments, elliptical orbits may also be of great interest, but launch companies less commonly offer these.

1.4.2.1 Radiation environment model

As the launch of MTCube is expected in beginning 2018 (at the time of the study), the solar cycle 24 will be nearing its end. The solar activity will hence be at the minimum of its 11-year cycle: it is hence expected that the GCR intensity will be higher, SEP will be reduced and high energy protons intensity will increase, as mentioned in sections 1.1.2 and 1.1.3.

As a first approximation for preliminary studies, we assumed the shielding being equivalent to 2 mm of aluminium (satellite wall) around the memory, which is a conservative assumption for dose and SEE measurements of components inside a CubeSat when considering the satellite wall as well as the internal structure that particles may have to cross before reaching the memories on the RES

experiment board. Lower values are very unlikely based on Robusta 1A considerations (when not considering the purposely made thinned regions of the satellite walls manufactured to increase the dose level on the bipolar devices). The estimated dose level (presented in Figure 16 and Table 3), using the OMERE software tool [OMERE, 2016], for the 2-year mission is about 8.4 krad(Al) behind 2 mm of aluminium wall. In Table 3, values are reported for slightly thinner and larger wall thicknesses as well in order to understand the effect on dose as the wall thickness may vary during the design phase. At this altitude, the dose is mainly due to electrons near the polar cusps and mainly due to protons when the satellite will pass through the SAA. Those levels of ionizing dose are very low and most (but not all) commercial electronic components are able to cope with at least a few tens of krad(Si). Hence, the main issue remains SEEs as expected for LEOs and this is the reason why it is the main goal of the MTCube project.

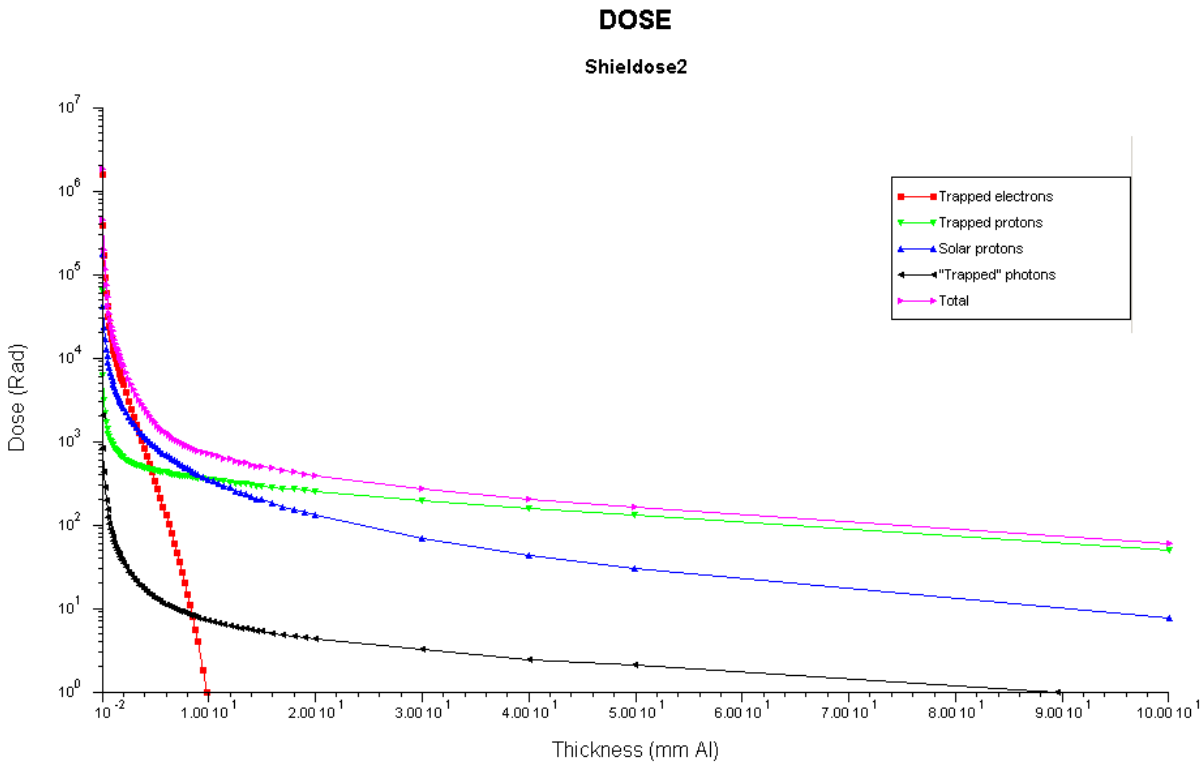


Figure 16: Total ionizing dose evolution with thickness in aluminium using OMERE for the studied orbit.

Shielding thickness	Dose (krad(Al))
1.5 mm (Al)	12.67
2.0 mm (Al)	8.41
2.5 mm (Al)	5.9
3.0 mm (Al)	4.3

Table 3: Total ionizing dose calculation in aluminium using OMERE for various wall thicknesses for the 2 year LEO mission.

With regards to SEE (Figure 17), in LEO, trapped protons (in the Van Allen belts) are expected to be the main source of SEEs especially near the South Atlantic Anomaly (SAA) where energies can go up to >100-150 MeV. Solar protons and heavy-ions may increase the error rate when the satellite is exposed to the Sun. Finally, most of the heavy-ion errors will likely occur near the Earth magnetic poles where the satellite is not protected by the Earth's magnetic field.

In order to ensure that the payload is able to withstand a LEO polar orbit radiation environment, as well as to be able to characterise the sensitivity of the payload memory, the following radiation testing approach is followed:

- single memories heavy-ion irradiation;
- single memories proton irradiation;
- testing of a Qualification Model (QM) with high-energy protons.

The first two irradiations will enable to estimate the sensitivity of each memory to various test stimuli as well as to quantify the expected number of upsets in orbit. The latter test will be performed on the entire QM in order to assess at a subsystem level the good functionality of the experiment board.

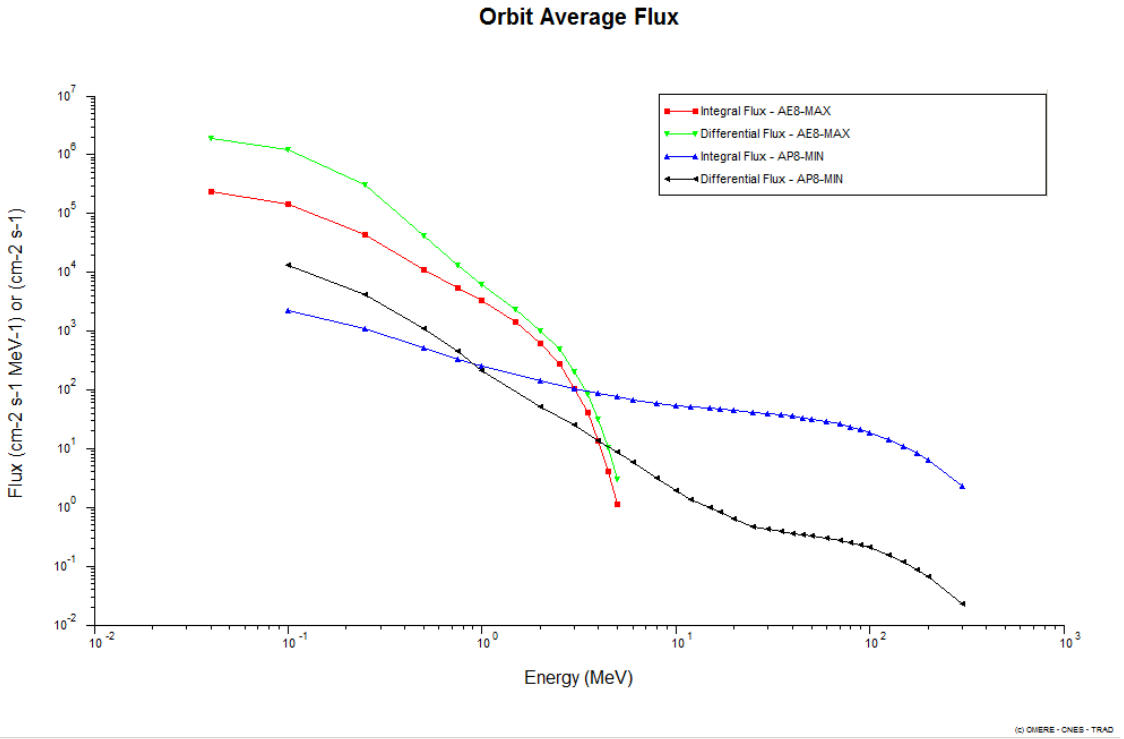


Figure 17: Example of a radiation environment spectrum for the MTCube orbit study case, showing the electron and proton flux energy spectrum behind 2 mm of Al shielding. The proton energy spectrum spreads beyond 200 MeV (but at a much lower average flux). The protons at such energies are mainly present in the SAA in LEO.

1.4.2.2 Radiation Model of the MTCube payload

In this section, the focus is made on the RES Experiment card and explanations are given on how the RES radiation model was built.

The RES Experiment board will comprise of seven memories and an FPGA. Other components such as DC/DC converters, CAN controller, clock oscillator, card connector were modelled as simple boxes in order to take into account the small masking effect they provide for the dose calculations on the memories (in order to have a good confident estimation although the effect is expected to be very small). Other smaller components were neglected for their negligible effects in the dose calculation. Figure 18 presents the model built for the calculations. The placement of the components was made in the position chosen when designing the RES EM. The placement is approximate but sufficient enough for dose calculations. Table 4 summarises the main components on the board as well as their constituting material.

The memories and FPGA were modelled using a carbon epoxy box and internal die in silicon with vacuum in between. The DC converter, oscillator and CAN transceiver were modelled only using carbon epoxy. Both 3D Plus memories (FRAM and MRAM) were modelled by using 4 stacked

MRAM and FRAM components as presented in Figure 19. Each of the internal stacked memories are modelled as for the above memories. To those stacked memories were assumed to be surrounded by carbon epoxy finished with 3 µm thick nickel and then 1 µm thick gold layer as specified in the 3D Plus datasheets. A radiation sensor was placed inside the die of each memories and FPGA. For the 3D Plus memories a radiation sensor was placed inside each stack die in order to assess the possible difference in dose expected depending on the position of the stacked memories.

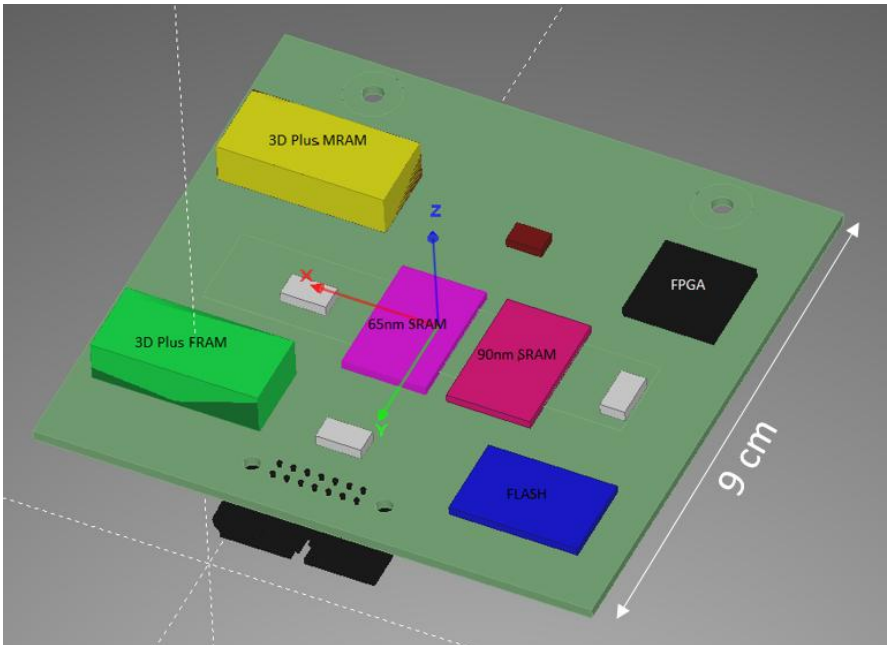


Figure 18: Overview of the RES Experiment FASTRAD Model.

A FASTRAD model of the MTCube platform was built [Rousselet, 2016] in order to assess more precisely the dose levels received at components level. As the platform of MTCube is still being built with some minor improvements from the recurrent Robusta 1A, platform a detailed analysis at platform level is not possible (besides the uncertainty about the orbit) but a confident rough value can be calculated on the dose level of critical components. Figure 20 shows the FASTRAD model. For the purpose of the radiation analysis, it is not necessary to model the external antennae.

Component	Size (mm^3)	Material
90nm SRAM	18.4 x 12 x 1.2	TSOP: carbon epoxy + vacuum Die : Silicon
65nm SRAM	18.4 x 12 x 1.2	TSOP: carbon epoxy + vacuum Die : Silicon
MRAM 3D plus	24 x 10.95 x 6.2	Casing: Gold, Nickel, Carbon epoxy + vacuum
MRAM	18.54 x 10.29 x 1	TSOP: carbon epoxy + vacuum Die : Silicon
FRAM 3D plus	24 x 10.95 x 6.2	Casing: Gold, Nickel, Carbon epoxy + vacuum
FRAM	18.54 x 10.29 x 1	TSOP: carbon epoxy + vacuum Die : Silicon
FLASH	18.4 x 12 x 1.2	TSOP: carbon epoxy + vacuum Die : Silicon
FPGA	13 x 13 x 1.75	Case: carbon epoxy + vacuum Die : Silicon
Oscillator	5 x 3.2 x 1.3	Aluminium
DC converter	6.5 x 3.56 x 1.6	Carbon Epoxy (full box)
CAN transceiver	5 x 4 x 1.75	Carbon Epoxy (full box)
Connector	24 x 8.6 x 8.5	Carbon Epoxy
PCB card	80 x 76 x 1.7	Glass Epoxy

Table 4: Components selected for the FASTRAD Model of the RES Experiment.

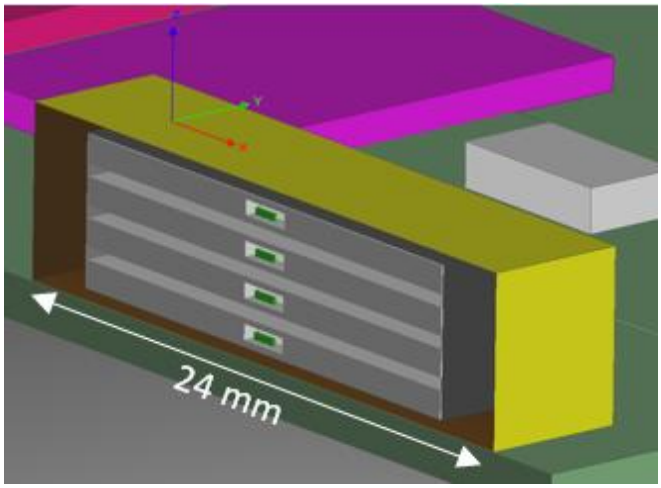


Figure 19: Zoom on the MRAM 3D Plus memory (virtually cut to see the internal structure). Four MRAM are stacked each one having its own silicon die (in green). The size of the die was kept at the default value in FASTRAD.

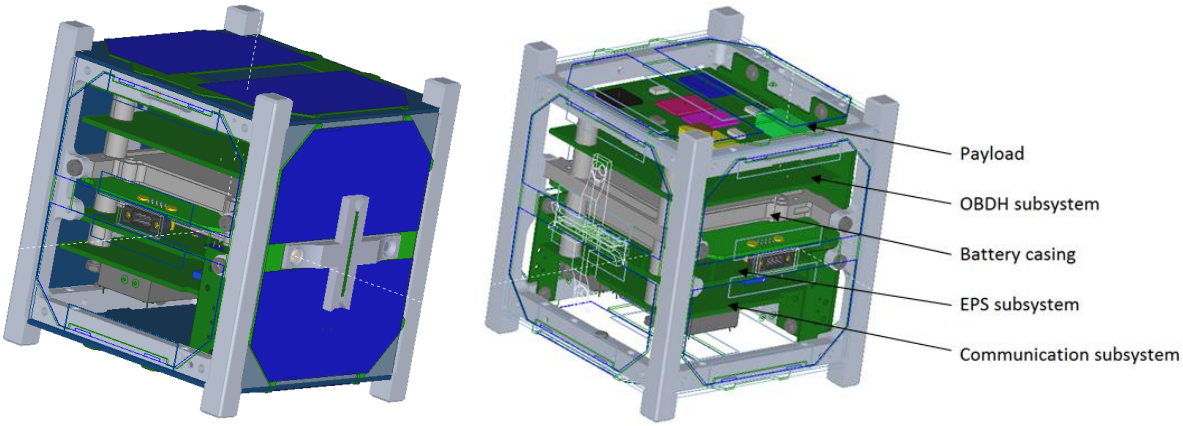


Figure 20: Preliminary FASTRAD model of MTCube. (left) One of the side panels was hidden in order to see the internal configuration of the satellite. (right) Internal configuration and subsystem card location inside MTCube.

1.4.2.3 Results

The model assumptions considered in FASTRAD for the dose calculation were the following:

- Slant Path method (true thickness crossed);
- Overlapping ignored;
- Step in azimuth and elevation angle of 100 for each;
- Radiation environment generated by OMERE using the following orbital parameters:
    - 650 km altitude circular orbit;
    - 98° inclination;
    - 360 LAN, E = 0°
    - Launch in Sept. 2016 for a 2 year mission duration (expected launch date when the radiation model study was performed)
    - Radiation environment model: AE8MAX/AP8MAX, ESP (solar proton), confidence level of 95%.

The orbital parameters are compatible with the orbit assumptions considered for the mission analysis of MTCube.

Components	Total dose [krad(Si)]
90nm SRAM	2.7
65nm SRAM	2.7
FRAM (top)	1.5
FRAM (middle top)	1.2
FRAM (mid. bottom)	1.1
FRAM (bottom)	1.0
MRAM (top)	1.5
FLASH	1.7
FPGA	2.0

Table 5: FASTRAD simulation results on the RES Experiment memory board.

It is first interesting to note in Table 5 that the dose does not exceed 2.7 krad(Si) for the 2 year mission duration giving roughly a dose of 1.4 krad(Si) per year maximum considering the RES Experiment components. This result is close to the more approximate calculations performed assuming a 3.5 mm aluminium shielding sphere. The dose level reached at the end of the nominal mission is not expected to be detrimental to the good behaviour of any of the payload components.

Another point worth mentioning is the higher dose level of both SRAMS. This can be well explained considering the position of the memories, facing the external side panels of the main structure and located right below the lowest thickness area of this panel. Indeed, the middle of the panel is not protected by a layer of solar nor PCB panel.

Finally, assuming the proper modeling of the 3D Plus memories, it can be noted that the lowest the memory is stacked the less dose it receives as the top layers act as additional barriers and the thinning of the bottom part does not compensate for that. The relative difference of dose level between the top and the bottom was estimated to be around 30 %.

1.5 Conclusion

In this chapter, first the space radiation environment has been introduced focusing on the three near-earth radiation sources: the Sun, the GCR and the Van Allen belts. The different effects induced by radiation have been introduced with a focus on SEEs, which will be the subject of the current study. The impact and importance of considering the spacecraft shielding for internal components has also been discussed.

The importance of reliability in space systems w.r.t SEEs has been highlighted through several examples of known space mission which have suffered from SEEs. The use of COTS and test methods used to qualify components for SEE has been introduced as well as their limitations and the necessity to have the possibility to get in-orbit results.

In this context, the MTCube project, which is the main application of the current study, has been introduced. The science experiment (the RES experiment) and the selected memories were described. The SEE test results of these memories will be presented in chapter 3, 4 and 5. The in-house-made PCB prototype was also presented.

Then, in order to ensure the feasibility of the mission, a mission analysis was performed based on an in-house tools. A critical point appeared to be the power consumption of the satellite on which dedicated effort is currently being put in order to better estimate the power consumption and characterize the capability of the battery with respect to temperature. This, in turn with a thermal

model of the satellite, currently being built at the time of writing, should provide sufficient information to ensure whether the power budget remains positive or whether alternative solutions should be investigated such as reducing the functionality of the payload during critical periods. Furthermore, thanks to the mission analysis, it was demonstrated that the previous data rate used of Robusta 1A and 1B, is not sufficient and requires updates. In the frame of the project, it was decided to upgrade the entire TT&C subsystem to a digital radio-communication module increasing the data rate as well as reducing power consumption. All the calculations previously presented are to be updated:

- when the orbit will be fixed (the baseline orbit for the study was chosen to be SSO at 650 km altitude);
- when the launch date will be confirmed as there is a dependance with the solar activity;
- when more realistic values (measured values of power consumption, etc.) are provided by the project team in order to ensure that the power budget is well within margin.

The development of the Robusta 1C platform (used for MTCube) was carried in order to ensure a good level of flexibility for future missions. Some of the improvements are listed below:

- the volume available for the payload was maximized;
- additional temperature measurements were performed on each face;
- battery charging, CAN sniffer and RBF pin connectors were put on the same face for easing the access during final integration and testing.

Finally, the radiation environment for the studied orbit was calculated. Preliminary dose calculations showed that, as expected based on the explanations given in 1.2.3, the dose received by the payload should not be detrimental to the good functionality of the subsystems, as well as should not impact the SEE characterisation of the selected memories due to synergetic effects.

In this chapter, radiation effects were discussed more generally at a spacecraft system level. The next chapter will focus on how an ionized particle interacting with matter may eventually lead to SEEs at a transistor level, which are the basic elements of many electronic components. This will allow to better understand commonly used parameters enabling the characterisation of the sensitivity of a memory that will be discussed in chapters 3, 4 and 5.

1.6 Bibliography

[Adams, 1981] J.H. Adams et al., “Cosmic ray effects on microelectronics, Part 1: The near-earth particle environment”, August 1981.

[Adams, 1983] J. H. Adams, Jr., J. R. Letaw, and D. F. Smart, "Cosmic Ray Effects on Microelectronics, Part II: The Geomagnetic Cutoff Effects," in *Naval Research Laboratory*, Washington D.C., NRL Memorandum Report 4506, May 1983.

[Arstechnica, 2016] Website: http://arstechnica.com/science/2013/03/flash-memory-issue-forces-curiosity-rover-into-safe-mode/, last accessed on the 01/12/2016.

[Barth, 2003] J. L. Barth, C. S. Dyer, E. G. Stassinopoulos, “Space, Atmospheric, and Terrestrial Radiation Environments”, in *IEEE Transactions On Nuclear Science*, Vol. 50, No. 3, June 2003.

[Bagatin, 2008] M. Bagatin et al., Key Contributions to the Cross Section of NAND Flash Memories Irradiated With Heavy-Ions, TNS, Vol. 55, No. 6, December 2008.

[Baumann, 2005] R.C. Baumann, “Radiation-Induced Soft Errors in Advanced Semiconductor Technologies”, in *IEEE Transactions on Device and Materials Reliability*, Vol. 5, No.3, Sept 2005.

[Bedingfield, 1996] K.L. Bedingfield, R.D. Leach, and M.B. Alexander, Editor, “Spacecraft system failures and anomalies attributed to the natural space environment”, in *NASA reference publication 1390*, August 1996.

[Boch, 2011] J. Boch *et al*., "ELDRS: Optimization Tools for the Switched Dose Rate Technique," in *IEEE Transactions on Nuclear Science*, vol. 58, no. 6, pp. 2998-3003, Dec. 2011.

[Bourdarie, 2008] S. Bourdarie and M. Xapsos, "The Near-Earth Space Radiation Environment," in *IEEE Transactions on Nuclear Science*, vol. 55, no. 4, pp. 1810-1832, Aug. 2008.

[Brown, 1990] D. B. Brown, "Total Dose Effects at Dose Rates Typical of Space," in *NSREC Short Course*, pp. 9-10, I-119, 1990.

[Cannon, 2008] E. H. Cannon et al., Multi-Bit Upsets In 65nm SOI SRAMs, CFP08RPS-CDR 46th Annual International Reliability Physics Symposium, Phoenix, 2008.

[CDS, rev13] CubeSat Design Specification, Cal Poly SLO, Rev. 13.

[CelestLab, 2016] Website: https://atoms.scilab.org/toolboxes/celestlab, last accessed on 05-12-2016.

[Croley, 1995] D. R. Croley, H. B. Garrett, G. B. Murphy and T. L. Garrard, "Solar particle induced upsets in the TDRS-1 attitude control system RAM during the October 1989 solar particle events," in *IEEE Transactions on Nuclear Science*, vol. 42, no. 5, pp. 1489-1496, Oct 1995.

[Deneau, 2010] C. Deneau, N. Roche, S. Jarrix, and L. Dusseau, "Robusta the first born French modular Cubesat", proceedings *Small Satellite Systems and Services*, Funchal, Madeira, Portugal, 31 May - 4 June 2010.

[Deneau, 2012] C. Deneau, J.R. Vaille, F. Bezerra, E. Lorfevre, R. Ecoffet, L. Dusseau, A compact dosimeter for space applications, Real Time Conference (RT), June 2012.

[Dyer, 2001] C. Dyer, "Radiation Effects on Spacecraft & Aircraft", in *Proc. "SOLSPA: The Second Solar Cycle and Space Weather Euroconference"*, Vico Equense, Italy, 24-29 Sept. 2001.

[Ecoffet, 2011] R. Ecoffet, "On-orbit Anomalies: Investigations and Root Cause Determination",

[Ecoffet, 2013] R. Ecoffet, "Spacecraft Anomalies Associated with Radiation Effects", in *RADECS 2013 Short Course Proceedings*, Chap. VIII, 2013.

[ESA, 2008] ESA-ADMIN-IPOL(2008)2 - Space Debris Mitigation for Agency Projects.

[ESCC25100, 2012] Single Event Effects Test Methods and Guidelines, *ESCC Basic Specification* No. 25100, Issue 1, October 2012.

[Ferlet-Cavrois, 2012] V. Ferlet-Cavrois, "Influence of Beam Conditions and Energy for SEE Testing", in *IEEE Transactions On Nuclear Science*, Vol. 59, No. 4, August 2012.

[Garrett, 2011] H.B. Garrett, "Spacecraft Environment Interactions", in *NSREC Short Course 2011: Back to Basics*, section I, 2011.

[Holmes, 1994] A. Holmes-Siedle, L. Adams, "Handbook of Radiation Effects", in Oxford Science Publications, 1994.

[IPOL, 2008] ESA-ADMIN-IPOL(2008)2 - Space Debris Mitigation for Agency.

[JEDEC57, 1996] Test Procedures for the Measurement of Single-Event Effects in *Semiconductor Devices from Heavy Ion Irradiation*, JEDEC Test Standard, No 57, December 1996.

[JPL, 2016] Website: http://www.jpl.nasa.gov/news/news.php?release=2013-078, last accessed on the 01/12/2016.

[J. D'Aleo, 2011] J. D'Aleo, Solar Changes and the Climate (Chapter 10), in *Evidence-Based Climate Science*, Elsevier 2011.

[Lawrence, 2009] R.K. Lawrence et al., Soft Error Sensitivities in 90 nm Bulk CMOS SRAMs, in *Radiation Effects Data Workshop*, July 2009.

[Lorentzen, 2002] K. R. Lorentzen, J. E. Mazur, M. D. Looper, J. F. Fennell, J. B. Blake, "Multisatellite observations of MeV ion injections during storms", in *Journal of Geophysical Research*, Vol. 107, Issue A9, Sept. 2002.

[LOS, 2008] Loi sur les Opérations Spatiales, LOI n° 2008-518 du 3 juin 2008 relative aux opérations spatiales.

[Mekki, 2015] J. Mekki, M. Brugger, R. G. Alia, A. Thornton, N. C. Dos Santos Mota and S. Danzeca, "A Mixed Field Facility at CERN for Radiation Test: CHARM," *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Moscow, 2015, pp. 1-4.

[MSL1, 2016] http://www.jpl.nasa.gov/news/news.php?release=2013-078.

[MSL2, 2016] http://arstechnica.com/science/2013/03/flash-memory-issue-forces-curiosity-rover-into-safe-mode/.

[NASA, 2014] NASA/Goddard Space Flight Center, Earth's radiation belt: Van Allen probes reveal 'zebra stripes' in space, http://www.sciencedaily.com/releases/2014/03/140319153200.htm, March 19 2014, last accessed on 06/04/2014.

[Nuns, 2008] T. Nuns et al., Evaluation of Recent Technologies of Nonvolatile RAM, IEEE Transactions On Nuclear Science, Vol. 55, No. 4, August 2008.

[O'Brien, 2013] T.P. O'Brien and J.E. Mazur, "The Space Radiation and Plasma Environment", in *RADECS 2013 Short Course*, 2013.

[OMERE, 2016] www.spenvis.oma.be (accessed on the 20th April 2016).

[Perez, 2010] S. Perez, C. Deneau, N. J-H. Roche, M. Bernard, L. Dusseau, S. Jarrix, "Concepts for Modularity and Standardization of Electronic Boards on Small Satellites", *IAC 61th conference (International Astronautical Congress)*, Prague, Czech Republic, 27 Sept.- 1er Oct. 2010.

[Petersen, 2011] E. Petersen, "Single Event Effects in Aerospace", in *IEEE Press*, 2011.

[Reames, 1995] D.V. Reames, "Solar energetic particles: A paradigm shift", in *Reviews of Geophysics*, supplement, p.585-589, July 1995.

[Reed, 2008] R. Reed, "Fundamental Mechanisms for Single Particle-Induced Soft Errors", in *NSREC Short Course 2008*, section I, 2008.

[Rousselet, 2016] M. Rousselet, "Developpement de méthodologies de tests en radiation des nanosatellites", *PhD manuscript*, defended on 16th Dec. 2016.

[Senni, 2016] S. Senni, "Exploration of non-volatile magnetic memory for processor architecture", *PhD manuscript*, defended on the 14th December 2015.

[SPENVIS, 2016] http://www.trad.fr/OMERE-14.html (accessed on the 20th April 2016).

[SRIM, 2013] http://www.srim.org/index.htm.

[Swift, 2000] G. M. Swift and S. M. Guertin, "In-flight observations of multiple-bit upset in DRAMs," in *IEEE Transactions on Nuclear Science*, vol. 47, no. 6, pp. 2386-2391, Dec 2000.

[Tipton, 2008] A. D. Tipton, "Device-Orientation Effects on Multiple-Bit Upset in 65 nm SRAMs", in *IEEE Transactions On Nuclear Science*, Vol. 55, No. 6, December 2008.

[Weulersse, 2011] C. Weulersse, "Développement et validation d'outils Monte-Carlo pour la prédiction des basculements logiques induits par les radiations dans les memories SRAM très largement submicroniques", *Thesis manuscript, Université Montpellier*, 6th Dec. 2011.

[Wilkinson, 1991] D. C. Wilkinson, S. C. Daughtridge, J. L. Stone, H. H. Sauer and P. Darling, "TDRS-1 single event upsets and the effect of the space environment," in *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1708-1712, Dec 1991.

[Weste, 2010] N. Weste, D. Money Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", section 9.5.2, fourth edition, March 11, 2010.

Chapter 2

Single Event Effect testing

2.1 Introduction

In this chapter, a focus will be made to briefly review how a particle may interact with matter and the different mechanisms responsible for the generation of bit upsets at IC system level. The focus will be on mechanisms inducing Single Event Effects (SEEs), as this is the main target of the current work. The generally adopted methods and parameters used to quantify the sensitivity of a memory device will be defined and presented as they will be used in the subsequent chapters (chapter 3, 4 and 5) that will focus more on the response and the possible failure mechanisms of the different tested memories. Finally, from a more experimental point of view, will be presented the testing methods used to test the current memory devices as well as the set-up used to implement these tests.

2.2 Single Event Effects on memories

In order to understand how SEE may occur on IC devices, and more specifically in memories, it is necessary to understand, at a physical level, how an ionized particle may interact with matter in general, and how the target material properties as well as the impinging particle physical characteristics may affect the ionization of the target material.

2.2.1 Introduction to particle-matter interaction

When passing through matter, a particle loses its energy either totally or partially. This energy is lost through a succession of different electromagnetic interactions with the atoms and/or their nuclei constituting the material. These interactions depend on the type of particle, its energy and the material itself. The effects of particle-matter interaction can be grouped into three main groups when it comes to the radiation effects on electronic components [Ecoffet, 2011]:

1. Creation of electron-hole pairs which can then be collected at a sensitive area and affect the good functionality of an electrical component or an electrical node (SEE);
2. Trapping of electron-hole pairs in dielectrics causing its progressive degradation (Total Ionizing Dose or TID);
3. Modification of the lattice structure due to impinging particles (Total Non Ionizing Dose or TNID).

The current work focuses on SEE generated in the space environment. Hence, the focus will be on the interactions between heavy-ions and protons with matter, as these two types of particles are those mainly responsible for SEE on ICs as it was presented in chapter 1. For these two types of particles, there are two mechanisms responsible for the loss of energy of the impinging particle in matter responsible for the ionization of matter: the direct and indirect ionizations (Figure 21). The impinging ion (leftmost particle) generates itself electron-hole pairs (plus and minus signs on Figure 21) through direct ionization process, while the p+ (or proton, rightmost particle) hits an atom from the target transferring some of its initial energy and generating a secondary ion, which will in turn generate electron-hole pairs. These two mechanisms will be described more in-depth in the next sections.

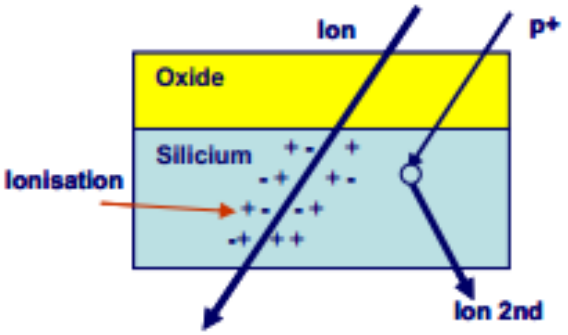


Figure 21: Simplified mechanisms of ionization responsible for SEE: direct (left) and indirect (right) ionization [Ecoffet, 2013].

2.2.2 Ion interact with matter: direct ionization

Due to its charge, an ion will directly interact with the atoms of the material through electromagnetic coulombic interactions. Through successive interactions, the ion progressively loses its energy.

Along its path through matter, the ion leaves a so-called ionizing trail: this trail is constituted of a high density of electron-hole pairs in a very localized area mostly along the straight path of the ion. Indeed, the ion does not much deviate from its initial direction if the energy loss along its path is well below its initial energy.

In order to quantify the ionization of matter induced by an ionized particle, the energy loss parameter is used which represents the mean amount of energy lost by the impinging ion through matter in the form of ionization by unit length. The total energy loss has two contributions (Equation 1): an electronic contribution (inelastic process during which the incident particle interacts with the electrons of the medium) and a nuclear contribution (elastic process during which the incident particle interacts with the nuclei of the medium). The total energy loss (per unit length) is also called stopping power. The linear energy transfer (or LET) on the other hand, is the local energy deposition in the material: hence, the LET value equals the total energy loss as long as radiative energy losses can be neglected [Kosmata, 2011]. The electronic contribution of the total energy loss is also called LET_{elect} or $\frac{dE}{dx}\Big|_{electronic}$ or electronic stopping power:

$$\frac{dE}{dx}\Big|_{total} = \frac{dE}{dx}\Big|_{electronic} + \frac{dE}{dx}\Big|_{nuclear}$$

Equation 1: Contributions to the total energy loss of a particle: electronic and nuclear contributions. Units are usually given in MeV/µm or MeV.cm²/mg.

As shown in Figure 22, for energies higher than MeV, the contribution of nuclear interactions to the total energy loss can be neglected and the total energy loss is almost completely equal to the electronic energy loss or LET_{elect} for heavy-ions. The simplified term of LET will be used from now onwards to refer to the electronic LET (LET_{elect}) as it will be used for the electronic LET of heavy-ions.

In order to have a value somehow independent of the material's phase the ion is passing through, the LET is mainly given by dividing it with the density of the matter. Above a few hundred of keV/nucleon, this LET can be estimated by the Bethe formula as presented in Equation 2 [Bethe, 1996]. However, other equations more or less accurate may be used to estimate the LET, the most accurate one being empirical but providing less insight about the impact of physical properties [Baze, 2011].

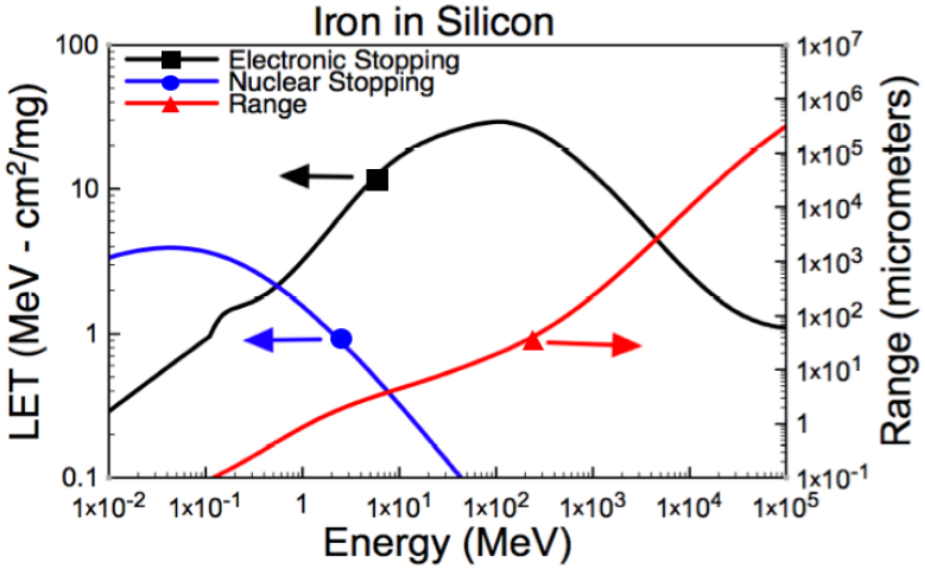


Figure 22: Example of the contribution of both electronic and nuclear interaction to the total energy loss of an iron in silicon along with its range based on SRIM results from [Reed, 2008].

$$\frac{1}{\rho}\left|\frac{dE}{dx}\right|_{elect} = LET_{elect} = \frac{4\pi}{m_e c^2}\frac{Z^2}{\beta^2}\frac{N_A Z_{target}}{A}\left(\frac{e^2}{4\pi\varepsilon_0}\right)^2\left[ln\left(\frac{2m_e c^2\beta^2}{I(1-\beta^2)}\right)-\beta^2\right] \propto Z^2 Z_{target}$$

Equation 2: Bethe-Block formula for the calculation of the electronic LET of an impinging ion in a target material.

Where ρ is the material density (kg.cm^{-3}), Z is the atomic number of the impinging ion, β the ratio between the particle speed over the speed of light c (m.s^{-1}), Z_{target} and A the atomic and mass number of the target atom constituting the matter the ion is crossing, m_e the mass of the electron at rest (kg), I the mean excitation potential of the target material (MeV – 0.170 MeV in silicon), N_A the Avogadro number (mol^{-1}), e the elementary charge (C) and ε_0 permittivity of vacuum (C.V^{-1}.cm^{-1}).

As shown in Equation 2, the electronic LET is independent from the mass of the impinging particle, but depends on its relative speed and is proportional to the square of its atomic number (Z). Hence, the higher the atomic number of an ion is, the higher the LET or the energy loss due to the higher colombic interactions.

In Figure 23 are presented the evolution of the LET vs. energy, and range vs. LET of the RADEF heavy-ion cocktail which is one of the tests facilities used several times for the experiments presented in this study. It can be seen that for a highly energetic particle, the LET progressively increases reaching a peak of ionization called the Bragg peak. Above this peak the energy, lost in electronic ionization, dramatically reduces along with the total energy of the particle.

At low energies (< few MeV), a proton's electronic LET is higher than at high energies. Hence, in sensitive components having a low enough LET threshold (below around 0.4 MeV.cm²/mg in silicon which is the maximum electronic LET of protons), low energy protons may induce upsets through direct ionization [Baze, 2011] as it can be seen in Figure 24. At higher energies, protons interact through indirect ionization processes as detailed in section 2.2.3.

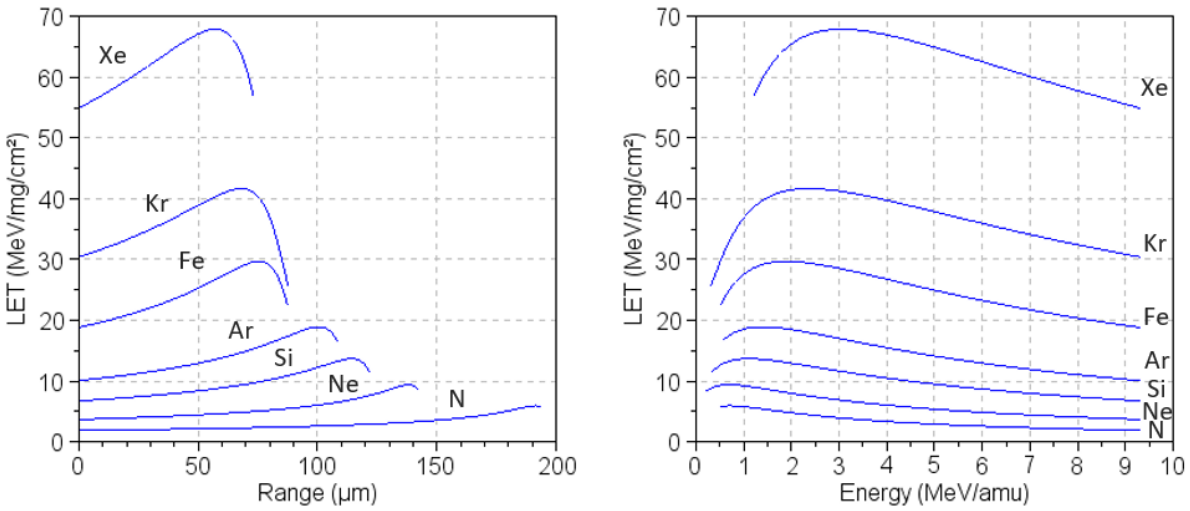


Figure 23: (left) Evolution of the LET (Y-axis in MeV.cm²/mg) along the path of the ion (range in µm) in silicon; (right) Evolution of the Energy (X-axis in MeV) of the ion with respect to its LET in silicon (Y-axis in MeV.cm²/mg). The maximum energy represented for all ions is 9.3 MeV/amu.

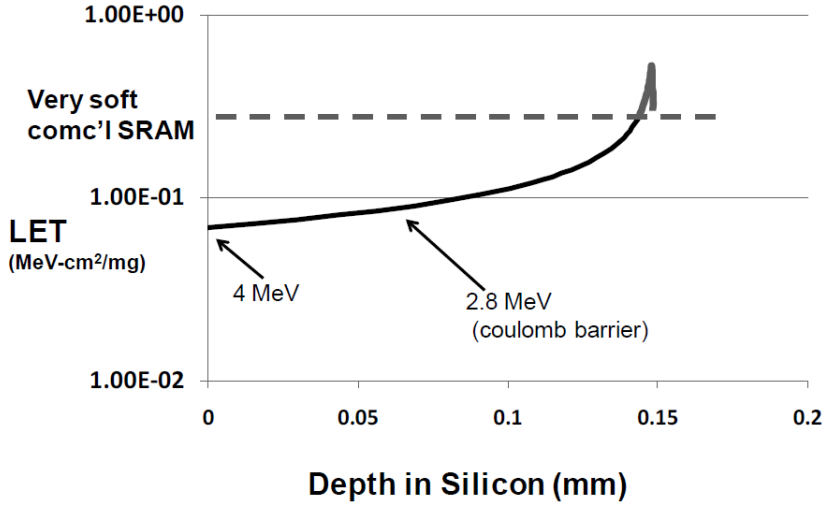


Figure 24: LET evolution vs. 4 MeV proton in silicon (initial energy) [Baze, 2011].

2.2.3 Nucleon interact with matter: indirect ionization

Protons are ions with the smallest charge, hence although there is a coulombic interaction with the atom of the target material, it is possible for a proton having sufficient energy to pass the Coulombic barrier and be able to interact (by strong interaction) directly with the atomic nuclei, similarly to neutrons which don't have any charge. The energy above which a proton is able to pass above the coulombic barrier is in the order of 4 MeV [Weulersse, 2011] (another value of 2.8 MeV is given in [Baze, 2011]) for a ^{28}Si target atom. The nuclear collision results in one or more ion recoils: each nuclear collision may generate one or more secondary ions having a particular charge, energy and angle with respect to the incoming proton. Considering a large proportion of protons generating nuclear reactions, overall, various species of secondary ions are created having different energies and angles. Some of the generated secondary ions have a LET, location and direction such that they are able to deposite a charge higher than the critical charge within the sensitive volume, and as such, they are able to induce a SEE.

Heavy-ions mostly interact with matter by direct ionization: due to the fact that they have a charge, the energy to go beyond the coulombic barrier is much higher. However, high energy, low *Z* and low LET

ions such as helium, lithium, beryllium that may be found in the space environment may be able to pass through the low columbic barrier and collide with a heavier nucleus from the target material generating higher LET recoil ions and hence a higher charge track [Baze, 2011].

Although neutrons are also able to generate SEE through indirect ionization, they are not usually considered in the upset rate calculation. Neutrons SEE in space may be due to nuclear atomic bombs exploding in the upper atmosphere as it occurred around the 1960s. Neutrons may also be created around 20 km in the Earth's atmosphere, mainly due to GCRs but also protons emitted from the Sun (the latter contribution is usually neglected except during solar events) some of which are directed outwards into space and then undergo a beta decay also contribution to the population of proton and electron in the inner Van Allen belt [Combier, 2016]. However, neutron SEEs are more of concern in atmospheric and ground environment.

2.2.4 Characterising memory sensitivity to SEEs

Whether from direct or indirect ionization, ultimately, electron-hole pairs are generated in the target material constituting the electronic device. The behaviour of those generated electron-hole pairs will heavily depend on the electrical properties of the device [Ecoffet, 2011].

The electron-hole pair track left by an impinging ion will directly undergo diffusion (recombination is neglected as their duration far exceed the duration of collection inducing SEE upsets) [Baze, 2011] [Weulersse, 2011]. If charges are generated in the depletion active region of a transistor, they will be promptly collected (< 1ns). Outside the depletion region the charge will be collected by diffusion at a later timeframe (~ 100 ns) which takes over at much longer timescales. However, when charges are collected near the depletion region, in the so-called funnelling region, which is in fact the deformation of the depletion region due to the trace left by the ionizing particle, charges are also very rapidly collected.

The charge collection at a critical node of a circuit may induce voltage and/or charge transients that in turn, either result in a transient response, which will not be enough to affect in a definitive way the expected output of the electrical system at a component level (generation of a SET), either in a change of state of the logic. The charge threshold above which such a change occurs is called the critical charge).

Stepping back from the transistor level to the whole IC device's point of view, when exposing an electronic component to a radiation environment inducing SEE, the resulting effects can be classified as presented in chapter 1, section 2.1.1.1. They may be self recoverable (SEU, MCU, MBU, some SEFI), recoverable after a specific action such as an erasing cycle, a power cycle (some SEFI, SEL), or not recoverable at all (stuck bits, SEB, SEGR).

By recording and counting the number of events (transient events, latch-up or bit flips) generated by a single particle on a given component, regardless of the number of errors it generated, it is possible to quantify the sensibility of the memory at a macroscopic level by calculating its cross-section by using the following equation (Equation 3):

$$\sigma_{events} = \frac{N_{events}}{F \times \#bits} \quad (in \frac{cm^2}{bit})$$

Equation 3: SEE cross-section for a given event (upset, transient, latch-up, etc.) regardless of the number of resulting bit flips but due to a single particle inducing an error.

N_{events} is the number of events (e.g. the number of impinging particles able to generated errors), F is the fluence or the number of particles per cm² received during the test, $\#bits$ is the size of the memory (in bits). The latter parameter allows comparing sensitivity at bit level, which makes easier to compare different memory cross-sections having different size or bit capacity.

The cross-section can be viewed as the probability of occurrence of a type of event in a given SEE radiation environment in cm^2 and per bit (in the case where the cross-section is divided by the bit capacity of the memory). The cross-section is given with respect to the incoming particle LET (for heavy-ion) or energy (for protons). Hence, by evaluating the sensitivity of the component at every LET or energy encountered in the space environment (or any other SEE inducing radiation environment) it may be possible to estimate the average number of SEE events occurring in the memory. However, as it is not possible to test all and every LET (or energy) the cross-sections need to be interpolated and extrapolated. More details will be provided in chapter 6 regarding this aspect.

2.3 Testing memories against SEE

The underlying mechanisms generating an SEE have been briefly reviewed at the particle and matter interaction level. At component level, it was explained how the sensitivity of the memory can be evaluated by estimating its cross-section. However, as it will be seen in chapters 3, 4 and 5, the cross-section depends not only on the beam conditions and other parameters such as tilt, but can be greatly impacted by the way the memory is stimulated during irradiation [Tsiligiannis, 2014]. Therefore, memory testing is performed using two types of testing methods: static and dynamic testing modes, which provide two different types of stimulation mimicking the behaviour of the memory: storing the information, and being actively accessed. The latter type of test mode (dynamic test) not only allows to stress the memory cells, but also all the peripheral controlling circuitry, which may also be sensitive to radiation. Furthermore, besides the test modes, other parameters may impact the memory sensitivity, such as temperature, power supply voltage, access frequency, or data background.

2.3.1 Test methods

In [ESCC25100, 2014], it is mentioned that "the SEE tests are performed with the conditions of a specific application or worst-case for each device type" concerning parameters such as clock frequency, temperature, and power supply. Indeed, worst case conditions are not necessarily the same for SEL or SEU detection. However, the type of test performed on the component is not clearly mentioned: indeed it greatly depends on the type of components.

There are four main types of static tests that are generally performed: a given pattern (solid '1', solid '0' checkerboard '01010101'or random/bespoke pattern) is written on the memory before irradiation. At the end of the irradiation, the memory is read back and SEE are counted and logged. In the case of non-volatile memories, these tests may also be performed when the memory in not biased, this test will be called unbiased testing in the next chapters.

In dynamic testing there are many possibilities due to the various combinations of operations, addressing schemes, and data sequences. Several dynamic test methods have been developed within the research group showing the impact of the type of test on an SRAM memory: a specific test called "March Dynamic Stress" test was tested on an SRAM in order to maximize the sensitivity of the SRAM memory cell due to Read Equivalent Stress effect [Rech, 2012] [Dilillo, 2005]. In [Tsiligiannis, 2012], a set of tests was conducted under neutron irradiation and similar dynamic tests were performed, this time in [Tsiligiannis2, 2014], under heavy-ions. These tests are presented in Figure 25. These test algorithms, called March tests, are composed of several elements, and each element is composed of several read/write operations: "r" stands for read and "w" stands for write; the "1" or "0" is the binary information stored or read. Each element is applied to each memory address (word) of the memory, by advancing in the address space either in an ascending or descending order. The operations of each element are enclosed in parenthesis, while the marching direction is indicated by the arrows as can be seen in the example for the March C-, March Dynamic Stress, Mats+, E and F algorithms.

In [Tsiligiannis2, 2014] was also studied the impact of the addressing scheme: by addressing the memory in logically increasing/decreasing order, line by line (Fast Row), column by column (Fast Column), pseudo-randomly (LFSR), or by changing one or all-except-one bit (Gray or inverse Gray) between two consecutive addresses. Clearly, the choice of a specific dynamic test affects both the bit and the event cross-section of the SRAM memory as thoroughly discussed in [Tsiligiannis3, 2014], where motivations are given for those addressing schemes. In the current work, the different dynamic tests will be again used on SRAM memories, when tested not only under heavy-ion and low energy protons, but also under high energy protons (chapter 3). This impact of dynamic tests will be analysed for the FRAM memory (chapter 4). Regarding the Flash memory (chapter 5), as mostly the NAND Flash memory remains in retention mode, static tests will be the test the most representative for this type of memory.

March C-:

$\{\uparrow (w0); \uparrow (r0, w1); \uparrow (r1, w0); \downarrow (r0, w1); \downarrow (r1, w0); \uparrow (r0)\}$

March Dynamic Stress:

$\{\uparrow (r1, w0, r0, r0, r0, r0, r0);$
$\uparrow (r0, w1, r1, r1, r1, r1, r1);$
$\uparrow (r1, w0, r0, r0, r0, r0, r0);$
$\downarrow (r0, w1, r1, r1, r1, r1, r1);$
$\downarrow (r1, w0, r0, r0, r0, r0, r0);$
$\uparrow (r0, w1, r1, r1, r1, r1, r1)\}$

Mats+:

$\{\uparrow (w0); \uparrow (r0, w1); \downarrow (r1, w0)\}$

E:

$\{\uparrow (w0); \uparrow (r0); \uparrow (w1); \downarrow (r1)\}$

F:

$\{\uparrow (r0, w1); \uparrow (r1, w0)\}$

Figure 25: All the dynamic test algorithms used in this current work.

A final aspect is worth introducing before presenting the experimental results. A single highly ionizing particle may generate several bit upsets topologically close one to each other (clusters) and occurring at the same time. Regrouping the errors and counting the number of clusters can then give valuable information to estimate the error event rate, regardless of the type of event and the size of the clusters. In order to operate this type of study, it is necessary to know the address scrambling and interleaving schemes of the memories in order to physically map the location of each memory cell. For the 90nm and 65nm SRAMs studied in this research, this information was provided by the producer. The clustering methodology is described in [Tsiligiannis3, 2014].

2.3.2 Test set-up

The test set-up that was developed for the different memories was built based on improvements from the previous set-up built by the group [Tsiligiannis3, 2014], with the idea of having it flexible and adaptable as much as possible to all memories. See Figure 26 for a schematic overview of the test set-up. As both considered SRAMs shared the same packaging and pinning scheme, one set-up was developed in order to be used with both devices. Similarly, the MRAM and FRAM share the same packaging and somehow compatible pinning which enabled preparing a set-up versatile enough to be used for both memories by playing with jumpers on the test cards. For the Flash memory, although the packaging was similar to the SRAMs, the pinning of the memory was too different to have a versatile yet simple set-up, and so a dedicated set-up was built.

During a test campaign, several memory chips may be tested. It was hence decided to build the set-up using sockets in order to change on-the-spot the DUT very quickly and easily. This allows testing several different DUTs with a single set-up. Furthermore, in order to reduce the cabling and mounting complexity prior each testing, the set-up was made to directly connect to the electronic card controlling the test sequence on the memory. As shown in Figure 27, from the memory side of the set-up, the set-up is constituted of a double layer PCB board built in the LIRMM laboratory and adapter for the "90nm SRAM/65 nm SRAM", the "MRAM/FRAM" and the Flash memories. Headers allow connecting to a dedicated socket (TSOP I or TSOP II depending on the memory), which can be removed when necessary. This choice was made in order to increase the flexibility of the set-up: in case, for example, of a damaged PCB board (the connectors for the FPGA for example), the socket was still re-usable on another set-up. The only downside to the use of a socket is the difficulty to test memories at very high angles due to partial masking caused by the edges of the socket.

Although the power could be supplied by the memory controller side of the test set-up, it was decided to keep the power supply of the memory separated in order to be able to separately power cycle the memory (keeping the memory controller switched on) if required and be able to monitor the rough supply current for possible latch-up occurrences during the tests.

On the memory controller side, similarly to the previous test set-up, a Finite State Machine (FSM) was implemented on a Xilinx Spartan 3 FPGA Starter Kit. The FSM was specific to each memory and was controlled remotely via a serial RS232 protocol in order to start/stop or launch a specific test. The serial link was also used to collect the data during or after irradiation: only the flipped bits (errors) were logged, along with the event timestamp, the corrupted data and their address in the memory. This information, along with the fluence, was logged in a test log file for each test run and used for post-processing purposes. Although the FSM for the SRAM and FRAM test control was already developed by the team at the beginning of the current thesis and did not necessitate major updates, an extensive work was performed in order to build the Flash FSM test controller, which required to implement an FSM from scratch (except the serial protocol) taking into account the particularities of NAND Flash memory protocols.

Both controller side and the memory side of the set-up were chosen to be directly connected without ribbon cables for heavy-ion and low energy proton testing, this in order to further simplify the mounting steps prior to irradiation, as the distance between the FPGA and the DUT was sufficient enough to prevent errors in the controller devices. However for the high-energy proton testing requiring at least 1 meter of distance from the DUT, ribbon cables had to be introduced in the setup.

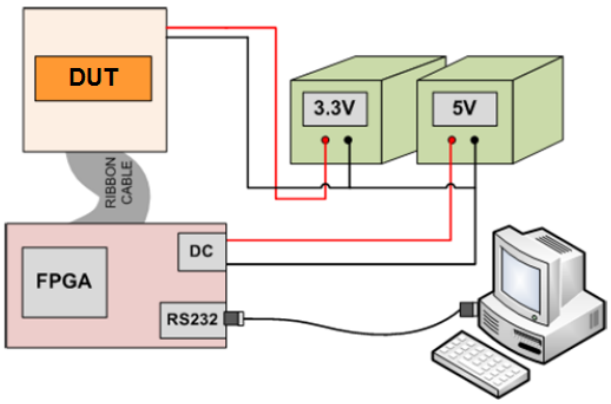


Figure 26: Schematic of the experimental set-up for SEE testing of memories. Sometimes used with ribbon cables and sometimes without.

The post-processing of the SRAM logs has been performed through an in-house tool (coded in C) that has been further improved, the post-processing of the Flash memory was coded in Scilab with the aim of being as much as possible automatized.

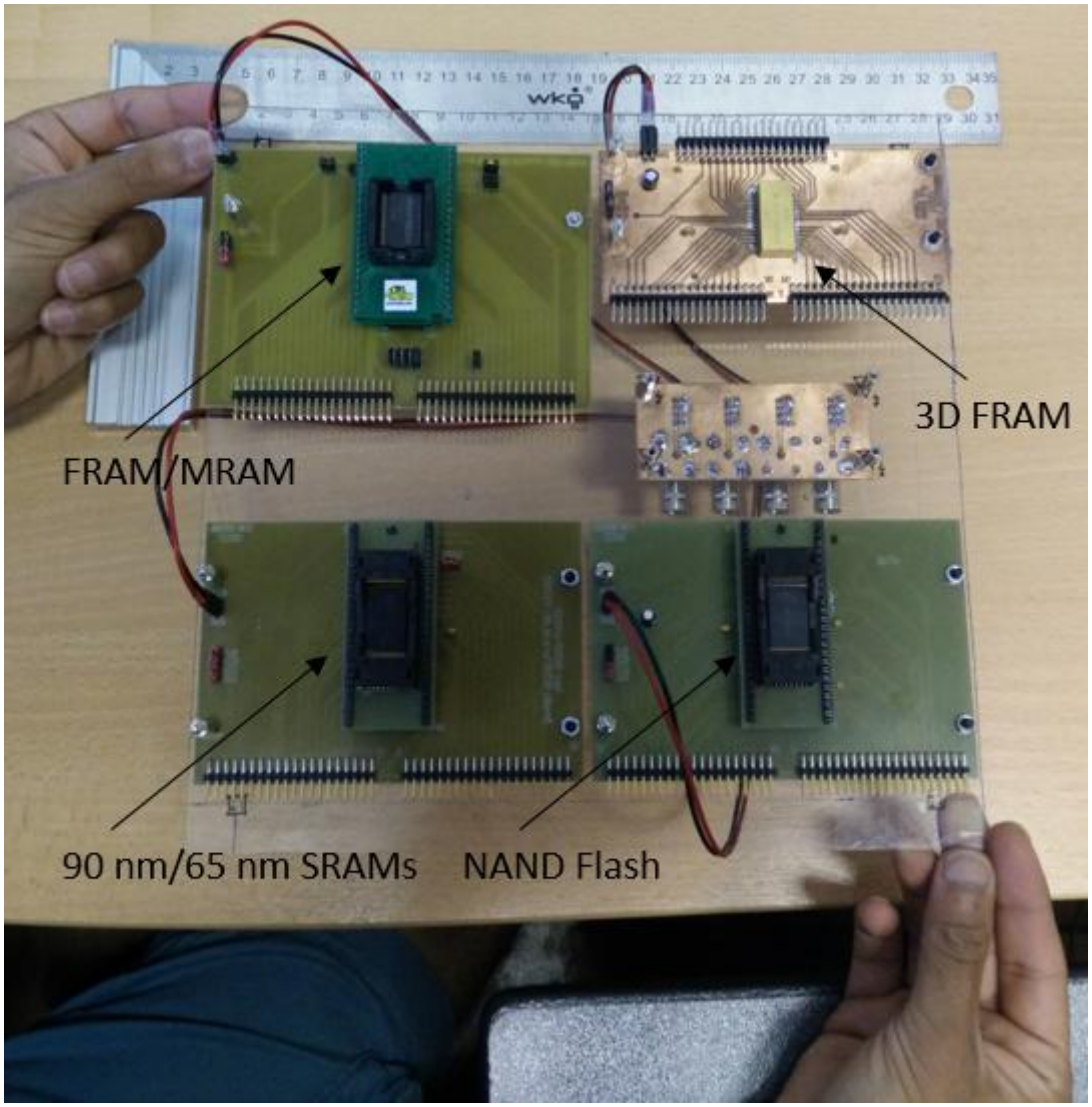


Figure 27: Example of a partial test set-up configuration used during the test campaigns showing the set-up directly exposed to the beam. Here four "memory side" set-ups can be seen (top-left: MRAM/FRAM, bottom-left: 90nm and 65nm SRAM, bottom-right: Flash, top-right: 3D FRAM). The removable memory sockets can be seen in the middle of each PCB card (except for the directly soldered 3D FRAM test board). The two headers at the bottom of the card make possible to either directly connect to the FPGA kit or to connect indirectly with ribbon cable. The shown set-up was actually used with ribbon cables during the PSI test campaign.

2.3.3 Test facilities

In order to measure the SEE sensitivity of the memory to a particular radiation environment, heavy-ion and proton tests must be performed as previously mentioned. The experimental data allows plotting the memory cross-section. This cross-section is then used to estimate the number of on-orbit errors for a particular space radiation environment, which depends on the orbit (chapter 6). Sixteen tests campaigns were performed so far and are summarized in Table 6. Tests were carried with low-energy protons (down to 600 keV) up to 50 MeV, high energy protons from 50 MeV to 200 MeV, as well as various heavy-ion cocktails, with LETs ranging from 1.1 to 67 MeV.cm²/mg. The last test campaign performed was different from the previous campaigns: an FRAM was tested using focused pulsed X-

ray beam (20-ID-B2 X-ray microprobe): the X-ray beam FWHM spot size was 1.77 µm x 1.87 µm and it's energy was 8 keV.

The RADEF Facility for heavy-ion [Virtanen, 2007] and for low-energy protons [Kettunen, 2014] is located in Finland and belongs to the University of Jyväskylä, the HIF facility (Heavy-Ion Facility) [Berger, 1996] belongs to the University of Louvain-La-Neuve in Belgium, The GANIL facility is located in Caën and the PSI (Paul Scherrer Institute) [Hajdas, 1996] is located in Switzerland. The ANL (Argonne National Laboratory) is located in Chicago, US. The beam is described in [Cardoza, 2015]. All these facilities are shown in Figure 28.

	TC1		TC2		TC3		TC4		TC5		TC6		TC7		TC8		TC9		TC10		TC12		TC13		TC15		TC16	
	RADEF		RADEF		RADEF		RADEF		HIF		RADEF		RADEF		RADEF		GANIL		RADEF		RADEF		RADEF		PSI		ANL	
	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D	S	D
SRAM90					t	t																								
SRAM65					t	t			t	t																				
FRAM						t	t	t								t					u,t	t								
Flash																							u,t	u,t						

HI cocktail N-Xe
HI cocktail Ne-Ar
UCL cocktail
GANIL cocktail
LEP (0.6-50 MeV)
HEP (50-200 MeV)
ANL microbeam
S,D static and dynamic
u test incl. unbiased mode
t test with tilt

Table 6: Summary of the test campaigns performed as of August 2016. TC stands for Test Campaign, HI for Heavy-ions, LEP for Low Energy Protons and HEP for High Energy Protons. TC11 and TC14 are not included as they are not part of the current study.

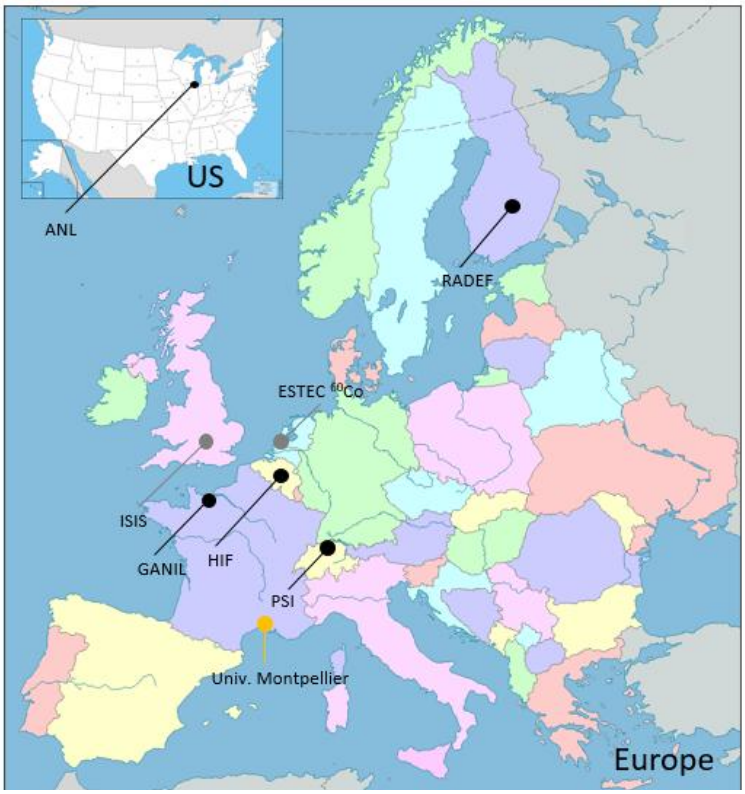


Figure 28: Location of all the SEE test facilities (in black) used to test the studies memories in the frame of the current study, but tests were also carried in ISIS (UK) and at the ESTEC ^{60}Co facility for other activities not developed here. The University of Montpellier is shown in yellow.

2.4 Conclusion

In this chapter, the basic physical mechanisms inducing radiation-related errors and damages in integrated circuits have been introduced, with a focus on Single Event Effects (SEEs). This enabled to present more in details some physical parameters such as the cross-section and the LET of heavy-ions or energy of protons that are measured or calculated and commonly used to assess the sensitivity of integrated circuits, in particular memories, after having performed SEE testing.

The test set-up used for the different memories was then presented and improvements from the previous test set-up made by the LIRMM team were highlighted. The fifteen test campaigns (TC) performed during this thesis represent a significant experimental work that has been summarised in Table 1. The experimental results presented in the next chapters (chapter 3, 4 and 5) are based on the results from those test campaigns using the above-mentioned set-up. The next chapters will present more in-depth the obtained results focusing in each chapter on a particular type of memory (SRAM, FRAM and Flash).

2.5 Bibliography

[Baze, 2011] M.P. Baze, "Single Event Effects in Digital and Linear ICs", in *NSREC Short Course 2011: Back to Basics*, section III, 2011.

[Bethe, 1996] Review of Particle Physics, Phys. Rev. D(54), pp. 132, 1996.

[Berger, 1996] G. Berger, G. Ryckewaert, R. Harboe-Sørensen, and L. Adams, "The heavy-ion irradiation facility at cyclone—a dedicated SEE beam line," in Proc. IEEE Rad. Effects Data Workshop Rec., Jul. 1996, pp. 78–83.

[Cardoza, 2015] D. Cardoza *et al*., "Investigating Pulsed X-ray Induced SEE in Analog Microelectronic Devices," in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2458-2467, Dec. 2015.

[Combier, 2016] A. CLARET; N. Combier; P. Laurent; V. Maget; D. Boscher; A. Ferrari; M. Brugger, "Improvements of FLUKA Calculation of the Neutron Albedo," in *IEEE Transactions on Nuclear Science* , vol.PP, no.99, pp.1-1.

[Dilillo, 2005] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan, "Efficient March Test Procedure for Dynamic Read Destructive Fault Detection in SRAM Memories", *JETTA Journal of Electronic Testing* - Theory and Applications, Springer, Vol. 21, n° 5, pp. 551-561, Octobre 2005.

[Ecoffet, 2011] R. Ecoffet, "On-orbit Anomalies: Investigations and Root Cause Determination", in *NSREC Short Course 2011: Back to Basics*, section IV, 2011.

[Ecoffet, 2013] R. Ecoffet, Spacecraft Anomalies Associated with Radiation Effects, RADECS 2013 Short Course Proceedings Chap. VIII, 2013.

[ESCC25100, 2014] "Single Event Effects Test Method and Guidelines, ESCC No.25100, Issue 2, Oct.2014.

[Hajdas, 1996] W. Hajdas, L. Adams, B. Nickson, A. Zehner, "The Proton Irradiation Facility at the Paul Scherrer Institute", *in Nuclear Instruments and Methods in Physics Research B*, vol. 113, pp.54, 1996.

[Kettunen, 2014] H. Kettunen, V. Ferlet-Cavrois, P. Roche, M. Rossi, A. Bosser, G. Gasiot, F.-X. Guerre, J. Jaatinen, A. Javanainen, F. Lochon, A. Virtanen, "Low Energy Protons at RADEF - Application to Advanced eSRAMs," in Proc. IEEE Rad. Effects Data Workshop Rec., July 2014, pp. 1-4.

[Kosmata, 2011] M. Kosmata, J. Auerhammer, M. Zier, F. Schlaphof, F. Schreiter and J. von Borany, "Influence of proton elastic scattering on soft error generation of SRAMs," 2011 12th European Conference on Radiation and Its Effects on Components and Systems, Sevilla, 2011, pp. 186-190.

[Rech, 2012] P. Rech, J-M. Galliere, P. Girard, A. Griffoni, J. Boch, F. Wrobel, F. Saigné, and L. Dilillo, “Neutron-Induced Multiple Bit Upsets on Two Commercial SRAMs Under Dynamic-Stress”, *IEEE Transaction on Nuclear Science*, Vol 59, Issue 4, pp 893-899.

[Reed, 2008] R. Reed, “Fundamental Mechanisms for Single Particle-Induced Soft Errors, *in NSREC Short Course 2008*, section I, 2008.

[Tsiligiannis, 2012] G. Tsiligiannis et al., Evaluation of test algorithms stress effect on SRAMs under neutron radiation, *in Proc. IEEE International On-Line Testing Symposium (IOLTS)*, pp.121-122, 2012.

[Tsiligiannis, 2014] G. Tsiligiannis et al., "Dynamic Test Methods for COTS SRAMs," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3095-3102, Dec. 2014.

[Tsiligiannis2 , 2014] G. Tsiligiannis, L. Dilillo, V. Gupta, A. Bosio, P. Girard, A. Todri, A. Virazel, H. Puchner, A. Bosser, A. Javanainen, A. Virtanen, F. Wrobel, L. Dusseau and F.Saigné, Efficient Dynamic Test Methods for COTS SRAMs Under Heavy-Ion Irradiation, *in NSREC 2014*, July 2014.

[Tsiligiannis3, 2014] G. Tsiligiannis, “Soft Errors in Memory Devices: Novel Methods and Practices for Dynamic and Static Testing”, Thesis manuscript, LIRMM/Université Montpellier, Sept. 2014.

[Virtanen, 2007] A. Virtanen, R. Harboe-Sørensen, A. Javanainen, H. Kettunen, H. Koivisto, and I. Riihimäki, “Upgrades for the RADEF facility,” in Proc. IEEE Rad. Effects Data Workshop Rec., Jul. 2007, pp. 38–41.

[Weulersse, 2011] C. Weulersse, "Développement et validation d’outils monte-carlo pour la prédiction des basculements logiques induits pou les radiations dans les mémoires SRAM très largement submicroniques", PhD Thesis, Montpellier, France, 6 Déc. 2011.

Chapter 3

Single Event Effect testing of volatile memories

3.1 Description of SRAM memories

3.1.1 Introduction

SRAM memories are one of the most commonly used volatile memories especially in embedded systems and a large part of the area of those systems is occupied by this type of memory. Besides, SRAM memories are used as processor cash, where latency (read/write latency <10ns) and power are of prime concern. On the other side, DRAM are preferred for their low cost and higher density at the expense of latency (read/write ~ 50 ns) [Troxel, 2009]. In fact, SRAM memories constitute a key device as their performance directly impacts the systems' overall performance and functionality. It is hence essential to understand their behaviour in a radiation environment.

SRAM memories are mainly produced with CMOS bulk and SOI technologies. The memory cell architecture the most widely used nowadays is the 6T structure: four transistors are used for the two-inverter loop (latch) and two access transistors allow accessing the cell nodes from the bit lines for read/write actions. No refresh of the content of the memory cell is required such as for DRAM or FRAM memories.

The SRAM memories under study in this work are Commercial-Off-The-Shelf (COTS) memories: these memories are readily available and were not designed for space applications. The advantage of COTS components is that they are usually lower in mass, they are denser, they consume less power and they have higher performance compared to their RadHard counterparts. One of the other main differences is also the price and availability. There has been a recent increase of the use of COTS components in satellites for the aforementioned reasons. Conversely, these components may require careful selection and characterisation in order to limit the risk of malfunction in space environment (vacuum, radiation, thermal cycling...). As a rough idea, the acceptable level of TID that can receive each group of component is typically:

- COTS components ➔ 5 to 20 krad;
- RadTolerant components ➔ 100 krad;
- RadHard components ➔ 1 Mrad.

In the next sections, the basic SRAM operations will be described along with the devices used for the current study, as well as the impact of a radiation environment on SRAM memories. This will then allow to better understand the results obtained during the several tests campaigned performed in order to characterise the sensitivity of SRAM memories selected for the scientific experiment of MTCube.

3.1.2 SRAM memory operations

In this section, we will briefly review the main operations allowing to store and read an SRAM memory cell. Although several types of architecture exist, the most common one, and the one used in the SRAM under study, is the 6T cell. This cell is constituted of six transistors (6T): there are two access transistors and four transistors (two PMOS and two NMOS) forming the two inverters, as can be seen in Figure 29.

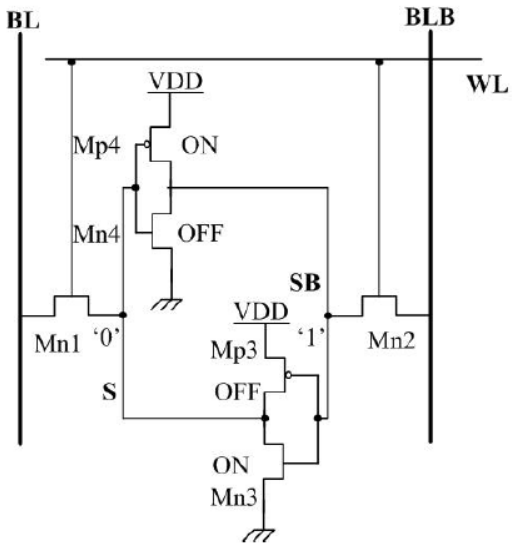


Figure 29: 6T transistor cell architecture (from [Dilillo, 2010]) BL and BLB are the two bit lines to which is connected the SRAM memory cell through the two access transistors (Mn1 and Mn2). The two nodes (S and SB) are where the information is stored.

A 6T memory cell is linked to the remaining memory circuitry through Bit Lines (BL) and Word Lines (WL), allowing accessing each individual cell (or word) and reading or writing data. In Figure 29, the access transistors are referred as Mn1 and Mn2.

First, in retention mode, the access transistors are switched OFF (WL at 0V) and the cell is isolated. The BLs are both pre-charged at V_{DD} and the latch made by the two-inverter loop (Mp4, Mn4, Mp3, Mn3 in Figure 29) stores the information by keeping one node at 0V (S in the example in Figure 29) and the other one (SB) in the opposite state (V_{DD}): depending on which node is at 0V, the cell stores a '0' or a '1'.

During a read operation, first the two BLs (BL and BLB) are pre-charged at V_{DD} and they are left floating which enables them to act as capacitors having the same potential. The access transistors are switched ON by setting the WL to V_{DD}. As the two nodes of the cell are in opposite states – one being at 0V (S at logic '0') the other one at V_{DD} (SB at logic '1'), the BL connected to the node at 0V will experience a small discharge whereas the other one will not, the node and the BLB being at the same potential. A differential sense amplifier will allow detecting which BL has been slightly discharged, this information in turn will provide in output the logic state stored in the cell.

Finally, in order to change the logic information stored within the memory cell, depending on the bit to be stored, the BLs will be set at either 0V or V_{DD} (BL and BLB always being at complementary logic values). Then the access transistors are turned ON. The write driver having high drive strength, the inverter loop will (or will not if the bit to be stored is the same as the previously stored bit in that memory cell) change its state.

In order to perform these operations, there are several other electrical blocks to activate these tasks, select the memory cells, read the stored information, send or receive data, synchronize and so on. Amongst other, in SRAM memories can be found:

- address decoders which allows selecting the row and column where to read/write;
- sense amplifiers which sense the state in which the memory cells is in order to convert in binary form;
- input/output (I/O) buffers where the content of the fetched data is retrieved prior latching the data on the I/O pins;
- synchronization circuitry ensuring that each action is performed one after the other;
- write/read drivers consisting of the logic sequence to perform the write/read operation;

- power and ground grids that feed the memory array as well as the peripheral circuitry;
- power switches that allow switching ON/OFF parts of the circuit. In the case of the studied SRAMs, they allow to select a supply voltage for the cell: low (~0.74V) to reduce power consumption but still be able to keep the stored data; high (> 1.1V) to allow read/write access without destroying the cell content during a read operation, or failing the write operation in a cell due to the reduced write noise margin.

Besides the memory cells, all the remaining electrical circuits (peripheral circuitry) may also be impacted by the radiation environment.

3.1.3 90 nm and 65 nm SRAM used in the current study

Two SRAM memories were studied as volatile memories in the current study. The first one is a 90 nm 32 Mb COTS asynchronous SRAM in bulk technology from Cypress. The second SRAM memory is similar to the previous one expect that it is manufactured with a more integrated technology (65 nm) and a size of 16 Mb. Furthermore, the 65 nm devices include a built-in error correction code (ECC), that could be disabled during radiation tests.

Several features are worth mentioning regarding these particular Cypress memories. First, the addresses are scrambled: the physical word (8 bits) locations of two continuous addresses are not next to each other. Then an interleaving scheme is also applied, which makes each bit of the same word topologically separated from each other. This architecture enables to make the memory less susceptible to MBUs: if a particle strike induces an MCU (small localised cluster of bit flips), the chances that more than one bit of a word flipping is reduced and the effectiveness of the ECC is enhanced (ECC are able to detect and correct only few bit errors in the same word). The memory is also divided in blocks electrically isolated by p-well and n-well taps. By doing so, latch-up occurrences are limited to those blocks and their propagation is spatially constrained [Tsiligiannis4, 2014]. Additionally, during read or write accesses, only the block where the accessed address is located at is powered to full V_{DD}; the remaining blocks are kept at lower voltage (low power). As will be discussed in the subsection 2.2, lowering the supply voltage, besides reducing the overall power consumption of the memory prevents the triggering of latch-up events in a radiation environment. On the other hand, lowering the voltage may reduce the SEU critical charge of the memory cell. Finally, the 32 Mb 90 nm SRAM has one particularity; it is constituted, as shown in Figure 30, of two identical stacked dies each of 16 Mb capacity.

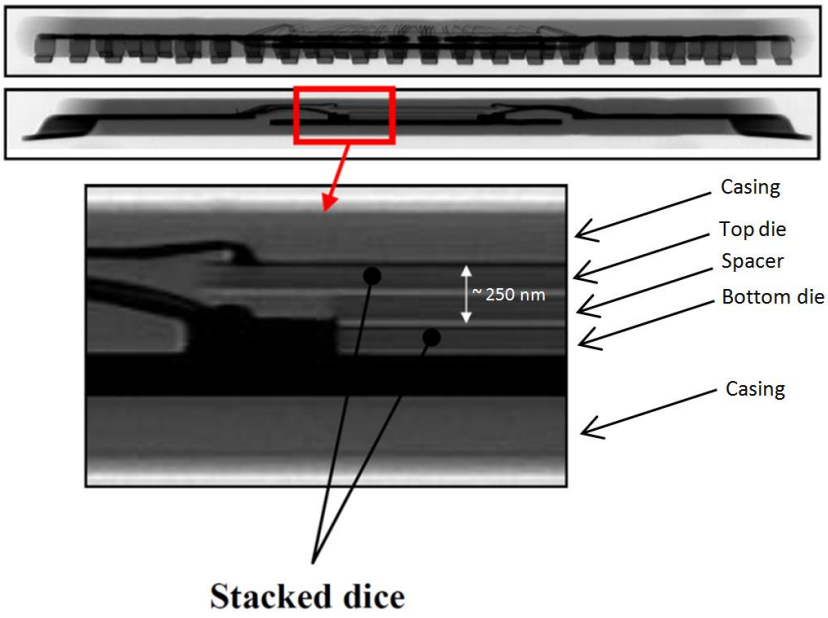


Figure 30: X-ray image of the 90 nm SRAM where the two vertically stacked dies can be seen.

Concerning the 65 nm SRAM, most of the features described above remain the same besides the fact that this memory is only constituted of a monolithic die. Improvements on the operation cycle and powering time of the block that are accessed are further added in order to increase the resilience of this memory to latch-up events by minimizing the power-up period (higher voltage) during operation access lowering the probability of a latchup occurrence. Finally, an ECC scheme was added which could correct a single bit error for every 32 bit (4 words of 8 bits). The ECC could be disabled thanks to information provided by the producer.

3.2 Radiation effects in SRAM memories

3.2.1 Core memory cell and peripheral circuitry sensitivity

Focusing solely on the SRAM memory cell structure, the weakest area is the reverse-biased junction [Baumann, 2005] [Pellish, 2010]. More specifically, the OFF state NMOS transistor's drain is found to be the weakest point against particle strikes (Figure 31). When a particle is able to directly or indirectly (via ion recoils) generate enough charge being able to be collected at this node, the parasitic current generated will force the node to which is connected the OFF state NMOS drain to discharge which may then lead to the entire flip of the bit cell.

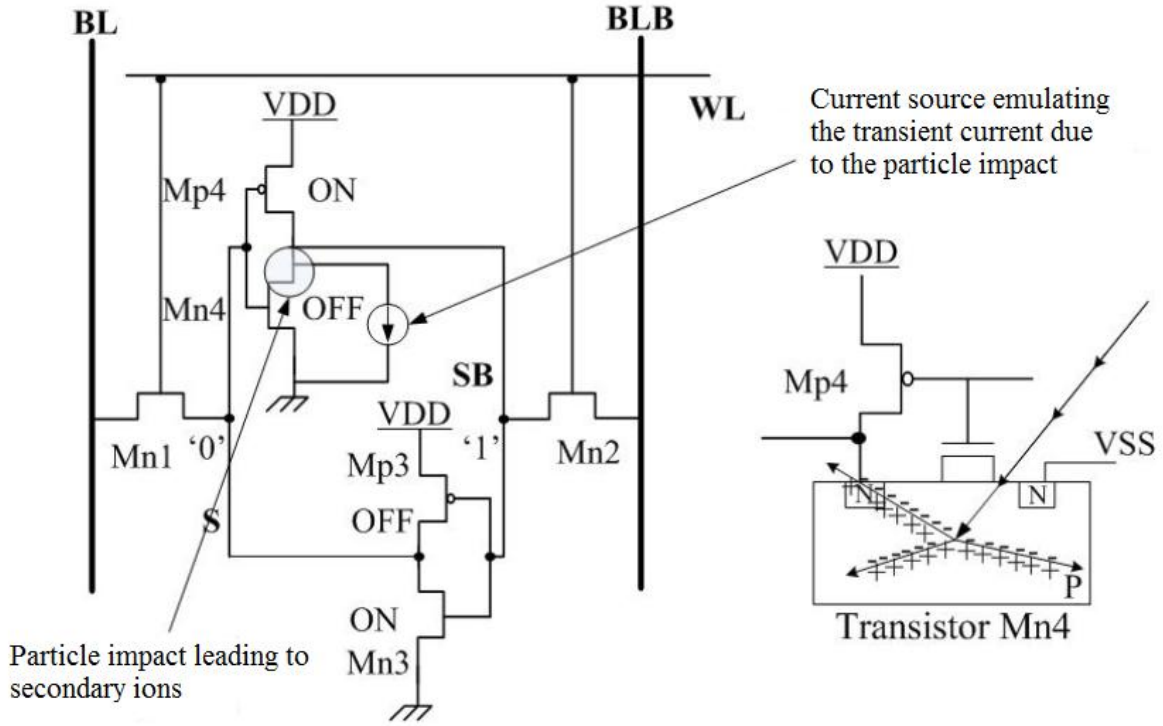


Figure 31: Electrical schematic of a 6T SRAM cell showing a current source simulating a current transient on the drain of a NMOS transistor in the OFF state due to a particle strike. This model is often used as a SRAM cell fault model. Slightly modified from [Tsiligiannis4, 2014].

Several techniques exist in order to mitigate or reduce as much as possible bit flips events in a radiation environment. Radiation hardening technics not only focuses on SEE but also TID mitigation. These RadHard components are designed to cope with space environment but their cost usually can be prohibitive and their performances are not those of COTS, especially for low cost missions. COTS components offer a better option (including lower power consumption, higher speed, higher density) at the expense of not necessarily being qualified for space application. Part qualification then has to be carried as explained in [ECSS-Q-ST-60, 2013]. That is particularly true for recent or new technologies, which have never been flown before.

Single events may not only induce SBU but MCU as well [Reed, 1997]. Recent technologies have experienced an increase in the number of MCUs. In fact, SBU are reduced due to the smaller cell area, but the size of MCU is increasing with technology [Tipton, 2006]: this is due to the fact that transistors are small and distances are reduced allowing the increase in probability of a particle impacting several memory cells or charge sharing occurring between cells. With downscaling, the critical charge is also reduced. The angle at which a particle strikes the memory plane appears to also increase the occurrence of MCUs [Felix, 2007].

In [Tsiligiannis2, 2014], the authors present a classification of the variety of events occurring on the 90 nm COTS bulk SRAM that was selected for the current study. Under heavy-ion, proton or neutron SEE testing, it is shown that not only the memory experiences SBU and MCUs, but some types of large scale errors that are in fact due to the peripheral circuitry of the memory. These Single Event Functional Interrupts (or SEFIs) may be due to temporary failure of the I/O circuitry, malfunction of the synchronization circuitry inducing delays on read/write operations, latchup of power switches resulting in large regions in errors. SEFIs appear only during dynamic mode testing as in static mode testing the peripheral circuitry is not solicited. As SRAM memory are types of memories often accessed, it is essential to also characterise its sensitivity in dynamic mode. Studies in [Tsiligiannis3, 2014] demonstrated the dependence of the access order on the SEE sensitivity of a 90 nm SRAM memory. In reality, the transistors used in the peripheral circuitry are much larger (thus robust) than those used for the memory cells. Nevertheless, a failure in this area may induce higher number of detected errors, with several hundreds or thousands of cells apparently failing [Baumann, 2005] [Tsiligiannis2, 2014].

3.2.2 Other parameters affecting SEE sensitivity of SRAM memories

Besides the inherent susceptibility of the memory plan and its peripheral circuitry, other aspects may increase the SEE sensitivity of memories. Regarding SEU sensitivity of the memory, the lower the power supplied to the core of the memory cell, the higher the SEU probability [Schwank, 2006]: this is due to the fact that lowering the voltage reduces the noise margins which the memory was initially designed for.

The biasing voltage plays an important role in the probability of appearance of latch-up events for latch-up sensitive devices. The lower the biasing voltage, the less probable is the appearance of a SEL, as discussed in [Felix, 2007] for the DUT memory under proton irradiation.

Temperature may also affect the SEU sensitivity of SRAM memories. As discussed in [Harboe, 2005], a small increase in the SEU cross-section was noticed at high LETs and for temperature of 100°C. Temperature increase may as well increase the probability of latch-up events as well. In [Tsiligiannis, 2014], the tested 90 nm SRAM saw an 80% increase of its event cross-section at 110°C when irradiated under neutron, whereas the 65 nm SRAM cross-section remained constant (with a small fluctuation within the statistical error range). Temperature increases leakage current reducing noise margin against SEEs.

In [Schwank, 2006] synergetic effects are studied, in order to understand the effect of Total Ionizing Dose (or TID), temperature and biasing on the memory SEU sensitivity. Not only a pattern dependency was shown on the SEU cross-section after TID tests perform for a given pattern, but a worse case was suggested by irradiating the memory at the maximum dose that it will experience, at the highest temperature and for the lowest supplied power. In [Schwank, 2005], the increase in SEU sensitivity post dose irradiation was attributed to radiation-induced increases in parasitic leakage current affecting the output voltage of bias level shift circuitry.

3.2.3 Scaling effect

The effect of SEE in modern technology is linked to the reduction of the minimum metal line width (technology node). Approximately every three years a more integrated technology is released on the market. Along with the metal line width, other components constituting the memory are shrinked. The gate oxide thickness reduction makes the transistors more robust against TID effects, since the positive oxide-trapped charges are more quickly removed from the oxide through the tunnelling process [Re, 2013]. The oxide traps are reduced, along with gate leakage currents due to dose effects [Ecoffet, 2011]. However, the CMOS technology has reached nowadays its limits (the leakage current increase, as the oxide thickness is reduced, leads to prohibitive power consumptions) and other different technologies are starting to be good candidates for smaller transistors such as FDSOIs and FinFETs.

In terms of SEEs, the smaller transistors induce a smaller sensitive volume hence a reduced probability for an ion to deposit enough charges inside [Wrobel, 2001]. Conversely, the total node capacitance along with the cell supplied voltage are reduced with downscaling, which in turns, implies a lower charge stored at the nodes (as a first approximation the charge stored at the node being the product of the node capacitance with the voltage supplied); the critical charge is then reduced leading to higher sensitivity of SRAM cells [Ecoffet, 2011]. For example, older technologies were not sensitive to low energy protons, which is the case with recent technologies due to direct ionization of protons at those very low energies (< 5 MeV). Another example, not related with space application, is the increase of sensitivity to muons [Bosser, 2016]. Besides, the increased frequency allowed by smaller transistors may increase the probability for a SET to get captured by a latch sampling and become a logic error.

Along with the smaller critical charge of a cell, the size of transistors being smaller, the distance between neighbouring cells is also reduced. This leads to the increase of MCU occurrence probability [Tipton, 2006], either by an impinging particle being able to strike several cells, or through charge sharing with nearby cells. If no countermeasures are implemented, the MCU cross-section is very likely increased with scaling whereas the SEU (event) cross-section may increase or remain stable due to the previously mentioned opposite effects of scaling. As can be seen in Figure 32, results in term of MCU size for the 90 nm and 65 nm SRAM under heavy-ion irradiation were compared and showed the increase in MCU size for the 65 nm (more integrated) compared to the 90 nm technology.

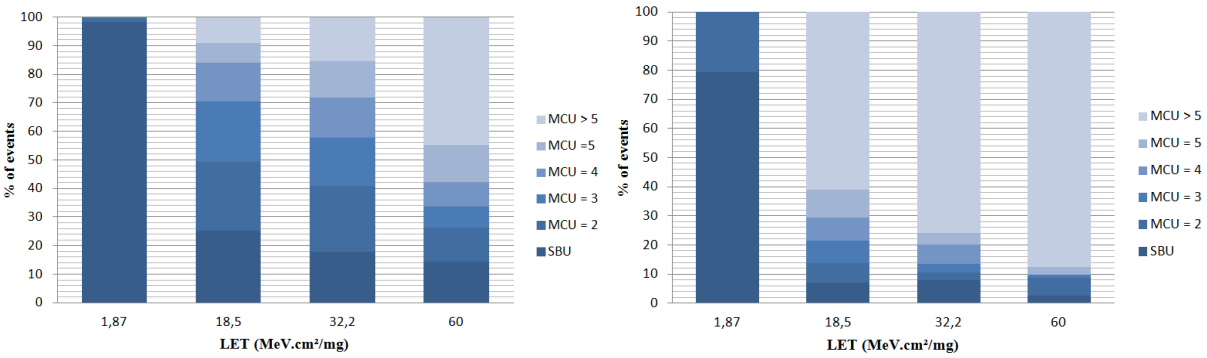


Figure 32: Histogram of the MCU size for the 90 nm (left) and 65 nm (right) SRAM subjected to heavy-ions [Georgios4, 2014].

Finally, SEFIs are becoming a growing concern: a failure of the periphery can induce several hundreds or even thousands or more cells to appear (or be) faulty. Due to the smaller propagation delays as the clock frequency is higher, and smaller load capacitances, the probability of an SET propagating to a logic block and inducing a faulty latch may lead to an increase of the SEFI cross-section [Baumann, 2005].

3.2.4 Bulk CMOS vs. SOI technologies

Besides bulk CMOS technology, SOI SRAMs are the preferred SRAM technology use for space applications thanks to their built-in resilience due to their design, suppressing the parasitic thyristor configuration that, when activated, results in a latch-up [Ferlet-Cavrois, 2002]. This is due to the complete isolation of the n-wells and p-wells. Figure 33 shows the differences between CMOS and SOI technology. Besides, the silicon volume between the gate oxide and the buried oxide is thin, which suppresses deep charge collection by funnelling that occur in bulk memories [Ferlet-Cavrois, 2002]. On the other hand, body ties are required to limit the parasitic bipolar structure that may be triggered during irradiation. This results in SOI process being more robust than bulk process as can be seen in [Roche, 2003] for neutron and alpha testing for 130 nm and 90 nm SRAM technologies, and also confirmed for low proton irradiation of 28 nm SRAM technologies [Kettunen, 2014].

Concerning the difference between SOI and bulk CMOS SRAM technology, [Pellish, 2010] explains that, due to the fact that bulk technology induces a thicker sensitive volume, and as many transistors are sharing the same n-well or p-wells, the number of MCU is higher for bulk CMOS technologies while it is not possible to have charge sharing occurring in SOI device [Raine, 2012], hence the multiplicity and number of MCU is very limited and can occur only if a particle is able to pass through two or more sensitive volumes. On the other hand, bulk technology does not appear to be pattern dependent which appears to be the case with SOI SRAMs at least as far as static tests are concerned.

Inclination also has an impact on the types of generated errors: bulk CMOS technology is much more dependent on the orientation of the particle than SOI technology [Pellish, 2010].

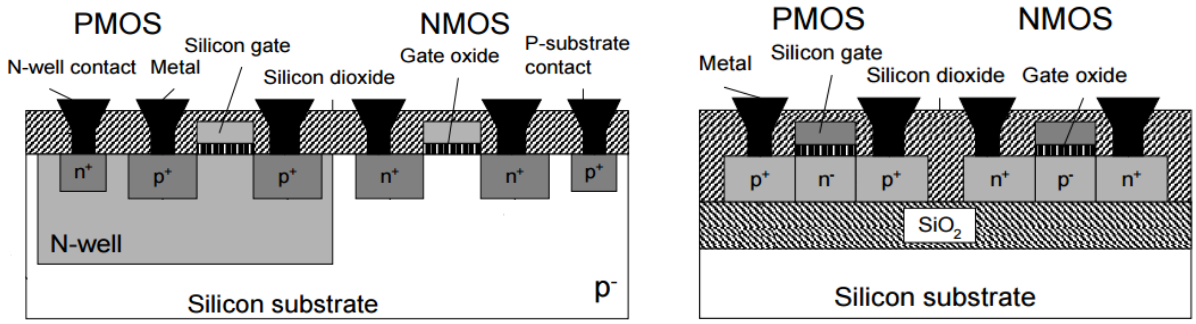


Figure 33: Cross section of a bulk (left) and SOI (right) CMOS technology from [Simonen, 2001] with minor modifications.

3.3 SRAM memories SEE characterisation

3.3.1 Heavy-ion testing results

The 90 nm and 65 nm SRAMs have been extensively tested against different dynamic and static test mode stimuli in [Tsiligiannis4, 2014]. The findings will be summarised in this section and new heavy-ion test data will be presented for both memories, which were in good agreement with the results obtained in [Tsiligiannis4, 2014].

3.3.1.1 90nm SRAM test results for single layer

For consistency sake, in this section, solely the upper layer of the two dies of the 90 nm memory was considered. Several tests were performed at different LETs in order to compare the response of the memory against SEEs. Such tests, as presented in Table 7 were: March Dynamic Stress [Rech, 2012], March C- [Marinescu, 1982] and Mats+ [Niggemeyer, 1998]. Each test is a succession of write and

read operations (‘w’ or ‘r’) writing a solid ‘0’ or solid ‘1’ pattern (‘0’ or ‘1’). A single March test is enclosed in brackets (‘{ }’) and inside, each element is enclosed in parenthesis (“( )”) and constituted of an operation. Each element is applied throughout the entire memory in an ascending (“↑”) or descending (“↓”) order. There is a multitude of ways of addressing a memory during dynamic test mode: assuming that the memory scrambling algorithm is known, the memory may be addressed by incrementing the addressing order of the memory (i.e. logical addressing), by addressing one raw after the other (i.e. fast raw addressing), similarly, by addressing column by column (i.e. fast column addressing), or even by addressing the memory in a random, pseudo-random to be precise (LFSR algorithm was used), order (i.e. random addressing). Finally, the order may be such that only one address bit is changed from one address to the next one (i.e. Gray addressing) or on the opposite, maximising the changes in the number of bits from one address to the next (i.e. inverse Gray addressing).

Name	Test
March C-	{↑(w0);↑(r0,w1); ↑(r1,w0); ↓(r0,w1); ↓(r1,w0); ↑(r0)}
Mats+	{↑(w0);↑(r0w1);↓(r1w0)}
March Dynamic Stress	{↑(r1,w0,r0,r0,r0,r0,r0); ↑(r0,w1,r1,r1,r1,r1,r1); ↑(r1,w0,r0,r0,r0,r0,r0); ↓(r0,w1,r1,r1,r1,r1,r1); ↓(r1,w0,r0,r0,r0,r0,r0); ↑(r0,w1,r1,r1,r1,r1,r1)}

Table 7: Marching Test algorithms used during SEE radiation testing (from [Tsiligiannis4, 2014]).

All these tests and addressing scheme combinations, along with static testing, were use to analyse their effects on both SRAM memories. These combinations enabled stressing various parts of the memory: not only the memory plan sensitivity, but also different parts of the peripheral circuitry such as the addressing decoders, the I/O buffers, or all of them at the same time [Tsiligiannis4, 2014].

Before presenting the results of the test campaigns, another important aspect is worth mentioning in order to better understand the results: Figure 34 depicts the physical location of errors (in black) on the memory plane with one pixel representing one bit. Besides single bit errors – or SBUs, there are many groups or clusters of errors. When looking more closely at those errors, it appears that not only they occur in small groups with bits next to each other (spatial proximity), they also occur about the same time (temporal proximity). These considerations highly favour the interpretation of a unique particle event inducing a large cluster of bit flips. The different topologies of clusters on the 90 nm SRAM were extensively studied in [Tsiligiannis2, 2014]; the clustering criteria selected for both SRAM memories are detailed in [Tsiligiannis4, 2014]. The resulting event cross-section, calculated by counting the number of events as opposed to the number of bit flips, provides a better insight in the sensitivity of the memory to impinging particles.

Static testing was performed using the most common patterns: solid ‘0’, solid ‘1’ and checkerboard patterns. Results showed no dependency of the static test patterns on the resulting bit cross-section. Figure 35 depicts the average bit and event cross-sections of all test campaigns performed on this particular memory for different particle LETs. In this figure and all subsequent figures, “LET at surface” means the LET of the particle reaching the surface of the die (and not the surface of the sensitive volume). It can be first noticed that, in static mode, the event cross-section is more than five times lower than the bit cross-section at high LETs. It means that, in average, each event leads to 5 upsets. In this figure, it can be noted that some bit and event cross-sections are lower than the expected trend around a LET of 20 and 32 MeV.cm²/mg. Looking more closely at those runs, it was noticed that

the total fluence in these cases were the lowest ones (in the order of 10^3 part/cm²), thus statistically less relevant.

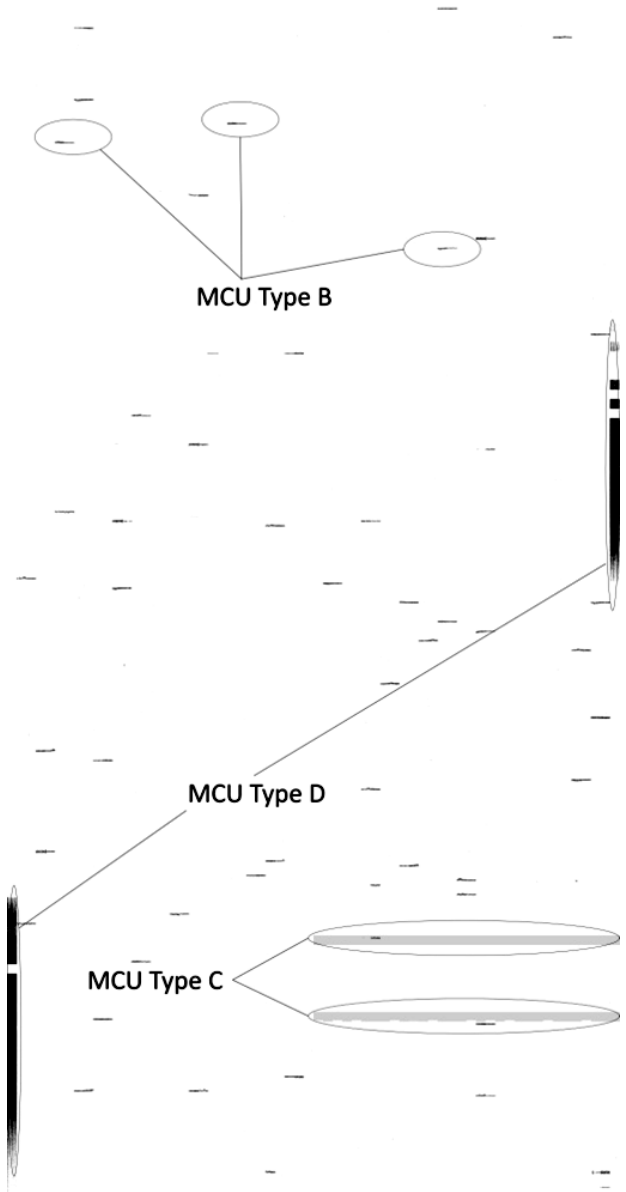


Figure 34: 90 nm SRAM bitmap irradiated to neutron at high temperatures from [Tsiligiannis4, 2014]. Each pixel represents one bit. The same types of clusters appear during heavy-ion irradiation. Type A clusters are not visible as they are small: they are small clusters of less than a few nearby bit flips, the same comment applies for SBUs.

Regarding dynamic test results, not only the SEE sensitivity of the memory is two orders of magnitude higher than in static mode when considering the total number of occurring bit flips, but the memory also shows a dependence on the order in which the memory cells are accessed. It appears that cross-section values have larger variations on the 90 nm as opposed to the 65 nm (as presented in the next subsection). This behaviour of the memory is due to the fact that it is much more prone to large cluster events (linked to the peripheral circuitry failure), or SEFIs, which occurred randomly during the runs. Hence for clarity, the static and dynamic tests are presented as average cross-section, which is caculated on several test campaigns under heavy-ions that were performed over the last two years. Detailed information regarding heavy-ion test results is discussed in [Tsiligiannis2, 2014].

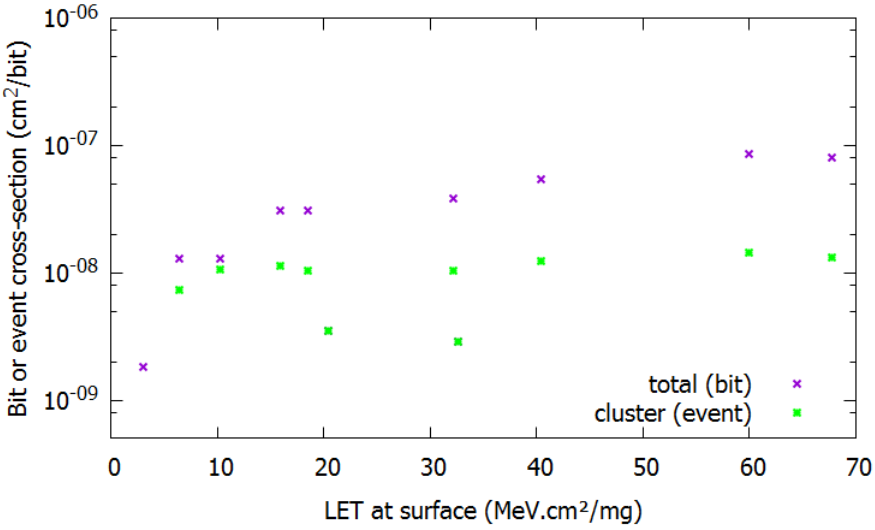


Figure 35: 90 nm top die SRAM static total and event heavy-ion cross-section per bit.

The March Dynamic Stress test has been selected for the MTCube RES experiment to maximize number of events, since it is the one that stresses (enhancing the sensitivity) the SRAMs the most, due to Read Equivalent effect [Dilillo, 2005]. Figure 36 shows the March Dynamic Stress cross-section of the memory. It can be seen that the bit cross-section can be up to more than two orders of magnitude higher to the event cross-section: this highlight the presence of large clusters of errors that may occur during dynamic testing of this memory. The selected addressing scheme chosen was a logical addressing scheme, which presents a good compromise in order not to avoid increasing the number of large clusters due to memory storage limitations. Due to the very wide range of type of cluster sizes and their high probability of occurrence in dynamic mode testing, the cross-section may vary from one run to the other. Hence, in Figure 36, the average cross-section is depicted where multiple runs in similar conditions were performed.

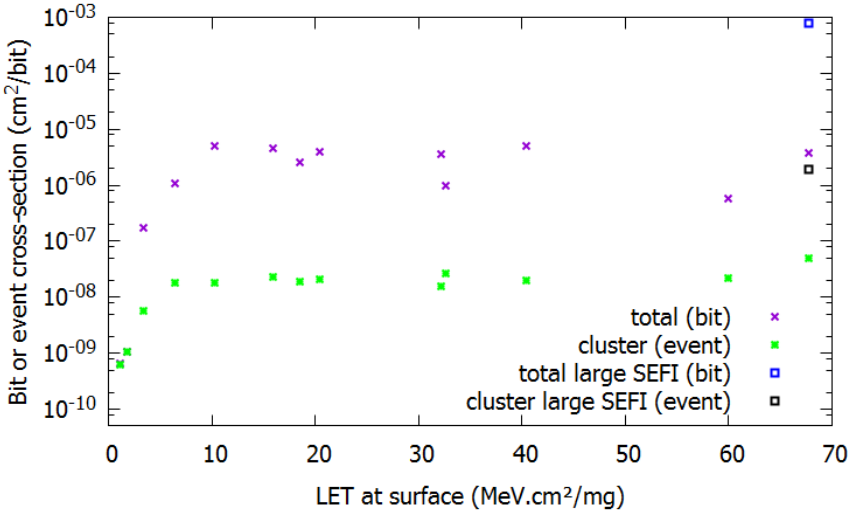


Figure 36: 90 nm top die SRAM March Dynamic Stress heavy-ion total and event heavy-ion cross-section per bit.

Regarding the few runs performed with a tilt, just considering the total flipped bit SEU cross-sections of static test of the upper layer, a comparison was made between the results obtained with high values of LET and those with high penetration (high energy) cocktail. The results are presented in the form of SEU cross-section plots in Figure 37. It can be seen that the SEU cross-sections obtained with both ion cocktails appear coherent. Nevertheless, at least two SEU cross-section points are lower than expected. In fact, three SEU cross-section points were obtained while having the memory placed at 45° for N, Ne and Ar ions providing values of effective LET of 4.7, 9.0, 22.5 MeV.cm²/mg, respectively. The

SEU cross-section for a LET of 4.7 MeV.cm²/mg and 9.0 MeV.cm²/mg does not follow the trend and present values lower than expected at these values of LET. A possible explanation is that the sensitive volume of each memory cell seems to be smaller in width compared to its vertical length.

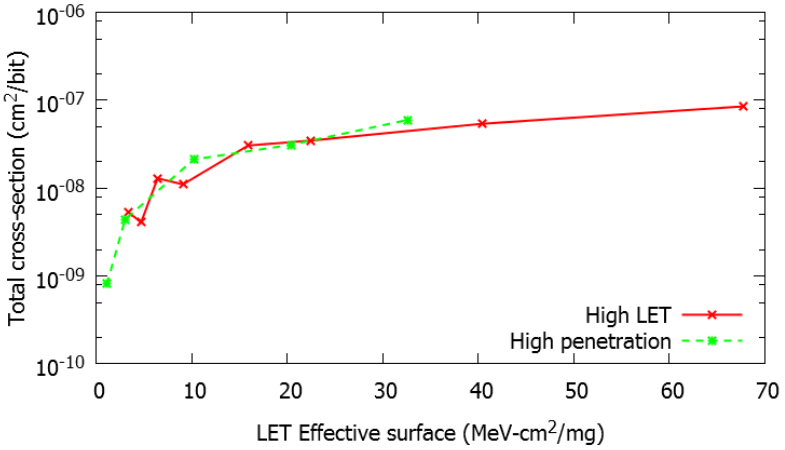


Figure 37: Total flipped bits heavy-ion SEU static cross-section of the upper layer for the high LET and high penetration cocktail. Data was obtained for 0° and in some cases 45°.

3.3.1.2 90 nm SRAM double layer considerations

SRAM devices, like in Systems in Packaging (SiPs), may be fabricated with several layers of dies; this is the case of the 90 nm Cypress 32 Mb SRAM (CY62177EV30 MoBL). As mentioned before, this memory is composed of two identical 16 Mb SRAM dies that are stacked on top of each other, as can be seen in Figure 38 presenting a schematic showing the layered structure of the memory. The thickness of each layer is not reported for confidentiality purposes.

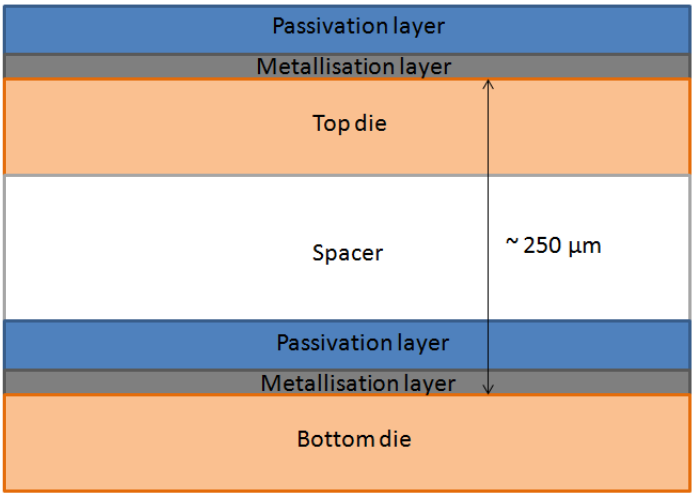


Figure 38: 90 nm SRAM simplified layer structure showing that the memory is constituted of two layers vertically stacked with an additional spacer in between the two dies (thicknesses are not mentioned for confidentiality purposes). The distance between the top of the two dies is approximately 250 µm.

For this study, the DUT was tested at two different facilities:

- The Radiation Effects Facility (RADEF) [Kettunen, 2014] in Jyväskylä (Finland) for the proton testing at energies below 50 MeV, which are considered low energies (tests being usually carried up to 200 MeV for SEE characterisation of components for space applications).
- Heavy-Ion facility (HIF) [Berger, 1996] in Louvain-La-Neuve (Belgium) for heavy-ion testing.

The used heavy-ion cocktail allowed testing from a LET of 1.1 MeV.cm²/mg up to 32.6 MeV.cm²/mg. As can be seen in Table 8, the particle range in silicon of those heavy-ions spans from 92.5 µm to 284

µm depending on the particle's LET. Similarly, as presented in Table 1 of chapter 1, the energies at which the DUT was tested under monoenergetic protons ranged from 0.6 MeV to 50 MeV. The protons had a range (in silicon) increasing with the energy from 8 µm (at 0.6 MeV) up to 12 mm (at 50 MeV), well beyond the thickness of the DUT.

Ion	Energy (MeV)	LET (MeV.cm²/mg)	Total range (µm)	Long. Straggling (µm)	Lateral Straggling (µm)
C	131	1.1	284.4	11.1	3.7
Ne	235	3	209.5	7.6	2.2
Ar	372	10.2	118.0	3.8	1.2
Ni	567	20.4	98.3	3.0	1.2
Kr	756	32.6	92.5	2.7	1.0

Table 8: Heavy-ions cocktail and their energies and ranges in silicon. Range and longitudinal and lateral straggling values are calculated by SRIM2013 in silicon target material.

For these test campaigns the various test methods presented in the previous section were similarly used to test the current SRAM memory. In this section, we will only consider the results coming from static test mode, since as explained earlier, it does not trigger large events such as SEFIs and SELs that could mislead the study.

3.3.1.3 Heavy-ion test results of stacked die SRAM memories

Based on the knowledge of the internal structure, it was possible to evaluate the LET at the surface of both dies assuming that the material was silicon. Asn in the ion cocktail used, the only ion able to penetrate more than the depth of the lower die (i.e. the carbon ion at 131 MeV) as depicted in Figure 39, the estimation was performed solely for this ion.

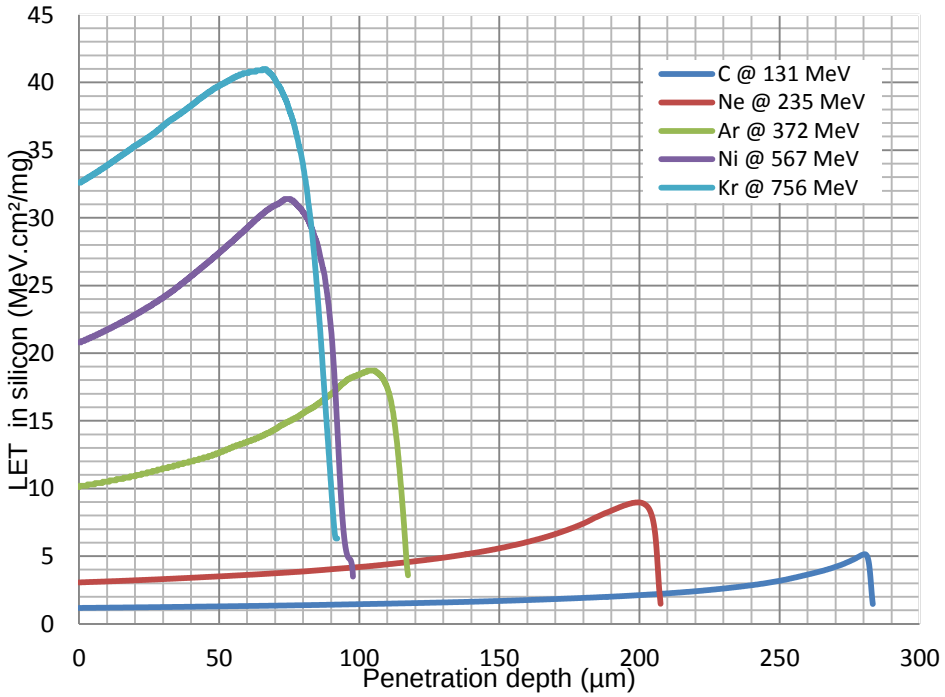


Figure 39: High penetration ions Bragg curves in Silicon.

The LET of the carbon ion being initially at 1.1 MeV.cm²/mg, its LET increases to about 3.3 MeV.cm²/mg at around 250 µm. This allows plotting the cross-section considering the LET at the surface of each die, which is shown in Figure 40. It can be noticed that the cross-section of the bottom die matches the top die cross-section.

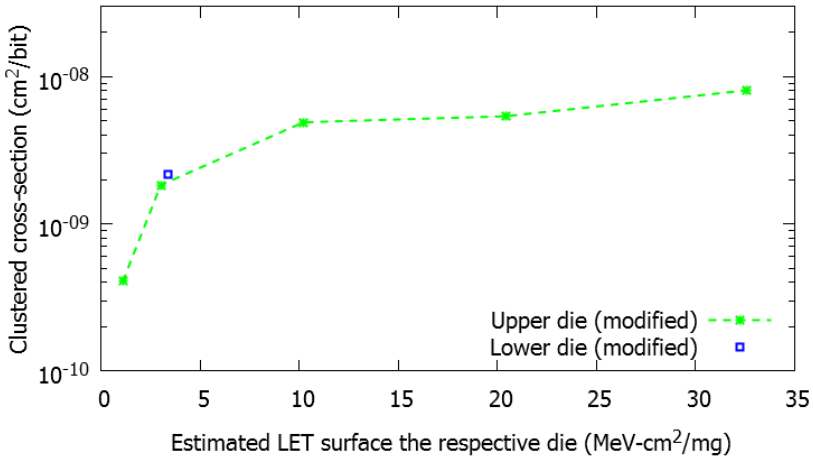


Figure 40: Heavy-ion SEU cluster cross-section of the SRAM under static test for the estimated LET at the surface of the respective dies. It can be noted that the lower die SEU cross-section point fits the upper die SEU cross-section. All errors have a 1σ standard deviation below 13% and are not plotted for clarity reasons (errors bars having similar size to the dots).

In order to confirm this result based solely on the experimental data, the SEU cross-section under static tests of the lower layer for carbon ions (which was estimated to reach a LET at the surface of the lower layer around 3.3 MeV.cm²/mg) and the SEU cross-section during static tests of the upper layer for nitrogen and neon ions (reaching a LET at the surface of the upper layer respectively at 3.3 and 3 MeV.cm²/mg) were compared.

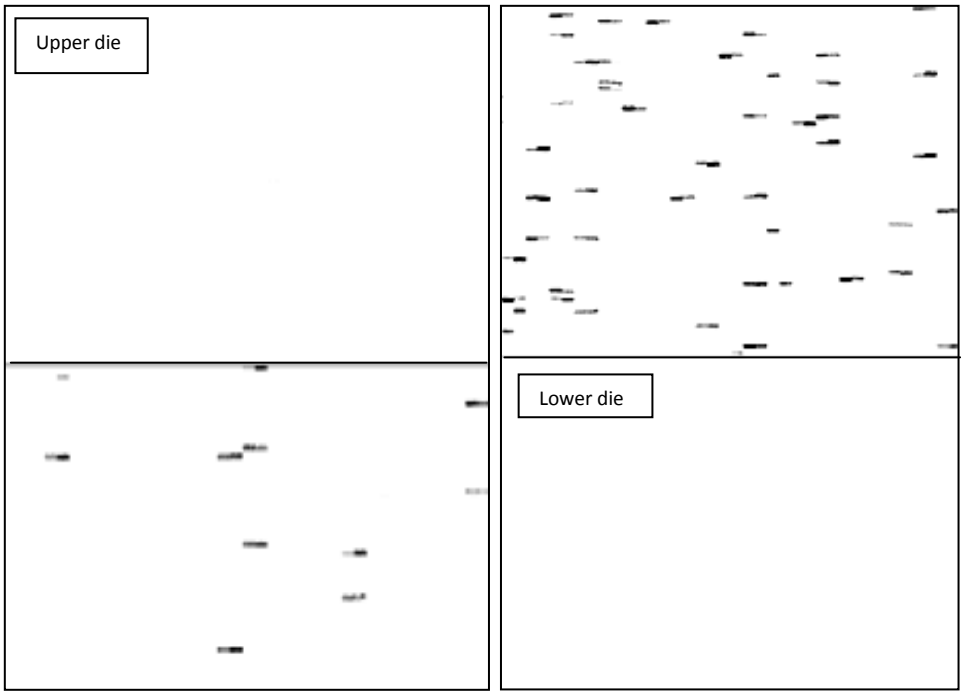


Figure 41: Physical bitmaps of the memory for carbon ion (left) and neon ion (right). On the left picture, the top die is solely affected by SEUs while there are SEUs and MCUs on the bottom die. On the right picture, the top die is affected by SEUs and MCUs while the bottom die is not affected by any SEUs nor MCUs. Note: The size of the picture does not allow to clearly see SEUs.

The analysis of the bitmaps revealed that errors on the lower die are also affected by large-scale events similarly to the upper die. These soft errors are caused by Single Event Functional Interrupts (SEFIs) and micro-latchups [Tsiligiannis3, 2014]. An in-house built clustering technique [Tsiligiannis4, 2014] was used to obtain a precise event SEU cross-section based on the actual number of occurring events

rather than on the raw count of the number of flipped bits, which can considerably vary. Figure 41 shows two physical bitmaps of memories showing similar types of clusters on the top and bottom dies. The leftmost image shows clustered events occurring on the lower die due to the highly penetrating carbon ion whereas the rightmost image shows similar types of cluster events occurring on the upper die at the same LET with an ion not able to penetrate enough to generate upsets in the lower die.

For the purpose of comparing the cross-section of both dies due to different ions having the same LET at the die surface, two specific test runs were performed and the results are summarized in the graph of Figure 42. The event SEU cross-section shown in the graph is obtained by applying the clustering technique mentioned above (all bit flips belonging to the same particle interaction counts as one event). The good matching of results in terms of SEU cross-section (total and event) between the upper and lower dice proves that the previous assumption (used to estimate the LET of 3.3 MeV.cm²/mg on the sensible area of the lower die) is correct.

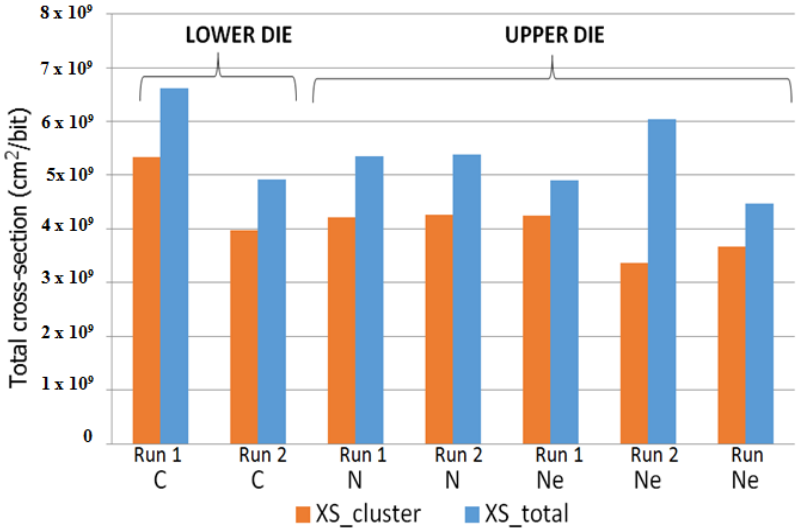


Figure 42: Total and event SEU cross-sections (XS) for various runs: results for carbon (C) are calculated for the lower layer (surface LET ~ 3.3 MeV.cm²/mg, results for nitrogen (N) and neon (Ne) are calculated for the upper die with surface LET respectively of 3.3 and 3 MeV.cm²/mg.

Assuming that the internal structure was unknown, the cross-section of the memory would be as depicted in red in Figure 43, compared to the upper die cross-section in green. The high cross-section at the lowest LET, which may seem counter-intuitive, is solely due to the stacked nature of this memory: the carbon ion's LET profile is here able to generate lower number of errors on the upper die (lower LET at upper die surface) and higher number of errors on the lower die (higher LET at the lower die surface).

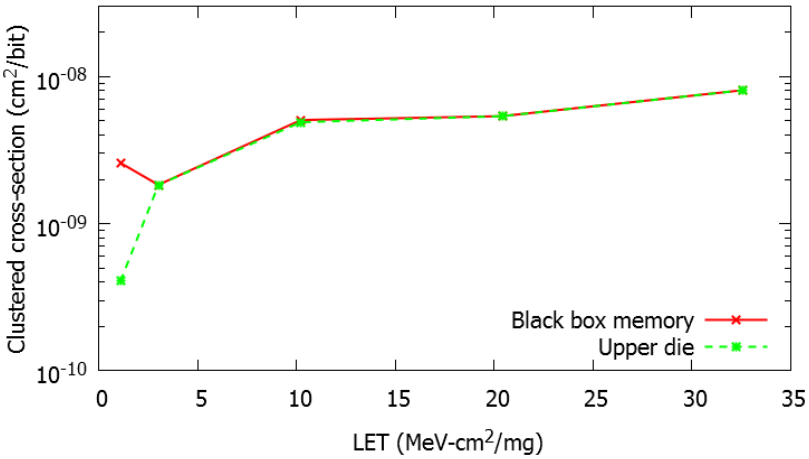


Figure 43: Heavy-ion SEU cluster cross-section of the SRAM under static test considering the memory as a "black-box" and solely considering the upper die.

3.3.1.4 Impact of stacked dies on the in-orbit SEE

Regarding the impact of the 90 nm SRAM being a stacked die component, none of the facilities used had enough energetic heavy-ion particles able to penetrate down to the lower die. For the estimation of the error rate that will be presented in chapter 6, it will be assumed that the cross-section will be twice the upper die cross-section, assuming hence that all particles which are able to penetrate the upper die will have enough energy to penetrate the lower die. This assumption is valid for highly energetic particles which is mostly the case for heavy-ions originating from GCR.

3.3.1.5 65 nm SRAM test results

Similarly to the 90 nm SRAM, the 65 nm SRAM's address scrambling scheme was made available by the producer, which allowed to correctly identify clusters of bit flips (MCUs). In order to compare the response of the 90 nm with the 65 nm, the same tests in dynamic and static modes are selected and experimental results from various test campaigns are presented in Figure 44 and Figure 45 for heavy-ions. The cross-section values are given per bit or event (cluster) and for each ion, the LET mentioned is the LET at which it reaches the DUT surface ("LET at surface").

Comparing the two static bit cross-sections of the two SRAM memories, they appear to be very similar; nevertheless, after clustering the events, the event cross-section of the 90 nm appears to be higher than the 65 nm. Hence, although both memories seem to have similar soft error sensitivity to heavy-ions, the 65 nm SRAM is more robust to impinging particles although an impinging particle induces higher multiple MCUs very likely due to charge sharing [Amusan, 2006]. Charge sharing occurs more likely in highly integrated technologies, due to the combination of a reduced amount of critical charge (mainly due to reduced supply voltage and node capacitance) and the reduced spacing between transistors both of which increase the likelihood of some of the induced charge generated by a single particle hitting a transistor to be collected by one or several neighbouring transistors through diffusion in the substrate or in the well.

In static mode testing, as for the 90 nm SRAM, no dependency on the pattern was observed.

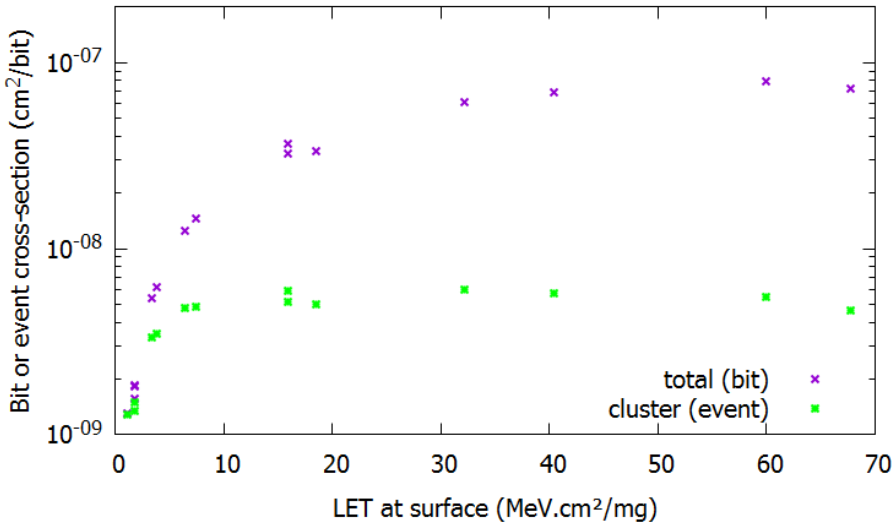


Figure 44: 65nm SRAM static total and event heavy-ion cross-section per bit.

The 65 nm SRAM was also thoroughly tested in dynamic mode and showed a higher SEE robustness. This is very likely due to a smart powering scheme where only specific blocks are powered at nominal voltage when accessing memory cells, while the remaining blocks stay at a low standby voltage, resulting in reduced power consumption and at the same time limiting the size of micro-latchups

[Tsiligiannis4, 2014]. Additionnally, the well tap scheme also plays an important role in the spatial limitation of micro-latchups.

No large-scale clusters of event occurred during dynamic (or static) mode testing which shows the efficiency of the mitigation technics employed in this memory. Clusters of size between 11 and 20 bits, started occurring at a LET of 15.9 MeV.cm²/mg in static mode, and 26.2 MeV.cm²/mg in dynamic mode. The largest cluster size on this memory was of a size between 21 and 50 bits, which started occurring with values of LET above 26.2 MeV.cm²/mg in static mode, at 32.1 MeV.cm²/mg (occurring once) and at 60 MeV.cm²/mg.

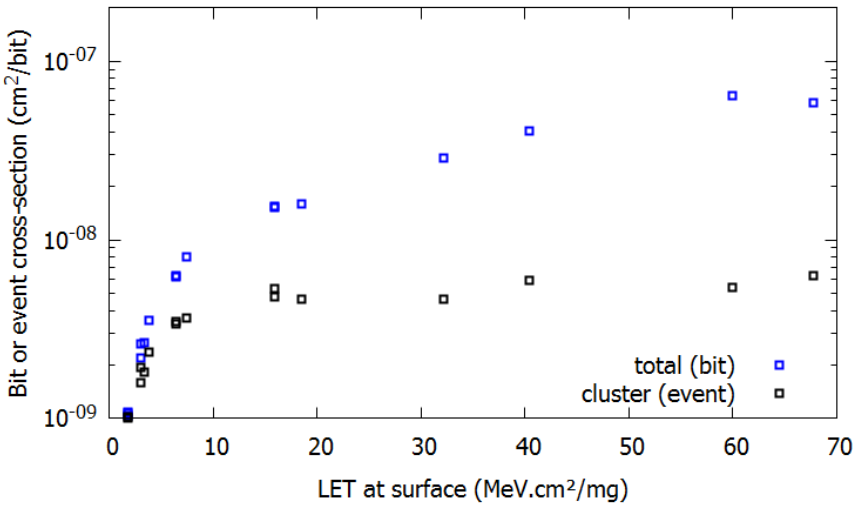


Figure 45: 65nm SRAM March Dynamic Stress total and event heavy-ion cross-section per bit.

Furthermore, this memory has an internal built-in ECC controller. During all test campaigns the ECC was deactivated, as it will be during the RES experiment in-orbit. Nevertheless, during the first test campaign, the ECC was turned successively OFF then ON during irradiation with the Fe heavy-ion in order to compare the response of the memory with and without ECC. The following table summarizes the number of total bit upsets (SEU total) and the total number of events (SEU events). In static mode, most of the bits are corrected but some remain (51 in the case of Static "0000"). Hencen as the ECC algorithm is based on parity bits, the non-corrected bits very likely originate from MBUs. In Dynamic mode the ECC is able to correct all the bits as the errors are not accumulating like in static mode. The ECC allows reducing the cross section by one to two orders in magnitude in the worse case (Table 9 and Figure 46). In dynamic mode, the memory appears to be very robust. In the frame of the RES Experiment, the ECC will nevertheless be deactivated to maximize the detection of soft errors.

Type of test		**ECC OFF**			**ECC ON**		
		SEU total	**SEU events**	**Cross section (cm²/bit)**	**SEU total**	**ECC corrected**	**Cross section (cm²/bit)**
Static	« 0000 »	5940	939	3.22×10^{-8}	51	6232	3.01×10^{-10}
Static	« 1111 »	5216	785	3.02×10^{-8}	192	6336	1.13×10^{-9}
Static	« 0101 »	6076	922	3.32×10^{-8}	26	6164	1.52×10^{-10}
Dynamic	Stress	3085	800	1.72×10^{-8}	0	3078	0
Dynamic	C- normal	2215	649	1.27×10^{-8}	0	4356	0
Dynamic	C- normal	2542	690	1.47×10^{-8}	1	4197	5.84×10^{-12}
Dynamic	C- fast row	2375	663	1.36×10^{-8}	0	5607	0
Dynamic	Stress fast row	-	-	-	0	3117	0

Table 9: Total number of SEU and total number of clusters (or events) for different static and dynamic tests on the 65nm SRAM tested against Fe ion (LET = 19 MeV.cm2/mg) and to a target fluence of 10 000 part/cm². Note: Dynamic C- normal scrambling has been run twice with good repeatability in ECC ON and OFF modes.

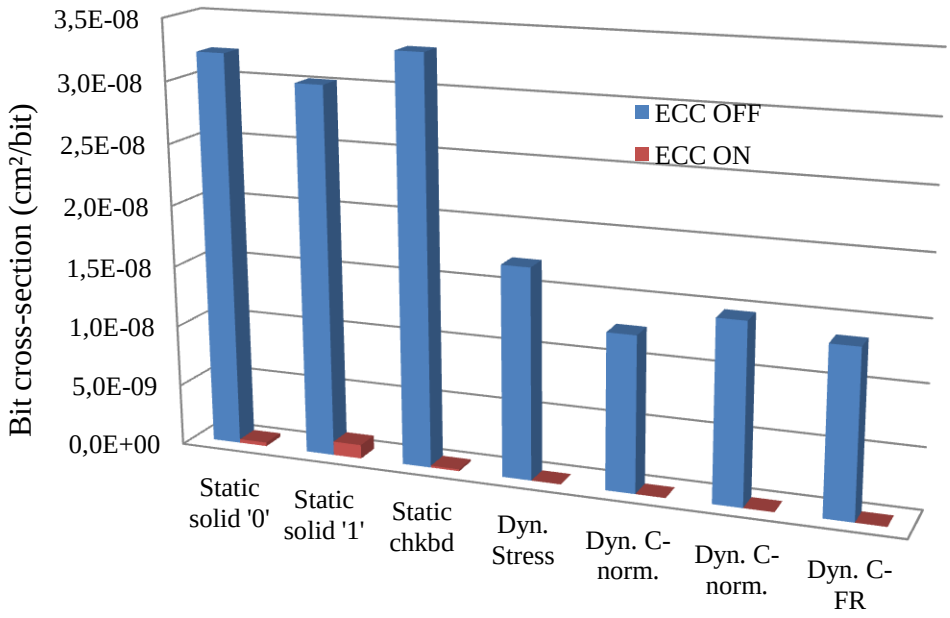


Figure 46: 65nm SRAM total cross-section with and without ECC tested against Fe ion (LET = 19 MeV.cm2/mg) and to a target fluence of 10 000 part/cm².

3.3.2 Low and high energy protons results

3.3.2.1 65 nm SRAM test results

Figure 47 presents the results based on proton testing of the 65 nm SRAM over a wide energy spectrum. Results summarise the Low Energy Proton (LEP, ≤ 50 MeV) and High Energy Proton (HEP, ≥ 50 MeV) testing performed at two different test facilities. Both set of results seem to agree very well at 50 MeV in static and dynamic mode.

The cross-section remains relatively flat throughout the proton energy spectrum for both performed static and dynamic tests. However, at very low energies (< 2 MeV), the memory's cross-section is much higher in static and dynamic mode. Theses high cross-section values are due to direct ionization of low energy protons first reported in [Rodbell, 2007]. In [Pellish, 2010] and references therein, it is mentioned that technologies below and including 90 nm have shown sensitivity to LEP. In [Sierawski, 2009], a 65 nm Bulk CMOS SRAM showed an increase of its cross-section (very likely in static mode although it is not mentioned in the paper) of about four orders of magnitude between proton energy from 100 MeV to 1 MeV due to proton direct ionization. For the currently studied memory, the increase is slightly more than three orders of magnitude higher at 1 MeV with respect to the cross-section at 100 MeV in static mode. In dynamic mode, the increase is smaller, about two orders of magnitude.

Low energy protons can reach a maximum LET of about 0.5 MeV.cm²/mg in silicon, and hence, are able to trigger upsets if the LET threshold is equal of lower to ~0.5 MeV.cm²/mg and of course, only if it occurs near the sensitive area [Sierawski, 2009]. Although it may be considered that direct ionization will induce mainly SBUs as inelastic collision is not very likely [Heidel, 2009], as depicted in Figure 48, the number of 2-bit clusters is very high at 0.98 MeV compared to 0.6 and 2.2 MeV and the proportion of bigger size clusters, although very small, is higher than for slightly lower and higher values. Besides, the proportion of 2-bit clusters is higher than for the lowest LET at which the memory was tested.

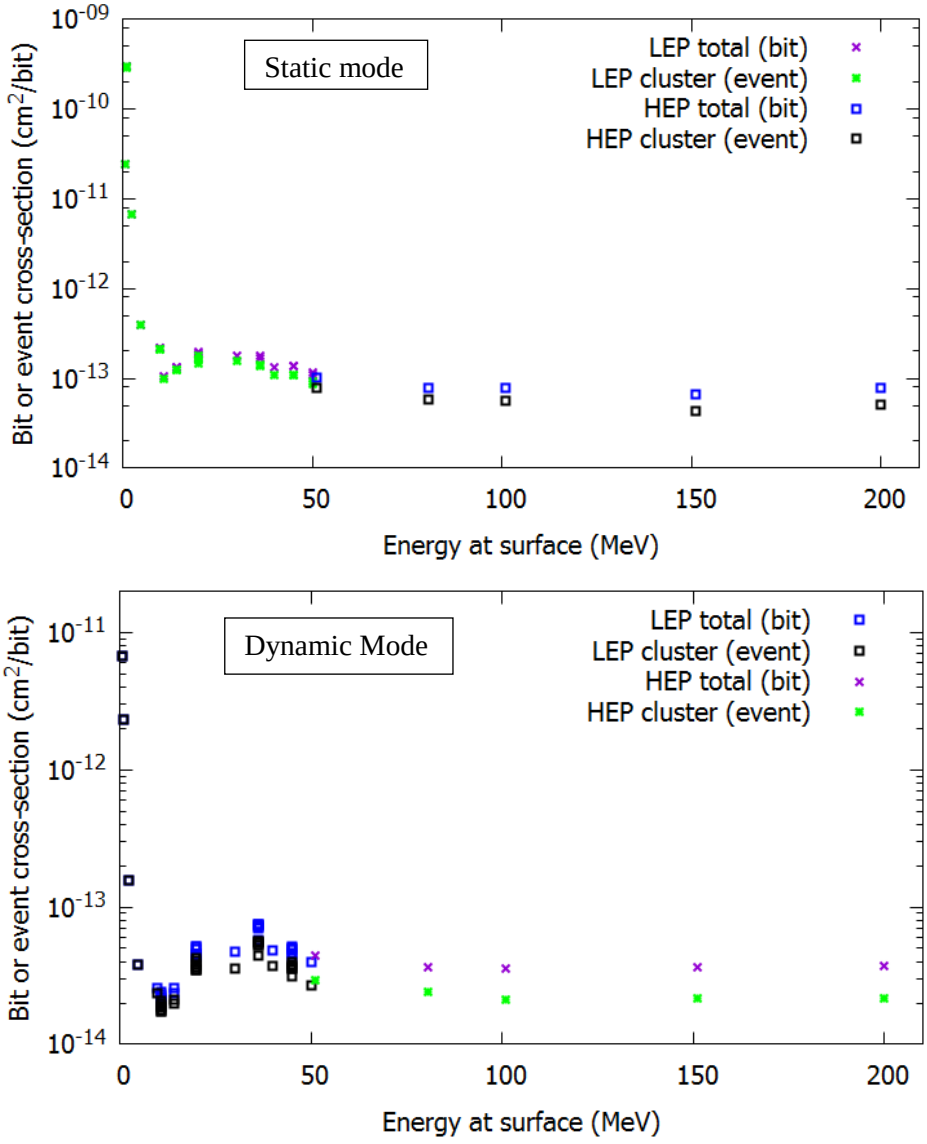


Figure 47: 65 nm top die SRAM static low and high energy proton total and event cross-section per bit (top), March Dynamic Stress total and event cross-section per bit (bottom).

It appears unexpected for protons, even at their maximum LET through direct ionization interaction, to generate more small-sized MCUs than light heavy-ions having a higher LET at the tested energies. In [Kosmata, 2011], it is mentioned that protons, able to have a $LET \geq LET_{th} = 0.3\ MeV.cm^2/mg$ for a 32 nm SRAM, only have a limited energy range between 9 to 400 keV. According to the same authors, knowing that the Coulomb barrier energy in silicon for protons is equal to 4.2 MeV above which inelastic nuclear interaction start occurring, protons with energy between 400 keV and 4.2 MeV interact by elastic backscattering interactions which results in a wide range of angular values at which a proton particle crosses a sensitive volume (or SV, is the volume in which a particle passing through will generate a soft error, if enough energy is deposited within), which may increase the chances of generating MCUs. At the present time, the mechanisms inducing MCUs at low proton energies is not very well understood as recognised in [Dodds, 2015] in which is it experimentally confirmed that the mechanisms inducing SBUs is clearly direct ionization contrary to what is suggested in [Kosmata, 2011]. However, again in [Dodds, 2015], it is mentioned that angular scattering is high at low energies especially when the particle is passing through large depth of matter before reaching the SV, which may hence result in higher number of small-size clusters.

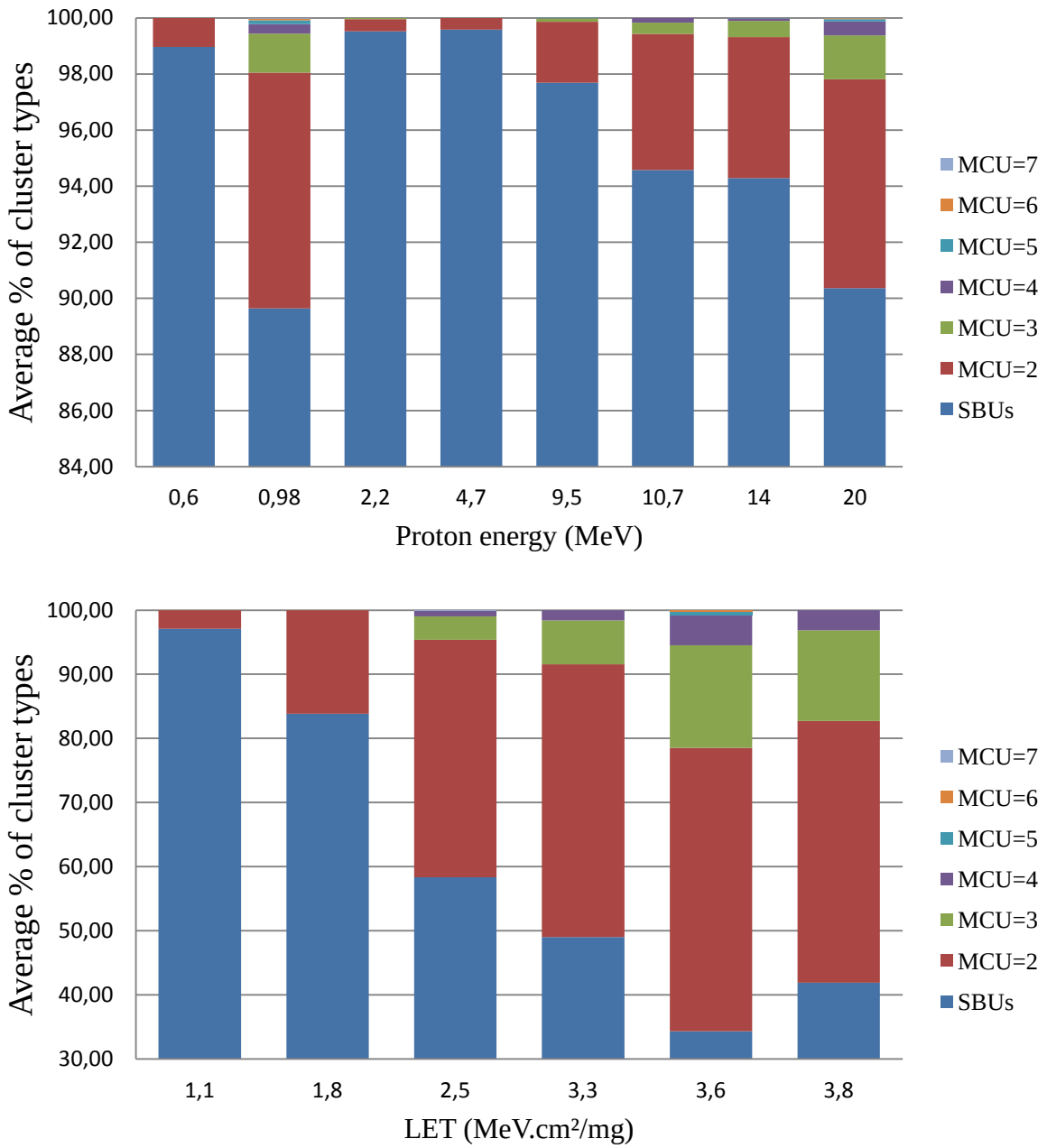


Figure 48: 65nm SRAM average % of clusters of difference size w.r.t total number of clusters for different proton energies (top) and different low LET values (bottom) in static mode. Below 84% (top)/30% (bottom), only SBUs were present and hence they are not shown for clarity.

Properly understanding the LEP mechanisms is difficult. In [Dodds, 2015] are listed the main issues having a large impact on the test results from LEP irradiation:

- energy straggling is high (besides energy degradation) which has a major variability effect on the LET of the particle at those energies reaching the SV through all the BEOL layers;
- flux attrition: which is the results of a reduced flux able to reach the SV due to the low range of those particles at these low energies;
- finally, angular scattering of protons is also high, increasing as the energy reduces. The angular scattering also affects the energy loss, energy straggles, and flux attrition of the particles reaching the SV, but this occurs at very low energies (few tens of keV) and depends on the materials crossed by the particles before hitting the SV.

Looking more closely at the bitmaps, it first appears that similarly to heavy-ion test results, no large clusters occur. The LET is not sufficient to trigger micro-latchups resulting in bitmaps with randomly distributed SBUs and small clusters. In fact, most of the clusters were smaller than 10 bits of size, at all proton energies, the proportion of SBU was larger than 65 (dynamic) -70 (static) % of the total number of clusters (counting a SBUs as a 1-bit cluster). Below 10.7 MeV, more than 90% are SBUs. The ratio of words with occurring MBU w.r.t to words in error is very low: the worse case ratio amounts for 0.35% of words being in MBU. At 0.98 MeV, this percentage doubles to 0.61% but still remains small.

The fact that the dynamic test mode cross-section, especially at very low proton energies, is higher compared to the static mode cross-section is explained in [Tsiligiannis, 2014]: the 65 nm SRAM, has a low power scheme in static mode (to prevent latch-up occurrences) where all the memory plan is set at low voltage , this may increase the sensitivity of the memory as the inverter loop is more prone to switch its state due to parasitic charges.

3.3.2.2 90nm SRAM test results for the top layer

Similarly, in Figure 49 are presented the 90 nm SRAM responses in static and dynamic modes to proton irradiation ranging from 0.6 MeV to 200 MeV. It can be noticed that although the static mode cross-section between LEP and HEP seems to agree well at 50 MeV, it is not the case for the total cross-section in dynamic mode, although the event cross-section, calculated after clustering the flipped bits, perfectly matches at 50 MeV ensuring that the data is consistent.

Artificially removing the large MCU clusters (type C and type D SEFIs) resulted in only halving the total dynamic cross-section (see chapter 1, section 1.2.1.1 for a definition of MCU). Further investigations showed that the large difference between the total and cluster cross-sections is in fact due to micro-latch-ups (type B clusters). Hence, the reason for this discrepancy is that the device used for testing at high proton energies is more sensitive to micro-latchups. However, when analysing more in depth the cross-section of the various types of clusters as presented in Figure 50, it can be seen that the micro-latchup cross-section is consistent between the two devices. These results shows that, the device's response to high energy protons inducing an increase in the total number of bits flips is not due to a higher number of micro-latchups but a higher number of flipped bits per micro-latchup. This may either be due to the device itself, or due to TID effects (tests were performed from 200 MeV down to 50 MeV reaching 1 krad based on measurements provided by the facility) although the level is rather small.

Furthermore, in Figure 49 it appears that in dynamic mode the total cross-section is much higher at 9.5 MeV than expected, whereas in static mode this trend does not appear; this higher cross-section is also visible in Figure 50. Based again on the analysis of the clusters, it appears that this peak on the total cross-section, is mainly due to an increase in the number of micro-latchups, as well as a minor increase in the number of SBU and/or small clusters. This small increase can be explained looking at the physical bitmap as presented in Figure 51: the higher number of small clusters is in fact due to micro-latchups bein not fully developed. However, the reason why at this energy the number of micro-latch-ups suddenly increases remains yet unknown. Again, during the LEP irradiation campaign, the device was last tested at 9.5 MeV (going from 50 MeV down to 9.5 MeV on one device) resulting in a device having accumulated a certain amount of TID. However, first the exact dose level accumulated by the device was not logged. Furthermore, going from 50 MeV down to 9.5 MeV (testing order) the cross-section does not seem to be directly impacted by TID as the cross-section is reducing until the sudden rise at 9.5 MeV. It may be interesting to pursue, in the future, some TID testing on this memory in order to understand its behaviour against TID as well as understand whether this memory is greatly affected by synergetic effects (increased effects of SEE due to TID).

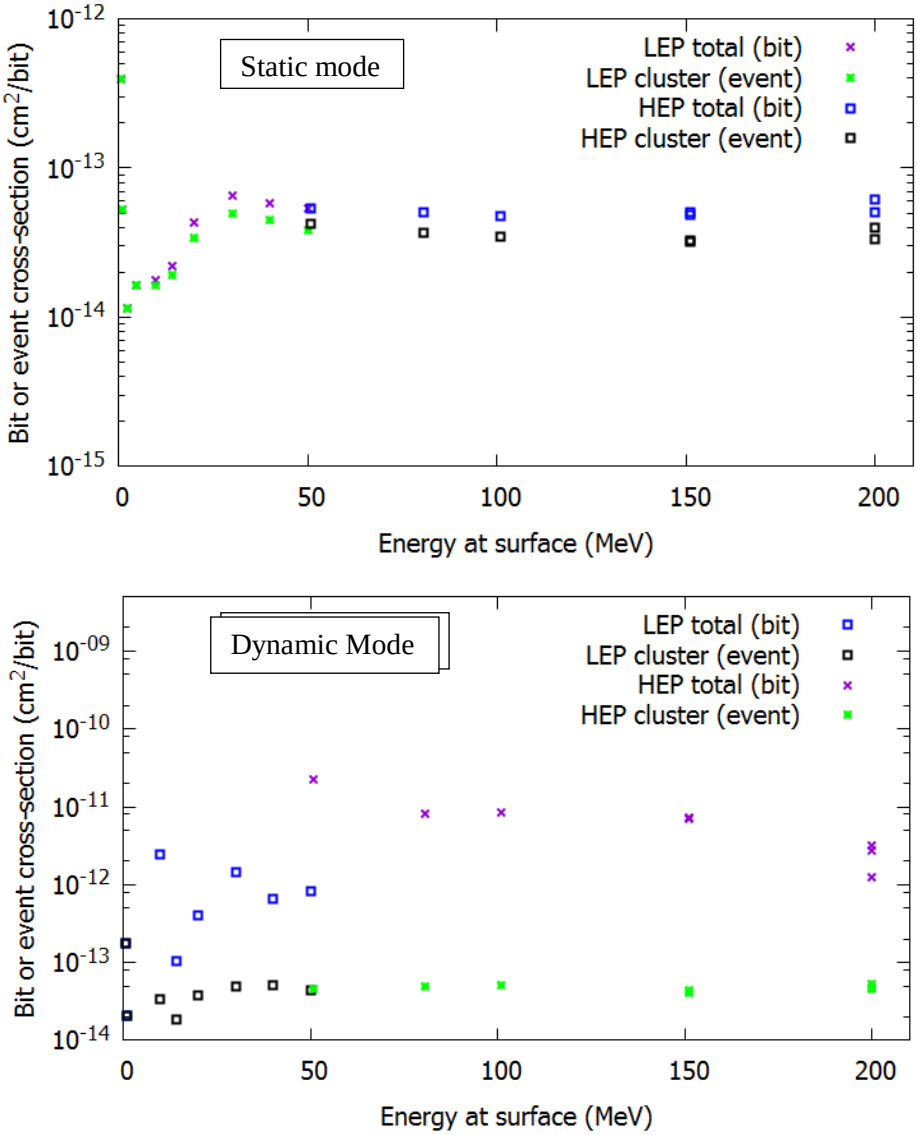


Figure 49: Average 90 nm top die SRAM static low and high energy proton total and event cross-section per bit (top), March Dynamic Stress total and event cross-section per bit (bottom). Contrary to the 65nm, only the average cross-section for each energy is shown as the variation of the total cross-section is non-negligible.

A last word on Figure 50: the various types of clusters seem to appear at different energy thresholds: micro-latchups start appearing at between 4.7 and 9.5 MeV; type D SEFIs appear between 20-30 MeV; and type C SEFIs appear between 40-51 MeV. However, more statistical data may be required in order to confirm these results as the number of large SEFIs is very small and the resulting uncertainty is large (although not presented here in order to avoid overcrowding Figure 50).

Regarding very low proton energies, similarly to the more integrated 65 nm, the 90 nm SRAM experiences direct ionization from protons although the highest cross-section at 0.6 MeV is only about one order of magnitude higher compared to the cross-section at 50 MeV in static mode. When looking at Figure 52, contrary to the 65 nm, the types of errors of the 90 nm remain SBUs. Larger size MCUs appear at higher energies between 5 and 9 MeV.

The 90 nm SRAM static total and cluster cross-sections are lower than the 65 nm (between 0.5 to 4 orders of magnitude at 1 MeV): this is actually the result of the higher critical charge of the 90 nm compared to the 65 nm. However, although the static cross-section of the 65 nm was higher than its dynamic cross-section, for the 90 nm the cluster static and dynamic cross-sections are in the same

range (about 5x 10^{-14} cm²/bit). The dynamic total cross-section is about two orders of magnitude higher than the cluster cross-section mainly due to micro-latchups as previously discussed.

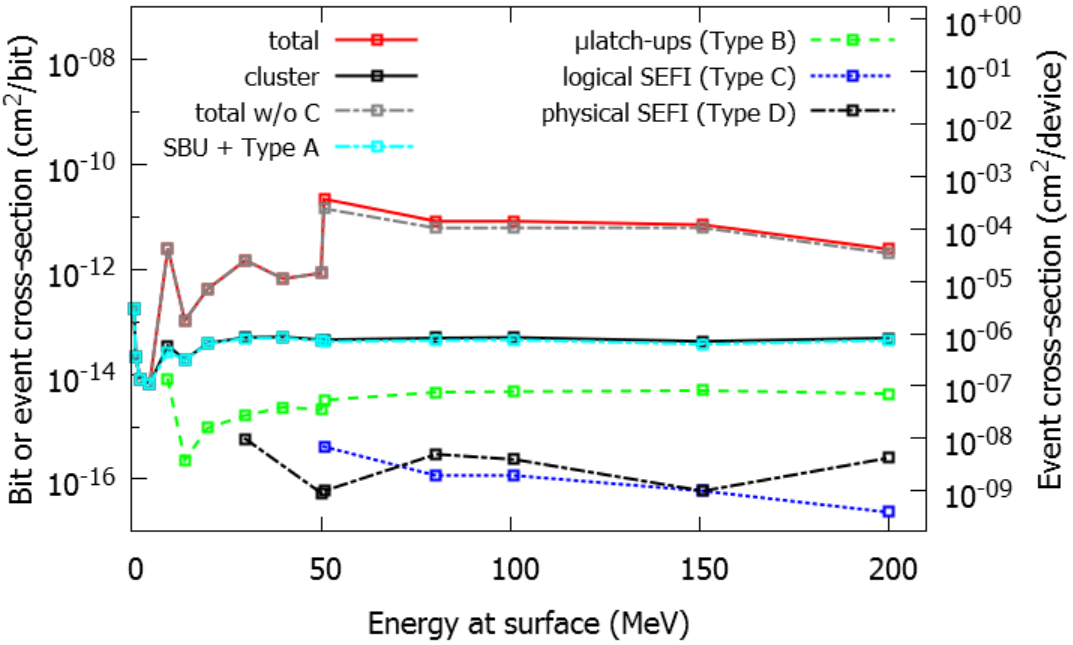


Figure 50: Dynamic mode 90nm SRAM cross-sections under high and low proton irradiation based on the cluster classification introduced in [Tsiligiannis4, 2014]. Logical and physical SEFI cross-sections are given in cm²/device, the remaining cross-sections are given in cm²/bit.

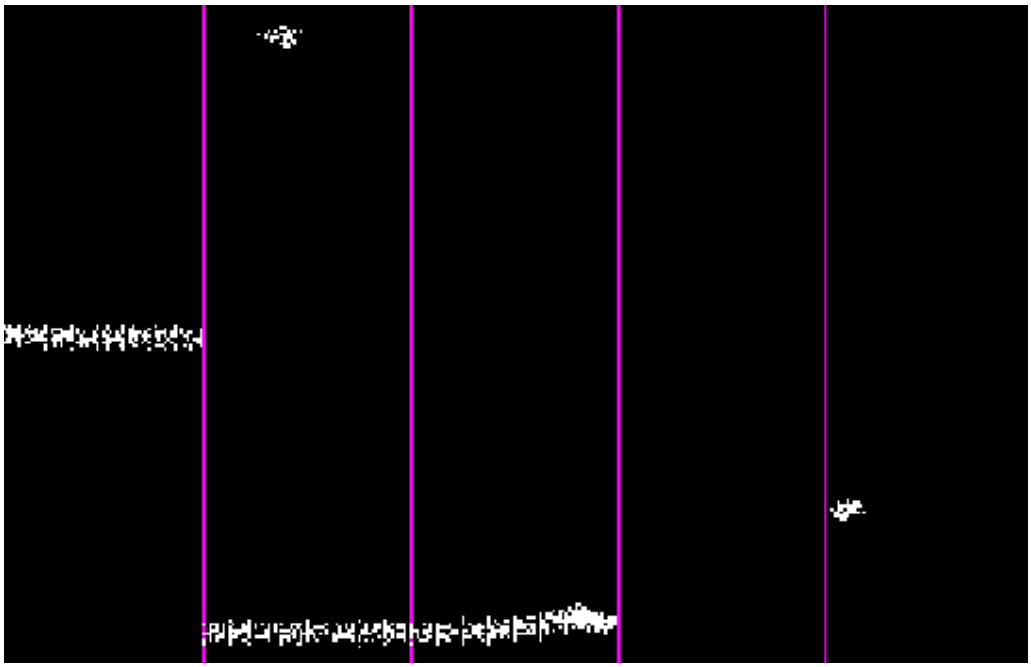


Figure 51: Partial physical bitmap of the 90nm SRAM under proton irradiation at 9.5 MeV. The picture has been modified to regroup more closely the shown clusters for display purposes. The large long clusters are micro-latchup [Tsiligiannis4, 2014], the small clusters appear to be none fully developed micro-latchups. The pink lines represent the well-taps in the memory.

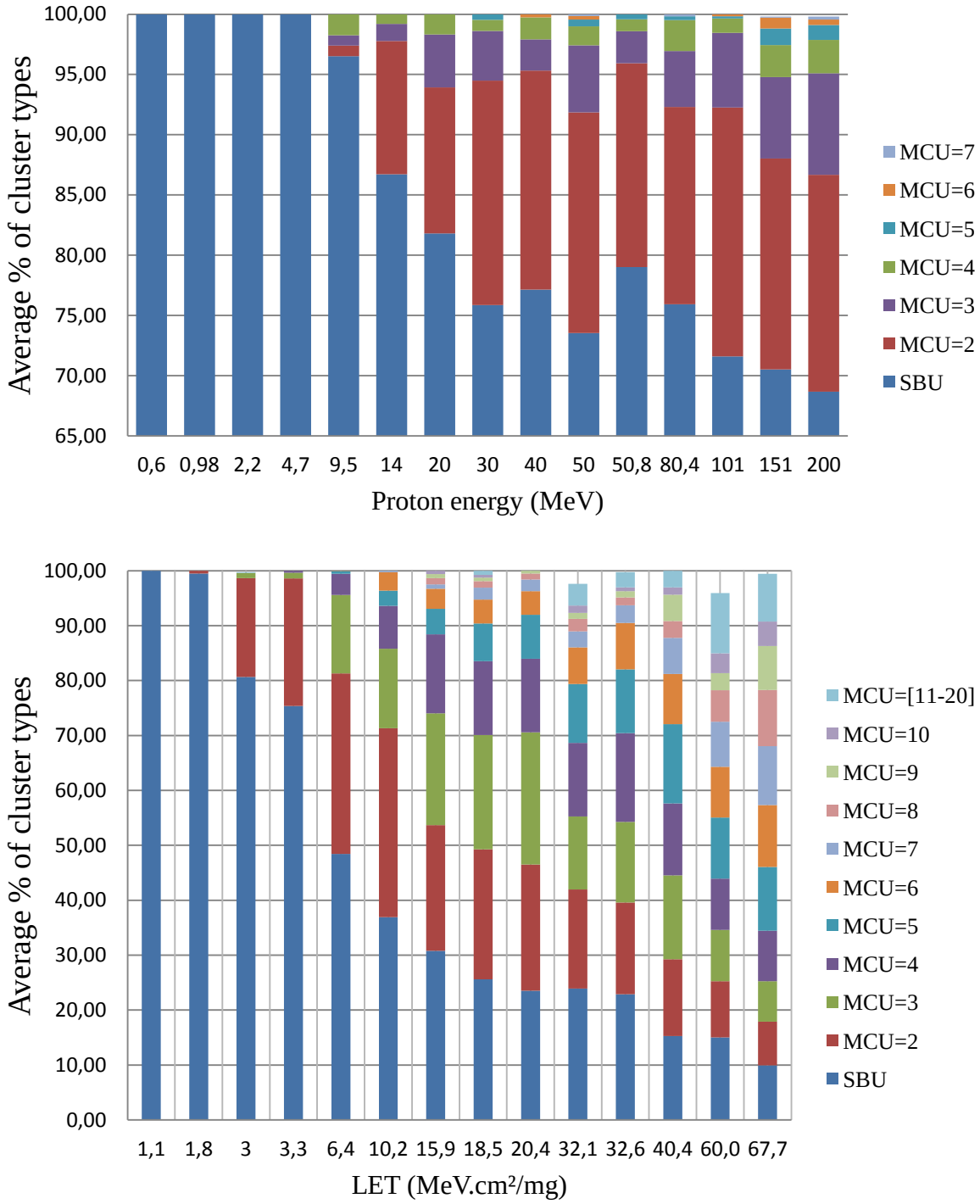


Figure 52: 90nm SRAM average % of clusters of difference size w.r.t total number of clusters for different proton energies (top) and different low LET values (bottom) in static mode. Below 65% (top) only SBUs were present and hence they are not shown for clarity. Some columns do not reach 100% as this remaining part includes the remaining clusters which are not shown (MCU size above 20 bits and larger SEFIs).

Regarding MBUs, results are summarised in Table 10. As it can be seen, proton tests result in a small percentage of MBU and their occurrence is higher in dynamic mode. These values are much higher than for the 65 nm SRAM. The maximum occurrence of MBU slightly decreases only when considering the runs without SEFIs but drastically reduces when considering the few runs without SEFIs nor micro-latchups. This allows saying that the biggest contributors to MBUs occurrence are micro-latchups.

	Worse case	Worse case due to SEFIs	Worse case due to µSELs	Worse case w/o SEFI and µSEL
Proton static	0.33%	-	-	-
Proton dyn.	83.0 %	16 %	58.0 %	9.0 %
HI static	30.0 %	-	-	-
HI dyn.	95.0 %	2 %	92.4 %	0.6 %

Table 10: Summary of the maximum contribution of SEFIs and µSELs (micro-latchups) on the percentage of words having MBU w.r.t total number of corrupted words for the various proton and heavy-ion irradiation in static and dynamic mode for the 90 nm SRAM. Percentage recorded for all runs regardless of the LET or energy.

3.3.2.3 90 nm SRAM double layer considerations

Low energy proton tests produced similar results as can be seen on Figure 53. Considering the top memory (blue curve), the peak at the lowest energies (600 keV) is due to the direct ionization process of the protons at those low energies at discussed previously. Nevertheless, the second peak on the lower die, around 9.5 MeV, is not usual for a typical SRAM memory cross-section.

The explanation may appear to be that direct ionization interactions are occurring around this energy on the lower die. When considering the types of errors, 99.85% of the errors were SBUs homogeneously distributed on the die, 0.15% were 2-bit clusters and no higher size clusters were detected. On the upper die, up to an energy of 4.7 MeV, 100 % of the errors are SBU. However, at 9.5 MeV, 96.52% are SBU and 0.87% are 2-bit, 0.87% are 3-bit and 1.74% are 4-bit clusters.

An attempt was made in order to simulate the stack structure of the memory and to try to reproduce the experimental results. However, preliminary results presented in Figure 54 were not successful to show that the LET reaching the lower die was near the proton's Bragg peak in silicon or due to other low LET ion recoils generated by the protons in the spacer. The simulation showed, based on information regarding the internal layer and structure provided by the manufacturer (none disclosable however), that the direct ionization peak should occur on the lower die at energies around 6 MeV. In order to assume that the peak was near the one noted during the experiment required the spacer density to be increased by about 3 times which appears very unlikely. More experimental results, especially at very low energies (< 2 MeV) and around the direct ionization peak occurring on the lower die (between 4.7 and 9.5 MeV) are required to better calibrate and model the stacked layer properly. It is believed that the observed peak on the lower die is also likely impacted by the energy straggling due to the crossed material as well as the initial beam energy distribution. Further analysis is required on this aspect.

Regarding the very low lower-die cross-section at 4.7 MeV, it represents one SBU located on the lower die. The range of proton at 4.7 MeV (194.5 µm in silicon) is less than the approximate 250 µm distance between the two dies, even when including the longitudinal straggling (8.20 µm in silicon). The spread in energy of the mono-energetic beam does not seem sufficient (< 10%) to explain this. Investigating further, a quick simulation was performed including a layer of epoxy (lower *Z* than silicon) between the two dies, which is a piece of information provided by the manufacturer. SRIM simulation provided a range of 238 µm with a straggling of 2.76 µm. Assuming that in our case the straggling was a little bit greater (or the range, as previous values are mean values), this could explain why in one particular case, a proton might have been able to penetrate the lower die. Possibly other reasons might exist but the above explanation seems the most likely reason.

Furthermore, for energies above 14 MeV, both dies event and total SEU cross-sections have similar values, showing that the sensitivity of both dies is similar at energies above 14 MeV.

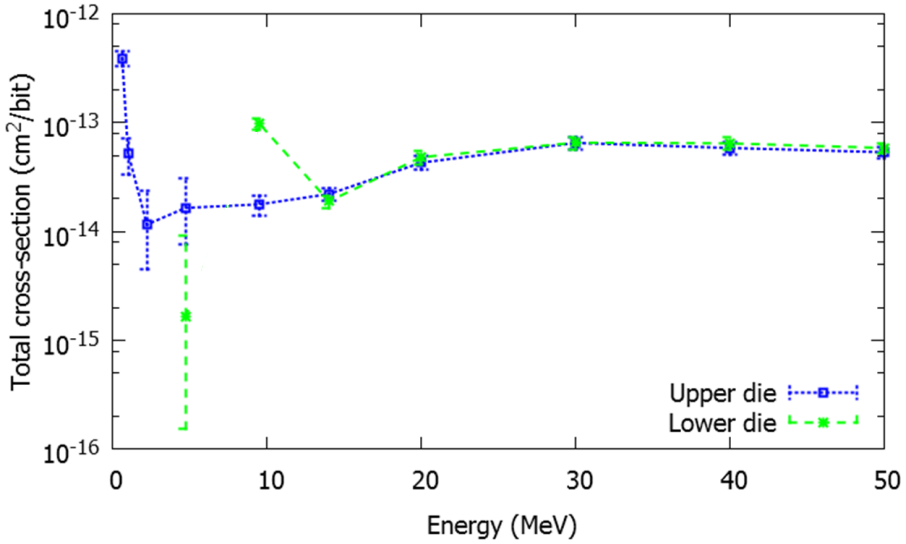


Figure 53: SRAM total cross-section under proton irradiation with static test calculated while considering the upper and lower die separately. 2σ error bars are shown: normal distribution is used for number of errors higher than 20 upsets and Poisson distribution for the number of errors lower than 20 upsets (essentially for 2.2 and 4.7 MeV).

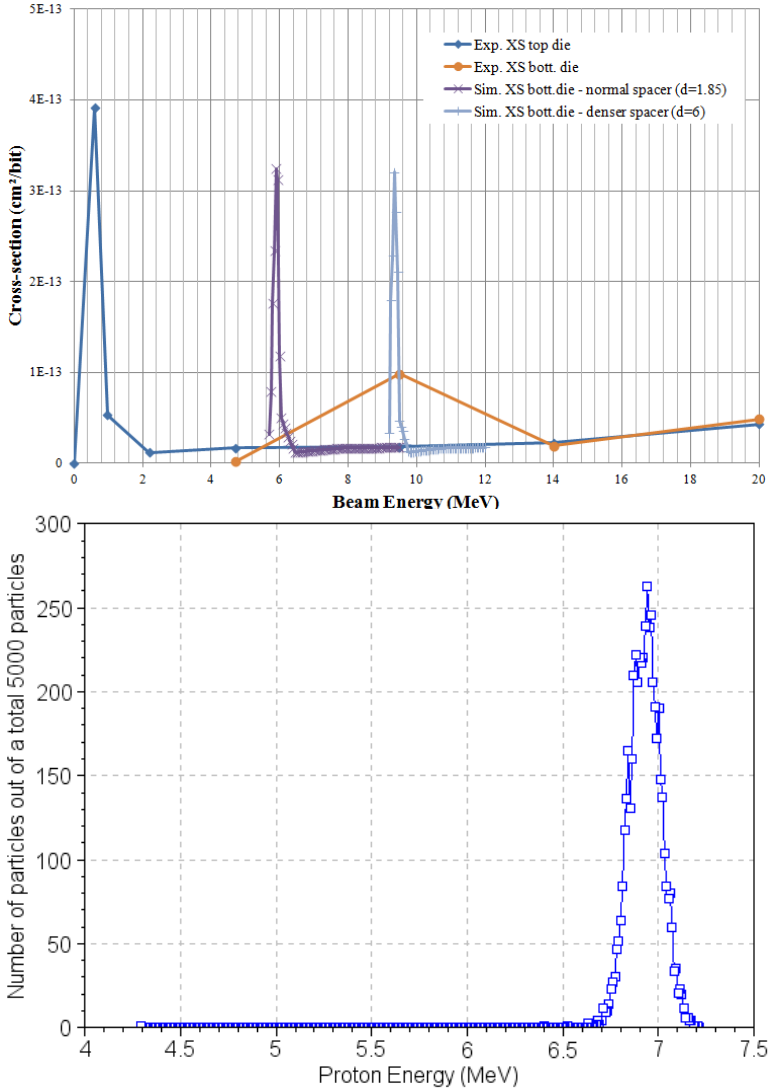


Figure 54: Results from SRIM simulation on the stacked-die 90 nm SRAM: (top) experimental and simulation cross-section of the top and bottom die; (bottom) energy of particles reaching the lower die for a 9.5 MeV mono-energetic beam, the mean energy reaching the lower die is 6.9 MeV.

3.3.1.6 Impact of stacked dies on the in-orbit SEE

Based on the static SEU cross-section obtained during proton testing, the impact of stacked-die structures is investigated on the SEE event rate. For this calculation, a Low Earth Orbit (LEO) was considered at an altitude of 630 km and an inclination of 98° as a case study. The proton radiation environment model used was AP8 min [Sawyer, 1976] for trapped protons and ESP [Xapsos, 2010] for solar generated protons. Protons originating from Galactic Cosmic Rays were not considered. Simulations of the radiation environment were made using the OMERE software [OMERE]. The environment was transported through a radiation shielding of 3.7 mm of aluminium simulating the equivalent material to be crossed by external particles to reach the upper memory die (i.e. external satellite shielding and plastic material of the component's packaging). In this part of the study, the results of the current dual-die SRAM were compared to an equivalent SRAM having the same die sensitivity (i.e SEU cross-section) and storage capacity of the studied SRAM but having a single-layer structure. Results are presented in Table 11.

Memory configuration	Proton SEE rate (/s/bit)
Stacked layer	5.36×10^{-12}
Single layer	5.12×10^{-12}

Table 11: Proton SEU rate at 630 km of altitude and an inclination orbit of 98° for a stacked layer and single layer memory.

The analysis of the results shows that the stacked memory undergoes an SEE rate increase of approximately 4.5% compared to an equivalent single layer memory.

3.4 Conclusion

In this chapter, the basic operations of SRAM memories have been reviewed. Radiation effects on SRAM memories have also been presented: SRAM memories are sensitive to SEE but also to TID. Other parameters such as temperature, core voltage and scaling have a direct impact on the memory's SEE sensitivity.

Then heavy-ion and proton radiation test results have been presented for both memories. A focus has been given to the 90 nm SRAM, which has the particularity of being constituted of two stacked dies. High penetrating heavy-ion cocktails and protons enabled to clearly show the effect of a stacked-die configuration on the radiation response of this memory. With low-energy protons, sensitivity of a component must be carefully considered in order to assess the effects of direct ionization as this process may occur at different values of energy, corresponding to the proton Bragg peak reaching each layer. The study was completed by an analysis resulting from the clustering of the flipped bits and showed a very similar type of response on both dies as expected. Based on the experimentally calculated SEU cross-section, it was then possible to estimate the SEE rate in LEO. Considering solely protons, a negligible increase in the proton induced SEE rate is revealed for the two stacked-dies w.r.t. a single layer device (~5%). Proton and heavy-ion results have been presented and the motivation being the usefulness of clustering errors has been introduced as well.

All these results will allow estimating the expected error rate during the MTCube mission and the results will be presented in chapter 5.

3.5 Bibliography

[Amusan, 2006] O. A. Amusan *et al.*, "Charge Collection and Charge Sharing in a 130 nm CMOS Technology," in *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3253-3258, Dec. 2006.

[Baumann, 2005] R. C. Baumann, "Radiation-induced soft errors in advanced semiconductor technologies," in *IEEE Transactions on Device and Materials Reliability*, vol. 5, no. 3, pp. 305-316, Sept. 2005.

[Berger, 1996] G. Berger, G. Ryckewaert, R. Harboe-Sørensen, and L. Adams, "The heavy-ion irradiation facility at cyclone—a dedicated SEE beam line," in *Proc. IEEE Rad. Effects Data Workshop Rec.*, Jul. 1996, pp. 78–83.

[Bosser, 2016] A. Bosser, V. Gupta, A. Javanainen, G. Tsiligiannis, A. Hillier, K. Ishida, H. Puchner, F. Saigné, F. Wrobel, A. Virtanen and L. Dilillo, "Comparison of the Effects of Muon and Low-Energy Proton Irradiation on a 65 nm Low-Power SRAM," in *Conference on Radiation and Its Effects on Components and Systems, 2016*, accepted for poster.

[Cannon, 2004] E. H. Cannon, D. D. Reinhardt, M. S. Gordon and P. S. Makowenskyj, "SRAM SER in 90, 130 and 180 nm bulk and SOI technologies," *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, 2004, pp. 300-304.

[Dodds, 2015] N. A. Dodds *et al.*, "New Insights Gained on Mechanisms of Low-Energy Proton-Induced SEUs by Minimizing Energy Straggle," in *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2822-2829, Dec. 2015.

[Dilillo, 2005] Luigi Dilillo *et al.*, « Efficient March Test Procedure for Dynamic Read Destructive Fault Detection in SRAM Memories", *in Journal of Electronic Testing: Theory and Application*, 21, 551-561, Springer Science, 2005

[Dilillo, 2010] Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, Advanced Test Methods for *SRAMs: Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies*, Springer US, ISBN: 978-1-4419-0937-4.

[Ecoffet, 2011] R. Ecoffet, "In-orbit anomalies due to radiation: Lessons learnt", in *presentation ESCCON 2011*, March 2011.

[ECSS-Q-ST-60, 2013] Space Product Assurance - Commercial electrical, electronic and electromechanical (EEE) components, ECSS-Q-ST-60-13C, 21-Oct-2013.

[Felix, 2007] J. A. Felix, J. R. Schwank, M. R. Shaneyfelt, J. Baggio, P. Paillet, V. Ferlet-Cavrois, P. E. Dodd, S. Girard, and E. W. Blackmore, ―Test procedures for proton-induced single event latchup in space environments,‖ in *9th European Conference on Radiation and Its Effects on Components and Systems, 2007. RADECS 2007*, 2007, pp. 1–5.

[Ferlet-Cavrois, 2002] V. Ferlet-Cavrois *et al.*, "Characterization of the parasitic bipolar amplification in SOI technologies submitted to transient irradiation," *Radiation and Its Effects on Components and Systems, 2001, 6th European Conference on*, 2001, pp. 217-222.

[Harboe, 2005] R. Harboe-Sorensen, F. X. Guerre and A. Roseng, "Design, Testing and Calibration of a "Reference SEU Monitor" System," *Radiation and Its Effects on Components and Systems, 2005. RADECS 2005. 8th European Conference on*, Cap d'Agde, 2005, pp. B3-1-B3-7.

[Heidel, 2009] D. F. Heidel *et al*., "Single-Event Upsets and Multiple-Bit Upsets on a 45 nm SOI SRAM," in *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3499-3504, Dec. 2009.

[Kettunen, 2014] H. Kettunen, V. Ferlet-Cavrois, P. Roche, M. Rossi, A. Bosser, G. Gasiot, F.-X. Guerre, J. Jaatinen, A. Javanainen, F. Lochon, A. Virtanen, "Low Energy Protons at RADEF - Application to Advanced eSRAMs," in *Proc. IEEE Rad. Effects Data Workshop Rec.*, July 2014, pp. 1-4.

[Kosmata, 2011] M. Kosmata, J. Auerhammer, M. Zier, F. Schlaphof, F. Schreiter and J. von Borany, "Influence of proton elastic scattering on soft error generation of SRAMs," 2011 12th European Conference on Radiation and Its Effects on Components and Systems, Sevilla, 2011, pp. 186-190.

[Marinescu, 1982] M. Marinescu, ―Simple and Efficient Algorithms for Functional RAM Testing., pp. 236–239, 1982.

[Niggemeyer, 1998] D. Niggemeyer, M. Redeker, and J. Otterstedt, ―Integration of non-classical faults in standard March tests, in *International Workshop on Memory Technology, Design and Testing, 1998. Proceedings*, 1998, pp. 91–96.

[OMERE] Official OMERE website: http://www.trad.fr/OMERE-Software.html.

[Pellish, 2010] J. A. Pellish *et al*., "Heavy-Ion Testing With Iron at 1 GeV/amu," in *IEEE Transactions on Nuclear Science*, vol. 57, no. 5, pp. 2948-2954, Oct. 2010.

[Raine, 2012] M. Raine, G. Hubert, P. Paillet, M. Gaillardin and A. Bournel, "Implementing realistic heavy-ion tracks in a SEE prediction tool: Comparison between different approaches," *Radiation and Its Effects on Components and Systems (RADECS), 2011 12th European Conference on*, Sevilla, 2011, pp. 363-370.

[Re, 2013] V. Re, L. Gaioni, A. Manazza, M. Manghisoni, L. Ratti and G. Traversi, "Radiation Tolerance of Devices and Circuits in a 3D Technology Based on the Vertical Integration of Two 130-nm CMOS Layers," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 6, pp. 4526-4532, Dec. 2013.

[Rech, 2012] P. Rech, J.-M. Galliere, P. Girard, A. Griffoni, J. Boch, F. Wrobel, F. Saigne, and L. Dilillo, ―Neutron-Induced Multiple Bit Upsets on Two Commercial SRAMs Under Dynamic-Stress, *IEEE Trans. Nucl. Sci.*, vol. 59, no. 4, pp. 893–899, Aug. 2012.

[Reed, 1997] R. A. Reed, M. A. Carts, P. W. Marshall, C. J. Marshall, O. Musseau, P. J. McNulty, D. R. Roth, S. Buchner, J. Melinger, and T. Corbiere, "Heavy-ion proton-induced single event multiple upset," in *IEEE Trans. Nucl. Sci.*, vol. 44, no. 6, pp. 2224–2229, Dec. 1997.

[Roche, 2003] P. Roche, G. Gasiot, K. Forbes, V. O'Sullivan and V. Ferlet, "Comparisons of soft error rate for SRAMs in commercial SOI and bulk below the 130-nm technology node," in *IEEE Transactions on Nuclear Science*, vol. 50, no. 6, pp. 2046-2054, Dec. 2003.

[Rodbell, 2007] K. P. Rodbell, D. F. Heidel, H. H. K. Tang, M. S. Gordon, P. Oldiges, and C. E. Murray, "Low-Energy proton-induced single-event-upsets in 65 nm node, silicon-on-insulator, latches and memory cells," in *IEEE Trans. Nucl. Sci.*, vol. 54, no. 6, pp. 2474–2479, Dec. 2007.

[Sawyer, 1976] D. M. Sawyer and J. I. Vette, (1976, Dec). AP-8 Trapped Proton Environment for Solar Maximum and Solar Minimum. NASA NSSDC report NSSDC/ WDC-A-R&S 76-06.

[Schwank, 2006] J. R. Schwank, M. R. Shaneyfelt, J. A. Felix, P. E. Dodd, J. Baggio, V. Ferlet-Cavrois, P. Paillet, G. L. Hash, R. S. Flores, L. W. Massengill, and E. Blackmore, ―Effects of Total Dose Irradiation on Single-Event Upset Hardness,‖ IEEE Trans. Nucl. Sci., vol. 53, no. 4, pp. 1772–1778, Aug. 2006.

[Schwank, 2005] J. R. Schwank, P. E. Dodd, M. R. Shaneyfelt, J. A. Felix, G. L. Hash, V. F. Cavrois, P. Paillet, J. Baggio, P. Tangyunyong, and E. Blackmore, "Issues for

single-event proton testing of SRAMs," IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3692–3700, Dec. 2004.

[Sierawski, 2009] B. D. Sierawski *et al*., "Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions," in *IEEE Transactions on Nuclear Science*, vol. 56, no. 6, pp. 3085-3092, Dec. 2009.

[Simonen, 2001] P. Simonen, A. Heinonen, M. Kuulusa and J. Nurmi, "Comparison of bulk and SOI CMOS technologies in a DSP processor circuit implementation," *Microelectronics, 2001. ICM 2001 Proceedings. The 13th International Conference on*, 2001, pp. 107-110.

[Tipton, 2006] A. D. Tipton, J. A. Pellish, R. A. Reed, R. D. Schrimpf, R. A. Weller, M. H. Mendenhall, B. Sierawski, A. K. Sutton, R. M. Diestelhorst, G. Espinel, J. D. Cressler, P. W. Marshall, and G. Vizkelethy, ―Multiple-Bit Upset in 130 nm CMOS Technology, in *IEEE Trans. Nucl. Sci*., vol. 53, no. 6, pp. 3259–3264, Dec. 2006.

[Troxel, 2009] I. Troxel, "Memory Technology for Space", presentation in *Seminar Day, Military and Aerospace Programmable Logic Devuce (MAPLD)*, NASA Goddard Space Flight Center, Aug. 2009.

[Tsiligiannis, 2014] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, A. Todri, A. Virazel, F. Wrobel, F.Saigné, ―A Novel Framework for Evaluating the SRAM Core-Cell Sensitivity to Neutrons, in *RADECS*, France, Sept. 2012.

[Tsiligiannis2, 2014] G. Tsiligiannis *et al*., "Multiple Cell Upset Classification in Commercial SRAMs," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 4, pp. 1747-1754, Aug. 2014.

[Tsiligiannis3, 2014] G. Tsiligiannis *et al*., "Dynamic Test Methods for COTS SRAMs," in *IEEE Transactions on Nuclear Science*, vol. 61, no. 6, pp. 3095-3102, Dec. 2014.

[Tsiligiannis4, 2014] G. Tsiligiannis, "Soft Errors in Memory Devices: Novel Methods and Practices for Dynamic and Static Testing", Thesis manuscript, LIRMM/Université Montpellier, Sept. 2014.

[Wrobel, 2001] F. Wrobel, J. M. Palau, M. C. Calvet, O. Bersillon and H. Duarte, "Simulation of nucleon-induced nuclear reactions in a simplified SRAM structure: scaling effects on SEU and MBU cross sections," in *IEEE Transactions on Nuclear Science*, vol. 48, no. 6, pp. 1946-1952, Dec 2001.

[Xapsos, 2010] M. A. Xapsos, G. P. Summers, J. L. Barth, E. G. Stassinopoulos, and E. A. Burke. (2010, Jun.). Probability model for cumulative solar proton event fluences. *IEEE Trans. On Nuclear Sci.*, vol. 47, no. 3, pp. 486–490.

[Ziegler, 2008] J. F. Ziegler, SRIM, 2008 [Online]. Available: http://www.srim.org.

Chapter 4

Single Event Effect testing of FRAM memory

4.1 Introduction on FRAM memories

Unlike volatile memories, the data stored in non-volatile memories is not erased when the supplied power is turned off. This has the advantage of optimizing the power resources by switching off components and unnecessary units when not in use. Indeed, power management and optimization is of great concern in spacecraft design where power is often scarce, especially when the stored data is not often used (for example software configuration parameters, scientific data...). However, volatile memories such as SRAM or DRAM are optimised for fast access necessary for on-board computers to work efficiently. This is not the case for non-volatile memories, which are, in general, slower. However, the search for a non-volatile memory with access speeds similar to volatile memories is still being investigated. Hence, their use is complementary in embedded systems and complex electronic designs.

Emerging memories have started being used in electronic systems, such as MRAM or FRAM memories. It is hence of valuable interest to investigate the potential use of such memories for space systems. Only a few FRAM memories have flown in space so far, and there is still the need to better understand how they behave in-orbit.

For this reason, one type of FRAM memory has been chosen to be part of the MTCube payload experiment. The technology used for the non-volatility properties will be presented below. Then, after a review of the current state-of-the-art with respect to radiation testing, the SEE test results obtained for the FRAM memory will be presented.

4.2 Description of FRAM memories

4.2.1 Introduction

The idea to build a memory based on ferroelectric material first appeared in the master thesis of an MIT student in 1952 [Buck, 1952]. Ramtron has developed the technology for use as RAM and has been selling it since 1992. In 2011, the first FRAM based microcontroller was built by Texas Instruments. In 2012, Cypress Semiconductor acquired Ramtron and is now selling most of the FRAM memories. FRAM memories have started to be used more widely in the last decade.

Regarding space applications, there is only very little space flight heritage of FRAM memories. Space agencies, as presented in [MacLeod, 2009], but also space industries are interested in the performances of FRAM memories for space application for several reasons. First of all, FRAM memories have the advantage of being at the same time non-volatile and having extremely low power consumption (less than a few mA per Mb). Those two features fit the constraints of space applications where power saving is a must in order to reduce the overall weight and size (lower power consumption leading, for example, to lower solar panel size and weight), or to provide more resources for power hungry science experiment. FRAM memories have a very high endurance (read/write cycles ~ 10^{12}) compared to Flash memories (read/write cycles ~ 10^{5}) which allow longer and more frequent usage on-board. However, FRAM memory density is far smaller than NAND Flash memories, write operation (in the order of 100-150 ns) in FRAM memories is at least one order of magnitude higher than for SRAM

memories (in the order of 10 ns). On the other hand, access speed of FRAM memories is also 100 times faster than for NAND Flash memories. This makes this type of memory not ideally suited for use as large data storage device or cache memory but fits the criteria for use as boot-up memory for FPGAs or microcontrollers, for example, or a good candidate for storage of critical parameters.

4.2.2 Description of FRAM memories

High density ferroelectric memory (FRAM) is based on metal-organic chemical vapor deposition (MOCVD) process of lead zirconium/titanate (PZT) thin films. SBT material was also used but is less employed nowadays. This device represents a promising candidate for applications requiring low power consumption, fast write access, high cycling endurance, non-volatile data storage and good resilience to radiation. An FRAM memory cell relies on the electrical polarization of the PZT film. The PZT material can be switched between two stable states across the centre of the oxygen - octahedron with the application of an electric field, as depicted in Figure 55 (top). Depending on whether the polarization is opposite or aligned with an applied electric field, different levels of displacement current are induced during a cell read operation. A current-sensing circuit determines whether the ferroelectric capacitor is in a '0' or '1' state prior to the read operation. The cell loses its configuration during a read operation, and as a result the memory circuitry has to restore the cell to its original value after each read action. Read and write endurance is greater than 10^{12} cycles [Gerardin, 2010] and automotive-grade data retention reliability has been demonstrated with FRAM memory cells.

The ferroelectric material is embedded in a capacitor, which has a characteristic in the shape of a hysteresis loop as presented in Figure 55 (bottom). In position A, the charge -Q_{st} is stored in the capacitor; applying an electric field across the capacitor will lead to a charge Q_{op} (point C) which will be slightly reduced to Q_{st} when the electric field is removed (point B). From point B, the opposite voltage (or electric field) will lead to point D, which will then go back to point A at rest when no potential is applied. Hence, depending on the voltage, the charge stored at the node is different, enabling to store the '1' (point A by convention) or '0' (point B).

The properties of the ferroelectric material are then used in a memory cell architecture very close to a DRAM cell structure. The core memory cell is constituted of a single capacitor and access transistor in a 1T-1C cell architecture. In order to increase the content readability (read noise margin), a 2T-2C cell architecture can be adopted. This is the case for the device under study here. The basic 2T-2C FRAM cell architecture is depicted in Figure 56. In order to perform a write operation, the BL is set at V_{DD} (resp. 0V) and the PL (Plate Line, also called Driveline DL) is set at 0V (resp. V_{DD}) in order to write a logic '0' (resp. logic '1') after switching ON the access transistor by switching the WL at V_{DD}. In a DRAM cell the capacitor has always one side connected to 0 V.

To perform a read operation, the access transistors are switched ON by setting the WL at V_{DD} after the PL is set at V_{DD} and the BL and BLB are set at 0V. If the capacitor is negatively charged ($-Q_{st}$), representing a '1' bit, only a small charge will flow towards the BL (from point A to D) and the sense amplifier will detect only a small potential difference. Alternatively, if the capacitor is charged positively (Q_{st}), a large charge (from point A to C), due to the re-orientation of the atoms, will flow to the BL generating a much bigger potential difference that will be detected by the sense amplifier on the BL. It is important to note that, in this case, the bit stored in the read memory cell is reversed and needs to be re-written. This aspect considerably slows down the read cycle speed.

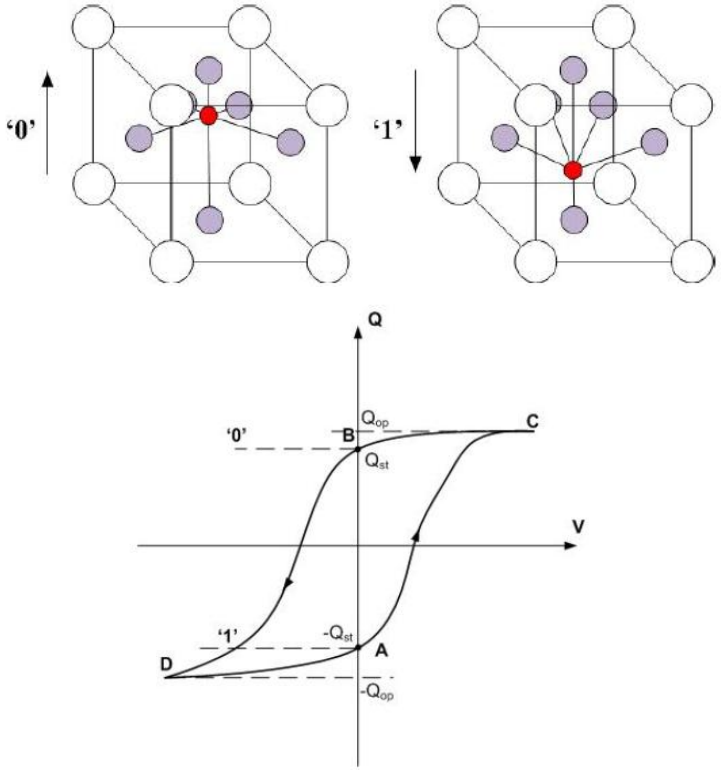


Figure 55 : (Top) PZT crystal with an oxygen atom in the centre. The two stable states of the crystal correspond to the two possible polarization configurations, which in turn correspond to the two possible states of a bit ('0' or '1'); (bottom) ferroelectric capacitor characteristics [Tsiligiannis, 2014].

In retention mode, BL, WL and PL are usually all kept at 0V.

The other ferroelectric capacitor needs to store the opposite value during a write operation; hence the electric field applied on the other capacitor is the opposite. Only during a read operation, both capacitors have a similar electric field direction applied to them [Moore, 1995].

The remaining peripheral circuitry is made with transistors in a similar fashion as for other RAM memories, to which is added the circuitry enabling to re-write the data that is lost during any read operation. Unlike a DRAM memory, the FRAM memory does not require any regular refresh of its content; on the other hand the cell area of an FRAM cell is much bigger than for a DRAM cell.

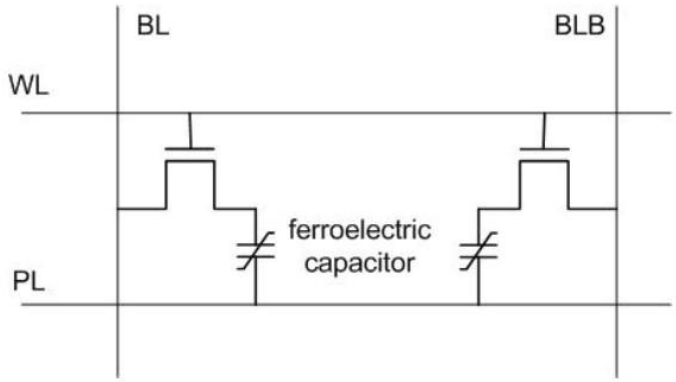


Figure 56 : 2T-2C FRAM cell architecture. The basic FRAM cell architecture (1T-1C) is solely constituted of one access transistor and ferroelectric capacitor [Tsiligiannis, 2014]. The gate of the access transistors is connected to the Bit Line (BL) or $\overline{Bit\ Line}$ (BLB). PL is the Plate Line. The presence of a PZT capacitor in opposite state in the same memory cell allows increasing the reliability of the memory cell at the cost of reducing the memory cell density.

4.2.3 FRAM memory under study

The device under test is a COTS 4Mb asynchronous FM22L16 FRAM memory that can be configured as a 256K*16 word bit or 512K*8 word bit memory. It is based on a 130 nm CMOS process and the cell structure is 2T-2C. This memory includes a low voltage monitor blocking the access when the supplied voltage drops below $V_{DD\,min}$ = 2.7 V. The device also includes a software-controlled write protection according to its datasheet but was not used during testing. Figure 57 depicts the lidded and delidded memory used in one of the test campaigns.

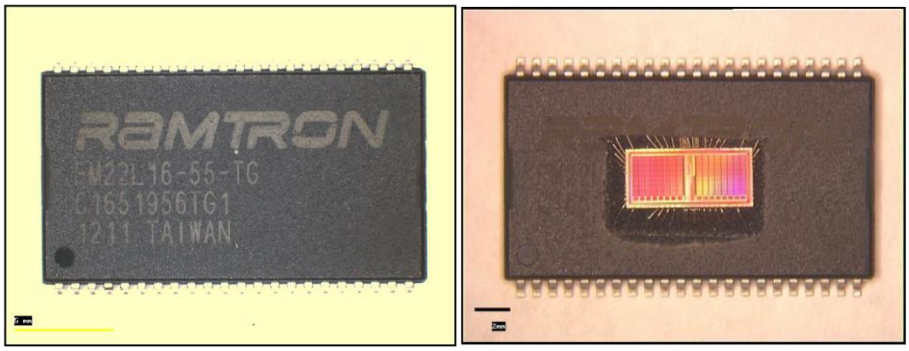


Figure 57 : Picture of the FRAM DUT used in this study (intact package and delidded package).

4.3 Radiation effects in FRAM memories

4.3.1 SEE on memory cells

Previous work studying the behaviour of FRAM under total ionizing dose [Nuns, 2007] showed that failure did not occur because of the ferroelectric thin film, but rather due to the control circuitry using non RadHard CMOS processes: heavy-ion irradiation with krypton ion at 0° and 45° (effective LET of 32.1 and 45.4 MeV.cm²/mg) and xenon ion with the same inclinations (effective LET of 60 and 85 MeV.cm²/mg) resulted in no error in unbiased mode testing. Since this non-volatile storage element is based on polarization and responds only to applied electrical fields, the FRAM memory cell is much less sensitive to soft errors from injected energetic particles compared to SRAM memory cells which are charge based.

4.3.2 SEE on the entire memory

In [Scheick, 2002], FM1806 and FM1808 Ramtron FRAM memories were tested against heavy-ions and resulted in soft errors. Considering that particle-induced parasitic currents cannot alter the polarization of the storage element, the susceptibility of the device to radiation effects is mostly due to failures in the control logic circuitry and peripheral circuit components such as the address decoders, I/O buffers, power switch, or sense amplifiers. Threshold LET for SEU was estimated at 22 MeV.cm²/mg and SEL LET threshold at a slightly lower value of 20 MeV.cm²/mg. The maximum SEU static (or dynamic? – not specified in the paper) bit cross-section was in the order of 10^{-9} cm²/bit but appears to be at an inclination ($\geq$ 45°). When errors occur, they appeared in blocks of tens/hundreds of errors leading to the authors' conclusion that they are probably due to SEFIs. More recent FM20L08 FRAM memories were tested in [Nuns, 2007], showing a static saturation bit cross-section of about 10^{-8} cm²/bit (higher sensitivity) and a static LET threshold above 40 MeV.cm²/mg. The dynamic bit cross-section was two orders of magnitude higher with a much lower LET threshold (4.7 MeV.cm²/mg). Similarly to [Scheick, 2002], the authors observed blocks (or bursts) of errors of a few (<10) addresses most of the time with possible MBUs. Thanks to laser testing, the authors were

able to show that a specific region was able to trigger clusters of eight to nine consecutive address errors, this region very likely being part of the peripheral logic.

Laser testing in [Scheick, 2002] also showed that some regions were very sensitive leading to all bits in error for all the addresses of the memory which required a power cycle to restore the device's functionality but this was not observed during heavy-ion testing.

Latch-up events may occur in FRAM memories: studies in [Scheick, 2002] and [Nuns, 2007] both showed latch-up events occurrences above a LET threshold of 20 MeV.cm²/mg as well (SEL saturation cross-section of about 10^{-6} cm²/bit in [Nuns, 2007] in both static and dynamic mode). On the other hand, in [Dalh, 2015], TI FRAM memories were tested for latch-ups under heavy-ions and proved to be SEL-free even at high supply voltage and high temperature at up to 45° inclination and an effective LET of 90 MeV.cm²/mg regardless of the operation mode (static/dynamic) and data pattern.

In [Zhang, 2015], the FM22L16 was tested in dynamic (successive reads) and unbiased mode. Similarly to previous results, the unbiased mode resulted in no error. The authors categorised the errors in different types: besides SBUs, they also noted clusters of bits in error in adjacent cells like previously noted in previous FRAM technologies, but also MBUs with either the address or the data showing only 0x0000. The authors also saw soft as well as hard SEFI and soft and hard SEL but it is unclear whether they were seen on the FM22L16 as well (the other FRAM tested memory was the FM18W08).

Regarding proton testing, tests performed at 200 MeV and a total fluence of 3×10^{11} protons/cm² showed a rather good robustness with only a few SEUs (6 SEUs) and no latch-ups occurrences [Nuns, 2007] resulting in a SEU cross-section of 5.72×10^{-17} cm²/bit with an upper 2σ uncertainty from Poisson distribution of 1.25×10^{-16} cm²/bit.

4.3.3 Dose

In 1991, Benedetto et al., an FRAM memory was tested against TID and showed a very poor TID resilience below 2 to 4 krad(Si) [Benedetto, 1991]. The degradation occurred due to the CMOS part of the memory (ferroelectric films being able to withstand > 10 Mrad(Si)) [Benedetto, 1991]. TID tests were conducted on FM1608 and FM1808 in 2001 [Nguyen, 2001], at both low and high dose rates (0.0116 and 50 rad(Si)/s) using Cobalt-60 but also protons. Results showed that above 12.5 krad(Si) errors started occurring (when biased at nominal 5V) and both memories failed at 25 krad(Si) without being able to recover even after annealing. Reducing the dose rate slightly increased the error threshold but at 25 krad(Si) at low dose rate and similarly with protons, both memories failed. Unbiased devices were still functional after 7 Mrad(Si). The authors concluded that the sense amplifier circuits as well as reference voltage generators (based on CMOS technology) were the cause of the failures for both memories. Similarly, in [Katz, 1999], although results did not allow for a high confidence guess, the authors suspected the sensing/writing circuitry of the memory to be sensitive to total dose exposure.

In [Nuns, 2007], a bunch of FM20L08 FRAM memories were tested against TID at a 60Co facility at a dose rate of 200 rad(Si)/h and maximum supplied power. Results showed that all parts survived, biased and non-biased survived up to 31 krad(Si). Some biased devices did not survive up to 35 krad(Si) but recovered after annealing at 100°C although the standby current increased for all biased components, whereas the non-biased devices were still functional. Tests conducted on FM18L08 memories [Zanata, 2008], showed that the peripheral circuitry starts failing at dose higher than 280 krad(Si) with complete failure at 400 krad(Si) although the core memory cells are able to withstand at least 1 Mrad(Si) without errors or stuck bits. Ferroelectric thin films are resilient to TID up to at least 1 Mrad(Si) [Moore, 1995]. This can increase to even 10 Mrad(Si) depending on the process used during the fabrication [Schwank, 1990].

In [Gu, 2014], two FRAM memories were tested at a Cobalt-60 facility (dose rate 100 rad(Si)/s) which showed good resilience: FM24CL16 (resp. FM25L04) functioned up to 100 krad(Si) (resp. 50 krad(Si)) although the current supply increased considerably after 30 krad(Si) (resp. 18 krad(Si)). After irradiation, it was possible to perform write operations and store data again in the biased FM25L04; the unbiased memory was still functional. However, both failed at 200 krad(Si). Regarding the FM24CL16, although both biased and unbiased memories were still functional. More recently, in [Dahl, 2015], the authors tested a TI FRAM embedded in a 180 nm CMOS technology and showed a good resilience regardless of the data pattern (no retention failure and low enough voltage margin changes) of biased 1C-1T cells up to 300 krad(Si) (for information, the dose rate was 87 rad(Si)/s). This result was shown to be even better for 2C-2T cells. Interestingly, the industrial standard FRAM showed large numbers of SEFIs linearly increasing with the heavy-ion fluence: this was in fact due to the SRAM part of the memory that remaps some FRAM memory cells which are malfunctioning.

4.3.4 Other effects

Temperature does impact the reliability of FRAM memory cells, by reducing the signal margin due to spontaneous polarization of the ferroelectric layer (thermal depolarization) [Dahl, 2015]. According to the authors, dynamic and static supply currents behave similarly at high temperature as when exposed to high TID.

Imprinting is also an issue in FRAM memories, which does not exist in memories such as in SRAM. This occurs when a specific bit is stored in a FRAM memory cell for a long period of time, then this bit becomes the preferred polarization state [Dahl, 2015]. The imprinting effect worsens with increasing temperatures. Imprint effects were first discovered in 1995 by Moore and al. at room temperature during irradiation under X-rays (this effect was known earlier but only at higher temperatures) up to 400 krad($Si0_2$) [Moore, 1995].

In [Zanata, 2008], the issue of stuck bits is raised on FM18L08 FRAM 1T-1C memories tested against 10 keV X-ray and 5 MeV protons as well as the impact of temperature. It was shown that the core memory cells are functioning at least up to 9 Mrad(Si) if kept in unbiased mode. Nevertheless, although the information is properly stored, stuck bits may occur when rewriting the memory. At higher dose levels (>1 Mrad(Si)), the PZT film may be subjected to hysteresis loop deformation due to charge trapping in the PZT material itself (smaller hysteresis loop, general degradation due to dose accumulation) or charge trapping at the ferroelectric/electrode interface (shifting of the hysteresis loop in a direction dependant on the polarization state, specific to ferroelectric material due to imprint effect) leading to stuck bits [Zanata, 2008]. This seems to show that imprinting issues are also worse in a very high radiation environment (>1 Mrad(Si)). Natural annealing may occur although cycling drastically increases the annealing time which can be further increased at higher temperatures (although high temperatures only provide an apparent recovery but subsequent TID tests demonstrated a even higher sensitivity compared with the initial irradiation).

Finally, Zanata et al. [Zanata, 2008] also showed that considering only the memory core cell, X-ray irradiation makes the cells more sensitive to TID with respect to proton irradiation and this could be due to dose enhancement effects as high-Z material are present especially in the PZT material.

4.3.5 Hardening techniques

2 Transistors-2 Capacitors (2T-2C) architecture, as mentioned above, allows reducing the sensitivity of FRAM memory cells by improving the voltage margin [Dahl, 2015]. But this architecture provides a lower memory cell density [Gerardin, 2010]. In [Dahl, 2015], a radiation hardened by design TI FRAM memory with improved robustness at high temperatures was tested and showed satisfactory

results for space applications. Previously, Kamp et al. designed a RadHard FRAM memory able to withstand 2 Mrad and be latch-up free up to 163 MeV.cm²/mg [Kamp, 2005], [Philpy, 2004].

It is hence possible to have extremely robust FRAM memories built for severe space applications. Nevertheless, these RadHard memories are still rather rare in the market and the use of COTS FRAM memories might be robust enough for low-severity radiation environment space mission such as for the MTCube mission.

4.4 FRAM test results based on heavy-ion testing

In this study the vulnerability of the COTS FRAM device selected for the MTCube project under heavy-ion radiation is investigated. For the MTCube project, the FRAM is provided by 3D Plus, and it is based on four vertically stacked FM22L16 memories produced by Ramtron. Due to the very low penetration of heavy-ions in most accelerator facilities, heavy-ion testing was conducted on standalone FM22L16 components.

All memories were delidded prior irradiation tests. Seven Test Campaigns (TC) were conducted at three different heavy-ion radiation test facilities: the RADEF facility in Jyväskylä hosted TC1, TC3, TC4, TC8 and TC12; the UCL facility in Louvain-La-Neuve hosted TC5; the GANIL facility in Caen was used for TC9. During each TC, a different FRAM was used, except during TC8 where two different components were tested. Heavy-ion cocktails applied for each test campaign are detailed in Table 12. During TC1, mainly static tests were performed together with two types of dynamic tests on a single DUT. The heavy-ion induced dose level reached on the DUT was estimated, based on the recommended dose estimation formula from the ESCC 25100 standard, to approximately 7 krad($Si0_2$) with an additional run during the same test campaign adding an extra 5 krad($Si0_2$). Static and dynamic tests were carried out during TC4 on another single DUT using several angles with two different types of particles. The estimated dose level was below 7 krad($Si0_2$). For TC8, two DUTs were tested under static and March Dynamic Stress conditions reaching respectively 9 krad($Si0_2$) and 33 krad($Si0_2$). Static and dynamic tests were conducted on one DUT in TC9, with estimated dose level of 1.4 krad($Si0_2$). Finally, one DUT was used to perform unbiased tests during a small test campaign (TC12). The tested memory, during TC5, very quickly failed after the third run. More information regarding the possible failure mechanisms is presented in section 4.4.4.4.

At all facilities, the beam homogeneity was determined to be +/- 10% or better over the chip surface. Several test runs were carried out during each test campaign, with ion species, energy and electrical stimuli varying from run to run. Depending on the run, the particle fluence was in the range of 5×10^3 up to 1.22×10^7 cm^{-2}.

The DUTs were mounted on PCB cards and connected to controllers implemented through FPGAs. Except for TC4 were the DUT was tested in air due to the configuration of the facility (the air and the degraders were taken into account when calibrating the beam in order to have the energies and LET mentioned in Table 12), for all test campaigns, the DUT was located in a vacuum chamber, directly exposed to the beam while the FPGA, although located in the chamber, was placed outside the beam line to ensure reliable operations. During each test run, in case a bit flip was detected the erroneous word, along with other information, such as the address and the timestamp, was transmitted to a computer, for storage and data processing.

As mentioned above, the memory devices were tested under two different test modes: the *static* and the *dynamic mode*. During the static mode a known data pattern is stored in the memory, which is then irradiated. Subsequently, a comparison is performed between the pre-irradiation and post-irradiation data to detect the bit flips. During dynamic mode testing, specific sequences of write and read operations are repeatedly performed during irradiation exposure. Read operations are fundamental in

dynamic mode, since they stimulate the control circuitry, while also providing the stored value of the memory cells.

Test Campaign (Facility)	Ion	Incl.	Energy (MeV)	Effective LET (@ Top of BEOL) (MeV/(mg/cm2))	Range to Bragg Peak (µm)
TC1 (RADEF)	N	0°	139	1.8	202
	Fe	0°	523	18.5	97
	Kr	0°	768	32.1	94
	Kr	45°	-	45.4	-
TC3 (RADEF)	N	0°	139	1.8	202
	N	45°	-	2.6	-
	N	60°	-	3.6	-
	Fe	0°	523	18.5	97
	Fe	45°	-	26.2	-
	Kr	0°	768	32.1	94
	Xe	0°	0°	1217	60.0
TC4 (RADEF)	Ne	0°	186	3.6	146
	Ne	30°	-	4.2	-
	Ne	45°	-	5.1	-
	Ar	0°	372	10.1	118
	Ar	30°	-	11.7	-
	Ar	45°	-	14.3	-
	Ar	50°	-	15.7	-
TC5 (UCL)	N	0°	60	3.3	59
TC8 (RADEF)	N	0°	139	1.8	202
	Fe	0°	523	18.5	97
	Kr	0°	768	32.1	94
	Xe	0°	1217	60.0	89
	Xe	30°	-	69.3	-
TC9 (GANIL)	Xe	0°	466	64.3	37
	Xe	0°	1790	50.2	137
TC12 (RADEF)	Xe	0°	1217	60.0	89
	Kr	0°	768	32.1	94
	Xe	45°	-	84.8	-
	Kr	45°	-	45.4	-

Table 12: Heavy-ion cocktails used at the different facilities. TC stands for Test Campaign. Inclination angle is defined as the angle between the axis normal to the die plan and the beam. The range to Bragg peak is the distance travelled by the ion from the surface of the die to the Bragg peak.

For the dynamic tests, we employed March algorithms that have been previously used on SRAM devices: March C-, Mats+ and March Dynamic Stress [Tsiligiannis2, 2014] [Tsiligiannis3, 2014] with the different addressing schemes as presented in chapter 3. The FRAM study will essentially focus on normal (i.e. logical) addressing scheme. The cross-sections presented below are the bit cross-sections, e.g. the cross-sections calculated by counting the number of bit errors.

4.4.1 Unbiased mode test results

During TC12, a FRAM specimen was tested in unbiased mode after storing a checkerboard pattern in the core memory cells. Due to time constraints, it was only possible to test the memory against the two highest ions available in the RADEF cocktail. Hence the memory was tested against Xe and Kr ions at normal incidence (3 different runs at each different LET of 32.1 and 60 MeV.cm²/mg) and 45°

incidence (1 run at each different LET) with an effective surface LET spanning from 32.1 to 84.8 MeV.cm²/mg. Various fluences were achieved from 1.1×10^5 cm^{-2} to 1.0×10^7 cm^{-2}. These tests resulted in no error detected when reading back the memory after irradiation. Biased functional tests were performed in order to ensure the good functionality of the set-up between each irradiation. Those results are in agreement with work presented in [Zhang, 2015] on the same memory.

4.4.2 Static mode test results (biased mode)

In this section, the results of *static mode* tests performed during all test campaigns with LET ranging from 1.8 up to 69.3 MeV.cm²/mg are presented, when the memory was biased. During static tests, the applied patterns were solid '0' (0x00), solid '1' (0xFF) and the checkerboard patterns (0xAA or 0x55). The radiation sensitivity of the FRAM did not show any dependency on the data background pattern.

Preliminary tests conducted on this FRAM, and summarized in [Gupta, 2016], led to the possible conclusion that the memory was impacted by fluence, possibly linked to temporary dose effects on the peripheral circuitry of the memory. Since then, additional tests were conducted and analysed. Fluence was increased and results from all test campaigns are summarized in Figure 58 showing the SEU bit cross-section. In this figure, only the non-zero cross-section obtained at high fluence (> 1.0×10^6 cm^{-2}) were considered. This is due to the fact that by grouping the runs according to the fluence, it appears that, almost all runs with fluence below or equal to 1.0×10^6 cm^{-2} lead to no error, whereas for higher fluence, the bit cross-section resulted, either in a large number of errors, or in no errors at all in some cases, at most of the LETs at which the device was tested. Some more insight may be provided by looking at logical bitmaps of the memory, which will be explored in the next sub-section. Indeed, runs performed at different LETs but resulting in peculiar types of errors (vertical lines or horizontal lines) always result in very high cross-sections compared to the tendency shown by the other obtained cross-sections. Hence, they are not included in the Weibull fit for this memory. Only one cross-section value obtained during TC3 remained rather high but the bitmap did not show any peculiarities.

In [Nuns, 2007], the authors tested an FRAM memory (FM20L08) and noticed that, during static tests, no errors were recorded if a power cycle was performed prior to reading the memory whereas without a power cycle bit flips could appear. During most of the runs performed in this study, it appears that all bits flipped could be corrected without the need of a power cycle. In rare cases, a power cycle was performed and was sufficient to remove errors and did not impact the good functionality of the memory. The same authors calculated a bit cross-section of about $\times 10^{-8}$ cm²/bit on a FM20L08, which is about an order of magnitude higher than the results obtained on the FM22L16 in this study. The most surprising observation is that the LET threshold for the FM22L16 is higher than 40 MeV.cm²/mg, which is not at all what was noticed for the current DUT FRAM.

Besides, a deeper analysis of the test data, by using the test log files, shows that the large numbers of bit flips obtained in certain runs are due, not to isolated SEUs, but rather to Multiple Bit Upsets (MBUs) within the same word. This aspect will be studied more in-depth with the support of logical bitmaps in section 4.4.4. MBUs did not appear during unbiased mode tests even with krypton (Kr) ion. Thus, it was concluded that MBUs are likely to be the consequence of errors occurring in the peripheral circuitry, such as the I/O buffers that are mapped as errors in the memory cell array.

In summary, Figure 58 demonstrates that this particular FRAM has a good heavy-ion SEU resilience in static mode at low levels of fluence such as those expected for the MTCube mission being in LEO polar orbit. For the purpose of MTCube, in static mode, the worse bit cross-section will be considered in chapter 5.

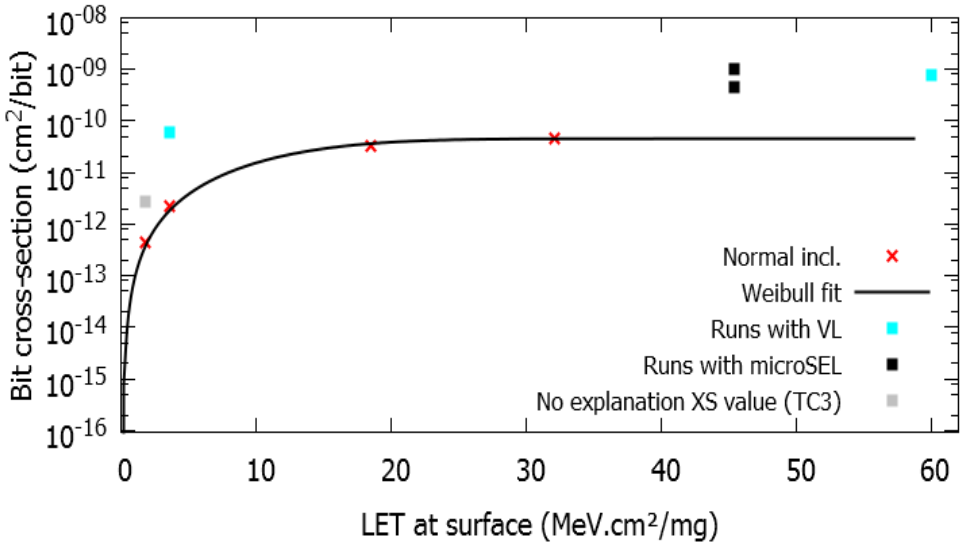


Figure 58: FRAM SEU bit cross-section in static mode regardless of the data pattern for runs resulting in non-zero cross-sections with fluences higher than 1.0 × 10^6 cm^{-2}. 1σ error bars are not shown as they are the size of the symbols. As several runs were performed for low LETs (1.8 and 3.6 MeV.cm²/Mg) the plotted cross-section is the average cross-section. The Weibull curve was fitted to the normal inclination resulting in "normal" bitmaps. Cross-sections with occurrences of VL (Vertical Lines) and µ-SEL are also shown.

4.4.3 Dynamic mode test results

Dynamic mode tests were conducted during all the test campaigns and the related results could only be performed on logical (not physical) schemes. For all applied March algorithms, the number of collected errors has been sensibly larger compared to static mode although the fluence was similar to the runs in static mode. The high failure rate could be associated to Single Event Transients occurring in the control logic during read/write access operations.

Figure 59 illustrates that, for each test algorithm, the radiation sensitivity of the memory follows a typical SEU cross-section curve with a LET threshold below 1.8 $MeV.cm^2/mg$ (the lowest LET at which the memory was tested). The calculated SEU cross-section takes into account the total number of bits flipped. This might explain, for example, why at 60 MeV.cm²/mg, the March C- dynamic SEU cross-section is higher than expected due to possible larger clusters of events (as the scrambling of the memory is currently unknown, it was not possible to properly cluster the events). The saturation for all curves occurs very rapidly with increasing LET values. It is interesting to notice that there is a clear difference between the March Dynamic Stress algorithm saturation SEU cross-section and all the other algorithms utilized during the test campaigns: there is almost two orders of magnitude of difference. Furthermore, it is observed that the March Dynamic Stress test presents an opposite behaviour than that observed for SRAMs. Among the various March algorithms applied on the 90 nm SRAM, the March Dynamic Stress test was the one that returned the highest SEU bit cross-sections. The opposite behaviour of the two types of memories may be explained by their architectural and functional differences. The March Dynamic Stress test has been specifically created to generate a 'hammering' effect on SRAM cells by performing sequences of read accesses for each memory location. In [Dilillo, 2005] and [Dilillo2, 2005], the hammering effect has been proven to reduce significantly and progressively the Read Noise Margin (RNM) of the SRAM cells, thus making them more prone to be upset if disturbed by radiation-induced transients. In the case of the tested FRAM device, the storage elements are ferroelectric cells that do not exhibit any RNM reduction, since a restoring write is operated after each read access, as explained above. Besides, as the cell structure of the FRAM under test is a 2T-2C structure, it is more immune to parasitic noise [Moore, 1995]. Moreover, in FRAMs, the most sensitive part is the CMOS control logic (address decoders, address/data registers, etc.), which is less affected by the March Dynamic Stress test, which presents the lowest switching activity for the peripheral electronics compared to the other algorithms, since the change of address is made

every seven access cycles (number of operations per element), and data up to six cycles (five consecutive read operations in one element and the first one of the next element).

Similarly to reference [Nuns, 20007], it was also noticed that most of the first errors occurring during dynamic mode testing occurred on consecutive addresses. Moreover, several bit errors were MBUs, highlighting the sensitivity of the memory to the switching activity. Those few consecutive errors were then followed by large clusters of block errors. Additionally, other types of dynamic tests (namely E and F in Figure 59) where used with high switching activity and resulted in SEU cross-section values similar to March C- of Mats+ dynamic tests. The bit cross-section obtained for the tested memory is about an order of magnitude lower than the one calculated by Nuns et al. (dynamic cross-section being 10^{-6} cm^{-2}/bit). Again the LET threshold found by the authors for the FM20L08 is higher than the one found for the FM22L16. All the previous remarks favour the hypothesis of the increase of sensitivity of the CMOS electronics in the peripheral circuitry, which is only solicited in dynamic mode testing.

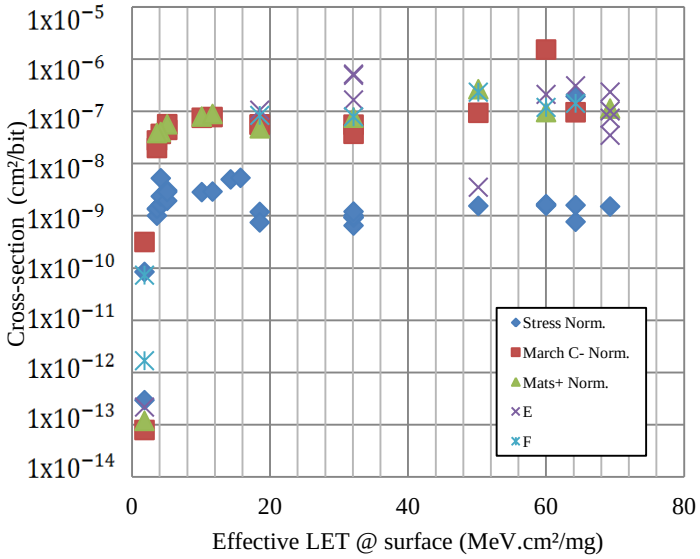


Figure 59: Heavy-ion SEU cross-section per bit during dynamic mode testing. Different markers are used for different testing algorithms. Norm. means that the addressing scheme is a logical increasing addressing scheme. The 1σ standard deviation (due to the number of counted errors and facility dosimetry) on the SEU cross-section did not exceed 15 % except for the Nitrogen particle.

In Figure 60, the effect of different types of addressing scheme applied during dynamic test is presented (normal addressing, LSFR, gray and anti-gray as described in [Tsiligiannis2, 2014]) for the March C- test. It appears that the addressing order at which the memory cells are accessed does not impact the sensitivity of the memory (which was the case, on the contrary, for SRAMs memories [Tsiligiannis2, 2014]). Similarly, no impact of the addressing scheme was observed on the March Dynamic Stress and Mats+ tests. The two orders of magnitude lower than expected cross-section, at a LET of 50 MeV.cm^2/mg, has not been yet fully undertood.

Finally, regarding the latchup occurrence, no important overcurrent due to SEL was recorded during the heavy-ion test campaigns. However, some current fluctuations have been noticed in a few runs, as it will be discussed in section 4.4.4. In [Scheick, 2002] and [Nuns, 2007] observations were made regarding latch-up events occurrences above a LET threshold of 20 MeV.cm²/mg as well. In [Zhang, 2015] SEL was also observed on a FRAM memory. Although the current has not been precisely measured during the above-mentioned TCs, no large current variations have been noticed. However, tests conditions were not optimal to trigger SEL (during all runs, the memory was supplied with nominal voltage and was kept at room temperature).

Contrary to the tested SRAM memories, the Dynamic March Stress test is the least stressful dynamic mode test whereas the other dynamic modes tested give similar cross-sections at all LETs. This result

may suggest that the switching activity, which is higher in all the other test modes, could imply a higher sensitivity of the periphery.

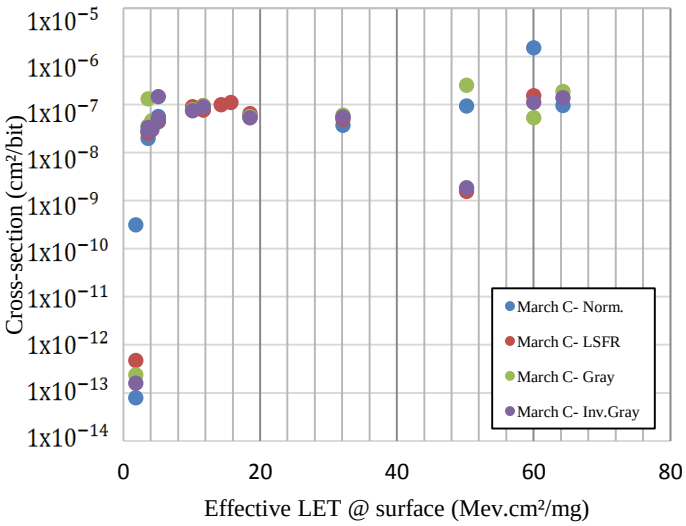


Figure 60: Heavy-ions SEU cross-section during dynamic mode testing on TC1, TC2, TC3 and TC4 focusing on the different addressing scheme of one type of dynamic mode test performed (here March C-). The 1σ standard deviation (due to the number of counted errors and facility dosimetry) on the SEU cross-section did not exceed 15 % except for the Nitrogen particle.

4.4.4 Bitmap analyses

4.4.4.1 Logical bitmaps generation assumptions

In order to further investigate the failure mechanisms induced by heavy-ions on the FRAM memory, in-house tools have been developed and adapted to the studied FRAM. As the scrambling scheme of the memory remains unknown, it was only possible to generate logical bitmaps. Bitmaps enable to show which word of the memory (and which bit of this word) appeared to have flipped during irradiation. The bitmaps have been constructed following the following rules: one pixel represents one bit, white pixels represent apparent (observed) flipped bits whereas black pixels represent bits correctly read by the memory. In logical bitmaps, memory cells with contiguous addresses are displayed as topologically neighbouring cells. On the other hand, a physical bitmap would allow representing the actual location of the memory cells on the die since it takes into account possible scrambling and interleaving schemes. However, unless provided by the manufacturer, this information is not shared to the customers. Physical bitmaps would allow a deeper understanding of failure mechanisms but also possibly look into, for example, the presence of sensitive regions on the die. This is not possible with logical bitmaps. However, logical bitmaps do not necessitate confidential information regarding the internal layout of the memory plan and may enable, to a certain extent, an understanding of the behaviour of failures during irradiations.

With the information provided by the datasheet of the studied memory, it was decided to generate bitmaps having four words per line. Indeed it is mentioned in the datasheet that: “Each row has 4 column locations, which allows fast access in page mode operations”. These consecutive words are accessed by the two Least Significant Bits (LSBs). In fact, this memory offers a “page mode operation” and when accessing a given column any other words of this column may be accessed without the need to toggle the Chip Enable pin but only by changing the two least significant bits. For this reason, all four words (each word of this memory has 16 bits in the configuration used for the tests of this work) having similar addresses only differing from the two LSBs are displayed on the same

line. No interleaving has been included, all bits of a word are depicted as contiguous. The fact that the array is organised as eight blocks of 8192 rows was not used, since the scrambling is unknown. In fact, for display and ease of analysis purposes, the bitmaps will present 32 blocks with a vertical axis length of 2048 bits. Hence the generated bit maps are made of 2048 pixels (32 columns made each of 4 consecutive words of 16 bits) on the horizontal axis and 2048 pixels on the vertical axis. In order to separate the blocks, grey lines have been added.

Logical bitmaps from static tests will be first treated, then dynamic test bitmaps will be discussed, by precisely describing the different topologies of encountered errors. The fault mechanisms beside the detected errors will be then proposed.

4.4.4.2 Results in static mode testing

The analyses of the bitmaps in static mode testing, for the runs resulting in upsets, showed interesting patterns on the logical bitmap. First, runs tested with nitrogen and neon ions (the lowest heavy-ion LETs at which the FRAM was tested) resulted mainly in very scarce SBUs (very few bits flipped). This is compatible with findings from [Zhang, 2015], where SBUs have been noticed. Static test results in TC3 are not included in this analysis as they presented logical bitmaps very different from the other static ones: during this campaign a true static test was not performed but rather a pseudo-static test with a periodic reading of the memory with a very small duty cycle. It is believe, with the amount of data acquired during the multiple test campaigns, that this might explain the reason why the topology of errors are very different, actually being due to the stress on the memory due to the dynamic access periods. These bitmaps will be analysed in the dynamic mode testing results, as presented below.

Testing with neon ion (Ne), using a ‘solid 1’ pattern in static mode, a small region of the bitmap showed discontinued vertical lines of single bit in error (Figure 61), the same bit of several words, besides some localized SBUs located next to those lines.

Finally, during TC1, when testing under krypton at 45° (effective LET of 45.4 MeV.cm²/mg), the memory’s power consumption increased up to 75 mA. During the first run, no errors were detected but during the next two runs, the logical bitmaps showed some stripes of errors in the first and last two blocks evenly spaced between them (Figure 62). No SBU was detected.

4.4.4.3 Results in dynamic mode testing

Now, analysing the logical bitmaps of dynamic tests, first the focus will be on March Dynamic Stress tests results. The effect of the addressing scheme will not be studied due to time constraints but would be interesting to explore. However, based on the bit cross-section calculation such as in Figure 60, it appears that there is no relevant impact of the addressing scheme.

Considering normal addressing March Dynamic Stress runs, bitmaps showed mainly Full Word Failures (FWF): all bits of a given words are failing (represented in a logical bitmap by a white line of 16 pixels or bits). No single bit events were recorded on the same device tested with nitrogen (N), iron (Fe), and krypton (Kr). During another test campaign testing with xenon (Xe, LET of 60 MeV.cm²/mg) apparent SBUs appeared along with FWFs. Besides FWFs, two words entirely failing on the same line of a block were observed (two consecutive FWF). Very rarely three consecutive FWFs were noticed (three words in one line). Further, entire lines appeared to be in errors with all words of one line partially in error (Figure 63): these will be called four consecutive Intermittent Words Failures (IWF), which started appearing when testing with iron (Fe). In [Nuns, 2007], MBUs have been reported on FM20L08, which might be linked to FWFs.

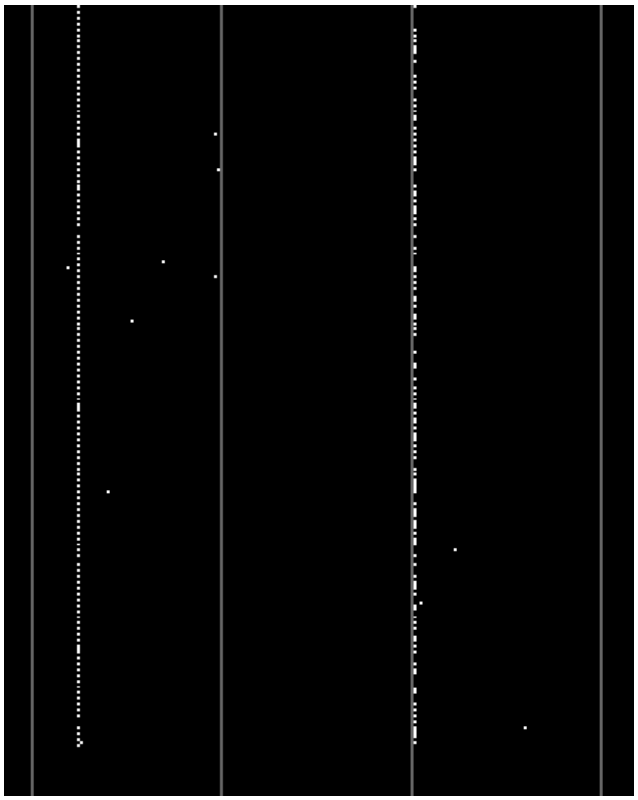


Figure 61: FRAM logical bitmap section showing discontinued vertical lines along with isolated bit errors when testing an FRAM memory under neon in 'solid 1'. White pixels represent bits not correctly read; grey vertical lines allow separating blocks for visual interpretation.

*Figure 62: FRAM logical bitmap section showing the leftmost part of the bitmap with double error lines spreading on two blocks (4*2 words). On the rightmost part of the memory only single lines spread are present also spreading on two blocks. The double error lines on the rightmost part of the bitmap are exactly similar.*

Figure 63: FRAM logical bitmap section showing examples of a failure of a line in one block (all 4 consecutive words in error but not all bits failing).

When testing at the same LET, Intermittent and Continued Vertical Lines (intermittent or continued) appeared, which are similar to those observed in static mode testing. Similar topology of errors occurred during various runs in dynamic mode testing during TC1, TC3, TC4 and TC7 (Figure 64 and Figure 65), most of the time, on the same region of the same DUT and only during the application of March Dynamic Stress, E and F tests.

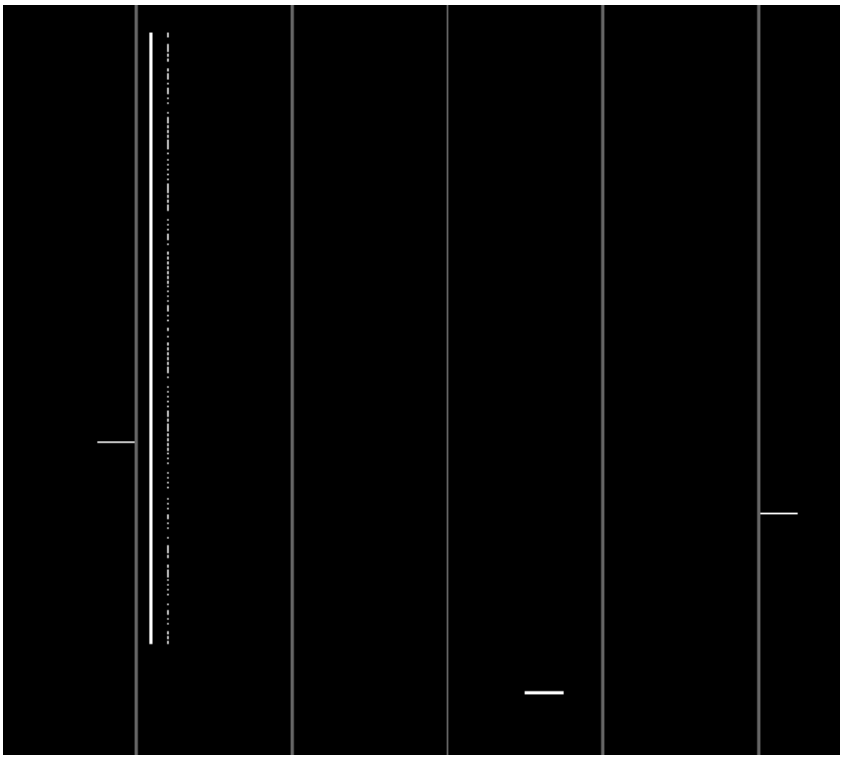


Figure 64: FRAM logical bitmap section showing discontinued and continued vertical lines (VL). Discontinued VL were also observed in static mode tests (Figure 61). Three FWF can also be seen on this logical bitmap section.

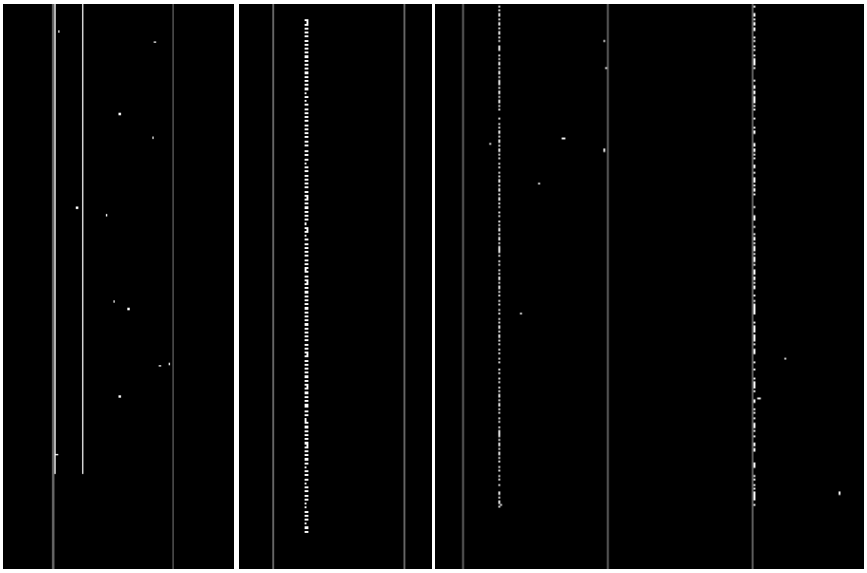


Figure 65: FRAM logical bitmap section showing the same region of the memory where intermittent vertical lines were spotted on the same DUT during the same TC: (left) during March Dynamic Stress, (middle) during test F, (left) during static solid'1' test two vertical lines can be spotted.

A recent testing opportunity allowed to test an FRAM with a 8 keV X-ray pulsed microbeam (equivalent to about a LET of 60 MeV.cm^2/mg). During this run, the region of the peripheral circuits placed in the central spine of the memory were targeted in the available time. It was possible to successfully reproduce apparent SBUs, some IWFs, and two IVLs during a single dynamic F test run. The resulted bitmaps sections are presented in Figure 66. When looking more closely at the log files, what appeared to be IWFs, were in fact all apparent SBUs which superposed over time (e.g. two SBUs occurring on the same address location at a different time interval).

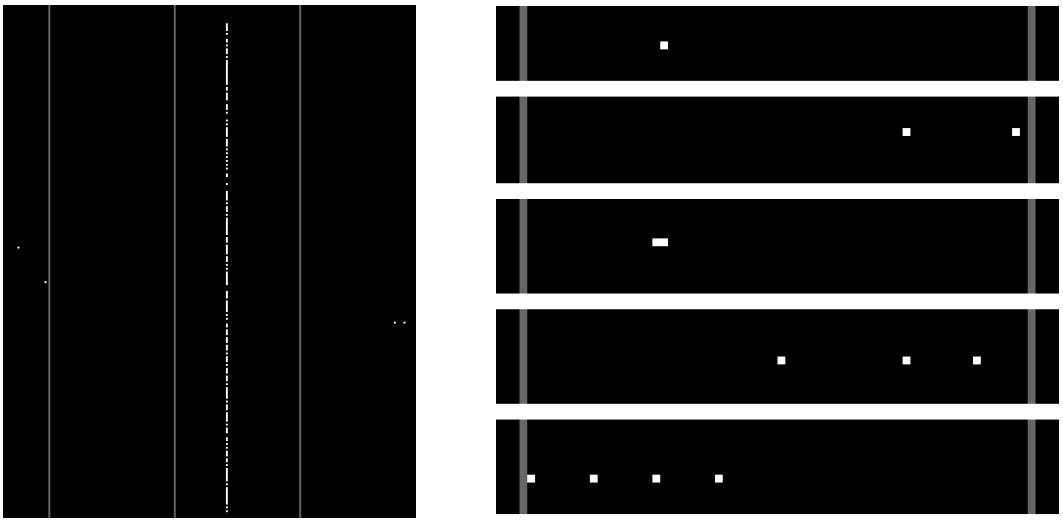


Figure 66: FRAM logical bitmap sections (at different scales) during X-ray microbeam irradiated at 8 keV under Dynamic F mode testing when irradiating a specific region of the memory periphery. Two intermittent VLs were successfully reproduced (left) as well as apparent SBUs or MBUs (right).

New error topologies not present in static mode testing also appeared at high LETs (Figure 67 and Figure 68): partial block entirely in error, when testing with krypton (Kr) accompanied with a small peak of current to 10 mA, and partial block intermittently in error, when testing with xenon (Xe), with the latter, being much larger that the former one. These consecutive addresses in errors have also been reported by [Scheick, 2002] on a FM1806 and FM1808, as well as in [Nuns, 2007] on FM20L08 and in [Zhang, 2015] on FM22L16.

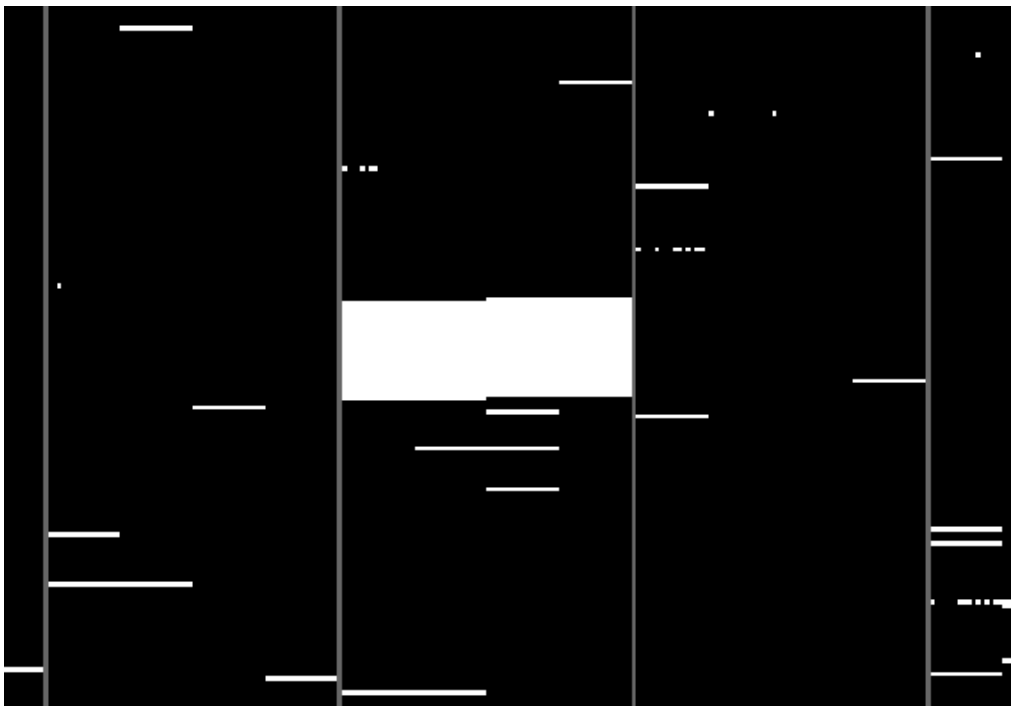


Figure 67: FRAM logical bitmap section showing a block failure: consecutive line of one block with all bits of the words failing. During this test, a peak of current was noted to 10 mA.

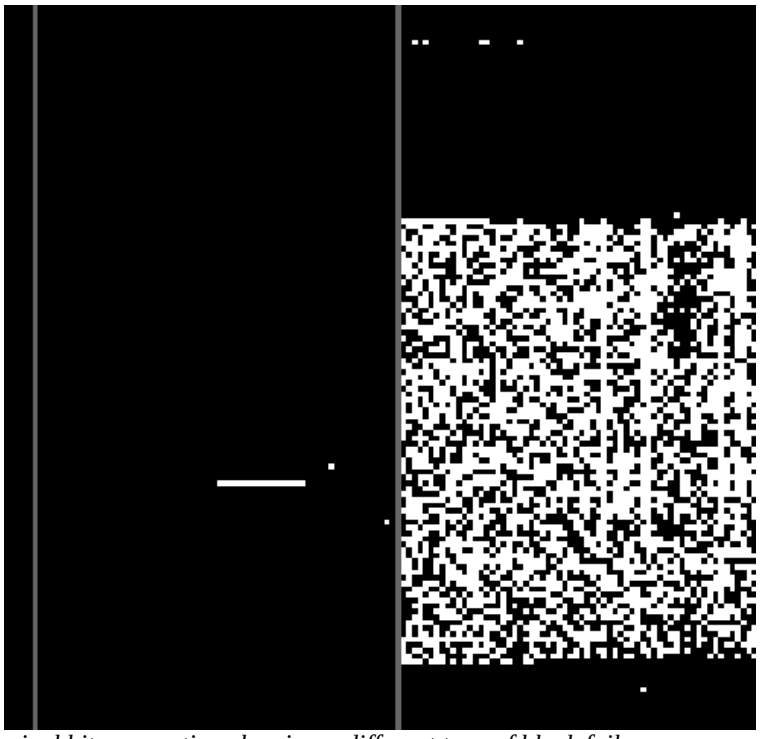


Figure 68: FRAM logical bitmap section showing a different type of block failure: consecutive line of one block with partial bits of the words failing.

As mentioned in the above analysed, logical bitmaps are a superposition of many read/write operations, it may be of interest to look at the results obtained during pseudo-static tests performed during TC3, where a read operation is performed at an extremely low read/irradiation duty cycle (read back every two minutes) during a long static irradiation of several minutes. During each run, a maximum of 5 read operations may have occurred during the pseudo-static test. Sections of the bitmap, which largely differ from common error topologies found in static mode, are shown in Figure 69. Besides FWFs, and very rare four consecutive FWFs or four consecutive IWFs or SBUs, we can first notice that near regions where four consecutive FWFs and four consecutive IWFs occurred may be found a higher density of apparent SBUs (Figure 69 – left). Where partial blocks intermittently in error started occurring, it can be noticed "on top" or "below" FWFs or three consecutive FWFs (Figure 69 – middle and left). Finally, an Intermittent VL is also clearly noticeable (Figure 69 – left).

During TC7, testing with neon (Ne), errors occurred on almost the first thousands of words of the memory, each address being in error at least six times during the test (Figure 70- left). Looking more closely to this test sequence, it appears that all read '1' operations failed on two consecutive elements of the test algorithm (each element passes through all memory addresses). Same typology of error occurred during TC12 under xenon (Xe) with an additional block of consecutive errors this time with not all bits of all words in error (Figure 70 - middle). In TC9, during irradiation under xenon (LET = 64.3 MeV.cm²/mg), a large block of errors occurred, with the current dropping down to 0 mA (as read on the power supply with low current accuracy) only for the duration of the errors' occurrence. During this event, the bit cross-section increased by at least two orders of magnitude compared to an exact similar run during the same test campaign on the same chip.

The focused X-ray microbeam test (at 8 keV) that was performed at a later stage also allowed to successfully reproduce this large block failure, when irradiation a different region of the memory periphery. In this register may be loaded the information regarding the size of the memory and perhaps also whether the memory can be accessed in 8 or 16 bit words. See the right bitmap section in Figure 70.

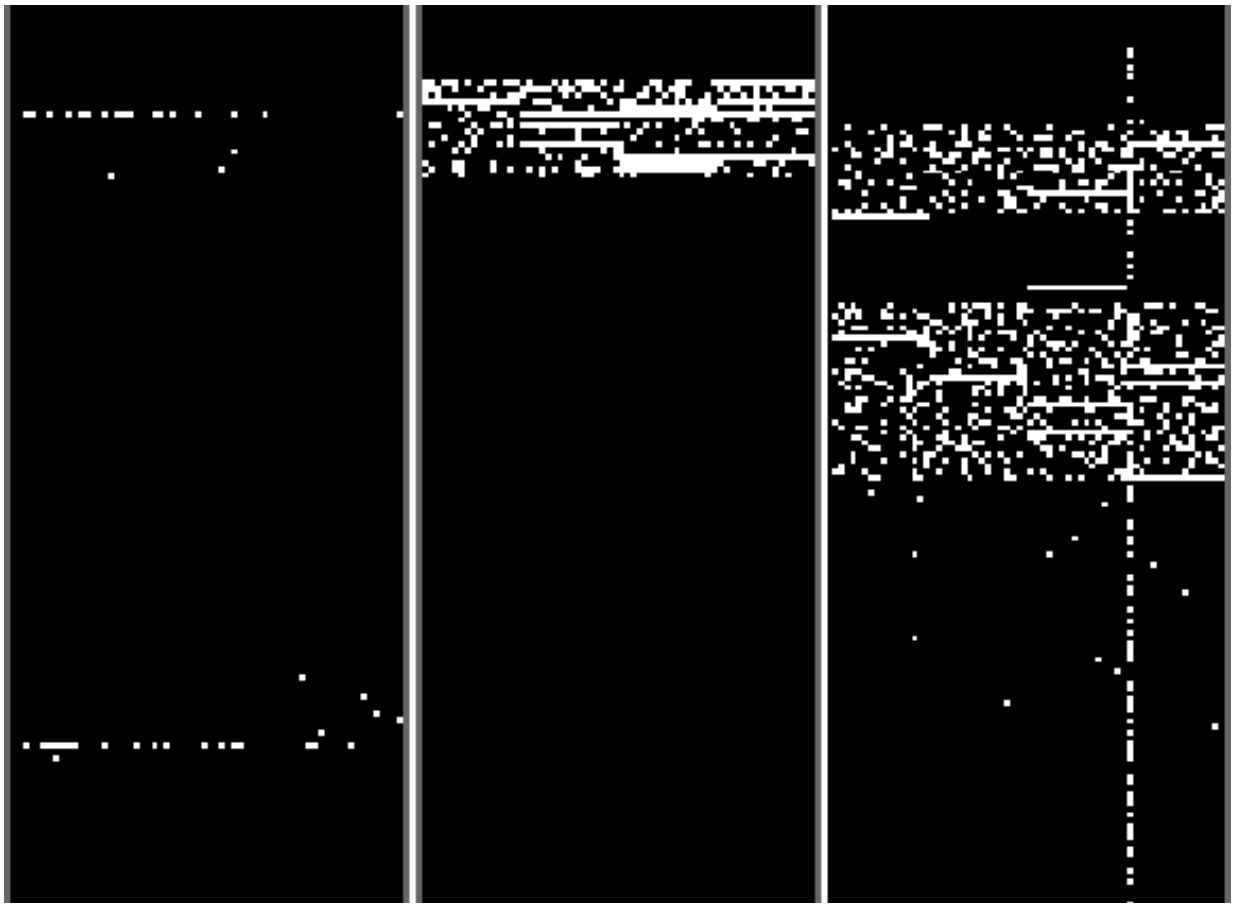


Figure 69: FRAM logical bitmap sections of during a pseudo-static solid '1' test irradiated under Xe (LET = 60 MeV.cm²/mg) showing different topologies of errors in three different blocks.

Comparing with March C-, Mats+, E and F tests, it appears that the number of partial blocks in errors is much higher than for March Dynamic Stress tests (Figure 71): this may explain the higher cross-section obtained for tests other than March Dynamic Stress.

Finally, it is worth mentioning two very strange behaviours, during TC9 and during TC5, that have not been reported in the literature to the best of our knowledge. During TC9 testing under xenon irradiation at a LET of 50.2 MeV.cm²/mg, during only one run in dynamic mode, although similar runs before and after occurred without this behaviour, the memory showed an extremely high number of errors, which continued after the end of the irradiation. A power cycle was required to recover from this malfunction. All read words were "00". In [Scheick, 2002], when testing an FM20L08, a similar behaviour occurred but during laser testing although this was not noticed by the authors during heavy-ion testing. The supply power current was unfortunately not monitored during this run. During TC5, a functioning device was tested at a flux of 1.0×10^4 part./(cm².s) and fluence of 1.0×10^6 part./cm² under March Dynamic Stress test, which resulted in a extremely high number of errors under itrogen (LET = 3.3 MeV.cm²/mg) and the memory had to be power cycled as errors were occurring after the beam was stopped.

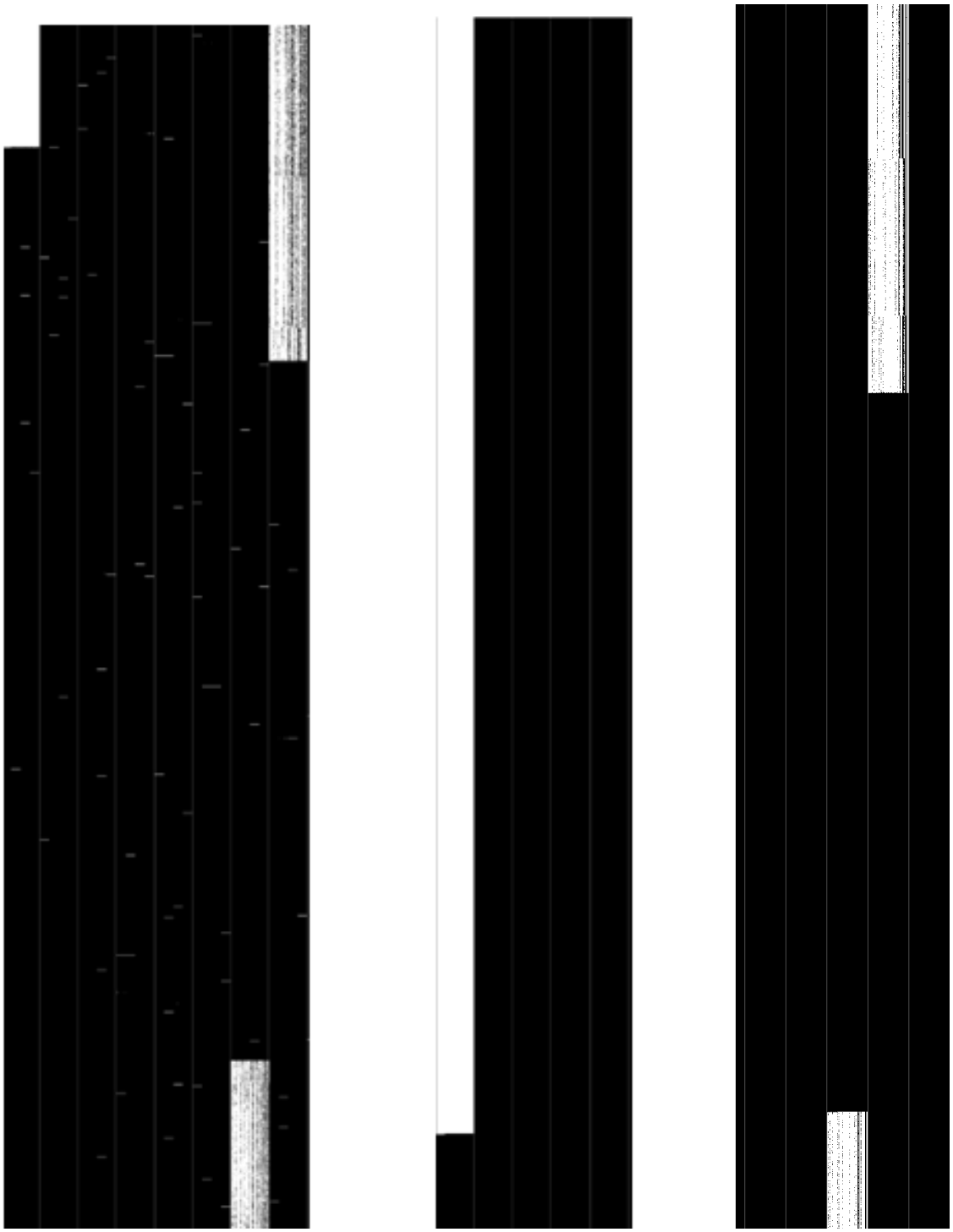


Figure 70: (Left) FRAM logical bitmap section showing the failure of the first thousands of addresses. (middle) FRAM logical bitmap section showing first few logical addresses in error, then a block with consecutive words failure with partial bit failure. (right) FRAM logical bitmap section reproducing a large block failure during X-ray microbeam irradiation on another region of the FRAM periphery.

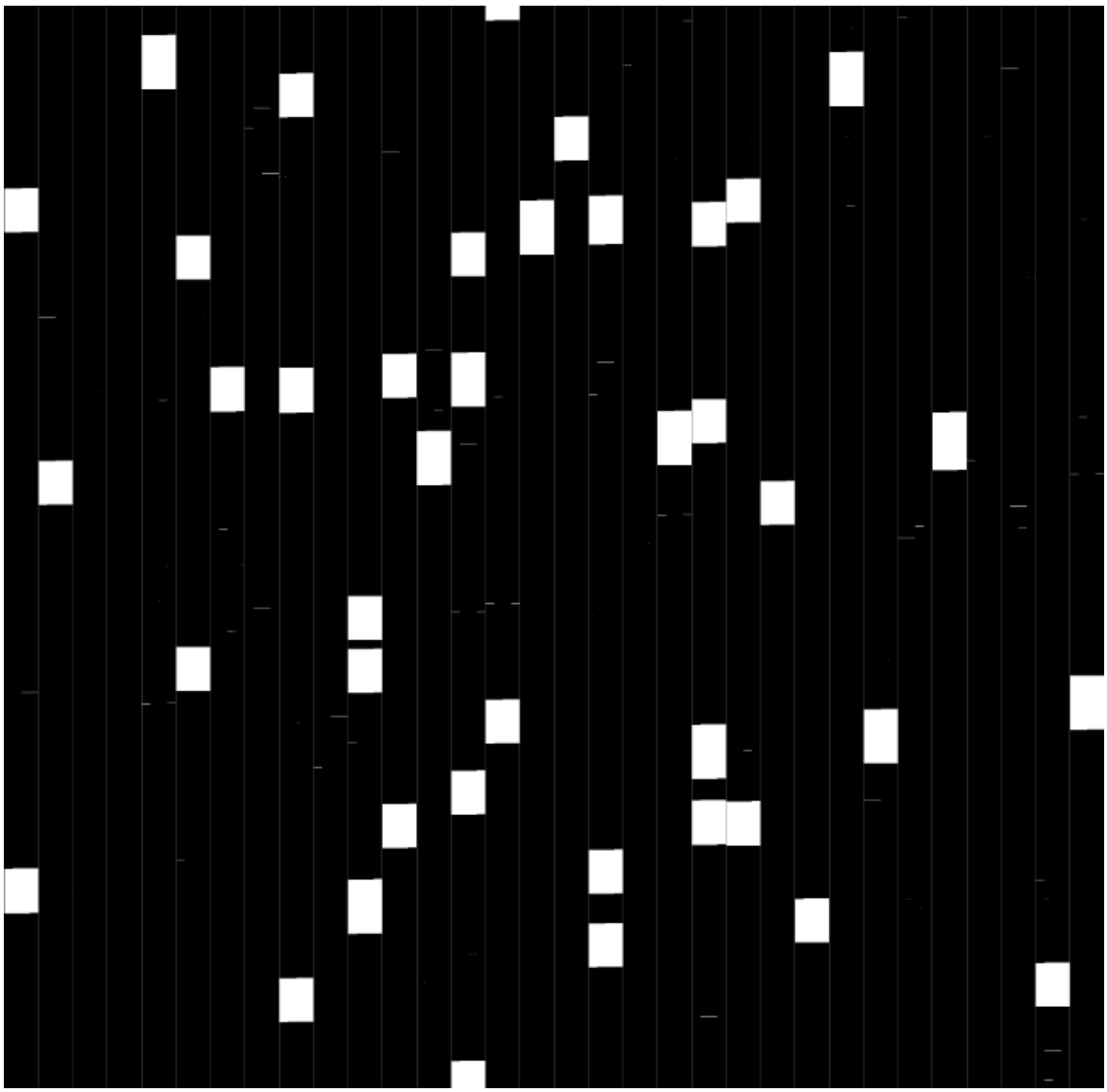


Figure 71: FRAM full logical bitmap when irradiation under Iron (Fe) during March C- dynamic test.

Further analysis was carried after generation of a logical bitmap as shown in Figure 72: the first word of every line is failing with sometimes the second word as well, leading to the explanation that the writing (or reading) of "FF" data background was not correctly done on the first and sometimes the second word of each line. After a power cycle, the memory was functional again and the next run, similar to the previous one with an order of magnitude lower fluence and flux, resulted, after 75 seconds, in an extremely large number of errors this time with a bitmap similar to Figure 70 (left), with write (or read) "00" operations that were not correctly performed. Several consecutive March Dynamic Stress tests were again made resulting in similar error topology, although in one test, errors started appearing similarly to
Figure 62. A checkerboard pattern was then run resulting in consecutive errors of all words proving that the write (or read) "00" operation was not performing correctly anymore. The memory was then discarded from the remaining tests.

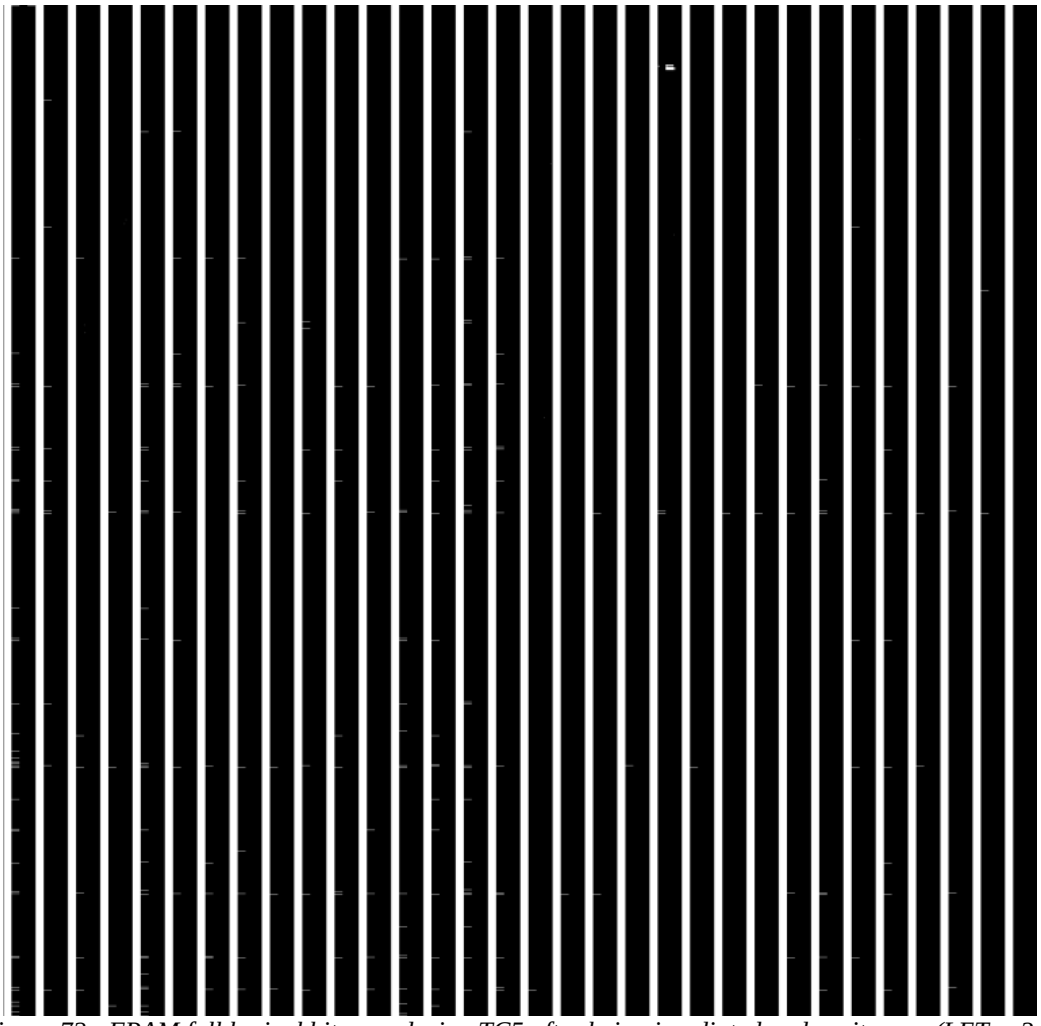


Figure 72: FRAM full logical bitmaps during TC5 after being irradiated under nitrogen (LET = 3.3 MeV.cm²/mg) under March Dynamic Stress mode testing. The white strips represent the words of each line fully in error (write or read "FF" not performed correctly). Sometimes the second word of each line appears to be also failing.

4.4.4.4 FRAM failure mode analysis

The analysis of the source of failures during irradiation requires a good knowledge of the internal structure of the memory and its architecture. Due to the lack of detailed information, failure mechanisms will be investigated on the base of reasonable hypotheses. Further information on the memory may provide more insights to confirm or not the assumptions provided here.

First of all, looking at "apparent" SBUs in static mode, it is clear that the errors are not due to the memory cell as no errors were found in unbiased mode. Possible failure of the periphery (address decoders, input buffers, output buffers, pre-chargers, sense amplifiers, etc.) due to lower resilience in biased mode may induced a higher number of errors: for example, the failure of an input/output buffer may induce an apparent higher number of bit failure that may not actually be present in the memory cell array. Recalling that SBUs and IWFs occurred during X-ray irradiation of FRAM peripheral circuitry, one of the possible explanations might be that some registers could be used to configure the spare elements (rows, columns, blocks) to replace parts of the cell array found defective during the manufacturing stage. In order to keep the non-volatile capability, these registers could probably be periodically loaded during normal operation or at each boot-up of the device. This hypothesis also explains why, in [Nuns, 2007], the authors noticed that no errors were detected if a power cycle was performed prior reading the memory: as the reconfiguration data are reloaded in those registers after a new boot, the correct content is restored.

However, tests under microbeam were performed in dynamic mode testing and not in static mode testing.The failure of a single access-transistor might also be a possible explanation, but it would lead to failures of other words sharing the same bit line in either solid ‘0’ or solid ‘1’ pattern (depending on which access transistor is faulty). One possible explanation may reside in the output buffer: it may be possible that the output buffer is made of SRAM cells (or other type of cell sensitive to SEEs) that may be flipped during static biased mode. Assuming that there are several buffers each one used for different regions of the memory, the first time the buffer is used, errors are detected independly of the accessed region in the cell array. The faulty buffer register may then be resetted afterwords and work properly for the subsequent reads.

Vertical lines in static mode testing, on the other hand, may be explained by a possible weakening of a sense amplifier, since the 1T-1C provides a lower charge on the bit line for sensing when compared to the 2T-2C cell configuration. But, it may also be possible that this type of error is due to an I/O buffer register failure (stuck-at bit) requiring a power cycle to be restored. The fact that the vertical lines are of the same length may be explained by the fact that they are limited to a region sharing the same failed peripheral circuitry, the remaining blocs not being affected. As those vertical lines are, in some cases, in regions with a high density of apparent SBUs, the weakening of an I/O buffer register may better explain the seen topology as the I/O buffer may also have other registered less weakened triggering those apparent SBUs. In other cases, the failure of an access transistor may also lead to the occurrence of errors in memory cells sharing the same BL, however in that case, there is not evident reason to see any higher density of SBUs in this area. The same explanation may be provided for the vertical lines of errors appearing in dynamic mode testing.

The peculiar horizontal lines of errors, shown in Figure 62, are accompanied with an increase of device current consumption and may be explained by localised micro-latchups occurring on a region of the memory. The regular pattern shown on the bitmap may be the result of the scrambling of the memory, possibly all failed words belonging to the same physical region of the memory. Depending on the scrambling of the memory, it may also be possible that all the failing words may belong to the same line: in that case, a power switch failure may also be a possible reason explaining the failure and increase in current.

The FWFs and IWFs (as well as the two consecutive WF, three consecutive WF and four consecutive WF, Full or Intermittent) are very likely to be linked to the architecture of this memory. The “page-mode operation” allowing to quickly read/write four consecutive words may be working as follows: when accessing one of the words of a four word-line, all the words (4*16 bits) as stored in the I/O buffer and the actual word is selected. Then while those words are in the buffer, then can be very quickly read without the need to access the actual content of the memory cell. Besides, it shall be recalled that reading of an FRAM cell is destructive and the content has to be re-written. Hence when all the four words are latched on the I/O buffer, those four words will have to be rewritten by the write controller. Hence, most likely the failure cause may either lay in the large I/O buffer or the write controller circuitry. An I/O buffer temporary failure will be observed through a read operation, while a write controller error will be detected only with a the subsequent read operation in the same memory location. It was also shown that the X-ray microbeam was able to reproduce some IWFs (up to four bit upsets in four consecutive words) and this occurred at least once for the beam hitting the central spine. However, FWFs were not successfully triggered, thus it cannot be proven whether FWFs and IWFs may only originate by failures in the same periphery region or elsewhere like page buffers, and also whether they correspond to the same fault mechanism or not. Further testing on the page buffer would allow a better understanding of this aspect. However, assuming that the scanned region of the periphery corresponds to the same functionality, the failures may result in various mapping in the cell array either being SBUs, apparent IWFs (actually composed of SBUs placed in neighbouring bits and occurring at a different time) or intermittent VLs.

Full and partial block failures show consecutive addresses failing. Blocks sizes appear to be of rather defined size. Due to the scrambling of the memory, it is very likely that the consecutive words are not close to each other. Hence, failure of I/O buffer, write controller, and other periphery is less likely.

One of the favoured reasons may be a failure of the address decoder for several consecutive addresses. This hypothesis is reinforced by the fact that the appearance of block is higher for March C- and Mats+ tests which have a higher logic switching activity than the March Dynamic Stress test.

Very large block errors were successfully reproduced by X-ray microbeam testing when irradiating another part of the periphery. It is probable that one of the main sources of those large errors may arise from failure in the electronics used for the configuration of the memory.

Finally, regarding the unusual FRAM behaviours, it is important to notice that:

- the memory includes a low voltage monitor blocking the access to the memory array when V_{DD} drops below 2.7V;
- the memory incorporates a software-controlled write protection state machine that can be switched on only after a very specific set of successive commands;
- the memory has a sleep mode that is controlled by an external pin and is logically connected to the CE pin with an AND gate.

All these malfunctions may result in unusual behaviour such as those detected during TC5 and TC9. Further possible fault mechanisms may fit for the same observed errors, and one of them may be the failure of the command signals of the reference voltage provided to the Plate Line (PL), which may be detrimental to the proper reading of the content of a cell. As far as the unusual behaviour detected in TC5 is concerned, as during test with checkerboard data background, only the bits at '0' were not properly written or read. This can be possibly due to the fact that the PL could not be set to 0V for a proper achievement of the write '0'. If the PL was not able to be set to V_{DD}, then all read operations would be failing and all words would be in error.

Table 13 summarizes the various types of error topology resulting from heavy-ion irradiation and analyses of logical bitmaps. All the above mentioned possible failure mechanisms, although possible, may be or not the exact cause of the failure. It is possible that other malfunctions may also induce the errors described above or even a combination of effects. The knowledge of the actual location of the errors as well as a deep understanding of the architecture and circuitry may allow to refine the above mentioned hypotheses, which are provided as first axes of reflexion into the failure of the tested FRAM memory during heavy-ion testing.

4.5 FRAM test results based on proton testing

4.5.1 High energy protons

High-energy protons testing was performed at the Paul Scherrer Institute (PSI) using the PIF facility and located in Switzerland. Tests were carried in open air at ambient temperature. The memory chips did not require any delidding since protons at energies above 50 MeV have a large enough penetration range enabling to reach the die with negligible energy loss.

Due to issues with the beam in the main cyclotron, the testing time planned for memory testing was drastically reduced, and hence, solely a minimum set of tests was possible in order to test the FRAM memory under high-energy protons. A single component was tested along with one 3D Plus FRAM memory. Table 14 summarised the tests performed on the FRAM memories. The fluence reached for each run was 10^9 protons/cm² except one run at 200 MeV for which the fluence was increased to $5 * 10^{10}$ protons/cm². The dynamic March C- test was the selected dynamic test as, under the light of the heavy-ion test results, this test is able to stress the most FRAMs.

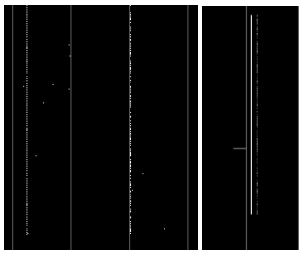
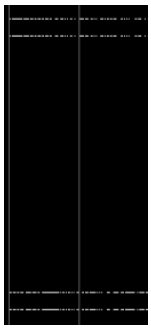
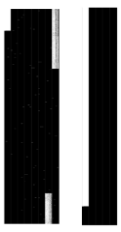
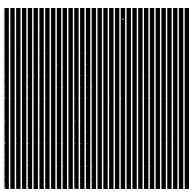
Error topology picture	Error topology name	Type of test	Possible failure mechanisms
	SBU	Static and Dynamic	• Due to peripheral circuitry (registers) • Output buffer (SEU in internal register)
	IVL/CVL (Intermittent and Continuous Vertical Lines)	Static and Dynamic	• periphery registers likely used for spare allocations. • Access transistor if not high SBU density in the failure area • Weakening of Sense Amplifiers • I/O buffer register failure
	Double error lines	Static @ 45°	• Micro latch-ups • Power switch failure
	FWF/IWF (Full and Intermittent Word Failure)	Dynamic	• IWF due to registers weakening • I/O buffer • Re-write controller
	PBEE/PBIE (partial block entirely/intermitte ntly in error)	Dynamic	• Address decoder
	Large block errors	Dynamic	• Registers used for configuration • Failure of Plate Line reference voltage • Address decoder • I/O buffer
	Temporary stucked bits in large part of entire memory and other unusual errors	Dynamic	• Registers used for configuration • Reference voltage of the PL

Table 13: Summary of FRAM logical bitmaps error topology when testing against heavy-ions/X-ray microbeam.

Memory	Energy (MeV)	Total fluence (part./cm²)	Type of test	Nb of runs
Standalone FRAM	200	5.9×10^{10}	Dynamic March C-	5
Standalone FRAM	200	4.2×10^{9}	Static checkerboard	4
Standalone FRAM	50.8	1.0×10^{9}	Dynamic March C-	1
Standalone FRAM	50.8	1.0×10^{9}	Static checkerboard	1
3D plus FRAM module	200	1.0×10^{9}	Dynamic March C-	1
3D plus FRAM module	200	1.0×10^{9}	Static checkerboard	1

Table 14 : Types of tests conducted on FRAM memories at the PSI Switzerland facility for high energy protons.

Results showed no error at all in all runs performed on both memory devices. As results showed no error even in static biased mode, and due to time constraints, unbiased testing was not conducted as it was already shown during heavy-ion testing that the memory was more robust (no events recorded) in unbiased mode.

Confidence was very high that the memory was correctly positioned under the beam (three cm diameter beam ensure a high confidence that the memory was irradiated). Besides, after irradiation, functional checks were carried making sure that the component and test controller were nominally working. Furthermore, between each run, a functional check with injected errors was carried making sure that the test set-up was properly working and the memory correctly responding. Besides, the tested FRAM memories, during heavy-ion campaigns and protons campaigns were from the same assembly lot which was directly shipped by the manufacturer (Cypress semiconductors).

As the LET of proton nuclear interaction in silicon can reach up to 15 MeV.cm²/mg [Yu, 2015], and considering the very low heavy-ion LET threshold in dynamic mode (< 1.8 MeV.cm²/mg), the high energy proton test results appear to be in contradiction with the heavy-ions test outputs. The answer may rely in statistics: in [Nuns, 2007] proton testing was conducted at 200 MeV up to a cumulative fluence of $3 * 10^{11}$ protons/cm² and got an overall total error of just six errors. After an additional investigation, test results were found in [O'Bryan, 2008], showing a cross-section at 200 MeV of less than 10^{-10} cm²/device. As the total cumulated fluence reached less than $6 * 10^{10}$ cm² on our component, it is statically possible not to have collected enough fluence to trigger an error. The cross-section calculated in [O'Bryan, 2008], will be used for the memory SEE rate calculation due to protons for the MTCube mission.

Finally, regarding latchups, no SEL were recorded during the proton test campaign.

4.5.2 Low energy protons

Low Energy Proton (LEP) testing has not been performed due to time constraint on this memory. It is nevertheless very likely that the ferroelectric immunity to heavy-ion implies that direct ionization is not a concern (as the maximum electronic LET of LEP is 0.45 MeV.cm²/mg [Yu, 2015]).

Regarding the peripheral circuitry of the memory, considering that it is made with 130 nm CMOS technology, it is not susceptible to direct ionization that seem to occur only for technologies below 90 nm.

4.6 Conclusion on FRAM testing

Heavy-ion testing confirmed that the static SEU cross-section in FRAM devices is low due to the intrinsic radiation hardness of the storage cell based on ferroelectric layer. Taking the example of the SRAMs memory in static mode presented in chapter 3, the FRAM bit saturation cross-section is more than three orders of magnitude lower than the 90 nm and 65 nm SRAMs and, if we consider the bit cross-section including the VL, the difference is of two orders of magnitude. Unbiased tests between an effective LET of 32.1 and 84.8 MeV.cm²/mg at the surface of the chip resulted in no observed error. Nevertheless, when the memory is biased, errors caused by temporary radiation cumulative effects may occur during high-fluence runs in static mode tests, leading to a non-negligible number of bits flips. Those errors disappeared after a power cycle or a simple scrubbing of the memory. On the other hand, upset rates during dynamic mode testing are much higher due to errors in the control logic and require additional mitigation techniques to improve their radiation behaviour. The dynamic SEU bit cross-section values are in the same order of magnitude as those of commercial 90 nm SRAM dynamic test SEU cross-sections measured in [Tsiligiannis2, 2014]. Further tests are required to understand the impact of the fluence on the cross-section, as well as to confirm latchup immunity at elevated temperatures. Additional knowledge on the scrambling may allow a better understanding of the impact of the peripheral circuitry by the analysis of the physical bitmaps. Further analyses of logical bitmaps has provided some more insight into possible failure mechanisms of this memory.

Regarding proton testing, low energy testing was not performed but appears not to be critical regarding the overall sensitivity characterisation of the memory. Considering the high energy testing campaign, the gathered fluence seems to be not large enough to conclude that the memory is immune to protons. Some research after testing showed a very low proton SEU cross-section that will be used for the estimation of the in-orbit error rate calculation in chapter 5.

SEL have not been observed although a possible µ-SEL event was noticed only once during TC1. However, the current has not been precisely monitored during the runs but no large current variations were noticed on the power supply used for FRAM testing. Although temperature may impact the sensitivity of the memory to SEEs, the temperature inside MTCube is not supposed to present large variations. Dose levels during the two year nominal mission in LEO is far less than what would induce malfunctions in new FRAMs although in our work no actual TID test has been performed as it is out of the scope of the current study. Finally, imprinting issues as mentioned above are not of concern, since dynamic tests implies that the content of the stored memory cell alternates between ‘1’ and ‘0’, while regarding static testing, the data background was changed between the various static test runs.

4.7 Bibliography

[Benedetto, 1991] J. M. Benedetto *et al*., "Radiation evaluation of commercial ferroelectric nonvolatile memories," in *IEEE Transactions on Nuclear Science*, vol. 38, no. 6, pp. 1410-1414, Dec 1991.

[Buck, 1952] Dudley A. Buck, "Ferroelectrics for Digital Information Storage and Switching." Report R-212, MIT, June 1952.

[Dahl, 2015] B. A. Dahl *et al*., "Radiation Evaluation of Ferroelectric Random Access Memory Embedded in 180nm CMOS Technology," *Radiation Effects Data Workshop (REDW), 2015 IEEE*, Boston, MA, 2015, pp. 1-6.

[Dilillo, 2005] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, S. Borri, M. Hage-Hassan, “Efficient March Test Procedure for Dynamic Read Destructive Fault Detection in SRAM Memories, ” *in JETTA*, Vol. 21, n° 5, pp. 551-561, Oct. 2005.

[Dilillo2, 2005] L. Dilillo, P. Girard, S. Pravossoudovitch, A. Virazel, and H.H. Magali Bastian, “Data Retention Fault in SRAM Memories: Analysis and Detection Procedures,” *IEEE VLSI Test Symp. Proc*, 2005.

[Gerardin, 2010] S. Gerardin and A. Paccagnella, “Present and future non-volatile memories for space,” *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3016–3039, Oct. 2010.

[Gu, 2014] Ke Gu, Ping Li, Wei Li, Xue Fan, Yahong Zhai, Bin Hu, Yang Liu, Zuxiong Li, “Total ionizing dose tests on ferroelectric random access memories, ” *in IEEE EDSSC*, pp.1-2, June 2014.

[Gupta, 2016] V. Gupta *et al*., "Heavy-Ion Radiation Impact on a 4 Mb FRAM Under Different Test Modes and Conditions," in *IEEE Transactions on Nuclear Science*, vol. 63, no. 4, pp. 2010-2015, Aug. 2016.

[Kamp, 2005] D. A. Kamp, A. D. DeVilbiss, G. R. Haag, K. E. Russell and G. F. Derbenwick, "High density radiation hardened FeRAMs on a 130 nm CMOS/FRAM process," *Symposium Non-Volatile Memory Technology 2005.*, Dallas, TX, 2005, pp. 4 pp.-51.

[Katz, 1999] R. Katz *et al*., "The effects of architecture and process on the hardness of programmable technologies," in *IEEE Transactions on Nuclear Science*, vol. 46, no. 6, pp. 1736-1743, Dec. 1999.

[MacLeod, 2009] T. C. MacLeod, W. H. Sims, K. A. Varnavas, R. Sayyah and F. D. Ho, "Satellite test of radiation impact on Ramtron 512K FRAM," *Non-Volatile Memory Technology Symposium (NVMTS), 2009 10th Annual*, Portland, OR, 2009, pp. 24-27.

[Marinescu, 1982] M. Marinescu, “Simple and Efficient Algorithms for Functional RAM Testing, ” *in Proc. Int. Test Conf.*, 1982, pp. 236-239.

[Nguyen, 2001] D. N. Nguyen and L. Z. Scheick, "TID testing of ferroelectric nonvolatile RAM," *Radiation Effects Data Workshop, 2001 IEEE*, Vancouver, BC, 2001, pp. 57-61.

[Moore, 1995] R. A. Moore and J. M. Benedetto, "Ionizing radiation-induced asymmetries of the retention characteristics of ferroelectric thin films," in *IEEE Transactions on Nuclear Science*, vol. 42, no. 6, pp. 1575-1584, Dec 1995.

[Nuns, 2007] T. Nuns, S. Duzellier, J. Bertrand, G. Hubert, V. Pouget, F. Darracq, J. P. David, and S. Soonckindt, “Evaluation of recent technologies of non-volatile RAM,” in *RADECS*, Deauville, 2007, pp. 1–8.

[O’Bryan, 2008] M. V. O'Bryan *et al*., "Compendium of Recent Single Event Effects Results for Candidate Spacecraft Electronics for NASA," *2008 IEEE Radiation Effects Data Workshop*, Tucson, AZ, 2008, pp. 11-20.

[Philpy, 2004] S. T. Philpy, D. A. Kamp and G. F. Derbenwick, "Nonvolatile and SDRAM ferroelectric memories for aerospace applications," *Aerospace Conference, 2004. Proceedings. 2004 IEEE*, 2004, pp. 2294-2299 Vol.4.

[Scheick, 2002] L. Scheick, S. Guertin, and D. Nguyen, ―Single Event Effect Evaluation of FeRAM Memories for Space Applications,‖ presented at the Non-volatile Memory Technology Symposium, 2002.

[Schwank, 1990] J. R. Schwank, R. D. Nasby, S. L. Miller, M. S. Rodgers, and P. V. Dressendorfer, “Total-dose radiation-induced degradation of thin film ferroelectric capacitors,” *IEEE Trans. Nucl. Sci.*, vol. 37, no. 6, pp. 1703–1712, Dec. 1990.

[Tsiligiannis, 2014] G. Tsiligiannis, “Soft Errors in Memory Devices: Novel Methods and Practices for Dynamic and Static Testing”, Thesis manuscript, LIRMM/Université Montpellier, Sept. 2014.

[Tsiligiannis2, 2014] G. Tsiligiannis, L. Dilillo, V. Gupta, A. Bosio, P. Girard, A. Virazel, H. Puchner, A. Bosser, A. Javanainen, A. Virtanen, C. Frost, F. Wrobel, L. Dusseau, F. Saigné, “Dynamic Test Methods for COTS SRAMs,” *IEEE Trans. Nucl. Sci.*, vol.61, no.6, pp.3095-3102, Dec. 2014.

[Tsiligiannis3, 2014] G. Tsiligiannis, L. Dilillo, A. Bosio, P. Girard, S. Pravossoudovitch, A. Todri, A. Virazel, C. Frost, F. Wrobel, F. Saigné, “Multiple-Cell-Upsets on a

commercial 90nm SRAM in dynamic mode", *IEEE Trans. Nucl. Sci.,* pp.1, 4, Sept. 2013.

[Yu, 2015] Q. Yu *et al*., "Experimental Study of 0.18µm and 65nm SRAM SEUs Induced by Heavy-Ions, High Energy Protons and Low Energy Protons on Orbits," *2015 15th European Conference on Radiation and Its Effects on Components and Systems (RADECS)*, Moscow, 2015, pp. 1-5.

[Zanata, 2008] M. Zanata, N. Wrachien and A. Cester, "Ionizing Radiation Effect on Ferroelectric Nonvolatile Memories and Its Dependence on the Irradiation Temperature," in *IEEE Transactions on Nuclear Science*, vol. 55, no. 6, pp. 3237-3245, Dec. 2008.

[Zhang, 2015] Z. Zhang *et al*., "Single Event Effects in COTS Ferroelectric RAM Technologies," *Radiation Effects Data Workshop (REDW), 2015 IEEE*, Boston, MA, 2015, pp. 1-5.

Chapter 5

Single Event Effect testing of NAND Flash memory

5.1 Introduction on NAND Flash

In the past, satellites have been using SSD (Solid State Disk), EPROM and E²PROM as non-volatile memories. Then, with new memories being built for Earth applications, their use has started to increase on satellites: this is the case for NAND Flash memories as well as NOR Flash memories. But these memories are not inherently radiation tolerant: for example, issues have been reported on Flash memories on-board the Opportunity rover, and more recently the Curiosity rover, that may be due very likely to radiation effects. Besides, more and more aggressive integration especially of NAND Flash memories with feature size of 25 nm and below, have to be constantly qualified for space applications as their sensitivity to SEE evolves (usually increases) as it will be presented below.

For this reason, one type of NAND Flash memory, along the previously mentioned FRAM memory, has been chosen to be part of the MTCube non-volatile memory payload experiment. Similarly to the previous chapter, the technology used for the non-volatility properties of the NAND Flash will be first presented. Then, after a review of the current state-of-the-art with respect to radiation testing, the SEE test results will be presented.

5.2 Description of Flash memories

5.2.1 Introduction

The first Flash memories emerged in the sixties with the scope to replace E²PROM. The advantage of a Flash memory compared to an E²PROM memory (both being electrically erasable), is that the time for erasing the data is much lower for a Flash memory resulting in an overall increase of the speed. Flash memories allow combining the high density of EPROMs with the capability to electrically erase the memory like E²PROMs. But, on the other hand, Flash charge pumps slow the access time by several orders of magnitude compared to SRAMs

There are two main Flash architectures as depicted in Figure 73: NOR and NAND Flash memories, which were developed by two different companies: Toshiba for NAND, Intel for NOR. NOR Flash memories, similarly to RAM memories, allow a random access to words: each floating gate cell (FG) can be access separately because each FG is connected to a word line (WL) and bit line (BL). This has the advantage of reducing the access time to read or write a specific word at the expense of a small memory cell density as each cell needs to be separately accessed. On the other hand, NAND Flash are denser (40% gain) as each cell node does not have to be directly connected to the memory network; reading/writing is performed page by page. As can be seen in Figure 73, several FGs are in serie and connected to the BL; it is not possible to access individually each FG. This, in turns, increases a lot the read/write access time to an individual word but allows being very efficient in sequential writing/reading. Nevertheless, in both architectures, erasure is performed per block (a block containing several pages). NOR Flash memories are usually guaranteed fault-free whereas this is not the case for NAND Flash memories which can have a very small technology node in order to increase storage

capacity: the use of NAND Flash requires the use of error correction features, allowing more aggressive scaling. FLASH endurance is limited to 10^4 to 10^5 erase/program cycles [Gerardin, 2013].

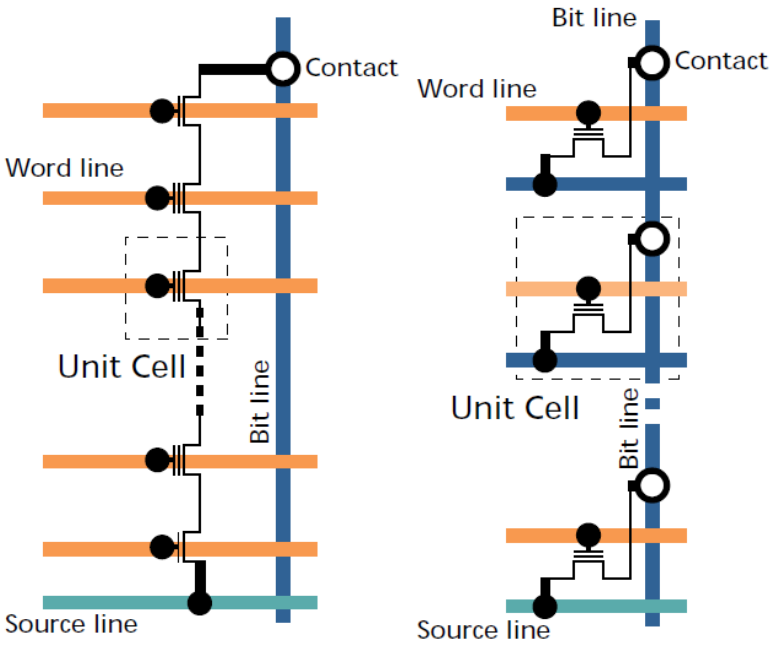


Figure 73: Architecture of NAND (left) and NOR (right) Flash memories [Micron, 2006].

Regarding space applications, Flash memories are used in solid-state recorders, since they are non-volatile and do not need refresh cycling [Irom, 2010], which is the case with DRAM based solid-state recorders [Nguyen, 2003]. Depending on their architecture, they may be used either as boot software or storage for large amounts of experimental data. In principle, Flash memory cells are more robust than other memories, like SRAMs for example, but due to the complexity of Flash internal architecture, they may suffer various types of malfunctions as it will be presented in section 5.3. Nevertheless, they are still attractive as RadHard non volatile memories are limited to typically 64 Mb of total capacity[Gerardin, 2013].

The current study on Flash memory will solely focus on NAND Flash memory in retention mode, as this type memory is selected for the science experiment study of the MTCube mission.

5.2.2 Description of NAND Flash memories

5.2.2.1 Flash memory cell

Flash memories non-volatility feature comes from the use of a Floating Gate (FG) made of polysilicium and sandwiched between two oxides: the control oxide above, on the top of which the actual gate is located and the thin (< 10 nm) tunnel oxide below, which lays on the substrate of the NMOS transistor (see Figure 74 - Left). The control oxide is usually an ONO (Oxide-Nitride-Oxide) stack. Thanks to this configuration, the FG is able to store electrons or holes and confine them in the FG (thanks to the oxides acting as potential barriers) even when the NMOS transistor is turned OFF. The amount of charge stored in the FG will affect the threshold voltage of the transistor which will require higher or lower voltage on the gate to activate the transistor's canal.

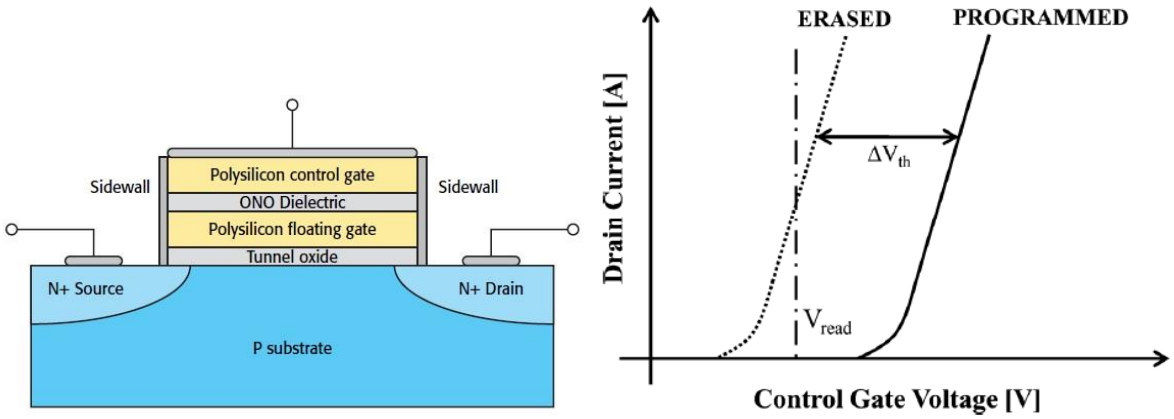


Figure 74: (Left) Flash memory cell configuration; (Right) Floating Gate I-V curve in programmed and erased state [Gerardin, 2013].

By convention for Single Level Cells (SLC), when electrons are trapped in the FG, this state corresponds to a binary '0' (the FG is charged). Conversely, a binary '1' is defined as the case when the FG is empty; the electrons being removed. There are two ways to program a FG cell [Gerardin, 2013]:

1. By injecting electrons over the potential barrier of the tunnel oxide (hot electrons). Electrons from the channel acquire energy by turning the gate and the drain ON and near the drain, a small number of electrons have enough energy to pass over the $Si/Si0_2$ barrier of the tunnel oxide and get trapped in the FG;
2. By injecting electrons/holes through the barrier (Fowler-Nordheim tunnelling) which is more efficient but slower. By switching ON the gate voltage and setting the substrate voltage to 0V, electrons are able to tunnel through the tunnel oxide and reach the FG.

Conversely, erasing a FG cell is performed by setting a high voltage on the substrate while keeping the gate voltage at 0V and drain and source node at high impedance: the resulting effect is the electron tunnelling back to the substrate.

By programming or erasing the cell, the transistor's I_{ds} - V_{gs} curve is modified and so is the voltage threshold as depicted in Figure 74 (right). By setting a voltage level between the voltage threshold for an erase and a programmed state, it is possible to know which is the according bit information stored in the FG cell by measuring the drain current (I_{ds}). In NAND Flash memories, reading implies that the unselected cells in the string must allow accessing the read-cell (high pass-through voltage to switch ON programmed and erase cells) [Gerardin, 2013].

Multi Level Cells (MLC) as opposed to SLCs, allow storing four (or more) bits in a single FG. This requires having very precise means of storing a given quantity of electrons in a floating gate as well as being able to sense more accurately the voltage threshold during a read operation; the noise margin being hence reduced. Hence, MLC are not widely used, as of today in space applications.

5.2.2.2 NAND Flash memory architecture

Besides the FG constituting the memory cell array, NAND Flash memories are constituted of several other circuitry similarly to other memories such as sense amplifiers, I/O buffers, address decoders, bit lines, word lines. Nevertheless, these circuitries are not enough to provide all the basic functions: the high voltage required for programming, erasing or by-passing a memory cell during a read operation requires the use of charge pumps as depicted in Figure 75.

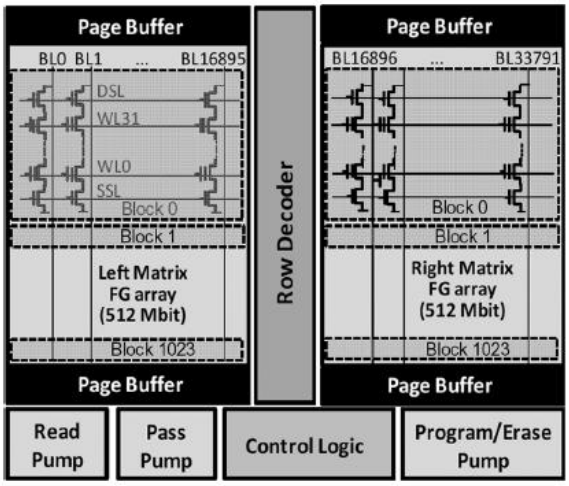


Figure 75: FLASH memory simplified layout with some of the peripheral circuitry [Bagatin, 2009].

In NAND Flash memories, cache registers (likely SRAM based) are present as well. They have the size of a page, which is constituted of a row of FG cells connected in serial and sharing the same bit line. Programming is performed at a page level in a NAND Flash. On the other hand, an erase operation is performed at a block level, which is constituted of several pages.

The I/O bus allows communicating with a Flash memory, but, as opposed to NOR Flash memories, the address and data bus are multiplexed on the same bus. This, along with other complex operations such as the dedicated circuitry for checking whether an erase or program operation has been properly implemented results in very complex operations and algorithms which are controlled by an internal microcontroller (operations implemented in state machines).

The "program (resp. erase) verify" functions work by setting gate voltage slightly above (resp. below) the read voltage (Figure 76). This is due to the fact that in reality the different erase/program voltage thresholds of each of the million FG cells are not exactly the same but follow a Gaussian distribution [Gerardin, 2013].

The complex internal circuitry of a NAND Flash memory, results in difficulties to understand the failure mechanisms due to radiation as many different parts may be affected at the same time besides not having thorough information regarding the peripheral circuitry and microcontroller.

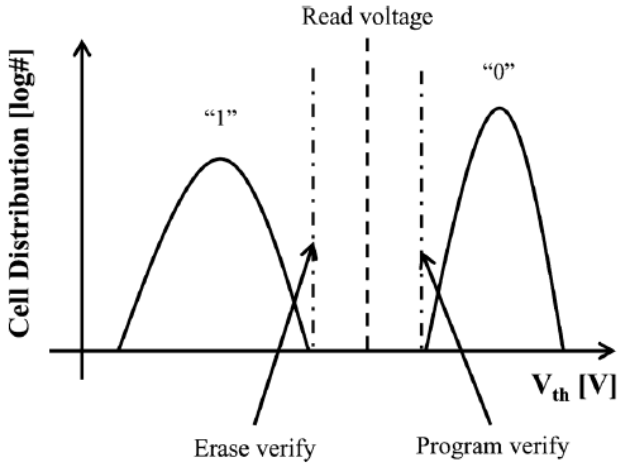


Figure 76: NAND FLASH read, erase verify, program verify voltage levels [Gerardin, 2013].

5.2.3 FLASH memory under study

The Device Under Test (DUT) is a 32 Gib Asynchronous Single-Level Cell (SLC) NAND Flash memory manufactured by Micron Technology (MT29F32G08ABAAA). The nominal operating voltage is 3.3V. The DUT is made of one Logical Unit (LU) itself constituted with two planes; each plane is made of 2048 blocks; each block is made of 128 pages, and each page is able to store one 8-bit word per column, with a total of 8192 columns per page. Extra bits are dedicated to One-Time Programmable (OTP) applications, but were not used in the current study. Four specimens were used and delidded before the irradiation tests using chemical means (Figure 77). All tested memories passed functional tests and were fully operational prior to the tests. According to [Irom, 2012], in which a similar memory was tested, the feature size is 25 nm.

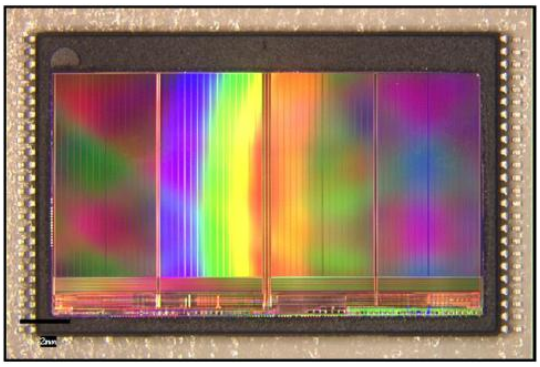


Figure 77: Picture of a delidded NAND FLASH specimen used for heavy-ions irradiations.

Three test campaigns were conducted on the target Flash devices, as summarised in Table 15. All tests were carried at normal beam incidence angle with respect to the die surface. The first test campaign was carried at the GANIL facility in Caen, France on two specimens. The primary xenon (Xe) beam was degraded in order to reach a LET (Linear Energy Transfer) of 26.75 MeV.cm²/mg at the surface of the DUT. Tests were performed in air. The second test campaign was carried at the RADEF facility at the University of Jyväskylä, Finland. Tests were carried on two specimens in vacuum, from 60 down to 1.8 MeV.cm²/mg. Fluences ranged from 1.0×10^4 to 1.5×10^5 cm^{-2} for each individual test, during both irradiation campaigns. Concerning static buffer testing (tested at RADEF), fluence ranged between 6.2×10^2 and 1.0×10^5 cm^{-2} per test. At both facilities the beam homogeneity is estimated to be +/- 10% or better over the device area. The final test campaign was conducted at PSI in Switzerland: biased and static tests were made (time was too short unfortunately for unbiased testing). Fluence ranged between 1.0×10^9 and 1.0×10^{11} cm^{-2} per test.

The DUTs were mounted on PCB cards and connected to FPGA-based controllers. The FPGAs, although located in the chamber, were placed aside from the beam line to ensure reliable operation. During each test run, when a bit error was detected, the erroneous word along with other information such as the address and the timestamp was transmitted to a computer, for storage and data processing.

The memory devices were tested under three different test modes: the *static (or retention) mode*, the *static buffer mode* and the *dynamic mode*. In static mode, a known data pattern (either all '1', all '0', or "checkerboard" patterns) is stored in the memory, which is then irradiated. Subsequently, a comparison is performed between the pre-irradiation and post-irradiation data to detect the bit flips. Due to the very large capacity of the memory, only 512 Mb out of 32 Gb were considered for the tests. In static buffer mode, the content of one page (64 kib) is stored on the memory data register prior to irradiation, and then the content of the register is read at the end of the irradiation.

Several operations (erase, write, read) were performed in between runs, before and after Power Cycles (PC), to sensitize and observe the errors occurring during the test runs but also to ensure that the memory was error free prior to the next run.

	Ion	Energy (MeV)	Effective LET (@ Top of BEOL) (MeV/(mg/cm^2))	Range to Bragg Peak (µm)
TC9 (GANIL)	Xe	2381	26.8	700
TC10 (RADEF)	N	139	1.8	202
	Fe	523	18.5	97
	Kr	768	32.1	94
	Xe	1217	60.0	89
TC15 (PSI)	Proton	200	3.6×10^{-3}	138630
		101	5.8×10^{-3}	42360
		51	9.7×10^{-3}	12620

Table 15: Heavy-ion cocktails used at the different facilities. TC stands for Test Campaign. TC9 values were provided by GANIL they include the ion initial energy passing through 10 µm of Inox and 61 mm of air, TC10 values calculated with SRIM. TC15 are the tests conducted at PSI. The range to Bragg peak is the distance travelled by the ion from the surface of the die to the Bragg peak.

5.3 Radiation effects in FLASH memories

Due to their internal complexity (charge pump, internal microcontrollers, cache registers...) with respect to RAM memories, it is quite difficult to study these memories, as lot of internal elements are generally not known. In this section, the focus will be on reliability issues in Flash memories related to SEE and TID radiation.

5.3.1 Total Ionizing Dose

Only programmed cells are sensitive to TID, some errors occurred in non-programmed cells at low dose rate in [Oldham, 2006] but were intermittent, and, according to the authors, not necessarily due to radiation effects. Erased cells show more robustness against TID although at the device level some errors may occur but attributed to circuitry or buffer regions [Irom, 2009]. In fact, in [Oldham, 2008], devices in unbiased mode showed to be able to withstand several hundreds of krad($Si0_2$).

TID effects on FG cells are mainly due to three mechanisms [Bagatin, 2011]. The first mechanism is positive charge injection in the FG, which neutralise the negative charge stored in FGs. These positive charges are induced by radiation in the surrounding oxides which are then injected into the FG due to the negative charges stored in the FG distorting the electric field in the oxide [Gerardin, 2013]. The second mechanism is due to photoemission of the stored FG carriers (charge loss): due to impinging radiation, some electrons stored within the FG acquire enough energy to leave the FG. This mechanism is higher at high dose rate [Cellere, 2004]. The last mechanism, which contributes, however to a smaller extent, to TID effects is charge trapping in the oxide layers surrounding the floating gate, in particular in the thin tunnel oxide. A small part is due to charge trapping/interface state generation [Bagatin2, 2009] in the surrounding oxides [Cellere, 2004]. All these mechanisms contribute to the reduction of the threshold voltage due to neutralization or loss of charge stored in the FG. Although positive charge injection and photoemission induce a permanent voltage shift, charge trapping in the oxide induced voltage threshold is reversible (due to charge detrapping and charge neutralization within the oxide) [Bagatin, 2009]. Erased cells do not have any charge stored in the FG. This reason explains why programmed FGs are more sensitive than erased FGs which can withstand up to 1 Mrad($Si0_2$).

The overall effect of TID on the FG cells is a shift towards lower levels of the Gaussian distribution of the threshold voltages of each cell: hence, as soon as the lower limit for reading a memory is reached,

the increase in errors may occur exponentially if no erase/program of the cell is performed [Gerardin, 2013]. Conversely to [Oldham, 2008], Gerardin et al. reveal only a small discrepancy between biased and unbiased FG cells. Schmidt and al. showed in [Schmidt, 2008] that read errors started occurring in biased mode around 20 to 30 krad(Si) showing a gain of robustness but also mentioned variability within DUTs from the same device. Same conclusions were presented in [Oldham, 2008], showing that depending on the manufacturer, but also the DUT itself, the DUT could survive higher dose levels (for example, in [Oldham, 2008], a Micron 4 Gb was tested, one DUT failed between 75 and 100 krad($Si0_2$), two others failed, on the other hand, between 100 and 150 krad($Si0_2$)). Rapid annealing at room temperature of devices may be due to the very thin tunnel oxide (< 10 nm) by tunnelling process as mentioned in [Oldam, 2006].

Effects of dose rate studies in [Oldham, 2008], did not show a clear trend over all manufacturers, some behaved the same way at under higher dose rates, some showed a slightly higher or even double (at least) TID robustness.

Regarding the peripheral circuitry, in [Nguyen, 1998] as well as in [Nugyen, 1999], the authors show that, when tested with 60Co, the charge pump is the main failure location in Flash memories, the charge pump starting to malfunction at dose levels between 8 to 14 krad(Si). Failure of the charge pump occurs before the FG TID failures. The conclusion was the same when testing MLC NAND Flash memories [Nguyen, 2003]. On the other hand, later, test results from [Irom, 2009] showed improvement in the charge pump robustness to TID, able to withstand up to 600 krad(Si02) or even higher, up to at least 700 krad(Si) [Oldham, 2008]. On a side note, the same authors in [Irom, 2009] showed that dose enhancement phenomena occurred also in Flash memories when irradiated with X-ray with respect to 60Co [Cellere, 2005]. The reason why the charge pump is rather sensitive to TID is that due to the high voltage required, thick oxides are used in the charge pump circuitry. Besides, the output voltage should be rather accurate to correctly perform the required operation: in [Bagatin, 2009], it was shown that the output voltage first reduces with initial dose levels, then fluctuates with increasing dose.

In [Oldham, 2008], a new failure type was reported for a Samsung NAND Flash: write operations after 50 krad($Si0_2$) performed during irradiation increased even more the apparent number of errors located in the same column of some blocks. The authors mentioned that the write operation programmed cells in expected locations; more than 50% of these cells were corrected during the irradiation. In [Oldham, 2006], a bitmap of errors occurring on a Micron Flash memory is presented after static biased irradiation at 75 krad(Si) and is showed in Figure 78 for convenience. Error concentration in line suggests errors in the periphery. Error in a specific column, around the column1000, seems to appear, but no further investigation on this aspect was done by the author.

More recently in 2009, Bagatin et al. showed in [Bagatin, 2009] the sequence of failure in a given ST-Microelectronics NAND Flash memory thanks to separate irradiation of each blocks constituting the memory: charge loss in FG first appears (if no scrubbing is performed meanwhile), followed by charge pump issues (output voltage reduction) then complete row decoder failure. TID worsens with the use of thick gate oxides that are usually present in the end product, which allows reducing cost. Output voltage reduction in the read charge pump due to TID may result in the apparent recovery of detected programmed cells such as in [Irom, 2012].

Regarding the memory of concern in this study, TID testing was performed in [Irom, 2012] showing that erase failure may start occurring (in refresh mode, erasing and reprogramming the cells in between each measurements) above 35 krad(Si) or higher. In no refresh mode (simply reading the memory), errors in the FG cells started occurring earlier (< 5 krad(Si)) with a rapid accumulation of errors up to 50-65 krad(Si), with a failed erase function occurring at the lowest level at 55 krad(Si).

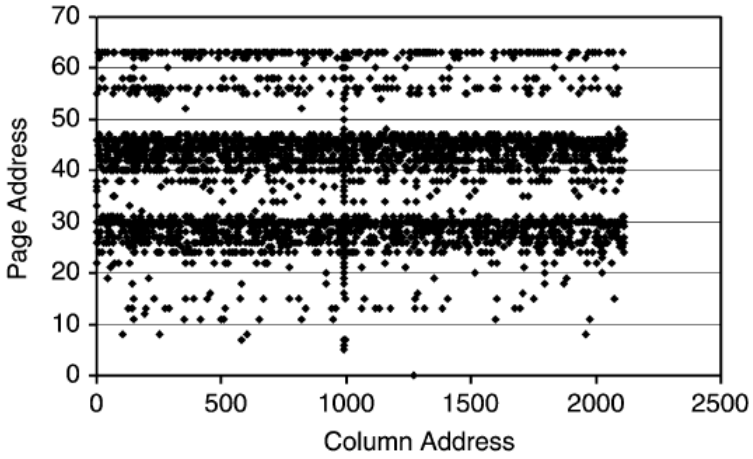


Figure 78: Show the bitmap of a Micron Flash exposed to TID @ 75 krad(Si$\mathbf{0_2}$) in static biased mode from [Oldham, 2006].

With respect to the MTCube mission, assuming a LEO circular polar orbit below 650 km, the memory will experience TID levels below 2-3 krad(Si): at those levels, the FG errors percentage is expected to be very low (< 10^{-7}% of programmed cells in error [Irom, 2012]), the standby current remains almost unaffected by TID up to about 25 krad(Si). This corresponds to one bit in error due to TID at the end of the mission, considering 1 Gb of cells. Hence TID issues are considered not to be of concern for the SEE experiment on Flash memories during the two-year mission lifetime.

5.3.2 Single Event Effects

5.3.2.1 Heavy-ions

Similarly to dose effects, regarding FG cells, errors occur only when a bit '0' is stored i.e. when the FG is programmed [Irom, 2012][Oldham, 2008]. The mechanism responsible for SEE induced deprogramming of a FG cannot be considered similar to that due to TID as explained in 5.3.1. There are two main mechanisms that may explain the erasure of a cell content due to ionizing single particles: as mentioned in [Oldham, 2008], the dense charge column created by a impinging ion creates a conducting transient path between the very thin channel oxide and the substrate allowing the charges stored in the FG to leak away resulting only in SBUs; another explanation is the imbalance between the transient carrier flux – generated by the high energy tail of the impinging particle – coming into the FG, and the flux of transient carriers leaving the FG, which results in a clear discharge of electrons from the FG due to the electric field generated across the oxides by the electrons stored in the FG [Butt, 2008].

The overall result of heavy-ion irradiation on the voltage threshold distribution of the FG cells is the appearance of a secondary peak: this shows an overall drift similar to TID effects but only on a smaller number of FG cells [Gerardin, 2013]. Gerardin et al., in [Gerardin, 2012], showed consistently with a previous studies, that at higher LETs, the larger the electric field in the tunnel oxide, the higher the voltage threshold reduction (in average on a large amount of cells). Same remark occurs for the relation with the LET and voltage threshold drift. Furthermore, in [Gerardin, 2010], by studying the voltage threshold distribution drift, the authors show that the appearance of the intermediate region – especially in integrated technologies –is due to secondary electrons (delta radiation) due to heavy-ions passing nearby a FG cell that could lead to errors in nearby FG cells although the energy deposited by those delta electrons may be much smaller that the energy deposited by a heavy-ion directly impacting a FG.

According to a study from Cellere et al. in [Cellere, 2008], the energy of an ion also impacts the number of FG errors (and voltage threshold shift). The authors showed that, at high LET, the higher

the energy of the ion at a given LET, the lower the cross-section, an observation possibly linked to the size of the ion track.

Angular dependence has been studied in [Grürmann, 2011], but also in [Gerardin, 2011] and [Cellere, 2007]. In [Gümann, 2011], results on Micron and Samsung devices showed that SEU sensitivity is angular dependent (and depends also on the manufacturer) above an elevation of 60°. Tilting along bit lines is one of the worse conditions although worse cross-sections may occur elsewhere especially for high angular sensitivity devices and depending on the ion cocktail used. The MBUs occur in addresses having a distance of one up to four cells. [Gerardin, 2011] showed that at very high grazing angles, up to 30 FG cells may be impacted by high-energy heavy-ions for a highly integrated device.

Regarding the SEE characterisation, effects on the control logic of NAND Flash memories is difficult due to the inner complexity and the number of elements present in a NAND Flash memory (charge pump, buffer(s), decoders, internal microcontroller and so on). Most SEFIs may be cured by a power cycle in the worse case, the advantage being that the data stored in the FG cells will not be lost in contrary to SEFIs occurring in volatile memories. For the definition of a SEFI concerning Flash memories the one proposed in [Oldham, 2008] is used: "In general, a SEFI is any event where the entire DUT, or a large part of it, stops working, presumably from an interaction with a single ion". Dynamic tests involving erase and write operations induced large numbers of SEFIs.

The page buffer (which has a size of approximately a few kbits, similar to the size of a page) is sensitive to ionizing radiation. Characterisation of the sensitivity of the page buffer has been made for example in [Bagatin, 2008], [Oldham, 2006] or [Nugyen, 1999] and seems to perfectly fit Weibull fitted cross-sections. These buffers are used during a read or program operation. Bit flips occurring during such an operation may add temporarily to the number of bit flips occurring in the FG cells.

In [Irom, 2010], the authors noticed SEFIs in a MLC Samsung 8 Gb MLC NAND memory having a LET threshold below 12 MeV.cm²/mg, which was able to self recover when a read operation was performed again, but other types of SEFIs required a power cycle and the device had to be re-initialized to return to normal operations.

In [Oldham, 2008], SEFIs were recorded, even in static biased mode, on pages or blocks or even spreading on several pages/blocs. But not much characterisation was made of those SEFIs regarding the topology and reason providing an insight into the triggering cause. Nevertheless a cross-section was provided. In some cases, it was also noted that the DUT stopped responding in static biased mode, which was considered, by the authors, to be "watchdog errors", probably due to malfunction of the in-built microcontroller. Transient read errors were also noticed in "read only dynamic mode" attributed to noise in the read circuit [Oldham, 2008].

Functional failures also occurred during heavy-ion testing such as in [Oldham, 2006] which were very likely attributed to SEGR. It is a complex task to exactly pinpoint the cause(s) of a SEFI, not only due to the complexity of the periphery as already mentioned, but also due to the fact that the occurrences of particles strikes at different locations at the same time may induce several SEFIs at the same time. Failures due to the embedded microcontroller are also difficult to characterise: an entire block failing may be due to a temporary failure [Gerardin, 2013]; temporary high current states that do not necessitate a power cycle to stop; memory temporary not responding and so on.

No SEL have been reported in NAND Flash memories even at increase temperature and supply voltage [Oldham, 2008]. But this doesn't mean that destructive events did not occur. In some cases, high current spikes (as high as 280 mA with a duration of < 400 ms) at high LET were noticed that sometimes resulted in a functional failure (loss of erase/write operation functionality) not related to TID [Irom, 2010]. Similar findings were presented in [Oldham, 2011]. This behaviour seemed to be device dependant. In fact, the high current spikes occurred also in static biased mode though never leading, in that case, to any damage. The authors were able to show that the charge pump was one of the causes for these high transient current levels and that it was liked to doping level concentration in

the NMOS of the charge pump. In [Bagatin, 2010], the authors concluded that those reversible currents spikes may be due to logic conflicts in the charge pump circuitry while the irreversible high-LET spikes may be the consequence of a SEGR in the thick gate oxide of the charge pump and capacitors. Three years earlier, Irom et al., in [Irom, 2007], postulated that those current spikes might be linked to micro-dose effects in the charge pump region, but this reason did not seem to be favoured later and doping level was found to be the reason. The mechanisms linking the current spikes directly to destructive events are still under debate [Gerardin, 2013].

Stuck bits were noted in [Oldham, 2006] and possibly attributed to micro-dose effects: one single ion strike is able to deposit a high dose (high density of charge) in a very small volume causing a voltage threshold shift leading to a leakage current that can be large enough to prevent the programming of a cell able to anneal quickly due to the very thin tunnel oxide [Dufour, 1992][Oldham, 1993][Poivey, 1994]. They essentially occur at high LETs.

Overall, as there is much more design margin integrated within the design of SLCs, they are more robust to their MLC counterparts [Irom, 2012][Irom, 2009]: MLC have a more complex design and lower read margins [Gerardin, 2013].

5.3.2.2 Protons

Regarding proton testing, tests were conducted in [Oldham, 2006] at 100 and 200 MeV resulting in no static errors though in dynamic mode, transient currents induced misreading of bits without the cell itself being impacted by protons. Once, the chip did not respond to a command for some time. The number of errors drastically increased when the TID reached the memory's limit, which proved that those latter errors are more likely TID related and than SEE related. In [Wester, 2004], irradiation at 200 MeV up to 83 krad(Si) showed very low rate of SBUs randomly distributed that in fact occurred in the buffer and not in the FG cells themselves. The authors also highlighted lot-to-lot variations.

More recently, in [Gerardin, 2012], a 41 nm feature size SLC NAND was tested in unbiased mode (the manufacturer remained unknown) showing indirect ionization occurrences along with unavoidable dose-liked degradation. Findings showed that proton induced upsets are enhanced by total dose effects and occurred on the memory mainly in programmed cells (although a few erased cells were affected), with an increase of SEU induced errors following the increase in impinging proton energy as results shown in [Gerardin, 2012] for energies between 34.5 MeV and 498 MeV for a given ionizing dose received by the component. This may be due to higher average energy of secondary ions, which increases their range and hence increase the probability of reaching the sensitive volume of a memory cell.

Indeed, synergetic issues were studies in [Bagatin2, 2010] showing that even at dose levels lower than 50 krad(Si), exposing the device to heavy-ions increases the MLC NOR memory cross-section especially at low LETs (if no program or erase operation is performed) and can reduce the LET threshold of the FG cell. Scrubbing greatly reduces these combined effects.

5.4 Flash test results based on heavy-ion testing

The device has been irradiated with heavy-ion beams in static mode, after having been written with different test patterns. Several large-scale events have been observed in the test results, along with other functional malfunctions. This section represents a step forward towards an improved characterisation of Flash technology, and the understanding of the physical and electrical origins of such large events, which can be disastrous in space applications. The test results were analyzed with the help of an in-house software tool based on Scilab to process the data and plot logical bitmaps, since the possible scrambling and interleaving schemes of the memory are unknown. First, the results obtained in retention mode will be presented: the retention mode is here defined as the mode when the

data is stored in the memory unbiased. Then, the results in static mode (the memory being biased during irradiation) will be shown. As the memory also embeds a large buffer, tests were conducted in static mode to characterize this part of the memory as well. Finally, a word will be given regarding latch-ups and erase and write status errors. The latter being messages triggered by the operation check parts of the memory in order to ensure that a given erase/write operation has been successfully carried or not.

5.4.1 Retention mode test (non biased)

The memory was tested in retention mode in order to study the SEE sensitivity of the FG cells alone: a data pattern is initially stored, then the memory is unbiased and irradiated. At the end of the irradiation run, the data stored in the memory is compared with the initial pattern. Fluence ranged between 1.0 $\times 10^4$ and 1.0 $\times 10^5$ cm^{-2}, the flux remained between 1.0 $\times 10^2$ and 1.0 $\times 10^3$ cm^{-2}/s and was adapted in order to collect enough events. Unbiased runs were performed with LET ranging between 3.6 and 60 MeV.cm²/mg.

The runs with a solid '1' pattern resulted in no errors for all LET values and fluence. This results is perfectly consistent with bibliography, where it was noticed that erased FG cells are resilient to heavy-ion irradiation: it is not possible for a single particle to be able to reprogram a FG cell, and the read voltage of the read charge pump does not shift to lower values when irradiated with heavy-ions. On the other hand, write and erase status errors occurred at higher LETs (from an LET of 10.1 MeV.cm²/mg, no errors below 4.2 MeV.cm²/mg) even on new DUTs. This part will be discussed in section 5.4.5 and results are similar regardless of the data pattern.

On the other side, as expected, the solid '0' pattern resulted in numerous read errors, at every LET at which the device was tested starting at a LET of 1.8 MeV.cm²/mg. The word cross-section is plotted in Figure 79. Besides, Figure 80 depicts a part of the bitmap showing the read word errors (one word read error represented by a black pixel – one word is in error if at least one of its bits is in error). The errors are randomly distributed across the tested section of the die, and small clusters of a few words can be seen vertically oriented (along the bit line). They are similar to the small clusters occurring in static biased mode testing and will be discussed in the following sub-section.

Finally, no vertical lines were spotted during unbiased mode testing, which significantly differs from the static biased results discussed in 5.4.2.

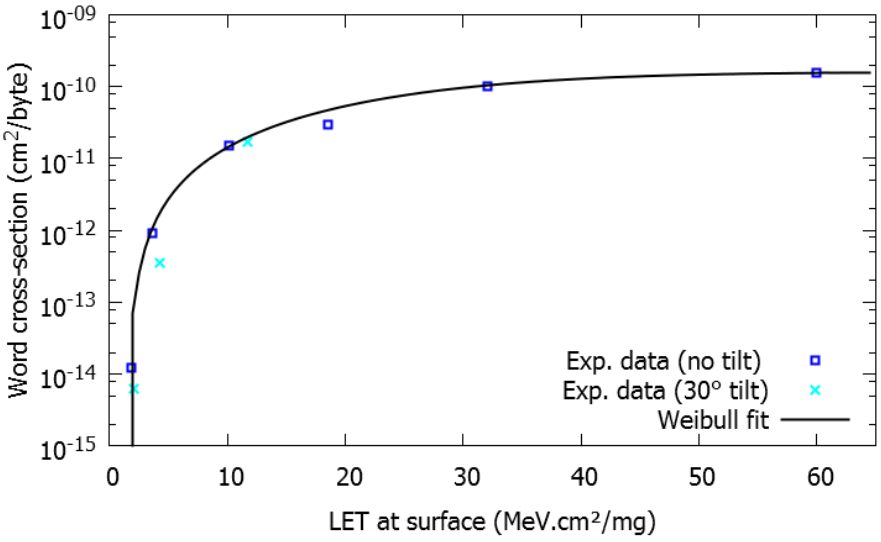


Figure 79: Word cross-section in unbiased mode.

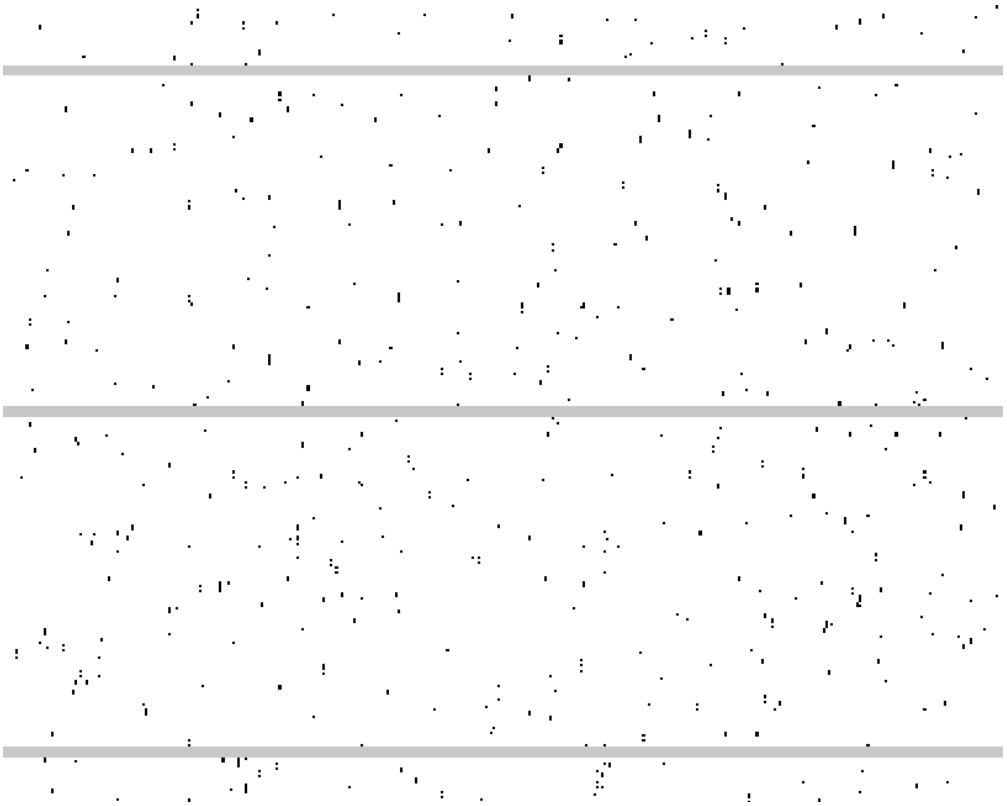


Figure 80: Close-up on a bitmap generated after unbiased mode testing irradiation with xenon (LET of 60 MeV.cm²/mg).

5.4.2 Static mode test (under bias)

Static tests performed with nitrogen (LET of 1.8 MeV.cm²/mg) resulted in respectively one and two SBUs (Single-Bit Upset within a word), when using the solid '0' pattern at a respective fluence of 3.0 $\times 10^4$ and 1.5 $\times 10^5$ part.cm^{-2}. At those levels of fluence, no errors were recorded when using the solid '1' pattern. An erase operation was sufficient to correct the SBUs without the need of a PC (Power Cycle).

Irradiation results with the other heavy-ion particles resulted in widely varying numbers of erroneous words per test, requiring a deeper analysis. Hence, besides counting the number of erroneous words, the number of upset bits was evaluated for each word presenting error(s). Moreover, a bitmap representation of each run was generated along with analytical histogram plots (Figure 81). The bitmap of the Flash memory (Figure 82)was plotted as follows: the left half of the bitmap contains the even blocks, while the right half contains the odd blocks (accordingly with the manufacturer datasheet). Each block is made of 128 horizontal lines, which each corresponds to a page. Each line is made of 8192 pixels, one per column – that is, one per memory word. The individual bits of each word are not represented. The structure is divided in two halves, and each seems to have its own data register. Due to the very large size of the generated bitmaps (over 64 million pixels each), it is not possible to clearly display them entirely, hence only their most relevant sections will be exhibited to support the test results analysis. Regular patterns of errors were observed such as Vertical Lines (VLs) of errors, as well as small clusters of words or isolated words with errors.

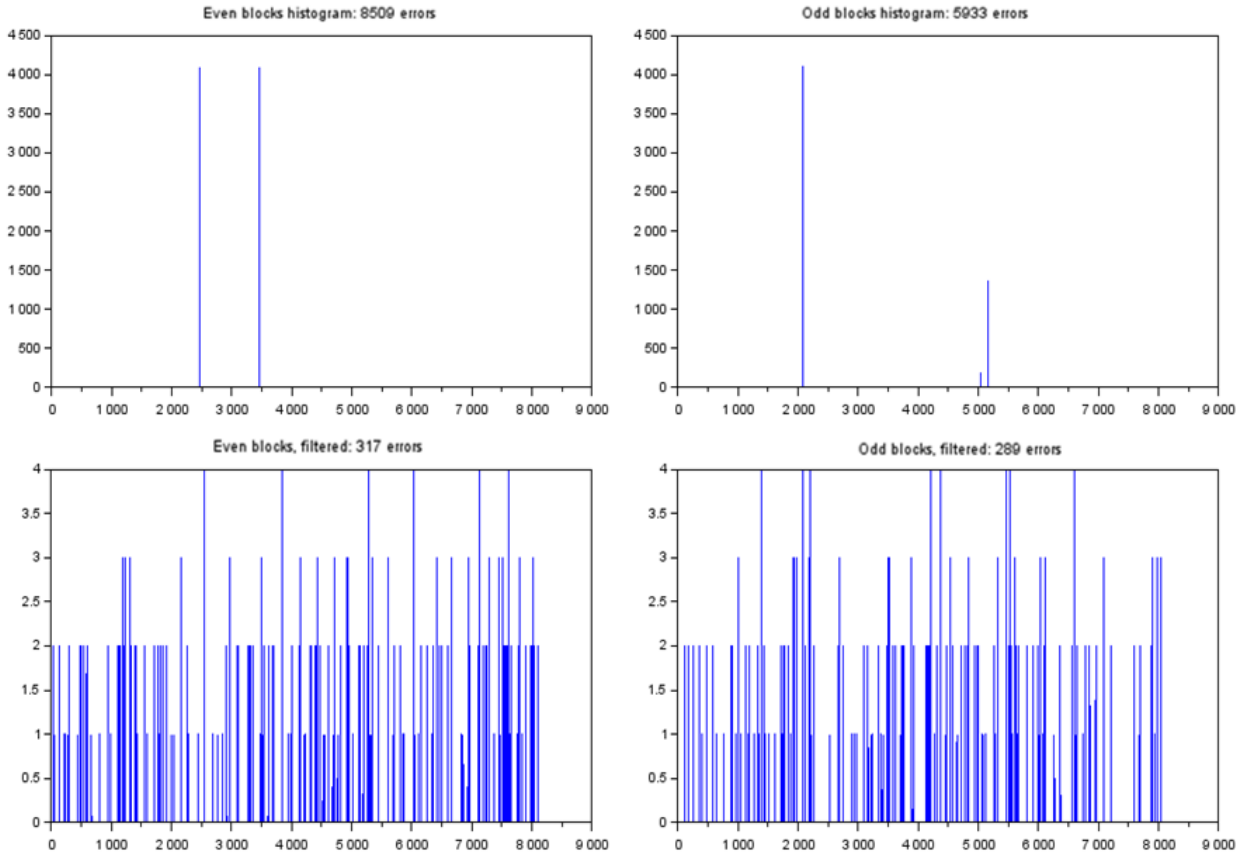


Figure 81: Histogram of a memory bitmap, where the number of word errors is plotted w.r.t each column. The two leftmost (resp. rightmost) plots represent the plane with the even (resp. odd) blocks. The bottom histograms are similar to the top ones after removing the VLs.

Finally, in order to further analyze the test log files, for each run, histograms were plotted where the total count of word errors is calculated for each column on the 512 Mb, corresponding to the section of the memory considered in the tests. An example of a histogram is shown in Figure 81. The leftmost plots represent one plane (odd blocks), the rightmost plots represent the second plane (even blocks). The top plots represent the total number of word errors per column while the bottom plots are similar the previous ones, but they do not display the columns which suffered too many word errors (the threshold was arbitrarily set to 64), allowing filtering the vertical lines of errors from smaller clusters. Thanks to this filtering, it was possible to plot the memory cross-section while only considering the small clusters of errors.

The different types of occurring errors will now be discussed.

Vertical Lines (VL) - For a large majority of plotted bitmaps, the most significant error types that appeared were VL of errors, running from the top to the bottom of the bitmap and crossing all blocks either in the left plane (even blocks) and/or in the right plane (odd blocks) (Figure 82).

Several VLs may occur on one plane and/or the other one. Those VLs did not occur at a LET of 1.8 MeV.cm²/mg but occurred at 18.5 MeV.cm²/mg. Hence, the LET threshold for the appearance of those VLs is likely to be between these two LET values although tests were not carried, due to lack of time, to LET values in between to define more precisely the LET threshold value for the appearance of those VLs. These vertical lines are sometimes continuous, with all words of the column exhibiting bit errors, and sometimes discontinuous, with sparse word errors along the column, as shown in Figure 82. The VL occurred in every run in static mode (solid ‘1’, solid ‘0’, checkerboard and anti-checkerboard data background patterns), on three specimens tested in two different test facilities (except when tested with nitrogen at 1.8 MeV.cm²/mg). An attempt was made to plot a VL cross-section and a Weibull fit was fitted to the results as shown in Figure 83.

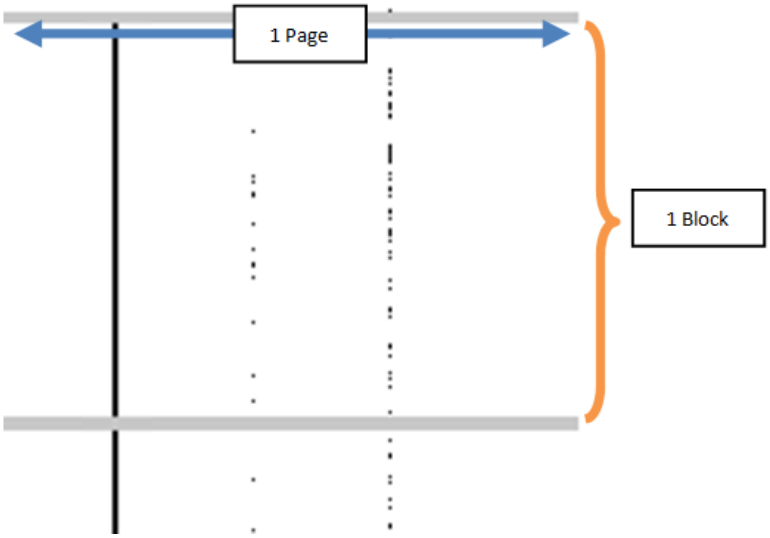


Figure 82: Close-up on a small region of a bitmap generated after static mode tests, where two types of VLs are visible (continuous and intermittent). Words are shown as black pixels if they exhibit bit errors, and as white pixels otherwise. The grey horizontal lines are used to highlight the boundaries between blocks and do not represent any errors.

It was noticed that, to suppress those VLs, neither an erase operation was sufficient, nor a power cycle (PC). In fact, only the combination of a PC followed by an erase operation stopped the persistence of VLs. To the best of our knowledge, this is the first time that such a characterisation of those VLs has been performed. Furthermore, after a static run, the VLs appeared to be "dependent" on the data background pattern: for example after beam exposition with a solid '0' the same VLs reappeared when writing then reading '0' whereas in between a write '1' and a read '1' other VLs appear, while the former ones "disappeared".

We propose two basic failing mechanisms that can explain the occurrence of VLs of errors. The first one consists of a malfunction in the read data buffer, the second one implies the malfunction of an electrical element of the failing column:

- A stuck bit in the data buffer. During a block read operation, one page at a time is loaded in the data buffer, which is then serially sent out of the memory. If one bit of the data buffer is stuck to a value, which is the opposite of the value stored in the memory (e.g. stuck to '1' when '0' are stored in the memory), at each page read the very same error will appear at the same location. Since the pages are represented by horizontal lines of pixels, the errors appear at the same position on each horizontal line of the bitmap, creating a VL of errors. This failure mechanism can explain the shape and extent of the VLs, but it cannot explain the fact that in order to stop this behaviour, an erase cycle is necessary, as the erase action does not affect the data buffer.

- The control electronics of the failing bit line. If the faulty behaviour is not due to the data buffer, it must depend on malfunctions at the bit line level and, in particular, its control logic, since it is very unlikely that a single particle or multiple particles would upset hundreds of cells at once and in that specific arrangement. For this reason, the failure must concern one of the elements in the column that are involved in the sensing action of the read operation. For example, in the event of a particle hit which would generate a large amount of charge, the concurrent effects of a triggered µ-latchup and charges trapped in the bit line access transistor [Bagatin, 2008] result in partial or total inhibition of the access to the bit line. All accesses to the column will be affected and generating errors with the shape of a VL. In order to stop the failing process, it is necessary to carry out both a PC, removing the µ-latchup, and the erase operation that restores the access transistor.

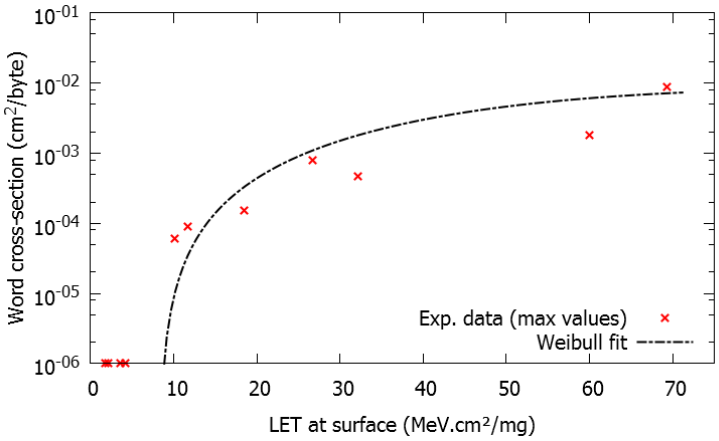


Figure 83: VL cross-section in biased static mode testing fitted with a Weibull curve. Cross-section values at $10^{-6} cm^2/byte$ actually represent runs with no upsets.

Isolated MBUs and clusters of MBUs - Besides those VL, isolated MBUs (Multiple Bit Upsets within the same word) were also observed along with small clusters of MBUs (two to five) lined up vertically (i.e. along the same bit lines), at contiguous line addresses. Neither diagonal nor horizontal clusters of errors were detected. These errors occur randomly across the entire bitmap. Examples of such error types are depicted in Figure 84. An interesting characteristic of those small clusters of MBUs is that the failing bits within the words are generally the same. It was nevertheless noticed that after a PC, the number of erroneous bits in each word was reduced to one (SBU). This is an important key point for applications, since it reveals the need to make a PC before reading sensitive data from the memory. These PCs do not accelerate the aging of the cell like erase actions do, and reducing to one the number of faulty bits allows the efficient use of error detection and correction techniques. Isolated and clusters of MBUs occurred only for solid '0' data background tests and never for solid '1' tests. This is in line with previous results, such as those reported in [Oldham, 2006], stating that during beam irradiation, FG cells are more resilient to bit flips when storing a '1' (floating gate with no charge) than when storing a '0' (charged floating gate). These errors can all be removed by an erase operation, which discharges the floating gate (whereas a PC does not). In fact, a read cycle made after a PC reveals about the same number of word errors with a small fluctuation in the number of errors. These fluctuations are likely due to borderline cells, i.e. cells that have their floating gates at an intermediated value of charge after irradiation, which makes the result of a read access uncertain (intermittent errors) [Bagatin, 2008]. These small error clusters occurring along the bit line with almost the same pattern of error can be explained by the action of a single particle hitting the memory plan. Charge sharing can also possibly occur, leading to several bits being upset in a single word. Secondary particles generated at angles may also be the cause of these vertical clusters, considering that spacers separate the columns and prevent/reduce the horizontal shaped clusters.

Figure 84: Close-up on a bitmap generated after static mode tests and showing the shape of single word errors or small cluster of errors.

In order to plot the static word cross-section of the memory core cells, the VL were first filtered. To do so, an arbitrary value of 60 was chosen: above 60 words in errors in the same column, all the errors on this column were removed. Though arbitrary, it appears that after filtering, the maximum number of errors in a column never exceeded six words. This give confidence that the value chosen is suited and conservative and could have been even set to a lower value (to 10 for example).

The resulting word cross-section is plotted in Figure 85, counting each word in error without performing any clustering of the small vertical detected clusters. It can be seen that the trend of this

cross-section appears to be compatible to usual cross-section trends. The cross-section plotted was the one for solid '0' static mode tests. After filtering the VLs, the solid '1' static mode cross-section of the memory was 0. The cross-section of checkerboard and anti-checkerboard patterns is also plotted and was performed only at one LET (26 MeV.cm^2/mg). The value is half the solid '0' cross-section.

The surprising result is at a LET of 60 MeV.cm²/mg. No errors were recorded after filtering the VLs (once an intermittent line occurred after a solid '0' static run at this LET). The reason is very likely due to the fact that the range of xenon ion (89 µm in silicon) is not sufficient to hit the sensitive volume of the memory while krypton ion, having a range of 94 µm at a lower LET, induced errors. The fact that an intermittent VL occurred with Xe allows predicting that the sensitive volume triggering a VL could probably be located less deeper than the sensitive volume of the FG cell.

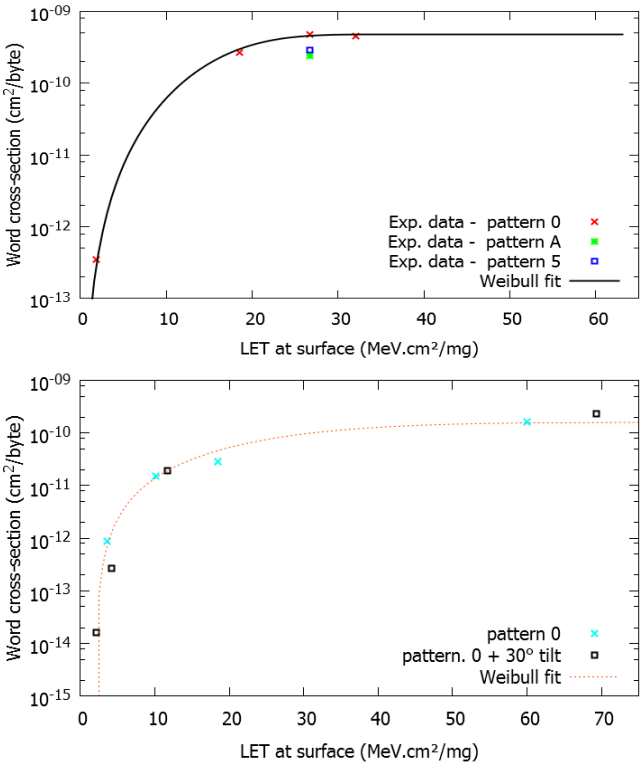


Figure 85: Word cross-section in static mode test after filtering the vertical lines of error.

5.4.3 Static buffer mode test (biased mode)

During static buffer mode tests, a checkerboard pattern was written on one page of the memory. Tests were carried at LETs of 1.8, 18.5, 32.1 and 60 MeV.cm²/mg. In two occasions, a solid '1' pattern was also used (at a LET of 1.8 and 60 MeV.cm²/mg). For these runs, instead of reading the memory, the sequence of commands to implement a reading operation was interrupted in order to keep the data stored in the data buffer (registers) of the memory. The memory was then irradiated and a buffer reading operation was finally performed to check its contents.

Irradiation at a LET of 1.8 MeV.cm²/mg resulted in no errors for both the checkerboard and solid '1' patterns. On the contrary, from a surface LET of 18.5 MeV.cm²/mg upwards, all runs resulted in errors. This allows us to speculate that the LET threshold of the data register is between 1.8 and 18.5 MeV.cm²/mg.

The results from these runs can be classified in two groups. In the first group, few errors were detected (between 12 and 40 failing words), while other runs resulted in the entire data register (i.e. 8192 words) failing. The latter event occurred twice on the three runs at a LET of 18.5 MeV.cm²/mg, and

once out of the three runs at 60 MeV.cm²/mg. A closer look at the number of bit errors per word when the entire data register failed shows that, for each faulty word (8 bits), 4 bits failed most of the time when the checkerboard pattern was used at a LET 18.5 MeV.cm²/mg as depicted in Figure 86. At 60 MeV.cm²/mg, when the solid '1' pattern was used, the data register failed once with every bit of each word failing. When the entire data register was not completely failing, most of the failing words presented only one bit in error with two exceptions:

- at 18.5 MeV.cm²/mg, out of the 29 failing words, 3 words had respectively 2, 2 and 5 bit upsets;
- at 60 MeV.cm²/mg, one word out of the 6 failing words had 3 bit flips.

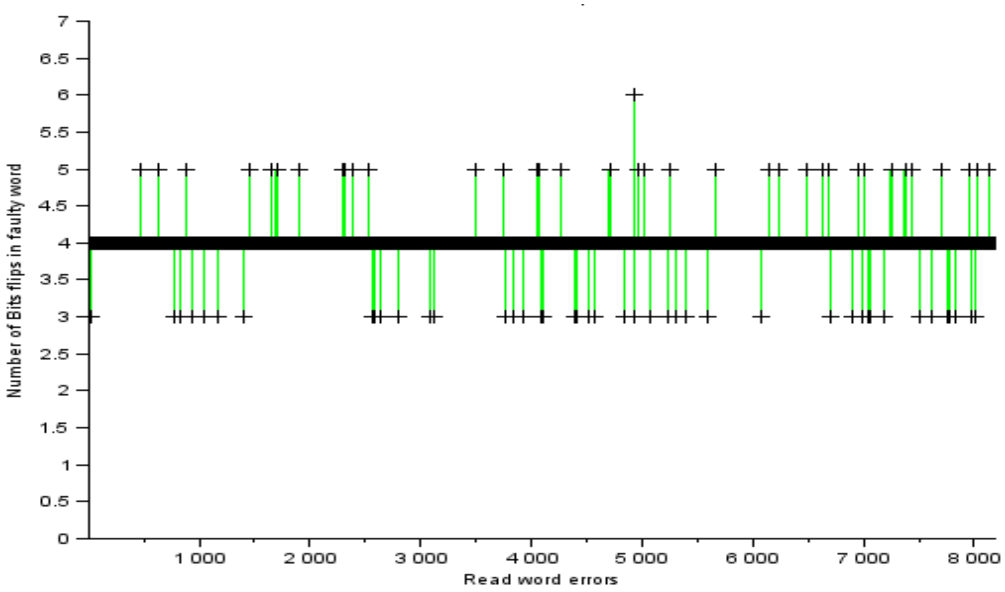


Figure 86: Number of data register bits failing in each failed word, in static mode, using a checkerboard pattern, at a surface LET of 18.5 MeV.cm²/mg.

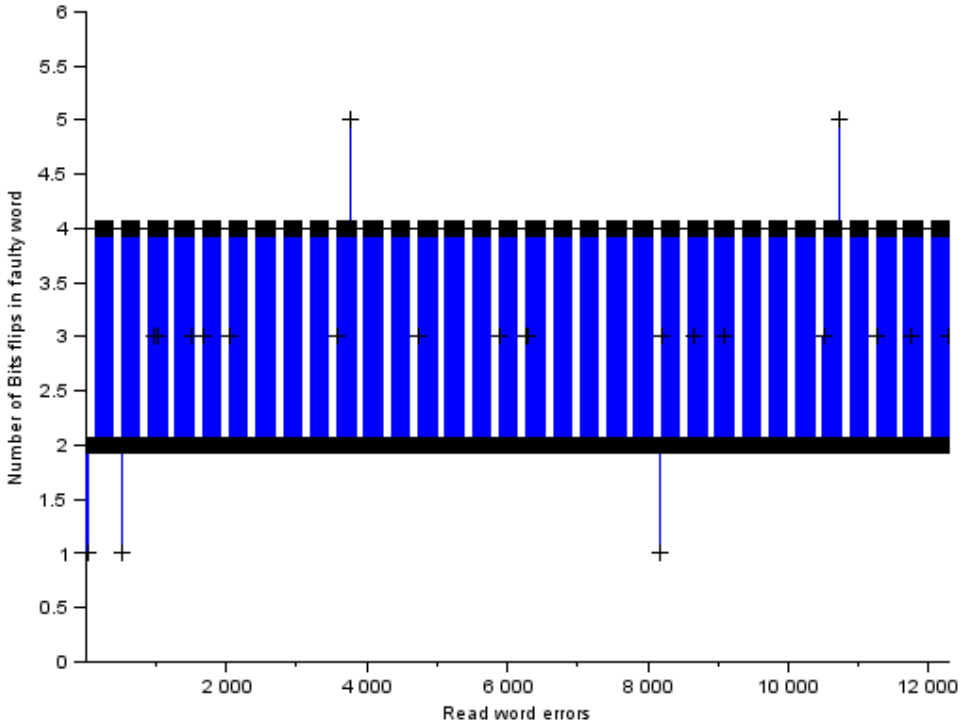


Figure 87: Number of bit flips in each word in errors after a static mode test using a solid '1' pattern using Fe particle (LET of 18.5 MeV.cm²/mg). Except a few words, the number of bits failing in each failed word appears to be following a period pattern.

When considering the tests with the buffer just partially failing, the word cross-section follows a Weibull curve, as depicted in Figure 88, though more data would be valuable, especially at LETs between 1.8 and 18.5 MeV.cm²/mg to improve the Weibull fit quality.

Similar experiments testing the data register were made by Bagatin et al., as mentioned in [Bagatin, 2008], on another NAND Flash component. The authors found a cross-section an order of magnitude lower than evidenced by our tests.

Regarding the runs with a fully faulty buffer, the fact that the checkerboard pattern leads to most or all words having four bits in error while the solid '1' pattern having all bits of all words in error tends to lead to the conclusion that during the irradiation, the control logic ruling the reset function of the data register produced unwanted asynchronous resets and all bits were set to '0'. As mentioned in the datasheet of the memory, a reset command to clear the data register content exists, supporting the above assumption. Concerning the errors with 3, 5 and 6 bit flips in some words within the full faulty buffer, this can be explained with the time occurrence of the faulty buffer reset. When the reset occurs closer to the beginning of the irradiation, all buffer cells are set to '0', and further irradiation generates other bit flips that modify the error pattern within the words. Conversely, the closer the faulty reset is to the end of the irradiation, the more regular the error pattern is, with 8 bit flips for solid '1' data background and 4 bit flips for checkerboard background.

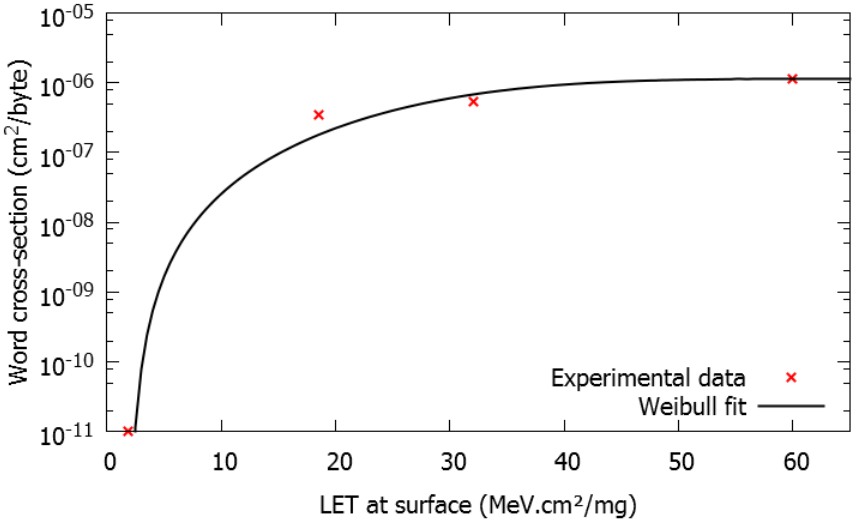


Figure 88: Word cross-section of the data register calculated by dividing the number of failing words by the fluence and the buffer word size (i.e. 8192 words). The LET threshold was guessed at 2 MeV.cm²/mg in order to fit the data with a Weibull curve. Weibull parameters used are: W=31.10, S=2.78, $\sigma_{sat} = 1.14 \times 10^{-6}$ $cm^2/byte$, $LET_{th} = 2.00$ $MeV.cm^2/mg$. Cross-section value at $10^{-11} cm^2/byte$ actually represents a run with no upsets.

5.4.4 Latch-up testing

No latch-up events were spotted up to an effective LET of 69.3 MeV.cm²/mg (using Xe with a 30° inclination).

5.4.5 Erase and Write status errors

The tested device provides the functionality of monitoring the status of each operation. During the runs, the status registers were read back, often showing failure of the operation. The number of failures had the tendency to increase from one run to the other. An interesting observation was that although the status showed failure of the operation, the operation was successfully executed. These

status errors could be attributed to SEUs occurring either to the status registers themselves, or SETs in the control circuitry. However, these status errors appeared also when the device was not irradiated. Taking the example of one of the Flash memory tested during TC10, at the end of the campaign, a functional check was performed on the memory and it resulted in 216 then 141 write status errors. Five days later, the memory was power cycled, and successive write and read operations were performed. During the successive read operations the number of write status errors was logged and showed a steady reduction in the number of status errors, from 129 to 14, as depicted in Figure 89. Similarly, the other Flash memory resulted in the same behaviour, with, however, less write status errors. This behaviour may be explained by a slight shift of the V_{th} distribution below the program voltage verification, but still above the read voltage, leading to apparent write status errors, which are however properly read. This shift is schematically presented in Figure 90. Successive write and erase operations may induce a shift in the opposite side of those cells.

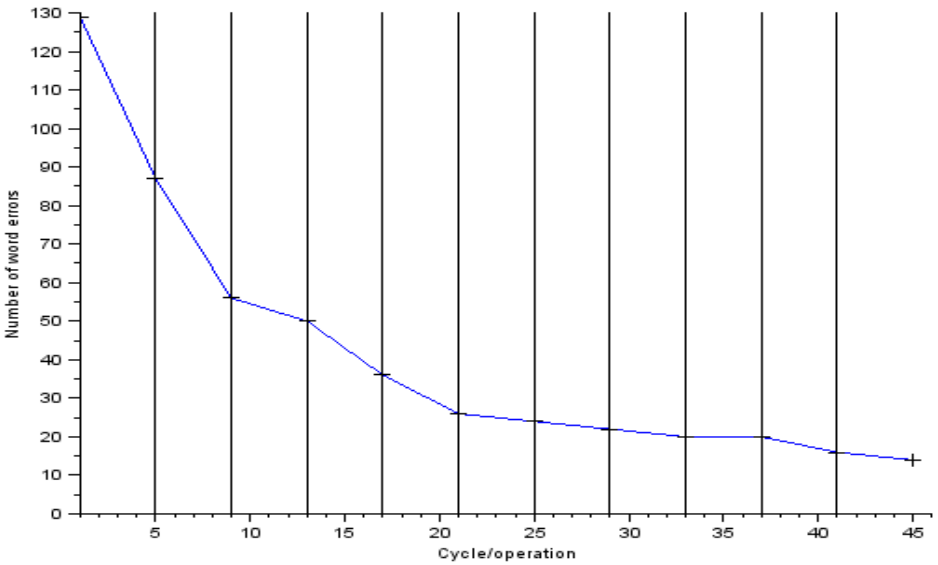


Figure 89: Reduction in the number of status errors five days after the irradiation campaign.

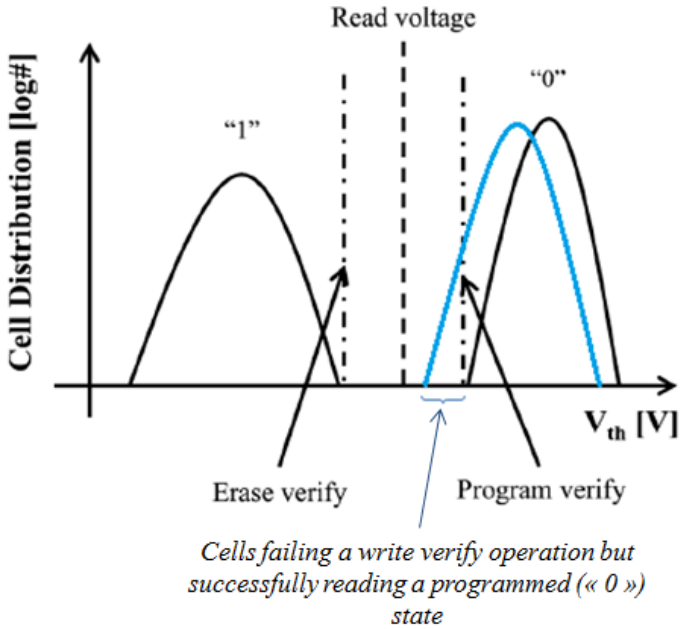


Figure 90: Illustration of the V_{th} distribution of FG cells when programmed or erased, slightly modified from [Gerardin, 2013]. The blue curve of V_{th} distribution of irradiated cells shows the shift induced by heavy-ion irradiation.

5.5 Flash test results based on proton test results

Due to technical issues with the main beam, only a few runs were possible using a single DUT of Flash to investigate the effects of mono-energetic protons at 200 MeV, 101 MeV and 51 MeV. During this test campaign static, buffer and dynamic tests were performed. Unfortunately, unbiased tests were not carried for the above-mentioned reason. The fluence ranged between 2×10^{9} and 2×10^{10} protons/cm².

Static biased testing are presented in Figure 91 (after filtering of any VL), which represents the word cross-section of the memory plan tested (512 Mb) using the solid '0' pattern. Similarly to what is mentioned for heavy-ion irradiation, solid '1' pattern, tested at 200 MeV only (fluence of 2×10^{9} protons/cm²) did not result in any bit flips. Two runs were made at 200 MeV at the beginning and the end of the irradiation time dedicated to the Flash memory in order to see if there was an impact due to dose deposited during each run. The memory was exposed to about 9 krad(Si) and the resulting word cross-section appears to be similar to the one obtained with the memory in a "pristine" state. However, more statistical data would be needed to confirm if, when irradiated, the cross-section is consistently lower when dose has been accumulated in the device.

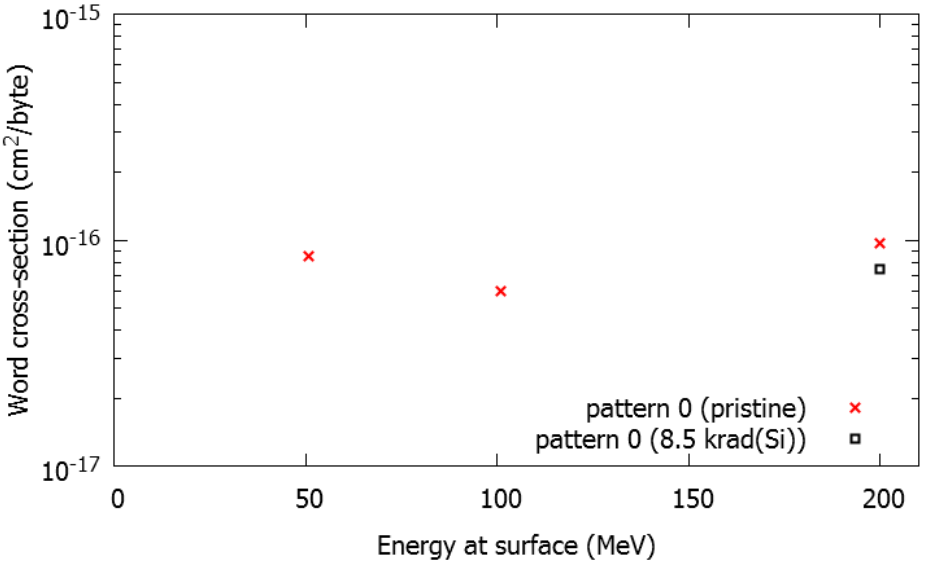


Figure 91: Proton word cross-section in static mode test after filtering the vertical lines of error.

Similarly to heavy-ion testing, the buffer register was also tested using a checkerboard pattern; the results are presented in Figure 92. Measurements could not be done with long exposures and hence the 1 σ standard deviation uncertainty is rather large. The second measurement done at 200 MeV at the end of the Flash campaign resulted in a word cross-section value four times lower: this difference does not seem to be due to TID effects but, as previously mentioned, very likely are due to the limited number of observed bit flips. Nevertheless, it can be seen that the buffer register appears to be more sensitive (more than 3 times higher word cross-section) than the FG cells itself.

Throughout the irradiation campaign no write error status occurred. On the other hand, although no erase status occurred for the first few runs at 200 MeV (cumulative fluence of 4.8×10^{10} protons/cm², estimated TID of up to 2.8 krad(Si)), when changing energies to 101 MeV, erase status errors started appearing in the next runs.

At 101 MeV, after a fluence of 6.8×10^{10} protons/cm² (estimated TID of 4.7 krad(Si)), the first VL appeared with exactly the same characteristics as those resulting from heavy-ion testing. VL appeared at 50.8 MeV, and also during the last run at 200 MeV contrary to the first few runs. It appears, although difficult to ensure with confidence that there might be a correlation between dose and the

appearance of VL or at least a weakening due to dose at least. Further tests need to be carried with other DUT to reproduce and better explore this behaviour, as well as possible TID testing that might provide interesting insight in the mechanisms triggering VLs.

Low energy proton testing has not been performed in this study due to the lack of opportunity and time.

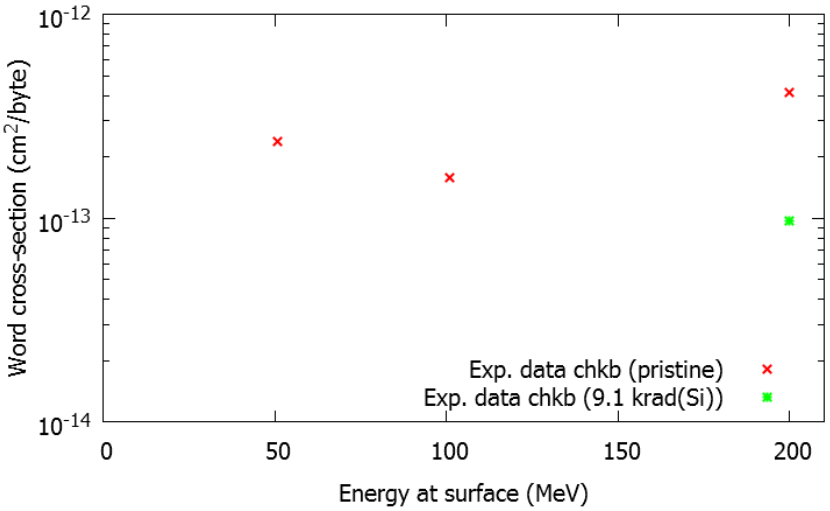


Figure 92: Word cross-section of the data register calculated by dividing the number of failing words by the fluence and the buffer word size (i.e. 8192 words).

5.6 Conclusion on NAND Flash testing

Similarly to what was noted in [Oldham, 2008], the cross-section of FG errors is very small especially when ECC is added. On the other side, SEFI events may be of concern. The current study focused mainly on the different topology of errors, most of them occurring in the peripheral circuitry. By combining power cycles, erase operations and other conditions, a better understanding was gained into the generation of Vertical Lines (VLs) which occurred during heavy-ion and proton testing. They have not been thoroughly studied in the literature so far. As the internal structure of the memory is unknown, similarly to the analysis performed on the FRAM tested memory, possible explanations have been given based on the various runs and test conditions implemented to characterise those VLs. The data register (buffer) was also characterised and a better insight was provided into possible reset occurrences of the buffer during irradiation, which would translate, depending on the stored data into a possible failure of an entire page.

The appearance of VLs is not limited to heavy-ion testing, but they also appeared during proton irradiation. Hence the appearance of VLs during the MTCube mission is not to be excluded, and due to the very large amount of corrupted words in the occurrence of VLs, special care will be take to manage them in order to have enough information recorded without saturating the experiment data buffer of the payload as well as being able to properly remove them afterwards. In order to minimize the occurence of errors, and thus the impact due to VLs, our studies show that the best solution would be a sequence of an erase operation and a power cycle.

In flight, it is expected to encounter some isolated MBUs and small MBU clusters and possibly the occurrence of VLs.

The obtained cross-section under heavy-ion and proton irradiation will be used to estimate the error rate of the two Flash memories that will fly on-board MTCube. This topic will be studied in the next chapter (chapter 6).

5.7 Bibliography

[Bagatin, 2008] M. Bagatin, S. Gerardin, G. Cellere, A. Paccagnella, A. Visconti, S. Beltrami, R. Harboe-Sorensen, and A. Virtanen, “Key contributions to the cross section of NAND Flash memories irradiated with heavy-ions,” *IEEE Trans. Nucl. Sci.*, vol. 55, pp. 3302–3308, Dec. 2008.

[Bagatin, 2009] M. Bagatin, G. Cellere, S. Gerardin, A. Paccagnella, A. Visconti and S. Beltrami, "TID Sensitivity of NAND Flash Memory Building Blocks," in *IEEE Transactions on Nuclear Science*, vol. 56, no. 4, pp. 1909-1913, Aug. 2009.

[Bagatin2, 2009] M. Bagatin, S. Gerardin, G. Cellere, A. Paccagnella, A. Visconti, M.Bonanomi, and S. Beltrami, “Error instability in floating gate Flash memories exposed to TID,” *IEEE Trans. Nucl. Sci.*, vol. 56, no. 6, pp. 3267–3273, Dec. 2009.

[Bagatin, 2010] M. Bagatin, S. Gerardin, A. Paccagnella, G. Cellere, F. Irom, D.N. Nguyen, Destructive events in NAND Flash memories irradiated with heavy-ions, Microelectronics Reliability, Volume 50, Issues 9–11, September–November 2010, Pages 1832-1836, ISSN 0026-271.

[Bagatin2, 2010] M. Bagatin, S. Gerardin, A. Paccagnella, G. Cellere, A. Visconti, and M. Bonanomi, “Increase in the heavy-ion upset cross section of floating gate cells previously exposed to TID,” *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3407–3413, Dec. 2010.

[Bagatin3, 2010] M. Bagatin, S. Gerardin, G. Cellere, A. Paccagnella, A. Visconti, S. Beltrami, M. Bonanomi, and R. Harboe-Sørensen, “Annealing of heavy-ion induced floating gate errors: LET and feature size dependence,” *IEEE Trans. Nucl. Sci.*, vol. 57, no. 4, pp. 1835–1841, Aug.2010.

[Butt, 2008] N. Butt and M. Alam, “Modeling single event upsets in floating gate memory cells,” *IRPS*, pp. 547–555, 2008.

[Cellere, 2004] G. Cellere, A. Paccagnella, A. Visconti, M. Bonanomi, Paolo Caprara, and S. Lora,” A model for TID effects on floating gate memory cells,” IEEE Trans. Nucl. Sci., vol. 51, no. 6, pp. 3753–3758, Dec. 2004.

[Cellere, 2005] G. Cellere, A. Paccagnella, A. Visconti, M. Bonanomi, A.Candelori, and S. Lora,” Effect of different total ionizing dose source on charge loss from programmed floating gate cells,” IEEE Trans. Nucl. Sci., vol. 52, no. 6, pp. 2372–2377, Dec. 2005.

[Cellere, 2007] G. Cellere, A. Paccagnella, A. Visconti, M. Bonanomi, R. Harboe-Sorensen, and A. Virtanen, “Angular dependence of heavy-ion effects in floating gate memory arrays,” *IEEE Trans. Nucl. Sci.*, vol. 54, pp.2371–2378, Dec. 2007.

[Cellere, 2008] G. Cellere, A. Paccagnella, A. Visconti, M. Bonanomi, S. Beltrami, R. Harboe-Sorensen, and A. Virtanen, “Effect of ion energy on charge loss from floating gate memories,” IEEE Trans. Nucl. Sci., vol. 55, pp.2042–2047, Aug. 2008.

[Dufour, 1992] C. Dufour, P. Garnier, T. Carriere, J. Beaucour, R. Eccofet, and M. Labrunee, “Heavy-ion induced single hard errors in submicronic memories,” *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 1693–1697, Dec. 1992.

[Gerardin, 2010] S. Gerardin, M. Bagatin, A. Paccagnella, G. Cellere, A. Visconti, M. Bonanomi, A. Hjalmarsson, and A. Prokofiev, “Heavy-ion induced threshold voltage tails in floating gate arrays,” *IEEE Trans. Nucl. Sci.*, vol. 57, no. 6, pp. 3199–3205, Dec. 2010.

[Gerardin, 2012] S. Gerardin, M. Bagatin, A. Paccagnella, J. R. Schwank, M. R. Shaneyfelt and E. W. Blackmore, "Proton-Induced Upsets in 41-nm NAND Floating Gate Cells," in *IEEE Transactions on Nuclear Science*, vol. 59, no. 4, pp. 838-844, Aug. 2012.

[Gerardin, 2013] S. Gerardin *et al.*, "Radiation Effects in Flash Memories," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1953-1969, June 2013.

[Grürmann, 2011] K. Grürmann, D.Walter, M. Herrmann, F. Gliem, H. Kettunen, and V.Ferlet-Cavrois, "SEU and MBU angular dependence of samsung andmicron 8-Gbit SLC NAND-Flash memories under heavy-ion irradiation," in *Proc. IEEE Radiation Effects Data Workshop*, 2011, pp. 1–5.

[Grürmann, 2012] K. Grürmann, M. Herrmann, F. Gliem, H. Schmidt, G. Leibeling, H.Kettunen, and V. Ferlet-Cavrois, "Heavy-ion sensitivity of 16/32-Gbit NAND-Flash and 4-Gbit DDR3 SDRAM," in *Proc. Radiation Effects Data Workshop*, 2012, pp. 114–119, IEEE.

[Irom, 2007] F. Irom and D. N. Nguyen, "Single Event Effect Characterization of High Density Commercial NAND and NOR Nonvolatile Flash Memories," in *IEEE Transactions on Nuclear Science*, vol. 54, no. 6, pp. 2547-2553, Dec. 2007.

[Irom, 2009] F. Irom, D. N. Nguyen, R. Harboe-S⊘rensen and A. Virtanen, "Comparison of TID response and SEE characterization of single- and multi-level high density NAND Flash memories," *Radiation and Its Effects on Components and Systems (RADECS), 2009 European Conference on*, Bruges, 2009, pp. 606-608.

[Irom, 2010] F. Irom, D. N. Nguyen, M. Bagatin, G. Cellere, S. Gerardin and A. Paccagnella, "Catastrophic Failure in Highly Scaled Commercial NAND Flash Memories," in *IEEE Transactions on Nuclear Science*, vol. 57, no. 1, pp. 266-271, Feb. 2010.

[Irom, 2012] F. Irom, D. N. Nguyen, G. R. Allen and S. A. Zajac, "Scaling Effects in Highly Scaled Commercial Nonvolatile Flash Memories," *2012 IEEE Radiation Effects Data Workshop*, Tucson, AZ, 2012, pp. 1-6.

[Jacob, 2008] Jacob Stéphanie, « Intégration, caractérisation et modélisation des mémoires non volatiles à nano-cristaux de silicium », Thesis manuscript, April 2008.

[Micron, 2006] TN-29-19: NAND Flash 101, Technical Note, 2006.

[Nguyen, 1998] D.N. Nguyen, C.I. Lee, and A.H. Johnston," Total ionizing dose effects on Flash memories", *1998 IEEE Radiation Effects Workshop Record*, p100.

[Nguyen, 1999] D.N. Nguyen, S.M. Guertin, G.M. Swift, and A.H. Johnston," Radiation Effects on advanced Flash memories," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1744-1750, Dec 1999.

[Nguyen, 2002] D. N. Nguyen and L. Z. Scheick, "SEE and TID of emerging non-volatile memories," *Radiation Effects Data Workshop, 2002 IEEE*, 2002, pp. 62-66.

[Nguyen, 2003] D. N. Nguyen and L. Z. Scheick, "TID, SEE and radiation induced failures in advanced Flash memories," *Radiation Effects Data Workshop, 2003. IEEE*, 2003, pp. 18-23.

[Oldham, 1993] T. R. Oldham, K. W. Bennett, J. Beaucour, T. Carriere, C. Poivey, and P. Garnier, "Total dose failures in advanced electronics from single ions," *IEEE Trans. Nucl. Sci.*, vol. 40, no. 6, pp. 1820–1830, Dec. 1993

[Oldham, 2006] T. R. Oldham *et al.*, "SEE and TID Characterization of an Advanced Commercial 2Gbit NAND Flash Nonvolatile Memory," in *IEEE Transactions on Nuclear Science*, vol. 53, no. 6, pp. 3217-3222, Dec. 2006.

[Oldham, 2008] T. R. Oldham *et al.*, "TID and SEE Response of Advanced 4G NAND Flash Memories," *2008 IEEE Radiation Effects Data Workshop*, Tucson, AZ, 2008, pp. 31-37.

[Oldham, 2011] T. R. Oldham *et al.*, "Investigation of Current Spike Phenomena during Heavy -Ion Irradiation of NAND Flash Memories," *2011 IEEE Radiation Effects Data Workshop*, Las Vegas, NV, 2011, pp. 1-9.

[Poivey, 1994] C. Poivey, T. Carriere, J. Beaucour, and T. R. Oldham, "Characterization of single hard errors (SHE) in 1M-bit SRAMs from single ions," *IEEE Trans. Nucl. Sci.*, vol. 41, no. 6, pp. 2235–2239, Dec. 1994.

[Schmidt, 2008] H. Schmidt, D. Walter, F. Gliem, B. Nickson, R. Harboe-Sorensen and A. Virtanen, "TID and SEE Tests of an Advanced 8 Gbit NAND-Flash

Memory," *2008 IEEE Radiation Effects Data Workshop*, Tucson, AZ, 2008, pp. 38-41.

[Wester, 2004] W. Wester, C. Nelson and J. Marriner, "Proton irradiation effects on 2Gb Flash memory," *Radiation Effects Data Workshop, 2004 IEEE*, Atlanta, GA, USA, 2004, pp. 68-71.

Chapter 6

A Case Study: The MTCube Science Mission

6.1 Introduction

The radiation test qualification, whether TID testing or SEE testing, of electronic components and more generally of electrical, electronic and electromechanical (EEE) components, is closely related to the space project. Depending on the type of orbit (around the Earth, around the Sun, around another planet or any other space object), as well as the surroundings and the location of the component, the radiation environment may be severely different. However, radiation testing standards have been made in order to test the radiation effects in a systematic way. For example for SEE testing, the two most famous standards are the [ESCC25100, 2014] and the [JESD57, 1996]. However, many points remain not perfectly defined because these standards address various types of EEE components. For example, no specific guidance is provided to implement dynamic testing: which sort of test should be used? Of course, for such a generic guideline, it is difficult to address specifically all types of testing and methods depending on the specificities of each EEE component.

In this chapter, the generic SEE radiation testing of the previous memories will be used in the frame of the MTCube mission. This will provide an example of how to use the experimental data in a concrete project, not only from the scientific point of view, but also the engineering point of view.

From the scientific point of view, one of the direct applications of SEE testing is to estimate the Single Error Rate (SER) of a given component during its mission, which gives an idea of the number of errors expected during the mission lifetime. In a given space project, this SER is then usually confronted to requirements on the maximum level of SER allowed for a given component. However, in the context of MTCube, the SER will provide a way to compare experimental and simulation results with in-orbit data. In order to do so, the OMERE freeware tool [OMERE, 2016], built by TRAD under the supervision of CNES, was used. The OMERE software enables the possibility to simulate the radiation environment for a given Earth orbit and estimate, based on various models, the TID and SER of components inside a spacecraft. However, as it will be explained in the current chapter, SER estimations are based on many assumptions, models and limited experimental results. The uncertainty associated with these SER results is thus high. Comparing estimated SER values with actual ones obtained in-orbit, may provide valuable insights in the goodness of the methodology that is used to estimate those error rates. Besides enabling this, the science payload of the satellite is designed in order to map the errors along its orbit, as it will be explained in section 6.4.1.

From the engineering point of view, the payload subsystem is designed in order to maximise the number of experiments as well as to take into account the constraints of the 1U CubeSat on which will be based the MTCube platform. Furthermore, the experimental data gathered from the tested memories will be used in order to estimate the amount of data based on the calculated SER, which provides a key parameter to assess the good design of the data handling of the platform: if the amount of data is bigger than the capacity of the memory where the information is stored during two communication links with the ground station, then some of the science data might be lost or, the science experimental outcome will be downscaled.

Finally, not only the memories will be subjected to the space environment but also all the other components used on the RES Experiment board. It is hence important, from an engineering point of view, to ensure that the experiment will be properly working in this specific environment. To do so, the latest RES Experiment prototype, which is the copy of the final flight model with some minor

modifications (presence of test points) has been subjected to high-energy protons in order to ensure the good payload subsystem functionality.

6.2 In-orbit Single Error Rate (SER) methodology

6.2.1 Weibull fitting

Based on the experimental data, as those obtained in chapter 3, 4 and 5 for various types of memories, the SEE cross-sections are calculated for various heavy-ion LET and various proton energies. As the cross-section can be obtained only for a limited number of energies and LETs (due to cocktail beam limitations, and/or time and/or financial constraints) the cross-section has to be interpolated in between the calculated data. Additionnaly, extrapolating – with care - the data may allow to estimate the cross-section even for very high or very low energies/LET, at which the component could not be tested. The most standard approach for the in-orbit rate calculation is to fit the experimental data to a Weibull function [Petersen, 1996] defined in Equation 4, which is fully characterised by four parameters: the on-set parameter (x_0), the saturation cross-section (σ_{sat}), the width parameter (W) and a dimensionless exponent (S). The on-set parameter is also called the threshold LET value for heavy-ions (or the energy threshold value for protons): this corresponds to the energy at which errors may start occurring on the memory, below this value, the memory is supposed not to be affected by any error.

$$\sigma(x) = \sigma_{sat}\left(1 - e^{-\left(\frac{x-x_0}{W}\right)^S}\right) \; if \; x > x_0$$

$$\sigma(x) = 0 \; if \; x \leq x_0$$

Equation 4: Weibull curve used for fitting heavy-ion and proton data: x represents either the LET for heavy-ions or the energy for protons and x_0 the LET or energy threshold.

Nevertheless, Weibull curves have been used to fit the data without any actual physical meaning of the Weibull parameters [Morris, 2010]. Indeed, a different fitting curve may have the consequence of giving a different in-orbit SER prediction value.

Previously, Weibull curves were used to fit heavy-ion experimental cross-section, and protons were fitted by a two-parameter Bendel function [Stapor, 1990]. However, nowadays, Weibull fits are generally used for both heavy-ion and proton experimental data fitting purposes. In this work, the fitting function considered for both the heavy-ion and the proton cross-section will be a Weibull curve based on the common approach. Indeed, the software tool OMERE that will be quickly presented in section 6.2.3, only uses Weibull fits for heavy-ions (for protons it is also possible to fit the curves with a Bendel function). In some cases, where the cross-section, especially for high energy protons, is very similar for different energies, a constant cross-section will be assumed (as a simplified assumption).

6.2.2 Sensitive volume geometry

Concerning the error rate due to direct ionization processes, the notion of sensitive volume shall be introduced. The Sensitive Volume (SV) is a 3D shape defined as the volume near the critical node of a component in which the deposited charge may trigger an upset. The critical charge is then defined as the minimum charge able to trigger an upset (Q_{crit}).

The most commonly used, and the most simple, method is the RPP model (Rectangular Parallelepiped Parallelogram) [Pickel, 1980] which considers the SV as being of a parallelepiped shape, in which, all the generated charge is collected, i.e. participating to a possible upset if the charge is above Q_{crit}. The shape does not necessarily have a direct physical sense but allows a simplified representation of the

complex particle-matter interactions and is a method that can be easily computed in SEE error rate prediction tools: indeed, diffusion and funnelling effects are considered somehow taken into account in the shape of the SV (if the SV is experimentally calculated).

Other more improved methods exist such as the IRPP model [Petersen, 1997], which builds on the RPP method and further improves it by considering several imbricated SVs having different weights to account for partial charge collection, especially when the particle strike is further away from the sensitive node. The IRPP method only requires the Weibull fitting parameters as well as the depth of the SV. The upset rate is then calculated based on the geometry of the SV and the direction of the ionizing particle. The cross-section allows determining the dimensions of the SV. In the OMERE software, the SV depth (SV_{depth}) and the threshold LET are related to the critical charge (Q_{crit}) Equation 5 (at normal incidence). Hence, finding experimentally the LET threshold may have a direct proportional impact on the critical charge and hence an increased effect on the SER. This aspect is also true for the depth of the SV.

$$Q_{crit} = LET_{th} \times \alpha \times SV_{depth}$$

Equation 5: Critical charge (in pC) calculation used on the OMERE software. α is equal to 1/22.5 pC/MeV, and is the inverse of the energy required to create 1 pC of charge assuming that 3.62 eV are required to generate an electron-hole pair in silicon. LET_{th} is in MeV.cm²/g and SV_{depth} in g/cm².

For heavy-ions, the knowledge of the shape of the SV as well as the critical charge is then required as an input of OMERE for the calculation of the error rate when the information regarding the environment is available. These parameters are device dependant and may change drastically from one component to another. Such information is not required by OMERE for high-energy protons.

6.2.3 Space radiation environment models & SEE rate estimation: use of OMERE

Based on the fitting curve characterising the sensitivity of the memory and the SV model, it is possible to estimate the direct ionization induced upset rate. To do so, the radiation environment at which is exposed the component must be first determined. Several models, based on experimental data, have been developed and are implemented in the OMERE tool. Based on the orbital parameters defined by the user, it is possible to estimate the radiation environment in the form of heavy-ion (resp. proton) fluence or flux energy spectra.

The second step is to take in account the equivalent shielding thickness, which any given particle will have to cross in order to reach the memory die location on the spacecraft. When unknown, conventional values (such as 100 mil) may be used in order to estimate the SER. However, when the satellite design is at an advanced stage, the equivalent shielding may be estimated by tools such as FASTRAD (see chapter 1 section 4.1.5.2 for the FASTRAD model of the RES Experiment). By using ray tracing methods, FASTRAD software is able to calculate the equivalent aluminium shielding thickness of a given component. As discussed in chapter 1 section 2.1.2, the shielding thickness has an impact on the transported environment, which will be "seen" by the components. The transport of the radiation environment by OMERE may be done by subroutines from CREME86 or SRIM2006. Based on all the previous knowledge, it is possible to estimate to error rate, which is done by using the CREME86 UPSET() subroutine which uses the IRPP model [CREME86, 2016].

Regarding nuclear reactions (protons at high energies), the upset rate is simply estimated by the cross-section integrated with the proton mission fluence energy spectra model.

If no experimental data is provided for protons, two commonly known methods exist in order to predict the proton cross-section based on the heavy-ion experimental data: the PROFIT [Calvel, 1996] and the SIMPA [Doucin, 1994] methods. In [Weulersse, 2011] a description is made on the

limitations of both methods. The PROFIT model is based on the assumption that all cells have the same SV but different threshold LETs. It is now proved to be an incorrect assumption [Petersen, 1996]. All nuclear reactions are assumed to be elastic (only Si recoils) and only LET < 14.9 MeV.cm²/mg are considered (max LET of Si recoils in Si) which underestimates the actual energy deposited in the SV especially for sensitive components. The SIMPA method is based, on the other hand, on the heavy-ion cross-section recalculated this time in function of the energy deposited in the SV (hence it is required to provide the SV depth), which is then convoluted to a data base of experimental data on the probability of protons depositing a certain amount of energy. In the OMERE tool, the parameters used to model the probability of protons depositing a given energy have been fixed to the values provided in [Doucin, 1994] for 6 µm although they were found to vary with the SV depth.

Finally, it is worth mentioning that the current version of OMERE (version 4.2) [OMERE, 2016] does not consider direct ionization, which however occurs at low energy protons.

6.3 In-orbit Single Error Rate (SER) estimation

6.3.1 Weibull curve approximation for the tested memories

Based on the bit and event cross-sections calculated for the SRAM memories (chapter 3), as well as the bit cross-sections of the FRAM (chapter 4) and the Flash memories (chapter 5), the Weibull fitting parameters for heavy-ion have been obtained for those memories, and are presented below (Table 16). The fitting has been performed using the OMERE tool according to the methodology specified in the OMERE User Manual [OMERE UM, 2014]. For all memories tested in dynamic mode: the most stressful dynamic March test has been chosen: hence for both SRAM memories, the March Dynamic Stress test is chosen; for the FRAM, the March C- test is chosen. The Flash memory, as previously mentioned, will be tested in static biased mode with a "solid 0" pattern.

The scrambling of the FRAM and the Flash memories being unknown, it is not possible to obtain their event cross-section. Due to current limitations of the OMERE software, it is neither not possible to take into account the direct ionization proton peak for the SRAM memories. For the 65 nm SRAM LET threshold value of the heavy-ion static cross-section, the LET threshold value has been manually changed to the value obtained for the clustered cross-section as the default value was set at 0.001 MeV.cm²/mg. Similarly, for the Flash heavy-ion static cross-section and the FRAM heavy-ion dynamic cross-section LET threshold, the values have been modified by the default value of 0.001 MeV.cm²/mg to 0.1 MeV.cm²/mg.

Heavy-ions static	Bit cross-section Weibull parameters				Event cross-section Weibull parameters			
	σ_{sat}	LET_{th}	W	S	σ_{sat}	LET_{th}	W	S
90nm SRAM	8.44×10^{-8}	1.08	35.31	1.24	1.43×10^{-8}	1.08	12.73	0.76
65nm SRAM	7.90×10^{-8}	1.04*	23.57	1.43	6.07×10^{-9}	1.04	4.20	0.6
FRAM	4.57×10^{-11}	1.8	6.66	0.72	-	-	-	-
Flash	1.60×10^{-10}	2.0*	29.03	2.51	-	-	-	-
Flash VL	8.77×10^{-3}	0.8	63.17	2.66	-	-	-	-
Flash unbiased	1.59×10^{-10}	1.63	28.3	1.9	-	-	-	-

Table 16: Weibull fitting parameters for the 90nm SRAM, 65nm SRAM, FRAM and Flash memories heavy-ion static cross-section selected for the RES Experiment payload of the MTCube CubeSat. An asterisk next to a value means that the parameter has been changed manually from the default value calculated by the OMERE software (*). As the scrambling is unknown for the FRAM and Flash devices, it is not possible to apply clusterisation technics which in turn cannot provide any Weibull event cross-section parameters for those memories.

Heavy-ions dynamic	Bit cross-section Weibull parameters				Event cross-section Weibull parameters			
	σ_{sat}	LET_{th}	W	S	σ_{sat}	LET_{th}	W	S
90nm SRAM	$5.16x10^{-6}$	1.08	18.67	1.80*	$4.66x10^{-8}$	1.08	33	0.8
65nm SRAM	$6.44x10^{-8}$	0.97	32.37	1.42	$6.26x10^{-9}$	0.97	8.9	0.7
FRAM	$9.55x10^{-8}$	1.77	9.52	1.1	-	-	-	-
Flash	-	-	-	-	-	-	-	-
Flash VL	$2.86x10^{-10}$°	3.00°	-	-	-	-	-	-

Table 17: Weibull fitting parameters for the 90nm SRAM, 65nm SRAM, FRAM and Flash memories heavy-ion dynamic cross-section selected for the RES Experiment payload of the MTCube CubeSat. An asterisk next to a value means that the parameter has been changed manually from the default value calculated by the OMERE software (*).

In *Table 18* and Table 19 are presented the Weibull fitting parameters for the proton static and dynamic experimental cross-sections. As direct ionization is not considered in the calculation of the SER, the energy threshold was chosen to be 3 MeV in order not to count effects due to direct ionization. For the 65nm SRAM Weibull fitting parameters, the default values calculated by OMERE were not satisfactory and were tuned to improve the fitting of the data. The Flash proton cross-section being almost constant, Weibull parameters could not be fitted and hence a step function had to be chosen and cross-section value extrapolated down to 3 MeV. All values differing from the default values calculated by OMERE are accompanied in the below tables by an asterisk (*).

Protons static	Bit cross-section Weibull parameters				Event cross-section Weibull parameters			
	σ_{sat}	E_{th}	W	S	σ_{sat}	E_{th}	W	S
90nm SRAM	$6.52x10^{-14}$	3.00*	16.27	1.16	$4.88x10^{-14}$	3.00*	17.02	0.45
65nm SRAM	$1.97x10^{-13}$	3.00*	5.02	0.95	$1.79x10^{-13}$	3.00*	3.00*	0.50*
FRAM	-	-	-	-	-	-	-	-
Flash	$9.69x10^{-17}$°	3.00°	-	-	-	-	-	-
Flash VL	$2.86x10^{-10}$°	3.00°	-	-	-	-	-	-

Table 18: Weibull fitting parameters for the 90nm SRAM, 65nm SRAM, and Flash memories proton static cross-section selected for the RES Experiment payload of the MTCube CubeSat. An asterisk next to a value means that the parameter has been changed manually from the default value calculated by the OMERE software (*). Values (°) calculated for the Flash memory as approximated by a step function starting at E_{th} with a constant cross-section value of σ_{sat}.

Protons dynamic	Bit cross-section Weibull parameters				Event cross-section Weibull parameters			
	σ_{sat}	E_{th}	W	S	σ_{sat}	E_{th}	W	S
90nm SRAM	$9.30x10^{-12}$	3.00*	40.30	2.68	$5.27x10^{-14}$	3.00*	5.93	0.51
65nm SRAM	$7.43x10^{-14}$	3.00*	8.85	0.57	$5.52x10^{-14}$	3.00*	3.59	0.30
FRAM	$4.02x10^{-18}$	3.00*	1.16	0.32	-	-	-	-
Flash	-	-	-	-	-	-	-	-

Table 19: Weibull fitting parameters for the 90nm SRAM, 65nm SRAM, and FRAM memories proton dynamic cross-section selected for the RES Experiment payload of the MTCube CubeSat. An asterisk next to a value means that the parameter has been changed manually from the default value calculated by the OMERE software (*).

6.3.2 Other approximations used for the SER estimation

The current OMERE software versions (4.0 and 4.2), allows to estimate the radiation environment for a given orbit without considering the orbital parameter drifts. In the case of MTCube, assuming the orbital parameters considered in chapter 1, the altitude will only slightly reduce from 650 km to about 649 km and remain circular: hence the radiation environment will remain the same.

Regarding the equivalent aluminium shielding thickness assumption, a FASTRAD model was built under work carried at the University Space Center (CSU) [GOURDIN, 2016] to which was added the FASTRAD payload model presented in chapter 1. For all memories, the worse equivalent aluminium thickness was calculated to be 2 mm. This will be the value considered for the estimation of the environment to which are exposed the memories.

Finally, regarding the SV depth (or thickness), it is generally assumed, by the radiation community, to use a standard 2 µm value.

Concerning the staked memories from 3D Plus, the error rate will be multiplied by the number of layers (four for the MRAM, and three for the FRAM, as one of the FRAM layers will be used as the main memory buffer and not for the science experiment).

6.3.3 In-orbit average rate calculation for the MTCube Science Experiment

In order to estimate the final SER of the memories on-board the RES Experiment, the same orbital and radiation environment parameters and models, as those presented in chapter 1, have been used except for the launch date, which was updated at the time of the calculation to reflect the new possible launch date. These parameters are briefly summarised below:

- 650 km altitude circular orbit;
- 98° inclination;
- 360 LAN, E = 0°
- Launch in 2017 for a 2 year mission duration
- Radiation environment model: AE8MAX/AP8MAX, ESP (solar proton), confidence level of 95%.

The results are summarized in Table 20 (unclustered or total SER) and Table 21 (clustered SER). For the FRAM and the Flash memory, the scrambling being unknown, the clustering could not be properly done. In Table 21, FLASH VL is related to the cross-section of the Vertical Lines (VL – detailed chapter 5) detected in static mode. Some tests, such as for example, unbiased testing of the FRAM under proton has not been performed due to time constraints; some other types of testing (i.e. unbiased testing of SRAM) does not make physical sense, or dynamic testing of the Flash memory is not foreseen on the present RES Experiment. These cases are thus left empty (full black boxes).

Furthermore, in order to calculate the number of errors per memory per day (usual units for in-orbit SER), each value was multiplied by the memory capacity: for the Flash memory, the value is 64 MB, for the 90 nm SRAM, it is 32 Mb, for the 65 nm SRAM, it is 16 Mb, for the FRAM finally, the value is 4 Mb. In order to take into account the fact that the FRAM memory is actually a stack of 3 single FRAM memories (and one additional layer used as the memory buffer of the RES Experiment – see section 6.4.1) the SER has been multiplied by the number of stacked dies. The results are finaly summarized in Table 22 (unclustered or total SER) and Table 23 (clustered SER).

Total	Heavy-ion SER (#/day/bit)			Proton SER (#/day/bit)			Total SER (#/day/bit)		
	U	**S**	**D**	**U**	**S**	**D**	**U**	**S**	**D**
90nm SRAM	-	$6.64x10^{-7}$	$1.53x10^{-4}$	-	$5.90x10^{-7}$	$5.06x10^{-5}$	-	$1.25x10^{-6}$	$2.04x10^{-4}$
65nm SRAM	-	$6.88x10^{-7}$	$3.68x10^{7}$	-	$2.23x10^{-6}$	$7.43x10^{-7}$	-	$2.90x10^{-6}$	$1.11x10^{-6}$
FRAM	0	$6.61x10^{-12}$	$2.23\ x10^{-6}$	-	-	$4.59x10^{-11}$	0	$6.61x10^{-12}$	$2.23x10^{-6}$
Flash (512/8) MB	$1.97x10^{-12}$	$3.97x10^{-13}$	-	-	$1.22x10^{-9}$		$1.93x10^{-12}$	$1.22x10^{-9}$	-

Table 20: Summary of the estimated unclustered error rate per bit for the RES Experiment selected memories. U = unbiased, S = static, D = dynamic. The black cells are values that cannot be calculated. The calculation assumes 2 mm of equivalent Al shielding and 2 µm of sensitive volume depth.

Clustered	Heavy-ion SER (#/day/bit)			Proton SER (#/day/bit)			Total SER (#/day/bit)		
	U	**S**	**D**	**U**	**S**	**D**	**U**	**S**	**D**
90nm SRAM	-	$3.81x10^{-7}$	$9.74x10^{-7}$	-	$4.21x10^{-7}$	$5.53x10^{-7}$	-	$8.02x10^{-7}$	$1.53x10^{-6}$
65nm SRAM	-	$2.57x10^{-7}$	$1.85x10^{-7}$	-	$2.02x10^{-6}$	$5.68x10^{-7}$	-	$2.28x10^{-6}$	$7.53x10^{-7}$
FRAM	-	-	-	-	-	-	-	-	-
Flash	-	-	-	-	-	-	-	-	-
Flash VL (#/day/memory)	-	$5.32x10^{-2}$	-	-	$3.59x10^{-3}$	-	-	$5.68x10^{-2}$	-

Table 21: Summary of the estimated clustered error rate per bit for the RES Experiment selected memories. U = unbiased, S = static, D = dynamic. The black cells are values that cannot be calculated. The calculation assumes 2 mm of equivalent Al shielding and 2 µm of sensitive volume depth. FLASH VL stands for the vertical line cross-section and is provided in different units (#/day/memory). As the scrambling was unknown for the FRAM and the Flash memories, clustered SER cannot be calculated.

Total	Heavy-ion SER (#/day/memory)			Proton SER (#/day/memory)			Total SER (#/day/memory)		
	U	S	D	U	S	D	U	S	D
90nm SRAM	-	$2.23x10^{1}$	$5.13x10^{3}$	-	$1.98x10^{1}$	$1.70x10^{3}$	-	$4.21x10^{1}$	$6.83x10^{3}$
65nm SRAM	-	$1.15x10^{1}$	$6.17x10^{0}$	-	$3.74x10^{1}$	$1.25x10^{1}$	-	$4.90x10^{1}$	$1.86x10^{1}$
FRAM	0	$8.32x10^{-5}$	$2.81x10^{1}$	-	-	$5.78x10^{-4}$	0	$8.32x10^{-5}$	$2.81x10^{1}$
Flash (512/8) MB	$1.32x10^{-4}$	$2.66x10^{-5}$	-	-	$8.19x10^{-2}$	-	$1.32x10^{-4}$	$8.19x10^{-2}$	-

Table 22: Summary of the estimated unclustered error rate per memory for the RES Experiment selected memories. U = unbiased, S = static, D = dynamic. The black cells are values that cannot be calculated. The calculation assumes 2 mm of equivalent Al shielding and 2 µm of sensitive volume depth.

Clustered	Heavy-ion SER (#/day/memory)			Proton SER (#/day/memory)			Total SER (#/day/memory)		
	U	S	D	U	S	D	U	S	D
90nm SRAM	-	$1.28x10^{1}$	$4.19x10^{1}$	-	$1.41x10^{1}$	$1.82x10^{1}$	-	$2.69x10^{1}$	$6.05x10^{1}$
65nm SRAM	-	$4.31x10^{0}$	$3.10x10^{0}$	-	$3.39x10^{1}$	$9.53x10^{0}$	-	$3.82x10^{1}$	$1.26x10^{1}$
FRAM	-	-	-	-	-	-	-	-	-
Flash	-	-	-	-	-	-	-	-	-
Flash VL	-	$5.32x10^{-2}$	-	-	$3.59x10^{-3}$	-	-	$5.68x10^{-2}$	-

Table 23: Summary of the estimated clustered error rate per memory for the RES Experiment selected memories. U = unbiased, S = static, D = dynamic. The black cells are values that cannot be calculated. The calculation assumes 2 mm of equivalent Al shielding and 2 µm of sensitive volume depth. FLASH VL stands for the vertical line cross-section. As the scrambling was unknown for the FRAM and the Flash memories, clustered SER cannot be calculated.

6.3.4 Pessimistic case soft error rate analysis

Finally, in order to provide a pessimistic scenario for the data collection of the RES Experiment, a special case was considered by combining slight variations from the calculated Weibull parameters resulting in higher cross-sections, this, in order to consider the impact of slight changes of those parameters on the total error rate. Values were modified as follows: the LET threshold was reduced by 0.5 MeV.cm²/mg, the *S*, *W* values were reduced by 10%. On the other hand, σ_{sat} was increased by 10%, the wall thickness was kept at 2 mm and the SV thickness was set to 1 and 2 µm. The results are shown in Table 24 for unclustered events.

TOTAL		**Protons**	**Heavy-ions**	**Total**	**Heavy-ions**	**Total**
Sensitive volume thickness		**1 & 2 µm**	**2 µm**	**2 µm**	**1 µm**	**1 µm**
90nm SRAM	Static	15 %	283 %	156 %	679 %	366 %
90nm SRAM	Dynamic	21 %	258 %	199 %	431 %	329 %
65nm SRAM	Static	12 %	236 %	65 %	573 %	144 %
65nm SRAM	Dynamic	11 %	270 %	97 %	653 %	224 %
FRAM	Static	-	237 %	-	**1413 %**	-
FRAM	Dynamic	11 %	117 %	117 %	258 %	258 %
Flash	Static	11 %	250 %	11 %	**1510 %**	11 %

Table 24: Worst case SER of the RES Experiment memories.

What can be seen is that in this pessimistic case, the increase may go up to almost a factor 2.9 (for the 90 nm SRAM memory in static mode) when the SV thickness is of 2 µm but can even go up to an order of magnitude increase in the case when the SV thickness is of 1 µm. This high sensitivity to the SV thickness was only calculated for the FRAM and Flash memories in static mode, the highest contribution to the increase in SER being due to the reduction in the SV thickness.

Concerning the FRAM in static testing, the 2/3 of the rate increase is due to the combination of the SV depth decreasing and the LET threshold reduction (each of these parameters taken separately are responsible respectively for a 25% and 9% increase). Regarding the Flash memory in static mode, the combination of SV depth decrease and LET threshold reduction only accounts for 38% of the increase, the elbow region of the Weibull fit combined with the SV depth decrease seems to have a higher impact (50% increase).

The average total increase for all memories varies from almost none to 3.6 times in the pessimistic case considering a 2 µm SV thickness and up to 6.3 times increase with a 1 µm SV thickness. Hence, as it can be seen in this case, the impact of the several parameters used for the SER calculation is non-negligible on the final SER value.

Based on those results it can be clearly seen that the proton error rate does not seem too sensitive to small changes for this orbit (< 20 %). The biggest impact is on the heavy-ion test results for which defining the SV depth as being set at 2 µm (as common practice requires it for this sort of calculation) does have a great impact on the error rate, even further when combined to other parameter uncertainties (and this, in a non-linear way). Besides, the biggest parameter impact does not seem to be necessarily the same as seen for the FRAM and Flash cases.

6.4 Impact of the memory SER on the RES Experiment

6.4.1 Nominal mode testing approach

The originality of the RES experiment resides in the fact that the memories will be stimulated both in static and dynamic mode. In order to account for one of the main constraints of a 1U CubeSat platform which is power limitation, memories will be tested in dynamic mode in turn, in a so-called Round Robin scheme: at each time, one memory will be tested in dynamic mode, while the other memories will be simply biased and hence tested in static mode. This strategy will allow maximizing the science return as well as limiting as much as possible the power requirements for the payload.

As mentioned above, for all memories except the Flash memory only tested in retention mode, the dynamic test selected for each memory is the one that resulted to be the most stressful one for each type of memory. Hence, for both SRAM memories, the March Dynamic Stress test will be implemented, whereas for the FRAM memory the March C- test will be selected. Although out of the scope of the present work, the MRAM will also be tested in dynamic mode through the March C- stimuli. The Flash memory on the other hand will be tested in retention mode biased and unbiased with a solid '0' pattern, which is the pattern the most sensitive to radiation as seen in chapter 5. For the remaining memories, as there is no pattern dependency on the SEE sensitivity, a checkerboard pattern is chosen for the static mode testing.

Each memory is power supplied through a anti-latchup circuitry based on COTS components, which will detect overcurrent and signal to the FPGA, SEL occurrences.

The FRAM memory being the most robust memory regarding SEE occurrences, one of the layers of the 4-layer 3D FRAM will be dedicated to store the experiment results and be, as such, the memory buffer of the science experiment. The experimental data will be stored and dumped to the OBDH subsystem when possible for downlink to Earth. Whether a bit flip detected on the memory due to a SEU, a SEFI or a micro-latchup or a SEL, the recorded event is logged in the memory buffer along with the timestamp of the event, the memory and addressing of the occurring event along with the faulty read word. All this information will enable to detect possible clusters of events, MCUs and SEFIs. The timestamp will enable to retrieve the location of the satellite where the error occurred allowing to map the errors in orbit for each memory during the two year nominal mission duration. The accuracy of the timestamp (200 ms) will be well above the accuracy requested for the MTCube mission (30 second accuracy).

6.4.2 Estimation of the average generated data

Based on the average SER of each memory, it is possible to estimate the average data that will be collected on the RES Experiment in the FRAM buffer. As each memory is being tested in dynamic mode once per Round Robin cycles, the remaining memories being kept in static mode, except for the Flash memories being only kept in retention mode (static mode), the average collected data can be calculated as per Equation 6:

$$Data_{science} = \left(\frac{1}{N_{RR}} \sum_{i=1}^{N_{RR}} \left(SER_{dyn_i} + (N_{RR} - 1) \times SER_{sta_i} \right) + \sum_{j=1}^{N_{\overline{RR}}} SER_{sta_j} \right) \times M$$

Equation 6: Equation estimating the average collected data for the MTCube mission.

$Data_{science}$ represents the amount of data in bits collected during 24h (one day), N_{RR} is the number of memories included in the Round-Robin (RR) test scheme (i.e. 9 memories), $N_{\overline{RR}}$ is the number of memories not included in the RR (i.e. the two Flash memories), SER_{dyn_i}, SER_{sta_i} and SER_{sta_j} the

SER of the *i* and *j* memories in dynamic or static mode (in error per memory per day); and finally M is the number of bits required to store one error which, in the case of the RES Experiment is 56 bits.

This calculation does not include of course the LEP contribution (not included in the SER of the memories), nor proton events on the FRAM (which, considering the experimental results is very likely extremely low). Furthermore, this calculation considered, on the other hand, that the 3D MRAM has a SER similar to the highest SER calculated (i.e. for the 90 nm SRAM) which is an extremely conservative assumption, along with an estimation of Vertical Lines that may occur on an entire column (2048 bits long) of both Flash memories according to their event rate. To this value is added an extra 20%, accounting for the additional few messages that may be added as well as the data for possible latch-up events. The final calculation gives the following results:

$Data_{science+20\%,\ normal}$ = 175 kbit/day or 11.0 kbit/orbit (assuming an orbit duration of 90 min).
$Data_{science+20\%,\ pessimistic}$ = 699 kbit/day or 43.7 kbit/orbit (assuming an orbit duration of 90 min).

Considering that the payload memory buffer (one of the FRAM memory layers) is of 4 Mb size, the science experiment may function in average (with no occurrence of major events, such as SEFI in SRAM) for slightly more than 24 days (or 6 days) continuously without emptying its memory buffer and without any loss of data. These calculations, not only are useful for mission simulations in order to ensure that the memory buffer, either the RES experiment or the main on-board computer, is sufficient to store the data, but also to evaluate the autonomous time the RES experiment may be able to work.

6.4.3 Solutions preventing a buffer overflow

As seen in section 6.4.2, the chances of having a science buffer overflow is very limited, as the science experiment is able to work autonomously without having to empty its buffer for 24 continuous days in average. However, in order to remain on the safe side, an "Error_limiter" parameter has been included in the design, which allows to simply count the number of errors above this "Error_limiter value" for a given memory in the case of an event generating a large amount of errors (thus data), like SEFI in SRAM memories, which could induce several thousands of bit errors as seen in chapter 3. All the errors below this value are recorded in the normal way (56 bits per error).

Furthermore, in the unlikely event of a buffer actually being full, the science experiment is designed to put all the memories in static (or retention) mode until the buffer is being able to get emptied. This allows, in the unexpected event of a buffer saturation to still be able to pursue some limited science considering the memories being in static mode. Furthermore, a second available data buffer is at disposal of the OBDH, which will host the experimental data (lowering the charge of the payload buffer) prior to the transmission to ground.

6.4.4 High proton energy testing

The latest RES Experiment prototype (prototype B – Figure 1) was functionally tested at PSI in Switzerland under high proton energies, in order to ensure that the payload is able to survive the severe proton irradiation, especially in the SAA (South Atlantic Anomaly) during the mission lifetime. The prototype hardware and software, as well as the experimental set-up has been fully designed and tested by the team, from the LIRMM laboratory, working on the payload subsystems. The prototype itself was manufactured and assembled by a French company: EdgeFlex [EdgeFlex, 2016]. This test was intended as a "GO/NO GO" test where, due to time constraints as previously mentioned, it was possible to test the memory at different energies and ensure that the functionality of the card remained enough for the card to be able to work. For such a test, a basic program was implemented on the FPGA in order to test, in static and dynamic mode, all the memories included in a Round Robin

scheme, and store the data in the memory buffer, as well as being able to retrieve the data. All these operations were being performed during irradiation.

Results showed that no latch-up events occurred on the FPGA, the CAN controller and transceiver and other components constituting the card. Memories recorded events that were stored and retrieved from the memory buffer. The memory was tested up to 10^{11} proton/cm² as per [ESCC25100, 2014] (estimated dose reaching 3.8 krad(Si)) at various energies (200 and 50 MeV) and resulted in no strange behaviour except once when the data was not retrieved (at a fluence of $5.3 * 10^{10}$ proton/cm² or a cumulated dose of 7 krad(Si)). The board was functional at the end of the irradiation. Subsequent testing resulted in functional errors and main current supply increasing from the initial 70 mA (@ 6V) to 150 mA in standby mode. The board was irradiated up to $1.78 * 10^{11}$ proton/cm² even when not functional at 200, 150 and 50 MeV (equivalent to a dose of 18.6 krad(Si)).

Nine weeks later, the memory was functionally tested in the laboratory and showed full functional recovery with every commands being functional. However, the main current was still higher than pre-irradiation tests (120 mA).

Heavy-ion irradiation of the entire board is much more difficult, as broad beams such as the one available at PSI for protons, does not exist at least in Europe. Furthermore, the energy of the heavy-ion beam should be sufficient to reach the sensitive volume of all tested components without having to delid them all. One solution could have been to test one-by-one each component of the RES Experiment to heavy-ion: however this is rarely done, especially in a low budget CubeSat mission, where it is difficult to afford and have enough time to test all parts. Furthermore, the usual financial resources for CubeSat mission are rather limited and purchasing RadHard components can be detrimental to the overall budget. The used approach, i.e. functional testing under proton beam, is the most beneficial in term of cost/risk ratio and this approach was recommended by ESA.

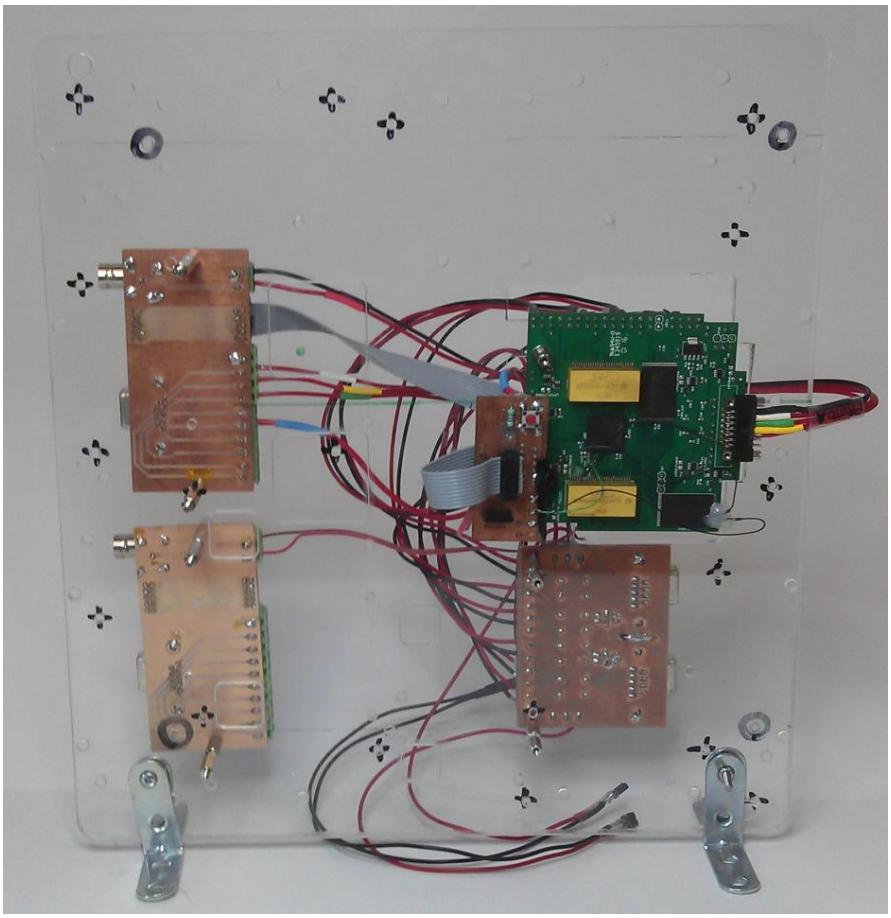


Figure 93: Set-up for high energy proton testing at PSI of the RES Experiment prototype B.

6.5 Conclusion

In this chapter, the assumptions and models commonly used to estimate the SER of components were presented. The experimental results from SEE testing of SRAMs (chapter 3), FRAM (chapter 4) and Flash (chapter 5), were applied to the case study of the MTCube project. Nevertheless, using similar methods, it is possible to estimate the SER for other types of Earth orbits using the OMERE software.

The results were calculated for the different tests (static and dynamic) for the memories selected for the MTCube RES Experiment. It was shown that the several parameters used to estimate the SER may induce relatively high variation of the SER which should be taken into account in the estimation of the amount of data, which may be gathered in-orbit.

The methodology used for the RES Experiment payload was presented, and it was shown how the design will allow maximising the science return and being at the same time as much as possible low in power consumption. A prototype version, very close to the flight model, was designed in-house. Finally, high energy proton irradiation testing enabled to ensure that all the components on the card will correctly function in-orbit, from the radiation environment point of view.

6.6 Bibliography

[Calvel, 1996] P. Calvel, C. Barillot, P. Lamothe, R. Ecoffet, S. Duzellier and D. Falguere, "An empirical model for predicting proton induced upset," in *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2827-2832, Dec 1996.

[CREME86, 2016] https://creme.isde.vanderbilt.edu/CREME-MC/help/upset-direct-ionization-induced-see-rate-calculation/?searchterm=UPSET, last accessed on the 23-09-2016.

[Doucin, 1994] B. Doucin *et al*., "Characterization of proton interactions in electronic components," in *IEEE Transactions on Nuclear Science*, vol. 41, no. 3, pp. 593-600, Jun 1994.

[EdgeFlex, 2016] http://www.edgeflex.fr/page.php?dst=home, last accessed on the 23-09-2016.

[ESCC25100, 2014] "Single Event Effects Test Method and Guidelines, ESCC No.25100, Issue 2, Oct.2014.

[Gourdin, 2016] A. Gourdin, "Analyses radiation et thermique du nanoSatellite MTCube", *CSU internship report*, version 0.4, 18-07-2016.

[Gupta, 2016] V. Gupta, A. Bosser, G. Tsiligiannis, F. Wrobel, F. Saigné, L. Dusseau, A. Zadeh, L. Dilillo, "MTCube Project : COTS memory SEE Ground-Test Results and In-Orbit Error Rate Prediction", 4S Symposium, La Valletta, Malta, 29 May – 30 June 2016.

[JESD57, 1996] "Test procedures for the measurement of single-event effects in semiconductor devices from heavy-ion irradiation," JEDEC Test Standard Dec. 1996, JESD57.

[Morris, 2010] R. D. Morris and C. C. Foster, "Cross-Section Estimation in the Presence of Uncertain Dosimetry," in *IEEE Transactions on Nuclear Science*, vol. 57, no. 6, pp. 3528-3536, Dec. 2010.

[OMERE, 2016] http://www.trad.fr/OMERE-Software.html, last accessed on the 23-09-2016.

[OMERE UM, 2014] OMERE Advanced Manual, V4.2, A. Varotsou, available in the folder when downloading the OMERE software tool, 19-01-2014.

[Petersen, 1996] E. Petersen, "Cross section measurements and upset rate calculations," in *IEEE Transactions on Nuclear Science*, vol. 43, no. 6, pp. 2805-2813, Dec 1996.

[Petersen, 1997] Petersen, E.L., “Single-event analysis and prediction”, *Short Course Notes*, ch. III, *IEEE Nuclear and Space Radiation Effects Conference*, Snowmass, 21 July 1997.

[Pickel, 1980] J. C. Pickel and J. T. Blandford, "Cosmic-Ray-Induced Errors in MOS Devices," in *IEEE Transactions on Nuclear Science*, vol. 27, no. 2, pp. 1006-1015, April 1980.

[Stapor, 1990] W. J. Stapor, J. P. Meyers, J. B. Langworthy and E. L. Petersen, "Two parameter Bendel model calculations for predicting proton induced upset [ICs]," in *IEEE Transactions on Nuclear Science*, vol. 37, no. 6, pp. 1966-1973, Dec 1990.

[Weulersse, 2011] C. Weulersse, "Développement et validation d’outils monte-carlo pour la prédiction des basculements logiques induits pou les radiations dans les mémoires SRAM très largement submicroniques", PhD Thesis, Montpellier, France, 6 Déc. 2011.

Conclusion

Final remarks and perspectives

Using state-of-the-art, cheap and power efficient COTS components, compared to their expensive RadHard counterparts, seems an attractive option for space applications not only to space industries but also space agencies. However, although this allows increasing the performance of the overall electronic system and helps reducing the overall hardware cost, the use of non-space components may increase the risk of the mission, particularly due to their unexpected behavior in a severe radiation environment from which a component cannot be fully protected from. This is true for high energetic particles, able to penetrate spacecraft shielding and reach directly or indirectly (by the secondaries they may generate) components inside the spacecraft shielding. This can lead to temporary or permanent damage and may result in a catastrophic loss of the mission if preventive measures have not been initially considered at the design phase.

These malfunctions are due to Single Event Effects (SEEs). Contrary to accumulative radiation effects (such as TID and TNID), SEEs may occur from the first day of the mission, even the protective magnetosphere of the Earth does not offer full protection in LEO, as spacecraft still have to pass through the South Atlantic Anomaly (SAA) and the polar cusps, where the environment is prone to SEEs. It is hence of prime important to test all new components, especially those with no flight heritage, to ensure their good behavior or take subsequent measures to avoid unwanted effects from highly energetic particles.

The presented study focused on the SEEs on various memory technologies. Memories are part of every electronic systems, whether embedded or not, and various memory technologies are used depending on their performance (non-volatility, access speed, power consumption and so on). Those memories respond differently to the SEE environment. The studied memories are: two SRAMs of different technology nodes (90 nm and 65 nm); a NAND Flash; and a FRAM memory. The general objective of this work aims at charaterising the SEE behavior of those memories by analyzing SEE test results performed during the last three years, as well as preparing a test bed in order to test those memories in actual operational conditions in space: this is the main objective of the MTCube 1U CubeSat. Due to delays in the conception of this nanosatellite, it has not been possible, until now, to compare the actual in-orbit results with those from the performed accelerated tests. However, based on the results obtained with the ground level tests, it was possible to estimate the error rate for the mission, which will then be compared with the actual data obtained when MTCube will be launched (expected in 2018 at the time of writing).

From a more general point of view, regarding the obtained experimental results, the difference in the SEE response of two different technologies is clear and expected: SRAM memory cells are much more sensitive than FRAM memory cells. However, when comparing dynamic tests results, SRAM and FRAM memories show similar bit cross-sections. Hence, although FRAM memories could almost be considered as error-free when used in static (or unbiased) mode, the knowledge and risk associated with its highly sensitive peripheral circuitry should be evaluated as a dynamic operation during the worse SEE environmental condition could create large scale SEFIs.

Furthermore, comparing again the results of SRAMs and FRAM SEE testing, it was shown that the same type of test is not necessarily the worse case for every device: for SRAMs, the March Dynamic Stress test provided the worse case dynamic bit cross-section, whereas for the FRAM memory, this test was the least stressful of all the performed dynamic tests. As there is no standard way of testing memories in dynamic mode, and since these tests are technology and application dependent, it is

important to consider the large variability of behaviors, especially in the case of critical applications. On the other hand, when performing static tests, some test protocols may perhaps use pseudo-static tests, in order to get periodical insights about how the current run is going, especially when the test run is very long. However, when the peripheral circuitry is very sensitive, this can lead to overestimating the static cross-section with soft errors induced in the periphery, as this was the case for the tested FRAM memory.

It is also essential to be aware about the basic internal structure of the tested component: as shown during the SRAM testing, it was realized, thanks to X-ray images, that the studied memory was composed of two stacked-dies. Performing heavy-ion testing without this knowledge and extrapolating to in-orbit rate estimation would have led to a factor of two discrepancy as the heavy-ions used in accelerated test facilities are often not able to penetrate deep enough to reach the bottom die, which is not the case for highly energetic GCRs in the space environment.

When performing SEE testing, calculating the bit-cross section in the different test modes provides only a partial picture for understanding the SEE sensitivity of the memory device. As it has been showed, for example for the 90 nm and 65 nm SRAM memories, along with a good knowledge of the behavior of the component and associated with a knowledge of the configuration and implementation on the chip, which may vary from one component to the other, it is important to study those results, in particular, the soft error per event due to a single particle rather than the mere numer of bit flips. Whereas bit cross-sections allow a representation of the SEE sensitivity of the memory from a usage perspective looking at the output of how many bits are flipped, which is, for example, an useful information to help select the most relevant ECC, looking as well at the event cross-section sheds light on the occurrence of a particular type of event due to a single particle. Besides, it appears to be the most suitable input, from a personal point of view, for the calculation of in-orbit errors as solely considering the total bit cross-section mixes all failure mechanisms in one. This is particularly true for SEFIs, for which, depending on the type and location of the error can generate from a few to several thousands of errors, due to a single particule. And although it is difficult to sometimes get detailed information regarding the scrambling/interleaving schemes within the memory, displaying logical bitmap results and analyzing them allows to spot possible failure mechanisms and group them as it was done for the NAND Flash and the FRAM memories.

In the future, as new memory technologies are matured enough for space applications, such as FRAM, MRAM or other types of memories, the most critical aspect of SEE testing will become the analysis of SEFIs and latch-up occurences. Two errors which are difficulty, if simply not, correctable using simple error correcting codes.

Considering the project application of MTCube and its science experiment – the RES Experiment, CubeSats are perfect test beds to carry in-orbit testing regarding radiation effects on components, especially, in commonly used low Earth orbits in order to carry SEE science experiments. For total dose testing, the study of low dose rate effects may also be useful. However, for TID studies a higher orbit altitude may be more convenient. First of all, carrying radiation testing does not impose stringent mission requirements: the satellite does not require any sort of stabilisation, which greatly reduces the mission complexity (and also the cost!); generally speaking, the power and weight cost of electronic components are not considered to be critical for a simple CubeSat level mission. Furthermore, the development of such CubeSat mission usually developed in several years, may allow to follow the high speed development of new technologies and help to constantly test in-orbit new components (e.g. FRAM, MRAM) for quicker use in more critical and challenging space applications.

Such small satellites can help, by providing actual results from space and by giving more insight into how to estimate the actual SEE error rate. Indeed results based on accelerated test present some limitations: the effect for example, of ommidirectionality of radiation particles is often not carried due to time and cost limitations as for the current study. As mentioned in [Pellish, 2010], when angle testing is performed, it is commonly done up to 60^{o} or 70^{o}; however, half of the GCR flux is at angles greater than 60^{o}! Hence, it is essential to also gather real environment results from components and not

only rely on accelerated testing. Such missions also allow to map the location of the occurring SEE events.

One important aspect to also consider, is the fact that more CubeSat missions are being studied for interplanetary missions: these missions provide an ideal and amazing test bed for characterisation in different radiation environments outside the protection offered by the Earth magnetic shield in Earth orbiting missions.

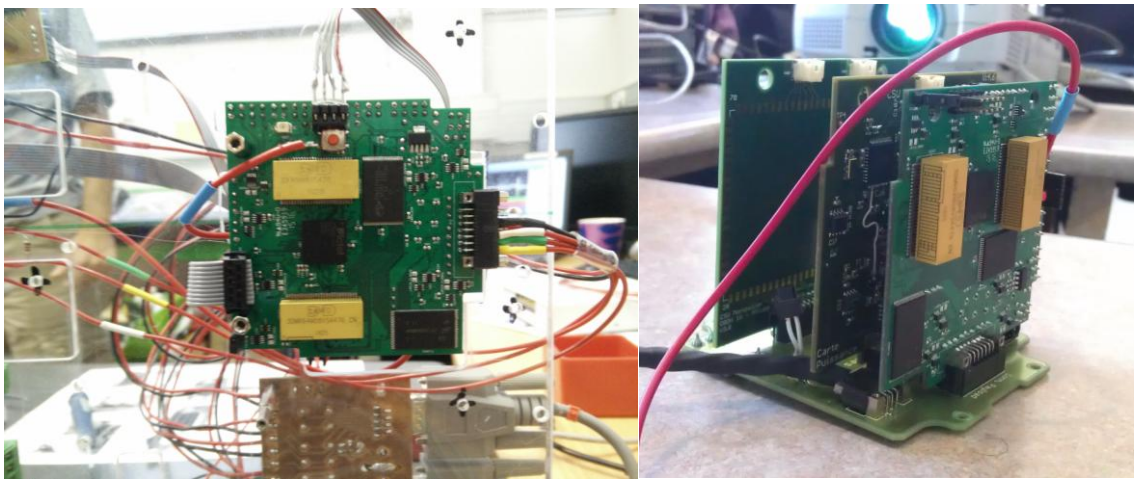


Figure 94: (left) Close-up of the RES experiment final engineering model getting ready for its first subsystem level proton testing mimicking some of the most intense SEE environment it will experience in LEO: (right) First integrated testing of the MTCube embryo: the main on-board computer system, the electrical power subsystem and the RES experiment successfully communicated: an exciting step forward toward the actual launch.

Unfortunately, several activities have not been carried due to time limitations in this study. Considering the possible next steps, besides finalizing the remaining work related to the RES experiment payload, several possible analysis and additional testing may be conducted in various areas. As a start, in order to fully SEE characterise all components, latch-up testing should be performed (including at different temperature levels and possibly different inclinations). Besides, although during the current study, test opportunities have been numerous, they were not sufficient to carry some high incidence angle testing in order to study also the impact of the generated errors on the angle. Regarding low energy proton testing, besides tests at different incidences, having more cross-section data at more energies between 600 keV and 10 MeV would be useful in the understanding of the mechanisms at play on the bottom die of the 90 nm SRAM. Low energy testing of the FRAM peripheral circuitry could also lead to interesting results. High energy proton testing of the FRAM at higher fluences could help provide more statistically meaningful results which we were not able to carry due to time constraints during the high energy proton tests. Flash memory has not been tested as well to low energy protons. The study of the mechanism underlying the appearance of vertical line errors, which were analyzed in this study, would be useful as they generate numerous errors. Dynamic test results of the Flash memory were obtained but they need to be more deeply analyzed. Similarly, although a MRAM memory was tested, the results have yet to be analyzed. Thanks to an opportunity that was offered at a very late stage of this study, microbeam testing of the FRAM revealed interesting results that still need to be analyzed but which enabled to isolate some types of errors that were noticed during heavy-ion and proton irradiations. These tests, if future collaboration allows it, are a complementary and useful approach to help understand the failure mechanisms and allow properly clusterizing the errors detected during full die irradiation. Testing in that way the Flash memory periphery may allow to trigger the VL mechanism to understand its origin. This, in turn, would allow to properly clusterise the bit errors and give insight into the likeliness of these events occurring in a given space radiation environment. Finally, performing TID analysis of these memories could complete the started radiation characterization, as well as, more generally, testing the effect of other parameters (clock frequency, temperature, power supply, for example). Regarding the error rate estimation, the effect of direct ionization has not at all been taken into account for the SRAM

memories especially and could lead to improve the overall error rate estimation if accompanied by additional low energy proton testing (and/or simulations).

From a broader perspective, the work carried during this thesis enables to select the most suited test for the mission, in the case of the MTCube project, the dynamic test allowing to maximize the memory's sensitivity. It also gives some more insights into the expected types of errors that may occur during the mission for each memory. Not only the calculated cross-sections provide a better understanding of the expected number of errors, being a comparision point to assess the goodness of the prediction tools and methods used for soft error rate estimations, these experimental results may also be reused on different satellites missions and orbits (e.g. different radiation environments) without the necessity of undergoing new extensive test campaigns. Furthermore, the RES experiment, tested against high energy protons may become an ideal test bed for new component in-orbit characterizations.

As a final and personal note, I believe, that one of the most exciting activities will be to analyse the in-orbit data acquired by MTCube (in Figure 94 is shown the first MTCube embryo), looking at actual bitmaps of memories tested in real space applications and confront those results with the accelerated testing performed and the error rate estimation calculated. Hence, I am eagerly waiting for the launch of MTCube and look forward for the first set of scientific data, hoping to be involved in the future analysis of those results.

List of publications

Journals:

- Bosser, **V. Gupta,** G. Tsiligiannis, C. Frost, Ali Zadeh, J. Jaatinen, A. Javanainen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel and L. Dilillo,"Methodologies for the Statistical Analysis of Memory Response to Radiation", Transactions on Nuclear Science, Vol 63, Issue 4,DOI:10.1109/TNS.2016.2527781, 2016.
- **V. Gupta**, A. Bosser, G. Tsiligiannis, A. Zadeh, A. Javanainen, A. Virtanen, H. Puchner,F. Saigné, F. Wrobel and L. Dilillo, "Heavy-ion Radiation Impact on a 4Mb FRAM under Different Test Modes and Conditions", IEEE Transactions on Nuclear Science, Vol 63, Issue 4, DOI: 10.1109/TNS.2016.2559943, 2016.
- L. Dilillo, G. Tsiligiannis, **V. Gupta**, A. Bosser, F. Saigné, F. Wrobel, "Soft Errors in COTS SRAM Memories", In press in Journal of Semiconductor Science and Technology (SST), 2016.
- A. Bosser, **V. Gupta**, G. Tsiligiannis, , A. Javanainen, H. Kettunen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel and L. Dilillo, "Investigation on MCU Clustering Methodologies for Cross-Section Estimation of RAMs", IEEE Transactions on Nuclear Science, Vol 62, Issue 6, DOI 10.1109/TNS.2015.2496874, pp 2620-2626, 2015.
- **V. Gupta**, A. Bosser, G. Tsiligiannis, A. Mohammadzadeh, A. Javanainen, A. Virtanen, H. Puchner,F. Saigné, F. Wrobel and L. Dilillo, "SEE on Different Layers of Stacked-SRAMs", IEEE Transactions on Nuclear Science, Vol 62, Issue 6, DOI 10.1109/TNS.2015.2496725, pp 2673 - 2678, 2015.
- G. Tsiligiannis, L. Dilillo, **V. Gupta**, A. Bosio, P. Girard, A. Todri-Sanial, A. Virazel, H. Puchner, A. Bosser, A. Javanainen, A. Virtanen, F. Wrobel, L. Dusseau and F.Saigne, "Dynamic Test Methods for COTS SRAMs", IEEE Transactions on Nuclear Science,Volume: 61 Issue: 6, 2014.

Conferences:

- A. L. Bosser, **V. Gupta**, A. Javanainen, G. Tsiligiannis, S.D. LaLumondiere, D. Brewe, V. Ferlet-Cavrois, S.P. Buchner, H. Puchner, F. Wrobel, F. Saigné, A. Virtanen and L. Dilillo, "Single-Event Effects in the Peripheral Circuitry of a Commercial Ferroelectric Random-Access Memory", RADECS Genève (accepted for oral presentation), 2017.
- **V. Gupta**, A. Bosser, G. Tsiligiannis, A. Mohammadzadeh, A. Javanainen, A. Virtanen, H. Puchner, F. Saigné, F. Wrobel and L. Dilillo, "Impact of Stacked-Layer Structure on SEE Rate of SRAMs", IEEE Nuclear and Space Radiation Effects Conference, Boston, US, 2015.
- Bosser, **V. Gupta**, R. Ferraro, A. Javanainen, H. Kettunen, H. Puchner, F. Saigné, A. Virtanen, F. Wrobel, L. Dilillo, « Investigation on MCU Clustering Methodologies for Cross-Section Estimation of SRAMs", IEEE Nuclear and Space Radiation Effects Conference, Boston, US, 2015.
- **V. Gupta**, A. Bosser, G. Tsiligiannis, A. Zadeh, A. Javanainen, A. Virtanen, H. Puchner, F. Saigné, F. Wrobel and L. Dilillo, "Heavy-ion radiation impact on a 4Mb FRAM under different test conditions", RADECS, Moscow, Russia, 2015.
- A. Bosser, **V. Gupta**, G. Tsiligiannis, R. Ferraro, C. Frost, A. Zadeh, A. Javanainen, H. Puchner, M. Rossi, F. Saigné, A. Virtanen, F. Wrobel and L. Dilillo, "A Methodology for the Analysis of Memory Response to Radiation through Bitmap Superposition and Slicing", RADECS, Moscow, Russia, 2015.
- L. Dilillo, A. Bosser, **V. Gupta**, F. Wrobel, F. Saigné, "Real-Time SRAM Based Particle Detector", IWASI, 2015.
- G. Tsiligiannis, L. Dilillo, **V. Gupta**, A. Bosio, P. Girard, A. Todri-Sanial, A. Virazel, H. Puchner, A. Bosser, A. Javanainen, A. Virtanen, F. Wrobel, L. Dusseau and F.Saigne,

"Efficient Dynamic Test Methods for COTS SRAMs Under Heavy-Ion Irradiation", IEEE Nuclear and Space Radiation Effects Conference, Paris, France, 2014.

- A.Bosser, L. Dilillo, **V. Gupta**, A. Javanainen, H. Kettunen, M. Rossi, G. Tsiligiannis and A. Virtanen, "Experimental Heavy-Ion SEU Cross- Sections Of Sram Memory Components", Physics Days 2014, Tampere, Finland, 11-12 March, 2014.
- **V. Gupta**, L. Dilillo, F. Wrobel, A. Zadeh, M. Bernard, G. Tsiligiannis, L. Dusseau, "Presentation of the MTCube CubeSat Project", Small Satellites Systems and Services (4S) Symposium, Majorca, Spain, 26-30 May 2014.

Annex A

MTCube initial mission feasibility study

Study orbit selection

At the initial stage of the project when the study was undertaken, initial estimations were made of the different subsystems regarding their mass, power and data budgets as well as a selection of a specific orbit for the analysis. The study will nonetheless have to be updated at a later stage of the project, when the orbit will be known, as well as when updated values with be available for the subsystems budgets.

Concerning the orbit selection for the feasibility study, the orbit in which will fly MTCube has not been defined. The first step is hence to find the most likely orbit for the initial assessment. However, the tool, based on the CelestLab library [CelestLab, 2016], built for this study, was made in a way to easily change the orbital parameters in order to re-run all simulations when the final orbit will be known. The most likely launch opportunities, for small satellites, are towards SSO (Sun Synchronous Orbits) circular orbits. The orbit altitude has to be chosen considering national and international space regulations such as [LOS, 2008] and [IPOL, 2008], which require a satellite to deorbit, or reach a graveyard orbit, within 25 years after the end of their mission. The lack of propulsion and deorbiting systems on MTCube requires choosing an altitude such that it will be allowed to naturally decay within 27 years (25 years + 2 years of nominal mission). A simulation tool (DAS) was used to ensure that at 650 km the satellite would re-enter within 27 years, the DAS tool being more conservative than the STELA tool (higher altitude orbits allowed). The remaining orbital parameters, as presented in Table 25, were chosen in order to have conservative estimations on power budgets.

Parameters	Value	Comments
Orbit altitude	650 km	Assumed altitude taking into account debris mitigation laws (< 25 years in orbit after the end of mission). Circular orbit considered.
Inclination	98°	In order to have Sun-synchronicity as SSO orbits are the most frequently used orbits.
MLTAN	12h	In order to have worse case eclipses in SSO.
A	0°	Guessed.

Table 25: Summary of the launch orbit parameters selected for the study.

Mission profile and operations

The mission is foreseen to run as much autonomously as possible, reducing the constraints on the operation team. This is possible because the tests performed on MTCube are repetitive. On the platform side, the main OBC will be in charge of monitoring the good behaviour of the satellite. No attitude and control is necessary to achieve the mission.

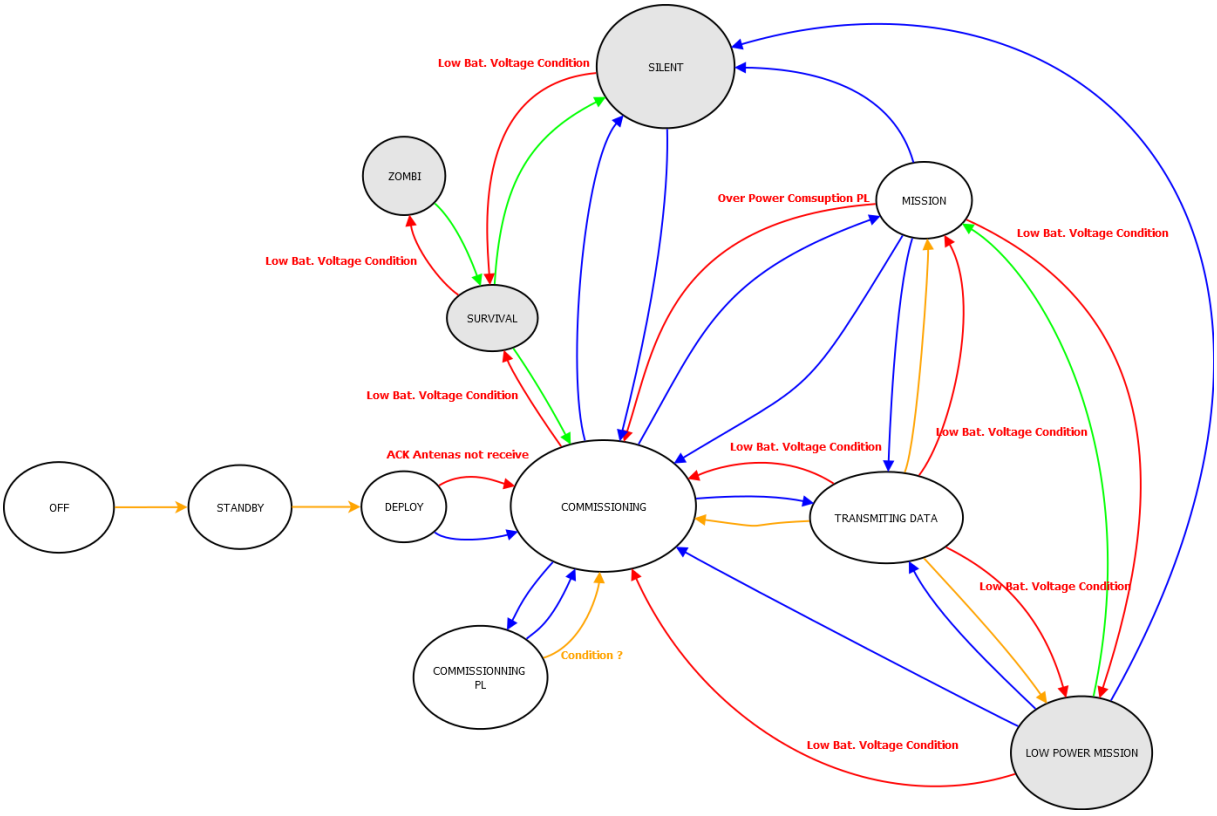
On the payload side, one FPGA will control the memories taking into account the fact that the Flash memories (that have much lower access time, with sensibly higher storage capacity) are placed on a separate bus and are controlled differently from the other memory types that will fly. All memories will be tested in static and dynamic modes: in static mode, the memory is irradiated with a known pattern stored in the memory prior irradiation; in dynamic mode, during irradiation the content of the memory is changed according to a specific sequence of read and write operations. More information regarding static and dynamic mode testing is given in chapter 2.

The deployment sequence will be fully automatic. After the antennae deployment, a command from ground shall be necessary to allow the satellite to enter into nominal mode. Hence, on the ground operation side, the work is foreseen to be minimum, collecting the data in order to process it, with the possibility of controlling key behaviours from ground such as forcing to reset the satellite, and put the satellite in silent mode (as per space radio regulations).

The CSU ground station will be the main ground station able to send commands and receive telemetry.

System modes

Work has also been undertaken regarding the definition of the system modes of MTCube. During the course of the feasibility study a simplified system mode diagram was used. After several iterations, the final modes diagram was defined and improved further after the feasibility study. Figure 95 provides an overview of the final satellite system modes. This work was done extensively with Prof. Jean-Roch Vaillé responsible for the OBDH subsystem and presently responsible for the 1U Robusta platform.



→	Transition by TC
→	Nominal
→	Automatic transitions due to a specific issue (battery voltage low, overcurrent...)
→	Automatic transitions when proper condition are met after an issue
MODE	Nominal mode
MODE	Degraded mode

Figure 95: MTCube System level mode diagram. Courtesy of J.R. Vaillé.

Besides the above mentioned modes, except during the Standby mode, the satellite will be broadcasting periodically 256 bytes of data providing increase opportunities to receive updated system parameters, to get a useful insight in the good functionality of the platform and payload. Amogst this broadcasting data, 144 bytes are dedicated to personalisable messages that can be uploaded from the CSU ground station to be shared with the radio-amateur community (the so-called "MTCube tweets").

Ground coverage

In order to calculate the ground coverage, the following table summarises the assumptions considered for the CSU main ground station (Table 26). The following values have been calculated based on a home-made program using CelestLab, a Scilab tool dedicated to mission anaylsis. Several parameters were retrieved in order to perform system level estimation for the mission that will be presented in the next subsections.

Parameter	Value
GS location	3.87° longitude 43.63° latitude 88 m altitude
GS min elevation	15°
GS min visibility time	2 min

Table 26: Ground Station assumptions for Ground coverage calculations.

The following Table 27 and Figure 96 show the results: with an average of around 3 passes per day, the average duration in-sight is expected to be around 6 min.

Ground Coverage		
Average time in sight	6.04	min
Max time in sight for a single pass	7.56	min
Min time in sight for a single pass	2.01	min
Average pass per day	3.14	#

Table 27: Ground Coverage statistics (for 2 years).

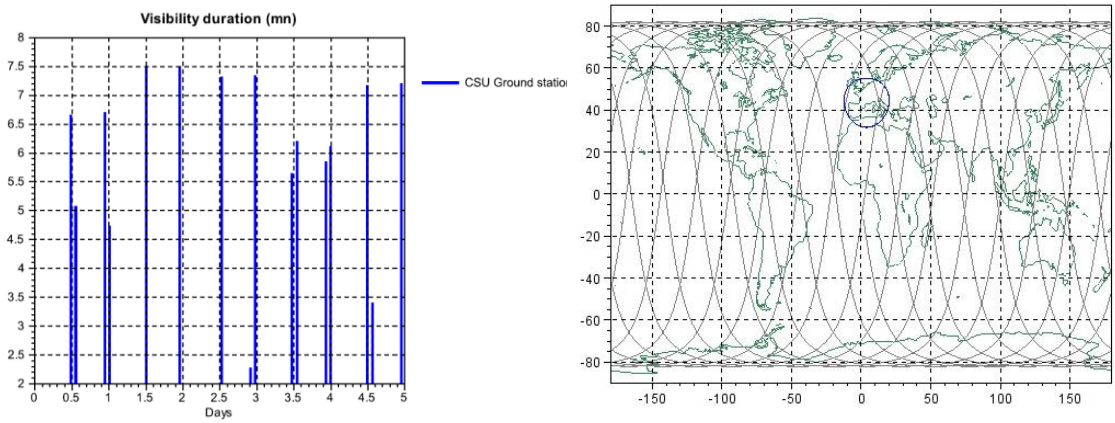


Figure 96: (left) GS visibility during the first 5 days in-orbit. (right) Plot of the ground tracks of MTCube for the first day in orbit and the simulated coverage area of the CSU main ground station.

MTCube power, mass and data budget assumptions

Based on information collected from Rob 1A and Rob 1B experiences, some assumptions were made, in order to evaluate the rough power, mass and data budgets.

The following Table 28 summarizes the assumptions made for each satellite subsystem. Each colour table represents a subsystem (besides the OBDH/OSL which represents the dosimeter that is part of the payload which will be installed on the OBDH card). For each subsystem, the power, housekeeping data and subsystem mass was estimated. The science data was included in the payload subsystem. The power and data rates represent average values that were estimated for different modes of each subsystem. All the subsystems are provided with +6V and each subsystem shall ensure regulation and convertion depending on their own power requirements. Each mode of the different subsystems was multiplied by a weighting factor in order to more accurately estimate the average power and data rate. For the following calculation, it was considered that the OBDH, EPS and payload were always in Mode 1 (ON) whereas the TTC was in transmission mode 20% of the time in one orbit and 80% of the time in reception mode. Similarly, the OSL was considered to be ON for only 20% of the time to make dose measurements per orbit. Although this estimation is guessed for the OSL, for the TTC, the 20% transmission time was calculated from the average number of communication possible links with the CSU ground station and average communication duration calculated for each pass duration.

						MODE AVERAGE				
		MODE 1	MODE 2	MODE 3	MODE 4	1	2	3	4	AVERAGE
OBDH										
	Mode name	ON	IDLE	OFF		1	0	0		1
POWER	Voltage (V)	6	6	6						
	Current (mA)	70	20	0						
	Power (W)	0,42	0,12	0						0,42
HK DATA	Data rate (bit/s)	5	5	5						5
MASS	Mass (g)									100
OBDH/OSL										
	Mode name	ON	IDLE	OFF		0,2	0,8	0		1
POWER	Voltage (V)	5	5	5						
	Current (mA)	60	30	0						
	Power (W)	0,3	0,15	0						0,18
HK DATA	Data rate (bit/s)	5	5	5						5
MASS	Mass (g)									50
TTC										
	Mode name	ON + Rx	ON+Tx+Rx	SILENT	OFF	0,8	0,2	0	0	1
POWER	Voltage (V)	5	5	5	5					
	Current (mA)	40	240	20	0					
	Power (W)	0,2	1,2	0,1	0					0,39446
HK DATA	Data rate (bit/s)	5	5	5	5					5
MASS	Mass (g)									200

						MODE AVERAGE (continued)				
		MODE 1	MODE 2	MODE 3	MODE 4	1	2	3	4	AVERAGE
EPS										
	Mode name	ON	IDLE	OFF	DEPLOY	1	0	0	0	1
POWER	Voltage (V)	6	6	6	6					
	Current (mA)	40	20	0	70					
	Power (W)	0,24	0,12	0	0,42					0,24
HK DATA	Data rate (bit/s)	5	5	5	5					5
MASS	Mass (g)									150
PAYLOAD										
	Mode name	ON	ECO	IDLE	OFF	1	0	0	0	1
POWER	Voltage (V)	6	6	6	6					
	Current (mA)	50	35	20	0					
	Power (W)	0,3	0,21	0,12	0					0,3
HK DATA	Data rate (bit/s)	5	5	5	5					5
SCIENCE DATA	Data rate (bit/s)	10	10	10	10					10
MASS	Mass (g)									200
STRUCTURE										
MASS	Mass (g)									300

Table 28: MTCube satellite subsystem power, mass and data estimation.

Those assumption lead to the following average consumption on-board MTCube (which includes a 20% system margin):

Parameter	Value	Unit
P_{MTCube} (incl. 20 %)	1.84	W
DR_{MTCube}(incl. 20 %)	42	bit/s
m_{MTCube}(incl. 20 %)	1.20	kg

Table 29: Mass, power and budget breakdown.

The mass estimation (Table 29) seems conservative as well as the assumptions made regarding the data rate of housekeeping and science data (on average). Although the power budget was estimated with care and seems reasonable with regards to CubeSat average power consumptions, it should be updated as soon as concrete (more realistic or measured) values are available.

Other subsystem parameters estimated for this study are presented in Table 30.

TTC		
Parameter	**Value**	**Unit**
Gain Sat	3,5	dBi
Trans. Output P	0,3	W
Modulation		-
Data rate down	1200	bit/s
Data rate up	1200	bit/s
Downlink f	435	MHz
Uplink f	145	MHz
System Temp.	933,25	K
Eb/No_req UP	19,5	TBD
Eb/No_req DOWN	19,5	TBD

EPS		
Parameter	**Value**	**Unit**
Battery Capacity	2,6	Ah
Voltage_ref	3,7	V
Battery Capacity	9,62	Wh
DoD	0,2	-

GROUND STATION		
Parameter	**Value**	**Unit**
Gain (downlink)	16	dBi
Gain (uplink)	13,2	dBi
System Temp.	1174,897555	K
Trans. Output P	120	W
Longitude	3,8669	°
Latitude	43,6331	°
Altitude	88	m
Antenna min elev	20	°
GS min visibility	120	s

Table 30: Other TTC, EPS and GS estimated parameters.

Mass budget

The preliminary mass is computed from Equation 7 and value provided in Table 31. A 20% margin is included in the final value to account for harness and other small uncounted items.

$$m_{tot} = m_{structure} + m_{OBDH} + m_{EPS} + m_{TTC} + m_{payload} + m_{OSL}$$

Equation 7: Mass estimation equation.

Parameter	Value (g)	Comments
$m_{structure}$	300	Structure, motherboard, battery casing, antennae, switches
m_{OBDH}	100	OSL not included
m_{EPS}	150	Solar array and battery not battery casing
m_{TTC}	200	Antennae not included
$m_{payload}$	200	
m_{OSL}	50	Dose monitor to be mounted on the OBC board
m_{tot}	1000	
m_{tot} incl. 20% margin	1200	Takes into account harness and other discrepancy with final measured values

Table 31: Mass budget breakdown.

The preliminary mass estimation shows a confidence margin with the maximum allowed mass of a 1U CubeSat fixed at 1330g including a 20% system margin.

Power budget

In order to assess the power budget, first the input power received on the solar array was calculated using the values provided in Table 32 and using Equation 8.

$$P_{array\_MTCube} = A_{array} * \Phi_{Sun} * Cos(\theta) * \eta_{cell} * \eta_{lifetime}$$

Equation 8: Solar energy input equation.

Parameter	Value	Comments
A_{array}	120,70 cm² (case 1) 170,70 cm² (case2)	One face towards Sun with 2 solar panels Two faces @ 45° with 2 solar panels.
Φ_{Sun}	1370 W/m²	Typical value @ Earth
$Cos(\theta)$	1	Angle considered in the Array calculation
η_{cell}	28%	GaAs 28% cell efficiency
$\eta_{lifetime}$	2.75%	GaAs degradation per year assumed for 2 years
P_{array_MTCube} EOL	2.19 W (case 1) 3.10W (case 2)	Best and worst case Solar array power @ EOL

Table 32: Parameters used for the Solar power input @ solar cells.

For information, the BOL power received from the solar array amounts to 2.30 W and 3.27 W showing that the estimated two years degradation amounts to around 100-170 mW approximately. It shall be noted that, assuming a randomly tumbling satellite, which is the case for MTCube, and taking into account the average cross-section area provided for the ballistic coefficient of 0.015 m², we have a received Solar array power of P_{array_MTCube} EOL = 3.29 W.

It was then checked, using the Equation 9, that the power consumed by the satellite in eclipse, for one orbit, could be provided by the energy stored on-board by the battery. The values used for this calculation are provided in Table 33.

For this calculation, it was assumed that the average power consumption in sunlight and eclipse of the subsystems is the same as the activity on-board is independent of illumination conditions.

$$Margin = E_{battery} - E_{eclipse} = E_{battery} - \left(P_{eclipse} * \tau_{eclipse} * \frac{1}{\eta_{charge} * DoD} \right) \geq 0$$

Equation 9: Required battery energy storage criteria.

Parameter	Value	Comments
$E_{battery}$	9.62 Whr	2600 mA @ 3.7V
$\tau_{eclipse}$	35.40 min	From simulation over the entire 2 year mission. Average eclipse time.
η_{charge}	90%	Estimated
DoD	20%	For Li-ion batteries
$P_{eclipse}$	1.84 W	Same power consumption in eclipse and sunlight
$E_{eclipse}$	6.00 Whr	Energy required in eclipse
Margin	3.58 Whr	Positive margin

Table 33: Parameters used for the battery sizing.

In conclusion from those calculations, it can be seen that the battery energy is, as expected, well sized (even over sized) for the consumption during sunlight.

Finally, it is considered that during the eclipse phase of the orbit, the necessary power (in average) that the satellite shall receive should be the power to be used during operations in sunlight added to the power that should be accumulated in the battery for the operations in eclipse. The equations used for this calculation are provided in Equation 10 and the estimated values are provided in Table 34. Note that this represents the worse case SSO orbit for eclipse.

$$\text{Margin} = P_{array\_MTCube} - P_{array} = P_{array\_MTCube} - P_{sun}\left(\frac{1}{\eta_{arr}} + \frac{1}{\eta_{charge}}\frac{\tau_{eclipse}}{\tau_{sun}}\right) \geq 0\ (?)$$

Equation 10: Criteria to assess if enough solar power input is received assuming the same average power consumption during sunlight and eclipse.

Parameter	Value	Comments
$\tau_{eclipse}$	35.40 min	From simulation over the entire 2 year mission. Average eclipse time.
τ_{sun}	$\tau - \tau_{eclipse}$	No comment
η_{charge}	60%	Conservative battery to subsystem loss
η_{arr}	80%	Loss between the solar array and the battery
P_{sun}	4.00 W	Power required for sunlight activity and battery charging
P_{array_MTCube} EOL	2.19 W (case 1) 3.10W (case 2)	Best and worst case Solar array power @ EOL
Margin	- 0.76 W (EOL) - 0.57 W (BOL)	End of Life, average surface exposed Beginning of Life, average surface exposed

Table 34: Parameters used for the required solar power during sunlight.

As can be seen with those calculations, the EOL margin is negative. This result demonstrates that taking into account orbital degradations, the mission may not be able to be performed during the entire orbit. Same comments at BOL. Nevertheless, several conservative values have been taken into account in these calculations (including system margin, worse case power transmission efficiency, and worse case orbit for eclipse in SSO).

Taking into account all the aspects, and considering that the margin is close to zero (taking into account the approximations made in the calculations), it may be possible to have a positive margin and it is recommended to update the power calculations with more realistic values as soon as they are made available.

Data budget

In this section we present results for the data evolution on-board the satellite. The parameters considered for the calculation are presented in Table 35.

Parameter	Value	Comments
$\eta_{overhead}$	10% + 30%	Addition OBDH data (clock time, etc…) and ECC overhead
$DR_{downlink}$	58.8 bps	As estimated for the subsystems including the overhead
$\tau_{GS\ no\ visibility}$	1.51 h (min) 7.53 h (av) 13.33 h (max)	Calculated
DR_{TTC}	1200 bps	From TTC
$Data_{onboard\_ini}$	0	Assumed 0 data stored onboard at the time of launch
η_{TTC}	100%	Data rate efficiency during download

Table 35: Parameters used for the on-board data evolution estimation. Assumptions: the data generated during the communication pass was neglected. The calculation accuracy is 1 min.

The conclusion is the following (Table 36 and Figure 97): considering a housekeeping data rate of 58.8 bps, in order to be able to download all data considering a reasonable on-board memory storage capacity, the true downlink data rate should be at least of 4.4 kbps (implying a maximum memory storage on-board of 8 Mb). Otherwise the data keeps accumulating on-board without being able to be sent to ground. In case the downlink data rate cannot exceed 1.2 kbps, the allowable housekeeping data rate cannot exceed 16 bps (maximum memory storage on-board is then around 2 Mb). Assuming a downlink data rate of 2.4 kbps, the housekeeping data rate cannot exceed 32 bps.

	HK data rate	TTC data rate	OBC memory
Case 1	< 16 bps	1.2 kbps	~2 Mb
Case 2	< 32 bps	2.4 kbps	~ 4 Mb
Case 3	58.8 bps	> 4.4 kbps	8 Mb
Case 4	58.8 bps	4.8 kbps	4 Mb

Table 36: Combination of parameters for various cases in order to ensure correct downloading capability of the on-board data during the 2 nominal mission years. In orange are the cells for which the calculation was done, in white are the resulting values.

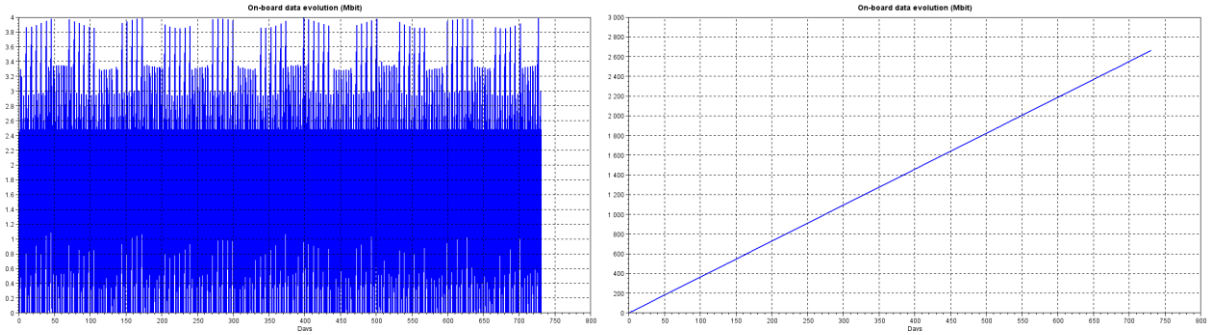


Figure 97: On-board data evolution plots results (left) HK DR=58.8bps, TTC DR=4.8kbps, (right) HK DR=58.8bps, TTC DR=1.2kbps.

Link budget

Finally, the link budget for the uplink and the downlink communication link was calculated using Equation 11 and values from Table 4.

$$\frac{E_b}{N_o}(\text{in dB}) = EIRP_{emitter} - L_s - L_a - L_{other} + FoM_{receiver} - k - R$$

$$\begin{cases} EIRP_{emitter} = P_{emitter} + G_{emitter} \\ FoM_{receiver} = G_{receiver} - T_{sys\ receiver} \\ L_s = \left(\frac{4\pi D}{\lambda}\right)^2 \end{cases}$$

Equation 11: Criteria to assess if the data budget is satisfactory.

Parameter	Downlink	Uplink	Comments
$P_{emitter}$	0.8 W	120 W	
$G_{emitter}$	3.5 dBi	13.2 dBi	Uplink and downlink GS antenna does not have the same Gain.
$G_{receiver}$	16 dBi	3.5 dBi	1 dB of conservative loss in the satellite cables for downlink and GS for uplink.
D	1205 km (min) 3035 km (av) 4573 km(max)		Calculated
f	435 MHz	144 MHz	Downlink UHF, Uplink VHF
L_s	159 dB	149 dB	Losses include transmitter, atmospheric, polarization and space losses
$L_a + L_{other}$	4.1 dB		Including polarization losses and…
k	-228.6 dBJ/K		No comment
R	1,2 kbps	1,2 kbps	Estimated based on Rob 1B
$\frac{E_b}{N_o}$ (cal)	23.74 dB	51.78 dB	
$\frac{E_b}{N_o}$ (req)	22 dB		Depends on the type of modulation and ECC implemented (this value has to be confirmed)
Margin	3.7 dB	29.8 dB	Positive margin for average distance.

Table 37: Parameters used for the link budget estimation.

As can be seen from the link budget calculation, the margin is above 3 dB for the uplink (as expected) but also the downlink for an average altitude. Even for the maximum altitude, the link budget has a positive margin showing that it is always possible to have a bi-directional communication link during the entire orbit defined for the study and considering all the assumptions made.

Feasibility results summary

In summary, in this section we have accessed the overall feasibility of the mission based on conservation assumptions on the orbital parameters, and the subsystem mass, generated data and power consumptions. This analysis showed that:

- mass budget is not a issue;
- the selected battery will be sufficient for the mission;
- the communication link is adequate within the margin for LEO orbits.

However, this study highlighted two potential issues requiring more in-depth study in order to guarantee a successful mission:

- power collected during sunlight is not enough to provide sufficient power in eclipse based on the conservative assumptions taken;
- the data rate shall be at least of 4.8 kbps in order to avoid filling-up the main OBC data buffer.

Hence, it was decided to switch from the previous Radiometrix analogic radio module to a newer radio module (CC1020) allowing an increase in the data rate (9.6 kbps) as well as being lower in mass and power consumption. Concerning the power budget for eclipse, more accurate data was required: later in the project, it was realised that the power consumption assumptions were very conservative and currently (at the time of writing) work is being performed to update the feasibility of the mission with measured values based on a built prototype.