Design of tunable radiofrequency blocks in FD-SOI technology for IoT applications

Jennifer Desèvedavy

THÈSE PRÉSENTÉE

POUR OBTENIR LE GRADE DE

DOCTEUR DE

L'UNIVERSITÉ DE BORDEAUX

ÉCOLE DOCTORALE DES SCIENCES PHYSIQUES ET DE L'INGENIEUR

SPÉCIALITÉ ÉLECTRONIQUE

Par Jennifer DESEVEDAVY

CONCEPTION DE CIRCUITS INTEGRES RADIOFREQUENCES RECONFIGURABLES EN TECHNOLOGIE FD-SOI POUR APPLICATIONS IOT

Sous la direction de : Thierry TARIS

(Co-directeur : Dominique MORCHE)

Soutenue le 8 octobre 2018,

Membres du jury :

M. David Bol	Professeur	Université de Louvain	Rapporteur
M. Sylvain Bourdel	Professeur	Université Grenoble Alpes	Président- Rapporteur
M. Olivier Tesson	HDR	NXP Caen	Examinateur
M. Thierry Taris	Professeur	IMS Bordeaux	Directeur de thèse
M. Dominique Morche	HDR	CEA Leti Grenoble	Co-directeur de thèse
M. Frédéric Hameau	Ingénieur	CEA Leti Grenoble	Encadrant
M. Patrick Audebert	Ingénieur	CEA Leti Grenoble	Co-encadrant

ABSTRACT

DESIGN OF TUNABLE RADIOFREQUENCY BLOCKS IN FD-SOI TECHNOLOGY FOR IOT APPLICATIONS

Communicating objects are inviting themselves into daily life leading to digitization of the physical world. This explosion of multimedia wireless applications for consumer electronics makes the power consumption a key metric in the design of multi-mode wireless portable devices. Conventional transceivers have fixed performances and are designed to meet high performances in all wireless link conditions. However, most of the time, the channel of communication is not at worst case and these transceivers are therefore over specified. Being aware of the channel link conditions would allow such devices to adapt themselves and to reduce significantly their power consumption. Therefore, the challenge is to propose a QoS (Quality of Service) in terms of communication range, response time as instance, equivalent to industrial modules with a reduced overall power consumption.

To address this purpose, this thesis proposes a design strategy for the implementation of adaptive radio-frequency receiver (Rx) modules. Hence the Rx front end achieves the correct QoS for various scenarii of communications with a minimum of power consumption.

As a proof of concept, the adaptive approach is demonstrated with the design of a tunable LNA (Low Noise Amplifier). As the first element of the receiver chain, the LNA limits the receiver in terms of sensitivity and is therefore a good candidate to perform reconfiguration. The body biasing of the FD-SOI (Fully Depleted Silicon-On-Insulator) technology is first exploited to reduce the power consumption of a circuit and then as an opportunity to perform circuit tunability.

KEYWORDS : Low Noise Amplifier – Integrated Circuit - FD-SOI – Radiofrequency - Reconfigurable

RÉSUMÉ

CONCEPTION DE CIRCUITS INTEGRES RADIOFREQUENCES RECONFIGURABLES EN TECHNOLOGIE FD-SOI POUR APPLICATIONS IOT

La pénétration importante d'objets communicants dans notre vie quotidienne révèle des défis important quant à leur développement. Notamment l'explosion d'applications multimédia sans fil pour l'électronique grand public fait de la consommation électrique une métrique clef dans la conception des dispositifs portables multimodes sans fil. Les émetteurs-récepteurs conventionnels proposent des performances fixes et sont conçus pour respecter ces hautes performances dans toutes les conditions de communication sans fil. Cependant, la plupart du temps, le canal n'est pas dans le pire cas de communication et ces émetteurs-récepteurs sont donc surdimensionnés. En connaissant l'état du canal en temps réel, de tels dispositifs pourraient s'adapter aux besoins et réduire significativement leur consommation électrique. Le défi consiste à respecter la Qualité de Service , ou Quality of Service (QoS) en anglais, imposée par les différents standards de communication. Afin de rester compétitifs, les émetteurs-récepteurs adaptatifs doivent donc proposer une même QoS que ceux déjà disponibles sur le marché. Ainsi, ni la portée de communication ni le temps de réponse ne peuvent être dégradés.

Basé sur ces exigences, cette thèse propose une technique d'adaptation pour la conception d'un récepteur reconfigurable qui fonctionne à la limite des performances nécessaires pour recevoir le signal utile. Ainsi, le récepteur proposé est toujours au minimum de consommation électrique tout en garantissant la bonne QoS. Ceci permet alors de multiplier la durée de vie de sa batterie par un facteur 5.

Cette adaptabilité est démontrée ensuite côté circuit par la conception d'un LNA (Amplificateur Faible Bruit) dont les performances sont reconfigurables. En effet, en tant que premier élément de la chaîne de réception, le LNA limite le récepteur en termes de sensibilité. Ces travaux exploitent la technologie FD-SOI (Fully Depleted Silicon-On-Insulator) pour d'une part, réduire la consommation du LNA et d'autre part, ajouter de la reconfigurabilité à ce même circuit.

MOTS-CLES : Amplificateur Faible Bruit - Circuits intégrés - FD-SOI – Radiofréquence - Reconfigurable

ACKNOWLEDGMENT

This work would not have been possible without the outstanding assistance and support of many other individuals.

First, I would like to thank my research advisor, Pr. Thierry Taris for his support and guidance throughout these three years, always available despite the distance. His vision of the research field has been both inspiring and challenging.

I would like to express my heartfelt gratitude to my thesis supervisor, Mr. Frédéric Hameau. He was always there every step of the way, guiding me in the right direction as I grew as a researcher and also as a human being. I sincerely thank him for that.

I take this opportunity to also thank my co-advisor, Dr. Dominique Morche for his ability to think out of the box which inspires me a lot.

I would also like to thank my co-supervisor, Mr. Patrick Audebert for his guidance and encouragement.

On a larger scale, the LAIR team has provided an interdisciplinary environment which encourages all sorts of productive research, so thank you all for the precious shared moments. I am thankful for the professional and personal support I received from many of my colleagues – Anthony, Baudouin, Clément, Ayssar, Alex G., Alex S., David, J-B, Gilles, Pierre, Carolynn, Didier, Emeric, Jérôme, Guillaume and many others – over these three years. I was lucky to cross paths with many interesting people who have enriched my life through these years at the LAIR lab.

My special thanks to Mr. Pierre Vincent and Mr. Eric Mercier for giving me the opportunity to study this interesting research topic within the DACLE/LAIR.

I sincerely appreciate what I learnt from my PhD student colleagues – Marguerite, Tu, Florian and Saad – to whom I wish much strength to complete their PhD degree.

I also thank the thesis committee members – Pr. David Bol from UC Louvain, Pr. Sylvain Bourdel from Université Grenoble Alpes and Mr. Olivier Tesson from NXP Caen – for evaluating my research and accepting to participate as the Jury.

I would like to thank Magali De Matos and Gabrielle Guitton from IMS Bordeaux for their availability and their help during the measurements of the ULP LNA.

I am extremely grateful to my mother Mrs. Marie-Jo Zaini and my father Mr. Serge Zaini for their unconditional love and their unshakable trust which I have felt not only during my thesis but all through my life. I have always found strength and encouragement in their love and support.

Many thanks to my sisters, especially Miss. Emmanuelle Zaini and Miss. Nadège Helly for their support (especially for the wedding organization!) and the continuous WhatsApp conversations that helped a lot during hard working days. Dadou, who provided real time pictures of my nephews Lucas and Ethan making me smile every day. Manu, our never-ending 4 in 1 conversations inspired me a lot. I also want to thank my entire extended family and my closest friends for their support and love.

I would especially like to present my deepest gratitude to my parents-in-law, Mrs. Pascale Desèvedavy and Mr. Hervé Desèvedavy for their continuous encouragement and precious advice during the past three years. Thank you for making me feel like your daughter, I am so lucky to be part of your family.

Last but definitely not least, I want to thank my husband Yann for his endless support, patience and care. He has always been there for me and I am very lucky to have him by my side. I am so thankful for his presence in my life and I dedicate this work to him. Merci mon amour.

Jennifer Desèvedavy
Grenoble, France

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

ADC	Analog-to-Digital Convertor
BBGEN	Back Bias Generator
BER	Bit Error Rate
BG	Back Gate
CG	Common Gate
CGA	Voltage Gain Amplifier
CS	Common Source
DPLC	Dynamic Packet Length Control
FD-SOI	Fully Depleted Silicon-On-Insulator
FoM	Figure of Merit
Gv	Voltage Gain
IC	Integrated Circuit
IIP3	Input Referred Third Order Intercept Point
IM	Intermodulation
IoT	Internet of Things
LNA	Low Noise Amplifier
LQE	Link Quality Estimator
NF	Noise Figure
P1dB	1-dB Compression Point
PDF	Probability Density Function
PLL	Phase Locked Loop
PVT	Process, Voltages and Temperature
QoS	Quality of Service
RSSI	Received Strength Signal Indicator
SNDR	Signal to Noise Distortion Ratio
SNR	Signal to Noise Ratio
SoA	State of the Art
SPI	Serial Peripheral Interface
ULP	Ultra-Low Power
ULV	Ultra-Low Voltage
UTBB	Ultra-Thin Body and Buried oxide
WSN	Wireless Sensor Network

CHAPTER 1

INTRODUCTION

Communicating objects are inviting themselves into daily life and the physical world becomes more and more digitized. This emerging technological age, called the Internet of Things (IoT), unveils new requirements in terms of cost, surface area and battery lifetime. The challenge is to find innovative solutions to add intelligence to communicating systems.

In this Chapter, the context of Wireless Sensor Network (WSN) for IoT applications is first presented. Then, the challenges in the design of wireless transceivers for WSN due to this IoT paradigm are commented. The interest of the Ultra-Thin Body and Buried-oxide Fully Depleted Silicon-On-Insulator (UTBB FD-SOI) technology to improve performances and flexibility of communicating nodes is discussed. Finally, the thesis organization and purpose are highlighted.

1.1 INTERNET OF THINGS AND WIRELESS SENSOR NETWORKS

Based on the Ericsson annual report of 2010 [1], the world went through a turning point for mobile communications which gave rise to a massive development of connections (more than 50 billion of connections are expected this year) as depicted in Figure 1.1. Objects are now connected to the Internet services, able to recognize their environment, to organize themselves into networks or interact with humans. IoT is totally shifting the way people interact with their surroundings.

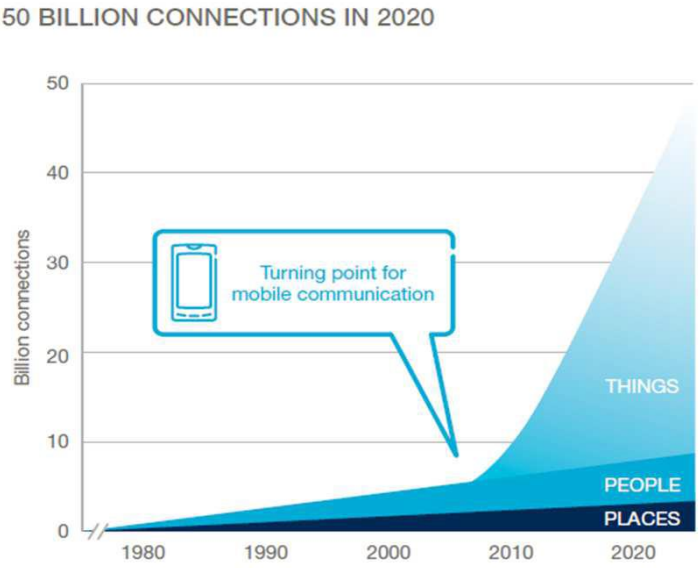


Figure 1.1 50 billion of connections in 2020 [1].

What makes IoT devices and components "smart" are the numerous sensors and microprocessors featuring the devices which enable advanced functionalities. WSNs are several types of sensors able to monitor information, to sense the environment, to collect important data and send them to a management entity. They are part of today's IoT paradigm.

As illustrated in Figure 1.2, there are various domains of applications of WSNs. Traditional homes or workplaces can be transformed to smart homes or smart workplaces. Intelligence can be broadened to a whole city becoming a smart city. In the health domain the IoT is also providing solutions.

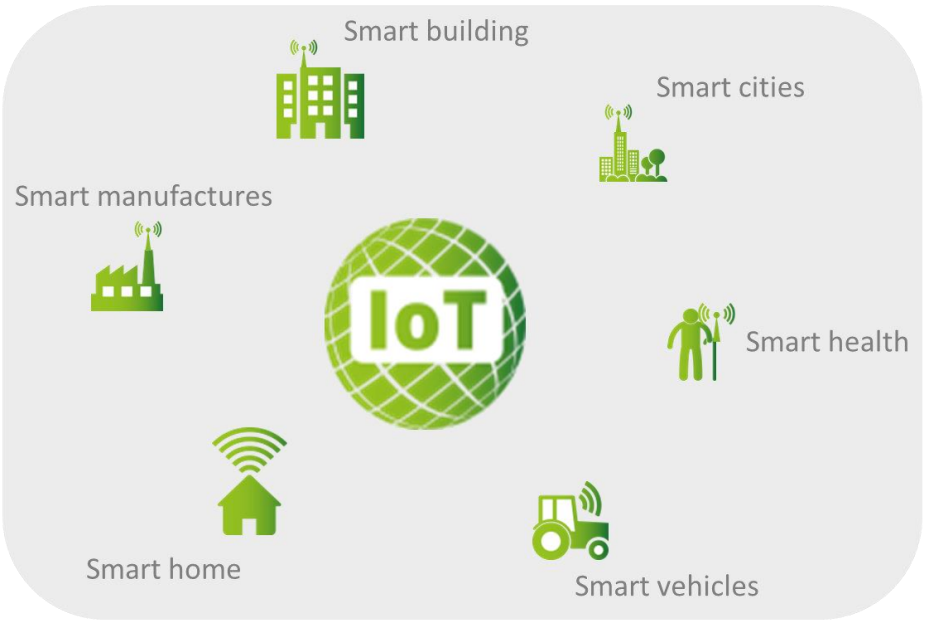


Figure 1.2 Application domains of the Internet of Things (IoT).

This massive development of sensors for IoT applications means wireless communicating nodes with small form factor for an easy distribution in the environment, reduced power consumption for an extended lifetime and limited impact on the environment as detailed in [2].

This vision of the IoT induces major challenges in the design of autonomous WSNs. The limited battery storage is the blocking point of fully energy autonomy. In fact, the evolution of battery technologies is not able to follow the trend of the drastic increase of energy efficiency.

These emergent technologies unveil new constraints for Integrated Circuit (IC) design.

1.2 CHALLENGES IN TRANSCEIVER DESIGNS

The power consumption of a node is shared between the radio communication part, the MicroController Unit (MCU) and sensors. For IoT applications, the radio part is one of the most power hungry part as illustrated in Figure 1.3 [3]. Therefore, it is of importance to further reduce the power consumption of RadioFrequency (RF) transceivers.

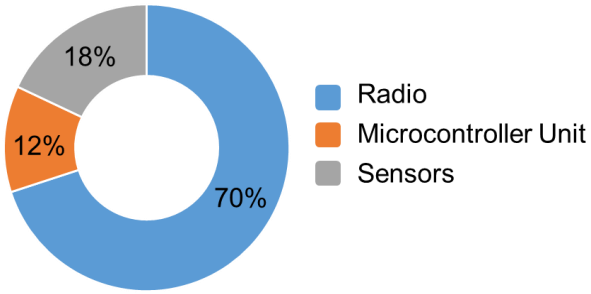


Figure 1.3 Repartition of the power consumption in a wireless sensor node [3].

Wireless communicating objects call for a high level of specifications to guarantee the Quality of Service (QoS) of specific standards along with a small power consumption.

Hence, challenges in Radio Frequency Integrated Circuit (RFIC) dedicated to IoT applications are as follows:

- SMALL FORM FACTOR: reducing the size of communicating nodes by decreasing the footprint of the circuits for total transparency in the environment and unobtrusive network to propose a "green connected planet";

- LOW POWER: in a large network with many communicating nodes, battery replacement can be difficult, expensive or even impossible. Nodes have to be able to operate over a long period of time;

- LOW COST: the deployment of billions of connected objects is only possible if the cost of a node is very low;

- QUALITY: fulfilling the performance requirements in order to respect the targeted QoS set by the standards is essential.

Therefore, further deployment of communicating objects demands a smart use of the available power budget. Consequently, these challenges become important targets in IoT RFIC designs to yield long lifetime autonomous WSNs which cope with these new constraints. The next Subsection demonstrates how advanced technologies can contribute to address the aforementioned challenges.

1.3 FD-SOI TECHNOLOGY: GOOD CANDIDATE FOR IOT APPLICATIONS

The technology scaling following the Moore's law is getting harder to keep on. The evolution towards the down-scaling of the sizes of transistors gates has reached its limits with the conventional bulk Complementary Metal Oxide Semi-conductor (CMOS) technology. In deeply scaled CMOS transistors, due to their narrow channels, small-geometry effects start to affect their behavior. The Short Channel Effects (SCE), as the Drain-Induced Barrier Lowering (DIBL) and the velocity saturation tend to increase the standby leakage currents and reduce the current efficiency of a transistor. As a consequence, the gate cannot completely shut down the transistor and the subthreshold leakage currents appear between the drain and the source [4].

A promising technology for overcoming this limitation is the FD-SOI technology. In fact, the critical and massive deployment of the IoT requires efficient energy flexibility. Therefore, adaptive solutions able to operate at different voltage supplies, even at very low voltages around threshold levels, are needed. The FD-SOI technology provides this flexibility and offers good performances from normal voltage operation mode to low voltage levels. Moreover, this technology is promising for designing very low leakage systems when the node will remain in idle state. The application of a back biasing voltage in FD-SOI enables a compromise between very low leakage and high speed and can change the operating conditions depending on the state of the device as demonstrated in [5].

The FD-SOI technology is therefore a good candidate to perform flexibility and to fulfil the needs of the wide deployment of the IoT applications:

- SMALL FORM FACTOR: the use of advanced node FD-SOI 28 nm technology is part of the surface reduction. The design of inductorless structures is also a good solution to decrease the surface area of the chip;

- LOW POWER: this technology offers possibility to decrease the power supply and to reduce the power consumption while maintaining good performances;

- LOW COST: the FD-SOI technology is a solution for integration of digital, analog mixed and Radio Frquency (RF) signals in a single System on Chip (SoC)

- QUALITY: the FD-SOI technology is able to provide a wide range of tunability between high speed and low leakage [5].

This work proposes to take advantage of this advanced node in order to, first, improve the performances of the analog part which becomes predominant as long as the technology scales and then, add tunability in circuits to work at minimum power levels.

1.4 THESIS PURPOSE AND ORGANIZATION

The purpose of this research is to reduce the energy dedicated to communication in wireless sensor nodes by bringing flexibility throughout technological and architectural solutions. First, a system level approach is proposed to increase the battery lifetime of WSNs is proposed. The FD-SOI technology is then investigfated to address the concept of tunability in Radio modules introduced in the system-level approach. The final target is the design of a low area and Ultra Low Power (ULP) Low Noise Amplifier (LNA) which can optimally adapt its performances and power consumption with the real-time needs of the receiver.

To address this goal, the thesis is organized as follow:

- Chapter 2 proposes a new approach to increase the battery lifetime of a radio receiver based on a discrete reconfiguration of the set of performances. More specifically, it defines with analytic demonstrations the thresholds of reconfiguration enabling a significant power saving.

- Chapter 3 concentrates on an optimization of the power consumption of the first block of a receiver: the LNA. It details the optimization of the design of an inductorless LNA able to address the low power mode of the tunable receiver. An investigation on the use of the body biasing of the FD-SOI technology to decrease the power supply and thus, the power consumption of the LNA without loss of performance is also proposed.

- Chapter 4 presents the design of a reconfigurable LNA which suits the three levels of performance defined in Chapter 2. It describes a new method to change the effective width of amplifying transistors in order to achieve at a maximum Figure of Merit (FoM) for each mode of operation.

- Chapter 5 outlines the conclusion of this thesis and discusses the future investigations.

CHAPTER 2

TUNABLE RECEIVER: SYSTEM-LEVEL ANALYSIS

The explosion of multimedia wireless applications for consumer electronics makes the power consumption a key metric in the design of multi-mode wireless portable devices. Conventional transceivers have fixed performances and are designed to meet high performance in all wireless link conditions. However, most of the time, the channel is not at worst case and these transceivers are therefore over specified. Being aware of the channel link conditions would allow such devices to adapt themselves and to significantly reduce their power consumption. However, the challenge is that the Quality of Service (QoS) of adaptive transceivers should be equivalent to that offered by conventional ones, to stay competitive. As an example, neither the communication range nor the data rate can be degraded. Therefore, the sensitivity of the proposed receiver has to be equal to the sensitivity of today's products.

This Chapter explores the benefits of an adaptive receiver featuring different modes of operation to save power. From a general perspective the proposed investigations address one of the tough challenges posed by the massive deployment of Internet of Things (IoT) communicating nodes:

How can battery lifetime of communicating nodes be significantly extended?

To answer this question, this Chapter proposes an adaptation technique for the design of a tunable receiver which can always operate at the edge of needed performances and thus, at minimum power consumption while keeping the needed QoS.

A State of the Art (SoA) of adaptive systems is first presented in order to evaluate the existing solutions dedicated to reduce the power consumption. Then, the general approach of the proposed channel aware receiver is described. A methodology to define the thresholds of reconfiguration for maximum energy efficiency in a receiver is detailed. Finally, a link budget analysis of the entire receiver down to the Low Noise Amplifier (LNA) is proposed in order to validate the feasibility of the proposed system analysis.

2.1 STATE OF THE ART OF ADAPTIVE RECEIVER TECHNIQUES

The energy cost of a transmission can be, at first order, assimilated to the integration of the instantaneous power consumption over the transmission duration. The possibilities to reduce this energy cost are twofold: reducing the instantaneous power consumption of the transceiver, or decreasing the transmission duration.

The performance degradation of energy reduction techniques is evaluated through the wireless link budget of Equation (2.1) [7].

$$SNR_{min} = P_{TX} - CL - (10.\log(BW) - 174 + NF) \quad (2.1)$$

With SNR_{min} in dB the minimum Signal to Noise Ratio required for correct quality of transmission, P_{TX} the transmission power in dBm, CL the Channel Loss in dB, BW the receiver bandwidth, -174 dBm the noise floor and NF the Noise Figure of the receiver.

Figure 2.1 illustrates a transmission between the transmitter and the receiver with the basic metrics of the wireless link equation.

Figure 2.1 Wireless link communication.

Therefore, reducing the energy cost of a transmission can be achieved by decreasing P_{TX} in the transmission module, and/or reducing the NF or BW of the receiver part, or varying the required SNR_{min}. Many works have been proposed to decrease the transmitted power such as adaptive Power Amplifier (PA) on the transmitter part.

This work concentrates on the receiver part. Different power reduction and adaptation strategies have already been proposed in the State of the Art as detailed in next Subsections.

2.1.1 WAKE-UP RECEIVERS

A first well-known solution is to resort to wake-up radio. This technique consists of adding a supplemental receiver in parallel to the main receiver. Its goal is to listen to the channel and to switch ON the main receiver only when a communication is requested. The basic concept of wake up radio is depicted in Figure 2.2.

In [8], a wake up radio design is proposed consuming only 52 µW. It shows that a wake up receiver is a good solution to drastically reduce the power consumption of the receiver.

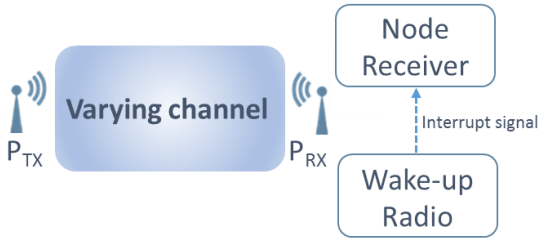


Figure 2.2 Basic concept of Wake-Up radio.

However, to decrease this consumption, the sensitivity is degraded to -72 dBm with 100 kbps of data rate. It is therefore impossible to detect a distant communicating node. This approach is very interesting to decrease the power consumption of short range communication but does not fulfill the high QoS required by the standards.

2.1.2 MAC OR NETWORK LEVEL ADAPTABILITY

New solutions to save power on the RadioFrequency (RF) communication have also been developed at MAC or network level such as energy efficient protocols where the transmission data rate can vary when the sensitivity of the node is reduced [9].

Adjusting the data rate to the receiver sensitivity technique has also been used in the industry. For instance, the Atmel AT86RF231 module proposes a variation of its data rate from 250 kb/s to 2 Mb/s. Consequently, the sensitivity is decreased from -101 dBm to -88 dBm respectively.

The work proposed in [10] adapts the spreading code lengths and enables an improvement of the battery lifetime of 36 %. A low power adaptive digital baseband for standard IEEE 802.15.4 through a variation of word length and sampling frequency is presented in [11]. Another technique to increase the battery lifetime is to modulate the transmitted packet length. In [12], a Dynamic Packet Length Control (DPLC) has been proposed for Wireless Sensor Network (WSN) applications. The authors show that the ratio between received useful bytes and the overall transmitted bytes can be used as a Link Quality Estimator (LQE). The results show a maximum power reduction of 41.8%

compared to a fixed frame length implementation. Nevertheless, the modulation on frame technique is more efficient on applications where large volumes of data have to be transmitted.

These approaches address mainly digital baseband. This is indeed particularly interesting but to be fully energy efficient, tunability has to be added to the analog-RF part of the receiver which consumes a significant portion of the power.

2.1.3 ANALOG-RF ADAPTABILITY

Very little research has been undertaken in this area. As an example, [13] investigates the interest of a power-reconfigurable Analog-to-Digital Convertor (ADC). It shows a power reduction by a factor of 25 using this reconfigurable ADC. In [14], the author shows that a fully reconfigurable Low Noise Amplifier (LNA) considerably decreases the power consumption of the receiver through behavioral modeling of building blocks for two standards: Bluetooth LE and IEEE 802.15.4. These works confirm the interest of the approach but unfortunately they are limited to system simulation which does not confirm the feasibility of the concept. Both a system simulation and a Proof of Concept (PoC) are needed to validate the approach.

In [15], the benefits of a receiver with dynamic adaptation to channel conditions is demonstrated. The methodology enables a self-learning of its power consumption and performance configurations based on real-time estimation of the channel conditions. With their artificial neural network learning technique, the authors demonstrate that this continuous tuning reduces the power consumption. Unfortunately, the factor of reduction is limited to 2. Moreover, the learning algorithm enabling the power saving calls for a complex implementation.

This limited scalability of power consumption is due to the big challenge in designing adaptive analog or radiofrequency building blocks. Indeed, in power efficient analog circuits, the current flowing through the transistor can only be modified in a limited range which severely impacts the performances. As a consequence, the power consumption of adaptive analog blocks is difficult to scale. Furthermore, the Figures of Merit (FoM) of these blocks degrade when tunability techniques are applied.

Atmel has shown an interest in adaptive receivers with the release of a transceiver: AT86RF233. In standard mode, it offers a -91 dBm sensitivity while consuming 10.5 mA under 1.8V. The power consumption can decrease to 8.5 mA while degrading the sensitivity to -49 dBm. This means that 42 dB degradation of the sensitivity is required to save only 20% of the current consumption.

Therefore, the proposed approach concentrates on the development of an optimal, energy-efficient reconfiguration technique which enables equivalent performances of industrial modules but significantly increases battery lifetime. A scaling factor of five to ten is needed to justify the interest of tunability.

2.1.4 PROPOSED APPROACH

The basic principle is depicted in Figure 2.3. The transmitted signal P_{TX} reaches a receiver P_{RX}, with various channel path length, attenuation and delay. At the receiver side, the environment conditions of the channel is estimated by the LQE. Different LQE can be exploited (Received Strength Signal Indicator (RSSI) or Bit Error Rate (BER) for instance). After processing, the required performances are selected and the tuning information is sent back to the analog and RF blocks which are able to scale their performance and power.

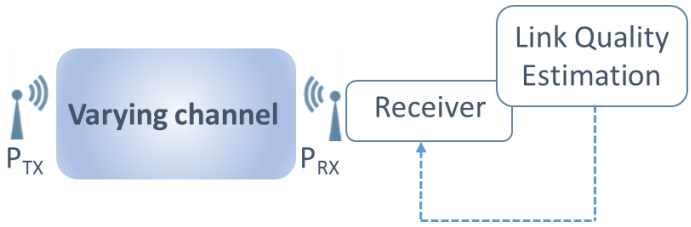


Figure 2.3 Adaptive transceiver illustration.

Through this approach, it is proposed to circumvent the adaptability challenge of the RF blocks by several parallel operating modes with various performances as shown in Figure 2.4. The high performance mode guarantees the QoS and the medium and low power modes permit to save power consumption in relaxed channel conditions. With several operating modes in parallel, the tunability becomes discrete and offers fast and simplified adaptive algorithm.

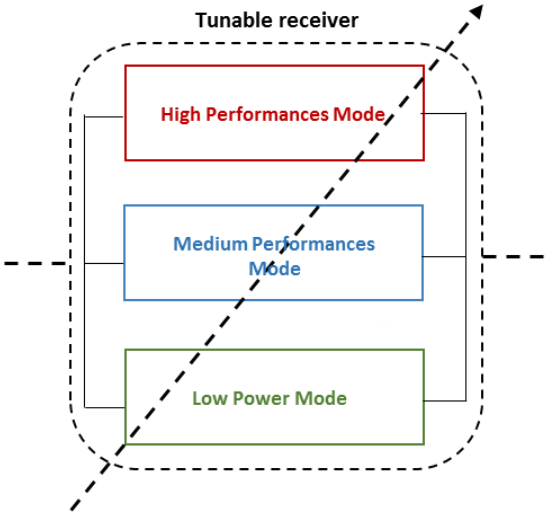


Figure 2.4 Illustration of the proposed tunable receiver.

The LQE of the receiver can be fast enough to enable an intra frame reconfiguration implementation. This LQE and the selection of the operating mode of the receiver can therefore be done during the synchronization preamble as illustrated in Figure 2.5.

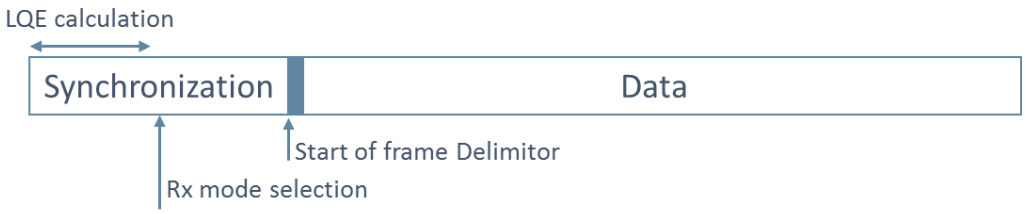


Figure 2.5 Selection of the receiver operating mode during the synchronization preamble.

Each synchronization frame starts with the highest performance level receiver. However, the operating modes can be changed very quickly after LQE. This technique, schematized in Figure 2.6, enables no frame loss.

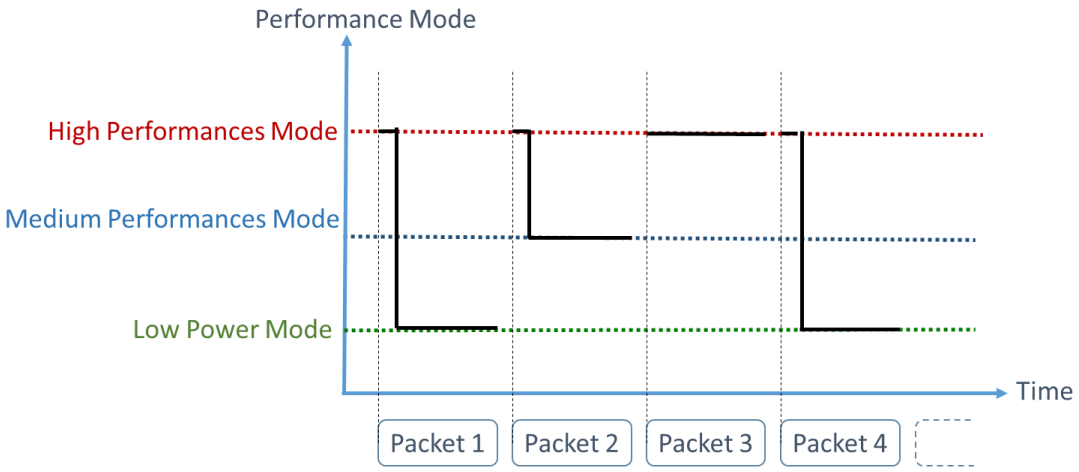


Figure 2.6 Intra-frame 3-levels tunable receiver.

The approach has been settled but it is now mandatory to identify the number of operating modes to achieve significant power saving. For each mode, the level of performance must be defined.

The next Section proposes a methodology to address this purpose. First, a distribution model of the channel attenuation is derived. Secondly, receiver consumption is evaluated as a function of the targeted sensitivity. Then, the optimal number of reconfiguration modes is calculated. Finally, the best level-thresholds are estimated accordingly.

2.2 PROPOSED CHANNEL AWARE RECEIVER

2.2.1 CONTEXT OF APPLICATION

In the context of development of smart applications dedicated to smart homes or smart industries, this probabilistic study considers, as a starting point, the following conditions of computation:

- IEEE802.15.4 ZigBee® standard addressed (ISM Worldwide band at 2.4 GHz);
- Indoor propagation channels without the presence of adjacent blocker;
- Peer-to-peer network arrangements (simplified connectivity compared to star networks);
- Random and uniform nodes locations distribution in the area (λ=0.001 in node/mm^2);
- Mean distance *d* between two nodes of 15 meters;
- Nodes communicate with their nearest neighbor(s) (n=1);
- Signal suffering from average path-loss attenuation only (Z=0);
- P_{TX}= 4 dBm is considered as the default ouput power transmitted by the node.

Table 2.1 details the basic standard specifications used for the following system analysis. The BER is the main specification for the required QoS. The Signal to Noise Ratio (SNR) is the ratio between the signal of interest power and the noise in the bandwidth of the signal. The relation between BER and SNR depends, among other things, on the required communication distance and the data rate, the modulation type and demodulation algorithms. The receiver sensitivity is the lowest power receivable at the input of the receiver for which it is capable to demodulate the information with the correct BER.

Modulation	**Frequency**	**Channel Bandwidth**	**Data rate**	**Number of nodes**	**Signal to Noise Ratio (SNR_{min})**	**Bit Error Rate (BER)**	**Packet Error Rate (PER)**
OQPSK	2.4 GHz (ISM Band)	5 MHz	250 kbits/s	2^{64}	10 dB	10^{-6}	1%

Table 2.1 IEEE802.15.4 Standard specifications.

For an optimized position of the discrete operating points, an estimation of the probability of the received signal power and the usage time in each mode is determined. Therefore, the model of the RF propagation conditions through the channel taking into account the context of application is demonstrated in next Subsection.

2.2.2 PROBABILITY DISTRIBUTION FUNCTION OF THE RECEIVED POWER SIGNAL

The strategy adopted in this thesis is to represent the deployment of a network as a probabilistic analysis based on a spatial random distribution of the different nodes. Establishing a model for RF propagation conditions is part of the challenge when designing an adaptive channel dependent optimized receiver. The transmitted signal reaches the receiver from different directions, with various path lengths, attenuation and delays. The summed contribution at the receiver $p_{RX}(d)$ results therefore in an attenuated signal [16] as shown in Equation (2.2) .

$$p_{RX}(d) = P_{TX} - 10.\log(\alpha) - 10.\beta.\log(d) - Z \qquad (2.2)$$

Where α is the linear attenuation with the reference of d_0=1m, β is the coefficient for path-loss, d the distance of transmission and Z a random coefficient which represents the shadowing effect.

Nodes communicate with their n^{th} nearest neighbor(s). They are immobile and randomly distributed in the area, their density in nodes/mm² is noted λ. Based on homogeneous Poisson process [17], the Probability Distribition Function (PDF) of d, the random distance between a node and its n^{th} nearest neighbor(s), is defined in Equation (2.3).

$$PDF_d(d) = \frac{2(\pi\lambda)^n.d^{2n-1}.e^{-\lambda\pi d^2}}{(n-1)!} \qquad (2.3)$$

The integrals of $PDF_d(d)$ defined in Equation (2.3) and $PDF_{p_{RX}}(p_{RX})$ in Equation (2.2) are equals to 1 over their integration domain [0;∞[and]-∞;∞[respectively which gives the equivalence of Equation (2.4).

$$\int_0^\infty PDF_d(d)\,dd = \int_{-\infty}^{\infty} PDF_{P_{RX}}(p_{RX})\,dp_{RX} = 1 \qquad (2.4)$$

From Equation (2.2), d and its derivate give the Equation (2.5) and Equation (2.6) respectively.

$$d = 10^{\frac{P_{TX} - 10.\log(\alpha) - p_{RX}}{10.\beta}} \tag{2.5}$$

$$dd = \frac{-ln10}{10.\beta} 10^{\frac{P_{TX} - 10.\log(\alpha) - p_{RX}}{10.\beta}} dp_{RX} \tag{2.6}$$

The proposed approach can be re-simulated and easily adapted to other propagation conditions, different network types or additional RF propagation phenomenon such as shadowing or fading effects for instance. In fact, the shadowing effect can be added to the analysis through Z in the Equation (2.2) as a random variable. On the other side, the fading effect can be modeled with Rician or Rayleigh distributions.

Considering the chosen conditions of computation, the $PDF_{P_{RX}}(p_{RX})$ can be expressed as in Equation (2.7).

$$PDF_{P_{RX}}(p_{RX}) = \frac{ln10}{10.\beta} . \frac{2(\pi\lambda)^n}{(n-1)!} . 10^{2nA} . e^{-\lambda\pi 10^{2A}} \tag{2.7}$$

Where $A = \frac{P_{TX} - 10\log(\alpha) - p_{RX}}{10\beta}$.

Figure 2.7 depicts this PDF of the received power signal $p_{RX}(d)$ in dBm at the input of the receiver. It shows that the power of the incoming RF signal ranges from -90 dBm to -20 dBm. Traditional receivers would be designed to work at the worst case scenario which corresponds to the minimum of incoming signal power, -90 dBm here. However, this worst case happens scarcely as the probability to receive the minimum power signal is very small (probability close to 0). As consequences, conventional receivers waste a large amount of power.

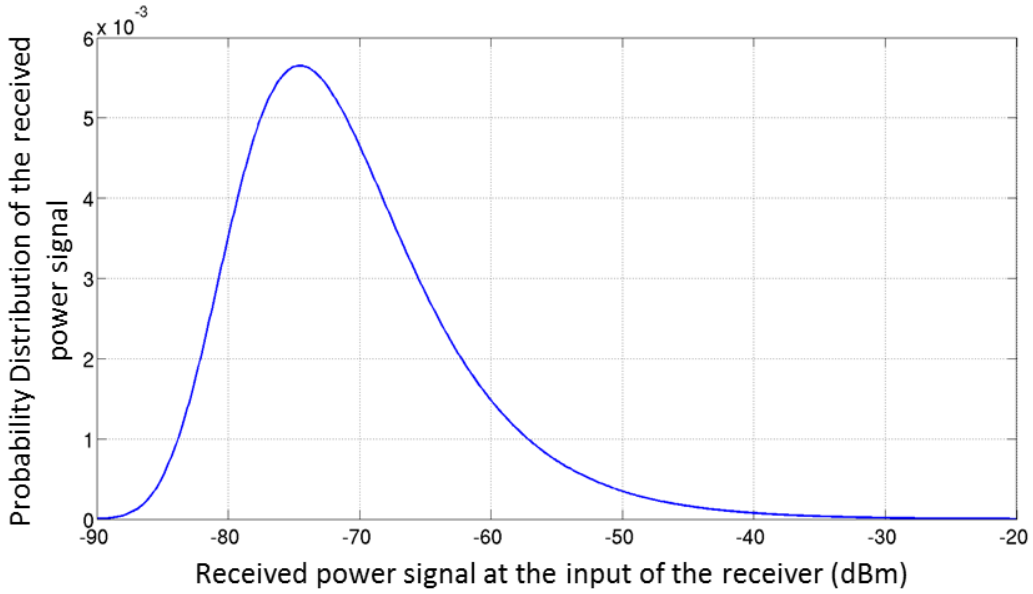


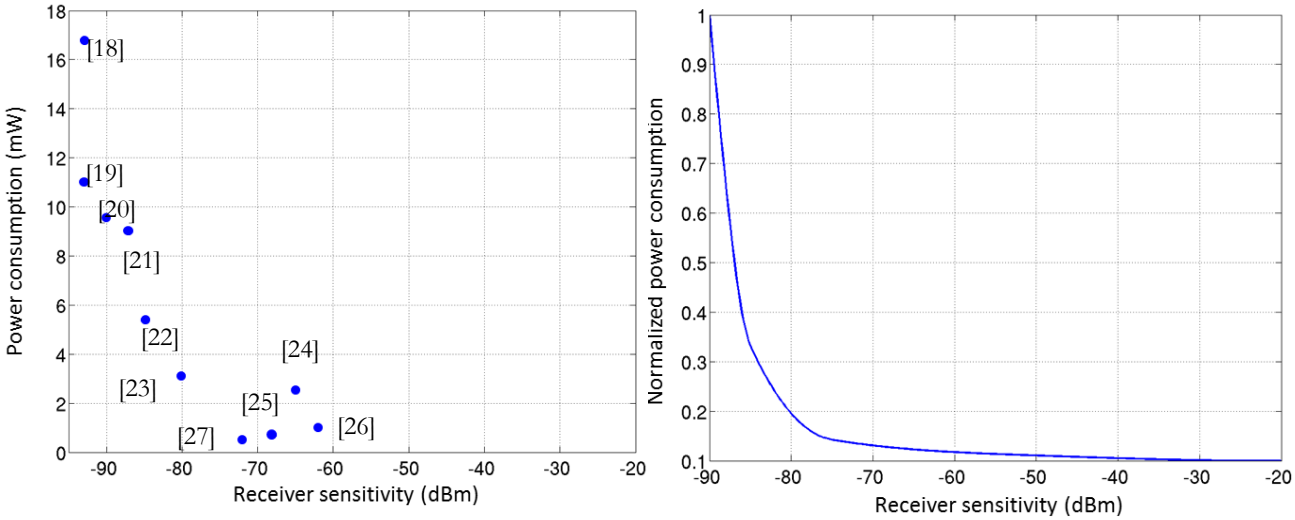
Figure 2.7 Probability Distribution Function of the received power signal at the input of the receiver.

To optimize the operating points of the tunable receiver, a model of the receiver sensitivity versus the power consumption is established in the next Section.

2.2.3 MODEL OF THE RECEIVER SENSITIVITY AND POWER CONSUMPTION

In order to evaluate the reduction in power consumption of the receiver when its sensitivity is degraded, the performances of receivers available in the literature are shown in Figure 2.8(a). The data rates of the receivers are comprise between 100kb/s and 1Mb/s. Because the data rate impacts directly the sensitivity of the receiver, the model can be adjusted with the data rate of the targeted application.

It demonstrates that, when the receiver sensitivity is relaxed, the overall power consumption of the receiver can significantly be reduced.



(a) (b)

Figure 2.8 Power consumption versus the receiver sensitivity: (a) State of the Art; (b) Normalized power consumption.

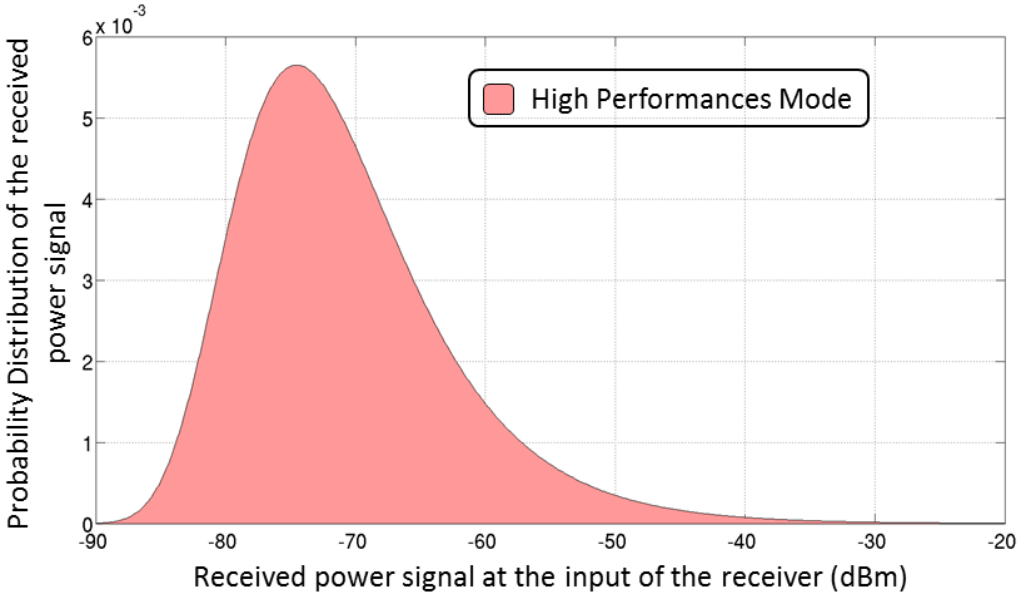
For the best approximation, an asymptotic curve is determined from the receiver's State of the Art performances. To do so, the power consumption is normalized with respect to the receiver with the minimum sensitivity as plotted in Figure 2.8(b).

This model is then used in the next step of the proposed methodology to define and optimize the discrete operating points of the proposed tunable receiver.

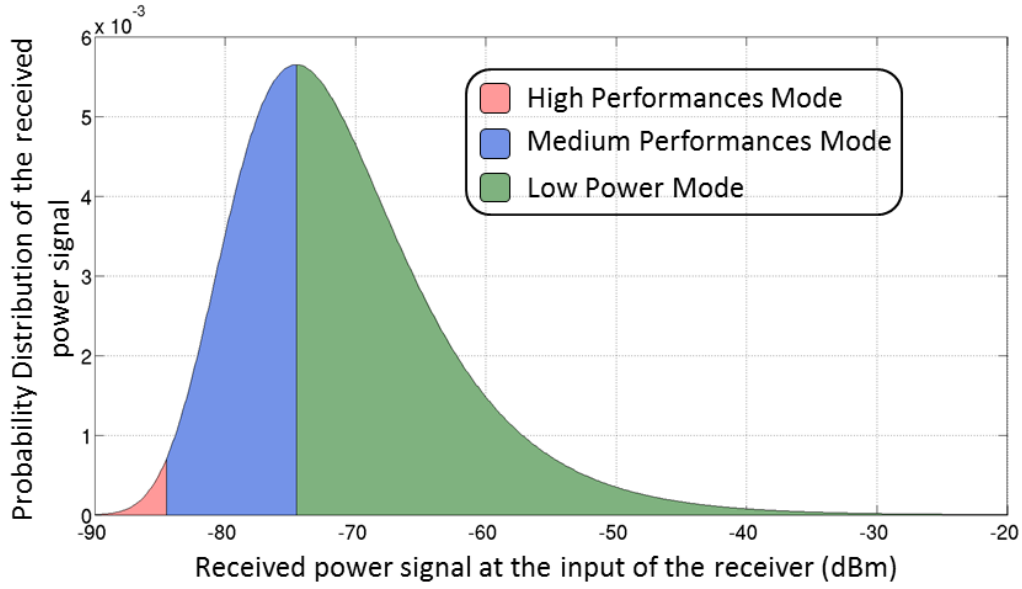
2.2.4 Optimal Reconfigurable Thresholds

This Subsection describes a methodology which works out the optimal number of operating modes and the associated sensitivity thresholds based on the model of the power consumption of the receiver. In fact, the final approach consists on an optimization of the thresholds using the probability distribution of the received power and the model of the sensitivity versus power consumption. Several sets of performances, each one dedicated to a specific range of sensitivity, are proposed. The objective is to find the best reconfiguration thresholds in order to optimize the power consumption with a moderate complexity in the system.

Figure 2.9 illustrates the difference between a traditional 1-mode receiver and a three performance modes tunable receiver.



(a)



(b)

Figure 2.9 (a) Traditional 1-mode receiver; (b) Tunable receiver for power savings.

The area under the PDF of each curve represents the duration time of the receiver in each of its modes. Therefore, the 1-mode receiver plotted in Figure 2.9(a) will be for 100% of its working time in the highest and unique performances mode. On the other side, a tunable receiver can relax its performance when the received signal power is stronger than worst case, and thus enabling power saving.

The gain on the overall power consumption, noted $Gain$, between 1-mode and *n*-modes receivers can be determined by Equation (2.8).

$$Gain = \frac{t_{mode_0}.P_{mode_0}}{t_{mode_1}.P_{mode_1} + \cdots + t_{mode_n}.P_{mode_n}} \quad (2.8)$$

With $t_{mode_0}.P_{mode_0} = 1$.

The fixed 1-mode performances receiver is called $mode_0$, t_{mode_n} is the usage time percentage in mode n and P_{mode_n} the power consumption normalized with respect to the high performance mode (for a 3-modes receiver, $n = 3$).

The sensitivity thresholds for the 3-mode operations are defined to optimize the overall gain of the power saving. In Figure 2.10, the gain is represented as a function of the first threshold (T1) and the second threshold (T2). The battery lifetime can be extended by a factor of 4.5 when T1 and T2 are set to -75 dBm and -85 dBm respectively.

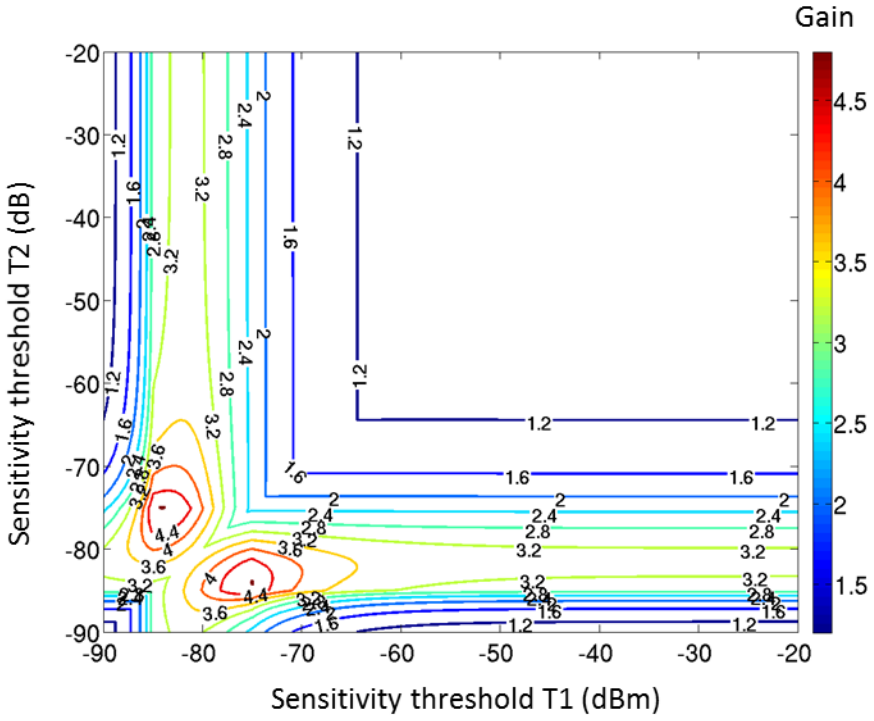


Figure 2.10 Best gain on the battery lifetime with two sensitivity thresholds (T1 and T2) for a 3-modes receiver.

The same methodology has been realized for several numbers of configuration modes. Figure 2.11 illustrates this gain as a function of the number of modes. The gain in battery lifetime is significantly increased from a single mode to a 3-modes receiver (red dot on Figure 2.11). Above, the gain still increases but the relative power saving is significantly reduced. Beside the complexity of implementation, the increase of silicon footprint limits the interest of developing a receiver featuring more than 3 operating modes.

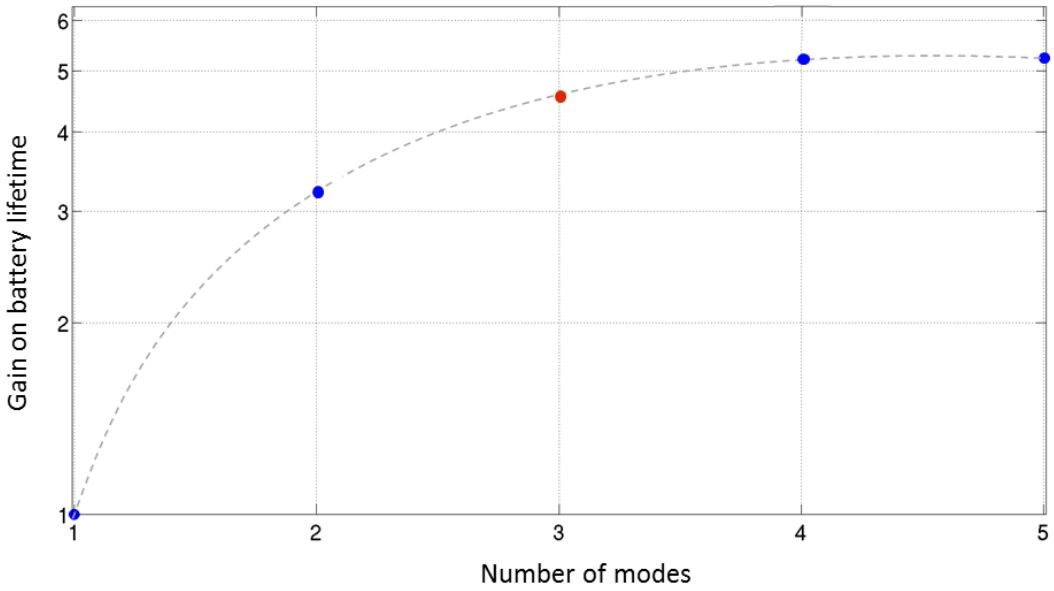


Figure 2.11 Maximum gain on the battery lifetime for each number of modes configurations.

Results of the computation for the proposed 3-modes receiver in terms of sensitivities P_{min}, percentages of the usage time and power consumptions P_{DC} of each mode are summed up in Table 2.2.

Mode	Low power mode	Medium performances mode	High performances mode
P_{min} (dBm)	-75	-85	-90
Usage time (%)	76	23	1
Pdc_{RX} (mW)	1.2	3.5	8

Table 2.2 Sensitivity thresholds for 3-modes tunable receiver.

In order to optimize the battery lifetime of the receiver, the proposed tunable receiver would feature the following conditions of operation:

- The low power mode has to be designed with a maximum power consumption of 1.2 mW. It will be in this state for 76 % of its lifetime.

- The medium mode has to consume less than 3.5 mW and it will be active for 23 % of its whole lifetime.

- The highest mode corresponds to the worst case scenario of communication, it is essential to guarantee the QoS. It is also the most power hungry mode (8 mW), for this reason it is only active 1 % of the receiver's lifetime.

The three optimized operating modes with the associated sensitivities and power consumptions are now defined from a receiver perspective. In order to evaluate the energy efficiency of the proposed receiver, the next Subsection compares the proposed optimized sensibility thresholds with an industrial module.

2.2.5 COMPARISON OF THE PROPOSED RECEIVER WITH AN EXISTING SOLUTION

Figure 2.12 illustrates the thresholds of a receiver available in the industry: the module from Atmel AT86RF233. The available Atmel adaptive receiver can reduce its power consumption between the two extreme modes by more than -20 %. However, the sensitivity of the receiver is degraded from -91 dBm to -49 dBm which offers very limited energy efficiency regarding the severe degradation of sensitivity. Moreover, the PDF of the received power signal demonstrates that aiming for a sensitivity of -49 dBm is not efficient as this case would happen less than 2 % in the lifetime of the receiver.

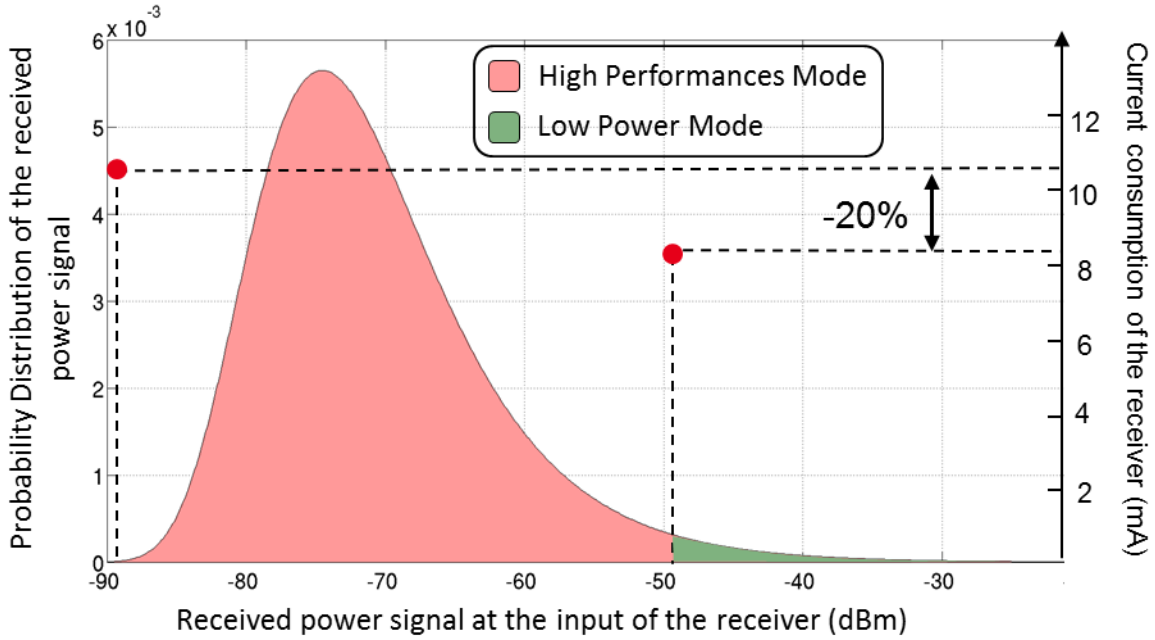


Figure 2.12 Tunable receiver thresholds illustration: Extreme modes of the Atmel AT86RF233.

Therefore, even if some industrial modules are tunable in order to gain battery lifetime, the energy efficiency is still low compared to the degradation of the performances. The proposed tunable receiver is optimized for both the power and the sensitivity.

Figure 2.13 illustrates the thresholds of the proposed optimized 3-modes receiver.

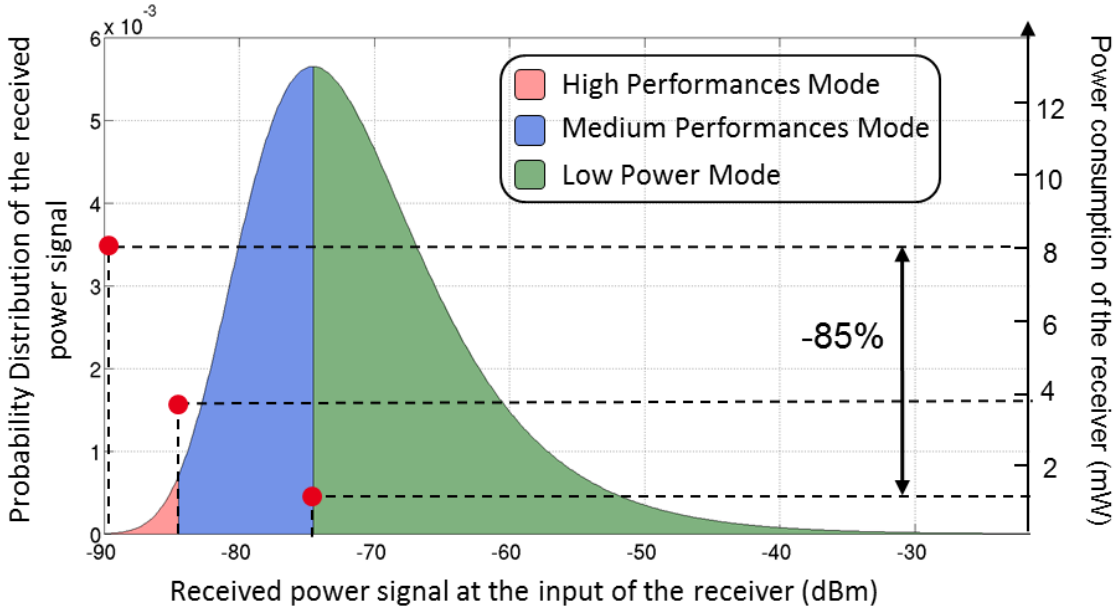


Figure 2.13 Proposed tunable receiver thresholds illustration.

The adaptive receiver proposed in this Chapter and the associate system analysis enable a significant power saving for the implementation of receivers dedicated to WSN based ZigBee® standard. Indeed, 85 % of reduced power is achieved between the high performances mode (sensitivity of -90 dBm) and the low power mode (sensitivity of -75 dBm) as illustrated in Figure 2.13.

Table 2.3 categorizes the differences between the Atmel module and the proposed tunable receiver.

Mode	ATMEL AT86RF233	Proposed Receiver
Tunability type	Continuous	Discrete
Number of modes	unlimited	3
Sensibility min HP mode (dBm)	-91	-90
Sensibility min LP mode (dBm)	-49	-75
Power reduction between the lowest and the highest modes	20 %	85 %

Table 2.3 Comparison of the proposed receiver with an industrial module.

The proposed 3-modes receiver enables a gain on the battery lifetime of factor of 4.5. This solution is thus well suited for low power IoT applications.

The next Section concentrates on a link budget on the proposed receiver in order to determine the set of specification of each block in each mode of operation.

2.3 LINK BUDGET ON THE PROPOSED RECEIVER

This Section proposes a link budget for the 3-modes receiver in order to determine the design specifications for each mode in terms of noise figure, gain, linearity and power consumption.

2.3.1 KEY PERFORMANCES OF THE BLOCKS COMPOSING A RECEIVER

A traditional receiver is composed of several building blocks as illustrated in the Figure 2.14.

The antenna filter selects the band with a minimum of attenuation. The LNA amplifies the weak signal collected by the antenna. It is expected to introduce a minimum of noise and deformation. The mixer performs the frequency down conversion of the RF incoming signal amplified by the LNA. To achieve the frequency translation the mixer needs a frequency synthesizer which delivers a stable continuous wave signal. The Phase Locked Loop (PLL) is a popular solution for the synthesis of the local oscillator. Before the analog to digital conversion by the ADC, further analog signal processing is performed based on filtering and Voltage Gain Amplification (VGA).

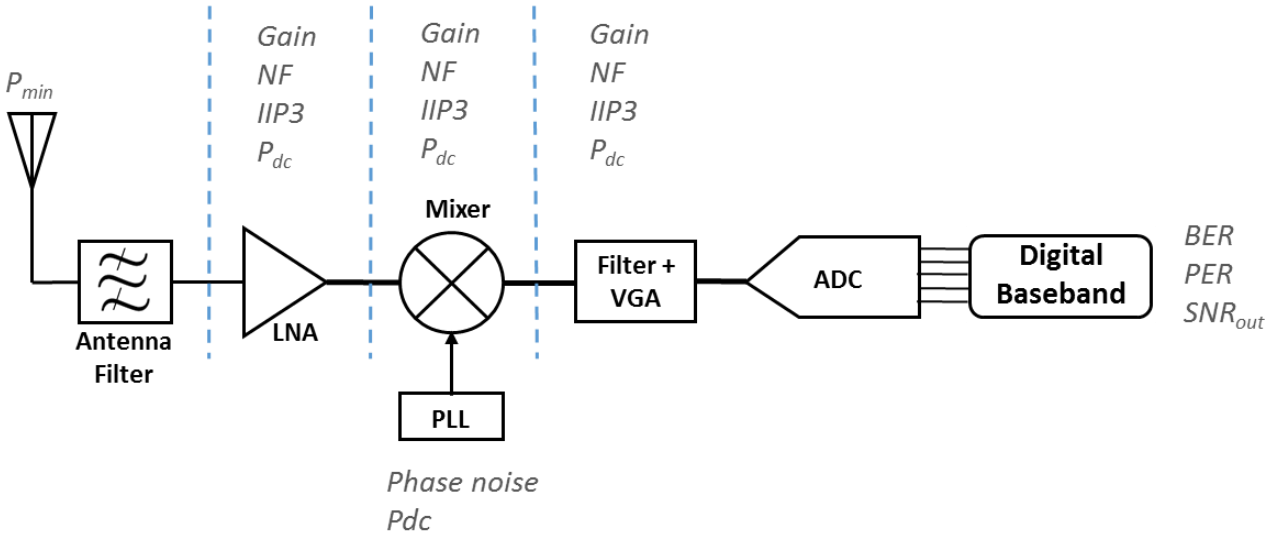


Figure 2.14 Traditional receiver architecture and key performances of the blocks.

2.3.2 PERFORMANCES OF THE RECEIVER IN EACH OPERATING MODE

The maximum Noise Figure (NF) of the receiver for each mode is derived with the equation of the sensitivity (Equation (2.9), [7]).

$$P_{min(dBm)} = NF_{RX(dB)} + 10.log(B) - 174 + SNR_{out(dB)} \quad (2.9)$$

Where P_{min} is the aimed sensitivity in each operating mode, the $SNR_{out(dB)}$ the signal to noise ratio, NF_{RX}, the noise of the receiver and B the bandwidth of the standard.

Both SNR_{out} and B are fixed by the standard requirements detailed previously in Table 2.1.

The aimed P_{min} and the usage time in each mode are determined with the thresholds optimization presented in Table 2.2.

The power consumption of the receiver (Pdc_{RX}) in each mode is based on the model of the sensitivity versus power consumption established previously and illustrated on Figure 2.8.

The final receiver specifications in each operating mode are detailed in Table 2.4.

Mode	Low power mode	Medium performances mode	High performances mode
P_{min} (dBm)	-75	-85	-90
Usage time (%)	76	23	1
NF_{RX} (dB)	22	12	7
Pdc_{RX} (mW)	1.2	3.5	8

Table 2.4 Receiver targeted design performances for each configuration.

Based on these three modes, the next Subsection concentrates on the performances of the LNA, the first block composing the receiver.

2.3.3 PERFORMANCES OF THE LNA IN EACH OPERATING MODE

As the first element of the receiver chain, the LNA limits the receiver in terms of sensitivity and is therefore a good candidate to perform optimized tunability.

From the performances of the receiver and Friis formulas (Equation (2.10), [28]), the specifications of the LNA in noise and gain are deduced.

$$NF_{RX} \approx NF_{LNA} + \frac{NF_{mix} - 1}{G_{LNA}} + \frac{NF_{VGA} - 1}{G_{LNA}G_{mix}} \quad (2.10)$$

The mixer performances are based on the mixer proposed in [29] which offers a gain G_{mix} of -8 dB and 15 dB of noise figure NF_{mix}.

The noise figure and gain performances of the Variable Gain Amplifier (VGA) are based on the VGA proposed in [30]. The authors propose a VGA which is able to provide a gain of 43 dB and a noise figure NF_{VGA} of 20 dB.

The power consumption of the LNA is based on the repartition of the power consumption in a receiver available in [76] and on the receiver power consumption model of Figure 2.8.

Finally, the Input Referred Third Order Intercept Point (IIP3) is specified to estimate the linearity. In the aimed application, the requirement on the IIP3 of the LNA is evaluated to a minimum of -15 dBm. This evaluation is further detailed in Chapter 3.

Table 2.5 presents the LNA targeted specifications for the three levels of performances.

Mode	Low power mode	Medium performances mode	High performances mode
P_{min} (dBm)	-75	-85	-90
Usage time (%)	76	23	1
NF_{LNA} (dB)	7	5	3
Gv_{LNA} (dB)	15	20	25
Pdc_{LNA} (mW)	0.3	0.9	2
$IIP3_{LNA}$ (dBm)	-15	-15	-15

Table 2.5 LNA targeted design performances for each configuration.

2.4 SYSTEM-LEVEL ANALYSIS: SUMMARY

A new method to increase the battery lifetime of a receiver is proposed in this Chapter. It is based on a discrete reconfiguration of the performances to enable a fast and efficient solution. As a case of study, the implementation of a WSN with the ZigBee® standard is developed. The analysis of the system demonstrates that a 3-modes receiver would achieve a factor of power saving of 4.5 compared to a fixed performance receiver. The specifications of the radio section are derived with an emphasis on the LNA performances, Table 2.5, for the 3 modes of operation.

Interestingly, the system analysis demonstrates that the proposed receiver is most of the time (76% of its lifetime) in low power mode. It makes sense to first optimize the design of the circuits for this mode of operation. The focus of the next Chapter is to propose an innovative solution for reducing the power consumption of inductorless ULP LNA design while respecting the targeted specifications of this mode.

CHAPTER 3

DESIGN OF AN ULP LNA USING FD-SOI BODY BIASING: CIRCUIT-LEVEL ANALYSIS

Previously, in Chapter 2, the system analysis demonstrates that the optimized channel aware receiver is for more than 75 % of its lifetime in low power mode. Therefore, this mode has to be power optimized. The two other modes: high and medium performances can be made from available industrial modules such as the Atmel AT86RF233. The optimized low power receiver is thus placed in parallel of this industrial module as depicted in Figure 3.1.

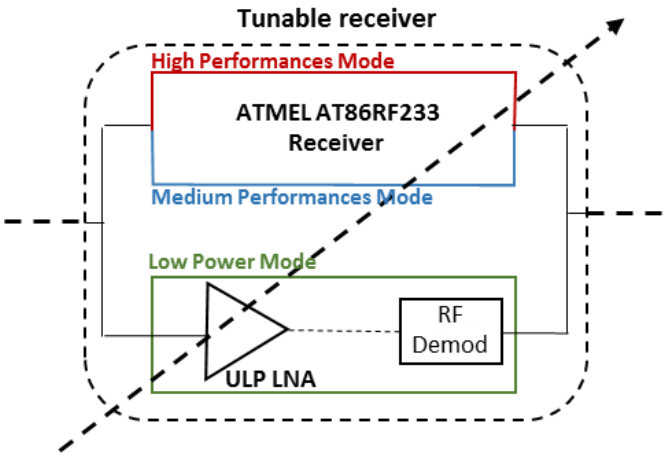


Figure 3.1 Tunable receiver first version.

This Chapter concentrates on the design of a power-optimized inductorless Ultra Low Power (ULP) Low Noise Amplifier (LNA), which fulfils the design requirements established in Chapter 2. Beside, the Fully Depleted Silicon-On-Insulator (FD-SOI) offering a new bias opportunity of the transistor, the 28 nm FD-SOI technology of STMicroelectronics has been selected to further explore our purpose.

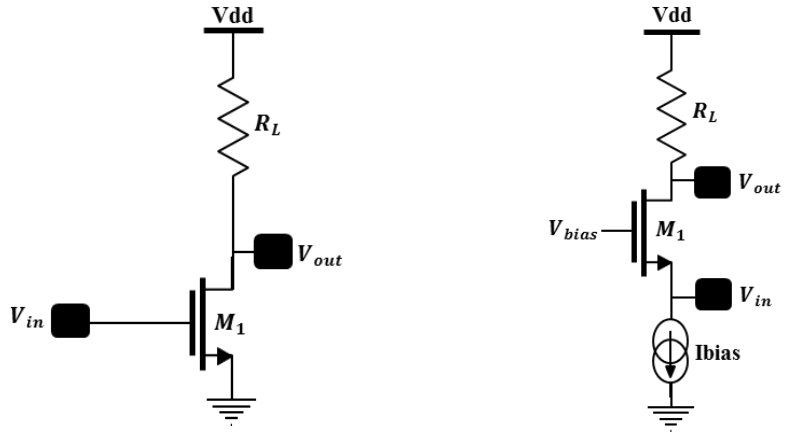
The first Section of this Chapter concentrates on a description of inductorless LNAs State Of the Art and of the techniques, proposed in the literature, to improve the performances of such circuit. Then, the proposed topology is described together with the analytic derivation of the most important characteristics -i.e. the voltage gain (Gv), the input impedance (Zin) and the noise figure (NF)-. The derivations of Gv, Zin and NF are further investigated to work out a first cut design for the targeted

performances. Interestingly, the Ultra-Thin Body and Buried oxide (UTBB) FD-SOI technology is exploited in order to decrease the power supply of the LNA while keeping constant performances. Finally, the Integrated Circuit (IC) measurements are presented in the last Section and compared with the LNAs of the literature.

3.1 STATE OF THE ART OF INDUCTORLESS ULP LNAS

The challenges for inductorless LNAs design is achieving high gain and low noise figure over a large bandwidth and a low power consumption. Moreover, because the LNA directly interfaces with the antenna, 50-Ω impedance matching at its input is essential.

There is two basic topologies for the implementation of an inductorless LNA: the common source configuration, Figure 3.2 (a) and the common gate configuration, Figure 3.2 (b).



(a) (b)

Figure 3.2 Basic topologies for amplifiers: (a) Common Source; (b) Common Gate.

These two basic topologies are now further detailed and discussed.

3.1.1 COMMON SOURCE (CS) TOPOLOGIES

In a basic Common Source topology, the input impedance is set by the gate-to-source capacitance. Hence, additional components are usually added at the input in order to match to the source impedance and to optimize the noise figure.

However, without any inductance, the only ways to reduce the input impedance of a Common Source topology is either by adding directly a 50-Ω resistance at the input or by adding a feedback stage.

Three popular topologies based on the CS configuration are further considered to address the context: the CS Resistively terminated based LNA, the CS Resistive Shunt Feedback LNA and the CS Active Shunt Feedback LNA.

CS RESISTIVELY TERMINATED BASED LNA

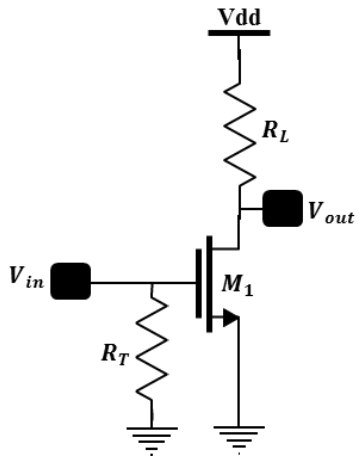


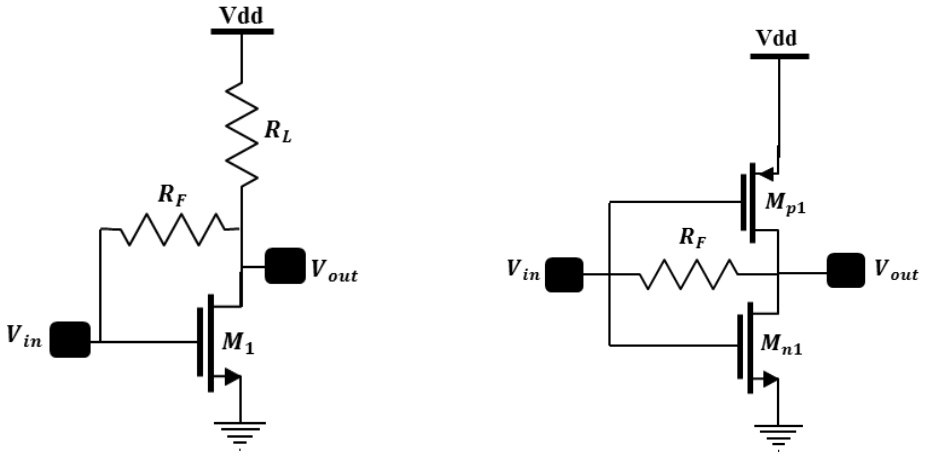
Figure 3.3 Common Source Resistively Terminated LNA.

This topology, Figure 3.3, benefits from no constraint on the transconductance of the transistor M_1 for the input matching as its input impedance is fixed by the resistance R_T (Equation (3.1)).

$$Zin = R_T \tag{3.1}$$

The gain only depends on the transconductance of M_1 and the load resistance R_L. The main drawback of the resistively terminated architecture is the impact of the thermal noise of R_T on the Noise Figure (NF) of the LNA. In [32], the authors demonstrate that, to obtain a NF of 6 dB, more than 25 mS are needed on the transconductance of M_1 which would demand large power consumption.

CS RESISTIVE SHUNT FEEDBACK BASED LNA



(a) (b)

Figure 3.4 Common Source Resistive Shunt Feedback LNA: (a) Resistive Shunt Feedback; (b) Current reused inverter.

The most popular implementation of a resistive feedback single stage amplifier is illustrated in Figure 3.4(a). Using the Miller's theorem the input impedance can be expressed as in Equation (3.2).

$$Zin = \frac{R_F}{1 - Gv}. \tag{3.2}$$

This structure achieves overall good performances with a significant power consumption ([32], [33], [34]). Indeed, the feedback resistance R_F reduces the output impedance and, as consequence, the voltage gain. To compensate it the transconductance $gm1$ is increased.

In order to double the transconductance, the load of the shunt feedback structure can be replaced by an active load, here the PMOS device. This topology is a push-pull inverter also called "current-reused" and is depicted in Figure 3.4(b). This circuit offers the possibility to enhance the equivalent gm for the same current and to keep the same input resistance and noise figure. However, the main disadvantage of this topology is the degradation of the bandwidth of the LNA as detailed in [35]. Furthermore just as for a cascode architectures, it also requires a higher supply voltage due to voltage headroom necessary for the additional PMOS.

CS ACTIVE SHUNT FEEDBACK BASED LNA

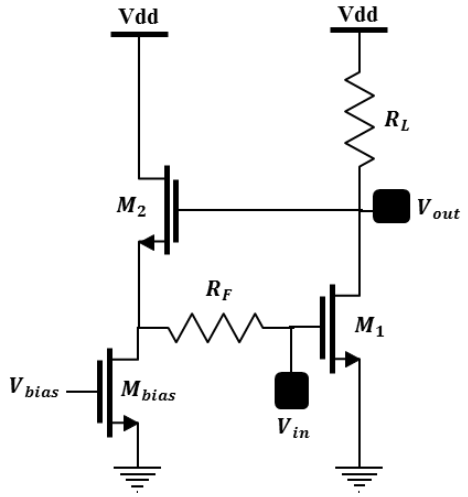


Figure 3.5 Common Source Active Shunt Feedback LNA.

Another option for inductorless CS architecture consists on adding an active source follower feedback to the input common source transistor as illustrated by Figure 3.5 [36]. In this topology, the input impedance is expressed by Equation (3.3).

$$Zin = \frac{1 + gm_2 R_F}{gm_2(1 - Gv)}. \tag{3.3}$$

The main tradeoff of this structure concerns the transconductance of M_2 and the feedback resistance R_F. The linearity and the noise of this structure depend on the value of R_F. Unfortunately the reduction of the NF requires a small value of R_F whereas an improvement of the linearity calls for a large resistance according to [37]. Furthermore, the active feedback around M_2 requires additional power consumption.

3.1.2 COMMON GATE (CG) TOPOLOGIES

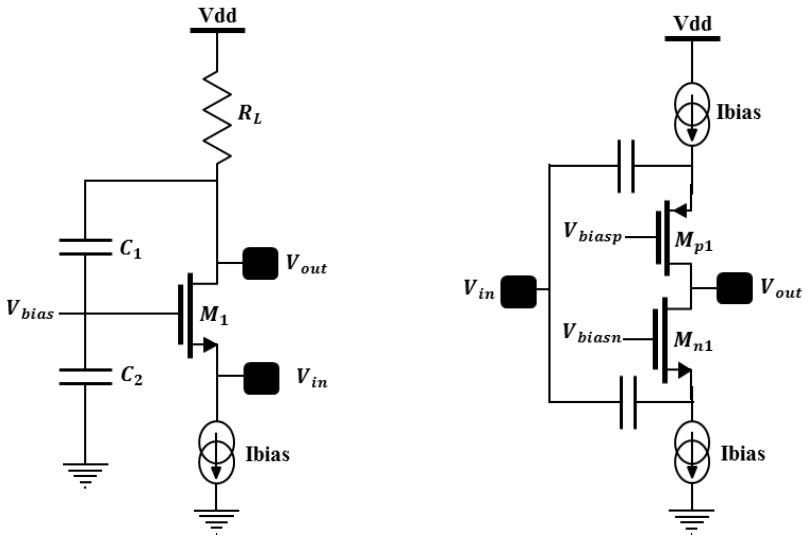
Designing CG inductorless LNAs offers the possibility of an easy input matching through the transconductance (gm) of the input transistor, as illustrated in Equation (3.4). This expression does not take into account the parasitics and further assumes a moderate impedance for the output load.

$$Zin = \frac{1}{gm}. \tag{3.4}$$

Furthermore, the CG configuration achieves overall good performances which makes it popular for the implementation of low cost radios. However, because the choice of the transconductance is enforced by the input impedance matching, this architecture generally exhibits a limited noise figure.

As for CS LNAs, there are several techniques available in the literature to improve the performances of a basic CG topology. The next Subsections introduce and discuss some of them.

CG PASSIVE FEEDBACK BASED LNA



(a) (b)

Figure 3.6 Common Gate Passive Feedback topologies: (a) Series Feedback; (b) Current Reused inverter.

In order to boost the linearity of the system, a series feedback made by a capacitive voltage divider [38] can be added to the basic CG structure as depicted in Figure 3.6(a). However, this technique deteriorates the gain and the bandwidth of the LNA.

Another solution to decrease the power consumption of a Common Gate topology is to double the available transconductance (gm) with a current reuse configuration as illustrated by Figure 3.6(b) [39]. Beside just as the CS current reuse configuration, the minimum supply voltage V_{DD} of the complementary topology of Figure 3.6(b) is larger than the supply voltage of the NMOS based implementation of Figure 3.6(a).

CG ACTIVE SHUNT FEEDBACK BASED LNA

This topology, illustrated in Figure 3.7, is based on a current amplifier made by a flipped voltage follower [40], [41]. The shunt feedback is realized by the CS $M2$ transistor. The performances are very restrictive for gain and noise figure optimization. Moreover, the power supply has to be sufficiently high because of the cascode PMOS making the current source.

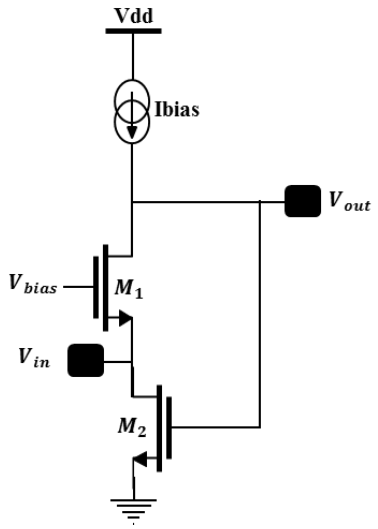


Figure 3.7 Common Gate Active Shunt Feedback topology.

CG FEEDFORWARD BASED LNA

A CG series feedforward LNA is based on a basic CG featuring an extra inverting amplifier ($-A$) between the input and the transistor's gate of the CG LNA. This gain can be passive, using the Capacitive Cross Coupling technique [42] or active with a complementary CS circuit [43].

This technique, also named gm-boost due to the boost effect on the gate to source voltage of transistor $M1$, enables a gain enhancement and a reduction of the noise figure with a small additional power budget.

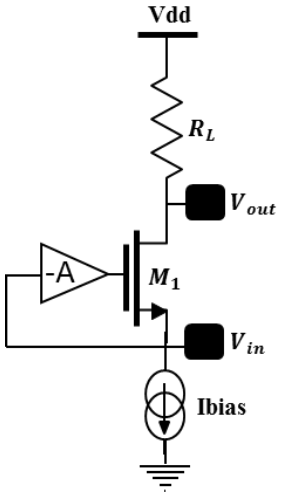


Figure 3.8 Common Gate Feedforward topology.

The next Subsection presents some complementary techniques introduced in the literature to improve the performances of inductorless LNAs.

3.1.3 OTHER DESIGN TECHNIQUES

NOISE CANCELLING

This technique based on Bruccoleri's theory, consists on designing structures in which the gain of the signal can be increased and, at the same time, the thermal noise can be suppressed [44], [45]. In Figure 3.9, the signal voltages at the input of node X and output of node Y have opposite signs due to the negative gain of a MOS transistor. On the other hand, the noise voltages of these two nodes have equal signs. This difference of the noise and signal signs at nodes X and Y enables a cancelling of the input device noise while simultaneously adding its signal. To do so, an amplifier of node X voltages and an adder of node X and Y have to be designed. The final theorical signal results on a larger voltage gain signal and a cancelled noise.

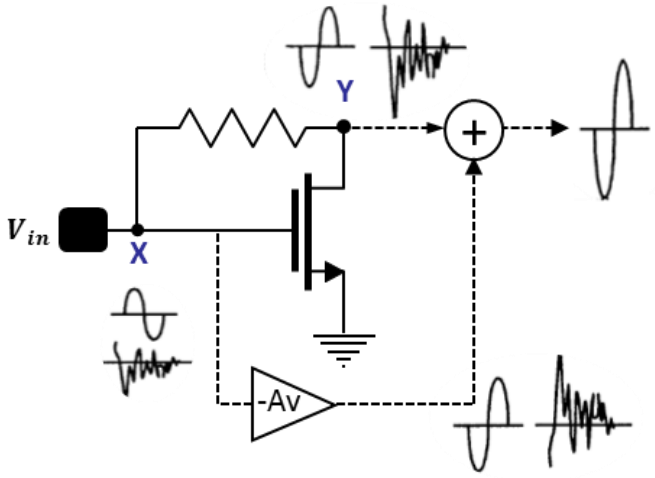


Figure 3.9 Noise Cancelling technique [44].

The theory of this technique seems very promising for LNA designs where the noise has to be minimized and the gain maximized. This technique has two main disadvantages. First, the additional amplifier is active and adds noise to the system. Thus, extra power consumption is needed to reduce its noise contribution. Then, the unpredictable effects of Process, Voltages and Temperature (PVT) variations can shift the phase of the noise and of the signal which could potentially reverse the situation and increase the noise.

DISTORTION CANCELLING

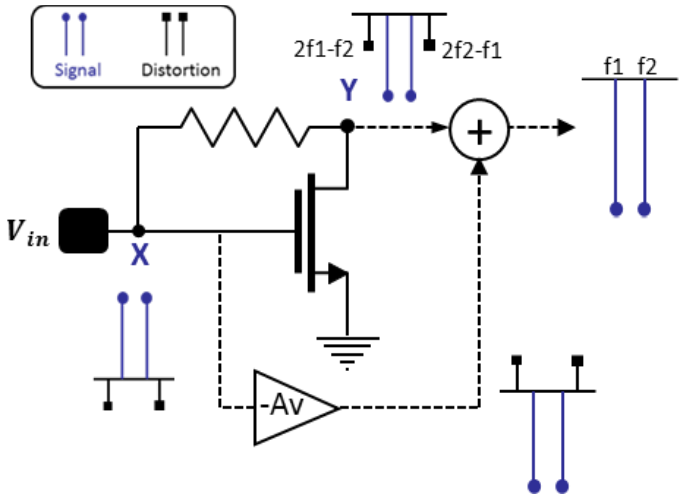


Figure 3.10 Distortion Cancelling technique [46].

This technique is based on the Taylor approximation of the drain current of a transistor. In that case, the non-linear high order terms are modeled by a current source in parallel of the active transistor. Two input frequencies $f1$ and $f2$ with the same amplitude produce two 3rd intermodulations (IM) at frequency $2f1.f2$ and $2.f2 - f1$. At node X and Y the wanted signals are in opposite phase while the distortion products are in phase. This technique is very similar to the noise cancelling technique. In fact, this difference between phases is used to cancel the distortion at the output thanks to feedforward inverter amplifier ($-Av$) which amplifies the signal and shifts the phases of the signal and distortion products (Figure 3.10, [46]).

Comparable to noise cancellation, the main disadvantages of this technique is weak robustness to PVT variations and extra power consumption needed for the design of the amplifier and adder.

3.1.4 STATE OF THE ART INDUCTORLESS ULP LNA: CONCLUSION

In Chapter 2, a system analysis has been proposed in order to determine the targeted performances of the LNA. Table 3.1 reminds the targeted performances in gain, noise figure, linearity, input matching and power consumption of the LNA for the low power mode.

Mode	Low power mode
S11 (dB)	<-10
NF_{LNA} (dB)	7
Gv_{LNA} (dB)	15
$IIP3_{LNA}$ (dBm)	-15
Pdc_{LNA} (mW)	0.3

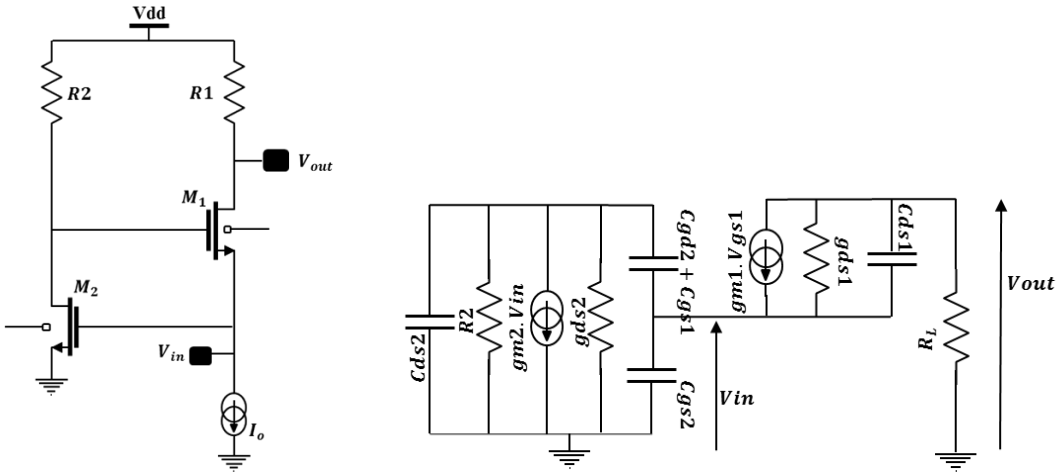
Table 3.1 ULP LNA specifications.

Based on the State of the Art of inductorless ULP LNAs and the targeted performances, the most promising configuration to address these specifications is the gm-boost CG Feedforward LNA. Indeed, it offers a good tradeoff between the performances of the LNA and its power consumption.

The next Section proposes an analytical description of a gm-boost CG LNA and a design methodology in order to fulfil the requirements of ULP designs. Then, a new technique to decrease the power consumption of the LNA with body biasing of FD-SOI transistors is demonstrated. Finally, the measurement results are shown and discussed.

3.2 PROPOSED ULP LNA

The topology of the proposed LNA and its simplified small signal model are depicted in Figure 3.11(a) and (b) respectively. The transistor $M1$ and the load resistance $R1$ feature the CG amplifier, and the forward amplifier is implemented with the CS configuration $M2$ and $R2$. The RF signal is simultaneously applied to the source and the gate of $M1$ through ($M2$-$R2$). This configuration enables an increase of its gate to source voltage (Vgs) and thus enhances the available gain.



(a) (b)

Figure 3.11 CG gm-boost LNA: (a) Schematic; (b) Small signal model.

The analytic derivations of the input impedance, the voltage gain, the noise figure and the linearity are proposed in the following Subsections to investigate the behavior of the circuit.

3.2.1 INPUT IMPEDANCE

If the input impedance Z_{in} of the LNA is not matched to the antenna, or antenna filter, the signal may bounce back to the antenna to be reradiated. Impedance matching is characterized by the S-parameter S_{11} expressed in Equation (3.5).

$$S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \tag{3.5}$$

Where Z_0 is the impedance of the source delivering the signal (the antenna filter as instance), typically 50 Ω. The S_{11} parameter is directly related to the input signal power and the power absorbed by the LNA as detailed in Equation (3.6).

$$1 - {S_{11}}^2 = \frac{Input\ Power\ of\ the\ LNA}{Available\ Power\ from\ the\ Source} \tag{3.6}$$

A S_{11} < -10 dB corresponds to a signal absorption of more than 90 %. It is the limit fixed in this work.

Based on its small signal model depicted in Figure 3.11(b), the input impedance of the proposed CG gm-boost LNA is determined by Equation (3.7).

$$Zin_{LNA} = \frac{V_{in}}{I_{in}} = \frac{1 + C_{ds2}.R_2.j\omega + C_{12}.R_2.j\omega}{gm_1(1 + gm_2R_2 + C_{ds2}R_2j\omega) - C_{gs2}j\omega - C_{ds2}C_{gs2}R_2\omega^2 + C_{12}j\omega + gm_2C_{12}R_2j\omega - C_{ds2}C_{12}R_2\omega^2 + C_{gs2}C_{12}R_2\omega^2} \tag{3.7}$$

With $C_{12} = C_{gd2} + C_{gs1}$.

3.2.2 VOLTAGE GAIN

The gain of the LNA impacts directly the noise of the system according Friis Formula [28]). The voltage gain of the CG gm-boost LNA is given in Equation (3.8).

$$Gv_{LNA} = \frac{Vout_{LNA}}{Vin_{LNA}} = \frac{\frac{gm_1.\ (1 + gm_2.R_2 + C_{ds2}.R_2.j\omega)}{1 + C_{ds2}.R_2.j\omega + (C_{gd2} + C_{gs1}).R_2.j\omega} + gds_1 + C_{ds1}.j\omega}{gds_1 + \frac{1}{R_1} + C_{ds1}.j\omega} \tag{3.8}$$

3.2.3 NOISE FIGURE

The noise figure defines the minimum detectable signal from the receiver. Also based on Friis Formula [28], the LNA, as the first element of the chain, constraints the receiver and dominates the noise contribution. Therefore, its intrinsic noise has to be minimized.

There are three noise sources in MOSFET transistors [47]: the thermal noise, the 1/f noise and the high frequency noise. In the design of a LNA for IoT applications, only the thermal noise is taken into account.

The model of the thermal drain current noise is defined in Equation (3.9).

$$\overline{i_d^2} = 4.k.T.gds_0 \tag{3.9}$$

With k the Boltzman constant, T the absolute temperature and gds_0 the output conductance of the transistor when $Vds = 0$.

This induced noise by the active transistors of the design is introduced in the calculation of the LNA's noise figure. The detail of the noise figure calculation is available in Appendix and is given in Equation (3.10).

$$NF_{LNA} = 1 + \frac{\frac{\gamma}{\alpha} + \frac{\gamma}{\alpha}.gm_2.R_2^2.gm_1 + \frac{4.R_2 gm_1}{(1+gm_1.R_s)^2}}{R_S.(1+gm_2.R_2)^2.gm_1}. \tag{3.10}$$

3.2.4 LINEARITY

The linearity performance gives information about the signal level that the receiver can properly process which defines the Signal to Noise Distortion Ratio (SNDR). The nonlinearity of elements such as transistors impact the quality of the signal transmission. The nonlinear relationship between the input and the output of a system is defined by the Taylor Series (Equations (3.11), [48]).

$$out(t) = a_1.in(t) + a_2.in^2(t) + a_3.in(t)^3 + \ldots \tag{3.11}$$

Where $out(t)$ is the output signal of a system, $in(t)$ the input and a_x are linear coefficients.

For the core of a Common Gate LNA, the gate terminal is at AC ground and the input-referred voltage intercept point for third-order intermodulation is given in Equation (3.12) [49].

$$\frac{1}{V_{IIP3_{CG}}^2} \cong \frac{3}{4}.\left|\frac{a_3}{a_1}\right| \qquad (3.12)$$

At the output, several nonlinearity types are present: signal distortions, harmonic distortions and intermodulation distortions (due to the presence of RF blockers for instance). In order to evaluate these distortions, two LNA characteristics have been defined.

First, the 1-dB Compression Point (noted P_{1dB}) which corresponds to the maximum input power level for which the output power response is no longer a linear function of the input power.

Then, the 3rd order Input Intermodulation Point (noted $IIP3$) is defined by the input level at which the fundamental output and the intermodulation product curves intercept, as depicted in Figure 3.12.

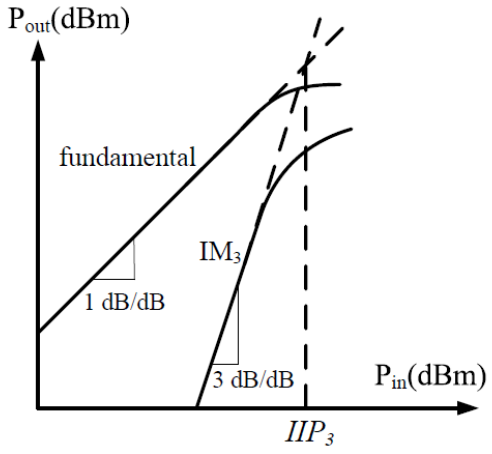


Figure 3.12 Definition of IIP3: output power versus input power at two frequencies.

The nonlinearity of a Common Gate gm-boost topology have been detailed and analyzed in [49]. The $IIP3_{CG\ gm-boost}$ of this structure is determined from the $IIP3_{CG}$ of a CG configuration and the gain of the boost G_{boost} as expressed in Equation (3.13).

$$V_{IIP3_{CG\ gm-boost}} = \frac{V_{IIP3_{CG}}}{1 + G_{boost}} \qquad (3.13)$$

In [43], the simulation and the calculation of the $IIP3$ based on this equation have been compared and Equation (3.13) can be considered as valid at first estimation.

3.3 DESIGN METHODOLOGY

The purpose is to design a LNA which addresses the specifications of Table 3.1 with the lowest power consumption. Therefore, a complete understanding of the behavior of the circuit and its limitations are essential to obtain the optimal design point.

This Section concentrates, first, on the behavior of the CG gm-boost LNA in order to find the best configuration. Then, the minimum power consumption which provides the correct performances is determined. Finally, an investigation on the possibility to decrease the power consumption of the LNA via the body biasing of the FD-SOI transistors is proposed.

3.3.1 BEHAVIOR OF THE CIRCUIT

Based on Equations (3.7), (3.8) and (3.10), the behavior of the input impedance Zin, the gain and the noise figure NF of the LNA for several couples of $(gm1, gm2)$ are plotted on Figure 3.13.

The input matching is considered as acceptable—i.e., real part of Zin between 25 Ω and 75 Ω and imaginary part of Zin close to 0 which gives a $S11$ under -10 dB. The conditions on $(gm1, gm2)$ which fulfil the requirements of Table 3.1 are also illustrated.

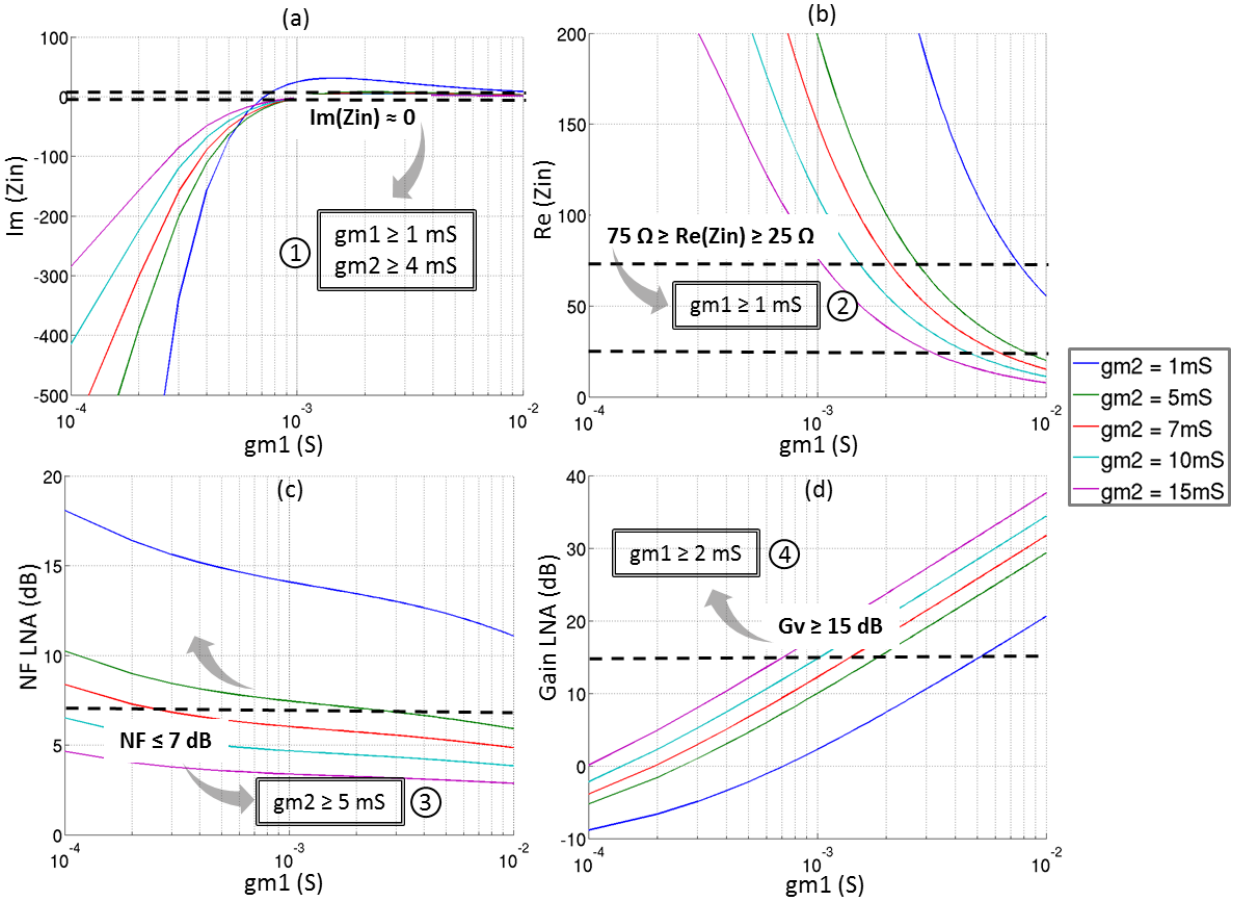


Figure 3.13 Behavior of the circuit for several (gm1, gm2): (a) Imaginary part of Zin; (b) Real part of Zin; (c) Noise Figure in dB and (d) Voltage gain in dB.

In order to optimize the power consumption of the proposed LNA, the minimum of $(gm1, gm2)$ respecting the conditions ①, ②, ③ and ④ are:

- $gm1$ = 2 mS;
- $gm2$ = 5 mS.

Active transistors of the LNA ($M1$ and $M2$) have minimum gate length to achieve a maximum bandwidth at a minimum power consumption. To work out the most relevant width of transistor with respect to the targeted specifications, a Figure of Merit (FoM_1) of the LNA is defined in Equation (3.14).

$$FoM_I = 20\,log\left(\frac{Gv_{lin}.BW_{GHz}}{Pdc_{mW}.(F_{lin}-1)}\right); \quad (3.14)$$

Where BW is the bandwidth in GHz, Gv is the voltage gain in linear, Pdc is the power consumption in mW and F is the noise figure of the LNA.

Figure 3.14 depicts the FoM1 of the LNA for each configuration of the current densities.

The optimum current densities are: $J1_{opt} = 9\mu A/\mu m$ in transistor $M1$ and $J2_{opt} = 11\mu A/\mu m$ in transistor $M2$. The width and the drain current of each Low Voltage Threshold (LVT) transistor are then derived to achieve the transconductance $gm1$ and $gm2$ previously extracted from Figure 3.13.

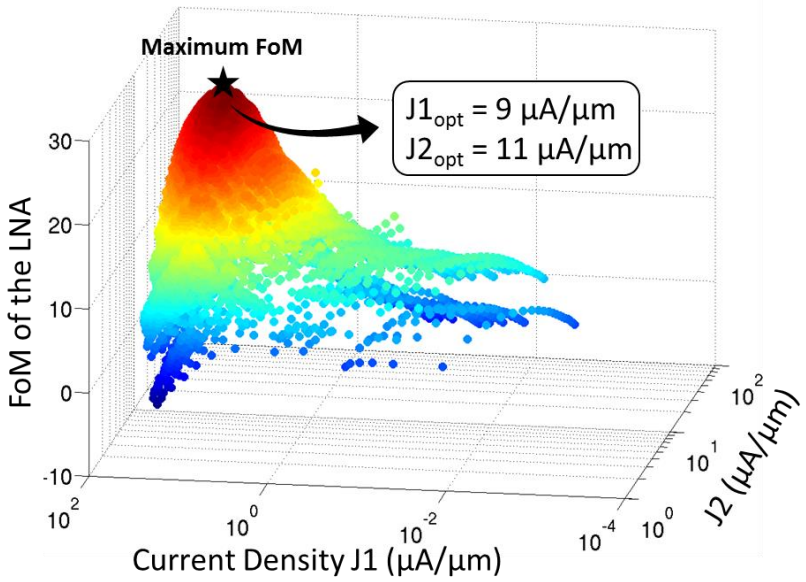


Figure 3.14 Factor of Merit of the LNA versus the current density of transistors M1 and M2.

The next Section works out the limitation of the proposed circuits in terms of power saving. Some circuit techniques are also discussed to improve the tradeoff between performances and power consumption.

3.3.2 LIMITATIONS

Considering the topology available in Figure 3.11(a), there are several ways to reduce the power consumption of the circuit: by tuning the power supply (Vdd), the current biasing ($Ibias$) and/or by adjusting the widths (W) of the transistors and the resistances (R).

These different techniques are further combined to reduce the overall power consumption of the LNA. Figure 3.15 illustrates the minimum of power consumption which guarantees the performances at several fixed supply voltages.

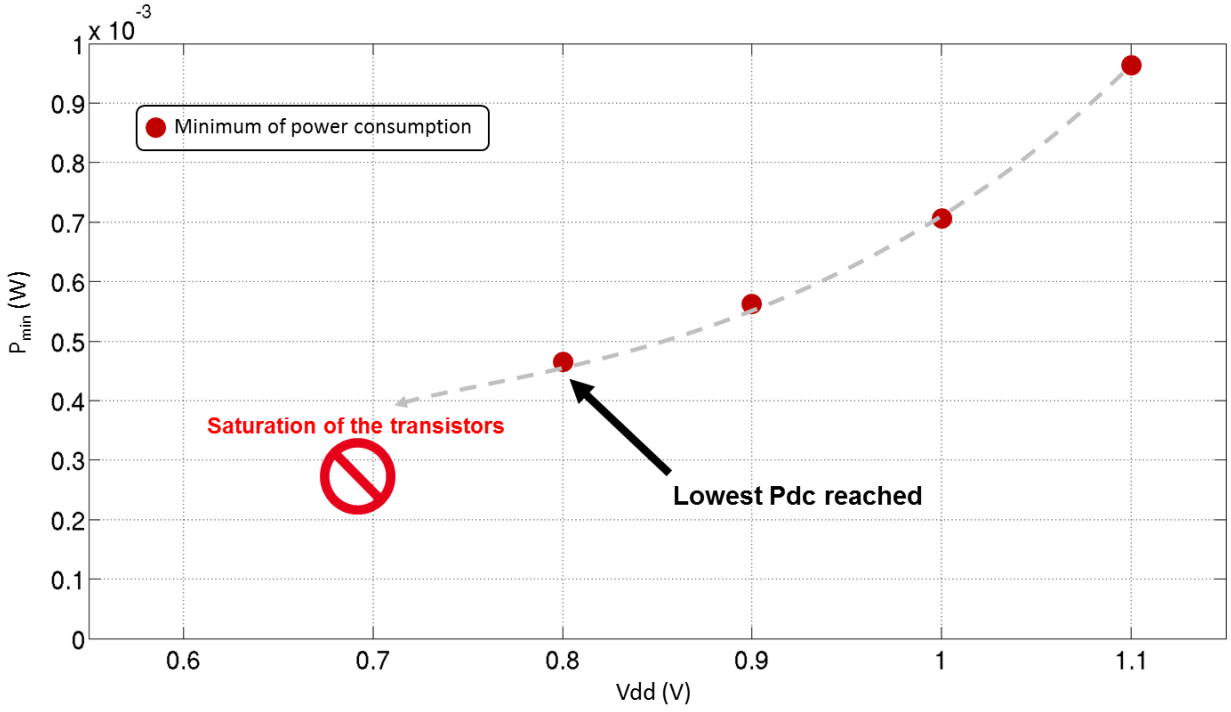
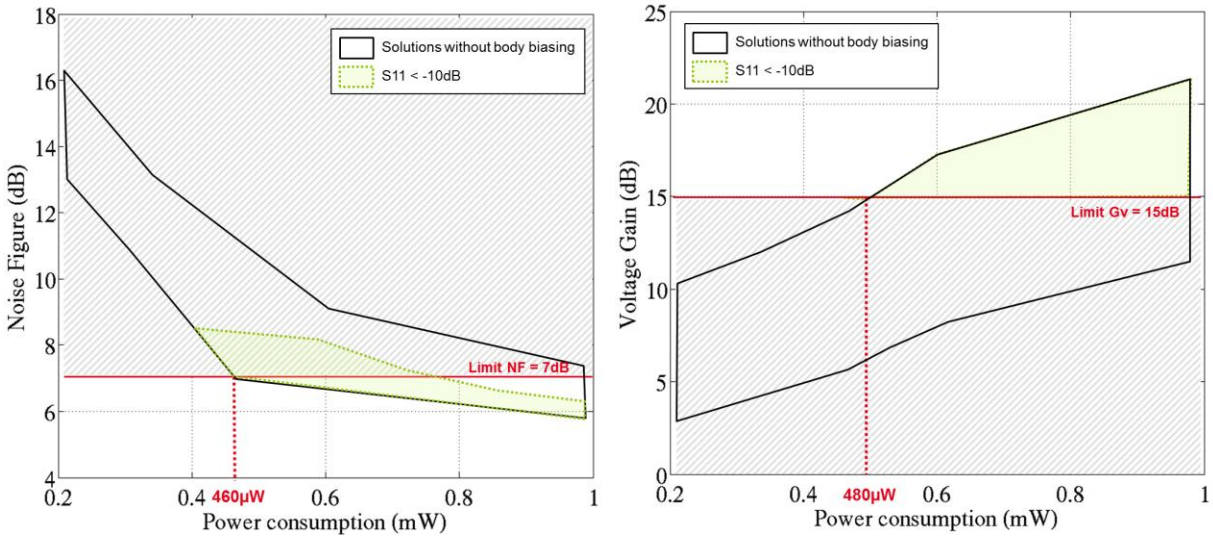


Figure 3.15 Minimum of power consumption for each power supply Vdd which respects the conditions Noise Figure < 7dB and Gain > 15 dB.

The minimum supply voltage in a body tied configuration, red dots in Figure 3.15, is 0.8V. Beyond this power supply, there is no solution for a correct saturation of the transistors.

Figure 3.16 shows the simulations for several $Vdd, Ibias, W$ and R. The minimum of power consumption required to address the performances of Table 3.1 is 480 µW at a supply voltage of 0.8V. At that power consumption, the LNA achieves a voltage gain of 15 dB and a noise figure of 6.9 dB.



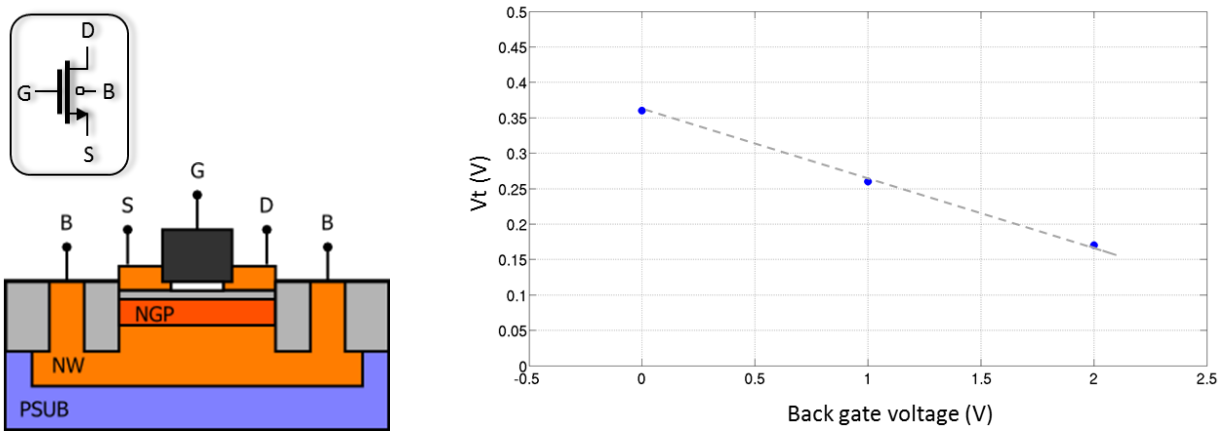
(a) (b)

Figure 3.16 Minimum of power consumption without body biasing to guarantee: (a) Noise Figure < 7 dB and (b) Gain > 15 dB.

An exploration of the back gate biasing of FD-SOI technology to further reduce the voltage supply is proposed in the next Subsection.

3.4 INVESTIGATIONS ON BACK BIAS

Figure 3.17(a) illustrates the cross section of a LVT NMOS FD-SOI transistor. As depicted, the channel is isolated from the substrate. The absence of bulk-drain and bulk-source junction diodes enables the biasing of the body over a large voltage range from 0 to +2 V (for LVT NMOS transistor). This body biasing enables a reduction of the transistor's threshold voltage with a slope of −80 mV/V (see Figure 3.17(b)).



(a) (b)

Figure 3.17 FD-SOI technology: (a) Cross-section of a NMOS LVT FD-SOI transistor; (b) Vth versus back gate voltage for NMOS LVT.

As discussed in the previous Subsection, the limitation of the power supply reduction is due to the incorrect saturation of the transistors. Adjusting the threshold voltage of each transistor through the body biasing gives a new possibility to push further this limitation.

Two additional knobs (V_{BG_1} and V_{BG_2}) are added to the design of the LNA as illustrated in Figure 3.18. This enables new biasing configurations to reach the targeted ($gm1, gm2$), and thus to exhibit the targeted performances.

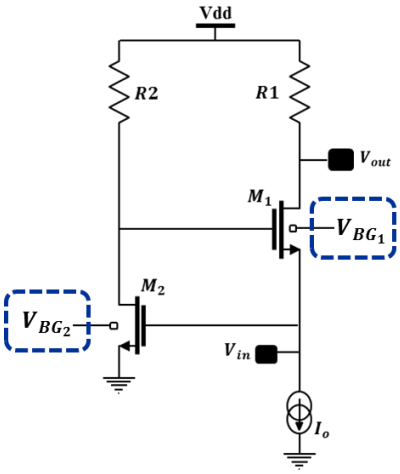


Figure 3.18 Common Gate gm-boost LNA with body biasing tuning knobs.

New solutions with a lower power supply are reached with the body biasing as depicted in Figure 3.19.

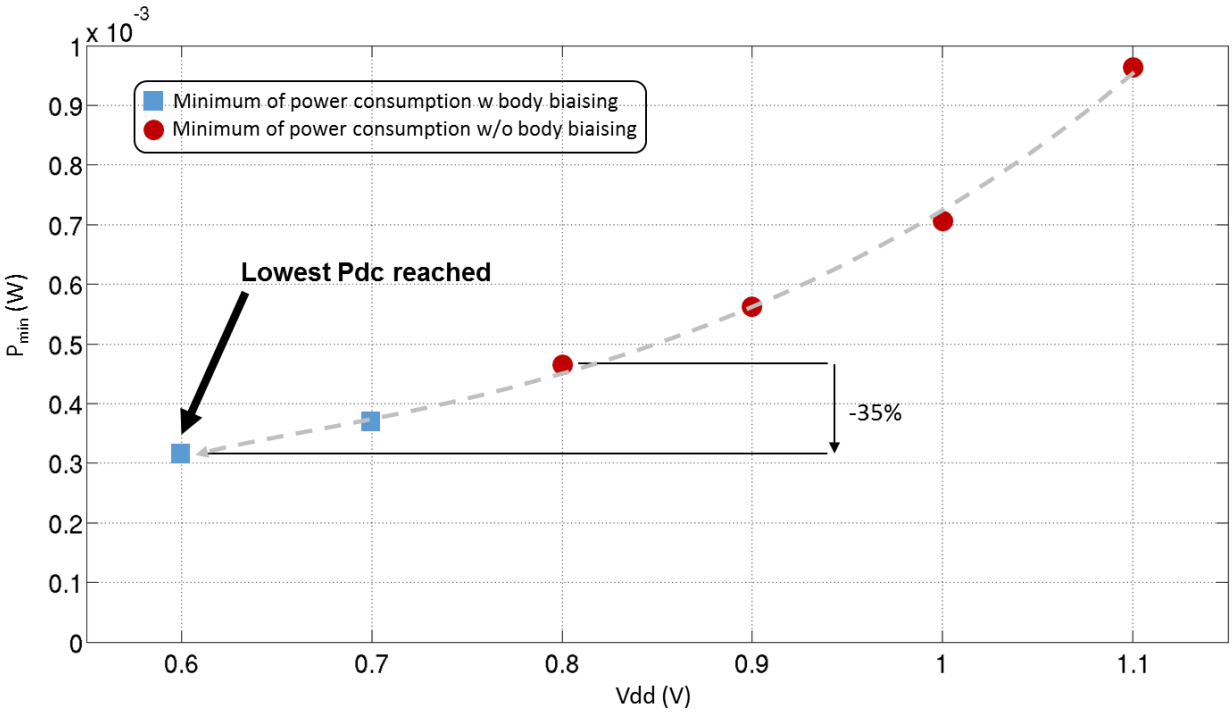
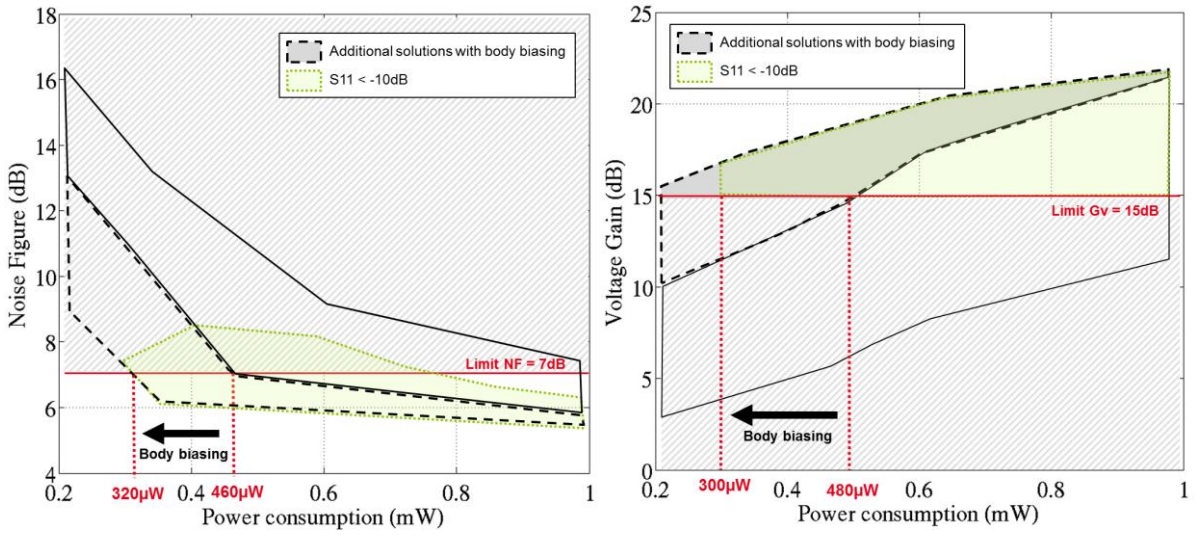


Figure 3.19 Minimum of power consumption for each power supply Vdd with and without body biasing which respects the conditions Noise Figure < 7dB and Gain > 15 dB.

With the body biasing, the power supply can be reduced to 0.6 V with -35% on the overall power consumption of the LNA while maintaining the targeted performances.

The effect of the body biasing on the performances of the LNA is illustrated by Figure 3.20.



(a) (b)

Figure 3.20 Minimum of power consumption with body biasing to guarantee: (a) Noise Figure < 7 dB and (b) Gain > 15 dB.

Comparing the design possibilities with and without body biasing of this topology, several observations have to be noticed:

- At a constant power consumption, the back gate offers an extended design space compared to the body tied configuration. For instance, at 500 µW, the maximum voltage gain reached is 15 dB without using the body biasing. By tuning the back gate, the voltage gain is increased and reaches more than 18 dB;

- For large supply voltage ($Vdd \geq 1$V), the body biasing does not achieve significant improvements in terms of gain, noise and power consumption;

- At constant noise figure or gain, the power consumption can be reduced with body biasing. For instance, targeting 15 dB of voltage gain can be reached with 35 % less of power consumption by using the body biasing.

As this Chapter addresses the design of a power-optimized LNA, the minimum of power supply which fulfils the targeted performances is implemented.

3.5 INTEGRATED CIRCUIT (IC) IMPLEMENTATION AND MEASUREMENT RESULTS

The ULP LNA circuit has been implemented in UTBB FD-SOI 28 nm ST-Microelectronics technology. Figure 3.21 shows the die micrograph and the layout view of the chip.

The complete chip presents an area of 0.5 mm² and the LNA core is only 0.0015 mm². The ULP LNA is followed by a buffer only added for test facilities (output matching). The S-parameters and characteristics of this buffer are de-embedded from the proposed measurement.

The back gate voltages are externally controlled (0V or +2V). The implementation of a complete chip in FD-SOI technology will need a back bias generator which is able to provide this voltage for the lowest power consumption and high efficiency as proposed in [50] for instance.

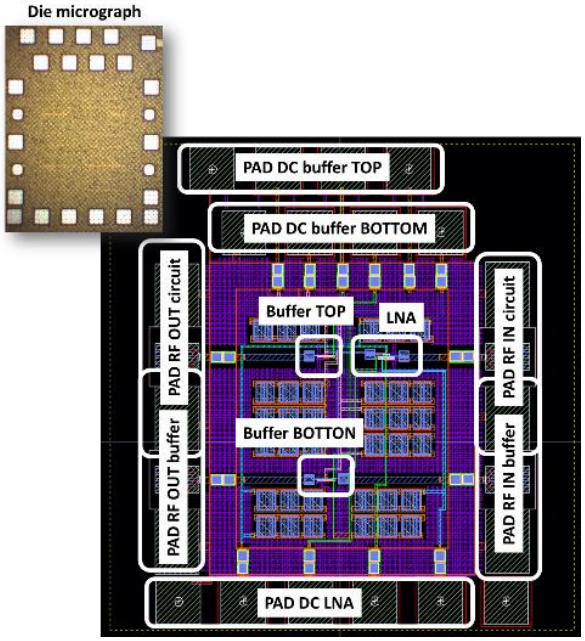


Figure 3.21 Layout view of the chip and die micrograph.

The measurement results of the voltage gain (Gv), the noise figure (NF), and the input matching ($S11$) for the optimized ULP mode are plotted in Figure 3.22. The proposed LNA achieves, at 2.4 GHz, a 16.8 dB voltage gain and a 7.3 dB noise figure for a power consumption of 300 µW under 0.6 V of power supply. Such performances are not achievable without the use of the back biasing (in this case +2 V on both transistors). This measurement set validates the benefits of the FD-SOI technology to decrease the power consumption of a block.

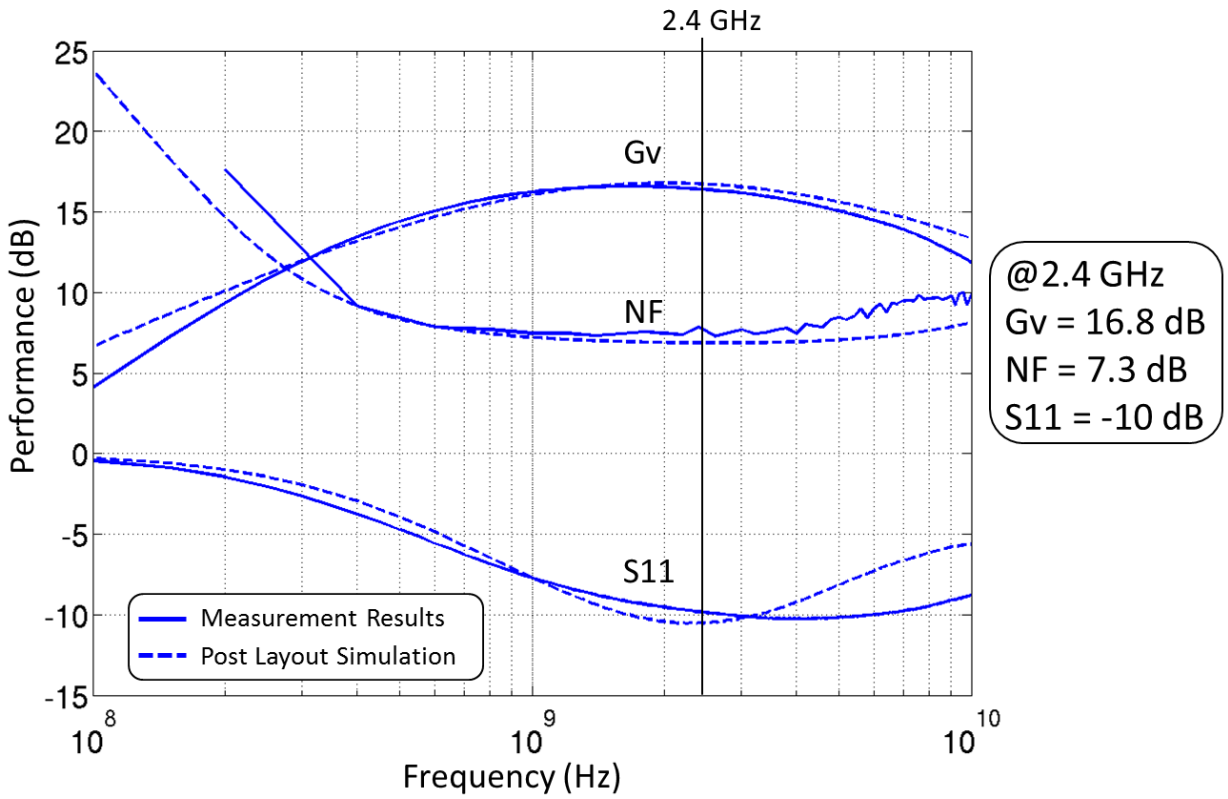


Figure 3.22 Gain, noise figure and input matching measurements results of the proposed ULP LNA.

The 1-dB Compression Point (P1dB) and the 3rd order Input Intermodulation Point (IIP3) have been measured by varying the input power from -40 dBm to 10 dBm. Two RF tones (f_1=2.42 GHz and f_2= 2.44 GHz) have been introduced to determine the IIP3 by Equation (3.15) [7]. The measurement screenshot is depicted in Figure 3.23.

$$IIP3_{dBm} = \frac{\Delta P_{dB}}{2} + Pin_{dBm} \tag{3.15}$$

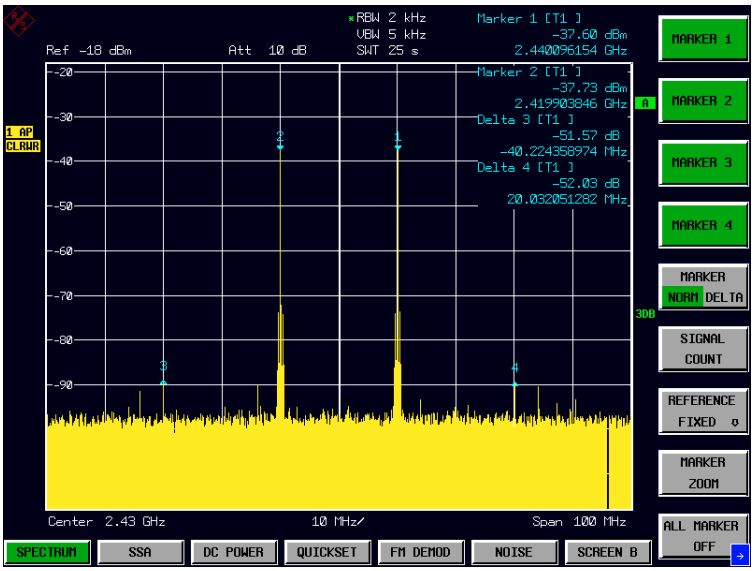


Figure 3.23 IIP3 measurement result of the ULP LNA.

The input power for this measurement is -42 dBm. ΔP_{dB} is the difference of magnitudes between the fundamental and the 3rd order Intermodulation ($IM3$) product.

Using Equation (3.15), the measured IIP3 of the LNA is -16 dBm.

Performances of the LNA are summarized and compared with the State Of the Art ULP LNAs in Table 3.2. In order to compare the circuits, two FoMs: FoM_I and FoM_{II} are used and defined in Equations (3.16) and (3.17) respectively.

$$FoM_I = 20\,log\left(\frac{Gv_{lin}.BW_{GHz}}{Pdc_{mW}.(F_{lin}-1)}\right). \quad (3.16)$$

$$FoM_{II} = 20\,log\left(\frac{Gv_{lin}.BW_{GHz}.IIP3_{mW}}{Pdc_{mW}.(F_{lin}-1).A_{mm^2}}\right). \quad (3.17)$$

Where BW is the bandwidth in GHz, Gv is the voltage gain in linear, Pdc is the power consumption in mW, F is the noise figure, $IIP3$ is the 3rd order Input Intermodulation Point in mW and A is the area in mm² of the LNA.

The proposed LNA achieves a very low power consumption with comparable State Of the Art LNAs performances, leading to highest FoM_I and FoM_{II} as depicted in Figure 3.24.

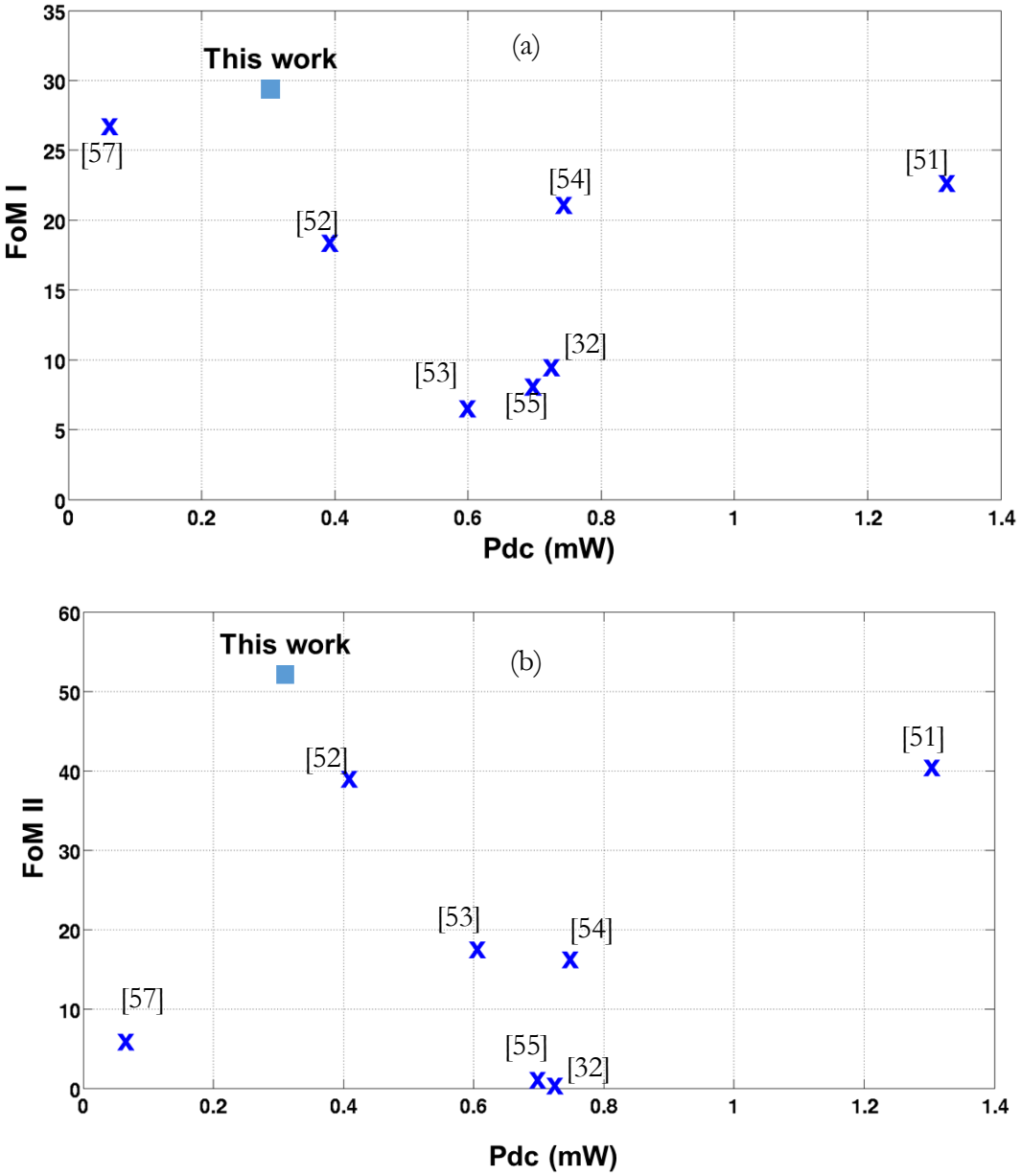


Figure 3.24 Comparison of the proposed LNA with the State Of the Art LNAs: (a) Figure of Merit I (FoM I) versus the power consumption and (b) FoM II versus the power consumption.

Results and State of the Art LNAs performances are summed up in Table 3.2.

Ref.	Gv (dB)	3 dB-BW (GHz)	NF (dB)	IIP3 (dBm)	Pdc (mW)	Supply (V)	Tech.	Area (mm^2)	FoM 1	FoM 2
T.W.	**16.8**	**0.45–6**	**7.3**	**−16**	**0.3**	**0.6**	**FD-SOI 28 nm**	**0.0015**	**29.3**	**53.7**
[51]	20	0.1–2.7	4	−12	1.32	1.2	CMOS 0.13 μm	0.007	22.3	41.4
[53]	14.7	2.1–2.5	4.8	2	0.6	1.8	CMOS 0.18 μm	0.39	7	19.2
[54]	12.6	0.1–7	6.5	−8	0.75	0.5	CMOS 90 nm	0.23	21.1	17.8
[32]	10.6 [1]	0.1–1	4	−10.2	0.72	1.2	CMOS 0.13 μm	0.26	8.9	0.3
[52]	9.9 [1]	0.1–2.2	5.5	−11.5	0.4	1	CMOS 0.1 μm	0.0052	16.7	39.4
[55]	9.7	2–2.8	4.4	−4	0.7	1.2	CMOS 90 nm	0.91	7.9	0.8
[57]	13[1]	1.5-2.4	5.3	-12.2	0.06	0.4	CMOS 0.13 μm	0.63	26.3	5.9

[1] Gv(dB) = 20.log(S21(mag)/(S11(mag) + 1).

Table 3.2 Comparison of the proposed LNA with the State of The Art LNAs.

The proposed LNA in its three operating mode achieves overall better performances than the state of the Art of LNAs, leading to highest FoM.

As depicted in Figure 3.24, the final FoM of the proposed ULP LNA is better than the State of the Art of LNAs for a lower power consumption. The use of the advanced node FD-SOI 28 nm technology, which presents a higher cutoff frequency but also better gain for lower drain current of a transistor is part of the good measurement results. Moreover, the reduction of the power supply to 0.6V could not have been possible without the threshold voltage modulation thanks to the body biasing.

3.6 DESIGN OF AN ULP LNA USING FD-SOI BODY BIASING: SUMMARY

This Chapter concentrates on the design of an inductorless LNA which can address the low power mode performances established in Chapter 2. First, a State of the Art of the inductorless ULP LNAs and techniques to improve the performances is presented. Common Gate with gm-boost technique is defined as a relevant solution to address the design of a sub-milliWatt LNA at 2.4GHz. An analytical description of the circuit behavior is then proposed to find the optimal design point (lowest power consumption) which yields the targeted specifications. This Chapter also emphasizes the limitations of the topology when the power supply is reduced. A new possibility to decrease the power supply by tuning the back gate voltages of FD-SOI transistors is demonstrated.

The final measurements confirm the possibility to use the body biasing of FD-SOI transistors to decrease the power supply and thus to reduce the power consumption of the circuit. It makes the FD-SOI technology a suited candidate for Ultra Low Voltage (ULV) and ULP designs.

The ULP LNA proposed in this Chapter is only optimized for one mode: the low power operation. The next Chapter investigates the possibility to use the FD-SOI technology to implement tunability in the proposed LNA.

CHAPTER 4

DESIGN OF A TUNABLE LNA WITH FD-SOI BACK GATE TUNING: CIRCUIT-LEVEL ANALYSIS

In the previous Chapter, the design of an inductorless Ultra Low Power (ULP) Low Noise Amplifier (LNA) is proposed. It demonstrates the possibility to use the body biasing of Fully Depleted Silicon-On-Insulator (FD-SOI) technology to decrease the power consumption of the circuit. The proposed ULP LNA fulfils the specifications of the low power mode defined previously in the system analysis of Chapter 2. However, this LNA is not able to provide the correct requirements for the other operating modes. Therefore, the final purpose is to design an adaptive LNA which is optimized for the three operating modes of the channel aware receiver.

In this Chapter, the possibility to use the body biasing of Ultra-Thin Body and Buried oxide (UTBB) FD-SOI technology to perform tunability in the proposed LNA is investigated.

The first Section of this Chapter presents the State of the Art of tunable LNA techniques. Then, the ULP LNA of Chapter 3 is modified in order to address the performances for the 3 modes of operation with an optimized Figure of Merit (FoM). To do so, the back gate voltage of the FD-SOI technology is exploited in order to tune the circuit by changing the region of operation of the transistors. The proposed width-scaling via body biasing technique is compared with different techniques of reconfiguration proposed in the literature. Finally, the Integrated Circuit (IC) measurements are presented in the last Section and a comparison with the LNAs of the literature is proposed.

4.1 STATE OF THE ART OF TECHNIQUES TO ADD TUNABILITY IN LNAS

Reconfigurable LNAs have been widely considered in the literature. Only the techniques relevant to our context of application are reported and discussed in this Section.

First, the biasing tuning consists in changing the power supply and/or current biasing in order to reach the performances. Then, the gain of a LNA can be tuned by changing its load. Finally, switches can be added to a topology to control the widths and the current flowing into the transistors.

In order to compare the LNA performances and the tuning capability, a Figure of Merit (FoM) is defined in Equation (4.1).

$$FoM = \frac{Gv_{lin}.BW_{GHz}}{Pdc_{mW}.(F_{lin}-1)}. \quad (4.1)$$

Where BW is the bandwidth in GHz, Gv is the voltage gain in linear, Pdc is the power consumption in mW and F is the noise figure of the LNA.

A LNA is considered as optimized when a maximum of FoM is reached.

4.1.1 BIASING SCALING TUNING

In the biasing scaling tuning technique, the tunability is achieved by changing the current (through modification of biasing) or the voltage (power supply). This method offers two possibilities:

- Increase the bias: the circuit is first optimized for low power mode, the current and/or voltage is increased in order to improve the performances (which consequently increases the power consumption).

- Decrease the bias: the circuit is first optimized for high performance mode, the current and/or voltage is decreased in order to lower the power consumption (which consequently degrades the performances).

These two possibilities are now further investigated, and compared with a selected LNA of the State of the Art.

INCREASE BIAS TECHNIQUE

This method has been realized on the optimized ULP LNA proposed in Chapter 3. The purpose is to cover a range of performances by tuning the current of the circuit. The measurements are done at fixed geometries optimized for the low power mode.

To boost the performances and to address the requirements of medium and high performance modes, the power supply Vdd, the current biasing I_o and the back gate voltages V_{BG} are adjusted. These four tuning knobs are tuned to achieve the best configurations for each operating mode.

Figure 4.1 depicts the tunable LNA based on the ULP LNA described in Chapter 3.

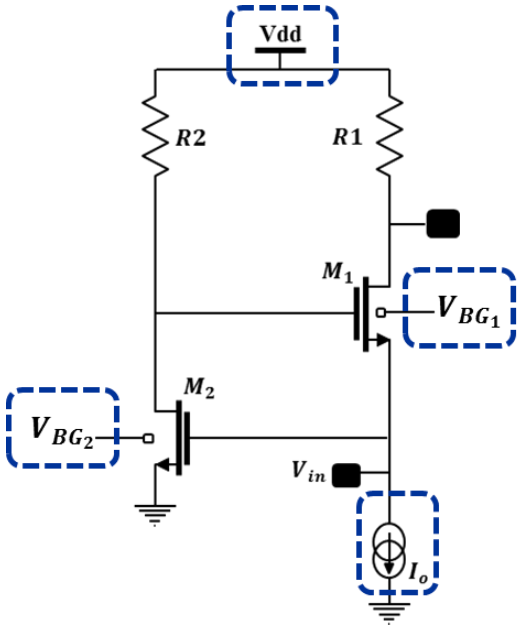


Figure 4.1 Reconfigurable LNA based on bias tuning technique [56].

The measurement results of this circuit, based on previous work [56], are reported in Table 4.1 for the three targeted modes of operation.

Mode	Low power mode	Medium performances mode	High performances mode
Gain (dB)	16.8	18.8	21.5
Noise Figure (dB)	7.3	6.7	6.3
Supply Voltage (V)	0.6	0.8	1
Back Gate Voltage (V)	2	1	0
Power Consumption (mW)	0.3	0.6	0.9
FoM 1	**26.4**	19.7	20.2

OPTIMIZED MODE

Table 4.1 Performances of the tunable LNA in [56].

The tuning range is very limited as the geometries of the transistors are fixed to operate in the low power mode performance, and struggle in steering large drain current. The optimal FoM, 26.4, is of course reached in the low power mode. FoM in the high performance mode, 20.2, is degraded by 23%.

The same technique can be realized in reverse approach, by optimizing a high performance mode and decreasing the biasing to reduce the power consumption. Next Subsection presents a tunable LNA of the State of the Art which offers several operating modes using this technique.

DECREASE BIAS TECHNIQUE

The decrease of the bias consists in an optimization of the high performance mode and offers other operating modes by decreasing the power consumption. This can be done by tuning the power supply voltage of the LNA as presented in [57], [58] and [59]. Some of this reconfigurable LNAs have been realized by adding, for instance, a Digital-to-Analog Converter (DAC) on the power supply as shown in Figure 4.2.

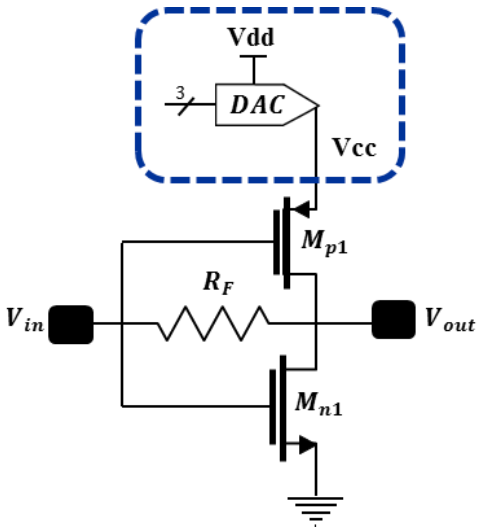


Figure 4.2 Reconfigurable LNA based on power supply tuning technique [57].

This technique enables a digital variation of the power supply, here Vcc, and thus discrete values of the current consumption.

The results are presented in Table 4.2. A significant power reduction is obtained by decreasing the supply voltage, the power consumption is only 30uW in low power mode.

Mode	Low power mode	Medium performances mode	High performances mode
Gain (dB)	9.4	12	14.6
Noise Figure (dB)	6.2	4.4	3.8
Supply Voltage (V)	0.3	0.4	0.6
Power Consumption (mW)	0.03	0.06	0.13
FoM 1	31	50.4	**59.1**

OPTIMIZED MODE

Table 4.2 Performances of the tunable LNA in [57].

As for the increase of the bias, discussed in the previous Section, only one mode of operation can reach a maximum of FoM. The other modes, where the voltage supply is decreased, are suffering from this lower supply voltage. The FoM of low power mode is degraded by 47% compared to the optimized high performances mode. The sizes of transistors and passive elements are not suited for this mode.

This method has also been proposed in [60] where the authors propose a reconfigurable LNA in which the performances can be orthogonally modified, Figure 4.3.

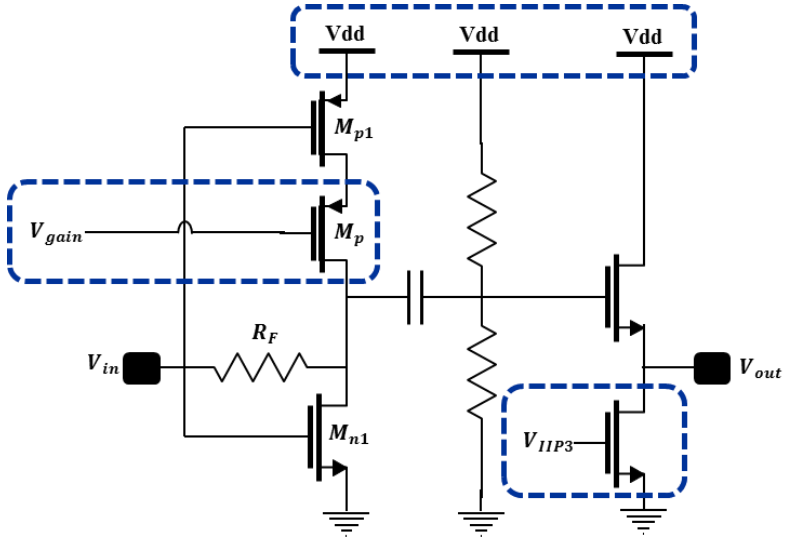


Figure 4.3 Reconfigurable LNA based on bias technique [60].

The performances are degraded by an decrease of the power supply Vdd along with the gate voltages V_{gain} and V_{IIP3}. The reached performances of three modes are presented in Table 4.3.

Mode	Low power mode	Medium performances mode	High performances mode
Gain (dB)	8	11	13
Noise Figure (dB)	5.5	4.3	3.8
Supply Voltage (V)	1	1.4	1.8
V_{gain} (V)	0	0.8	1.3
Power Consumption (mW)	9.6	13	18
FoM 1	**0.1**	**0.8**	**0.9**

Table 4.3 Performances of the tunable LNA in [60].

The reached FoM of this LNA is lower than the FoM obtain with a non-modified current reused topology as, for instance, the current reused LNA presented in [57] , Table 4.2.

With this technique, the added tuning knobs degrade the initial performances of the LNA. In fact, a higher power supply is needed because of the added stacked transistors. Without these additional knobs, the topology offers better performances with fixed structures.

4.1.2 LOAD TUNING

The load tuning consists in an adjustment of the load of the LNA with the bias in order to offer several performances. The authors in [36] propose a shunt-shunt feedback amplifier with low-noise abilities upon 50 Ω input matching. The LNA is made from a cascode amplifier stage and an active feedback stage.

Figure 4.4 illustrates the reconfigurable LNA based on the load tuning proposed in [36].

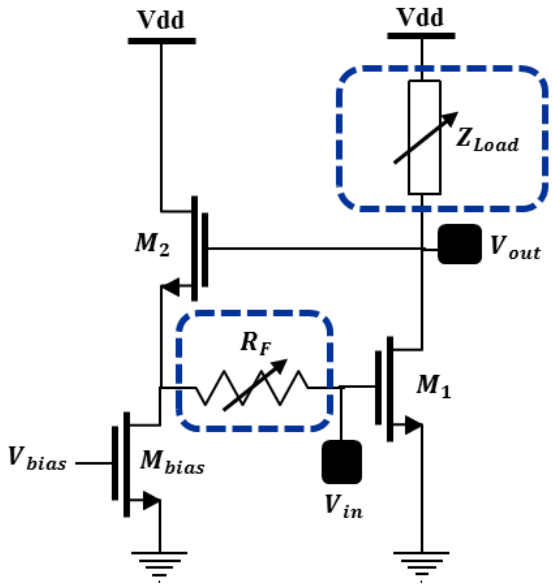


Figure 4.4 Reconfigurable LNA based on load tuning technique [36].

The load and the feedback resistance are tuned to propose several operating points. The reached performances of three operating modes are presented in Table 4.4.

Mode	Inductive Load Mode	Resistive Load Mode R_F=100Ω	Resistive Load Mode R_F=0Ω
Gain (dB)	20.8	16.5	16.5
Noise Figure (dB)	2.2	2.7	2.5
Supply Voltage (V)	1.2	1.2	1.2
Power Consumption (mW)	3.8	9.7	9.2
FoM 1	**26.3**	**5.2**	**6.1**

Table 4.4 Performances of the tunable LNA in [36].

This technique is at the expense of optimized performances, which are better at fixed load, here with inductive load. Tuning the value of the load and/or the feedback resistance demands switching techniques which degrade the overall performances.

For instance, a tunable gain LNA with load tuning, proposed in [61], is achieved by adjusting the load with active CMOS resistances. The feedback resistance is also tuned in order to maintain the correct input impedance in each operating mode. However, the implementation of the active CMOS resistances degrades the noise figure of the LNA compared to a structure with fixed resistances. An active inductor tunable load is also presented in [62] with overall good performances but it offers a low range of tunability (only 2 dB on the gain and 0.2 dB on the noise figure of the LNA).

4.1.3 TRANSISTORS SWITCHES TUNING

Another possibility to design reconfigurable LNAs is to scale the transistor size with a switching approach. The structure proposed in [63] offers several operating modes obtained by duplicating the main active transistor with stacked switch transistors above. This work also uses the biasing tuning technique since it decreases the voltage supply of the structure.

This tunable LNA is depicted in Figure 4.5.

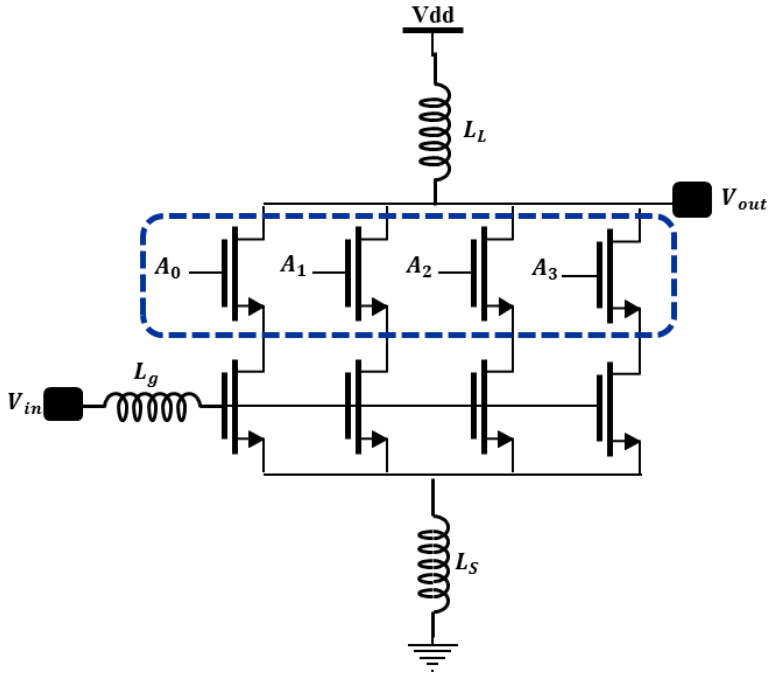


Figure 4.5 Reconfigurable LNA based on width scaling technique [63].

This technique, also called width-scaling, enables a variation of the width and the biasing of the input active transistor. The initial topology is an inductively degenerated common source and the equivalent width of the input transistor is 4-bit binary weighted controlled by the switches A0-A3. The maximum width of the input transistor (all switches A0 to A3 are ON) is optimal for the minimum of noise figure. It is also the most power hungry mode. When the power supply and the widths of transistors (switches A1 to A3 OFF) are reduced, the performances are therefore degraded.

Table 4.5 presents the results of the extreme modes of the tunable LNA described in [63].

Mode	Low power mode	High performances mode
Gain (dB)	14	26
Noise Figure (dB)	7.5	4
Supply Voltage (V)	0.8	1.2
$\boldsymbol{A_0A_1A_2A_3}$	1000	1111
Power Consumption (mW)	0.3	2.1
FoM 1	**21.6**	**25.1**

Table 4.5 Performances of the tunable LNA in [63].

This technique is well suited for the design of reconfigurable LNA offering several operating modes. The widths of the transistors can be adjusted to the drain current. With this technique, the degradation of the FoM between the low power and the high performances modes is only 14%.

Nevertheless, this technique requires stacked switches transistors which limits the output dynamic and limits the possibility to decrease the power supply voltage. Moreover, as in the tuning load, the original inductive degeneration structure would probably offers better performances without the modifications (additional stacked transistors).

The width-scaling technique is also used in [64] where the authors also propose a mix of the two methods for the design of a reconfigurable LNA. The current source biasing of the feedback stage is width-scaled and the power supply is tuned by a DAC in order to offer several operating modes.

4.1.4 STATE OF THE ART OF TUNABLE LNAS: CONCLUSION

Based on the analysis of the State of the Art of tunable LNAs, three approaches have been discussed.

First, the bias tuning can achieve a maximum FoM for an operating mode but degrades the performances in the other modes.

Then, the load tuning technique enables a variation of the gain of the LNA but the added tunability degrades the initial performances of the structure without varying load.

Finally, a combined approach embedding the scaling of the transistor size and the tuning of the bias allows for an optimum set of performance in each mode of operation accounting for the loss induced by the switches. However, this technique needs additional stacked transistors which limits the power supply reduction and degrades the initial performances of the structure excluding the switches.

This Chapter focusses on an architecture of LNA which keeps constant, and maximum, the FoM for each targeted mode of operation. The design issues of such LNAs are:

- To respects the target performances (established in Chapter 2) for each mode;
- To challenge the performance of the original (non -modified) topology;
- To achieve a maximum FoM in each mode of operation

The following Section describes the adopted strategy to optimize all the operating modes of a tunable LNA with the use of the FD-SOI technology.

4.2 PROPOSED TUNABLE LNA DESIGN

First, the design guide allowing the best configuration of transistor size, current density and transconductance to address the targeted specifications is proposed. Then, a specific use of the back gate of the FD-SOI transistors to switch the region of operation of the transistors in order to add tunability to the LNA is demonstrated. Finally, this Section describes the final proposed tunable LNA and it three modes of operation.

4.2.1 DESIGN FLOW

The targeted performances of the tunable LNA, Table 4.6, are based on the results of the system analysis presented in Chapter 2.

Mode	Low power mode	Medium performances mode	High performances mode
P_{min} (dBm)	-75	-85	-90
Usage time (%)	76	23	1
NF_{LNA} (dB)	7	5	3
Gv_{LNA} (dB)	15	20	25
Pdc_{LNA} (mW)	0.3	0.9	2
$IIP3_{LNA}$ (dBm)	-15	-15	-15

Table 4.6 LNA targeted design performances for each configuration.

In Chapter 3, the design of a ULP LNA which offers the required performances for low power mode is presented. The methodology for the design of the proposed tunable LNA is based on the same design flow.

More specifically the methodology first consists in the sizing of three different LNAs, each one is optimized for a mode of operation, according the parallel flow chart presented in Figure 4.6, green, blue and red paths.

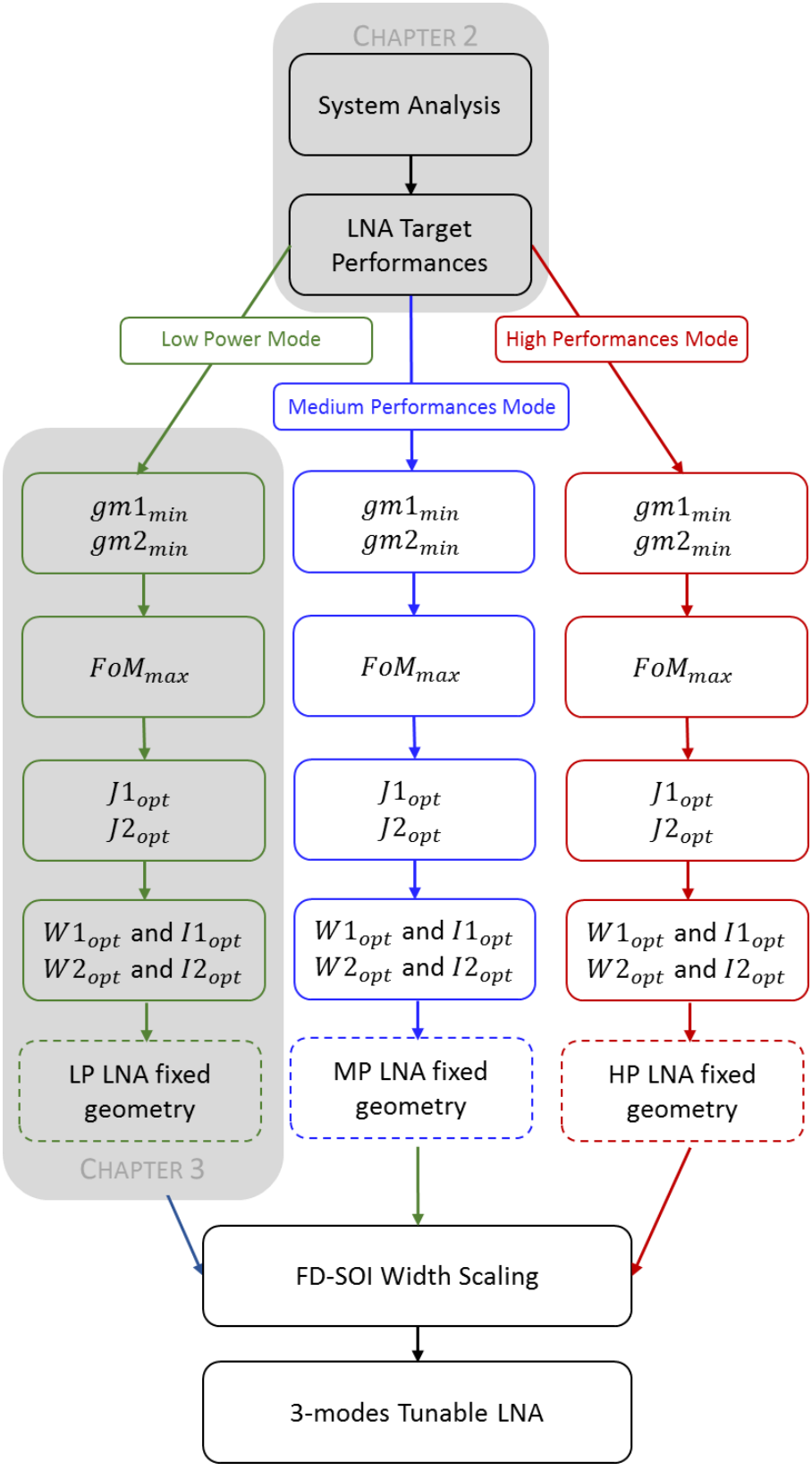


Figure 4.6 Design Flow of the proposed tunable LNA.

As for the low power LNA, the medium and high mode are designed separately in order to find the best configuration in widths and biasing of the transistors. For each mode, the minimum transconductance for transistors $M1$ and $M2$ are determined. Then, the maximum FoM_{max} and corresponding optimal current densities $J1_{opt}$ and $J2_{opt}$ are selected and appears to be equal for the three designs.

Finally, the widths and the drain current of the two active transistors are selected in order to provide the correct transconductances gm_1 and gm_2. The performances in noise figure NF_{LNA}, gain Gv_{LNA} and power consumption Pdc_{LNA} are finally checked in order to respect the specifications. For each mode, the minimum of power supply voltage which enables a correct biasing of the transistor, is chosen in order to reduce the power consumption of the LNA.

To illustrate this design flow three optimized LNA, Figure 4.7, are sized to address the three modes of operation.

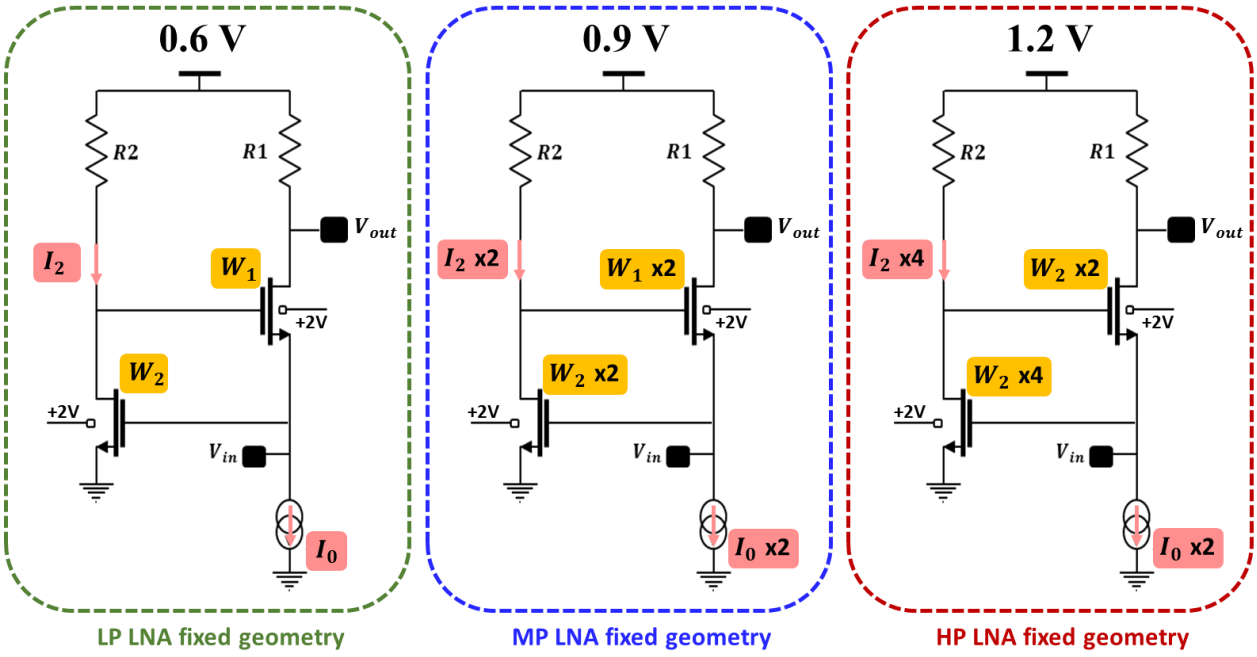


Figure 4.7 Design of three fixed geometry LNAs

Table 4.7 presents the details of the size of transistors, current and power supply for the three fixed optimized LNAs. Each of the LNA fits the target performances (available in Table 4.6) of its mode.

Fixed LNAs	Low power LNA	Medium performances LNA	High performances LNA
Vdd (V)	0.6	0.9	1.2
$\boldsymbol{I_0 = I_1}$ **(µA)**	180	360	360
$\boldsymbol{I_2}$ **(µA)**	320	640	1280
$\boldsymbol{W_1}$ **(µm)**	20	40	40
$\boldsymbol{W_2}$ **(µm)**	30	60	120
$\boldsymbol{J_1}$ **(µA/µm)**	---------- 9 ----------		
$\boldsymbol{J_2}$ **(µA/µm)**	---------- 10.7 ----------		
FoM 1	---------- MAX ----------		
$\boldsymbol{V_{BG}}$ **(V)**	---------- $V_{BG1} = +2V$ & $V_{BG2} = +2V$ ----------		

Table 4.7 Details of the three LNAs.

According Chapter 3, the design of the low power LNA is optimized to work out the best configuration of size and current for each transistor. Based on the literature ([65], [66]), there is an optimal current density for a specific architecture. This leads to the following observations on the optimization of the fixed medium and the fixed high performances LNAs.

- Back gate voltages are set to a maximum (here +2V) to reduce the supply voltage in low power mode according the investigations of Chapter 3;

- A constant current density J for the three LNAs is essential to achieve a maximum FoM in each mode of operation.

Considering these observations, the widths of transistors should be adjustable in order to keep a constant current density to stay at FoM_{max}. The next Subsection investigates on the possibility to use the body biasing of FD-SOI technology to implement an optimized 3-modes LNAs.

4.2.2 INVESTIGATION ON BACK BIAS OF FD-SOI TRANSISTORS

The back gate tuning of FD-SOI MOS transistor offers a novel, and interesting knob to change the bias conditions of a transistor. In order to understand the effect of the body biasing on a single transistor, Figure 4.8 depicts the drain current dropped versus the gate-to-source voltage for several back gate voltages.

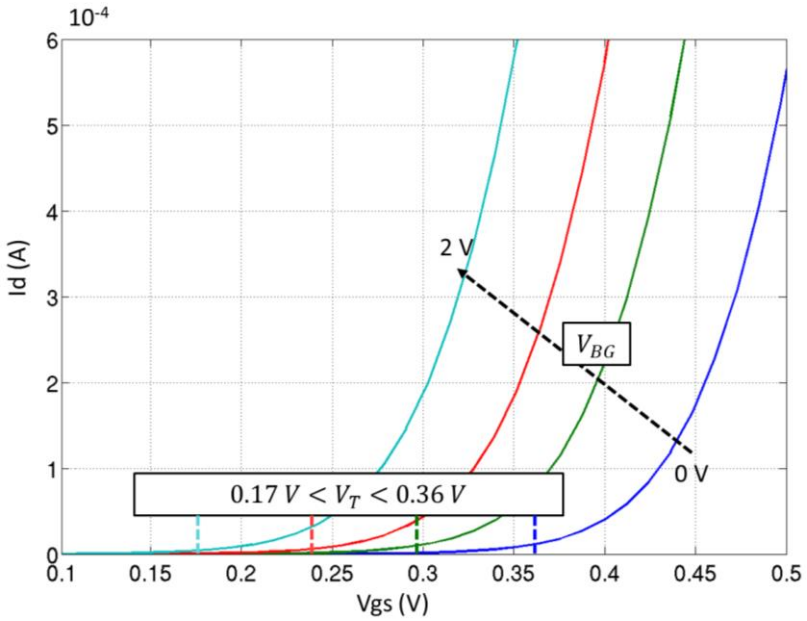


Figure 4.8 Drain current Id versus gate-to-source voltage Vgs for several back gate voltage. Simulations performed for a NLVT, W=20µm, Lmin transistor.

The threshold voltage V_{th} of the transistor decreases as the back gate voltage V_{bg} increases, jumping from the dark blue to light blue transistor characteristics.

This Subsection investigates on the possibility to keep a constant gate to source voltage V_{gs} while changing the region of operation of the transistor via its back gate voltage.

Referring to Figure 4.8, if V_{gs} is fixed to 270 mV, the transistor can be biased in strong inversion region with a back gate voltage V_{BG} of +2V (curve in light blue). For the same biasing condition, its region of operation can be changed to subthreshold (curve in dark blue) adjusting V_{bg} to 0V.

For maximizing the range of drain current reached by tuning the back gate voltage while maintaining the same V_{ds} and V_{gs}, V_{gs} has to be chosen as defined in Equation (4.2).

$$V_{gs} \approx \frac{V_{th_{MAX}} - V_{th_{MIN}}}{2} + V_{th_{MIN}} \quad (4.2)$$

Where $V_{th_{MAX}}$ is the maximum threshold voltage when the back gate voltage is at a minimum and $V_{th_{MIN}}$ is the minimum of threshold voltage when the back gate voltage is at a maximum.

The proposed idea is to use the back gate voltage to change the region of operation of active transistors in order to adjust the width of a transistor to the drain current to keep the current density constant.

The technique consists in adding a transistor in parallel of the original transistor to adjust the width of the transistor at J_{opt} as illustrated in Figure 4.9. The back gate of this additional transistor is set to a minimum (0 V). The drain current is kept to I_1 flowing into W_1. To boost the performances of the equivalent transistor, the back gate is set to +2 V. In this case, the total width is $2.W_1$ with a current of $2.I_2$.

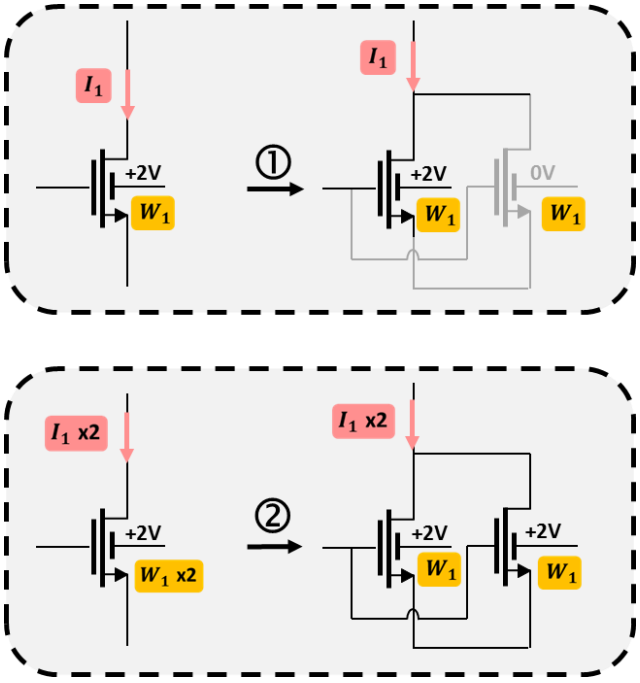


Figure 4.9 Effects of the back gate voltage.

If transformations ① and ② can be achieved, it means that it is possible to tune the LNA into three modes by adjusting the back gate voltage of parallel transistors.

The next Sections investigate whether these transformations are possible and the limitation of this technique.

4.2.3 PROPOSED TECHNIQUE FOR RECONFIGURABLE LNA DESIGN

The proposed tunable LNA is based on the same topology of the three fixed LNAs. The active transistors are implemented with parallel transistors in order to reach the optimized width of the fixed geometries LNAs.

As illustrated in Figure 4.7, the optimized high performances LNA with fixed geometry that reaches the targeted performances needs a double width of M_1 and a W_2 multiplied by 4. Therefore, one transistor is added in parallel of M_1 and four transistors are added in parallel of M_2.

In the proposed reconfigurable LNA, each mode has its unique ideal back gate configuration which enables the LNA to provide the targeted performances. The 3-modes are now described and their operating points are detailed.

LOW POWER (LP) MODE

This mode is illustrated in Figure 4.10. In this operating state, the LNA can be compared to the ULP LNA presented in Chapter 3. Only two transistors (M_{11} and M_{21}) are in strong inversion. Their back gate voltages are at a maximum (+2 V) in order to decrease the threshold voltage. All the threshold voltages of other transistors are at a minimum (V_{BG}=0V) for minimizing their contribution on the performances of the LNA. Therefore, M_{12} and $M_{22}$to M_{24} are in subthreshold regions.

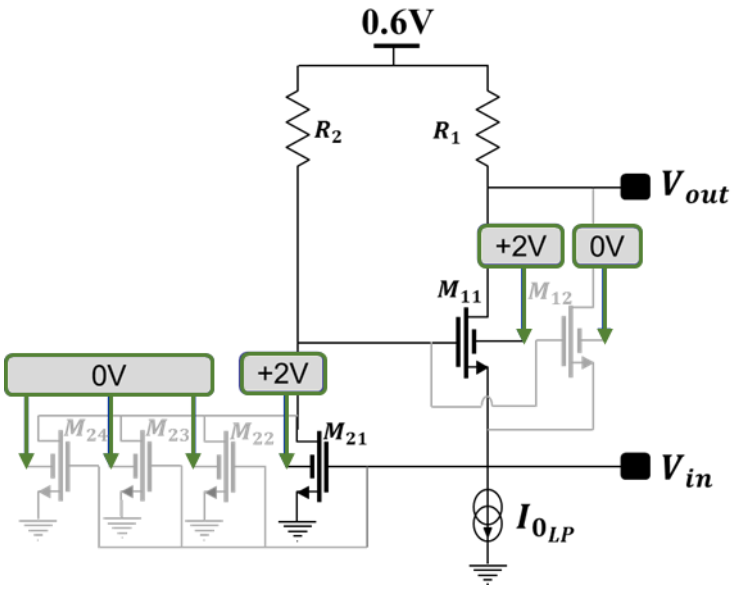


Figure 4.10 Proposed reconfigurable FD-SOI LNA in its low power mode.

MEDIUM PERFORMANCES (MP) MODE

In the medium mode configuration, depicted in Figure 4.11, the LNA fulfils the medium performances requirements. Four transistors (M_{11} M_{12} and $M_{21}M_{22}$) are in strong inversion. As for the fixed MP LNA, the drain currents and the widths of the equivalent M_1 and M_2 are doubled.

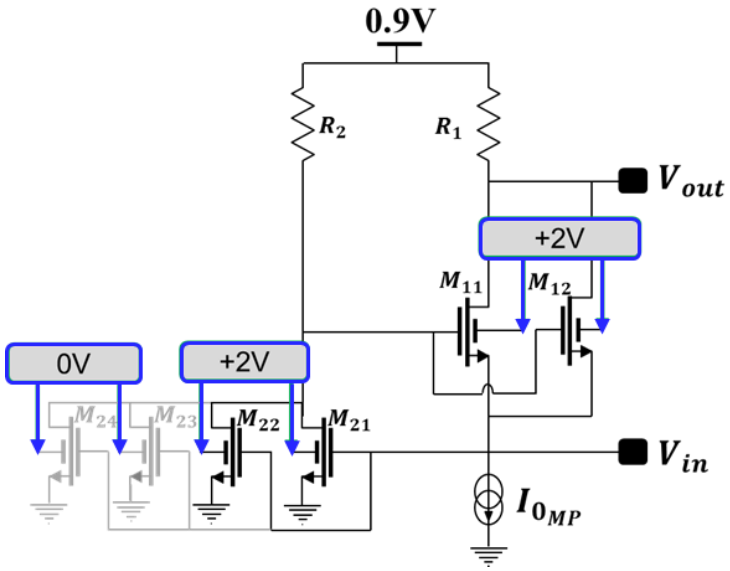


Figure 4.11 Proposed reconfigurable FD-SOI LNA in its medium performances mode.

HIGH PERFORMANCES (HP) MODE

The high performances mode, detailed in Figure 4.12, is the most power hungry as all the transistors are in strong inversion. The power supply and the current biasing are tuned to reach the targeted performances. It corresponds to the HP LNA with fixed geometry. This mode can be compared to the multifingering technique where the transistors are usually split into several fingers in order to optimized the noise figure of a transistor as described in [67].

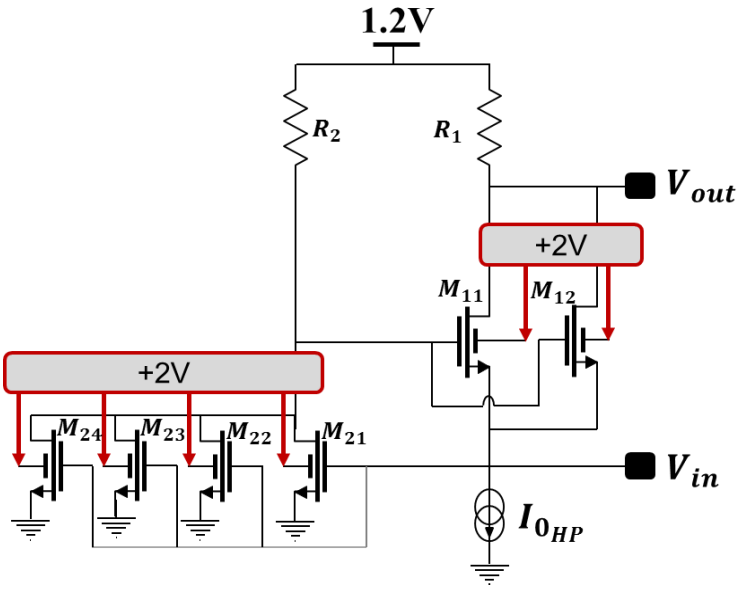


Figure 4.12 Proposed reconfigurable FD-SOI LNA in its high performances mode.

The proposed technique for switching the region of operation of the transistor embroils additional parasitic elements.

The next Section proposes an evaluation of the advantages and limitations of this adaptive method and compare the performances with the other techniques used to tune LNAs.

4.3 EFFICIENCY EVALUATION OF THE PROPOSED TECHNIQUE

The purpose of this Section is to evaluate the advantages and the limitations of the proposed technique. It exposes the different solutions to face the parasitic elements brought by the switch via back gate tuning. The technique is also compared with the bias tuning and the width scaling tuning techniques.

4.3.1 ADVANTAGES & LIMITATIONS OF THE PROPOSED TECHNIQUE

ADVANTAGES

The main advantage of this technique is the optimization of performances in all the operating mode. The degradation of the initial topology is limited compared to the width scaling method because there is no need of additional stacked switches transistors with the proposed technique. Therefore, the power supply can be decreased to the minimum allowed by the core of the LNA.

An optimized 3-in-1 LNA becomes feasible without any additional switching device.

Although the technique with additional transistors in parallel does not have any negative impact in high performance mode, it degrades the performances in medium and low power modes.

Still these auxiliary transistors bring two important limitations on the final performances of the LNA.

LIMITATION N°1: shift of the current density

As detailed on the design methodology, the current density of the transistor has to be constant to maximize the FoM of the LNA. This means that the additional transistor in subthreshold region should not impact the current density of the transistor in strong inversion.

Figure 4.13 presents the three possibilities to deal with the transistors in subthreshold region and their impacts on the current density.

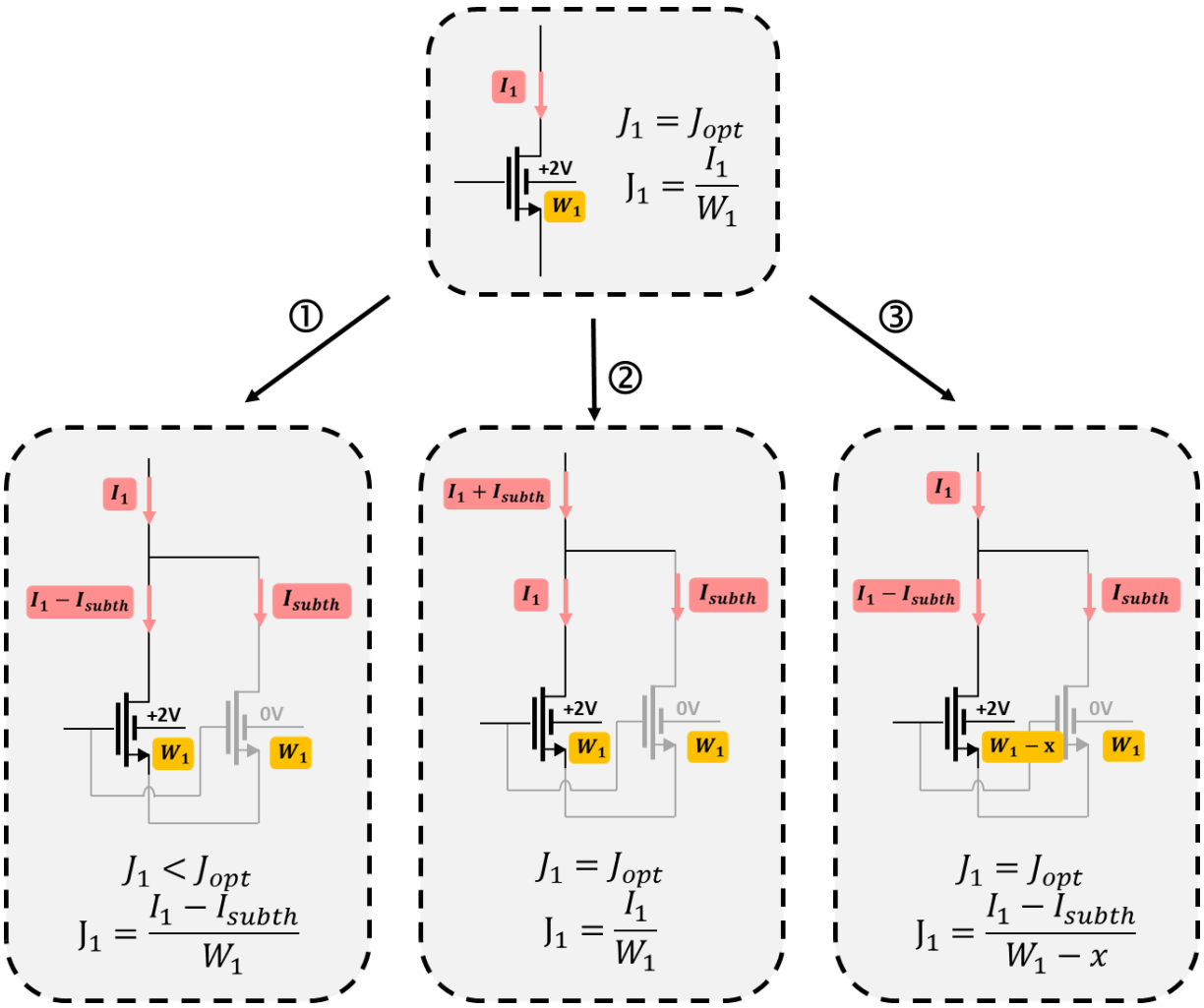


Figure 4.13 Three possibilities to compensate the effect of the subthreshold transistor.

To illustrate the purpose we want I_1 flowing into W_1 to obtain $J_1 = J_{opt}$ as depicted on the top of the figure. An additional transistor is then implemented to provide tunability. This transistor is in subthreshold region. Therefore, there is a part of the current which flows into this transistor.

Three choices to take into account this current is then possible:

- Option ①: the current I_1 is not changed which means that the transistor in strong inversion receives I_1 minus I_{subth}, the current of the subthreshold transistor. In this case, the current density J_1 of the strong inversion transistor is lower than the optimal current density targeted. The drawback of this current density shift from $J_1 = J_{opt} = 9$ to $J_1 = 8$ is the lower

transconductance gm_1. Finally, this degradation is impacting the performances of the reconfigurable LNA ($\Delta FoM = 0.5$). However, with this solution, the overall current I_1 and the power consumption of the LNA (Pdc) are kept constant.

- Option ②: the current flowing into the transistor in strong inversion is constant in order to reach the optimal current density $J_1 = J_{opt} = 9$. In this case, the targeted transconductance gm1 is preserved. However, the total current of the branch is increased by the additional current I_{subth} of the transistor in subthreshold region. The power consumption of the LNA (Pdc) is therefore increased which degrades the FoM ($\Delta FoM = 1$). Choosing this second possibility would increase the power consumption of the LNA.

- Option ③: the total current is kept constant to I_1. As the transistor in strong inversion receives a lower current due to the current absorbed by the subthreshold transistor, its width could be decreased proportionally in order to insure the optimal current density $J_1 = J_{opt} = 9$. This solution would deteriorate the performances of the high performances mode as the total width when all transistors are in strong inversion will be smaller than needed. Therefore, the correct current density in this HP mode will not be respected or the current will be decreased and the performances degraded.

This last option is not chosen because of the modification of the sizes of transistors that will impact the high performances mode. This solution is nonviable in the context of three modes LNA as it would need an adjustment of the size for the medium mode which will be different than for the low power mode.

In order to choose between the options ① and ②, an evaluation of the degradation of the FoM of the LNA is proposed.

Table 4.8 presents the variations of the performances of the transistor and the degradation of the FoM1 compares to the targeted maximum FoM.

	Option ①	Option ②
Pdc	→	↗
$\boldsymbol{J_1 / I_{M1}}$	↘	→
$\boldsymbol{gm_1}$	↘	→
$\boldsymbol{FoM_{LNA}}$	↘	↘
$\Delta FoM = \boldsymbol{FoM_{max} - FoM_{LNA}}$	0.5	1

Table 4.8 Evolution of the performances between options ① and ②.

In option ①, the degradation of the FoM in due to the lower transconductance of the transistor. On the other side, in option ②, the degradation of the FoM is due to the increase of the power consumption because of the subthreshold transistor.

The first option is chosen for the design of the proposed tunable LNA. Even if it does not propose the optimal density in M_1 and M_2 for the low power mode and in M_2 for the medium performances mode, the degradation only due to this shift of the optimal current density can be neglected. Moreover, it is the easiest solution to implement. Indeed, a self-control tunable current source on the subthreshold transistor would be needed if the option ② is chosen.

The first limitation of this technique: the shift of the optimal current density does not deteriorate significantly the targeted performances of the LNA. However, this shift is not the only disadvantage brought by the proposed switching technique. The following paragraph exposes another limitation of this technique: the impact of the parasitic capacitance on the bandwidth of the LNA.

LIMITATION N°2: degradation of the bandwidth of the LNA.

Figure 4.14 illustrates the difference on the small signal model of a single transistor in strong inversion and a subthreshold transistor in parallel of a transistor in strong inversion. Considering the same biasing conditions and the same current I_1 flowing into the transistor(s), the parasitic capacitance C_{gs} and the gate resistance R_g impact the cutoff frequency and thus, degrade the bandwidth of the LNA.

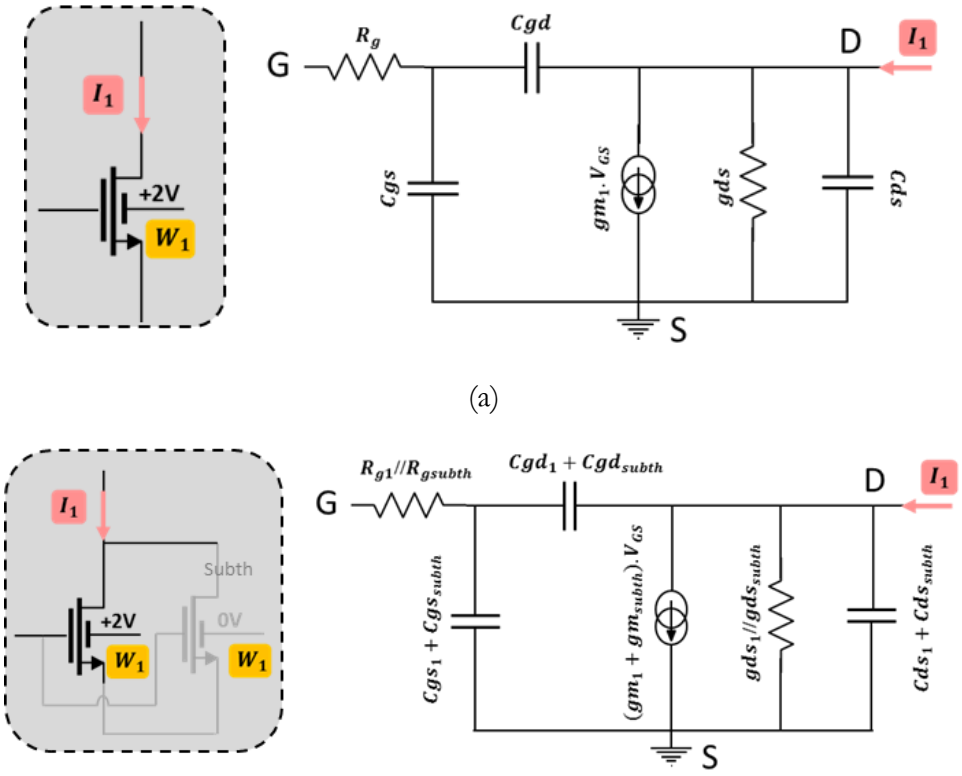


Figure 4.14 Small signal model of (a): the transistor in strong inversion alone and (b): the transistor in strong inversion with the subthreshold transistor in parallel.

In order to evaluate the additional capacitance added to the circuit by an additional transistor operating in subthreshold region, the gate-to-source capacitance is simulated for several back gate voltages. All other biasing are kept constant. Figure 4.15 depicts the simulation results on a transistor.

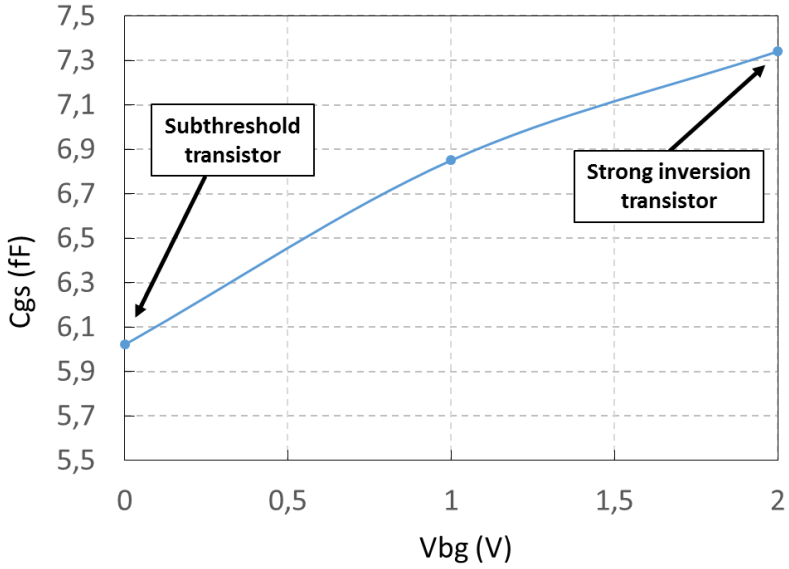


Figure 4.15 Simulation of the effect of the back gate on the gate-to-source capacitance at fixed biasing (Vds=500mV; Vgs=300mV) on a single transistor (W=20um; Lmin).

Even if the gate-to-source capacitance of a subthreshold transistor is reduced, its impact is not negligible as it comes directly in parallel to the main transistor's gate-to-source capacitance.

Figure 4.16 depicts a comparison between the gain of the tunable LNA in its low power mode with the gain of the low power LNA at fixed geometry (no subthreshold transistor in parallel).

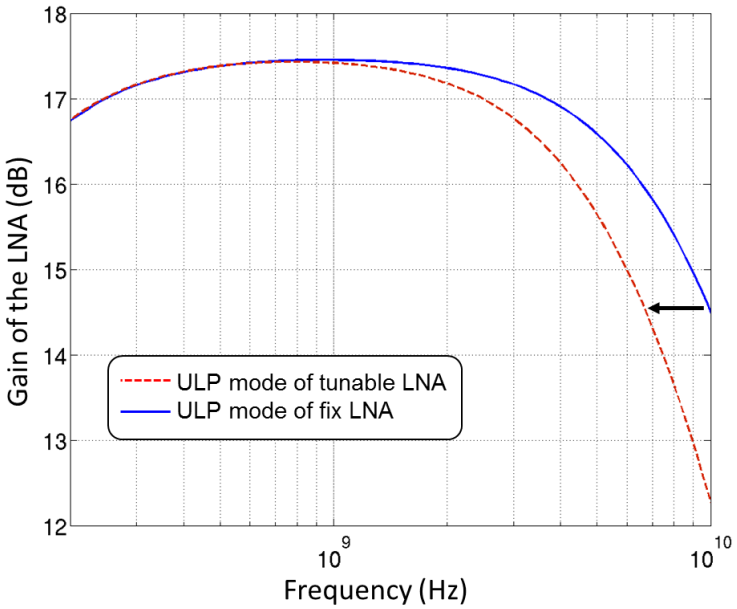


Figure 4.16 Effect of subthreshold parallel transistors on the simulated gain of the tunable LNA in low power mode.

The bandwidth of the LNA in low power mode is impacted proportionally with the number of subthreshold transistors added in parallel of the main transistor. Thus, the medium performance mode is less impacted by this parasitic element as it features only two transistors in subthreshold region.

The next Subsection compares the proposed technique of tunability with the techniques of the State of the Art of tunable LNAs presented in Section 4.1. The goal is to evaluate, for each technique, the degradation of the performances with respect to the tuning capability.

4.3.2 Comparison of the Proposed Method with Other Methods

To compare the proposed technique with the biasing scaling technique, two LNAs based on the same topology but at fixed geometries are designed and simulated.

First, the increase biasing technique is tested on the fixed low power LNA. This LNA, detailed in Chapter 3, has been optimized for the low power mode. Then, its biasing is increased (via the power supply and the current biasing) in order to boost its performances.

Then, the decrease biasing technique has been done from a fixed high performance LNA and a decrease of its biasing to lower its power consumption. Consequently, this leads to a degradation of the performances.

Figure 4.17 illustrates the input matching $S11_{LNA}$, the gain Gv_{LNA} and the noise figure NF_{LNA} of the fixed LP LNA and its degraded mode when the power consumption is increased (**Increase biasing technique**), the fixed HP LNA and its degraded mode when the power consumption is decreased (**Decrease biasing technique**) and the LP and HP modes of the proposed tunable LNA (**Proposed technique**).

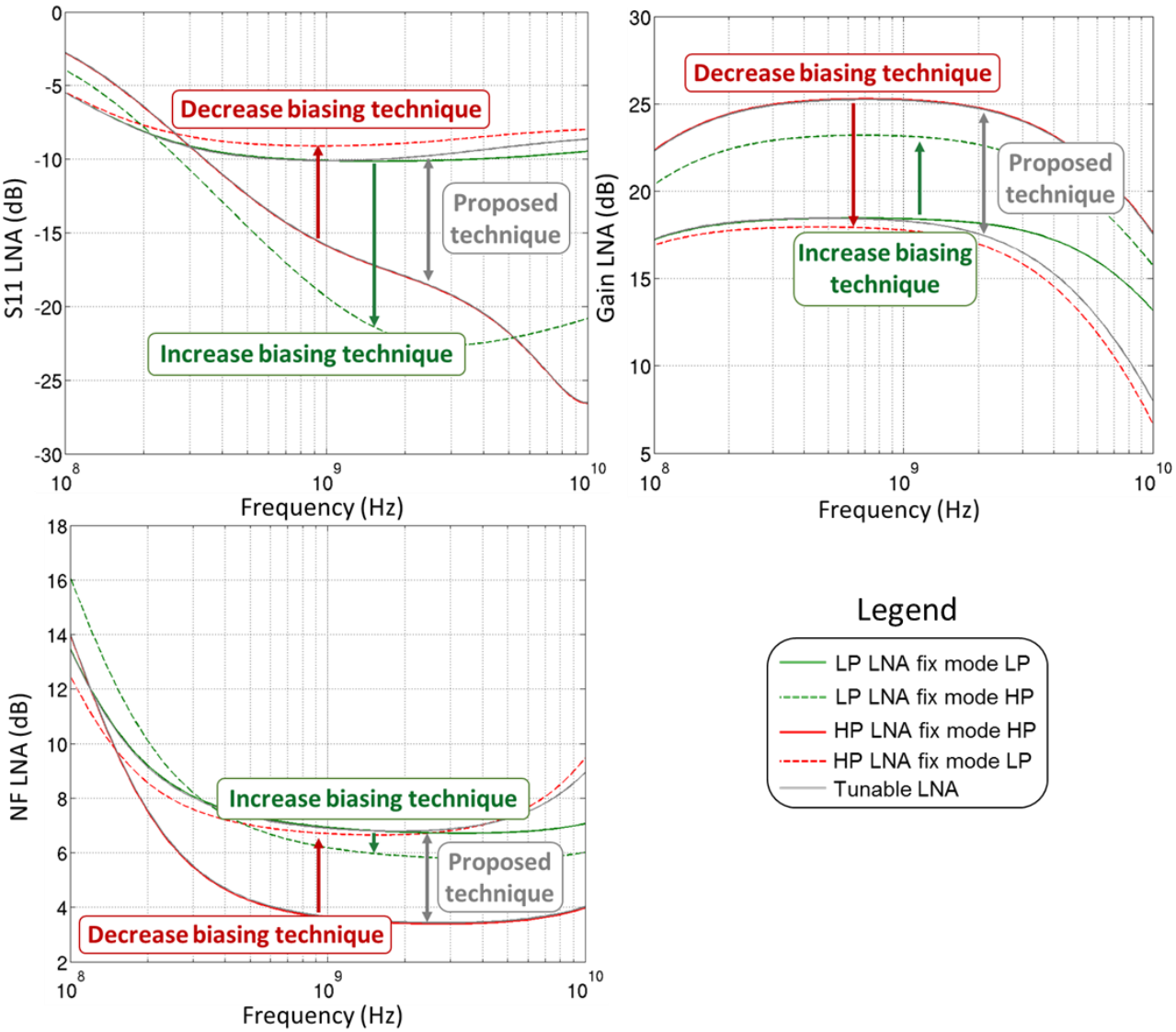


Figure 4.17 Comparison of the Noise Figure, Gain and Input Matching of the tunability methods on the CG gm-boost LNA.

The proposed method is able to reach the performances of the fixed geometry low power LNA and of the fixed geometry of the high performances LNA.

In order to compare the performances of each design in the different techniques, a FoM is defined in Equation (4.3).

$$FoM = 20\,log\left(\frac{Gv_{lin}.BW_{GHz}.IIP3_{mW}}{Pdc_{mW}.(F_{lin}-1).A_{mm^2}}\right). \quad (4.3)$$

Where BW is the bandwith in GHz of the LNA and A the area in mm².

The performances of the LNAs in each case are detailed in Table 4.9. The 3rd order Input Intermodulation Point ($IIP3$) and the area of the circuit are constant for all the designs ($IIP3 = -16\,dBm$ and $A = 0.0015\,mm^2$).

@2.4 GHz	Performances	Increase biasing technique	Decrease biasing technique	Proposed technique
LP	**NF_{LNA} (dB)**	7	7	6.7
	Gv_{LNA} (dB)	17.2	15.4	17
	$FoM1_{LNA}$	55.4	45.9	**52.3**
	Pdc_{LNA} (mW)	0.3	**0.51**	0.32
HP	**NF_{LNA} (dB)**	**5.9**	3.6	3.6
	Gv_{LNA} (dB)	22	24	24
	$FoM1_{LNA}$	46.8	56.4	**56.4**
	Pdc_{LNA} (mW)	2	2	2

Table 4.9 Comparison of the performances for three methods of reconfiguration at a simulation level.

From both fixed geometry LNAs, it is not possible to reach the performances of the opposite mode. For instance, with the increase biasing technique, the noise figure does not reached values under 5.9 dB. With the decrease biasing technique, the failure is on the power consumption of the low power mode which is 1.7 times higher than the low power mode of the other techniques for comparable performances.

The FoM of the LNA and the design points (LP and HP) for the three techniques are presented in Figure 4.18. If we consider a maximum degradation of 10% of FoM between LP and HP modes, only the segmented LNA with constant J_{opt} can achieve this performance as illustrated in Figure 4.18(d).

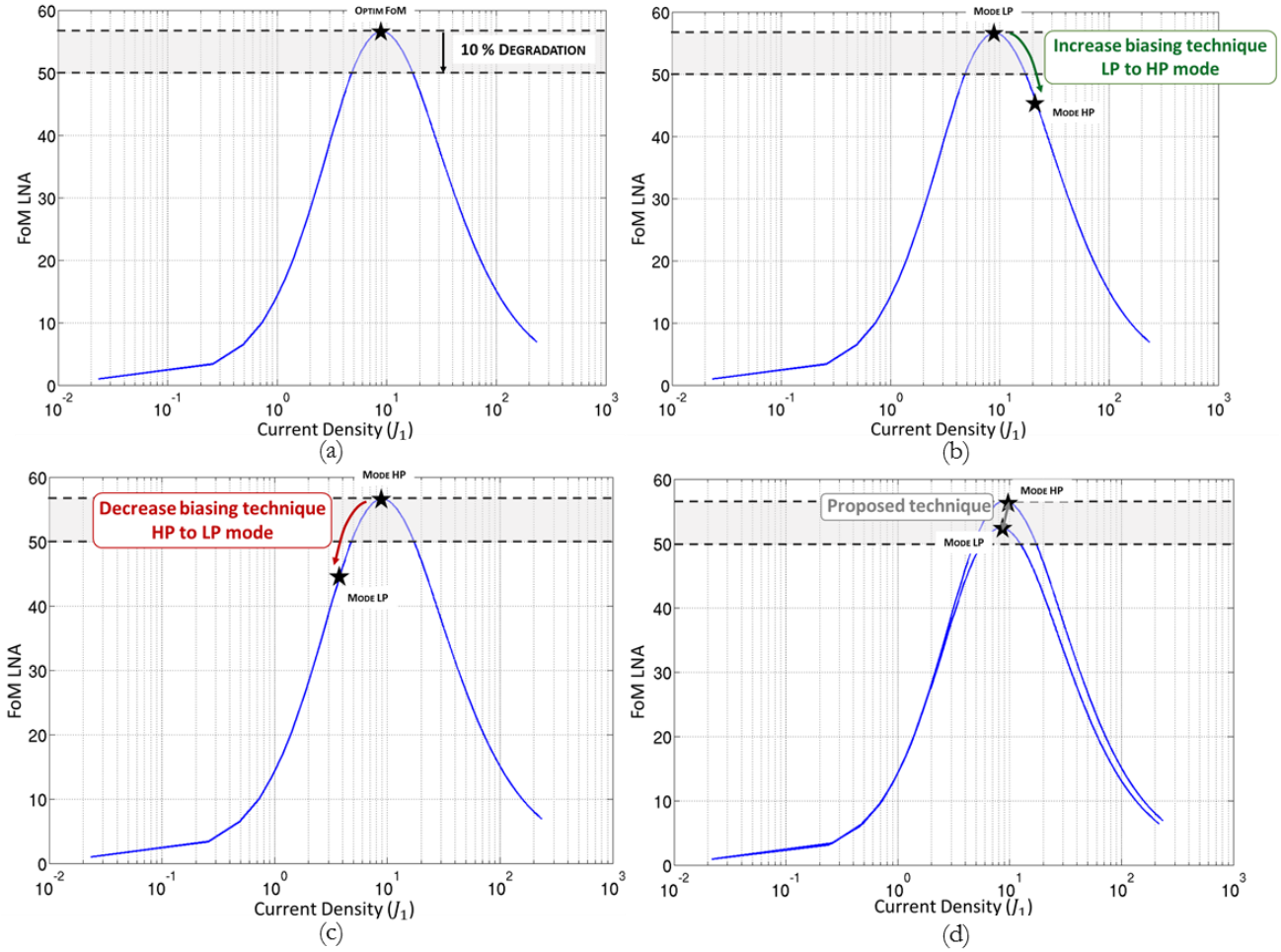


Figure 4.18 Comparison of FoM1 of the tunability methods on the CG gm-boost LNA: (a) FoM1 versus current density in transistor M1 for this structure and maximum degradation; (b) Results for increase biasing technique; (c) Results for decrease biasing technique; (d) Results for proposed technique.

The FoM of the LP mode with the proposed tuning technique (Figure 4.18 (d)) is degraded by 7% compared to the maximum FoM. This degradation is lower than 10% and the reached performances are better than with the increase and decrease biasing techniques.

These observations have been realized at a simulation level, next Subsection presents the Integrated Circuit (IC) implementation and the measurement results of the proposed tunable LNA.

4.4 INTEGRATED CIRCUIT (IC) IMPLEMENTATION AND MEASUREMENT RESULTS

This Section describes the implementation of the chip and presents the measurement results of the proposed 3-modes LNA. A comparison between the low power LNA of Chapter 3 and the low power mode of the tunable LNA is also proposed. Finally, the results are compared with the State of the Art of fixed and tunable LNAs.

4.4.1 THE CHIP

The proposed tunable LNA has been implemented in UTBB FD-SOI 28 nm from technology STMicroelectronics.

As for the proposed inductorless ULP LNA described in Chapter 3, the complete chip presents an area of 0.5 mm^2 and the inductorless tunable LNA core is 0.0015 mm^2.

The tunable LNA is followed by a buffer which is adapted to the output impedance of the LNA in all its operating modes. The same buffer is de-embedded in order to isolate the performances of the LNA.

The back gate voltages controls could be implemented by a Serial Peripheral Interface (SPI). However, for test facilities, the back gate voltages are externally controlled (0V or +2V). The implementation of a complete chip in FD-SOI technology will need a back bias generator which is able to provide this voltage for the lowest power consumption and high efficiency as proposed in [50] for instance.

The layout and the die micrograph of the chip are depicted in Figure 4.19.

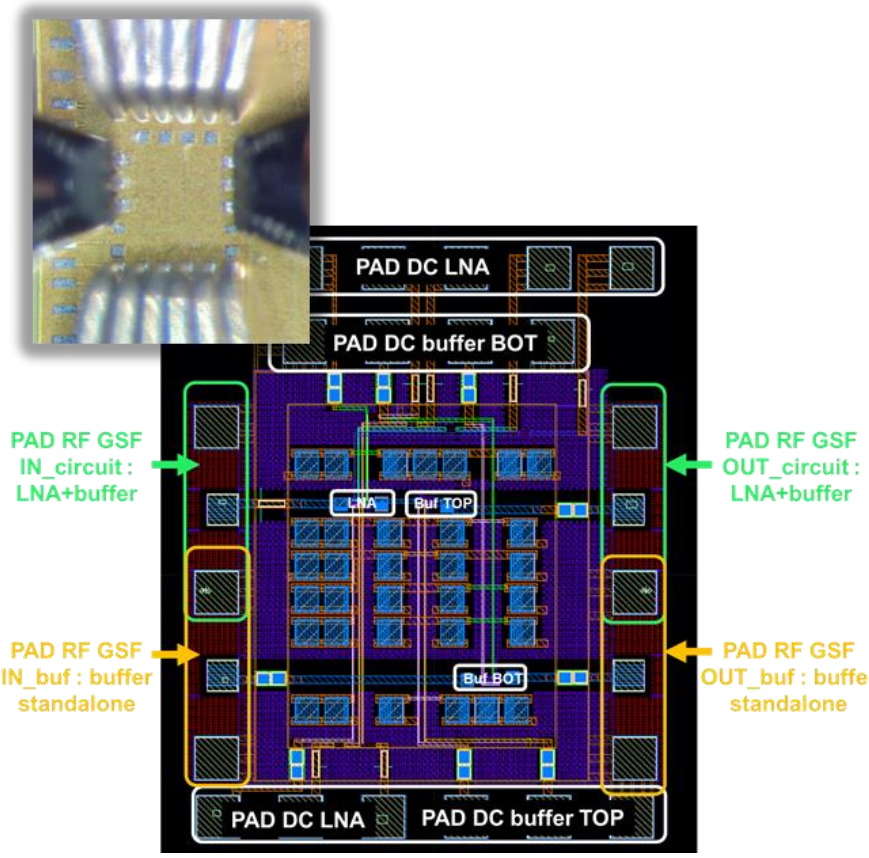


Figure 4.19 Layout and die micrograph of the chip.

4.4.2 MEASUREMENT RESULTS

THREE OPERATING MODES OF THE TUNABLE LNA

The DC operating point (currents and voltages of the power supply, the current biasing, the input and the output) are verified for the three modes of the LNA.

Several chips have been tested and the results of all the chips are similar.

Results of the Post Layout Simulations (PLS) and the measured voltage gain (Gv), noise figure (NF), and input matching ($S11$) for the optimized three modes LNA are plotted in Figure 4.20.

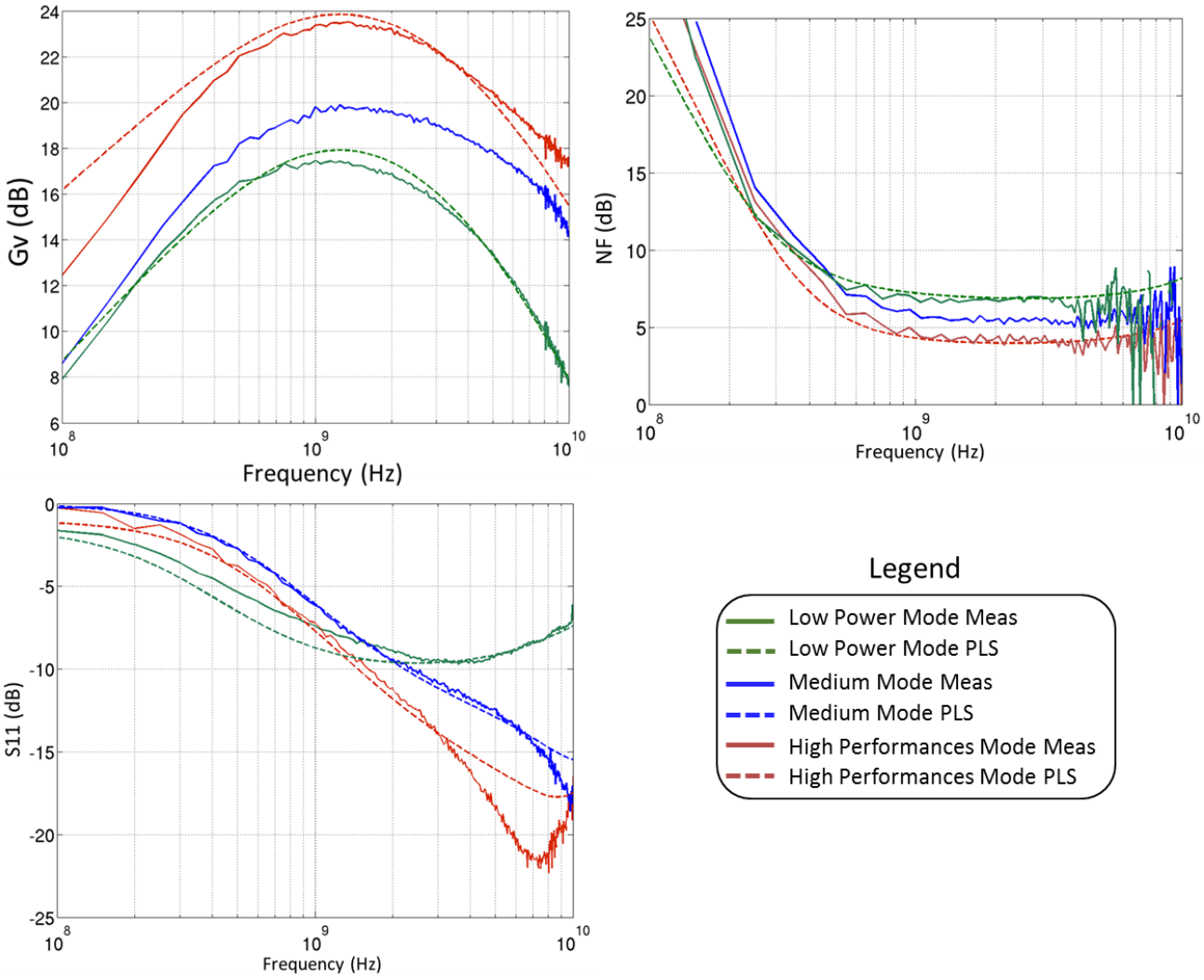


Figure 4.20 Voltage gain (dB), noise figure (dB) and input matching (dB) measurements and Post Layout Simulation results of the tunable LNA in its three operating modes.

The 1-dB Compression Point ($P1dB$) and the 3rd order Input Intermodulation Point ($IIP3$) are measured with a variation of the input power from -50 dBm to -10 dBm. Two RF tones with a 10 MHz difference are applied to determine the $IIP3$.

$IIP3$ and $P1dB$ measurements in the three modes are depicted in Figure 4.21 and Figure 4.22 respectively.

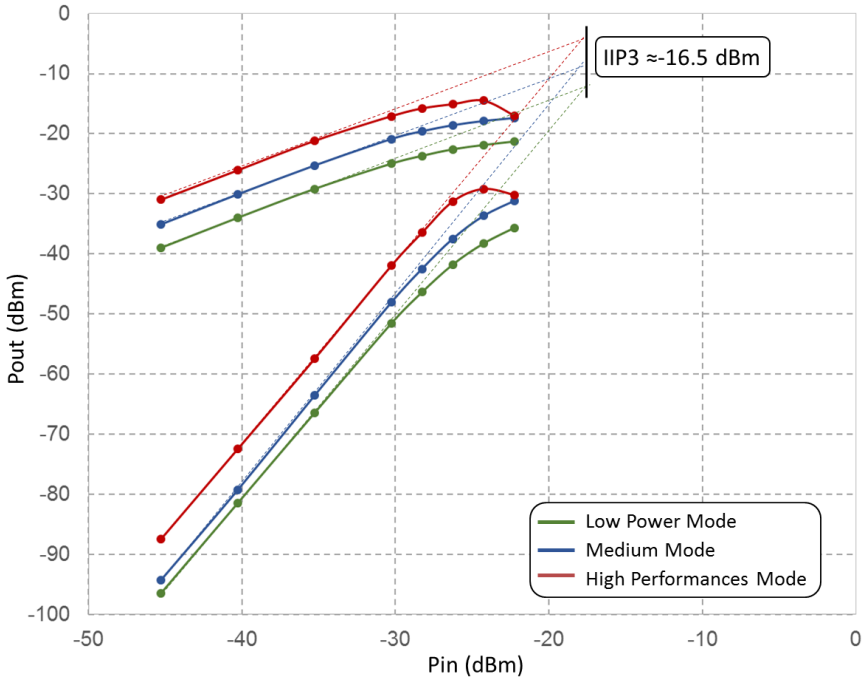


Figure 4.21 3rd order Input Intermodulation Point (IIP3) measurements results of the tunable LNA in its three operating modes.

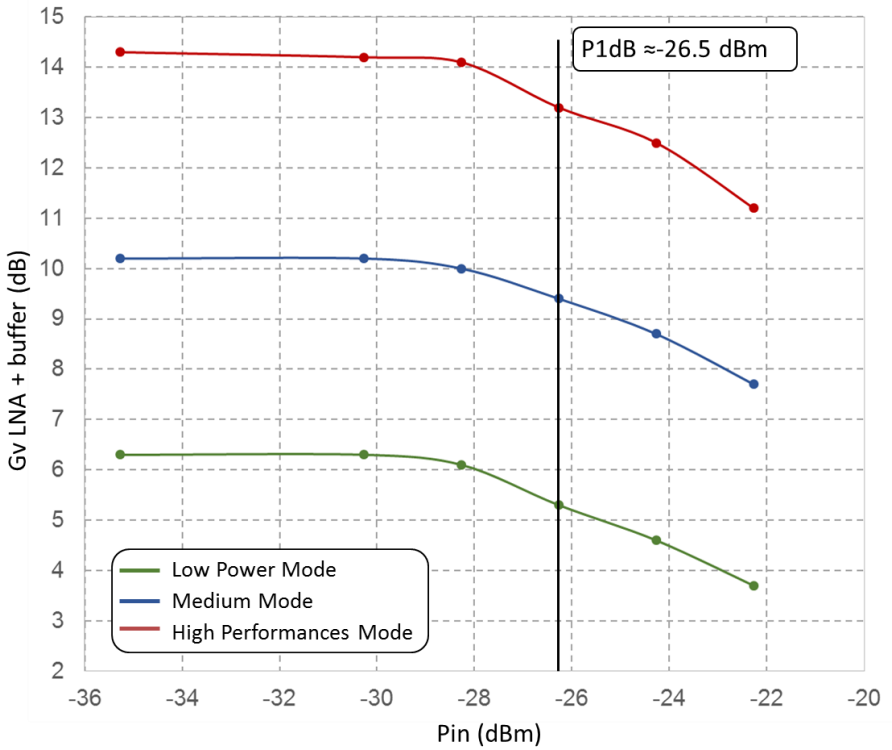


Figure 4.22 1-dB Compression Point (P1dB) measurements results of the tunable LNA in its three operating modes.

Table 4.10 details the measurements results for the three modes of operation.

@2.4GHz	3 dB-BW (GHz)	Gv (dB)	NF (dB)	IIP3 (dBm)	Pdc (mW)	Supply (V)	Back Gate (0=0V & 1=2V) $M_{11}M_{12}M_{21}M_{22}M_{23}M_{24}$
Low Power Mode	4.1	16.8	6.6	-16	0.35	0.6	101000
Medium Mode	6.3	19.4	5.4	-16	0.9	0.9	111100
High Performances Mode	6.4	22.9	3.6	-16	2	1.2	111111

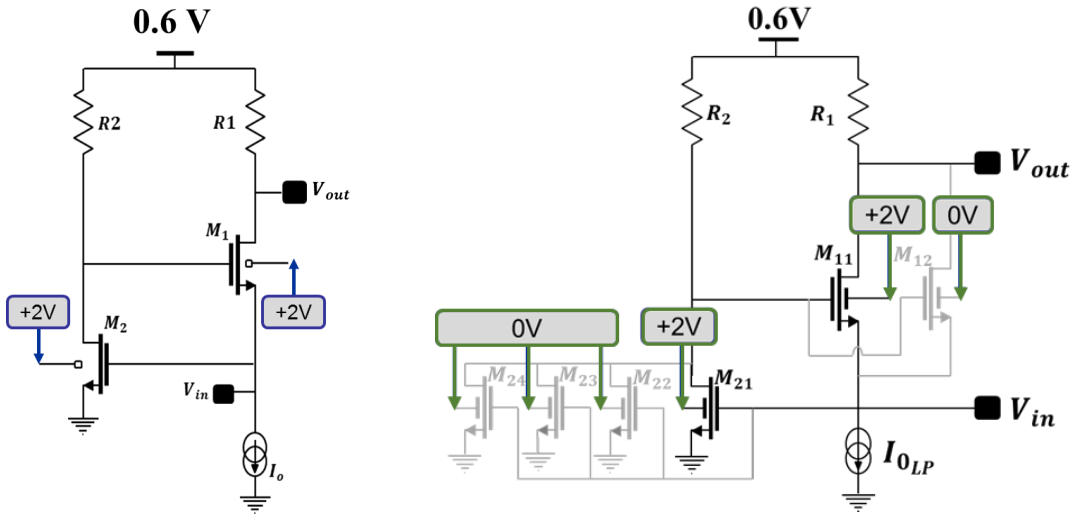
Table 4.10 Measurement results of the tunable LNA at 2.4GHz.

The measurement results of low power mode of the tunable LNA is now compared with the ULP LNA of Chapter 3 in order to evaluate the degradation attributed to the additional transistors in subthreshold region.

Focus on the Low Power Mode

In this mode, the tunable LNA can be compared to the ULP LNA presented in Chapter 3. Only two transistors (M_{11} and M_{21}) are in strong inversion. Their back gate voltages are maximum (+2 V) in order to decrease their voltage thresholds. All the threshold voltages of other transistors are maximized to reduce their contribution to the performances of the LNA. Therefore, M_{12} and $M_{22}$to M_{24} are operating in subthreshold region.

Figure 4.23 depicts the ULP LNA of Chapter 3 and the tunable LNA in its low power mode.



(a) (b)

Figure 4.23 Comparison of: (a) the ULP LNA of Chapter 3 and (b) the low power mode of the proposed tunable LNA.

A comparison of the measurements results voltage gain (Gv), noise figure (NF), and input matching ($S11$) of the fixed ULP LNA and the tunable LNA in low power mode are plotted and compared in Figure 4.24.

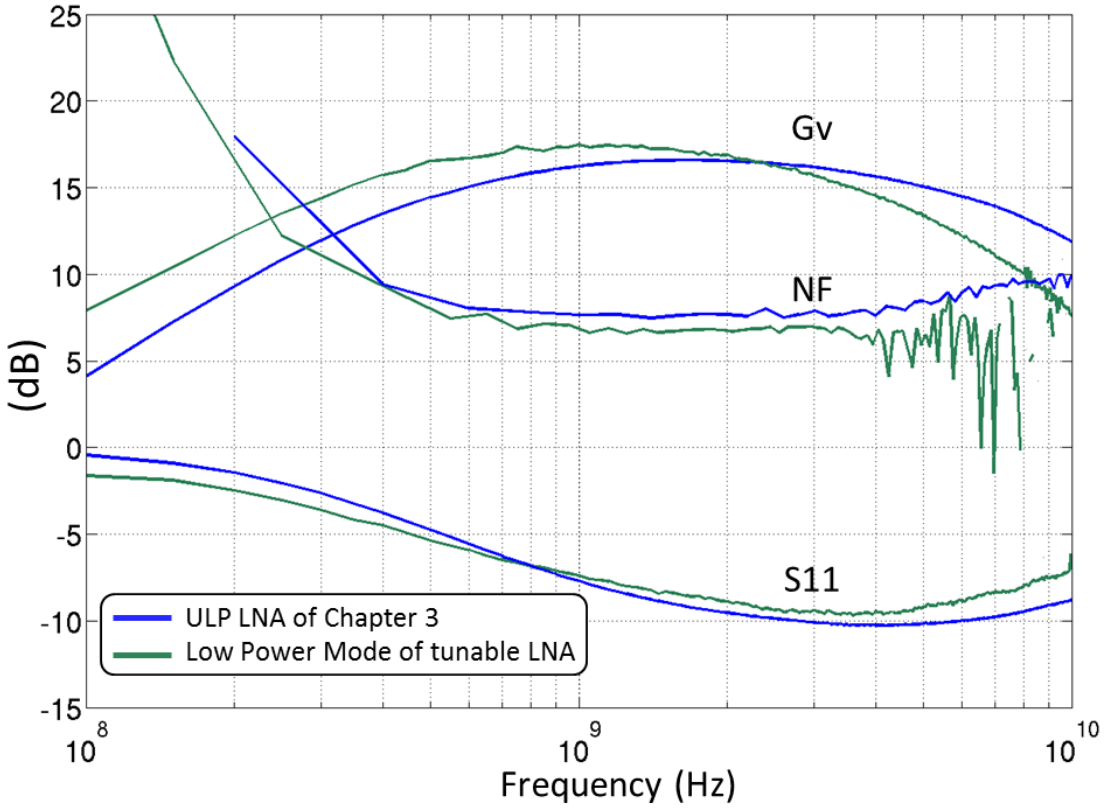


Figure 4.24 Measurement results of ULP LNA of Chapter 3 and proposed tunable LNA in its low power mode.

The voltage gain of the low power mode of the tunable LNA is higher at low frequency. This is mainly due to the improvement of the layout of the coupling capacitance at the input of the LNA. The bandwidth of the tunable LNA is degraded compared to the ULP LNA as detailed previously.

The noise figure of the tunable LNA is improved by 0.7 dB. This improvement is linked to the 15 % of additional power consumption in the tunable LNA compared to the ULP LNA.

Moreover, the input matching ($S11$) of the low power mode of the tunable LNA is degraded compared to the input matching of the ULP LNA. This is due to two different effects. First; the lowest transconductances gm_1 and gm_2 of the active transistors as the current flows both into the active transistors and the subthreshold transistors impact the input matching. Then, the additional capacitance brought by the transistors in subthreshold region also degrades the matching.

4.4.3 COMPARISON WITH EXISTING LNAS

COMPARISON WITH NON-ADAPTIVE LNAS

The performances of the tunable LNA are compared with the State Of the Art of non-tunable LNAs. In order to compare the circuits, the FoM_2 defined in Equation (4.3) is used. Figure 4.25 depicts the FoM_2 versus the power consumption of the State of the Art of LNAs.

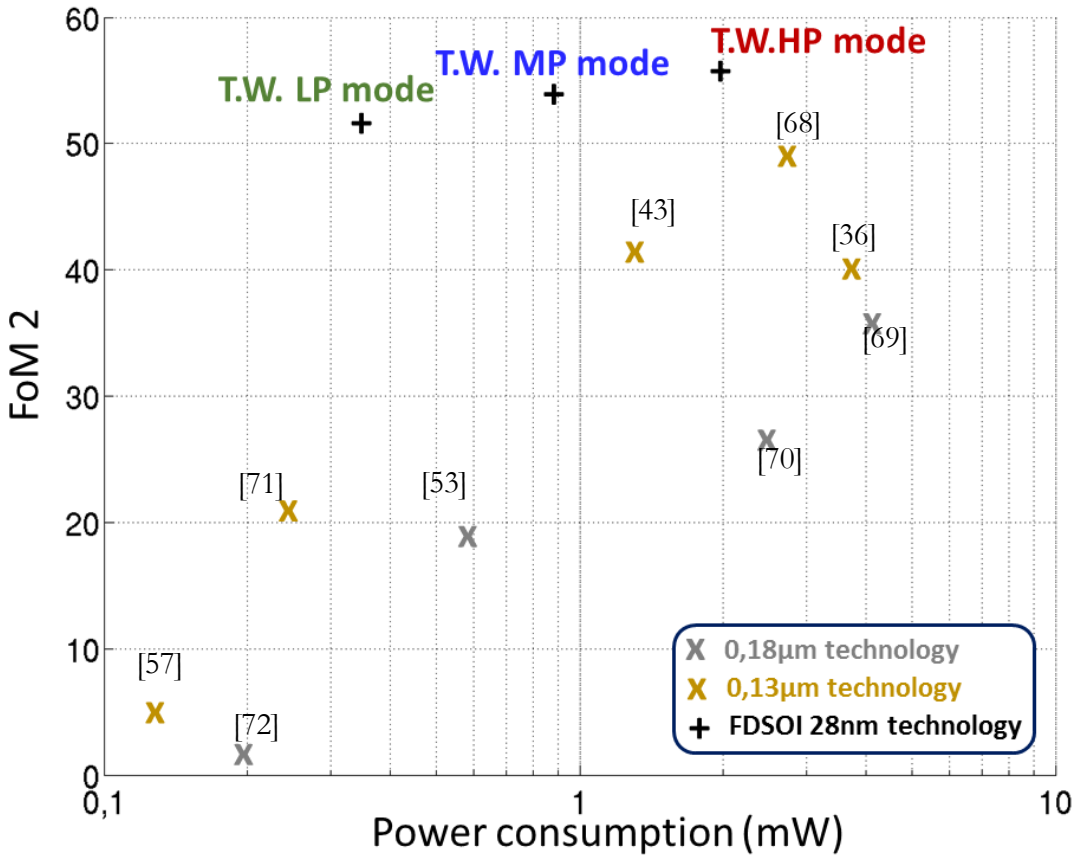


Figure 4.25 Figure of Merit (FoM2) of the State of the Art LNAs versus the power consumption.

As depicted, the final FoM_2 of the proposed LNA is better than the State of the Art of LNAs for the same power consumption range. Considering the technology, the advanced node FD-SOI 28 nm technology, presents better performances than the 180 nm and 130 nm CMOS technology. A higher cutoff frequency but also better gain for lower drain current of a transistor is part of the good measurement results. Moreover, the proposed technique for tunability is only possible with a FD-SOI technology where body biasing is allowed.

The performances of the tunable LNA and the State of the Art LNAs are detailed in Table 4.11.

Ref.	Gv (dB)	3 dB-BW (GHz)	NF (dB)	IIP3 (dBm)	Pdc (mW)	Supply (V)	Tech.	Area (mm^2)	FoM 2
T.W. LP	**16.8**	**0.1–4.2**	**6.6**	**-16**	**0.35**	**0.6**	**FD-SOI 28 nm**	**0.0015**	**51.6**
T.W. MP	**19.4**	**0.1–6.4**	**5.4**	**-16**	**0.9**	**0.9**	**FD-SOI 28 nm**	**0.0015**	**53.2**
T.W. HP	**22.9**	**0.1–6.5**	**3.6**	**-16**	**2**	**1.2**	**FD-SOI 28 nm**	**0.0015**	**55.4**
[43]	20	0.1–2.7	4	-12	1.32	1.2	CMOS 0.13 µm	0.007	41.4
[53]	14.7	2.1–2.5	4.8	2	0.6	1.8	CMOS 0.18 µm	0.39	19.2
[68]	23	0.1–1.77	1.85	−2.9	2.8	2	CMOS 0.13 µm	0.03	48.2
[71]	14	0.6–4.2	4	−10	0.25	0.5	CMOS 0.13 µm	0.39	21.8
[57]	13[1]	1.5-2.4	5.3	-12.2	0.06	0.4	CMOS 0.13 µm	0.63	5.9
[72]	15	0.4-1	4.2	-15	0.2	1	CMOS 0.18 µm	0.27	1.7
[69]	12	3-8.1	2.8	4.2	4.2	0.6	CMOS 0.18 µm	0.23	35.7
[36]	20.8	0.1-3.5	2.2	-11.5	3.8	1	CMOS 0.13 µm	0.007	40
[70]	13.9	1.5-3	5	2.8	2.5	0.5	CMOS 0.18 µm	0.18	27.7

Table 4.11 Comparison of the proposed LNA with the State of The Art LNAs.

The proposed LNA in its three operating mode achieves overall better performances than the state of the Art of LNAs, leading to highest FoM.

COMPARISON WITH TUNABLE LNAS

The variation ranges in noise figure and voltage gain of existing tunable LNAs are compared with the proposed tunable LNA.

Table 4.12 presents the performances of the extreme modes (lowest and highest) of the State of the Art of tunable LNAs.

Mode	Performances	This Work	[63]	[56]	[73]	[74]	[64]	[59]	[75]
Lowest	**NF_{LNA} (dB)**	**6.6**	7.5	7.3	4	5.3	3.4	3.6	6.3
	Gv_{LNA} (dB)	**16.8**	14	16.8	14.8	13.1	15	9.2	4.5
	Pdc_{LNA} (mW)	**0.35**	0.3	0.3	3.2	0.06	1.52	1	0.16
Highest	**NF_{LNA} (dB)**	**3.6**	4	6.3	3	4.6	2.5	2.9	4.7
	Gv_{LNA} (dB)	**22.9**	26	21.5	19	15.7	17	14.4	9.1
	Pdc_{LNA} (mW)	**2**	2.1	0.9	5.7	0.13	7.1	5.4	0.4

Table 4.12 Comparison of the ranges of performances of the State of the Art tunable LNAs.

The performances in noise figure and voltage gain of several modes for each available tunable LNAs in the literature are depicted in Figure 4.26.

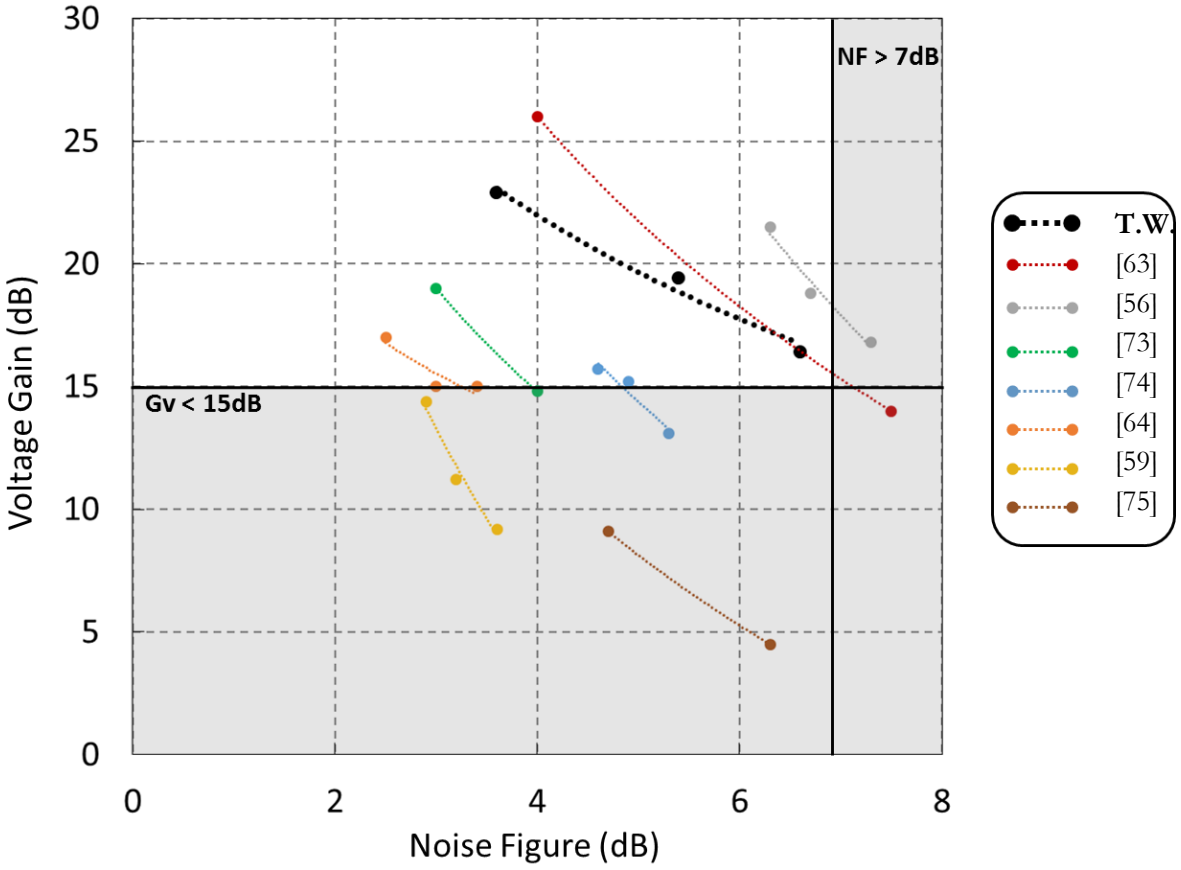


Figure 4.26 State of the Art of tunable LNAs: variation range of performances in noise figure and voltage gain.

In addition to the highest FoM, the proposed LNA offers the largest range of variation in terms of voltage gain and noise figure while maintaining the minimum conditions (Gv > 15 dB and NF < 7 dB).

4.5 DESIGN OF A TUNABLE LNA WITH FD-SOI BACK GATE TUNING: SUMMARY

This last Chapter concentrates on the design of a tunable LNA which is able to address the three operating modes established in Chapter 2. First, a State of the Art of the methods to add tunability in the design of LNAs is presented. From the techniques of the State of The Art, the tuning capability is: either possible only in a limited range, or the performances of the LNA are optimized only in one mode and the other modes are degraded. From these observations, the optimal design points which yield the targeted specifications in each of the three operating modes are determined from design with fixed geometries. A design flow where the maximum Figure of Merit (FoM) is maintained in every mode is then proposed.

A new method to add tunability on the performances of the LNA by tuning the back gate voltages of FD-SOI transistors is demonstrated. This method offers the possibility to optimize all the operating modes and to keep the performances at a maximum FoM.

The final measurements confirm the possibility to use the body biasing of FD-SOI transistors in order to change their region of operation and thus, add tunability in a LNA while offering optimized performances in each mode. Even if the tuning technique adds parasitic elements and degrades the maximum FoM, the proposed LNA offers the highest FoM and the best range of performances tunability of the State of the Art.

CHAPTER 5

CONCLUSION AND PERSPECTIVES

The first Chapter presents the Internet of Things (IoT) context and the main challenges brought by this critical and vast Wireless Sensor Networks (WSNs) deployment. To answer these needs, this thesis proposes a system level analysis and a Proof-of-Concept (PoC) on circuit level for the design of channel aware receiver. The purpose of this thesis is to address some important challenges of the development of radio interfaces dedicated to IOT applications which are:

- SMALL FORM FACTOR: reduce the size of communicating nodes by decreasing the footprint of the circuits for a total transparency in the environment and unobtrusive network to propose a "green connected planet";

- LOW POWER: in a large network with many communicating nodes, the battery replacement can be difficult, expensive or even impossible. Nodes have to be able to operate for long period;

- LOW COST: the deployment of billions of connected objects is only possible if the individual cost of a node is very low;

- QUALITY: fulfil the performances requirements in order to respect the targeted Quality of Service (QoS) set by the standards is essential.

At system-level, this thesis investigates on the design of a power optimized receiver which is able to adapt its performances with the state of the channel. At circuit-level, this thesis explores the benefits of the Ultra-Thin Body and Buried-oxide Fully Depleted Silicon-On-Insulator (UTBB FD-SOI) technology to design an adaptive Low Noise Amplifier (LNA) with optimized power for a given set of performance.

This Chapter summarizes the key contributions of the work in the design of smart wireless receivers for WSNs and IoT applications. The perspectives of the work and suggestions for future research on the subject of channel aware receiver design are then commented.

5.1 KEY CONTRIBUTIONS OF THIS WORK

The research presented in this thesis consists in the following key contributions:

- A system level analysis to optimize a channel aware receiver is proposed in Chapter 2. A new method to increase the battery lifetime of a receiver is demonstrated. It consists in a discrete reconfiguration of the performances to enable a fast and efficient solution. The proposed method is evaluated on the implementation of a WSN with the ZigBee® standard. The final analysis of the system demonstrates that a 3-mode receiver would achieve a factor of power saving of 4.5 compared to a fixed performance receiver.

- The design of an inductorless LNA which can address the low power mode performances is proposed in Chapter 3. The design methodology includes the threshold voltage adjustment of the FD-SOI transistors via their body biasing. It demonstrates a new possibility to decrease the power consumption of the LNA by tuning their back gate voltages. The final measurements confirm the possibility to use the body biasing of FD-SOI transistors to decrease the power supply and thus to reduce the power consumption of the circuit. It makes the FD-SOI technology a suited candidate for Ultra Low Voltage (ULV) and ULP designs.

- Chapter 4 describes the design of an innovative reconfigurable LNA which is able to address three optimized operating modes. A design flow which maximizes the tradeoff performance versus power consumption in all the modes is proposed. A new method to add tunability on the performances of the LNA by tuning the back gate voltages of FD-SOI transistors is demonstrated. The final measurements confirm the possibility to use the body biasing of FD-SOI transistors in order to change their region of operation and add tunability in a LNA while offering optimized performances in each mode.

The design of the reconfigurable LNA with FD-SOI technology demonstrates the possibility to tune a circuit without degrading the targeted performances. The PoC lays the first stone of a complete optimized performances versus power consumption tunable receiver. The next Subsection presents several directions for future research on the design of a channel aware transceiver for IoT applications.

5.2 FUTURE WORK

In this research direction, several improvements and further developments are opened:

- The targeted performances for the receiver and for the LNA, see Chapter 2, are based on a specific type of network for a specific standard and on specific propagation conditions between the transmitter and the receiver. The probability distribution of the received power at the input of the receiver is different when other propagation conditions are taken into account as depicted in Figure 5.1. The thresholds optimization described in Chapter 2 is dependent on these conditions. Therefore, all the tunable blocks of the receiver should be able to reconfigure themselves with the variations of the reconfiguration thresholds. Different design choices for the receiver and the LNA could be optimal in other network environments.

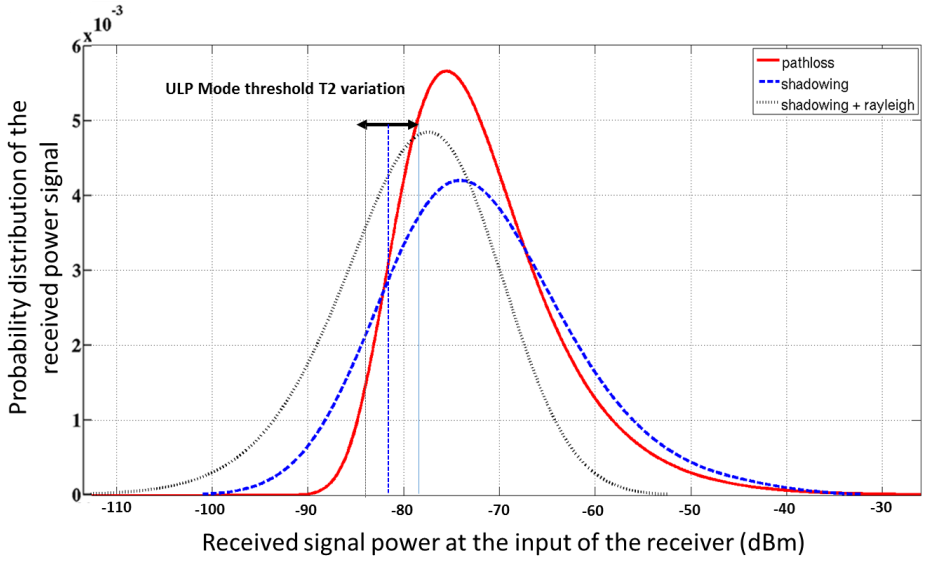


Figure 5.1 Probability distribution of the received power signal for several channel conditions.

- An innovative use of the FD-SOI technology to tune a LNA has been proposed. The other blocks of an adaptive transceiver could benefit from the body biasing. For instance, the same width scaling via back gate tuning technique could be implemented in a Power Amplifier (PA) to offer several transmitted power level while maintaining an optimized drain efficiency. The Gm-C filters use switched inverters and vary the width of the inverter by adding several inverters in parallel. The switched transistor could be avoid by tuning the back gate of the FD-SOI transistors and the cutoff frequency could be therefore tuned. A FD-SOI mixer could be implemented with a Local Oscillator (LO) signal applied on the back gate as it is

possible to switch the transistor with specific biasing condition. The mixer could also be merged with the proposed tunable LNA, by replacing the load resistance. It would demand higher voltage supply but the current would be reused from the LNA to the mixer.

- The FD-SOI technology can also be used to calibrate and compensate the Process Voltage Temperature PVT variations. A self-healing receiver able to correct these variations with Built-In-Self-Tests (BISTs) could be implemented. The receiver would be more robust to the production variations.

5.3 LIST OF CONTRIBUTIONS

J. Zaini, F. Hameau, T. Taris, D. Morche, L. Q. V. Tran, and P. Audebert, "Channel aware receiver front end for low power 2.4 GHz Wireless Sensor Network: A system level analysis," in 2016 14th IEEE International New Circuits and Systems Conference (**NEWCAS**), 2016, pp. 1–4.

J. Zaini, F. Hameau, T. Taris, D. Morche, P. Audebert, and E. Mercier, "A tunable Ultra Low Power inductorless Low Noise Amplifier exploiting body biasing of 28 nm FDSOI technology," in 2017 IEEE/ACM International Symposium on Low Power Electronics and Design (**ISLPED**), 2017, pp. 1–6.

J. Zaini, F. Hameau, T. Taris, D. Morche, and P. Audebert, "Ultra low power inductorless low noise amplifier: Comparison of FDSOI technologies," in 2017 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (**S3S**), 2017, pp. 1–2.

J. Zaini-Desevedavy, F. Hameau, T. Taris, D. Morche, and P. Audebert, "An Ultra-Low Power 28 nm FD-SOI Low Noise Amplifier Based on Channel Aware Receiver System Analysis," J. Low Power Electron. Appl. (**JLPEA**), vol. 8, no. 2, p. 10, Apr. 2018.

APPENDIX

LNA NOISE CALCULATION

The purpose of this appendix is to determine the noise figure of the proposed gm-boost CG LNA. All the element which contribute to the noise are isolated one by one in order to establish the final equation of the noise figure of the LNA.

I. OUTPUT NOISE GENERATED BY TRANSISTOR M1

Figure A.1 shows the equivalent small signal circuit for calculation of $V_{noise_{M_1}}$, the output noise generated by transistor M1. All other noise source are neglected in order to isolate only noise of transistor M1.

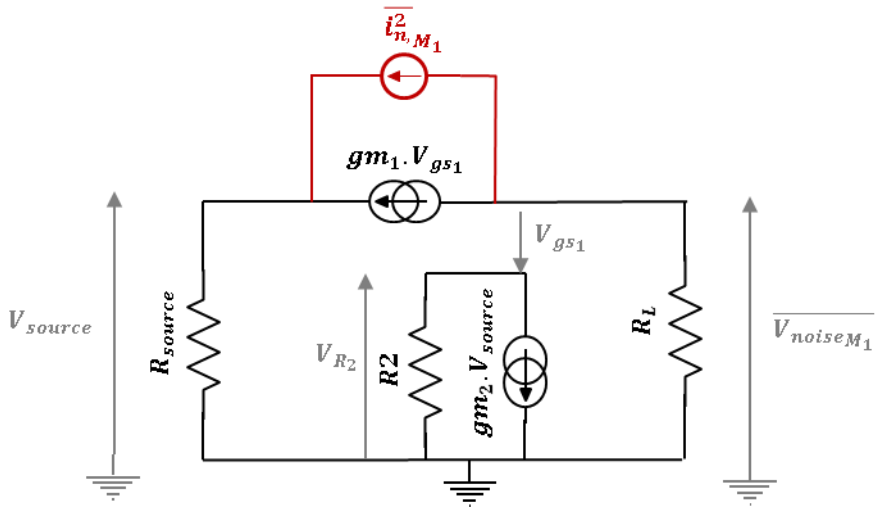


Figure A.1 Output noise generated by transistor M1.

From this small signal circuit, the following equations or equivalence can be deducted.

$$\begin{cases} V_{gs_1} = V_{R_2} - V_{source} \\ V_{source} = R_{Source}.\left(gm_1.V_{gs_1} + i_{noise_{M_1}}\right) \\ i_{noise_{M_1}} = \sqrt{4.k.T.\frac{\gamma}{\alpha}.gm_1} \\ V_{R_2} = -R_2.gm_2.V_{source} \\ V_{noise_{M_1}} = -R_L.\left(\sqrt{4.k.T.\frac{\gamma}{\alpha}.gm_1} + gm_1.V_{gs_1}\right) \end{cases}$$

After simplification, $V_{noise_{M_1}}$ the noise generated by transistor M1 is defined in Equation (A.4).

$$V_{noise_{M_1}} = \frac{-R_L.\sqrt{4.k.T.\frac{\gamma}{\alpha}.gm_1}}{1 + R_2.gm_2.R_{Source}.gm_1 + R_{source}.gm_1} \quad (A.4)$$

II. OUTPUT NOISE GENERATED BY TRANSISTOR M2

The equivalent small signal for the output noise generated by transistor M2 is illustrated in Figure A.2.

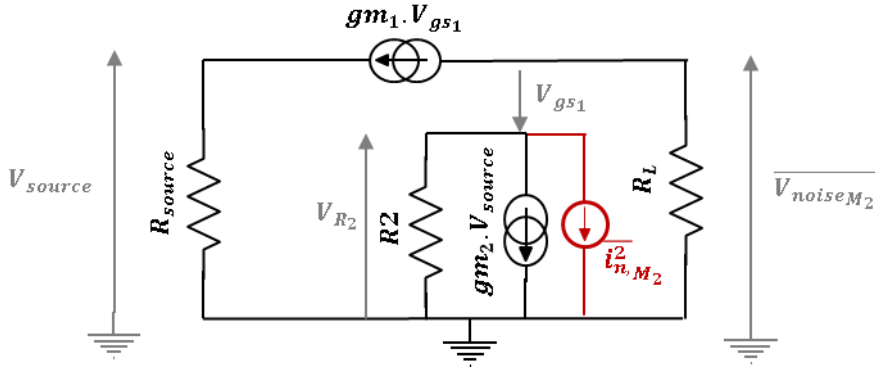


Figure A.2 Output noise generated by transistor M2.

$$\begin{cases} V_{source} = R_{Source}.gm_1.V_{gs_1} \\ V_{noise_{M_2}} = R_L.\left(-gm_1.V_{gs_1}\right) \\ i_{noise_{M2}} = \sqrt{4.k.T.\frac{\gamma}{\alpha}.gm_2} \\ V_{R_2} = -\left(gm_2.V_{source} + i_{noise_{M2}}\right) \\ V_{gs_1} = V_{R_2} - V_{source} \end{cases}$$

The noise generated by M2 after simplification is given in Equation (2.10).

$$V_{noise_{M_2}} = \frac{R_2.R_L.gm_1.\sqrt{4.k.T.\frac{\gamma}{\alpha}.gm_2}}{1 + R_2.gm_2.R_{Source}.gm_1 + R_{source}.gm_1} \qquad (A.5)$$

III. OUTPUT NOISE GENERATED BY RESISTANCE R2

The same methodology has been done for the calculation of the noise generated by R2 as illustrated in Figure A.3.

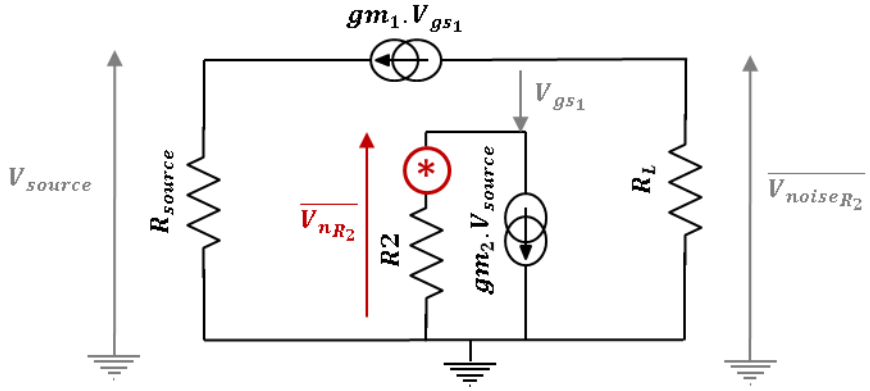


Figure A.3 Output noise generated by resistance R2.

The equation set for the output noise of R2 is defined:

$$\begin{cases} V_{n_{R_2}} = \sqrt{4.k.T.\frac{\gamma}{\alpha}.R_2} \\ V_{gs_1} = V_{R_2} - V_{source} \\ V_{noise_{R_2}} = -R_L.gm_1.V_{gs_1} \end{cases}$$

Which gives the final noise generated by R2, Equation (A.6).

$$V_{noise_{R_2}} = \frac{-R_L.gm_1.\sqrt{4.k.T.\frac{\gamma}{\alpha}.R_2}}{1 + R_{source}.gm_1} \qquad (A.6)$$

IV. OUTPUT NOISE GENERATED BY THE SOURCE RESISTANCE

The contribution of the source resistance on the output noise is then established as depicted in Figure A.4.

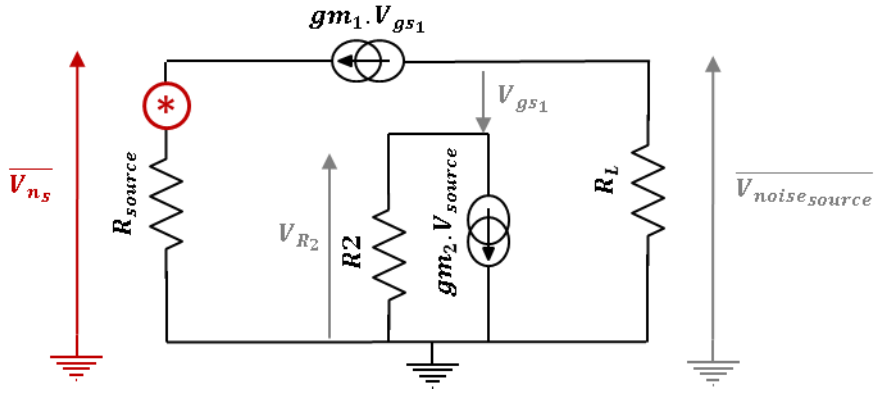


Figure A.4 Output noise generated by the source resistance Rsource.

$$\begin{cases} V_{n_s} = \sqrt{4.k.T.\frac{\gamma}{\alpha}.R_{Source}} \\ V_{gs_1} = V_{R_2} - V_{source} \\ V_{R_2} = -R_2.gm_2.V_{source} \end{cases}$$

Finally, the noise generated by the source resistance is given in Equation (A.7).

$$V_{noise_{Source}} = R_L . gm_1 . \sqrt{4.k.T.\frac{\gamma}{\alpha}.R_{source}}.(1 + gm_2.R_2) \quad (A.7)$$

V. OUTPUT NOISE GENERATED BY THE LOAD RESISTANCE RL

The last contributor on the noise of the proposed LNA is the load resistance RL. The small signal model of its noise contribution is illustrated in Figure A.5.

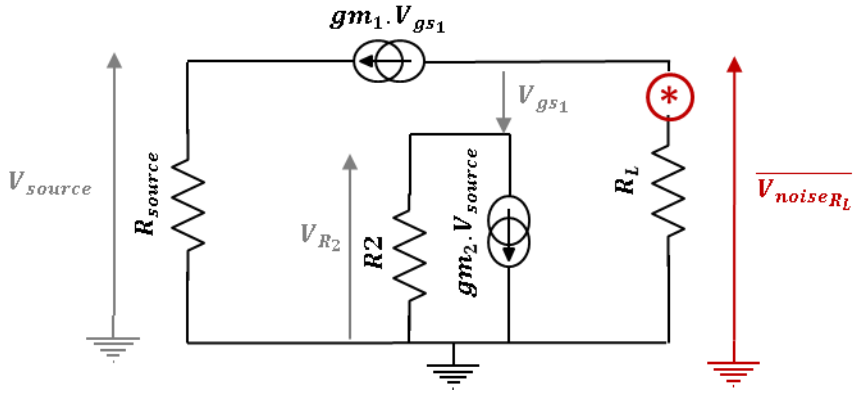


Figure A.5 Output noise generated by the load resistance RL.

The equation of the noise of the load resistance is given in Equation (A.8).

$$V_{noise_{R_L}} = \sqrt{4.k.T.\frac{\gamma}{\alpha}.R_L} \quad (A.8)$$

VI. TOTAL NOISE OF THE LNA

The overall noise of the LNA is based on Friis Formula [1], Equation (A.9).

$$F_{LNA} = \frac{\overline{V_{noise_{source}}^2} + \overline{V_{noise_{M_1}}^2} + \overline{V_{noise_{M_2}}^2} + \overline{V_{noise_{R_2}}^2} + \overline{V_{noise_{R_L}}^2}}{\overline{V_{noise_{source}}^2}} \quad (A.9)$$

The final noise of the LNA is given in Equation (A.10).

$$F_{LNA} = 1 + \frac{\frac{\gamma}{\alpha} + \frac{\gamma}{\alpha}.gm_1.gm_2.R_2^2 + \frac{4.R_2.gm_1}{(1+gm_1.R_S)^2}}{gm_1.R_S.(1+gm_2.R_2)^2} \quad (A.10)$$

BIBLIOGRAPHY

[1] "TAKE THE WORLD WITH YOU." [Online]. Available: https://www.ericsson.com/assets/local/investors/documents/financial-reports-and-filings/annual-reports/ericsson_ar_2010_en.pdf. [Accessed: 13-Dec-2017].

[2] D. Bol *et al.*, "Green SoCs for a sustainable Internet-of-Things," in *2013 IEEE Faible Tension Faible Consommation*, 2013, pp. 1–4.

[3] A. Bachir, M. Dohler, T. Watteyne, and K. K. Leung, "MAC Essentials for Wireless Sensor Networks," *IEEE Commun. Surv. Tutor.*, vol. 12, no. 2, pp. 222–248, Second 2010.

[4] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits," *Proc. IEEE*, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[5] R. Wilson *et al.*, "A 460MHz at 397mV, 2.6GHz at 1.3V, 32b VLIW DSP, embedding FMAX tracking," in *2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC)*, 2014, pp. 452–453.

[6] G. de Streel *et al.*, "SleepTalker: A ULV 802.15.4a IR-UWB Transmitter SoC in 28-nm FDSOI Achieving 14 pJ/b at 27 Mb/s With Channel Selection Based on Adaptive FBB and Digitally Programmable Pulse Shaping," *IEEE J. Solid-State Circuits*, vol. 52, no. 4, pp. 1163–1177, Apr. 2017.

[7] B. Razavi, *RF Microelectronics*. 1998.

[8] N. M. Pletcher, S. Gambini, and J. Rabaey, "A 52 mu W Wake-Up Receiver With $-$ 72 dBm Sensitivity Using an Uncertain-IF Architecture," *IEEE J. Solid-State Circuits*, vol. 44, no. 1, pp. 269–280, Jan. 2009.

[9] S. Lanzisera, A. M. Mehta, and K. S. J. Pister, "Reducing Average Power in Wireless Sensor Networks through Data Rate Adaptation," in *2009 IEEE International Conference on Communications*, 2009, pp. 1–6.

[10] F. Qin, Y. Chen, and X. Dai, "Utilize Adaptive Spreading Code Length to Increase Energy Efficiency for WSN," in *2013 IEEE 77th Vehicular Technology Conference (VTC Spring)*, 2013, pp. 1–5.

[11] S. Dwivedi, B. Amrutur, and N. Bhat, "Power Scalable Radio Receiver Design Based on Signal and Interference Condition," *J. Low Power Electron. Appl.*, vol. 2, no. 4, pp. 242–264, Oct. 2012.

[12] W. Dong *et al.*, "Dynamic Packet Length Control in Wireless Sensor Networks," *IEEE Trans. Wirel. Commun.*, vol. 13, no. 3, pp. 1172–1181, Mar. 2014.

[13] A. Oguz, D. Morche, and C. Dehollaini, "Adaptive power reconfigurability for decreasing power dissipation of wireless personal area network receivers," in *2011 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011, pp. 1900–1903.

[14] L. Lolis, M. de Souza, L. B. Zambon, and A. Mariano, "Impact of a fully reconfigurable LNA on an RF front-end: A system level analysis," in *2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2014, pp. 662–665.

[15] D. Banerjee, B. Muldrey, X. Wang, S. Sen, and A. Chatterjee, "Self-Learning RF Receiver Systems: Process Aware Real-Time Adaptation to Channel Conditions for Low Power Operation," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 64, no. 1, pp. 195–207, Jan. 2017.

[16] J. G. Proakis, *Digital Communications*, 4th ed. McGraw-Hill, 2000.

[17] H. R. Thompson, "Distribution of Distance to Nth Neighbour in a Population of Randomly Distributed Individuals," *Ecology*, vol. 37, no. 2, pp. 391–394, 1956.
[18] G. Retz *et al.*, "A highly integrated low-power 2.4GHz transceiver using a direct-conversion diversity receiver in 0.18 #x00B5;m CMOS for IEEE802.15.4 WPAN," in *Solid-State Circuits Conference - Digest of Technical Papers, 2009. ISSCC 2009. IEEE International*, 2009, pp. 414–415,415a.
[19] J. Prummel *et al.*, "13.3 A 10mW Bluetooth Low-Energy transceiver with on-chip matching," in *2015 IEEE International Solid-State Circuits Conference - (ISSCC) Digest of Technical Papers*, 2015, pp. 1–3.
[20] S. Sayilir, W. F. Loke, J. Lee, B. Epstein, D. L. Rhodes, and B. Jung, "A #x2212;90dBm sensitivity wireless transceiver using VCO-PA-LNA-switch-modulator co-design for low power insect-based wireless sensor networks," in *2013 Symposium on VLSI Circuits*, 2013, pp. C152–C153.
[21] Y.-I. Kwon, T. J. Park, K.-S. Cho, and H.-Y. Lee, "A 9 mW Highly-Digitized 802.15.4 Receiver Using Bandpass ADC and IF Level Detection," *IEEE Microw. Wirel. Compon. Lett.*, vol. 18, no. 12, pp. 824–826, Dec. 2008.
[22] M. Camus, B. Butaye, L. Garcia, M. Sie, B. Pellat, and T. Parra, "A 5.4mW 0.07mm2 2.4GHz Front-End Receiver in 90nm CMOS for IEEE 802.15.4 WPAN," in *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, 2008, pp. 368–620.
[23] X. Zhang, B. Chi, B. Liu, and Z. Wang, "#x2212;80dBm #x223C;0dBm dynamic range, 30mV/dB detection sensitivity piecewise RSSI for SDR/CR receivers," in *2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2014, pp. 89–92.
[24] D. C. Daly and A. P. Chandrakasan, "An Energy-Efficient OOK Transceiver for Wireless Sensor Networks," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1003–1011, May 2007.
[25] B. G. Perumana, R. Mukhopadhyay, S. Chakraborty, C.-H. Lee, and J. Laskar, "A Low-Power Fully Monolithic Subthreshold CMOS Receiver With Integrated LO Generation for 2.4 GHz Wireless PAN Applications," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2229–2238, Oct. 2008.
[26] J. H. Jang, D. F. Berdy, J. Lee, D. Peroulis, and B. Jung, "A wireless sensor node for condition monitoring powered by a vibration energy harvester," in *2011 IEEE Custom Integrated Circuits Conference (CICC)*, 2011, pp. 1–4.
[27] L. Huang *et al.*, "Performance evaluation of an ultra-low power receiver for body area networks (BAN)," in *2010 IEEE 21st International Symposium on Personal, Indoor and Mobile Radio Communications Workshops*, 2010, pp. 89–94.
[28] H. T. Friis, *Noise figures of radio receivers*. 1944.
[29] M. Lont, D. Milosevic, G. Dolmans, and A. H. M. van Roermund, "Mixer-First FSK Receiver With Automatic Frequency Control for Body Area Networks," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 60, no. 8, pp. 2051–2063, Aug. 2013.
[30] H. Elwan, A. Tekin, and K. Pedrotti, "A Differential-Ramp Based 65 dB-Linear VGA Technique in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2503–2514, Sep. 2009.
[31] J. Zaini-Desevedavy, F. Hameau, T. Taris, D. Morche, and P. Audebert, "An Ultra-Low Power 28 nm FD-SOI Low Noise Amplifier Based on Channel Aware Receiver System Analysis," *J. Low Power Electron. Appl.*, vol. 8, no. 2, p. 10, Apr. 2018.
[32] S. B. T. Wang, A. M. Niknejad, and R. W. Brodersen, "Design of a Sub-mW 960-MHz UWB CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2449–2456, Nov. 2006.
[33] B. G. Perumana, J.-H. C. Zhan, S. S. Taylor, B. R. Carlton, and J. Laskar, "Resistive-Feedback CMOS Low-Noise Amplifiers for Multiband Applications," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 5, pp. 1218–1225, May 2008.

[34] M. Chen and J. Lin, "A 0.1 #x2013;20 GHz Low-Power Self-Biased Resistive-Feedback LNA in 90 nm Digital CMOS," *IEEE Microw. Wirel. Compon. Lett.*, vol. 19, no. 5, pp. 323–325, May 2009.
[35] M. El-Nozahi, A. A. Helmy, E. Sanchez-Sinencio, and K. Entesari, "An Inductor-Less Noise-Cancelling Broadband Low Noise Amplifier With Composite Transistor Pair in 90 nm CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1111–1122, May 2011.
[36] J. Borremans, P. Wambacq, C. Soens, Y. Rolain, and M. Kuijk, "Low-Area Active-Feedback Low-Noise Amplifier Design in Scaled Digital CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 11, pp. 2422–2433, Nov. 2008.
[37] L. Belostotski, A. Madanayake, and L. T. Bruton, "Wideband LNA With an Active -C Element," *IEEE Microw. Wirel. Compon. Lett.*, vol. 22, no. 10, pp. 524–526, Oct. 2012.
[38] A. Liscidini, G. Martini, D. Mastantuono, and R. Castello, "Analysis and Design of Configurable LNAs in Feedback Common-Gate Topologies," *IEEE Trans. Circuits Syst. II Express Briefs*, vol. 55, no. 8, pp. 733–737, Aug. 2008.
[39] F. Gatta, E. Sacchi, F. Svelto, P. Vilmercati, and R. Castello, "A 2-dB noise figure 900-MHz differential CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 36, no. 10, pp. 1444–1452, Oct. 2001.
[40] R. G. Carvajal *et al.*, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 52, no. 7, pp. 1276–1291, Jul. 2005.
[41] K. Allidina and M. N. El-Gamal, "A 1V CMOS LNA for low power ultra-wideband systems," in *15th IEEE International Conference on Electronics, Circuits and Systems, 2008. ICECS 2008*, 2008, pp. 165–168.
[42] W. Zhuo, S. Embabi, J. P. de Gyvez, and E. Sanchez-Sinencio, "Using capacitive cross-coupling technique in RF low noise amplifiers and down-conversion mixer design," in *Proceedings of the 26th European Solid-State Circuits Conference*, 2000, pp. 77–80.
[43] F. Belmas, F. Hameau, and J. Fournier, "A Low Power Inductorless LNA With Double Enhancement in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1094–1103, May 2012.
[44] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, "Noise cancelling in wideband CMOS LNAs," in *Solid-State Circuits Conference, 2002. Digest of Technical Papers. ISSCC. 2002 IEEE International*, 2002, vol. 1, pp. 406–407 vol.1.
[45] G. de Streel, D. Flandre, C. Dehollain, and D. Bol, "Towards ultra-low-voltage wideband noise-cancelling LNAs in 28nm FDSOI," in *2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S)*, 2015, pp. 1–2.
[46] F. Bruccoleri, E. A. M. Klumperink, and B. Nauta, *Wideband Low Noise Amplifiers Exploiting Thermal Noise Cancellation*. Springer US, 2005.
[47] A. V. D. Ziel, *Noise in Solid State Devices and Circuits*. Wiley, 1986.
[48] W. Sansen, "Distortion in elementary transistor circuits," *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 46, no. 3, pp. 315–325, Mar. 1999.
[49] I. R. Chamas and S. Raman, "Analysis, Design, and X-Band Implementation of a Self-Biased Active Feedback $_m$ -Boosted Common-Gate CMOS LNA," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 3, pp. 542–551, Mar. 2009.
[50] A. Quelen, G. Pillonnet, P. Flatresse, and E. Beigné, "A 2.5 #x03BC;W 0.0067mm2 automatic back-biasing compensation unit achieving 50% leakage reduction in FDSOI 28nm over 0.35-to-1V VDD range," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 304–306.
[51] F. Belmas, F. Hameau, and J. Fournier, "A 1.3mW 20dB gain low power inductorless LNA with 4dB Noise Figure for 2.45 GHz ISM band," in *2011 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011, pp. 1–4.

[52] M. Parvizi, K. Allidina, and M. N. El-Gamal, "An Ultra-Low-Power Wideband Inductorless CMOS LNA With Tunable Active Shunt-Feedback," *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 6, pp. 1843–1853, Jun. 2016.
[53] Z. Li, Z. Wang, M. Zhang, L. Chen, C. Wu, and Z. Wang, "A 2.4 GHz Ultra-Low-Power Current-Reuse CG-LNA With Active -Boosting Technique," *IEEE Microw. Wirel. Compon. Lett.*, vol. 24, no. 5, pp. 348–350, May 2014.
[54] M. Parvizi, K. Allidina, and M. N. El-Gamal, "A Sub-mW, Ultra-Low-Voltage, Wideband Low-Noise Amplifier Design Technique," *IEEE Trans. Very Large Scale Integr. VLSI Syst.*, vol. 23, no. 6, pp. 1111–1122, Jun. 2015.
[55] R. Fiorelli, F. Silveira, and E. Peralı´as, "MOST Moderate #x2013;Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 3, pp. 556–566, Mar. 2014.
[56] J. Zaini, F. Hameau, T. Taris, D. Morche, P. Audebert, and E. Mercier, "A tunable Ultra Low Power inductorless Low Noise Amplifier exploiting body biasing of 28 nm FDSOI technology," in *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, 2017, pp. 1–6.
[57] T. Taris, J. Begueret, and Y. Deval, "A 60 uW LNA for 2.4 GHz wireless sensors network applications," in *2011 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2011, pp. 1–4.
[58] H. Wang, L. Zhang, and Z. Yu, "A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.
[59] D. Linten *et al.*, "Low-power 5 GHz LNA and VCO in 90 nm RF CMOS," in *2004 Symposium on VLSI Circuits, 2004. Digest of Technical Papers*, 2004, pp. 372–375.
[60] S. Sen, M. Verhelst, and A. Chatterjee, "Orthogonally tunable inductorless RF LNA for adaptive wireless systems," in *2011 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2011, pp. 285–288.
[61] S. Popuri, V. S. R. Pasupureddi, and J. Sturm, "A tunable gain and tunable band active balun LNA for IEEE 802.11ac WLAN receivers," in *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, 2016, pp. 185–188.
[62] A. Slimane, M. T. Belaroussi, F. Haddad, S. Bourdel, and H. Barthélemy, "A reconfigurable inductor-less CMOS low noise amplifier for multi-standard applications," in *10th IEEE International NEWCAS Conference*, 2012, pp. 57–60.
[63] K. Ghosal, S. A. Kannan, and B. Amrutur, "A power scalable receiver front-end at 2.4 GHz," in *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, 2011, pp. 2765–2768.
[64] M. D. Souza, A. Mariano, and T. Taris, "Reconfigurable Inductorless Wideband CMOS LNA for Wireless Communications," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 64, no. 3, pp. 675–685, Mar. 2017.
[65] A. Shameli and P. Heydari, "Ultra-low power RFIC design using moderately inverted MOSFETs: an analytical/experimental study," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2006*, 2006, p. 4 pp.–.
[66] R. Fiorelli, F. Silveira, and E. Peralı´as, "MOST Moderate #x2013;Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 3, pp. 556–566, Mar. 2014.
[67] M. J. Deen and T. A. Fjeldly, *CMOS RF Modeling, Characterization and Applications*. World Scientific, 2002.
[68] E. A. Sobhy, A. A. Helmy, S. Hoyos, K. Entesari, and E. Sanchez-Sinencio, "A 2.8-mW Sub-2-dB Noise-Figure Inductorless Wideband CMOS LNA Employing Multiple Feedback," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 12, pp. 3154–3161, Dec. 2011.

[69] C. S. Chang and L. C. Guo, "Ultra-low voltage and low power UWB CMOS LNA using forward body biases," in *2013 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2013, pp. 173–176.
[70] S. Hyvonen, K. Bhatia, and E. Rosenbaum, "An ESD-protected, 2.45/5.25-GHz dual-band CMOS LNA with series LC loads and a 0.5-V supply," in *2005 IEEE Radio Frequency integrated Circuits (RFIC) Symposium - Digest of Papers*, 2005, pp. 43–46.
[71] M. Parvizi, K. Allidina, and M. N. El-Gamal, "Short Channel Output Conductance Enhancement Through Forward Body Biasing to Realize a 0.5 V 250 0.6 #x2013;4.2 GHz Current-Reuse CMOS LNA," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 574–586, Mar. 2016.
[72] H. J. Liu and Z. F. Zhang, "An Ultra-Low Power CMOS LNA for WPAN Applications," *IEEE Microw. Wirel. Compon. Lett.*, vol. 27, no. 2, pp. 174–176, Feb. 2017.
[73] H. Wang, L. Zhang, and Z. Yu, "A Wideband Inductorless LNA With Local Feedback and Noise Cancelling for Low-Power Low-Voltage Applications," *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 57, no. 8, pp. 1993–2005, Aug. 2010.
[74] T. Taris, A. Mabrouki, H. Kraimia, Y. Deval, and J. B. Begueret, "Reconfigurable Ultra Low Power LNA for 2.4GHz Wireless Sensor Networks," in *2010 17th IEEE International Conference on Electronics, Circuits, and Systems (ICECS)*, 2010, pp. 74–77.
[75] H. Lee and S. Mohammadi, "A 3GHz subthreshold CMOS low noise amplifier," in *2006 IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006, p. 4 pp.–.
[76] M. K. Raja, X. Chen, Y. D. Lei, Z. Bin, B. C. Yeung, and Y. Xiaojun, "A 18 mW Tx, 22 mW Rx transceiver for 2.45 GHz IEEE 802.15.4 WPAN in 0.18- #x00B5;m CMOS," in Solid State Circuits Conference (A-SSCC), 2010 IEEE Asian, 2010, pp. 1–4.

RESUME

CONCEPTION DE CIRCUITS RADIOFREQUENCE RECONFIGURABLE EN TECHNOLOGIE FD-SOI POUR APPLICATIONS INTERNET DES OBJETS (IOT)

La pénétration importante d'objets communicants dans notre vie quotidienne révèle des défis important quant à leur développement. Notamment l'explosion d'applications multimédia sans fil pour l'électronique grand public fait de la consommation électrique une métrique clef dans la conception des dispositifs portables multimodes sans fil.

Cette thèse s'inscrit dans le contexte de l'internet des objets. A l'heure où les objets du quotidiens communiquent et interagissent entre eux, ce nouveau monde connecté impose de nouvelles contraintes aux concepteurs de circuits intégrés. La durée de vie des batteries doit être de plus en plus élevées et le facteur de forme le plus faible possible pour permettre une dissémination plus facile dans l'environnement.

La figure suivante illustre le domaine très varié de l'Internet des objets. Que ce soit dans l'agriculture, dans les véhicules ou les bâtiments, les objets qui communiquent entre eux se multiplient jusqu'à atteindre près de 20 milliards d'objets connectés sur la planète en 2020.

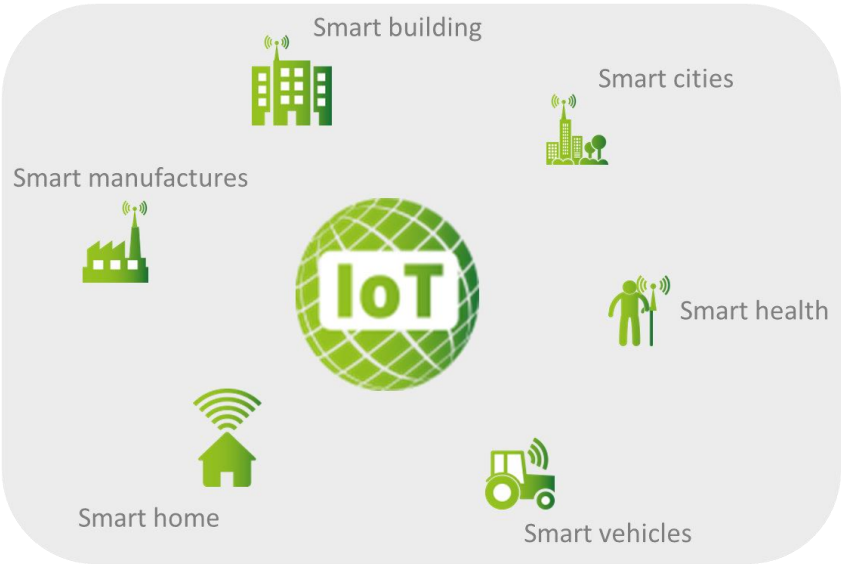


Figure 1. Domaine de l'internet des Objets

Les émetteurs-récepteurs conventionnels proposent des performances fixes et sont conçus pour respecter ces hautes performances dans toutes les conditions de communication sans fil. Cependant, la plupart du temps, le canal n'est pas dans le pire cas de communication et ces émetteurs-récepteurs sont donc surdimensionnés. En connaissant l'état du canal en temps réel, de tels dispositifs pourraient s'adapter aux besoins et réduire significativement leur consommation électrique.

Le défi consiste à respecter la Qualité de Service , ou Quality of Service (QoS) en anglais, imposée par les différents standards de communication. Afin de rester compétitifs, les émetteurs-récepteurs adaptatifs doivent donc proposer une même QoS que ceux déjà disponibles sur le marché. Ainsi, ni la portée de communication ni le temps de réponse ne peuvent être dégradés.

Basé sur ces exigences, cette thèse propose une technique d'adaptation pour la conception d'un récepteur reconfigurable qui fonctionne à la limite des performances nécessaires pour recevoir le signal utile. Ainsi, le récepteur proposé est toujours au minimum de consommation électrique tout en garantissant la bonne qualité de service. Ceci permet alors de multiplier la durée de vie de sa batterie par un facteur 5.

La Figure 2 présente le récepteur reconfigurable qui est proposé dans cette thèse. L'efficacité énergétique entre le niveau de hautes performances et le mode très faible consommation est maximisée (-85% de consommation). Cette efficacité énergétique permet de gagner un facteur 5 sur la durée de vie de la batterie du récepteur.

De plus, trois modes de fonctionnement est proposé car il est démontré dans la thèse que c'est le meilleur compromis entre la complexité de conception de circuits reconfigurable et le gain sur la durée de vie totale de la batterie.

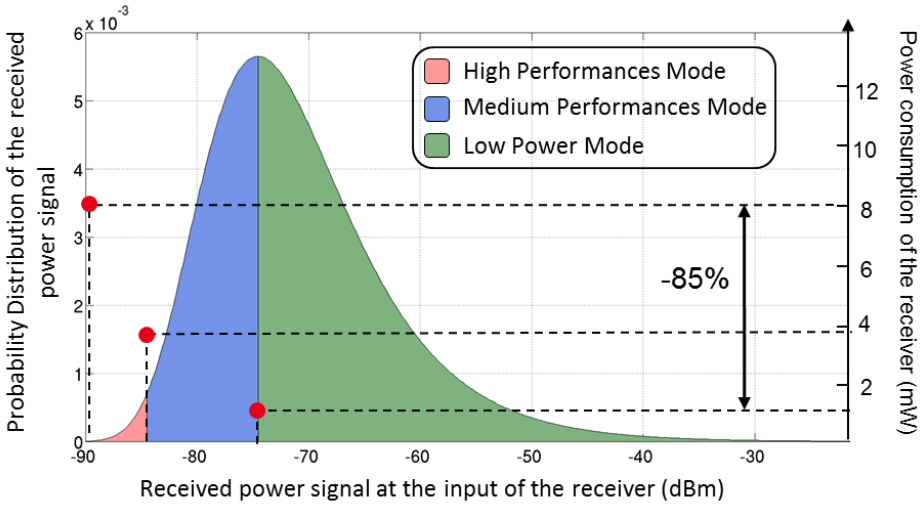


Figure 2. Récepteur reconfigurable proposé.

Ensuite, une étude système a été réalisée sur la base d'un bilan de liaison radiofréquence par simulation sous le logiciel Matlab et basée sur la chaîne de réception telle que présentée en Figure 3. Cette première approche a eu pour but de proposer une méthodologie de conception d'un récepteur adaptable avec l'état du canal de transmission.

L'objectif de ce bilan de liaison a été de déterminer les meilleures performances de l'amplificateur faible bruit, le premier bloc traversé par le signal utile provenant de l'antenne de réception.

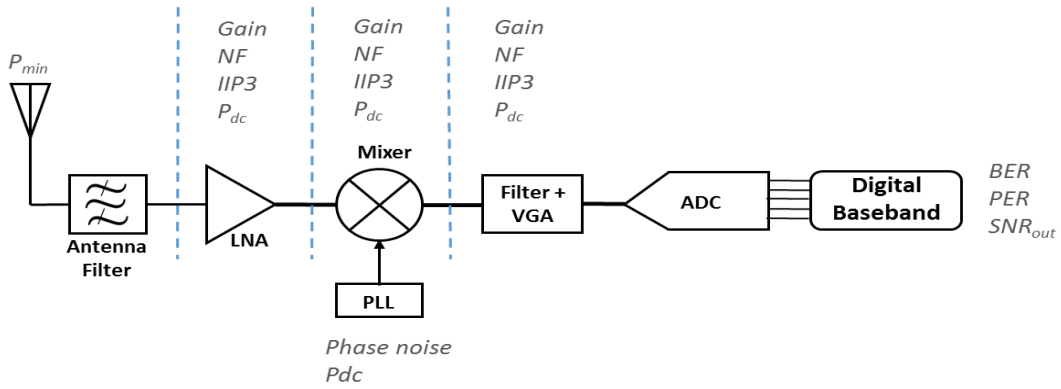


Figure 3. Chaîne de réception.

Cette adaptabilité est démontrée ensuite côté circuit par la conception d'un LNA (Amplificateur Faible Bruit) dont les performances sont reconfigurables. En effet, en tant que premier élément de la chaîne de réception, le LNA limite le récepteur en termes de sensibilité. Ces travaux exploitent la technologie FD-SOI (Fully Depleted Silicon-On-Insulator) pour, d'une part, réduire la consommation du LNA et d'autre part, ajouter de la reconfigurabilité à ce même circuit.

Un premier circuit non reconfigurable est proposé dans la thèse. Il utilise la technologie FD-SOI pour minimiser la puissance consommée par l'amplificateur faible bruit. Une nouvelle technique pour diminuer la tension d'alimentation en utilisant la polarisation par la grille arrière est proposée dans cette thèse.

Ensuite, une technique innovante pour ajouter de la reconfiguration dans l'amplificateur faible bruit est proposée. En utilisant une technique de changement de zone de polarisation de chaque transistor à l'aide de la grille arrière des transistors FD-SOI, l'amplificateur faible bruit est capable d'adresser les trois modes de fonctionnement. De plus, cette technique permet d'optimiser le compromis performances versus puissance consommée.

La Figure 4 présente l'amplificateur faible bruit reconfigurable dans son mode très faible consommation. Deux des six transistors sont en mode très forte inversion alors que les quatre autres transistors sont en polarisation sous le seuil. Ce changement de polarisation est réalisé à l'aide de la grille arrière des transistors FD-SOI.

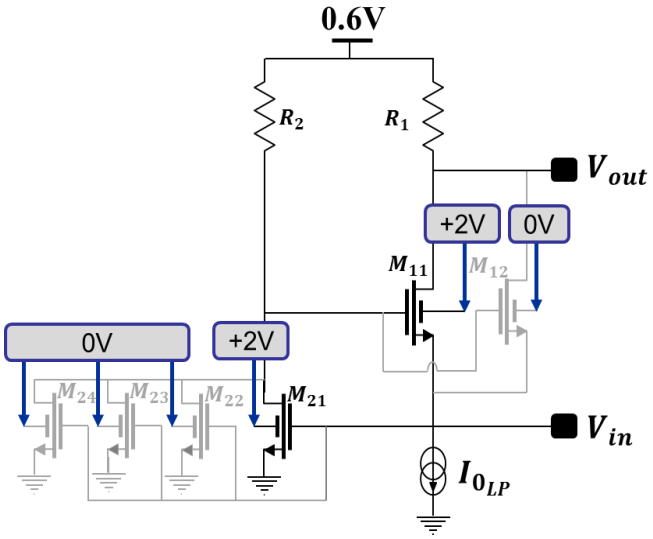


Figure 4. Amplificateur Faible Bruit reconfigurable proposé.

L'ensemble des performances des trois modes de fonctionnement de l'amplificateur faible bruit sont résumées sur la Figure 5 ci-après. La figure de mérite (FoM) choisie est dépendante du gain, de la bande passante, de la surface du circuit, de la consommation, du bruit et de la linéarité du circuit. Le circuit final proposé présente les meilleures figures de mérite dans les trois modes de fonctionnement.

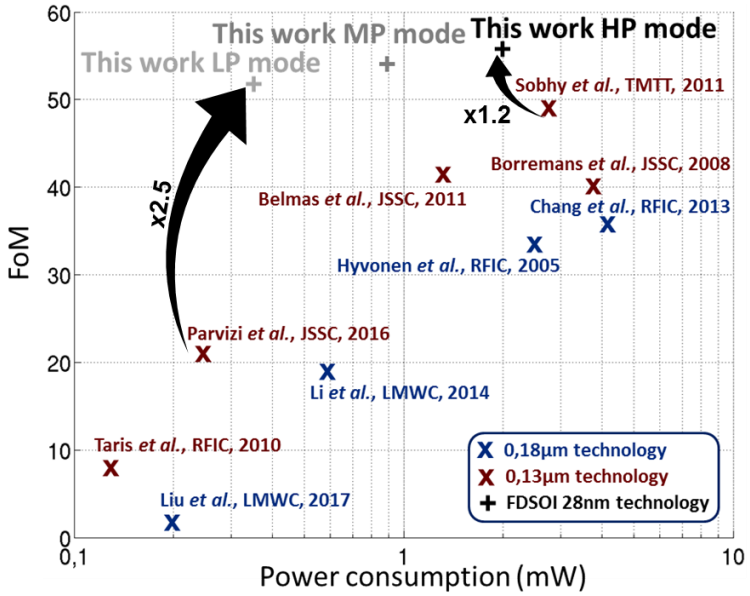


Figure 5. Placement dans l'état de l'art d' l'amplificateur faible bruit proposé.

Cette thèse présente la conception d'un amplificateur faible bruit reconfigurable sur trois modes de fonctionnement optimisés. Elle pose les premières briques de la conception d'un récepteur entièrement reconfigurable pour l'internet des objets. La conception des autres blocs constituant la chaîne de réception ainsi que les autres fonctionnalités d'un capteur pour internet des objets restent à développer pour valider la preuve de concept proposée dans cette thèse.