Control and analysis of DC Microgrid with multiple distributed generators

Nanfang Yang

SPIM

Thèse de Doctorat

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Nanfang Yang

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Control and Analysis of DC Microgrid with Multiple Distributed Generators

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Thesis Committee:

Dr. Babak Nahid-Mobarakeh	Université de Lorraine
Prof. Yvon Besanger	Institut national polytechnique de Grenoble
Prof. Mohamed Gabsi	Ecole normale supérieure de Cachan
Prof. Weiguo Liu	Northwestern Polytechnical University
Prof. Lhassane Idoumghar	Université de Haute-Alsace
Prof. Abdellatif Miraoui	Université de technologie de Belfort-Montbéliard
Dr. Damien Paire	Université de technologie de Belfort-Montbéliard
Dr. Fei Gao	Université de technologie de Belfort-Montbéliard

Abstract

The direct integration of renewable energy resources to the utility grid is pretty tough due to their intermittent feature and dispersed nature. Microgrid is one promising approach to gather the local distributed generators (DGs), supply local loads as well as exchange power with the utility grid as a controllable unit. This local-generation-local-consumption mode is able to avoid the long distance power transmission, thus can benefit a higher efficiency. DGs can be connected to a common DC-bus via power converters to form a DC microgrid. The control aim is to make the multiple DGs share the load properly as well as to maintain the voltage stability. This dissertation discusses the modeling, analysis and control of DC microgrid with multiple DGs to improve its performances in steady-state and dynamic state.

Although the traditional master-slave control can achieve good voltage regulation and equal load sharing, its dependencies on high-bandwidth communication and master unit reduce significantly the system reliability. On contrary, droop control provides a distributed control scheme without the need of communication. As an output impedance programming method, voltage control and load sharing are achieved automatically according to DGs' output impedances. Thus it is sensitive to the connecting cable impedances and the nominal voltage reference offsets in low-voltage applications.

In steady-state, a compensation method using common current reference is proposed to enhance DC-bus voltage and load sharing performance simultaneously. The margins of the voltage compensation coefficients are analyzed by using small-signal stability tests. Simulations in MATLAB/Simulink and experimental tests in the laboratory test bench are carried out to verify the effectiveness of the proposed method.

To investigate the dynamics of the multi-time scale DC microgrid, i.e., DGs have different dynamics, a series connection of virtual inductor and droop resistor is introduced to represent the DG under droop control. Then a comprehensive model (CM) of the DC microgrid can be obtained. Using lumped parameters to represent the distributed parameters, the reduced 4th-order model (R4M) and the reduced 2nd-order model (R2M) can be developed. Small-signal and large-signal stability tests discover that these reduced order models are ineffective to represent multi-time scale systems. Therefore, a novel reduced-order multi-time scale model (RMM) is proposed, which groups the DGs with similar time constants together to form an equivalent DG, and combines the equivalent DGs to build RMM. It reduces significantly model complexity as well as keeps major time scale information.

The effectiveness of the proposed RMM is confirmed by numerical simulations and experimental tests.

A voltage control based on Active Disturbance Rejection Control (ADRC) is introduced to realize time scale droop control of the DG. It not only simplifies the design of DG's dynamics by adjusting the bandwidths of the observer and controller, but also robust to system model errors. Then a general procedure to calculate the range of the DC-bus capacitance for a stable multi-time scale DC microgrid is discussed based on the new parameterized RMM (N-RMM). Simulations and experiments are conducted to verify the proposed implementation method.

Résumé

L'intégration des sources d'énergies renouvelables sur le réseau électrique est complexe en raison de leur nature intermittente et décentralisée. Le micro-réseau est une approche prometteuse pour interconnecter des générateurs distribués (DGs) locaux, alimenter des charges locales et également échanger de l'énergie avec le réseau électrique de manière contrôlée. Ce mode de production/consommation locales permet d'éviter la transmission d'électricité sur de longues distances, et implique donc une plus grande efficacité. Les DGs sont connectés à un bus continu via des convertisseurs de puissance pour former un micro-réseau continu. Le contrôle du micro-réseau continu permet que les DGs se répartissent l'alimentation des charges et qu'ils maintiennent également la tension du bus continu. Dans ce mémoire, nous examinons la modélisation, l'analyse, et le contrôle d'un micro-réseau continu constitué de multiples DGs pour améliorer ses performances statique et dynamique.

Même si la commande utilisant la méthode maître-esclave permet d'obtenir une bonne régulation de la tension et du partage de charge, ses dépendances vis-à-vis d'une communication à large bande et du contrôleur maître réduisent la fiabilité du système. En revanche, la commande du statisme (droop control) donne une méthode de contrôle distribué sans avoir besoin de moyens de communication. Cependant, comme le procédé de programmation de l'impédance de sortie, la régulation de la tension du bus continu et le partage de charge sont effectués automatiquement selon la valeur de l'impédance. Ainsi, cette méthode est sensible à l'impédance du câble de liaison et à la référence de tension nominale dans les applications basse tension.

À l'état statique, une nouvelle méthode utilisant une référence de courant commune est proposée pour la compensation de la régulation de la tension et le partage de la charge. Les marges des coefficients de compensation sont analysées en menant des tests de stabilité aux petits signaux. Des simulations dans MATLAB/Simulink et des expériences sur le banc d'essai en laboratoire sont menées pour tester la méthode proposée.

Une inductance virtuelle et une résistance de statisme connectées en série sont utilisées pour modéliser la dynamique du DG, afin d'étudier le micro-réseau à plusieurs échelles de temps à l'état dynamique. Certaines méthodes de réduction de modèles sont adoptées pour obtenir le modèle réduit à l'ordre 4 (R4M) puis le modèle réduit à l'ordre 2. Cependant, les essais de stabilité petits signaux à l'aide du tracé des valeurs propres, et de stabilité grands signaux par multi-modélisation montrent que la méthode traditionnelle de réduction de modèles est inefficace lorsque les systèmes à plusieurs échelles de temps sont étudiés. Par conséquence, un nouveau modèle à plusieurs échelles de temps

et ordre réduit (RMM) est développé, il regroupe les DGs avec des échelles de temps similaires pour former un DG équivalent. Cette méthode diminue considérablement la complexité du modèle et garde également l'information temporelle. L'efficacité de RMM proposé pour l'analyse de stabilité est confirmée par des analyses numériques et des expériences sur banc d'essai dans le laboratoire.

Une méthode à base de contrôle de rejet actif de perturbation (ADRC) est détaillée pour mettre en œuvre le contrôle local de la tension des DGs avec multiples échelles de temps. Cette méthode permet de simplifier la conception de la bande passante du système en ajustant la bande passante de la commande et celle de l'observateur. Une procédure pour concevoir un micro-réseau continu stable à plusieurs échelles de temps est ensuite présentée, basée sur le nouvel RMM paramétré. Des simulations et des expériences sont menées pour vérifier la méthode proposée.

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Chapter 1 Introduction

1.1 The microgrid

With the gradually exhaustion of fossil fuels, the increasing concern of environmental pollution and the requirement of stable and high quality power supply, the demand of a flexible power system to supply clean and reliable electricity is becoming emergent. The intermittent nature of renewable energy resources (e.g., wind power and solar energy) makes it difficult to connect them directly to the utility grid. Therefore, the new generation power system must be flexible to integrate renewable energy resources and also reliable.

The microgrid has become a popular solution to harness the renewable energy resources and enhance the power system stability. According to the definition of U.S. Department of Energy (DoE), a microgrid is:

> A group of interconnected loads and distributed energy resources within clearly defined electrical boundaries that acts as a single controllable entity with respect to the grid. A microgrid can connect or disconnect from the grid to enable it to operate in both grid-connected and island-mode. [1]

Furthermore, this local-generation-local-consumption mechanism can significantly reduce the long distance power transmission loss, thus benefits a higher efficiency.

The microgrids can be distinguished into AC microgrids and DC microgrids. Most of the discussions about the AC versus DC include a retelling of the famous technical and commercial battle between Edison and Westinghouse/Tesla [2]. The success of Tesla leaded to the domination of AC in present power grid. The DC grid was constrained by the problem of commutation and the nonavailability of equipment for voltage transformation and the interruption of currents at that time [3]. Nowadays, the development of modern power electronics gives DC another chance to rebirth, and a lot of High Voltage DC (HVDC) power transmission systems have been constructed all over the world since 1954 [3].

Although most microgrids adopt AC like the conventional power system (e.g., the U.S. CERTS microgrids test bed [4], the EU More microgrids project in Kythnos island [5], and the Hachinohe project developed by NEDO in Japan [6]). DC microgrids can work better with the connection of DC sources (e.g., photovoltaic (PV) system, fuel cell (FC), and secondary battery [7], [8]). Compared to the AC microgrid, the DC microgrid can achieve:

1) Higher efficiency. From the view of consumption, lots of electronic loads, e.g., LED lights, computers, and adjustable speed drives in household equipment, require DC power. When supplied by DC power, the AC-DC rectifiers and power factor corrections of the loads can be thrown off, thus the average input loss can decrease from 32% down to 10% [9]. From the view of generation, the DC-AC inverters can be abandoned for DC sources to receive more energy saving. The analysis of a building power grid shows that the whole losses of DC grid are around 15% lower than that of AC system during one year [10]. Besides, the reduction of power conversion stages not only reduce the losses but also costs.
2) Higher reliability. DC microgrids can easily form redundant structures; e.g., the ring-type microgrid [11], [12]. This will give more flexibility to realize fault tolerance and isolation.
3) Free of frequency issue and synchronization. DC microgrids can get rid of some troublesome things in AC grid; e.g., the frequency and phase regulation, the reactive power control, and the synchronization. The DC microgrids can be easily and conveniently interconnected or connected with other grids [8], [13].
4) Free of three-phase unbalance. DC microgrids uses only positive and negative power lines, which can avoid the three-phase unbalance in AC grid when large single phase loads exist [14].
5) Easy connection of energy storages. The energy storages such as batteries can be directly connected to the DC-bus or through bi-directional DC-DC converter in DC microgrids; while in AC system a more complex interface with AC-DC rectifier and DC-AC inverter is required [15].

In our view, the DC microgrids research is not to replace the whole traditional AC grid but to supply an efficient and effective supplementation for the traditional AC grid. Moreover, the DC microgrid is more suitable for several applications such as data center power supply [15], [16], marine power system [17]–[20], railway power system [21], rural electrification [22] and building power solution [2], [23].

1.2 Research scope

In the structure of DC microgrids, the DC-bus can adopt the unipolar structure with only 2 wires or the bipolar structure with 3 wires [7]. The 380 V DC is commonly recommended for the DC-bus in U.S. to connect to the 120 Vrms AC utility grid directly through a front-end rectifier [23]; while in other countries using 220 Vrms AC, the voltage level higher than 600 V DC is usually adopted [24]. On the other side, the bipolar bus voltage ±170 V DC is also investigated by [8] to be compatible with the 100 Vrms AC utility grid in Japan. In the application of railway electrification in Spain, the

24 kV DC-bus voltage is considered in [21]. Other low-voltage distribution levels (e.g., 48 V) can also be applied to the power supply of building [23].

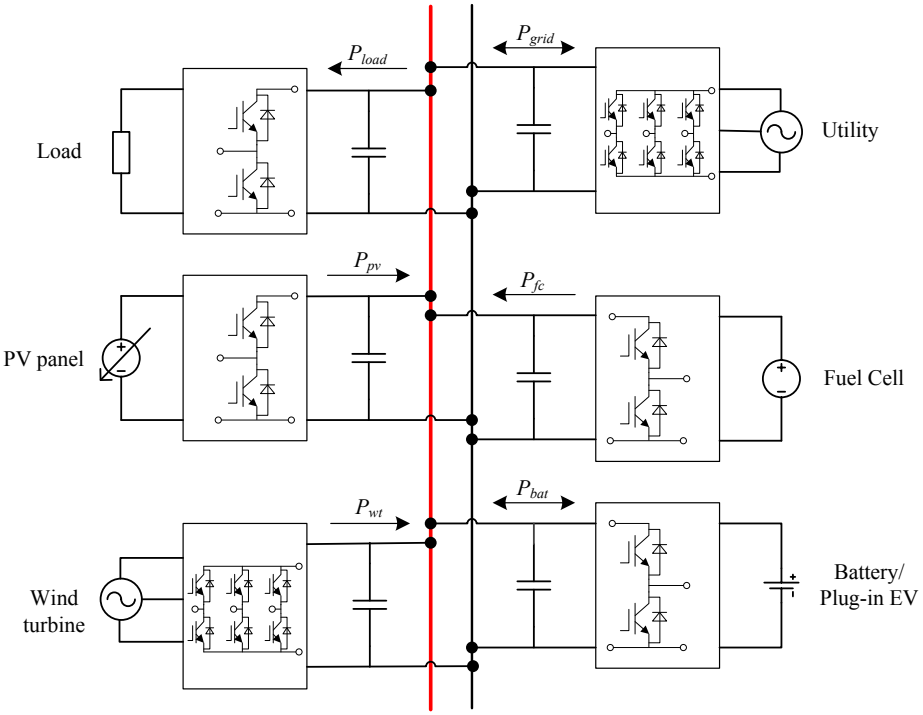


Figure 1.1 The diagram of a typical single bus DC microgrid with multiple DGs

The connections of distributed generators are very flexible, and this makes the topologies of DC microgrids also varied. The topology can be radial type, ring type [11], [12] or zonal form [17]–[20], [25]. These complicated topologies are all based on the basic single bus diagram [26], [27] as shown in Figure 1.1. In the typical microgrid, the utility grid, PV panels, wind turbines, FCs, and batteries (or plug-in electric vehicles (EVs)) are connected via power converters to the common DC-bus. The PV panel or wind turbine under Maximum Power Point Tracking (MPPT) is considered as non-dispatchable generator. The others that adjust their outputs according to the DC-bus condition are dispatchable generators (also referred as slack terminals in [28]). The PV panels or wind turbines may participate into voltage control when the DC-bus voltage is too high (e.g., the system have surplus power), and they are considered as dispatchable generators in those cases.

The DC microgrid can operate autonomously (island-mode) or with the support of the utility grid (grid-connected mode). But the distinction between these two operation modes is not considered in this dissertation. The utility grid interfaced by power converters can also be considered as a normal dispatchable distributed generator when it is connected, and this makes the grid-connected mode can also be viewed similar as the island-mode with one more generator plugging in.

The DC microgrid can be abstracted into the system where multiple generic dispatchable distributed generators in parallel supply power to the net load. The net load includes the loads and the non-dispatchable generators. To simplify the expression, the after-mentioned 'distributed generators (DGs)' exclusively represent the dispatchable distributed generators.

This dissertation limits the topic into the coordinate control of the multiple DGs in DC microgrids, to maintain the system stability, voltage regulation and load sharing in both steady-state and dynamic state. The specified control strategies for renewable energy resources and storage systems, as well as the protection [29], feasibility [30] and economical optimization are not the main topics of this dissertation.

1.3 Literature review

In this section, the previous researches in literature about the control, modeling and analysis of DC microgrids with multiple DGs are sorted by their topics and discussed in order to obtain a general review.

1.3.1 Hierarchical control structure

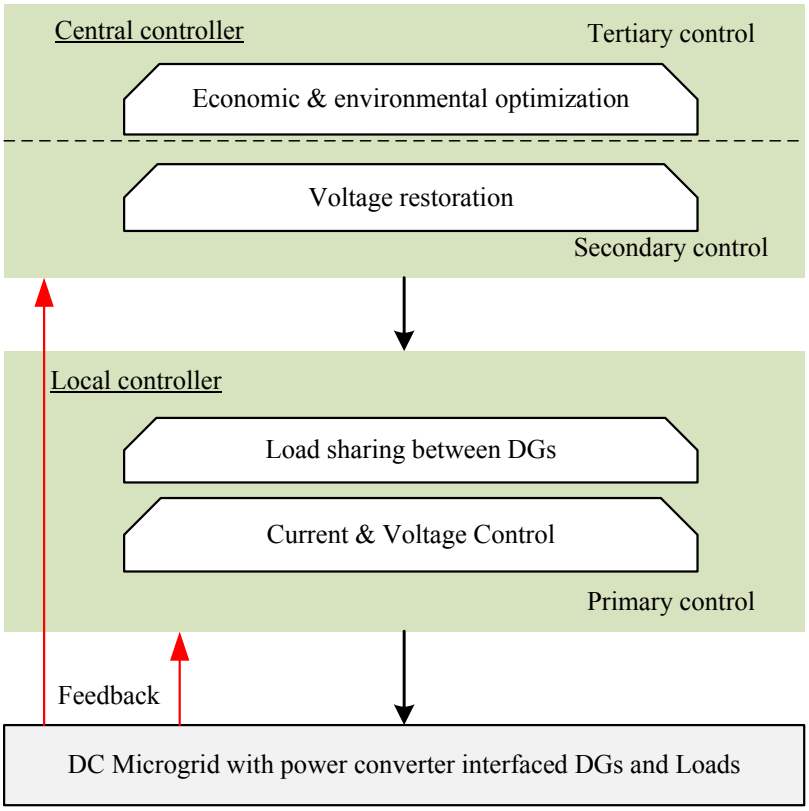


Figure 1.2 Hierarchical control structure for DC microgrids

Similar as the hierarchical control structure used in the traditional AC power system, the hierarchical control layers can be defined for DC microgrids [31]–[38], as shown in Figure 1.2. The three control levels from bottom to top are defined as: primary control, secondary control and tertiary control, respectively. The primary control located in the local controller is responsible for the current control, voltage control and also load sharing, while the secondary located in the central controller focus on the DC-bus voltage restoration as well as load sharing of the DGs sometimes. The tertiary control in the central controller takes charge of economic and environmental optimizations of the whole energy system and the connection with the utility grid [39].

Usually the primary control (in local controller) adopts the droop control method, and the secondary control is a common DC-bus voltage controller to restore the voltage deviation introduced by droop control [32]. In this configuration, the low-bandwidth communication is required to transfer the local measurements to the central controller and pass the references from the remote central controller to the local controllers.

The major control objective of DC microgrids is to obtain low voltage variation and equal load sharing in per unit among the DGs [33], [40]. The control methods fall into two major categories: active current sharing scheme [41] and droop control [31], [42].

1.3.2 Active current sharing versus droop control

A. Active current sharing

The principle of active current sharing is to generate a voltage compensation based on the error of output current of individual module and the overall average or maximum current reference, and then use it to compensate the nominal voltage reference in each module [43]. The mostly referred methods are average current sharing and master-slave current sharing [41], [44].

In the average current sharing, an analogue sharing bus is utilized to interconnect all the paralleling modules. The average current signal from the sharing bus is fed back and compared to the individual measured module current, then the generated error is used to adjust the voltage or current reference such that equal load sharing can be achieved.

The popular master-slave control uses one module to operate as the master, which is responsible for voltage control, while other slaves trace the output current of the master or the references given by the master, as shown in Figure 1.3. Some derivations of the master-slave control such as dedicated master, rotating master and automatic master can reduce the system dependency on the specified master [43].

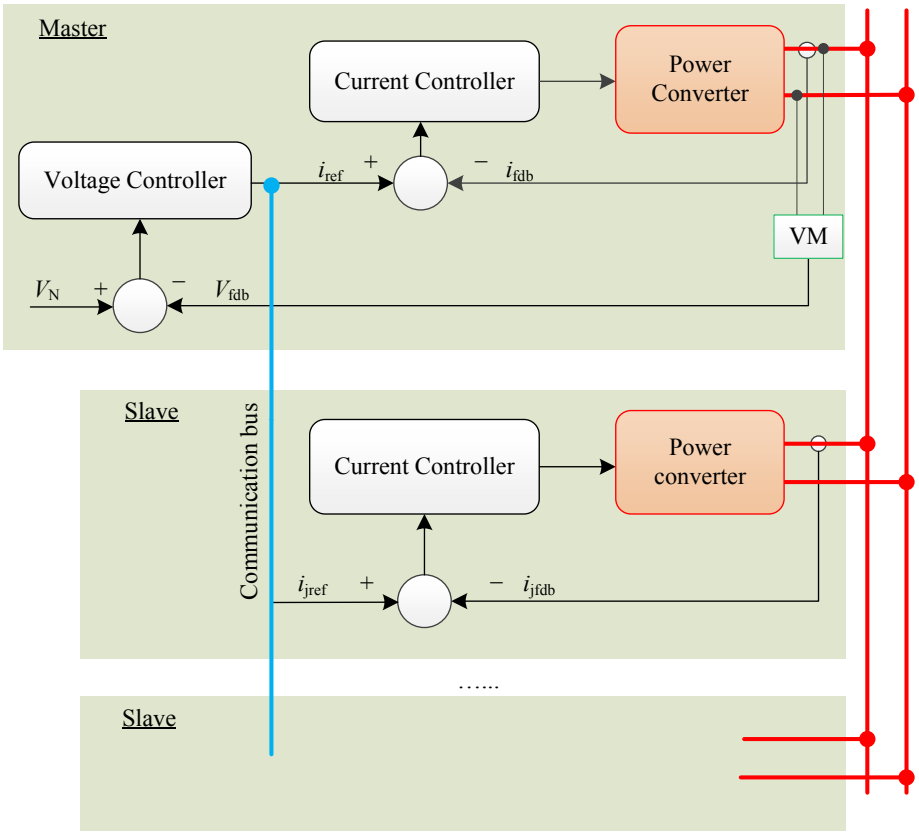


Figure 1.3 Master-slave control structure

Although the master-slave control can achieve good voltage regulation and load sharing performance, the main drawback is that the reliability of the entire system is highly depended on the master and the high-bandwidth communication [45]. The failure of the master or communication will result in the outage of the entire system.

B. Droop control

Droop control is a kind of output impedance programming method, and the output voltage linearly decreases with the output current/power. In this distributed control scheme, all units adopt same control structure and participate into the DC-bus voltage regulation, as shown in Figure 1.4. The power balance is achieved automatically, and the load is shared among the connected DGs according to their output impedances. Compared to the master-slave control, this distributed control scheme can enhance system reliability by eliminating the dependencies on the specific master unit and the high-bandwidth communication. The redundancy, modularity, and size reduction designs can be achieved conveniently by this distributed control [46].

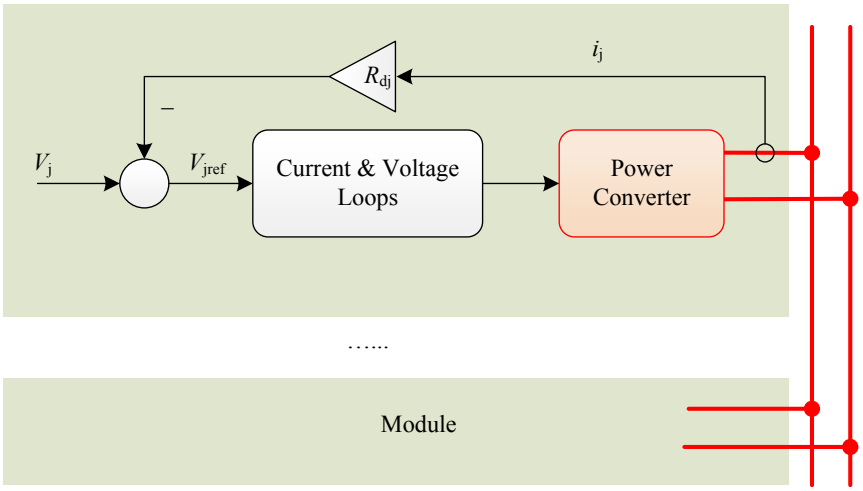


Figure 1.4 The structure of droop control

In the traditional three-phase AC grid, the real power-frequency ($P-f$) droop and reactive power-voltage ($Q-V$) droop laws are deduced from the assumption that the transmission lines are mainly inductive [47]. Similarly, the power-voltage droop ($P-V$) can be adopted for the control of DGs in DC grid [48]. It can be implemented by using DC-bus signaling [34], [49]–[53], in which the line resistances and voltage sensing errors are omitted, and the DC-bus voltage is regulated in a relatively large range. The DC-bus voltage, indicating the load condition of the system, can be utilized as the index of different control modes, such that some mode-adaptive control structures can be realized [16], [24], [54]. The voltage control right is hold by one unit, and it transfers to another unit when the DC-bus voltage level changes; e.g., the battery controller will takes charge of the voltage control instead of the grid converter controller when the utility grid is not available and the DC-bus voltage drops to a certain value. However, the design of suitable voltage variation bands is not an easy task. Large voltage band leads to poor voltage regulation while small voltage band may result in control oscillation between different modes. The DC-bus voltage level bands need to be designed properly to avoid oscillation between control modes as well as obtain good voltage performance.

1.3.3 Voltage regulation and load sharing

Like the problem faced in the reactive power control of low-voltage AC grids [55], the effects of transmission line resistances in low-voltage DC applications cannot be omitted. The unequal line parameters will cause serious load sharing problem, especially when the droop resistance is small. Not only the voltage drops through the transmission lines can cause unequal load sharing, the nominal voltage reference offsets in local voltage control can also lead to the same problem. The local voltage control loops require the feedback sensing signal, and the unavoidable measurement errors in the voltage feedback control can also lead to load sharing performance deterioration [40].

The challenge is how to compensate the voltage deviation caused by the droop control, and the load sharing error introduced by the unequal line parameters or nominal voltage reference offsets. The adjustment of the droop resistance cannot satisfy simultaneously these two requirements. The choice of droop resistance needs to consider the trade-off between voltage regulation and load sharing performance. Higher droop resistances lead to better load sharing but larger DC-bus voltage variation, while lower droop resistances result in poor load sharing but smaller DC-bus voltage variation [56]. The impact of the connecting line voltage drops on the load sharing also depends on the topology of the DC microgrid, the location of the load, the transmission line parameters and voltage droop constants [11], [40], [45]. Therefore, the compensation methods based on full knowledge of the system [57] is not suitable for the systems with varied structure.

A. Voltage regulation

To reduce the voltage deviations, a hierarchical structure with low-bandwidth communication is proposed in [31], [58] to adjust nominal voltage references in a secondary central controller. The second controller can eliminate the voltage deviation, but not the load sharing error, because the voltage error compensation feeding to each unit is the same. Another one with a supervisory control [36] is proposed to adjust the droop constants (or droop resistors) instead of the nominal voltage references in the supervisory controller. A disturbance observer based voltage control method is proposed by [59] to improve the quality of the DC-bus voltage. Their common shortcoming is that, the enhanced performance relies on the upper layer controller thus requires an additional central controller and communication line.

To avoid the central controller, distributed methods with dedicated low-bandwidth communication are proposed. Local current/voltage is shared with this communication line and the common average current or average voltage through the whole system can be generated in each local controller. The common average current [33], [60] or average voltage [61], can represent the load condition, and is used to generate voltage compensations in local control. They can be seen as the distributed form of secondary controller, using the common average current or average voltage instead of the voltage at the common coupling point.

Another distributed method using adaptive droop constants (also referred as gain-scheduling) in local controller is proposed by [62], [63] in a bipolar DC microgrid, in which the droop constant is adjusted in the local control according to the output power, so as to obtain a better voltage regulation. Though the DC-bus voltage performance can be improved, the unequal load sharing problem is not considered as well as the effect of unequal line parameters.

B. Steady-state load sharing

The aims of load sharing is to improve the global efficiency of the system [64], [65], obtain equal converter temperature [66], [67], maintain equal State-of-Charge (SOC) for battery packs [36], [37], [68], perform same amount of head room for multiple power converters [69], or share equal portion of power according to their rated volumes [33], [57], [61], [70].

The most intuitive method to reduce the load sharing error is to calculate droop resistances according to the detailed system parameters especially the transmission line impedances [71], [72], or design load sharing compensations by detailed line parameters [57], [73]–[75]. Although no additional communication is needed for these methods, the main drawback is the requirement of full knowledge of line parameters throughout the system. In [76] line resistances estimation is introduced instead of using the pre-calculated values. It requires the microgrid operating in grid-connected at first so as to estimate the line resistances, and then these values can be used in the islanding mode.

The load sharing error caused by nominal voltage reference offsets can be represented by circulation currents among the units under no-load condition. An iterative method is proposed to adjust the nominal voltage references during no-load condition to obtain zero circulation currents [70]. This method requires all units start from no-load condition at the same time. A similar process is also proposed in [77], [78] to adjust the droop constants during initial process. However, these methods will lead to the loss of plug-and-play capability (i.e., flexibility) and also the influence of unequal transmission line impedances to load sharing is not properly considered.

A distributed compensation structure with low-bandwidth communication is proposed in [61]. The voltage and current information are shared though the whole microgrid by using this communication. The load sharing error is compensated by the error of local current and the average common current in the local control. The local current is controlled by a PI controller or sliding-mode-controller [79], [80] to follow the common average current, such that equal load sharing can be achieved. A similar structure is adopted to compensate the DC-bus voltage using error of the common average voltage and the local output voltage. Although this structure considers the impact of unequal transmission line impedances, the tuning of the two PI type compensation controllers remains a great challenge.

In order to reduce the amount of information to exchange through the communication line, the use of regional communication is also proposed. The neighborhood current and voltage information are adopted to estimate common voltage and current through the microgrid, then these estimated values are performed as references to regulate the local control so as to obtain equal load sharing [81], [82].

To reduce the complexity of additional communication line, a communication method using the power line is proposed in [83]. In this method, the local controller injects small sinusoidal AC signals of the specific frequency into the common DC-bus in order to communicate with each other.

C. Dynamic load sharing

The previous part reviews the steady-state load sharing of DGs, where the dynamics of the DGs are not considered. However, if the dynamics of the multiple type energy resources in the DC microgrid are largely different, much attention needs to be paid on the dynamic load sharing performance. The dynamic load sharing deals with the load sharing in frequency spectrum not in power scale, so as to respect the dynamics of energy resources; e.g., using the FC to response high dynamic loads will reduce its life-span [84], and the grid converter requires a smooth power exchange to eliminate the influence of microgrid on utility grid [28].

In [27], [28], a grid-connected DC microgrid with wind turbine and an energy storage system is studied. The grid converter is designed with a small gain to have slow dynamic response while the energy storage converter is controlled with large gain to have high dynamic response. The high frequency power due to load or wind turbine will be supply or absorbed by the energy storage. The similar control method is also applied to the DC grid with integration of PV panels [85]. Another method using forward path low-pass filter is proposed by [26], [86]. The cut-off frequency of the low-pass filter can be utilized to tune the dynamics of the DGs. The frequency responses of different DGs are also studied in the design of droop constants for a multi-terminal Voltage Source Converter HVDC (VSC-HVDC) grid in [71].

1.3.4 Load side control

In the finite volume microgrid, when the generators cannot supply sufficient power for all the loads, some load side control can be performed to guarantee the supply for the sensitive loads and maintain system stability. The load side control can be realized by load shedding according to the priorities [87], reducing the non-sensitive load when the DC-bus voltage drops [88], or change the feature of the load to maintain system stability during the transients (e.g., maintain constant input impedances for the constant power loads [87]).

A. Steady-state control

A priority based load shedding algorithm is proposed in [87]. Some voltage levels are defined that when the operating voltage falls under these voltage limits, the loads with lower priority will be shut down. Another method proposed in [88], which reduces the consumption of the controllable loads instead of shut them down; e.g., electric water heaters and the batteries are taken as controllable loads, and they are adjusted according to the DC-bus voltage level. When the DC-bus voltage falls, the electric water heater reduces its power, while batteries increase their discharging powers or decrease their charging powers; when the DC-bus voltage rises, the electric water heater increases its power, while batteries decrease their discharging powers or increase their charging powers.

B. Dynamic load control

The widely used tightly controlled power electronics interfaced loads can be viewed as constant power loads (CPLs). The negative impedance feature of idea CPL will result in the instability of the system. The distributed local control method for each point-of-load (POL) converter is proposed in [87] to be functional with a power buffer, which is used as an energy assistance to support the system stability when short-term voltage sag occurs. In this way, the input impedance of the CPL will be controlled to be constant to avoid the collapse of DC-bus voltage.

1.3.5 Control oriented modeling

Lots of researches in literature study the modeling of DC microgrids or VSC-HVDC grids [89] to conduct power flow calculation and stability analysis. The structure of the DC microgrids and VSC-HVDC are similar when the inner detailed control loop is not taken into consideration.

A. Steady-state modeling

According to Thévenin theorem, the DG under droop control can be modeled as an imperfect voltage source (an ideal voltage source and a resistor in series) [11], [33], [36], [40], [50], [60], [78], [82], [86], [90]–[92]. Other non-dispatchable generators (e.g., MPPT controlled PV panels) can be modeled as current sources. Another alternative equivalent circuit in Norton form can also be applied, in which the DG is represented as a current source and a resistor in parallel [90], [93]–[98]. The latter one is commonly utilized for the analysis of VSC-HVDC grids.

The steady-state model of a generic load can be expressed as the function of power in terms of voltage [99]:

$$P(V) = A_{CR}V^2 + A_{CC}V + A_{CP} \tag{1.1}$$

where A_{CR} is the Constant Resistive load coefficient, A_{CC} is the Constant Current load coefficient, and A_{CP} is the Constant Power load coefficient.

The steady-state model of a DC grid is constructed in [93] with the connecting cables represented by lumped resistors, to analyze the steady state power flow, and optimize the selection of droop resistances. This model is also used in [78] to analyze the load sharing error among the DGs and the circulating current, as well as the voltage regulation [11].

The steady-state model can represent the DC grid in a very simple circuit, which is intuitive and convenient to the analysis of steady-state voltage and load sharing performance, but it cannot reflect the dynamic behaviors of the DGs, connecting cables, and the loads.

B. Dynamic modeling

To conduct the dynamic analysis or dynamic related analysis, the dynamic behaviors of the DGs [86] [100], the connecting cables [11], [64], [90], [97], and the loads [101] need to be considered. The

connecting cable is usually represented by the Γ or Π equivalent circuit to include its dynamics. The dynamic model of a load can be formed by the combination of the steady-state model with an input RLC filter [99].

In addition to the dynamics of the transmission lines and loads, the dynamic behaviors of DGs also need to be considered. In real applications, different kind of DGs may have largely different dynamic behaviors (also referred as multiple time or frequency scales); e.g., the grid converter connecting the microgrid and the utility grid requires a smooth power exchange, which indicates a slow dynamics [28]. FCs are usually limited to slower dynamic responses to benefit longer life-span, while the super-capacitors or batteries can be used to absorb/supply high frequency power during limited time range, which have fast dynamic responses [26]. Furthermore, the dynamics of the power converter connecting the DG can be considered and modeled as a resistor and inductance in series [100], to conduct small-signal stability tests. The dynamics of the DG can be modeled by a low-pass filter connected to the steady-state model [86], such that the analysis of load sharing in frequency spectrum can be performed.

Besides, an online impedance estimation method has been proposed by [102], which can construct the simple equivalent circuit online using the estimated impedance and conducted the calculation of stability boundaries.

In summary, the modeling and the equivalent circuit of the droop controlled DC microgrid in steady-state has been well discussed. However for the dynamic modeling, especially the dynamics of DGs, there is little research cover this issue in literature. The detailed analysis of the DC microgrid with multiple time scales still requires lots of work to be conducted.

1.3.6 Small-signal stability

Stability is the first and foremost feature that needs to be guaranteed for a real system. The introduction of the power converters into the DC microgrid, makes it largely different from traditional power system which is based on synchronous machines. Thus the stability problem of these systems need to be carefully examined.

The instability of the DC microgrid can be interpreted in two different ways. The first one states that the tightly controlled power electronic interfaced loads can be viewed as CPLs, and CPL introduces negative impedance to the system and results in instability problem during transients [103], [104]. Another one states that the stability degradation is due to the interactions among the feedback loops of the interconnected power converters [103].

A. Nyquist Criterion based method

The stability test of linear time-invariant systems can be derived in the frequency domain. It is the well-known Nyquist stability criterion, which is based on the complex analysis result of Cauchy's argument principle. The information about stability of the closed-loop system transfer function can be obtain by drawing Nyquist plot of the open-loop system transfer function [105]. The Nyquist Criterion states:

> The number of unstable closed-loop poles is equal to the number of unstable open-loop poles plus the number of encirclements of the point (-1, 0).

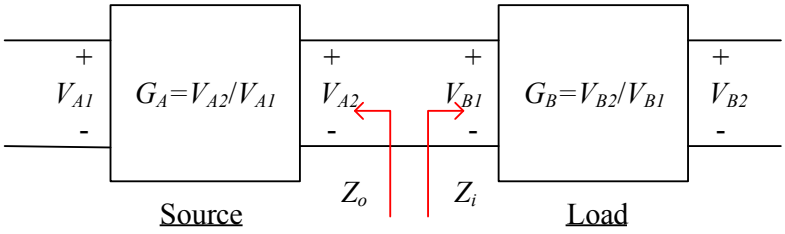


Figure 1.5 A typical two cascaded subsystems.

To apply the Nyquist Criterion to the electrical network, the source-load system is separated into two subsystems to investigate the interactions: a source subsystem and a load subsystem. A typical two cascaded subsystems is shown in Figure 1.5. The source subsystem has an input-to-output transfer function G_A and the load system has an input-to-output transfer function G_B. Then the overall input-to-output transfer function can be expressed by:

$$G_{AB} = \frac{G_A G_B}{1 + T_M} \text{ with } T_M = \frac{Z_o}{Z_i} \tag{1.2}$$

where Z_o is the output impedance of the source subsystem; Z_i is the input impedance of the load subsystem. The impedance ratio is defined as the minor loop gain T_M of the source-load subsystems [106]. Assume the subsystems are stable, then the principle of the Nyquist Criterion based methods is to develop the specifications to avoid the encirclement of the (-1, 0) point in Nyquist contour.

The Nyquist contour can be directly applied to analyze the influence of the droop constant on the system stability [107], but the more convenient method is to find out the impedance criterions. Lots of the small-signal stability analysis methods based on the Nyquist Criterion have been developed to design the input or output impedance, such as the Middlebrook Criterion (MC) [108], Gain Margin and Phase Margin Criterion (GMPMC) [106], Opposing Argument Consortium (OAC) [109], and the Energy Source Analysis Consortium (ESAC) [104], [110]. The boundaries of these stability criteria are shown in Figure 1.6, and the detailed explanations are addressed in the following sections.

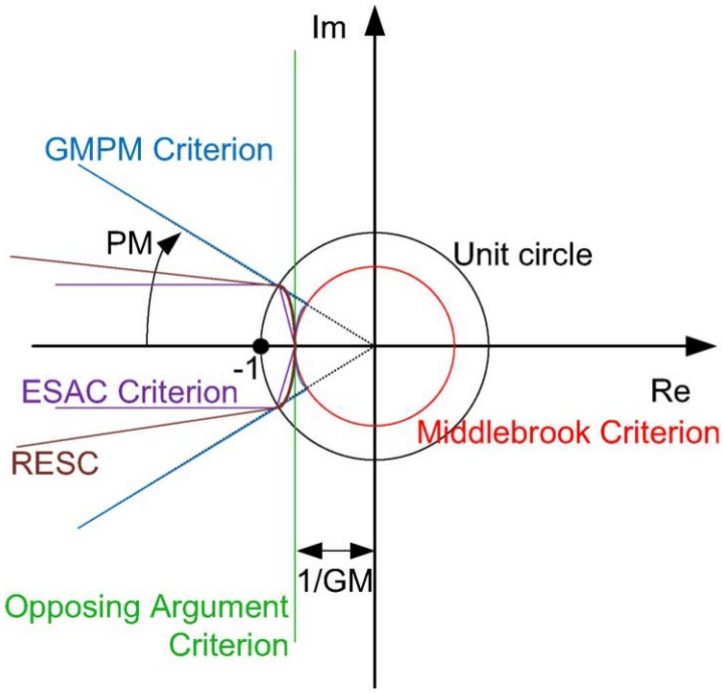


Figure 1.6 Stability criterion boundaries [103]

Middlebrook Criterion (MC)

The Middlebrook Criterion [108] gives a simple design-oriented sufficient stability specification for the output impedance of input filter $|Z_o|$ for a given load input impedance $|Z_i|$.

$$|Z_o| \ll |Z_i| \text{ or } |T_M| = |Z_o/Z_i| \ll 1 \tag{1.3}$$

Which leads to the minor loop gain always lies inside a circle with radius equals the inverse of the desired Gain Margin (GM), given by:

$$|T_M| = \left|\frac{Z_o}{Z_i}\right| = \frac{1}{GM} \text{ with } GM > 1 \tag{1.4}$$

T_M is always limited inside the unit circle, thus the encirclement of the (-1, 0) point never occurs. It gives a practical and pretty conservative method to choose the impedance of input filter Z_o, when the input impedance of the load Z_i is known. The sufficient condition is applied and when the minor loop gain lies outside the circle, the connection system may still be stable.

Gain Margin and Phase Margin Criterion (GMPMC)

MC requires the output impedance of the filter $|Z_o|$ should be smaller than the input impedance of the load $|Z_i|$ in all frequency range to maintain the stability. The condition can be released in some frequency range where $|Z_i| > |Z_o|$ and the system is still stable. The design of the load impedance can be bounded by the forbidden region, defined by [106]:

$$(|T_M|_{dB} = |Z_o|_{dB} - |Z_i|_{dB}) > -GM \text{ [dB]} \tag{1.5}$$

$$180° - PM1 < (\arg T_M = \arg Z_o - \arg Z_i) < 180° + PM2 \tag{1.6}$$

where PM is the Phase Margin. The gain limit is developed by:

$$|Z_{Lim}|_{dB} = |Z_o|_{dB} + GM \text{ [dB]} \tag{1.7}$$

If the input impedance of the load subsystem $|Z_i|_{dB}$ stays above the gain limit $|Z_{Lim}|_{dB}$, the load subsystem meets the specification MC automatically, however, when $|Z_i|_{dB}$ falls under the gain limit, the phase needs to be examined. In this case, the unacceptable phase band of $\arg Z_i$ with a given $\arg Z_o$ is defined by (1.6). To avoid the forbidden region, $\arg Z_i$ should be kept outside of the unacceptable phase band, when $|Z_i|$ is lower than the gain limit.

Opposing Argument Consortium (OAC)

When *n* individual loads are considered, then the resulting minor loop gain is expressed by:

$$T_M = \frac{Z_o}{Z_i} = \frac{Z_o}{Z_{i,1}} + \frac{Z_o}{Z_{i,2}} + \cdots + \frac{Z_o}{Z_{i,n}} \tag{1.8}$$

The previously mentioned GMPMC is difficult to extend to the design of individual impedances, when the individual impedances are not proportional to the load power level [109]. An alternative method, the Opposing Argument Consortium (OAC) has been proposed by [109], given by :

$$\text{Re}(T_M) = \text{Re}\left(\frac{Z_o}{Z_i}\right) \geq -\frac{1}{GM} \text{ with } GM > 1 \tag{1.9}$$

The forbidden region is the left region of a vertical line that intersects the *x*-axis at *–GM*, and the encirclement of (-1, 0) point is avoided with a certain $GM > 1$. Then the individual forbidden region of each subsystem loop gain $T_{M,k} = Z_o/Z_{i,k}$ is defined by shifting the vertical line according to the power level, given by:

$$\text{Re}\left(T_{M,k}\right) = \text{Re}\left(\frac{Z_o}{Z_{i,k}}\right) \geq -\frac{1}{GM} \times \frac{P_{load,k}}{P_{source}} \tag{1.10}$$

Where $T_{M,k}$ is the minor loop of the *k*th load subsystem. If the gain margin $GM = 2$ is chosen, as well as the output impedance of source subsystem Z_o, the individual load impedance specification could be constrained by two rules: if the magnitude (1.10) is satisfied, no phase limitation is required; otherwise the phase band should satisfy:

$$-90° - PM < (\arg T_{M,k} = \arg Z_o - \arg Z_{i,k}) < 90° + PM \tag{1.11}$$

where

$$PM = \arcsin\left|\frac{1}{2}\frac{Z_{i,k}}{Z_o}\frac{P_{load,k}}{P_{source}}\right|. \quad (1.12)$$

This specification provide the sufficient condition of the system stability. If the individual system loop gain doesn't enter into the individual forbidden region, the whole system loop gain will have the defined stability margin.

Energy Source Analysis Consortium (ESAC)

The ESAC can further reduce the artificial conservativeness by specifying a smaller forbidden region, which allows to impose a desired minimum *GM* and *PM* like in GMPMC [104]. Another advantage of this method is that it suffers less from component grouping when defining source impedance and load impedance than GMPMC. This leads to that some components of the electric system are able to works as both sources and loads.

B. Passivity based methods

The Nyquist Criteria based methods require all the source and load subsystems to be predefined, thus it is hard to be expanded to the analysis of a generic electric network which can absorb or supply power. The passivity can provide a good solution for this problem.

A system is passive if it only dissipates energy [111]. For a linear time-invariant 1-port system the input-to-output transfer function in Laplace form is:

$$h(s) = \frac{y(s)}{u(s)} \quad (1.13)$$

where, $u(.)$ is the input, $y(.)$ is the output and $u(t), y(t) \in \mathbb{R}^m$. Then the linear time-invariant system is passive if and only if [112]:

1) $h(s)$ has no right half plane poles;
2) $h(s)$ has a Nyquist plot which lies wholly in the closed right half plan.

According to Routh-Hurwitz Stability Criterion, a passive system is stable and $\arg h(s)$ is limited between -90° and 90°, thus passivity is a sufficient condition of stability. Furthermore, any combination of passive systems in parallel or feedback is passive thus stable [111].

For a 1-port electric network, it is passive if it can only absorb energy [103]. When the 1-port electrical system is modeled from current to voltage, the input-to-output transfer function (also impedance) is $Z(s) = V(s)/I(s)$. The Passivity-Based Stability Criterion (PBSC) proposed by [113] is based on the stability of passive system, it states:

> If the passivity is satisfied for $Z_{total}(s) = Z_o(s) \parallel Z_i(s)$, then the overall system consisting of the two interacting subsystems is stable [113].

1.3.7 Large-signal stability

The small-signal stability tests can only guarantee the stable operation nearby an equilibrium point. In order to obtain the asymptotical stable operation range (the domain of attraction), large-signal stability tests are required. The introduction of the CPL makes the DC microgrid to be a nonlinear system, and the system stability analysis can be conducted either using the linearized system or the original nonlinear system.

A. Lyapunov linearization theorem

As mentioned before, the power converter interfaced electronic loads with tight control can be viewed as CPLs, which is the origin of nonlinearity introduced to DC microgrids. To get the approximate linearized model, the CPL can be linearized at the operation point using Taylor expansion. With the linearized model of CPL, the original nonlinear system model becomes a linearized model, and the stability of the original system can be analyzed by the eigenvalues of the state matrix in the linearized model according to the Lyapunov linearized theorem. It states [114]:

> If the linearized system is strictly stable (all the eigenvalues of the state matrix have negative real parts), the operation point is asymptotically stable for the original system;
>
> If the linearized system is unstable (at least one eigenvalue of state matrix has real positive part), the equilibrium point is unstable for the original system;
>
> However, if the state matrix has eigenvalues with null real part, the linearization does not give information on the stability of the considered equilibrium point. The second method of Lyapunov needs to be used to construct a Lyapunov function to examine the stability of the original system.

Based on the Lyapunov linearized theorem, the influence of equivalent negative impedance of the CPL on the system stability can be analyzed by the eigenvalue traces of the state matrix [35], [96]. The ratio of CPL (the percentage of whole load taken by CPL) in the combined CPL and resistive load is also investigated to maintain system stability [115].

The sensitivity of the connecting cable resistances and inductances are investigated by the system matrix eigenvalues in a reduced-order model [91], as well as the effect of CPL and converter parameters [116]. The influence of the communication delay in secondary control and tertiary control on the system stability are also analyzed by eigenvalue traces, in the hierarchical control structure [32] as well as the influence of communication delay in the distributed control structure [61]. The stability of the DC microgrid under variable structures is also investigated and analyzed based on the eigenvalues traces in the complex coordination [117].

B. Lyapunov function based methods

The Lyapunov function method to analyze the large-signal stability is based on the definition of Lyapunov function, it states [118]:

> A function $V(x)$: $R^n \rightarrow R$ is a Lyapunov function in $\vartheta(0,\rho)$ for system $\dot{x} = f(x)$, if: (1) $V(x)$ is positive definite in $\vartheta(0,\rho)$; (2) $V(x)$ has continuous first-order partial derivatives with respect to x; and (3) $V(x) = \langle grad\ V, f(s)\rangle \leq 0\ \forall x \in \vartheta(0,\rho)$, $\langle grad\ V, f(s)\rangle = \langle grad\ V, \dot{x}(t)\rangle$.

The conditions to realize asymptotic stability in the sense of Lyapunov states [118]:

> Asymptotic stability: The zero state is asymptotically stable in the sense of Lyapunov if there exists a Lyapunov function $V(x)$ in a neighborhood of the origin $\vartheta(0,\rho)$ such that $dV(x)/dt < 0$ for all $x \in \vartheta(0,\rho), x \neq 0$.
>
> Asymptotic stability domain: Let $V(x)$ be a Lyapunov function and h a positive real number such that the open set $D = \{x: \dot{V}(x) < h\}$ is bounded and let $dV(x)/dt < 0$ for all $x \in D, x \neq 0$. Then, all trajectories starting from a point in the set D converge asymptotically to zero.

This method is also usually referred as the direct method of Lyapunov or Lyapunov second method. The major issue to adopt this method is that there is no general method to develop the Lyapunov function. To analyze the large-signal stability and obtain the asymptotic stability domain (domain of attraction), efforts are required on the construction of Lyapunov function.

Lots of methods have been developed in literature to construct the optimal Lyapunov function, and some common methods are utilized in the analysis of nonlinear electric circuits and their applications. They are reviewed as follows.

Mixed potential function

The mixed potential type Lyapunov function can be developed by using the elements and the topology of the studied circuit. Brayton and Moser propose three theorems to analyze the nonlinear circuit stability in large disturbance [119], [120]. They can be applied to the circuits which contain purely linear resistors or conductor combined with nonlinear or linear inductors and capacitors, or to the circuits contain purely linear inductors or capacitors combined with linear or nonlinear resistors and conductors [121]. This method is adopted to analyze the stability problem of CPLs with multistage LC filters [122]. The missing case that the circuits contain nonlinear resistors, conductors, inductors, and/or capacitors at the same time, is examined in [121], [123].

Searching method

Many practical methods have been proposed to estimate the domain of attraction; e.g., the Jacobian Diagonalization Lyapunov Function (JDLF), the Full Quadratic Lyapunov Function (FQLF), the Block Diagnonalized Quadratic Lyapunov Function (BDQLF) and the Hyper Cylindrical Lyapunov Function (HCLF). However, the resulted domain of attraction is usually over-convective. In order to obtain the domain of attraction closer to the real domain of attraction, an optimal searching method using genetic algorithm to find out the optimized Lyapunov candidate function is proposed by [124], [125]. Other alternative methods (e.g., linear programing [126]) can be applied to perform the similar selection procedure.

Multiple local models

Instead of directly deriving the Lyapunov function from the original nonlinear system, another class of methods using local linearized models has been developed, in which the nonlinear system is represented by the convex combination of multiple linear local models. The Lyapunov function is then developed from the analysis of these local models.

In the Polytopic model method, proposed by [127], the original nonlinear model is represented by a convex combination of multiple linear local models, which are the linearized models at equilibrium points. The number of local models depends on the divisions in the operation plant. Smaller divisions lead to more local models as well as higher accuracy. Then a common Lyapunov function satisfying the stable requirement of all the local models can be obtained. This Lyapunov function can guarantee the globally asymptotical stability at these operation points for the original system. Finally, the domain of attraction around the equilibrium point for the original system can be obtained by the direct Lyapunov method using the resulted Lyapunov function.

Takagi-Sogeno (TS) Multimodel [128], [129] has the similar structure as the Polytopic model. It also uses a convex sum of multiple linear local models, which are deduced from the nonlinear system, to represent the original nonlinear model. The fuzzy rule '*if-then*' is adopted to represent the input-output linear local relations of the nonlinear model [129]. TS Multimodel can represent the nonlinear system with a limit number of local models. Each nonlinearity admits two values: the minimum value and the maximum value. Then the resulting model has at least 2^q local models (q is the number of nonlinearity), and the number of local models depends on the number of nonlinearities instead of divisions. The Lyapunov function of the original system is obtained when all the state matrices of the local linear models and their sum are Hurwitz, and then the estimated domain of attraction can be deduced from this Lyapunov function.

1.4 Motivation and objective

From the reviewed literatures, it can be seen that the DC microgrid has been studied at different levels by the researchers. However, there are still some topics need to be further investigated; e.g., the comprehensive comparison of the steady-state compensation methods, the dynamic modeling and analysis of multi-time scale DC microgrids. The objectives of this dissertation are thus:

- To improve the load sharing performance and bus voltage regulation in droop control based DC microgrids;
- To investigate the modeling methodologies of DC microgrids with multiple time scales;
- To analyze the small-signal and large-signal stability of multi-time scale DC microgrid;
- To develop a proper time scale droop control for multi-time scale DC microgrids.

1.5 Outline of the dissertation

This dissertation is organized in six chapters. **Chapter 1** presents the background of the microgrid, comparison of AC and DC microgrids, literature review as well as the motivation and objectives of this dissertation.

Chapter 2 focuses on the steady-state voltage regulation and load sharing performance in DC microgrids. It starts from the analysis of basic droop control in low-voltage DC microgrid, where DGs are connected to the common DC-bus via power converters. The limits of the basic droop control and the conflict of voltage regulation and load sharing are investigated. Then the compensation methods to improve voltage regulation and load sharing are reviewed and compared, and a unified compensation structure based on the common current is proposed. The boundaries of the voltage compensation constant is investigated to maintain system stability. Some simulations in MATLAB/Simulink and experimental tests are carried out to verify the proposed method.

Chapter 3 turns the attentions to the modeling and stability analyses of the multi-time scale DC microgrid. A virtual inductor is introduced to combine with the droop resistor, such that the dynamic behaviors of the DG can be properly presented by the ratio of the virtual inductance over the droop resistance. Then, a comprehensive model (CM) of the DC microgrid is developed. To simplify the model of the system, several model reduction technologies are adopted to reduce the high order CM to a reduced 4th-order model (R4M) and further to a reduce 2nd-order model (R2M). The reduced order models are deduced on the assumptions of similar inductance and similar inductance/resistance ratio, thus single time scale. They cannot represent the real system with multiple time constants properly. Therefore a novel multi-time scale reduced model (RMM) is proposed, which groups the DGs with similar time constants together and then combines the groups to form a new model. This proposed model can effectively reduce the complexity of CM while maintain the major time scale

information. The effectiveness of RMM for multi-time scale DC microgrids is confirmed through simulations and experimental tests.

Chapter 4 deals with the control realization of multi-time scale DC microgrid. Different realization methods using feedback low-pass filter, forward path low-pass filter, and PI voltage control combined with virtual droop resistor are compared. They all based on the precise system model, which is hard to obtain in some cases. Thus a novel method based on Active Disturbance Rejection Control (ADRC) is proposed to implement the time scale droop control of the DGs. It can simplify the tuning of the system bandwidth and reduce the sensitivity to system model errors. Then the influence of DC-bus capacitance and constant power loads on the system stability is analyzed based on the new parameterized RMM, and a general procedure to design the capacitance for a stable multi-time scale DC microgrid is constructed. Simulations and experimental tests are conducted to verify the proposed method.

Chapter 5 studies a general case with the power sources of FC, batteries and PV panels. The control performances of the classic droop control, classic droop control with steady-state compensations, ADRC based time scale droop control and ADRC based time scale droop control with steady-state compensations are compared and analyzed in MATLAB/Simulink simulations as well as in experimental tests.

A general conclusion and perspective of the future works are given in **Chapter 6**.

Chapter 2 Compensations of Droop Control in DC Microgrids

The control objective of DC microgrids under steady-state condition is to maintain stable system operation, low voltage regulation and equal load sharing in per unit among the distributed generators (DGs). Droop control is an effective method to implement the control of DC microgrids with multiple DGs. However in the applications of low-voltage DC microgrids, the nominal voltage reference offsets and unequal connecting cable resistances will lead to that the trade-off to be made between voltage regulation and load sharing.

This chapter discusses the control methods to compensate the voltage error introduced by classic droop control and the unequal load sharing due to the connecting cable impedances and the nominal voltage reference offsets. At first, the influences of the nominal voltage offsets and unequal connecting cable impedances on voltage and load sharing performances in classic droop control are analyzed. Then the compensation methods in literature using common voltage or/and common current are reviewed, and a novel unified compensation method is proposed based on the common current. In this scheme, the voltage deviation is compensated with a simple P controller while the load sharing is compensated through a PI controller to make the local current follows the common current. A dedicated low-bandwidth communication is introduced to share the output current information, such that the common current (normalized average current through the system) can be generated in the local control. The boundaries of the compensation parameters are examined to maintain the stability of the system. Simulations in MATLAB/Simulink environment and experimental tests are carried out in laboratory scale test bench to verify the proposed control method.

2.1 Analysis of the Classic Droop Control

According to Thévenin theorem, the power converter interfaced DG can be modeled as an imperfect voltage source (an ideal voltage source with inner resistor in series), when droop control is applied [130]. Then the corresponding DC microgrids can be represented as the parallel connection of multiple imperfect voltage sources. The relationship between output current and voltage reference can be expressed by:

$$V_j - V_{MG} = i_j \, (R_{oj} + R_{cj}) \tag{2.1}$$

The subscript $j = 1, 2, \ldots$ indicates the jth DG; V_j denotes the equivalent nominal voltage reference of the jth DG; V_{MG} denotes the microgrid voltage, as well as the voltage at load point; i_j denotes the

injected current to DC-bus by the module; R_{oj} denotes the equivalent output resistance; R_{cj} denotes the connecting cable resistance. It can be seen from (1.1) that the current/power injected to the DC-bus depends on the voltage deviation and output resistance R_{oj}, thus the output current/power can be adjusted by the nominal voltage references or output resistances.

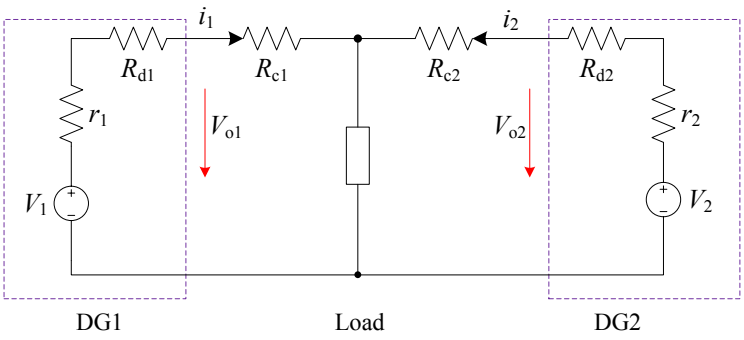


Figure 2.1 Equivalent circuit of a DC microgrid with two distributed generators

The equivalent circuit of a DC microgrid with two DGs is shown in Figure 2.1. The equivalent output resistor R_{oj} is composed of the built-in resistor r_j and virtual droop resistor R_{dj}. It can be expressed by:

$$R_{oj} = r_j + R_{dj} \tag{2.2}$$

Then output current can be deduced from the equivalent circuit, as follows,

$$i_j = \frac{V_j - V_{MG}}{R_{oj} + R_{cj}} = \frac{V_j - V_{MG}}{r_j + R_{dj} + R_{cj}} \tag{2.3}$$

The built-in resistances are determined by the structure and physical parameters of the power converters, thus aren't identical in different DGs. This is one source of the unequal load sharing. The cable resistances and nominal voltage offsets also result in the unequal load sharing issue. The built-in resistances are pretty small compared to virtual droop resistances. When the built-in resistances are omitted, the steady-state load sharing error between the two DGs is given by (2.4),

$$\Delta i_{12} = i_1 - i_2 = \frac{(R_{d2} + R_{c2})(V_1 - V_{MG}) - (R_{d1} + R_{c1})(V_2 - V_{MG})}{(R_{d1} + R_{c1})(R_{d2} + R_{c2})} \tag{2.4}$$

where Δi_{12} is the load sharing error between the two DGs. The load sharing error relies on the output resistances and nominal voltage references. Equal load sharing can be achieved with identical output resistances and accurate voltage nominal references. Small nominal voltage offsets introduced by voltage feedback sensing signals, or equal connecting cable resistances may result in significant performance deterioration, the effects are analyzed in the following subsections.

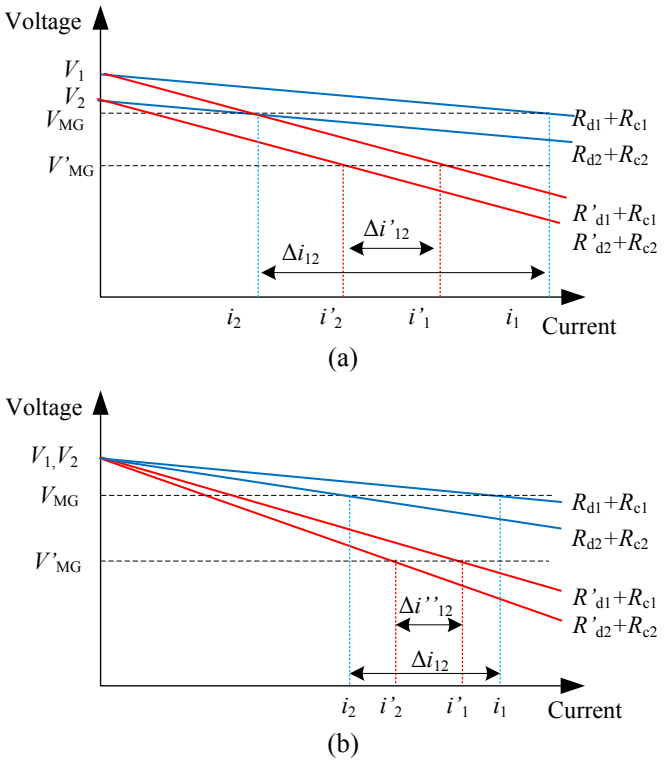


Figure 2.2 The influences of unequal nominal voltage references and cable resistances on the load sharing and DC-bus voltage regulation. (a) The nominal voltage references are different, the cable resistances are the same; (b) The nominal voltage references are identical and the cable resistances are different $R_{c1} < R_{c2}$.

2.1.1 Nominal Voltage Reference offset

The nominal voltage reference offsets are usually introduced by the physical implementation of voltage measurement [33]. A small sensed voltage error may lead to a significant load sharing error, especially when the virtual droop resistances are relatively small. The influence can be demonstrated by Figure 2.2. When two DGs are paralleling connected to supply power for a constant current load. Then load sharing error of two DGs is given by:

$$\Delta i_{12} = \frac{(R_{d2} + R_{c2})(V_N + \delta V_1 - V_{MG}) - (R_{d1} + R_{c1})(V_N + \delta V_2 - V_{MG})}{(R_{d1} + R_{c1})(R_{d2} + R_{c2})} \tag{2.5}$$

where V_N is the nominal microgrid voltage, δV_j is the jth DG's nominal voltage offset and the DG's nominal voltage reference is $V_j = V_N + \delta V_j$.

When per unit system is adopted, the normalized droop resistances are selected to be the same $R_{d1} = R_{d2} = R_d$. If the cable resistances are equal $R_{c1} = R_{c2} = R_c$, the load sharing error and the DC-bus voltage drop can be expressed as:

$$\Delta i_{12} = \frac{\delta V_1 - \delta V_2}{R_d + R_c} \tag{2.6}$$

$$\Delta V_{MG} = \frac{1}{2}[\delta V_1 + \delta V_2 - (R_d + R_c) i_L] \tag{2.7}$$

where i_L is the load current; ΔV_{MG} is the DC-bus voltage error compared to the nominal value V_N. It can be seen from Figure 2.2 that higher droop resistance $R'_d > R_d$ leads to better load sharing but poorer DC-bus voltage performance. The load sharing error and voltage drop become:

$$\Delta i'_{12} = \frac{\delta V_1 - \delta V_2}{R'_d + R_c} < \Delta i_{12} \tag{2.8}$$

$$\Delta V'_{MG} = \frac{1}{2}[\delta V_1 + \delta V_2 - (R'_d + R_c) i_L] > \Delta V_{MG} \tag{2.9}$$

According to (2.8) when the nominal voltages offset of DG1 is 1% and zero for DG2; i.e., $\delta V_1 = 1\%, \delta V_2 = 0$, droop resistance is chosen as $R_d = 0.03$pu and the line resistances $R_c = 0.01$pu, the resulted load sharing error will be as large as 25%, when a 0.8pu load is connected. If the droop resistances increase to $R'_d = 0.08$pu, then the current error deceases to 11.1% of the rated current. But the DC-bus voltage drop increases from less than 2.7% to about 6.7%, this may be not acceptable. The load sharing error and DC-bus voltage drop in relationship of droop resistance are shown in Figure 2.3. It indicates that the influence of unequal nominal voltage can be reduced with higher droop resistance, but the performance of voltage regulation becomes worse.

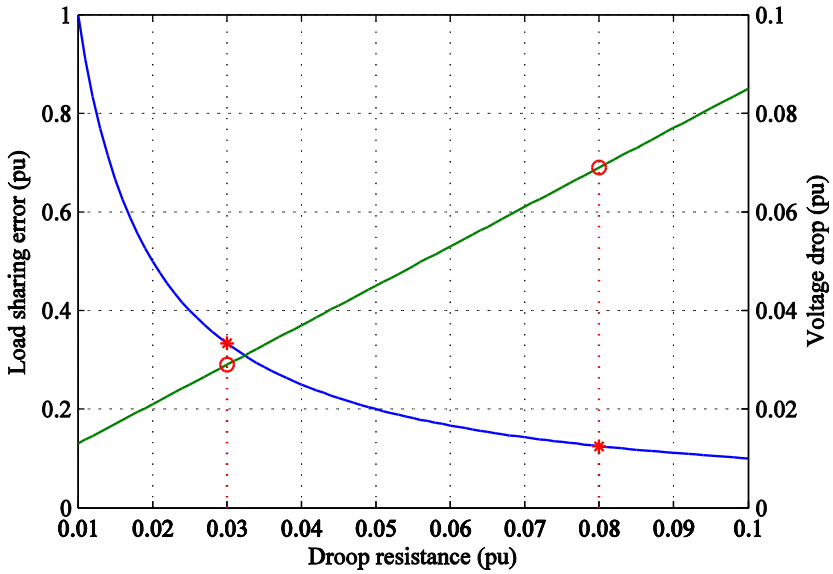


Figure 2.3 The load sharing error and DC-bus voltage drop in relationship of the droop resistance, with 1% nominal voltage reference offset

2.1.2 Unequal cable resistances

Due to geographic locations of DGs, the line resistances may be comparable to droop resistances; this will cause significant load sharing errors. It can be demonstrated in Figure 2.2b. Similarly, the

effect of unequal line resistances can be reduced by relative higher droop resistances, but the voltage regulation performance may be decreased. If the nominal voltage reference error is not considered ($V_1 = V_2 = V_N$), the load sharing error deduced from (2.4) is:

$$\Delta i_{12} = \frac{(R_{d2} + R_{c2})(V_N - V_{MG}) - (R_{d1} + R_{c1})(V_N - V_{MG})}{(R_{d1} + R_{c1})(R_{d2} + R_{c2})} \tag{2.10}$$

With the droop resistances are selected to be same $R_{d1} = R_{d2} = R_d$ in per unit system, and the load sharing error and DC-bus voltage drop can be expressed as:

$$\Delta i_{12} = \frac{(R_{c2} - R_{c1})(V_N - V_{MG})}{(R_d + R_{c1})(R_d + R_{c2})} \tag{2.11}$$

$$\Delta V_{MG} = V_N - \frac{R_d + R_{c1}}{2R_d + R_{c1} + R_{c2}} i_L \tag{2.12}$$

When higher droop resistor $R'_d > R_d$ is adopted, the load sharing error and voltage drop become:

$$\Delta i''_{12} = \frac{(R_{c2} - R_{c1})(V_N - V_{MG})}{(R'_d + R_{c1})(R'_d + R_{c2})} < \Delta i_{12} \tag{2.13}$$

$$\Delta V''_{MG} = V_N - \frac{R'_d + R_{c1}}{2R'_d + R_{c1} + R_{c2}} i_L > \Delta V_{MG} \tag{2.14}$$

Then a better load sharing is achieved, but worse voltage performance at the same time.

In brief, the classic droop control benefits high reliability and easy implementation because it does not require any communication between connected DGs. On the other hand, this method is an open loop technique to individually program the output impedance of each DG, thus sensitive to the cable impedance difference and the nominal voltage reference offset. A trade-off must be made between the load sharing and output voltage regulation. Some compensations with the aid of low-bandwidth communication can be applied to adjust droop resistance or nominal voltage reference, so as to achieve good voltage regulation and load sharing simultaneously.

2.2 Compensation of the Classic Droop Control

As aforementioned, the problem of the classic droop control is the conflict between voltage regulation precision and load sharing performance. The inherent limits make that it cannot realize precious voltage regulation and equal load sharing simultaneously. The voltage through the whole DC microgrid is not constant, thus cannot be used as the global variable like frequency in AC microgrid. Thus low-bandwidth communication is introduced to share voltage or current information, in order to generate a common reference through the microgrid. The low-bandwidth communication is used as an auxiliary to the classic droop control, such that system performance can be enhanced

with this low-bandwidth communication and the system still can work without communication or when the communication fails.

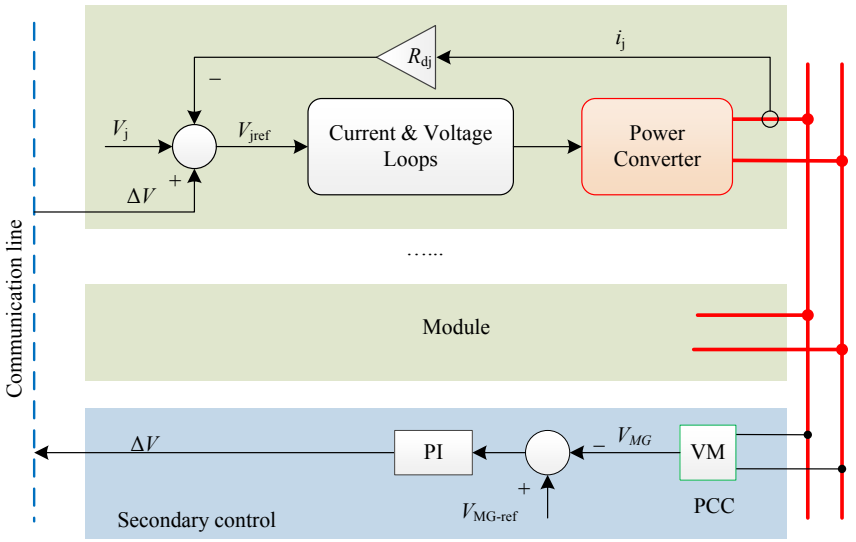
Many compensation methods have been studied to improve the performance of droop control with low-bandwidth communication; e.g., using an hierarchical structure to restore the voltage deviation in a centralized secondary controller [31], generating voltage compensations in local controller by average current [33], or generating load sharing compensation according to the error of the common voltage reference and local voltage [32]. According to their objectives, these compensation strategies can be classified into three categories: voltage deviation restoration, load sharing compensation and mixed method.

2.2.1 Voltage deviation restoration

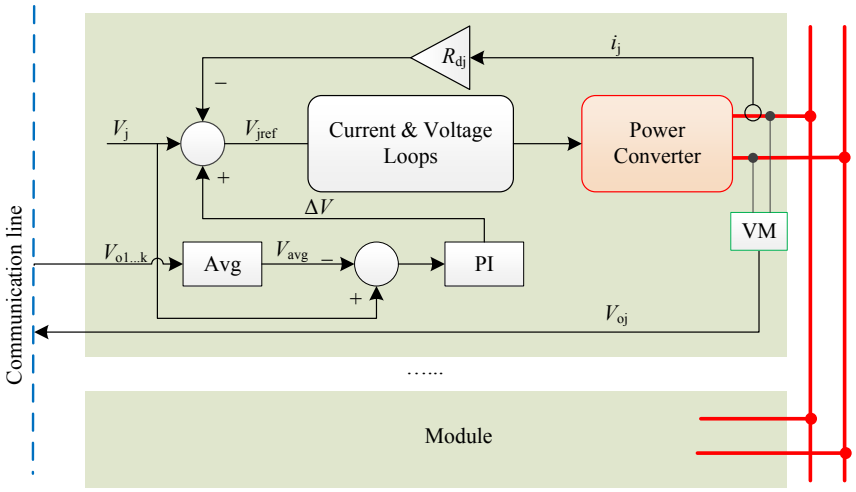
A hierarchical control structure is proposed by [31] to restore the voltage deviation (referred as Type AI), as shown in Figure 2.4a. The low-bandwidth communication line between the secondary controller and local controllers is used to transmit the voltage compensation from the secondary control to local control. The secondary controller compares the voltage reference with measured voltage in point of common coupling (PCC) or point of load (POL), and the voltage error goes through a voltage regulator to generate the global voltage compensation. The voltage compensation is transmitted to all local controllers through a low-bandwidth communication.

The voltage deviation of droop control can also be compensated locally by voltage error [32] with the aid of dedicated communication line (referred as Type AII), as shown in Figure 2.4b. The output voltage information of all DGs are shared with a dedicated low-bandwidth communication line. Each DG receives the voltage information to generate common average voltage (common voltage). The error between the common voltage and the local nominal voltage reference passes through voltage compensation controller to generate voltage compensation individually in each local control. This compensation method can be viewed as the distributed form of Type AI, in which the average output voltage is used to represent the load voltage and the voltage restoration control is dedicated into each DG.

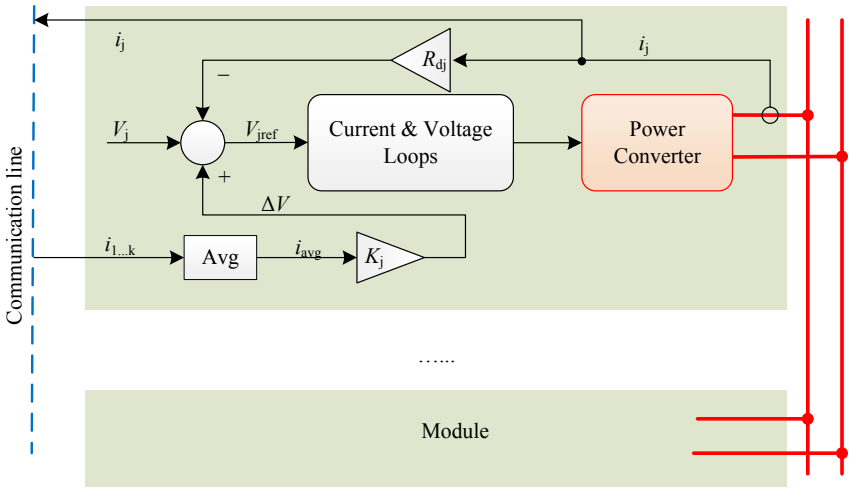
Besides the average output voltage, the common average output current (common current) can also be used to design the voltage drop compensation in local control [33], which is shown in Figure 2.4c (referred as Type AIII). In this scheme, the current information of all connected DGs are shared through a dedicated low-bandwidth communication line. The common current is generated in each local controller, and then the voltage compensation is generated by the product of common current and a voltage compensation coefficient K_j. The maximum current value through the whole microgrid instead of the average current could be an alternative to be used to generate voltage compensation.



(a) Type AI



(b) Type AII



(c) Type AIII

Figure 2.4 Voltage compensation methods for classic droop control

The aforementioned Types AI and AII use the nominal voltage as reference to regulate the load voltage or common voltage, thus the load voltage or common voltage can achieve the nominal voltage reference without static error. However the design of the voltage control, such as PI controller is not an easy task, and the compensation loop should be much slower so as to avoid the coupling with voltage control loop of the DG. Although the voltage derivation cannot be totally avoid by using Type AIII, it can be significantly reduced with a properly selected voltage compensation coefficient. Besides, the design of the compensation coefficient is rather intuitive in Type AIII. Compared to Type AI, the Types AII and AIII can enhance the system reliability by using dedicated communication without the need of a central controller. It must be noted that, these voltage compensation methods generate global voltage compensation (i.e., same compensation in the each local control), thus only the voltage performance is improved, but the load sharing performance remains the same as the classic droop control.

2.2.2 Load sharing compensation

Different from the voltage compensation, the load sharing compensation can't be realized in global manner, and individual compensation in each local control is required. A dedicated low-bandwidth communication line is required to connect the DGs so as to share the current information [32]. As shown in Figure 2.5 (referred as Type B), the shared current information is used to generate the normalized average common current reference, and a load sharing compensation regulator is used to control the local current to follow this common reference. Thus all DGs can share the load equally. An alternative using the maximum current reference can achieve similar performance. Type B can achieve equal load sharing without error when PI control is adopted, but the voltage performance keeps the same as the classic droop control.

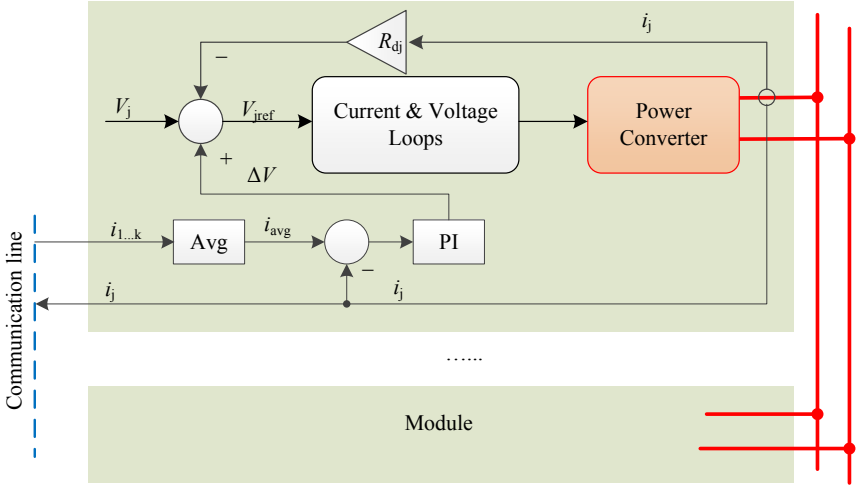


Figure 2.5 Load sharing compensation method (Type B) for classic droop control

2.2.3 Mixed method

The above discussed methods can only realize voltage compensation or load sharing compensation, thus a mixed method is required to achieve both compensations. The DC-bus voltage can be restored by the global voltage compensation generated by common voltage or current information, while the load sharing compensation requires common current information. Therefore two mixed methods can be deduced from the combination of the compensation methods: Type CI, as shown in Figure 2.6a, uses the shared voltage information to generate global voltage compensation like in Type AII, while uses the shared current information to generate load sharing compensation like in Type B [32]; Type CII, as shown in Figure 2.6b, uses the shared current information to compensate both bus voltage and load sharing performance, like the combination of Types AIII and B [131].

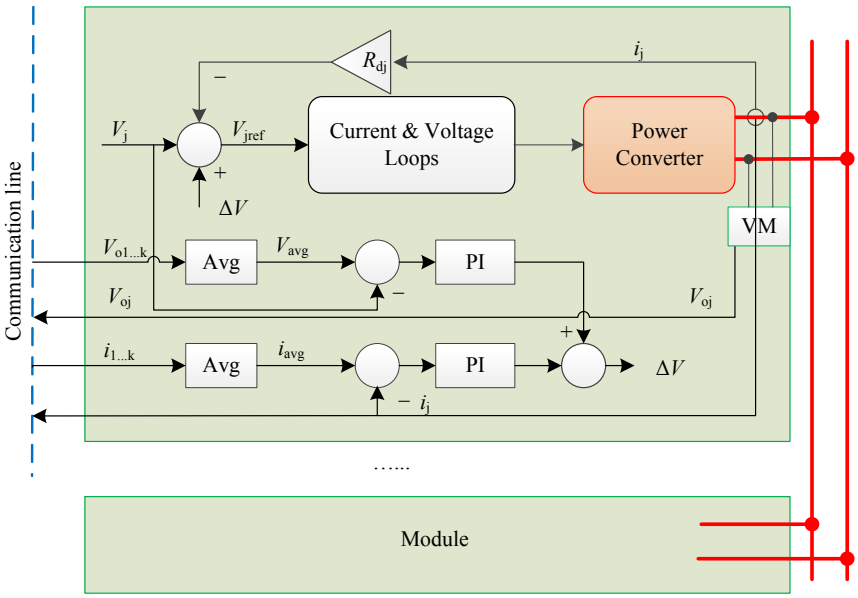
Type CI inheriting the performance of Type AII, is able to achieve zero error in DC-bus voltage compensation, while Type CII can only improve the control of DC-bus voltage with the adjustment of compensation coefficient. However Type CI requires the communication to share both the output voltage and current information, and the parameters of the two PI type compensation controllers need more effort to be tune. In contrast, the proposed Type CII can reduce the communication burden by using only shared current information, as well as the tuning of the parameters in the compensation controllers is much easier than that of Type CI.

The comparison of different compensation methods are shown in Table 2.1 according to their voltage performances, load sharing performances, communication burdens and complexities. It can be seen that although Type CI achieves the best performance, it requires the highest communication burden and has the most complicated structure. The proposed Type CII can be a better candidate which can achieve comparable performance using medium communication burden and medium complicated structure.

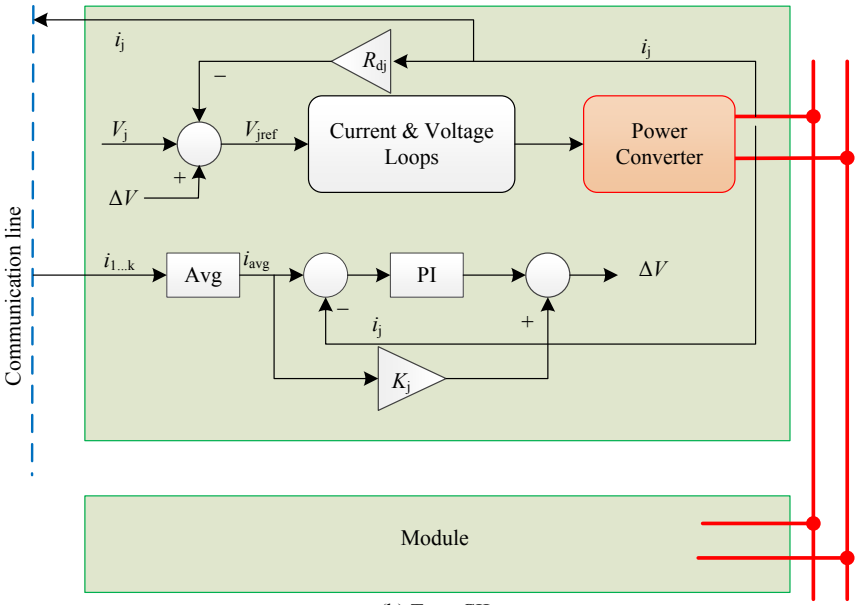
Table 2.1 Comparisons of the droop control compensation methods

Type	Voltage performance	Load sharing	Comm. burden	Complexity
Classic droop control (Type A)	Fine	Fine	Zero	Simple
Type AI	Good	Depend	Light	Medium
Type AII	Medium	Depend	Medium	Medium
Type AIII	Medium	Depend	Medium	Medium
Type B	Depend	Good	Medium	Medium
Type CI	Good	Good	Heavy	Complicated
Type CII*	Good	Good	Medium	Medium

*The proposed method



(a) Type CI



(b) Type CII

Figure 2.6 Mixed compensation methods for classic droop control, in which Type CII is the proposed compensation method.

2.3 Implementation and Analysis of the Compensation

The DC-bus voltage drop is derived from the droop control in local controller, while the unequal load sharing comes from the unequal output impedances, connecting cable impedances and nominal voltage reference offsets. Therefore, the voltage and load sharing compensation can be separately designed using the aforementioned mixed compensation method Type CII.

As shown in Figure 2.6, a dedicated low-bandwidth communication is introduced to share the local current through the whole system. Then the normalized common average current reference is generated in the local controller by:

$$i_{avg} = \frac{\sum i_j I_{Nj}}{\sum I_{Nj}} \tag{2.15}$$

where i_{avg} is the normalized common average current reference, which represents the load condition of the whole system; I_{Nj} is the rated current of the *j*th DG; i_j is the local current of the *j*th DG.

2.3.1 Voltage deviation compensation

In classic droop control, the output voltage changes linearly with the output current/power, and this unavoidably leads to the DC-bus voltage deviation. The most intuitive method is to compensate the voltage deviation by the load current or common average current as described in Type AIII. The voltage compensation is given by:

$$\Delta V_j' = K_j i_{avg} \tag{2.16}$$

where K_j is the voltage compensation coefficient to restore bus voltage, and it should be selected with the same normalized value for each DG. Moreover, its value should be smaller than the droop resistance to retain the droop control function [33] and also be selected properly to maintain the system stability (detailed analysis in Section 2.3.3).

When the DC microgrid is simplified to be a source-load system, the voltage error V_{drop} reduces with the increase of the compensation coefficient as shown in (2.17), if nominal voltage reference offset is not considered.

$$V_{drop} = R_{dj} i_j - K_j i_{avg} \tag{2.17}$$

The normalized common current i_{avg} equals to the normalized local current i_j, and the DC-bus voltage performance can be improved; e.g., when the compensation coefficient is selected to be half of the virtual droop resistance, the voltage error would decrease to half, if the built-in resistance of the DG is neglected.

2.3.2 Load sharing compensation

Load sharing errors come from the differences among the DGs, thus they need to be compensated individually in the local control of each DG rather than using the global compensation. Similar as the voltage compensation, the normalized common current reference is used to compare with the local current, and then the error feeds into a PI to generate load sharing compensation. The local current is controlled to follow the common current reference such that equal load sharing is achieved. The load sharing compensation is given by:

$$\Delta V_j'' = \frac{K_{Pj}s + K_{Ij}}{s}(i_{avg} - i_j) \tag{2.18}$$

where s is the integrator; K_{Pj}, K_{Ij} are the gains of load sharing PI compensator in the jth DG. In steady-state, the normalized local current can be controlled well following the common current reference, and ideally no load sharing error. The compensation loop needs to be designed much slower than the voltage control loop to avoid the interaction between them; e.g., the voltage loop bandwidth is 100 rad/s and then the bandwidth of compensation loop can be selected no higher than 20 rad/s.

2.3.3 Stability analysis

The adoption of the voltage compensation coefficient in Type AIII or Type CII will reduce the effect of droop control, and may affect the stability of the system, especially when the constant power load (CPL) is connected [132]. Therefore a model of the DC microgrid is required to conduct the stability tests, such that the boundaries of the compensation coefficient can be determined.

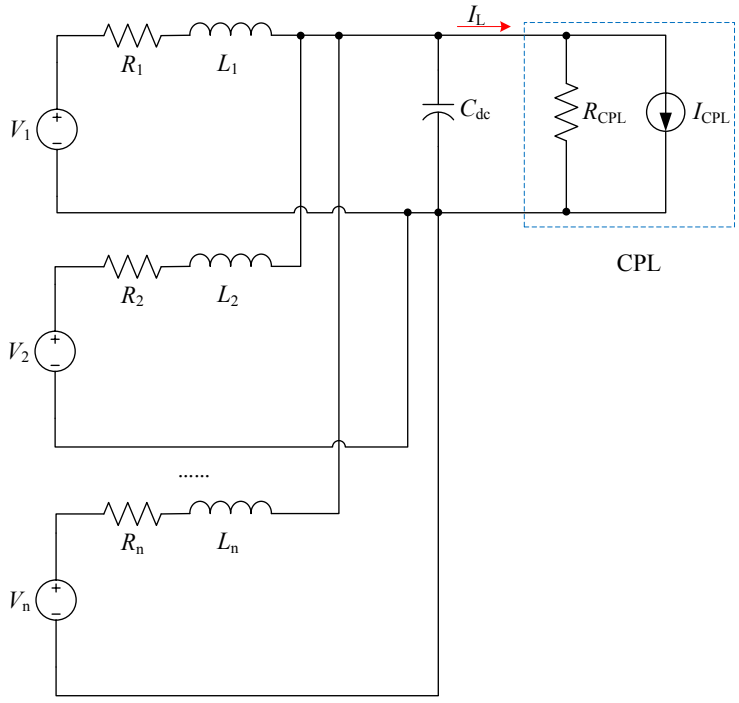


Figure 2.7 The equivalent circuit of a DC microgrid with n DGs and one CPL

As mentioned before, the droop controlled DG can be represented by an imperfect voltage source using Thévenin theorem. The cable resistance and inductance can be combined together with the equivalent circuit of the DG, then it becomes the perfect voltage source with an equivalent source resistor and an equivalent inductor in series. Then the DC microgrid can be represented by multiple DG equivalent circuits in parallel as shown in Figure 2.7. V_j is the nominal voltage reference of the

jth DG, R_j is the combination of droop resistance and the line resistance, and the built-in resistance is not considered; L_j is the connecting cable inductance; and C_{dc} denotes the combination of source output capacitance and load input capacitance.

Consider the microgrid supplying power to a Constant Power Load (CPL). The relationship of the load current and the load voltage in ideal CPL is written by:

$$I_L = \frac{P_{CPL}}{V_L} \tag{2.19}$$

where I_L is the current absorbed by the CPL; V_L is the load voltage. Then, the linearized CPL model can be obtained by using Taylor expansion at the operation load voltage V_e, the obtained load current approximates:

$$I_L \approx I_{CPL} + \frac{V_L}{R_{CPL}} \tag{2.20}$$

The resulted equivalent circuit of CPL is composed of a negative resistor $R_{CPL} = -V_e^2/P_{CPL}$ and a current sink $I_{CPL} = 2P_{CPL}/V_e$ in parallel.

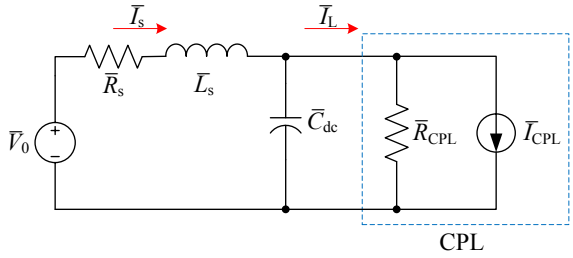


Figure 2.8 Reduced order model of the DC microgrid

Using the arithmetic mean value to represent the distributed parameters of individual DGs, the equivalent circuit of the microgrid can be reduced to an equivalent DG supplying power to the CPL [92]. The equivalent circuit of the reduced order model is shown in Figure 2.8, and the linearized state-space form is given by:

$$\frac{d}{dt}\begin{bmatrix}\bar{I}_s \\ V_L\end{bmatrix} = \begin{bmatrix}-\frac{\bar{R}_s}{\bar{L}_d} & -\frac{1}{\bar{L}_d} \\ \frac{1}{\bar{C}_{dc}} & -\frac{1}{\bar{C}_{dc}\bar{R}_{CPL}}\end{bmatrix}\begin{bmatrix}\bar{I}_s \\ V_L\end{bmatrix} + \begin{bmatrix}\frac{1}{\bar{L}_d} & 0 \\ 0 & -\frac{1}{\bar{C}_{dc}}\end{bmatrix}\begin{bmatrix}V_N \\ \bar{I}_{CPL}\end{bmatrix} \tag{2.21}$$

where V_N is the nominal voltage of the microgrid also voltage reference in each local voltage control; $\bar{I}_s$ is the average current supply by the equivalent DG, $\bar{R}_s$ denotes the equivalent combined average droop resistance and average cable resistance; $\bar{L}_s$ denotes the equivalent average cable inductance; $\bar{R}_{CPL}, \bar{I}_{CPL}$ denote the equivalent resistance and current sink for the equivalent load in reduced order

model. Consider a microgrid with n DGs, the load parameters can be converted into equivalent average parameters for the reduced order model, as follows:

$$\begin{cases} \bar{R}_{CPL} = n \times R_{CPL} \\ \bar{I}_{CPL} = \dfrac{I_{CPL}}{n} \\ \bar{C}_{dc} = \dfrac{C_{dc}}{n} \end{cases} \tag{2.22}$$

Using the linearized model of CPL, the DC microgrid can be viewed as a linear time-invariant (LTI) system, the global asymptotical stability can be analyzed by the locations of the state matrix eigenvalues. When all the eigenvalues have negative real parts, the system is stable in the sense of Lyapunov. If any of the eigenvalues has positive real part, the system is unstable. The introduction of voltage compensation changes the value of the equivalent source resistance $\bar{R}_s$, which will affect the eigenvalues of the state matrix. Thus small-signal stability tests are required to determine the margins of the equivalent source resistance.

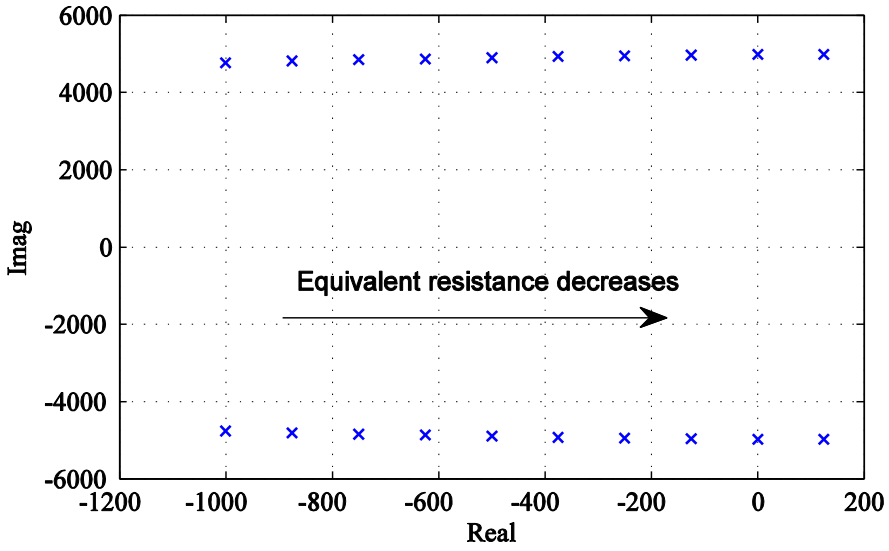


Figure 2.9 The eigenvalue traces of the system state matrix with the decrease of equivalent source resistance

The eigenvalue traces of the state matrix in the reduced model are shown in Figure 2.9 with variable equivalent source resistance. The equivalent source resistance decreases from 0.1 Ω to 0.02 Ω (20% of the original value). The other parameters used for the analysis are listed in Table 2.2.

Table 2.2 The parameters of the equivalent circuit to conduct the stability analysis

	Equiv. resistance	**Equiv. inductance**	**Equiv. capacitance**	**Equiv. load**
Value	0.5 Ω	200 μH	0.2 mF	1000 W

The eigenvalues are gradually approaching the right-hand side, with the decreases of the equivalent resistance, the real part of the eigenvalues become positive when the equivalent resistance reaches

0.03 Ω. Therefore the minimum value that can be applied is around 30% of the original value; i.e., the voltage compensation coefficient needs to be limited no larger than 70% of the droop resistance, so as to not threat system stability.

2.4 Simulation

2.4.1 Simulation setup

The DC microgrid with three DGs is modeled and simulated in MATLAB/Simulink environment. The rated power/voltage of the three DGs are 700W/70V (M700), 50W/50 V (M500) and 300W/60V (M300), respectively. The DGs are connected to the common DC-bus via boost type DC-DC converters. The DC-bus voltage adopted is 100 V. Other parameters of the three DGs used for simulation are listed in Table 2.3. It is assumed that the three DGs are geographically distributed, and M300 is located near the load, M700 and M500 are connected to the load with cables about 1 m and 3 m, respectively. Single conductor cable (5.5 mm^2) is used as the connecting cable, then the resistors are designed to be 0.01 Ω, 0.03 Ω, to consider the influences of connecting cables [10]. To simulate the influence of unequal nominal references, the nominal reference offsets for these three DGs are manually set to 0.5%, 0%, and 0.25%, respectively.

Table 2.3 Parameters of the examined DC microgrid

Module	Rated voltage	Rated current	Line Resistance	Voltage offset
M700	70 V	10 A	10 mΩ	0.5%
M500	50 V	10 A	30 mΩ	0%
M300	60 V	5 A	0 Ω*	0.25%

* The value is smaller than 1 mΩ during experiments

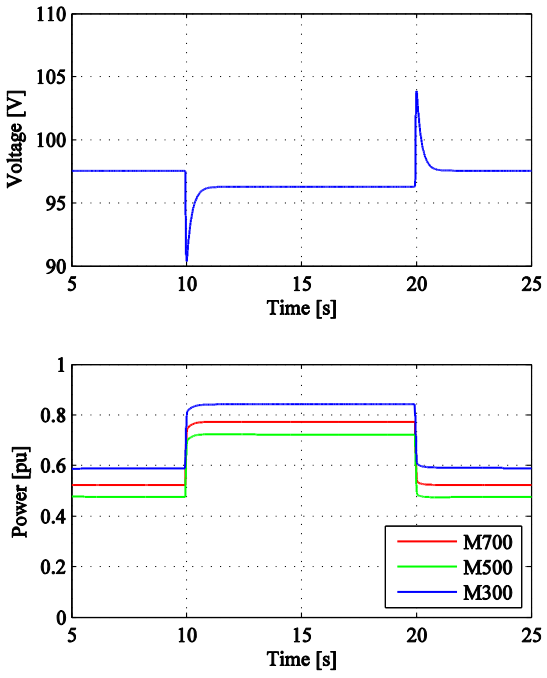
The inner current loop can be implemented by peak current modulation or average current control using PI control or sliding mode control [133], to obtain a 1st-order current response. The time constant of current loop is usually as small as one or several of the current control periods, thus very small compared to that of the voltage loop. In the simulation, the inner current loop is simplified to be a current source, and then the equivalent model of the DG becomes a controllable current sources paralleled with an output capacitor. A PI controller is used for voltage control loop, and the droop resistors are set to 0.05pu, to achieve 5% voltage regulation theoretically. Per unit system is adopted, as it is convenient to compare the performance of the DGs with different rated powers. The base value of voltage, is selected as 100 V for all the DGs while the base current is chosen as the rated current of the individual DG and the base resistance is the ratio of base voltage over base current.

2.4.2 Simulation results

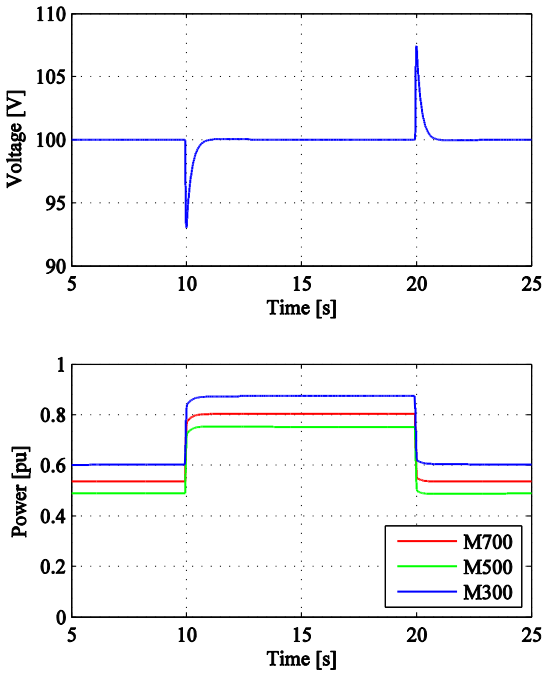
The aforementioned classic droop control, hierarchical structure with secondary central controller (Type AI), dedicated voltage compensation using the common voltage (Type AII), dedicated voltage

compensation with the common current (Type AIII), load sharing compensation with the common current (Type B), voltage compensated using the common voltage and load sharing compensated by common current (Type CI), and the proposed compensation method (Type CII) using the common current are all simulated to compare their steady-state performances. A load step is applied to test the performance of these compensation methods. The load steps up from 800 W to 1200 W at t=10s and then steps back at t=20s. The simulation results are shown in Figure 2.10.

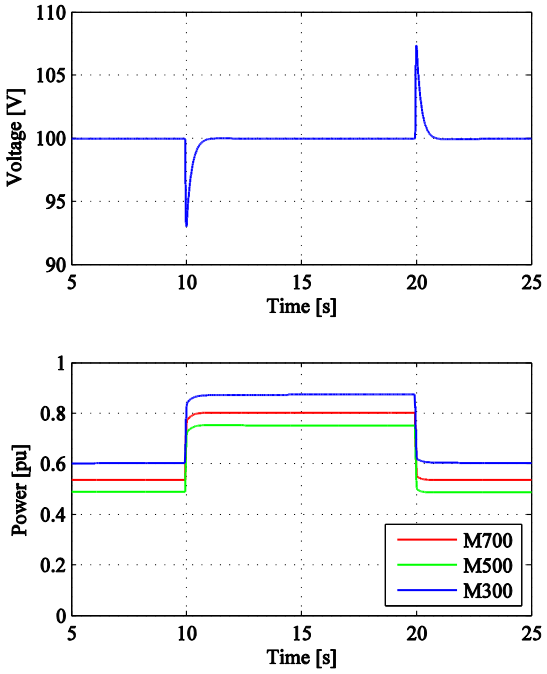
Compared to the classic droop control, Type AI can only restore the DC-bus voltage deviation without any load sharing improvement. Type AII and AIII can obtain similar results as that of Type AI. The DC-bus voltage control still have droop feature in Type AIII, while the DC-bus voltage in Type AI and AII is controlled to be the same value as the reference without steady-state error. On the contrary, Type B can only obtain equal load sharing but the voltage performance is the same as that of the classic droop control. It can be observed from the Figure 2.10g that, the proposed method (Type CII) could enhance both voltage performance and load sharing performances, during different load conditions, which has similar performance as Type CI, but with a more simple compensation structure and lighter communication burden.



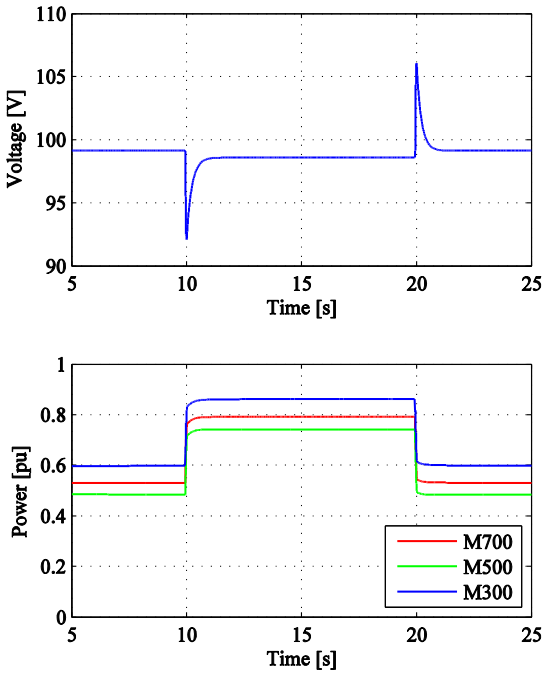
(a) Type A – Classic droop control. Without communication, the drop in voltage is adjusted by the droop resistance, and heavy load leads to larger drop in voltage; the load sharing performance of the three modules are compared in per unit, the load cannot be shared proportionally due to the unequal line impedances as well as the nominal voltage reference offsets.



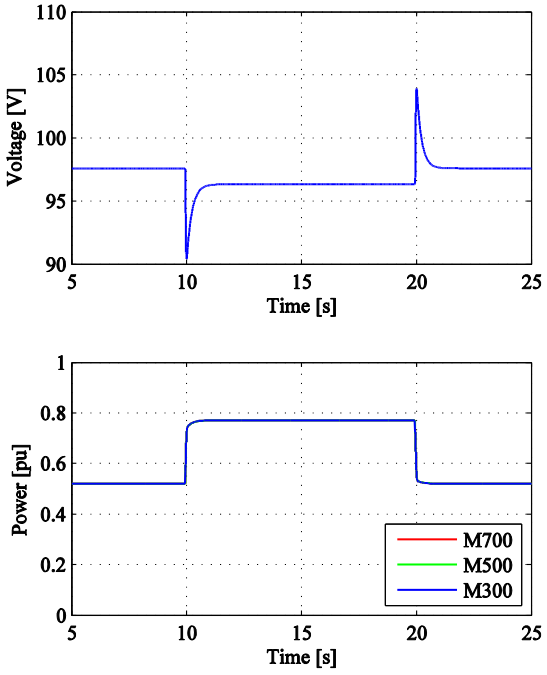
(b) Type AI – Hierarchical structure with secondary control. With the introduction of secondary voltage control at PCC, the static voltage is controlled at the reference point no matter heavy load or light load is applied. The load sharing error among the three modules cannot be compensated.



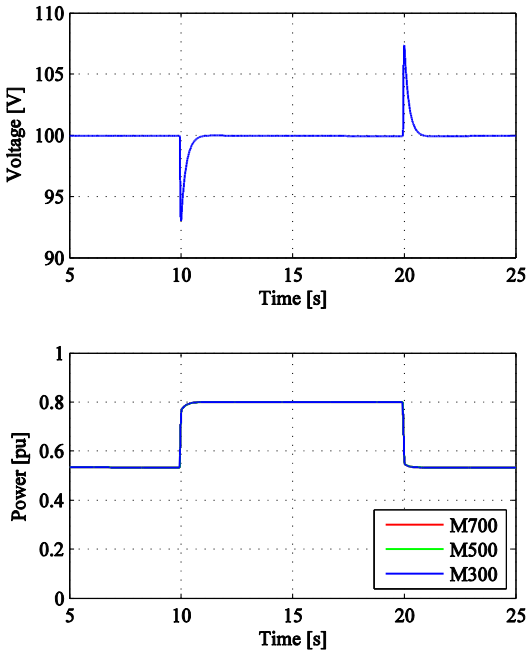
(c) Type AII – Dedicated voltage compensation using common voltage. With the dedicated voltage compensation at each local controller, the static voltage is controlled without error as Type AI. No improvement can be observed in the load sharing performance.



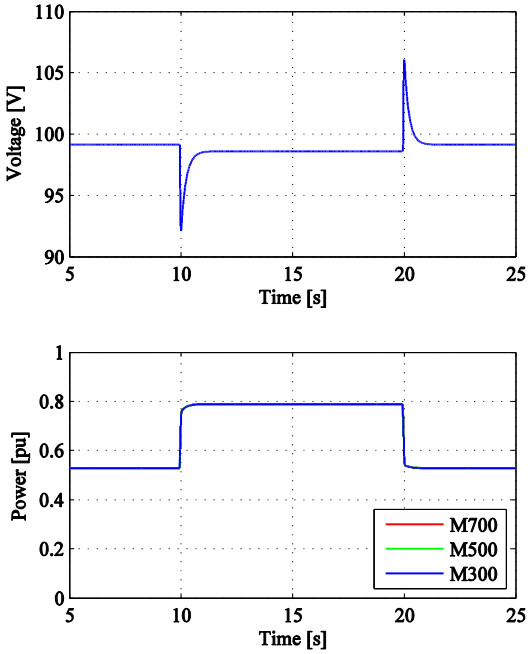
(d) Type AIII – Dedicated voltage compensation using common current. With the help of dedicate communication line, the common current (normalized global average current) is generated in each module. The droop effect can be partially compensated by the common current, and the drop in voltage is reduced. The load sharing performance is the same as that of classic droop control.



(e) Type B – Load sharing compensation using common current. Similar to Type AIII, the common current is generate in each module. But this common current is used as reference and local currents are controlled to follow this reference. Thus proportional load sharing is achieved and no improvement in voltage performance.



(f) Type CI – Mixed compensation using common current and voltage. The common current and voltage references are generated with the aid of dedicated communication line. Like the combination of Type AII and Type B, it can achieve good performances in both voltage and load sharing.



(g) Type CII – Mixed compensation using common current (proposed method). The generated common current is utilized to compensate voltage as Type AIII and load sharing error as Type B. It can achieve good voltage performance and proportional load sharing with a simple structure.

Figure 2.10 Simulation results of different compensation methods. The droop resistance is 0.05pu for every module, and the voltage compensation coefficient adopted in Type AIII and Type CII is 0.02pu.

2.4.3 *Evaluation of the compensation methods*

To evaluate the performances of the compensation methods, some metrics are introduced to achieve quantitative comparison, i.e., the voltage regulation index and the load sharing index.

The voltage regulation index VI is utilized to reflect the overall DC-bus voltage deviation from the nominal voltage, which is defined by:

$$\mathrm{VI} = \sqrt{\frac{\sum_{t=1}^{T}(V_t - V_N)^2}{T}} \tag{2.23}$$

where T is number of the sampling points to be considered; V_N is the DC-bus nominal voltage. A zero VI value indicates a perfect voltage regulation without error, and higher VI means larger DC bus voltage deviation.

Similar as the voltage regulation VI, the load sharing index LSI is built to measure the error between the local output current and the common current, which is defined by:

$$\mathrm{LSI} = \sqrt{\frac{\sum_{j=1}^{n}\left(\frac{\sum_{t=1}^{T}\left(I_{j,t} - I_{N,t}\right)^2}{T}\right)}{n}} \tag{2.24}$$

where n is the number of DGs; $I_{j,t}$ is the sampling current of the jth DG; and $I_{N,t}$ is the common average current of the n DGs through the microgrid.

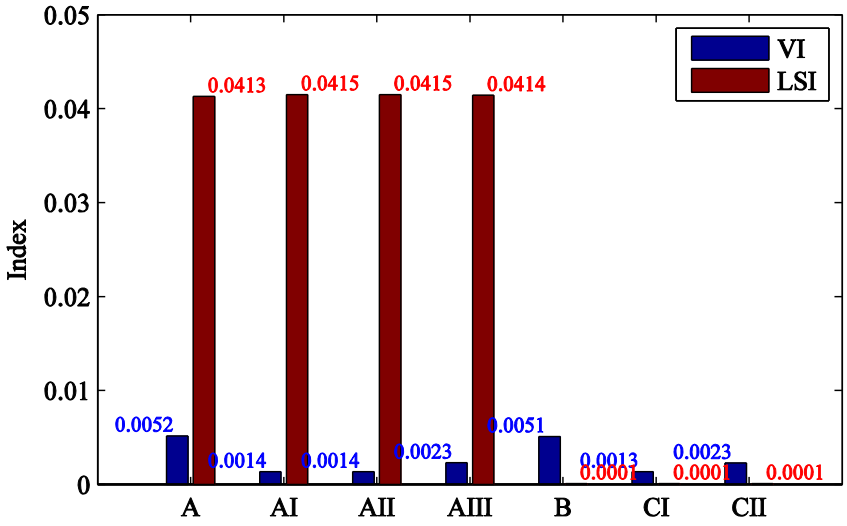


Figure 2.11 Quantitative comparison of the compensation methods

The performances of different compensation methods are evaluated by VI and LSI, the results are given in Figure 2.11. The dark red bars show the VI while the blue bars give the LSI. Type AI, AII

and CI can achieve best voltage performance, i.e., lowest VI. Type B, CI and CII achieve best load sharing performance, i.e., lowest LSI around 0.0001. Overall best performance is achieved by Type CI, and followed by CII, which has simpler structure and flexibility to adjust the voltage regulation.

2.5 Experimental Verification

2.5.1 Experiment setups

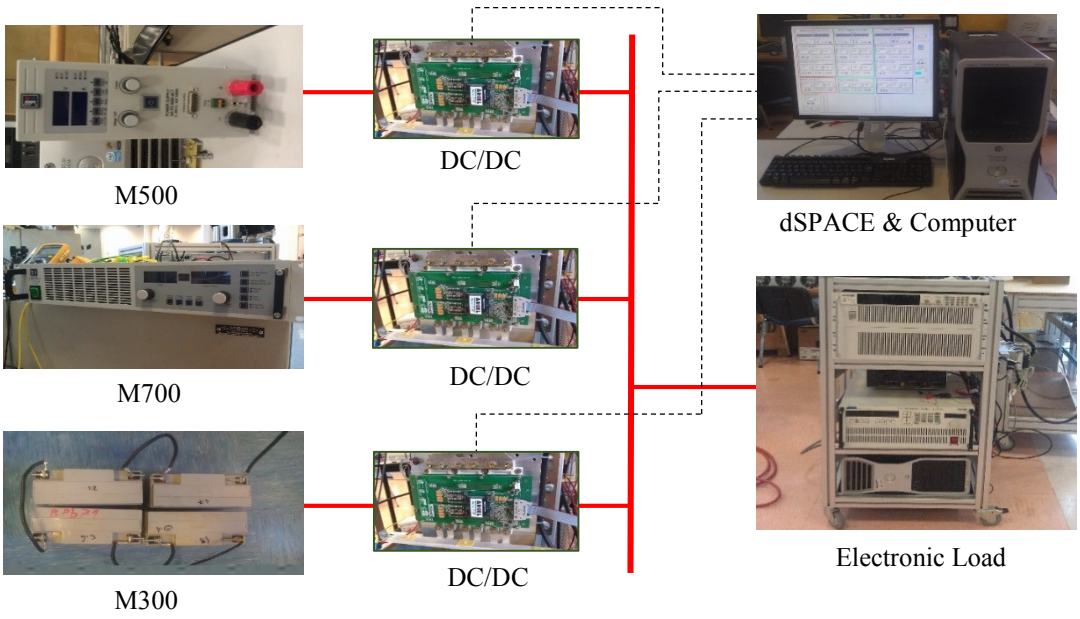


Figure 2.12 Laboratory scale set-up of the DC microgrid

A laboratory scale low-voltage DC microgrid, with three DGs, as shown in Figure 2.12, is developed to test the compensation algorithms. The three DGs are connected to the common DC-bus via boost type DC-DC converters. Similar control structure using droop control with compensation is adopted for each DG. The parameters of the three DGs and the connecting cable parameters are the same as that used in simulations, listed in Table 2.3. M300 is directly connected with load, the others are connected with cables in distance with corresponding cable resistances.

The schematic diagram of the experimental platform is shown in Figure 2.13, in which the output voltages and input currents are sensed using LEM sensors with low-pass filters (the cut-off frequency is 5 kHz). The filtered signals are then fed into analogue to digital conversion (ADC) board to be converted to digital signals for the control loop. It should be noticed that, the adoption of per unit system allows the using of local input current not only local output current. This can reduced the requirement of output current sensors, because the input current sensor is essential for the inner current control loop.

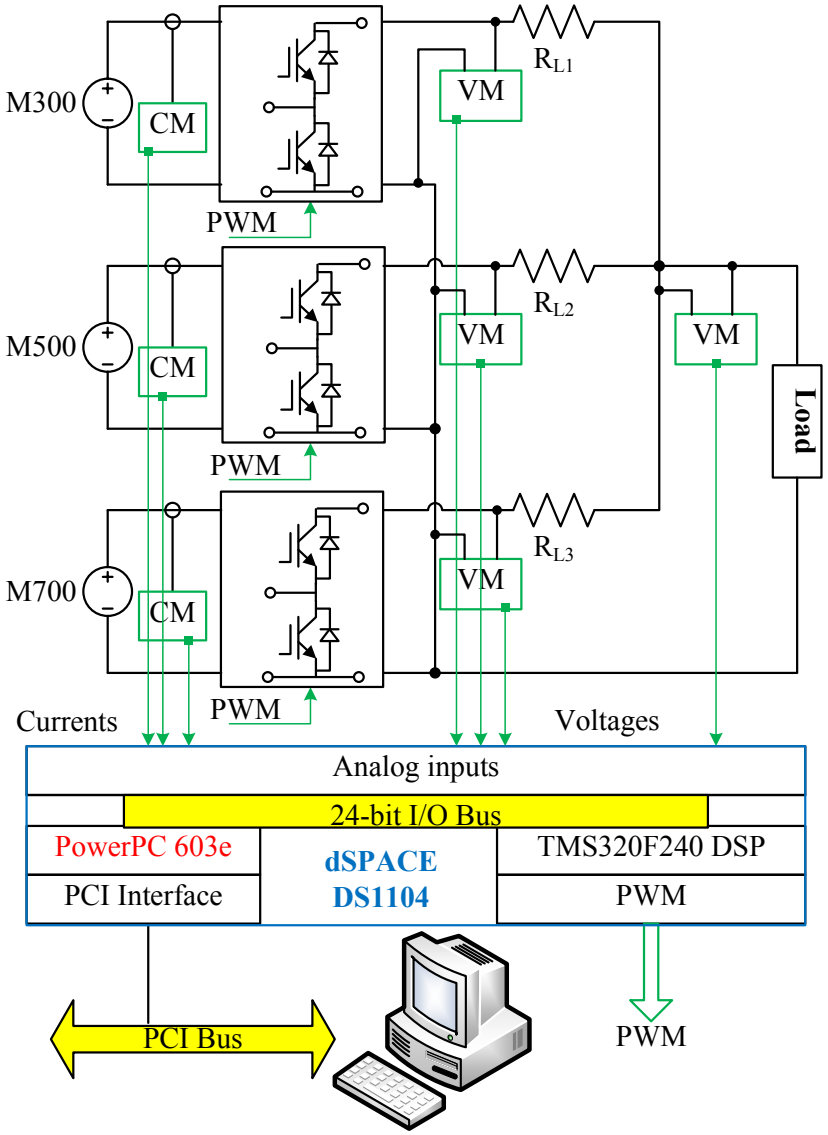


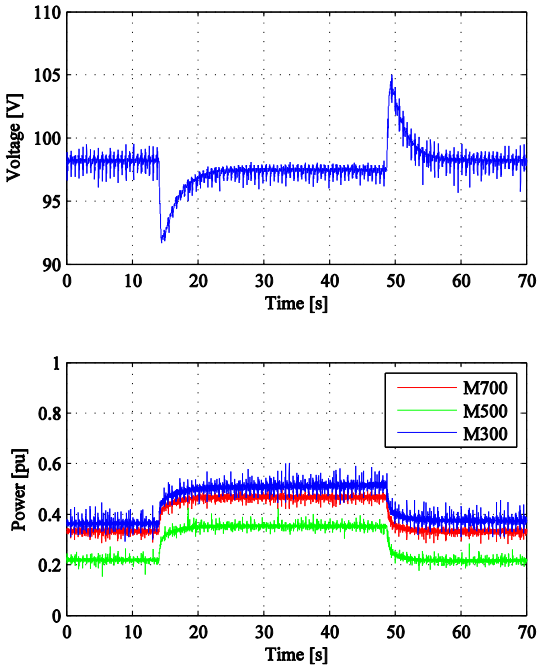
Figure 2.13 The schematic diagram of the laboratory scale DC microgrid

The control algorithms of the three DGs are implemented in a real-time platform dSPACE DS1104. The control implementation includes four sub-units: an inner current loop with the cycle of 0.2 *ms*, a voltage control loop operates every 1.0 *ms*, a droop control unit, and a compensation unit with the time constant of 10 *ms*. Both the current control and voltage control are implemented by simple PI controllers. A five point moving average filter is adapted to the output current signals, before they are used in droop control sub-units and as well as for sharing with low-bandwidth communication. In this experimented test bench, the real digital communication is not implemented but emulated with a time delay of 10 *ms* inserted in the receiving of the current/voltage information. The PWM signals are generated by TMS320F240 chip in DS1104 to control the DC-DC converters.

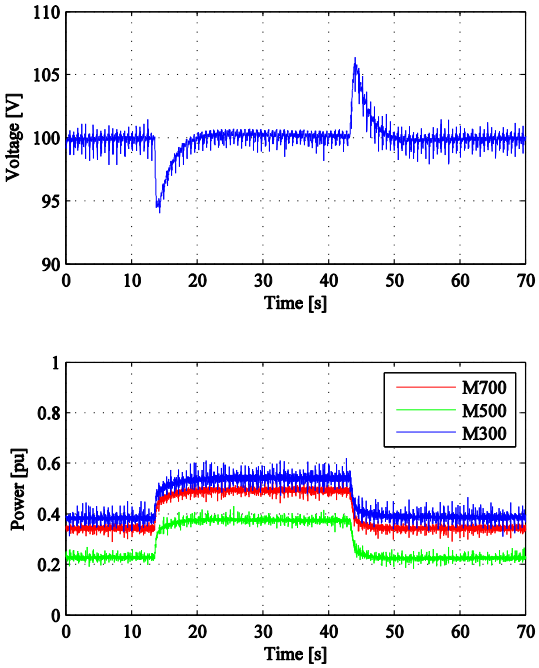
2.5.2 Results and discussion

To verify the performance of the proposed method and to compare with others, resistive load steps are utilized to conduct the experimental tests. The resistive load steps up from 400 W to 600 W at around t=13s and then steps back at around t=50s. Because the load steps are manually manipulated, the step timings for different tests are not exactly the same.

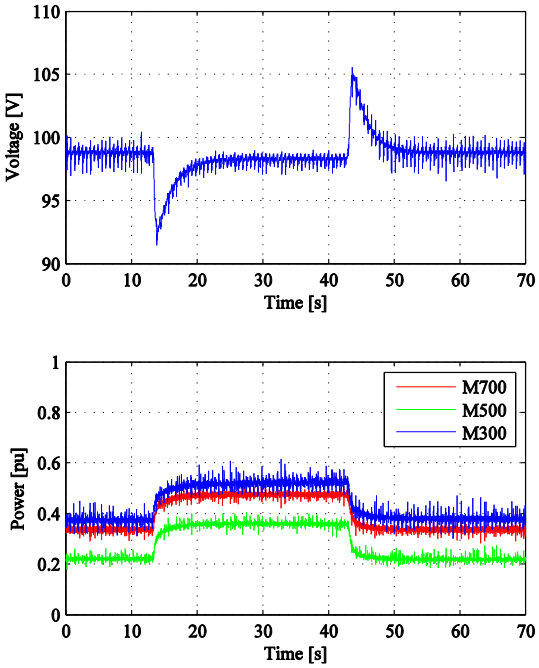
The voltage performance and load sharing performance using the previous discussed compensation methods are shown in Figure 2.14. The same conclusion can be drawn according the comparison of these results. Moreover, it should be noticed that heavier load may cause some DGs go into current limit control mode without load sharing compensation. Under such circumstance, the secondary controller will become ineffective, while the proposed method can overcome this, and operates well during a wider range of load changes.



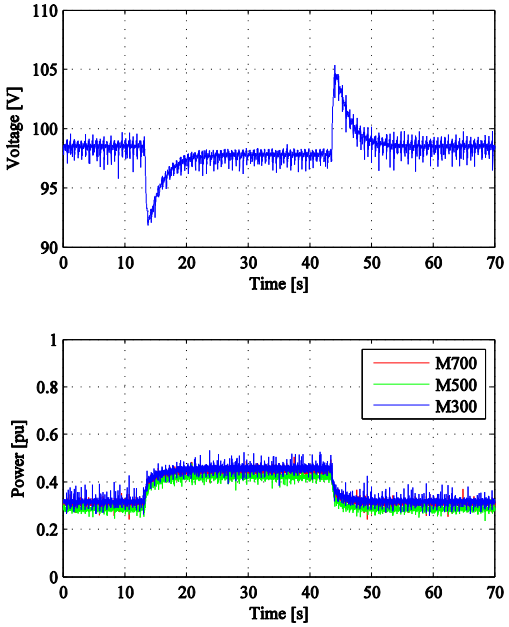
(a) Type A - Classic droop control. The experimental results are similar to the simulation results under classic droop control. The bus voltage drops with heavier load, and the load cannot be shared proportionally. The sensor noises can be observed in the experimental results and not in simulations.



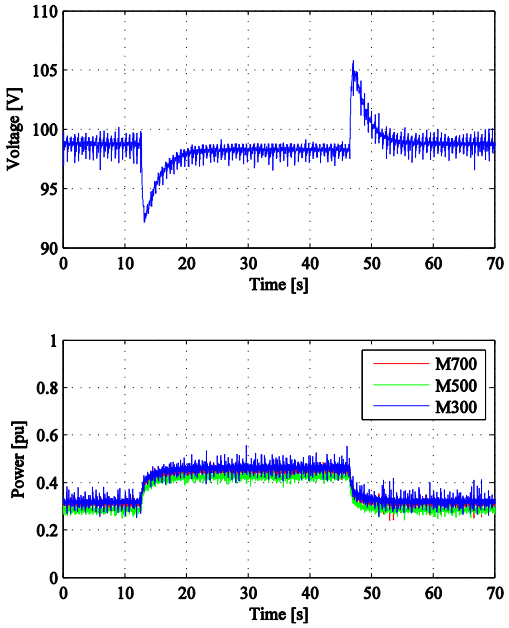
(b) Type AI - Hierarchical structure with secondary control. Similar to the corresponding simulation results, the static voltage can be well compensated without error, while the load sharing error still exists.



(c) Type AIII – Dedicate compensation using common current. Similar to the simulation results, the voltage performance can be enhanced by the adjusting of the voltage compensation constant, while no improvement can be observed in load sharing.



(d) Type B – Load sharing compensation using common current. Using the common current as the reference to control the local current, the three modules can share proportional load with very slight errors. But the voltage performance is similar to that of classic droop control.



(e) Type CII – Mixed compensation using common current (proposed method). Both voltage and load sharing performances are enhanced with the aid of common current, similar to the simulation results. The bus voltage can be adjusted by the voltage compensation constant, while the load is shared proportionally nearly without errors.

Figure 2.14 Voltage and load sharing performance of different control methods. The droop resistance is 0.05pu and the voltage compensation coefficient adopted in Type CII is 0.02pu.

2.6 Conclusion

The classic droop control requires a trade-off to be made between voltage regulation and load sharing, especially when the nominal voltage reference offsets and unequal connecting cable resistances are considered in low-voltage DC microgrids. Although the hierarchical structure with secondary voltage control can be used to restore the voltage drops, there is no improvement in load sharing performance. In this chapter, different droop control compensation methods in literatures with low-bandwidth communication are at first classified and compared. Then a novel mixed compensation method using the common current is proposed to enhance both voltage performance and load sharing performance. Small-signal stability tests are conducted using the reduced-order model to determine the boundaries of the compensation coefficients. Finally, some simulations and experimental tests have been conducted to verify the performance of the proposed method. The obtained results have confirmed its effectiveness. Besides, it should be notice that these compensation methods only deal with the steady-state performance, and the issue of dynamic performance will be discussed in the following chapters.

Chapter 3 Modeling and Analysis of Multi-time Scale DC Microgrids

The analysis of DC microgrid under droop control in the previous chapter doesn't consider the DG's dynamics, only the steady-state performance is analyzed and discussed. The DG under droop control is modeled by the Thévenin theorem as an imperfect voltage source [43]. Then the DC microgrid becomes the parallel of multiple imperfect voltage sources [130]. This modeling approach is adopted in lots of researches when the dynamics of DGs are out of consideration. However, in real applications, different type DGs may have largely different dynamic characteristic, referred as multiple time scales or frequency scales. For example, the grid converter connecting the microgrid to the utility grid requires a smooth power exchange, which indicates a slower dynamic response or large time constant [28]. FCs are usually limited to slower dynamic response to benefit longer life-span, while the super-capacitors or batteries can be used to absorb/supply high frequency power peaks during limited time range, which has fast dynamic response or small time constant [26].

In this chapter, an equivalent circuit composing of a perfect voltage source, droop resistor and virtual inductor is introduced to represent the dynamic model of the DG under droop control. Then, a comprehensive model (CM) and several reduced-order models are developed to conduct small-signal and large-signal stability tests. These reduced order models are constructed based on the assumption of similar time scale and power scale, thus they are not valid anymore in multi-time scale systems. A novel reduced-order multi-scale model (RMM) is proposed to solve this problem. In this proposed model, the DGs with similar time constants are grouped together, and the equivalent DGs represent the groups are connected in parallel, such that RMM not only reduces model complexity but also keeps the major dynamic information. Simulations conducted in MATLAB/Simulink and experimental tests carried out in the laboratory scale test bench have verified the effectiveness of the proposed RMM.

3.1 Modeling DC microgrid components

A general DC microgrid with three DGs is given by Figure 3.1. The three DGs are connected separately through connecting cables to the common load point, where the loads are connected. Droop control (e.g., current/voltage droop or power/voltage droop) is adopted in the local voltage control, such that all three DGs participates in the DC-bus voltage control and the load sharing is automatically achieved.

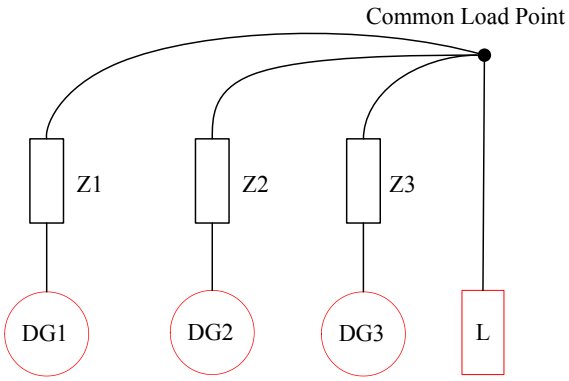


Figure 3.1 A general DC microgrid with three DGs

3.1.1 Equivalent circuit of DGs under droop control

In the classic droop control, only the power scale is considered; i.e., power/voltage droop in DC grid or real power/frequency and reactive power/voltage droop in AC grid. The dynamics of the DG and the inner loops can be introduced as another degree of freedom, referred as the frequency scale or time scale [86]. The frequency or time scale droop control can be realized by a forward path low-pass filter (LPF), feedback LPF added to the classic droop control loop [26], or directly by using a PI controller in the voltage control with an additional droop control loop.

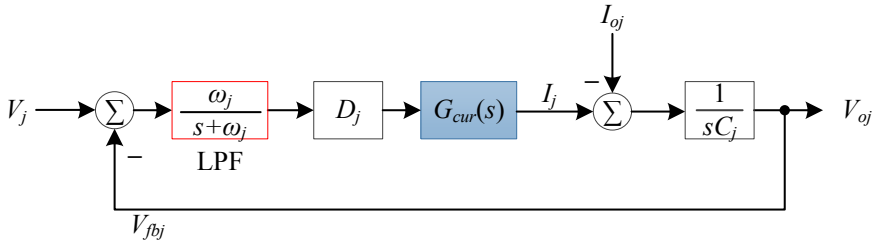


Figure 3.2 Local voltage control using forward path LPF to realize time scale droop control

The analyses of these implementations are similar. Let's take the first method (i.e., traditional droop control with a forward path LPF) as an example, which is shown in Figure 3.2. In the local control, the inner current loop is usually much faster than other loops. Thus the transfer function of current loop can be assumed to be unit $G_{cur}(s) = 1$ to simplify the analysis. The input-to-output voltage open-loop transfer function $G_{vo}(s)$ can be given by:

$$G_{vo}(s) = \frac{D_j \omega_j}{sC_j(s + \omega_j)} \tag{3.1}$$

where the subscript j denotes the jth DG; D_j denotes the droop constant of the jth DG; ω_j denotes the cut-off frequency of the forward path LPF; C_j is the output capacitance. With a unit voltage feedback, the input-to-output voltage closed-loop transfer function $G_{vc}(s)$ is:

$$G_{vc}(s) = \frac{D_j\omega_j}{C_j s^2 + C_j\omega_j s + D_j\omega_j} \tag{3.2}$$

The characteristic polynomial of the voltage closed-loop transfer function for the DG under time scale droop control can then be expressed by:

$$p(s) = s^2 + \omega_j s + \frac{D_j\omega_j}{C_j} \tag{3.3}$$

Given the standard characteristic polynomial of the second order transfer function as:

$$p(s) = s^2 + 2\zeta_{Nj}\omega_N s + \omega_{Nj}^2 \tag{3.4}$$

where the damping ratio ζ_{Nj} of the voltage closed-loop transfer function is:

$$\zeta_{Nj} = \frac{1}{2}\sqrt{\frac{C_j\omega_j}{D_j}} \tag{3.5}$$

And the natural frequency ω_{Nj} of the voltage closed-loop transfer function is:

$$\omega_{Nj} = \sqrt{\frac{D_j\omega_j}{C_j}} \tag{3.6}$$

Then, the voltage error $V_j - V_{oj}$ to source current I_j transfer function is given by:

$$Y_j(s) = \frac{D_j\omega_j}{s + \omega_j} = \frac{1}{R_{dj}(\tau_j s + 1)} \tag{3.7}$$

where V_{oj} is the output voltage of the jth DG as well as the voltage of the output capacitor; $R_{dj} = 1/D_j$ is the droop resistance, which is the inverse of the droop constant; I_j is the current supplied by the jth DG; $\tau_j = 1/\omega_j$, the inverse of the frequency scale ω_j, is the time constant of voltage control loop, and also used to represent the DG's time scale.

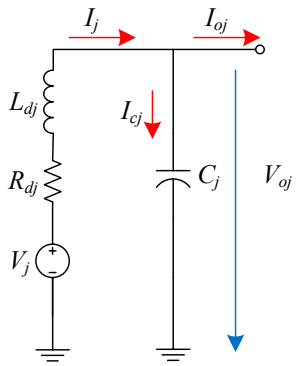


Figure 3.3 The equivalent circuit of the DG under time scale droop control

According to the previous analysis, the equivalent circuit of a time scale droop controlled DG is developed and shown in Figure 3.3. The DG's time scale is represented by the droop resistor and the virtual inductor in series. An output capacitor connected in parallel represents the output voltage dynamics. The time constant τ_j is the ratio of the virtual inductance over the droop resistance.

$$\tau_j = \frac{L_{dj}}{R_{dj}} = \frac{1}{\omega_j} \tag{3.8}$$

This proposed equivalent circuit not only considers the effect of droop control in power scale but also the time scale information, thus it is more precise than the traditional models using only voltage source and resistor in series [91] or current source and capacitor in parallel [71]. An alternative equivalent circuit can be deduced by using Norton form: a perfect current source, resistor, inductor and capacitor connected in parallel. Then, the time domain model of the DG under time scale droop control, deduced from the equivalent circuit, is written as:

$$\begin{cases} \frac{d}{dt} I_j = -\frac{R_{dj}}{L_{dj}} I_j + \frac{1}{L_{dj}} \left(V_j - V_{oj} \right) \\ \frac{d}{dt} V_{oj} = \frac{1}{C_j} \left(I_j - I_{oj} \right) \end{cases} \tag{3.9}$$

where I_{oj} is the current injected into the common DC-bus by the *j*th DG.

The droop constant D_j or droop resistance R_{dj} is determined by the DC-bus voltage performance requirement, the rated voltage and the rated current of the corresponding DG. The value is calculated by:

$$D_j = \frac{1}{R_{dj}} = \frac{I_{Nj}}{\delta(1-\delta)V_{Nj}} = \frac{1000 P_{Nj}}{\delta(1-\delta)V_{Nj}^2} \tag{3.10}$$

where V_{Nj}, I_{Nj} are the rated output voltage and current of the *j*th DG; P_{Nj} is the rated power of the *j*th DG in kW; δ is the voltage tolerance in percentage. Larger voltage tolerance indicates poorer voltage performance.

Assume the damping ratio of the voltage loop is controlled to be $\zeta_{Nj} = \sqrt{2}/2$, and the voltage tolerance is selected to 5% around 380 V. Then the DC-bus capacitance can be calculated by:

$$C_j = \frac{2D_j}{\omega_j} = \frac{2000 \tau_j P_{Nj}}{\delta(1-\delta)V_{Nj}^2} = 291.6 \times 10^{-3} \tau_j P_{Nj} \tag{3.11}$$

When the time constant is 0.01 *s* the required DC-bus capacitance ratio is 2916 μF/kW. Assume the DC-bus capacitance are equally distributed into the sources and loads, the capacitance ratio for DGs

can be chosen half of the DC-bus capacitance ratio (i.e., 1458 μF/kW) which is referred as the basic capacitance ratio.

3.1.2 Equivalent circuit of connecting cables

The lumped model of connecting cables is usually presented by Γ or Π type equivalent circuit. In the latter, the capacitances can be viewed distributed to the output of the DGs and the input of loads, and then the equivalent circuit is formed as the series connection of a resistor and the corresponding inductor.

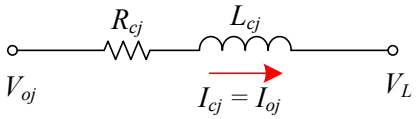


Figure 3.4 The equivalent circuit of the connecting cable between the *j*th DG to the common load point

Consider a DC microgrid with *n* DGs, the DGs are connected to the common load point with separate equivalent cables. The equivalent circuit of one connecting cable is shown in Figure 3.4. The time domain model of the cable between the *j*th DG and the common load point is:

$$\frac{d}{dt}I_{cj} = -\frac{R_{cj}}{L_{cj}}I_{cj} + \frac{1}{L_{cj}}(V_{oj} - V_L) \tag{3.12}$$

where I_{cj} denotes the current flowing from the *j*th DG to the common load point through the connecting cable, and it equals to the output current of the *j*th DG; R_{cj}, L_{cj} are equivalent cable resistance and inductance, respectively; and V_L is the voltage at the common load point.

3.1.3 Equivalent circuit of general loads

Neglecting fast dynamics, a general DC microgrid load could be Constant Resistive Load (CRL), Constant Current Load (CCL), Constant Power Load (CPL), or Constant Voltage Load (CVL). Thus a general load can be written as:

$$P_L = P_{CPL} + P_{CRL} + P_{CCL} + P_{CVL} \tag{3.13}$$

where $P_{CPL}, P_{CRL}, P_{CCL}$ and P_{CVL} are the power of CPL, CRL, CCL and CVL at rated DC-bus voltage, respectively.

The nonlinear relationship of the load current and the load voltage in ideal CPL is written by:

$$I_{L11} = \frac{P_{CPL}}{V_L} \tag{3.14}$$

where I_{L11} is the current absorbed by the CPL. The linearized model can be obtained using *Taylor* expansion at the operation load voltage V_e. Then the equivalent circuit of the linearized CPL is given by Figure 3.5a, and the load current is:

$$I_{L11} \approx I_{CPL} + \frac{V_L}{R_{CPL}} = 2\frac{P_{CPL}}{V_e} - \frac{P_{CPL}}{V_e^2}V_L \tag{3.15}$$

The equivalent circuit of CPL is composed of a negative resistor $R_{CPL} = -V_e^2/P_{CPL}$ and a current sink $I_{CPL} = 2P_{CPL}/V_e$, which are connected in parallel.

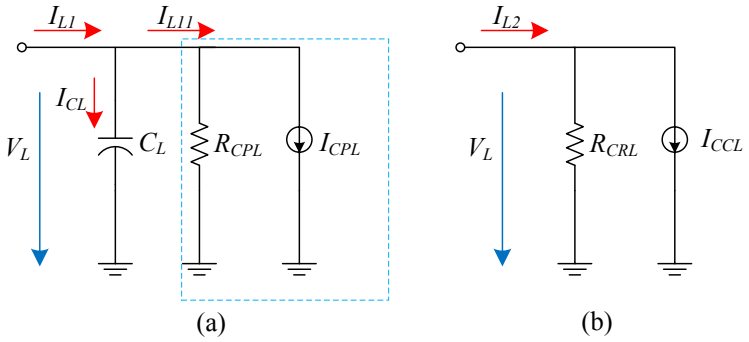


Figure 3.5 The equivalent circuit of the (a) Constant Power Load, (b) combined Constant Current Load and Constant Resistance Load or Constant Voltage Load

According to Kirchhoff's Current Law (KCL), the model of the input capacitor at CPL is written as:

$$\frac{d}{dt}V_L = \frac{1}{C_L}(I_{L1} - I_{L11}) \tag{3.16}$$

where I_{L1} denotes the input current supplying CPL; C_L is the equivalent input capacitance of loads.

A non-ideal CVL as well as the combination of CRL and CCL can also be represented by a resistor and a current sink connected in parallel, as shown in Figure 3.5b. The current flowing into the loads is:

$$I_{L2} = \frac{V_L}{R_{CRL}} + I_{CCL} \tag{3.17}$$

where R_{CRL} denotes the resistance of CRL; I_{CCL} denotes the current sink of CCL.

Thus, the total load current is the sum of all the load currents:

$$I_L = I_{L1} + I_{L2} \tag{3.18}$$

where I_L denotes the total current flowing to loads.

3.2 Modeling single bus DC microgrids

3.2.1 Comprehensive model

Consider a single bus DC microgrid with *n* DGs, the DGs are connected to the common load point through separate cables. The model with *n* DGs, deduced from the single DG model, is expressed in matrix notion by:

$$\frac{d}{dt}\boldsymbol{I} = -\boldsymbol{W_d I} + \boldsymbol{Y_d}(\boldsymbol{V} - \boldsymbol{V_o}) \tag{3.19}$$

where the state variables vector is $\boldsymbol{I} = [I_1 \quad I_2 \quad \dots \quad I_n]^{\mathrm{T}}$; the voltage reference vector is $\boldsymbol{V} = [V_1 \quad V_2 \quad \dots \quad V_n]^{\mathrm{T}}$ and the output voltage vector is $\boldsymbol{V_o} = [V_{o1} \quad V_{o2} \quad \dots \quad V_{on}]^{\mathrm{T}}$. The inverses time constant matrix and inverse inductance matrix are:

$$\boldsymbol{W_d} = \mathrm{diag}\left(\frac{R_{d1}}{L_{d1}} \quad \frac{R_{d2}}{L_{d2}} \quad \dots \quad \frac{R_{dn}}{L_{dn}}\right)_{n\times n} \tag{3.20}$$

$$\boldsymbol{Y_d} = \mathrm{diag}\left(\frac{1}{L_{d1}} \quad \frac{1}{L_{d2}} \quad \dots \quad \frac{1}{L_{dn}}\right)_{n\times n} \tag{3.21}$$

where the diagonal components of state matrix $\boldsymbol{W_d}$ are the inverses of DGs' time constants. The model of the output capacitance for the DGs is rewritten by:

$$\frac{d}{dt}\boldsymbol{V_o} = \boldsymbol{G_o}(\boldsymbol{I} - \boldsymbol{I_o}) \tag{3.22}$$

where the output current vector is $\boldsymbol{I_o} = [I_{o1} \quad I_{o2} \quad \dots \quad I_{on}]^{\mathrm{T}}$. The inverse output capacitance matrix is given by:

$$\boldsymbol{G_o} = \mathrm{diag}\left(\frac{1}{C_1} \quad \frac{1}{C_2} \quad \dots \quad \frac{1}{C_n}\right)_{n\times n} \tag{3.23}$$

All the DGs are viewed connecting through separate cables to the common load point, so the output current equals to the current goes through the corresponding connecting cable.

$$I_{cj} = I_{oj} \text{ or } \boldsymbol{I_c} = \boldsymbol{I_o} \tag{3.24}$$

where $\boldsymbol{I_c} = [I_{c1} \quad I_{c2} \quad \dots \quad I_{cn}]^{\mathrm{T}}$ denotes the connecting cable currents flowing into the common load point. The differential equations of *n* connecting cables are:

$$\frac{d}{dt}\boldsymbol{I_o} = -\boldsymbol{W_c I_o} + \boldsymbol{Y_c}(\boldsymbol{V_o} - \boldsymbol{E}V_L) \tag{3.25}$$

where $\boldsymbol{E} = [1 \quad 1 \quad \dots \quad 1]^T_{n\times 1}$ is the one vector. The inverse cable time constant matrix and inverse cable inductance matrix are:

$$\boldsymbol{W_c} = \text{diag}\begin{pmatrix}\frac{R_{c1}}{L_{c1}} & \frac{R_{c2}}{L_{c2}} & \dots & \frac{R_{cn}}{L_{cn}}\end{pmatrix}_{n\times n} \tag{3.26}$$

$$\boldsymbol{Y_c} = \text{diag}\begin{pmatrix}\frac{1}{L_{c1}} & \frac{1}{L_{c2}} & \dots & \frac{1}{L_{cn}}\end{pmatrix}_{n\times n} \tag{3.27}$$

The total current I_s supplied by the DGs is expressed by:

$$I_s = \sum_1^n I_{oj} = \boldsymbol{E}^T \boldsymbol{I_o} \tag{3.28}$$

when (3.17), (3.18) and (3.28) are substituted into (3.16), the differential equation of the load can be rewritten as:

$$\frac{d}{dt}V_L = \frac{1}{C_L}\boldsymbol{E}^T\boldsymbol{I_c} - \frac{1}{R_L C_L}V_L - \frac{1}{C_L}I_{CC} \tag{3.29}$$

where R_L denotes the equivalent total load resistance:

$$R_L = R_{CRL} \parallel R_{CPL} \tag{3.30}$$

and I_{CC} denotes the equivalent total current sink:

$$I_{CC} = I_{CPL} + I_{CCL} \tag{3.31}$$

The DC microgrid model can be formed by the combination of the differential equations of DGs (3.19), output capacitors (3.22), connecting cables (3.25), and the load (3.29), referred as the comprehensive model (CM). The equivalent circuit of the DC microgrid including *n* DGs is given by Figure 3.6 and the linearized model in matrix notation is rewritten by:

$$\frac{d}{dt}\boldsymbol{X} = \boldsymbol{AX} + \boldsymbol{BU} \tag{3.32}$$

where state variable vector is $\boldsymbol{X} = [\boldsymbol{I} \quad \boldsymbol{I_c} \quad \boldsymbol{V_o} \quad V_L]^T$; input variable vector is $\boldsymbol{U} = [\boldsymbol{V} \quad I_{CC}]^T$. The state matrix and the input matrix are:

$$\boldsymbol{A} = \begin{bmatrix} -\boldsymbol{W_d} & \boldsymbol{0}_{n\times n} & -\boldsymbol{Y_d} & \boldsymbol{0}_{n\times 1} \\ \boldsymbol{0}_{n\times n} & -\boldsymbol{W_c} & \boldsymbol{Y_c} & -\boldsymbol{Y_c}\boldsymbol{E} \\ \boldsymbol{G_o} & -\boldsymbol{G_o} & \boldsymbol{0}_{n\times n} & \boldsymbol{0}_{n\times 1} \\ \boldsymbol{0}_{1\times n} & \frac{1}{C_L}\boldsymbol{E}^T & \boldsymbol{0}_{1\times n} & -\frac{1}{R_L C_L} \end{bmatrix}_{(3n+1)\times(3n+1)} \tag{3.33}$$

$$\boldsymbol{B} = \begin{bmatrix} \boldsymbol{Y_d} & \boldsymbol{0}_{n\times 1} \\ \boldsymbol{0}_{n\times n} & \boldsymbol{0}_{n\times 1} \\ \boldsymbol{0}_{n\times n} & \boldsymbol{0}_{n\times 1} \\ \boldsymbol{0}_{1\times n} & -\frac{1}{C_L} \end{bmatrix}_{(3n+1)\times(n+1)} \tag{3.34}$$

CM has the order of $3n+1$, where n is the number of DGs in the examined microgrid. When the number of DGs is high, the system becomes too complicated to be analyzed. Thus some model reduction technologies need to be performed.

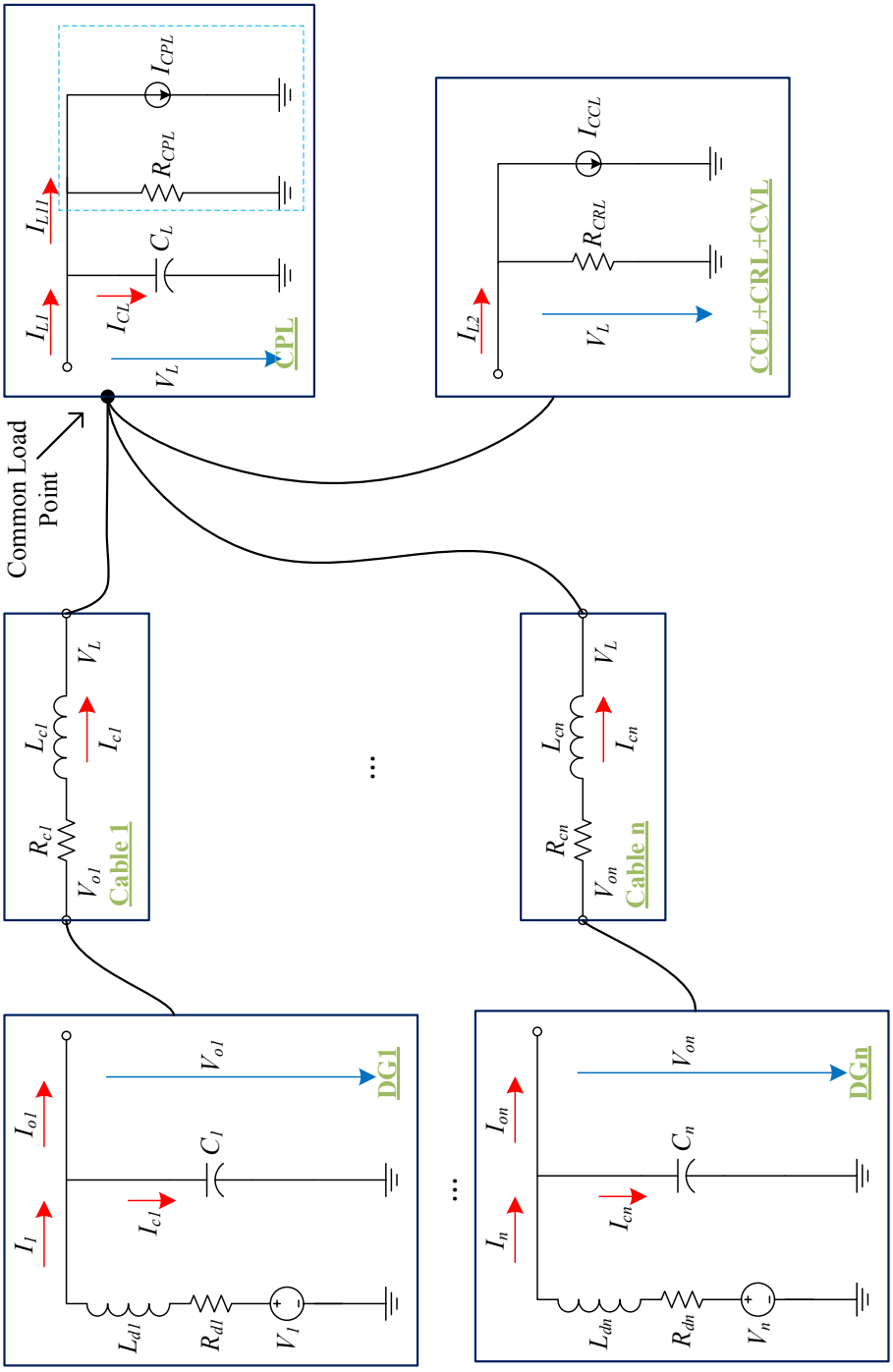


Figure 3.6 The equivalent circuit of a single bus DC microgrid with n DGs

3.2.2 Reduced 4th-order model

One popular method to study DC microgrids is to use the lumped mean circuit values (e.g., resistance, inductance, capacitance, current and voltage) to replace the distributed values, when they are similar [92]. In particular, this method is applicable to small-scale microgrids with similar DGs. Considering a small-scale DC microgrid with single time scale, thus the time constants of the droop controlled DGs can be considered same. The power scales are comparable such that the droop resistances and virtual inductances are approximate.

$$\begin{cases} \dfrac{R_{d1}}{L_{d1}} \cong \dfrac{R_{d2}}{L_{d2}} \cong \cdots \cong \dfrac{\bar{R}_d}{\bar{L}_d} \\ \dfrac{1}{L_{d1}} \cong \dfrac{1}{L_{d2}} \cong \cdots \cong \dfrac{1}{\bar{L}_d} \end{cases} \tag{3.35}$$

where $\bar{R}_d$ and $\bar{L}_d$ are the mean values of R_{dj} and L_{dj}, respectively.

Regarding the DGs, they are assumed to have the similar nominal voltage references:

$$V_1 \cong V_2 \cong \cdots \cong V_n \cong V_N \tag{3.36}$$

where V_N is the common voltage reference for the DGs. Thus the model of DGs under droop control in (3.19) and (3.22) can be simplified to:

$$\begin{cases} \dfrac{d}{dt}\bar{I} = -\dfrac{\bar{R}_d}{\bar{L}_d}\bar{I} + \dfrac{1}{\bar{L}_d}(V_N - \bar{V}_o) \\ \dfrac{d}{dt}\bar{V}_o = \dfrac{1}{\bar{C}}(\bar{I} - \bar{I}_c) \end{cases} \tag{3.37}$$

where $\bar{I}$ and $\bar{V}_o$ are the mean values of I_j and V_{oj}, respectively; $\bar{C}$ is the mean value of C_j.

Suppose all the connecting cables between DGs and the common load are the same type, thus the impedance per length is the same as well as the ratio of inductance over resistance [92]. Assuming close distances, it yields:

$$\begin{cases} \dfrac{R_{1L}}{L_{1L}} \cong \dfrac{R_{2L}}{L_{2L}} \cong \cdots \cong \dfrac{\bar{R}_c}{\bar{L}_c} \\ \dfrac{1}{L_{1L}} \cong \dfrac{1}{L_{2L}} \cong \cdots \cong \dfrac{1}{\bar{L}_c} \end{cases} \tag{3.38}$$

where $\bar{R}_c$ and $\bar{L}_c$ denote the mean values of R_{cj} and L_{cj}, respectively. Therefore the *n* differential equations of cables in (3.25) can be combined and simplified to:

$$\frac{d}{dt}\bar{I}_c = -\frac{\bar{R}_c}{\bar{L}_c}\bar{I}_c + \frac{1}{\bar{L}_c}(\bar{V}_o - V_L) \tag{3.39}$$

where the state variable $\bar{I}_c$ denotes the average value of I_{cj}.

The corresponding load model for the equivalent average DG can also be given by:

$$\frac{d}{dt}V_L = \frac{1}{\bar{C}_L}(\bar{I}_c - \frac{V_L}{\bar{R}_L} - \bar{I}_{CC}) \tag{3.40}$$

where $\bar{R}_L, \bar{C}_L, \bar{I}_{CC}$ denote the equivalent parameters of the load, and they are calculated by:

$$\begin{cases} \bar{R}_L = n \times R_L \\ \bar{I}_{CC} = \dfrac{I_{CCL}}{n} + \dfrac{I_{CPL}}{n} \\ \bar{C}_L = \dfrac{C_L}{n} \end{cases} \tag{3.41}$$

Thus a reduced 4th-order model (R4M) (3.42) of the DC microgrid can be obtained by combining (3.37), (3.39) and (3.40), and the state-space form is given by (3.42). The equivalent circuit is shown in Figure 3.7, which can be viewed as a voltage source supplying power to a load through cascaded low-pass *RLC* filters.

$$\frac{d}{dt}\begin{bmatrix} \bar{I} \\ \bar{I}_c \\ \bar{V}_o \\ V_L \end{bmatrix} = \begin{bmatrix} -\dfrac{\bar{R}_d}{\bar{L}_d} & 0 & -\dfrac{1}{\bar{L}_d} & 0 \\ 0 & -\dfrac{\bar{R}_c}{\bar{L}_c} & \dfrac{1}{\bar{L}_c} & -\dfrac{1}{\bar{L}_c} \\ \dfrac{1}{\bar{C}} & -\dfrac{1}{\bar{C}} & 0 & 0 \\ 0 & \dfrac{1}{\bar{C}_L} & 0 & -\dfrac{1}{\bar{C}_L\bar{R}_L} \end{bmatrix}\begin{bmatrix} \bar{I} \\ \bar{I}_c \\ \bar{V}_o \\ V_L \end{bmatrix} + \begin{bmatrix} \dfrac{1}{\bar{L}_d} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & -\dfrac{1}{\bar{C}_L} \end{bmatrix}\begin{bmatrix} V_N \\ \bar{I}_{CC} \end{bmatrix} \tag{3.42}$$

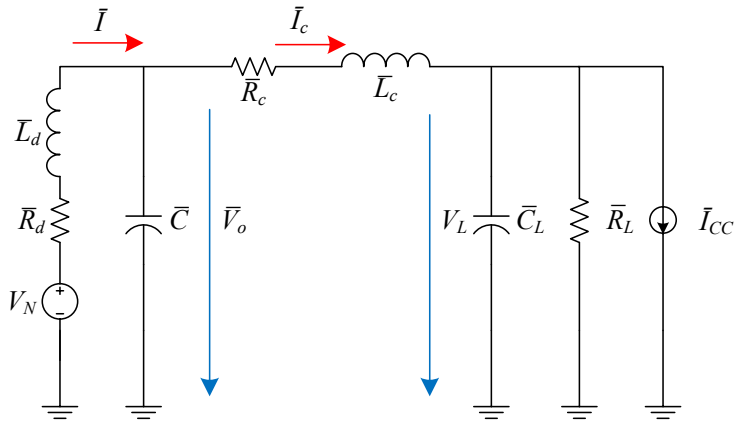


Figure 3.7 Equivalent circuit of the DC microgrid in R4M

3.2.3 *Reduced 2nd-order model*

Most often, in small-scale low-voltage DC microgrids, the connecting cables are considered to be resistive, because the DG's time constant is much larger than that of the connecting cable (the ratio of the cable inductance over the cable resistance).

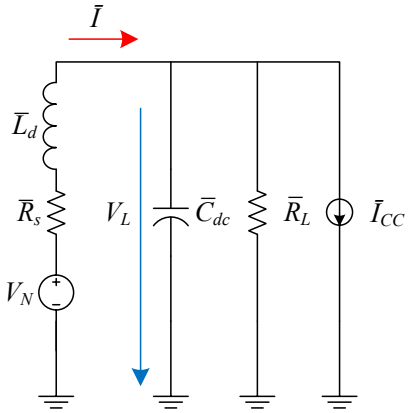


Figure 3.8 Equivalent circuit of the DC microgrid in R2M

The effect of the cascaded low-pass *RLC* filters in R4M is dominated by the one with narrower bandwidth. The wider bandwidth filter introduced by the connecting cable has very limited influence thus it can be further neglected. Therefore the cable inductance is negligible; i.e., resistive cable, and the cable resistance can be further fused with the droop resistance. This simplification leads to a reduced 2nd-order model (R2M), as shown in Figure 3.8. The output capacitors and the input capacitor of the load are also combined to form the DC-bus capacitor. The model in state-space form is expressed as:

$$\frac{d}{dt}\begin{bmatrix}\bar{I}\\ V_L\end{bmatrix}=\begin{bmatrix}-\frac{\bar{R}_s}{\bar{L}_d} & -\frac{1}{\bar{L}_d}\\ \frac{1}{\bar{C}_{dc}} & -\frac{1}{\bar{C}_{dc}\bar{R}_L}\end{bmatrix}\begin{bmatrix}\bar{I}\\ V_L\end{bmatrix}+\begin{bmatrix}\frac{1}{\bar{L}_d} & 0\\ 0 & -\frac{1}{\bar{C}_{dc}}\end{bmatrix}\begin{bmatrix}V_N\\ \bar{I}_{CC}\end{bmatrix} \tag{3.43}$$

where $\bar{R}_s = \bar{R}_d + \bar{R}_c$ denotes the equivalent source resistance for the equivalent DG, which are the combination of the cable resistance and the droop resistance; $\bar{C}_{dc} = \bar{C} + \bar{C}_L$ is the equivalent DC-bus capacitance, which is the sum of the DG's output capacitance and the load's input capacitance.

3.2.4 *Comparison of the three models*

The previously presented reduced-order models are based on the similarity of connecting cables and the similarity of DGs' time scales. When the cable parameters or the time constants of DGs are largely different, the reduced-order models may lead to significant errors. R2M is further deduced under the assumption of neglectable cable inductance.

The reduced-order models can be easily adopted to conduct the DC microgrid stability tests, as well as to size the bus capacitor due to their low order. However the load sharing performance can only be observed in CM, because the reduced-order models doesn't contain details of every single DG.

The primary comparisons of the three models are conducted in frequency and time domains to confirm the validities of the reduced models. The stability of the system depends on the locations of eigenvalues of state matrices. The eigenvalues of the state matrices of CM, R4M and R2M are shown in Figure 3.9, for a typical DC microgrid with three DGs. The parameters of the examined DC microgrid are listed in Table 3.1, and the capacitance ratio is selected equal to 10% of the basic value (i.e., 145.8 μF/kW). CM has the order of ten, as well as ten eigenvalues. The six eigenvalues of CM with large real parts are represented by two eigenvalues in R4M, and further disappeared in R2M. The eigenvalues nearby the origin are shown in the second graph of Figure 3.9. Both the reduced-order models have similar eigenvalues as that of CM, which indicates the effectiveness of reduced model to be used for the analysis of the original system, when similar DGs' time scales are applied.

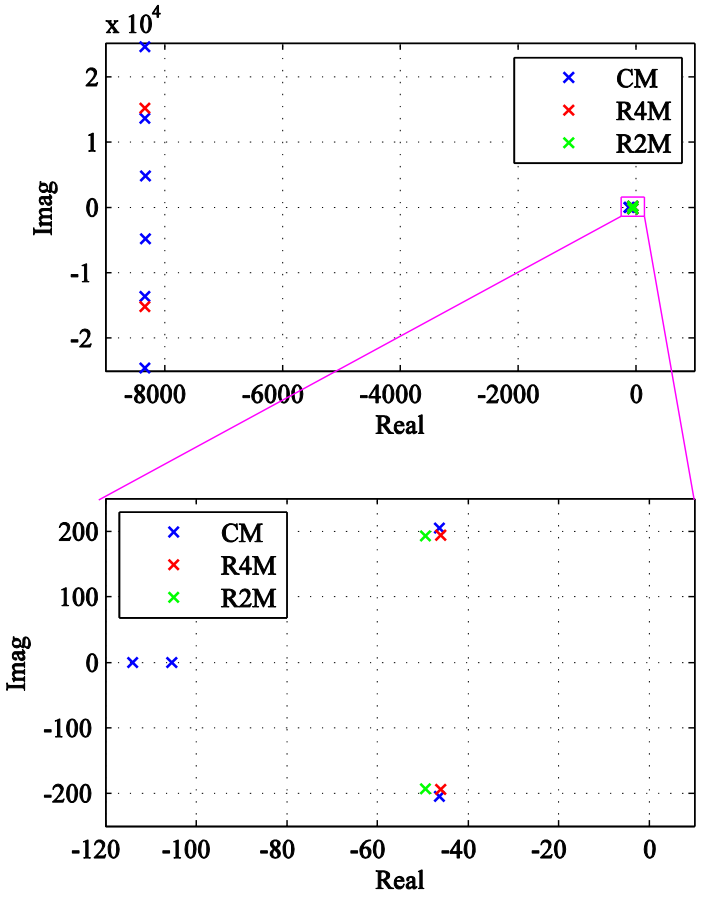


Figure 3.9 The eigenvalues of the state matrices in CM, R4M and R2M

Table 3.1 The parameters of the investigated DC microgrid

	Power	Equiv. res.	Equiv. induct.	Time const.	Length
DG1	1.0 kW	*7.22 Ω	*72.2 mH	*0.01 *s*	
DG2	0.5 kW	14.44 Ω	144 mH	0.01 *s*	
DG3	1.0 kW	7.22 Ω	72.2 mH	0.01 *s*	
Cable 1		0.25 Ω	15 µH		50 m
Cable 2		1.00 Ω	60 µH		200 m
Cable 3		1.50 Ω	90 µH		300 m

* Nominal values, different values are used in simulations and analysis

Time domain simulations are also conducted in MATLAB/Simulink to verify the reduced-order models. A combination load of CPL 1500 W, CRL 288.8 Ω and variable CCL is applied. With CCL steps from 0.0 A to 1.0 A at t=0.5s, the voltage and current performances in different models are shown in Figure 3.10, Figure 3.11 and Figure 3.12. The reduced-order models keep the major voltage and current dynamics properly during CCL step. However, the DGs' load sharing performance cannot be observed in the reduced-order models.

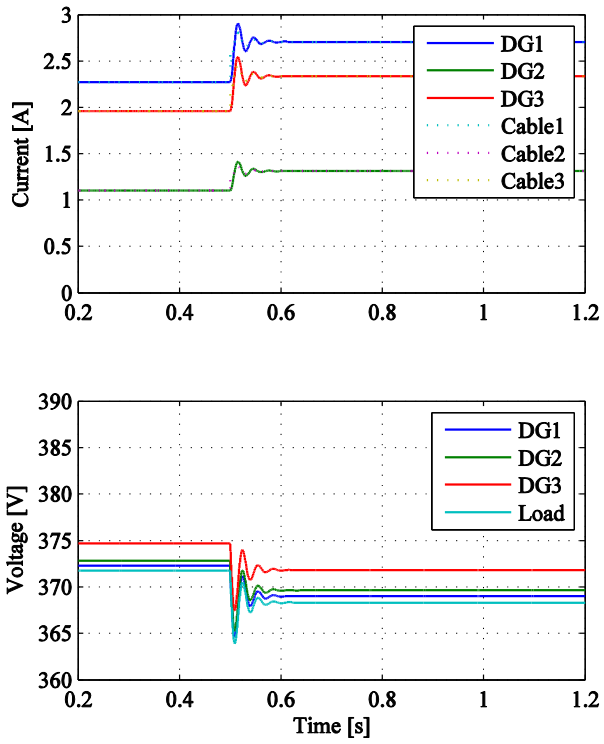


Figure 3.10 Time simulation results of CM under CCL step

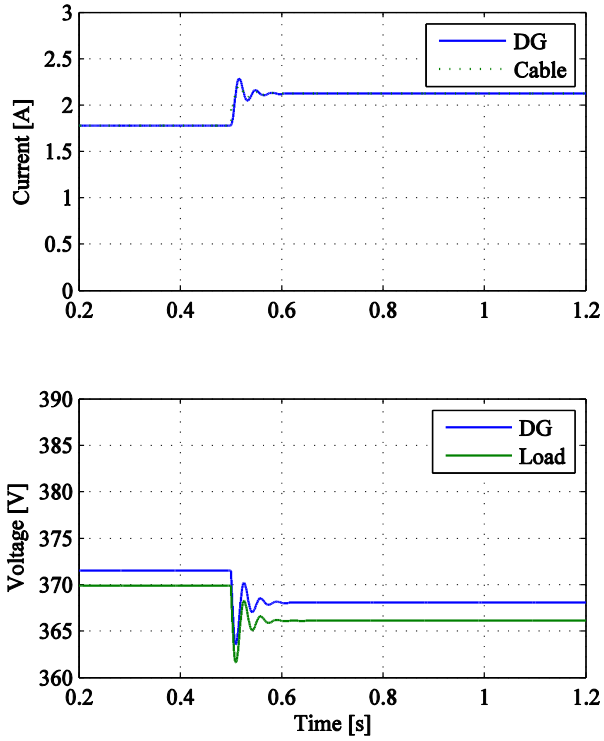


Figure 3.11 Time simulation results of R4M under CCL step

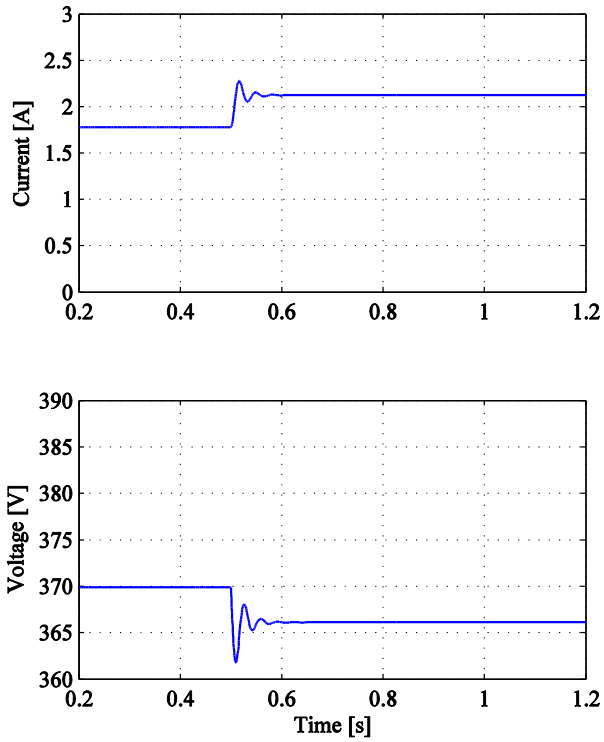


Figure 3.12 Time simulation results of R2M under CCL step

3.3 Stability analysis

3.3.1 Stability analysis methods

The stability of the DC microgrid can be analyzed by either the location of the eigenvalues of the state matrix for the linearized model or an estimation of the asymptotically stability domain (domain of attraction) using Lyapunov function for the original nonlinear model, or time simulation for the numerically implemented model.

For a Linear Time-Invariant (LTI) system, the global asymptotical stability can be analyzed by the eigenvalues of system state matrix. If all the eigenvalues have negative real parts, the system is asymptotically stable. However this stability test requires the linearization of the nonlinearities (e.g., CPLs). Therefore the stability analysis is only able to ensure the asymptotical stability nearby the equilibrium point. The stable operation domain of the system requires the direct examination of the original nonlinear model, using the large-signal stability analysis methods based on the Lyapunov direct method (also referred as the second Lyapunov theorem).

The core issue to apply the second Lyapunov theorem is the select of the Lyapunov function, which can be constructed by many different methods. Takagi-Sugeno (TS) multi-modeling method can be used to determine the largest estimation of the domain of attraction for nonlinear electric systems [129]. In this method, a set of linear local models are deduced from the nonlinear system and interconnected by the nonlinear activation functions verifying the property of convex sum. It uses '*if-then*' rules to represent the input-output linear local relationships. Consider k distinct nonlinearities in the nonlinear model. Assume each nonlinearity can admit a maximum and a minimum in the studied domain. Then, replacing it by these two extremes, the nonlinear model can be represented by 2^k local models, each one under the following LTI form [129]:

$$\begin{cases} \dfrac{d}{dt}x(t) = A_i x(t) + B_i u(t) \\ y(t) = H_i x(t) \end{cases} \tag{3.44}$$

where A_i, B_i and H_i are constant matrices. To achieve the nonlinear model, a normalized weight $w_i(x)$ is attributed to each local linear model, and then the following convex sum represents the nonlinear model [129]:

$$\begin{cases} \dfrac{d}{dt}x(t) = \sum_{i=1}^{k} w_i(x)(A_i x(t) + B_i u(t)) \\ y(t) = \sum_{i=1}^{k} w_i(x) H_i x(t) \end{cases} \tag{3.45}$$

The local models can be formed as autonomous models using coordination transformation to move the equilibrium point to origin. Then the nonlinear model is stable if:

$$\begin{cases} M = M^T > 0 \\ A_i^T M + M A_i < 0, \forall i = 1, \dots, 2^k \end{cases} \tag{3.46}$$

This means the existence of a common positive definite matrix *M* satisfying the Lyapunov inequality for all the 2^k local models is sufficient, but not necessary, to prove the stability of the nonlinear model. In this case, The Lyapunov function is:

$$F(s) = x^T M x \tag{3.47}$$

Then the domain in which all the 2^k+1 inequalities in (3.46) hold is an estimation of the domain of attraction.

In the examined DC microgrid, only the CPL introduces the nonlinearity. Consider the R2M for a DC microgrid with only CPL, the nonlinear system model can be expressed by:

$$\begin{cases} \frac{d}{dt}\bar{I} = -\frac{\bar{R}_s}{\bar{L}_d}\bar{I} - \frac{1}{\bar{L}_d}V_L + \frac{1}{\bar{L}_d}V_N \\ \frac{d}{dt}V_L = \frac{1}{\bar{C}_{dc}}\bar{I} - \frac{1}{\bar{C}_{dc}}\frac{P_{CPL}}{V_L} \end{cases} \tag{3.48}$$

To analyze the large-signal stability of this system around its equilibrium point (I_e, V_e), we introduce $x_I = \bar{I} - I_e$ and $x_V = V_L - V_e$ to move the equilibrium point to the origin. I_e and V_e are respectively the source current and the DC-bus voltage of the microgrid at the equilibrium point for a given load power P_{CPL}. Then, the model (3.48) can be rewritten as follows:

$$\frac{d}{dt}\begin{bmatrix} x_I \\ x_V \end{bmatrix} = \begin{bmatrix} -\frac{\bar{R}_s}{\bar{L}_d} & -\frac{1}{\bar{L}_d} \\ \frac{1}{\bar{C}_{dc}} & f(x_V) \end{bmatrix}\begin{bmatrix} x_I \\ x_V \end{bmatrix} \tag{3.49}$$

where the nonlinearity element (i.e., the last diagonal element of the above matrix) is given by:

$$f(x_V) = \frac{P_{CPL}}{\bar{C}_{dc} V_e (x_V + V_e)} \tag{3.50}$$

Then, the boundary of the estimated domain of attraction can be obtained by solving (3.46) as described in [129].

Time simulation can be performed to confirm the above results on the stability. Moreover, they can be easily confirmed by experimental tests. However, the time simulation can only test a few number of points, the test of the overall domain requires extensive simulation time.

3.3.2 Application to DC microgrids

To verify the effectiveness of these reduced order methods, both small-signal and large-signal stability tests are applied to analyze the models CM, R4M and R2M. A typical DC microgrid with

three DGs are considered to conduct the comparisons. The first DG's time constant can vary between 0.01 s and 1 s while the others' are kept constant at 0.01 s. The capacitance ratio is selected equal to 10% of the basic value (i.e., 145.8 μF/kW), and the other parameters are listed in Table 3.1.

For the small-signal stability analysis, the eigenvalue traces of the state matrices in different models are presented in Figure 3.13. According to the traces of R4M and R2M, the system becomes unstable when the time constant of DG1 is greater than 0.33 s, while the eigenvalues of CM still stay in the left-hand half plane for all values of τ_1 from 0.01 s to 1 s. Therefore, the use of reduced-order models makes the small-signal stability analysis of the microgrid very conservative.

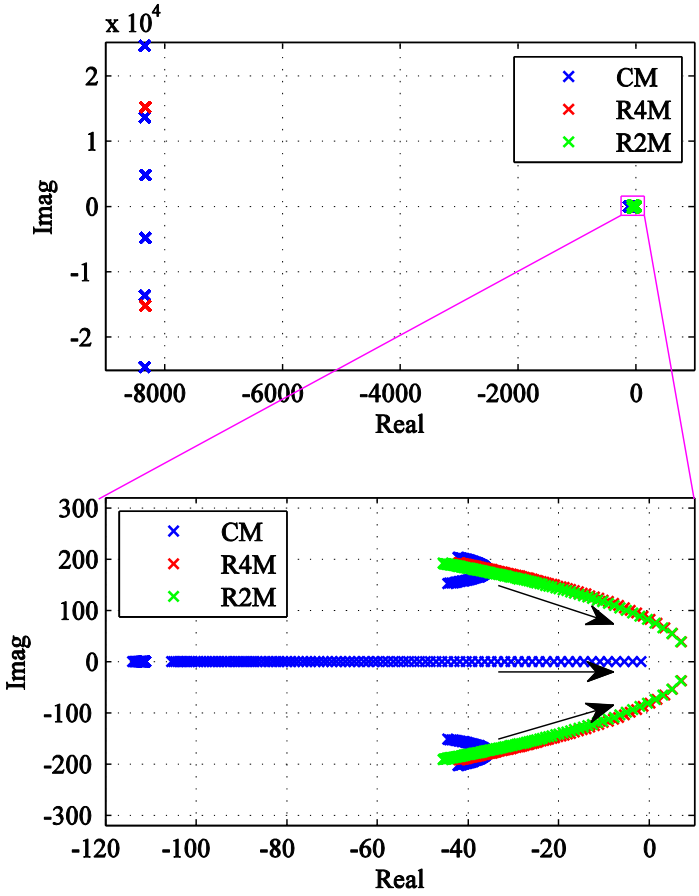


Figure 3.13 Eigenvalue traces of the state matrices in different models with τ_1 varies from 0.01 s to 1 s.

The large-signal stability analysis allows to estimate the domain of attraction around the equilibrium point. The results are given in Figure 3.14, using the TS multi-modeling method. It can be seen that when τ_1 goes from 0.01 s to 1 s, the estimated domain of attraction shrinks quickly in the reduced-order models while it keeps relatively constant with the CM. The adoption of R4M and R2M may lead to over conservative results (i.e., too large bus capacitor). Once again, it can be concluded that

these reduced-order models can properly represent the original system only if the assumption on the similarity of the time constants holds.

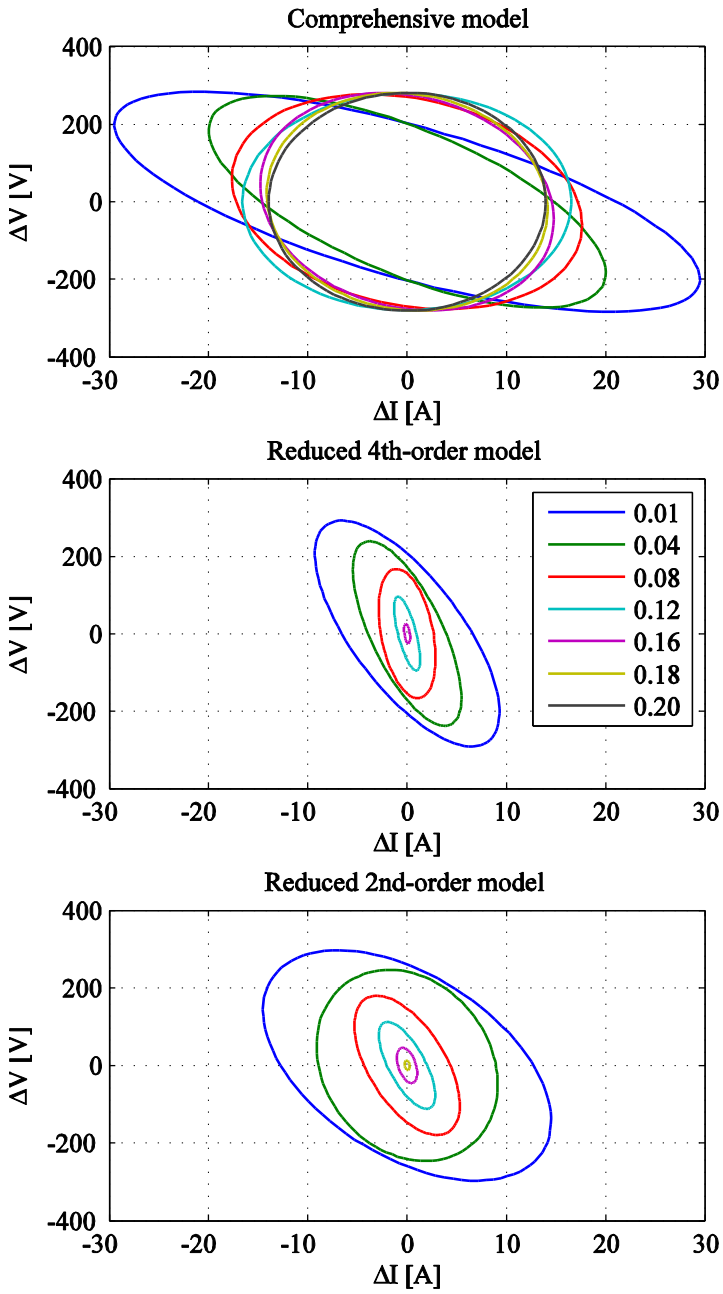


Figure 3.14 Estimated domains of attraction in different models with τ_1 varies from 0.01 *s* to 0.2 *s*.

To further demonstrate the differences of the three models with different time scales, a simulation using MATLAB is performed. The time constant of DG1 is 20 times of the others' (i.e., 0.2 *s*). A CPL step steps from 1 kW to 2 kW is applied at t=1.0s. The time domain responses of the three

models are shown in Figure 3.15, Figure 3.16, and Figure 3.17. Although the system can operate stably with a 1kW CPL, only CM presents stable operation phenomenon while the others are not stable.

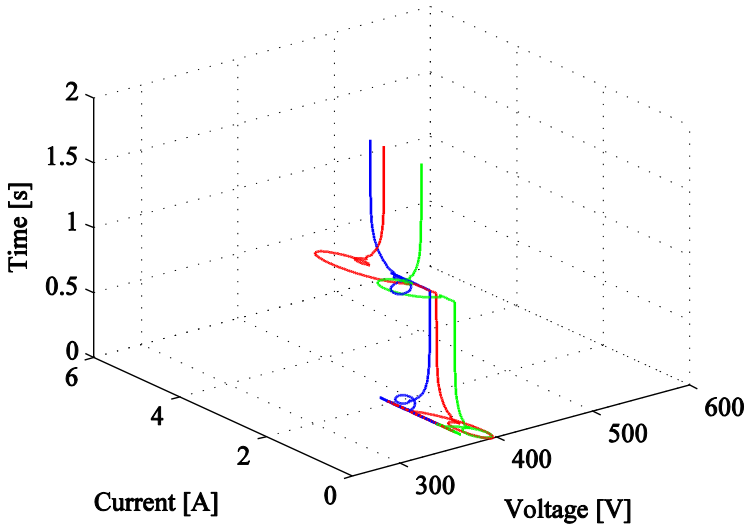


Figure 3.15 Time response of load steps by CM in current-voltage-time space

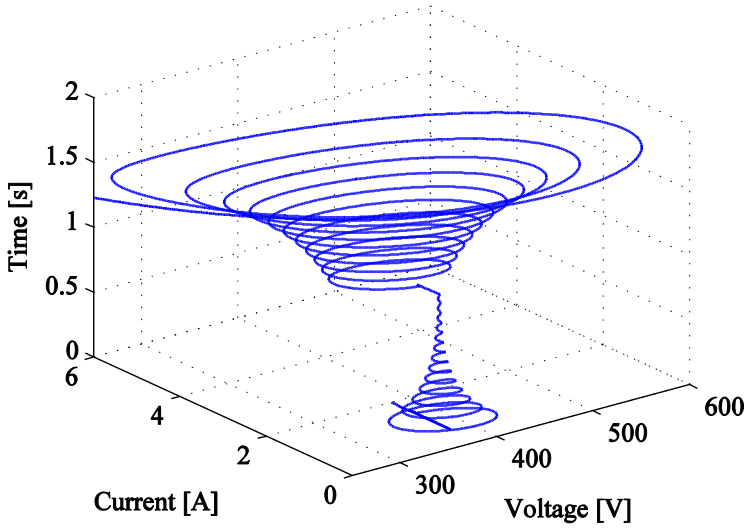


Figure 3.16 Time response of load steps by R4M in current-voltage-time space

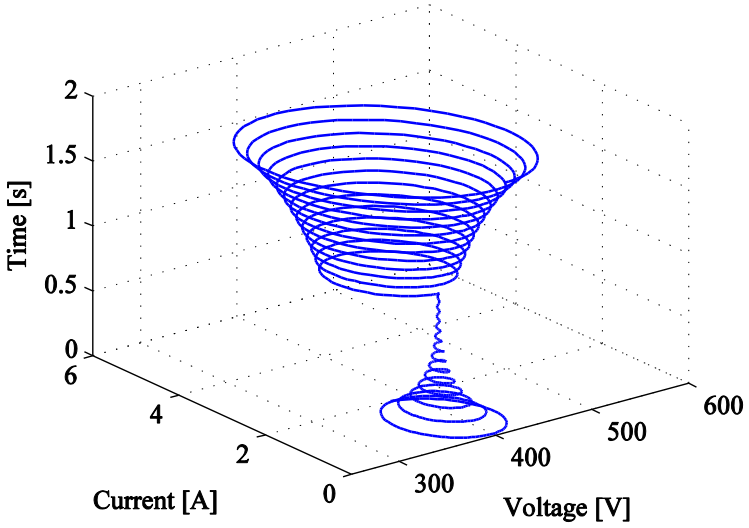


Figure 3.17 Time response of load steps by R2M in current-voltage-time space

In conclusion, these studies show that the DG's time constant affects significantly the performances of R4M and R2M; i.e., R4M and R2M cannot represent the original system properly when the time constants are largely different.

3.4 Proposed new multi-scale model

3.4.1 Reduced-order multi-scale model

The previous analyses show that the time scale have to be considered in the modeling of the multi-time scale DC microgrid. Although CM contains naturally the time scale information of every DG, it is rather complex and the order increases quickly with the number of DGs. Thus CM is not a good candidate for analytical studies. The comparison of R4M and R2M discovers that R4M has no significant improvement compared to R2M. Therefore, DGs with similar time constant can be grouped together to form an equivalent DG like in R2M, and then the equivalent DGs are combined to construct a reduced-order multi-scale model (RMM). The order of RMM is the function of the number of groups instead of number of the DGs. It not only reduces the complexity of the model but also keeps the major time scale information. Consider a DC microgrid with n DGs, and the DGs are divided into m groups according to their time scales. The time domain model in state space form can then be expressed as:

$$\frac{d}{dt}\begin{bmatrix}\bar{I}' \\ \bar{I}'' \\ \vdots \\ \bar{I}^m \\ V_L\end{bmatrix}=\begin{bmatrix}-\frac{\bar{R}_s'}{\bar{L}_d'} & 0 & \dots & 0 & -\frac{1}{\bar{L}_d'} \\ 0 & -\frac{\bar{R}_s''}{\bar{L}_d''} & \dots & 0 & -\frac{1}{\bar{L}_d''} \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ 0 & 0 & 0 & -\frac{\bar{R}_s^m}{\bar{L}_d^m} & -\frac{1}{\bar{L}_d^m} \\ \frac{1}{\bar{C}_{dc}} & \frac{1}{\bar{C}_{dc}} & \dots & \frac{1}{\bar{C}_{dc}} & -\frac{1}{\bar{C}_{dc}\bar{R}_L}\end{bmatrix}\begin{bmatrix}\bar{I}' \\ \bar{I}'' \\ \vdots \\ \bar{I}^m \\ V_L\end{bmatrix}+\begin{bmatrix}\frac{1}{\bar{L}_d'} & 0 \\ \frac{1}{\bar{L}_d''} & 0 \\ \vdots & \vdots \\ \frac{1}{\bar{L}_d^m} & 0 \\ 0 & -\frac{1}{\bar{C}_{dc}}\end{bmatrix}\begin{bmatrix}V_N \\ \bar{I}_{CC}\end{bmatrix} \tag{3.51}$$

where m is the number of time constant groups, and the order of RMM is (m+1); $\bar{I}', \bar{I}'', \dots, \bar{I}^m$ denote the currents of the equivalent DG for different groups; $\bar{R}_s', \bar{R}_s'', \dots, \bar{R}_s^m$ denote the source resistances of the equivalent DG for different groups; $\bar{L}_d', \bar{L}_d'', \dots, \bar{L}_d^m$ denote the virtual inductances of the equivalent DG for different groups. These parameters of the equivalent DGs are calculated by:

$$\begin{cases}\bar{R}_s^x = \dfrac{1}{k_x}\sum_{k_x+1}^{k_{x-1}+k_x}(R_{dj}+R_{cj}) \\ \bar{L}_s^x = \dfrac{1}{k_x}\sum_{k_{x-1}+1}^{k_{x-1}+k_x} L_{dj}\end{cases} \tag{3.52}$$

where $k_x, x = 1,2, \dots, m$ is the number of DGs in the xth group, and $k_0 = 0$.

Consider the previous example with three DGs, they are divided into two groups to form two equivalent DGs; i.e., the Equivalent Slow DG (DG1 with large time constant) and the Equivalent Fast DG (the other DGs with small time constant). The (m+1)-order multi-scale model becomes a 3rd-order model, which is given by:

$$\frac{d}{dt}\begin{bmatrix}\bar{I}' \\ \bar{I}'' \\ V_L\end{bmatrix}=\begin{bmatrix}-\frac{\bar{R}_s'}{\bar{L}_d'} & 0 & -\frac{1}{\bar{L}_d'} \\ 0 & -\frac{\bar{R}_s''}{\bar{L}_d''} & -\frac{1}{\bar{L}_d''} \\ \frac{1}{\bar{C}_{dc}} & \frac{1}{\bar{C}_{dc}} & -\frac{1}{\bar{C}_{dc}\bar{R}_L}\end{bmatrix}\begin{bmatrix}\bar{I}' \\ \bar{I}'' \\ V_L\end{bmatrix}+\begin{bmatrix}\frac{1}{\bar{L}_d'} & 0 \\ \frac{1}{\bar{L}_d''} & 0 \\ 0 & -\frac{1}{\bar{C}_{dc}}\end{bmatrix}\begin{bmatrix}V_N \\ \bar{I}_{CC}\end{bmatrix} \tag{3.53}$$

where $\bar{I}'$ and $\bar{I}''$ denote the equivalent slow and fast DGs' currents, respectively; $\bar{R}'_s$ and $\bar{R}''_s$ denote the equivalent slow and fast DGs' resistances; $\bar{L}'_d$ and $\bar{L}''_d$ denote the equivalent slow and fast DGs' virtual inductances. The corresponding equivalent parameters are:

$$\begin{cases} \bar{R}'_s = \dfrac{1}{p}\sum_1^p \left(R_{dj} + R_{cj}\right) \\ \bar{R}''_s = \dfrac{1}{n-p}\sum_{p+1}^n \left(R_{dj} + R_{cj}\right) \\ \bar{L}'_s = \dfrac{1}{p}\sum_1^p L_{dj} \\ \bar{L}''_s = \dfrac{1}{n-p}\sum_{p+1}^n L_{dj} \end{cases} \tag{3.54}$$

where the jth DG is slow DG when $j = 1,2 \ldots, p$, and fast DG when $j = p+1, \ldots, n$. As adopted in the previous example, the Equivalent Slow DG has the time constant 0.2 s, while the Equivalent Fast DG has the time constant 0.01 s.

3.4.2 Model analysis

A. Influence of bus capacitance

To verify the effectiveness of the proposed RMM, system stability is analysis with variable DC-bus capacitance ratio, in different models (CM, R4M, R2M, and RMM).

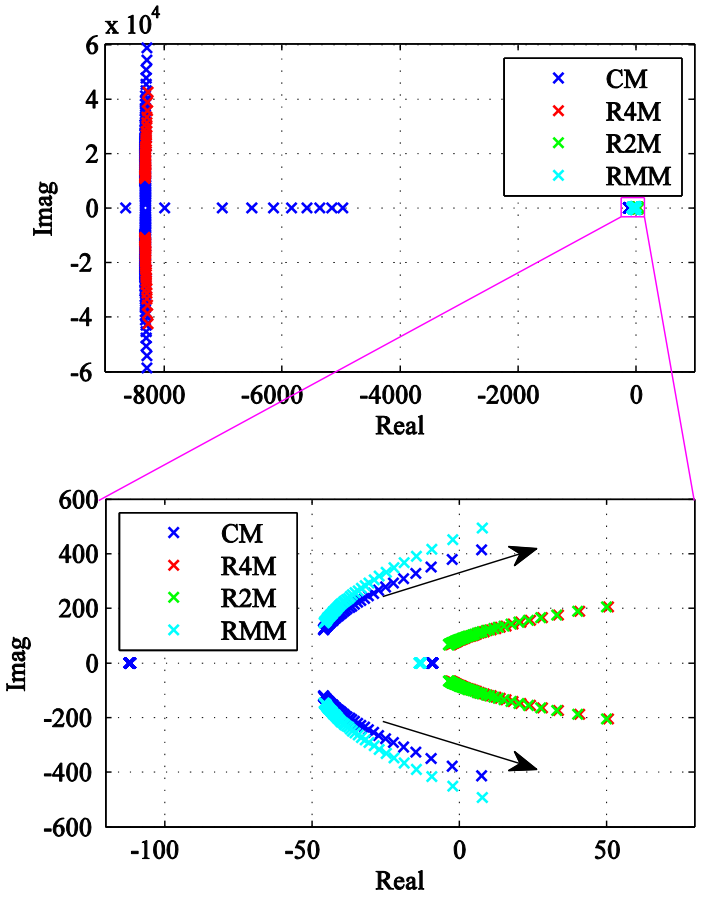


Figure 3.18 Eigenvalues traces of the state matrices in the four models, with the capacitance ratio varies from 232 μF/kW to 23.2 μF/kW.

The capacitance ratio decreases from 232 μF/kW (i.e., 20% of the basic capacitance ratio) with the step 4.64 μF/kW, until 2.32 μF/kW. The eigenvalues traces of in different models are shown in Figure 3.18. Although the R4M and R2M show similar tendency with the CM, the eigenvalues in R4M and R2M start to enter into the right-hand plant (instability region) much earlier than that of CM. The results of R4M and R2M are pretty conservative than CM, but the proposed RMM can give coincident results compared to CM. That's because R4M and R2M are based on the assumption of similar time scale, and they would become too conservative when the time constants of DGs are largely different.

The estimated domains of attraction with variable capacitance ratio projected on the surface of the current of DG1 (current of the Equivalent Slow DG) and load voltage are presented in Figure 3.19. The results of RMM can match that of CM properly, showing the validity of the RMM used for the analysis of system stability.

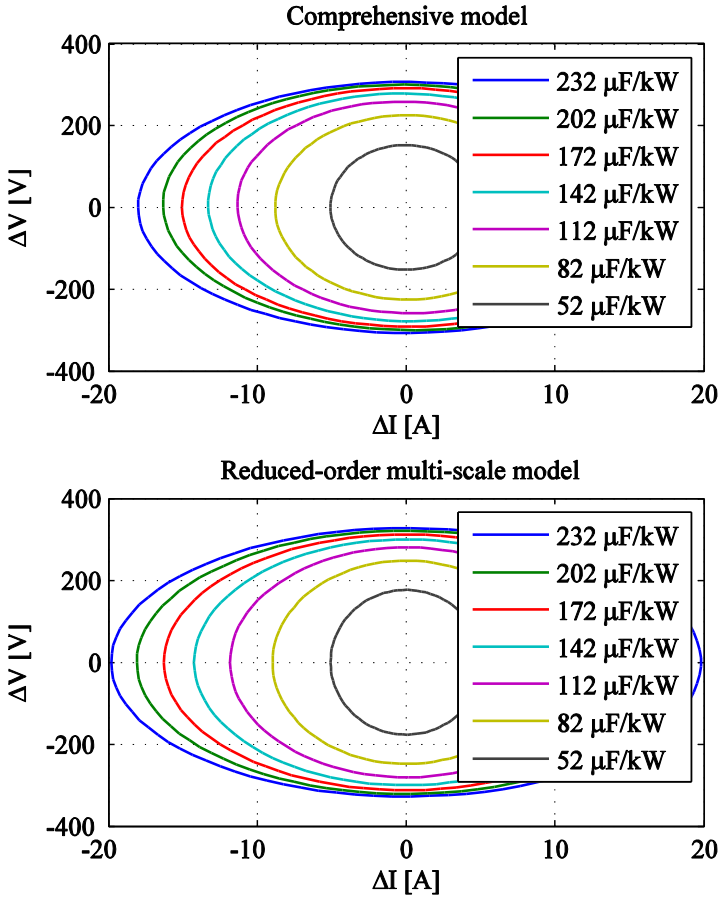


Figure 3.19 Estimated domains of attraction for CM and RMM, with the capacitance ratio varies from 232 μF/kW to 23.2 μF/kW.

B. Influence of the time constant

The influence of variable time constant in the RMM is examined and compared with CM. The eigenvalue traces in CM and RMM are shown in Figure 3.20. The time constant of DG1 increases from 0.01*s* to 1 *s*, while the others' are kept constant. It can be seen that the RMM can present similar eigenvalue trace patterns as that of CM for the eigenvalues near the origin. The result of RMM is more precise than that of R4M and R2M presented in Figure 3.13.

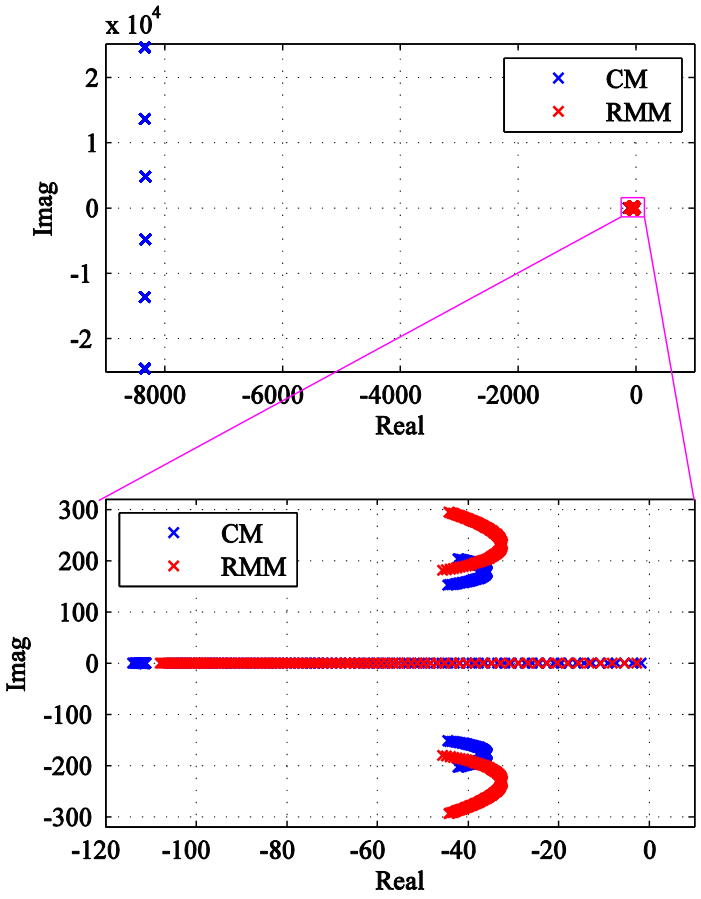


Figure 3.20 Eigenvalue traces of the state matrices in CM and RMM with τ_1 varies from 0.01 *s* to 1 *s*.

The effect of variable time scale on the estimated domain of attraction in RMM is also analyzed and the results are presented in Figure 3.21. The domain of attraction shrinks gradually, with the increase of the time constant of DG1. The RMM can give similar results as that of CM, this confirms the effectiveness of the proposed RMM in the analysis of large-signal stability.

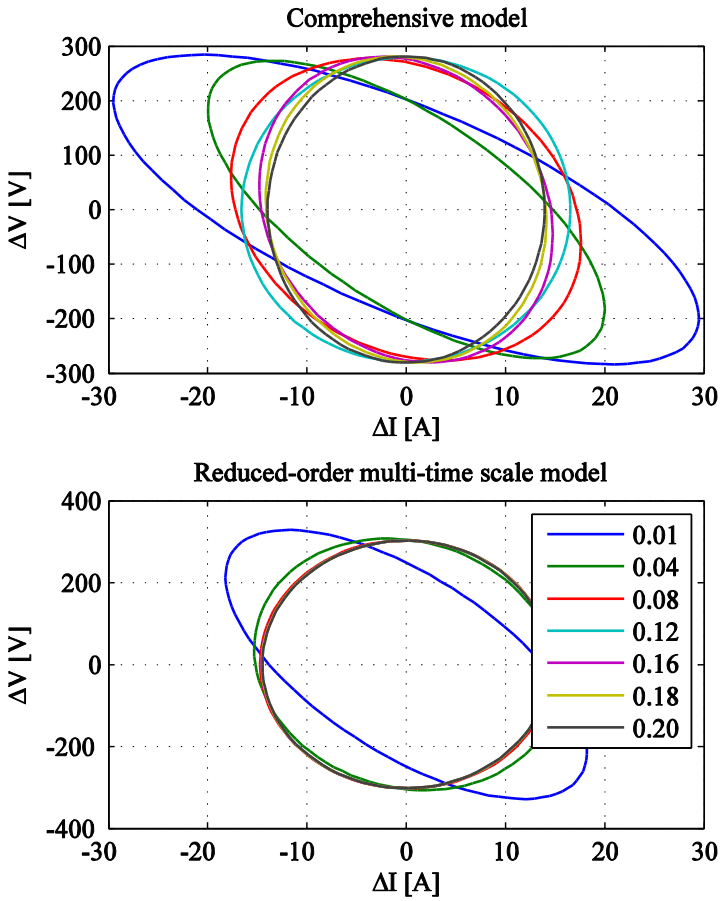


Figure 3.21 Estimated domains of attraction for CM and RMM with τ_1 varies from 0.01 *s* to 1 *s*.

C. Time domain simulations

Time simulations are also conducted to test the dynamic performance of the proposed RMM. The CPL steps from 1 kW to 2 kW at t=1.0s and the results of CM and RMM are shown in Figure 3.22 and Figure 3.23. The Equivalent Slow DG (ESDG) in the RMM supply only basic current without high frequency part, while the Equivalent Fast DG (EFDG) can track the load step to supply high frequency current during the transient like the results presented in CM.

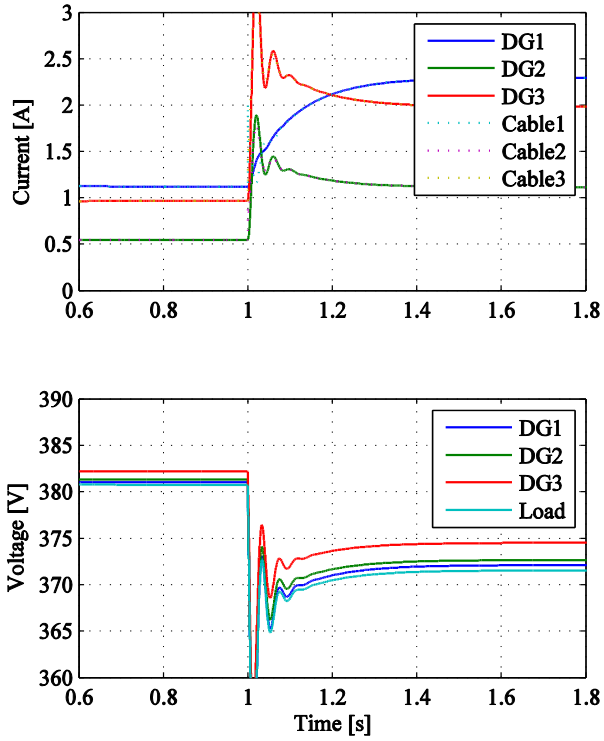


Figure 3.22 Time simulation results in CM under CPL step

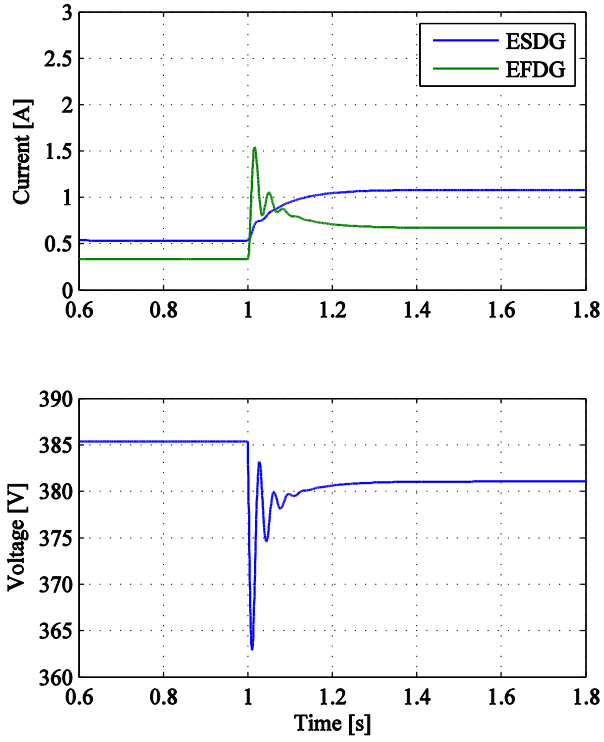


Figure 3.23 Time simulation results in RMM under CPL step

3.4.3 Primary discussion about the grouping of DGs

The proposed RMM can effectively reduce the order of the model, as well as keep the major time scale information in the DC microgrid model. However, the new problem is how to group the DGs together. Consider the previous DC microgrid with three DGs divided into two groups, a slow DG (DG1) with time constant 0.1 *s* and two fast DGs (DG2 and DG3) with time constant 0.01 *s*. Now, consider that the time constant of DG2 τ_2 varies from 0.01 *s* to 0.1 *s*. Although DG2's time constant changes, we keep it always grouped into the fast DGs for analysis. An aggressive capacitance ratio 80 μF/kW is selected. The operation voltage limits in large-signal stability tests for CM and RMM are presented in Figure 3.24. In this figure, ΔV limit is the voltage operation boundary around the equilibrium point; i.e., when the voltage limit reaches zero, any small disturbance changing the DC-bus voltage will make the system loss its stability. The error between CM and RMM increases quickly with the increase of τ_2. When it is over four times larger than the original time constant of the corresponding group, the voltage operation limit drops to almost zero. Therefore, an approximated threshold to keep DGs with similar time scale group is around three times. In real applications, the grouping of the DGs also need to consider the balance of accuracy and complexity.

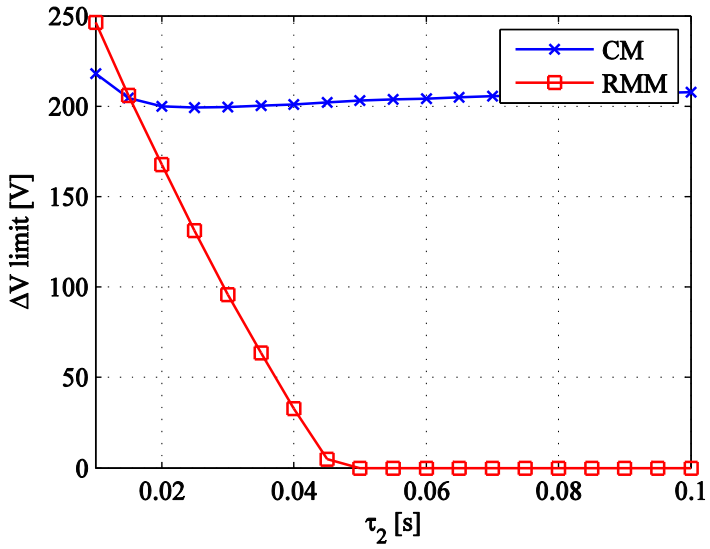


Figure 3.24 The effect of grouping with τ_2 varies from 0.01 *s* to 0.1 *s*.

3.5 Experimental verification

A laboratory scale test bench is built to verify the proposed RMM model, and to analyze the stable operation domain. Two DC power sources are used to represent the DGs and they are connected to the common DC-bus via boost type DC/DC converters. An active load is connected to the DC-bus to represent the CPL. Separate connecting cables are used to connect the DGs and the load. The DC-

bus voltage is selected to be 100 V, due to the limit of the hardware. The parameters of the DGs are listed in Table 3.2.

Table 3.2 The parameters of the laboratory scale DC microgrid test bench

	Power	Input voltage	Input current	Time const.
DG1	300 W	50 V	6 A	0.05 *s*
DG2	300 W	50 V	6 A	variable

The DC-bus capacitance can be calculated according to (3.11). Considering the smaller time constant 0.05 *s*, then the DG's required basic capacitance ratio is 105.25 mF/kW (i.e., 126.3 mF for the DC-bus capacitance). To verify the stability margin, a much aggressive DC-bus capacitor 2.93 mF is selected. The time constant of DG1 keeps constant to 0.05 *s*, while that of DG2 is variable. The eigenvalues traces of the state matrices in R2M and RMM with the time constant of DG2 varies from 0.05 *s* to 0.5 *s* are shown in Figure 3.25. The result of RMM indicates that the multi-scale system can be stable even when the time constant of DG2 is as high as 10 times of DG1's. While the R2M shows the system becomes unstable when DG1's time constant is about 5 times of DG2's. The multi-time scale DC microgrid with DG2's time constant 10 times of DG1's will be verified in experimental test, to verify the accuracy of RMM.

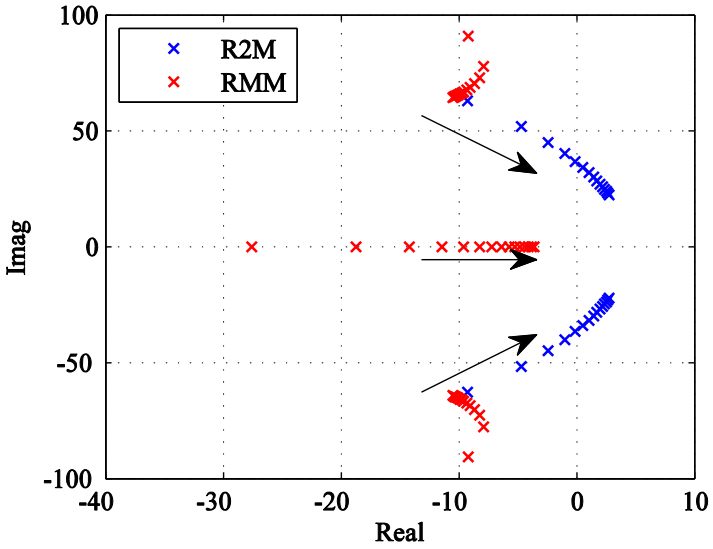


Figure 3.25 Eigenvalue traces of the state matrices in R2M and RMM with the time constant of DG2 increases from 0.05 *s* to 0.5 *s*.

To compare RMM and R2M from view of large-signal stability, two scenarios are considered: a single-time scale microgrid and a multi-time scale microgrid. In the former scenario the time constant of DG2 is the same as that of DG1 (i.e., 0.05 *s*); while in the latter one, the time constant of DG2 is 10 times that of DG1 (i.e., 0.5 *s* for DG2). The estimated domains of attraction in RMM and R2M for both the single-time scale system and the multi-time scale system are shown in Figure 3.26. Although the R2M gives identical domain as that of RMM in a single-time scale system, the results

of R2M in a multi-time scale system is too conservative in such a manner that no stable operation range is found. In contrast, the proposed RMM can give less conservative results with an estimated domain of attraction as shown in Figure 3.26. The comparison will be verified by experimental tests in the following part.

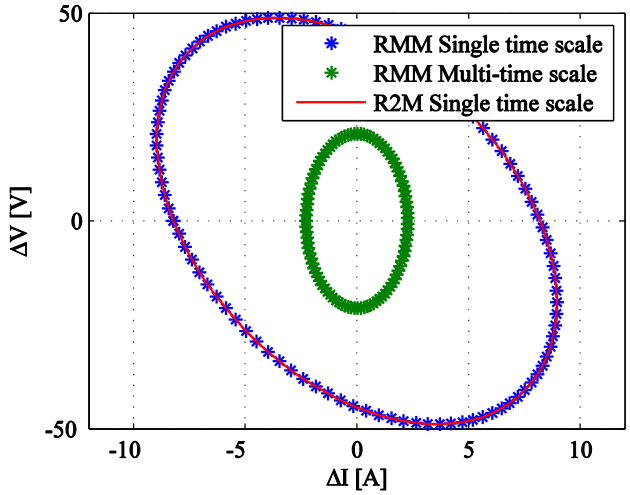


Figure 3.26 Estimated domains of attraction for RMM and R2M with variable time constant of DG2

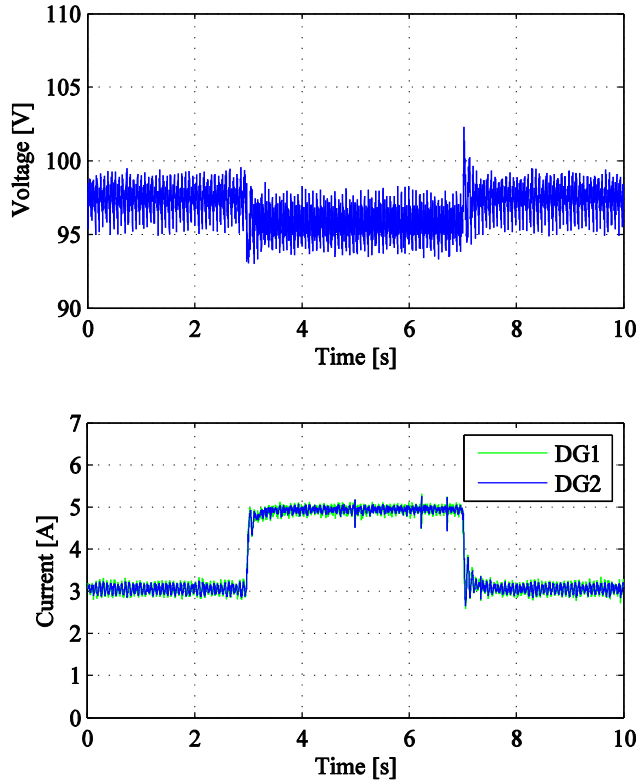


Figure 3.27 Experimental results of the DC microgrid with single time scale

Two experimental tests with single time scale and multi-time scale are conducted to verify the previous analysis for the proposed RMM model. The CPL steps from 300 W to 500 W at t=3s and step back to 300 W at t=7s. The voltage performance and load sharing are given by Figure 3.27, when single time scale is considered. The system is stable and DG1 and DG2 and share the load proportionally in steady-state and dynamic states. This verify the effectiveness of the analyses by R2M and RMM in the single time scale system.

The experimental results of the multi-scale system are shown in Figure 3.28, where the DG2's time constant is 10 times of DG1's. With the step of CPL, the system is still stable and the DG1 responds quickly to absorb the high frequency term, while DG2 shows a slow dynamic response. This result confirms that this operation point is in the domain of attraction and the result given by RMM is more accuracy than R2M. It should be noticed that, the analysis results of R2M doesn't consider this case as stable, and requires larger DC-bus capacitance.

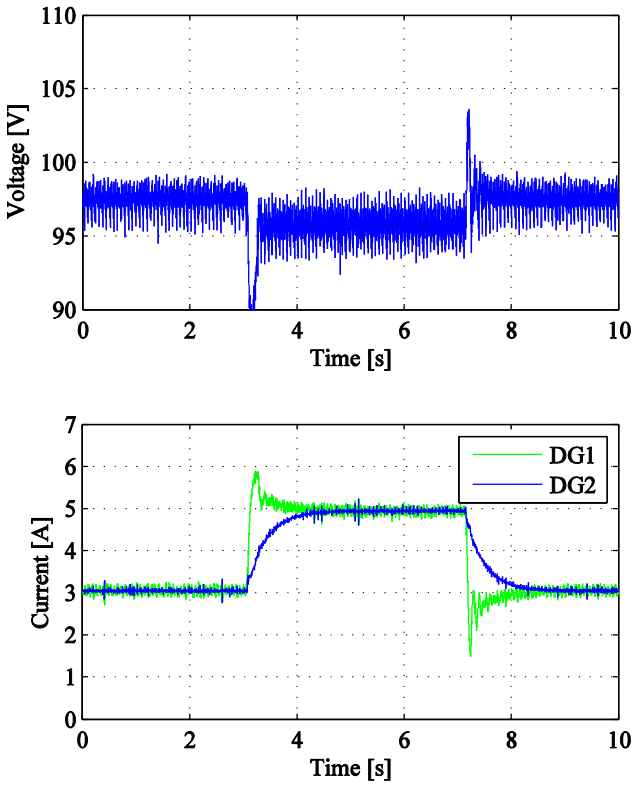


Figure 3.28 Experimental results of the DC microgrid with multi-time scale

3.6 Conclusion

This chapter discusses the modeling of multi-time scale DC microgrids. Several reduced order models are constructed using the average value to replace the distributed parameters. The influence

of time constant on the stability is analyzed using small-signal, large-signal stability tools in CM and several reduced order models. These traditional reduced order models cannot represent the system well in the multi-scale environment. The proposed multi-scale model RMM can significantly reduce the model complexity as well as keep major time scale information. Small-signal and large-signal stability tests of the proposed RMM are compared with those of the comprehensive model (CM) in MATLAB/Simulink environment, and also experimental tests in a laboratory scale DC microgrid. The simulation and experimental results have confirmed the accuracy of the proposed RMM.

Chapter 4 Implementation of Time-scale Droop Control Based on ADRC

The previous chapter studies the modeling and stability issues of multi-time scale DC microgrids. It has been demonstrated that the previously proposed reduced-order multi-time scale model (RMM) can significantly reduce model complexity as well as keep major time scale information, thus represent the original system with better accuracy. This chapter continues the topic about multi-time scale DC microgrids and discusses how to design a stable multi-time scale system with dedicate control method.

This chapter reviews the common three implementation methods using forward path low-pass filter, feedback low-pass filter and PI type voltage controller with an additional droop loop. These three methods are equivalent when the parameters are properly selected. A novel implementation method based on the Active Disturbance Rejection Control (ADRC) is proposed to reduce the dependency on precise DG models. The proposed method can explicitly adjust local voltage control bandwidth, which will affect the DG's time scale. A new parameterized reduced-order multi-scale model (N-RMM) is introduced and the general procedure to design a stable DC microgrid is also discussed. Finally, simulations in MATLAB/Simulink as well as experimental tests are carried out to verify the proposed method.

4.1 Time-scale droop control

4.1.1 Local control

As defined in the hierarchical structure, the three control layers of DC microgrids are: primary control (local control), secondary control and tertiary control [31]. The local control focus on the current and voltage control of the DG; i.e., the output voltage control as well as the load sharing. One popular method is the usage of droop control, which controls the output current/power according to the bus voltage level (load condition) and the load is shared automatically among the DGs according to their output impendences.

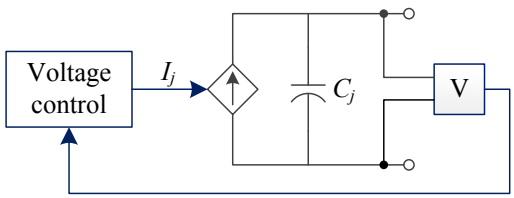
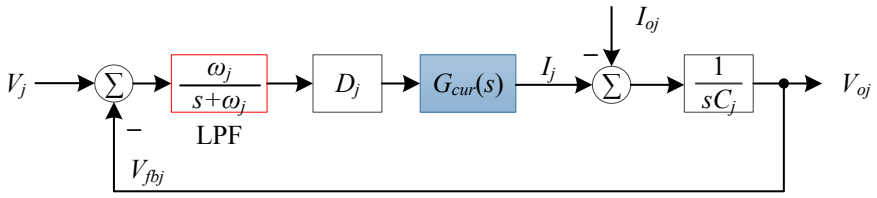


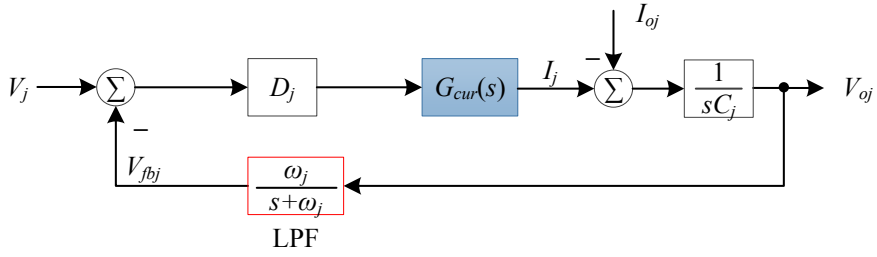
Figure 4.1 The Norton equivalent circuit of the DG with local control

The local control is usually implemented by a cascaded control structure with inner current control loop and outer voltage control loop. Droop control can be combined with voltage control or realized in an additional droop loop. The inner current loop regulates the power converter interfaced DG to realize a first-order control feature. The method like peak-current modulation can be adopted to obtain a high dynamic response. The equivalent circuit of the DG under local control in Norton form is shown in Figure 4.1. The inner current control loop can be modeled as a perfect controllable current source I_j, when the control bandwidth is large enough and out of consideration. The local output voltage is sensed on the output capacitor C_j and fed back to the voltage controller. Then the voltage controller uses the error between the voltage reference and the feedback signal to generate current reference.

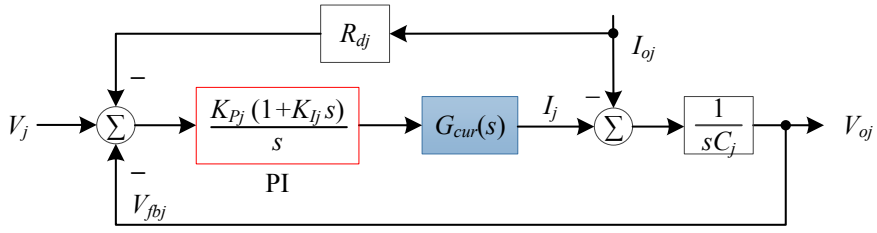
4.1.2 Droop control with time scale



(a) with forward path low-pass filter



(b) with feedback low-pass filter



(c) PI control with an additional droop loop

Figure 4.2 Different implementations of droop control with time scale

In addition to the power scale droop control concerned in the traditional droop control, the dynamics of the DG can be introduced as another freedom in the local control, referred as the time-scale droop control [86]. As discussed in section 3.1.1, it can be realized by a forward path LPF, or a feedback LPF adding to the classic droop control structure, or a PI type voltage control with an additional

droop loop. A more detail analysis about the three implementations will be addressed in this section. They are shown in Figure 3.2, in which $G_{cur}(s)$ represents the transfer function of inner current control loop. The transfer function of the current loop can be approximated to be unit $G_{cur}(s) = 1$ because the current control bandwidth is usually much higher than the others'. The subscript j indicates the jth DG; ω_j denotes the cutoff frequency of the applied forward or feedback LPF; C_j denotes the output capacitance of the jth DG; V_j denotes the nominal voltage reference of the jth DG; I_{oj} is the current injected by the jth DG into the common DC-bus; and V_{oj} is the local output voltage of the jth DG.

The droop constant D_j or virtual droop resistance R_{dj} is determined by the DC-bus voltage performance requirement. They can be calculated by:

$$D_j = \frac{1}{R_{dj}} = \frac{I_{Nj}}{\delta(1-\delta)V_{Nj}} \tag{4.1}$$

where I_{Nj}, V_{Nj} are the rated output current and voltage of the jth DG, respectively; δ is the DC-bus voltage tolerance in percentage. Higher voltage performance requirement leads to larger droop constant but smaller droop resistance.

Let's consider at first the implementation with a forward path LPF, as shown in Figure 3.2a. Assume the current control loop transfer function $G_{cur}(s) = 1$, then the input-to-output voltage closed-loop transfer function can be expressed by:

$$G_{c1}(s) = \frac{D_j\omega_j}{C_j s^2 + C_j\omega_j s + D_j\omega_j} \tag{4.2}$$

Similarly, for the second implementation with LPF in the feedback path, as shown in Figure 3.2b, the input-to-output voltage closed-loop transfer function is given by:

$$G_{c2}(s) = \frac{D_j\omega_j}{C_j s^2 + C_j\omega_j s + D_j\omega_j} \tag{4.3}$$

It can be seen that the closed-loop transfer functions of the first two implementations are the same, thus these two implementations are equivalent.

In the third implementation, a PI type voltage control and an additional droop loop are adopted as shown in Figure 3.2c. In this scheme, the bandwidth of the voltage control is determined by the PI controller not the droop loop. Thus the influence of the droop loop on the analysis of the voltage control bandwidth can be neglected. The input-to-output voltage closed-loop transfer function can then be given by (4.4) without consideration of the droop loop.

$$G_{c3}(s) = \frac{K_{Pj}K_{Ij}s + K_{Pj}}{C_j s^2 + K_{Pj}K_{Ij}s + K_{Pj}} \tag{4.4}$$

where K_{Pj} is the proportional gain; and K_{Ij} is the integral gain. In order to achieve equivalent dynamics as the other two implementation methods presented in (4.2) and (4.3), the gains of the PI controller need to satisfy:

$$\begin{cases} K_{Pj} = D_j\omega_j \\ K_{Ij} = \dfrac{C_j}{D_j} \end{cases} \tag{4.5}$$

From (4.2), (4.3), (4.4) and (4.5), the common characteristic polynomial of the voltage closed-loop transfer function for the three implementations can be deduced:

$$p(s) = s^2 + \omega_j s + \frac{D_j\omega_j}{C_j} \tag{4.6}$$

Given the standard form of the 2nd-order characteristic polynomial as:

$$p(s) = s^2 + 2\zeta_{Nj}\omega_{Nj}s + \omega_{Nj}^2 \tag{4.7}$$

where ζ_{Nj} is the damping factor of the voltage control loop; and ω_{Nj} is the natural frequency. When compare (4.7) with (4.6), the voltage loop parameters can be calculated by:

$$\begin{cases} \zeta_{Nj} = \dfrac{1}{2}\sqrt{\dfrac{C_j\omega_j}{D_j}} \\ \omega_{Nj} = \sqrt{\dfrac{D_j\omega_j}{C_j}} \end{cases} \tag{4.8}$$

It can be seen from (4.8) that the damping factor and the natural frequency depend on the selection of droop constant, output capacitance and the LPF's cutoff frequency.

4.2 Time-scale droop control based on ADRC

The aforementioned three implementation methods are all based on the precise description of DG, and the assumption of ideal current control loop. When the precise model of DGs cannot be obtained or the performance of the current control is not ideal, the design of the time-scale droop control may encounter some problems. A control method which is not sensitive to the error of the system model can be useful.

Disturbance rejection technique is kind of a control concept largely different from the principle of PID control. In this scheme, the system is modeled as an input term and an input disturbance which represents any differences between the model and actual system. The basic principle of disturbance

rejection control is to estimate the disturbance real-time and cancel it in the forward path, instead of using the error-based feedback in PID control.

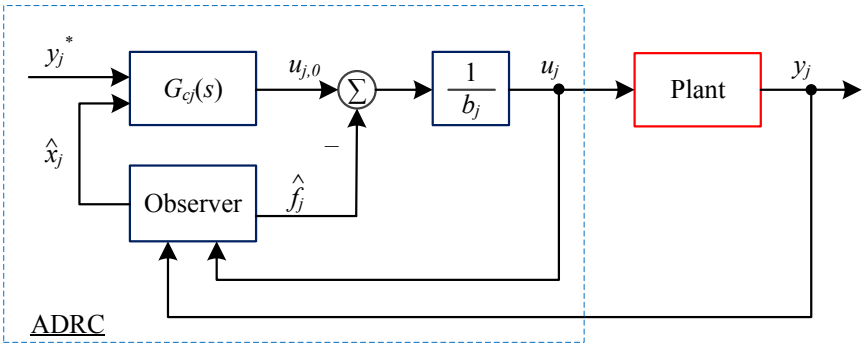


Figure 4.3 The scheme of the Active Disturbance Rejection Control

The Active Disturbance Rejection Control (ADRC) allows the simplest possible model ($1/s^n$) to be used in designing the input disturbance observer [134], [135]. As shown in Figure 4.3, the plant is the DG under current control. It consists of two main parts: the linear extended states observer (LESO) and the controller $G_{cj}(s)$. The advantage of ADRC is that it is robust and it doesn't require precise plant model. ADRC can tune explicitly the bandwidths of state observer and controller, by using the parameterization and tuning method proposed in [136].

4.2.1 Construction of ADRC

In local voltage control of the *j*th DG, the DG and its inner control loops are viewed as the plant for the voltage control. To adopt ADRC, the plant can be rearranged as the sum of the input term and the total disturbance f_j:

$$y_j^{(p)} = f_j + b_j u_j \tag{4.9}$$

where p denotes the order of the plant which depends on the inner current loop and the dynamics of the DG; f_j denotes the total disturbance; b_j is the direct input gain or an estimation of the direct input gain; u_j, y_j denote the input and output vectors of the concerned plant, respectively.

Let the extended state variables $x_j = \left[x_{j,1}, x_{j,2} \ldots x_{j,p}, x_{j,p+1}\right]^T = \left[y_j, \dot{y}_j, \ldots y_j^{(p-1)}, f_j\right]^T$, in which the total disturbance f_j is added as an extended state. Assume f_j is differentiable and $h_j = \dot{f}_j$ is bounded. Then the augmented state-space form of the plant can be expressed by:

$$\begin{cases} \dfrac{d}{dt}x_j = Ax_j + Bu_j + Eh_j \\ y_j = Cx_j \end{cases} \tag{4.10}$$

where

$$A = \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \cdots & \cdots & \cdots & \ddots & \vdots \\ 0 & 0 & 0 & \cdots & 1 \\ 0 & 0 & 0 & \cdots & 0 \end{bmatrix}_{(p+1)\times(p+1)}$$

$$B = [0 \quad 0 \quad \cdots \quad b_j \quad 0]^T_{(p+1)\times 1}$$

$$E = [0 \quad 0 \quad \cdots \quad 0 \quad 1]^T_{(p+1)\times 1}$$

$$C = [1 \quad 0 \quad \cdots \quad 0 \quad 0]_{1\times(p+1)}$$

A linear extended state observer (LESO) [137] can be then designed as (4.11) to estimate the states of the plant described in (4.10).

$$\begin{cases} \frac{d}{dt}\hat{x}_j = A\hat{x}_j + Bu_j + L_j\left(y_j - \hat{y}_j\right) \\ \hat{y}_j = C\hat{x}_j \end{cases} \tag{4.11}$$

where $\hat{x}_j$ is the estimation of the state variable and $\hat{y}_j$ is the estimation of the plant output. The observer gains L_j can be chosen as:

$$L_j^T = [\alpha_{j,1} \quad \alpha_{j,2} \quad \cdots \quad \alpha_{j,p+1}]^T$$

The elements $\alpha_{j,k}, k = 1,2,\dots,(p+1)$ need to be chosen such that the characteristic polynomial is Hurwitz, to ensure the stability of the observer. For simplicity, $\alpha_{j,k}$ can be selected to satisfy [138], [139]:

$$\lambda_{oj}(s) = s^{p+1} + \alpha_{j,1}s^p + \cdots + \alpha_{j,p}s + \alpha_{j,p+1} = \left(s + \omega_{oj}\right)^{p+1} \tag{4.12}$$

where

$$\alpha_{j,k} = \frac{(p+1)!}{k!\,(p+1-k)!}\omega_{oj}^k, k = 1,2,\dots,p+1.$$

where $\omega_{oj} > 0$ denotes the bandwidth of the observer. This selection method leads to all the roots of the characteristic polynomial of the observer are placed at $-\omega_{oj}$. Thus ω_{oj} becomes the only tuning parameter of this state observer [138], [139].

When the states of the system are closely tracked by a well-tuned LESO, the control law to cancel the disturbance real-time can be defined as [138]:

$$u_j = \frac{u_{j,0} - \hat{f}_j}{b_j} \tag{4.13}$$

Then the plant of the voltage control for the jth DG described by (4.9) can be simplified to be a unit gain cascaded integrator:

$$y_j^{(p)} \approx u_{j,0} \tag{4.14}$$

For this system, a simple 2-Degree of Freedom (DOF) technique can be adopted [139], given by:

$$u_j = \beta_{j,1}\left(y_j^* - \hat{x}_{j,1}\right) - \beta_{j,2}\hat{x}_{j,2} - \cdots - \beta_{j,p}\hat{x}_{j,p} \tag{4.15}$$

where y_j^* is the desired trajectory. Again, the controller gains are selected such that the closed-loop characteristic polynomial is Hurwitz. In addition the entire controller poles can be placed at $-\omega_{cj}$ to further reduce the tuning parameters. Thus the closed-loop characteristic polynomial becomes:

$$\lambda_{cj}(s) = s^p + \beta_{j,p}s^{p-1} + \cdots + \beta_{j,1} = \left(s + \omega_{cj}\right)^p \tag{4.16}$$

where

$$\beta_{j,k} = \frac{p!}{k!\,(p+1-k)!}\omega_{cj}^{p+1-k}, j = 1,2,\ldots,p.$$

This makes $\omega_{j,c}$ to be the bandwidth of the controller, as well as the only parameter of the controller that needs to be tuned. Furthermore, a basic tracking controller law can be used to replace (4.15) to reduce the tracking error [139], which is given by:

$$u_j = \beta_{j,1}\left(y_j^* - \hat{x}_{j,1}\right) + \cdots + \beta_{j,p-1}\left(y_j^{*(p-1)} - \hat{x}_{j,p-1}\right) + \hat{x}_{j,p} \tag{4.17}$$

The approximate closed-loop characteristic polynomial can be expressed as similar as (4.16). The control law is simply a P control, if a 1st-order plant is adopted; while for a 2nd-order plant, the control law is a PD control.

4.2.2 Application in the voltage control

The three parameters need to be determined in ADRC framework are the input gain b_j, the observer bandwidth ω_{oj} and the controller bandwidth ω_{cj}. The control can work well with a rough estimation of the input gain [139]. The dynamics of the voltage control can be adjusted by the observer bandwidth and the controller bandwidth.

Assume that the plant of the jth DG can be modeled as a 1st-order system, the resulted controller in ADRC framework is a P controller, and the observer is a 2nd-order system, as shown in Figure 4.4. The controller $G_{cj}(s)$ can be designed according to the requirement of DC-bus voltage performance. The time-scale of the system is determined by the observer's bandwidth. The transfer function from system output y_j to the system output estimation $\hat{y}_j$ can be expressed by:

$$G_{oy}(s) = \frac{\alpha_{j,1}s + \alpha_{j,2}}{s^2 + \alpha_{j,1}s + \alpha_{j,2}} \tag{4.18}$$

where $\alpha_{j,1}$ and $\alpha_{j,2}$ are the elements of the observer gain L_j; i.e., $L_j = [\alpha_{j,1} \quad \alpha_{j,2}]^T$.

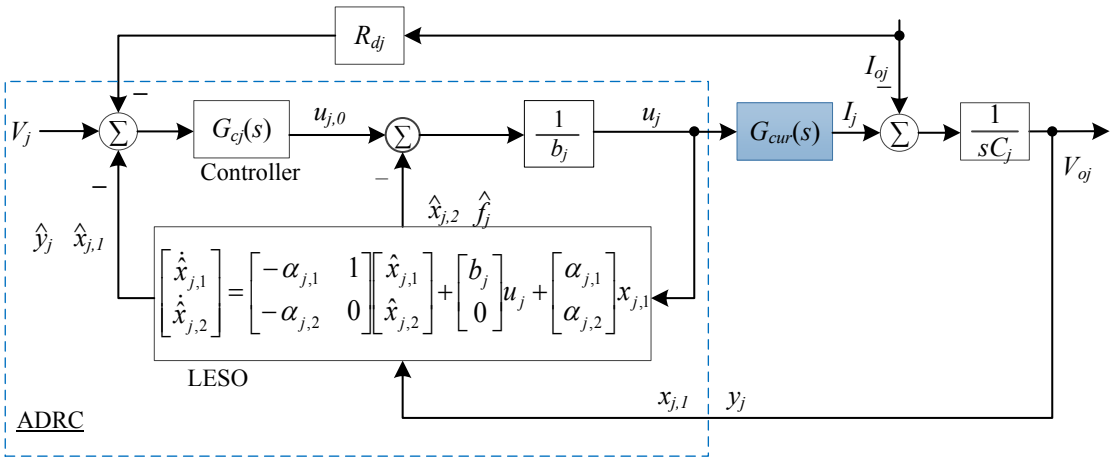


Figure 4.4 Implementation of the time scale droop control based on ADRC

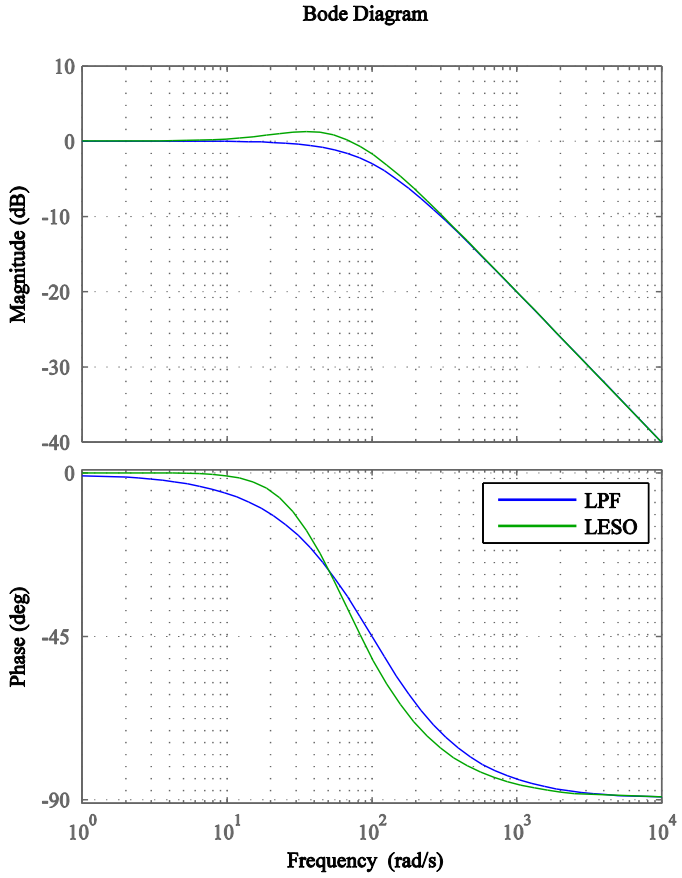


Figure 4.5 The Bode diagrams of the feedback LPF and LESO

To obtain equivalent control performance as the one with feedback LPF, the bandwidth of the LESO can be selected to be double of the LPF's cutoff frequency (i.e., $\omega_{oj} = 2\omega_j$). The Bode diagrams of these two methods are compared in Figure 4.5, in which the cutoff frequency of the LPF equals to 100 rad/s while the bandwidth of the LESO equals to 200 rad/s. It can be seen from the figure that, although the proposed LESO has some differences compared to the classic method with feedback LPF nearby the cutoff frequency, they match each other well in most part of the frequency spectrum, and have the same pattern.

The step responses of the feedback LPF and the LESO are shown in Figure 4.6. The bandwidths are selected as the same as in the analysis of Bode diagrams. The apparent difference is that the response of LESO has about 15% overshoot during the step transient while zero for the LPF. This overshoot in LESO may not be preferred in real applications, and it might be partially removed with efforts tuning the observer gains. However, the tuning of observer gains will loss the advantage of simple parameters design.

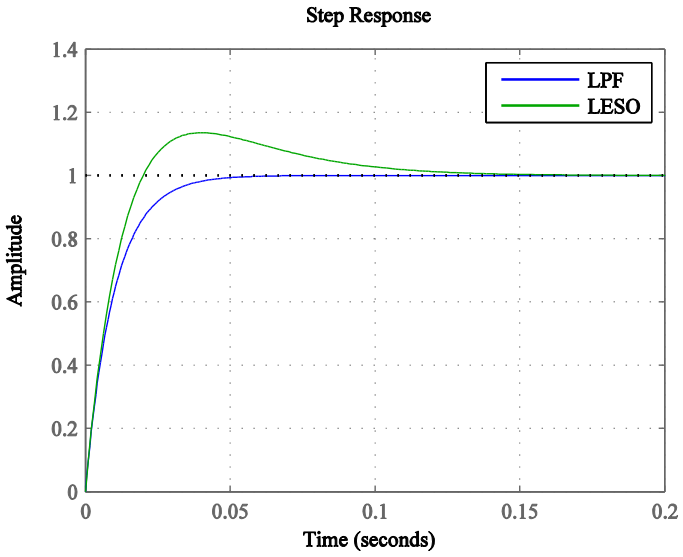


Figure 4.6 Step responses of the feedback LPF and the LESO

With these parameters, the obtained ADRC based time scale droop control can obtain equivalent performance compared to other implementations (e.g., the one with feedback LPF). Besides, the proposed ADRC based method is robust and not sensitive to the mismatch of the inner control loop and the DG's dynamics. Therefore, the DC microgrid under ADRC based droop time scale control can be analyzed by using the common character polynomial presented in (4.2).

4.3 Modeling of the multi-time scale DC microgrid

To analyze the multi-time scale DC microgrid under ADRC based droop control intuitively, the equivalent circuit of the DC microgrid can be constructed using basic electric components. The main results of the complete model (CM) will be retold in this section and a new parameterized reduced-order multi-scale model (N-RMM) will be introduced.

4.3.1 Equivalent circuits of DGs, cables and loads

The DG under droop control based on ADRC can be represented by the equivalent electric circuit in Thévenin form as an ideal voltage source with a *RLC* low-pass filter, as shown in Figure 4.7. The value of the perfect voltage source is the nominal voltage reference V_j, the resistance is the droop resistance R_{dj}, which is the inverse of droop constant D_j; C_j is the output capacitance. The reference voltage to the output voltage transfer function from the equivalent circuit is:

$$G_{eq}(s) = \frac{\frac{1}{L_j C_j}}{s^2 + \frac{R_{dj}}{L_j} s + \frac{1}{L_j C_j}} \tag{4.19}$$

Compare the equivalent circuit transfer function (4.19) with the common input-to-output transfer function (4.2), the relationship can be obtain is:

$$\omega_j = \frac{R_{dj}}{L_{dj}} \tag{4.20}$$

Therefore the value of virtual inductance can be solved from (4.20), with a predefined LPF cutoff frequency, which is also referred as the frequency scale of the voltage control loop. The time constant of the voltage control loop τ_j is defined as the inverse of the frequency scale, which is given by:

$$\tau_j = \frac{1}{\omega_j} = \frac{L_{dj}}{R_{dj}} \tag{4.21}$$

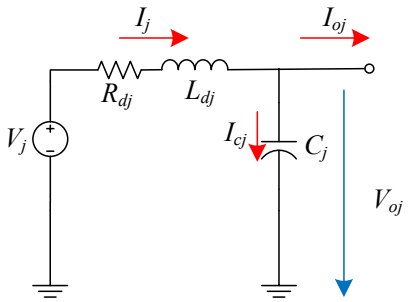


Figure 4.7 The equivalent circuit of the DG under droop control

This equivalent circuit contains the time scale information of the specified DG, and thus more precise than the traditional model using only perfect voltage source and resistor in series or current source and capacitor in parallel. Then the time domain DG model given by (3.9) is retold here:

$$\begin{cases} \frac{d}{dt} I_j = -\frac{R_{dj}}{L_{dj}} I_j + \frac{1}{L_{dj}} (V_j - V_{oj}) \\ \frac{d}{dt} V_{oj} = \frac{1}{C_j} (I_j - I_{oj}) \end{cases} \tag{4.22}$$

The time domain model of the cable between the *j*th DG and the common load point given by (3.12) in Chapter 3 is retold here:

$$\frac{d}{dt} I_{cj} = -\frac{R_{cj}}{L_{cj}} I_{cj} + \frac{1}{L_{cj}} (V_{oj} - V_L) \tag{4.23}$$

where $I_{cj} = I_{oj}$ denotes the current flowing from the *j*th DG to the common load point through the connecting cable, which equals to the output current of the *j*th DG; R_{cj} and L_{cj} are equivalent cable resistance and inductance, respectively; and V_L is the voltage at the common load point.

The tightly controlled load can be viewed as CPL, and the stability analysis of the system with CPL is a more critical task than in traditional power systems [104]. The relationship of load current as a function of load voltage in the ideal CPL is written by:

$$I_L = \frac{P_{CPL}}{V_L} \tag{4.24}$$

where P_{CPL} is the power absorbed by CPL; V_L is the load voltage. As presented in (3.15), the approximate linearized model can be obtained by conducting Taylor expansion at the operation point V_e, which is written by:

$$I_L \approx 2\frac{P_{CPL}}{V_e} - \frac{P_{CPL}}{V_e^2} V_L = I_{CPL} + \frac{V_L}{R_{CPL}} \tag{4.25}$$

Thus the linearized equivalent circuit of CPL can be viewed as a negative resistor $R_{CPL} = -V_e^2/P_{CPL}$ and a current sink $I_{CPL} = 2P_{CPL}/V_e$ connected in parallel.

4.3.2 New parameterized reduced-order multi-scale model

As discussed in the previous section 3.2.1, the combination of the equations (4.22), (4.23), and (4.25) forms the CM of the DC microgrid. CM has the order of 3*n*+1, where *n* is the number of DGs. The order increases with the number of DGs, this makes CM difficult to be applied directly for analytical stability tests in the microgrid with multiple DGs.

Although the practical DC microgrid may have multiple time scales, in most applications the time scales can be divided into two levels: small time scale group (fast DGs) and the large time scale

group (slow DGs). Then the system with *n* DGs can be represented by the fast-slow model which is composed of the equivalent fast DG (EFDG) and the equivalent slow DG (ESDG), as defined in the structure of RMM. They are given as:

$$\begin{cases} \frac{d}{dt}I' = -\frac{R'_d}{L'_d}I' + \frac{1}{L'_d}(V_N - V'_o) \\ \frac{d}{dt}I'' = -\frac{R''_d}{L''_d}I'' + \frac{1}{L''_d}(V_N - V''_o) \end{cases} \tag{4.26}$$

where I', I'' denote the current supplied by ESDG and EFDG, respectively; V'_o, V''_o denote the output voltages of ESDG and EFDG; R'_d, R''_d denote the equivalent virtual droop resistances of ESDG and EFDG; L'_d, L''_d denote the virtual inductances in ESDG and EFDG; and V_N is the common nominal voltage reference.

To combine the multiple DGs with similar time scale together, the arithmetic mean values of the droop resistance, virtual inductance can be adopted as proposed in [92]. But for the combination of DGs with different time scales and different power scales, the parameters of the ESDG and EFDG need to be rescale to per unit system (e.g., take 1 kW as the base). This leads to the new parameterized RMM (N-RMM). The calculation of the parameters is composed of two steps: first, calculate the normalized parameters of ESDG and EFDG; second, rescale the parameters of the equivalent DGs to a per kW system according to their power scales.

Normalized ESDG and EFDG

The parameters of the normalized ESDG and EFDG are obtained from the calculation of the normalized average values (per kW) of the DGs in the same group. They are given by:

$$\begin{cases} R'_d = \frac{1}{m}\sum_1^m R_{dj}P_{Nj} \\ R''_d = \frac{1}{n-m}\sum_{m+1}^n R_{dj}P_{Nj} \\ L'_d = \frac{1}{m}\sum_1^m L_{dj}P_{Nj} \\ L''_d = \frac{1}{n-m}\sum_{m+1}^n L_{dj}P_{Nj} \end{cases} \tag{4.27}$$

where P_{Nj} is the rated power of the *j*th DG in kW, the *j*th DG $j = 1,2 \dots, m$ is considered to be a slow DG, while $j = (m+1), \dots, n$ indicate that is a fast DG.

In low-voltage small-scale DC microgrids, the connecting cables can be viewed purely resistive. The equivalent cable resistances for ESDG and EFDG can be calculated using the similar method as described, the resulted equivalent parameters are:

$$\begin{cases} R_c' = \dfrac{1}{m}\sum_1^m R_{cj}P_{Nj} \\ R_c'' = \dfrac{1}{n-m}\sum_{m+1}^n R_{cj}P_{Nj} \end{cases} \tag{4.28}$$

where R_c', R_c'' are the connecting cables resistances of the normalized ESDG and EFDG, respectively.

Equivalent per kW system

The parameters of the equivalent per kW system can be obtained by rescaling the normalized ESDG and EFDG as well as the cable parameters. They are given by:

$$\begin{cases} \bar{R}_d' = R_d' \times ratio \\ \bar{R}_d'' = R_d'' \times (1-ratio) \\ \bar{L}_d' = R_d' \times ratio \\ \bar{L}_d'' = L_d'' \times (1-ratio) \end{cases} \tag{4.29}$$

$$\begin{cases} \bar{R}_c' = R_c' \times ratio \\ \bar{R}_c'' = R_c'' \times (1-ratio) \end{cases} \tag{4.30}$$

where $\bar{R}_d', \bar{R}_d''$ are droop resistances of ESDG and EFDG in equivalent per kW system, respectively; $\bar{L}_d', \bar{L}_d''$ are the virtual inductances of ESDG and EFDG in equivalent per kW system; $\bar{R}_c', \bar{R}_c''$ are the resistances of cable connecting ESDG and EFDG in equivalent per kW system; $ratio$ is the percentage of the power taken by the slow DGs, which is calculated by:

$$ratio = \frac{\sum_1^p P_{Nj}}{\sum_1^n P_{Nj}} = \frac{\text{power of slow DGs}}{\text{total power}} \tag{4.31}$$

Droop resistance and the equivalent cable resistance for each DG can also be combined to simplify the reduced-order model, given as:

$$\begin{cases} \bar{R}_s' = \bar{R}_d' + \bar{R}_c' \\ \bar{R}_s'' = \bar{R}_d'' + \bar{R}_c'' \end{cases} \tag{4.32}$$

where $\bar{R}_s', \bar{R}_s''$ denote the total resistance of ESDG and EFDG in equivalent per kW system. The output capacitors of DGs and the input capacitor of the load are fused together to form the normalized DC-bus capacitor $\bar{C}_{dc}$, as expressed by:

$$\bar{C}_{dc} = \frac{\sum_1^n C_j + C_L}{\sum_1^n P_{Nj}} \tag{4.33}$$

The parameters of the CPL also need to be converted into equivalent per kW value, thus the resulted equivalent CPL power is given by:

$$\bar{P}_{CPL} = \frac{P_{CPL}}{\sum_1^n P_{Nj}} \tag{4.34}$$

Then the equivalent circuit of the N-RMM with ESDG and EFDG can be represented by Figure 4.8, and the time domain nonlinear model is given by:

$$\begin{cases} \frac{d}{dt}\bar{I}' = -\frac{\bar{R}_s'}{\bar{L}_d'}\bar{I}' + \frac{1}{\bar{L}_d'}(V_N - V_o') \\ \frac{d}{dt}\bar{I}'' = -\frac{\bar{R}_s''}{\bar{L}_d''}I'' + \frac{1}{\bar{L}_d''}(\bar{V}_N - V_o'') \\ \frac{d}{dt}V_L = \frac{1}{\bar{C}_{dc}}\left(\bar{I}' + \bar{I}'' - \frac{\bar{P}_{CPL}}{V_L}\right) \end{cases} \tag{4.35}$$

where $\bar{I}'$ and $\bar{I}''$ are the normalized equivalent current of ESDG and EFDG in the per kW system.

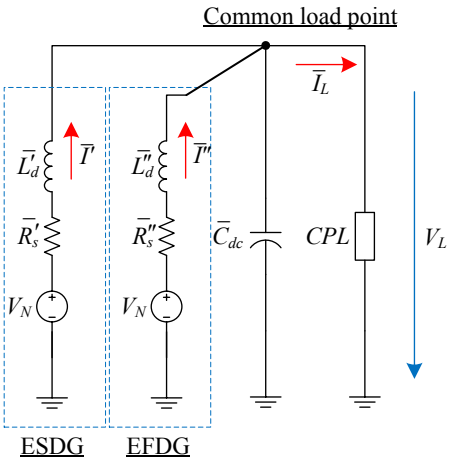


Figure 4.8 Equivalent circuit of the N-RMM represented by ESDG and EFDG

Replace the nonlinear CPL with a linearized model, then the approximate linearized model is:

$$\begin{cases} \frac{d}{dt}\bar{I}' = -\frac{\bar{R}_s'}{\bar{L}_d'}\bar{I}' + \frac{1}{\bar{L}_d'}(V_N - V_o') \\ \frac{d}{dt}\bar{I}'' = -\frac{\bar{R}_s''}{\bar{L}_d''}\bar{I}'' + \frac{1}{\bar{L}_d''}(V_N - V_o'') \\ \frac{d}{dt}V_L = \frac{1}{\bar{C}_{dc}}\left(\bar{I}' + \bar{I}'' - 2\bar{I}_{CPL} + \frac{1}{\bar{R}_{CPL}}V_L\right) \end{cases} \tag{4.36}$$

where the equivalent parameters in the linearized model are: the equivalent negative resistance $\bar{R}_{CPL} = -V_e^2/\bar{P}_{CPL}$ and the equivalent current sink $\bar{I}_{CPL} = 2\bar{P}_{CPL}/V_e$.

4.4 System stability analysis with ADRC control loop

The linearized model (4.36) can then be used to conduct stability test using Hurwitz-Routh stability criteria. The stability of the linear time-invariant (LTI) system depends on the locations of the state

matrix's eigenvalues. The system is stable when the real parts of the eigenvalues are all negative. The state matrix deduced from (4.36) is given by:

$$M = \begin{bmatrix} -\frac{\bar{R}_s'}{\bar{L}_d'} & & -\frac{1}{\bar{L}_d'} \\ & -\frac{\bar{R}_s''}{\bar{L}_d''} & -\frac{1}{\bar{L}_d''} \\ \frac{1}{\bar{C}_{dc}} & \frac{1}{\bar{C}_{dc}} & \frac{1}{\bar{C}_{dc}\bar{R}_{CPL}} \end{bmatrix} \tag{4.37}$$

It can be seen that, the system stability depends on the load condition as well as the value of the DC-bus capacitance.

In the ADRC based droop control, the damping ratio of the voltage control loop is controlled to be $\zeta_{Nj} = \sqrt{2}/2$. Then the relationship of DC-bus capacitance and the frequency scale can be deduced from (4.8), given by:

$$C_j = \frac{2D_j}{\omega_j} \tag{4.38}$$

Assume the required voltage tolerance $\delta = 5\%$ near the nominal voltage 380 V and the frequency scale is slected $\omega_j = 100\ rad/s$, the DC-bus capacitance can be calculated by:

$$C_j = \frac{2000P_{Nj}}{\omega_j\delta(1-\delta)V_{Nj}^2} = 2916 \times 10^{-6}P_{Nj} \tag{4.39}$$

Assume the DC-bus capacitance is equally distributed into DGs and the load, the output capacitance ratio per kW for DGs is half of the DC-bus capacitance ratio 2916 μF/kW (i.e., 1458 μF/kW) referred as basic capacitance ratio for DGs.

4.4.1 Sensitivity of DC-bus capacitances

Sizing of the output capacitances for DGs and input capacitances for CPLs is an important task in the design of a stable DC microgrid. Over conservative selection will lead to bulk capacitors and higher costs while over aggressive selection will let the system expose to the risk of instability in some critical operating conditions.

Stability testes are conducted in a three-DG system with variable capacitance ratio, to analyze the influence of the capacitance ratio on the system stability. The parameters of the examined multi-time scale DC microgrid are listed in Table 4.1, and a 2.5 kW CPL is applied. The DGs are divided into two groups, DG1 is slow DG with time constant 0.1 *s*; while DG2 and DG3 are both fast DGs with the time constant 0.01 *s*.

Table 4.1 The parameters of the examined DC microgrid

	DG 1	DG 2	DG 3	Cable 1	Cable 2	Cable 3
Rated power	1000 W	500 W	1000 W			
Equiv. Resistance*	6.86 Ω	13.72 Ω	6.86 Ω	0.25 Ω	1.0 Ω	1.5 Ω
Virtual inductance	0.686 H	0.137 H	0.0686 H			
Time constant	0.1 *s***	0.01 *s*	0.01 *s*			
Output capacitance	1458 μF	729 μF	1458 μF			

* the voltage error in 5% (DC-bus voltage 380V)

** the time constant is changeable also the virtual inductance

The eigenvalues traces of the state matrices in the CM and N-RMM with variable capacitance ratio are shown in Figure 4.9. The capacitance ratio decreases from the basic value (1458 μF/kW) with a step -1% of the basic value, until 1% of basic capacitance ratio. The roots are approaching the right-hand side with the decreases of capacitance ratio. When the capacitance ratio is smaller than 3% of the basic value (i.e., 43.74 μF/kW), the roots may enter into the right-hand side. It can be seen from the figure that, the proposed N-RMM can achieve similar results as that of the CM.

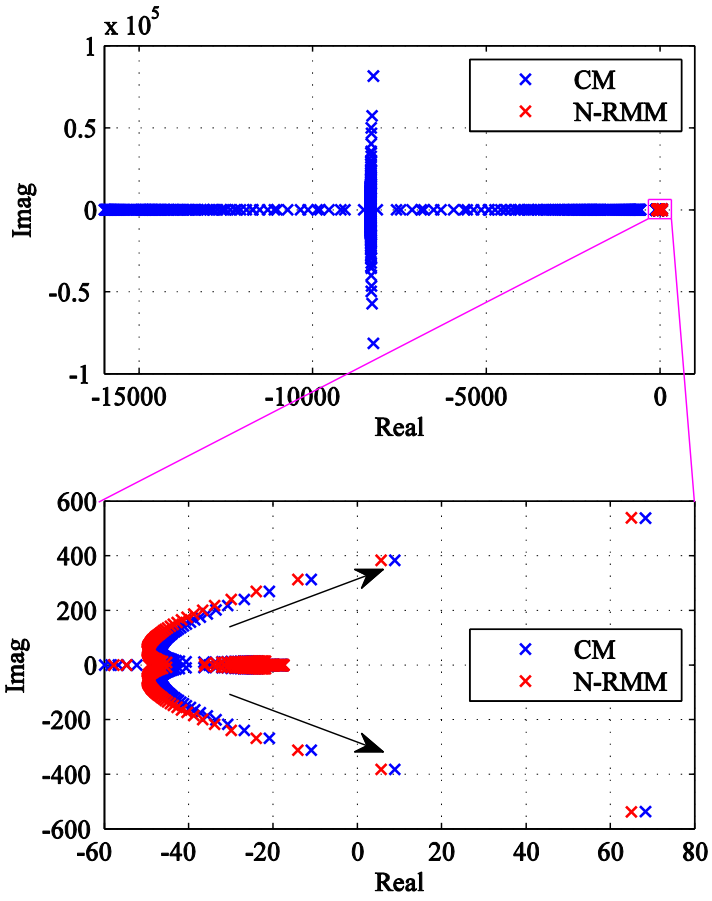


Figure 4.9 Eigenvalues traces of the state matrices in CM and N-RMM with variable DC-bus capacitance ratio

The estimated domains of attraction of N-RMM can be obtained from the original nonlinear model (4.35), by using the multi-modeling method [129]. This large-signal stability test can get the asymptotic stability domain. The resulted domains with variable DC-bus capacitance ratio are shown in Figure 4.10. These domains give the operation range around the equilibrium operation point (I_e, V_e) (refer to [129] to see details). It can be seen from the figure that the stable operation range shrinks quickly, with the decrease of DC-bus capacitance. When the capacitance ratio is smaller than 3% of the basic value (i.e., 43.74 μF/kW) the system becomes unstable, which is agree with the stability analysis of the linearized model using Hurwitz-Routh criteria.

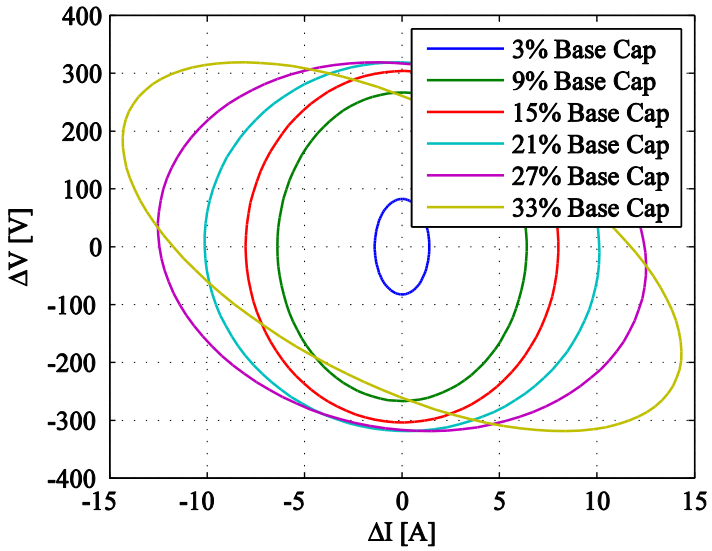


Figure 4.10 Estimated domains of attraction with variable DC-bus capacitance ratio in the N-RMM

4.4.2 Sensitivity of CPLs

From the state matrix, it can be seen that the small-signal stability of the system will be influenced by the power scale of CPL, which effects the values of the negative resistance. The same 3-DGs system is utilized with the same configuration as in the analysis of capacitance. The power of the CPL changes from 250 W to 2500 W gradually. The traces of the eigenvalue in CM and N-RMM with variable CPL are shown in Figure 4.11. The eigenvalues are approaching the positive real half-plant with the increases of load power. The system may become unstable when the load is higher than 80% of the rated power in condition that a very aggressive capacitance ratio 30 μF/kW (2.06% of basic capacitance ratio) is adopted.

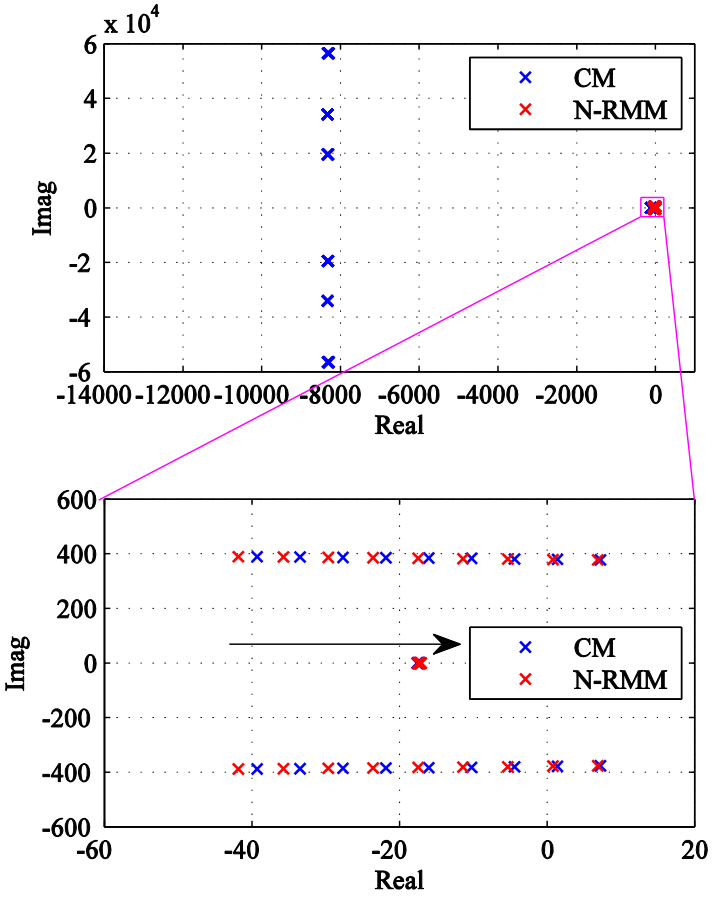


Figure 4.11 Eigenvalues traces of the state matrices in CM and N-RMM with variable CPL

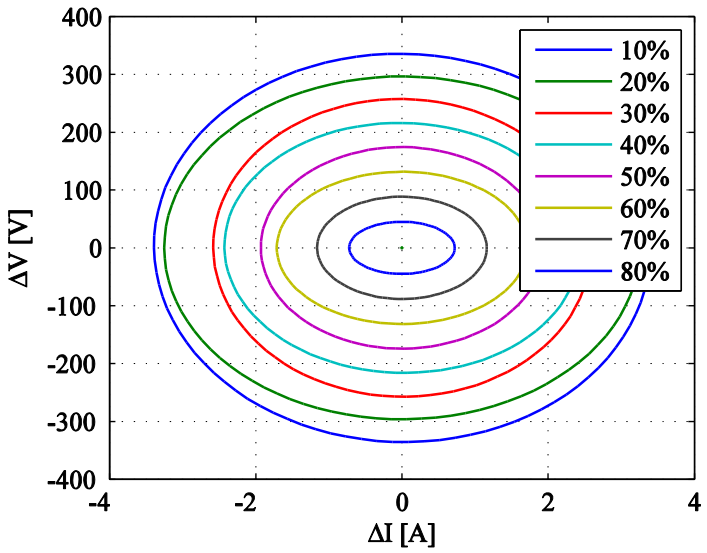


Figure 4.12 Estimated domain of attraction in N-RMM with variable CPL

The estimated domains of attraction with variable loads can also be obtained by using the multi-modeling method [129]. The results are shown in Figure 4.12, when the CPL varies from 10% rated load to the full rated load. The estimated domains of attraction shrink gradually with the increase of loads, and the system become unstable when CPL is high than 80% rated power.

4.4.3 Numerical simulation

Numerical simulation is conducted for the N-RMM in MATLAB/Simulink environment with CPL steps, and the simulation results are shown in Figure 4.13. The capacitance ratio selected is 145.8 μF/kW (i.e., 10% of the basic capacitance ratio). The CPL steps up from 60% to 100% of the rated load at t=2s and steps back at t=4s. ESDG and the EFDG share the load proportionally in steady-state; i.e., EFDG takes around 1.5 times of the load taken by ESDG, which is proportional to their rated power. During the step transients, EFDG takes the high frequency load variations to ensure the power balance and the voltage performance while ESDG smoothly changes the output current/power to response the steps (with slow dynamic response).

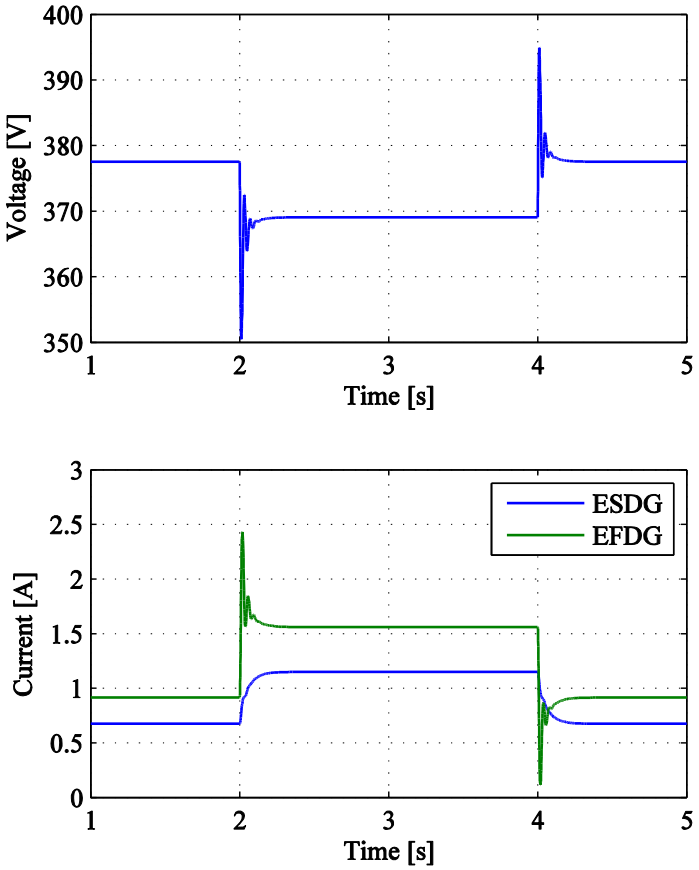


Figure 4.13 Numerical simulation results of N-RMM under CPL steps with the capacitance ratio 145.8 μF/kW

If a more aggressive capacitance ratio 30 μF/kW (i.e., 2.0% of the basic capacitance ratio) is adopted the system will become unstable when CPL overpass 80% rated power according to the previous stability tests. The numerical simulation results are presented in Figure 4.14 with CPL steps. The system becomes unstable when the CPL steps up from 60% to 100% rated load at t=2s, which agrees with the previous analyses.

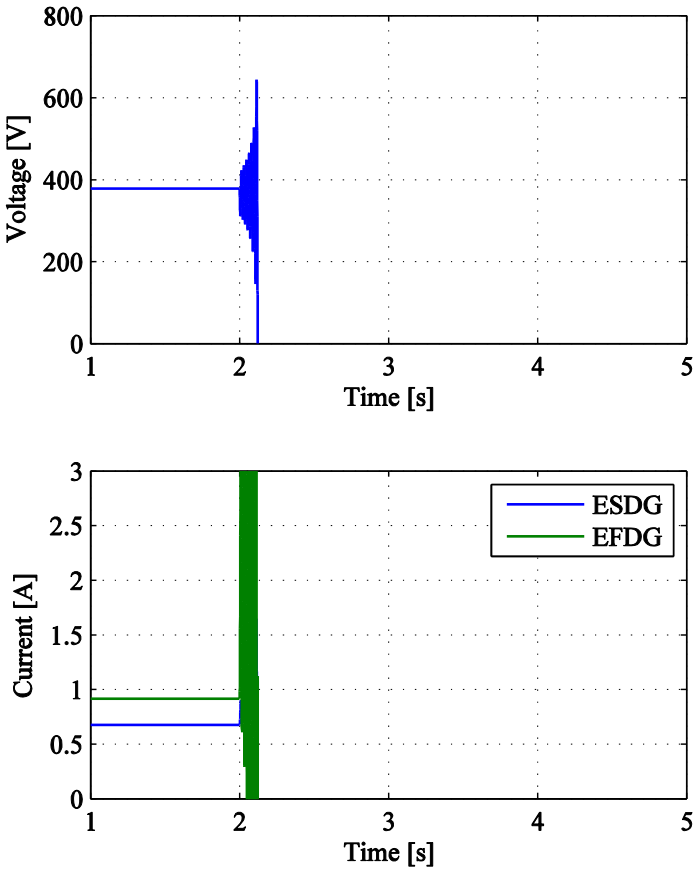


Figure 4.14 Numerical simulation results of N-RMM under CPL steps with the capacitance ratio 30 μF/kW

4.4.4 The procedure to design a stable DC microgrid

Instead of directly using iterative routines to try the size of DC-bus capacitance, the procedure can start from the basic capacitance ratio, and then decreases the value of DC-bus capacitance ratio until the system become unstable in any of the stability tests with CPL.

The flowchart of the proposed procedure is shown in Figure 4.15. Firstly, the dynamics of the current control loop for each DG is determined by measurements or estimations, and then the proper local voltage control frequency scale can be selected by (4.15). Secondly, the basic DC-bus capacitance ratio is calculated according to (4.39), using the largest time constant in a multi-time scale system. At last, the DC-bus capacitance ratio is iteratively reduce with a constant interval until any of the

stability tests cannot be satisfied. The minimum capacitance to maintain the multi-time scale DC microgrid stable can thus be obtained.

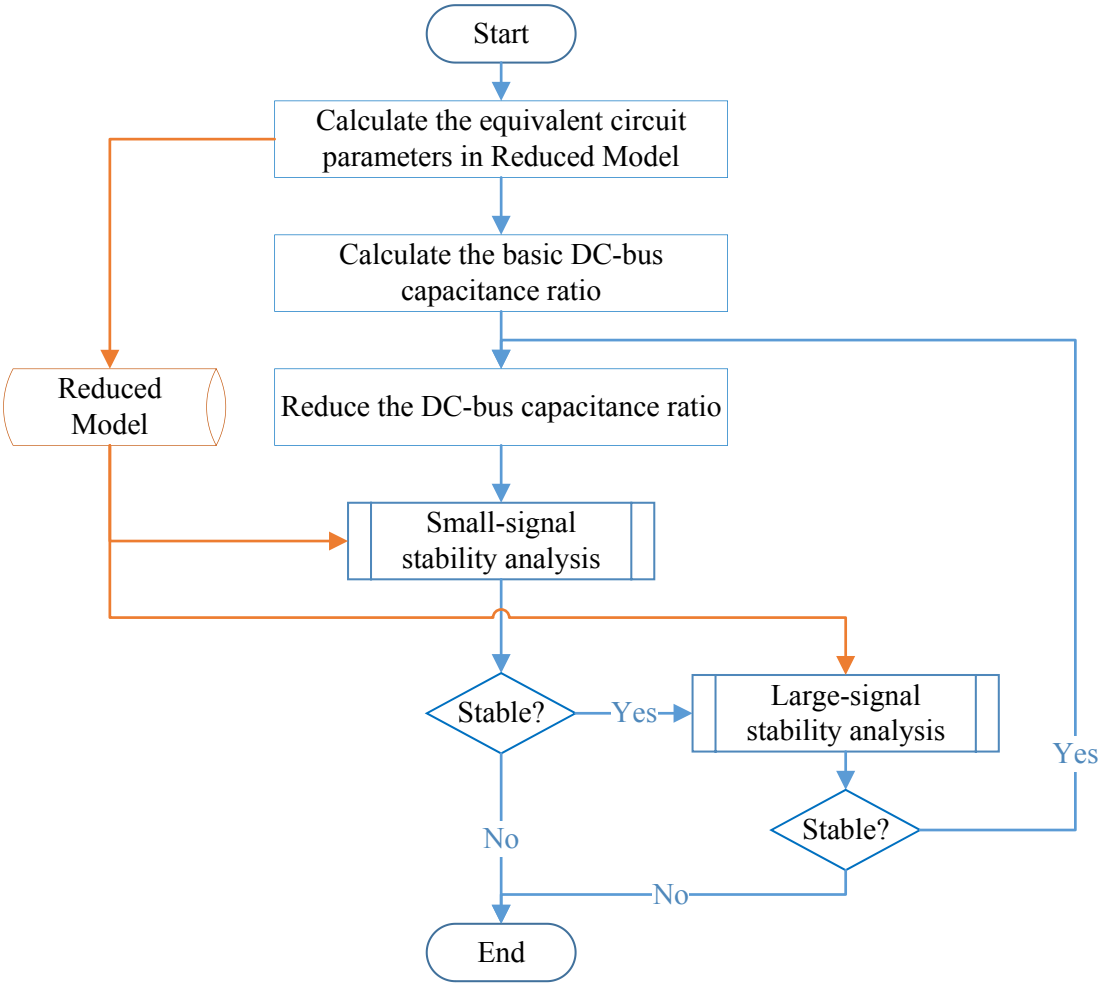


Figure 4.15 The procedure to calculate the minimum DC-bus capacitance ratio

4.5 Simulation

A typical multi-time scale DC microgrid with three DGs is built in MATLAB/Simulink environment. The ADRC based time scale droop control is adopted in the voltage control of each DG. DG1 has a low dynamic response with the time constant 0.1 *s* while the other two have fast dynamics with the time constant 0.01 *s*. The detailed parameters of the system are the same as these used for the stability analysis, listed in Table 4.1.

A relative aggressive capacitance ratio 60 μF/kW (i.e., about 13% of basic capacitance ratio) is adopted, which is also around four times of the minimum capacitance ratio. Numerical simulations are performed with CPL steps in MATLAB/Simulink. CPL steps from 1 kW to 2 kW at t=2s and then steps back at t=4s. Two scenarios are considered; i.e., single time constant and multiple time constants. If the time constants of the three DGs are all set 0.01 *s*; i.e., the observers' bandwidths are

200 rad/s. The simulation results with CPL steps are shown in Figure 4.16. The three DGs have same dynamic responses and share the load proportionally in both steady-state and dynamic states.

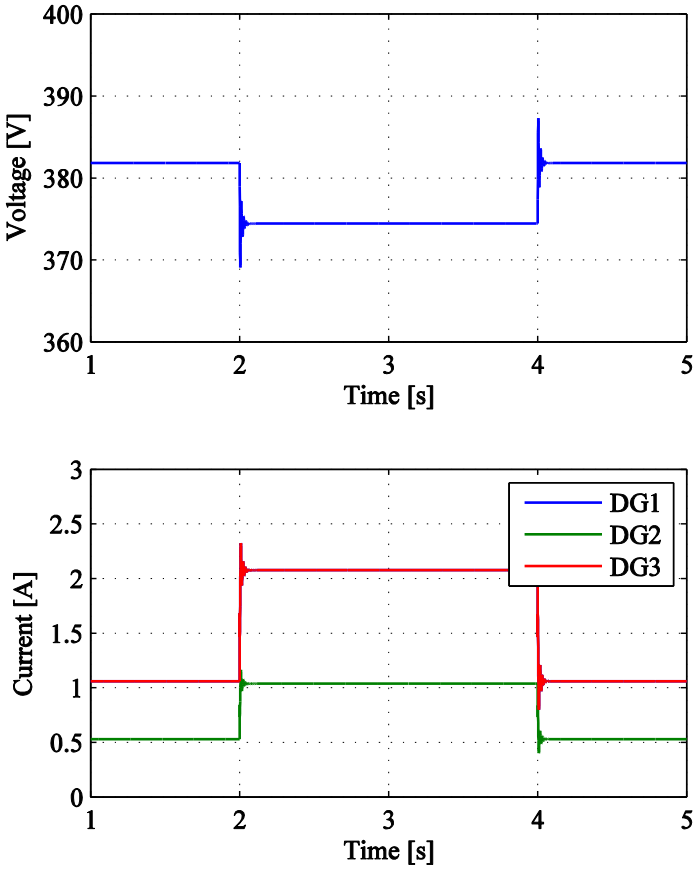


Figure 4.16 Simulation results of the DC microgrid with single time scale under ADRC droop control

When different time constants of the DGs are considered, the three DGs are set with different time constants; i.e., the observer bandwidth in DG1 is 20 rad/s and that of DG3 is 200 rad/s. The simulation results of voltage and the output currents with CPL steps are given in Figure 4.17. The three DGs share the load proportionally according to their rated power in steady-state; i.e., the output current of DG1 and DG3 is double of DG2's. During the step transients, the slow DG1 changes smoothly while the others response quickly to balance the power and maintain the DC-bus voltage.

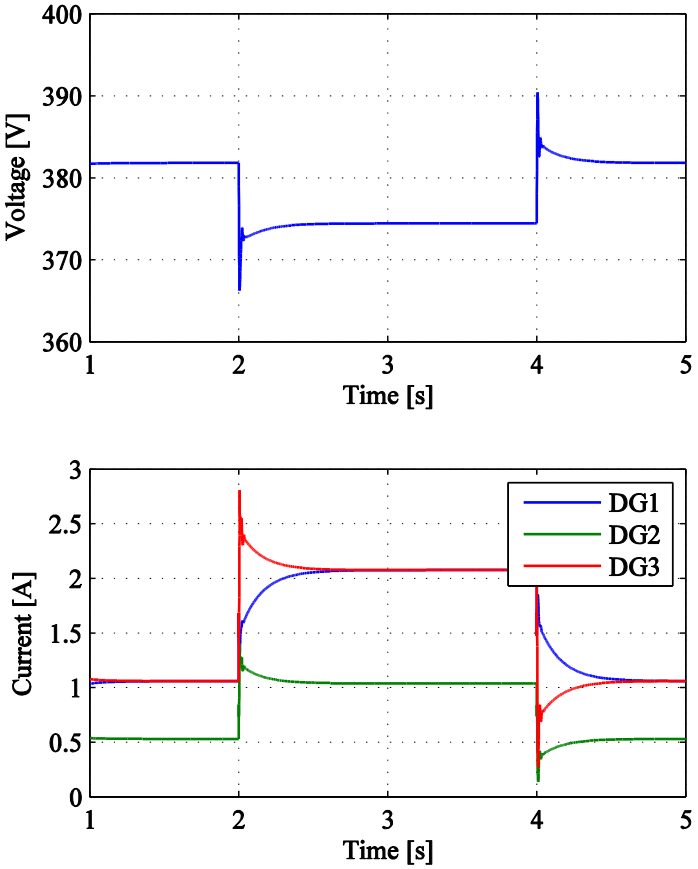


Figure 4.17 Simulation results of the DC microgrid with multi-time scale under ADRC droop control

Furthermore, the simulation results of the two LESO observers (in DG1 and DG3) are shown in Figure 4.18. The LESO in the slow DG (DG1) with the bandwidth 20 rad/s, can track the states smoothly; while the LESO in the fast one (DG3) with the bandwidth as high as 200 rad/s, can track more details of the transient information.

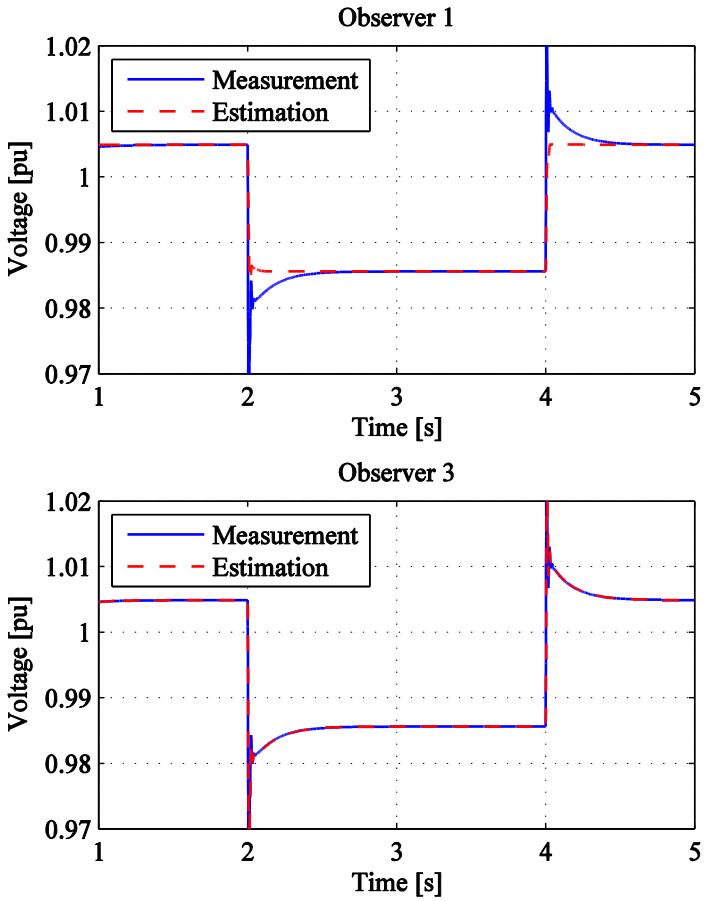


Figure 4.18 Simulation results of the Linear Extended State Observers in DG1 and DG3

4.6 Experimental validation

A laboratory scale DC microgrid is built to verify the proposed control method and the previous analyses. The test bench includes two DGs, both of them are connected via power converters to the DC-bus, and one resistive load is also connected via power converter to the DC-bus in order to act as CPL. Due to the limit of the hardware the DC-bus voltage 100 V DC is selected, which is lower than the expected level. The rated currents of the two DGs are both 3 A; i.e., 300 W for each DG (the input voltage/current of the DG is 50V/6A). The output of the DGs and the input of the load are connected to a common DC-bus capacitor.

The time constants of the two DGs can be different or same, with the variable time constant of DG1. The DG2 is a fast DG with the time constant 0.01 *s*, while that of DG1 can be 0.01 *s*, or 0.1 s as a slow DG. The basic DC-bus capacitance ratio is calculated from (4.39) (i.e., 42.1 mF/kW), when the time constant 0.01 *s* is considered. The required minimum capacitance ratio from the procedure Figure 4.15 is around 8% of the basic DC-bus capacitance ratio (i.e., 3.37 mF/kW). Therefore the

DC-bus capacitance should be selected between 2.02 mF and 25.26 mF. During the experimental tests a very aggressive value 2.93 mF is adopted.

CPL steps are applied to conduct the tests in order to verify the performance of the proposed control method. The CPL steps up from 300 W to 500 W at t=3s and then steps back at t=7s. Two scenarios are considered; i.e., single time scale and multiple time scales.

If the time constants of both the DGs are designed to be 0.01 *s*; i.e., the observers' bandwidths equal to 200 rad/s. The two DGs having same dynamic responses can share the load equally in steady-state and dynamic states during the test, as shown in Figure 4.19.

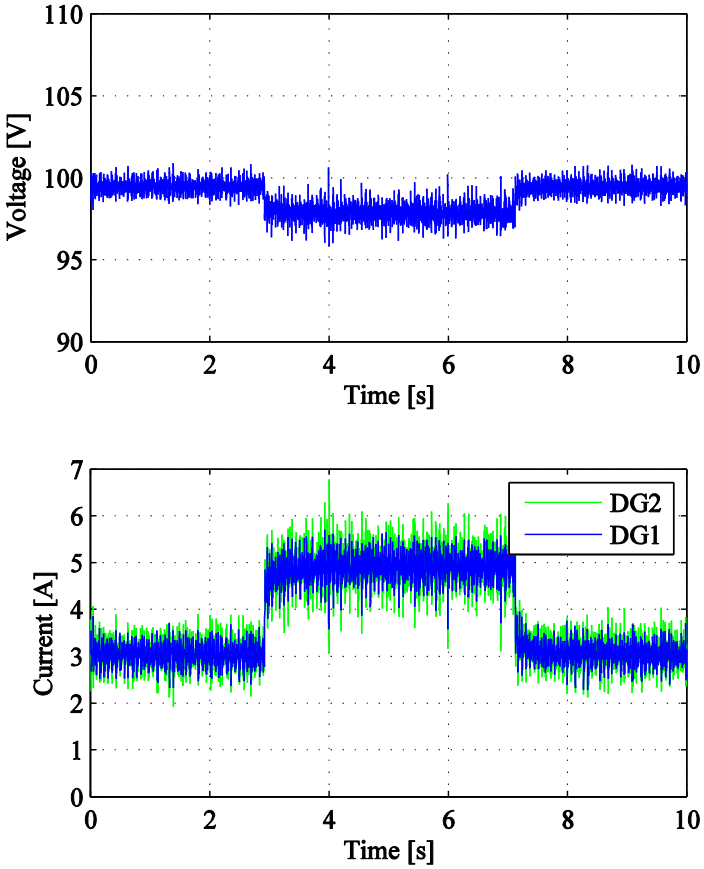


Figure 4.19 Experimental results of DC microgrid with single time scale using ADRC based control

When a multi-time scale DC microgrid is considered; i.e., the bandwidths of the two observers are 20 rad/s and 200 rad/s in DG1 and DG2, respectively. The experimental results with CPL steps are shown in Figure 4.20. The two DGs can equally share the load during steady-state. During step transients, the fast DG (DG2), supply/absorb the high frequency power, and DG1 changes its output smoothly.

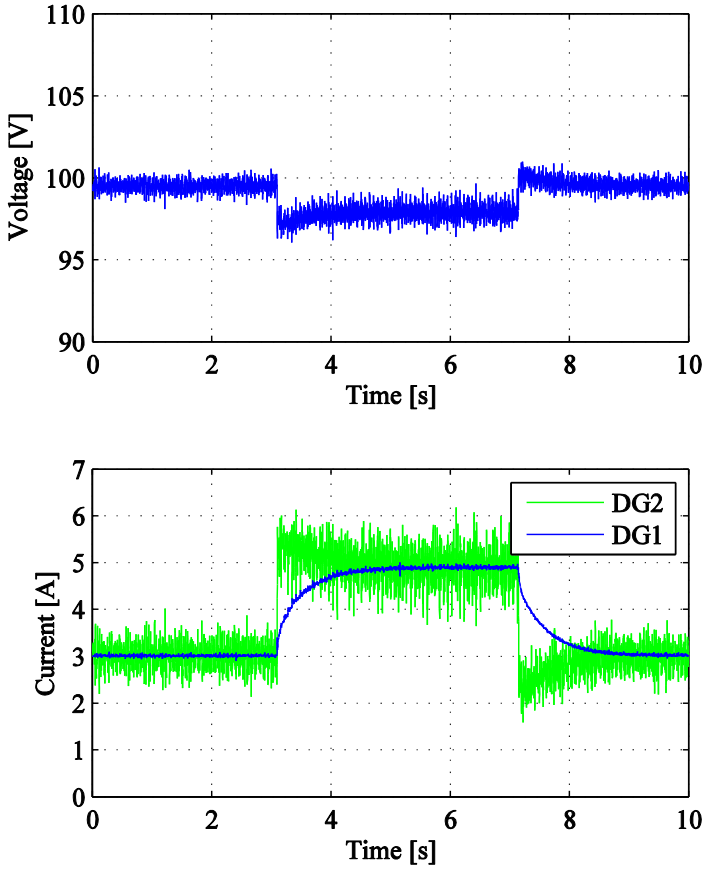


Figure 4.20 Experimental results of the DC microgrid with multi-time scales using ADRC based control

4.7 Conclusion

This chapter studies the implementation methods of droop control considering the DG's dynamic response. A time-scale droop control based on ADRC is proposed, and it can simplify the design of the system bandwidth by adjusting the bandwidths of the observer and the controller. A new parameterized reduced-order multi-scale model (N-RMM) is constructed to replace the complex complete model (CM). Based on this proposed N-RMM, a general procedure to design the DC-bus capacitance ratio for a stable multi-time scale DC microgrid is also introduced. Simulations and experimental test are carried out to verify the proposed method, and the obtained results are agreed with the theoretic analyses.

Chapter 5 Case Study

The previous chapters have studied the control and analysis of steady-state and dynamic states of DC microgrid separately. This chapter will examine the combination of steady-state compensations with dynamic control; i.e., the proposed ADRC based time scale droop control. The different four control methods (i.e., classic droop control, classic droop control with steady-state compensation, ADRC based time scale droop control, and ADRC based control with steady-state compensation) are applied to a general case so as to conduct comparisons. The model of the general case is built in in MATLAB/Simulink environment and simulations are conducted. The simulation results of these four methods are compared and discussed to conclude.

5.1 Presentation of the DC microgrid

Consider a general islanded low-voltage DC microgrid, which uses FC, PV panels and batteries to supply power to the local loads. The productions of renewable energies (e.g., PV panels under MPPT) are considered as disturbances because their output are not adjustable according to the microgrid requirement. Therefore PV panels and the load are combined to form the net load. FC and batteries are dispatchable generators (DGs), which adjust their output to maintain the balance of power. Moreover, FC requires to be controlled in a slow dynamic response to benefit of a long life-span, while batteries can response quickly to ensure voltage performance and absorb high frequency load.

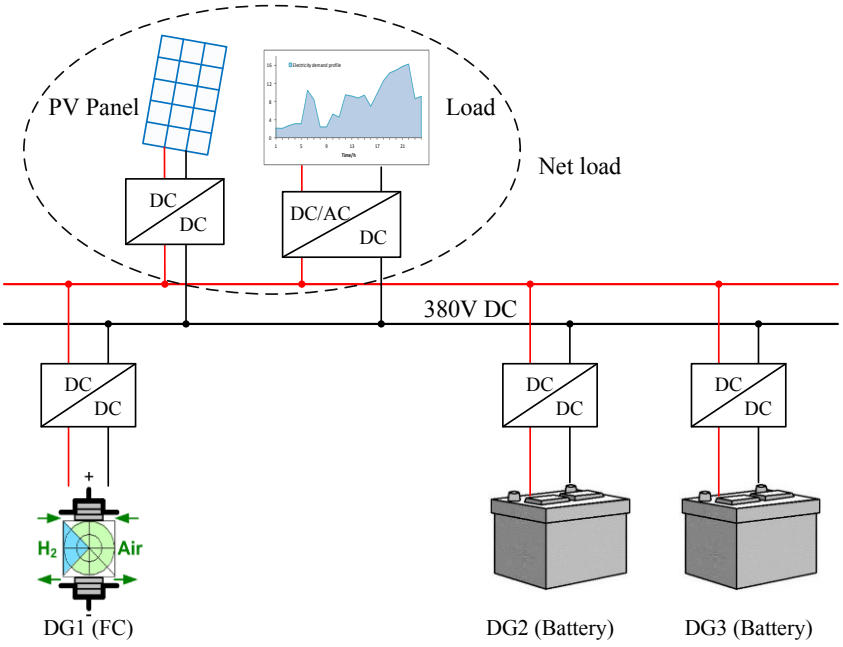


Figure 5.1 Structure of the DC microgrid with FC and batteries

The structure of the islanded DC microgrid is shown in Figure 5.1, the DGs are connected to the common DC-bus via power converters. Due to the geographical distribution, the connecting cables between the DGs and the load are not equal, thus the cable impedance are different. The DGs are viewed connected to the load point through equivalent connecting cables. The parameters of the DGs and the cables are listed in Table 3.1. The DC-bus voltage is designed to be 380 V.

Table 5.1 The parameters of the investigated DC microgrid with FC and batteries

	Power	Resistance	Inductance	Length
DG1 (FC)	1.0 kW			
DG2 (Battery)	0.5 kW			
DG3 (Battery)	1.0 kW			
Cable 1		5.00 Ω	300 μH	1000 m
Cable 2		1.00 Ω	60 μH	200 m
Cable 3		1.50 Ω	90 μH	300 m

5.2 Simulation analysis

The model of a 3-DG DC microgrid is built in MATLAB/Simulink environment. The classic droop control, droop control with steady-state compensation, ADRC based time scale droop control, and ADRC based time scale droop control with steady-state compensation are adopted to conduct the simulations. The control cycle of the steady-state compensation is rather large (e.g., 1.0 s is adopted) while the voltage is controlled every millisecond. The droop resistance is selected to be 0.05pu to ensure a voltage variation no more than 5%.

As discussed in the previous chapters, the common electronic loads with power electronic interfaces can be view as constant power loads (CPL). A CPL step is applied to test the aforementioned four control methods. A moderate capacitance ratio 500 μF/kW is selected to size the DC-bus capacitance. The load steps up from 1 kW to 2 kW at t=10s and steps back at t=20s. The simulation results of the classic droop control and classic droop control with steady-state compensation are shown in Figure 5.2 and Figure 5.3, respectively.

The steady-state performance is enhanced by the steady-state compensations proposed in Chapter 2, as shown in Figure 5.3. The load sharing between these DGs are proportion to their rated power; i.e., the output current of DG1 equals that of DG3, and they are double of DG2's. The load sharing error in classic droop control is eliminated by the steady-state compensation, while the dynamic responses are the same. The DG1 (FC) is forced to supply high frequency power, although it requires a slow dynamic response.

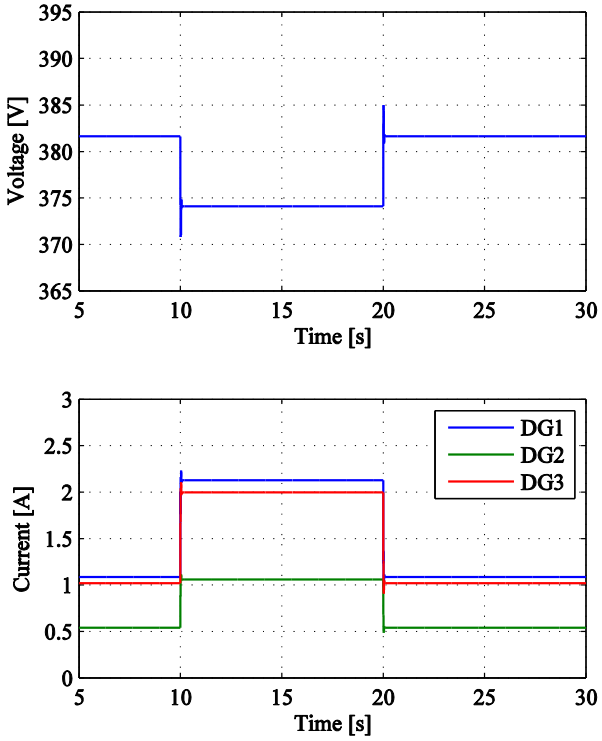


Figure 5.2 Simulation results of the classic droop control

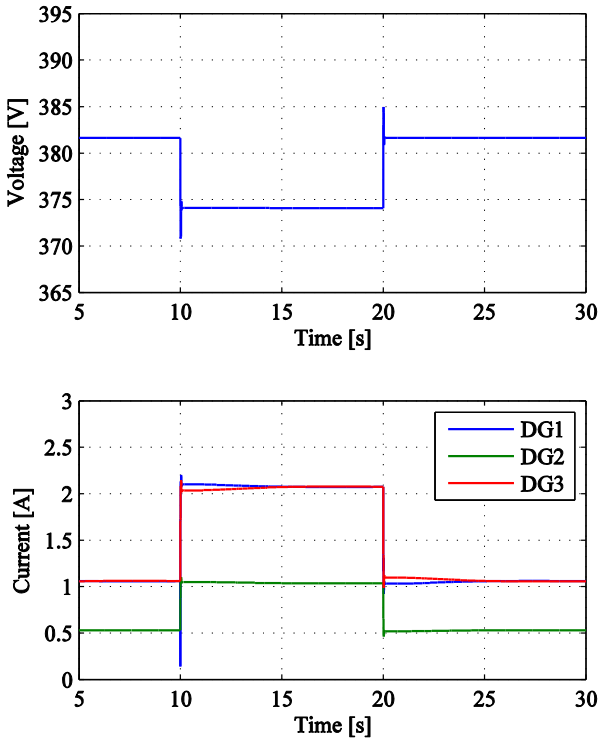


Figure 5.3 Simulation results of the classic droop control with steady-state compensations

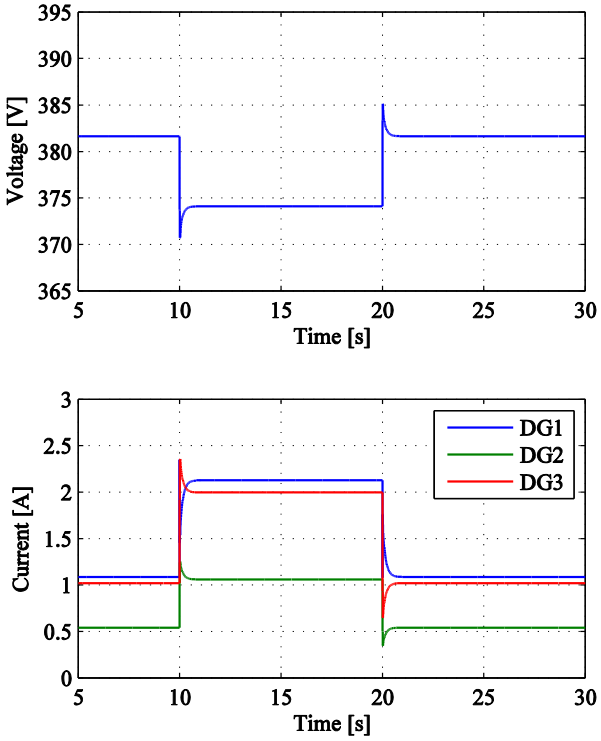


Figure 5.4 Simulation results of ADRC based time scale droop control

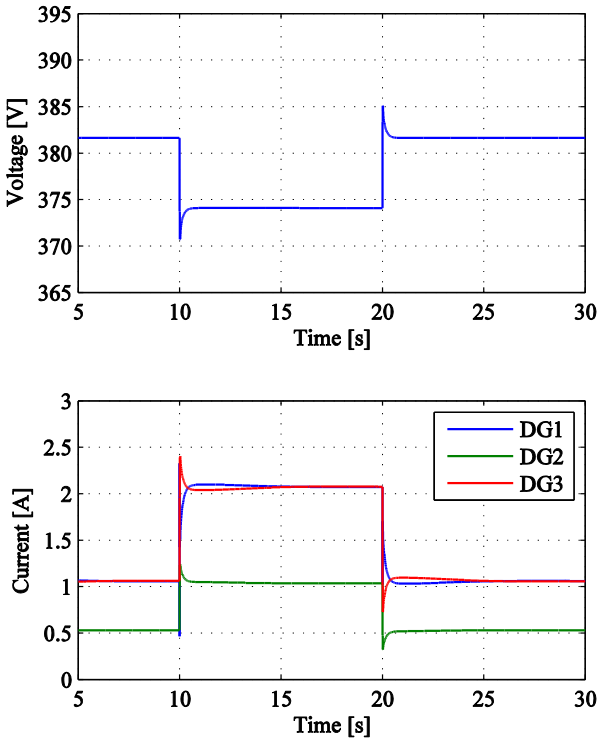


Figure 5.5 Simulation results of ADRC based time scale droop control with steady-state compensations

Furthermore, ADRC based time scale droop control without and with steady-state compensation are adopted to compare with classic droop control. DG1 (FC) is designed to have slow dynamic response with the time constant 0.1 *s*, while the other DGs have fast dynamic response with the time constant 0.01 *s*.

The simulation results of voltage and load sharing are shown in Figure 5.4 and Figure 5.5. With the utilization of ADRC based time scale droop control, DG1 can only response to slow frequency load, while DG2 and DG3 can response quickly to maintain the voltage performance and power balance. The load sharing error in steady-state between the DGs, as shown in Figure 5.4, is also eliminated by steady-state compensations without harming the dynamic feature, as shown in Figure 5.5.

5.3 Experimental validation

A laboratory scale DC microgrid test bench with three DGs are built to verify the performance comparison of the different control methods. The three DGs are represented by three DC power sources, and they are connected to the DC-bus via boost DC-DC power converters. The parameters of the three DGs and the corresponding connecting cables are listed in Table 5.3. The DC-bus voltage is select to be 100 V DC due to the limit of the hardware.

Table 5.2 The parameters of the laboratory DC microgrid test bench

	Voltage	**Current**		**Resistance**
DG1 (FC)	60 V	6 A	**Cable 1**	0.1 Ω
DG2 (Battery)	60 V	3 A	**Cable 2**	0.08 Ω
DG3 (Battery)	60 V	6 A	**Cable 3**	0.05 Ω

The control of the three DGs are realized by a real-time simulator dSPACE DS1104, in which the control algorithms are designed in MATLAB/Simulink, then be complied and downloaded into the dSPACE. This makes the test of different algorithms can be rapidly and easily implemented.

The four control methods are tested under the step of the resistive load, which can step from 24.2 Ω to 16.1 Ω and then step back. To reduce the number of current sensors, only the input current of the power converters are measured not the output current. The experimental results of the classic droop control without and with steady-state compensations are shown in Figure 5.6 and Figure 5.7. It can be seen clearly that the DGs cannot share proportionally load when compensations are not applied; e.g., the input current error between DG1 and DG2 is not zero. Once steady-state compensations are adopted, the DGs can share the load proportionally according to their rated volumes; i.e., the current of DG1 equals to that of DG3, which is the double DG2's current. Though a good performance is achieved with these compensation, the FC (DG1) is forced to take high frequency load variations, which will reduced its life-span.

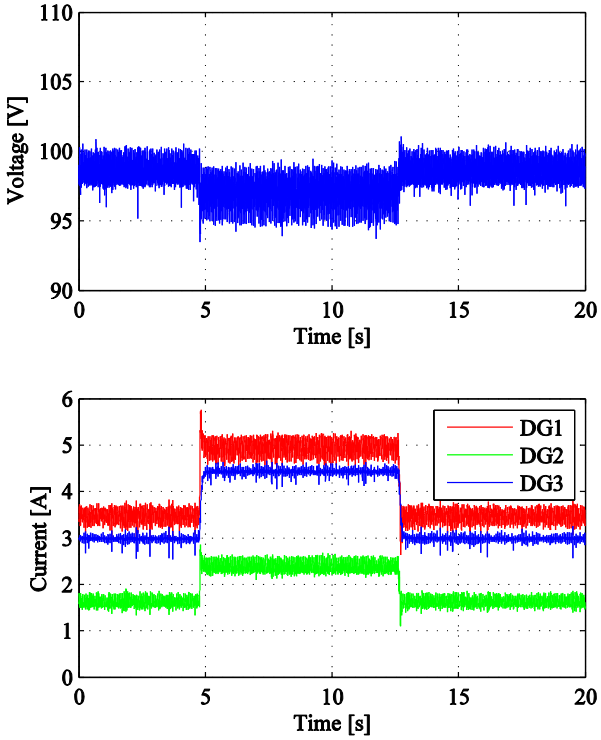


Figure 5.6 Experimental results of classic droop control

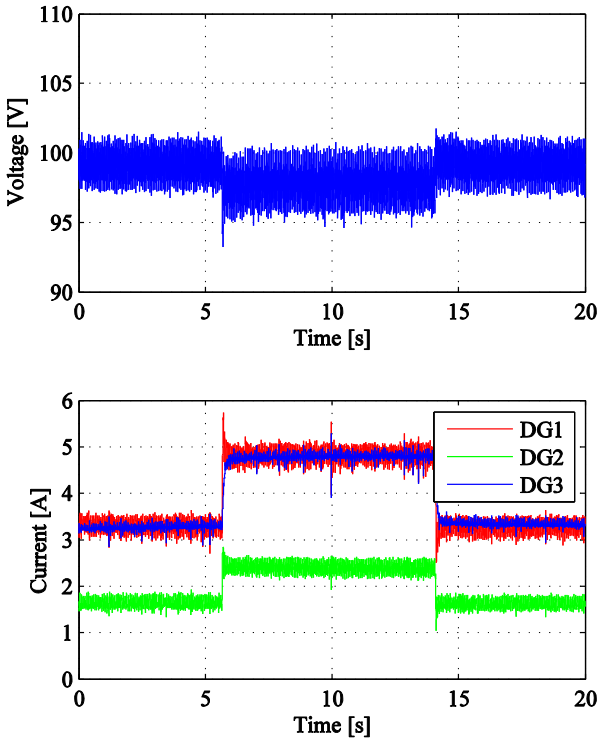


Figure 5.7 Experimental results of classic droop control with steady-state compensations

To consider the dynamics of the DGs, the time scale ADRC based droop control without and with steady-state compensations are also examined by load steps. The experimental results are shown in Figure 5.8 and Figure 5.9. In these two control methods, the DG1 (FC) only supply low frequency load while other DGs takes the high frequency load to maintain the power balance. The steady-state load sharing errors among the DGs in Figure 5.8 can be compensated by the proposed compensation method, as shown in Figure 5.9, the three DGs share the load properly in both steady-state and dynamic state. The experimental results are agree with the simulation analyses, which confirms that the ADRC based time scale control can be combined with the steady-state compensations to satisfy the requirements for both steady-state and dynamic performances.

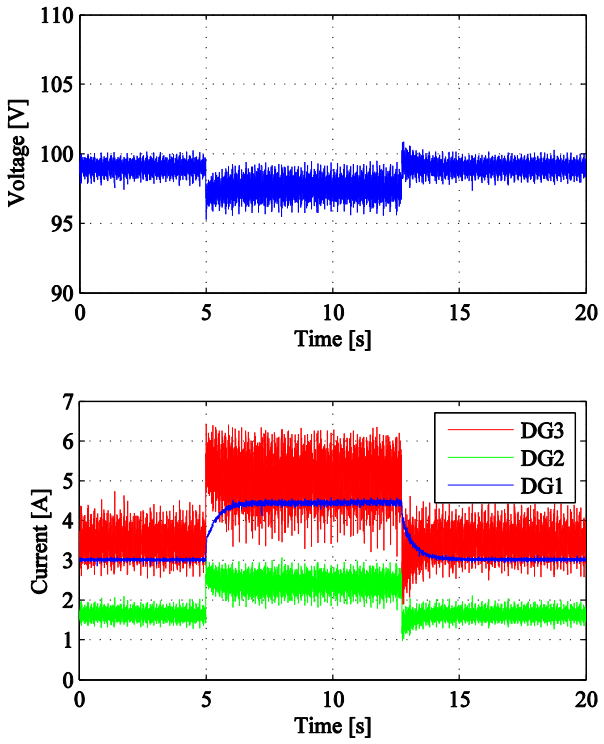


Figure 5.8 Experimental results of ADRC based time scale droop control

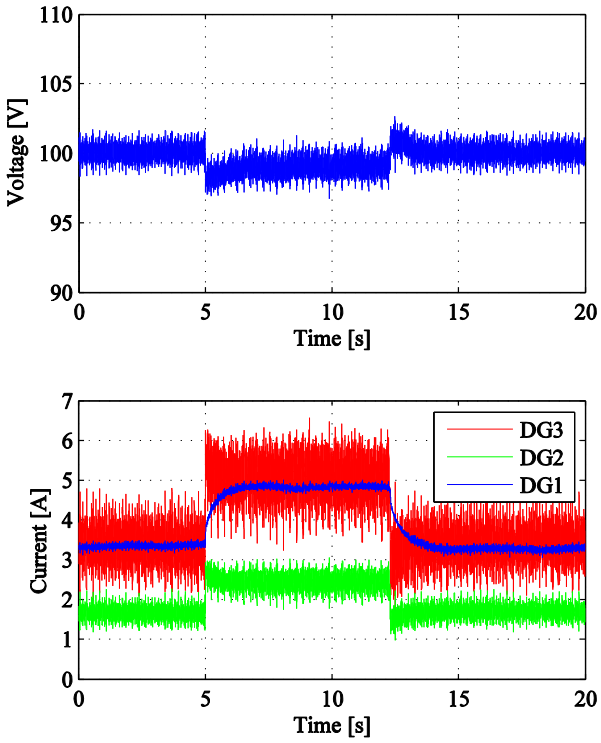


Figure 5.9 Experimental results of ADRC based time scale droop control with steady-state compensations

5.4 Conclusion

In summary, the proposed ADRC based time scale droop control is verified that it can be combined with steady-state compensations to enhance the performance of DC microgrid in both steady-state and dynamic states. The comparison of these four different methods according to their steady-state and dynamic performances is shown in Table 5.3.

Table 5.3 The performance comparison of different control methods

	Steady-state performance	**Dynamic performance**
Droop control	Fair	Poor
Droop control with compensations	Good	Poor
ADRC based control	Fair	Good
ADRC with compensations	Good	Good

Chapter 6 General Conclusions

6.1 Summary of the dissertation

In this dissertation, we focus on three topics regarding the control and analysis of the DC microgrid. The three discussed topics and the experimentations in this dissertation are summarized in the following parts.

6.1.1 Voltage control and load sharing in steady-state condition

The classic droop control faces the conflict between voltage regulation and load sharing performance when applied to the low-voltage DC microgrid. In this dissertation a unified compensation structure based on the common current is proposed, to enhance the voltage and load sharing simultaneously. The boundaries of the compensation parameters are also analyzed to maintain the system stability.

6.1.2 Modeling and analysis of multi-time scale DC microgrid

A virtual inductor is introduced to combine with the droop resistor, such that the dynamics of the distributed generator can be properly considered. Then, a reduced-order multi-scale model (RMM) is proposed to represent the multi-time scale DC microgrid, which groups the distributed generators with similar time constants together, and then the groups are combined to form the model. It not only reduces the order of the model but also maintains the major time scale information.

6.1.3 Time scale droop control using ADRC

A time scale droop control method based on Active Disturbance Rejection Control (ADRC) for the DG is proposed. It is robust to model description error and the voltage dynamics can be explicitly adjusted by the bandwidth of controller and observer. Based on the new parameterized reduced-order multi-scale model (N-RMM) of the DC microgrid, a general procedure to design a stable DC microgrid is also constructed.

6.1.4 Experimental validation

A laboratory scale DC microgrid is built to verify the proposed method and analysis. It comprises three distributed generators connected to the common DC-bus via power converters, and a variable resistive load. The control algorithm can be realized by the real-time simulator dSPACE DS1104. The control strategies designed in Matlab/Simulink can be downloaded into the real-time controller of dSPACE to carry out the tests. This flexible platform makes the tests of different configurations and control algorithms to be easily realized.

6.2 Future works

6.2.1 The application of multi-time scale DC microgrid

The basic modeling and analyses have been discussed in this dissertation, as well as some laboratory scale experimental tests. However, the application of the proposed methods in a real DC microgrid with multiple distributed generators needs to be conducted so as to further confirm their effectiveness.

6.2.2 The control under various complex configurations

This dissertation work focuses on a single bus DC microgrid, the complex configurations are not considered. The expansion of the multi-time scale modeling method to other complicated topologies still needs to be investigated.

6.2.3 Online monitoring

The stability is not only concerned in the design stage but also in the operation, especially for the configurable DC microgrids. The benefit of the reduced-order multi-scale model is its simplicity, thus the application of the proposed model in the online stability monitoring will be an interesting topic. Thus the system parameters need to be estimated in the higher level controller or distributed in some local controller, and the stability level of the system can be evaluated online.

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SPIM

■ École doctorale SPIM - Université de Technologie Belfort-Montbéliard
F - 90010 Belfort Cedex ■ tél. +33 (0)3 84 58 31 39
■ ed-spim@univ-fcomte.fr ■ www.ed-spim.univ-fcomte.fr

utbm
université de technologie
Belfort-Montbéliard