Vieillissement accéléré de modules de puissance de type MOSFET SiC et IGBT Si basé sur l'analyse de profils de mission d'onduleurs photovoltaïques.

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Mission Profile-Based Accelerated Ageing Tests of SiC MOSFET and Si IGBT Power Modules in DC/AC Photovoltaic Inverters

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To my family, my source of love, self-confidence, encouragement and inspiration...

My father Gabriel, my mother Josephine, my brother Barrak and my dear sisters Layaly, Hanadi and Amanie, it's to you that I dedicate my success, my doctorate degree and these years of challenging work spent far from you...

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Abstract

In the case of photovoltaic installations, the DC/AC inverter has the highest failure rate, and the anticipation of its breakdowns is still difficult, while few studies have been done on the reliability of this type of inverter. The aim of this PhD is to propose tools and methods to study the ageing of power modules in this type of application, by focusing on ageing phenomena related to thermo-mechanical aspects.

As a general rule, the accelerated ageing of power modules is carried out under aggravated conditions of current (Active Cycling) or temperature (Passive Cycling) in order to accelerate the ageing process. Unfortunately, when applying this type of accelerated ageing tests, some failure mechanisms that do not occur in the real application could be observed, while inversely, other mechanisms that usually occur could not be recreated.

The first part of the PhD focuses on the implementation of an accelerated ageing method of the semiconductor devices inside photovoltaic inverters. This is accomplished by analyzing the mission profiles of the inverter's output current and ambient temperature, extracted over several years from photovoltaic power plants located in the south of France. These profiles are used to study photovoltaic current dynamics, and are introduced into numerical models to estimate losses and junction temperature variations of semiconductors used in inverters, using the cycle counting algorithm "Rainflow".

This method is then performed in two experimental test benches. In the first one, the devices under test are IGBT modules, where the accelerated ageing profile designed is implemented using the opposition method. Moreover, an in-situ setup for monitoring ageing indicators (thermal impedance and dynamic resistance) is also proposed and evaluated. The second bench is devoted to study the ageing of SiC MOSFET power modules. The accelerated ageing test is carried out under the same conditions as for the IGBT modules with more monitored electrical indicators, but this time by disconnecting the semiconductor devices from the inverter. The results obtained allowed to determine several potential ageing indicators of IGBTs and SiC MOSFETs used in a photovoltaic inverter.

Keywords

Photovoltaic Inverter - Mission profile - Silicon Carbide MOSFET - Accelerated ageing tests - Power cycling - Thermal cycling - Reliability - Condition monitoring - Failure indicators - Power losses estimation - Junction temperature estimation

Résumé

Dans le cas des installations photovoltaïques, l'onduleur est le premier élément défaillant dont il est difficile d'anticiper la panne, et peu d'études ont été faites sur la fiabilité de ce type de convertisseur. L'objectif de cette thèse est de proposer des outils et méthodes en vue d'étudier le vieillissement des modules de puissance dans ce type d'application en se focalisant sur les phénomènes de dégradation liés à des aspects thermomécaniques.

En règle générale, le vieillissement accéléré des modules de puissance est effectué dans des conditions aggravées de courant (Cyclage Actif) ou de température (Cyclage Passif) pour accélérer les processus de vieillissement. Malheureusement, en appliquant ce type de vieillissement accéléré, des mécanismes de défaillances qui ne se produisent pas dans la vraie application peuvent être observés et, inversement, d'autres mécanismes qui se produisent habituellement peuvent ne pas apparaître.

La première partie de la thèse se focalise donc sur la mise en place d'une méthode de vieillissement accéléré des composants semi-conducteurs des onduleurs photovoltaïques. Cela est fait en s'appuyant sur l'analyse des profils de mission du courant efficace de sortie des onduleurs et de la température ambiante, extraits des centrales photovoltaïques situées au sud de la France sur plusieurs années. Ces profils sont utilisés pour étudier les dynamiques du courant photovoltaïque, et sont introduites dans des modèles numériques pour estimer les pertes et les variations de la température de jonction des semi-conducteurs utilisés dans les onduleurs, en utilisant l'algorithme de comptage de cycles "Rainflow".

Cette méthode est ensuite mise en œuvre dans deux bancs expérimentaux. Dans le premier, les composants sous test sont des modules IGBT. Les composants sont mis en œuvre dans un banc de cyclage utilisant la méthode d'opposition et mettant en œuvre le profil de vieillissement défini précédemment. Un dispositif in-situ de suivi d'indicateurs de vieillissement (impédance thermique et résistance dynamique) est également proposé et évalué. Le deuxième banc est consacré à l'étude de modules de puissance à base de MOSFET SiC. Le vieillissement est effectué dans les mêmes conditions que pour les modules IGBT et de nombreux indicateurs électriques sont monitorés mais, cette fois ci, en extrayant les composants de l'onduleur de cyclage. Les résultats obtenus ont permis de déterminer des indicateurs de vieillissement d'IGBT et de MOSFET SiC utilisés dans un onduleur photovoltaïque.

Mots clés

Onduleur photovoltaïque - Profils de mission - MOSFET en Carbure de Silicium - Tests de vieillissement accéléré - Cyclage actif - Cyclage passif - Fiabilité du semi-conducteur - Suivi de l'état de santé - Estimation des pertes - Estimation de la température de jonction

Abbreviations

AC	Alternative Current
Al	Aluminum
Al_2O_3	Aluminum Oxide
AlN	Aluminum Nitride
APC	Active Power Cycling
BJT	Bipolar Junction Transistor
BTI	Bias Temperature Instability
CM	Condition Monitoring
CT	Current Transformer
CTE	Coefficient of Thermal Expansion
Cu	Copper
DC	Direct Current
DCB	Direct Copper Bonded
DFT	Discrete Fourier Transform
DMOS	Double-diffused Metal–Oxide–Semiconductor
DPT	Double Pulse Test
DUT	Device Under Test
FFT	Fast Fourier Transform
FIB	Focused Ion Beam
FPGA	Field Programmable Gate Array
FT	Fourier Transform
GaN	Gallium Nitrade
HALT	Highly Accelerated Life Test
HF	Humidity Freeze
HMI	Human Machine Interface
HTGB	High Temperature Gate Bias
HTOB	High Temperature Operating Bias
IDFT	Inverse Discrete Fourier Transform
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PTC	Passive Temperature Cycling
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SAM	Scanning Acoustic Microscopy
SEB	Single-Event-Burnout
SEGR	Single-Event-Gate-Rupture
SEM	Scanning Electron Microscopy
Si	Silicon
SiC	Silicon Carbide
SiO_2	Silicon Dioxide
TSCT	Two Stage Current Transformer
TSEP	Thermo-Sensitive Electrical Parameters

Notations

α	PWM duty cycle
C	Heat capacity
C_{bus}	DC bus link capacitor
C_{cb}	Collector-base capacitance
C_{dec}	Decoupling capacitors
C_{DS}	Drain-source capacitance
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
$C_{i_{ss}}$	MOSFET's input capacitance
$Cos\ \varphi$	Power factor
$C_{o_{ss}}$	MOSFET's output capacitance
$C_{r_{ss}}$	MOSFET's reverse capacitance
C_{th}	Thermal capacitance
D	Cumulative damage
D_i	Device i
ΔI	Current variation
$\Delta I/\Delta t$	Slope of a current's variation
ΔI_{min}	Minimum current variation
ΔT_C	Case temperature swing
ΔT_J	Junction's temperature swing
ΔT_{JA}	Difference between the junction and the ambient temperatures
ΔT_{J_D}	Diode's T_J swing on a fundamental period
ΔT_{J_T}	Transistor's T_J swing on a fundamental period
Δt	Time step
D_w	Diameter of the wire bonding
dZ_{th}	Derivative of the thermal impedance
E	DC-link voltage
E_{off}	Turn-off energy losses
E_{on}	Turn-on energy losses
E_{rec}	Diode's reverse recovery energy losses
E_T	IGBT's threshold forward voltage
E_0	Diode's threshold voltage
φ	Flux density
f_{out}	Fundamental frequency
f_{sw}	Switching frequency
I	Power Switch's total current
I_B	Current per wire bonding
I_{CE_S}	Collector-emitter cut-off current
I_{Clear}	Current produced during clear sky
I_{C_r}	IGBT's rated collector current
I_D	Drain current
I_{D_D}	Direct off-state current
I_{D_r}	MOSFET's rated drain current
I_{DS_S}	Drain leakage current
I_{f_M}	Diode's mean forward current
I_{GE_S}	IGBT's Gate leakage current
I_{GS_S}	MOSFET's gate leakage current
I_{GT}	Gate trigger current

I_m	Low current injected during TSEP measurement
I_{MAX}	Maximum value of an RMS current's profile
I_{R_D}	Direct reverse current
I_T	Transistor's current
J	Current density
L	Load inductance
λ_{th}	Thermal conductivity
m	PWM modulation depth
N	Number of temperature cycles
P	Power losses
$\hat{P}$	P power spectral density
P_{condD}	Diode's total average conduction losses
$P_{condD}Inv$	Diode's average conduction losses during MOSFET's conduction phase in the 3rd quadrant
$P_{condD}tm$	Diode's average conduction losses during dead time
P_{condT}	Transistor's average conduction losses
P_h	Power losses at thermal equilibrium
P_m	Power losses during TSEP measurement
P_{off}	Turn-off power losses
P_{off_l}	Turn-off power losses of low side transistor
P_{on}	Turn-on power losses
P_{on_l}	Turn-on power losses of low side transistor
P_{rec_h}	Reverse recovery losses of high side diode
P_{sw_D}	Diode's average switching losses
P_{sw_T}	Transistor's average switching losses
P_{tot_D}	Diode's total average power losses
P_{tot_T}	Transistor's total average power losses
r_d	Dynamic resistance
$R_{DS_{on}}$	Drain-source on-state resistance
R_g	Internal gate resistance
$R_{g_{on}}/R_{g_{off}}$	External gate resistances
R_{th}	Thermal resistance
$R_{th_{JC}}$	Junction-Case thermal resistance
σ	Electrical conductivity
t	Time
T	Temperature
T_a	Ambient Temperature
$\widehat{T_a}$	T_a power spectral density
T_amax	Maximum ambient temperature value
T_amin	Minimum ambient temperature value
T_C	Case temperature
T_h	High side transistor
T_H	Heat sink's temperature
τ_H	Heat sink's time constant
T_J	Junction temperature
$\widehat{T_J}$	T_J power spectral density
$T_{J_D}max$	Diode's maximum T_J on a fundamental period
$T_{J_D}min$	Diode's minimum T_J on a fundamental period
T_{J_h}	Junction temperature at thermal equilibrium
$T_{J_T}max$	Transistor's maximum T_J on a fundamental period

$T_{J_T}min$	Transistor's minimum T_J on a fundamental period
T_{J_m}	Instantaneous junction temperature estimated by measuring the TSEP
T_{J_M}	Mean junction temperature
$T_{J_{max}}$	T_J of the hottest power module
$T_{J_{MAX}}$	Maximum T_J given in a power module's datasheet
$T_{J_{min}}$	Cycle's minimal value
T_l	Low side transistor
t_m	Dead time
T_{off}	Power-off-time during power cycling
T_{on}	Power-on-time during power cycling
T_{out}	Fundamental period
t_p	Time delay between two consecutive ageing profiles
t_{rr}	Reverse recovery time
T_{sw}	Switching period
V	Electrical potential
V_{bus}	Voltage measured across the DC bus
V_C	Blocking voltage rating
V_{ce}	Collector-emitter voltage
$V_{ce_{sat}}$	Collector-emitter saturation voltage
$V_{ce_{th}}$	Collector-emitter threshold voltage
V_d	PWM delta-shaped voltage
$\widehat{V_d}$	Fundamental amplitude of the PWM delta-shaped voltage
V_{dr}	Driver's voltage
V_{DS}	Drain-source voltage
V_{DS_h}	Drain-source voltage measured across high side transistor
V_{DS_l}	Drain-source voltage measured across low side transistor
V_f	Diode's forward voltage
V_{ge}	Gate-emitter voltage
V_{GS}	Gate-source voltage
$V_{GS_{th}}$	Gate-source threshold voltage
V_{G_T}	Gate trigger voltage
V_{isol}	Isolation test voltage
V_L	Inverter's output AC voltage
$\widehat{V_L}$	Fundamental amplitude of the inverter's output AC voltage
V_{ref}	PWM Sinusoidal reference voltage
$\widehat{V_{ref}}$	Fundamental amplitude of the PWM sinusoidal reference voltage
V_{SD}	MOSFET's body diode forward voltage
Z_{ii}	Junction-Ambient self-heating thermal impedance of device D_i
Z_{ji}	Mutual thermal coupling impedance between devices D_j and D_i
Z_{th}	Thermal impedance
$Z_{th_{CH}}$	Case-Heat sink thermal impedance
$Z_{th_{JC}}$	Junction-Case thermal impedance
$Z_{th_{HA}}$	Heat sink-Ambient thermal impedance

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Introduction

The biggest challenge of the 21st century is finding effective alternative energy resources for fossil fuels, as well as trying to resolve the global warming issue by minimizing carbon gas emission. In this context, renewable energies are becoming primordial for a real energy transition, particularly solar energy, becoming recently one of the cheapest energy resources, with a spectacular growth rate of photovoltaic installations.

Therefore, the reliability of photovoltaic systems is primordial for an effective and low cost energy production, since the maintenance cost including the interventions as well as the replaced components is relatively high compared to the whole system price. In photovoltaic (PV) systems, the DC/AC inverter has the highest failure rate, and the anticipation of its breakdowns is still difficult [1]. Moreover, some field experiences reveal that PV inverters are responsible for more than one-third (37 %) of the unscheduled maintenance and more than a half (59%) of the associated cost during 5 years of operation of a 3.5 MW PV plant [1] [2] [3], as illustrated in Fig. 1. Furthermore, other studies of field's data from 600 PV systems (1500 PV inverters from 16 manufacturers) showed that more than 43 % of failure occurrences and more than 35% of energy losses are due to the inverter [4] [5], as demonstrated in Fig. 2.

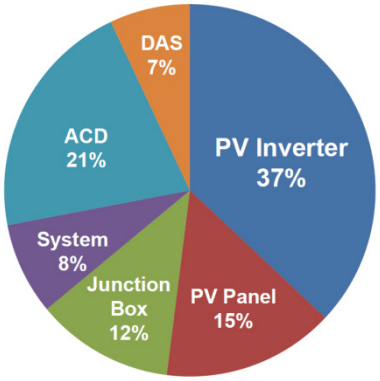


Fig. 1: Unscheduled maintenance events in PV system [2] [3]

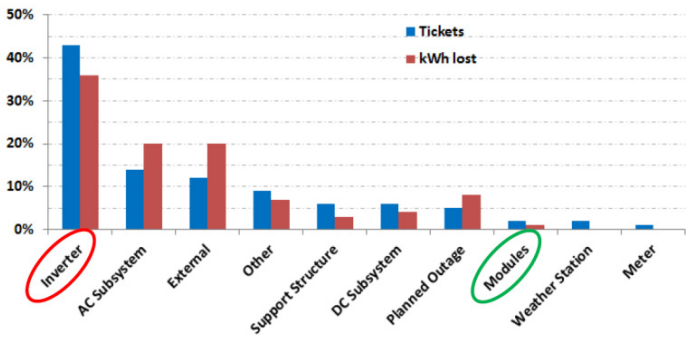


Fig. 2: Frequency (%) of failure occurrences and associated energy losses [4] [5]

Nowadays, the lifetime target of PV systems is around 20 years with PV panels' lifetime of 20 to 25 years. However, the expected lifetime of the PV inverter is only 5 to 10 years [1]. Thus, the improvement of PV inverter's reliability is a key factor for reducing the real cost of the PV system. Among different components of the PV inverter, the semiconductor devices are the most vulnerable parts [1] [6]. According to several recent evaluations, transistors contribute on average to 69% of the overall failure rate, diodes to 16%, capacitors to 14%, and magnetic elements to 1% [7]. Moreover, according to [8], and as shown in Fig. 3, power devices represent more than 30% of the total inverter's failures, followed by the capacitors with a failure rate of approximately 18%.

Failures of PV inverters can occur under non-intentional operations in islanding mode or under grid faults, or under normal operations due to several factors such as humidity, electrical overstress, temperature and severe users. The most observed factors among those latter are related to the temperature, including peak temperature and temperature swings [1] [8]. It can be seen in Fig. 4 that steady-state and cyclical temperature represent 55% of the stress sources [9].

However, it can be found in [6] and [7] that absolute temperature is not the dominant factor in the reliability performance, while thermal cycles contribute to a large percentage of the overall failure rate [3]. Hence, cyclic loads are more important than peak loads, especially that PV inverters often experience large temperature swings, due to variable solar irradiance and ambient temperature. In case of high temperature variations, failures are usually induced by the mismatch in the coefficients of thermal expansion of the different materials in the chip and package [7].

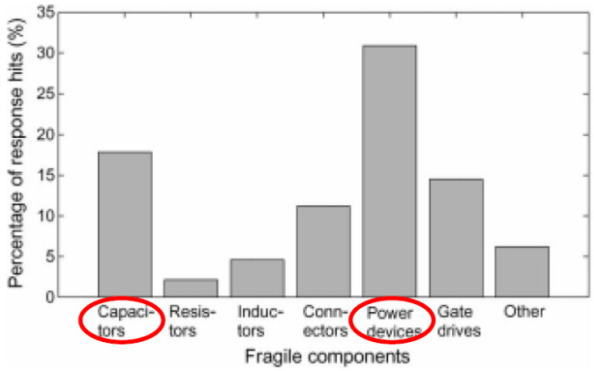


Fig. 3: Percentage of failure occurrences [4][10]

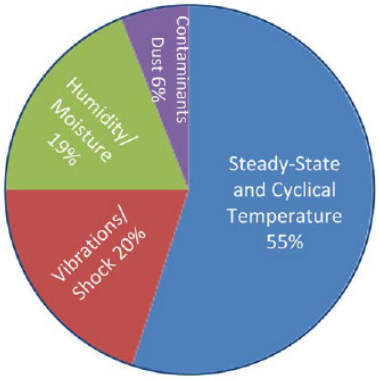


Fig. 4: Source of stress distribution [9] [11]

With power electronics increasingly used, features such as reliability, condition monitoring, lifetime estimation and predictive maintenance become increasingly important. The required lengthy lifespan for power devices and the reduction of the maintenance cost entail an assessment of their reliability and their main failure mechanisms and indicators, considering the field conditions. Condition monitoring has already proved to be cost-effective in different applications, yet for power semiconductor devices in power electronic inverters it is at a more embryonic stage and therefore needs more improvements.

Statistically speaking, nowadays the big majority of all the power electronic inverter systems are using Silicon (Si)-based power semiconductors, especially the Silicon Insulated Gate Bipolar Transistor (Si IGBT). Actually, silicon is an extremely mature technology with over half a century of research and one of the most studied materials. However, wide-bandgap semiconductor devices are being increasingly used in power electronic applications, such as Silicon Carbide Metal Oxide Semiconductor Field Effect Transistor (SiC MOSFET).

Indeed, SiC-based semiconductor devices comprise various advantages over Si-based devices. Having a wider bandgap limiting the extrinsic carrier concentration, SiC-based devices can operate at a higher temperature. Moreover, with a higher breakdown field that limits avalanche breakdown, they can withstand higher voltages (higher breakdown voltage). SiC-based devices have also higher electron saturation velocity and current density. They have lower on-state resistance, leading to lower conduction losses with the same voltage rating. Furthermore, they can switch faster than Si-based devices, with a low dielectric constant that limits the parasitic capacitance. This leads to lower switching losses, especially with high-frequency operations. Moreover, having a higher thermal conductivity which leads to a lower Junction-Case thermal impedance, heat is more easily conducted away from the device.

All these advantages lead to a much-reduced thermal management system, as well as to a reduction in the volume and weight of the inverter and filter. In turn, this leads to an improvement of the overall efficiency and/or the compactness of the inverter, as well as a

reduction of the heat sink and filter's costs. Fig. 5 represents a diagram illustrating relative magnitudes of five properties of SiC relatively to Si.

Presently, the most studied SiC-based devices are Junction Field Effect Transistor (JFET), Bipolar Junction Transistor (BJT) and MOSFET which is the most commonly used SiC-based device. Despite all of the promising advantages of this type of semiconductors, the number of interfacial charges trapped in the case of SiC MOSFET devices at and near the $SiC-SiO_2$ inversion channel-gate insulator's interface is much greater than in the case of Si. This can prompt a significant degradation in the device's reliability and performance by shifting the threshold voltage and substantially reducing the effective channel mobility due to coulombic scattering of the free carriers, which are themselves reduced by charge trapping.

However, with the big number of SiC-based devices' advantages over Si-based devices, it is probable that the majority of these latter will be replaced in the future with SiC-based devices. However, SiC technology remains new, with the first commercial MOSFET produced in 2011, thus further work should be done to study and improve the reliability of these promising devices. It should be noted that Gallium Nitrade (GaN) is another promising wide-bandgap material. However, GaN power devices have just begun to be offered commercially, while these solutions are still in their infancy (relatively low breakdown voltage) [12-20].

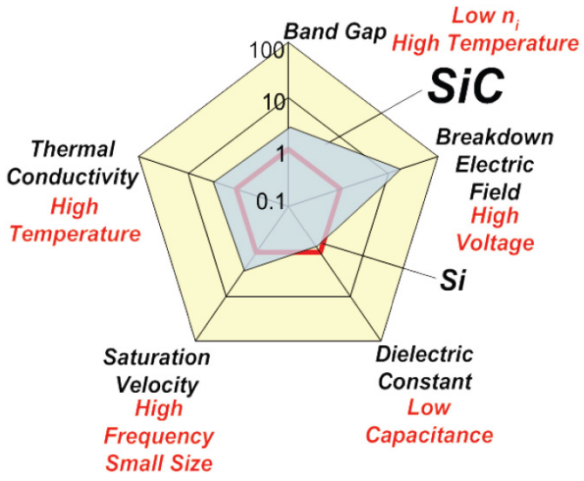


Fig. 5: Diagram illustrating relative magnitudes of five properties of SiC relatively to Si [13] [20]

Accordingly, this manuscript addresses the accelerated ageing of photovoltaic inverter's semiconductor devices, considering the thermo-mechanical constraints encountered in the field. The purpose is to determine a methodology for better representing the natural ageing process of the power modules in inverters than the traditional accelerated ageing. Actually, the existing reliability tests including Active Power Cycling (APC) and Passive Temperature Cycling (PTC) are not necessarily well adapted to photovoltaic applications. When applying these tests, mechanisms of failures that do not occur in the real application could be observed, and inversely other mechanisms that usually occur could not be recreated. Thus, these tests need better correlation with field conditions, as well as better consideration of the photovoltaic mission profiles.

The methodology that is proposed in the following chapters looks at the mission profiles of the current and ambient temperature, extracted over several years from several photovoltaic power plants. These profiles are used to study the dynamics of the photovoltaic current and ambient temperature as it will be represented in Chapter 4, in order to design an accelerated ageing current's profile. The purpose of this profile is to induce similar thermo-

mechanical constraints as those seen by semiconductor devices in a PV inverter, in an ageing test including APC and PTC simultaneously.

In order to estimate the junction temperature of the semiconductor devices corresponding to the mission profiles and to the accelerated ageing one, a numerical power losses estimation model (Chapter 2) and a numerical thermal model (Chapter 3) will be developed. These models are coupled in order to consider the electro-thermal coupling of temperature-dependent electrical parameters.

Accordingly, the designed accelerated ageing current profile will be applied in two test benches: one for studying SiC MOSFET power modules (Chapter 5) and another one dedicated to IGBT ones (Chapter 6).

Chapter 1:
State of art and proposed approach

Chapter 1: State of art and proposed approach

1.1. Introduction

This chapter discusses the state of art of the accelerated ageing methodologies of semiconductor power modules, of their main failure mechanisms, as well as of the main failure indicators and condition monitoring. Based on this review an approach will be proposed to follow throughout this study.

Initially, this chapter discusses the semiconductor power modules' main failure mechanisms, starting with the Si IGBT chip-related main failure mechanisms. Then, SiC MOSFET chip-related main failure mechanisms will be discussed, where the gate oxide problems as well as the instability of the gate-source threshold voltage will be detailed. Furthermore, packaging-related main failure mechanisms usually induced by power and/or thermal cycling will be depicted.

Afterwards, main accelerated ageing tests will be represented and discussed. After that, a review of active power cycling's state of art will be represented, where main control strategies will be discussed, as well as the common types of power cycling, classified mainly into DC current and Pulse Width Modulation PWM active power cycling (APC) tests. Eventually, a statistical review of the APC tests will be represented, including the APC tests type, the tested power modules' type and technology, as well as the control strategy and the encountered failure mechanisms.

Afterwards, a review of failure indicators and health monitoring in APC tests will be represented. It discusses the main failure electrical indicators, as well as their threshold value indicating the damage of the power modules. These indicators are related mainly to the voltages, the thermal resistance/impedance and the currents.

Eventually, the approach proposed in this PhD will be demonstrated and discussed with a brief description of each chapter's contents.

1.2. Semiconductor power modules' main failure mechanisms

Before discussing the main failure mechanisms of a semiconductor power module, its typical cross-sectional structure is described in the following section.

1.2.1. Semiconductor power module structure

The cross-sectional structure of a typical power module packaging is represented in Fig. 1.1. Its main constitutive elements are [21]:

- Power semiconductor chips (IGBT, MOSFET, diode…): they provide the current flow control function.
- Die-attach technology: it connects the die electrically, mechanically and thermally to the substrate.

• Interconnections (top-side): they provide electrical contacts on the device's top-side and sometimes top heat extraction.

• An electrically insulating and thermally conductive substrate: it is the mechanical support of the devices, tracks and terminals. It permits the electrical insulation between some of them, and provides an efficient heat extraction path.

• Substrate: it is the mechanical support of the tracks, terminals and devices, while providing heat extraction and electrical insulation.

• Encapsulating material: typically, it consists of a conformal coating or casting for mechanical as well as environmental protection.

• Base plate: it provides a mechanical support, and favors both the spreading and conduction of heat towards the heat sink.

• Case and cover: it is a housing structure that provides protection of the interconnections and devices.

Typical materials used in power modules' packaging are briefly described as follows:

• Semiconductor chips: mainly silicon-based, silicon carbide-based or gallium nitride-based chips.

• Substrate: Usually ceramic substrates are made of Al_2O_3, AlN, Si_3N_4 or BeO with copper layers on both sides. The Direct Copper Bonded DCB is the typical technology used in power modules.

• Base plate: based typically on nickel plated copper slabs. Other used materials are metal matrix composites such as aluminum matrix reinforced with SiC, copper matrix composites reinforced with diamond, carbon-reinforced composites, etc.

• Die-attach: usually PbSnAg alloy is used, however recently other lead-free alloys and new materials are being used such as silver nano-sintering.

• Interconnections (top-side): Large aluminum wire-bonding is the most used technology, while others include metal bumps and pressure-type contact.

• Case and cover: Thermoset and thermoplastic materials including epoxies and silicones [21].

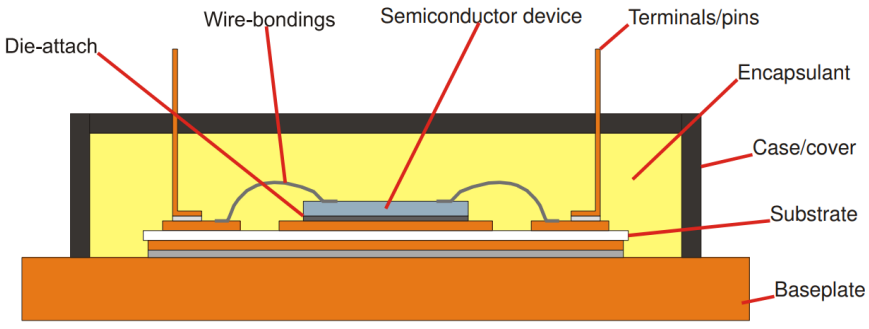


Fig. 1.1: Typical power electronics package structure [21]

The failure mechanisms of semiconductor power modules are mainly classified into packaging-related and chip-related mechanisms. These latter depend in most of cases on the semiconductor type whether it was Si IGBT or SiC MOSFET. Accordingly, the chip-related main failure mechanisms will be represented for Si IGBT and then for SiC MOFET in the

following sections. Afterwards, the packaging-related main failure mechanisms will be represented for both devices.

1.2.2. Chip-related main failure mechanisms

1.2.2.1. Si IGBT

IGBT chip-related failure mechanisms can be generally classified into wear-out failures and catastrophic/random failures. Wear-out failures are due to accumulation of incremental physical damage under the operating load conditions, such as passivation failure at the blocking junction, gate oxide breakdown, dielectric failure of the insulating material, etc. These failure mechanisms alter the device properties beyond the functional limits [22].

However, catastrophic/random failures can be caused by external accidental events such as voltage transients, particle radiation and damage by service actions, leading to momentary over-stress [22]. The chip-related catastrophic failure mechanisms in IGBT are mainly due to short-circuit. IGBT short-circuit failures can lead to potential destruction of the IGBT, as they induce uncontrolled high current through the circuit. Short-circuit failures can be classified mainly into high voltage breakdown, static/ dynamic latch-up, second breakdown and energy shocks.

A) Static/ dynamic latch-up

The IGBT has a parasitic intrinsic thyristor structure between the collector and the emitter (Fig. 1.2). When the parasitic thyristor is turned-on, the IGBT current cannot be controlled by the Metal Oxide Semiconductor (MOS) gate. Two modes of parasitic thyristor latch-up can occur in IGBTs: static and dynamic latch-up modes [23].

Static latch-up happens at high collector currents, which turn-on the parasitic NPN transistor by increasing the voltage drop across the parasitic resistance. However, dynamic latch-up happens during switching transients, usually during turn-off, when the parasitic NPN transistor is biased by the displacement current through junction capacitance C_{cb} between the deep P^+ region and the N^- base region. It is worth mentioning that latch-up is not a common failure anymore due to improvements in the IGBTs' structure [24].

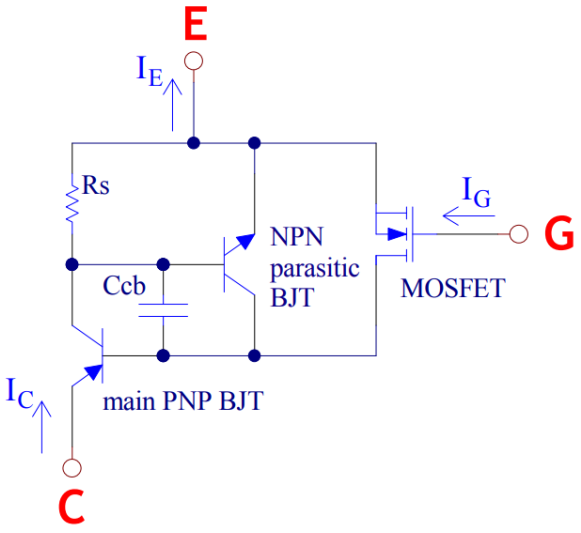


Fig. 1.2: Equivalent circuit of IGBT [24] [25]

B) High voltage breakdown

The IGBT can be destroyed during turn-off due to high voltage spikes induced by high falling rate of collector current and stray inductance. The high turn-off voltage spikes can break down one or a few IGBT cells first, and lead to a high leakage current as well as a high local temperature [24].

C) Second breakdown

Second breakdown is a kind of local thermal breakdown for transistors due to high current stresses. It can also happen to IGBTs during both turn-off and on-state [24].

D) Energy shocks

Energy shock is defined as a high power dissipation within a short time. The IGBT failure could happen due to high power dissipation during a short circuit at the on-state [24].

Moreover, the avalanche conduction mode is another failure mechanism that can occur in IGBTs. In the case of a static avalanche, the device is in the normal forward conduction mode, thus the voltage across the device is low while the current is high. In the case of dynamic latching both the voltage and current are high [26]. Dynamic avalanche can cause current imbalance between the cells of the IGBT, while it can be self-induced if the gate resistance is too low causing high gate currents.

More failure mechanisms can be found in the literature [27], such as gate oxide breakdown, etc. However, this mechanism is not predominant in Si IGBTs, in contrary to SiC MOSFET as it will be discussed in the following section.

1.2.2.2. SiC MOSFET

This section represents a review of the state of art of the SiC MOSFET chip-related main failure mechanisms [16-18] [28-30].

1.2.2.2.1. Gate threshold voltage $V_{GS_{th}}$ instability

The gate oxide is commonly known as the weakest part of the SiC MOSFET illustrated in Fig. 1.3, where a cross-sectional view of an N-channel MOSFET's elementary cell is represented. Considering the semiconductors and insulators' band diagrams shown in Fig. 1.4, it can be noticed that the tiny difference between the SiC-4H conduction band's energy and that of the SiO_2 is responsible for the gate's robustness defects. Actually, this tiny difference in energy levels facilitates the circulation of a tunnel current generating traps in the oxide and at the SiC / SiO_2 interface. Therefore, the improvement of the gate's manufacturing process is the current problem of the SiC MOSFET, however good progress has been made in terms of its reliability [28].

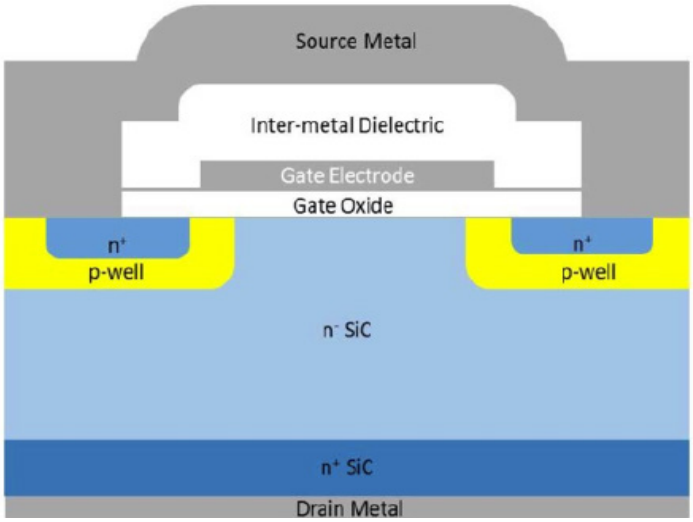


Fig. 1.3: Cross-sectional view of an N-channel MOSFET's elementary cell [31]

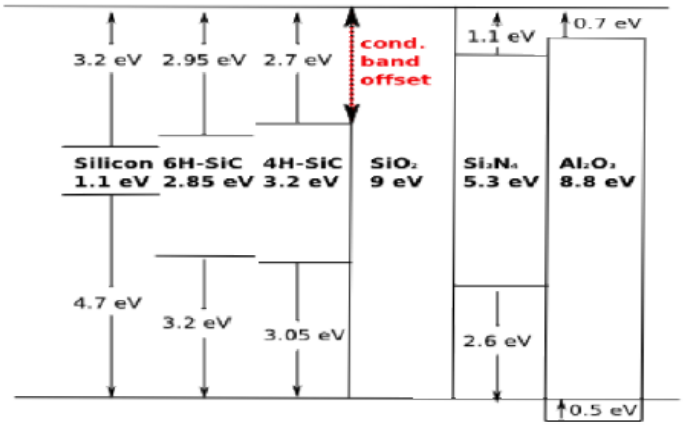


Fig. 1.4: Semiconductors and insulators' energy band diagrams [32]

Interface defects are related to impurities, structural or chemical defects in the oxide. They can significantly affect the electrical properties of the MOSFET with a shift in the threshold voltage, influencing the reliability of the components. There are three types of charges present in the oxide of a MOSFET's structure as illustrated in Fig. 1.5.

A) The mobile charges that are related to the oxidation process and ionic impurities such as Na+, K + and Li + ions. These charges may move in presence of an electric field, in particular between the gate and the source, causing a modification of the electrical characterizations.

B) The charges at the interface (negative or positive) are carriers moving from the semiconductor and trapped in the interface. It is possible to charge or discharge them depending on the applied polarization.

C) Trapped oxide charges (negative or positive) are carriers trapped due to impurities, radiation damages or hot carriers in the oxide. It is important to separate the notions of quantity of traps in the oxide and the charges trapped in the oxide. Actually, the amount of traps is related to the quality of the oxide, if the number of traps increases with an ageing phenomenon, this degradation is irreversible.

The trapped charges will be located in these impurities under the effect of a current, an electric field or heat. These charges can be released by inversing the electric field or applying thermal energy. In other words, the traps presented in the oxide can receive negative charges (electrons) or positive ones (holes). The amount of trapped charges influences the measured electrical parameters, however it is possible to reobtain the initial properties by releasing these charges. This phenomenon is reversible and these traps create a hysteresis on the I_D-V_{GS} measurement.

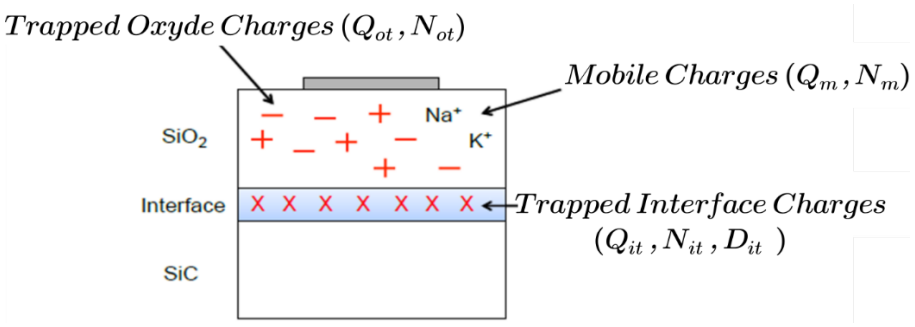


Fig. 1.5: Three types of load and their location in a MOSFET (adapted from [28] and [33])

Actually, when $V_{GS} > 0$, negative charges move from the semiconductor and are trapped by tunnel effect in the oxide or at the interface, as represented in Fig. 1.6. Inversely, when $V_{GS} < 0$, negative charges are liberated by tunnel effect from the oxide or the interface, as represented in Fig. 1.7 [28]. The SiC MOSFET threshold instability is frequently studied in the recent literature [16-18] [28-30].

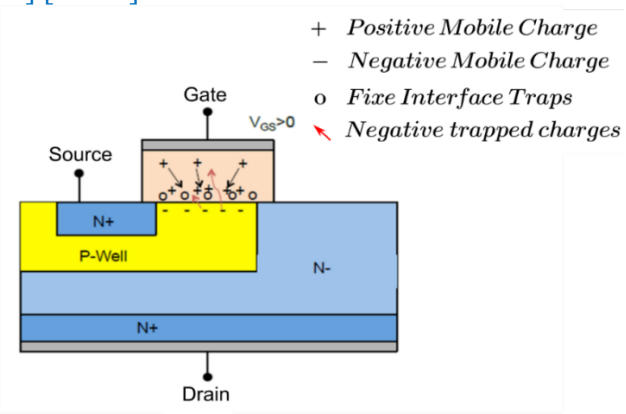


Fig. 1.6: Diagram of the charges in the MOSFET when a positive gate-source voltage is applied (adapted from [28])

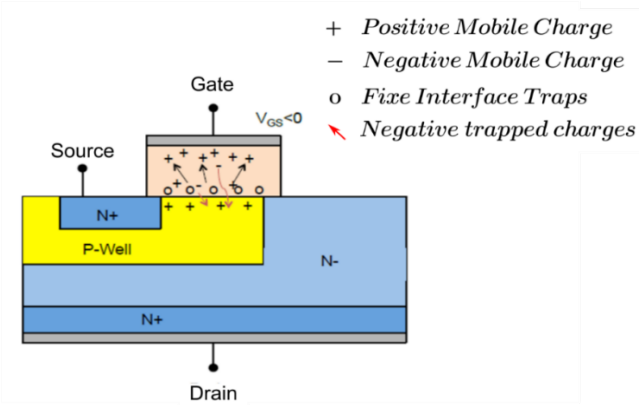


Fig. 1.7: Diagram of the charges in the MOSFET when a negative gate-source voltage is applied (adapted from [28])

1.2.2.2.2. Gate oxide cracks and breakdown

The high switching frequency of the gate-source voltage V_{GS} can lead to the gate oxide cracking and breakdown at high temperature levels. Fig. 1.8 shows a Scanning Electron Microscopy (SEM) image of the FIB cutout where the gate's fault can be seen, while Fig. 1.9 shows an SEM image of the gate's cracks. These cracks are located at the gate oxide's metallization. Usually, this fault is detectable by a significant increase in the gate's leakage current.

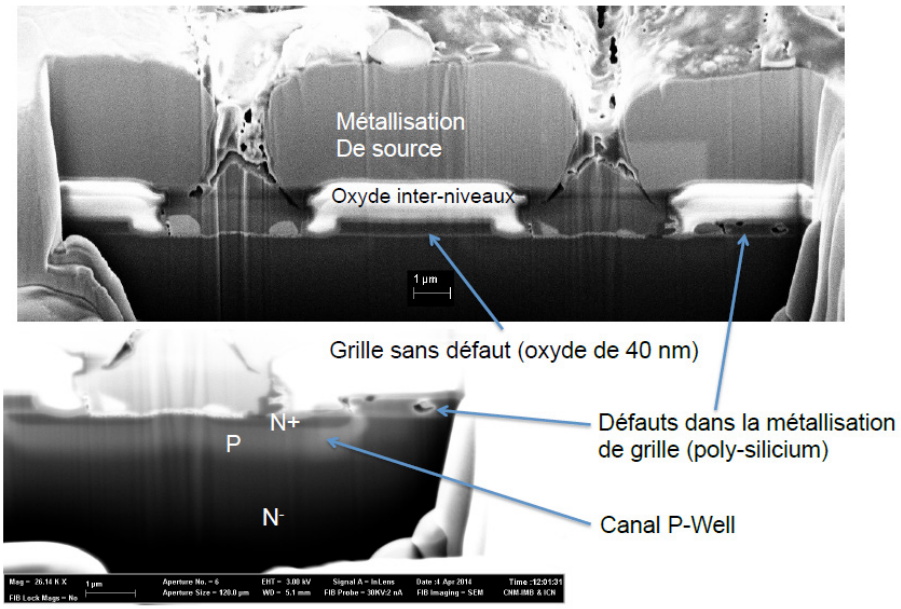


Fig. 1.8: SEM image of the FIB cutout where the gate's fault can be seen [28]

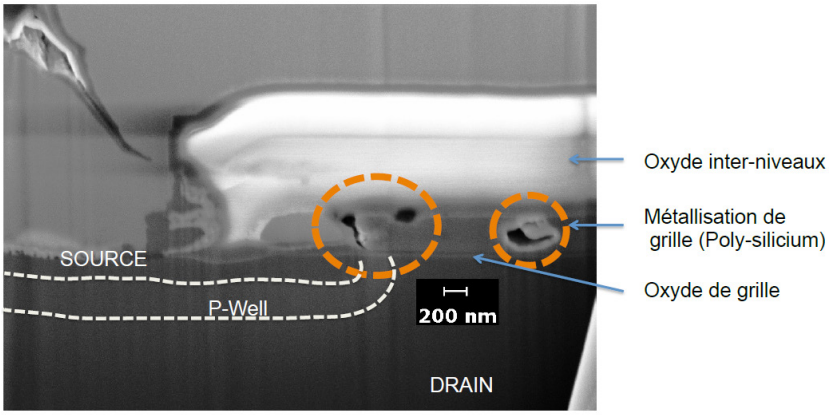


Fig. 1.9: SEM image of the gate's cracks [28]

1.2.2.2.3. Single-event-gate-rupture (SEGR)

SEGR is another failure mechanism of oxide breakdown of SiC MOSFET. Usually, the natural space contains heavy ions and high-energy protons. When a heavy ion penetrates the gate region of N-channel SiC power MOSFET while the drain is under positive bias, the electron-hole pairs generated along the path of the ion start to separate as shown in Fig. 1.10. This charge separation leads to the accumulation of a positive charge in the silicon at the Si-SiO_2 interface. A transient electric field increases upon the gate oxide results from this charge

build up. The oxide breakdown occurs resulting in a permanent short circuit through the oxide if the critical oxide breakdown's electric field E_{cr} is exceeded [23].

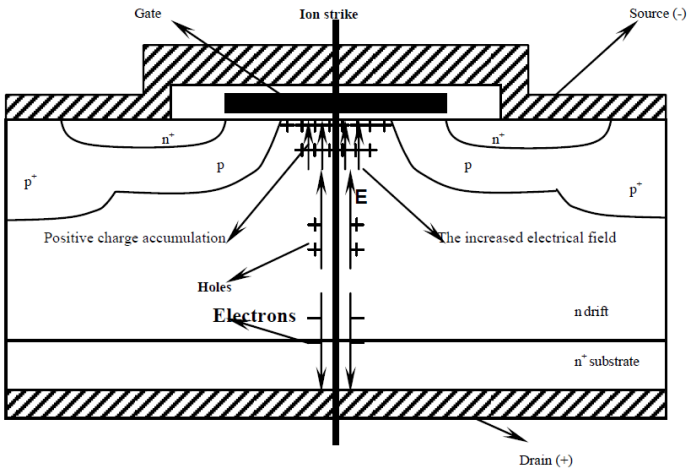


Fig. 1.10: SEGR of SiC MOSFET [23]

1.2.2.2.4. Activation of parasitic bipolar junction transistor (BJT) in SiC power MOSFET

The inherent parasitic structure in power MOSFET includes a parasitic bipolar junction transistor BJT and a parasitic diode as represented in Fig. 1.11.

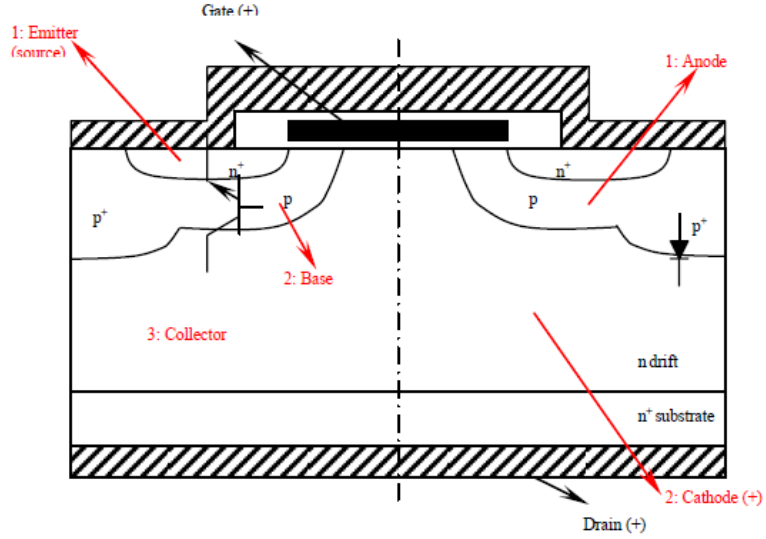


Fig. 1.11: Parasitic NPN transistor and diode inherent to DMOS [23]

Given that the base-emitter junction is shorted together, the BJT is normally inactive. Despite that the base-emitter junction is shorted externally, the BJT can still be turned-on under certain circumstances. This may lead to losing the gate control of the MOSFET and results in failure of the device. Usually, two types of mechanisms can activate the parasitic BJT in power MOSFETs.

The first mechanism is triggered when the power MOSFET is turned-off, where the very high dV/dt or dI/dt can activate the parasitic BJT, reducing the MOSFET's breakdown voltage. Consequently, the device can fall into an avalanche breakdown if the drain-source voltage V_{DS} is larger than the new breakdown voltage. Accordingly, the device can be

thermally destroyed if no external limitation exists for the avalanche current. Fig. 1.12 illustrates the equivalent circuit for an N-channel power MOSFET [23].

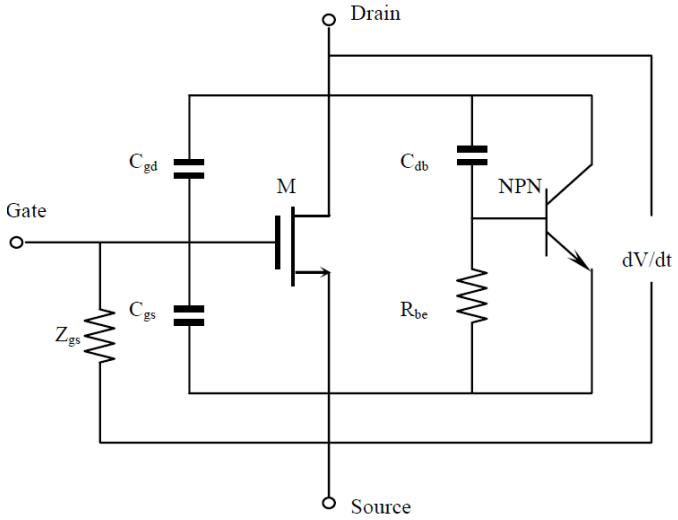


Fig. 1.12: Equivalent circuit of a power MOSFET [23]

When the parasitic BJT latches, thermal runaway destroys the MOSFET as illustrated in Fig. 1.13. The IGBT is significantly less rugged than the SiC MOSFET, given that the IGBT does not contain internal body diode. However, as demonstrated previously, the IGBT has a parasitic thyristor, thus it is not considered avalanche capable. The avalanche ruggedness capability of IGBTs significantly reduces with temperature [34].

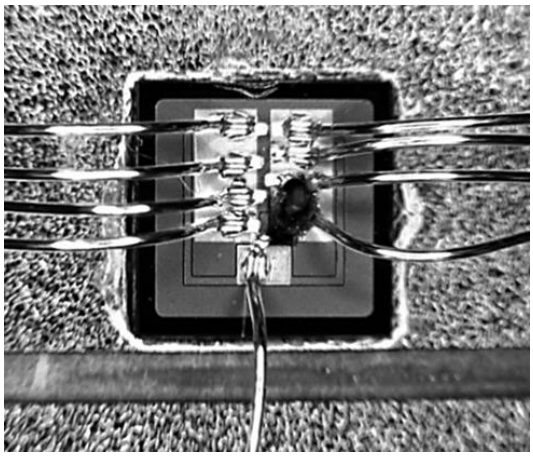


Fig. 1.13: Destroyed MOSFET due to activation of the parasitic BJT [34]

1.2.2.2.5. Single-event-burnout (SEB)

When SiC power MOSFET is used in a high radiation environment, the parasitic BJT can be turned-on if a heavy ion strikes on the MOSFET. Cosmic radiation constantly showers our earth with highly energetic particles, mainly protons and nuclei of $10^9 - 10^{17}\ eV$. Secondary particles with energies up to 1 GeV reach sea level via collisions with air molecules [30] [35].

Being relevant at ground level, this effect gains even more importance for power electronics used at high altitudes (e.g. in airplanes, since the particle density in 13 km altitude is about 300 times higher than at sea level). However, the higher melting temperature, the much higher breakdown electric field and the wider band gap compared to Si may lead to the

assumption that SiC-based devices have superior radiation hardness than Si-based devices [30].

Similarly to SEGR, SEB can be also initiated with a heavy ion strike through a SiC power MOSFET, biased in off-state. Electron-hole pairs are generated along the track length of a heavy ion traversing the MOSFET, and create transient currents in which holes flow up towards source via the lateral base region and electrons toward drain. A voltage drop in the base-emitter junction is generated by the current leaking through the P-base region as shown in Fig. 1.14. The MOSFET's inherent parasitic BJT will be turned-on when the voltage drop is larger than a threshold value. High voltage and current will occur in the device channel and trigger the second breakdown of the device and destroy the MOSFET, due to a regenerative feedback mechanism [23]. Although being depicted only in the case of SiC MOSFETs, it is worth mentioning that SEB can occur also in Si IGBTs.

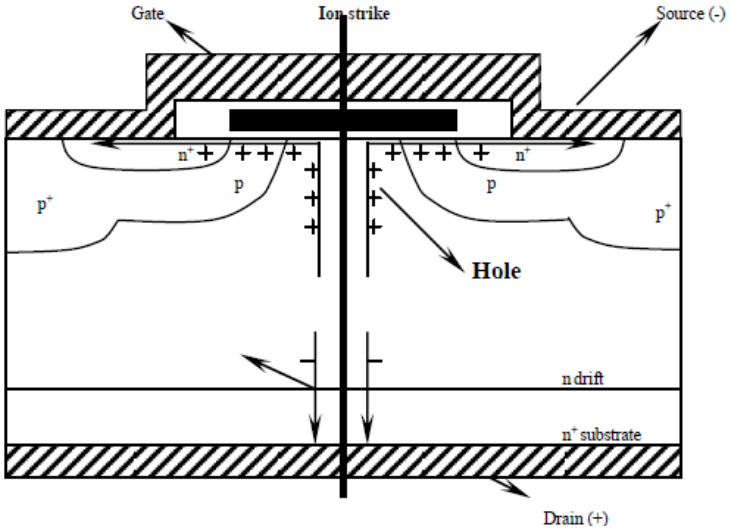


Fig. 1.14: SEB of MOSFET [23]

1.2.2.2.6. Parasitic diode avalanche breakdown

Avalanche breakdown can happen in the power MOSFET's parasitic diode. As shown in Fig. 1.11 the parasitic diode is formed between the source and drain of the device. The drain forms the cathode while the source forms the anode. A brutal increase of the drain-source voltage V_{DS} may lead to an avalanche breakdown in the parasitic diode, given that it is always under reverse biased [23].

1.2.2.2.7. Body diode switching failure

When the body diode conducts in forward mode there is considerable charge storage in the MOSFET drift region. As the diode is turned-off, the turn-off dV/dt combined with the drain-to-body capacitance causes a current to flow. If the capacitor's discharge current and the reverse recovery current are large enough to forward bias the parasitic BJT, then the device can latch with destructive consequences.

The rate at which the body diode of the MOSFET is switched will determine the peak reverse recovery current. The reverse recovery characteristics of the MOSFET body diodes have a significant impact on the device voltage overshoot. Actually, voltage overshoots as high as 2.5 kV can occur with a DC-link voltage of just 800 V. Fig. 1.15 represents a failed SiC MOSFET power module due to body diode switching failure [34].

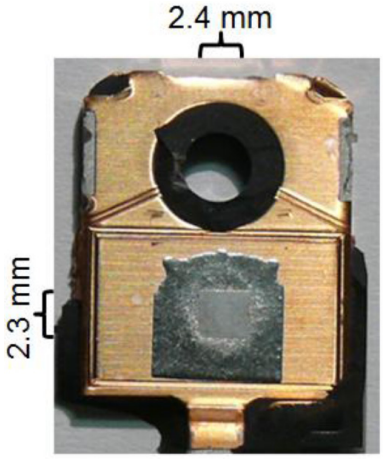


Fig. 1.15: Failed SiC MOSFET power module due to body diode switching failure [34]

1.2.3. Packaging-related main failure mechanisms

This section presents a study of the state of art of the packaging-related main failure mechanisms, usually induced by power and/or thermal cycling [12] [36-43]. About 65% of failures occurring in power modules are due to thermo-mechanical phenomena [4] [12] [27], which represent the primordial cause of packaging-related failures.

1.2.3.1. Bond wire fatigue

The repeated flexure of the bond wire or the shear stresses generated between the bond pad and the bond wire are the main causes for bond wire fatigue, considered as one of the most commonly observed packaging related failures mechanisms. It is actually caused by temperature cycling during operation [1].

The failure of bond wires leads to a change either in the internal distribution of the current or in the contact resistance, such that it can be traced by monitoring $V_{ce_{sat}}$. Two types of bond wire fatigue exist:

- Bond wire lift off
- Bond wire heel crack

1.2.3.1.1. Bond wire lift off [12] [21] [34] [36] [38] [40] [41] [43]

The bond wire lift off failure is caused by the CTEs (Coefficients of Thermal Expansion) mismatch between the aluminum wire (23.5 ppm/K) and the Si/SiC chip (2.8 ppm/K for Si). This difference leads to the destruction of the interface and to the wire lift off, due to plastic strain accumulated in the bond wire. The crack propagates towards the bond's center within the wire's material. It is initiated from either end of the interconnected area [12]. The following figures illustrate examples of bond wire lift off, with Fig. 1.16 representing an optical image, whereas Fig. 1.17 shows a Scanning Electron Microscopy (SEM) image of a lifted off bond wire.

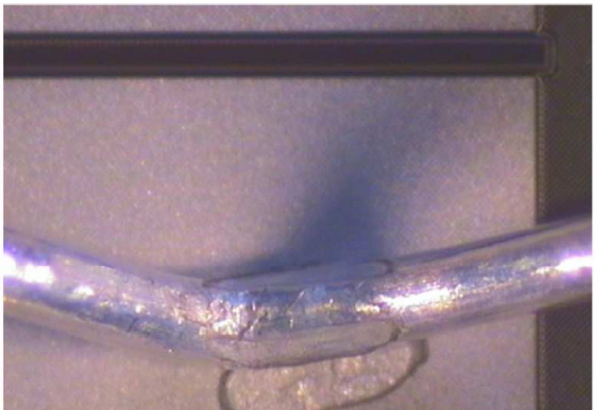


Fig. 1.16: Bond wire lift off (optical image) [37]

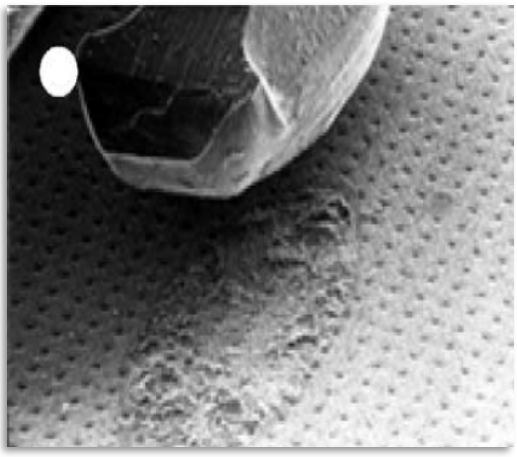


Fig. 1.17: Bond wire lift off (SEM image, x40) [39]

1.2.3.1.2. Bond wire heel crack [12] [37] [38] [41] [43]

Bond wire heel cracking is usually encountered after long endurance tests of temperature cycles, where the bond wire expands and contracts, undergoing flexure fatigue. Actually cyclic plastic strain is generated by repetitive heel bending, leading to accumulated deformations and a crack propagating until the complete wire failure [12] [44]. Fig. 1.18 illustrates a visualization of degradation effects inside the Device Under Test (DUT) by means of a Scanning Electron Microscope (SEM).

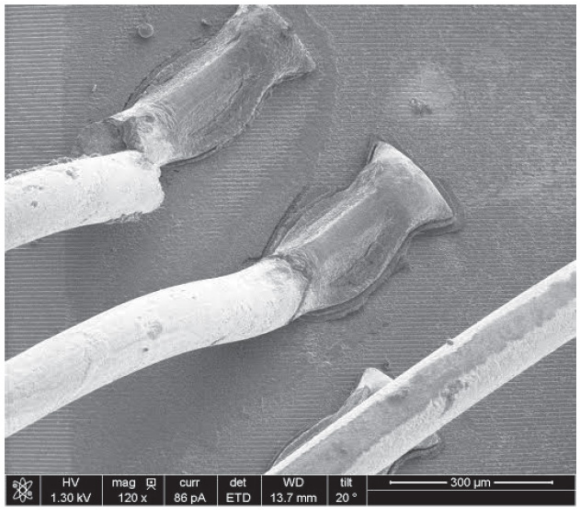
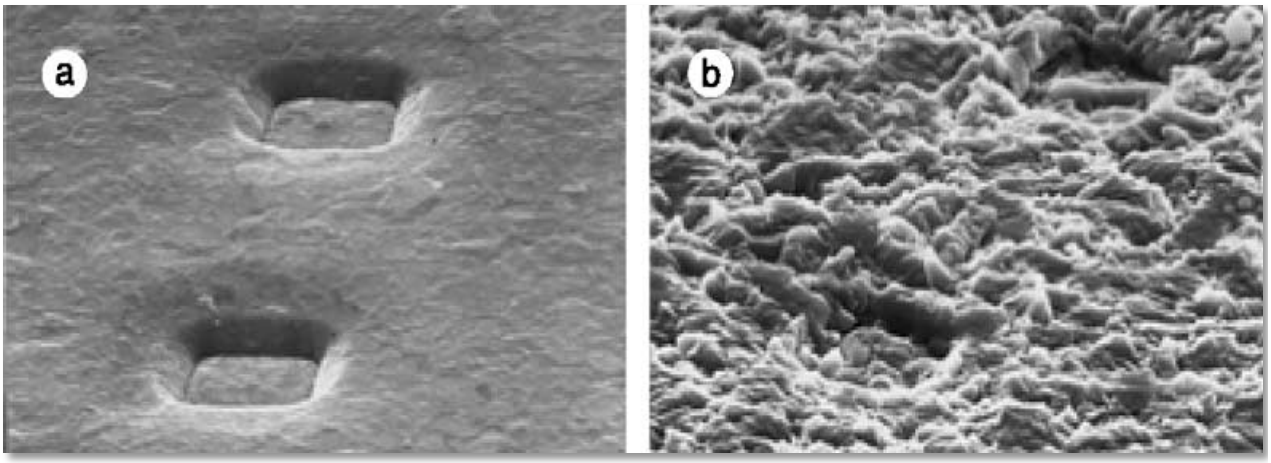


Fig. 1.18: Visualization of degradation effects inside the DUT by means of a Scanning Electron Microscope (SEM) [45]

1.2.3.2. Aluminum metallization reconstruction [12] [39] [41] [43]

The thin film of alloyed aluminum deposited onto the silicon substrate is called aluminum metallization. It forms a bondable metal layer, used to establish electrical connections with the chip and with other chips via bond wires. The aluminum metallization reconstruction is one of the most common failure mechanisms encountered in power modules [12].

Periodical compressive and tensile stresses are introduced in the metallization film by the different CTEs of the Si/SiC chip and the aluminum, during thermal cycling of semiconductor devices. Depending on temperature and stress conditions, the stress relaxation can occur mainly by diffusion creep, grain boundary sliding, or by plastic deformation through dislocation glide. During power cycling tests, this mechanism linearly increases V_{ce} as a function of the cycles' number [39]. Fig. 1.19.a represents an SEM image of the emitter metallization of an IGBT chip before power cycling, whereas Fig. 1.19.b represents the same SEM image after 3.2 millions of power cycles between 85 °C and 125 °C, where the reconstructed emitter metallization can be seen.



a) Emitter metallization of an IGBT chip before power cycling (SEM image, 1000)

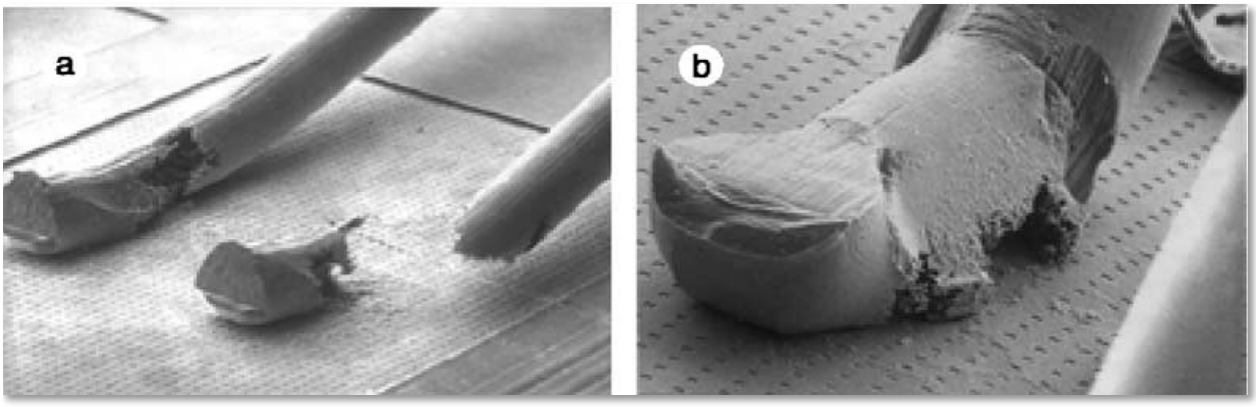
b) Reconstructed emitter metallization after 3.2 millions of power cycles between 85 °C and 125 °C (SEM image, 1000)

Fig. 1.19: Aluminum metallization reconstruction [39]

1.2.3.3. Corrosion of interconnections

Corrosion of aluminum as in Al bond wire is a well-known failure mechanism. When pure aluminum is exposed to an oxygen O_2 containing atmosphere, a thin native Al_2O_3 surface layer is grown passivating the metal.

The corrosion can occur with the local formation of gaseous inclusions within the silicone gel, sometimes noticed during high-temperature operation of power modules. The corrosion of the bond wire is strongly correlated with mechanical stresses, arising due to residual deformation stresses in the bond, or due to thermo-mechanical cycling [39]. Fig. 1.20.a illustrates an SEM image of an emitter bond wire's rupture due to stress corrosion, whereas Fig. 1.20.b demonstrates a detail of a corroded emitter bond wire.



a) Rupture of emitter bond wires due to stress corrosion (SEM image, 30) **b) Detail of a corroded emitter bond wire (SEM image, 80)**

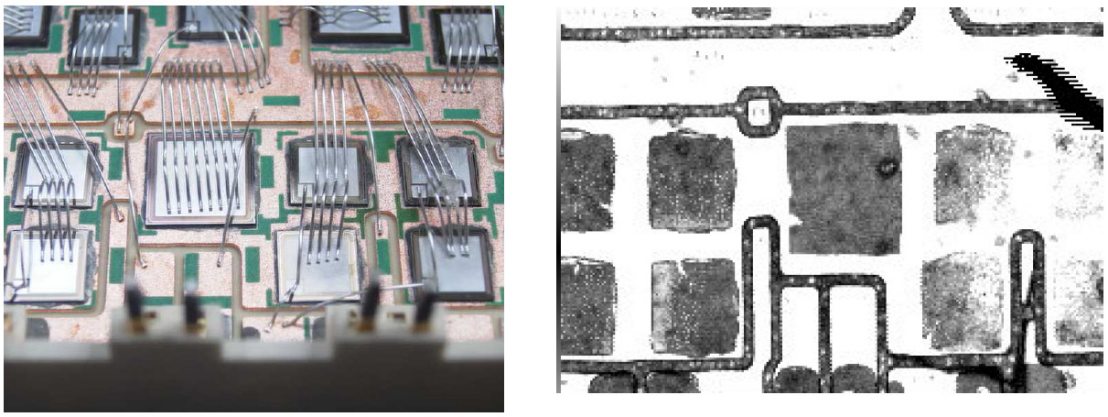
Fig. 1.20: Example of bond wire corrosion [39]

1.2.3.4. Solder fatigue [12] [21] [37] [38] [39] [40] [41] [42] [43]

Solder fatigue can be mainly categorized into solder fatigue in chip soldering and on the base plate.

1.2.3.4.1. Solder fatigue in chip soldering

Solder fatigue in chips primordially appears together with bond wires' damage. The higher the temperature of the whole module gets, the more the solder connection is strained. Actually, solder fatigue leads the thermal resistance R_{th} and the junction temperature T_J to increase, causing in their turn higher power losses and hence higher temperature variations ΔT_J in the power module, accelerating the ageing process. Fig. 1.21 represents an example of solder delamination under 4 IGBT chips due to power cycling. The 4 parallel jointly current-carrying IGBT have their hottest spot in the center, where the delamination starts at the inner corners [38].



a) Optical image of IGBT chips before cycling **b) Scanning Acoustic Microscopy (SAM) image of IGBT chips' solder after cycling**

Fig. 1.21: Chip solder fatigue caused by power cycling test [38]

1.2.3.4.2. Solder fatigue on the base plate

The most critical interface is represented, especially in the case of copper base plates, by the solder between the base plate and the ceramic substrate. With the worst mismatch in the CTEs, the maximum temperature swing combined with the largest lateral dimensions can be found at this interface [21] [40], with the solder connection starting to crack at the corners [37]. The thermal resistance of the semiconductor device will increase during power cycling, due to the delamination of the solder [43]. Fig. 1.22 represents an optical image of a 34 mm IGBT module representing solder fatigue at light-colored areas, whereas Fig. 1.23 represents an SAM image of an AlN-module with copper baseplate after thermal cycling (16,000 cycles of $\Delta Tc = 50\ K$).

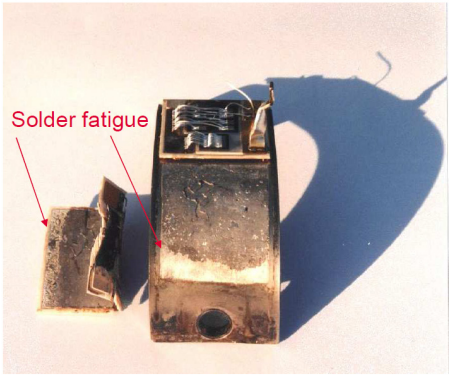


Fig. 1.22: 34 mm module with torn off DBC (light-colored areas show solder fatigue) [37] [46]

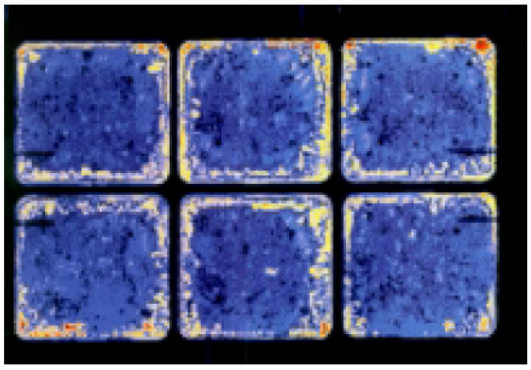


Fig. 1.23: AlN-module with copper baseplate after 16,000 cycles ($\Delta Tc = 50\ K$) [37] [46]

Furthermore, during the joining process an empty volume (named void) can be formed in the solder layer. It floats to the top of the drop and forms scum and bubbles when the solder melts and releases oxides [12].

Gross voids can have a harmful effect on dissipating power modules. Actually, they can significantly increase the peak junction temperature of the semiconductor device and hence accelerate the evolution of several failure mechanisms such as solder fatigue and bond wire lift off [39]. Fig. 1.24 illustrates an X-ray microscopy image of an IGBT module showing a large void immediately below three IGBT chips located in the die-attach layer.

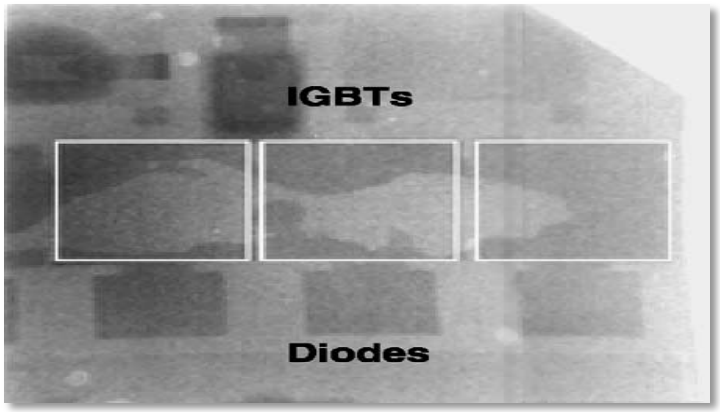
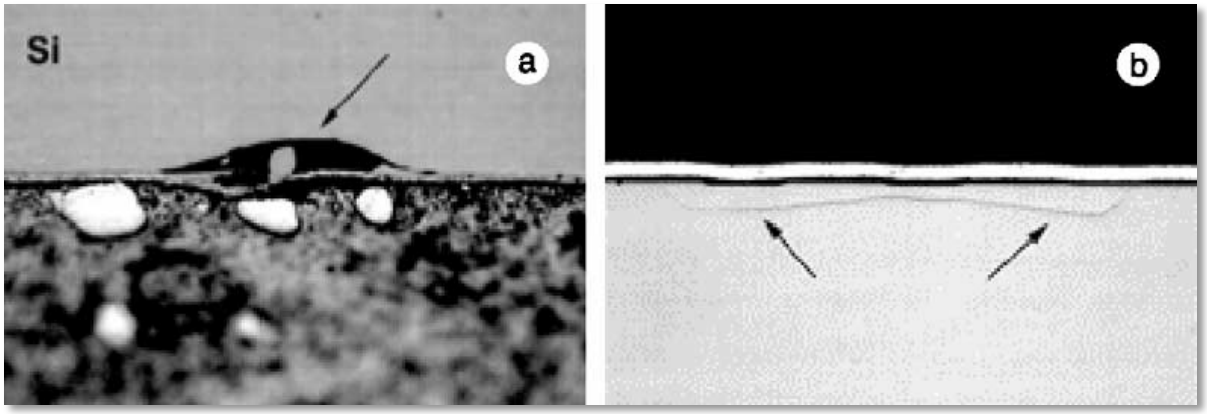


Fig. 1.24: X-ray microscopy image of an IGBT module showing a large void immediately below three IGBT chips (0.8) [39]

1.2.3.5. Brittle cracking [12] [39] [43]

The brittle materials used in power modules are the ceramic substrate, the single crystal silicon and the thin insulating layers on it. One among the main assumptions in fracture mechanics of brittle materials is that the rupture under the influence of external mechanical stresses is led by sharp stress concentration at pre-existing damages. Without any plastic deformation, ultimate brittle fracture can occur suddenly when an initial crack is present whose length exceeds a critical size, specific to every brittle material.

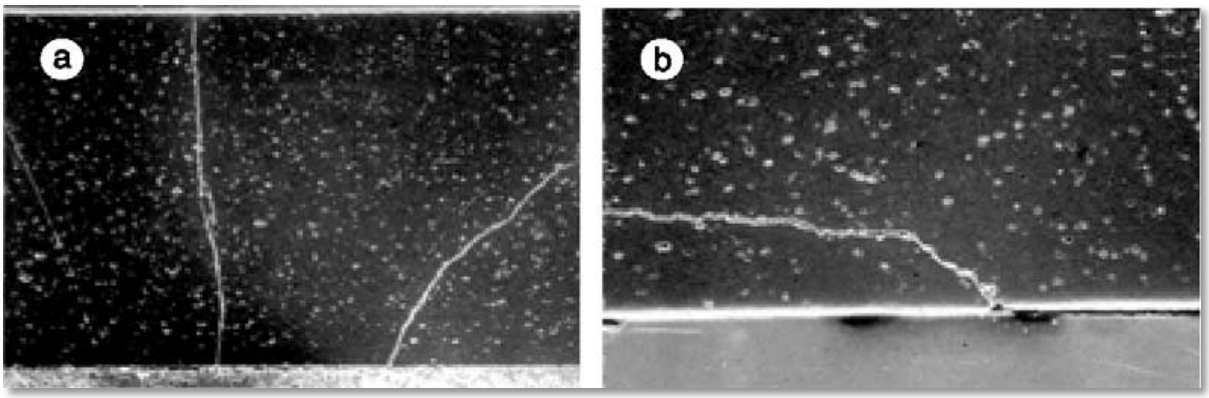
Actually, pre-existing defects can be originated for example by processing problems (e.g. during dicing), by assembly problems (e.g. hard wire bonding), or by soldering (e.g. voids in solder alloys) [12] [39] [43]. Fig. 1.25.a represents an optical image of silicon chip brittle cracking, where a notch in the silicon chip formed during diamond sawing of the silicon wafer can be seen. Fig. 1.25.b illustrates an optical image of a crack in the silicon chip due to bending stresses in the base plate. Fig. 1.26.a represents an SEM image of a vertical crack within an Al_2O_3 ceramic substrate, due bending stresses, while Fig. 1.26.b illustrates an SEM image of a crack within an Al_2O_3 ceramic substrate initiated from an inhomogeneity in the solder layer.



a) Notch in the silicon chip formed during diamond sawing of the silicon wafer (micro-section, optical image, 250)

b) Crack in the silicon chip due to bending stresses in the base plate (micro-section, optical image, 300)

Fig. 1.25: Example of silicon chip brittle cracking [39]



a) Vertical crack within an Al_2O_3 ceramic substrate, due bending stresses (micro-section, SEM image, 400)

b) Crack within an Al_2O_3 ceramic substrate initiated from inhomogeneity in the solder layer (micro-section, SEM image, 600)

Fig. 1.26: Example of substrate brittle cracking [39]

In order to understand these failure mechanisms, to determine the correspondent indicators of their occurrence as well as to estimate the lifetime of power modules etc., various accelerated ageing tests are being applied to semiconductor devices. The following section represents the main accelerated ageing tests used to evaluate the power modules reliability.

1.3. Main accelerated ageing tests

1.3.1. Reliability tests categories

Reliability testing can be categorized into capability, durability and technological-specific testing, described in [37] as follows:

A) Capability Testing: It confirms the ability of the product to withstand specific stresses, hence verifying that the product is capable for such stress factors which are not related to any life time or durability factors. Some examples are: flammability testing, water/dust protection, electrical testing (over voltage, reverse polarity) and drop test [37].

B) Technology-Specific testing: It activates specific failure modes by applying specific highly accelerated test conditions. It is quite suitable to assess new product and process technologies regarding these specific failure modes in a short time. The technology specific tests are based on the Mission Profile and the Knowledge Matrix, and should be performed as soon as possible in the prototype phase. Some examples are: high and low steady DC voltage and current levels, transient voltages and currents, high and low steady state temperature operation, thermal cycles and shock, humidity, mechanical random vibration, sine vibration, and shocks, exposure to environmental pollutants and customer usage cycles (Mission Profiles) [37].

C) Durability testing: It assesses how long the product is able to perform to specification when subjected to various stress factors. Durability tests can be performed using either a test-to-failure or a "success run" approach against specified end-of-test criteria. To make such durability tests possible within a reasonable time frame, the stress factors can be set at accelerated stress levels which are based on mathematical models. Some examples are: high temperature durability testing, power thermal cycling testing and mechanical endurance test [37].

The objectives of reliability tests are [37]:

- Ensuring general product quality and reliability

- Establishing the limits of systems by exposing them to various test conditions

- Ensuring process stability and reproducibility of production processes

- Evaluating the impact of product and process changes on reliability

1.3.2. AEC-Q101 and IEC 62093 Ed.2 stress based qualification tests

Many stress based qualification tests exist in different application fields, like MIL STP for aeronautic applications, ESA for aerospace applications and AEC-Q101 for automotive applications. This latter is a group of failure mechanism based stress tests qualification, used

originally for discrete semiconductors in automotive applications. It includes High Temperature Reverse Bias, High Temperature Gate Bias, Temperature Cycling, Intermittent Operational Life, Power and Temperature Cycle and Autoclave tests. Furthermore, it includes High Humidity High Temp. Reverse Bias Highly Accelerated Stress Test, Vibration, Mechanical Shock, Thermal, Thermo-mechanical and Humidity tests [47].

Moreover, IEC 62093 Ed.2 is a reliability tests standard used for PV inverters. It includes the following tests: Highly Accelerated Life Test (HALT), Damp Heat (DH), Humidity Freeze (HF), High Temperature Operating Bias (HTOB), Thermal Cycle (TC), Salt Mist and UV. However, these tests do not quantify lifetime of a product, nor address all possible failure modes in all possible climates and system designs, neither identify wear-out mechanisms at the end of a products lifetime. These tests need better correlation with field conditions, and better consideration of the photovoltaic mission profiles [4] [48].

1.3.3. SiC MOSFET $V_{GS_{th}}$ instability testing

Recently commercialized, SiC MOSFET has quickly gained much interest due to its various advantages over Si IGBT. Accordingly, reliability testing is being increasingly applied on the MOSFET, in order to study its gate threshold voltage instability, as it will be demonstrated in this section.

1.3.3.1. Static gate oxide ageing test applying high temperature steps

In [28], the DUT is a discrete SiC MOSFET power module (CMF20120D - 1200V - 42A), where the drain-source voltage $V_{DS} = 540\,V$ and the case temperature T_C alternates between 50 °C and 250 °C. During the first test, the gate-source voltage $V_{GS} = +20V$, whereas during the second one $V_{GS} = -5V$. Fig. 1.27 illustrates the derivation of the normalized threshold voltage for a positive and negative gate voltage. It can be concluded that $V_{GS_{th}}$ increases when a positive V_{GS} is applied (first test), whereas it decreases when a negative V_{GS} is applied (second test), thus it depends on the polarity of the applied gate-source voltage.

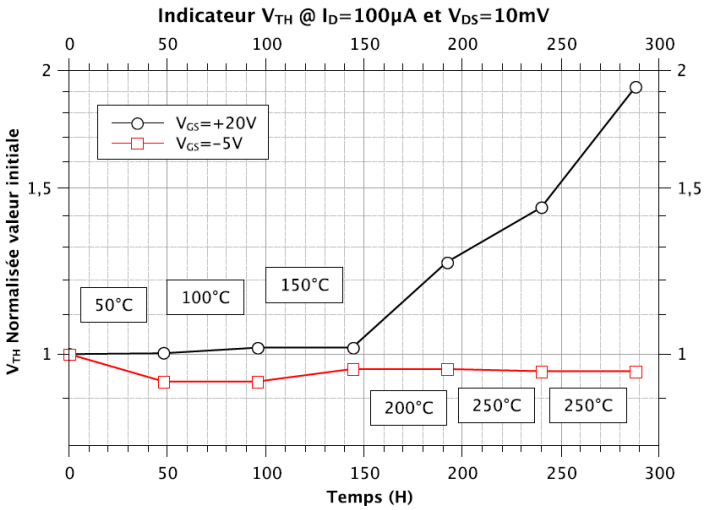


Fig. 1.27: Derivation of the normalized threshold voltage for a positive and negative oxide gate voltage [28]

1.3.3.2. HTGB test with increasing stress time

HTGB or High Temperature Gate Bias, also known as Bias Temperature Instability BTI was applied in numerous studies [16-18] [29] [30]. Fig. 1.28 illustrates the HTGB test configuration, representing the gate voltage as a function of time. In [28] the HTGB test was applied for V_{GS} alternating between -5 V and +20 V at an ambient temperature of 175 °C and 250 °C with an incrementing stress time. The gate's stress time increments as follows: 10s, 36s, 100s, 360s, 1000s, 3600s, 10000s and 36000s.

The test's results are represented in Fig. 1.29, where the gate-source threshold voltage is plotted as a function of incrementing stress time. Each measurement is taken at the end of the stress time, directly before switching V_{GS}. Accordingly, the measurements corresponding to $V_{GS} = +20\,V$ are plotted together, separately from the measurements corresponding to $V_{GS} = -5\,V$ which are plotted similarly. It can be seen that as discussed in Section 1.2.2.2.1, the threshold voltage increases with temperature when applying a positive V_{GS}, while decreases with temperature when applying a negative V_{GS}.

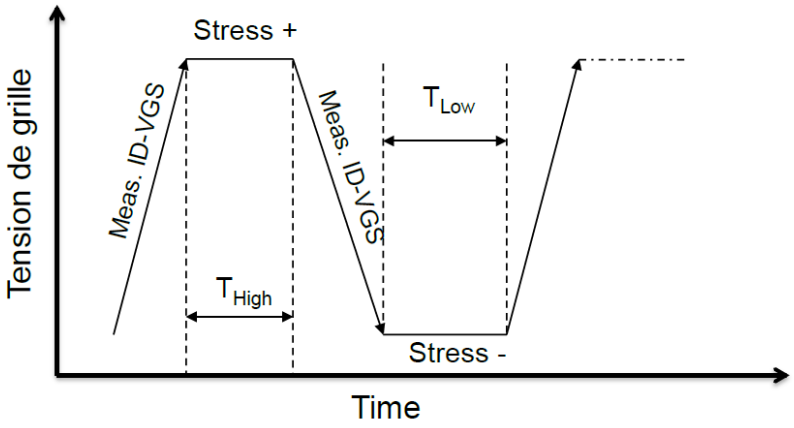


Fig. 1.28: HTGB test configuration, representing the gate voltage as a function of time [28]

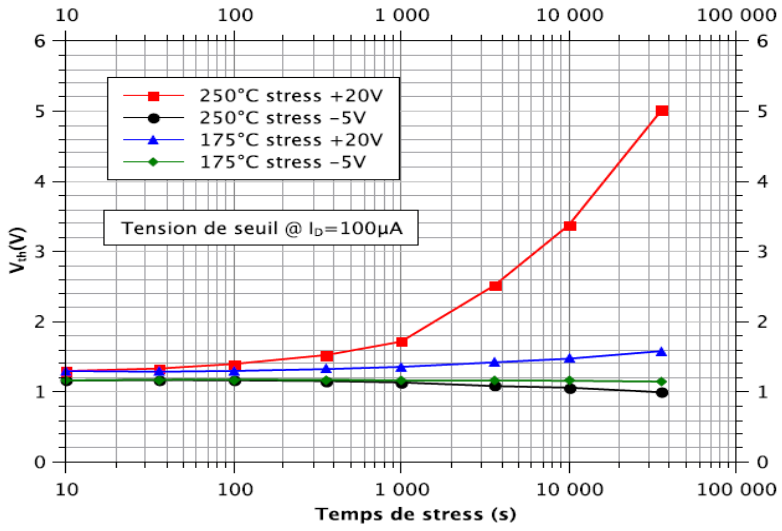


Fig. 1.29: Threshold voltage evolution as a function of incrementing stress time [28]

1.3.3.3. HTGB test with fix stress time

In this test, the stress cycle time is fixed at 1000 s with a temperature of 250 °C and V_{GS} switching between -5 V and +20 V. The test's results are illustrated in Fig. 1.30 where the difference measured between the threshold voltages during the increasing and the decreasing of V_{GS} simultaneously is represented as a function of the cycles' number.

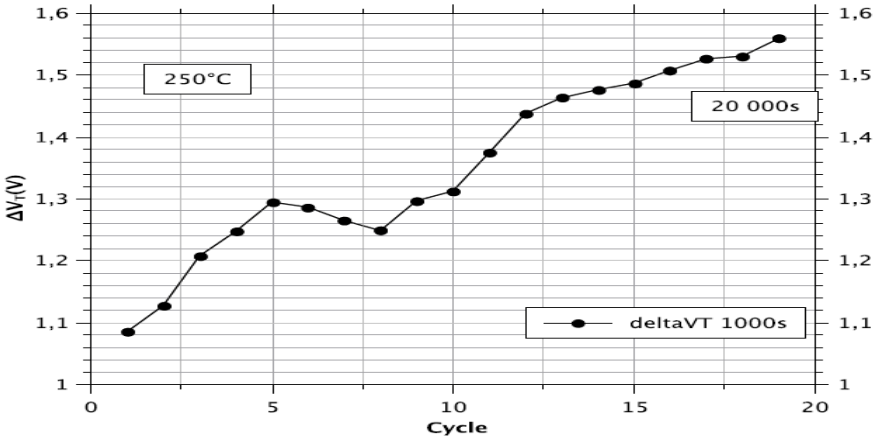


Fig. 1.30: Threshold voltage's difference as a function of cycles' number [28]

Having a fix stress time, the increasing of the threshold voltage's difference from 1.08V to 1.56V (44%) indicates an increasing of the trapped charges. Actually, this phenomenon of degradation is irreversible and can have disastrous consequences. However, as the gate manufacturing's quality is the preponderant factor of the instability, the BTI phenomena may decrease with the improvement of the oxidation processes (using "NO Annealing" procedure) [28]. Similar results can be found in the recent literature [16-18] [29] [30].

These tests described above are used to study the reliability of the gate oxide. However, as previously mentioned in the Introduction of this manuscript, the most observed failures under normal conditions in a PV inverter are related to the temperature, including peak temperature and temperature swings [1] [8]. Moreover, it was found in [6] and [7] that absolute temperature is not the dominant factor in the reliability performance, while thermal cycles contribute with a large percent to the overall failure rate [3]. Hence, cyclic loads are more important than peak loads, especially that PV inverters often experience large temperature swings, due to variable solar irradiance and ambient temperature. In case of high temperature variations, failures are usually induced by the mismatch in the coefficients of thermal expansion of the different materials in the chip and package [7]. Accordingly, the following section represents an overview of power cycling's state of art.

1.3.4. A review of power cycling's state of art

1.3.4.1. Active Power Cycling (APC) [12] [36] [38]

Active power cycling is one of the most important accelerated ageing tests, since that around 65% of failures encountered in power modules are due to thermo-mechanical phenomena [4] [12] [27]. Active power cycling (APC) and passive temperature cycling (PTC) are the two most common thermal acceleration tests used in assessing reliability. During power cycling the current is periodically switched on and off, hence the chips' temperature rises and falls due to alternating heating and cooling, inducing a junction temperature

swing ΔT_J. One power cycle is the period of heating up the junction from minimum temperature to maximum temperature and then cooling it down again.

APC tests usually accelerate the thermo-mechanical stress between layers with different CTEs. Actually, the connections between the DCB and the chip as well as bond wire connections are particularly subject to stress. This test heats up the power modules actively as they would be exposed to during normal operation due to different kinds of stress. Once the monitored indicators of failure APC test exceed their threshold value, the End of Life criteria is considered fulfilled. The number of cycles to failure N_f is then determined as a function of the junction temperature swing amplitude ΔT_J, and then used in models for lifetime estimation.

In APC tests, the chip is the heating source whereas in PTC tests the heating source is external to the power module. Accordingly, the temperature distribution in the DUT is different, since the temperature is spatially not homogenously distributed in APC tests whereas for PTC tests the temperature of the semiconductor device is more uniform. Moreover, the commonly used cycle times are about ten to hundred times shorter in APC test (from 0.2 seconds to 1 minute) than at PTC tests (from 15 minutes to 1 hour). Certain type of APC tests are preferred to PTC tests where the semiconductor devices switch as in the real application. However, the acceleration of both methods by increasing the temperature variations is controversial due to the activation of different material related mechanisms.

LESIT (LeistungsElektronik Systemtechnik und InformationsTechnologie) project was one of the earliest and most known APC tests, while many military specifications are used to standardize the APC test procedures for military applications. Moreover, Joint Electron Devices Engineering Council (JEDEC) standards JESD22-105C and JESD22-A122 are two well-known APC testing protocols. However they do not explain in detail about the dependence of operating conditions, indicators of failure and failure criteria. Hence, APC procedures need to be standardized with more details.

RAPSDRA (Reliability of Advanced Power Semiconductor Devices for Railway traction Applications) was another important research program on APC reliability testing [49]. It includes 2 power cycling types, where the first test focuses on the bond wire reliability with a minimal junction temperature of $55\,°C$ and ΔT_J varying between $50°C$ and $70°C$. In this test, the power-on-time T_{on} is short so that the cycle's period is lower than 3 seconds. The second APC test type focuses on the solder reliability, with same temperature conditions but with longer cycle (1 min). Actually, the type of the encountered failure mechanisms is dependent on the choice of T_{on} [12] [36] [38]. Hence, the study of the application's mission profiles is primordial when performing accelerated ageing tests. This issue represents the main concern in this PhD, as it will be discussed in details at a later stage.

1.3.4.2. Control strategies

Four control strategies are commonly used in APC tests. These strategies are described and compared in [12] [50]:

A) T_{on} = constant and T_{off} = constant

In this strategy of constant timing, the load current is switched on and off in fixed time intervals. ΔT_J is defined at the beginning of the test by applying a constant current. However ΔT_J increases during the test due to ageing effects. This method is the most sever one, but the closest to the application.

B) ΔT_C = constant

Using this strategy, the heat sink's temperature is controlled, with on-time T_{on} and off-time T_{off} are variable, but determined by the time needed to heat up and cool down the power module, until reaching the desired temperatures. Any change in the cooling liquid's temperature can be compensated by adjusting the heating and cooling times, in order to maintain a constant temperature swing. This strategy is less severe than the first strategy, given that a possible degradation of the thermal interface between heat sink and module can be compensated.

C) P = constant

Using this strategy, T_{on}, T_{off} and the power losses are kept constant. This can be done by controlling the gate voltage or current to compensate an increase in collector-emitter voltage V_{ce} in case of an IGBT. Given that it reduces the acceleration effect of different failure mechanisms, this strategy is much less severe for the device, and significantly increases the number of cycles to failure.

D) ΔT_J = constant

Using this strategy, both the minimum and maximum junction temperature are kept constant by reducing T_{on} and the load current. This strategy leads to the highest lifetime by compensating all degradation effects.

1.3.4.3. Type of APC tests

Generally speaking, 2 families of APC tests are in use: DC current and Pulse Width Modulation PWM APC tests. The main circuits used in literature are briefly described in [36] [51] as follows:

1.3.4.3.1. DC current source

The goal of DC current injection (Fig. 1.31) is inducing thermal stress by creating a thermal flux in the IGBT module. The advantages of the DC test bench are the relative simplicity and the possibility to easily perform "online" measurements of electrical and thermal indicators without having to stop power cycling. However, the electrical excitation of devices is not realistic since no switching and no high voltage is applied. The junction temperature is adjusted by controlling the duration and amplitude of the current injection [51].

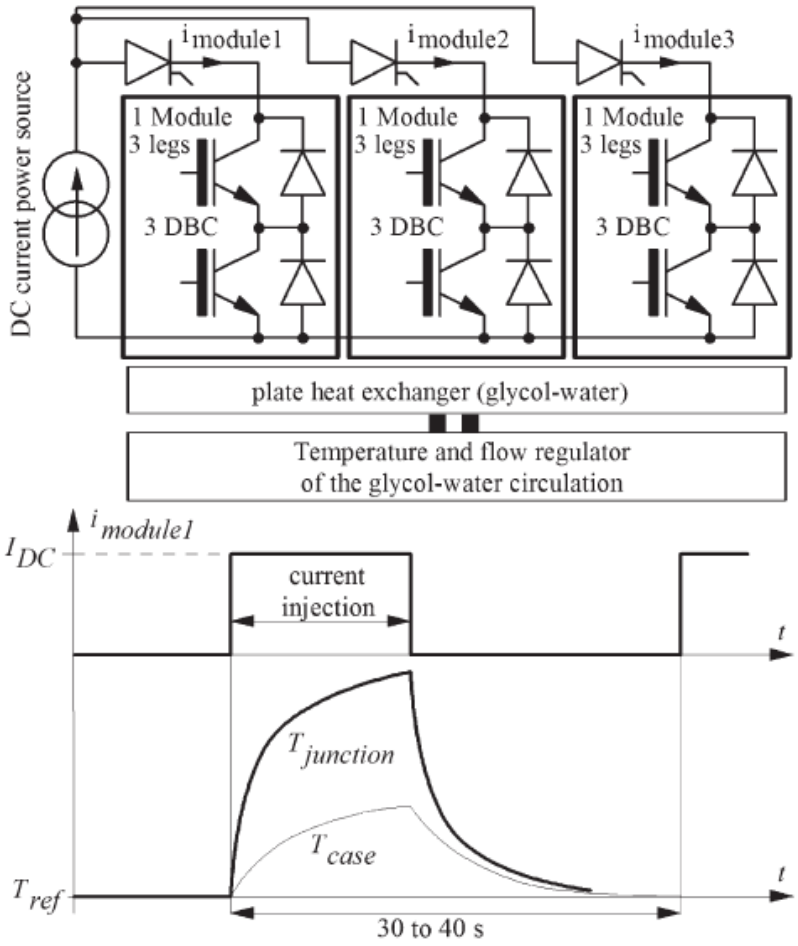


Fig. 1.31: DC current APC test bench [51]

1.3.4.3.2. Full-bridge inverter with inductive load

The full bridge inverter with an inductive load has several advantages over other circuits, where the inductive load ensures the distribution of losses between diode and IGBT. This is a back-to-back topology using the opposition method with pulse width modulation [52] [53]. Since the power is circulating between the phase legs, the input power is only required to supply the device's losses [36] [51] [54].

The PWM test bench shown in Fig. 1.32 was designed to generate power cycling with realistic electrical stress on the power devices. Two legs (two DCBs) of the IGBT module are joined to constitute a single-phase PWM inverter with an adjustable switching frequency. For power devices, the operating conditions are similar to those existing in a drive inverter. The principle of this test bench is described in details in the literature [51] [55].

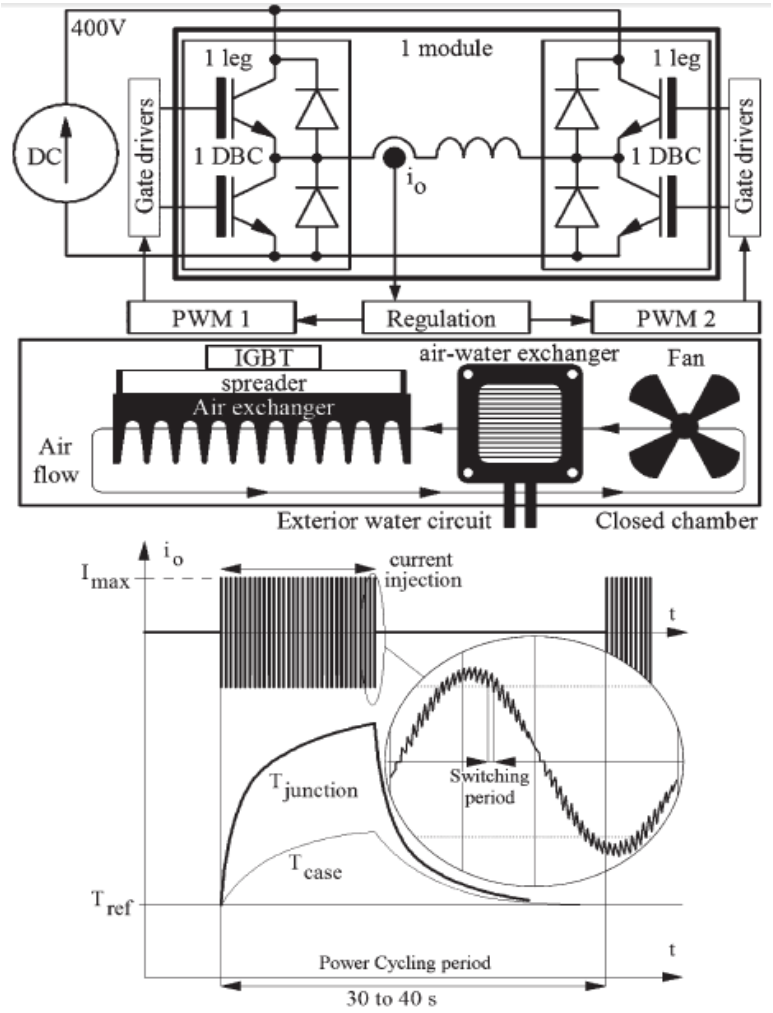


Fig. 1.32: Elementary block of the PWM test bench [51]

According to [51], balancing the current between the module's three legs on the DC test bench (Fig. 1.31) cannot be very accurate, and the electrical stress is not strictly identical. In the PWM test bench, the switched currents in the device are identically set by the load. It should be noted that, due to the absence of switching losses, the RMS current per chip must be higher and adjusted in the case of a DC test bench in order to generate the thermal fluxes needed.

On the other hand, the RMS current per chip is fixed in the case of a PWM test bench, where the thermal flux can be adjusted by the switching losses that depend on the switching frequency value. Moreover, spatial temperature distribution is not identical given that the diodes are not used in the DC mode [51].

1.3.4.3.3. Inverter-inverter back-to-back

Two three-phase identical inverters can be arranged in a back-to-back form with inductors joining the three phases as shown in Fig. 1.33 (for traction application). The system currents are made to circulate between the two inverters so that they can each operate to their full power of 800 kW. Similarly to the previous topology, this one applies the pulse width modulation PWM mode too, while only the losses are provided by the DC power supply [52]. Moreover, it can be applicable to test semiconductors in three-phase inverter application, however the three-phase control is complicated compared to single phase control [36] [56].

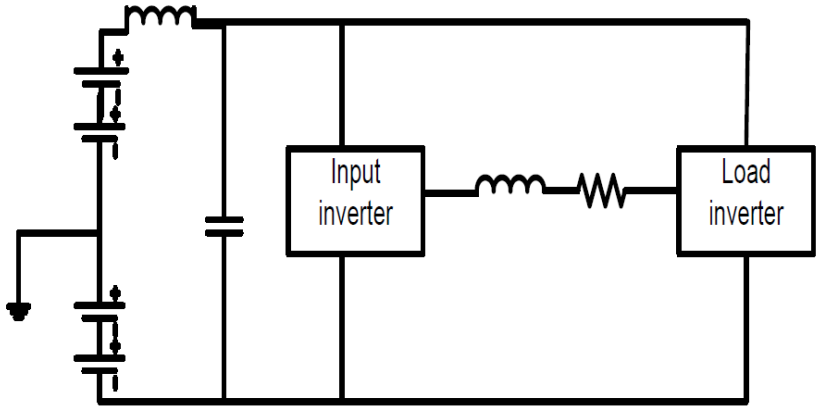


Fig. 1.33: Three phase back-to-back inverters test circuit [36] [56]

More power cycling circuits are depicted in [36] like push-pull topology [57], low frequency and high frequency topologies, half bridge inverter with inductive load topology and overload current circuits for motors applications.

1.3.4.4. Review of APC tests

70 publications on active power cycling from 1993 to 2014 were reviewed in [12]. The quantity of modules tested, the type of modules, the test conditions as well as the analysis methods, the goal of studies and the lifetime estimations were reported and analyzed for all the publications. The study reveals that the big majority of tests are performed on IGBT (about 65%), then come diode (10%) and MOSFET (10%). Most of the DUTs are power modules with Al wires, a lead free die-attach, a DCB soldered with a lead-rich alloy on a Cu base plate, and without any encapsulating material. However, a lot of information are missing, such as the type of solder for both die-attach and DCB-attach as well as the type of the used DCB [12]. Moreover, most of the tests were done with the first control strategy, where T_{on} and T_{off} are kept constant.

The failure analyses done were often dedicated to study one particular layer of the module. In more than 30% of cases, the die-attach is the center of interest, followed by bond wires studied in 28% of papers. The chip metallization on top of the chip is also frequently observed (18%), as well as the DCB attach (15%).

Eventually, the failure criteria were based on 6 different parameters: collector-emitter voltage V_{ce}, thermal resistance R_{th}, thermal impedance Z_{th}, drain-source on-state resistance $R_{DS_{on}}$, gate leakage current I_{GE_S} and maximum junction temperature. In some papers no failure criterion is defined and the test lasts until the complete failure of the device, which is referred as the End of Life of the device. Most of the tests considered an increase of 5% in V_{ce} and of 20% in R_{th} as failure criteria, often in combination. An increase of 20% in V_{ce} is also used as failure criterion in 13% of the tests. It should be noted that the use of $R_{DS_{on}}$ as failure criterion begins to expand [12].

1.4. Condition monitoring and failure indicators in APC tests

Generally, the condition monitoring of power semiconductors can be partially done by measuring periodically different ageing indicators as the on-state voltage and resistance, thermal resistance and impedance, gate threshold voltage, gate leakage current and breakdown voltage, etc. In this section the main ageing indicators will be discussed.

1.4.1. Voltages

The collector-emitter voltage V_{ce} in the case of IGBTs, the drain-source voltage V_{DS} in the case of MOSFETs, and the forward voltage V_f in the case of diodes under a given current are commonly used as ageing indicators. These parameters are widely used in the literature [27] [39] [58] [59] [60], where the ageing monitoring is done periodically in an accelerated ageing test bench, directly after each accelerated ageing phase. Inversely, the monitoring of these electrical parameters can be done online also, during the functioning of the inverter, as proposed in [61].

An increase in these voltages under given current and temperature, of between few percent to 20% (mostly 5%) is considered to be an indicator of the power module ageing. In the case of silicon devices that can indicate bond wire lift off and/or heel crack, or a reconstruction of the metallization surface. The relative variations due to bond wires damage are very low since the low voltage across the connections constitutes to a weak part of the total on-state voltage. Therefore this measurement must be made with a very high degree of accuracy [12]. Fig. 1.34 represents an example of V_{ce}'s evolution as a function of cycles' number during an APC test. In this case, the IGBT is near destruction after 4748 kcycles, with the discrete steps of V_{ce} assumed to be due to bond wire lift off [58].

In the case of MOSFETs, V_{DS} can be replaced by the drain-source on-state resistance $R_{DS_{on}}$ [62]. In order to determine $R_{DS_{on}}$, the APC test has to be stopped, then a current is injected in the device, while the exact drain current I_D that is injected through the device and the drain-source voltage V_{DS} are measured. The increase in $R_{DS_{on}}$ can indicate bond wire lift off and/or heel crack, or a reconstruction of the metallization surface. It tends also to increase in electrical tests when the component thermal performances are decreasing, while a steep increase is observed when the percentage of failure is important [12]. For this parameter, the threshold value is generally 20%.

Moreover, the gate threshold voltage $V_{GS_{th}}$ is considered as an indicator of gate oxide based failures. A variation of 20% in gate threshold voltage is considered as a failure criterion in [36].

Breakdown voltage indicates passivation based substrate degradation or failures. However, breakdown voltage was not considered widely as a failure indicator. Actually, the measurement of breakdown voltage during power cycling is difficult, since it involves circuit change from a high current and low voltage circuits used for power cycling to a high voltage, low current circuits to measure breakdown voltage degradation [36].

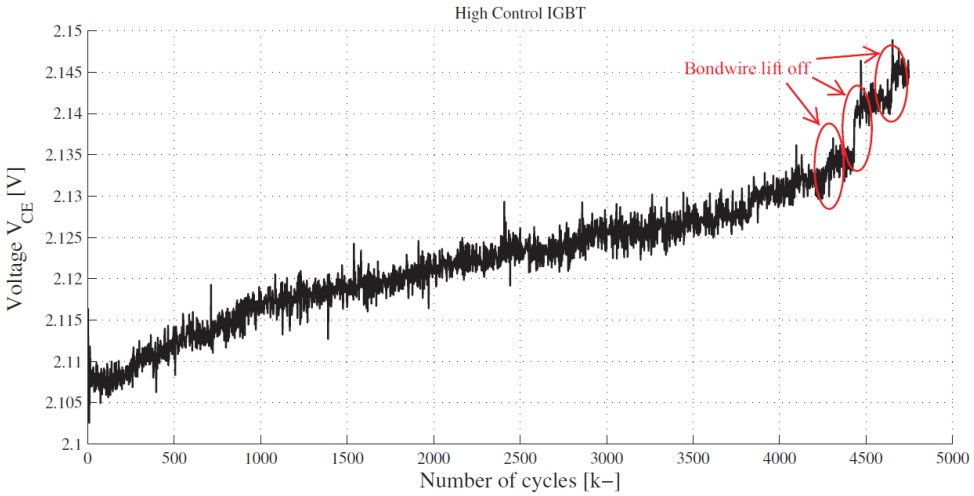


Fig. 1.34: Measured *Vce* for IGBT [58]

1.4.2. Thermal resistance and impedance

Another damage indicator of the power modules is the increase of the power modules' thermal resistance R_{th} or thermal impedance Z_{th}. Usually, this parameter is calculated especially from the active part temperatures that are estimated conventionally, by injecting a constant current in each semiconductor device, provided by an external current source. The calculation of the thermal impedance is often carried out during the cooling phase, after switching off the current source. If a power module with closed package is under test, the easiest way to measure T_J is via the measurement of TSEP [12], such as IGBT's collector-emitter voltage and the forward voltage V_f in case of diodes. In case of a MOSFET, the forward voltage of the MOSFET's intrinsic body diode can be used as TSEP.

However, this method widely presented in the literature [63] [64] [65] [66] requires a total disconnection of the characterized semi-conductor device from the rest of the inverter, and needs an independent high current source. Thus, the monitoring of Z_{th} in APC tests where PWM current is applied is still complicated. Accordingly, this issue represents a main concern in this PhD, as it will be discussed in details later on. Usually, an increase of about 20% in Z_{th} as represented in Fig. 1.35 is considered as an indicator of the soldering and/or substrate fatigue (sometimes between 10% and 20%). However, other methods can be found in the literature, where the measurement of the junction temperature is done without disconnecting the power modules, yet that requires a more instrumented test bench [67].

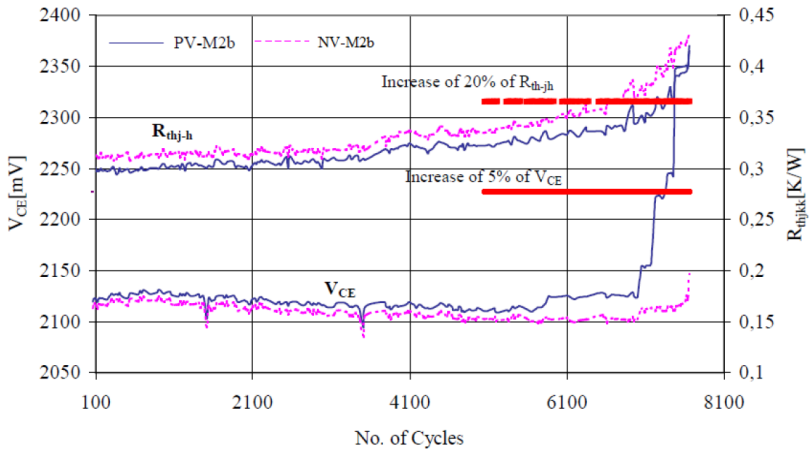


Fig. 1.35: Evolution of V_{ce} and R_{th} during APC test of ECONOPACK power modules at ΔT_J = 113 K [12] [68]

1.4.3. Currents

Collector/drain and gate leakage currents are the usual indicators of failure. Current measurement is more difficult than voltage measurement and hence is not commonly used. A 20% increase in the conducting current (collector current) is an indicator of thermal hotspot and short circuit failures. A 20% increase in the gate saturation current is an indicator of gate short circuit failure [36].Usually, the gate leakage current increases when tests are applied at high temperatures, as represented in the study done in [69] on SiC MOSFET devices.

According to this literature's review, different ageing indicators are monitored during power cycling, where the most used indicators are on-state voltage/resistance as well as the thermal resistance/impedance. This can be also noticed from a review of the state of art in [36] that summarizes different power cycling tests and tabulates the operating conditions, failure indicators used, temperature swings considered, and the time duration of tests as exhibited in Table 1.1.

[36] represents semiconductor devices' common failure mechanisms as found in the literature, as exhibited in Table 1.2, while Table 1.3 represents examples of common failure criteria for the different ageing indicators, as found in [38] according to international norms.

Table 1.1: Comparison of different power cycling tests in literature [36]

Reference/method	Testing profile	Measurements	Cooling	Temperature swing and Tmax	Failures and indicators	Failure mechanism	Circuit
[70]	250 A for 0.9 s and off for 1.3 s	Junction temp. *Vce*, *Ic*	Water cooled	ΔT=60K *TJmax*=105-115 °C	*Vce* increase at 400000 cycles	Bond wire lift off	Pulse
[71]	500 A for 45 s and 2000 A for 5 s	DC voltage (*Vdc*), AC current (*Iac*) IGBT temp.	Air cooled	ΔT= 7 K		No failures after 113522 cycles, 1491 hours	1 phase H bridge
[57]	200 A for 20 s, off for 40 s	Junction temp *Vce*, *Ic*		ΔT=80 K *TJmax*=150 °C	*Vce* increase at 42800 and failure at 43,500 cycles	Gate leakage failure	3 phase inverter with current generator
[56]	Real-time current profile of traction used. 113 s period	Automatic temp. measurements			No failures after 2200 hours		Two inverters joined by inductors, 800kW power, 60KW losses

<table>
<tr><td rowspan="2">[72]</td><td>Half sinusoidal current by rectifier bridge, different current profiles used</td><td>Vce and T_J</td><td></td><td>ΔT=100 to 150 K</td><td>Shown in table below</td><td></td><td>6 diodes tested</td></tr>
<tr><td colspan="7"><table>
<tr><th>Results</th><th>ΔT_J (°C)</th><th>Heating time</th><th>Cooling time</th><th>Load current Failure</th><th>Cycles</th></tr>
<tr><td>PC1:Module 1</td><td>105</td><td>38</td><td>56</td><td>18</td><td>60 k</td></tr>
<tr><td>PC2:Module 2</td><td>130</td><td>20</td><td>70</td><td>28</td><td>-</td></tr>
<tr><td>PC3:Module 3</td><td>155</td><td>28</td><td>85</td><td>32</td><td>-</td></tr>
<tr><td>Copper molded</td><td>110</td><td>21</td><td>84</td><td>28</td><td>3800</td></tr>
</table></td></tr>
<tr><td>[73]</td><td>50 A in 12 s period to maintain 10 to 150 °C</td><td>IGBT Temperature</td><td>Thermo-electric coolers</td><td>ΔT=140 K</td><td>1427 cycles, 37 hours</td><td>Bond wire lift off</td><td>1 phase inverter</td></tr>
<tr><td>[74]</td><td>23 s heating and 5 s cooling cycle</td><td>Vce, Rth</td><td>Water cooled</td><td>ΔT=80 K
ΔT =110 K
85360 cycles at
ΔT=80 K</td><td>28900 cycles at 110 K</td><td>Bond wire lift off</td><td>6 pack IGBT module,2 IGBTs in central H-bridge tested in series</td></tr>
</table>

Table 1.2: Semiconductor devices' common failure modes [36]

Failure Factor	Failure Mode
Diffused Junction Substrate	Decreased breakdown voltage Short circuit Increased leakage current
Gate oxide film Field oxide film	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or V_{th} drift
Die bonding : Chip-frame connection	Open circuit Short circuit Unstable/intermittent operation Increased thermal resistance
Wire bonding: Wire bonding connection Wire lead	Open circuit Short circuit Increased resistance
Input/output pin:	Open circuit

Static electricity Surge Over voltage Over current	Short circuit Increased leakage current
Passivation : Surface protection film Interlayer dielectric film	Decreased breakdown voltage Short circuit Increased leakage current h_{FE} and/or V_{th} drift Noise deterioration

Table 1.3: Failure criteria for the different ageing indicators [38]

Parameter	**% Degradation for failure**
Thyristors / diodes	
Direct reverse current / direct off-state current I_{R_D}, I_{D_D}	+ 100% above the upper limit
Gate trigger voltage / current V_{G_T}/I_{G_T}	+ 10% above the upper limit
On-state / forward voltage V_T/V_f	+ 10% above the upper limit
IGBT / MOS	
On-resistance / saturation voltage $R_{DS_{on}}$, $V_{ce_{sat}}$	+ 20% of start value
Max. change in threshold voltage $V_{GS_{th}}$, $V_{GE_{th}}$	$\pm$20% of the limits
Gate leakage current I_{GS_S}/I_{GE_S}	+ 100% above the upper limit
Drain-source current / collector-emitter cut-off current I_{DS_S}, I_{CE_S}	+ 100% above the upper limit
All modules	
Internal thermal resistance junction to case $R_{th_{JC}}$	+ 20% of start value
Isolation test voltage V_{isol}	Specified limit

1.5. Conclusions and proposed approach

According to the state of art, the most observed failures in PV inverters are due to the temperature, including peak temperature and temperature swings. More specifically, within those two factors, the absolute temperature is not the dominant factor in the reliability performance, while thermal cycles contribute with a large percent to the overall failure rate. Hence, cyclic loads are more important than peak loads, especially that PV inverters often experience large temperature swings, due to variable solar irradiance and ambient temperature. In case of high temperature variations, failures are usually induced by the mismatch in the coefficients of thermal expansion of the different materials in the chip and package.

However, the existing reliability tests (including APC and PTC tests) are not necessarily well adapted to photovoltaic applications. When applying these tests, mechanisms of failures that do not occur in the real application could be observed, and inversely other

mechanisms that usually occur could be not recreated. Moreover, the type of the encountered failure mechanisms strongly depends on the choice of the APC tests' parameters, such as cycles' duration and amplitude. Thus these tests need better correlation with field conditions, as well as better consideration of the photovoltaic mission profiles.

Accordingly, the following chapters will expose a new methodology to carry out accelerated ageing of photovoltaic inverter's semiconductor devices, aiming to better represent the natural ageing process of the power modules in inverters than the traditional accelerated ageing processes. This is done by considering the mission profiles of the current and ambient temperature, extracted over several years from several photovoltaic power plants. These profiles are used to study the dynamics of the photovoltaic current and ambient temperature as it will be represented in Chapter 4, in order to design an accelerated ageing current's profile. The purpose of this profile is to induce thermo-mechanical constraints close to those seen by the semiconductor devices in a PV inverter, during an ageing test that includes APC and PTC simultaneously.

In order to estimate the junction temperature of the semiconductor devices corresponding to the mission profiles and to the accelerated ageing one, a power losses estimation model (Chapter 2) and a thermal model (Chapter 3) will be developed. These models are coupled together in order to consider the electro-thermal coupling of temperature-dependent electrical parameters.

Another statement concluded by studying the APC's state of art is that when APC is applied using PWM mode, the operating conditions are similar to those existing in a drive inverter, where the semiconductor devices are switching under the DC bus voltage. Moreover, when using the opposition method in this type of test circuits, the input power is only required to supply the device's losses, which represent less than 5% of the total inverter's power. Accordingly, in the present work, the designed accelerated ageing current profile will be performed in test benches inducing simultaneously passive and active cycling under switching nominal conditions and PWM operating mode in a back-to-back configuration using the opposition method.

The previews state of art revealed that the big majority of APC tests were performed with Si IGBTs and much less with SiC MOSFETs. However, it revealed also great advantages of silicon carbide-based devices over silicon-based devices, which makes it probable that SiC MOSFETs will replace Si IGBT in the future. Nevertheless, despite all the promising advantages, the interfacial charge trapped in the case of SiC-based devices at and near the $SiC-SiO_2$ inversion channel-gate insulator interface is much greater than in the case of Si. This can lead to significant degradation in the device's reliability and slow down the deployment of SiC MOSFET power modules in the industry.

Accordingly, a first test bench will be dedicated to test SiC MOSFET power modules as it will be represented in Chapter 5, in order to identify the potential indicators of ageing/failure and failure mechanisms of SiC MOSFET devices used in photovoltaic DC/AC inverters.

The review of health monitoring's state of art revealed that the thermal impedance represents the main indicator of failures of the soldering and/or substrate fatigue. Moreover, nowadays this parameter is calculated especially from the active part temperatures that are estimated conventionally, by injecting a constant current in each semiconductor device, provided by an external current source. Thus, using this method in the APC test bench with PWM requires a full disconnecting of the power modules from the inverter, which represents a complicated task. It should be noted that other methods can be found in the state of art,

where monitoring of the junction temperature is done without disconnecting the power modules, but demands additional instrumentation of the test bench [67].

Accordingly, an in-situ setup for monitoring ageing indicators (thermal impedance and dynamic resistance) will be proposed and evaluated in another test bench dedicated to test Si IGBT power modules as it will be represented in Chapter 6. Using this method, the monitoring can be done without disconnecting the drivers, neither the DC-link capacitors, nor the DC-link bus. Moreover, the condition monitoring is done under the actual DC-link voltage, hence there is no need for an independent current source. Eventually, some examples of condition monitoring implementation in DC/AC photovoltaic inverters will be proposed. The global approach followed in this manuscript is illustrated in Fig. 1.36.

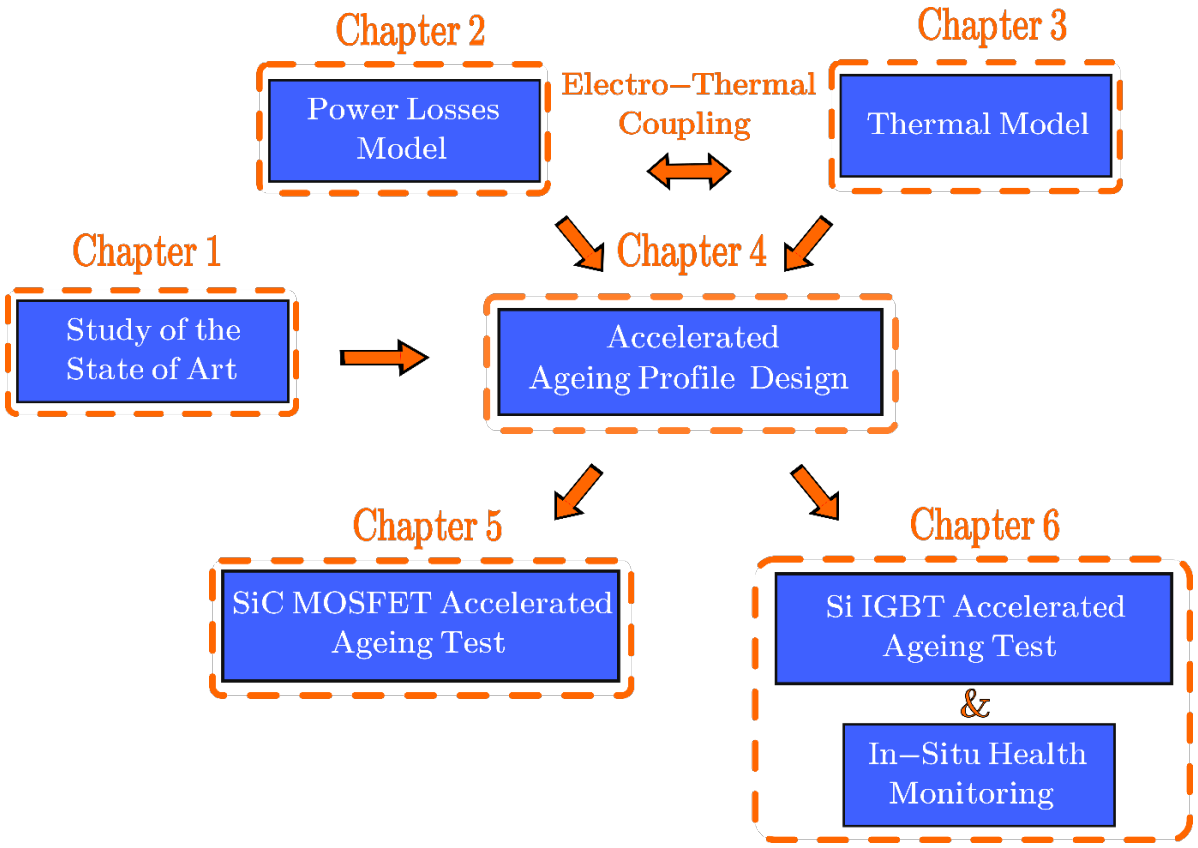


Fig. 1.36: Global approach of the study

Chapter 2:
Power losses estimation

Chapter 2: Power losses estimation

2.1. Introduction

While operating, semiconductor devices like IGBTs, MOSFETs and diodes dissipate energy in the form of heat. The estimation of power losses in these devices is therefore crucial for estimating their junction temperature and choosing suitable heatsinks.

There are several types of power losses in transistors, which can be classified into static losses, switching losses and driving losses as represented in Fig. 2.1. Forward blocking losses and driving losses account only for a small share of the total power dissipation for high power transistors hence they can be normally neglected. In case of high blocking voltages ($> 1kV$) and/or high operating temperatures ($\geq 150°C$), blocking losses may gain importance and may even result in thermal runaway owing to the exponentially rising reverse currents [38] [75] [76].

In the case of diodes, there are no driving losses. The turn-on losses caused by the forward recovery process for fast diodes are neglected, and turn-off losses are due to the reverse recovery losses. Since it only accounts for a minor share of the total power dissipation, reverse blocking power may also be neglected [38].

Considering these hypothesis, only the on-state losses and the switching losses will be taken into account in this chapter, dedicated mainly to present a power losses estimation model. This model will be used to estimate the semiconductors' power losses corresponding to a given current mission profile (Chapter 4), in the case of a Pulse Width Modulation (PWM) DC/AC inverter. In the following sections, the methodology of the power losses estimation from datasheets and from measurements using the double pulse test will be detailed, as well as the electro-thermal coupling of certain electrical parameters of devices that are temperature-dependent. Then the model created using *Matlab* will be represented, and the results will be compared to other simulators results, such as *PSIM*, *IPOSIM* (*Infineon*) and *SemiSel* (*SEMIKRON*) for IGBTs, and *Speedfit* (*WolfSpeed*) for MOSFETs (refer to Fig. 1.36).

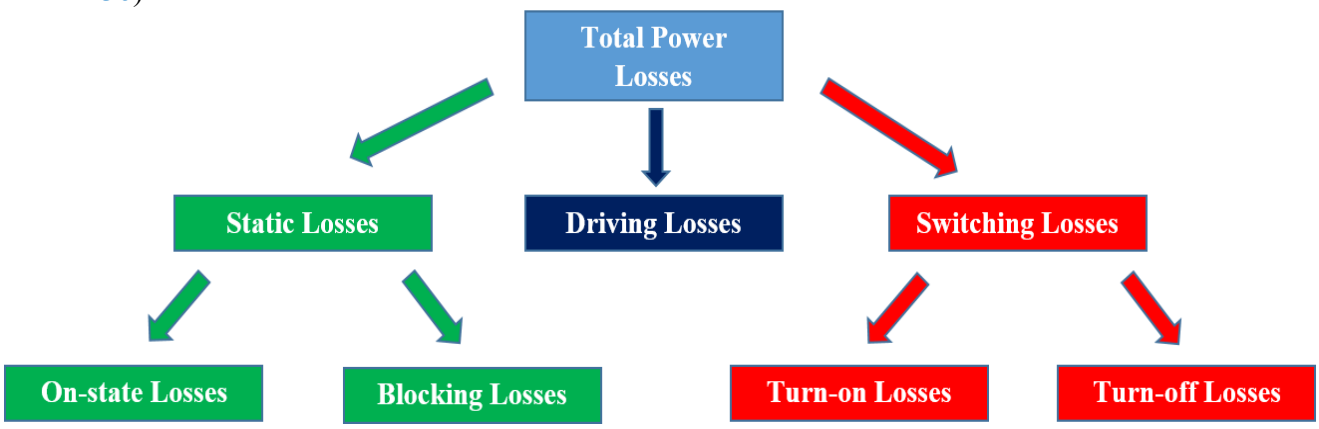


Fig. 2.1: Types of power losses in IGBTs and MOSFETs

2.2. Intersective Pulse Width Modulation (PWM)

As presented in Chapter 1, the conduction losses and the switching losses will be estimated in the case of a PWM two-level DC/AC voltage inverter, represented in Fig. 2.2. As demonstrated in Fig. 2.3, the Intersective Pulse Width Modulation (PWM) involves generating a pulse pattern by comparing a sinusoidal reference voltage V_{ref} to a delta-shaped voltage V_d. V_{ref} sets the fundamental frequency f_{out} of the inverter (usually 50Hz), while V_d sets the switching frequency f_{sw}. The switching happens at the intersections of these two signals (every $T_{sw} = \frac{1}{f_{sw}}$). The ratio of the reference signal's amplitude to the delta-shaped signal's amplitude is called the modulation factor or the modulation depth, and can be expressed as follows:

$$m = \frac{\widehat{V_{ref}}}{\widehat{V_d}} \tag{2.1}$$

This modulation factor can also be defined as the ratio between the fundamental amplitude of the AC voltage V_L, and 50% of the DC-link voltage E as expressed in Eq. 2.2:

$$m = \frac{\widehat{V_L}}{E/2} \tag{2.2}$$

In order to obtain a linear modulation, this factor should be in the range of 0 to 1 ($0 \leq m \leq 1$).

Due to the symmetrical structure of the inverter, the power losses of the different switches are identical, where a switch represents the transistor and its antiparallel diode. Accordingly, it is sufficient to estimate these losses in only one switch, and then multiply them by the number of the switches to obtain the total power losses of the inverter. Therefore, only the power losses of the transistor T_1 and the diode D_1 (Fig. 2.2) will be represented in the following sections.

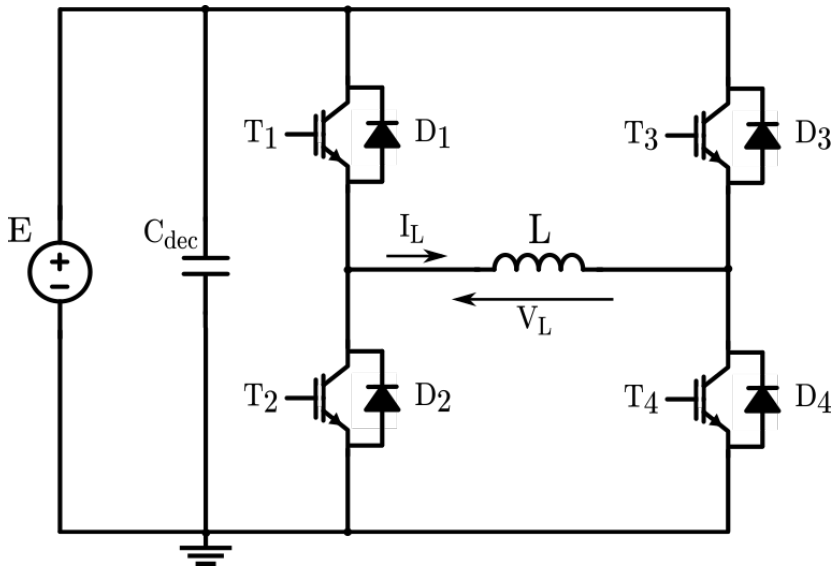


Fig. 2.2: PWM two-level DC/AC voltage inverter in back-to-back configuration

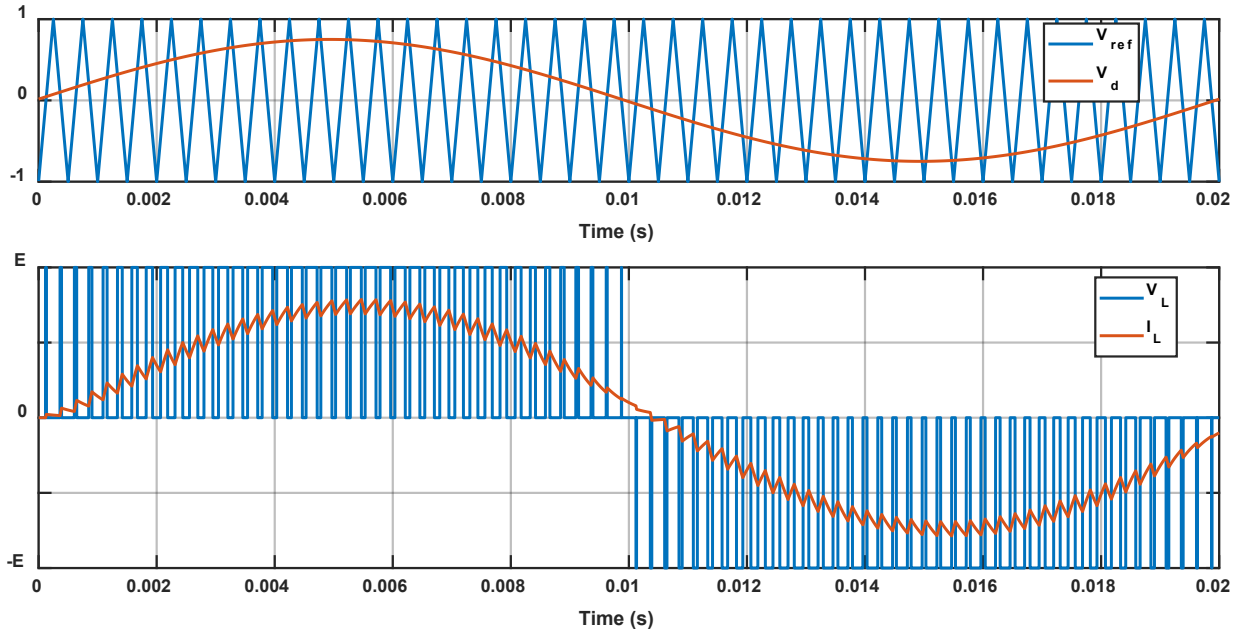


Fig. 2.3: Pulse pattern generation / Load voltage and current

The width of the V_L's pulses in Fig. 2.3 is determined by the duty cycle α, presented in Fig. 2.4 and expressed as follows:

$$\alpha(t) = \frac{1}{2} \cdot (m \cdot \sin(2 \cdot \pi \cdot f_{out} \cdot t) + 1) \tag{2.3}$$

Accordingly, the current I_L in the load can be expressed as follows:

$$I_L(t) = \hat{I} \cdot \sin(2 \cdot \pi \cdot f_{out} \cdot t) + 1) \tag{2.4}$$

It should be noted that the power factor is considered equal to 1 in the whole study.

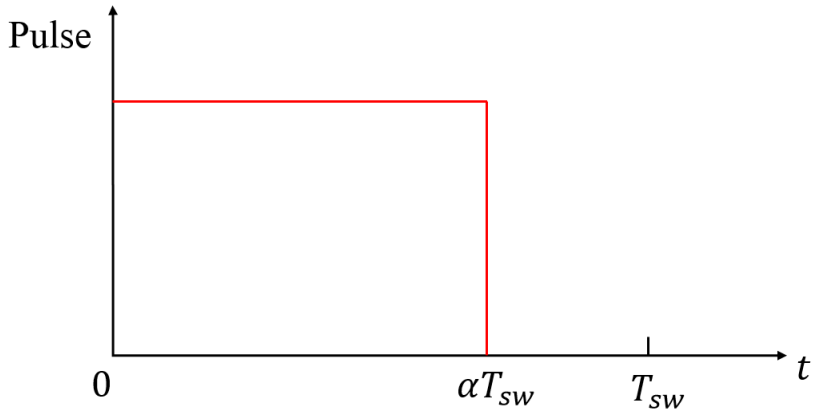


Fig. 2.4: The duty cycle α over a switching period T_{sw}

In the case of IGBT power modules, the conduction phase cycles of T_1 and D_1 can be briefed in Table 2.1, where I_T is the current in T_1, I_f the forward current in D_1, and I_L the current in the load, as shown in Fig. 2.5.

Table 2.1: The cycles of the semiconductors conduction phases in the case of IGBT power modules

$\boldsymbol{Current\ I_L \setminus Time\ t}$	$\boldsymbol{0 \le t \le \alpha T_{sw}}$	$\boldsymbol{\alpha T_{sw} < t < T_{sw}}$
$I_L < 0$	$I_T = 0$ $I_f = -I_L$	$I_T = 0$ $I_f = 0$
$I_L \ge 0$	$I_T = I_L$ $I_f = 0$	$I_T = 0$ $I_f = 0$

However, the case of MOSFET power modules represented in Table 2.2 is more complicated as it will be demonstrated in the next section.

Table 2.2: The cycles of the semiconductors conduction phases in the case of MOSFET power modules

$\boldsymbol{Current\ I_L \setminus Time\ t}$	$\boldsymbol{0 \le t \le \alpha T_{sw}}$	$\boldsymbol{\alpha T_{sw} < t < T_{sw}}$
$I_L < 0$	$I_T = -\dfrac{E_0 - R_D \cdot I_L}{R_{DS_{on}} + R_D}$ $I_f = -\dfrac{R_{DS_{on}} \cdot I_L + E_0}{R_{DS_{on}} + R_D}$	$I_T = 0$ $I_f = 0$
$I_L \ge 0$	$I_T = I_L$ $I_f = 0$	$I_T = 0$ $I_f = 0$

2.3. Conduction losses estimation

2.3.1. Case of IGBT power modules

The conduction losses P_{cond} in a switch as represented in Fig. 2.5 depend on the load current, the junction temperature and the duty cycle. Let's consider I the current through each switch. It can be defined as $I = I_T - I_f$ with I_T the current in the transistor and I_f the current in the diode.

2.3.1.1. Operation in the first quadrant ($\boldsymbol{I_L > 0\ and\ 0 \le t \le \alpha T_{sw}}$)

When the transistor is turned on and the current I_L is positive, the current in the transistor I_T equals I since the antiparallel diode is in off-state. The collector-emitter voltage V_{ce} across power terminals can be expressed by [38] [77]:

$$V_{ce} \approx E_T + R_T \cdot I_T \tag{2.5}$$

where E_T is the threshold forward voltage of the IGBT and R_T its dynamic resistance. These two parameters are temperature-dependent, and can be extracted from the manufacturer's datasheets (see Fig. 2.6).

2.3.1.2. Operation in the third quadrant ($I_L < 0$ *and* $0 \leq t \leq \alpha T_{sw}$)

When the load current is negative and the transistor is turned on, the current can only pass through the antiparallel diode. Then the diode's current is $I_f = -I$ and the voltage across the diode can be approximated by:

$$V_f \approx E_0 + R_D \cdot I_f \tag{2.6}$$

where E_0 is the threshold voltage of the diode and R_D is its dynamic resistance.

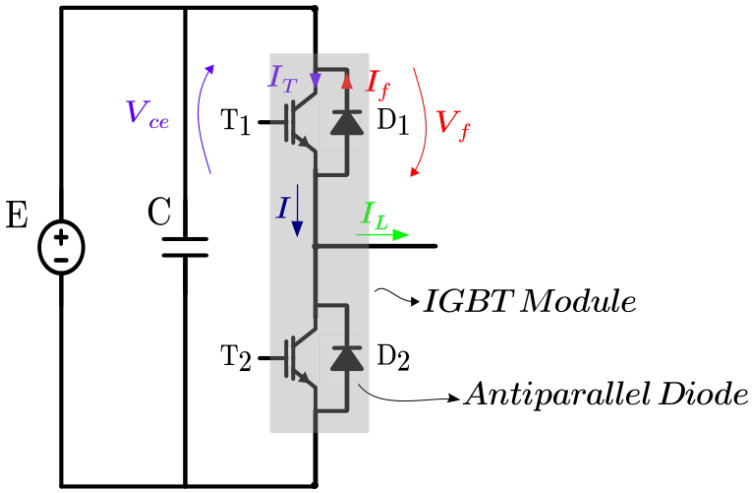


Fig. 2.5: IGBT phase-leg

2.3.1.3. IGBT's conduction losses

As mentioned in Chapter 1, the power losses model will be used to estimate the corresponding losses of current's mission profiles over several years, with more than 800 million samples each, thus only the average losses within a fundamental period T_{out} will be calculated [78]. The average conduction losses can be estimated by the following equation:

$$P_{condT} = \frac{1}{T_{out}} \int_0^{T_{out}} \alpha(t) \cdot V_T(t) \cdot I_T(t) \cdot dt \tag{2.7}$$

where

$$I_T = I_L \text{ if } t \in \left[0, \frac{T_{out}}{2}\right] \tag{2.8}$$

or

$$I_T = 0 \text{ if } t \in \left[\frac{T_{out}}{2}, T_{out}\right] \tag{2.9}$$

2.3.1.4. Diode's conduction losses

The conduction losses in the antiparallel diode P_{condD} can be calculated as follows:

$$P_{condD} = \frac{1}{T_{out}} \int_0^{T_{out}} \alpha(t) \cdot V_f(t) \cdot I_f(t) \cdot dt \tag{2.10}$$

where

$$I_f = 0 \text{ if } t \in \left[0, \frac{T_{out}}{2}\right] \tag{2.11}$$

or

$$I_f = -I_L \text{ if } t \in \left[\frac{T_{out}}{2}, T_{out}\right] \tag{2.12}$$

2.3.1.5. Electro-thermal coupling

The electro-thermal coupling of temperature-dependent electrical parameters should be considered. In the case of an IGBT module, the collector-emitter voltage V_{ce} and the forward voltage of the diode V_f are temperature-dependent parameters. In fact, not taking the electro-thermal coupling into account while estimating the power losses can mislead the results. Therefore Eq. 2.5 becomes:

$$V_{ce}(T_J) \approx E_T(T_J) + R_T(T_J) \cdot I_T \tag{2.13}$$

where

$$E_T(T_J) = E_{T_0} + TC_{v_T} \cdot (T_J - T_{J_0}) \tag{2.14}$$

and

$$R_T(T_J) = R_{T_0} + TC_{r_T} \cdot (T_J - T_{J_0}) \tag{2.15}$$

where E_{T_0} and R_{T_0} are the threshold voltage and the on-state resistance respectively, issued from a line approximation of the forward characteristic of the IGBT, at rated junction temperature T_{J_0}. TC_{v_T} and TC_{r_T} are temperature coefficients, corresponding to the slopes of the lines $E_T = f(T_J)$ and $R_T = f(T_J)$ respectively. By solving Eq. 2.7, the average IGBT's conduction power losses on a fundamental period can be obtained as follows:

$$P_{condT} = I \cdot \sqrt{2} \cdot \left(\frac{1}{2\pi} + \frac{m}{8}\right) \cdot \left(E_{T_0} + TC_{v_T} \cdot (T_J - T_{J_0})\right) + 2 \cdot I^2 \cdot \left(\frac{1}{8} + \frac{m}{3\pi}\right) \cdot \left(R_{T_0} + TC_{vr_T} \cdot (T_J - T_{J_0})\right) \tag{2.16}$$

where m is the modulation factor. Fig. 2.6 from [38] described well the extraction of the thermal coefficients (TC) from the transistor's forward characteristics, corresponding to the slopes of the lines $E_T = f(T_J)$ and $R_T = f(T_J)$ respectively.

The same can be applied to the diode, by replacing E_{T_0} by E_{D_0}, R_{T_0} by R_{D_0}, TC_{v_T} by TC_{v_D} and TC_{r_T} by TC_{r_D}. Then, by solving Eq. 2.10, the diode's conduction power losses can be expressed as follows:

$$P_{condD} = I \cdot \sqrt{2} \cdot \left(\frac{1}{2\pi} - \frac{m}{8}\right) \cdot \left(E_{D_0} + TC_{v_D} \cdot (T_J - T_{J_0})\right) + 2 \cdot I^2 \cdot \left(\frac{1}{8} - \frac{m}{3\pi}\right) \cdot \left(R_{D_0} + TC_{vr_D} \cdot (T_J - T_{J_0})\right) \tag{2.17}$$

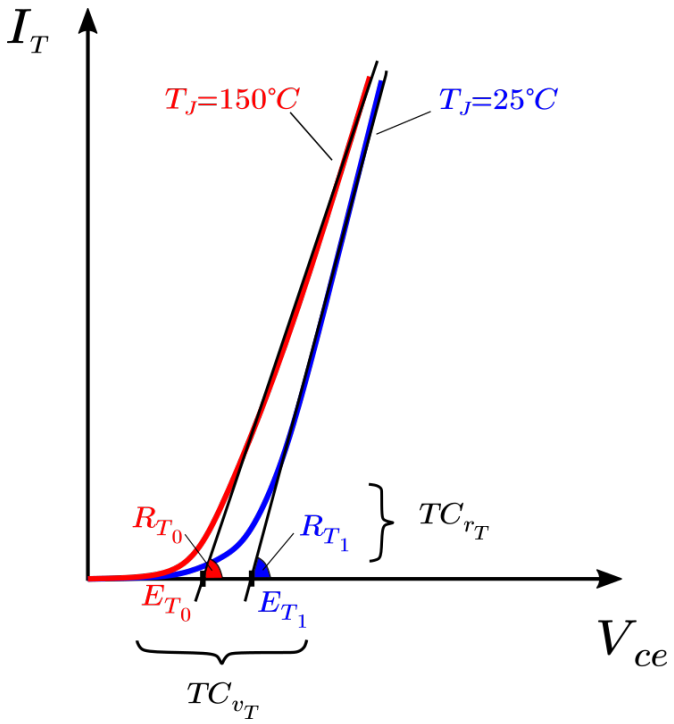


Fig. 2.6: Approximation of on-state characteristic using substitutional straight lines, and extracting TC_{v_T} and TC_{r_T} [38]

2.3.2. Case of SiC MOSFET power modules

In order to study the case of SiC MOSFET power modules, the *Cree*'s device *CAS300M17BM2,* a phase-leg 1700V-300A SiC MOSFET power module with antiparallel Schottky diodes, serves as an example of application in the following sections.

2.3.2.1. Operation in the first quadrant ($I_L > 0$ *and* $0 \leq t \leq \alpha T_{sw}$)

In the case of MOSFET, the relationship between the current I_T and the voltage V_{DS} across the power terminals is:

$$V_{DS} = R_{DS_{on}} \cdot I_T \tag{2.18}$$

where $R_{DS_{on}}$ is the on-state resistance of the MOSFET. This parameter extracted from the manufacturer's datasheets is highly temperature-dependent.

2.3.2.2. Operation in the third quadrant ($I_L < 0$ *and* $0 \leq t \leq \alpha T_{sw}$)

In the case of a MOSFET without an external diode (Fig. 2.7), the current is shared between the MOSFET's channel and its intrinsic body diode. Whereas for a MOSFET module with an antiparallel Schottky diode (Fig. 2.8), the current passes through both the MOSFET and the Schottky diode. This Schottky, having a threshold voltage E_0 smaller than that of the body diode, this latter conducts very little reducing the switching losses, which are almost null in the SiC Schottky diode [79] [80] [81] [82]. Actually, the current distribution between the MOSFET channel and the diodes depends on the overall level of current required by the load.

Fig. 2.9 represents in the case of a MOSFET module with Schottky diodes, the modeling of the I_T current in the transistor, the current in the Schottky diode I_f and the total

current I, as a function of the voltage V_{DS} across both devices. In this modeling approach, the current in the MOSFET's body diode is neglected, which is confirmed by the power modules datasheets. It is assumed, in fact, that the Schottky diode is blocked if the voltage is less than its threshold voltage E_0, and is equivalent to a voltage source E_0 in series with a resistor R_D otherwise. Therefore, if $V_{DS} < E_0$, the MOSFET channel conducts alone with $I_T = I$. Otherwise, if $V_{DS} \geq E_0$, the MOSFET and the diode both conduct ($I = I_T - I_f$) with:

$$I_T = -\frac{E_0 - R_D \cdot I}{R_{DS_{on}} + R_D} \tag{2.19}$$

and

$$I_f = -\frac{R_{DS_{on}} \cdot I + E_0}{R_{DS_{on}} + R_D} \tag{2.20}$$

where E_0, R_0 and $R_{DS_{on}}$ can be fitted from the manufacturer's datasheets. Fig. 2.9 compares also the modeling of the conduction in the 3rd quadrant with the values given in the datasheet.

On the other hand, Fig. 2.10 represents the waveform of the current I_T as a function of time on a fundamental period $T_{out} = 20$ ms. It is noticeable, that at certain point during the negative half cycle of the current I, the sinusoidal shape of the current I_T is distorted; it is at that point that the diode begins to conduct outside the dead time. Fig. 2.11 represents as well the waveform of the current I_f as function of time on a fundamental period. Actually, when the current is negative, the diode conducts also during the dead time.

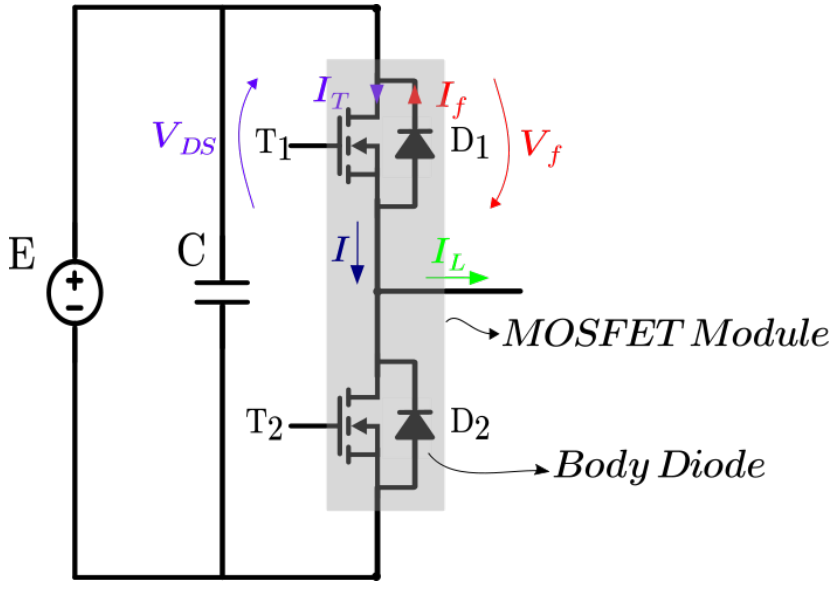


Fig. 2.7: MOSFET module without antiparallel diodes

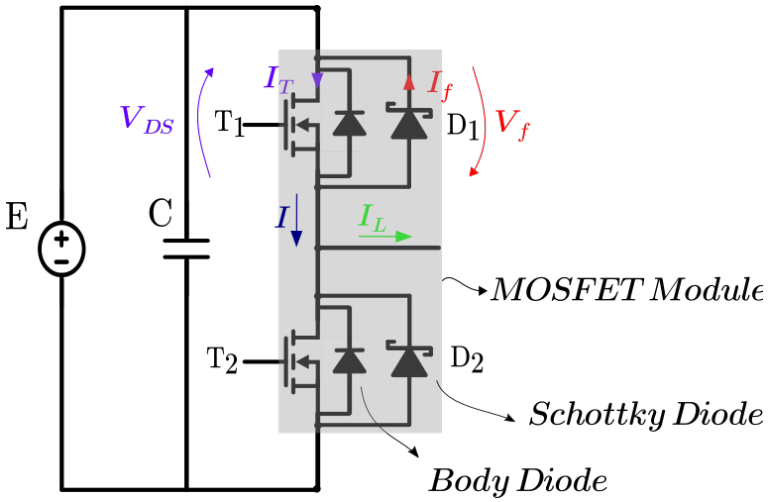


Fig. 2.8: MOSFET module with antiparallel Schottky diodes

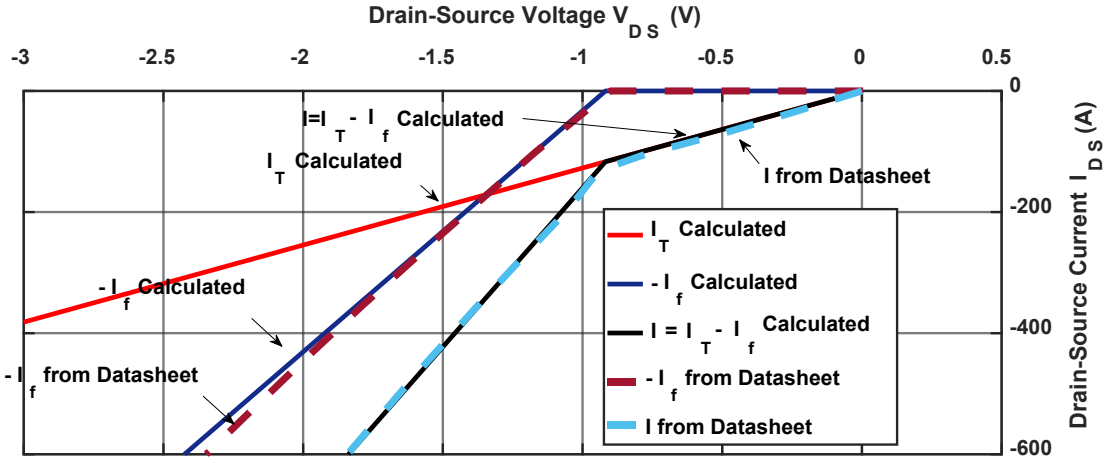


Fig. 2.9: Total current I, current in the transistor I_T and current in the diode $I_{f,}$ as a function of the drain-source voltage V_{DS} from the manufacturer's datasheet

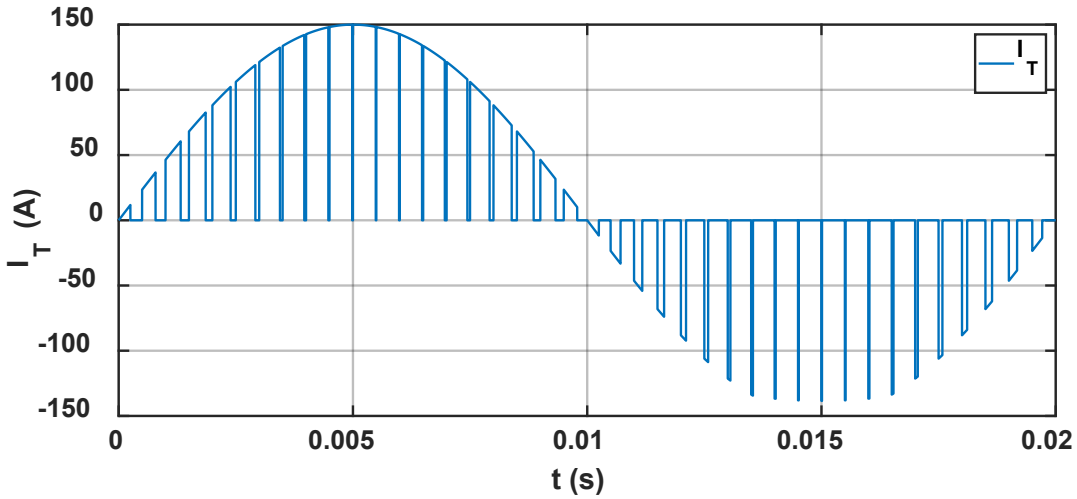


Fig. 2.10: Current I_T in the transistor as a function of time

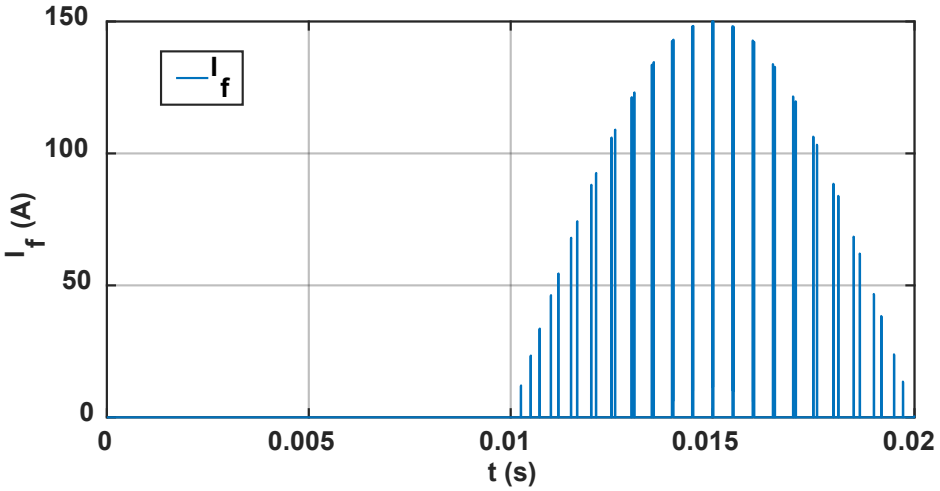


Fig. 2.11: Current I_f in the diode as a function of time

Using this approach, it is now possible to calculate the conduction losses of the MOSFET in the 1st and 3rd quadrants.

2.3.2.3. MOSFET's conduction losses

As mentioned above, and as represented in Fig. 2.12, the current is shared between the antiparallel Schottky diode and the MOSFET's channel between times t_{m1} and t_{m2}. Same as for the IGBT, the average conduction losses can be estimated by Eq. 2.7, with the following differences:

$$I_T = I \text{ if } t \in [0, t_{m1}] \text{ or } t \in [t_{m2}, T_{out}] \tag{2.21}$$

or

$$I_T = \frac{-E_0 + R_D.I}{R_{DS_{on}} + R_D} \text{ if } t \in [t_{m1}, t_{m2}] \tag{2.22}$$

Fig. 2.12 represents the instantaneous conduction losses in the case of MOSFET on T_{out}.

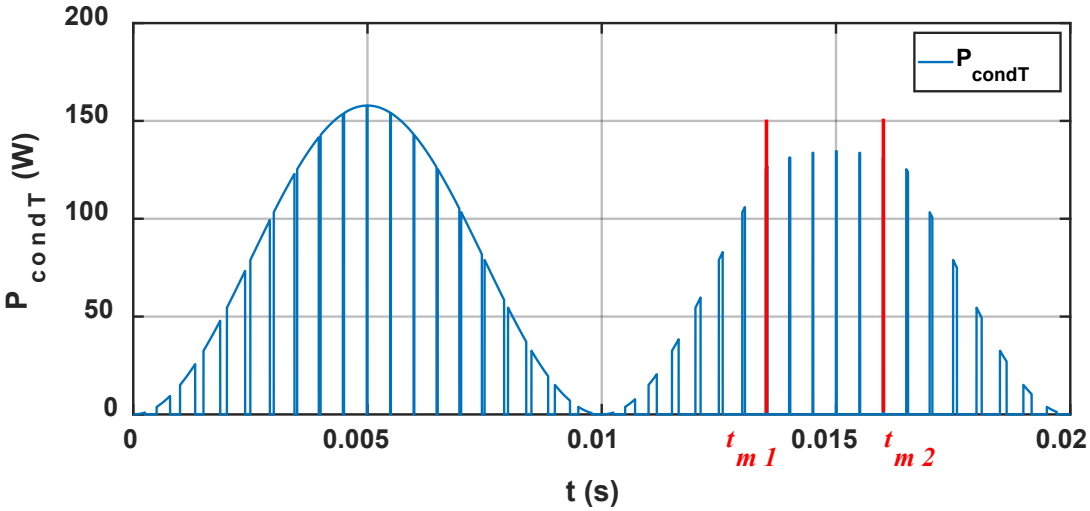


Fig. 2.12: Conduction losses of the MOSFET on T_{out}

2.3.2.4. Diode's conduction losses

The diode's instantaneous conduction losses are represented as a function of time ($P_{condD} = f(t)$) on T_{out} in Fig. 2.13, while Fig. 2.14 highlights it to better distinguish the different phases of conduction. It can be noticed that the diode conducts all the current I during the dead time t_m, while the current level decreases when the MOSFET conducts. The average conduction losses of the diode can be expressed by:

$$P_{condD} = P_{condD}Inv + P_{condD}tm \tag{2.23}$$

where:

$$P_{condD}Inv = \frac{1}{T_{out}} \int_{t_{m1}}^{t_{m2}} \alpha(t) \cdot V_f(t) \cdot I_f(t) \cdot dt \tag{2.24}$$

and

$$P_{condD}tm = \frac{2t_m}{T_{out}.T_{sw}} \int_{\frac{T_{out}}{2}}^{T_{out}} \alpha(t) \cdot V_f(t) \cdot -I_L(t) \cdot dt \tag{2.25}$$

where t_m is the dead time and T_{sw} is the switching period. In the last equation, it is assumed that the diode current's value remains the same during both of the dead times of one switching period.

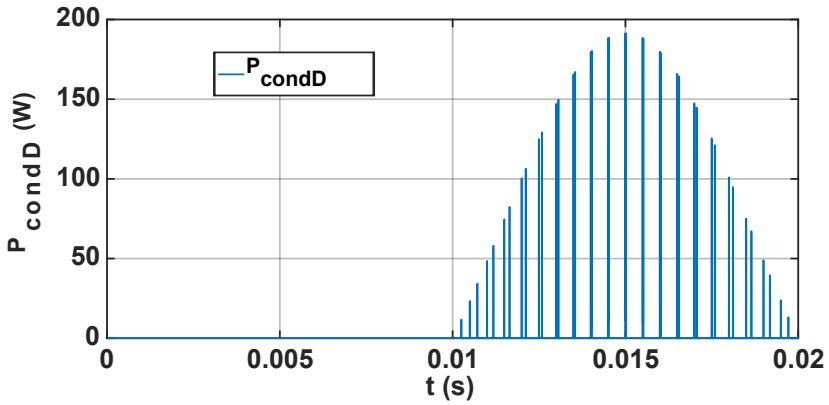


Fig. 2.13: Conduction losses of the Schottky diode

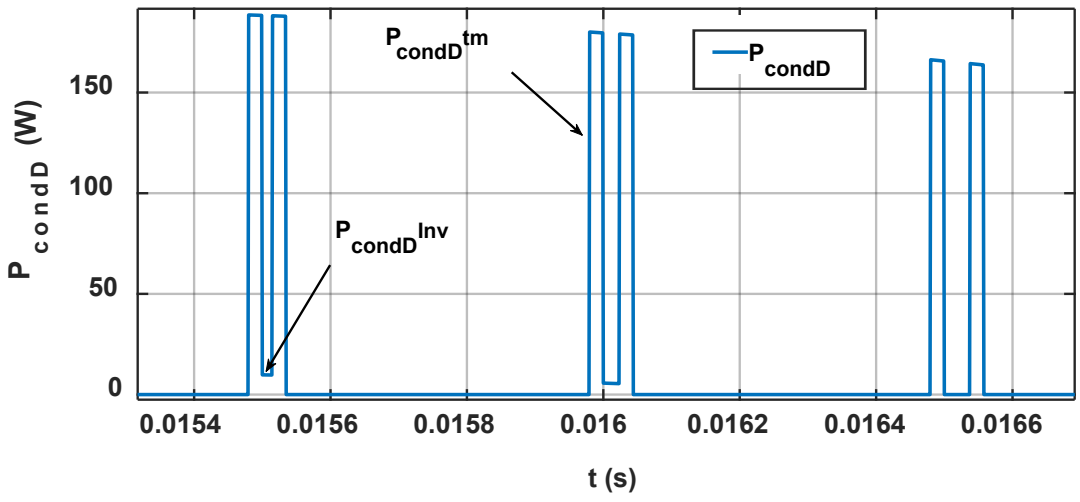


Fig. 2.14: Conduction losses of the Schottky diode (highlight on Fig. 2.13)

2.3.2.5. Electro-thermal coupling

The electro-thermal coupling is much more important in the case of MOSFET than in the case of IGBT, in particular for $R_{DS_{on}}$. Figures 2.15 to 2.17 show the temperature dependence of parameters E_O, R_D and $R_{DS_{on}}$ respectively. Note that this latter also depends on the current I_T, thus Fig. 2.17 shows its variation as a function of both the current and the junction temperature [83]. By applying the electro-thermal coupling, these parameters can be fitted with polynomial equations of the 3rd order. As a matter of fact, that leads to obtain very long equations for the power losses, that's why they won't be presented here.

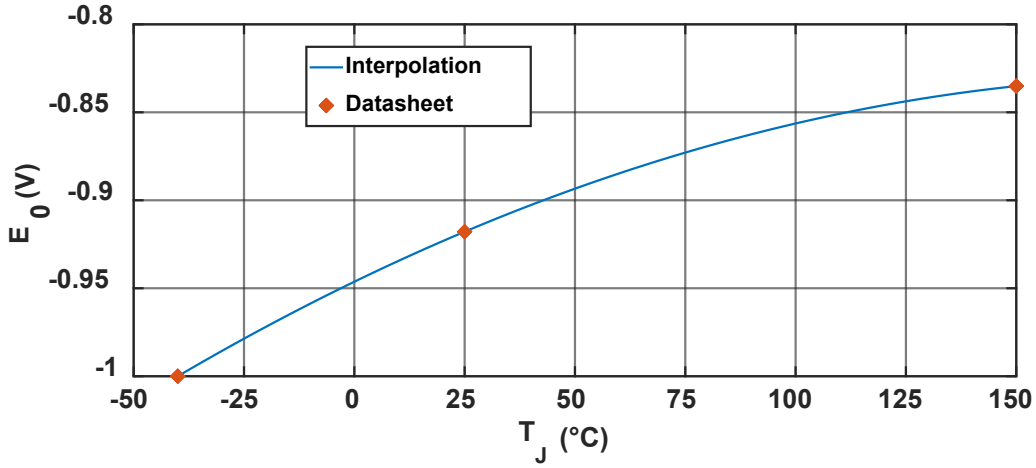


Fig. 2.15: Diode's threshold voltage as a function of the junction temperature, issued from the datasheet and from interpolation respectively

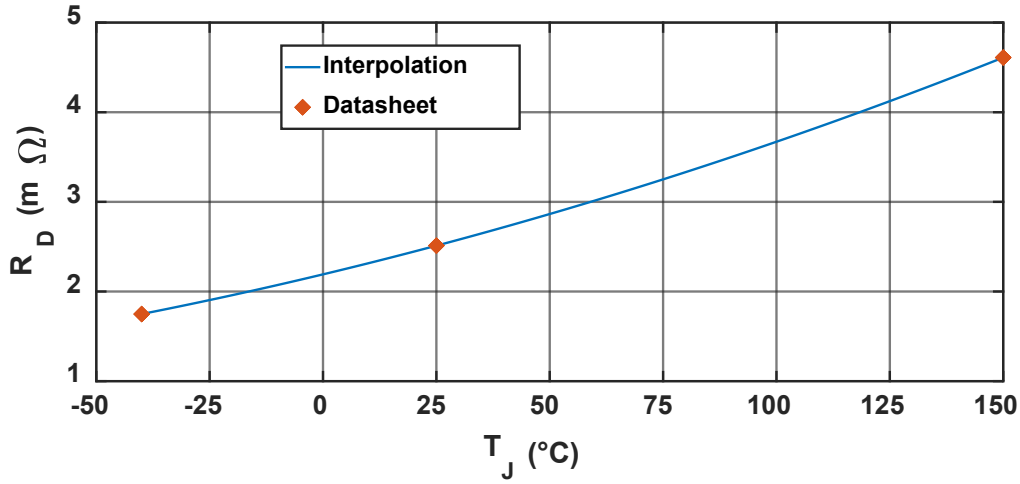


Fig. 2.16: Diode's internal resistance as a function of the junction temperature, issued from the datasheet and from interpolation respectively

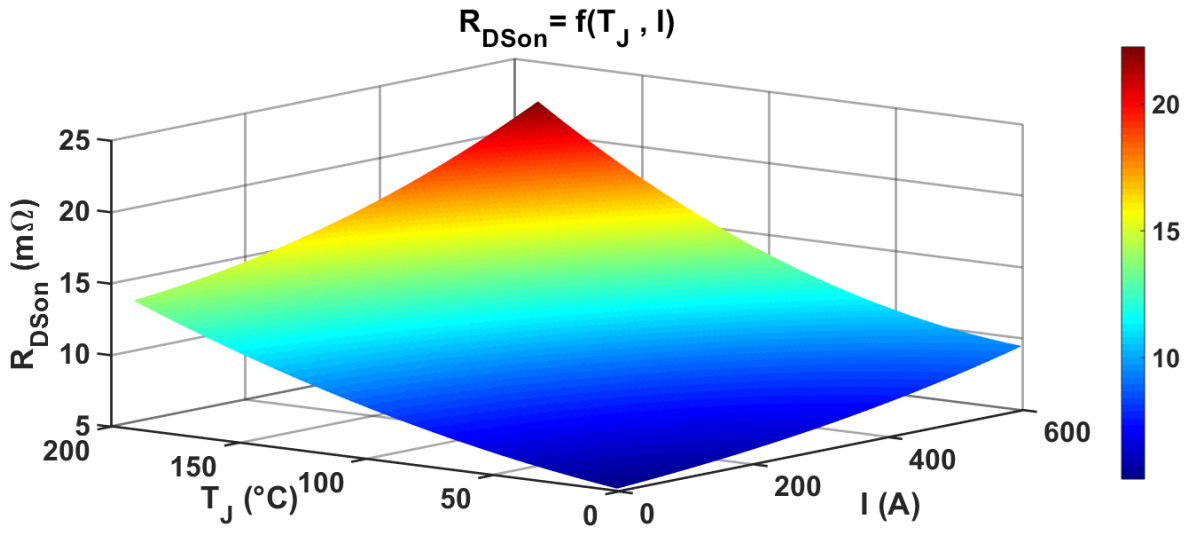


Fig. 2.17: On-state resistance of the MOSFET as a function of both the junction temperature and the current

2.4. Switching losses estimation

2.4.1. Extraction of datasheet's switching losses

2.4.1.1. Transistor's turn-on and turn-off energy losses

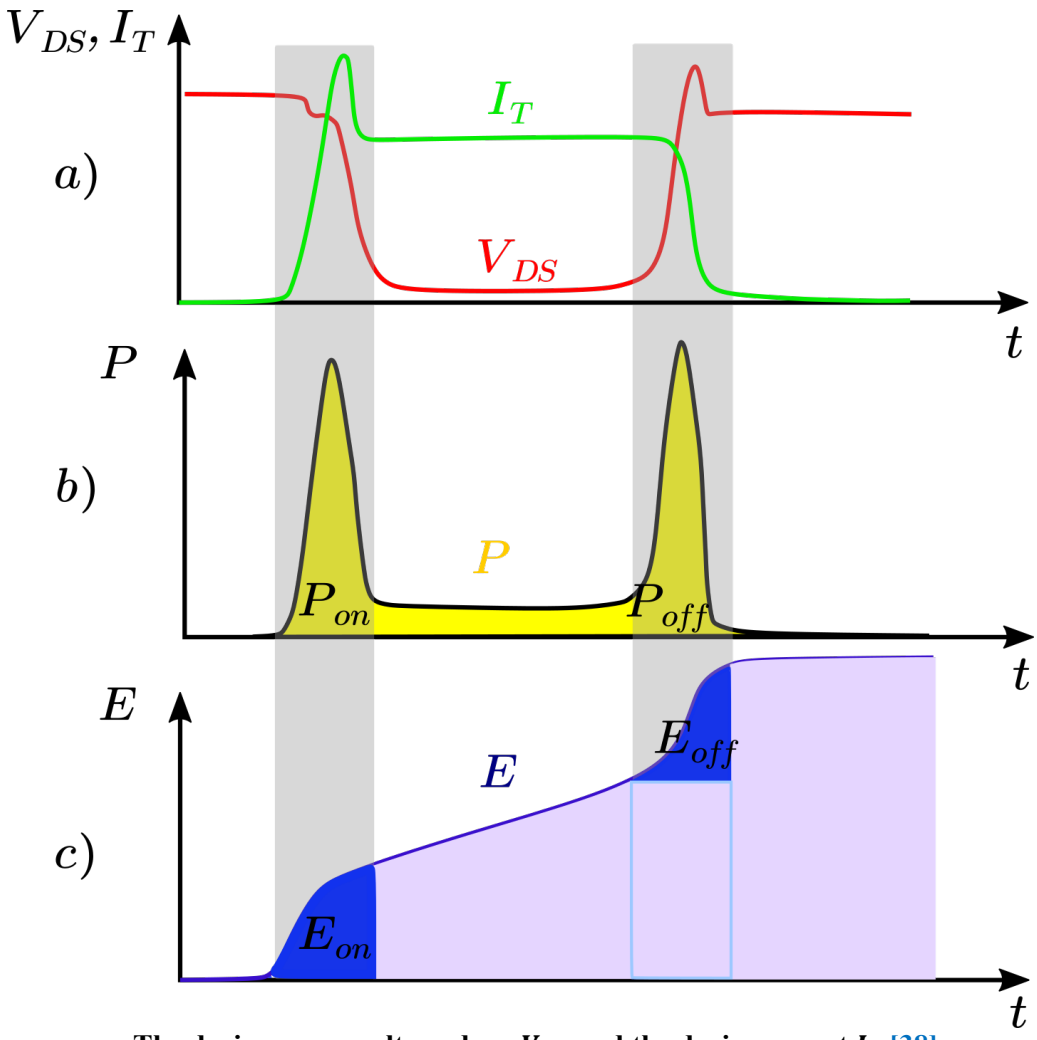
Switching energy losses represent the dissipated energy during the turn-on and the turn-off of the semiconductors. For given control parameters and neglecting parasitic effects, turn-on and turn-off power losses (P_{on} and P_{off}) are dependent on the load current and the electrical load type, the DC-link voltage, the junction temperature and the switching frequency [38]. Fig. 2.18 represents the switching operation, where Fig. 2.18.a. represents the drain-source voltage drop V_{DS} and the drain current I_T (in the case of a MOSFET). Fig. 2.18.b represents the turn-on and turn-off power losses, and Fig. 2.18.c. represents the cumulative energy losses. The general form of the instantaneous power losses during switching can be expressed as follows:

$$P_{\frac{on}{off}}(t) = V_{DS}(t) \cdot I_T(t) \tag{2.26}$$

Accordingly, the energy losses can be expressed as follows:

$$E_{\frac{on}{off}}(t) = \int_{t_{\frac{on}{off}}} P_{\frac{on}{off}}(t) = \int_{t_{\frac{on}{off}}} V_{DS}(t) \cdot I_T(t)\, dt \tag{2.27}$$

where t_{on} is the turn-on time and t_{off} the turn-off time .The turn-on and turn-off energy losses E_{on} and E_{off} can be either extracted directly from the power modules datasheet, or calculated indirectly using other parameters provided in the datasheet [84] [85] [86] [87].



a. The drain-source voltage drop V_{DS} and the drain current I_T [38]

b. The turn-on and turn-off power losses.

c. The cumulative energy losses.

Fig. 2.18: Switching Operation

2.4.1.2. Diode's reverse recovery energy

The recovered charge is the total charge which flows from the diode to the outer circuit, after having switched over from a defined forward current load to a defined reverse current load. This charge depends on the rate of fall of the decaying current $-dI_f/dt$, the mean forward current I_{f_M} effective at the point of switching, and the virtual junction temperature [38]. Fig. 2.19 represents the diode's reverse recovery energy E_{rec} given by:

$$E_{rec} = \int_{t_{rr}} V_D . I_D \, dt \tag{2.28}$$

whereas the reverse recovery power losses P_{rec} by:

$$P_{rec} = E_{rec} . f_{sw} \tag{2.29}$$

where t_{rr} is the reverse recovery time, V_D the voltage measured across the diode, I_D measured in the diode, and f_{sw} the switching frequency [38] [87] [88]. E_{rec} is usually given in the manufacturer's datasheet.

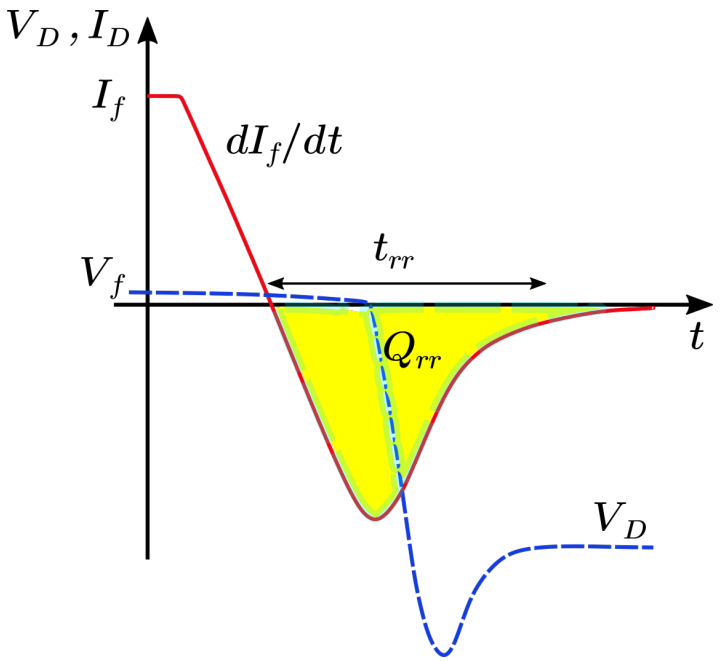


Fig. 2.19: The diode's reverse recovery energy [38]

2.4.2. Switching losses measurement using double pulse test

2.4.2.1. Justification for the use

A more accurate method for estimating the transistor's switching power losses, and the diode's reverse recovery power losses is by directly measuring them while switching the power module. Usually, the switching processes are affected by the parasitic connection inductances present in the components and connections, and generated by connecting transistor chips in power modules. They induce transient overvoltages and may cause oscillations due to the circuit and transistor capacitances [38]. Given that, the values of E_{on}, E_{off} and E_{rec} provided in datasheets may not be accurate enough for the study.

As mentioned before, in the case of a SiC MOSFET power module with an antiparallel SiC Schottky diode, the recovery losses in the Schottky diode are negligible, since the corresponding recovering energy E_{rec} is almost zero [79]. Meanwhile, in the case of a SiC MOSFET power module without an antiparallel diode, the body diode was found to dissipate non-negligible switching losses in the transistor. Despite this, the reverse recovering energy of the MOSFET's body diode was found in various recent studies to be comparable to that of the Schottky diode [80] [81] [82].

In order to verify this theory, and to have more accurate values of E_{on} and E_{off}, the double pulse test was applied on the *Microsemi*'s device *APTMC120AM16D3AG*, a phase-leg 1200V-136A SiC MOSFET power module without antiparallel Schottky diodes. The E_{rec}'s value of the MOSFET's intrinsic body diode is not provided in the datasheet, thus it is crucial to measure it given that this power module will be used at a later stage during the accelerated ageing tests.

2.4.2.2. Test's description

The double pulse test's electrical circuit is represented in Fig. 2.20, where the MOSFET power module (phase-leg) is tested inside the inverter which will be used later on during the ageing test, in order to obtain exactly the same switching and recovery losses. In this figure, E is the bus voltage source, C_{bus} the DC bus link capacitors, C_{dec} the decoupling capacitors and TSCT is a Two Stages Current Transformer. In short, the double pulse test incorporates applying two consecutive pulses on the gate driver's voltage V_{dr} of the low side MOSFET T_l, while the high side MOSFET T_h is kept blocked, using a battery in reverse between the gate and the source [89] [90].

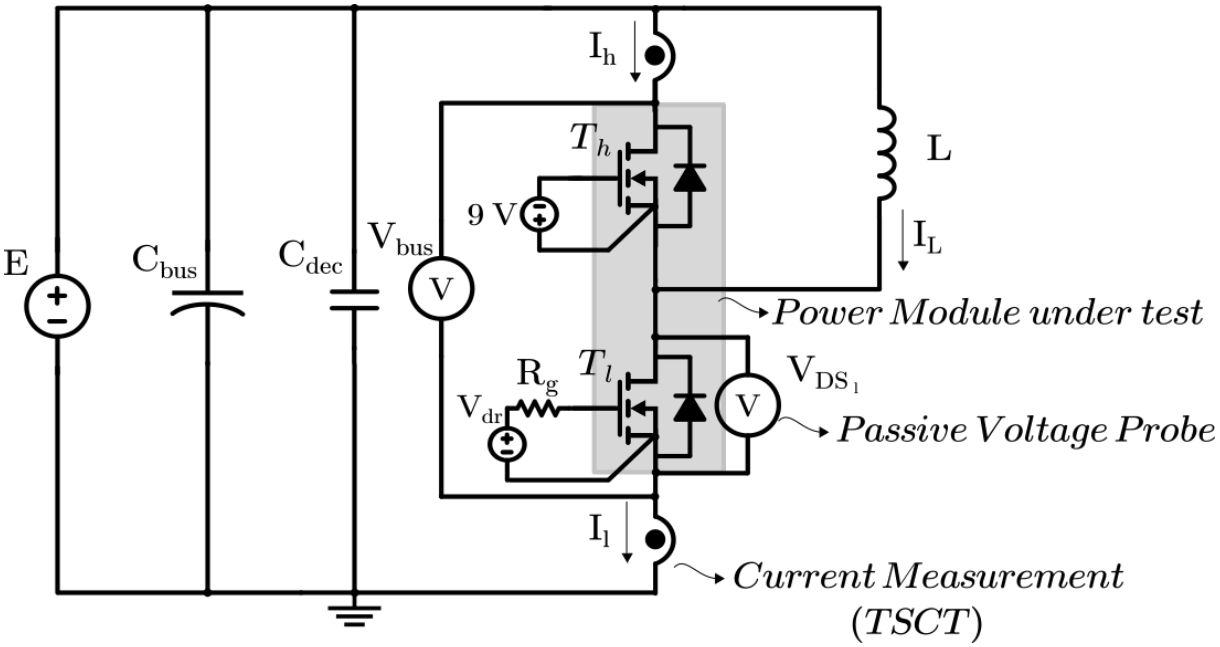


Fig. 2.20: The double pulse test's electrical circuit

Fig. 2.21 represents the sequence of the V_{dr} pulses with the correspondent typical profiles of the voltage across the low side MOSFET V_{DS_l}, the low side MOSFET's current I_l, the high side MOSFET's current I_h and the load's current I_L, where:

- **a)** The 1st pulse must be long enough to establish the desired current value I_L in the inductive load L.
- **b)** Turning-off the 1st pulse blocks the low side MOSFET T_l, and its turn-off losses can be thus estimated.
- **c)** The current in the load passes through the free-wheeling body diode of the high side MOSFET T_h, and the turn-on losses of the diode can be estimated (usually neglected).
- **d)** The 2nd pulse is a shorter one, resulting in reverse recovery losses in the high side diode, while the current overshoots in the low side MOSFET. Thereby, the reverse recovery losses of the high side diode and the turn-on losses of the low side MOSFET can be estimated.

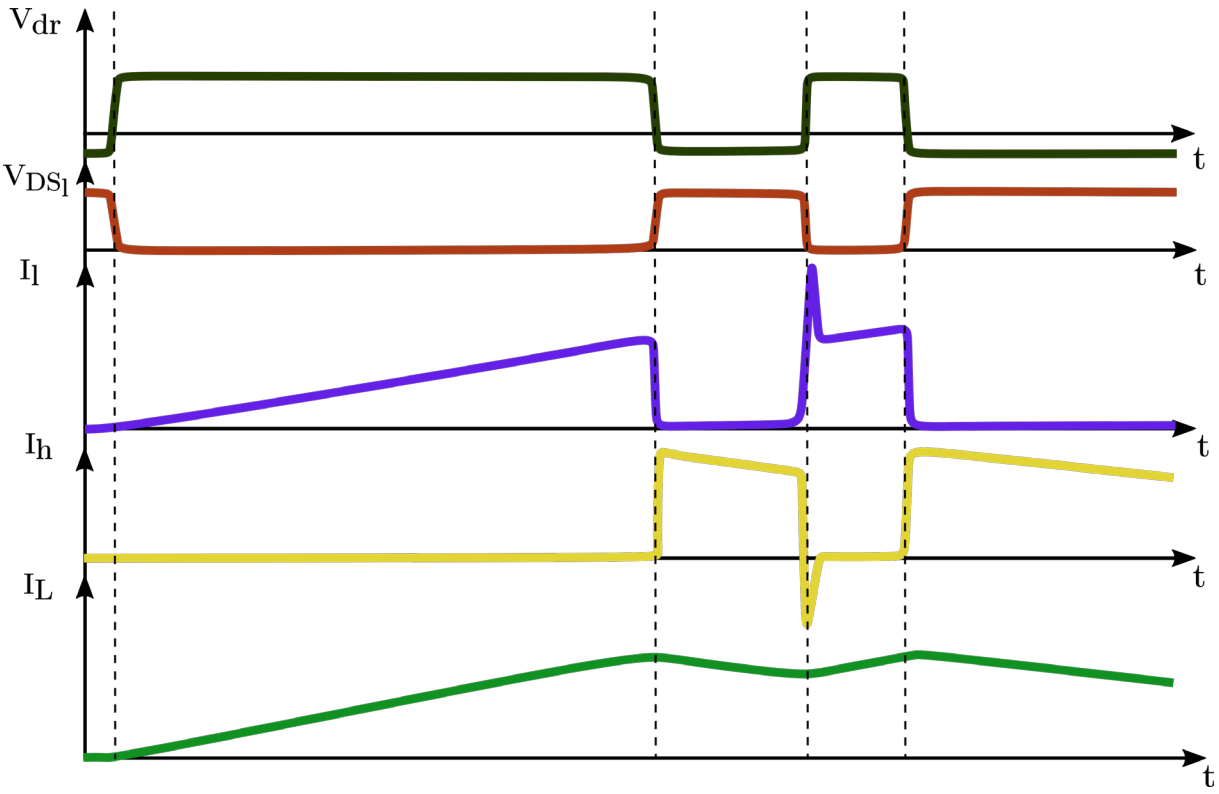


Fig. 2.21: The corresponding graphs of the double pulse test

2.4.2.3. Test's application

As mentioned above, the chosen DUT is the *APTMC120AM16D3AG*, a phase-leg SiC MOSFET power module without antiparallel Schottky diodes. The voltage source is $E = 750\ V$, the inductance value $L = 380\ \mu H$ and the external gate resistances $R_{g_{on}} = R_{g_{off}} = 10\ \Omega$, while the high side MOSFET T_h is kept blocked with a $9\ V$ battery ($V_{GS} = -9\ V$).

Primarily, the double pulse test (DPT) has several advantages such as the fast measurement duration (thus keeping a fixed junction's temperature), obtaining the turn-on and the turn-off losses separately, and having a simple test setup, using 2 current and voltage probes for the measurement. Nevertheless, this test presents some complexities, such as the need for wide bandwidth current and voltage probes, the need for the insertion of a current sensor in the switching cell (hence increasing the inductance stray), and the existence of a phase shift between the probes [91] [92].

2.4.2.3.1. Voltage probe's bandwidth

LECROY passive voltage probes of $2\ kV$, $50\ M\Omega$ with a wide bandwidth $BW = 400\ MHz$, were used to measure the voltages V_{bus} and V_{DS_l} (Fig. 2.20), without the need for a more expensive voltage probe, since the bandwidth of the measured signal is lower than $500\ MHz$ [93] (V_{bus} is different than E due to overvoltages at power module terminals). The passive probe used during the DPT was adjusted as shown in Fig. 2.22 in order to reduce the stray inductance in the measurement circuit.

Fig. 2.22: The adjusted passive voltage probe

2.4.2.3.2. The current measurement method

The current measurement can be usually done with a Pearson current monitor [94], a Rogowski coil [95] or with coaxial current shunt [96]. The coaxial current shunt has the highest bandwidth (up to several Giga Hertz) but it does not provide galvanic isolation. On the other hand, the Pearson current monitor has a galvanic isolation but a lower bandwidth than that of the coaxial current shunt. The shortcoming of the Pearson current monitor is relatively its large physical size which introduces large stray inductance. Although Rogowski coil does not have the physical size problem, however, it has a limited bandwidth (around 30 MHz). Consequently, those three current sensors are not adequate for the accurate current measurement for wide-band gap devices, having high switching speed with a current's rise time of around 20 ns.

Therefore, in order to measure the current properly, the method presented in [97] was applied, consisting of adding a second CT (Current Transformer) stage to a Pearson current monitor. The chosen additional CT is made of a $4F1$ high-frequency ferrite core ($NiZn$ material) and is thinner than the Pearson current monitor. This flat CT composed of 18 turns into a single layer winding forms the primary stage of the TSCT (Two Stage Current Transformer) shown in Fig. 2.23, and introduces a minimum amount of stray inductance in the switching cell. CT_2 is a Pearson Current Monitor 2877 model ($300\,Hz < BW < 200\,MHz\ @3dB\ and\ t_{rise} = 2\,ns$) with a single turn winding in the primary side [91].

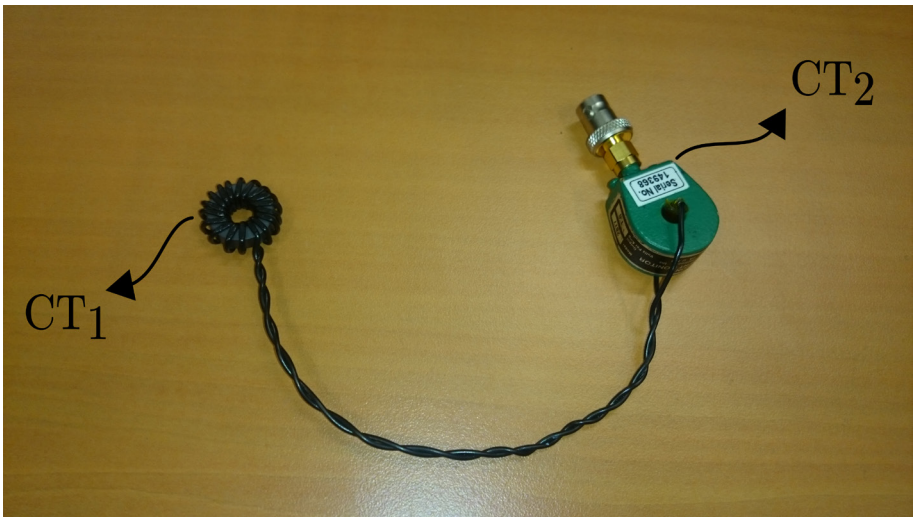


Fig. 2.23: The used TSCT

2.4.2.3.3. Eliminating the skew between probes

The phase shift between probes also known as skew results from the difference in the probes' frequency behaviors and from the reflection phenomena. To eliminate this skew the method proposed in [94] is applied, consisting in measuring the current and the voltage across a none-inductive resistor with the different used probes, using a special PCB circuit. Since the measurement of the switching losses is extremely sensitive to the delay between the current and the voltage signals as being demonstrated in [98] and [99], the elimination of this skew is highly recommended before applying the DPT [91].

2.4.2.3.4. The test bench

The double pulse test bench is presented in Fig. 2.24, where the DUT is fixed on a thermal baseplate controlled with a water heatsink, and connected to an air inductance of 380 μH.Furthermore, a *dSpace* controller was used to apply adjustable pulses, and an oscilloscope to measure and save the probes' signals. Fig. 2.25 highlights the test bench installed in a high voltage secured room, where the heatsink, the *dSpace*, the oscilloscope and the voltage source are all controlled from outside, as shown in Fig. 2.26.

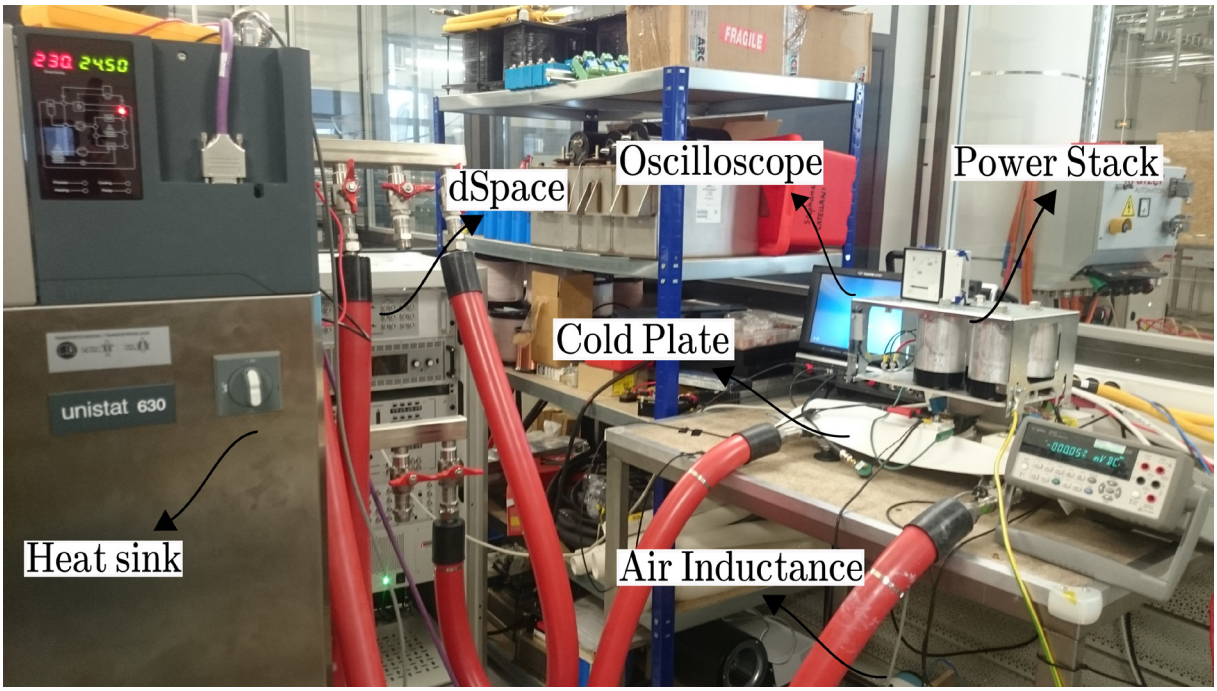


Fig. 2.24: The double pulse test bench

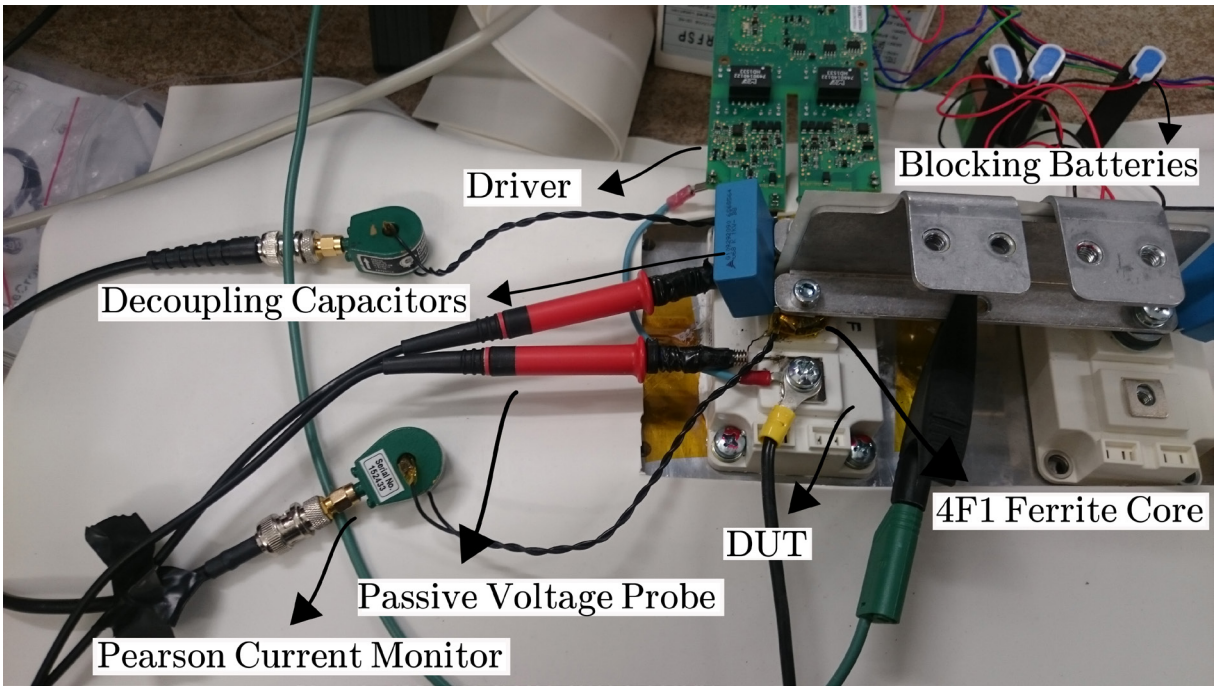


Fig. 2.25: Highlight on the double pulse test bench

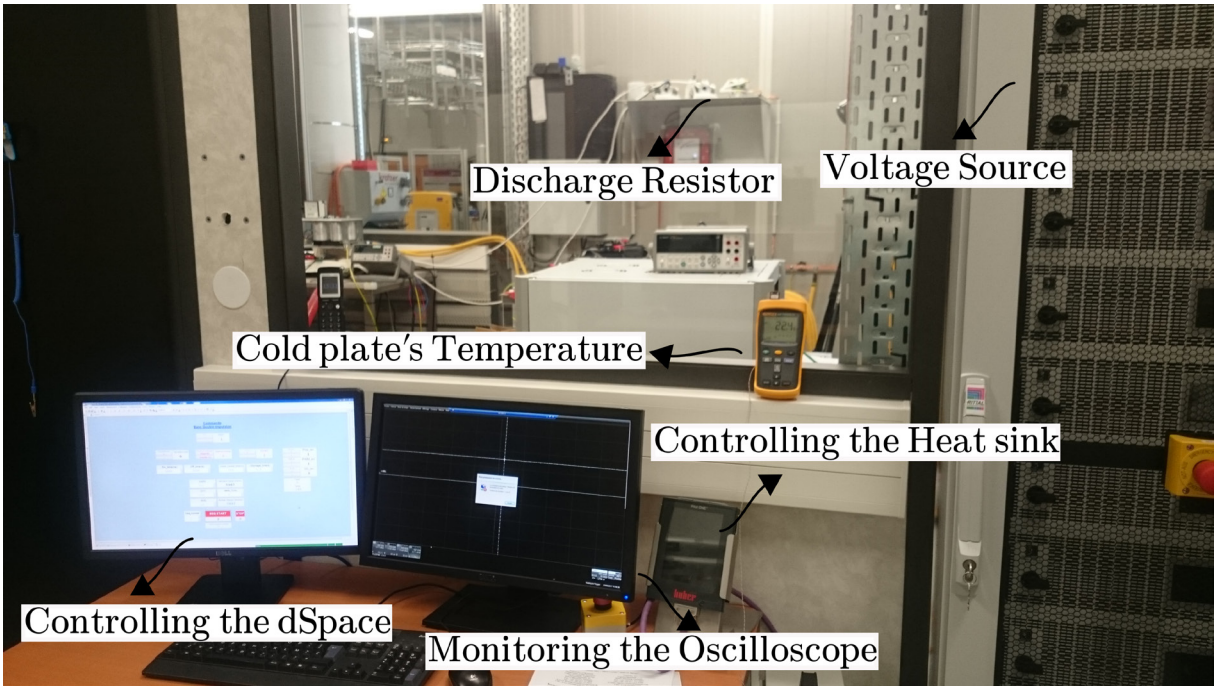


Fig. 2.26: Control and monitoring of the test bench

2.4.2.4. Results

In order to obtain the switching energy losses as a function of the current and the junction temperature, the tests were applied for the following load current values: $I_L = 10A, 30A, 45A, 60A, 90A, 120A$, and for two junction temperatures: $T_J = 25°C$ and $100°C$. At thermal equilibrium, the junction temperature can be estimated by measuring the thermal baseplate's temperature directly under the dies, using a thermocouple.

Fig. 2.27 and Fig. 2.28 represent an example of the waveforms of V_{DS_l}, I_l and the corresponding turn-on power losses P_{on_l} and turn-off power losses P_{off_l} respectively, of the low side MOSFET T_l as a function of time, for $I_L = 120A$ and $T_J = 25\,°C$. The observed overshoot on V_{DS_l} over E results mainly from the parasitic inductances in the commutation circuit. It grows in proportion to the increasing turn-off speed $-dI_l/dt$ of the MOSFET [38].

Similarly, Fig. 2.29 represents an example of the waveforms of V_{DS_h}, I_h and the corresponding reverse recovery power losses P_{rec_h} of the high side MOSFET's body diode as a function of time, for $I_L = 10A$ and $T_J = 100\,°C$. V_{DS_l} is the drain-source voltage of the high side MOSFET T_h, calculated as follows:

$$V_{DS_h} = V_{bus} - V_{DS_l} \tag{2.30}$$

The real values of the voltage and the power losses are adjusted in Fig. 2.27, Fig. 2.28 and Fig. 2.29, in order to fit them in the same graph properly according to the current.

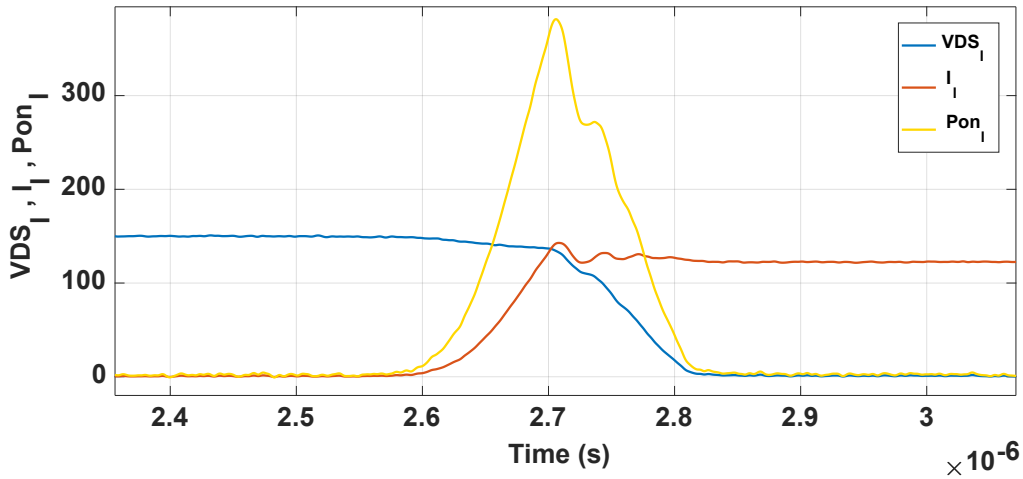


Fig. 2.27: The waveforms of V_{DS_l}, I_l and P_{on_l} as a function of time

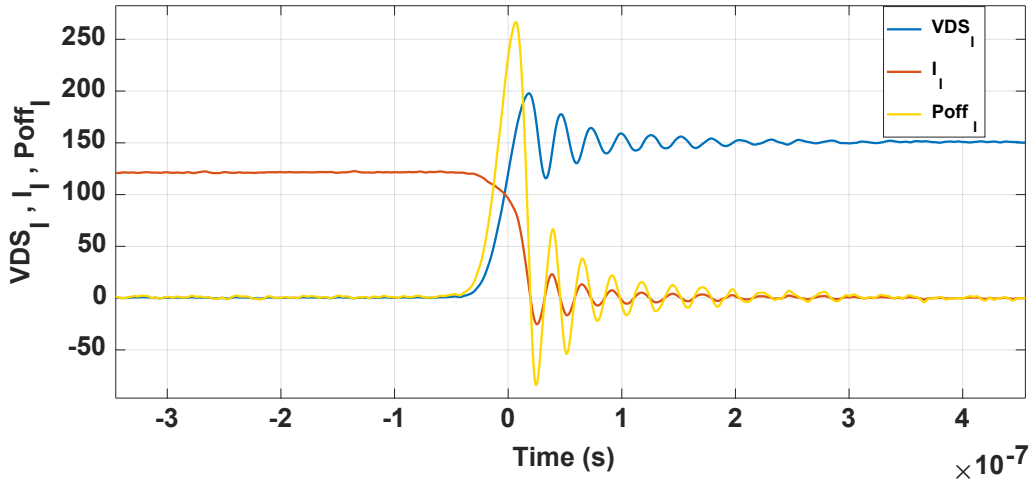


Fig. 2.28: The waveforms of V_{DS_l}, I_l and P_{off_l} as a function of time

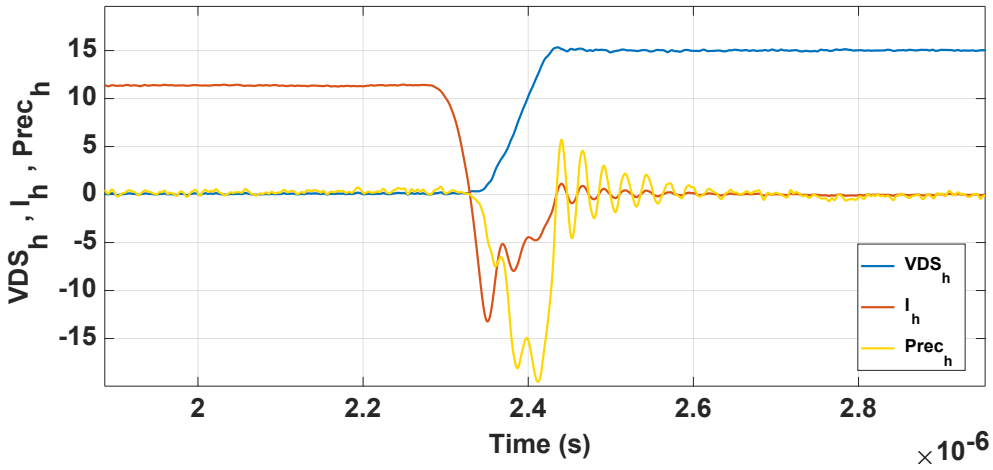


Fig. 2.29: The waveforms of V_{DS_h}, I_h and P_{rec_h} as a function of time

Accordingly, it is now possible to estimate E_{on}, E_{off} and E_{rec} as described in Section 2.4.1. Fig. 2.30 represents the turn-on energy losses as a function of the low side current ($E_{on} = f(I_l)$) for $T_J = 25°C\ and\ 100°C$, while Fig. 2.31 represents them as a function of the low side current and the junction temperature ($E_{on} = f(I_l, T_J)$). The turn-off losses are represented in the same way in Fig. 2.32 and Fig. 2.33.

Using *Matlab*'s fitting tool, the obtained E_{on} can be expressed as follows:

$$E_{on} = p_{00n} + p_{10n} \cdot I_L + p_{01n} \cdot T_J + p_{20n} \cdot I_L^2 + p_{11n} \cdot I_L \cdot T_J + p_{30n} \cdot I_L^3 + p_{21}n \cdot I_L^2 \cdot T_J \quad (2.31)$$

and E_{off} as follows:

$$E_{off} = p_{00f} + p_{10f} \cdot I_L + p_{01f} \cdot T_J + p_{20f} \cdot I_L^2 + p_{11f} \cdot I_L \cdot T_J + p_{30f} \cdot I_L^3 + p_{21f} \cdot I_L^2 \cdot T_J + p_{40f} \cdot I^4 + p_{31f} \cdot I^3 \cdot T_J \quad (2.32)$$

where p_{ijn} and p_{ijf} are the polynomial fitting parameters. Similarly, Fig. 2.34 represents the reverse recovery energy losses as a function of the high side current ($E_{rec} = f(I_h)$) for $T_J = 25°C$ and $100°C$. It can be noticed that E_{rec} of the MOSFET's body diode are very low compared to E_{on} and E_{off}, and thus will be neglected.

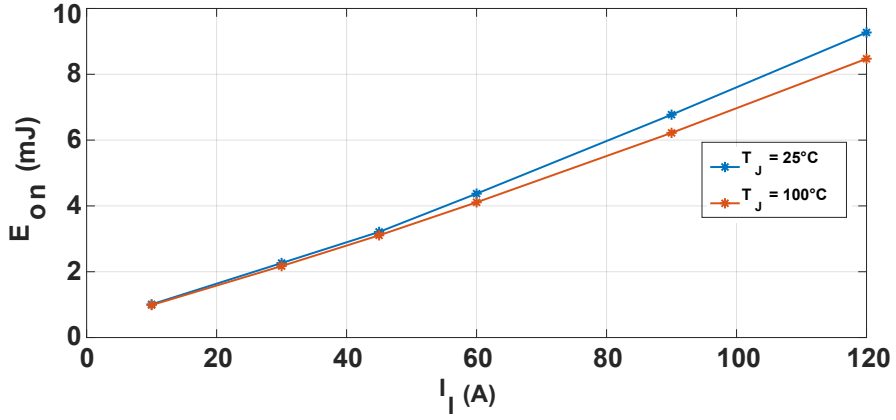


Fig. 2.30: The turn-on energy losses as a function of the low side current ($E_{on} = f(I_l)$) for $T_J = 25°C$ and $100°C$

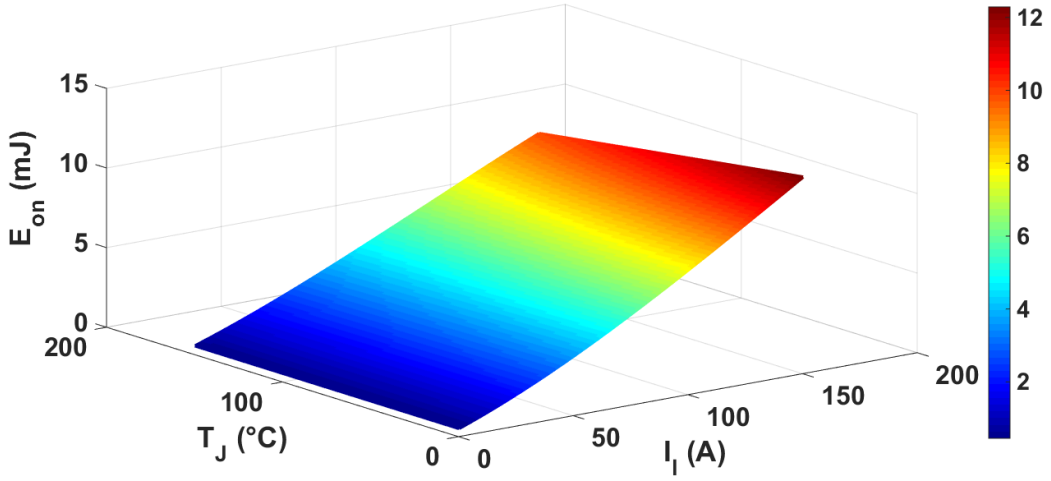


Fig. 2.31: The turn-on losses as a function of the low side current and the junction temperature ($E_{on} = f(I_l, T_J)$)

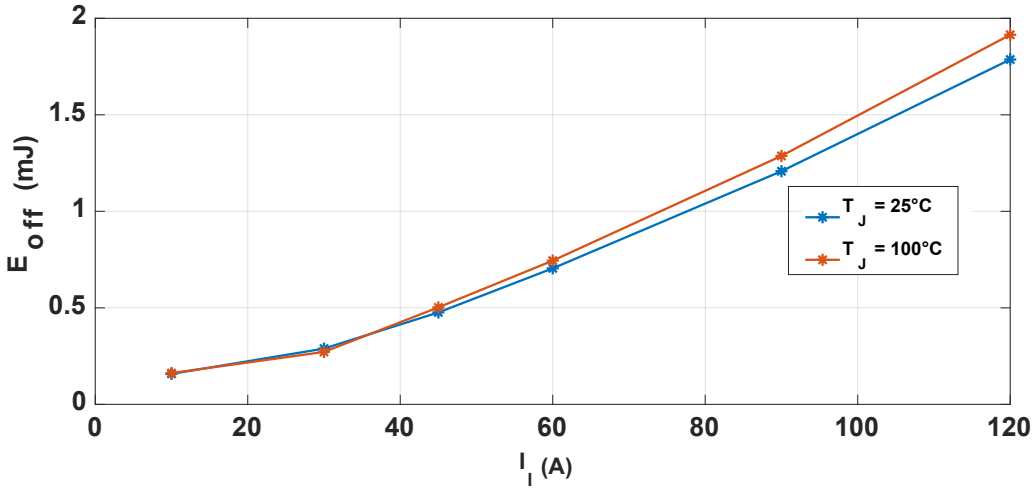


Fig. 2.32: The turn-off energy losses as a function of the low side current ($E_{off} = f(I_l)$) for $T_J = 25°C$ and $100°C$

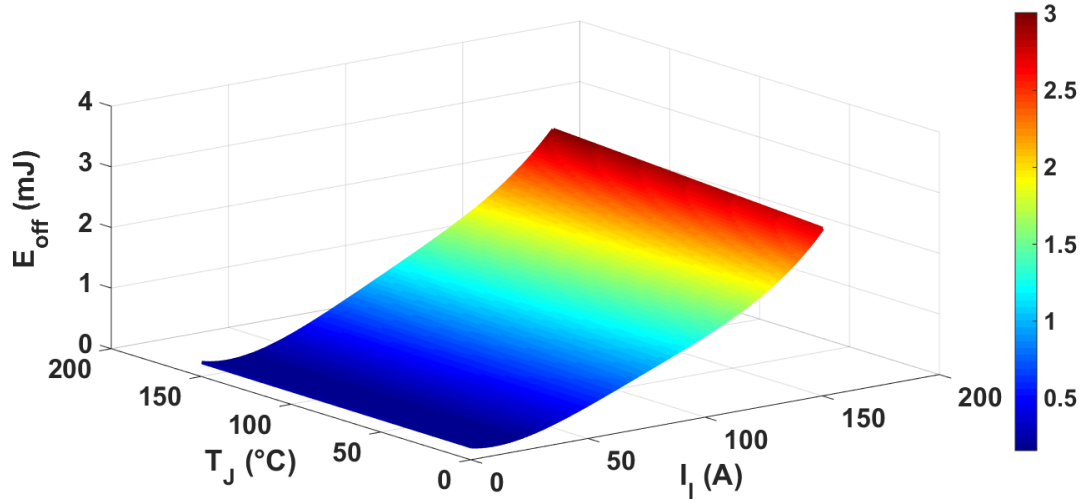


Fig. 2.33: The turn-off losses as a function of the low side current and the junction temperature ($E_{off} = f(I_l, T_J)$)

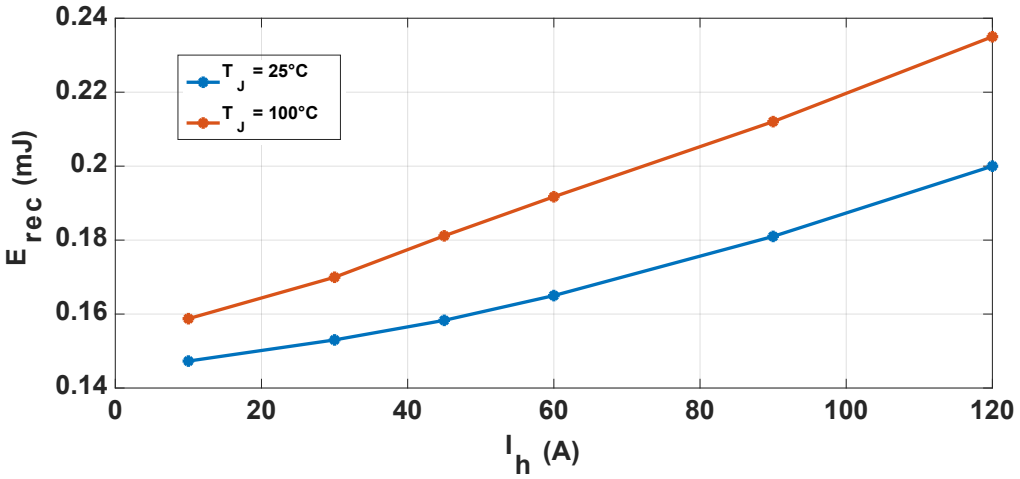


Fig. 2.34: The reverse recovery energy losses as a function of the high side current ($E_{rec} = f(I_h)$) for $T_J = 25°C$ and $100°C$

2.4.3. Case of a PWM voltage inverter

2.4.3.1. The transistor's switching losses

In the case of an IGBT or a MOSFET power module, the transistor only switches during the positive half cycle of the load current I_L. Hence, the average switching losses of the transistor on T_{out} can be demonstrated as follows:

$$P_{sw_T} = \frac{1}{T_{out}} \int_0^{\frac{T_{out}}{2}} (E_{on} + E_{off}) \cdot f_{sw} \tag{2.33}$$

Similarly to Section 2.3.1.5, by considering the electro-thermal coupling of E_{on} and E_{off}, as well as their dependencies of the DC-link voltage E and the switch RMS (Root Mean Square) current I_{RMS}, Eq. 2.33 becomes [38]:

$$P_{swT} = f_{sw} \cdot \left(E_{on_0} + E_{off_0}\right) \cdot \frac{\sqrt{2}}{\pi} \cdot \left(\frac{I_{RMS}}{I_0}\right)^{K_{i_T}} \cdot \left(\frac{E}{E_0}\right)^{K_{vT}} \cdot (1 - TC_{E_{sw}} \cdot (T_{J_0} - T_J)) \tag{2.34}$$

where K_{v_T} and K_{i_T} are exponents for the voltage and the current dependencies of the transistor's switching losses ($\cong 1.3 \ldots 1.4$. for the IGBT) respectively. $TC_{E_{sw}}$ is the temperature coefficient of the switching losses ($\cong 0.003\ 1/K$ for the IGBT), and T_{J_0}, I_0, E_0, E_{on_0} and E_{off_0} represent the rated or reference junction temperature, switch RMS current, DC-link voltage, turn-on and turn-off energies respectively. These parameters can be extracted from the manufacturer's datasheets. However, in the case of the MOSFET power module, the values of E_{on} and E_{off} obtained in Eq. 2.31 and Eq. 2.32 respectively were directly inserted in Eq. 2.33. Fig. 2.35 represents the switching power losses of the MOSFET on T_{out}.

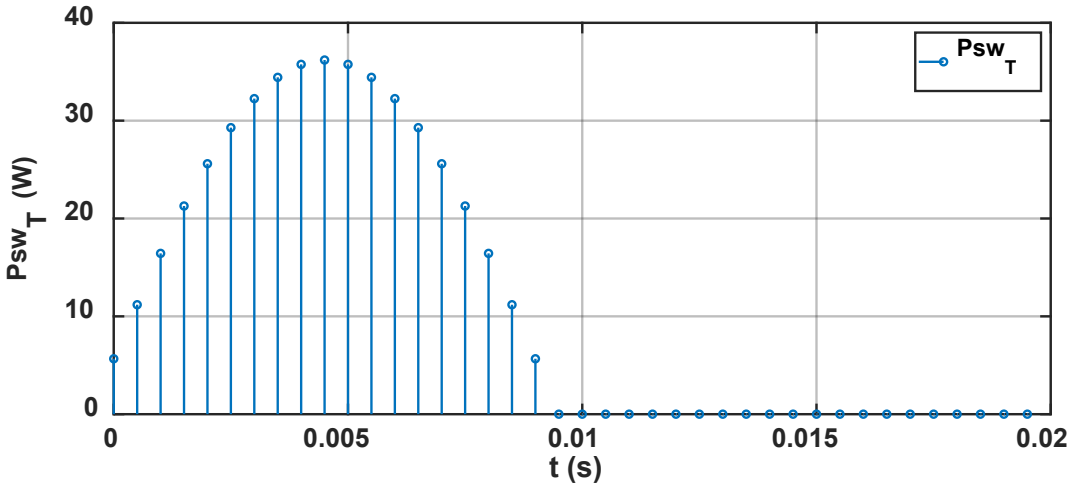


Fig. 2.35: Switching power losses of the MOSFET on T_{out}

2.4.3.2. The diode's losses

Similarly, the diode's switching losses can be estimated as follows:

$$P_{sw_D} = \frac{1}{T_{out}} \int_{\frac{T_{out}}{2}}^{T_{out}} E_{rec} \cdot f_{sw} \tag{2.35}$$

where E_{rec} is the recovery energy losses of the diode. By applying the same method to the diode's switching recovery losses, Eq. 2.35 becomes:

$$P_{swD} = f_{sw} \cdot E_{rec_0} \cdot \frac{\sqrt{2}}{\pi} \cdot \left(\frac{I_{RMS}}{I_0}\right)^{K_{i_D}} \cdot \left(\frac{E}{E_0}\right)^{K_{v_D}} \cdot (1 - TC_{E_{rec}} \cdot (T_{J_0} - T_J)) \tag{2.36}$$

where K_{v_D} and K_{i_D} are exponents for the voltage and the current dependencies of the diode's switching losses ($\cong 0.6$ for the IGBT's antiparallel diode) respectively, and $TC_{E_{rec}}$ the temperature coefficient of the recovery losses ($\cong 0.006\,1/K$ for the IGBT's antiparallel diode). E_{rec_0} represents the rated or the reference recovery energy losses of the diode, usually provided in the datasheets. As mentioned before, in the case of the SiC MOSFET power module, the switching losses both in the SiC Schottky diode as well as in the MOSFET's body diode are negligible.

2.5. Validation

2.5.1. Case of IGBT power modules

The power losses model described in the previous sections was implemented using *Matlab*, in pursuance of obtaining for a given current's mission profile, the correspondent power losses' profile. In order to validate this model, it was compared with several simulators such as *PSIM*, *IPOSIM* (*Infineon*) and *SemiSel* (*Semikron*).

PSIM is a software that provides simulation solutions for power electronics applications. It can easily handle power converters and estimate the power losses inside the power modules for a given current value. Fig. 2.36 represents the simulation of the DC/AC inverter with *PSIM*, where the Device Database Editor is a toolbox for power losses estimation that takes into consideration the datasheet's parameters. The conduction and the switching power losses of the transistor and the diode respectively can be easily obtained by measuring the output of this toolbox with ammeters. Thereupon, the output is shown in Fig. 2.37, where the power losses are represented on several fundamental periods T_{out}. Finally, the average values of the power losses on T_{out} were calculated in order to compare them with the *Matlab* model's results.

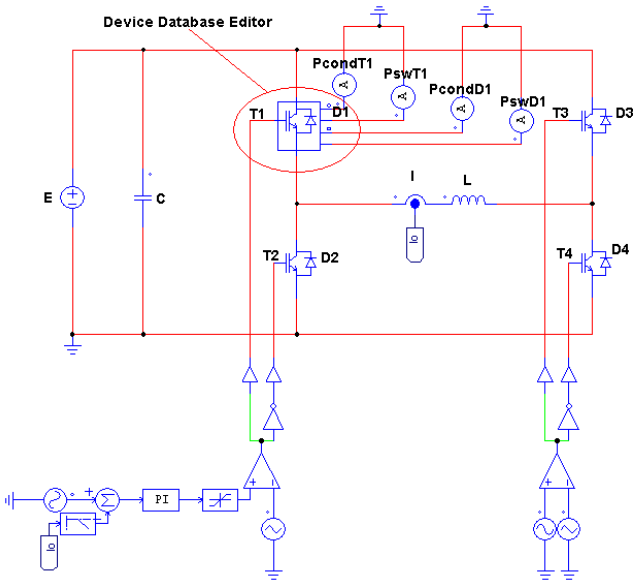


Fig. 2.36: The simulation of the DC/AC inverter with *PSIM*

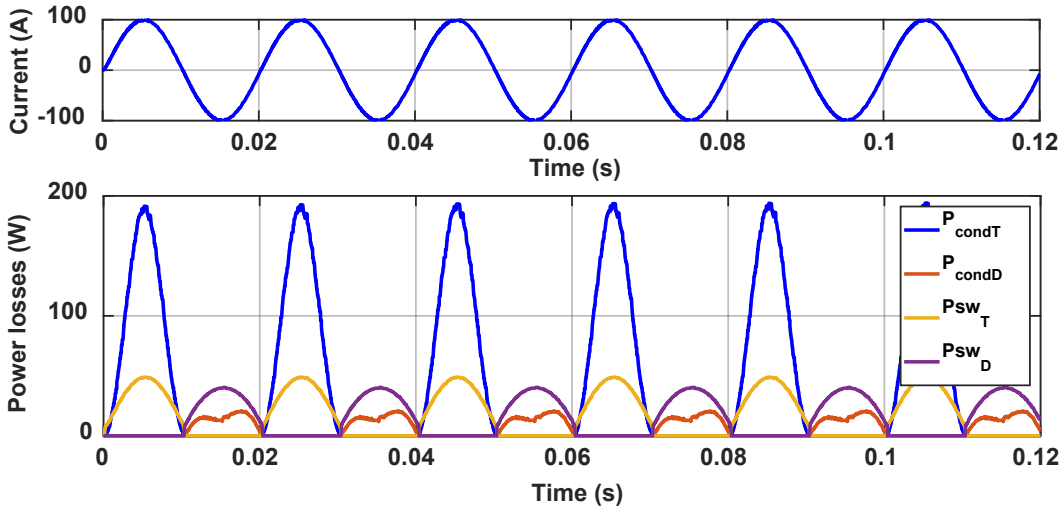


Fig. 2.37: The estimated power losses with *PSIM*

IPOSIM is the other simulator used to validate the *Matlab* model. This online simulator developed by *Infineon* allows estimating the power losses for a chosen power module, as presented in Fig. 2.38 [100].

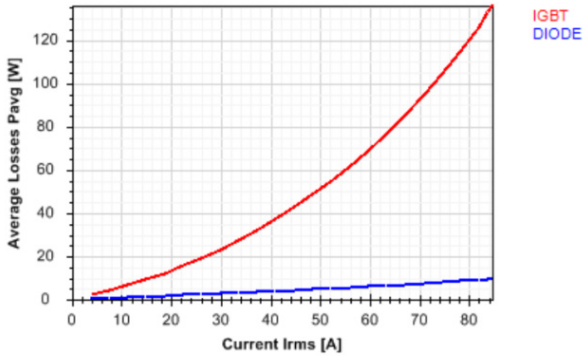


Fig. 2.38: The estimated power losses with *IPOSIM*

In order to compare the three simulators, several simulations were applied to five IGBT power modules. Table 2.3 represents the estimated power losses, corresponding to a load current of $70A\ RMS$, for one of the five IGBTs since the results for the other IGBTs are similar. It can be noticed from Table 2.3 that the obtained values of the mean power losses (estimated on T_{out}) are very close. The slight differences between the results could be due to imprecisions with the data entry of the parameters' values, extracted from the datasheet's curves. The same approach was applied to another IGBT power module *SKM200GB12E4* with *SemiSel*, a *Semikron*'s online design simulator [101], and close results were obtained too for a load current of $200A\ RMS$, as exhibited in Table 2.4. It should be noted, that this phase-leg 1200V-200A IGBT power module will be used later on in this study, during the accelerated ageing tests.

Table 2.3: Comparison of the power losses obtained with the different simulators

$\boldsymbol{Simulator \setminus Power\ Losses}$	$\boldsymbol{P_{cond_T}}$ (W)	$\boldsymbol{P_{cond_D}}$ (W)	$\boldsymbol{P_{sw_T}}$ (W)	$\boldsymbol{P_{sw_D}}$ (W)	$\boldsymbol{P_{tot_T}}$ (W)	$\boldsymbol{P_{tot_D}}$ (W)
$\boldsymbol{IPOSIM}$	50.51	6.34	15.77	14.79	66.28	21.13
$\boldsymbol{PSIM}$	50.301	6.78	16.771	14.679	67.072	21.459
$\boldsymbol{Matlab}$	51.1973	6.6093	15.6842	14.7497	66.8815	21.359
$\boldsymbol{\Delta(IPOSIM - PSIM)\%}$	0.41%	6.94%	6.35%	0.75%	1.19%	1.55%
$\boldsymbol{\Delta(IPOSIM - Matlab)\%}$	1.36%	4.25%	0.54%	0.27%	0.91%	1.08%
$\boldsymbol{\Delta(Matlab - PSIM)\%}$	1.75%	2.58%	6.93%	0.47%	0.28%	0.46%

Table 2.4: Comparison of the power losses obtained with *SemiSel*

$\boldsymbol{Simulator \setminus Power\ Losses}$	$\boldsymbol{P_{cond_T}}$ (W)	$\boldsymbol{P_{cond_D}}$ (W)	$\boldsymbol{P_{sw_T}}$ (W)	$\boldsymbol{P_{sw_D}}$ (W)	$\boldsymbol{P_{tot_T}}$ (W)	$\boldsymbol{P_{tot_D}}$ (W)
$\boldsymbol{Matlab}$	177.31	60.95	113	21.26	291.7	82.21
$\boldsymbol{SemiSel}$	172	59	114.39	21	285	80
$\boldsymbol{\Delta(Matlab - SemiSel)\%}$	3%	3.2%	1.23%	1.22%	2.3%	2.7%

2.5.2. Case of MOSFET power modules

SpeedFit is a free online circuit simulation tool, developed by *WolfSpeed* to help accelerate SiC device evaluation and adoption [102]. This simulator presented in Fig. 2.39 was used to validate the MOSFET's power losses estimation model, applied for the case study presented in Table 2.5.

Table 2.5: Case study

Circuit	$Inverter\ (3ph)$
Input voltage	$1.200\ kV$
Output voltage	$690\ V$
Rated power	$126.8\ kVA$
Switching frequency	$20\ kHz$
Module	$CAS300M17BM2$

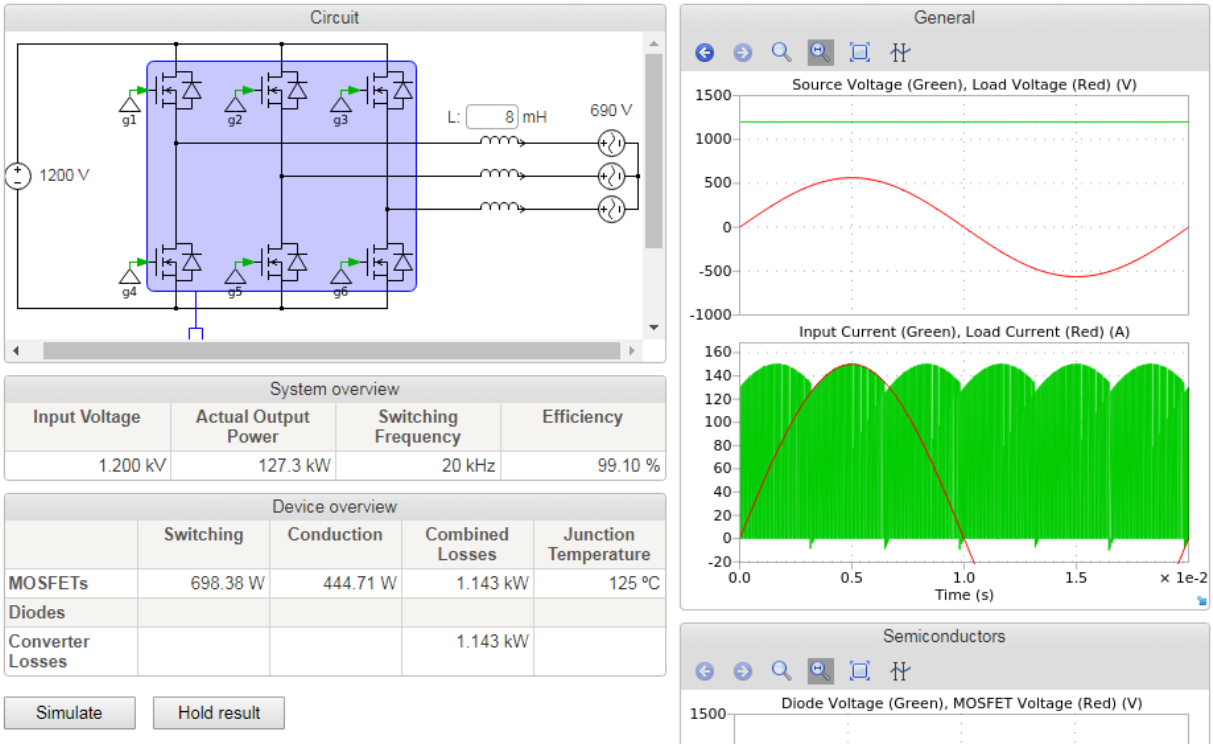


Fig. 2.39: A screenshot on the results of the *SpeedFit* simulator

Table 2.6 represents a comparison between the conduction, switching and total losses estimated by the *Matlab* model and the *SpeedFit* simulator. The results represent the total power losses of all the MOSFET modules in a three phase inverter (total of 6 MOSFETs). It can be noticed from Table 2.6 that the results are very close, with a difference in the total power losses of 2.72%, which validates the *Matlab*'s model. *SpeedFit* does not calculate the power losses in the diode, that's why only the comparison of the MOSFET power losses is represented in Table 2.6.

Table 2.6: Comparison between the simulators results

	Matlab Model	***SpeedFit Simulator***	$\%\Delta P$
$P_{Cond}\ (W)$	420.612	444.71	5.41%
$P_{sw}\ (W)$	691.369	698.38	1%
$P_{Tot}\ (W)$	1111.981	1143.09	2.72%

2.6. Conclusions

This chapter presented the basics of the semiconductors' power losses estimation, in the case of the SiC MOSFET, Si IGBT and diodes. The power losses were estimated for the case of a DC/AC inverter using the Pulse Width Modulation (PWM). Moreover, a detailed description was represented on the operating mode, as well as on the conduction phase of each semiconductor, especially in the case of the SiC MOSFET's operation in the third quadrant.

Initially, the average conduction power losses equations on a fundamental period were detailed, without taking into account the electro-thermal coupling. Then, the equations were updated by considering the electro-thermal coupling of some parameters such as the threshold voltage and on-state resistance. Finally, the conduction power losses were estimated by extracting the equations' parameters from the manufacturer's datasheets.

Furthermore, the average switching power losses were described, and their typical waveforms and equations were elaborated. Usually, these parameters can be extracted either directly or indirectly from the manufacturer's datasheets. However, the switching processes are affected by the parasitic connection inductances present in the components and connections, and generated by connecting transistor chips in power modules. Hence, it was proposed to directly measure the switching energies using the Double Pulse Test (DPT) for the SiC MOSFET power module. This module will be used later on during accelerated ageing tests. The DPT concept, application and results were detailed, where the SiC MOSFET's body diode showed negligible recovery losses.

Afterwards, the equations of P_{on}, P_{off} and P_{rec} were elaborated in the case of a PWM DC/AC inverter, with and without considering the electro-thermal coupling of the switching energies.

Eventually, all the equations of average power losses on a fundamental period were implemented in a *Matlab* model. This model was compared and validated using simulators such as *IPOSIM* (*Infineon*), *SemiSel* (*Semikron*) and *PSIM* in the case of the IGBT module, while *Speedfit* (*Wolfspeed*) was used in the case of the SiC MOSFET module. Already validated, this numerical model will be used at a later stage to estimate the corresponding losses of current's mission profiles over several years, with more than 800 million samples each. The output of this model represents the input of the thermal model depicted in the next chapter.

Chapter 3:
Construction, evaluation and identification of thermal models

Chapter 3: Construction, evaluation and identification of thermal models

3.1. Introduction

The estimation of semiconductors' junction temperature is crucial for choosing suitable thermal management systems and estimating semiconductors' lifetime. In fact, the variations of the junction temperature over time, induced by the current's variations, contribute much to semiconductors degradations [88] [90] [103]. However, the measurement of the semiconductors' junction temperature in on-line conditions is still complicated, thus several alternative methods are used instead for indirectly estimating this temperature. The main methods are for instance the finite element modeling and the numerical modeling using equivalent electrical circuits.

In this chapter, a numerical model (refer to Fig. 1.36) using equivalent Foster circuits will be presented. The output of the power losses estimation model depicted in Chapter 2 corresponds to the input of this thermal model. Furthermore, these two models are coupled together in order to take into account the dependence of some electrical parameters on the junction temperature.

Since the thermal model will be used to estimate the junction temperature of several semiconductors during several months, only the average temperature within a fundamental period T_{out} will be calculated. Furthermore, a comparative study between several computation methods will be represented in order to determine the fastest one. Afterwards, the developed thermal model, using the manufacturers' data, will be validated using several simulators in the case of IGBT and SiC MOSFET power modules.

Eventually, a thermal model based on mutual thermal coupling impedances will be presented. This model will be used at a later stage to experimentally identify the thermal behavior of the semiconductor devices which will be used in the accelerated ageing test benches (Chapters 5 and 6).

3.2. Basics of power assemblies' thermal modeling

3.2.1. Equivalence between thermal and electrical parameters

Usually, the heat transport is based on the following three fundamental mechanisms [104] [105] [106]: thermal radiation, convection and conduction. Thermal conduction is the transfer of heat by microscopic collisions of particles and movement of electrons within a body. It is usually the main heat transfer mechanism in a power module [107]. In an opaque solid, the relation between the heat flux density φ and the temperature T is given by the Fourier law:

$$\vec{\varphi} = -\lambda_{th} \cdot \overrightarrow{grad(T)} \tag{3.1}$$

where λ_{th} represents the thermal conductivity. Similarly, in electrical conduction the relation between the current density J and the electrical potential V can be obtained as follows:

$$\vec{J} = -\sigma \cdot \overrightarrow{grad(V)} \tag{3.2}$$

where σ represents the electrical conductivity. Using the equivalence between these two formulas, the equivalence between thermal and electrical parameters can be obtained as exhibited in Table 3.1.

Fig. 3.1 represents the heat conduction $P(t)$ through a given material, with t representing the time, d the thickness of the material, S the surface area, while $T_x(t)$ and $T_y(t)$ represent the material surfaces' temperatures. Based on the equivalence between electrical and thermal conduction, the material's thermal resistance can be obtained in the case of a one directional heat transfer and without an internal heat source as follows:

$$R_{th} = \frac{d}{\lambda_{th} \cdot S} \tag{3.3}$$

Moreover, Fig. 3.2 represents simultaneously the equivalent electrical and thermal circuits, where C_{th} represents the thermal capacitance in the case of thin objects. The latter is defined by Eq. 3.4 when the temperature is supposedly uniform in the solid.

$$C_{th} = \rho \cdot C \cdot S \cdot d \tag{3.4}$$

where ρ is the density of the material and C is the heat capacity.

Despite the restrictive assumptions for using electrical equivalent circuits (1D heat flux without heat sources for the thermal resistance, and uniform temperature for the thermal capacitance), they remain common tools for the thermal modeling of power assemblies. They are usually constituted by R_{th}-C_{th} networks as it will be presented in the following paragraph.

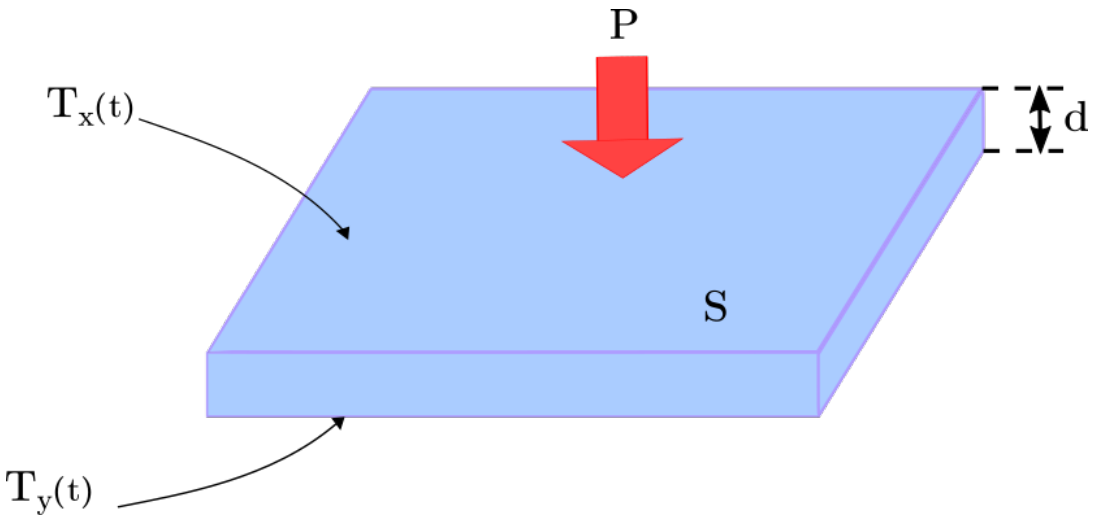


Fig. 3.1: Heat conduction through a given material

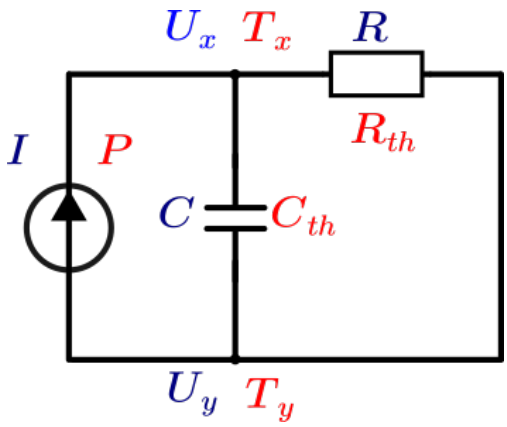


Fig. 3.2: Equivalent electrical and thermal circuits

Table 3.1: Equivalence between thermal and electrical parameters [107]

Thermal Parameters			Electrical Parameters		
Parameter	**Description**	**Unit**	**Parameter**	**Description**	**Unit**
T	Temperature	K	U	Voltage	V
J	Heat flow	W/m^2	J	Current density	A/m^2
P	Heat power losses	W	I	Current	A
Q	Heat amount	$J = W \cdot s$	Q	Charge	$C = A \cdot s$
λ_{th}	Conductivity	$W/(K \cdot m)$	σ	Conductivity	$1/(\Omega \cdot m)$
R_{th}	Resistance	K/W	R	Resistance	$V/A = \Omega$
C_{th}	Capacity	$W \cdot s/K$	C	Capacity	$A \cdot s/V = F$

3.2.2. Cauer and Foster networks

In order to estimate the semiconductors' junction temperature as a function of time, it is possible to use the notion of thermal impedance. This thermal impedance Z_{th} represents the step response of the system considered linear, and therefore describes its thermal behavior during transient [107]. Applied in the simple example illustrated in Fig. 3.1, the thermal impedance can be expressed as follows:

$$Z_{th}(t) = \frac{T_x(t) - T_y(t)}{P} \tag{3.5}$$

In the case of a power module mounted on a heat sink during functioning, the temperature of the die rises due to the power losses. In consequence, the heat flows from the junction in all directions, but mostly in a vertical way down towards the heat sink as represented in Fig. 3.3. Thereby, the heat flows through the different layers of the packaging, until reaching the thermal interface before being dissipated by the heat sink. For modeling this heat transfer mechanism, the most common thermal circuits are the "physical" equivalent circuit, known as Cauer network, and the "mathematical" equivalent circuit known as Foster network [36] [38] [106].

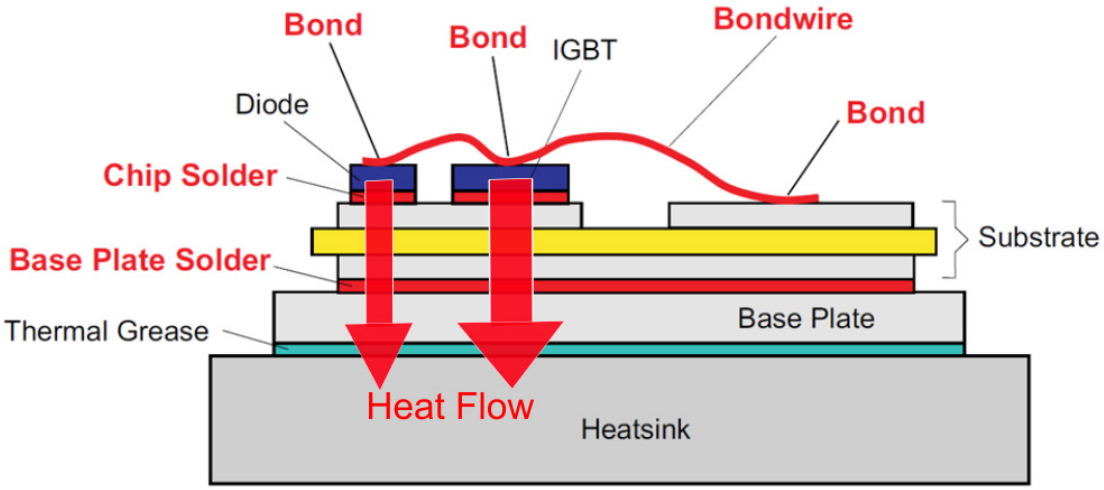


Fig. 3.3: **Heat flows from the junction down towards the heat sink (adapted from [38])**

A. Cauer network

The Cauer network can be obtained by extending the example illustrated in the previous section by series connecting multiple R_{th}-C_{th} cells, corresponding each to a layer in the system, as illustrated in Fig. 3.4. T_J, T_C, T_H and T_a represent the junction, case, heat sink and ambient temperatures respectively, while P represents the power losses in the semiconductor [108]. The thermal impedance of this network, which represents also its transfer function, can be expressed in Laplace-domain by the following complicated form [107]:

$$Z_{th}(s) = \cfrac{1}{s \cdot C_{th_1} + \cfrac{1}{R_{th_1} + \cfrac{1}{s \cdot C_{th_2} + \cfrac{1}{R_{th_2} + \cdots + \cfrac{1}{s \cdot C_{th_i} + \cdots + \cfrac{1}{R_{th_n}}}}}}} \tag{3.6}$$

where R_{th_i} and C_{th_i} represent the thermal resistance and the capacitor of layer i respectively, and n represents the total number of layers in a given system. Note that the values of R_{th}-C_{th} elements in the power module depend faintly on the boundary conditions. Hence, they are slightly dependent on the heat sink technology which constitutes one limit of this thermal modeling approach.

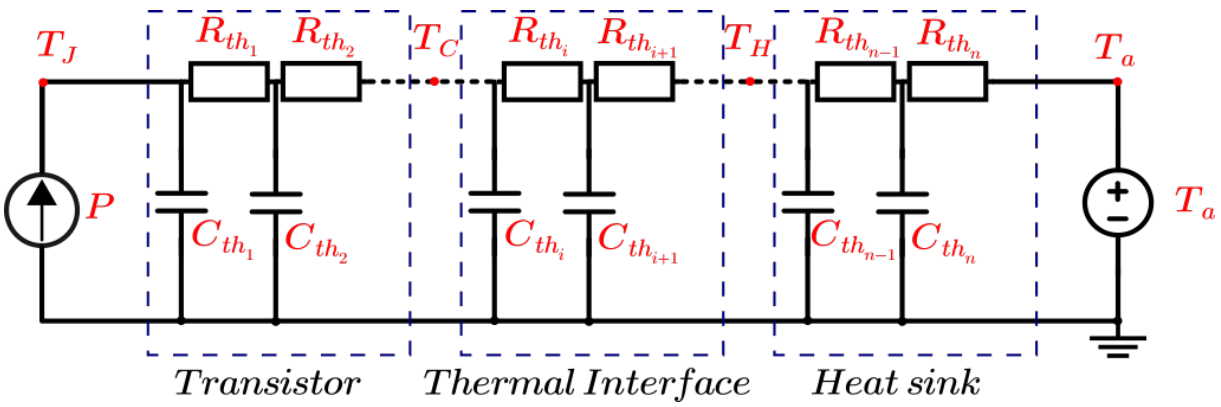


Fig. 3.4: **Cauer network equivalent circuit**

B. Foster network

A Foster network represents only a mathematical description of a given system, and should not be considered as a physical model. In fact, the heat propagation through the Foster circuit is instantaneous, as illustrated in Fig. 3.5, where the heat flow reaches the heat sink without delay, which is physically wrong. Actually, it needs some time for a given layer to warm up, before the heat flow reaches the next layer, as in the case of Cauer networks [108]. Moreover, the R_{th}-C_{th} cells do not represent real physical layers, hence the nodes between these cells do not refer to specific geometric points in the system [109].

Usually, the manufacturer's datasheets provide the R_{th}-C_{th} cells' values of a Foster network, since it is easier to fit the measured thermal impedance curve with the Foster network equivalent impedance:

$$Z_{th}(t) = \sum_{i=1}^{i=N} R_{th_i} \cdot \left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{3.7}$$

where R_{th_i} is one elementary thermal resistance of the model, τ_i is one elementary time constant ($\tau_i = R_{th_i} \cdot C_{th_i}$), while N is the number of R_{th}-C_{th} cells in the model. Similarly to the Cauer network, when the power module is used with a given heat sink the datasheet's R_{th}-C_{th} values are slightly modified. Furthermore, Foster equivalent circuit of the total system cannot be directly obtained by a simple series connection of the power module, the thermal interface and the heat sink Foster networks because of the non-physical representation of this network. Thereupon, a measurement of the total thermal impedance should be performed in order to evaluate the R_{th}-C_{th} values of the global Foster network if accurate estimations are expected. Eventually, Table 3.2 represents a comparison between Cauer and Foster networks characteristics [104].

Table 3.2: Comparison between Cauer and Foster networks characteristics [104]

Cauer Network	Foster Network
Physically consistent model	Not a physically consistent model
Inner nodes represent geometrical locations	Inner nodes have no geometrical relevance
R_{th}-C_{th} elements are not exchangeable	R_{th}-C_{th} elements are exchangeable
Networks can be separated and connected	Networks cannot be separated and connected
Analytical solution is complicated	Analytical solution is simple

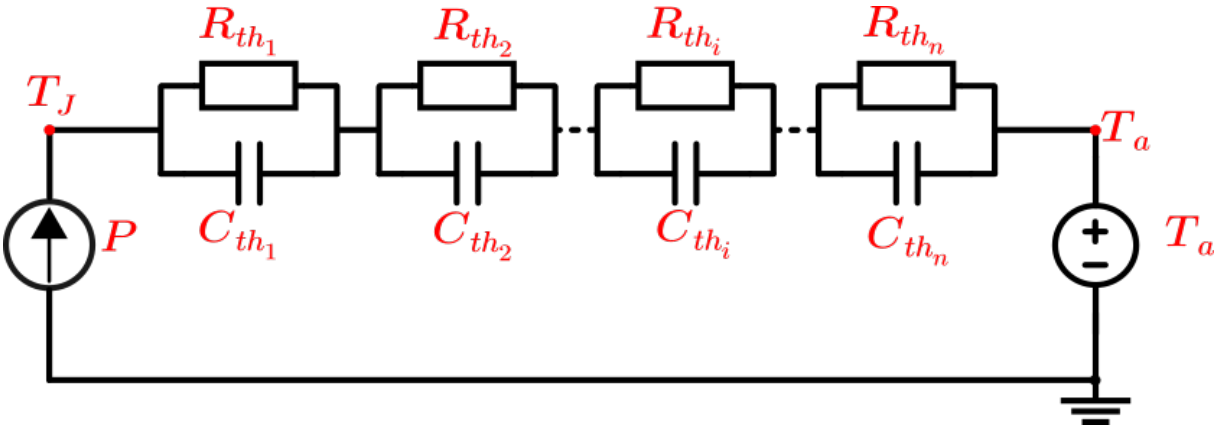


Fig. 3.5: Foster network equivalent circuit

3.2.3. Thermal coupling between several chips

When the semiconductors in a given system are turned on, the heat flowing from the junction of each one of them will raise the temperature of all the others in the system. This effect is called thermal coupling, and should be taken into account to prevent the underestimation of the semiconductors' junction temperature [106] [110] [111]. However, in the previous thermal circuits, only the self-heating effect of the semiconductor devices was taken into account. Hence, these equivalent circuits should be updated in order to consider the thermal coupling between the devices if accurate results are needed [27] [112] [113]. Accordingly, the devices' junction temperature can be estimated by solving the following equation:

$$\begin{pmatrix} T_{J_1} \\ T_{J_2} \\ . \\ . \\ T_{J_i} \\ . \\ . \\ T_{J_n} \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{21} & . & . & Z_{i1} & . & . & Z_{n1} \\ Z_{12} & Z_{22} & . & . & Z_{i2} & . & . & Z_{n2} \\ . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . \\ Z_{1i} & Z_{2i} & . & . & Z_{ii} & . & . & Z_{ni} \\ . & . & . & . & . & . & . & . \\ . & . & . & . & . & . & . & . \\ Z_{1n} & Z_{2n} & . & . & Z_{in} & . & . & Z_{nn} \end{pmatrix} \cdot \begin{pmatrix} P_1 \\ P_2 \\ . \\ . \\ P_i \\ . \\ . \\ P_n \end{pmatrix} + T_a \cdot \begin{pmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{pmatrix} \quad (3.8)$$

where T_a represents the ambient temperature, while P_i and T_{J_i} represent the power losses in device D_i and its junction temperature respectively. Z_{ij} represents the mutual thermal coupling impedance between devices D_i and D_j [111].

3.3. Junction temperature calculation methods

As mentioned in Section 3.2.2, the transient thermal impedance Z_{th} represents the step response of the system. Once Z_{th} is determined, the semiconductors' junction temperature $T_J(t)$ corresponding to a given power losses profile $P(t)$ can be calculated, when neglecting the thermal coupling between semiconductor chips. The aim of this chapter is to build a numerical thermal model with *Matlab*, having as input the power losses, already depicted in the previous chapter. In order to do so, a compact Foster model will be considered, for the case of a two-level DC/AC inverter.

As detailed in Chapter 2 (sections 2.3.1.5 and 2.3.2.5), the electro-thermal coupling of the temperature-dependent parameters are considered to accurately estimate the junction temperature. In the case of an IGBT power module, these parameters are the collector-emitter voltage V_{ce}, the diode's forward voltage V_f and the energy losses. However, in the case of a SiC MOSFET power module, these parameters are the drain-source on-state resistance $R_{DS_{on}}$, its intrinsic diode's forward voltage V_f and the switching energies. Therefore, the power losses' estimation model and the thermal model are coupled together. Thus, at each iteration of the *Matlab* model's code, the junction temperature is reinjected in the power losses' estimation model in order to update the values of the temperature-dependent parameters.

Several computation methods for estimating the junction temperature were tested and implemented in the thermal model. These methods, as well as a comparison between them in terms of performance, will be depicted in this section. Accordingly, the fastest method will be used in the final model.

3.3.1. Time-Domain Estimation

The junction temperature of a semiconductor mounted on a heat sink can be obtained in time-domain by the convolution product of $P(t)$ and $dZ_{th}(t)$ as follows [83] [107] [108]:

$$T_J(t) = \Delta T_{JA}(t) + T_a(t) = P(t) \otimes dZ_{th}(t) + T_a(t) \tag{3.9}$$

in other terms:

$$T_J(t) = \int_0^t P(\tau) \cdot dZ_{th}(t-\tau)\, d\tau + T_a(t) \tag{3.10}$$

where t represents the time and ΔT_{JA} the difference between the junction and the ambient temperatures, while dZ_{th} represents the derivative of the thermal impedance. In other words, dZ_{th} represents the impulse response of the complete system (semiconductor + thermal interface + heat sink). This equation is valid by considering that the ambient temperature's dynamics are slow compared to those of the junction temperature. Since the *Matlab* model is numerical, $t, P(t), dZ_{th}(t), T_a(t)$ and $T_J(t)$ are discrete data vectors, and thus discrete convolution has to be used. Hence Eq. 3.10 becomes:

$$T_J(m) = \sum_{n=0}^{n=m} P(n) \cdot dZ_{th}(m-n) + T_a(m) \tag{3.11}$$

In the case of a Foster network, dZ_{th} can be expressed as follows:

$$dZ_{th}(t) = \sum_{i=1}^{i=N} \frac{R_{th_i}}{\tau_i} \cdot e^{-\frac{t}{\tau_i}} \tag{3.12}$$

Unfortunately, the convolution requires a long calculation time, add to this the complexity of considering the electro-thermal coupling when using it. In fact, the electro-thermal coupling requires a reinjection of the calculated junction temperature in the power losses estimation model after each iteration, in order to update the values of the temperature-dependent parameters. Nevertheless, the convolution needs to be applied on two data vectors, hence the parameters' update cannot be achieved for every power losses sample, but every set of power losses data instead.

3.3.2. Fast Fourier Transform FFT

Beside the use of the time-domain convolution, another method was implemented in the thermal model, using Fast Fourier Transform FFT. The Fourier Transform FT converts an analog signal from its original domain (here time), to a representation in the frequency-domain. By applying the FT on a continuous time signal $s(t)$, its power spectral density $\hat{S}(f)$ can be obtained as follows [113]:

$$\hat{S}(f) = \int_{-\infty}^{+\infty} s(t) \cdot e^{-i2\pi f t} dt \tag{3.13}$$

where t represents the time and f the frequency.

The Discrete Fourier Transform DFT is the equivalent of the FT, used when dealing with digital (discrete) signals. It can be obtained for a discrete signal of length N, as follows:

$$\hat{S}(k) = \sum_{n=0}^{n=N-1} s(n) \cdot e^{-i2\pi k\frac{n}{N}} \qquad \text{for } 0 \leq k < N \tag{3.14}$$

Conversely, the Inverse Discrete Fourier Transform IDFT can be obtained as follows:

$$s(n) = \frac{1}{N} \sum_{k=0}^{k=N-1} \hat{S}(k) \cdot e^{i2\pi n\frac{k}{N}} \tag{3.15}$$

Since the Fourier transform is linear, by applying the DFT on Eq. 3.9, the power spectral density of $T_J(t)$ can be expressed as follows:

$$\widehat{T_J}(k) = \widehat{\Delta T_{JA}}(k) + \widehat{T_a}(k) = F(P(t) \otimes dZ_{th}(t)) + \widehat{T_a}(k) \tag{3.16}$$

Eventually, given that the Fourier transform translates between convolution and multiplication of functions (convolution theorem), Eq. 3.16 can be expressed as follows:

$$\widehat{T_J}(k) = \hat{P}\,(k) \cdot \widehat{dZ_{th}}(k) + \widehat{T_a}(k) \tag{3.17}$$

Once $\widehat{T_J}(k)$ is determined, $T_J(n)$ can be calculated by applying the IDFT.

In order to accelerate the calculus time, fast algorithms are usually used to reduce the complexity of the DFT, known as Fast Fourier Transform FFT. By far, the most commonly used FFT is the Radix-2 Cooley–Tukey algorithm [114]. This algorithm requires that time-domain data has a power-of-two number of samples, therefore zero-padding is applied to the data, by adding zeros to their end. Now given a time-domain vector of N samples, the application of the traditional DFT represented in Eq. 3.16 requires $O(N^2)$ operations (additions and multiplications), while the FFT requires only $O(N \log_2 N)$ operations [115]. Eventually, the junction temperature vector can be calculated as follows:

$$T_J(n) = IFFT\left(FFT\big(P(n)\big) \cdot FFT\big(dZ_{th}(n)\big)\right) + T_a(n) \tag{3.18}$$

where IFFT is the Inverse Fast Fourier Transform.

Although being faster than the time-domain convolution, the FFT cannot reduce alone the complication of the electro-thermal coupling implementation. Therefore, the Overlap-Add method will be applied together with the FFT, which will also lead to accelerate the FFT's calculation time.

3.3.3. FFT with Overlap-Add method

Generally, the Overlap-Add method is used to break long signals into smaller segments for easier processing with the FFT. Let's consider a time-domain vector of N samples, the FFT applied alone requires $O(N \log_2 N)$ operations. Now using the overlap-add

method to break the original vector into n segments each of $\frac{N}{n}$ samples, the number of required operations becomes $O\left(n * \frac{N}{n} \log_2 \frac{N}{n}\right) = O\left(N \log_2 \frac{N}{n}\right)$. That means less in theoretically $O\left(\frac{\log_2 N}{\log_2 \frac{N}{n}}\right)$ operations than the FFT used alone.

The Overlap-Add method was applied in the thermal model, in order to break down the power losses mission profile into smaller segments. Hence, it was easier to consider the electro-thermal coupling by updating the temperature-dependent parameters, before the application of the FFT on the next segments.

Now let's consider a discrete-time power losses mission profile P(n) of length L_P, and a discrete-time impulse response $dZ_{th}(n)$ of length M. The linear convolution of the two time-vectors produces a discrete-time convolved result of length $L_P + M - 1$. Moreover, since the convolution is linear, hence:

$$(P_1(n) + P_2(n)) \otimes dZ_{th}(n) = P_1(n) \otimes dZ_{th}(n) + P_2(n) \otimes dZ_{th}(n) \qquad (3.19)$$

The application of the Overlap-Add algorithm in the thermal model is illustrated in Fig. 3.6 and can be exhibited as follows [116]:

1. Break the mission profile $P(n)$ into B non-overlapping blocks $P_i(n)$ of a given length L.
2. Zero pad $dZ_{th}(n)$ to be of length $N = L + M - 1$.
3. Apply FFT on $dZ_{th}(n)$ to obtain $\widehat{dZ_{th}}(k), k = 0, 1, \ldots, N - 1$.
4. For each block i:
   - 4.1 Zero pad $P_i(n)$ to be of length $N = L + M - 1$.
   - 4.2 Apply FFT on $P_i(n)$ to obtain $\hat{P}_i(k)$, $k = 0, 1, \ldots, N - 1$.
   - 4.3 Calculate: $\hat{T}_{J_i}(k) = \hat{P}_i(k) \cdot \widehat{dZ_{th}}(k)$, $k = 0, 1, \ldots, N - 1$.
   - 4.4 Apply IFFT on $\hat{T}_{J_i}(k)$ to obtain $T_{J_i}(n)$, $n = 0, 1, \ldots, N - 1$.
5. Consider the electro-thermal coupling and update the values of $P_{i+1}(n)$, by reinjecting $T_{J_i}(n)$ in the power losses estimation model.
6. Form $T_J(n)$ by overlapping the last $M - 1$ samples of $T_{J_i}(n)$ with the first $M - 1$ samples of $T_{J_{i+1}}(n)$, and adding the result.

Accordingly, the Overlap-Add method allows updating the temperature-dependent parameters every L samples, therefore the lower the L is, the higher the precision of the calculus is. However, by excessively decreasing L, the execution time of the thermal model becomes longer, due to a higher number of loops iterations. Eventually, in order to accelerate the calculus time and take the electro-thermal coupling into account at each iteration (equivalent to $L = 1$), another method will be tested and demonstrated in the following section.

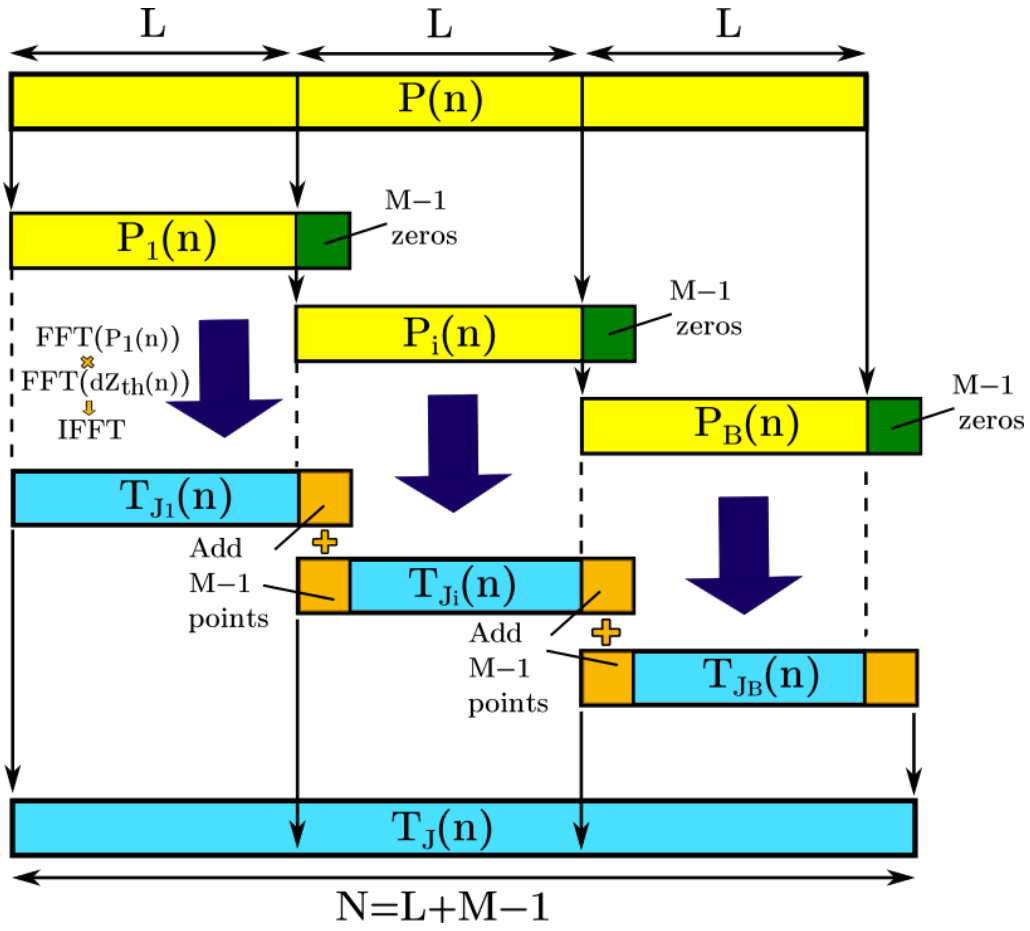


Fig. 3.6: Concept of the Overlap-Add method [116]

3.3.4. Breaking down the mission profile into single pulses

This method depicted in [38] and [104] consists of considering the power losses mission profile as a sequence of rectangle single pulses. It considers the analytical solution of the Foster network's thermal impedance represented in Eq. 3.7. Thus the solution for $\Delta T(t)$ represented in Eq. 3.11 can be analytically obtained as follows:

$$\Delta T(t) = \int_0^t P(x) \cdot \frac{d}{dx}\left[\sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t-x}{\tau_i}}\right)\right] dx \tag{3.20}$$

Let's consider a power losses square pulse $P(t)$, having an amplitude of P_0 between time 0 and time t_1, as represented in Fig. 3.7. Assuming a fixed reference temperature, $\Delta T(t)$ becomes:

$$\Delta T(t) = \begin{cases} P_0 \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t}{\tau_i}}\right) & for\ 0 \le t < t_1 \\ P_0 \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t}{\tau_i}}\right) - P_0 \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t-t_1}{\tau_i}}\right) & for\ t \ge t_1 \end{cases} \tag{3.21}$$

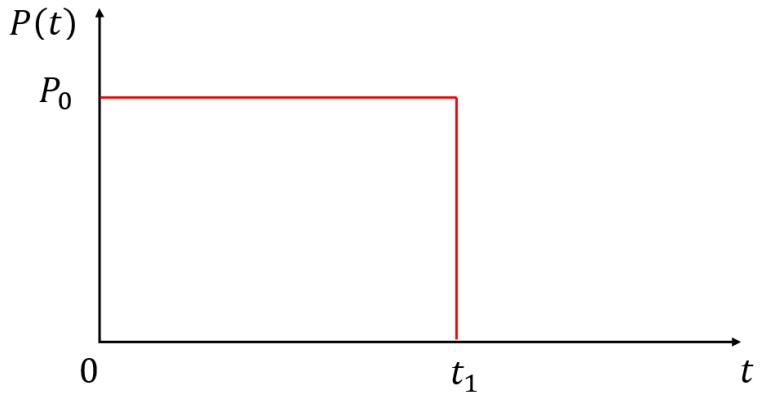


Fig. 3.7: A single power pulse

Similarly to the case of a single pulse, and considering the power losses' mission profile represented in Fig. 3.8, the temperature variation at time t_1 can be obtained as follows [104]:

$$\Delta T(t_1) = P_1 \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t_1}{\tau_i}}\right) \tag{3.22}$$

whereas the variation at time t_2:

$$\Delta T(t_2) = P_1 \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t_2}{\tau_i}}\right) + (P_2 - P_1) \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{(t_2 - t_1)}{\tau_i}}\right) \tag{3.23}$$

and at time t_3:

$$\Delta T(t_3) = P_1 \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t_3}{\tau_i}}\right) + (P_2 - P_1) \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{(t_3 - t_1)}{\tau_i}}\right) + (P_3 - P_2) \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{(t_3 - t_2)}{\tau_i}}\right) \tag{3.24}$$

Eventually, the general form of the junction temperature variation at a given time t_N, can be expressed as follows:

$$\Delta T(t_N) = \sum_{k=1}^{k=N} (P_k - P_{k-1}) \sum_{i=1}^{i=n} R_{th_i}\left(1 - e^{-\frac{t_N - t_{k-1}}{\tau_i}}\right) \tag{3.25}$$

The colors highlighting these formulas refer to the colored blocks and temperature variations illustrated in Fig. 3.8.

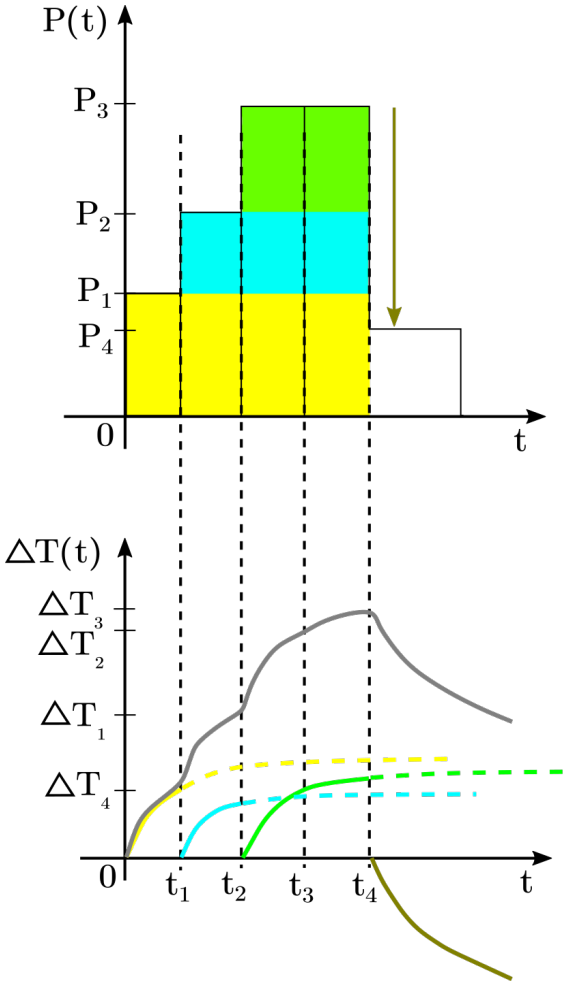


Fig. 3.8: Power losses' mission profile with the corresponding temperature variations [104]

This method was implemented in the *Matlab* thermal model, enabling the discretization of any power losses mission profile, hence avoiding the application of time-domain convolution, and thus, enormously reducing the calculus time. However, the estimation of $\Delta T(t_N)$ at a given moment t_N, requires as represented in Eq. 3.25, to sum N times the expression $(P_k - P_{k-1}) \sum_{i=1}^{i=n} R_{th_i} \left(1 - e^{-\frac{t_N - t_{k-1}}{\tau_i}}\right)$, which represents a considerable disadvantage with long mission profiles.

3.3.5. Analytical solution

For long power losses mission profiles and complicated systems with multiple power modules, where the thermal coupling effect between the modules is considered, the method detailed in Section 3.3.4 is not enough to accelerate sufficiently the calculus time. Hence, this section presents a mathematical solution of Eq. 3.25, where the calculus of $\Delta T(t_N)$ depends only on $P(t_N)$ and $\Delta T(t_{N-1})$. Accordingly and by developing Eq. 3.25, $\Delta T(t_N)$ the temperature variation at time t_N can be expressed as follows [117]:

$$\Delta T(t_N) = \sum_{i=1}^{i=n} \left(\left(\Delta T(t_{N-1}) - R_{th_i} \cdot P(t_N) \right) \cdot e^{-\frac{\Delta t}{\tau_i}} + R_{th_i} \cdot P(t_N) \right) \tag{3.26}$$

where Δt represents the time step between two consecutive samples. Given that the mission profile is sampled at the fundamental frequency f_{out} rate, hence Δt equals T_{out}.

3.3.6. Comparison between the methods

As mentioned in the introduction section, the thermal model will be used to estimate the semiconductors' junction temperature T_J over several years. Thus, it should be fast enough to process mission profiles with more than 800 million samples each. Therefore, all the methods represented above were implemented and tested with *Matlab* in order to select the fastest one.

First, the results obtained with all methods were compared with each other to verify whether identical results would be obtained. Accordingly, Fig. 3.10 represents the different methods' outputs corresponding to the current and ambient temperature mission profiles represented in Fig. 3.9. It can be seen that all the methods (M_1 to M_6) have provided exactly the same results, which validates the different algorithms.

Eventually, Table 3.3 represents a comparison of the different methods' execution time needed to process a current mission profile of 750 $k$samples, corresponding to a duration of approximately 2 hours (50 sample/s rate). The methods are applied in the case of a two-level single-phase inverter with 4 IGBTs and 4 diodes. As it will be presented at a later stage, the thermal coupling between devices is taken into account which results in obtaining 64 thermal impedances, each one being composed by a Foster network. Since it is independent from the thermal model, the execution time of the power losses model is included in the total execution time, exhibited in Table 3.3.

It can be clearly noticed that the analytical method of Section 3.3.5 represents by far the best performance. It should be noted that the longer the mission profile is, and the more complex the system is, the wider the gap will be between the methods performances. In consequence, the last method was chosen to estimate the junction temperatures in IGBT and SiC MOSFET inverters.

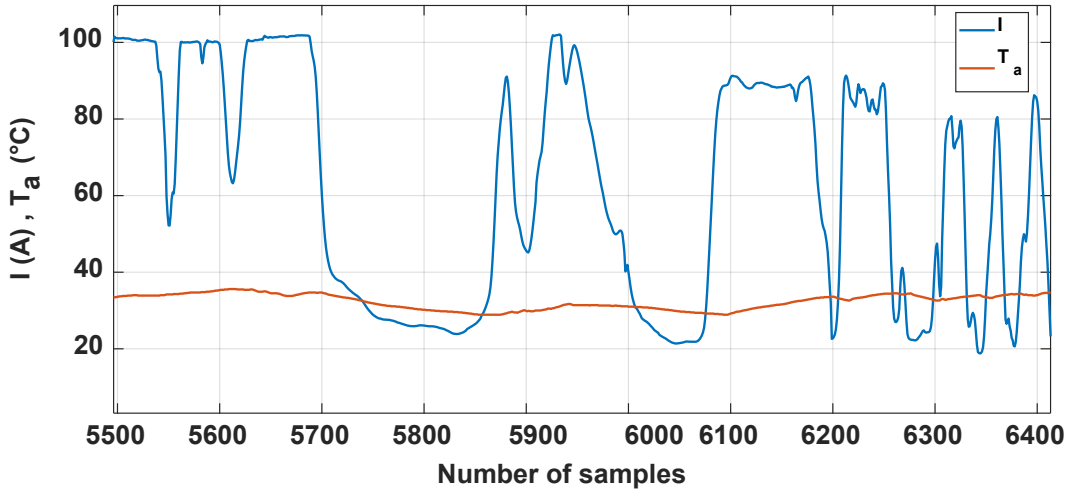


Fig. 3.9: Current and ambient temperature mission profiles, used to compare the different methods performance

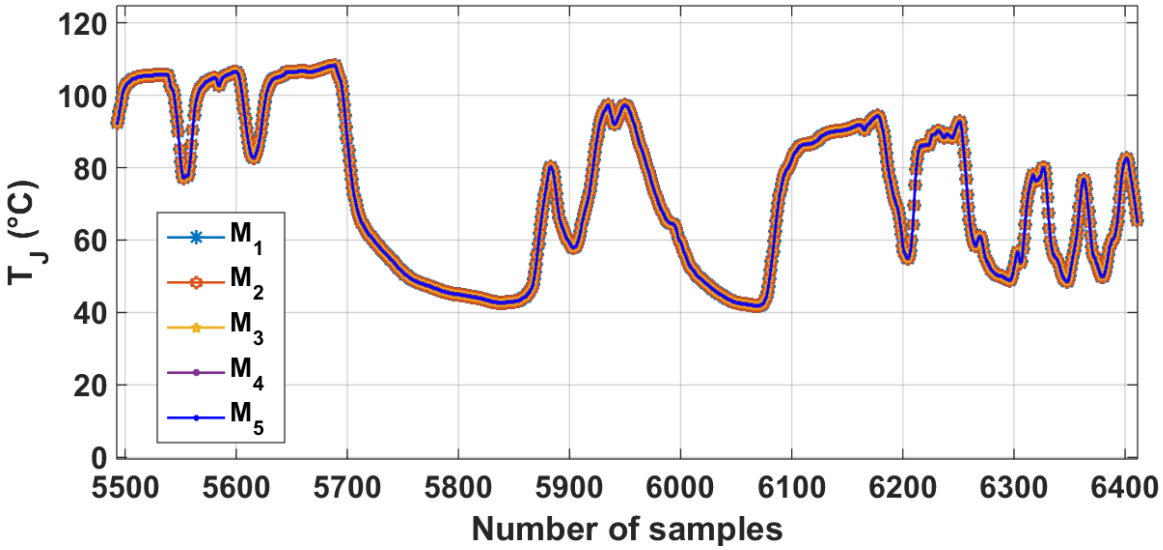


Fig. 3.10: Estimated junction temperature, corresponding to the current's profile of Fig. 3.9

Table 3.3: Comparison of the different methods' execution time

Method	Execution Time
Time-Domain Estimation	$+\infty$ (machine blocked)
Fast Fourier Transform FFT	$\cong 1\ h$
FFT with Overlap-Add method	$\cong 10\ min$
Breaking down mission profile into single pulses	$\cong 5\ min$
Analytical solution	$\cong 1\ s$

3.4. Models validation

This section is dedicated to validate the thermal model and is based on the examples and simulators detailed in Chapter 2 Section 2.5. Thus, the whole *Matlab* model (thermal model + power losses estimation model) will be validated. However, in these examples the parameters are extracted from the manufacturer' datasheets, thus the thermal coupling between devices is not taken into account. Moreover, the use of Foster models is only possible if the temperature of the case (base plate) T_C remains constant. Hence, if it varies slowly comparatively to the power module's time constant (about 1 s), the use of this type of model gives good results. This is usually the case of air coolers considered in the following examples. It is worth mentioning that the thermal impedances used in the following figures of this chapter are equivalent to Foster network's *R*-*C* cells.

3.4.1. Case of IGBT power modules

In the case of IGBT power modules, the thermal model is compared with several simulators such as *PSIM*, *IPOSIM* and *SemiSel*. First, Fig. 3.11 depicts the simulation of the DC/AC inverter with *PSIM* (refer to Fig. 2.36). This model uses the Foster network to simulate the thermal behavior of the system and can estimate the junction temperature of the semiconductors simply with voltmeters. The output is illustrated in Fig. 3.12 (refer to Fig. 2.37), where the current and the junction temperatures are represented on several fundamental

periods T_{out}. Eventually, the average values of the junction temperatures on T_{out} were calculated in order to compare them with the *Matlab* model's results.

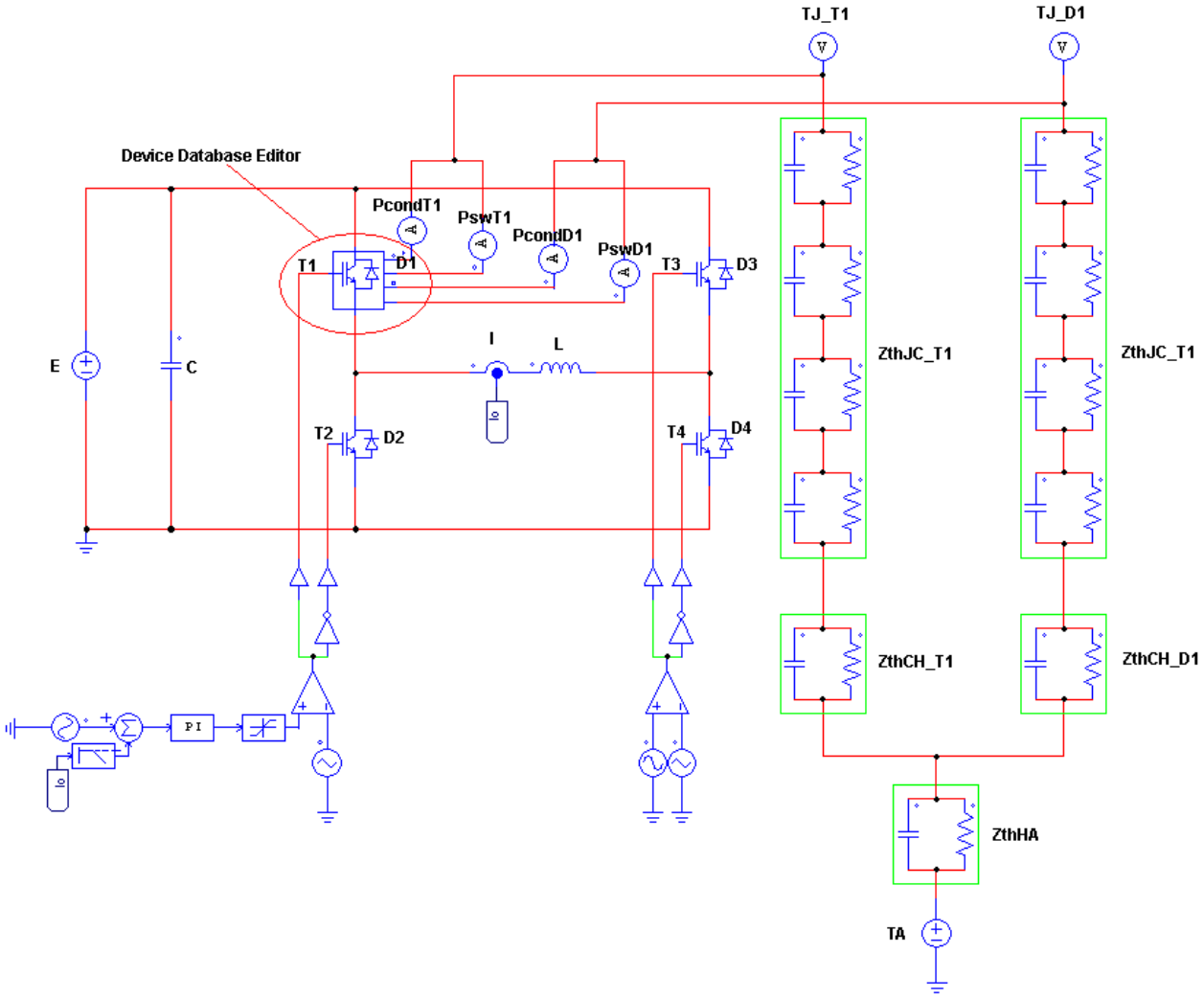


Fig. 3.11: **Estimating the semiconductors' junction temperature with *PSIM***

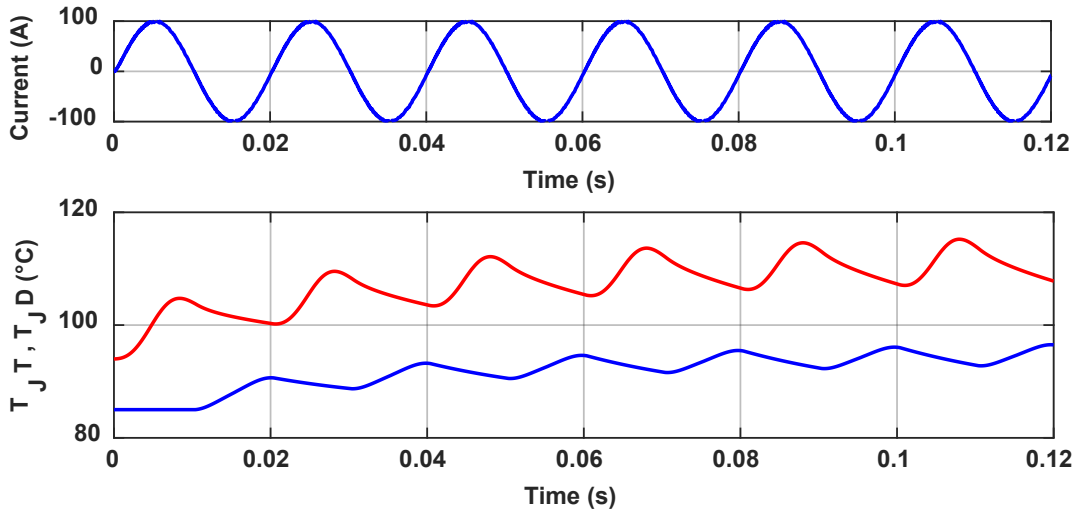


Fig. 3.12: **Example of the junction temperature estimation with *PSIM***

Similarly, *IPOSIM* is the other simulator used to validate the *Matlab* model. This online simulator developed by *Infineon* allows estimating the junction temperature of a given power module in steady state, as represented in Fig. 3.13 (refer to Chapter 2 Fig. 2.38).

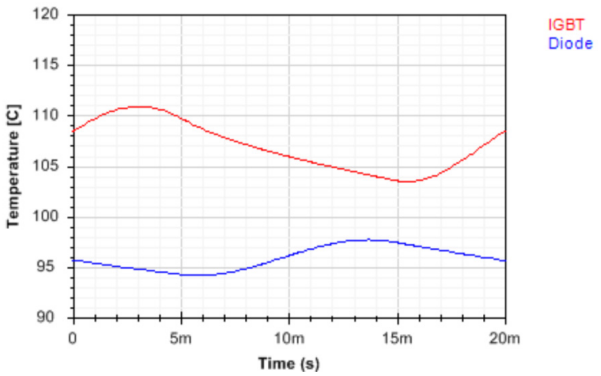


Fig. 3.13: Example of the junction temperature estimation on T_{out} with *IPOSIM*

In order to compare the three simulators, a simulation was applied on five IGBT power modules. Table 3.4 displays the estimated junction temperatures in steady state, corresponding to a current step of 70 $A\ rms$, for one of the five IGBT modules since the other IGBTs represent similar results. This table compares the minimum and maximum values of the junction temperatures, as well as its variation over a fundamental period T_{out}. It's remarkable in Table 3.4 that the obtained values of the mean junction temperature over T_{out} are very close to each other. The slight differences are due partially to the differences in the estimated power losses (refer to Chapter 2 Table 2.3). $T_{J_T}min$ and $T_{J_T}max$ are the local minimum and maximum values respectively of the transistor's T_{J_T} on T_{out}, while ΔT_{J_T} represents the difference between these values. $T_{J_D}min$, $T_{J_D}max$ and ΔT_{J_D} represent the same for the diode.

The same approach was applied on another IGBT power module *SKM200GB12E4* with *SemiSel*, a *Semikron*'s online design simulator, and proximate results were also obtained. Actually, for the same example considered in Chapter 2 Table 2.4, the IGBT's junction temperature estimated with *SemiSel* is equal to 123.5°C, whereas it equals 125 °C with *Matlab*. Similarly, the diode's junction temperature estimated with *SemiSel* is equal to 117.5°C, while it equals 115 °C estimated with *Matlab*. It should be noted, that this IGBT power module will be used at a later stage in this study, during the accelerated ageing tests (Chapter 6).

Table 3.4: Comparison of the junction temperature obtained by the different simulators

Simulator \ Power Losses	$T_{J_T}max$ (°C)	$T_{J_T}min$(°C)	ΔT_{J_T}(K)	$T_{J_D}max$ (°C)	$T_{J_D}min$ (°C)	ΔT_{J_D}(K)
IPOSIM	125.23	117.68	7.55	112.46	108.68	3.77999
PSIM	126.03	117.946	8.084	112.579	109.02	3.559
Matlab	125.0495	117.4	7.64949	112.2235	108.6	3.6235
$\Delta(IPOSIM, PSIM)\%$	2.56%	1.12%	7.07%	0.64%	2.32%	5.85%
$\Delta(IPOSIM, Matlab)\%$	0.58%	1.18%	1.31%	1.28%	0.54%	4.31%
$\Delta(Matlab, PSIM)\%$	3.14%	2.33%	5.68%	1.95%	2.88%	1.78%

3.4.2. Case of MOSFET power modules

In the case of SiC MOSFET power modules, the thermal model is compared with the *WolfSpeed*'s online simulator *SpeedFit*. In this section, the example illustrated in Chapter 2 Section 2.5.2 is considered. The equivalent Foster circuit of the full system is represented in Fig. 3.14. Chapter 2 Fig. 2.39 represents a screenshot on the results of the *SpeedFit* simulator, while Table 3.5 represents a comparison between the resulted MOSFET's mean junction temperature on T_{out}, estimated with the *Matlab* model and the *SpeedFit* simulator (Chapter 2 Table 2.6). It can be noticed from Table 3.5 that the results are very close, with a maximum junction temperature's difference of 2.11%, which validates the *Matlab* model ($T_a = 40\ °C$).

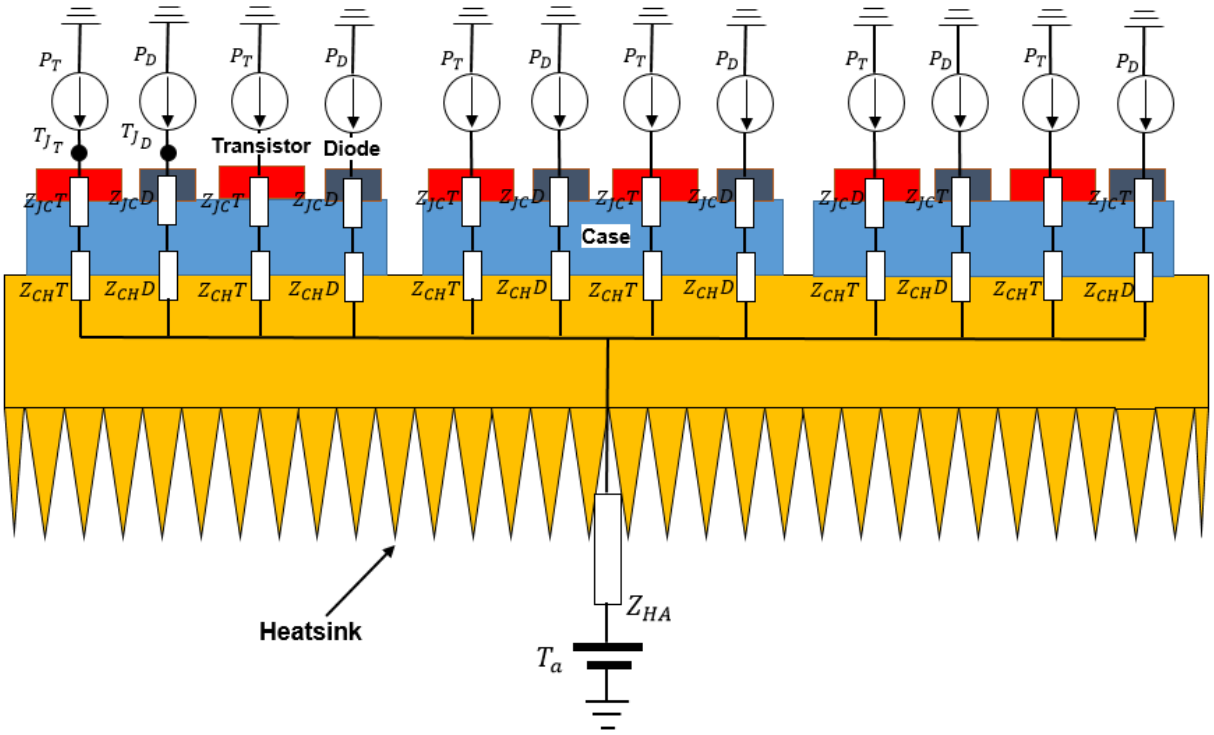


Fig. 3.14: Equivalent Foster circuit of the full system

Table 3.5: Comparison between the simulators results

	Matlab Model	***SpeedFit Simulator***	$\%\Delta T_{J_T}$
T_{J_T} (°C)	127.7	125	2.11%

3.5. Self-heating and mutual thermal coupling impedances measurements

3.5.1. Justification for measurement tests

Although the previous thermal models for IGBT and SiC MOSFET power modules were validated with several simulators, these models and simulators use the values of the R_{th}-C_{th} cells provided by the manufacturer's datasheets. However, during the accelerated ageing tests depicted in Chapters 5 and 6, liquid-cooled heat sinks are deployed. Thus, in order to accurately estimate the junction temperature of the semiconductor devices used in the test benches, it is crucial to directly measure the mutual thermal coupling and self-heating impedances for the following reasons:

- The values of R_{th}-C_{th} cells depend on the used heat sink.
- The values of R_{th} and C_{th} of the thermal interface and the heat sink are not available.
- The manufacturer's datasheets cannot be used for considering the thermal coupling between devices

Consequently, the thermal model of the inverter is built by filling the matrix form represented in Eq. 3.8 with the measured mutual thermal coupling impedances, as well as with self-heating impedances between the devices' chips and the ambient (the cooling fluid). Accordingly, the Z_{th} measurement tests for the cases of IGBT and SiC MOSFET power modules will be depicted in the following sections.

3.5.2. Choice of the measurement method

In order to identify the thermal impedance matrix of the system, the semiconductors' junction temperature should be estimated (accordingly to Eq. 3.7) when applying power dissipation to the semiconductor devices. Nowadays, three main methods are being used to evaluate the junction temperature of the semiconductor devices: optical methods, physical contact methods and electrical methods [64] [65] [104].

Several optical methods, such as infrared (IR) thermography or thermo-reflectance techniques allow for direct mapping of the temperature in the power module. Moreover, the laser deflection technique measures the temperature gradients directly inside the chip. However, in order to use these methods the chip has to be uncovered, thus the polymer package and the dielectric gel have to be removed. However, the measurement with optical fibers can be fulfilled without removing the dielectric gel, but this technique only allows for an evaluation of the local temperature [64].

Physical contact methods consist of measuring the chip temperature by direct contact with a thermo-sensitive material like crystals, thermographic phosphors, thermistors or thermocouples. However, the dynamic response is relatively low, and the junction temperature evaluation is local.

Eventually, electrical methods necessitate using Thermo-Sensitive Electrical Parameters (TSEPs) to evaluate the junction temperature using current and voltage probes, with response times typically shorter than $100\mu s$ [64]. Accordingly, in our study, the measurement of the thermal impedances of the systems will be done using TSEPs.

3.5.3. Choice of the TSEP

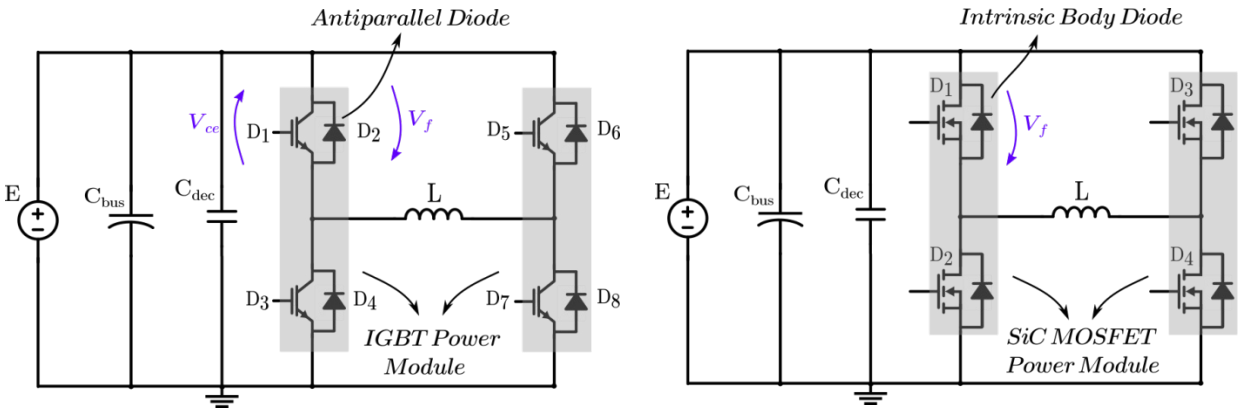
[64] presents a review of the main TSEPs like voltage under a low current, threshold voltage, voltage under a high current, gate-emitter voltage, saturation current and switching times. In this paper, the different TSEPs are compared in terms of sensitivity, linearity, accuracy, genericity, calibration needs, and possibility of characterizing the thermal impedance or the temperature during the operation of the converter. According to this study, the voltage under a low current TSEP represents the best compromise between all these characteristics, and it is adapted for thermal impedance measurements. Hence, the TSEPs that will be used in this study will be the collector-emitter voltage V_{ce} for IGBTs, V_f for the antiparallel diodes and the MOSFET's intrinsic body diodes.

3.5.4. Z_{th} measurement with TSEPs: methodology and tests

Three steps are necessary for determining the thermal impedances of semiconductor power devices using the voltage under low current as TSEP:

1. Calibration of the TSEP as a function of the temperature
2. High current injection and temperature measurement
3. Temperature estimation during cooling

This section introduces the methodology and the test benches used to measure all the thermal impedances (self-heating and thermal coupling impedances) using IGBT and SiC MOSFET power modules. Fig. 3.15 represents the two-level single-phase DC/AC inverters where Fig. 3.15.a shows the case of the two phase-leg IGBT power modules with antiparallel diodes. Similarly, Fig. 3.15.b shows the case of the two phase-leg SiC MOSFET power modules. Here, the represented diodes are the MOSFETs' intrinsic body diodes.



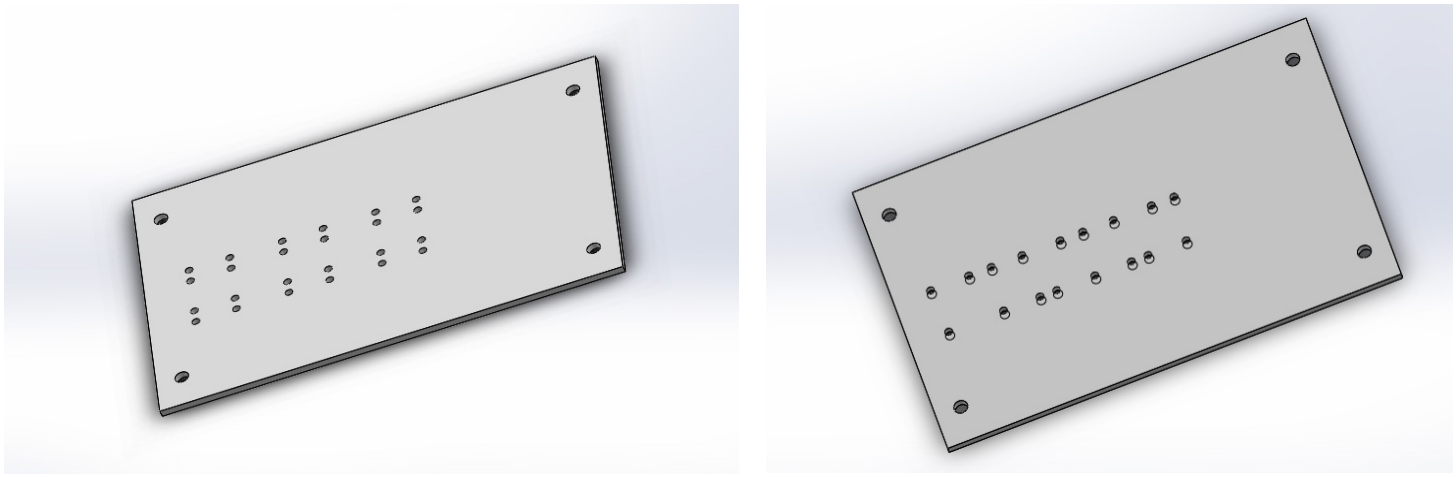
a) IGBT power modules **b) SiC MOSFET power modules**

Fig. 3.15: Two-level single-phase DC/AC inverters

3.5.4.1. Calibration of the TSEP as a function of the temperature

The calibration is used to determine the relationship between the TSEP and the semiconductor's junction temperature. During the calibration phase, the system's temperature is fixed with a liquid-cooled heat sink. At thermal equilibrium, it is assumed that the

semiconductors' junction temperatures are equal to the heat sink's temperatures ($T_J = T_H$) measured with T-type thermocouples. To do so, the cold plates are drilled under the center of each semiconductor's chip, and the thermocouples are inserted in the drilled holes. Eventually, after the insertion of the thermocouples the holes are sealed with an Al-filled glue [37]. Fig. 3.16.a illustrates the 3D geometry of the cold plate used for the IGBT test, while Fig. 3.16.b demonstrates the one used for the SiC MOSFETs. Moreover, Fig. 3.17 represents the drilled cold plate for IGBT power module cooling with 16 thermocouples inserted directly under the center of the chips.



a) Case of IGBT **b) Case of SiC MOSFET**

Fig. 3.16: 3D geometry of the cold plates with the drilled holes for inserting the thermocouples

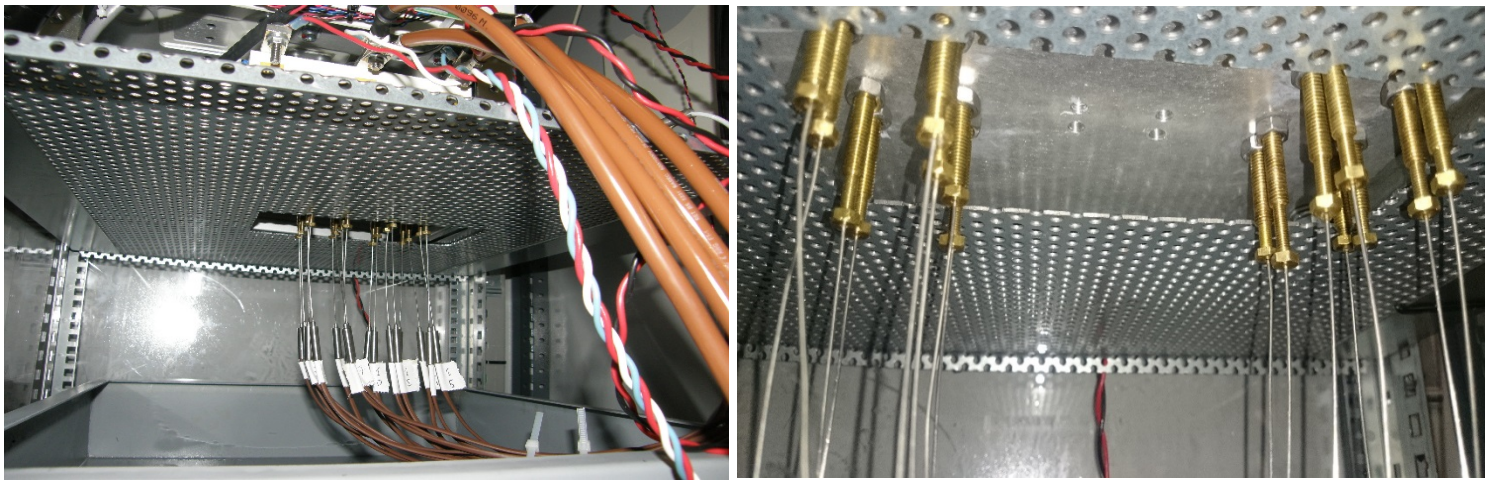


Fig. 3.17: Insertion of the thermocouples under the center of the chips

In order to obtain the relationship between the junction temperature and the TSEP, the cooling fluid's temperature is fixed at different levels. Once the thermal equilibrium is attained (in approximately 30 mins), the TSEP is measured. It should be noted that, in the case of SiC MOSFET power modules, the gate-source voltage V_{GS} was stabilized using capacitors.

Fig. 3.18 represents the IGBT's collector-emitter voltage V_{ce} and the antiparallel diode's forward voltage V_f as a function of the junction temperature, estimated using a low current of 100 mA. Actually the resulting power losses during the measurement P_m should be negligible

to prevent the self-heating of the DUT. Similarly, Fig. 3.19 represents the body diode's forward voltage V_f as a function of the junction temperature in the case of the SiC MOSFET power module. The fitted equation forms of $V_{ce} = f(T_J)$ and $V_f = f(T_J)$ of the different semiconductors are also illustrated in these figures.

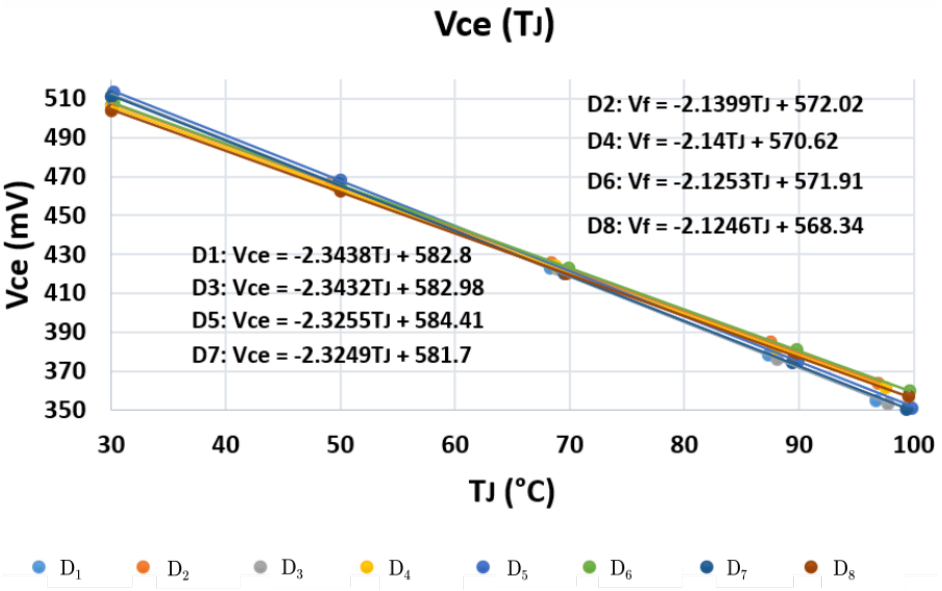


Fig. 3.18: IGBT's collector-emitter voltage V_{ce} and diode's forward voltage V_f as a function of the junction temperature, in the case of the IGBT power modules

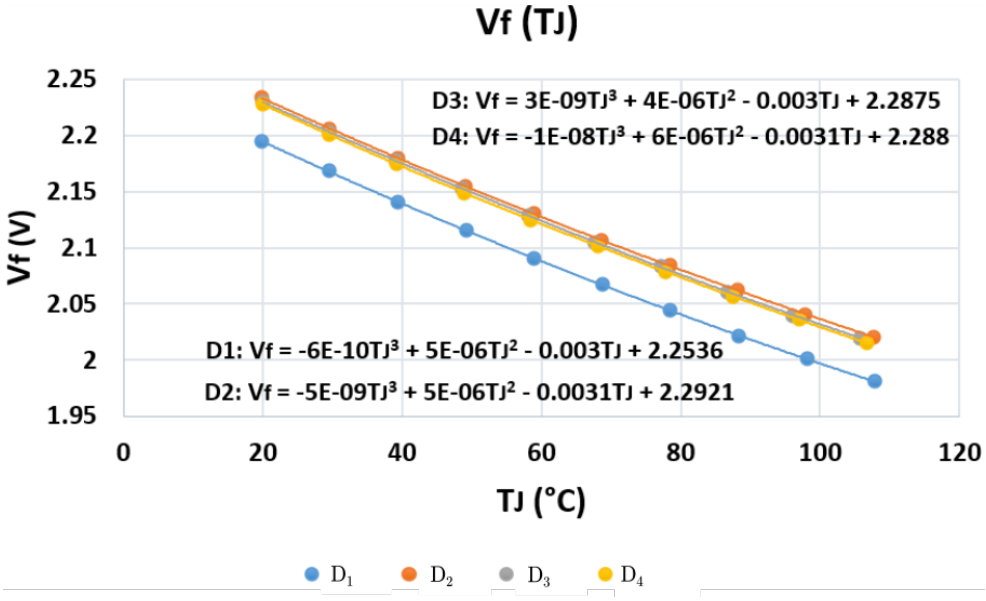


Fig. 3.19: MOSFET body diode's forward voltage V_f as a function of the junction temperature in the case of SiC MOSFET power modules

3.5.4.2. High current injection and temperature measurement

The second step consists of injecting a high current in the DUT which creates high heat losses, and thus elevates the DUT's junction temperature. Actually, in order to easily calculate the thermal impedance, the transfer function requires an ideal power losses' step

function. However, since the forward voltage drop of almost all the semiconductors is temperature-dependent, the power losses' step function cannot be ideal during the heating phase. Thus, the best solution in the case of the selected TSEP is to choose the cooling curve to measure the thermal impedance, after the achievement of the thermal equilibrium [37].

During the cooling phase, a low current is injected in the DUT in order to measure the TSEP. Thus, the measurement of the TSEP is done under the same low current of $I_m = 100\ mA$, used during the calibration. This method is illustrated in Fig. 3.20, where P_h and T_{J_h} represent the power losses and the junction temperature at thermal equilibrium respectively. T_{J_h} can be estimated by extrapolation as it will be represented in details in the next section. Accordingly, the thermal impedance can be calculated as follows:

$$Z_{th}(t) = \frac{T_{J_h} - T_{J_m}(t)}{P_h} \tag{3.27}$$

where $T_{J_m}(t)$ is the instantaneous junction temperature estimated by measuring the TSEP during the cooling phase and using the calibration curves [64].

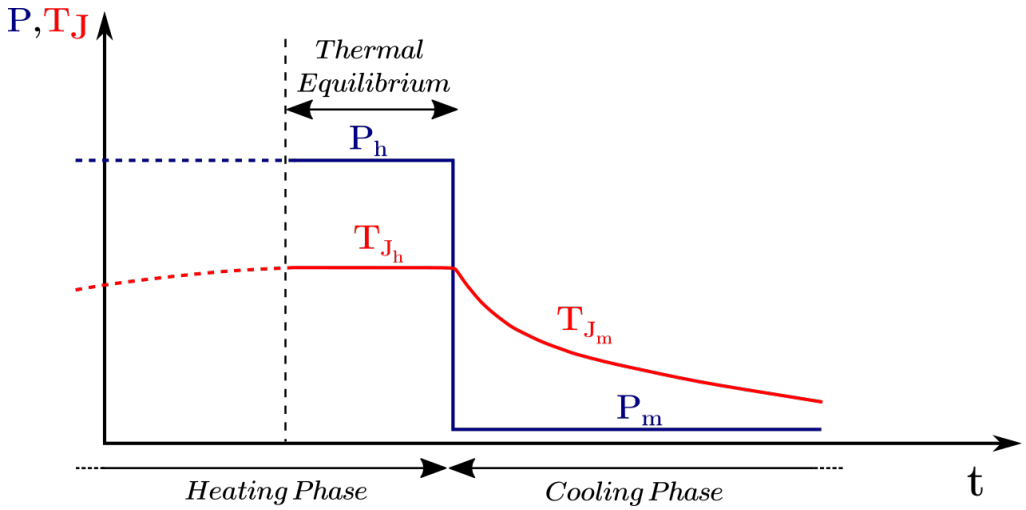


Fig. 3.20: Power losses and junction temperature represented as a function of time during heating and cooling phases

In order to apply this method, the gate drivers, the DC-link capacitors and the DC-link busbars are disconnected from the power modules. Fig. 3.21 demonstrates the electrical circuit used for the implementation of this method, where I_h is a high current source and I_{m_1} to I_{m_4} are four low current sources. D_1 to D_8 represent the semiconductor devices, while K_1 and K_2 are circuit breakers (power transistors) used to control the high current injection as illustrated in Fig. 3.22. The high current source and the low current sensing sources are connected to the DUT to measure its self-heating thermal impedance. Similarly, the other low current sensing sources are connected to the other power devices to allow measuring the mutual thermal coupling impedances.

Fig. 3.23 represents the full measurement test bench, where the data are recorded using a data logger. Usually, the junction temperature decreases sharply after the high current turning-off, hence, a high sampling rate acquisition is required (here 1MS/s). However, a measurement of the total impedance during 30 $mins$ is required, which is unattainable to do

with a high rate data acquisition. Thus, multiple measurements with different durations and acquisition rates were performed, and eventually, all the measurement data were recombined to reconstruct the final curves.

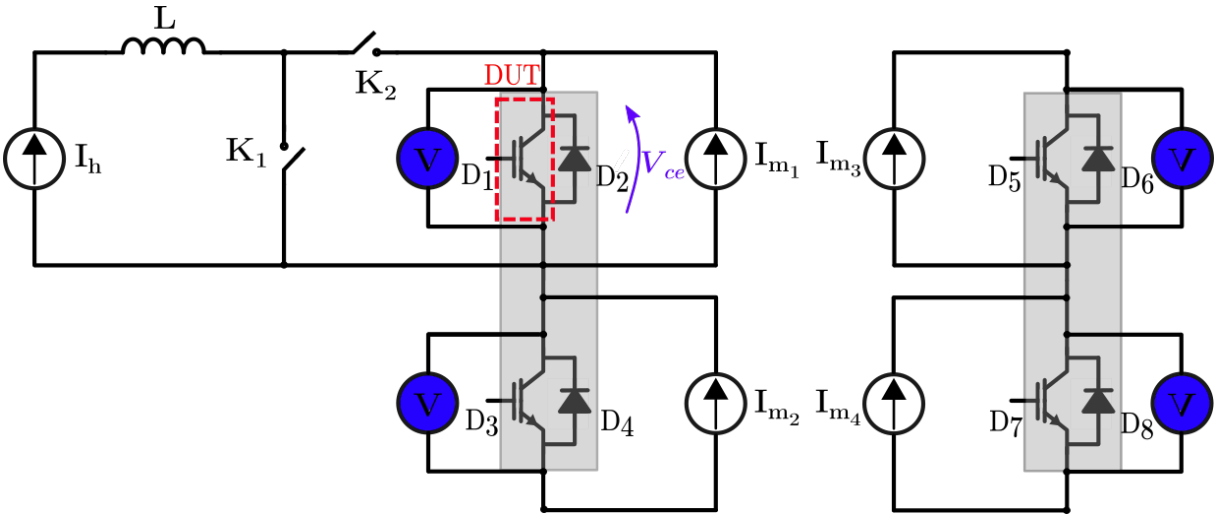


Fig. 3.21: Simplified electrical circuit used for the thermal impedances measurement

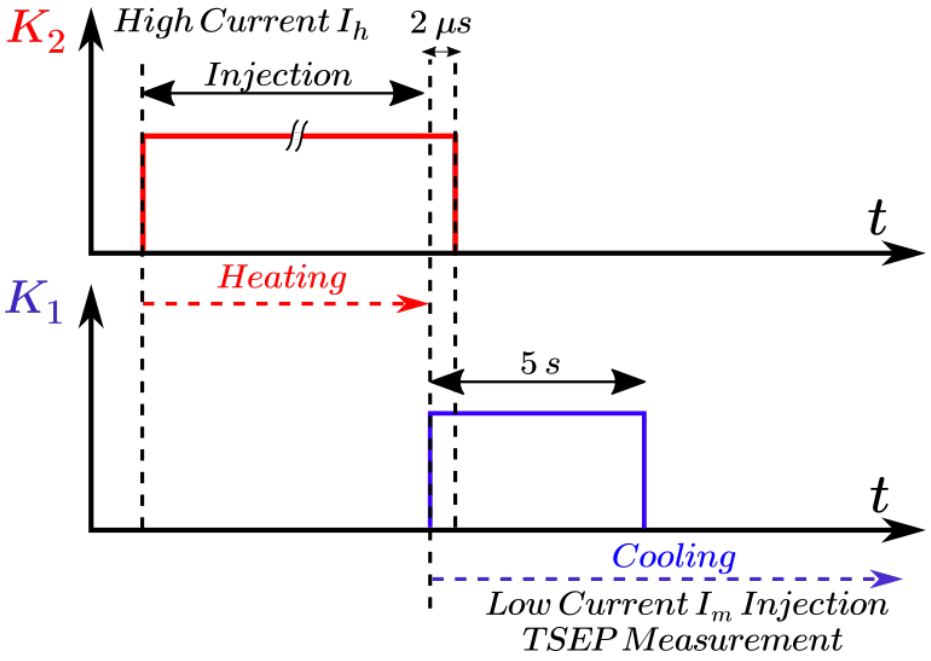


Fig. 3.22: Chronograms of the circuit breakers' control

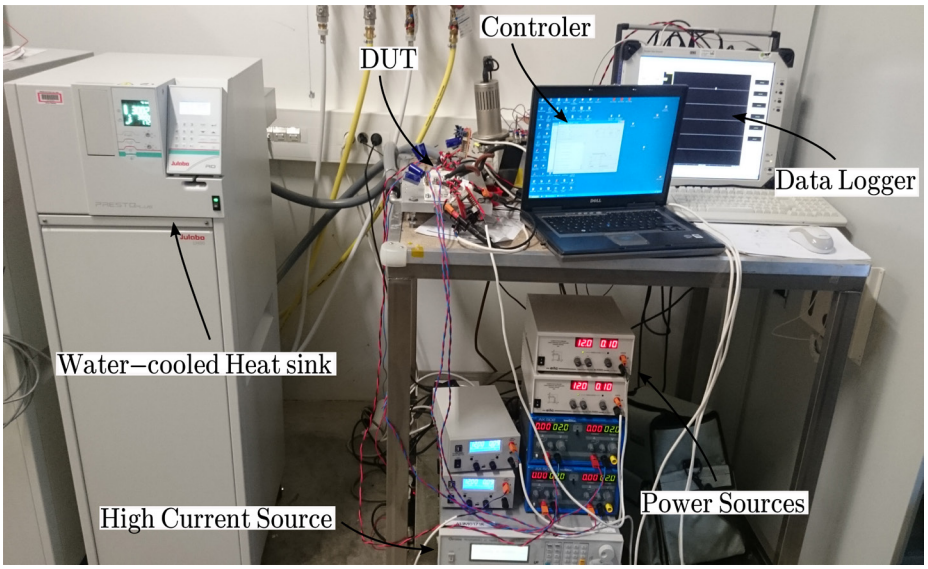


Fig. 3.23: Thermal impedances measurement's test bench

3.5.4.3. Temperature estimation during cooling

Since the transition between the high current and the low current is not instantaneous, some electrical transients occur after this event. Hence, the value of the TSEP should not be used to estimate the junction temperature during a given time (typically several µs to several tens of µs). Consequently, an extrapolation is crucial to estimate the junction temperature T_{J_h} before the current variation. The corresponding time is noted $t = 0$. Accordingly, a linear extrapolation was performed on the TSEP curve during the cooling phase, assuming that the temperature decreases linearly with the square root of time [63] [64] [66]. Fig. 3.24 represents an example of the linear extrapolation of V_{ce} in the case of the IGBT power modules.

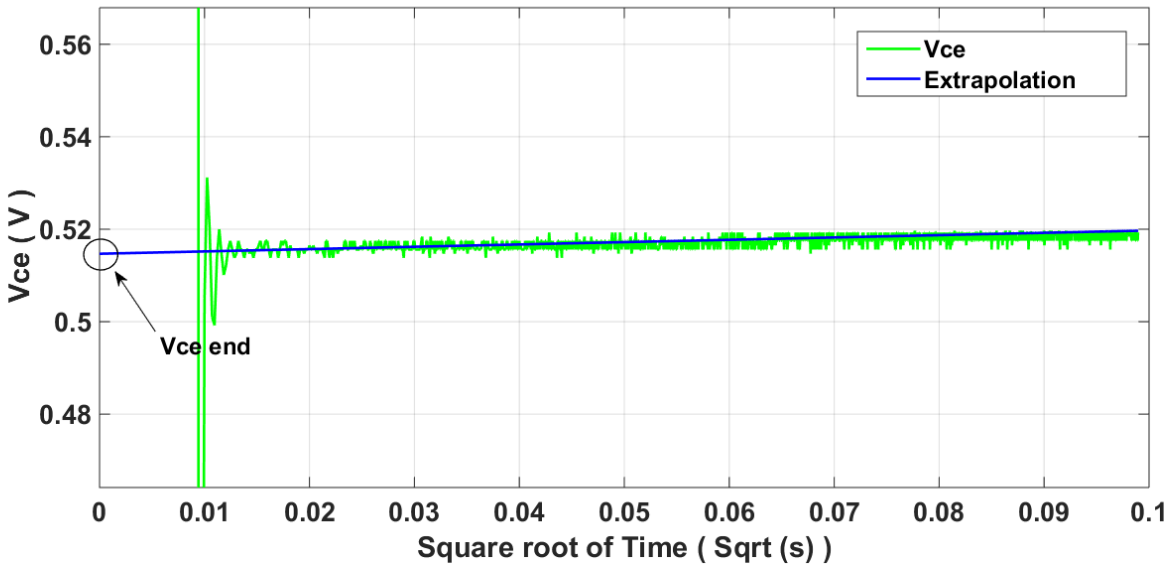


Fig. 3.24: Linear extrapolation of V_{ce} represented as a function of the square root of time

3.5.5. Results

3.5.5.1. Results of the thermal impedances measurements and fitting

The junction temperature before switching T_{J_h} being determined, the thermal impedances can be calculated as explained in Eq. 3.27. Fig. 3.25 demonstrates the acquired thermal impedances in the case of the IGBT inverter, whereas Fig. 3.26 represents them in the case of the SiC MOSFET inverter. The thermal impedances in these figures are classified into four categories as follows:

Cat1: Self-heating Z_{th}
Cat2: Mutual Z_{th} between the transistor and its antiparallel diode, and vice versa
Cat3: Mutual Z_{th} between two semiconductors in the same power module
Cat4: Mutual Z_{th} between two semiconductors in different power modules

It can be noticed from these two figures that the mutual thermal coupling impedances between two semiconductors in different power modules (Cat4) are very low, thus can be neglected. However, the mutual impedances between the semiconductors inside the same module (Cat2 and Cat3) are relatively high in comparison with the self-heating thermal impedances (Cat1). Therefore, it is vital to consider the thermal coupling between the semiconductors in the inverter in order to accurately build its thermal model.

After the measurement campaigns, all the thermal impedances were fitted with the Least Squares Methods. Z_{th} from Cat1 and Cat2 were fitted with 6 R-C cells, whereas Z_{th} from Cat3 were fitted with 3 R-C cells, while Z_{th} from Cat4 were fitted with 2 R-C cells. Note that the fitting equation is not important in itself, since the Foster network doesn't have any physical significance in any way. Fig. 3.27 represents an example of the Z_{th} fitting for D_1, in the case of the IGBT inverter (refer to Fig. 3.21). Note that Z_{ii} represents the Junction-Ambient self-heating thermal impedance of the device D_i, whereas Z_{ji} represents the mutual thermal coupling impedance between D_j and D_i.

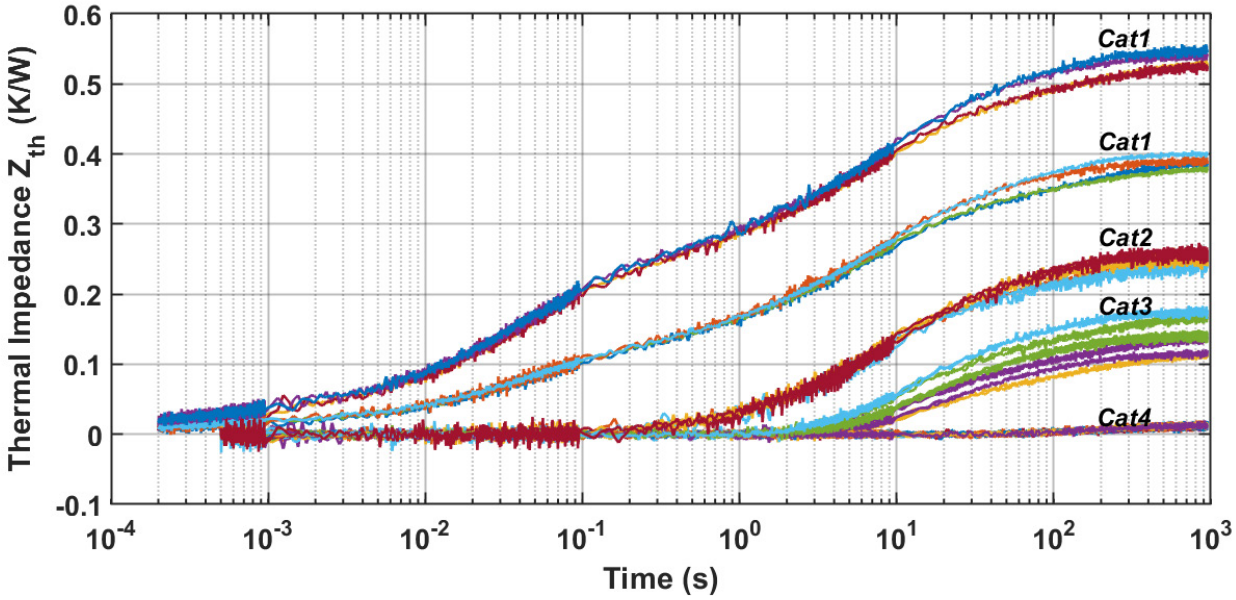


Fig. 3.25: Measured thermal impedances in the case of the IGBT inverter

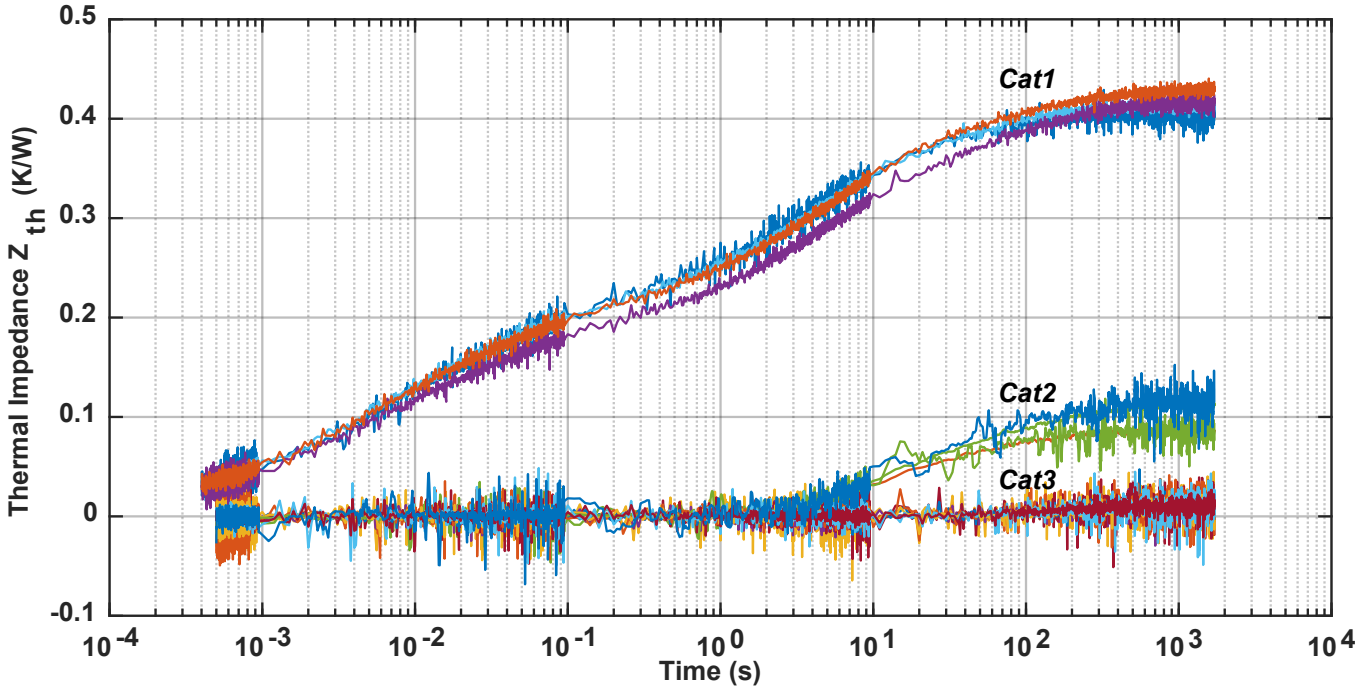


Fig. 3.26: Measured thermal impedances in the case of the SiC MOSFET inverter

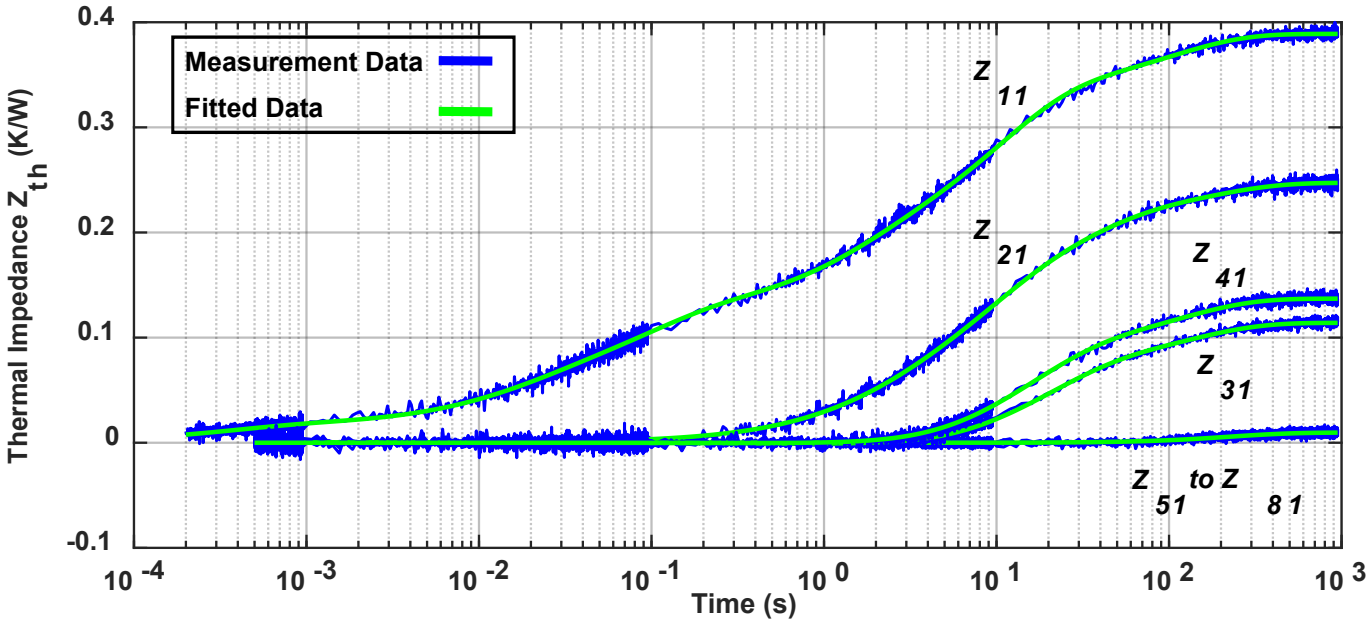


Fig. 3.27: Fitting the thermal impedances for device D_1 in the case of the IGBT inverter

3.5.5.2. Estimating the junction temperature

The thermal coupling between devices is considered to be practical for systems with up to only four or five power devices as stated in [118]. In fact, as the number of devices increases, the number of equations that have to be solved simultaneously increases rapidly. Moreover, by considering the electro-thermal effects due to temperature-dependent

parameters, the calculations become very complicated. Consequently, the values of the devices' power losses have to be updated after the estimation of the devices' junction temperature at each iteration of the code.

However, since the created thermal model's resolution was optimized using Eq. 3.26 and showed high performance in terms of computation speed (Table 3.3), hence the problem of the high number of devices was finally overcome. Actually, it takes approximatively 5 s to estimate the junction temperatures of the 8 devices in the IGBT inverter (4 IGBTs + 4 external antiparallel diodes), corresponding to a current's profile of 12 h long. Now in order to estimate simultaneously all the devices' junction temperatures, the following matrix form should be solved at each code iteration:

$$\begin{pmatrix} T_{J_1} \\ T_{J_2} \\ T_{J_3} \\ T_{J_4} \\ T_{J_5} \\ T_{J_6} \\ T_{J_7} \\ T_{J_8} \end{pmatrix} = \begin{pmatrix} Z_{11} & Z_{21} & Z_{31} & Z_{41} & Z_{51} & Z_{61} & Z_{71} & Z_{81} \\ Z_{12} & Z_{22} & Z_{32} & Z_{42} & Z_{52} & Z_{62} & Z_{72} & Z_{82} \\ Z_{13} & Z_{23} & Z_{33} & Z_{43} & Z_{53} & Z_{63} & Z_{73} & Z_{83} \\ Z_{14} & Z_{24} & Z_{34} & Z_{44} & Z_{54} & Z_{64} & Z_{74} & Z_{84} \\ Z_{15} & Z_{25} & Z_{35} & Z_{45} & Z_{55} & Z_{65} & Z_{75} & Z_{85} \\ Z_{16} & Z_{26} & Z_{36} & Z_{46} & Z_{56} & Z_{66} & Z_{76} & Z_{86} \\ Z_{17} & Z_{27} & Z_{37} & Z_{47} & Z_{57} & Z_{67} & Z_{77} & Z_{87} \\ Z_{18} & Z_{28} & Z_{38} & Z_{48} & Z_{58} & Z_{68} & Z_{78} & Z_{88} \end{pmatrix} \cdot \begin{pmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \\ P_5 \\ P_6 \\ P_7 \\ P_8 \end{pmatrix} + T_A \cdot \begin{pmatrix} 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \\ 1 \end{pmatrix} \quad (3.28)$$

The MOSFET thermal model can be solved similarly using a $4x4$ Z_{th}-matrix instead with only 16 thermal impedances.

3.6. Conclusions

In this chapter, a numerical thermal model based on Foster networks was built with *Matlab* to estimate the semiconductors' junction temperatures in a two-level DC/AC inverter, with IGBT and SiC MOSFET power modules.

Then, six T_J calculation methods were tested and compared in terms of execution time and ability to consider the electro-thermal coupling. These methods are: time-domain estimation, fast Fourier transform FFT, FFT with overlap-add method, breaking down mission profile into single pulses, and lastly an analytical solution. These methods provide the same temperature results which allow their validation. However, the analytical solution showed the highest performance in term of execution time, mostly with very long mission profiles. Furthermore, it allows considering the electro-thermal effect every T_{out}, by updating the power losses mission profile at each code iteration. Hence, this method was selected to be used in the final *Matlab* thermal model.

The thermal model was then validated using several simulators. Accordingly, the simulators *PSIM*, *IPOSIM* (*Infineon*) and *SemiSel* (*Semikron*) were selected to validate the IGBT model, whereas *SpeedFit* (*WolfSpeed*) was chosen to validate the SiC MOSFET's model.

For estimating the junction temperatures in the test benches (which will be depicted in Chapters 5 and 6), measurement tests of the self-heating and the mutual thermal coupling impedances were performed in the case of IGBT and SiC MOSFET inverters. These measurements were done using a classical method by measuring a TSEP during the cooling of

the DUT. In the case of IGBT, the chosen TSEP was the collector-emitter voltage V_{ce}, as for the diode and the SiC MOSFET the chosen TSEP was the diode's forward voltage.

Correspondingly, the methodology and the test benches of the thermal impedances measurements were depicted, and the results of the measurements were represented, and fitted with the Least Squares Methods. The obtained mutual thermal coupling impedances were not negligible in comparison with the self-heating impedances.

Lastly, the measured impedances were implemented in the final sophisticated thermal model of the IGBT and the SiC MOSFET DC/AC inverters. This model, coupled with the power losses estimation model of Chapter 2, will be used to estimate the semiconductors' junction temperatures, corresponding to given power losses mission profiles, with more than 800 million samples.

The power loss model and the thermal model represented in Chapters 2 and 3 respectively, will be used in the next chapters in order to define an accelerated ageing profile representative of the photovoltaic application for both the IGBT and SiC MOSFET power modules.

Chapter 4:
Accelerated ageing methodology: from mission profiles to semiconductors accelerated ageing tests

Chapter 4: Accelerated ageing methodology: from mission profiles to semiconductors accelerated ageing tests

4.1. Introduction

This chapter presents a new method of accelerated ageing of photovoltaic (PV) inverters' semiconductors, created by analyzing mission profiles of current and ambient temperature, extracted over several years from different photovoltaic power plants (refer to Fig. 1.36). Many characteristics of the photovoltaic application are represented and analyzed, such as the shape of the inverter's RMS output current, the diffuse current, the slope of the current variations, the difference between the seasons, the delays between the current variations, and the ambient temperature.

Accordingly, two accelerated ageing methods are developed considering all the characteristics mentioned above. The 1st method generates maximum current variations, whereas the 2nd one reproduces the real current variations extracted from measured mission profiles.

As represented in Fig. 4.1, the power losses estimation model (Chapter 2) as well as the thermal model (Chapter 3) are used to estimate the junction temperature profiles, corresponding to different current and ambient temperature profiles. The 1st one corresponds to real current mission profiles, the 2nd one corresponds to accelerated ageing profile built with the 1st method, the 3rd one corresponds to accelerated ageing profile built with the 2nd method, and finally the 4th one corresponds to a classical power cycling current profile. In Fig. 4.1, I represents the RMS current profile at the output of the inverter over a fundamental period $T_{out} = 20\ ms$. P represents the semiconductor power losses profile, T_J the junction temperature profile, ΔT_J the temperature swings, T_{J_M} the mean temperature of each temperature swing and T_a the ambient temperature.

Next, a cycle counting algorithm named Rainflow is appointed to extract the cycles from the junction temperature profiles, as well as the corresponding T_{J_M} and ΔT_J of each extracted cycle. Then, the ageing profiles are refined according to the desired T_{J_M} and ΔT_J's distributions. Afterwards, a comparison is performed between the different profiles, regarding the distributions of ΔT_J and T_{J_M}. Finally, the tests' duration is estimated using Palmgren-Miner rule with a lifetime estimation model, and then the profiles for the IGBT and MOSFET ageing tests are designed using the adequate method.

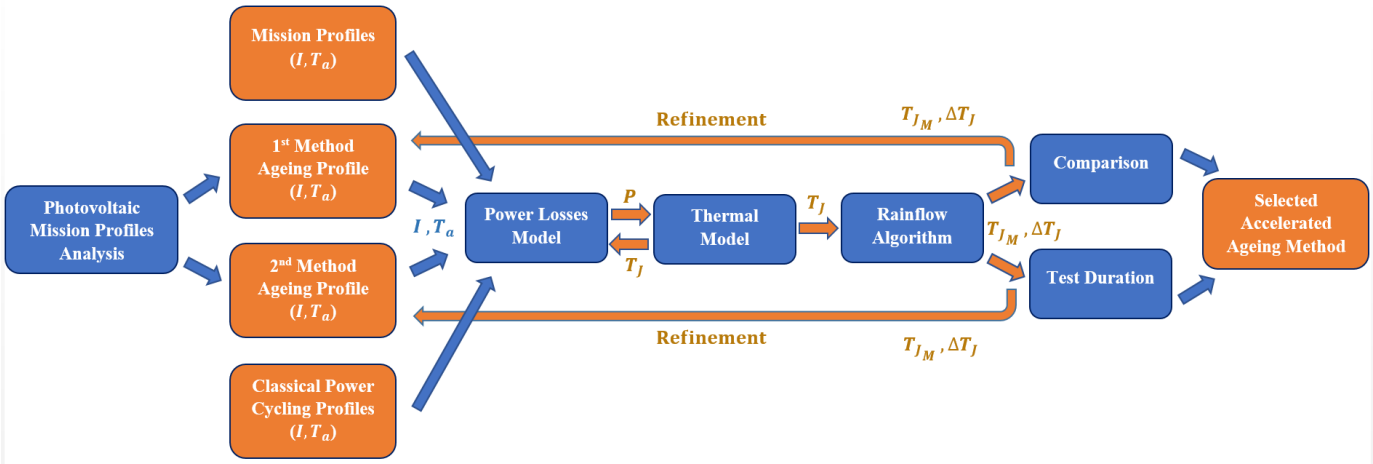


Fig. 4.1: Full approach of the study

4.2. Methodology for accelerated ageing profiles generation

4.2.1. Analysis of photovoltaics' mission profiles

As mentioned in Chapter 1, the aim of this study is to create an accelerated ageing method, generating thermo-mechanical stress in the semiconductors, considering the photovoltaic application. Thus, mission profiles of inverters' RMS output current and ambient temperature are extracted from four photovoltaic power plants, located in the south of France over the years 2013, 2014 and 2015. The mean power range of the power plants is ~ 4 MW (16 MW maximum), while the data sampling rate of extracted mission profiles is 1S/5s. Due to similarities within the data, one mission profile over a single year serves as an example in this chapter.

In the case of the photovoltaic application, the RMS current at the output of the inverter is proportional to the solar irradiance, which in its turn can be described with mathematical equations arising from the rotation of the earth around itself (variation over a day) and around the sun (variation over a year). The profiles of the current and ambient temperature can show clear sky days as in Fig. 4.2, or cloudy days as in Fig. 4.3, highlighted in Fig. 4.4. The variations of the current as represented in Fig. 4.3 lead to numerous and sudden variations of semiconductors' junction temperature during the day. These variations are an important factor of the inverter semiconductors' damaging as found in the literature in case of IGBT power modules [119] [120]. By analyzing the current profiles, several characteristics can be identified, as it will be presented in the upcoming sections. It should be noted that the values of certain parameters may depend on the power plant's location and size.

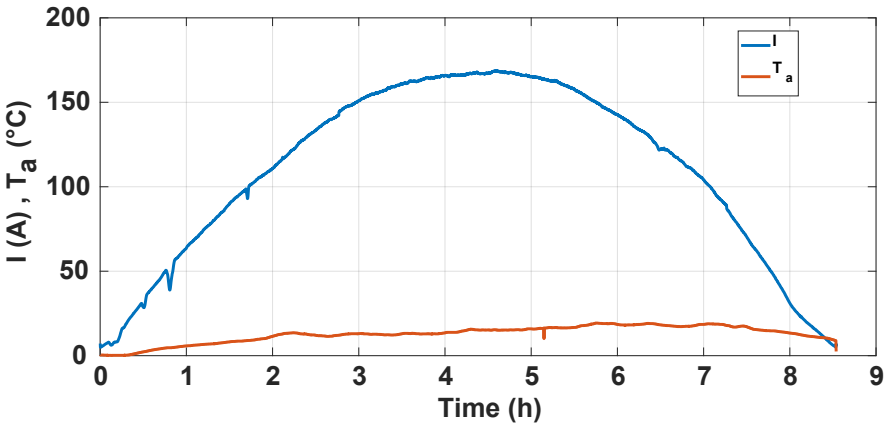


Fig. 4.2: ***I* and T_a mission profiles over a clear sky day**

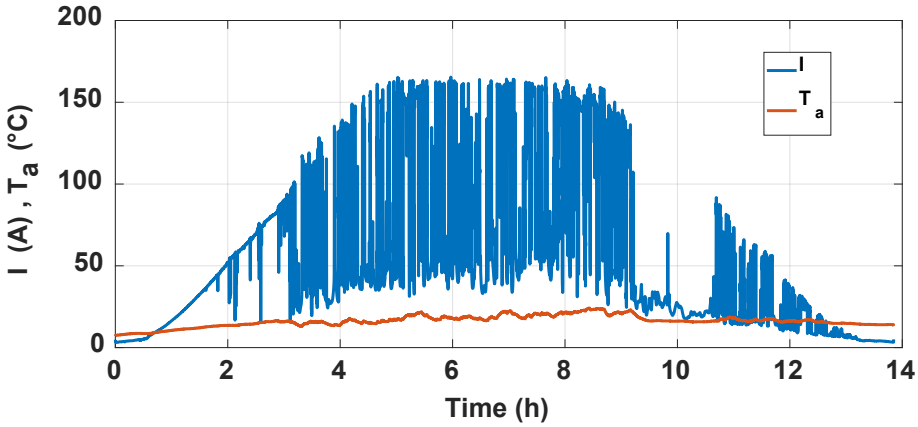


Fig. 4.3: ***I* and T_a mission profiles over a cloudy day**

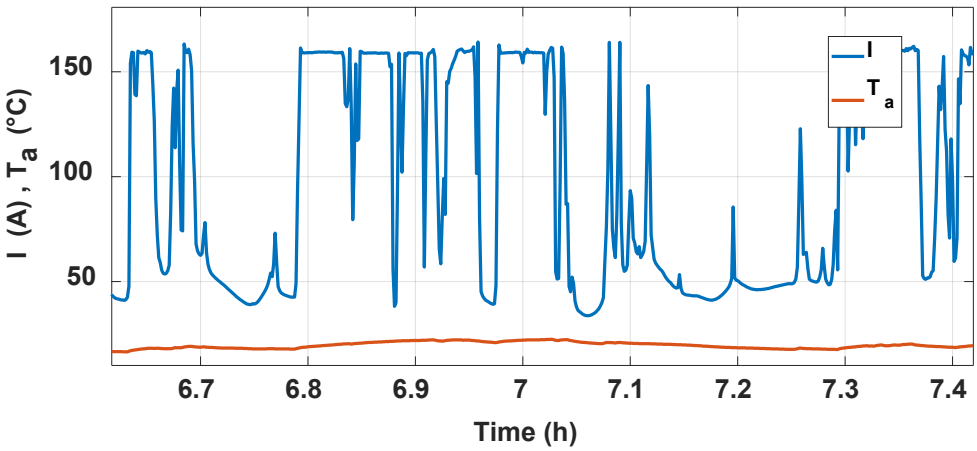


Fig. 4.4: **Highlight on several current variations from Fig. 4.3**

4.2.1.1. The shape of the current

As it can be noticed in Fig. 4.2, the shape of the RMS output current of the DC/AC inverter during the sunshine can be described by a complex mathematical equation as follows:

$$\alpha \cdot sin(t) \cdot \cos(t) \tag{4.1}$$

where t is a parameter that depends on time, and α a variable representing several parameters, such as the geographical area, the orientation of the photovoltaic panels and many others [121]. The number of sunshine hours depends on the season as well as on the geographical zone, while no current is produced by the PV panels during the night.

4.2.1.2. The diffuse current

The minimum value that the current can reach during a given day is proportional to the diffuse solar radiation. This latter -represented over one day in Fig. 4.5- results from diffraction of sunlight by the clouds and its scattering by the various molecules and particles suspended in the atmosphere, as well as from its refraction by the ground. This is therefore a radiation which does not follow a defined direction by the sun, in the direction of the observation point on the surface of the Earth. The global radiation is equal to the sum of direct and diffuse radiations, where diffuse radiation at a given moment is close to 10% of the global radiation. Hence, the current produced during the passage of clouds at a given moment is close to 10% of the total current that the PV panels produced directly before the passage of the clouds [122].

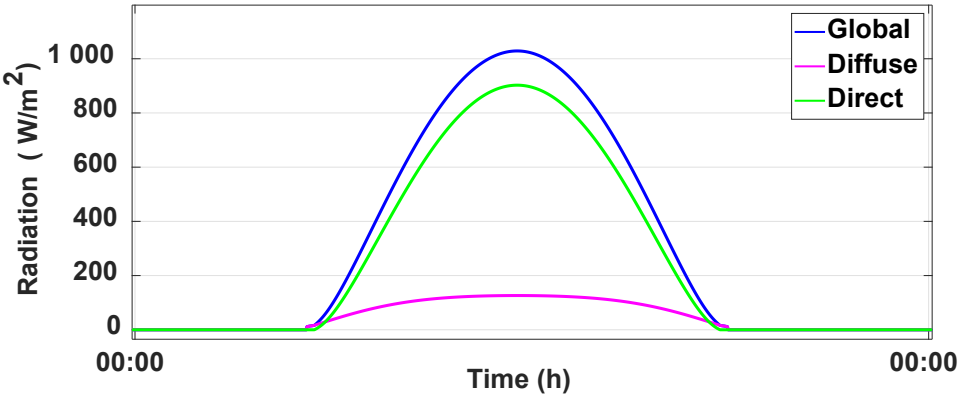


Fig. 4.5: Solar radiation over one day

4.2.1.3. The slope of the current variations

During traditional power cycling tests, the variations of the current are abrupt, which may accelerates the damaging of the module, potentially in a non-representative way. As far as we know, the current variations' slope has never been studied in the literature, despite the fact that the thermo-mechanical stress may be dependent of it. Thus, it was an interesting fact, during this study to consider the current variations slope during the accelerated ageing of the semiconductor devices. In order to build a profile that accelerates the ageing of the power modules of the DC/AC photovoltaic inverter, slight current variations are neglected. Thus, only the current variations higher than ΔI_{min} leading to $\Delta T_J \geq 30\ K$ were retained, where the value of $30\ K$ is arbitrary selected. The value of ΔI_{min} can be determined using the thermal model described in Chapter 3. Fig. 4.6 represents the extraction of current's considerable variations over several days represented with a red line, with a highlight on several variations represented in Fig. 4.7 as a function of time.

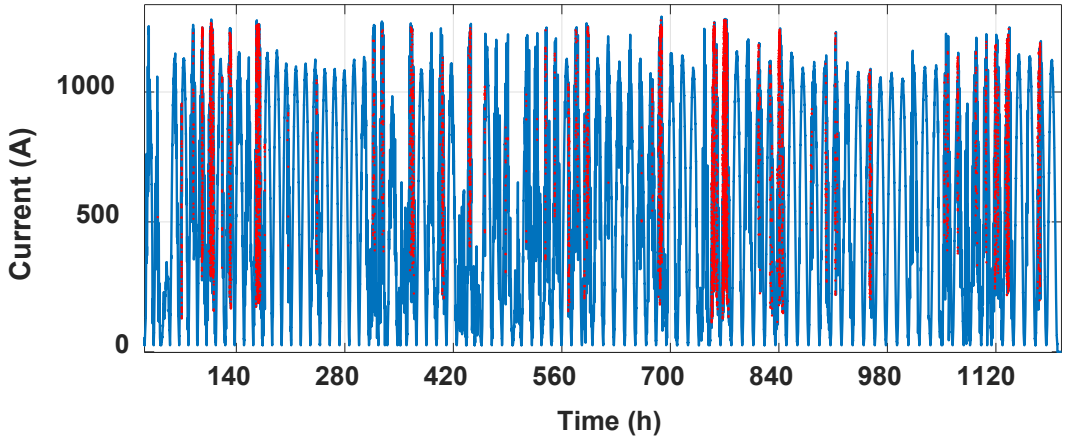


Fig. 4.6: Extraction of current's considerable variations

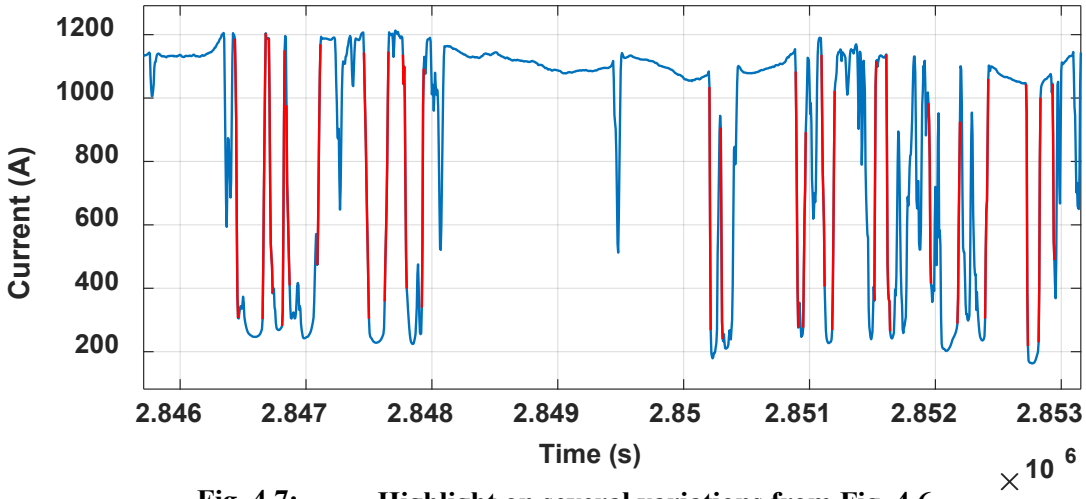


Fig. 4.7: Highlight on several variations from Fig. 4.6

As shown in Fig. 4.7, the variation's speed of the RMS current value can be very fast due to cloudy passageway. Actually, it depends on the wind speed as well as on the size of the photovoltaic power plant. Considering the available data, the slope of these sudden variations is estimated to be:

$$\frac{\Delta I}{\Delta t} = 0.15 \cdot I_{MAX} \text{ (A/s)} \tag{4.2}$$

where I_{MAX} is the maximum RMS current reached during one year. This specific value of the photovoltaic application is obtained through statistical studies, carried out on current measurements at the output of photovoltaic power plants located in south of France, hence it may be different in another geographical zone.

4.2.1.4. Delays between the current variations

As mentioned previously, slight current variations are neglected in this study, thus only the delays between the current variations higher than ΔI_{min} are therefore considered. The histogram illustrated in Fig. 4.8 represents the percentage of occurrences of the delays between these big variations, in other words the delays between two consecutive passages of

clouds inducing high temperature swings. More than 50% of these delays are higher than 120 s , while more than 40% are between 10 s and 115 s.

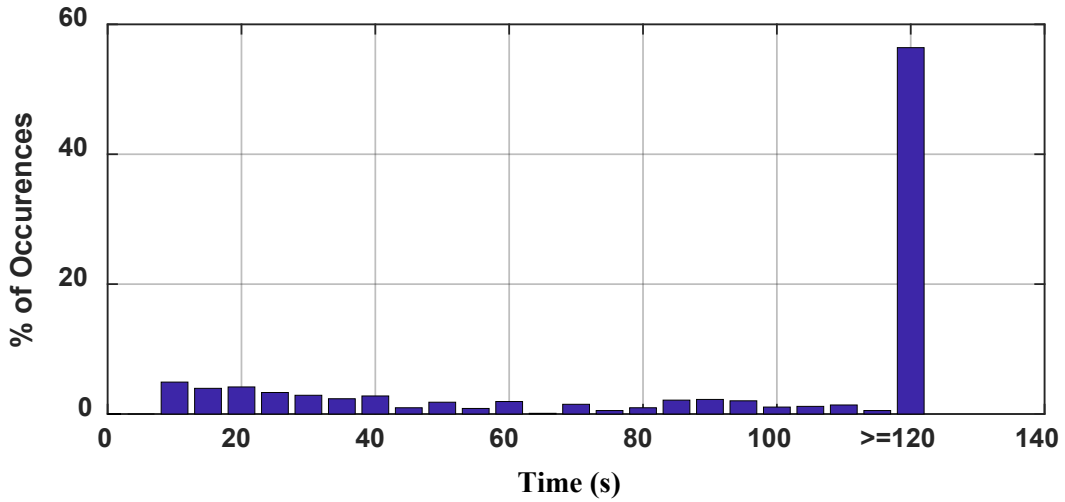
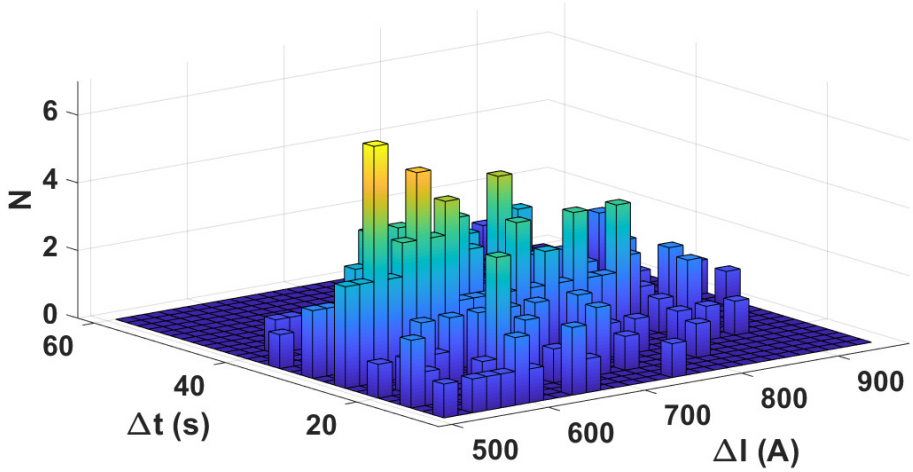


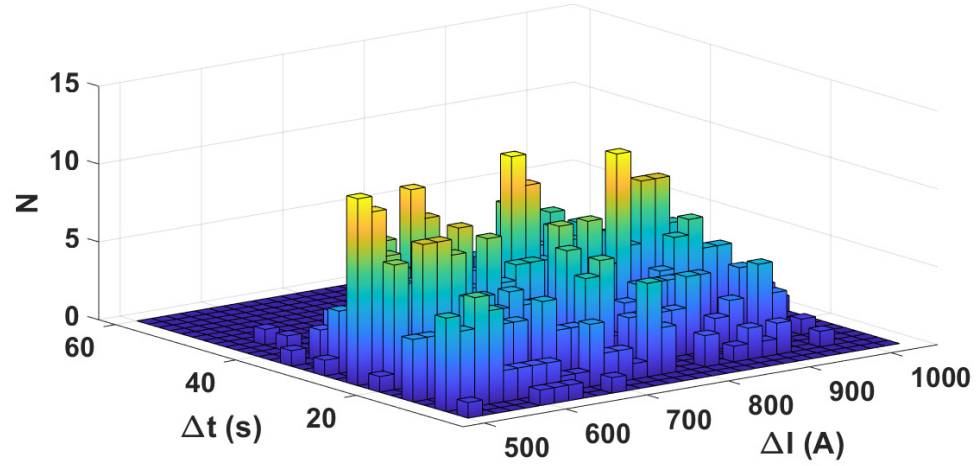
Fig. 4.8: Histogram of occurrences (in percentage) of the delays between two consecutive big variations of the current

4.2.1.5. Seasons

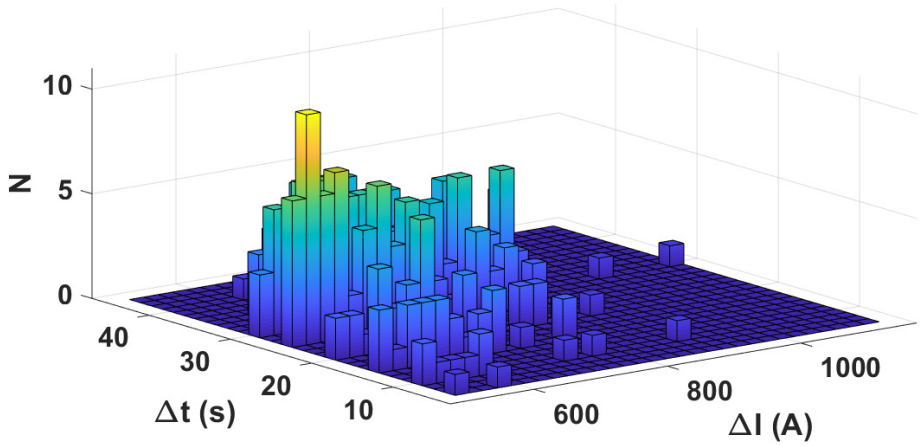
By analyzing the photovoltaic mission profiles, it can be noticed that all the current's characteristics represented previously are unconstrained by the seasons. However, in the south of France, it is noticeable that Spring is the most constraining season, since it brings at the same time a high number of sunshine hours, high radiation levels and a maximum number of high current variations due to the cloudy periods. The number of occurrences of the current's variations as a function of their duration and amplitude is represented in Fig. 4.9.a, Fig. 4.9.b, Fig. 4.9.c and Fig. 4.9.d for Winter, Spring, Summer and Fall respectively.



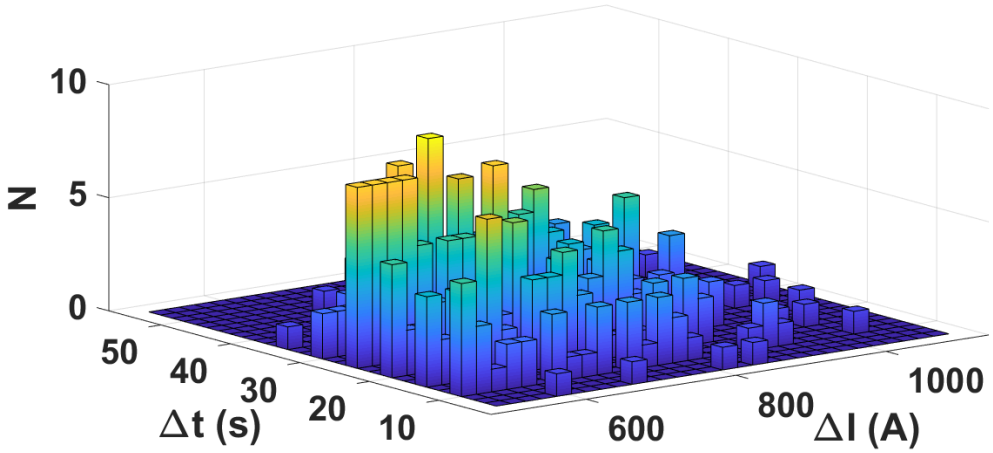
a) Winter



b) Spring



c) Summer



d) Fall

Fig. 4.9: Histograms representing the number of occurrences of the current's variations as a function of their duration and amplitude

4.2.1.6. Ambient Temperature

Ambient temperature has a sinusoidal shape during the day (without considering the night), as represented in Fig. 4.10, with its extreme values dependent on the geographical zone. It is noticeable that during the day, the temperature variations can be higher than 20°C. Generally, it varies over the year as represented in Fig. 4.11.

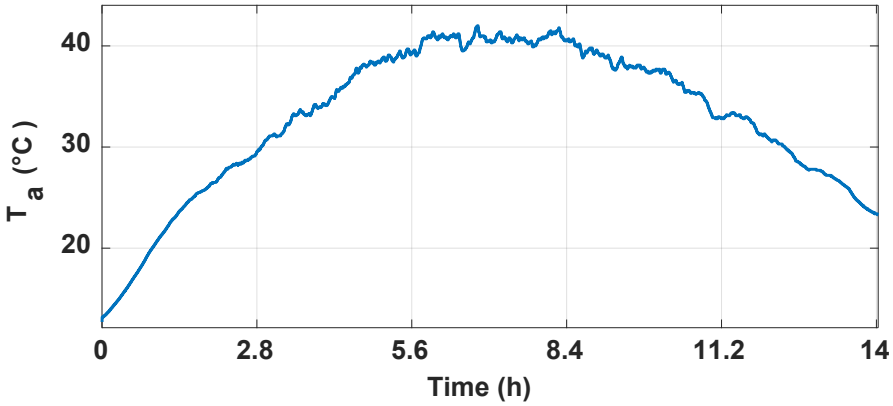


Fig. 4.10: Ambient temperature profile over one day

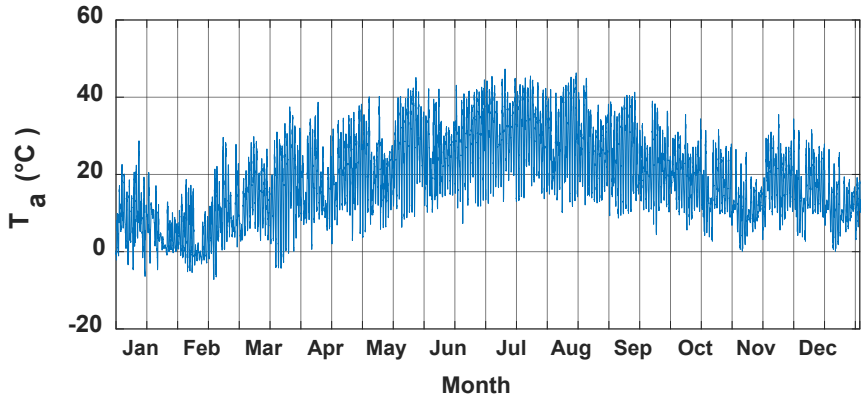


Fig. 4.11: Ambient temperature profile over year 2015

4.2.2. 1st method: Generating maximum variations

4.2.2.1. Building the accelerated ageing profile

Considering the characteristics of the photovoltaic mission profiles represented in the last section, this study proposes the accelerated ageing profile represented in Fig. 4.12. This profile of approximately 8.7 h has the same shape as that of a one day PV mission profile (without considering the night). Similarly to the real application, the maximum RMS current profile has a sinusoidal shape (Section 4.2.1.1) while the minimum current value after a current drop is equal to 10% of the current's value before the occurrence of the variation (Section 4.2.1.2). Hence, the current's variation at a given time can be expressed as follows:

$$\Delta I = 0.9 \cdot I_{Clear} \tag{4.3}$$

where I_{Clear} represents the RMS current's value before a current drop or after a current rise (corresponding to a clear sky). This parameter is represented in Fig. 4.13 highlighting Fig. 4.12, where I_{MAX} represents the peak value of the RMS current.

It is noticeable that a truncation is applied at both extremes of the profile, so that the current value starts at I_{LIMIT} instead of 0 to prevent inducing $\Delta T_J < 30$ K, by applying $\Delta I \geq \Delta I_{min}$. Hence, the value of I_{LIMIT} can be determined after the application of the thermal model. As described in Section 4.2.1.6, and as it can be seen in Fig. 4.12, the ambient temperature T_a has a sinusoidal shape varying between $T_{a_{min}}$ and $T_{a_{max}}$. As detailed in Section 4.2.1.3 the slope $\frac{\Delta I}{\Delta t} = 0.15 \cdot I_{MAX}$ (A/s), while T_{on} and T_{off} (Section 4.2.1.4) represent the delays between two current variations, as illustrated in Fig. 4.13.

Eventually, and since the characteristics of the current profiles are the same during the 4 seasons, it was decided to represent them all with a unique profile. This current profile is applied sequentially during the power cycling using the opposition method, where a thermal cycling is applied simultaneously by varying the ambient temperature. The time delay between two consecutive ageing profiles $t_p = 15\,minutes$ allows for the relaxation of the viscoelastic constraints in the power module [123] [124].

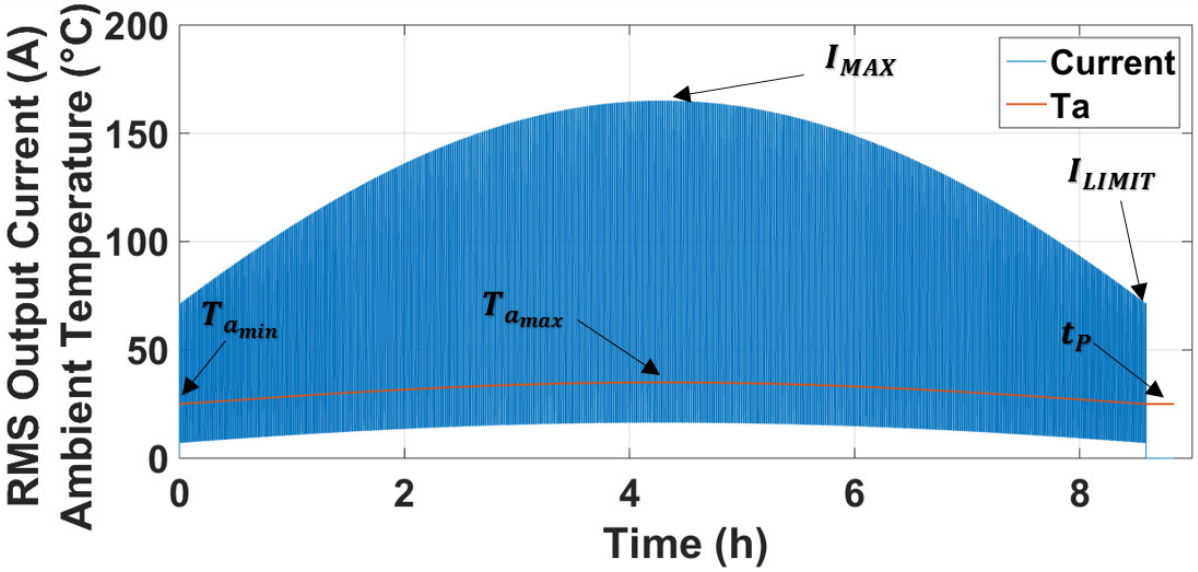


Fig. 4.12: Accelerated ageing profile simulating one day of real application

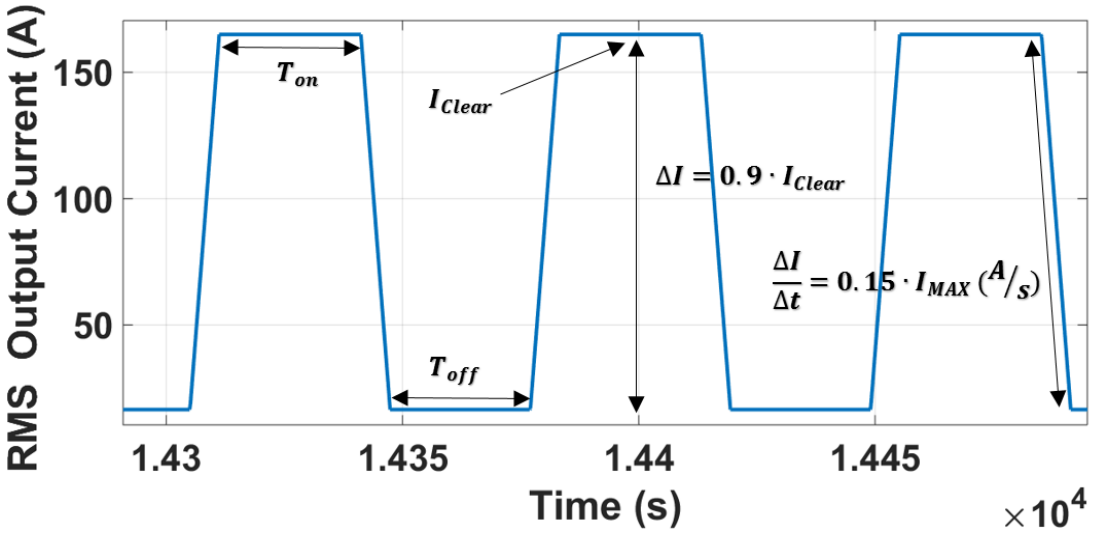


Fig. 4.13: Highlight on several current's variations

4.2.2.2. Determining the profile parameters

This section demonstrates an example of the method implementation, in pursuance of determining the parameters values of the accelerated ageing profile, using simplified power losses and thermal models.

4.2.2.2.1. Case Study

This method is applied on a two-level three-phase photovoltaic inverter with a DC-link voltage E of 1200 V, phase to phase output voltage of 690 V, grid frequency f_{out} = 50 Hz, modulation factor m = 0.95, switching frequency f_{sw} = 20 kHz, and power factor cosφ = 1. The SiC MOSFET power module *CAS300M17BM2* (1700V-300A phase-leg power module with Schottky antiparallel diodes and maximum junction temperature $T_{J_{MAX}} = 150\,°C$) is selected to conduct this study. Ultimately, the heat sink is considered to have a time constant $\tau_H = 10\ s$, corresponding to a water-cooled heat sink.

4.2.2.2.2. Power losses and thermal models

The power losses and thermal models are used to estimate the corresponding power devices T_J for a given current profile. These models use advanced equations as mentioned in Chapter 3 to shorten the computation time for mission profiles over several years with important number of samples [117].

The thermal model is based on the use of thermal impedances $Z_{th_{CH}}$ (Case-Heat sink) and $Z_{th_{JC}}$ (Junction-Case) obtained from the manufacturer's datasheet. $Z_{th_{HA}}$ (Heat sink-Ambient) is estimated considering the heat sink's time constant $\tau_H = 10s$, while the global thermal impedance is determined using Foster equivalent networks [38] [77] [83].The value of $R_{th_{HA}}$ -the Heat sink-Ambient thermal resistance- is selected in a way to prevent T_J from exceeding 130 °C. Considering the heat sink's time constant and the histogram represented in Fig. 4.8, where more than 85% of the time delays between the variations are higher than $30s$ $(3\tau_H)$, T_{on} and T_{off} were selected to be equal to $30s$, to maximize the number of large temperature swings ΔT_J. Furthermore, using the thermal model, ΔI_{min} is found to be equal to 43% of I_{MAX}.

After introducing the accelerated ageing profile into the thermal model, the "Rainflow Algorithm" (depicted in Section 4.3.1) is applied to the resulting junction temperature profile, to obtain the corresponding ΔT_J and T_{J_M}. Accordingly, the accelerated ageing profile parameters are refined until obtaining the desired ΔT_J and T_{J_M}. By Using the thermal model on this example it was found that the variations of the junction temperature can be maximized by altering the ambient temperature between $T_{a_{min}} = 25\,°C$ and $T_{a_{max}} = 35\,°C$. The resulting junction temperature profile is presented in Fig. 4.14, where it can be seen that the maximum T_J is 130°C. Fig. 4.15 highlights Fig. 4.14 where the maximum junction temperature swing is ≅ 85°C.

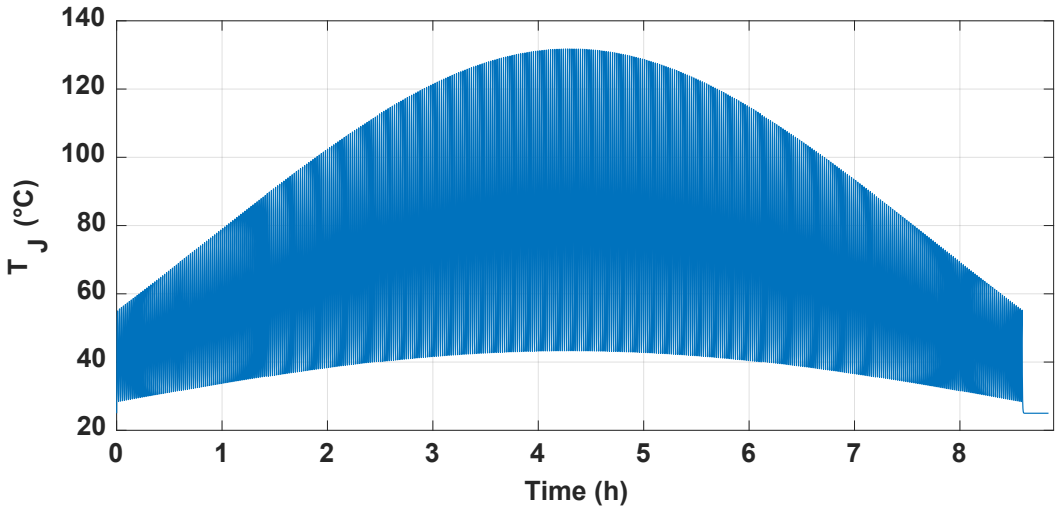


Fig. 4.14: MOSFET junction temperature's profile during the accelerated ageing (representing one day)

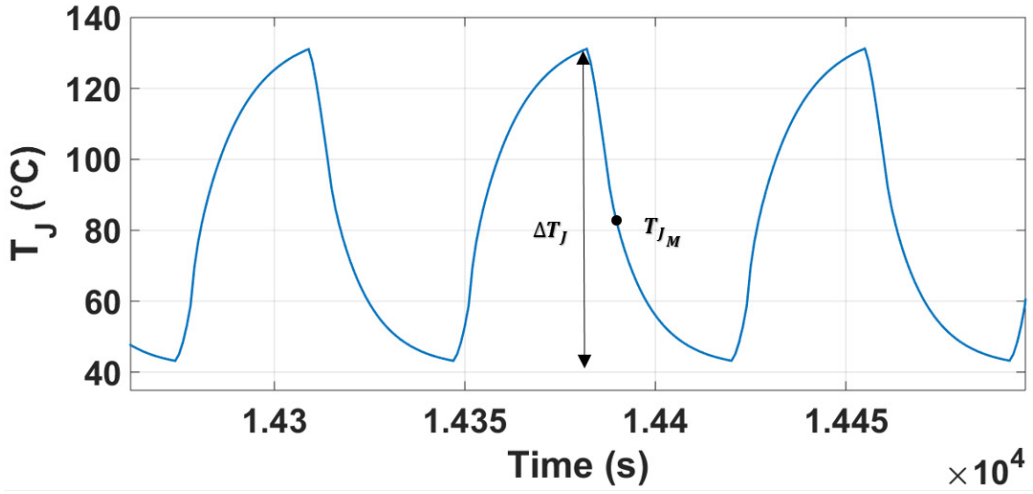


Fig. 4.15: Highlight on several junction temperature variations from Fig. 4.14

4.2.3. 2nd method: Regenerating real variations

In this method, all the variations of the RMS current which exist in the real measured profile over one year, and which generate $\Delta T_J \geq 30\text{K}$ are extracted and rearranged in the new accelerated ageing profile. Hence, instead of introducing current's variations $\Delta I = 0.9 \cdot I_{Clear}$ (as in the case of the first method), which is the maximum value of the variations induced by the passage of clouds, the 2nd method reproduces the real current variations ΔI of the measured current with slight modifications. Fig. 4.16 shows an example of the significant variations' extraction from the measured mission profile. Once these variations extracted, the long delays between them are reduced to 30 s, in order to accelerate the ageing test. Consequently, the same number of significant current's variations occurring during one year of application are accumulated in one accelerated ageing profile of approximately 36 hours long. Moreover, the variations are rearranged in a symmetrical way as visible in Fig. 4.17, in order to obtain similar shape as that of the mission profile over a cloudy day.

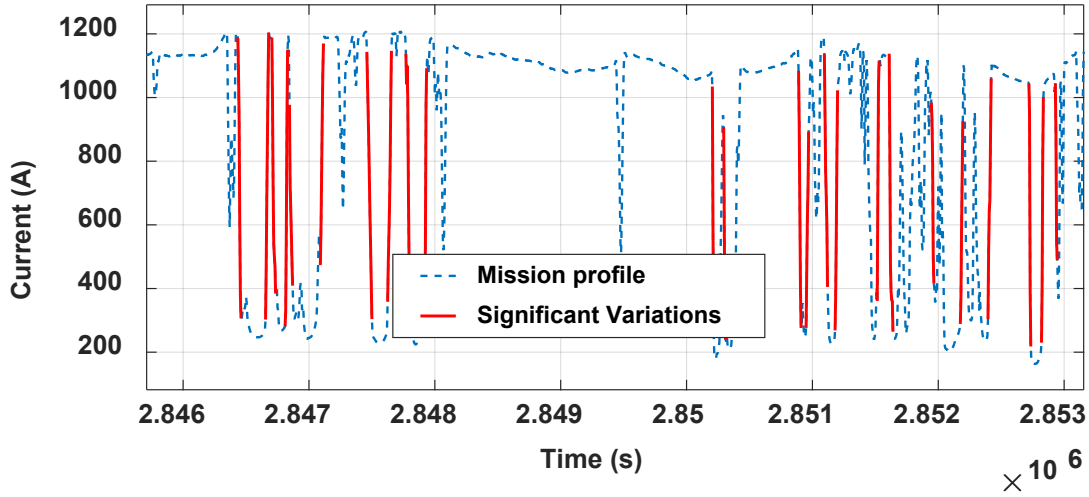


Fig. 4.16: Extraction of the significant variations from the current's profile

It should be noted that the two accelerated ageing profiles have same values of $\frac{\Delta I}{\Delta t}, T_{on}, T_{off}, I_{LIMIT}$ and t_P, whereas the only differences reside in ΔI and T_a values. In fact, the ambient temperature T_a still has a sinusoidal evolution, while the values of $T_{a_{min}}$ and $T_{a_{max}}$ are modified.

After introducing the 2nd accelerated ageing profile into the thermal model, the "Rainflow Algorithm" (depicted in Section 4.3.1) is applied to the resulting junction temperature profile, to obtain the corresponding ΔT_J and T_{J_M}. The 2nd accelerated ageing profile can be obtained as represented in Fig. 4.17, after several refinements. Since the delays between the variations are shortened to accelerate the ageing test, some refinements of the profile are necessary, consisting of slightly modifying the values of T_a and the real ΔI, to obtain similar ΔT_J and T_{J_M} distributions as those of the mission profile. Fig. 4.18 highlights the 2nd profile, where the obtained ambient temperature during the refinement alternates between 25 °C and 40 °C.

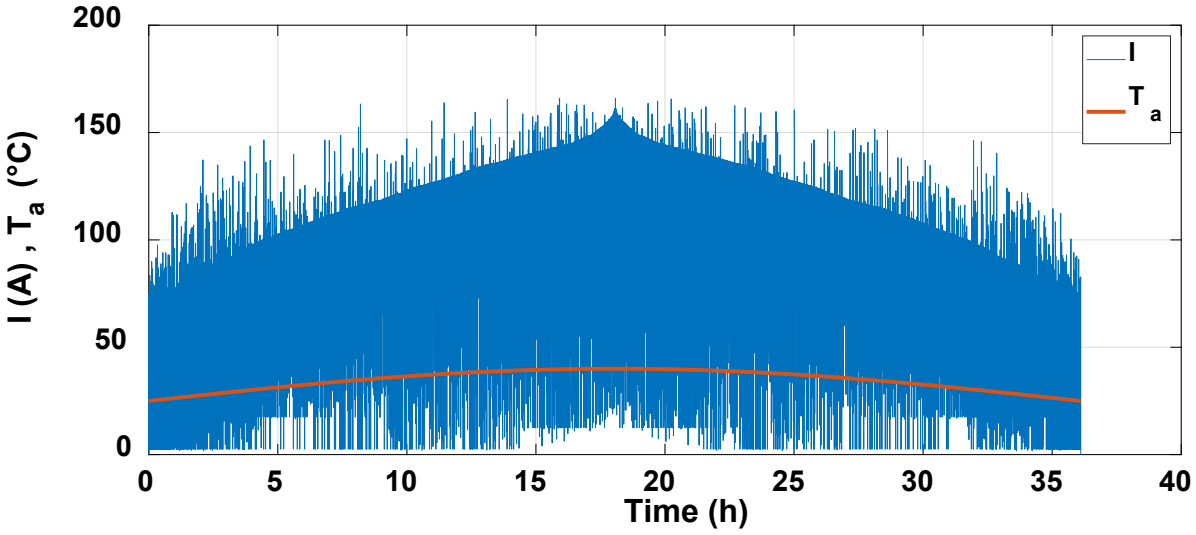


Fig. 4.17: 2nd ageing profile accumulating all the significant variations occurring over one year

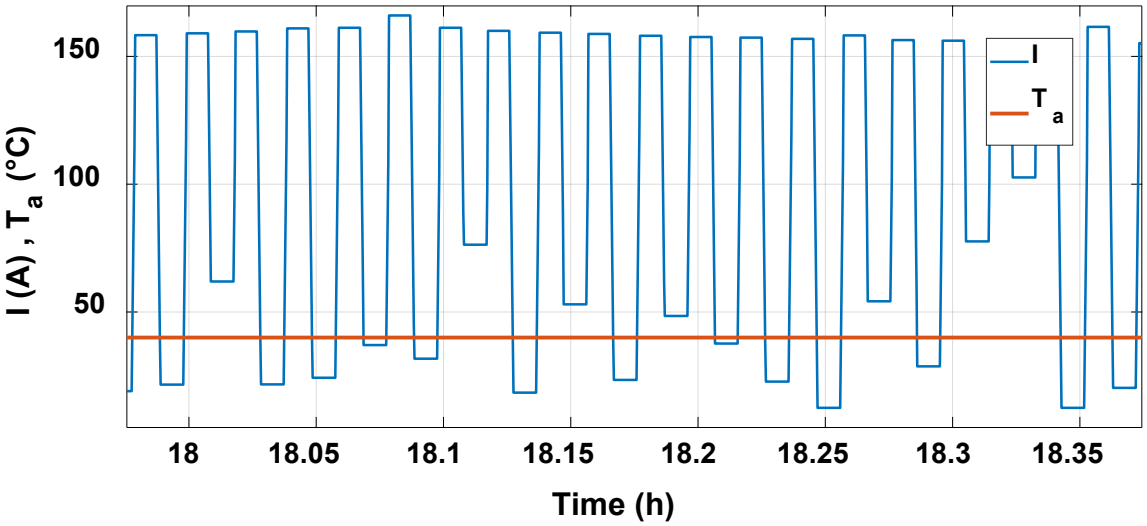


Fig. 4.18: Highlight on several current variations from the profile in Fig. 4.17

4.3. Evaluation and comparison

4.3.1. "Rainflow" counting algorithm

Cycle counting algorithms allow extracting and counting the cycles contained in a random history loading or mission profile, and determining the average values of the cycles, as well as their amplitudes. Though there are many cycle counting algorithms such as "half-cycle" peak through counting, "maximum edge" peak through counting and "rising edge" peak through counting [125], the "Rainflow" algorithm developed by Tatsuo Endo and M. Matsuishi in 1968 [126] is the most used algorithm [127] [128] [129].

For simple periodic mission profiles as shown in Fig. 4.19, counting algorithms are unnecessary since the cycles can be easily determined. However, in case of an aperiodic mission profile (Fig. 4.20), the use of counting algorithms such as "Rainflow" is very efficient to extract the cycles from it. This algorithm is based on comparing the mission profile to a "Pagoda" with rainwater flowing down its roof as shown in Fig. 4.21. The algorithm consists of the following steps [126]:

1. Reduce the mission profile by just keeping the turning points.
2. Turn the mission profile graph clockwise 90°, like the "Pagoda" roof.
3. Peaks are considered as water drops that flows down the pagoda.
4. Count the number of half cycles, considered to be achieved when either:
   - They reach the end of the mission profile.
   - They merge with a flow that started at an earlier peak.
   - They flow when an opposite peak has greater magnitude.
5. Repeat step 4 for valleys.
6. Pair up half cycles of identical magnitude with opposite sense to count the number of complete cycles.

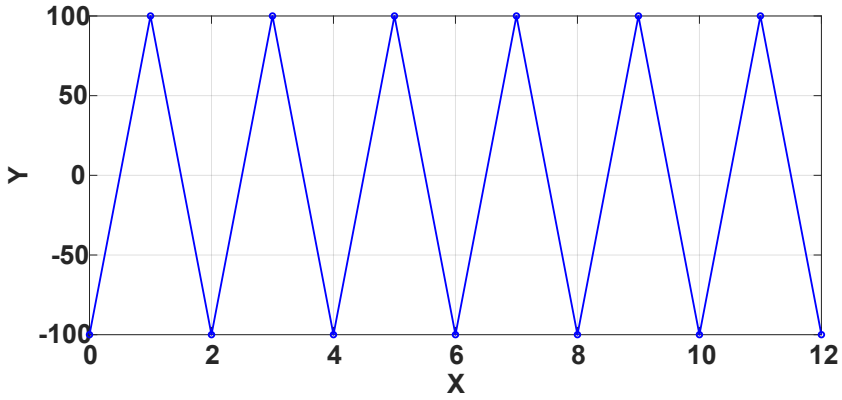


Fig. 4.19: Periodic Signal

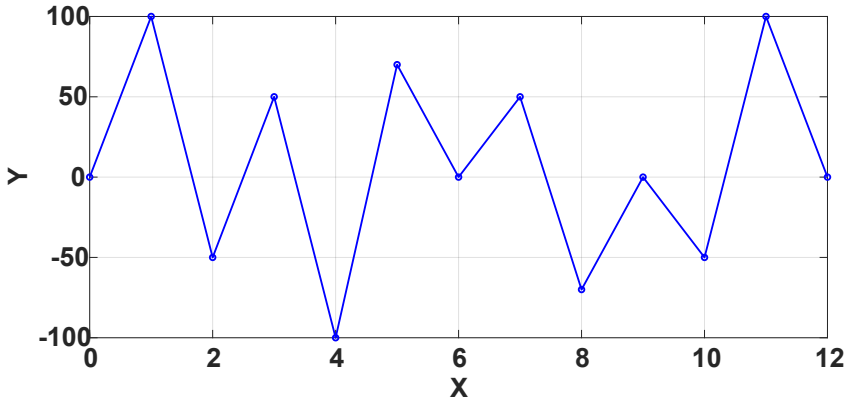


Fig. 4.20: Aperiodic Signal

Fig. 4.21: Chinese Pagoda with the rain flow [130] [131]

An example of the algorithm application on the mission profile of Fig. 4.20 is illustrated in Fig. 4.22 with the results represented in Fig. 4.23, where [132]:

- Half cycles A, B and D start at a peak and continue until a valley lower than the start value is found.

- Half cycles E and F start at a peak and terminate when they intersect with other cycles falling off from higher peaks.
- Half cycle C starts at a peak and terminates at the end of the time history for not finding a deeper valley than its starting point.

Similar half cycles are calculated for the valleys (G, H, I, J, K, L), and the half cycles with opposite sense are then matched as in Fig. 4.23. A summary of the calculation results is represented in Table 4.1.

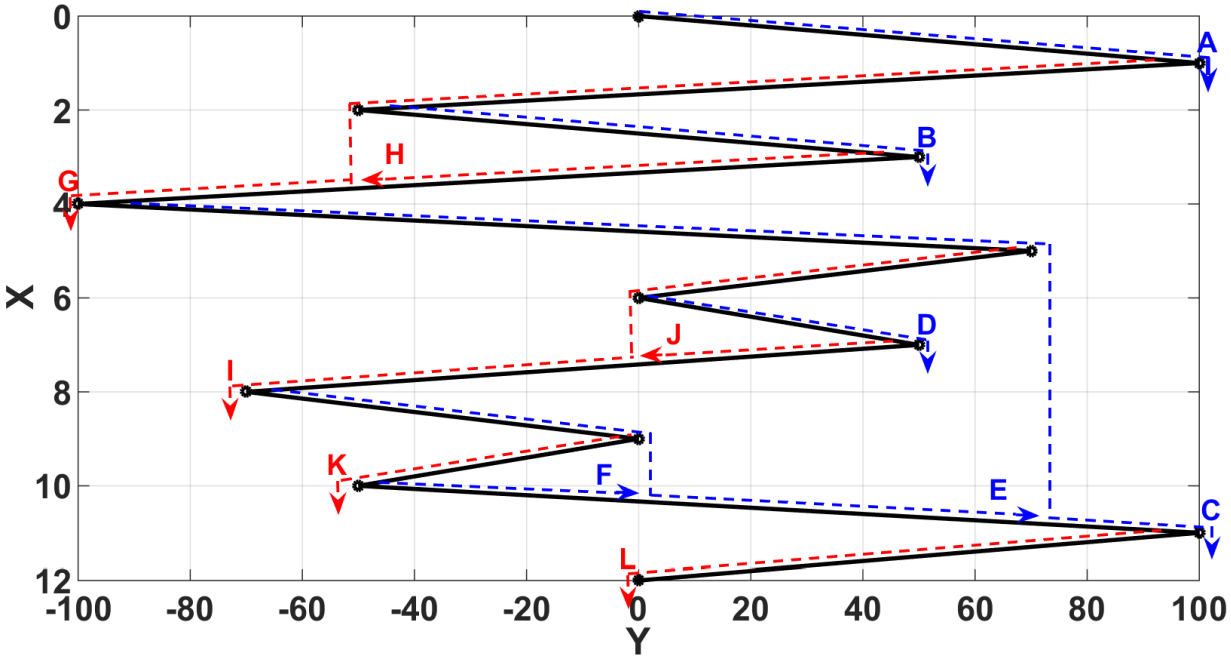


Fig. 4.22: Applying the Rainflow algorithm on the mission profile of Fig. 4.20

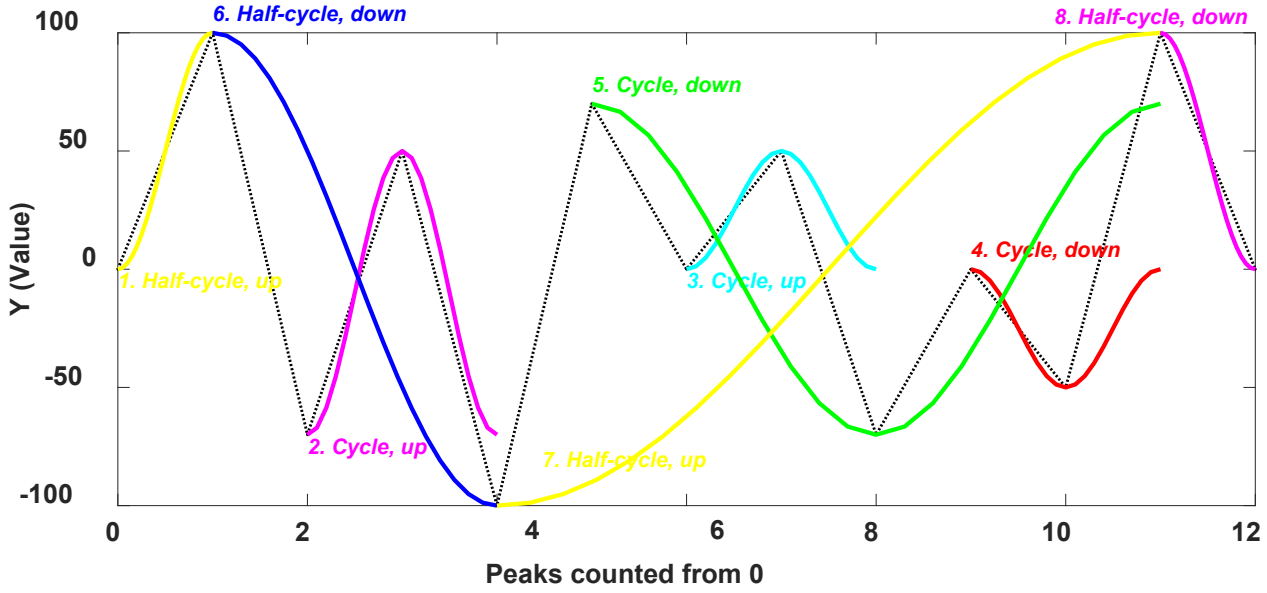


Fig. 4.23: Extracting the cycles from the mission profile

Table 4.1: Rainflow algorithm calculation results

Cycle	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*
Amplitude	*50*	*50*	*25*	*25*	*70*	*100*	*100*	*50*
Mean Value	*50*	*0*	*25*	*-25*	*0*	*0*	*0*	*50*
Number of Cycles	*0,5*	*1*	*1*	*1*	*1*	*0,5*	*0,5*	*0,5*
Occurrence Time	*0*	*2*	*6*	*9*	*5*	*1*	*4*	*11*
Period	*2*	*2*	*2*	*2*	*6*	*6*	*14*	*2*

In this study, the Rainflow algorithm is applied on the mean junction temperature profiles calculated over $T_{out} = 20$ ms. The output of the algorithm is the number of occurrences N of each value of the cycles' amplitude (ΔT_J), at a given level of average junction temperature of the cycles (T_{J_M}) (refer to Fig. 4.15), represented in the form of matrixes, tables or histograms ($N = f(T_{J_M}, \Delta T_J)$).

In this study, the Rainflow algorithm is just used to extract the cycles from the junction temperature profiles. Indeed, it was found to be insufficient to analyze the current mission profiles because of two main drawbacks:

1) Although that Rainflow algorithm can determine the period of the cycles, however for very long mission profiles, only the turning points are kept in order to accelerate the algorithm's execution time. Accordingly, most of the samples are eliminated, thus the cycles period calculated by the algorithm are shorter than the reality.

2) The sequence of cycles is not considered in Rainflow algorithm.

Because of these drawbacks, the current profiles were analyzed as represented in Section 4.2.1, without simply using Rainflow algorithm.

4.3.2. Comparison between different methods

4.3.2.1. ΔT_J and T_{J_M} distributions

The Rainflow algorithm is applied to the junction temperature profiles, corresponding to the real application current profile over one year, as well as to T_J profiles, corresponding to the different ageing methods. Accordingly, Fig. 4.24 illustrates the obtained histograms of the percentage of the junction temperature cycles number, represented as a function of the average junction temperature swings (*% Number of cycles = f* (ΔT_J)). Similarly, Fig. 4.25 illustrates the histograms of the percentage of the junction temperature cycles number, represented as a function of the average junction temperature value (*% Number of cycles = f* (T_{J_M})). As previously mentioned, the 2nd method's ageing profile has the same number of current's variations as that of the real application mission profile. However, the number of cycles in Fig. 4.24 and Fig. 4.25 is represented in percentage, since that the total number of

the measured profile's cycles over one year (~2000 cycles) is much higher than that of the 1st method ageing profile (~150 cycles).

It is noticeable that the 1st method represents the application better than classical power cycling, which leads in this example to single values of $T_{J_M} = 90°C$ and $\Delta T_J = 80K$, for constant ΔI, $T_{on} = 15s$ and $T_{off} = 15s$. These power cycling test parameters' values are selected arbitrary, and may have any other values in other power cycling examples. Despite that the 1st method generates close values of T_{J_M} to those of the real application, however the distributions of ΔT_J are still different. Actually, by inducing maximum current variations, the 1st method increases the number of high ΔT_J while decreases the number of low ΔT_J, whereas the 2nd method shows almost similar distributions to those of the real application.

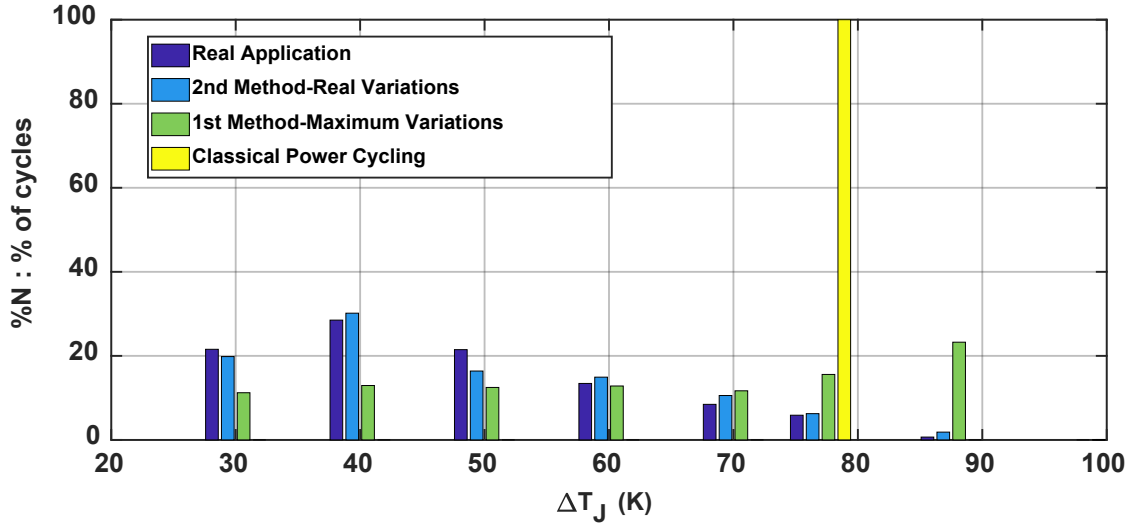


Fig. 4.24: **Histograms of the percentage of the junction temperature cycles number, represented as a function of the average junction temperature swings**
$$\%\boldsymbol{Number\ of\ cycles} = \boldsymbol{f}(\Delta \boldsymbol{T_J})$$

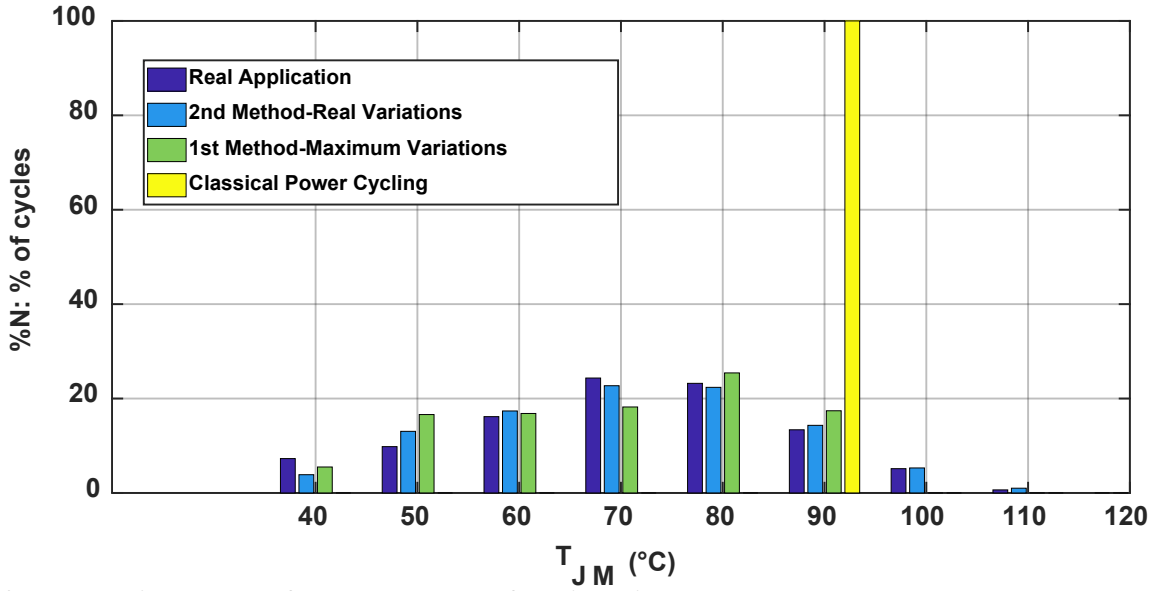


Fig. 4.25: **Histograms of the percentage of the junction temperature cycles number, represented as a function of the average junction temperature value**
$$\%\boldsymbol{Number\ of\ cycles} = \boldsymbol{f}(\boldsymbol{T_{J_M}})$$

4.3.2.2. Tests duration and acceleration factors

Once ΔT_J and T_{J_M} histograms are established, it is important to verify that the application of a new ageing method will not last for a long time comparing to classical power cycling. Assuming that the semiconductors fatigue caused by the variation of the junction temperature is linear, it is then possible to use the Palmgren-Miner rule expressed by Eq. 4.4 and Eq. 4.5 [127] [132] [133] [134]:

$$D_{i,j} = \frac{n_{i,j}}{N_{f_{i,j}}} \tag{4.4}$$

where $D_{i,j}$ is the damage caused by the cycle $C_{i,j}$, having a mean junction temperature $T_{J_M} = T_{J_{M_j}}$ and an amplitude $\Delta T_J = \Delta T_{J_i}$. $n_{i,j}$ is the number of cycles $C_{i,j}$ whereas $N_{f_{i,j}}$ is the number of cycles $C_{i,j}$ to failure. The cumulative damage D or the Life Consumption (LC) can be calculated as follows:

$$D = \sum_{i=1,j=1}^{i=j=N} D_{i,j} = \sum_{i=1,j=1}^{i=j=N} \frac{n_{i,j}}{N_{f_{i,j}}} \tag{4.5}$$

The failure of the semiconductors occurs when the cumulative damage $D = 1$. The power module used in this study does not have a specific lifetime model, hence a lifetime estimation model from the literature is employed. In fact, the literature presents several lifetime models [135] [136], however a model represented in [38] [137] is used, since it takes into account a high number of parameters as demonstrated in Eq. 4.6. Moreover, the manufacturer of *SKM200GB12E4* (the IGBT power module that will be used during the accelerated ageing tests) recommended the employment of this model to estimate the *SKM200GB12E4*'s lifetime. In this model, $N_{f_{i,j}}$ can be expressed as follows:

$$N_f = A.\Delta T_J^{\beta 1}.exp\left(\frac{\beta 2}{T_{J_{min}}+273}\right).T_{on}^{\beta 3}.I_B^{\beta 4}.V_C^{\beta 5}.D_w^{\beta 6} \tag{4.6}$$

where N_f is the number of cycles before failure illustrated in Fig. 4.26, ΔT_J the amplitude of a junction temperature cycle, $T_{J_{min}}$ the cycle's minimal value, V_C the blocking voltage rating of the chip, D_w the diameter of the wire bonding, I_B the current per wire and T_{on} the pulse duration. $A, \beta 1, \beta 2, \beta 3, \beta 4, \beta 5$ and $\beta 6$ are all fitting parameters. Accordingly, Table 4.2 represents the accelerated ageing tests' estimated duration, resulting from the application of this lifetime model on the histograms of the different methods. However, in this study the ageing test is performed by switching the semiconductors as in the real application, with $T_{on} = T_{off} = 30\ s$, while the current varies with a slope of $15\%\ I_{MAX}$. Thus, the recommended conditions for using this model are not totally respected. Accordingly, by considering these differences, the results obtained with this lifetime estimation model should be used only to get an approximate estimation of the test duration.

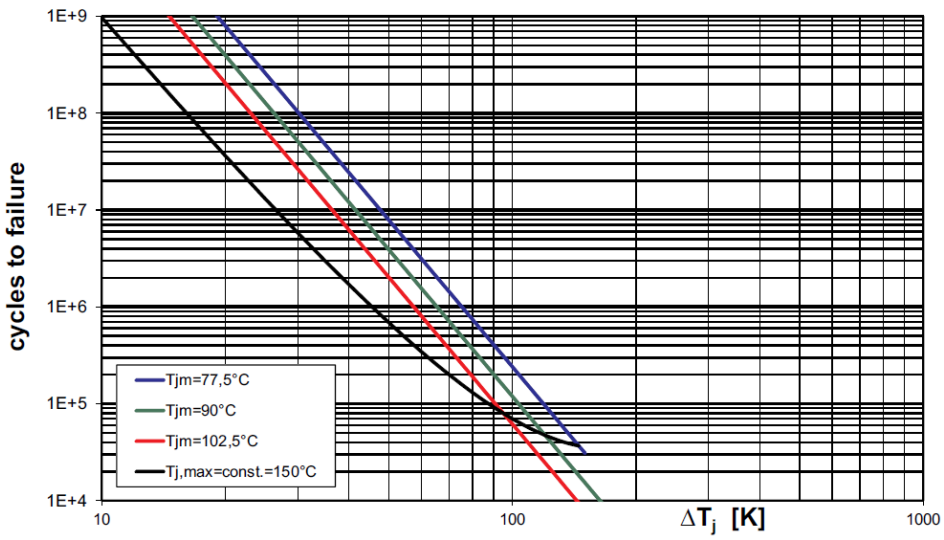


Fig. 4.26: **Dependency of the power cycling value N_f as a function of the temperature cycling amplitude ΔT_J and for different mean temperatures T_{J_M} [38]**

Table 4.2: Comparison of the different tests estimated durations

	Real application	***Classical Power cycling***	***1st method-Maximum variations***	***2nd method-Real variations***
Test duration (Days)	*4320 (~12 years)*	*40.9 (~1.5 months)*	*73 (~2.5 months)*	*153.5 (~5 months)*

It is noticeable from Table 4.2 that the classical power cycling applying relatively high $\Delta T_J = 80K$ at $T_{J_M} = 90°C$ is the fastest among the presented ageing tests, while the 2nd method is the slowest. However, this latter showed the best representation of the photovoltaic application. Nevertheless, the 1st method represents a compromise between the speed and the good representation of the application, hence it will be applied in the first place during the ageing tests depicted in the next chapters.

4.4. Design of the ageing tests profiles

In order to apply the selected method, the ageing profile should be customized for each ageing test, using the power losses estimation model and the thermal model from Chapter 2 and Chapter 3 respectively. These two models allow determining the maximum junction temperature for each semiconductor, where the profile is designed in respect to the hottest semiconductor.

4.4.1. Case of IGBT power modules

In the case of IGBT power modules, it is decided that the ageing profile raises the junction temperature (over a fundamental period corresponding to $f_{out} = 50\,Hz$) of the hottest power module to $T_{Jmax} = 150\,°C$. The case study is summarized in Table 4.3 where I_{Cr} is the rated current, $T_{J_{MAX}}$ the maximum junction temperature of the power modules, f_{out}

the fundamental frequency, f_{sw} the switching frequency, E the DC-link voltage, m the modulation factor and $cos\varphi$ the power factor.

Table 4.3: Summary of the case study for the IGBT ageing test

Power Module	*Type*	I_{C_r}	$T_{J\,MAX}$	*Inverter Topology*	f_{out}	f_{sw}	E	m	$cos\varphi$
SKM200GB12E4	*Phase-Leg Si IGBT*	*200 A*	*175°C*	*Two-level Single-Phase Inverter*	*50 Hz*	*4 KHz*	*750 V*	*0.87*	*1*

The resulting accelerated ageing profile is represented in Fig. 4.27 where the maximum current and junction temperature are $I_{MAX} = 143\ A$ and $T_{J\,max} = 150°C$, while the ambient temperature T_a alternates between $T_{a_{min}} = 15°C$ and $T_{a_{max}} = 35°C$. The DC/AC inverter topology is represented in Fig. 4.28, while the corresponding junction temperature profiles of each semiconductor obtained by applying the thermal model on the ageing profile are represented in Fig. 4.29 with a highlight in Fig. 4.30. It can be noticed that diode D_4 has the lowest T_J while IGBT D_7 has the highest one with $T_{J_{max}} = 150°C$.

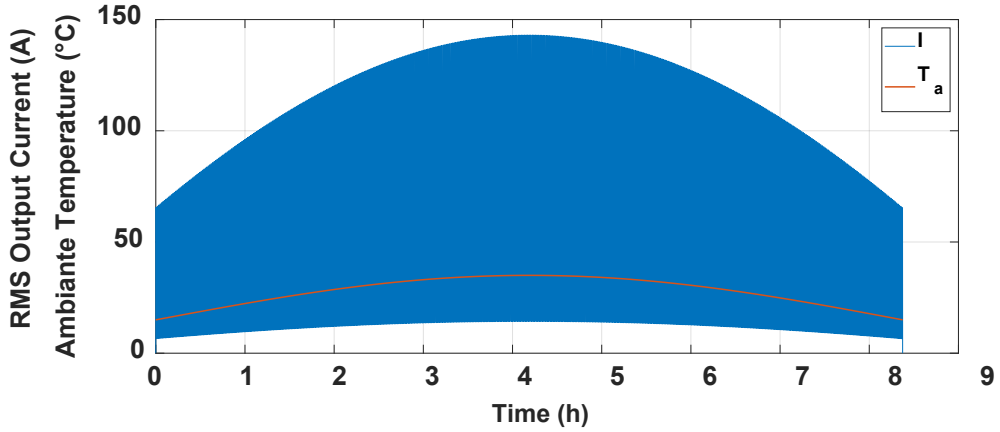


Fig. 4.27: Resulting accelerated ageing current's profile designed for the IGBT aging test

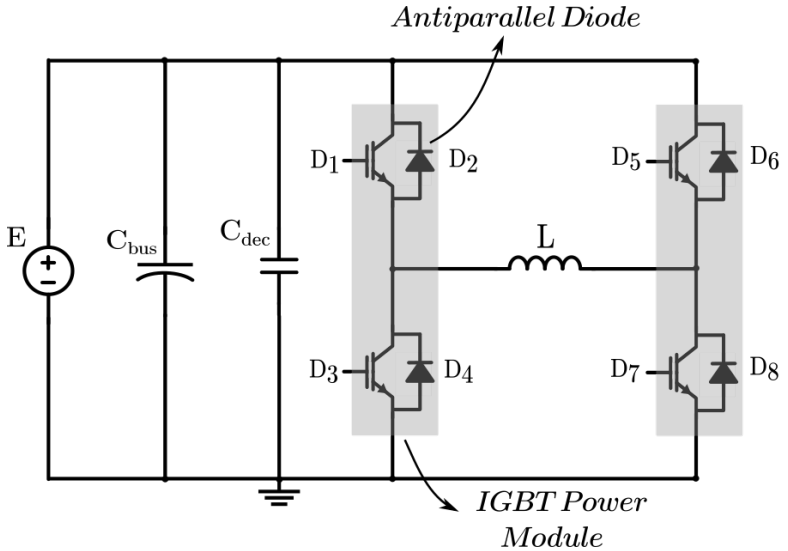


Fig. 4.28: Two-level single-phase DC/AC inverter

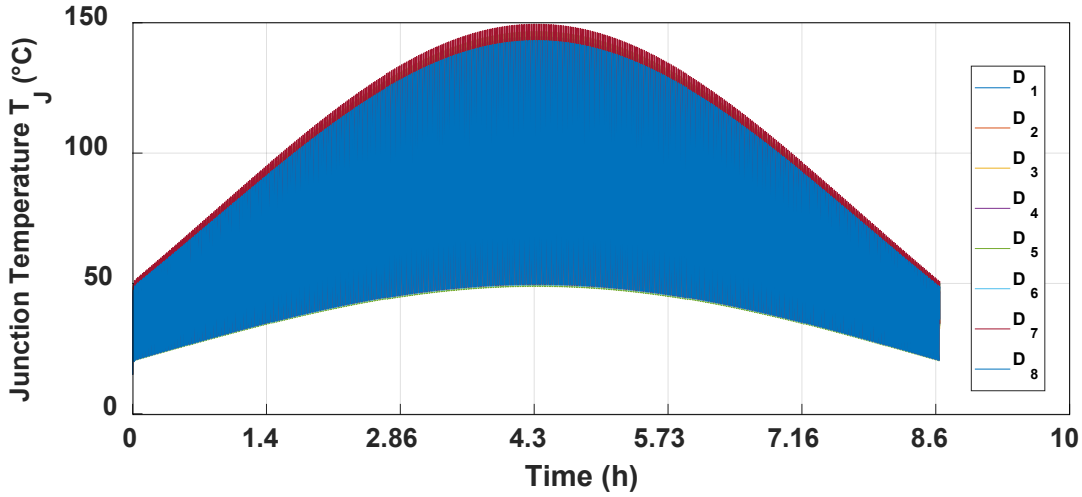


Fig. 4.29: Resulting junction temperature's profile for the IGBT ageing test

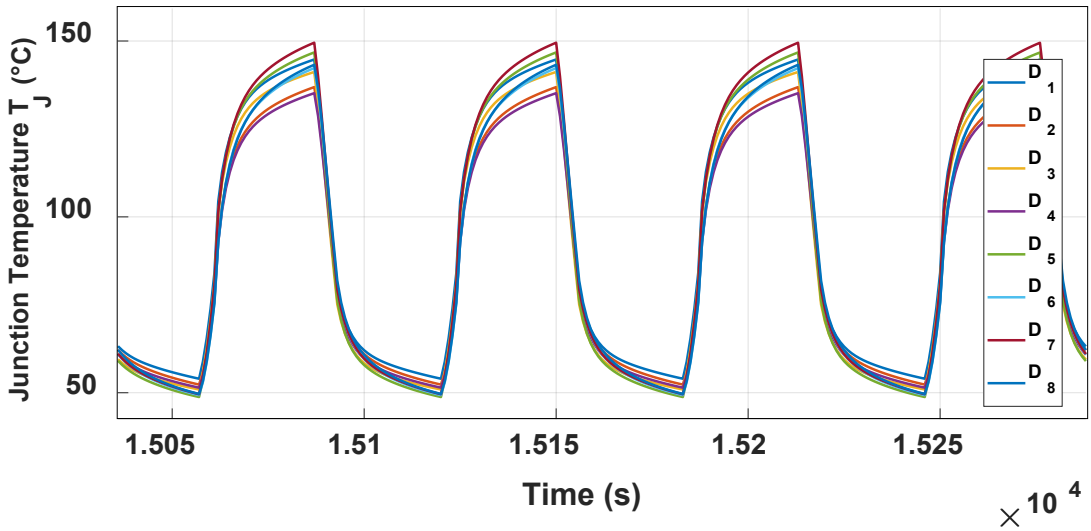


Fig. 4.30: Highlight on Fig. 4.29 where IGBT D_7 has highest $T_{J_{max}}$

By applying the lifetime estimation model demonstrated above on the T_J profile of the hottest semiconductor device D_7 represented in Fig. 4.30, the cumulative damage D equals 1 after 40 estimated days of accelerated ageing. It should be noted here that this lifetime estimation model was built by applying classical power cycling campaigns without switching, with $T_{on} = T_{off} \leq 15\ s$ and instantaneous variations of the current. However, as mentioned previously in this study, the test is performed by switching the semiconductors as in the real application, with $T_{on} = T_{off} = 30\ s$, while the current variations' slope fixed at $0.015 \cdot I_{MAX}\ (\frac{A}{s})$. Taking all of these differences into consideration, the results obtained with this lifetime estimation model should be only used to have an approximate estimation of the test duration.

4.4.2. Case of SiC MOSFET power modules

The case study for the MOSFET ageing test is summarized in Table 4.4. The same procedure is applied for the MOSFET power modules, with $I_{MAX} = 90A$ while T_a alternates between $T_{a_{min}} = 10°C$ and $T_{a_{max}} = 40°C$. It does not exist in the literature a specific lifetime estimation model for the MOSFET module *APTMC120AM16D3AG* (rated current $I_{D_r} = 136\ A$ at $T_C = 25°C$). However, a model obtained with thermal cycling performed on similar modules from the same manufacturer can be useful to approximately estimate the test duration. The lifetime estimation model is not to be represented here for confidentiality issues, however using this model, the obtained cumulative damage D equals 1 after one month and a half of accelerated ageing.

Table 4.4: Summary of the case study for the MOSFET ageing test

Power Module	***Type***	I_{D_r}	$T_{J_{MAX}}$	***Inverter Topology***	f_{out}	f_{sw}	***E***	***m***	$cos\varphi$
APTMC120AM16D3AG	*Phase-Leg SiC MOSFET*	*136 A Tc= 25°C*	*150°C*	*Two-level Single-Phase Inverter*	*50 Hz*	*10 KHz*	*750 V*	*0.8709*	*1*

4.5. Conclusions

This chapter demonstrated a new method for the accelerated ageing of photovoltaic inverters, created by analyzing the mission profiles of the current and ambient temperature, extracted over several years from different photovoltaic power plants. Many characteristics of the photovoltaic application were studied like the shape of the RMS output current of the inverter, the diffuse current, the slope of the current variations, the difference between the seasons, the delays between the current variations and the ambient temperature.

A 1st accelerated ageing method was represented, considering all the characteristics mentioned above and generating maximum current variations. Subsequently, a 2nd accelerated ageing method was illustrated taking into account the same characteristics, but regenerating the real current variations extracted from the measured mission profiles. The corresponding ageing profile of each method was designed and refined successively, using the power losses estimation model from Chapter 2, and the thermal model from Chapter 3 to estimate the corresponding junction temperature profiles. A cycle counting algorithm named Rainflow was used to extract the cycles from the junction temperature profiles, as well as the corresponding T_{J_M} and ΔT_J of each extracted cycle. Then, the ageing profiles were refined according to the desired T_{J_M} and ΔT_J's distributions. Afterwards, a comparison between the real application, a classical power cycling and the two accelerated ageing methods was performed, considering the distributions of T_{J_M} and ΔT_J.

It was noticeable that the 1st method represented the application better than the classical power cycling, which leads to a single value of T_{J_M} and ΔT_J. However, despite that the 1st method generated close values of T_{J_M}, the distributions of ΔT_J were yet different, while the 2nd method showed almost similar distributions, compared to the real application.

Next, a second comparison was performed concerning the tests duration, by applying Palmgren-Miner rule and using a lifetime estimation model. Consequently, classical power cycling was found to be the fastest among the methods, then the 1st ageing method and lastly the 2nd one. However, the 1st method showed a compromise between the speed and the good representation of the application, hence, it was selected to be applied in the first place during the accelerated ageing test. Eventually, the profiles for the IGBT and MOSFET ageing tests were designed using the selected method.

Although being slower than classical power cycling, these methods are expected to show more representative results, and thus reducing the favoring of certain failure modes to the detriment of others. Moreover, these methods can be used to reveal the weak points of the power modules used in photovoltaic inverters, and thus lead to improve the fabrication processes in the future.

Chapter 5:
SiC MOSFET's accelerated ageing tests

Chapter 5: SiC MOSFET's accelerated ageing tests

5.1. Introduction

Already presented in Chapter 4, the accelerated ageing current's profile for SiC MOSFET should be now applied in real accelerated ageing tests (refer to Fig. 1.36). As previously mentioned, in this type of tests passive and active cycling are simultaneously applied under switching nominal conditions and pulse width modulation (PWM) operating mode using the opposition method.

The main purpose of this study is to apply the proposed ageing method in a real test bench, in order to check its feasibility, duration and complexity, as well as to find potential indicators of failure corresponding to this type of tests. Thus, being new, the accelerated ageing tests presented in this chapter are applied for a preliminary check, and therefore the failure mechanisms analysis will not be discussed in details in this study.

Initially, the tests' methodology will be described, where the accelerated ageing tests as well as the failure indicators selection and measurement will be depicted.

Afterwards, this chapter will demonstrate the different steps for designing the 52 kW two-level DC/AC single-phase inverter (Fig. 5.1), which will be used during the accelerated ageing tests. Hence, the choice of the power stack and the current transducers, the design of the pre-drivers and the load inductor, as well as the temperature regulation and the control systems will be all detailed in the following sections.

Lastly, preliminary results of accelerated ageing tests will be represented and discussed in order to determine the potential indicators of ageing/failure of SiC MOSFET power modules used in DC/AC photovoltaic inverters.

5.2. Tests' methodology

5.2.1. Accelerated ageing tests

The proposed tests apply active and passive cycling simultaneously under switching nominal conditions and PWM operating mode. The devices are fed with a regulated sinusoidal current with an adjustable frequency in a back-to-back configuration using the opposition method, as illustrated in Fig. 5.1 [53] [92]. It is the electrical circuit of a two-level DC/AC single-phase inverter with a pure inductive load. In this type of tests the operating conditions are similar to those existing in a drive inverter, where the semiconductor devices are switching under the DC bus voltage. Moreover, the opposition method presents a great advantage since the input power is only required to supply the devices' losses, which represent less than 5% of the inverter's total power [36] [51] [54]. Some studies can be found in the literature on power cycling under PWM operating mode [51] [55].

The originality in this study is the application of accelerated ageing profiles of current and temperature representative of the PV application, as demonstrated in Chapter 4. The current's profile sets the inverter's RMS output current while the temperature profile controls

the heat sink temperature. The parameters of both profiles were already selected and are represented in Section 4.4.2.

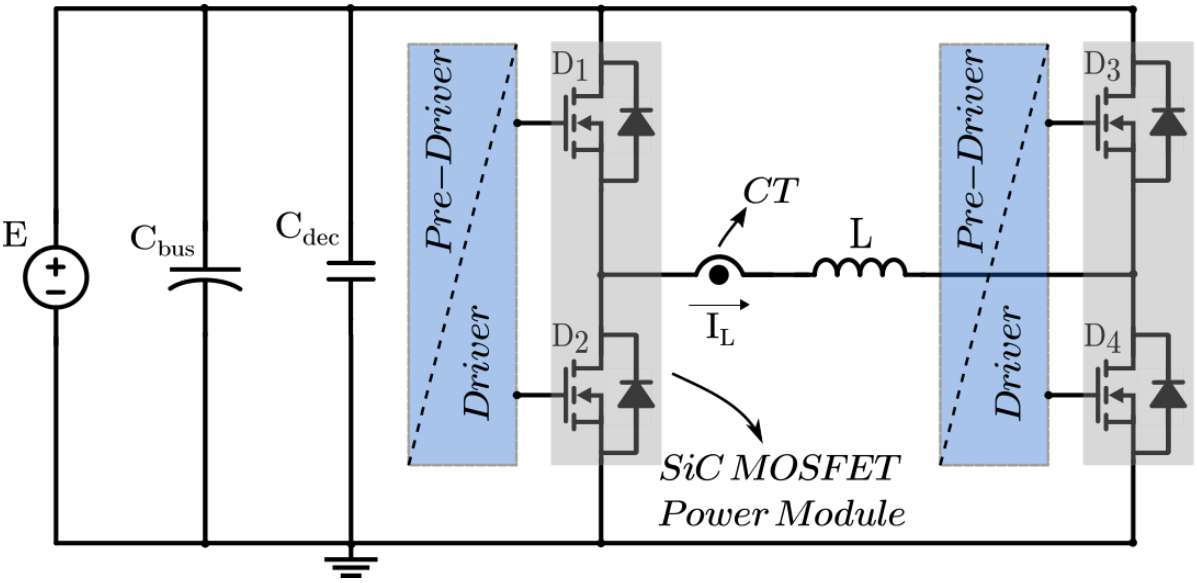


Fig. 5.1: Equivalent electrical circuit of back-to-back configuration

5.2.2. Failure indicators measurement

5.2.2.1. Selection of failure indicators

According to literature (Chapter1 Section 1.4), several failure indicators can be used to monitor the condition of the SiC MOSFET devices in APC and PTC tests, mainly the drain-source on-state voltage $V_{DS_{on}}$ or resistance $R_{DS_{on}}$ as well as the thermal impedance Z_{th}. An increase in $R_{DS_{on}}$ under given current and temperature is considered as indicator of the power module ageing, indicating bond wire lift off and/or heel crack, a reconstruction of the metallization surface or a decrease in device's thermal performances. The relative variations due to bond wires damage are very low since the low voltage across the connections constitutes a small percentage of the total on-state voltage. Therefore, this measurement must be made with a very high degree of accuracy [12] [45] [62]. Usually, in order to determine $R_{DS_{on}}$ the APC test has to be stopped, then a high current is injected in the device, while the exact drain current I_D that is injected through the device and the drain-source voltage V_{DS} are measured.

Another commonly used failure indicator in APC tests is the thermal resistance R_{th}. An increase of about 20% in R_{th}/Z_{th} is considered as an indicator of the soldering and/or substrate fatigue.

Less commonly used failure indicators in APC tests are drain leakage current I_{DS_S}, gate leakage current I_{GS_S} and gate threshold voltage $V_{GS_{th}}$. This latter is considered as an indicator of gate oxide based failures, due to interfacial charge trapped at and near the $SiC-SiO_2$ inversion channel-gate insulator interface [28].

Leakage current is a quantum phenomenon where electrons tunnel through an insulating region. Actually, semiconductors may conduct a small amount of current even when they are turned off, referred to as leakage current. Increased leakage current is a common failure mode resulting from non-catastrophic overstress of a semiconductor device,

when the gate oxide or the junction suffer permanent damage not sufficient to cause a catastrophic failure [12].

Furthermore, there are several parameters that are not commonly monitored during APC tests, such as the MOSFET's body diode forward voltage V_{SD}, the internal gate resistance R_G, the input capacitance $C_{i_{ss}}$, the output capacitance $C_{o_{ss}}$ and the reverse transfer capacitance $C_{r_{ss}}$. These parasitic capacitances are given by $C_{r_{ss}} = C_{GD}$, $C_{i_{ss}} = C_{GD} + C_{GS}$ and $C_{o_{ss}} = C_{GD} + C_{DS}$, where C_{GD}, C_{GS} and C_{DS} represent the gate-drain, gate-source and drain-source parasitic capacitances respectively.

The aim of this study is to monitor the maximum number of electrical parameters, in order to determine potential ageing/failure indicators of SiC MOSFET power modules used in DC/AC PV inverters. Accordingly, the selected electrical parameters to be monitored are: the gate leakage currents I_{GS_S} and $I_{GS_{S(-)}}$, the drain-source on-state resistance $R_{DS_{on}}$, the gate-source threshold voltage $V_{GS_{th}}$, the drain leakage current I_{DS_S}, the body diode forward voltage V_{SD}, the internal gate resistance R_G, the input capacitance $C_{i_{ss}}$, the output capacitance $C_{o_{ss}}$ and the reverse transfer capacitance $C_{r_{ss}}$.

Unfortunately, the thermal impedance will not be monitored in this study. Indeed, the most commonly used method for measuring Z_{th} is by calculating it from the active part temperatures that are estimated conventionally, by injecting a constant current in each semiconductor device, provided by an external current source. The calculation of the thermal impedance is often carried out during the cooling phase, after switching off the current source. If a power module with closed package is under test, the easiest way to measure T_J is via the measurement of TSEP, such as the forward voltage of the MOSFET's intrinsic body diode. This method is depicted in Chapter 3.

Nevertheless, this method widely presented in the literature is time consuming and requires a total disconnection of the characterized semiconductor device from the rest of the inverter. Thus, the monitoring of Z_{th} in APC tests with PWM mode is still complicated. However, other methods are found in the state of art, where the measurement of Si IGBTs' junction temperature is done without disconnecting the power modules, yet that requires a more instrumented test bench [67]. Actually, a new in-situ method for measuring Z_{th} is developed and applied in IGBT's tests as it will be represented in Chapter 6. However, due to time constraints, this method could not be used for the SiC MOSFET's tests for the moment, but it will be implemented in the future.

5.2.2.2. Measurement methodology

In the case of healthy semiconductor devices, the drain and gate leakage currents are very low (in the range of nA). Thus, given that the monitoring of these indicators requires very high precision measurement, and since that many failure indicators were selected to be monitored, the measurements were done by the *B1506A Keysight* Analyzer [138] while fixing the DUT's temperature using a Thermo Stream (Fig. 5.2). This allows for a minimum instrumentation of the test bench, while monitoring a maximum number of electrical parameters.

Accordingly, the cycling is interrupted periodically every 24 h to monitor the semiconductor devices' condition while disconnecting them totally from the inverter, then using the *B1506A* Analyzer for the measurement. Indeed, this is a complicated and time-consuming process that could be automated in the future. Table 5.1 exhibits the measurement conditions of the selected electrical parameters.

It should be noted that a carbon sheet serves as thermal interface between the cold plate and the MOSFETs, which are fixed with a constant tightening torque of 5 N.m to prevent any variation in the thermal behavior of the system while disconnecting them. The global tests' methodology is illustrated in Fig. 5.3.

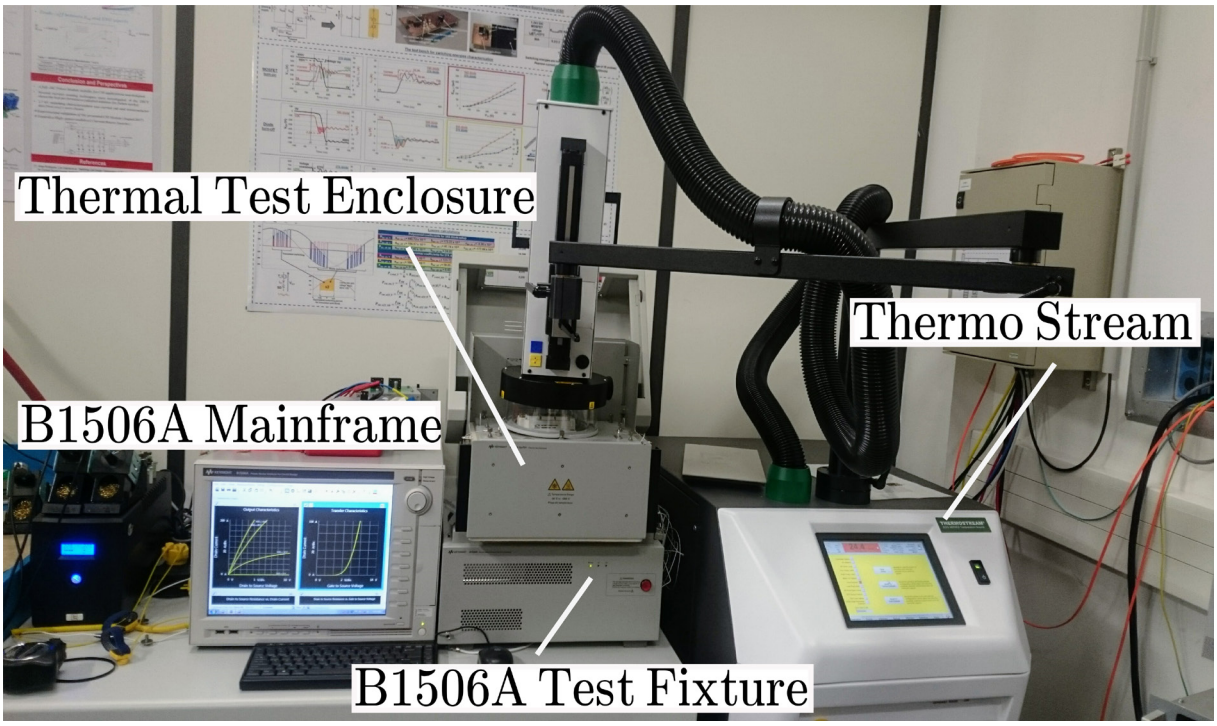


Fig. 5.2: Monitoring the electrical parameters using the *B1506A* Analyser with the Thermo Stream

Table 5.1: Measurement conditions of the selected electrical parameters

Electrical parameter	Measurement conditions
Gate leakage current I_{GSS}	$V_{DS} = 0, V_{GS} = +20\ V$
Gate leakage current $I_{GSS(-)}$	$V_{DS} = 0, V_{GS} = -5\ V$
Gate to source threshold voltage $V_{GS_{th}}$	$V_{DS} = V_{GS}, I_D = 5\ mA$
Internal gate resistance R_G	$V_{GS} = 0\ V, f = 100\ kHz$
Drain leakage current I_{DSS}	$V_{DS} = 750\ V, V_{GS} = 0\ V$
Drain-source on-state resistance $R_{DS_{on}}$	$I_D = 100\ A, V_{GS} = 20\ V$
Body diode forward voltage V_{SD}	$I_S = 50\ A, V_{GS} = -5\ V$
Input capacitance $C_{i_{ss}}$	$V_{DS} = 750\ V, V_{GS} = 0\ V, f = 100\ kHz$
Output capacitance $C_{o_{ss}}$	$V_{DS} = 750\ V, V_{GS} = 0\ V, f = 100\ kHz$
Reverse transfer capacitance $C_{r_{ss}}$	$V_{DS} = 750\ V, V_{GS} = 0\ V, f = 100\ kHz$

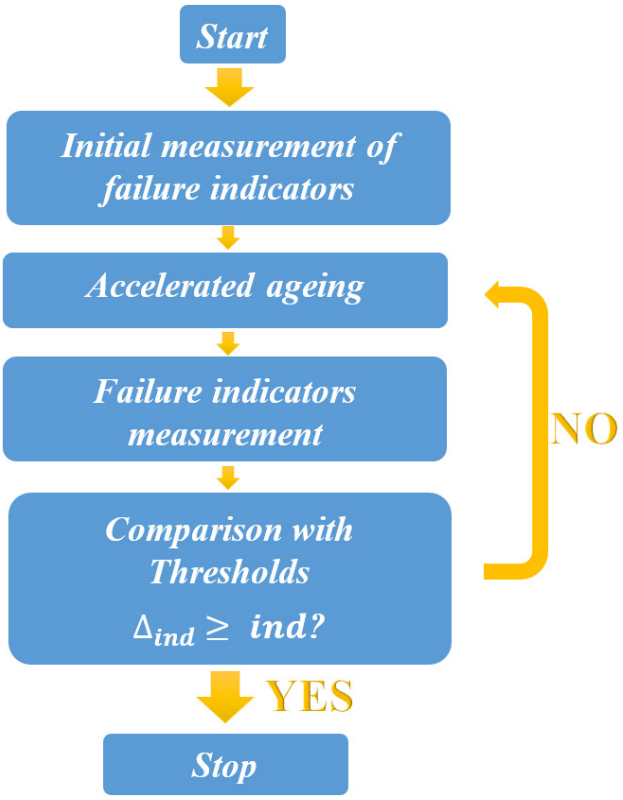


Fig. 5.3: Global tests' methodoly

5.3. Test bench

5.3.1. Power circuit

The selected device is the SiC MOSFET power module *APTMC120AM16D3AG* (1200V-136A phase-leg 62mm standard packaging power module without antiparallel diodes). The power modules are integrated in a power stack with 4x420 µF DC-link capacitors (C_{bus}) and 2x1 µF decoupling capacitors (C_{dec}), with an applied DC-link voltage E = 750V. Fig. 5.4 shows the selected MOSFET power module, while Fig. 5.5 represents the single-phase inverter. It should be noted that all self and thermal coupling mutual impedances of the inverter's system (power modules + heat sink) were already estimated as presented in Chapter 3.

Fig. 5.4: *APTMC120AM16D3AG* SiC MOSFET power module

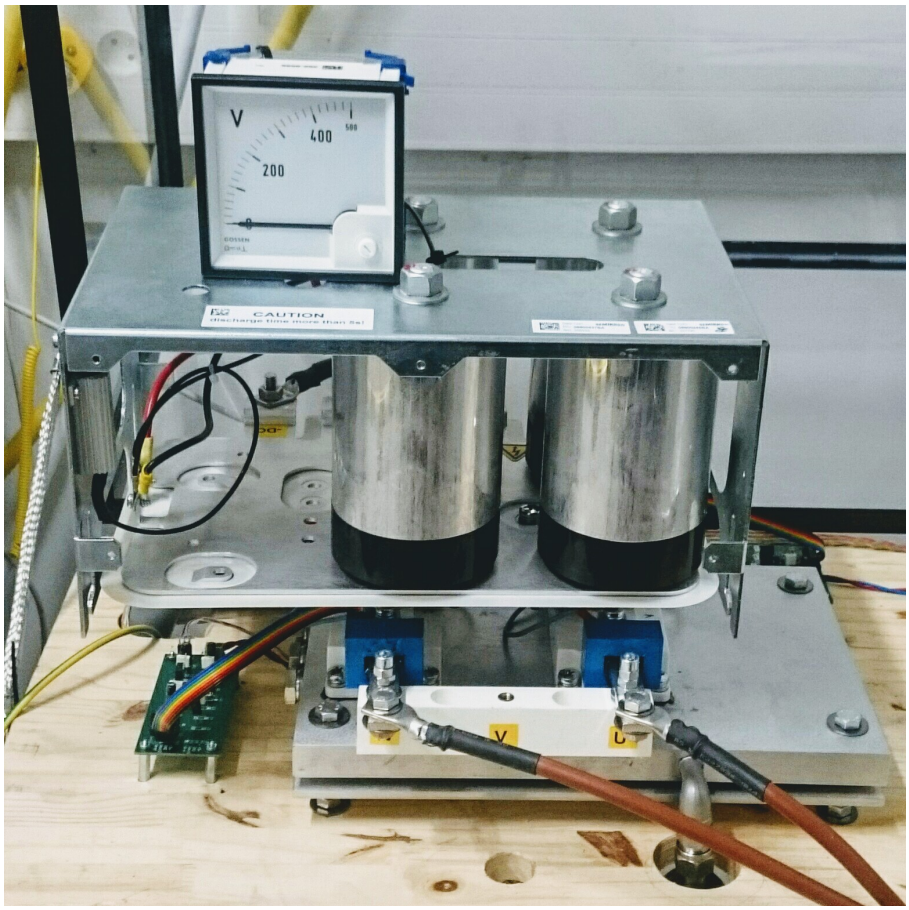


Fig. 5.5: 52 kW two-level single-phase DC/AC inverter

As previously mentioned, the opposition method used for power cycling requires the use of a relatively low DC-link power supply, comparing to the inverter power rating. Actually, in a back-to-back configuration (Fig. 5.1) the circuit consumption is equal to the inverter's power losses only. Hence, a 52 kW inverter with 97% efficiency and 3% power losses needs only a 1.56 kW power supply in back-to-back configuration. Accordingly, the DC-link voltage E = 750V is sourced by a 15 kW power supply, the *PS 9000 3U Series* 1.5 kV– 30 A, controlled by a 0-10V analog input, while 2 series connected inductors of 120 µH were designed and connected to the inverter's output (Fig. 5.6)

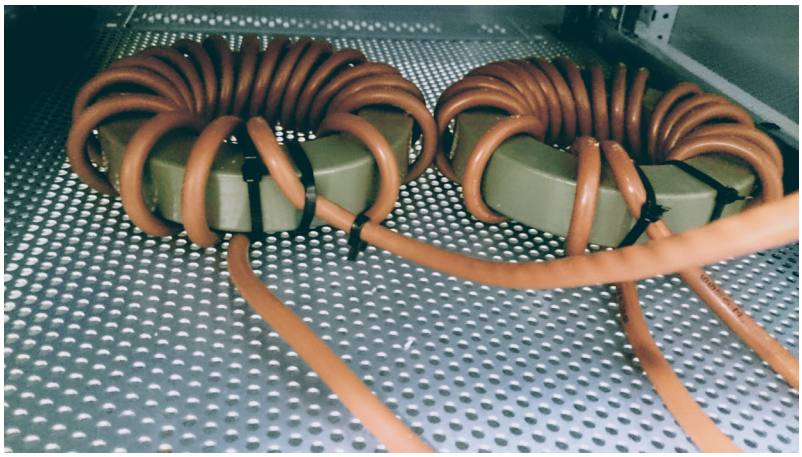


Fig. 5.6: Two series connected inductors

5.3.2. PCBs design

In order to drive the MOSFETs, the *PT62SCMD12* drivers from *Cree* were selected. They have a +20V/-6V output signal, adjustable dead-time generator and over current protection system. Two pre-driver PCBs were designed to adapt the output signals of the FPGA core of a *PXI* system (*National Instruments*) that commands the drivers, since the *PT62SCMD12* expects only differential input signals. The pre-diver circuit transforms the 0-10 V digital output signal of the FPGA core to a -10 V/+10 V analog signal, using push-pull circuits to amplify the driving signals. Moreover, the pre-driver supplies the driver with a 15 V-24 V voltage, transmits its status to the *PXI* and resets it after an over current detection. Fig. 5.7 shows one pre-driver PCB.

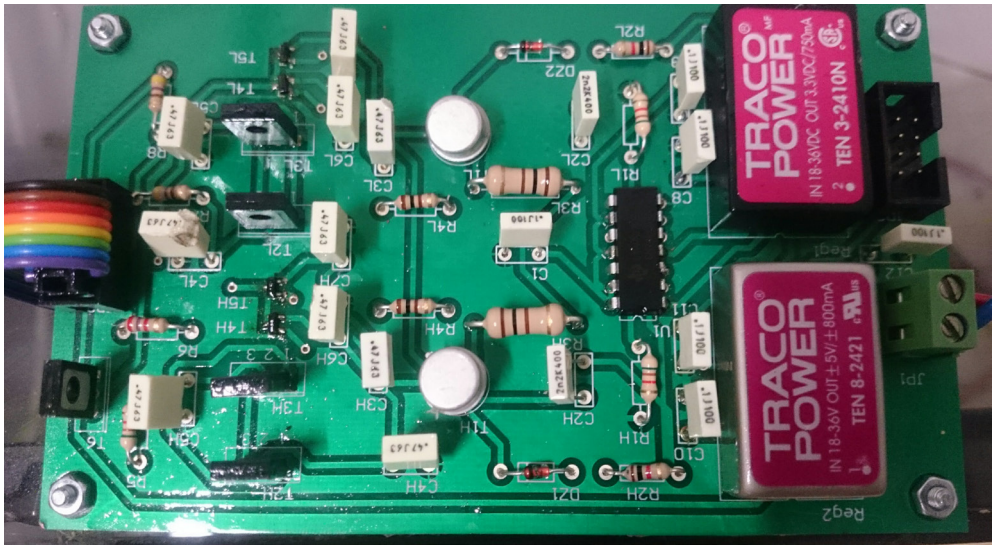


Fig. 5.7: Pre-Driver PCB

Two *LEM* current transducers *HAS 100-S* were selected with a nominal current of 100 A for the measurement and the closed loop control of the load's current I_L. The Current Transducers (CTs) are supplied by a 5 V and a 2.5 V voltages, generated by the PCB represented in Fig. 5.8 (the 2.5 V power supply serves as reference voltage). A low-pass filter is inserted between the output of the PCB and the input of the *PXI* to eliminate the high frequency noise from the current's measurements.

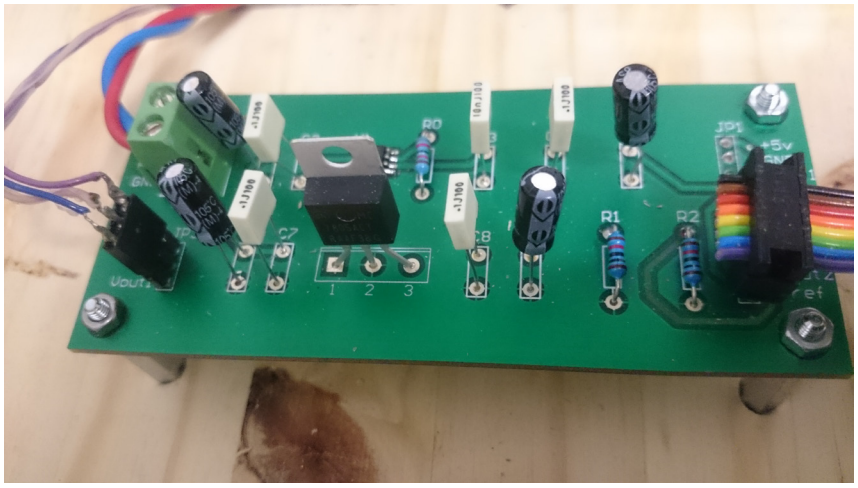


Fig. 5.8: CT's power supply PCB

5.3.3. Temperature regulation system

LH50plus system from *JULABO* represented in Fig. 5.9 is selected for the inverter's temperature regulation, having the following technical data exhibited in Table 5.2 [139]:

Table 5.2: Technical data of *LH50plus*

Technical data	Value				
Working temperature range (°C)	-50…+250				
Heating capacity (kW)	6				
Cooling capacity (Medium Ethanol)	T(°C)	200	20	-20	-40
	P(kW)	5.5	7	2.6	0.5
Pump capacity flow rate (l/min)	16-30				
Cooling of compressor	Water				
Digital interface	RS232, RS485, Profibus (optional)				

The temperature of this water-cooled heat sink is controlled by the *PXI* via a 0 V-10 V analog signal, allowing to apply during the accelerated ageing test the ambient temperature profile built in Chapter 4. The heat sink is connected to a cold plate, designed to optimize the cooling of the semiconductors' chips, by leading the thermal fluid the nearest possible to chips positions, and minimizing the thermal coupling between them. As mentioned in Chapter 3 and as represented in Fig. 5.10, the cold plate designed with *SolidWorks* is drilled under the center of the semiconductors' chips positions to allow for the insertion of thermocouples. Eventually, Fig. 5.11 represents the prototype of the inverter mounted on the cold plate.

Fig. 5.9: *LH50plus* temperature regulation system

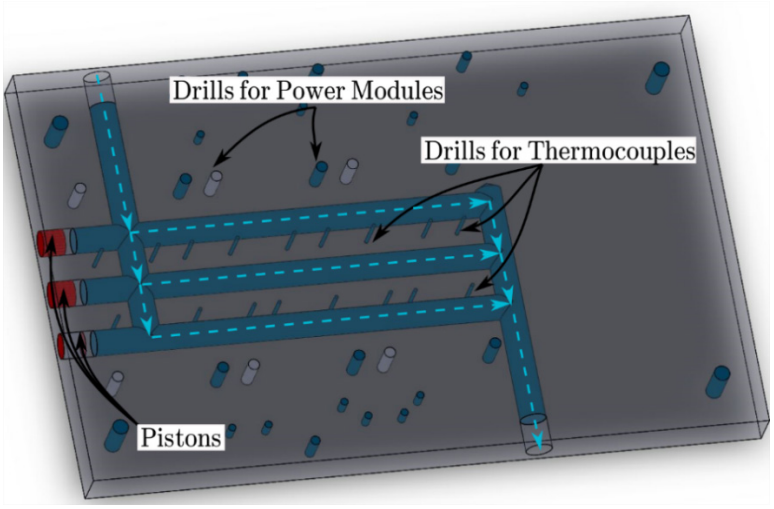


Fig. 5.10: 3D plan of the cold plate

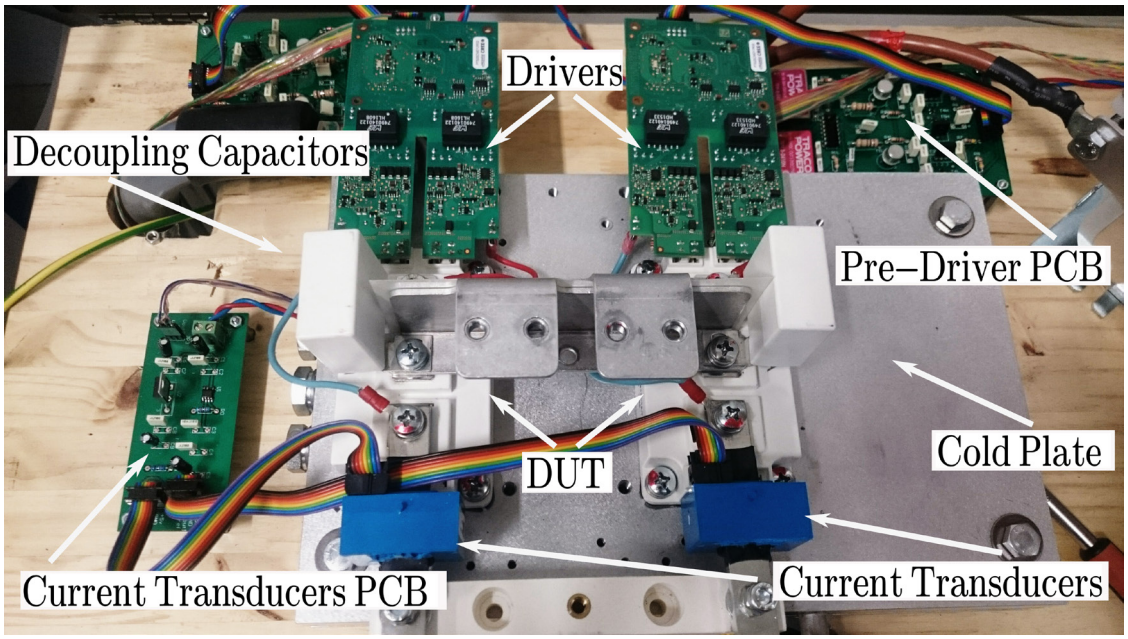


Fig. 5.11: Inverter's prototype

5.3.4. Control system

An FPGA module of a *PXI* system (*National Instruments*) controls all the test bench components via a computer HMI (Human Machine Interface) using *LabVIEW* software. *PXI* is a rugged PC-based platform for measurement and automation systems (Fig. 5.12) used to monitor the test bench. It also controls the DC-link power supply as well as the heat sink temperature. Moreover, the *PXI* applies the opposition method, so it reads the current measurement of the CT and commands the MOSFETs in real-time via the pre-drivers with a 20 MHz clock rate. The technical specifications of the used FPGA module *NI PXI-7854R* are exhibited in Table 5.3.

Fig. 5.12: *PXI* with real-time RT and *NI PXI-7854R* FPGA modules

Table 5.3: *NI PXI-7854R* module's technical specifications

Module	Maximum Sample Rate	Number of Analog Input Channels	Number of Analog Output Channels	Number of Bidirectional Channels
NI PXI-7854R	750 KS/s	8	8	96

Fig. 5.13 represents the control system's diagram, where the HMI (the computer machine) sends the mission profiles' configurations and drives the real-time RT module integrated into the *PXI*. In its turn, the RT module processes the files and transfers the commands to the FPGA module. Then, the FPGA processes the mission profiles by applying the opposition method, while reading the load's current, the drivers' status, the power supply alerts and the heat sink temperature. Finally, these data are transferred to the HMI via the RT module to monitor the accelerated ageing tests.

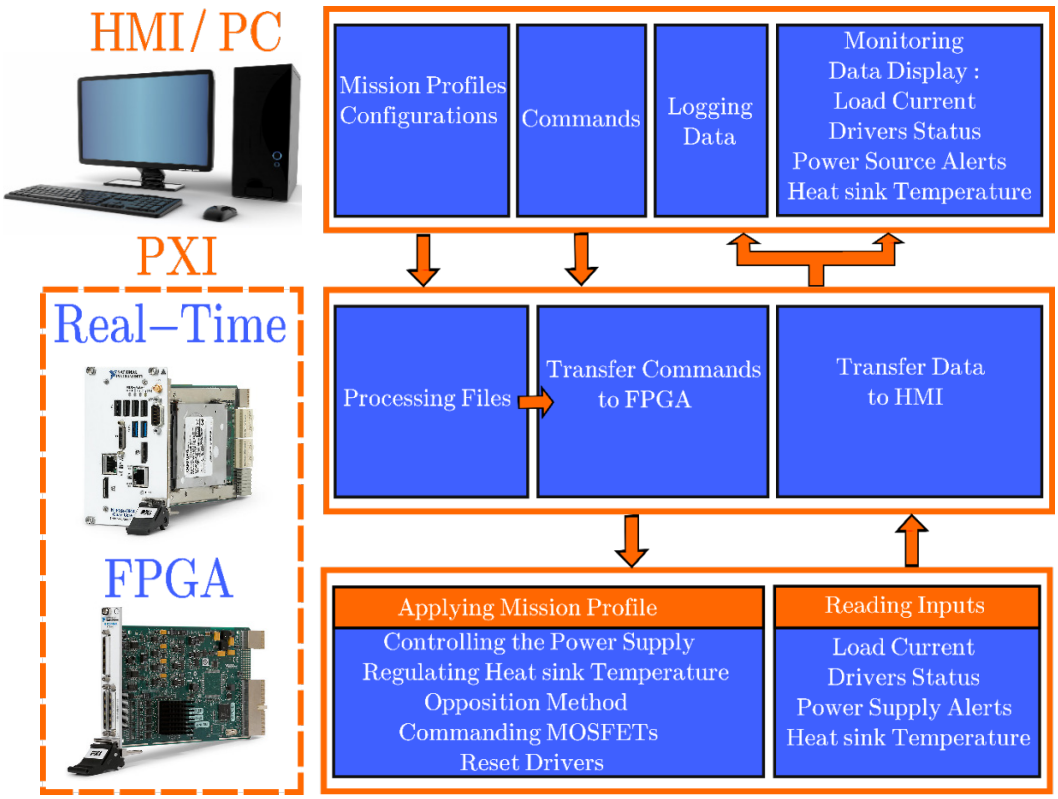


Fig. 5.13: Control system's diagram

Fig. 5.14 represents a screenshot of the HMI screen, where the played current ageing profile, the measured RMS output current, the drivers' status, the power supply alerts and the heat sink's temperature can be monitored. Finally, Fig. 5.15 represents the global accelerated ageing test bench.

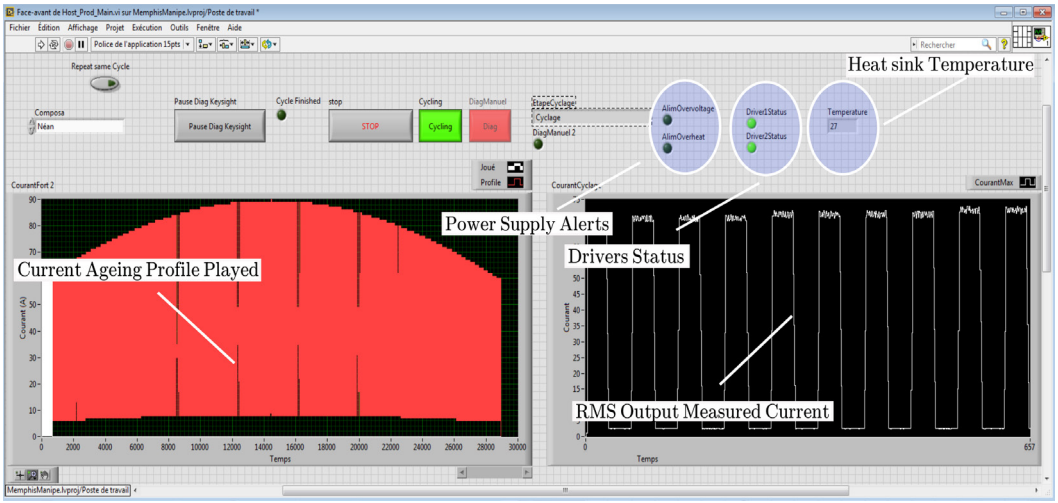


Fig. 5.14: Screenshot of the HMI screen

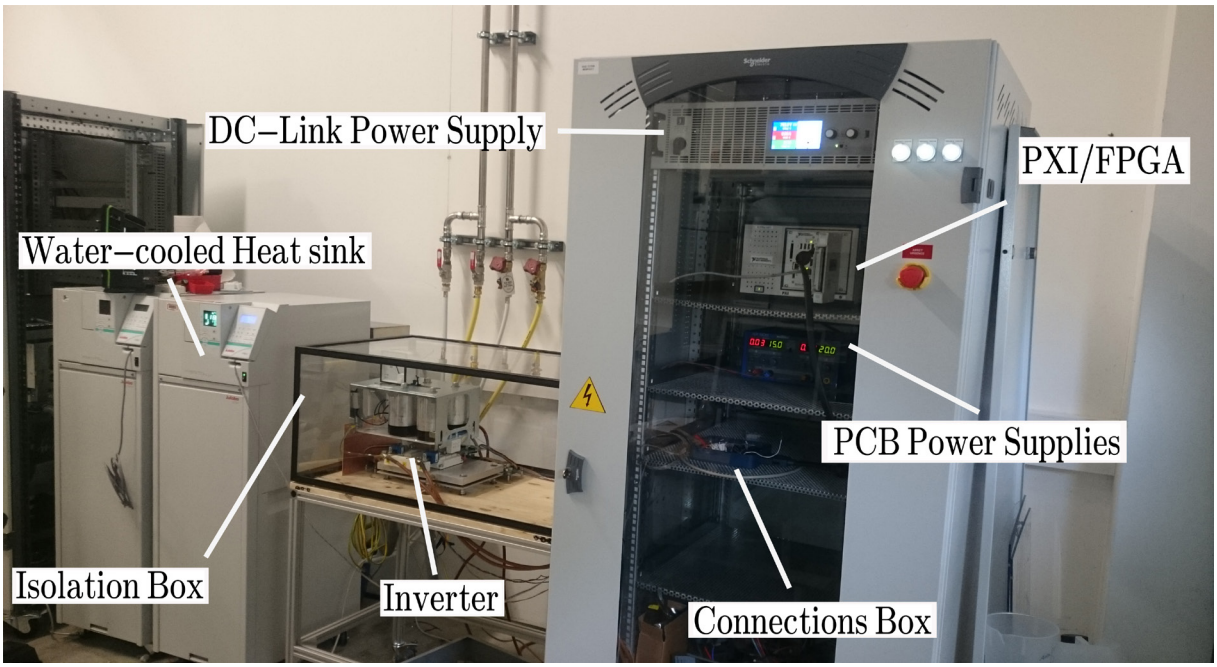
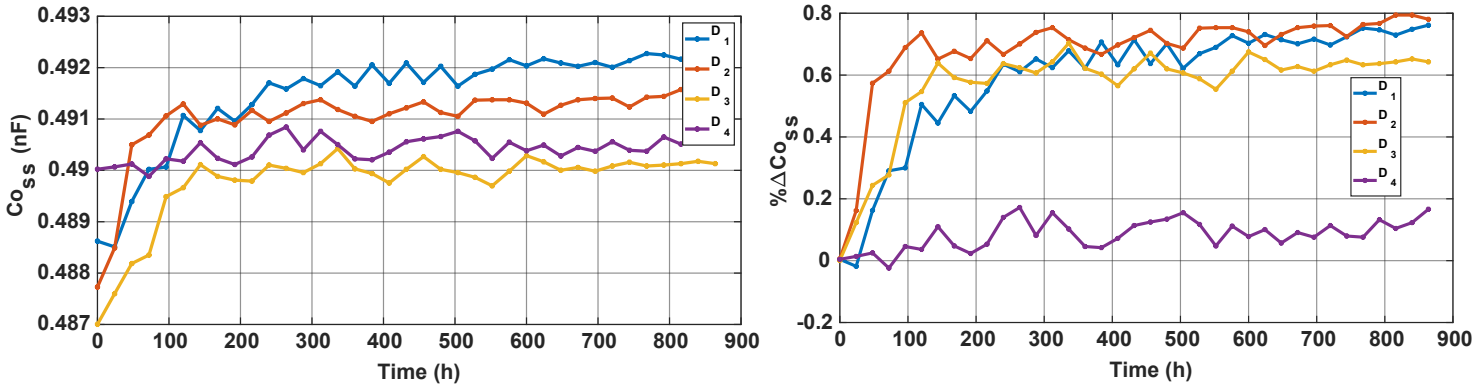


Fig. 5.15: Global test bench

5.4. Ageing tests results

The accelerated ageing tests were done with the selected SiC MOSFET power module *APTMC120AM16D3AG*, applying the accelerated profiles described in Section 4.4.2. These tests lasted for 864 h, until the gate of MOSFET D_4 became uncontrollable by the driver, and $R_{DS_{on}}$'s derivation of MOSFET D_3 exceeded the threshold value of 20%. The evolution of the monitored parameters measured at $T_J = 25°C$ is represented in the following figures with both absolute values and variations in percentage as a function of time.

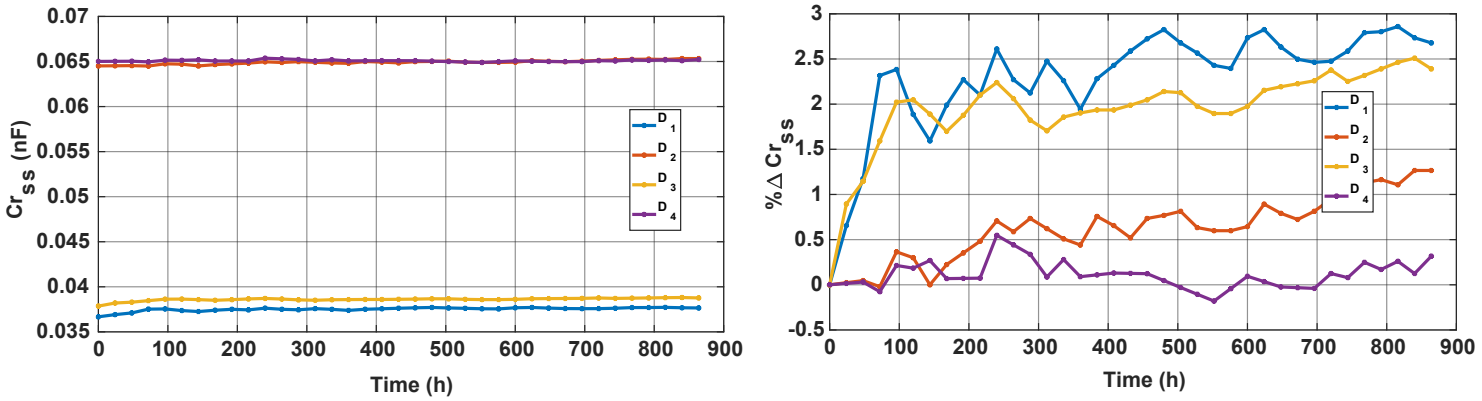
Fig. 5.16 represents the evolution of the output parasitic capacitance $C_{o_{ss}}$ as a function of cycling time. It can be seen that $C_{o_{ss}}$ slightly increases ($\leq 0.8\%$) in the case of D_1, D_2 and D_3 whereas it increases by less than 0.2% in case of D_4. Similarly, Fig. 5.17 represents the evolution of the reverse transfer parasitic capacitance $C_{r_{ss}}$ as a function of cycling time, where it increases by less than 3%, 1.5%, 2.5% and 0.5% in the case of D_1, D_2, D_3 and D_4 respectively. In the same way, Fig. 5.18 represents the evolution of the input parasitic capacitance $C_{i_{ss}}$ as a function of cycling time, where it decreases by less than 0.5%, 0.4%, 0.3% and 0.65% in the case of D_1, D_2, D_3 and D_4 respectively. The net decrease in $C_{i_{ss}} = C_{GD} + C_{GS}$ could be due to gate's oxide fatigue. The measurements of $C_{o_{ss}}$ and $C_{r_{ss}}$ show some incertitude as those capacitances are very low, in the range of some pF. However, the low variation of these parasitic capacitances could be related to the chip fatigue.



a) Absolute values

b) Derivation in precentage

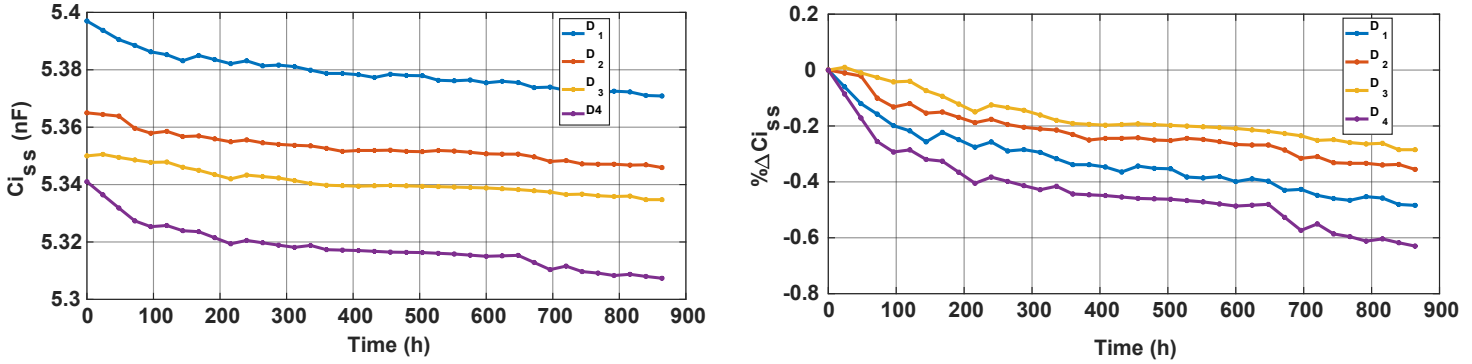
Fig. 5.16: Evolution of $C_{o_{ss}}$ as a function of cycling time



a) Absolute values

b) Derivation in precentage

Fig. 5.17: Evolution of $C_{r_{ss}}$ as a function of cycling time



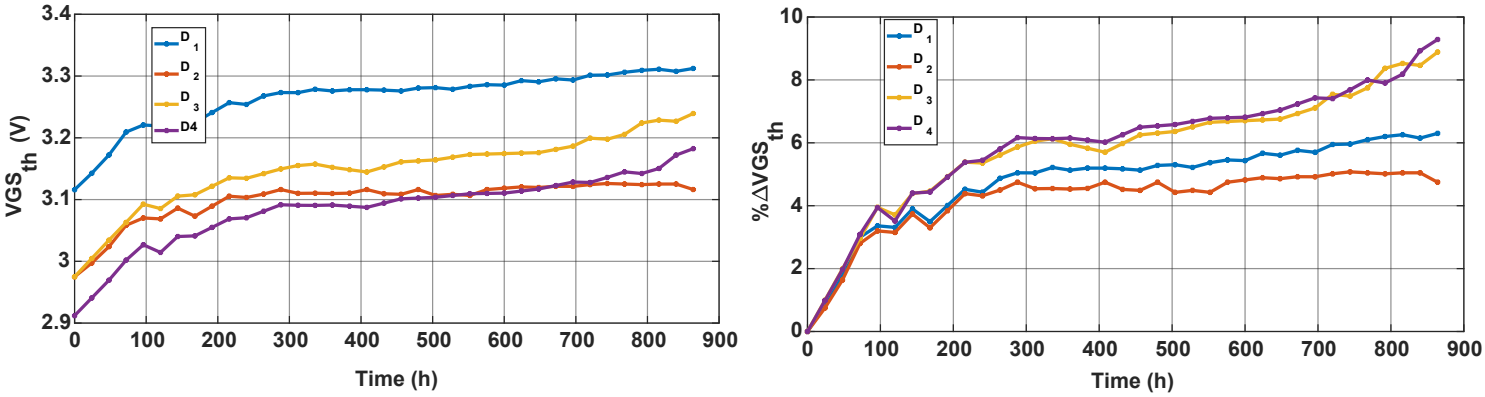
a) Absolute values

b) Derivation in precentage

Fig. 5.18: Evolution of $C_{i_{ss}}$ as a function of cycling time

Fig. 5.19 represents the evolution of the gate-source threshold voltage $V_{GS_{th}}$ of the MOSFETs as a function of cycling time. $V_{GS_{th}}$ increases gradually by approximately 6.5%, 5%, 9% and 9.5% respectively in the case of D_1, D_2, D_3 and D_4. Usually, the gate threshold voltage $V_{GS_{th}}$ is considered as indicator of gate oxide based failures, due to interfacial charge trapped in the case of SiC-based devices at and near the SiC−SiO_2 inversion channel-gate

insulator interface [28]. A derivation of 20% in gate threshold voltage is considered as failure criterion in [36]. This can lead to significant degradation in the device's reliability and performance by shifting the threshold voltage and substantially reducing the effective channel mobility, due to coulombic scattering of the free carriers which are themselves reduced by charge trapping.



a) Absolute values **b) Derivation in precentage**

Fig. 5.19: Evolution of $V_{GS_{th}}$ as a function of cycling time

Meanwhile, Fig. 5.20 represents the evolution of the gate leakage current $I_{GSS(-)}$ of the MOSFETs as a function of cycling time. It can be clearly seen that it has just moved of approximately -10% for all MOSFETs. Similarly, Fig. 5.21 represents the evolution of the gate leakage current I_{GSS} of the MOSFETs as a function of cycling time. It can be clearly seen that in the case of D_4 it increases sharply by approximately 50000% in the last measurement, reaching approximately 460 µA before the damaging of the MOSFET gate's oxide. Meanwhile, the gate leakage current has barely moved in the case of other MOSFETs (less than 200%), as it can be seen in Fig. 5.22, where the large variations are due to measuring incertitude as values are really low. Gate leakage current I_{GSS} is caused by carriers tunneling via the gate insulator, leaking between gate and source, due to gate's oxide failure, which was probably the cause of MOSFET D_4 failure. This could be also due to the overheating of the semiconductor device. It is remarkable that the variation of I_{GSS} is higher than that of $I_{GSS(-)}$ for all MOSFETs. This could be explained by the fact that I_{GSS} is measured for $V_{GS} = +20\ V$ whereas $I_{GSS(-)}$ is measured for $V_{GS} = -5V$.

The evolution of the internal gate resistance R_G is not represented here, since no remarkable variations were detected due to high measurement incertitude.

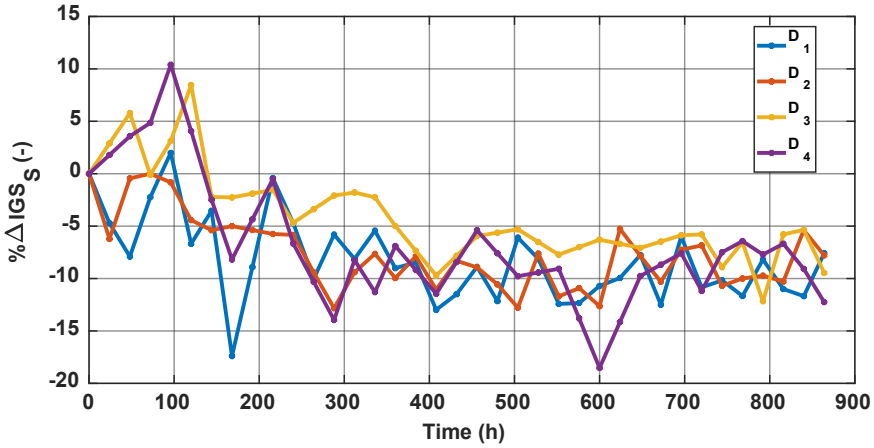
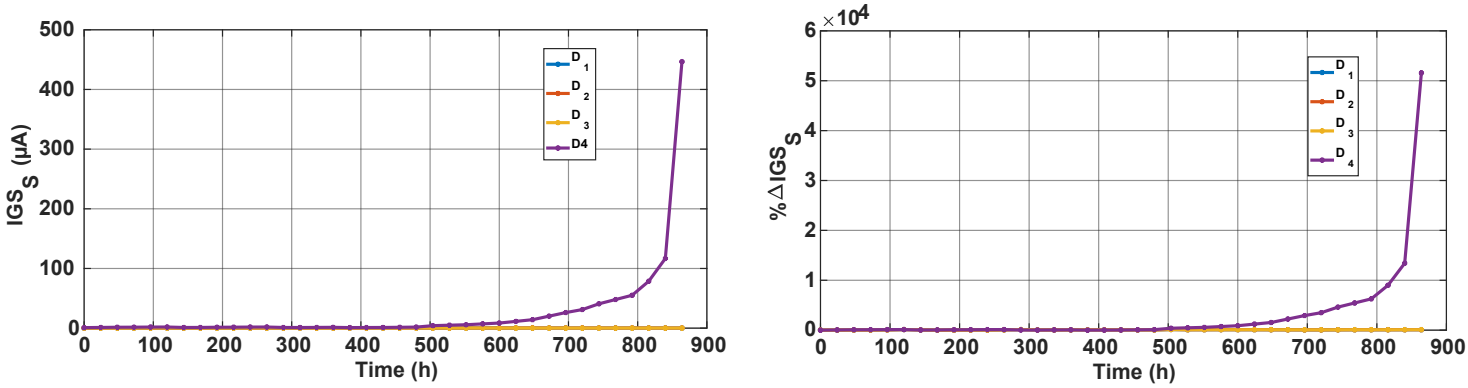


Fig. 5.20: Variation in percentage of $I_{GS_{S(-)}}$ as a function of cycling time



a) Absolute values **b) Derivation in precentage**

Fig. 5.21: Evolution of I_{GS_S} as a function of cycling time

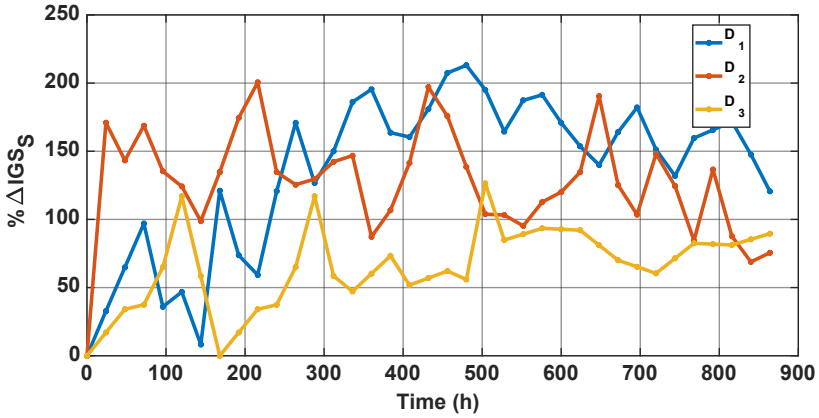
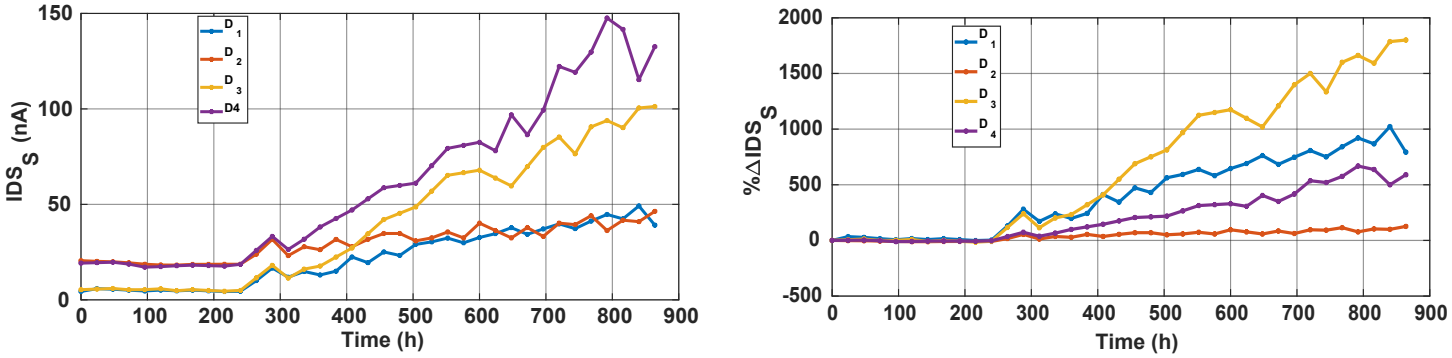


Fig. 5.22: Highlight on Fig. 5.21.b

Fig. 5.23 represents the evolution of the drain leakage current I_{DSS} as a function of cycling time. This parameter decreases a tiny bit gradually during 264 h for all MOSFETs, then increases abruptly of approximately 300%, 63%, 240% and 73% for D_1, D_2, D_3 and D_4 respectively. Then, it continues to increase gradually to reach at the end of the test approximately 800%, 100%, 1800% and 600% in the case of D_1, D_2, D_3 and D_4 respectively. A damage of a single cell in the MOSFET would lead to an increase in the drain leakage

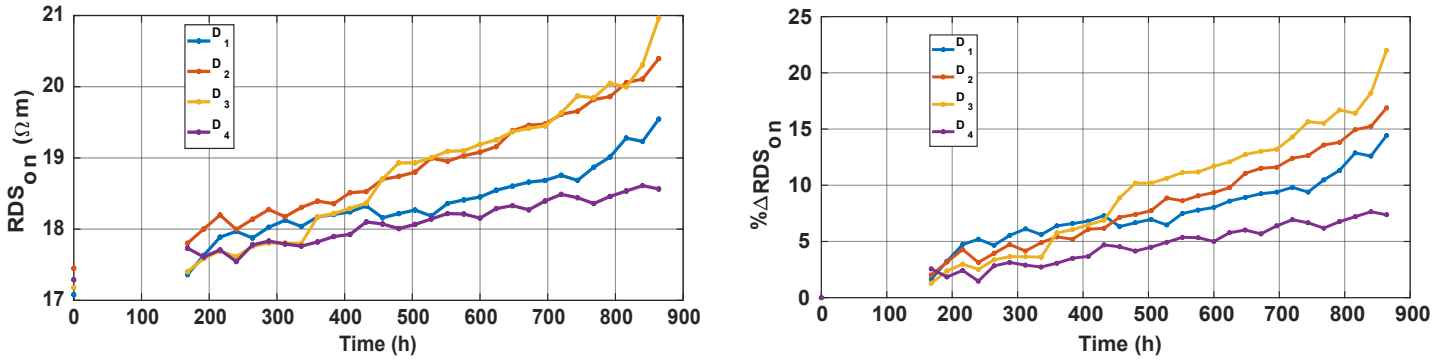
current, while the carriers can leak between source and drain terminals of a MOS (subthreshold conduction) [12].



a) Absolute values b) Derivation in precentage

Fig. 5.23: Evolution of I_{DSS} as a function of cycling time

Similarly, Fig. 5.24 represents the evolution of the MOSFETs drain-source on-state resistance $R_{DS_{on}}$ as a function of cycling time. This parameter increases gradually to reach approximately 15%, 17%, 22% and 7% for D_1, D_2, D_3 and D_4 respectively. Accordingly, the value of $R_{DS_{on}}$ in the case of MOSFET D_3 crosses the commonly used threshold value, corresponding to an increase of 20% above the initial value. The increase of this parameter can be considered as indicator of the wire bonding lift off, a reconstruction of the metallization surface [37] [61], a decrease in device's thermal performances, and/or a degradation of the die given that $V_{GS_{th}}$ has also increased. It should be noted that V_{SD} showed close evolution as that of $R_{DS_{on}}$, being not represented here.



a) Absolute values b) Derivation in precentage

Fig. 5.24: Evolution of $R_{DS_{on}}$ as a function of cycling time

Table 5.4 summarized the results obtained, exhibiting the minimum and maximum variations of the electrical parameters, as well as their corresponding threshold values (Chapter 1 Table 1.3).

According to literature, $R_{DS_{on}}$ is one of the most monitored parameters [12] [45] [62] in APC tests of SiC MOSFET devices, however I_{GS_S} and $V_{GS_{th}}$ are more frequently monitored during gate stress tests [16-18] [28-30]. Nevertheless, in the case of this test simulating the PV application, the results showed that it is probable that the SiC MOSFET gate's oxide could fail before the packaging. However, this is not certain given that the damage could be due to semiconductor device overheating, which couldn't be verified since the thermal impedance

was not monitored. Given the results represented above, $R_{DS_{on}}$, I_{DS_S}, I_{GS_S} and $V_{GS_{th}}$ can be considered as potential ageing indicators of SiC MOSFET devices in photovoltaic inverters. However only I_{GS_S} and $R_{DS_{on}}$ could be considered as failure indicators, since that their variations have reached the correspondent threshold values before I_{DS_S} and $V_{GS_{th}}$. Nevertheless, more tests have to be done on the same device type as well as on others to check if similar results would be obtained.

This work will be completed with further investigations of failure mechanisms with Scanning Acoustic Microscopy (SAM) analysis, where different layers of the packaging can be detectable. Moreover, Scanning Electron Microscopy (SEM) analysis could be used also to detect potential cracks in the gate oxide's metallization, bond wires lift off and heel cracks, metallization degradations, etc.

Table 5.4: Variations of the electrical parameters and their corresponding threshold values

Electrical parameter	Variation (%)		Threshold
	Minimum	Maximum	
Gate leakage current I_{GS_S}	75 %	51570 %	+ 100% above the upper limit
Gate leakage current $I_{GS_{S(-)}}$	-2.5 %	-12.5 %	+ 100% above the upper limit
Gate to source threshold voltage $V_{GS_{th}}$	4.74 %	9.28 %	$\pm$ 20% of the limits
Drain leakage current I_{DS_S}	125.8 %	1800 %	+ 100% above the upper limit
Drain to source on resistance $R_{DS_{on}}$	7.37 %	22.01 %	+ 20% of start value
Input capacitance $C_{i_{ss}}$	-0.28 %	-0.62 %	---
Output capacitance $C_{o_{ss}}$	0.16 %	0.78 %	---
Reverse transfer capacitance $C_{r_{ss}}$	0.31 %	2.67 %	---

5.5. Conclusions

This chapter presented a new concept of ageing test bench dedicated to photovoltaic inverters, where the accelerated ageing tests reproduce the typical profile of the photovoltaic inverters RMS output current designed in Chapter 4.

Initially, the tests' methodology was described, the accelerated ageing tests as well as the failure indicators selection and measurement were depicted. Accordingly, several electrical parameters were selected to be monitored using the *B1506A Keysight* Analyzer. These parameters are: the gate leakage currents I_{GS_S} and $I_{GS_{S(-)}}$, the drain-source on-state resistance $R_{DS_{on}}$, the gate-source threshold voltage $V_{GS_{th}}$, the drain leakage current I_{DS_S}, the body diode forward voltage V_{SD} , the internal gate resistance R_G, the input capacitance $C_{i_{ss}}$, the output capacitance $C_{o_{ss}}$ and the reverse transfer capacitance $C_{r_{ss}}$.

Afterwards, the different steps for designing the 52 kW two-level DC/AC single-phase inverter that was employed during the accelerated ageing were depicted. Accordingly, the choice of the power stack and the current transducers, the designing of the pre-drivers and the load inductor, as well as the temperature regulation and the control systems were detailed.

According to the results obtained, $R_{DS_{on}}$, I_{DS_S}, I_{GS_S} and $V_{GS_{th}}$ showed the most remarkable variations during the accelerated ageing tests. $R_{DS_{on}}$ of MOSFET D_3 increased by approximately 22% exceeding the commonly used threshold value of 20%. This could be due to wire bonding lift off, a reconstruction of the metallization surface, a decrease in device's thermal performances, and/or a degradation of the die given that $V_{GS_{th}}$ has also increased. However, only MOSFET D_4 has failed, directly after a steep increase in the leakage current of approximately 50000%, while the gate became uncontrollable. The increase in gate leakage current could be caused by carriers tunneling via the gate insulator, leaking between gate and source due to gate's oxide failure. Nevertheless, this could be also due to the overheating of the semiconductor device. Moreover, the gate threshold voltage has increased showing instability, which could be due to the interfacial charge trapped in the case of SiC-based devices at and near the $SiC-SiO_2$ inversion channel-gate insulator interface

This work will be pursued by further investigation of failure mechanisms with Scanning Acoustic Microscopy (SAM) analysis, where different layers of the packaging can be detectable. Moreover, Scanning Electron Microscopy (SEM) analysis can be also used to detect potential cracks in the gate oxide's metallization, bond wires lift off and heel cracks, metallization degradations, etc.

According to literature, $R_{DS_{on}}$ is one of the most monitored parameters in APC tests of SiC MOSFET devices, however I_{GS_S} and $V_{GS_{th}}$ are more frequently monitored during gate stress tests. Nevertheless, in this type of tests simulating the PV application, the results showed that SiC MOSFET gate's oxide could fail before the packaging. However, this is not sure since the damage could be due to semiconductor device overheating, which couldn't be verified as that the thermal impedance was not monitored due to time constraints. Given the results represented above, $R_{DS_{on}}$, I_{DS_S}, I_{GS_S} and $V_{GS_{th}}$ can be considered as potential ageing/failure indicators of SiC MOSFET devices in photovoltaic inverters.

Accordingly, in this type of tests simulating the PV application, the results showed that SiC MOSFET gate's oxide could fail before the packaging, which leads to think that IGBTs are more reliable than SiC MOSFETs used in PV application. However, this is not certain since the damage could be due to semiconductor device overheating, which couldn't be verified as the thermal impedance was not monitored due to time constraints.

Actually, the main purpose of this study was to apply the tests in a real test bench, in order to check their feasibility, duration and complexity, as well as to find potential indicators of failure corresponding to this type of tests. Thus, being new, the accelerated ageing tests presented in this chapter were applied for a preliminary check. Hence, a campaign of tests has to be executed in the future on the same device type as well as on others to check if similar results could be obtained.

These tests have demonstrated comparable duration to that of a classical power cycling, while they are expected to show more representative results, leading to reduce the favoring of certain failure modes to the detriment of others. Therefore, it would be of high interest to apply classical power cycling to the same devices to compare the obtained indicators variations and failure mechanisms.

Furthermore, the parameters of the accelerated ageing profiles could be modified to test the impact of each parameter on the obtained failure mechanisms and indicators. Moreover, it could be interesting to also apply the second methodology, in order to compare its results with those obtained with the 1st methodology. In addition, it could be interesting to readjust these methodologies so that the devices are kept at peak temperature while eliminating the temperature swings. Accordingly, it would be possible to check if the temperature swings accelerate more the ageing of SiC MOSFET than by keeping them at peak temperature.

Chapter 6:
In-situ condition monitoring system and IGBT accelerated ageing tests

Chapter 6: In-situ condition monitoring system and IGBT accelerated ageing tests

6.1. Introduction

The ageing/failure indicators in the case of the MOSFET's test bench were monitored by disconnecting the devices from the power stack as demonstrated in Chapter 5. Indeed, the purpose was to determine the maximum number of potential indicators of SiC MOSFET's failures in a PV application, however this process is complicated and time-consuming. Since the failure indicators of IGBT power modules are well known, an in-situ Condition Monitoring (CM) setup will be developed in the case of IGBT's test bench to automatically monitor the devices condition. The purpose of this setup is to be finally deployed in a condition monitoring system of PV inverter's semiconductors, where measurements are performed during the night.

This chapter presents the accelerated ageing and condition monitoring test bench of the IGBT power modules, where the accelerated ageing profiles of the current and ambient temperature designed in Chapter 4 will be applied (refer to Chapter1 Fig. 1.36). Similarly to Chapter 5, passive and active cycling are simultaneously applied during the tests under switching nominal conditions and pulse width modulation (PWM) operating mode, using the opposition method. The ageing test is regularly interrupted to apply an in-situ monitoring of different damage indicators [27] [39] [58] [59] [60]. As it will be demonstrated, during the condition monitoring phase these indicators are measured in an unclassical way without disconnecting the devices.

Initially, the condition monitoring methodology then the accelerated ageing and CM test bench will be described. Afterwards, the developed in-situ measurement method will be compared and validated with *B1505A Keysight* analyzer and traditional thermal impedance measurement method. Then, the results of the ageing tests will be completed by an acoustic microscopy analysis. Lastly, several examples of implementation in PV inverters will be proposed.

6.2. In-situ condition monitoring methodology

6.2.1. General methodology

The electrical diagram of the ageing test bench is based on a single-phase inverter feeding a pure inductive load (Fig. 6.1). As represented in Fig. 6.2 and as proposed in [58] and [61], this inverter is successively used for monitoring the condition of the semiconductor devices, and for accelerating their ageing by applying the same method represented in Chapter 5. A relaxation phase is added between the production/ageing and the monitoring phases, by stopping the inverter during several tens of minutes in order to decrease the devices' temperature [123] [124]. When a damage indicator crosses a defined damage threshold, the accelerated ageing is stopped.

In this setup, the condition monitoring phase allows for an in-situ measurement of three damage indicators of each semiconductor device. The first ageing indicator is the collector-emitter voltage V_{ce} for IGBTs or the forward voltage V_f for diodes. The second indicator is the dynamic resistance r_d, and the third one is the thermal impedance Z_{th}. As demonstrated in Chapter 1, in the case of silicon devices the increase in V_{ce} and V_f can indicate bond wire lift off and/or heel crack, or a reconstruction of the metallization surface. Similarly, an increase in Z_{th} is considered as an indicator of the soldering and/or substrate fatigue. It should be noted that r_d is monitored since it is supposed to be more sensitive to the wire bonding degradation than V_{ce} or V_f. According to literature, this parameter has never been monitored yet in a similar way.

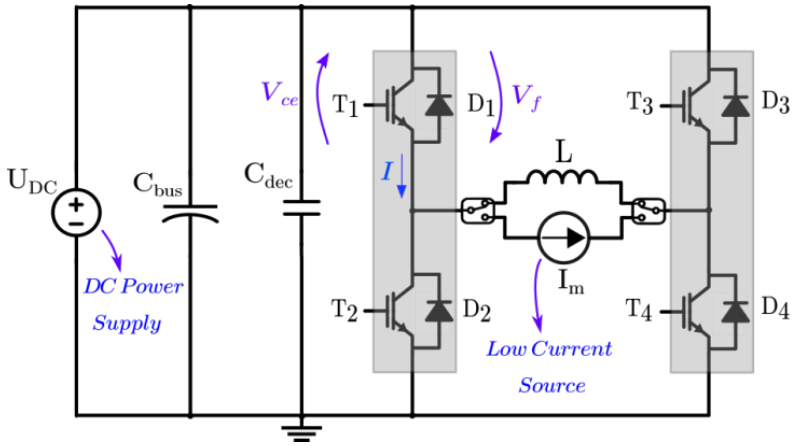


Fig. 6.1: Schematic of the power inverter in back-to-back configuration

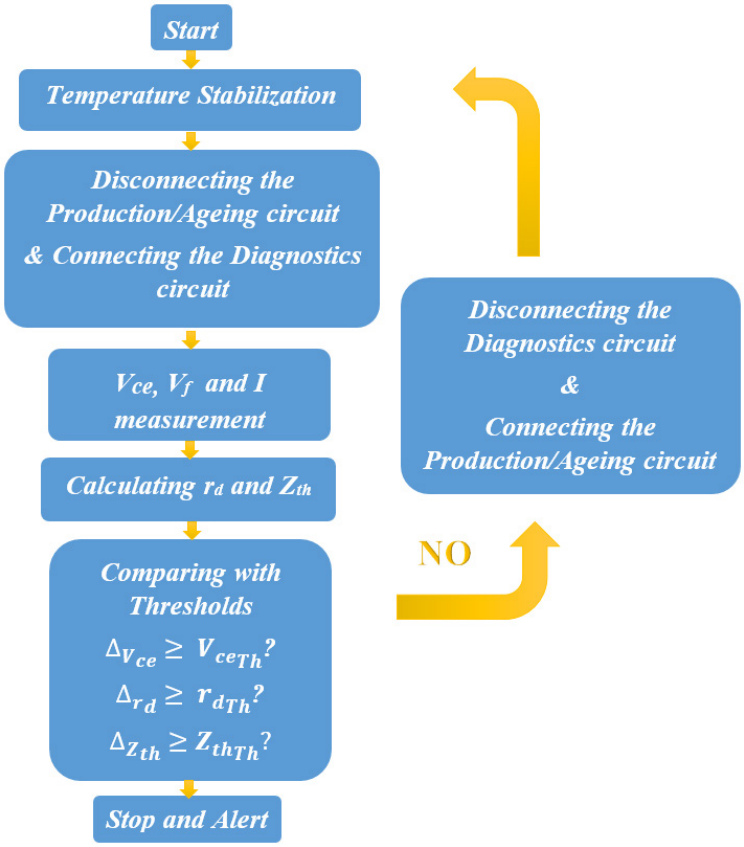


Fig. 6.2: General principle of the proposed condition monitoring method

6.2.2. In-situ condition monitoring

6.2.2.1. Parameters calculation

It should be noted that in the previous chapters, the semiconductor devices were defined as D_1 to D_8. However, in this chapter and for a better distinction between the different devices' conduction phases, the transistors will be defined as T_1 to T_4, whereas the diodes as D_1 to D_4, as illustrated in Fig. 6.1.

During diagnostics phase, four monitoring configurations are successively applied to characterize the damage indicators of four devices' couples: (T_1, D_3), (T_2, D_4), (T_3, D_1) and (T_4, D_2). In order to simplify the depiction of the method, only the estimation of IGBT T_1 damage indicators will be represented. Accordingly, the monitoring cycle demonstrated in Fig. 6.3 is used to characterize (T_1, D_3).

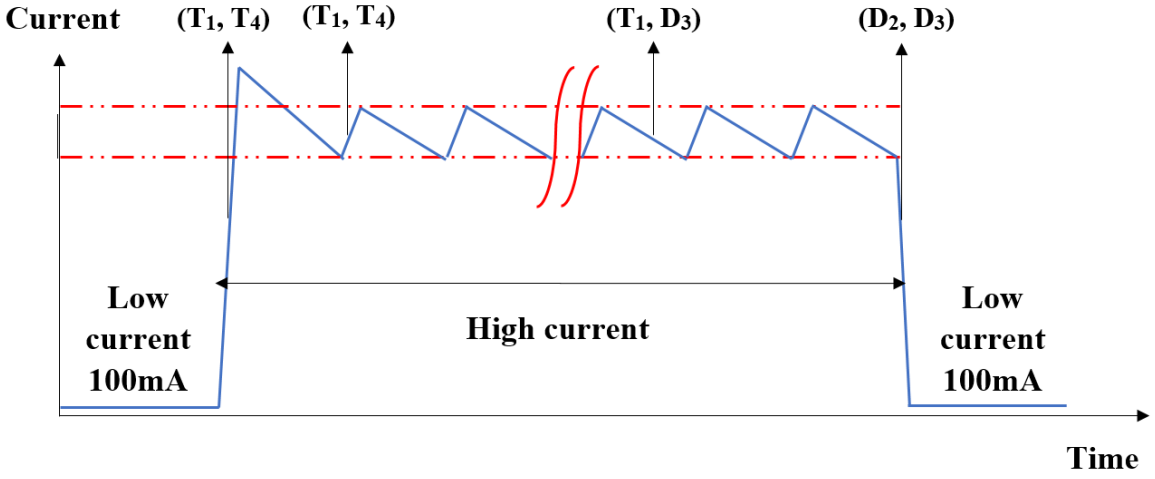


Fig. 6.3: Monitoring cycle for (T_1, D_3) (typical current's waveform)

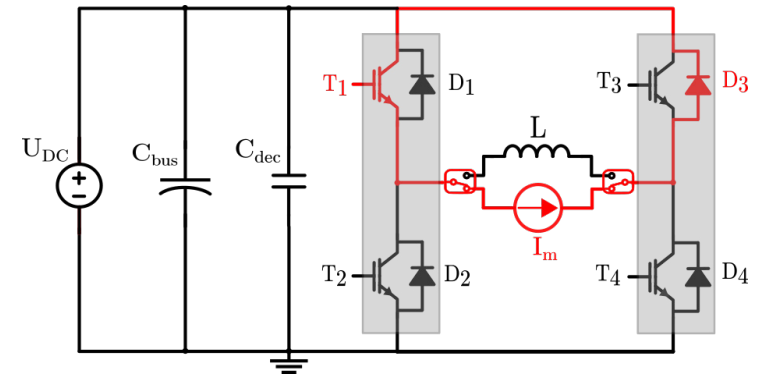
Initially, the V_{ce} value under a low current of 100 mA is measured to estimate the junction temperature $T_{J_{start}}$ of the IGBT, just before the high current injection. For this measurement, T_1 and T_3 are in on-state and T_2 and T_4 in off-state, as represented in 172. After a while, T_4 is turned-on and T_3 turned-off, leading to a rise of the load's current as represented in 172. Then, after several tens of µs T_4 is turned-off, which results in a slow V_{ce} voltage's decrease allowing the measurement of the first damage indicator V_{ce} under high current as represented in 172. Afterwards, T_1 is turned-off as illustrated in 173 leading to cancel the high current, before the low current injection. Furthermore, during the first freewheeling phase of the current, V_{ce} and I are simultaneously measured for different times which allows for an estimation of the IGBT dynamic resistance r_d as represented in Fig. 6.5. This is done, by linearly fitting the corresponding measurements V_{ce_0} and I_0 $(V_{ce_0} = f(I_0))$, as demonstrated in Fig. 6.6, using the following equation:

$$V_{ce_0} = r_d \cdot I_0 + V_{ce_{th}} \tag{6.1}$$

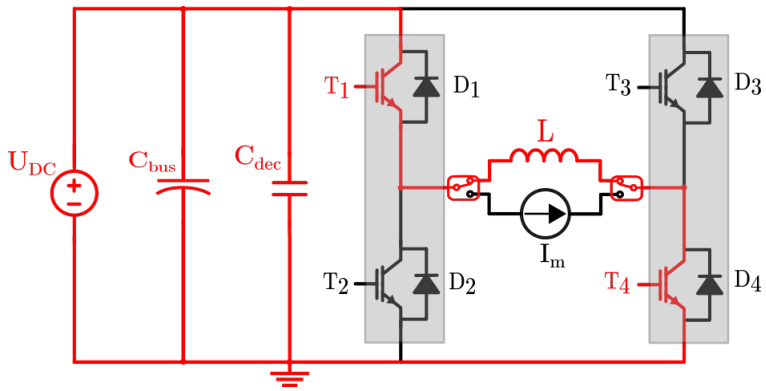
where $V_{ce_{th}}$ represents the collector-emitter threshold voltage of the IGBT. After a while, the high current in the transistor is canceled by turning-on T_2 and T_3, and then the voltage V_{ce} can be measured under an injected current of 100 mA. Thus, the junction temperature $T_{J_{end}}$ after the current injection can be estimated, and then used to calculate a thermal impedance value:

$$Z_{th} = \frac{T_{Jend} - T_{Jstart}}{P} \tag{6.2}$$

where P is the mean power dissipated by the IGBT during the current injection, estimated by multiplying $V_{ce\,High\,Current}$ by $I_{High\,Current}$ (Fig. 6.5). Note that the power varies with time during the current injection, since V_{ce} is temperature-dependent [37]. However, this phenomenon is not considered in this setup, since the objective is not to measure the exact thermal impedance value, but rather its increase with ageing. Concerning D_3, the estimation of the power loss is a bit more complicated, since it switches during the monitoring cycle. Switching losses are thus added to conduction losses using current measurements and switching energies from the manufacturer's datasheets.



a)



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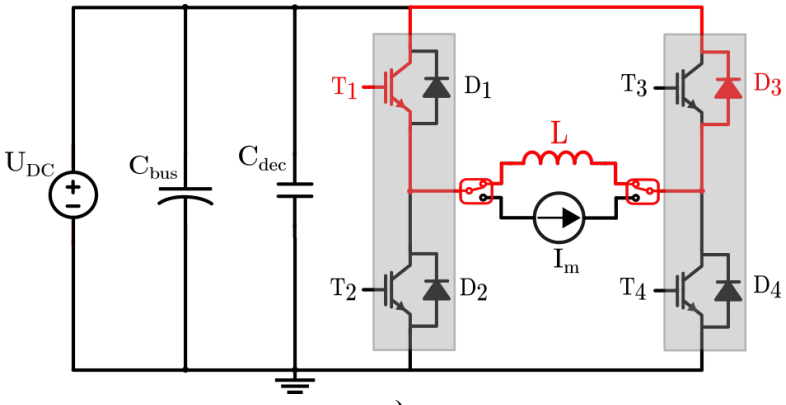

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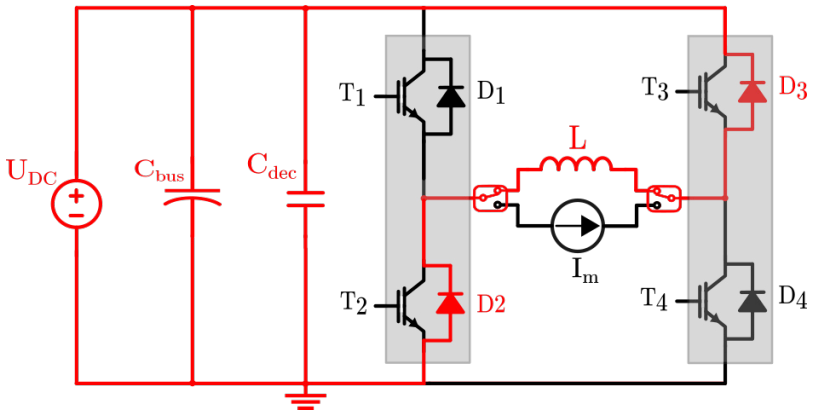


d)

Fig. 6.4: Different conduction phases

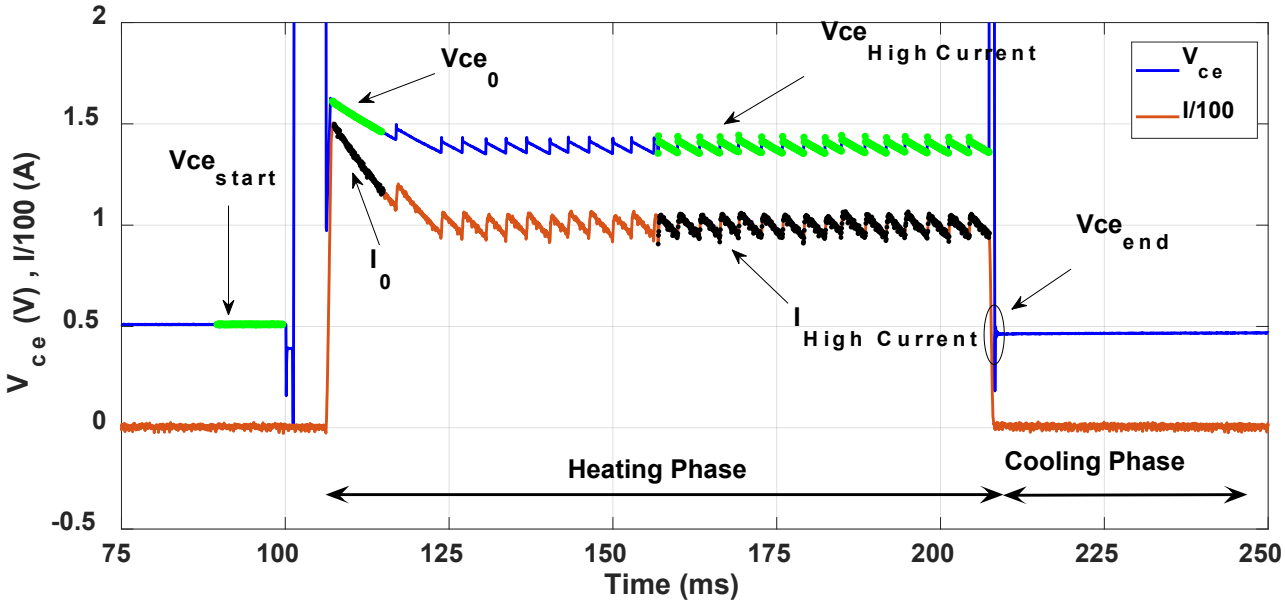


Fig. 6.5: Monitoring cycle for (T_1, D_3) (real measurement waveforms of V_{ce} and I)

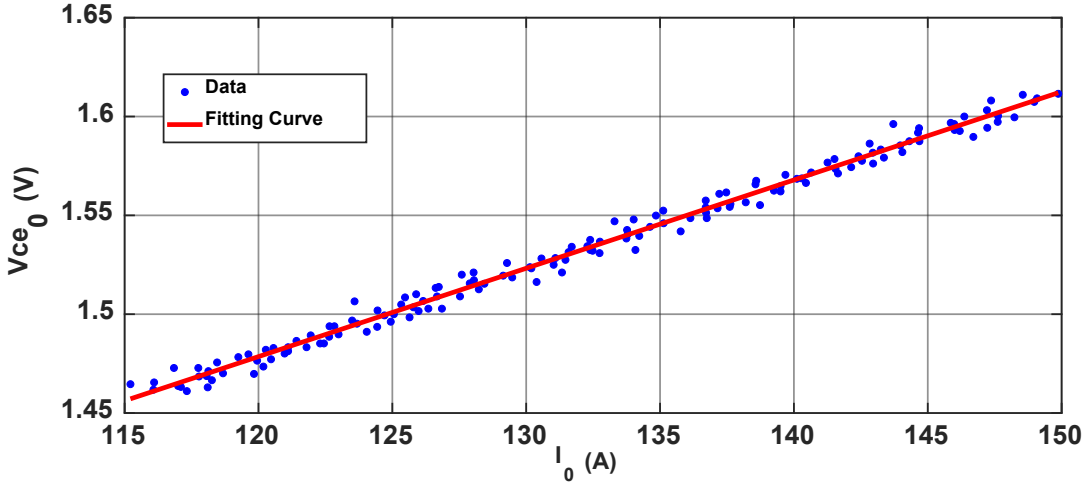


Fig. 6.6: Fitting the equation of V_{ce_0} represented as a function of I_0

6.2.2.2. TSEP measurement and calibration

According to Eq. 6.2, the semiconductors junction temperature should be determined in order to calculate the thermal impedances of the system. However, since the direct measurement of this temperature during semiconductor's conduction is still complicated, it is estimated using a thermo-sensitive electrical parameter (TSEP) [36] [63] [64] [66] [140]. This TSEP is the collector-emitter voltage V_{ce} under a low current of 100 mA for the IGBTs as presented in Chapter 3. Similarly, the TSEP for the diodes is the forward voltage V_f measured under the same current level.

6.3. IGBT's test bench

6.3.1. Power stack

The back-to-back configuration illustrated in Fig. 6.1 can be obtained using a power stack as that selected for the test: the *SEMIKRON SemiKube T0.5 IGD-1-424-P1N4-DL-FA* shown in Fig. 6.7. It is a full bridge three-phase power stack integrating:

- *SKM400GB12E4* IGBT power modules (1200V- 400A)
- IGBT drivers
- Measurement of phases current and DC-link voltage
- Protection and user interface electronics

The main electrical characteristics of the power stack are exhibited in Table 6.1.

Table 6.1: Main electrical characteristics of the *SEMIKRON* power stack

Electrical characteristic	***Value***
Rated DC voltage E	*750 V*
Rated output current I_{out_r}	*200 A*
Output voltage V_{out}	*400 V*
Rated output power P_{out_r}	*140 kW*
Maximum switching frequency f_{sw_m}	*25 KHz*
DC-link capacitors C_{bus}	*1.68 mF*
Drivers' supply voltage V_{dr}	*24 V*

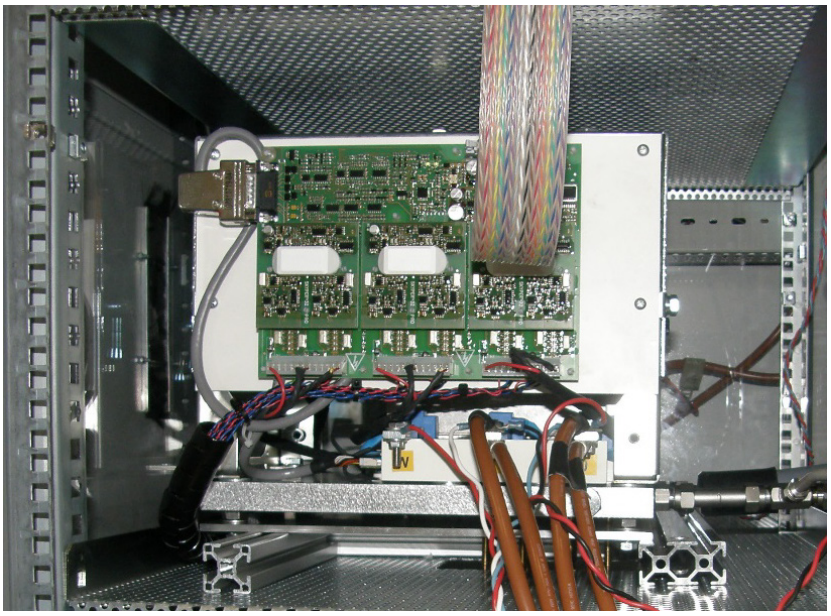


Fig. 6.7: SEMIKRON SemiKube T0.5 IGD-1-424-P1N4-DL-FA power stack

In order to simplify the accelerated ageing test, the three *SKM400GB12E4* power modules with a nominal current of 400 A were replaced by two *SKM200GB12E4* (1200V-200A phase-leg IGBT power modules with anti-parallel diodes) having the same *SEMITRANS3* packaging (Fig. 6.8). Originally, the power stack is mounted on air-cooled heat sink but it was replaced with a liquid-cooled heat sink similar to that presented in Chapter 5 Section 5.3.3 for MOSFET power modules. Similarly, the cold plate is drilled under the center of the semiconductors chips positions to allow the insertion of thermocouples.

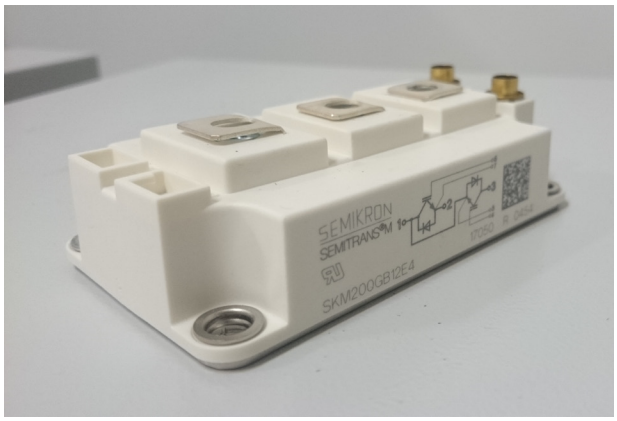


Fig. 6.8: SKM200GB12E4 IGBT power module

As represented in Chapter 5 Section 5.3.1, when using the opposing method the inverter consumption is only equal to its power losses. Thus, the same power supply *PS 9000 3U Series* 1.5 kV– 30 A–15 kW used for the MOSFET test is also employed here to source the DC-link voltage *E=750 V*.

During the diagnostics phase, the load inductor should generate a fast current ramp to measure V_{ce} under high current, without causing significant thermal heating of the semiconductors' junction. However, this ramp should not be too fast comparing to the acquisition system that measures V_{ce}. Accordingly, the calculations led to a load inductor L of 120µH.

6.3.2. Measurement PCBs

Three PCBs were developed in *CEA-INES* in order to perform the diagnostics method described in the previous section. The first PCB is dedicated to V_{ce}, V_f and V_{ge} measurements, as well as to adapt the I/O signals between the *PXI* and the power stack. The measurement precision should be of approximately 1mV with voltage withstand of 1400V, using an operational amplifier with high common-mode rejection ratio and PhotoMOS relays.

The second PCB injects a bidirectional low current of 100 mA for TSEP measurement. At the same time, the PCB should withstand the DC-link voltage during the ageing phase, thus the current source is inserted in a MOSFET full bridge topology circuit. With a response time lower than 3µs, the PCB allows a fast injection of the low current directly after the heating phase (Fig. 6.5).

The third PCB serves as a switch, disconnecting the load inductors during the diagnostics phase and connecting the low current source, using MOSFETs with switching times lower than 50 µs.

6.3.3. Control system and full test bench

All the components of the IGBT's test bench are controlled by a *PXI* system, similar to the one employed for the MOSFET test and represented in Chapter 5 Section 5.3.4. However, the *PXI* system used for the IGBT test integrates the additional acquisition thermocouple module *NI PXIe-4353* with 32 channels (24-bit, 90S/s).

The FPGA core system drives the IGBTs and the DC-link power source. It also controls in real-time the different PCB and controls the coolant fluid's temperature. The implementation diagram of the CM method with *LabVIEW* is illustrated in Fig. 6.9, whereas Fig. 6.10 represents a screenshot of the HMI. Furthermore, the connections between the different test bench's components are demonstrated in Fig. 6.11, whereas Fig. 6.12 shows the electrical cabinet of the test bench.

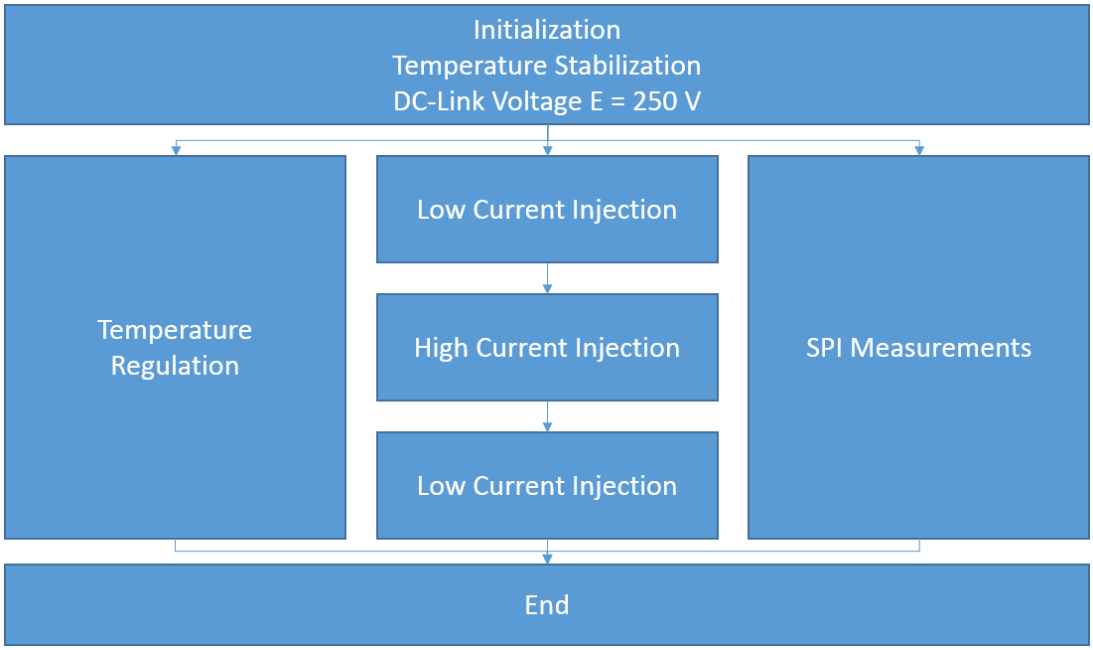


Fig. 6.9: Implementation diagram of the CM method with LabVIEW

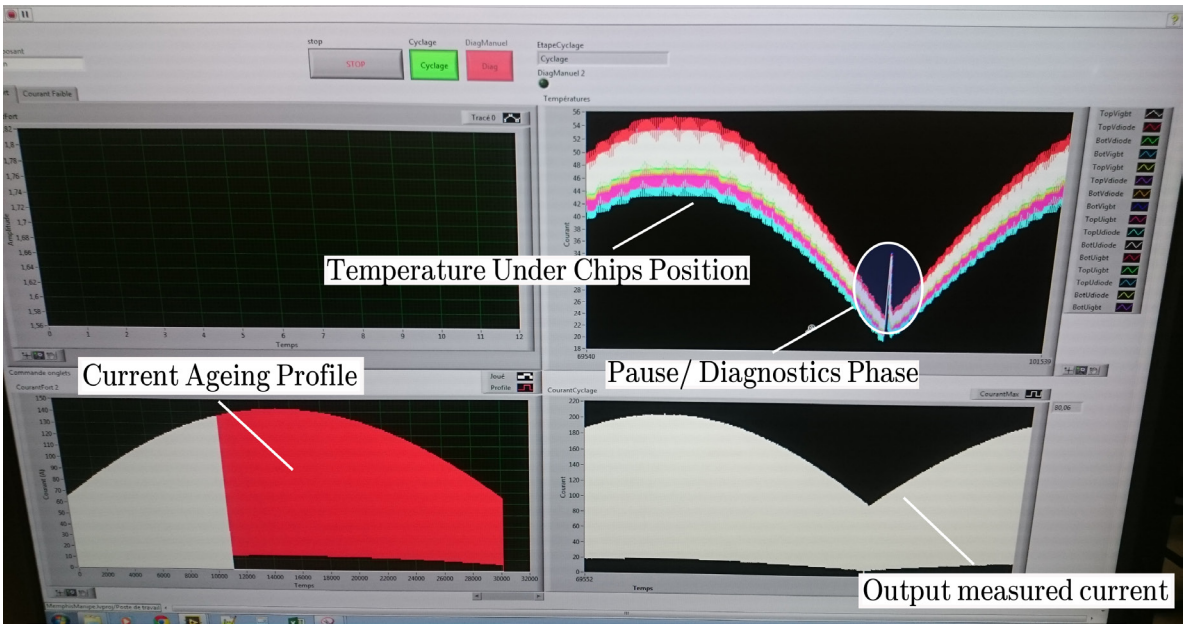


Fig. 6.10: Screentshot of the HMI

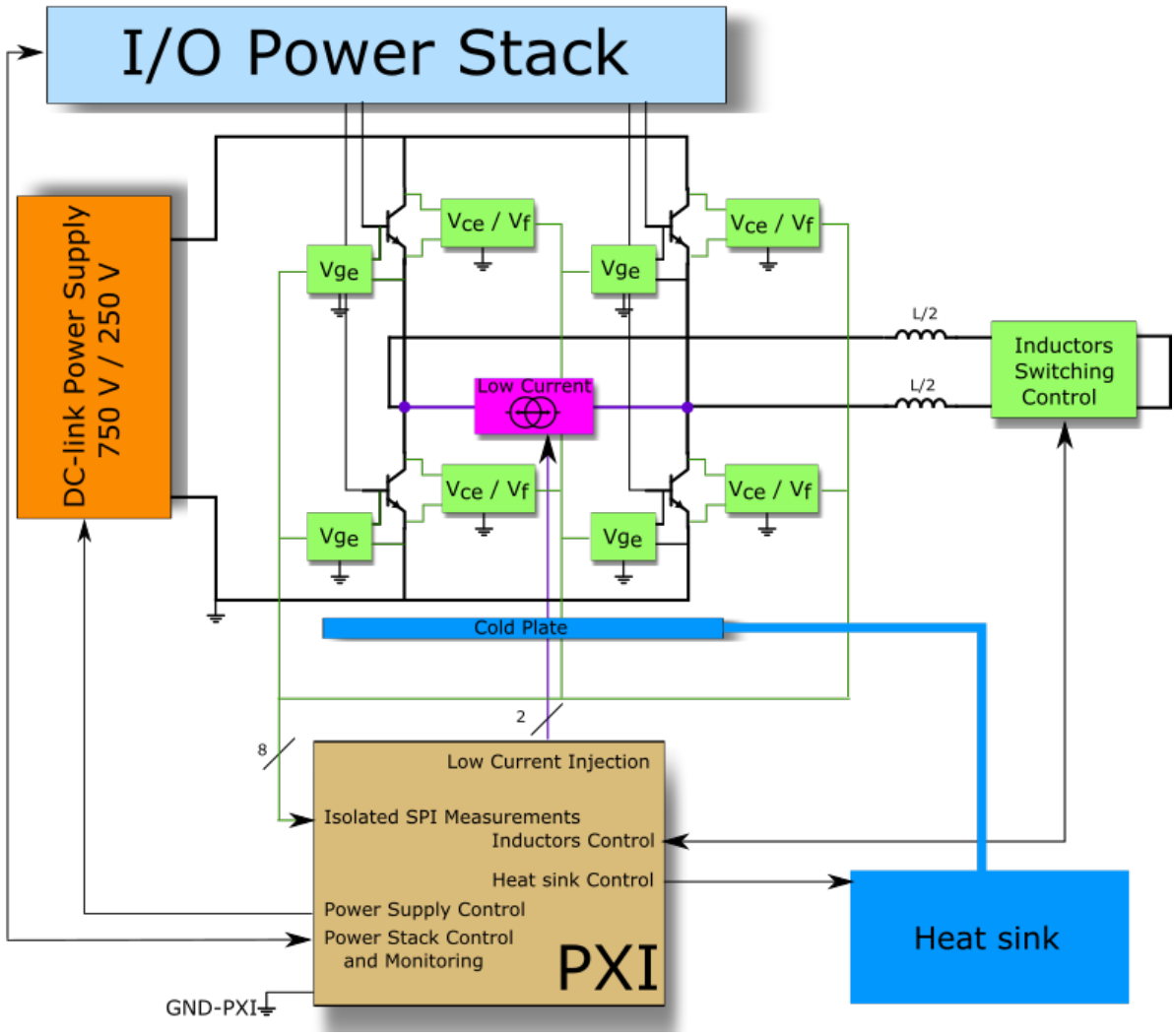


Fig. 6.11: Connections between the different components of the test-bench

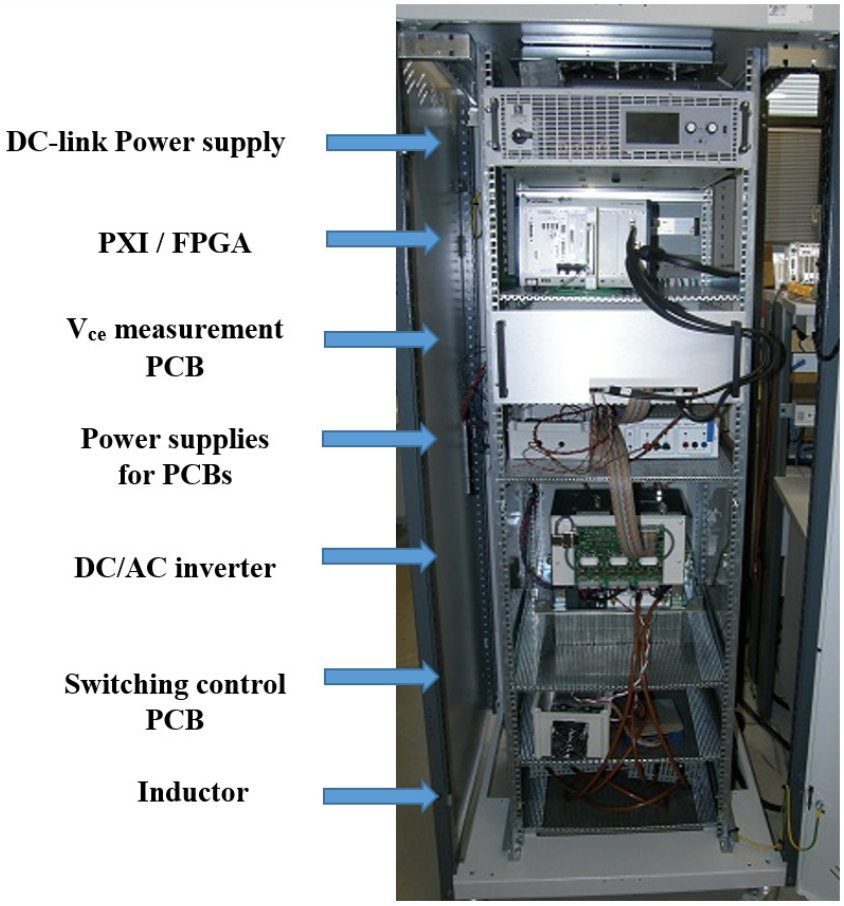


Fig. 6.12: Electrical cabinet of the test bench

6.4. Validation of the in-situ condition monitoring system

Before using the condition monitoring setup previously described, it is crucial to validate V_{ce},V_f, r_d and Z_{th} measurements, as it will be represented in the following sections.

6.4.1. Validation of V_{ce}, V_f and r_d measurements

It should be noted that the study presented in this chapter is a part of the *ANR MEMPHIS* project, in collaboration with *SATIE/IFSTTAR* laboratory. Accordingly, in order to validate the measurements of V_{ce}, V_f and r_d, two IGBT power modules were tested at *SATIE/IFSTTAR* laboratory using the *B1505A Keysight* Analyzer at different temperatures. The IGBTs' collector current I_c was measured as a function of collector-emitter voltage V_{ce} for V_{ge}=15 V, as well as the diodes' forward current I_f was measured as a function of forward voltage V_f.

Consequently, the values of V_{ce} and V_f corresponding to a 140 A current are compared with the values obtained with the test bench as demonstrated in Fig. 6.13, while the obtained values of r_d are compared in Fig. 6.14. It is noticeable that the maximum difference between the V_{ce} measurements for all devices is less than 5%. Similarly, the maximum difference between the r_d measurements is less than 10% for IGBTs and less than 12% for diodes. Therefore, considering the results represented above, it can be visible that the precision

of V_{ce},V_f and r_d measurements of the test bench is comparable to that of *B1505A Keysight* Analyzer.

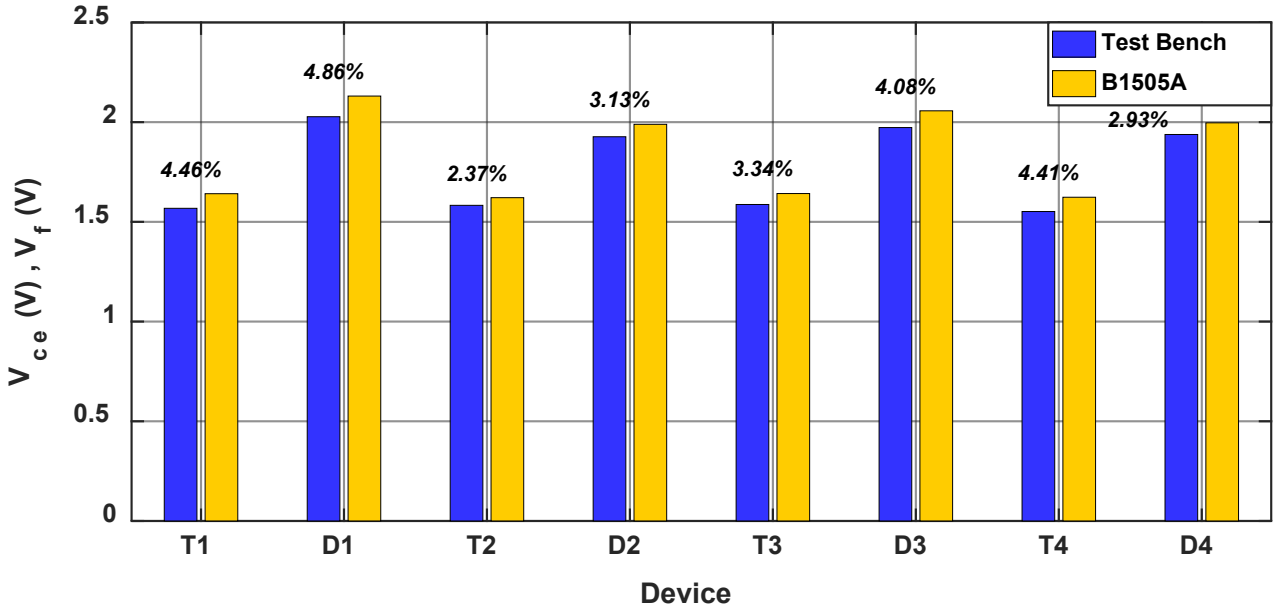


Fig. 6.13: Comparative histograms of V_{ce} and V_f values corresponding to a 140 A current obtained with test bench and *B1505A* measurements

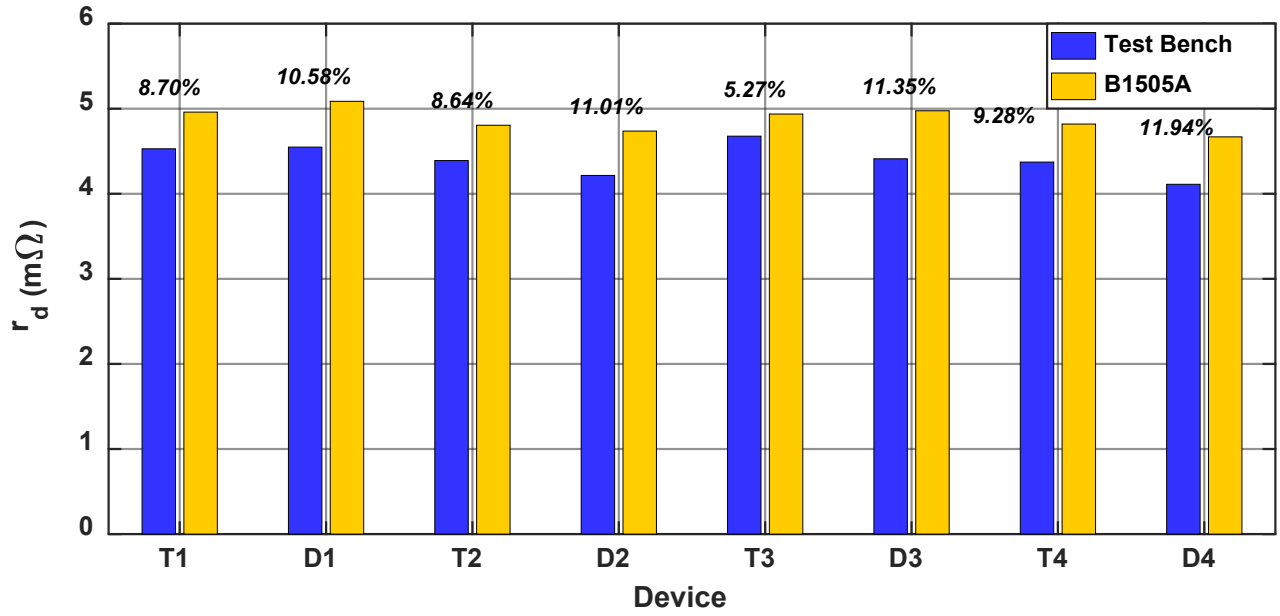


Fig. 6.14: Comparative histograms of r_d values obtained with test bench and *B1505A* measurements

6.4.2. Validation of thermal impedance measurement

In order to validate Z_{th} measurement, several measurements of the thermal impedances were executed using the in-situ method with different current injection durations (between $10^{-2}s$ and 10s). Then, the results were compared with those obtained with the

classical method presented in Chapter 3 Section 3.5. Accordingly, Fig. 6.15 represents a comparison between the measured thermal impedances of IGBT T_1 obtained by both the classical and the in-situ methods, while Fig. 6.16 represents the same for diode D_1.

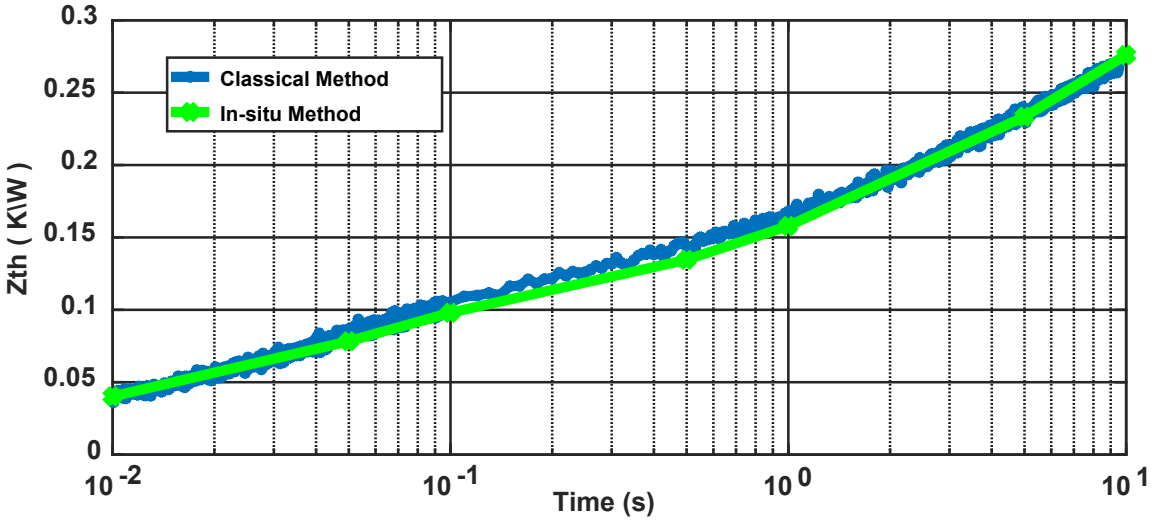


Fig. 6.15: Thermal impedance of IGBT T_1 obtained by both methods

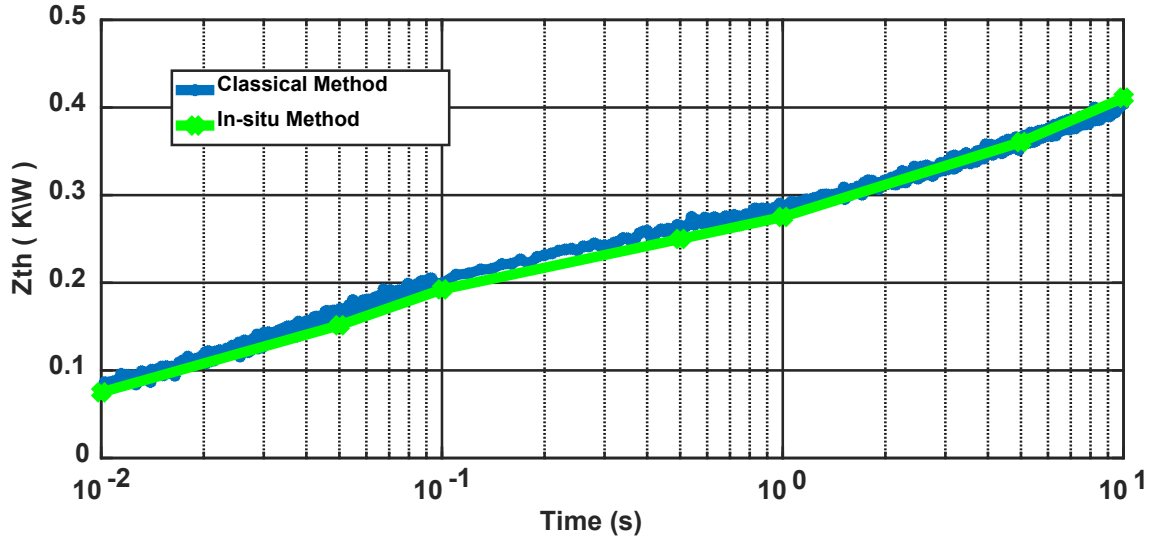


Fig. 6.16: Thermal impedance of diode D_1 obtained by both methods

It can be noticed that the results obtained with the in-situ method are very close to those obtained with the classical method, which allows the validation of the in-situ method. Here, only the results for T_1 and D_1 are represented, however, the measurements for the other devices show similar results.

In a CM system, the measurement of the thermal impedance using the in-situ method can be done just by calculating some points, as represented in Fig. 6.15 and Fig. 6.16. Each point corresponds to one current pulse duration. The choice of the pulse duration is important in the final application, as it will determine the type of degradations that could be observed. For very short durations (several ms), it will be possible to observe the degradation of the die-attach. However, for the duration of several tens of ms to several hundreds of ms, the measurements will be impacted by substrate damages. Nevertheless, for longer durations

(several s to several hundreds of s), it will be possible to observe the degradation of the thermal interface material or the cooling device respectively.

6.5. Application of the accelerated ageing tests

The accelerated ageing profiles of the current and ambient temperature designed in Chapter 4 were applied during two accelerated ageing campaigns of IGBT *SKM400GB12E4* power modules. The application of one ageing profiles takes approximately 8.7 h, followed by a diagnostic phase allowing for an in-situ monitoring of V_{ce},V_f, r_d and Z_{th}.

Due to technical issues encountered with a PCB and time constraints, the two accelerated ageing tests -each lasting for 210 hours- were stopped very early before the failure of the power modules. However, they were long enough to notice an evolution of V_{ce},V_f, r_d and Z_{th} during both tests. Correspondingly, Fig. 6.17 represents in percentage the variation of V_{ce} and V_f of devices T_1 and D_1 respectively as a function of test time. It is noticeable that V_{ce}'s value increased gradually of approximately 1%, whereas V_f increased similarly of approximately 0.6%. Usually, an increase of this voltage under given current and temperature of 5% (commonly used threshold) indicates the power module fatigue.

Similarly, Fig. 6.18 represents T_1 and D_1 dynamic resistance's variation in percentage as a function of test time. r_d's value increased gradually of approximately 4.5% in the case of T_1 and of approximately 2.2% in the case of D_1. It is noticeable that for the same devices and ageing tests, the semiconductors' dynamic resistance showed approximately 4 times more sensitivity to packaging degradation than that of V_{ce} and V_f. Thus, monitoring r_d instead of V_{ce} and V_f could allow for more precise measurements, and an easier detection of wire bonding lift-off, usually identified by a slight sudden increase of V_{ce} and V_f during the ageing tests [37].

Lastly, Fig. 6.19 represents T_1 and D_1 thermal impedance's variation in percentage as a function of test time. Z_{th}'s value increased gradually by approximately 3.5% for T_1 and by approximately 1.3% for D_1. Usually, an increase of approximately 20% of this parameter is considered as an indicator's threshold of the soldering and/or substrate fatigue. It should be noted that the other semiconductors showed similar results in both tests, so they will not be represented here. Eventually, in a photovoltaic inverter these parameters can be potentially used as indicators of semiconductors' ageing, a theory that could be validated with supplementary ageing tests.

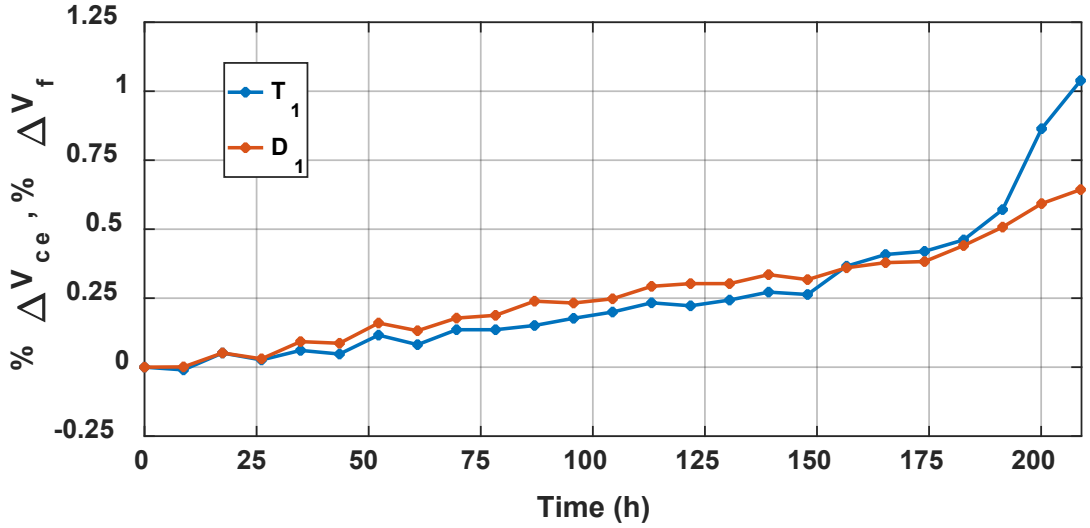


Fig. 6.17: Variation in percentage of V_{ce} and V_f of T_1 and D_1 respectively as a function of the test time

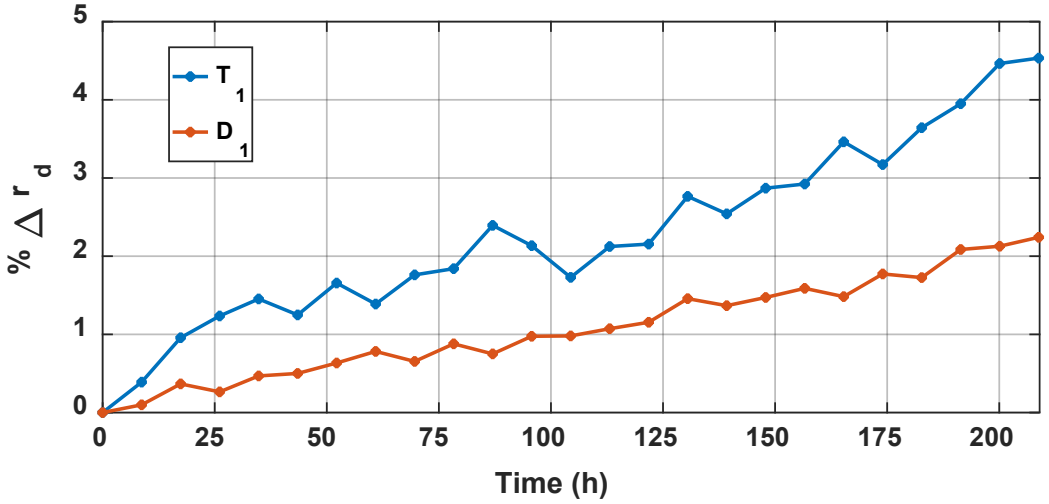


Fig. 6.18: Variation in percentage of r_d of T_1 and D_1 as a function of test time

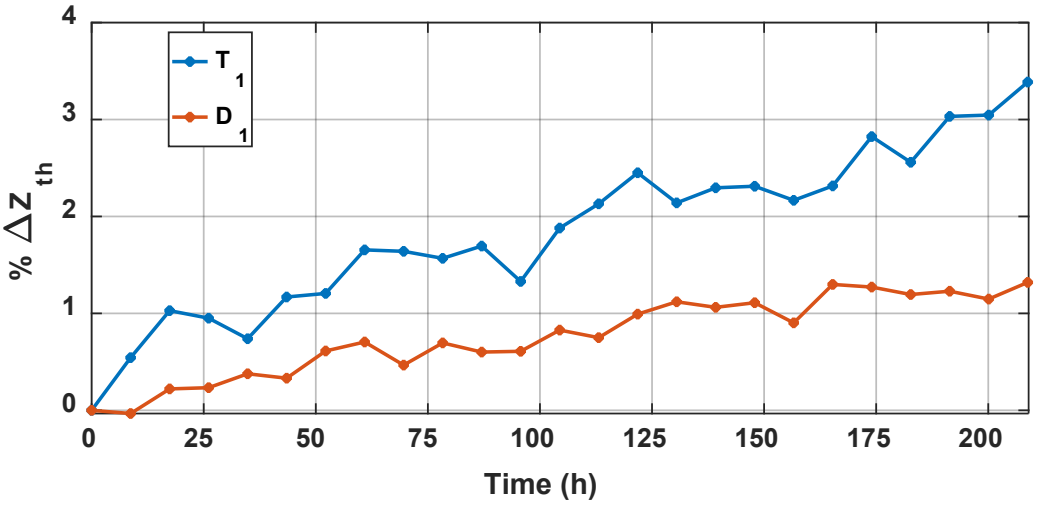


Fig. 6.19: Variation in percentage of Z_{th} of T_1 and D_1 as a function of test time

An acoustic microscopy analysis was performed in *SATIE/IFSTTAR* laboratory on the four power modules after ageing tests. Fig. 6.20 demonstrates substrate layer in one the IGBT power modules, where it can be seen that a substrate's delamination start to propagate. However, further analysis should be done for longer ageing tests, in order to determine the corresponding degradation modes.

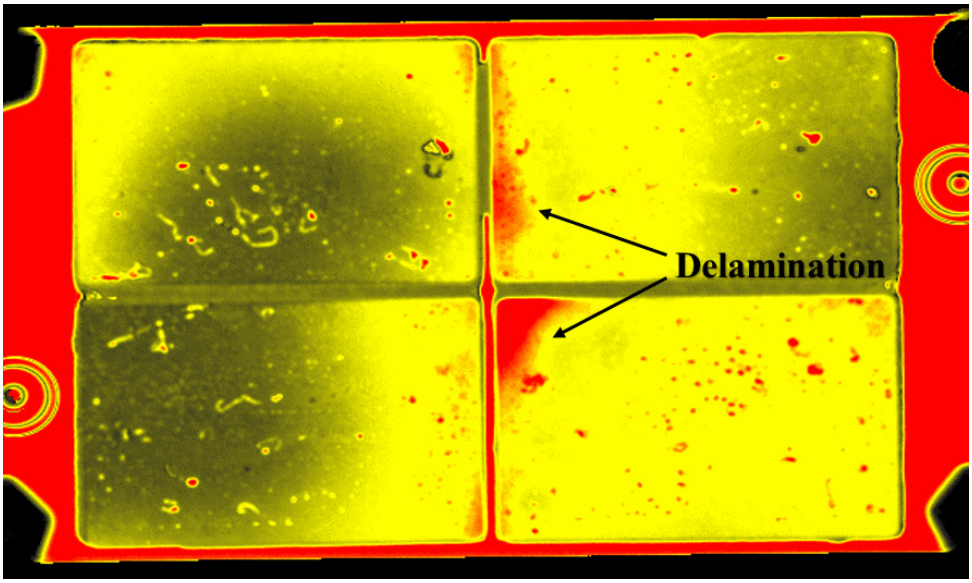
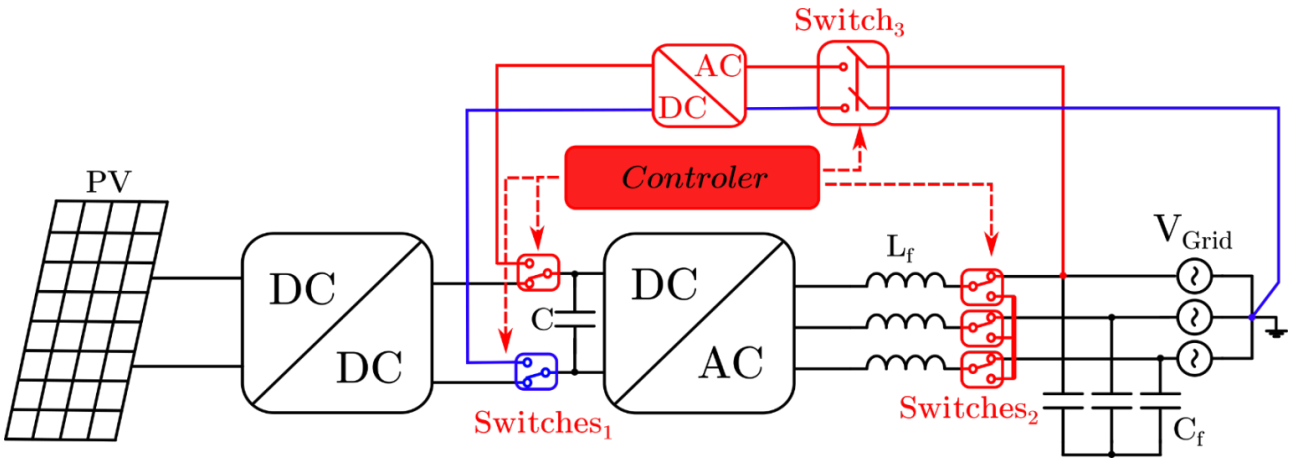


Fig. 6.20: Acoustic microscopy analysis of one IGBT power module

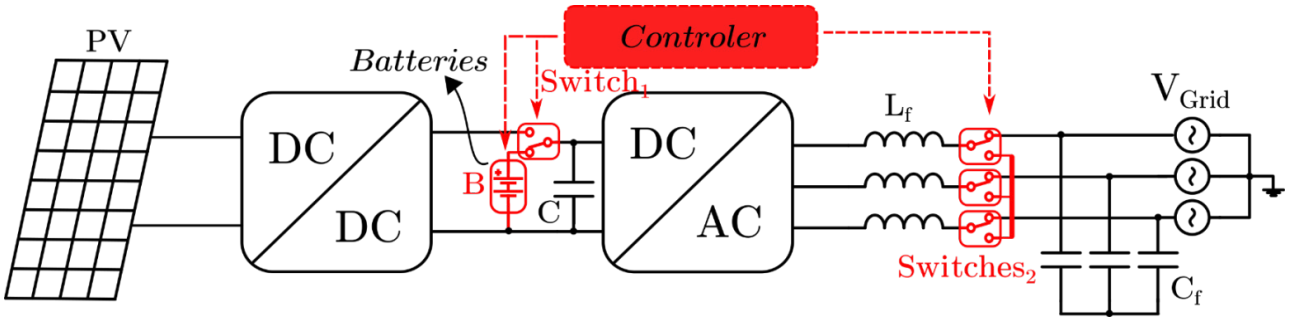
6.6. Implementation in a condition monitoring system of photovoltaic inverters

As it was previously shown, the measurements of the CM setup were validated, where the *B1505A Keysight* Analyzer was used to validate the V_{ce},V_f and r_d's measurements, while Z_{th}'s measurements were validated using the classical method. Then the CM setup was tested successfully in the accelerated ageing test bench, where the failure indicators started to increase during the tests.

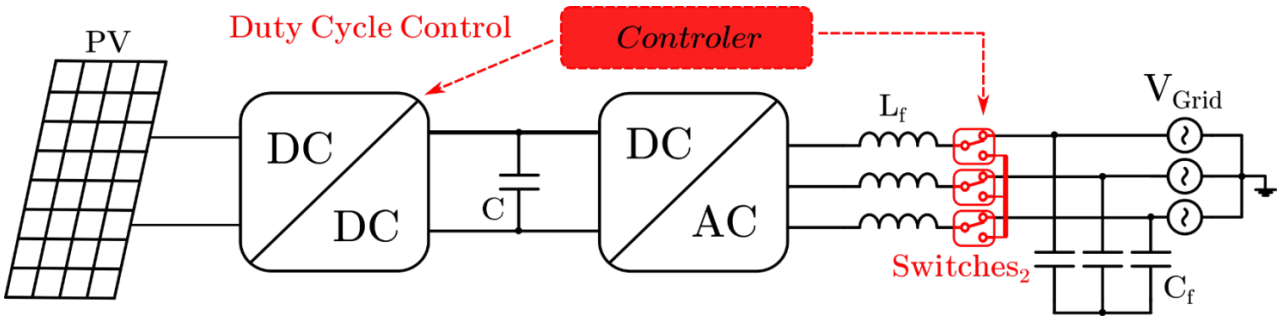
In the future, the in-situ condition monitoring method should be implemented in a condition monitoring system inside a real photovoltaic inverter. However, the diagnostics phase should be done during the non-operation period of the inverter (eventually at night). It would therefore be necessary to determine how the DC-link bus could be supplied. It should be noticed that the power needed to apply the method is only equivalent to the inverter's power losses, during relatively short times (the inverter power losses $\leq 3\%$ of the inverter's input power during operative production). Thus, the energy needed for the condition monitoring system would be negligible when compared to the PV system's produced energy. Hence, three possible solutions are proposed in this study, illustrated in Fig. 6.21 as follows:



a) Using a rectifier



b) Using batteries



c) Using the DC/DC inverter

Fig. 6.21: Different proposed topologies of the photovoltaic inverter's condition monitoring system

184 suggests using a rectifier connected to the grid, to supply the DC-link bus of the photovoltaic inverter. The controller connects and disconnects the switches (Switches 1 and 2), in order to apply the diagnostics cycle during the night. $Switches_2$ are used to disconnect the group of inductances L_f from the grid, and to reconnect them together during the diagnostics phase. According to this solution, the diagnosis phase can be applied every day or every few days.

184 suggests using batteries that can be connected to power the DC-link bus during the diagnostics phase (night), and then recharged during the production phase. According to this solution, the diagnostics phase can be applied every day, or every few days.

Similarly to the other solutions, the one illustrated in 184 proposes to wait for the daylight to produce sufficient energy to power the DC-link bus, using the PV panels. This can be done by controlling the duty cycle of the DC/DC inverter.

The three proposed methods suggest adding some components to the PV system, which may increase the system's both complication and cost. It is clear that the two first methods are more expansive than the last one, where an AC/DC inverter is added to the PV system in the first method, while adding batteries in the second one. However, these methods provide sufficient energy for the CM system whenever time is needed. Nevertheless, the first method cannot be deployed in isolated PV systems since it is dependable on the grid.

On the other hand, the control system of the third method is more complicated than that of the others, since the duty cycle of the DC/DC inverter should be controlled, however this method seems promising since only the switches and the controller are added to the PV system. In the end, all these propositions are only preliminary ideas for future implementations of the in-situ condition monitoring in PV inverters. They have to be designed, validated and carried out in prototypes. Furthermore, the cost of these solutions has to be estimated and compared in order to determine if these solutions could be commercially viable.

6.7. Conclusions

This chapter presented the accelerated ageing test bench for IGBT power modules. Initially, the test bench instrumentation was depicted concerning the power stack, the DC-link power supply, the load inductor design as well as the control system, etc. The accelerated ageing profiles of current and ambient temperature designed in Chapter 4 were applied during two different accelerated ageing tests.

Then, a new method for in-situ condition monitoring of semiconductor devices in PV DC/AC inverters was presented. It consists of measuring the voltage drop across the collector-emitter junction, the dynamic resistance and the thermal impedance of each device.

Afterwards, in order to validate the measurements of V_{ce}, V_f and r_d, they were compared to those obtained by the *B1505A Keysight* Analyzer. Similarly, Z_{th} measurements were compared to those obtained by the classical Z_{th} measurement method. All the comparisons showed very close results, which allowed to validate the in-situ method measurements.

Then, the results of the accelerated ageing test were represented, where the values of V_{ce},V_f, r_d and Z_{th} increased gradually. Moreover, it was noticeable that for same devices and ageing tests, the semiconductors' dynamic resistance showed approximately 4 times more sensitivity to packaging degradation than that of V_{ce} and V_f. Thus, monitoring r_d instead of V_{ce} and V_f could allow for more accurate measurements, and an easier detection of wire bonding lift-off, usually identified by a slight sudden increase of V_{ce} and V_f during the ageing tests. Accordingly, in a photovoltaic inverter these parameters can be used as potential indicators of semiconductors' ageing, a theory that could be validated with supplementary ageing tests.

Using the in-situ method detailed in this chapter, the monitoring can be done without disconnecting the drivers, neither the DC-link capacitors, nor the DC-link bus. Moreover, the condition monitoring is done under the actual DC-link voltage, hence, there is no need for an

independent current source. Now, it is possible to monitor three different failure indicators of IGBT power modules using the in-situ method demonstrated in this chapter.

Consequently, promising prototype solutions for condition monitoring of PV inverter's semiconductors are suggested, while their costs have to be estimated and compared in order to determine if these solutions could be commercially viable.

Conclusion and Perspectives

The initial goal of this study was to develop a new methodology to carry out accelerated ageing of photovoltaic (PV) inverter's semiconductor devices, aiming to better represent the natural ageing process of the power modules in PV inverters, rather than the classical accelerated ageing tests. Given the maturity of Silicon (Si) IGBT technology, as well as the great number of Silicon Carbide (SiC) MOSFET's advantages over this latter, both semiconductor devices were studied. Another aim of this study was also to develop and validate an in-situ condition monitoring (CM) solution for semiconductor devices in photovoltaic inverters.

The methodology presented in this work consisted of analyzing the mission profiles of the current and ambient temperature, extracted over several years from several PV power installations. Therefore, various characteristics of PV application were studied, such as the shape of the inverter's RMS output current, the diffuse current, the current variations' slope, the difference between the seasons, the time delays between the current variations and the ambient temperature.

As a result of this study of PV mission profiles, accelerated ageing profiles of current and ambient temperature were developed in Chapter 4. The purpose of these profiles is to induce, during ageing tests, thermo-mechanical constraints close to those seen by the semiconductor devices in a PV inverter. These tests include simultaneous passive temperature cycling and active power cycling done under switching nominal conditions and pulse width modulation PWM operating mode, in a back-to-back configuration using the opposition method.

In order to design and determine the adequate parameters of the accelerated ageing profiles, the junction temperature T_J of the semiconductor devices corresponding to the mission and accelerated ageing profiles had to be estimated. Accordingly, a power losses estimation model and a thermal model were developed with *Matlab*.

The principle of power losses calculation was depicted in Chapter 2 in the case of both Si IGBT and SiC MOSFET used in a two-level DC/AC PWM inverter. Accordingly, average conduction and switching losses were estimated on a fundamental period T_{out}, by extracting the equations' parameters from the manufacturer's datasheets. This model has been validated using various manufacturers' simulators, and was coupled with the thermal model in order to consider the electro-thermal coupling of temperature-dependent electrical parameters.

However, the switching processes are usually affected by the parasitic connection inductances present in the components and connections, and generated by connecting transistor chips in power modules. Hence, the switching energies were then directly measured using the Double Pulse Test (DPT) with the SiC MOSFET power module, where its body diode showed negligible recovery losses.

Afterwards, a thermal model based on Foster networks was also built and identified to estimate the junction temperature of both Si IGBT and SiC MOSFET power modules, as being represented in Chapter 3. The thermal model had to be fast enough to process mission profiles of more than 800 million samples each.

Hence, six T_J calculation methods were tested and compared. These methods were: time-domain estimation, fast Fourier transform FFT, FFT with overlap-add method, breaking down mission profile into single pulses, and finally an analytical solution. All the methods

have provided the same temperature results which allowed validating them. However, the analytical solution demonstrated the highest performance in term of execution time, mostly with very long mission profiles. Furthermore, it allowed considering the electro-thermal effect every T_{out}, by updating the power losses mission profile at each code iteration. Hence, this method was eventually adopted for the estimation of the junction temperatures, and then the thermal model was validated using various manufacturers' simulators.

Once the accelerated ageing profiles have been designed, they were applied later in real ageing tests. Thus, in order to accurately estimate T_J of the devices corresponding to the accelerated ageing profiles, the self-heating and mutual thermal coupling impedances were directly measured in the case of IGBT and SiC MOSFET devices. These measurements were done using a classical method by measuring a TSEP during the cooling of the DUT, where the obtained mutual thermal coupling impedances were found to be not negligible compared to the self-heating impedances.

Afterwards, two methodologies were adopted to design the current's accelerated ageing profiles. The first one considered all the studied characteristics of the PV mission profiles, and generated maximum current variations. On the other hand, the second methodology considered the same PV characteristics, but regenerated the real current variations extracted from the measured mission profiles, while reducing the delays between them.

Next, the two accelerated ageing methodologies and a classical power cycling example were compared to each other in terms of test duration and distributions of the mean junction temperature T_{J_M} and amplitude ΔT_J of their correspondent extracted cycles. Accordingly, the 1st method showed a compromise between the speed and the good representation of the application, hence, it was selected to be applied in the first place during the accelerated ageing tests.

A first, test bench was built to test SiC MOSFET power modules, in order to identify the potential indicators of ageing/failure and failure mechanisms of SiC MOSFET devices used in PV inverters. Hence, several electrical parameters were monitored during the tests represented in Chapter 5. According to the obtained accelerated ageing results, $R_{DS_{on}}$, I_{DS_S}, I_{GS_S} and $V_{GS_{th}}$ showed the most remarkable increase during the accelerated ageing tests. $R_{DS_{on}}$ of one MOSFET has increased by approximately 22%, which could be explained by wire bonding lift off, a reconstruction of the metallization surface, a decrease in device's thermal performances, and/or a degradation of the die given that $V_{GS_{th}}$ has also increased. However, only one MOSFET has failed, directly after a steep increase in the leakage current of approximately 50000%, while the gate became uncontrollable. The increase in gate leakage current could be caused by carriers tunneling via the gate insulator, leaking between gate and source due to gate's oxide failure. Moreover, the gate threshold voltage has increased showing instability, which could be due to the interfacial charge trapped in the case of SiC-based devices at and near the $SiC-SiO_2$ inversion channel-gate insulator interface

Accordingly, in this type of tests simulating the PV application, the results showed that SiC MOSFET gate's oxide could fail before the packaging, which leads to think that IGBTs are more reliable than SiC MOSFETs used in PV application. However, this is not certain since the damage could be due to semiconductor device overheating, which couldn't be verified as the thermal impedance was not monitored due to time constraints. Given the results represented above, these parameters could be considered as potential ageing indicators of SiC MOSFET devices in photovoltaic inverters.

This work will be pursued by further investigations of failure mechanisms with Scanning Acoustic Microscopy (SAM) analysis and/or Scanning Electron Microscopy (SEM) analysis. However, the main purpose of this study was to apply the tests in a real test bench for a preliminary check. The diagnostics phase has to be automated in the future, and a measurement setup of the junction temperature and the thermal impedance have to be added to the test bench.

Moreover, a campaign of tests has to be executed in the future on the same device type as well as on others to check if similar results could be obtained. Furthermore, the parameters of the accelerated ageing profiles could be modified to test the impact of each parameter on the obtained failure mechanisms and indicators. Moreover, it could be interesting to also apply the second methodology, in order to compare its results with those obtained with the 1st methodology. In addition, it could be interesting to readjust these methodologies so that the devices are kept at peak temperature while eliminating the temperature swings. Accordingly, it would be possible to check if the temperature swings accelerate more the ageing of SiC MOSFET, than by keeping them at peak temperature.

These tests have demonstrated comparable duration to that of a classical power cycling, while they are expected to show more representative results, leading to reduce the favoring of certain failure modes to the detriment of others. Therefore, it would be of high interest to apply classical power cycling to the same devices to compare the obtained indicators variations and failure mechanisms. This type of test could be used to reveal the weak points of the power modules used in photovoltaic inverters and thus lead to improve the production processes. However, the results should be ideally compared to feedbacks from PV installations, when these are available.

A 2nd accelerated ageing test bench was dedicated to test initially, on IGBT power modules, a new solution for in-situ condition monitoring of semiconductor devices in PV inverters, as being demonstrated in Chapter 6. It consisted of measuring the voltage drop across the collector-emitter junction V_{ce}, the dynamic resistance r_d and the thermal impedance Z_{th} of each device. Due to technical problems and time constraints, the accelerated ageing tests were stopped earlier before the devices' failure; however the methodology was tested and validated with classical measurements.

Considering the accelerated ageing test results, it was noticeable that for the same devices and ageing tests, the semiconductors' dynamic resistance showed approximately 4 times more sensitivity to packaging degradation than of V_{ce} and V_f. Thus monitoring r_d instead of V_{ce} and V_f could allow for more accurate measurements, and an easier detection of wire bonding lift off, usually identified by a slight sudden increase of V_{ce} and V_f during the ageing tests. Accordingly, in a PV inverter these parameters can be potentially used as indicators of semiconductors' ageing, a theory that could be validated with more ageing tests.

By using this in-situ methodology, the monitoring can be done without disconnecting the drivers, neither the DC-link capacitors, nor the DC-link bus. Moreover, the condition monitoring is done under the actual DC-link voltage; hence, there is no need for an independent current source. Consequently, promising prototype solutions for condition monitoring of PV inverters' semiconductors were suggested, while their costs have to be estimated and compared in order to determine if these solutions could be commercially viable. Indeed, the deployment of these solutions into the PV system could be expensive, therefore the CM methodology would have to be readjusted and optimized to be integrated in the PV system without adding further components.

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