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Abhijeet Dasgupta

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High Efficiency S-Band Vector Power Modulator Design using GaN Technology

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"You cannot teach a man anything; you can only help him discover it in himself"

Galileo Galilei

To the young minds of India,
To my Grandmother,
To my Parents,

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No one who achieves success does so without acknowledging the help of others. The wise and confident acknowledge this help with gratitude.

Alfred North Whitehead

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General Introduction

The process of communication has always been an integral part of the human society. The present era is dedicated to the evolution of modern communications (HDTV's, satellite communications etc) and information processing technologies which has also made human life pleasant and lot more easier. The need for human beings to continuously process information and communicate effectively over remote distances has tremendously led to the boost of mobile telecommunications and wireless industries leading to the rise of sophisticated communication standards over the years starting from GSM in the early 90's up to present research in LTE and beyond for 5G technologies. Due to the never ending demands of the subscribers for frequency flexibility, portability and above all greater wireless connectivity between devices, various communication standards and protocols and services beyond machine-machine learning has led to exponential increase of popularity for personal communications, internet and, recently, the so-called "Internet-of-Things (IoT's)" which is affecting human lives one way or the another.

The processing and transmission of such complex protocols, standards and constantly evolving signal schemes has imposed stringent requirements before the designers to address these issues and make innovative and efficient approaches towards transmitter architectures in terms of signal integrity, bandwidth and above all without compromising the performances in terms of power consumption and signal quality. In this regard, over a decade ago, there was a significant breakthrough in solid state RF power devices based on compound semiconductor technology such as SiC and GaN. Among the various available technologies, GaN because of its high power handling capabilities along with frequency flexibility and higher breakdown voltage has emerged as a very promising candidate for a wide variety of high power transmitter architectures. Several space industries and foundries such as Qorvo, Wolfspeed, Mitsubishi, Nitronex, NXP and UMS among others are constantly maturing in terms of improving the performances of such technologies to make it more viable for various commercial and defence related applications.

One of the most important part of any power transmitter is the RF power amplifier which suffers from the issues arising from the trade-offs between linearity, bandwidth and above all the DC power consumption. The main objective of this thesis work lies in the analysis of technical approaches that make use of signal conditioning and signal controlled power amplification to improve energy efficiency and flexibility of communication transmitters. To achieve this objective, a specific laboratory test bench developed in XLIM laboratory, University of Limoges has been used. Two new two-stage GaN based architectures have been proposed, design and presented that works on the principle of Saturated Variable Gain (SVG) using supply modulation technique. A new biasing architecture to improve bandwidth performances has also been presented as a part of this thesis work.

This thesis is divided into the following four chapters:

The **First chapter** highlights various design issues, challenges and Figures of Merit (FOM's) of communication transmitters. It also presents various potentialities of the GaN transistors used in the design procedure in this thesis and the simplified illustration of the transistor current source and its analysis and impact on communication transmitter design.

The **Second chapter** illustrates the properties of modern complex modulated signals with high PAPR and comments on various advanced transmitter architectures for their efficient amplification. This chapter also explains the limitations of conventional transmitter architectures based on supply modulation technique for the generation of high PAPR power waves and proposes an improvement on such architectures necessary for high power wave generation.

The **Third chapter** presents the design procedure of an high efficiency Vector Power Modulator (VPM) circuit and its simulated and measured performance analysis comparison. In this chapter, the designed circuit and its association with a high speed and efficient supply modulator has also been highlighted and the principle of Saturated Variable Gain (SVG) has been demonstrated.

The **Final chapter** proposes a new biasing architecture and an improved VPM version with investigations on bandwidth enhancement capabilities.

Finally, a general conclusion along with some interesting future perspectives for the extension of this work has been highlighted at the end of this thesis.

Chapter I

Challenges and Design Considerations in GaN based RF Power Generation

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1 General Context of RF Power Transmitters

1.1 General Requirements for Modern RF Transmitters

A general representation of an RF Power Transmitter chain is illustrated in fig. I.1.

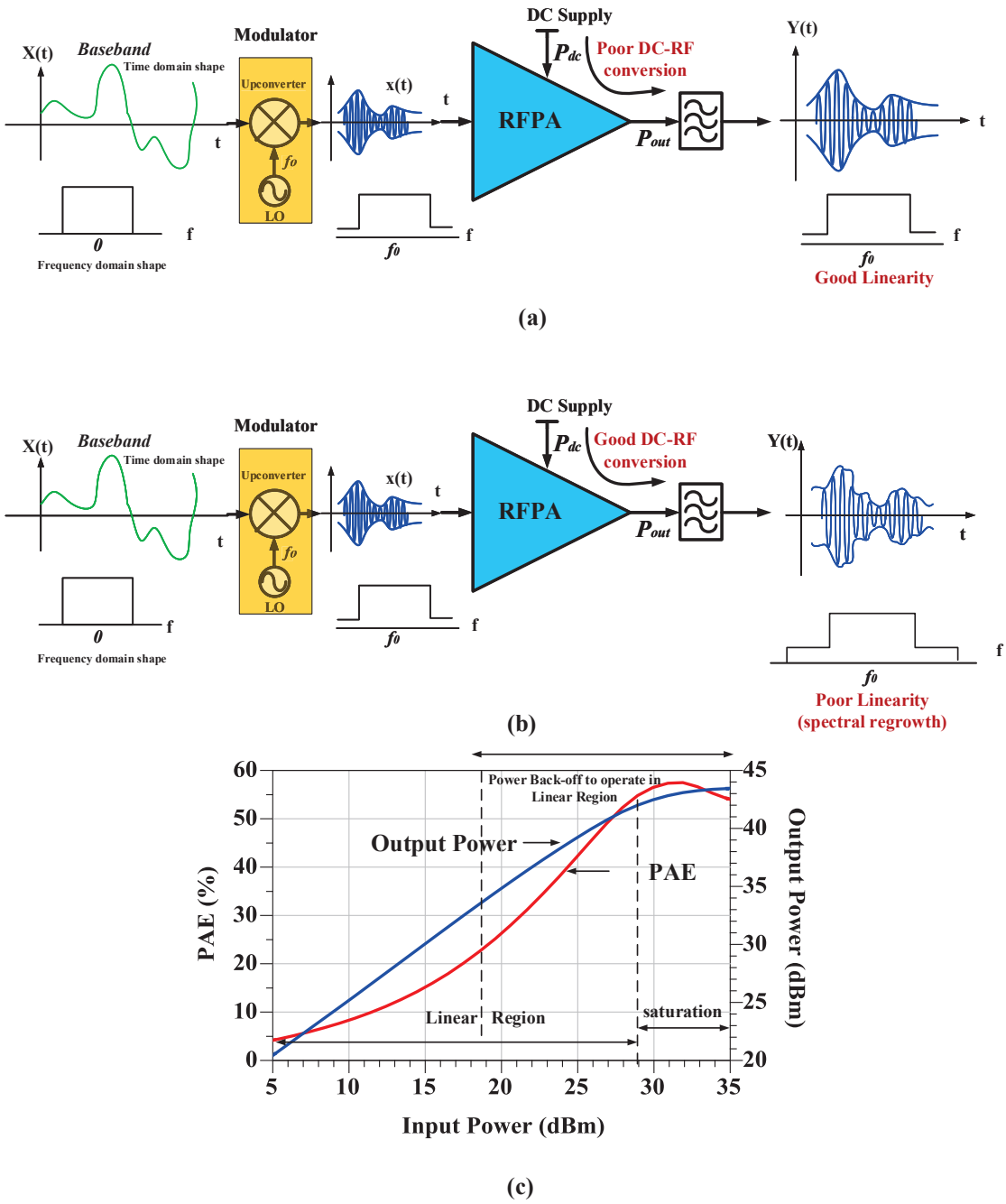

Figure I.1: General Architecture of an RF Power Transmitter Chain (a) Linear case (b) Non-linear case and (c) General power characteristics of an RFPA

The continuous evolution of communication transmitter systems has always been governed by the increase in the complexity of communication signals (from constant-envelope to non-constant envelope signals) starting from GSM (2-G systems) in the beginning upto LTE (4-G systems) currently and beyond (5-G systems).

This has led to the investigations and development of spectral efficient complex modulation techniques like n-QAM. Such modulation techniques lead to non-constant envelope signals having large Peak to Average Power Ratio (PAPR). This main characteristic is the cause of higher sensitivity to different sources of distortions and more power consumption.

To maintain the signal integrity, conventional power amplifiers, PA (which are the most power consuming in a transmitter) are generally operated at power back-off levels which leads to poor average efficiency (case of fig. I.1 (a)). This implies that modern PAs must be specially designed for high PAPR signals for providing efficient operation at average power levels [1]. If power amplifiers operate in their saturation region to improve PAE performances (case of fig. I.1 (a)). Then the signal reaches its peak power and the non-linear behaviour of the RFPA leads to spectral regrowth and poor linearity performances. Basically a digital predistortion technique must be implemented to meet the linearity requirements. This has also forced the designers to put forward a cost-effective, reliable, portable and light weight equipment for efficient transmission with main focus on the compactness of the different analog segments, power and frequency flexibility, and minimizing the energy consumed under the stringent constraint of acceptable signal integrity (linearity).

The compactness and ease of integrating complex modulation and energy conversion functions and their co-design within the transmitting part of a communication system is the principle idea on which the development of this thesis is focused.

This idea is furthermore associated with three fundamental parameters that have to be accommodated as far as the designing aspect is concerned:

Efficient DC-RF energy conversion at average power levels over wide frequency bandwidth maintaining an acceptable amount of signal linearity with minimum DC power consumption for complex modulated signals.

The flexibility of a transmitter implies a relatively wide band functional operation to address multi-standard or multi-function applications. It induces the need to jointly take into account various functions such as amplification, filtering and signal conditioning for

the design of the RF power generation function at the transmitter.

Miniaturization in the presence of high power levels (of the order of ten watts) induces an essential factor which is the power density of active devices and the increase in operating frequencies. Furthermore, wideband functions are required instead of multi-channel bands.

With extensive research over past few years, Gallium Nitride (GaN-HEMT) technology has emerged as a potential candidate for high frequency and high power applications because of numerous advantages over its existing counterparts such as Si-LDMOS like high power density, higher breakdown voltage. GaN technology is more attractive for wideband power amplifier design and can result in smaller circuits or design sizes for the same amount of output power.

In this general context, this chapter highlights the description and basic considerations in RF power generation process employing GaN devices suitable for RF power transmitters. The chapter also highlights the main characteristics and performance criteria of power transistors and power amplifiers. The issue of the trade-off between various figures of merit has also been addressed.

Finally, the chapter is concluded with the addressing of the main characteristics of GaN technology suitable for high efficiency and high power amplifier design.

1.2 Microwave Power Transmitter Architecture

Fig. II.2 illustrates a basic block diagram of an RF power transmitter.

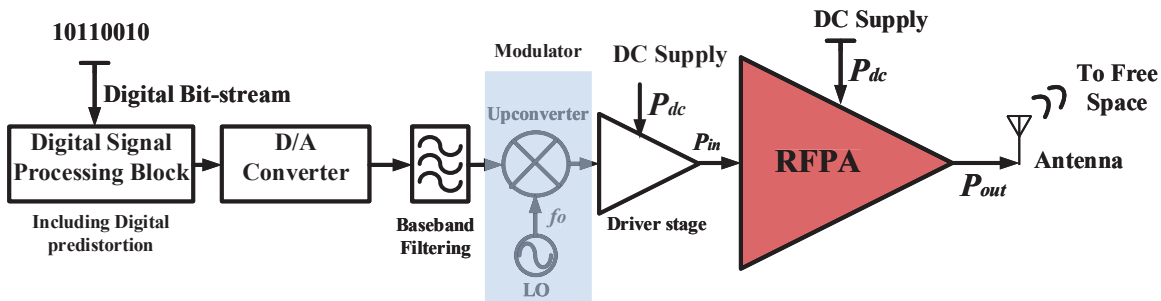

Figure I.2: General Architecture of RF Power Transmitter Chain

In the overall transmission chain, the RF power amplifier (RFPA) is the main source of DC power consumption. Any power amplifier converts the DC power supplied into output RF signal power. An ideal RF Power Amplifier can hence be defined as a transducer that converts DC power to useful RF power under the influence of an RF input signal. Traditionally, the design of power amplifiers predominantly focuses on the main power stage and the gain requirement is usually met by adding linear gain elements (drivers) before the amplifier (Fig. II.2). These driving stages are made linear in order to maintain the overall linearity of the power amplifier [2].

Concerning the RF power amplifier, if efficiency is not optimized, a great amount of DC consumption is dissipated into heat and thermal management of the system is more complex along with a significant increase in the cost of products.

Good efficiency is obtained when transistors operate at saturation which is prejudicial for linearity. A trade-off always exists between power efficiency performances and linearity when power back-off is applied. However, the most challenging aspect today is to propose solutions that enables the optimization of both efficiency and linearity rather than to find acceptable trade-offs. Moreover, PA operating over wide frequency bandwidths are required. All that makes PA design a major challenge in RF transmitter chain.

1.3 Issues and challenges in RF Power Amplifiers

1.3.1 Basic Architecture of an RF Power Amplifier

Fig. I.3 shows the general block diagram of an RF power amplifier (RFPA) along with a simplified non-linear equivalent model of the active device, the transistor, which acts as an ideal voltage controlled current source. The transistor here is considered to be an unilateral device. The input circuit is assumed to be linear (R_{in}, C_{in}). Output capacitance C_{out} is also assumed to be constant. The unique but fundamental non-linearity is the drain current source, I_{ds}. The matching networks at the input and output of the transistor are necessary to ensure the maximum transfer of power from source to the load. The bias networks are used to provide the proper DC operating conditions to the transistor. Additionally, some passive components connected in the input matching and biasing network might also be necessary to satisfy the electrical stability of the RF power amplifier.

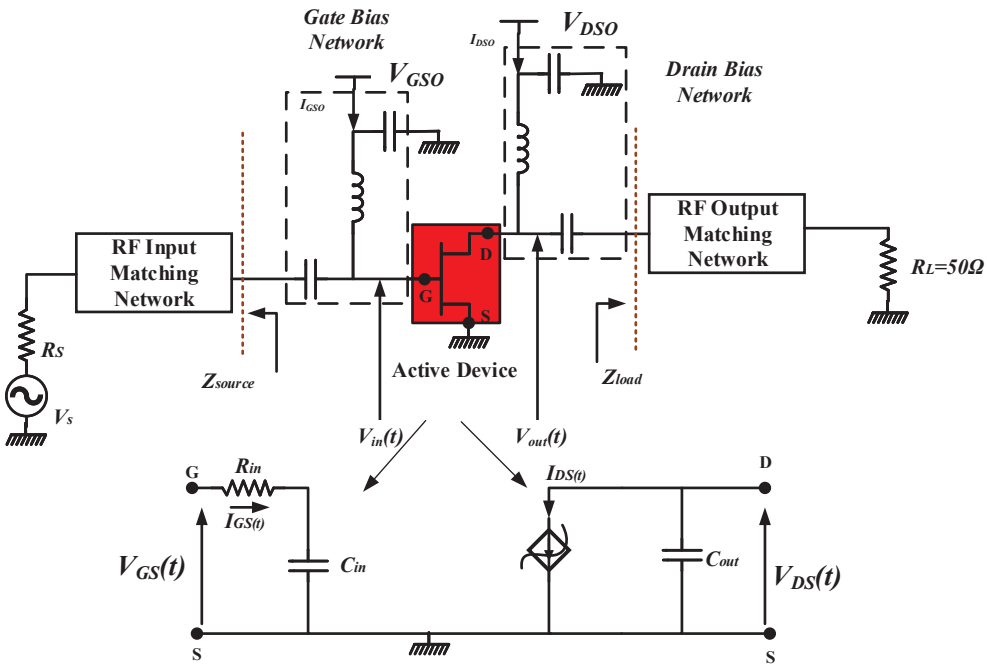

Figure I.3: Block Diagram of RF power amplifier and simplified model of the transistor

The nonlinear behavior of any circuit is relatively complex to analyze theoretically and it is difficult to use analytical functions to characterize its nature. Therefore a simplified approach based on piecewise linear approximations is used and simplifies the analytic approach to deduce the basic behavior of the device. The assumptions that are considered for a simplified approach towards the analysis of the amplifier can be illustrated by the simplified piecewise-linear DC-IV characteristics of a power transistor as shown in Fig. II.4. V_p is the pinch-off voltage which is the minimum voltage below which the transistor is in off state.

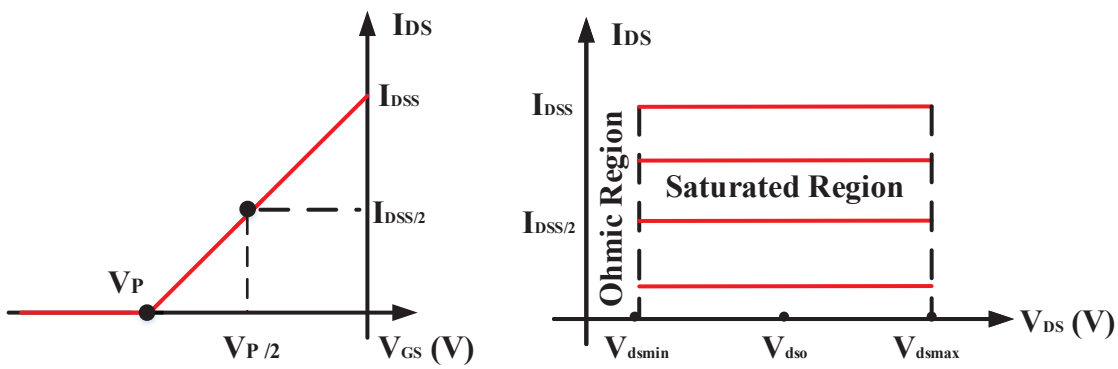

Figure I.4: Static piecewise-linear DC-IV characteistics of a simplified power transistor model

The static IV characteristics of a transistor can be represented as straight lines. This technique based on the linear piecewise approximation of the device transfer function provides a clear insight into the basic behaviour of power amplifier and its operating modes. Following the piecewise linear approximation, let us define the following parameters and signal expressions:

The saturated region (used for amplification function) is limited by the ohmic region (V_{dsmin}) and the breakdown voltage, V_{dsmax}. I_{ds} versus V_{ds} curves for different values of V_{gs} approximately have a slope equal to zero which assumes that the self heating effects are not taken into account. Increasing the V_{gs} values leads to a linear increase in the drain current I_{ds} which is considered as independent of V_{ds} and is a linear function for $V_{gs} > V_p$ and is null for $V_{gs} < V_p$.

The maximum output voltage swing of the transistor is limited between V_{dsmin} and V_{dsmax}. That is

$$V_{DSmin} \leq V_{DS}(t) \leq V_{DSmax} \tag{I.1}$$

$$I_{DS} = 0 \quad \text{when} \quad V_{GS} < V_P \tag{I.2}$$

and

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{when} \quad V_P < V_{GS} < 0 \tag{I.3}$$

Fig. II.5 shows the transistor configuration with the load and the biasing networks. The input sinusoidal voltage waveform V_{gs1} cos (ωt) is applied at the gate terminal once the proper gate biasing voltage V_{gso} has been established.

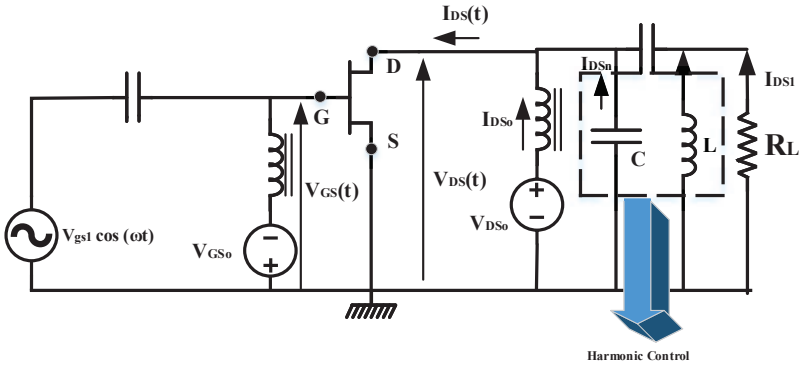

Figure I.5: Representation of different current flow within a simplified amplifier model

$$V_{gs}(t) = V_{gso} + V_{gs1} cos\omega t \tag{I.4}$$

and

$$I_{gs}(t) = I_{gso} + I_{gs1} cos(\omega t + \xi) \tag{I.5}$$

where $I_{gso} \cong 0$ and $\xi \simeq \pi$ / 2 due to the capacitive behaviour at the gate port.

The ideal load network of a transistor is assumed to behave as an ideal parallel resonating network including C_{out} at the fundamental frequency. In this condition, the intrinsic load seen by drain current generator is purely real and the harmonic components of currents are ideally terminated into a short circuit. Hence the representation of intrinsic time domain drain voltage can be expressed mathematically as follows :

$$V_{ds}(t) = V_{dso} - V_{ds1} cos\omega t \tag{I.6}$$

where $V_{ds1} = R_L I_{ds1}$

And the generalized output current is represented by the following equations :

$$I_{ds}(t) = I_{dso} + \sum_{n=1}^{\infty} I_{dsn} \cos(n\omega t) \tag{I.7}$$

where n denotes the number of harmonics.

This general analysis will lead to the definition of a very important term known as the conduction angle which is illustrated in fig. I.6 for an example of Class-AB amplifier.

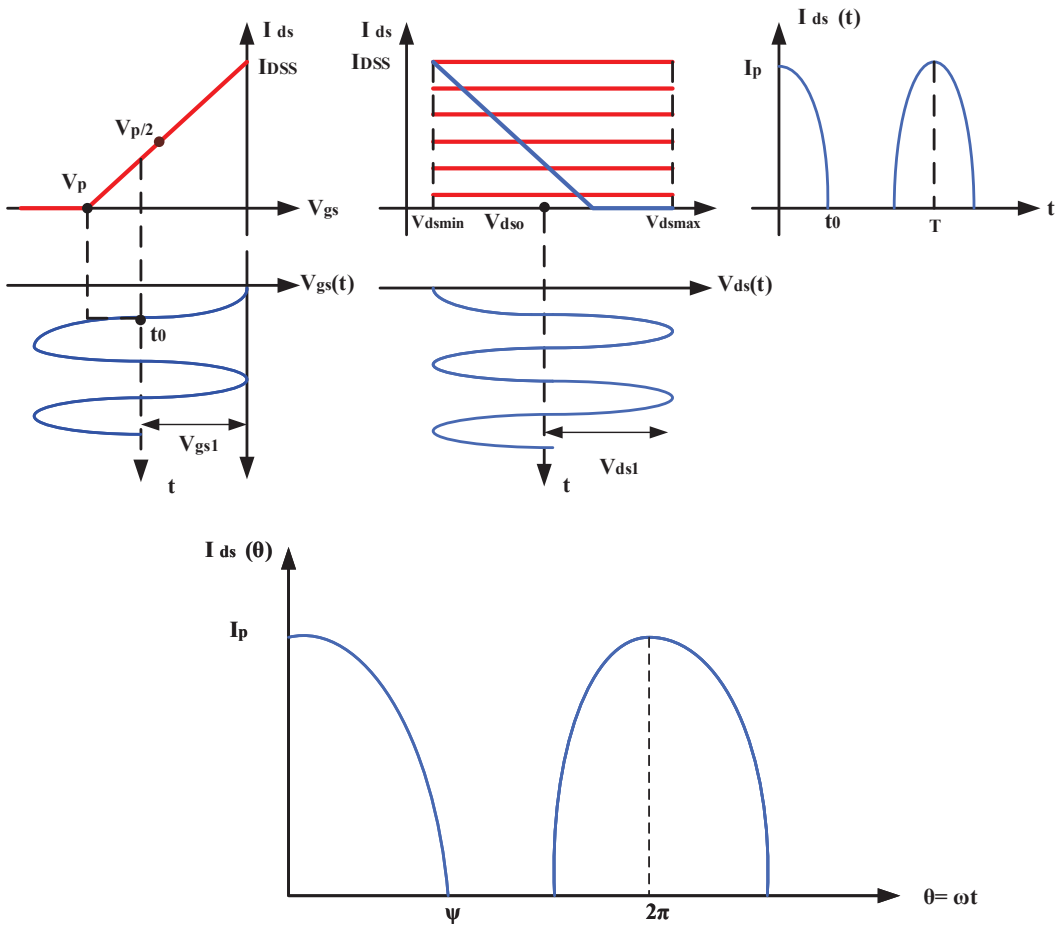

Figure I.6: Illustration of the conduction angle phenomenon from simplified voltage-current characteristics of a power transistor, $I_P = I_{DSS}$ and $V_{GSmax} = 0$

I_p is the peak value of the drain current waveform shown in fig. I.6 and needs to be equal to I_{dss} for maximum output power performances.

Using a variable change, $\theta = \omega t$, we get $V_{gs}(\theta) = V_{gso} + V_{gs1}\cos\theta$

At a certain time instant $t = t_0$, $V_{gs}(t) = V_p$, therefore,

$$V_p = V_{gso} + V_{gs1}\cos(\omega t_0) \tag{I.8}$$

The term ωt_0 is known as the conduction or the aperture angle ψ. Hence from the above equation, it can be deduced that

$$V_p = V_{gso} + V_{gs1} cos\psi \tag{I.9}$$

The above equation can be re-written as

$$\psi = \arccos\left(\frac{V_p - V_{gso}}{V_{gs1}}\right) \tag{I.10}$$

And hence the overall output current equation in terms of θ can be written as follows:

$$I_{ds}(\theta) = \frac{I_{dss}}{-V_p}(V_{gso} + V_{gs1}cos(\theta) - V_p) \tag{I.11}$$

which can be written as

$$I_{ds}(\theta) = \frac{I_{dss}}{-V_p}V_{gs1}(cos(\theta) - cos(\psi)) \tag{I.12}$$

for $V_p \leq V_{gs}(t) \leq 0$

And $I_{ds}(\theta) = 0$, for $V_{gs} < V_p$.

For $\theta = 0$, $I_{ds}(\theta) = I_p$, and $\cos\theta = 1$ therefore,

$$I_p = \frac{I_{dss}}{-V_p}V_{gs1}(1 - cos(\psi)) \tag{I.13}$$

Substituting the value of $\frac{I_{dss}}{-V_p}V_{gs1}$ in equation of $I_{ds}(\theta)$ above, we get,

$$I_{ds}(\theta) = \frac{I_p}{1 - cos(\psi)}(cos(\theta) - cos(\psi)) \tag{I.14}$$

The DC and the fundamental component of drain current can be obtained by integrating the above equation over a period of 2π.

$$I_{dso} = \frac{1}{2\pi}\int_0^{2\pi} \frac{I_p}{1 - cos(\psi)}(cos(\theta) - cos(\psi)) \quad d\theta \tag{I.15}$$

and

$$I_{ds1} = \frac{1}{\pi}\int_0^{2\pi} \frac{I_p}{1 - cos(\psi)}(cos(\theta) - cos(\psi))cos\theta \quad d\theta \tag{I.16}$$

Solving above two equations using well defined relations of Fourier series, we get

$$I_{dso} = \frac{I_p}{\pi}\frac{sin(\psi) - \psi cos(\psi)}{1 - cos(\psi)} \tag{I.17}$$

$$I_{ds1} = \frac{I_p}{\pi}\frac{\psi - sin(\psi)cos(\psi)}{1 - cos(\psi)} \tag{I.18}$$

The above two equations for the fundamental component of the output current (I_{ds1}) and the DC component of the current (I_{dso}) hold very important and form the basis for estimation of various performances of the RF Power Amplifier like the output power, DC power and drain efficiency. For higher (n^{th}) order harmonics we have the following equation :

$$I_{dsn} = \frac{2}{n\pi}\frac{cos(\psi) - sin(n\psi) - nsin(\psi)cos(n\psi)}{(1 - cos(\psi))(n^2 - 1)} \tag{I.19}$$

Fig. I.7 illustrates the classification of RFPA classes as a function of conduction angle ψ and the current amplitudes of the fundamental and harmonics respectively normalized for $I_p = 1$ A.

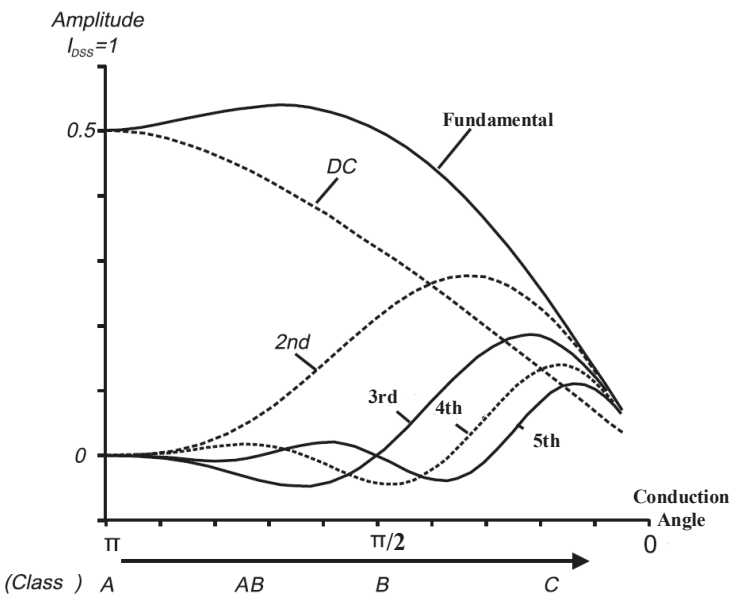

Figure I.7: Illustration of the conduction angle phenomenon from simplified voltage-current characteristics of a power transistor.

Next are few very important terms associated with an RFPA performances namely

the input and output powers respectively. The mathematical expressions of the input and output powers are given as follows:

$$P_{in}(Watts) = \frac{1}{2}\Re(V_{gs1}.I^*_{gs1}) \tag{I.20}$$

where $\Re$ denotes the real part.

$$P_{out}(Watts) = \frac{1}{2}\Re(V_{ds1}.I^*_{ds1}) \tag{I.21}$$

$$P_{DC}(W) = (V_{dso}.I_{dso}) \tag{I.22}$$

$$G_p = \frac{P_{out}}{P_{in}} \tag{I.23}$$

is called the power gain and drain efficiency, η_D is expressed as

$$\eta_D = \left(\frac{P_{out}}{P_{DC}}\right) \tag{I.24}$$

The next two subsections of this chapter highlight general design considerations and figures of merit (FOM) and classification of power amplifiers.

1.3.2 General Design Considerations and Figures of Merit (FoM)

Different properties of the RF power amplifier are crucial for suitability to different applications. For instance, high efficiency is important for increased battery life. Increased efficiency in the base station PA will directly decrease the power dissipation, reducing the need for cooling.

On the other hand, output power might be equally important for applications which rely on long range transmission in noisy environment. Another challenging design aspect for PAs is to get acceptable linearity performances with high PAE.

Based on different applications and design requirements, following are the important FOM for any power amplifier:

1.3.2.1 Power Characteristics and Power Budget Power Added Efficiency (PAE) can be considered as the most important performance criterion for an RF power amplifier. PAE is defined mathematically by the following equation:

$$PAE(\%) = \frac{P_{out}(W) - P_{in}(W)}{P_{DC}(W)}.100 \tag{I.25}$$

Let us consider again the I/V characteristics of a transistor to simply illustrate the optimum operating conditions for maximum Power Added Efficiency and maximum output power as shown in fig. I.8 :

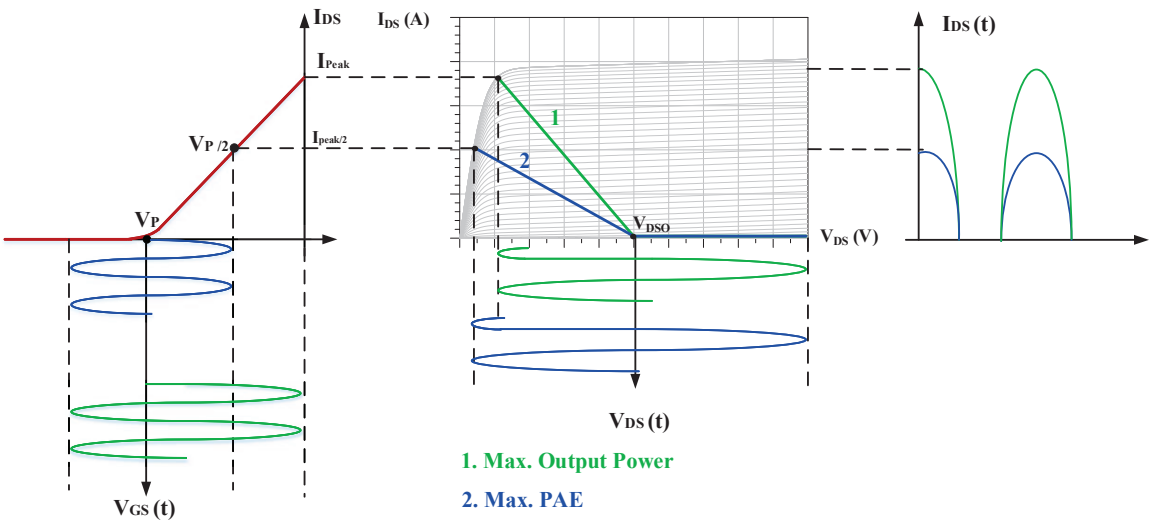

Figure I.8: Transistor loadline illustration for maximum PAE (in blue) and output power (in green).

Assuming again that the harmonic components at the input and output are ideally terminated into short circuit, Power Added Efficiency (PAE) is defined by equation III.34 as far as we assume a purely real load impedance at the intrinsic level of the drain current source:

$$PAE = \frac{1}{2}\left(\frac{V_{ds1}.I_{ds1} - \Re[V_{gs1}.I^*_{gs1}]}{V_{dso}.I_{dso}}\right) \tag{I.26}$$

Considering firstly $P_{in} << P_{out}$ and $V_{gso} = V_p$ which is in the appropriate region of

fig. I.8 (class-B), the time domain waveforms of the drain current is a half sine wave.

In this case when the input gate to source voltage varies, the peak current I_P varies simultaneously but the ratio $\frac{I_{ds1}}{I_{dso}} = \frac{I_P/2}{I_P/\pi} = \frac{\pi}{2}$ remains constant. So, PAE $= \frac{1}{2}\left(\frac{V_{dS1}.I_{dS1}}{V_{dso}.I_{dso}}\right)$. Given a fixed drain bias voltage V_{dso} , PAE will be maximum if V_{ds1} is maximum. The corresponding slope of the loadline illustrating this condition corresponds to the blue curve in fig. I.8. The maximum theoretical efficiency is then 78.5% that is $\pi/4$, if V_{dsmin} would be zero and hence $V_{ds1} = V_{dso}$. The output power on the other hand is maximized, if the product $(V_{ds1}.I_{ds1})$ is maximized, illustrated in fig. I.8 by the green curve.

Power gain is another crucial criterion that evaluates the performance of an amplifier in terms of it's linearity. To get a flat shape of power gain as a function of input power, the quiescent bias point is chosen a little bit above the pinch-off voltage as illustrated in fig. I.9.

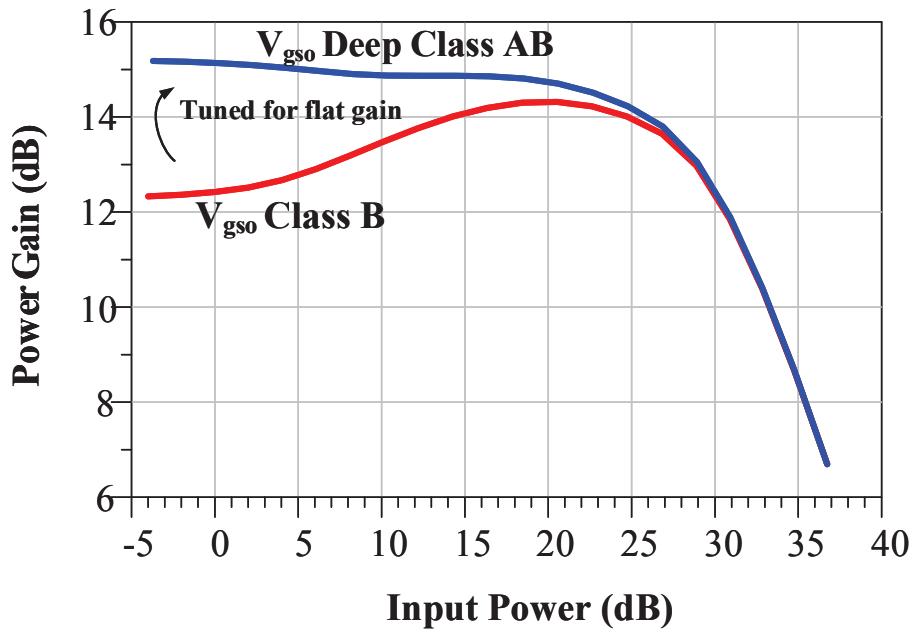

Figure I.9: Gain characteristics of a conventional RF power amplifier

Finally, we get the overall power characteristics of a conventional RF power amplifier at center frequency as illustrated in fig. I.10.

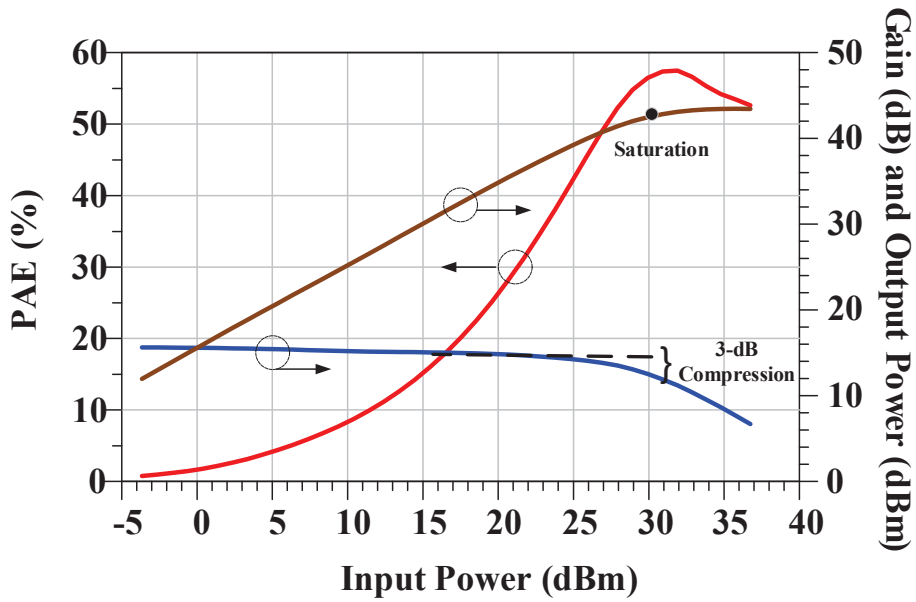

Figure I.10: Power characteristics of a conventional GaN based RF power amplifier

As the input power is increased further beyond a certain point called saturation point V_{ds1} is limited to (V_{dso} - V_{dsmin}) and the power characteristics no longer increases and they remain constant. Once the input power is increased beyond the active device voltage and current handling capabilities, that is limitation of V_{ds} by ohmic region, the power added efficiency (PAE) tend to fall gradually.

1-dB gain compression point is the first indication of non-linearity before the device is driven into hard-saturation. However, this value is very small in case of high power GaN technology, therefore for industrial design purposes, 3-dB compression point is an appropriate figure of merit for linearity/efficiency classification in GaN devices.

It can also be observed from Fig. I.10 that the efficiency of the amplifier is at its peak only in saturation where the device is under the influence of severe distortion thereby affecting the signal integrity or linearity. This leads to the conclusion that there is always a trade-off between linearity and energy consumption of an amplifier which further poses challenges to the designers to mitigate both the causes and establish a suitable compromise between the performances. Several techniques have been implemented to attempt to obtain both optimized linearity and efficiency by changing the transmitter architectures as presented in Chapter-II.

Fig. I.11 shows the power flow diagram for a typical RF Power Amplifier.

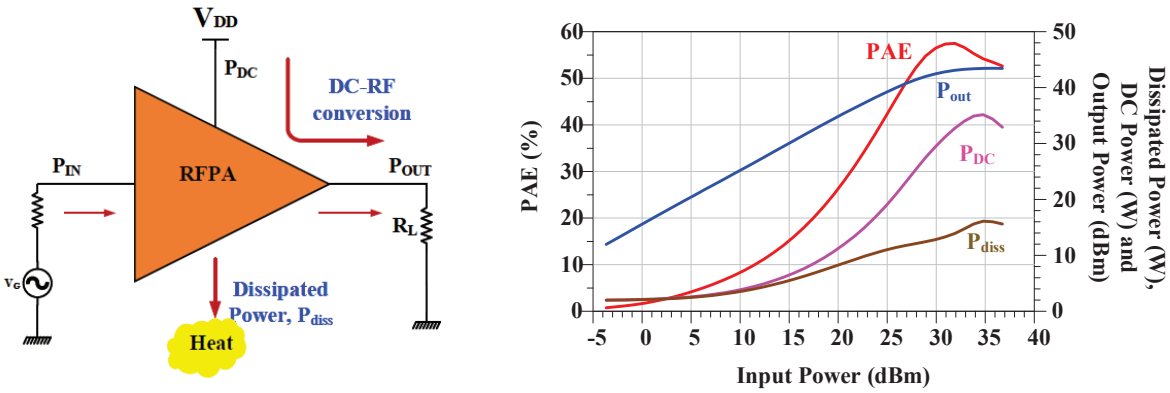

Figure I.11: Power Budget Analysis

The power flow relation is expressed mathematically as :

$$P_{in}(W) + P_{DC}(W) = P_{out}(W) + P_{diss}(W) \tag{I.27}$$

In order to accomplish high efficiency the power amplifier must be driven into non-linear region and be subject to gain compression. This will generate harmonics of higher order which can be exploited to enhance efficiency performances.

Fig. I.12 shows the effect on the overall power characteristics and hence the performances of an RFPA in simulations when the second harmonic is properly terminated.

Fig. I.12 (a) illustrates an example of the ideal (favourable) and the worst case regions of the location of second harmonic impedance and consequent intrinsic drain voltage and current waveforms in both conditions (Fig. I.12 (b) and (c)). As the effect of proper load termination of the second harmonic leads to the reduction of overlapping area under the voltage and current waveforms, consequently, it minimizes the dissipated power. Hence it results in lower DC power consumption and enhancement of PAE as illustrated in Fig. I.12 (d) and (e) respectively.

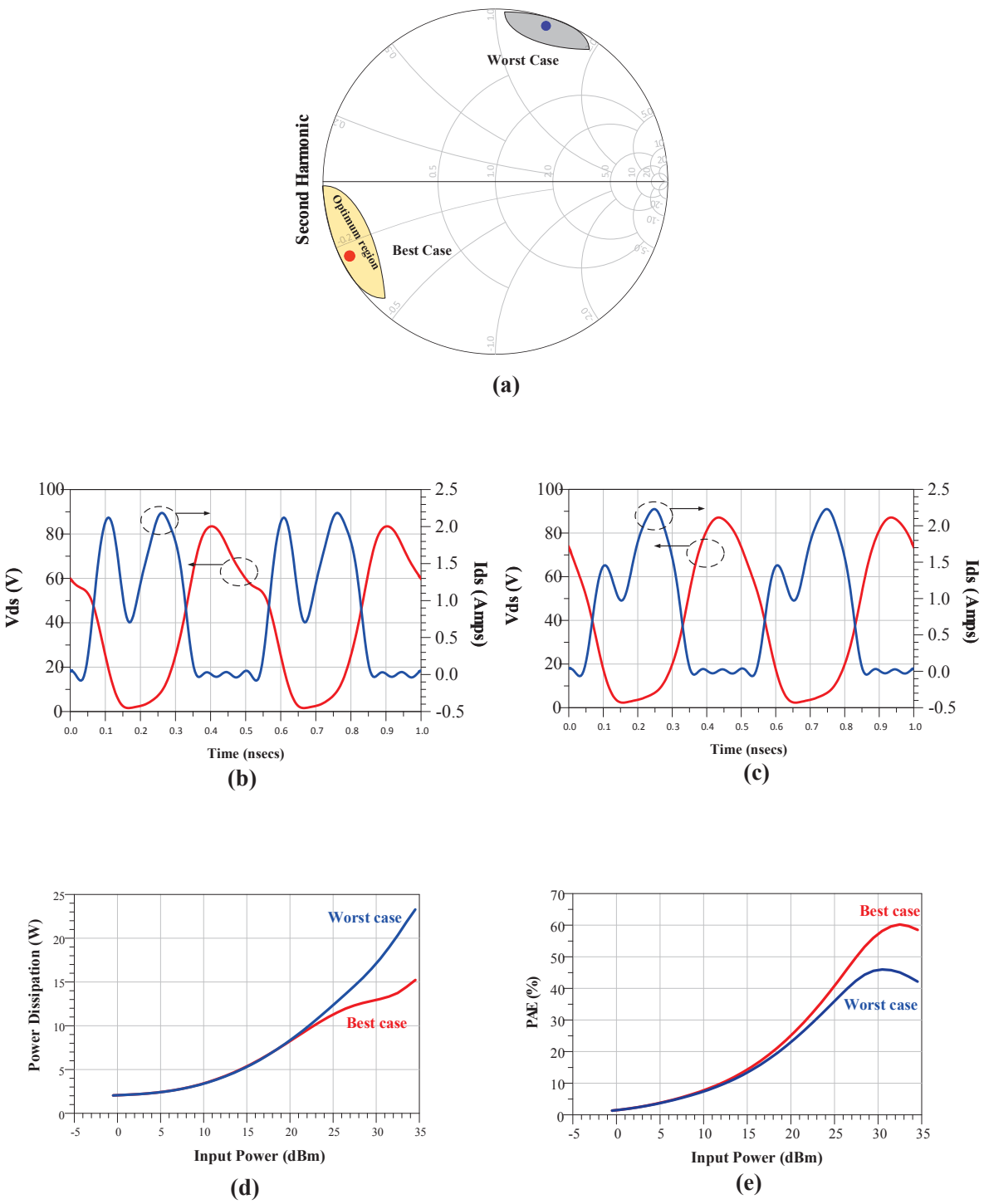

Figure I.12: Performance illustration for worst and best case load termination of second harmonic (a) Worst and ideal regions of second harmonic load impedance (b) Intrinsic drain voltage and current waveforms in worst case (c) Intrinsic drain voltage and current waveforms in best case (d) Power dissipation comparison between best and worst case and (e) Efficiency comparison between best and worst case.

1.3.2.2 Linearity Criteria One of the most common feature is the generation of intermodulation distortion (IMD) products which arise when there are more than one RF tone in the input spectrum. Basically, the first qualification of the linearity degree of an RFPA is ahieved by using a two-tone input signal.

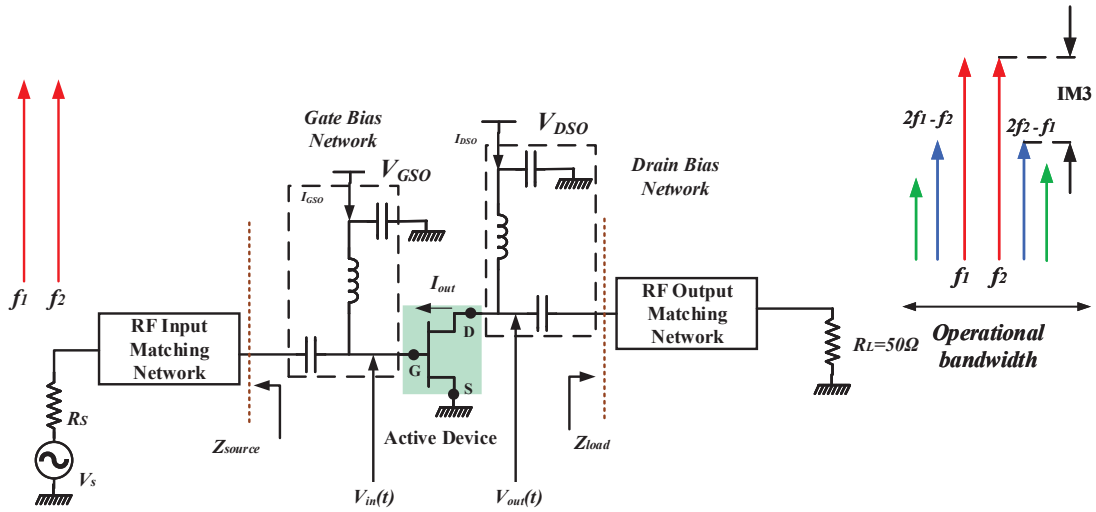

Figure I.13: General schematic of an RFPA indicating the input and output voltages

When the input signal of the generator drives the power amplifier and at the same time, we assume the input of the transistor is linear and I_{out} is depending mainly on V_{in} (t) [3, 4], we have,

$$I_{out}(t) = \alpha_1 V_{in}(t) + \alpha_2 V_{in}^2(t) + \alpha_3 V_{in}^3(t) + ... \tag{I.28}$$

For a single-tone excitation,

$$V_{in}(t) = V_{gso} + V_{gs1} cos(2\pi f t) \tag{I.29}$$

The spectrum shape of I_{out} is illustrated in fig. I.14.

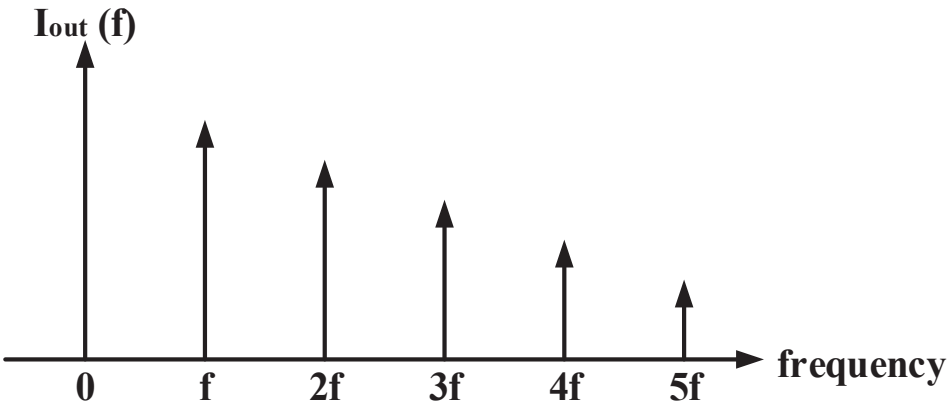

Figure I.14: Shape of the output current spectrum for a single tone linear excitation.

The spectrum of V_{out} has the same shape respectively. An important point to highlight is that the magnitude of the spectral components of drain voltage V_{out} depends on the values of load impedances of the output matching networks (OMN) at harmonics.

If the input of an amplifier is excited by a two- tone signal as shown in fig. I.13, then

$$V_{in}(t) = V_{gso} + V_{gs1}cos\omega_1 t + V_{gs1}cos\omega_2 t \tag{I.30}$$

This quite simple signal is a non-constant envelope signal which can be rewritten as:

$$V_{in}(t) = V_{gso} + 2V_{gs1}cos\Omega t \quad cos\omega_0 t \tag{I.31}$$

where $\Omega = \left(\frac{\omega_1 - \omega_2}{2}\right)$ and $\omega_0 = \left(\frac{\omega_1 + \omega_2}{2}\right)$

Fig. I.15 shows the time domain shape of this signal. The Peak to Average Power Ratio (PAPR) of this signal is 2 (3 dB). If this input signal is injected in equation. I.28, we have the following shape for the spectrum of the output current I_{out} as shown in fig. I.16.

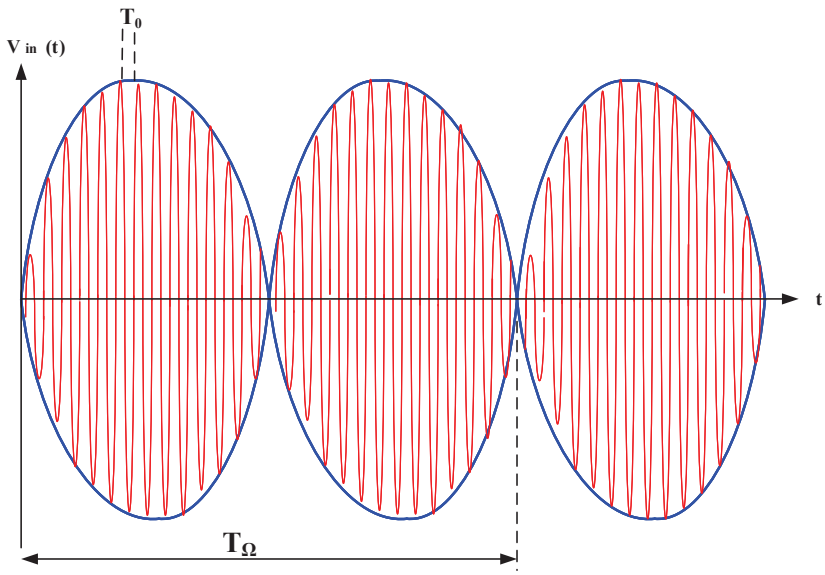

Figure I.15: General shape of a modulated signal with two-tone excitation.

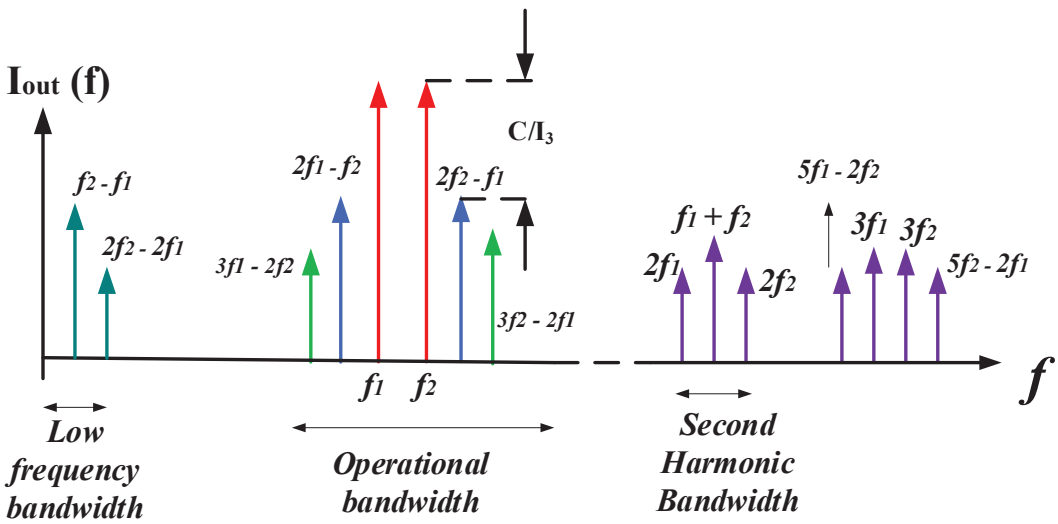

Figure I.16: Illustration of output current spectrum under a two tone excitation showing the intermodulation products.

Intermodulation products appears in the operational bandwidth and cannot be filtered out whereas the low frequency components of the currents are present within the drain bias network. The spectrum of V_{out} has same shape depending upon the load impedances presented at each frequency components by the output bias network and RF matching networks respectively. Consequently if in a more accurate approach, we consider that $I_{out}(t)$ is a function of both $V_{in}(t)$ and $V_{out}(t)$, we can easily understand that the real

behaviour of the amplifier designed for operational bandwidth depends on the entire wide band impedance network from DC up to the harmonic range.

Three major bandwidths have to be carefully analyzed in the designing of a power amplifier. The low frequency bandwidth namely "video bandwidth", the "operational bandwidth" at fundamental frequency and the "bandwidth corresponding to second harmonic". Multiple mixing of products in the video bandwidth, fundamental frequency and second harmonic bandwidths due to the non-linear behaviour of the transistor fall within the operational bandwidth and hence have a significant impact on IM3. For example, if there is a resonance in the video bandwidth due to the drain bias network terminated in the drain access of the device, asymmetries appear between the upper and lower IM3 products. Due to this effect, the linearity of the RFPA is degraded and linearization of PA's using predistortion techniques is more difficult to achieve and sometimes fails.

The third order carrier to intermodulation ratio is defined as the ratio (C/I_3) between the power level of fundamental tones to that of the intermodulation products and is mathematically expressed as :

$$C/I_3(dB), (upper) = 10log\left(\frac{P_{f2}}{P_{2f_2-f_1}}\right) \tag{I.32}$$

and

$$C/I_3(dB), (lower) = 10log\left(\frac{P_{f1}}{P_{2f_1-f_2}}\right) \tag{I.33}$$

There are other criteria that indicate the linearity when the amplifier is excited with non-constant envelope modulated signals like Noise Power Ratio (NPR), Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR) which are explained in the second chapter.

2 Transistor Technology : Gallium Nitride (GaN)

2.1 Why Gallium Nitride ?

GaN-HEMT devices came into the picture in 2004 with depletion-mode power transistors built by Eudyna Corporation. The HEMT structure was first illustrated in 1975 by T. Mimura et al. [5], and in 1994 by M. A. Khan et al. [6], which has shown high electron mobility in the interface between aluminum gallium nitride (AlGaN) and GaN layers. GaN transistors have demonstrated significant amount of suitability for high power RF applications over the years. In June 2009, the Efficient Power Conversion Corporation (EPC) introduced the first enhancement-mode GaN on silicon FETs designed specifically as power MOSFET replacements.

Firstly, GaN-HEMT's were produced in bulk and at low cost thanks to the silicon manufacturing technology and facilities. Since then, Matsushita, Transphorm, GaN Systems, RFMD, Panasonic, HRL, and International Rectifier, among others, have manufactured high power GaN transistors for the power conversion market. The main requirements for semiconductors used in high power applications are efficiency, reliability, and cost effectiveness without which they would not be economically viable [7].

GaN HEMT transistor technology has matured in the last few years demonstrating high power density and high-frequency performance except for thermal conductivity. The thermal performance of GaN-based devices depends on the thermal conductivity of the substrate. For example, SiC has a thermal conductivity of around 120W/mK having an upper hand over Silicon based substrates, but it is not so cost effective.

RF power amplifier designing has benefited significantly from these interesting potentialities, for example the output capacitance has reduced by a factor of 10 comparable with LDMOS, also increased input and output impedance has enabled lower-loss and broader-band matching circuits, increased reliability under high temperature operation, maximum operating frequency increased by more than a factor of 8 compared with LDMOS, and above all increased drain voltage breakdown limits.

HEMT operation is different as compared to conventional MOSFET devices. The conduction channel is formed due to the junction between two materials having different band gaps (called a heterojunction). In this way current travels through high-mobility electrons generated at the heterojunction in a thin layer called the two-dimensional electron gas (2DEG). Instead of the MOSFET gate oxide, the HEMT has a Shottky gate which allows

forward current conduction under saturation. Also unlike MOSFETs, microwave HEMTs are generally depletion mode that is a negative voltage is required to turn off the channel.

GaN HEMTs on the other hand have several drawbacks also in terms of cost as compared to LDMOS. GaN devices are commercially available from manufacturers such as NXP, UMS, QORVO, TriQuint, Nitronex, Wolfspeed, Sumitomo, and RF Micro Devices among others. A type of memory effect behavior usually attributed to charge trapping is particular to III-IV semiconductor devices. The behavior can be qualitatively described as a reduction in quiescent current immediately following a high-power pulse. The quiescent current recovers gradually to its original value with a time constant ranging from microseconds to minutes depending upon device design. This leads to time-varying quiescent current which depends on the history of the output power, and thus time-varying PA gain [8, 9, 10].

2.2 General Figure of Merits for GaN Device Selectivity

Table I.1 gives a comparison of principal properties of Silicon, GaAs, GaN and SiC materials.

Parameters	**Units**	**Silicon**	**GaAs**	**GaN**	**Sic**
Band Gap, E_g	eV	1.1	1.4	3.4	2.9
Critical Field, E_{crit}	Mv/cm	0.3	0.4	3.3	2.5
Electron Mobility, μ_n	cm^2/V-s	1300	5000	2000	950
Saturation Velocity	10^7 cm/s	1	1	2.2	2
Thermal Conductivity, λ	W/cm-K	1.5	0.46	1.3	4.9
Permittivity, ε_r		11.4	13.1	9	9.7

Table I.1: Comparison of principal material properties of Silicon, GaAs, GaN and SiC.

Based on the above key material properties, some Figures of Merit for GaN are highlighted in the following sections.

2.2.1 Band Gap, Intrinsic Charge Density and Breakdown Field

The difference in the energy level between valence and conduction bands identifies the energy band gap of any semiconductor material. A free electron from valence band jumps to the conduction band, thereby contributing in the conduction current. Due to its large forbidden band gap (3.4eV), GaN naturally has a high $E_{Br.}$ breakdown field from where the phenomenon of destructive breakdown occurs along with its conduction which can be

mathematically expressed as:

$$E_{Br.} \propto E_g^{3/2} \tag{I.34}$$

This allows the GaN components to develop power under high voltage, which is of great interest in applications to high power electronics circuits like PA's. Furthermore, RF matching conditions close to 50 Ohms are made easier. This gap on one hand, exhibits a low density of intrinsic carriers at high temperature, and on the other hand, low leakage currents. Because of the lattice arrangements of the crystal lattice structure with the temperature, the value of the energy band-gap tends to decrease with an increase in temperature. The performance will therefore be degraded by temperature of the GaN component.

2.2.2 Thermal Conductivity

The thermal conductivity defines the capacity of the material to transmit heat. This varies significantly depending on the temperature. Thermal conductivity is the contribution to the atomic level of two distinct origins: the movement of free carriers, and the structure of the crystal lattice to thermal equilibrium. As SiC has a high thermal conductivity, GaN on SiC substrate will have superior performance but at the detriment of price factor.

2.2.3 Johnson's Figure of Merit (JFM) and Baliga's Figure of Merit (BFM)

There are several additional figure of merits that exist at high frequencies for different choices of device technology, the important one being :

$$JFM = \frac{E_c v_s}{2\pi} \tag{I.35}$$

$$BFM = \epsilon_r \mu_n E_c^3 \tag{I.36}$$

where, E_C is the critical field, v_s is the saturation velocity of the free carriers, ϵ_r is the relative permittivity, and μ is the mobility of electrons in the semiconductor material. It highlights in particular the high value of the critical field, the highest saturation speed and the best thermal conductivity for GaN material with respect to Si and AsGa, resulting in a standardized figure of merit which is 17 and 22 times higher than those of AsGa and Si

[11]. BFM indicates the switching losses of the material and JFM indicates the switching delay. Table I.2 indicates the JFM and BFM values for Si and GaN materials respectively.

Parameters	Silicon	GaN
JFM	1	850
BFM	1	1090

Table I.2: JFM and BFM values for Silicon and GaN.

2.3 GaN Device Structure

The operation of AlGaN/GaN HEMT is based on the properties of the heterostructure which is formed when a layer of the wide band gap material AlGaN (doped or undoped) is grown on the narrow band gap material GaN layer. Due to the difference in their band gaps, band-bending takes place in both conduction band and valence band. The energy band diagrams of both narrow and wide band-gap semiconductors are illustrated in Fig. I.17. Because of the depletion mode characteristics, GaN is usually a normally-ON device.

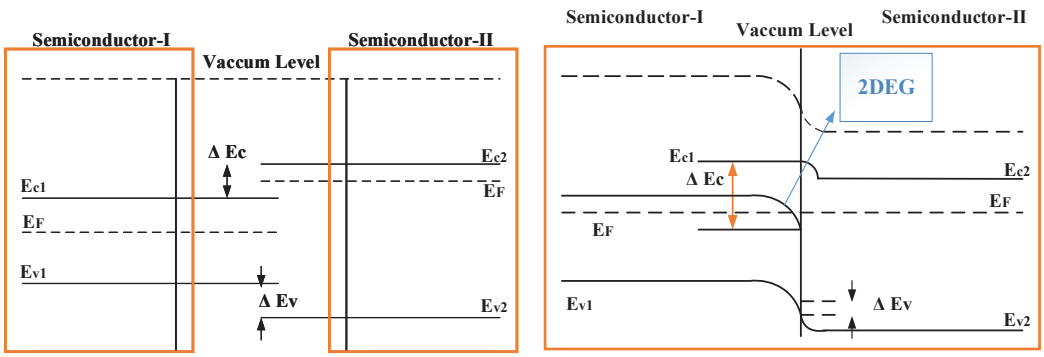

Figure I.17: Energy band diagrams for narrow (I) and wide (II) band gap semiconductors (left) and also the discontinuities in bands after equilibrium in the heterostructure (right).

Fig. I.18 (a) shows the simplified cross-section of AlGaN/GaN-HEMT and fig. I.18 (b) shows the cross-section of AlGaN/GaN-HEMT on a Silicon substrate seen with a scanning electron microscope.

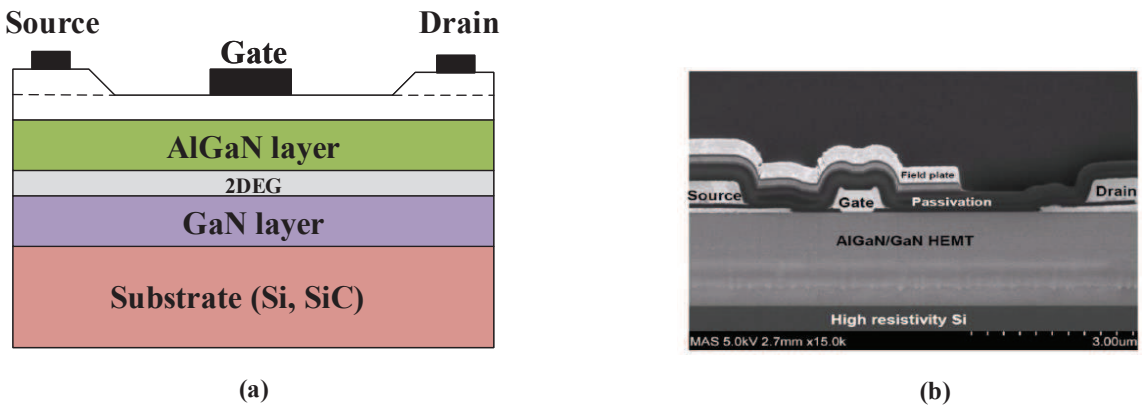

Figure I.18: (a) Simplified cross-section of AlGaN/GaN-HEMT and (b) Cross-section of AlGaN/GaN-HEMT on a Silicon substrate seen with a scanning electron microscope.

Near the heterojunction of the GaN layer, a channel is formed because of the discontinuity in the conduction band. This two dimensional electron gas (2DEG) acts as the conducting channel for the HEMT. Due to the wurtzite crystal structure, GaN lacks symmetry [7]. This leads to large spontaneous polarization (PSP). In addition, the piezoelectric coefficients (PPE) of III-Nitrides are very stronger than any III-V semiconductor.

These effects facilitate the AlGaN/GaN heterostructure to form the 2DEG without any external doping in the AlGaN layer. HEMT is a three terminal device where the current between the drain (D) and source (S) flows through the 2DEG conducting channel and is controlled by the space charge which changes according to the applied voltage at the gate (G) terminal. If the gate voltage is increased in the negative values, the space charge below the gate starts to spread and deplete the channel. At some point the channel is totally pinched-off. The presence and quality of the 2DEG largely affects the quality of performance of a HEMT.

GaN is a polar crystal which exhibits strong polarization effects at the hetero-junction interface due to which, it can achieve very high values of 2DEG sheet carrier concentration (ns). Carrier concentration of 1013 atoms/cm_2 [12] is achieved without any external doping [13] in the device structure. In general, the doping could reduce the electron mobility through scattering mechanisms. In case of an undoped AlGaN/GaN HEMT device, there is little possibility of electron scattering, the electrons tend to have high mobility and hence the device is referred to as High Electron Mobility Transistor.

There are two kinds of polarization namely spontaneous and piezoelectric polarization that contributes to the formation of 2DEG in the AlGaN/GaN HEMT [12]. The sponta-

neous polarization results from the built-in polarization field in an unstrained GaN crystal and exists when the crystal lacks its symmetry and the bond between two atoms is not purely covalent. This results in the accumulation of surface charge of opposite polarity across both the ends of the crystal. In an ordinary GaN crystal, the polarization charges do not accumulate because the oppositely charged charges tend to cancel each other and the resultant spontaneous polarization is zero. However in AlGaN/GaN heterostructure, the GaN crystal suddenly ends and AlGaN crystal begins so there is an abrupt change at the hetero-junction interface gives rise to an electrically charged region in the vicinity of the junction. The surface charge formed due to the spontaneous polarization is shown in fig. I.19.

Figure I.19: Spontaneous polarization induced surface charges in the AlGaN and GaN structure.([14])

The piezoelectric polarization normally occurs because of distortion of the crystal lattice. Due to the larger difference in lattice constants between the AlGaN and GaN materials, the AlGaN barrier layer grown over the GaN substrate experiences a tensile strain and is shown in fig. I.20.

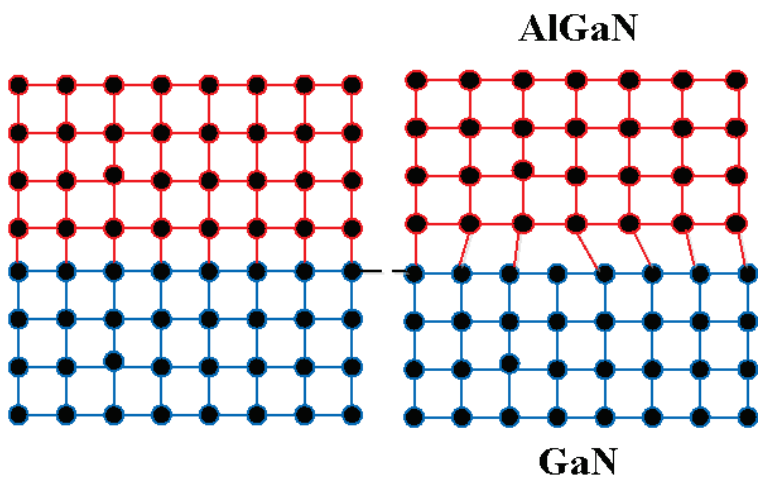

Figure I.20: Strain induced piezoelectric polarization in the AlGaN/GaN heterostructure ([14]).

The amount of strain produced is directly related to the thickness of the barrier layer. The piezoelectric coefficient is generally higher for GaN material and hence the strain results in high sheet charges at the hetero-junction interface. The strain induced due to piezoelectric polarization can alter the band structure and thus changes the sheet carrier concentration in the channel region. Hence, the strain induced polarization provides an additional way of engineering, through which the HEMT device characteristics can be altered.

In a typical doped depletion mode (normally ON) AlGaN/GaN HEMT structure, the doped AlGaN barrier layer carries electrons to the heterostructure interface. The contribution of the doped AlGaN barrier layer to the 2DEG at the hetero interface region is reported to be less than 10% due to the polarization nature of GaN material [15]. It has also been reported that the doped AlGaN/GaN HEMT structures shows better DC performance compared to undoped GaN HEMTs but the higher doping in AlGaN barrier layer increases the scattering effects and it may degrade the RF performance of the device [16].

The AlGaN/GaN HEMT is a depletion mode device and the Schottky gate contact has two major functions in device operation (i) it depletes the channel (ii) it avoids the parasitic parallel conduction between the source and drain regions. The source and drain contacts are usually formed using Ti/Al (or) Ti/Au and the Schottky gate contact is made from Ni/Au (or) Pt/Au [17]. The typical structure is subjected to major problems such as DC-RF dispersion which is related to surface and bulk traps and high leakage current [18].

2.4 General Overview of the GaN Devices used in this work

In this thesis work, Dual-flat-no-lead (DFN) packaged GaN transistors from Wolfspeed have been used for the design procedure of the proposed circuit as shown in fig. I.21. Two transistors, namely Wolfspeed **CGHV1F006S** [19] and Wolfspeed **CGHV1F025S** [20] have been used as driver and the power stages of the circuits designed in this thesis. They have the capability to deliver 6W and 25W CW output powers respectively. Different potentialities of the transistors individually are explained in the next few sections below with the help of simulations in Keysight ADS.

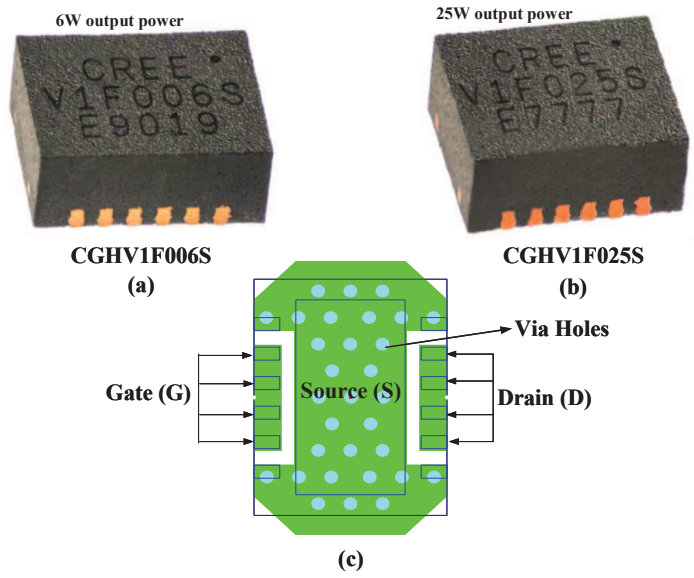

Figure I.21: Packaged transistor technology used: (a) Cree CGHV1F006S (b) CGHV1F0025S and (c) Transistor footprints indicating the different terminals.

2.4.1 DC-IV curves

Fig. I.22 illustrates the simulated DC-IV characteristics of the 6 W and 25 W GaN transistor respectively highlighting the ohmic region and the maximum current handling capabilities.

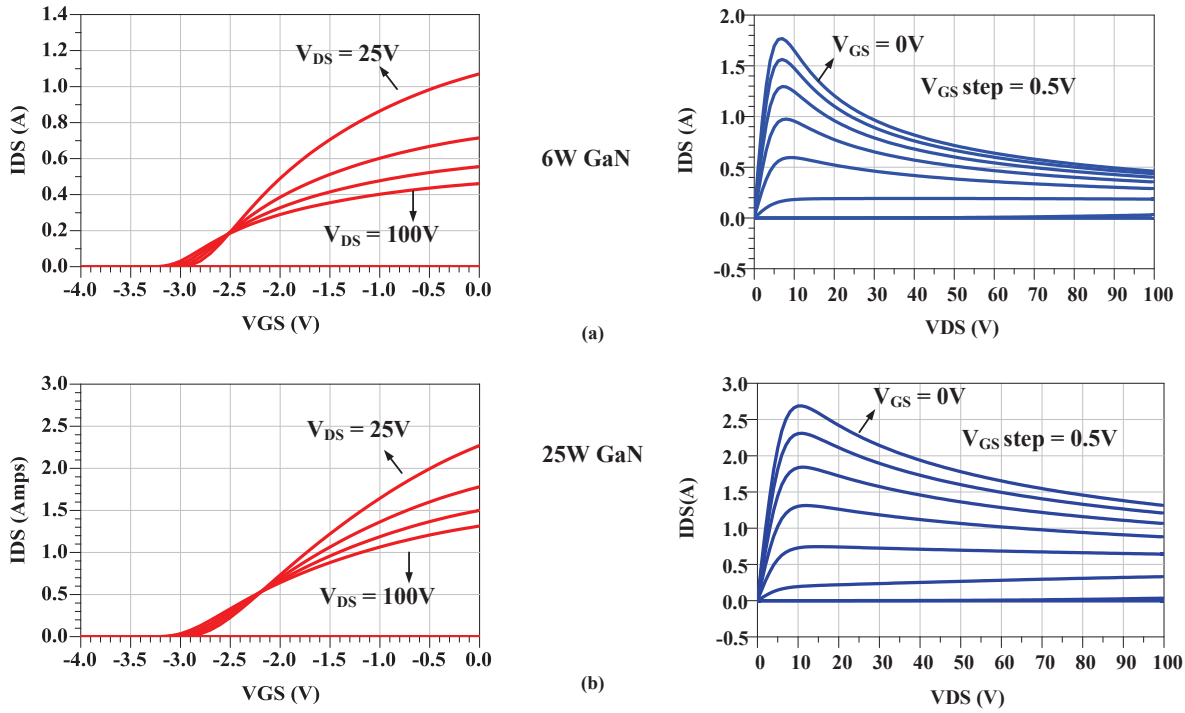

Figure I.22: DC-IV characteristics: (a) Cree CGHV1F006S (b) CGHV1F0025S.

The operating conditions for both the transistors have been chosen close to class B mode of operation for the purpose of higher efficiency when designing the amplifiers. Both the GaN transistors are designed specifically for high efficiency, high gain and wide bandwidth capabilities and can be operated at a frequency of up to 18 GHz (L, C, X and Ku bands).

2.4.2 Maximum Available Gain (MAG) and Maximum Stable Gain (MSG)

The Maximum Available Gain (MAG) of an amplifier is always defined for a condition when the input and output of the transistor are conjugate matched and the gain is said to be then maximized with respect to the load and source impedance. Maximum Stable Gain (MSG) is obtained under the condition when the transistor is not unconditionally stable, i.e the Rollet's stability factor K < 1.

where

$$\Delta = 1 + |S_{11}|^2 - |S_{22}|^2 + |S_{11}.S_{22} - S_{12}.S_{21}|^2 \quad > 0 \tag{I.37}$$

and,

$$K = \frac{1 + |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}.S_{21}|} \quad > 1 \tag{I.38}$$

Mathematically, MAG is expressed as follows :

$$MAG = \frac{|S_{21}|}{|S_{12}|}(k - \sqrt{k^2 - 1}) \tag{I.39}$$

Mathematically, MSG is expressed as follows :

$$MSG = \frac{|S_{21}|}{|S_{12}|} \tag{I.40}$$

Fig. I.23 illustrates the MSG and MAG capabilities of the 6 W and 25 W unmatched transistors with ideal DC feed and DC block for operating conditions close to class B. It can be observed in the red curve that the MAG becomes the MSG beyond a certain frequency when K factor becomes greater than 1.

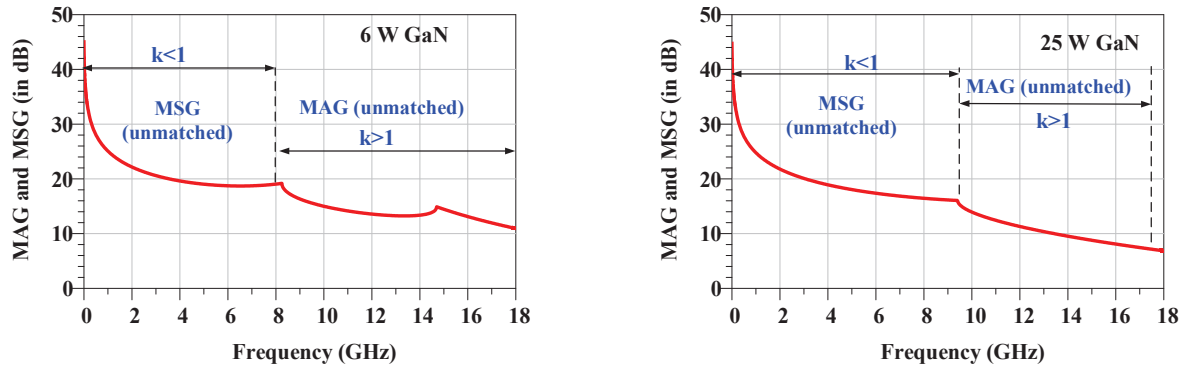

Figure I.23: Simulated MAG and MSG capabilities of the 6 W (left) and 25 W (right) packaged GaN transistor alone.

It can be observed from fig. I.23 that at least 10 dB small signal gain can be obtained up to a frequency of around 18 GHz for the 6 W device and 14 GHz for the 25 W device. The description of small-signal analysis, stability factor and concerned issues of the individual 6 W and 25 W amplifiers and their design issues are addressed in the third chapter of this thesis.

3 Conclusions

The semiconductor technology used in the power amplification function has evolved constantly in the past few decades. The GaN material associated with an SiC substrate offers much better electrical properties as compared to silicon in terms of breakdown field, working temperature and current density. Normally ON GaN technology has a very high potential for high frequency applications.

However, its manufacture remains costly and its technological process still suffers from a lack of knowledge concerning the dispersive effects of traps (inherent in HEMT technology) and reliability. The GaN HEMT technology on silicon appears to be a promising solution in terms of manufacturing costs and performance [21], and can allow GaN to be established for new RF applications. For power management applications, it has the disadvantage of being normally ON. It is therefore not easily integrable in architectures related to MOSFET's (normally OFF). To ease this problem and offer new fields of applications to GaN, the e-mode HEMT GaN is making its appearance. This technology appears to be a promising solution however, it is still not matured, nevertheless it already surpasses the performance of MOSFET in power management applications.

Therefore, the GaN HEMT d-mode is today an ideal candidate to be used for the design of microwave power circuits. As a result, it has attracted a lot of interest in exploiting its potential in the search for innovative power amplification architectures. The basic requirements and the great difficulty in this area relate to the high-performance broadband operation with high efficiency for high power variations.

Along with a brief overview of GaN device technology for high power applications, this chapter has also highlighted the different design considerations, issues and parameters associated with designing modern RF power transmitters. Due to the ever increasing subscriber demands for power and frequency flexibility, more complex spectral efficient schemes have been introduced which cause high peak to average power ratio (PAPR) of the RF signal to amplify thereby degrading average efficiency in the presence of modulating signals at the RFPA input. The second chapter of the thesis briefly adresses this issue along with some associated challenges and topologies for high efficiency amplification process and gives a further insight in the objective of this thesis which is the investigation of the feasibility of a high efficiency Vector Power Modulator (VPM).

Chapter II

High Efficiency RF Power Transmitter Architectures

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1 Introduction

1.1 Motivation

The never-ending requirements for higher capacity and data rates have put increasing demands on the nominal output power from radio base stations. At the same time, operators want to cut their radio network operating expenses, out of which, the energy consumption is the most important factor. All these factors have contributed to the evolution of complex modulation techniques which lead to improvement of spectral efficiency. At the same time, it also imposes severe design constraints for the designers and hence the conventional transmitter architectures are no longer able to keep up the pace with increased signal quality. Moreover, with improved channel capacity, the rate of evolution in communication transmitter architectures have come at a slow rate.

To meet the requirements of modern transmitter systems, some advanced architectures of power amplifiers have come into existence to improve the average efficiency of the system. The factor of average efficiency comes into the picture when the signal to be transmitted has a non-constant envelope shape which arises when multiple modulated carriers are integrated together within an allocated frequency band. This gives rise to Peak to Average Power Ratio (PAPR) of the useful signal thereby enabling amplifiers to operate at high efficiency only at peak power whereas causing degradation at the average power level for most of the time.

This chapter is dedicated to the presentation of few of the main characteristics of complex modulated signals along with the problems associated with high power amplification in the transmitter chain. This chapter highlights also some of the advanced RF power transmitter architectures that help in efficient amplification of high PAPR signals.

1.2 Basics of Modern Modulation Schemes

Spectrally efficient modulated signals have non-constant envelopes generating high PAPR. With high PAPR signals, a very small portion of the DC power used by the PA's is converted to radiated energy because efficiency peaks up at saturated power and drops significantly when it is backed-off causing also severe distortions which is due to the non-linear gain shape. Furthermore, the linearity of the RFPA is another important requirement. If linearity is not sufficiently good, the situation can be catastrophic if the transmitter is a multi-carrier system as it introduces interference with the adjacent channels. As PAPR has grown into a major concern for modern transmitter design procedures [22, 23], it is

therefore important to understand the main features of such complex modulated signals before proceeding towards the design.

In fact, most spectral efficient modulation types, such as QAM and OFDM, exhibit similar high-PAPR characteristics of the order of 10 dB. The characteristics of any modulated signal that contribute to efficiency degradation are explained in the following sections.

1.2.1 RF Modulation Scheme in Bandpass Radio Communication Channel

In radio communications, modulation can be described as the process of conveying a message signal by superimposing an information bearing signal onto a carrier signal by varying the signal characteristic. Modulation is the process of changing a higher frequency signal in proportion to a lower frequency one. The higher frequency signal is referred to as the carrier signal and the lower frequency signal is referred to as the baseband signal. The characteristics (amplitude, frequency or phase) of the carrier signal are varied in accordance with the information bearing signal. These high-frequency carrier signals can be transmitted over the propagating channel.

The use of high frequency signals will make the amplifier and antenna design easier for effective radio design. Fig. II.1 shows the up conversion of the complex-valued baseband signal X'(t) to the passband then the transmission of the real-valued bandpass signal X(t) through the communication channel. After the bandpass signal goes through the channel, a down-conversion of the bandpass output Y(t) into a complex-valued baseband signal Y'(t) occurs in the receiver. The baseband signal X'(t) is up-converted to the bandpass signal by amplitude, phase or frequency modulation in order to transmit it.

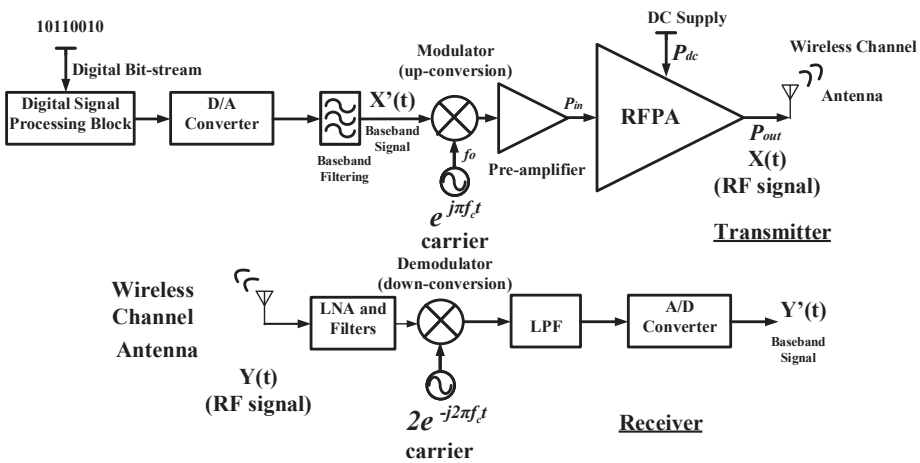

Figure II.1: General Illustration of Communication Transceiver Chain

Any complex modulated bandpass signal can therefore be written in a general form by the following equation :

$$X(t) = V(t)[cos2\pi f_c t + \phi(t)] \tag{II.1}$$

Where X(t) is considered here as a voltage across a 50 Ohm standard load R_o, f_c is the carrier frequency, V(t) is the time domain envelope and $\phi(t)$ is the phase of the signal.

The bandpass signal X(t) has an envelope bandwidth which is lesser than the carrier frequency f_c. Using trigonometric identities, the modulated signal can be re-written as follows:

$$X(t) = I(t)cos(2\pi f_c t) - Q(t)sin(2\pi f_c t) \tag{II.2}$$

Where I(t) is the baseband in-phase component and Q(t) is the baseband quadrature phase component of the signal respectively and are represented as:

$$I(t) = V(t)cos\phi(t) \tag{II.3}$$

and

$$Q(t) = V(t)sin\phi(t) \tag{II.4}$$

Replacing the values of I(t) and Q(t) in equation equation II.2, we get,

$$X(t) = V(t)cos\phi(t)cos(2\pi f_c t) - V(t)sin\phi(t)sin(2\pi f_c t) \tag{II.5}$$

or

$$X(t) = Re\left[V(t)e^{j(2\pi f_c t + \phi(t))}\right] \tag{II.6}$$

The above equation can be rewritten as

$$X(t) = Re\left[X'(t)e^{j(2\pi f_c t)}\right] \tag{II.7}$$

where X'(t) is the baseband input signal and can be represented as:

$$X'(t) = I(t) + jQ(t) \tag{II.8}$$

or

$$X'(t) = V(t)e^{j\phi(t)} \tag{II.9}$$

Similarly, the baseband output signal $Y'(t)$ can be obtained from the bandpass output signal Y(t) through demodulation process. The choice of a modulation scheme depends on the physical characteristics of the channel, required levels of performance and hardware trade-offs.

Fig. II.2 shows the ideal Quadrature Transmitter System and thus the generation process of in-phase and quadrature phase signals. To do this, an oscillator is used which converts a DC supply power into RF carrier which is then combined with the modulator. The data adjust or modulate the characteristics of the carrier (amplitude and phase) in a controlled manner.

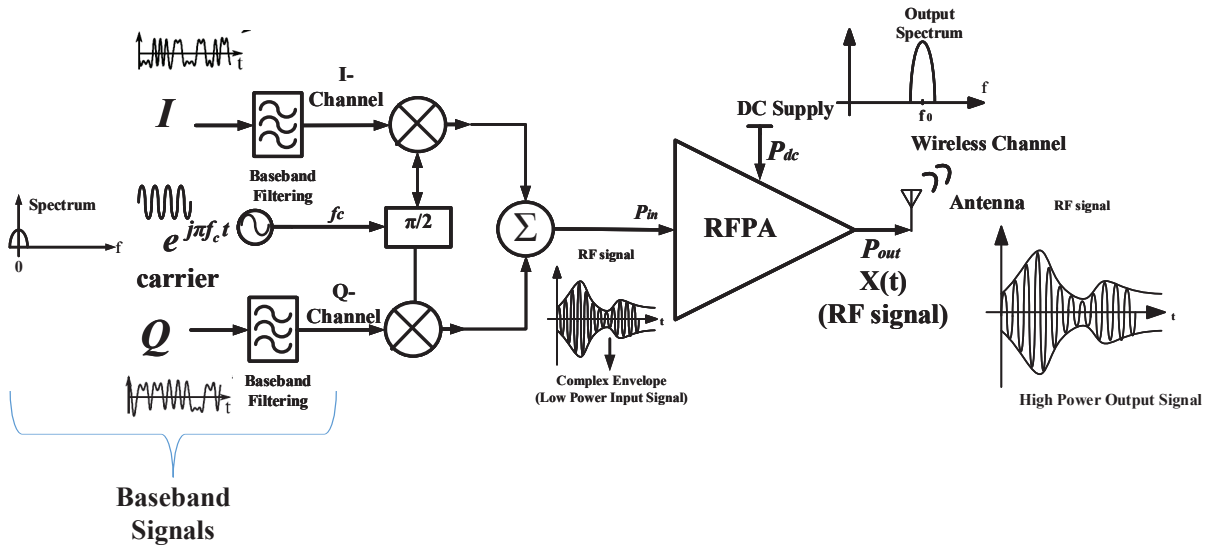

Figure II.2: Ideal Quadrature Transmitter System

The final and the most critical step is then to increase the signal strength with an RFPA so that it can be detected by the receiver. The output of the power amplifier feeds an antenna which transmits the information carrying signal into the channel which is free space for wireless communication.

1.3 Characteristic Features of Modern Modulated Signals

Once the general transmitter architecture has been presented in the above section, now we can define certain properties that characterize such signals. The key figures of merit associated with any complex modulated signal are as follows:

1.3.1 Crest Factor and Peak to Average Power Ratio (PAPR)

Before analyzing the complex modulated power, it is very important to have an idea about the time domain shape of the signal. Crest factor is a measure of a waveform, showing the ratio of the peak power value to the average value. In other words, crest factor indicates how extreme the peaks are in a waveform. Crest factor equivalent to one indicates no peaks, such as a CW tone. Higher crest factors indicate peaks [22].

For a modulated signal that shows high PAPR, crest factor is defined mathematically as:

$$\xi = \frac{V_{peak}}{V_{RMS}} \tag{II.10}$$

Where V_{peak} is the peak amplitude of the voltage and V_{RMS} is the root mean square value of the modulated signal voltage respectively as represented in Fig. II.3.

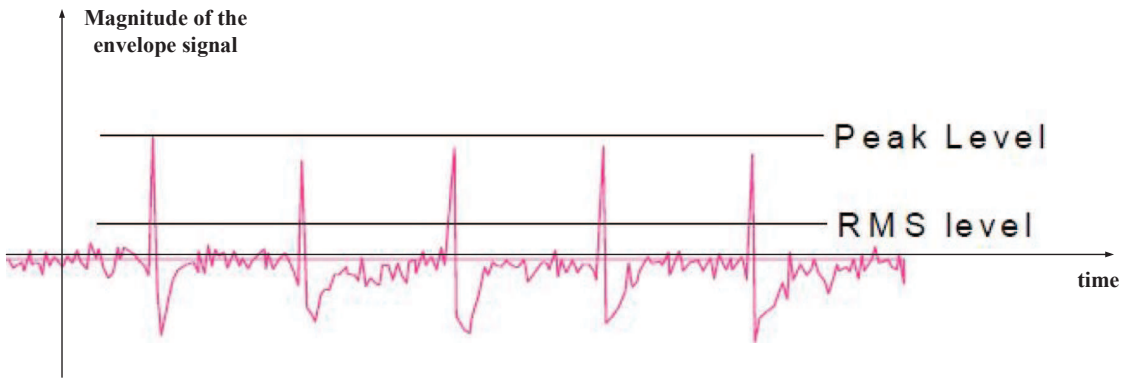

Figure II.3: Crest Factor Representation for Complex Modulated Signal

When expressed in decibels, crest factor is equivalent to Peak to Average Power Ratio and is mathematically defined as:

$$PAPR \quad (dB) = 10.log_{10}(\xi^2) \tag{II.11}$$

or

$$PAPR \quad (dB) = 20.log_{10}(\xi) \tag{II.12}$$

The statistical analysis of PAPR is done using Complimentary Cumulative Distributive Function (CCDF) which indicates the probability that the instantaneous output power would be higher than a certain value.

Consider for an example that the signal has a PAPR of 10 dB. This implies that if we imagine a signal with average power of 0.1 Watts is to be transmitted, the transmitter must be able to handle power peaks which are 10 times higher, so the saturated power must be at least 1 W. This power is dissipated most of the time in form of heat as the peaks are only occurring momentarily thereby reducing the overall efficiency.

1.3.2 Average and Instantaneous Power for Modulated Signals

Fig. II.4 shows a simplified representation of an amplitude modulated signal with variable envelope represented as E(t) = E (1+kcosΩt) . cosω_0t, where $0 < k < 1$ and E(t) is a voltage across a 50 Ohm load, R_0.

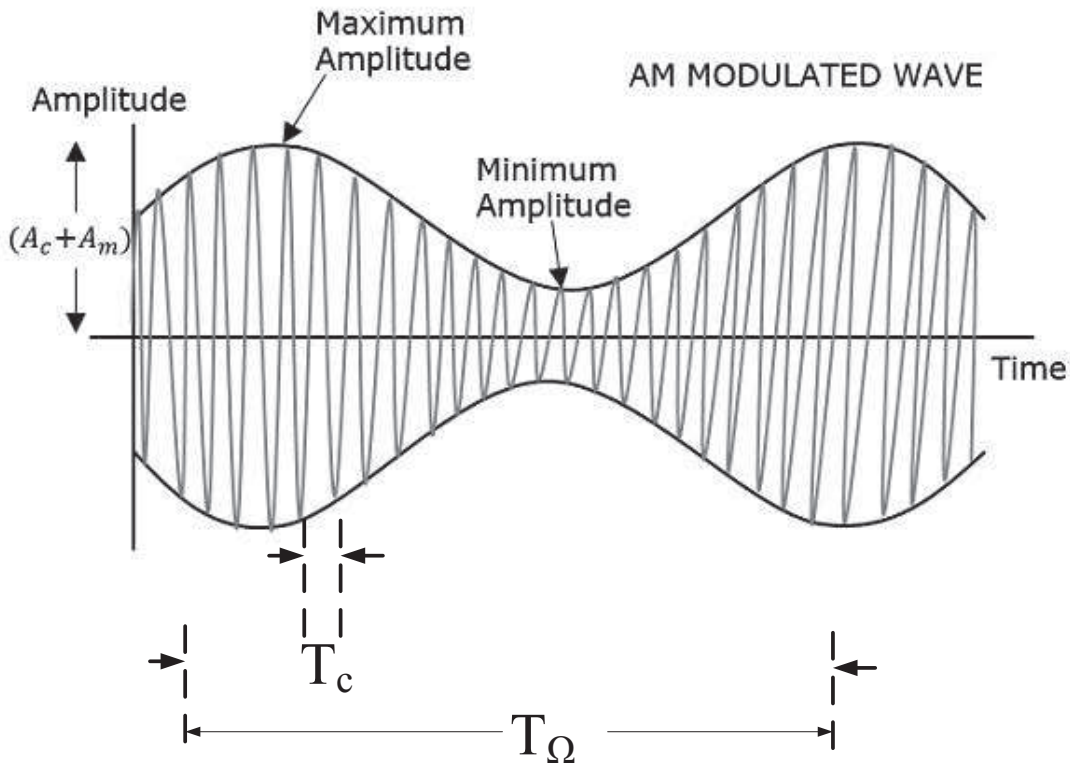

Figure II.4: Simplified representation of an amplitude modulated signal with variable envelope

The envelope of this signal is represented as E'(t) = E (1+kcosΩt)

The average power of such modulated signal is expressed by the following relation:

$$P_{avg}(W) = \frac{1}{R_0.T_\Omega}\int_0^{T_\Omega} |E(t)|^2 \quad dt \tag{II.13}$$

which is equivalent to

$$P_{avg}(W) = \frac{E^2}{2R_0}.(1+\frac{k^2}{2}) \tag{II.14}$$

The instantaneous envelope power is given by the relation :

$$P_{inst}(t) = \frac{1}{R_0}.|E(t)|^2 \tag{II.15}$$

which is equivalent to

$$P_{inst}(t) = \frac{E^2}{R_0}.(1+kcos\Omega t)^2 \tag{II.16}$$

The peak envelope power is reached when cosΩt = 1. Therefore peak envelope power can be defined mathematically as:

$$P_{peak} = \frac{E^2}{R_0}.(1+k)^2 \tag{II.17}$$

The average envelope power is given by

$$P_{avg} = \frac{1}{R_0.T_\Omega}\int_0^{T_\Omega} [E(1+kcos\Omega t)]^2 \quad dt \tag{II.18}$$

On solving above equation, we get

$$P_{avg} = \frac{E^2}{R_0}.\left(1+\frac{k^2}{2}\right) \tag{II.19}$$

And thus, PAPR of this signal can be expressed by the following expression:

$$PAPR(dB) = 10 \quad log_{10}\left(\frac{P_{peak}}{|P_{avg}|}\right) \tag{II.20}$$

which is equivelent to

$$PAPR(dB) = 10 \quad log_{10}\left(\frac{[1+k]^2}{1+\frac{k^2}{2}}\right) \tag{II.21}$$

For example, if k=1, PAPR = 4.26 dB.

1.3.3 Probability Density Function (PDF)

The Probability Density Function (PDF) of a signal is the statistical representation taken by the amplitude of the envelope (which is considered as a random variable), over the entire signal duration. Practically, PDF gives information on the percentage of time during which the signal has a specific given amplitude.

A PDF of a complex modulated signal always depends on the type of modulation and the baseband filtering conditions applied to the I and Q channels. Probability density function (PDF) indicates the probability of a specific instantaneous envelope power level through a normalized histogram of the data based on the time domain analysis where the flow of power is represented in the form of quantified variable in histogram [11, 22]. Because the digital modulation has evolved with ever more complex modulation schemes, the PAPR is ever larger, and the PDF moves toward a low power region in the histogram plot.

Fig. II.5 illustrates an example of PDF and typical gain and PAE behaviour of a conventional RFPA. The effect of high PAPR on average efficiency when the output power is backed-off to preserve the signal linearity is clearly visible as well as the need to operate at an input power back-off to stay in the linear region of the power gain.

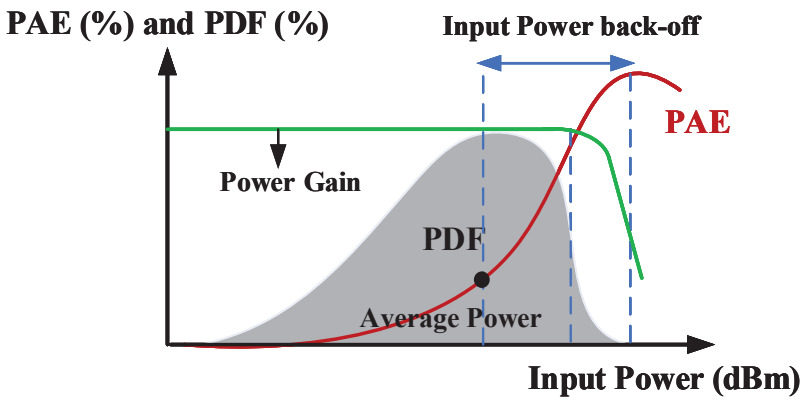

Figure II.5: Typical RFPA efficiency with respect to input power. Probability density function for a high PAPR signal at an average output power level example is illustrated.

Efficiency drops quickly as input power is backed off from the peak power so that the PA can operate in a more linear region to meet linearity criteria. Amplitude-modulated signals such as 4G LTE have probability distributions away from maximum output power and PAE, hence resulting in inefficient operation at the time-average power level.

1.4 RFPA Spectral Regrowth and Adjacent Channel Power Ratio (ACPR) : Out-of Band Distortion

Adjacent-channel power ratio is the linearity figure-of merit for wireless communication systems employing non-constant envelope modulation techniques. These linear modulation techniques, although spectrally efficient, produce modulated carriers with envelope power fluctuations. This fluctuation results in signal distortion and spectral spreading when the modulated carrier is passed through a saturated RF power amplifier as illustrated in Fig. II.6.

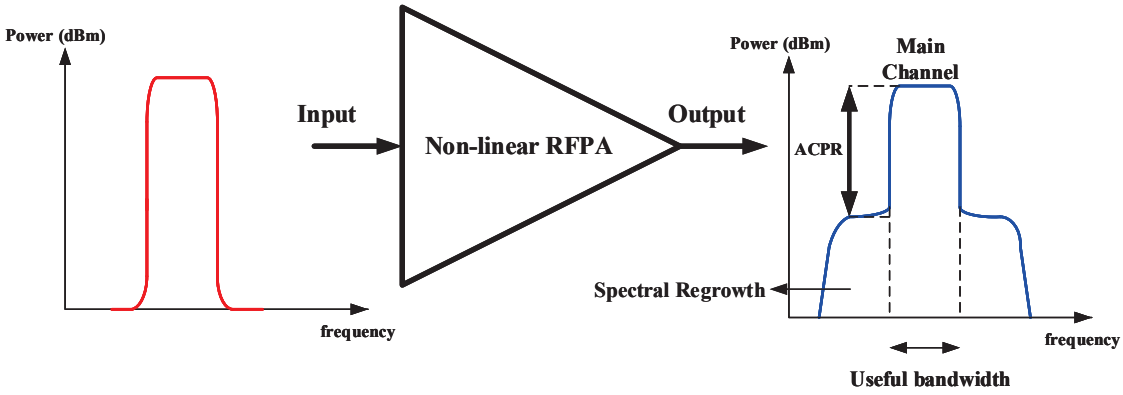

Figure II.6: Graphical depiction of ACPR for Complex Modulated Signals, Input spectrum of the modulated signal (left, in red) and Output Spectrum (right, in blue)

When a modulated wideband signal is incident on a non-linear Device Under Test, spectral re-growth occurs which has the consequence of leaking into the adjacent channel, causing over-the-air interference within a different carriers channel bandwidth. Fig. II.7 shows the example of an output spectrum of an RFPA with spectral regrowth.

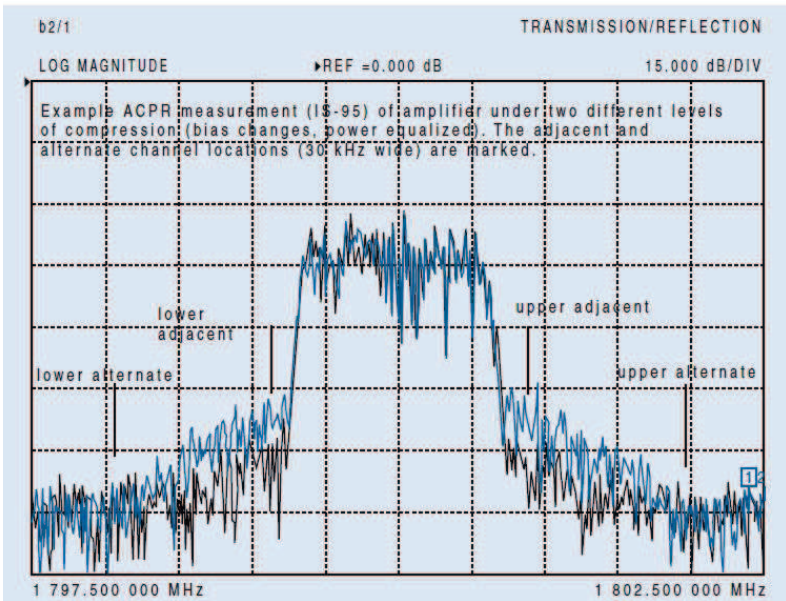

Figure II.7: Example of a non-linear RFPA output spectrum illustrating spectral regrowth ([24]).

ACPR is mathematically expressed by the following relation:

$$ACPR(dB) = 10log_{10}\left(\frac{\int_{main-channel} P_{out}(f)df}{\int_{adjacent-channel} P_{out}(f)df}\right) \tag{II.22}$$

Where $P_{out}(f)$ is the power spectral density of the envelope signal at the output of the PA. The ACPR then corresponds to the ratio between the average power present in the main transmission channel and the average power falling on the upper or lower adjacent bands.

1.4.1 Error Vector Magnitude (EVM) : In-band Distortion

For achieving acceptable DC-RF power conversion, the power amplifier should operate at peak power level close to saturation which makes the output signal distorted in a non-linear manner. These nonlinear distortions cause in-band interference further leading to amplitude and phase deviation of the modulated signal across the PA output. In band interference causes errors in the symbol vectors. While ACPR is an estimation of the non-linear effects on other channels, the error vector magnitude (EVM) is used to analyze in-band distortion.

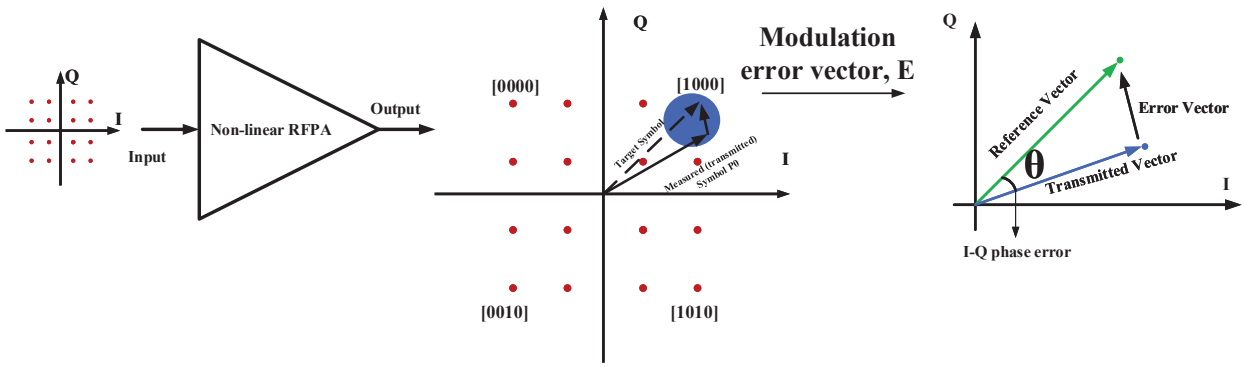

Figure II.8: Demonstration of EVM principle for 16-QAM constellation example across RFPA output

EVM is the measure between the ideal reference symbol vector and the transmitted measured symbol vector which are defined in the I-Q constellation diagram. EVM measures the modulation quality of the signal and indicates modulation accuracy. The ratio of the error vector magnitude to the original symbol magnitude defines the EVM as:

$$EVM = \frac{E}{P_0} \tag{II.23}$$

Where E is the error vector and P_o is the transmitted measured symbol vector. An unimpaired 16-QAM digitally modulated signal would have all of its symbols land at ex-

actly the same 16 points on the constellation over time. Real-world impairments cause most of the symbol landing points to be spread out somewhat from the ideal symbol landing points as illustrated in Fig. II.8 across the RFPA output. [25].

The RMS value of EVM is expressed by the following relation:

$$EVM_{RMS} = \sqrt{\frac{\frac{1}{N} \quad \sum_{i=1}^{N} [|S_{reference,r} - S_{measure,r}|]^2}{\frac{1}{N} \quad \sum_{i=1}^{N} [|S_{reference,r}|]^2}} \quad . \quad 100\% \qquad \text{(II.24)}$$

Where, $S_{measure,r}$ is the normalized rth symbol in a stream of measured symbols, $S_{measure,r}$ is the ideal normalized constellation point for the rth symbol, and N is the number of distinct symbols in the constellation [25].

1.4.2 Noise Power Ratio (NPR)

Fig. II.9 illustrates a digital NPR test stimulus with a white noise source.

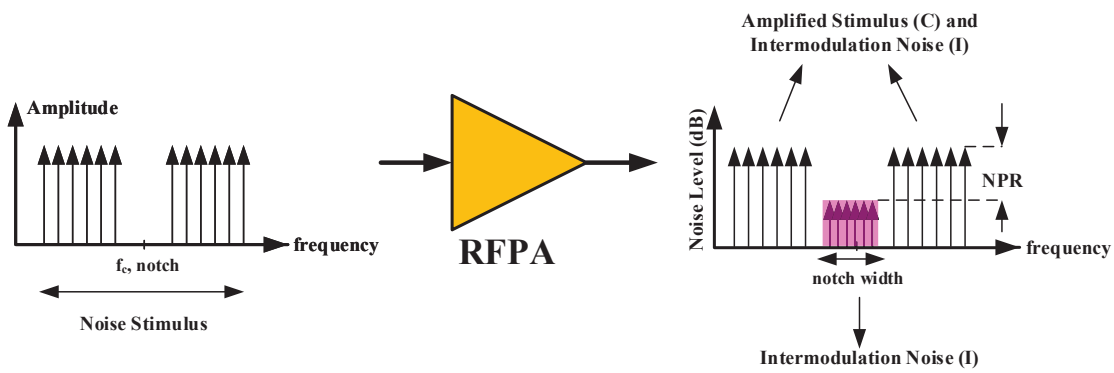

Figure II.9: A digital NPR test stimulus with white noise source connected in cascade with a bandpass filter and a notch filter. The notch depth can be measured with a Spectrum Analyzer.

The performance of high power amplifiers with many carriers (usually > 10) is normally tested using a noise power ratio (NPR) measurement technique. In this measurement procedure, Additive White Gaussian Noise (AWGN) is used to simulate the presence of many carriers of same amplitude and random phase. A gaussian white noise can be digitally generated with large number of tones having different frequencies with same magnitude and random phase (uniform distribution from 0 to 2π) [26, 27] as illustrated

in fig. II.9.

This noise signal is then transmitted at the input of the non-linear PA which will produce IMD products, which tend to fill in the notch [11]. The ratio of power outside the notch and within the notch is the Noise Power Ratio (NPR).

NPR can therefore be considered a measure of multi-carrier inter-modulation ratio (C/I). NPR differs from multi-carrier C/I in that it is the ratio of carrier plus intermodulation to intermodulation (C+I)/I.

Mathematically, NPR is expressed by the following relation:

$$NPR \quad (dB) = 10 \quad log. \left(\frac{C+I}{I} \right) \tag{II.25}$$

Error vector magnitude (EVM) and noise power ratio (NPR) measurements [28] are quite well established techniques to estimate the in-band distortion of RF power transmitters. One of the major advantage for NPR estimation over EVM is that it does not require demodulation of the transmitted signal [29].

NPR only requires power measurements in different frequency bands for multi-carrier systems and quantifies the spectral distortions falling into the operational band of the amplifier, and defines a signal-to-noise intermodulation ratio in the band.

2 High Efficiency Power Transmitter Architectures for Modulated Signals

High efficiency performances of RF power amplifiers are obtained if the transistors operate at saturation. The saturated behaviour of transistors occurs when the dynamic load line comes weakly in the ohmic region. In order to get a modulated RF power wave across a 50 Ohm output of a power wave generator, there are two possibilities which can ideally be implemented to meet the requirements of both high efficiency and linearity, as indicated in fig. II.10 (a) and (b).

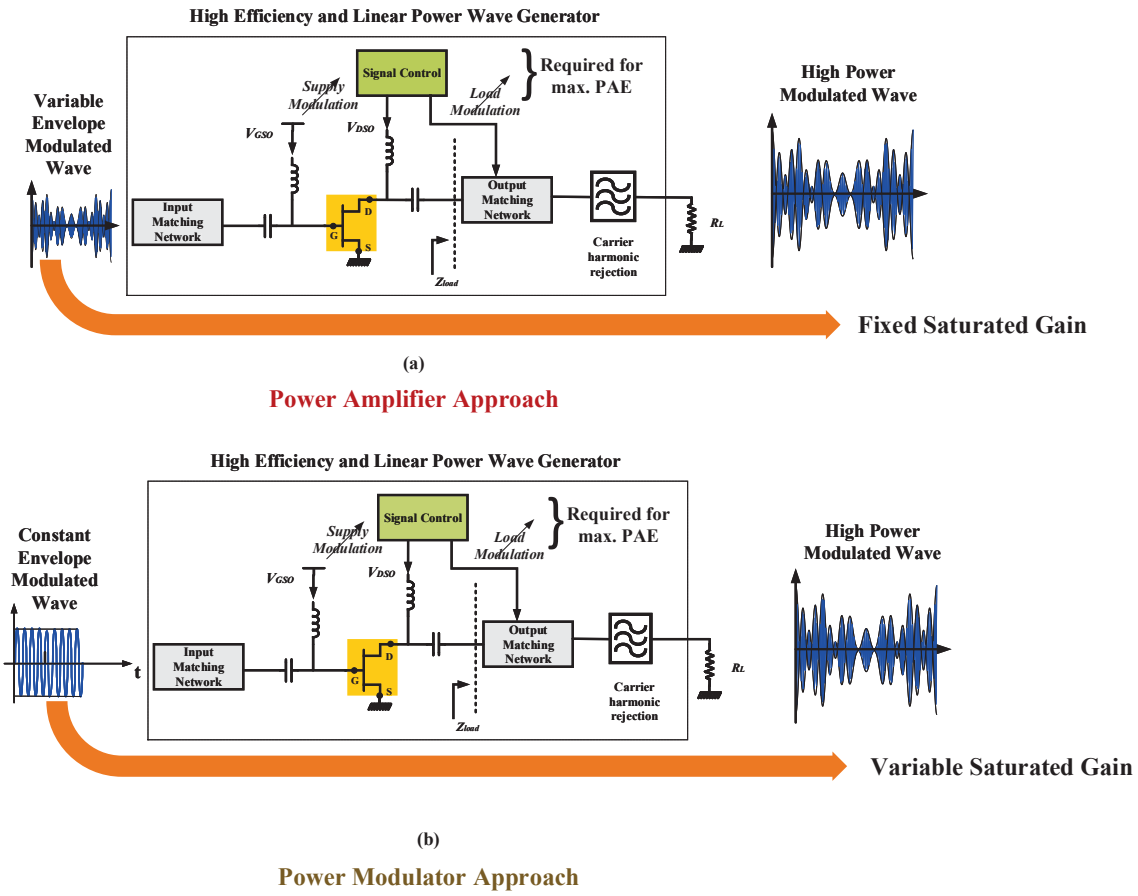

Figure II.10: General architecture of a modulated power wave generating system for modulated signals (a) fixed saturated gain and (b) variable saturated gain.

If the input power wave has a variable envelope (fig. II.10 (a)), the power wave generator must have a fixed power gain for each instantaneous envelope power of the input signal in order to generate an undistorted amplified power wave at 50 Ohm output load. To be efficient, the transistor must operate with a fixed saturated gain. This can be achieved if the drain bias voltage or the load impedance varied using an appropriate signal control. If this signal control acts on the drain bias voltage, we get envelope tracking architecture. If the signal control acts on load impedance, we get load modulation architecture.

On the other hand, if the input power wave has a fixed envelope (fig. II.10 (b)), that is only phase modulation, the power wave generating system must have a variable gain to reproduce the required amplified modulated power wave at 50 Ohm output load. To be efficient, the transistor again must operate at saturation and therefore the system must operate with a Variable Saturated Gain and gain variations must be linear with large dynamic range. This can also be achieved using an appropriate signal control to make drain bias or load impedance variations. If the signal control acts on the drain bias voltage, we

get Envelope Elimination and Restoration (EER) architecture and if the signal control acts on the load impedance, we get outphasing architecture.

The system shown in fig. II.10 (a) can be qualified as a power amplifying system whereas the system shown in fig. II.10 (b) can be qualified as a power modulator system. In both the cases (fig. II.10 (a) and (b)), the signal control can be monitored by the envelope or baseband signal (Envelope Tracking, EER or passive load modulation using varactors in the output matching network) or the control can be achieved by the RF signal (Doherty and outphasing architecture) which requires at least two RF amplifying cells.

2.1 Load Modulation Technique and Doherty Architecture

This part of the chapter is dedicated to a general overview of high efficiency transmitter architectures based on load modulation.

2.1.1 Principle of Doherty Technique

Fig. II.11 gives the general schematic for the static CW simulation of a GaN transistor (Wolfspeed 25 W) with a load tuner showing the power characteristics for three different load impedances. The transistor is biased at V_{gso} = -2.8 V and V_{dso} = 50 V.

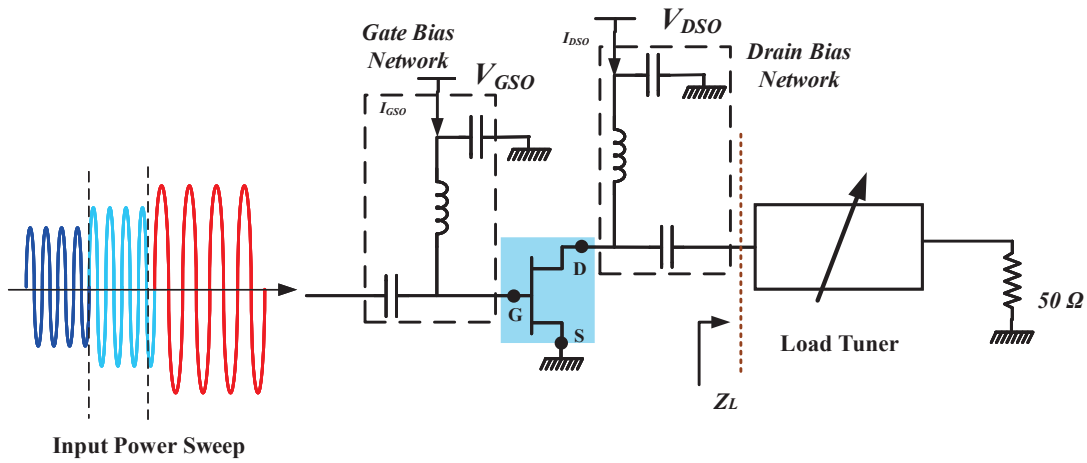

Figure II.11: General schematic of an RFPA with a load tuner demonstrating load variation for three different input power levels.

Fig. II.12 shows the shape of Power Added Efficiency as a function of output power

for three different load impedances A, B and C.

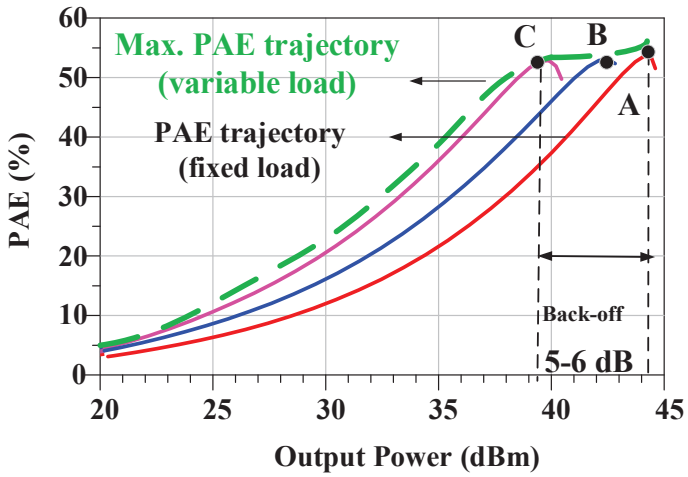

Figure II.12: Power Added Efficiency as a function of output power for three different load impedances A, B and C.

Fig. II.13 shows the intrinsic load lines at maximum input power levels corresponding to the beginning of the output power saturation for each cases A, B and C respectively. We can see that the load line with higher slope provides high efficiency at high output power whereas the loadline with lower slope provides the best efficiency at back-off. This illustrates that load modulation is necessary to maintain high efficiency performances on an output dynamic range of about 6-dB back-off.

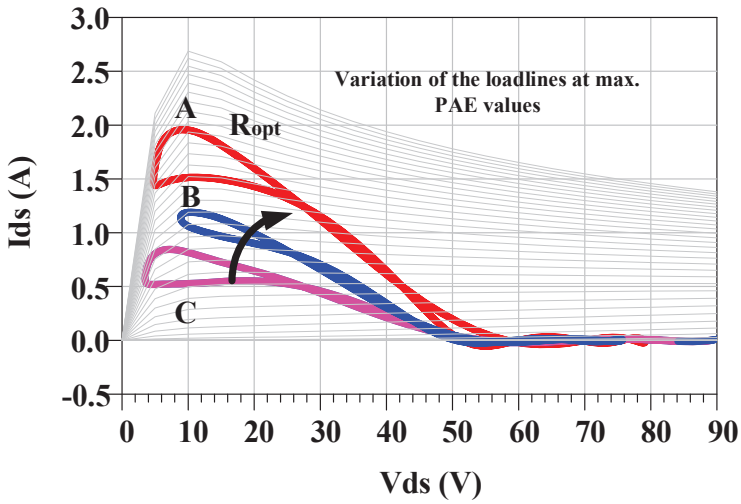

Figure II.13: Intrinsic loadlines corresponding to three different load impedances A, B and C.

Fig. II.14 shows the gain shape (corresponding to input power) obtained when the load impedance varies to get the maximum PAE trajectory. It can be observed that although high efficiency at back-off is achieved, gain flatness is poor indicating poor linearity and the need for a digital predistortion to meet linearity specifications in Doherty architecture.

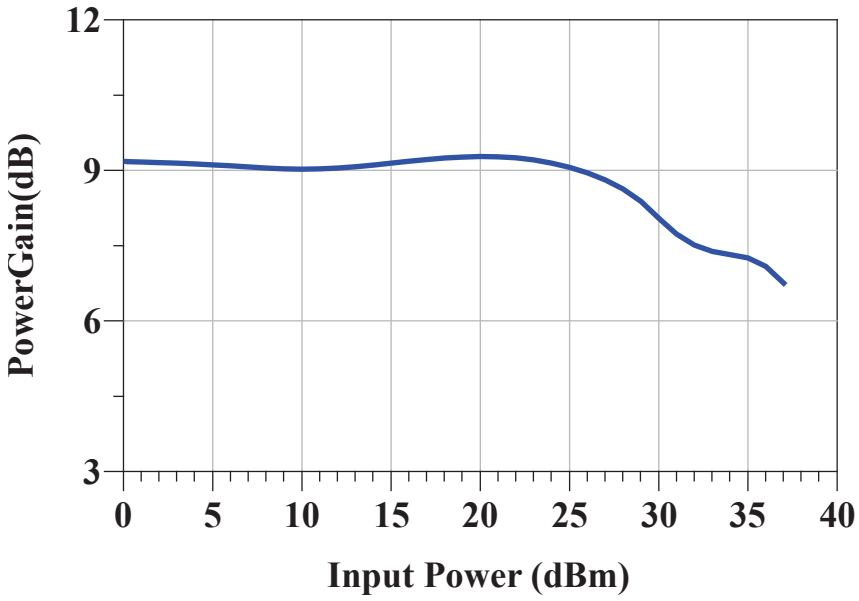

Figure II.14: Gain shape for varied load impedances versus input power.

2.1.2 Implementation of the Doherty Principle

The Doherty architecture for power amplifiers was first proposed by W.H Doherty [30] from Bell Labs. Corp. in the year 1936 for efficiency improvement of microwave tubes and RF-PAs. The Doherty PA technique involves the approach for active load modulation of a main transistor by the use of an auxiliary transistor. The implementation of active load modulation requires two transistors represented in fig. II.15 by their ideal drain current sources at fundamental frequency respectively I_m for the main and I_a for the auxiliary respectively.

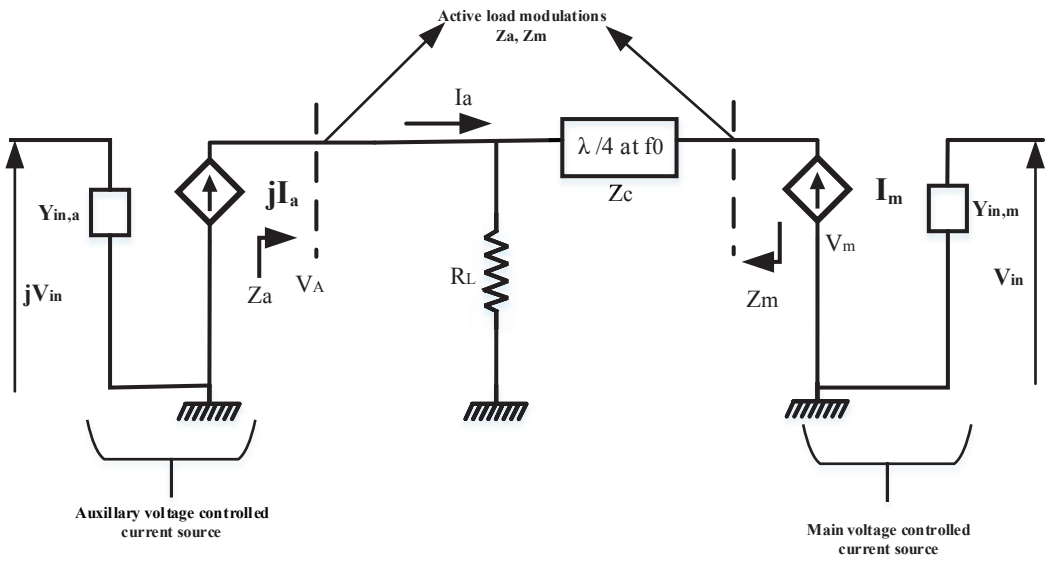

Figure II.15: Principle of Active Load Pull in Doherty Technique.

The main (I_m) and the auxiliary (I_a) current sources are voltage controlled by an input gate to source voltage, V_{in}. They are connected to a common load, R_L through a quarter-wave transmission line with a characteristic impedance of Z_C which provides a transmission phase shift of 90^0 between the currents flowing from the main and the auxiliary devices respectively. For an in-phase combination of currents in the common load R_L, the phase shift between the two current sources must be 90 degrees. The auxiliary Power Amplifier (I_a) is in off state when the power level is very low. As the power level increases the current in the auxiliary amplifier increases thereby leading to a variation in the optimal load due to the load-pulling effect discussed previously.

Generally, the auxiliary device is assumed to turn ON at a specific input power level (transition voltage, V_T), typically some portion backed-off from the maximum total power of the Amplifier, and then it starts to generate the current Ia that increases until it reaches almost the same maximum value of I_m at maximum power of operation. Typical voltage and current variations versus input voltage V_{in} are shown in fig. II.16.

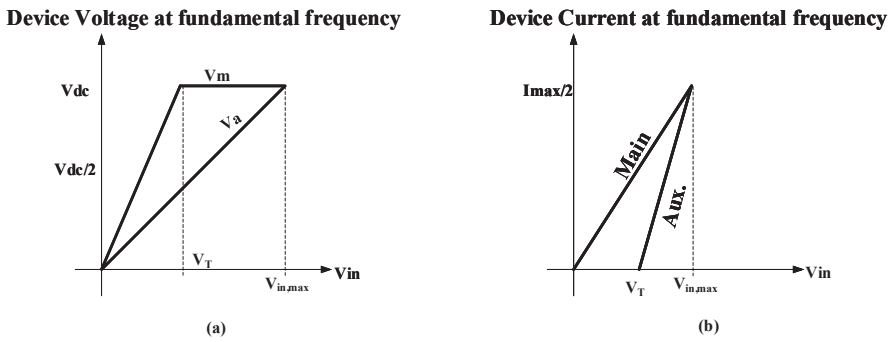

Figure II.16: (a) Voltage and (b) current combination for the main and auxiliary transistors.

This principle is exploited in the architecture shown in fig. II.17 which illustrates conventional Doherty power amplifier and the loadlines associated with main amplifier.

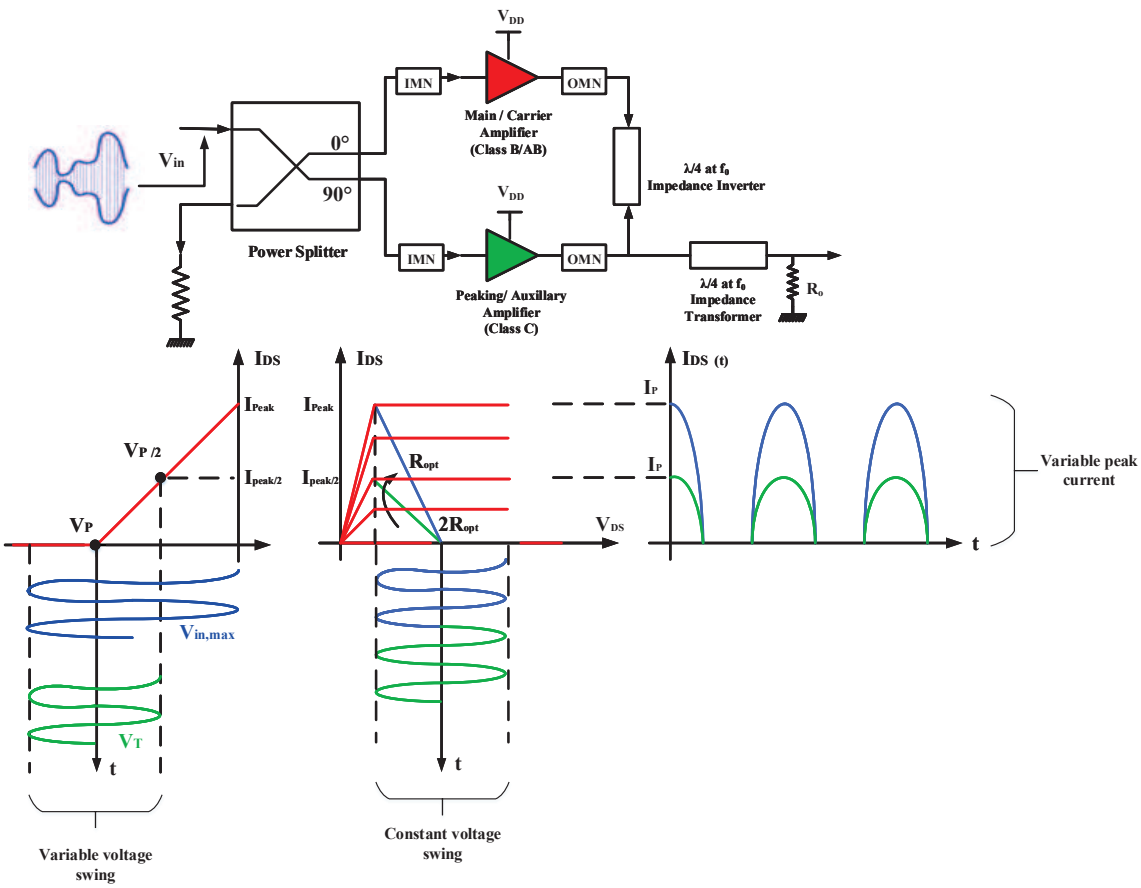

Figure II.17: Conventional Doherty Architecture and Ideal piecewise linear I/V characteristics of the voltage controlled drain current source along with voltage and current waveforms and associated loadlines for the Main Amplifier.

The basic Doherty amplifier consists of two amplifier circuits which are biased differ-

ently, that is $V_{dso,main} = V_{dso,auxiliary}$ whereas $V_{gso,main}$ is not equal to $V_{gso,auxiliary}$. The main amplifier is biased in class B whereas the auxiliary is biased in class C. The main objective of Doherty technique is to dynamically modulate the load impedance seen by the main amplifier to enable the overall amplifier to operate at saturation always (from $V_{in} = V_T$ up to $V_{in} = V_{in,max}$), that is V_{ds} swing remains constant as shown in fig. II.17.

For low to medium input power levels (from $V_{in} = 0$ to V_T), the main amplifier operates till it reaches saturation (loadline with slope $2R_{opt}$ enters in the ohmic region) whereas the auxiliary amplifier is off. As the input power is further increased ($V_{in} > V_T$), the auxiliary amplifier is turned on as the input signal reaches beyond the pinch-off due to the increase in input power, leading to current flow in the load. Due to this action, the load seen by the main amplifier is varied from $2R_{opt}$ to R_{opt} thanks to the impedance inversion property of the quarter-wave transmission line, leading to high efficiency up to maximum output power.

2.1.3 Limitations in Doherty Power Amplifier Implementation

One of the main challenge in Doherty PAs is the instantaneous bandwidth limitation of the circuit due to the quarter-wave impedance inverter at the output. As the quarter-wave inverter is frequency dependent, therefore it has a fixed topology and it becomes a challenging aspect to provide frequency flexibility or to shift the operation of the DPA from one frequency band to another. Several solutions have been proposed in order to tackle the frequency dependent character of the quarter-wave transmission line analog topology.

One of the promising technique is the digitally-assisted Doherty [31] where the input amplitude and phase is controlled digitally using digital signal processing blocks (DSP). This provides additional degree of freedom at the output of the combiner enabling digital control of the phase misalignment ensuring an optimal Doherty performance [32]-[33], like a reconfigurable circuit.

Fig. II.18 shows an example setup for the digitally assisted Doherty PA. Magnitude and phase of the two input signals are monitored digitally to improve the overall PAE performances [34].

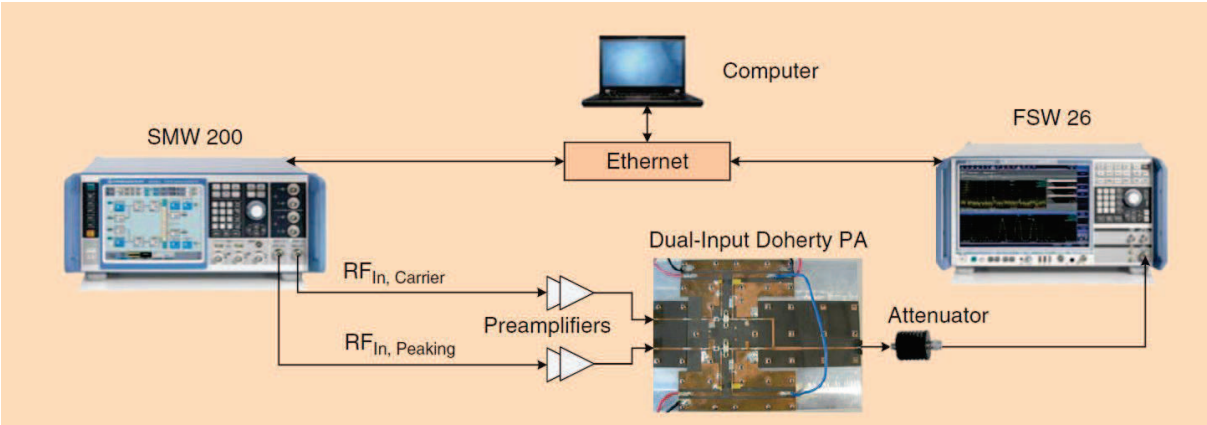

Figure II.18: A mixed-signal demonstrator setup for the digitally equalized Doherty PA ([32]).

As the modern communication signals are getting more complicated, it also raises the PAPR, therefore one solution to improve the output power range at maximum PAE (up to 9 dB for example) is to use Asymmetrical Doherty [35] where the auxiliary amplifier is of a bigger size than the main amplifier. This enhancement involves a wider load modulation range, however at the cost of slightly lower average efficiency because of the power dissipated due to the large size of the class C biased auxiliary transistor when it begins to turn on.

Another solution to improve the load modulation is to adjust the gate bias of the peaking PA (gate envelope tracking) [36]. The principle objective is to gradually modify the gate bias of the peaking PA. This technique offers the possibility to make the power gain shape of Doherty amplifiers more flat versus input power to improve the linearity performance.

2.2 Envelope Tracking Technique

Envelope Tracking (ET) [37] is another commonly used technique to address the average efficiency enhancement of RF Power Amplifiers. In this technique, the drain bias voltage is varied according to the instantaneous envelope power variations at the input of the RF power amplifier. That is the drain bias voltage is lowered for lower input power level and raised for higher input power level.

2.2.1 Principle of Envelope Tracking Technique

Fig. II.19 gives a general schematic for the static CW simulation of a 25 W GaN transistor with fixed load impedance and variable drain bias voltage showing power characteristics for three different drain bias voltages respectively.

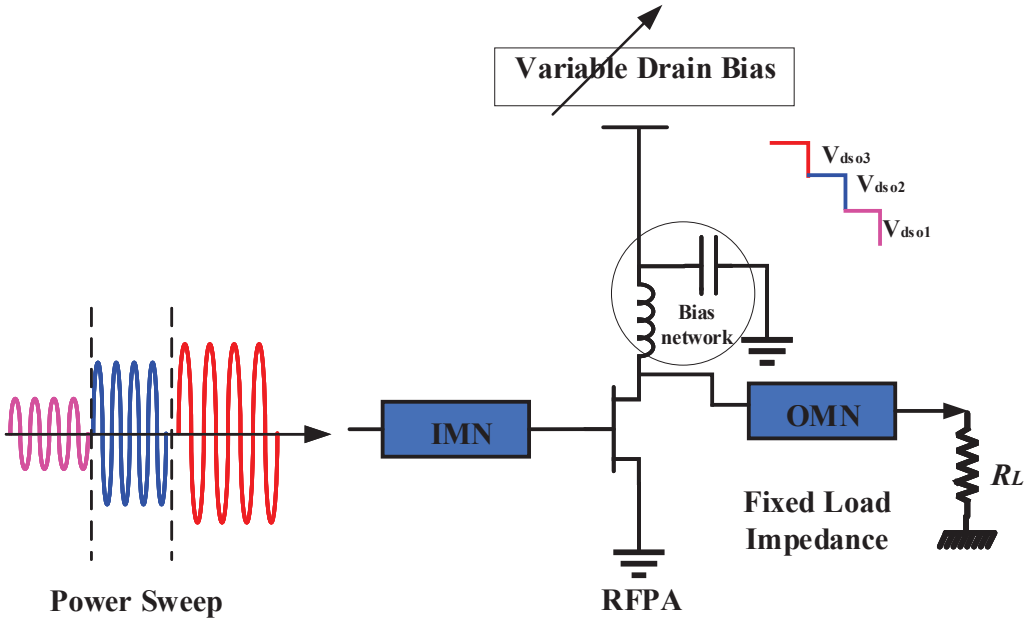

Figure II.19: General schematic of a Wolfspeed packaged GaN 25 W transistor RFPA with a fixed load impedance and variable drain bias voltage demonstrating envelope tracking principle for three different input power levels.

Fig. II.20 (a) shows the shape of PAE versus output power for three different drain bias voltages, 20V, 30V and 40V respectively at center frequency of 2.5 GHz. Fig. II.20 (b) shows the intrinsic loadlines corresponding to maximum PAE (points 1, 2 and 3) for each drain bias voltage. PAE performances can be ideally improved by 10 to 20 points if the drain bias voltage is lowered when the output power decreases as compared to the PAE performances obtained at fixed drain bias voltage of 40 V.

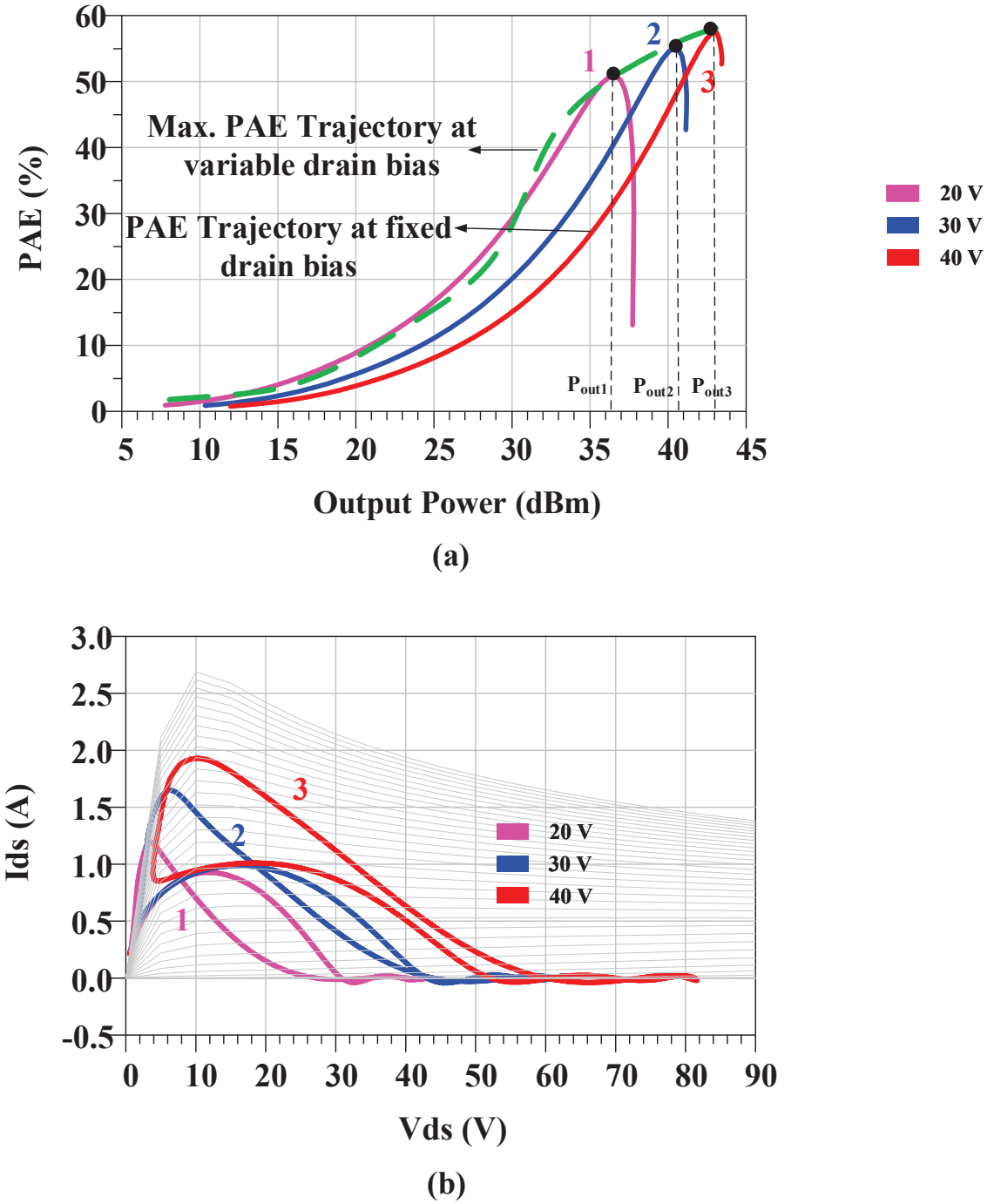

Figure II.20: (a) Corresponding simulated PAE performances as a function of output power, indicating the optimum trajectory for maximum PAE and (b) Intrinsic loadlines for three drain bias voltage.

To get the maximum PAE trajectory at variable drain bias, V_{dso} versus input power P_{in} control law should be the one represented in fig. II.21.

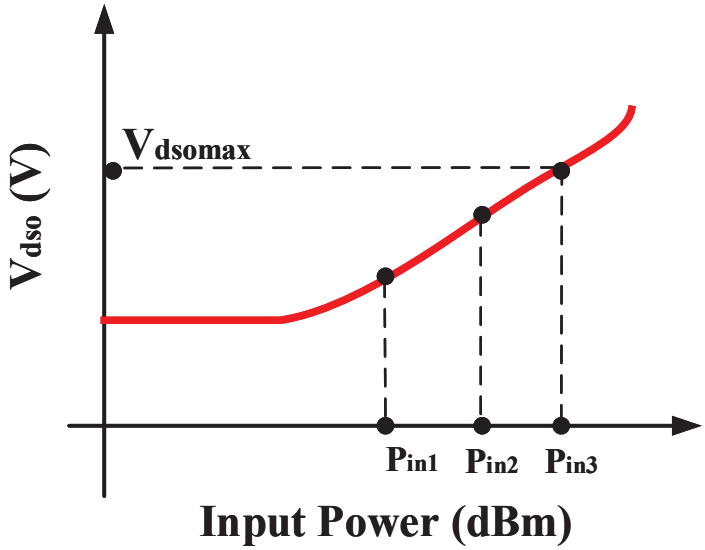

Figure II.21: Drain bias law versus input power to get the maximum PAE trajectory .

Fig. II.22 shows the simulated quasi-static gain characteristics as a function of output power. The power gain shape plotted in dotted lines is obtained when the variation of drain voltage V_{dso} versus the input power follows the curve shown in fig. II.21. One can obtain by principle a linear quasi-static gain as depicted by the dotted line indicated in fig. II.22.

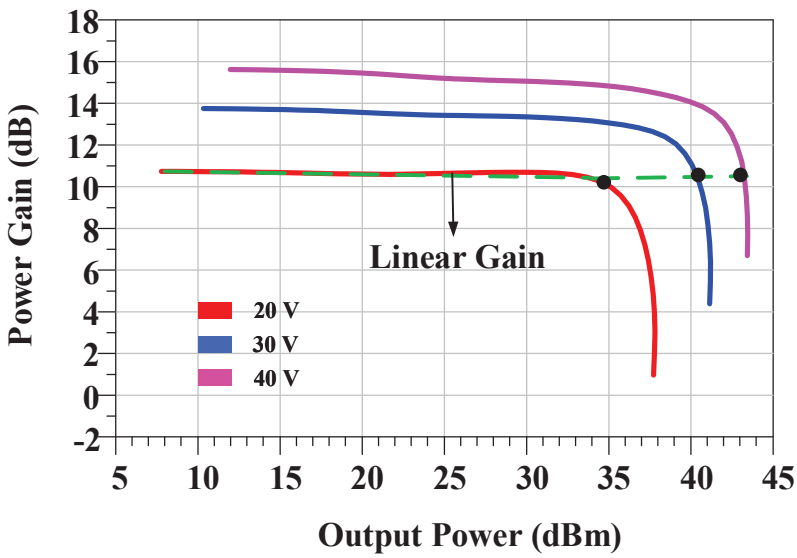

Figure II.22: Simulated CW gain characteristics as a function of drain output power with the optimum trajectory corresponding to linear gain at different drain voltages.

Hence, it can be deduced that supply modulation technique could prove to address linearity and efficiency optimization necessary for power transmitter designers however there are certain design issues associated with practical implementation of such a system which are addressed in the following subsection.

2.2.2 Implementation of Envelope Tracking Architecture

Fig. II.23 shows a simplified architecture of an envelope tracking amplifier consisting of an RFPA and a supply modulator [38]-[39]-[40]-[41]. The switching between different bias voltage is provided with a combination of a pulse width modulator and a power switch (Buck or Boost DC-DC converter) with a low pass filter.

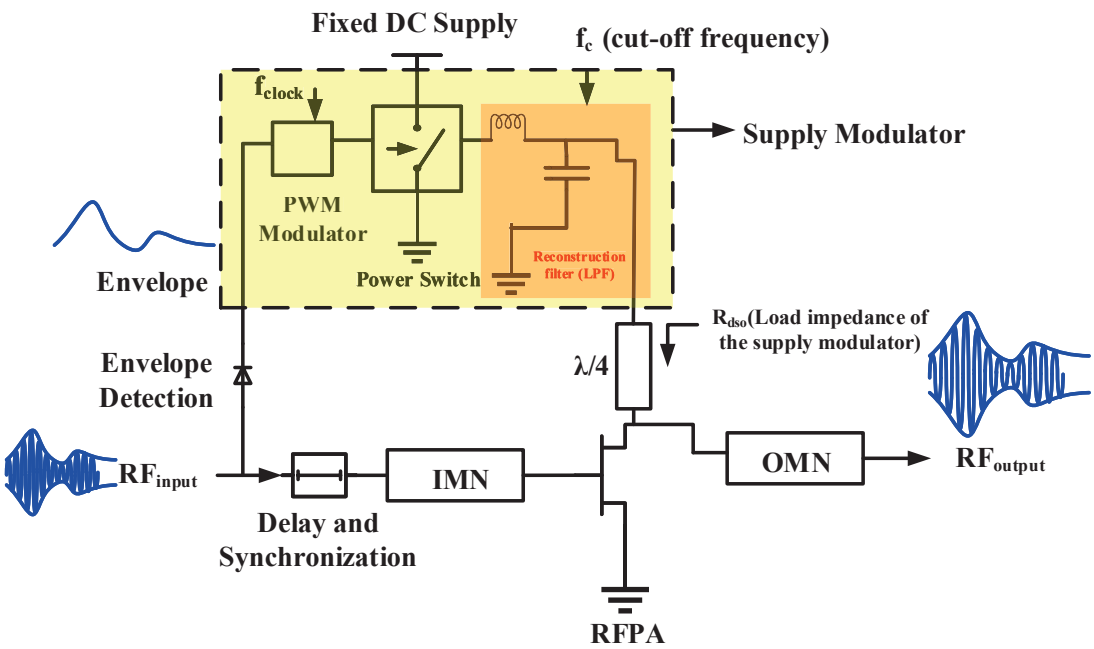

Figure II.23: Simplified architecture of Envelope Tracking amplifier

The PWM modulator has a clock frequency f_{clock} which must be 6 to 7 times greater than the cut-off, f_c frequency of the low path reconstruction filter, in order to reproduce the continuous envelope signal monitoring the drain bias of the RFPA. The envelope signal that drives the PWM circuit input is extracted with the help of an envelope detector.

2.2.3 Major Design Challenges in Conventional ET Implementation

When the drain voltage is varied dynamically, the drain impedance R_{dso} presented by the drain port of RFPA to the supply modulator varies and follows the black dotted line curve. The resulting mismatch between the supply modulator and the RFPA is one of the main source of the overall efficiency degradation [42] (fig. II.24).

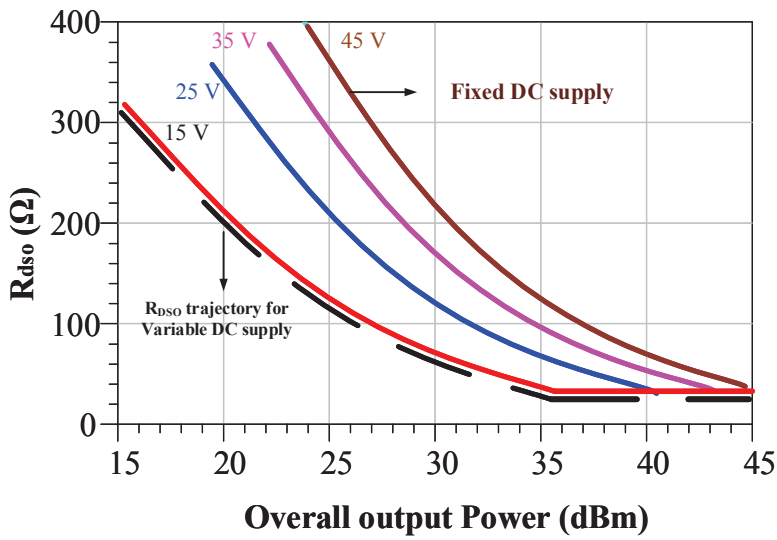

Figure II.24: Simulated values of drain resistance R_{dso} as a function of output power.

As the overall efficiency of the system is a product of the individual efficiencies of the RFPA and the supply modulator ($\eta_{total} = \eta_{RFPA} \cdot \eta_{SM}$), it is necessary to implement a supply modulator with high efficiency (at least 80 %) and high switching speed.

The third critical issue to be addressed is the bandwidth of the supply modulator for high power and high speed applications. The bandwidth should be sufficiently high to replicate the envelope at the output according to the incoming signal. This also leads to control and provide proper timing alignment and synchronization between the input and output respectively.

2.3 Outphasing Technique

2.3.1 Principle of Outphasing

The principle of Outphasing [34] technique is shown in fig. II.25.

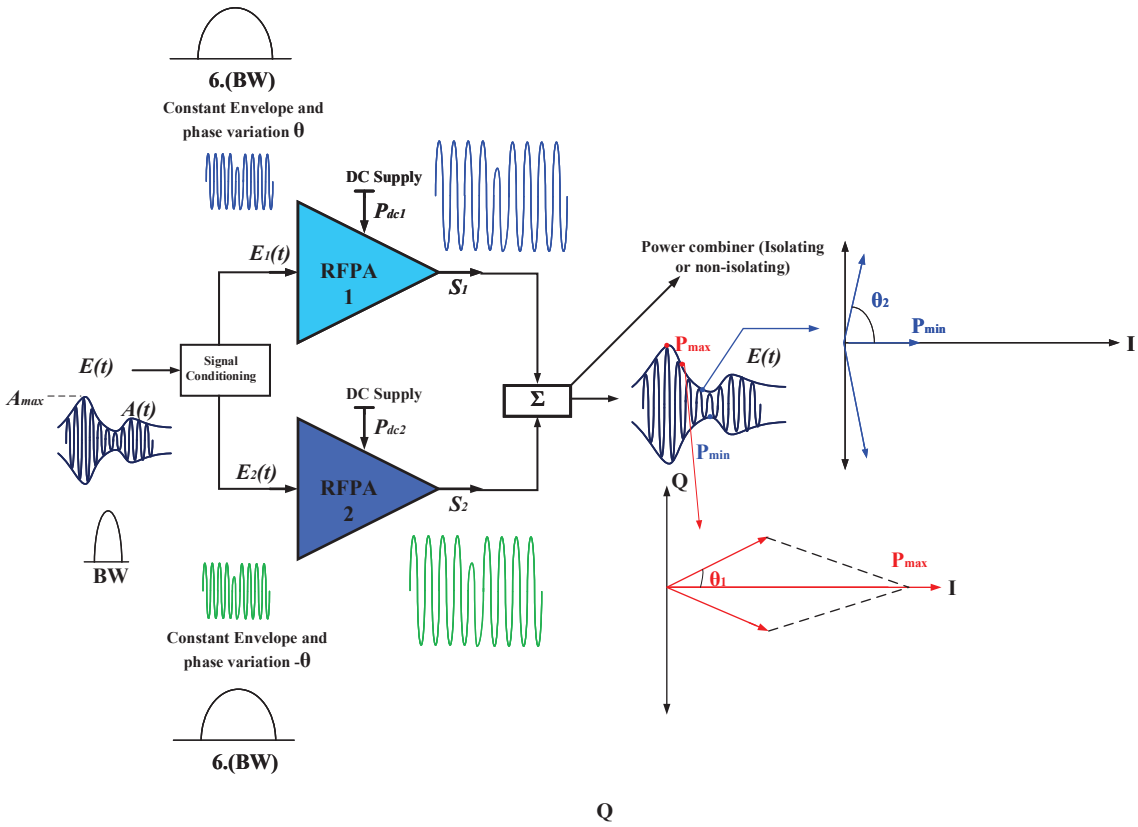

Figure II.25: Simplified block diagram of an outphasing transmitter architecture.

In outphasing technique, a complex modulated and envelope varying input signal is divided and processed into two individual and envelope constant CW signals E $_1$(t) and E_2(t) according to Fresnel representation shown in the same figure. The signal decomposition function is performed at the input by signal conditioning [43].

As only phase modulated signals drives both the amplifiers, it is possible to implement amplifiers that operates at saturation. The input signal E(t) in outphasing transmitter architecture can be expressed by the following relation :

$$E(t) = A(t)cos[\omega_0 t + \varphi(t)] \tag{II.26}$$

which can be rewritten as

$$E(t) = \frac{A_{max}}{2} cos[\omega_0 t + \varphi(t) + \theta(t)] + \frac{A_{max}}{2} cos[\omega_0 t + \varphi(t) - \theta(t)] \quad \text{(II.27)}$$

that is E(t) = E_1(t) + E_2(t)

where θ(t) = Arc cos($\frac{A(t)}{A_{max}}$)

An important feature and drawback is that if the input signal E(t) has a bandwidth BW, E_1(t) and E_2(t) have an increased bandwidth of approximately six times BW. If the gain, G of both the RFPA is constant over entire 6.BW, then,

$$S_1(t) = G.E_1(t) \quad \text{(II.28)}$$

$$S_2(t) = G.E_2(t) \quad \text{(II.29)}$$

The output signal then can be represented as:

$$S(t) = G[E_1 + E_2] \quad = GE(t) \quad \text{(II.30)}$$

where G is the gain of the amplifiers and θ(t) is the outphasing angle and φ(t) is the phase of the baseband signal respectively.

2.3.2 Implementation of Outphasing Architecture

Unlike in Doherty PA, where load modulation is achieved through turning on both main and auxiliary PAs at different power conditions, in outphasing amplifiers: load modulation is achieved by keeping the PAs at peak power and by generating a phase shift. Outphasing architecture utilizes two separate amplifying cells and an output combiner to restore a linear output amplitude modulated power. In the case of an isolating power combiner, the output signal is restored with good linearity performances. Nevertheless, to avoid output power losses occurring in an isolating power combiner (Wilkinson combiner for example), a non isolating power combiner must be used, as shown in fig. II.26.

Fig. II.26 shows a general schematic for the static CW simulation of two packaged GaN 25 W transistors from Wolfspeed connected in parallel by a simplified non-isolating

combiner topology, with fixed input power and drain bias voltage for maximum PAE for four different values of phase angles respectively.

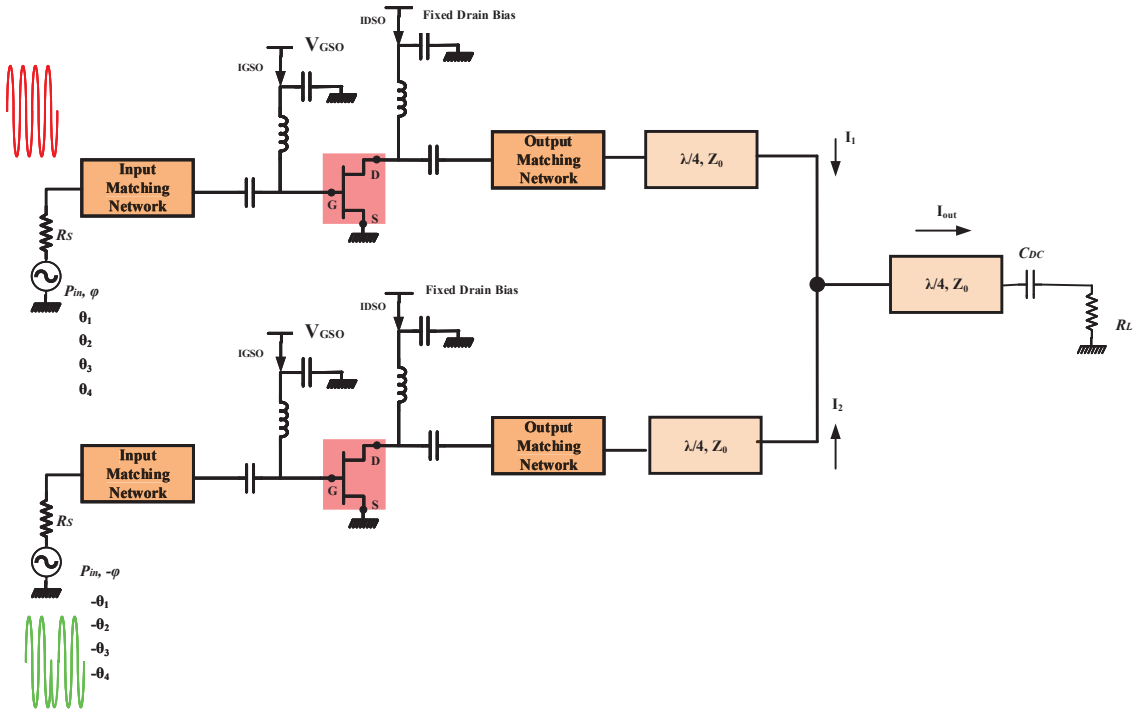

Figure II.26: General schematic of an outphasing principle with a non-isolating power combiner.

Fig. II.27 shows the intrinsic loadlines at maximum PAE and fixed input power for four different outphasing angles θ_1, θ_2, θ_3, θ_4. It can be observed from the figure that the loadlines corresponding to the best efficiency is achieved when the outphasing angle is 0 degrees that is when both the input signals are in phase and loadlines tends to open when the phase angle increases leading to poor efficiencies for high θ values (between 50 to 90 degrees).

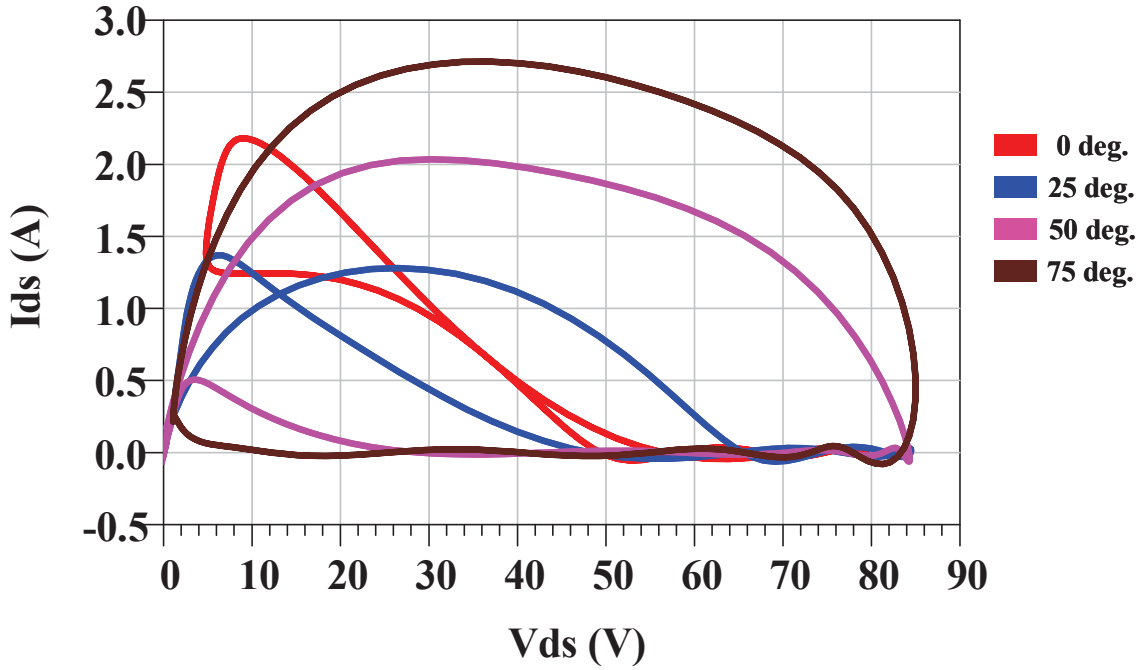

Figure II.27: Intrinsic loadlines at maximum PAE and fixed input power for four different outphasing angles.

2.3.3 Design Issues with Outphasing Architecture Implementation

Although outphasing transmitter architecture is capable of providing high efficiency only for low outphasing angles ($\theta < 30$ degrees), it has still not being widely implemented in commercial applications because of stringent phase alignment requirements between the two signal components at the input and the losses encountered at the output due to the passive power combiner. Conventional outphasing architecture is able to provide high efficiency performances only for low PAPR values (2-3 dB). The bandwidth of the combiner is also a problematic issue. Several techniques have been implemented to minimize the outphasing angle in order to compensate for the phase distortion (active compensation) termed by investigating different combiner topologies and a combination with envelope tracking [44, 45, 46, 47, 48, 49], however leading to very complex circuit architectures. There are also stringent requirements for higher outphasing angles as it is evident that wide opening of loadlines lead to high power dissipation of the transistors at back-off.

2.4 Envelope Elimination and Restoration (EER)

2.4.1 Principle of operation of EER Technique

Fig. II.28 shows a general schematic for the static CW simulation of a packaged GaN 25 W transistor from Wolfspeed, with fixed load impedance and input power and variable drain bias voltage V_{DD} for the analysis of EER principle.

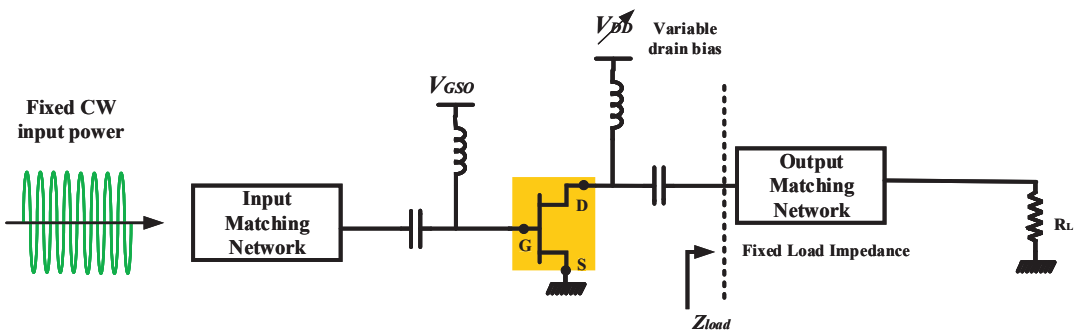

Figure II.28: General Schematic of a 25 W GaN transistor based RFPA with fixed input power and variable drain bias.

The principle of operation of EER is illustrated by fig. II.29 which shows the simulated PAE and output power characteristics of Wolfspeed 25 W packaged GaN transistor for three different drain voltage values, 20V, 30V and 40V respectively matched for maximum PAE.

The operational region of the RFPA in EER technique is at a fixed input power P_{in} depicted by dotted line in fig. II.29 (a).

For this fixed input power (30 dBm), the output power varies if the drain bias voltage V_{DD} is varied from 20 V to 40 V. The resulting power gain variation versus V_{dso} is plotted in fig. II.29 (b). It can be observed that only 5 dB gain variations can be obtained which is not sufficient for the generation of output power wave having PAPR of the order of 10 dB. Furthermore, from fig. II.29 (a), it can be observed that maximum PAE performances are not achieved at 20 V.

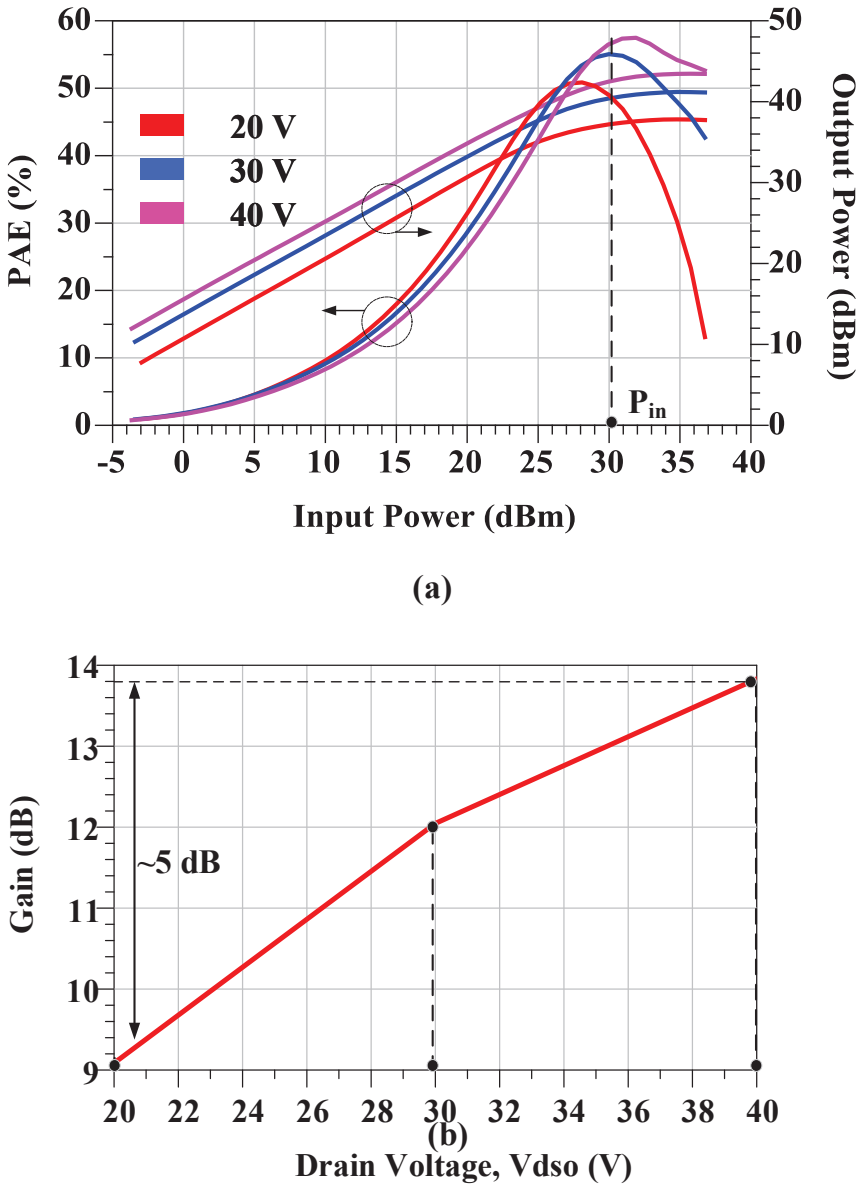

Figure II.29: Simplified principle of operation for EER technique (a) PAE and output power as a function of input power and (b) Gain variation as a function of drain voltage.

2.4.2 Implementation of EER Technique

The operational region of the the RFPA in EER technique is always at saturation. In EER technique [50]-[51], the modulated signal is divided into the envelope (amplitude information) and a phase modulated CW signal which is used as an input of an RFPA as shown in fig. II.30 . The supply modulator on the other hand produces an output voltage which varies accordingly with the instantaneous envelope of the incoming RF signal.

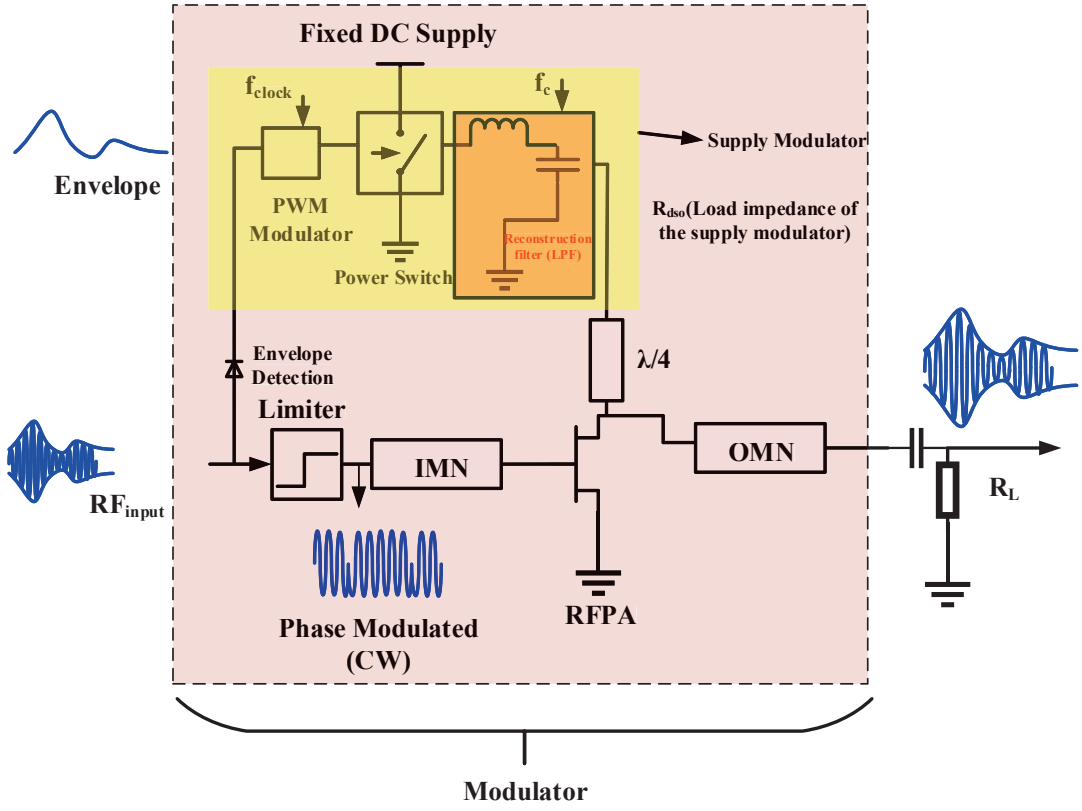

Figure II.30: Architecture of Classical EER Transmitter with separate amplitude and phase information.

The restoration of the amplitude variations of the output power wave is achieved thanks to the V_{DD} variations. The working principle of EER is based on the idea that high efficiency power supply (envelope amplifier) could be used to modulate the envelope of highly efficient non linear power amplifiers (switched mode RFPA's for example). Because of separate amplitude and phase processing, EER is sometimes also referred as the polar transmitter architecture [52, 53].

The linearity of the overall EER system depends on the delay between amplitude and phase paths which may cause distortion along with the V_{DD}-PM conversion factor of the RFPA as well.

2.4.3 Major Design Challenges in Conventional EER Implementation

There are several design issues associated with the practical implementation of EER technique. Therefore to make a highly efficient amplifier, conventional EER architectures usually use switch mode (class-E) power amplifiers in the RF chain. The main constraint

associated with switch mode power amplifiers is although they are highly efficient, but the multiple resonances provided by the implementation of harmonic control circuits limits their bandwidth. This in turn is a limiting factor for the bandwidth of the overall system. Therefore for a wideband system, multiple RFPA's have to be implemented which increases the system complexity.

Fig. II.31 shows the variation of drain resistance R_{dso} as a function of drain supply voltage V_{dso}. The variation of R_{dso} is less as compared to Envelope Tracking indicating the suitability of this technique more for power modulator approach.

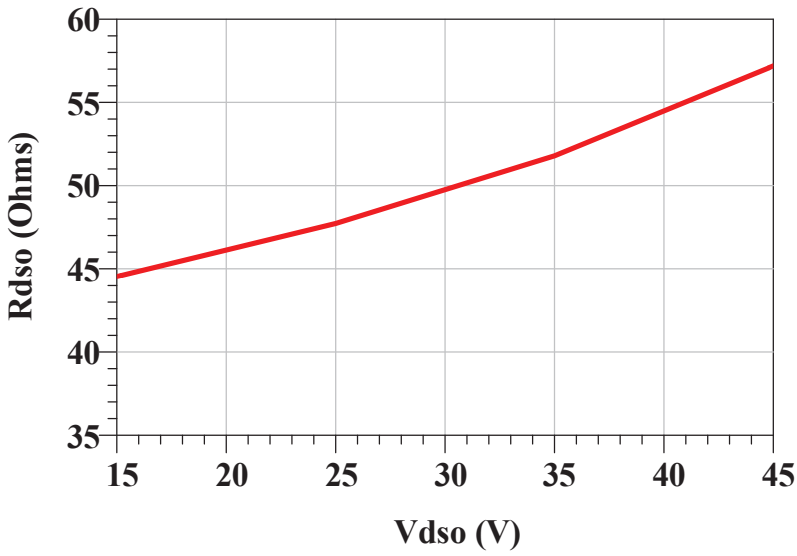

Figure II.31: Variation of R_{dso}versusV_{dso}.

Proper timing alignment and synchronization between the amplitude (envelope) and phase paths during reconstruction of the RF signal at the output still remains a challenge for practical EER system implementation. In present architectures, some form of signal feedback needs is used to adjust the time delay [54]. Linearity of the supply modulator is also an important issue to be taken care of in order to minimize the envelope distortions along with V_{DD}-PM conversions of the RF power amplifier. This requires several advanced predistortion techniques [55].

3 Conclusion

This chapter of the thesis has briefly covered some of the important figures of merit for complex modulated signals exhibiting high Peak to Average Power Ratio (PAPR). This chapter has also presented some of the existing advanced power transmitter architectures implemented for higher transmitter efficiency based on load modulation and supply modulation respectively. However, these existing architectures have their own design issues and challenges in implementation in terms of complexity, efficiency and wideband capabilities.

As it has been explained before that in EER, it is only possible to achieve a maximum 5 dB output variations with efficiencies lower at lower V_{dso} values. The solution to this issue has been attempted to investigate as a part of this thesis work where a modified version of EER has been proposed. This new GaN based architecture is based on Saturated Variable Gain (SVG) approach providing high dynamic range of over 10 dB always at peak efficiencies.

To address these trade-offs and to converge to a potential solution, in this thesis, a possible attractive solution using supply modulation technique for the development of next generation communication systems has been examined. This approach is based on the merging of digital modulation and DC to RF energy conversion functions into a single compact mixer-less module. A novel vector power modulator approach is proposed to improve linearity-efficiency and reconfigurability trade-offs in transmitters. By taking the advantages of high voltage 50 V GaN technology, a concept demonstrator has been built and validated with a specific laboratory test bench. The design procedure and the associated performances are illustrated in Chapter-3 of this thesis.

Chapter III

Design and Characterization of S-Band GaN RF Vector Power Modulator

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1 Motivation

The role of modern communication satellite technology [56, 57, 58, 59] is essential to receive a set of up-coming signals from earth gateways, perform a frequency translation and amplify signals to be sent to ground equipment. This signal regeneration performed by each transponder is based on separated HF blocks (e.g. mixers, filters, amplifiers) that are used to produce in an ideal case, a linear, stepped-up transposition of the original information.

In conventional power transmitter architecture, the final High Power Amplifier (HPA) is used to boost up the power of the output HF signal, and its DC-RF energy efficiency conversion is strongly impacted by the signal's properties (eg. Peak to Average Power Ratio - PAPR, Probability Density Function - PDF and bandwidth).

Extensive research has been conducted on Solid State Power Amplifier (SSPA) and HPA technology so far with an objective to improve the energy efficiency of RF/HF terrestrial terminals when employing modulated signals with complex architectures such as Envelope Tracking, Envelope Elimination Restoration [60]), Doherty and outphasing [30]-[34]-[61]. Also they were revealed very effective to mitigate the energy consumption expansion for typical narrowband point to point or point to multi-point microwave backhauling. They rely on linear baseband to RF frequency transposition approach that inherently put stringent constraints on HPA's efficiency in case of wideband and high PAPR driving conditions.

This chapter of the thesis therefore is dedicated to the design procedure and implementation of a novel microwave circuit that implements direct base-band-to-RF conversion and RF power amplification. This circuit converts a digital base-band data stream into analog modulated power waves with high dynamic range. It is based on the combination of digital modulation and DC-to-RF energy conversion functions into a compact GaN based mixer-less circuit, and appears very suitable for wide-band transponders in the context of regenerative satellite communication, taking advantage of their on board processing capabilities. An hybrid demonstrator circuit which is composed of a two-stage high efficiency saturated variable gain circuit and a multi-level discrete supply modulator has been built and experimentally validated for a 20 W average output power 16-QAM modulated signal generation at S-band frequencies. The design of a two-stage high efficiency circuit is the main work presented in this thesis. The supply modulator [62] has been the purpose of another task achieved by Anthony Disserand in his PhD work.

2 Principle of the Vector Power Modulator

The following section and its parts highlight the general architecture of the Vector Power Modulator circuit and the requirements of a two-stage circuit.

2.1 General Architecture

Fig. III.1 illustrates the conventional transmitter architecture.

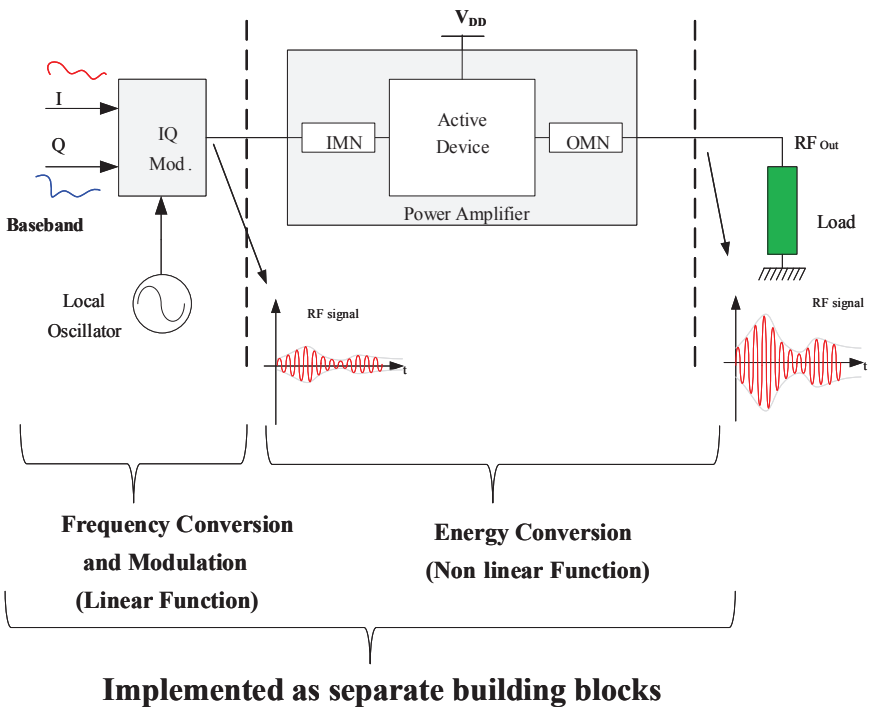

Figure III.1: Conventional transmitter architecture.

In this conventional approach, the modulation function and energy conversion function are designed and implemented as separate building blocks to provide a modulated power wave at the output. The modulation and up conversion process is designed to be very linear. The DC to RF energy conversion is achieved by the power amplifier (whose behaviour must be non-linear) to have good efficiency performances. To meet the linearity specifications of the overall transmitter, a digital predistortion of the baseband signal is generally performed.

The purpose of the work described in this chapter is to merge both modulation and energy conversion functions within the same module as illustrated in fig. III.2.

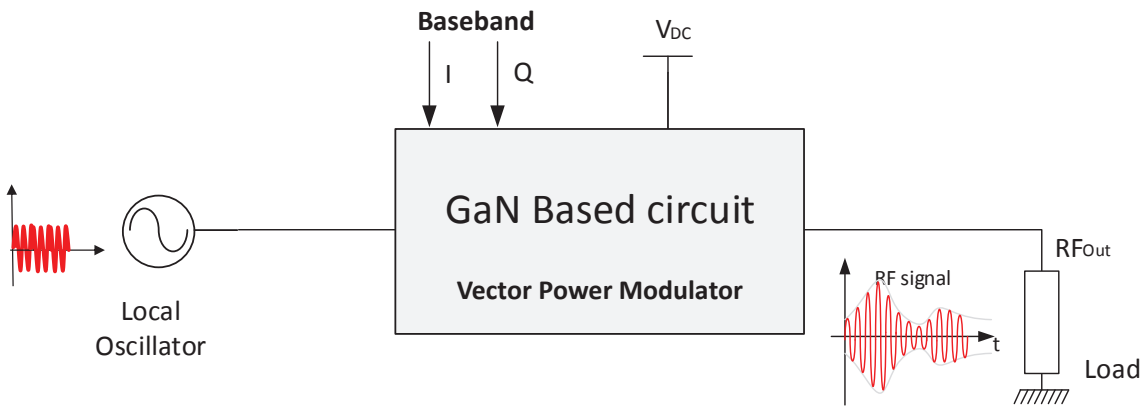

Figure III.2: Proposed GaN based Vector Power Modulator.

The proposed approach is to design a GaN based high efficiency Vector Power Modulator circuit to generate a modulated power wave at the output. Compared to the conventional approach shown in fig. III.1, the proposed approach is mixerless. This design approach has been carried out by taking the advantages of high voltage (50 V) GaN-HEMT [63] technology. The working principle of the proposed Vector Power Modulator is shown in fig. III.3.

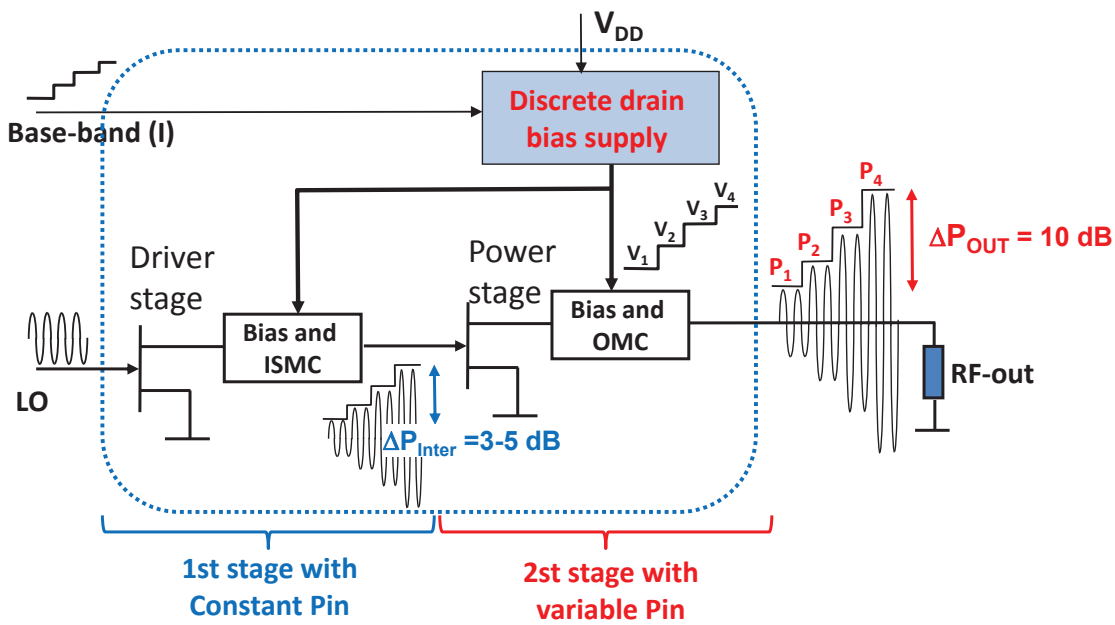

Figure III.3: Working principle of the Vector Power Modulator.

The design methodology addresses the class-B operation of GaN-HEMT devices and

power gain control using supply modulation technique applied at drain port of a two stage circuit, at a center frequency f_0 of 2.2 GHz. The driver stage is designed with a 6 W GaN transistor and the power stage is designed with a 25 W GaN transistor respectively.

The driver stage, operating at a constant LO input power provides the output power variation required to drive the power stage which is coupled via an inter-stage matching circuit (ISMC). The discrete drain bias supply as indicated in fig. III.3 is necessary for RF carrier amplitude modulation and makes use of high speed switching GaN cells [62, 64]. As it will be shown later, two-stages are needed to generate modulated RF power waves with high peak-to-average power ratios (PAPR > 10 dB).

The proposed Vector Power Modulator appears as a variable gain amplifier. The design of variable gain amplifiers (VGA) have been reported in literature in the past [65], but to our knowledge, mixerless power modulator with variable gain capabilities operating always at peak efficiencies has not been reported so far. A small example of the specifications required in modern transmitter design could be to have over 10 dB power back-off, output power over few tens of watts and around 500 MHz instantaneous bandwidth at L, S or C-bands.

2.2 GaN Transistors and PCB Technology Selected

Once the objective of this work has been established and well defined, one of the most important steps is the selection of the active device technology. For this purpose, high voltage (50 V) Gallium Nitride (GaN) technology was selected considering numerous advantages of GaN as discussed briefly in chapter-1.

Table III.1 summarizes the key characteristics of the GaN transistors selected.

Properties	**6 W GaN**	**25 W GaN**
f_{max} (GHz)	15	15
Max. P_{out} (W)	8	25
V_{DSmax} (V)	40	40
$I_{DSS,max}$ (A)	1	3
V_{GS}, pinch-off (V)	-3	-3
V_{DS}, Breakdown (V)	100	100
η_{drain} (%)	45 at P_{in} 26 dBm and V_{DS} 40 V	53 at P_{in} 34 dBm and V_{DS} 40 V
Small Signal Gain (dB)	17 at P_{in} 10 dBm and V_{DS} 40 V	15 at P_{in} 10 dBm and V_{DS} 40 V

Table III.1: Key characteristics of the GaN transistors selected.

Both the 6 W transistor (CGHV1F006S) and the 25 W transistor (CGHV1F025S) were supplied by Wolfspeed technologies and operate on a 40 V rail circuit while boarded on a 3 mm x 4 mm, surface mount, dual-flat-no-lead (DFN) package (fig. III.4).

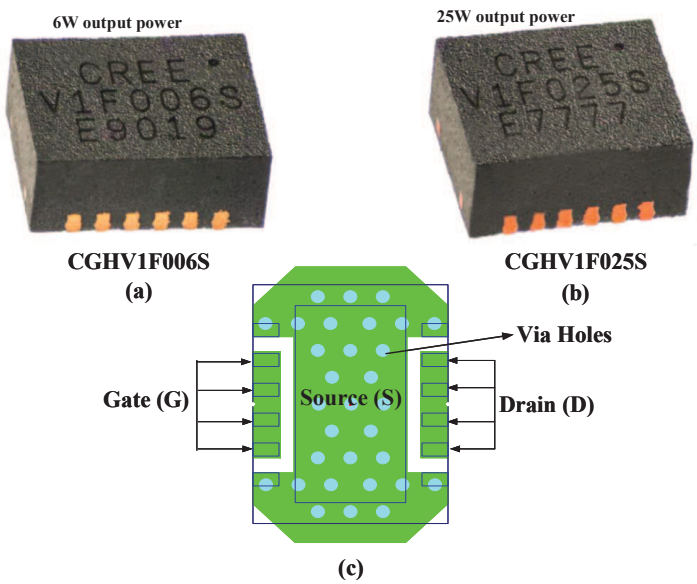

Figure III.4: Packaged transistor technology used: (a) Cree CGHV1F006S (b) CGHV1F0025S and (c) Transistor footprints indicating the different terminals.

General DC-IV characteristics of the 6W and 25 W transistors are plotted in fig. III.5.

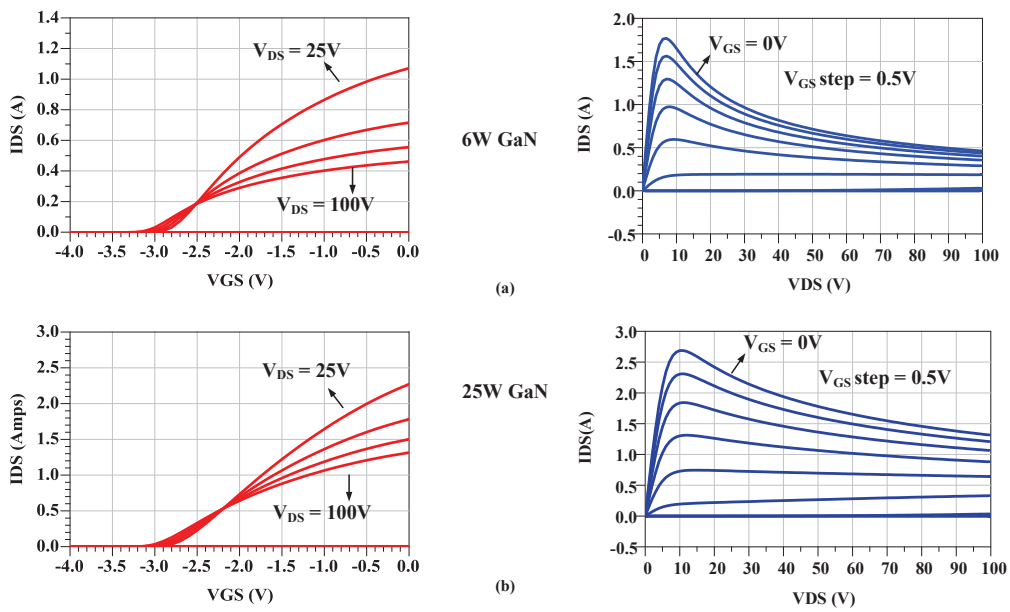

Figure III.5: DC-IV characteristics of the GaN transistor (a) 6 W and (b) 25 W.

The bias conditions V_{gso}= -2.8 V and V_{dso}= 40 V provide quiescent bias currents of 12 mA and 79 mA for the 6 W and 25 W transistors respectively which were the initial operating conditions for the design procedure.

The overall two-stage circuit was realized in hybrid Printed Circuit Board (PCB) technology for S-band operation (2 GHz-3 GHz). For this purpose, Rogers RO4350B substrate was selected. The substrate material possesses the properties needed by designers of RF microwave circuits. Low dielectric loss allows the material to be used in many applications where higher operating frequencies limit the use of conventional circuit board laminates. Table. III.2 highlights the key characteristic properties of R04350B [66].

Substrate Properties	**Values**
Dielectric Permittivity, ϵ_r	3.48
Loss Tangent of dielectric, tanδ	0.0031
Substrate Thickness, T	35 um
Conductor Thickness, H	0.508 mm
Conductivity, σ	5.1e^7 S/m

Table III.2: Principal Properties of Rogers RO4350B substrate.

2.3 Overview of the Design Methodology

Fig. III.6 illustrates the design flow chart indicating different steps to be followed for the circuit design starting from the selection of the transistor operating class upto the measurements of the fabricated device. For the electrical design, Keysight ADS have been used whereas GENESYS and Momentum have been used for the matching topology and layout respectively.

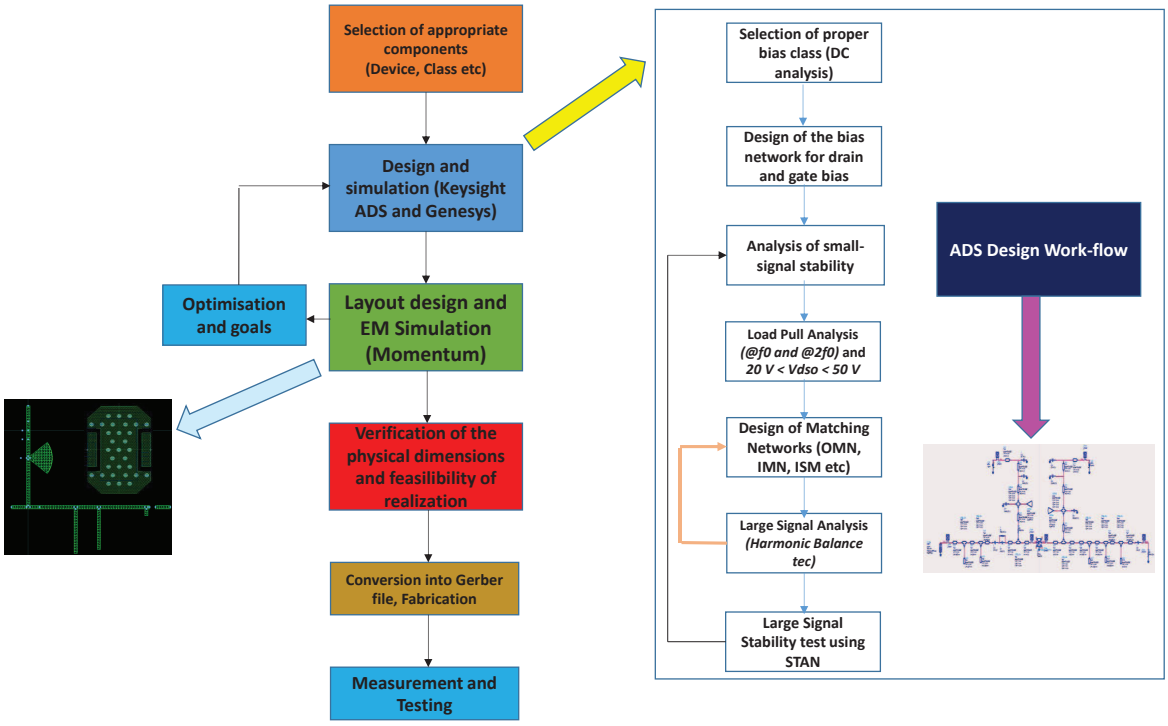

Figure III.6: Design methodology steps for the overall two-stage circuit .

3 Design Procedure of the Power Stage

This section briefly illustrates the procedure followed and various design steps adopted for the power stage circuit design, which is the first step of the overall work.

3.1 Bias Circuit Architecture and Stability Issue

The most widely used bias network design takes the advantage of a quarter wave line (high impedance) with a radial stub (low impedance) in shunt, which acts as a capacitor. The quarter wave ($\lambda/4$) line, at the fundamental frequency presents a very high impedance to the main RF line thereby acting close to an open circuit. In the gate bias, the main issue that must be taken into account is the stability whereas for the drain bias, video bandwidth is a key criteria.

Fig. III.7 shows the general topology of the gate and drain bias circuits used for the power stage design procedure.

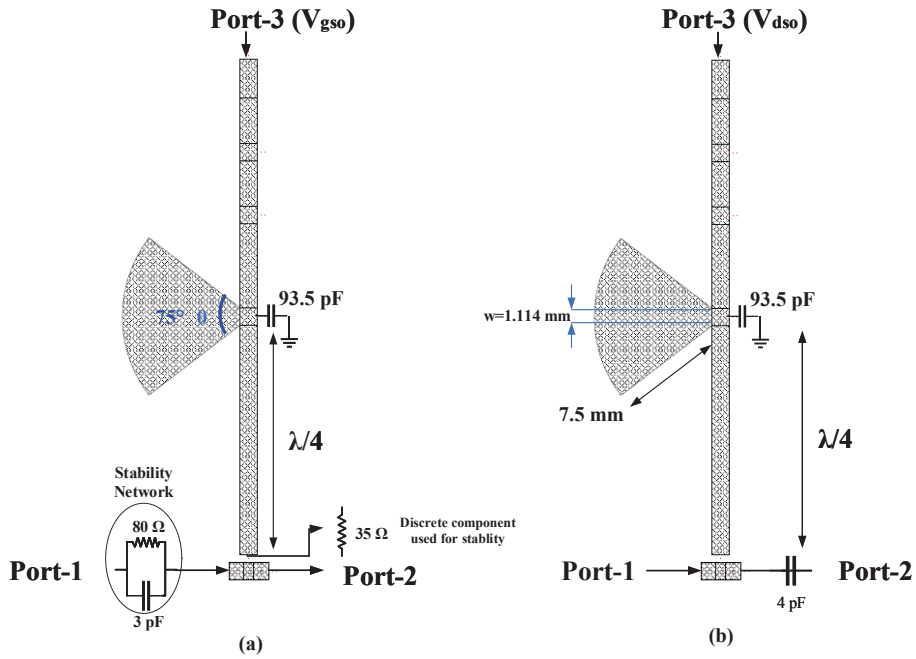

Figure III.7: Topology of the biasing circuits along with the stability network for the power stage (a) gate bias circuit and (b) drain bias circuit.

The radial stub is used in order to avoid the undesired parasitic effects generated by the decoupling capacitors at higher frequencies. Moreover, the radial stub can provide wide bandwidth operation. An important secondary function of the bias network is to present a short circuit for the second harmonic, as second harmonic control is necessary for achieving high efficiency.

One of the most important feature in selecting a bias network is also to make sure that it provides suitable video bandwidth for integrating wide base-band signal.

Fig. III.8 shows the simulated S-parameter response of the drain bias network topology shown in Fig. III.7 (b) using real values of capacitor models.

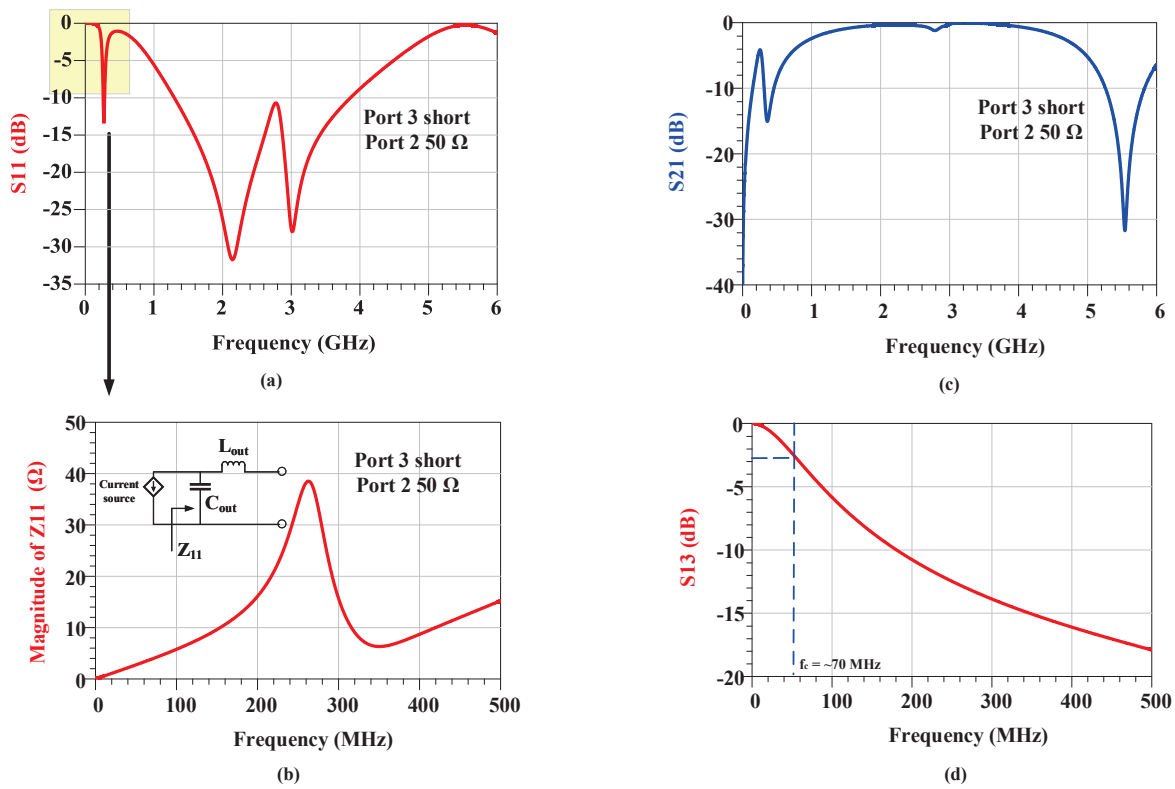

Figure III.8: Simulated S-parameter results of the output bias network (a) S_{11} response (b) Low frequency impedance Z_{11} (c) S_{21} response and (d) Isolation between DC and RF ports.

If fig. III.8 (a) is analyzed from DC up to 6 GHz, it gives an indication of S_{11} less than -10 dB for the center frequency 2.5 GHz whereas a flat gain response S_{21} over the entire band fig. III.8 (c).

Fig. III.8 (b) shows the impedance Z_{11} seen by drain of the transistor at low frequencies when the DC port is terminated into a short and the output shunt capacitance C_{out}=2.2 pF and series inductance, L_{out}=0.2 nH of the transistor (LC network) are taken into account. Z_{11} exhibits a sharp resonance at around 250 MHz. This resonant frequency must be increased to have better video bandwidth capabilities [67].

Thanks to the low value of the output capacitance C_{out} by factor of 10 for GaN transistors as compared to LDMOS for example, the resonance can be shifted to higher frequencies. The resonance presented gives a strong indication of baseband memory effects and is usually difficult to model in a polynomial based predistortion system.

Fig. III.8 (d) shows S_{13} parameter at low frequency when all the three ports are terminated with 50 Ω indicating a frequency bandwidth of around 70 MHz of the bias circuit

alone.

In the gate bias circuit, it is necessary to implement additional passive elements to ensure the unconditional stability [3] of the circuit within the band of operation (from DC to 10 GHz). For a small signal, the stability of any RFPA is analyzed using S-parameters along with stability (K) factor and stability measure (Δ). That is, the source and load reflection coefficients should be less than unity for the appropriate design of the input and output matching circuit for maximum power transfer.

Negative impedance seen looking into the ports of either input or output results in oscillations which can be avoided by decreasing the gain and hence introducing losses at low frequencies using stability networks. To ensure unconditional stability of the RFPA, a serie resistor (35 Ω) is connected at the gate bias and a parallel RC circuit (acting as a High Pass Filter, R=80 Ω and C=3 pF) is incorporated at the input of the transistor before the gate bias network is incorporated. It is important to validate the unstable reflection coefficient regions at different frequencies within the Smith chart to make sure that the unstable impedances remain out of the region. Fig. III.9 shows an example of the source (left) and load (right) stability circles for a packaged 25 W GaN transistor at a drain voltage of 28V without incorporating any stability network. It can be observed from the figure that unstable region is spread everywhere within the smith chart therefore indicating unstable operation for a frequency range of 0.1 to 10 GHz respectively.

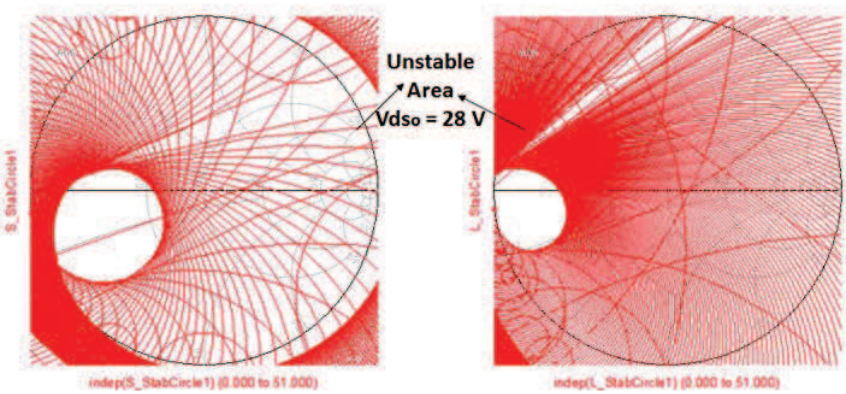

Figure III.9: Simulated stability circles (left) Source stability circles (right) Load stability circles for determination of unconditional stability.

As the intended design methodology and the proposed circuit is specified for supply modulation technique, the stability analysis was performed for different drain bias voltages for the power-stage.

Fig. III.10 illustrates the overall individual stability performances for the band of interest for the power-stage at four drain bias voltages of 15 V, 25 V, 35 V and 45 V. It can be observed from fig. III.10 that the implementation of the specified stability networks has caused unconditional stability for all the drain bias voltages and at every frequency points within the band of interest and beyond.

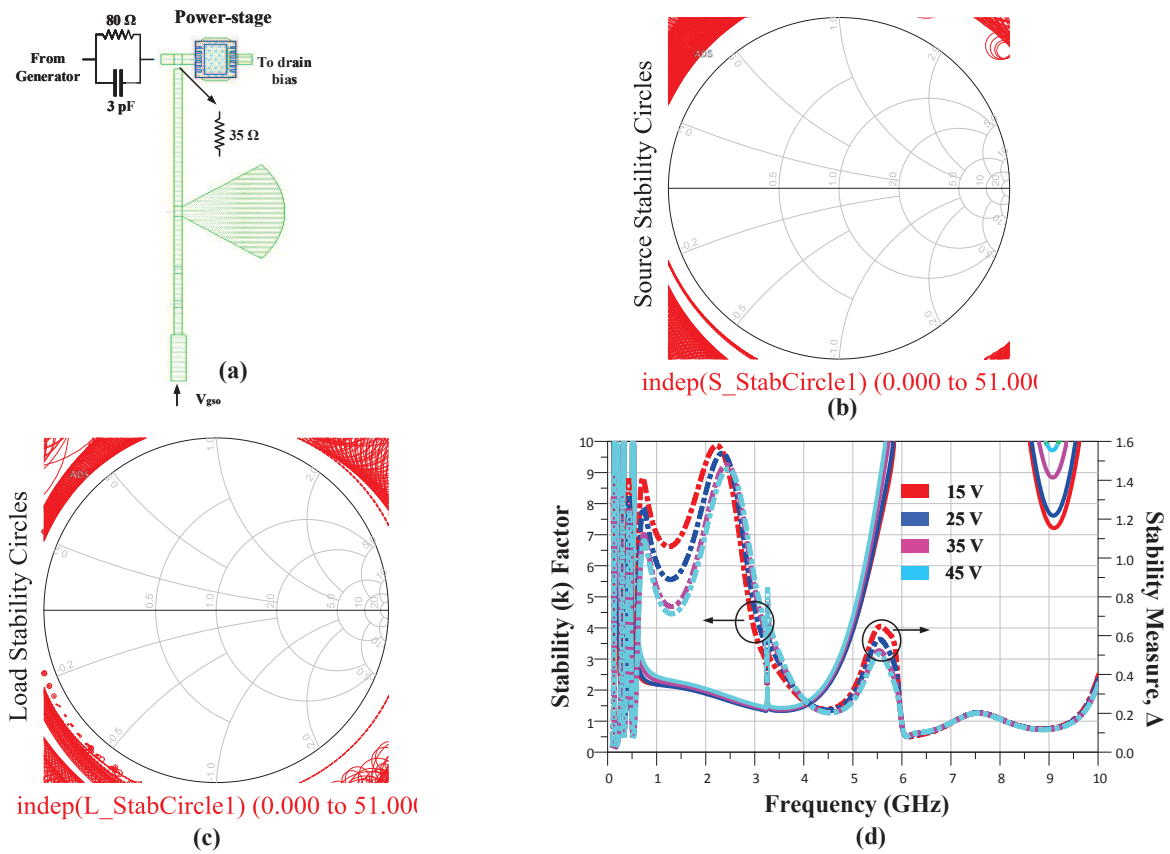

Figure III.10: Unconditional Stability after the implementation of the stability network for the power-stage (a) Stability Network (b) Source Stability Circles (c) Load Stability Circles and (d) Stability Factor, k and Stability Measure, Δ.

Once the stability for the power-stage has been ensured, the next step in the design procedure is to obtain appropriate load and source impedance at each of the transistor's package plane in order to transform them to standard 50 Ω load and source for maximum transfer of power.

3.2 Matching Network Design

This section highlights the detailed procedure for obtaining the optimum load impedances at different drain voltages and different frequencies :

3.2.1 Load-Pull Analysis

For high power amplifier design, the small signal PA design techniques are not useful since at high input power levels, the non-linearity of the transistor becomes predominant. The most widely used technique for the large signal PA analysis is the load pull simulations using harmonic balance technique.Load pull analysis uses impedance tuners to vary the source and load impedance seen by the transistor and highlights the performances such as output power and PAE. The data obtained from the load pull can then be mapped onto the Smith chart as load pull power contours. The load pull contours generally represent the actual behaviour of the active device and from these, the optimum impedances can be selected to obtain the desired RF performance. Fig. III.11 shows the general loadpull schematic for initial conditions with a tuner [68] where the second harmonic was kept shorted. This has been achieved by taking into account the designed bias network and appropriate stability networks as explained in the previous section.

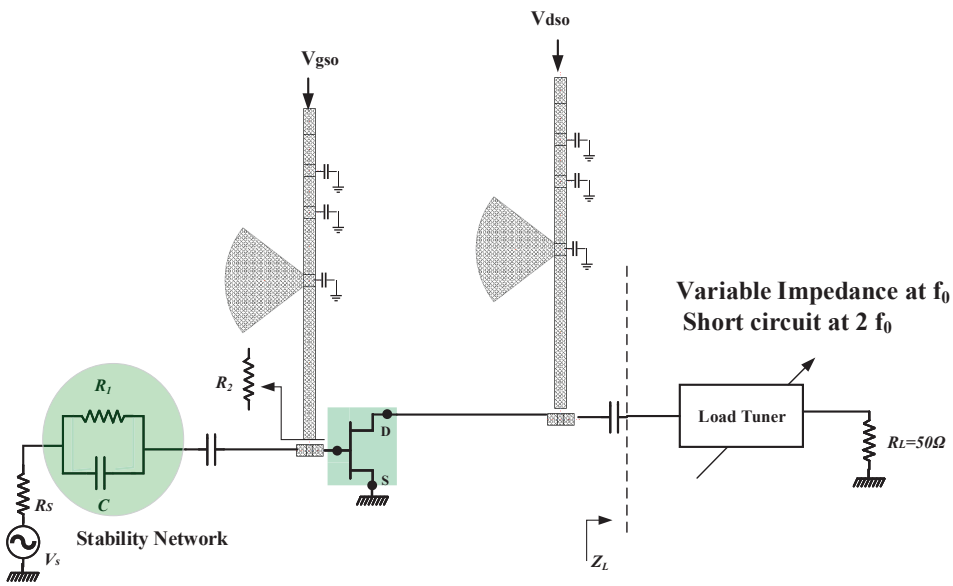

Figure III.11: General schematic of initial loadpull analysis using load tuner with second harmonic as short.

The objective of this thesis work is to have high efficient performances over a wideband therefore load pull simulations to target maximum PAE have been performed. However, the use of commercial simulating tools such as Keysight ADS demands the accurate large

signal model of the device to characterize the device properly at the intrinsic current generator plane. The issues of the accuracy of the large signal model leads the RF power amplifier design cycle to iterate several times and it also needs a lot of effort to achieve the desired amplifier specifications. In addition, the RF voltage and current waveforms at the current generator plane are not available easily for the large signal models provided by many foundries. As in this design process, commercially packaged GaN transistors are used from Wolfspeed, it is not possible to investigate the performances beyond the package levels but we have access to the intrinsic voltage and current probes that enable us to plot the dynamic loadlines.

Fig. III.12 shows the initial loadpull contours corresponding to maximum PAE and output power for 25 W GaN transistor when second harmonic is terminated by a short. It can be observed from fig. III.12 that there is a certain trade-off between the load impedance values for maximum PAE and maximum output power. As the design procedure is based on supply modulation, it is an important point to highlight that from the loadpull simulations, the optimum impedance region for maximum PAE remains in the same area for different drain bias voltages which is highly required.

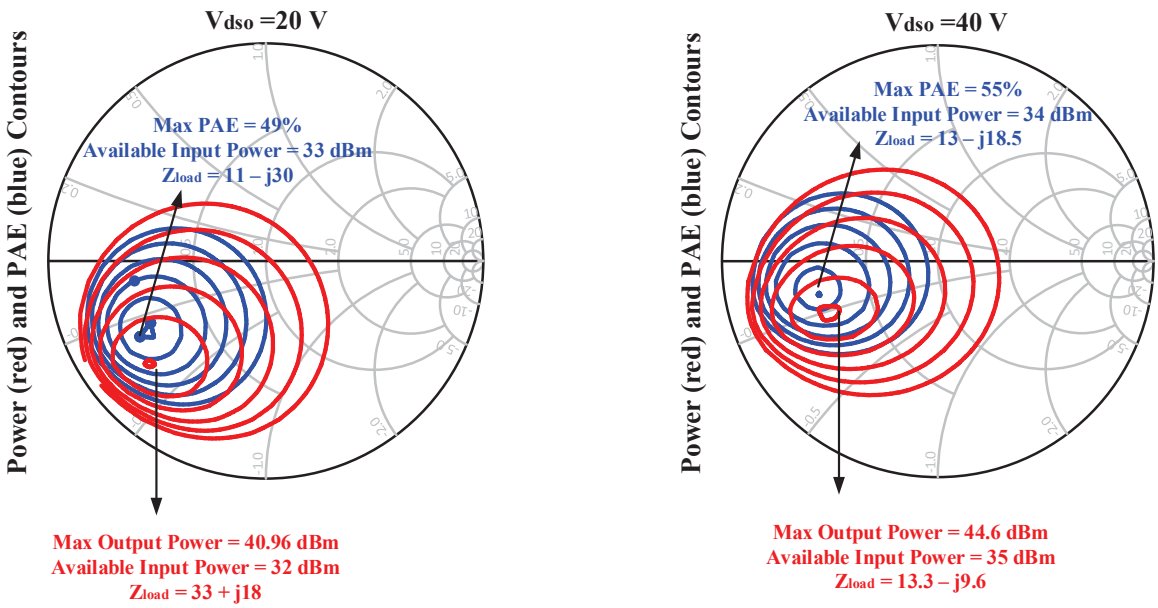

Figure III.12: Initial loadpull contours for maximum output power and maximum PAE at (a) V_{dso}=20 V and (b)V_{dso}=40 V optimized for maximum PAE when $2f_0$ is short.

Fig. III.13 highlights an example of dynamic loadlines for maximum output power and maximum PAE of Wolfspeed 25 W GaN transistor at a frequency of 2.5 GHz and at 40 V drain bias voltage respectively. It can be observed that the dynamic loadlines corre-

sponding to maximum output power and PAE have a difference because of the different peak currents and minimum voltages in each condition (fig. III.13).

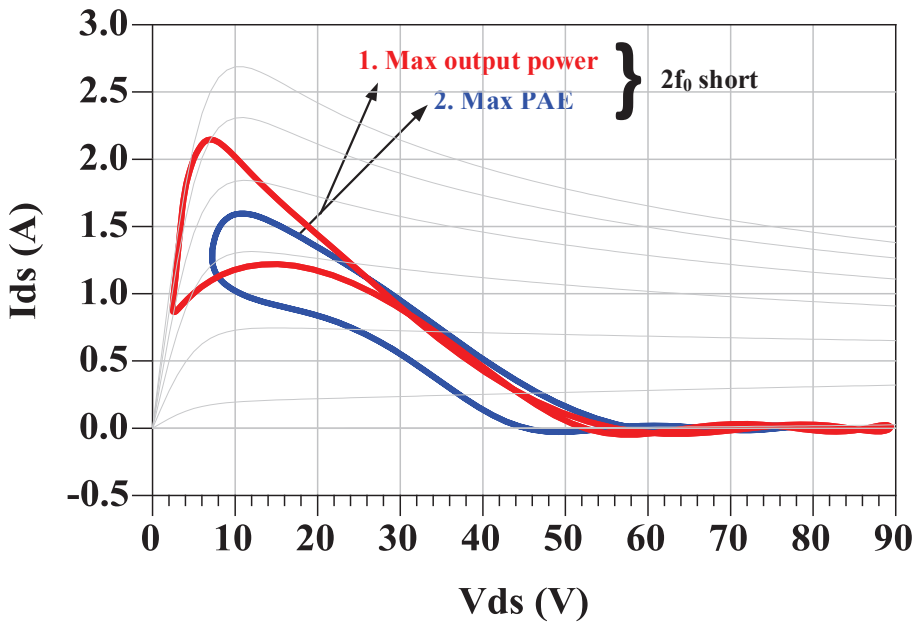

Figure III.13: Loadlines for maximum output power (red) and maximum PAE (blue) at f_0=2.5 GHz and V_{dso} = 40 V when $2f_0$ is short.

To achieve high efficiency, harmonically tuned loadpull simulations up to second harmonic has been performed. This involves at first step, finding the optimum load impedance at fundamental by keeping the second harmonic short. The next step is to keep the fundamental fixed and optimize second harmonic. The final step is to keep the second harmonic fix as obtained from the previous step and retune the fundamental.

Fig. III.14 shows an example of power characteristics versus input power at f_0=2.5 GHz and V_{dso} = 40 V in two simulation cases. In first case, the second harmonic is terminated into a short and load impedance at fundamental frequency is optimized for achieving maximum PAE performances. In second case, load impedances at both the fundamental and second harmonic were optimized.

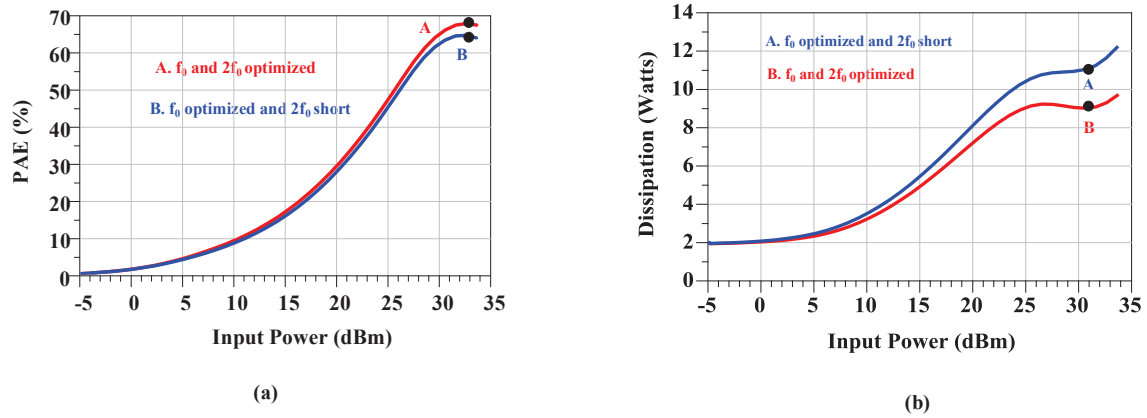

Figure III.14: Example of power characteristics of 25 W transistors when the second harmonic is short and both fundamental and second harmonic are optimized at f_0=2.5 GHz and V_{dso} = 40 V

Fig. III.15 shows the associated loadlines and the voltage and current waveforms for both the cases. A clear difference of the waveforms can be observed in the peak current values which in turn effects the overall power characteristics as shown in fig. III.14.

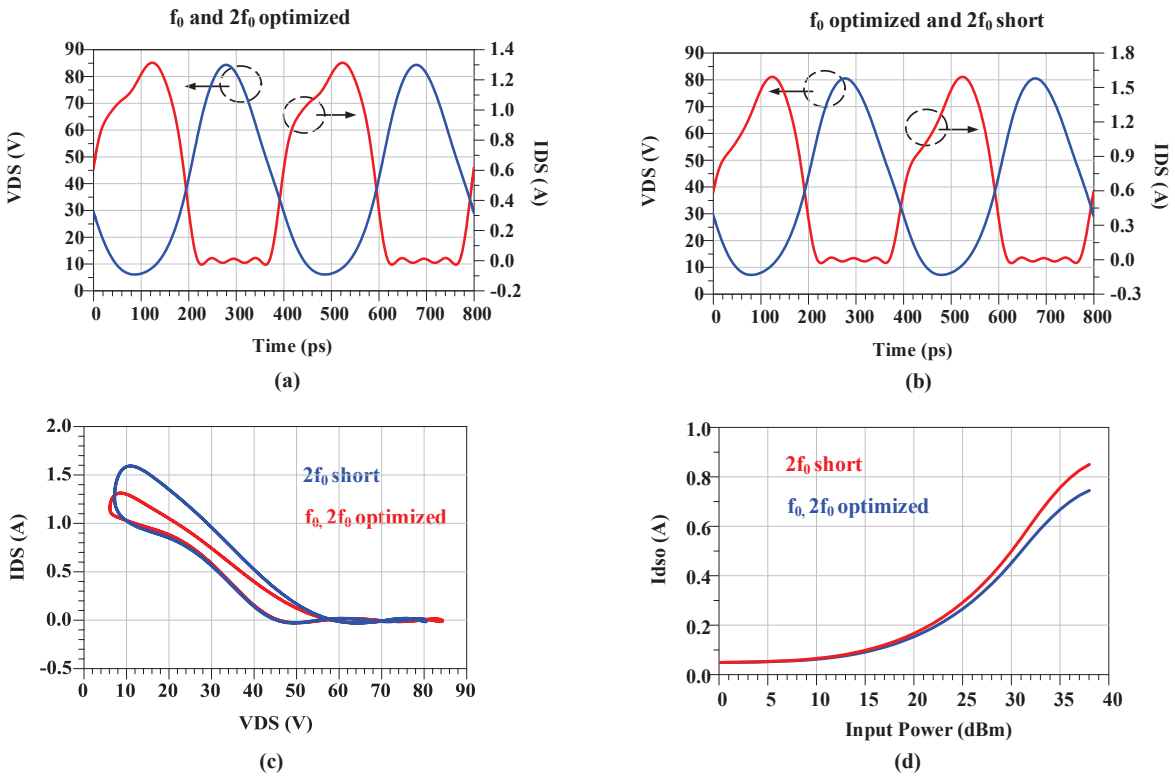

Figure III.15: Loadlines and voltage-current waveforms when the second harmonic is short and both fundamental and second harmonic optimized at saturation for f_0=2.5 GHz and V_{dso} = 40 V

The optimization of second harmonic and fundamental re-tuning yield improved efficiency performances of about 7 points. Once both the load impedances at fundamental and second harmonic were optimized for f_0=2.5 GHz, the loadpull procedure was repeated for frequency varying between 2 GHz and 3 GHz and drain bias varying from 20 V to 40 V respectively.

Fig. III.16 shows the corresponding impedance loci for the minimum and maximum drain bias voltages. It also indicates the best and unfavourable regions for second harmonics.

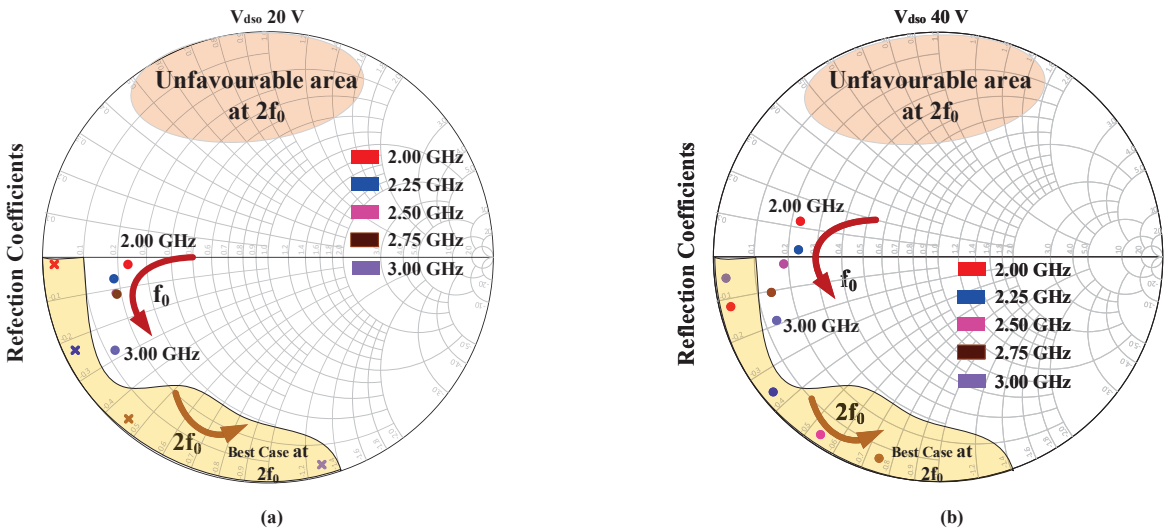

Figure III.16: Optimum load impedances obtained from loadpull simulations with f_0 and $2f_0$ optimized for maximum PAE within the band of interest, (a) V_{dso}=20 V and (b) V_{dso}=40 V.

It can be observed from fig. III.16 that the variation of impedance loci versus frequency does not change a great deal with the drain supply voltage V_{dso}.

3.2.2 Design of Output Matching Network for the Power Stage

Conventional ways of designing RFPA matching networks can be classified into three main categories namely matching networks with lumped elements which is usually a network of LC low pass filter sections, matching networks with lumped and distributed elements which also acts as an LC network combination and matching network with stepped impedance networks.

Fig. III.17 (a) illustrates the power stage distributed stepped impedance output matching network topology and fig. III.17 (b) the impedance transormation trajectory at center

frequency. The matching network was designed using Keysight Genesys and Smith Chart tool in Keysight ADS and the loadpull simulations were performed initially at a drain supply voltage of 40 V. Fig. III.17 (c) and (d) shows the corresponding optimum impedance loci Z_L obtained from the loadpull simulations at specific frequency points within the band of interest with initial design center frequency of 2.5 GHz at V_{dso} =20 V and 40 V along with the trajectory of the designed matching Z_L. The optimum match involves circling around the region of optimal impedances for maximum PAE. In order to have a high efficiency over wide bandwidth, it has to be taken into account that the matching network trajectory should be as close as possible or cover the second harmonic region as well as it is the case shown in fig. III.17 (c) and (d) .

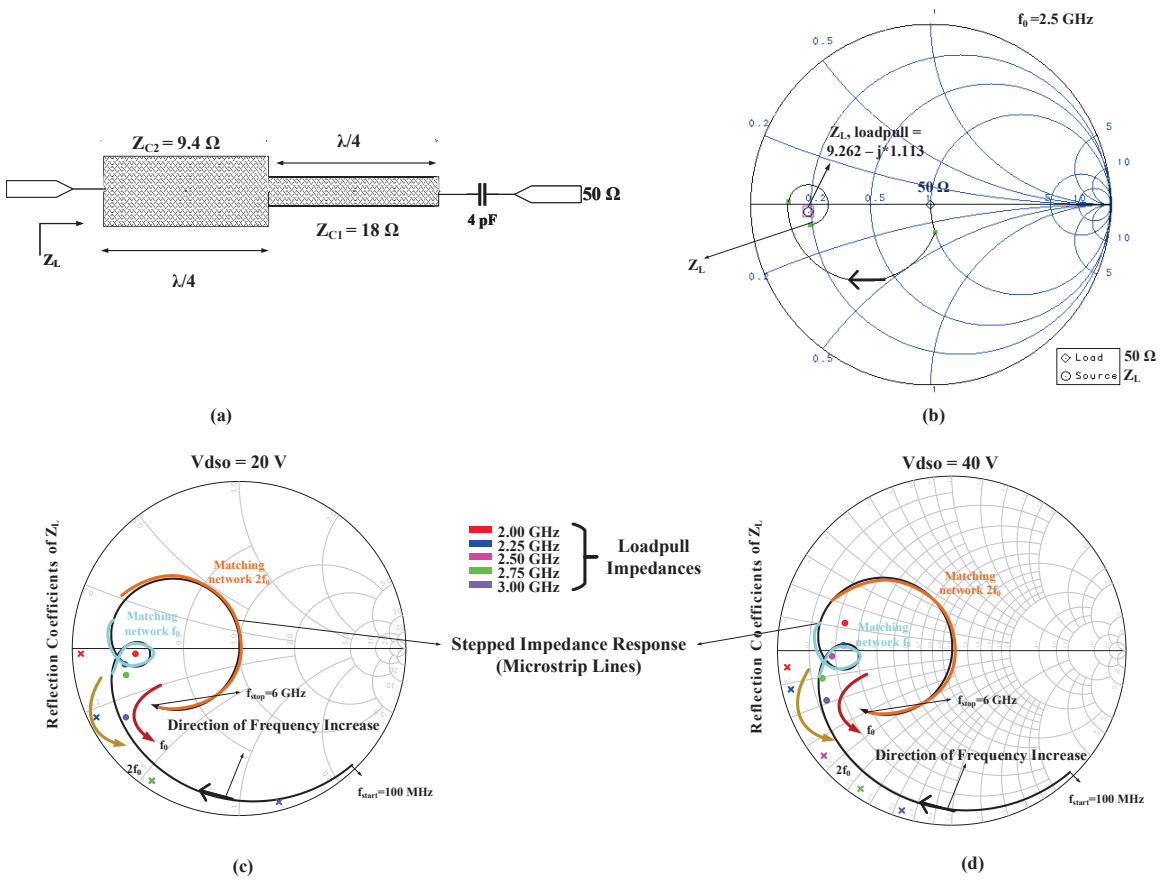

Figure III.17: Stepped impedance output match topology for the power stage (a) layout (b) impedance transformation trajectory and comparison between stepped impedance response versus frequency with loadpull impedances at V_{dso} = 20 V (c) and V_{dso} = 40 V (d).

It can be observed from fig. III.17 (c) and (d) that the optimum impedance locations from loadpull is in the counter clockwise direction whereas the matching network response is in clockwise direction. It implies an ideal matching network following optimal load in

the right directions versus frequency is not realizable without negative capacitance and inductance. This is because LC matching network consisting of non-negative element value always produce clock-wise phase rotation (evident from plotting jωL and $\frac{1}{j\omega C}$ on the smith chart versus frequency) [69]. Therefore, some impedance mismatch will be present, and the design objective is to determine the suitable trade-off that minimizes the mismatch across the design bandwidth. Also, the second harmonic region for the loadpull and matching network trajectory are not in the same region, but the important point to mention is that they do not fall in the unfavourable region for low efficiency.

3.2.3 Frequency and Power Characteristics of Power Stage

Fig. III.18 shows the layout of the power stage with stepped impedance output matching network and the inpt impedance locus versus frequency obtained from loadpull simulations when both f_0 and $2f_0$ are optimized.

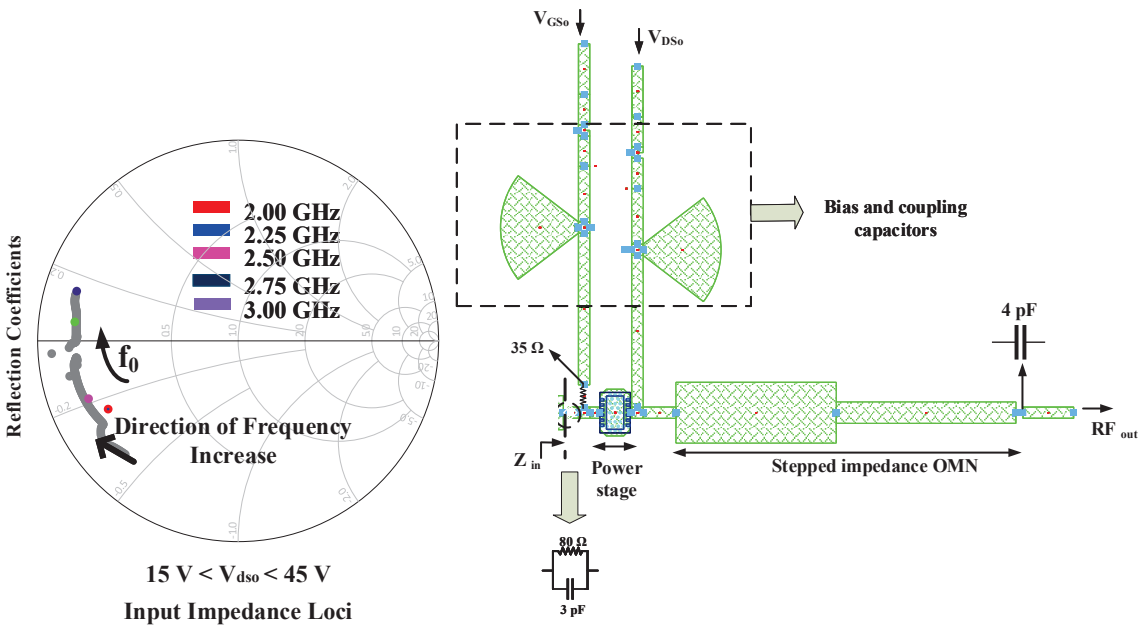

Figure III.18: Layout of the power stage with stability and stepped-impedance output matching networks showing input impedance loci from loadpull at V_{dso} = 40 V and the synthesized circuit.

Fig. III.19 (a) and (b) shows the intrinsic load lines and drain voltage and current waveforms of the power stage RFPA optimized for maximum PAE at an input power corresponding to 32 dBm (at saturation) and frequency equal to 2.5 GHz. The dynamic

loadlines at different voltage levels are optimized quite well with very small openings indicating good efficiency by the small area under the overlap between the intrinsic drain voltage and current waveforms in fig. III.19 (b).

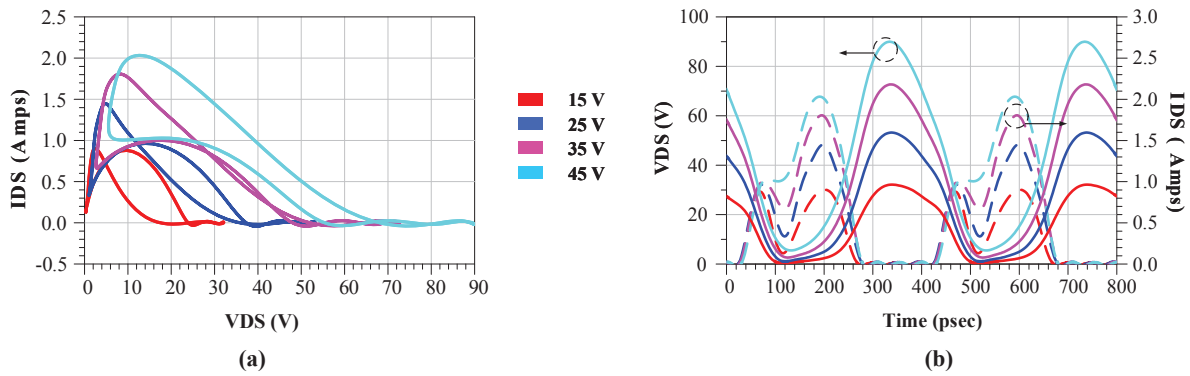

Figure III.19: (a) Simulated intrinsic loadlines and (b) drain voltage and current waveforms of power stage at 2.5 GHz and P_{in}= 32 dBm.

Fig. III.20 shows the large signal power characteristics of the power stage in Harmonic Balance simulations at f_0 = 2.5 GHz. The input power here is the power really entering at the gate port taking into account the fact that the device is not matched at its input.

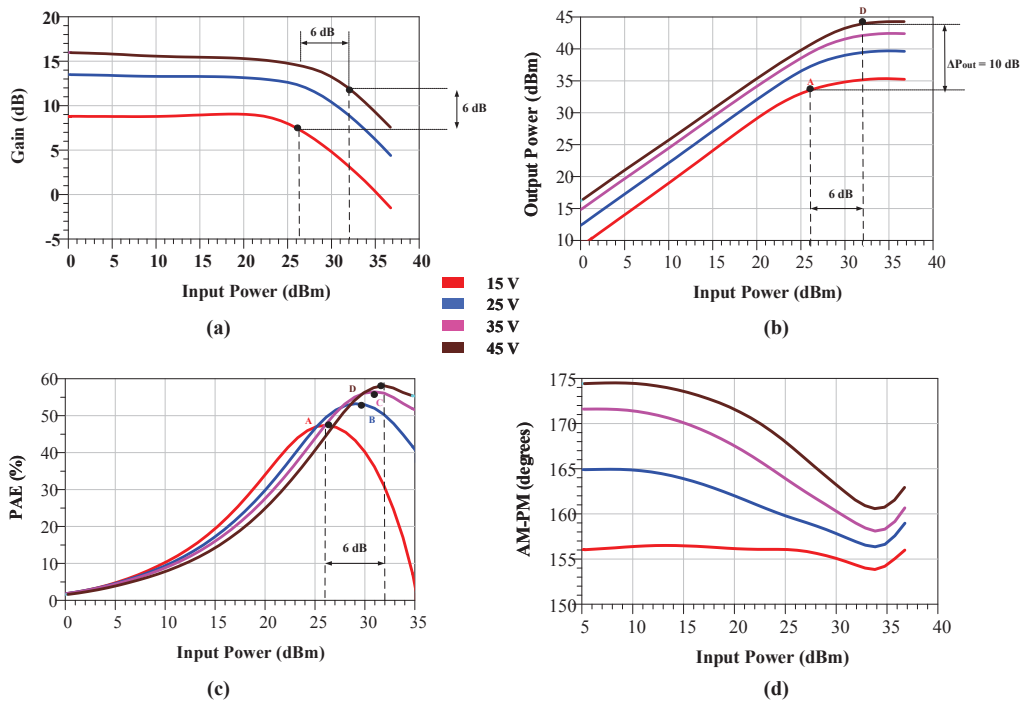

Figure III.20: Simulated large signal CW power performances of the power stage at 2.5 GHz and 15 V < V_{dso} < 45 V.

Fig. III.20 (a) and (b) illustrate the gain variation from 8 dB to 14 dB under an RF input at saturation corresponding to output powers of 35 dBm at V_{dso} = 15 V to close to 44 dBm at V_{dso} = 45 V. If the efficiency performances are analyzed in fig. III.20 (c) with respect to the input power variation of the power stage, it can be observed that the range of input power required for maximum efficiencies varies from 27 dBm at V_{dso} = 15 V to 33 dBm at V_{dso} = 45 V. From fig. III.20 (a) and (b), we can see that we cannot get both high efficiency and significant gain variations if we fix a constant input power. If we accept to have around 6 dB input power variations, we can reach 6 dB gain variations and 10 dB output power variations as indicated in fig. III.20 (a).

This appropriate input power variation has to be provided by a driver circuit which will be driven by a constant input power and will provide output power variations thanks to the V_{dso} variations. Same V_{dso} variations will be provided to both the driver and the power stage. The requirement of a two-stage circuit is explained in more details in the next section.

Finally to validate the large signal performances of the power stage alone at center frequency, the AM-PM conversion as a function of input power was analyzed [shown in fig. III.20 (d)]. It can be observed that the phase variation is quite small indicating nominal phase distortions with respect to drain supply voltage.

Also, fig. III.21 illustrates the power characteristics as a function of frequency at P_{in}= 33 dBm. It can be observed that the design procedure in simulation yields around 700 MHz bandwidth with PAE > 40% except at 15 V which can be attributed to the accuracy of the transistor model below 20 V and around 700 MHZ for high output power and gain variation from 15 V to 45 V drain voltage levels, however the low variation versus frequency can again be attributed to the model accuracy as specified in the datasheets.

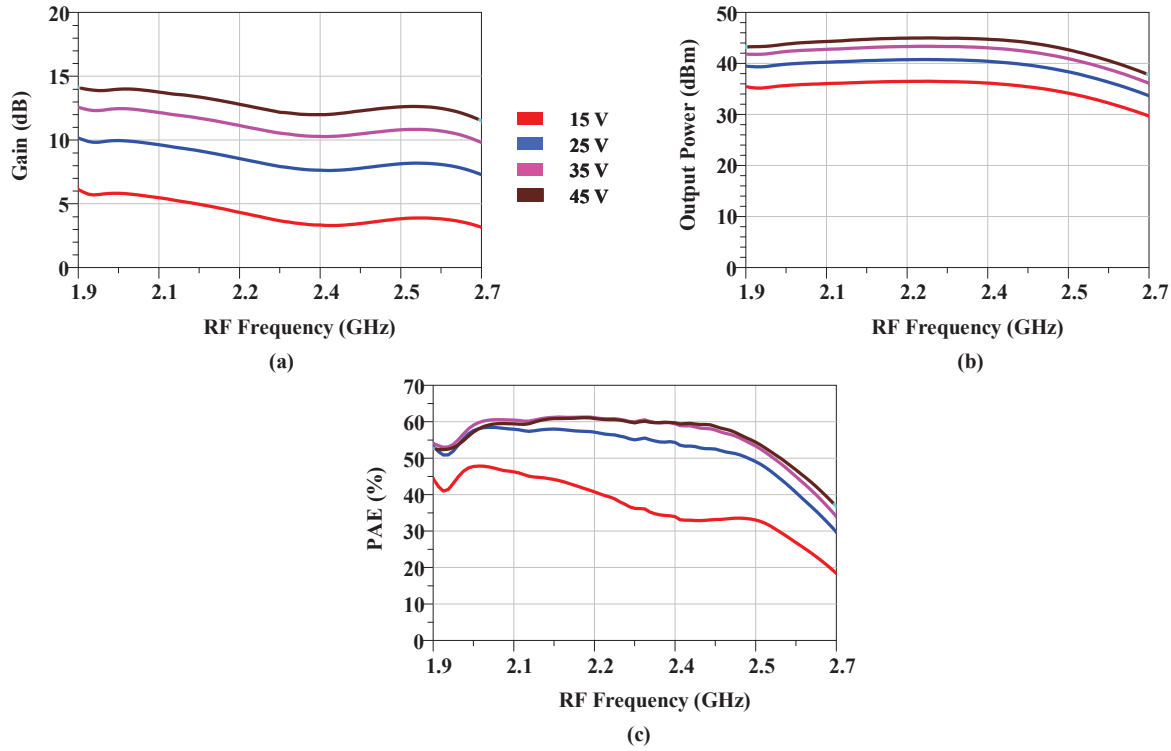

Figure III.21: Simulated power characteristics of power stage RFPA alone as a function of RF frequency over the band of interest (a) Gain (b) Output Power and (c) PAE.

3.2.4 Requirements of a Two-stage Circuit

To understand the requirement of a two-stage circuit, fig. III.22 (a) and (b) shows the simulated input output power characteristics and PAE performances for the power stage for three different drain bias voltages. The analysis is being shown with three bias levels in accordance with the power dynamic of 9.5 dB corresponding to PAPR of 16-QAM modulation schemes (three levels). It can be observed from fig. III.22 (a), that at a constant input power (for example 30 dBm), the output power variation across the load is around 8 dB varying from around 34 dBm at 15 V to 42 dBm at 45 V. From fig. III.22 (b), it can be observed that for similar output power levels, the PAE levels at 15 V is considerably low. Therefore, a conclusion can be drawn that a single power-stage with fixed input power cannot satisfy both the requirements of high PAE and power variations simultaneously for each drain voltage.

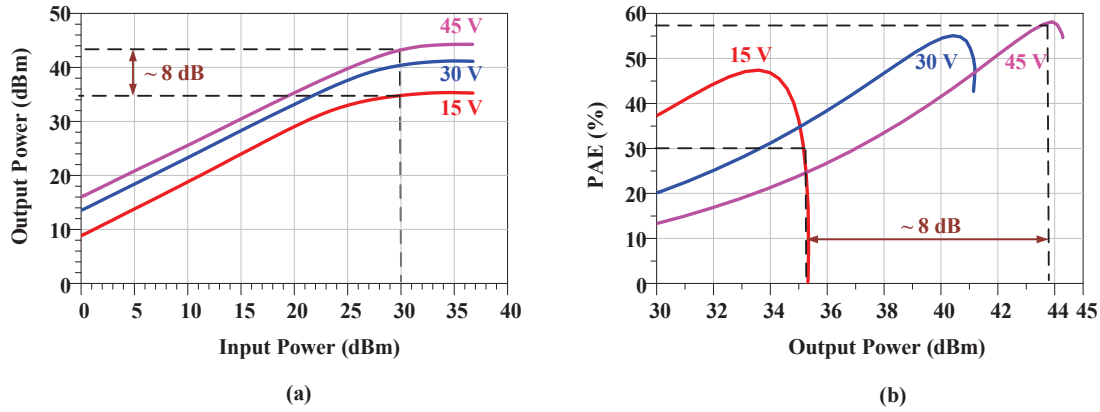

Figure III.22: Simulated input and output power (a) and PAE characteristics (b) of the power stage, analysis is made for three different drain bias voltages for a constant input power for the power stage at 2.5 GHz.

However, if an input power variation of around 5-6 dB for the power stage is accepted from 26 dBm at 15 V to 32 dBm at 45 V (fig. III.23 (a)), both large output power (gain) variations and high PAE levels (fig. III.23 (b)) can be achieved together justifying the need of an additional driver stage required to provide the necessary gain variations for the principle of Saturated Variable Gain (SVG). The output power variation of the driver stage will be achieved with drain bias variations.

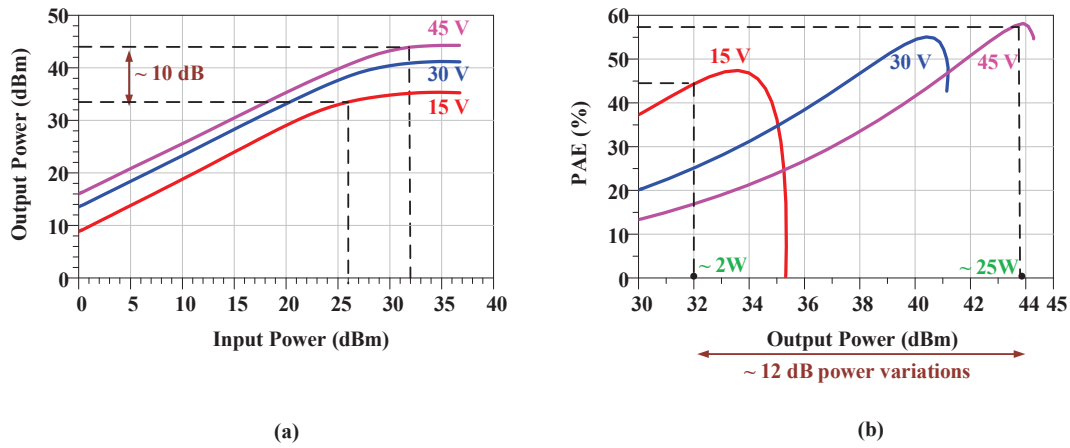

Figure III.23: Simulated input and output power (a) and PAE characteristics (b) of the power stage, analysis is made for three different drain bias voltages for a small variation of input power for the power stage at 2.5 GHz.

Therefore, the next section is dedicated to the design procedure of a two-stage circuit.

4 Design Procedure of the Two-stage Circuit

4.1 Bias Circuit Architecture and Stability Issue of the Driver Stage

The basic architecture for the gate bias of the driver stage is similar as that of the power stage except for the difference in the stability network lumped component values. Fig. III.24 shows the gate bias architecture of the driver stage. The drain and gate bias networks have the similar dimensions.

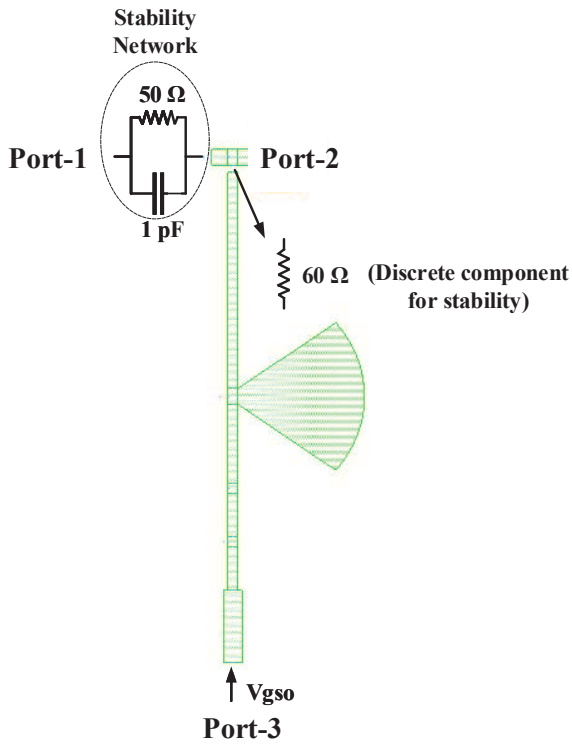

Figure III.24: Architecture of the driver stage gate bias with stability network.

Fig. III.25 illustrates the unconditional stability of the driver stage within the band of interest after the incorporation of the stability network at the input. It can be observed that the transistor is unconditionally stable for all the frequency points within and beyond the band of interest.

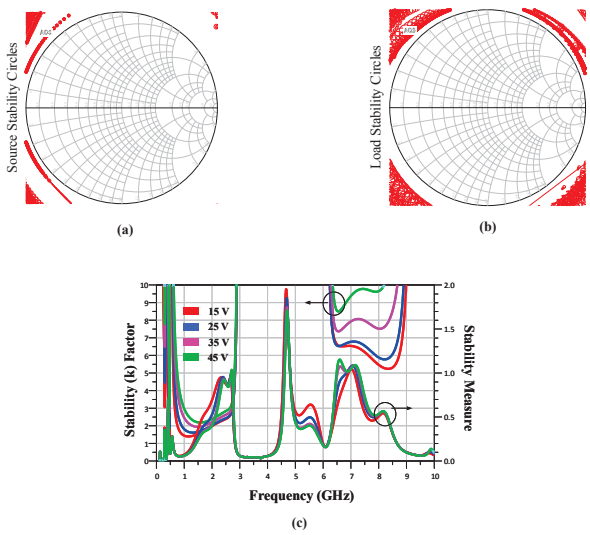

Figure III.25: Unconditional Stability after the implementation of the stability network for the driver-stage (a) Source Stability Circles (b) Load Stability Circles and (c) Stability Factor, k and Stability Measure, Δ .

4.2 Matching Network Design

4.2.1 Load-Pull Analysis of the Driver Stage

The loadpull analysis of the driver stage has the same procedure as that of the power stage explained earlier in this chapter. Both fundamental and second harmonic optimization of the impedances within the band of interest were performed for achieving maximum PAE as it was done for the power stage. Fig. III.26 illustrates the location of the fundamental and second harmonic impedances for different frequencies when both f_0 and $2f_0$ are optimized for maximum PAE performances at V_{dso} = 20 V and 40 V respectively.

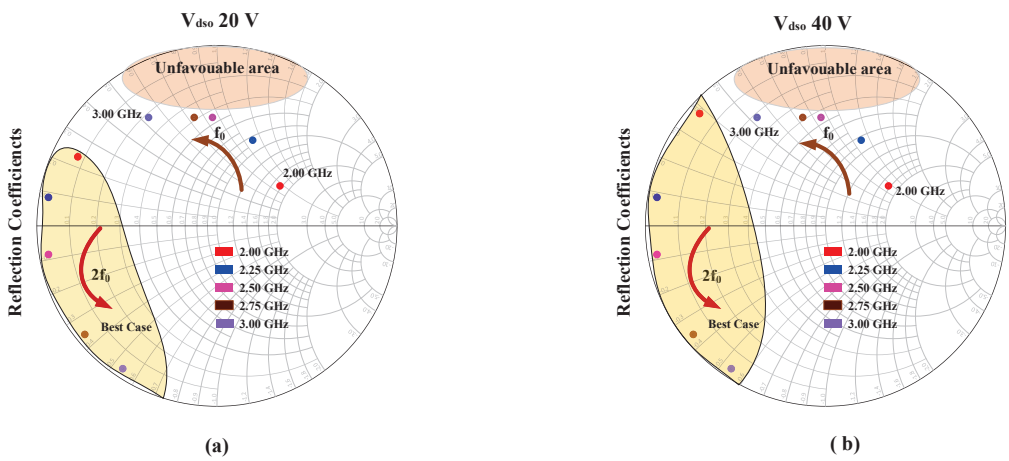

Figure III.26: Optimal load impedance at fundamental and second harmonic favourable and unfavourable region for maximum PAE of the driver stage vs frequency.

Fig. III.26 indicates the unfavourable area corresponding to second harmonic for efficieny performances. It can be observed that the impedance loci almost remains constant as the drain supply voltage is changed.

Fig. III.27 shows the associated loadlines at f_0 = 2.5 GHz and power characteristics for the 6 W transistor obtained from loadpull simulations when $2f_0$ is shorted and when f_0 and $2f_0$ are optimized like it was done for 25 W transistor which gives a PAE improvement of around 8 points.

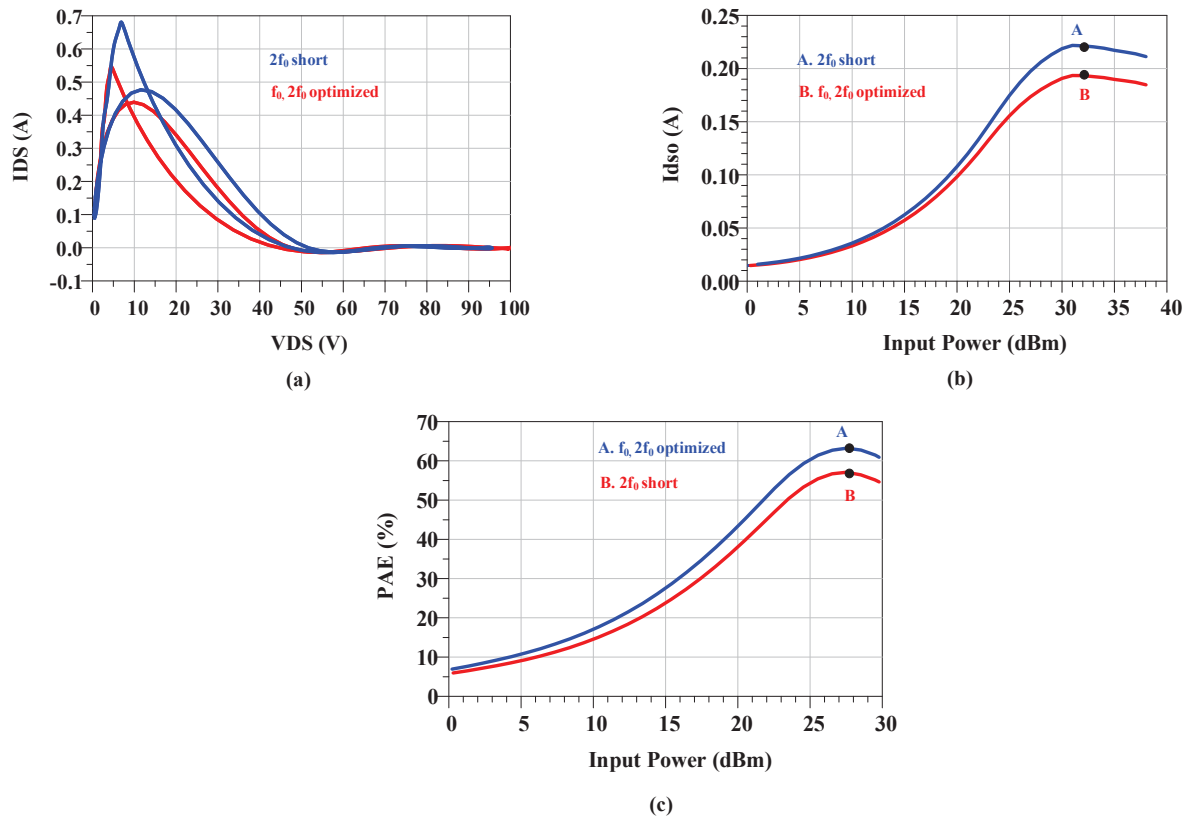

Figure III.27: Example of power characteristics of 6 W transistor when the second harmonic is short and both fundamental and second harmonic optimized at f_0=2.5 GHz and V_{dso} = 40 V.

4.3 Two-stage Saturated Variable Gain Power Modulator Circuit

Fig. III.28 shows the electrical design schematic of the two-stage circuit with the input, output and interstage matching circuits along with appropriate bias and stability networks for the driver and power stages respectively. The dimensions of the distributed

elements are specified in the figure. It can be observed from the figure that a common drain access supply has been implemented for both the driver and power stages as both the stages are similarly biased.

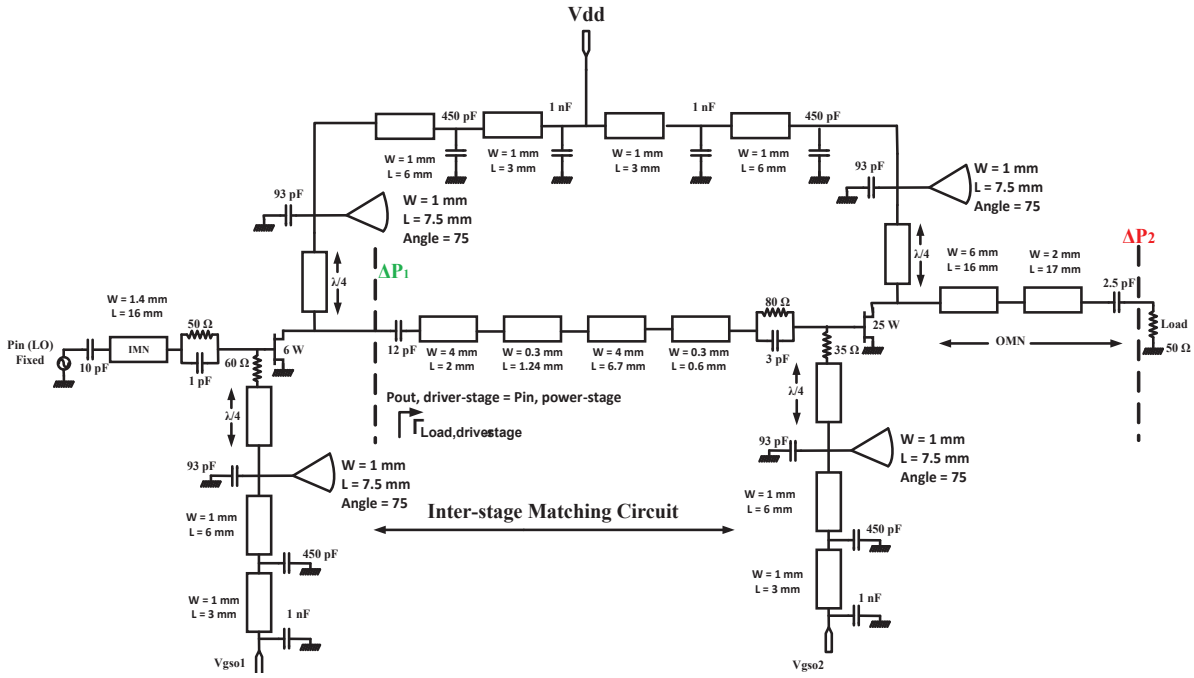

Figure III.28: Electrical design schematic of the two-stage SVG circuit

The gate bias of the two stages are independent in order to adjust precisely the quiescent bias points.

The interstage matching circuit plays a very critical role in the design procedure of the two-stage circuit and therefore has to be designed carefully. It has been designed using stepped impedance architecture. This circuit ensures the necessary power transfer from the output of the driver stage to the input of the power stage for different drain supply voltages which in turn will lead to a large output power (gain) variations > 10 dB across the load always at saturation or close to maximum efficiency points.

4.3.1 Frequency and Power Characteristics of the Driver Stage

Fig. III.29 shows the load impedance locus of the driver stage at the package plane of the 6 W transistor along with the optimum loadpull locus for load impedance of the driver stage and input impedance of the power stage at 40 V at P_{in} fixed = 19 dBm. It also illustrates the synthesized impedances for the ISMC for 15 V < V_{dso} < 45 V and versus frequency.

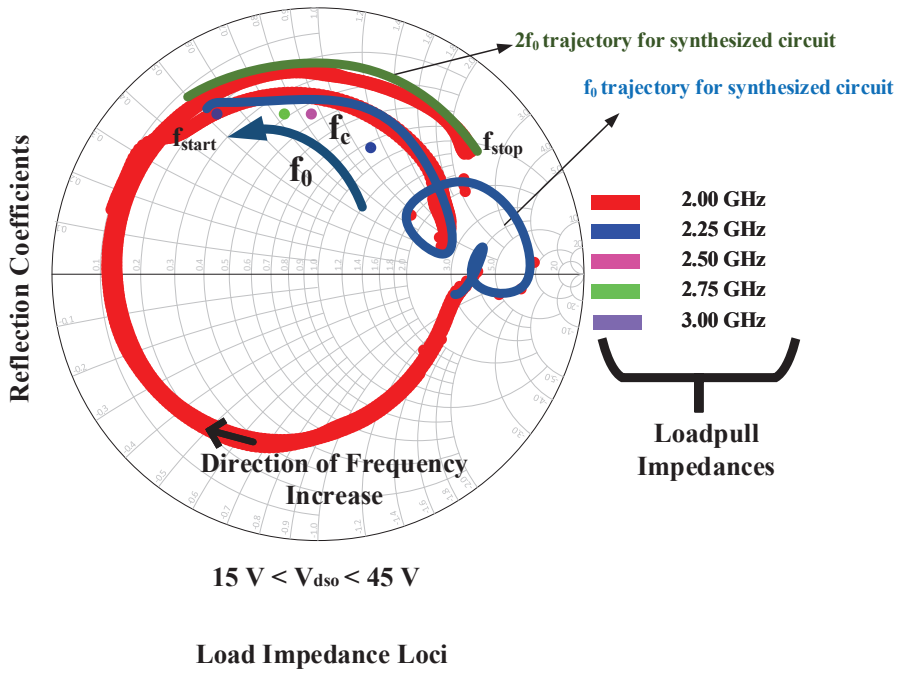

Figure III.29: Optimum load impedance loci of the driver stage from loadpull and from the synthesized circuit at reference plane ΔP_1 of fig. III.28. The impedance indicates clearly the $2f_0$ of the synthesized circuit is not well matched and is close to the unfavourable region.

The design procedure for the interstage matching circuit involves firstly the power matching of the load impedance of the driver stage to the input impedance of the power stage at center frequency and at a constant input power LO for the driver stage as shown in fig. III.29 (at 40 V and 2.5 GHz obtained from loadpull). Using this topology and this driver size, it is not possible to get appropriate input power variations for the power stage and second harmonic conditions for maximum PAE over large bandwidth. As the objective is to have higher output power (gain) variations with minimum input power variations for the power stage at different drain voltages at saturation, the impedances were slightly optimized to mismatch the power without compromising the efficiency performances to a great deal.

The important aspect of this design methodology is to make sure that the impedances obtained from loadpull for the driver are well matched or closely spaced for different drain bias voltages also as the overall two-stage circuit has to be validated for supply modulation. The overall large signal matching principle and results at the input and output of the interstage matching network is validated when the overall circuit is connected together which forms the next section of this chapter. An important point to note here is that along with the impedances at fundamental, the matching of second harmonic is a

key part of the design procedure as it impacts both the efficiency and the RF bandwidth of the overall circuit. This effect has been improved in the second prototype of the overall two-stage circuit by the implementation of new bias architecture as well as interstage matching circuit and is elaborated in the fourth chapter of this thesis.

Fig. III.30 shows the simulated CW large signal power characteristics at 2.5 GHz of the driver connected to the power stage at different drain bias voltages and taking into account the losses of the interstage matching circuit. Fig. III.30 (a) and (b) illustrates the driver stage output power and gain variations.

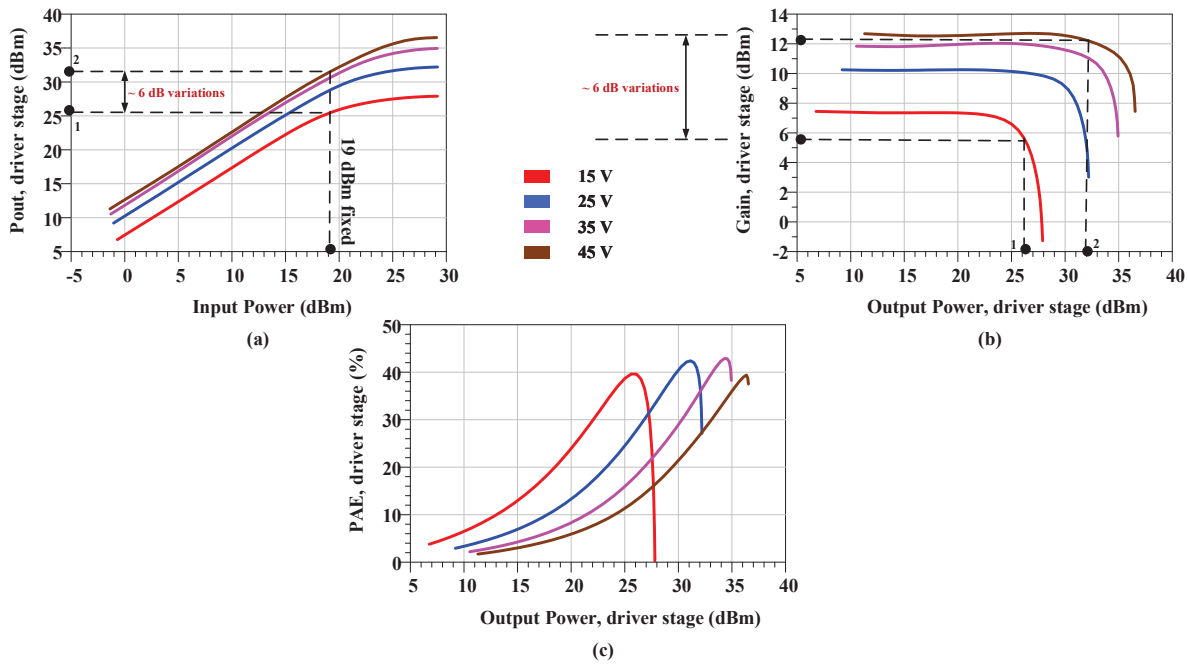

Figure III.30: Simulated large signal CW power performances of the driver stage at 2.5 GHz.

It can be observed from fig. III.30 (a) that for a fixed input power selected in simulations (19 dBm), the output of the interstage matching circuit generates desired power variations of 6 dB (26-32 dBm) corresponding to V_{dso} = 15 V and V_{dso} = 45 V. Similar gain variations are obtained as shown in fig. III.30 (b).

Fig. III.30 (c) shows the simulated efficiency performances of the driver stage amplifier corresponding to different drain supply voltages. The driver stage amplifier exhibits efficiencies between 30 % and 40 % for 15 V $<$ V_{dso} $<$ 45 V at 2.5 GHz. The efficiency of the driver stage is important to achieve a higher global efficiency of the two-stage circuit but with a less impact on the overall PAE budget than the impact of the power stage.

4.3.2 Two-stage GaN-HEMT Power Modulator : Simulation Results

Fig. III.31 shows the fabricated two-stage circuit (right) alongside the layout (left) on Rogers RO4350 substrate. Electrical and electromagnetic (EM) simulations have been carried out using Harmonic Balance in ADS and have been found to be in good agreement with each other.

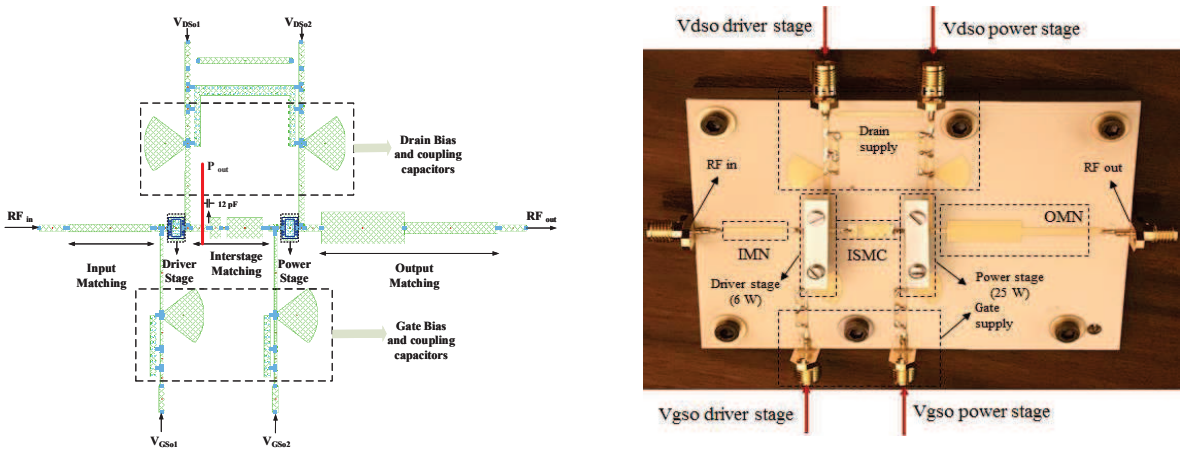

Figure III.31: Layout (left) and fabricated (right) two-stage vector power modulator circuit. The circuit has been fabricated on Rogers RO4350 substrate with $\epsilon_r = 3.48$ ([70])

Fig. III.32 illustrates the simulated power characteristics of the overall two-stage circuit [71] at 2.5 GHz. From simulations, a constant input power acting as LO for the driver stage was chosen to be 19 dBm. The output power of the driver stage plotted here is the power at the input reference plane of the power stage.

It can be observed in fig. III.32 (a), that at a constant input power LO of 19 dBm, the output of the driver stage generates a 6 dB output power variations starting from 26 dBm corresponding to $V_{dso} = 15$ V (point A) to 32 dBm corresponding to $V_{dso} = 45$ V (point B). This 6 dB of power variation is coupled through the inter-stage matching circuit to the input of the power stage (fig. III.32 (b)) and for same input power variations of the power stage, the overall output power variations across the load is 34 dBm corresponding to $V_{dso} = 15$ V (point C) to 44 dBm corresponding to $V_{dso} = 45$ V (point D).

This indicates an overall power (gain) variation of 10 dB indicating modulation of power. Similarly, fig. III.33 [72] illustrates the gain characteristics of the driver and power stages respectively at 2.5 GHz corresponding to the similar levels of power at the input

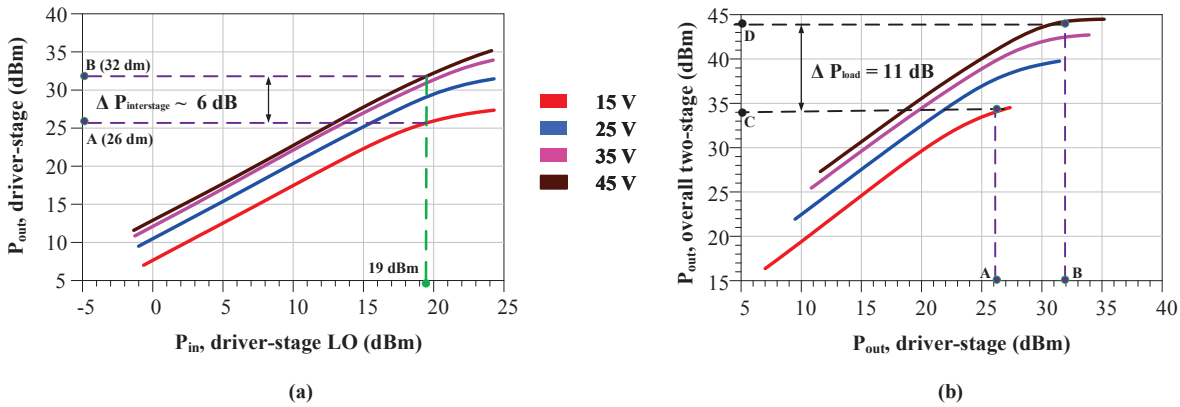

Figure III.32: Input and output power characteristics of the (a) driver-stage and (b) power stage at 2.5 GHz when the two-stage circuit is connected together.

of the interstage matching circuit.

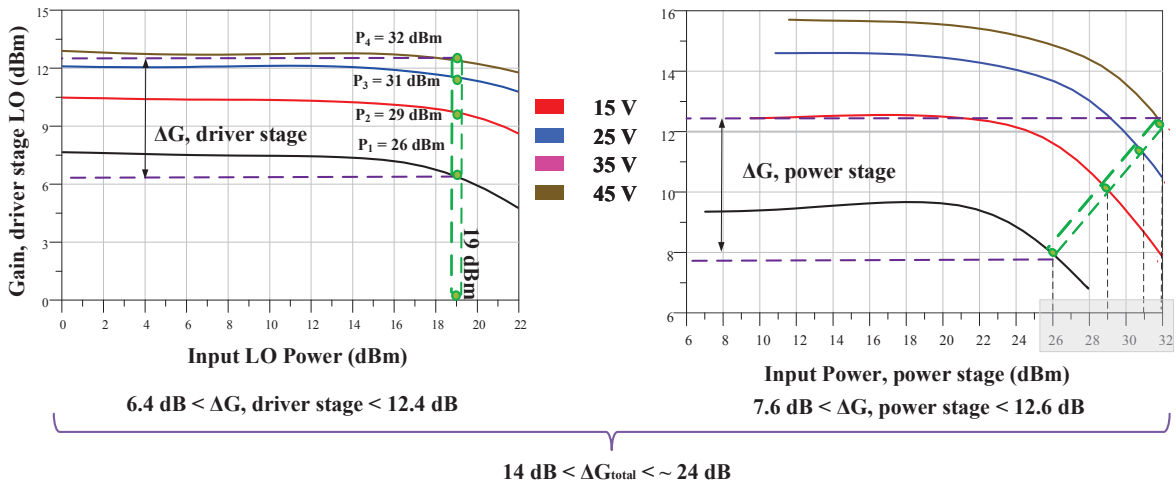

Figure III.33: Demonstration of gain transfer principle showing gain characteristics of the (a) driver stage LO and (b) power stage respectively at 2.5 GHz.

From fig. III.33, it can be concluded that the driver stage generates power variations corresponding to each value of drain bias voltage V_{dso}.

It also adds gain to the overall chain (indicated in the figure) and provides power for the overall circuit stage (>10 dB). The driver stage generates an overall gain of 6.4 dB corresponding to V_{dso} = 15 V to 12.4 dB corresponding to V_{dso} = 45 V at 2.5 GHz whereas the power stage generates an overall gain of 7.6 dB corresponding to V_{dso} = 15 V to 12.6 dB corresponding to V_{dso} = 45 V which produces an overall gain variation of 11 dB validating the principle of variable gain.

Under this condition, if the global efficiency performances of the overall two-stage circuit is analyzed at 19 dBm input power LO (shown in fig. III.34), it can be observed that the PAE corresponding to all the four drain bias voltages is very close to or at saturation.

Fig. III.33 has demonstrated the principle of variable gain whereas fig. III.34 shows the efficiency performances obtained when the input power level of the driver stage is 19 dBm. The overall efficiency stands above 50 % except at V_{dso} = 15 V. Hence, the necessity of two-stage circuit for the principle of Saturated Variable Gain (SVG) has been validated and the methodology imagined works well in simulations at center frequency of 2.5 GHz.

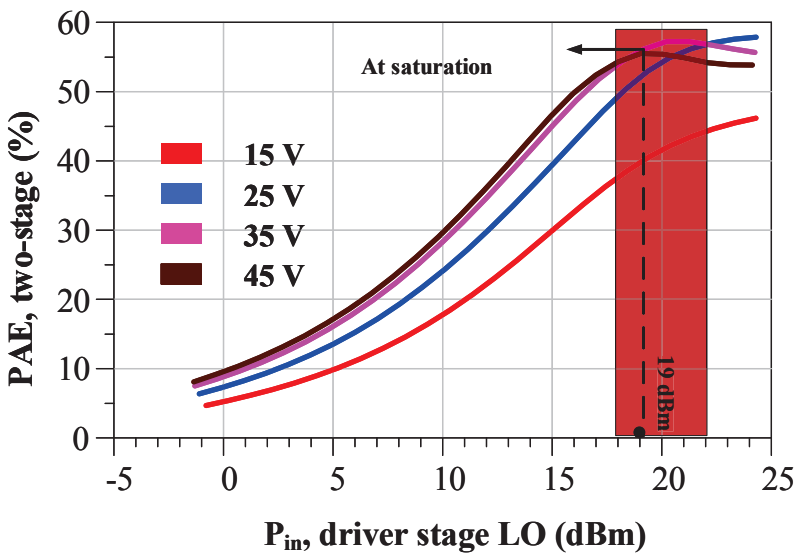

Figure III.34: PAE as a function of input power LO of driver stage for the overall two-stage power modulator circuit at 2.5 GHz.

As the principle of SVG has been demonstrated for 2.5 GHz, the next objective is to have the same power performances at saturation for an acceptable RF bandwidth within the band of interest.

Fig. III.35 shows the static CW simulated power characteristics of the overall two-stage power modulator circuit as a function of RF frequency for different drain bias voltages respectively.

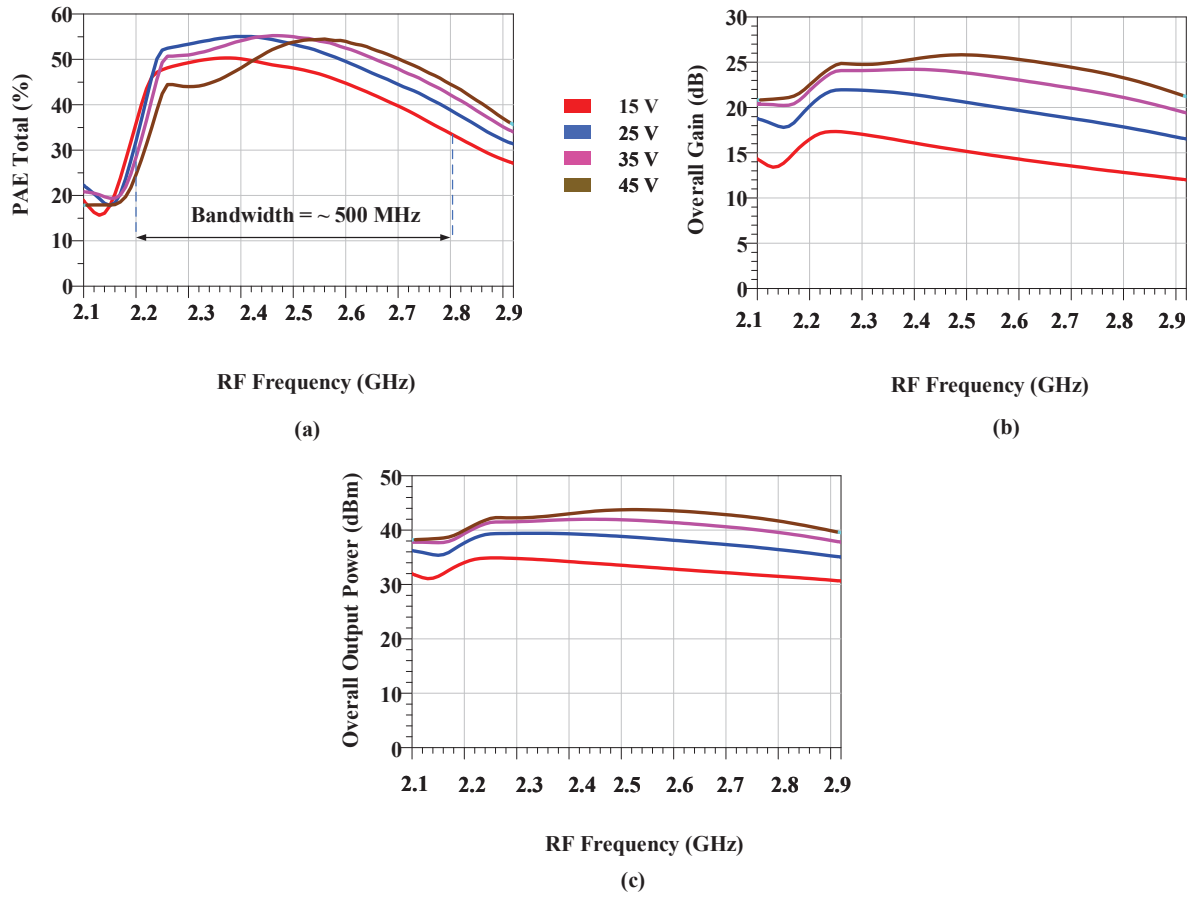

Figure III.35: Simulated power characteristics of the two-stage power modulator circuit as a function of RF frequency (a) PAE as a function of RF frequency and (b) Overall two-stage circuit gain and (c) output power.

From fig. III.35 (a), it can be observed that overall PAE of > 40 % is achieved for an RF bandwidth of around 500 MHz in simulations whereas fig. III.35 (b) illustrates a flat gain and output power characteristics with an overall variation > 10 dB for an RF bandwidth of around 700 MHz which gives quite promising validation for the principle imagined.

Using the topology of the circuit shown in fig. III.28, multiple tuning does not allow to get higher PAE versus bandwidth than the one shown in fig. III.35 (a).

Due to this, the intrinsic loadlines of the driver stage in particular at frequency points below and above the center frequency are opened as shown in fig. III.36 which explains the limitations of bandwidth in terms of efficiency. This effect has been better managed in the concluding chapter where a new power modulator circuit with better second harmonic impedance matching within the band and a new bias architecture has been proposed.

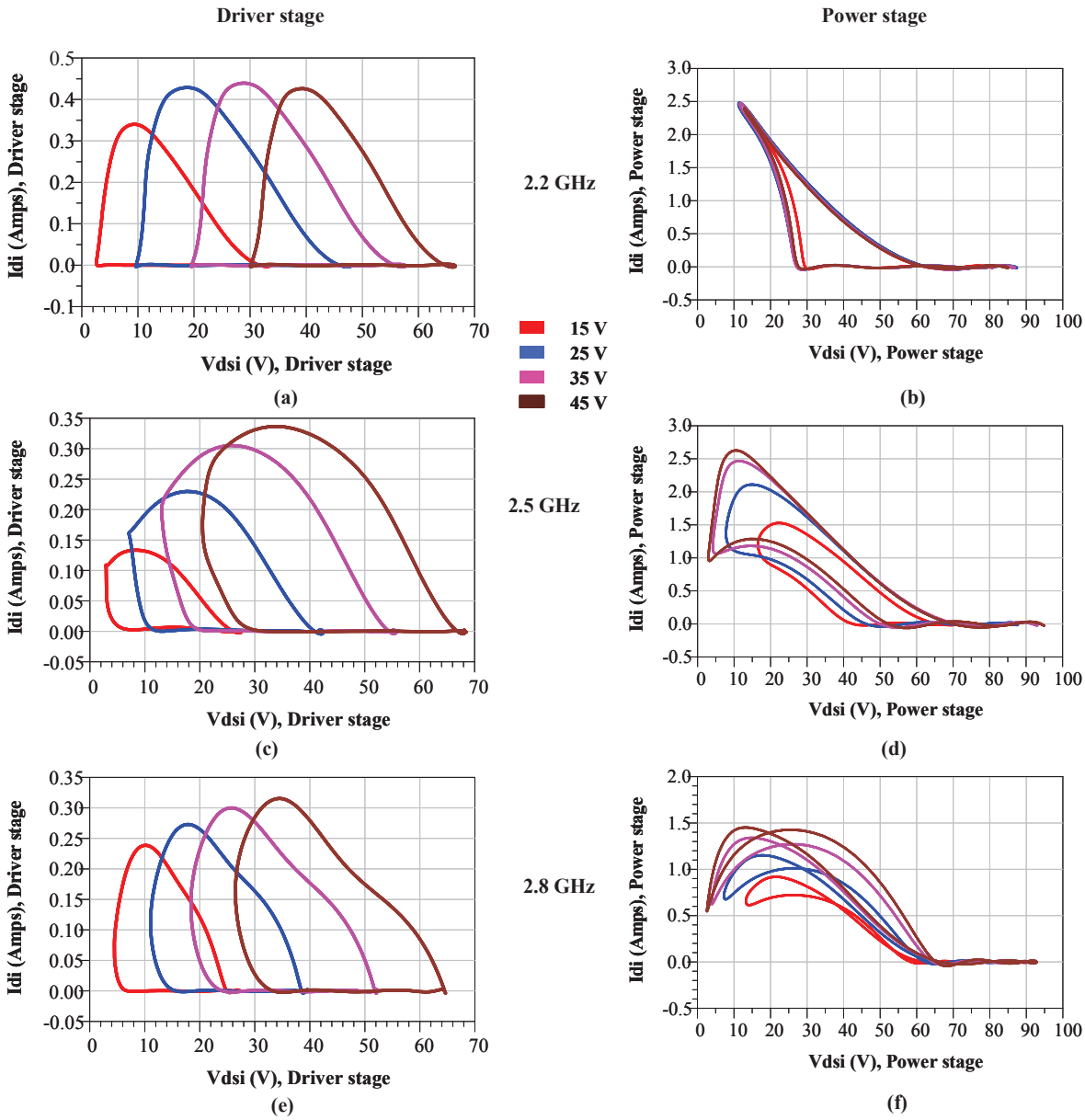

Figure III.36: Simulated intrinsic loadlines for driver and power stages (a) -(b) at 2.2 GHz, (c) -(d) at 2.5 GHz and (e) -(f) at 2.8 GHz respectively.

After the validation of the SVG principle in simulations along with the power characteristics, the next two sub-sections of this chapter illustrates the static CW and dynamic measurement results of the fabricated circuit.

5 Measurement Results

5.1 Quasi-static Measurement Results of the Two-stage Power Modulator Circuit

Fig. III.37 shows the quasi-static measurement performances [70, 71, 72] of the two-stage power modulator circuit. These preliminary measurement results gives a good indication of the validation of the principle of Saturated Variable gain (SVG) before it can be tested with the supply modulator for 16-QAM modulation schemes.

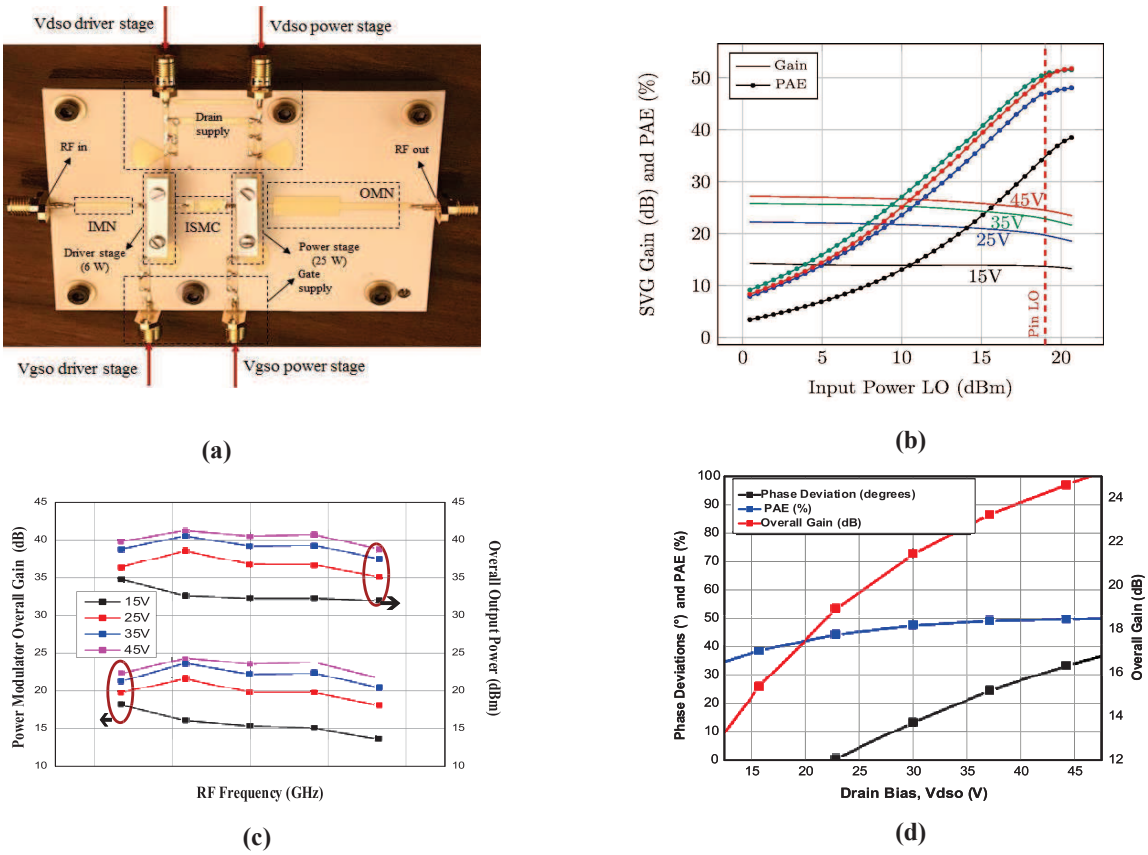

Figure III.37: Measured CW quasi-static power performances of the two-stage circuit alone (a) fabricated circuit (b) efficiency and gain variation demonstration (c) power characteristics as a function of frequency and (d) phase deviation and PAE as a function of drain supply voltage.

An important point to mention here is that due to the fabrication process and the permittivity of the substrate, there was a shift of center frequency from 2.5 GHz in simulations to 2.2 GHz in measurements.

Fig. III.37 (b) shows the static CW measured power gain and efficiency performances of the overall power modulator circuit at 2.2 GHz for 15 V < V_{dso} < 45 V. It can be observed that at constant input power LO of 19 dBm for the driver stage, the PAE values for each drain bias voltage is very close to or at saturation. At the same instant, large gain (power) variations of 11 dB from 13 dB (at 15V) to 24 dB (at 45V) is obtained in the measurements which demonstrates the SVG principle in measurements. Also, at a constant input power, the values of output powers corresponding to maximum and minimum Vdso values are 33 dBm (at 15V) and 44 dBm (at 45V) respectively with a power variation of 11 dB giving an indication for a power modulation as shown in fig. III.37 (c) for both gain and output power as a function of RF frequency demonstrating an RF bandwidth of around 400 MHz. The proposed design provides a measured PAE of 51.4% at 45V and 39% at 15V respectively at saturation. The lower efficiency at 15 V can be attributed to the accuracy of the transistor models below 20 V.

In order to validate the modulation function, fig. III.37 (d) highlights the measured overall system gain and phase variations along with saturated PAE performances versus supply voltage V_{dso}. It has to be noted that the phase deviation of the two-stage circuit is almost linear and has a smooth shape with respect to the drain supply voltage indicating that phase compensation can be implemented quite easily.

Fig. III.38 shows the simulated and measured PAE performances at center frequency for different drain bias voltages.

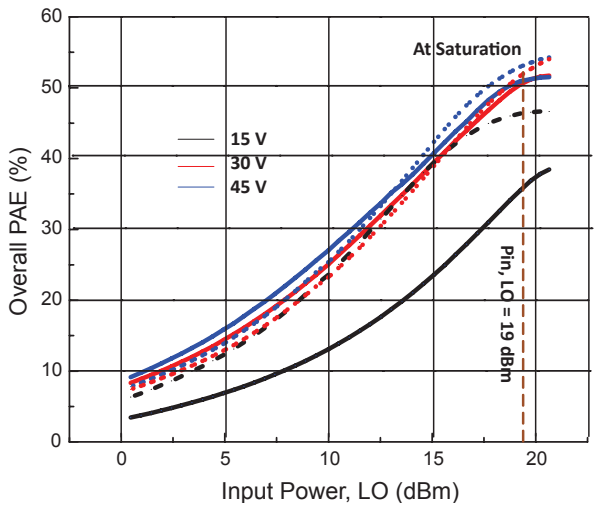

Figure III.38: Measured (full lines) and simulated (dotted lines) PAE comparison of the two-stage VPM circuit [71].

The measured and simulated performances are in a quite good agreement with each other and at saturation for a constant input power LO = 19 dBm. However the low efficiency value measured at 15 V is attributed to the effectiveness of the transistors models below V_{dso} = 20 V.

The measured PAE performances of the overall two-stage circuit as a function of RF frequency is shown in fig. III.39. It can be observed that an RF bandwidth of approximately 400 MHz is achieved over the band of interest. The decrease of efficiency at the higher frequencies can be attributed to the power level mismatch and the impact of second harmonic impedances at these frequency points as explained earlier in this chapter.

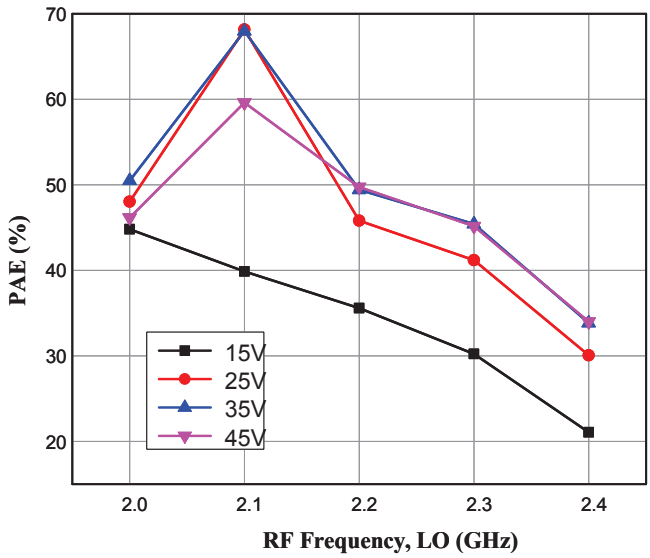

Figure III.39: Measured PAE performances of the two-stage circuit as a function of RF frequency.

5.2 Association of the Supply Modulator and the Two-stage Circuit : The Vector Power Modulator

This section of the chapter highlights the association of the two-stage GaN based power modulator with a GaN based supply modulator circuit to validate the principle of SVG for 16-QAM modulated schemes. This section begins with a small description of the hybrid supply modulator circuit used to implement the Vector Power Modulator.

5.2.1 The Vector Power Modulator Key building Blocks

This section illustrates the final objective of this thesis which is to propose a compact GaN based Vector Power Modulator circuit exhibiting Saturated Variable Gain (SVG) properties for the generation of non-constant envelope signals with high PAPR. This approach is based on the merging of digital modulation and DC to RF energy conversion functions into a single compact mixer-less module.

Fig. III.40 shows the key building blocks of the proposed vector power modulator circuit.

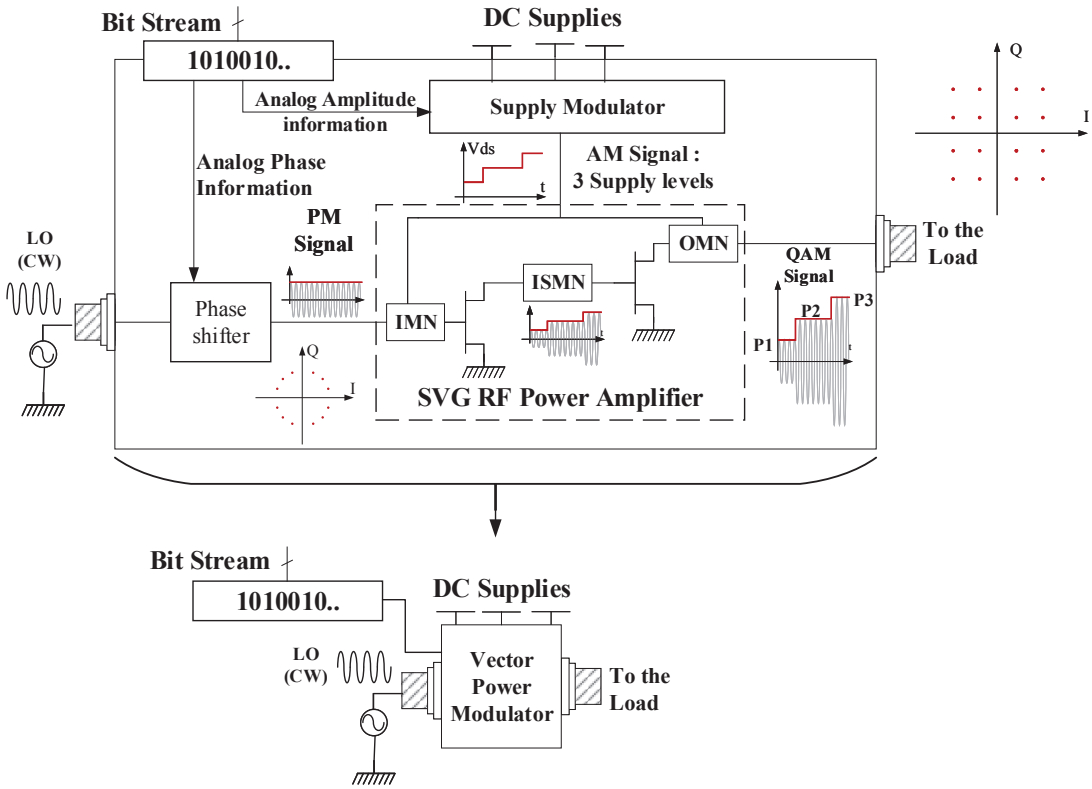

Figure III.40: Final schematic of the compact GaN based Vector Power Modulator circuit .

It is an association of a two-stage SVG amplifier (Power modulator) and a multi-level supply modulator. The overall vector power modulator combines RF modulation and energy conversion within the same module unlike conventional existing architectures. The input for the overall VPM is a phase shifted constant CW signal which acts as Local Oscillator (LO), therefore a mixerless circuit. The VPM delivers 3 gain controlled power levels at the output corresponding to 3 different bias supplies to generate a power mod-

ulated 16-QAM signal at 2.2 GHz [73]. The overall Vector Power Modulator circuit can also be considered as an RF power generation device with variable gain functionalities always operating at or very close to maximum efficiency.

5.2.2 Multi-level discrete GaN Based Hybrid Supply Modulator Circuit : Implementation and Working Principle

The multi-level supply modulator circuit has been designed as a part of thesis work of Anthony Disserand [74]. It is also a critical part of the overall system as it modulates the drain voltage levels according to the instantaneous envelope of the incoming RF signal. The efficiency and the switching speed of the supply modulator is very important in determining the overall performances of the system [22]. Therefore, to dynamically shape the output power of the SVG, a fast and efficient supply modulator has to be implemented. Fig. III.41 shows the function of the switching cells implemented for the supply modulator.

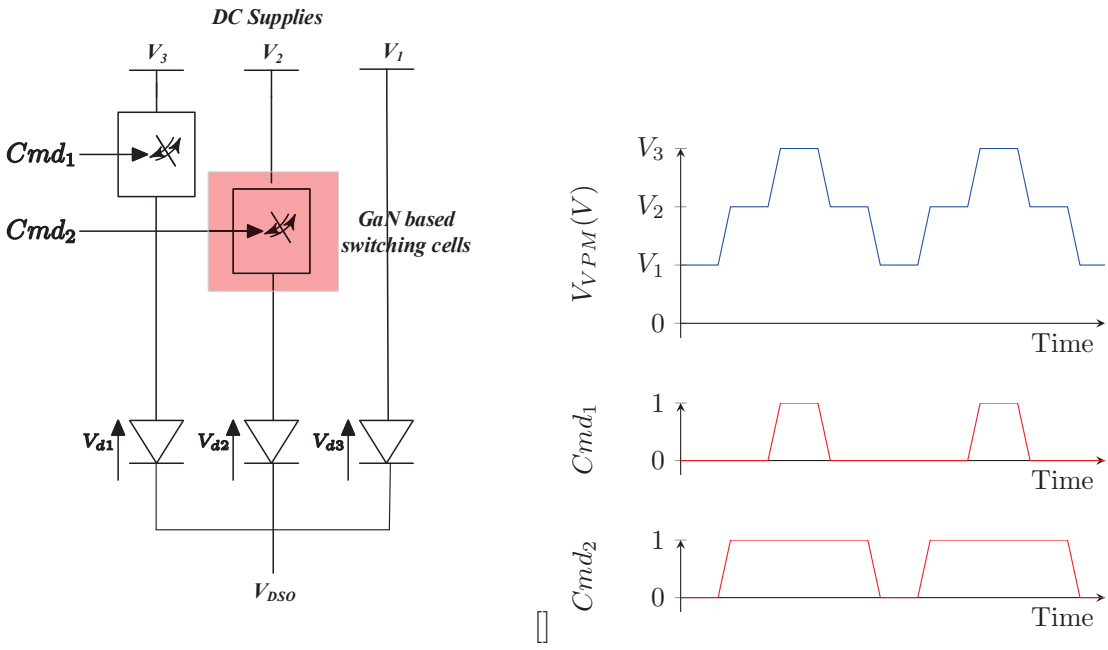

Figure III.41: Function of Switching Cells (a) Diode OR logical function implementation to the VPM output and (b) Associated output DC envelope corresponding to different drain voltages.

The number of discrete levels to generate is a function of the modulation constellation desired at the output of the SVG amplifier, three supply levels are needed for a 16-QAM. The implementation of the supply modulator is based on previously designed GaN based switches, described in [62, 75]. A switch can deliver 100 W peak power (50V on a 25

Ω load) up to 100 MHz switching frequencies. Two switching cells are combined using logical OR functions implemented thanks to fast switching diodes (fig. III.41 (a)). The diodes used here (CPWR-0600-S001B and CPWR-0600-S002B from Cree) are sized by using the maximum current flow on one hand, and by presenting a very small serial capacitance on the other hand. The supply modulator have been realized with RF GaN GH50 transistors from United Monolithic Semiconductors. These transistors have a saturated current (I_{dss}) of 0.8 A/mm [76]. Power devices grid length have been set to 10 x 8 x 150 μm (12mm) reducing by this way the equivalent resistance of the drain to source channel during saturation (0.18) and so limiting the power losses of the switch. The supply modulator implementation requires generation of a driving signal for every independent switches (fig. III.41 (b)). The supply modulator was tested alone for switching frequencies of up to 150 Msymbols/seconds with efficiency of more than 70% for voltage ranging from 10 V to 45 V respectively and a switching speed of 100 MHz.

5.2.3 Association of the Two-stage SVG and Supply Modulator Circuit

Fig. III.42 shows the association of the two fabricated GaN based circuits indicating the different voltages, input and output ports. V_1, V_2 and V_3 corresponds to the three different drain bias voltages levels coherent to 16-QAM constellation levels.

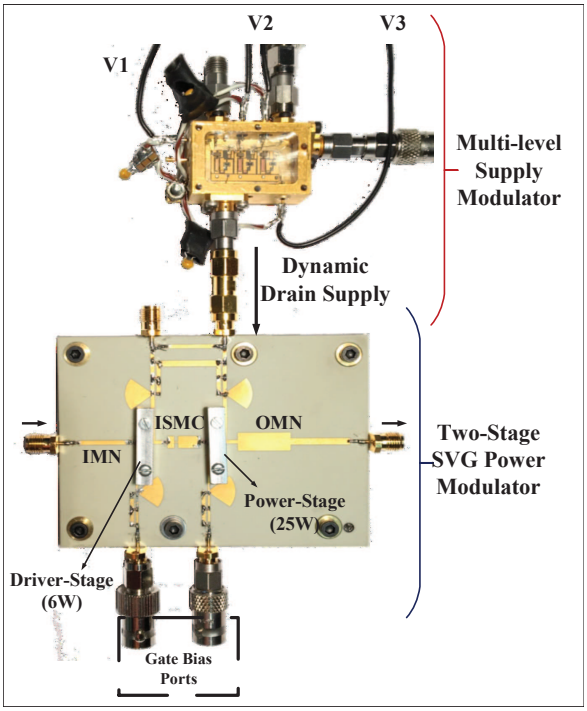

Figure III.42: Integration of the Two-stage SVGA and architecture of the multi-level supply modulator.

As both the hybrid circuits have been fabricated individually, it is very important to make sure that the drain impedance (R_{DSO}) at the point between the drain access of the two-stage power modulator and the supply modulator remains constant, otherwise there might be a loss of DC power at the expense of impacting the global efficiency of the overall system in general.

Fig. III.43 shows the simulated drain resistance (R_{DSO}) of the two-stage power modulator circuit as a function of output power for 15 V < V_{dso} < 45 V at 2.2 GHz.

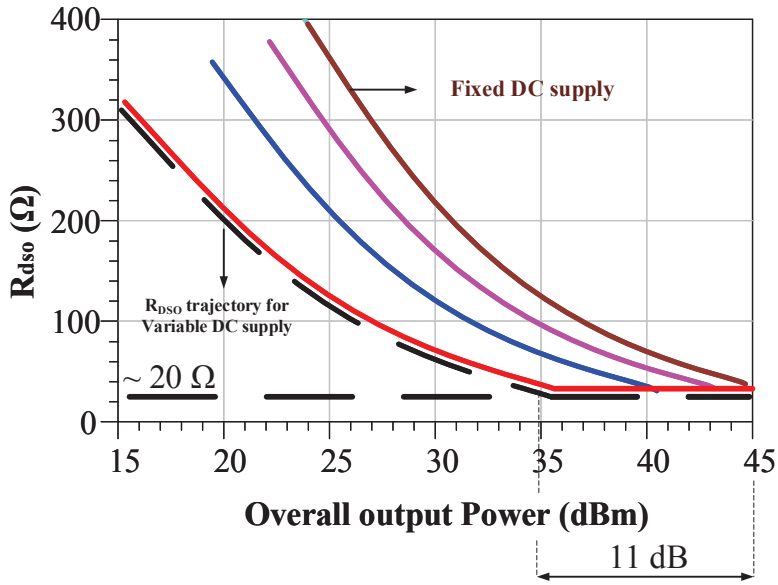

Figure III.43: Simulated static resistance presented by the power modulator circuit to its drain access for different drain bias voltages with respect to output power.

It can be estimated that with large output variations of 11 dB, the R_{DSO} values remains more or less stagnant with the drain supply voltages which gives an indication of very low DC power loss and hence lesser impact on the global efficiency. However, losses due the connectors between the drain access cannot be fully neglected in measurement procedure. Therefore, co-design of both the circuits on a single chip has been proposed as a part of future works.

5.2.4 Vector Power Modulator Dynamic Measurements

Fig. III.44 shows the photograph of the specific test bench developed in XLIM laboratory for the dynamic measurements of the Vector Power Modulator (VPM) for modulated signals.

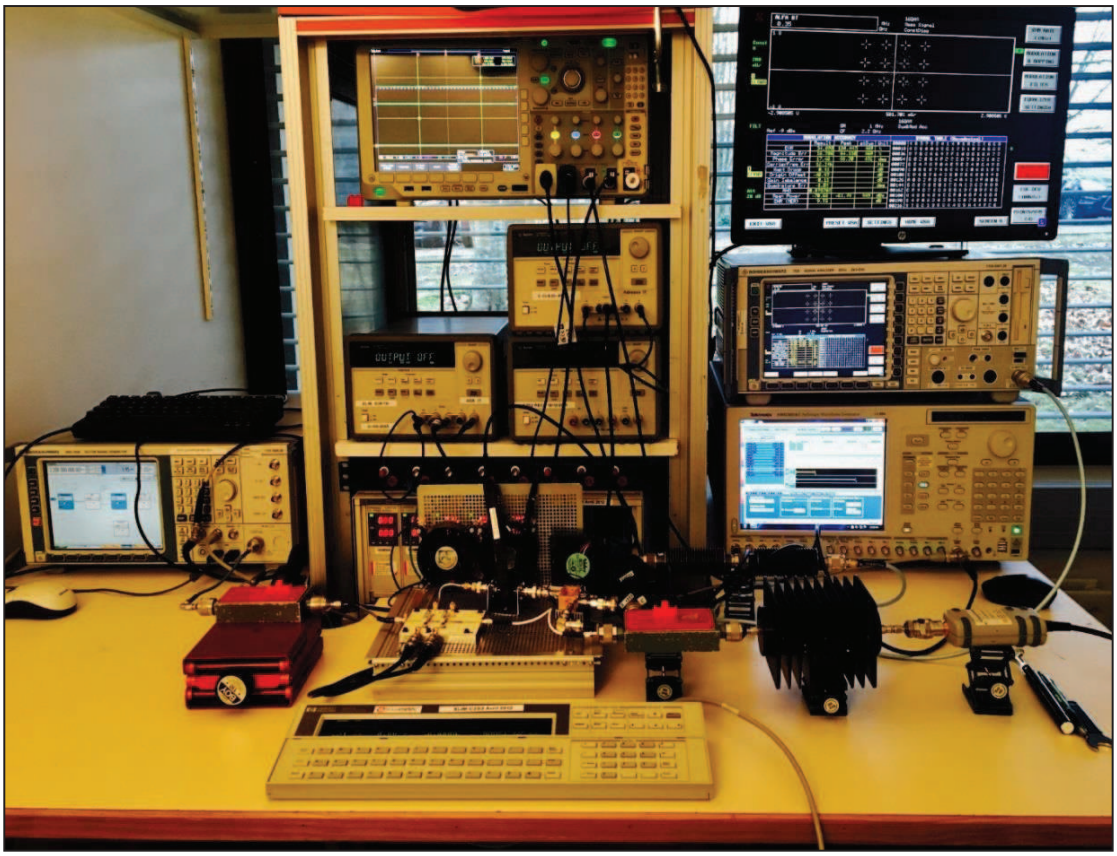

Figure III.44: Photograph of the measurement test bench.

The detailed description of the devices used in measurement procedure to validate the principle of Vector Power Modulator is illustrated in fig. III.45. The envelope test bench is equipped with a vector signal generator whose maximum frequency sampling rate is 100MHz (Rohde Schwarz SMU200A. A constant CW phase shifted input power signal acting as LO at 2.2 GHz was applied at the input of the SVG circuit. Appropriate phase shifts were done by monitoring the I-Q baseband signals of the signal modulation unit (indicated as RF source in fig. III.45). The output signal of the VPM is demodulated by using a vector signal analyzer (VSA) and I-Q baseband signals are processed to calculate and plot output envelope power variations.

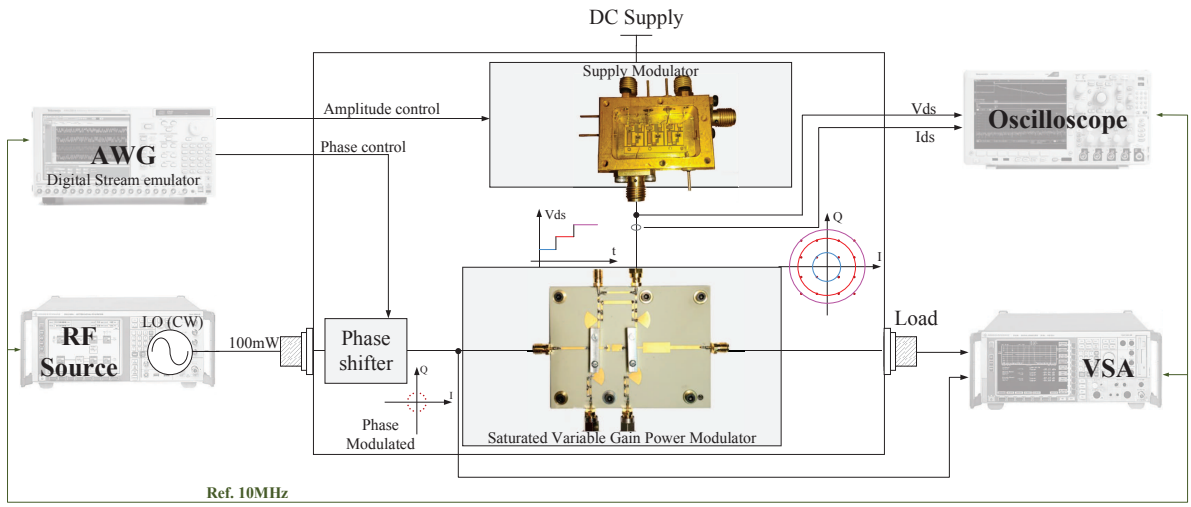

Figure III.45: Photograph of the measurement setup and description of the measurement bench.

Fig. III.46 (a) and (b) illustrates the measured dynamic large signal power characteristics of the two-stage power modulator circuit at an average input power LO of 19 dBm at 2.2 GHz.

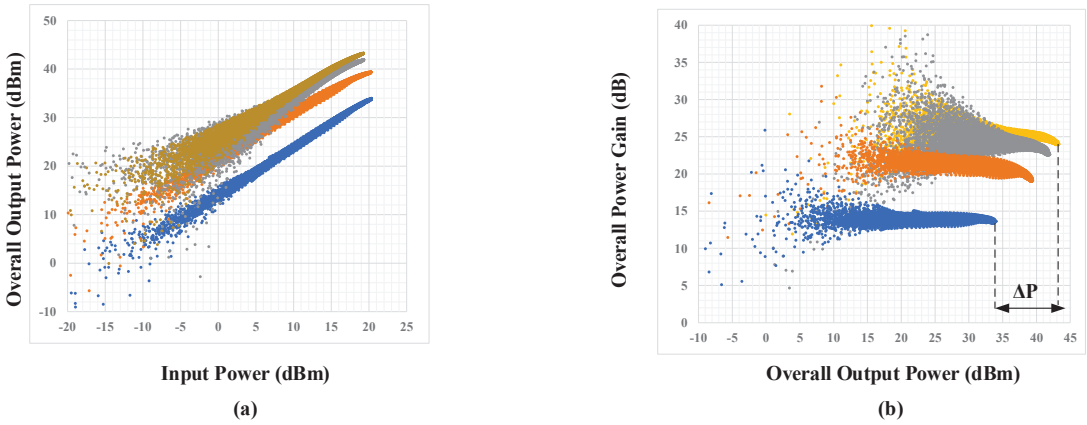

Figure III.46: (a) Measured input and output power characteristics and (b) Envelope gain variation as a function of output power at 2.2 GHz.

It can be observed from the figure that the principle of variable gain (and hence power modulation) is validated in dynamic measurements providing an 11 dB overall output power variation (fig. III.46 (b)) across the load.

Fig. III.47 illustrates the measured PAE of the overall two-stage SVG power modulator circuit at 2.2 GHz as a function of output power when the supply modulator is connected to it's drain access. It can be observed from the figure that dynamic output power ranges

from 31 dBm at 15 V to 43 dBm at 45 V providing an overall dynamic range of 10 dB at saturation.

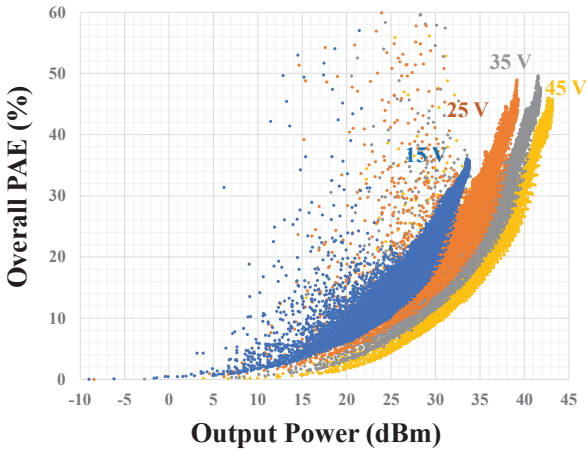

Figure III.47: (a) Measured overall PAE at 19 dBm input power LO at f_c = 2.2 GHz.

Fig. III.46 (a) and (b) and fig. III.47 further validates the concept imagined for Saturated Variable Gain.

5.2.5 Application to 16-QAM Generation

Three voltage levels were used in order to generate constellation levels for 16 QAM modulation schemes. The PC-controlled Arbitrary Waveform Generator (AWG) as shown in the fig. III.45 is synchronized to the VSG with the help of a trigger signal to implement the proper timing alignment between the envelope and RF signal at the output. In order to minimize the overall Error Vector Magnitude (EVM) performance, two steps were followed [73]: first, the amplitude information of the output modulated wave was optimized by tuning the 3 specified voltage levels of the supply modulator. Secondly, the appropriate phase shift was implemented at the input phase information plane to compensate for the Vds-to-PM distortions that occurs at the output. This gives the appropriate power levels corresponding to optimized voltage levels of 18.5 V, 31.5 V and 43.4 V for inner, middle and outer circles of the output constellation respectively as shown in fig. III.48 with dynamic range close to 10 dB.

Fig. III.48 shows the measured 16-QAM output constellations across the load for three drain bias voltages. Excellent efficiencies and output power ranges are obtained for all the three levels validating the design procedure for modulated signals.

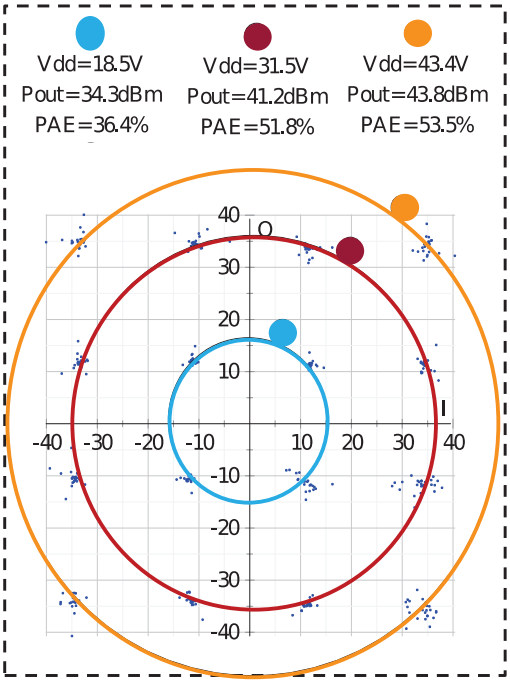

Figure III.48: Measured 16-QAM output constellations at a symbol rate of 40 Msym/sec.

Fig. III.49 shows the measured EVM and PAE of the overall system and the average PAE of the two-stage SVG RF power amplifier alone as a function of symbol rate. Good EVM (less than 5%) can be observed and power performances with high quality modulation have been achieved for high symbol rates.Similar measurements were repeated for variable symbol rates from 0.25 Msymbols/sec up to 100 Msymbols/ seconds with excellent performances in terms of data rate capabilities indicating the quality of modulation.

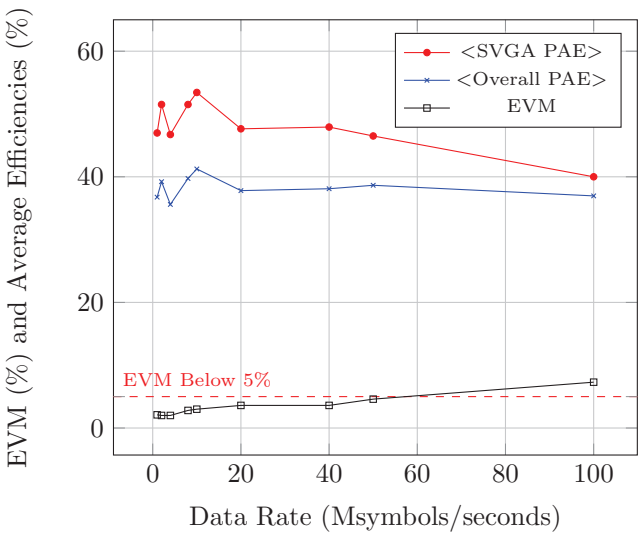

Figure III.49: Measured overall average PAE, EVM and PAE of the SVG circuit at 19 dBm average input power LO at 2.2 GHz.

One of important aspect of the dynamic measurements is that in order to validate the design principle of the Vector Power Modulator, only non-filtered output was considered for the spectrum at the output. Since this is not compliant with the currently existing systems, a possible solution to confine the spectrum of the output signal using phase filtering must be investigated.

6 Prospectives and Conclusions

In this chapter, an innovative GaN based Vector Power Modulator circuit has been proposed and experimentally demonstrated to efficiently generate wideband and high PAPR modulated RF power waves. Thanks to its direct baseband-to-RF disruptive approach, it appears very suitable to meet the needs of flexible and adaptive on board RF payload for new Adaptive Coding and Modulation (ACM) technology used in DVB S2X satellite communication standards. The proposed VPM differentiates from previously reported variable gain (VGA) polar modulators topologies [25] in its systematic design approach methodology to ensure high dynamic amplitude variations with maximum efficiency. Investigations of different performance parameters were carried out to come up with a potential circuit solution for next generation communication transmitters. Furthermore, it is believed that the proposed circuit proof of concept principle can be advantageously transposed to higher frequency e.g. Ku or Ka bands without any loss of generality because of its relative frequency agnostic topology.

As one of the most challenging aspects in designing communication transmitter is to address the trade-off between efficiency and RF bandwidth, at the same time it is also essential to make sure that the RFPA has sufficiently high video bandwidth which enables it to be digitally predistorted for linearity aspects.

One of the major drawback of conventional bias network topology is the proper optimization of second harmonics. The bias line presents ideally a short for second harmonic impedances. However, this also imposes a challenge for the design of output matching networks concerning second harmonic matching and becomes difficult to co-design both the biasing circuit and matching network.

An attempt has been made to address this issue by the use of a new bias architecture and a second Vector Power Modulator circuit based on the similar principle of Saturated Variable Gain (SVG) has been proposed in the penultimate chapter of this thesis. This new GaN based architecture consists of a novel bias architecture based on modified two-radial stub topology without any usage of frequency limited (bandwidth) shunt capacitors

in the bias lines and a newly optimized inter-stage matching circuit which takes into account the appropriate optimization of frequency bandwidth in terms of second harmonic optimization.

Chapter IV

Investigation of New Bias Architecture for Bandwidth Enhancement of Vector Power Modulator

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1 Motivation

The design of an RF power circuit requires great efforts to improve power characteristics and efficiency over large frequency bandwidth as possible. For wideband operation, the design of both bias circuits and matching circuits plays an important role to manage load impedances presented to the active cells in three frequency regions, namely the envelope or video bandwidth [67, 77, 78, 79, 80] necessary for digital predistortion techniques [81, 82, 83], the operational bandwidth at fundamental frequency and the bandwidth corresponding to second harmonic.

In this last chapter, a second version of the two-stage Vector Power Modulator circuit is proposed. The initial idea was to implement a bias circuit topology inspired from [84, 85, 86] and was initially reported to be applicable for the design of wideband bias architecture at C-band for microwave measurements.

The design procedure of the second VPM version is similar to that followed for the first version and simply begins with the implementation of the new bias architecture either for gate and drain bias of both the 6W driver stage and 25W power stages respectively.

The main objective of the second version of the VPM is to improve the overall PAE versus frequency characteristics over a wide frequency range of the first version as shown earlier in (chapter-3).

2 Presentation of the New Bias Circuit

This section highlights a new inclined two-radial stub based bias architecture investigated for the design of the new VPM circuit. The circuit topology used here is a modified two-radial stub topology as shown in Fig. IV.1.

2.1 Proposed Architecture and Comparison with the First Version

Fig. IV.1 illustrates the layouts of the first biasing circuit and the two-radial stub architecture along with the modified layout and the final fabricated version of the new biasing architecture respectively.

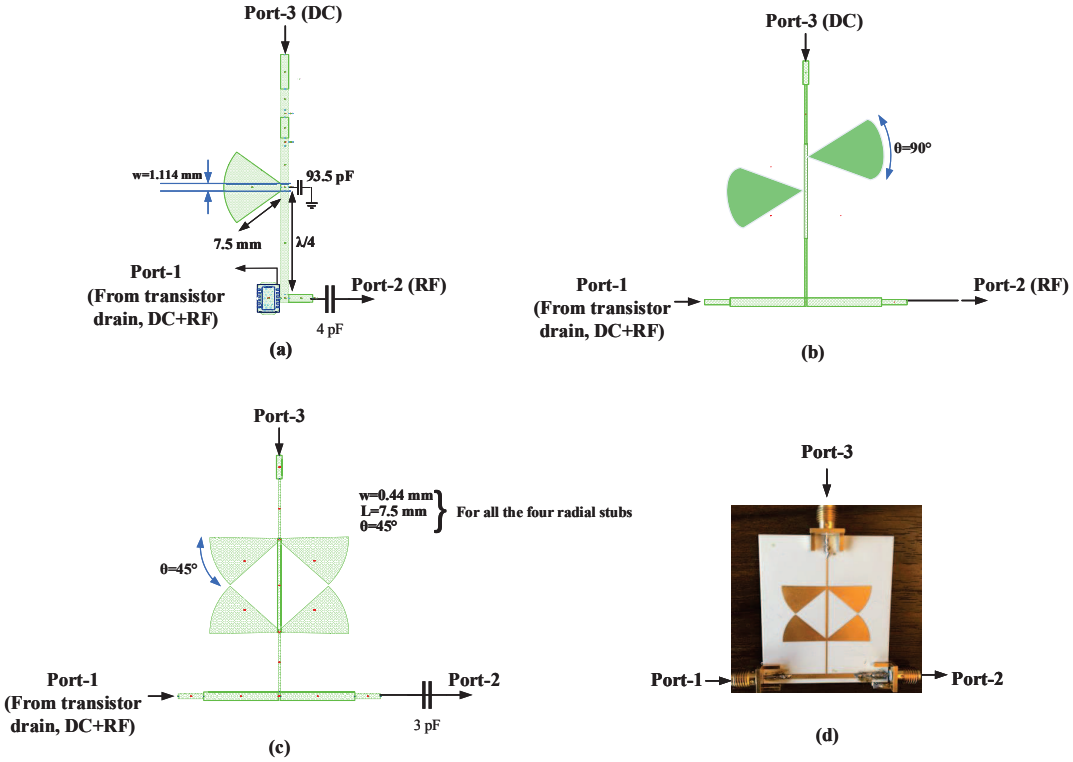

Figure IV.1: Modifications of bias network topology (a) conventional bias architecture (b) two-radial stub topology (c) modified two-radial stub topology with size reduction (d) fabricated circuit.

The combination of two cascaded radial stub is used to increase the frequency bandwidth [87]. One of the advantage is the removal of the surface mounted frequency dependent capacitor which also has a drawback of size complexity.

It has been demonstrated in [87] that the new structure which is a new single element radial stub, exhibits broadband capabilities and is compact as well. The size reduction is about 50% of an ordinary two-stub resonator and provides better isolation and is applicable to be used as biasing architecture in power amplifier design.

The selected broadband resonator originally reported for C-band applications has been scaled down to the RF bandwidth of interest (f_0 = 2.5 GHz) and has been designed using ADS momentum on Rogers RO4350B substrate.

Fig. IV.2 highlights the key comparison in simulations between the conventional and the new bias architectures respectively.

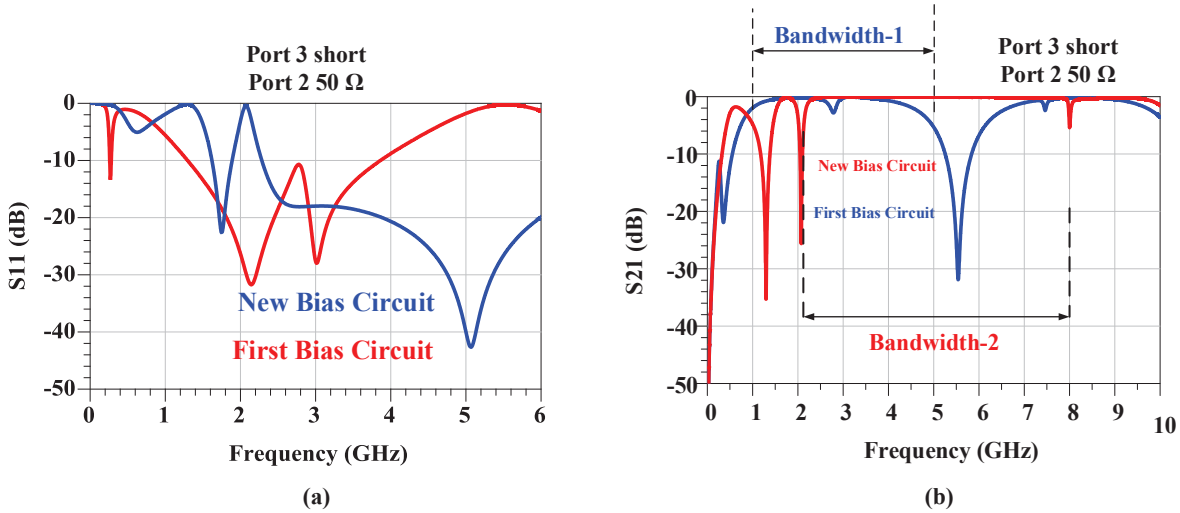

Figure IV.2: Simulated S-parameters comparison between both the output bias architectures (a) Simulated S_{11} of both the bias circuits (b) Simulated S_{21} response of both the bias circuits.

Fig. IV.2 (a) shows the simulated S-parameter drain bias response for the new and old bias architecture using real values of capacitor models. It can be observed that the S_{11} performances for the new bias architecture is less than -10 dB for almost all the bandwidth of interest (DC-6 GHz) where it is less than -10 dB for the old bias architecture between 2-4 GHz.

Fig. IV.2 (b) illustrates S_{21} comparison between the old and new biasing architectures respectively. It can be observed from fig. IV.2 (b) that the new bias circuits exhibits a flat response for a broader bandwidth.

From fig. IV.2 (b), some important observations can be made. S_{21} response of the first version of the bias topology exhibits a sharp resonance (short) in the second harmonic bandwidth (Bandwidth-1). For conventional RFPA design, ideally the second harmonic should be close to a short or should exhibit a very low impedance. This functionality is managed partly by the bias circuit and poses complexities for design of the output matching networks concerning second harmonic matching. The new biasing topology exhibits a broader bandwidth (Bandwidth-2) beyond second harmonic. This indicates that the output matching circuit is independent of the location of the second harmonic and hence provides an additional degree of freedom to manage the bias circuit and output matching independently. By changing the optimal region for the second harmonics from being close to short for the previous circuit to being inductive gives the deduction that the new bias architecture acts inductive to second harmonic but without impacting the

overall efficiency of the circuit.

As it was explained in the design procedure of the first VPM circuit in chapter-3, appropriate stability networks at the gate bias networks of both the driver and power stage (shown in fig. IV.3) were implemented to ensure unconditional stability of the overall new VPM circuit for the entire bandwidth of interest (DC- 10 GHz) as shown in fig. IV.4.

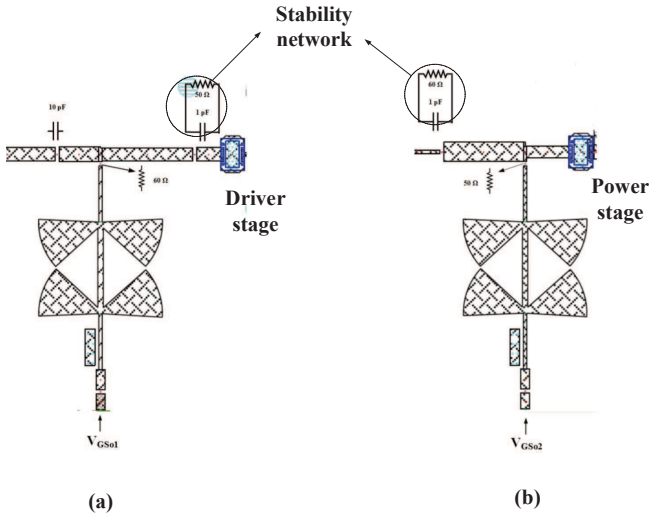

Figure IV.3: Implementation of stability networks at the input of (a) driver stage and (b) power stage respectively .

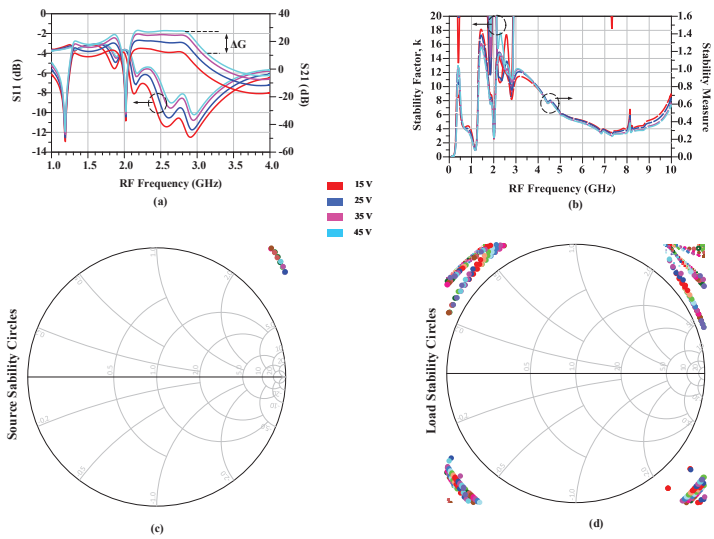

Figure IV.4: S-parameters of the new vector power modulator circuit (a) S_{11} and S_{21} (b) Stability factor , k and stability measure (c) Source stability circles and (d) Load stability circles .

3 Vector Power Modulator Design with New Bias Circuit

The design procedure of the new circuit is similar to that of the first circuit and starts with the designing of the power stage first. The analysis presented in this chapter is associated with the design of the overall circuit therefore, the detailed procedure of designing individual stages have not been repeated again.

Loadpull simulations with both fundamental f_0 and second harmonic $2f_0$ were optimized targetting maximum efficiency performances similar to that of the first circuit at different frequency points and at different drain bias voltages for both the driver and power stages.

Fig. IV.5 shows the load impedances of the power and driver stage transistors as a function of frequency at V_{dso}= 40 V obtained from loadpull when both f_0 and $2f_0$ are optimized for maximum PAE performances. The load impedance loci are obtained when the new bias circuit and appropriate stability networks are connected to the transistors.

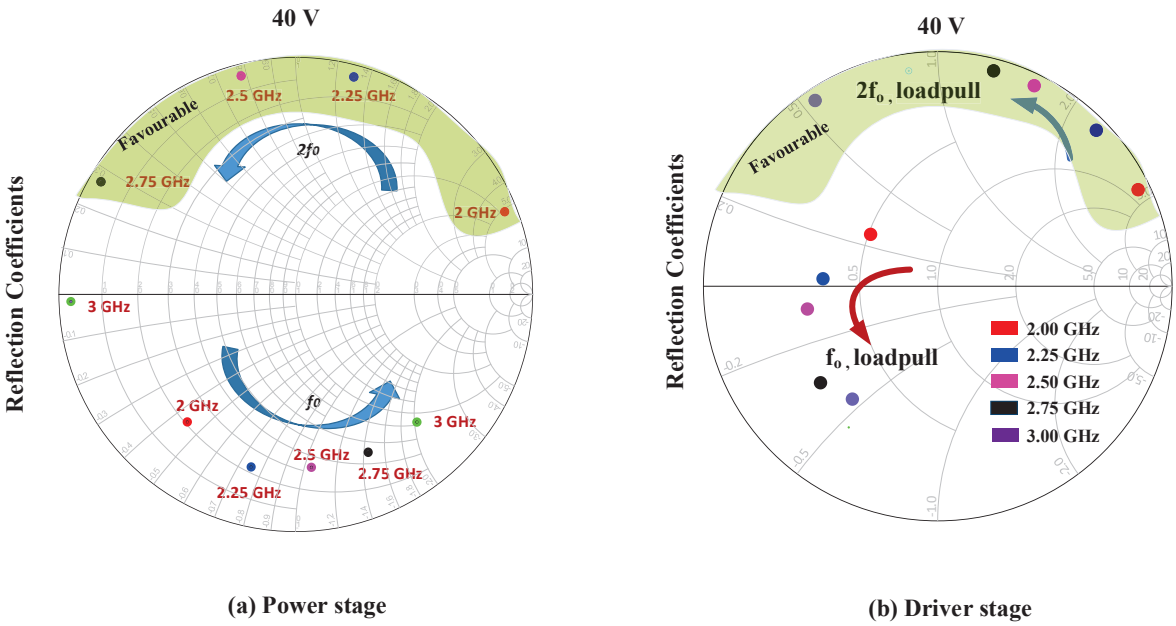

Figure IV.5: Location of load impedances for the power and driver as a function of frequency obtained from loadpull simulations.

It can be observed from fig. IV.5 (a) and (b) that the favourable region corresponding to high PAE for second harmonic is not close to short (as in the case of first circuit) but is inductive. This is due to the fact that no coupling capacitors have been used in the

design process. Another information that can be obtained is that the variation of second harmonic versus frequency depends on the architecture of the bias network itself.

This also gives an additional degree of freedom to design the interstage matching circuit and the bias circuit individually as compared to a conventional bias architecture where the trade-off power mismatch at second harmonic (ideally close to short) like in the case of first circuit can be managed more efficiently leading to improved performances.

3.1 Design of the New Vector Power Modulator Circuit

Fig. IV.6 shows the layout of the new vector power modulator circuit with the stability networks , input, output matching network and newly optimized interstage matching circuit with the new biasing architecture.

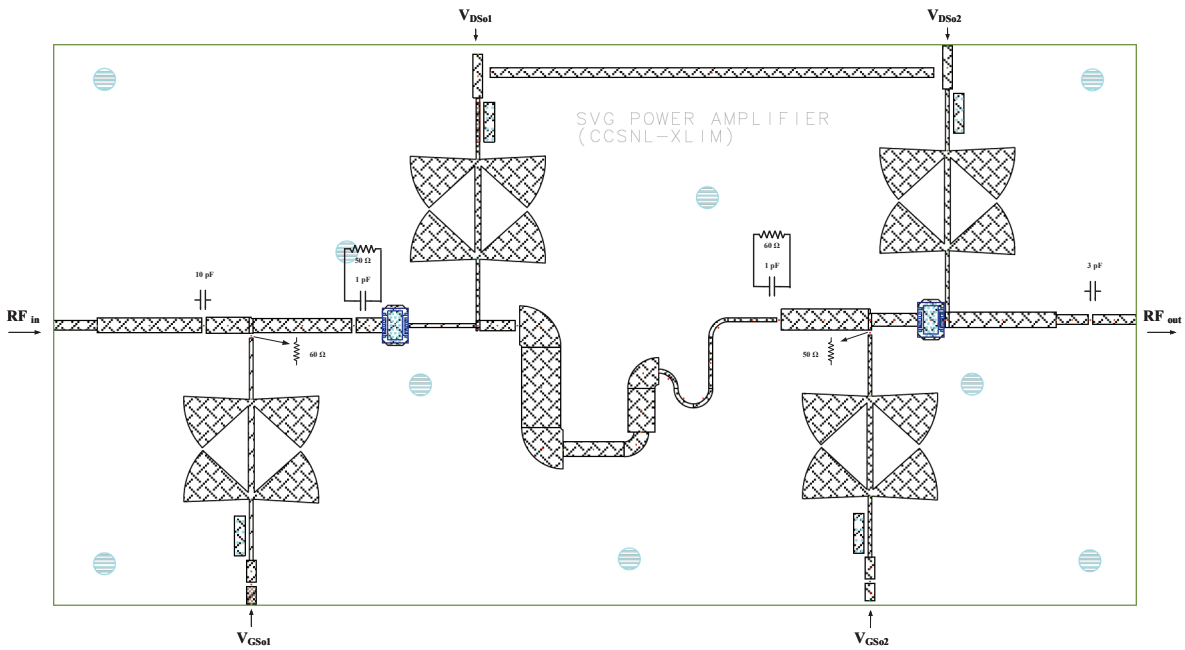

Figure IV.6: Layout of the new two-stage power modulator circuit.

It has to be noted from fig. IV.6 that the overall circuit has been designed with no parallel stubs which could act as a limiting factor in terms of RF bandwidth of the circuit.

The design procedure for the interstage matching circuit involves firstly the power matching of the load impedance of the driver stage to the input impedance of the power stage at center frequency and at a constant input power LO for the driver stage and then optimizing it for different frequency points within the band of interest as it was done for

the first circuit.

Fig. IV.7 shows the layout of the newly optimized interstage matching circuit designed using Genesys first using stepped impedance lines. Then the geometry was optimized to make the overall circuit compact and verified using ADS Momentum .

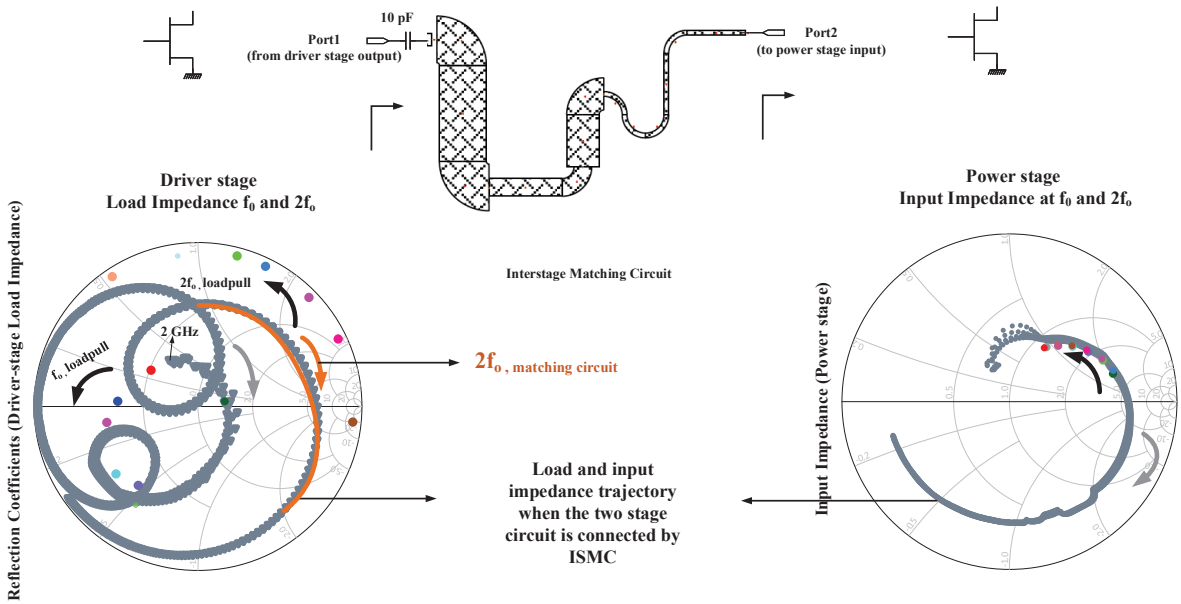

Figure IV.7: Newly optimized inter-stage matching circuit for the new power modulator circuit. The optimum load impedances of the driver stage and the input impedances of the power stage as a function of frequency obtained from loadpull simulations and the impedance trajectory when the inter-stage matching circuit is connected to the two-stage circuit are highlighted.

Fig. IV.7 also shows the optimum load impedance of the driver stage and input impedance of the power stage at f_0 and $2f_0$ as a function of frequency for V_{dso}=45 V obtained from load pull simulations along with the trajectory of the impedances at the input and output of the interstage matching circuit when the overall two-stage circuit is connected together and simulated in Harmonic Balance over a frequency sweep and for 15 V $< V_{dso} < 45V$.

The trajectory at the input and output of the interstage matching circuit is very close compared to the impedance obtained from loadpull analysis for both f_0 and $2f_0$. This gives an indication of better power matching. This optimization will be quite significant with respect to the overall performances of the circuit with respect to frequency.

The size of the interstage matching is slightly longer as compared to the circuit designed for the first VPM. This has been done in order to better power match the optimum load and input impedances and for better RF bandwidth with a very small impact on the overall efficiency performances.

3.2 Performances of the New Vector Power Modulator Circuit

Fig. IV.8 shows the simulated power characteristics of the overall new two-stage circuit as a function of input power.

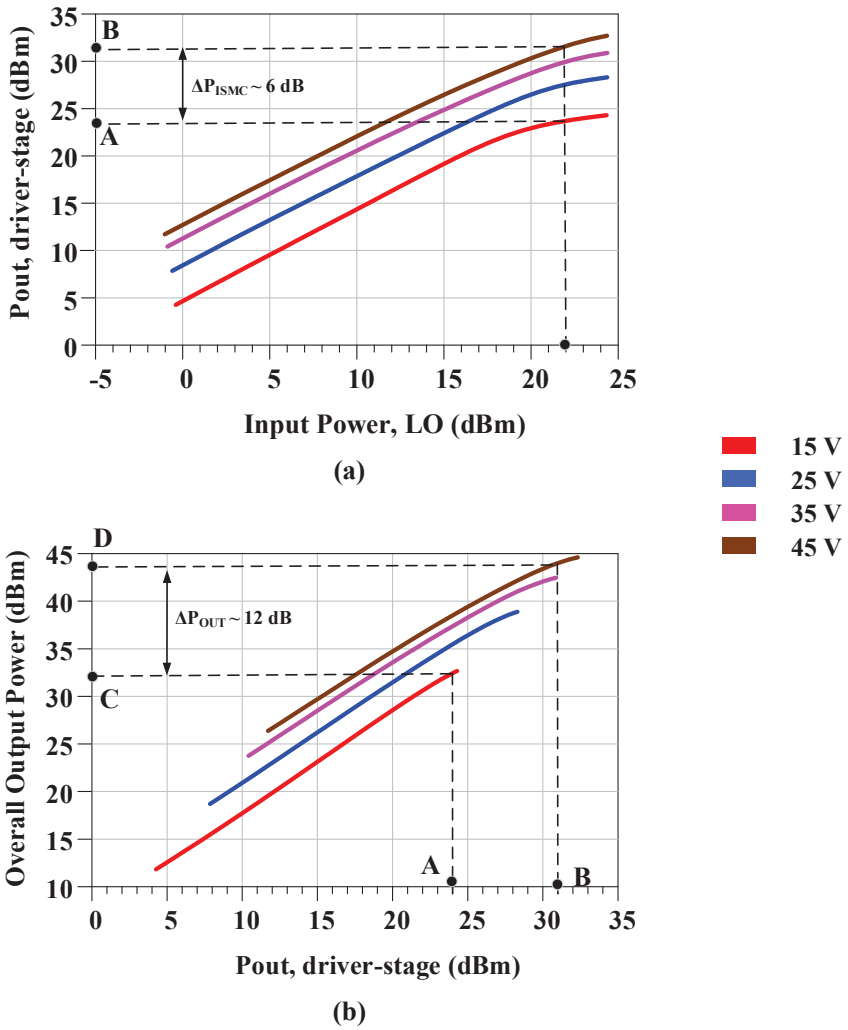

Figure IV.8: Power characteristics of the driver and power stages respectively demonstrating the overall output power variation at center frequency of 2.5 GHz .

It can observed from fig. IV.8, that from simulations, at a constant input power LO of the driver stage of 22 dBm, the variation of power at the input of the power stage is 7

dB corresponding to 24 dBm at V_{dso}= 15 V to around 31 dBm at V_{dso}= 45 V as shown in fig. IV.8 (left) indicated by points A and B.

At the same input power variations, the overall output variations across the load is 12 dB corresponding to 32 dBm at V_{dso}= 15 V to around 44 dBm at V_{dso}= 45 V as shown in fig. IV.8 (right) indicated by points C and D. Under these conditions, if the overall efficiency and gain of the novel two-stage circuit is analyzed, as shown in fig. IV.9, it can be observed at a constant P_{in}, LO = 22 dBm at center frequency of 2.5 GHz, the gain variation of 12 dB is always at maximum efficiency corresponding to 15 V $< V_{dso} < 45V$.

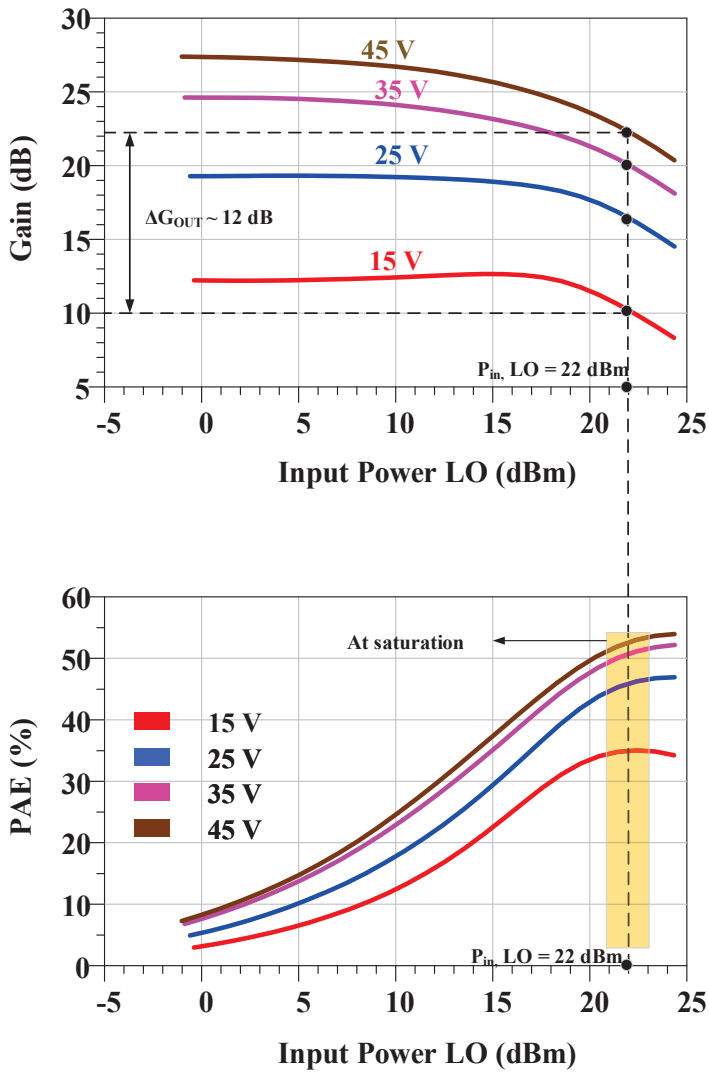

Figure IV.9: Illustration of the Saturated Variable Gain (SVG) principle for the new power modulator circuit at input power of 22 dBm and at a center frequency of 2.5 GHz.

Hence, the principle of Saturated Variable Gain (SVG) [72] with the new biasing

architecture has been validated at center frequency. The next steps involves the effective demonstration of this principle over a range of frequency points and its comparison with the first circuit employing the conventional biasing architecture. This involves the comparison of the driver stage performances over a range of frequencies.

3.3 Comparison between Previous and the New Vector Power Modulator Circuit

This section highlights the comparative analysis of the old and the new VPM circuits in terms of RF and video bandwidths respectively.

3.3.1 Comparison in terms of RF Bandwidths

Fig. IV.10 illustrates the comparative analysis of the dynamic loadlines of the drain current source of the driver and power stages respectively of both the circuits at center frequency (2.5 GHz).

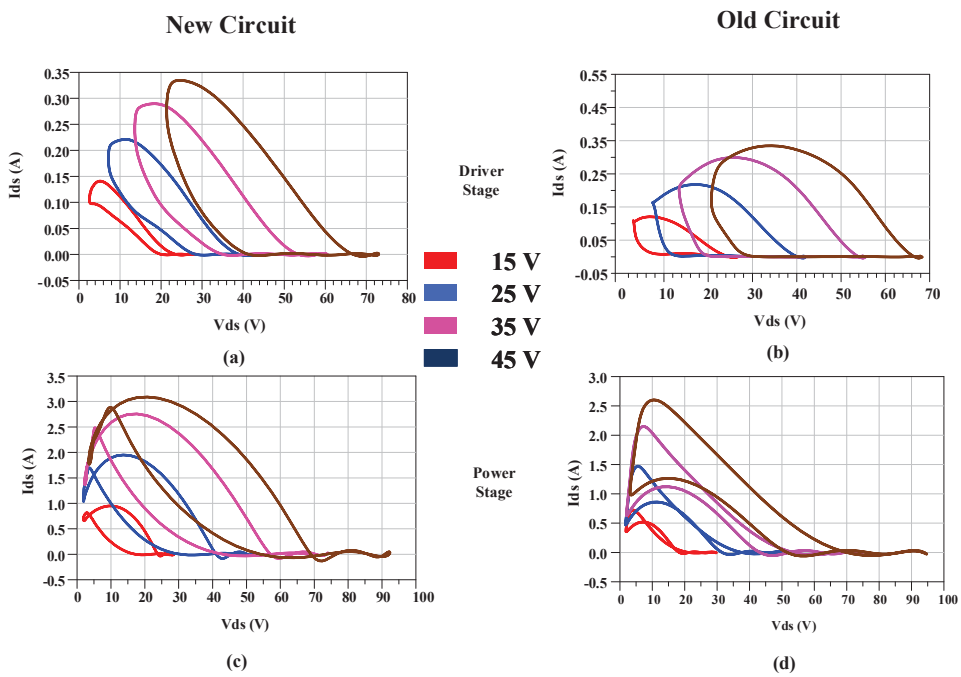

Figure IV.10: Dynamic loadlines of the drain current source of the driver and power stages respectively for the old and new circuits.

It can be observed from fig. IV.10 (a) and (b) that the dynamic loadlines of the driver stage for the new circuit is closely spaced compared to that of the old circuit which is

opened enabling a better voltage swing. On the other hand, it can be observed from fig. IV.10 (c) and (d) that the peak current in the power stage with new biasing architecture is slightly high which might have a small impact on the overall efficiency performances of the circuit.

Fig. IV.11 shows the corresponding intrinsic time domain waveform of the driver and power stages respectively of the new circuit optimized for maximum PAE at an input power corresponding to 22 dBm for the driver stage and frequency equal to 2.5 GHz.

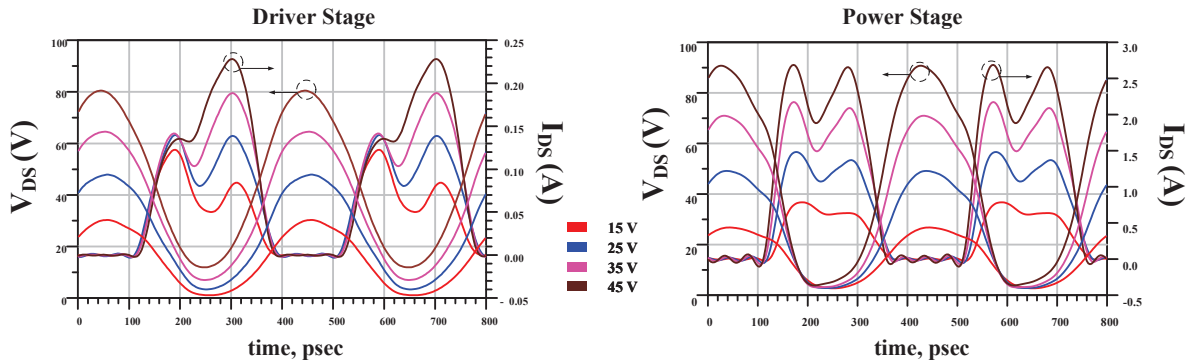

Figure IV.11: Intrinsic time domain voltage and current waveforms at center frequency and P_{in}=22 dBm for the driver and power stages respectively.

The dynamic loadlines at different voltage levels are optimized quite well with very small openings indicated for good efficiencies by the area under the overlap between the intrinsic drain voltage and current waveforms.

Once the overall performances of the two-stage circuit has been demonstrated at center frequency, the following sections involves the performance analysis over a wide range of RF bandwidth. The proper design of the driver stage circuit has a significant impact on the overall performances of the two-stage circuit as it has been established from the design procedure of the first circuit.

Two things have to be carefully taken into consideration during the design procedure. First, the performances of the driver stage circuit at center frequency as illustrated in fig. IV.10 and fig. IV.11. Secondly, to make sure that the overall RF bandwidth is acceptable, it is also necessary to optimize the driver stage performances individually for the fundamental and second harmonic respectively at different frequency points. This has been ensured by the designing and optimization of the new interstage matching circuit which has shown significant performance improvement for the driver stage at fundamental

and second harmonics. This difference can be clearly observed from the dynamic loadlines of the driver stage circuit alone and its comparison with the driver stage performances of the old circuit at different frequency points as shown in fig. IV.12 which shows that the dynamic loadlines of the driver stage in the new circuit is better optimized which is encouraging for enhanced performances within the band of interest.

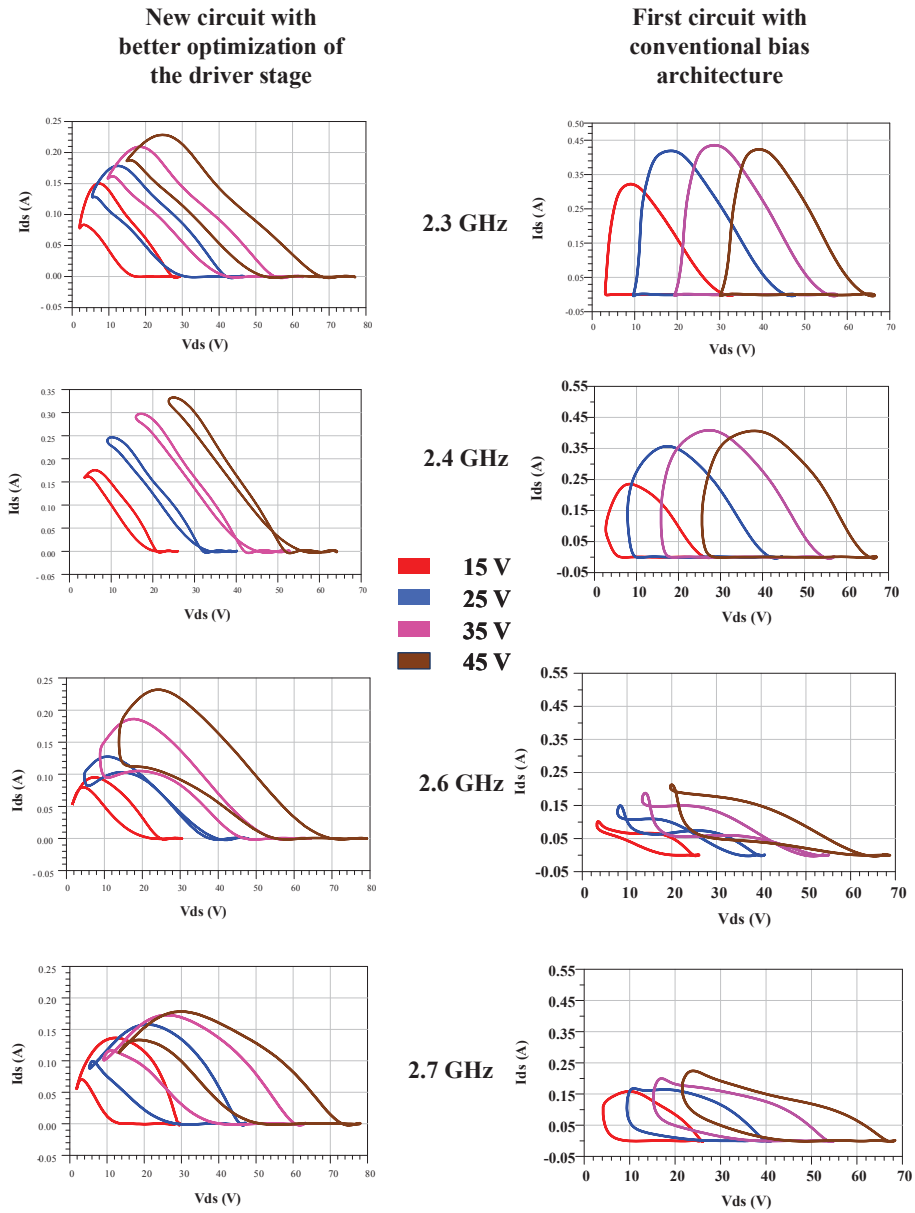

Figure IV.12: Comparison of the driver stage current source dynamic loadlines at different frequencies for P_{in}=22 dBm (new circuit), P_{in}=19 dBm (first circuit) and 15 V < V_{dso} < 45 V.

Fig. IV.13 illustrates the RF bandwidth comparison between the new proposed and the old two-stage circuit in simulations.

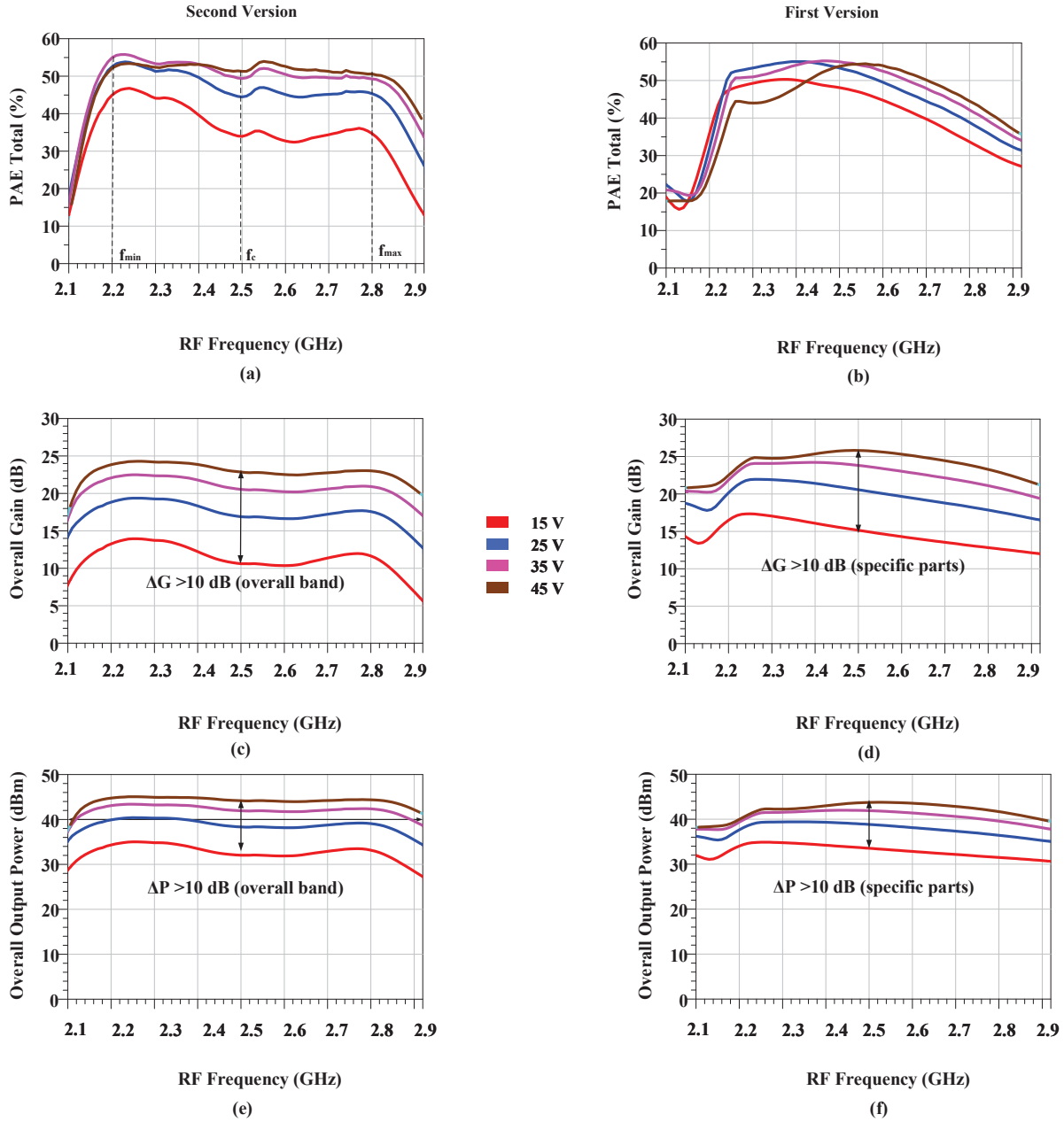

Figure IV.13: Comparison of the simulated power characteristics as a function of frequency for the first and second power modulator circuits (a) PAE of the new circuit (b) PAE of the first circuit (c) Overall gain of the new circuit (d) Overall gain of the first circuit (e) Overall output power of the new circuit and (f) Overall output power of the first circuit.

It can be observed from fig. IV.13 that the power gain and output power characteristics of the first VPM circuit is quite constant over wide frequency range however the PAE performances tends to fall sharply at frequencies above the center frequency.

Thanks to the better optimization of the second harmonic using a new interstage matching circuit and the bias circuit topology, it can be observed that the power charac-

teristics have been managed better above and below the center frequency with an overall dynamic range of above 10 dB for an RF bandwidth of 700 MHz compared to around 400 MHz for the old circuit showing a significant improvement versus frequency.

However, the low efficiency performances at V_{dso}= 15 V can be attributed to the accuracy of the packaged GaN transistors below 20 V as mentioned in their respective data-sheets [19, 20].

Finally to summarize the large signal performances of the new circuit, fig. IV.14 illustrates the simulated AM-PM performances at center frequency of 2.5 GHz. It is important to analyze the AM-PM conversion as the input of the overall two-stage circuit is a phase modulated CW signal. It can be observed that there is very less phase distortion with respect to the drain supply voltage which validates the design procedure.

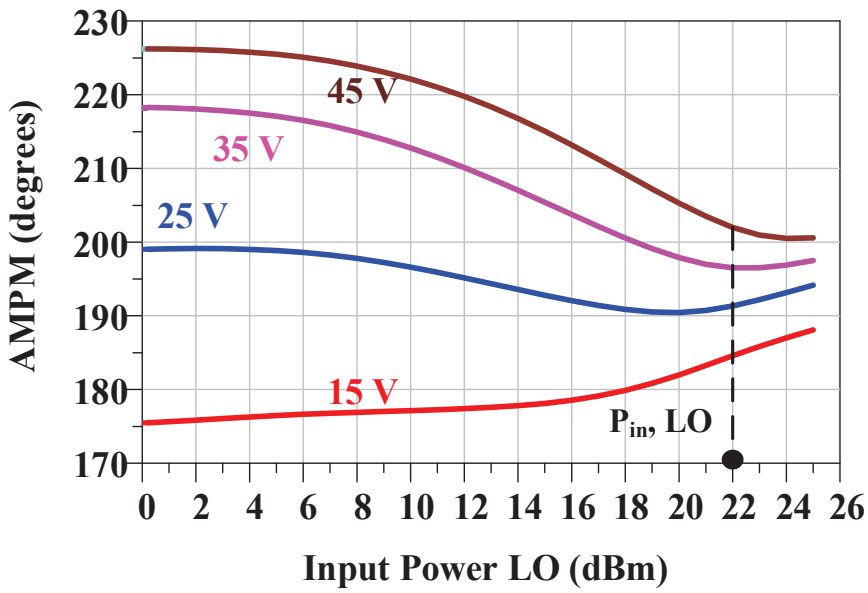

Figure IV.14: AM-PM of the new power modulator circuit as a function of input power at f_0=2.5 GHz.

Fig. IV.15 shows the power characteristics of the new version of the Vector Power Modulator circuit in simulations as a function of drain supply voltage, V_{dso}. The results corresponds to three different frequencies f_{min}, f_c and f_{max} respectively at 2.2 GHz, 2.5 GHz and 2.8 GHz respectively.

It can be observed from fig. IV.15 that the power characteristics varies quite linearly in shape with respect to drain supply voltage V_{dso}. This also validates the key charac-

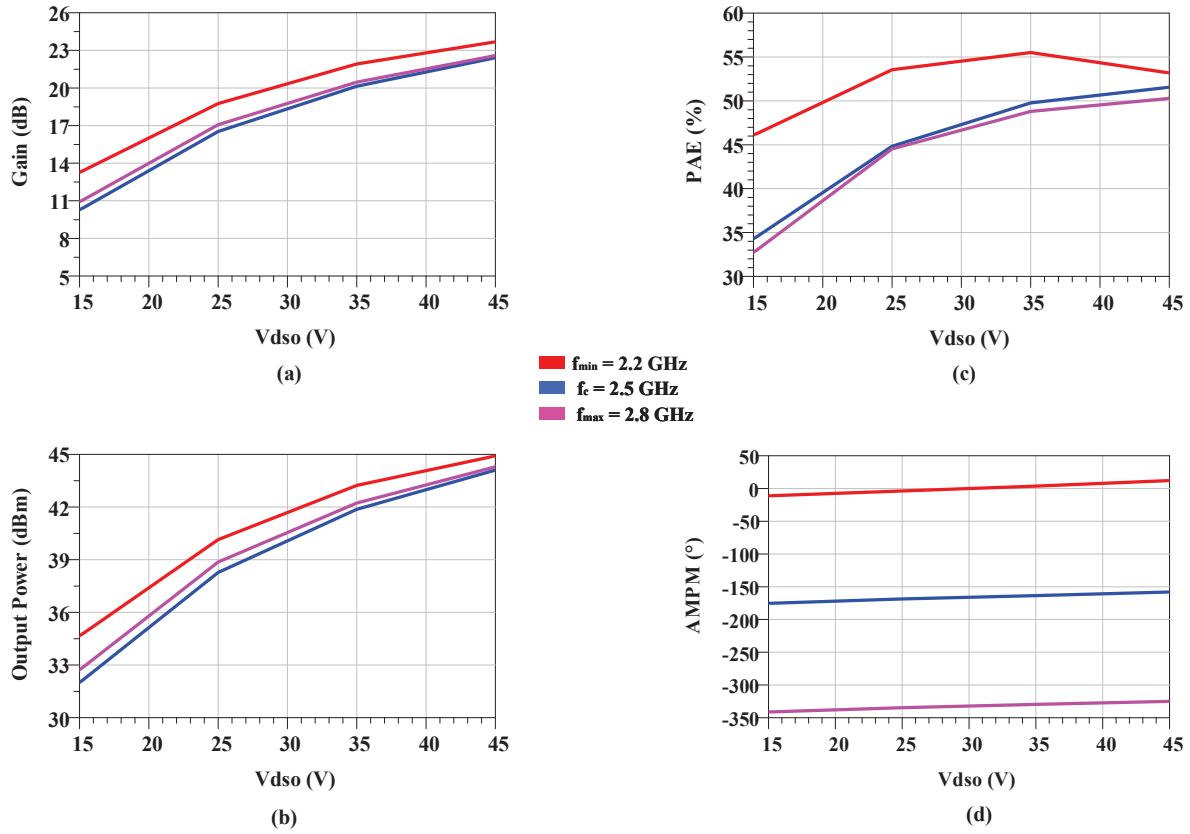

Figure IV.15: Power characteristics at different frequency as a function of drain supply voltage V_{dso} (a) Gain (b) PAE (c) Output power and (d) AM-PM.

teristic features of a modulator and hence validating the concept for the new VPM version.

4 Conclusions

This chapter has presented the investigations on the trade-off between RF and video bandwidths of RF power amplifier and has presented a new biasing architecture topology based on four radial stubs inclined at an angle of 45 degrees forming a compact broadband resonator.

This chapter has also highlighted the design procedure of a new and compact inter-stage matching circuit which is better optimized for the second harmonic impedances both for the output of the driver stage and input of the power stage respectively. The simulated comparative analysis in terms of power characteristics at center frequency and within the band of interest has also been illustrated.

The new biasing topology has shown some promising features especially in terms of bandwidth enhancement. This can be attributed to the inductive behaviour with respect to the second harmonic load impedance of the novel resonator. Several investigations to improve the performances further can be implemented like the co-design of the supply modulator and the two-stage SVG circuit together to minimize the effect of drain access impedance of the SVG circuit on overall performances.

A new technique could be deduced for application of a suitable spectral mask at the output of the first and new proposed circuit as it is a non-filtered output. The new proposed two-stage power modulator circuit has been fabricated but was not evaluated in measurements because of the unavailability of the transistors model in time. The measurements of the new circuit can be very interesting to make a potential trade-off between RF and video bandwidths for digital predistortion [88] of power amplifiers.

In general, both the proposed two-stage SVG circuits have shown considerable potentialities in addressing the efficiency versus linearity issues of modern power transmitters and this analysis seems to be very useful for investigation of next generation future communication transmitters for high PAPR signals.

General Conclusions and Perspectives

The never ending demands of subscribers for effective connectivity have kept designers to always investigate new and efficient transmitter architectures for signal processing to meet the demands. Due to the constant evolution of wireless communication systems for integration of multiple functionality together, the designers have to come up with several complex modulation schemes like n-QAM, OFDM [89] etc. These spectral efficient modulation techniques have tremendously led to the increase in channel capacity in terms of bandwidth but at the cost of increased Peak to Average Power Ratio (PAPR).

When such high PAPR signals are transmitted over a wireless medium, RF power amplifier designers have to encounter additional issues to maintain an acceptable amount of average efficiency by maintaining the signal quality as well because the envelope of high PAPR signals are non-constant. As a result of this, the power amplifier is operating at maximum efficiency close to saturation whereas efficiency is degraded in order to keep the signal integrity intact. Another factor associated with such conventional transmitter architectures is that the amplification function and the modulation function are implemented as separate blocks of the overall system which adds on more complexity.

This thesis work in general is an attempt to investigate some of the main design challenges for RF power transmitter architectures for high PAPR signals and proposes certain new topologies for high efficiency and dynamic range functionality by the use of commercially available high power 50 V GaN-HEMT technology.

In this context, the **First chapter** of this thesis has highlighted the basics of conventional RF power transmitters and the main design parameters to be taken care of like efficiency, linearity, output power and gain. It has also presented the recent trends in GaN wide-band gap semiconductor technology along with the description of the devices used in this work.

The **Second chapter** has been an attempt to illustrate first the characteristics and Figures of Merit for non-constant envelope signals and some of the commercially implemented high efficiency transmitter architectures based on fixed saturated gain (Doherty and Envelope Tracking) and variable saturated gain (Envelope Elimination and Restoration [EER] and Outphasing) and their main design issues and principle using simulations in ADS. It also explained the selection of the proposed circuit based on saturated variable gain for the design procedure.

The **Third chapter** has proposed complete design procedure, implementation and measurement results of a new two-stage Vector Power Modulator (VPM) circuit [72] operating on the principle of supply modulation. This principle acts as an improvement over conventional EER architectures. The proposed principle has also proven effective in terms of compactness of the circuit by the merging properties of modulation and amplification (DC-RF conversion) functions into a single mixer-less module which is the principle objective of this thesis work. The principle of gain transfer has also been explained in this chapter. This has demonstrated a dynamic range of > 10 dB for an Rf bandwidth of around 400 MHz with maximum efficiency. Along with the design procedure, this chapter has demonstrated the association of the two-stage SVG circuit with a GaN based discrete supply modulator [62] for the principle of supply modulation that has led to defining the term **Vector Power Modulator** for the overall system. This has been tested for 16-QAM modulation schemes up to a symbol rate of 100 Msym/sec and has shown excellent modulation qualities in terms of EVM $< 7\%$ for symbol rates upto 100 Msym/sec. The overall principle can be summarized as a proposition of a device that generates high efficiency analog modulated power waves at the output by processing digital information at the input.

The **Final chapter** of this thesis work is dedicated to the investigation of trade-off between video and RF bandwidths respectively. This has enabled the proposition of a new and compact broadband resonator for biasing architecture based on the combination of four radial stubs. Additionally, an improved inter-stage matching circuit optimized for second harmonic impedance and a novel two-stage SVG circuit has been designed and fabricated. However, the new transistor models available from Wolfspeed shows large current dispersion compared to the old models and the reason is being currently investigated, the measurements were therefore not possible on time. The new two-stage circuit shows improved performance in terms of dynamic range (12 dB), and RF bandwidth in simulations which shows the potential of the proposed circuit. A comparative analysis between the old and new power modulator circuits has also been commented upon in

terms of RF and low frequency characteristics.

There are certain interesting perspectives that can possibly be investigated for the future extension of this work. This involves the replacement of the standard load with an active integrated antenna for phased array and beam forming applications for enhanced efficiency performances [90, 91, 92]. Another possibility is the MMIC co-design of the supply modulator and the two-stage SVG circuit with optimum sizing of driver and power devices for mitigating the effects of the losses due to the impedance mismatch at the drain access of the two-stage SVG circuit.

The third perspective that can be applicable is the implementation of a suitable spectral mask [93] at the output of the overall two-stage circuit. Finally, there are many possibilities for enhanced efficiency by parallel connection of two or more such SVG circuits but at the expense of system complexity and to go for higher modulation schemes like 64-QAM and also adaptive modulations [94] for MIMO systems.

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List of Publications

-Abhijeet Dasgupta, Anthony Disserand, Jean-Michel Nébus, Audrey Martin, Philippe Bouysse, Pierre Medrel and Raymond Quéré, **High Speed and Highly Efficient S-Band 20 W Mixerless Vector Power Modulator**, in IEEE-MTT IMS-2017, Honolulu, Hawai'i. **(Best Paper and Poster Award IEEE-MTT(s) France Section, BEE Week-2017, Bordeaux)**

-Abhijeet Dasgupta, Anthony Disserand, Tibault Reveyrand, Pierre Medrel, Philippe Bouysse and Jean-Michel Nébus, **Conception d'un modulateur de puissance large-bande á deux étages en technologie GaN**, in 20eme Journées Nationales Microondes (JNM-2017), Saint-Malo.

-Abhijeet Dasgupta, Arnaud Delias, Pierre Medrel, Philippe Bouysse and Jean-Michel Nébus, **A New Design Approach of High Efficiency S-band 25 W Mixerless Power Modulator based on High Voltage 50V GaN-HEMT Technology**, in IEEE-MTT Asia Pacific Microwave Conference (APMC-2016).

-Abhijeet Dasgupta, Philippe Bouysse, Jean-Michel Nébus and Raymond Quéré, **Design of an Efficient and Wideband Two-stage GaN-HEMT Power Modulator**, in European Space Agency ESA-ECSAT 8th Wideband Gap Semiconductor Workshop-2016, Harwell, UK.

Résumé

Conception d'un Modulateur Vectoriel de Puissance à Haut Rendement, bande S, en technologie GaN.

L'évolution des systémes de télécommunications, liée à une demande sans cesse croissante en termes de débit et de volume de données, se concrétise par le développement de systémes proposant des bandes passantes trés larges, des modulations à trés hautes efficacités spectrales, de la flexibilité en puissance et en fréquence d'émission. Par ailleurs, la mise en oeuvre de ces dispositifs doit se faire avec un souci permanent d'économie d'énergie d'où la problématique récurrente de l'amplification de puissance RF qui consiste à allier au mieux rendement, linéarité et bande passante. L'architecture conventionnelle d'une chaine d'émission RF consiste dans une premiére étape à réaliser l'opération de modulation-conversion de fréquence (Modulateur IQ) puis dans une deuxiéme étape l'opération de conversion d'énergie DC-RF (Amplificateur de Puissance), ces deux étapes étant traditionnellement traitées de maniére indépendante. L'objectif de ces travaux de thése est de proposer une approche alternative qui consiste à combiner ces deux opérations dans une seule et même fonction : le modulateur vectoriel de puissance à haute efficacité énergétique. Le coeur du dispositif, conçu en technologie GaN, repose sur un circuit à deux étages de transistors HEMT permettant d'obtenir un gain en puissance variable en régime de saturation. Il est associé à un modulateur de polarisation multi-niveaux spécifique également en technologie GaN. Le dispositif réalisé a permis de générer directement, à une fréquence de 2.5 GHz, une modulation vectorielle 16QAM (100Msymb/s) de puissance moyenne 13 W, de puissance crête 25W avec un rendement global de 40 % et une linéarité mesurée par un EVM à 5% .

Mots clés : PAPR, Gain Variable Saturé, Vector Power Modulator, Polarisation Dynamique, GaN-HEMT.

Abstract

High Efficiency S-Band Vector Power Modulator Design using GaN Technology.

The evolution of telecommunications systems, linked to a constantly increasing demand in terms of data rate and volume, leads to the development of systems offering very wide bandwidths, modulations with very high spectral efficiencies, increased power and frequency flexibilities in transmitters. Moreover, the implementation of such systems must be done with a permanent concern for energy saving, hence the recurring goal of the RF power amplification which is to combine the best efficiency, linearity and bandwidth. Conventional architectures of RF emitter front-ends consist in a first step in performing the frequency modulation-conversion operation (IQ Modulator) and then in a second step the DC-RF energy conversion operation (Power Amplifier), these two steps being usually managed independently. The aim of this thesis is to propose an alternative approach that consists in combining these two operations in only one function: a high efficiency vector power modulator. The core of the proposed system is based on a two-stage GaN HEMT circuit to obtain a variable power gain operating at saturation. It is associated with a specific multi-level bias modulator also design using GaN technology. The fabricated device generates, at a frequency of 2.5 GHz, a 16QAM modulation (100Msymb/s) with 13W average power, 25W peak power, with an overall efficiency of 40% and 5% EVM.

Key words: Power Amplification, IQ Modulation, Power Modulator, Envelope Tracking, EER, Saturated Variable Gain, GaN HEMT.