Iontronics - Field effect study of different devices, using techniques of ionic liquid gating

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For Püntl

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Contents

Acronyms and Abbreviations

1D	One-dimensional
2D	Two-dimensional
2DEG	Two-dimensional electron gas
AFM	Atomic force microscope
Au	Gold
B_{g}	Backgate
BCl_3	Boron cloride
c	Velocity of light
C_{d}	Capacitance of channel
C_{g}	Capacitance of gate dielectric
C_{IL}	Capacitance of ionic liquid
C	Carbon
CCD	Charge coupled device
CNT	Carbon nanotube
CMOS	Complementary metal oxide semi-conductor
d	Layer thickness
DC	Direct current
DS-FED	Drain-source field effect diode
e	Electron charge
E	Particle energy
E_{DS}	Electric field between drain and source
E_0	Activation energy
E_{C}	Conduction band edge
E_{F}	Fermi energy
E_{g}	Bandgap

$E_{\mathrm{g}}^{\mathrm{d}}$	Direct gap
$E_{\mathrm{g}}^{\mathrm{i}}$	Indirect gap
EDL	Electric double layer
FED	Field effect diode
FET	Field effect transistor
G	Conductance
$G_{\square}$	Sheet conductance
G_{D}	Top gate on side of the drain
G_{S}	Top gate on side of the source
h	Planck constant
I_0	saturation current for relaxation at $t = \infty$
I_{DS}	Drain-source current
$I_{\mathrm{DS,leak}}$	Leakage current passing through ionic liquid between source and drain
I_{g}	Gate leakage current
I_{off}	Off-state current
I_{on}	On-state current
$I_{\mathrm{DS,sat}}^{\mathrm{el}}$	Saturation current at electron side
IEF	Institut d'Electronique Fondamentale
INT	Inorganic nanotube
k_{B}	Boltzmann constant
$\mathbf{k}$	Momentum
k_{F}	Fermi wave vector
l	Electronic mean free path
L	Channel length
L_{INT}	Length of an inorganic nanotube
LED	Light emitting diode
LET	Light emitting transistor
MH-FED	Complex field effect diode
MIT	Insulator-to-metal transition
MoS_2	Molybdenum disulphide
MOSFET	Metal oxide semi-conductor field effect transistor

MWNT	Multi-walled nanotube
n_{2D}	Sheet carrier density
n	Charge carrier density
n_B	Boron concentration
n_h	P-type charge carrier density
n_c^{MIT}	Critical concentration for insulator-to-metal transition
n_c^S	Critical concentration for superconducting transition
Pd	Palladium
Pt	Platinum
R_{sat}^{2t}	2-terminal saturation resistance
$R_{\square,sat}^{2t}$	2-terminal saturation sheet resistance
$R_\square$	Sheet resistance
$R_{\square,sat}$	Sheet resistance at saturation
$R_{\square,INT,sat}$	Intrinsic sheet resistance of inorganic nanotube at saturation
R_c	Contact resistance
R_{sat}^{el}	Saturation resistance for high electron doping
R_{sat}^{h}	Saturation resistance for high hole doping
R_H	Hall resistance
r_{INT}	Radius of an inorganic nanotube
$R_{INT,sat}$	Intrinsic resistance of inorganic nanotube at saturation
R_{xx}	Longitudinal resistance
R_{xy}	Transversal resistance
$S_{s\text{-}th}$	Subthreshold swing
$S_{s\text{-}th}^{el}$	Subthreshold swing for electron doping
$S_{s\text{-}th}^{h}$	Subthreshold swing for hole doping
S-FED	Modified field effect diode
Si	Silicon
SiO_2	Silicon dioxide
SOI	Silicon-on-insulator
$SrTiO_3$	Strontium titanium oxide
T	Temperature

T_0	Activation temperature
T_c	Superconducting critical temperature
T_{c0}	Superconducting critical temperature of undoped material
TFET	Tunnelling field effect transistor
Ti	Titanium
TMDC	Transition metal dichalcogenide
UV	Ultraviolet
V_{bias}	Bias voltage
V_{DS}	Drain-source voltage
V_g	Gate voltage
V_{GAP}	gate voltage interval corresponding to the transistor off-state
V_{on}	On-state voltage
V_{th}	Threshold voltage
V_{DS}^{th}	Drain-source threshold voltage
V_{xx}	Longitudinal voltage
V_{xy}	Transversal voltage
W	Channel width
WS_2	Tungsten disulphide
Δ_σ	Quantum correction to conductance
ε_0	Vacuum permittivity
ε_r	Dielectric constant
κ	Dielectric constant
μ	Carrier mobility
μ_e	Electron mobility
μ_{FE}	Field effect mobility
μ_h	Hole mobility
μ_H	Hall mobility
ν	Frequency
ν_d	Carrier or drift velocity
ρ	Resistivity
σ	Conductivity

σ_0	residual conductance
τ	electron phase-relaxation time
Φ	Electrostatic potential
$\Phi_{\mathrm{B,p}}$	Schottky barriers heights for p-type charge carrier injection
$\Phi_{\mathrm{B,n}}$	Schottky barriers heights for n-type charge carrier injection
ψ	surface potential with respect to the bulk (band bending, positive when bending down)

Introduction

An ionic liquid is a tool for ultra-high electrostatic charge carrier doping. It is a transparent and oily fluid, consisting of cations and anions of an average diameter of $\approx 2\,\mathrm{nm}$, which is ionically conducting and electrically insulating. If a droplet of ionic liquid is placed between a conducting material and a counter electrode, a strong electric field can be established on the ionic liquid/conductor interface by applying a voltage to the electrode. This applied voltage will force a reorganisation of the liquid ions, because one type will be attracted by the charges in the counter electrode and the other type will accumulate on the conductor's surface. Such a device geometry is illustrated in Fig. 1(a), with a positive voltage applied to the counter electrode, which leads to a cation layer on the surface of the conducting material. The distance between the positive charges in the cation layer and the conductor is determined by the size of the ions and is therefore of the order of 1 nm. Consequently, an extremely high electric field is built up on the electrolyte/conductor interface, which can exceed $10\,\mathrm{MV\,cm^{-1}}$. This field is counterbalanced by an accumulation of charge carriers with opposite polarity (electrons in the displayed case) on the conductor's surface, where the two layers of opposite charges are called "electric double layer" (EDL).

This device can be seen as a planar capacitor with the capacitance given as $C = \varepsilon_\mathrm{r} A/d$, with ε_r being the dielectric constant, A being the surface covered by ionic liquid and d

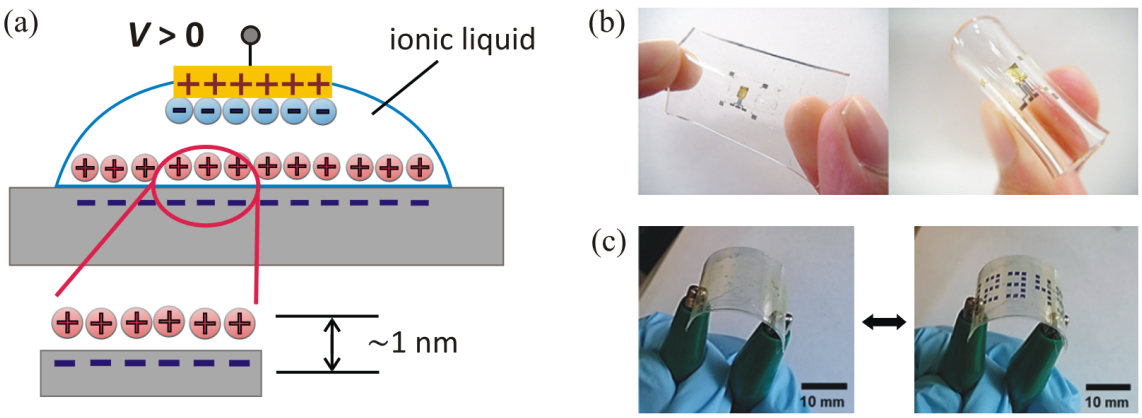

Figure 1: (a) Schematic drawing of an ionic liquid under in its function as capacitor plate. A droplet of electrolyte is placed between a conductor and an electrode on which a positive voltage is applied. The ions are rearranged, due to the applied field, and an electric double layer is formed on the ionic liquid/conductor interface. (b) Illustration of a flexible MoS_2 thin-film transistor, using an elastic ion gel gate. Taken from [167]. (c) Photo of a flexible and transparent display, taken from [141].

being the thickness of the electric double layer. As d is with $\approx 1\,\mathrm{nm}$ extremely small, ultra-high capacitances result, which can be increased even more by modulating the surface of the conducting material.

The specific capacitance of several ionic liquids was measured on organic semiconductors by Ono *et al.* [154], who observed capacitances in the range of 3-170 $\mu\mathrm{F\,cm^{-2}}$ at low frequencies. For a standard solid dielectric, the specific capacitance can easily be calculated via $C = \varepsilon_\mathrm{r}\varepsilon_0/d$, with ϵ_0 being the vacuum permittivity. Considering a 100 nm thick layer of SiO_2 as dielectric, the resulting capacitance is $0.035\,\mu\mathrm{F\,cm^{-2}}$, which is by two orders of magnitude inferior to the lowest value obtained for ionic liquids on organic semiconductors and by almost four orders of magnitude inferior to the highest value. This outstanding property of an ionic liquid was widely made use of in so-called EDL transistors, which are field-effect transistors, where the solid gate dielectric is replaced by an ionic liquid. The high capacitance leads to ultra-high charge carrier accumulation on the surface of the transistor's channel. However, in the case of a high-quality FET, operation performance is limited by several factors, where one of great importance is the surface quality of the channel material. For instance, surface roughness, intercalated or adsorbed impurities, trapped states and dangling bonds lead to localised ions which can no longer contribute to the EDL and locally diminish the gate effect.

One of the most promising family of materials consists in transition metal dichalcogenides (TMDC) which are semiconducting crystals having a layered structure, similar to graphene and can therefore appear e.g. as stacked monolayers and as layers rolled up to nanotubes. One outstanding characteristic of TMDCs is their high crystal quality, that is an atomically flatness of exfoliated flakes and nanotubes with very few trapped states and dangling bonds. Additionally, these materials have remarkable mechanical and electronic properties. For instance, the in-plane strength can be up to 30 times larger than steel [18], they emit light in the visible range and they possess a strong spin-orbit coupling which leads to a spin-orbit splitting of valence and conduction band edges. Monolayer TMDCs have a particular band structure without inversion centre that leads to the access of a novel degree of freedom, the valley degree of freedom, that preludes a new field of physics called valleytronics. As EDL-gated transistors, they show excellent low-power, ambipolar operation.

TMDC nanotubes have quite similar mechanical properties as thin films, whereas their electronic properties are poorly known. Theoretical work predicts that the confined structure will lead to more distinct electrical and optical properties than it is the case for two-dimensional flakes [38, 187]. The first presented WS_2 nanotube FET with a standard solid backgate shows very poor general transistor performance, but reveals a mobility almost as high es highest reported values for WS_2 flakes [115]. Due to the liquid nature of the an electrolyte as dielectric, the channel material can be of any geometry, which can be covered by an ionic liquid. Therefore, nano-objects, including nanotubes, that are not entirely flat and therefore difficult to be doped electrostatically using a solid backgate may experience a great improvement of performance in an EDL-gated transistor. Very recently,

the first EDL-gating TMDC nanotube became superconducting [168], which underlines the strength of this technique.

This last property of ionic liquids mentioned is true as well for a network of semi-conducting nano-objects that can be electrostatically manipulated very efficiently with the technique of EDL-gating. Electrically connected, but movable nanostructures form the base of flexible and printable devices and since the successful gelation of ionic liquids, these devices gained in stretchability and ease of handling. Some of the arising potential applications are transparent displays, foldable screens, wearable communication devices, bio-integrated circuits and robotic sensory skin [203]. Two photos of a stretchable, transparent transistor, based on a MoS_2 thin film provided with an elastic ion gel gate are displayed in Fig. 1(b). Panel (c) shows a flexible, transparent, gel-based electrochromic device. These and many other examples indicate that one future path of ionic liquids and gels lies in printable and/or flexible electronics [41].

In our work, we present some underlying research on the path to "futuristic" electronics, which is the investigation of new materials and the study of both ionic liquids and ion gels as tools for novel physics and applications. This leads to quite a varied work and to an exploration in many directions, whereas our main focus is on the investigation of isolated multi-walled WS_2 nanotubes.

Interestingly, the fabrication of TMDC nanotubes has been known since 1992 [212], whereas the first investigation of electronic properties was published in 2013, by the same group that had succeeded in their fabrication 20 years earlier [115]. A second publication on transport properties of WS_2 nanotubes appeared at the beginning of 2017, more than three years after we had started to characterise them [168]. This lack of investigation is astonishing when the fact is regarded that carbon nanotubes are some of the most studied nanomaterials ever. We hope that this work will help to valorise the remarkable properties of WS_2 nanotubes and will earn them more attention in the future.

In **chapter 1**, we will introduce ionic liquids and their main fields of applications. After a short display of the history of room temperature ionic liquids, we will show the structure of some of the most common cations and anions and list their remarkable properties. We will introduce all common uses, including chemical and electro-analytical ones, and then focus on the use of ionic liquids as gate dielectrics. We will give a historical overview of electric double layers and will discuss the principle of the technique and the main achievements of iontronics. Finally, we will present the disadvantages of ionic liquid-gating together with suggestions for improvement.

Chapter 2 is a small review of transition metal dichalcogenides and their applications, with a first focus on their remarkable applicability in ionic liquid-gated devices, and a second focus on their allotrope: multi-walled nanotubes. Together with the main applications

of TMDCs, we will show their favourable positioning for digital electronic applications compared to many other semi-conducting materials. We will display improvements of FET device performance when using the technique of EDL-gating and show examples of revealed ambipolar operation and superconductivity. After introducing TMDC (especially WS_2) nanotubes, we will discuss their high potential for various applications, e.g. as novel matter for the continued minimisation of digital devices and in EDL-gated networks for flexible, stretchable and printable devices.

Chapter 3 displays several fabrication processes we developed or refined in order to obtain samples of high quality. For the two types of TMDCs investigated in the course of this work, we will show the established processes of the complete fabrication from nanotube powder or mother crystal to contacted FET device, based on an individual nanotube or a mechanically exfoliated multi-layer flake. We will also explain the process of realising ohmic contacts patterned in a Hall bar design on intrinsic diamonds with hydrogen-terminated surface. Finally, we will display two main issues we had to face during the cleanroom processes and the solutions we found.

In **chapter 4**, we will present an EDL-gated field-effect transistors based on individual multi-walled WS_2 nanotubes. We will start by presenting their ambipolar operation and FET characteristic properties, such as mobility, subthreshold swing, and current on-off ratio. We will discuss these properties and compare them to equivalent devices based on TMDC thin flakes. Then, we will demonstrate and discuss metallic conduction at low temperatures at high n-type doping levels. We will present a study of the two performance-limiting factors of EDL-gated transistors: sweep velocity and temperature in order to evaluate the conditions for the highest performance of the devices. We will evaluate some statistics in device performance, based on measured nanotubes of various diameters. To emphasise the strength of ionic liquids as gate dielectrics, we will compare two gate sweeps, one using the liquid topgate and the other one using the solid Si/SiO_2 (300 nm) backgate. At the end of the chapter, we will explain the difficulty we had in performing four-probe measurements which is a fabrication issue rather than a material one and we will give a suggestion of how to adapt the fabrication process in order to solve this problem.

In **chapter 5** we will use the ability of an electrolyte to electrostatically induce a pn-junction in the channel material, in order to create a light-emitting transistor. We will explain in detail how a pn-junction can be established purely electrostatically and give some examples from literature. We will present electroluminescence spectra and compare our results to electro- and photoluminescence measurements that were performed on TMDC thin films by using the same technique. Additionally, we observed an alterable photocurrent when shining laser light of different power densities on the device. Both electroluminescence and photocurrent show polarisation dependent intensities. Finally, we will pronounce some doubts concerning the mechanism that leads to light emission.

The extremely high capacitances of ionic liquids enable the doping of large-gap semiconductors and insulators in order to achieve a metallic or even superconducting state. In **chapter 6** we will demonstrate the field-effect via EDL-gating on the two large-gap semiconductors: diamond and silicon. We will show a field-induced insulator-to-metal transition in intrinsic diamond with hydrogen-terminated surface and high surface charge accumulation in pre-doped, metallic silicon.

In **chapter 7** we will introduce a solid tool for high charge carrier accumulation, an ion gel with the cations fixed on one surface of the gel film, while the anions are still able to move freely through the matter. This tool allows us to create a novel type of field-effect diode, which operates with only one voltage bias applied. We will describe on the basis of literature the fabrication and the functionality of an ion gel with both types of charge carriers free to move. After the display of the state of the art of common field-effect diodes, we will describe the low-power working principle of our novel device with cation-fixed ion gel. Finally, we will characterise this ion gel in terms of general gating performance and compare it to an example from literature.

CHAPTER 1

Ionic Liquids

"The beauty of ionic liquids is that virtually anything is possible." (Marr *et al.*, 2015)

This statement originates from the fact that ionic liquids are purely synthetic materials, which can be adapted to the user's requirement. It also emphasises that finally, chemists and physicists fully appreciate the potentials of ionic liquids. In this chapter, we will give an overview over the already existing and trendsetting abilities and utilities of ionic liquids with the focus on the branch of application important for this work: the use of an ionic liquid as gate dielectric. We will start with a short historical introduction of ionic liquids, followed by their description and their common uses. We will furthermore focus on the technique of electric double layer-gating, presenting the historically first calculations and fabricated devices, the technique itself and main achievements. Finally, we will display the disadvantages of ionic liquid-gating together with suggestions for improvement.

1.1 History, Structure and Utility

Ionic liquids are molten salts which consist of cations and anions bound together by electrostatic interactions. In the following, we will describe the rise of ionic liquids, their structure and their common uses.

1.1.1 The Rise of Ionic Liquids

The history of ionic liquids began in 1914 when Paul Walden reported the properties of water-free molten ammonium salts which are liquid at temperatures below 100 °C [224]. In contrast to inorganic salts which melt at 300 °C to 600 °C, these organic salts could be investigated by standard methods and apparatus employed at usual temperatures and they gave the reproducibility which had been lacking up to that point. Walden imposed the current definition of an ionic liquid to be a material composed of cations and anions, which melts at temperatures $\leq 100\,^{\circ}\mathrm{C}$[1]. Melting temperatures could be reduced by enlarging the

1 Even if the term "ionic liquid" had not existed yet at that time, the definition has remained until today.

size of the cations, until the first room temperature ionic liquid was mentioned in 1948 in the patent literature and later in the open literature [88, 89]. An ionic liquid that is fluid in ambient conditions was a very important discovery, but this first room temperature ionic liquid was chemically complicated and a real breakthrough in the field of ionic liquids came 25 years later, started by the Osteryoung group in 1975 [43]. It took another 17 years until the first air and water stable room temperature ionic liquid was found and with Wilkes and Zaworotko presenting their *"Air and water stable 1-ethyl-3-methylimidazolium based ionic liquids"* [231], the era of ionic liquids began for real. Since then, a wide range of ionic liquids has been developed with various types of anions and cations, amongst others, hydrophobic anions to reduce water absorption [27]. It soon became clear that over one million simple ionic liquids could be synthesised [163].

1.1.2 Structure and Properties of Ionic Liquids

In contrast to solid salts that pack neatly together to form a crystalline structure, the ions of an ionic liquid are poorly coordinating, which allows a certain freedom of movement and is responsible for the liquid character down to a temperature of $\approx 220\,\mathrm{K}$ [132]. A functionality can be introduced on both cations and anions and as they can be combined in various ways, 10^{18} different types of ionic liquids are theoretically possible [132]. The most widely used ionic liquids are those containing N-heterocyclic cations, for example imidazolium salts. Melting points, solubility and viscosity can be tuned either by varying the substituents at the nitrogen atoms of the cations or by varying the type of anions. Some of the most commonly used cations and anions are displayed in Fig. 1.1. The ions that build the electrolyte used in this work, EMIM-TFSI, are emphasised. A list of the compound names is given in appendix A.1.

The liquid body at low temperatures and the possibility of "tailoring" a functional ionic liquid are only two of many extraordinary properties of ionic liquids. For instance,

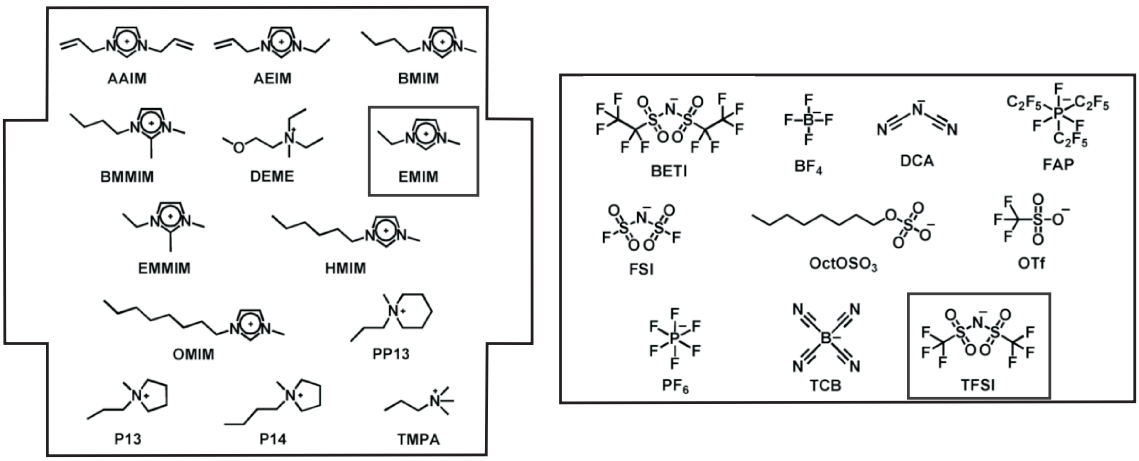

Figure 1.1: Some examples of common ionic liquid cations and anions, taken from [62]. The ions used in this work are emphasised. A list of the abbreviations and names is given in A.1.

negligible vapour pressure, wide liquid range, high thermal and electrochemical stability, wide electrochemical windows, non-flammability, high inherent conductivities, lack of reactivity, high recyclability and solubility of feed materials make room temperature ionic liquids very attractive for a wide range of applications [75, 136].

1.1.3 Fields of Application

In general, ionic liquids belong to the field of chemistry and come along with the two terms "Green Chemistry" and "Designer Solvents". The fields of application, however, exceed chemical applications by far. In the following, we will show the impact on green chemistry and the importance of designer solvents, but we will also give a display of the wide range of applications of ionic liquids.

Green and Sustainable Chemistry

One of the biggest challenges for synthetic chemists today is to minimize chemical pollution. The term "Green Chemistry" was used for the first time by Paul T. Anastas in 1991 with the purpose of designing *"chemicals and chemical processes that will be less harmful to human health and environment"* [9]. Amongst many, the leading research areas in the field of green chemistry are environmentally friendly solvents and catalysts [222]. Twelve guiding principles were defined and build the basis of the approaches to green chemistry, and one of these principles says: *"The use of auxiliary substances (e.g., solvents, separation agents, etc.) should be made unnecessary wherever possible and innocuous when used."* [9, 10]. Ionic liquids have an extremely promising non-volatile behaviour [158], are designed to be biodegradable and made from renewable resources and/or made to be durable and long lasting [132], which makes them one of the three solvents broadly accepted as environmentally friendly, besides water and supercritical carbon dioxide [85].

The possibility of easily adding functional groups to cations and anions in ionic liquids allows the fabrication of very specified solvents or catalysts for chemical reactions. For instance, they can be designed to separate azeotropic mixtures and to dissolve a wide range of natural materials, such as cellulose, carbohydrates and lignin. As many of the processes and reactions, where ionic liquids are used as solvents or catalysts, are compatible with the guideline of green chemistry mentioned above, ionic liquids are often called "green solvents"[1]. For instance, the dissolution processes of some natural materials normally require unusual solvents that cannot be recovered and reused after the process. While this causes serious environmental problems [82], ionic liquids can help to reduce the amount of solvents and catalysts and are reusable. One very important example: the dissolution of

1 This term is slightly misleading because ionic liquids are purely synthetic products and as long as some of them are toxic and not biodegradable, we cannot generally call them "green" [163].

cellulose[1].

Traditional cellulose extraction methods require a lot of energy, are expensive and cause environmental problems, whereas some hydrophilic ionic liquids[2] dissolve cellulose easily, and the cellulose can by regenerated by adding water, ethanol or acetone to the solution. The ionic liquid can be recovered and reused many times. [264]

The cellulose extraction is one of many examples, where tailored ionic liquids replace usual solvents in an environmentally friendlier way. More information about ionic liquids as designer solvents and catalysts can be found in the reviews [85, 163, 222]. Further on, ionic liquids in green chemistry can be used as support calls and enzymes, to kill microbes and as supercapacitors. They have functional pharmaceutical therapeutic abilities and facilitate the clean up and removal of environmental pollutants. A review of applications in green and sustainable chemistry is given in [132].

Electro-analytical Applications of Ionic Liquids

With all their remarkable properties, room temperature ionic liquids are perfectly suited for electro-analytical applications. Iontronic functionalities are applications in energy storage, as supercapacitors[3], in thermoelectrics, as printable electronics of solution-processable materials and nanostructures, as bioinspired and biocompatible electronic devices and sensors and as light-emitting electrochemical cells [20]. For instance, their use in photo-electrochemical solar cells, as electrolytes in rechargeable cells, in electro-deposition of metals and alloys and as new energy-harvesting devices, where energy is gained by utilising ionic-liquid movement has been discussed [158].

Another iontronic application is the use of ionic liquids as dielectrics for high surface charge carrier accumulation. The carrier injection works due to a very high electric field established in a so-called electric double layer (EDL). As our interest in ionic liquids lies exclusively in this fraction, we will discuss the rise of electrolyte-gating, the principle and its potential for applications in the following section. For a general review of electro-analytical applications see ref. [20, 56]

1 We just want to emphasise the importance of cellulose dissolution, which even made governments put pressure on researchers. Cellulose is the most abundant renewable resource in the world, can be extracted from a wide range of sources, including recycled paper and plants, and it has the ability to reduce society's dependence on non-renewable petroleum-based synthetic polymers [82, 206]. This clearly displays the environmental advantage of using cellulose as raw material. As one example, the Australian company Zeo developed a process to build a hardwood-like material known as Zeoform, using just cellulose and water, which is a promising, eco-friendly alternative to the use of plastics and resins [255]. Some more examples for cellulose composites are given in [174, 264].

2 The ionic liquid that can be used for cellulose dissolution are 1-butyl-3-methylimidazolium chloride (BMIMCl) and 1-allyl-3-methylimidazolium chloride (AMIMCl).

3 More information on supercapacitors can be found under [45] and http://www.spectrum.ieee.org/transportation/advanced-cars/the-charge-of-the-ultra-capacitors

An Explosion of Possibilities

Due to their remarkable properties, room temperature ionic liquids are suitable for many more aspects of application than those described above, e.g. in the fields of petrochemicals, pharmaceuticals, biotechnology, hydrometallurgy, biomass processing, sustainable energy, and nuclear science [132]. Ionic liquids can be used, recycled and reused several times, as catalysts with high catalytic activity and without many of the negative effects of conventional catalysts during reactions [222]. They produce high performing synthetic lubricants [263] and are used for many applications in analytical chemistry [158]. Even chromatographic applications, such as sensing and spectrometry are conceivable. Note that on average, ionic liquids are 5-20 times more expensive than molecular solvents, but the fact that they can be recycled and reused many times (>50) makes them significantly cheaper [163].

Research is going on and new potential applications arise constantly. For more details concerning properties and utilities of ionic liquids, see for example books and reviews [20, 75, 85, 136, 222].

1.2 Electric Double-Layer-Gating

Electric double layer-gating, short EDL-gating, first appeared as *"exciting interdisciplinarity"* [158], but has meanwhile gained a lot of interest, even if it remains a tiny fraction of the vast field of applications of ionic liquids. In the following, we will give the historical background of EDL-gating, explain the technique itself and give an overview of the main achievements reached by using this technique. At the end of this section, we will display the limiting factors of ionic liquid-gating together with suggestions for improvement.

1.2.1 The History of EDL-Gating

The first to suggest a model for an EDL was Helmholtz in 1853 [83]. He mathematically described the concept of a simple, plane and nanometric dielectric capacitor: a conductor A is electrically charged and brought in contact with a second, uncharged solid or ionic liquid conductor B, under the condition that no charge transfer can happen between A and B. Then, charges or ions of polarity opposite to the charges in A will accumulate on the surface of B, touching A. Helmholtz called the two layers of opposite polarity on the interface *"Doppelschicht"*, which can be translated as electric double layer. The definition in the original paper is displayed in Fig. 1.2(a). Due to his theory, the ion layer formed on the surface of B, was given the name "Helmholtz layer" [62]. In it, the surface charge is completely screened and the potential drop does not extend further in the material.

The first to actually fabricate an EDL transistor one century later was John Bardeen, the only person to have been awarded the Nobel Prize in Physics twice. His concept, presented in his Nobel lecture 1956 [15], is shown in Fig.1.2(b). The following ion-sensitive

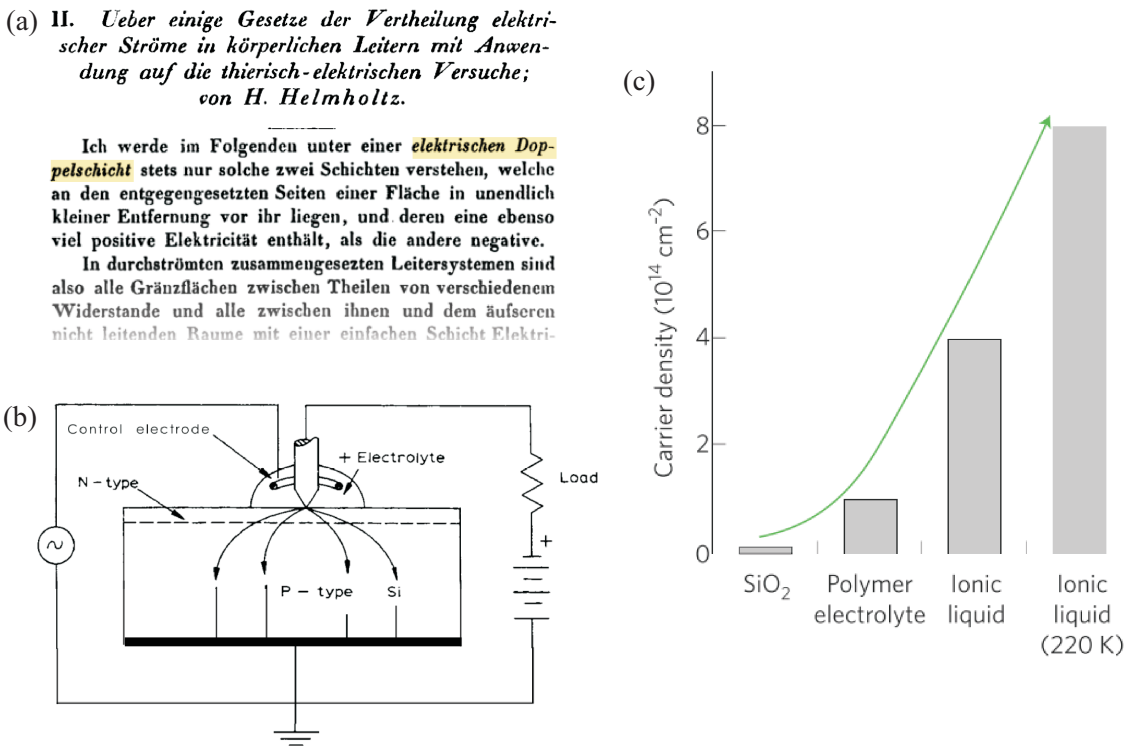

Figure 1.2: (a) Extract of the original paper of Helmholtz with the first definition of an electric double layer [83]. (b) Diagram of the first published electrolyte field-effect transistor, realised by Bardeen [15]. (c) Evolution of electrostatically achieved charge carrier densities. The carrier density increases dramatically when solid gate dielectrics are replaced by liquid ones, taken from [166].

solid-state device was reported in 1970 [17], where the electrolyte is composed of Na+ ions in a solution. After a pause of 30 years, two groups realised EDL transistors, using salty water as electrolyte on carbon nanotubes (CNT), where the salt in solution was $LiClO_4$ [104] and NaCl [177] respectively. Both groups observed a channel/gate coupling enhanced by one order of magnitude and ambipolar transport. A short time later, at the beginning of 2004, the first EDL transistor provided with a room temperature ionic liquid was realised [101], with CNTs and fullerene peapods as channel materials. It was soon followed by two simultaneously published reports of electrolyte-gated CNTs [122, 200]. From this time on, the research on ionic liquid-gated field-effect transistors started to grow and is still expanding today with many different applications in sight.

1.2.2 The Concept of Ionic Liquid-Gated Field-Effect Transistors

An EDL transistor is a field-effect transistor, where the solid gate dielectric is replaced by an ionic liquid. A very important property in this context is the fact that the electrolyte is ionically conducting, but electrically insulating. As an ionic liquid is solvent-free, very stable, has a low vapour pressure (even compatible with ultra-high vacuum) and has high capacitances up to 170 µF cm^{-2} [154], it is well suited for the use as gate dielectric and largely outperforms standard solid dielectrics. The development of possible surface charge

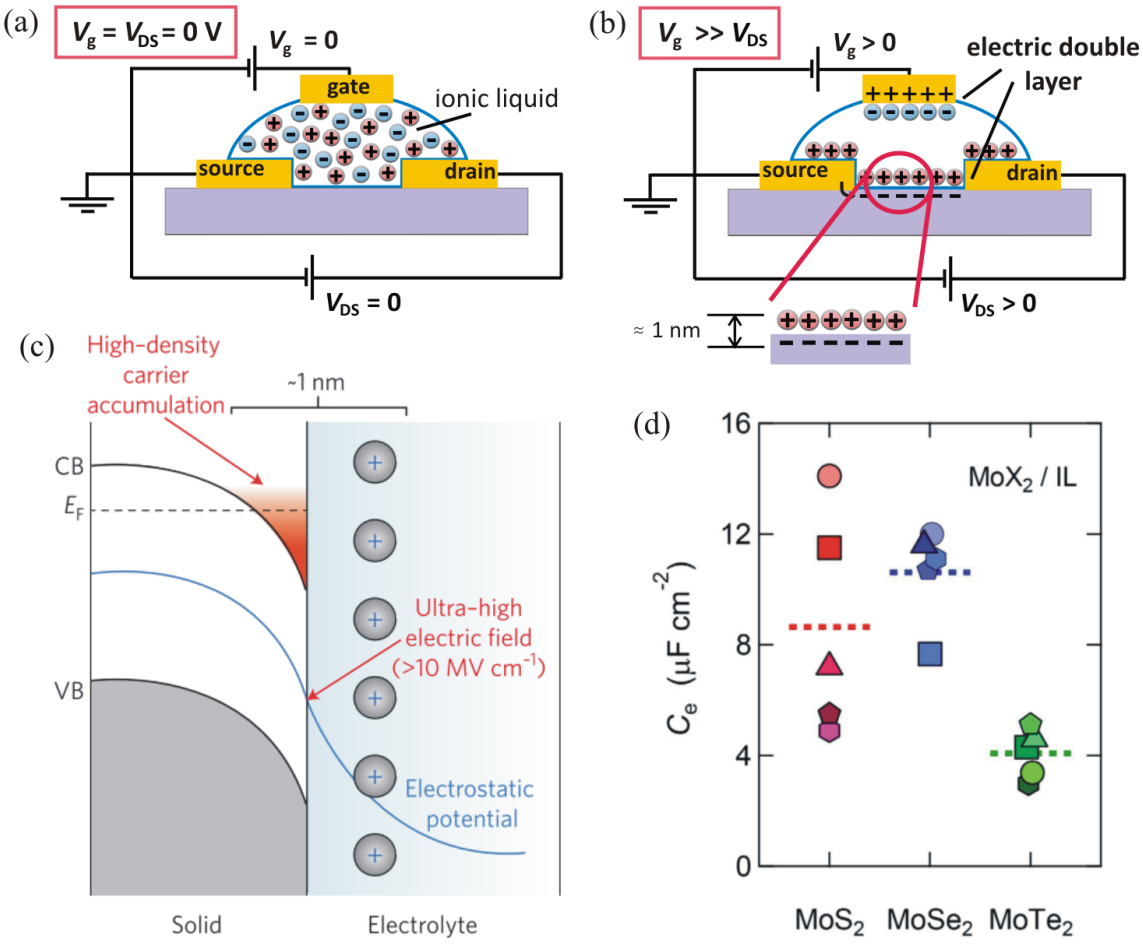

Figure 1.3: (a), (b) Schematic drawing of an EDL-gated substrate without any voltage applied and with positive drain-source and gate voltage $V_g \gg V_{DS}$ applied respectively. The gate bias leads to the formation of two electric double layers. (c) Illustration of the EDL on the ionic liquid/semiconductor interface. The electric bands of the semiconductor with strong bending on the interface and the zone of high carrier accumulation are indicated, taken from [166]. (d) Capacitances for electron accumulation of the ionic liquid DEME-TFSI when used as dielectric on three different types of TMDC thin films. Different symbols represent different devices and the horizontal short dashed lines correspond to the average values, taken from [194].

carrier accumulation connected with the discovery of new gate dielectrics is shown in Fig. 1.2(c). For instance, 2D charge carrier densities up to $10^{15}\,\mathrm{cm}^{-2}$ can be reached nowadays, which exceed those of SiO_2 by two orders of magnitude and those achieved by the high-κ-dielectric HfO_2 by at least one order of magnitude. Such high values allow the investigation of exotic electronic phases and therefore rich physics, but had only been accessible via chemical doping until room temperature ionic liquids were discovered [3].

This remarkably high charge carrier injection is possible due to very strong electric fields created in the electric double layer on the sample's surface. The principle of ionic liquid-gating is illustrated in Fig. 1.3(a) and (b), where schematic drawings of an electrolyte-gated substrate are displayed. When neither a gate voltage V_g nor a drain-source voltage V_{DS} are applied, the ions in the electrolyte are mixed in order to keep charge neutrality (see (a)).

When a small drain-source voltage (in general $\gg$1 V) and a positive gate voltage $V_g \gg V_{DS}$ are applied, the ions will rearrange themselves due to the strong gate-field: the positive charges in the gate electrode attract cations which accumulate around it, whereas anions are repulsed. The latter will accumulate on the surfaces the furthest away from the cloud of cations, which are the metal electrodes and the channel. The charge layer on the channel surface creates a very high electric field of more than 10 MV cm^{-1} which is compensated by the injection of charges of opposite polarity into the channel region, as shown in Fig. 1.3(b). In this ion configuration, two electric double layers are established, one on the interface between gate electrode and electrolyte and the other one at the interface between electrolyte and channel (see zoom in Fig. 1.3(b)).

The electric double layer on the channel/electrolyte interface is illustrated in Fig. 1.3(c). Due to the strength of the electric field in the EDL, charge accumulation takes place only on the channel's surface. The strong band bending of the semiconducting channel material and the high charge carrier accumulation on the surface are indicated in the illustration which is taken from [166]. Note that we only explained the case of a positive gate voltage applied and therefore the creation of a two-dimensional electron gas in the channel, as the other case of a negative V_g applied is exactly inverse and results in a 2D p-type channel.

Due to the nanometric thickness of the EDL on the semiconductor/electrolyte interface, the capacitance of an ionic liquid depends on the channel material, more precisely on the surface of the material. The group of Iwasa measured capacitances of 15 different TMDC devices built with three different molybdenum containing thin flakes and provided with the same ionic liquid, DEME-TFSI. The result of their study is displayed in Fig. 1.3(d), where the capacitances of all 15 devices and their mean values for each material are shown. Even for the same material, the capacitance values of the electrolyte are broadly spread, which might be due to the existence of different surface states in the individual thin flakes, created during the fabrication process. However, the average values of capacitances of the three crystals clearly differ. The minimum value was observed for $MoTe_2$ with 4.1 µF cm^{-2}, the average values for MoS_2 and $MoSe_2$ are 8.6 µF cm^{-2} and 10.6 µF cm^{-2} respectively.

In a transistor with a liquid as topgate dielectric, the gate voltage can be applied by either a metallic wire dipped in the liquid droplet or by a counter electrode placed beside the device. The size of this counter pad is a very important parameter for good gating performance. It was demonstrated that an electric field on top of the channel surface is only created, if the surface area of the counter electrode is by 1-2 orders of magnitude bigger than the total size of all remaining metal surfaces covered by the ionic liquid [161]. Another desirable condition for good gating performance is a very flat channel surface with a minimum of trapped states and dangling bonds because the latter would lead to localised ions on the channel's surface and therefore shielding effects, which would degrade the operation performance.

All the electronic properties and functions which are based on ionic motion and on controlled ion formations are called iontronic [259].

1.2.3 The Main Achievements of Iontronic

In contrast to chemical doping, the ability of EDL-gating to induce 2D charge carrier densities of up to $10^{15}\,\mathrm{cm}^{-2}$ opens the door to rich physics, that is new electric states, functions and properties in various materials without the creation of undesired disorder. In the following, we will give an overview of the main achievements of iontronic. We will start with a comparison of electric-field doping and chemical doping and continue with a display of all sorts of field-effect-induced properties, such as phase transitions, light emission and transistors of various materials based on examples from literature. Finally, we will display how ionic liquids decrease contact resistance and why this technique is very promising in terms of the down-scaling of devices.

Chemical Doping versus Electrostatic Doping

Before the era of EDL-gating, ultra-high charge carrier densities could only be reached by chemical doping. We will to display why high charge carrier injection by field-effect was such an important discovery. The first difference between the chemical intercalation of charge carriers and purely electrostatic doping is to be found in nature of doping. While chemical doping is a permanent change of the material with the inclusion of foreign atoms, electrostatic doping is completely reversible and can work for both polarities in the same sample. As the inclusion of foreign atoms is at the same time an inclusion of impurities, chemical doping enhances the disorder in the semiconductor, whereas field-effect doping is free from lattice distortion. Another difference is the dimensionality of the conduction channel. As illustrated in Fig. 1.3(c), the ultra-high electric field in the EDL induces charge carriers only on the semiconductor's surface, which leads to a two-dimensional conduction channel. Chemical doping generally goes deeper and in most cases, the conduction channel has a three-dimensional nature rather than a 2D one.

Chemical doping has limits, where only electrostatic doping can be successful. For instance, electric field carrier injection is possible on any material that can be fabricated as field-effect transistor, while chemical dopants have to match with the mother material. Consequently, field-effect doping is still possible in materials, where foreign atom intercalation is very difficult or impossible. For instance, it is not realistic to introduce dopants in ultra-thin 2D crystals, but carrier density can be controlled perfectly well via field-effect in crystal layers of a thickness down to single-atom size [259]. To give an example, it was EDL-gating which led to the discovery of a superconducting transition in potassium tantalite, which has such a poor chemical solubility that charge carrier densities achieved via chemical doping were not high enough to reach superconductivity [218]. In general, the critical charge carrier concentration for an insulator to become metallic is low and can be reached by chemical doping, the critical concentration for a superconducting transition, however, is very often much higher and can only be achieved by EDL-gating. More examples will be given in the following section.

As electrostatic doping can work for both p- and n-type charge carriers in the same channel material, ambipolar transistor operation is possible as well as simultaneous injection of charge carriers of opposite polarities. The result is the creation of a pn-junction in the channel and with it possible radiative recombinations. In contrast to a chemically doped pn-junction, the creation of the latter via field-effect doping does not only lead to the control of the doping level, but also to the control of the recombination zone [21, 253]. Both, ambipolar transport and electric field-induced pn-junctions have been demonstrated on various materials, including ultra-thin layers. We created a pn-junction via field-effect and observed light emission. The results are presented and discussed in chapter 5.

Ionic Liquid as Tool for Disorder-Free High Carrier Doping

Organic crystals were one of the first class of materials to be EDL-gated with immediate success. The first polymer electrolyte-gated organic field-effect transistor was realised by Panzer *et al.* in 2005 [160]. They presented the low-voltage p-type operation of a pentacene FET with a threshold voltage of $-1\,\mathrm{V}$, current on/off ratios of 10^4 and a subthreshold swing of $180\,\mathrm{mV/decade}$. Other EDL-gated organic FETs with enhanced operation performance compared to a Si/SiO_2 backgated transistor followed soon [159, 197, 198]. When a polymer electrolyte was used as a gate dielectric, a remaining limit was observed to be the switching speed, as it depends on the response time of the ions in the polymer matrix to an applied gate bias. Suggestions made for an for improvement of the switching speed included the decrease of the channel length and the polymer electrolyte film thickness as well as the increase of the ionic conductivity by modulating the electrolyte [160]. In 2008, a high-mobility, low-power, and fast-switching organic field-effect transistor was realised by Ono *et al.* [155], using a room temperature ionic liquid as gate dielectric. At the same time, first applications of EDL-gated organic semiconductors in flexible electronics were discussed [159].

Only a short time after the first ionic liquid-gated field-effect transistors had been realised, the ability of the strong surface gating to induce new electric states in various materials was discovered. For instance, insulator-to-metal transitions were demonstrated in ZnO [90], in $NdNiO_3$ [183] and in the conjugated polymer semiconductor pBTTT-C14 under a combined control of gate voltage and high pressure [193]. Ambipolar insulator-to-metal transitions were discovered in Black Phosphorus [179] and in various transition metal dichalcogenides (TMDC), such as MoS_2 [171] and TaS_2 [248]. The first superconducting transition in an insulator was realised by Ueno *et al.* in 2008. $SrTiO_3$ became superconducting at a field-induced charge carrier density of $\approx 5 \times 10^{13}\,\mathrm{cm^{-2}}$ with a critical temperature $T_c = 0.4\,\mathrm{K}$ [217]. In 2011, the same group observed superconductivity in $KTaO_3$ with a T_c of $50\,\mathrm{mK}$ [218] and Ye *et al.* discovered superconductivity with a high critical temperature of $15.2\,\mathrm{K}$ in ZrNCl [244].

The modulation of the critical temperature in high-T_c superconductors with the change of charge carrier density was reported for two ultra-thin cuprate films. In $YBa_2Cu_3O_{7-x}$,

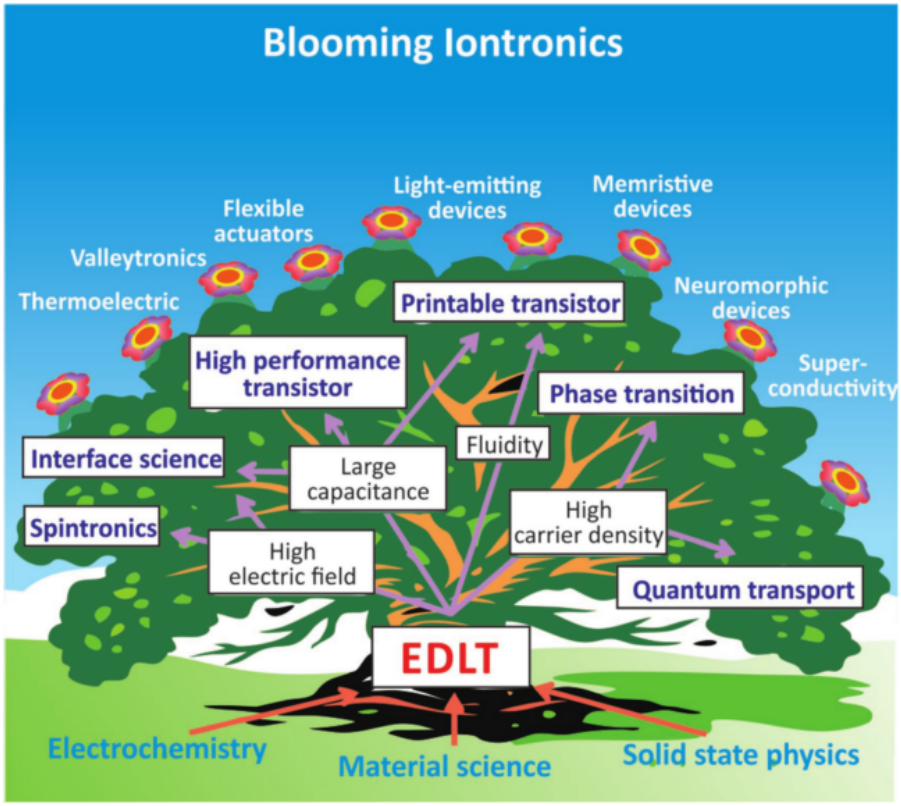

Figure 1.4: Multidisciplinary fields of research and applications of ion-controlled electronics, taken from [20].

the critical temperature could be enhanced by up to 38 K and the highest onset of a superconducting transition observed was reported to be at 134 K [51]. In $La_{2-x}Sr_xCuO_4$, a T_c-shift of up to 30 K with a maximum of 40 K was reached [26]. Besides increasing the critical temperature, it is also possible to kill superconductivity by field-effect charge carrier modulation (e.g. in $YBa_2Cu_3O_{7-x}$ [114]) or to modulate superconducting properties. Disordered indium-oxide films near the superconductor-insulator transition could be driven from insulating to superconducting and the magnetoresitance peak was tuned by EDL-gating [112]. Even light-induced superconductivity was reported where an electric double layer was photo-induced in a photochromic spiropyran monolayer [204].

In terms of EDL-gating, an important family of materials are TMDCs and many of them undergo a superconducting transition at high field-induced doping levels. The properties of these materials in general and combined with EDL-gating will be discussed in the following chapter. More information about EDL-gate-induced superconductivity in two-dimensional atomic crystals and other materials is given in [166, 180, 219]. A third phase transition can be induced by field-effect doping, which is a ferromagnetic transition, and it was observed in cobalt and cobalt-doped titanium dioxide [195, 238].

Besides the electric state, there are other parameters that can be modulated by high charge carrier doping. For instance, the conductance modulation of gold thin films and a change

of the channel thickness by doping was reported [47], an anomalous Hall effect was found in platinum films [196] and even a collective bulk carrier delocalisation with resulting 3D conduction by electrostatic surface charge accumulation was discovered in the strongly correlated material VO_2 [145].

Ambipolar transport has been demonstrated in organic semiconductors, CNTs and TMDCs (see next chapter) and electric field-induced pn-junctions, which may eventually lead to radiating recombinations, have been demonstrated in these materials [21, 139, 253]. Many fields of research and applications of iontronic are displayed in Fig. 1.4.

A general overview of the current status of the theory and application of EDLs in room temperature ionic liquids is given in [20, 56].

Reduced Contact Resistance Due to Ionic Liquids

It was shown by Lee *et al.* that the mobility in TMDC field-effect transistors might be largely underestimated due to the influence of high contact resistances created by large Schottky barriers on the metal/channel interfaces [110]. In the case of EDL-gating, this problem becomes less important, as mobile ions on the metal/semiconductor interface thin the barriers at the contacts. This was already observed in 1998 by the group of Friend, who showed that a density of ionic charges above a metal/semiconductor interface which exceeds $10^{20}\,\mathrm{cm}^{-3}$ thins the barrier widths to only a few Å. In general, this results in ohmic behaviour and the choice of the contact metal does no longer importantly affect the device performance [50]. Later on, many groups observed a significant increase of the tunnelling efficiency with electrolyte dielectrics due to drastically reduced Schottky barriers. The originating effect is a strong band bending in the semiconductor provided by the nanometer-thick EDL with a high capacitance [161]. The effect is illustrated in Fig. 1.5. In panel (a), a schematic drawing of a device and of the electric bands on the metal/semiconductor interface are displayed in the equilibrium case. Panel (b) shows the case of a negative gate voltage applied. The FET in the drawings is the case with Schottky barriers width for p-type carrier injection. The negative gate bias causes a strong band bending which results in a decrease of the Schottky barrier until charge carrier injection via tunnelling is easily possible, indicated as red arrows.

As expected, the thinned injection barriers and therefore the reduced contact resistances lead to improved transistor operation. For instance, Wang *et al.* fabricated suspended MoS_2 field-effect transistors and discovered an increase of the conductance by 3-4 orders of magnitude just by comparing values before the provision with electrolyte and with an ionic liquid droplet on the device. The room temperature mobilities increased from 0.01 to $10\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ without liquid to $46\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ after provision of electrolyte [91]. This emphasises the efficiency of EDL-gating and the ability to improve intrinsic channel-limited device properties. More examples are given in ref. [30, 120, 161, 197].

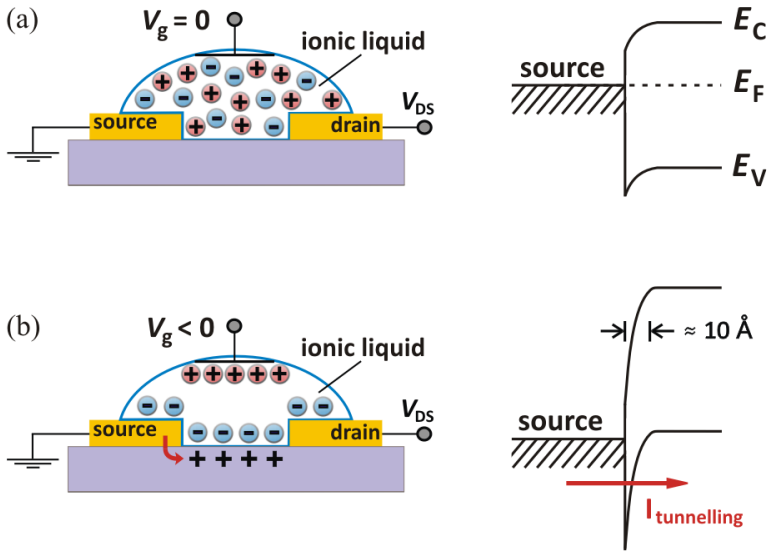

Figure 1.5: Schematic drawings of an EDL-gated FET and the electric bands on the metal/semiconductor interface to illustrate the thinning effect of Schottky barriers when an ionic liquid is used as gate dielectric, drawn after [49, 50]. (a) Case of a EDL-gated transistor with Schottky barriers for hole injection in equilibrium. (b) The same transistor with a negative gate bias. A strong band bending results in Schottky barriers of about 10 Å width and charge injection via tunnelling (red arrow) is possible.

1.2.4 Restrictions of EDL-Gating and Solution Strategies

After having shown the various achievements and promising abilities of EDL-gating, we cannot deny that this technique has its limits. Its most obvious disadvantage is the liquid body, which, on the one hand, reduces stability and reproducibility and, on the other hand, disables gate controllability at temperatures below the freezing point of the ionic liquid. A second limiting factor is the low operation speed, when compared with solid-state field-effect devices, as the gating process is limited by the motion velocity of the ions. A third disadvantage is charge disorder induced on the surface by the ionic liquid or by electrochemical reactions, which is responsible for the appearance of an upper limit of mobility [64, 162]. The last, but rather important limiting factor consists of gate leakage currents, which generally degrade device performance. It was shown that the resistance of an ionic liquid is in general lower than that of a solid dielectric, which results in a tendency to higher leakage currents [197].

Most of these limits have already been investigated and solutions have been found. The gelation of the electrolyte brought an improvement in stability and some possibilities of device integration (For more information about ion gel gating see chapter 7). Operation speed was improved by enhancing the ion conductivity and therefore the motion speed of ions [233] and surface disorder could be decreased by adding a thin boron nitrate flake as spacer between the channel and the electrolyte [64, 162].

Finally, we investigated the origin of gate leakage currents and their temperature dependence and we discovered a way to drastically reduce these parasitic currents only by freezing the

ionic liquid. Our achievements will be discussed in the following.

Temperature Dependence of Electrochemical Reactions

One origin of gate leakage currents I_g is to be seen in electrochemical reactions that may occur between the ionic liquid and the channel material as well as between the ionic liquid and the contact metals. The term of "chemical window" is commonly used when speaking of electrolytes and it is the interval of applied voltages, which does not lead to electrochemical reactions. The chemical window is an intrinsic property of the electrolyte and temperature independent, whereas the intensity of electrochemical reactions depends on the materials in contact with the ionic liquid and on temperature.

In order to evaluate the influence of temperature in the gate leakage current, we measured I_g as a function of gate voltage V_g at different temperatures, starting from 200 K, a temperature below the melting point ($\sim$ 220 K) of the ionic liquid, and going in steps of 10 K up to room temperature. The ionic liquid output characteristics in forward sweep direction are displayed in Fig. 1.6, where we can clearly see that there is no current flow through the electrolyte at the two lowest temperatures, when the ionic liquid is frozen. The gate leakage currents increase with increasing temperature and the gate voltage interval in which leakage currents are negligibly small in getting narrower. For instance at $V_g = \pm 4$ V, which is the gate bias we needed to apply in order to reach the charge carrier concentrations revealing rich physics, the gate leakage currents stay below 1 nA only at temperatures $T \leq 260$ K.

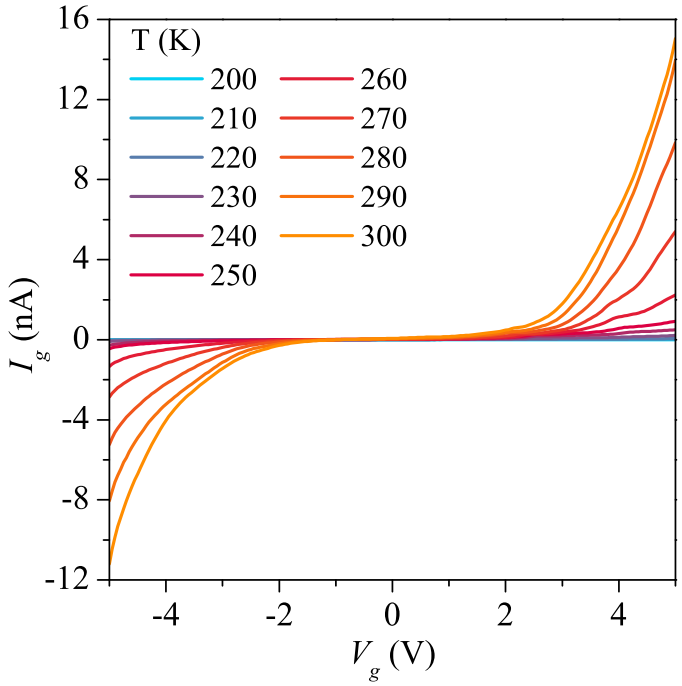

Figure 1.6: Current-voltage characteristics of the electrolyte-gate at different temperatures. Gate leakage currents generally increase with increasing temperature.

This small study shows that the temperature at which measurements are performed plays an important role when an ionic liquid is used as electrolyte and that temperatures just above its melting point are preferable. A study of how the gate leakage current influences the operation performance of a FET is shown in chapter 4, section 4.2.3.

Reduction of Leakage Currents after Freezing the Electrolyte

In general, there are two factors that create leakage currents through an ionic liquid. One consists of electrochemical reactions, which we discussed above, and the other one of impurities trapped in the electrolyte. As ionic liquids absorb molecules like water, nitrogen and oxygen, outgassing of the ionic liquid is very important in order to limit leakage currents [30, 251]. Part of the impurities can be removed by pumping the environment of the device provided with electrolyte to high vacuum. We discovered that additional cryogenic pumping[1] is an important factor in order to remove molecules like water, nitrogen and oxygen and therefore decrease gate leakage currents.

Interestingly, the creation of motion inside the ionic liquid and especially forcing them to build up a crystalline structure causes outgassing effects. We observed that in a well performing device, leakage currents are of the order of 10^{-10} A and decrease with the number of gate sweeps performed at temperatures ≤ 250 K and in a gate voltage range $|V_g| \leq 4$ V. We ascribe this behaviour to outgassing, due to the permanent reorganisation of the liquid ions. Note that this effect was visible for devices with palladium or gold as sticking-layer, whereas in the case of titanium, electrochemical reactions were so strong

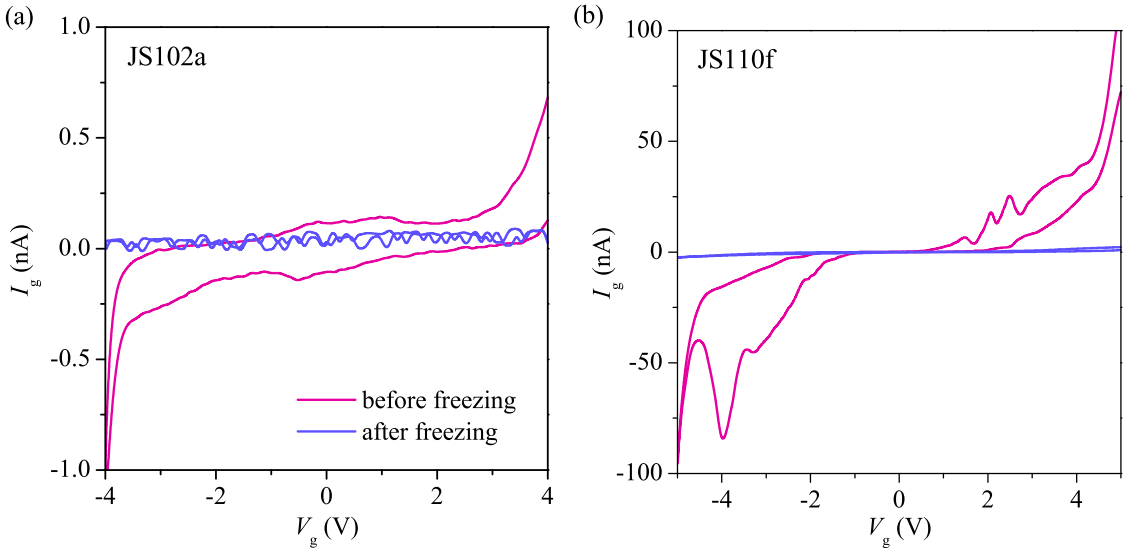

Figure 1.7: Comparison of the gate leakage current before and after freezing the ionic liquid gate dielectric in (a) device JS102a and (b) device JS110f.

1 Cryogenic pumping stands for the adsorption of molecules like water, nitrogen and oxygen at the dip-stick's cover, when the latter is dropped into liquid helium.

that I_g increased with the number of performed gate sweeps and reached values up to 10^{-8} A.

Our close collaborator Shimpei Ono (researcher in CRIEPI, Yokosuka, Japan), who has the possibility of performing measurements in a cryostat provided with a window, observed outgassing effects in the ionic liquid when cooling it through its freezing temperature. At temperatures just above the freezing point and therefore just before the arrangement in a crystal structure, small bubbles emerged in the liquid droplet. We discovered that this outgassing effect results in leakage currents reduced by orders of magnitude. In Fig. 1.7, two extreme cases are displayed: on the one hand, a device with extremely low initial leakage currents in (a), and on the other hand, a device with rather high initial leakage currents in (b). In each panel, I_g is shown as a function of V_g at $T = 250$ K before and after freezing the ionic liquid. In both cases, I_g decreases by two orders of magnitude, due to the freezing from 1×10^{-9} A to 1×10^{-11} A and from 4×10^{-8} A to 4×10^{-10} A at $V_g = 4$ V respectively.

We can conclude that cooling the sample below 200 K one time before performing measurements is not a necessary step, but may increase the operation performance of the devices on the sample.

1.3 Conclusion and Outlook

We have discussed the various fields of application of ionic liquids and we have found that in this respect, green chemistry certainly has the biggest impact on today's research. Nevertheless, simply the interdisciplinary use of ionic liquids for electro-analytical applications opens a wide range of research directions, where the ionic liquid is either the tool to investigate, as in our case of EDL-gating, or an active matter, as it is the case in supercapacitors and light-emitting cells.

We explained the technique of EDL-gating and its advantages and presented the most important fields of research and applications of iontronic. Amongst others, the fact that replacing chemical charge carrier injection by field-effect doping leads to new high-T_c superconductors or increased critical temperatures, due to fewer impurities, is a big achievement. It was shown that within this technique, Schottky barriers are thinned drastically and tunnelling efficiency increases so much that the choice of the contact metal is of minor importance.

Several times, the possibility of gelation of ionic liquids came up. This new field opens the door to printable, flexible and transparent electronic devices which can be fabricated on various materials, amongst others plastic and paper. Some printed low-voltage transistors and circuits have already been realised [72, 86, 188, 233]. Thus, the future of ionic liquids might lie in printable and/or flexible electronics and in nano-scale integrated systems [41].

CHAPTER 2

Transition Metal Dichalcogenides

Transition metal dichalcogenides (TMDCs) are layered materials with the formula MX_2, where M is a transition metal element from the groups IV, V or VI and X is a chalcogen (S, Se or Te). Each monolayer is formed by three atomic planes of X-M-X and exhibits a strong in-plane bonding, whereas the distinct layers are stacked together via weak Van de Waals bonds. TMDCs have been studies for decades (one of the first publications dates from 1967 [59]), but their importance as near-atomically thin materials is new. It was after the discovery of the technique of mechanical exfoliation in 2004 [150], that materials with strong in-plane bonding and weak out-of-plane interactions gained a lot of interest. Since that time, new opportunities of two-dimensional TMDCs in nanoelectronics and optoelectronics have opened up [228]. The existence of TMDC nanotubes had been known more than 10 years earlier than the technique of fabricating thin, planar layers was discovered. However, the consideration of tubular TMDCs in electrical devices only started in 2013 when Levi *et al.* presented the first WS_2 field-effect transistor [115].

This chapter will introduce the family of transition metal dichalcogenides and outline their remarkable properties which make TMDCs suited for nano- and optoelectronics. We will display the most important fields of research and application on the basis of literature. The suitability of TMDC thin films for EDL-gating will be demonstrated, showing the achievements attained up to now. In the course of this work, we investigated EDL-gated MoS_2 and WS_2 thin film FETs, in order to confirm the quality and authenticity of techniques of device fabrication and to extract the capacitances of our used ionic liquid. The results of these measurements are displayed and discussed in appendix A.2.

We will then focus on WS_2 nanotubes and their potentials in nanoelectronics. Their possible application in flexible, stretchable and printable devices when combined with ionic liquids or ion gels will be introduced. Furthermore, the potential of EDL-gated TMDC nanotubes as active matter in ever smaller devices, bypassing the problems of short-channel effects, will be discussed.

2.1 TMDC Thin Films

Graphene with its extremely high stability, purity, transparency and mobility is certainly the most-studied in the family of two-dimensional crystals and compounds. However, graphene has a drastic drawback in terms of electrical applications, which is the lack of a bandgap. Consequently, the discovery of layered compounds with similar stability and purity under the possession of a bandgap was a great achievement in the fields of nanoscience and nanoelectronics. The group of non-graphene 2D materials includes metal chalcogenides, oxides, hydroxides, oxychlorides and the graphene-like boron nitride. Most of them are either not air-stable or cannot be successfully isolated as high-quality thin films, and only few of them are semiconducting. In the following, we will show the potentials of transition metal dichalcogenides in this context. General properties and fields of applications will be displayed.

2.1.1 TMDCs: Well Suited for Nano- and Optoelectronics

A considerable number of transition metal dichalcogenides are very promising candidates for electrical applications, as they own all the qualities required for nanoelectronic and optoelectronic applications. For instance, molybdenum- and tungsten-based TMDCs are semiconducting, structurally and thermally stable, and their bandgaps range from visible to near-infrared. Additionally, MoS_2 and WS_2 have a relatively high Earth abundance [228].

The stacked MX_2 monolayers that build the structure of a TMDC crystal are illustrated in Fig. 2.1(a), where yellow and black spheres correspond to chalcogen and transition metal atoms respectively. The distance of two layers is about 6.5 Å. Three WS_2 crystals and one MoS_2 crystal are shown in Fig. 2.1(b) and (c) respectively. An optical image and an AFM image of two MoS_2 multi-layer flakes exfoliated from the bulk crystal presented in (c) are presented in Fig. 2.1(d) and (e) respectively. A surface profile across the two flakes is shown in Fig. 2.1(f)[1]. The investigation with an AFM clearly displays the atomically flat surface of the MoS_2 flake. TMDCs are known to have very few trapped states and dangling bonds, which makes them suitable for many applications, especially in the context of ionic liquid topgates. A detailed discussion of TMDCs as channel materials in EDL transistors will be given in section 2.2.

In nature, the most commonly found lattice structure of TMDCs is hexagonal, rather than tetragonal, and it was found that this structure provides higher dynamic and thermal stability [125]. Ataca *et al.* predicted 52 different stable transition metal oxide and dichalcogenide single layer compounds from 88 different element combinations [13].

1 The two crystals presented in Fig. 2.1(b) and (c) are the mother crystals for exfoliated flakes that we investigated in the form of EDL-gated field-effect transistors. For instance, the flakes in Fig. 2.1(d) and (e) became later device JS087a, whose investigation will be shown and discussed in section A.2, together with measurements on WS_2 thin flakes.

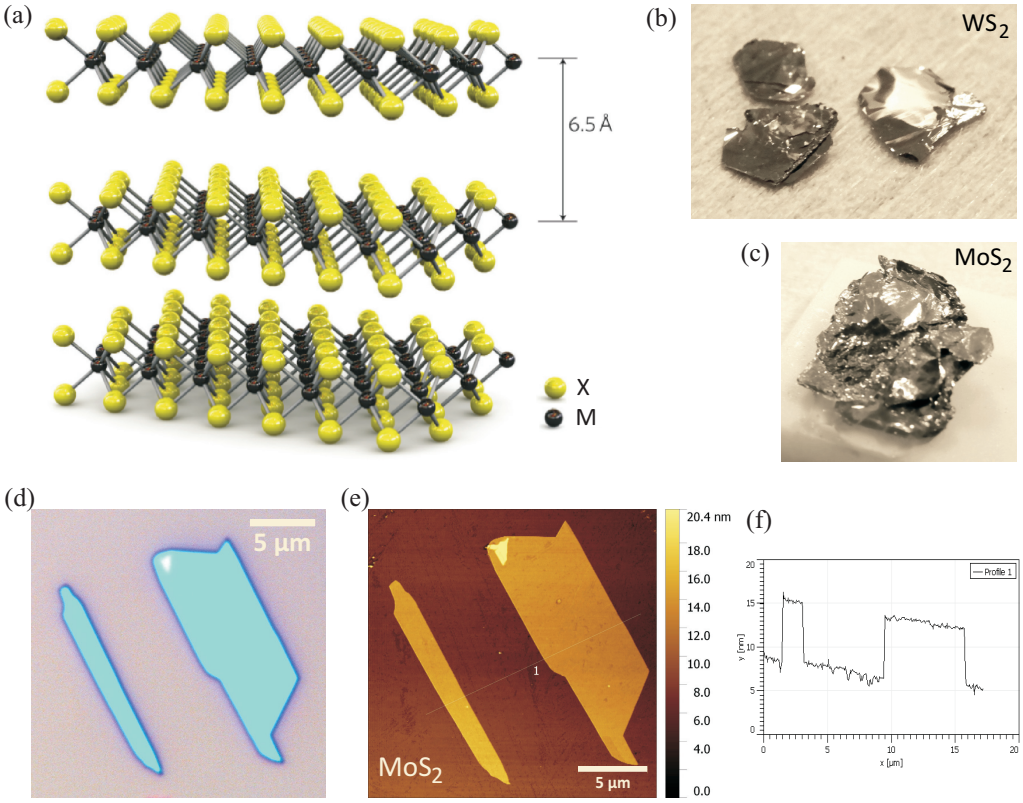

Figure 2.1: (a) Structure of a TMDC crystal, taken from [170]. (b), (c) Photos of three WS_2 and one MoS_2 crystals. (d) Optical image of MoS_2 thin flakes after exfoliation onto a SI/SiO_2 substrate. (e), (f) AFM image and surface profile of the same flakes. Atomically flatness and therefore high quality of the flakes is noticeable.

It was discovered that the band structure of a TMDC thin film changes when the number of layers is decreased. In particular, the group VI compounds develop a transition from an indirect bandgap at the Γ-point of the Brillouin zone to a direct bandgap situated at the K-point in the monolayer limit [105, 129]. This reveals new properties such as a valley degree of freedom (see in the following section) and it allows applications in the fields of photodetectors and electroluminescent devices. The monolayer bandgaps of TMDCs vary from 1.1 eV to 2.1 eV, depending on the constituent elements. These gap values are comparable to the bandgap of silicon (1.1 eV), which makes TMDC flakes potential replacements of silicon, for example in digital transistors [228]. Note that TMDC crystals are expected to have the Fermi energy in the centre of the bandgap and are therefore well suited for ambipolar operation. One exception is MoS_2, which is always slightly n-doped, due to sulphur vacancy [151, 170].

One factor which might potentially limit the operation performance of TMDC transistors is the phonon-limited mobility. In the case of MoS_2, a mobility maximum of $\approx 400\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at room temperature is theoretically expected and the highest room temperature mobilities in TMDCs were predicted for monolayer WS_2 and calculated to reach $\approx 1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [46]. In practice, mobility is limited by several factors and not only depends on temperature, but also on the amount of impurities as scattering centres and the dielectric environment.

Consequently, TMDCs might never compete with conventional transistors on mobility, but nevertheless, due to their high degree of electrostatic control, they are good candidates for low-power electronics [228].

2.1.2 Main Applications of TMDCs

Due to their high Earth abundance, their thermal stability and their structure of only very weakly bond layers, the main application of TMDCs lies in lubricants. However, after the realisation of the first working nano-devices, the investigation of TMDC devices has expanded a lot and especially after the discovery of direct bandgaps in monolayers, the fields of possible applications have multiplied in manifold respects.

One of the first experimental observations was photoluminescence in monolayer TMDCs, e.g. in MoS_2 [202] and in synthetic WS_2 [74]. Interestingly, photoluminescence was not only observed for monolayers, but also in the case of indirect bandgap multi-layers. The evolution of photoluminescence intensity with the number of layers will be discussed in chapter 5, based on some more examples from literature.

The probably most ground-breaking work on TMDC thin flakes was presented by the group of Kis in Lousanne in 2011, who realised a high-performing MoS_2 monolayer transistor with a 30 nm thick layer of HfO_2 as topgate high-κ dielectric [170]. A 3D drawing of the device is shown in the inset of Fig. 2.2(a), whereas the figure itself shows the transistor transfer characteristic in semi-logarithmic scale. The operation is n-type, as expected for MoS_2. Current on-off ratios of $>10^8$ and a subthreshold swing of 74 mV/decade were observed. Even more excitingly, room temperature field-effect mobilities of up to $217\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ were found, which is by about two orders of magnitude higher than mobilities of MoS_2 reported up to that point. A linear transfer characteristic is displayed in 2.2(b), where a grey dashed line indicates the highest slope, used to calculate mobility.

Another high-performing ambipolar TMDC transistor, based on synthetic few-layered $MoSe_2$, was presented by Pradhan *et al.* [164]. I_{on}/I_{off} ratios of up to six orders of magnitude were observed for both hole and electron doping and even though the dielectric is a standard SiO_2 layer, room temperature Hall mobilities up to $\mu_H = 250\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ were observed. Source-drain current versus backgate voltage and square resistivity as well as Hall mobility as a function of gate bias are displayed in 2.2(c) and (d) respectively.

The highest mobility in WS_2 crystals achieved so far, was obtained in monolayers sandwiched between two hexagonal boron nitride films and reaches values up to $214\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at room temperature [92]. Other techniques to increase device operation performance and especially intrinsic mobility consist in improving the contacts. For instance, high performing WSe_2 transistors were reported with either chemically doped contacts [55] or using highly doped graphene as contact material [42]. More references and examples of TMDC thin film FETs are given in [94, 228].

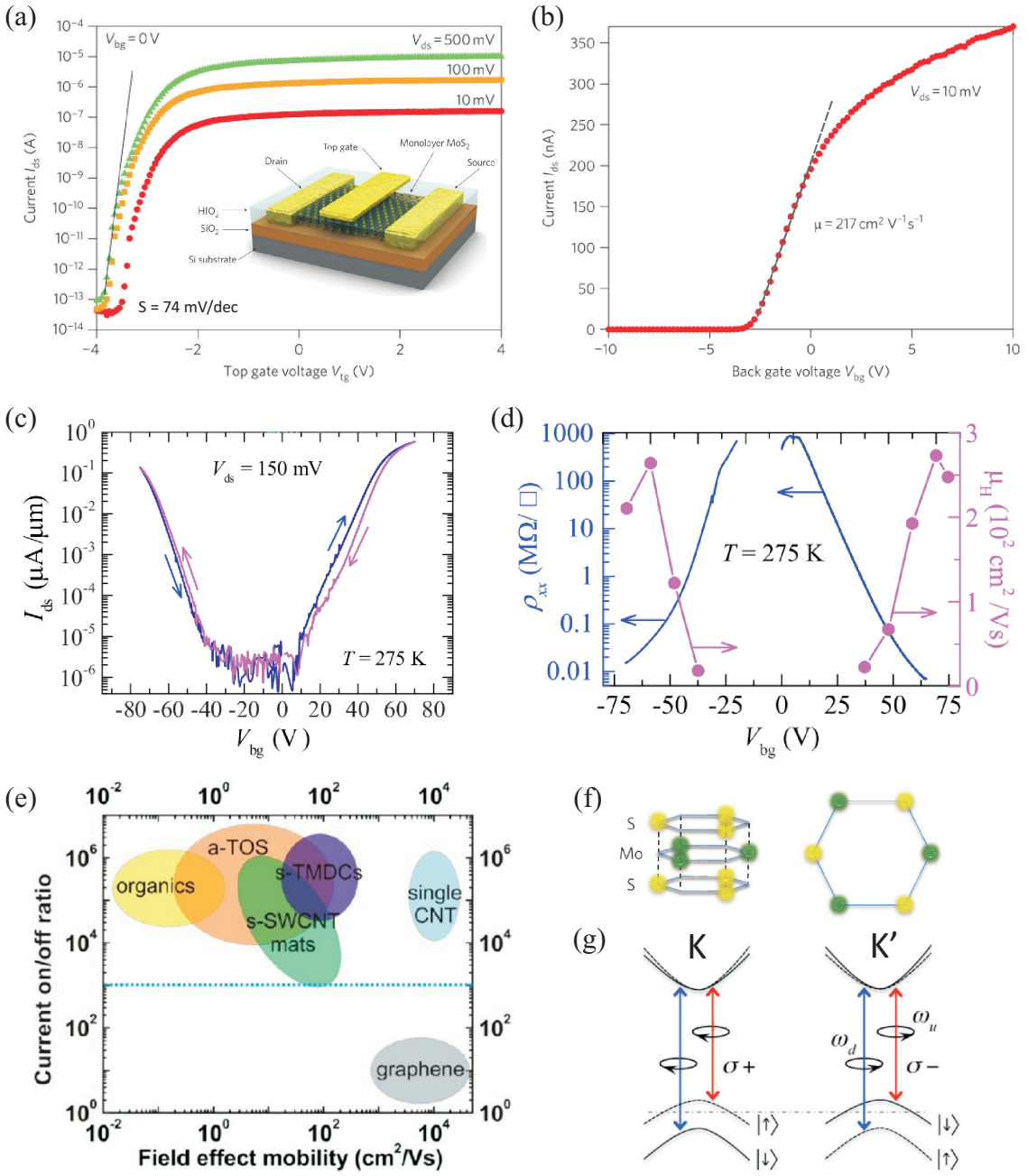

Figure 2.2: (a), (b) Transistor transfer characteristic in semi-logarithmic and linear scale respectively of a high mobility, n-type MoS_2 FET with the high-κ dielectric HfO_2 as topgate. The inset shows the device structure. Taken from [170]. (c), (d) Transfer characteristic and four-terminal resistivity as well as mobility as a function of gate voltage of an ambipolar, high mobility $MoSe_2$ FET, taken from [164].(e) Comparison of field-effect mobilities and on-off current ratios of different families of semiconductors, taken from [94]. TMDCs lie in a favourable position compared to other semiconductors. (f) Drawing of the honeycomb lattice structure of monolayer MoS_2 with broken spatial inversion symmetry taken from [128]. (g) Illustration of the electric structure of a monolayer TMDC crystal, which displays the selection rules of valley and spin optical transition. Taken from [234].

Fig. 2.2(e) classifies the potential of TMDCs for digital electronic applications. It shows the comparison between field-effect mobilities and on-off current ratios for different families of semiconductors. The blue dashed line indicates the minimum requirement of I_{on}/I_{off} ratios for the applicability in digital electronics. TMDCs have similar current on-off ratios as organics, amorphous oxide semiconductors and semiconducting single-walled CNTs and mobilities of TMDCs can even reach higher values. For more details, see ref. [94]. The emergence of TMDCs as high-performing field-effect transistors motivated researchers to integrate them into functional digital circuits, e.g. inverters and logic gates. For instance, the successful fabrication of integrated circuits and logic operations based on MoS_2 single layers was demonstrated [172]. More examples are given in ref. [94, 228, 250]. Another very promising field for future applications is the possibility of creating stacked heterostructures of 2D materials and therefore nano-scale junctions and other functionalities, operating in the out-of-plane direction. For more details, see ref. [8, 66, 209]. Additionally, first heterojunction and thin film TMDC tunnel field-effect transistors were realised [5, 68, 96, 119].

One of the most recent discoveries in monolayer TMDCs is a valley degree of freedom. In the same way as in spintronic devices, where the spin of electrons is used as degree of freedom, valleytronics makes use of the fact that in some materials, the conduction (valence) bands have at least two minima (maxima) at equal energies, but at different positions in the momentum space. The possibility of populating the two valleys separately and to control the population can be used as new and so-called valley degree of freedom [254]. It was found that two-dimensional crystals with a honeycomb lattice structure possess energy-degenerated valleys at the conduction and valence band edges. Transition metal dichalcogenides MX_2, with M = Mo, W, and X = S, Se have all identical, inversion asymmetric crystal structure and their monolayer appearances have a direct bandgap. Therefore, they are very promising candidates for valleytronics. The honeycomb lattice structure with broken spatial inversion symmetry is schematically displayed in Fig. 2.2(f), using the example of monolayer MoS_2. The sublattice sites have an alternating occupation by either one molybdenum or two sulphur atoms [128]. The fundamental bandgaps are located at the K and K' valleys of the Brillouin zone and are spin-split by the spin–orbit interactions [130]. Therefore, split valleys have charge carriers with opposite spin, which results in a coupling between spin and valley degree of freedom [234]. Panel (g) shows the electric structure of a monolayer TMDC crystal and illustrates the selection rules of valley and spin optical transition. Split conduction band minima and valence band maxima at K and K' are displayed and spin-up (-down) quantisation is labelled beside the split valence bands and indicated as dashed (solid) curves. Due to the coupling between spin and valley degrees of freedom, charge carriers can be confined in one particular valley and valley polarisation was achieved by optical pumping with circular polarised light [94, 128, 254].

Xiao *et al.* reported a second feature based on the broken inversion symmetry and gap opening, which is the valley Hall effect, an analogy to the spin Hall effect. The electrons in

different valleys experience effective magnetic fields of opposite signs and equal magnitudes. When a bias voltage is applied, this effect results in Lorentz-like forces and electrons move in opposite directions, perpendicular to the drift current [234].

The valley degree of freedom can potentially be used as information carrier [127] and as valleytronics has operating modes similar to spintronics, analogous devices are feasible, such as valley filters and valves [35]. More information about valleytronics in TMDCs is given in ref. [35, 103, 130, 234, 237, 259].

We have displayed the most studied applications of transition metal dichalcogenides. Some further potential and/or existing applications are based on the abilitiy of the layered structure to intercalate ions or molecules. Therefore, e.g. ion batteries, hydrogen storage and catalysts can be realised [110].

One field of research and applications is the controllability of both p- and n-type charge carrier densities by field-effect, which is especially interesting in the case of high carrier injection when an ionic liquid is used as gate dielectric. This field will be discussed in detail in the following.

2.2 EDL-gating on Transition Metal Dichalcogenides

The surface of exfoliated TMDCs is atomically flat and has very few trapped states and no dangling bonds, which makes this family of semiconductors highly suited for field-effect devices [259]. Especially ionic liquid-gated devices, where an impurity-free and flat surface is crucial for good gating-performance [56], benefit from this cleanliness. For instance, the extraordinary surface quality allowed Braga *et al.* to extract the bandgap of EDL-gated ambipolar operating single WS_2 sheets [30].

The conduction channel built up by field-effect carrier injection in multi-layered TMDCs has proved to be less than 2 nm thick, as Brumme et al. showed that 90 percent of induced charge carriers are accumulated in the first two layers [31]. This study confirms the two-dimensional nature of a conduction channel established by EDL-gating.

As the Fermi energy in high-quality crystals is placed in the centre of the bandgap, transition metal dichalcogenides are expected to show ambipolar behaviour, even the weak n-doping in MoS_2. However, conventional gating methods revealed ambipolar operation only in very few cases (e.g. in $MoSe_2$, presented in Fig. 2.2(b)). With the help of ionic liquids as gate dielectrics, ambipolar operation was found in various TMDCs, amongst others in MoS_2 [161, 194, 260], in $MoSe_2$ [153, 194], in $MoTe_2$ [235], in WSe_2 [176] and in WS_2 [30]. The ambipolar operation of four of the five crystals mentioned, is displayed in Fig. 2.3, where their transistor transfer characteristics are shown. Current on-off ratios of 6-8 orders of magnitude were observed for all TMDC compositions presented, and subthreshold slopes are generally low ($<$100 mV/decade), each time for both polarities. Threshold voltages are $\leq \pm 2$ V for all presented materials. This confirms the excellent low-power, ambipolar

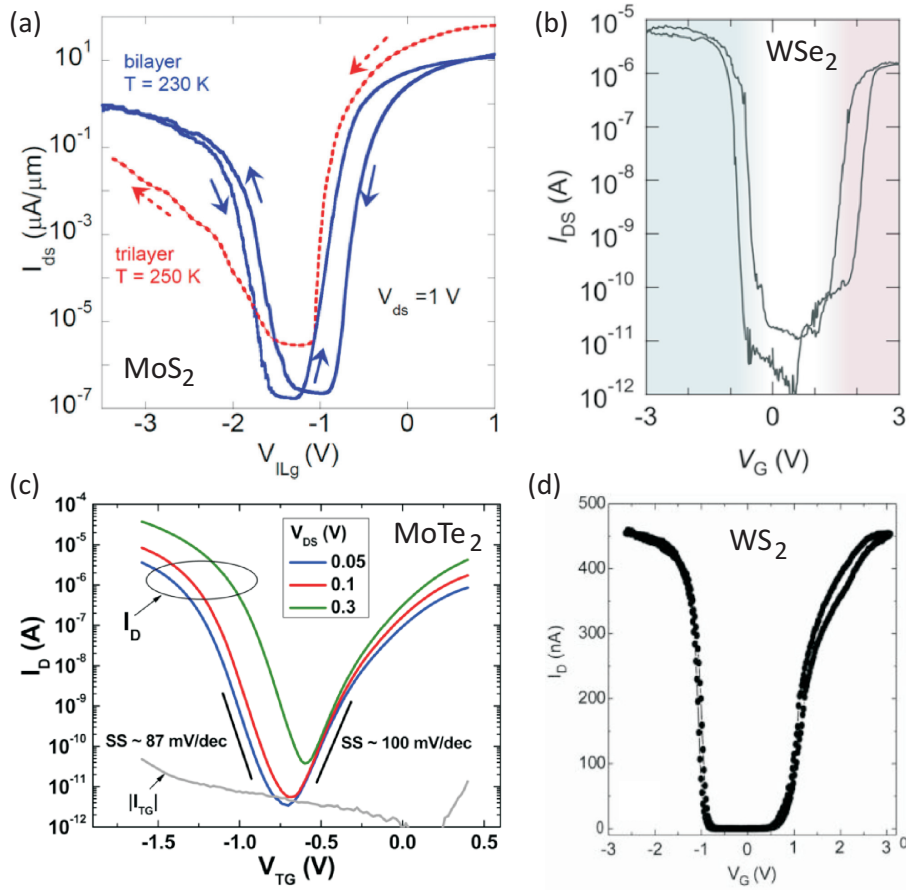

Figure 2.3: Ambipolar operation for five different transition metal dichalcogenide few-layer flakes. (a) MoS_2, taken from [161]. (b) WSe_2 monolayer, taken from [256]. (c) $MoTe_2$, taken from [235]. (d) WS_2, taken from [30].

transistor operation of exfoliated TMDC thin films. The presented WSe_2 and WS_2 devices are non-doped, $MoSe_2$ is weakly n-doped and MoS_2 even slightly higher n-doped, which is the expected behaviour[1]. The best values of EDL-gated TMDC flake transistors are displayed in table 2.1.

Most of the best known transition metal dichalcogenides (e.g. $MoTe_2$, WS_2, $MoSe_2$, MoS_2) become superconducting at high field-effect n-type doping levels with transition temperatures ranging from 3 K to 10 K. The superconducting transitions of MoS_2, WS_2 and $MoSe_2$ flakes are displayed in Fig. 2.4(a)-(c). At high doping levels, all crystals show clearly metallic behaviour. A list of critical temperatures and materials is given in table 2.1. Note that superconductivity has only been observed for electron doping up to this point, the observation of hole superconductivity is still missing.

Two more phase transitions were observed by using the technique of EDL-gating. For

1 The weak doping of the presented MoS_2 crystal as well as weak doping in other TMDC materials that have been presented in literature, e.g. [6, 42, 98, 164] is due to impurities and different crystal qualities in naturally grown crystals.

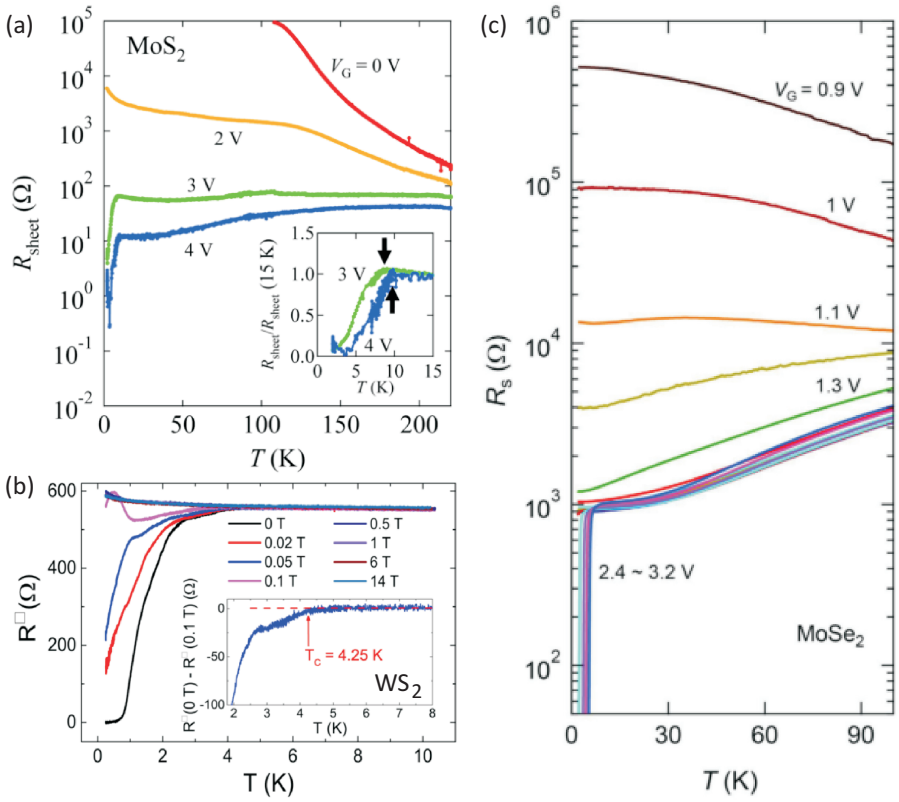

Figure 2.4: Superconducting transition for three different transition metal dichalcogenide few-layer flakes, all measured in four-probe configuration. (a) MoS_2, taken from [210]. (b) WS_2, taken from [98]. (c) $MoSe_2$, taken from [194].

Table 2.1: Critical temperatures and record values of different parameters of EDL-gated transition metal dichalcogenides.

parameter (unit)	MoS_2	$MoSe_2$	$MoTe_2$	WS_2	WS_2 nanotubes	WSe_2
T_c (K)	10 [210]	7 [194]	3 [194]	4 [98]	5,8 [168]	
μ_h ($cm^2\,V^{-1}\,s^{-1}$)	86 [260]		26 [235]	90 [30]		1800 [247]
μ_{el} ($cm^2\,V^{-1}\,s^{-1}$)	100 [161]		30 [117]	83 [46]		100 [257]
$S^{h}_{s\text{-}th}$ (mV/decade)	≈50 [161]		87 [235]	63 [99]		≈60 [165]
$S^{el}_{s\text{-}th}$ (mV/decade)	≈50 [161]		100 [235]	52 [99]		63 [165]
$h - I_{on}/I_{off}$	$>10^6$ [161]		10^5 [235]	10^5 [99]		10^6 [257]
$el - I_{on}/I_{off}$	$>10^7$ [161]		10^5 [235]	10^6 [156]		10^7 [42]
I_{off} (pA)	<100 [245]		<10 [235]	3 [156]		<10 [256]

instance, an insulator-to-metal transition was observed in TaS_2 [248] and a ferromagnetic transition was observed in cobalt and cobalt-doped titanium dioxide [195, 238].

One of the most remarkable abilities of EDL-gated transistors is the purely electrostatic formation of a pn-junction in the conduction channel. This effect was first shown in MoS_2 by Zhang *et al.* [258], followed by the observation of field-effect induced pn-junctions in various TMDC materials. The detection of a pn-junction was mostly done by the observation of radiative recombinations and therefore electroluminescence. At the beginning, radiative recombinations were expected only in monolayer flakes, due to their direct bandgaps. However, electroluminescence has been observed experimentally in few-layer flakes and even in bulk material with largely reduced intensities. Especially at room temperature, both electroluminescence and photoluminescence were measurable in thick films. The reason is that high temperatures allow both the phonon-assisted recombination in an indirect bandgap and the population of the higher energetic direct gap, which is still present in multi-layer flakes. For instance, electroluminescence was detected in ambipolar FETs based on WS_2 mono- and bilayer [99] and circular polarised light emission in EDL-gated WSe_2 and $MoSe_2$ [153, 257], as well as in synthetically grown MoS_2 [241]. Due to the effect of valley polarisation, the chirality was observed to be electrically switchable by changing the polarity of the drain-source bias [256].

The explanation of how an electrostatically induced pn-junction is created in an EDL-gated transistor will be given in chapter 5, together with studies on the variation of electro- and luminescence intensities caused by changing the number of layers.

2.3 TMDC Nanotubes

After the discovery of the potential of carbon nanotubes in electric devices, a new and exciting field of novel nano-scale materials developed. One year after the first synthesis of CNTs in 1991, R. Tenne and co-workers developed a growth process for WS_2 nanotubes and MoS_2 nanotubes [57, 212]. These inorganic tubular nano-structures are multi-walled and diameters range from several tenths to hundredths of nm with lengths of several µm [205]. As MoS_2 nanotubes have hardly been studied, we will not consider them any further. Investigations of WS_2 nanotubes with a transmission electron microscope (TEM) revealed that approximately half the diameter is hollow [212] and that the nanotube edges can be both open and closed. Fig. 2.5(a) shows an optical image of a WS_2 nanotube with a length of 12 µm and a diameter of 50 nm. Panel (b) and (c) display three-dimensional graphic simulations of a multi-walled TMDC nanotube, showing the different walls in each of which an atomic layer of transition metal atoms (blue) is sandwiched between two atomic layers of chalcogen atoms (yellow). It is also observable that one wall of the inorganic nanotube can be seen as a rolled WS_2 monolayer. 2.5(d) is a TEM image of a WS_2 nanotube with a diameter of 25 nm. The inner and outer diameters are indicated by white lines.

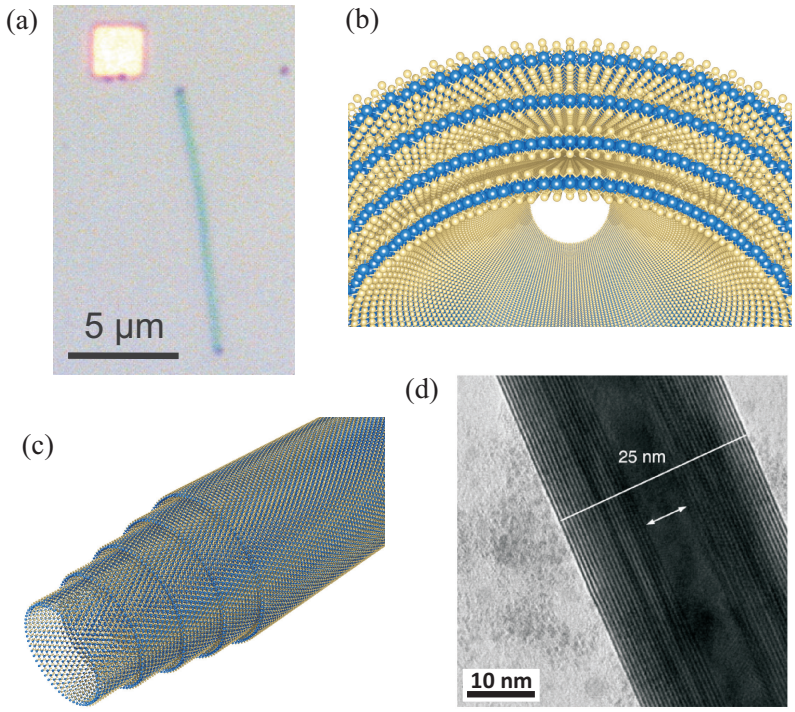

Figure 2.5: (a) Optical images of an isolated WS_2 nanotube on a Si/SiO_2 substrate. (b), (c) 3D graphics of a multi-layered TMDC nanotube, simulation done by Johann Coraux, Néel Institute, CNRS Grenoble. (d) TEM image of a multi-walled WS_2 nanotube. Inner and outer radius are indicated, the outer radius of this tube is 25 nm. the image was received from the manufacturer of the nanotubes used in this work, Reshef Tenne.

WS_2 nanotubes have quite similar mechanical properties as the two-dimensional crystal appearance. Even though their electronic properties are poorly known, they are predicted to be all semiconducting, in contrast to CNTs[1] and to possess an indirect band gap of a size similar to that of bulk WS_2 layered crystals (1-1.3 eV) [187, 232, 261]. This indicates a strong potential for the use in semiconducting device applications and soon after the discovery, a huge interest was growing towards using WS_2 nanotubes as functional devices or in highly integrated functional devices. For instance, theoretical work predicts that the confined structure will lead to more distinct electrical and optical properties than it is the case for two-dimensional flakes [38, 187]. Many studies have been done to investigate electromechanical properties [67], applications in medicine [108] and potential applications such as biosensors, safe containers, strengthening fibres, high-energy-density batteries, sensors and in the photoconversion of solar energy[2] [79]. Studies of their use in electronic devices revealed their potential for vacuum nanoelectronics, flat panel display applications [223] and field-effect sensitive devices [115].

Theoretical studies showed that nanotube transistor devices would perform best with a

1 Single-walled carbon nanotubes exhibit metallic properties with a particular chiral structure [178]
2 Note that up to now, due to their high thermal stability, the main application of WS_2 nanotubes is as lubricants, similar to the layered 2D crystals.

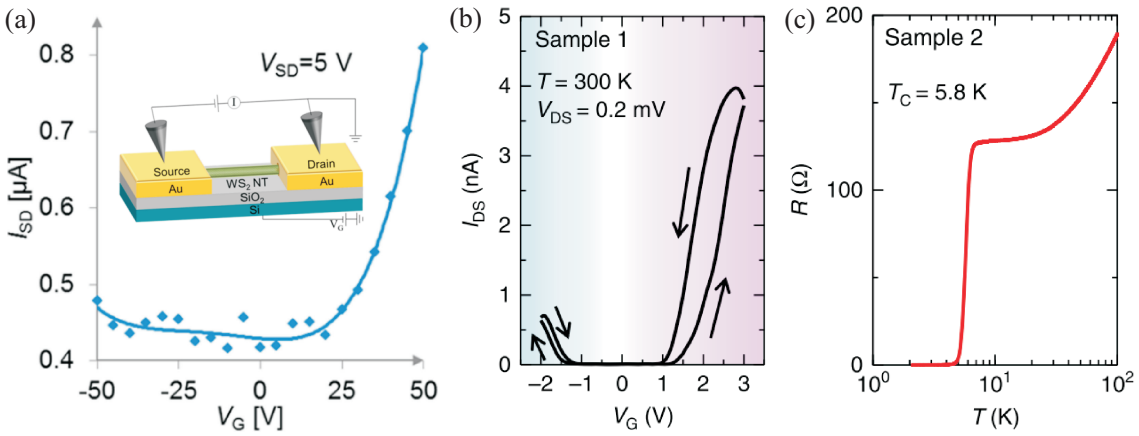

Figure 2.6: (a) Transfer characteristic of the first field-effect transistor based on a multi-walled WS_2 nanotube. The inset shows the device structure of the backgated tube, taken from [115]. (b) Ambipolar transistor transfer characteristic of the first ionic liquid-gated multi-walled WS_2 nanotube. (c) Superconducting transition of the same tube. (b) and (c) taken from [168].

gate around the tube [70, 81, 189]. Due to their similarly high surface qualities, WS_2 nanotubes promised to be as good candidates for EDL-gating, similar to WS_2 thin flakes. As an ionic liquid provides a gate all around the nanotube, EDL-gating appears to be a promising technique to create high performance field-effect transistors. For instance, one ionic liquid-gated WS_2 nanotube transistor was realised very recently by the group of Iwasa [168] and outperforms the only published solid backgated WS_2 nanotube FET [115] by far. Backgated and liquid-gated field-effect transistors are displayed in Fig. 2.6(a) and (b) respectively. Lower off-currents and ambipolar behaviour characterise the EDL-gated transistor. The lower on-state currents, compared to the backgated transistor, have their origin in the voltage bias which is by more than one order of magnitude lower than that of the solid-gate FET. Furthermore, the liquid-gated nanotube becomes superconducting at high electron doping levels. The superconducting transition at a critical temperature $T_c = 5.8\,\mathrm{K}$ is displayed in Fig. 2.6(c). For comparison, the critical temperature of the WS_2 nanotube is displayed in table 2.1 together with the values obtained in TMDC thin films. Note that in contrast to the hardly longer existing CNTs, WS_2 nanotubes were investigated very little. Especially their electronic properties were presented by no more than two groups up to this point, whereas one of them published after we had started to examine their transport properties.

The combination of a random network of WS_2 nanotubes and ionic liquid promises to be applicable in transparent, flexible and stretchable devices, as well as in printed devices. The first realisation of such a random network of nanotubes was recently presented by the group of Yanagi, who presented an ambipolar operation with current on-off ratios of almost four orders of magnitude and hole (electron) mobilities of $3.6\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ ($0.3\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$) [205]. They also investigated thermoelectric properties [102]. These studies underline the high potential of TMDC nanotubes for easily fabricated flexible electric devices. In chapter 7, we will explain that the gelation of ionic liquids is a necessary step in order to realise

such novel electric devices.

2.4 Downscaling of FETs by Using TMDC Nanotubes and Ionic Liquids

Ongoing downscaling of field-effect devices is limited by severe short-channel effects, such as increased off-currents, increased subthreshold swings and lowered I_{on}/I_{off} ratios [211]. The search for new materials is on, in order to continue miniaturisation at the current level. Promising candidates for overcoming parasitic effects are carbon nanotubes with a ring gate around the nanotube [70]. CNTs itself can carry high current densities over several micrometers with a fixed resistance and are free from edge effects [123], which makes them well suited for on-chip interconnect applications. However, it is not yet possible to control the growth of CNTs in a way that only semiconducting nanotubes are produced. A solution can be found by replacing CNTs by other nanotubes of similar stability and current carrying capacity. TMDC nanotubes were found to be good candidates to minimize parasitic effects at the limits of scaling [123].

In another approach, calculations showed that replacing a solid gate dielectric by a state-of-art high-κ dielectric lowers short channel effects drastically and the channel length can be reduced to a sub-10 nm length [36]. For instance, it was shown that short-channel effects can be suppressed by high transversal electric fields, generated by an electric double layer [84].

An EDL-gated TMDC nanotube device satisfies all requirements: the tubular channel, the gate geometry all around the tube and a very high capacitance. Therefore, our devices of ionic liquid-gated multi-walled WS_2 nanotubes are promising candidates to replace existing nanoelectronics.

A detailed overview of the arising problems with device miniaturisation and the potentials of inorganic nanotubes in this field is given in [79].

2.5 Conclusion and Outlook

We summarised the properties and main applications of transition metal dichalcogenides with a focus on EDL-gated devices. The high potential of this family of materials to be used in various fields, such as low-power, fast switching, ambipolar FETs and light-emitting transistors were shown on the basis of literature. The remarkable band structure gives rise to a new degree of freedom, the valley degree of freedom, which can potentially be used as information carrier. Additionally, most of the best known TMDC materials become superconducting at high n-type doping levels with T_c ranging from 3 K to 10 K.

We also introduced a second allotrope of TMDCs, i.e. nanotubes, where we focused on the most studied species, at WS_2 nanotubes. Their mechanical and electrical properties are close to those of few-layer flakes and first investigations, using the EDL-gating technique,

showed ambipolar behaviour and superconductivity at high electron doping levels. EDL-gated nanotubes were found to be good candidates for novel materials in the context of the downscaling of devices, because short-channel effects are diminished.

It was mentioned that these inorganic nanotubes can be used in the "futuristic" fields of flexible, stretchable, printable and wearable electronics. Their ability to build up random networks that, when combined with ion gels, can be ultra-thin and patterned on any substrate, is all that is required for printable and stretchable devices. The discussed first and very promising attempt of ambipolar transistors based on random networks of WS_2 nanotubes was realised very recently [205]. Improvement is to be expected soon.

CHAPTER 3

Fabrication

In this chapter, we will present the fabrication of multi-walled WS_2 nanotube, WS_2 flake and diamond devices. All fabrication steps from the bare substrate to the finished device, provided with ionic liquid, will be explained. We will start with the description of the dispersion and localisation of WS_2 nanotubes as well as exfoliation and visualisation of TMDC crystals and the realisation of metallic contacts on the TMDC materials. Then we will present the fabrication process of intrinsic diamond Hall bars. We will give a general description of the technique used to provide devices with a droplet of ionic liquid, which was the same for all investigated materials. Finally, we will discuss the problems we had to face during the development of fabrication processes.

All fabrication steps described in this chapter were done in the Nanofab cleanroom facilities and laboratories of the Néel Institute in Grenoble, France. The fabrication of samples that was not done by us will be described roughly in the corresponding chapter, which is chapter 7 for $SrTiO_3$ samples and chapter 6 for doped Si samples.

3.1 Fabrication of TMDC Samples

The main focus of this work was put on the investigation of the possibilities offered by EDL-gating of multi-walled WS_2 nanotubes. Consequently, the development of a good fabrication process for realising such samples was crucial. In parallel, we investigated two types of TMDC thin films, MoS_2 and WS_2 in order to prove our ability to reproduce published data and to determine the field-effect-induced charge carrier densities. With the latter, we can calculate the capacitance of the ionic liquid used for our measurements. Note that Hall measurements cannot be done on nanotubes, which was the main reason for us to measure WS_2 flakes, patterned in Hall bar geometry. In the following, we will describe both the fabrication steps from powder to contacted nanotubes and the technique of isolating several TMDC monolayers and the steps necessary to have a finished device.

3.1.1 Realisation of Electrical Contacts on WS_2 Nanotubes

Inorganic WS_2 MWNTs were grown in a large-scale fluidized-bed reactor [252]. We received them as powder, grown and provided by our collaborator Reshef Tenne from the Weizmann

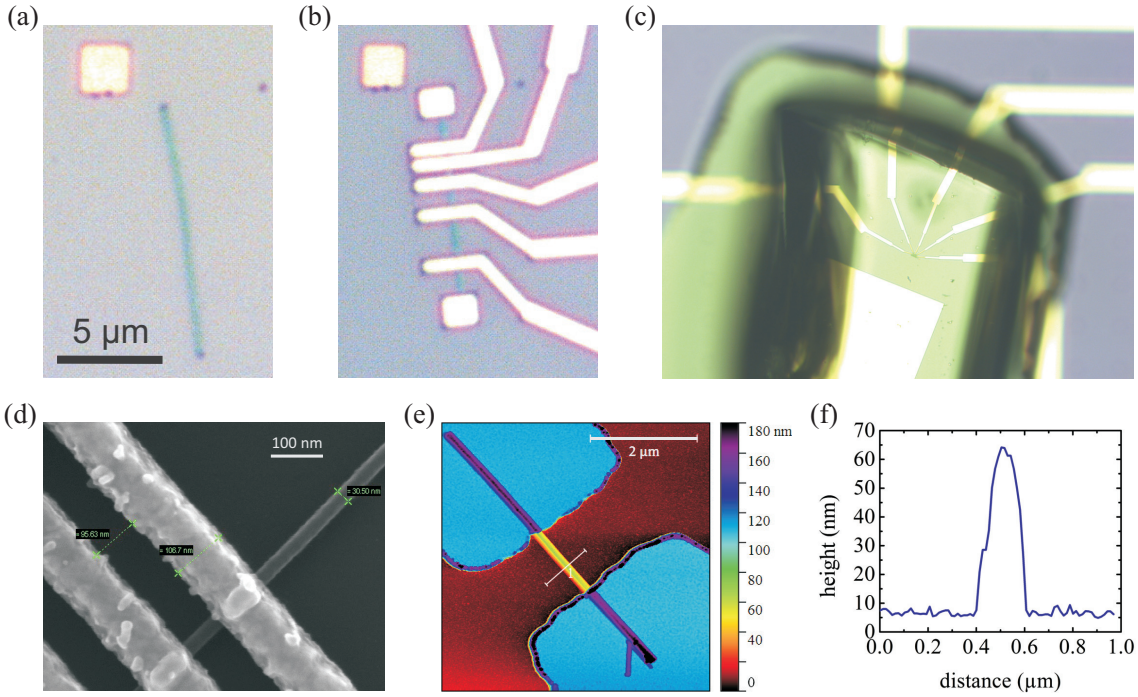

Figure 3.1: (a), (b), (c) Optical images of an isolated WS_2 nanotube on the Si/SiO_2 substrate after dispersion, after the lift-off and provided with ionic liquid ready to be measured. (d), (e) Scanning electron microscope and AFM image of two different WS_2 nanotubes. Both microscopy techniques were used to measure the nanotube's diameter. (f) Surface profile of the AFM image across the nanotube, which we used to extract the diameter.

Institute of Science, Israel. We diluted the tubes in ethanol and as they were accumulated in packets, the nanotubes had to be separated by putting the dispersion in an ultrasound bath at lowest power for about 30 s[1]. Si++/SiO_2(285 nm) substrates, provided with a markerfield, were placed and left in the dispersion for 1 min and subsequently dried in air, which resulted in dispersed, isolated INTs all over the substrate. WS_2 MWNTs were located using optical microscopy. Fig. 3.1(a) shows an optical image of one 12 µm nanotube. On one sample, the number of INTs qualitatively good enough for being measured varied from 3 to 8, whereas tube length was in the range of 3 µm to 16 µm and diameters in the range of 25 nm to 100 nm. The metal square visible in the photo belongs to the markerfield that was used to locate the INTs on the substrate[2]. From now on, we will refer to one contacted nanotube as one device and to a substrate with several devices as a sample.

Nanotube diameters as well as the quality of the tubes' surfaces were determined by either atomic force microscopy (AFM) or scanning electron microscopy. Images of two INT devices, taken with both a scanning electron microscope and an atomic force microscope are displayed in Fig. 3.1(d) and (e). A profile across the AFM imaged nanotube is shown

1 It was very important to limit time and power to a minimum in order to avoid damaging the nanotubes.
2 Many squares were added inbetween the coordinate system of the markerfield. They were used to position the optical images in the design of the markerfield in order to be able to draw the contact design for the lithography.

in (e), where a diameter of $\sim 60\,\text{nm}$ can be extracted. Contact electrodes on the INT were made by electron beam lithography (masquer Nanobeam Nb5 (20kV-100 kV)) and subsequent e-gun evaporation of metal contacts consisting of Pd/Au/Pt with thicknesses of 5 nm/80-110 nm/5 nm. The palladium is the so-called sticking layer that establishes the electric contact to the WS_2 and the platinum layer serves as protection layer to diminish electrochemical reactions between ionic liquid and metal contacts. The thickness of the gold layer was adapted to the diameters of the nanotubes in order to deposit a total layer of metal which exceeds the diameter of the largest nanotube on the substrate by at least 20 %.

Within the lithography step for the contact lines, each device was provided with small metal squares closing the tube and preventing the electrolyte from entering the tube (see Fig. 3.1(b)). In the same step, a coplanar, rectangular electrode was placed close to the nanotube, which acts as gate for the ionic liquid. We will refer to it as counter pad or counter electrode. The finished device provided with ionic liquid is displayed in Fig. 3.1(c). The big counter electrode is clearly visible beside the device. As described in section 1.2, the counter pad's surface needs to be by 1-2 orders of magnitude larger than the total surface of all transport contacts covered by electrolyte, in order to enable charge carrier injection [161]. A finished sample after lift-off is displayed in Fig. 3.2(a).

3.1.2 TMDC flakes - from Bulk Crystal to Thin Film Device

TMDC crystals are layered materials consisting of stacked monolayers bond via Van der Waals forces. As the structure of these materials is the same as in graphite, the layers can

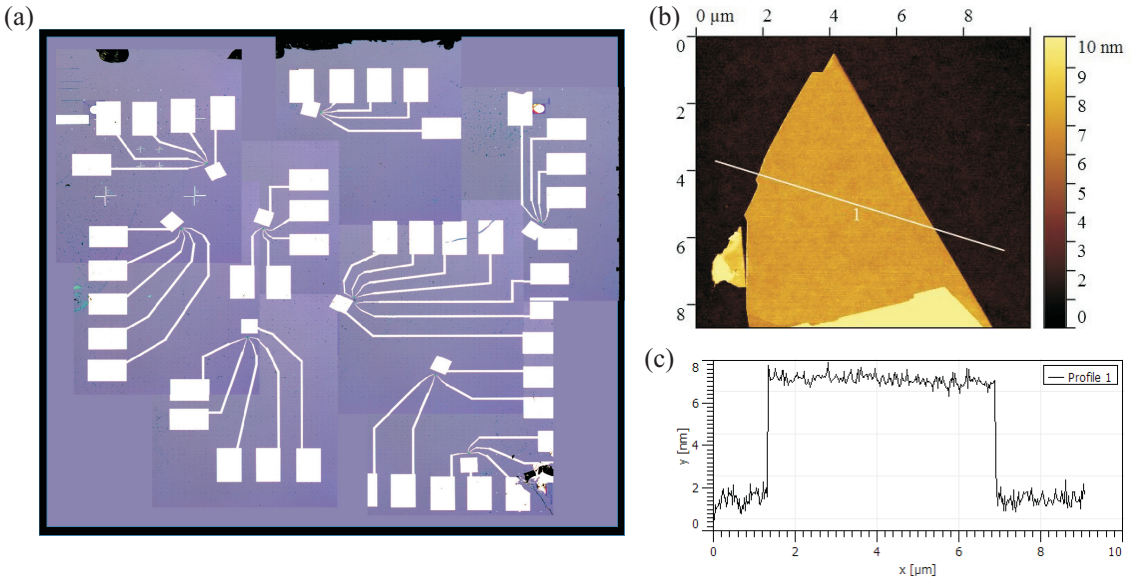

Figure 3.2: (a) Sample JS110: optical images of all devices of one sample after the lift-off, reassembled to show the whole sample. (b), (c) AFM image and surface profile of a WS_2 flake with a thickness of 5.5 nm. The cleanliness and atomic flatness of the exfoliated flake is clearly visible.

easily be separated by the scotch-tape exfoliation technique demonstrated by Geim and Novoselov to isolate graphene[1] [150, 151]. We want to cite a beautiful sentence of their paper which describes this technique better than we could do: "Superficially, the technique looks as nothing more sophisticated than drawing by a piece of graphite or its repeated peeling with adhesive tape until the thinnest flakes are found." [214]. The idea is to put a small graphite crystal on a piece of scotch tape and to cleave it repeatedly with the same tape until the latter is covered by crystal pieces. When placing the tape on a cleaned[2] substrate, flakes of various thickness fall down on the substrate, which can be located by using an optical microscope.

We exfoliated the two materials WS_2 and MoS_2 and obtained atomically flat flakes suitable for measurements with a thickness ranging from 5 nm to 85 nm. Thickness and surface quality were measured by AFM imaging. One AFM image of a 5 nm thick WS_2 multi-layer and a surface profile across the flake are shown in Fig. 3.2(b) and (c) respectively.

3.1.3 Contact Metal for Highest Charge Carrier Doping

In the case of electrolyte-gated TMDC field-effect transistors, three general factors are important in order to choose the right contact material.

The first is the choice regarding work function. It was observed and analytically verified that contact metals with lower work functions are preferable, as they lead to smaller Schottky barrier heights and consequently to higher charge carrier injection through the contacts [225]. However, this statement was demagnified by Yang *et al.* who claimed that simply using contact metals with low work functions is not sufficient to achieve low contact resistances, as the Fermi energy is pinned at the charge neutrality level, which is the centre of the bandgap in clean TMDCs and therefore, there will always be Schottky barriers [240][3]. Another observation of Du *et al.* emphasises that just comparing work function values is not sufficient, due to heavily pinning effects: the contact metal Fermi-level is pinned near the conduction band edge of the semiconductor and therefore both low and high work function metals result in an n-type electrical characteristic [52]. Additionally, first-principles calculations showed that adsorbed gas molecules or physisorbed molecules change the work function and carrier concentration, without destroying the band structure of monolayer WS_2 [262]. Therefore, the coverage with ionic liquid might as well change electric properties of the crystal. All in all, this field is still under study and regarding work functions will not necessarily help us to find the best contact metal.

1 With this technique, Gaim and Novoselov demonstrated that graphene (monolayers of graphite) can be separated from the bulk crystal and that it is stable. The two physicists were awarded the Nobel price for "groundbreaking experiments regarding the two-dimensional material graphene" in 2010.

2 All our substrates were cleaned in acetone and isopropanol and organic residues were removed by applying oxygen plasma for 5 min.

3 Note that they achieved record low contact resistance on both MoS_2 and WS_2 flakes after effective chloride molecular doping.

The second factor is the strong band bending due to the ionic liquid as discussed in the previous chapter in section 1.2.3. The strong electric field established at the channel/ionic liquid interface causes an important band bending which very efficiently thins the Schottky barriers present at the contacts [161]. Charge injection happens by tunnelling through the barriers and consequently, the barrier heights are no longer important. This statement would make a choice of material unnecessary as nearly any metal should lead to similar contact resistance.

However, another parameter gets important when an electrolyte is used as gate dielectric: the gate leakage current caused by electrochemical reactions with the metal contacts, which is our third factor. In section 1.2.4 we discussed the origin of leakage currents and their dependence on contact metals, where we observed that up to a gate voltage of $\leq \pm 4\,\mathrm{V}$ applied to the ionic liquid, only titanium shows a sign of electrochemical reactions and therefore an increase in leakage current. Hence, we can conclude that titanium is to be avoided as contact metal, but all other tested metals are good candidates for EDL-gating.

Our final choice of palladium as sticking layer was done by the most pragmatic way, by observation. On WS_2 MWNTs, we only tried gold, palladium and titanium. Best ambipolar device performance was given with palladium as sticking layer, whereas gold was hardly less performing. Titanium gave rather bad performance and enabled only very low current injection ($I_{on}/I_{off} \leq 10^2$). As work functions of palladium and gold are 5.12 eV and 5.1 eV respectively [137], the work function of titanium is 4.33 eV [137], whereas the work function of WS_2 is 5.1 eV [58], this observation suggests that an alignment of work functions might still be a necessary condition for ambipolar operation. For a general conclusion, however, a wider analysis is needed.

3.2 Fabrication of Diamond Samples

All diamond substrates used in this work are of the brand Sumitomo and are of crystal direction (100). After growth, the substrates of $3 \times 3\,\mathrm{mm}$ and $300\,\mu\mathrm{m}$ height were highly polished in order to gain a roughness of $<1\,\mathrm{nm}$. Fig. 3.3(a) shows an AFM image taken in the centre of a clean and highly polished intrinsic diamond substrate, (b) shows a surface profile and (c) the 3D graphic of the AFM image. The average roughness was estimated to be $\approx 0.1\,\mathrm{nm}$, which indicates the high quality of the diamond.

Before using the substrates, we cleaned them in acetone and ethanol (each time 5 min in an ultrasound bath with highest power) and finally in Aqua Regia (HNO_3, HCl (1:3)), in order to remove any residual product.

We used a standard optical contact lithography process to pattern the sample with a Hall bar design. After the development, residual resist was removed by 30 s of oxygen plasma. The sample was metallised immediately with Ti/Pt/Au (40 nm/50 nm/30 nm) with subsequent lift-off in Acetone. Ohmic contacts on the intrinsic diamond were realised by

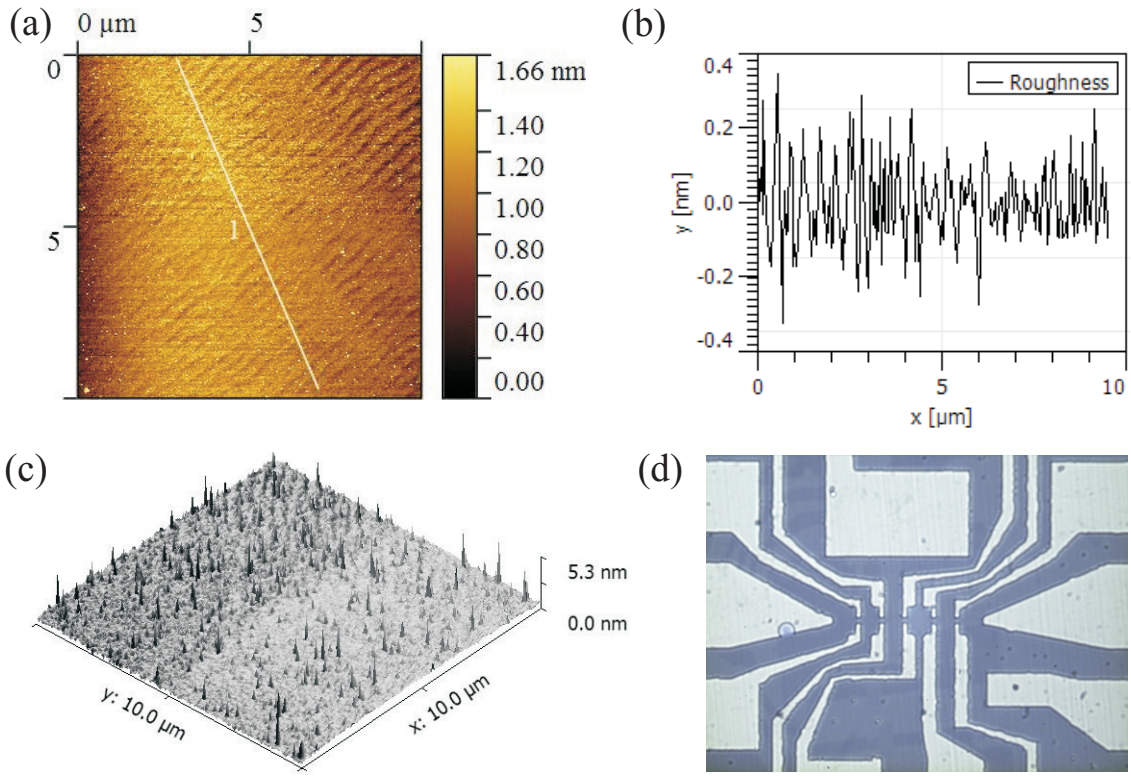

Figure 3.3: (a) 10×10 µm AFM image of the highly polished diamond substrate. (b) Roughness profile along the line in (a). (c) 3D plot of the same AFM image. (d) Optical image of a finished diamond device before provision with ionic liquid.

30 min annealing in high vacuum ($<1 \times 10^{-8}$ mbar) at $T > 600\,^{\circ}$C. During the annealing step, a titanium carbide layer was formed at the titanium/diamond interface, allowing better electric access to the semiconductor. An optical image of a finished diamond sample is shown in Fig. 3.3(d).

Without any further treatment, the carbon atoms on the surface will be saturated with oxygen, hydrogen or other atoms in a non-structured way. Therefore, the surface is disordered and electrically inhomogeneous and has to be treated by either a hydrogen plasma for hydrogen-termination or by an ozone environment for an oxygen-termination of the surface. In both cases, the benefit is an atomically controlled surface, chemical stability and low trap density [182], qualities important for EDL-gating, as trapped states and impurities lead to a degradation of the gating performance. We used substrates with a hydrogen-terminated surface which has the additional property of being conducting. Further explanations of surface properties will be given in chapter 6.1. The hydrogen-termination was realised by 30 min of hydrogen plasma at a temperature of 880 °C.

3.3 Provision with Ionic Liquid

The ionic liquid we used for all measurements presented in this work is 1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIm][TFSI]). We kept the elec-

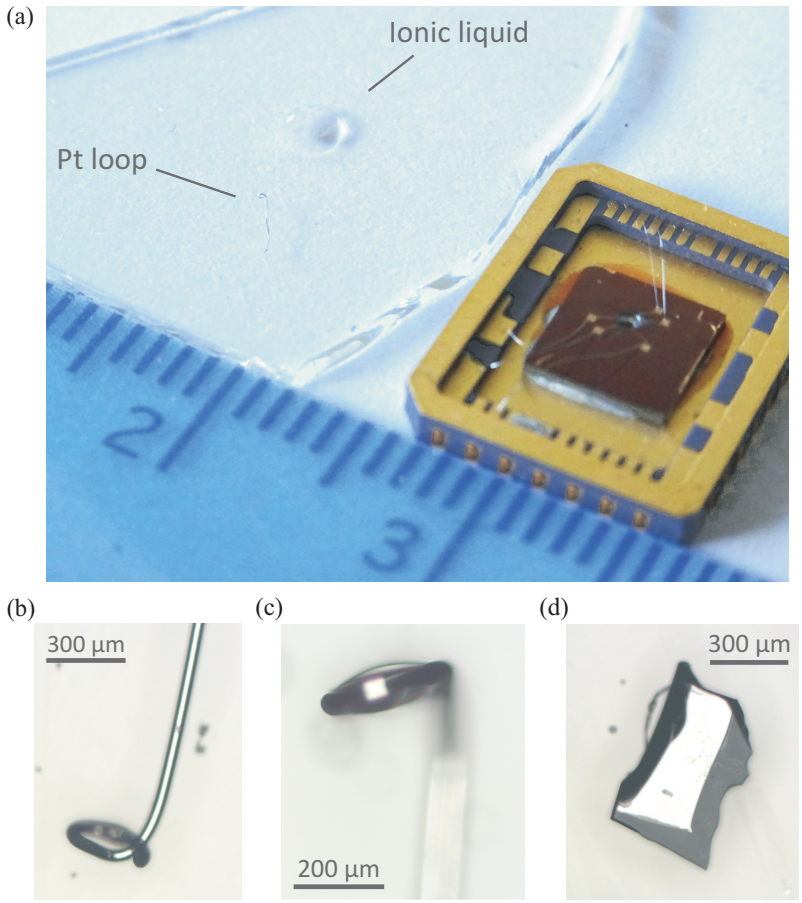

Figure 3.4: (a) Bonded sample on a chip after ionic liquid provision. An electrolyte droplet on a glass slide beside the chip served as stock for the provision of one sample. The tool used to place a small droplet on the device, a thin platinum wire which was bent to a loop on one extremity, is just visible beside the droplet on the glass slide. (b), (c) Photos of the platinum wire and loop without and with ionic liquid droplet. (d) Small piece of a glass substrate we used to cover the electrolyte on the device.

trolyte in a small bottle in a glovebox in argon environment, as it absorbs water when left in air, which degrades its dielectric abilities. For each sample, we only took a small droplet on a glass slide out of the argon environment.

To keep a high ratio between counter electrode surface and total surface of all transport contacts covered by electrolyte, the droplet of ionic liquid should ideally cover no more than the entire counter pad and the conduction channel. Therefore, we used a droplet just big enough to cover these two areas. To do so, we fabricated a special tool: we took a small piece of platinum wire (diameter of 40 µm) and bent one extremity to a tiny loop. When the loop is dipped into the electrolyte, a small quantity of liquid will fill the loop due to capillarity and can then be placed on the sample's surface. A photo of a sample, glued and micro bonded to a chip and provided with a droplet of ionic liquid, is presented in Fig. 3.4(a). The glass slide with the electrolyte droplet we took out of the glovebox and the fabricated tool are displayed beside the chip with the sample. Two photos of the bent platinum wire, one without ionic liquid and one filled with liquid are shown in Fig. 3.4(b)

and (c).

There are two effects which demand another challenge of dexterity. On the one hand, once the electrolyte is placed on top of the device, capillarity effects will make the liquid creep along the edges of the metal contact lines and if the distance to a bonding pad is short, the liquid might eventually end up accumulated at the bonding wire on top of the bonding pad instead on top of the device. On the other hand, it was observed by our close collaborator Shimpei Ono (researcher in CRIEPI, Yokosuka, Japan) that when cooling down a sample provided with electrolyte and passing the freezing point of the liquid, the droplet lifts from the sample's surface and freezes in the shape of an almost perfect sphere. This effect cannot only break a nano-device, but will also block the gate effect, as the interface ionic liquid/channel is then reduced to one boundary point. To avoid such effects, a small piece of a 100 nm thick glass substrate was placed on each device. A photo of a suitable glass piece is shown in 3.4(d). It sticks to the device via capillarity and therefore stabilises the liquid on top of the device. A micro-bonded WS_2 MWNT device, covered by electrolyte and a glass slide, is shown in Fig. 3.1(c).

3.4 Observation and Solution of Fabrication Problems

The development of a fabrication process is in general no straightforward path. During different steps, various challenges have to be faced. In this section, we will display the main issues we had to face on the way to obtain working samples.

3.4.1 Strain Effects in Contact Lines

The metal composition of electric contacts is crucial in our devices. As discussed above, the choice of suiting material is not a trivial one. We have discovered tactics to reduce leakage currents caused by impurities in the electrolyte, but there will still occur electrochemical reactions at high gate voltages applied. These reactions can occur between the electrolyte and the material of investigation, as well as between the electrolyte and the metal contacts. The least reactive metal is known to be platinum, of which we systematically deposited a protection layer on top of our metal electrodes, thick enough to eliminate electrochemical reactions. At the beginning, we chose a thickness of 20 nm for the platinum protection layer, which made us discover that thermal extensions are not negligible. The volumetric thermal expansion coefficient of gold of $42 \times 10^{-6}\,\mathrm{K}^{-1}$ is by more than a half higher than the coefficient of platinum of $27 \times 10^{-6}\,\mathrm{K}^{-1}$. The adhesion between the SiO_2 substrate surface and the palladium is very weak. Therefore, the temperature difference between evaporation process and room temperature caused enough strain between gold and platinum in the contact lines so that the latter came off during the lift-off process. Some tests showed that a platinum protection layer of 5 nm does not cause important strain effects by keeping reasonably low leakage currents ($\lesssim 1\,\mathrm{nA}$).

3.4.2 Border Effects of Photoresist on Diamond Substrates

The contact design on the diamonds was patterned by standard contact lithography, using the photoresist S1818. This resist has a high viscosity which results in border effects during spin coating. This effect is illustrated in Fig. 3.5(a), where a drawing of bare substrate and a photo of a substrate with photoresist after spin coating are shown. The thickness of the resist increases a lot on the border of the substrate and as the diamond substrates show rather a high border/surface ratio due to their small size, the part suitable for photo lithography is limited to the centre of the substrate. At the same time, enhanced thickness on the border prevents the lithography mask from touching the photoresist's surface. The result is a degradation in edge sharpness of the photoresist mask after development and consequently of the metal contact lines. Thus, the device geometry suffers from the strong border effects.

To overcome this problem, we designed a special spin coater support, together with Laurent Del-Rey, technician of the "pôle Ingénièrie Expérimentale" in the Néel institute. The working principle of the support is illustrated in Fig. 3.5(b) and our designed spin coater support is presented in three photos in Fig. 3.5(c). The diamond is placed in the centre, between two elbow fittings with exactly the same height as the substrate. One of the fittings is mobile and can be screwed in a position so that the substrate is squeezed in-between the two of them. Hence, the dispersion of the photoresist continues beyond the substrate's edges and the border effects are largely reduced. The third panel of 3.5(c) shows the support with a mounted diamond substrate after spin coating where the photoresist is spread over both the diamond's surface and the support's surface. Border effects were largely reduced.

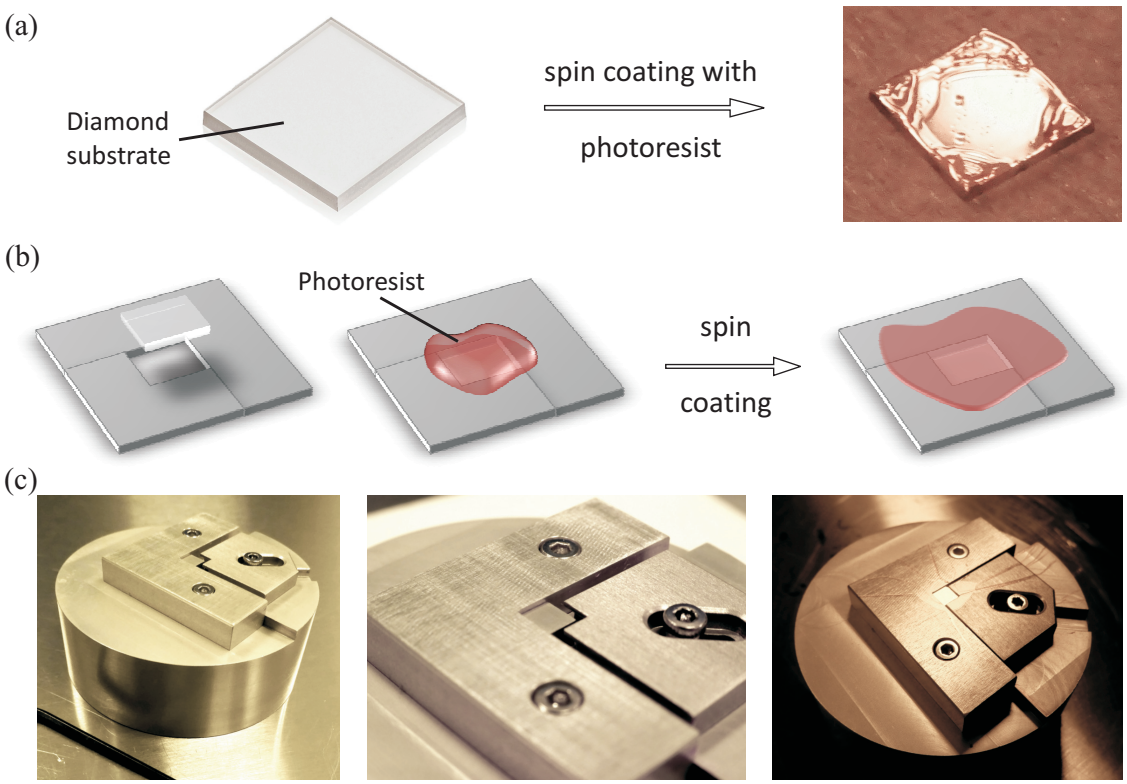

Figure 3.5: (a) Drawing of a diamond substrate and a photo of a substrate spin coated without any support. The photoresist's thickness will be enhanced on the edges of the diamond substrate. (b) Illustration of the spin coating with our designed support: border effects are largely reduced as the photoresist spreads beyond the substrate's edges. (c) Spin coater support to diminish the border effects. The third panel shows the support with a mounted diamond substrate just after the spin coating: the photoresist is spread over the surfaces of both diamond and support.

3.5 Conclusion

We developed a complete fabrication process to realise multi-walled WS_2 nanotube field-effect transistors with an ionic liquid topgate, from the nanotube powder to the finished device. This process includes the method used to provide a device with a small droplet of ionic liquid. In parallel, we fabricated EDL-gated TMDC thin film FETs, using the technique of mechanical exfoliation and else the same fabrication process developed for nanotubes. Additionally, we presented how we realised ohmic contacts in Hall bar geometry on an intrinsic diamond substrate. Finally, we demonstrated how we succeeded in overcoming two big issues we had to face during the development of fabrication processes.

CHAPTER 4

WS_2 Multi-Walled Nanotube FET

This chapter presents ambipolar field-effect transistors (FET) based on individual, intrinsic tungsten disulphide multi-walled nanotubes (WS_2 MWNTs), discussing their EDL-gate transfer and output characteristics. Due to its inorganic nature and for facilitation, we will refer to it as inorganic nanotube (INT). Such a tube as basis for our investigation is an indirect bandgap semiconductor possessing a bandgap of 1.27 eV [67]. FET properties such as mobility, I_{on}/I_{off} ratio and subthreshold slope will be discussed and evidence for metallic conduction at low temperature for high electron doping will be given. Furthermore, effects of gate sweep velocity and temperature on FET properties will be discussed as well as relaxation of the electrolyte. After investigation of more than 15 devices, we performed some statistics that enabled us to extract values for contact resistance and to discuss relations between extracted parameters, such as transport gap and diameter. We will compare the performance of an electrolyte-gated device with the performance of a standard Si/SiO_2 backgated device. Therefore, we will display two transistor transfer characteristics of the same INT, one using the liquid topgate and one using the solid backgate with a 285 nm SiO_2 layer as dielectric. Finally, we discuss the difficulty to perform correct four-terminal measurements on a nanotube.

Samples were glued and micro bonded on a chip and then mounted in a vacuum dip-stick with operating temperatures ranging from 4 K to 300 K. The dip-stick was pumped until a pressure of the order of 10^{-5} mbar was reached before being dropped into a liquid helium dewar. The 4 K environment ensures cryogenic vacuum, which is the adsorption of molecules like water, nitrogen and oxygen at the dip-stick's cover. This step is essential to withdraw those molecules from the electrolyte in order to significantly reduce gate leakage currents. Two-terminal measurements were performed with an Agilent B2902A source-measurement-unit or lockin-amplifier technique.

4.1 FET-Characteristic Properties of a WS_2 MWNT FET

We present systematic transport measurements performed on more than 20 WS_2 MWNTs with diameters of 25 nm to 100 nm. All measurements were taken in a two-probe configuration, shown schematically in Fig. 4.1(a), using either a standard lock-in technique or

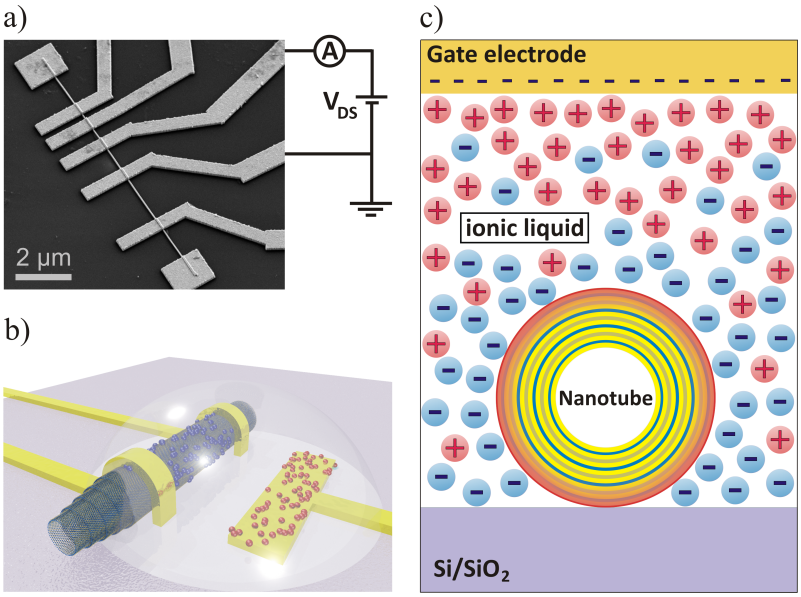

Figure 4.1: (a) Device JS102d. SEM image of a 12 µm WS_2 MWNT with a diameter of 50 nm. Five transport contacts were realised on the INT as well as two patches on each end of the tube to prevent liquid from flowing inside. (b) Simulated 3D schematic of a WS_2 MWNT device with two transport contacts and a counter electrode, all covered by ionic liquid. A negative voltage is applied to the counter pad. The simulation was done by Johann Coraux, Néel Institute, CNRS Grenoble. (c) Schematic drawing of a cross section through the device that shows the ionic liquid and the gated nanotube in the same gating situation as in (b), a negative V_g is applied, which leads to hole doping on the surface of the INT indicated in red.

a DC Source/Measure unit. V_g represents the voltage applied to the counter electrode and therefore to the electrolyte, which enables the formation of an EDL at the tube's surface. More details to the EDL-gating technique are given in section 1.2. This technique is particularly convenient in the case of a tube as it allows conformal doping all around the tube, as shown schematically in Fig. 4.1(b) and 4.1(c) in the case of hole doping. When performing measurements the leakage current I_g passing through the ionic liquid between source and gate electrode is measured at the same time. A two-probe configuration was chosen because of two reasons. Firstly, the intrinsic semiconducting INT is highly insulating even at room temperature and only becomes conducting when highly hole- or electron-doped. Most of the measurements were based on the transition of the nanotube from highly insulating to conducting, which means that for parts of the measurements, the INT's resistance is higher than the impedance of the measurement unit and in four-probe configuration, we would not measure the true values. Secondly, even when the tube is driven in the conducting regime, the fact of having a topgated device of tubular geometry and a tube-crossing contact design makes four-probe measurements useless. A detailed and illustrated explanation of this problem and a suggestion of a contact design suited for four-probe measurements is given at the end of this chapter in section 4.5.

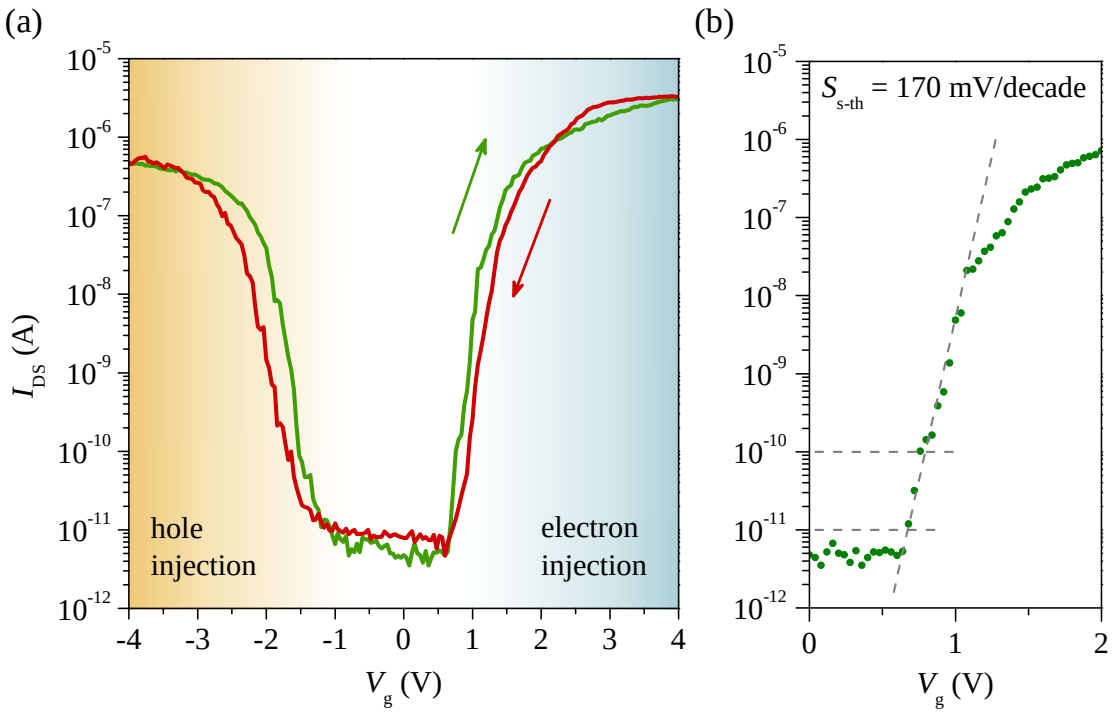

Figure 4.2: Device JS072d. (a) Drain-source current as a function of gate voltage of one INT with a diameter of 60 nm. Modulations of the current up to 5 orders of magnitude at the hole side and up to 6 orders of magnitude at the electron side are realised. The sweep was done in forward and backward direction at a bias voltage of 180 mV and at a temperature of 255 K. (b) Zoom into the forward sweep at electron injection. Dashed grey lines indicate the determination of the subthreshold swing: the gate voltage change needed to increase I_{DS} by one order of magnitude.

4.1.1 Gate Sweep

One of the most important results of this work is the ability to dope an individual WS_2 MWNT continuously from the valence to the conduction band by using EDL-gating, which leads to an ambipolar field-effect transistor. One representative field effect transfer characteristic obtained on a 60 nm thick tube is presented in Fig. 4.2(a). The drain-source current I_{DS} in logarithmic scale is shown as a function of V_g in forward and backward sweep directions at a bias voltage of 180 mV and a temperature of 255 K. The reversibility proves that doping is not likely the consequence of chemical reactions[1] or chemical doping of the nanotube. No hysteresis was observed, but as hysteresis effects are strongly dependent on the sweep velocity and the temperature, a detailed study is presented in 4.2.

The off-state of the transistor is defined as the state of very low current and therefore high resistance ranging from $V_g = -1.5$ V to 0.8 V. The current is in the range of pA, which is the noise ground of the measurement unit and corresponds to a tenth of GΩ. Later we will refer to this interval as the transport gap E_t. The on-states at higher positive and

1 Chemical reactions can occur between either the WS_2 or the metal electrodes and the ionic liquid at $V_g \gtrapprox 2.5$ V.

negative V_g values show significantly higher drain-source currents. The INT transistor in Fig. 4.2(a) exhibits excellent I_{on}/I_{off} ratios which reach values of up to 10^5 on the hole side and up to 10^6 on the electron side. This characteristic property depends on the bias voltage V_{DS} (see discussion in section 4.3.3 and Fig. A.5(c)) and is limited by sensitivity of the current measurement, the mentioned noise ground of the measurement unit. This last statement includes that the off-state currents I_{off} of all our devices are, with measured values ranging from 1.5 pA to 110 pA, extremely low, which is one of the required properties for FETs to operate with low static power dissipation. Any potential replacement of silicon in CMOS-like digital logic devices must have excellent switching capabilities, which are low I_{off} values and high I_{on}/I_{off} ratios of 4-7 orders of magnitude [124, 157, 170, 185], two conditions that are fulfilled in our devices. Note that the ionic liquid has its own inconveniences and limitations. Some, like electrochemical reactions with certain materials, have already been discussed in chapter 1, others will be discussed in the course of the chapter.

The transition between off- and on-state can be split up into two regions, the subthreshold region with an exponential current increase and the injection region where the current increases linearly. The V_g value separating these regimes is the threshold voltage V_{th} and is defined as the moment when the conduction (valence) band of the channel is approximately aligned with the Fermi energy E_F of the source electrode in the case of electron (hole) doping [11]. In other words, V_{th} indicates the moment when charge carriers start to be injected in the INT. Both regions will be discussed in detail in the following sections.

4.1.2 Subthreshold Swing

The subthreshold region describes the V_g range just below V_{th}, where the surface is very weakly doped. In this region in a standard FET, e. g. a MOSFET, I_{DS} is determined by thermal activation, $I_{DS} \propto \exp(1/k_B T)$. The inverse of this so-called subthreshold slope is another characteristic parameter of a FET, the subthreshold swing $S_{s\text{-}th}$ which is the gate voltage change needed to increase I_{DS} by one order of magnitude. In [207] and [211] it is shown that

$$S_{s\text{-}th} = \frac{dV_g}{d\log_{10}(I_{DS})} = \ln(10)\frac{dV_g}{d(\psi)}\frac{d(\psi)}{dI_{DS}} \approx \ln(10)\left(1+\frac{C_d}{C_g}\right)\frac{k_B T}{e} \xrightarrow{C_g \gg C_d} \ln(10)\frac{k_B T}{e},$$

with ψ being the surface potential with respect to the bulk[1] and C_d and C_g being the capacitances of the channel material and the gate insulator respectively. Therefore the lowest theoretical limit at room temperature is 60 mV/decade and at 250 K, the temperature at which we usually performed our measurements, it is 50 mV/decade. The exponential increase of I_{DS} with I_g is visible in Fig. 4.2(b). The forward sweep of (a) on the electron side with dashed lines as guides for the eyes, indicating the linear range and one decade of

1 In other words ψ stands for the band bending and is for example positive for downwards bending.

current change. In this sample, JS072d, the subthreshold swing is about 170 mV/decade, in other samples we obtained values down to 80 mV/decade for electron doping and 110 mV/decade for hole doping. On average, we observed rather higher subthreshold slopes of ≈200 mV/decade for electron doping and ≈400 mV/decade for hole doping.

The subthreshold swing is one of the key parameters to keep power consumption low and is therefore essential for the ongoing miniaturisation of transistors [95, 186]. Smaller subthreshold swings and therefore steeper subthreshold slopes lead to smaller threshold voltages due to the relation $V_{\text{th}} = S_{\text{s-th}} \cdot I_{\text{on}}/I_{\text{off}}$ [186]. So far, transistor performance has been improved by the reduction of gate oxide thickness, which leads to an increase in the capacitance between channel and gate [81]. However, the reduction of the dielectric thickness increases tunnelling through the gate-insulator, the so-called gate leakage. As miniaturisation stands at the same time for channel length reduction, short-channel-effects are adding up and, all in all, downsizing of FET devices leads to increased off-currents and subthreshold swings and to lower $I_{\text{on}}/I_{\text{off}}$ ratios [211].

The case of an only T-dependent $S_{\text{s-th}}$ described before is true for FETs with ohmic contacts between electrodes and channel[1]. After investigation of many devices under different conditions we observed no striking temperature dependence, but a very slight V_{DS} dependence of $S_{\text{s-th}}$ on the hole side (more detail are given in A.3). This indicates Schottky barriers at the contacts rather than ohmic contacts [11]. In our case the Pd contacts were just deposited on the semiconducting INT without any preceding or subsequent treatment. Therefore, it is likely that we have Schottky barriers at the semiconductor/metal interface and the physics behind the subthreshold swing is no longer the same. Fig. 4.3 is an illustration of the band bending for different gate-source and drain-source voltages applied in the case of Schottky barriers for hole injection. Panel (a) and (b) show the equilibrium

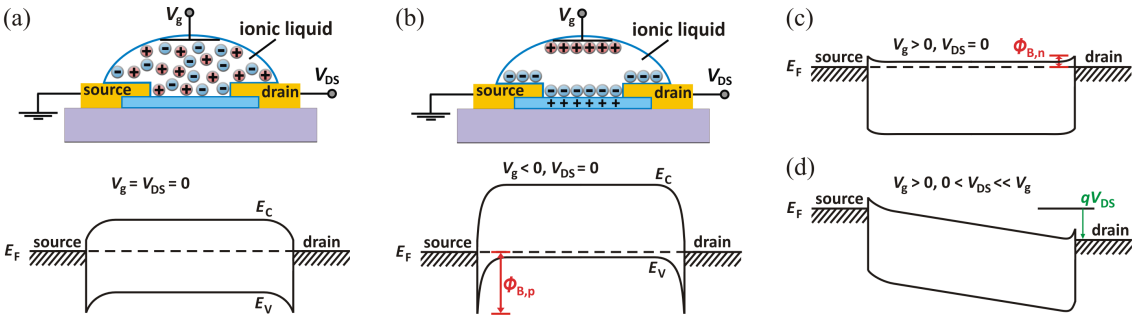

Figure 4.3: FET device with Schottky barriers for hole injection. (a), (b) Cross section of a device and corresponding band diagram along the WS_2 MWNT surface, where (a) displays the situation in equilibrium and (b) with a negative gate voltage applied. (c), (d) Band diagrams of the transistor under positive gate bias and with $V_{\text{DS}} = 0$ V and $V_{\text{DS}} > 0$ V applied respectively. $\Phi_{\text{B,p}}$ and $\Phi_{\text{B,n}}$ label the Schottky barriers heights for p- and n-type charge carrier injection respectively. Band diagrams are drawn after [207].

1 Ohmic contacts can be achieved for instance by local doping underneath the contacts [249], by choosing contact materials with work functions matching with those of the channel material [229], by annealing (e.g. CNTs [133, 243]) or by an additional double gate on the channel/metal interfaces [143].

case and the case of a negative gate voltage applied. The latter modulates the band structure of the INT in a way so that the Schottky barrier width decreases with increasing V_g. Panel (c) and (d) illustrate the case of a positive gate voltage applied and with $V_{DS} = 0\,V$ and $V_{DS} > 0\,V$ applied respectively. In the drawn case, the Schottky barrier for electron doping is negligibly small.

In the subthreshold region, the source-drain current is a tunnelling current through the Schottky barriers[1]. As illustrated in Fig. 4.3, a gate bias shifts the bands and therefore decreases the barrier width. Consequently, I_{DS} increases exponentially with increasing V_g due to the exponential sensitivity of a tunnelling current on the barrier width. As $S_{s\text{-}th}$ reflects the decrease of Schottky barrier widths, it is no longer T-dependent, but is supposed to depend on the dielectric thickness and slightly on the drain-source field V_{DS}.

Our lowest $S_{s\text{-}th}$ values obtained are higher than the theoretical lower limit of 50 mV/decade at 250 K, but still very low and comparable to values obtained for carbon nanotubes (CNT) with a high-κ-dielectric in top-gated geometry [95] or EDL-gated CNTs [122, 200] (all about 70-100 mV/decade). At the same time, these values are much lower than values obtained for CNT transistors with a standard Silicon backgate where $S_{s\text{-}th} \approx 1\,V$/decade [95, 122] and only slightly higher than the best value for a scaled MOSFET at room temperature. Such low subthreshold swings indicate efficient gating due to good gate-channel coupling, which means very few trapped states or impurities on the electrolyte/INT interface [11, 24, 81, 95].

4.1.3 Mobility

At the threshold voltage for charge injection V_{th}[2], the current versus V_g turns from exponential increasing into linear increasing, as discussed in section 4.1.1. The carrier mobility μ is directly proportional to the resulting slope of the linear regime. To explain this, we start from the relation $\sigma = \mu n e$, with σ being the conductivity and e the electron's charge. The charge carrier density is given by $n = C(V_g - V_{th})/e$, where C is the capacitance

1 Even if low resistive metal-semiconductor contacts are very important for good device performance, a newer type of transistor uses the tunnelling effect in an advantageous way to create tunnelling field-effect transistors (TFET) where the subthreshold swing is no longer limited by temperature [123, 186]. The IBM group was the first to demonstrate subthreshold swings below the MOSFET limit as they obtain $S_{s\text{-}th}$ values as low as 40 mV/decade in a CNT-TFET [12]. Short-channel-effects will limit the performance of MOSFETs when the down-scaling of devices continues to ever smaller dimensions and a lower limit of the subthreshold swing cuts off the path to lower system power. Therefore, a tunnelling field-effect transistor is a promising alternative and as transition metal dichalcogenides are supposed to be good candidates for high quality TFETs [68, 96], WS_2 MWNTs offer a high quality nano-scale alternative to currently used FETs [14, 211].

2 In the case of Schottky barriers at the semiconductor/metal interface, at V_{th} the barrier heights are then significantly reduced and a further increase of V_g will no longer have a strong impact on the barrier heights.

of the dielectric. Therefore, the mobility is given by [53, 184]

$$\mu = \frac{1}{C}\frac{L}{W}\frac{G}{(V_g - V_{th})} \ . \tag{4.1}$$

In a 2-dimensional electron gas (2DEG), the conductivity is given as $\sigma = G \cdot \mathrm{L/W}$, where G is the conductance and L and W are the channel's length and width respectively. In the case of single-walled CNTs of diameter $d \leq 1.5\,\mathrm{nm}$ [37, 61], the channel width is not taken into account and the conductivity results as $\sigma = G\mathrm{L}$. In our case, we have rather thick multi-walled INTs, where even the thinnest with a diameter of 25 nm is thick compared to a single-walled CNT. Additionally, the use of an ionic liquid, a gate dielectric which covers the nanotube's whole surface, implements conformal doping and hence the creation of a conduction channel on the whole WS_2 MWNT's surface. Thus, instead of a uni-dimensional capacitor, one should consider a planar geometry in which the INT is unzipped, as illustrated in Fig. 4.4(a). Finally, we can model our system as a nanoribbon with a planar gate and the surface $2\pi r_{INT} L$, with r_{INT} being the INT radius. We will use the sheet conductance $G_\square$ in order to calculate mobility[1].

In Eq. (4.1) the threshold voltage V_{th} appears, which is a parameter hard to define unambiguously. To compare device properties of FETs, it is therefore reasonable to use

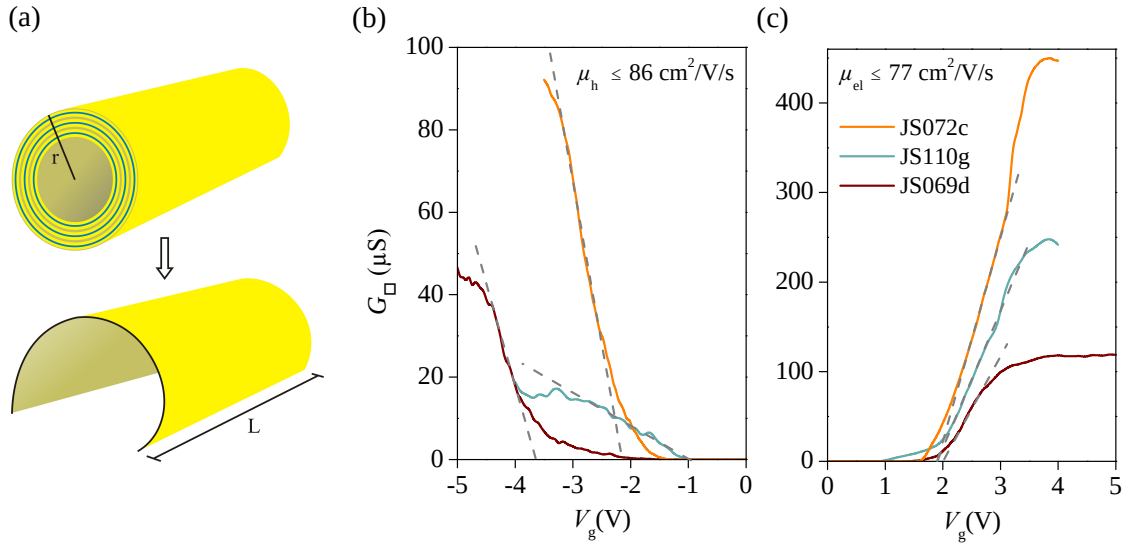

Figure 4.4: (a) Illustration of the unzipping of a WS_2 MWNT. We consider it as a planar capacitor with the surface $2\pi r_{INT} L$, with r_{INT} being the INT radius and L being the channel's length. (b), (c) Sheet conductance versus EDL-gate voltage in linear scale on the hole and electron side respectively. Dashed lines as guides for the eyes indicate the slopes used to calculate mobility. Note that the maximum values of conductance are four times higher on the electron side.

1 In the case of a 2DEG, the sheet conductance is the conductivity.

the so-called field-effect mobility μ_{FE} [53, 184], which is given as

$$\mu_{FE} = \frac{1}{C_{IL}} \frac{dG_{\square}}{dV_g} \ . \tag{4.2}$$

The value of the capacitance C_{IL} per unit area of our ionic liquid [EMIm][TFSI] is based on the Hall measurements done on exfoliated WS_2 flakes[1] and presented in appendix A.2.2. The resulting capacitance values are 0.8 and 3 µF cm^{-2} for hole and electron doping respectively.

Fig. 4.4 shows the square conductance $G_{\square}$ as a function of V_g in linear scale for three different devices. Clear linear regimes, indicated by dashed lines as a guide for the eyes, denote constant derivatives $dG_{\square}/dV_g$ over a certain V_g interval. These slopes are the values to be used for the calculation of the field-effect mobilities in Eq.(4.2). The resulting hole mobilities μ_h and electron mobilities μ_{el} are displayed in table 4.1.

Mobility determines the carrier or drift velocity via $v_d = \mu E_{DS}$, with E_{DS} being the electric field between drain and source in V/m, and hence switching speed, in FETs. In our way of calculation, this is reflected by the steepness of the slope as a higher mobility is equal to a steeper slope and therefore stands for faster transistor switching from *off* to *on*. High speed is crucial for a lot of applications, such as high-speed FETs and memory devices [53]. At the same time, high mobility stands for low power consumption, as it can be translated into the so-called overdrive voltage which is the gate voltage difference between on-state and threshold $V_{on} - V_{th}$. The higher the mobility, the steeper the slope, the smaller the overdrive voltage, the lower the supply voltage of operation.

In our devices, both electron and hole mobilities reach values up to 80 cm^2 V^{-1} s^{-1}, which exceeds the highest value reported so far in backgated WS_2 nanotube FETs of 50 cm^2 V^{-1} s^{-1} [115] by more than a half. Our mobilities are of the same order of magnitude as lately reported values for WS_2 thin film FETs [30, 156]. Compared to the mobilities in the first ambipolar transistor based on a network of electrolyte-gated WS_2 MWNTs ($\leq$3.6 cm^2 V^{-1} s^{-1}), our mobility values are by two to three orders of magnitude higher for electrons and holes respectively than the reported values [205]. Even high-κ dielectrics, which lead to field-effect

Table 4.1: Field-effect hole and electron mobilities of the three devices shown in Fig. 4.14.

sample	μ_h (cm^2 V^{-1} s^{-1})	μ_{el} (cm^2 V^{-1} s^{-1})
JS072c (orange)	86	77
JS110g (blue-green)	15	43
JS069d (red)	77	26

1 The capacitance of an ionic liquid is frequency- and material-dependent. Therefore, only Hall measurements on the same crystal (in its flat appearance) and by using the same setup can give us a truthful value for further calculations.

mobilities $>1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ in MoS_2 monolayers [113], did not lead to mobilities in WS_2 monolayers higher than $83\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ [46].

Let us compare our values to the highest mobilities reported so far for other types of TMDC crystal flakes. In EDL-gated field-effect transistors, hole mobilities of up to $\approx 1800\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ were reported for WSe_2 trilayers [247] and electron mobilities up to $\approx 100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ were reported for MoS_2 few-layers [161]. Those enhanced values reflect the non-negligible higher focus that was put on MoS_2 and WSe_2 so far compared to WS_2, rather than intrinsic material properties. Mobility in TMDC few-layer flakes is phonon-limited as a result of its low effective mass. Calculations predict a room-temperature electron mobility higher than $1000\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for WS_2 monolayers, which is the highest among semiconducting TMDCs.

In practice, mobility and therefore device performance is limited by scattering with intrinsic sources, such as charged impurities or defects, and by scattering with surface-optical phonons. In semiconducting TMDCs, low mobilities were due to the presence of Schottky barriers at the channel/metal interfaces [110]. Our high two-terminal mobilities indicate very good electrostatic coupling between the INT surface and the electrolyte, which results from very clean and high quality WS_2 MWNTs and therefore from few trapped states. At the same time, this is in agreement with the picture of reduced Schottky barriers and therefore contact resistances due to the EDL-gating technique used, as discussed in 1.2.3.

4.1.4 Transistor Output Characteristics

The asymmetry observed between electron and hole doping is reflected in the current-voltage characteristics. Fig. 4.5(a) and 4.5(b) show I_{DS} versus V_{DS} of a 45 nm thick INT at different values of V_{g} for hole and electron side respectively. Let us first have a look at the characteristics for electron doping. Fig. 4.5(b) is split into three regions which are illustrated in Fig. 4.5(c): in four panels, the cross section along the tube's axis of an electrolyte-gated nanotube device is drawn schematically to explain the injection regimes I, II and III, together with the equilibrium case of $V_{\mathrm{g}} = V_{\mathrm{DS}} = 0\,\mathrm{V}$, where cations and anions are mixed.

Regions I and II display typical FET output characteristics. Region I is the linear, ohmic regime, where the gate voltage exceeds the source-drain voltage strongly and the whole n-type conduction channel is built up. Region II is the saturation regime which indicates the pinch-off of the conduction channel. In the case of an ionic liquid topgate, the pinch-off is due to the interplay between the two electric potentials drain-source and gate-source. Under a constant gate bias, V_{DS} can be increased so far that cations start to be repelled from the drain electrode. It starts when V_{DS} reaches the value for saturation

$$V_{\mathrm{DS,\,sat}} = V_{\mathrm{g}} - V_{\mathrm{th}}\ , \tag{4.3}$$

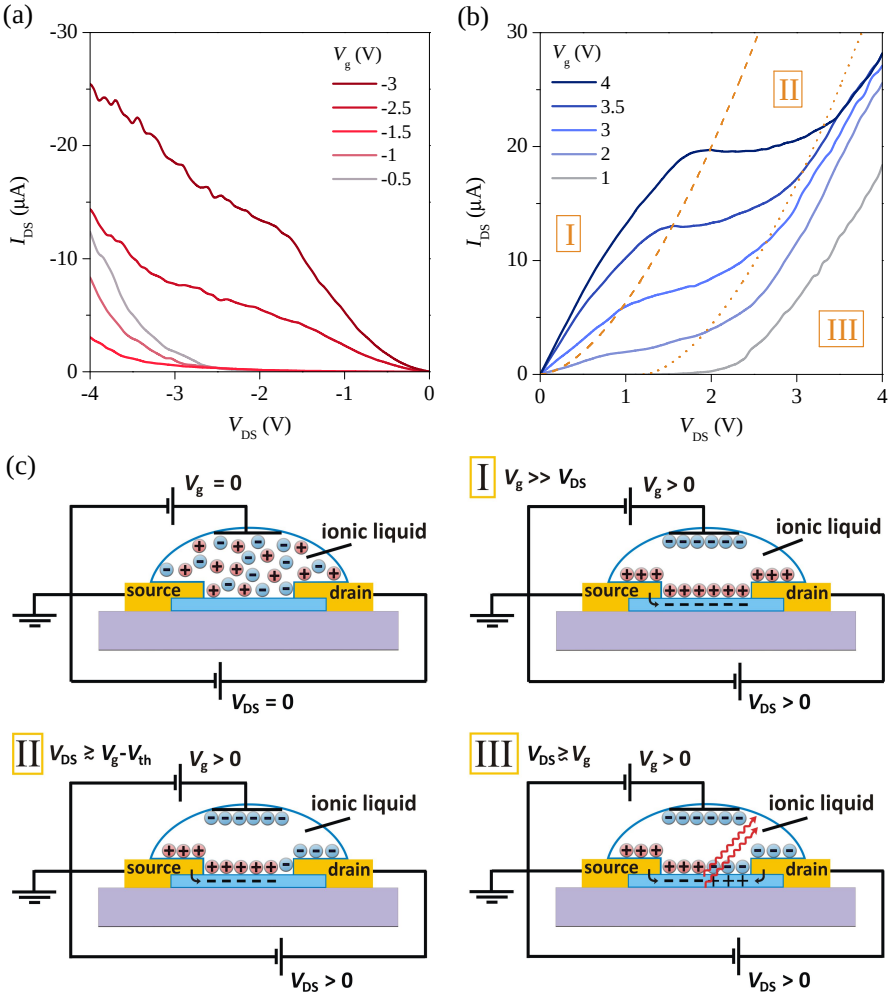

Figure 4.5: Device JS099a. I_{DS} versus V_{DS} of a 35 nm INT at different (a) negative and (b) positive V_g values. We observe standard transistor behaviour for high positive and negative gate voltages (region I and II in (b)), whereas the influence of the Schottky barrier on the hole side results as convex current increase at low voltage bias. At low V_g and high V_{DS} the current experiences a steep increase, which indicates that the INT enters into a regime of simultaneous electron-hole injection (region III). (c) Schematic drawings of the EDL-gated INT in the equilibrium case and the three regions I-III indicated in (a).

indicated by a dashed curve in the figure[1]. The drawing of region II shows this effect, the accumulation of anions on the drain electrode and an interruption (pinch-off) of the electron-doped channel, starting from the metal contact.

In contrast to a standard FET, there is a third regime when using an electrolyte as gate dielectric. Instead of a continuing pinch-off with a further increase of the drain-source voltage, the effect of anion accumulation on the drain electrode will eventually lead to a hole injection from the very same contact, as it is illustrated in the schema for regime III. Consequently, n-type carriers injected from the source and p-type carriers injected from the drain will meet in the channel, which means that a pn-junction is established in the

1 The dashed line in Fig. 4.5(b) is a power law fit of the I_{DS} - $V_{DS,\,sat}$ pairs.

nanotube. On the junction, electrons and holes will recombine[1] causing a current increase, which is clearly visible in region III in Fig. 4.5(b). Note that this effect is only possible in the case of an ambipolar FET where a simultaneous injection of electrons and holes into the channel is possible [135].

The start of the third regime is indicated in Fig. 4.5(b) as a dotted line. We observed that the pinch-off regime lasts only over a gate voltage interval of about 0.75 V, as taking the dashed line and shifting it by this value to the right coincided very precisely with the current increase due to electron-hole recombinations. Similar measurements done on other devices have shown that this shift is either equal or superior to the threshold gate voltage for charge injection V_{th}[2]. Therefore, using the theory for the start of the pinch-off Eq. (4.3), the hole injection from the drain electrode begins when $V_{\mathrm{DS}} \geq V_{\mathrm{g}}$. Despite the fact that WS_2 is an indirect bandgap semiconductor at the temperature of 250 K, where the measurements were performed, there is a possibility of radiative recombinations, indicated as wavy red arrows in the drawing.

The output characteristics for hole doping differ from those of electron doping in several points. First of all, they are not ohmic at low negative I_{DS}, but exhibit nonlinear, upward turning behaviour, which is very clearly visible for $V_{\mathrm{g}} = -2.5$ and -3 V in Fig. 4.5(a). This indicates Schottky barriers at the contacts rather than ohmic contacts and has already been seen in various groups [84, 135, 161]. At the same time, the pinch-off plateaux are much less pronounced and current continues to increase. Especially for low negative ionic liquid-gate voltages the current increases significantly at $V_{\mathrm{DS}} < -3$ V. This again suggests electron-hole recombination and indicates that a pn-junction is created as in the case of electron doping.

In both cases, the electron-hole recombination may be a radiative one. For instance, light emission has already been seen in the case of WS_2 mono- and bilayers [99]. Indeed, we observed that a portion of the electron-hole pairs recombine radiatively. An ambipolar WS_2 MWNT FET operated as light-emitting transistor and its output characteristics will be discussed in detail in chapter 5.

4.1.5 Metallic Conduction at low Temperatures

The high electron doping evokes a transition to metallic conduction. Fig. 4.6(a) and 4.6(b) show the sheet resistance versus temperature for different negative and positive gate voltages respectively done in two-probe configuration. The inset of Fig. 4.6(b) indicates the doping level for each resistance versus temperature curve. It shows the corresponding

1 In this pn-junction, which does not originate from irreversibly p- and n-doped zones, there is no space charge region or depletion layer at the interface between p and n. Therefore no threshold bias voltage is needed to enable recombination.

2 For instance, in this device, the shift coincides exactly with V_{th}, but statistics which can lead to a final conclusion are still missing.

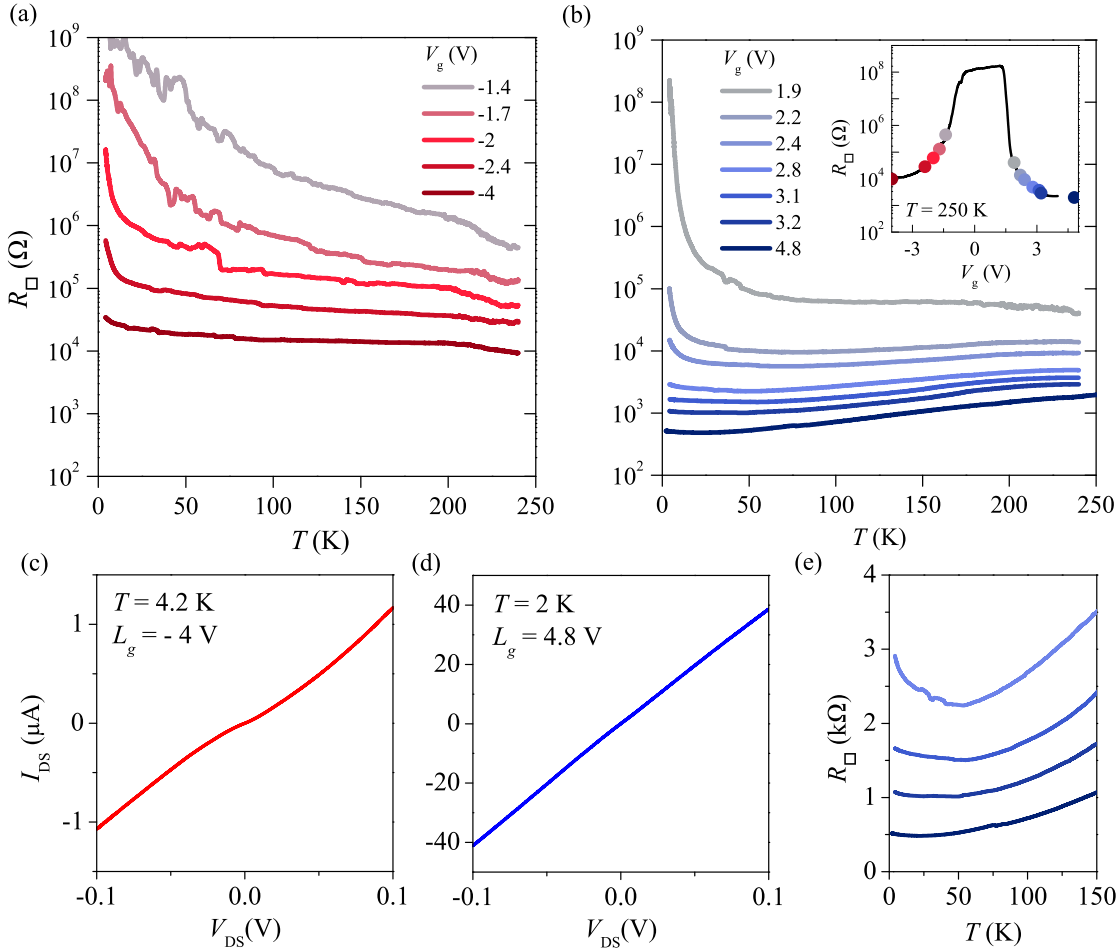

Figure 4.6: Device JS072c. (a), (b) resistance versus temperature at different V_g values applied, ranging from −1.4 volts to −4 volts on the hole and from 1.9 volts to 4.8 volts on the electron side. The inset shows the resistance versus V_g at 250 K with the 250 K-sheet-resistance values from the resistance versus temperature measurements indicated as circles. (c), (d) Current-voltage characteristics at lowest temperatures measured and at highest hole and electron doping respectively. The curve for hole doping shows a small plateau around $V_g = 0$ V, which indicates insulating behaviour, whereas for electron doping the characteristic is strictly ohmic. (e) resistance versus temperature plots for high electron doping in linear scale. The weak localisation upturn at low temperatures is visible.

$R_\square - V_g$ data pairs as dots in the corresponding colours on a gate characteristic for the same INT. Regarding the electron side, resistance is decreasing with decreasing temperature for $V_g \geq 2.4$ V (corresponding to 250 K-sheet-resistance values ≤ 20 kΩ), which demonstrates the presence of metallic conduction. Only at temperatures below 50 K the resistance increases slightly even in the case of high doping. Fig. 4.6(e) shows the four least resistive curves in linear range to visualise this upturn which is less pronounced the higher the doping level. We will show later in this chapter that this resistance increase at low temperatures is due to disorder-induced weak localisation effects at high doping levels and turns into strong localisation at low doping levels. This crossover underlines the field-effect-driven transition from an insulating into a metallic state.

The situation on the hole side is different as the resistance in general is by 1-2 orders of magnitude higher than on the electron side even at high negative V_g values and no metallic behaviour was found. This is directly reflected in the transistor output characteristics taken at highest doping levels and lowest temperatures measured for hole and electron side, which are presented in Fig. 4.6(c) and (d) respectively. The characteristic of hole doping is flattened at low V_{DS} in the $\pm 15\,\mathrm{mV}$ range. This small plateau around zero bias which is a characteristic of insulating behaviour. The current-voltage characteristic for electron doping, however, shows perfect ohmic behaviour giving a resistance value of $2.5\,\mathrm{k\Omega}$.

Weak Localisation

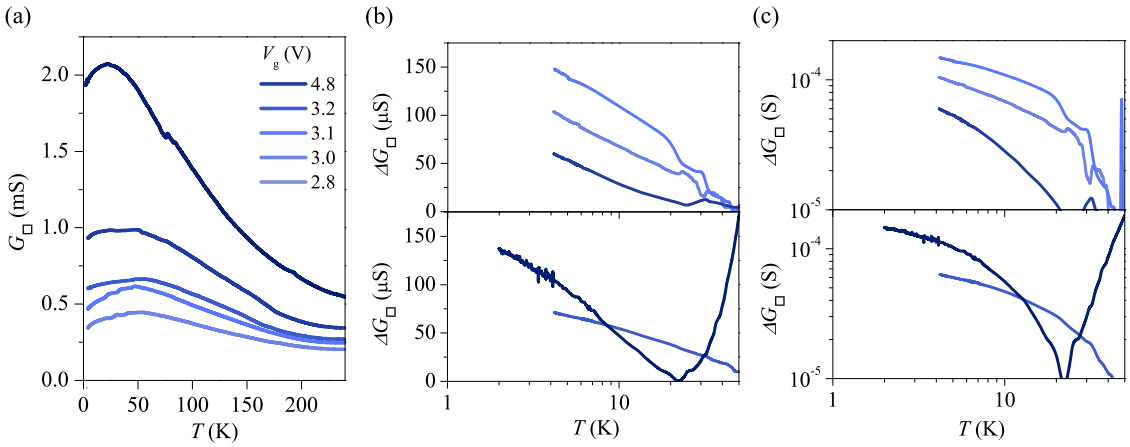

Figure 4.7: Device JS072c. (a) Sheet conductance as a function of temperature for high doping levels ($V_g \geq 2.8\,\mathrm{V}$). (b), (c) Normalised sheet conductance $\Delta\sigma = \sigma_0 - \sigma$ versus temperature of the same data in semi- and double-logarithmic scales respectively.

An increase in resistance at low temperatures is due to weak localisation: even at weakest disorder, impurities influence the electrons' motion due to quantum interferences between electronic wave functions, which leads to their localisation. This low-temperature quantum effect implies that no metallic state can exist in two dimensions at $T = 0$ [1]. As charge localisation and therefore the system's conductivity depends on dimension, the investigation of the weak localisation upturn will give information about the nature of our INT conduction channel. For a two-dimensional system, the quantum correction to conductivity $\Delta\sigma = \sigma_0 - \sigma$ depends on T via $\Delta\sigma \propto \ln(T\tau)$, with τ being the electron phase- relaxation time, whereas in a three-dimensional system, the relation is $\Delta\sigma \propto T^{3/2}$ [7].

Fig. 4.7(a) shows sheet conductance as a function of temperature for positive gate voltages $V_g \geq 2.8\,\mathrm{V}$ (presented in Fig. 4.6). The values of σ_0 are the peak conductances. Fig. 4.7(b) and (c) show $\Delta\sigma$ versus temperature in semi-logarithmic and logarithmic scales respectively. A linear or very close to linear behaviour at low temperatures is given for all semi-logarithmic plots, whereas the logarithmic plots all show a clear deviation from linear behaviour. Consequently, $\Delta\sigma \propto \ln T$, which shows that the conduction channel on the surface of our WS_2 MWNTs is two-dimensional, as expected, given the large diameters of the nanotubes. At the same time, this confirms the statement of Brumme *et al.*, that

90% of the charge carriers accumulated in TMDC crystals by EDL-gating are distributed in the first two crystal layers [31].

Activation

We now turn our attention to the semi-conducting behaviour of the temperature-based evolution of resistance at moderate and low doping. Fig. 4.8(a) and (b) display Arrhenius plots for the sheet resistance on the hole and electron side respectively. We clearly see activated behaviour for both doping regimes, indicating that the INT is insulating at these doping levels. At lowest hole-doing levels the measurement became very noisy at low temperatures so that activation energies T_0 were extracted from the slopes at higher temperatures. T_0 varies between 2 K and 260 K. Fig. 4.8(c) shows all extracted activation energies versus the absolute value of $V_g - V_{th}$ in semi-logarithmic scale and in linear scale (inset). Astonishingly, instead of the linear relation we expected, we noticed an exponential behaviour which we fitted, using $T_0 = T_0^* exp(A|V_g - V_{th}|)$ (black line in graph). This strongly suggests that there is an additional effect on resistance which might stem from the contact resistances as all measurements were done in two-probe configuration. If there are Schottky barriers present, charge injection happens via tunnelling through these barriers. Tunnelling current exponentially depends on the barriers' widths which depend on V_g. Barriers affect the resistance and with it the slopes in the Arrhenius plots. Therefore, the exponential dependence of T_0 on V_g might reflect the thinning of Schottky barriers.

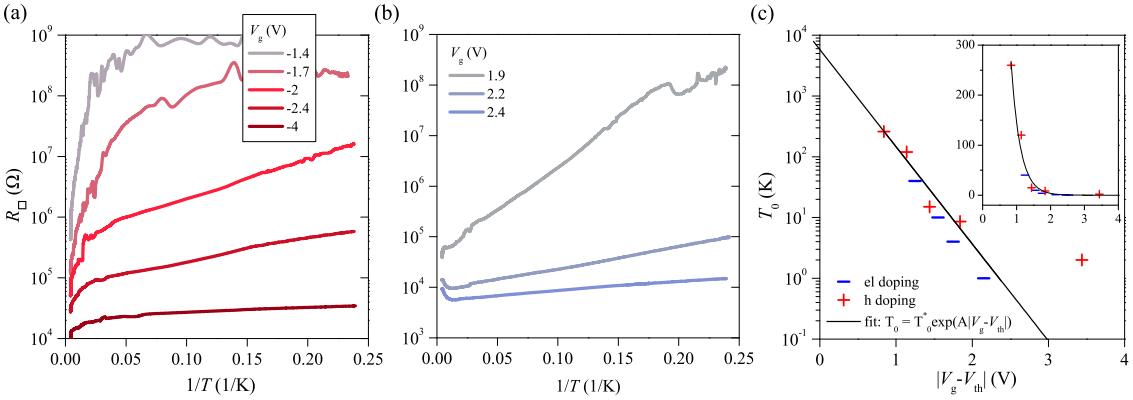

Figure 4.8: (a), (b) Arrhenius plots of the curves shown in Fig. 4.6 for hole and electron doping respectively. The existence of a linear regime for each doping level shows that thermal activation is present. (c) Activation temperatures T_0 extracted from Arrhenius fitting versus absolute value of the liquid gate voltage in semi-logarithmic scale and linear scale (inset). The activation energy decreases exponentially with increasing doping level instead of linearly. This suggests an additional effect due to Schottky barriers.

4.2 Ionic Liquid Stabilisation

It was mentioned above that hysteresis effects strongly depend on sweep velocity and temperature. This is due to the slow motion of the ions. When a certain liquid gate voltage is applied, the ions pass from a disordered state into a more highly ordered formation to build up the EDL on the device's surface.

Liquid ions have an average diameter of $\approx 2\,\mathrm{nm}$, which is rather big, and their long polymer chains create some viscosity. The additional absence of solvent might further decrease their diffusion. Even if those parameters are unknown, the resulting dynamics are visible in the experiments as characteristic time interval needed to re-establish a stable ion-formation on the ionic liquid/sample interface when the gate voltage was changed. In the following, two different approaches to study the importance of ionic liquid relaxation time will be discussed. Furthermore, we will show a study of device performance with respect to temperature.

4.2.1 Leakage Current Relaxation

A good way to study and visualise the time scale of ions' motion consists in monitoring the relaxation of leakage current I_g after a change of V_g. We therefore performed the following process at seven different temperatures: apply $V_g = 3\,\mathrm{V}$, wait 15 min, apply $V_g = 3.5\,\mathrm{V}$ and measure I_g versus time. The result is a power law relaxation for short times (up to $\approx$1000 s), which is shown in Fig. 4.9(a) where I_g is plotted as a function of time in logarithmic scale. The power law fits are displayed in green, whereas dash-dotted lines are

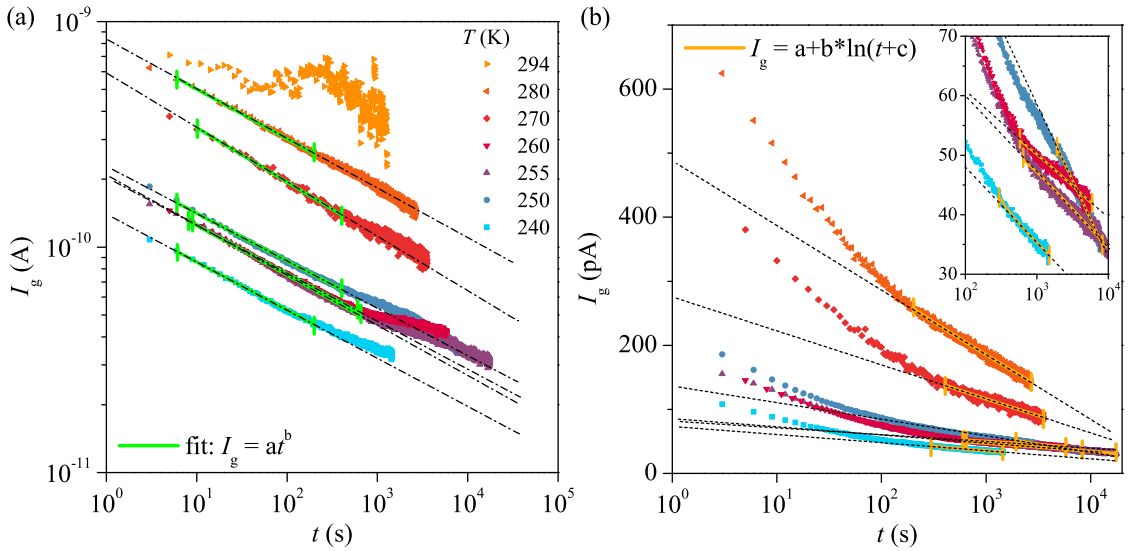

Figure 4.9: Device JS072d: (a), (b) I_g versus time for different temperatures after the application of 3.5 V in double- and semi-logarithmic scales respectively. The inset shows a zoom on the four lowest temperatures. From 0 s to 500-1000 s a power law is fitting the data best, but after longer waiting times we find a logarithmic decay. Power law and logarithmic fits are displayed in green (left) and orange (right) respectively. Dashed lines were added as guides for the eyes.

added as guides for the eyes to emphasise the fits. The room T data was not fitted, as it is too noisy to get an informative relation. Resulting exponents range from -0.21 for the lowest temperature of 240 K to -0.26 at room T. Deviation from straight lines and therefore from the power law behaviour are visible for longer relaxation times. Exponents < 1 suggest damped relaxation and therefore logarithmic behaviour rather than power. Fig. 4.9(b) shows the data in semi-logarithmic scale, the inset shows a zoom into the low temperature data. We observe a logarithmic relaxation for $t > 1000$ s. Logarithmic fits are displayed in orange and again dashed lines were added as guides for the eyes. A very clear deviation from logarithmic behaviour is visible for short times. The conversion from power law to logarithmic decay suggests inhomogeneous relaxation, which is faster at the beginning and starts to slow down after about 500 s. With a rough estimation for the saturation current $I_0 := I_g(t = \infty)$ half-value times were extracted to be in the order of tenth of seconds.

The time scales important for measurement performance cannot be extracted from these data. Further discussions will follow after the study presented in section 4.2.2.

In order to investigate the relaxation in terms of temperature, we will take a closer look at the slopes of the fits. The result is the same for both short and long relaxation times: the slopes increase with increasing T, which indicates that liquid stabilisation is faster at higher temperatures. At the same time, the absolute value of I_g was observed to increase at higher temperatures. For instance, when $T \leq 260$ K I_g depends only slightly on T, whereas I_g doubles when passing from 260 K to 270 K and ends up being by one order of magnitude

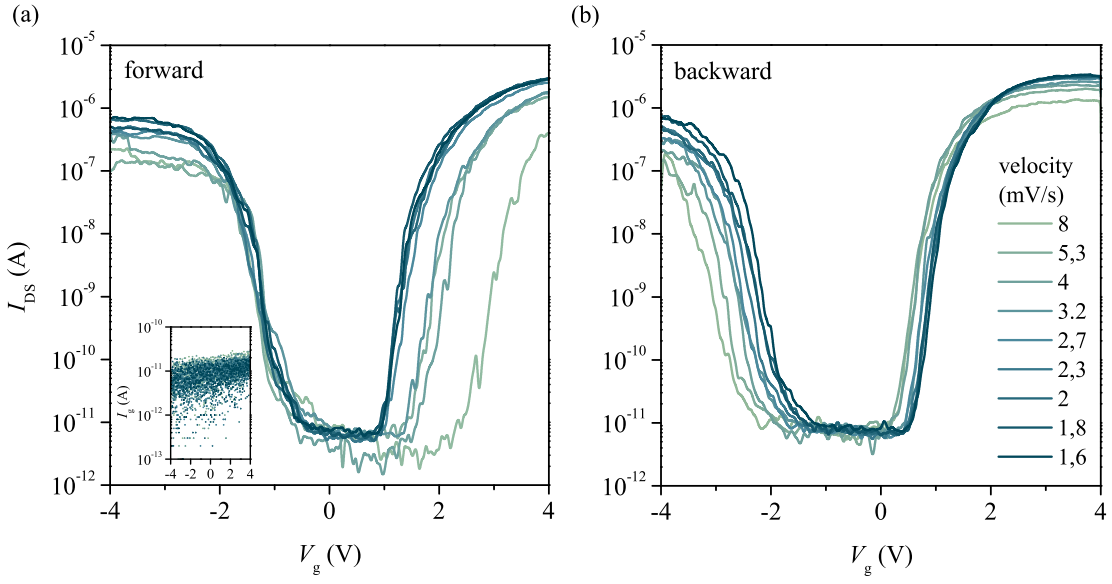

Figure 4.10: Device JS072d: Transfer characteristics in forward (a) and backward (b) sweep direction measured at 250 K with different sweep velocities. When the speed is decreased the transport gap decreases and gets more centred around $V_g = 0$ especially in forward sweep direction. The inset shows the leakage current as a function of V_g for all measurements. It is negligibly small even for high gate voltages applied.

higher at room temperature. A small value for the stabilisation time of the ionic liquid is favourable and the leakage current should also be kept as small as possible because it influences the quality of the measurement. Those are two counteracting processes, as the first decreases with T while the second increases with T and a good compromise has to be found. In this work, most measurements were done at T =250 K to keep I_g very small (in the order of some tenth of pA). Further discussions of temperature effects will follow in section 4.2.3.

4.2.2 Effects of gate sweep velocity

Let us now investigate and discuss the importance of measurement speed in order to limit hysteresis effects. To investigate hysteresis we performed liquid gate sweeps on the WS_2 MWNT presented in Fig. 4.2(a) at a fixed temperature of 250 K and with different sweep velocities. Fig. 4.10(a) and (b) show the measurements in forward and backward sweep direction respectively. The inset shows the leakage current that was measured between drain and gate electrode during the gate sweeps. It is $\approx$ 10 pA which is only slightly superior to the noise ground of the measurement unit for the whole V_g range. Thus, I_g won't influence the measurement's quality.

The modulation of sweep velocity was done by a change of the time delay per data point where the highest velocity of 8 mV s^{-1} corresponds to a delay of 5 s and the lowest speed of 1.6 mV s^{-1} is a delay of 25 s between points (separated by ΔV_g = 0.04 V). The first observations are the decrease of noise level when the sweep velocity was slowed down and the change of the transport gap E_t. The latter becomes better defined and narrower and gets more and more centred around $V_g = 0$.

Other parameters that help to characterise the quality of the gate sweep in terms of speed velocity like mobility are not directly visible in the graph. Therefore, we carefully extracted and compared all characteristic parameters discussed in section 4.1 and the result of this study is shown in Fig. 4.11. Sheet resistance values at the saturation $R_{\square,\mathrm{sat}}$ and mobilities as a function of sweep delay are shown for hole doping in (a) and (b) and for electron doping in (d) and (e), each time for forward and backward sweep direction. A criterion was found to define hysteresis, the V_g range between forward and backward sweep at $\frac{1}{2} I^{\mathrm{el}}_{\mathrm{DS,\,sat}}$ as displayed in (c). Finally, (f) shows the hysteresis values as a function of sweep delay. The translation from sweep delay into sweep velocity is added in this panel. All values shown improve significantly when the sweep velocity is slowed down. The decrease of $R_{\square,\mathrm{sat}}$ for hole and electron side as well as the hysteresis experience a steep decrease at the beginning and turn into saturation when a sweep delay of 20 s was reached. Hysteresis reaches values close to zero in the saturation regime. The mobilities μ_h and μ_{el} show the same behaviour in inverse direction, they increase fast at the beginning and experience saturation at high sweep delays. Both reach values 3-4 times higher at low speed compared to the highest speed.

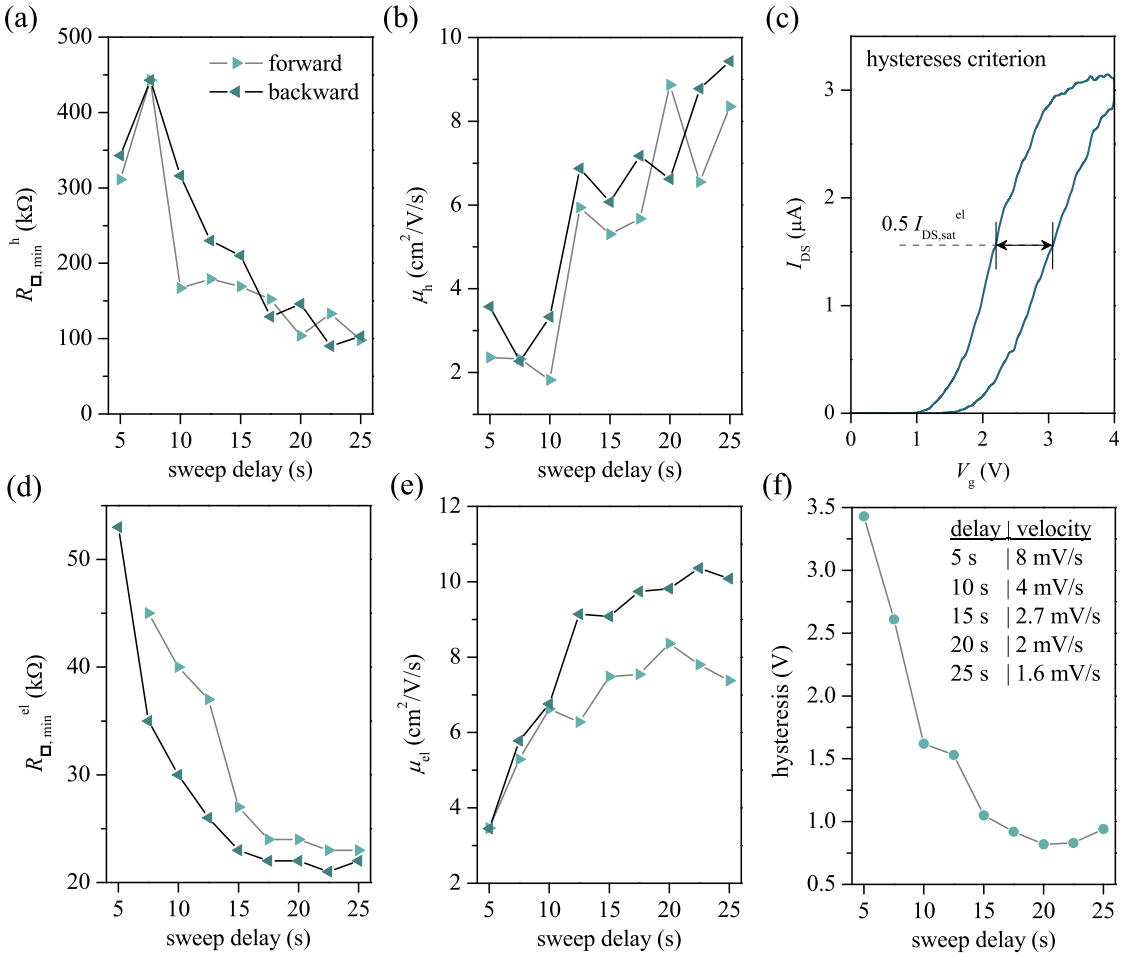

Figure 4.11: From the measurements shown in Fig. 4.10 extracted parameters and their dependence on speed velocity: (a), (d) saturation sheet resistance for hole and electron doping, (b), (e) electron and hole mobilities. (c) difference between forward and backward sweep at $\frac{1}{2} I^{\mathrm{el}}_{\mathrm{DS,\,sat}}$ as chosen criterion to define a hysteresis value. (f) hysteresis versus speed velocity. All parameters improve when the sweep velocity is reduced.

We can conclude that after 20 s the ions are still moving and far from a stable formation, but with a sweep delay of the same length, hysteresis is almost absent. A possible explanation is that the EDL on the device's surface is stabilised at first and only the remaining liquid ions far from the interfaces will continue to arrange themselves for many hours. The value of 20 s can be understood as characteristic time delay threshold from which on reasonably good quality EDL-gate sweeps result.

4.2.3 Temperature effects

It was discussed above that temperature affects leakage and drain-source current. To analyse these effects and especially the relation between I_{g} and I_{DS}, a study similar to the one described in the previous section was performed on the very same device, this time keeping the sweep velocity constant at $2\,\mathrm{mV\,s^{-1}}$ (= sweep delay of 20 s) and changing the temperature.

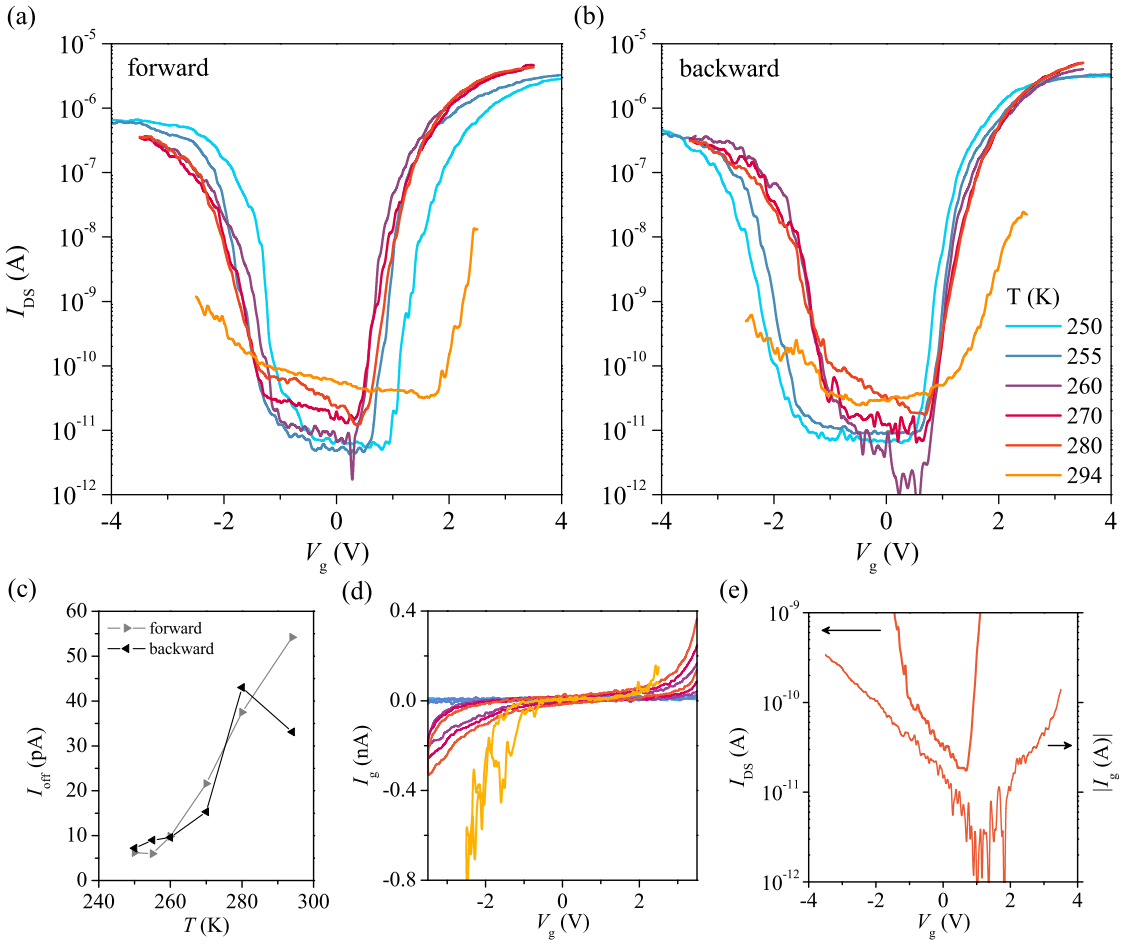

Figure 4.12: Device JS072d: Transfer characteristics at different temperatures performed with a speed velocity of $2\,\mathrm{mV\,s^{-1}}$. Hysteresis is small, but measurements become noisier at higher temperatures (mostly on the hole side) and off-state currents I_{off} are increasing with increasing T. (c) I_{off} versus T for both sweeping directions. It increases by almost one order of magnitude. (d) I_{g} as a function of V_{g}, it is increasing with increasing T. (e) Comparison of I_{off} and $|I_{\mathrm{g}}|$: both are plotted versus V_{g} in semi-logarithmic scale for $T = 280\,\mathrm{K}$ and show a similar slope, which suggests that the increase of I_{off} with T is a reflection of the increase of I_{g}.

In Fig. 4.12(a) and (b) the EDL-gate sweeps at 6 different temperatures are presented in forward and backward sweep direction respectively. The measurements were done, starting from the coldest and ending at 294 K, while the sweep range was decreased from $\pm 4\,\mathrm{V}$ at low T to $\pm 2.5\,\mathrm{V}$ at 294 K to avoid electrochemical reactions. The first observation is the huge difference between the room temperature gate sweep and all the other sweeps. It is very noisy in comparison and the transport gap is about 2 times bigger and less well defined than for the measurements at lower T. In general, the noise level increases with heating, especially on the hole side. E_{t}, however, is still very well defined and narrow for intermediate temperatures.

Another clear observation is an increase of the off-state current I_{off} when warming the system. Fig. 4.12(c) shows I_{off} as a function of T in forward and backward sweep direction. It hardly changes for $T \leq 260\,\mathrm{K}$, but experiences a steep increase when heating further

and reaches values by almost one order of magnitude higher for $T \geq 280\,\mathrm{K}$ than the low temperature values. This observation is coherent with the T dependence of leakage current I_g discussed in section 4.2.1. This suggests a correlation between I_g and I_{off}.

Fig. 4.12(d) shows the current-voltage characteristics of the ionic liquid, I_g versus V_g for both sweeping directions. The gate leakage current is almost constant and inferior to 20 pA for the two lowest temperatures, but increases continuously for increasing temperatures to end up being by two orders of magnitude higher at room T. Around $V_g = 0$, I_g has a small positive slope that gets higher when the temperature increases. In Fig. 4.12(a) and (b) it is clearly visible that for $T \geq 260\,\mathrm{K}$, the off-state current is no longer constant, but shows a negative slope which increases when T is increased. This fact again suggests a relation between the slopes of I_{off} and of I_g, which we will investigate in more detail in the following.

Fig. 4.12(e) shows the backward sweep at 280 K of both the drain-source current and the gate leakage current (in the case of I_g being the absolute value) as a function of gate voltage in semi-logarithmic scale. The two curves have almost exactly the same effective slope in the V_g interval of the transport gap, which leads to the conclusion that I_{off} is dominated by the leakage current passing through the ionic liquid between source and drain electrode, which we will call $I_{DS,leak}$. Note that as I_g is negative in this interval, its real slope is inverse to the one of I_{off}, a fact we will explain with the help of an illustration shown in Fig. 4.13. What is displayed is a cross section of the device along the tube's axis with arrows in the liquid droplet indicating all leakage currents and the directions of charge carrier flow[1]. Charge carriers (electrons or holes) move from source to drain electrode when participating in I_{DS}, but also when participating in $I_{DS,leak}$. I_g is the gate leakage current, where charge carriers move from both source and drain to the gate. In our setup, measurements are always made between drain and gate electrode. Regarding the situation from the drain electrode's "point of view", $I_{DS,leak}$ is created by charge carriers moving towards the drain and I_g by charge carriers moving away from it. Consequently, measured

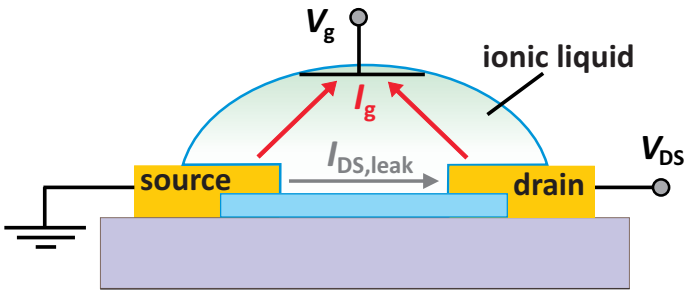

Figure 4.13: Schematic drawing of the cross section of an electrolyte-gated nanotube FET. The two leakage currents through the ionic liquid are drawn in the liquid droplet with arrows indicating the directions of charge carrier flow.

1 Note that this is not the technical direction of electrical current, which would be inverse.

$I_{\mathrm{DS,leak}}$ and I_{g} are exactly inverse to each other[1], which proves that I_{off} is dominated by $I_{\mathrm{DS,leak}}$ and higher off-state currents at higher temperatures do not originate from the INT itself.

The general observation is that heating increases leakage currents through the ionic liquid which directly affect the measurement and therefore gating becomes less efficient. At room temperature, leakage currents and noise get so high that no reasonable measurement can be performed. Possible reasons are on the one hand outgassing effects (e.g. of resist, water or glue) on the sample, chip, chip holder and surroundings, which leads to the accumulation of particles in the electrolyte which act as charge carriers. On the other hand, the reaction rate k of electrochemical reactions between ionic liquid and INT or contacts is related to T via the Arrhenius law ($k \propto \exp(-\mathrm{A}/T)$, $\mathrm{A} > 0$) and therefore, electrochemical reactions increase with increasing temperature. These reactions can strongly affect device performance.

As an increase of temperature results in a faster ionic liquid relaxation, we can conclude that the ideal temperature for the utilisation of EDL-gate transistors is 250-255 K.

4.3 Statistics

For this work, 18 devices (over 42 devices) on 12 samples were measured successfully. Gate sweeps were performed between different contact pairs or between the same contacts with changing V_{bias}. The sweep velocity was kept close to $2\,\mathrm{mV\,s^{-1}}$ in order to have minimal hysteresis effects. In total, 68 gate sweeps were used for statistical investigations. They were all measured in 2-probe configuration[2] and show very similar results, even though a certain dispersion of extracted parameters like sheet resistance and mobility is present. The causes of those differences are certainly differences in material and contact quality, but might also be of geometrical nature, like diameter and contact distance or differences in bias voltage. In this section, all transfer characteristics and resulting parameters will be compared to see tendencies and discuss preferable settings for future work.

4.3.1 Estimation of the Contact Resistance

We define the resistance values at the saturation regime for high doping levels as $R^{\mathrm{h}}_{\mathrm{sat}}$ and $R^{\mathrm{el}}_{\mathrm{sat}}$ for the hole and electron side respectively. As all measurements were performed in 2-probe configuration, the two-terminal saturation resistance is given by

$$R^{\mathrm{2t}}_{\mathrm{sat}} = R_{\mathrm{INT,sat}} + 2R_{\mathrm{c}} \ , \tag{4.4}$$

1 It was tested and observed that I_{g} is double as high as the leakage between source and drain as it consists of two parts, one between source and gate and the other one between drain and gate.

2 An explanation why 4-probe measurements were not performed in this system is given in 4.5.

with $R_{\mathrm{INT,sat}}$ being the intrinsic resistance of the inorganic nanotube at the saturation and R_{c} being the contact resistance. Wire resistances ($\approx 120\,!$ per wire) are by orders of magnitude smaller than the sample's resistance (from some kΩ up to GΩ) and can be neglected.

All nanotube devices vary in tube diameter and contact distance and therefore in the number of squares of the conduction channel. This number changes a lot, when comparing all measured devices, and can help to estimate values for the contact resistance on both hole and electron side. To do so, Eq. (4.4) was divided by the number of squares:

$$R^{\mathrm{2t}}_{\square,\mathrm{sat}} = R_{\square,\mathrm{INT,sat}} + \frac{2R_{\mathrm{c}}}{\#\mathrm{squares}}\ , \tag{4.5}$$

with $R^{\mathrm{2t}}_{\square,\mathrm{sat}}$ and $R_{\square,\mathrm{INT,sat}}$ being sheet resistance values. Thus, large numbers of squares diminish the contribution of the contact resistance in the measurement.

Fig. 4.14(a) and (b) show the sheet resistance values at saturation of all measurements versus the number of squares for hole and electron doping respectively. The data were fitted by the formula $y = c + b/x$ in order to extract the values $R_{\square,\mathrm{INT,sat}} = c$ and $R_{\mathrm{c}} = b/2$ for hole and electron doping.

The values obtained from the fitting and the fitting errors are shown in table 4.2. Already from a look at Fig. 4.14, it becomes obvious that fitting errors are enormous, especially at the hole side. Those errors come firstly from the determination of the INT's diameters by either atomic force or scanning electron microscopy. Secondly, the ions' slow motion might have influenced the extraction of saturation resistance values from the EDL-gate sweeps.

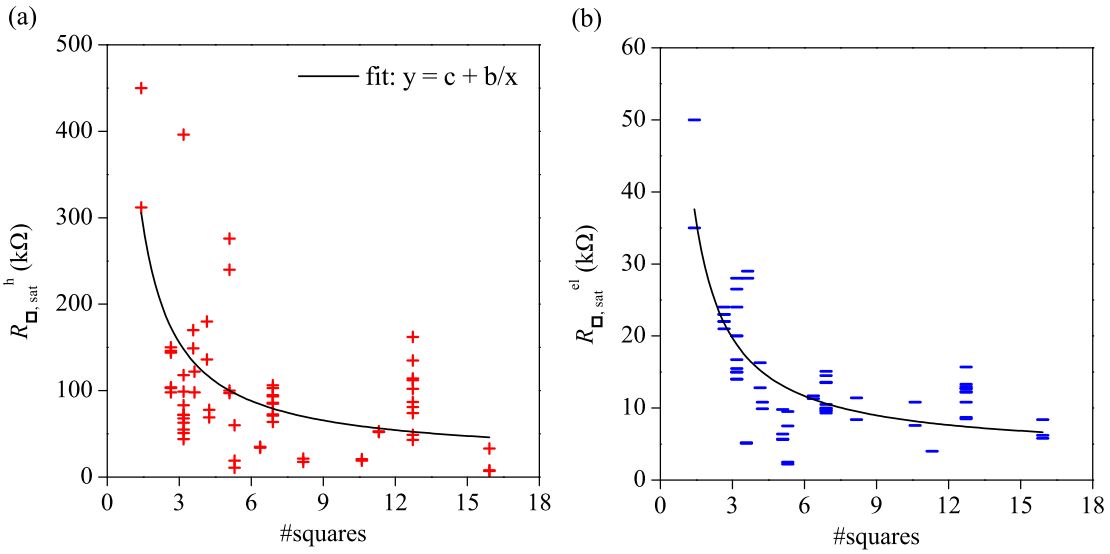

Figure 4.14: Square resistance at the saturation versus number of squares in the conduction channel at hole (a) and electron (b) side respectively. A numerical fit of a rational law helps to estimate contact resistances and intrinsic resistances of the 2D conduction layer for hole and electron doping.

Table 4.2: Parameters resulting from the fits shown in Fig. 4.14 and their fitting errors.

parameter	value (kΩ)	error (kΩ)
$R^{\mathrm{h}}_{\square,\mathrm{INT}}$	20.6	20.9
$R^{\mathrm{h}}_{\mathrm{c}}$	202	41.4
$R^{\mathrm{el}}_{\square,\mathrm{INT}}$	3.6	1.2
$R^{\mathrm{el}}_{\mathrm{c}}$	24.1	2.5

As we have seen, ionic liquid relaxation is a long process and the sweep velocities as well as the waiting times at highest gate voltages might not always have been sufficiently long to obtain the true values for $R^{\mathrm{2t}}_{\mathrm{sat}}$. Still, this method allows to give a rough estimation of contact resistances. We will ignore the error bars for an instant and just see how the knowledge of R_{c} affects mobilities. After subtracting R_{c} from R, an upgraded value for $G_{\square}$ can be calculated and used as basis for the extraction of mobilities.

This was done for the INT presented in Fig. 4.2(a), 4.10 and 4.12, which is a device with a very small contact distance so that the conduction channel only consists of 2.65 squares. In this case, μ_{el} increases by one order of magnitude from $\approx 10\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $\approx 100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and μ_{h} becomes about six times higher than without considering R_{c}. If an INT with different geometry is regarded, that is an INT with a huge number of squares, the change of mobility values is much less dramatical. For instance, in device JS069e with 16 squares and already quite high mobilities, both μ_{el} and μ_{h} only double after subtracting R_{c}: μ_{el} changes from $46\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $87\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and μ_{h} changes from $92\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ to $207\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$.

4.3.2 Diameter Dependences

For a tubular geometry, one of the most interesting relations is the possible diameter dependence of the bandgap. In the case of WS_2 thin films, Braga *et al.* claim that, when the technique of EDL-gating is used, it is possible to determine the energy bandgap from the EDL-gate characteristic (e.g. Fig. 4.2(a)) [30]. In general, a gate voltage change is the change of the material's chemical potential plus the variation of the electrostatic potential, which for a field-effect transistor is given as

$$e\Delta V_{\mathrm{g}} = \Delta E_{\mathrm{F}} + e\Delta\Phi = \Delta E_{\mathrm{F}} + \frac{e^2 n}{C_{\mathrm{g}}}\ , \tag{4.6}$$

with Φ being the electrostatic potential, n being the charge carrier density and C_{g} being the gate capacitance. If the last term can be neglected, the change of V_{g} equals the change of the chemical potential and Eq. (4.6) applied to the off-state range of V_{g} results as $e\Delta V_{\mathrm{GAP}} = \Delta E_{\mathrm{F}} =: E_g$. According to Braga *et al.*, the term $e^2 n/C_{\mathrm{g}}$ can be neglected in the case of EDL-gated WS_2, as the capacitance of an ionic liquid is extremely large and the crystals have a very high surface quality. Their WS_2 flakes have a negligible small density

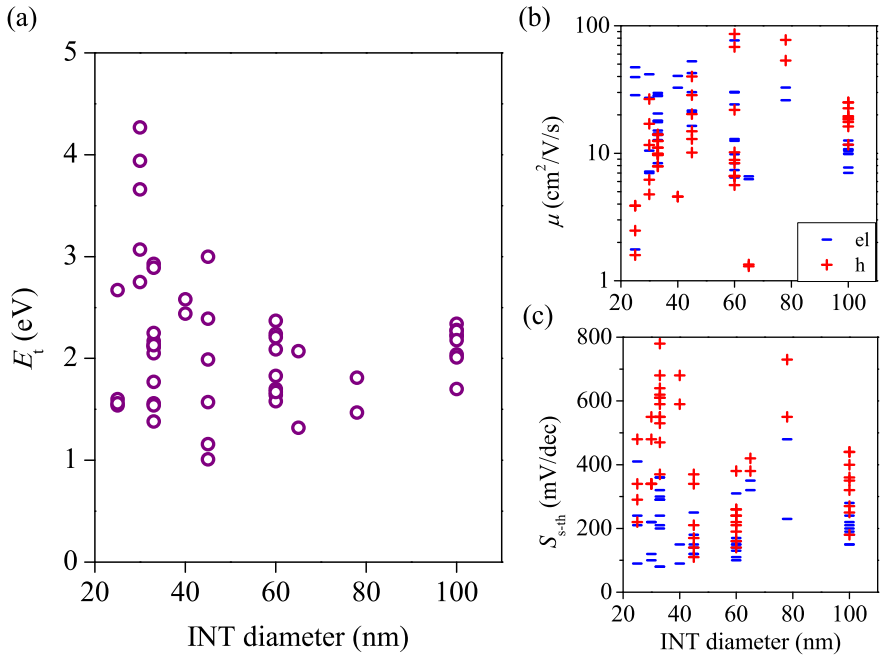

Figure 4.15: (a) Transport gap as a function of INT diameter. Gap values are more spread for small diameters, but no clear dependence is visible. (b), (c) Mobility and subthreshold swing versus INT diameter, each for electron and hole doping. Hole data are more scattered than the values for electron doping, but there is no diameter dependence present. Both μ_h and μ_{el} reach values up to $80\,cm^2\,V^{-1}\,s^{-1}$. $S_{s\text{-th}}$ on hole and electron side reach values down to 110 mV/decade and 80 mV/decade respectively.

of trapped states in the gap, shown by small off-state currents ($\sim 5 \times 10^{-11}$ A) and by low subthreshold swings ($\sim$90 meV/decade), which results in nearly perfect capacitive coupling between the electrolyte and the surface of WS_2 [30]. Note that similar studies have been done on WSe_2 [165] and on organic single-crystals [246]. Braga et al. observed 1.4 eV as gap size for multilayer WS_2 flakes, which coincides with the bandgap value of bulk WS_2 of $\approx$ 1.3-1.35 eV [106] within 10 % accuracy. In their following work, they extracted the bandgap values for mono and bilayer WS_2 again with high accuracy, being 2.14 eV and 1.82 eV respectively [99]. In this work, this gap is referred to as transport gap (E_t). Even if highest purity was assumed, due to the two-terminal configuration used, E_t includes the energy bandgap and some additional energy needed to overcome the Schottky barriers on the contacts. Consequently, we believe that the extracted E_t values are no more than upper limits for the bandgap.

Theoretical studies of single-walled WS_2 INTs predict that the bandgap increases with increasing INT diameter for very small diameters and approaches the single-layer limit for diameters $\gtrsim$6 nm [138]. The electronic band calculations were carried out by the density-functional tight-binding INTs with different chiralities and diameters varying from 2 nm to 17 nm.Theoretical studies of large diameter INTs were carried out by Ghorbani-Asl et al., who used density-functional theory and calculated the bandgap of large diameter single-walled, double-walled and multi-walled WS_2 INTs to be 2.01 eV (direct), 1.52 eV

(indirect) and 1.27 eV (indirect) respectively [67].

All measurements in this chapter were done on EDL-gated multi-walled WS_2 INTs with diameters varying from 25 nm to 100 nm (in the limit of large diameters) and with arbitrary chiralities. As EDL gating stands for surface doping and the creation of a 2D conduction channel, the charge transport in the WS_2 MWNTs is performed only in the few outer layers. The exact number of layers is currently unknown, but a gated tube can be seen as a few-layer tube, probably even mono- or bilayer. The underlying undoped layers stay isolating and are no longer to be taken into account.

Transport gaps were extracted from all EDL-gate sweeps and are shown Fig. 4.15(a) as a function of INT diameter. There is no dependence visible. Gap values are more scattered for smaller diameters, which is just due to the fact that most of the measured WS_2 MWNTs have diameters $\leq$60 nm. Most of the extracted E_t values are in-between 1.2 eV and 2.5 eV, which overlaps with the range of theoretically calculated bandgaps for large diameters. It is not astonishing that there is no diameter dependence of the transport gap as all nanotubes measured have diameters $\gg$6 nm and therefore their bandgaps are supposed to be in the thin film limit.

This fact suggests that there is no other diameter dependence to be expected and there wasn't found any. Fig. 4.15(b) and (c) show two parameters[1], mobility and subthreshold swing, as a function of INT diameter, each for hole and electron doping. In general, the values for hole doping are more scattered than for electron doping, but no diameter dependence is visible.

4.3.3 General Conclusions Based on the Statistics

It was mentioned above that differences in the properties of the WS_2 MWNTs are due to variations in tube quality and contact quality, or of geometrical nature, like diameter and contact distance. Some properties can additionally depend on the bias voltage. The conclusion of the last section was that the INT diameters of the tubes we measured are large and therefore have no influence on intrinsic parameters. Further studies show that the other geometrical factor, the contact distance, only influences the number of squares for the calculation of sheet resistance and mobilities. The bigger the distance between drain and source, the more squares build the conduction channel and the less important is the contact resistance (see also section 4.3.1). From all the statistics that were drawn up, no striking dependences result. A graphical summery over all statistics will be given and shortly discussed in appendix A.3.

At this place, the general results of the statistics will be shown and compared with values from literature. Mean, maximum and minimum values of the most important parameters

1 These two plots were not chosen due to any particularities. Different parameters would have lead to the same conclusion.

Table 4.3: Mean, maximum and minimum values of the parameters extracted from all EDL-gate transfer characteristics. For comparison the best room temperature values published so far on WS_2 flakes are given.

parameter (unit)	mean value	max value	min value	WS_2 flakes: best value
μ_h ($cm^2\,V^{-1}\,s^{-1}$)	17.0	86.2	1.3	90 [30]
μ_{el} ($cm^2\,V^{-1}\,s^{-1}$)	20.7	76.8	1.8	83 [46]
$R^{h}_{\square,sat}$ (kΩ)	98.2	450	10.8	
$R^{el}_{\square,sat}$ (kΩ)	16.8	148	2.2	
$S^{h}_{s\text{-}th}$ (mV/decade)	392	780	110	63 [99]
$S^{el}_{s\text{-}th}$ (mV/decade)	208	480	80	52 [99]
$h - I_{on}/I_{off}$ (decade)	3.8	5	2	5 [99]
$el - I_{on}/I_{off}$ (decade)	4.5	6	3	6 [156]
I_{off} (pA)	27.3	110	1.5	3 [156]
E_t (eV)	2.1	4.3	1.0	

are displayed in table 4.3 and best values reported so far on WS_2 flakes are given for comparison. Even if the resulting parameters are spread over quite a big interval, especially on the hole side, the devices show quite good performance compared to published results on WS_2 MWNTs and flakes. For instance, the mean values of our electron and hole mobilities are of the same order of magnitude as the highest electron mobilities of WS_2 MWNTs so far published of $50\,cm^2\,V^{-1}\,s^{-1}$ [115] and values for WS_2 thin film FETs lately reported (40 and $83\,cm^2\,V^{-1}\,s^{-1}$) [46, 156]. Only once, hole mobilities as high as the values we observed of $90\,cm^2\,V^{-1}\,s^{-1}$ were reported on WS_2 thin film FETs [30]. As contact resistance influences the extraction of mobility values, it was seen in section 4.3.1 that intrinsic mobilities can be by one order of magnitude higher than the presented ones. Current on-off ratios reach values as high as the highest values for WS_2 flakes published (10^6 and 10^5 for electron and hole doping respectively) [99, 156] and almost two times higher than the value of almost 10^4, reached in WS_2 MWNT systems [205]. Off-state currents with some 10th of pA on an average are as low as the lowest values reported (3 and 20 pA) [99, 156].

4.4 Ionic Liquid Gate-Characteristics in Comparison to an Electrostatic Backgate

It was mentioned several times that EDL-gating is especially convenient on a tubular geometry as it allows conformal doping on the entire surface. To underline this statement, we performed a backgate sweep with a 285 nm layer of SiO_2 as dielectric and compared it with an electrolyte-gate sweep. For the backgate (B_g) sweep we fixed the EDL-gate at 1.6 V, which is the threshold voltage for electron injection, and cooled down the device to 200 K. At this temperature, the ionic liquid is frozen so that ions are immobile and we

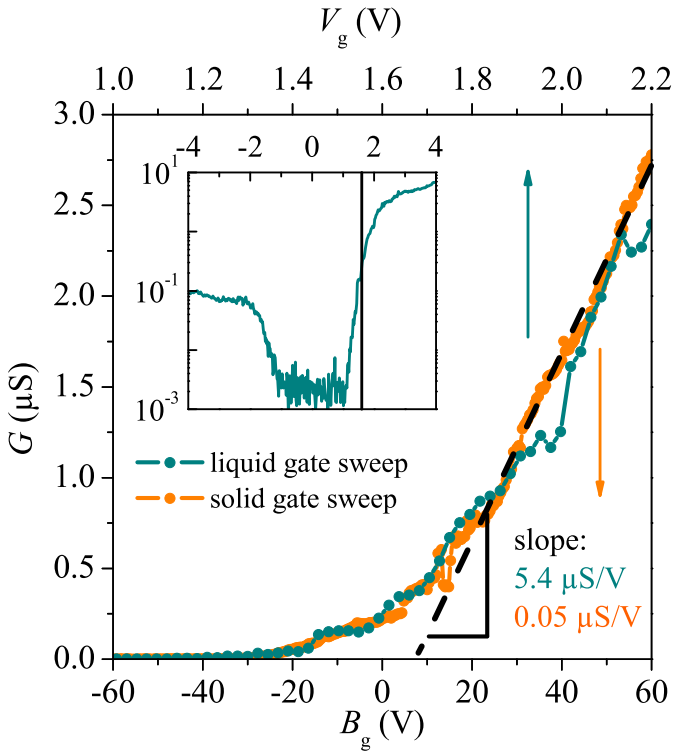

Figure 4.16: Device JS024b. Comparison of a solid backgate transfer characteristic (orange) at a fixed $V_g = 1.6\,\mathrm{V}$ and at $T 200\,\mathrm{K}$ and an EDL-gate characteristic (dark cyan) of a 70 nm thick INT in the same conductance range. The inset shows the whole electrolyte-gate sweep at 240 K, where a solid line indicates the fixed V_g voltage for the backgate sweep. 5 % of the solid gate voltage applied to the EDL-gate is sufficient to reach the same electron conductance.

can manipulate the charge carrier density by applying a voltage to the backgate, without risking side effects on the electrolyte. Fig. 4.16 presents the conductance as a function of B_g with frozen ionic liquid (orange) as well as a function of V_g at 240 K (dark cyan) in linear scale. Both sweeps were performed on the same WS_2 MWNT with a diameter of 70 nm. Both measurements are displayed within the same conductance range. The inset shows the entire EDL-gate sweep in logarithmic scale, where the black line indicates the fixed value $V_g = 1.6\,\mathrm{V}$, which was applied before freezing the ionic liquid in order to perform the B_g sweep.

A dashed line indicates the linear conduction increase which allows the extraction of mobility. The slope of the EDL-gate sweep is 100 times higher than the one of the backgate sweep, in other words, 0.2 V applied to the electrolyte correspond to almost 20 V applied to the solid backgate. Consequently, we find a big difference in subthreshold swing which is 9.8 V/decade in the case of SiO_2 as gate dielectric and 0.22 V/decade in the case of the electrolyte dielectric.

The mobility of the INT does not depend on the gate dielectric. We calculated it in both cases, using Eq. (4.2) in the case of the electrolyte-gate sweep, and the mobility results as $5.1\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. In the case of the SiO_2 dielectric, we calculated the field-effect mobility

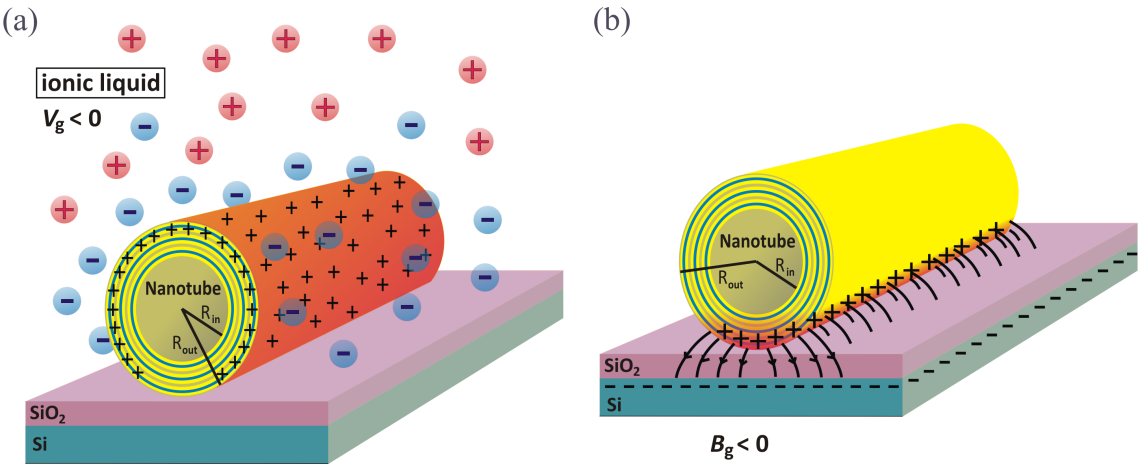

Figure 4.17: Schemata showing the difference between electrolyte-topgate and backgate field-effect doping, where created conduction channels are indicated in red: (a) WS_2 MWNT covered by an ionic liquid with a negative voltage applied to it and without backgate voltage applied. Negative ions are pulled towards the INT's surface, enabling hole injection (black plus signs) on the entire tube's surface. (b) WS_2 MWNT without ionic liquid and a negative voltage applied to the backgate. Hole injection only happens at the close surrounding of the INT/substrate interface.

with a formula for a backgated nanotube [134]:

$$\mu_{\mathrm{FE}} = \frac{dG}{dB_{\mathrm{g}}} \frac{L_{\mathrm{INT}}^2}{C_{\mathrm{g}}} \text{ , with } C_{\mathrm{g}} = \frac{L_{\mathrm{INT}} 2\pi\varepsilon_{\mathrm{r}}\varepsilon_0}{\ln(2h/r_{\mathrm{INT}})}. \tag{4.7}$$

L_{INT} and r_{INT} are the length and radius of the inorganic nanotube, ε_0 is the vacuum permittivity and $\varepsilon_{\mathrm{r}} = 3.9$ and h are the dielectric constant and the thickness of the SiO_2 layer. By using the values of our device, $L_{\mathrm{INT}} = 1\,\mu\mathrm{m}$, $r_{\mathrm{INT}} = 35\,\mathrm{nm}$ and $h = 285\,\mathrm{nm}$, we evaluated the mobility of $6.7\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. The difference of the two values is very small and as the backgate sweep was done at a temperature of 200 K, which is 40 K lower than the EDL-gate sweep, a slightly higher mobility was to expected.

This huge difference in the gate sweeps can be explained by a comparison of conducting surface areas displayed schematically in Fig. 4.17. A WS_2 MWNT is shown in (a) with an electrolyte as topgate with $V_{\mathrm{g}} > 0$ applied and no backgate voltage applied and in (b) without ionic liquid and only a backgate voltage $B_{\mathrm{g}} > 0$ applied. The doped channel region in each case is indicated by black plus signs and red colour. We assume that in the case of electrolyte-doping, transport occurs on the whole INT surface, whereas the conduction channel induced by the backgate is only built up in the close vicinity of the INT/substrate interface. We do not know the exact dimension of the conducting channel in this case and consequently cannot compare sheet conductances.

Nevertheless, the latter comparison emphasises the fact that ambipolar charge injection, low subthreshold swings, high mobilities and high charge carrier densities in WS_2 MWNTs can altogether only be achieved by using EDL-gating technique.

4.5 4-probe measurements of electrolyte-gated nanotubes

The electric contacts on a nanotube are generally fabricated in a way, so that they cross the nanotube, as shown schematically in Fig. 4.18(a), where a nanotube provided with four metal contacts is displayed. A cross section of Fig. 4.18(a) along the indicated plane is shown in Fig. 4.18(b). The electrolyte droplet with a positive voltage applied to the gate is indicated and the electron-doped regions in the nanotube are indicated in blue. The nanotube cannot be doped entirely, as in the case of a topgate dielectric, the gate effect is shielded by the metal contacts. Therefore, charge carrier accumulation only takes place at the tube's surface in-between the transport contacts reaching just far enough underneath the edges of the contacts to enable charge injection. The nanotube's surface underneath the metal will not be doped and is therefore always highly insulating. As a result, current passes alternating through the metal contacts and through the nanotube, as indicated in Fig. 4.18(b). Consequently, when a four-probe measurement is performed the contact resistance of the two voltage contacts will add up to the channel's resistance and it is impossible to get the intrinsic resistivity of the channel.

A solution can be the design of contacts which do not cross the nanotube, but stop at its centre. Such a contact design is possible and has already been realised by Hultin *et al.* [87], but adds delicate steps to the nano fabrication process[1]. This concept is feasible and should be a main goal for future devices, in order to obtain intrinsic values of resistance and mobility, as well as values for the contact resistance. Additionally, a superconducting

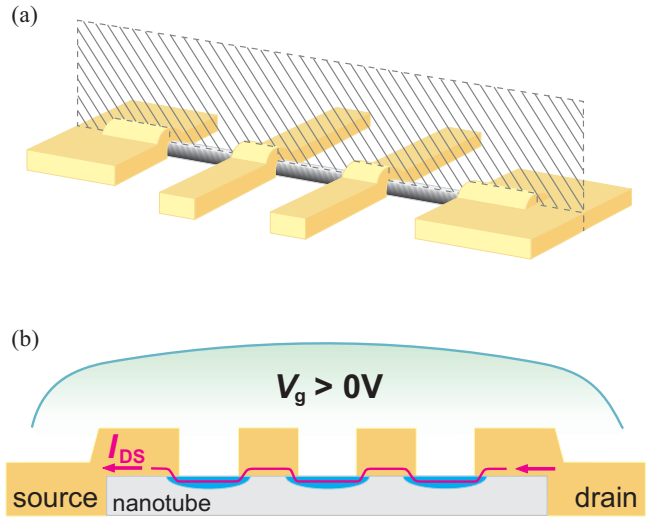

Figure 4.18: (a) Schematic drawing of a nanotube device provided with four electric contacts. (b) Cross section of the device shown in (a) along the indicated plain. A liquid droplet and doped regions in the nanotube are added, as well as the current path from drain to source.

1 Optical images would no longer be sufficient in precision for proceeding the design and the use of scanning electron microscopy would be inevitable for a perfect alignment of contacts and nanotubes. As this technique of microscopy creates charging effects, precautions have to be taken.

transition might only be observable in four-terminal configuration.

4.6 Conclusion

We succeeded in creating ambipolar field-effect transistors based on isolated multi-walled WS_2 nanotubes, using the EDL-gating technique. Our nano-scale transistors show promising performance, as our best devices show mobilities, on-off current ratios and transistor off-state currents comparable to highest values obtained for WS_2 thin flake FETs so far. The subthreshold swings we obtained are on average higher than lowest values published, but the subthreshold swings of our best samples approach the minimum values obtained on WS_2 flakes.

At low temperatures, we observed a field-effect induced insulator-to-metal transition and the investigation of weak-localisation effects clearly show that our conduction channel is in the two-dimensional limit. This confirms the statement of Brumme *et al.*, that 90% of the charge carriers accumulated in TMDC crystals by EDL-gating are distributed in the first two crystal layers [31].

Transfer characteristics showed standard transistor behaviour for $V_{DS} < V_g$, but a current increase was observed when the drain-source voltage exceeded the gate voltage. This feature was seen before in EDL-gated TMDC thin film transistors and is a sign of electroluminescence. Further investigations of optical activity in EDL-gated, multi-walled WS_2 nanotubes will be shown in the following chapter.

A study of ionic liquid relaxation and gate sweep velocity showed that a sweep velocity of $\leq 2\,\mathrm{mV\,s^{-1}}$ at $T = 250\,\mathrm{K}$ allows the ions inside the electrolyte to progressively rearrange following the gate voltage change, which results in non-hysteretic behaviour. The temperature influence was studied in a similar way and an important increase of leakage currents was found for temperatures $\geq 260\,\mathrm{K}$. As the preceding study yielded a faster ionic liquid relaxation with increasing temperature, T=250-255 K was found to be ideal for EDL-gating.

In total, we investigated 18 well performing devices, which allowed us to evaluate some statistics. For instance, we found a way to roughly estimate contact resistances, although we were limited to two-probe measurements. Ignoring the error bars, we were then able to give a tendency of mobility increase by a factor two, when subtracting contact resistances. Additionally, we demonstrated that, in the diameter range of measured nanotube devices (25 nm to 100 nm), the INT diameter does neither influence the device quality, nor the transport gap size.

We compared the gating performance of one device when using a SiO_2 backgate with the performance when using an electrolyte topgate. The observation of an equal intrinsic mobility gave proof that both configurations are working in our device. However, the general transistor performance, when using the ionic liquid-gate, was by orders of magnitude higher, shown by the fact that 20 V applied to the solid backgate correspond to $\approx$0.2 V applied to the electrolyte topgate. This leads to an increase of subthreshold swings by a factor of 45. Additionally, ambipolar behaviour was only observed in electrolyte-gated

devices, which leads to the conclusion that high charge carrier injection of both polarities into a nanotube is only possible by using an ionic liquid topgate.

Finally, we explained the difficulty of realising a contact design suitable for four-probe measurements on a tubular nanostructure. A solution is discussed and may be feasible for future devices.

CHAPTER 5

WS_2 Nanotube Light Emitting Transistor

This chapter presents our results of light emission by a multi-walled tungsten disulphide nanotube (WS_2 MWNT), prepared as an EDL-gated ambipolar FET. First, some theoretical background information will be given, followed by the realisation of an optical device within our system, the creation of a pn-junction in the inorganic nanotube (INT) only by adjusting electrical potentials applied to the device. Electroluminescence and photocurrent with their polarisation dependence will be discussed as well as the displacement of the pn-junction along the tube's axis when changing either the drain-source or the gate voltage. All measurements presented in this chapter were done at 250 K and in two-terminal configuration. The transport measurements were performed with an Agilent B2902A SMU, which then was used to apply drain-source and gate voltage during the optical measurements. The setup consists of a small cylindrical He-flow cryostat with optical access to the sample. The plain of the sample is imaged onto a CCD camera. A 405 nm laser is aligned with the objective and the sample in order to perform photocurrent measurements. Electroluminescence spectra were taken, using a spectrometer with a focal length of 550 mm and a 150 groove/mm grating.

5.1 Theoretical Background

One of the principles of quantum mechanics is the wave-particle duality which results in a relation between the particle's energy E and the frequency ν of the wave or its wavelength λ accordingly [60]:

$$E = h\nu = h\frac{c}{\lambda} = \frac{1240}{\lambda}\text{eV} \ , \tag{5.1}$$

with λ given in nm, h being the Planck constant and c being the velocity of the light. Equation (5.1) shows that energy is related to a characteristic wavelength. Accordingly, the energy value of the band gap of a semiconductor is related to a wavelength, too. The latter gives information about the light that can excite an electron from the valence into the conduction band or which will be emitted in the case of spontaneous or induced emission. These processes come along with the creation or recombination of electron-hole pairs. For optoelectronics, radiative recombination is essential, which has a much

higher probability in a direct bandgap semiconductor: photons have an almost nonexistent momentum which makes nearly vertical ($\mathbf{k} \approx 0$) recombination highly favourable. In an indirect bandgap semiconductor, an additional momentum is needed for the conservation of the total quantity of motion. This momentum is too large to stem from the photon itself and can be provided by the creation or annihilation of a phonon. This phonon's momentum must be the difference between the electron's and the hole's momentum. The bigger part of recombinations will take place at defects and impurities, considerably decreasing the probability of radiative recombinations [207].

An adsorbed photon creates an electron-hole pair, resulting in a photocurrent. Good efficiency is desired for photovoltaic devices and is equally more difficult to obtain in an indirect bandgap semiconductor, if the radiated light has exactly the energy of the bandgap. In this case only, a photon and a phonon have to be absorbed simultaneously. The radiation of higher energetic light will lead to direct transitions from any place in the valence and conduction bands. The carriers created in this way are called hot charge carriers, but they can relax efficiently inside the bands to gain the lowest energy possible.

In a semiconducting material at a non-zero temperature and without any external field applied, there will always be both spontaneous recombination and absorption processes with equal probabilities. In order to create a light source, free electrons are needed in the conduction band as well as free holes in the valence band. For instance, this is the case in a pn-junction, which is the way we use to create light.

5.2 Creation of a pn-junction

An ionic liquid as topgate is a ideal tool for the creation of a pn-junction. All processes needed are of electrostatic nature and therefore do not create defects and are completely reversible. Additionally, ionic liquids are transparent and almost optically inactive [99, 120], which proves them to be perfect topgate dielectrics for optoelectronic devices. The creation of a pn-junction with the help of an ionic liquid has already been mentioned in chapter 4 when transistor output characteristics were discussed (4.1.4). The group of Iwasa was the first to demonstrate the formation of a stable pn-junction on an EDL-gated transistor in 2013 by only playing with applied electric fields [258]. They built an ambipolar transistor of MoS_2 thin flakes and adjusted three different voltages in order to create a pn-junction: drain-source, gate-source and gate-drain (see Fig. 5.1(a)). The stabilisation was done by cooling and therefore freezing the electrolyte while applying the required voltages in order to create the pn-junction.

Later on, it was shown that two applied voltages, namely drain-source (V_{DS}) and gate-source (V_g) are sufficient to create a pn-junction in an electrolyte-gated device. For instance, the group of Morpurgo created a light-emitting diode based on ambipolar, electrolyte-gated WS_2 thin flake FETs in this way [99] (see Fig. 5.1(b)). Additionally, it was shown by Li *et al.* that photocurrent and photoluminescence are enhanced under EDL-gating [120].

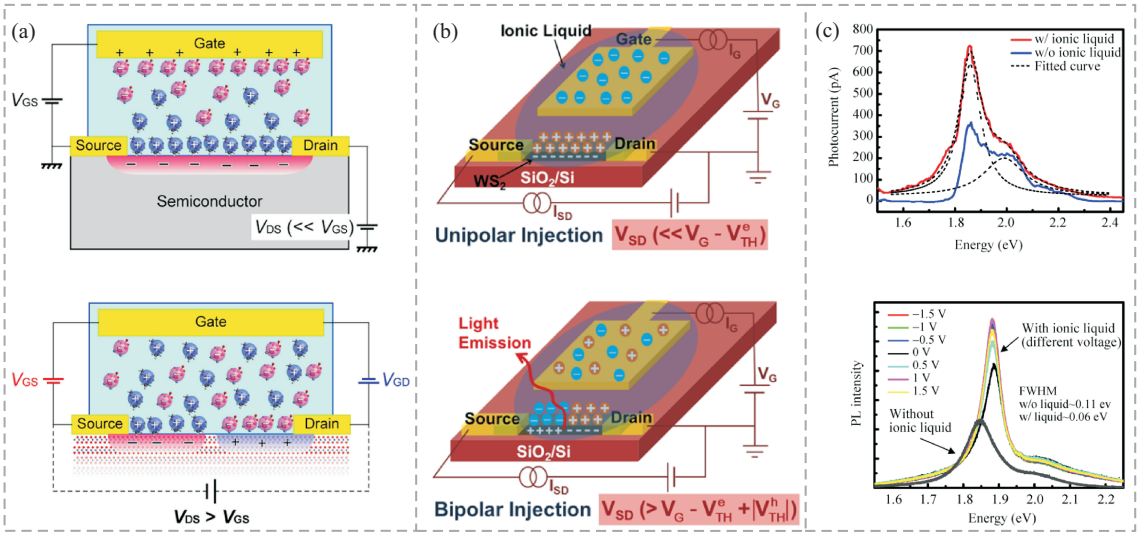

Figure 5.1: Three literature examples. (a) Creation of a pn-junction in an electrolyte-gated MoS_2 thin flake transistor by adjusting three voltages: drain-source V_{DS}, gate-source V_{GS} and gate-drain V_{GD}, taken from [258]. (b) Formation of a pn-junction in an electrolyte-gated WS_2 thin flake transistor by adjusting only two voltages: drain-source V_{DS} and gate-source V_G by [99]. (c) Demonstration of enhanced photocurrent and photoluminescence under EDL-gating, taken from [120].

Their experimental work is displayed in Fig. 5.1(c). How the interplay of drain-source and gate-source fields enables simultaneous electron and hole injection and therefore the creation of a pn-junction, will be explained in detail in the following.

An optical image of a typical INT transistor device is displayed in Fig. 5.2(a), taken after the lift-off process. The big rectangular, planar counter electrode is clearly visible, the contacted INT is just underneath. A zoom onto the nanotube will be shown later in this chapter in Fig. 5.7. The area which was covered by ionic liquid afterwards is highlighted in the image. It covers the whole counter electrode and the contacted nanotube. As for the FET devices, before performing the measurements, a thin glass slide was placed on top of the droplet (not shown in the image).

The EDL-gated INT transistor is displayed schematically in Fig. 5.2(b)-(c) with different electric field configurations. When no voltage is applied to the system, the liquid ions are mixed and homogeneously distributed in the electrolyte as shown in (b). In this figure, we only consider the case of positive voltages applied, the case of negative or mixed voltages would only change signs of ions and injected charges. In (c), a gate voltage $V_g > V_{th}$ and a drain-source voltage $V_{DS} \ll V_g$ are applied, which is the requirement for the creation of a conduction channel (in this case with electrons as charge carriers). So far, this case was the only one considered because the only interest was to dope the WS_2 MWNT homogeneously with either electrons or holes.

As the ions are liquid at 250 K and able to move freely through the droplet, they will react to any electric field applied. Consequently, an applied $V_{DS} > 0$, while $V_g = 0$, will lead to an accumulation of anions on the drain electrode and repel the cations. The latter will

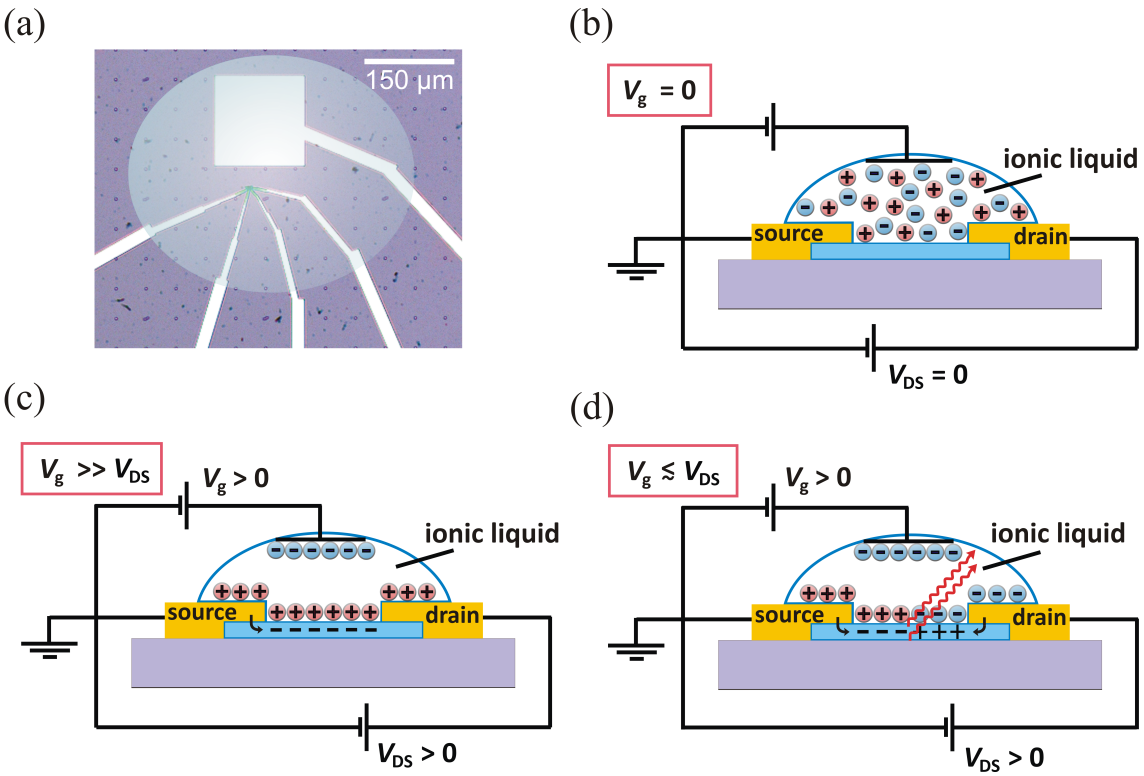

Figure 5.2: (a) Optical image of the device JS110g after the lift-off process. The area which was covered by ionic liquid afterwards is highlighted. (b)-(d) Schematic drawings of the electrolyte-gated INT transistor with no voltage applied in (b), a small drain-source and a high gate voltage applied in (c) and comparable voltages applied to both gate and drain-source in (d), which results in simultaneous electron and hole injection. Recombination and therefore light emission happens on the created pn-junction.

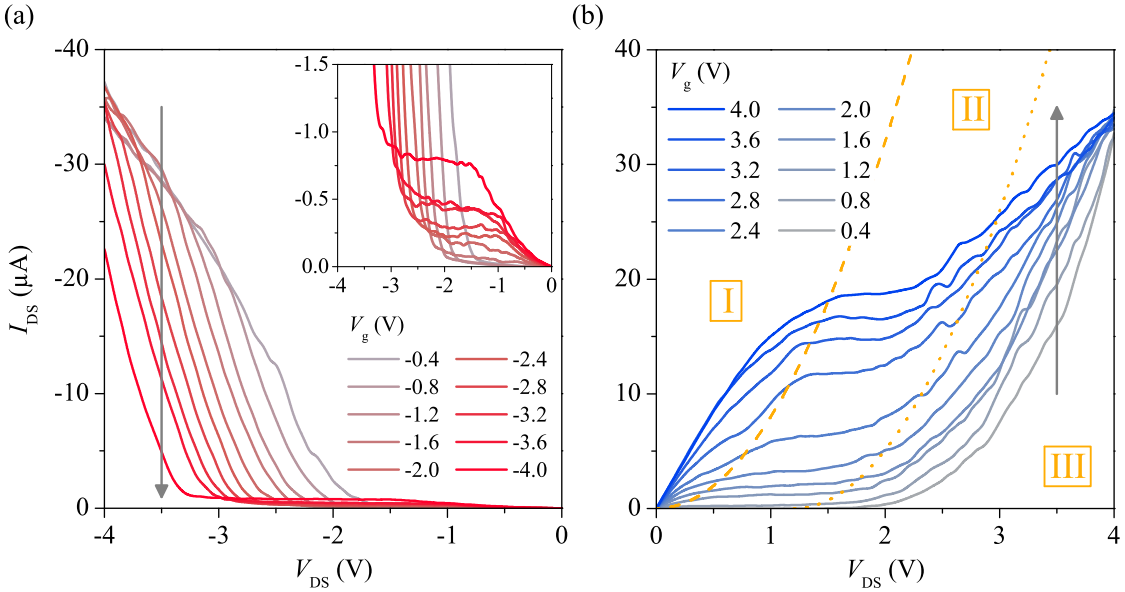

Figure 5.3: Device JS110g. Output characteristics of the WS_2 MWNT chosen for optical measurements with different (a) negative and (b) positive electrolyte-gate voltages applied. The maximal currents reach up to 35 µA at high V_{DS} values for both polarities. The inset in (a) shows a zoom into the low I_{DS} range. The characteristics are typical of EDL-gated TMDCs and are similar to those discussed in section 4.1.4.

accumulate on all metallic surfaces available which are the contact lines covered by ionic liquid and particularly the big counter electrode which has about three times more surface than the other three contact lines together.

For the creation of a pn-junction, the idea is to establish an accumulation of cations on and around the source electrode, which is big enough to enable electron injection from the very same electrode into the channel. This will happen with the help of a positive gate voltage applied. At the same time, a positive voltage applied to the drain electrode will lead to an accumulation of anions around this electrode, which then will lead to a hole injection from the drain contact. In the centre of the INT, injected electrons from the source and injected holes from the drain will meet, which directly results in the creation of a pn-junction. As we don't have any chemical dopants, there is no depletion layer of ionised dopants and electron-hole recombination can happen immediately.

Note that due to the big surface difference between drain contact and counter electrode, the system is much more sensitive to a variation of V_g than a variation of V_{DS}. The case of an established pn-junction ($V_g \lesssim V_{DS}$) is displayed in Fig. 5.2 (d).

As it was mentioned in section 4.1.4, the three regimes observed in the FET output characteristics (see Fig. 4.5) come along with the changes of ion formation due to changes of applied fields. IV characteristics of the same device displayed in Fig. 5.2(a) with a channel length of 1.6 µm are shown in Fig. 5.3(a) and (b) at different gate voltages applied and for hole and electron side respectively. The inset in (a) is a zoom into the low I_{DS} range to visualise the transistor characteristics at high gate voltages. The three regimes already discussed in section 4.1.4, are indicated in (b). Regions I and III are illustrated by the drawings in Fig. 5.2(c) and (d) respectively. Grey lines indicate the configurations for the spectra that will be presented later in this chapter (section 5.3). These output characteristics look very similar to those shown in section 4.1.4, especially on the electron side, where the ohmic and the saturation regime as well as the current increase at high drain-source voltages are clearly visible. On the hole side, the first two regimes are less pronounced in this tube: the curves are even more starved at low drain-source voltages and the saturation currents are by more than one order of magnitude smaller than it was the case for device JS099a. This is a sign of the presence of a higher Schottky barrier for hole injection in this nanotube compared to the one discussed in 4.1.4. Still, on both hole and electron side the third regime is very well pronounced, which is the current increase at high negative and positive V_{DS} values, and current values reach $\approx 35\,\mu A$ on both sides.

The ohmic regime stands for an established conduction channel as shown in the drawing Fig. 5.2(c). The second regime of pinch-off and current saturation starts when V_{DS} is getting strong enough so that cations are repelled from the drain contact and the conduction channel begins to disappear, starting from this contact. This situation would be in-between drawing 5.2(c) and (d) when the drain-source field is not yet strong enough to enable hole injection from the drain contact. As soon as V_{DS} is so strong that hole injection is possible, electrons and holes will meet in the INT and start to recombine and create a

current leading to the current increase observed in regime III. This situation corresponds to the drawing 5.2(d), where possible radiative recombinations are indicated by arrows.

As finally on both hole and electron side both types of charge carriers are injected with the according voltage configuration, we will from now on refer to the two sides as the case of negative or positive voltages applied.

The mechanism described above leads to the conclusion that at low gate voltages applied, even low drain-source voltages (of the order of V_g) lead to the creation of a pn-junction. Therefore, the output characteristic curves should all cross, as it is clearly the case for only negative electric potentials applied as shown in Fig. 5.3(a). Here, highest currents are achieved for lowest negative V_g values. In the case of only positive voltages applied (Fig. 5.3(b)) there is no crossing visible, but it might most probably happen at higher drain-source voltages. We were not able to observe the crossing as higher voltages applied would risk the damage of the INT. This observed asymmetry between positive and negative fields applied can be explained by the big Schottky barrier present for hole doping only. With a positive voltage applied to the gate and $V_{DS} = 0$, a conduction channel consisting of electrons will be established. In order to additionally inject holes from the drain electrode, V_{DS} must be high enough to create a field effect around the electrode and to overcome the barrier for hole injection. When starting with a negative gate voltage applied and therefore a conduction channel of holes, already V_{DS} values that create a small electric field close to the drain contact will be sufficient to inject electrons as no barrier has to be overcome.

5.3 Electroluminescence

Measurements of electroluminescence can give a hint of success in the creation of a pn-junction in our multi-walled WS_2 nanotube. While only very little theoretical work and no experimental work has been done so far on basic excitonic properties of TMDC nanotubes, flakes have been studied in various ways. We will give an overview of literature before presenting light emission of our nanotubes.

5.3.1 State of the Art on WS_2 Flakes

Theoretical and experimental studies demonstrate that basic excitonic properties are fundamentally different in monolayer and multilayer TMDCs. It is most common belief that the bandgap changes from an indirect to a direct one in the monolayer limit. A direct gap has equally been predicted for single-walled WS_2 nanotubes only, depending on the calculation method used and the chirality of the tube [67, 138]. In the case of multi-walled nanotubes, the gap is indirect, as it is the case for bulk WS_2, and light emission is much less efficient. The direct gap is always present at the K point of the Brillouin zone, but higher energetic than the indirect gap for layer numbers ≥ 2. Therefore, a pronounced transition is always associated with the direct bandgap for any number of layers.

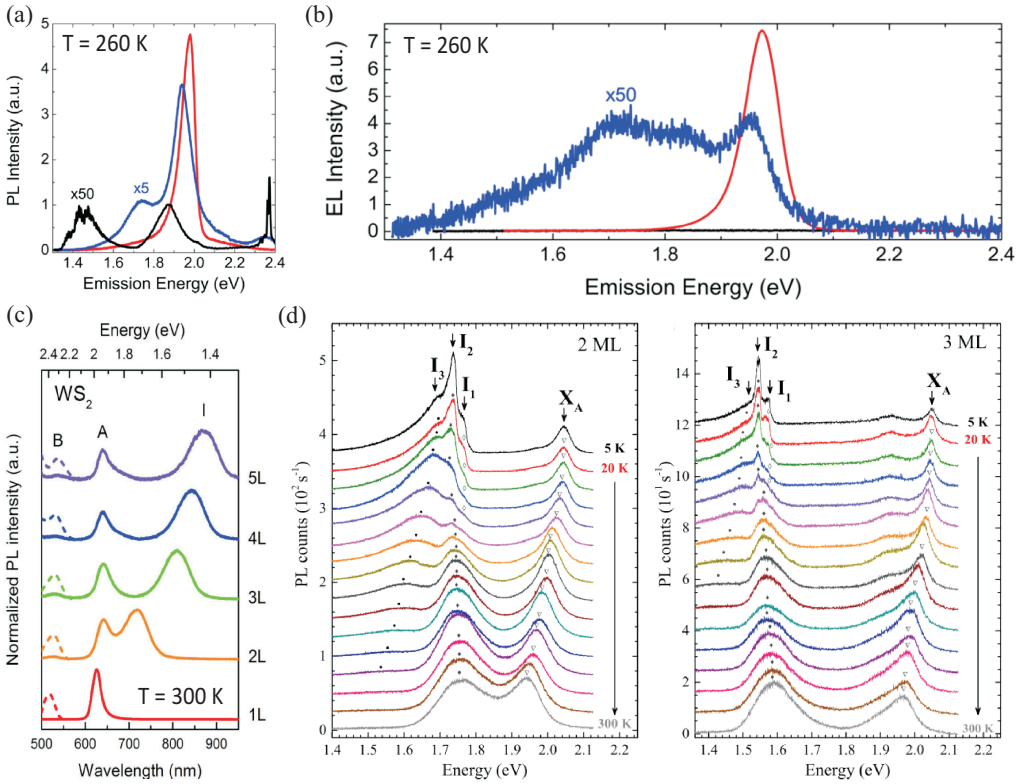

Figure 5.4: (a), (b) Photoluminescence and electroluminescence spectra of a WS_2 monolayer (red), bilayer (blur) and multilayer (bulk) flake (black), measured at $T = 260\,\mathrm{K}$. (c) Photoluminescence spectra of a WS_2 thin flake, measured at $T = 300\,\mathrm{K}$, with an increasing number of layers. (d) Photoluminescence spectra of WS_2 thin flakes with increasing temperature (from top to bottom) in the case of two and three layers respectively. The indirect transitions are labelled with the capital letter I and indices and the direct transitions are labelled as A, B or X_A. (a), (b) from [99], (c) from [261], (d) from [140].

So far, various measurements of photoluminescence and some measurements of electroluminescence have been performed on WS_2 thin flakes. Fig. 5.4(a) and (b) show photoluminescence and electroluminescence spectra of mono- and bilayer, as well as for a multi- (bulk) layer of WS_2, measured at $T = 260\,\mathrm{K}$ by the group of Morpurgo in Geneva [99]. Their samples were provided with an ionic liquid as topgate and they succeeded in creating a pn-junction as described above and displayed in Fig. 5.1(b). The monolayer exhibits a single peak, whereas bi- and multilayer exhibit one additional peak in the electroluminescence spectra and two additional peaks in the photoluminescence spectra. As expected for indirect bandgap semiconductors, the intensities of bi- and especially multilayer are largely reduced. The two most pronounced peaks were identified as direct transition peak at $\approx 2\,\mathrm{eV}$ and lower energetic, indirect transition peak. Fig. 5.4(c) displays the evolution of photoluminescence with the number of WS_2 layers at $T = 300\,\mathrm{K}$, measured by [261]. Two peaks for the direct transition, labelled as A and B, are visible. The peak energies are almost independent of the number of layers, whereas the situation is different for the indirect bandgap energy I. It is very close to the direct bandgap energy (1.98 eV [261]) in the bilayer case and approaches the bulk value (1.3 eV to 1.35 eV [100, 105]) when

the number of layers is increased. This observation was confirmed by [39, 103, 140], but is unexpected, as in general, when the layer thickness is increased, both direct and indirect bandgaps should decrease. Consequently, the shrinkage of the bands at the K point is mostly compensated by the decrease of the exciton binding energy [103].

Panel (d) shows a study done by the group of Potemski in Grenoble [140]: photoluminescence spectra at temperatures ranging from 5 K to 300 K (from top to bottom) in the case of two and three layers respectively. At $T = 5\,\mathrm{K}$, all peaks are very sharp and the indirect transition is split into three distinct maxima. I_1 and I_2 recombination processes are assumed to involve two different phonons and are assigned to the $\Lambda - \Gamma$ recombination processes, whereas the origin of the I_3 emission band is not entirely clear [140]. All peaks become smoother and broader with increasing temperature and the splitting of the indirect transition peak vanishes. The direct transition peak shifts towards lower energies for increasing T due to thermal expansion of the crystal, whereas the indirect transition peak energy is almost temperature independent and even a slight shift to higher energies is observed for the I_1/I_2 band. The reason is the occupation of higher energy states at higher temperatures and the increasing number of phonons. Therefore, there is no restriction for the phonon-assisted recombination of any higher energetic electron-hole pair and the emission peak is shifted to higher energies, which compensates the effects of crystal expansion.

The valence band maximum and conduction band minimum at the K point are split due to interlayer and spin-orbit coupling [169], which originate from the heavy transition metal atoms. This spin-orbit splitting is large only in the valence band (up to $\approx 400\,\mathrm{meV}$ in monolayer WS_2). As the conduction band is built by other heavy transition metal orbitals than the valence band, the splitting is considerably smaller ($\approx -30\,\mathrm{meV}$). In our case, all measurements were performed at high temperatures ($T = 250\,\mathrm{K}$) so that both split conduction bands will be populated and the effect of this splitting is negligible. Therefore, the valence band splitting only accounts at first approximation for the two most characteristic direct interband transitions A and B [103], labelled in Fig. 5.4(c)[1].

Note that most of the accomplishments just described originate from investigations of TMDC flakes. As very little and only theoretical work has been done on multi-walled nanotubes so far, we will mostly refer to the work done on the two-dimensional system. Band diagram calculations show that the general band structure dos not undergo a crucial change from flake to large, multi-walled nanotube and the discussion on the basis of TMDC flakes is reasonable. For instance, the theoretical work of the group of Heine [67] suggest a convergence of the indirect bandgap energy to the direct bandgap energy and a probable cross-over from indirect to direct bandgap in the single-walled limit.

1 Even if not mentioned in the publication, the B exciton transition is visible as a small peak at higher energies in the photoluminescence spectra shown in 5.4(a).

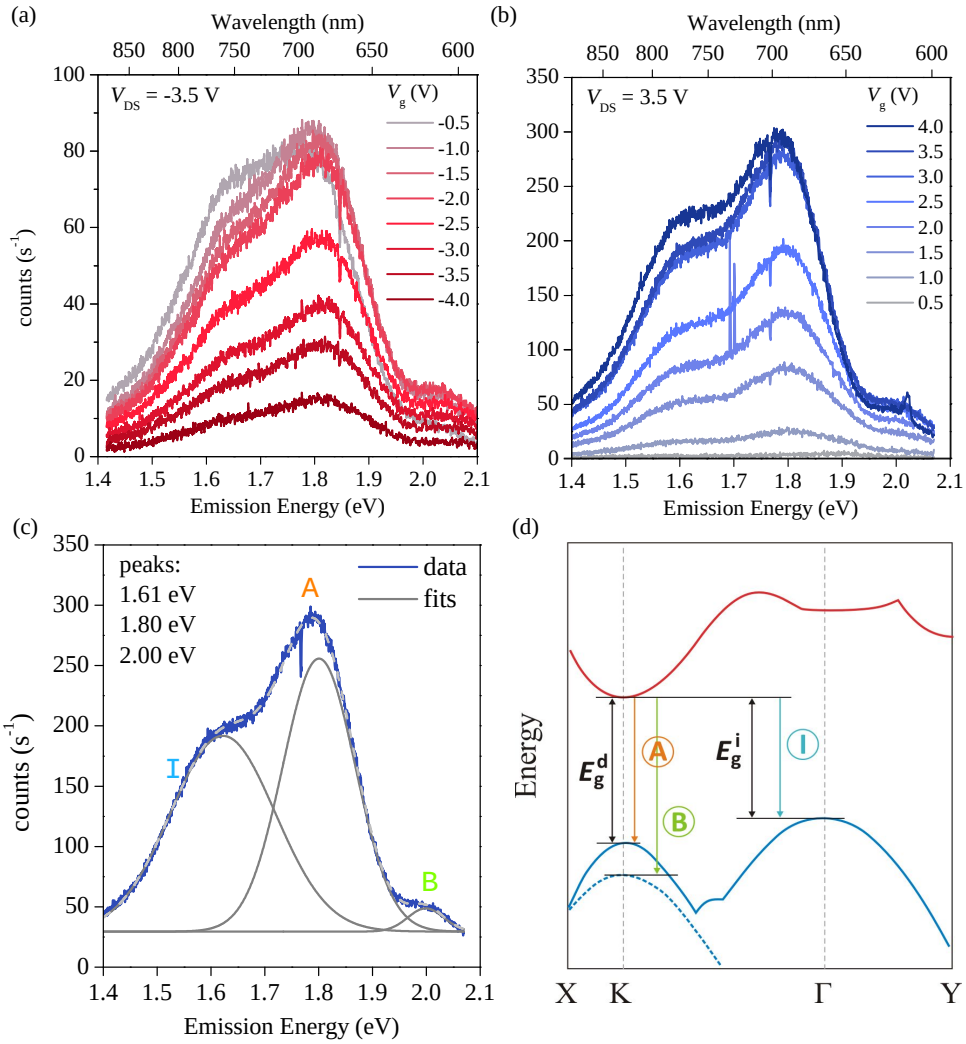

Figure 5.5: Device JS110g. (a), (b) Electroluminescence spectra for either negative or positive voltages applied at different V_g values. V_{DS} was kept constant at $-3.5\,V$ in (a) and $3.5\,V$ in (b). (c) Spectrum at V_g=3.5 V with Gaussian fits of the three peaks for the transitions A, B and I. (d) Simplified band structure of a multi-walled WS_2 nanotube, showing the lowest conduction band and the highest split valence band in red and blue respectively. A and B are the direct-gap (E_g^d) transitions and I is the indirect-gap (E_g^i) transition. Drawn after [67].

5.3.2 Light Emission by Multi-walled WS_2 Nanotubes

To observe electroluminescence, we applied gate- and drain-source voltages in a way that the tube was in the third regime, which was defined in the output characteristics (see section 5.2), where simultaneous electron and hole injection and therefore light emission are expected. Fig. 5.5 (a) and (b) show the emission spectra at constant $V_{DS} = -3.5\,V$ for different negative gate voltages applied and at constant $V_{DS} = 3.5\,V$ for different positive gate voltages applied respectively. For clarity, the configurations of applied voltages are indicated as grey arrows in the output characteristics in Fig. 5.3, indicating the direction of increasing V_g. One curve at $V_{DS} = V_g = 3.5\,V$ is displayed in Fig. 5.5(c) together with Gaussian fits for the three pronounced exciton transitions labelled with A and B for the

direct transitions at the K point and I for the indirect transition. Fig. 5.5(d) is a simplified drawing of the band diagram of a WS_2 MWNT, showing only the lowest conduction band and the highest valence band. The direct and indirect gaps are labelled with E_g^d and E_g^i respectively. The drawing is based on theoretical work of the group of Heine who employed density-functional theory to calculate the electronic structure of single-, double and multi-walled WS_2 nanotubes [67].

The spectra have all quite similar shapes and the gate dependence of the intensity is consistent with the gate dependence of I_{DS} at $V_{DS} = \pm 3.5\,V$ (along the grey lines in Fig. 5.3): the highest intensity for negative V_{DS} applied is observed at lowest V_g, whereas for positive V_{DS} applied, highest intensities are observed at highest V_g. Three distinct peaks are visible which are associated with the indirect transition for the lowest energetic peak, labelled as I and with the radiative recombination of the A and B excitons at higher energy. It is not astonishing that the A exciton transition is the most intense one, as it is the energetically lowest direct gap transition where radiative combinations occur more easily. The indirect transition peak is the second highest and therefore higher than the peak for the direct B exciton transition. This results from the high temperature ($T = 250\,K$) at which our measurements were done: radiative recombinations resulting from the indirect gap are more likely at high temperatures as more and higher energetic phonons are available. Note that the B exciton transition is only visible due to high temperature, where the corresponding split band edge is populated. At drain-source currents lower than $\approx \pm\, 2.5\,V$, no light emission could be detected, which proves that the current increase in region III is due to recombinations of electrons and holes, thereunder radiative recombinations.

The peak positions as a function of gate voltage for both positive and negative voltages applied are displayed in Fig. 5.6. For the main peaks, A and I, peak positions are constant, only for the B exciton transition, the peak position seems to evolve slightly. However, we should not be too excited about this observation, as the peak intensities of the B transition are generally very low compared to the A and I transition intensities and thus a credible extraction of the peak position is almost impossible. A real feature, however, is that peak positions for negative voltages applied are slightly shifted to higher energies. So far, we have no explanation for this observation, but will discuss a possibility at the end of this chapter in section 5.5.

Extracted bandgap values from the spectra and theoretical values from literature are displayed in table 5.1. It is not astonishing that there are big differences between the measured and calculated bandgap values. Firstly, no calculation of the direct transitions in multi-walled nanotubes exists and we cannot directly compare single-walled and multi-walled nanotubes. Secondly, the exact calculation of the band structure of a multi-walled nanotube does not have a unique solution as the shape of bands depends on many parameters. For instance, INT diameter, chirality of each wall and the orientation between neighbouring walls influence the band structure.

The full width at half maximum of the Gauss peaks are 0.19 eV for the indirect transition,

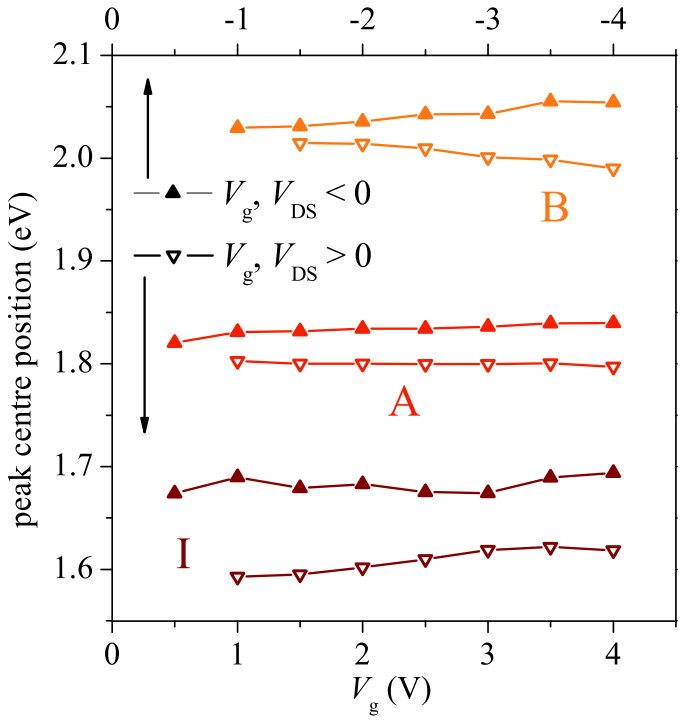

Figure 5.6: Peak centre positions of the three transitions (from Gauss fitting) and for negative (top axis) and positive (bottom axis) voltages applied.

0.13 eV for the A exciton recombination and 0.07 eV for the B exciton recombination. This result was to be expected, as the smallest gap shows the broadest transition due to populated higher energy states at the measured temperature of 250 K.

In our case, the indirect bandgap energy is closer to the direct bandgap energy than to the calculated bulk value of 1.27 eV [67], which is not expected for a thick multi-layer nanotube. Reasons might be strain effects or effects caused by the dielectric environment. The latter can be excluded as the dielectric environment is the same as the one of the measurements presented in Fig. 5.4(a) and (b), where no unusual behaviour was observed [99]. Calculations of the band structure of mono-, double- and multi-walled WS_2 nanotubes with different strains applied to the tube show that a strain would affect all band edges. Therefore, all transition energy value would change, not only one [67]. Consequently, neither the dielectric environment, nor strain effects should cause a shift of the indirect transition to higher energies. When we compare our spectra to photoluminescence spectra shown in Fig. 5.4, we see that our spectra resemble those of the bilayer case which suggests that our tube is in the few-layer limit rather than in the bulk limit.

Some of the features observed are not easy to understand. For instance, the intensity for negative voltages applied is three times smaller than that for positive voltages applied. Additionally, the peak positions are not exactly at the same emission energy for negative and positive voltages applied as shown in table 5.1. These two features could be a sign of a mechanism different from an established pn-junction that underlies light emission in

Table 5.1: Peak positions (averaged over all V_g values) extracted from the Gaussian fits of the spectra for both negative and positive voltages applied and calculated bandgap sizes for single-walled WS_2 and multi-walled nanotubes, as well as bulk crystal from the literature.

	MEASUREMENT		LITERATURE		
	peak position (eV)		bandgap sizes (eV)		
transition	V_{DS},$V_g < 0$	V_{DS},$V_g > 0$	single-walled	multi-walled	bulk crystal
A	1.83 ± 0.013	1.80 ± 0.003	2.01[67], 1.42 and 1,56[138]		1,79[100], 2.1[105]
B	2.04 ± 0.014	2.00 ± 0.015			
I	1.68 ± 0.012	1.61 ± 0.016	1,51[138], 1.55[107]	1.27[67]	1.3[105], 1,35[100]

our system. There might even be two different mechanisms depending on the electric field configuration. Further discussions of other possibilities will follow in section 5.5 at the end of this chapter.

5.3.3 Spatial Mapping and Anisotropy of the Light Emission

As WS_2 nanotubes emit light in the visible range, we were able to observe the light spot on the INT with an optical camera. Fig. 5.7(a) shows an optical image of the device taken directly after the lift-off process and (b) shows the same device inside the cryostat, provided with ionic liquid and a glass slide. In this image, the INT is in the light emission regime with $V_g = V_{DS} = 4\,V$ applied between the two contacts farthest right, with a distance of 1.6 µm. A green LED illuminates the device. An acquisition time of one minute was used to detect the light spot (highlighted by a red circle), the green LED was switched off less

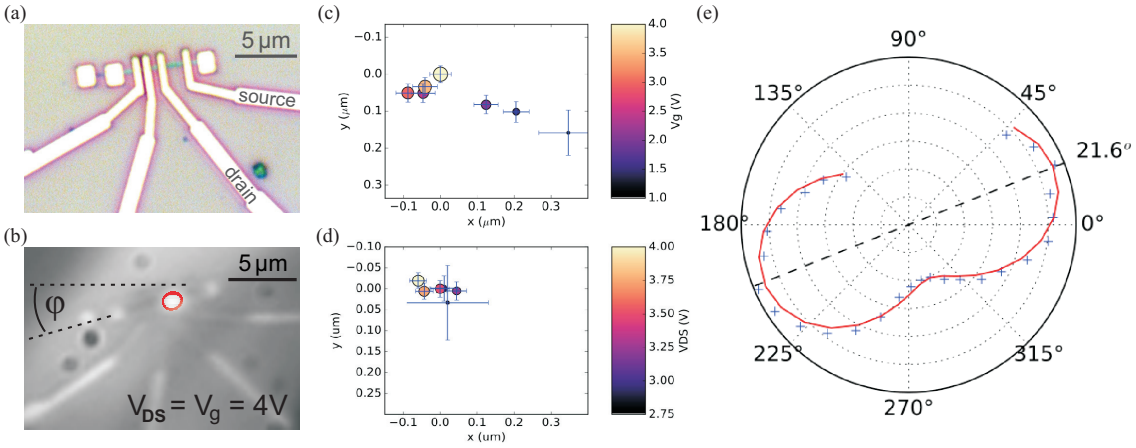

Figure 5.7: Device JS110g. (a) Optical image of a contacted INT device taken directly after the lift-off process. (b) Optical image of the same INT inside the optical setup. 4 V are applied to both source and gate electrode to establish a pn-junction and enable light emission. The light spot on the INT is emphasised by a red circle. (c) Displacement of the light spot with $V_{DS} = 3.5\,V$ and V_g varying. (d) Displacement of the light spot with $V_g = 4\,V$ and V_{DS} varying. The circle diameter indicates the intensity of the light spot. (e) Polar plot of emission intensity versus linear polariser direction normalised within the orientation of the optical image shown in (b). Highest intensity was observed for a polarisation along the tube axis within an error of about 5°.

than one second after starting the measurement in order to visualise both device and light spot in the same image. The angle $\varphi \approx 15°$ indicates the orientation of the nanotube in the optical setup. In this image, we can clearly see that the light source is our gated WS_2 MWNT as the spot is on the INT very close to the drain electrode.

Fig. 5.7(c) and (d) show the displacement of the light spot when V_{DS} was kept constant at 3.5 V and V_g was varied from 1 V to 4 V in steps of 0.5 V in (c) and when V_g was kept constant at 4 V and V_g was varied from 2.75 V to 4 V in steps of 0.25 V in (d). The positions are extracted from two-dimensional Gaussian fits of the light spots. The plot is normalised within the axis of the INT so that the y axis is the direction parallel to the tube. The size of the circles indicates the intensity of the light spot, error bars for the position in the x-y plain are added. A displacement of the light spot is only visible for changing the gate voltage in the interval from 1 V to 2.5 V. The spot moves in the direction from source to drain electrode and is generally very close to the drain contact. A variation of V_{DS} does not influence the spot position as can be seen in Fig. 5.7(d): the spot moves rather randomly and with distances of the order of the error bars. Such a small displacement of the light spot of only few hundreds of nm or no displacement at all is unusual and cannot be explained easily. Some further discussion will follow at the end of this chapter in section 5.5.

Finally, we placed a linear polariser in the optical axis in order to analyse the polarisation of the emitted light. A polar plot of emission intensity as a function of the polarisation angle is shown in Fig. 5.7(e). It is normalised within the orientation of the optical image shown in (b). We observed a maximum of intensity at a polarisation in the direction of the INT axis within an error of less than 5°[1]. Polarisation anisotropy for electroluminescence as well as photocurrent is expected in a nanotube due to diameters smaller than the wavelength of the applied light and therefore due to lateral confinement [44, 190]. For instance, it has been observed in CNTs [121, 139], in nanowires [4, 34, 93, 227] and in WS_2 NTs [242]. The intensity ratio between polarisation perpendicular and parallel to the axis is about 60-80%, which is consistent with values observed for different laterally confined structures [4, 76, 93, 121].

5.4 Photocurrent

A light-emitting optical device can at the same time have the ability to perform the inverse process of light absorption which results in photocurrent. By receiving a photon with an energy at least as high as the bandgap energy, electrons get excited from the valence into the conduction band, creating an electron/hole pair. The photon source can be a laser, halogen lamp or another light source with a corresponding wavelength. The electrons

1 Fitting errors and errors in the estimation of the tube's orientation in the setup, done by optically measuring the angle, add up so that an error of 5° is a reasonably good accordance.

and holes will then drift in the applied electric field to the source and drain electrodes. The Schottky barrier helps to separate charges, as it prevents charges from entering the channel, but allows charges to go out [61]. This process results in a so-called photocurrent which acts as an additional current source. We were able to measure a photocurrent in our WS_2 MWNT when exciting the INT by a continuous wave laser beam with a wavelength of 405 nm, which corresponds to an energy of ≈ 3 eV. The laser spot was enlarged to a diameter of ≈ 100 µm in order to have a homogeneous illumination of the device.

To visualise the photocurrent, we measured the drain-source current as a function of liquid gate voltage twice while shining laser light with two different power densities on the device and then compared it with the sweep without irradiation. Fig. 5.8(a) shows the three sweeps without any light applied and with a laser beam of 0.02 and of 1.7 kW cm^{-2} shone on the tube. Above, there is the gate leakage current I_g displayed as a function of V_g measured at the same time as the gate transfer characteristics. The bias voltage applied is 0.2 V, the gap region is emphasised in both panels. The inset shows a zoom into the gap region. From these plots we can observe three general features: the off current I_{off} is increased by more than one and almost three orders of magnitude upon irradiation with 0.02 and 1.7 kW cm^{-2} respectively, the curves for irradiation are shifted to the right and therefore more centred around $V_g = 0$ V and the slope of I_{off} is inverted when the curves for "no light" and irradiation are compared. The photocurrent increases linearly with the laser power density in the off-state ($V_g = 0$ V), as displayed in Fig. 5.8(b). Source-drain current in the off-state ($V_g = 0$ V) is plotted versus laser power density. As the INT is insulating at this gate voltage, the measured current is directly the photocurrent.

As explained in the preceding chapter in section 4.2.3, the negative slope of I_{off} without laser irradiation stems from leakage currents passing through the ionic liquid from source to drain electrode, which we called $I_{DS,leak}$[1]. In the case of illumination, the negative slope in the gap region vanished. Slightly increased leakage currents are expected [120] and observed, however, the slope of I_g is continuously positive and it stays at values below 300 pA in the gap region (see inset of Fig 5.8(a)). Consequently, the increased off-currents with irradiation are not an effect of increased leakage currents, but a real photocurrent. At higher negative and positive gate voltages, there is no effect of photocurrent visible. This is the case because the INT is strongly doped due to the field effect and a photocurrent of less than 1 nA is too small to affect I_{DS} considerably.

To obtain values for the right-shift observed after illumination, we extracted the centres of the gaps in the transfer characteristics and observed a shift of the centre of ≈ 400 mV. Such a right-shift was seen once before in CNTs [61] and its explanation was the capacitive coupling of the electrodes and the silicon backgate, which causes transients for a change in

1 The slope is inverse to the slope of the leakage current between source and drain electrodes and gate electrode, as on the one hand, charge carriers flow to the gate contact, away from the drain contact, and on the other hand, from the source towards the drain contact (see Fig. 4.13).

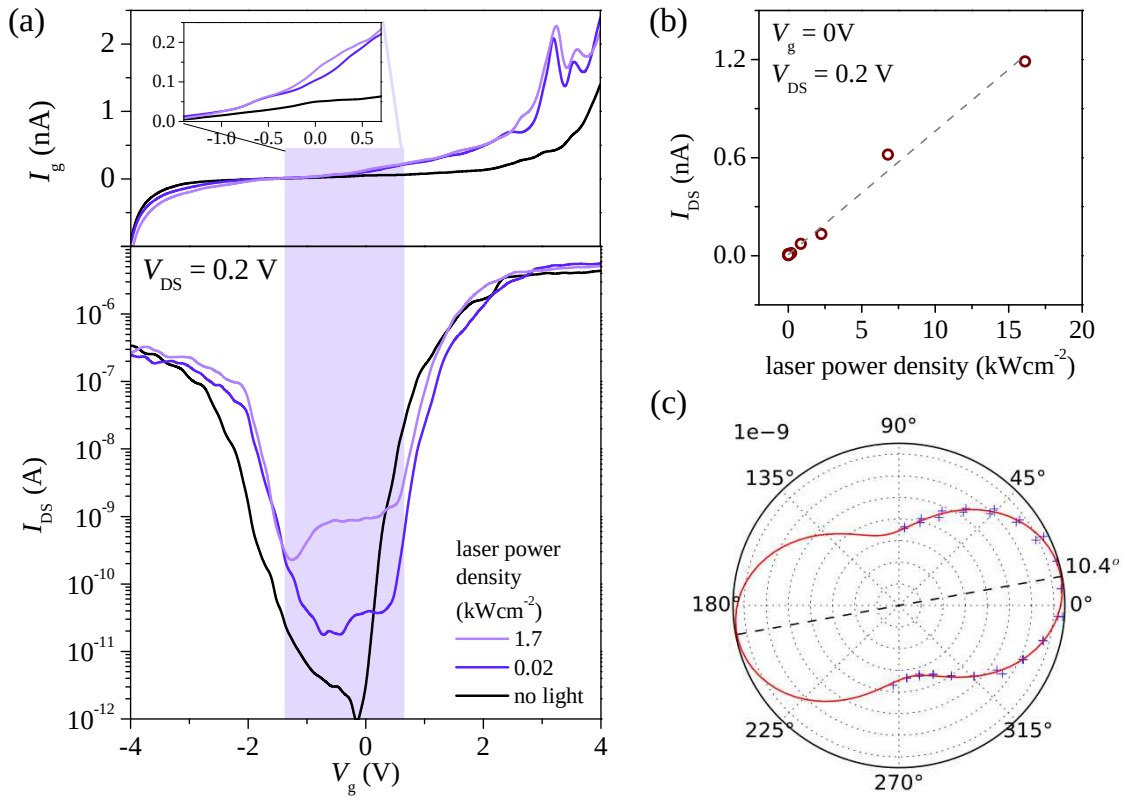

Figure 5.8: Device JS110g. (a) FET transfer characteristics with and without light irradiation with a laser of 405 nm wavelength. (b) Drain-source current as a function of laser power intensity at $V_g = 0\,V$. We find a linear relation. (c) Photocurrent at $V_g = 0\,V$ as a function of the polarisation angle normalised in the same way as in the case of emission shown in Fig. 5.7(e). The concentric circles show the light intensity in arbitrary units.

the photocurrent. As it has been seen on two tubular geometries, the shift might as well stem from chirality effects.

A linear polariser was mounted in the laser beam between the INT devices and the laser so that the polarisation angle of the light with respect to the direction of the nanotube axis could be adjusted to observe the polarisation dependence of the photocurrent. We found the expected polarisation anisotropy as displayed in Fig.5.8(c). Again, the maximum photocurrent was found for a linear polarisation along the INT axis, and the photocurrent ratio between polarisation perpendicular and parallel to the axis is about the same as the ratio observed for electroluminescence. We made one interesting observation which is the difference of the polarisation angle with respect to the nanotube axis for emission and absorption. The maximum of intensity for emission is reached at a $+5°$ shift, the maximum of photocurrent for absorption at a $-5°$ shift with respect to the INT axis. On the one hand, a variation of $5°$ is still within the possible errors, when measuring angles and calculating the fits. On the other hand, two shifts of the same size and in two different directions for emission and absorption, which are two inverse processes, suggest additional effects, such as chirality effects. This observation demands more investigations, but might be interesting to explore.

5.5 Arguments Against the Creation of a pn-junction

The only way of creating light emission considered so far was an induced pn-junction. However, we made certain observations which we cannot explain easily and which suggest different sources of the creation of light.

When the output characteristics in Fig. 5.3 are regarded, the current increase at low V_g and high positive and negative V_{DS} values is much more abrupt on the hole side and resembles very much a breakdown of the channel. Additionally, light emission takes place mostly very close to the drain contact, as shown in Fig. 5.7. Those two features may suggest light emission due to impact ionisation at the Schottky barrier at the drain contact, as has been seen for example in monocrystalline silicon [236], in ultrathin amorphous silicon layers containing silicon nanocrystals [63], but also in many other materials, e.g. [19, 226]. The mechanism is shown schematically and explained in Fig. 5.9(a).

With the knowledge of the breakdown field of the WS_2 nanotube, we can evaluate if the drain-source field E_{DS} can be sufficient to cause a breakdown. Fig. 5.9(b) shows the breakdown voltage as a function of the bandgap for many semiconducting materials in logarithmic scale. As there is a clear logarithmic dependence, we can classify the breakdown field for a multi-walled WS_2 nanotube as $\approx 4-5\times10^5\,\mathrm{V\,cm^{-1}}$, using the bandgap value of bulk WS_2 (1.27 eV [67]). The electric field along the INT is given as $E_{DS} \simeq V_{DS}/L$, with L being the channel length. In order to calculate the electric field at the probable breakdown, we use the voltage at the beginning of zone III in the current-voltage characteristic Fig.

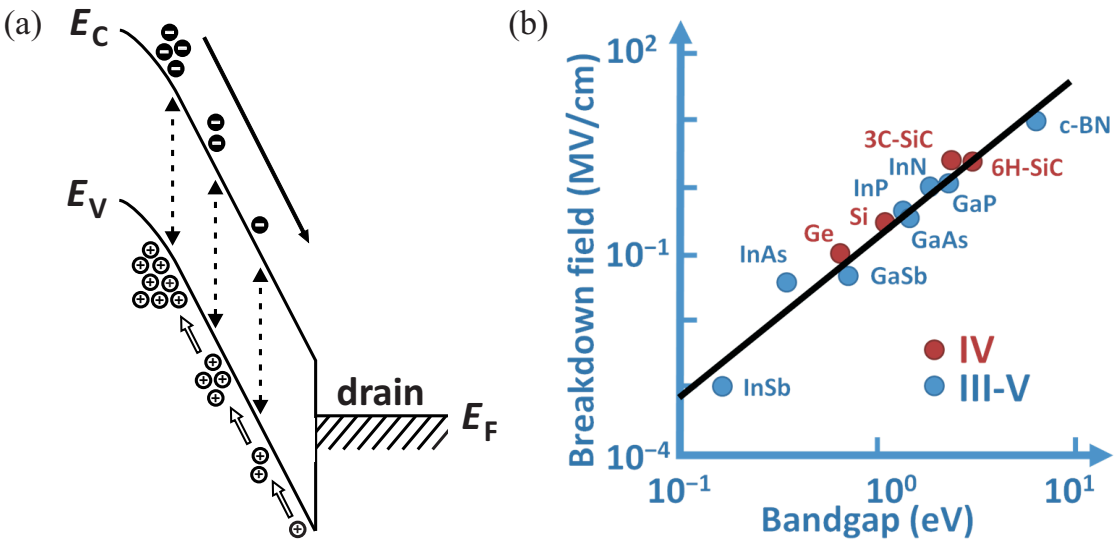

Figure 5.9: (a) Schematic drawing of an avalanche impact ionisation due to holes: the high drain-source field accelerates a hole until it is so energetic that it ionizes a lattice atom by collision, and a free electron-hole pair is created. The first and the newly created charge carrier will again be accelerated and an avalanche-like increase in the number of free carriers will evolve. The current is increasing substantially, but at the same time, the created electron-hole pairs can recombine radiatively. Drawn after [63, 207, 236]. (b) Breakdown field as a function of bandgap for selected materials in logarithmic scale, taken from [2]

5.3 as breakdown voltage, which is $\approx 2\,\mathrm{V}$ for low gate bias. The channel has a total length of 1.6 µm, thus the field at breakdown results as $\approx 1.3 \times 10^4\,\mathrm{V\,cm^{-1}}$, which is by more than one order of magnitude smaller than the breakdown field of the material. However, it would be wrong to consider the whole channel length of 1.6 µm in the calculation, as the tube is in the pinch-off regime before the breakdown. Thus the total voltage drop occurs in the pinched-off channel region, which is a fraction of the whole length and may be much shorter than 1 µm. In this case, an electric breakdown due to accelerated charge carriers is contemplable.

There might also be the possibility of two different sources of light emission, that is a pn-junction for positive voltages applied and impact ionisation for negative voltages applied. This would explain the still visible displacement of the light spot observed for a positive constant V_{DS} values and a variation of V_{g}, as well as the differences of the peak positions displayed in Fig. 5.9(b). The peak centre positions of the Gaussian fits for the three transitions A, B and I are shown in the case of negative (upwards triangles and top axis) and positive (downwards triangles and bottom axis) voltages applied respectively. The peaks for negative voltages applied are slightly shifted to higher energies over the whole gate voltage range. An explanation could be the very strong band bending at the Schottky contact, where impact ionisation induces avalanche recombination and therefore light emission [63], which might locally cause a slight variation of the band structure. At the same time, two different sources of light emission would give an explanation for the big difference of the IV characteristics and electroluminescence intensity for negative and positive voltages applied.

No general conclusion can be given at this point and more experimental investigations are needed in order to confirm the process responsible for light emission in WS_2 MWNTs.

5.6 Conclusion and Outlook

We presented a light-emitting transistor based on a isolated TMDC nanotube. The basic ingredient for light emission is simultaneous injection of electrons and holes that can recombine in a radiative way. In the previous chapter, we presented the ability to inject both types of charge carriers in a WS_2 MWNT field-effect transistor. Here, we demonstrated the convenience of an ionic liquid as gate dielectric to allow simultaneous electron and hole injection and therefore to create a pn-junction just by applying the right combination of gate-source and drain-source fields. We observed electroluminescence in the visible range (600 nm to 780 nm) for the two voltage configurations where radiative recombinations are expected. An optical image proves that the light source is the nanotube itself and a displacement of the light spot along the nanotube's axis was visible for a modulation of V_{g}. We recorded electroluminescence spectra and observed three distinct peaks which are associated with the radiative recombination of the A and B exciton of the direct bandgap in the K point as well as the indirect transition of lowest energy. The

latter is a sign of the nanotube being multi-walled and therefore an indirect semiconductor. These observations are in agreement with spectra that have been measured on WS_2 flakes, however, the transition peak energies resemble rather the bilayer case, than the bulk limit. We gave arguments against a strong influence of dielectric and strain effects, which lead to the conclusion that our INT is in the few-layer limit rather than in the bulk limit.

Besides electroluminescence measurements, we were able to inject electron-hole pairs in the nanotube and measure the resulting photocurrent which increases linearly with increasing power density of the illumination laser. We observed partial linear polarisation anisotropy for both photoluminescence and electroluminescence, as expected for confined structures such as nanotubes and nanowires.

Some of our observations arise doubts upon the mechanism that underlies the observed light emission. Due to the strong confinement in the tube geometry and Schottky barriers present at the contacts, an important acceleration of charge carriers might lead to the creation of electron-hole pairs by impact ionisation.

For gaining evidence in all observations, more devices have to be investigated at various temperatures, especially at low temperatures, where thermal broadening is no longer present. For instance, a reproduction of the spectra for nanotubes with a varying number of walls would suggest that strong surface doping influences the band structure in a way that the underlying layers have no great importance any more and the INT cannot be considered as a bulk, but as a tube with only few layers.

Improvement in light emission intensity can be achieved with contacts of higher quality. Therefore, more effort has to be put into decreasing Schottky barriers. A very interesting study would be that of the basic excitonic properties of single-walled TMDC nanotubes in order to prove the existence or non-existence of a direct gap in the single-walled limit.

CHAPTER 6

Ionic Liquid Gating of Large-Gap Semiconductors

One of the greatest advantages of an ionic liquid as gate dielectric is the ability to fabricate ambipolar field effect transistors based on semiconductors with bandgaps up to $\approx 2\,\mathrm{eV}$ without big difficulties. Monopolar charge carrier injection has already been performed on semiconductors with even bigger bandgaps, for example on the insulator $SrTiO_3$ [217] with a bandgap of 3.25 eV [16].

The biggest problem when performing field-effect measurements on large-gap semiconductors and insulators is the realisation of electrical contacts [25]. Especially ambipolar field-effect transistors are a great challenge as even with the best aligned work functions, for one single contact material the Schottky barrier at the contact will always be bigger for the injection of one of the charge carrier types. Methods as local gates [143] or different contact materials for hole and electron injection respectively [229] might give a solution. These methods require complicated steps of fabrication and are therefore not very practical. However, as seen in the preceding chapter, ambipolar operation is the basis for some efficient optical devices. As EDL-gating evokes a very strong band bending at the metal/semiconductor interface (see 4.1), it is banned from being a perfect tool for charge carrier injection into large-gap semiconductors.

Our most challenging and ambitious project was the realisation of an ambipolar field-effect transistor based on hexagonal boron nitride with a bandgap of $\approx 6\,\mathrm{eV}$. Similar to the TMDCs boron nitride is a layered material which possesses a direct bandgap in the monolayer limit. Together with the resemblance to graphene, boron nitride monolayers open the door to very interesting physics, for example the potential of replicating phenomena that occur only in graphene, with the advantage of possessing a bandgap, and applications such as high temperature electronics and UV lasing [97, 118, 230]. After time-consuming and very careful sample fabrication, we managed to see a very slight field-effect in a multilayer boron nitride flake. However, good electrical contacts are still a huge problem and a lot more effort has to be put into this field in order to strongly reduce contact resistance and realise a boron nitride FET.

In this chapter, we present instead field-effect measurements performed on two other large-gap semiconductors will be presented: diamond with a bandgap of $\approx 5.5\,\mathrm{eV}$ and

silicon with a bandgap of 1.1 eV at 300 K. In the case of boron doping[1], both diamond and silicon become superconducting when the amount of substitutional boron atoms and therefore of charge carriers reaches a specific critical level [32, 33]. The big disadvantage of impurity doping is that it causes enhanced disorder which can lead to many undesired effects. The motivation for the measurements presented in the following is to dope the intrinsic semiconductors electrostatically in order to accumulate the critical amount of charge carriers and obtain superconductivity. We have not reached this goal yet, but will present first steps towards field-effect superconductivity in both materials. The field-effect will be demonstrated by the resistance change with gate voltage modulation in the temperature range of 250 K to 4 K. Values for charge carrier density, mobility and capacitance, extracted from Hall measurements, will be shown and discussed in comparison with published results in similar systems. An Agilent B2902A was used to apply the gate voltage, whereas four-probe measurements for longitudinal and transversal resistance were done by using lock-in amplifier electronics, while providing up to 5 T. All measurements were done in vacuum and in a cryostat equipped with a superconducting coil.

6.1 Diamond

Diamond is the hardest material known so far and at the same time a beautiful jewel. In the world of science, diamond is well known for its outstanding physical properties such as high thermal conductivity ($22\,\mathrm{W\,K\,cm^{-1}}$) and a very high Debye temperature (1860 K) due to its strong sp^3 chemical bonds [208]. When doped with boron, the band insulator becomes a p-type semiconductor with a dopant level at ≈ 0.35 eV from the valence band [54]. The semiconducting diamond has a large breakdown field ($<10\,\mathrm{MV\,cm^{-1}}$), which makes it a very promising material for high-frequency and high-power devices [208].

The intercalation of boron atoms into the diamond lattice not only leads to a semiconducting nature of the diamond, but at high enough doping levels the diamond becomes metallic and eventually changes into a superconductor at low temperatures. First, it was common belief that the boron concentration n_B corresponding to the onset of superconductivity coincides with that of the insulator-to-metal transition (MIT). Only recently Bousquet *et al.* made an extensive study in order to unveil a new phase diagram differing from all previous reports [28], which is presented in Fig. 6.1(a). The Ioffe-Regel parameter $k_\mathrm{F}l$ (with k_F being the Fermi wave vector and l being the electronic mean free path), the superconducting critical temperature T_c and the residual conductance σ_0 (deduced from $\sigma(T) = \sigma_0 + \mathrm{A}\sqrt{T}$) are displayed as a function of n_B. A metallic, non-superconducting phase was observed (indicated in the plot as grey area) where T_c vanishes and σ_0 is still bigger than zero and only vanishes at the MIT. The doping concentration for the MIT was observed to be $n_\mathrm{B} = n_\mathrm{c}^\mathrm{MIT} = 3 \pm 1 \times 10^{20}\,\mathrm{cm^{-3}}$ and the boron-doped diamond becomes

1 A substitutional boron atom has one electron less than a silicon or carbon atom and therefore acts as charge acceptor that is incorporated into the valence band as a hole [142, 208].

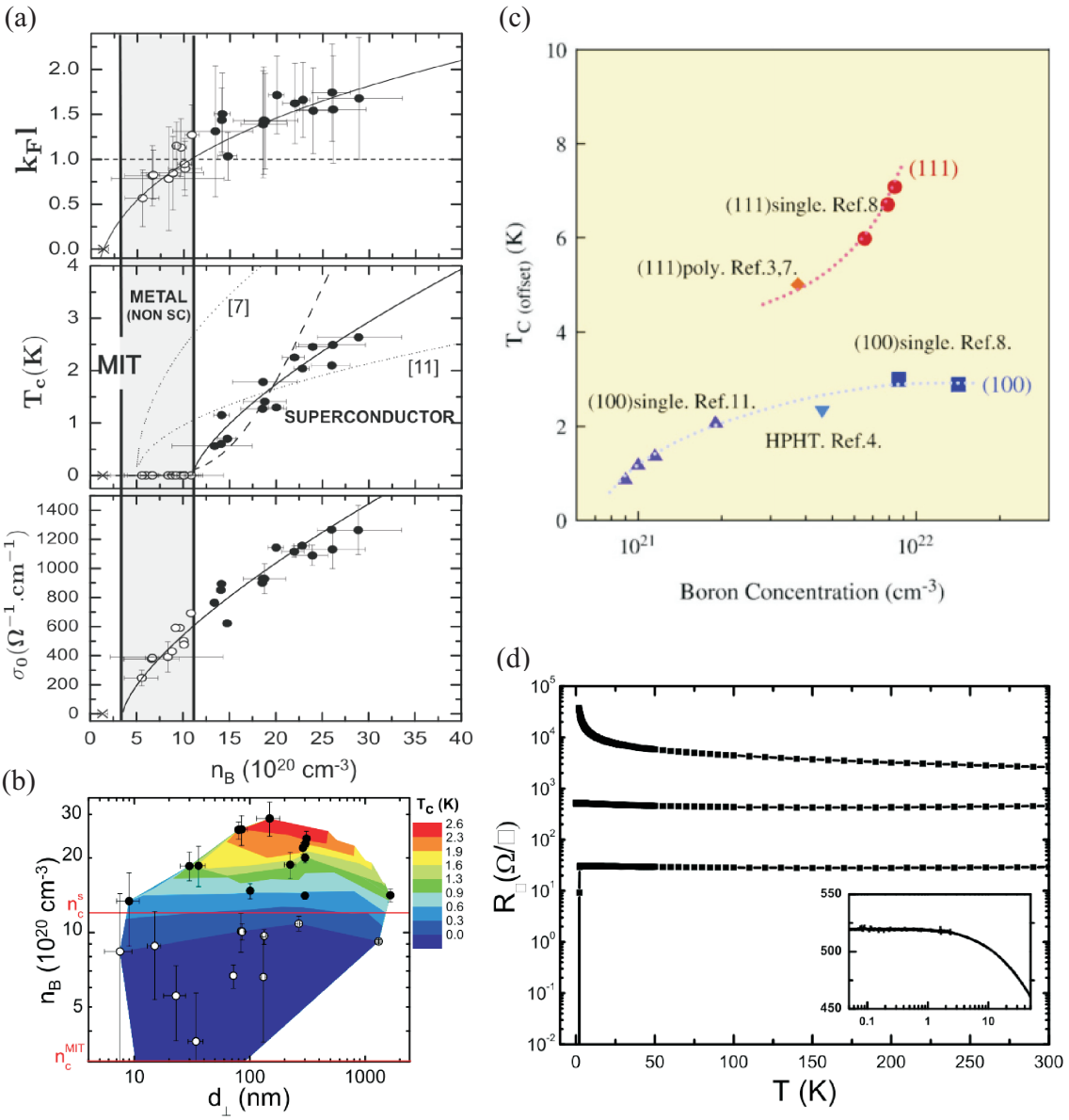

Figure 6.1: (a) $k_F l$ value, critical temperature and residual conductance as a function of boron concentration n_B. The metallic, non-superconducting phase is indicated as grey area. The solid lines are guides to the eyes showing that the MIT does not coincide with the onset of superconductivity. (b) T_c as a function of thickness and n_B. Open circles are samples in the non-superconducting, metallic phase. This plot clearly shows that T_c does not depend on layer thickness down to 8 nm. (c) Evolution of T_c with n_B taken from different publications. (d) Sheet resistance versus temperature of three boron-doped diamond films with the three possible comportments: insulating, metallic and superconducting. The inset shows a zoom into the low temperature part of the metallic sample. (a), (b) from [28], (c) from [208], (d) from [29].

superconducting from $n_B = n_c^S = 1.1 \pm 0.2 \times 10^{21}\,\mathrm{cm}^{-3}$. A dashed line indicates that superconductivity vanishes when the parameter $k_F l \sim 1$, which indicates that disorder

plays un important role in this system[1]. Fig. 6.1(b) underlines the existence of a metallic, non-superconducting phase (open symbols) above the critical boron concentration for the MIT. The figure also shows that there is no dependence of the critical temperature on the film thickness down to 8 nm.

According to the McMillan relation, the high Debye temperature of diamond can lead to high T_c superconductivity. The first superconducting boron-doped diamonds as well as the samples presented in Fig. 6.1(a) have superconducting critical temperatures $\leq 2.3\,\mathrm{K}$ [28, 32, 54] and one limiting factor was observed to be the electron-phonon coupling weak than expected which stems from low charge carrier concentration and the disorder caused by the dopants (vibrational modes strongly localised on the boron atoms) [22, 54]. Therefore, it was suggested that decreasing the disorder (e.g. by doping periodically [199]) and confining surface doping may lead to larger T_c values. In general, the strong covalent bonds in the sp^3 structure lead to large phonon frequencies and therefore to a large electron-phonon coupling potential, which should contribute to decrease T_c. Eventually, the difficulty in achieving high boron concentrations proved to be the main reason for restricting T_c. The highest present accessible boron concentration in diamond is 5 %, leading to the highest achieved T_c of 11 K [208]. At the same time, it was shown that films with (111) crystal orientation show highest critical temperatures. Fig. 6.1(c) shows the evolution of T_c with n_B for the two orientations (100) and (111), whereas the upwards pointing triangles are the values displayed in (a). 6.1(d) shows the temperature dependence of sheet resistance of three boron-doped diamond films with the three possible behaviours: insulating, metallic and superconducting. The graph shows that superconductivity was found in samples with a sheet resistance of a few kΩ. The inset is a zoom into the low temperature part of the metallic sample.

The fact that disorder is not the only T_c restricting component was shown by calculations which take into account effects of boron substitutional disorder [142]. Possible superconducting critical temperatures of $>50\,\mathrm{K}$ for heavily boron-doped diamonds were expected for $n_B > 20\,\%$. A technique of synthesis to achieve heavy boron-doping experimentally was proposed [142], but no success has been reported so far.

The surface of a diamond is known to be conducting when hydrogen-terminated with a sheet density of p-type carriers $10^{12} - 10^{13}\mathrm{cm}^{-2}$ [126, 131, 147]. The origin of the conductivity is not directly the hydrogen, as an adsorbed water layer is necessary, which is always present when left in ambient conditions. It provides an electron-sink and therefore provokes a hole accumulation on the surface [126]. Ohmic contacts on diamond have been a challenge for a long time, but the conducting surface enables the fabrication of low resistive contacts on the crystal [213]. In addition, the hydrogen-termination leads to an atomically controlled surface, chemical stability and low trap density [182], which

1 $k_F l$ is an indicator for the MIT and in our case for the suppression of superconductivity as well. Only in highly disordered materials, the MIT occurs at values $k_F l \leq 1$ [71].

are properties important for EDL-gating. The 2D nature of the surface conduction layer was experimentally demonstrated [77], whereas the exact thickness of the doped layer is unknown: it has been calculated in various ways to be between 5 Å and 2 nm [144, 147, 216] and therefore confines the holes in several carbon layers. To avoid disorder by chemical dopants, field effect doping which does not add any disorder to the crystal was proposed. First-principle calculations showed that electric-field driven hole accumulation potentially exceeds the critical concentration needed for superconductivity [144]. With the technique of EDL-gating, charge carrier accumulation up to two orders of magnitude stronger than with a standard dielectric gating is possible. The combination of both hydrogenation-terminated surface and efficient field-effect doping should lead to the desired result: superconductivity in intrinsic diamond with enhanced critical temperatures.

This prediction motivated us to conduct a systematic study of EDL-gated intrinsic diamond and search for superconductivity at low temperatures.

6.1.1 Sample Preparation

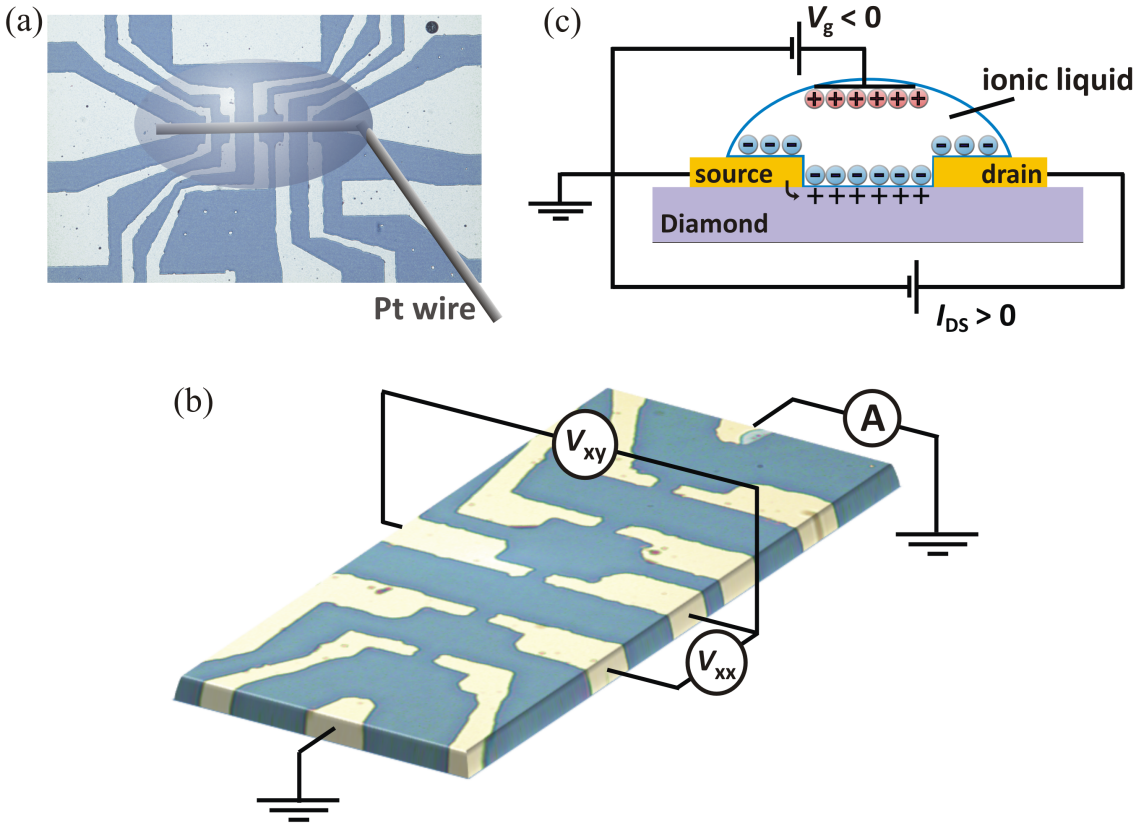

Figure 6.2: (a) Optical image of sample JS011 after the lift-off, the ionic liquid droplet is drawn on the photo to indicate the doped region. (b) Zoom into the channel region of the image shown in (a) with the contact configuration added for the measurements of longitudinal and transversal resistance. (c) Schematic drawing of an EDL-gated diamond sample with a negative gate voltage applied in order to accumulate holes on the channel surface.

We used non-intentionally doped, highly polished (100) substrates with hydrogen-terminated

surface as basis for electrostatic doping with the use of an electrolyte-gate. The average roughness of the diamond surface is $\approx 0.1\,\mathrm{nm}$, which underlines the high quality of the substrate. The preparation of a diamond sample is explained in detail in chapter 3 and an AFM image together with a roughness profile of the diamond surface is shown in Fig. 3.3. Electrical contact between gold bonding wires and both chip and bonding pads of the sample was realised by conducting silver paint. A photo of a diamond substrate with evaporated Hall bar is shown in Fig. 6.2(a). The droplet of ionic liquid on top of the channel region is drawn onto the image together with a platinum wire which was used as counter electrode. A zoom into the channel region is shown in Fig. 6.2(b) together with drawn contact lines to show the four-probe configuration for measuring both longitudinal voltage V_{xx} and transversal voltage V_{xy}. Fig. 6.2(c) is a schematic drawing of a contacted intrinsic diamond substrate with an ionic liquid gate. A negative voltage is applied to the counter electrode in order to accumulate p-type charge carriers on the diamond surface.

It is possible to geometrically define the conduction channel with an additional fabrication step[1]. We did not perform such an additional step, and therefore the whole surface covered by IL is doped and the sheet resistance is difficult to estimate. The number of squares in parallel is $\approx 3-6$, and we will only show the most resistive limit when considering six squares in parallel.

6.1.2 Metal-to-Insulator Transition

Sheet resistance $R_{\square}$ versus temperature for different gate voltages applied is displayed in Fig. 6.3. The inset shows a zoom into the low temperature part for high gate voltages applied. There is one additional data point visible for $V_{\mathrm{g}} = -7\,\mathrm{V}$ and $T = 2.2\,\mathrm{K}$, which was obtained by pumping on the helium reservoir inside the cryostat. In general, resistance decreases for increasing doping (= increasing negative gate voltage). Our first observation is that the diamond is conducting at room temperature without any gate voltage applied, which is the result of the hydrogen-terminated surface. At 230 K the sheet resistance varies very little, from $4.7\,\mathrm{k\Omega}$ at $V_{\mathrm{g}} = 0\,\mathrm{V}$ to $3.2\,\mathrm{k\Omega}$ at $V_{\mathrm{g}} = -7\,\mathrm{V}$. A big resistance change with gate voltage is only present at low temperatures ($<100\,\mathrm{K}$), where the diamond exhibits a semiconducting behaviour. At gate voltages ranging from $0\,\mathrm{V}$ to $-2\,\mathrm{V}$, the sample is insulating as resistance increases strongly with decreasing temperature. For higher doping ($V_{\mathrm{g}} \geq -3\,\mathrm{V}$) the resistance is almost T-independent and shows the behaviour of a dirty metal, which is a very slight resistance increase for decreasing temperature due to disorder-induced weak localisation[2].

1 In chapter 7, samples will be presented which are provided with a photo-resist mask that exactly defines the region where IL touches the surface, the conduction channel.

2 An slightly increasing $R_{\square}$ with lowering T is consistent with all measurements presented in literature so far, even for the superconducting samples. The first to observe almost temperature independent sheet resistance were Yamaguchi *et al.* in an EDL-gated intrinsic, hydrogen-terminated diamond [239]. Discussions will follow later in this chapter.

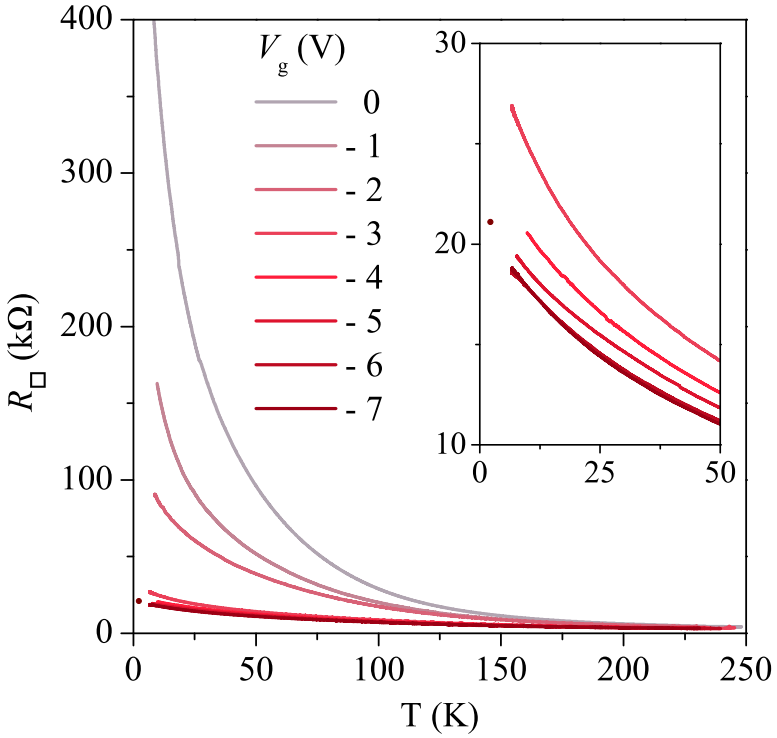

Figure 6.3: Sample JS011. Sheet resistance as a function of temperature for different gate voltages applied. The inset is a zoom into the low temperature range at high negative gate voltages applied. A transition from insulating at low hole doping levels to a dirty metal at higher doping levels. One additional data point at $V_g = -7\,\mathrm{V}$ and $T = 2.2\,\mathrm{K}$ was obtained by pumping on the helium reservoir inside the cryostat.

In the metallic range, the resistance decrease with increasing doping is very small and at $T \leq 100\,\mathrm{K}$ the sheet resistance for $-7\,\mathrm{V}$ applied becomes superior to $R_\square$ for $-6\,\mathrm{V}$ applied to the gate (see inset of 6.3). This increase might stem from electrochemical reactions which are expected at such high gate voltages and occur at $T = 250\,\mathrm{K}$ before cooling down. It is rather surprising that these kinds of reactions did not occur at much smaller V_g values, especially as the contacts contain titanium, which was shown to react much faster with the IL than palladium, gold or platinum (see section 1.2.4). A possible reason for the absence of electrochemical reactions is the carbide formation between titanium and diamond during the annealing step after lift-off. This titanium carbide alloy might be much more resistive to electrochemical reactions.

We could not observe any hint of a superconducting transition even when the sample was cooled down to $2.2\,\mathrm{K}$ at $V_g = -7\,\mathrm{V}$. When we compare our results with the study of various boron-doped samples in the insulating, metallic and superconducting doping regime displayed in 6.1(d), the lack of a superconducting transition is less surprising. The superconducting sample reaches a sheet resistance of a few kΩ, whereas our least resistive curve has a sheet resistance of almost $20\,\mathrm{k\Omega}$ at low temperatures. It is therefore close to the metallic sample, and the temperature dependence of the sheet resistance has a similar shape as the presented metallic sample.

6.1.3 High Mobility Charge Carrier Injection

We performed systematic Hall measurements at different temperatures and different gate voltages applied to access the p-type charge carrier density n_h, mobility μ_h and the capacitance of the ionic liquid C_IL. We consider our system as 2D electron gas and use the sheet conductance to calculate the mobility approximatively with $\mu_\mathrm{h} = G_\square/(n_\mathrm{h}e)$. The carrier concentration and mobility as a function of temperature are displayed in Fig. 6.4(a) and (b) respectively. Carrier density decreases with decreasing temperature, which is a sign of disorder [221], and increases with increasing negative gate voltage. There is a jump in hole concentration when V_g is increased from $-2\,\mathrm{V}$ to $-3\,\mathrm{V}$, which is consistent with the $R_\square$ versus T measurements presented above, where a strong resistance decrease was observed within the same variation of gate voltage. At $V_\mathrm{g} = 0\,\mathrm{V}$, the p-type carrier density is already of the order of 10^{13}, which is in the upper limit of expected hole concentration gained by surface treatment. With strongest field-effect modulation ($V_\mathrm{g} = -6\,\mathrm{V}$) we reached values up to $18 \times 10^{13}\,\mathrm{cm}^{-2}$ at $T = 200\,\mathrm{K}$ and up to almost $5 \times 10^{13}\,\mathrm{cm}^{-2}$ at $T = 50\,\mathrm{K}$.

Fig. 6.4(c) shows the hole density as a function of applied gate voltage with linear fits, indicated as dashed lines in order to calculate the capacitance of the IL via $C_\mathrm{IL} = e{\cdot}\mathrm{d}n_\mathrm{h}/\mathrm{d}V_\mathrm{g}$. The extracted capacitances as a function of temperature are displayed in Fig. 6.4(d). C_IL scales nearly perfectly as T^2, which we were not able to explain.

6.1.4 Discussion

We compare now boron concentrations of bulk diamond and field-effect induced carrier concentration on the surface. When the critical bulk boron concentration for a superconducting transition $n_\mathrm{c}^\mathrm{S} \approx 1.1 \times 10^{21}\,\mathrm{cm}^{-3}$ is taken and translated into sheet carrier density, the critical amount of holes results as $1.1 \times 10^{14}\,\mathrm{cm}^{-2}$ to $1.1 \times 10^{15}\,\mathrm{cm}^{-2}$ for a doped layer thickness of 1-10 nm. Consequently, the maximum carrier density we were able to induce via field-effect is not sufficient for superconductivity and is just above the critical boron concentration for a MIT ($n_\mathrm{c}^\mathrm{MIT}$ =$3 \times 10^{13}\,\mathrm{cm}^{-2}$-$3 \times 10^{14}\,\mathrm{cm}^{-2}$ for a channel thickness of 1-10 nm). This observation is in accordance with the sheet resistance obtained at highest doping levels (see Fig. 6.3), which is potentially too high for a superconducting transition.

We considered the thickness of our conduction channel to be $\geq 1\,\mathrm{nm}$, whereas from the discussion at the beginning of the chapter results that the channel thickness could be much smaller (down to 5 Å). In this case, our observed charge carrier density is much closer to the critical concentration for superconductivity and we must ask ourselves again why no superconducting transition is visible in our sample. Fig. 6.1(b) showed that T_c does not change with a decrease of the film thickness down to 8 nm. Together with theoretical predictions of possible surface superconductivity [69], this observation suggests that low-dimensional superconductivity could exist in diamond. However, except for very few examples, superconductivity is generally destroyed in reduced dimensionality, whereas disorder might play a crucial role [78, 146, 201]. A very important observation in this

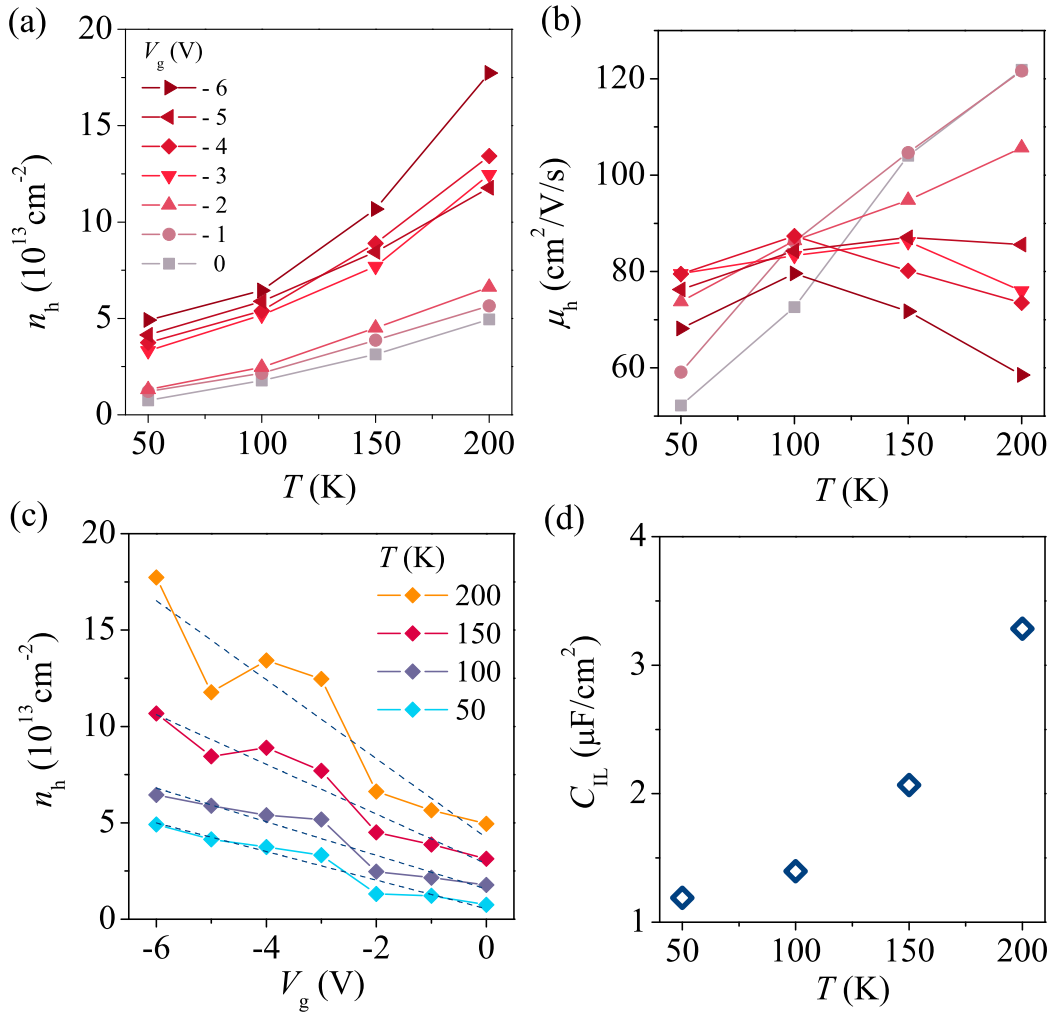

Figure 6.4: Sample JS011. (a) Charge carrier density as a function of temperature. n increases with increasing doping level as well as with increasing T. (b) Hall mobility of p-type carriers versus T. The V_g dependences of μ_h at 200 K and 50 K are inverse, whereas at high gate voltages, μ_h stays in the range of $60-90\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$. (c) Charge carrier densities plotted as a function of gate voltage for four temperatures. Linear fits displayed as dark blue lines were used to calculate the capacitances of the ionic liquid C_{IL} on hydrogenated diamond. The resulting values are displayed in (d) as a function of T.

context is quite a high level of disorder despite the fact that we induced charge carriers via field-effect into very clean, intrinsic diamond. The proof of disorder in the system is the increasing sheet resistance and the decreasing charge carrier density with decreasing temperature. The disorder might stem from charge disorder induced on the surface by the ionic liquid. With disorder clearly present in our sample, pure surface superconductivity becomes unlikely, which would again explain the high sheet resistance at highest doping levels and the lack of a superconducting transition.

We will now compare our data with published data of the same kind of system: a EDL-gated, intrinsic diamond with a hydrogen-terminated surface that has been measured by Yamaguchi *et al.* [239]. Their results are presented in Fig. 6.5, where sheet resistance and

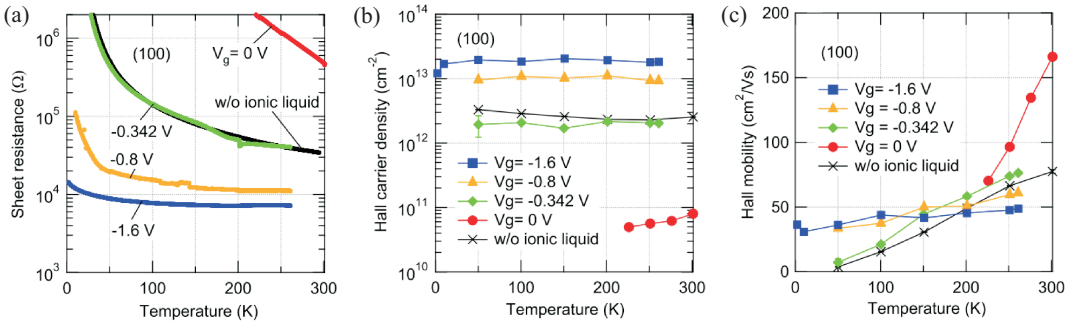

Figure 6.5: (a)-(c) Sheet resistance, Hall carrier density and Hall mobility versus temperature for different applied electrolyte-gate voltages applied. Taken from [239].

Hall carrier density are plotted versus temperature in semi-logarithmic scale (a)-(b), and the Hall mobilities as a function of temperature are displayed in linear scale (c). Their sample is more resistive at low gate voltages, but at highest doping sheet resistance reaches the same order of magnitude and even values of one order of magnitude less (depending on the crystal direction) compared to our samples, and they observe even less variation with T than we do. In fact, they were the fist ever to report nearly temperature independent sheet resistance in diamond. Their charge carrier densities were of the same order of magnitude as ours for equal gate voltages applied[1], but varied less with T. Their and our Hall mobilities behave in the same way in the same gate-voltage range[2]. The V_g-dependence of mobility is almost inverse at low and high temperatures respectively. At 200 K μ_h decreases with increasing charge carrier injection, which Yamaguchi *et al.* explained by an increased acoustic phonon scattering. At $T = 50$ K mobility first increases with increasing gate voltage, but re-diminishes slightly for $V_g > -4$ V. The increase was explained by an enhanced screening of the Coulomb potential created by excess anions accumulated on the crystal's surface. In general, mobility is in the range of 50 to 120 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (and 60 to 90 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for $V_g \geq -2$ V), which means that our mobilities exceed their mobility values by at least a factor two in the same temperature and gate voltage range. Our capacitances are of the same order of magnitude as those presented by Yamaguchi *et al.*. In general, their and our devices behave in a pretty similar way. The contradicting fact that their sheet resistance is lower and our mobilities are higher despite equal charge carrier densities might just indicate differences in the type of the used ionic liquid, the cooling speed and the choice of the electrodes' material. The latter is important in terms of electrochemical reactions.

Compared to mobilities measured in boron-doped, superconducting diamond, we observe

1 Yamaguchi *et al.* struggled a lot more with electrochemical reactions and could not apply gate voltages higher than −1.6 V.

2 Note that charge carrier density at $V_g > -5$ V and therefore mobility are not coherent with the measurements at all other gate voltages. This can have various reasons, amongst others an accidental variation of cooling speed when freezing the ionic liquid, which might lead to a variation in crystal formation of the IL and with it to variations in field-effect efficiency.

values which are by a factor of 20 higher [28], which is not surprising, as the boron doping increases the disorder. To our knowledge, our mobilities are the highest values reported so far for such high charge carrier densities. It is worth noting that all our calculations are based on a sample geometry of six squares in parallel, which is the maximum value estimated. Consequently, sheet resistance could be up to two times smaller and sheet conductance as well as mobility two times higher than presented.

It was again Yamaguchi *et al.* who made quite an interesting study of the influence of the ionic liquid droplet on the doping mechanism of the hydrogenated surface. They compare all parameters for two scenarios: the pure diamond before provision with ionic liquid and the diamond with an IL droplet, but at 0 V applied to the gate electrode. Their observation was that when placing the droplet on the diamond surface, parts of the adsorbed water responsible for hole accumulation gets dissolved in the IL, leading to a resistance increase of one order of magnitude. In general, −0.342 V applied to the electrolyte-gate reproduces the behaviour without ionic liquid. Consequently, the ionic liquid reduces the effect of the hydrogenation and changes the initial hole concentration on the surface by more than one order of magnitude. The importance of this change might not be very big at first sight as less than −1 V applied to the gate is sufficient to re-establish the initial doping level, but maybe this makes the difference for the ability to reach superconductivity by electrostatic doping.

As it is still not fully understood where charge carrier accumulation takes place in a hydrogen-terminated surface and as it is unknown if the surface treatment changes more than the hole concentration, we cannot be sure that surface superconductivity is generally possible in a hydrogenated diamond. Therefore, we made first tests of field-effect doping on intrinsic diamond with an oxygenated surface which was measured to be highly insulating[1] [213]. We have not been successful so far, but this may be due to many reasons, for instance because our design was not very well adopted to this kind of device[2]. Further efforts could lead to success and should be considered as future projects.

6.2 Silicon

Silicon is the second most abundant element in the earth's crust after oxygen. Monocrystalline Silicon is the most important materials in the semiconductor industry as it constitutes the semi-conducting matrix for integrated circuits. It has also become the most popular material for high power devices due to its thermal stability and high breakdown field. Additionally, despite the indirect bandgap, silicon has become one of the most promising

1 In order to have ohmic contacts, the surface was first highly hydrogenated, followed by lithography, metallisation and lift-off, before performing the ozone treatment for the oxygen-termination of the surface.

2 Contact distances should be kept small, especially they should be smaller than the distance from channel to counter electrode. The latter has to be as big as possible to build up a very high electric field and allow the doping of a highly insulating sample.

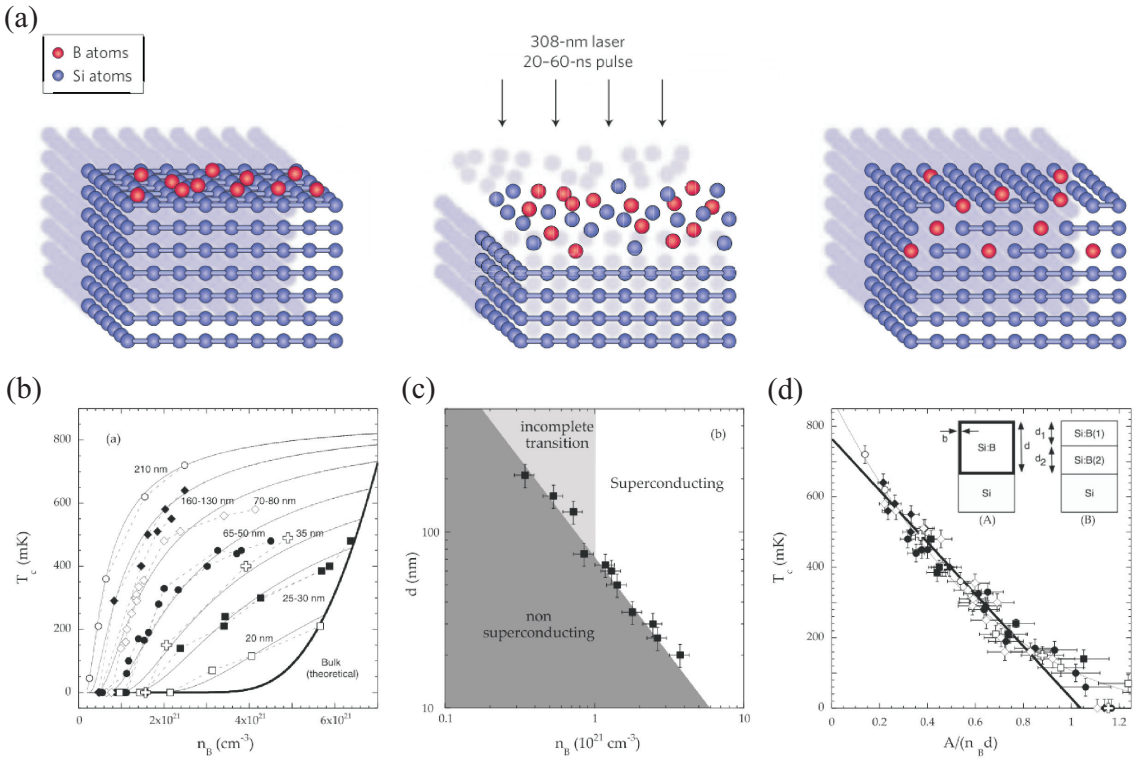

Figure 6.6: (a) Illustration of the laser-assisted intercalation of boron atoms in the silicon matrix. In this technique, BCl_3 gas is chemisorbed on the silicon surface. A laser burst melts the surface of the silicon crystal and the re-solidification is slow enough to allow crystal reconstruction and boron intercalation. From [23] (b), (c), (d) show the thickness dependence of the superconducting critical temperature in heavily boron-doped silicon films, taken from [73]. (b) displays T_c as a function of n_B for samples with varying channel thickness. (c) shows that the critical boron concentration needed for superconductivity (black squares) scales as $1/d$ and (d) shows that T_c is fully determined by the scaling with $1/(n_B \cdot d)$. Symbols correspond to the samples presented in (b).

candidates for light sources, because LEDs made from silicon-based materials can be integrated into the existing microelectronic and optoelectronic technologies in a highly economical way [235].

6.2.1 Doping Mechanism and General Properties of Boron-Doped Silicon

Similar to diamond, the electronic properties of silicon can be modulated by boron intercalation into the crystal matrix. In contrast to the chemical vapour deposition grown doped diamond layers, highly boron-doped silicon thin layers on p-type silicon substrates are realised by gas immersion laser doping. This technique allows to incorporate boron into cubic silicon well above its equilibrium solubility. Fig. 6.6(a) is an illustration of the laser-assisted doping process. The boron is injected box-like homogeneously into a layer thickness d varying from 5 nm to 300 nm. The concentration varies from $6 \times 10^{18}\,\mathrm{cm}^{-3}$ to $6 \times 10^{21}\,\mathrm{cm}^{-3}$. For further details of fabrication see ref. [23, 33, 40].

In the same way as diamond, silicon can be transformed into a superconductor when a critical boron concentration $n_c^S = 5 \pm 2 \times 10^{21}\,\mathrm{cm}^{-3}$ is reached [33]. In contrast to

diamond, the MIT in silicon happens for boron concentrations orders of magnitude below the transition to a superconductor: $n_c^{MIT} \approx 1 \times 10^{18}\,cm^{-3}$ [48]. Critical temperatures stay with 0.03-1.4 K [175] very low and due to the lower electron-phonon coupling, T_c values are lower than in diamond. Similar to diamond, the high boron concentration of several % of the Si atoms (up to 11 % [40]) to a high level of disorder which may degrade superconducting properties [182, 199].

Grockowiak *et al.* studied the thickness dependence of T_c in heavily boron-doped silicon [73] and their main observations are displayed in Fig. 6.6(b)-(d). Panel (b) shows the boron concentration dependence of T_c for samples with thickness ranging from 20 nm to 210 nm. Interestingly, the influence of d remains visible up to the thickest sample investigated, where d is well above the coherence length and/or the electronic mean free path. Panel (c) and (d) show the most surprising results of their work. In (c) the film thickness is plotted versus n_B, whereas black squares indicate the onset of superconductivity n_c^S. It is clearly visible that n_c^S scales as $1/d$. Panel (d) shows that all the $T_c(n_B,d)$ curves, displayed in panel (a), can be rescaled on one single curve, when plotting T_c versus $1/(n_B \cdot d)$. This indicates that the superconducting critical temperature is fully determined by the boron dose $n_B \cdot d$ and can be well approximated by $T_c(n_B,d) = T_{c0}[1 - A/(n_B \cdot d)]$, with $T_{c0} \sim 750$ mK and $A \sim 8 \pm 1 \times 10^{15}\,cm^{-2}$. Finally, Grockowiak *et al.* observed that T_c decreases with decreasing d, but as conductivity is increasing with decreasing T_c and disorder is low ($k_F l \sim 10$), their system with a minimum sample thickness of 20 nm is far from transition to an insulator.

6.2.2 High Surface Doping of Metallic Silicon

High-T_c superconductivity has never been suggested for doped silicon. However, evidence was given that highly doped column-IV sp^3 covalent insulators or semiconductors could be turned into superconductors with T_c exceeding a few kelvin [23].

In order to reduce disorder, it is again of great interest to introduce charge carriers by using field-effect doping. The technique of EDL-gating has been used on silicon for different purposes. One example is the introduction of a very low concentration of carriers into lightly p-doped single-crystal in order to enable nearest neighbour hopping as transport mechanism [1] [148]. Two groups have already tried to find superconductivity in Si by using EDL-gating. One of them in a lightly p-doped substrate with additional hole doping on the surface [149] and the other one in an undoped Si with a hydrogen-terminated surface [182]. Both could see a transition from an insulating state into a metallic state, but were not able to reach n_c^S and did not observe a superconducting transition.

We used samples with an initial boron concentration very close to n_c^S. The goal was to add the residual charge carriers to reach superconductivity by field-effect doping, using

1 Sparse liquid anions form acceptor-like states on the surface between which nearest neighbour hopping takes place.

the technique of EDL-gating. The samples were fabricated by our collaborator Francesca Chiodi, associated professor at the University Paris-Sud, attached to the "Centre de Nanosciences et de Nanotechnologies" (C2N). The sample presented in this section was irradiated by five laser shots which are supposed to induce a charge carrier concentration of about $1.3 \times 10^{20}\,\mathrm{cm}^{-3}$ in a layer of 62 nm thickness, a concentration well above the one needed for a transition from insulator to metal. Consequently, there is no question about obtaining ohmic contacts on the crystal. The sample geometry is a Hall bar, etched into the doped layer in order to be able to precisely determine sheet resistance and resistivity. We provided the sample with ionic liquid before mounting it in the setup.

To verify the concentration of boron atoms, we performed Hall measurements at $T = 200\,\mathrm{K}$ and $V_\mathrm{g} = 0\,\mathrm{V}$. The resulting value of p-type sheet carriers was $n_\mathrm{h} \approx 3.78 \times 10^{12}\,\mathrm{cm}^{-2}$ which corresponds to a 3D carrier concentration of $\approx 6.1 \times 10^{19}\,\mathrm{cm}^{-3}$ (the channel thickness is 62 nm), which is inferior to the expected value with 5 shots. It was shown that the provision with ionic liquid changes surface doping even without any voltage applied to the counter electrode. One reason is that in air a water layer is adsorbed on the sample's surface, which can lead to substrate charging. The ionic liquid dissolves this water layer and might therefore slightly change the electronic properties of the surface [200, 239]. Another reason is the enhanced disorder created by Coulomb scattering due to the large amount of charges near the channel [162]. Both effects are degrading the charge carrier density and could explain n_h being lower than expected.

The sheet resistance as a function of temperature at different negative gate voltages is displayed in Fig. 6.7, with a zoom into the low-temperature part as inset. All curves

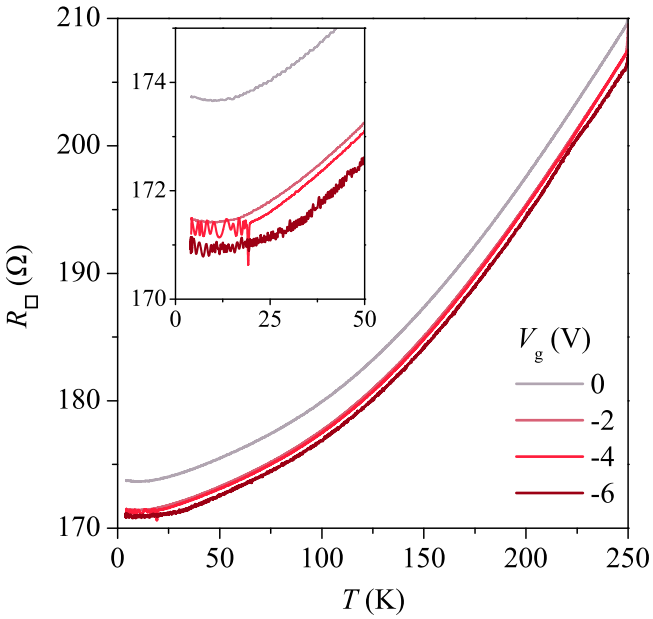

Figure 6.7: Sheet resistance as a function of temperature of boron-doped silicon at different negative gate voltages.

show metallic behaviour, as resistance decreases with decreasing temperature and saturates at low temperatures (T<10 K) or increases very slightly, which might be a sign of weak localisation due to disorder. This confirms the metallic nature of the boron-doped surface expected with a surface treatment of five laser shots. With a negative gate voltage applied, the sheet resistance decreases globally, but changes only about 2% between 0 V and −6 V applied. No hint of a starting superconducting transition is visible.

In this kind of sample with a three-dimensional, metallic conduction channel, additional charge carriers will accumulate only on the surface of the metallic silicon, opening a second conduction channel in parallel to the bulk. We performed Hall measurements at $V_g = -5\,V$, that is at the beginning of the conductance maximum peak, indicated as grey, dashed line in the graph. The extracted sheet carrier concentration n_h is $3.8 \times 10^{14}\,cm^{-2}$, which corresponds to a bulk concentration of $6.13 \times 10^{21}\,cm^{-3}$ when a channel thickness of 62 nm is considered. We have seen before, that the pre-doped bulk concentration is $6.1 \times 10^{19}\,cm^{-3}$, but as the EDL-gating opens a purely two-dimensional conduction channel on the silicon's surface, all additional charge carriers (of the order of $10^{14}\,cm^{-2}$) must be accumulated in this surface channel.

The mobility of our silicon is about $80\,cm^2\,V^{-1}\,s^{-1}$, which is by almost one order of magnitude inferior to published values [182]. This is not astonishing, regarding the high amount of charge carriers accumulated on the sample's surface.

6.3 Conclusion and Outlook

We investigated the two best known group IV semiconductors, diamond and silicon. Both proved to develop superconductivity when sufficiently boron-doped and are even promising candidates for high-T_c superconductivity or at least, in the case of silicon, superconductivity above liquid helium temperature. However, the substitutional intercalation of boron atoms in the crystal matrix increases the disorder in the systems, resulting in reduced critical temperatures and lowered mobilities. We used EDL-gating in order to preserve high doping levels in less disordered systems.

We performed transport measurement on differently pre-doped samples. On the one hand, we analysed highly polished intrinsic diamond substrates with a hydrogen-terminated surface ($n_h \sim 10^{13}\,cm^{-2}$) and on the other hand metallic, but non-superconducting boron-doped silicon layers ($n_B \sim 1.9 \times 10^{20}\,cm^{-3}$). We succeeded in highly doping the surfaces of both crystals and reached 2D charge carrier densities of $1.8 \times 10^{14}\,cm^{-2}$ in diamond and of $3.8 \times 10^{14}\,cm^{-2}$ in silicon. When a conduction channel thickness of 1 nm is considered, the density of accumulated charge carriers in diamond is not sufficient for superconductivity, whereas in silicon, it is just on the edge between the metallic and the superconducting state. However, we did not observe any hint of superconductivity down to 4 K in both materials. What we did observe is a significant gate effect. Diamond made the transition from an insulating state into the state of a dirty metal at low temperatures, where sheet resistance

decreases slightly and charge carrier density increases slightly with decreasing temperature. The lowest sheet resistance achieved is higher than published values of superconducting films. This observation is consistent with the induced charge carrier density which is in-between the critical carrier concentrations for an MIT and for superconductivity.

On the one hand, the diamond's behaviour of a metal in the dirty limit indicates that disorder is still present in the film even without chemical doping. As an explanation, it was shown very recently that an introduction of disorder could stem from the EDL-gating technique, as the large number of charged ions near the channel inevitably results in Coulomb scattering and therefore a reduction of mobility [162]. On the other hand, we reached mobilities ranging from 60-120 $\mathrm{cm^2\,V^{-1}\,s^{-1}}$ at $T = 200\,\mathrm{K}$, which are to our knowledge higher than the highest values reported so far within the same level of charge carrier concentration. Additionally, our Hall mobilities are 20 times higher than reported values in boron-doped, superconducting films, which indicates a strong decrease of disorder when injecting charge carriers via field-effect gating.

In general, surface superconductivity might be possible in both systems, but disorder rather leads to a suppression of superconductivity in reduced dimensionality. Disorder can be reduced by adding a thin protection layer (e.g. a few-layer boron nitride flake) between channel and ionic liquid [162], which would furthermore - for the right choice of material - act as a protection from electrochemical reactions and would therefore allow the application of higher gate voltages leading to higher charge carrier concentrations.

The ability to inject high amounts of holes into metallic silicon arises the motivation for investigating the sample at $T < 4\,\mathrm{K}$. At the same time, this indicates the possibility of T_c modulation in superconducting films via field-effect gating, as it was done in high-T_c superconductors [26, 51, 114] and in the amorphous superconductor indium oxide [112].

In the case of diamond, there is another incertitude which is the general ability of the hydrogenated surface to become superconducting. Therefore, another system might be worth further investigation, which is intrinsic diamond with an oxygen-terminated, insulating surface. It should be possible to preserve ohmic contacts, by keeping hydrogen-termination underneath the contacts. We are confident that it is possible to reach critical carrier concentration for superconductivity in diamond when the contacts are protected from electrochemical reactions.

CHAPTER 7

Ion Gel Gating

An ion gel is a polymer matrix which contains ionic liquid. The gel is stable in ambient conditions, has a rubber-like elasticity and the liquid ions are mobile inside the polymer, but the gel is not electrically conducting. This makes the gel a squashy but solid dielectric for high charge carrier doping.

In this chapter, a new type of ion gels with cations fixed on one surface of the gel and mobile anions will be presented. First, the advantages and the utility of ion gels in general will be discussed together with some historical aspects, followed by the ideas behind the fabrication and use of an ion gel with fixed cations as gate dielectric. Then, the fabrication of such gels will be explained briefly.

With this ionic tool as dielectric we created a new type of field-effect diode. The principle and functionality of this new field-effect device will be demonstrated, using a strontium titanium oxide ($SrTiO_3$) substrate as device material. Additionally, the general dielectric performance of the cation-fixed ion gel will be presented and compared with the published characterisation of ionic liquid-gated $SrTiO_3$ substrates. We will show that the ion gel has almost the same gating capabilities as an ionic liquid.

7.1 History and Motivation

All previous chapters focused on the advantageous abilities of ionic liquids when used as gate dielectrics. These are high ionic conductivity, large specific capacitances and therefore the capability to reduce threshold voltages drastically, wide electrochemical windows, the ability to form a conduction channel with up to $\approx 1 \times 10^{15}\,\mathrm{cm}^{-2}$ charge carriers, negligible vapour pressure, non-inflammability and favourable chemical and thermal stability [80, 246]. Amongst others, strong charge carrier accumulation due to ionic liquids had led to field-induced electronic phase transitions and ionic liquids has also successfully been applied to organic single-crystal devices [246].

However, the instability of the liquid body, the possible electrochemical reactions at high gate voltages and the absorption of water and other impurities set limitations to practical use. A big part of these problems can be solved by the gelation of ionic liquids. Thereby,

the ionic liquid gets embedded in a solid matrix of base matter to gain a gel-like and stable film in which liquid ions can move freely.

First attempts were made more than 20 years ago, but the results were not very satisfying as the fabricated gels were either not stable in ambient conditions or showed very poor gate dielectric performance [116]. A big improvement was achieved by the use of polymers as base matter for solid systems containing ionic liquids. The first success in building such ion gels with reasonable gating performance was the polymerisation of ionic liquids [152] and the doping of polymers with ionic liquids [116]. Improvement came through the self-assembly of a triblock copolymer in a room-temperature ionic liquid, a technique which requires significantly less polymer and offers improved ion conductivity [80, 109]. High ion conductivity is very important as it defines the polarisation time in an EDL-gated transistor and therefore determines the switching frequencies of the transistor [159].

After this last improvement, ion gels were used in various devices. The group of C. D. Frisbie realised printed ion gel-gated transistors and integrated circuits with very promising performance [111, 233] and sub - 1 V, flexible displays on plastic [141]. Several approaches to flexible electronics and solar cells exist, e.g. [167]. The ion gels containing a triblock copolymer and ionic liquid are not the only ion gels that are printable and have excellent gating performance. For instance, Thiemann *et al.* fabricated spray-coatable ion gels based on silane-ionic liquids with high capacitances ($\leq 10\,\mu F\,cm^{-2}$) [215]. In these gels, cations are involved in the network formation and only anions are mobile. Consequently, these ion gels cannot be used for ambipolar charge injection.

It proved to be very difficult to fabricate ion gel thin films with molecular flatness. In all the examples mentioned above the ion gel was fabricated directly on the semiconductor, a process that limits the choice of materials to those which resist organic solvents. The thickness of the dielectric film is important: a thinner film means a faster response speed, which is mandatory for high-speed EDL electronics. Only recently, Yomogida *et al.* succeeded in fabricating molecularly flat (roughness of $\approx 0.3\,nm$), sticky and rubber-like ion gel thin films with specific capacitances which almost reach those of ionic liquids [246].

The knowledge of producing ion gel films opens the door to other field-effect tools. For instance, one type of ions can be integrated in the polymer matrix to be fixed in a specific area inside the solidified body of the gel. Our collaborator Shimpei Ono (researcher in CRIEPI, Yokosuka, Japan) provided us with an ion gel with cations fixed on one surface of the gel and anions still able to move freely through the film. With this kind of film we succeeded in fabricating a two-terminal field-effect diode, which is very easy to fabricate and has a very low power consumption. Those devices do not suffer from off-state leakage current, and nanoscale devices with high performance are conceivable.

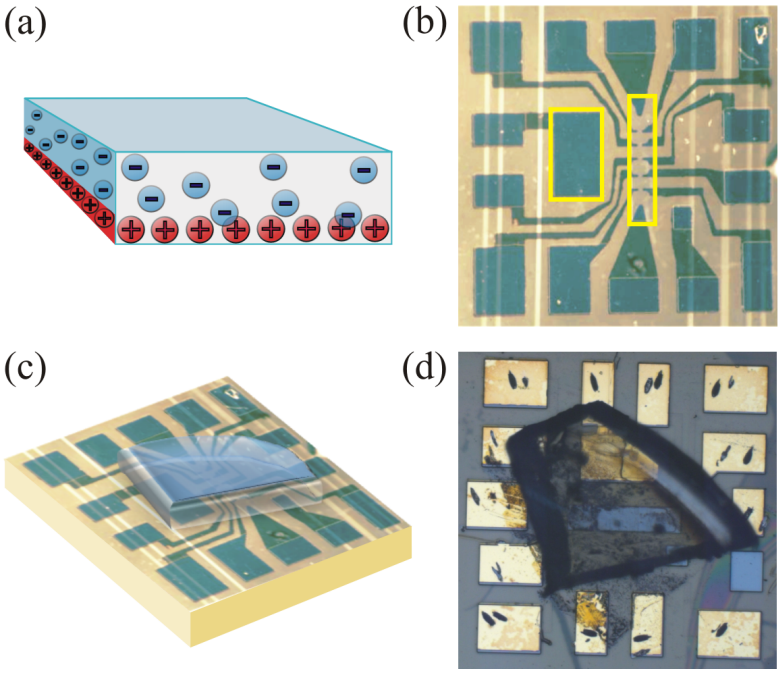

Figure 7.1: (a) Schematic drawing of an ion gel with the cations fixed on one surface of the gel. The anions can move freely as if in a highly viscous liquid. (b) Optical image of a $SrTiO_3$ sample with metallic contacts and a protection layer of photo resist which covers the contact lines and leaves the conduction channel, the counter electrode and the bonding pads accessible. The counter electrode, which serves as gate electrode, and the conduction channel are indicated by yellow rectangles. (c) Schematic drawing of a $SrTiO_3$ sample with a piece of ion gel placed on it. The gel entirely covers both the conduction channel and the gate electrode. (d) Optical image of the device covered by an ion gel film.

7.2 Fabrication and Technique

The ion gel with fixed cations is based on a polymer and a room-temperature ionic liquid with unsaturated bonds on the cations. It was fabricated in the Central Research Institute of Electric Power Industry (CRIEPI), Yokosuka, Japan. The ingredients are polymers, polymerisation initiator and an ionic liquid with unsaturated bonds on the cations. They were mixed and sandwiched in-between two electrodes made of gold and indium tin oxide. An electric field of 5 V was applied between the two electrodes that separated the liquid ions. Shining a UV light on the mixed substances connected the cations to the polymer matrix. Due to the external field applied, the cations are fixed on the surface closest to the anode. The anions stay pristine during the whole solidification process and are able to move freely through the gel as if in a very viscous liquid when the external field is removed. They will mix up with the localised cations in order to regain charge neutrality. A schematic drawing of the ion gel is presented in Fig. 7.1(a). The gel is a rubber-like, sticky and transparent film of about 0.5 mm thickness. The gel has to be manipulated by a non-conducting tool to avoid discharging effects.

Our samples are substrates of the semiconductor $SrTiO_3$, which possess a bandgap of 3.25 eV [16]. The contacts on the $SrTiO_3$ substrate were defined by standard optical

lithography followed by electron beam evaporation of chromium and gold. The design is a Hall bar with five pairs of Hall contacts. A counter electrode, which is acting as the gate electrode for applying an external field to the gel, was added in the same step. A second photo lithography served to open a window for the doping region and to protect the contact lines with photo resist. Fig 7.1(b) shows the optical image of a $SrTiO_3$ sample after the second lithography. The conduction channel and the gate electrode are highlighted by yellow rectangles.

The ion gel was placed - cations facing down - on the centre of the sample so that it entirely covers both the conduction channel and the counter electrode. Fig. 7.1(c) and (d) show a schematic drawing and an optical image of an $SrTiO_3$ sample with a piece of the ion gel placed on top of it. Four FET devices were prepared in the same way and measured with an Agilent B2902A DC source measurement unit. Measurements were performed in two- and four-probe configurations, which will be described more precisely in the text.

7.3 $SrTiO_3$ Field-Effect Diode

A field-effect diode (FED) is a pn-junction diode, where the p- and n-doped regions are formed via field-effect by two local topgates on the channel [173, 191]. Fig. 7.2(a) shows the schematic drawing of a standard silicon FED with chemically n- and p-doped source

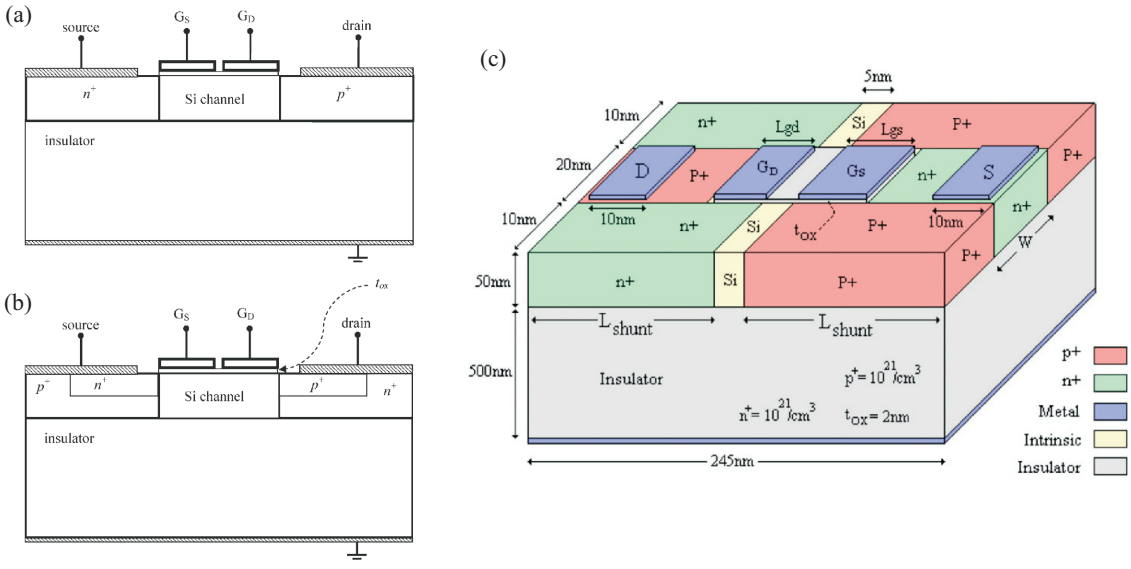

Figure 7.2: (a) Schematic drawing of the first proposed field-effect diode. The silicon layer underneath the source and drain electrodes is n- and p-doped respectively, the intrinsic channel can be locally doped in two areas by two separate topgates G_S and G_D. (b) Schematic drawing of the modified FED with source and drain both n- and p-doped. (a), (b) taken from [192]. (c) 3D drawing of the modified FED with the strongly doped regions at source and drain in the same plain, taken from [65].

and drain area[1] and the two topgates G_S (on the same side as the source) and G_D (on the same side as the drain) above the intrinsic silicon channel. A thin insulating layer between the channel and the topgates acts as dielectric. When a negative voltage is applied to G_S and a positive voltage to G_D, the diode is in its on-state with a n-n-p-p channel configuration. The output characteristic is that of a forward biased diode. In the case of inversely applied topgate voltages, the diode is in its off-state with a n-p-n-p channel configuration, which is the off-state of a thyristor [191].

A Field-effect diode can provide on-state currents of up to two orders of magnitude larger than a comparable MOSFET[2], because pinch-off, the limiting factor in a MOSFET, does not occur. Large on-state currents imply high I_{on}/I_{off} ratios which define the switching efficiency and additionally, these currents are sufficiently high for high frequency operation. FEDs were proposed to be used as active elements in novel high-speed circuits. Simulations have shown that these circuits are 1-2 orders of magnitude faster than conventional circuits [191]. Another application suggested is the use of FEDs in devices for electrostatic discharge protection [181].

In general, FEDs as basis of digital circuits have a great potential to improve speed, power

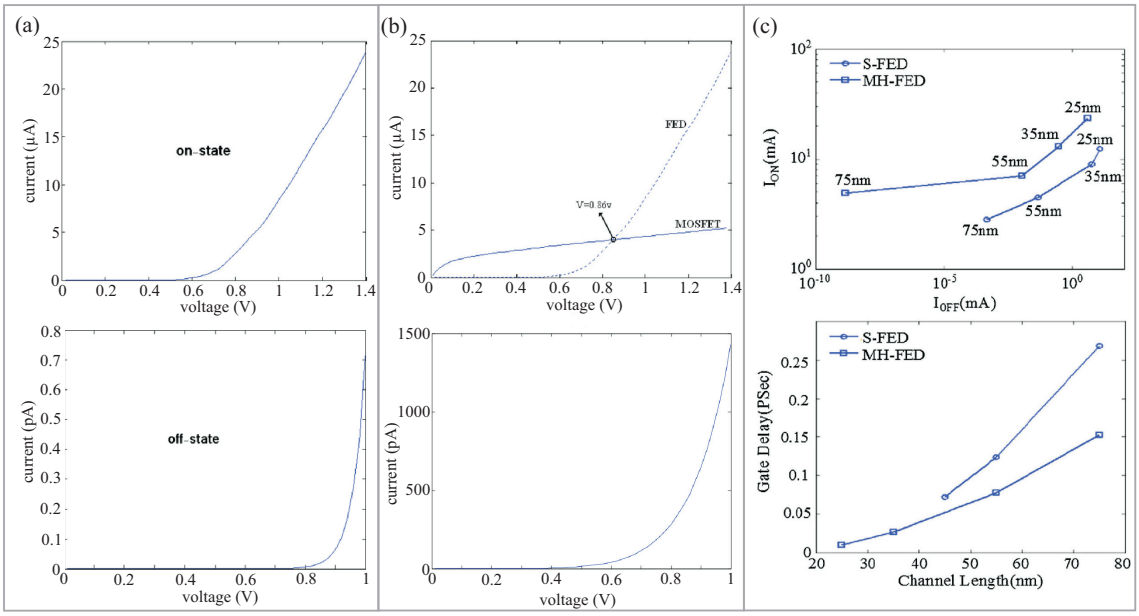

Figure 7.3: (a), (b) Simulated output characteristics of a modified FED and a MOSFET respectively. Both devices have a length of 75 nm. In each case, on-state and off-state characteristics are presented. Adopted from [65]. (c) I_{on} versus I_{off} for different channel lengths and the gate delay as a function of channel length, in both cases for a modified FED (labelled as S-FED) and an even more complex design of a FED (labelled as MH-FED) in comparison, taken from [220].

1 The doping of the area underneath the metal electrodes is important in order to form Schottky-barrier free, ohmic contacts.

2 The comparison was made with a MOSFET using the technology silicon-on-insulator (SOI), which is the technology needed for fabricating a FED.

consumption and size. To achieve high I_{on}/I_{off} ratios in FEDs with a channel length <100 nm, the standard FED design shown in Fig. 7.2(a) is not appropriate, as the injection of excess minority carriers interferes with the normal operation of the device and the FED does not turn off[1]. A new design proposed by Sheikhian and Raissi [192] is shown in Fig. 7.2(b). Their simulations show a great improvement in the I_{on}/I_{off} ratio, due to a significant increase of the off-state current, evoked by added shunts under the source and drain electrodes, which act as short path for minority charge carriers between the channel and the electrodes[2]. However, the fabrication of this design is rather difficult and an improved design was suggested by the same group four years later [65], which is shown in Fig. 7.2(c). The general idea is the same, but the shunts are in the same plain as the channel and the other doped regions and the fabrication is compatible with standard CMOS processes.

The performance of this improved 3D-FED simulated by Gatabi and Raissi [65] is displayed in Fig. 7.3(a) and (b): the output characteristics in both on- and off-state of a FED and a MOSFET are shown respectively. The on-state current of the FED increases above that of a MOSFET for $V_{DS} > 0.86\,V$ and the output impedance is much smaller. The off-state current of the FED is more than three orders of magnitude smaller than that of the MOSFET so that I_{on}/I_{off} ratios are up to five orders of magnitude higher than in a MOSFET.

Later on, even higher performance was achieved by Vadizadeh [220], using a more complex design with heavily doped layers in the channel and a strain applied to it. Fig. 7.3(c) shows simulations of I_{on} versus I_{off} for different channel lengths and the gate delay as a function of channel length, each time for a modified FED (labelled as S-FED) and the new complex FED (labelled as MH-FED) in comparison. With regard to the speed, short devices show better performance in both device types. However, high I_{on}/I_{off} ratios for channel lengths shorter than 75 nm were only achieved in the complex MH-FED.

Here, we propose a new design for a field-effect diode, using the ion gel described in section 7.2. To better understand the field effect when an ion gel with fixed cations and mobile anions is used as gate dielectric, we will first describe the functionality of this gel. The mobile anions move under any electric field in the vicinity of the gel and can therefore be manipulated by an applied gate-source voltage V_g or drain-source voltage V_{DS}. Fig. 7.4(a) shows the schematic drawings of the ion gel configurations for different values of V_{DS} and V_g. Without any voltage applied the anions mix with the cations on the surface to obtain charge compensation (see Fig. 7.1(a)). Consequently, when the gel is placed on the sample,

1 Excess minority charge carriers injected from source and drain into the channel increase the electron and hole concentration in the p-doped region (under G_S) and the n-doped region (under G_D). In devices with channel length >100 nm, these injected carriers recombine before reaching the other gate. For short-channel devices, the excess minority carriers can reach under the second gate and turn on the device.

2 To realise these shunts, source and drain have to be both highly n- and highly p-doped. The layer doped in the same polarity as the respective excess minority charge carriers will retract those from the channel.

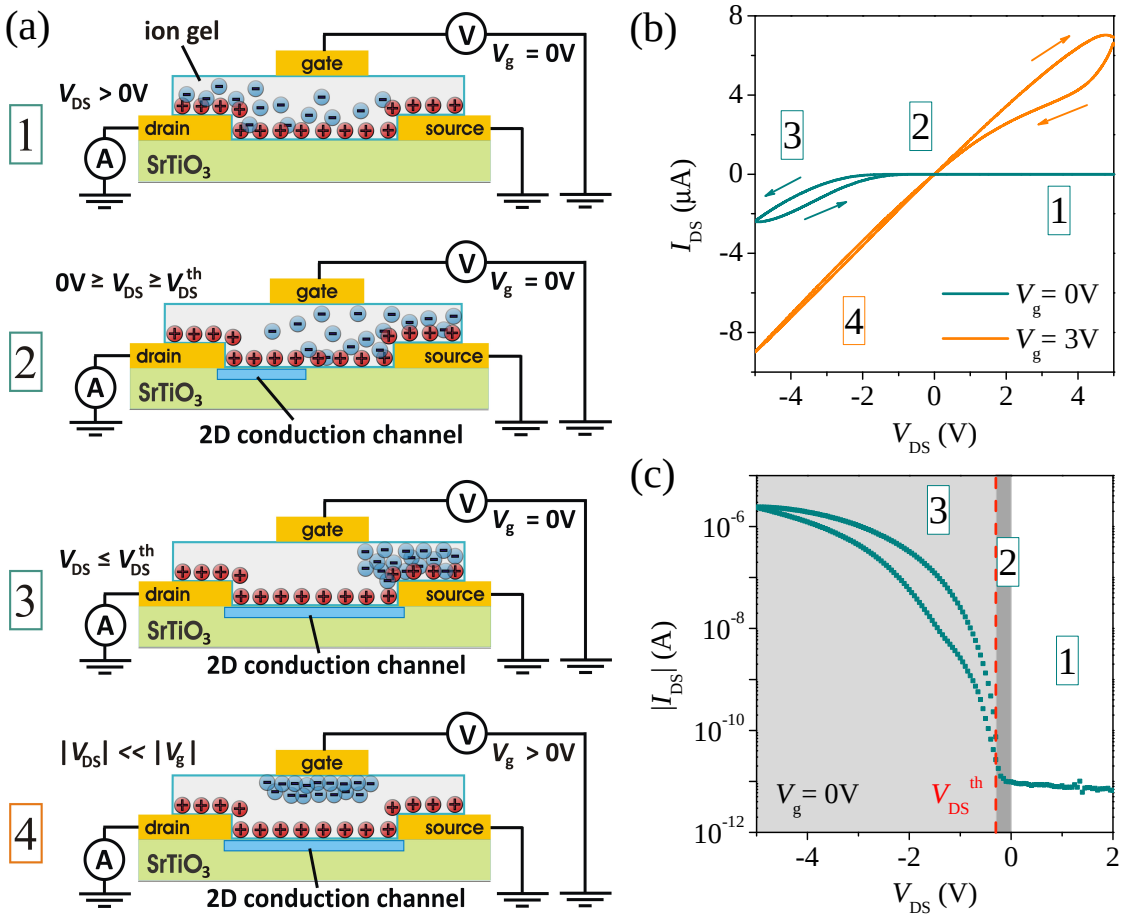

Figure 7.4: (a) Schematic drawings of four cases of different ion configurations in the gel due to different negative drain-source voltages V_{DS} applied (1)-(3) and in the case of a positive gate voltage $V_g \geq V_{DS}$ applied. The four cases are indicated in the measurements shown in (b) and (c) in the appropriate places. (b) Transistor output characteristics measured at $V_g = 0\,V$ (green) and $V_g = 3\,V$ (orange). (c) Absolute value of I_{DS} at $V_g = 0\,V$ as a function of V_{DS} in logarithmic scale. The current increases by more than five orders of magnitude below a negative threshold voltage $V_{DS}^{th} = -0.3\,V$.

the 2D conduction channel on the $SrTiO_3$'s surface will not be established immediately. When a positive drain-source voltage is applied, anions will be accumulated around the drain electrode and even for high V_{DS} values, there will always be some anions on top of the channel region very close to the drain electrode, interrupting the channel formation. This case is displayed in panel (1).

Panel (2) and (3) show the progressive formation of a surface conduction channel when the gate voltage is kept zero and only a negative drain-source voltage is applied. The negative V_{DS} will repulse the anions inside the gel and little by little the cations on the gel's surface will be isolated from the anions. An electric field on the gel/device interface is established progressively, starting from the drain electrode, and with it electron injection begins. Once a certain drain-source threshold voltage V_{DS}^{th} is reached, a conduction channel is built up on the device's surface, as shown in panel (3). The more obvious technique to form the

conduction channel is the familiar method of using a gate. Panel (4) shows the situation of a small drain-source and a positive gate voltage applied with $|V_g| \gg |V_{DS}|$[1]. The positive gate voltage attracts the anions and depletes them from the channel region in order to allow the creation of a 2D conduction channel on the $SrTiO_3$'s surface by electron injection from the metal contacts.

The way of ion formation just described is directly visible in the current response in the transistor transfer characteristics. Fig. 7.4(b) shows the IV characteristics with $V_g = 0\,V$ in green and with $V_g = 3\,V$ in orange at $T = 255\,K$. Both forward and backward sweeps are displayed and a hysteresis is visible, which is due to the slow motion of the anions. Fig. 7.4(c) shows the absolute value of I_{DS} at $V_g = 0\,V$ as a function of V_{DS} in logarithmic scale. The four cases illustrated in (a) are indicated in the plots and partly clarified as grey areas. When the output characteristic at $V_g = 0\,V$ is regarded, at positive V_{DS} no current passes through the $SrTiO_3$ and the device is insulating (case (1)). When V_{DS} reaches the negative threshold voltage $V_{DS}^{th} = -0.3\,V$, the current increases steeply by more than five orders of magnitude (case (3)), clearly to be seen in panel (c). This is the exact behaviour of a semiconductor diode with a negative V_{DS} as forward bias.

Indeed, Fig. 7.4 shows that we succeeded in creating of a novel type of field-effect diode in which the drain-source field alone is sufficient to switch on and off the diode. We named the diode drain-source field-effect diode (DS-FED). Consequently, the device is based on two terminals (source and drain) and neither a backgate and nor local gates are needed. Fabrication is much simpler than that of any FED design proposed so far. Off-state currents in our device are extremely low as in the off-state, there are always parts of the channel undoped and therefore highly insulating. Thus, very high I_{on}/I_{off} ratios are expected in a DS-FED. The design, the fact that only one applied voltage is needed and the low threshold voltage indicate that the DS-FED is a very promising candidate for low cost and low power-consuming devices.

A DS-FED might also be a candidate for nanoscale devices. Restrictions for ever lower dimensions are mostly given by the size of the ions in the ion gel. A homogeneous cation distribution in the gel above the channel is necessary and anions need to be able to mix with the cations in order to switch off the device. A design with source, drain and channel in the same plain would increase the quality of the interface between ion gel and channel, as in a nanoscale limit, if the contacts are higher than the channel region, the ion gel must be very flexible in order to obtain good gel/channel and gel/metal interfaces. In this case, channel lengths of few tenth of nm are conceivable.

We have to assure that the current increase at $V_g = 0\,V$ and $V_{DS} < 0\,V$ is not caused by a different effect than the suggested one. Electro-chemical reactions can be excluded, as

1 $|V_{DS}| \ll |V_g|$ has a negligible effect on the anions. However, when V_{DS} is of the order of V_g, an interplay of the two electric fields is present and the anions' formation is intermediate of those presented in panel (3) and (4).

all measured devices show similar, reproducible and reversible FET output characteristics and gate leakage currents stayed below 200 pA. It is still important to prove that the gel is composed in the way we want, which means that the cations are completely stable on the gel's surface and only anions move through the gel when an electric field is applied. Therefore we focus on the FET output characteristic with $V_g = 3\,V$ applied (orange curve in Fig. 7.4(b)). The IV characteristic is ohmic in forward direction and only deviates from a straight line when V_{DS} exceeds V_g. The backward sweep deviates strongly from a straight line for $V_{DS} > 0.5\,V$ and is otherwise almost linear. This hysteresis is again due to the slow motions of the anions. When the value of V_{DS} equals the value of V_g, there are two effects which compete with each other, the attraction of anions by the gate electrode on the one hand and by the source electrode on the other hand. This explains the depression of I_{DS} when $V_{DS} \geq V_g$. The absence of such depression of I_{DS} at negative V_{DS} values proves that cations are integrated in the polymer matrix. If they were not fixed inside the gel, they would be attracted by the negative drain-source voltage applied and accumulate on the drain electrode. The conduction channel would be interrupted, starting from the source electrode, which would cause a decrease of I_{DS}. The demonstration that cations are located on the gel's surface will be given in the next section.

7.4 Ion Gel Field-Effect Performance

The main application foreseen for ion gels is the use as EDL dielectric for high charge carrier injection in order to reach charge carrier densities comparable to those achieved with ionic liquids. We investigated the general gating performance of our cation-fixed ion gel on the same $SrTiO_3$ sample we used for the DS-FED.

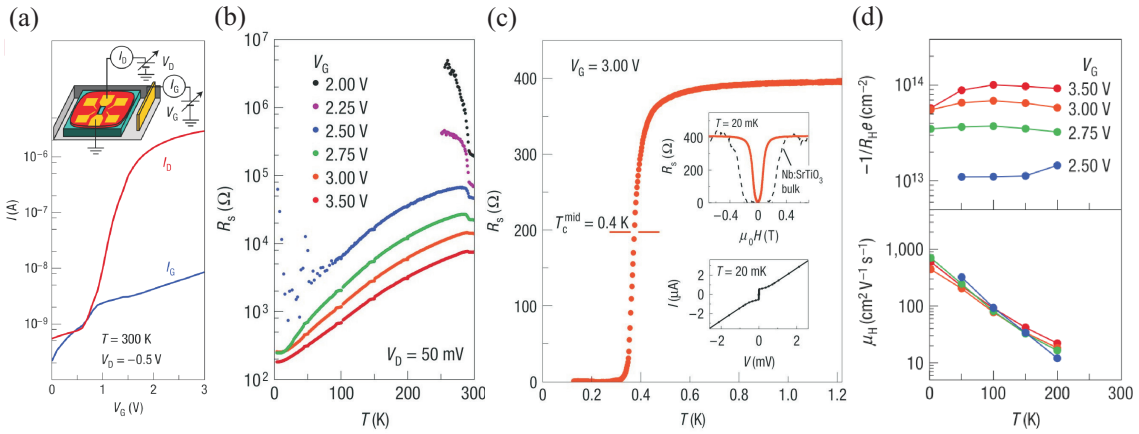

Figure 7.5: Comparison with literature: ionic liquid-gated $SrTiO_3$ FET measured by [217]. (a) Transistor transfer characteristic (red) and leakage current (blue) measured in two-probe configuration (see schematic drawing in the inset). (b) Sheet resistance versus temperature for different ionic liquid-gate voltages applied. (c) Temperature dependence of the sheet resistance at $T < 2\,K$ with $V_g < 3\,V$ applied, measured in four-probe configuration. At a critical temperature of 0.4 V the $SrTiO_3$ becomes superconducting. (d) Results of Hall measurements: temperature dependence of sheet carrier density and mobility.

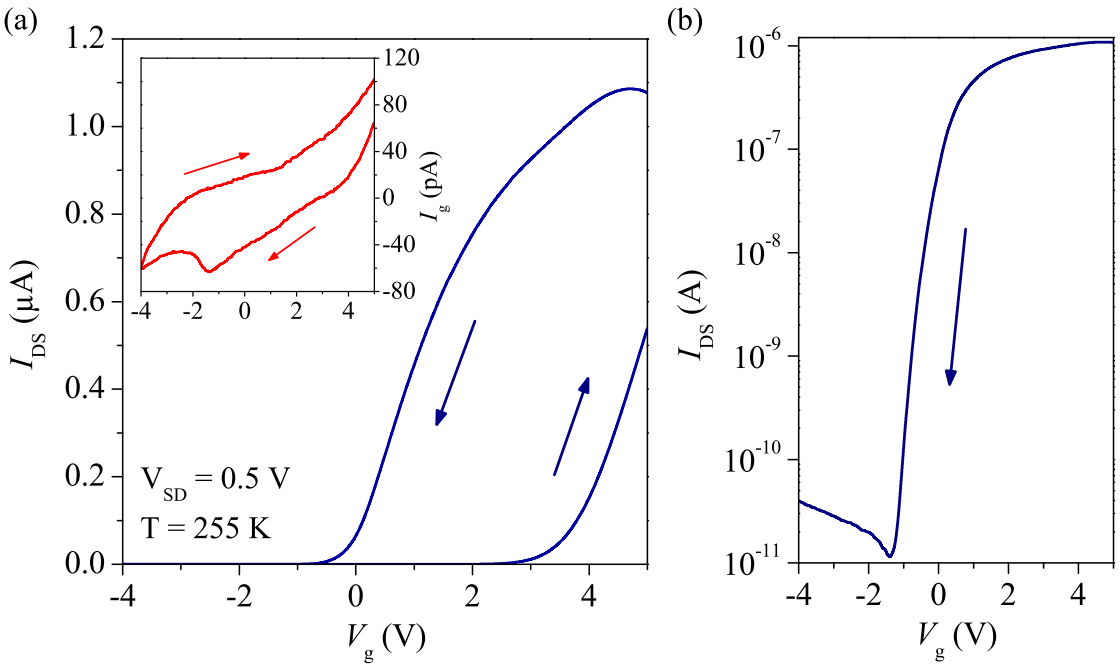

Figure 7.6: (a) I_{DS} as a function of V_{g} in forward and backward sweep direction, plotted in linear scale. The hysteresis is due to the slow motion of the anions in the gel. The inset shows the leakage current measured at the same time as I_{DS}. (b) Backward sweep of the same data in logarithmic scale to point out the current increase of almost five orders of magnitude by electron doping.

As a matter of fact, the first field-effect induced superconductivity into an insulator via ionic liquid-gating was observed in $SrTiO_3$ by Ueno *et al.* [217]. They succeeded in inducing surface charge carrier densities up to $1 \times 10^{14}\,\mathrm{cm}^{-2}$, which are by one order of magnitude higher than in conventional FETs. Fig. 7.5 is a summary of their observations. Panel (a) shows the drain-source current (red) and the gate leakage current (blue) as a function of gate voltage at $T = 300\,\mathrm{K}$. A clear transition from off- to on-state with an $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratio of more than three orders of magnitude is visible, while the gate leakage current stayed below 10 nA for the entire V_{g} range. (b) shows the temperature dependence of the sheet resistance for different gate voltages. An insulator-to-metal transition is visible as metallic states appear for $V_{\mathrm{g}} \geq 2.5\,\mathrm{V}$. A superconducting transition emerged for applied gate voltages $V_{\mathrm{g}} \geq 2.7\,\mathrm{V}$. The superconducting transition for $V_{\mathrm{g}} \geq 3\,\mathrm{V}$ is displayed in Fig. 7.5(c). Panel (d) shows the parameters obtained by Hall measurements: the sheet carrier density $n_{2\mathrm{D}} = -1/R_{\mathrm{H}}e$ and the Hall mobility μ_{H}. While $n_{2\mathrm{D}}$ is almost temperature independent, μ_{H} steeply increases with decreasing T. The gate voltage dependence is inverse, μ_{H} is almost independent of V_{g}, whereas $n_{2\mathrm{D}}$ increases with V_{g}. The charge carrier density at $V_{\mathrm{g}} \geq 2.7\,\mathrm{V}$ and therefore the one needed for superconductivity is $\approx 3 \times 10^{13}\,\mathrm{cm}^{-2}$.

We will now discuss the gating performance of the cation-fixed ion gel and compare the results with the ones just shown. Fig. 7.6 shows the drain-source current as a function of gate voltage measured with a bias voltage of 0.5 V and at a temperature of 255 K.

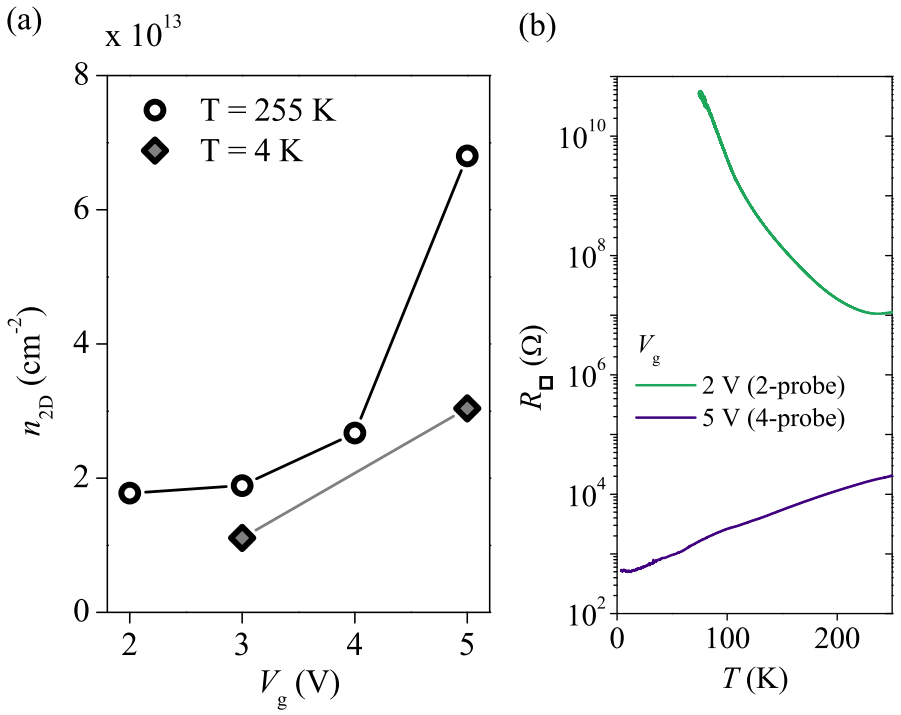

Figure 7.7: (a) Charge carrier densities obtained by Hall measurements at $T = 255\,\mathrm{K}$ (circles) and $T = 4\,\mathrm{K}$ (diamonds) for different positive gate voltages applied. (b) R versus T in three different configurations. The two upper curves are measurements in two-probe configuration for an applied gate voltage of 2 V and 5 V, respectively. The lowest curve was measured in four-probe configuration with an applied gate voltage of 5 V.

In (a) both forward and backward sweeps are displayed in linear scale and in (b) the backward sweep is shown in logarithmic scale. The measurement was done in two-terminal configuration, sweep directions are indicated by arrows. Between forward and backward sweep a huge hysteresis is present, which is due to the slow motion of the anions in the gel. Note here that the sweep velocity is with $5.6\,\mathrm{mV\,s^{-1}}$ rather high. Compared to the detailed analysis of the influence of sweep velocity in the case of ionic liquid-gating presented in section 4.2.2, a hysteresis is expected. It was shown that hysteresis only vanishes for sweep velocities $<2\,\mathrm{mV\,s^{-1}}$. With regard to the forward sweep, as long as $V_\mathrm{g} < 0\,\mathrm{V}$ no current passes through the device until at $V_\mathrm{g} \approx 2\,\mathrm{V}$ the current increases. This is the moment when electrons start to get injected from the metal contacts into the $SrTiO_3$ surface, creating a 2D conduction channel as illustrated in Fig. 7.4(a) case (4). The off-current of our transistor is with some tenth of pA in the noise ground of the measurement unit and the $I_\mathrm{on}/I_\mathrm{off}$ ratio reaches almost five orders of magnitude. The inset of Fig. 7.6(a) shows the gate leakage current which hardly exceeded 100 pA. Such low leakage and off-state currents and the high $I_\mathrm{on}/I_\mathrm{off}$ ratio show improvement compared to the ionic liquid-gated FET of [217].

We performed four-terminal Hall measurements at two different temperatures and extracted the sheet charge carrier densities n_2D. Fig. 7.7(a) shows n_2D at 255 K (circles) and at 4 K

(diamonds) for different gate voltages applied. Note that the liquid ions in the gel freeze at a temperature of $\approx 220\,\mathrm{K}$. Therefore, we wormed up the sample after each measurement in order to change the gate voltage at temperatures superior to the freezing temperature of the ion gel (250 K). High temperature charge carrier densities of almost $7 \times 10^{13}\,\mathrm{cm}^{-2}$ for highest doping were reached. $n_{2\mathrm{D}}$ increases with increasing V_g and decreases with decreasing temperature. Hall mobilities of $7\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ at $T = 255\,\mathrm{K}$ and $400\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$ at $T = 4\,\mathrm{K}$ were reached, whereas the longitudinal sheet resistance values needed for the calculations were extracted from IV measurements in 4-probe configuration. Fig. 7.7(b) shows the sheet resistance versus temperature at $V_\mathrm{g} = 2\,\mathrm{V}$ in 2-probe configuration and at $V_\mathrm{g} = 5\,\mathrm{V}$ in 4-probe configuration. While the $SrTiO_3$ is insulating at $V_\mathrm{g} = 2\,\mathrm{V}$, it shows clear metallic behaviour at $V_\mathrm{g} = 5\,\mathrm{V}$ as the resistance increases with temperature by almost two orders of magnitude. Our mobility values are only slightly lower than the values presented by Ueno *et al.* and our extracted values for $n_{2\mathrm{D}}$ are of the same order of magnitude than theirs. At low temperature, the 4-probe sheet resistance at $V_\mathrm{g} = 5\,\mathrm{V}$ is $\approx 500\,\Omega$, which is of the same order of magnitude as the sheet resistance of the ionic liquid-gated $SrTiO_3$ just before the superconducting transition. These observations suggest that it is possible to induce superconductivity into $SrTiO_3$, using our ion gel as gate dielectric. The comparison of all measurements presented in this section with the results from literature shown above prove that our cation-fixed ion gel has gating abilities comparable to those of an ionic liquid. At the same time, the ion gel is a solid dielectric, stable in ambient conditions and easy to handle. The only restriction we have to accept with this non-liquid EDL tool is a low ion conductivity reflected by the large hysteresis in Fig. 7.6. But as our gel is the first success in producing such a type of ion gel, there is still room for improvement.

7.5 Conclusion and Outlook

We successfully fabricated a new type of ion gel film based on a polymer with the cations fixed on one surface of the film and the anions able to move freely through the gel. This cation-fixed ion gel used as gate dielectric offers a new design for a field-effect diode. We named this diode drain-source field-effect diode (DS-FED) as the drain-source voltage alone is sufficient to switch on and off the device and no pre-doping of the channel is needed. The diode's quality is promising as off-currents are with $\leq 10\,\mathrm{pA}$ very low and $I_\mathrm{on}/I_\mathrm{off}$ ratios of $> 10^5$ were reached. Additionally, this device shows potential to be scaled down to ever smaller dimensions without a loss of quality. The two-terminal nature and the low off-currents show that we created a low power-consuming device.

Besides the new type of diode, we built an n-type FET, using this gel as gate dielectric. The transistor performance and therefore the gating abilities of the ion gel are quite good with $I_\mathrm{on}/I_\mathrm{off}$ ratios of almost 10^5, a low temperature mobility of $400\,\mathrm{cm}^2\,\mathrm{V}^{-1}\,\mathrm{s}^{-1}$, induced charge carrier densities of up to $7 \times 10^{13}\,\mathrm{cm}^{-2}$ and both off-state and gate leakage currents

of less than 100 pA. Therefore, the gating performance of the gel presented in this chapter is very close to that of an ionic liquid without the problem of instability of the liquid body. The only restriction is a low ion conductivity, but improvement in the gel composition might still be possible.

After the success in fixing one type of ions in a defined area in the gel, new ideas with different ion formations in the film arise. A next step could be to fix the anions on the opposite surface of the ion gel film in order to create an in-built electric field, a so-called electret. Applications are vast, as this leads to mechanical doping, which is "doping by sticking". Semiconductors could be pre-doped to set the Fermi energy just below (above) the conduction (valence) band and further charge carrier accumulation (depletion) could be done by the modulation of the backgate voltage. This enlarges the choice of materials for high-speed transistors with low consumption to those of larger bandgaps. The knowledge of how to fix the two types of ions accumulated in the gel separately is still missing and research is going on.

Summary and Perspectives

In this work we focused on one specific utility of room temperature ionic liquids: their use as ultra-high-capacitance dielectrics in field-effect transistor devices. We used this technique of electric double layer-gating (short EDL-gating) to fabricate state-of-the-art nano-devices which were either field-effect transistor, light-emitting transistor or field-effect diode. The material widest studied in this work consists of multi-walled WS_2 nanotubes which are part of a family of very promising semiconductors with high crystal quality and remarkable mechanical and electric properties: transition metal dichalcogenides (TMDC).

A great capability of ionic liquids as gate dielectric is the possibility to dope a surface with any spatial extension as long as it can be covered by an ionic liquid droplet. Therefore, nano-objects which have a geometry other than flat can easily be manipulated electrostatically by an electrolyte, where a solid fails. We successfully fabricated EDL-gated field-effect transistors based on multi-walled WS_2 nanotubes and observed high-performance ambipolar transistor behaviour. In our best operating devices, both electron and hole mobilities are with $80\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ as high as highest reported values in thin film transistors of the same material. I_{on}/I_{off}-ratios are with $\geq 10^5$ and $\geq 10^6$ for hole and electron doping respectively nearly as high as highest reported values. Our subthreshold swings are in average higher than lowest published values, but our best samples come very close to best performing WS_2 thin film transistors.

We demonstrated the distinct drawback of a solid backgate in comparison to an ionic liquid topgate when gating other than plane materials. Therefore we compared two transistor transfer characteristics performed on the same nanotube, one using the ionic liquid topgate and the other one using the Si/SiO_2 (285 nm) backgate. Both gating techniques are generally working as we observed equal intrinsic mobilities, however, subthreshold swings were increased by a factor 45 in the topgate sweep and ambipolar operation as well as high I_{on}/I_{off}-ratios were only found when using the EDL-gating technique. In terms of power consumption as well, the topgated device outperforms the backgated one largely as 20 V applied to the silicon gate correspond to 0.2 V applied to the ionic liquid.

In an EDL transistor device, it is possible to create a purely electrostatically induced pn-junction by applying the right combination of drain-source and gate-source voltages. We succeeded in creating a pn-junction in a multi-walled WS_2 nanotube and observed radiative recombination via light emission in the visible range (600 nm to 780 nm). The

emission spectra shows the three well-known peaks from light-emitting transistors based on TMDC thin flakes, which come from the direct A and B exciton transitions in the K point and from the lowest energetic transition in the indirect bandgap. We were able to inject electron-hole pairs in the nanotube by shining laser light on the device. The resulting photocurrent increases linearly with increasing power density of the illumination laser.

The electrostatic force of ionic liquids allow to dope semiconductors with large bandgaps, amongst others $SrTiO_3$ ($E_g = 3.25\,eV$) and TMDC monolayers ($E_g = 1.1 - 2.1\,eV$). We investigated two of the best known semiconductors, diamond and silicon. Both materials are proven to become superconducting at chemical doping levels, which are too high to be reached electrostatically with a standard solid backgate. Therefore, EDL-gating could lead to high-T_c superconductivity in structurally cleaner devices. We successfully induced an insulator-to-metal transition in intrinsic diamond with hydrogen-terminated surface and we were able to induce very high p-type charge carrier densities on the surface of pre-doped, metallic silicon. In diamond, we even achieved record mobilities of 60-120 $cm^2\,V^{-1}\,s^{-1}$ for the induced charge carrier density of $\approx 1 \times 10^{14}\,cm^{-2}$. Superconductivity was not observed, however these preliminarily results presented are promising and motivate to continue in this field.

The gelation of ionic liquids offered a solid tool for high charge carrier accumulation with an improvement in practical use for applications, e.g. in integrated circuits. In this process the liquid ions are embedded in a solid matrix, where they can still move freely and react to an applied electric field. We investigated a novel ion gel with the cations fixed on one surface of the film and the anions still able to move freely through the matter. This tool allowed us to realise a novel, low-power type of field-effect diode, which needs only one voltage bias applied to operate. The diode shows promising qualities, like high current on-off ratios of $>10^5$ and off-state currents of $\leq 10\,pA$. We generally characterised the new cation-fixed gel as dielectric and observed a gating performance close to that of an ionic liquid without the inconveniences of a liquid. For instance, leakage currents were reduced to less than 100 pA at applied gate voltages up to $V_g = \pm 5\,V$ at a temperature of 255 K.

After the gelation of ionic liquids with fixing the cations on one surface, the next step could be the fabrication of an electret, where the anions are fixed on the opposite surface than the cations. As one example, this tool could be used to predope the channel material of a FET in order to place the Fermi energy just below (above) the conduction (valence) band and to switch the device from off to on by applying a small backgate voltage. This can lead to a low-power consumption, high-speed device.

The combination of an ion gel with connected, but movable random networks of nano-objects defines one potential use of ion gels in future devices: as medium and dielectric in printable, flexible, stretchable and wearable electronics. Due to their high stability and crystal quality, promising semiconducting nano-objects are TMDC flakes and nanotubes.

One of the most promising perspectives of ionic liquids or gels and TMDC nanotubes

is as new materials in the ongoing downscaling process of electric devices. We could combine three theoretically proven approaches to ever smaller devices without the parasitic short-channel effects: semiconducting nanotubes as channel material, a ring-gate geometry around the channel and ionic liquids.

A Appendix

A.1 List of Ionic Species Abreviations

Cation	
AAIM	1,3-diallylimidazolium
AEIM	1-allyl-3-ethylimidazolium
BMIM	1-butyl-3-methylimidazolium
BMMIM	1-butyl-2,3-dimethylimidazolium
DEME	*N*,*N*-diethyl-*N*-methyl(2-methoxyethyl)ammonium
EMIM	1-ethyl-3-methylimidazolium
EMMIM	1-ethyl-2,3-dimethylimidazolium
HMIM	1-hexyl-3-methylimidazolium
OMIM	1-octyl-3-methylimidazolium
PP13 (MPPR)	*N*-methyl-*N*-propylpiperidinium
P13	*N*-methyl-*N*-propylpyrrolidinium
P14	*N*-butyl-*N*-methylpyrrolidinium
TMPA (TPA)	*N*,*N*,*N*-trimethyl-*N*-propylammonium
Anion	
BETI	bis(pentafluoroethanesulfonyl)imide
BF_4	tetrafluoroborate
DCA	dicyanamide
FAP	tris(pentafluoroethyl)trifluorophosphate
FSI	bis(fluorosulfonyl)imide
$OctOSO_3$	*n*-octylsulfate
OTf	trifluoromethanesulfonate
PF_6	hexafluorophosphate
TCB	tetracyanoborate
TFSI	bis(trifluoromethylsulfonyl)imide

Figure A.1: Taken from [62].

A.2 Measurements of TMDC Thin Flakes

In the course of this work, we fabricated EDL-gated field-effect transistors based on two types of TMDC thin flakes, MoS_2 and WS_2. The mother flakes used for exfoliation are displayed in Fig. 2.1(b) and (c). The WS_2 crystal is a synthetic crystal (grown by flux-based growth technique by "2Dsemiconductors"), whereas the MoS_2 crystal is a naturally grown crystal. Field-effect transistors were fabricated and provided with the ionic liquid EMIM-TFSI as it was described in chapter 3.

A.2.1 Observation of a Superconducting Transition in MoS_2 Flakes

We investigated the EDL-transistor operation performance of an MoS_2 multi-layer with a thickness of 7 nm. An optical image and an AFM image together with a surface profile across the flake are displayed in Fig. 2.1(d)-(f), which clearly show the high quality of the exfoliated flake. A transfer characteristic of the bigger flake, measured in the usual two-probe configuration[1], is shown in Fig. A.2(a). The crystal is slightly n-doped, as the centre of the transport gap is shifted in the direction of negative gate bias. This behaviour is expected in MoS_2, due to sulphur vacancy [151, 170]. We observed I_{on}/I_{off} ratios of $>10^4$ on the hole side and of $>10^5$ on the electron side. Field-effect mobilities were extracted, using the formula $\mu_{FE} = dG_{\square}/dV_g \cdot 1/C_{IL}$ and mobilities of $\approx 10\,cm^2\,V^{-1}\,s^{-1}$ and $\approx 29\,cm^2\,V^{-1}\,s^{-1}$ resulted for holes and electrons respectively. The capacitances used for the calculations were extracted from Hall measurements performed on the same flake (not shown), and resulted as $2\,\mu F\,cm^{-2}$ and $5\,\mu F\,cm^{-2}$ on the hole and electron side respectively. These capacitances are similar to values published by Shi *et al.* [194] (see Fig. 1.3(d)) and our field-effect mobilities are slightly smaller, but of the same order of magnitude as the published values of EDL-gated thin flakes. For example, in suspended MoS_2 thin flake transistors, mobilities of $46\,cm^2\,V^{-1}\,s^{-1}$ were reached [91] and in thin flakes on Si/SiO_2 hole (electron) mobilities up to $44\,cm^2\,V^{-1}\,s^{-1}$ ($86\,cm^2\,V^{-1}\,s^{-1}$) [260] were achieved.

We cooled down the flake and measured its longitudinal sheet resistance in four-terminal configuration with a gate voltage of 4 V applied to the counter electrode. An optical image of the device with the four-terminal measurement configuration is displayed in the inset of Fig. A.2(a). From the previously performed Hall measurements, we know that the gate bias $V_g = 4\,V$ corresponds to an injected surface charge carrier concentration of $9 \times 10^{13}\,cm^{-2}$. The device became superconducting at a critical temperature of 5 V (taken at the half of the transition). The sheet resistance versus temperature over the whole temperature range is shown in Fig. A.2(b) and a zoom into the low-temperature part, highlighting the superconducting transition, is displayed in Fig. A.2(c). Our device behaves similarly to a device measured by Taniguchi *et al.*, who equally used a natural MoS_2 crystal: for gate

1 In order to be able to probe the drain-source current continuously from hole to electron doping, crossing the gap with extremely low currents, a four-terminal measurement would not give correct values, as the resistance in the gap would exceed the impedance of the measurement unit.

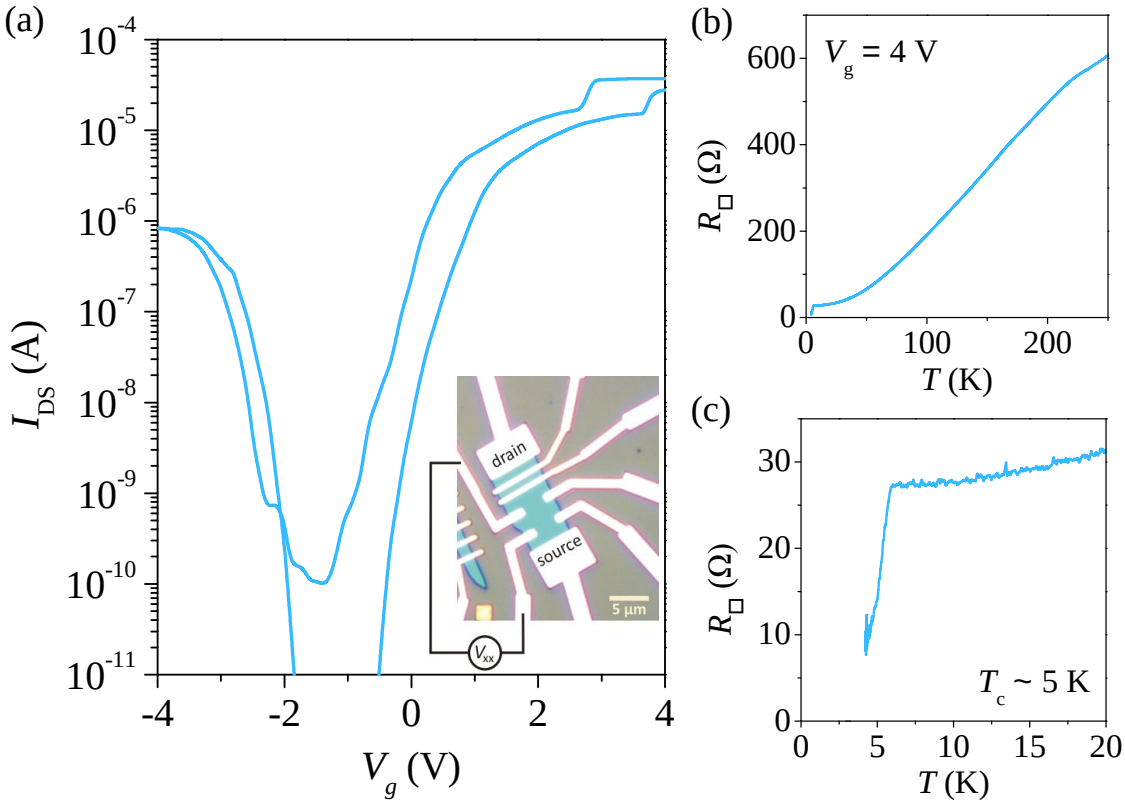

Figure A.2: Device JS087a1. (a) Transistor transfer characteristic of a 7 nm thick MoS_2 flake in semi-logarithmic scale. The inset shows an optical image of the device after lift-off with the measurement configuration of the device. This gate sweep was done in two-terminal configuration between drain and source contacts. (b) Sheet resistance versus temperature in four-terminal configuration and with $V_g = 4\,V$ applied to the liquid gate. (c) Zoom into the low-temperature part of the measurement shown on (b). A superconducting transition is visible with an onset of $\approx 6\,K$.

voltages of 3 V and 4 V applied, they observed a superconducting transition at 5 K and 7 K respectively. Their measurements are displayed in Fig. 2.4(a). Interestingly, at $t = 250\,K$, our device has a sheet resistance which exceeds their value by one order of magnitude, even though the sheet resistances just before the superconducting transitions are almost equal. Additionally, our field-induced charge carrier densities are generally lower than those achieved by Taniguchi *et al.*, which means that our device became superconducting with carrier concentrations lower than their critical concentration for superconductivity. These differences possibly originate from the different sources of the two naturally grown MoS_2 crystals and therefore from slightly different compositions and properties. For instance, our superconducting transition is much sharper than theirs, which indicates a higher crystal quality.

A.2.2 WS_2 Thin Flake Transistors

We investigated two EDL-gated WS_2 thin film FETs of different thickness, where the thinner flake shows mobilities three times higher than the thicker one. We will start with

the characterisation of the thin flake and then show Hall measurements done on the thicker one.

High Mobility EDL-gated Transistor

We performed two-probe measurements on an exfoliated WS_2 thin flake of 7 nm thickness. Fig. A.3(a) shows the sheet conductance as a function of gate voltage in linear scale. Dashed lines indicate the highest slopes which we used to calculate the field-effect mobilities, using the relation $\mu_{\mathrm{FE}} = dG_{\square}/dV_{\mathrm{g}} \cdot 1/C_{\mathrm{IL}}$. The capacitances used for the calculation were extracted from Hall measurements performed on the thicker flake, which will be presented in the following section. The highest resulting values for the hole and electron mobilities are $287\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ and $137\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ respectively. The inset of Fig. A.3(a) is the transistor transfer characteristic in semi-logarithmic scale. $I_{\mathrm{on}}/I_{\mathrm{off}}$ ratios of more than 10^4 on the hole side and of $\geq 10^5$ on the electron side were observed. The mobility values are higher than the highest values published so far for EDL-gated WS_2 thin flake transistors at $T \geq 250\,\mathrm{K}$, which hardly reach $100\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ (see table 2.1). This indicates the very high sample quality which is at the same time reflected in the very high on-state currents. The latter at highest hole and electron doping can be translated into the two-terminal resistances which reach values as low as $5.5\,\mathrm{k\Omega}$ and $1.5\,\mathrm{k\Omega}$ for hole and electron doping respectively.

The two-terminal resistance at $V_{\mathrm{g}} = 4\,\mathrm{V}$ decreases further when the temperature is reduced,

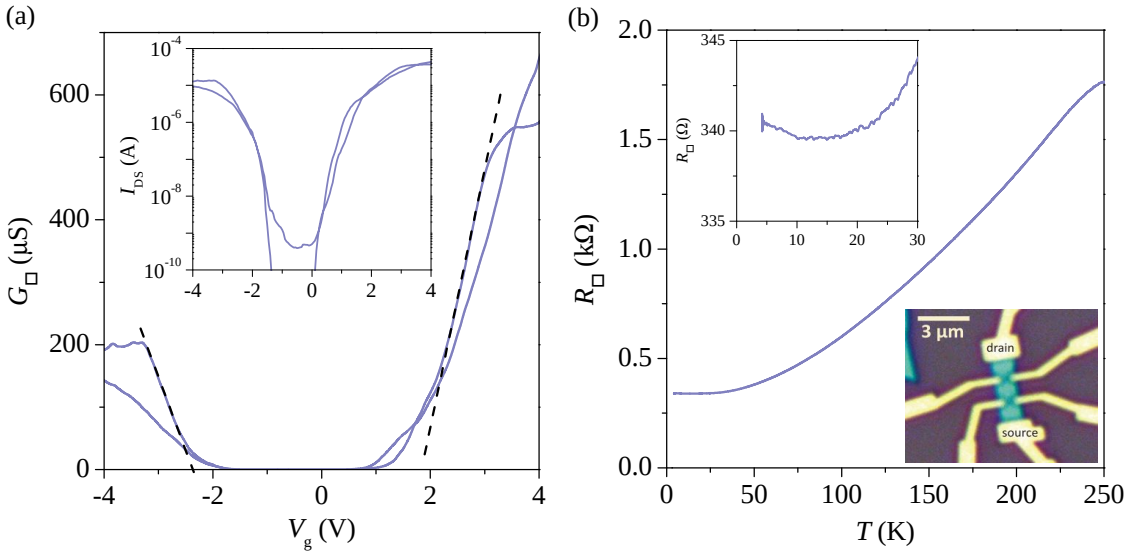

Figure A.3: Device JS105b. (a) Sheet conductance versus liquid-gate voltage of a high mobility WS_2 thin flake. Dashed lines indicate the steepest slopes, which were taken to calculate the field-effect mobilities. The inset shows the source-drain current versus gate voltage in semi-logarithmic scale. (b) Sheet resistance as a function of temperature at a gate voltage of $V_{\mathrm{g}} = 4\,\mathrm{V}$ applied. The insets show a zoom in the low-temperature part of the resistance versus temperature measurement and a photo of the device with the two-terminal measurement configuration.

revealing the metallic state of the flake at high n-doping levels. The sheet resistance versus temperature, measured in two-terminal configuration, is displayed in Fig. A.3(b). The two insets show the zoom in the low temperature part and an optical image of the device after the lift-off with source and drain contacts indicated. The resistance decreases down to a temperature of $\approx 15\,\mathrm{K}$ and re-increases very slightly at $T < 10\,\mathrm{K}$. Even though measured in two-terminal configuration, the sheet resistance of $\approx 340\,\Omega$ at the lowest measured temperature of 4 K, hardly reaches two thirds of the sheet resistance of the superconducting sample presented in Fig. 2.4(b) just before the superconducting transition. It can therefore be expected that our device would undergo a superconducting transition at $T < 4\,\mathrm{K}$ as well.

Characterisation of a High-Capacitance Ionic Liquid on WS_2

The second WS_2 device we investigated is a flake of a thickness of 85 nm patterned with a Hall bar design and provided with ionic liquid. We performed Hall measurements at different n- and p-doping levels in order to receive the according capacitance values of our ionic liquid used on WS_2.

The Hall resistance R_H of the two-dimensional conduction channel is given as

$$R_\mathrm{H} := \frac{dR_\mathrm{xy}}{dB} = -\frac{1}{ne}\,, \tag{A.1}$$

with R_xy being the transversal resistance, n being the charge carrier density and e being the electron charge. We can then calculate the capacitance of the ionic liquid C_IL and the Hall mobilities of the charge carriers μ via

$$C_\mathrm{IL} = \frac{ne}{V_\mathrm{g}} = -\frac{1}{R_\mathrm{H} V_\mathrm{g}} \quad \text{and} \quad \mu = \frac{R_\mathrm{H}}{\rho}\,, \tag{A.2}$$

with ρ being the sample's resistivity. The four-terminal measurement configuration is shown in the inset of Fig. A.4(a). Both longitudinal and transversal resistances were measured at the same time and we used the longitudinal sheet resistance $R_{xx}/(\#\mathrm{sheets})$ in a zero magnetic field as resistivity to calculate the Hall mobility.

The two-dimensional charge carrier densities as a function of gate voltage are shown in Fig. A.4(a). They increase with increasing negative or positive gate voltage until they reach their maximum at $V_\mathrm{g} = \pm 6\,\mathrm{V}$. The highest densities obtained are $\approx$2-3 $\times\, 10^{13}\,\mathrm{cm}^{-2}$ for hole doping and about $\approx 1.2 \times 10^{14}\,\mathrm{cm}^{-2}$ for electron doping. The gate voltage dependence of the capacitances calculated with Eq. (A.2) are displayed in Fig. A.4(b). C_IL increases up to $-3\,\mathrm{V}$ on the hole side and up to 5 V on the electron side and re-decreases for higher doping levels. We estimated the average capacitances at high doping levels to be 0.8 and $3\,\mu\mathrm{F\,cm}^{-2}$ for hole and electron doping respectively These are the values we used for the calculation of the field-effect mobilities of all WS_2 flakes and nanotubes investigated in the course of this work. The big difference of the capacitances at hole and electron side is due

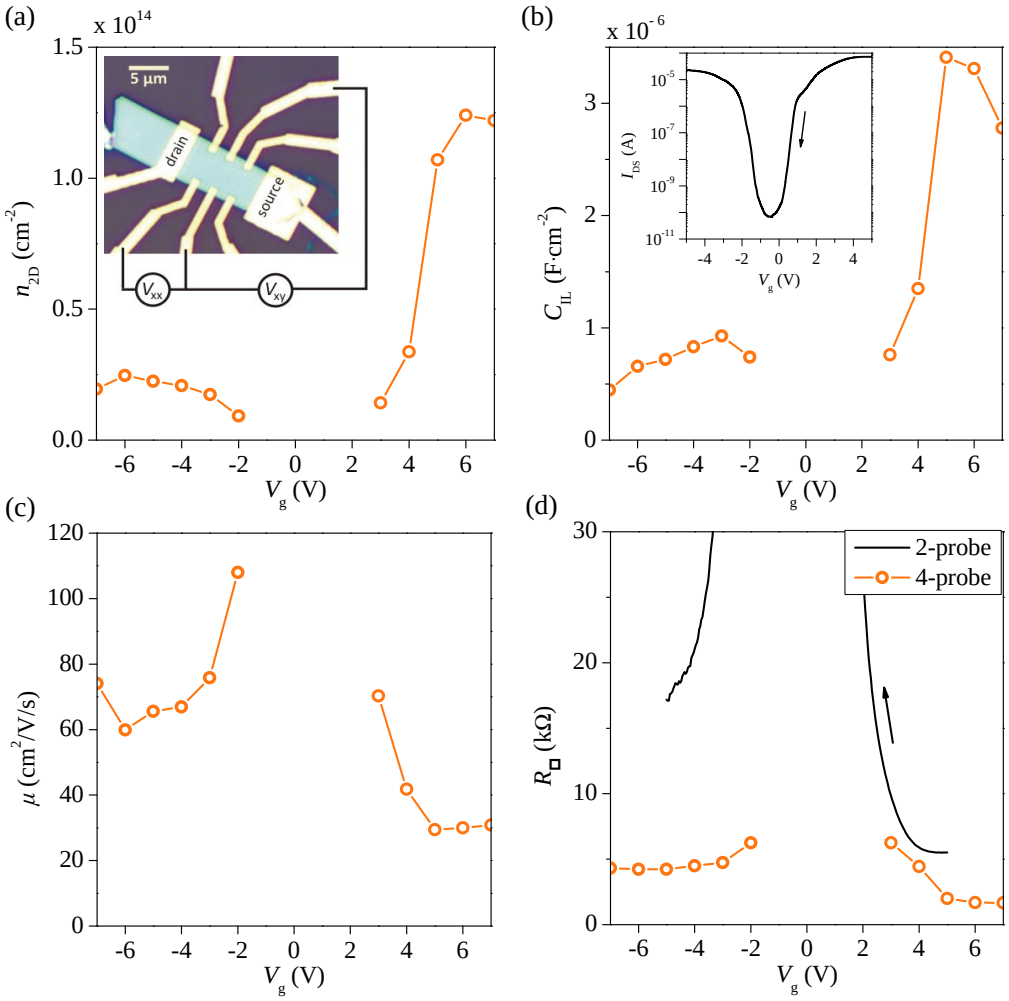

Figure A.4: Results of Hall measurements on device JS105c. (a)-(d) 2D charge carrier density, ionic liquid capacitances, sheet resistance and Hall mobility versus gate voltage respectively. The inset in (a) displays an optical image of the device after lift-off with the drawn four-probe configurations for the measurements of both longitudinal and transversal resistances. The inset in (b) is a two-probe transistor transfer characteristic in semi-logarithmic scale. In (d), the four-probe resistances are compared to a two-probe measurement between the same voltage contacts in order to estimate contact resistances.

to the size difference between liquid anions and cations [30].

The inset of Fig. A.4(b) displays the source-drain current as a function of V_g, which shows the ambipolar operation of this thin film transistor. Current on-off ratios of more than five orders of magnitude on the hole side and of about six orders of magnitude on the electron side are reached, which underlines excellent transistor behaviour. The field-effect mobilities $\mu_{FE} = dG_{\square}/dV_g \cdot 1/C_{IL}$ resulted as $56\,cm^2\,V^{-1}\,s^{-1}$ and $23\,cm^2\,V^{-1}\,s^{-1}$ for hole and electron doping respectively. The Hall mobilities calculated with Eq. (A.2) are plotted versus the gate voltage in Fig. A.4(c). Mobility increases with increasing $|V_g|$ and starts saturating at $\approx -4\,V$ and at $\approx 5\,V$ on the hole and electron side respectively. Such a gate voltage dependence of the mobility has already been observed before, as for example displayed in Fig. 2.2(d) or in ref. [260]. The saturation of mobility indicates that the

conductance channel is completely established. The saturation Hall mobilities match pretty well with the field-effect mobilities calculated. This correspondence confirms that we can use the extracted capacitance values for further calculations of μ_{FE}.

Finally, we will compare four-probe and two-probe sheet resistances in order to estimate the contact resistance. In Fig. A.4(d), the values of R_{xx} in a zero magnetic field divided by the number of sheets (=1/2) are plotted versus the corresponding gate voltage. Note that these are the four-probe sheet resistance values we used to calculate the Hall mobilities. In the same graph, the two-terminal sheet resistance versus gate voltage is shown, originating from the same gate sweep, which is displayed in the inset of panel (b). The resistance differences at highest doping levels correspond to the contact resistances and were observed to be $\approx 12\,\mathrm{k}\Omega$ for hole doping and $\approx 4\,\mathrm{k}\Omega$ for electron doping.

A.3 Statistics

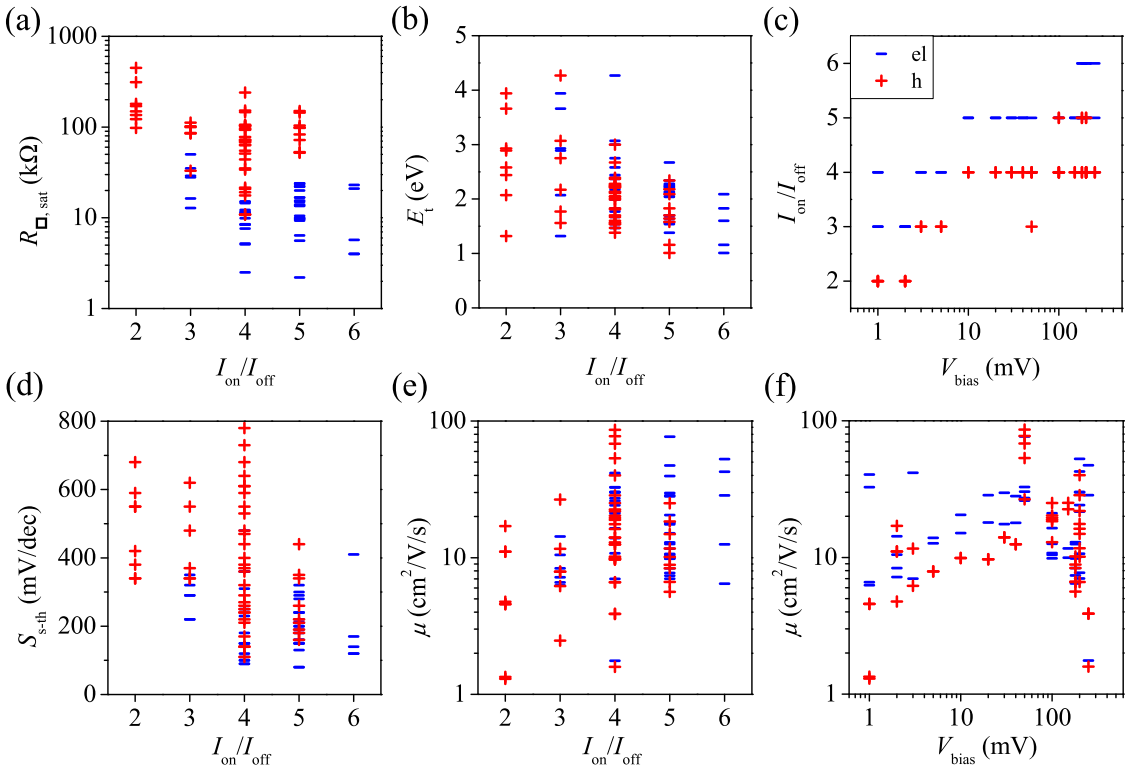

Figure A.5: (a), (b), (d), (e) Current on-off ratio dependence of the saturation sheet resistance, the transport gap, the subthreshold swing and the mobilities, each time for hole and electron doping. General conditions are better when I_{on}/I_{off} is higher, Δ_t becomes less dispersed and narrower. (c), (f) I_{on}/I_{off} and μ as a function of V_{bias}. The current on-off ratio is increasing for increasing bias voltage, whereas mobilities increase only up to $V_{bias} \approx 50\,\mathrm{mV}$.

In chapter 4, section 4.3, statistics over all measured and well performing devices were discussed. Here, we will show all sample parameters that entered in the statistics.

From all the statistics that were drawn up very few striking dependences result. The most pronounced ones are displayed in Fig. A.5, where (a), (b), (d) and (e) show sheet resistance at the saturation, transport gap, subthreshold swing and mobility versus current on-off ratio, each time for hole and electron doping. These plots demonstrate that devices with highest I_{on}/I_{off} are in general the best performing devices: $R_{\square,\mathrm{sat}}$ and $S_{s\text{-}th}$ are decreasing for increasing I_{on}/I_{off} and μ_h, μ_{el} as well as Δ_t show a tendency of increment for increasing I_{on}/I_{off}. In the case of Δ_t there is also a tendency of less dispersion. Fig. A.5(c) and (f) show the current on-off ratio and the mobilities as a function of bias voltage.

One more parameter should be mentioned shortly, the off-state current. Astonishingly, there is no clear dependence of any parameter on I_{off}. For electronic devices low I_{off} values are important, but in terms of mobility and subthreshold swing intrinsically less resistive INTs can also show a very good performance.

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Résumé

Johanna SEIDEMANN

Iontronic - Etude de dispositifs à effet de champ à base des techniques de grilles liquides ioniques

Les liquides ioniques sont des fluides non volatiles, constitués de cations et d'anions, qui sont conducteurs ioniques, isolants électriques, et peuvent avoir des valeurs de capacité très élevées. Ces liquides sont susceptibles non seulement de remplacer les électrolytes solides, mais également de susciter des champs électriques intenses ($>10\,\mathrm{MV\,cm^{-1}}$) au sein d'une couche dite double couche électronique (electric double layer, EDL) à l'interface entre le liquide et le matériau sur lequel il est déposé. Ceci conduit à une injection de porteurs de charge bidimensionnelle avec des densités allant jusqu'à $10^{15}\,\mathrm{cm^{-2}}$. Cet effet de grille remarquablement fort des liquides ioniques est réduit en présence d'états piégés ou de rugosité de surface. À cet égard, les dicalchogénures de métaux de transitions, de très haute qualité cristalline et atomiquement plats, font partis des semi-conducteurs les plus adaptés aux grilles EDL.

Nous avons réalisé des transistors à effet de champ avec des EDL dans des nanotubes multi-couches de WS_2, avec des performances comparables à celles de transistors EDL sur des îlots de WS_2, et meilleurs que celles de nanotubes de WS_2 avec une grille solide. Nous avons obtenu des mobilités allant jusqu'à $80\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ pour les porteurs n et p, et des ratios de courants on/off dépassant 10^5 pour les deux polarités. Pour de forts dopages de type électron, les nanotubes ont un comportement métallique jusqu'à basse température. De plus, utiliser un liquide ionique permet de créer une jonction pn de manière purement électrostatique. En prenant avantage de cet effet, nous avons pu réaliser un transistor photoluminescent dans un nanotube.

La possibilité de susciter de très forte densités de charges donne la possibilité d'induire des phases métalliques ou supraconductrices dans des semi-conducteurs a large bande interdite. Nous avons ainsi réussi à induire par effet de champ une phase métallique à basse température dans du diamant intrinsèque avec une surface hydrogénée, et nous avons obtenu un effet de champ dans du silicone dopé métallique.

Les liquides ioniques offrent beaucoup d'avantages, mais leur champ d'application est réduit par l'instabilité du liquide, ainsi que par les courants de fuites et l'absorption graduelle d'impuretés. Un moyen efficace de s'affranchir de ces inconvénients, tout en conservant la possibilité d'induire de très fortes densités de porteurs, est de gélifier le liquide ionique. Nous sommes allés plus loin en fabriquant des gels ioniques modifiés, avec les cations fixés sur une seule surface et les anions libres de se mouvoir au sein du gel. Cet outil nous a permis de réaliser une nouvelle diode à effet de champ de faible puissance.

Mots clés: Double couche électrique, fort dopage, dicalchogénures de métaux de transition, semiconducteur, nanotube, transistor ambipolaire, transition isolant-métal, transistor à émission de lumière, gel ionique, diode à effet de champ

Abstract

Johanna SEIDEMANN

Iontronics - Field effect study of different devices, using techniques of ionic liquid gating

Ionic liquids are non-volatile fluids, consisting of cations and anions, which are ionically conducting and electrically insulating and hold very high capacitances. These liquids have the ability not only to replace solid electrolytes, but to create strongly increased electric fields ($>10\,\mathrm{MV\,cm^{-1}}$) in the so-called electric double layer (EDL) on the electrolyte/channel interface, which leads to the injection of 2D charge carrier densities up to $10^{15}\,\mathrm{cm^{-2}}$. The remarkably strong gate effect of ionic liquids is diminished in the presence of trapped states and roughness-induced surface disorder, which points out that atomically flat transition metal dichalcogenides of high crystal quality are some of the semiconductors best suited for EDL-gating.

We realised EDL-gated field-effect transistors based on multi-walled WS_2 nanotubes with operation performance comparable to that of EDL-gated thin flakes of the same material and superior to the performance of backgated WS_2 nanotubes. For instance, we observed mobilities of up to $80\,\mathrm{cm^2\,V^{-1}\,s^{-1}}$ for both p- and n-type charge carriers and our current on-off ratios exceed 10^5 for both polarities. At high electron doping levels, the nanotubes show metallic behaviour down to low temperatures. The use of an electrolyte as topgate dielectric allows the purely electrostatic formation of a pn-junction. We successfully fabricated a light-emitting transistor taking advantage of this utility.

The ability of high charge carrier doping suggests an electrostatically induced metal phase or superconductivity in large gap semiconductors. We successfully induced low temperature metallic conduction into intrinsic diamond with hydrogen-terminated surface via field-effect and we observed a gate effect in doped, metallic silicon.

Ionic liquids have many advantageous properties, but their applicability suffers from the instability of their liquid body, gate leakage currents and absorption of impurities. An effective way to bypass most of these problems, while keeping the ability of ultra-high charge carrier injection, is the gelation of ionic liquids. We even went one step further and fabricated modified ion gel films with the cations fixed on one surface and the anions able to move freely through the film. With this tool, we realised a novel low-power field-effect diode.

Key words: electric double layer, ultra-high doping, transition metal dichalcogenides, semiconductor, nanotube, ambipolar transistor, insulator-to-metal transition, light-emitting transistor, ion gel, field-effect diode