Smart power management silicon integrated interfaces for capacitive vibration energy harvesters

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devant le jury composé de :

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Smart power management silicon integrated interfaces for capacitive vibration energy harvesters

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Abstract

Vibrational energy is an attractive power source for self-powered wireless sensors. A mainstream harvesting technique for vibrational energy is electrostatic MEMS harvesters (e-VEH). Various circuit architectures have already been introduced with many successful implementation, yet a load interface that efficiently manages the harvested energy has rarely been reported.

In this work a load interface is proposed which is suited for any condition circuit (CC) implementing rectangular QV cycles. In general, a rectangular QV conditioning circuit has an optimum interval of which the energy harvested is maximised, thus the harvested energy should be periodically removed to maintain maximising the harvested energy. This is achieved through the load interface (LI). The LI proposed is a switched inductor capacitive architecture with a LI controller allowing the extraction of the energy in a multiple energy shot fashion. The LI controller incorporate an ultra low power clock for switching events, as well as low power comparator for switching decision. Power consumption is reduced by operating at a low supply voltage (1.1V).

The proposed load interface is implemented in AMS0.35HV technology with a mixed high voltage and low power control blocks. It takes into account the harvester operation to maximise the energy extracted from the harvester. It overcomes the constrained limited biasing power, and tackles resistive losses and power handling transistor long channels by transferring the energy in a multiple shots fashion. A complete CMOS implementation is proposed along with the simulation results with an average consumed power of the controller less than 100nW allowing the system to operate with input power levels as low as few hundreds of nanowatts.

Keywords: vibration, vibrational energy, power management, integrated circuit, high voltage, controller, voltage regulation, switch, MEMS, capactive transducer.

Abstract - French

Les vibrations ambiantes représentent une source potentielle d'énergie pour alimentation des capteurs sans fil autonomes. La transduction électrostatique est une des techniques utilisées pour la conversion de l'énergie des vibrations en électricité. De nombreuses réalisations des transducteurs et leurs circuits de conditionnement ont déjà été présentées dans la littérature. Pour transmettre l'énergie convertie vers une charge utile (par exemple, une batterie), des interfaces spécifiques doivent être conçues. Ce dernier sujet a été peu abordé dans la littérature.

Ce travail étudie une interface avec la charge dans un dispositif de récupération d'énergie vibratoire. L'architecture proposée au cours de cette étude est particulièrement adaptée aux circuits de conditionnement de type pompe de charge, qui fonctionne selon un cycle charge-tension rectangulaire. L'interface proposée accomplit deux tâches. Premièrement, il permet de transférer l'énergie électrique du circuit de conditionnement vers une charge tout en abaissant la tension d'une manière adiabatique, c.a.d., en minimisant les dissipations. Deuxièmement, il permet de réguler le débit d'extraction d'énergie du circuit de conditionnement en ajustant dynamiquement la puissance de ce transfert. Cela est réalisé avec un circuit intégrée en technologie 0.35 um CMOS haute tension dont l'architecture est inspirée d'un convertisseur DC-DC de type Buck fonctionnant en régime discontinu. La consommation de l'interface est minimisée grâce à l'utilisation du régime sous le seuil des transistors MOS pour pratiquement tous les blocs, grâce à une alimentation réduite à 1.1 Volt. L'interface consomme en dessous de 100 nanoWatts, et est capable de gérer des sources d'énergie à puissance en dessous de 1 microWatt.

"But man is not made for defeat" he said.
"A man can be destroyed but not defeated".

– *Ernest Hemingway, The Old Man and the Sea*

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Abbreviations

CC Conditioning Circuit

RF Radio Frequency

EM Electromagnetic

ES Electrostatic

PE Piezoelectric

VEH Vibration Energy Harvesters

e-VEH Electrostatic Vibration Energy Harvesters

MEMS Micro-Electro-Mechanical-System

CCR Conditioning circuit Regulator

LVR Load voltage Regulator

MPPT Maximum power point tracking

TC Time Control

VC Voltage Control

DTVC Discrete-Time Voltage Control

Chapter 1

Introduction

Contents

1.1 Overview

Energy harvesting has been around since hundreds, if not thousands, of years. Whether it was windmills, waterwheels or even the simple concept of storing the energy from heat and vibrations. In fact, before the electrical era, energy harvesting was the only possible way to get any useful form of energy.

Fast forward to today, the term Energy Harvesting is used to refer to extracting energy from surrounding environment. The research behind energy harvesting has grown wide recently and its driven by the need for autonomously power embedded systems. Traditionally Li-ion batteries have been the go-to method for powering such system, yet they impose certain limitations such as their lifespan and maintenance. In

these applications, batteries proved to be inadequate and unpractical for applications such wearable gadgets and implantable medical devices.

With the gap between the energy required to operate such devices and the functionality expected out of it is closing more and more with each year (mirco-watts range), energy harvesting presents a solution to power such application. This said, energy harvesting raises some issues that need to be addressed before it can be used. These includes:

– Capture and transform the energy efficiently.

– How to accumulate, store and condition the harvested energy.

The issue of efficiently capturing the energy is introduced and studied extensively within the energy harvesting community[1]. This PhD project is concerned with how to manage the captured energy. However, before discussing our approach of how to tackle this issue, a brief introduction to energy harvesting fundamentals is presented in this chapter.

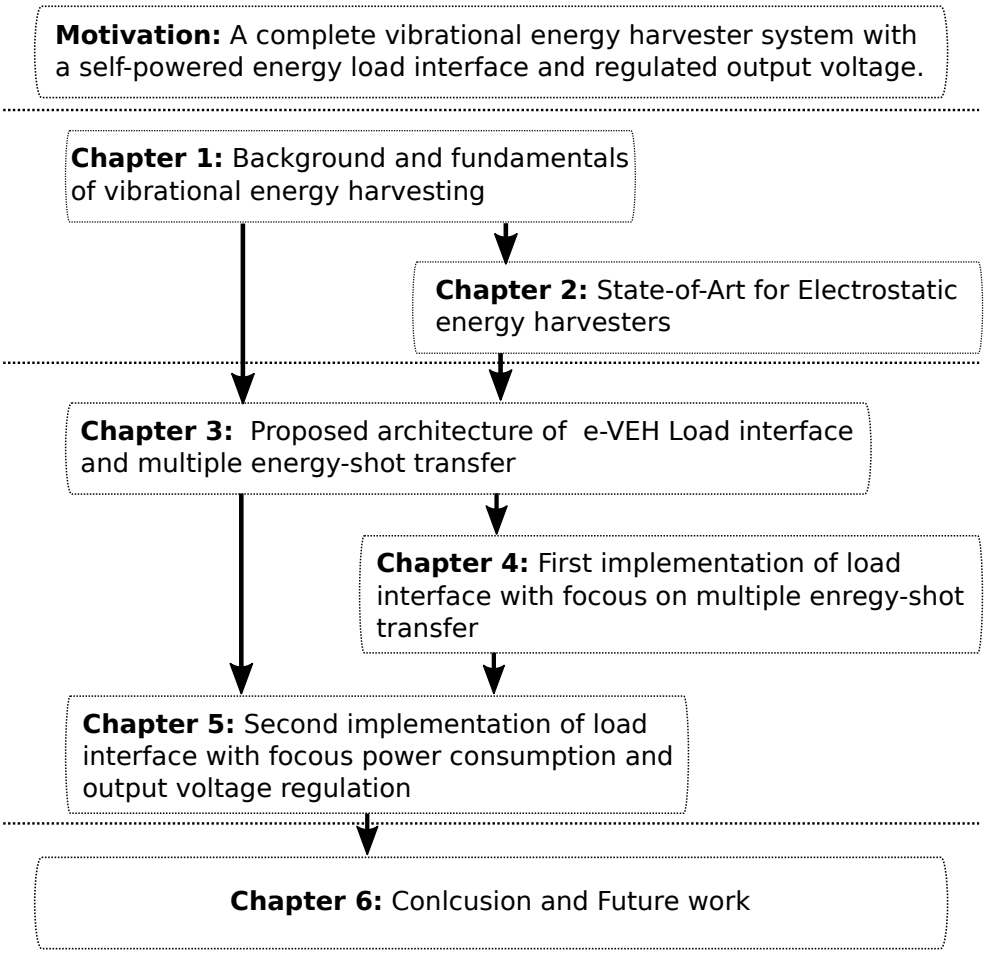


Figure 1.1: Thesis chapters and outline

1.2 Thesis Outline

The thesis outline, shown in Figure 1.1, is as follows: Chapter 1 presents the fundamentals of Vibration Energy Harvesters (VEH) and especially Electrostatic Vibration Energy Harvesters (e-VEH) as well as the motivation for this PhD project. Chapter 2 highlights the recent reported vibrational harvesters and energy management interfaces. The methodology we present to tackle the problem of load interfacing with the vibrational energy harvester is discussed in Chapter 3. A first approach towards a smart energy management interface for e-VEH is proposed in Chapter 4, while an improved version of the load interface addressing how to make the management interface work autonomously is presented in Chapter 5. This work conclusion and future work are summarised in Chapter 6.

1.3 Harvestable Energy Sources

Our surrounding environment is filled with various sources of energy that await to be harvested. These sources share few common features such as being abundant, and available yet free. The sources that are of interest for energy harvesting applications can be classified by the nature of the energy harvested. These types include:

– *Mechanical energy* where vibration or mechanical stress/strain sources exists. These sources could be a factory engine or a truck on a bridge.

– *Thermal energy* where sources of heater exists. These include industrial machinery, furnaces and friction.

– *Light energy* this is usually implemented by solar panels that make use of direct sunlight or even ambient light sources.

– *Electromagnetic energy* where source of Radio Frequency (RF) waves are used to wireless transfer energy. This is commonly used for RFID and wireless charging of electronic devices.

The sources of energy can also be classified by the amount of energy available to be harvested. By defining the scale of application they can be classified into nano-watt, milli-watt and Mega-watt applications as shown in Figure 1.2. For the application that requires megawatt power range waterfalls and wind turbines as well as solar cell panels are appropriate. For mid range power applications (milli to micro watts) piezoelectric, electrostatic and electromagnetic energy harvesters from sources like vibration are proven to be sufficient. For nano watt application the technology bound needed to be pushed a little further towards piezoelectric nanowires and Nano-sensors. To put this into perspective, Table 1.1 summarises the power density for each energy source. This PhD project is concerned with micro-scale energy harvesting that is derived from Micro-Electro-Mechanical-System (MEMS) devices. Targeted applications include health monitoring wearables where a typical case is to harvest a user's vibrational energy and then use it to monitor and transmit data without the need for a battery [1]. In the next section, vibrational energy is introduced as well as its transduction to electrical energy methods.

[1]The health monitoring wearable is not the scope of this thesis whereas the energy management interface is the main focus of this work.

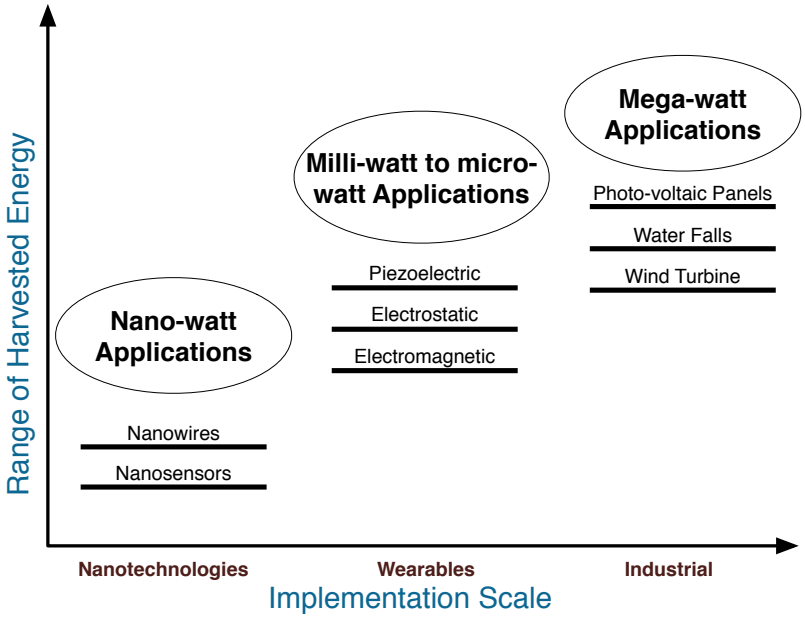


Figure 1.2: Harvested energy range and application

Table 1.1: Estimated harvestable power density

Energy Source	Characteristics	Harvestable Power
Vibration	Hz - Human kHz - Industrial	$4\mu W/cm^2$ $800\mu W/cm^3$
Thermal	Human Industrial	$60\mu W/cm^2$ $1-10\mu W/cm^2$
Light	Outdoor Indoor	$100mW/cm^2$ $100\mu W/cm^2$
Radio Frequency	GSM 900 MHz WiFi	$0.1\mu W/cm^2$ $0.001/muW/cm^2$

1.4 Vibration Energy Harvesting

The source of vibration energy could be any ambient kinetic energy in the surrounding environment. It could be a car engine, a washing machine or simply a running man. The frequency and amplitude of such source vary since they vary in their nature. Figure 1.3 shows some selected vibration spectrum from different ambient sources while Table 1.2 presents the amplitude and peak frequency of vibrations in some ambient sources.

As can be seen from Figure 1.3 the vibration spectrum spread over a range of frequencies yet most of its power is concentrated in a narrow band of frequencies. Moreover, Table 1.2 it is clear that the ambient vibration sources in the low frequency range.

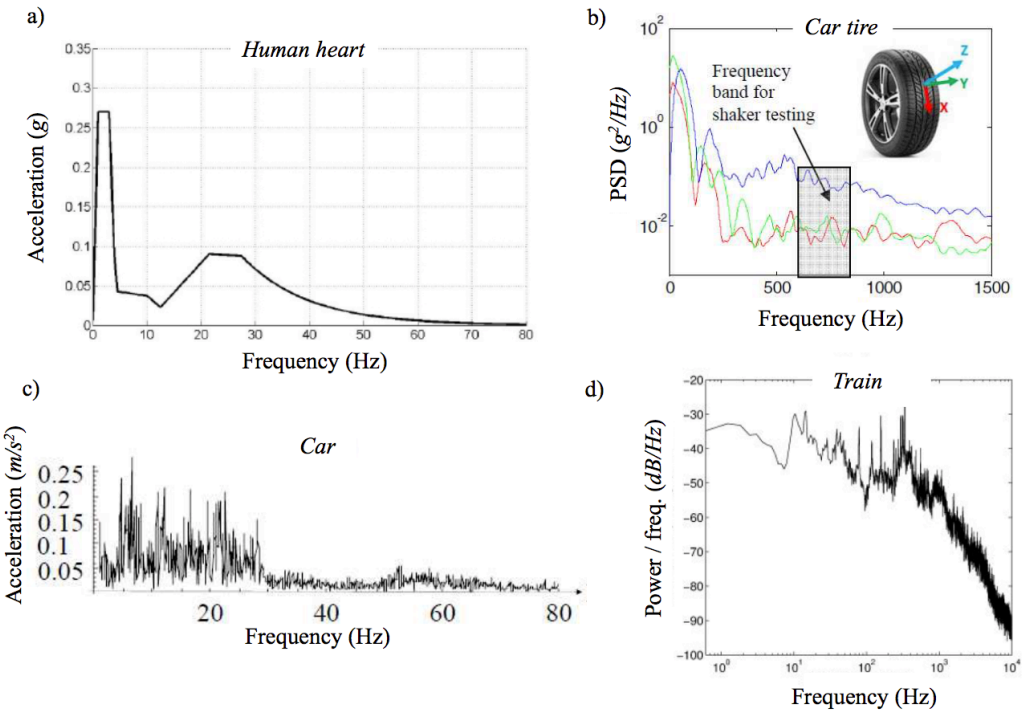


Figure 1.3: Vibration spectrum of (a) human heart blood acceleration[2] (b) tire inner surface @60 km/h[3] (c) car acceleration[4] (d) train acceleration[5]

Table 1.2: Vibration spectrum of different vibrating source [6]

Vibration source	Peak acceleration [m/s^2]	Peak frequency F_{peak} [Hz]
Car engine compartment	12	200
Kitchen blender casing	6.4	121
Clothes dryer	3.5	121
HVAC vents in office building	0.5	60
Wooden deck with foot traffic	1.3	385
External window of a busy street	0.7	100
Washing machine	0.5	109
Refrigerator	0.1	240

1.5 Vibrational energy transduction methods

This section presents the common methods of converting vibration energy into electrical energy with an emphasise what is called *electrostatic energy harvesting*. These methods of converting mechanical energy into electrical energy exits, cf. Figure 1.4, includes: Electromagnetic (EM) , Electrostatic (ES) and Piezoelectric (PE) [7–9].

Piezoelectric (PE): Consider a clamped cantilever made of two bimorph layers and separated by a thin dielectric film and a proof mass attached its tip, cf. Figure 1.4a.

The mass is allowed to move freely with an external vibration are exerted on it. This creates a strain on the piezoelectric material and separates charges across it. If the movement of the mass is caused by a periodic vibration, an alternating voltage is created. With rectification stage, this voltage can be captured and stored in a battery [10, 11]. Some successful implementation of PE transducers was presented [12–15]

Electromagnetic (EM): They are based on electromagnetic induction and ruled by Lenz's law where an electromotive force is generated from a relative motion between a coil and a magnet [16]. Assuming a movable coil attached to proof mass which resonates with an external vibrating source, cf. Figure 1.4b. As the movable coil cuts through the permanent magnetic flux it induces a current in the coil[2]. Electromagnetic transduction usually requires a boost converter stage to provide sufficient voltage for standard rectification techniques [17]. Some practical implementation was presented in [18, 19]

Electrostatic (ES): vibration transducer is implemented by a variable MEMS capacitor, cf. Figure 1.4c. A proof mass is attached to one of the electrodes and is allowed to resonate [3]. The principle of energy conservation states that for the transducer to transform the mechanical energy into electrical energy, an electrically-originated damping force on the moving mass should be applied to purposely reduce its kinetic energy.

Electrostatic transduction usually features high voltage with relatively low output power (typically less than $10\mu W$ [1]). It is easier to integrate with power electronics compared to other transduction methods [6], since it uses MEMS silicon technology. This allows implementing the transducer along with its driving CMOS electronics on the same wafer. A detailed survey of electrostatic energy transducers state-of-the-art will be presented in Chapter 2.

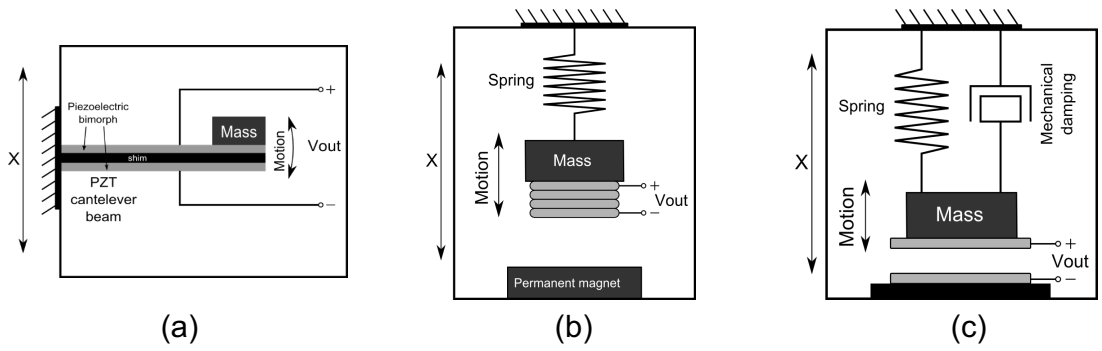


Figure 1.4: Illustration of (a) Piezoelectric (b) Electromagnetic (c) Electrostatic transduction

Each of the mentioned methods of transduction has its advantages and disadvantages as summarised in Table 1.3. In most cases, PE and ES devices are more appropriate for small scale energy harvesters (<1-10 cm^3) while EM converters are better for larger devices[16]. Moreover, ES converters show more potential when it comes to monolithic integration. Electrostatic converters feature low output power levels, yet with power electronics shifting towards ultra low power consumption, they

[2]The moving part can be either the movable coil or the permanent magnet.

[3]Electrostatic transducers can be non-resonators, yet in this context they are assumed resonant structures.

now can be introduced as a valuable power source. This PhD project is concerned with electrostatic transduction and thus the next section is dedicated to discussing its fundamentals.

Table 1.3: Comparison between PE, EM and ES transduction methods

Method	Advantages and Disadvantages of conversion methods
Piezoelectric (PE)	*Advantages:* - high output power density[6] - no separate pre-charging voltage source - no need to control any gap [16] *Disadvantages:* - expensive material[20] - hard to integrate with CMOS technology[6]
Electromagnetic (EM)	*Advantages:* - high output current[20] - long lifetime[16] - robustness[16] *Disadvantages:* - low output voltages [16] - low efficiency in low frequencies[16]
Electorstatic (ES)	*Advantages:* - high output voltage[21] - low cost[16] - easy to integrate with CMOS[6] *Disadvantages:* - requires a separate pre-charging voltage source[6] - high impact of parasitic[16] - need to precisely define μm-dimensions[16]

1.6 Electrostatic vibrational energy harvesters

Electrostatic Vibrational Energy Harvester e-VEH systems refer to a wide array of architectures that aims to manage the energy harvesting process and prove a stable constant DC voltage to a load or a buffer. In fact, a vibrational energy harvester system can be break up into :

– *The transducer interface* which is the system input where the source vibration energy is applied. This part of the system is responsible of regulating the energy transduction process and accumulating the energy on to a reservoir. This part of the system includes variable MEMS capacitors as transducers, see section 1.7, and conditioning circuit CC, see section 1.9, section , which synchronise the energy conversion with the capacitor variation.

This stage is chosen according to the nature of the transducer - whether it is piezoelectric, electromagnetic or electrostatic - different implementation of these interfaces are used. For example, piezoelectric transducer requires an AC-to-DC rectification as

the piezoelectric transducer provides an AC output voltage. Electromagnetic transducers on the other hand require a boost dc-dc converter and rectification stages as its transducers usually provide low AC output voltage. For electrostatic VEH the transducer is accompanied by a conditioning circuit (CC), that synchronises the energy conversion with the movement of the variable capacitor, such as [6, 22–25].

– *Power management interface* This block controls the energy flow between the transducer interface and the load interface blocks. For electrostatic vibrational harvesters this block is usually rarely address with most of the community research focusing on the transducer interface block (either the transducer itself or its synchronising electronics and the CCs).

– *Load interface* This is the output of the system, where the electrical energy is consumed by a load. This block aims to provide the load with a stable regulated DC voltage.

In chapter 2, the recent progress of energy management interfaces is described in details. Moreover, this PhD work is concerned with developing and implementing a whole system of e-VEH with focus on the energy management interface and the load regulation.

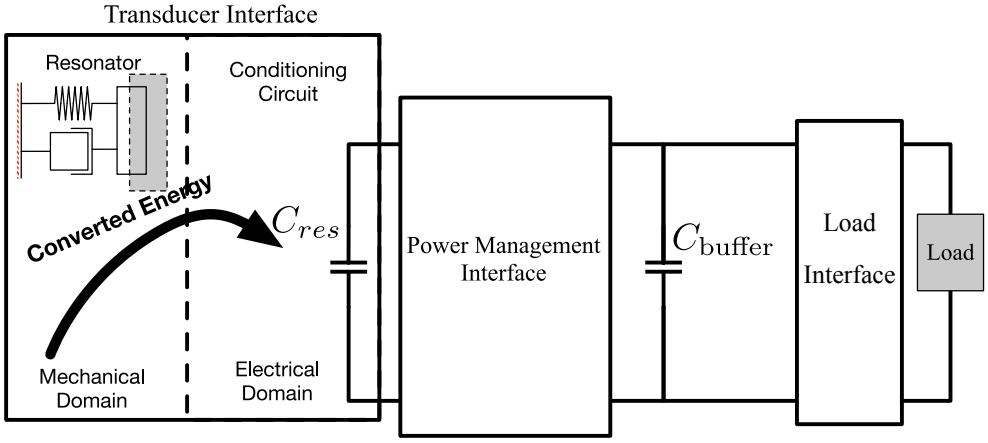


Figure 1.5: Electrostatic vibrational energy harvester systems

1.7 Electrostatic Transducers

Electrostatic transducers are usually based on Micro-Electro-Mechanical-System (MEMS) capacitors [1]. These capacitors are two terminal devices with one terminal attached to a mobile proof mass while the other is fixed to a non inertial reference frame. The variable MEMS capacitor response is described according to the direction of motion of the external vibration exerted on the proof mass. This leads to a change in one of the capacitor parameters, cf. Figure 1.6a, where the capacitance C_{var} is expressed as,

$$C_{var} = \epsilon \frac{W \cdot l}{d} \tag{1.1}$$

where ϵ is the permittivity of the medium between the two plate ($\epsilon = \epsilon_r \epsilon_0$ where ϵ_r is the relative permittivity and ϵ_0 is vacuum permittivity), W and l are the width and

the length of the parallel plates while d is the distance between the parallel plates.

It can be seen the geometry variation can be classified into: parallel movable plate, movable dielectric and gap closing capacitor Figure 1.6. The movable dielectric geometry depends on varying the effective area of the dielectric material by sliding it between the capacitor's plate. The out-of-plan parallel electrodes geometry refers to the type of variable capacitor where the effective parallel plate area varies. A gap-closing capacitor operates by varying the gap between the capacitor two plates.

The most common geometry of the variable plate capacitor in the context of energy harvesting is the gap varying capacitor [6]. For a gap-varying capacitor, equation 1.1 is reduced to,

$$C_{var} = \epsilon \frac{W \cdot l}{d_0 \pm x} \tag{1.2}$$

where x is the displacement of the movable plate as illustrated in Figure 1.6. As the gap moves towards closer the capacitance increases. The translation of the source vibration into a displacement of the variable capacitor movable plate can be simplified with the aid of two frames of reference, cf Figure 1.7. First the inertial reference (global frame) (0_Y) of which the vibration source occurs, while the second reference is a non-inertial reference frame (0_X) of attached to the source of the external vibrations.

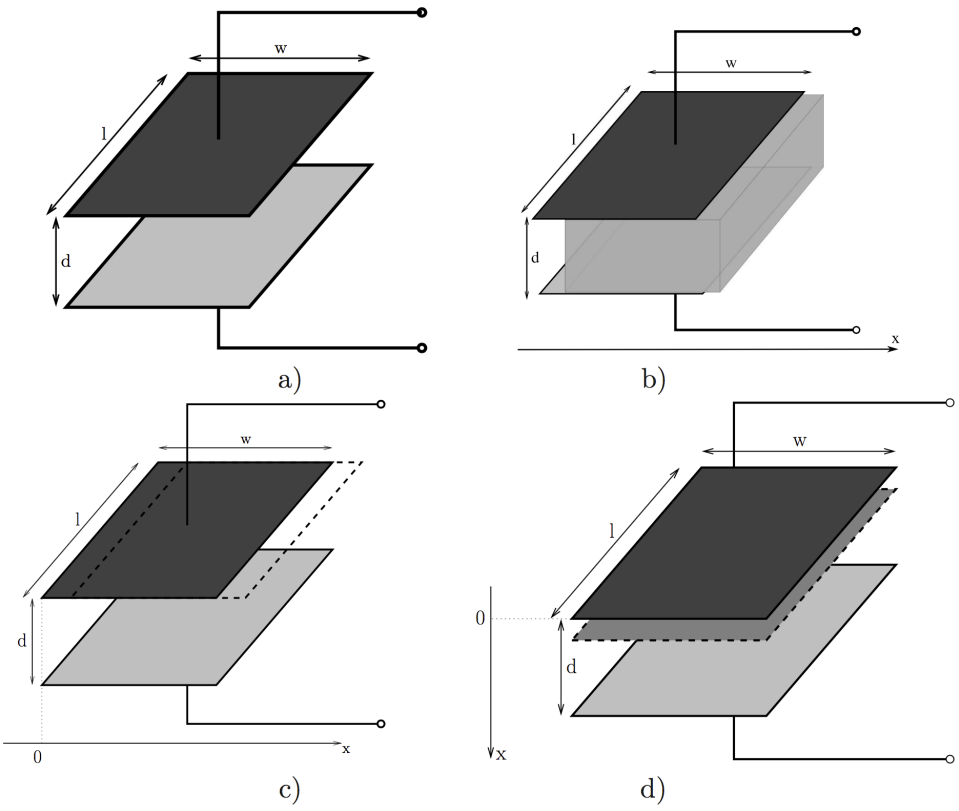


Figure 1.6: Different transducer geometries (a) parallel plate (b) a movable dielectric (c) out-of-plan parallel electrodes (d) gap-closing capacitors.

As the global reference accelerates with a_{ext}, one can write the 2nd Newtonian law

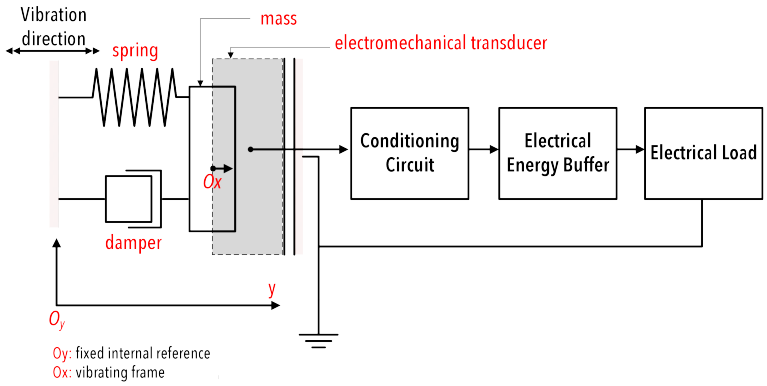


Figure 1.7: General vibration energy harvester system

for the non-inertial (second) reference frame, where the movable mass is subject to an apparent force equal $-ma_{ext}$. The principle of energy conservation states that in an isolated system the energy remains constant over time. This means that for the transducer to transform the mechanical energy into electrical energy an electrically-originated damping force on the moving mass is applied to purposely reduce its kinetic energy. In the case of parallel plate capacitor, such force is an electrostatic force which is expressed by,

$$F_{elec} = \frac{1}{2}V^2\frac{dC_{var}}{dx} \tag{1.3}$$

Where V is the voltage across the parallel plate capacitor and $\frac{dC_t}{dx}$ is the space gradient of the capacitance. Plugging in Eq.1.2 into Eq. 1.3,

$$F_{elec} = \frac{1}{2}\epsilon V^2\frac{W \cdot l}{(d \pm x)^2} \tag{1.4}$$

This shows that the electrostatic force does not scale down with the device dimensions, since both $W \cdot l$ and $(d_0 \pm x)^2$ scale quadratically, whereas mechanical forces are proportional to the linear dimensions of the spring and to the cube for the mass inertia which means that electrostatic forces are too weak to be useful at the macroscale[1]. Moreover, it can be seen that this force is dependent on the voltage V and thus the transducer mechanical behaviour can be controlled by changing biasing voltage.

1.8 Energy conversion using variable capacitor

This section discusses the energy conversion from the mechanical domain into the electrical domain using a variable capacitor. Capturing the external vibration using a resonator with the aid of interface circuit to induce an electromechanical feedback force acting on the variable capacitor. For example, consider a gap-closing variable MEMS capacitor which is exposed to an external vibration, the vibration is captured and translated into a force acting on the capacitor movable plate. This changes the capacitor "physical" parameter, in this case the gap, which in turn changes the stored energy in the capacitor. For all cases of the variable capacitors geometries the energy

stored in the capacitor is defined as,

$$U = \frac{QV}{2} = \frac{Q^2}{2C_{var}} \tag{1.5}$$

It can be seen that the stored energy is controlled by either the amount of the charges or the induced voltage difference. Allowing vibrations to decrease the capacitance of a variable capacitor while keeping its voltage or charge constant produces energy in the form of charge or voltage, respectively[23]. These are indeed the two conversion schemes which are used to transducer the mechanical energy into electrical energy using a variable capacitor. The energy conversion process can either be charge-constrained or voltage constrained. Constraining the charge generates high voltages (up to 250V) that easily exceed the breakdown limits of standard CMOS technologies [26]. However, constraining the voltage while allowing the variable capacitor to make use of the already existing energy source to drive and to sink the harvested energy into it [23].

Charge-constrained: Let us consider the scenario where the charges Q on the variable capacitor is forced to be fixed. Also, let us assume that the rest position of that capacitor is where the $x = 0$.

The proof mass attached to the movable plate induced a displacement due to the external vibration exerted on it. The new displacement d_1 is the maximum allowed displacement for the movable plate. This will force the capacitance of C_{var} to decrease which in turns will increase the voltage across the plate according to $Q = CV$. The converted energy can be calculated as the difference between the capacitor's final energy state and the initial energy state as follows,

$$\Delta U = \frac{1}{2}(C_{max}V_0^2 - C_{min}V_{max}^2) \tag{1.6}$$

where C_{max} is the initial capacitance value with an initial voltage of V_0 while C_{min} is the final capacitance reach by the capacitor corresponding to the maximum voltage of V_{max} is reached. Given that constant charge Q_0 is assumed at all time,

$$C_{max}V_0 = Q_0 = C_{min}V_{max} \tag{1.7}$$

then the converted energy can be expressed as,

$$\Delta U = \frac{1}{2}V_0^2 C_{max}(\frac{C_{max}}{C_{min}} - 1) \tag{1.8}$$

Voltage-constrained: This conversion scheme assumes that the voltage is fixed during the movement of the movable plate. Considering the rest position is when the gap is d_0 and the capacitance is at its local maximum. As the capacitance starts to decreases the charges Q decreases following $Q = CV$. The converted energy can be expressed as,

$$\Delta U = \frac{1}{2}(C_{max}V_{const}^2 - C_{min}V_{const}^2) = \frac{1}{2}V_{const}^2 C_{min}(\frac{C_{max}}{C_{min}} - 1) \tag{1.9}$$

Q-V diagrams

The Q-V diagrams present the states of the variable capacitor at different moment in time. This representation allows to easily estimate the converted energy per capacitance variation cycle. The converted energy is given by the enclosed area of the Q-V diagram. It is intuitive to use Q-V diagram as a graphical tool to analyse these two conversion schemes, constant voltage and constant charge.

Charge-constrained Q-V diagram: The Q-V diagram of charge constraned scheme is shown in Figure 1.8. The states of the variable capacitor are as follows:

– First, the capacitor C_{var} is connected to a reservoir, cf. Figure 1.8a.

– Next the capacitor decreases from C_{max} to C_{min} forcing the voltage to increases the energy stored in the capacitor from E to $E\frac{C_{max}}{C_{min}}$. During this stage the variable capacitor is isolated from the load, cf. Figure 1.8b.

– Finally, the variable capacitor is connected to a reservoir allowing to discharge the harvested energy, cf. Figure 1.8c.

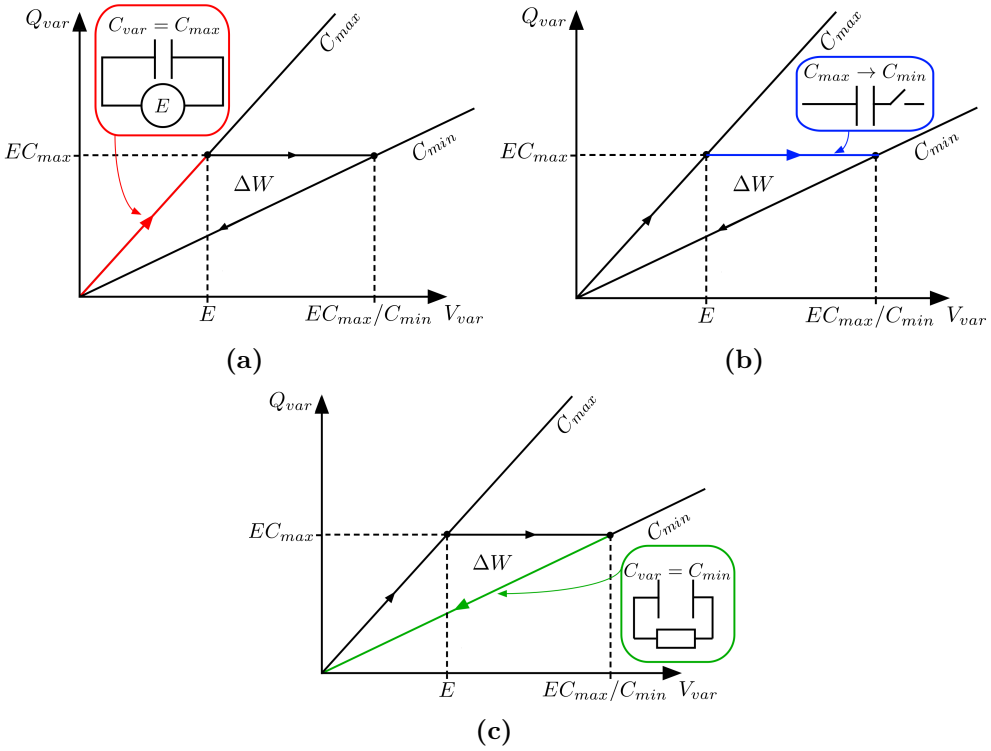


Figure 1.8: Charge constrained Q-V diagram energy conversion cycle

Constant Voltage Q-V diagram: Figure 1.9a shows the capacitor states in a constant voltage scheme. Theses states are as follows,

– First the capacitor C_{var} is connected to an energy source charging it with its initial energy until maximum capacitance V_{res} is reached.

– Next, C_{var} is allowed to decrease while fixing the voltage using a voltage source.

– Finally, the variable capacitor is connected to a reservoir allowing to discharge the harvested energy.

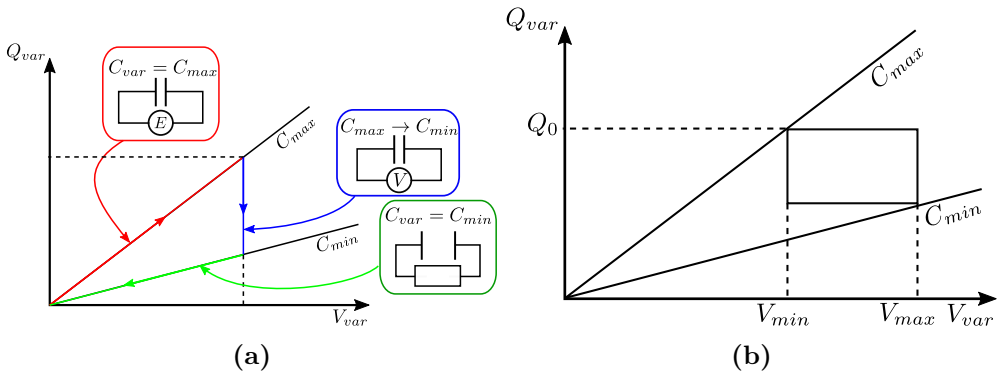


Figure 1.9: Q-V diagram for (a) Voltage constrained (b) Rectangular

For both conversion schemes the harvested energy is numerically equivalent to the area enclosed by the QV diagram. It should be mentioned that practical implementation of these schemes is hard to be achieved precisely. This is as it requires a synchronisation between the charge flow and the capacitance variation. In most implementations, a modified Q-V cycle is adopted which is called rectangular Q-V cycle, cf. Figure 1.9b.

To decide which scheme - charge or voltage constrained- is better, certain hypotheses using the Q-V diagram must be considered. If the voltage source available initially is greater than the achievable voltage then constant charge scheme will produce more energy than the constant voltage. However, if the voltage equally limited in both schemes, then the constant voltage will provide more energy.

In the previous conversation schemes, it is assumed that a certain control is imposed to fix the charge, for fixed charge conversion, or the voltage, for fixed voltage conversion. In reality this is achieved through what is called Conditioning Circuit (CC). The conditioning circuits fundamentals and their requirements as electrostatic CC are discussed in the next section.

1.9 Conditioning circuit

This section presents different conditioning circuits as well as their implementation. First a basic conditioning circuit is introduced, then a primitive rectangular Q-V conditioning circuit. This section concludes with what is called a series-parallel charge pump CC, which is used for this project.

To study the conditioning circuits CC, the variation of transducer capacitance $C(t)$ is must be defined and fully characterised as a function of time. A main hypothesis of the transducer capacitance is periodic with period T and having only one local maximum and minimum (C_{max} and C_{min}) over this period should be emphasised [1]. In reality, because of the electromechanical coupling, the $C(t)$ depends on the electrical operation of the conditioning circuit can be non-periodic. However, assuming a predetermined $C(t)$ is a necessary step in the to present CC operation and will be assumed as such in the rest of this context.

1.9.1 Basic conditioning circuit

This CC is regarded as the simplest implementation of a CC where the transducer is connected in series with a load and a large capacitor reservoir C_{res}, cf. Figure1.10. This implementation is first described in [27] to characterise an electret based transducer - see chapter 2. In this arrangement a change in capacitance will always cause a charge transfer between the two capacitors through the load resistance imposing work on the load [28]. As the capacitor's movable plate moves due to the external vibration, its

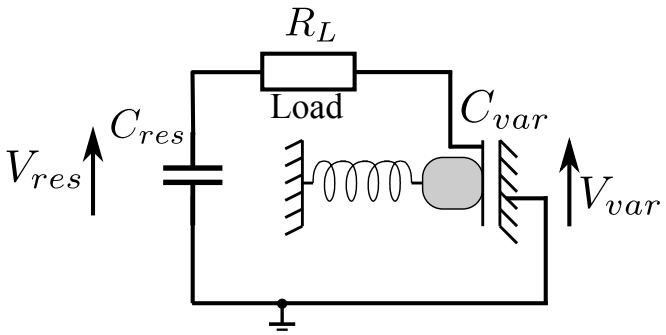


Figure 1.10: Basic conditioning circuit

charges vary resulting in a current flow $i(t)$ between the two capacitors through R_L which is expressed as,

$$i(t) = \frac{dQ_{var}(t)}{dt} \tag{1.10}$$

where Q is the instantaneous charge on the capacitance. This current dissipates power on the resistance, and this power can only come from the mechanical domain, not from the initial charge of C_{res}. Indeed, the system goes back to its initial electrical state after each periodic cycle of C_{var} since the charges on C_{var} and C_{res} are constant.

The drawback of this CC is that the load experiences an AC current with each capacitor cycles which would require a rectification step to supplying DC loads[20]. Moreover, this CC is unable to increase its internal energy [1].

1.9.2 Charge constrained CC

Another conditioning circuit implementation which is called charge constrained CC is shown in Figure 1.11a. This CC requires precise switching mechanism to insure proper energy extraction as shown in Figure 1.11b [4]. Charge-constrained CC operates as follows:

– Assuming initially $C_{var} = C_{max}$ and with charge of Q_0. With the switches $SW1$ and $SW2$ are turned off. As the C_{var} decreases by separating the plates of the capacitor due to the external vibration source, the voltage increases as the charges are forced to be constant.

– When the capacitance on $C_{var} = C_{min}$ reaches its local minimum, the switch $SW2$ is turned on, removing some charges [5] from C_{var} and moving its energy into the

[4] Figure adopted from [29]

[5] The time constant of when the capacitors is connected to the inductor is much shorter than the vibration period.

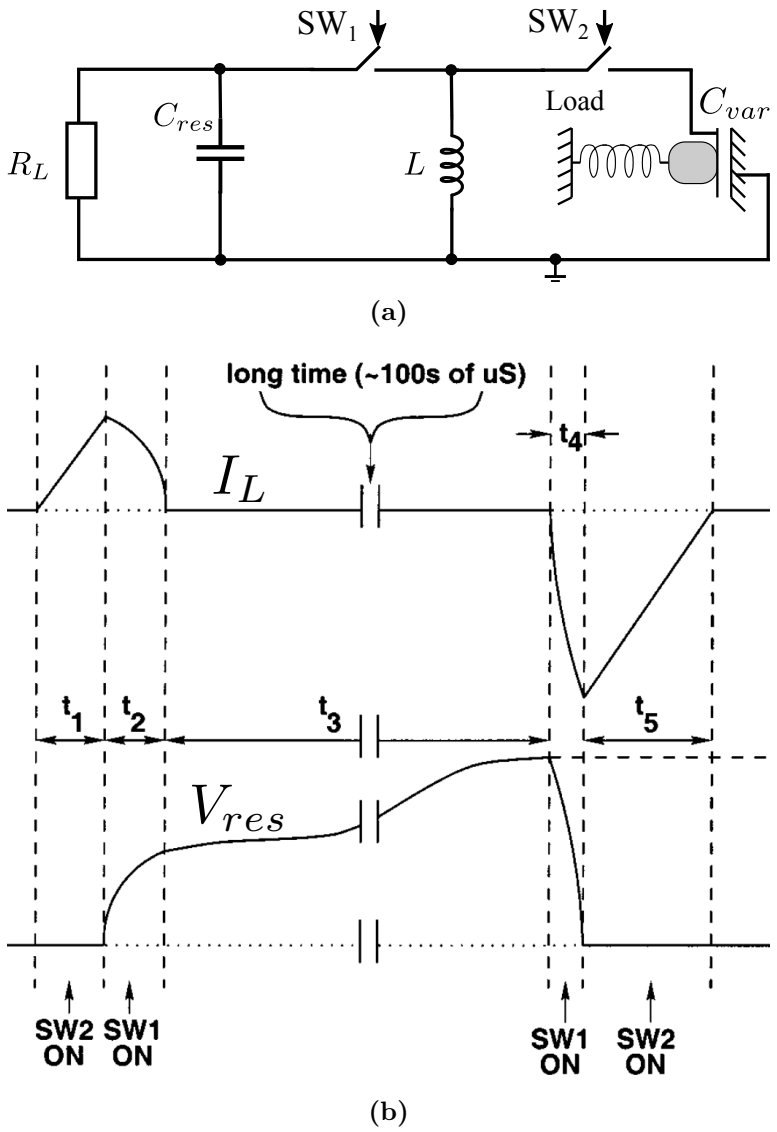


Figure 1.11: Charge-constrained CC (a) schematic (b) switching timing

inductor in the form of an inductor current i_L.

– Afterwards when V_{res} drops to zero and i_L is maximised, the switch $SW1$ is turned on and the charges removed from C_{var} are placed on C_{res} without losses. The capacitor C_{var} moves back to its maximum value.

– The process is repeated with the overall system energy increasing.

One of the first realisations of the charge-constrained cc was introduced in 2001 by Meninger et al; [29]. Another implementation was proposed later in 2005 by Despesse et al; [4]. This CC requires precise switching mechanism for the CC be able to function. In [29] a digital control was proposed with a counter and a delay line to achieve this precise switching mechanism, see Chapter 2.

1.9.3 Rectangular Q-V CC

Rectangular Q-V CC has two advantages over the two previous CC (i) rectangular Q-V cc allow self-increasing of the accumulation of converted energy starting from initially small bias. (ii) they can be implemented without external electronics to synchronise the charge from the transducer with the mobile mass[1]. Two variations of rectangular Q-V CC will be presented in this subsection: Charge-Pump CC and Series-Parallel Charge Pump CC.

Charge-Pump CC

The first implementation of rectangular QV CC was introduced by [6]. It is based on the traditional charge pump architecture and was implemented as shown in Figure 1.12.

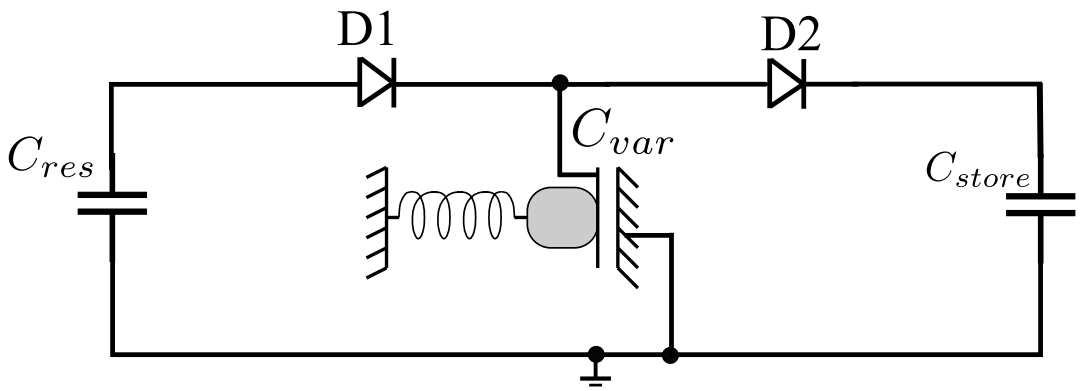


Figure 1.12: Charge Pump Conditioning Circuit

Assuming initially $V_{var} = V_{res} = V_{store}$, $C_{var} = C_{max}$ and both diodes D1 and D2 are turned off. The charge-pump CC operates as follow:

– As C_{var} decreases, V_{var} increases since the charge is kept constant.

– When V_{var} is high enough to turn D2 ON, V_{store} is connected.

– The charges are removed from C_{var} into C_{store}, dropping the voltage on C_{var}. In other words, the charges are pumped from C_{var} into C_{store}.

– The charges are pumped until D2 no longer is forward biased, and C_{var} moves from its local minimum value to its local maximum value, which decreases the voltage on C_{var}.

– As C_{var} decreases further D1 is forward biased allowing charges to move from C_{res} into C_{var}.

– As V_{var} increases reaching D1 is no forward biased, stopping the charge transfer.

– This process is repeated as C_{var} cycles between its maximum and minimum local values.

In sum, the mechanical vibrations have done a work on the C_{var} increasing the total energy stored in the system.

Practical implementation of charge-pump CC

To illustrate the charge-pump conditioning circuit, a VHDL-AMS model is used to simulate its behaviour as shown in Figure 1.13. The Charge Pump CC simulated had the following parameters similar to the one presented in [21]:

– Initial voltage on C_{res} equal to $V_{res} = 5$V
– Variable capacitor C_{var} varying between 100-200F.
– Reservoir capacitor was $C_{res} = 1\mu$F
– Storage capacitor of $C_{store} = 3n$F.

The simulation shows that after few cycles of energy harvesting and increasing of C_{store} voltage, a saturation state is reached. To ensure continuous energy harvesting process a mechanism by which charges from C_{store} is extracted is removed from the CC is needed. Most practical implementations of charge pumps conditioning circuits implement some sort of feedback mechanism, where after few energy harvesting cycles the charges are removed from C_{store} and placed on C_{res}. This could be a resistive flyback such as in [30] and [31], or an inductive flyback such as in [21].

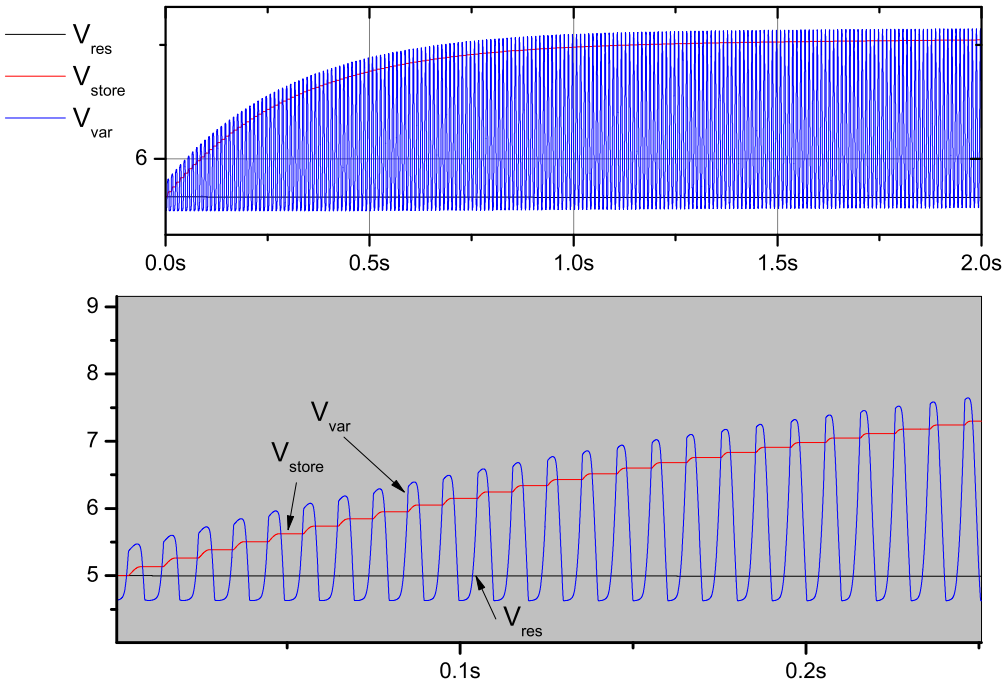


Figure 1.13: Charge-pump CC simulation

An example of the flyback mechanism is shown in Figure 1.14 where an *inductive flyback mechanism* is proposed. The flyback switching mechanism was defined by two voltages an upper and lower bound voltages. When the upper bound is reached flyback is activated while when the lower bound is reached flyback is turned off. The voltage on C_{strore} is periodically compared with these two voltages.

The charge-pump with inductive flyback mechanism simulated with and presented

in [21]. The flyback is activated at $V_2 = 9$V and deactivated at $V_1 = 6$V using the freewheeling diode and $15mH$ inductor with 31Ω winding resistance. As can be seen from the simulation, cf. Figure 1.13, the charge-pump with the flyback mechanism is able to maintain continuous harvesting process with self-increasing internal voltage on C_{res}, unlike the CC without flyback mechanism.

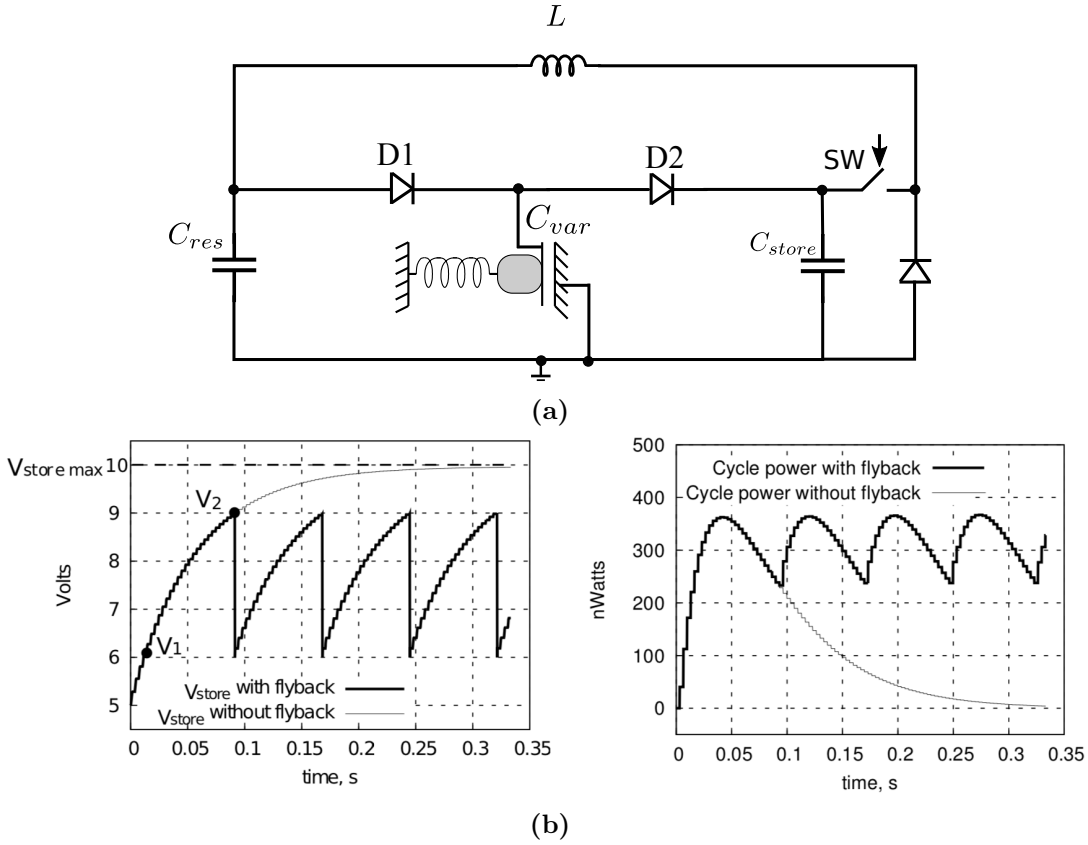


Figure 1.14: Charge-Pump CC with flyback (a) schematic (b) behaviour simulation[20]

This CC raises some issues when considering practical implementation such as:

– The voltage on C_{res} is increasing with time, and would eventually require regulation to ensure that maximum energy flux is extracted with the flyback mechanism.

– Without C_{res} regulation, the switching events which is supplied by C_{res} will vary as the voltage V_{res} slowly increases. This is due to the flyback mechanism slowly, but gradually, increases the biasing conditions of the CC when charges are removed from C_{store} into C_{res}. In practical implementations such as [21] a periodic re-calibration phase was proposed. In this implementation a semi-empirical calculation is achieved to deduce and update the two switching voltages.

Series-Parallel Charge Pump

The series-parallel charge pump conditioning circuit is a modified architecture from what is called Bennet's doubler, which was first introduced by Queriroz et al. [32] in 2014. It gained the interest of the electrostatic energy harvesting community as

it is well suited with CMOS integration when the variable macroscale capacitor is replaced by microscale MEMS capacitors. It is a new family of CCs that is capable of exponentially increasing their internal accumulated harvested energy and the energy converted at each cycle [1]. These CC are capable of continuous harvesting operation through self-increasing their internal voltage.

A generic topology for series-parallel charge-pump conditioning circuits can be seen in Figure 1.15a. It is composed of the variable MEMS capacitor C_{var} and number of voltage doubling cell. A details description of the series-parallel charge pump behaviour is found in [1, 33–35] It is worth to mention that in practical implementation this self-increasing of the internal voltage process actual reach a stopping point when the electromechanical coupling becomes dominant [33, 34].

Practical implementation of series-parallel charge-pump CC

A simulation of series-parallel charge pump CC behaviour can be seen in Figure 1.15b and 1.15c. These simulation are for a CC with C_{var} varying between $C_{min} = 100$pF, $C_{max} = 180$pF, N=2, $C1 = 1$nF, $C2 = 10$nF and $V_{var_0} = 5$V. As can be seen starting from initial low voltage invested on C_{var}, the internal voltage of the harvester exponentially increases as the variable MEMS capacitor transducer the mechanical energy from vibration into an electrical energy. Moreover, the area enclosed in the QV diagram with every cycle of the transducer increases with time indicating an increase in the harvested energy.

The drawback of the series-parallel charge pump is that after few cycles the electromechanical coupling forces become dominant stopping the converted energy from increasing. As can be seen in Figure 1.15d this behaviour of exponentially self increasing the internal voltage of the CC is not exhibited in real implementation, see Chapter 3. It is evident that to keep the energy harvesting process going on in the CC, part of the energy captured in has to be periodically extracted from the conditioning circuit.

1.10 Necessity of load interfaces

In e-VEH the harvested energy is accumulated on a reservoir capacitor, however without regulation of the internal voltage of the harvester's CC, a saturation state will occur. If part of the reservoir capacitor energy is periodically removed this will ensure that the harvesting process will not reach the saturation state. The removed energy from C_{res} is temporarily stored onto a buffer capacitor. This buffer capacitor is necessary for two reasons:

– First, the reservoir capacitor can not directly supply the loads as it has to sustain sufficient energy across it to allow the harvester to properly function.

– Second, the voltage across the reservoir capacitor is usually high to directly interface with the load, so a step down voltage converter needs to be used.

For these reasons we proposed a load interface that transfers the energy from the reservoir capacitor into a buffer capacitor. This interface is able to maintain maximum energy flux from the energy harvester. It defines the amount of energy needed to be extracted from the harvester without compromising its efficiency and transfer this

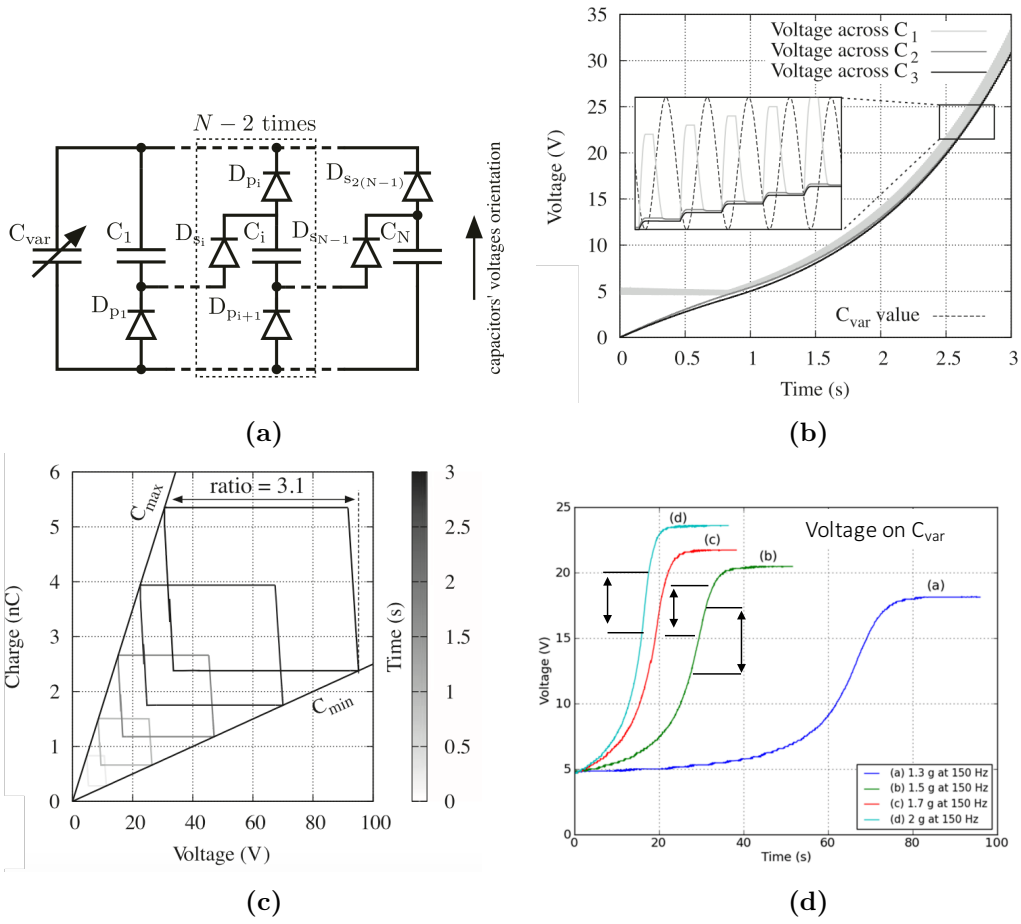


Figure 1.15: Series-parallel charge-pump CC (a) Generic topology (b) output voltage simulation (c) Q-V diagram with time (d) measurement of V_{var} for different excitation[34]

energy to a temporary storage to be later used to supply a low voltage load. This interface is responsible for the following requirements to be fulfilled:

– Regulating the reservoir voltage to its optimal mode.

– A stabilised load voltage around a nominal low voltage.

1.11 Thesis contribution

This thesis is concerned with rectangular Q-V CC. It addresses the implementation of a complete vibrational energy harvesting system as imagined in Figure 1.5. As mentioned earlier in sections 1.9.3 and 1.10, a part of the energy accumulated on the CC needs to be removed and stored temporarily onto a buffer capacitor.

This PhD work tackles this problem using the starting point of an optimum interval to extract the energy from C_{res} [34]. We propose a method of energy extraction without impacting the efficiency of the energy harvester. The amount of energy extracted as well as when this energy is extracted impact on the harvesting process will be discussed see Chapter 3. However, this function is achieved with what we call a load interface.

This thesis introduces Conditioning Circuit Regulator (CCR) which interfaces the rectangular Q-V CC to buffer capacitor. This CCR periodically extracting part of CC harvested energy into a buffer capacitor. The next step is Load Voltage Regulation (LVR) block which is responsible for regulating the output voltage within a nominal low voltage. This thesis manuscript reports the following:

- Proposed a new ultra low power architecture for e-VEH with rectangular Q-V CC load interface that is based on DC-DC buck converter.
- Provided an optimised mixed-signal load interface controller operating with an input power at least 2μW.
- Proposed a low output voltage regulator for the load in conjunction with the proposed load interface enabling a load to be periodically supplied by the e-VEH.

1.12 Chapters summaries

Chapter 1 This chapter presents the fundamentals of energy harvesting in general. It focuses on vibrational energy harvesting and more specifically electrostatic energy harvester. First we summarise the different methods of transduction of vibrational energy. Then electrostatic transduction ES advantages over other types of transduction methods are listed. These include: the high output voltage of ES, relatively low cost, and ease of integration with CMOS. Afterwards, the three main blocks of any smart electrostatic vibrational energy harvesters (e-VEH) is highlighted. These blocks are the transducer interface, the power management interface and the load interface. The transducer interface is responsible for transduction the vibrational energy into electric energy as well as conditioning the output voltage from the transducer using a conditioning circuit. Afterwards, the power management interface ensures that the conditioning circuit is operating at its maximised output energy flux rate. This is achieved by maintaining the internal voltage of the CC within its optimum interval through periodically extracting part of the CC energy and temporary store onto a buffer storage. The proposed buffer storage can be a rechargeable battery of a capacitor. The last block of the e-VEH is the load interface, which is responsible for the regulated low output voltage and supplying the load the harvested energy when available.

The rest of the chapter is dedicated to discussing the fundamentals of the electrostatic transducer, conditioning circuits and the necessity of load interfaces for e-VEHs. For the conditioning circuit, this work incorporates rectangular QV cycle CC. Even though the interface we propose can work with any rectangular QV cycle CC, yet the design of interface targeted series-parallel charge pump. This is a new family of CC with a key feature of its capability of self-increasing of the CC internal voltage starting from relatively low voltage.

Chapter 2 In this Chapter the state-of-the-art of electrostatic energy harvesters is discussed. An overview of the practical implementations in the last decade is presented, distinguishing between four main steps towards what can be called a complete e-VEH. The main characteristic to differentiate between these steps was the control electronics.

With the research in the community shifting from developing a simple transducer, to incorporating synchronised and self-synchronised conditioning circuit to a full system that takes into account the optimum operating conditions of the CC as well as the load interface. This chapter highlights the fact that a mature and smart e-VEH with both load and energy management interfaces is still not explorer within the community. The goal of this PhD work is to tackle this problem for a particular type of e-VEH CC namely series-parallel charge pump CC.

Chapter 3 In Chapter 3, we describe the architecture developed within the frame of this work. First different mechanisms which are used to transfer and manage the energy extraction between two capacitor storage is discussed. These include dc-dc interfaces that are capable of transferring the energy with minimum losses between capacitors. A justification for using buck dc-dc converter is explained with the two regulation processes that dictated by the e-VEH. The regulation process is the reservoir voltage regulation and the load voltage regulation. The reservoir voltage regulation is necessary to keep the harvesting processing from reaching saturation, while the load voltage regulation is necessary for the low output regulated voltage for the load. The reservoir voltage regulation strategies are proposed through first defining the optimum interval of the CC internal voltage. Afterwards, the load interface control technique is explained. For this work, the load interface control is achieved through a discrete-time voltage control which is explained by the aide of behaviour model simulation. Finally, one major type of losses is identified, namely condition losses. To overcome such issue, multiple energy-shots transfer is proposed. In such scheme the energy extraction from the energy reservoir to a buffer reservoir through a number of small shot instead of a single shot. This maintains the interface inductor current within an upper bound and helps mainly minimal losses during the transfer. This chapter concludes with a VHDL-AMS behaviour model for the multiple energy-shot load interface. In chapter 4 a transistor level implementation is proposed while in chapter 5 an improved implementation of the LI addressing the power consumption is addressed.

Chapter 4 In this chapter the multiple energy-shot transfer is implemented in transistor level for e-VEH load interface. This implementation promises an adequate energy transfer technique regardless of the maximum inductor current limit dictated by the LT switch. Moreover, a degree of modification for the switching thresholds is proposed using an adjustable Schmitt trigger comparator that can be used to autonomously adjust with the change of the optimum reservoir voltage caused by dynamics of the harvester. This chapter begins by describing the technology of which the transistor level implementation is proposed in. Justification for choosing such technology is listed. Next, the structure of the load interface implementation is described. This implementation had three main blocks including switching decision block, clock generator block and the switch control block. Each of the proposed blocks is described in details through out this chapter. At the core of the LI controller is a low power hysteresis comparator which is used to generate the required logical commands for the LI switch, activating/deactivating the energy extraction according to the state of the system. A sampled scaled down version of the CC internal voltage is applied to the comparator allowing this logical command generation. Other blocks include an ultra low power clock generator, zero-static current level shifter and a power switch. The chapter concludes with a complete transistor level implementation of the reservoir

voltage regulator and summary of the average power consumption of each of the LI controller blocks.

Chapter 5 A second low power load interface is proposed in this chapter. Similar to the first implementations it makes use of series-parallel charge pump CC as a conditioning circuit and a mix of high voltage interface with an ultra low power control block to maintain maximum energy harvested from e-VEH. The main focus of this implementation was to reduce the average power consumption of the LI controller and provide low output voltage regulation for the load. This required a modified LI controller architectures with a new hysteresis comparator based on RS triggers. All necessary modification required for the LI controller was carried out to reduce to reduce the power consumption. Simulated results show that the second implementation LI controller power overhead is less than 100nW thanks to an ultra low power RS-trigger based comparator.

1.13 Summary

In this chapter, the fundamental of energy harvesting was introduced. A general model of vibrational energy harvesters is presented before discussing the types of conditioning circuits. With the main focus of this PhD project around electrostatic vibrational energy harvester e-VEH , a complete e-VEH system is introduced with three main blocks clearly distinguished. These main blocks general purpose is indicated, with the target of implementing a transistor level e-VEH in the subsequent sections of this thesis.

The next chapter summaries the recent advances in electrostatic energy harvesters regarding both the transducers and the energy management interfaces. In Chapter 3, the specification of the targeted e-VEH implementation is presented. Finally chapters 4 and 5 present two complete transistor level implementation for what we call smart energy management interface for e-VEH.

Chapter 2

State of the Art for Electrostatic Vibrational Energy Harvesters

Contents

2.1 Overview

In the previous chapter the principle of electrostatic vibrational energy conversion was discussed in details. This chapter presents a literature review on what have been proposed by the community in the recent years.

First we discusses the approach towards using this transducers for energy harvesting, starting with electronics synchronising the charge flow of with the vibration movement, moving to architecture which extract the charges moving towards a complete system. Then we discuss the evolution of the vibrational electrostatic harvesters through their different steps which unfolded in the last decade. We then conclude with presenting our approach towards a complete energy harvesting system that can extract, manage, regulate and deliver the energy for a load.

Before we begin presenting the survey of different electrostatic transducers, we first distinguish between four steps starting from a simple transducer and ending up with a complete e-VEH system.

These steps can be listed as follows,

- Step 1: Primitive transducer, Figure 2.1a.
- Step 2: Synchronised transducer, Figure 2.1b.
- Step 3: Synchronised conditioning circuit, Figure 2.1c.
- Step 4: Complete energy harvester system, Figure 2.1d.

The rest of this chapter summarises the recent transducers advancements as well as the energy management interfaces. The chapter is organised as follows, first the electrostatic transducers two types (electret-free and electret-based) are discussed. A summary of the last decade progress is presented. Next, the trends of load interfaces are listed according to the steps presented in Figure 2.1.

2.2 Electrostatic transducer

This section summarise some of the proposed primary electrostatic harvesters which presented either the Step 1, Figure 2.1a, or Step 2, Figure 2.1b, towards a complete system of e-VEH. In this section we distinguish between implementations that makes use of what is called electret transducers and electret-free transducers. The implementations are presented in chronological order, with a Table 2.1 summarising the list of implementations. The capacitive electrostatic transducers can be classified into two categories according to the charging method:

- **Electret-free**. These are transducers that requires an external source of charges to harvest the vibrational energy. The external source provides the initial invested energy for the transducer before the conversion of energy takes place. They usually require active electronics to synchronise the movement of the capacitor with the movement of the charges[23].
- **Electret-based** These are transducers that uses an electret material to maintain the charge of the electrostatic converter through time. Electrets are dielectrics able to keep an electric field , as shown in Figure 2.2 in the form of a surface voltage for years by trapping the charges on the surface [36].

2.2.1 Electret-Free transducers

This section presents electret-free transducers implementations. This kind of transducers requires a source of charges and thus would also require some managing electronics to operate. Most of electret-free transducers are either implementing the scheme presented in 2.1b or 2.1c.

The first electret-free e-VEH develop as a comb based VEH was presented in 2001 by Meninger et al; [29]. This implementation presented a prototype that is capable of delivering a 8μW of usable power. The synchronisation mechanism was based on inductor switching as was presented in section 1.9.2. In 20103 Roundy et al. [6] proposed an in-plane gap closing e-VEH that is capable of delivering up to $100\mu\text{W/cm}^3$ harvested power using an external vibration source with $2.2m/s^2$ at 120Hz. In 2005

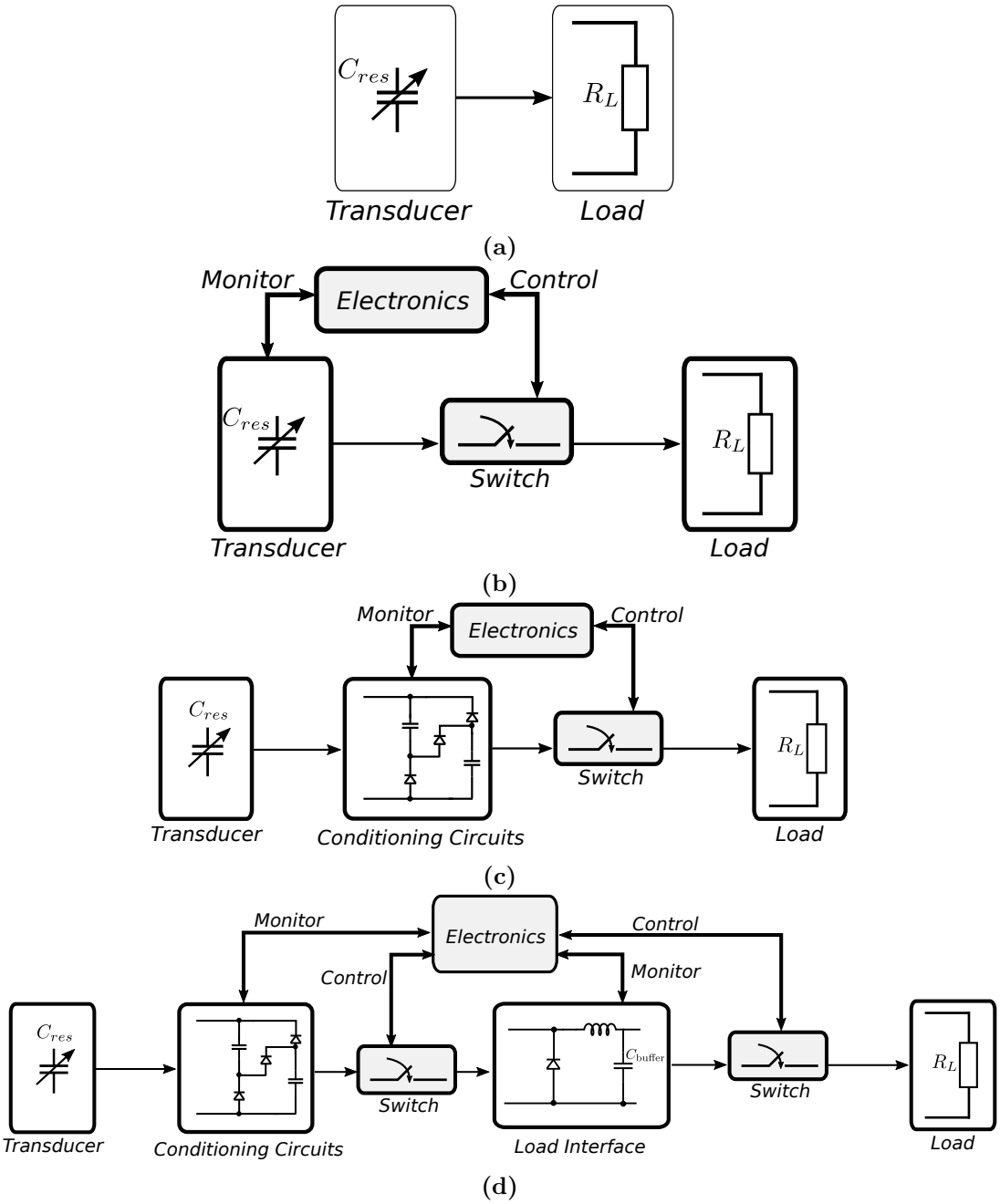


Figure 2.1: E-VEHs progress showing (a) Primitive transducer (b) Synchronised transducer (c) Synchronised conditioning circuit (d) Complete energy harvester system

Despesse [37] et al. proposed an e-VEH that is able to provide harvested power of 1mW with a 0.2g vibration source at 50Hz. It must be noted that all the previous examples of electret-free transducers used charge-constrained scheme to harvest the energy with inductive-switching to synchronise the energy extraction, see section 1.9.2, . In 2011 Hoffmann et al [38] developed a triangular electrode electrostatic energy harvester

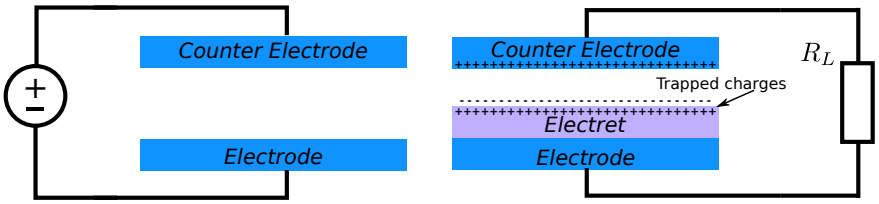
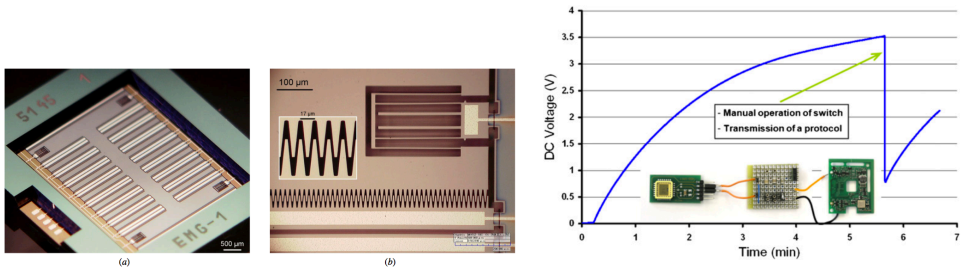


Figure 2.2: Electret-Free (Left) versus Electret (Right)

that provides higher capacitance per unit displacement 2.3a. This harvester was able to harvest 123μJ of energy into a 20μF capacitor given a bias voltage of 15V and the acceleration amplitude of 2ms^{-2}. The energy was accumulated then manually release using a wireless transmitter model that was charged to 3.5V in 5.7 minutes.

In this work, a first implementation of a simple conditioning circuit CC was introduced. This CC was was a full wave rectifier and it implements in a continuous circuit scheme using two complementary variable MEMS capacitors. This scheme of harvesting the vibration energy is shown in Figure 2.1d where the transducer movement and charge accumulation is synchronised using a CC and the energy is to a load. The load interface was a simple full-wave rectifier which does not take into account extracting the energy efficiently from the CC. Moreover, the energy was released with manual triggers to the load - wireless transmitter - when enough energy was accumulated on the buffer capacitor as shown in Figure 2.3b. Even-though this implementation was permeative in terms of the a whole e-VEH, yet it indicated the main block necessary to build a complete e-VEH.



(a) **(b)**

Figure 2.3: E-VEH presented in [38] (a) Microscopic images (b) Voltage characteristic of the storage capacitor using a transmission module.

2.2.2 Electret-based transducers

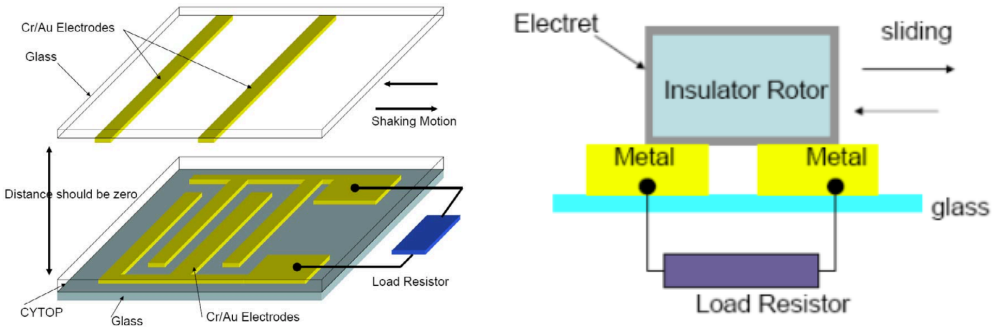
These are variable capacitors with electret material between its plates. It has the capability to directly transform the mechanical energy into electrical energy [1].

In 2007 Loa et al [46] developed an electret based e-VEH that operates in low frequency. The prototype proposed in Figure 2.4a was capable of producing an output power of 2.26μW through an output load of 40MΩ. The measurement was achieved through at a vibrating source frequency of 60Hz.

Table 2.1: State-of-art for electret-free electrostatic transducer

Source	A_{ex} [g]	f [Hz]	Power [μW]	Load [Ω]	Precharge [V]	Year
Meninger [29]	n/a	2200	8	n/a	5	2001
Mitcheson[39]	n/a	41	0.0072	n/a	30	2004
Despesse [37]	9.36g	50	70	n/a	40	2005
Bartsch [40]	n/a	1738	n/a	340kΩ	70	2007
Basset [41]	0.25g	250	0.061	60MΩ	n/a	2009
Yang [42]	0.25g	63	0.39	80MΩ	n/a	2010
Choi [43]	n/a	5	35.3	n/a	1	2011
Hoffmann [38]	5.1g	1075	0.82	60kΩ	20	2011
Basset [44]	n/a	150	2.2	5.4	30	2013
Lu [45]	2g	15	2.8	6.6MΩ	20	2017

Later in 2008, Lao et al [47] improved there prototype through using parylene HT as the electret material and a new design that both electrodes are on the stator plate and the rotor are in an insulator blocks coated with electret material. The device was able to harvest a maximum output power of 17.98μW at 50Hz through a load of 80MΩ .



(a) **(b)**

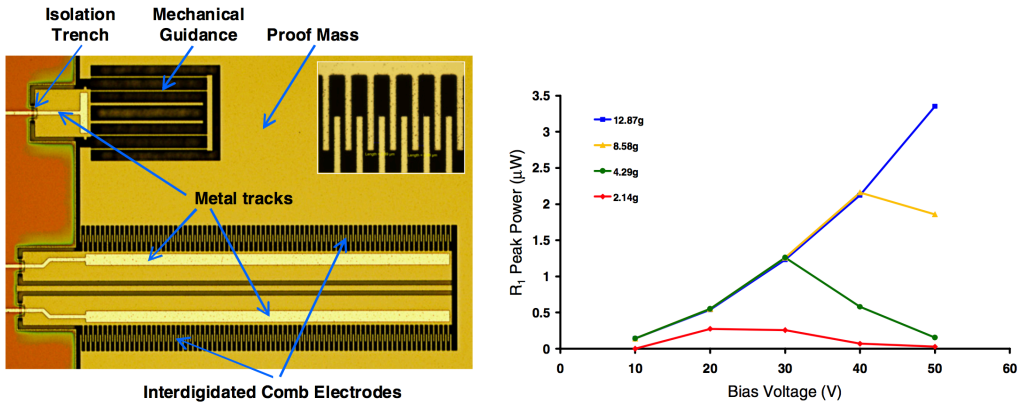
Figure 2.4: Schematic of energy harvester presented in (a) [46] (b) [47]

In 2009, Hoffmann et al [48] developed an electrostatic micro-generator shown in Figure 2.5a. It is capable of extracting vibrational energy and delivering up to 1.58 μW average output power. It is packaged in 0.2cm^3 volume using a modified SOI technology developed for inertial sensors at HSG-IMIT. Experiment results highlighted two important results:

– An optimal bias voltage where the output power is maximal exists. Thus, the bias voltage has to be considered as a design parameter with respect to the excitation conditions of the corresponding application [48].

– At larger excitations above a critical level the mechanical stoppers come into effect causing the output power to flatten and weakly decrease, cf. Figure 2.5b [48].

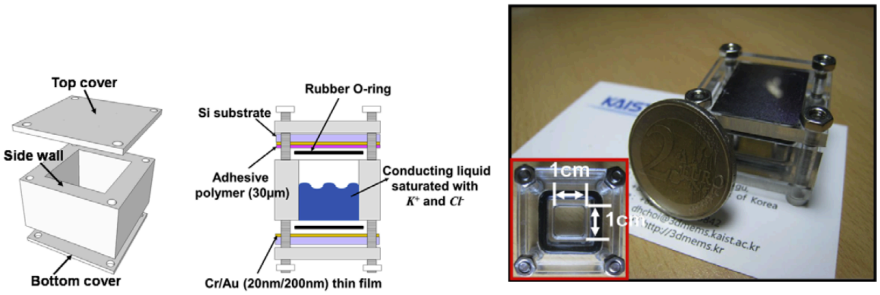
In 2011 Choi et al [43] reported a liquid based electrostatic energy harvester shown



(a) (b)

Figure 2.5: Electrostatic harvester presented in [48] (a) Microscopic view (b) Experimental results showing bias voltage effect using a load resistance of 560kΩ

in Figure 2.6. The harvester a variable capacitance ranging between 10 nF and 5pf which ensures a high capacitance ratio of 2000. It is capable of theoretical energy generation of 45.3μW at 5Hz periodic vibration excitation. The harvester uses a charge-constrained conversion and an auxiliary voltage of 1V. overall device size was 1 cm^2.



(a) (b)

Figure 2.6: Proposed device in [43] (a) a conceptual view (b) fabricated prototype[43]

In 2013 Altena et al [49] presented a method of an *electret-based MEMS vibrational* electrostatic energy harvester that is capable of producing up to 175μW of power shown in Figure 2.7. This two order of magnitude high output power is due to a different electrical connection principle of the harvester and an optimised geometrical configuration of the electrodes. The devices was tested under sinusoidal excitation with acceleration of 2.5g at 1187Hz frequency and optimum load of 3.2MΩ. The electret potential is 200V and device size of 1cm^2.

In 2013 Chiu et al [50] reported an out-of-plane *electret* vibration energy harvester made of Copper plates and flexible printed circuit board (FPCB). It can produce output power up to 20.7μW with 50MΩ load. The measurement is given an external vibration source of 110Hz and 2g acceleration. The electret potential was 400V and the whole device size was 4cm^2. Wang et al [51] developed advice of 1.43cm^2 device. It is

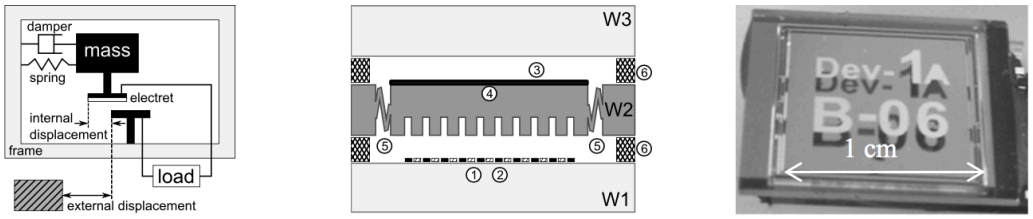


Figure 2.7: Left: schematic, middle: device cross section Right: Top view [49].

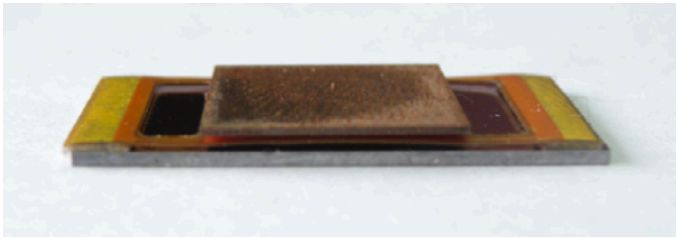


Figure 2.8: Proposed harvesters presented in [50]

capable of producing up to 0.15μW power when connected to external load resistance of 13.4MΩ. The vibration source had 1g at 96Hz.

In 2014, Tao et al; develop a 3 dimensional electret based harvester that supports a multiple vibration mode. They proposed a rotational symmetrical resonator as shown in Figure 2.9. Electret material was charged through corona charging method and the harvester prototype was able to produce 4.8nW of power given an external vibration acceleration of 0.05g[52].

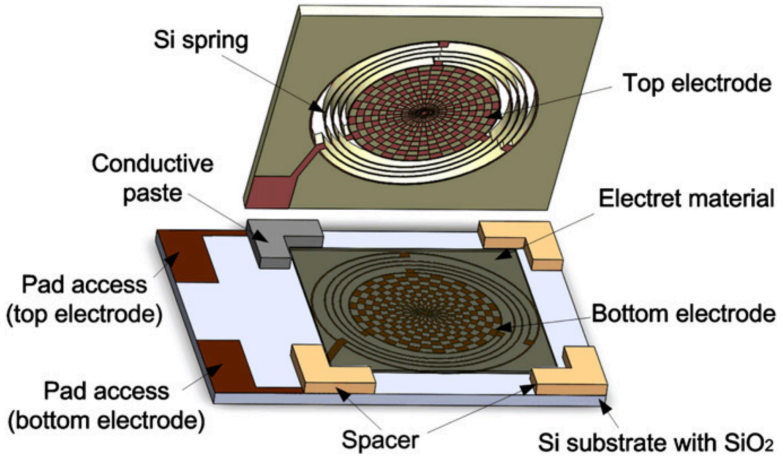
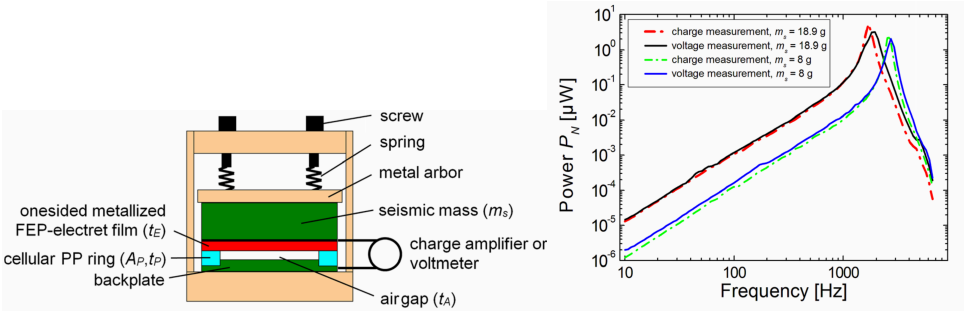


Figure 2.9: Schematic of the energy 3-dimensional harvester proposed in [52]

In 2015 J. Hillenbrand et al; proposed a vibration-based electret energy harvesters with soft cellular spacer [53]. The proposed harvesters were designed to work with acceleration of 8g to 23g and surface potentials in the 500V regime. It shows a measured harvested power of up to 8μW at 2 kHz and an acceleration of 1g. This soft

cellular spacer design has several advantages over traditional design such as a compact design as the harvesters is slightly larger than the seismic mass. This means that these harvesters can operate with low resonance frequencies (< 100 Hz) and produce with relatively high output power. Figure 2.10 shows an illustration of the proposed design as well as the measured normalized power.



(a) **(b)**

Figure 2.10: Proposed e-VEH by[53] (a) schematic (b) harvested power

In 2015 Perez et al [54]; an airflow energy harvester was presented using an electret-based conversion to turn the air flow into membrane movement and in turn into electrical energy. The device proposed was implemented in 25μm thick Teflon PTFE electret layer as shown in Figure 2.11. The device is able to harvest up to 2.1mW output power with a 3g acceleration vibrating source with of 300Hz. The measured output was the optimal load of 14MΩ.

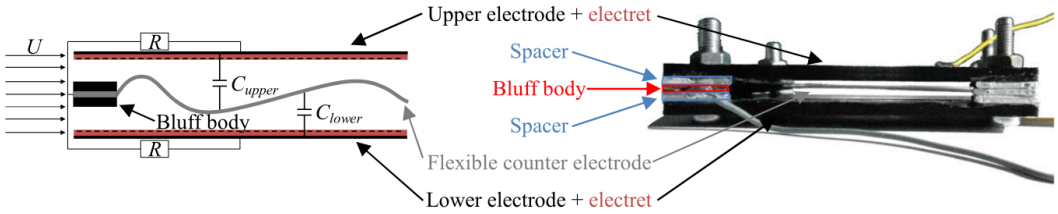


Figure 2.11: Flutter-and-electret-based airflow energy harvester by [54]

Later in 2017 Tao et al [55] developed an improved version of the electret based vibrational energy harvester. The new design was a sandwich structure MEMS that has two opposite charged electrics integrated into a single electrostatic device. With overall devices package of 0.24cm^3 size, it generates a power of 0.22μW with a vibration acceleration of 1g with 122Hz and a load of 30 MΩ. Adopting this new MEMS structure resulted in a direct improve of e-VEH performance compared to the perviously introduced model with the output voltage increased by 80.9% with an input acceleration of 5ms^{-2}.

Table 2.2 summarises most of the recent implementations of electret-based transducers in the energy harvesting community.

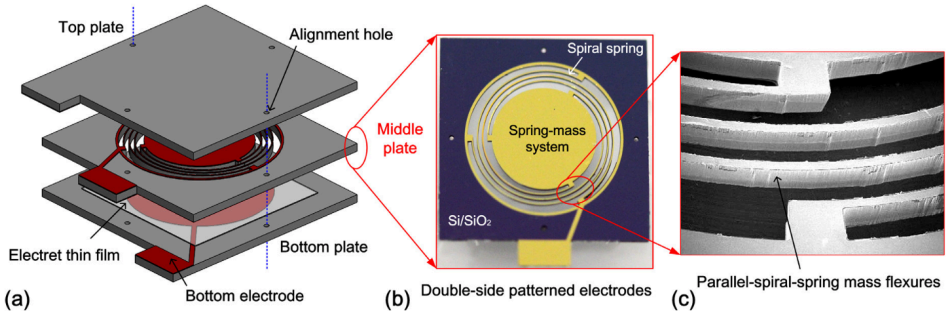


Figure 2.12: Proposed device by [55] (a) three-plate MEMS e-VEH schematic (b) device optical image (c) parallel-spiral-spring flexures and disk-shaped seismic mass SEM

Table 2.2: State-of-art for electret-based electrostatic transducer

Source	A_{ex} [g]	f [Hz]	Power [μW]	Load [Ω]	Year
Boland [56]	7.1g	50	6	12MΩ	2005
Tsutsumino [57]	1.5g	20	37.7	60MΩ	2006
Lo [46]	14.2g	60	2.267	40MΩ	2007
Lo [47]	4.93g	50	17.98	80MΩ	2008
Sakane [58]	0.9g	20	700	2.5MΩ	2008
Edamoto [59]	0.87g	21	12.5	8.5 MΩ	2009
Hoffman [48]	13g	1460	3.5	560kΩ	2009
Naruse [60]	0.4g	2	40	7MΩ	2009
Jang [61]	0.7g	20	5.9	6.26kΩ	2011
Boisseau[36]	0.9g	50	50	300MΩ	2011
Altena [49]	2.5g	1187	495	3.2MΩ	2013
Chiu [50]	2g	110	20.7	50MΩ	2013
Bu [62]	2.5g	120	0.66	36.5MΩ	2013
Wang [51]	1g	96	0.15	13.4MΩ	2014
Tao [52]	0.05	66	$4.80 \cdot 10^{-3}$	60M Ω	2014
Perez [54]	1.3g	406	2100	14MΩ	2015
Tao [55]	1g	122.1	22	30MΩ	2017

2.3 E-VEH with energy management interfaces

This section discuss energy management interfaces for the e-VEH. As was shown in Figure 2.1, we distinguish between four type of e-VEH with a key parameter to differentiate between these interfaces is the monitoring electronics. The first step, 2.1a, lacks any monitoring electronics that synchronise the charge movement with the interface. The second step, Figure 2.1b, includes synchronising electronics allowing a synchronised charge movement from the transducer to a load or a capacitor. The third step, Figure 2.1c, rely on CC to autonomously accumulated the harvested charges on a storage capacitor and uses monitoring electronics to control the energy discharge on a load when enough energy is accumulated.

2.3.1 E-VEH Step 1: Primitive transducer

This is the simplest implementation of the vibrational harvesters implementation where the variable capacitor is directly connected to the load. These implementation are usually used either characterise the MEMS transducer.

Few implementations of such interface were presented in 2009 by Paracha et al.[41], in 2011 by Boisseau et al. [36] and in 2013 by Bu et al. [62]. In this interface the variable MEMS capacitor is connected directly to a reservoir which could be capacitor or a resistive load as shown in Figure 2.13. These kinds of interfaces has several drawbacks including:

– They are not capable of synchronising efficently the charge movement with the capacitor mechanical movement. This results in harvested energy loss [23].

– They are not able to self-increase their internal energy. This lead to eventually stopping of the harvesting process [1].

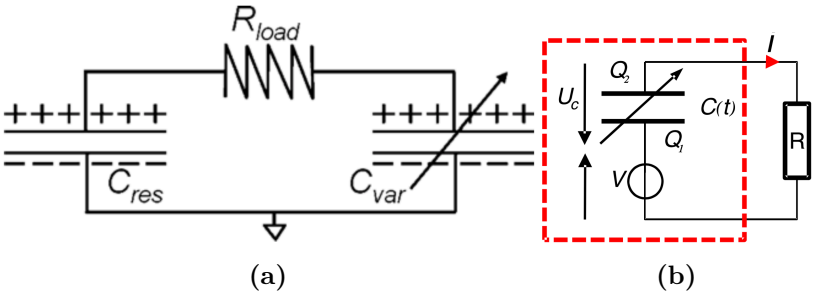


Figure 2.13: Energy extraction mechanism proposed in (a) [41] (b) [36]

2.3.2 E-VEH Step 2: Synchronised transducer

In these e-VEH interfaces the main concern is to synchronise the charge movement, thus the interface controller relied on sensing the variable MEMS capacitor voltage to activate the extraction mechanism, cf. Figure2.1b. Examples on such interfaces was reported in [6, 23, 24, 29].

As can been in Figure 2.14a Meninger et al. proposed an switched-inductor interface that synchronises the switching event for SW1 and SW2 with the variable capacitor to achieved efficient energy extraction, see section 1.9.2. The drawback of such implementation is that the controller assumes known and fixed operating condition prior the harvesting process. This however is not possible when considering harvesting energy from ambient vibration source.

In the proposed implementation by Torres et al. a load interface which precharges, detects, and synchronises to a variable voltage-constrained capacitor was presented [23]. The variable MEMS was an electret-free and thus required a battery which was used as both the voltage-constraining device and precharging source. As can be seen in Figure 2.14b the proposed interface had a state detector to distinguish between the different states of the variable capacitor and generate the appropriate switching signals to either extract or. replenish C_{var} charges.

In step 2, the main focus was to achieve proper synchronisation of the variable

MEMS capacitor according with the charge extraction through switches and sensing electronics, this however was partially abandon with the adoption of self-synchronised conditioning circuits as will be shown in step 3.

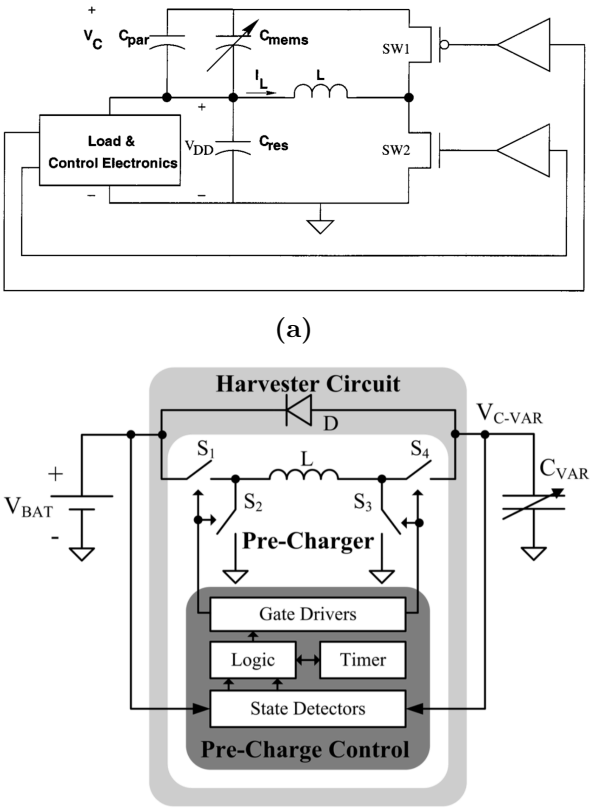


Figure 2.14: Synchronized energy extraction by (a) Meninger et al. [29] (b) Torres et al.[23]

2.3.3 E-VEH Step 3: Synchronised conditioning circuit

In step 3 most of the research of the community shifted towards investigating self-synchronised conditioning circuits. These were CC based on charge-pump and was able to achieve energy extraction from the variable MEMS capacitor thanks to replacing the switches with a network of diodes.

Such interface first implementation was introduce by Roundy et al. in 2002 [6] It relied on charge pump arrangement and later in 2004 replaced the switches with diodes, cf. Figure 2.15a and section 1.9.3. This type of interface allowed self-synchronisation of the charges with the variable capacitor movement, however as was shown in section 1.9.3 it suffers from saturation after few harvesting cycles. In 2005 Ben Yen et al. [24] proposed a flyback mechanism as shown in Figure 2.15b and in 2011 Dudka et al. [21, 63] proposed an improved version with a self-calibrated flyback thresholds. In 2011 Querioz et al.[64, 65] proposed a new CC based on Bennets doubler. It has gained the interest of the electrostatic harvesting community since then such as [33, 66–68].

In all of implementations proposed in Step 3, the interface control from step 2 was replaced by improved self-synchronising CC and thus the controller electronics shifted from monitoring the transducer to monitoring the internal voltage of the CC. The load interface in this stage was merely addressed.

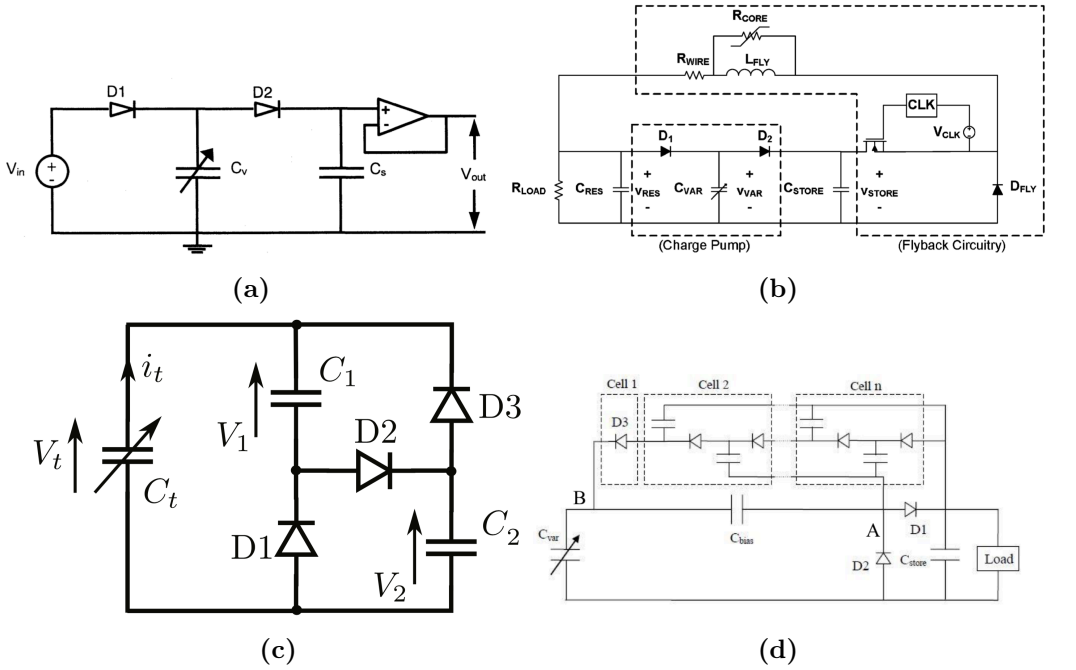


Figure 2.15: Self-Synchronized energy extraction showing (a) Charge-Pump by Roundy et al. [6] (b) Charge-pump with flyback by Yen et al.[24] (c) Bennet's doubler by [33] (b) Modified Bennet's doubler by [67]

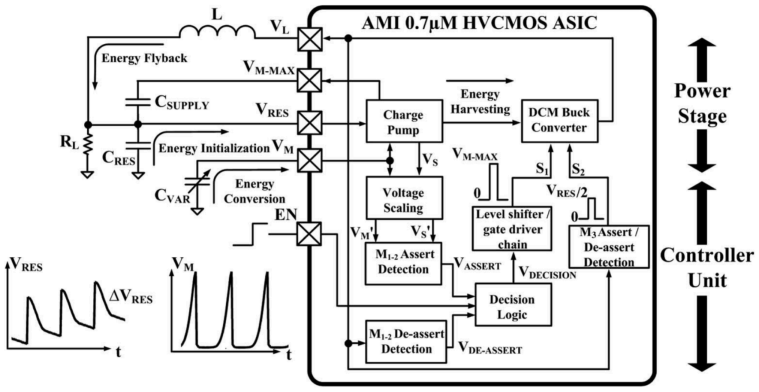
2.3.4 E-VEH Step 4: Complete energy harvester system

In this step of load interfaces implementation, a whole system is considered from the transducer synchronisation, conditioning of the voltage and load interfacing as shown in Figure 2.1d. Only few groups have proposed a complete system as such, since the main focus was on the harvester itself. With the transducer and its conditioning circuits becoming more mature and fully characterised and analysed it is now most appropriate to address the implementation of a whole e-VEH system.

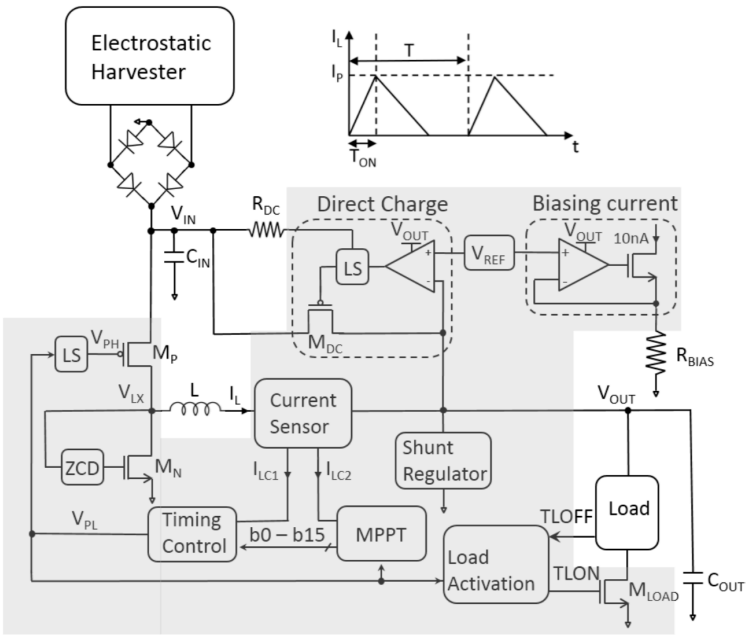
One of the preliminary implementation was done by Asantha Kempitiya et al. [25, 69] in 2013. They proposed a low power energy harvesting circuit that performs synchronous energy harvesting on tri-plate variable capacitor. The proposed design was a charge pump CC architecture implementing a charge constrained energy conversion. The power IC control was implemented in AMI0.7μm high voltage CMOS process. The overall harvester implementation was capable of generating a 308nW (at 98Hz vibration). This implementation presented a new class of micro generators with the potential for higher energy conversion than regular electrostatic energy harvesters.

More recent attempt for an efficient electrostatic energy harvesters is done by Stefano et al [70, 71]. The implemented a high voltage and low power inductive

DC-DC buck converter for e-VEH interface. The implementation was done using TSMC 0.25μm CMOS technology and included a maximum point tracking algorithm for matching the the internal impedance of the harvester and AC-DC converter. This approach usually has a drawback of complex digital processing or a simple but analog to perform the Maximum power point tracking (MPPT). The reported measured peak end-to-end efficiency is 88% and control average power of 5000nW and does not operate under 25μW available power. An improved version of the harvester interface was proposed later on by the same team on 2015 that is capable of operating with input power under 1μW and with a controller average power of 500nW.



(a)



(b)

Figure 2.16: Complete e-VEH system proposed by (a) Kempitiya et al. [25] (b)Stanzione et al. [71]

2.4 Summary

In this chapter a summary of electrostatic energy harvesters was discussed. A distinguish between four chronological steps of e-VEH system was proposed. These steps summarises the progress done towards a complete e-VEH system from a simple transducer to conditioning circuits and ending with a system employing an energy management interface. With the recent advances in e-VEH CC it is now more challenging to introduce a complete e-VEH system that is capable of managing the harvested power, maintaining a maximised energy flux rate and regulating a low output voltage for a load. In this thesis work, we propose a harvester interface as shown in Figure 2.1d, in Chapter 3 the fundamentals of the load interface is discussed and in Chapter 4 and Chapter 5 CMOS implementation of such interface is proposed.

Chapter 3

Load Interface for E-VEH

Contents

3.1 Overview

This chapter describes the architecture developed in this thesis for interface between two energy storages: an internal capacitor of a conditioning circuit (called a reservoir capacitor) which receives the energy converted from mechanical domain and a capacitor supplying a low voltage load (called buffer capacitor), cf. Figure 3.1. This interface transfers the energy of the reservoir capacitor while fulfilling the requirement applied to this transfer (sec. 1.10) :

– The voltage on the reservoir is regulated as required by the optimal operation mode of the conditioning circuit.

– The voltage of the load is stabilised around the nominal low voltage.

– If the voltage of the reservoir is much larger than the voltage of the load (this is a typical situation in electrostatic harvesters), the energy transfer should be as efficient (lossless) as possible.

After a short review of DC-DC interfaces (sec.3.2), we present the design steps justifying the architecture of the load interface selected in this work.

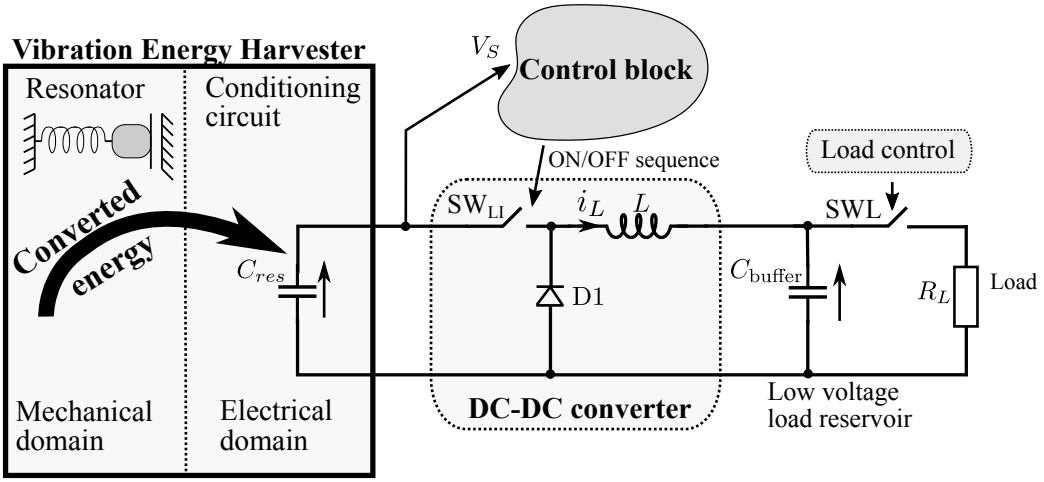


Figure 3.1: Overview of the system Blocks for a e-VEH

3.2 Review of DC-DC Interfaces

A DC-DC interface generates a required DC voltage using a voltage source with a different DC voltage. In majority of cases, the DC-DC converters are used for the power supply generation. According to the particular applicative context, different requirements are applied to them: stabilization of the output voltage (voltage regulators), minimization of the voltage loss (Low Dropout Voltage, when the required output voltage is comparable to the input voltage), minimization of the conversion losses... In the case of capacitive energy harvesters, the main attention of DC-DC converter designers is a delivery of the maximum of energy generated by the harvester to the load, while respecting the required load operation conditions: the nominal load voltage and the voltage regulation.

In the majority of the harvesters, the available output voltage is very low, and the challenge is a stepping up of the output voltage (e.g., RF powering interfaces, thermoelectric generators, miniature electromagnetic converters, etc). In the capacitive harvesters, the output voltage is generally *much higher* than the voltage required by the load. Hence a stepping down is required. Generally, it means that the harvested energy is accumulated in a high-voltage capacitor (the reservoir capacitor), and it must be transferred to a capacitor having a large capacitance and a low voltage (a load capacitor).

The circuits used for a transfer of energy between two capacitors are similar to the conventional DC-DC converters, although their modes of operation are slightly different. In this section, we present three types of capacitive interface: (a) Resistive interface, which is a trivial topology, but whose analysis emphasizes the problem of the energy transfer in capacitive networks, (b) interface based on Buck-Boost DC-DC topology, (c) interface based on Buck topology. The section will conclude with a justification of the choice of the Buck converter interface for this PhD project.

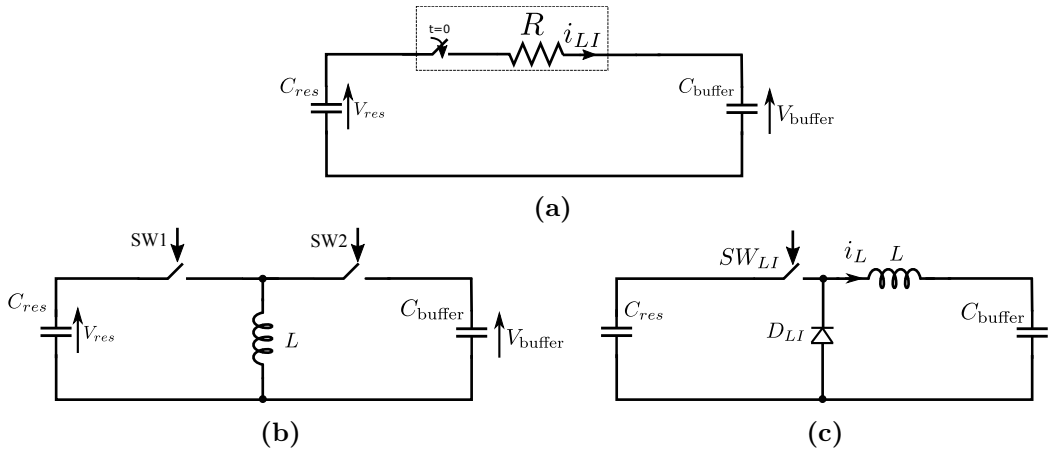


Figure 3.2: Load interfaces (a) Resistive (b) Buck-Boost (c) Buck Interfaces

3.2.1 Resistive interface

Resistive interfaces - cf. Figure 3.2a - are the simplest form of interface allowing an energy transfer between two capacitors. Such an interface allows to transfer energy from a high voltage capacitor to a lower voltage capacitor, and never to the opposite direction. The advantage of these interfaces is their simplicity. Unfortunately, the energy transfer is done with some incompressible losses, which cannot be reduced by any design effort.

Energy transfer between two identical capacitors: Let us assume that two capacitors C_{res} and C_{buffer} charged to V_0 and 0. For simplicity and demonstration purposes, we suppose them identical with capacitance C. Suppose, the goal is to transfer as much energy as possible from C_{res} to C_{buffer}. Initially, all system energy is stored in C_{res}, and is equal to:

$$U_0 = U_{res_0} = \frac{CV_0^2}{2} \tag{3.1}$$

When the two capacitors are connected, the charges are redistribution between them. Since the two capacitors are identical, the charges are distributed equally between each capacitor and their voltages become $V_0/2$. The of energy stored in the system after the transfer is,

$$U_{final} = U_{res} + U_{\text{buffer}} = \frac{CV_0{}^2}{4} = \frac{U_0}{2} \tag{3.2}$$

It is to be noted that the final energy of the system does not depend on the value of the resistance, which suggest that this loss is structural, and can't be reduced by

a design effort, for example, by reducing the resistance of the connexion R. This is known as capacitors energy paradox [72]. Indeed, the direct calculation of the energy lost in the resistance R gives:

$$U_R = \int_0^\infty i_R^2 R = \int_0^\infty (\frac{V_r es_0}{R} e^{\frac{-2t}{RC}})^2 R dt = \frac{CV_0^2}{4} = \frac{U_0}{2} \tag{3.3}$$

so that the lost energy does not depend on the resistance value, and so the loss cannot be reduced by minimizing the resistance.

The situation will be even worse if $C_{load} \gg C_{res}$: in this case, the part of the energy lost in the resistance will be close to $1 - C_{res}/C_{load}$.

Because of this structural loss, resistive interfaces are seldom used in the energy harvesters. The next two interfaces presented in subsections 3.2.2 and 3.2.3 overcome this drawback.

3.2.2 Buck-Boost DC-DC Load Interfaces

The only way to transfer energy between two capacitors without losses is to use an inductor as an intermediate energy transfer medium. A Buck-Boost interface is the most generic and straightforward solution for that, cf. Figure 3.2b.

The network includes the two capacitances C_{res}, C_{buffer}, an inductor and two synchronised switches - SW1 and SW2 and a some control unit generating switching commands.

Buck-Boost Interface Operation: Let us assume the reservoir capacitor C_{res} is initially charged to V_{res_0}, the buffer capacitor C_{buffer} charged to zero, and the switches are off. The goal of the network is to extract some predefined quantity of energy ΔW from C_{res}, and to transfer it to C_{buffer}. The switching events corresponding to the Buck-Boost operation are given in Figure 3.3.

Switching on of SW1 for τ_1 extracts the energy from the reservoir and transforms it into magnetic energy in the inductor L. When the required energy is extracted from C_{res} the switch states are complemented for a time τ_1. The energy is transferred from the inductor onto C_{buffer}.

– After the energy transfer is completed the switches are turned off. This process is repeated when energy extraction is needed.

The switching time τ defines the energy ΔW to be extracted from C_{res}. If all the energy of C_{res} is required to be extracted, the time τ has to be equal to quarter resonant period, i.e $\tau = \frac{\pi}{2}\sqrt{LC_{res}}$. When initially charged to zero, after the transfer the buffer capacitor C_{buffer} raises its voltage to,

$$V_{\text{buffer}} = \begin{cases} V_{res}\sqrt{\frac{C_{res}}{C_{\text{buffer}}}}, & \tau = \frac{\pi}{2}\sqrt{LC_{res}} \\ \frac{V_{res}}{\sqrt{LC_{\text{buffer}}}}\tau, & \tau < \frac{\pi}{2}\sqrt{LC_{res}} \end{cases} \tag{3.4}$$

The principle of energy transfer doesn't change if the buffer capacitor has a non-zero initial energy. The Buck-Boost architecture allows a transfer whatever is the ratio between V_{res} and V_{buffer}, even if $V_{\text{buffer}} > V_{res}$. This is a strong advantage of the Boost-Buck topology, in particular, comparing to the resistive interface, where a transfers requires $V_{res} > V_{\text{buffer}}$.

This energy transfer scheme has two drawbacks:

(a) It requires precise synchronization of the switches,

(b) The polarity of the output voltage V_{buffer} is reversed with regards to V_{res}. This is problematic for some applications and would require an extra regulation step.

In section 3.2.3 Buck DC-DC converters are presented as Load Interfaces that overcome the drawbacks (a) and (b) for Buck-Boost converters. Later in section 3.6 a method is introduce to overcome drawback (c) using multiple of energy-shot transfer.

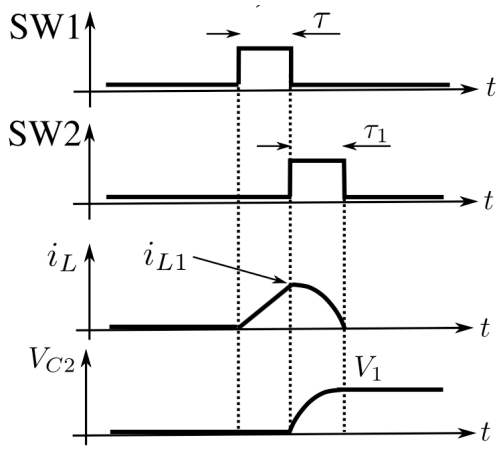


Figure 3.3: Buck-Boost DC-DC Load interface

3.2.3 Buck DC-DC Load Interface

This section presents the operation of the Buck DC-DC converter as an interface between two capacitors. First, the operation of Buck DC-Dc converters is introduced. Later a justification for using Buck DC-DC converters over Buck-Boost converters in the context of e-VEH is presented.

Buck DC-DC converter is composed on the same components as the Boost converter, but in a slightly different topology, cf. Figure 3.2c (the diode playing the role of the second switch). The Buck converter operates in two phases:

– *Phase I - SW_{LI} On*: The reservoir C_{res} is connected to the buffer capacitor C_{buffer} through the inductor L_{LI} initiating energy transfer from C_{res} to the network $C_{\text{buffer}}L$. For that to be possible, it is required $V_{res} > V_{\text{buffer}}$. During this transfer, the diode $D1$ is reverse biased and is off. As charges flow through L_{LI} an electromagnetic energy gradually builds up and by the end of Phase I, and the energy removed from C_{res} is partly transformed into electromagnetic energy of the inductor and partly transferred to C_{buffer}. Assuming that initially C_{res} and C_{buffer} are charged with voltages V_{res0} and V_{buffer0} respectively, the electrical dynamic quantities of the circuit can be found from the equation:

$$\begin{cases} \frac{Q_{res}(t)}{C_{res}} - \frac{Q_{\text{buffer}}(t)}{C_{\text{buffer}}} - Li'_L(t) = 0 \\ Q_{res}(t) + Q_{\text{buffer}}(t) = Q_0 \\ i_L = Q'_{\text{buffer}} \end{cases} \tag{3.5}$$

where, $Q_{res}(t)$ and $Q_{\text{buffer}}(t)$ are the charge-time functions of the reservoir and buffer capacitors respectively. By defining the governing equations (see Appendix I), the inductor current i_L is as follows,

$$i_L(t) = \sqrt{\frac{C_{eq}}{L}}(V_{res_0} - V_{buffer_0})sin(\omega t) \tag{3.6}$$

If in this equation t is substituted by τ, the ON time of the first switch, the last equation gives the current in the inductor at the end of the process. Obviously, the maximum useful value for this parameter is $T/4$, where T is the oscillation period of the circuit composed from L and series connection of C_{res} and C_{buffer}.

In the context of using Buck DC-DC converters as LI, it is convenient to analyse the LI in terms of the energies of the components.

It should be noted that most of the energy extracted from C_{res} in Phase I is transformed into the inductor and only small part ends up on C_{buffer}. If C_{buffer} is chosen such that $C_{\text{buffer}} \gg C_{res}$, the energy accumulated on C_{buffer} can be neglected.

The energy extracted from C_{res} in Phase I can be expressed as,

$$\Delta U_{res} = \frac{1}{2}C_{res}\left(V_{res_0}^2 - \left(\frac{(V_{res_0} - V_{\text{buff}_0})cos(\omega\tau) + V_{\text{buffer}_0} + V_{res_0}\dfrac{C_{res}}{C_{\text{buffer}}}}{C_{res} + C_{\text{buffer}}} \cdot C_{\text{buffer}}\right)^2\right) \tag{3.7}$$

A part of this energy is stored in the inductor:

$$U_L = \frac{(V_{res_0} - V_{\text{buffer}_0})^2}{2}\frac{C_{\text{buffer}}C_{res}}{C_{res} + C_{\text{buffer}}}sin^2\omega\tau \tag{3.8}$$

If $C_{\text{buffer}} \gg C_{\text{res}}$, the expressions (3.7) and (3.8) can be simplified:

$$\Delta U_{res} = \frac{1}{2}C_{res}\left[V_{res_0}^2 - [(V_{res_0} - V_{\text{buffer}_0})cos(\omega\tau) + V_{\text{buffer}_0}]^2\right] \tag{3.9}$$

and

$$U_L = \frac{(V_{res_0} - V_{\text{buffer}_0})^2}{2} \cdot C_{res}sin^2\omega\tau \tag{3.10}$$

At the end of the phase 1, the inductor current is maximum. Its value is a key design parameter, since it defines the sizing of the active circuits. The calculated energy U_L is directly linked with the inductor current through the formula $U_L = LI_L^2/2$, so that the current is proportional to the square of $sin\omega\tau$. If $\tau \ll T$, the maximum current of the inductor is simply proportional to τ, and so can be easily controlled.

– *Phase II - SW_{LI} Off*: The reservoir C_{res} is disconnected from C_{buffer} and energy extraction from the reservoir is stopped. However, thanks to the presence of the diode D_{LI} called a flyback diode, the inductor is now connected to C_{buffer}. Since the inductor is biased negatively (with regard to the current direction), the inductor reduces its current and transfers the energy into C_{buffer}. The duration of this process τ_1 is at

most the quarter of period of the LC_{buffer}. The precise duration depends on the ratio between the energy in the inductor and in the C_{buffer} at the beginning of the Phase II. The value of the time $\tau_1$can be calculated from the following equation:

$$sin^2\omega_1\tau_1 = \frac{LI_0^2}{LI_0^2 + C_{\text{buffer}}V_{\text{buffer}}^2} \tag{3.11}$$

At the end of this process, all energy extracted from C_{res} during the phase I is transformed into electrical energy stored in C_{buffer}. We note that the total charge of C_{res} and C_{store} is larger at end than at the beginning of the Buck transfer cycle: Indeed, during the phase II, the energy stored in the inductor was used to generate (to separate) new charges on C_{buffer}. On the contrary, the energy balance is fully respected, as far as the losses are negligible.

Justification for DC-DC Buck Converters The main advantages of the Buck DC-DC Load Interface over the Buck-Boost load interface is that, The output voltage - V_{buffer} - is in phase with the input voltage - V_{res}- thus no extra regulation step is needed. The next section discuss how the Buck converter is used in the context of e-VEHs.

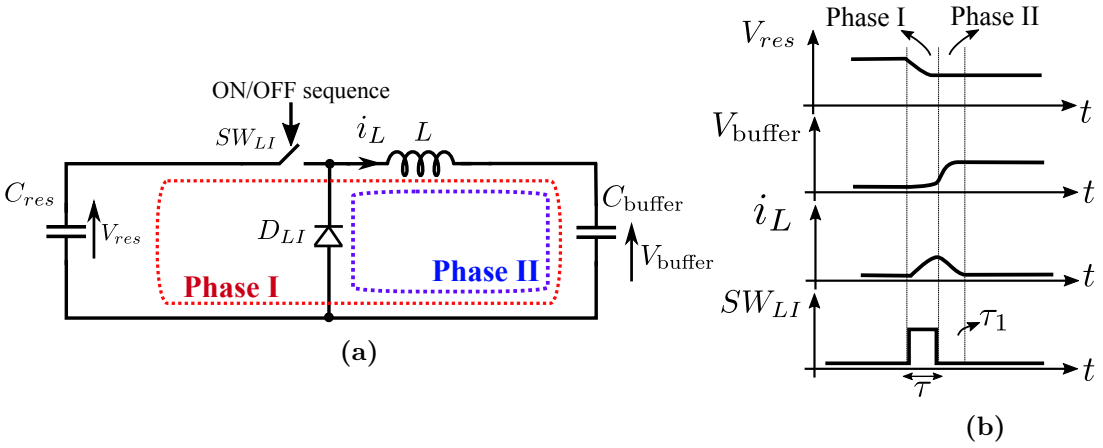


Figure 3.4: Buck converter interface (a) Buck Load schematic (b) Switch time digram

3.3 Buck Converters as Load Interface for CCs

This section present how a DC-DC Buck converter architecture fulfils the function of a load interface in a capacitive energy harvester, and to respond to the requirements given in sec. 1.10. We note that the requirement of a high efficiency energy transfer is fulfilled by the choice of the architecture, as mentioned in sec. 3.2.3. In the next two subsections we show how the requirements of regulation of the reservoir and load voltages is fulfilled.

3.3.1 Reservoir voltage regulation

A voltage regulation requires a possibility to increase or to decrease the target voltage. As explained in sec. 3.2.3, the amount of energy transferred during one cycle shown in Figure. 3.4 is controlled by the duration of the switch ON τ pulse. Since the transfer of energy toward the buffer capacitor decreases the voltage of the reservoir, the timing of the switch drive controls the rate of the reservoir voltage decrease. We note that the Buck DC-DC converter is not able to increase the reservoir voltage on its own.

The increase of the reservoir voltage is possible thanks to the energy flux coming from the harvester. This flux is not controlled; however, the overall energy flux on the reservoir capacitor is given by:

$$P_{C_{res}} = \underbrace{P_{harv}}_{\text{uncontrolled}} - \underbrace{P_{LI}}_{\text{controlled}} \tag{3.12}$$

where, $P_{C_{res}}$, P_{LI} and P_{har} are the energy fluxes on the reservoir capacitor, buffer capacitor and the harvester output respectively. In sec 3.4 control strategies to control P_{LI} - and in turn $P_{C_{res}}$ - are discussed.

3.3.2 Load Voltage Regulation

The operation of the Buck converter transfers the energy toward the buffer capacitor, and so tends to increase its voltage. The intensity of this flux is controlled by the switch timing. If the switch timing is already used for the control of the reservoir voltage, this mechanism can not be used for an arbitrary control of the buffer capacitor voltage. In this way, the buffer capacitor receives some uncontrolled incoming energy flux, which contributes to the increase of the load voltage.

A regulation of the load voltage is only possible if we introduce a controllable outgoing flux. This flux is naturally implemented by the load, which consumes energy of the buffer capacitor. However, the power of this flux is defined by the nature and the needs of the load, and is not directly controlled, neither.

The only solution for the load voltage regulation is to introduce a control of the load. In the most simple case, this control can be implemented by a load switch (SWL) - cf. 3.1 - which connect the load if the V_{load} is in the vicinity of the nominal (desired) load voltage, and disconnect it if the load voltage fall too low. This operation supposes that the energy flux consumed by the load is always superior to the incoming energy flux; in this case the average duty cycle of the SWL can fully regulate the voltage on the load resistance [21].

Different strategies of the load voltage regulation are possible. All of them are function of the load operation management and are tightly linked to the application context. In addition, since the buffer capacitance is of a low voltage, the implementation of such control is not a major technical problem (some commercial ICs address the problem of the load management, for instance, TPS22860 of Texas Instruments). For this reason, the PhD project addresses only the problem of the reservoir-to-buffer energy transfer with a side goal of the reservoir voltage control. The next section presents control strategy for Buck converter to regulate the reservoir voltage.

3.4 Reservoir Voltage regulation Strategies

In chapter one the CCs were introduced with section 1.5 highlighting the need for a load interface to regulate the reservoir voltage. This section discusses in details how this regulation is defined, then explains how this regulation can be achieved.

3.4.1 Defining V_{res} Regulation Interval

As mentioned earlier, a primary goal for the LI is to maintains the internal voltage of the harvester - in this case V_{res} - within is optimum value to maximise the rate of the harvested energy per cycle. To illustrate the harvester optimum value, we propose to consider the measurements of a series-parallel charge pump harvester's output voltage shown in Figure 3.5. The measurements shows that for every set of operation condition, their exists an optimum point of V_{opt} that maximizes the output energy flux. The only way to regulate V_{res} to a it's optimum value, is to know forehand the set of operating conditions. This however is not realistic for real-life e-VEH, where some - if not all the operating conditions - such as vibration frequency and amplitude.

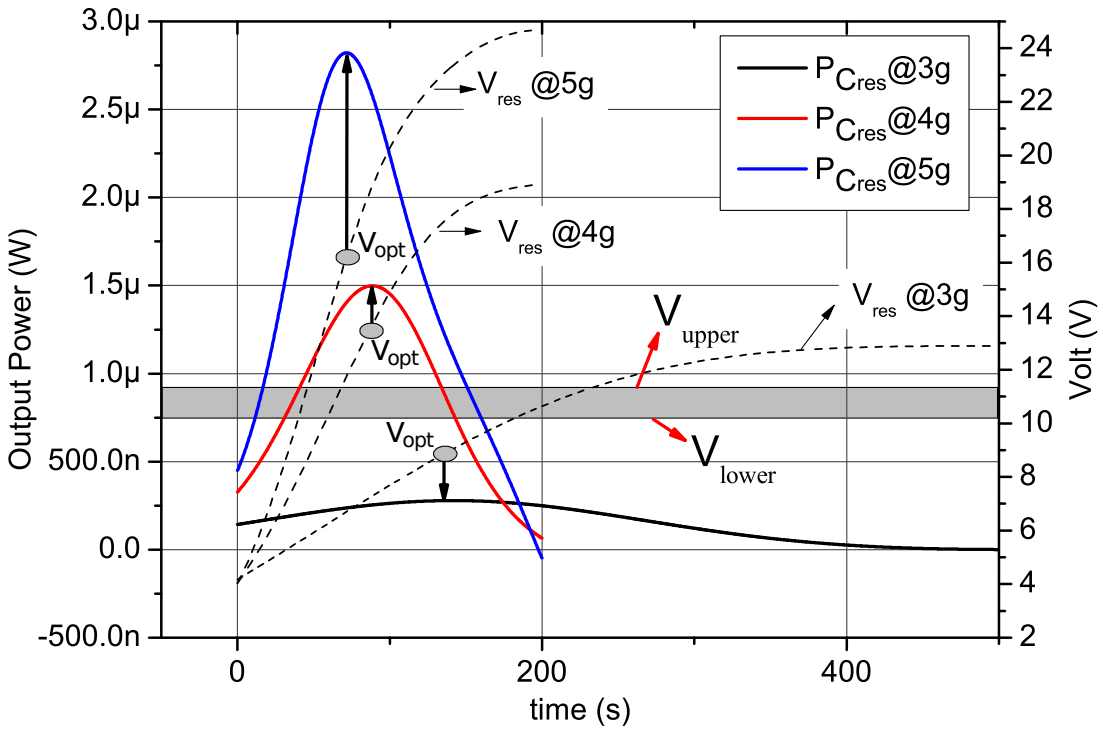


Figure 3.5: Series-Parallel Charge Pump CC measurements for V_{res} and $P_{C_{res}}$ different g with vibration frequency of 187.2 Hz, $C_{res} = 1\mu F$ and $C_{store} = 2.8nF$.

For this PhD we propose to adopt a range of permissible voltages rather than fixed value of V_{res}, cf. Figure 3.5 grey region. The permissible voltages are chosen empirically to satisfy the majority of the operating conditions. This range of permissible voltages is defined by an upper V_{upper} limit and a lower V_{lower} limit on V_{res}.

Another advantage of adopting a range of permissible voltage rather than a single operating point V_{opt} is a reduction of the frequency of the required energy transfer.

Indeed, it takes some time to the conditioning circuit to charge C_{res} from V_{lower} to V_{upper}. During this time, the load interface is idle, and only spend energy for monitoring of the evolution of V_{res}. As a consequence, such an operation is more energy saving comparing to a configuration where V_{res} would be maintained close to the optimal voltage. From this point of view, the permissible interval should be defined as large as possible. However, if the interval is too large, the system operates far from the optimal mode during long time intervals (cf. fig. 3.5). A compromise depends on the practical implementation of the system which defines the energy cost of V_{res} regulation. This will be discussed in chapter 4 when a CMOS implementation of the system will be presented.

Different strategy allows a regulation of the V_{res} voltage with use of the presented Buck interface. The most straightforward way is to use a "single shot" energy transfer: when V_{res} reaches V_{upper}, the switch SW_{LI} becomes on and the phase I of the Buck transfer cycle starts. The τ parameter is chosen exactly so to transfer to C_{buffer} the amount of energy corresponding to decrease of V_{res} to V_{lower}. After that, the LI interface stays idle till V_{res} crosses the upper threshold again. In next subsection more detail will be given about possible strategies of regulation of V_{res}. Such an operation ensures that the voltage on V_{res} is always within the predefined region (V_{lower}, V_{upper} by regularly extracting the energy from C_{res} and by transferring in onto C_{buffer}, cf. Figure 3.6.

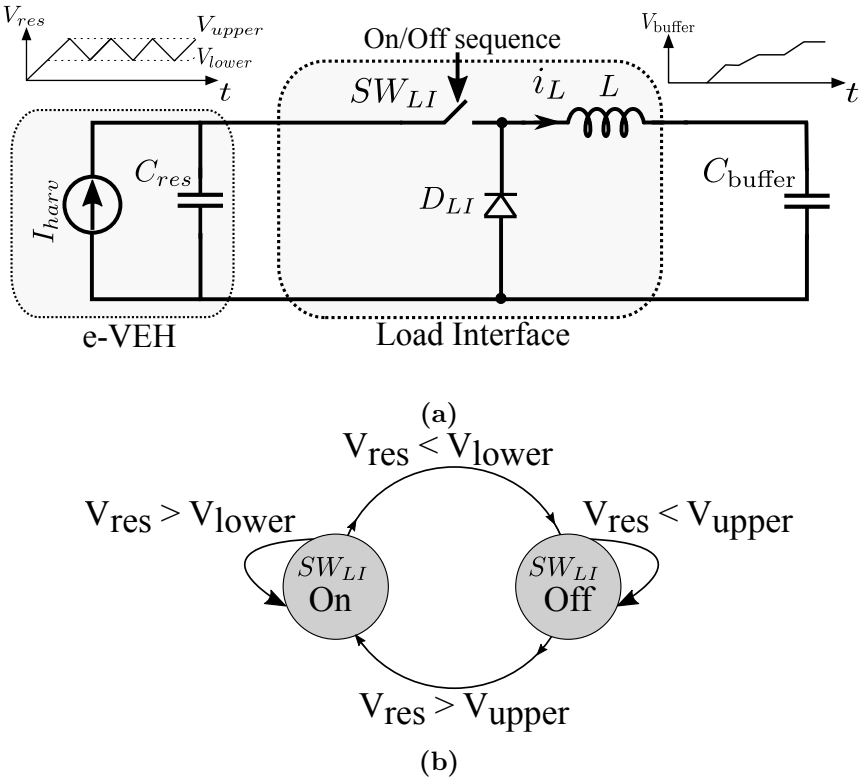


Figure 3.6: Buck Converter as LI of CCs (a) V_{res} regulation (b) state-machine diagram

3.4.2 Load Interface Control

To achieve the regulation goal for V_{res}, switching commands has to be generated to control the LI switch SW_{LI}. This control commands can be time-controlled, voltage controlled or a mix of the two controls. Here we discuss these options.

Time Control (TC): The switching commands is achieved through on/off pulse sequence where the command signal duty cycle and the frequency is fixed. The on τ and off τ_1 times are predefined and fixed so to ensure the V_{res} variation in the predefined interval, cf. Figure 3.7a. Such an open-loop operation can only be valid when the harvester operates under periodic vibrating source with known and relatively stable parameters. Since this is seldom the case in practice, a regulation feedback should be introduced.

Voltage Control (VC): The SW_{LI} switching commands rely on measuring V_{res}, cf 3.7b. In this control scheme two comparators are needed to compare V_{upper} and V_{lower} with the V_{res}. Moreover SW_{LI} switching commands has take into account the previous state of the switch. If the current state of the switch is not know before generating the next switching command, the SW_{LI} can end up latching to one of the its states. As a consequence, the switch SW_{LI} state is controlled by a finite state automaton presented in Figure 3.6b. A presence of a feedback on the value of V_{res} guarantees a robust operation of the system.

Discrete-Time Voltage Control (DTVC) is a variant of the voltage control. In this control strategy V_{res} used to control the finite state automaton in Figure 3.6b is sampled in time. A clock is used to synchronise the sampling process and to activate the comparators detecting events for the automaton operation. The sampling allows to reduce the energy consumption of the regulation circuit, since the measurement, comparison and decision taking will be achieved at discrete time, and not continuously. For this reason DTVC were adopt for this PhD project.

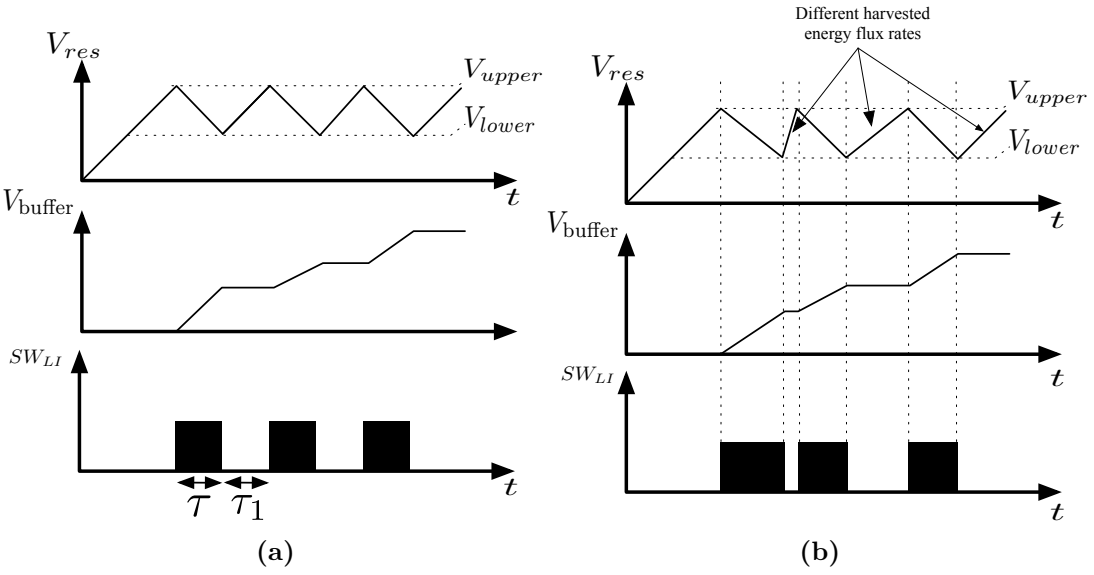


Figure 3.7: LI control strategies (a) Time control scheme (b) Voltage control scheme

3.5 DTVC Control

This section describes how the DTVC is implemented to fulfil V_{res} regulation goals, see section 3.4. It discuss V_{res} regulation phases, the requirements of the sampling clock and introduces hysteresis comparators to generate switching commands of SW_{LI}.

The DTVC control is composed of a sampling circuit followed by a comparator, cf. Figure 3.8. These blocks are described in the rest of this section. However, it is convenient to first define V_{res} operating phases as it gives better insight of the LI operation.

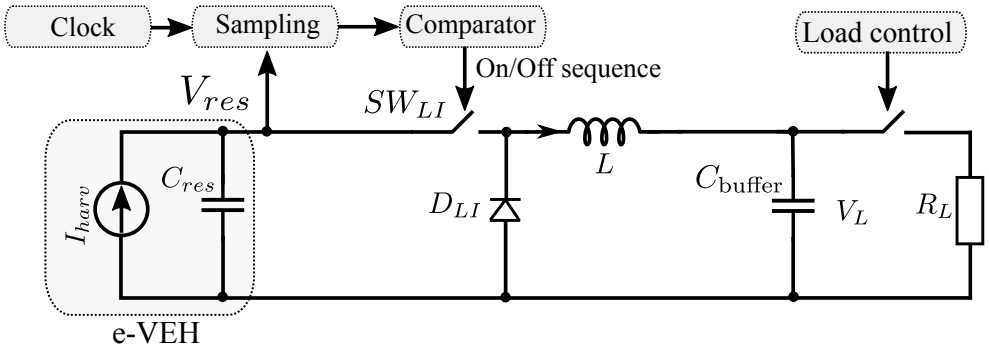


Figure 3.8: Discrete Time Voltage Control model

3.5.1 Reservoir Voltage Regulation Operating Phases

Consider the model shown in Figure 3.8. The current source I_{harv} models a series-parallel charge pump CC. The model uses the following parameters: – The reservoir capacitor $C_{res} = 100$nF is initially charged to $V_{in_0} = 5$V.

– The buffer capacitor C_{buffer} is initial discharged.

– LI inductor $L = 10$mH with winding resistance $L_{R_{LI}} = 42\Omega$

– An ideal diode mode D_{LI} and switches SW_{LI} and SW_L.

– The SW_{LI} switch thresholds are $V_{upper} = 16$V and $V_{lower} = 13$V.

– The SW_{load} switch thresholds are 1V and 1.1V.

– $I_{harv} = 0.2\mu$A supplying C_{res} with constant charge accounting for 3μW average harvested energy flux.

The model simulation shows that energy accumulation on C_{res} initially takes 5.5 seconds, while its voltage rises from 5 V to V_{upper}. After that the first energy extraction - which lasts for 460μs - V_{res} regulation repeats every 1.5 seconds as can be seen in Figure 3.9. Three distinct phases of the e-VEH from V_{res} and V_{buffer} regulation point of view can be identified:

– Conditioning circuit setup : the conditioning circuit accumulate its internal energy so to reach the optimal mode of the energy harvesting. The voltage V_{res} increases but there is no transfer of the energy to the load.

– Buffer setup: output (load) buffer accumulates energy in order to reach a nominal voltage of the buffer.

– Steady State operation: the energy is converted and is transferred to the load a nominal rate.

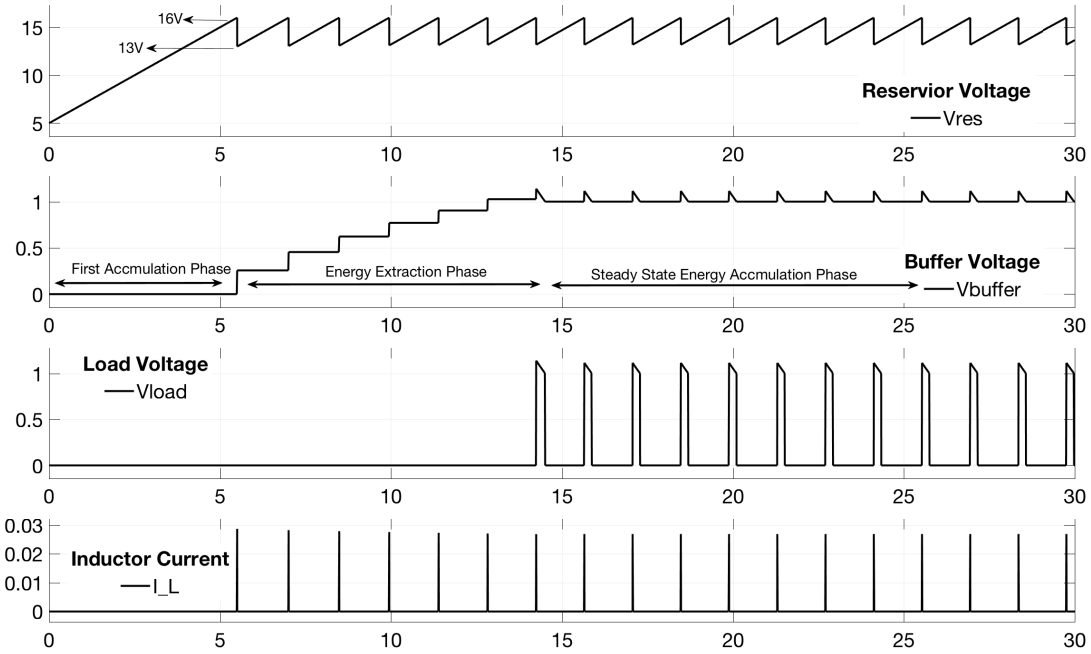


Figure 3.9: Discrete Time Voltage Control Simulink model

3.5.2 DTVC Sampling Clock

The discrete time operation of the voltage regulator requires a clock. The clock frequency is a critical design parameter for as it defines the voltage regulation resolution and the power consumption. A high frequency sampling will results in accurate switching in contrast to a low frequency sampling, but it results in a higher energy cost.

It happens that the operation of the circuit has two processes having different rates. When the switch SW_{LI} is on during the time τ, the voltage V_{res} reduces by 2 V. Although τ is not known a priori, we can consider its upper bound $T/4 = \pi/2\sqrt{(LC_{res}C_{\text{buffer}}/(C_{res} + C_{\text{buffer}})}$ equal to 160 μs. Hence, if 5% of the precision is required, the time resolution of the sampling must be 0.05τ which yields 8 μs for the sampling time (a 125 kHz clock frequency).

However, when the capacitor C_{res} increases it voltage because of the energy harvesting process (e.g., with a current $I_{harv} = 0.2\mu A$ as in the previous example), 10 seconds is necessary to increase its voltage from 6 to 8 V, and if 5% of precision is required in the V_{res} definition, it is enough to have a 0.5s for the sampling period.

For this reason, practical implementation of the circuit will require two clocks: a low frequency one for monitoring of the slow rising of V_{res}, and a high frequency one for monitoring the energy extraction process during the phase I of the Buck converter.

3.5.3 Conduction losses

In the study case shown in section 3.5.2, it can be seen that the inductor current I_L reaches up to tens of mA - cf. Figure 3.9. This value is reached at the end of the time interval τ (the phase I of the Buck converter operation). The current of the inductor is

given by the calculations presented in sec. 3.2.3. It can be seen that the value of this current increases with the square root of C_{res}. Indeed, a part of the energy extracted from C_{res} is temporary stored in the magnetic field of the inductor, and it is clear that the corresponding current increases with this capacitance.

A high current in the inductor may have significant impact on energy transfer efficiency. Not only the switching losses increase, the technology of which the switch is implemented sets a fundamental upper limit on the allowed inductor current ($I_{L_{max}}$).

Loss power - resulting from ohmic losses in the power switches SW_{LI} and the the inductor L - can be defined as [73]. The energy cost of one Buck converter transfer cycle due to the conductive loss is given by:

$$P_{cond} = \int\limits_{\text{Phases I and II}} I_L^2(t) R_{LI} \mathrm{d}t \tag{3.13}$$

where I_L is the instantaneous current through the inductor and R_{LI}, and the resistance R_{LI} accounts for the winding resistance of the inductor as well as for the switch on resistance. It can be seen that the power loss is proportional to square the current. Moreover, if the current is high, the size of the transistor must be increased. In turn, it will increase the capacitance of the switch, and will require a higher energy for the switch driving.

Thus, in an effort to lower these losses it is more adequate to reduce the current I_L. One method to achieve that goal is to introduce multiple energy-shot transfer. The idea is to transfer the energy ΔU_{res} which correspond to lowering of C_{res} voltage from V_{upper} to V_{lower} not in one single Buck cycle, but in several cycles (shots). Since the energy transferred at each shot is lower than when a single-shot transfer was used, the maximum current is lower. This concept is explained in details in the next section 3.6.

3.6 Multiple Energy-shot transfer

This section presents what we call "Multiple energy-shot transfer" strategy, consisting in transferring a desirable amount of energy from C_{res} to C_{buffer} within Each single energy-shot transfer is done exactly as a the Buck converter transfer cycle described in sec. 3.2.3, as a two phase process:

Phase I: In this phase, the switch SW_{LI} is turned on, for a time t_{on}, chosen so that the inductor current does not exceed some predefined current $I_{L_{max}}$. This allows a part of the energy δU to be removed from C_{res}. If the current I_{max} is fixed, the time t_{on} is given by the following equation:

$$t_{on} = \frac{1}{\omega} \sin^{-1}\left[\frac{I_{L_{max}}}{V_{res_0} - V_{\text{buffer}_0}} \sqrt{\frac{L}{C_{eq}}} \right] \tag{3.14}$$

where, $\omega = \sqrt{1/LC_{eq}}$, C_{eq} is the equivalent series capacitance of C_{res} and C_{buffer}, V_{res_0} and V_{buffer_0} are the initial voltage at $t = 0$. The link between t_{on} and the extracted energy δU is given by eq. (3.7), where τ should be substituted by t_{on} and ΔU_{res} by δU.

Equation (3.14) provides an upper bound of t_{on} which guarantees that, under given initial voltages on the capacitors, the inductor current doesn't exceed I_{max}. This upper

bound depends as well on $V_{res_0} - V_{\text{buffer}_0}$. So, the absolute upper bound of t_{on} is given by:

$$t_{on_{max}} = \frac{1}{\omega}\sin^{-1}\left[\frac{I_{L_{max}}}{V_{res_{0\ max}}}\sqrt{\frac{L}{C_{eq}}}\right] \tag{3.15}$$

i.e., when V_{res_0} has a maximum value, and V_{buffer_0} is zero.

We note that for a given $I_{L_{max}}$, t_{on} .

Second Phase: This phase begins when SW_{LI} is turned off, and lasts for a time t_{off}. This allows the energy accumulated on the inductor to be fully transferred to the load capacitor. The maximum time guarantying full energy transfer t_{off} is defined as,

$$t_{off} = \frac{\pi}{2}\sqrt{LC_{\text{buffer}}} \tag{3.16}$$

These two phases of energy transfer process is repeated until ΔU is extracted from C_{res}. Both of t_{on} and t_{off} are chosen to be fixed and equal time needed to the energy-shot transfer when $V_{\text{buffer}} = 0$, since this is the only transfer where $I_{L_{max}}$ is reached. The V_{res}, V_{buffer} and i_L evolution in a multiple energy-shot transfer are illustrated in Figure 3.10.

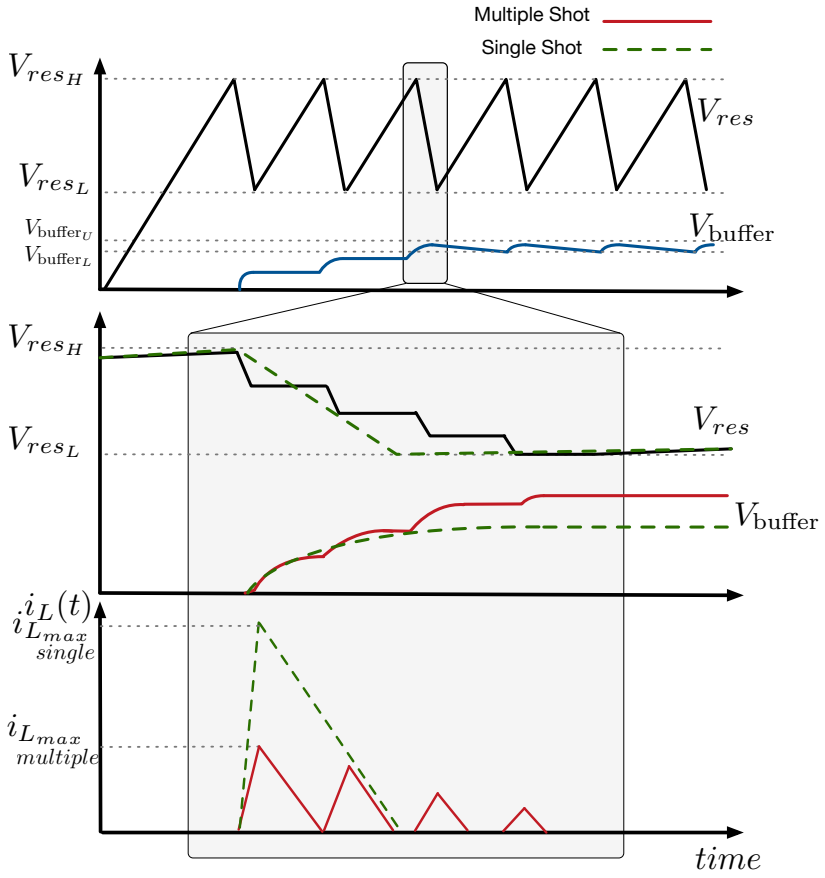


Figure 3.10: Reservoir voltage $V_{res}(t)$, buffer voltage $V_{\text{buffer}}(t)$ and inductor current $i_L(t)$ illustration of multiple energy-shot transfer (solid line) single shot transfer (dashed-line)

3.7 Load Interface Behavioural Model

To show the multiple energy-shot transfer in action, a mixed Spice/behavioural model is introduced for the LI, as shown in Figure 3.11. The switching decisions are implemented by a hysteresis comparator modeled with a Spice macromodel. A current source mimics the influx of a harvested energy as a constant charge intake on capacitor C_{res} whose voltage has a constant is maintained within the predefined limits V_{lower} and V_{upper}. The model is simulated with the ADMS tool of Mentor Graphics with the results shown in Figure 3.12.

This results shows a practical case illustrating the advantage of using the multiple energy shot transfer over a conventional single shot transfer. If an optimum V_{res} interval is defined by $10V < V_{res} < 20V$, and given that $C_{res} = 1\mu F$, $C_{load} = 20\mu F$ and $L = 15mH$, the energy to be extracted so to drop V_{res} from V_{res_H} to V_{res_L} is $150\mu J$.

Assuming initially the buffer is at $V_{\text{buffer}} = 3.3V$, with a single-shot transfer, the inductor current can reach up to $120mA$, according to Eq. 3.6. However, if for some reasons the current must be limited to $15mA$, this constraint can be satisfied with the multiple-energy shot operation: as shows the simulation in fig. 3.12b, the energy is transferred with 6 cycles (shots) and the current I_L never overpass $15mA$.

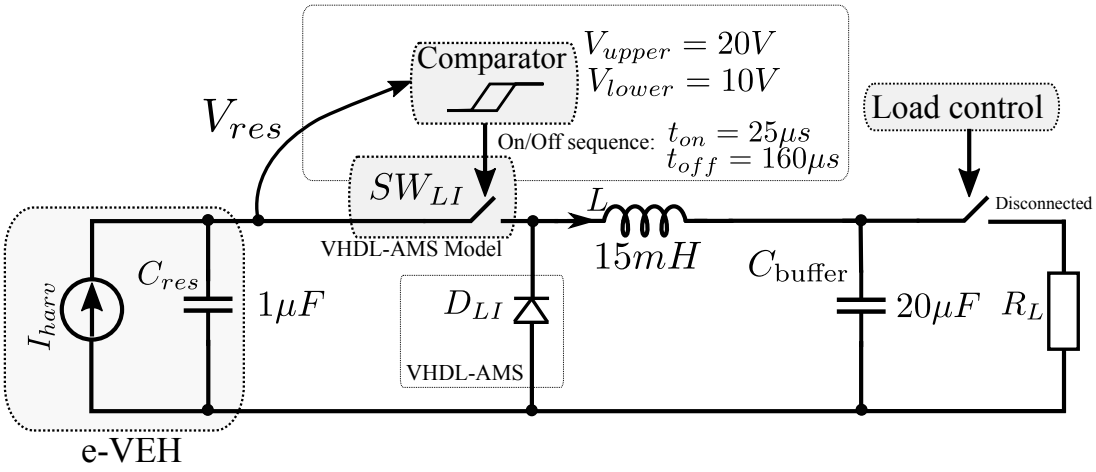


Figure 3.11: Multiple Energy-Shot transfer LI VHDL-AMS model

3.8 Strategy of CMOS implementation

In the next two chapters, a CMOS implementation is proposed for the LI adopting the multiple energy-shot transfer mechanism. First an appropriate cmos technology is chosen to implement the LI controller. Second to be able to achieve a complete e-VEH system we shifted our attention towards implementing a multiple energy-shot controller. For this first implementation an external voltage source was assumed to be available to supply the LI controller. Moreover, the load voltage regulation was postponed for the next stage. After the compilation of the first implementation, power

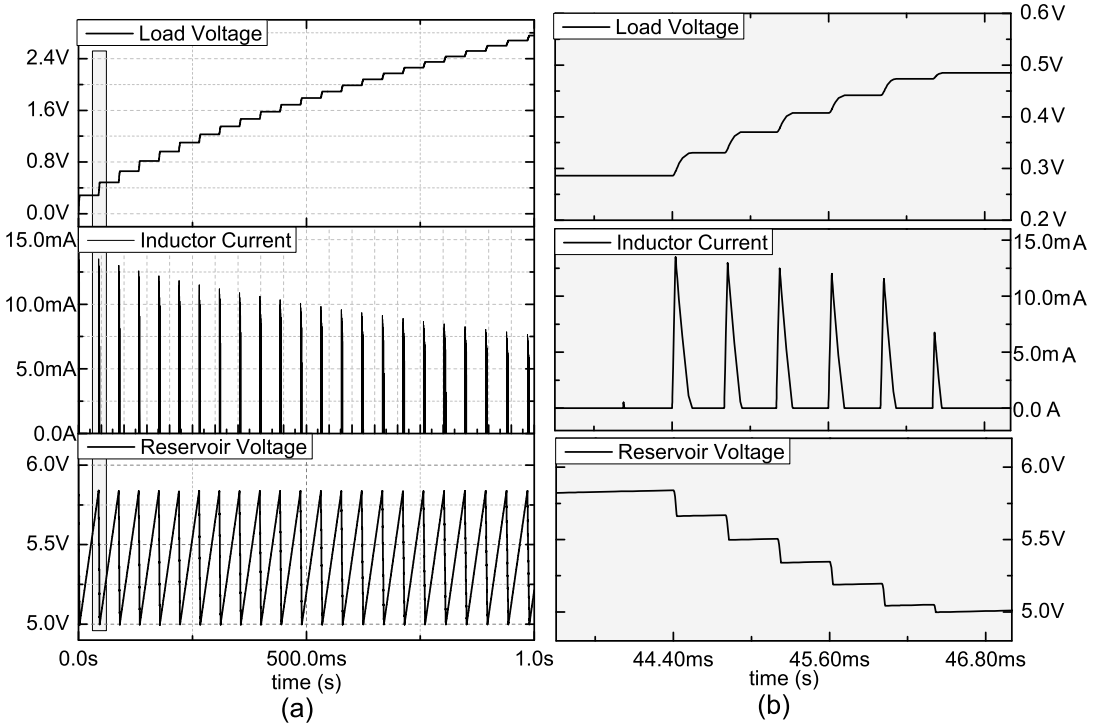


Figure 3.12: VHDL-AMS model of multiple shot energy transfer showing inductor current $i_L(t)$, reservoir $V_{res}(t)$ and load $V_{load}(t)$ voltages with design parameters $L = 10mH$, $C_{res} = 1\mu F$, $C_{load} = 20\mu F$, $V_{res_H} = 6V$, $V_{res_L} = 5V$, $I_{harv} = 2mA$, $I_{L_{max}} = 15mA$, $t_{on} = 25\mu s$ and $t_{off} = 160\mu s$ where (a) $0s < t < 1s$ and (b) $44ms < t < 47ms$.

consumption assessment was overtaken to analyse each block of the loads interface controller. This design is presented in Chapter 4.

With the main energy consuming blocks identified we shifted our attention towards implementing self powered load interface. In this second implementation we included the load voltage regulation block and targeted a self-power LI controller. This design is presented in Chapter 5.

3.9 Summary

This chapter presented DC/DC buck converters as load interfaces for e-VEH. We showed how hysteresis comparator can be used to generate the proper switching commands for the LI and shred light on the need for two switching modes - idle and switching modes - for the to operate. Moreover, multiple energy-shot transfer was introduced to as an intuitive method improve the LI transfer efficiency and to keep the LI current within the technology limits. In the two following chapters, two CMOS implementations of the multiple energy-shot transfer strategy will be proposed.

Chapter 4

First Implementation of Load Interface System

Contents

4.1 Overview

This chapter presents a first implementation of the load interface (LI) for vibrational energy harvesters. As introduced earlier in pervious chapters, the goal is to implement a load interface that acts as an intermediate stage between the CC and the load. This load interface maintains a maximised harvested energy rate and uses a dc-dc buck converter to supply a low voltage buffer capacitor, which in turns periodically supply a load.

The first architecture developed in the PhD project accomplishes the goal of maximising the harvested energy and achieves the multiple energy-shot transfer, by implementing the architecture of Figure 3.8.

This implementation of the Load Interface LI we present here addresses the reservoir voltage V_{res} regulation. The V_{res} regulator system-level approach discussed in Chapter 3 is broken down to sub-block. Each block works in coordination with the other to generate the switching commands of the LI switch, with the global goals mentioned in Chapter 1 as key motivation behind this *first implementation*. Later in the Chapter 5, more goals are added to the list including optimising the power consumption and addressing the regulation of the load voltage.

This chapter is organised as follows: First the CMOS technology used is presented, then the LI design parameters are discussed. Afterwards, the LI control blocks are designed in transistor level. Finally we conclude with a complete transistor-level simulation of the system.

4.2 AMS 0.35μm CMOS Technology

In this PhD project, the technology used to implement Load Interface Controller in transistor-level is H35 of AMS, which is a 0.35μm CMOS technology providing high voltage devices. It is a technology optimized for complex analog and mixed signal circuits operating with voltages up to 120V. The H35 technology has two poly-silicon layers and four metal layers, cf Figure 4.1. It provides a variety of high voltage transistors as well as standard low voltage transistors, as in the standard low voltage technology C35. It is a mature technology that comes with a design kit (Hitkit) reliable enough for "first time right" designs.

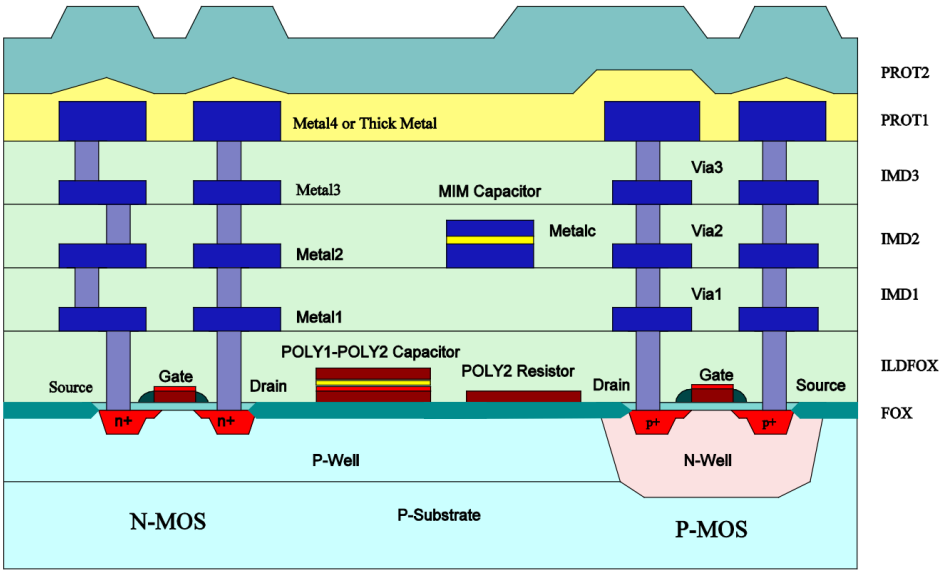


Figure 4.1: Cross section view of the AMS-0.35μm technology [74]

Table 4.1: CMOS 0.35μm H35B4D3 technology specifications

Technology	**0.35μm H35B4D3**
Number of Masks	27
Substrate Type	p-type
Maximum Die Size	$2cm \cdot 2cm$
Poly layers	2 High Resistive Poly
Metal layers	4 Thick Metal
Metal Type	Aluminum
POLY1/POLY2 Current Density	0.34/0.2 mA/mum
High Resistive Poly Current Density	0.07 mA/μm
Metal (MET1,2,3) Current Density	0.67 mA/mum
Thick Top Metal Current Density.	3.35 mA/mum
Capacitor Types	MOS, PIP
Gate Oxide Capacitance	4.54 fF/mum^2
V_{th} of 3.3V NMOS/PMOS	Typical $+0.59V/-0.72V$
Core Cells	300 Standard Digital Cells
Periphery Cells	A/D LV, HV and Floating LV
Supply Voltage	3.3V, 5V, 20V, 50V, 120V
Temperature Range	From$-40C/+125C$
Special Features	High Performance Analog/Digital/HV Process

This technology is appropriate for sensors and energy harvesting applications due to its reliability and low power consumption thanks to its low leakages transistors. It is a perfect choice for the load interface control we propose as it provides the required high and low voltage transistors, as well as MIM capacitors). The core transistors provided within ams 0.35μm technology is based on thin-gate oxide 3.3V transistors with a minimum channel length L of 0.35μm. Moreover the process family includes a 5V and 20V gate options with a mid-oxide and thick oxide gates for both transistors. The high voltage transistors have several limitations that can severely affect the analog design such as they require a longer channel length L which results in higher ON channel resistance R_{ON} and higher gate charge Q_G. The consequence is a higher power dissipation because of significant conduction and switching losses. This must be taken into account for a refined final design. Another important element in energy harvesting applications is on chip capacitors. These can be achieved by the two available polysilicon layers (Poly1 and Poly2). They are layouted as Poly1-Insulator- Poly2 (PIP) capacitor or CPOLY capacitor which occupy less area then MOS capacitor of the same capacitance value, yet they suffer from higher resistive losses. A summary of the technology parameters are shown in Table 4.1 and Table 4.2.

4.3 First implementation of Load Interface

In this first implementation of the load interface only the reservoir voltage regulator is considered. The capacitors (C_{res} & C_{buffer}), inductor and the diode are discrete

Table 4.2: High voltage transistor parameters of AMS H35B4D3

Paramater	**NMOS50T**	**PMOS50T**
Oxide thickness T_{ox} $[m]$	$7.575 \cdot 10^{-9}$	$7.66 \cdot 10^{-9}$
Oxide capacitance C_{ox} $[F/m^2]$	$4.555 \cdot 10^{-3}$	$4.506 \cdot 10^{-3}$
Electron mobility μ $[m^2/V \cdot s]$	0.039	0.0128
V_{th} [V]	0.47	0.63
$V_{gs,max}$ [V]	3.3	3.3

components, cf. Figure 4.2. It must be notice that the reservoir capacitor C_{res} is a part of the harvester's CC and for the LI design perspective it is predefined by the CC. The C_{buffer} is chosen 20 times larger to serve as the buffer and eventually as the power supply for the LI. The first LI implementation has the parameters summarised in Table 4.3.

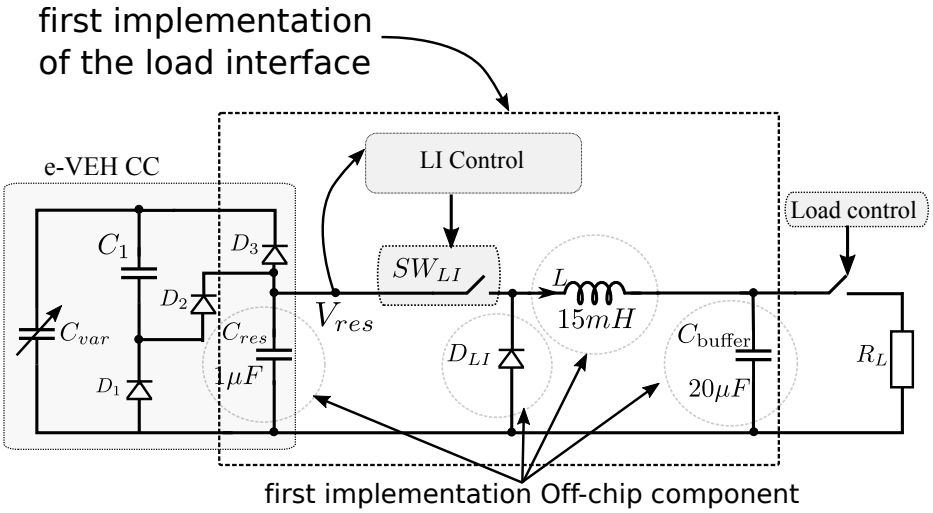


Figure 4.2: Load Interface showing off chip blocks

Table 4.3: Design parameters of the load interface first implementation

Element	Value	Note
C_{res}	$1\mu F$	harvester capacitor
$V_{res_{opt}}$	$5V < V_{res_{opt}} < 6$V	optimum interval
C_{buffer}	$20\mu F$	temporary buffer capacitor
$I_{L_{max}}$	$15mH$	load interface inductor
E_{harv}	$< 5\mu$ W	input energy flux
V_{DD}	3.3V	LI control supply

4.4 Structure of the implemented load interface

As explained earlier, the design presented in this section focus on implementation of the load interface achieving only the regulation of the reservoir voltage V_{res}. The designed circuit is composed of three blocks: switching decision block, clock select block and switch controllers block as shown in Figure 4.3. In this section we specify the operation of each of these three blocks.

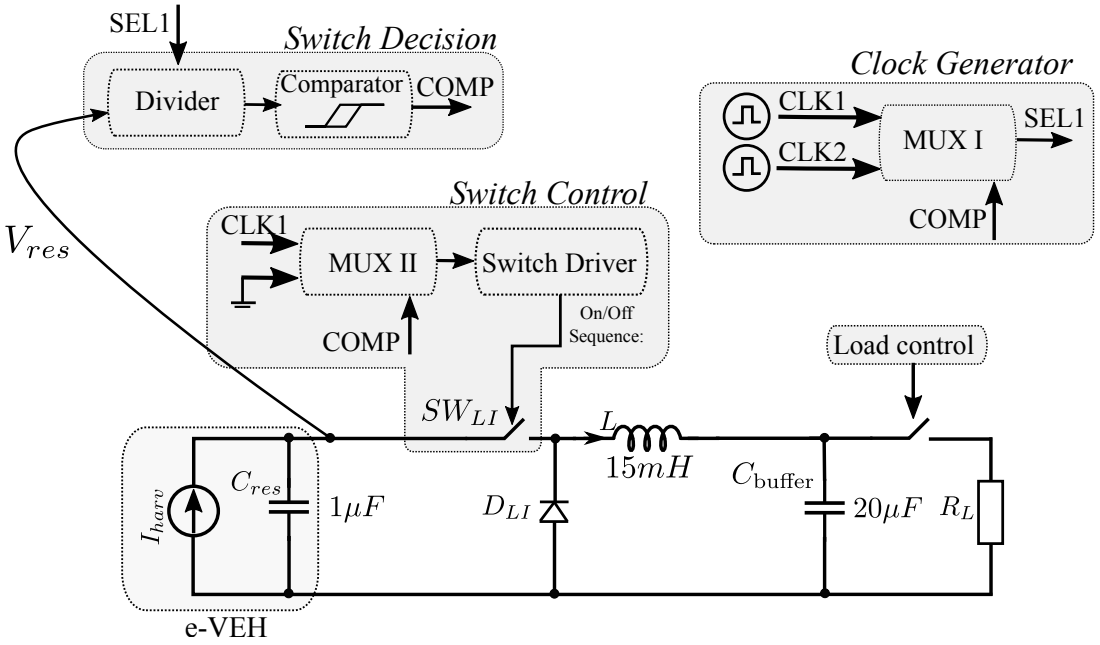


Figure 4.3: Load interface architecture implementing the V_{res} regulation

1. The Switch Decision block: The role of this block is to generate a binary signal enabling (when the output is '1') the transfer of energy from C_{res} to C_{buffer}. It is composed of a voltage divider and a hysteresis comparator.

   The switching decision is achieved in two steps:

   – First V_{res} is sampled and scaled down by a voltage divider (as V_{res} is higher than the VDD voltage of the comparator).

   – Second, the sampled downscaled version of V_{res} is introduced to a hysteresis comparator with the thresholds corresponding to the downscaled V_{res} optimal interval V_{res_H} and V_{res_L}.

   More precisely, the comparator outputs '1' when:

   - $V_{res} > V_{res_H}$,
   - $V_{res} > V_{res_L}$ and V_{res} decreases.

   The '1' level at the output of the comparator initiates the generation of the SW_{LI} control signals.

For the reasons explained in section 3.5.2, the reservoir voltage V_{res} is sampled using one of two sampling frequencies correspond to the two modes: an accumulating mode and a transfer mode, cf. Figure 4.4. The accumulating mode is when C_{res} is accumulating energy from the harvester (SW_{LI} is OFF), it correspond to a slow variation of V_{res} and hence to a low sampling frequency, while the transfer mode is when C_{res} transfers ΔW to C_{buffer} (SW_{LI} is On), it corresponds to a fast variation of V_{res} and hence to a high sampling frequency.

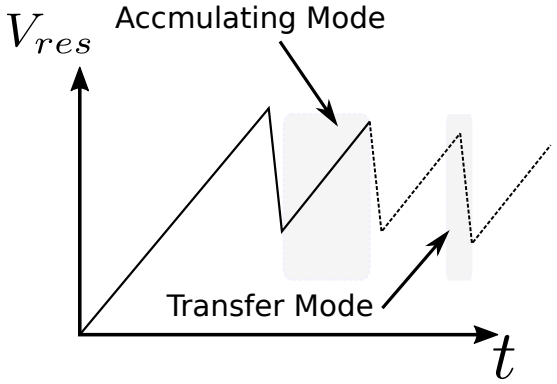


Figure 4.4: Energy Transfer Modes

2. The clock generator: is composed of a multiplexer MUXII and two clocks (a high frequency f_H clock CLK1 and a low frequency f_L clock CLK2). The output of the switch decision block (the comparator output) controls the path selection of the multiplexer. According to the mode (accumulation or transfer modes), the block generates a high frequency or a low frequency clock.

   The high frequency clock is set to frequency of $1/(t_{on} + t_{off})$, while the low frequency clock is chosen to reduce power consumption for when LI is accumulation mode. The time t_{on} is the time for a single energy shot - see section 3.6.

3. The Switch Control block: This block produces the switching signal for the switch SW_{LI}. This block is composed on the multiplexer MUXII generating the required switch state, and on the switch driver, which converts the logical switch state to physical signal required for the switch driving.

   When the COMP signal is zero (the accumulation mode), the switch must be off and the MUXII block generates zero. When the COMP signal is high (the transfer mode), the switching signal is the same as the high frequency clock (CLK1). Note that the use of CLK1 for the switching synchronises the energy transfer with the sampling of C_{res} voltage.

This architecture has previously been modeled with a behavioural model at a high abstraction level in section 3.7. The next sections present its design at transistor level in CMOS process AMSH35 technology.

4.5 Switch Decision Block

The transistor-level implementation of the Switch Decision block is shown in Figure 4.5. It is responsible for initiating the switching decision commands and is break up into two sub-circuits:

– Voltage divider.

– Hysteresis comparator.

The thresholds for V_{res} regulations were chosen to be $V_{upper} = 6V$, $V_{lower} = 4.8V$. The proposed architecture allows an adjustment of these parameters through either changing the division factor or the thresholds of the comparator if another optimum interval is targeted.

The next two subsections discuss the transistor-level implementation of these two blocks.

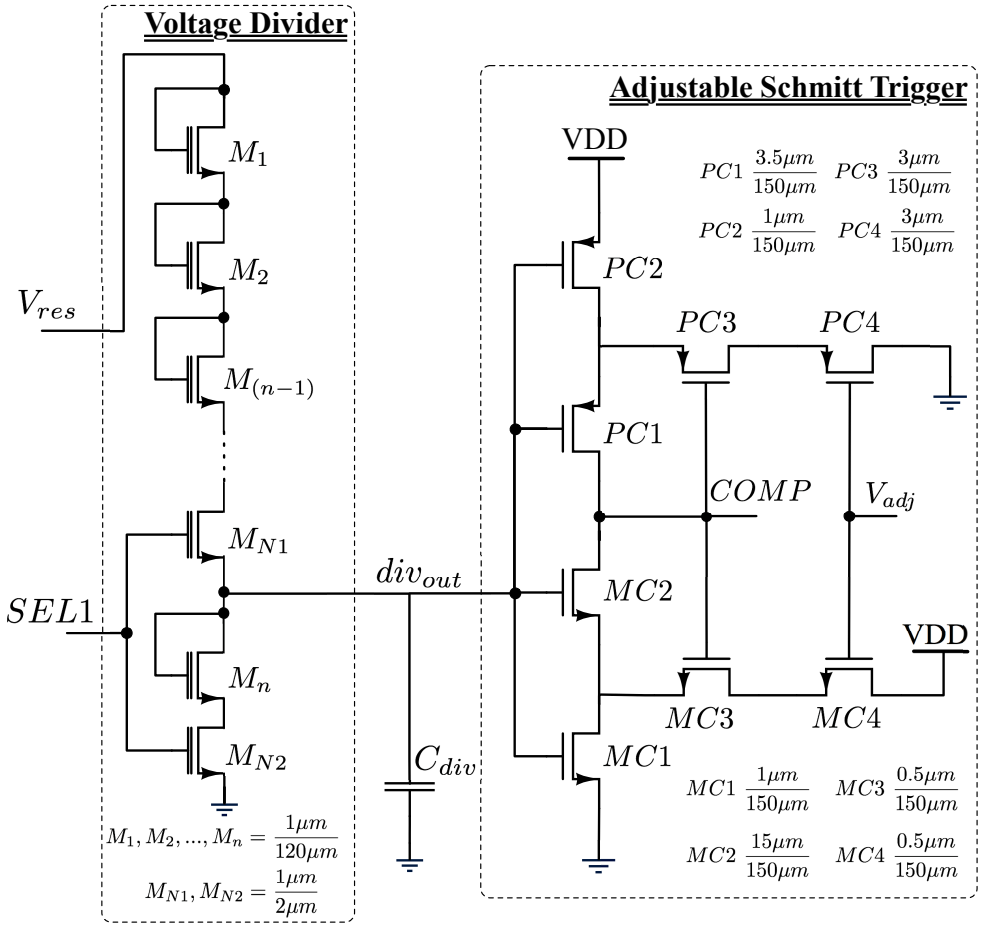


Figure 4.5: Switching Decision block showing the voltage divider and an adjustable Schmitt Trigger comparator

4.5.1 Voltage Divider

An energy efficient voltage division is achieved using MOSFET divider. It is implemented by N stages of diode-connected high-voltage NMOS transistors connected in series. The division factor is equal to N-1. To allow a sampling of V_{res}, two switching transistors M_{N1} and M_{N2} are added with an enable signal $SEL1$ (cf. fig. 4.3). The enable signal $SEL1$ is generated from the switching control block, which will be presented in section 4.7. The timing of the sampling process is defined by the clock CLK1 of the switch control block.

To design the voltage divider one must take into account the trade-off between the static and dynamic power consumption. The static power consumption is defined by leakage current of the divider when the transistors MN1 and MN2 are off. The dynamic power consumption is due to the direct current from VDD to the ground and to the charging of the capacitive load connected to the output of the divider, C_{div}. In sum the voltage divider design must find a trade-off for the following features:

– Low static power consumption: through a high off resistance R_{off} of MN1 thus minimizing the static current.

– Low dynamic power consumption: through low R_{on} for both of MN1 and MN2 thus allowing fast charging of the readout capacitance C_{div}.

With the aid of DC analysis, the minimal size of transistors MN1 and MN2 is found as shown in Figure 4.5 to provide minimal ON current through the divider. The DC analysis of the voltage dividing along with the leakage current is shown in Figure 4.6. With the division factor N set to 5, a voltage sweep of the input shows that the voltage can be divided in a linear manner by the voltage divider - up to 10V - as well as a maximum current of $2.3\mu A$.

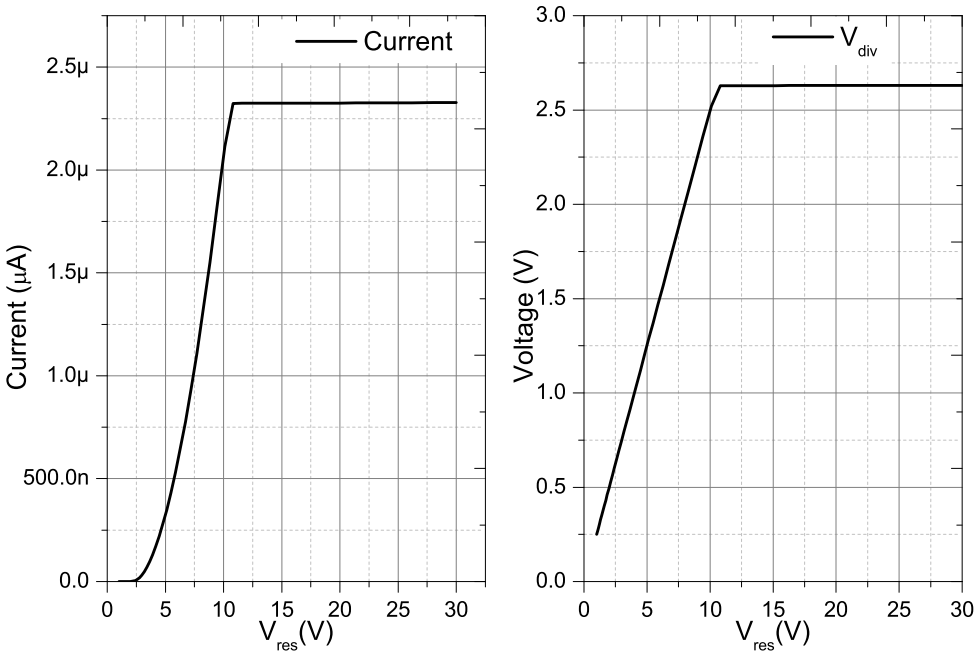


Figure 4.6: Voltage Divider Current DC analysis

4.5.2 6T Comparator overview

The comparator shown in Figure 4.7a is implemented based on [75], and is called 6T Schmitt-trigger comparator. It is composed of two symmetric circuits each defining upper V_{upper} and lower V_{lower} thresholds. The hysteresis gap is defined by sizing the transistors MC1 and MC3 for V_{lower}, as well as PC1 and PC3 for V_{upper}. The transistor sizing was concluded to the shown in Figure 4.5 setting $V_{lower} \approx 1.2V$ and $V_{upper} \approx 1.5V$ with $V_{adj} = 3.3V$, cf. Figure 4.7b. The comparator operation is described in details in the next subsection.

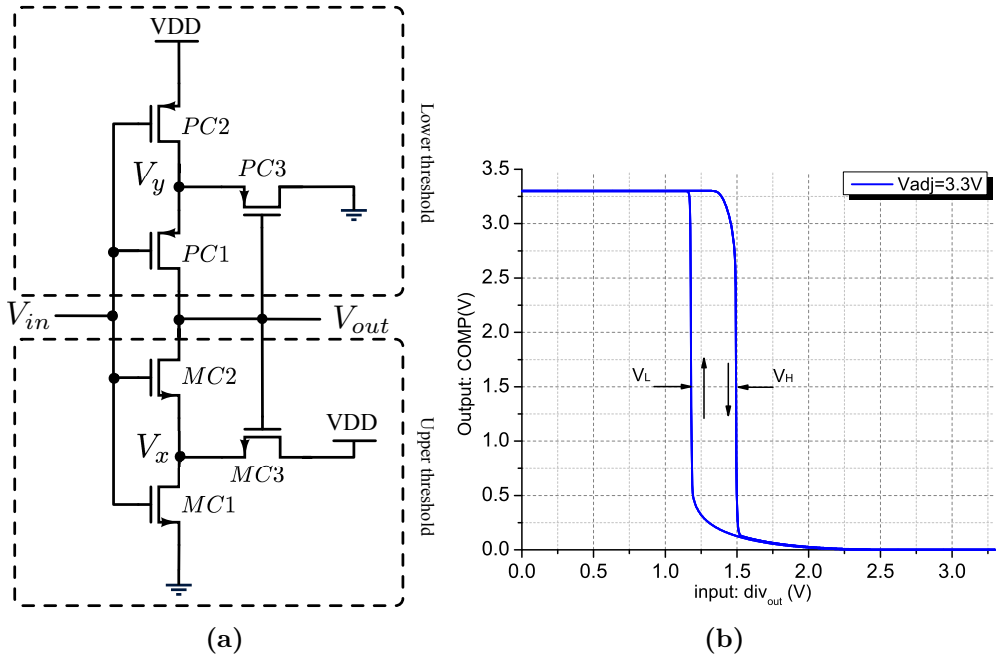


Figure 4.7: 6T Comparator (a) Schematic (b) Transfer function

4.5.3 6T Comparator Analysis

Assuming initial conditions $V_{in} = 0$, which in turns defines the output initially as $V_{out} =$ VDD. It follows that MC1, MC2 and PC3 are off, while MC3, PC1 and PC2 are on at this state. Moreover, the two PMOS transistors PC1 and PC2 at this stage provides a DC path from VDD to V_{out}.

Considering the upper threshold part of the circuit, cf. Figure 4.8, as the V_{in} starts to increase above $V_{th_{MC1}}$ MC1 begins to switch ON. This leads to V_x is gradually being pulled to the ground. However, at this stage MC3 is still OFF, since V_{out} is High (VDD), and thus try pull V_x to $VDD - V_{th_{MC3}}$. When V_{in} increases further and exceeds MC2 $V_{th_{MC2}}$, MC2 turns ON. This pulls V_{out} to ground, consequently turning MC3 OFF which in turn pulls V_x fully to ground. This voltages defines the **upper threshold of the 6T comparator** V_H.

Nevertheless, considering the upper part of the Schmitt tigger at this stage, where V_{out} is LOW, PC3 is turned ON, while PC1 and PC2 begins to turn OFF cutting the

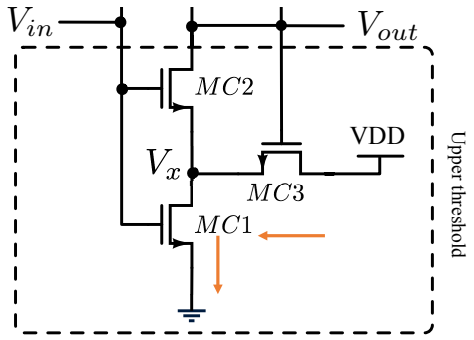


Figure 4.8: 6T comparator Upper threshold

DC path of VDD.

Considering the I_{DS} current equations when both MC1 and MC3 are ON and MC2 is OFF, the drain current $I_{D_{MC3}}$ flows into the drain current $I_{DS_{MC1}}$, thus $I_{DS_{MC1}} = I_{DS_{MC3}}$

$$\frac{\beta_{MC1}}{2}(V_{GS_{MC1}} - Vth_{MC1})^2 = \frac{\beta_{MC3}}{2}(V_{GS_{MC3}} - V_{th_{MC3}})^2 \tag{4.1}$$

which follows,

$$\beta_{MC1}(V_{in} - 0 - Vth_{MC1})^2 = \beta_{MC3}(V_{DD} - V_x - V_{th_{MC3}})^2 \tag{4.2}$$

However, as V_{in} and MC2 start to switch ON, then V_H can be defined as, cf. Figure 4.9,

$$V_H = V_x|_{V_{in}=V_H} + V_{th_2} \tag{4.3}$$

Now substituting using Equation 4.3 into Equation 4.2 and taking into account that MC2 and MC3 are tied together at the source (i.e $V_{th_{MC2}} = V_{th_{MC3}}$ and any increase in the threshold voltages of these two caused by the body effect is the same), then,

$$\frac{\beta_{MC1}}{\beta_{MC3}} = \frac{W_1 L_3}{L_1 W_3} = (\frac{V_{DD} - V_H}{V_H - V_{th_{MC1}}})^2 \tag{4.4}$$

thus,

$$V_H = \frac{V_{DD} + \alpha V_{th_{MC1}}}{1 + \alpha} \tag{4.5}$$

where

$$\alpha = \sqrt{\frac{\beta_{MC1}}{\beta_{MC3}}}$$

When the 6T comparator fully switches state, transiting from low to high, MC3 is turned OFF while MC1 and MC2 are turned ON. It is worth to mention that, at this stage PC3 is now turned on while PC1 and PC2 are turned off. Since, the high threshold voltage that switches MC2 on, is not the same voltage that would completely turn PC1 and PC2 off. *This means that at this transition of the output from High to Low, a current path from VDD to ground is created causing a current leakage.*

Similar analysis can be conducted to define the lower threshold V_L. If V_{in} is arbitrary assumed high (VDD), thus MC1, MC2 and PC3 are ON, while PC1, PC2 and

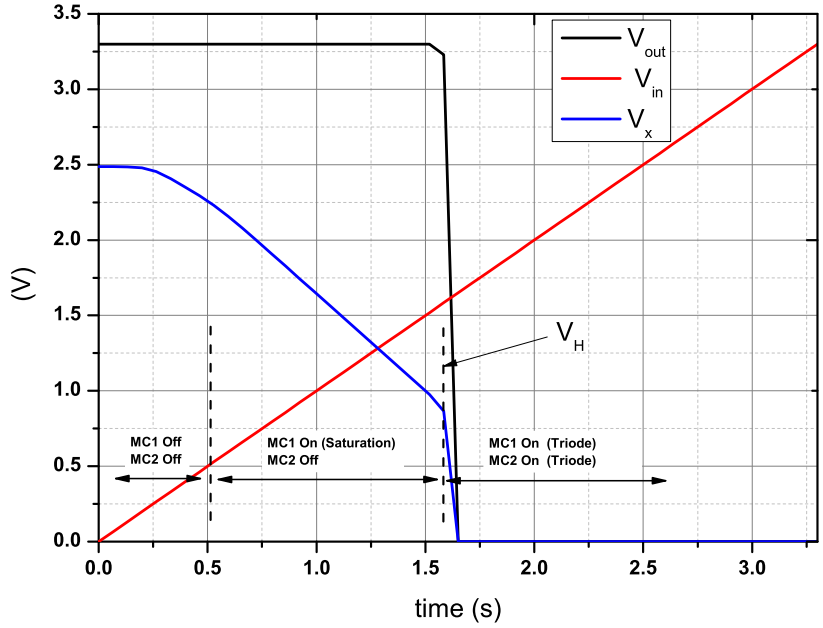


Figure 4.9: Transition of V_x with V_{in} increases

MC3 are OFF which follows that output is LOW. As the input starts to fall from VDD towards the grounds, PC2 starts to turn ON, which in turns pulls V_y up towards VDD. However, since PC3 is ON, it tries to keep V_y to ground ($\approx -V_{th_{P3}}$). As the input voltage drops further, a second threshold is reach that would switch PC1 On. Just before PC1 is turned on, only the current flow from PC2 into PC3, or $I_{DS_{PC2}} = I_{DS_{PC3}}$.

$$\frac{\beta_{PC2}}{2}(V_{SG_{PC2}} - Vth_{PC2})^2 = \frac{\beta_{PC3}}{2}(V_{SG_{PC3}} - V_{th_{PC3}})^2 \tag{4.6}$$

which in turns,

$$\frac{\beta_{PC2}}{2}(V_{DD} - V_{in} - Vth_{PC2})^2 = \frac{\beta_{PC3}}{2}(V_y - V_{th_{PC3}})^2 \tag{4.7}$$

However, the input voltage that turns PC1 ON defines the lower threshold voltage V_L,

$$V_L = V_y|_{V_{in}=V_L} + V_{th_{PC1}} \tag{4.8}$$

but since $V_{th_{PC1}} = V_{th_{PC3}}$, then

$$\frac{\beta_{P2}}{\beta_{P3}} = \frac{W_{P2}L_{P3}}{L_{P2}W_{P3}} = [\frac{V_L}{VDD - V_L - V_{th_{PC2}}}]^2 \tag{4.9}$$

Thus, the low threshold voltage can be defined as,

$$V_L = \frac{\xi}{1+\xi}(V_{DD} - V_{th_{PC2}}) \tag{4.10}$$

where,

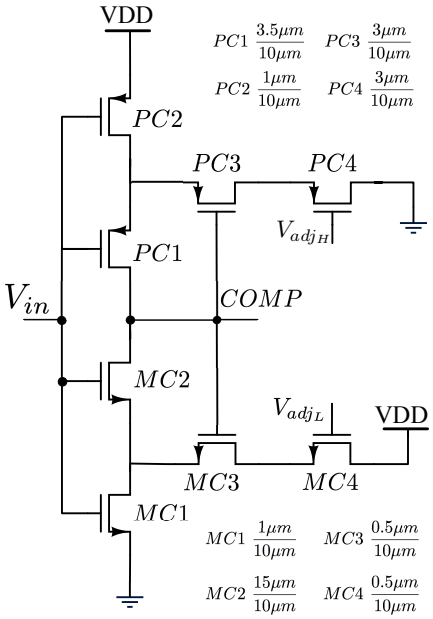
$$\xi = \sqrt{\frac{\beta_{PC2}}{\beta_{PC3}}} \tag{4.11}$$

As was shown, the threshold voltage can be adjusted by sizing both MC1 and MC3 for V_H and PC2 and P3 for V_L.

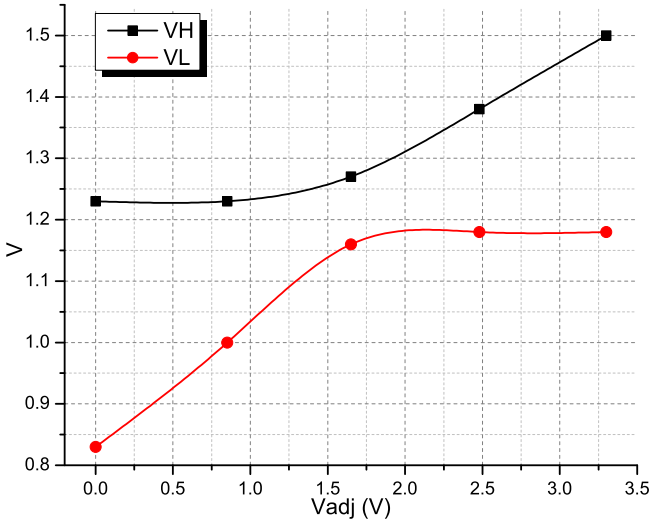
4.5.4 Adjustable 6T Schmitt Trigger Comparator

An adjustable hysteresis gap, cf. Figure 4.10, is achieved adding two cascoding MC4 and PC4. Both the low V_L and high V_H threshold can be relaxed -thus changing the hysteresis gap - by adjusting V_{adjL} and V_{adjH} as shown in Figure 4.10a . The MOS transistor sizing is concluded to the shown values setting the lower threshold $V_L \approx 1.2V$ and the upper threshold $V_H \approx 1.5V$ with $V_{adjH} = V_{adjL} = 3.3V$.

The adjustable 6T thresholds versus V_{adj} are shown in Figure 4.10b. The V_H can be adjusted from 1.3V to 1.5V while the V_L from 0.8V to 1.2V.



(a)



(b)

Figure 4.10: 6T Comparator with adjustable thresholds with 3.3V VDD

The power consumption can be reduced with scaling down of V_{DD} to $1.1V$. Again, the thresholds can be adjusted as shown in Figure 4.11. The thresholds can be adjusted in a linear fashion by sweeping V_{adjH} or V_{adjL}. They can be adjusted independently as proposed here or complementary by tying V_{adj} and V_{adjL} together. This low supply implementation of the 6T comparator with adjustable threshold is not used for this first implementation, yet in it was developed to the serve for the second implementation when the power consumption of the controller is addressed.

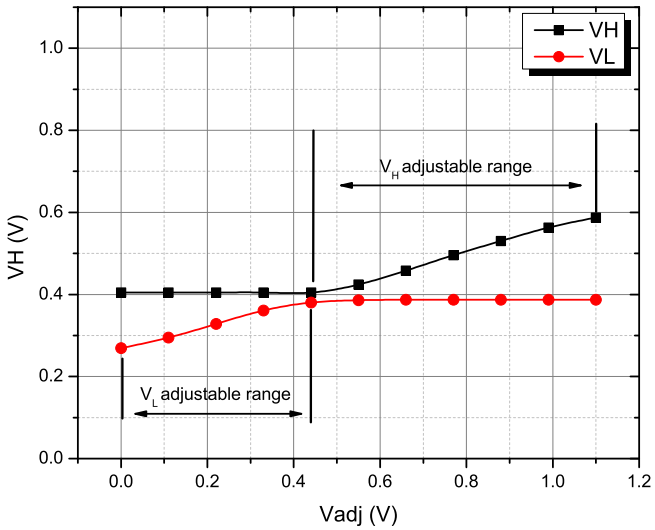


Figure 4.11: Comparator thresholds V_H and V_L versus V_{adj} with 1.1V VDD

4.6 The clock generator

This block is responsible for selecting the clock pulses according to the mode of operation - the Accumulating Mode and Transfer Mode. It includes two clocks and enabled multiplier as shown in Figure 4.3. One of two clocks is selected according to the output of the switch decision comparator. This section discusses the clock generator design.

Clocks CLK1 and CLK2 are generated with an ultra low power clocks generator implemented as shown in Figure 4.12. The generator is a relaxation oscillator inspired by [76]. The two clocks are of frequencies $f_H = 5$ kHz and $f_L = 1.25$ kHz for the fast and slow switching respectively.

The clock generator is composed of four blocks:

– Proportional-To-Absolute Temperature PTAT Voltage Reference

– Comparator

– Pulse generator

– A Self Biased Current Source SBCS

The clock pulses are generated as follows, First, the SBCS provides a constant current to charge C_{CLK} and biases the PTAT. The PTAT voltage reference generates a DC voltage V_{ref} which is constantly compared with the C_{CLK} voltage. This voltage

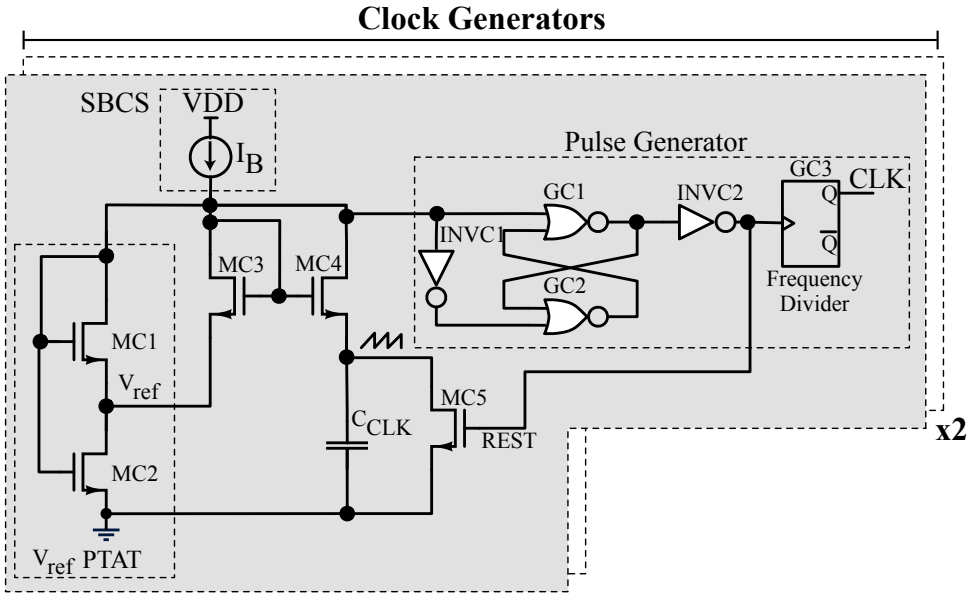


Figure 4.12: Ultra low power clocks

V_{ref} can be expressed by,

$$V_{ref} = \frac{K_B T}{q} ln\left[\frac{(w/l)_{MC2}}{(w/l)_{MC1}})\right] \tag{4.12}$$

where, K_B is Boltzmann's constant, T is the absolute temperature and q is the electron charge.

As the voltage on C_{CLK} increases reaching V_{ref} the pulse generator is triggered. The pulse generator then generates a reset pulse discharging C_{CLK}. This allows the charging process to repeat resulting in a sawtooth V_{CLK} with a period of T_{CLK}. This period can be expressed as,

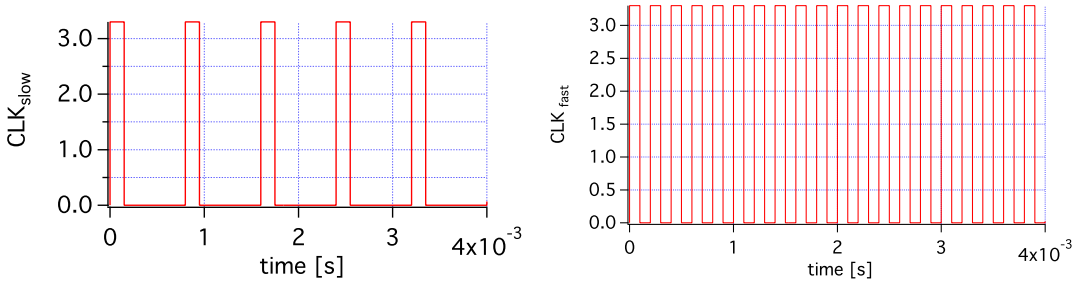
$$T_{CLK} \approx \frac{C_R V_{ref}}{I_B} \tag{4.13}$$

where V_{res} is the voltage reference generated from the PTAT voltage reference - cf. Figure 4.12.

It must be noticed that the output clock signal CLK is generated by a toggle flip flop which receives the reset pulses at its input and generates a 50% duty cycle signal with half the frequency of the sawtooth signal. The VDD for the two clocks is $3.3V$ and the comparator capacitor C_{CLK} is 0.5pF and 2.9pF for the fast (5kHz) and slow (1.25kHz) clocks respectively with the rest of the design parameters summarised in Table 4.4a. [1] A detailed analysis and design for the Self-Biased Current Source (SBCS) is presented in Appendix I.

The multiplexer MUXI multiplexer is a standard cell element assuring from the digital low voltage library of the Design Kit H35.

[1] This clock design is later on modified to decrease the power consumption using a lower VDD of 1.1V in the next chapter.



(a) Slow clock $f = 1.25$kHz **(b)** Fast clock $f = 5$kHz

Figure 4.13: Fast and Slow clock outputs

Element	Width [μm]	Length [μm]
MC1	4	4
MC2	4	32
MC3	0.4	0.4
MC4	0.4	0.4
MC5	15	0.35

(a) Clock generator MOS parameters

Element	Name	Library
INVC1	INV0	CORELIB
INVC2	INV0	CORELIB
GC1	NOR20	CORELIB
GC2	NOR20	CORELIB
GC3	TFC1	CORELIB

(b) Standard Cell Gates

Element	Value	Note
I_B	100 pA	Generated by SBCS
V_{ref}	70mV	Generated by PTAT
C_{CLK1}	0.5pF	Fast Clock 5kHz
C_{CLK2}	2.9pF	Slow Clock 1.25kHz

(c) General Design Paramaters

Table 4.4: Design parameters for the two clock generators

4.7 Switch Control Block

The switch control block presented earlier in Figure 4.3 is responsible of generating the power switch SW_{LI} control commands, see section 4.4. It is composed of:

– Multiplexer - MUXII.

– Switch Driver which includes:

(a) Time delay (b) Edge Detector (c) Flip-flop gate driver

– Flip-Flop level shifter.

– Power Switch - SW_{LI}.

This section is dedicated to the transistor level implementation of the switch control block.

The MUXII, which allows an activation of the switch driver, is a standard gate cell identical to MUXI.

The architecture of the switch driver is motivated by the following consideration. Using AMS 0.35μm technology, the high voltage transistors can stand high voltages up to 50V between the source and the drain electrode, yet the gate voltage is limited

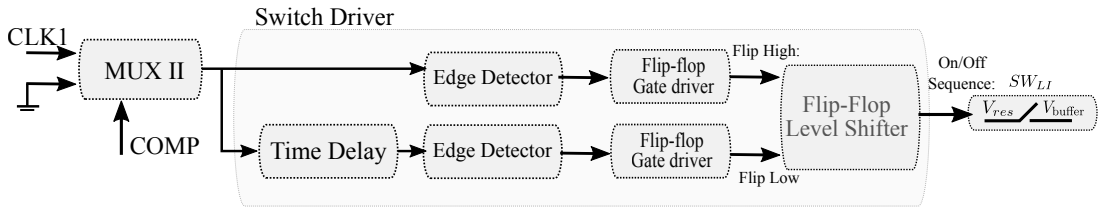


Figure 4.14: Switch Control Block

to a low voltage of 3.3V [2] - with respect to the bulk. If PMOS transistor is to be used, the gate voltage is has to be referenced to the source voltage, which is connected to V_{res} in our design. Thus, to be able to operate the PMOS gate the control command should swing between V_{res} and $V_{res} - 3.3V$. However, since all the controlling block of the LI controller operates in low voltage (e.g 3.3V) a level shifting stage is needed. This level shifting is performed using a dynamic flip-flop level shifter, cf Figure 4.15.

Thus the LI switch must compose of [21]:

– The high-side PMOS transistor operating in triode mode when on.

– The level-shifter LS block translating a low-voltage enable pulse so to generate on or off gate voltage referenced to V_{res}.

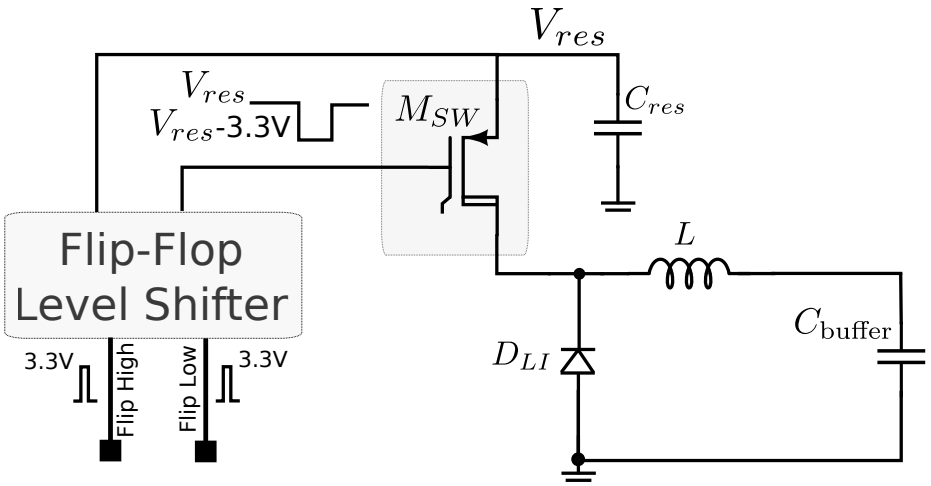


Figure 4.15: Power switch with a level shifter to operate its gate commands

4.7.1 Power Switch - SW_{LI}

The switch M_{SW} was developed by a previous PhD student - Andrii Dudka [21] and is slightly modified to suit our design. The PMOS switch M_{SW} [3] is triggered to V_{res} for its Off state and $V_{res} - 3.3$V for the On state using a level-shifter to raise the low trigger voltage into this necessary voltages.

[2] Later this block is adjusted to operate with lower trigger voltage of 1.1V (Chapter 5)

[3] A PMOS transistor is driven with a voltage level lower than the highest potential in the circuit. In contrast, using a NMOS switch would require to generate a voltage above the higher voltage, adding complex and energy consuming blocks to the design.

The power switch M_{SW} is designed to withstand current up to few tens of milli-ampere and also to have a low on resistance. This is achieved through maximising the W/L ratio. With a minimum length of $L = 1\mu m$ dictated by the technology constrains, the width of M_{SW} is chosen to be $1000\mu m$ and the on-resistance is 39Ω [21].

4.7.2 Dynamic flip-flop level shifter

This dynamic flip-flop level shifter was first introduced by [22]. It uses two capacitors to maintain the set C_{set} and reset C_{rest} state of the flip flop, cf. Figure 4.16. This is achieved through two controlling pulses to charge either the state-storing capacitors C_{res} or C_{rest} according to the required state. Depending on the input at which a pulse is applied ("on" or "off"), one of the output nodes - set or reset - is connected to V_{res} or $V_{res} - 3.3$ respectively. The change in states is achieved by charging the state-storing capacitors through the bias currents I_b.

Through using series of forward-biased didoes, the voltage drop at the output node V_{out} is limited. However, these diodes usually exhibit losses through junction capacitance in reverse bias which contribute to gradually losing the stored state in the capacitors C_{set} and C_{rest}, due to charge sharing. This leads to a decrease in V_{out} of the flip-flop which is the gate driving voltage for the power switch M_{SW}. This in turns will increase the on resistance of the power switch, leading to higher energy consumption. To overcome charge sharing problem Dudka et al; [21] proposed to introduce two switches on' and off' to isolate the C_{res} from C_{rest} when flipping the state. This is achieved through synchronised yet shorter pulses matching the on and off controlling pulses, cf. Figure 4.16, through SW3 and SW4 switches.

The transistor level implementation of the flip-flop and the power switch M_{SW} are shown in Figure 4.17. The switches SW3 and SW4 are implemented using current mirrors that allow to disconnect C_{res} and C_{rest} earlier as the transition from high-to-low happens for the trigger pulses on the switches MN1 and MN2. This technique replaces the need to implement a synchronised SW3 and SW4 switches, as does not require additional control signals on' and off' and hence presents a more simple and less power-consuming solution [21]. Moreover, exploiting transistor gate capacitance allows the replacement of the two capacitors C_{set} and C_{reset} by the gate capacitances of the transistors MP4 and MP5, though a proper sizing.

– The set capacitor is equivalent to the gate capacitance of M_{SW} and $MP4$ and is calculated by,

$$C_{set} \approx C_{ox}\left[(WL)_{M_{SW}} + (WL)_{MP4}\right] = 4.7pF \tag{4.14}$$

– The reset capacitor is the $MP5$ gate capacitance and is calculated by,

$$C_{reset} \approx C_{ox}\left[WL\right]_{MP5} = 0.55pF \tag{4.15}$$

– The charging current of for the set and reset capacitors has to be independent on V_{res}. It is supplied through MN1 and MN2 respectively. Both MN1 and MN2 are designed to operate in saturation region with $I_{d_{MN1,2}} = 2mA$, and the ratio of W/L =

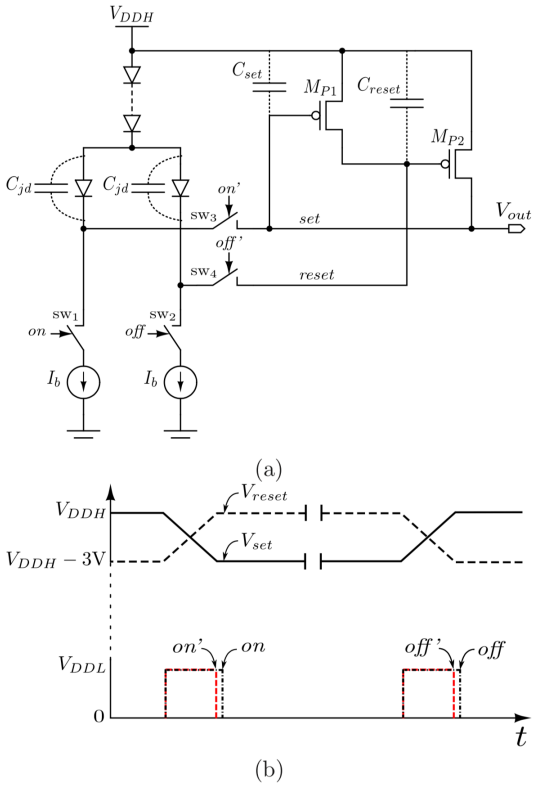


Figure 4.16: (a) Dynamic flip-flop voltage level shifter [21]. (b) Voltage diagram of the proposed level shifter switching levels

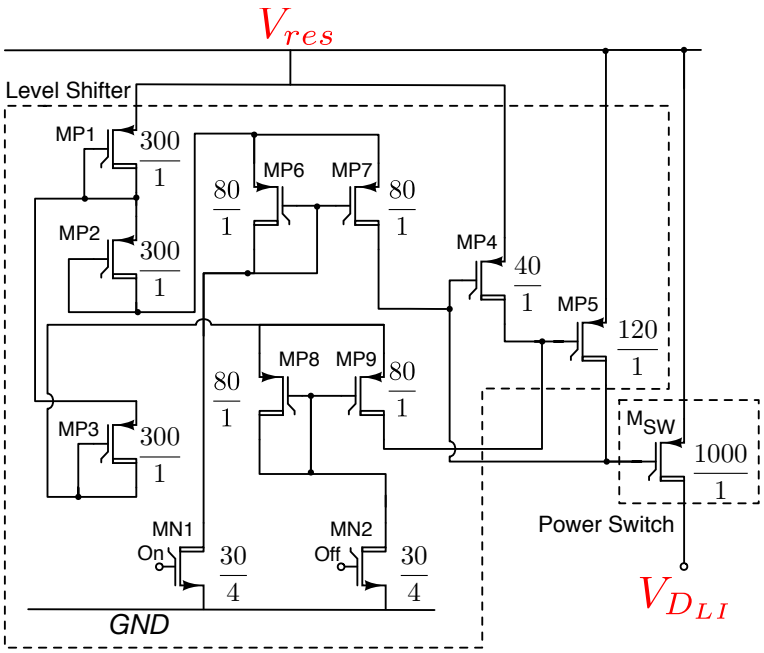


Figure 4.17: High Side power switch developed in AMS 0.35μm technology

30/4 [4]. This is calculated from,

$$I_{d_{MN1,2}} = \frac{1}{2}\mu_n C_{ox}\left[\frac{W}{L}\right]_{MN1,2}(V_{gs_{MN1,2}} - V_{th})^2 \tag{4.16}$$

with transistor parameters listed in Table 4.2. The value of $V_{gs,\mathrm{MN1,2}}$ are determined by the voltage drop on two series diode connected transistors MP1 and MP2. Together MP1-MP2 and MP1-MP3 provide a voltage drop of -2.8V.

– The time needed for both the on and off triggers is the time needed to charge the set and reset capacitors to their V_{gs} and can be calculated by,

$$t_{on} = \frac{C_{set} \cdot V_{gs,MN4}}{I_{d_{MN1}}} \quad , \quad t_{off} = \frac{C_{set} \cdot V_{gs,MN5}}{I_{d_{MN2}}} \tag{4.17}$$

The t_{on} and t_{off} are set to 50ns and are triggered using gate flip-flop gate driver block, see section 4.7.3. Moreover the frequency and the duty cycle of the trigger pulses are defined by other elements of the switch control block, namely the MUXII and the time delay element, as will be explained in the next subsections.

4.7.3 Switch Driver

The gate driver generates the switching commands to SW_{LI} as shown in Figure 4.18. As can be seen, the clock pulse CLKI is with 50% duty cycle which is used to generate the switching pulse. Generating SW_{LI} command depends on the implementation of the switch itself. The SW_{LI} is controlled through a flip-flop level-shifter that flips its state through low voltage pulse command. This means precise triggering command is needed to flip the state of SW_{LI} with a distinction between two pulses t_{on} and t_{off}, subsection 4.7.1.

The output of MUXII is used to trigger the flip-flop level shifter high, while a delayed version of the output is used to flip it back low. This is explained in details in the rest of this subsection.

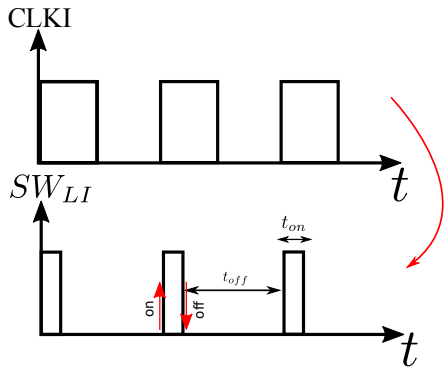


Figure 4.18: Switch Driver command to SW_{LI}

[4]Later this ratio will be increase to allow for 1.1 pulse to operate the level shifter

Edge Detector

The rising edge detector senses the low-to-high transition of MUXII output. This is achieved through comparing MUXII output with an AND gate of an inverted and delayed version of MUXII output. The duration of the pulse that is seen on the output of the AND gate is defined by the RC delay. A 50ns output pulse of the edge detector is achieved though a 50KΩ and capacitance of 1pF with both implemented on chip.

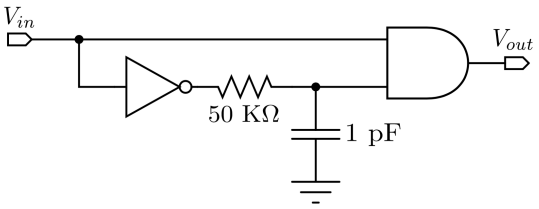


Figure 4.19: Rise-edge detection circuit for SW_{LI} command generation;

Gate Driver

To drive the two transistors responsible for flipping the state of the level-shifter MN1 and MN2, cf. Figure 4.20, an inverting gate drive is used. This gate driver amplify the switching command from the MUXII. This is achieved through three series inverters stages. Each stage has an increased size as shown in Figure 4.20. It must be notice that the first inverter is a part of the rising edge detector.

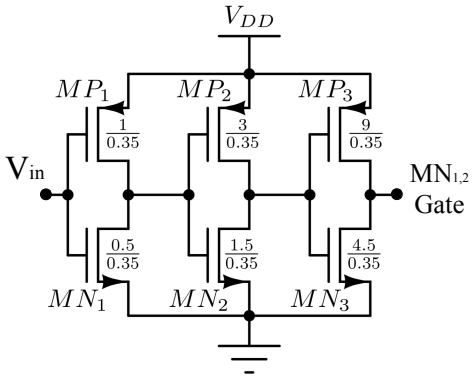


Figure 4.20: Level shifter gate drivers for MN1 and MN2

Time Delay

Time delay block is used to generate a delayed version of the flip-flop level shifter on-trigger. This delayed trigger is the low pulse of the level shifter. It is necessary for the multiple energy shot transfer. Recalling section 3.6, the energy transfer is achieved in a multiple energy shot. With each on pulse followed by an off pulse by a time constant that defines the energy shot. Since this time constant - energy shot time - is constant, it is defined by an integrated RC circuit.

4.8 Simulation Results: First Implementation

The load interface controller transistor level implementation was simulated with the design parameters of:

– Inductor $L = 10\text{mH}$ and the maximum allowed current $I_{L_{max}} = 15\text{mA}$.
– Reservoir capacitor $C_{res} = 1\mu\text{F}$.
– Optimum interval for V_{reS} between $V_{res_H} = 6\text{V}$ and $V_{res_L} = 5\text{V}$.
– Buffer capacitor $C_{\text{buffer}} = 20\mu\text{F}$.
– The timing of the switch is $t_{on} = 25\mu s$ and $t_{off} = 175\mu s$.
– For this simulation the input energy flux is assumed to be much greater than in real application, $I_{harv} = 2\mu A$. This will reduce the simulation time. It must be noticed that the load interface control is not impacted with the input energy flux at this stage, since its supply voltage is assumed to be an standard voltage supply of 3.3V.

The simulation shown in Figure 4.21a is for 5 seconds operation. A zoomed plot shows the details of the multiple energy-shot transfer of energy from C_{res} to C_{buffer}, Figure 4.21b. As can be seen the maximum inductor is indeed fixed to less than 15mA, with each successive energy-shot transfer having lower max current. This is due to that in each energy-shot transfer the buffer voltage is increased by the pervious energy shot transfer.

The main goal for this implementation was to present a transistor level implementation of LI where the energy is extracted from the CC C_{res}, and dumped into a intermediate storage C_{buffer}. Moreover, multiple energy-shot transfers was adopted to increase the transfer efficiency, see chapter 3. At this stage no load is connected nor load regulation was considered, as power consumption optimazation was first needed for the LI blocks.

The average total power consumption of each block is shown in Figure 4.22, with the switch and comparator consuming the largest average power of the LI. The average power consumption of each block is presented with an overall power consumption of $2.1\mu W$ for 5s operation .

This however pushes the boundaries for the energy consumption of the LI controller, and leaves the load with barely any energy. Thus, in the next chapter, we tackle the blocks of the LI controller which consumes most of the energy, mainly the comparator. Moreover, the next goal would be to implement a semi-autonomous system that is capable to operate with just an initial charge to its harvesters and buffer capacitors. Thus, load regulation block must be addressed in the next step of the system design.

4.9 Summary

This chapter presented the main blocks for the intimidate LI block including the LI controller. This block is responsible for regulating the internal voltage of the CC, V_{res} , through regularly extracting the energy from the CC into a buffer capacitor C_{buffer}. The energy extraction is achieved through first defining the mode operating for the LI, and then generating sequences of command pulses that controls the LI switch SW_{LI}, which allows the energy to be extracted in the form of multiple energy-shot transfer.

The LI was fully proposed in transistor level using ams 0.35 μm high voltage technology H35B4D3, with the LI controller being fully integrated in CMOS. The goal of

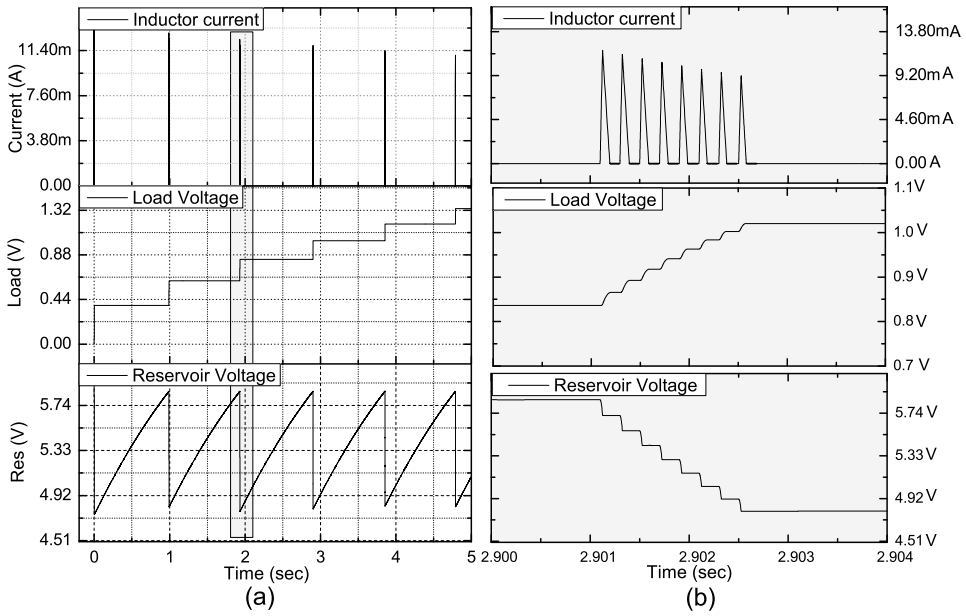


Figure 4.21: Load interface MOSFET simulation of multiple energy-shot transfer showing inductor current $i_L(t)$, reservoir $V_{res}(t)$ and load $V_{load}(t)$ voltages where (a) $0s < t < 5s$ (b) $2.9s < t < 2.904s$

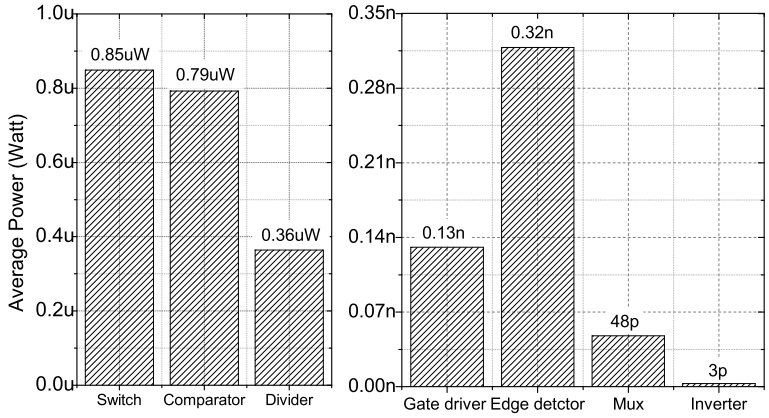


Figure 4.22: The average power of each LI block simulated over 5 seconds

maintaining V_{res} within its optimum region was met through using a hysteresis comparator that has its hysteresis gap fitted to the optimum interval of V_{res}. A degree of freedom with the thresholds was introduced through proposing adjustable thresholds of the comparator. A transistor level simulation showed that the LI controller consumed around 2μW of average power in 5s of operation

In the next chapter we tackle the power consumption problem, proposed a buffer voltage regulation block and introduce a semi-autonomous system that operates with only charges in the CC and the buffer capacitor.

Chapter 5

Second Implementation of Load Interface System

Contents

5.1 Overview

This chapter presents an improved version of the Load interface in terms of power consumption and load voltage regulation. First we investigate the power consuming elements of the design presented in Chapter 4, then we introduce alternative implementations for these elements which ends up reducing the overall power consumption.

Second, a load voltage regulator is introduce to periodically supply a load with a regulated voltage. Finally, the autonomy of the system is test by self-supplying the reservoir capacitor voltage regulator and the load voltage regulator using the buffer capacitor.

The improved system address the following goals:

– Lowering the power consumption of the LI controller.

– Stablilized the load voltage around the nominal low voltage.

– Improving the energy transfer efficiency.

In addition to the implementation presented earlier in Chapter 4 goals which included:

– Regulating V_{res} to optimal operation mode of the conditioning circuit.

– Stepping down of V_{res} since to supply the load.

The implementation presented in Chapter 4 suffered from few short comings that needed to be improved upon to decrease the overall power consumption of LI controller aught.

These short comings, which are summarised in Figure 5.1, include:

– High losses in comparator conduction current when switching states.

– Two clocks working in background regardless of the operating mode.

– Standard supply voltage source of 3.3V which is separated from the LI controller.

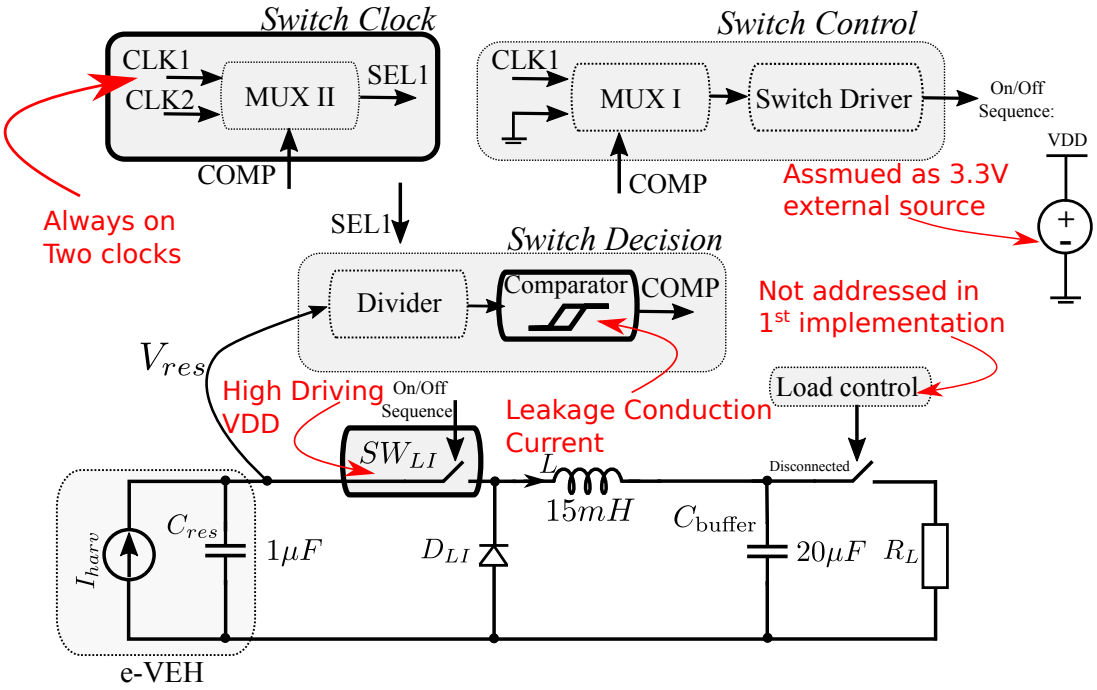


Figure 5.1: First implementations drawbacks

5.2 Second implementation modification

The LI modified controller, shown in Figure 5.2, can be summarised in the following points:

– First the supply voltage is reduced from 3.3V to 1.1V which allowed quadratically reduction of power.

– The diode-connected voltage divider where replace by two off-chip resistances for the voltage divider. This allowed the elimination of V_{res} sampling process.

– To ensure energy is transferred in precisely defined shots a safe-clock gating block is used.

– Load voltage regulation is added allowing the buffer capacitor to supply the LI controller with the required supply voltage.

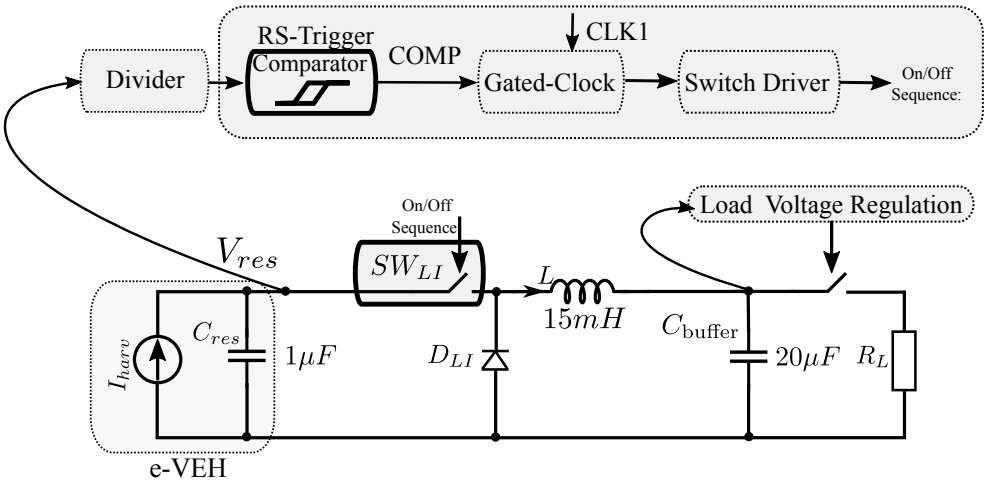


Figure 5.2: Modified Load Interface system blocks

First, the improved implementation is examined in terms of the power consumption with no load voltage regulation. Then the load voltage regulation implementation is proposed and a full transistor level simulation is presented. To distinguish between the two regulating block through out this chapter the reservoir regulation block is called condition circuit regulator CCR, while the load voltage regulator is called LVR.

5.3 Comparator Modification

In the first implementation presented in chapter 4, the main power consuming block was the 6T hysteresis comparator. This is due to the direct current path it provides between VDD to ground when switching states. A first attempt to reduce this power consumption was to reduce the VDD required to power up the comparator. This however reduced the adjustable range of the comparator's thresholds, cf. Figure 4.11 due to scaling down the supply voltage to values comparable to the transistors threshold voltage (see Table 4.2). To further reduce the power consumption of the comparator, we adopted another comparator design based on RS triggers.

5.3.1 RS-Trigger based Hysteresis Comparator

A low power implementation of the Hysteresis comparator is the RS-Trigger based comparator shown in Figure 5.3a. It was first reported in [77, 78]. The design was later improved upon in [79] as shown in Figure 5.3a. These hysteresis comparator circuit proved to have a very well defined hysteresis gap and is well suited for low-voltage and high speed applications. However the drawback of such circuit was that logical threshold voltages are fixedly designed. Later in this chapter, we present an adjustable threshold implementation of the RS-trigger based comparator.

5.3.2 RS-trigger hysteresis comparator operation

The RS-trigger comparator is composed of two inverters INV1 and INV2. These two inverters have two different inverting points V_H and V_L. The outputs of the two inverters connected to a NAND RS-Trigger where the output of V_H inverter is connected to the SET terminal of the RS-Trigger and the V_L is connected the RESET terminal. The transition of each switching event can be seen in Figure5.3b.

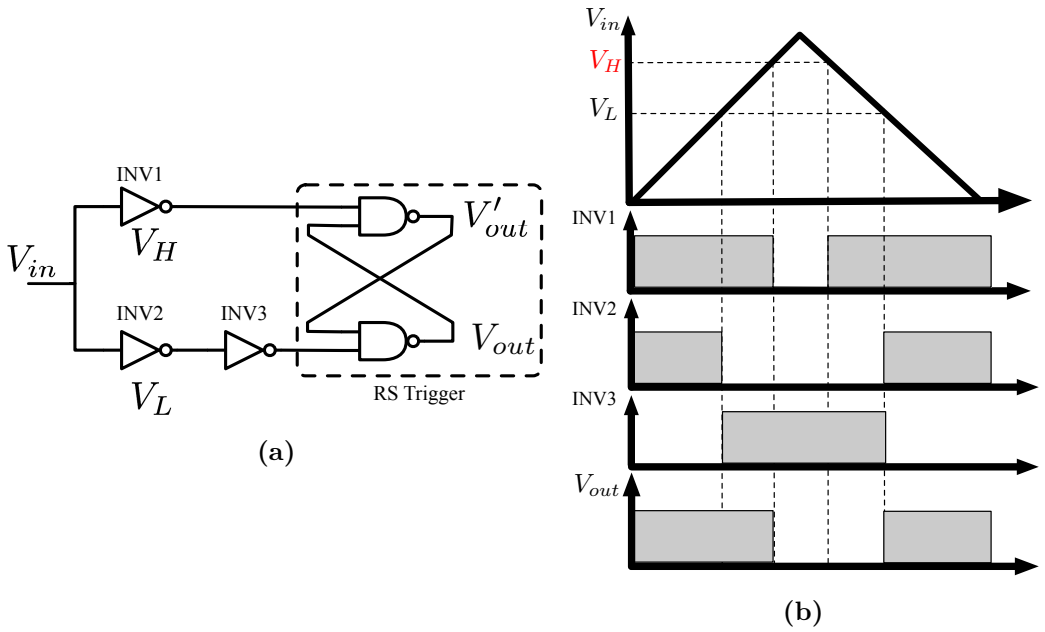


Figure 5.3: RS Trigger comparator (a) schematic (b) switching transition

The operation of the RS-trigger comparator can be explained as follows:

– Assuming the input voltage is initially zero. The output of INV1 and INV2 are both high, while INV3 is low. Thus the RS trigger set is high, and reset is low rendering the output of the comparator high.

– As the input voltage increases and reaches the first triggering voltage V_L the lower inverter INV2 is trigger to switch to low which in turns triggers INV3 high. The high threshold inverters keeps its high state. The RS trigger is now subjected to both high set and reset, forcing the comparator output to keep its previous high state.

– As the input voltage increases further and reaches the high trigger voltage V_H for high inverter INV1, INV1 changes its state to low. Still both INV2 and INV3 keep their pervious state. The RS trigger input at this stage is low set and high reset, thus the comparator output is now flipped to low.

– Now, when the input voltage starts to decrease, the first inverter to switch its state will be the high comparator INV1, flipping back to high when the input voltage decreases below V_H. The input of the RS trigger now will be high set and high reset which again force to comparator to keep its pervious output low state.

– Finally, when the input voltage falls below the triggering voltage of INV2, INV2 switch state which in turns forces INV3 to flip from high to low. The input to the RS trigger now would be high set and low reset, rendering the output of the comparator to flip again to high.

It must be noticed that, since by definition the upper threshold $V_H$is always higher than the lower threshold V_L, the illegal state of the RS-Trigger (Set=0, Reset=0) is granted not to occur.

5.3.3 RS-trigger comparator design

The design of the RS-trigger thresholds is achieved by defining the logical thresholds for the inverters INV1 and INV2 through defining the inverters' aspect ratio. If a supply low supply voltage of 1.1V - which is comparable to the threshold of the CMOS transistor used - powered the inverters, the triggers threshold are defined by [77],

$$V_M = \frac{V_{Tn} + r(\mathrm{VDD} + V_{Tp})}{1 + r} \tag{5.1}$$

where $r = \sqrt{k_p/k_n}$, $k_p = \mu_p C_{ox}\left[\frac{W}{L}\right]_p$, $k_n = \mu_n C_{ox}\left[\frac{W}{L}\right]_n$, V_M is the inverter trigger point and V_{T_n} and V_{T_p} are the threshold voltages for the nmos and pmos transistors used for the inverter [77].

The inverter trigger point is weakly sensitive to the variation of the transistor's aspect ratio, especially when the ratio of the supply voltage to the transistor threshold is small. This gives the RS-trigger comparator the advantage of being less sensitive to fabrication process variation. However, this comes with the cost of larger die size especially when adjustable threshold RS-comparator is proposed later in section 5.3.5 .

5.3.4 Comparing 6T and RS-trigger comparators

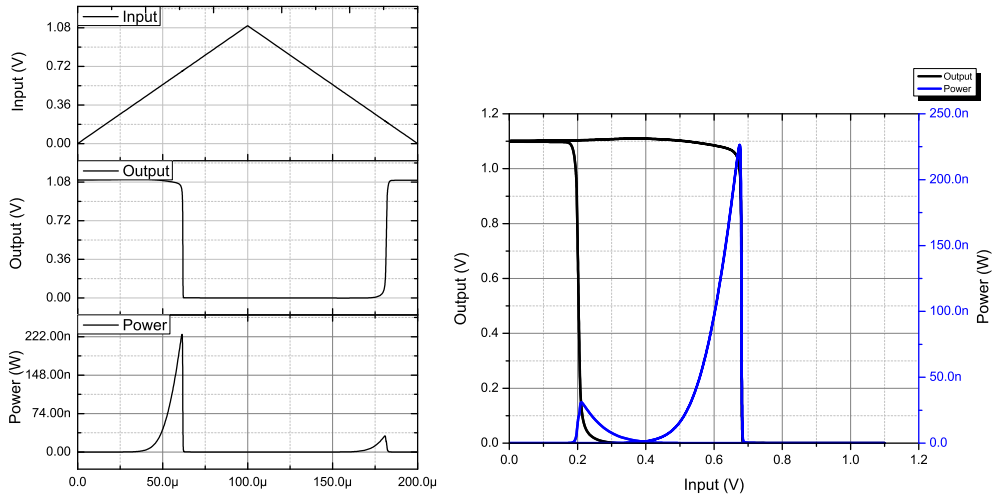
To compare between the two comparators architectures, 6T and RS-trigger, in terms of power consumption a test-bench is set up for both comparators where both are implemented in ams 0.35μm technology. Both designs will target the same switching triggers and thus the transistors dimensions will be updated accordingly. Moreover, the length size of all transistors in both architectures are kept equal. The power supply for both architectures examined are low supply voltage of 1.1V.

6T comparator testbench

A testbench is set for the 6T comparator similar to the one presented in chapter 4, cf. Figure 4.7. The transistor sizing is concluded to the summarized value shown in Table 5.1. These will set the lower threshold $V_L \approx 200mV$ and the upper threshold $V_H \approx 680mV$. The simulation results are shown in Figure 5.4. Figure 5.4a shows the input voltage changes between 0V to 1.1V, the output of the comparator being triggered at different upper and lower triggering voltage and the instantaneous consumed power. It can be seen that the transition does not happen instantaneous at V_M. This drawback allow a direct current path when changing states, especially when transition from high to low, see section 4.5.3.

Table 5.1: 6T comparator transistor sizing

CMOS	Width(μm)	Length (μm)
MC1	1	10
MC2	2	10
MC3	0.5	10
PC1	3.5	10
PC2	1	10
PC3	3	10



(a) **(b)**

Figure 5.4: Simulation of 6T comparator (a) Transient Response (b) Transient response presented as a parametric curve of input-output along with the instantaneous power

RS-trigger Comparator

A similar testbench is build for the RS-Trigger comparator with identical thresholds targeted to match with the 6T comparator where $V_L \approx 200mV$ and $V_H \approx 640mV$.

The MOS sizing were concluded to the values shown in Table 5.2. The comparator is subjected to the same input single. The transfer characteristic is shown in Figure 5.5.

Table 5.2: RS-Trigger CMOS sizing

Element	CMOS	Width (μm)	Length (μm)
INV1	MN	0.35	10
	MP	100	10
INV2	MN	0.35	10
	MP	0.5	10
INV3	MN	0.35	10
	MP	0.5	10

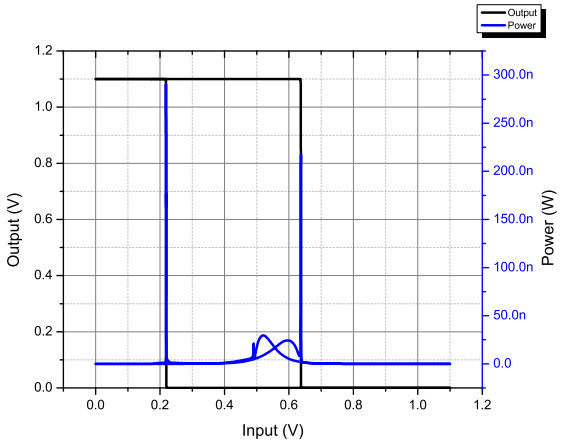


Figure 5.5: Transient response presented as a parametric curve of input-output along with the instantaneous power simulation for RS-trigger comparator

Energy consumption of 6T and RS-trigger comparator

To illustrate the superiority of the Rs-trigger comparator over the 6T comparator, the energy consumed in two transitions - high-to-low and low-to-high - is calculated for the pervious testbenches. The energy consumed is calculated for duration interval of $200\mu s$ with results shown in Table 5.3.

The results shows almost 4 times reduction in the consumed energy between the two comparators under the same operating conditions. This lower energy consumption justifies the adoption of the RS-trigger comparator over the 6T comparator. The rest of this chapter is dedicated to discuss the modification required for LI controller that allows the adoption of this comparator.

5.3.5 Adjustable RS-Trigger comparator

This section presents a method to allow a degree of freedom to the RS-Trigger comparator fixed thresholds. As described in 5.3.3, the threshold of the comparators are defined through the aspect ratio of the transistors forming INV1 and INV2. These

Table 5.3: Energy for Single ON and OFF switching

Comparator	Energy (Joules)
6T	$1.89 * 10^{-12}$
RS	$0.503 * 10^{-12}$

are thus fixed once the chip is fabricated. What we propose is adding a number of folded inverter design for these inverters that can be activated with external enable signals when needed allowing to modify the effective aspect ratio of the transistor. A self-adapting thresholds is not the focus of this work.

An adjustable RS Trigger comparator as shown in Figure 5.6 through external enable commands a_0 & a_1 for the lower threshold. The principle behind this adjustability is to change the effective equivalent width of the transistor.

Consider only a lower adjustable threshold two cascaded inverters are introduced. These inverters are composed of two main transistors N0 and N1 as well as two enabling transistors NE0 and NE1. The sizing of N0, N1, NE0 and NE1 are summarized in the Table 5.4. This arrangement allows a dynamic range of almost 100mV.

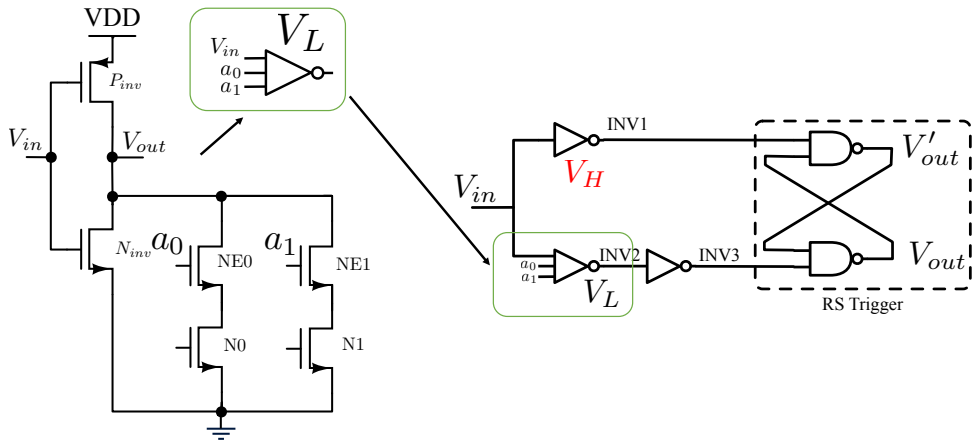


Figure 5.6: Adjustable inverter switching point

Table 5.4: Adjustable Inverter Sizing

CMOS	Width (μm)	Length (μm)
N0	10	0.35
NE0	0.5	0.35
N1	100	0.35
NE1	0.5	0.35

Table 5.5: Adjustable V_{lower}

State	V_{lower}V
a0=0, a1=0	453mV
a0=1, a1=0	400mV
a0=1, a1=1	365mV

A test-bench was setup for to test the adjustable lower threshold for the RS-comparator as been from the transfer characteristic shown in Figure 5.7. It demonstrates that the dynamic adjustable range for the lower threshold is 100mV from 350mV to 450mV with a 50mV step set by the two bit control a0 and a1. This however comes

at the cost of power consumption as can be seen from Figure 5.8 which shows the transit response of the adjustable RS-trigger comparator along with the instantaneous power consumption.

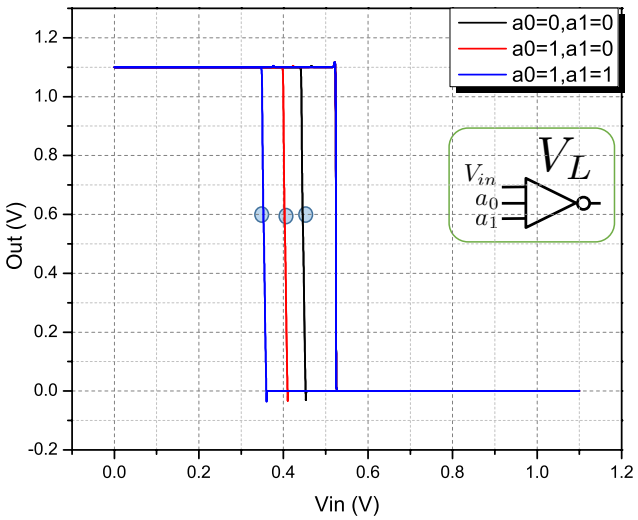


Figure 5.7: Adjustable lower threshold switching point

In the practical implementations this can be adopted to provide an adjustable threshold that can be controlled externally when needed. The rest of this chapter is dedicated to present an improved version of the LI in terms of the power consumption.

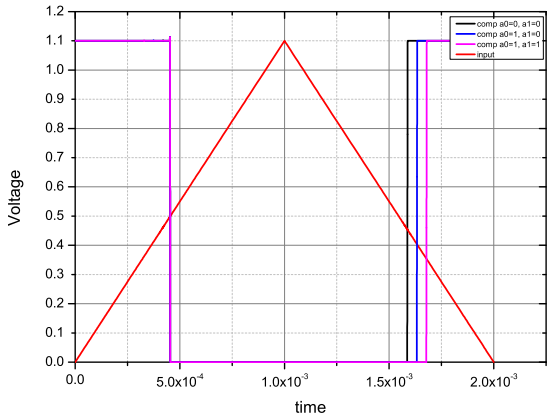
5.4 The CCR comparator

The internal voltage of the harvester V_{res} is regulated to its optimum interval by CCR Controller. By fitting the hysteresis gap of COMP1 comparator to a scaled down version of C_{res} optimum interval a switching decision. This comparator for the CCR replaces the 6T comparator in the previous implementation, yet serves the same purpose of generating the switching decisions described in section 4.4.

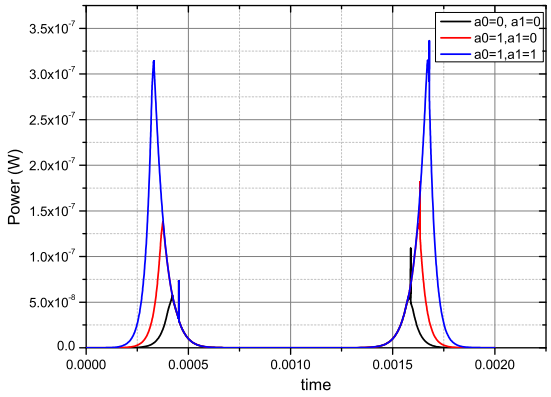
The sizing of COMP1 transistors are shown in Figure 5.9, with the standard NAND gates with both pull-up and pull-down transistors minimum size to ensure fast transition ($\frac{0.35\mu m}{10\mu m}$).

5.5 High side power switch - SW_{LI}

The high side power switch - shown in Figure 5.10 is composed of a level shifter based on zero-static current analogy flip-flop topology level shifter and a high voltage PMOS pull-up transistor presented earlier in Chapter 4. The level shifter flip flop holds its state through the two capacitors C_{set} and C_{reset}. These capacitors are formed by the gates of the high voltage transistors MP4 and MP5. The C_{set} represented the total capacitance of the gates of MP4 and MSW, while C_{reset} is the gate capacitance of MP5. The on and the off signals are handled by the two NMOS transistors MN1 and MN2. They flip the state of the flipflop through either charging C_{set} or C_{reset} to $V_{res} - 2.8V$.



(a)



(b)

Figure 5.8: Simulation results for an adjustable RS-trigger comparator (a) Transient Response (b) instantaneous power

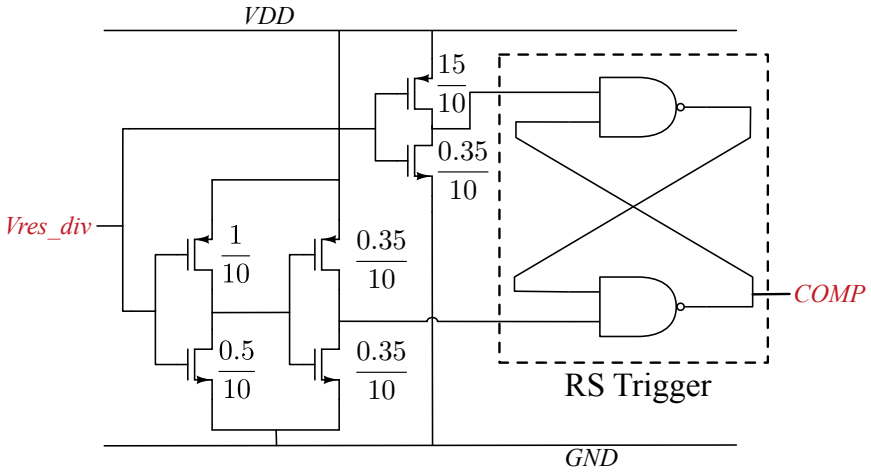


Figure 5.9: Hysteresis comparator schematic - COMP1

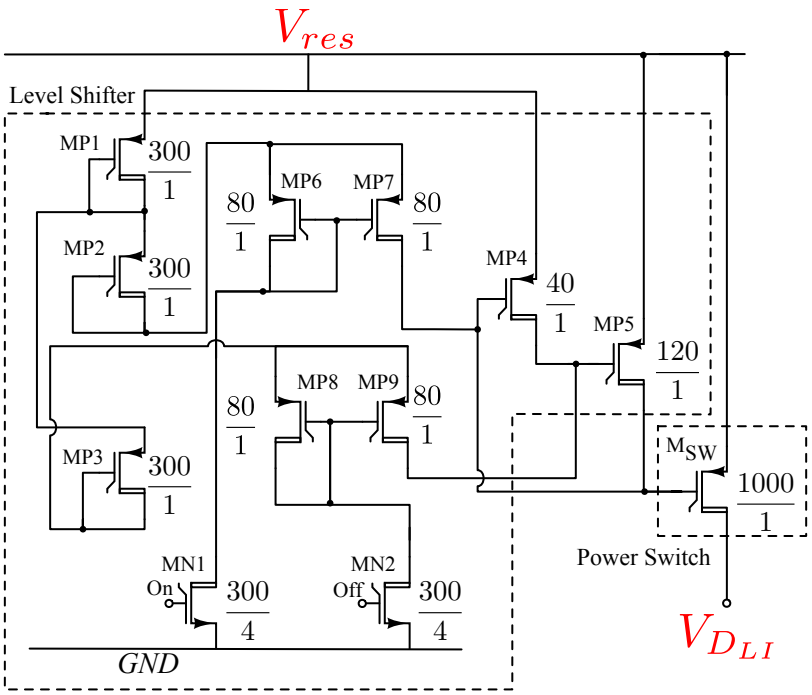


Figure 5.10: Power Switch with zero-static current level shifter

The ON (OFF) pulse duration is modified from the earlier version of the switch and is set to charge C_{set} (C_{reset}) using a low voltage of 1.1V. The necessary adjustments is made to the power switch control transistors MN1 and MN2 with the lengths shown in Figure 5.10. The width is increased to 300μm for both MN1 and MN2 to maintain the drain current of 2mA as shown in Figure 5.11. This however will require to also modify the gate driver to be able to safely drive MN1 and MN2 gates with their increased capacitive load. A 2.5V voltage drop is defined by MOS diodes connected transistors M1 - M3. This low supply voltage is necessary to maintain low power consumption of the CCR blocks. It also enables the system to self power using a pre-charged supply capacitor V_{buffer}.

5.6 Safe-clock gating block

To insure proper switching for the harvester regulator and that every ON command is followed by a OFF command an enabled clock (latch trigger) is used as shown in Figure 5.12. This block is needed in order to have integer number of the clock pulses and to avoid truncated clock pulse. The CCR Controller incorporates a 3kHz clock similar to the one introduced in Chapter 4.

5.7 CCR using the second LI implementation

The transistor level implementation of the CCR controller is shows in Figure 5.13. With the controller power optimised to operating at a low VDD of 1.1V, simulation -

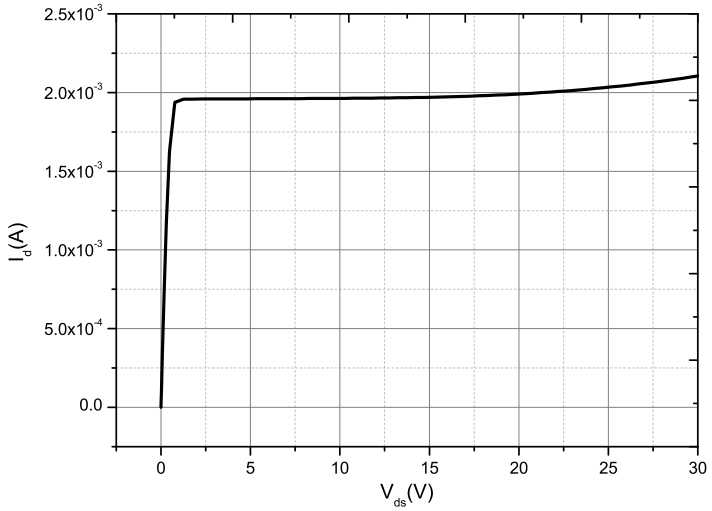


Figure 5.11: Characteristic of MN1 and MN2 showing V_{ds} vs I_d

shown in Figure 5.14 - shows the LI controller average power is $<$ 100nW as summarised in Table 5.6. This is an order of magnitude improvement in the consumed power compared to the first LI implementation presented in section 4.8 which had an average power consumption of 2μW.

The transistor level simulation shown in Figure 5.17, had the following parameters:

– Optimum interval set for $V_{upper} = 10$V and $V_{lower} = 7.5$V.

– LI inductor = 15mH.

– Reservoir capacitor of $C_{res} = 1\mu$F with initial voltage of 10V.

– Buffer capacitor $C_{\text{buffer}} = 20\mu$F which was initially depleted of charges.

– CCR controller supply is a pre-charge capacitor separated from the controller.

– Input energy flux is defined by a current source accounting for 0.6μW input power.

The system was simulated to run for 120s in which 3 energy transfers occurred. A zoomed-in of the simulation is shown in Figure 5.17 showing the multiple energy-shot transfer taking place. A series of precisely defined on/off pulses defines these shots.

To compare the performance of the improved implementation with the implementation of Chapter 4, the average power consumption of each block of the LI is calculated for 120s of operation. In section 5.9.3, the energy consumption of a single transfer is discuss in details, yet here the average power is presented as an indicator to the reduced overall power of the LI controller. As shown in Table 5.6, the comparator average power consumption over 120s is 3.3nW while the time delay is 75nW. The time delay consumption is inevitable, since it is used with every single energy-shot transfer, while the comparator is only activated 3 times in the 120s.

In the next section, we focus on regulating the load voltage as without such regulation V_{buffer} will continue to increase until reaching a saturation point where no more energy can be transferred. Moreover, the buffer voltage needs to be regulated as it should eventually replace the dummy supply voltage C_{dummy}. This will allow autonomous operation of the LI controller.

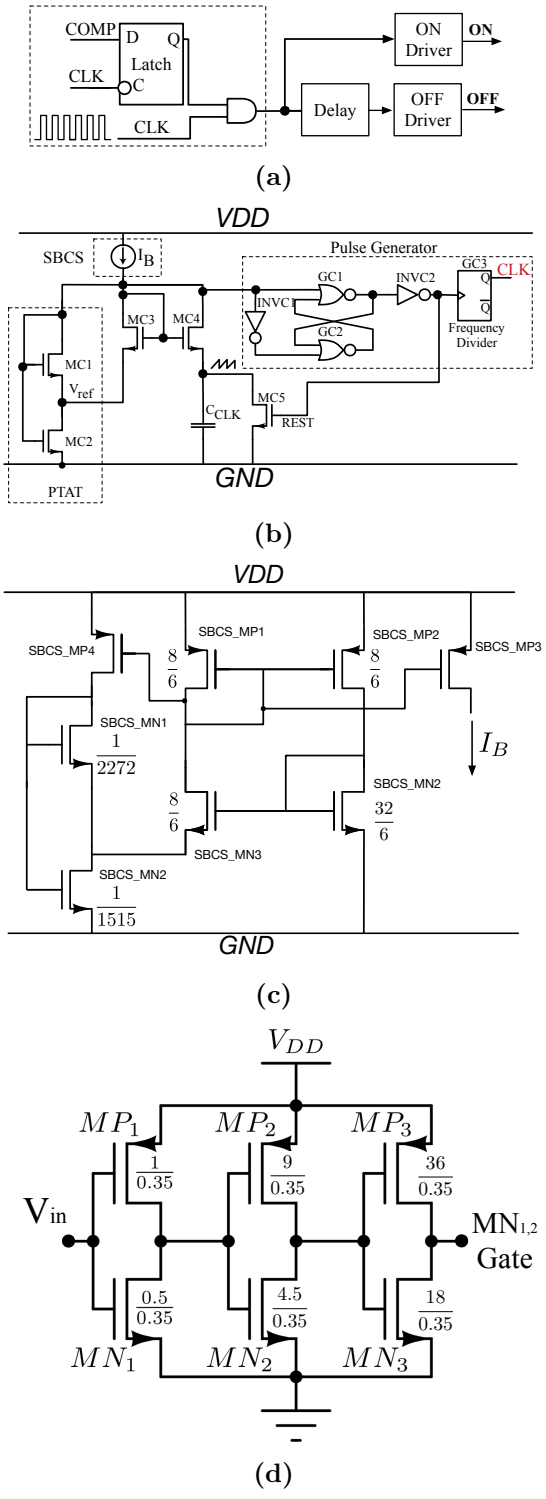


Figure 5.12: Safe-clock gating showing (a) ON/OFF switching architecture (b) clock generator (c)self-biased current source SBCS (d) gate drivers

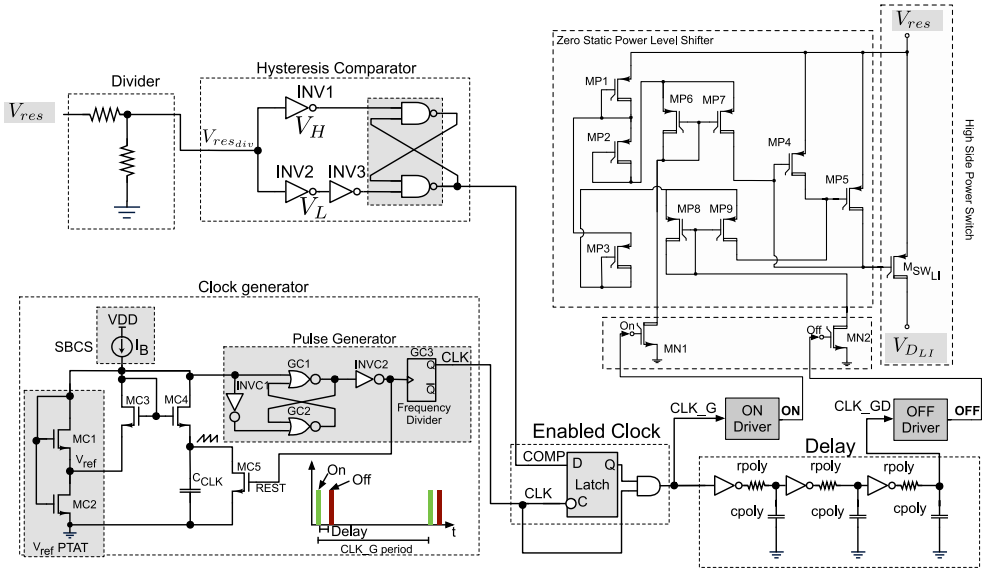


Figure 5.13: Modified Load Interface system blocks

Table 5.6: Average Power Consumption modified LI

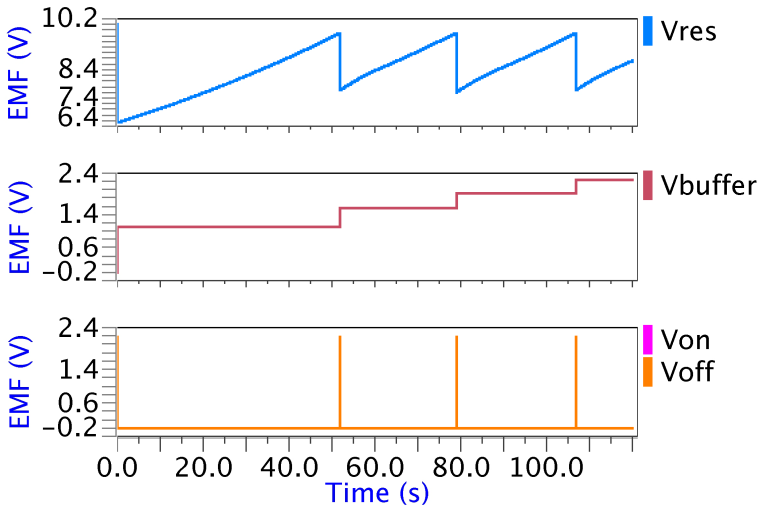
Element	Average Power (nW)
Clock Generator	18.75
Hysteresis Comp	3.30
Delay	75
Gate Drivers	0.76
Level Shifter	0.24
Total	98.05

5.8 Load voltage Regulator LVR

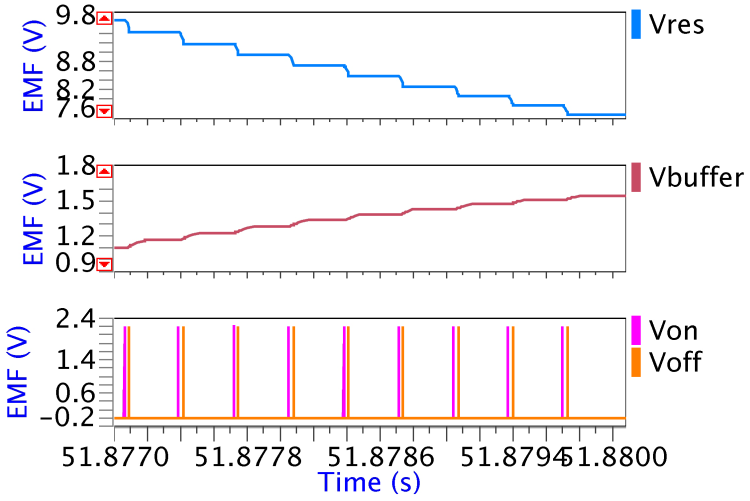
As described earlier in Chapter 3, the load is periodically supplied by C_{buffer} with the load voltage regulator block (LVR) managing this process. First, the LVR controller senses a divided voltage of V_{buffer} using a second comparator (COMP2) as shown in Figure 5.15. Second, the output of COMP2 controls a low voltage switch SW_{load} connecting the load when sufficient energy is accumulated on C_{buffer} and disconnected when C_{buffer} voltage falls below a certain voltage. Thus maintaining V_{buffer} low voltage between $V_{\text{buffer}_{\text{U}}}$ and V_{buffer_L}.

The LVR uses an off-chip resistive voltage divider allowing a degree of freedom to shift the regulation interval for V_{buffer} when needed by changing the division factor. The buffer voltage V_{buffer} is then regulated through using a hysteresis comparator COMP2 similar to CCR comparator.

The voltage divider was chosen with a ratio of (30G/10G Ω). The transistor sizing of COMP2 is summarised in Table 5.7. The switch SW_{load} is a low voltage pmos switch with an aspect ratio of $\frac{1000\mu m}{10\mu m}$. A full transistor level simulation was conducted including the CCR an the LVR. The V_{buffer} is $2V < V_{\text{buffer}} < 2.3V$ by allowing the



(a)



(b)

Figure 5.14: LI energy transfer in (a)120s (b)zoom in interval of $51.877s < t < 51.88s$.

discharge of C_{buffer} into a resistive load of 52Ω in 1ms thus supplying the harvester supply the load with energy of 3uJ shot.

Table 5.7: RS-Trigger comparator COMP2

Element	CMOS	Width (μm)	Length (μm)
INV1	MN	0.35	10
	MP	2	10
INV2	MN	0.5	10
	MP	2	10
INV3	MN	0.35	10
	MP	0.35	10

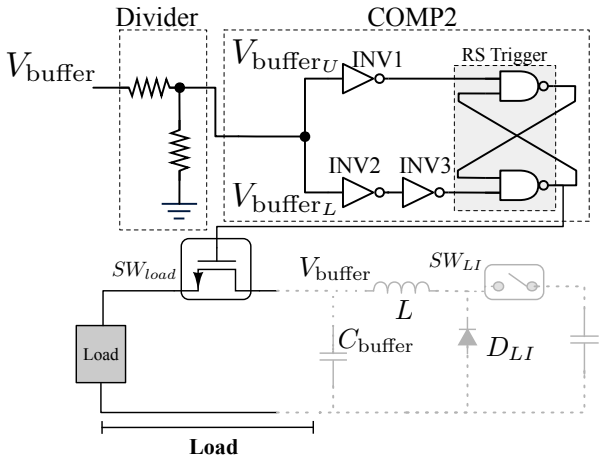


Figure 5.15: Load voltage regulator

5.9 Autonomy of second implementation

In Chapter 3 a multiple energy-shot transfer was proposed to handle high inductor's current when regulating the harvester voltage, see section 3.6, yet the system autonomy was not examined. Thanks to the minimised power consumption of CCR controller and LVR we obtained in the second design, the interface circuit can now be self-powered with the energy provided by the conditioning circuit and accumulated on the buffer capacitor. This buffer capacitor should eventually be the supply source for the LI controllers in future implementations. This section presents a three step investigation of an autonomous operation of the circuit:

– First step: We examen the system autonomously through supplying the CCR and LVR with a separated voltage source that is identical to the buffer capacitor. This power source receives no restoring energy and is allowed to drain its energy driving the CCR and LVR controllers for a fixed duration. The energy consumed by this source is examined at the end of the duration to determine the amount of energy necessary to safely drive the LI.

– Second step: The energy extracted from the reservoir and redistributed in the system (into C_{buffer}, CCR, LVR and the load) is examined in details.

5.9.1 Autonomous energy management system setup

To illustrate that the improved energy management system is capable of running from a pre-charged state a pre-charged capacitor was used to supply the CCR controller, cf. Figure 5.16. The system is allowed to run for a 1ms draining that supply. For this demonstration the V_{buffer} is regulated to be within 1.6V and 1.8V, while the V_{res} is regulated to be within 15.5V and 17.5V. Since the supply for CCR and the LVR is separated from C_{buffer}, the energy intake is accelerated to decrease simulation run time.

Figure 5.17 shows the result simulation of the system showing that V_{buffer} was initially discharged while the V_{res} initially charged to $17V$. As the energy accumulates

on the reservoir capacitor by the CC, V_{res} increases to reach $17.5V$. When this upper limit is reached the energy extraction process begins, and part of the charges are removed from C_{res} into C_{buffer}. Since the charge removal rate is much higher than the charges replenished by the CC, the voltage on C_{res} drops. When the lower threshold for V_{res} is reached, the transfer process is stopped, allowing the energy harvesting process - through the CC - to be resumed. This process of accumulation of energy and extraction is repeated. The energy is accumulated on the buffer capacitor until it reaches $1.8V$. When this upper limit is reached a load is connected and is powered by both the CC and the buffer capacitor. The load is allowed to be connected until it drop the buffer voltage to $1.6V$, then it is disconnected. The discharged buffer voltages was charged to $1.8V$ in two successive transfers.

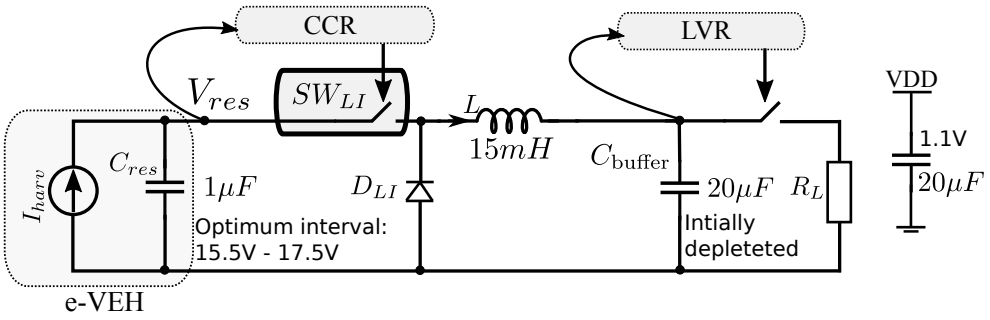


Figure 5.16: Schematic of first step simulation

Afterwards, the load is connect 7 successive times. The VDD powering the energy extraction controller and load regulator dropped from $1.1V$ to $1.096V$ through $1s$ which corresponds to 87nJ. To this figure, we need to add the energy consumed by the clock generator (which, in this simulation, was substitute by its behavioural model for reduction of the simulation time). As said in section 5.7, the clock generator consumes for 1 second of operation corresponds to 18.75nJ. So, the overall energy consumed during 1 second of operation is 105.75nJ, and the average power is $\approx 105nW$. This is far less than typical power provided by conditioning circuit, which is of order of 1μW.

Next, the output voltage voltage was adjusted to a narrower thresholds (here it is set between 1.6V and 1.7V) where this narrower thresholds will be required for the proposed future work of a self-power LI. This will allow a stabilised supply source for the CCR and LVR controller.

Moreover, to present the system versatility we changed modified slightly the CCR comparator thresholds. In this second simulated results the thresholds was raised to higher level where V_{res} is now maintained between $19V < V_{res} < 15V$ along with a a lower input energy flux of $1.8\mu W$, to show the system versatility when modified optimum interval is needed. The behaviour of the system is shown in Figure 5.18.

It must be highlighted that the LVR process is independent from the CCR process, meaning that the load can be connected as V_{res} being regulated. In this second simulation the load was connected twice while CCR is turned on as shown in Figure5.18.

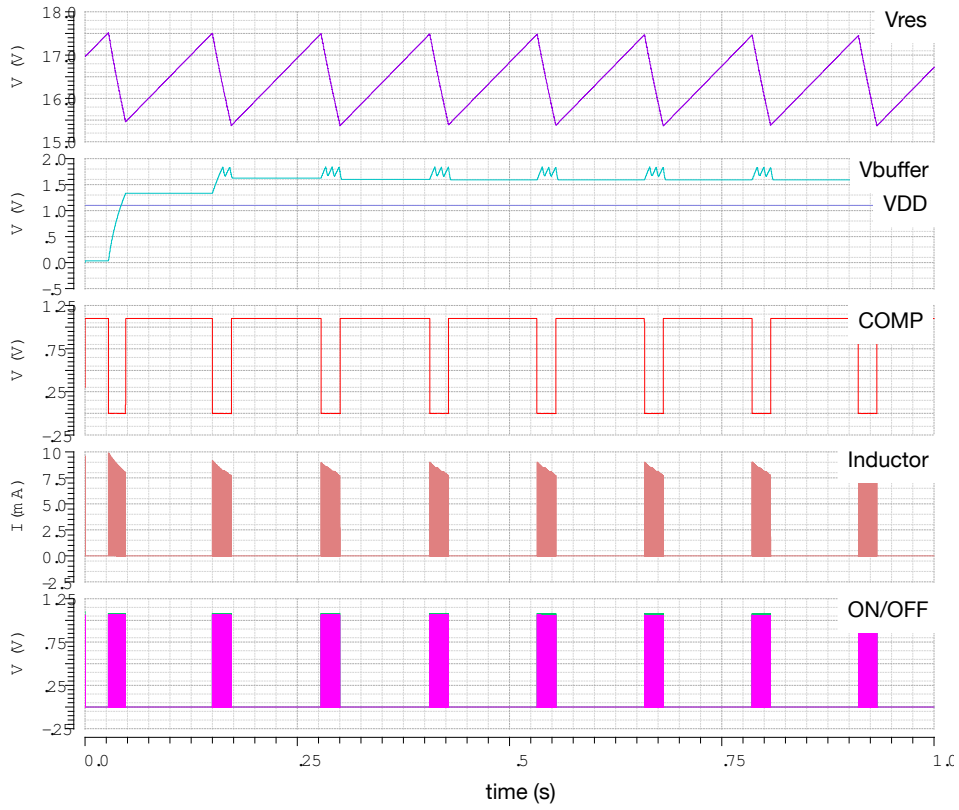


Figure 5.17: Simulation results showing V_{res}, V_{buffer}, COMP, I_L and ON/OFF commands

5.9.2 Connection between on-chip and off-chip components of the load interface

The designed load interface contains off-chip and on-chip blocks. The only off-chip blocks are the inductor, the freewheeling diode, the buffer capacitor and the resistances of the divider used in CCR. The connection between on-chip and off-chip components is achieved with use of pads. These pads are provides with AMS $0.35\mu m$ technology design tool kit. For our design we used the high voltage pads - APRIOP_HV - as can be seen in Figure 5.19. This section presents the simulated results of the system modelled the connecting pads. The design schematic can be found in Appendix C. Similar design conditions are used as in the previous section first simulation [1].

The simulation results are shown in Figures 5.20, 5.21,5.22. They show the energy extraction process from C_{res} into C_{buffer} maintaining V_{res} within a predefined optimum interval as shown in Figure 5.20a. The buffer capacitor was initially depleted and was charged to its steady-state regulated interval after two energy extraction (from t=0s to t=2s), cf. Figure 5.20b. When enough energy is accumulated on C_{buffer} its voltage is then regulated through connecting a load - 1kΩ - periodically (at $t \approx 2s, 3s, 4s$), cf Figure 5.20c. The inductor current is kept constrained with a maximum current of 10mA as shown in Figure 5.20d.

[1] Only the input energy flux was slightly decreased

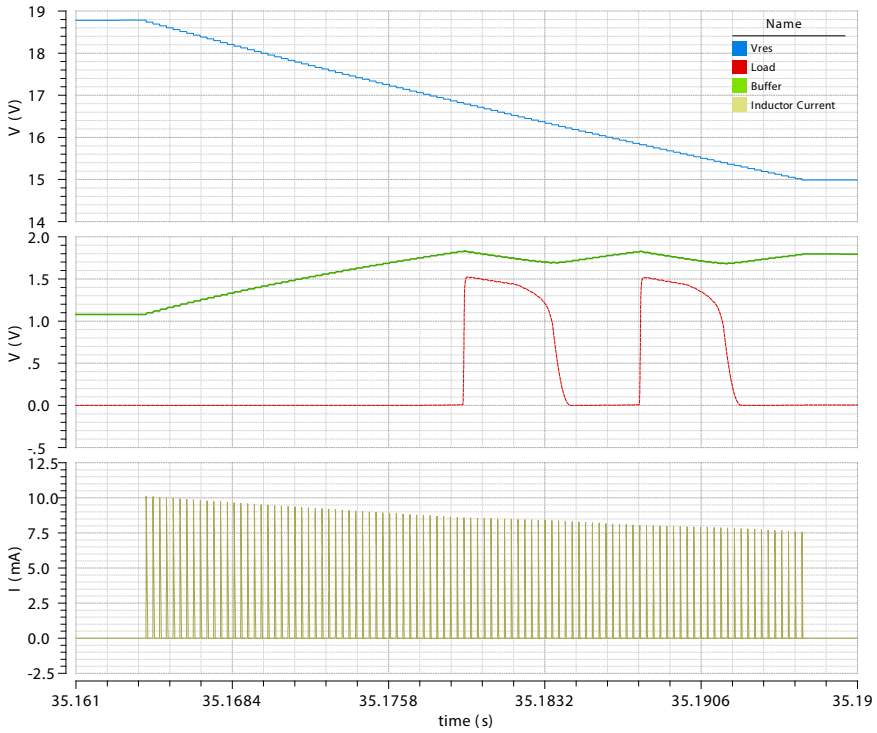


Figure 5.18: An energy shot transfer showing V_{res}, V_{buffer}, V_{load} and I_L

The CCR comparator output is shown in Figure 5.21a which designate an energy extraction interval to initiate. As can be seen in Figure 5.21b, a zoomed-in of on energy extraction interval is shown. The energy extract from C_{res} into C_{buffer} from 17.7V to 15.7V takes 18ms and is done through 56 shots with each lasting 320μs. This slightly shifted thresholds are due to using the pad. During the energy extraction from C_{res} into C_{buffer} the voltage V_{buffer} increases and is regulated separately from V_{res} as shown in Figure 5.21c. The 1kΩ load voltage is shown in Figure 5.21d while a zoomed-in of the inductor current I_L is shown in Figure 5.22a. The safe-gated clock is shown in Figure 5.22b and 5.22c.

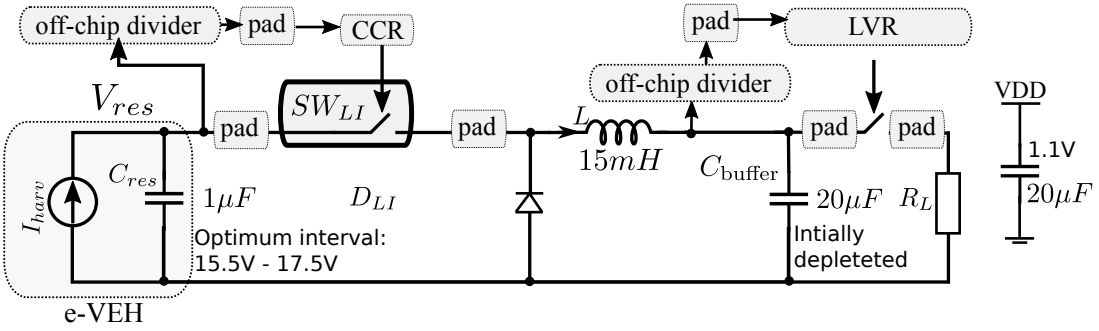


Figure 5.19: Schematic of step simulation with pads

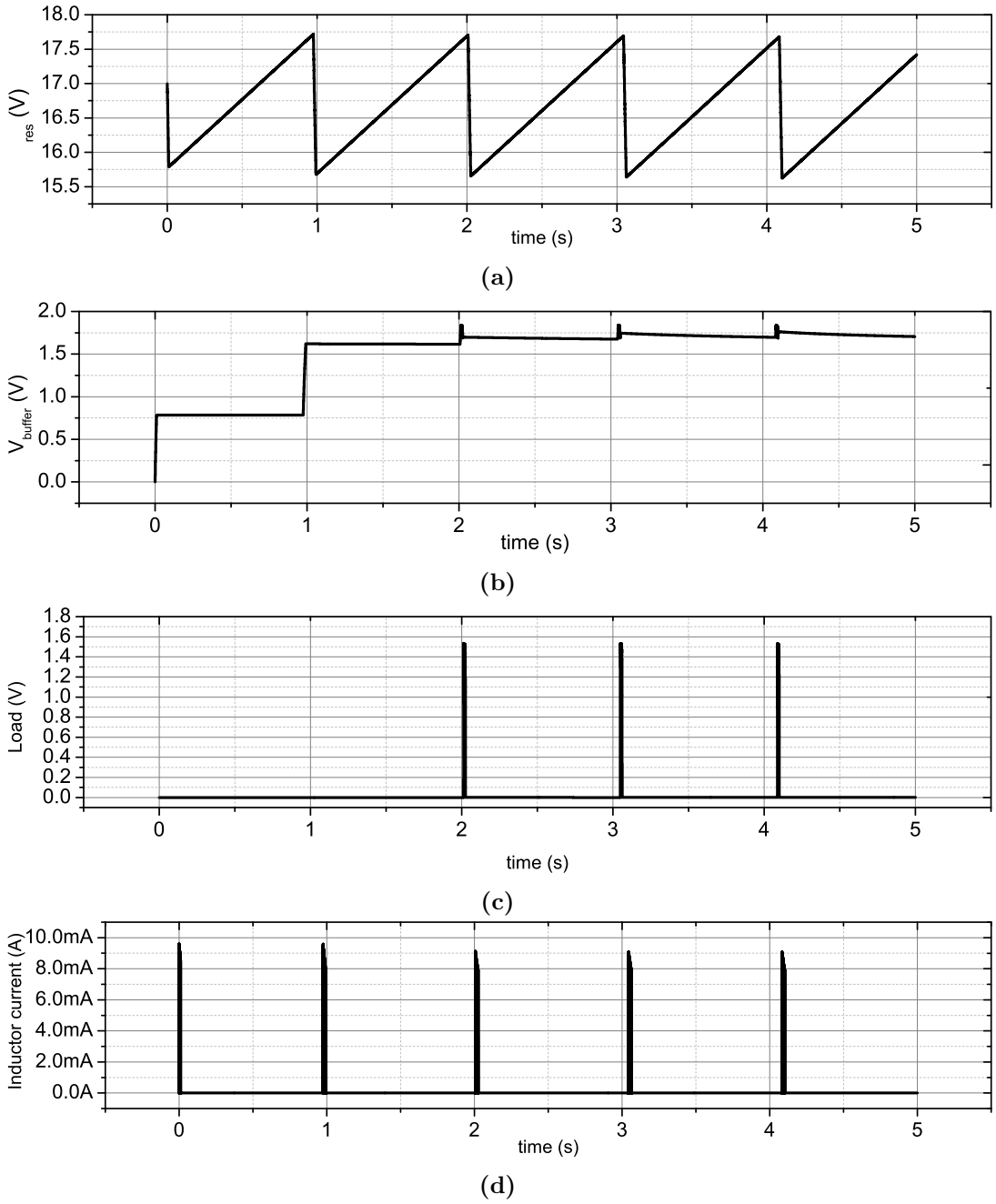


Figure 5.20: Simulations with Pads - part 1 , (a) Reservoir capacitor voltage V_{res} (b) Buffer capacitor voltage V_{buffer} (c) Load resistance voltage (d) LI inductor current

5.9.3 Discussions

This section presents the results obtained of the final simulation results presented in the pervious section. With the energy extracted from C_{res} is bumped into both C_{buffer} and the load, the steady-state energy extraction phase is analysed. Given that all the blocks of LI receives a portion of this energy, each element was examined and the

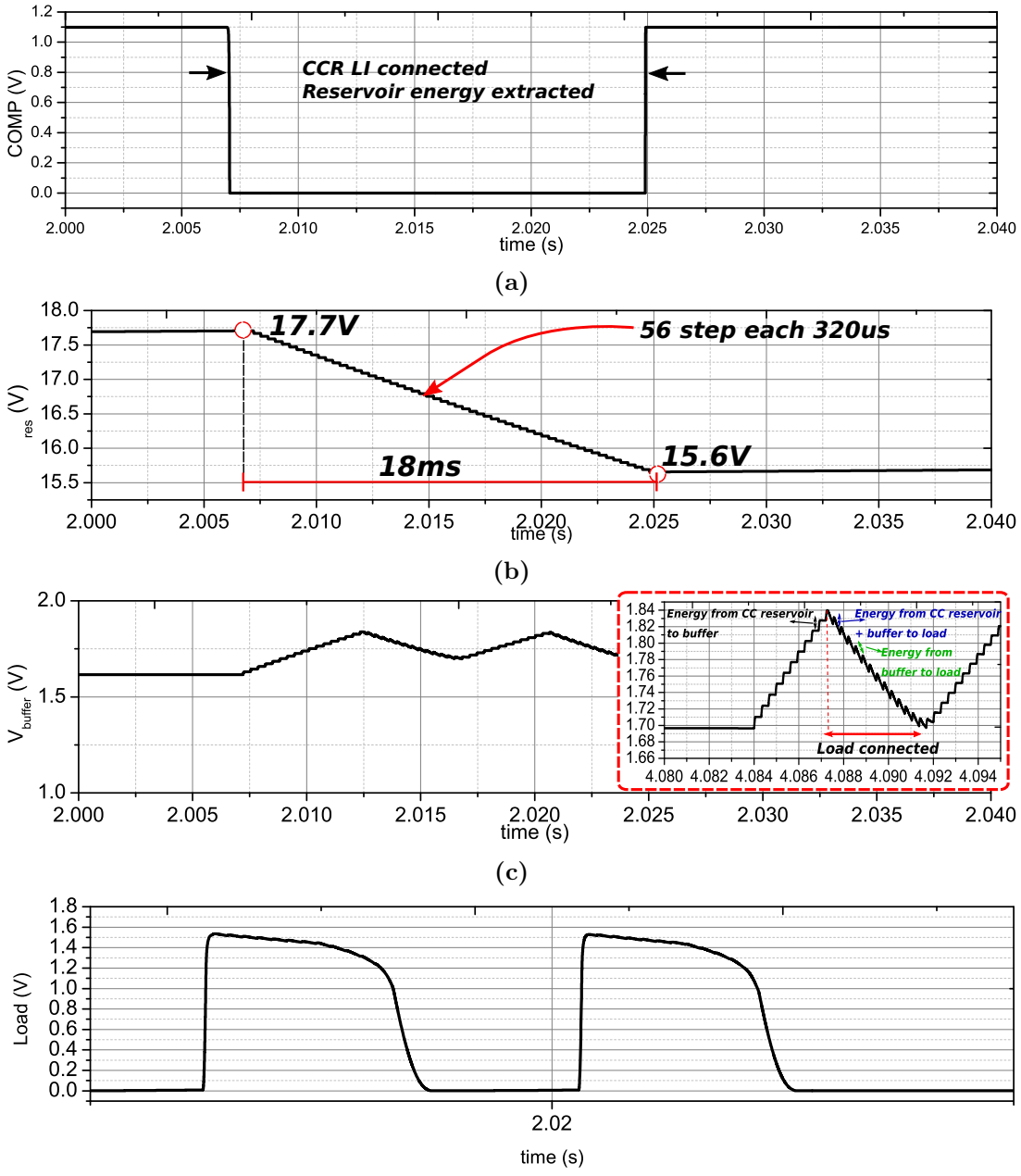


Figure 5.21: Simulations with Pads - part 2 (a) CCR Comparator output at 2.s to 2.04s (b) V_{res} at 2s to 2.04s (c) V_{buffer} at 2s to 2.04s (d) Load resistance voltage at 2.01s to 2.35s

energy they receive in *an energy transfer* is calculated.

The energy of a transfer (at time t=0.97s to t=1s) is calculated as shown in Figure 5.24. The reservoir capacitor voltage V_{res} drops from 17.7V to 15.6V which corresponds to 33.2μJ while the energy received by the buffer capacitor is 20.1μJ. These results shows that the transfer efficiency of almost 60% at this transient state. Most of the loses are due to the diode.

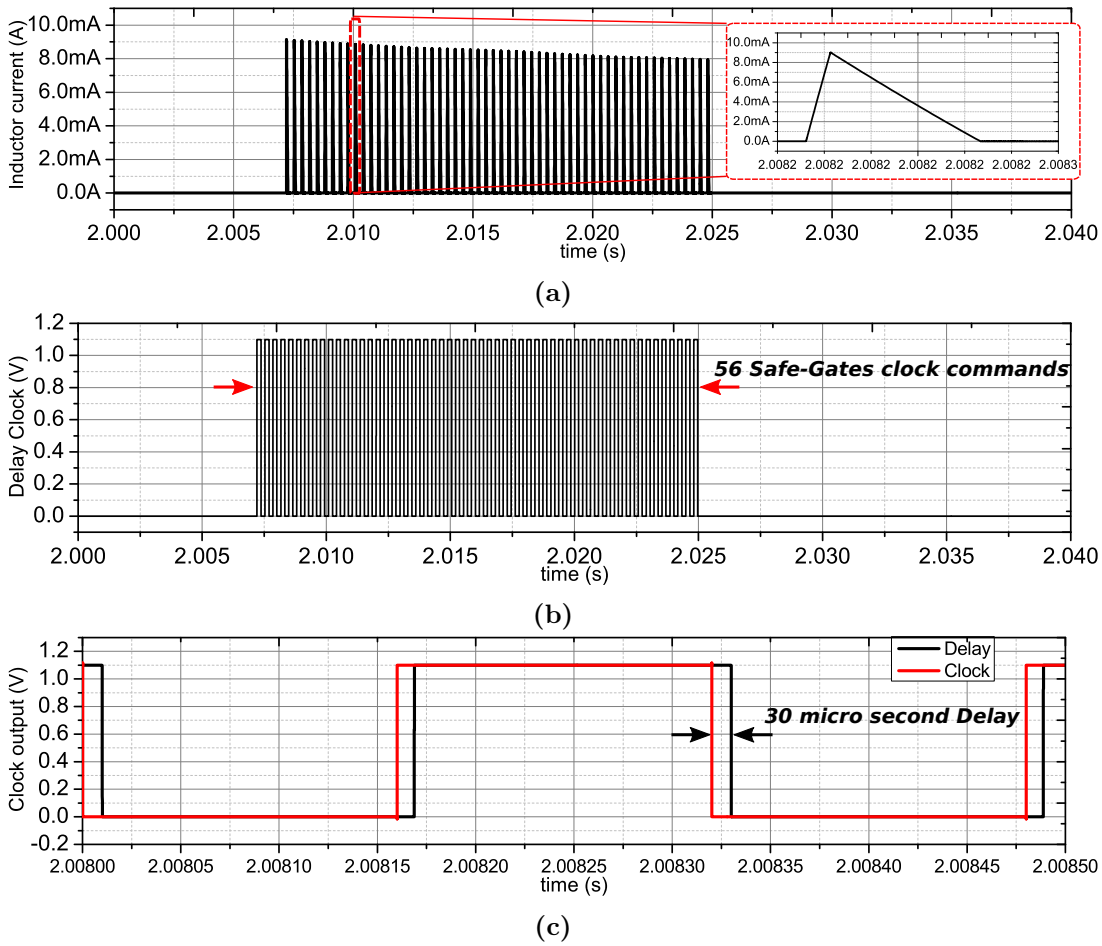


Figure 5.22: Simulations with Pads - Part 3 (a) Inductor current at 2.s to 2.04s (b) Safe Gated delayed clock at 2s to 2.04s (c)Delayed clock at 2.008s to 2.0085s

Table 5.8: CCR comparator consumed energy per transfer

Transfer stars	Transfer Ends	Energy consumed per transfer
0.97s	1s	90.29pJ
2s	2.03s	101.5pJ
3.04s	3.07s	88.15pJ
4.08s	4.11s	84.27pJ

The "freewheeling" diode D_{LI} losses become more significant when operating at low voltage (1.1V) since each energy transfer an amount of energy is lost in the forward biasing the diode ($\Delta W_{diode} = \Delta q \cdot V_D$, where q is the charges passing through the diode). This can be in future LI implementations by replacing the freewheeling diode with a synchronised switch at the expense of increased system complexity [80]. For the analysed energy transfer (at time t=0.97s to t=1s) the diode losses accounts for 10μJ which is 33%. These diode losses are the highest since they occur at the transient stage - where C_{buffer} is still charging to its steady state value.

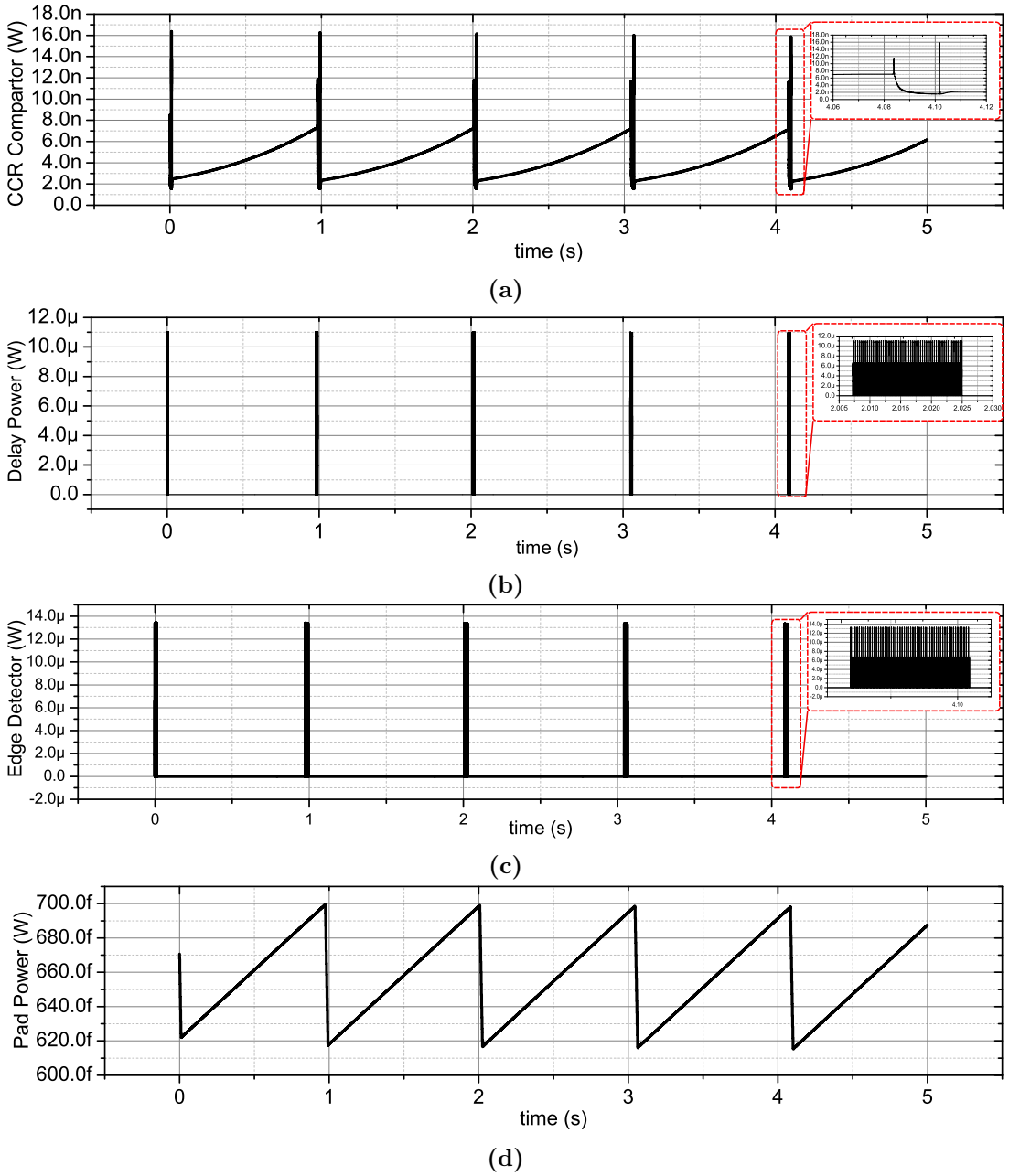


Figure 5.23: Instantaneous power consumption of (a) CCR comparator (b) time delay block (c) edge detector block (d) CCR controller pad

The energy consumption of the CCR comparator can be calculated with average energy consumption per of 91pJ for one V_{res} regulation - from $V_{res} = 17.7V$ to $V_{res} = 15.7$ as can be seen in Table 5.8.

The instantaneous power consumption of the highest power consuming blocks - CCR comparator, time delay element, the edge detector block and the CCR controller pad - are shown in Figures 5.23a, 5.23b, 5.23c and 5.23d respectively.

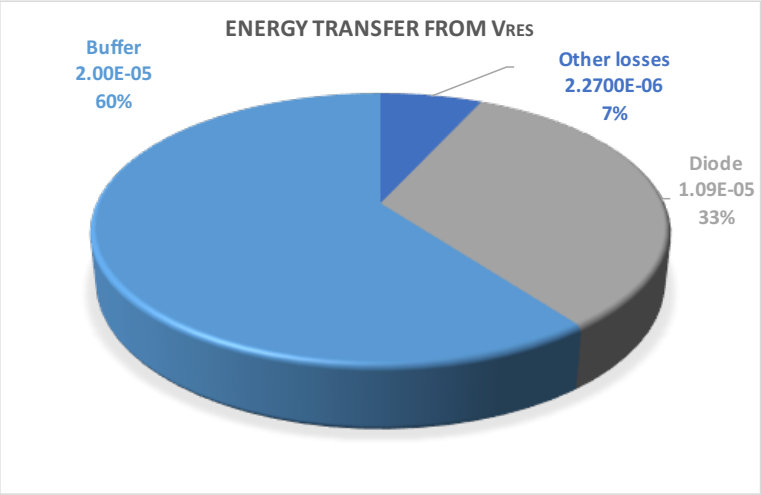


Figure 5.24: Diagram showing each block received energy precentage during an energy transfer at t=0.97s to t=1s where the total energy given by V_{res} is 33.2μJ.

5.10 Summary

In this chapter we presented an improved implementation of the LI controller as well as load voltage regulator block. The system was examined in terms of power consumption to insure an overall power consumption for the LI controller to be less than $1\mu W$. All the controlling blocks, including the CCR and LVR controllers - consume less than this budget energy leaving enough energy to periodically power a load. For the proposed LI we demonstrated as system the is capable of:

(1) transferring part of the reservoir capacitor (C_{res}) energy towards a buffer capacitor (C_{buffer}).

(2) ensuring V_{res} is maintained within its optimum. This is however challenging since V_{res} optimum interval can be as high as 30V for some capacitive transducers, whereas the load buffer voltage is 1-2V.

(3) Multiple energy-shot transfer was introduce to for the CC energy extraction to avoid high inductor current. This allows a transfer with lower resistive loses.

(4) The average power consumption of the active blocks load interface (excluding losses in the switches during the energy transfer) is estimated to be 105 nW in the steady-state mode. When the block is inactive (e.g., when the input energy flow is weak and the comparator doesn't order transfers), only the comparator and the clock consume power. This idle power is estimated to be less than 30 nW (less then 10 nW for the comparator, cf. Figure. 5.23a and 18nW for the clock). Such a low energy consumption allows the circuit to operate even when the input energy flow is few hundreds of nanowatts.

(5) A buffer low voltage regulation through periodically connecting to the load when enough energy is accumulated on C_{buffer}.

(6) An end-to-end efficiency of 60%, thanks to the multiple energy-shot technique, that can be improved by replacing flyback diode with an active switch.

Chapter 6

Summary, conclusions and perspectives

Contents

In this chapter we summarise the work presented in this manuscript. The main contribution of this work is discussed and perspectives for future work are listed.

6.1 Conclusions

Electrostatic energy harvesting is a challenging research domain that requires an interdisciplinarian knowledge. It raises many challenges such due to its particular characteristics. This characteristics includes a relatively high voltage and low output power which eventually requires a mixed of a high voltage/low power design to take full advantage of the electrostatic harvester.

In the last decade, electrostatic energy harvesting has gained more attention and has just started to pick up peace with other energy harvesting techniques such as piezoelectric energy harvesting. Unlike its counter part, electrostatic energy harvesting is still not mature enough to compete with other transduction methods such as piezoelectric where the design stream flow is already well defined [81]. However, with the recent trend of power electronics shifting towards ultra low power consumption along substantial development of electrostatic energy harvesters and new conditioning circuits - such as series-parallel charge pumps it is expected that in the next three to five years the capacitive transduction will be widely adopted for applications that requires tens micro watts of power [82].

In this work we demonstrated a full e-VEH load interface for rectangular QV-cycles CC which to our knowledge, was never been addressed before. For our implementation we adopted the series-parallel charge pump which allowed to self-increase of the internal voltage of the CC from relatively low voltage [34]. Afterwards, we proposed an intermediate stage permitted the regulation of the CC internal voltage keeping it from saturation and maintain it within it optimum interval range [83]. This was complemented with an added stage of low voltage regulation for the load [83]. A focus on low power average consumption for the load interface blocks was taken into account to reduce it to less than 100nW [84]. With these implementations it is obvious that a self-power and self-regulating interface for any rectangular QV cycle CC is possible.

The focus of this work is towards implementing a load interface controller that allows to maximise the harvested energy. Thus an adoption of different mixed signal - high voltage and low power - techniques is needed for the proposed custom tailored controller. Each of the fundamental blocks was build in AMS 0.35μm technology including an ultra low power clock, hysteresis comparator, high-voltage level shifter and a power switch. The power cost of the controlling is less than 100 nW in average, and the efficiency of the power transfer from the conditioning circuit to the load voltage low is 60 %. The last figure can be improved by implementing freewheeling with an active zero-threshold diode. Such performances allows the system to operate with input power levels as low as few hundreds of nanowatts.

The biggest challenge was to implement a low power hysteresis comparator and adjust its hysteresis gap to the CC optimum interval. To achieve such goal we incorporated two comparators for each of the proposed design.

Another challenge was to generate a precisely defined switching command using a single clock generator that can be used to trigger the LI and allowing multiple energy-shot transfer to take place. This was achieved by using a time delay and separating the on and off command generation for the switch.

As mentioned earlier, the design flow of electrostatic energy harvester has not been fully standardised, yet some key features can be examined if the overall system performance is to be compared to similar design approaches. In Table 6.1, we summarises these key features of our design and compare it to two designs developed at imec in 2013 and 2015.

For our design we used AMS 0.35μm technology while the other mentioned work TSMC 0.25 μm BCD was used. In the two implementation in [70] and [71], a Maximum Power Point Tracking algorithm for matching the equivalent source resistance of harvester and AC-DC converter were used. This replaces the series-parallel charge pump in our design. In [63] The input energy range was assumed to be significantly higher than in our design with ranges between tens of micro watts up to 1mW. The reported end-to-end efficiency was higher than our proposed design, yet that can be improved by reducing the losses of the flyback diode.

A few challenges however are still need to be address to achieve a complete system. These are discussed in the rest of this chapter.

Table 6.1: Comparison with similar work

Element	This work	imec 2013 [70]	imec 2015 [71]
CMOS Process	$0.35\mu m$ AMS	$0.25\mu m$ BCD	$0.25\mu m$ BCD
Input Power	$1 - 5\mu W$	$25 - 1600\mu W$	$1\mu W - 1mW$
Input Voltage	5-50V	5-60V	5-60V
Output Voltage	1.6-2.6 V	2-5 V	0-5V
Inductor Current	15mH	10mH	n/a
Average static current	$< 90nA$	$1.3\mu A$	n/a
Control Power	100nW	5000nW	500nW
Battery-less	Yes	No	Yes
Reported end-to-end efficiency	74%	89 %	85%

6.2 Perspectives and Future work

In order to complete the e-VEH system, a few points needs to be addressed. These includes a start-up circuit, reducing the diode losses and the integration of the CC.

6.2.1 Start-up circuit

In the proposed design, it was assumed a supply source is available to power the LI controller from the start of its operation. However, the ultimate goal is to supply the LI controller through the harvested energy without the need of any external or pre-charged supply source. This will require a startup circuit enabling a cold start of the controller [85]. One proposed architecture proposed by Stenzione et al. [71] was to permit a direct charging of the supply source before enabling the LI controller.

6.2.2 Diode losses

The diode losses is a major issue when it comes to energy transfer efficiency. This energy consuming element is dictated by the architecture of the dc-dc buck converter load interface not by the LI controller design. To prevent the LI diode losses, an active diode or an synchronised switch should be implemented. This however is not a straight forward problem as it would require current sensing of a high voltage node. This topic is the ongoing research of our team.

6.2.3 Integration of CC

The ultimate goal for a smart e-VEH is to integrate all of its components on-chip. This is yet challenging as the series-parallel charge-pumps utilises a multiple of diodes and relatively high capacitance ratios. With better understanding of how these CC behave such as the work presented in [34, 68] and thanks to new cmos technologies developing an integrable version of the CC can be possible. This issue is the currently being investigate by our team.

6.2.4 Self-adjustability threshold

In the presented work, we proposed an externally adjustable threshold controls for the LI comparators. For the future work, these thresholds should be able to dynamically change as the operating conditions of the CC change with the external vibration, i.e MPPT. One way to achieve such self-adjustability is to introduce a calibration phase where the energy harvesting process is withheld temporary for few seconds and new thresholds values are refreshed to new values if necessary. A similar calibration phase was proposed within our team in [21] in the frame of flyback mechanism for charge-pump CC. This work can be adopted for the LI proposed for this work, yet few challenges needs to be overcome including power consumption and proper command generation that can be used to drive the ultra low power comparators proposed in this PhD work.

6.3 Publications

1. **M. Bedier**,Armine Karami, Dimitri Galayko, Philippe Basset *"Autonomous Energy Management Interface for Electrostatic Series-Parallel Charge Pump Vibrational Energy Harvester"*, 15th IEEE International New Circuits and Systems Conference (NEWCAS), 2017.

2. Armine Karami, **M. Bedier**, Dimitri Galayko, Philippe Basset *"Analysis and Comparison of Charge-Pump Conditioning Circuits for Capacitive Electromechanical Energy Conversion"*, IEEE International Symposium on Circuits and Systems (ISCAS), 2017.

3. **M. Bedier** and Dimitri Galayko *"A Smart Energy Extraction Interface for Electrostatic Vibrational Energy Harvester"*, 23rd IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2016.

4. **M. Bedier** , P. Basset & D. Galayko *" A Smart Load Interface and Voltage Regulator for Electrostatic Vibration Energy Harvester"* PowerMEMS **2016**, Paris France, Journal of Physics: Conference Series - PowerMEMS, pp. 012105, Vol 773, 2016.

5. **M. Bedier** and Dimitri Galayko *"Low Power Multiple Energy-shot Load Interface for Electrostatic Vibrational Energy Harvesters"*PwrSoc **2016** , Madrid Spain, Conference paper.

6. **M. Bedier** and Dimitri Galayko *"A 100nW Power Overhead Load Interface for Electrostatic Vibrational Energy Harvester with a High Biasing Voltage"*, EuroSensors **2016** Procedia Engineering, Volume 168, 2016, Pages 1693-1697, ISSN 1877-7058, http://dx.doi.org/10 .1016/j.proeng.2016.11.492.

7. **M. Bedier** and Dimitri Galayko *"Multiple Energy-Shot Load Interface For Electrostatic Vibrational Energy Harvesters"* 2016 14th IEEE International New Circuits and Systems Conference (NEWCAS), Vancouver, BC, 2016, pp. 1-4. doi: 10.1109 / NEWCAS.2016. 7604771

8. **M. Bedier** and Dimitri Galayko *"Low Power Load Interface For Vibrational Energy MEMS harvesters"*, JNRSE **2016** , Bordeaux Conference Paper.

Appendix A

Analysis of Current and Energy for dc-dc buck load interface

Defining the governing equations, assuming voltage and current directions as show in Chapter 1 where,

$$i_L(t) = -i_{res}(t) \tag{A.1}$$

$$i_L(t) = i_{load}(t) \tag{A.2}$$

$$i_{load}(t) = \frac{dQ_{load}(t)}{dt} \tag{A.3}$$

$$i_{res}(t) = \frac{dQ_{res}(t)}{dt} \tag{A.4}$$

Differentiating Eq.3.5 with respect of time,

$$\therefore \frac{d}{dt}\left\{\frac{Q_{res}(t)}{C_{res}} - \frac{Q_{load}(t)}{C_{load}} - Li'_L(t)\right\} = 0 \tag{A.5}$$

thus,

$$\frac{1}{C_{res}}\frac{dQ_{res}(t)}{dt} - \frac{1}{C_{load}}\frac{dQ_{load}(t)}{dt} - Li''_L(t) = 0 \tag{A.6}$$

Using the governing equation of Eq.A.1 and Eq.A.4,

$$i_L(t) = -i_{res}(t) = -\frac{dQ_{res}(t)}{dt} \tag{A.7}$$

which follows that,

$$i''_L(t) = -Q'''_{res}(t) \tag{A.8}$$

Substituting in Eq.A.5

$$\frac{1}{C_{res}}\frac{dQ_{res}(t)}{dt} - \frac{1}{C_{load}}\frac{dQ_{load}(t)}{dt} + LQ'''_{res}(t) = 0 \tag{A.9}$$

Also, expressing $Q_{load}(t)$ in terms of $Q_{res}(t)$ using Eq.A.1, Eq.A.2 and Eq.A.3 as follows,

$$\frac{dQ_{load}(t)}{dt} = i_{load}(t) = -i_{res}(t) = -\frac{dQ_{res}(t)}{dt} \tag{A.10}$$

Then,

$$\frac{1}{C_{res}}\frac{dQ_{res}(t)}{dt} + \frac{1}{C_{load}}\frac{dQ_{res}(t)}{dt} + LQ'''_{res}(t) = 0 \tag{A.11}$$

Re-arranging,

$$Q'_{res}(t)\left(\frac{1}{C_{res}} + \frac{1}{C_{load}}\right) + LQ'''_{res}(t) = 0 \tag{A.12}$$

Let,

$$\frac{1}{C_{eq}} = \left(\frac{1}{C_{res}} + \frac{1}{C_{load}}\right) \tag{A.13}$$

Then,

$$Q'''_{res}(t) + Q'_{res}(t)\frac{1}{LC_{eq}} = 0 \tag{A.14}$$

Solving for $Q_{res}(t)$, Assume $Q_{res}(t) =$

Let,

$$Q_{res}(t) = e^{-\lambda t} \tag{A.15}$$

$$\therefore Q'_{res}(t) = -\lambda e^{-\lambda t} \tag{A.16}$$

$$\therefore Q''_{res}(t) = \lambda^2 e^{-\lambda t} \tag{A.17}$$

$$\therefore Q'''_{res}(t) = -\lambda^3 e^{-\lambda t} \tag{A.18}$$

Substituting in Eq.A.14,

$$-\lambda^3 e^{-\lambda t} - \lambda e^{-\lambda t}\frac{1}{LC_{eq}} = 0 \tag{A.19}$$

Substituting in Eq.A.14,

$$\lambda^3 + \lambda\frac{1}{LC_{eq}} = 0 \tag{A.20}$$

then,

$$\lambda_0 = 0 \tag{A.21}$$

$$\lambda_{1,2} = \frac{\pm i}{\sqrt{LC_{eq}}} \tag{A.22}$$

Thus,

$$Q_{res}(t) = Ae^{\lambda_0 t} + Be^{\lambda_1 t} + Ce^{\lambda_2 t} \tag{A.23}$$

Which is,

$$Q_{res}(t) = A + Be^{\lambda_1 t} + Ce^{\lambda_2 t} \tag{A.24}$$

Using Eurler's expression, where,

$$e^{iat} = cos(at) + isin(at) \tag{A.25}$$

$$e^{-iat} = cos(at) - isin(at) \tag{A.26}$$

Thus,

$$Q_{res}(t) = A + B'cos(\omega t) + iC'sin(\omega t) \tag{A.27}$$

where,

$$B' = B + C \tag{A.28}$$

$$C' = B - C \tag{A.29}$$

and,

$$\omega = \frac{1}{\sqrt{LC_{eq}}} \tag{A.30}$$

The first initial conditions for the load interface can be defined as follows:

$$i_L(t)|_{t=0} = 0 \tag{A.31}$$

From governing equations of Eq.A.1 and Eq.A.4,

$$i_L(t)|_{t=0} = -\frac{dQ_{res}(t)}{dt}\Big|_{t=0} = 0 \tag{A.32}$$

Substituting into Eq.A.27 where,

$$\frac{dQ_{res}(t)}{dt}\Big|_{t=0} = -\omega B' \sin(\omega t) + i\omega C' \cos(\omega t)|_{t=0} = 0 \tag{A.33}$$

Thus,

$$C' = 0$$

and Eq.A.27 reduces to,

$$Q_{res}(t) = A + B' cos(\omega t) \tag{A.34}$$

The second initial conditions for the load interface can be defined as follows,

$$Q_{res}(t)|_{t=0} = Q_{res_0} \tag{A.35}$$

Where, the suffix of Q_{res_0} defines the charge cycle number. Thus, Eq.A.34 can be expressed as follows,

$$Q_{res}(t)|_{t=0} = A + B' = Q_{res_0} \tag{A.36}$$

thus,

$$B' = Q_{res_0} - A \tag{A.37}$$

Substituting into Eq.A.34 then,

$$Q_{res}(t) = A + (Q_{res_0} - A) cos(\omega t) \tag{A.38}$$

which is,

$$Q_{res}(t) = A(1 - cos(\omega t)) + Q_{res_0} cos(\omega t) \tag{A.39}$$

The third initial condition for the load interface can be defined as follows,

$$V_L(t) = L\frac{di_L(t)}{dt} = L\frac{d^2Q_{res}(t)}{dt^2} \tag{A.40}$$

thus,

$$\frac{d^2Q_{res}(t)}{dt^2} = \frac{V_L(t)}{L} \tag{A.41}$$

However at $t = 0$

$$V_L(t)|_{t=0} = V_{res_0} - V_{Load_0} \tag{A.42}$$

then,

$$\left.\frac{d^2Q_{res}(t)}{dt^2}\right|_{t=0} = \frac{V_{res_0} - V_{Load_0}}{L} \tag{A.43}$$

From Eq.A.34 differentiating twice with respect of time,

$$\frac{d^2Q_{res}(t)}{dt^2} = -B'\omega^2 cos(\omega t) \tag{A.44}$$

Which wields,

$$\left.\frac{d^2Q_{res}(t)}{dt^2}\right|_{t=0} = -B'\omega^2 cos(\omega t)\Big|_{t=0} = -B'\omega^2 \tag{A.45}$$

Thus, from Eq.A.43,

$$\frac{1}{L}(V_{res_0} - V_{Load_0}) = -B'\omega^2 \tag{A.46}$$

Which reduces to,

$$B' = C_{eq}(V_{Load_0} - V_{res_0}) \tag{A.47}$$

From Eq.A.37 and Eq.A.47,

$$C_{eq}(V_{Load_0} - V_{res_0}) = Q_{res_0} - A \tag{A.48}$$

Re-arranging,

$$A = Q_{res_0} - C_{eq}(V_{Load_0} - V_{res_0}) \tag{A.49}$$

Substituting Eq.A.49 into Eq.A.39,

$$Q_{res}(t) = (Q_{res_0} - C_{eq}(V_{Load_0} - V_{res_0}))(1 - cos(\omega t)) + Q_{res_0}cos(\omega t) \tag{A.50}$$

Simplifying,

$$Q_{res}(t) = Q_{res_0} - C_{eq}(V_{Load_0} - V_{res_0})(1 - cos(\omega t)) \tag{A.51}$$

However,

$$i_L(t) = -i_{res}(t) = -\frac{dQ_{res}(t)}{dt} \tag{A.52}$$

Then,

$$i_L(t) = C_{eq}(V_{Load_0} - V_{res_0})\omega(sin(\omega t)) \tag{A.53}$$

$$i_L(t) = \sqrt{\frac{C_{eq}}{L}}(V_{Load_0} - V_{res_0})sin(\omega t) \tag{A.54}$$

Appendix B

Second implementation schematic

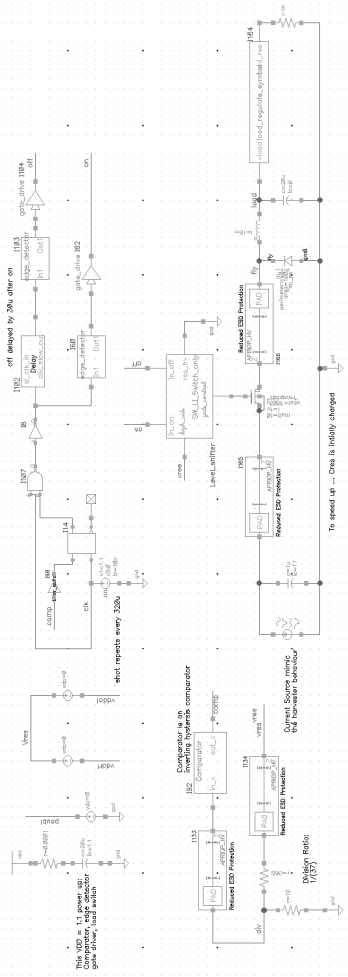


Figure B.1: Second implementation schematic overview

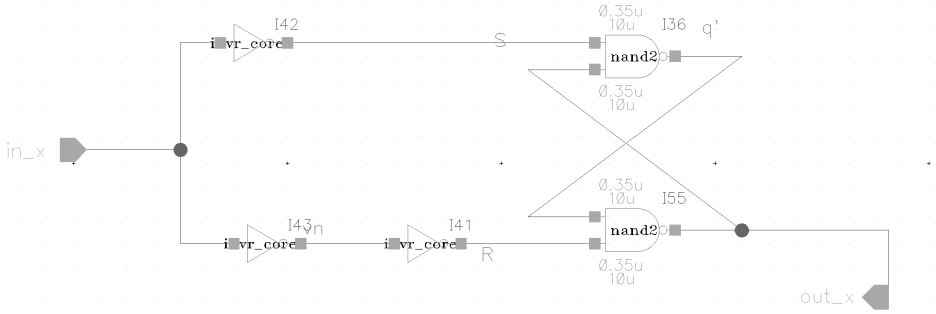


Figure B.2: Second implementation comparator

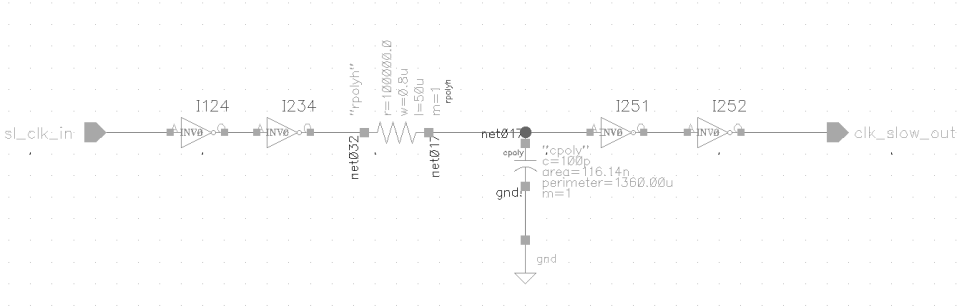


Figure B.3: Second implementation 30μs delay

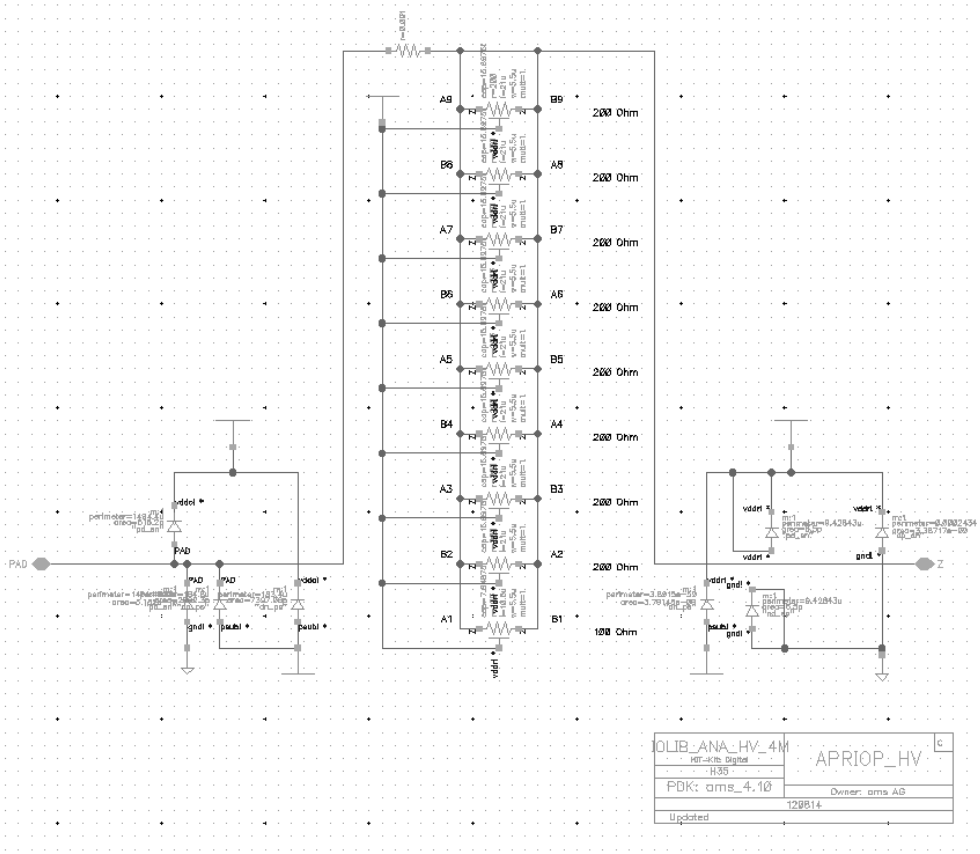


Figure B.4: Second implementation CCR pad

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