Power modules design and optimization for medium power of MMC inverters : high insulation voltage gate driver system and 3D packaging

Sokchea Am

Communauté
UNIVERSITÉ Grenoble Alpes

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Présentée par

Sokchea AM

Thèse dirigée par **Pierre LEFRANC** et
Co-encadrant par **David FREY**

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devant le jury composé de :

M. Bruno ALLARD
Professeur, Laboratoire Ampère, Lyon, Président
M. François COSTA
Professeur, Laboratoire SATIE, Cachan, Rapporteur
M. Nicolas GINOT
Professeur, Laboratoire IETR, Nantes, Rapporteur
M. Pierre LEFRANC
Maître de conférences, Laboratoire G2ELAB, Grenoble, Directeur de thèse
M. David FREY
Maître de conférences, Laboratoire G2ELAB, Grenoble, Co-encadrant
M. Jean-christophe CREBIER
Directeur de recherche CNRS, Laboratoire G2ELAB, Grenoble, Examinateur

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General Introduction

According to EIA (Energy Information Administration) in 2011, the 40% of the energy consumption worldwide are the electricity generation and its demand is expected to increase. As an evidence, an annual energy outlook 2015 with projections to 2040 of EIA shows that the total electricity generation increases by 24% from 2013 to 2040. This growth in demand is partly because of increase in number of digital devices, and hence, power electronic converters which must regulate power at almost any arbitrary voltage, current and frequency. The power electronic converters can be found through the electrical system as they enable efficient conversion for generation, storage and end-user applications. The applications of power electronic devices are for example: electric vehicles, electric aircrafts, electric ships or naval systems, motor drives, etc. Thus, increase the number of digital devices will also increase the demand of power electronic converters. Therefore, the effective design techniques (the design optimization) are required to achieve higher performance indices for power electronic converters, which include size, weight, efficiency, cost and reliability.

In this research, the author focuses on both a design optimization for a Medium-Voltage Modular Multilevel Converter (MV-MMC) use as a DC/AC or AC/DC converter and gate drivers systems for IGBT modules which are used in this kind of application. For example, the MMC converters are used in Medium-Voltage Direct Current (MVDC) electrical ship power systems. For such application, according to the IEEE document [IEE10], the DC bus voltage can be up to 35kV. Hence, gate drivers' systems for IGBT modules for MVDC-MMC applications are major concerns in terms of architectures and insulation voltage capabilities. Thus, this dissertation provides solutions to answer these problems. The study also includes the studies of a dielectric material which is used as insulation material. The results of experimental tests of a proposed dielectric material for different layers thicknesses to sustain different insulation voltage levels are also provided to clearly validate this study. Actually, a MMC converter composes of a number of converter cells connected in series. One cell (converter's sub-module) is classically composed of two IGBT modules. Based on the cell topology, a challenged gate driver's architecture for power semiconductor modules is proposed and compared to the classical one in terms of high and low galvanic insulation voltage levels' requirements, converter's cell size, etc.

This thesis dissertation is organized into three main chapters:

Chapter 1 presents the global optimization of Modular Multilevel Converter (MMCs) and the gate drivers' architectures for IGBT modules for a sub-module (SM) of this converter. First, the multilevel converter topologies (Neutral-point-clamped (NPC), Cascaded H-bridge (CHB) and Flying-capacitor (FC) structures) are presented and

[IEE10] IEEE recommended practice for 1kV to 35kV medium voltage DC power system on ships. DC Power syst. On Ships Working Group of IEEE Industry Applicat. Soc. Petroleum & Chemical Industry (IAS/PCI) Committee, IEEE Std. 1709-2010, 2010

compared to the MMC one for a MV application. As a result, a MMC structure is selected. Then, a generic virtual prototyping tool to optimize MMC converters is illustrated. The MMC modeling (control law, loss modeling, thermal modeling, etc.) are performed with MATLAB^{TM}/Simulink. Number of optimization variables and parameters are defined depending on the building components in the MMC converter. The objectives are to maximize the converter efficiency and to minimize the converter volume. This bi-objective problem is solved by the help of a genetic algorithm (GA) coded in MATLAB^{TM} software. To validate a generic virtual prototyping tool, some converter's specifications are proposed. Then, at the end of this chapter, gate drivers' architectures for IGBT modules for Medium-Voltage Modular Multilevel Converters (MV-MMCs) are presented. Furthermore, the requirements for a high galvanic insulation voltage level are also mentioned.

Chapter 2 presents a design methodology to optimize gate drivers for IGBT modules for high insulation voltage capabilities. At first, high galvanic insulation voltage technologies of an insulated pot core planar transformer are described. Moreover, the studies about the dielectric material to sustain the static insulation voltage are also provided. To clearly validate this material selection, several experimental tests of the proposed dielectric material were realized and compared to a printed-circuit-board (PCB) FR4 for exactly the same dimension. As a result, 1mm thickness of a selected dielectric material can achieve at least 40kV for a testing period of 2 hours.

In a second step, the optimization design for high galvanic insulation signal transmission function is presented. Descriptions of a proposed circuit and optimization variables, parameters, constraints are shown. An impulse signal circuit with a series resonance between a capacitor (C_1) and a primary side of a transformer and a parallel resonant at the secondary side is proposed. This circuit is supplied by a DC voltage V_{DC} = 15V. To generate the impulse signal, a fast N-MOSFET is placed in series at the primary side of the transformer. The optimization variables, parameters and constraints are composed by the electrical devices and transformer's geometry in the proposed circuit. After that, the optimization objectives (maximizing the output voltage $V_{out,signal}$ and minimizing the input current i_{mos}) are defined as a bi-objective optimization problem. With the help of a virtual prototyping tool based on the combination of a finite element software FEMM^{TM} (to optimize the geometry of a pot core transformer) and a transient electrical software LTSpice^{TM} (to simulate and to optimize the electrical circuit) in a genetic algorithm coded in MATLAB^{TM}, the bi-objective optimization problem is ended under Pareto fronts' results. As a result, numerous optimal Pareto fronts are obtained as a function of a pot core ferrite diameter (D_F = {7mm, 9mm and 14mm}) and an insulation layer (ep_I = {0.5mm to 3mm}). The post analyses of these results are performed till the suitable solution (for ep_I = 0.5mm and D_F = 9mm which achieves at least 20kV of insulation voltage level) for practical work is chosen.

The same optimization philosophy is also applied for a power transmission function's topology. The proposed topology for an insulated power transmission function for gate

drivers for IGBT module is a DC-DC full-bridge series-series (FBSS) resonant converter. The main optimization objective is to maximize the converter efficiency ($\eta_{con.}$). Then, with the help of a virtual prototyping tool, numerous optimal Pareto fronts' results are plotted as a function of the pot core diameter (D_F = {14mm, 18mm, and 22m}) and the insulation layer (ep_1 = {0.5mm to 3mm}). Finally, an optimal solution for ep_1 = 0.5mm and D_F = 14mm is selected for an experimental work. Then, at the end of this chapter, an intelligent IGBT gate driver to measure a sub-module voltage is also briefly presented.

Chapter 3 presents the conception and realization of an optimized sub-module (SM). The separated validations of a signal transmission and a power transmission function are first illustrated in the beginning of this chapter. After that, a single channel IGBT gate driver validation is presented. And at the end of this chapter, 3D aspects towards 3D-MMC are illustrated. Finally, the general conclusions and some perspectives for future works are provided and the end of this thesis dissertation.

Chapter 1:

Global Optimization of MMCs and Gate Drivers Architectures

This Chapter presents the pre-dimensioning design for Modular Multilevel Converters (MMCs) for Medium Voltage (ex. Medium Voltage Direct Current (MVDC)) applications by the help of a virtual prototyping tool. Fig. 1.1 illustrates the potential roles of multilevel converters in MVDC applications. These converters can be used to transfer the power to the MVDC buses from ac- and dc-sources. They can also be used to feed the (ac- and dc-) loads from main MVDC buses. For example, the article [Spi13] presents the utilization of the MMC as an inverter to drive a propulsion motor in MVDC electric ship application. The optimization consideration of this kind of converters/inverters over their internal control structure to optimize the oscillating components of circulating current is presented in the reference [Nik15]. The objective of this paper is to reduce the noise which perturbs the converter operation. Moreover, the reference [Arm16] proposes the optimization design of MMC converters for HVDC application. The optimization problem is solved by the help of optimization-based sub-module selections. The authors also present the converter losses related to the modulation and power cell selections. As a result, the converter total losses are reduced by 60% if the suitable modulation method and the cells are used. In this dissertation, to respond to various applications, the optimization over their performances (efficiency, volumes, cost, etc.) is proposed with the help of a virtual prototyping tool. Furthermore, the challenges of power semiconductors' gate drivers of power converter cell are also introduced.

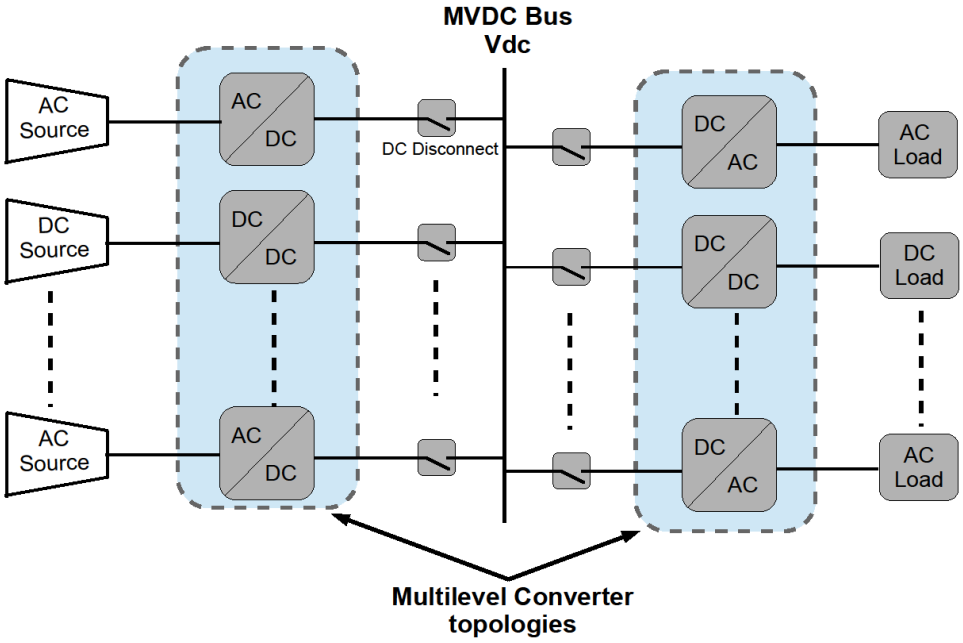


Fig. 1.1: Example of Medium Voltage Direct Current (MVDC) bus applications.

Before going deeply into the pre-dimensioning design for MMC converters, several multilevel converter topologies are studied and compared. Therefore, Section 1.1 introduces these multilevel converter topologies: such as neutral-point-clamped (NPCs) converters, flying-capacitor (FCs) converters, cascaded H-bridge (CHBs) converters, and modular multilevel converters (MMCs). The operations and controls of each structure are

provided based on their numerous pertinent publications. Then, the brief comparisons between them for MV applications are exposed until the MMC is selected.

Then, Section 1.2 details a generic virtual prototyping tool to optimize modular multilevel converters (MMCs). Firstly, a generic modeling of MMC is proposed to be adapted to various applications. After that, the optimization characteristics such as: variables, parameters, objectives, constraints, and procedure are defined. Then, with the help of an optimization tool (genetic algorithm (GA) coded in MATLAB^{TM}), the optimization problems are solved.

In Section 1.3, the challenge over gate drivers for MMC sub-modules are introduced. For safety and long production life reason, the insulation voltage level must be considered and developed. Then, to achieve the most efficient solution, gate drivers' topologies are presented and discussed.

1.1. Introduction to multilevel converters

As illustrated in Fig. 1.1, the multilevel converters or inverters are connected to the medium-voltage direct current (MVDC: where the DC bus voltage is up to 30kV) network. Today, it is hard to connect a single power semiconductor switch directly to a medium-voltage grid. For these reasons, beside the well-known two-level voltage source converter (2L-VSC: Fig. 1.2), a family of multilevel converters/inverters has emerged as the solution to work with higher voltage levels. Multilevel converters include an array of power semiconductors and capacitor voltage sources to generate stepped voltage waveforms.

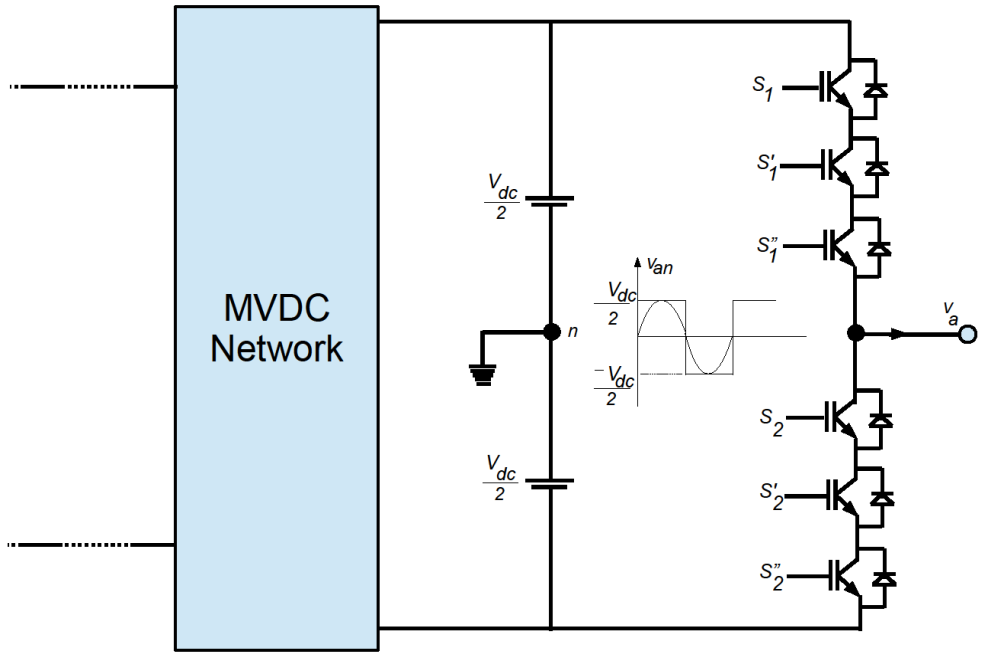


Fig. 1.2: Conventional two-level voltage source converter (2L-VSC) with three switches in series connection controlled with the same gating signal.

Four different topologies are proposed for multilevel converters/inverters: diode-clamped (neutral-point-clamped (NPC)) [Nab81], capacitor-clamped (flying-capacitors (FCs)) [Mey92] [Mey07], cascaded multi-cell with separate DC sources (cascaded H-bridge (CHB)) [Bak75], and modular multilevel converters (MMC) [Mar02] [Mar03] are available for medium- and high- voltage applications. The most attractive features of these topologies are as follow:

1) They can generate output voltages with extremely low distortion and lower *dv/dt*.

2) They can operate with a lower switching frequency. Thus, high converter efficiency is achieved.

In this section, these four multilevel topologies are studied and compared. For each structure, the converter modelings (modulation and control techniques, applications, derived structures etc.) are proposed.

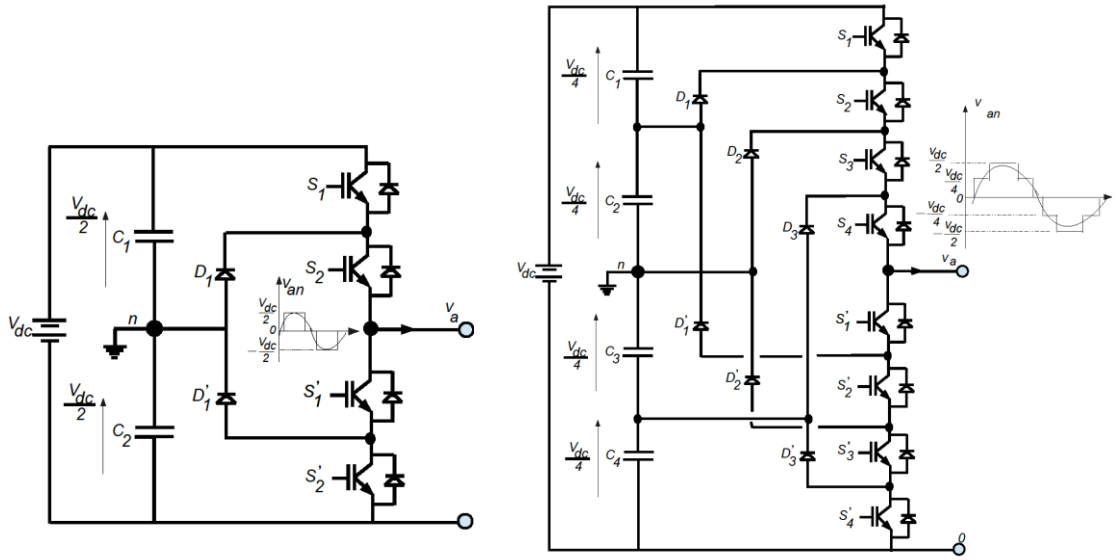
1.1.1. Neutral-point-clamped (NPC) multilevel converter

Neutral-point-clamped (NPC) multilevel inverters, illustrated in Fig. 1.3, prevailed in the 1980s by [Nab81]. For understanding the operation of this kind of converter, a three-level NPC (3L-NPC) and a five-level NPC (3L-NPC) configuration are considered.

Topology descriptions: A 3L-NPC converter is shown in Fig. 1.3a. The key components that distinguish this circuit from a conventional two-level converter are two clamping diodes: D_1 and D'_1. Since all semiconductors operate at a commutation voltage of half of the DC-link voltage, the topology offers a simple solution to extend voltage and power ranges of the existing 2L-VSC technology, which are severely limited by the blocking voltage of power semiconductors with active turn-on and turn-off capabilities. Hence, the converter is of particular interest for medium-voltage (MV) applications (ex. 3L-NPC for MV drive in article [Chr07]: V_{DC} = 12V, V_{out} = 7.2kV, S = 8.7MVA). The DC-bus voltage of this circuit is split into three levels by two series-connected bulk capacitors, C_1 and C_2. The middle-point of the two capacitors *n* can be defined as the neutral point. The output voltage v_{an} has three states: $V_{dc}/2$, 0, and $-V_{dc}/2$. For the voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S'_1 and S'_2 need to be turned on; and the 0 level, S_2 and S'_1 need to be turned on. Table 1.1 summaries the conduction states to be generated.

Table 1.1: Three-level switching states of 3L-NPC

S_1	S_2	S'_1	S'_2	Output voltage v_{an}
1	1	0	0	$+V_{dc}/2$
0	1	1	0	0
0	0	1	1	$-V_{dc}/2$



(a) (b)

Fig. 1.3: Neutral-point-clamped multilevel converters:
(a) Three-level configuration (3L-NPC), and
(b) *Five-level configuration (5L-NPC).*

Fig. 1.3b shows a 5L-NPC converter in which the DC-bus consists of four bulk capacitors: C_1, C_2, C_3, and C_4. As seen in this figure, the voltage across each capacitor is $V_{dc}/4$, and each device voltage stress will be limited to one capacitor voltage level $V_{dc}/4$ through clamping diodes. The five states of the output voltage v_{an} are: $V_{dc}/2$, $V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$. The switching states combinations of power semiconductor devices in this circuit to produce five-level of output voltage v_{an} are summarized as follows and in Table 1.2 (Note: the state "1" and "0" indicate the corresponding switch is "ON" and "OFF", respectively.):

1) For voltage level $v_{an} = V_{dc}/2$, all upper switches S_1-S_4 need to be turned on.

2) For voltage level $v_{an} = Vdc/4$, three upper switches S_2-S_4 need to be turned on and one lower switch S'_1 turned on.

3) For voltage level $v_{an} = 0$, turn on two upper switches S_3-S_4 and two lower switches S'_1-S'_2.

4) For voltage level $v_{an} = -V_{dc}/4$, turn on one upper switch S_4 and three lower switches S'_1-S'_3.

5) For voltage level $v_{an} = -V_{dc}/2$, turn on all the lower switches S'_1-S'_4.

Table 1.2: Five-level switching states of 5L-NPC

S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4	Output voltage v_{an}
1	1	1	1	0	0	0	0	$+V_{dc}/2$
0	1	1	1	1	0	0	0	$+V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{dc}/4$
0	0	0	0	1	1	1	1	$-V_{dc}/2$

Control (modulation) methods: there are different modulations schemes to generate the desired converter output voltage. The commonly applied modulation methods in this kind of multilevel converter are: the carrier-based pulse-width modulation (CB-PWM), the space-vector modulation (SVM), and selective harmonic elimination (SHE). The article [Jos02] details all the control and modulation strategies for this kind of converters. As an example, the article [Jos07] used phase-disposition sine-triangle modulation (PD-PWM) as modulation method for a 3L-NPC converter. In this example, to generate switching pulses, two triangle waveforms with the same switching frequency and phase with different amplitudes (one with 0 to 1 amplitude, but another one with -1 to 0 amplitude) are needed as presented in Fig. 1.4. As a result, three levels of output voltage v_{an} ($V_{dc}/2$, 0, $-V_{dc}/2$) can be achieved.

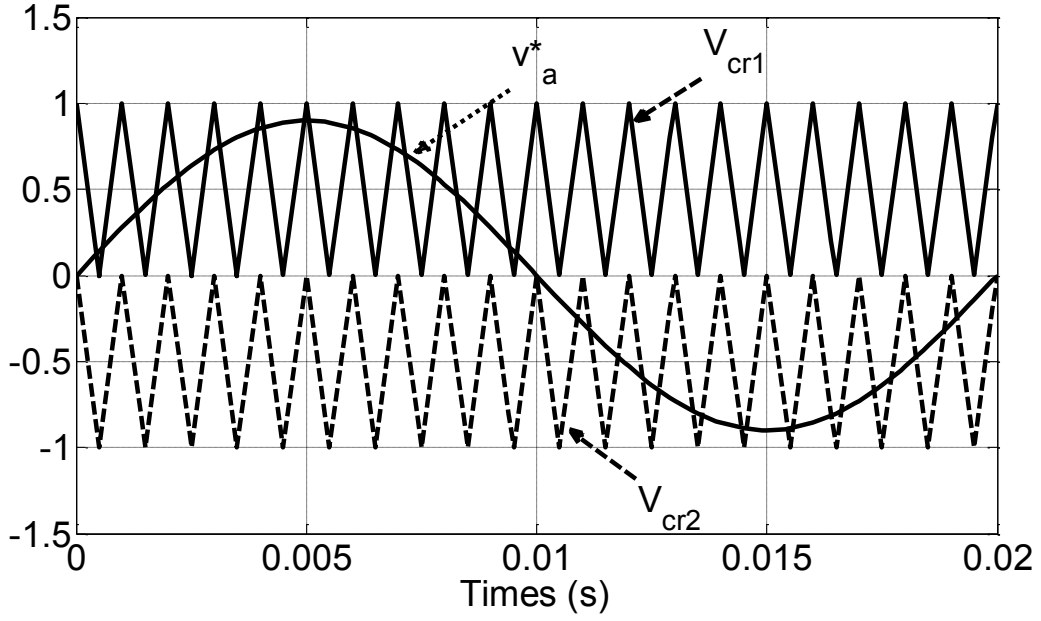
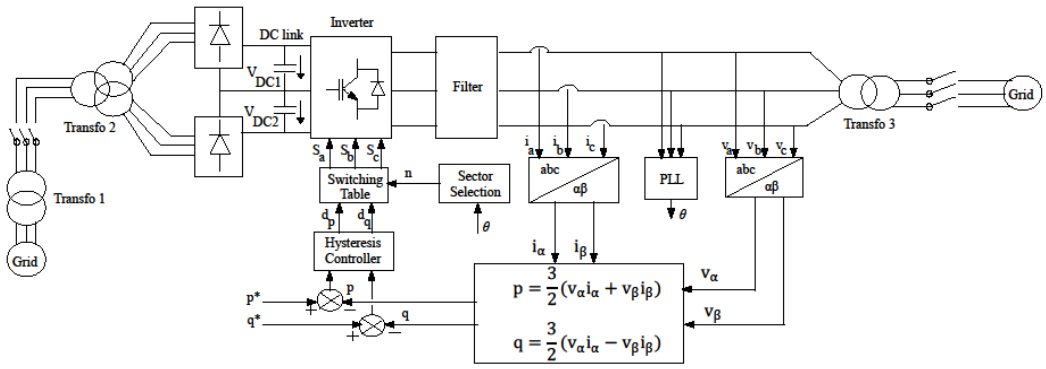
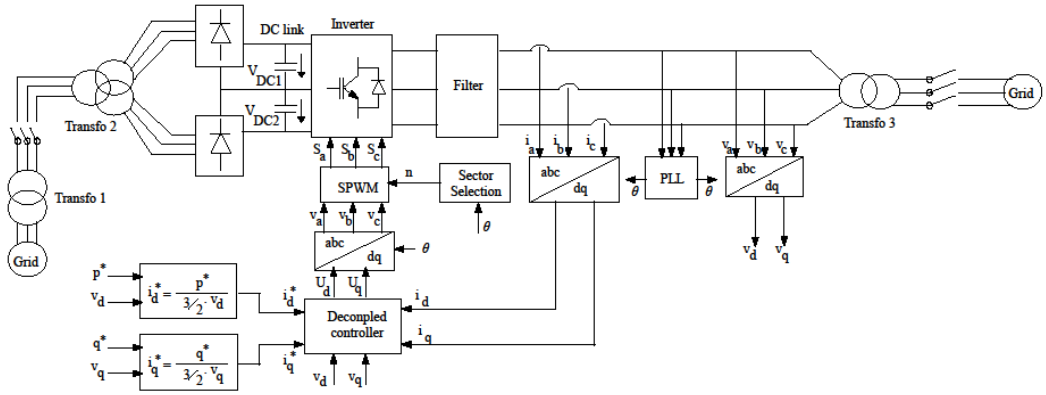


Fig. 1.4: Example of phase-disposition (level-shift) modulation for 3L-NPC converter

Moreover, to ensure the inverter operation, the DC-bus capacitor voltages need to be balanced and the output quantities (i_x, v_x, '$x=\{A,B,C\}$') must be controlled. Several control solutions are proposed based on its main applications. As an example, in Fig. 1.5a and Fig. 1.5b, a reference [Han15] proposes two control methods (Direct Power Control (DPC) and Voltage Oriented Control (VOC)) of a 3L-NPC grid connected converter.



(a)



(b)

Fig. 1.5: Example of the proposed control design for 3L-NPC converter:
(a) Direct power control (DPC) methods proposed by [Han15]
(b) *Voltage oriented control (VOC) methods proposed by [Han15]*

According to the articles [Jos02] and [Han15], the objective of DPC is to control the active and reactive power directly. As seen in Fig. 1.5a, it mainly consists of an instantaneous active power and reactive power calculation, the hysteresis controller and switching states table (modulation technique). The hysteresis controller block is used to control the active (P) and reactive (Q) power with the hysteresis bands (H_p for active power and H_q for reactive power). This block produces two output d_p and d_q with only two states (states "0" and "1") to adjust the controlled variables. States "0" and "1" means the desired effect on controlled variable needs to be decreased and increased, respectively. Switching table with space-vector modulation (SVM) is used to generate the

gate signal after receiving the d_p and d_q informations from hysteresis block. Design of hysteresis controller and switching table with space-vector modulation (SVM) are detailed in references [Nog98] [Han15].

Voltage oriented control (VOC) is commonly used for grid connected converters. As shown in Fig. 1.5b; the control structure consists of a phase-locked loop (PLL) block, a proportional integral (PI) decoupled controller for the grid current, and sinusoidal modulation method (SPWM). A decoupled controller is used to control the output currents and voltage of the inverter by comparison to their reference values. Then, the output voltage waveform of this controlled block goes into SPWM to produce the controlled gate signals of the inverter. The design of PI controller and other designs (filters, DC voltage balancing controls, etc.) are presented in the article [Han15].

Recent researches: Table 1.3 lists several recent researches of NPC multilevel converter topology: different control methods, applications, and also the derived structures.

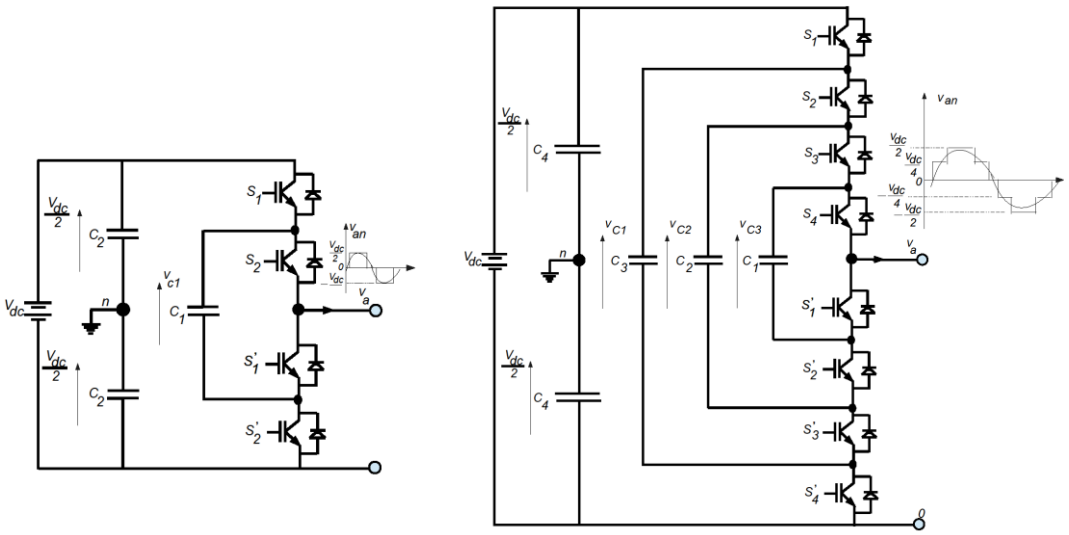
Table 1.3: List of publications about NPC inverter applications, capacitor voltage balancing algorithms, etc.

Controls	**Applications**	**Derived structures**
- [Cho14] presents a simplified PWM strategy for 3L-NPC with unbalanced DC link. The authors propose the SV-PWM method and provide the analytical expression of the unbalanced DC-bus capacitor voltages. Then, for balancing the DC bus voltages, they propose a PI controller to control a neutral-point current. - [Chi13] proposes triangular carrier PWM modulation to control the gate pulse signal for the Flexible AC Transmission Systems (FACTS) applications (FACTS) applications. The input voltage information of CB-PWM block can be a sinusoidal waveform with second harmonics injections, sixth harmonics injections, and square sixth harmonics injections. Moreover, for each technique, the capacitor voltage balancing algorithm is also described. - [Cho16] presents a DC-bus voltage balancing algorithm for 3L-NPC inverter to drive motor with reduced common-mode voltage. The authors detail the SV-PWM control (switching	- Medium voltage drive [Cho15] [Cho16], - Renewable energy generation [Tey14], - Electric vehicle traction [Cho14], - flexible AC transmission systems (FACTS) applications [Chi13], - …	- Active neutral-point-clamped (ANPC) [Pul11]

vector control combination), analytical expression of load (permanent magnet synchronous machine (PMSM)), proposed control strategy and voltage balancing block integration etc. - DC-link voltage balancing methods: keeps all the capacitor voltage stay near V_{dc}/N, where N is number of power devices. • External hardware based technique [Sch01] • PWM control based techniques [Cho14] [Cho15] [Cho16]		

1.1.2. Flying capacitor (FCs) multilevel inverter

Topology descriptions: Flying capacitors (FCs) multilevel converter as voltage-source converters (VSC) was introduced in 1991 by Prof. Meynard T.A. and Prof. Foch H. [Mey92] [Mey98]. This thesis dissertation presents the concept of three- and five-level flying capacitors topologies (as illustrated in Fig. 1.6) and their proposed control methods. The circuit has been called the flying capacitor converter with independent capacitors clamping the device voltage to one capacitor voltage level.



(a) (b)

Fig. 1.6: Flying capacitors multilevel converter topologies:
(a) Three-level (3L-FCs),
(b) Five-level (5L-FCs),

A three-level flying capacitors (3L-FCs) converter's circuit is illustrated in Fig. 1.6a. Three-level output voltages across phase *a* and *n* are: $v_{an} = [V_{dc}/2, 0, -V_{dc}/2]$. For voltage level $V_{dc}/2$, switches S_1 and S_2 need to be turned on; for $-V_{dc}/2$, switches S'_1 and S'_2 need to be turned on; and for 0 level, either pair (S_1, S'_1) or (S_2, S'_2) needs to be turned on. These switching states are resumed in Table 1.4.

Table 1.4: Three-level switching states of 3L-FCs

S_1	S_2	S'_1	S'_2	Output voltage v_{an}
1	1	0	0	$+V_{dc}/2$
1	0	1	0	0
0	1	0	1	
0	0	1	1	$-V_{dc}/2$

Fig. 1.6b illustrates the fundamental building block of a phase-leg five-level flying capacitors (5L-FCs) converter. The voltage synthesis in a 5L-FCs has more flexibility than a 5L-NPC converters. According to [Mey92], the nominal voltage across clamping capacitors; C_1, C_2, and C_3 are $v_{C1} = 1/4V_{dc}$, $v_{C2} = 2/4V_{dc}$, and $v_{C3} = 3/4V_{dc}$; respectively. Hence the five states of the output phase voltage with respect to the neutral point *n,* v_{an} are: $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$, and $-V_{dc}/2$. This voltage v_{an} can be synthesized by the following switch combinations:

1) For voltage level $v_{an} = V_{dc}/2$, all the upper switches S_1-S_4 are turned on.

2) For voltage level $v_{an} = V_{dc}/4$, there are four combinations between these eight switches:

   a) S_1, S_2, S_3, and S'_1 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) – $V_{dc}/4$ (from C_1) (see: Fig. 1.7).
   b) S_1, S_2, S_4, and S'_2 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) $-V_{dc}/2$ (from C_2) + $V_{dc}/4$ (from C_1).
   c) S_2, S_3, S_4, and S'_4 are turned on: $v_{an} = 3V_{dc}/4$ (from C_3) – $V_{dc}/2$ (from lower C_4).
   d) S_1, S_3, S_4, and S'_3 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) - $3V_{dc}/4$ (from C_3) + $V_{dc}/2$ (from C_2).

3) For voltage level $v_{an} = 0$, there are six combinations between these eight switches:

   a) S_1, S_2, S'_1, and S'_2 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) – $V_{dc}/2$ (from C_2).
   b) S_3, S_4, S'_3, and S'_4 are turned on: $v_{an} = V_{dc}/2$ (form C_2) – $V_{dc}/2$ (from lower C_4).
   c) S_1, S_3, S'_1, and S'_3 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) – $3V_{dc}/4$ (from C_2) – $V_{dc}/4$ (from C_1).
   d) S_1, S_4, S'_1, and S'_4 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) – $3V_{dc}/4$ (from C_3) + $V_{dc}/4$ (from C_1).

e) S_2, S_4, S'_2, and S'_4 are turned on: $v_{an} = 3V_{dc}/4$ (from C_3) – $V_{dc}/2$ (from C_2) + $V_{dc}/4$ (from C_1) – $V_{dc}/2$ (from lower C_4).

f) S_2, S_3, S'_1, and S'_4 are turned on: $v_{an} = 3V_{dc}/4$ (from C_3) – $V_{dc}/4$ (from C_1) – $V_{dc}/2$ (from lower C_4).

4) For voltage level $v_{an} = -V_{dc}/4$, there are four combinations from these eight switches:

a) S_1, S'_1, S'_2, and S'_3 are turned on: $v_{an} = V_{dc}/2$ (from upper C_4) – $3V_{dc}/4$ (from C_3).

b) S_2, S'_1, S'_2, and S'_4 are turned on: $v_{an} = -V_{dc}/2$ (from lower C_4) + $3V_{dc}/4$ (from C_3) – Vdc/2 (from C_2)

c) S_3, S'_1, S'_3, and S'_4 are turned on: $v_{an} = V_{dc}/2$ (from C_2) – $V_{dc}/2$ (from lower C_4) – $V_{dc}/4$ (from C_1)

d) S_4, S'_2, S'_3, and S'_4 are turned on: $v_{an} = V_{dc}/4$ (from C_2) – $V_{dc}/2$ (from lower C_4).

5) For voltage level $v_{an} = -V_{dc}/2$, all the lower switches S'_1-S'_4 are turned on.

Moreover, Table 1.5 lists the switch combinations used to synthesize the output voltage v_{an}. This table indicates also the states of the flying capacitors corresponding to the switch combination chosen. Charging of a capacitor is indicated by "+", discharging by "-", and "NC" shows neither charging nor discharging.

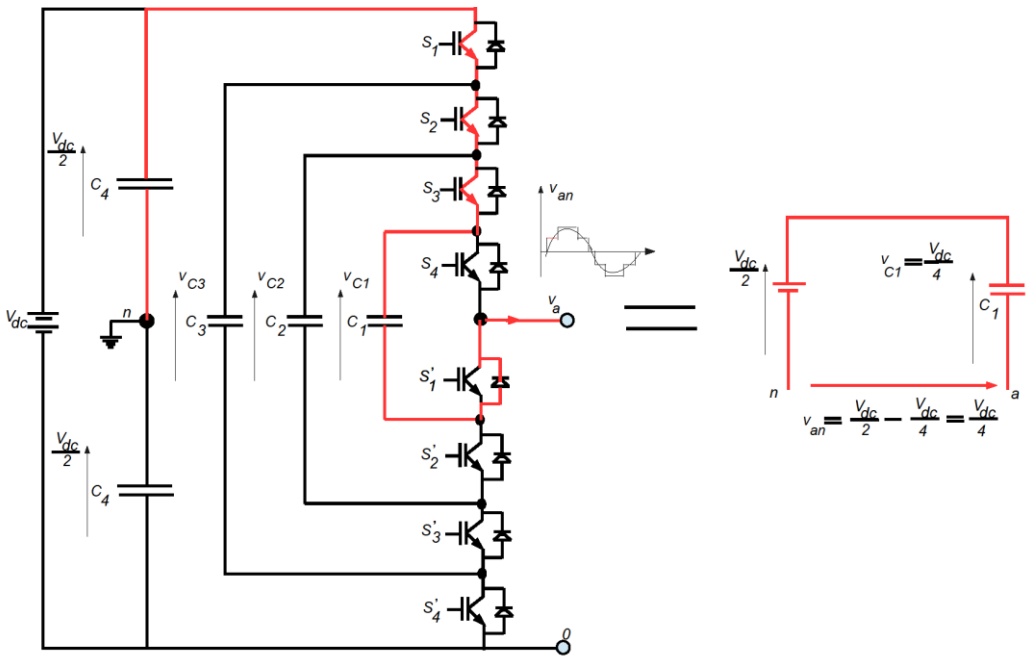


Fig. 1.7: One example of an operation mode $v_{an} = V_{dc}/4$ with S_1-S_3 are turned on for higher switches parts and S'_1 is turned on for the lower switches parts

Table 1.5: Switching scheme for one-phase of a 5L-FCs

S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4	C_1	C_2	C_3	v_{an}
1	1	1	1	0	0	0	0	NC	NC	NC	$+V_{dc}/2$
1	1	1	0	1	0	0	0	+	NC	NC	
1	1	0	1	0	1	0	0	-	+	NC	
1	0	1	1	0	0	1	0	NC	-	+	$+V_{dc}/4$
0	1	1	1	0	0	0	1	NC	NC	-	
0	0	1	1	0	0	1	1	NC	-	NC	
0	1	0	1	0	1	0	1	-	+	-	
0	1	1	0	1	0	0	1	+	NC	-	0
1	0	0	1	0	1	1	0	-	NC	+	
1	0	1	0	1	0	1	0	+	-	+	
1	1	0	0	1	1	0	0	NC	+	NC	
1	0	0	0	1	1	1	0	NC	NC	+	
0	1	0	0	1	1	0	1	NC	+	-	
0	0	1	0	1	0	1	1	+	-	NC	$-V_{dc}/4$
0	0	0	1	0	1	1	1	-	NC	NC	
0	0	0	0	1	1	1	1	NC	NC	NC	$-V_{dc}/2$

Control (modulation) methods: According to [Mey92], [Mey98], [Jos07], the preferred modulation strategy is the phase-shifted pulse-width modulation (PS-PWM). PS-PWM provides the natural capacitor voltage balance, but the quality line-to-line voltage is not the best. It is a passive method and no measurements are needed, but the balancing process is not satisfactory, since dynamic is low for the FC voltages and the control imposes some constraints to the control signals [Fra10]. On the other hand, phase-disposition modulation (PD-PWM) produces better line-to-line voltage quality than PS-PWM, but the natural capacitor voltage balance cannot be achieved. However, the closed-loop voltage balancing algorithm method can be applied to balance these capacitor voltages.

The voltage balancing method is used to ensure the clamping capacitor voltages to follow their references. Voltages across capacitors are expressed as: $V_{Ck} = k.V_{dc}/N$; where k corresponds to indices of clamping capacitors ($k = 1, ..., N-1$), and N is number of power semiconductors per arm of one-phase. As an example, the article [Ame15] implements a single-carrier PD-PWM for FCs multilevel converters. These carrier triangle waveforms are in the same switching frequency f_{sw}, but different amplitudes which can be calculated as a function of the number of power semiconductors in FCs circuit. This reference provides also the explanations of the cell selection considerations from PD-PWM modulation method. This cell selections algorithm is an essential tool for voltage balancing control method, where we need to know which capacitors need to be charged and to be discharged (detail in [Ame15] and Table 1.5).

Beside the capacitor voltages balancing control, the flying capacitors (FCs) multilevel converters require to control the output current. To achieve this; several

controls efforts such as: direct predictive control strategy [Fra10], Petri Nets control design method [Sal15], hysteresis-based control method [Mos13] are proposed. As an example here, Fig. 1.8 presents a direct predictive control method proposed by [Fra10]. The capacitor voltages and phase current are measured and compared to their references. Then, the output of each controller (voltages/current) and the sign of phase current are the input for profile table selection block. This sequence table is a main tool for capacitor voltage balancing achievements. After that, the controlled signals can be generated to power semiconductors with respect to the specific application requirements.

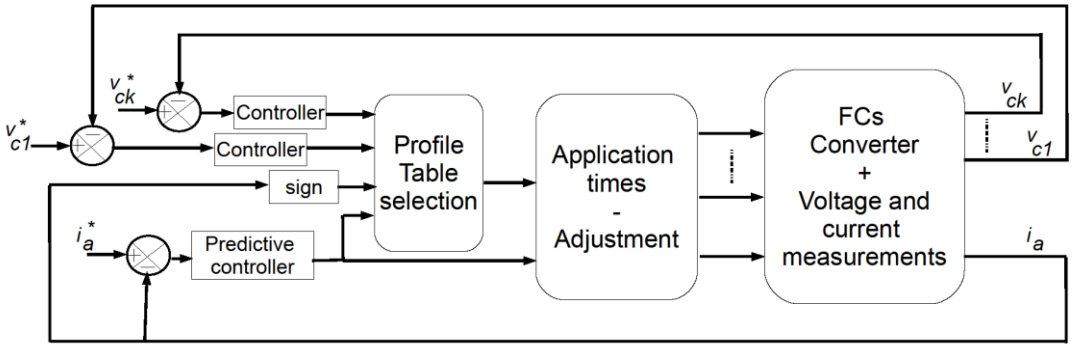


Fig. 1.8: Direct control of one-phase of flying capacitors (FCs) multilevel converter proposed by [Fra10]

Recent researches: Table 1.6 lists several recent researches about FCs multilevel converter topology: different control methods, applications, and also the derived structures.

Table 1.6: List of publications about FCs inverters applications, capacitor voltage balancing algorithms, etc.

Controls	**Applications**	**Derived structures**
- [Fan10] presents a direct control strategy for a 4-L FC inverter. The authors propose proportional (P) controller for capacitor voltage balancing and proportional integral (PI) controller for output current regulation. Moreover, PS-PWM modulation is used to generate the IGBTs/MOSFETs pulse signals. - [Ame15] uses PS-PWM and PD-PWM for generating pulse signals,	- Uninterruptable power supply (UPS) applications [Sto11], - AC transmission systems [Shu04], distributed generation applications [Min14], - Double star induction machine applications [Oud10], - …	- A new 5L half-bridge based on a hybrid ANPC/FC DC-source inverter [Joa15] - 7L-FC based ANPC inverter [Kon12], - FC-boost converter with synchronous rectification [Gui16]

respectively. The closed-loop voltage balancing is also presented. - [Sal15] presents control design strategy for FC multilevel converter based on Petri Nets (PN) (Petri Nets incorporate additional analysis tools for an efficient solution of the control problem and does not require to enumerate explicitly the state space). - [Sat15] study on minimum required capacitor in FC inverter topology. - …		

1.1.3. Cascaded H-bridge (CHB) multilevel converters

The cascaded H-bridge (CHB) multilevel converter appeared first in 1975 [Bak75]. It matured during the 1990s and gained more attention after 1996 [Lai96], [Ham97]. Due to its modular structure and power-quality operational characteristics, this topology has been used in Medium-Voltage (MV) high power-drives (maximum rates of 13.8kV, 1400A, and 31MVA) applications.

Topology descriptions: The CHB is composed by the series connection of H-bridge (HB) power cells as shown in Fig. 1.9b. Each cell uses an independent dc-link voltage to generate a modulated voltage at the output terminals. This dc-source voltage is supplied by an isolated dc-to-dc converter. Each HB cell (cf. Fig. 1.9a) is able to produce three output voltage (V_{ab}) levels: $+V_{dc}$, 0, and $-V_{dc}$ by the combination of power switches. For voltage level $+V_{dc}$, switches S_{11} and S_{41} need to be turned on; for $-V_{dc}$, switches S_{21} and S_{31} need to be turned on; and for level 0, either pair of (S_{11}, S_{31}) or (S_{21}, S_{41}) need to be turned on. This structure is capable of reaching medium output voltage levels using only standard low-voltage mature technology components. The maximum number of voltage levels of the phase voltage L_{ph} is given by:

$$L_{ph} = 2N_{HB} + 1 \tag{1.1}$$

Where, N_{HB} is the number of H-bridge power cells. As an example, a five-level CHB inverter is presented in Fig. 1.9c. The five states of a phase voltage v_{an} are: +2Vdc, Vdc, 0, -Vdc, and -2Vdc. The switching states combinations of power semiconductor devices in this circuit to produce five-level of output voltage v_{an} are presented in Table 1.7.

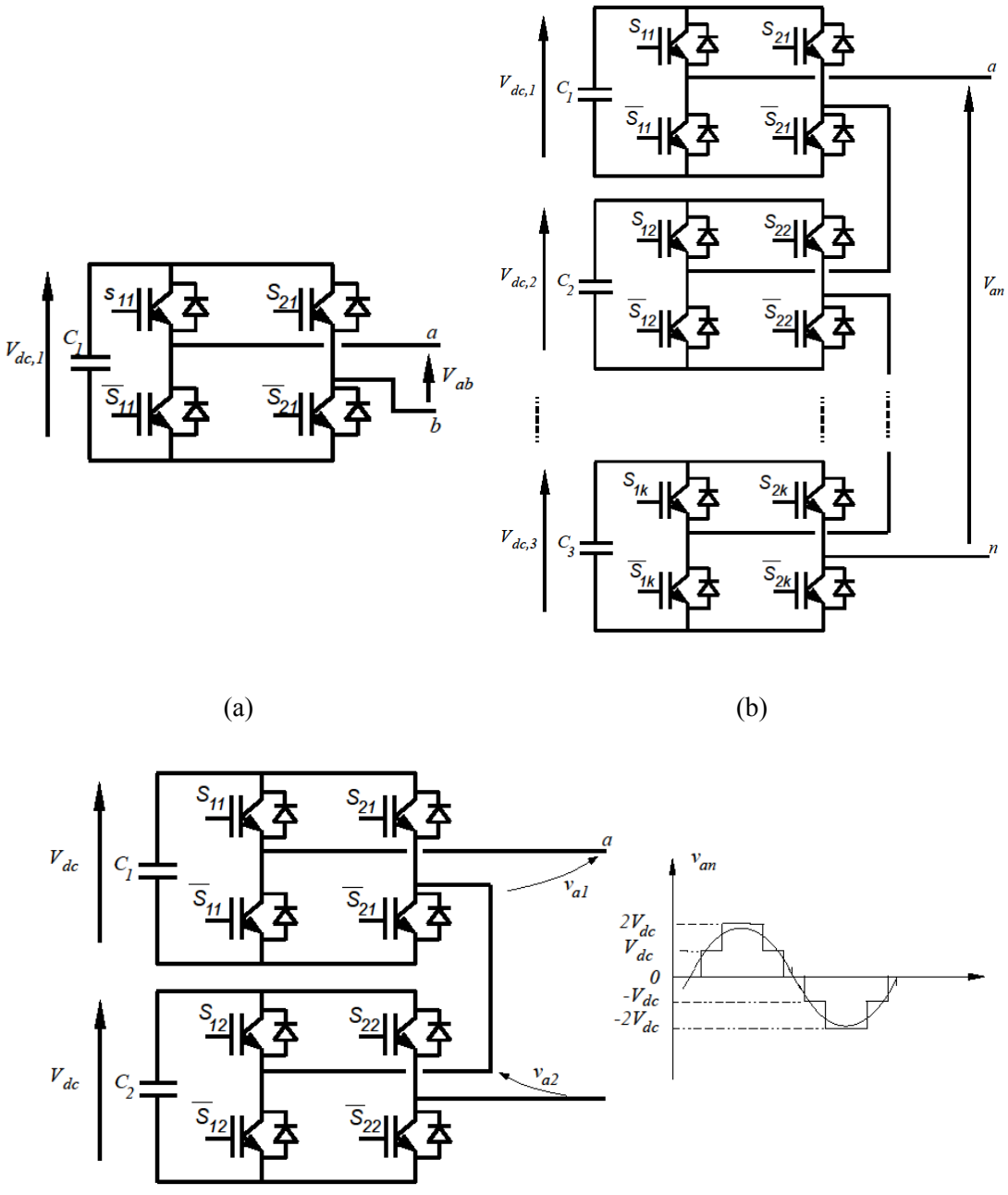


Fig. 1.9: Cascaded H-bridge (CHB) multilevel converter description:
(a) A power cell produces three-level of output voltage: $+V_{dc}$, 0, $-V_{dc}$
(b) (2NHB+1)-level of one phase output voltage v_{an}
(c) *Five-level CHB converter (5L-CHB).*

Table 1.7: Switching states for five-level CHB converter (5L-CHB)

Cell 1			Cell 2			Output voltage v_{an}
S_{11}	S_{12}	v_{a1}	S_{12}	S_{22}	v_{a2}	
1	0	V_{dc}	1	0	V_{dc}	$+2V_{dc}$
1	0	V_{dc}	0	0	0	$+V_{dc}$
1	0	V_{dc}	1	1	0	
0	0	0	1	0	V_{dc}	
1	1	0	1	0	V_{dc}	
0	0	0	0	0	0	0
0	0	0	1	1	0	
1	1	0	0	0	0	
1	1	0	1	1	0	
1	0	V_{dc}	0	1	$-V_{dc}$	
0	1	$-V_{dc}$	1	0	V_{dc}	
0	1	$-V_{dc}$	1	1	0	$-V_{dc}$
0	1	$-V_{dc}$	0	0	0	
0	0	0	0	1	$-V_{dc}$	
1	1	0	0	1	$-V_{dc}$	
0	1	$-V_{dc}$	0	1	$-V_{dc}$	$-2V_{dc}$

Control (modulation) methods: Phase-shifted PWM (PS-PWM) is the natural PWM method for CHB, mainly due to the modularity of this topology. According to Fig. 1.9a; each power cell, made of four switches, requires two triangle waveforms with 180^o different phase and the same reference voltage signal. As presented in [Jos07], the lowest output voltage distortion is achieved with $180^o/N_{HB}$ phase shifts between the carriers, for N_{HB} power cells. The operating principle is shown for two-cell five-level CHB (5L-CHB) in Fig. 1.10. Where 90^o phase shifts between two carrier cells are implemented to achieve five states of one phase output voltage (v_{an}: $+2V_{dc}$, V_{dc}, 0, $-V_{dc}$, and $-2V_{dc}$) with low harmonic distortion. Another main advantage of PS-PWM is a power distribution among power cells in the CHB converter. Where, the PD-PWM technique produces uneven distribution of power among cells (reference [Mar10] explains this phenomena). The selective harmonic elimination (SHE) and space-vector (SV) modulation methods have been proposed to control CHB converter for low-switching-frequency application [Jos07].

To fully control CHB multilevel converters, the output phase current and dc capacitor voltage balancing must be controlled. As an example, a reference [Hyu14] proposes few proportional-integral (PI) controllers to control the output current and dc-link voltage (cf. Fig. 1.11). The measurements of output current and dc-link voltage information are needed to be compared to their reference values. Moreover, as seen in this figure, the authors also propose a power imbalance block to control the power distribution among cells and power balance between phases of CHB converter. The idea is to ensure the average power for each phase to stay in the constraint limit values (details

in [Hyu14]). Then, PS-PWM modulation method is used to generate gate signals with the advantages of power distribution among power cells.

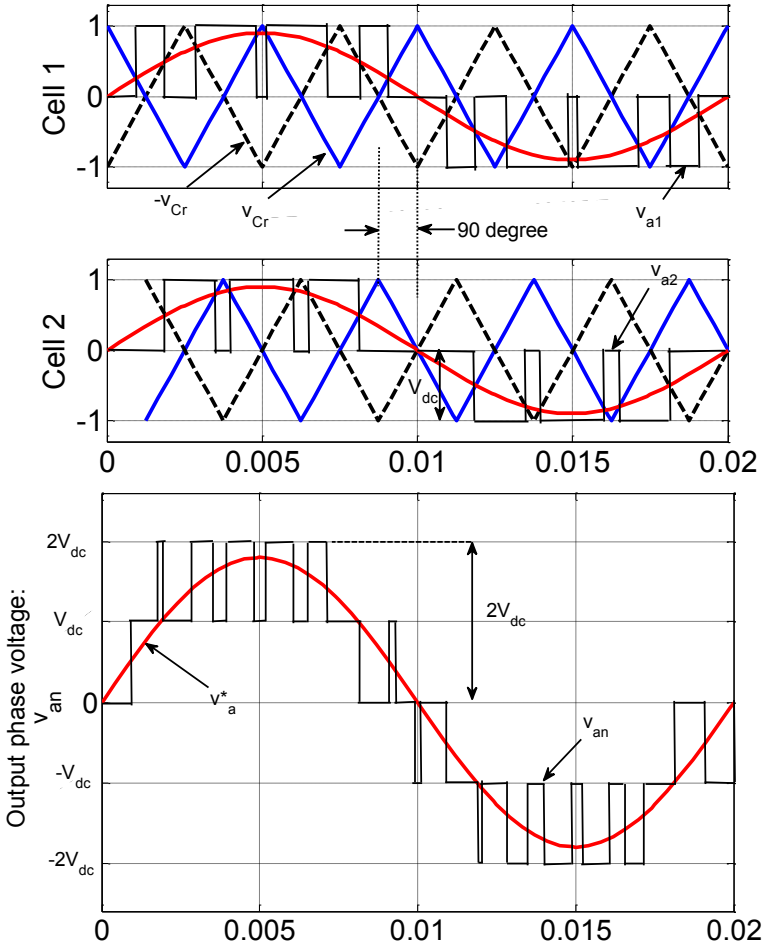


Fig. 1.10: Two-cell five-level CHB (5L-CHB) PS-PWM waveform generation

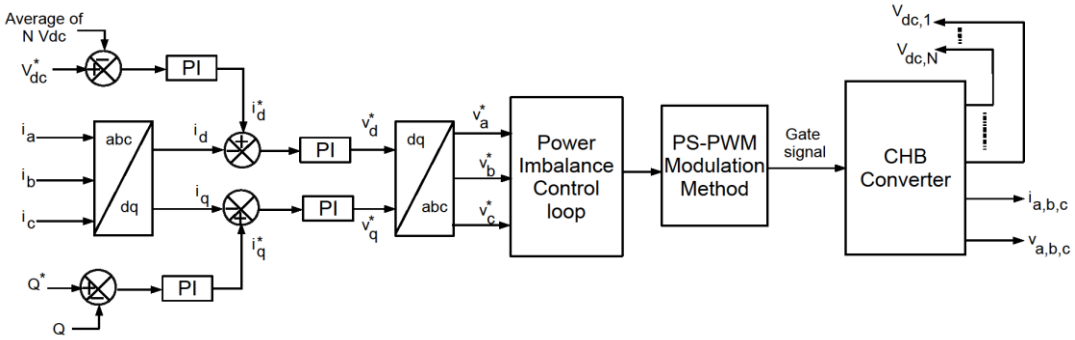


Fig. 1.11: Control diagram of the CHB converter proposed by [Hyu14]

Recent researches: Table 1.8 lists several recent researches about CHB multilevel converter topology: different control methods, applications, and also the derived structures.

Table 1.8: List of publications about CHB inverters applications, capacitor voltage balancing algorithms, etc.

Controls	**Applications**
- [Hyu16] proposes PD-PWM to control the seven-level CHB (7L-CHB) inverter. The authors also study the switching faults of semiconductors in a power cell. Then, they propose fault-detection methods and the fault diagnosis. The proposed methods are supported by the simulation and experimental results. - [Yif16] studies about the power balance optimization of CHB multilevel converters for large-scale photovoltaic (PV) integration. The authors propose a zero sequence injection method to optimize the converter power balance, extending the converter operation with severe power imbalance between phases and among power cells in one phase. To support this proposed method, the simulation results of a 10MW PV power plant and experimental results from a scale-down prototype 9kW are provided. - …	- [Jos07] presents the CHB for industrial medium-voltage drives. - [Mar10] presents the various applications of CHB: to drive high-voltage high-power pumps and fans for numerous power plants (oil and gas plant, cooling system, etc.), STATic COMpensator (STATCOM), traction system, and liquefied natural gas (LNG) plants. - …

1.1.4. Modular Multilevel Converters (MMCs)

The modular multilevel converter (MMC) was first introduced in 2002 by Prof. Rainer Marquardt *et al.* [Mar02], [Mar03]. Due to the high modularity, high scalability, and high power quality; this converter has been proposed first for high voltage direct current (HVDC) applications (an example of HVDC rate: 50MVA, up to 138kV of nominal output voltage, 60kV of dc-link voltage).

Topology descriptions: Fig. 1.12 illustrates the MMC converter. Each phase (MMC leg) is composed by two MMC arms, and each arm is made of power cells (sub-module: SM) in series. This figure also shows the arm inductance L_j which must be connected in series with each group of cells in order to limit the current due to instantaneous voltage differences of the arms. Hence, this converter is suitable for high-and very high-voltage high-power applications by using only the available power semiconductors on the trade. Then, based on some recent research articles [Hag09] [Roh10] [Kol12], this converter is also interesting for medium-voltage (MV) applications such as: MV drives, traction system, etc.

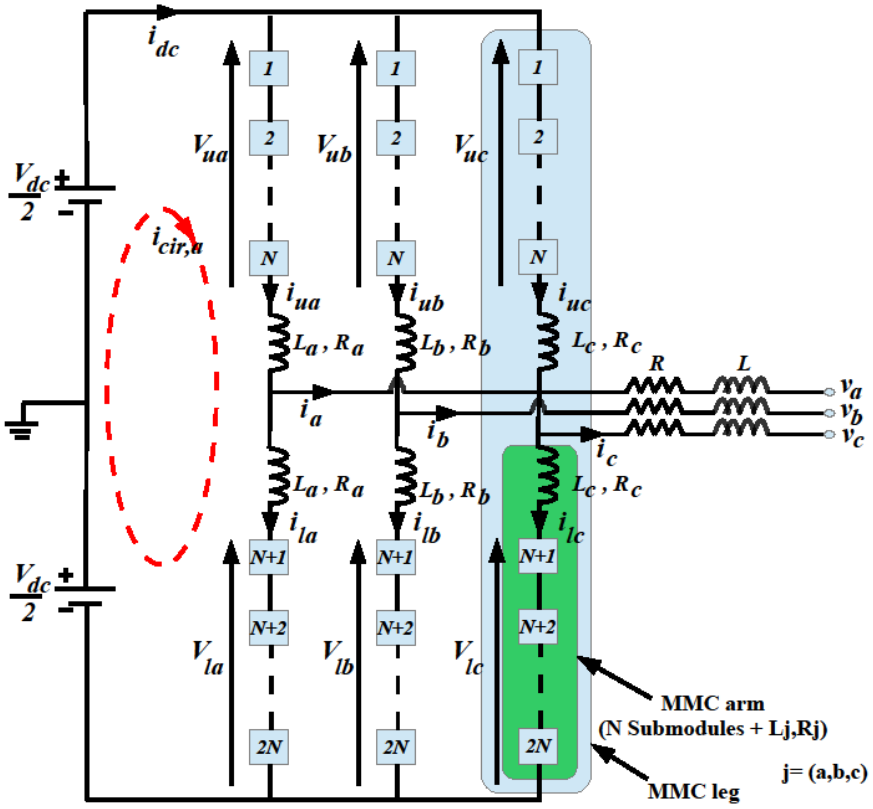


Fig. 1.12: Three-phase modular multilevel converter (3p-MMC)

Unlike the power cell topology of the CHB converter, the power cell topologies of the MMC converter are flexible as illustrated in Fig. 1.13. They are summarized as follow:

1) *Half-bridge (HB) sub-module*: This power cell topology is illustrated in Fig. 1.13a. It is made of an inverter leg (two power semiconductors) and one capacitor. The HB cell can generate only two-state of output voltage (V_{SM}: 0 and a positive voltage V_c).

2) *Full-bridge (FB) sub-module*: Fig. 1.13b illustrates full-bridge (FB) cell which requires two inverter legs (four semiconductors) and a capacitor. This cell can generate positive, zero, and negative output voltages. The implementation of this sub-module's topology provides additional degree of freedom to control the capacitor voltages.

3) *Unidirectional sub-module*: This cell, shown in Fig. 1.13c, has been proposed to reduce the number of semiconductors per cell, but the switching states are restricted and depend on the current direction [Sou13].

4) *Multilevel inverter as MMC's sub-module*: Considering multilevel inverters as sub-modules of MMC converter are proposed by [Sol13A] [Sol13B]. For

instance, in those references, 3L-NPC (Fig. 1.13e), 3L-FC (Fig. 1.13d), and two-level (2L) with numerous switches in series (Fig. 1.13f) are used as MMC's multilevel sub-module concepts. The main objective of using these structures as sub-modules is to achieve a better usage of the trade components such as semiconductors. Thus, it means that with the available power semiconductors, a novel MMC can be achieved to respond to new converter specifications (very high-voltage application). The controls structure, validation results (simulation and experimental), and comparison with other sub-modules are clearly presented in [Sol13A] [Sol13B].

5) *More challenging sub-modules*: two more sub-module topologies are illustrated in Fig. 1.13g and Fig. 1.13h, are cells with resonant inverter for inductive transfer and current source cell [Per15]. Sub-modules with resonant inverters for inductive transfer are proposed to help MMC control structure, specifically the capacitor voltage balancing control. Whereas, current source power cells are proposed to achieve a higher voltage level and power rating than the traditional voltage source power cells.

Brief comparisons of SM topologies for MV applications: Two main critical points for SM topology selection are control complexities and available components on the trade.

1) Control complexities: Keeping in mind that the MMC structure requires to control the circulating current in each phase loop (averaging control) and balancing the capacitor voltages of SMs (capacitor voltage balancing algorithm). As just presented previously, the half-bridge sub-module (HB-SM) has less power semiconductor components compared to other proposed topologies in literature. Hence, its control structure is very simple and easy to be implemented.

2) *Available components on trade:* The specification of MV dc voltages is in the range of few-kilovolts to few ten-kilovolts. For instance, as presented in [Roh10], the $V_{dc,bus}$ = 10kV requires twelve HB-SMs per arm (V_{SM} = 833V). FZ600R17KE3 IGBT module (V_{CES} = 1.7kV ($V_{CE,ref}$ = 900V) and $I_{C,nom}$ = 600A) from Infineon/EUPEC company are used. Moreover, currently, 3.3-, 4.5-, and 6.5-kV IGBTs (modules or press packs) and 4.5- and 5.5-kV IGCTs are available on the market [Jos07].

Thus, for MV applications of MMC converters, half-bridge (HB-SM) is a suitable choice. With this SM's topology, (N+1)-level of output phase voltage is achieved where N is the number of SMs per converter's arm.

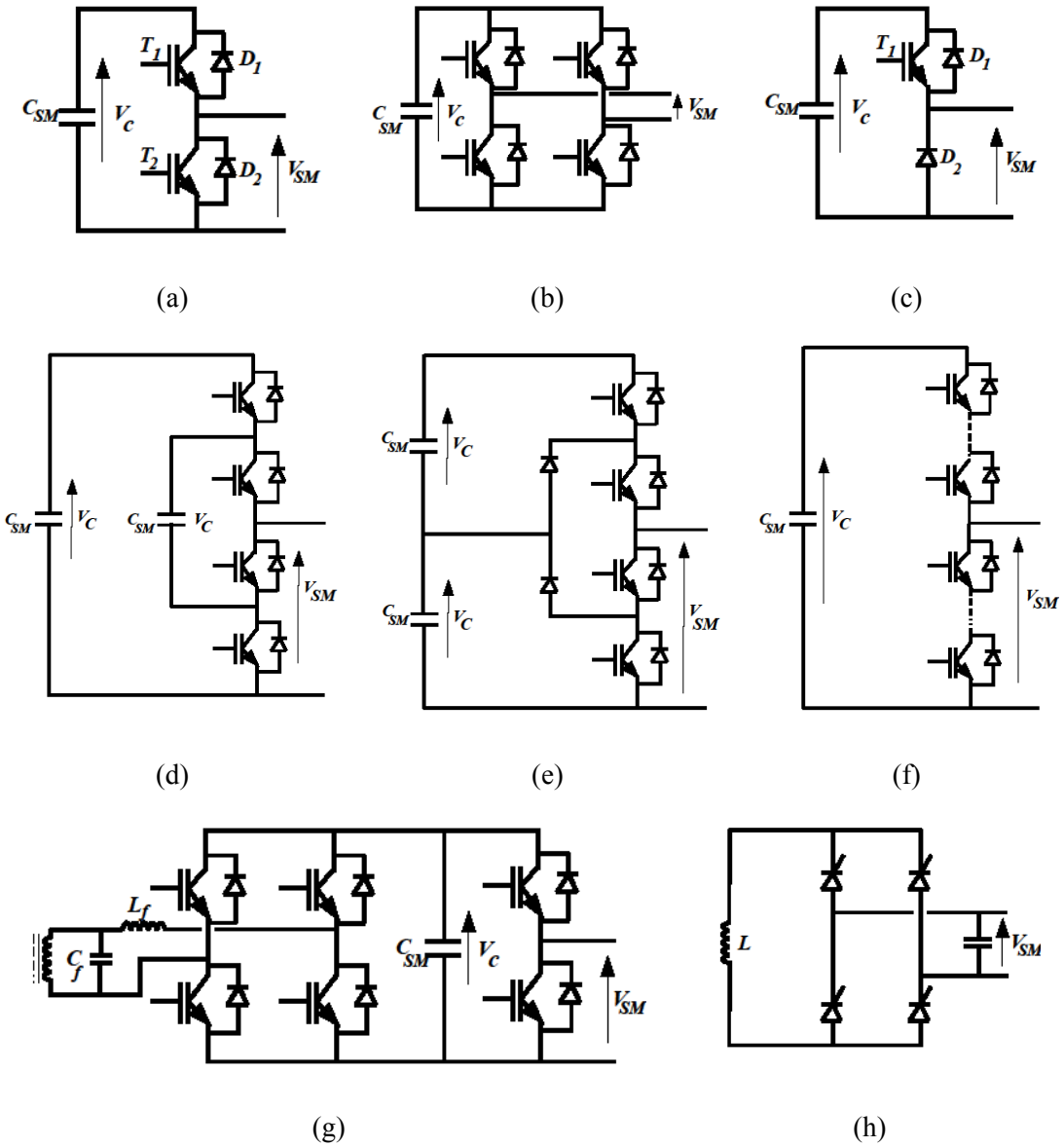


Fig. 1.13: Various sub-module topologies for MMC converter:

(a) Half-bridge (HB) power cell,

(b) Full-bridge (FB) power cell,

(c) Unidirectional cell,

(d) Three-level FC (3L-FC) power cell,

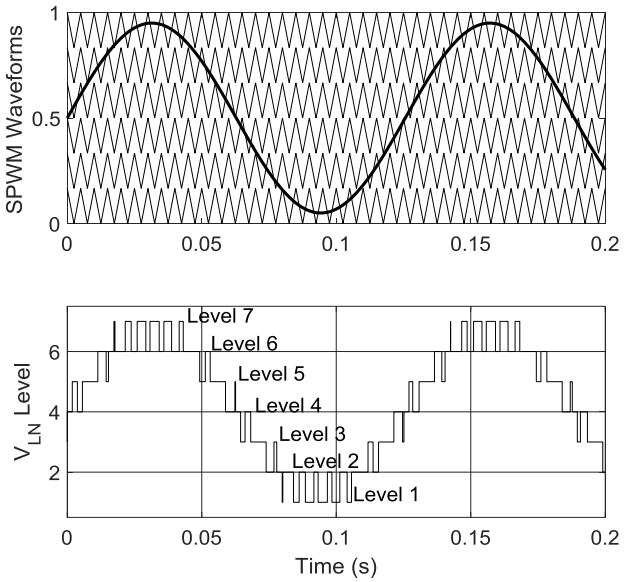
(e) Three-level NPC (3L-NPC) power cell,

(f) Two-level (2L) power cell with numerous power semiconductors in series,

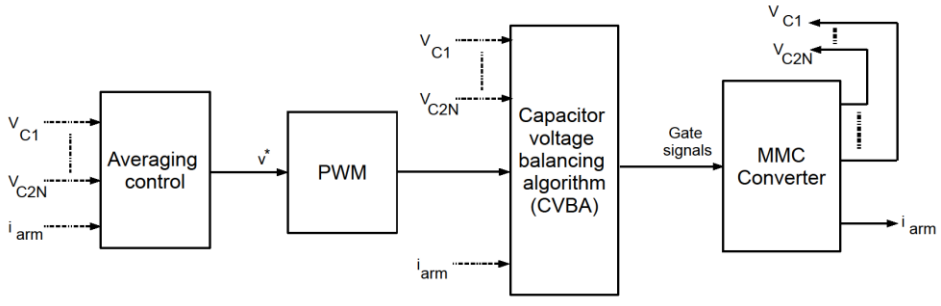
(g) Power cell with resonant inverters for inductive power transfer, and

(h) Current source power cell.

Control (modulation) methods: To ensure the operation of MMC in various applications: modulation methods, averaging control of capacitor voltage, and capacitor voltage balancing control are three mains required tools for internal control of MMC. PS-PWM, PD-PWM, SHE-PWM (Selective Harmonic Eliminated PWM), SV-PWM are applicable modulation methods to generate gate signals of semiconductors in MMC topology. To achieve a natural capacitor voltage balancing, PS-PWM is proposed but its low power quality and high harmonic distortion are inconvenient compared to others (PD-PWM, SHE-PWM, SV-PWM). With high number of sub-modules to produce high voltage level requirements, the complication of high number of different voltage vectors is a critical point for SV-PWM control method. For-low-switching applications, SHE modulation should be used. The main advantage of this method is that the converter switches few times per cycle, reducing the switching losses to a minimum [Jos07]. To obtain an excellent output voltage and excellent power quality of MMC, PD-PWM modulation method is proposed in [Sae10] (see Fig. 1.14a: six HB sub-modules to produce seven-level output phase voltage). But actually, MMC with PD-PWM requires inevitably a capacitor voltage balancing block.



(a)



(c)

Fig. 1.14: Summarizes of internal control of MMC converter:

(a) Example of PD-PWM modulation to produce 7L output phase voltage,

(b) MMC control building blocks.

Adding to PWM modulation, averaging control of capacitor voltage and capacitor voltage balancing control are needed to ensure the MMC operation. An averaging control forces the capacitor voltage of each phase to follow its command (reference value). And the capacitor voltage balancing control balances the sub-module voltages by performing proper selection of which capacitors need to be charged or discharged. In the next section, these two controls are explained in detail. Hence, as summarized here, Fig. 1.14b shows the control building block for MMC converter.

Recent researches: Table 1.9 lists several recent researches about MMC converter topology: different control methods, applications, and also the derived structures.

Table 1.9: List of publications about MMC converter: applications, capacitor voltage balancing algorithms, etc.

Controls and topologies	**Applications**	**Derived structures**
- [Chu11] proposes a novel topology and control strategy of MMC converter by mixing half-bridge (HB-SMs) and a full-bridge (FB-SM) in each arm (positive and negative arms). The main objective of this novel topology is to obtain high output voltage levels compared to the traditional one. In this paper, the control strategies are: averaging control (circulating current control), capacitor voltage balancing control, and PD-PWM to generate signals to HB-SMs and FB-SM. This idea is validated by the simulation results for MV application (V_{dc} = 2.25kV). - [Gao15] proposes the parallel connection of the MMC converters. The objective of the proposed article is to enhance the operational reliability, to help the selection of semiconductors rating and its fault-tolerant operations. Classical control strategies are applied (averaging control, balancing control, PWM method), but must take care about the operation of MMC1 to MMC2. This paper also provides the analysis of harmonics spectrum and total harmonic distortion (THD) of line voltage. - [Ken15] [Gow15] present an	- The original proposed application for MMC is high-voltage direct-current (HVDC) [Mar02] [Mar03]. - [Hag09], [Kol12], and [Ant15] present the MMC converter for drive applications (motor drive, …) - [Spi13] presents the MMC converters for propulsion system of electric ship applications. - …	- [Mar15] presents the advanced topologies of MMC converters, under the names as follow: middle-cell MMC, alternate arm MMC, hybrid MMC, hexagonal MMC, and matrix MMC. - …

insulated bidirectional dc/dc structure based on MMC converters, which takes the role of tape changer. A reference [Gow15] details more about dc/dc converter based on MMCs for a high-voltage high-power dc transfer applications with dc fault insulation capability based on insulated transformer. - [Dan15] presents a fast sorting method for balancing capacitor voltages in MMC converters. This article details an innovative sub-module selection method for the sub-module capacitors' voltage balancing within one arm of MMC. To achieve fast sorting in sub-module selection process, the authors use "the Tortoise and the Hare" sorting method (detail in [Dan15]). This proposed method is validated experimentally on a three-phase 10kVA converter specification. - [Ber13] presents an energy-based controller for HVDC-MMC applications. - …		

Comparison with other multilevel structures: According to references [Mar03], [Roh10], [Lad12], and [Con14], the advantages and disadvantages of MMC are presented as follows:

1) Advantages of MMC are:
   a) Operation's continuities: MMC sub-modules are in series. If few sub-modules stop working, the overall MMC can continue to work.
   b) Modular structure: MMC can scale to different power- and voltage-levels.
   c) Standard machines [Mar15] or grid-connection converters: it is potentially a filterless configuration with high voltage-level and low total distortion harmonic (THD). Moreover, it can use a standard transformer or transformerless for grid connection applications.
   d) High efficiency

2) Disadvantages of MMC converters are:
   a) Higher number of power semiconductor devices.
   b) High energy stored in capacitors.

To support these analyses, articles [Lad12] and [Con14] compare the losses of MMC converter to FCs converter for all operation modes (inverter operating mode, rectifier operating mode, and reactive power compensation mode). These two articles show that MMC total losses are lower than FCs converter. Reference [Lad12] does not present only the comparison of power losses but also the comparison of the stored energy in capacitors. As a result, the total stored energy of distributed capacitors of MMC converter is higher than the FCs one. These results are validated by the simulation works. Moreover, in [Con14], the thermal analysis of one SM is also provided to verify each component losses in one SM.

1.1.5. Conclusion and objectives

Thus, in this dissertation, the MMC converter with HB-SM is the selected topology for MV applications. At first, a pre-dimensioning of this converter for MV applications is presented in the next section. The first objective is to propose an optimization method based on an optimization tool to design MMC in Medium Voltage applications (up to 50kV). So the aim of this section is to propose a generic optimization tool that can optimize the MMC structure for different converter applications. Recently, few articles about the optimization of MMC are proposed [Sok15A] [Sum16] [Arm16]. In this manuscript, the optimization design of MMC depends on the internal control which ensures the operation of MMC (voltage balancing algorithm, circulation current control). So, in the next section, we propose the overall modeling of the MMC (with Half-Bridge Sub-Module) that leads to the optimization process.

1.2. A generic virtual prototyping tool for MMCs converters

This section presents a generic virtual prototyping tool to optimize MMC converters. The objective is to optimize the components of this multilevel converter for medium-voltage applications. Furthermore, the geometry of the arm inductor is proposed and optimized. A generic model of MMCs and an optimization tool implemented in MATLAB^{TM}/Simulink software are presented. Maximize the converter efficiency (η_{mmc}) and minimize the converter volume (vol_{mmc}) define a bi-objective optimization problem. The optimization results are proposed under Pareto fronts' forms: η_{mmc} against vol_{mmc}. Our proposed method is validated by simulation works for two different converter specifications: converter 1 (S_{con1} = 13.85kVA, $V_{ll1,rms}$ = 400V, V_{dc1} = 687V) and converter 2 (S_{con2} = 398kVA, $V_{ll2,rms}$ = 2.3kV, V_{dc2} = 3.9kV).

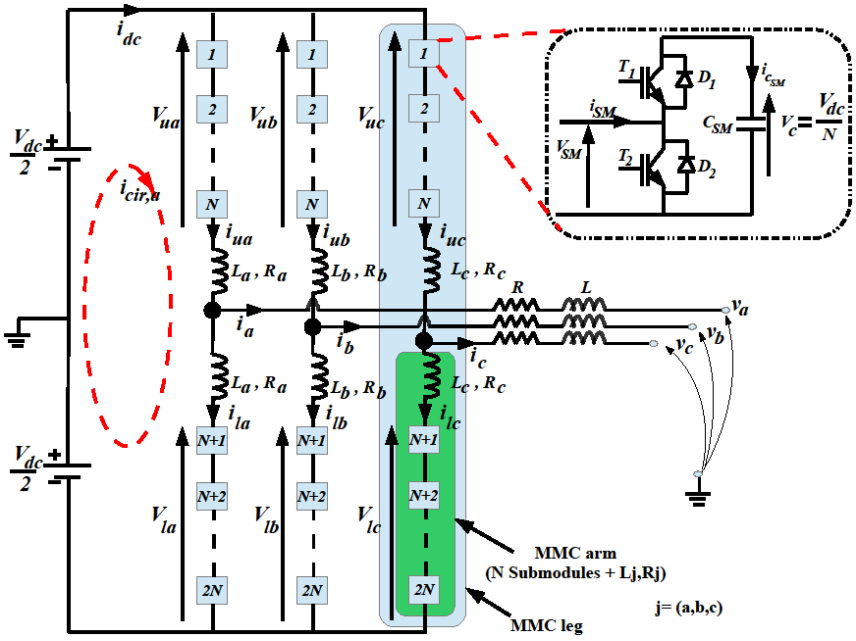
1.2.1. MMC modeling

1.2.1.1. Basic of MMC

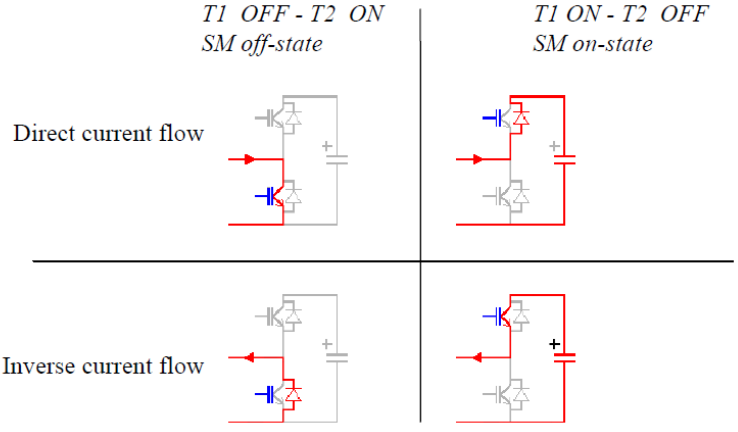
Fig. 1.15a shows the topology of a three-phase MMC with *N* half-bridge sub-modules (HB-SMs). The DC side is modeled by two DC voltage sources $\frac{V_{dc}}{2}$. The three-phase AC side (at the terminal a, b, and c) is modeled by a series connection of R and L.

As presented previously, each SM is composed of two IGBT switches (T_1; T_2), two antiparallel diodes (D_1; D_2), and a capacitor (C_{SM}). As shown in Fig. 1.15b, the SM output voltage V_{SM} has two values (i.e., $V_{SM} = V_C$ when T_1 is switched on and T_2 is switched off, and V_{SM}=0 when T_1 is switched off and T_2 is switched on). That means that each SM has two states in normal operation: switched-on (V_{SM}=V_C) or switched-off (V_{SM}=0).

As shown in Fig. 1.15a, V_{dc} and i_{dc} are the total DC bus voltage and DC current, respectively. v_j and i_j (j = a,b,c) are the converter output phase voltages and the line currents. The SMs in each arm are controlled to generate the required AC phase voltage. According to [Sae10] [Hag11], for ensuring the internal operation of MMC, their circulating current $i_{cir,j}$ must be controlled and the capacitor voltages of each SM must be balanced.



(a)



(b)

Fig. 1.15: MMC topology descriptions:
(a) Three-phase DC/AC MMC inverter with half-bridge sub-module
(b) Sub-Module or cell operation states

According to [Sho12] [Tuq11], the upper (i_{uj}) and lower (i_{lj}) arm currents of each phase can be expressed as a function of the circulating currents (i_{cirj}) and load current (i_j).

$$i_{uj} = i_{cir,j} + \frac{i_j}{2} \tag{1.2}$$

$$i_{lj} = i_{cir,j} - \frac{i_j}{2} \tag{1.3}$$

According to [Tuq11] and (1.2)-(1.3), the MMC can be characterized by the following equations:

$$i_{cir,j} = \frac{i_{uj} + i_{lj}}{2} \tag{1.4}$$

$$i_j = i_{uj} - i_{lj} \tag{1.5}$$

$$v_{cir,j} = \frac{1}{2}\left[V_{dc} - \left(v_{uj} + v_{lj}\right)\right] = L_j \frac{di_{cir,j}}{\mathrm{dt}} + R_j i_{cir,j} \tag{1.6}$$

where v_{cirj}, v_{uj}, v_{lj} are regarded as the inner unbalance voltage, upper arm voltage and lower arm voltage of phase j.

1.2.1.2. MMC control: Pulse-width modulation (PWM) and control loop

The completed controls of MMC must control the DC and AC sides [Per15], the energy transfer of the structure [Ber13], and the internal control (circulating current control and voltage balancing control). The internal control is the essential control part needed to ensure the operation of the converter for all the applications.

The internal control of MMC can be divided into averaging control and capacitor voltage balancing control. In [Hag09], a block diagram for averaging control is shown on Fig. 1.16. This control forces the phase averaging voltage v_{cj} to follow the reference v^*_{cj}, but it does not guarantee the balance of the capacitor voltages. Where v_{cj} is given by:

$$v_{cj} = \frac{1}{2N}\sum_{i=1}^{2N} v_{cji} \;\; ; \quad j = (a,b,c) \tag{1.7}$$

According to (1.6), the circulating current ($i_{cir,j}$) can be directly controlled by regulating the voltage $v_{cir,j}$. The averaging control compares v_{cj} to the reference v^*_{cj}, generating the circulating current $i^*_{cir,j}$ via the primary controller ($C_v(s)$). Then, the measured DC-loop current can follow this generated reference to tune the $v_{cir,j}$ through the second controller $C_i(s)$. For example, when $v^*_{cj} > v_{cj}$, $i^*_{cir,j}$ increases, the function of the inner current loop on Fig. 1. 16 forces the actual circulating current $i_{cir,j}$ to follow its command $i^*_{cir,j}$. As a result, the feedback control of $i_{cir,j}$ enables v_{cj} to follow its command v^*_{cj} without being affected by the current load i_j.

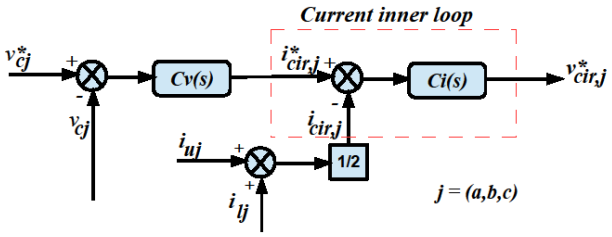


Fig. 1.16: Averaging control proposed by [Hag09]

To generate the gate signal for each SM, several control schemes are proposed. The most implemented is a sinusoidal pulse-width modulation (PWM) technique. As presented in [Deb15], various PWM control techniques such as phase disposition (PD-PWM), phase opposition disposition (POD-PWM), alternate phase opposition disposition (APOD-PWM), phase-shifted carrier (PSC-PWM), and saw-tooth, are studied and compared. This modulation block receives the reference voltage v^*_{uj} (see Fig. 1.17b). As shown in Fig. 1.17b, the number of SMs that need to be switched on for upper arm and lower arm are calculated at this stage. However, the specific SMs to be turned on are not determined yet. The maximum phase voltage ($V_{LN,max}$) are expressed as a function of the modulation index m ($0 \leq m \leq 1$). Thus, the modulation index m can be calculated and inserted into the PWM modulation block.

$$V_{LN,max} = m \times \frac{V_{dc}}{2} \tag{1.8}$$

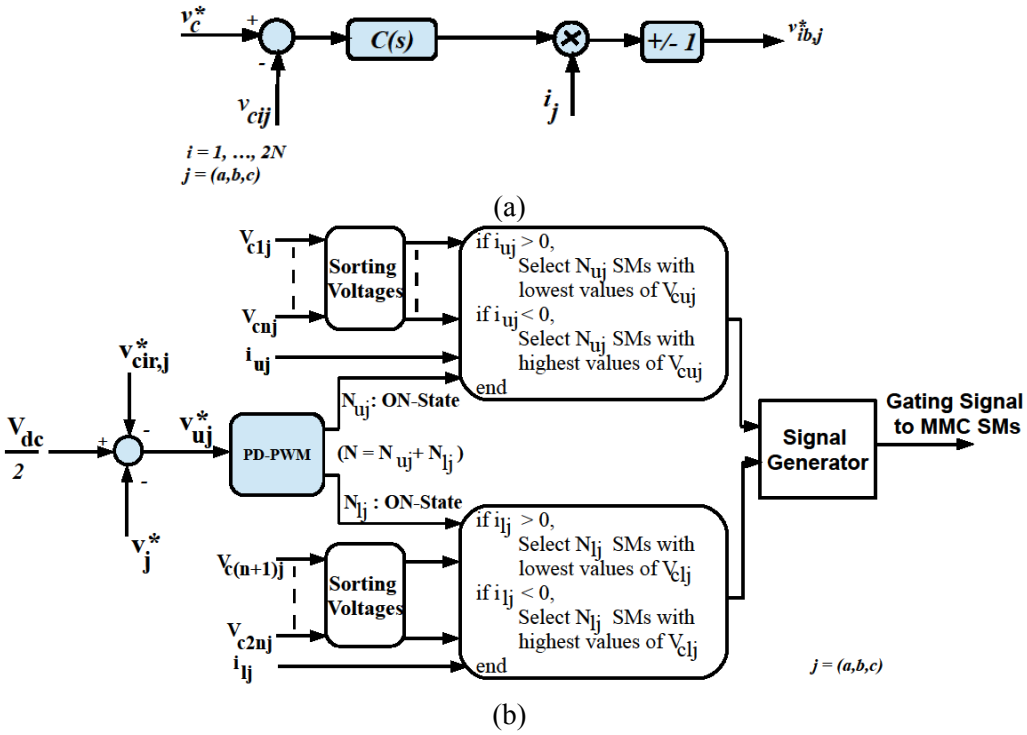


Fig. 1.17: Capacitor voltage balancing control methods:
(a) Individual capacitor voltage balancing (ICVB) proposed by Hagiwara M. [Hag11]
(b) Central capacitor voltage balancing (CCVB) proposed by Saeedifard [Sae10]

The Capacitor Voltage Balancing (CVB) control is needed for proper selection of SMs that should be turned-on. Two most implementations of CVB are:

1) *Individual capacitor voltage balancing (ICVB)* (proposed by: *Hagiwara M., et al.* [Hag09] [Hag11]: Fig. 1.17a shows a block diagram of ICVB control method (also called "local capacitor voltage balancing control method"). The authors propose controller C(s) to force the individual DC capacitor voltage to follow its command v^*_{csm}. As presented in this figure, the balancing control is based either upper- or lower-arm current, thus the polarity of output voltage reference v^*_{ibj} should be changed according to the arm current (see details in [Hag09] [Hag11]). According to [Sho12] and [Hag11], the ICVB with PS-PWM control method requires another control block (called "arm balancing control") for the MMC stability.
2) *Central capacitor voltage balancing (CCVB)* (proposed by: *Saeedifard* and *Iravani* [Sae10]): As presented in Fig. 1.17b, CCVB is implemented just after the modulation block (which decides how many SMs should be turned on). The input of the CCVB algorithm are: the number of turned-on sub-modules (N_{uj} and N_{lj}), the polarities of current arms (i_{uj} and i_{lj}), and the sorting of capacitor voltages (V_{c1j}, …, V_{cnj}). Then, the specific SMs to be turned-on or turned-off are determined. Moreover, as presented in [Deb15] [Hag11] [Sae10], the CCVB with PD-PWM does not need additional control block. So, the CCVB with PD-PWM is selected as the converter control method in this dissertation.

Thus, the completed internal control method (averaging control and capacitor voltage balancing control method) is illustrated in Fig. 1.18.

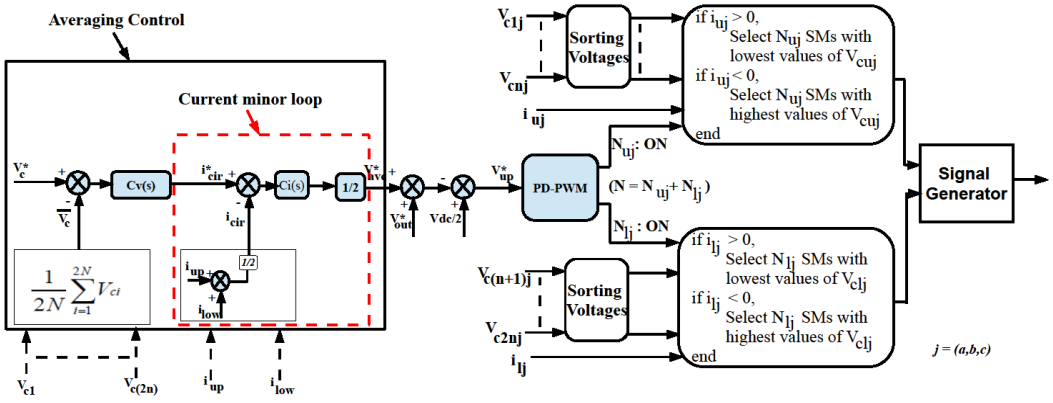
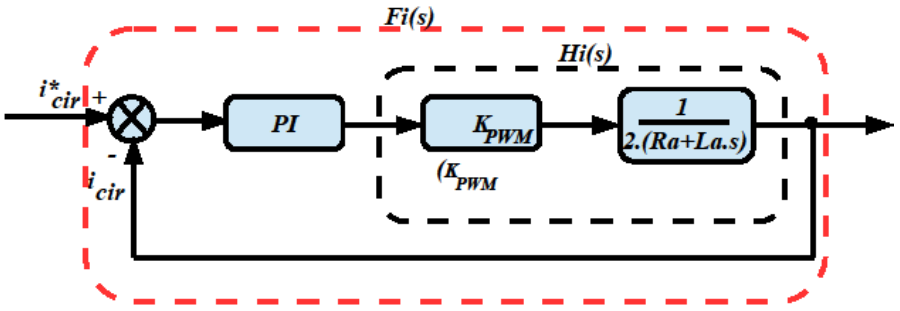
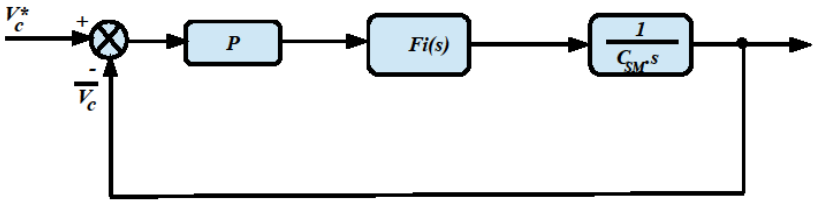


Fig. 1.18: Completed internal control of MMC converter

According to Equation (1.6), the controller gains for the circulating current depend on a series resistance R_a, inductance L_a, and the PWM gain (as shown in Fig. 1.19a). The controller gain for the voltage block can be calculated directly from the capacitor in SM (see Fig. 1.19b). These gains basically depend on L_a, R_a, and C_{SM}.



(a)



(b)

Fig. 1.19: Controller design:
(a) PI control block for circulating current controller
(b) Capacitor voltage control block

1.2.1.3. MMC losses modeling

Maximize the converter efficiency (η_{con}) is set as one of our optimization objective. To achieve this, the converter losses modeling must be computed. This modeling is presented in this sub-section. The approximate semiconductor losses are calculated by using the simulated current waveforms and the semiconductor specifications from the manufacturers. The IGBT and diode on-state voltages and the switching energy losses of the semiconductor devices are approximated by [Roh10]:

$$g_{(i)} = \mathrm{u} + \mathrm{v}\left(\frac{i}{[A]}\right)^{w} \tag{1.9}$$

where i is the simulated device current $i_C(t)$ or $i_F(t)$. g can be a collector-emitter voltage (v_{CE}) or an energy on/off ($E_{on,T}$ and $E_{off,T}$) of IGBTs. g can also be a recovery voltage (v_F) or a recovery energy ($E_{rec,D}$) of anti-parallel diode (see Fig. 1.20a-b). u, v and w are the fitting parameters for voltage and energy of the semiconductor devices. These parameters are calculated by using the characteristic curves of v_{CE}, $E_{on,T}$, $E_{off,T}$, $E_{rec,D}$ as a function of the collector current i_C according to manufacturer's datasheets.

In [Gra08] [Zho14], the MOSFETs and diodes on-state voltage and the energy switching losses of the devices are approximated by:

$$v_{DS}(\mathrm{t}) = R_{on}.i_D(\mathrm{t}) \tag{1.10}$$

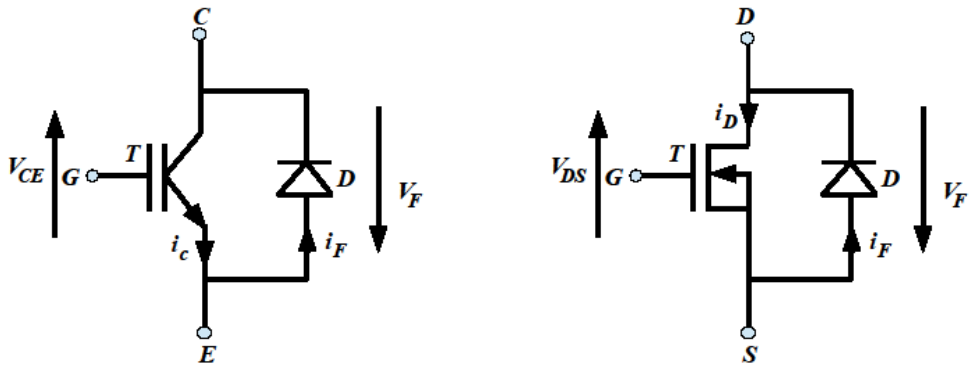
$$v_F(\mathrm{t}) = R_{FO} + R_{don}.i_F(\mathrm{t}) \tag{1.11}$$

$$E_{on,M} \approx V_{DS}(t_{sw}).i_D(\mathrm{t}_{sw}).\frac{t_{fall}}{2} \tag{1.12}$$

$$E_{off,M} \approx V_{DS}(t_{sw}).i_D(\mathrm{t}_{sw}).\frac{t_{rise}}{2} \tag{1.13}$$

$$E_{rec,D} \approx V_F(t_{sw}).Q_{rr} \tag{1.14}$$

where t_{fall}, t_{rise}, Q_{rr} are fall times, rise times and reverse recovery charge, respectively.



(a) (b)

Fig. 1.20: Power semiconductor devices:
(a) IGBT and anti-parallel diode.
(b) MOSFET and anti-parallel diode.

In [Roh10], from Equations (1.9)-(1.14), conduction and switching losses are calculated within one fundamental output time period $2\pi/\omega$ with the simulated currents $i_n(t)$ and the use of characteristic curves and values in manufacturer's datasheets:

$$P_{con,n} = \frac{\omega}{2\pi}\int_{t_s}^{t_s+\frac{\omega}{2\pi}} i_n(\tau)v_n\left(i_n(\tau)\right)\mathrm{d}\tau \tag{1.15}$$

$$P_{sw,n} = \frac{\omega}{2\pi}\sum_{sw,n=1}^{N_{sw,n}}\left[\frac{v_{n,off}(t_x)}{v_{n,ref}}E_n(i_n(t_{sw,n}))\right] \tag{1.16}$$

where *n* can be IGBT part, MOSFET part and diode part. $P_{sw,n}$, $E_{sw,n}$ are the power switching losses and the energy switching losses of device *n*. $E_{sw,n}$ is calculated at each

switching time $t_{sw,n}$. $N_{sw,n}$ are the numbers of all switching events of device n. $v_{n,off}$ and i_n are the simulated voltage and current of the device *n*. The total losses of each part are calculated by Equation (1.17).

$$P_{t,n} = P_{con,n} + P_{sw,n} \tag{1.17}$$

As described in [Kol12] [Mar02], as shown in Equation (1.18), the minimum value required for the capacitor of one cell can be expressed as a function of the maximum pulsation energy (ΔW_{max}), the number of SMs (N), the capacitor voltage ripple (ε_v) and the nominal capacitor voltage ($V_{c,nom}$). The minimum inductor value with PD-PWM Equation (1.19) is expressed as a function of the arm current ripple (ε_i), the switching frequency (f_{sw}), the maximum capacitor voltage ($v_{c,max}$) and the number of SMs (N):

$$C_{SM,min} = \frac{\Delta W_{max}}{N.\varepsilon_v.v_{c,avg}} \tag{1.18}$$

$$L_{j,min} = \frac{0.5}{N.\varepsilon_i.f_{sw}}.\ v_{c,max} \tag{1.19}$$

In [Mir14], capacitor losses are usually calculated considering an equivalent series resistance (ESR) and the capacitor current i_{CSM} (see Fig. 1.15a):

$$ESR = \frac{\tan(\delta)}{C_{SM}\omega} \tag{1.20}$$

$$P_{C,SM} = ESR.i^2_{C_{SM,eff.}} \tag{1.21}$$

where ω is a frequency in radians and tan(δ) is a loss angle which is nearly constant for each type of dielectric materials.

In this thesis manuscript, the authors propose the geometry of the arm inductor as shown in Fig. 1.21. Then the inductor losses (core loss Steinmetz Equation (1.22) [Ven02]) and winding losses Equation (1.24) are computed as a function of its geometry variables, arm currents (i_{uj}, i_{lj}), and also materials (details are given in [Lef12]). Thus, the total inductor losses is the sum of core losses and winding losses as shown in Equation (1.25).

$$P_{iron,vol}\left[{}^{W}/_{cm^3}\right] = k.f_s^{\alpha}.B_M^{\beta} \tag{1.22}$$

$$vol_{core}[m^3] = 4S\left(\sqrt{S} + \sqrt{A} - {}^{e}/_{4}\right) \tag{1.23}$$

$$P_{copper} = r_{winding}.i^2_{uj,eff}\ ,\quad \mathrm{j} = (\mathrm{a},\mathrm{b},\mathrm{c}) \tag{1.24}$$

$$P_{t,ind} = P_{iron,vol} \times vol_{core} + P_{copper} \tag{1.25}$$

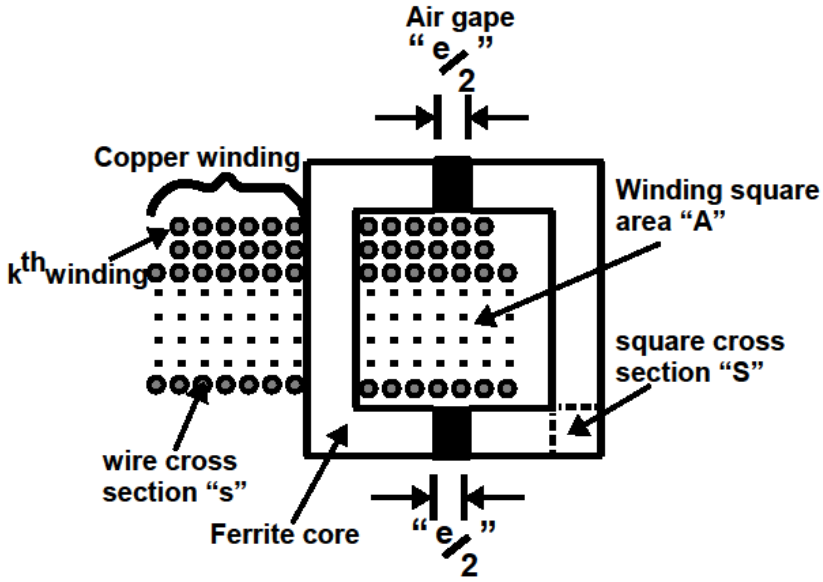


Fig. 1.21: Geometry of inductor.

where k, α, and β are coefficients that depend on core material, operating frequency and core shape [Sul11]. S, A, and e are square cross section of ferrite core, winding square area, and air gap of inductor design respectively.

These geometric variables will be defined as optimization variables and are described in Section 1.2.2. The overall losses of MMC is given by Equation (1.26):

$$P_{t,MMC} = 6 \times (N(P_{t,n1} + P_{t,n2} + P_{C,SM}) + P_{t,ind}) \quad (1.26)$$

$$\text{where, } P_{t,n1} = P_{t,T1} + P_{t,D1} \text{ or } P_{t,n1} = P_{t,M1} + P_{t,D1} \quad (1.27)$$

$$P_{t,n2} = P_{t,T2} + P_{t,D2} \text{ or } P_{t,n2} = P_{t,M2} + P_{t,D2} \quad (1.28)$$

1.2.1.4. Thermal and heat-sink modeling

The equivalent thermal circuit diagram presented in [Roh10] is used to calculate the junction temperature of semiconductor devices in SM-MMC (sub-module MMC). Furthermore, for the same objective, [Qin11] proposed the power loss calculation with junction temperature feedback. In this dissertation, the thermal diagram is used to calculate the thermal resistance R_{thhs}. Thanks to the datasheet of the heat-sink and its analytical model (1.29), its length L_{hs} and its volume can be calculated as shown in Fig. 1.22 [Lef12]. Where a_{hs}, b_{hs}, c_{hs} are fitting parameters of the heat-sink from manufacturer's datasheets (details in [Lef12] [Sok15A]).

$$R_{thhs}(L_{hs}) = a_{hs} + b_{hs}e^{-c_{hs}L_{hs}} \quad (1.29)$$

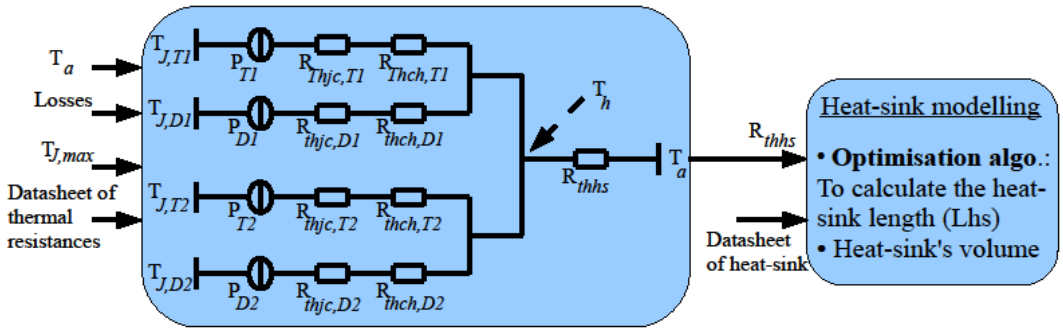


Fig. 1.22: Thermal and heat-sink modeling.

1.2.2. Pre-dimensioning design for MMCs

In this sub-section, we present the optimization problem such as: objectives, variables and parameters, constraints, optimization tool and its process. Then some converter specifications are proposed in order to validate our generic design to optimize MMC converters.

1.2.2.1. Optimization design description

Optimization objective: Maximizing the converter efficiency (η_{MMC}) and minimizing the overall volume (Vol_{MMC}) is defined as a bi-objective optimization problem:

$$P_{out} = \left|\sqrt{3} \times V_{LL,rms} \times I_{p,rms} \times \cos(\varphi)\right| \tag{1.30}$$

$$\eta_{MMC} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{t,MMC}} \tag{1.31}$$

$$Vol_{MMC} = Vol_{t,hs} + Vol_{t,capa} + Vol_{t,ind} \tag{1.32}$$

where $Vol_{t,hs}$, $Vol_{t,capa}$, $Vol_{t,ind}$ are the total volume of heat-sinks, capacitors, and inductors. The volume calculation of heat-sink and capacitor are based on manufacturer's datasheets. The calculation of the inductor volume is computed by its geometry as proposed in Fig. 1.21.

Table 1.10: Design converter specifications

Converter 1		**Converter 2**	
$V_{LL,rms}$	400V	$V_{LL,rms}$	2.3kV
$I_{p,rms}$	20A	$I_{p,rms}$	100A
V_{dc}	687V	V_{dc}	3.9kV
S_{out}/ Cos(φ)	13.85kVA/0.95	S_{out}/ Cos(φ)	398kVA/0.95
m	0.95	m	0.95

To validate the generic prototyping tool, two converter specifications are proposed in Table 1.10. Then, the simulation results are presented in Section 1.2.3.

Optimization variables: the number of SMs (N_{SM}) is defined as an optimization variable. In Section 1.2.1.3, the minimum required value for capacitor and arm inductor are calculated individually. However, in some converter applications, these minimum values are not the accurate selection criteria. The paper [Zyg13] shows the relationship between these two variables. That is why C_{SM} and L_j should be considered as optimization variables. Numerous heat-sinks (N_{hs}) from manufacturers are also introduced in the optimization process and regarded as one of optimization's variables. The carrier frequency (f_c) is also considered as an optimization variable for the compromise between converter efficiency and THD of the output voltage. Finally, some geometry inductor variables such as air gap (e), wire cross section (s), core square cross section (S), winding square area (A), and wire turn numbers (n_l) are defined as optimization variables. Thus, the eleven optimization variables are defined in the vector X and are presented in the following list:

$$X = (N_{SM}, T_{semi}, C_{SM}, L_j, N_{hs}, f_c, e, A, S, s\ n_l)^t$$

- $N_{SM} \in \{2, 3, 4, 5, 6 , 7, 8, 9, 10, 11, 12, 13, 14, 15\}$;
- T_{semi}: table of semiconductor devices;
- $C_{SM} \in [0.1mF,10mF]$;
- $L_j \in [0.1mH, 10mH]$;
- $N_{hs} \in \{1, \ldots, 15\}$ list of 15 types of heat-sink ;
- $f_c \in \{1kHz, \ldots , 10kHz\}$;
- $e \in [0, 5mm]$;
- $A \in [10^{-4}m^2, 100x10^{-4}m^2]$;
- $S \in [10^{-6}m^2,36x10^{-4}m^2]$;
- $s \in [10^{-7}m^{2,}\ 16x10^{-6}m^2]$;
- $n_l \in [1, 200]$.

Optimization constraints: in this optimization design, some optimization constraints over electrical, thermal, geometric and operating conditions are considered as follow and summarized in Table 1.11.

Table 1.11: Optimization design constraints

Quantity	**Constraints**
Cell capacitor	$C_{SM,min} \leq C_{SM}$
Arm inductor	$L_{j,min} \leq L_j$
THD of phase voltage	THD≤14%
Semiconductor	$V_{SM} \leq V_{semi,ref}$
Junction temperature	$T_j \leq T_{j,max}$
Current density	$J \leq 10A/mm^2$
Inductor geometric	$n_l.s < k_w.A$
Heat-sink length	$L_{semi} < L_{hs}$

- *Electrical*: the cell capacitor and arm inductor selection must be greater than its minimum values as described in the previous section (with ε_v = 10% and ε_i = 10%). Moreover, the reference voltage of semiconductor ($V_{semi,ref}$) must be higher than SM voltage (V_{SM}). In [Fal14], the total harmonic distortion (THD) of the phase voltage is studied. In this manuscript, the THD is set as one of the constraints.
- *Thermal*: the junction temperature T_j of the system must not exceed a maximum junction temperature that is imposed by the device manufacturers ($T_{j,max}$).
- *Current density*: the current density (J) in the copper wire must be lower than 10A/mm^2, to avoid excessive temperature rise in the inductor wire.
- *Inductance*: the geometric variables are independent. Equation (1.33) presents the geometric constraint for the inductor. This constrain must ensure that the area of the wire section multiplied by the number of windings must be lower than the winding area window A (considering a filling factor k_w). The 3F3 power material is used as the magnetic material.

$$n_l . \mathrm{s} < k_w . \mathrm{A} \tag{1.33}$$

- *Length*: the heat-sink length (L_{hs}) must be longer than the maximum semiconductor length (L_{semi}).

1.2.2.2. Optimization tool and process

Optimization tool: Several optimization methods are discussed in [Mir14]. The MMC modeling is implemented with MATLAB/Simulink. Some variables being continuous and some being discrete, a mixed integer programming problem is considered. According to [Mir14], the stochastic Genetic Algorithm (GA) method is a suitable choice to solve this optimization problem and especially in power electronics [Sok15B] [Sok15A]. A NGPM-NSGA-II program in MATLAB, proposed in [Lin11], is used to solve this bi-objective problem. Finally, the Pareto fronts are proposed and discussed in the next section.

Optimization process: Fig. 1.23 shows an optimization flowchart for this pre-dimensioning design. The IGBTs, MOSFETs, heat-sinks, and capacitors databases are classified and summarized in Appendix A.

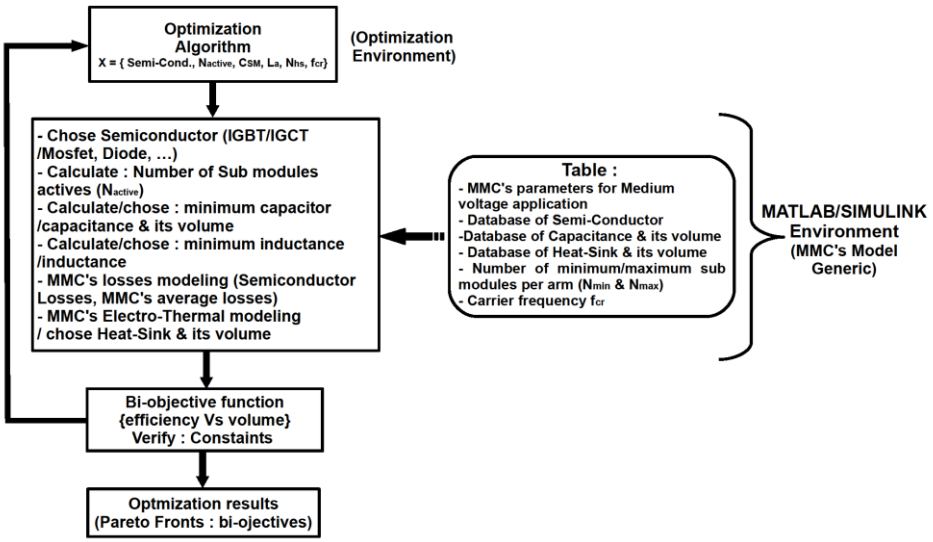


Fig. 1.23: Optimization flowchart

1.2.3. Optimization results

In this section, the optimization results for two converter specifications are presented and analyzed in detail. The selection of the optimal solution is reached by the help of a posterior analysis.

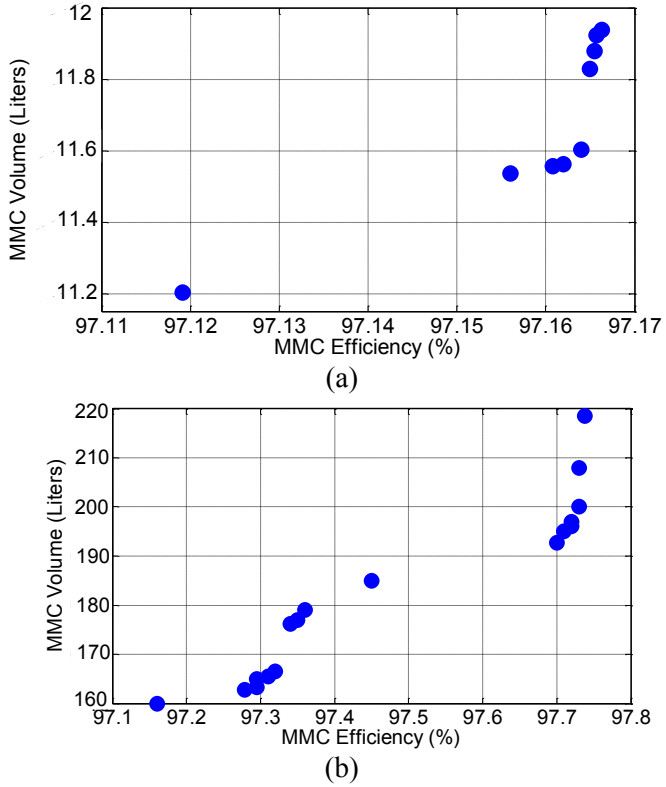


Fig. 1.24: Pareto fronts' results:
(a) Design converter 1, S=13.85kVA, V_{dc}=687V
(b) Design converter 2, S=398kVA, V_{dc} = 3.9kV.

1.2.3.1. Pareto fronts' results

The GA parameters are: 50 generations and 20 individuals (24 hours of computational time with DELL Intel Core 2). For a generic optimization tool, two Pareto fronts for two different converter applications are illustrated. For each Pareto front, the number of points in the Pareto front depends on the number of individuals and generations. Thus, the designer cannot set, a priori, the number of points on the Pareto front. Fig. 1.24a and Fig. 1.24b represent the Pareto fronts of converter 1 and converter 2, respectively:

- Converter 1 (S_1 = 13.85kVA, V_{dc1} = 687V, $V_{ll1,rms}$ = 400V): Pareto front provides 9 optimal solutions from the last generation. The converter efficiency and its volume vary from 97.1% to 97.165% and from 11 to 12 liters.
- Converter 2 (S_2 = 398kVA, V_{dc2} = 3.9kV, $V_{ll2,rms}$ = 2.4kV): Pareto front provides 17 optimal solutions. The converter efficiency and the converter volume are in the range from 97.14% to 97.78% and from 160 to 218 liters, respectively.

1.2.3.2. Optimization solution discussions

The converter efficiency is mainly limited by the THD constraint. This constraint leads to have a higher number of SMs or to increase the switching frequency which leads to increase the converter losses. Nevertheless, the advantages of this constraint are the reduction of the cost and the size of the output filter stage. For example, 4 SMs per arm for converter 2, its efficiency is higher than 99% but its THD of phase voltage is higher than 35%. So the converter needs a large output filter stage. Whereas, all optimal solutions, the converter efficiency is between 97.14% and 97.78% but its THD is below 14% which is a compromise of the output filter design.

To further analyze optimization solutions, the optimization results of converter 2 are deeply described. As mentioned in the previous section, THD constraint is a major factor for converter efficiency evolution. The four variables (N_{SM}, C_{SM}, L_{arm}, F_{cr}) from eleven variables of the vector X are the main candidates to ensure the THD level to stay below a limit. As shown in Fig. 1.25a, N_{SM} is equal to nine or ten. Actually, this variable could be higher than ten that surely would give a very low THD but would increase the converter power losses. Unfortunately, that would lead to decrease the converter efficiency that we want to maximize. According to 17 optimal solutions in the Pareto front, the evolution of C_{SM} results is between 6mF to 7.6mF (Fig. 1.25b). In Fig. 1.25c, we can notice that L_{arm} varies from 2.5mH to 4.6mH. Fig. 1.25d shows that the variable F_{cr} does not vary so as to minimize switching losses of active components. And Fig. 1.25e-i are the evolution results of the inductor geometric variables (e, S, A, s, n_l). These solutions must verify the optimization constraints (see Table 1.11).

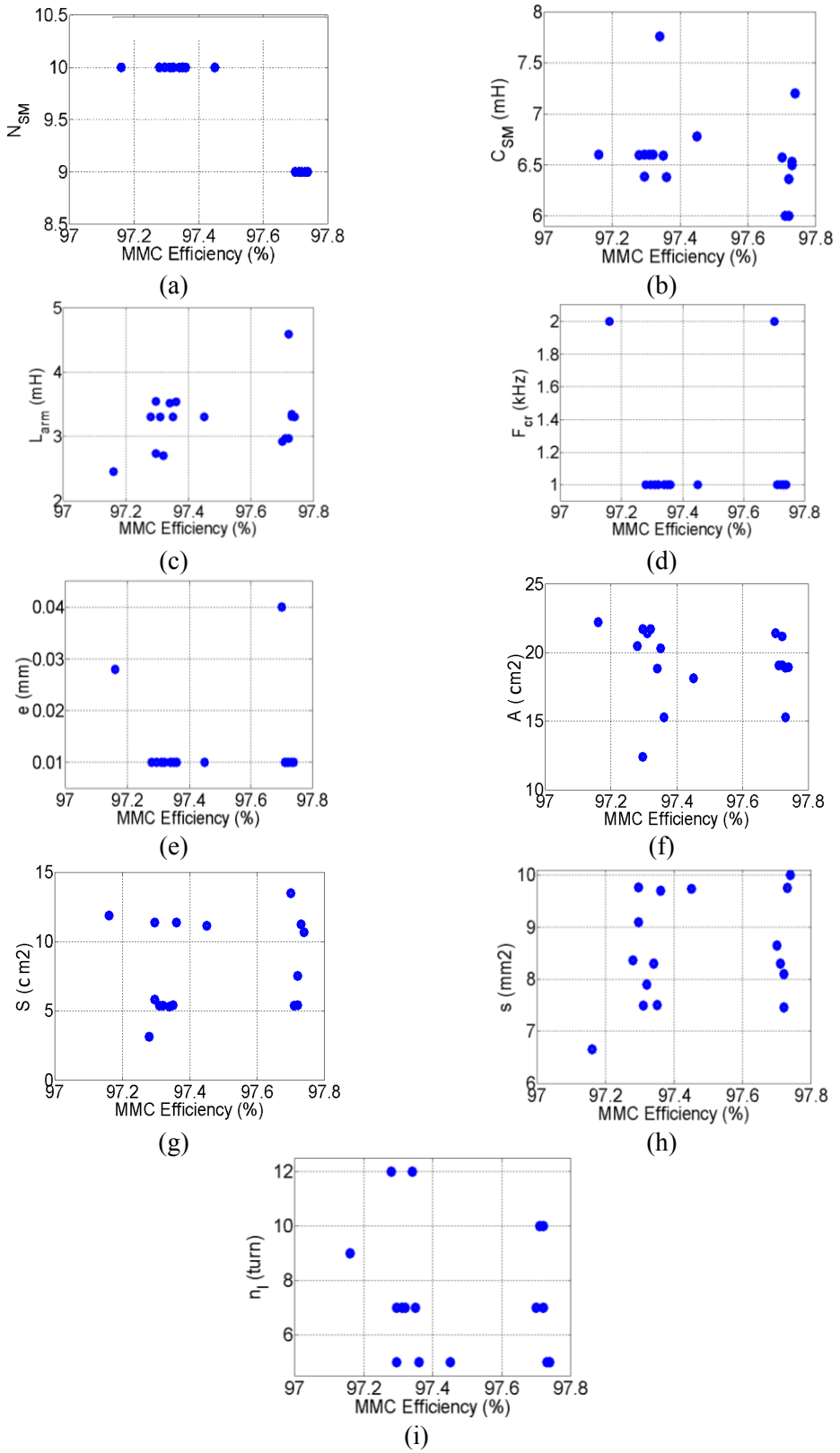
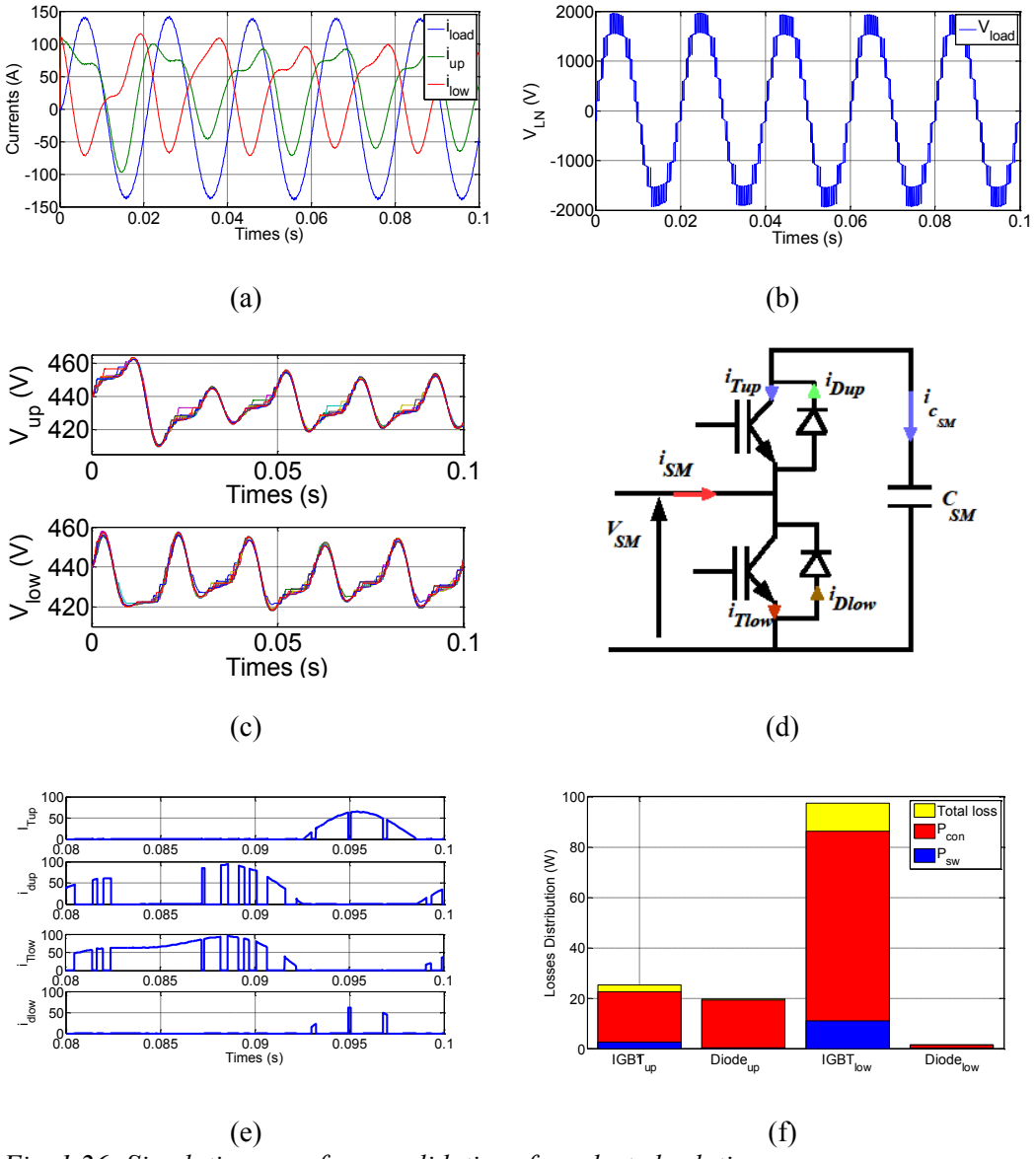


Fig. 1.25: Results of each optimization variable which corresponds to the 17 solutions for the converter 2 (Fig. 1.24b: Pareto fronts results of converter 2).



(a) (b)

(c) (d)

(e) (f)

Fig. 1.26: Simulation waveforms validations for selected solution:

(a) Current waveforms: i_{load}, i_{up}, and i_{low}

(b) 10- levels line-to-neutral voltage for nine SMs per arm

(c) Capacitor voltage balancing for upper and lower arm in one phase

(d) Current definition of one SM

(e) Current waveforms for each component in one SM

(f) Corresponding losses of each component in one SM.

The selection of an optimal point from the Pareto front is, normally, based on the choice of designers or sometime is based on the external special constraints [Sok15B]. Here, we chose the efficiency to be the priority criterion. So, some electrical waveforms of this optimal point (η_{MMC} = 97.78% and Vol_{MMC} = 218 liters from converter 2: S_2 = 398kVA, V_{dc2} = 3.9kV, $V_{ll2,rms}$ = 2.4kV) are presented. Fig. 1.26a-c show the output current and branch current waveforms, ten levels line-neutral voltages ($V_{LN,max} = mV_{dc}/N$ =1.85kV), and waveforms of capacitor voltages ($V_{CSM} = V_{dc}/N$ = 433V), respectively. Furthermore, Fig. 1.26d presents the definition of current path through each component in one SM. Their corresponding waveforms are illustrated in Fig. 1.26e that lead to assume that the power losses in the lower IGBT are the highest amongst other. In contract to this, its anti-parallel diode power losses are the lowest one. These analyses are validated with the power losses diagram of each component in one SM in Fig. 1.26f.

As shown in Table 1.12, the majority of MMC losses are semiconductor losses. Moreover, nearly 90% of losses are conduction losses. These results match to the results of converters losses calculations in [Roh10] [Zho14].

Table 1.12: MMC loss and volume distributions of converter

Optimal	Losses	Volumes
η_{MMC} = 97.78% Vol_{MMC} = 0.218m^3	P_{sw} = 750W; (9.9%) P_{con} = 7kW; (89%) P_{CSM} = 10W; (0.1%) $P_{t,ind}$ = 65W; (1%) $P_{t,MMC}$ = 7.825kW	Capacitor 0.1063m^3; (49%) Heat-sink 0.106 m^3; (49%) Inductor 0.003 m^3; (2%)

1.2.4. Conclusion

We propose a generic virtual prototyping tool to optimize the MMCs. In order to achieve this goal, two main important parts are needed: a generic model of MMC and an optimization tool. Maximize the converter efficiency and minimize its volume define a bi-objective optimization problem. The optimization variables and constraints in the system are discussed. The optimization tool allows analyzing the Pareto fronts. To validate a generic virtual prototyping tool, two different converters specifications are optimized: 13.85kVA and 398kVA. Optimization solutions are illustrated in Pareto fronts.

After the global MMC structure is pre-determined, we look inside one sub-module about its fundamental auxiliary functions (IGBTs gate driver functions). They are introduced shortly in the following section and detailed in the next chapter.

A high galvanic insulation voltage gate driver system (signals transmission, power transmission, protections and defaults information transmission) of IGBT or MOSFET in one SM will be proposed and optimized for MMC in medium voltage applications (where the DC voltage is up to 50kV).

1.3. Introduction to gate drivers for IGBT modules in MMC-MVDC (Medium-voltage direct current) applications

In this section, we present the main requirements of gate drivers for IGBT in MMC-MVDC applications. Moreover, the discussions about the IGBT gate drivers topologies are provided.

1.3.1. Requirements and challenges for IGBT gate drivers in MMC-MVDC applications

As presented in Fig. 1.27, the galvanic insulation level is equal to the DC bus voltage. In case of V_{dc} up to 50kV, there are multiple challenges for gate drivers designs such as: insulation technologies (optical, capacitive coupling, planar transformer, coreless transformer, ceramic etc.), gate driver topologies, etc. Moreover, the optimization aspect consideration is also a major concern. The function of a gate driver is not just to transmit the orders but also to provide the power supply, protect the IGBT module, and return the status of the switch (see Fig. 1.27). Thus, the IGBT gate drivers for high insulation voltage capabilities designs are detailed in Chapter 2.

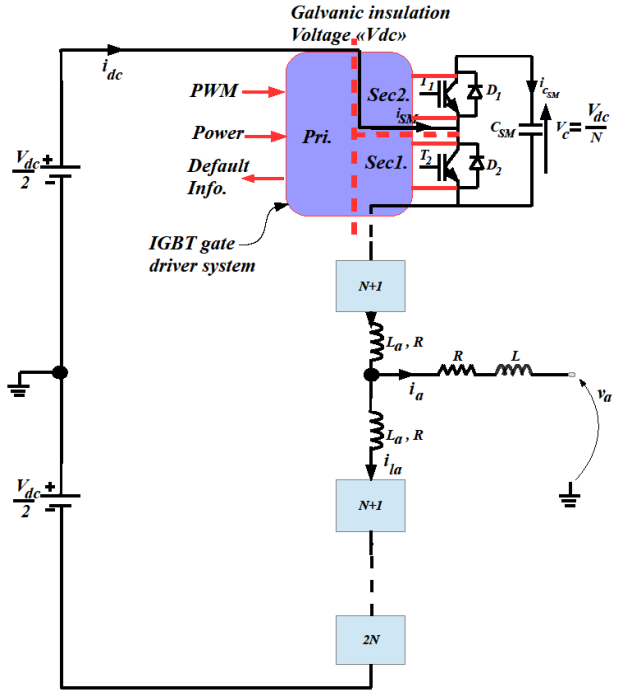


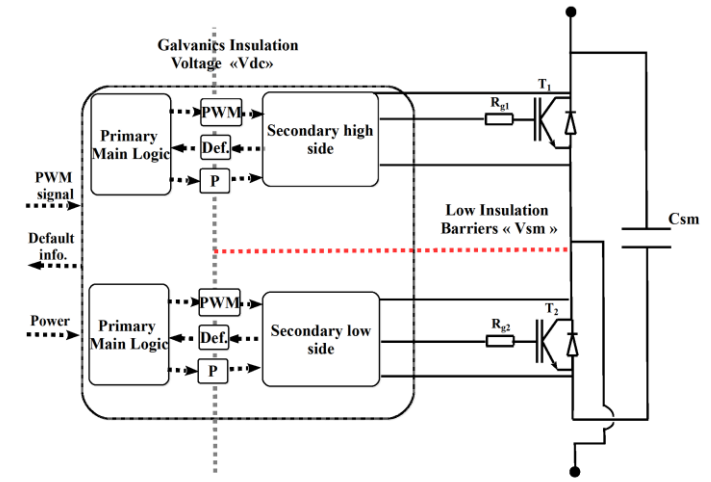
Fig. 1.27: Synopsis of IGBT gate drivers: proposed IGBT gate drivers for one SM with determined galvanic insulation voltage level (V_{dc})

1.3.2. General synopsis of IGBT gate drivers for a sub-module (SM) of MMC-MVDC applications

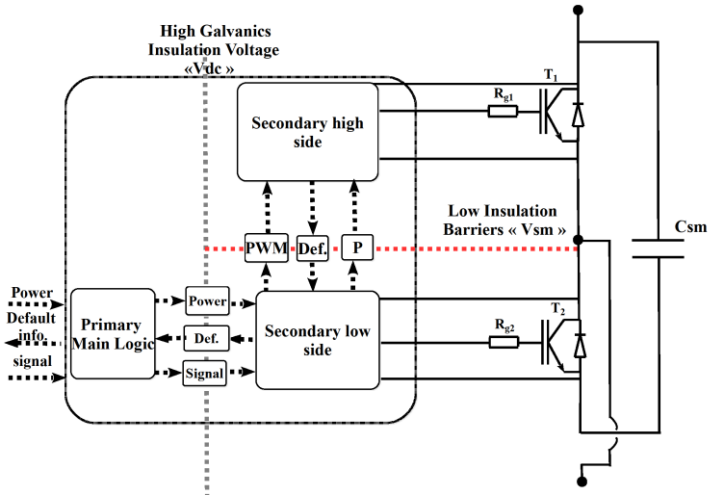
Fig. 1.28a and Fig. 1.28b show two synopsizes of IGBT gate drivers for one SM of MMC. Basically, in one SM (see Fig. 1.13a), there are two insulated groups of signals to transfer by the help of IGBTs' gate drivers. To design these gate drivers' systems, we can

perform with a classical solution (see Fig. 1.28a) and a challenge solution (see Fig. 1.28b). We have two different insulation voltage levels: one is a high galvanic insulation (V_{dc}) and another one is a low insulation voltage level (V_{SM}).

For example, a MV-MMC converter specification: V_{dc} = 15kV, and N_{SM} = 10 per arm. So, $V_{SM} = V_{dc}/N_{SM}$ = 15kV/10 = 1.5kV. Thus, V_{dc} = 15kV and V_{SM} = 1.5kV are a high- and low-insulation voltage requirements, respectively. In Fig. 1.28b; all the information such as PWM, power supply, defaults are transmitted from primary side to the secondary side through high insulation barrier (V_{dc}) for the lower IGBT. Then, at secondary side, the information is forwarded from the lower IGBT to the higher IGBT through a lower barrier insulation voltage level (V_{SM}). This technique provides us several advantages compared to the classical method as in Fig. 1.28a: reduction of the size of the overall gate drivers, reduction of electromagnetic immunities (EMI) problems (reduced common-mode circulating current in SM structure [Ngu16]).



(a)



(b)

Fig. 1.28: Synopsis of IGBT gate drivers:

(a) Classical solution for high insulation voltage IGBT gate driver in one SM

(b) Challenging solution for high insulation voltage IGBT gate driver in one SM

1.4. Conclusion

This chapter presents a global optimization of MMCs for MV applications with the help of a generic virtual prototyping tool (generic modeling of MMC converters and optimization tool). Generic converter modeling and optimization tools are implemented in MATLAB^{TM}/Simulink. Maximizing the converter efficiency and minimizing its volume are set as a bi-objective problem to be solved with respect to numerous constraints.

To validate our proposed MMC optimization designs, two different converter specifications (converter 1: S_1 = 13.85kVA, V_{dc} = 687V, $V_{ll,rms}$ = 400V. Converter 2: S_2 = 398kVA, V_{dc} = 3.9kV, V_{llrms} = 2.3kV) are considered. The optimization results under Pareto fronts for each proposed converter were shown. Then, the detailed analyses of these results were also mentioned.

After pre-dimensioning MMC converters, we look inside a power cell (Sub-Module) design for MV-applications of this multilevel converter. So, at the end of this chapter, we provide the challenge design of power semiconductor gate drivers and also limitation of galvanic insulation for safety reason. As a result, high galvanic insulation capability of power device gate drivers design is required for MV-MMC applications. Two feasible gate driver topologies are discussed by taking into account high- and low-insulation considerations. Actually, the gate driver system should be optimized and will be presented in the next chapter.

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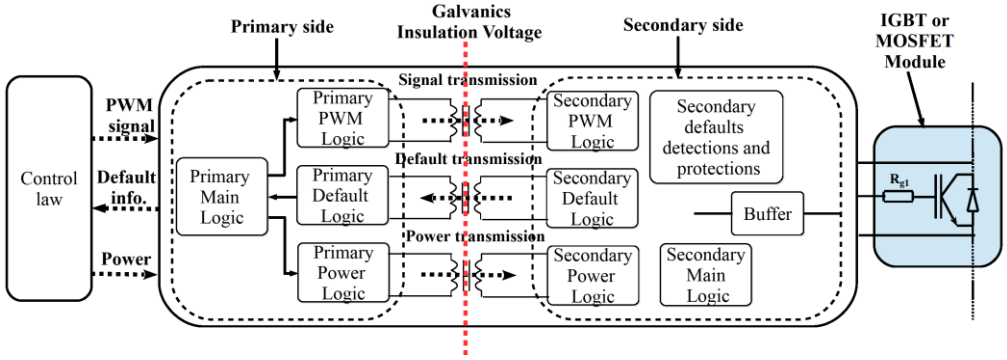
Chapter 2:

Design methodology to optimize gate drivers for IGBT modules for high insulation voltage capabilities

2.1. Introduction

In this chapter, we present the design methodology to optimize gate drivers for IGBT modules for high insulation voltage capabilities. As depicted in Fig. 2.1, the synopsis and functions of a single and a dual channel for Insulated Gate Bipolar Transistor (IGBT) gate driver are: (i) signals transmission, (ii) defaults transmission, (iii) power transmission and (iv) protections [Sok14], [Sok15B], [Sok16C]. The protections and defaults transmission functions are clearly demonstrated in the manuscript thesis [Lef05]. This thesis dissertation details the optimization design of signal transmission function and a power transmission function for IGBT gate drivers for high galvanic insulation voltage for Medium Voltage (MV) converter applications (where the DC voltage is up to 50kV).



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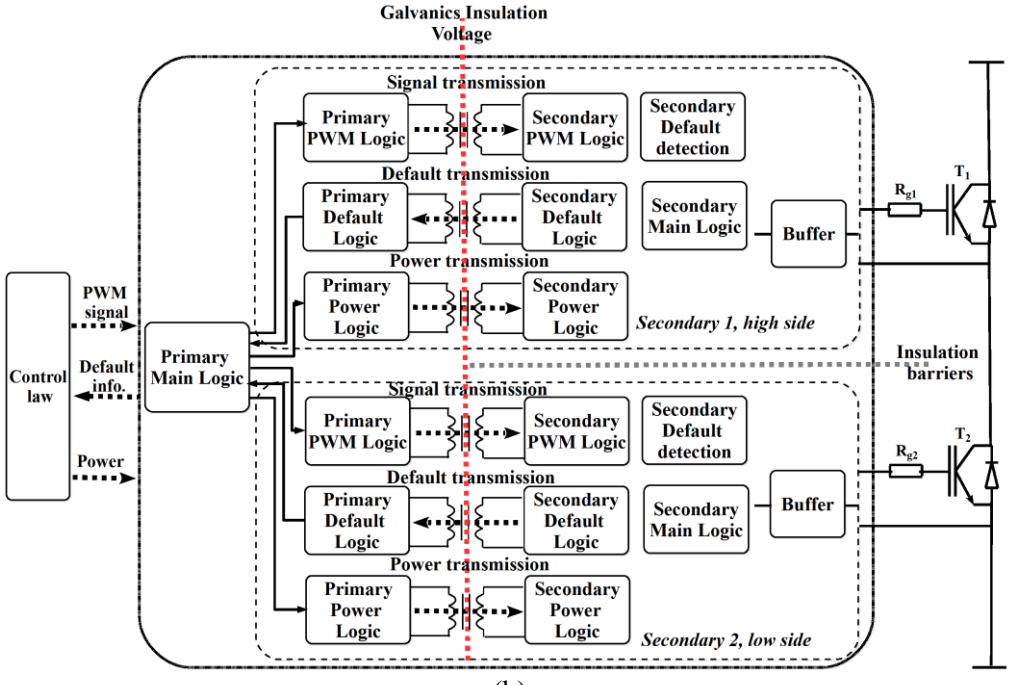


(b)

Fig. 2.1.: Synopsis of:
(a) a single channel IGBT gate driver,
(b) a dual channel IGBT gate driver.

This chapter is organized into five sections as summarized here:

Section 2.1 is about high galvanic insulation voltage techniques and technologies. In this section, some insulation technologies (such as planar transformer, piezoelectric, optical insulation, etc) are briefly compared for high insulation voltage up to 50kV applications. Then, based on numerous publications, a planar transformer is chosen. The air gap length and its dielectric material are the main factors to determine the insulation voltage level. Moreover, this section studies also the geometries of transformers and dielectric materials which provide the best performances for signal transmission function and high efficiency of a DC-DC converter for power supply function. Then, the validation of the insulation material is provided by experimental works. Furthermore, simulation and experimental results are illustrated to support our transformer selection.

Section 2.2 details the optimization design for a high galvanic insulation signal transmission function. First, the signal transmission topology is described. After that, the study is about the optimization of the selected circuit. The objectives of the study are to optimize the geometrical aspects of the planar transformer and its associated components in the circuit by the help of an optimization tool (genetic algorithm (GA)). The same optimization philosophy is also applied for the power supply topology in Section 2.3.

Section 2.4 presents the concept of the intelligent gate driver systems which can measure the voltage states of a sub-module of a modular multi-level converter (SB-MMC). The advantages of this proposed smart gate drivers are to help the internal control methods (such as voltage balancing algorithm). As presented in Chapter 1, the capacitor voltage balancing control requires the online capacitor voltages (with the help of voltage sensors) from sub-modules. Thus, in this chapter, a novel capacitor voltage balancing algorithm with capacitor voltage states (with the help of gate drivers) is proposed.

And Section 2.5 concludes this chapter and also provides the inherent perspectives for the future works.

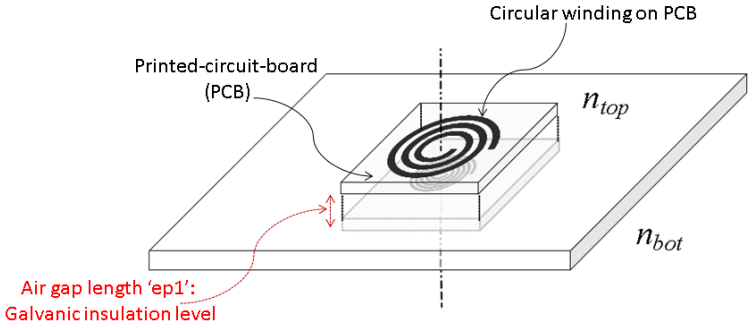
2.2. High galvanic insulation voltage techniques and technologies

In this section, we present the comparison of galvanic insulation technologies. Finally, the high insulation voltage system is based on a planar transformer. Different transformers are compared until the suitable one is selected. The studies of several insulation materials are provided. Moreover, experimental validations are also mentioned in order to clarify the insulator choice.

2.2.1. Comparison of galvanic insulation technologies

As previously mentioned, for the applications of IGBT modules in Medium Voltage (MV) converters or multilevel converters, gate drivers require high galvanic insulation capabilities for the safety and long product life reasons. The galvanic insulation capability can be performed through technologies such as: magnetic field of ferrite core

planar transformers [Sok15B] [Sok16A] [Sok16B] [Lef13], magnetic field of coreless transformer [Tang01] [Tang99], optical insulation system [Rou11] [Fuj13], and piezoelectric coupling [Vas06]. According to [Wan11], the optical insulation devices such as optocoupler have a limited range of operating temperature, generally less than 100 °C. In addition to this, as discussed in [Hei98] [Fuj13] [Vaf12], the optically power supply is today impractical (for few Watts) because of a power efficiency limited to around 5%. Other insulation technologies such as piezoelectric coupling cannot respond to the high insulation voltage demands. Therefore, our choice is to use and optimize a planar transformer with ferrite cores.



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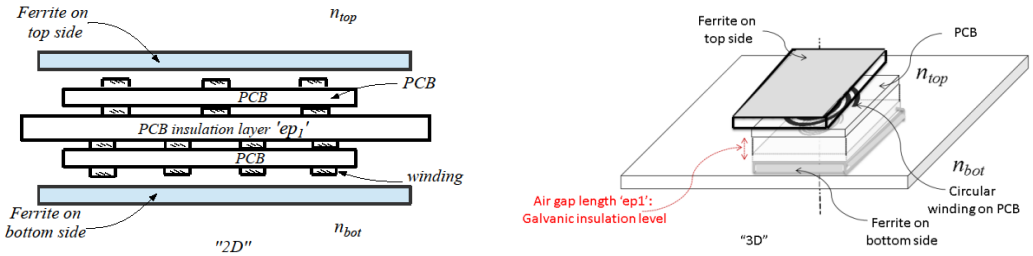


(b)

Fig. 2.2.: Compact planar transformer:
(a) a coreless transformer,
(b) a ferrite core transformer: "2D" on the left side and "3D" on the right side.

Actually, there are two types of planar transformers: a coreless transformer (***cf.*** Fig. 2.2a) and a compact ferrite core transformer (***cf***. Fig. 2.2b: "2D" on the left side and 3D on the right side). For the high insulation voltage IGBT gate driver implementations, the magnetic coupling factor (k) and inductor values of the transformer are important parameters to be analyzed. The transformer with highest coupling coefficient (k) and inductors provide the best performance for signal transmission and less energy consumption, and obtain the highest efficiency for power supply function of IGBT gate drivers systems. According to [Dij12], with the same transformer dimension, coreless planar transformer and ferrite core planar transformer are investigated and compared in term of coupling coefficient (k) and inductor values. As a result, the compact ferrite core printed-circuit-board (PCB) planar transformer achieves higher coupling (k) and higher inductors than the coreless one. Moreover, according to [Ouy12], planar transformer has become very popular in high-frequency power converters because of their advantages that

they achieve in terms of low profile, excellent thermal characteristic, modularity and manufacturing simplicity. Thus, the high insulation technology with high air gap compact ferrite planar transformer is proposed.

2.2.2. High insulation capabilities materials studies

As an example, a compact planar transformer with windings on PCB is presented in Fig. 2.2b. In this figure, the primary and secondary sides are separated by an air gap (which is used to determine the galvanic insulation voltage level). In the final applications, the air gap will be replaced by high voltage insulation materials to sustain high galvanic insulation voltage level capabilities. Thus, at first, few insulators are studied for this application. Moreover, some comparisons and validations are provided to ensure our high insulation design system.

2.2.2.1. Choice of the galvanic insulation barrier for insulation system in compact transformers

The galvanic insulator barrier suffers from two main issues under high electric fields. The first one is dielectric breakdown related to the bulk properties of the insulating materials (defects, electrical and mechanical properties, interfaces and electrode nature…) while the second is due to the external partial discharge occurrence related to the environment and electric field distribution around the electrodes which can lead to the sample degradation and its failure.

Firstly, the most used dielectric materials for galvanic insulation are categorized into ceramics and polymeric films [Bar09]. Ceramic dielectrics have relatively low dielectric strength (< 50 kV/mm) due to the presence of grain boundaries, porosity, and other defects. Polymer dielectrics, especially unfilled films, have higher dielectric strength (> 300kV/mm), lower dielectric loss (< 0.01) and dielectric permittivity (< 4). According to the application needs (i.e. high dielectric strength and low dielectric constant at room temperature operation), it appears that polymers are more adequate than ceramics since they can withstand the target voltage with thinner films, and hence they allow the increase of the transformer efficiency. Among the different polymer materials, dielectric epoxy films are generally used in such applications. However, their main drawback is the high water adsorption capability. The influence of water adsorption on epoxy composite has been widely reported. It has been evidenced that the moisture increases the dielectric permittivity and the loss tangent and reduces the breakdown voltage [Fuk97], [Nag02]. Similarly, fillers generally decrease the breakdown voltage of polymer. A hydrophobic and unfilled polymer, such as polysterimide, is necessary to increase the breakdown voltage of the insulation barrier. Polysterimide has also a high dielectric strength (50-100 kV/mm), a low dielectric constant (3.5) and films of few millimeters are simple to be built. The breakdown field and the reliability of polysterimide under AC voltage will be experimentally investigated in the following validation. The influence of moisture and filler will be also revised.

Secondly, the field distribution and the environment where the sample is placed can significantly change the partial discharges apparitions and activities and hence affect the reliability of the dielectric material. The reduction of field strength enhances significantly the system lifetime. For a constant applied voltage, the field strength can be essentially reduced by changing the nature of the packaging system (around the electrodes and the dielectric) as well as the geometry of insulator and the electrodes. As electrical discharges occur in air for a local field of 3 kV/mm (at room temperature and at atmospheric pressure), it is important to avoid the exposure of the system to ambient air. It should be provided to package the pore planar transformer within an insulator having higher dielectric strength than the air (such as gel or liquid insulator). It should be noted that higher is the permittivity of the packaging insulator, the lower is the local field.

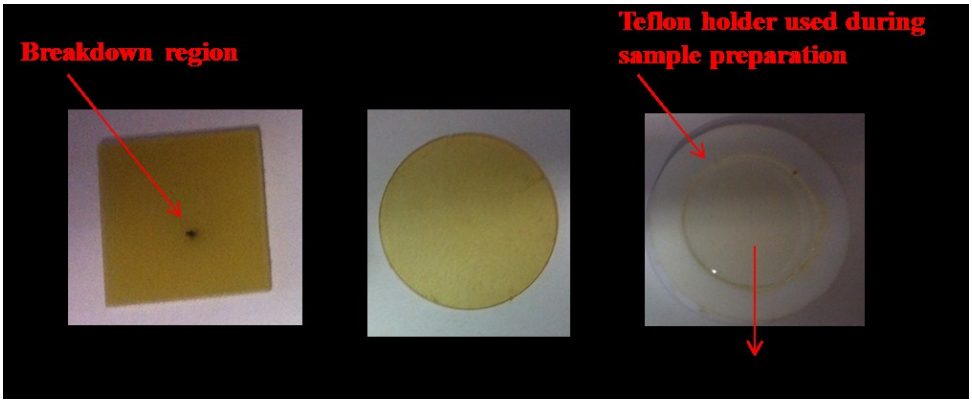
2.2.2.2. Insulator breakdown voltage validations

In order to verify the influence of the moisture, fillers and sample diameter on the dielectric strength of the selected polymers experimental measurements are carried out. Breakdown measurements are done at a frequency of 50 Hz with an applied voltage up to 40 kV. In order to minimize the influence of surface discharges on the breakdown voltage, measurements are done in a sphere plane electrode system immerged in vegetal oil, as described in Fig. 2.3. The sphere and the plane electrode diameters are 2.5 cm and 2 cm, respectively. Breakdown is detected by the large current spike occurring when the sample is short-circuited by the breakdown arc.

The breakdown measurements versus sample type, diameter and water content are presented in Table 2.1. The results demonstrate that the breakdown voltage is more influenced by the water content than the filler. One of the features of such results is that the dielectric strength of polysterimide (hydrophobic and unfilled polymer) is higher than 40kV. It can be used as insulator barrier for the planar transformer.

Table 2.1: The experimental results for validation the insulator (sample thickness: 1 mm)

Poly. name	**Specifications**	**Sample dia.**	**Breakdown voltage**
Epoxy	Unfilled – 0.8% of water content	40 mm	28 kV
	Glass filled epoxy (PCB – FR4) – ~ 0.2% of water content	25 mm	Surface discharges followed by breakdown at 37 kV
Polysterimide	Unfilled and hydrophobic polymer	25 mm	Surface discharges followed by breakdown at 40 kV (after 5 min)
		40 mm	> 40 kV No breakdown at 30 kV (for at least 2 hours)



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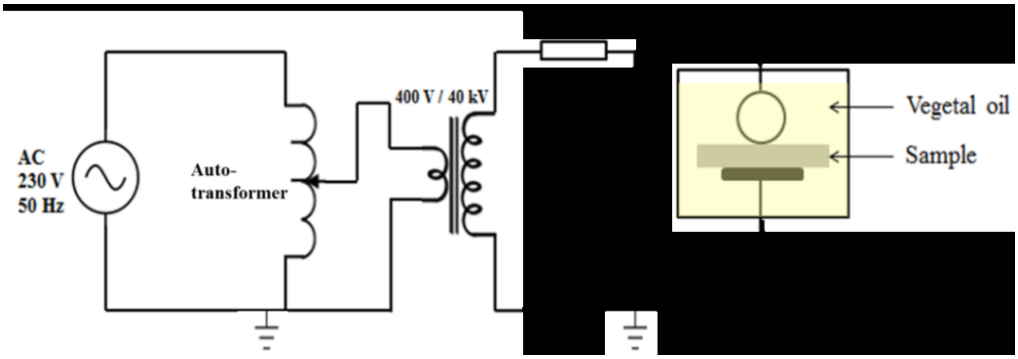

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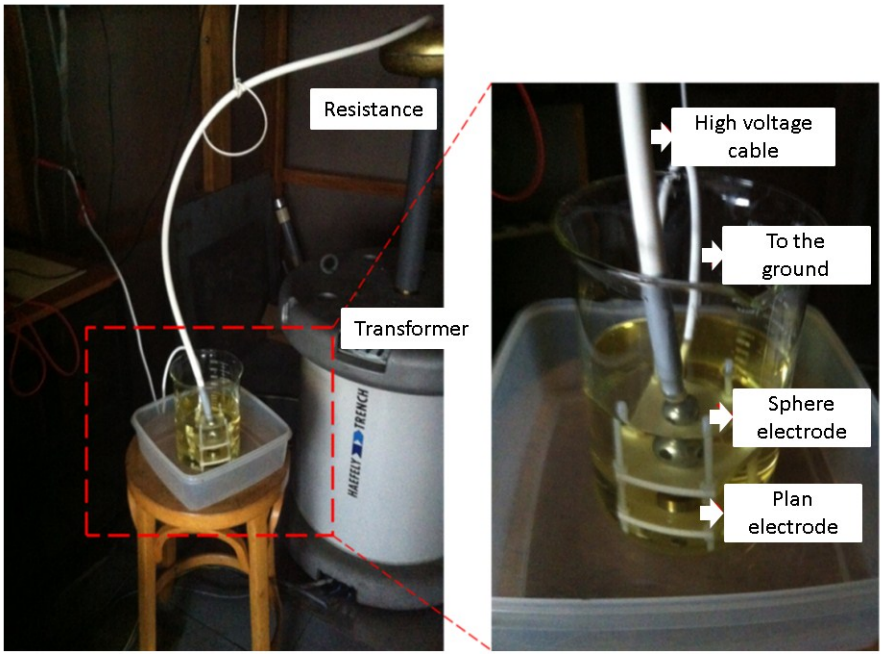


(c)

Fig. 2.3.: Validation of the insulator breakdown voltages:
(a) Sample insulator for testing experimental works: glass filled epoxy, polysterimide,
(b) Schematic of the experimental set-up for breakdown measurement,
(c) Experimental instruments for breakdown voltage measurement works of insulators.

2.2.3. High air gap transformer investigations and analyses

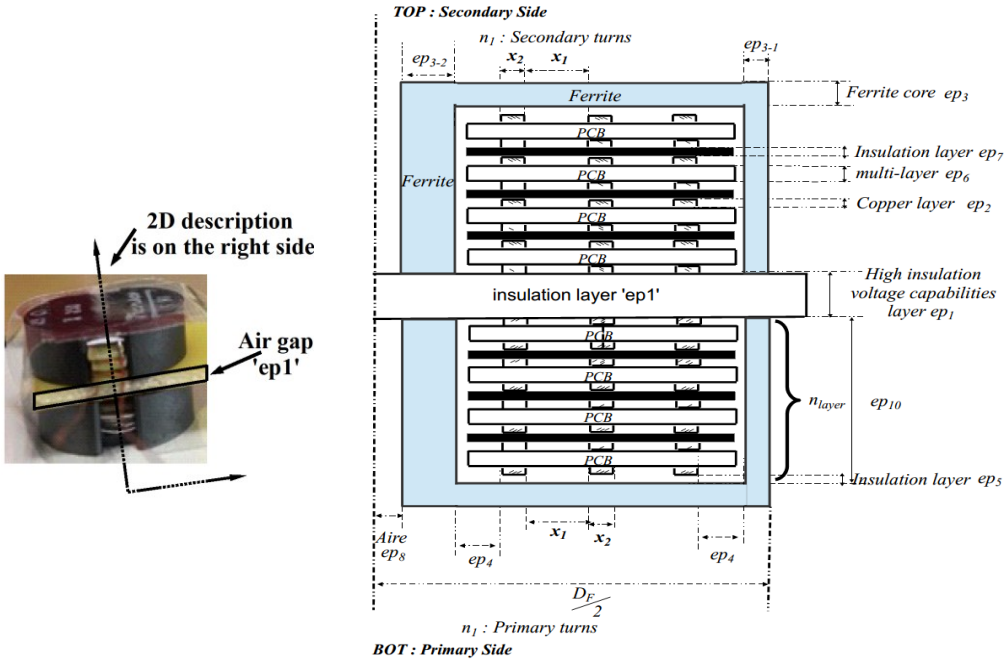
After the validations of some insulator types, polysterimide is selected as insulation material for the final application. This polysterimide insulator can achieve higher insulation voltage and longer operation life than the classical epoxy for the same insulation layer and diameter. Thus, in this section, we will investigate some geometries of planar transformer with polysterimide insulator. The main constraint of the comparison is to achieve high efficiency for power transmission function and to provide better performance for the signal transmission function.

As presented previously, the higher magnetic coupling *k* of transformer provide the better performance and high efficiency of IGBT gate drivers systems. Thus, at this stage, the winding shapes and ferrite core shapes of transformer are studied and analyzed for this kind of application.

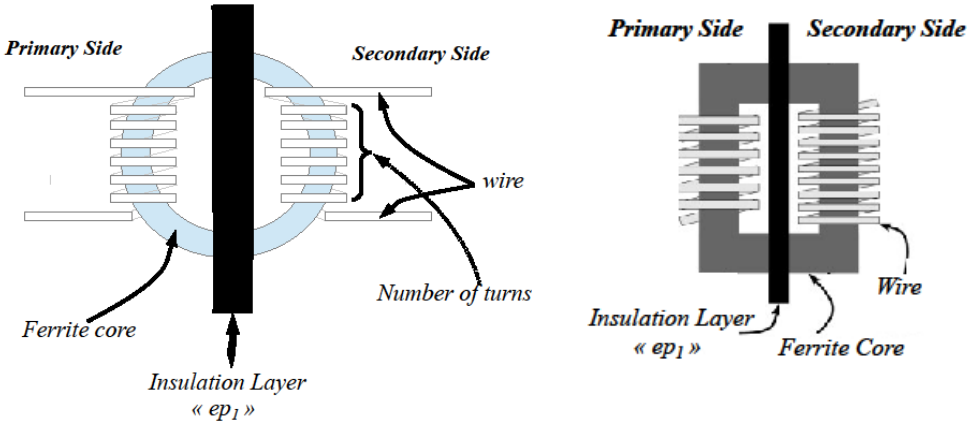
Winding shapes: according to [Bos13], several coil geometries are studied and compared in term of transformer coupling factor (k) for power transfer application. As a result, the circular coil (see Fig. 2.2a) shape achieves higher coupling coefficient which provides higher efficiency than other coils for the same configuration. Thus, the circular windings on PCB are selected.

Magnetic cores: as illustrated in [Leg07] [Sme10], the comparison between a pot core transformer and other magnetic cores are illustrated. As a conclusion, the pot core transformer gives the best performance indexes in terms of flux density, high magnetic coupling, minimal core losses and winding losses.

From these reasons, we select pot core planar transformers with circular coils on PCB for this gate driver application. To justify our choice on the transformer selection, some transformer geometries are selected and compared experimentally. As shown in Fig. 2.4, pot core (PC18/11), toroidal core and UU core are investigated as transformer core geometries. The parameter ep_1 (air gap) varies from 1mm to 3mm for each transformer core. The experimental results with Agilent 4294A precision impedance analyzer are presented in Table 2.2. As a result, the ferrite pot core has the best magnetic coupling factor compared to the two other geometries.



(a)



(b) (c)

Fig. 2.4.: Transformer cores:

(a) 2D pot core with PCB windings,

(b) Toroidal core and windings,

(c) UU core and windings.

TABLE 2.2: The experimental results of the selected three ferrite cores

Transformer Core	**Insu. layer (ep_1)**	**L_p [µH]**	**L_s [µH]**	**M [µH]**	**k**
"UU"	*1mm*	31	30	10.25	0.336
"Toroidal"		5.14	5.2	2.13	0.411
"PC18/11"		**19.11**	**18.1**	**12.34**	**0.664**
"UU"	*1.5mm*	29.8	30	9.17	0.312
"Toroidal"		4.98	4.9	1.94	0.392
"PC18/11"		**16.53**	**15.4**	**8.97**	**0.562**
"UU"	*2mm*	28.7	28	8.77	0.309
"Toroidal"		4.6	4.7	1.39	0.298
"PC18/11"		**15.2**	**13.9**	**7.18**	**0.495**
"UU"	*2.5mm*	27.8	27	6.53	0.238
"Toroidal"		4.47	4.7	1.39	0.276
"PC18/11"		**14.25**	**13.28**	**5.66**	**0.411**
"UU"	*3mm*	27.3	26.8	6.12	0.226
"Toroidal"		4.29	4.4	1.07	0.246
"PC18/11"		**13.72**	**12.88**	**4.76**	**0.358**

In the next sub-section, the magnetic and electrostatic modelings of the selected transformer are presented. This modeling step is a very important part to optimize geometrical aspects of the transformer. In the optimization procedure of each gate driver function of IGBT module, this process is used to calculate the inductances, resistances, mutual inductance, and parasitic capacitors by the help of geometrical optimization variables and parameters.

2.2.4. Magnetic modeling of pot core planar transformers

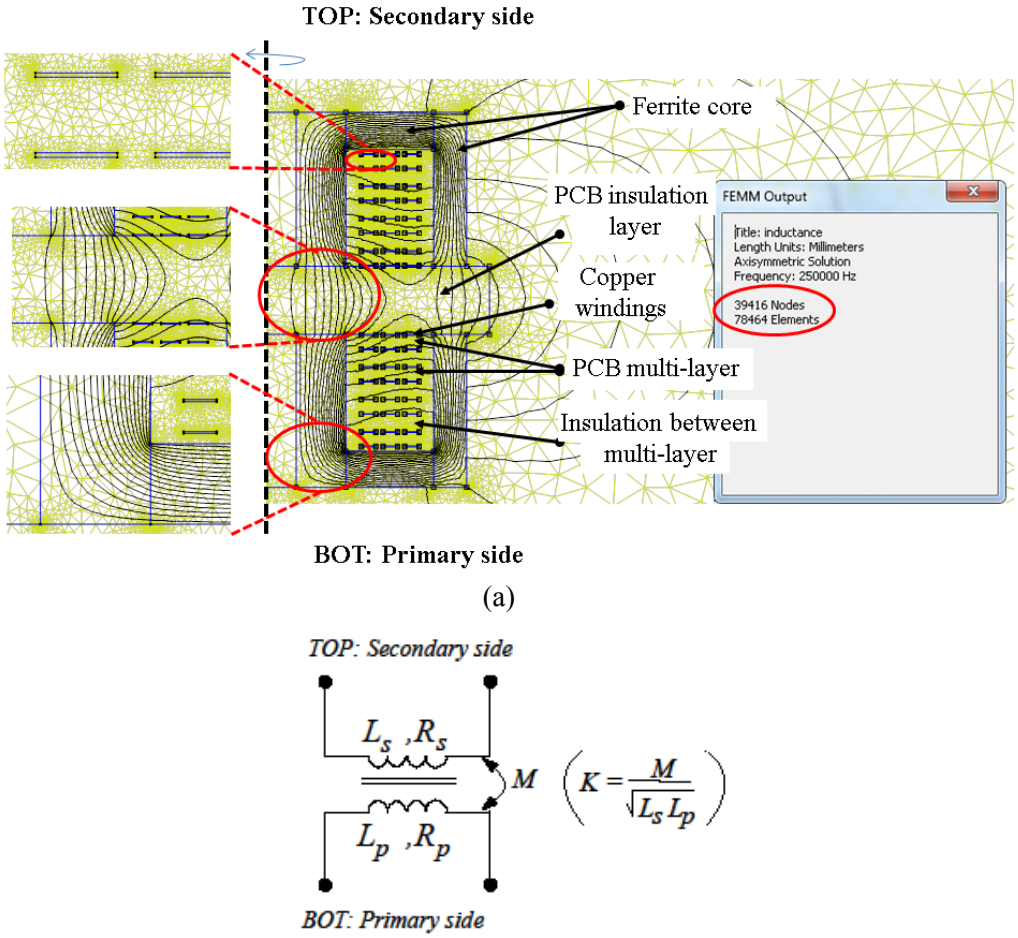
A magnetic modeling of a pot core planar transformer is performed by the help of a finite element software such as: FLUX™, COMSOL™, FEMM™, etc. Generally, the finite element method (FEM) cuts a structure (pot core planar transformer) into numerous elements (pieces of the structure). Then these elements are reconnected by "nodes". In this dissertation, the axis-symmetrical analyses of pot core planar transformers with circular winding shapes are performed with the FEMM™ simulation software. First of all, we create a pot core transformer geometry. Then, each region is defined and its material properties (ferrite, copper, dielectric, etc.: permeability, current density, etc.) are also mentioned. After that, the meshing step is introduced with respect to surface of each region. By injecting a current into a structure, the magnetic energy stored (W_m) in each transformer side and its heat losses (P_{hl}) are obtained. Hence the inductance values (L_p, L_s) of pot core transformer for both sides can be calculated by two times the magnetic energy divided by the square value of the injected current. The resistance value of each transformer side can be computed by heat losses divided by the square value of the injected current. After the inductance values are known, the mutual inductance (M) can be solved as presented in Equation (2.3). Then, the Equation (2.4) expresses the transformer magnetic coupling coefficient (k).

$$L_{Pr\ or\ Se} = \frac{2 \times \mathrm{W}_{mP\ or\ mS}}{\mathrm{I}^2_{P\ or\ S}} \tag{2.1}$$

$$R_{Pr\ or\ Se} = \frac{\mathrm{P}_{hlP\ or\ hlS}}{\mathrm{I}^2_{P\ or\ S}} \tag{2.2}$$

$$M = \frac{\mathrm{W}_m - (L_P \times I_P^2 + L_S \times I_S^2)/2}{\mathrm{I}_P \times \mathrm{I}_S} \tag{2.3}$$

$$k = \frac{\mathrm{M}}{\sqrt{L_P . L_S}} \tag{2.4}$$



(a)

(b)

Fig. 2.5.: Pot core transformer modeling considerations:

(a) An example of magnetic modeling of a proposed pot core transformer from Table 2.3 with FEMM™

(b) An equivalent circuit of the transformer.

As an example, Fig. 2.5a presents the FEMM^{TM} screenshot of a pot core transformer (2D axis-symmetrical). In this example, ep_1 is equal to 3mm and other geometrical variables/parameters are summarized in Table 2.3. As presented in this figure, we have 78464 elements which are connected by 39416 nodes. On the left side, we present three different regions: galvanic insulation layer, ferrite, and PCB (printed-circuit-board) multi-layer. Then, a brief comparison between the simulation and experimental results are presented at the lower part of Table 2.3. These comparison results surely validate our magnetically modeling of the pot core transformer. For IGBT gate driver optimization design, the magnetic modeling of transformer is one of the essential parts in the optimization process. Details about these designs (optimization variables/parameters) are illustrated in Sections 2.3 and 2.4.

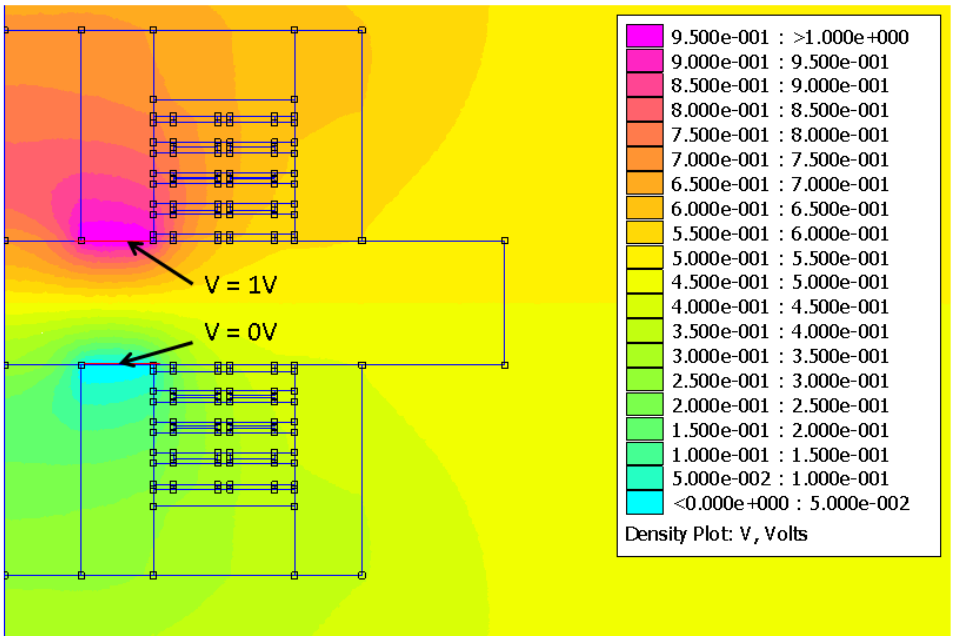
Table 2.3: Example of transformer design and its simulation results

Parameter	**Value**	**Description**	
ep_1	3 mm	galvanic insulation layer	
ep_2	35 µm	copper layer	
ep_3	1.6 mm	PC18/11 ferrite thickness	
$ep_{3\text{-}1}$	1.425 mm	PC18/11 ferrite thickness	
$ep_{3\text{-}2}$	2.175 mm	PC18/11 ferrite thickness	
ep_4	0.65 mm	reserve length of PCB from last coils	
ep_5	0.5 mm	insulation layer	
ep_6	0.5 mm	PCB for multi-layer	
ep_7	0.745 mm	insulation layer between multi-layer	
ep_8	1.55 mm	radius internal air of PC18/11	
x_1	0.3 mm	distance between the coppers	
x_2	0.63 mm	copper's width	
n_1	3 turns	number of turns	
n_{layer}	4 layers	number of multi-layers	
Comparison results of pot core transformer			
Parameters (cf.: Fig. 2.5b)	**Simulated with FEMM^{TM}**	**Measured with Agilent 4294A**	**Error relative (%)**
L_{pr}	13.65 µH	13.72 µH	0.5
L_{se}	13.30 µH	12.88 µH	3.15
M	4.95 µH	4.76 µH	3.83
k	0.367	0.358	2.45
C_{ps}	4.02 pF	4.50 pF	10.67

2.2.5. Electrostatic modeling of pot core transformer

A reference [Ngu16] presents problematic propagation paths for electromagnetic interference (EMI) of power semiconductor's gate driver circuit. The major problem comes from the parasitic elements (inductances and capacitances) in a gate driver

topology. To reduce this problem, minimizing the parasitic capacitor value is one of the main solutions. Thus, the equivalent parasitic capacitor value of planar transformer is estimated and studied.



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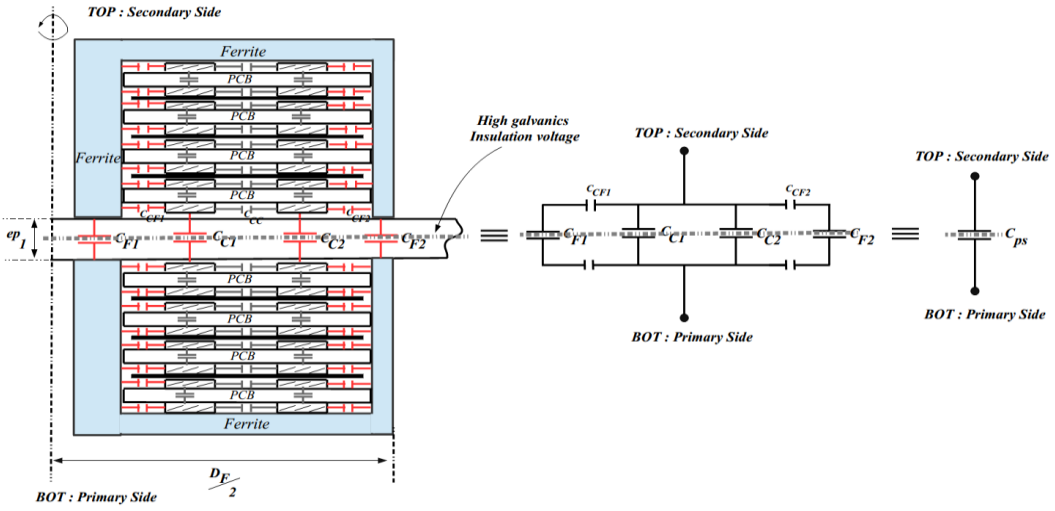


(b)

Fig. 2.6.: Pot core planar transformer modeling considerations:

(a) An example of electrostatic modeling of a proposed pot core transformer from Table 2.3,

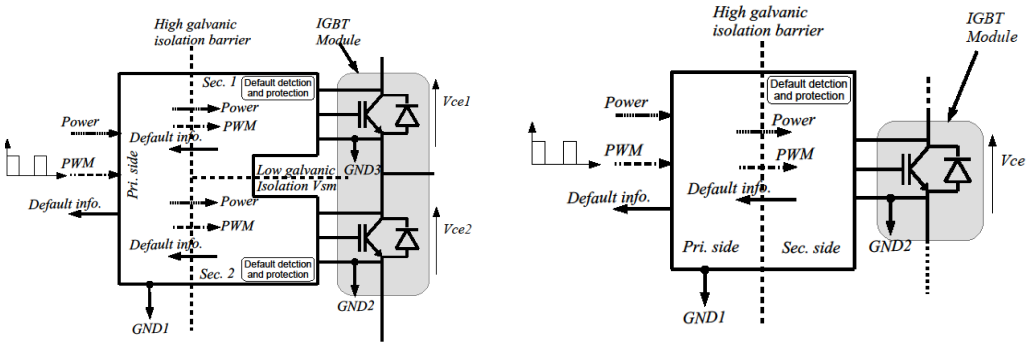
(b) Equivalent circuit of parasitic capacitance of the pot core transformer.

A reference [Fre03] presents an electrostatic modeling of power component structures with finite element software. Hence, in this thesis dissertation, an electrostatic simulation with FEMM^{TM} software is used to calculate the parasitic capacitor value of a pot core planar transformer. In this step, we impose the electrical potentials to two segments (see Fig. 2.6a). Then, the electrostatic energy (W_c) stored between these two segments is computed. Thus, one parasitic capacitor value can be calculated by the following equation [Wen13]:

$$C_x = \frac{2 \times W_C}{V_x^2} \quad ; x = \{C_{F1,F2}, C_{C1,C2}, C_{CF1,CF2}\} \tag{2.5}$$

Fig. 2.6b presents a parasitic capacitance network. Then, the equivalent capacitor circuit is presented in the middle of this figure. To simplify the complexities of a capacitor network, at first, the equivalent parasitic capacitor considers only parasitic capacitors of the first layer. After each parasitic capacitor value is computed. The equivalent parasitic capacitor (C_{ps}) between a primary side and secondary side is obtained. Then, the simulation result of this equivalent capacitor is compared to the experimental one for the same transformer dimension (as shown in Table 2.3). As presented at the lower part of Table 2.3, the validation of the equivalent capacitor C_{ps} as considered in Fig 2.6b is presented with the relative error of around 10% between the simulation and experimental results. According to this result, we notice that the parasitic capacitors of the first layer of a pot core planar transformer are the dominant parasitic elements to calculate the equivalent parasitic capacitor C_{ps}.

After the demonstrations of insulation material properties and transformer core geometries, in the next section, we present the optimization design for signal and power transmission functions. As cited earlier, the synopsis of a dual and a single IGBT gate driver system with high insulation barrier are summarized in Fig. 2.7. Section 2.3 details the optimization design for signal transmission function. Then, Section 2.4 illustrates the optimization design for the power transmission function.



(a) (b)

Fig. 2.7.: Synopsis of IGBT gate drivers system:
(a) A dual channel IGBT gate drivers,
(b) A single channel IGBT gate driver.

2.3. Optimization design for a high galvanic insulation signal transmission function

First, the signal transmission circuit is described. Then, the optimization of a compact ferrite transformer and its associated components in the circuit is proposed thanks to a virtual prototyping tool. At this stage, two different types of transformers are optimized and compared for several aspects. Finally, the optimization results are illustrated and discussed at the end of this section.

2.3.1. Signal transmission function topology

The synopsis of the signal transmission function for IGBT gate driver and the basic structure of the signal impulse transmission circuit by using magnetic insulation are illustrated in Fig. 2.8. The galvanic insulation level depends on the barrier thickness and its material. The primary side of the transformer is a series resonant topology (between primary side of transformer and a capacitor C_1) and an N-MOSFET. Then, a resistor R_1 is placed in parallel with a series capacitor C_1. At secondary side of the transformer, L_s and C_2 are in a parallel resonant topology.

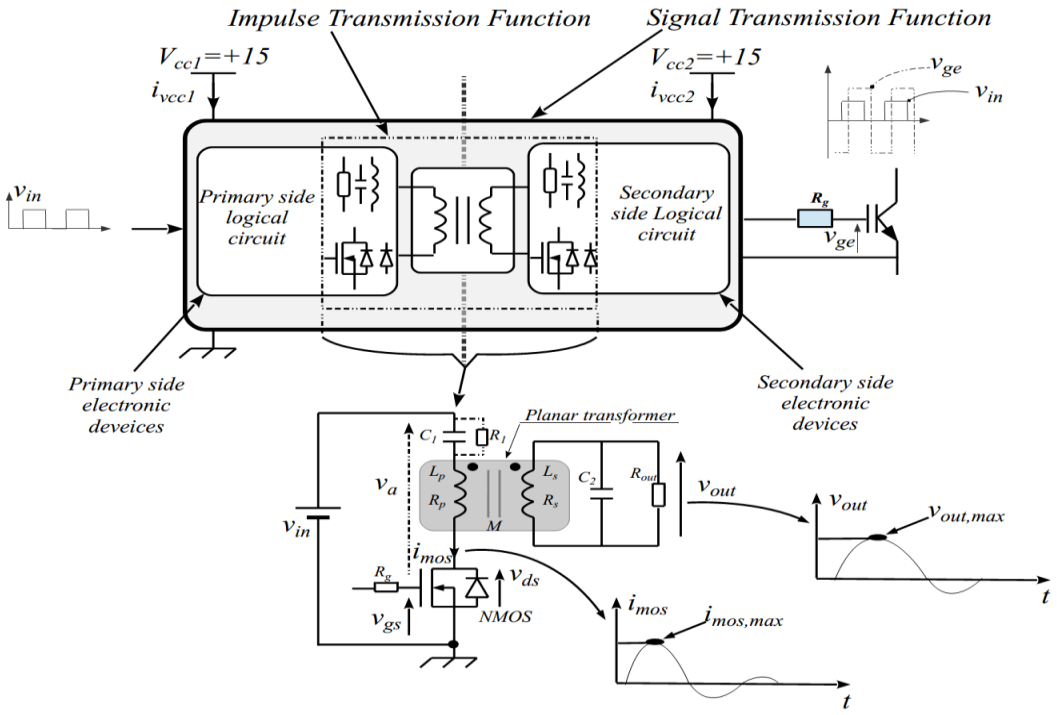


Fig. 2.8.: Synopsis and schematic of the impulse and signal transmission function based on a magnetic transformer.

This N-MOSFET is used to generate an impulse voltage (0V and V_{in} = 15V) and a series capacitor C_1 to avoid a steady-state current in the primary side of the transformer. When the forward current passes through the primary side of the transformer, the capacitor C_1 is charged. Once the capacitor C_1 is fully charged (more than the supply

voltage), the capacitor discharges through the parallel resistance R_1 to make ready the circuit for the next cycle of operation.

Then, we define three electrical variables: C_1, C_2 and the resistive load R_{out}. In the simulation and experimental works, the primary parallel resistance R_1 is fixed at 10kΩ and is not taken into account as an optimization variable. The other electrical variables are related to the geometrical variables of the proposed transformer structures. These geometrical variables are detailed in the next sub-section.

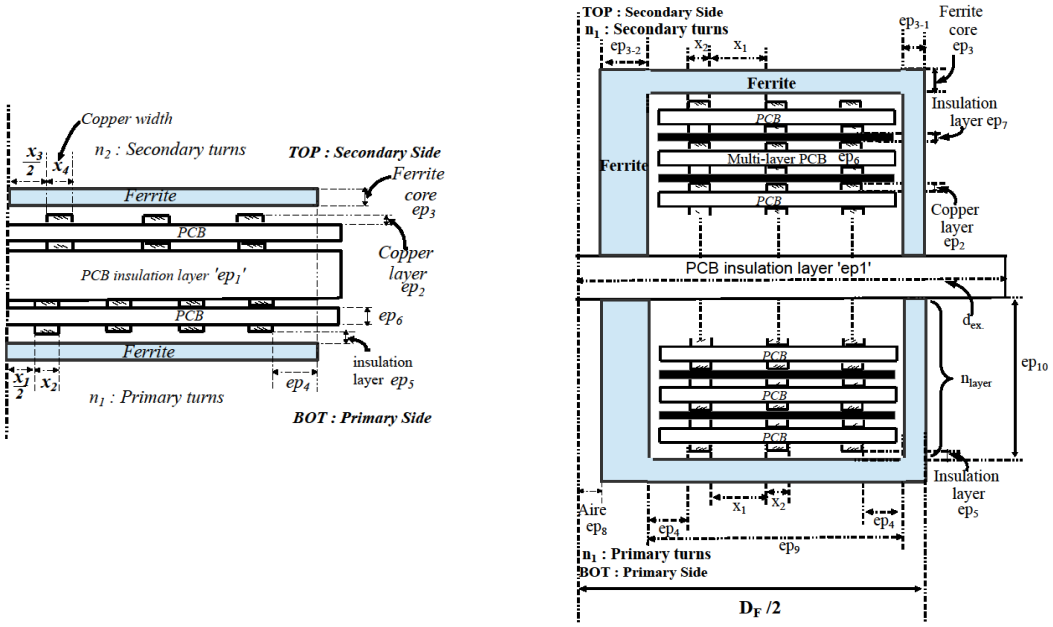
Maximizing the maximum value of the output voltage ($V_{out,max}$: see Fig. 2.8) and minimizing the maximum value of the primary side current ($i_{mos,max}$: see Fig. 2.8) are set as a bi-objective problem. The value of $V_{out,max}$ must be maximized so as to be in the range of (4V-6V) required for "the secondary side logical circuit". And the current at the primary side is minimized for the objective to minimize the power consumption within the proposed electrical circuit. A bi-objective problem of the overall system leads to Pareto fronts. Several Pareto fronts' results are obtained assuming different insulation layers thickness (which define our galvanic insulation voltage level). The chosen transformer solution is justified by the galvanic insulation level of the system. Then, the experimental works and results are presented in Chapter 3. After that, those results are compared with the simulation ones to validate our proposed design methodology.

2.3.2. Signal transmission function optimization descriptions

The insulation barrier is a critical function and must verify many constraints: static insulation voltage, parasitic capacitances values between the primary and secondary sides, delay/propagation time, dv/dt and di/dt immunities, noise immunities etc. Thus, the geometry of the transformer and some electrical components must be optimized to achieve sufficient output impulse voltage information and low power consumption within the system. At this stage, in order to support our ferrite pot core choice, we present two transformer geometries: double-layer with I core planar transformer (Fig. 2.9a) and multi-layer pot core planar transformer (Fig. 2.9b). Both are optimized and compared in detail.

2.3.2.1. Signal transmission optimization variables and parameters

As presented in Fig. 2.9a and Fig. 2.9b, a double-layer planar transformer (DBL) and a multi-layer pot core planar transformer (MLPC) are illustrated, respectively. Based on the different geometrical transformer constructions, optimization variables and parameters are presented.



(a) (b)

Fig. 2.9.: Transformer geometries:
(a) 2D description of the double-layer (DBL) planar transformer,
(b) *2D description of the multi-layer pot core (MLPC) planar transformer.*

Optimization variables: depend on the electrical circuit in Fig. 2.8, C_1, C_2 and R_{out} are defined as three electrical variables. Double-layer planar transformer and multi-layer pot core transformer variables are different due to the technical constraints. The turn number, copper width and distance between two copper windings are different between the primary and the secondary sides of a double-layer planar transformer. Thus, there are six geometrical variables for double-layer planar transformer: $\{n_1, n_2, x_1, x_2, x_3, x_4\}$ (detail in Table 2.4).

Whereas, a multi-layer pot core planar transformer technology, the turn numbers and distance between two copper windings should be considered the same because of the small winding space of a pot core ferrite technology. Thus, we define two variables: $\{n_1, x_1\}$ for multi-layer pot core transformer. The copper width x_2 cannot be considered freely as an optimization variable due to the winding space constraint of the proposed ferrite core. Thus, x_2 must be considered as an internal variable. This variable can be computed after n_1 and x_1 are set (see Equation (2.7) and Table 2.5). And the number of layers n_{layer} should be regarded as an integer optimization variable type. Finally, double-layer planar transformer and multi-layer pot core transformer variables are summarized in Table 2.4.

Optimization parameters: the constant parameters' definitions and their values are defined in Table 2.5.

Table 2.4: Optimization variables' definitions

Double-layer planar transformer (6 variables)	***Multi-layer pot core planar transformer (3 variables)***
• n_1: turn number on the primary side; • n_2: turn number on the secondary side; • x_1: distance between two copper windings on the primary side; • x_2: copper width on the secondary side; • x_3: distance between two copper windings on the secondary side; • x_4: copper width on the secondary side. $\overline{X_{DB}} = \{n_1, n_2, x_1, x_2, x_3, x_4\}$	• n_1: turn number on the primary/secondary sides; • x_1: distance between two copper windings on the primary/secondary sides; and • $n_{layer} = \{2, 3\}$: number of layers. $\overline{X_{PC}} = \{n_1, x_1, n_{layer}\}$
Electrical variables	
• C_1: series capacitor on the primary side; • C_2: parallel capacitor on the secondary side and • R_{out}: parallel resistor on the secondary side.	
Optimization variables	
$\overline{X_{XDB}} = \{n_1, n_2, x_1, x_2, x_3, x_4, C_1, C_2, R_{out}\}$;	$\overline{X_{XPC}} = \{n_1, x_1, n_{layer}, C_1, C_2, R_{out}\}$;

Table 2.5: Optimization parameters' definitions

Double-layer planar transformer (cf. Fig. 2.9a)	***Multi-layer pot core planar transformer (cf. Fig. 2.9b)***
• ep_1 = {1.6mm, 2mm, 2.5mm, 3mm}: galvanic insulation barrier thickness; • ep_2 = 35µm : copper thickness; • ep_3 = 0.3mm : ferrite core thickness; • ep_4 = 1mm : extra length of the ferrite relative to the edge of the last coil; • ep_5 = 35µm : insulation between coil and ferrite; and • ep_6 = 1.6mm : PCB thickness for primary and secondary windings; • D_F = {7mm, 9mm and 14mm} : maximum ferrite diameters.	• ep_1 = {0.5mm, 1mm, 1.6mm, 2mm} : galvanic insulation barrier thickness; • ep_2 = {70µm, 105µm} : copper thickness; • ep_4 = 0.2mm : extra length of the ferrite relative to the edge of the last coil; • ep_6 = 0.4mm : PCB thickness for multi-layer assembling; • ep_7 = 18µm : insulation thickness between layers of multi-layer; • {ep_3, ep_{3_1}, ep_{3_2}, ep_8, ep_9, ep_{10}}: pot core dimensions (D_F = {7mm, 9mm, 14mm}); • $ep_5 = ep_{10} + ep_7 - n_{layer}(ep_6 + ep_7 + 2 \times ep_2)$ (2.6) : insulation between coil and ferrite • $x_2 = \frac{ep_9 - 2ep_4 - (n_1 - 1)x_1}{n_1}$ (2.7) : copper width

2.3.2.2. Signal transmission optimization objectives

Generally, the optimization objectives of the optimization process depend on the requirements of the final application. For this design, the first objective is to obtain the maximum value of output voltage $V_{out,max}$ and the secondary objective to be minimized is the primary side or MOSFET current $i_{mos,max}$. $V_{out,max}$ must be maximized to increase the electromagnetic immunity of the system, whereas $i_{mos,max}$ must be minimized to decrease the average power consumption of the system. The Pareto front of $V_{out,max}$ against $i_{mos,max}$ is the main plot to be analyzed to choose the most suitable configuration.

2.3.2.3. Signal transmission optimization constraints

According to industrial issues, the variables must be considered under constraints. Table 2.6 presents the optimization constraints for each transformer.

Table 2.6: Optimization constraints

Double-layer planar transformer (cf. Fig. 2.9a)	***Multi-layer planar transformer (cf. Fig.2.9b)***
• Variables ✓ $n_1, n_2 \in \{2, 3, 4, 5, 6\}$; ✓ $x_1, x_2, x_3, x_4 \in [0.2mm, 1mm]$; ✓ $C_1, C_2 \in [0.1nF, 1nF]$; and ✓ $R_{out} \in [1k\Omega, 30k\Omega]$.	• Variables ✓ $n_1 \in \{2, 3\}$; ✓ $x_1 \in [0.2mm, 0.4mm]$; ✓ $n_{layer} \in \{2, 3\}$; ✓ $C_1, C_2 \in [0.1nF, 1nF]$; and ✓ $R_{out} \in [1k\Omega, 30k\Omega]$. • Technical constraints ✓ $B_{max} < B_{sat}$: maximum induction; ✓ $ep_5 < 0.3mm$, ✓ $C_{ps} < 10$ pF.

2.3.2.4. Signal transmission computation procedure and optimization algorithm

The pre-sizing tool is described in Fig. 2.10. It combines a finite element software FEMM™ and LTSpice™ software with the help of a genetic algorithm (GA) coded in a MATLAB™ script. As presented in this figure, FEMM™ software calculates (L_p, L_s, R_p, L_s, M, k) with the help of geometrical variables ($\overline{X_{DB}}$ or $\overline{X_{PC}}$). Then, LTSpice™ software runs an electrical transient simulation with the help of (L_p, L_s, R_p, R_s, M, k) numerical values and electrical variables (C_1, C_2 and R_{out}) of the system.

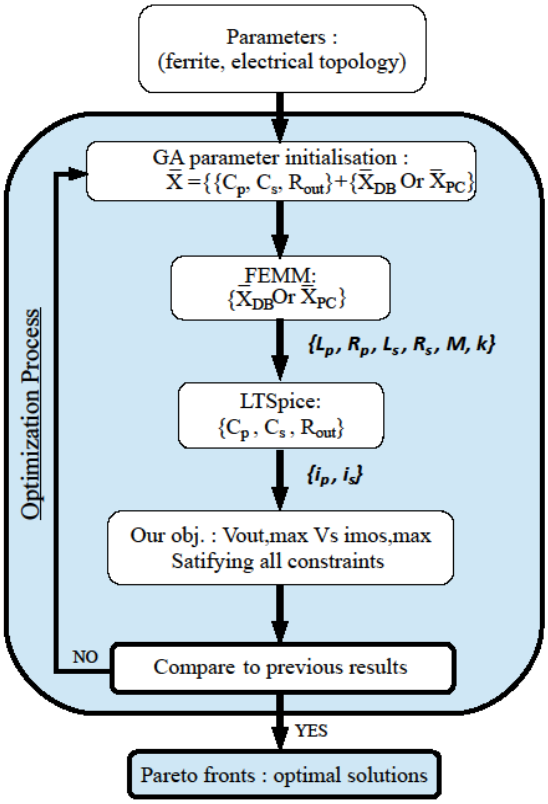
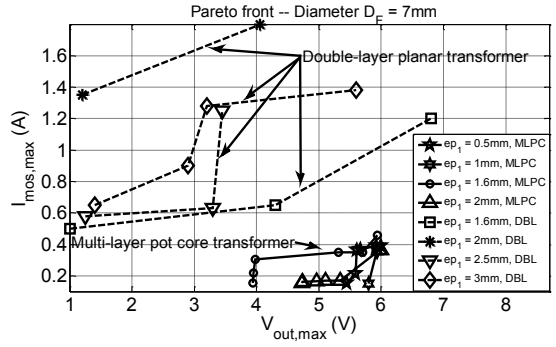


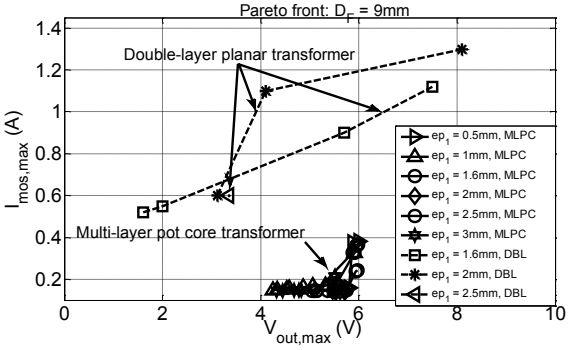
Fig. 2.10.: Genetic algorithm (GA) flowchart for overall system optimization based on FEMM™ and LTSpice™ softwares.

2.3.3. Signal transmission optimization results: Pareto fronts' results

The parameters of the genetic algorithm (GA) are 10 individuals and 50 generations and it requires 2 hours of computation times (with an Intel Core 2Duo CPU, DELL). Fig. 2.11a-c illustrate all the Pareto fronts' curves for different insulation barrier thickness (ep_1 = {0.5mm, 1mm, 1.6mm, 2mm}), different ferrite maximum diameters (7mm, 9mm and 14mm) and different type of transformer designs (double-layer transformer and multi-layer pot core transformer). For each Pareto front, the number of points depends on the number of individuals and generations. Therefore the designer cannot set, a priori, the number of points on the Pareto front. He can add individuals and generations to potentially increase the number of points but the total computing time increases too. Nevertheless, it remains a choice to be solved by the designer. Then, the optimization process leads to Pareto fronts that must be analyzed regarding additional constraints. In the objective of choosing a practical solution, additional constraints must be defined and depend on the electronic devices in the secondary side that need a power supply of 5 V: authors have chosen a Schmitt trigger to transform the analogical impulse voltage (V_{out}) into logical information (to be treated by a T flip-flop). Thus, as shown in Fig. 2.11d, the chosen solutions must be in the range of 4–6 V for $V_{out,max}$.



(a)



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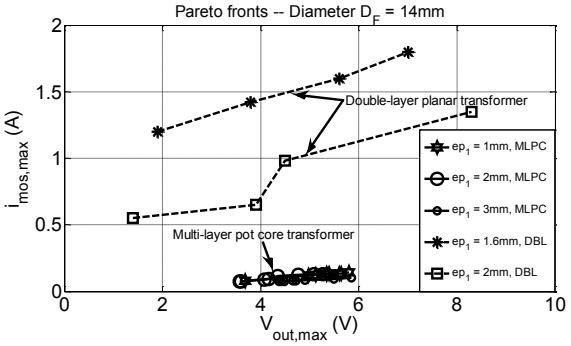

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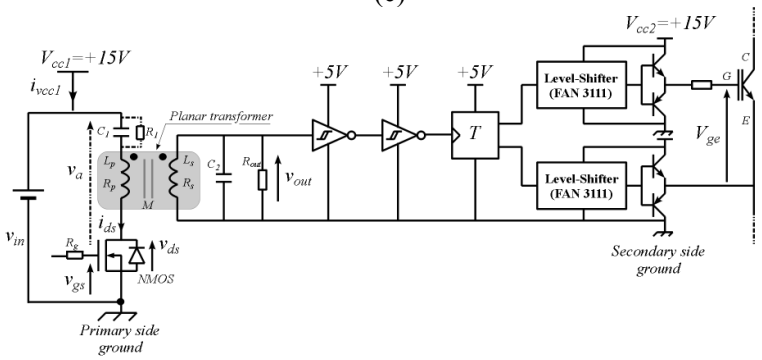


(d)

Fig. 2.11.: Signal transmission optimization results:

(a) Optimization results under Pareto fronts for D_F = 7mm,

(b) Optimization results under Pareto front for D_F = 9mm,

(c) Optimization results under Pareto front for D_F = 14mm, and

(d) *Schematic of IGBT gate drivers with secondary electronic devices.*

According to the power consumption consideration, the input current $i_{mos,max}$ must be minimized for the objective of power consumption. As presented in Fig. 2.11, for all ferrite diameters, optimization results of high insulation capabilities signal transmission function IGBT gate driver with multi-layer pot core transformer consume less energy compared to double-layer planar transformer technology. Moreover, the propagation delay between the drain-source V_{ds} of N-MOSFET and gate-emitter V_{ge} of IGBT must be considered. Based on the experimental results in Chapter 3, the propagation delay of double-layer planar transformer and multi-layer pot core planar transformer are in the same range. Thus, based on these analyses, a multi-layer pot core planar transformer is a suitable candidate for this application.

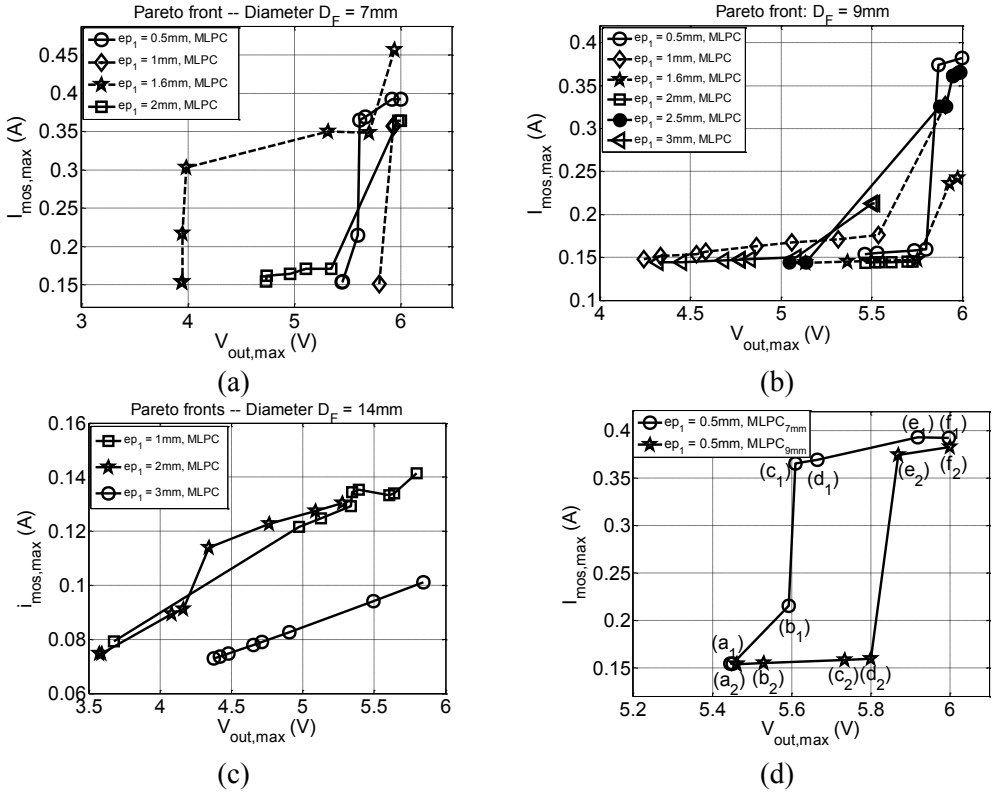


Fig. 2.12.: Pareto fronts' results for multi-layer pot core transformer technology:
(a) Pareto fronts' results for D_F = 7mm,
(b) Pareto fronts' results for D_F = 9mm,
(c) Pareto fronts' results for D_F = 14mm, and
(d) Pareto fronts' results for our design target.

In Fig. 2.12, we propose optimization results for multi-layer pot core planar transformers. Fig. 2.12a-c presents the Pareto fronts' results of ferrite diameters 7mm, 9mm and 14mm, respectively. According to the insulation material validation in Section 2.2.2, in order to achieve an insulation voltage of 30kV ($V_{DC,MMC}$ = 30kV), a 0.5mm of polysterimide seems to be a suitable choice. Thus, our further analysis for practical design is focused on 0.5mm of insulation barrier. As presented in Fig. 2.12d, two interesting Pareto fronts from two different ferrite diameters are plotted in the same graph. We notice

that for the same output voltage range from 5.4V to 5.8V, the optimal solutions based on a 9mm diameter pot core provide the best performances with low power consumption compared to the 7mm ones. Thus, the optimal solutions {(a_2), (b_2), (c_2) and (d_2)} from the 9mm of pot core diameter are the dominants solutions. Nevertheless, the solution (a_1) would be interesting to be compared to solution (a_2).

Among these four solutions, the power consumption is nearly the same based on the values of $i_{mos,max}$. Thus, as the secondary power electronic devices require a supply voltage of around 5V, the solution (d_2) is the best choice by reserving the little voltage drop over the system. The optimization results of the selected solution (d_2) are presented in Table 2.7. As shown in Fig. 2.13a-f, capacitor C_1 is equal to 108pF and C_2 to 316pF. The parallel resistance R_{out} = 30kΩ is needed. The characteristic of the optimal transformer are: 2 double layers per side, 2 turn windings on PCB, and distance between the copper x_1 = 0.32mm. From the FEMM^{TM} simulation; $L_p = L_s$ = 2.03µH, $R_p = R_s$ = 0.26Ω and the coupling value k = 0.776 are the electrical values of the transformer.

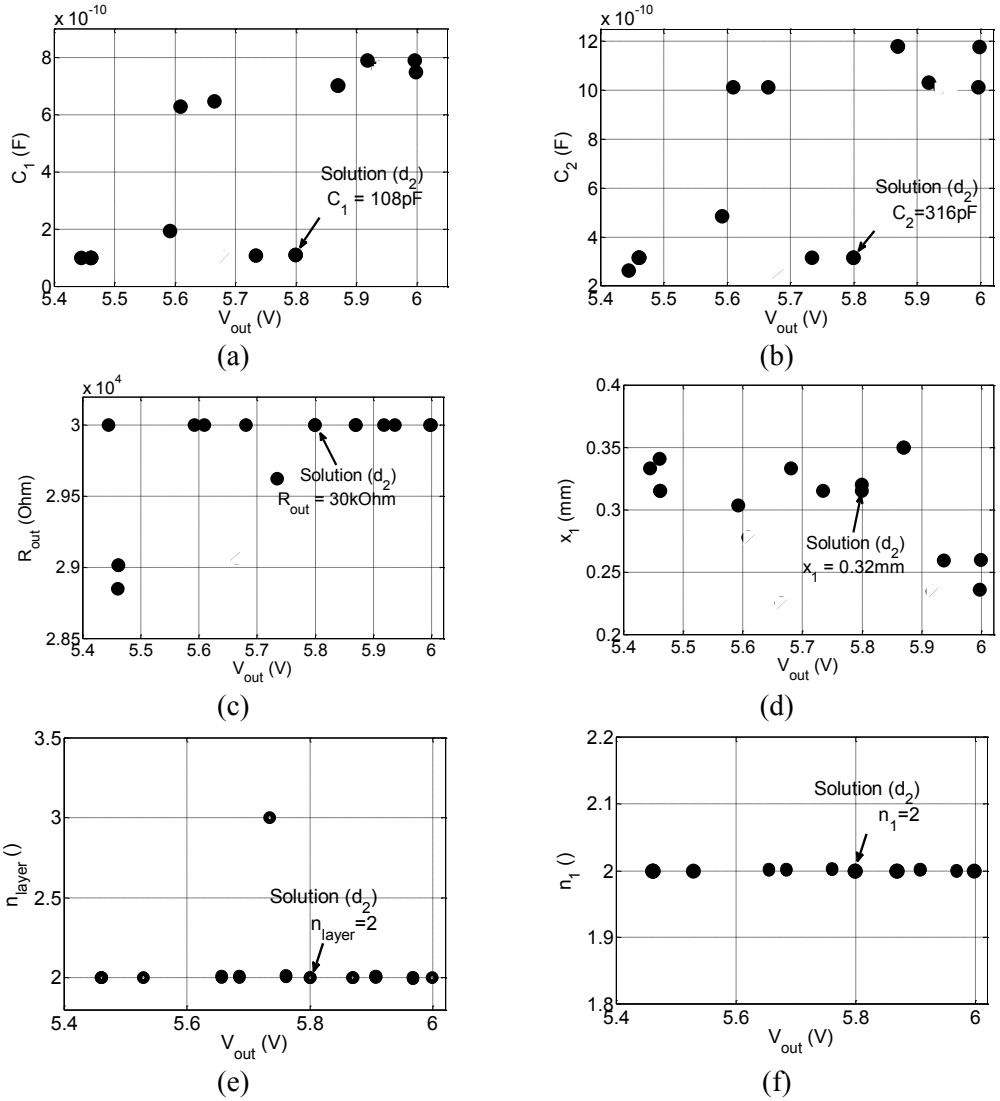


Fig. 2.13.: Evolution of the variables as a function of the output voltage V_{out}

Table 2.7: Simulation results of optimal solution (d_2)

	Solution (d_2)		
V_{out} / i_{mos}	5.8V / 0.15A (see Fig. 2.13)		
ep_1/D_F	0.5 mm/9 mm		
C_1 / C_2	108.64 pF/ 316 pF	L_p / R_p	2.03 µH / 0.26Ω
R_{out}	30 kΩ	L_s / R_s	2.03 µH / 0.26Ω
x_1	0.32 mm	M/k	1.57 µH / 0.776
n_1/ n_{layer}	2 turns / 2 layers	C_{ps}	2 pF

Fig. 2.14 shows the simulation waveforms of the output voltage (V_{out}), the primary side current (i_{mos}), the drain-source voltage (V_{ds}) and the gate-source voltage (V_{gs}) of the N-MOSFET at the primary side of the electrical circuit for the chosen optimal solution (d_2).

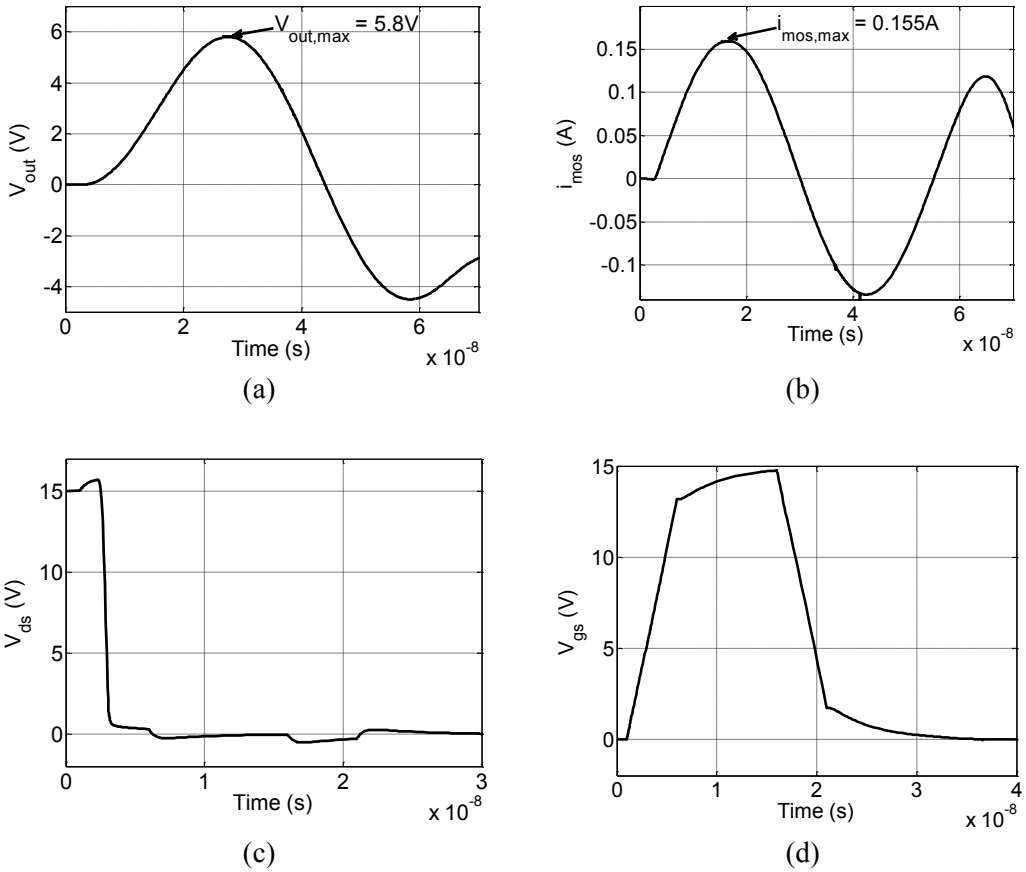


Fig. 2.14.: Simulation result's waveform of an optimal solution (d_2):

(a) Output voltage waveform of the proposed electrical circuit,

(b) Primary side current waveform,

(c) Drain-source current of a MOSFET at the primary side, and

(d) Gate-source voltage of a MOSFET at the primary side.

In Chapter 3 Section 3.3, our proposed optimization design methodology to optimize a high galvanic insulation barrier signal transmission function IGBT gate drivers is validated experimentally. Then, the comparison between the simulation and experimental results are presented to validate our proposed design methodology.

2.3.4. Conclusion: Signal transmission function for IGBT gate driver

When designing high insulation barrier capabilities signal transmission function for IGBT gate drivers, two critical points are: the output voltage information of signal transmission system (V_{out}) and the power consumption of the system. The required supply voltage 5V is needed to supply the electronic devices at the secondary side of the proposed circuit. Thus, the output voltage information $V_{out,max}$ solutions must be in the range of 4-6V. Two different transformers are proposed for this design: double-layer planar transformer and multi-layer planar transformer. Then, we have developed an accurate virtual prototyping tool in order to design such as low-power system. A finite element software FEMM^{TM} is used to calculate the electrical values (L_p, R_p, L_s, R_s, M and k) of the proposed transformer by the help of geometrical variables ($\overline{X_{DB}}$ or $\overline{X_{PC}}$). Then, these electrical values combined with other electrical variables in signal circuit are simulated with an electrical transient simulator LTSpice^{TM}. These two main steps are performed in the optimization process coded in a MATLAB^{TM} script. Finally, with a set of insulation layer ep_1 and different ferrite diameters D_F, several Pareto fronts' are plotted in a bi-objective optimization problem.

Numerous optimization results for these two different transformer technologies are presented and analyzed in detail. As a result, with multi-layer pot core technologies, the proposed system consumes less energy than the double-layer one for the same output voltage information immunity. Hence, the optimization results with ferrite pot core are further investigated until the suitable solution is chosen for practical works. Furthermore, among the selected optimization results for experimental works, the optimal solution (d_2) is the most suitable solution in terms of low power consumption and output voltage information. The simulation results of this solution are provided and summarized in Table 2.7. Then, the simulation waveforms of the output voltage and primary current are presented in Fig. 2.14. In Chapter 3, this optimal solution is validated experimentally.

In the next section of this Chapter, a power transmission function for IGBT gate drivers for MMC-MVDC applications is studied and optimized.

2.4. Optimization design for a high galvanic insulation power transmission function

A power supply function is another main function in IGBT gate drivers. As presented in Fig. 2.15, for a single channel IGBT gate driver, a DC-DC converter as a power transmission function is used to supply the secondary side of a PWM signal transmission. The galvanic insulation voltage of this converter must be the same rate as the signal transmission function (eg.: for MMC-MVDC applications with an insulation voltage level is up to 30kV).

Thus, this section details the design methodology to optimize a selected DC-DC power supply topology by the help of a virtual prototyping tool. The optimization strategies are: to optimize a pot core transformer by the help of FEMM^{TM}, to simulate the selected DC-DC converter by the help of LTSpice^{TM}, and a GA code is used to run these two simulators to obtain the optimization objective.

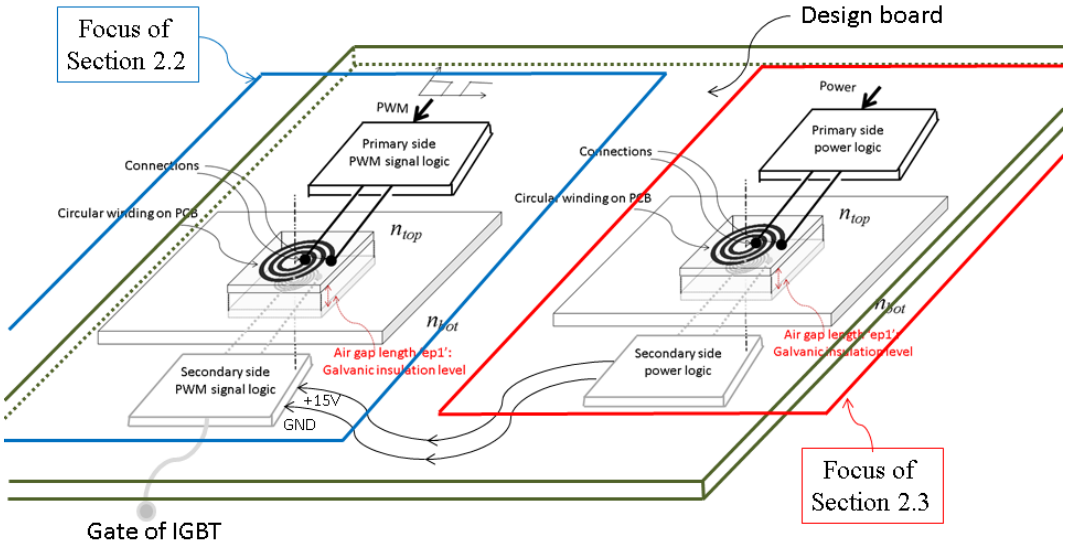


Fig. 2.15.: Example of a design board for a single channel IGBT gate driver: a signal transmission function and a power transmission function with two insulation transformers.

Maximize the efficiency of the proposed DC-DC converter is set as our main optimization objective. And then, as IGBT gate drivers system requires low power supply (1W to 3W), minimize the converter output power P_{out} is set as another optimization objective. This support objective also helps the gate drivers' designers to choose an optimal solution. Hence, maximize the converter efficiency (η_{con}) and minimize the converter output power (P_{out}) form a bi-objective optimization problem. This bi-objective optimization problem of the overall system that leads to a Pareto front is presented.

As presented in previous sections, with the same ferrite dimension, pot core ferrite transformers provide better performances compare to double-layer planar transformer. Thus, at this stage, pot core ferrite forms are chosen. But the diameter is bigger than the signal transmission function. Three pot core diameters 14mm, 18mm and 22mm are selected. The reasons to choose these ferrites are the output power of a DC-DC converter (at least 1W), and to achieve high transformer coupling (to obtain high converter efficiency).

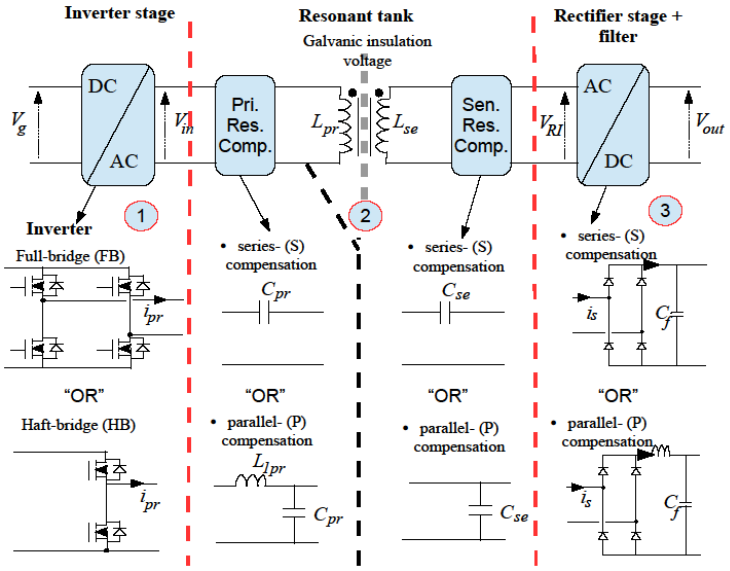
Thus, based on a set of insulation layer ep_1 and pot core ferrite diameters D_F, numerous optimization Pareto fronts' results are shown. Then, these results are compared till the suitable solution for practical works is made.

2.4.1. Basic overview of high insulation voltage power supply topologies

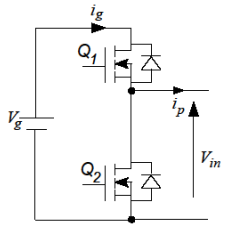
There are two main categories of DC-DC power converters. One is non-insulated topologies (buck, boost …) and the other one is insulated topologies (flyback …). The article [Sem14] shows several insulated (based on magnetic transformer) topologies and the power ranges are also mentioned. In order to increase the barrier insulation level, the air gap transformer must be increased. This means that the high insulation voltage barrier transformer design will lead to have a low coupling coefficient (k). For this loosely coupled transformer, the main drawbacks are the leakage inductances on the primary and secondary sides. Thus, the power supply designers proposed the DC-DC converter topologies which can take these leakage inductances as an advantage. Finally, resonant converter topologies are proposed to mitigate these leakage inductances.

Actually, in literatures, DC-DC resonant converter topologies are combined by several aspects: transmitter structure side (inverter bridge), resonant tank topologies, rectifier network and output filter. Fig. 2.16a presents all the possible combinations of DC-DC resonant topologies. In this dissertation, the converter transmitter side converts the DC signal (V_g) to AC signal (V_{in}) and can be performed by a full-bridge (FB) or a half-bridge (HB) structure. As shown in Fig. 2.16b-c, the input voltage V_{in} of a resonant tank of these two bridges are illustrated. According to [Bos14], the first harmonic approximation is sufficiently accurate for this system analysis. With HB configuration, this input voltage V_{in} is a square waveform oscillating between 0 and $+V_g$. And with FB configuration, the input voltage of resonant tank V_{in} is a square waveform oscillating between $-V_g$ and $+V_g$. Therefore, for a brief comparison between them, if the same bridge output power is desired, the half-bridge input voltage needs to be twice as high as the full-bridge input. Thus, in this work, the FB structure is a suitable choice in term of low input voltage (V_g = [12V-15V]).

The resonant tank configurations can be series resonant (S) or parallel resonant (P) between the transformer and the compensation capacitors. To enhance the power transfer and achieve high efficiency, DC-DC insulated resonant converters should resonate on both sides of the transformer. In [Chw05] (see Fig. 2.16a), several resonant tanks (series-series: SS, series-parallel: SP, parallel-series: PS, parallel-parallel: PP) and its equivalent impedance models are presented for a contactless electric vehicle battery charger application. The article [Bos15] presents the complexities and disadvantages of a parallel compensation of the transmitter and receiver coils. According to [Hei98] and [Bos15], the parallel configuration at the inverter side requires an additional inductor connected in series between the resonant tank and the power converter side. This series inductor is used to regulate the inverter current i_{pr} flowing into the parallel resonant tank. As presented in [Gre94], the parallel resonant configuration at the transmitter coil side is useful for contactless power distribution networks, where the high circulating current is controlled in a track to supply multi receivers. But for only one receiver, as considered in this dissertation (cf. Fig. 2.16a), this inductor will leads to increase the total converter losses. A parallel compensation at the secondary side coil requires the high circulating current at the primary side of the transformer and an additional inductor in the output

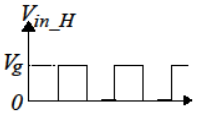


(a)



Fundamental component:

$$V_{in\_H} = \frac{4}{\pi}\frac{V_g}{2}\sin(\omega t) \qquad (2.8)$$



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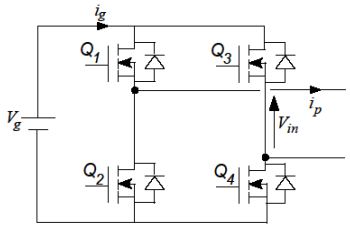
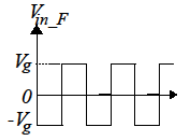


Fundamental component:

$$V_{in\_F} = \frac{4}{\pi}V_g \sin(\omega t) \qquad (2.9)$$



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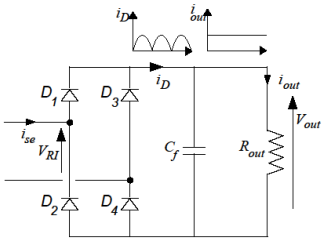

Fundamental component:

$$V_{RI} = \frac{4}{\pi}V_{out}\sin(\omega t) \qquad (2.10)$$

(d)

Fig. 2.16.: Description of insulated DC-DC resonant converter topologies:
(a) Possible DC-DC resonant converters,
(b) A half-bridge (HB) configuration,
(c) A full-bridge (FB) configuration,
(d) *A rectifier network.*

filter at the receiver side is needed (cf. Fig. 2.16a and [Bos15]). This normally leads to increase the winding losses in the transformer as well as the converter total losses. In addition, the voltage transfer ratio of the parallel compensations topology is always dependent to the magnetic coupling (k) of the transformer and the load. In [Chw05] and [Zhi14], the advantages of SS resonant tank with loosely coupled transformer are presented: the voltage ratio can be independent of the magnetic coupling of the transformer and the load; an additional inductor is not needed; that ensure a high efficiency by minimizing the circulating current through a transformer. Thus, in this application, SS resonant tank is selected.

Next, as shown in Fig. 2.16d, the rectifier network produces DC voltage by rectifying the AC current with rectifier diodes and a capacitor C_f.

Finally, the complete DC-DC full-bridge series-series (FB-SS) resonant converter is illustrated in Fig. 2.17a.

2.4.2. DC-DC full-bridge series-series (FBSS) resonant converter

In this section, a DC-DC FBSS resonant converter modeling is proposed: the series-series (SS) resonant tank, the voltage transfer ratio ($G_v = V_{out}/V_g$), the zero voltage switching (ZVS) condition for minimizing switching losses and the converter total losses are mentioned sequentially.

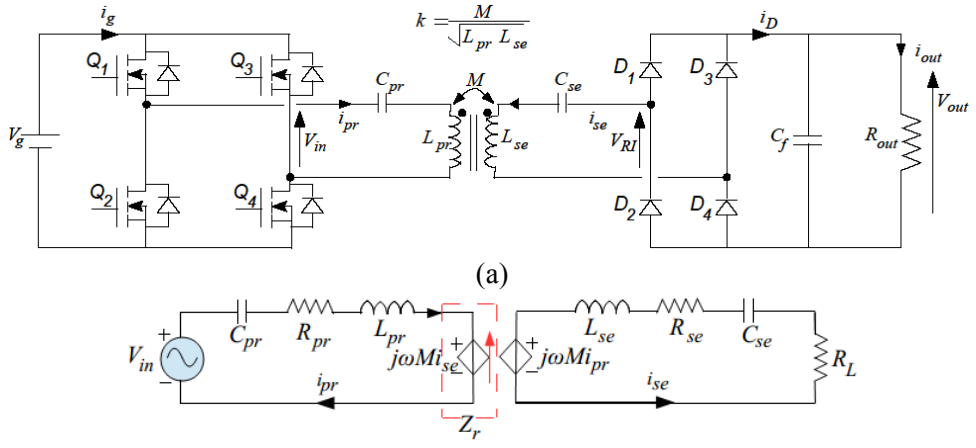

Fig. 2.17.: A selected resonant converter topology for this high insulation application:
(a) DC-DC full-bridge series-series (FBSS) resonant converter, and
(b) A mutual coupling modeling of this structure.

2.4.2.1. Series-series (SS) resonant tank modeling

L_{pr}, L_{se} and M are the primary side inductance, the secondary side inductance and the mutual inductance of the transformer, respectively. R_{pr} and R_{se} are the winding resistances of the transformer that depend on the operating frequency due to skin effect. C_{pr} and C_{se} are the primary and secondary external compensation capacitors, to enhance the energy transfer from input voltage tank V_{in} to an equivalent output loading resistance

R_L. These capacitors are calculated as expressed in Equations (2.11) and (2.12). The mutual coupling inductance model of the SS resonant tank is presented in Fig. 2.17b.

$$C_{pr} = \frac{1}{\omega^2 L_{pr}} \tag{2.11}$$

$$C_{se} = \frac{1}{\omega^2 L_{se}} \tag{2.12}$$

Where, $\omega = 2\pi f_{sw}$, f_{sw} is a switching frequency. The voltage dependent source ωMi_{se} in Fig. 2.17b can be replaced by an equivalent impedance Z_r which is calculated by dividing ωMi_{se} with i_{pr}. And other equivalent impedances for the resonant system are described in [Chw05], [Zhi14], and summarized in Table 2.10.

Table 2.10: Parameters' calculations from Fig. 2.17

Definition	**Equations**
Primary side impedance	$Z_{pr} = j\omega L_{pr} + 1/j\omega C_{pr} + R_{pr}$
Secondary side impedance	$Z_{se} = j\omega L_{se} + 1/j\omega C_{se} + R_{se}$
Equivalent impedance	$Z_r = (\omega M)^2/(Z_{se} + R_L)$
Primary side current	$i_{pr} = V_{in}/(Z_{pr} + Z_r)$
Secondary side current	$i_{se} = j\omega M i_{pr}/(Z_{se} + R_L)$
Equivalent load	$R_L = 8R_{out}/\pi^2$
Output voltage of resonant tank	$V_{RI} = R_L i_{se}$

2.4.2.2. Voltage transfer ratio G_v

From the parameter calculations in Table 2.10, by replacing i_{pr} into i_{se}, the expression of fundamental output voltage V_{RI} divided by input voltage V_{in} is defined. Next, the voltage transfer function (G_v) (output voltage V_{out} divided by V_g) is derived: Equation (2.15).

$$i_{se} = \frac{j\omega M V_{in}}{(Z_{pr} + Z_r)(Z_{se} + R_L)} \tag{2.13}$$

$$V_{RI} = R_L \frac{j\omega M V_{in}}{(Z_{pr} + Z_r)(Z_{se} + R_L)} \tag{2.14}$$

$$G_v = \frac{V_{out}}{V_g} = \frac{j\omega M}{\frac{Z_{pr}Z_{se} + (\omega M)^2}{R_L} + Z_{pr}} \tag{2.15}$$

From Equations (2.8)-(2.9) and Equation (2.14), the expression of G_v of FB-SS is expressed in Equation (2.15). According to [Zhi14] [Wei14], and Equation (2.15), the G_v can operate independently of the magnetic coupling (k) and the load (R_L) at two different

specific frequencies ($f_{v,l} = f_{res}/\sqrt{1+k}$ is lower than resonance frequency and $f_{v,h} = f_{res}/\sqrt{1-k}$ is higher than resonance one, where f_{res} is the resonant frequency). As an example, the capacitors of 22nF are selected to resonate with transformer inductances ($L_{pr} = L_{se} = 4.66\mu H$) at 500 kHz. Loading conditions vary from 45Ω to 105Ω. In Fig. 2.18, their magnitudes G_v are plotted. As shown in this figure, $f_{v,l}$ and $f_{v,h}$ are the two frequencies where G_v is independent of R_L.

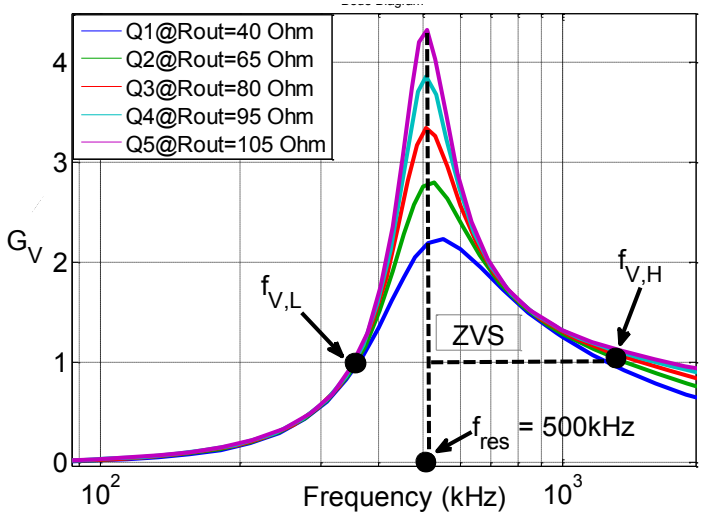

Fig. 2.18.: Magnitude analysis of voltage transfer ratio G_v

2.4.2.3. Zero voltage switching (ZVS) consideration

In order to reduce the switching losses, the designer must pay attention for the choice of the converter topology which can achieve zero voltage switching (ZVS) condition. In this case, each MOSFET turns on when the voltage across it is zero. Theoretically, it will imply zero switching losses. However, zero switching losses are not strictly achievable in practice. Therefore, even with a small deviation from the ideal case, the converter with high efficiency will be achieved. To achieve ZVS on the inverter switches for FB-SS resonant converter, the input impedance Z_{in} of the resonant circuit must exhibit an inductive behavior. Then, the phase angle (φ_{in}) of the input impedance must be greater than zero ($\varphi_{in}>0$).

Equations below present the analysis of Z_{in}:

$$Z_{in} = Z_{pr} + Z_r \tag{2.16}$$

$$R_{in} = \frac{\omega^2 M^2 R_L}{\left(\omega L_{se} - 1/\omega C_{se}\right)^2 + R_L^2} \tag{2.17}$$

$$X_{in} = \left(\omega L_{pr} - 1/\omega C_{pr}\right) - \frac{\left(\omega L_{se} - 1/\omega C_{se}\right)}{\left(\omega L_{se} - 1/\omega C_{se}\right)^2 + R_L^2} \tag{2.18}$$

$$\varphi_{in} = \frac{180}{\pi} tan^{-}(\frac{X_{in}}{R_{in}}) \quad (2.19)$$

As shown in Fig. 2.18, at the resonant frequency point (f_{res}), the input phase angle φ_{in}=0, thus Z_{in} is always resistive. In the frequency range $f_{v,l}$ to $f_{res.}$, the input impedance Z_{in} is always capacitive. In the frequency range f_{res} to $f_{v,h}$, the input impedance Z_{in} is always inductive. Thus, in order to achieve ZVS, the operating frequency f_p of the converter must be in the range f_{res} to $f_{v,h}$ (see Fig. 2.18).

2.4.2.4. Converter loss analysis

The losses of the converter mainly come from three parts: primary inverter full-bridge stage (4 MOSFETs), series-series resonant tank stage (mainly from transformer), and rectifier network (4 diodes). The losses calculations are based on the simulated or measured current waveforms and the manufacturer's datasheet.

Inverter full-bridge losses: power losses of semiconductor components can be divided into two groups: conduction losses and switching losses. In Equation (2.20), the switching loss is expressed as a function of the switching actions of the MOSFET current ($i_{SW,M}$(i), where i can be MOSFET Q_1, MOSFET Q_2, MOSFET Q_3, MOSFET Q_4), the drain-source voltage (V_{DS} =V_g), the rise time (t_r), the fall time (t_f) and the operating frequency (f_p). The conduction losses can be calculated using the MOSFET drain-source on-state resistance (R_{DS}) and the root mean square value of MOSFET simulated or measured current waveforms ($i_{M,rms}$(i)) (Equation (2.21)).

$$P_{SW,M(i)} = V_{DS} i_{SW,M(i)} \left(t_r + t_f\right) f_P \quad (2.20)$$

$$P_{CON,M(i)} = R_{DS} \cdot i^2_{M,rms(i)} \quad (2.21)$$

Rectifier network losses: according to [Fan15], the switching losses of the rectifier are almost eliminated in the case of Schottky diodes. The main losses are the conduction losses which can be expressed as:

$$P_{CON,D(i)} = V_D \frac{V_{out}}{R_o} + R_D \cdot i^2_{D,rms(i)} \quad (2.22)$$

Transformer losses: the transformer losses are a large part of the total losses of the converter. The transformer losses can be divided into two main parts: core losses and winding losses. The core losses can be described as in Equation (2.23) and the winding losses are expressed in Equation (2.24).

$$P_{C,T} = \rho f^{\alpha} B_m^{\beta} V_e \quad (2.23)$$

$$P_{cu,T} = R_{pr} i^2_{p,rms} + R_{se} i^2_{s,rms} \quad (2.24)$$

Finally, the converter efficiency can be computed by:

$$\eta_{con} = \frac{P_{out}}{P_{out} + P_L} \tag{2.25}$$

where, $P_{out} = {V_{out}^2}/{R_{out}}$ and $P_L = P_{SW,M(i)} + P_{CON,M(i)} + P_{CON,D(i)} + P_{C,T} + P_{Cu,T}$: the total losses of converter.

2.4.3. Power transmission function optimization descriptions

In this section, the optimized design of the power transmission function IGBT gate driver with high insulation barrier capabilities by the help of virtual prototyping tool is presented.

2.4.3.1. Power transmission optimization variables and parameters

Optimization variables: x_1, n_1 and n_{layer} are considered as optimization variables. But, x_2 is regarded as an internal variable and can be computed after the values of x_1, n_1, ep_9 and ep_4 are set (see Fig. 2.9b/Fig. 2.19 and Equation (2.7)). The combinations of different copper layer (ep_2), PCB multi-layer (ep_6) and number of layers (n_{layer}) must be considered carefully for the transformer design. So ep_2, ep_6 and n_{layer} should be included in the optimization vector. Hence, (x_1, n_1, ep_2, ep_6, n_{layer}) are the main geometrical variables.

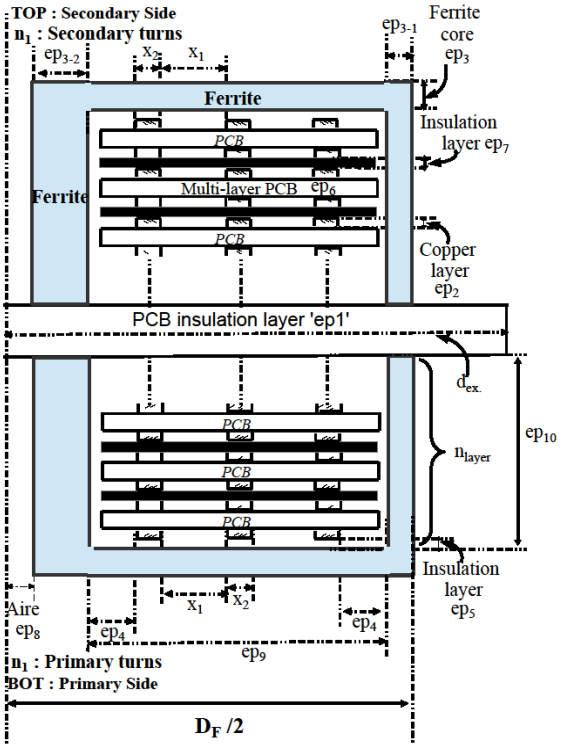

Fig. 2.19.: Multi-layer pot core transformer 2D description (re-call of Fig. 2.9).

As shown in Fig. 2.17a, C_{pr}, C_{se}, R_{out} and the operating frequency (f_p) are regarded as electrical optimization variables. According to series-series resonant tank modeling, in order to enhance the energy transfer from primary side to secondary side, C_{pr} and C_{se} must be designed attentively: these two capacitors are then considered as electrical optimization variables. As presented previously, in order to achieve ZVS condition, the converter's operating frequency f_p is a main variable to be considered. Then, the operating frequency f_p must be located between the resonant frequency f_{res} (where the voltage transfer ratio G_v is at the peak) and the frequency point where the voltage transfer ratio $G_v = 1$ (at the high side). The output power of this converter is up to 10W. The output voltage V_{out} must be higher or equal to the input voltage V_g = [12V – 15V]. Thus, to achieve the desired output power, R_{out} should be regarded as one of the electrical variables.

Thus, the optimization variables are defined in the vector $\overline{X_v}$ and summarized in Table 2.11.

Table 2.11: Optimization variables' definitions for power transmission function

Geometrical variables ***(Pot core transformer: cf. Fig. 2.19)***	***Electrical variables*** ***(DC-DC FBSS converter: cf. Fig. 2.17a)***
• x_1 : distance between two copper windings for both sides, • n_1 : turn numbers of transformer, • ep_2 : copper thickness, • ep_6 : multi-layer PCB thickness, • n_{layer} : number of layers	• C_{pr} : compensation capacitor at primary side, • C_{se} : compensation capacitor at secondary side • f_p : operating frequency, • R_{out} : output resistance.
Optimization variables	
$\overline{X_V} = \{x_1 , n_1 , ep_2 , ep_6 , n_{layer} , C_{pr} , C_{se} , f_p , R_{out}\}$	

Optimization parameters: the constant parameters are presented in Table 2.12. These constant parameters come from the pot core transformer definition. The galvanic insulation barrier is still in the range of 0.5mm to 3mm to respond to several different high insulation voltage applications. Three pot core diameters (14mm, 18mm and 22mm) are selected. Other numerical values and their descriptions are both provided in Table 2.12.

Table 2.12: Optimization parameters' definitions for the power transmission function

Geo. para.	*Values*	*Descriptions*
• ep_1	{0.5mm to 3mm}	galvanic insulation barrier
• ep_4	0.2 mm	extra length of the ferrite relative to the edge of the last coil
• ep_7	18 µm	insulation thickness between layers of multi-layer
• D_F	{14mm, 18mm, 22mm}	ferrite pot core diameters
• ep_3, ep_{3_1}, ep_{3_2}, ep_8, ep_9, ep_{10}	depend on pot core dimensions	Pot cores: 14mm, 18mm and 22mm
• ep_5	depends on ep_7, ep_2, ep_6, ep_{10}, and n_{layer}	Equation (2.6) : insulation between coils and ferrite
• x_2	depends on x_1, n_1, ep_9 and ep_4	Equation (2.7) : copper width (*internal variable*)
Optimization parameters		
$\overline{P_v} = (ep_1, ep_3, ep_{3\_1}, ep_{3\_2}, ep_4, ep_5, ep_7, ep_8, ep_9, ep_{10}, x_2, D_F)^t$		

2.4.3.2. Power transmission optimization objectives

Maximize the converter efficiency η_{con} is the main optimization objective. And then, the output power P_{out} is defined as another optimization objective to provide a feasible configuration for experimental works. Thus, the proposed Pareto fronts are: the converter efficiency (η_{con}) as a function of the converter output power (P_{out}).

2.4.3.3. Power transmission optimization constraints

The optimization variables' constraints are summarized in the higher part of Table 2.13. Some variables are discrete values and some others are real values. Beside the optimization variables' constraints, the optimization (geometrical and electrical) constraints (for $P_{out} \leq 10W$) are also required. These constraints are summarized in the lower part of Table 2.13. To ensure that the designed converter power is under 10W, the output voltage stays between the input voltage (V_g = [12V – 15V]) and 20V. And the output current i_{out} must be lower than 0.5A. As presented above, the high magnetic coupling of transformer provides high converter efficiency. Thus, the coupling coefficient *k* should be higher than 0.2. ep_5 should be set under 0.3mm for technical constraint of pot core planar transformer. The final constraint is the parasitic capacitor between the primary side and secondary side (C_{ps}). This capacitor should be set under 10pF for electromagnetic compatibility (EMC) reasons.

Table 2.13: Optimization constraints for the power transmission function

Variable constraints	*Values*	*Variable types*
• x_1	[0.2mm, 0.5mm]	Real
• n_1	{1, 2, 3, 4, 5}	Integer
• ep_2	{35, 70, 105, 210, 235, 435} [µm]	Integer
• ep_6	{0.4, 0.5, 0.8, 1.2, 1.6} [µm]	Integer
• n_{layer}	{1, 2, 3, 4, 5}	Integer
• C_{pr}	[1nF, 10nF]	Real
• C_{se}	[1nF, 10nF]	Real
• f_p	[150kHz, 1MHz]	Real
• R_{out}	[10Ω, 100Ω]	Real
Technical constraints		
• $V_g \leq V_{out} \leq 20V$, $i_{out} \leq 0.5A$, • $B_m \leq B_{sat}$, $k > 0.2$, $ep_5 \leq 0.3mm$ and $C_{ps} < 10pF$		

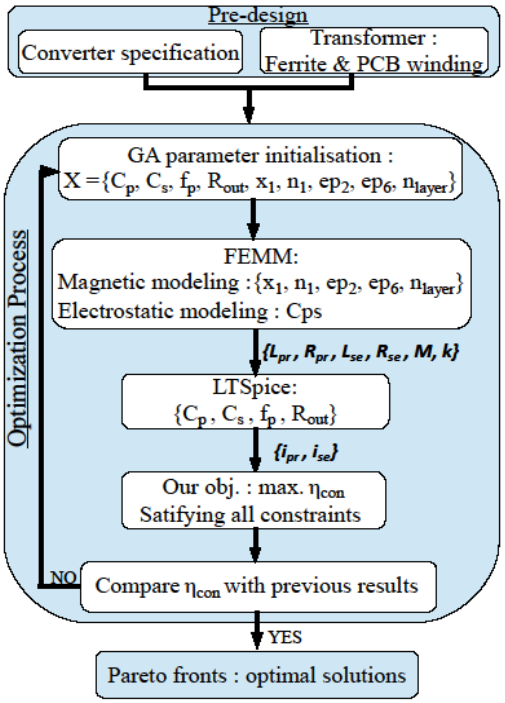

Fig. 2.20.: Optimization flowchart with genetic algorithm (GA) code in a MATLAB™ script.

2.4.3.4. Power transmission computation procedure and optimization algorithms

The optimization flowchart is described in Fig. 2.20. It combines a finite element simulation (FEMM™) and an electrical transient simulator (LTSpice™) software with the help of a genetic algorithm (GA) coded with MATLAB™. FEMM™ software calculates

the electrical parameters of transformer (L_{pr}, R_{pr}, L_{se}, R_{se}, M, k, and C_{ps}) with the help of geometrical variables (x_1, n_1, ep_2, ep_6 and n_{layer}). After that, LTSpice^{TM} software runs a transient simulation with the help of (L_{pr}, R_{pr}, L_{se}, R_{se}, M, k) and electrical (C_{pr}, C_{se}, R_{out} and f_p) variables. Next, all the electrical waveforms (currents and voltages) of each component are simulated to calculate losses. If all constraints are satisfied, the converter efficiency η_{con} is computed by the help of the total loss evaluation. Finally, the converter efficiency η_{con} is plotted as a function of the output power (Pareto fronts).

2.4.4. Power transmission optimization results: Pareto fronts' results

The set of Pareto fronts' solutions are presented and analyzed to make a suitable choice for prototype fabrications. The parameters of the GA are: 30 individuals and 100 generations which require 2 hours of computational times per one diameter and one insulation layer ep_1. As presented in Table 2.12, diameters of pot core which have been selected are 14mm, 18mm and 22mm. And the insulation thickness ep_1 varies between 0.5mm to 3mm. Thus, several Pareto fronts' results are obtained and illustrated in Fig. 2.21.

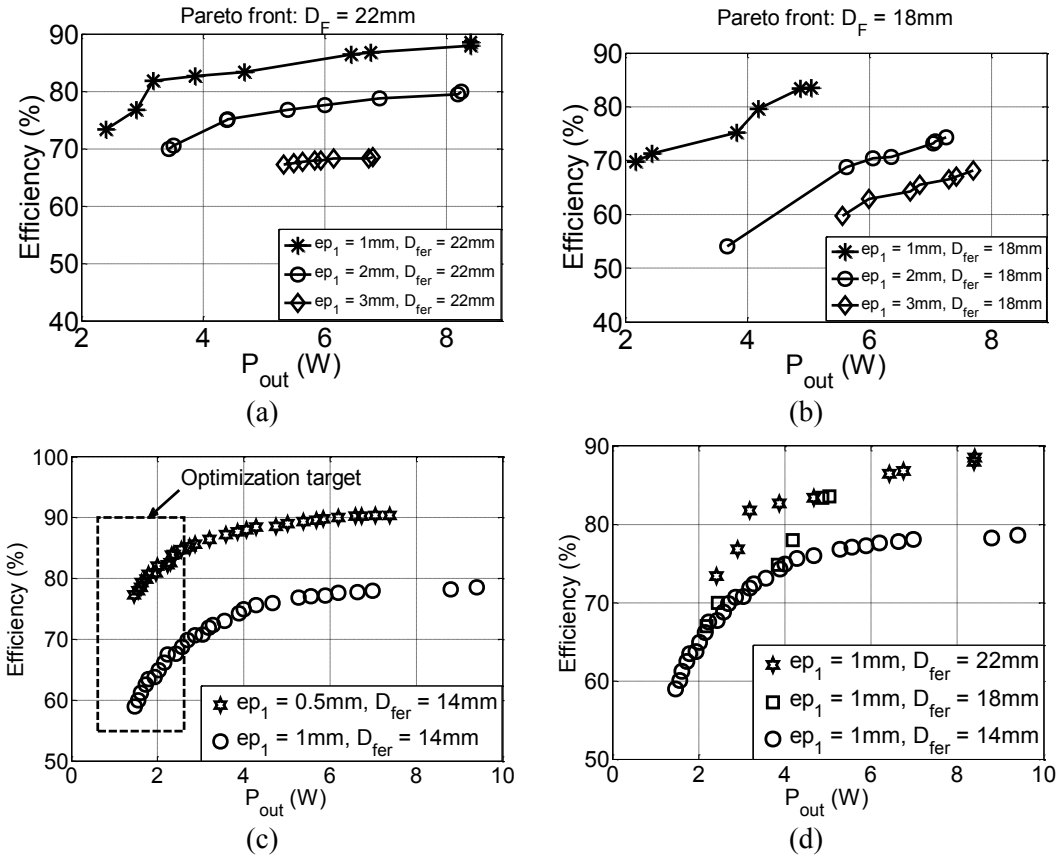

Fig. 2.21.: Optimization results for power transmission IGBT gate drivers:
(a) Pareto fronts' results for D_F = 22mm and ep1 = {1mm, 2mm, 3mm},
(b) Pareto fronts' results for D_F = 18mm and ep1 = {1mm, 2mm, 3mm},
(c) Pareto fronts' results for D_F = 14mm and ep1 = {0.5mm, 1mm},
(d) Pareto fronts' results for D_F = {14mm, 18mm, 22mm} and ep_1= 1mm.

Theoretically, for the same ferrite diameter and the same winding configurations, the lower air gap length leads to have a higher coupling coefficient (k) and higher inductor values ($k_{ep1=\ 0.5mm} > k_{ep1=1mm} > k_{ep1=\ 2mm} > k_{ep1=3mm}$ and $L_{ep1=0.5mm} > L_{ep1=1mm} > L_{ep1=2mm} > L_{ep1=3mm}$). Moreover, from the FOM (Figure Of Merit) factor analysis in [Kne15], the converter efficiency is expressed: $\eta \approx 1 - 2/(kQ)$. Where, the inductive quality Q is proportional to the inductance and frequency, but inverse to the winding resistance. So, the higher magnetic coupling k, L_{pr} and L_{se} values provide the higher converter efficiency. Hence, for each diameter and the same converter output power, the predicted efficiency is: $\eta_{ep1=0.5mm} > \eta_{ep1=1mm} > \eta_{ep1=2mm} > \eta_{ep1=3mm}$. As an evident of these analysis, Fig. 2.21a-c present the Pareto fronts' results for ferrite pot core diameters 22mm, 18mm and 14mm. Each Pareto front represent the optimal design for one thickness of the insulation layer (ep_1 = {0.5mm, 1mm, 2mm and 3mm}). Moreover, Fig. 2.21d focuses on 1mm of insulation layer with three pot core diameters {14mm, 18mm, 22mm}. According to this figure, with the same insulation thickness, the highest diameter provides the highest converter efficiency.

To further analyze the practical aspect, the supplied power is around 2W at 10 kHz for 3.3kV IGBT modules in a Medium-Voltage Direct Current Modular Multilevel Converter (MVDC-MMC) application (where a 30kV of insulation voltage is required). Moreover, as demonstrated in Section 2.2: insulation dielectric material validations, 1mm of polysterimide material can sustain at least 40kV of insulation voltage level. Thus, according to Fig. 2.21, some optimal solutions of the Pareto fronts' results of 14mm (pot core diameter) are the dominants solutions in term of power density, final application requirements, etc. These selected solutions are plotted in Fig. 2.22. For experimental results, we have chosen the solution (a) that corresponds to an output power of 2W with an insulation thickness of 0.5mm and a ferrite core of a diameter of 14mm.

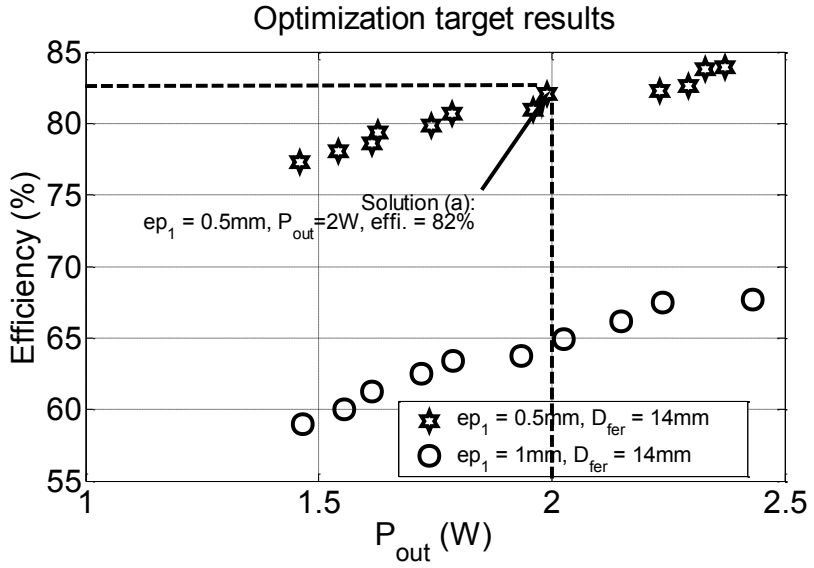

Fig. 2.22.: Optimization target results for experimental works.

The simulation results of this solution are summarized in Table. 2.14. The converter needs to operate at 266 kHz to achieve ZVS conditions and obtain high efficiency. Series capacitors are equal to 68nF. The characteristics of the optimal transformer are: 4 multi-layers, 2 turns per side of layer, 105µm of copper thickness, etc. As a result, $L_{pr} = L_{se}$ =17.24µH, $R_{pr} = R_{se}$ = 0.46Ω and C_{ps} = 6.67pF are the electrical values of this optimal transformer.

Table 2.14: Simulation results of the optimal solution (a)

Opti. obj.	**Solution (a)**		
η_{con}	82 %		
ep_1/D_F	0.5 mm/14 mm		
C_{pr} / C_{se}	68 nF/ 68 nF	P_{out}	2 W
f_p	266 kHz	V_{out}/ I_{out}	12.3V/ 0.16A
R_{out}	76.9 Ω	L_{pr} / R_{pr}	17.24 µH/ 0.46Ω
x_1 / x_2	0.25 mm /0.87mm	L_{se} / R_{se}	17.24 µH/ 0.46Ω
n_1 / n_{layer}	2 turns / 4 layers	M / k	10.49 µH / 0.6
ep_2 / ep_6	105 µm / 0.4 mm	C_{ps}	6.67 pF

Fig. 2.23 presents the simulation results of the optimal solution (a). Fig. 2.23a plots the voltage transfer ratio G_v. According to this figure, the ZVS condition can be achieved from 160 kHz to 350 kHz. This frequency range must verify all the optimization constraints. The output voltage constraint must be between V_g = [12V – 15V] and V_{out} < 20V. Thus, according to this figure and V_{out} < 20V, the operating frequency ranges is from 200 kHz to 350 kHz. Fig. 2.23b illustrates the input voltage of a resonant tank V_{in}, primary side current i_{pr}, and secondary side current i_{se} for the solution (a).

Influence of the switching frequency: Fig. 2.23c shows the converter efficiency (η_{con}) obtained from simulation as a function of the frequency. According to this figure, the switching frequency of 200 kHz provides the highest efficiency which correspond the highest converter output voltage and power (see Fig. 2.23a).

Fixed frequency application: as shown in Table 2.15, at a fixed frequency operating mode, when the load varies, the converter efficiency is a function of the output power. The load resistance R_{out} varies from 39Ω to 82Ω and corresponds to V_{out} from 12.47V to 13.07V (see Fig. 2.23e and Table 2.15). This achieves the efficiency from 82% to 88% and output power from 2W to 4W (cf. Fig. 2.23d).

Table 2.15: Summarized results of fixed frequency and varied loads

R_{out} (Ω)	***V_{OUT} (V)***	***P_{out} (W)***	***η_{con} (%)***
39	*12.47*	*2*	*82*
47	*12.64*	*2.8*	*85.5*
56	*12.93*	*3.4*	*86.2*
82	*13.07*	*4*	*88*

In Chapter 3, the experimental results are provided and compared to the simulation ones to validate our proposed design methodology.

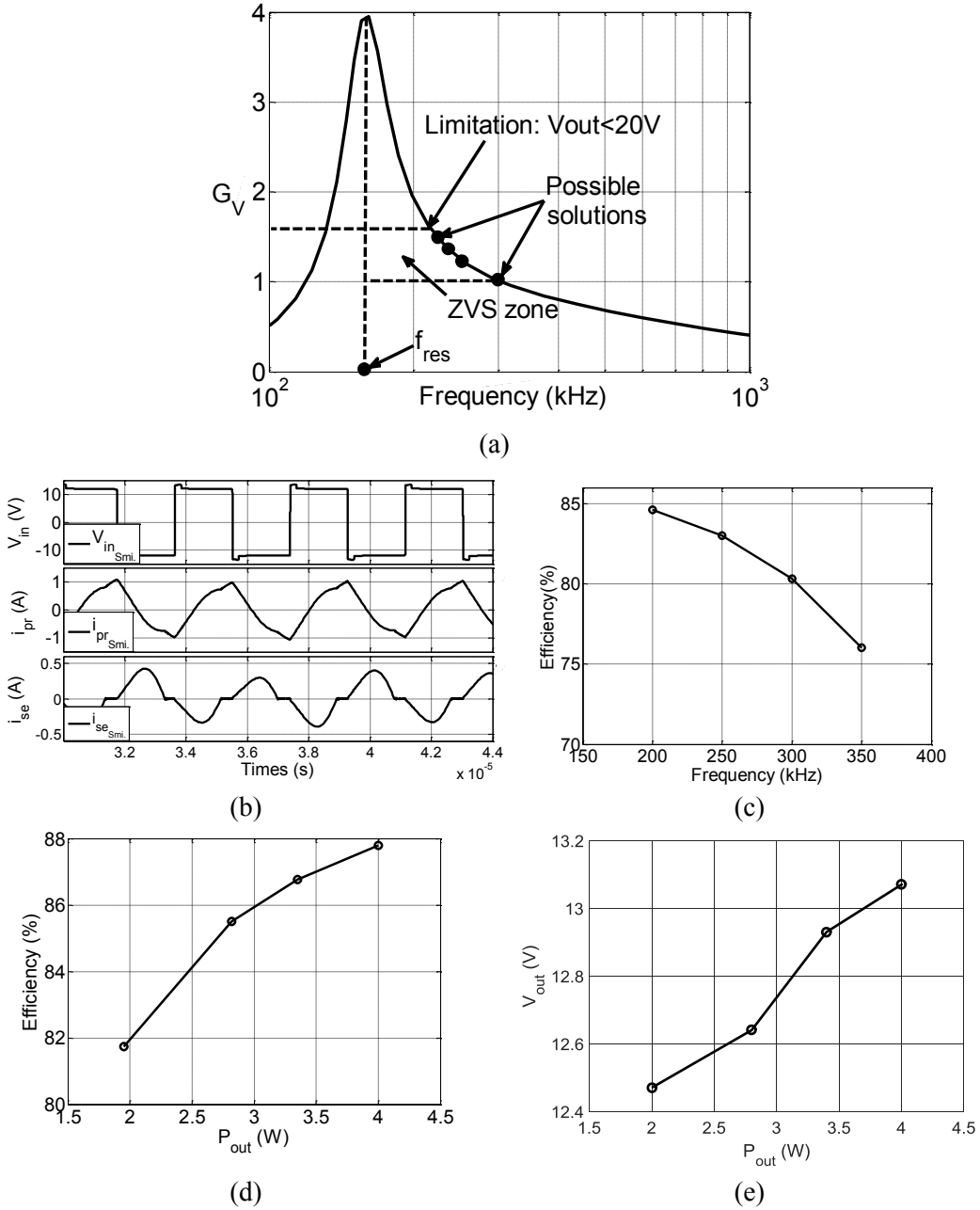

Fig. 2.23.: Simulation results for the optimization solution (a):

(a) Voltage transfer ratio G_v of the optimal solution,

(b) Simulation waveforms of input tank voltage V_{in}, primary current i_{pr}, secondary current i_{se},

(c) Power converter efficiency as a function of the operating frequency,

(d) Power converter efficiency for a frequency of 200 kHz and resistive load varies from 39Ω to 82Ω,

(e) The converter output voltage (V_{out}) as a function of the converter output power (P_{out}) for a fixed frequency of 200kHz and resistive load varies from 39Ω and 82Ω.

2.4.5. Conclusion: power transmission function for IGBT gate drivers

In this thesis dissertation, a DC-DC full-bridge series-series (FBSS) resonant converter is selected. The high insulation voltage barrier must be achieved by the help of a pot core planar transformer with its air gap material. The optimized design for this system is proposed with the help of a virtual prototyping tool. This pre-sizing step is very important for the prediction of the converter performances. Optimize the geometrical aspects of the transformer is performed through a finite element software (FEMM^{TM}). Then, a transient simulator software LTSpice^{TM} is used to simulate the electrical circuit. Maximize the converter efficiency and minimize the converter output power define a bi-objective optimization problem. Some pot core dimensions (D_F = {14mm, 18mm and 22mm}) and some insulation thicknesses (ep_I = {0.5mm, 1mm, 2mm, and 3mm}) provide several Pareto fronts'. Finally, a Pareto front of a pot core of 14mm (diameter) and 0.5mm of insulation thickness is selected for further analysis. Then, an optimal solution is chosen for experimental works. The main characteristics of the proposed solution are the output power of around 2W and the insulation voltage level of around 30kV.

In Chapter 3, the experimental results will be presented and analyzed. Then, the comparisons between the simulation and experimental results are taking place to validate our proposed optimization methodology.

2.5. Voltage measurement for SM

On main feature on the MMC structure is to control the voltage of the capacitor sub-module. Therefore, it is necessary to obtain the voltage of each sub-module in order to use voltage balancing technics. The most critical one are based on a voltage measurement, a sorting between all the values in order to determine which sub-module has to be inserted. However, this necessitates an accurate measurement based on voltage sensors and the necessity to insulate data. This can be done by an insulation of the analogic signal which can be tricky due to EMC perturbations or by the transmission of a digital value based on the use of an analog to digital converter implemented on the sub-module. This solution needs a high speed data transmission. Another family of voltage control algorithms is based on tolerance band solutions. That means that for these sorting algorithms, the information that the voltage is inside or outside of a tolerance band is sufficient. In this section, we present a new concept for measurement of the sub-module capacitor voltage which is well suited for this type of voltage control algorithms.

2.5.1. Voltage measurement for voltage balancing: different techniques

Our concept uses gate drivers system to replace the sensors: the gate driver provides voltage range (3 ranges) with a state {-1, 0, 1} (see Fig. 2.24). For example, if voltage of sub-module (j) is higher than 10% of its reference, its state is equal to 1. In case of -10% of V_{ref}, its state is equal to -1. And in the case of the sub-module voltage stays in the +/-10% zone of its reference, its state is 0. Thus, we define three states {-1, 0,

1} for sub-module voltage as summarized in Table 2.16. Then, we add counters for SMs to count their past states. From these informations, a novel capacitor voltage balancing algorithm is proposed and summarized in Fig. 2.24.

Table 2.16: States of sub-module voltage compared to its reference

V_{SM}	*States*
$V_{SM} \geq 10\% V_{SM,ref}$	1
$-10\% V_{SM,ref} \leq V_{SM} \leq 10\% V_{SM,ref}$	0
$V_{SM} \leq -10\% V_{SM,ref}$	-1

First, the states of capacitor voltages and total past actions of their counters are sorted. Then, the numbers of SMs that need to be inserted (or switched on) for upper arm and lower arm are calculated at PWM stage. As presented in Fig. 2.24, these informations and polarities of arm currents are the inputs of the selection algorithms. Then, the gate signals are generated to IGBTs in SMs by the help of IGBT gate drivers systems. Within these systems, the voltage states of each SM are obtained. And they are considered as the inputs of capacitor voltage balancing algorithm.

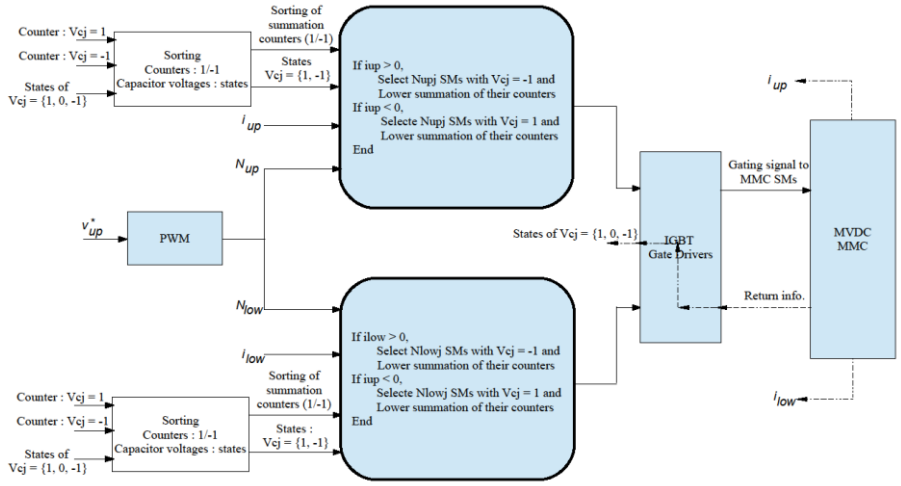

Fig. 2.24.: A novel capacitor voltage balancing algorithm with voltages states

To support this proposed idea, we provide preliminary simulation results of the converter specification in Table 2.17. According to this table, the capacitor voltage of each sub-module must stay around 15V ($V_{dc}/N = 60/4 = 15V$).

Table 2.17: MMC converter specification for testing a proposed novel capacitor voltage balancing algorithm with only three capacitor voltage states

DC voltage V_{DC}	60 V
Number of sub-modules per arm (N_{SM})	4
C_{SM}	1 mF
Load (R_{load}/L_{load})	11.25Ω / 10mH
L_{arm}/R_{arm}	400µH/1.5Ω
modulation (m)	0.85
Switching frequency (f_{sw})	100kHz

Fig. 2.25 presents the simulation for two different capacitor voltage balancing methods: on-line capacitor voltages with voltage sensors (solution (1)) and three voltage states {-1, 0, 1} within IGBTs gate drivers systems (solution (2)). Fig. 2.25a and Fig. 2.25b illustrate the voltage balancing of a proposed novel method and classical method, respectively. According to these figures, after 0.15s, all the capacitors voltages follow their references. As seen in Fig. 2.25a, all the capacitors voltages for upper arm and lower arm are not well balanced (compare to classical method in Fig. 2.25b) but they stay around their references. Its ripple voltage (ΔV) is about 6V (3 times higher than voltage sensors solution: see Fig. 2.25b, ΔV = 2V). These are major critical points for our proposed intelligent gate driver to help a capacitor voltage balancing control of MMC converter. The main factor, which causes higher ripple voltage for the proposed solution (2), is passive components (sub-module's capacitors, arm inductors). The optimization method, which considers passive components' dimensioning with novel capacitor voltage balancing control (solution (2)), must be proposed in a future work.

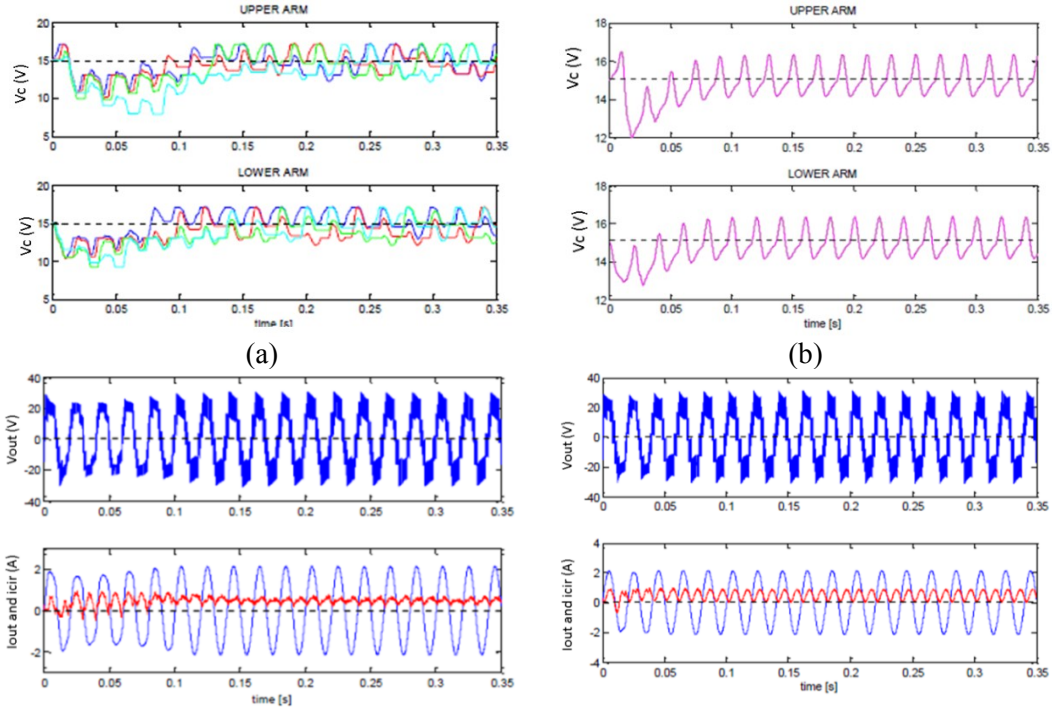

Fig. 2.25.: Simulation results of (provided by a trainee of master degree who was supervised by the author of this manuscript [Yaf]):

(a) Capacitor voltages with a proposed novel control method with only the voltage states (ripple voltage: ΔV = 6V),

(b) Capacitor voltage with classical method (ripple voltage: ΔV = 2V),

(c) Line-to-neutral output voltage V_{LN} (upper waveform), output current i_{out} (blue waveform) and circulating current i_{cir} (red waveform) waveforms with a proposed novel method,

(d) Line-to-neutral output voltage V_{LN} (upper waveform), output current i_{out} (blue waveform) and circulating current i_{cir} (red waveform) waveforms with a classical method.

For further validations, Fig. 2.25c and Fig. 2.25d show line-to-neutral output voltage (V_{out}: upper waveform), output current (i_{out}: blue waveform), and circulating current (i_{cir}: red waveform) for these two methods.

Based on these results, we noticed that the capacitor voltage balancing control of MMC converter can be done with only the voltage states {-1, 0, 1}. These voltage states can be easily obtained within IGBTs gate drivers. Actually, these return informations from secondary side to primary side of gate drivers must respect the insulation constraint. Thus, in the next section, we provide briefly a new concept of intelligent IGBT gate driver.

2.5.2. Insulated transmission function for voltage measurement

As previously presented in Chapter 1, the gate drivers topologies are compared for this kind of application. Fig. 2.26 shows the proposed measurement of sub-module's voltage within the gate driver system. As presented in the previous section, all the transmitter functions of gate driver must provide a high galvanic insulation voltage capability. Hence, the information (from secondary to primary side) must also respect this main constraint.

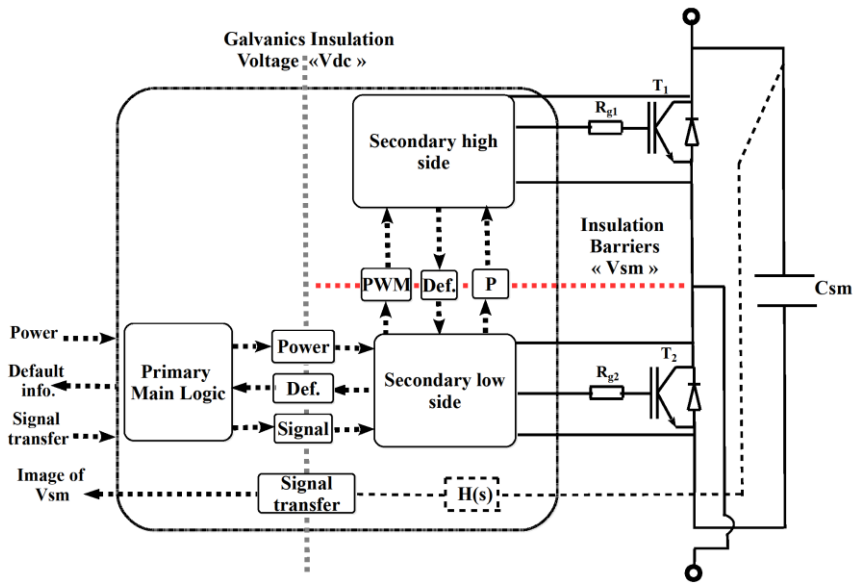

Fig. 2.26.: Proposed voltage measurement for a SM of MMC converter within high insulation gate driver system.

2.6. Conclusion

In this chapter, we detail the design methodology to optimize gate drivers (PWM signal transmission function and power supply function) for IGBT modules for high insulation voltage capabilities. The insulation by planar transformer has been chosen as high insulation system. After the selection of topologies for each function, the optimization methodology is proposed to optimize the transformer geometries and the

associated electronic devices. These optimizations are achieved by the help of a virtual prototyping tool (basically depends on a genetic algorithm (GA) developed in a MATLAB™ script).

To provide numerous choices for various applications, the insulation barrier varies from 0.5mm to 3mm which corresponds to the insulation level up to 50kV with the proposed polysterimide material. Numerous Pareto fronts' results are obtained from the optimization designs for each gate driver function. Then, these results are compared and analyzed until the suitable choice is selected for our final application for MMC converter. Furthermore, the simulation waveforms are provided to support our proposed methodology. These results will be validated experimentally in Chapter 3.

At the end of this chapter, we also introduce the intelligent gate drivers system to replace the voltage sensors in MMC converter. Furthermore, some advices and instructions are given for the adaptation of this gate driver to the MMC internal control structure, especially the averaging and voltage balancing control.

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Chapter 3:

Conception and realization of an optimized sub-module (SM)

3.1. Introduction

As presented in the previous chapter, optimization designs of IGBT gate drivers for high insulation voltage capabilities are presented. In this chapter, a signal and a power transmission functions are experimentally validated.

Section 3.2 presents a power transmission function validation. Brief discussions about the simulation results are provided. Then, the experimental set up of a DC-DC converter, which is used as a power transmission function to the secondary side of IGBT gate drivers, is presented. After that, the experimental results are compared to the simulation results to validate our proposed design methodology.

Section 3.3 validates a signal transmission function. The optimal (pot core and I core) transformers are built and described. Moreover, experimental results are compared to support the transformer choice experimentally. To validate the proposed design methodology, the comparison between the simulation and experimental results for a proposed impulse transmission circuit are provided.

Section 3.4 presents a single channel IGBT gate driver for experimental validations. At this stage, a signal and a power transmission functions are integrated in a prototype on the same PCB.

Section 3.5 describes the 3D (three-dimensional) aspects of one Sub-Module (SM) for Modular Multilevel Converters (MMCs).

Finally, section 3.6 concludes this chapter and provides the perspectives for future works.

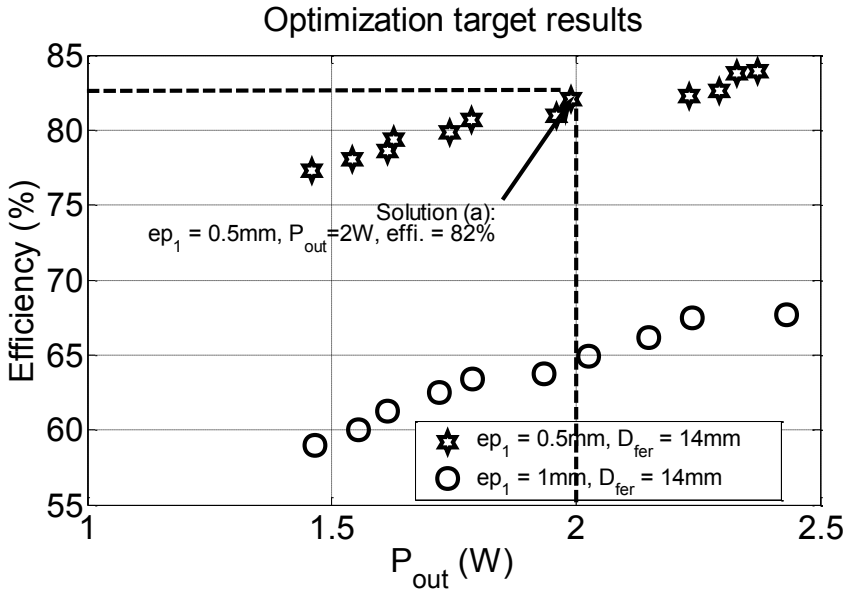


Fig. 3.1: Optimization target results for power transmission

3.2. Power transmission function validations

In this section, the experimental set up for an optimal solution is built. Then, the results are compared to the simulation ones to validate our proposed power supply design and optimization methodology. Moreover, the improved optimization design and its results are also mentioned.

3.2.1. Power transmission function set up

The optimization target results for experimental works for a power supply function are based on a pot core diameter of 14mm and insulation layers of {0.5mm and 1mm}. These Pareto fronts' results are represented in Fig. 3.1. Discussions about these results are provided in the previous chapter, an optimal solution (a) is chosen. The optimal results are represented in Table 3.1.

Table 3.1: Simulation results of the optimal solution (a)

	Solution (a)		
η_{con}	82 %		
ep_1/D_F	0.5 mm/14 mm		
C_{pr} / C_{se}	68 nF/ 68 nF	P_{out}	2 W
f_p	266 kHz	V_{out}/ I_{out}	12.3V/ 0.16A
R_{out}	76.9 Ω	L_{pr} / R_{pr}	17.24 µH/ 0.46Ω
x_1 / x_2	0.25 mm /0.87mm	L_{se} / R_{se}	17.24 µH/ 0.46Ω
n_1 / n_{layer}	2 turns / 4 layers	M / k	10.49 µH / 0.6
ep_2 / ep_6	105 µm / 0.4 mm	C_{ps}	6.67 pF

3.2.1.1. Optimal transformer set up

From the simulation results in Table 3.1, an optimal pot core planar transformer is built. The circular windings are firstly designed by the help of the Kicad™ software. So, the windings on PCB are fabricated and illustrated in Fig. 3.2a. For each PCB, the top windings are connected to the bottom windings by a plated through-hole close to the internal circular hole (see Fig. 3.2a). The thickness of a PCB and the copper are 0.4mm and 105µm respectively. According to the optimization results in Table 3.1, four PCB layers are required to build one side of the transformer. These four layers are connected to each other and inserted into the pot core ferrite. The pot core shapes are presented in Fig. 3.2b. To achieve this, the bottom side of one layer is connected to the top side of the second layer. Then, the bottom side of the second layer is connected to the top side of the third, etc.: Fig. 3.2c details step by step the process. The primary and the secondary sides of the transformer are separated by an air gap of 0.5mm. This length and a polysterimide material define a galvanic insulation of about 20kV (details in Chapter 2). Then, the

experimental electrical characteristics (L_{pr}, R_{pr}, L_{se}, R_{se}, M, k, and C_{ps}) of this transformer are measured with the impedance analyzer Agilent 4294A (see Fig. 3.2d).

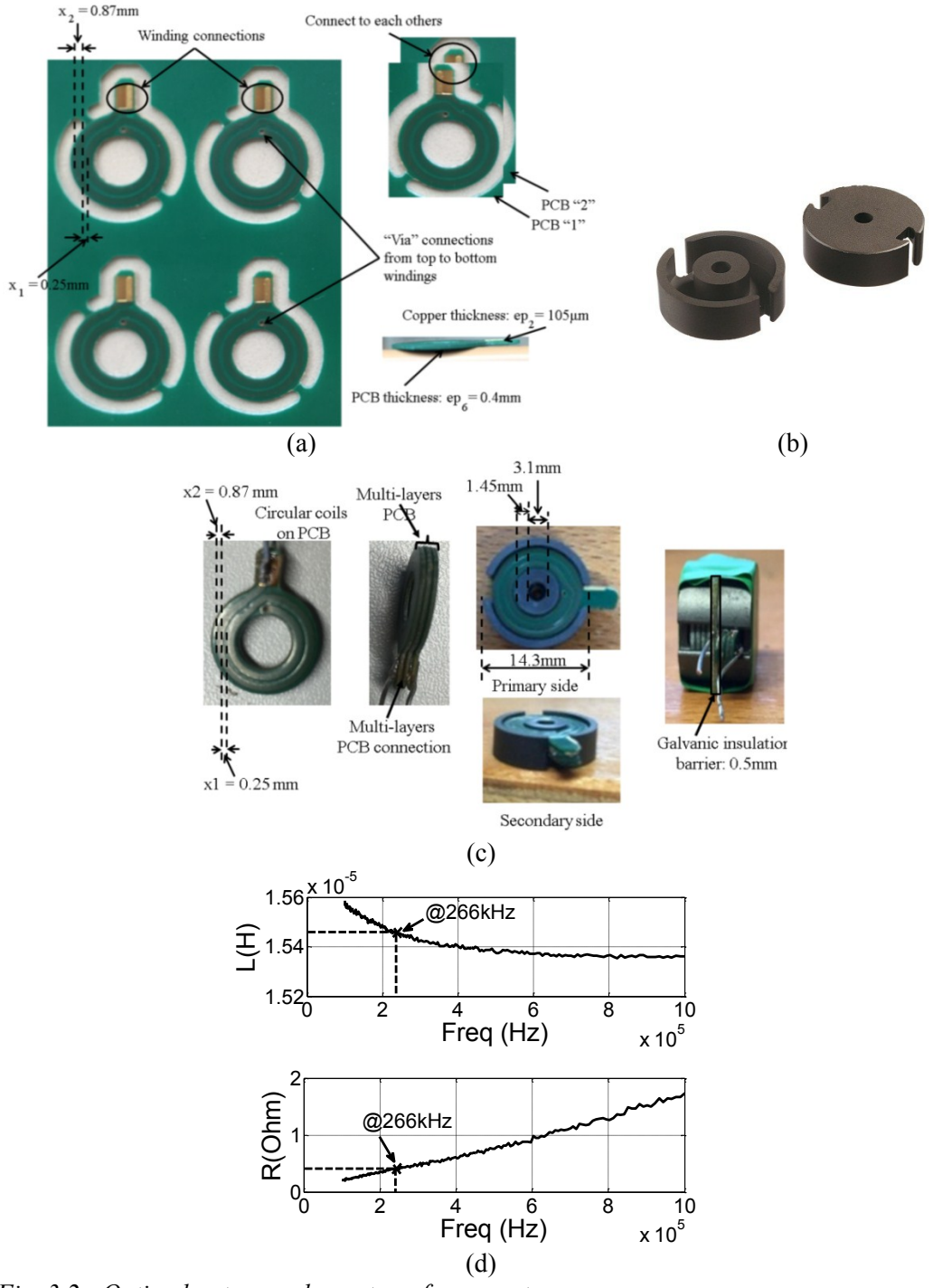


Fig. 3.2.: Optimal pot core planar transformer set up:

(a) Windings on PCB,

(b) Pot core ferrites,

(c) Procedure of fabrication of an optimal pot cot planar transformer,

(d) Experimental results of transformer.

The comparisons between the simulation and the experimental results are given in Table 3.2. According to this table, we notice that the relative error is lower than 15% between the simulation and experimental results.

Table 3.2: Comparison results of an optimized transformer

Para.	Simulated	Measured	Error relative
L_{pr} / R_{pr}	*17.24 µH / 0.46*Ω	*15.44µH / 0.48*Ω	*11.66 %*
L_{se} / R_{se}	*17.24 µH / 0.46*Ω	*15.23 µH / 0.48*Ω	*13.20 %*
M / k	*10.49 µH / 0.6*	*11.83 µH* /0.768	*11.33 %*
C_{ps}	*6.67 pF*	*6.8 pF*	*2 %*

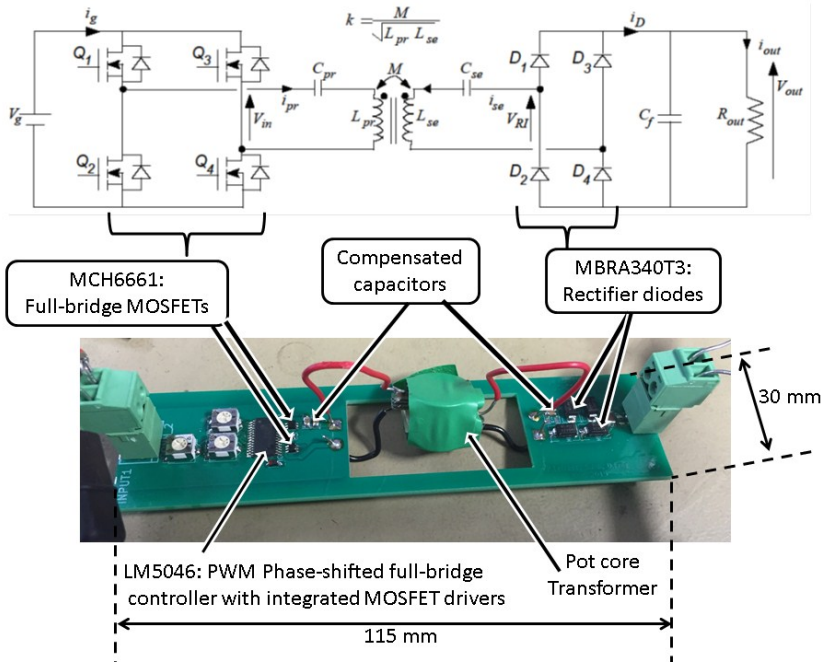
3.2.1.2. DC-DC full-bridge series-series (FBSS) converter testing board

Beside an optimal transformer, other electrical variables' results are presented in Table 3.1.: $C_{pr} = C_{se} = 68$ nF, $R_{out} = 80$ Ω, and $f_p = 266$k Hz.

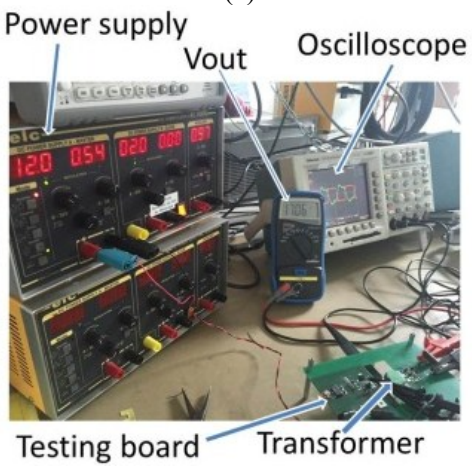
The experimental components are presented in Fig. 3.3 and described as follow:

1) Insulated transformer: one pot core planar transformer (as presented in previous section).
2) Full-bridge controller: a LM5046 PWM phase-shifted full-bridge controller with integrated MOSFET drivers is used to control these four MOSFETs. The switching frequency (f_p) is provided by this component.
3) Full-bridge network: two N-MOSFETs (MCH6661) from ON Semiconductor Company are used. One MCH6661 N-MOSFET is equal to one inverter leg ((Q_1 and Q_2) or (Q_3 and Q_4)).
4) Rectifier network: four Schottky power diodes (MBRA340T3) are used to rectify the output current of resonance tank.
5) Capacitors: CMS capacitors with small packages (0603) are used.

The optimal testing board is illustrated in Fig. 3.3a. Board dimensions are 115mm length and 30mm width. Fig. 3.3b shows all the instruments used for this experimental work.



(a)

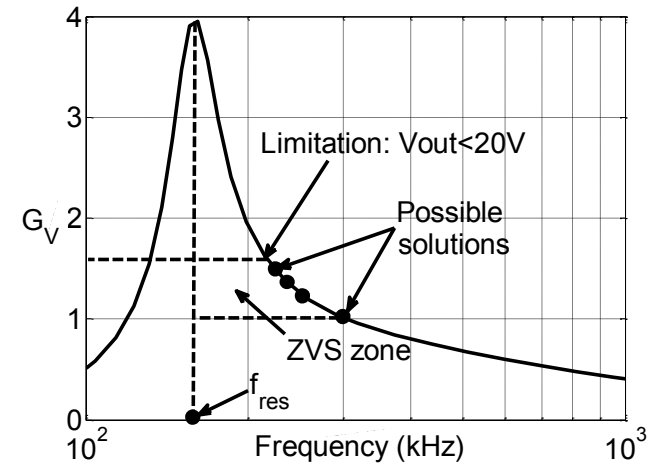


(b)

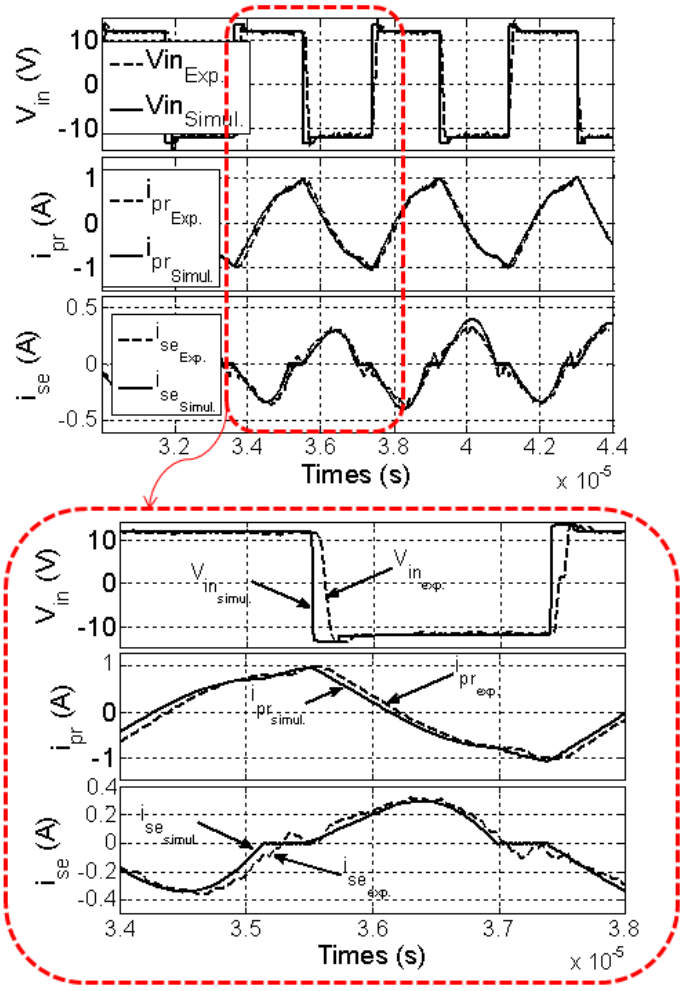
Fig. 3.3: A testing board:
(a) An optimal prototyped board,
(b) Physical prototype instruments.

3.2.2. Comparison results for a power transmission function

According to the voltage transfer ratio G_v that is presented in Fig. 3.4a, the ZVS condition can be achieved from 160 kHz to 350 kHz. To ensure $V_{out} < 20V$, the operating frequency f_p range must be from 200 kHz to 350 kHz. Fig. 3.4b presents the comparison results between the simulation and experimental works for the input voltage resonant tank V_{in}, primary and secondary side currents for the optimal solution (a) (where $f_p = 266kHz$). The top of this figure illustrates these comparison waveforms for some electrical periods. And the lower part shows only one period to see clearly the comparison trends.



(a)



(b)

Fig. 3.4.: Validation results:
(a) Voltage transfer ratio,
(b) Comparison results of V_{in}, i_{pr}, i_{se} for an optimal solution (a).

Influence of the operating frequency: Fig. 3.5a shows the power efficiency (η_{con}) from the simulation and experimental results as a function of the operating frequency. According to this figure, a frequency of 200 kHz provides the highest efficiency which corresponds to the highest converter output voltage and power (see Fig. 3.4a). The differences between the voltage and current waveforms (see Fig. 3.4b) could be explained by the small differences between simulated and measured values of the electrical parameters such as L_{pr}, R_{pr}, L_{se}, R_{se}, M, C_{pr}, and C_{se}. Thus, as a result, the experimental efficiencies are lower than the simulation ones as presented in Fig. 3.5a.

Influence of the output resistor: as discussed in the previous chapter (Chapter 2), at a fixed frequency, when the load varies from 39Ω to 82Ω, efficiency increases from 82% to 88% and output power from 2W to 4W are achieved as plotted in Fig. 3.5b.

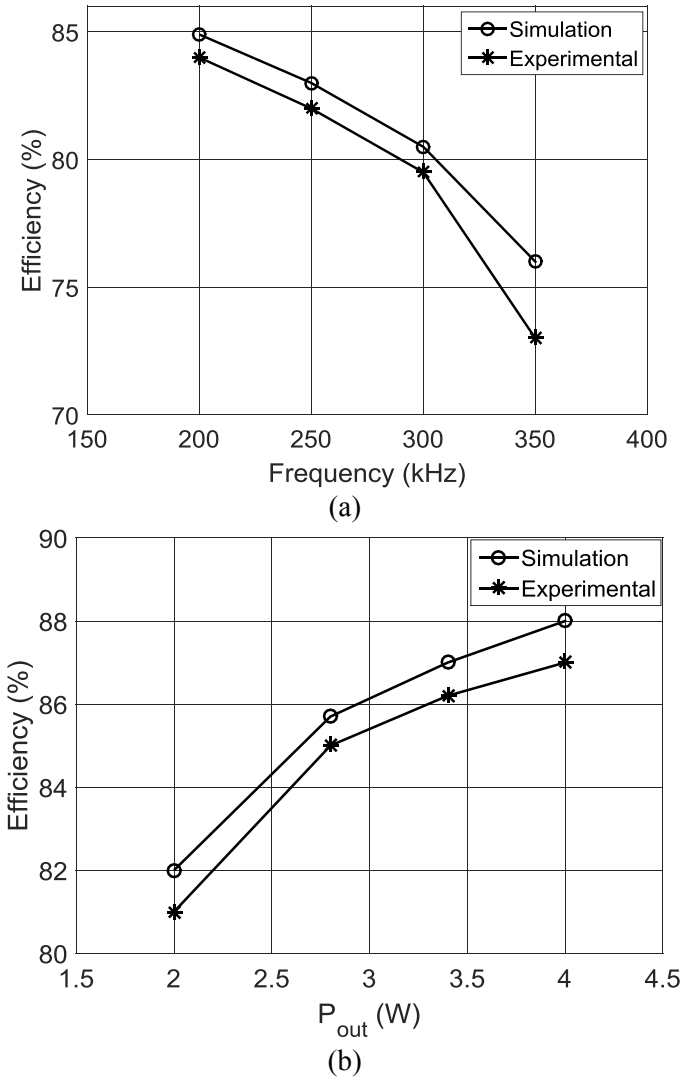


Fig. 3.5.: More validation results for a power transmission function:

(a) Power converter efficiency as a function of the operating frequency,

(b) Power converter efficiency for a fixed frequency of 200kHz as a function of the output power.

Improved optimization design for very high insulation voltage application: so as to reach higher insulation level up to 50kV, the air gap length must be increased to 3.1mm. So, the idea is to use the former transformer (solution (a)) and run a new optimization process considering only C_{pr}, C_{se}, f_p and R_{out} as optimization variables with ep_1 that can vary from 1.5mm to 3.1mm. According to the previous chapter, these insulation thicknesses correspond to insulation voltage level higher than 40 kV if polysterimide material is applied. Hence, the geometric variables $\{x_1, n_1, ep_2, ep_6$ and $n_{layer}\}$ of the transformer do not vary and are considered as fixed parameters. By changing the insulation thickness ep_1, the finite element FEMM^{TM} is still needed to calculate $\{L_{pr}, R_{pr}, L_{se}, R_{se}, M$, and $k\}$. In order to present the effectiveness of our proposed methodology, the optimization design is implemented. To achieve high converter efficiency, the electrical variables $\{C_{pr}, C_{se}, f_p$ and $R_{out}\}$ must be calculated by the optimization GA process as presented in Fig. 3.6. The Pareto fronts' results are the converter efficiency η_{con} versus the converter output power P_{out}.

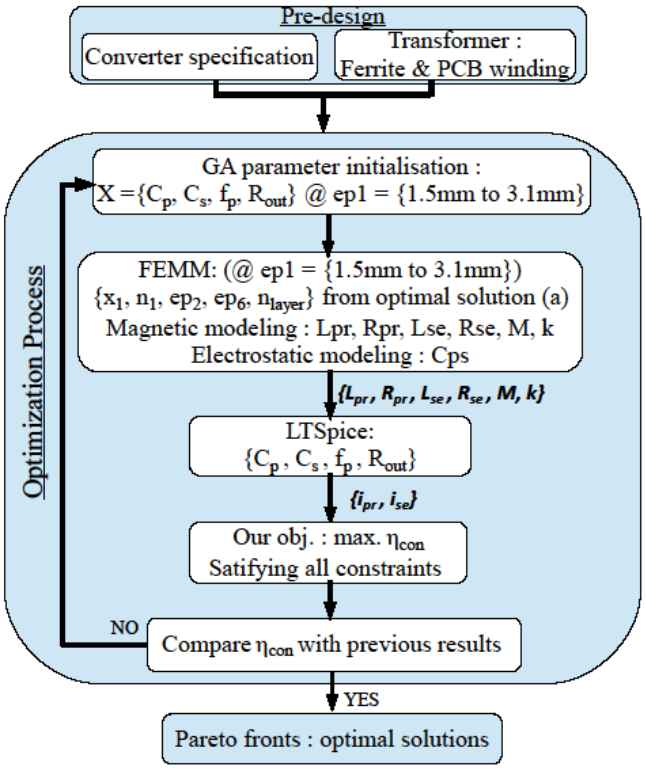


Fig. 3.6.: Improved optimization flowchart.

The parameters of the GA optimization process are: 30 individuals and 100 generations which require 2 hours of computational times (with an Intel Core 2Duo CPU, DELL). Fig. 3.7a illustrates all the improved optimization results of the converter efficiency η_{con} as a function of the converter output power P_{out}. According to these results, for the interesting output power design (P_{out} = 2W), the converter efficiencies vary from 45% (for ep_1 = 3.1mm) to 65% (for ep_1 = 1.5mm). For experimental validations of our improved design, two optimal solutions with ep_1 = 2.5mm and ep_1 = 3.1mm are selected for further works and analyses.

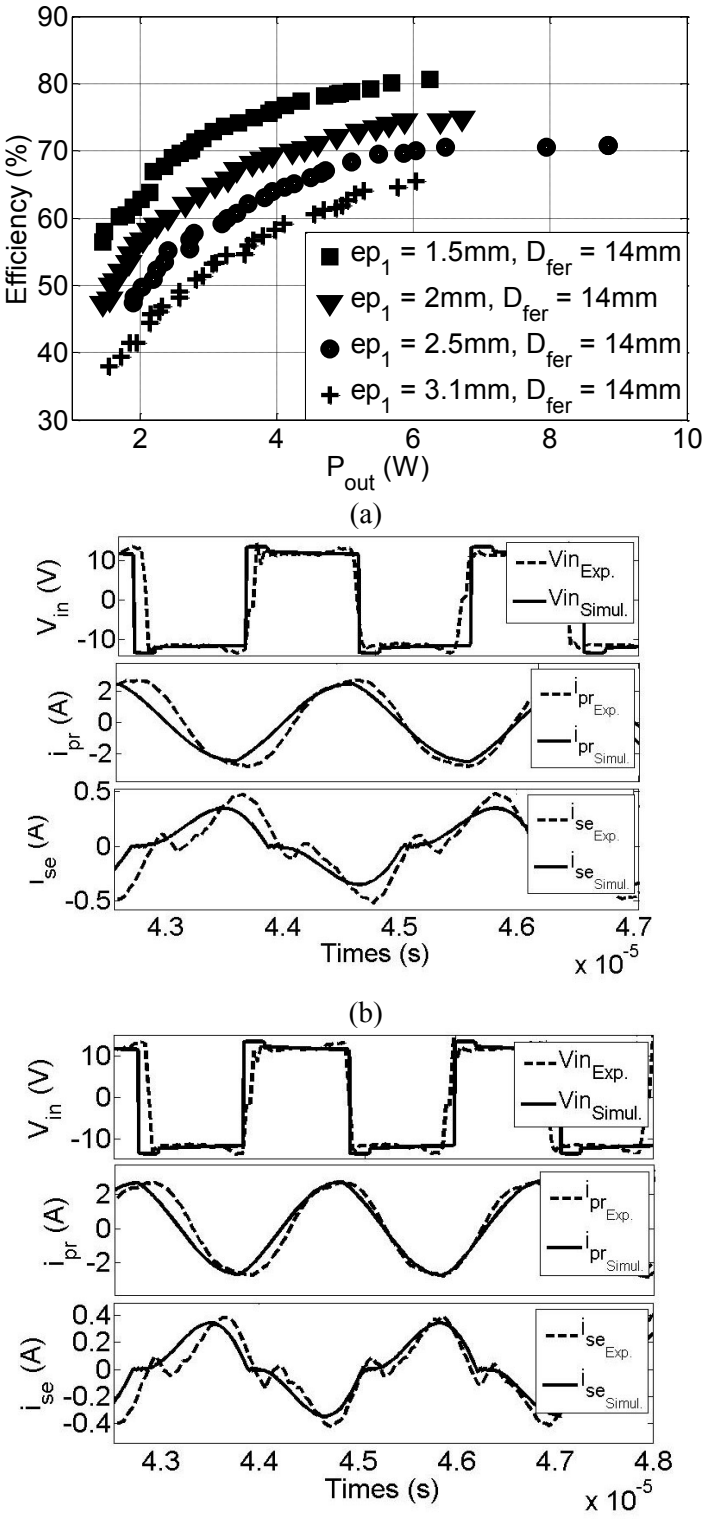


Fig. 3.7.: Improved optimization results:

(a) Pareto fronts of the improved optimization,

(b) Experimental and simulation results from ep_1 = 2.5mm,

(c) Experimental and simulation results from ep_1 = 3mm.

Simulation results are summarized in Table 3.3. For an insulation layer of ep_1 = 2.5mm, an efficiency η_{con} = 50% and η_{con} = 45% for ep_1 = 3.1mm. Beside the converter efficiency and high insulation achievements, a low parasitic capacitor (C_{ps} < 2pF) is another main advantage of these proposed designs. Based on this table, the experimental set-up are made. Fig. 3.7b and Fig. 3.7c present the comparisons results (V_{in}, i_{pr}, i_{se}) between the simulation and experimental works for ep_1 = 2.5mm and ep_1 = 3.1mm, respectively. The differences between the simulation and the experimental results of V_{in}, i_{pr} and i_{se} come from: difference values between simulation and experimental (C_{pr}, C_{se}, R_{out}), parasitic elements of passive components (capacitors, planar transformer). According to these comparison waveforms, the converter power loss of the experimental work is higher than the simulation one. As a result, the experimental efficiencies are lower than the simulation ones. The measured efficiencies are 47% (for ep_1 = 2.5mm) and 43.4% (for ep_1 = 3.1mm). These efficiencies are about 3% lower than the simulation works.

Table 3.3: Simulation results of optimal solution ep_1 = 2.5mm and ep_1 = 3.1mm

	ep_1 = 2.5mm	ep_1 = 3.1mm
η_{con}	50 %	45%
C_{pr} / C_{se}	*19.95 nF/ 19.95 nF*	*15.38 nF/ 15.38 nF*
f_p	*467.74 kHz*	*518.8 kHz*
R_{out}	*75.93 Ω*	*77 Ω*
L_{pr} / L_{se}	*8.247 µH / 8.28 µH*	*8.029 µH / 8.046 µH*
M / k	*2.2.816 µH / 0.3408*	*2.325 µH / 0.289*
C_{ps}	*≈ 2 pF*	*≈ 1.9 pF*

As a conclusion, our proposed resonant converter based on planar transformers for high insulation voltage level capabilities IGBT gate drivers system with optimization design consideration can fulfill our requirements: high insulation voltage level (up to 50kV), high efficiency achievement (43.4% (ep_1 = 3.1mm) to 82% (ep_1 = 0.5mm)) for the required power range, and low parasitic capacitor C_{ps} (less than 2pF).

3.2.3. Conclusion: power transmission function validations

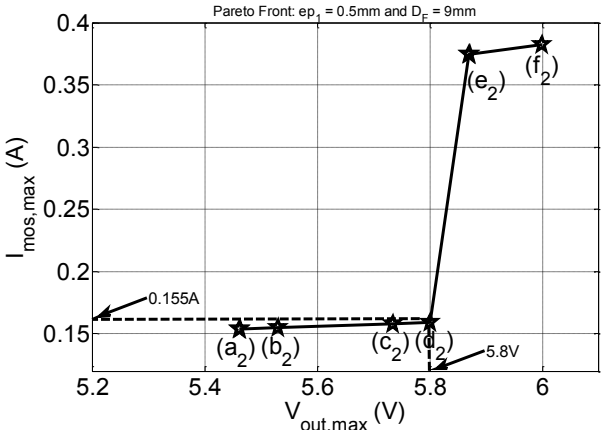
In this section, to deeply prove the efficiency of the proposed methodology to optimize a power transmission topology proposed in Chapter 2, physical designs are presented. An application for IGBT gate driver leads to the choice of a 2W converter. The experimental results are compared to the simulation ones for an air gap of 0.5mm. This leads to the partial conclusion that the proposed methodology is suitable to optimize power transmission function for IGBT for Medium Voltage (MV) applications. Further optimizations with air gap of 2.5mm and 3.1mm are proposed. Insulation voltage level of 40kV to 50kV could be reached with an accurate dielectric material such polysterimide (polymer).

3.3. Signal transmission function validations

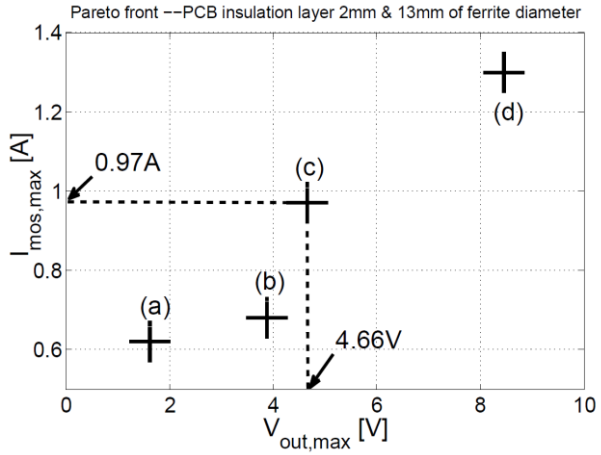
In this section, the experimental results for a signal transmission function with two different geometries (pot core planar and double-layer planar) transformer are presented. The experimental results are compared to the simulation ones to validate the proposed design. Furthermore, the experimental results of pot core technology are also compared to the double-layer planar technology to validate the transformer geometry choice.

3.3.1. Signal transmission function set up

In Chapter 2 and in [Sok16C], the optimization results of a signal transmission function with a pot core planar transformer are presented and illustrated in Fig. 3.8a. Fig. 3.8b presents the optimal result with a double-layer planar transformer [Sok15B]. Optimal solution (d_2) for pot core and optimal solution (c) for double-layer are selected for practical works. The simulation results are illustrated in Table 3.4.



(a)



(b)

Fig. 3.8.: Simulation results for a signal transmission function with two different transformers:

(a) Pot core multi-layer planar transformer,

(b) Double-layer planar transformer.

Table 3.4: Selected optimal solutions for signal transmission with different transformer cores

	Solution (d_2): Multi-layer pot cores	**Solution (c): double-layer I cores**
V_{out} / i_{mos}	5.8V / 0.15A	4.6V / 0.97 A
ep_1/D_F	0.5 mm/9 mm	2mm / 13mm
C_1	108.64 pF	800 pF
C_2	316 pF	525 pF
R_{out}	30 kΩ	20 kΩ
x_1	0.32 mm	0.47 mm
x_2	0.54 mm	0.51 mm
x_3	x_1	0.27 mm
x_4	x_2	0.95 mm
n_1	2 turns	5 turns
n_2	n_1	5 turns
n_{layer}	2 layers	--

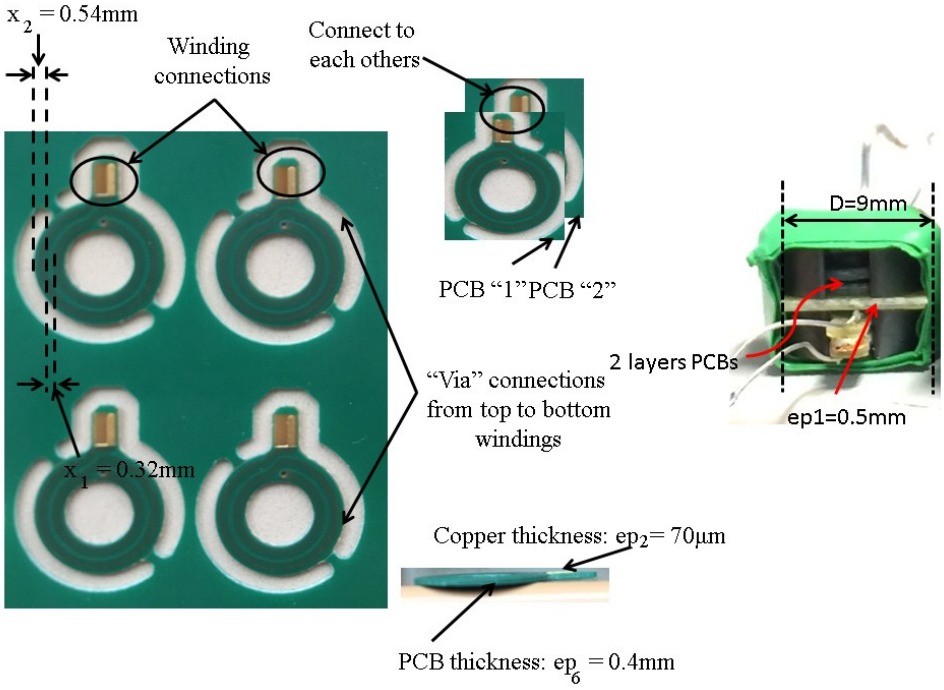
3.3.1.1. Optimal transformer set up

From geometric results of Table 3.4, a pot core transformer and a double-layer planar transformer are built as presented in Fig. 3.9a and Fig. 3.9b, respectively. The characteristics of an optimal pot core transformer are: 2 PCB windings layers per side, copper thickness of ep_2 = 70µm, PCB thickness' layer ep_6 = 0.4mm. For an optimal double-layer planar transformer are: copper thickness of ep_2 = 35µm and PCB thickness' layer ep_6 = 1.6mm.

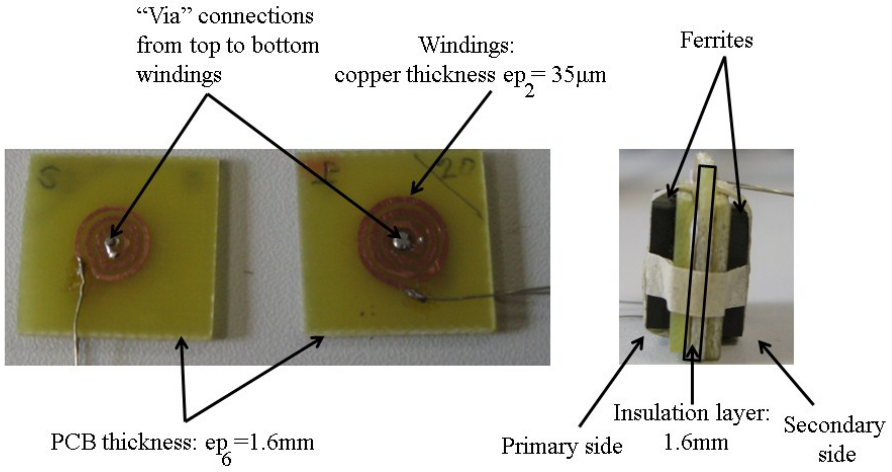
To validate the transformer modeling, these two transformers are measured with the impedance analyzer 4294A. The comparisons between the simulation and experimental results (L_{pr}, R_{pr}, L_{se}, R_{se}, M, k and C_{ps}) are presented in Table 3.5. According to this table, the relative errors are lower than 15% between the simulation and experimental results.

Table 3.5: The comparisons between the simulation and experimental results for optimal transformer

	Solution (d_2): Multi-layer pot cores			**Solution (c): double-layer I cores**		
	Simulated	Measured	Error	Simulated	Measured	Error
L_{pr} / R_{pr}	2.03µH/0.26Ω	2.27µH/0.28Ω	10.5%	180 nH/0.52Ω	190 nH/0.60Ω	5.26%
L_{se} / R_{se}	2.03µH/0.26Ω	2.27µH/0.28Ω	10.5%	192 nH/0.83Ω	198 nH/0.90Ω	3.03%
M / k	1.57µH/0.776	1.47µH/0.65	6.37%	55 nH/0.296	54 nH/0.278	1.82%
C_{ps}	2 pF	2.3 pF	13%	--	--	--



(a)



(b)

Fig. 3.9.: Procedure of optimal transformer fabrications for two different ferrite cores:
(a) Pot core multi-layer planar transformer,
(b) Double-layer planar transformer.

3.3.1.2. Signal transmission function testing board

Beside a transformer and its optimal associated components (C_1, C_2, R_{out}) for an impulse circuit, other components required for a signal transmission function testing board are:

1) Primary side logic gate to control N-MOSFET at the primary side of an impulse circuit: MOSFET gate drivers, voltage regulator.

2) Secondary side:
   a) Schmitt trigger (74HC14): the supply voltage for this logic component is 5V because the maximum voltage supply for this high-speed trigger is 7V. Thus, as presented in Fig. 3.10, the output voltage of an impulse circuit is used to supply this component.
   b) T flip-flop (type 'D' 74HC74): this device is used to convert impulse information into state information.
   c) Level-shifter (FAN-3111E): to feed an IGBT gate, the low-voltage and high-impedance output of T flip-flop are feeding a level-shifter (FAN-3111E) to transform the (0, +5V) into (0, +15V) voltage information. Then, fast bipolar transistors (FZT849-FZT949) are used in a H-bridge push-pull topology to directly feed the IGBT gate-emitter voltage V_{ge}.

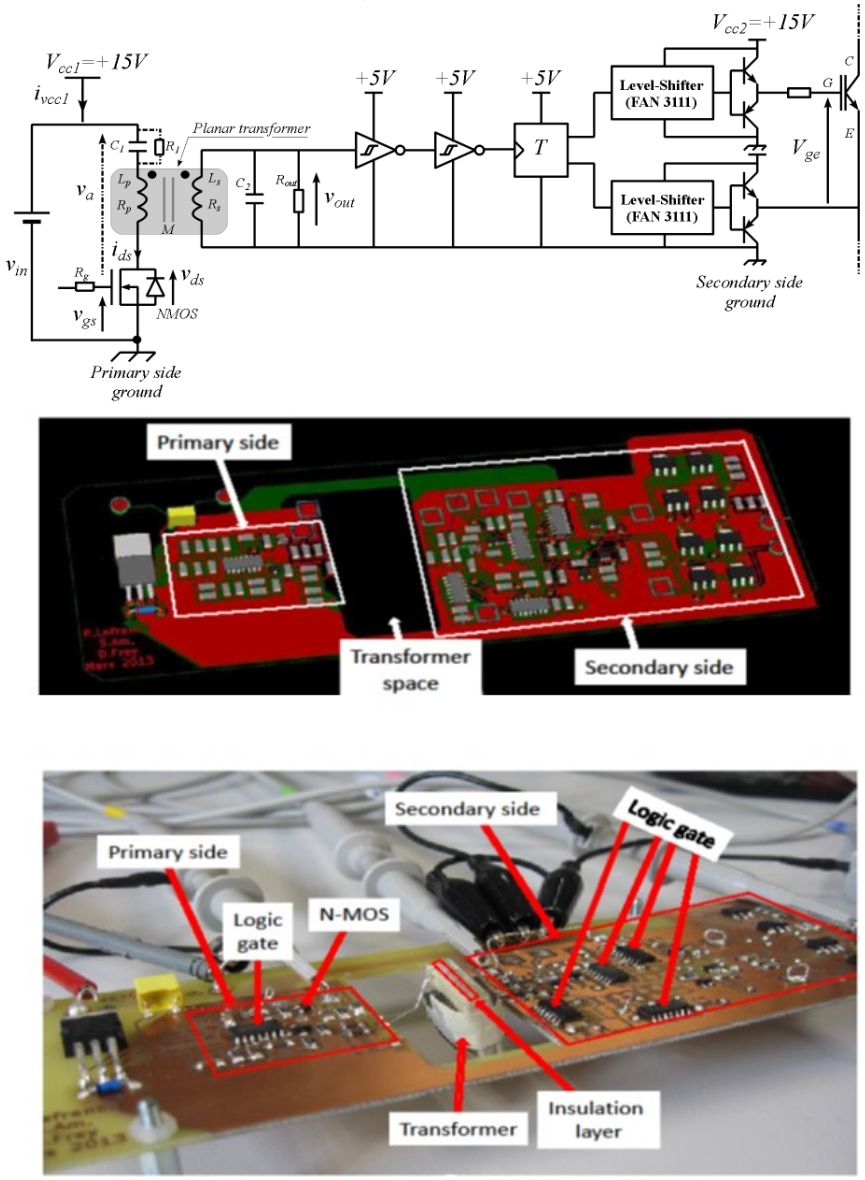


Fig. 3.10.: Testing board for a signal transmission function of IGBT gate drivers.

3.3.2. Comparison results for signal transmission function

As presented in the previous section, the output voltages of an impulse circuit for two optimal transformers are in the range of 4V to 7V. One main objective to consider between these two transformers is a primary side current i_{mos} to calculate the power consumption within the system. Fig. 3.11a and Fig. 3.11b present waveforms of i_{mos} with a pot core planar transformer and a double-layer planar transformer, respectively. According to these figures, a circuit with a pot core technology consumes an average power seven times less than a double-layer one. Their rise times are in the same range (t_{rise} = 18ns). Fig. 3.11c and Fig. 3.11d illustrate the experimental results (V_{out}, V_{ds}, V_{ge}) for a pot core and a double-layer technologies, respectively. The gate-emitter voltage (V_{ge}) is equal to +15V and -15V. The propagation delays between V_{ds} (primary side) to V_{ge} (secondary side) for these two transformers are about 70ns. From these results, a pot core multi-layers transformer is a dominant solution. Hence, in the following, the comparison between the simulation and experimental results are focused on a pot core ferrite technology.

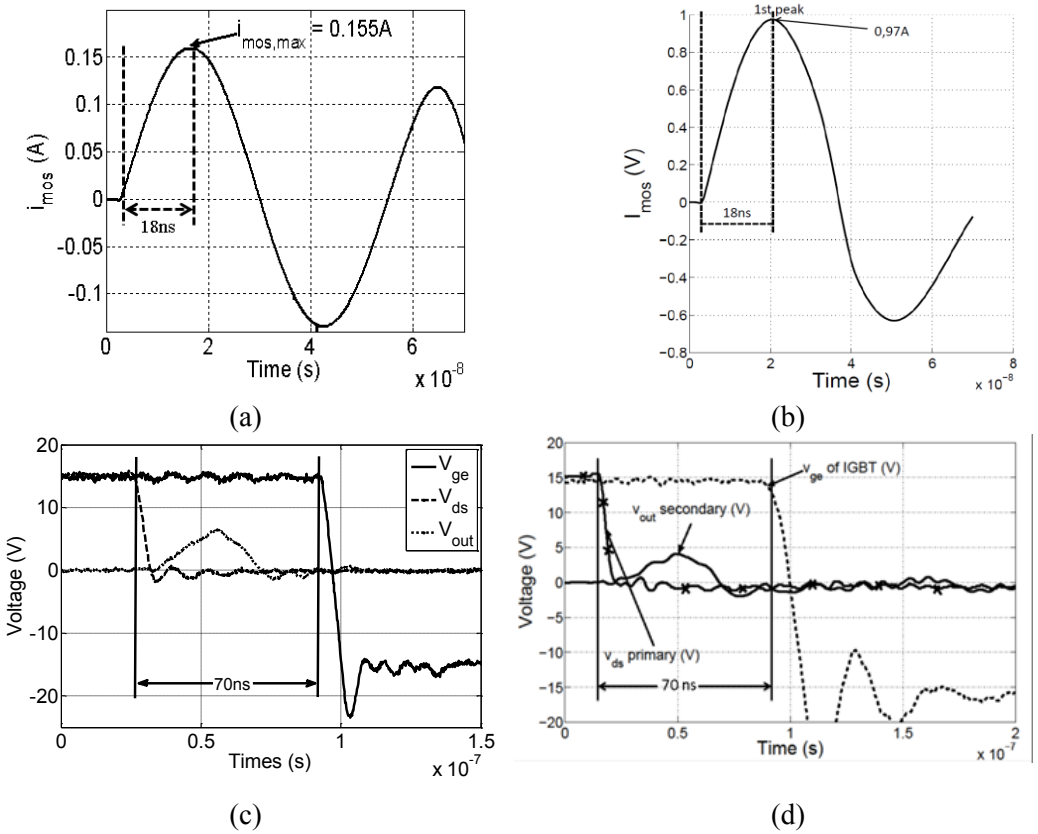


Fig. 3.11.: Optimal results:

(a) Primary side current i_{mos} waveform for pot core planar transformer technology,

(b) Primary side current i_{mos} waveform for double-layer planar transformer technology,

(c) Experimental results of the output voltage (V_{out}),N-MOSFET drain-source current (V_{ds}), IGBT gate-emitter voltage (V_{ge}) for a pot core multi-layer technology,

(d) Experimental results of the output voltage (V_{out}), N-MOSFET drain-source current (V_{ds}), IGBT gate-emitter voltage (V_{ge}) for a double-layer technology.

To compare the simulation results to the experimental ones, the output voltage V_{out} of the transformer is the most important variable to be considered. As illustrated in Fig. 3.12a, $V_{out,max}$ is about 5.8V for simulation result and about 5V for experimental one. And the rise time to the peak value is around 18ns. The difference clearly comes from the switching speed of the drain-source voltage V_{ds}, the gate-source voltage V_{gs} of N-MOSFET at a primary side (as presented in Fig. 3.12b and Fig. 3.12c), the parasitic elements of passive components, and circuit layout.

So as to improve the accuracy of the modeling, an investigation is done towards the excitation voltage of the N-MOSFET on the emitter side. As shown in Fig. 3.12c, the V_{gs} voltage has a huge difference between simulation and experimental results. Therefore the V_{gs} waveform taken from the experimental setup is recorded and sent into the simulation software. Then, Fig. 3.12d presents the comparison of V_{out} voltage with V_{gs} waveform taken from the experimental set up. We can notice that the accuracy of the modeling is further improved.

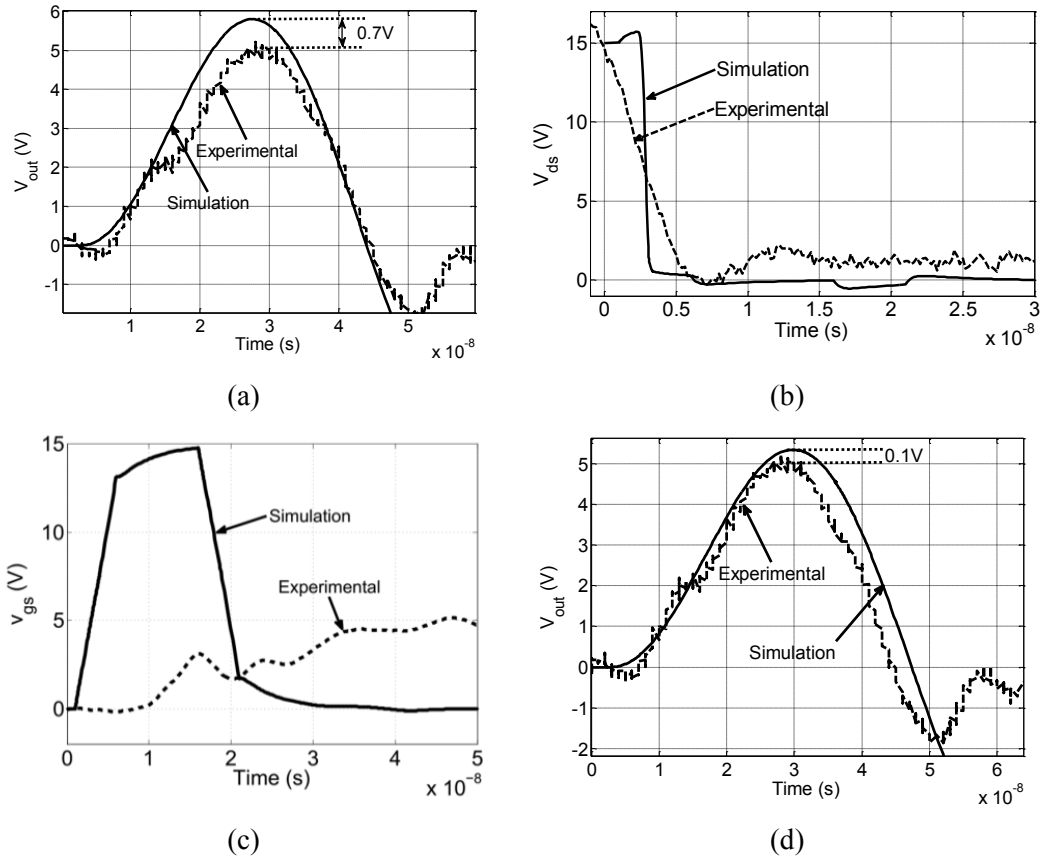


Fig. 3.12.: Validation results for the signal transmission function:
(a) V_{out} waveform comparison between the simulation and experiment results,
(b) V_{ds} waveform comparison between the simulation and experimental results,
(c) V_{gs} waveform comparison between the simulation and experimental results,
(d) V_{out} waveform comparison for an improved modeling (by injecting V_{gs_exp}. into the simulation work)

Moreover, for further validation, the comparison of i_{mos} waveform between the simulation and experimental results are shown in Fig. 3.13a. Then, the V_{ge} voltage of the IGBT module is equal to -15V or +15V as presented in Fig. 3.13b. As depicted in Fig. 3.13c, the waveforms (for the rise time and the fall time) are presented. The gate current i_g is also provided to show that the gate driver can feed few amperes to the gate for turn-on and turn-off.

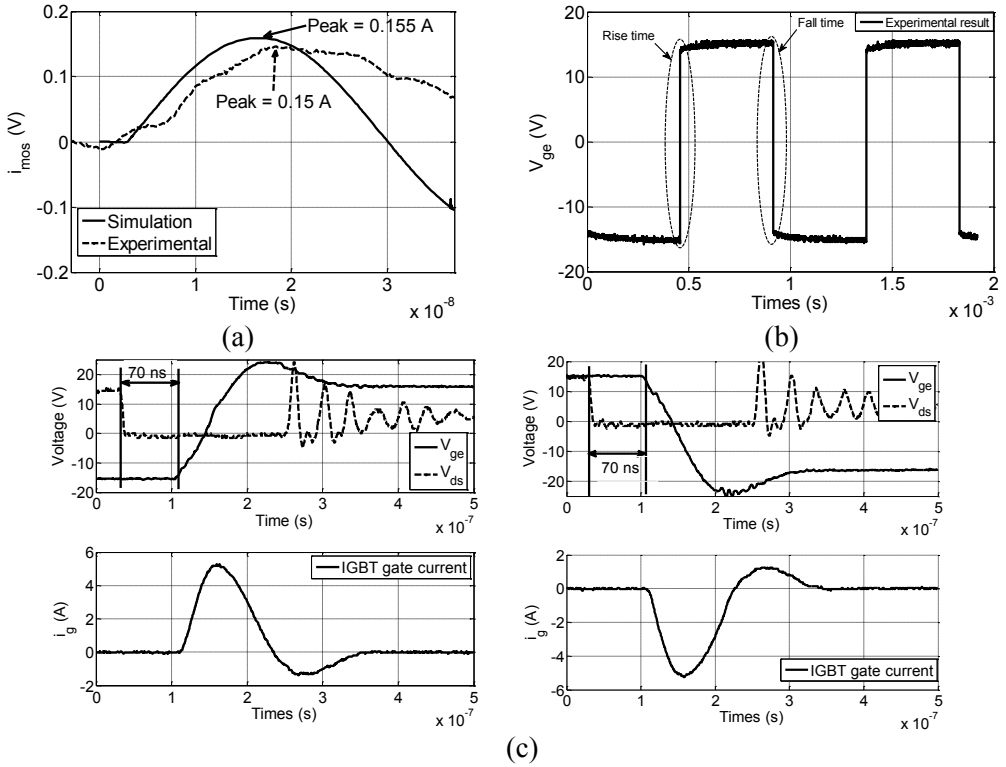


Fig. 3.13.: Validation results for signal transmission function:
(a) i_{mos} waveform comparison between the simulation and experimental results,
(b) Experimental result of $V_{ge}(t)$ = +/-15V for few electric periods,
(c) Experimental results (V_{ds}, V_{ge}, i_g) for the rise side and fall side of $V_{ge}(t)$.

3.3.3. Conclusion: signal transmission function validations

The design and optimization methodology of a signal transmission function for high insulation capability is validated experimentally in this section. Two physical transformers (pot core planar and double-layer planar) and testing instruments are also presented. The experimental results are extracted. Then, the simulation and experimental results are compared to validate our proposed design methodology.

The choice of a pot core planar transformer is also validated experimentally by comparing its experimental results to a double-layer technology transformer. The maximum primary side current waveforms and propagation delay are the main factors for the comparison of these transformer technologies. As a result, a pot core technology is the best solution in term of low average power consumption. Furthermore; the output voltage waveform $V_{out,max}$, the primary side current $i_{mos,max}$, and a drain-source voltage of N-

MOSFET V_{ds} are compared between the simulation and experimental works to validate our proposed signal transmission function methodology. Then, a gate-emitter voltage V_{ge} = +/- 15V are measured experimentally with a gate current i_g of a few amperes.

3.4. A single channel IGBT gate driver validation

This section validates the separated optimal designs in previous sections in a new testing board (combine a signal and power transmission functions). At this stage, the insulation thickness ep_1 is equal to 0.5mm. Then, the experimental results for ep_1 = 1mm are also provided to respond to a very high insulation voltage capability application. Thus, Table 3.6 summarizes the constraints for a single channel IGBT gate driver.

Table 3.6: Constraints for a single channel IGBT gate driver

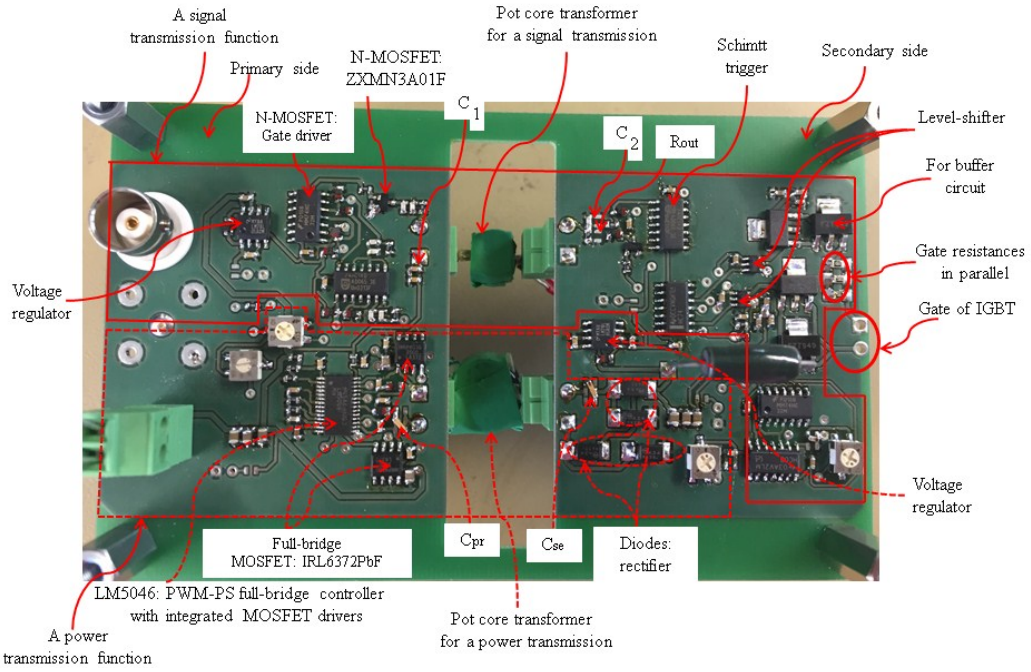
Power transmission function	Signal transmission function
• $P_{out} \leq 2W$ • $V_{in,power} = 15V$ • $V_{out,power} = 15V$ • ep_1 = {0.5mm, 1mm} • Insulation voltage (V_{insu}) > 20kV	• Low average power consumption • $V_{in,signal} = 15V$ • $V_{out,signal}$ = [3V – 7V] • ep_1 = {0.5mm, 1mm} • Insulation voltage (V_{insu}) > 20kV

3.4.1. Experimental testing board descriptions

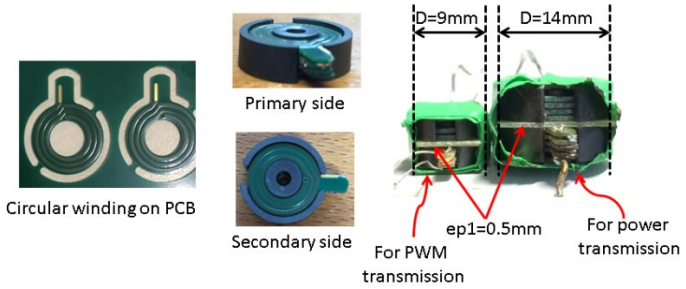
A single channel IGBT gate driver testing board: to design a new single channel IGBT gate driver testing board, numerous components are needed as presented in Fig. 3.14a. These devices are described as follow:

- An impulse circuit for a signal transmission function:
  - One N-MOSFET at primary side: ZXMN3A01F,
  - One gate driver for this N-MOSFET: 74LS32,
  - Two voltage regulators (V_{in} = 15V and V_{out} = 5V): LM78L05ACM,
  - Capacitors C_1 and C_2: CMS components,
  - Load resistance R_{out},
  - Logic devices: Schmitt triggers, level-shifters, buffer circuit,
  - Gate resistances in parallel,
  - One pot core planar transformer: diameter of 9mm.

- A power transmission function:
  - Two full-bridge MOSFETs (IRL6372PbF),
  - One PWM-PS full-bridge controller with integrated MOSFET drivers (LM5046),
  - Capacitors C_{pr} and C_{se},
  - Four diodes for rectifier,
  - Load resistance R_{out},
  - One pot core planar transformer: diameter of 14mm.



(a)



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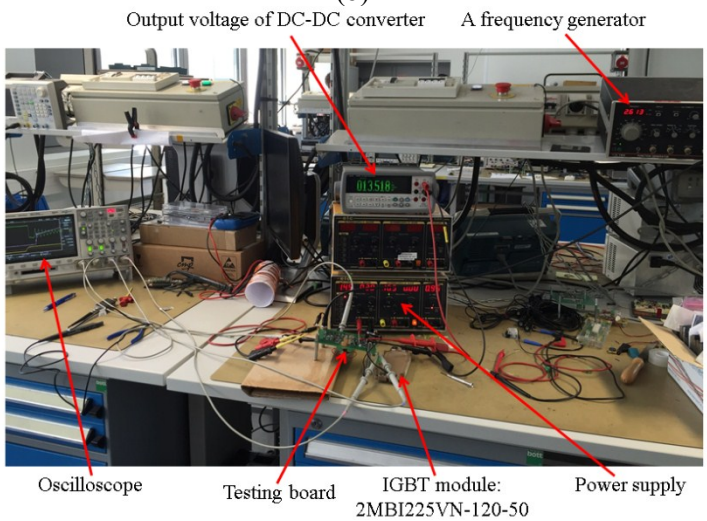


(c)

Fig. 3.14.: Testing board descriptions:
(a) A testing board with a signal transmission and a power transmission function,
(b) Optimal transformer set up,
(c) Experimental instruments.

Two pot core planar transformers: Fig. 3.14b presents the experimental set up of these two transformers. As presented in this figure, pot core diameters of 9mm and 14mm are built for a signal transmission and a power transmission, respectively. These transformers are measured with the Agilent 4294A precision impedance analyzer and compared to the simulation results. Fig. 3.14c illustrates the experimental instruments to perform the experimental works. A testing board IGBT gate driver is used to drive an IGBT module (2MBI225VN-120-50, inverter leg 1200V-225A).

3.4.2. A single channel IGBT gate driver validations for ep_1 = 0.5mm

According to Table 3.2 in Section 3.2.1.1, the comparison between the experimental and the simulation results for a pot core transformer with insulation thickness of 0.5mm is shown. Then, based on the optimization results for a power transmission and a signal transmission functions from a previous section, the experimental works to validate these gate driver functions in one testing board can be done.

Power supply results: two capacitors (C_{pr} and C_{se}) of 68nF and a load resistance of 80Ω are installed in a testing board. Then, the main factors for comparisons are the primary side and the secondary side currents of a DC-DC full-bridge series-series converter (see Fig. 3.15). According to this figure, we notice that the currents' waveforms are similar. And the output voltage of this DC-DC converter $V_{out,power}$ is equal to 15V. These results clearly validate the proposed power transmission function for a single channel IGBT gate driver.

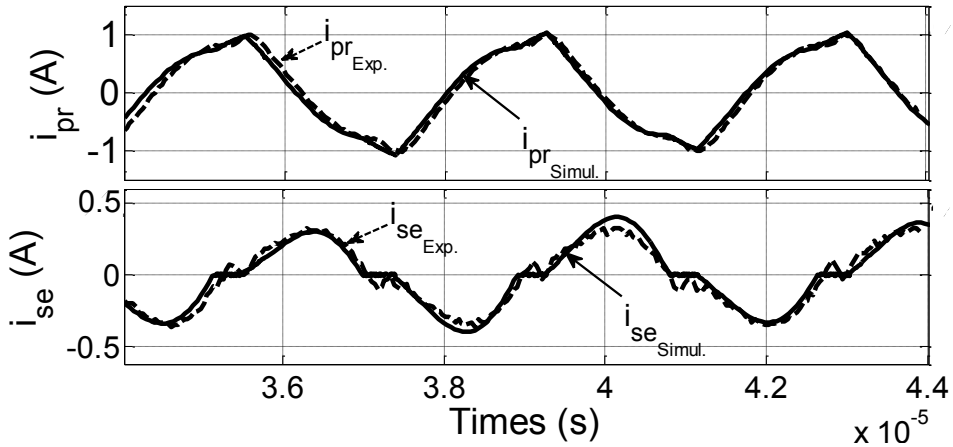


Fig. 3.15. Validation results for a power transmission function (ep_1 = 0.5mm): the comparison of i_{pr} and i_{se} between the simulation and the experimental results,

Signal transmission results: Fig. 3.16 shows that the output voltage ($V_{cc2} \approx 15V$) of a DC-DC power supply converter is used to supply the secondary side of a signal transmission function. According to this figure, level-shifters and buffer's circuit components require a supply voltage of around 15V. Some logic components such as Schmitt trigger, flip-flops in the signal transmission function are feed by the output voltage ($V_{out} \approx 5V$) of the impulse circuit.

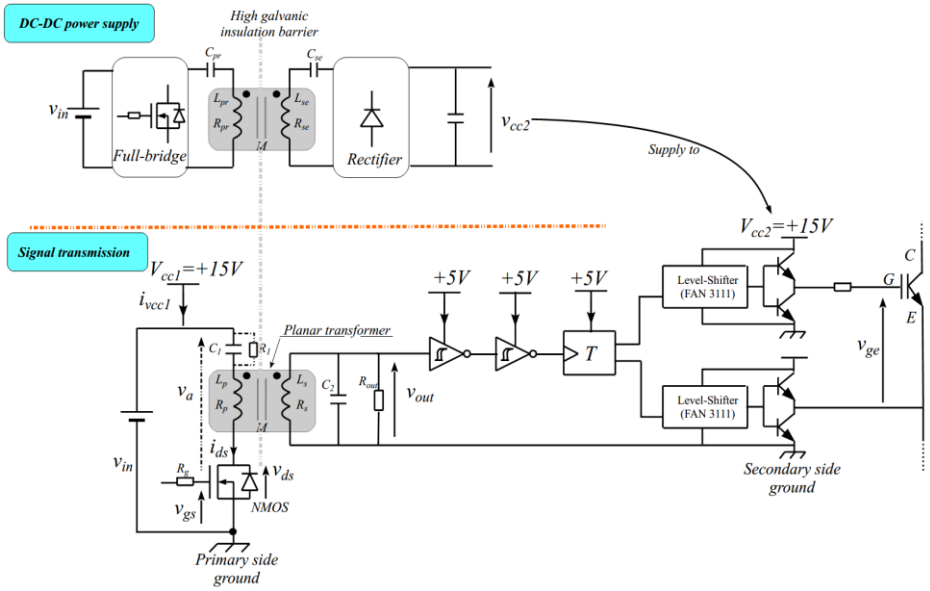
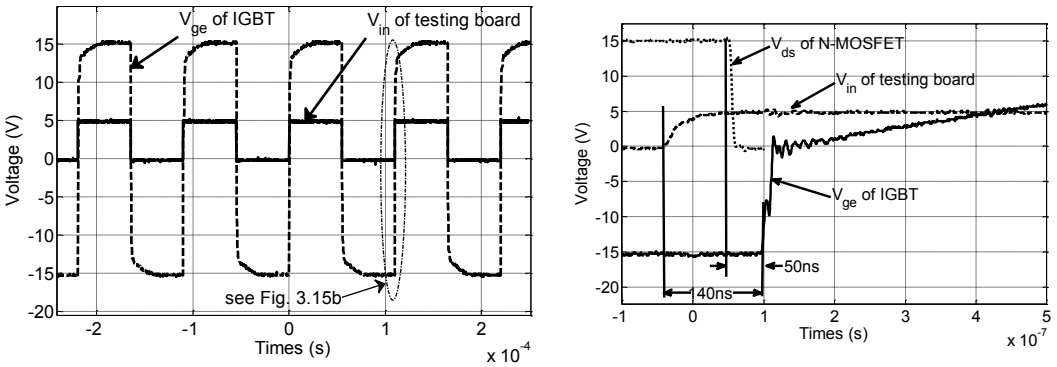


Fig. 3.16.: Implementation of a power transmission and a signal transmission functions for a single channel IGBT gate driver.

Fig. 3.17a illustrates some electrical periods of the gate-emitter voltage (V_{ge}) of the IGBT and the input voltage of the testing board V_{in}. Then, Fig. 3.17b demonstrates the drain-source voltage (V_{ds}) of the N-MOSFET in the primary side, the gate-emitter voltage (V_{ge}) of the IGBT module, and the input voltage of the testing board (V_{in}). According to this figure, we notice that the propagation delay is around 140ns between V_{in} and V_{ge} of the IGBT module. The propagation delay between V_{ds} and the V_{ge} is around 70ns.



(a) (b)

Fig. 3.17.: Validation results for a signal transmission function (ep_1 = 0.5mm):
(a) The experimental results of V_{ge} = +/- 15V for a few electrical period,
(b) The experimental results of V_{ds} of N-MOSFET, V_{in} of a testing board, V_{ge} of IGBT.

To strongly validate our proposed design methodology and to answer a very high insulation voltage requirements of a single IGBT gate driver, we provide comparison results for an insulation layer ep_1 = 1mm (which can achieve at least 30kV of insulation voltage level if a dielectric polysterimide is used).

3.4.3. A single channel IGBT gate driver validation for ep_1 = 1mm

The same testing board is used to perform the practical works. The insulation layer of the two transformers (ep_1) is 1mm. First, the optimal Pareto fronts for a power transmission and a signal transmission function for ep_1 = 1mm are presented. Then, two pot core planar transformers are built and measured with the Agilent 4294A precision impedance analyzer.

Power transmission results for ep_1 = 1mm: Fig. 3.18 illustrates an optimal Pareto front between the converter efficiency (η_{con}) and the converter output power (P_{out}). According to this figure, we select a solution (a_a) to build an experimental work because its geometrical results are the same as solution (d_2) of ep_1 = 0.5mm. The optimization results are presented in Table 3.7. As presented in this table, two capacitors $C_1 = C_2$ = 66 nF and a resistive load of $R_{out,power}$ = 68 Ω are needed. In order to operate in ZVS condition and to achieve high efficiency, the converter must operate at 362 kHz. The input voltage V_{in} is equal to 15V. These combinations provide the output voltage V_{out} = 13.5V, the converter efficiency η_{con} = 57 %, and the converter output power P_{out} = 1.5W.

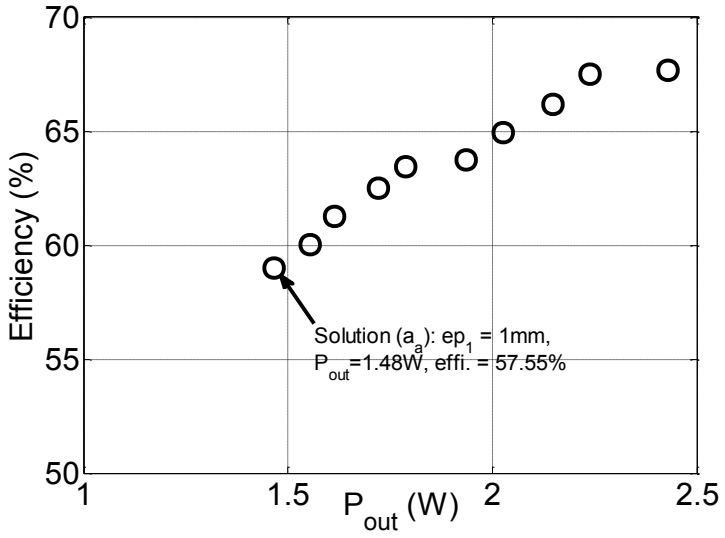


Fig. 3.18.: A Pareto front for a power transmission function for ep_1 = 1mm.

Table 3.7: Optimization results for solution (a_a)

Variable	Values
ep_1 / D_F	1mm / 14mm
η_{con} / P_{out}	57 % / 1.5 W
$C_1 = C_2$	66 nF
$R_{out,power}$	68 Ω
f_p	362 kHz
V_{in}	15V
V_{out}	13.5V

First, a pot core transformer is built and compared to the simulation one (see Table 3.8). According to this table, we notice that the relative error between the simulation work and the experimental work is lower than 15%.

Table 3.8: Comparison between the simulation and experimental results of optimal transformer for solution (a_a)

Variable	Experimental	Simulation	Error relative
L_{pr}	10.44 µH	11.2 µH	6.78 %
L_{se}	10.26 µH	11.2 µH	8.39 %
M	6.164 µH	6.6 µH	6.66 %
K	0.5954	0.6409	7 %
R_{pr}	0.92 Ω	0.97 Ω	5.15 %
R_{se}	0.988 Ω	0.97 Ω	1.82 %

Fig. 3.19 shows the comparison results of an input voltage (V_{in}), a primary side current (i_{pr}) and a secondary side current (i_{se}). According to this figure, we notice that the input voltage of the resonant tank V_{in} between the simulation and experimental results are exactly the same waveform. The experimental input currents (i_{pr} and i_{se}) are not fitting exactly to simulation ones. These problems basically come from parasitic components of capacitors and the planar transformer parameters as shown in Table 3.8.

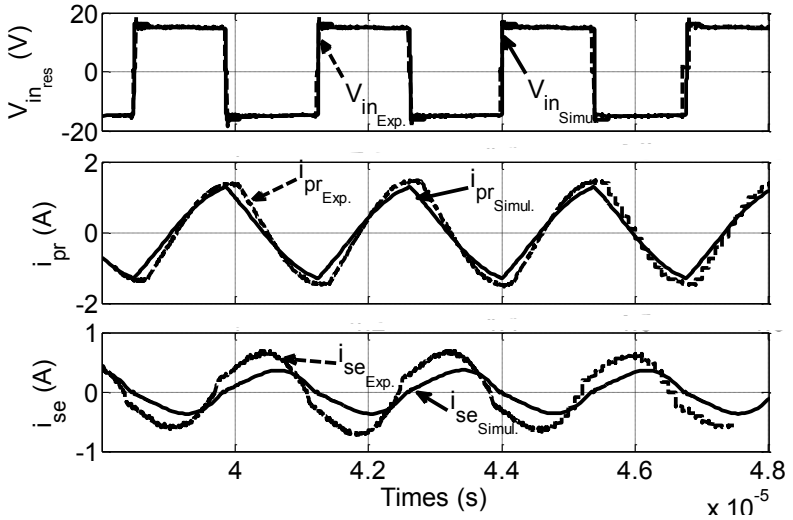


Fig. 3.19.: Validation results for a power transmission function (ep_1 = 1mm): the comparison of $V_{in,power}$, i_{pr} and i_{se} between the simulation and the experimental results

Signal transmission function for 1mm: Fig. 3.20 illustrates the optimal Pareto front of a signal transmission function for an insulation of ep_1 = 1mm and a ferrite diameter of 9mm. We have nine optimal solutions. To perform the experimental works, we select a solution (x) (see Fig. 3.20). The numerical solutions are presented in Table 3.9. The maximum output voltage $V_{out,max}$ and the maximum input current $i_{mos,max}$ values are around 5V and 0.155 A, respectively. The value of a primary side capacitor is equal to

100pF. The secondary side capacitor is equal to 150pF. The resistive load of this impulse circuit is equal to 30 kΩ.

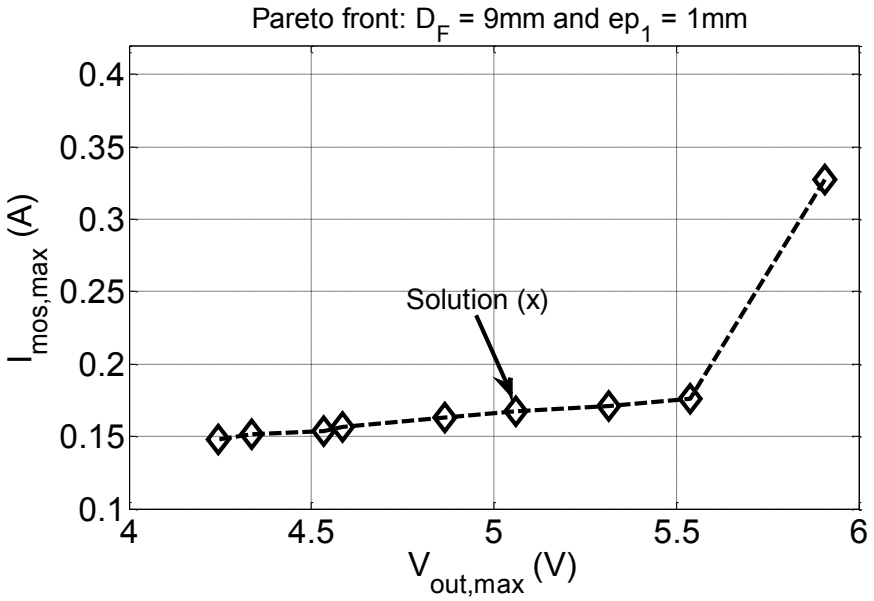


Fig. 3.20.: Pareto front for a signal transmission function with ep_1 = 1mm.

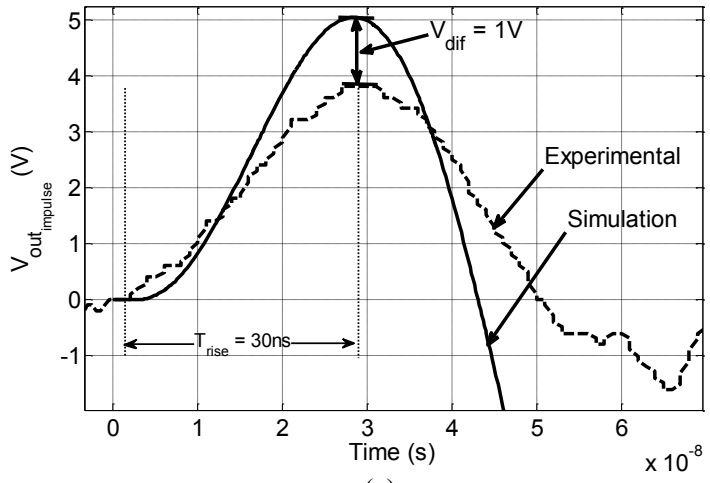
Table 3.9: Simulation for optimal solution (X)

Variable	Values
$V_{out,max}$	5 V
$i_{mos,max}$	0.155 A
C_1	100pF
C_2	150pF
R_{out}	30kOhm
$f_{sw,IGBT}$	2.62kHz

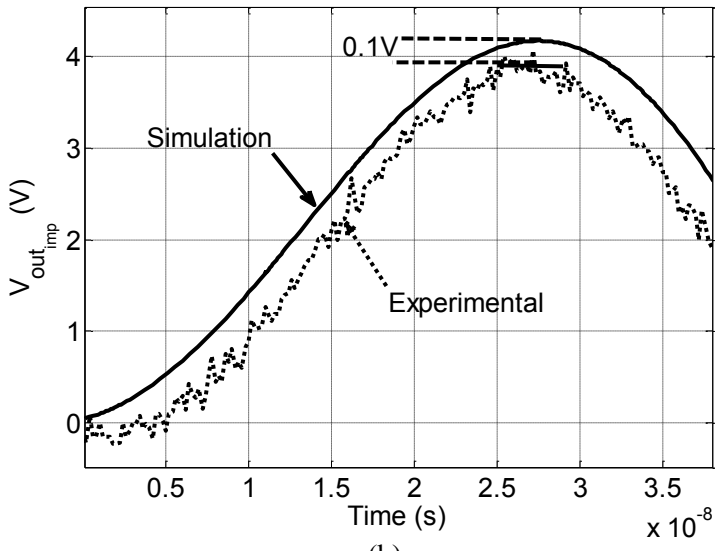
First, a pot core transformer is built and compared to the simulation one (see Table 3.10). According to this table, we notice that the relative error between the simulation work and the experimental work is fewer than 15% for the inductance values. Fig. 3.21a presents the comparison between the simulation and the experimental results for the output voltage $V_{out,impulse}$. We remark that the maximum value of an output voltage from the experimental work is equal to 4V. This means that the maximum value of output voltage from the measurement is 1V lower than the simulation one (see Fig. 3.21a). As presented previously, this phenomenon clearly comes from the switching speed of the drain-source voltage V_{ds}, the gate-source voltage V_{gs} of N-MOSFET at a primary side (as presented in Fig. 3.12b and Fig. 3.12c) and parasitic elements of capacitors. Then, V_{gs} from experimental work is recorded and sent into the simulation one. As a result, Fig. 3.21b illustrates the improved comparison results for output voltage V_{out_imp}. Little error still occurs due to the parasitic elements of passive components.

Table 3.10: Comparison between the simulation and experimental results of optimal transformer for solution (X)

Variable	Experimental	Simulation	Relative error
Lp	1.532 µH	1.447 µH	5.88 %
Ls	1.59 µH	1.447 µH	8.9 %
M	0.726 µH	0.852 µH	14.78 %
K	0.45	0.589	23.6 %
Rp	0.2 Ω	0.199 Ω	0.5 %
Rs	0.2 Ω	0.199 Ω	0.5 %



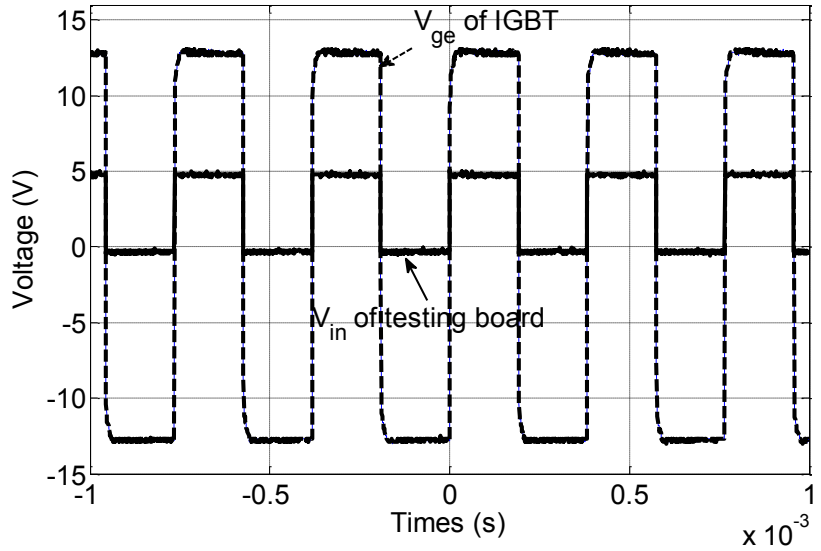
(a)



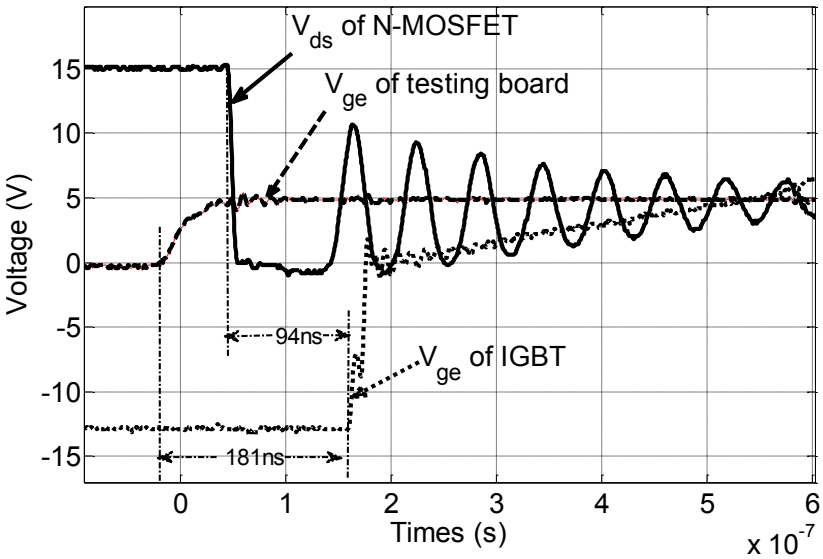
(b)

Fig. 3.21.: Comparison results for a signal transmission circuit:
(a) V_{out} waveform comparison between the simulation and experiment results,
(b) V_{out} waveform comparison after $V_{gs\_exp.}$ sent into the simulation.

Fig. 3.22a illustrates some electrical periods of an input voltage (V_{in}) of the starting point of a testing board and a gate-emitter voltage (V_{ge}) of IGBT module. We notice that V_{ge} = +/- 13.5V because of the output voltage of a DC-DC converter is equal to this voltage level. Then, Fig. 3.22b shows the zoom of the waveforms of V_{ds} (N-MOSFET), V_{in}, and V_{ge} (IGBT). The propagation delay of around 181ns is measured between the starting input voltage (V_{in}) of the testing board and the gate-emitter voltage (V_{ge}) of the IGBT. The propagation delay of 94ns from V_{ds} to V_{ge} is measured. Compare to the experimental results for ep_1 = 0.5mm, we see that these delay are higher than the experimental results of ep_1 = 0.5mm.



(a)



(b)

Fig. 3.22.: Validation results for a signal transmission function (ep_1 = 1mm):
(a) The experimental results of V_{ge} = +/- 15V for a few electrical period,
(b) The experimental results of V_{ds} of N-MOSFET, V_{in} of the testing board, V_{ge} of IGBT

As a conclusion for this section, the increase of insulation thickness layer increases the insulation voltage capabilities of the system. Thus, this design is suitable for IGBT gate drivers where high insulation voltage capabilities are required. However, there are few consequences for this design:

1. For a power transmission function: the main concern is about the converter efficiency. As we have seen, for ep_1 = 1mm, the converter efficiency is around 57% for an output power P_{out} = 1.5W.
2. For a signal transmission function: higher propagation delay is a main disadvantage of this design.

3.5. 3D aspects towards 3D-MMC

Nowadays, many researches efforts focus on three-dimensional (3D) packaging concept for an inverter leg (two power semi-conductors' dies and two diodes' dies) for semiconductors' high commutation speed applications [Eric10A] [Eric10B] [Jea12] [Jea14] [Gui16A] [Gui16B]. Compared to a classical 2D packaging, 3D packaging provides two main advantages: minimize the parasitic inductances in a commutation loop and evacuate the heat of power dies on both sides [Eric10A] [Eric10B]. According to latest references [Gui16A] [Gui16B], a 3D (embedded dies) packaging of a switching cell based on SiC MOSFET is developed with a parasitic inductance of only 0.25nH. In [Xin98], with a 2D technology (wire bondings, copper track and lyres connections), a value of 50nH is proposed. Hence, to improve the performance of MMC converter for specific applications, 3D package technology of sub-module (SM) should be implemented.

3D packaging concept for a SM-MMC: As shown in Fig. 3.23a, lower dies (T_{L1} and D_{L1}) are placed between the bus "-DC" and the middle point. Upper dies (T_{U1} and D_{U1}) are between the middle point and the bus "+DC". Moreover, semiconductor gate drivers' positions are also considered with the reflection to insulation voltage levels. A high galvanic insulation voltage gate driver (GD in Fig. 3.23b) is placed on a bus "-DC" to control the lower semiconductor dies. This system should be placed with the compromise between the parasitic inductances and the high insulation voltage capability. Then, at the gate driver's secondary side, the lower side (Sec. 1) communicates with the higher side (Sec. 2) through a very low insulation barrier (voltage "V_{sm}"). This gate driver architecture, proposed by *Nguyen V.S et al*. [Ngu16], can achieve perturbation current ten times lower than a classical architecture (two independent gate driver paths: see Fig. 1.28a). One more main advantage is the very low insulation can be done with the integrated transformers (see [Adr16]). These transformers can be fully integrated into a middle electrode of a 3D packaging (see Fig. 3.23b). Hence, some parts of gate drivers are packaged in three-dimension with semiconductors' dies. Then, heat-sinks are used on both sides to evacuate the heat of power dies. The SM capacitors C_{SM} should be placed as close as possible to the SM.

Fig. 3.23b illustrates a 3D packaging for a SM-MMC with supported references.

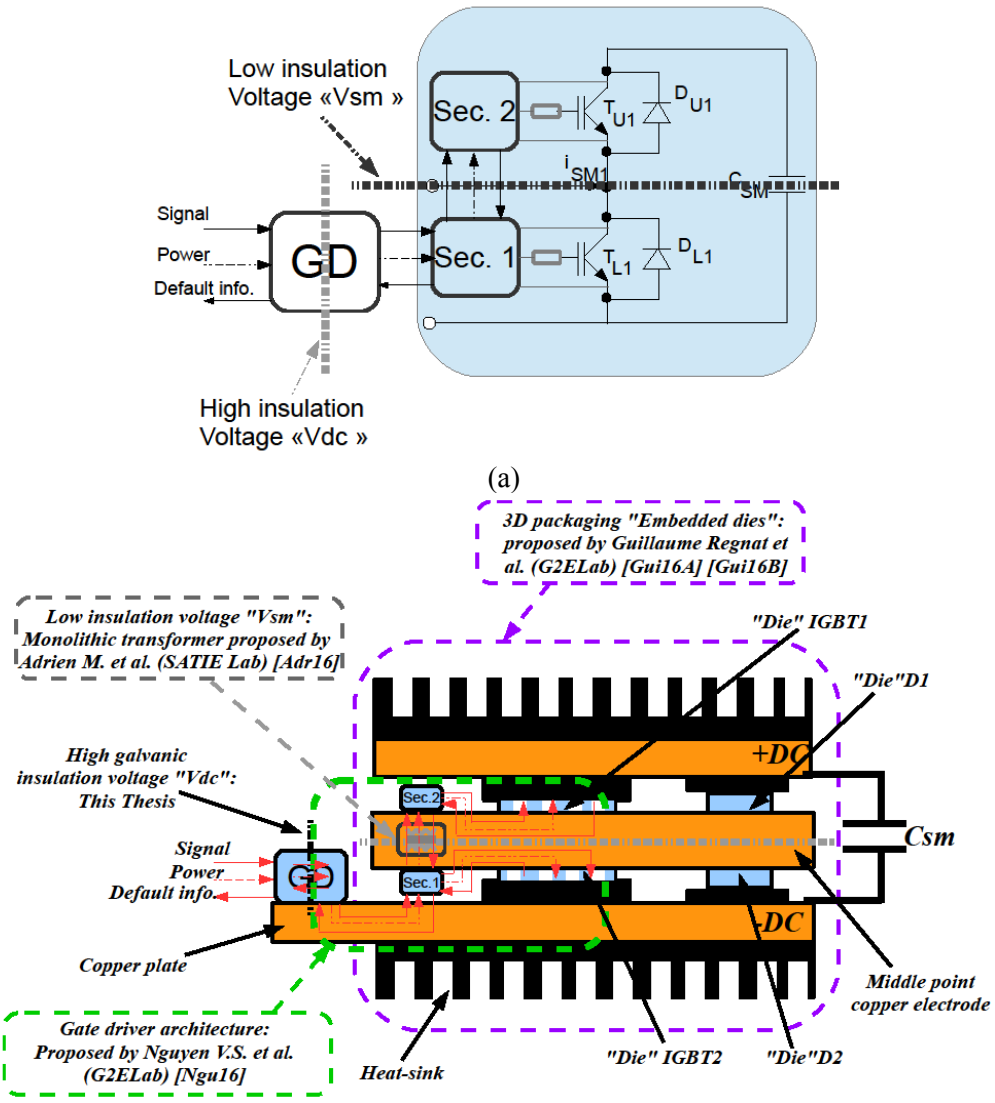


Fig. 3.23: 3D packaging of active power modules for SM:
(a) Decomposition of IGBTs and diodes' position,
(b) Proposed 3D SM with 3D packaging technology.

3.6. Conclusion

The experimental validations of IGBT gate drivers for high insulation voltage capabilities are presented in this chapter. First, a signal transmission and a power transmission functions are performed and validated separately. Several critical points are compared between the simulation and experimental results to strongly validate our proposed design methodology. In a second time, one testing board for a single channel IGBT gate driver is proposed. Then, numerous supported comparison results (for ep1 = {0.5mm and 1mm}) are provided. Experimental results are also proposed with an air gap of 3.1mm to potentially provide gate drivers up to 50kV.

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General conclusion and perspectives

This dissertation presents both the global optimization for Medium-Voltage Modular Multilevel Converter (MV-MMC) applications and the optimization methodology to optimize gate drivers for high and very high galvanic insulation voltage capabilities for power semiconductor modules in MV-MMC converters.

At the first time, a global optimization tool for MMC structures is proposed. It is partially validated with two converters specifications (converter 1: S_1 = 13.85kVA, V_{dc1} = 687V, $V_{ll1,rms}$ = 400V and converter 2: S_2 = 398kVA, V_{dc2} = 3.9kV, $V_{ll2,rms}$ = 2.4kV). Active components (IGBTs, Diodes, etc.) and passive components (capacitor and inductor's geometry) are defined as optimization variables. The optimization objectives are to maximize the converter efficiency and to minimize the converter volume. With the help of a genetic algorithm coded in MATLAB^{TM}, the results are plotted under Pareto fronts forms. As a result, two optimal Pareto fronts are obtained for converter 1 and converter 2, respectively.

- For converter 1: Pareto front provides 9 optimal solutions from the last generation of a virtual prototyping tool simulation. The converter efficiency and its volume vary from 97.1% to 97.165% and from 11 to 12 liters.
- For converter 2: Pareto front provides 17 optimal solutions. The converter efficiency and converter volume are in the range from 97.14% to 97.78% and from 160 to 218 liters, respectively.

Analyses of these optimal results are provided till the optimal solution is selected. As an example, from a total harmonic distortion (THD) constraint point of view, an optimal solution of η_{MMC} = 97.78% and Vol_{MMC} = 218 liters is selected. And their simulation results and some electrical waveforms are illustrated in the first chapter. At the end of this step design, the IGBT modules are selected. Then, the gate drivers can be designed in a second step. The challenges of gate drivers' structures for IGBT modules in one SM-MMC are proposed at the end of the first chapter of this dissertation.

The optimization designs for each driver's function (power transmission function and signal transmission function) of IGBT gate drivers for high galvanic insulation voltage level are presented in the second chapter. Insulation systems are based on compact pot core planar transformers. The insulation voltage level of the system is based on an air gap (ep_1) and its dielectric material. The study focuses on ep_1 = 1mm to 3mm. According to dielectric material's study, the insulation voltage level of 20kV to 50kV can be achieved if a polysterimide material is used. The geometrical modeling is performed with a finite element FEMM^{TM} software.

A DC-DC full-bridge series-series (FBSS) resonant converter is used for a gate drivers' power transmission function. Three pot core diameters (14mm, 18mm and 22mm) are selected for this study. The objective of this design is to maximize the converter efficiency for different combinations of insulation thickness (ep_1) and ferrite diameters (D_F). With the help of a virtual prototyping tool (FEMM^{TM} is used for geometrical simulations and LTSpice^{TM} is used for electrical transient simulations), numerous optimal Pareto fronts are plotted with respect to different ferrite diameters (D_F) and insulation layer (ep_1). The post analyses of these results are made till the optimal choice is selected with ep_1 = 0.5mm (around 20kV of insulation voltage level) and an output power of around 2W for a pot core diameter D_F = 14mm. With these parameters, the converter efficiency of 82% is achieved by simulation works. Then, the prototypes' validations are provided in Section 2 of the third chapter in this dissertation. Several comparisons such as the input voltage of the resonant tank (V_{in}), current waveforms for both sides of the resonant tank, and the converter efficiencies are presented to validate our proposed design methodology. More improved optimization results are also provided by increasing the insulation layer (up to 3mm) to respond to a very high insulation voltage application (up to 50kV). Finally, these improved designs are also validated experimentally.

Then, beside a power transmission function, a signal transmission function for gate driver for one IGBT module is proposed. An impulse circuit with a series resonant (between the capacitor and the primary side of the transformer) and a parallel resonant topology is used. To generate an impulse signal from a DC voltage (V_{dc} = 15V), an N-MOSFET at the primary side of the topology is implemented. The optimization objectives are to maximize the output voltage information and to minimize the input current of the proposed impulse circuit. A virtual prototyping tool with the same design philosophy as the power transmission is used to solve a signal transmission function problem. Thus, several Pareto fronts' for different combinations of an insulation layer ep_1 = {0.5mm to 3mm} and a transformer diameter D_F = {7mm, 9mm and 14mm} are obtained. These results are discussed till the optimal solution is selected with ep_1 = 0.5mm and D_F = 9mm. With this achieved solution, the output voltage $V_{out,signal}$ = 5.8V of the impulse circuit is obtained and used to supply logic components at the secondary of an impulse transformer such as Schmitt trigger (74HC14), etc. And other logic components of this signal transmission function, which require 15V voltage supply, are alimented by the output voltage of an insulated DC-DC power transmission function ($V_{out,power} \approx$ 15V). The simulation waveforms ($V_{out,singal}$, V_{ds} and V_{gs} and i_{mos} of MOSFET, and V_{ge} of IGBT module) are presented in the second chapter. Then, these waveforms are validated with the experimental waveforms in the third chapter of this manuscript.

For the overall validations for final applications, one optimized testing board is built to drive an IGBT module (2MBI225VN-120-50, inverter leg 1200V-225A). In this testing board, a power transmission function and a signal transmission function are performed simultaneously. The comparison results between the simulation and experimental works for these two functions are illustrated in Section 4 of the third

chapter. The comparison objectives of each function are the same as preformed in the individual validations. According to these comparison results, our proposed design methodologies are clearly validated.

Nevertheless, to continue to work towards industrial applications, some future works should be considered. They are summarized as follow:

1. For signal transmission function: study about the parasitic elements of passive components in a designed board.
2. For power transmission function: primary side and secondary side control structures.
3. Study about the optimal transformer with a selected dielectric material (polysterimide):
    - Understanding of the failures of solid insulating materials, used in a pot core planar transformer, caused by the electrical breakdown voltage in the air vacuum. Then, to solve these problems, some insulating materials (such as gel, oil, etc.) are proposed to replace air space in a whole transformer structure.
    - First, some simulation works of a pot core transformer for difference vacuums (air or gel) should be performed to validate the problem considerations and to select a suitable insulating material. The simulation works can be done with a finite element software by applying a high voltage (up to 30kV) to a transformer structure (for insulation thickness layer is up to 3mm).
    - Second, the experimental verifications should be proposed to clearly validate these systems. The works can be done by putting a whole transformer into an insulating gel or oil. A high voltage is applied to the tested transformer. This test should be performed for some hours to surely ensure the operating of the transformer.
4. Experimental verifications for an optimized sub-module (SM) of MMC converter: a classical and a challenge gate driver's topologies should be built and their results should be compared to support the proposed challenge topology. Moreover, testing insulation voltage level with a whole structure of the transformer should be performed.
5. 3D experimental set-up for one SM. According to literature, a Power-Chip-on-Chip (PCoC) technology which is briefly presented in this dissertation is a suitable candidate to solve this problem. Thus, the prototype set-up of an optimal 3D for SM should be implemented to increase the converter's SM performances.
6. 3D architecture considerations for an MMC inverter leg. One question is how to organize one sub-module to another sub-module? And one phase to another phase?

Appendix A: IGBTs, heat-sinks, and capacitors databases

Table A.1: Heat-sinks databases

Number	Manufacturer	Reference	Force type	Height (m)	Longer (m)	a_{th}	b_{th}	c_{th}
1	Arcel	AR150	Natural	0.027	0.15	0.8727	1.5529	7.9851
2	ABL	335AB	Natural	0.0325	0.099	1.1281	2.9764	24.5556
3	ABL	345AB	Natural	0.037	0.12	0.7694	2.1032	21.1463
4	ABL	340AB	Natural	0.035	0.088	1.3179	3.4951	23.4490
5	ABL	83AB	Natural	0.012	0.086	1.921	3.8437	12.2912
6	ABL	87AB	Natural	0.004	0.1	2.4968	5.9058	37.5542
7	Arcel	ARP300	Natural	0.084	0.3	0.8856	1.2139	0.3016
8	Arcel	AR125	Natural	0.125	0.125	0.3092	0.7702	12.2378
9	Arcel	AR160	Natural	0.04	0.16	0.3842	1.0712	6.2634
10	Arcel	ARP215	Ventilator force	0.077	0.215	0.0647	38.268	40.1338
11	Arcel	ARTB	Natural	0.07	0.2	0.2513	0.4995	8.1346
12	ABL	85AB	Natural	0.012	0.146	1.4	3.2	13.8629
13	ABL	89AB	Natural	0.022	0.086	1.6942	2.4175	15.6428
14	ABL	108AB	Natural	0.015	0.115	1.549	3.6028	14.4304
15	ABL	110AB	Natural	0.016	0.105	1.5536	2.5856	20.1011
16	ABL	114AB	Natural	0.025	0.1354	0.9086	6.5128	21.3337
17	ABL	115AB	Natural	0.027	0.15	0.8621	6.1941	21.2753
18	ABL	120AB	Natural	0.03	0.185	0.2951	3.2122	12.6683
19	ABL	124AB	Natural	0.02	0.2	0.5	2.4	13.8629

Table A.2: IGBTs databases

Number	Manufacturer	Reference	$V_{ce,max}$ (V) @Tj,max	$V_{ce,on}$ (V) @Tj = 25°	I_{ce} (A) @Tj = 25°
1	IR_D2PaK	IRFS4010PbF	100	0.5	108
2	IR_TO262	IRFSL4010PbF	100	0.5	106
3	IR_TO220	IRF510	100	0.5	5.6
4	Fairchild	FDH3632	100	0.5	80
5	IR_D2PaK	IRFS4010PbF	100	0.5	106
6	IR_TO262	IRFS4010PbF	100	0.5	106
7	ON	NTB35N15	150	0.5	37
8	Fairchild	HUF75852G3	150	0.5	75
9	IR	IRFP4568PbF	150	0.5	171
10	IR	IRFB52N15D	150	0.5	60
11	IR	IRFSS2N15D	150	0.5	60
12	Fairchild	FQP46N15	150	0.5	45.6
13	Vishay	IRF640	200	0.5	18
14	Vishay	IRFI620G	200	0.5	4.8
15	Vishay	IRFI630G	200	0.5	5.9
16	Vishay	IRLI640G	200	0.5	17
17	Vishay	IRLI630G	200	0.5	9
18	IR	IRLI620GPbF	200	0.5	5.2
19	Vishay	IRF624	250	0.5	4.4
20	Vishay	IRF634	250	0.5	5.6
21	Vishay	IRF644	250	0.5	7.9
22	Fairchild	FGPF30N30D	300	0.7	30
23	Fairchild	FGA180N30D	300	0.7	30
24	IXYS	IXGH100N30B3	300	0.8	30

25	IXYS	IXGH120N30C3	300	1.75	120
26	IXYS	IXGN400N30A3	300	0.7	400
27	Fee-Front runner	2MBI150U2A-060	600	0.8	150
28	POWREX	CM200DY-12NF	600	1.2	200
29	FUJI Electric	1MBH50D-060	600	1.1	20
30	Infineon	IHW30N60T	600	1.1	60
31	Infineon	IHW40N60RF	600	1.1	40
32	Infineon	IWW30N60H3	600	1.3	30
33	IXYS	IXGR60N60C3C1	600	1	75
34	IXYS	IXGN400N60B3	600	1	28
35	Infineon	FF600R07ME4-B11	650	0.7	700
36	Infineon	F3L400R07ME4-B23	650	0.75	450
37	Infineon	FF450R07ME4-B11	650	0.7	560
38	Infineon	FF400R07KE4	650	0.68	485
39	Infineon	FF300R07ME4-B11	650	0.7	390
40	IXYS	IXYP8N90C3D1	900	1.4	8
41	IXYS	IXYA8N90C3D1-ND	900	1.4	8
42	IXYS	IXYH40N90C3D1	900	1.2	40
43	IXYS	IXYN80N90C3H1	900	1.25	70
44	IXYS	IXYH24N90C3D1	900	1.5	24
45	Infineon	FF400R12KE3	1200	0.75	400
46	Infineon	FF200R12KS4	1200	1.5	200
47	Infineon	FF450R12HT4	1200	0.7	450
48	Eupec	FF800R12KF4	1200	1.2	800
49	DYNEX	DIM800DCM12-	1200	1	1600

		A000			
50	DYMEX	DIM800DDM12-A000	1200	1	800
51	IXYS	IXYH30N120C3D1	1200	1.4	30
52	Infineon	FZ600R17KE3	1700	0.9	600
53	Infineon	FF300R17KE4	1700	1.05	300
54	ABB	5SNA1600N170100	1700	1	1600
55	ABB	5SND0800M170100	1700	1.05	800
56	ABB	5SNE0800M170100	1700	1	800
57	DYNEX	DIM400PHM17-A000	1700	1	400
58	DYNEX	DIM600DDM17-A000	1700	1.5	600
59	ABB	5SNA1200E250100	2500	1.5	1200
60	ABB	5SNA1500E250300	2500	1	1500
61	Mitsubishi	CM400DY-50H	2500	2	400
62	Mitsubishi	CM800HB-50H	2500	1.8	800
63	Mitsubishi	CM1200HC-50H	2500	1.7	1200

Table A.3: Capacitors databases

Number	Manufacturer	Reference	V_{rate} (V)	C (F)
1	RoHS	ALS—332ND250	250	3.3×10^{-3}
2	RoHS	381LR271M250H022	250	2.7×10^{-4}
3	RoHS	381LR331M250H032	250	3.3×10^{-4}
4	RoHS	381LR391M250J022	250	3.9×10^{-4}
5	RoHS	ALS3—472QD250	250	4.7×10^{-3}
6	RoHS	381LR681M250J452	250	6.8×10^{-4}
7	RoHS	ALS3—223QT250	250	2.2×10^{-2}
8	RoHS	ALS3—153NT250	250	1.5×10^{-2}
9	RoHS	ALS3—103QH250	250	1×10^{-2}
10	RoHS	ALS3—682QC250	250	6.8×10^{-3}
11	RoHS	ALS3—331DA350	350	0.33×10^{-3}
12	RoHS	ALS3—471DE350	350	0.47×10^{-3}
13	RoHS	ALS3—681DF350	350	0.68×10^{-3}
14	RoHS	ALS3—102KE350	350	1×10^{-3}
15	RoHS	ALS3—152KF350	350	1.5×10^{-3}
16	RoHS	ALS3—222ND350	350	2.2×10^{-3}
17	RoHS	ALS3—332MF350	350	3.3×10^{-3}
18	RoHS	ALS3—472QH350	350	4.7×10^{-3}
19	RoHS	ALS3—682NP350	350	6.8×10^{-3}
20	RoHS	ALS3—103NT350	350	1×10^{-2}
21	KEMET	C44AFGP6100ZG0J	400	1×10^{-4}
22	KEMET	C44AFGP6130ZA0J	400	1.3×10^{-4}
23	KEMET	C44AFGP6150ZA0J	400	1.5×10^{-4}
24	KEMET	C44AFGR6250ZA0J	400	2.5×10^{-4}
25	KEMET	C44AFGR6200ZA0J	400	2×10^{-4}

26	KEMET	C44AFGR6300ZA0J	400	3×10^{-4}
27	KEMET	C44AFGR6330ZA0J	400	3.3×10^{-4}
28	EPCOS	B4345*A9688MO##	400	6.8×10^{-3}
29	EPCOS	B4345*A9828MO##	400	1×10^{-2}
30	EPCOS	B4345*A9159MO##	400	1.5×10^{-2}
31	EPCOS	B4345*A6828MO##	500	8.2×10^{-3}
32	EPCOS	B4345*B6688MO##	500	6.8×10^{-3}
33	EPCOS	B4345*A6688MO##	500	5.6×10^{-3}
34	EPCOS	B4345*B6478MO##	500	4.7×10^{-3}
35	EPCOS	B4345*A6398MO##	500	3.9×10^{-3}
36	EPCOS	B4345*A6338MO##	500	3.3×10^{-3}
37	EPCOS	B4345*B6278MO##	500	2.7×10^{-3}
38	EPCOS	B4345*B6228MO##	500	2.2×10^{-3}
39	SBE	700D10896-348	600	1×10^{-3}
40	KEMET	C44AHGP6100ZA0J	600	0.1×10^{-3}
41	KEMET	C44AHGP575ZA0J	600	75×10^{-6}
42	KEMET	C44AHGP5700ZA0J	600	70×10^{-6}
43	KEMET	C44AHGP5500ZG0J	600	50×10^{-6}
44	KEMET	C44AHFP5300ZC0J	600	30×10^{-6}
45	KEMET	C44AHFP5250ZB0J	600	25×10^{-6}
46	KEMET	C44AHFP5220ZA0J	600	22×10^{-6}
47	KEMET	C44AHFP5200ZB0J	600	20×10^{-6}
48	KEMET	C44AHFP5150ZA0J	600	15×10^{-6}
49	KEMET	C44AJGR6100ZA0J	700	1×10^{-4}
50	KEMET	C44AJGR5750ZA0J	700	75×10^{-6}
51	KEMET	C44AJGP5700ZA0J	700	70×10^{-6}

52	KEMET	C44AJGP5600ZA0J	700	60×10^{-6}
53	KEMET	C44AJGP5500ZA0J	700	50×10^{-6}
54	KEMET	C44AJGP5250ZA0J	700	25×10^{-6}
55	KEMET	C44AJGP5220ZA0J	700	22×10^{-6}
56	KEMET	C44AJFP5100ZA0J	700	7.5×10^{-6}
57	KEMET	C44AJFP4600ZA0J	700	6×10^{-6}
58	KEMET	C44AJFP4500ZA0J	700	5×10^{-6}

Appendix B: Detail of simulation results for the selected solutions for signal transmission function

B.1. I planar ferrite transformer technology

B.1.1. Double-layer I planar hard ferrite transformer

Fig. B.1 illustrates Pareto fronts' solutions for double-layer I planar transformer. And all variables (transformer and electrical circuits) correspond to the six possible chosen solutions are shown in Table B.1.

Table B.1: Optimal solution values

Results	*Transfo.1*	*Transfo. 2*	*Transfo. 3*	*Transfo. 4*	*Transfo. 5*	*Transfo. 6*
V_{out}	*5.6792 V*	*5.8539 V*	*6.7387 V*	*4.28 V*	*4.66 V*	*5.65 V*
I_{mos}	*1.57 A*	*0.93 A*	*1.09 A*	*1.02 A*	*0.97 A*	*1.39 A*
x_1	*0.32 mm*	*0.79 mm*	*0.77 mm*	*0.43 mm*	*0.47 mm*	*0.42 mm*
x_2	*0.53 mm*	*0.86 mm*	*0.67 mm*	*0.77 mm*	*0.51 mm*	*0.50 mm*
x_3	*0.21 mm*	*0.49 mm*	*0.58 mm*	*0.54 mm*	*0.27 mm*	*0.94 mm*
x_4	*0.33 mm*	*0.49 mm*	*0.50 mm*	*0.47 mm*	*0.95 mm*	*0.24 mm*
n_1	*3 turns*	*3 turns*	*4 turns*	*4 turns*	*5 turns*	*3 turns*
n_2	*4 turns*	*4 turns*	*5 turns*	*4 turns*	*5 turns*	*3 turns*
C_1	*294 pF*	*245 pF*	*788 pF*	*496 pF*	*802 pF*	*269 pF*
C_2	*276 pF*	*198 pF*	*417 pF*	*215 pF*	*525 pF*	*145 pF*
R_{out}	*24.46 kΩ*	*21.89 kΩ*	*18.4 kΩ*	*21.89 kΩ*	*20 kΩ*	*25.29 kΩ*

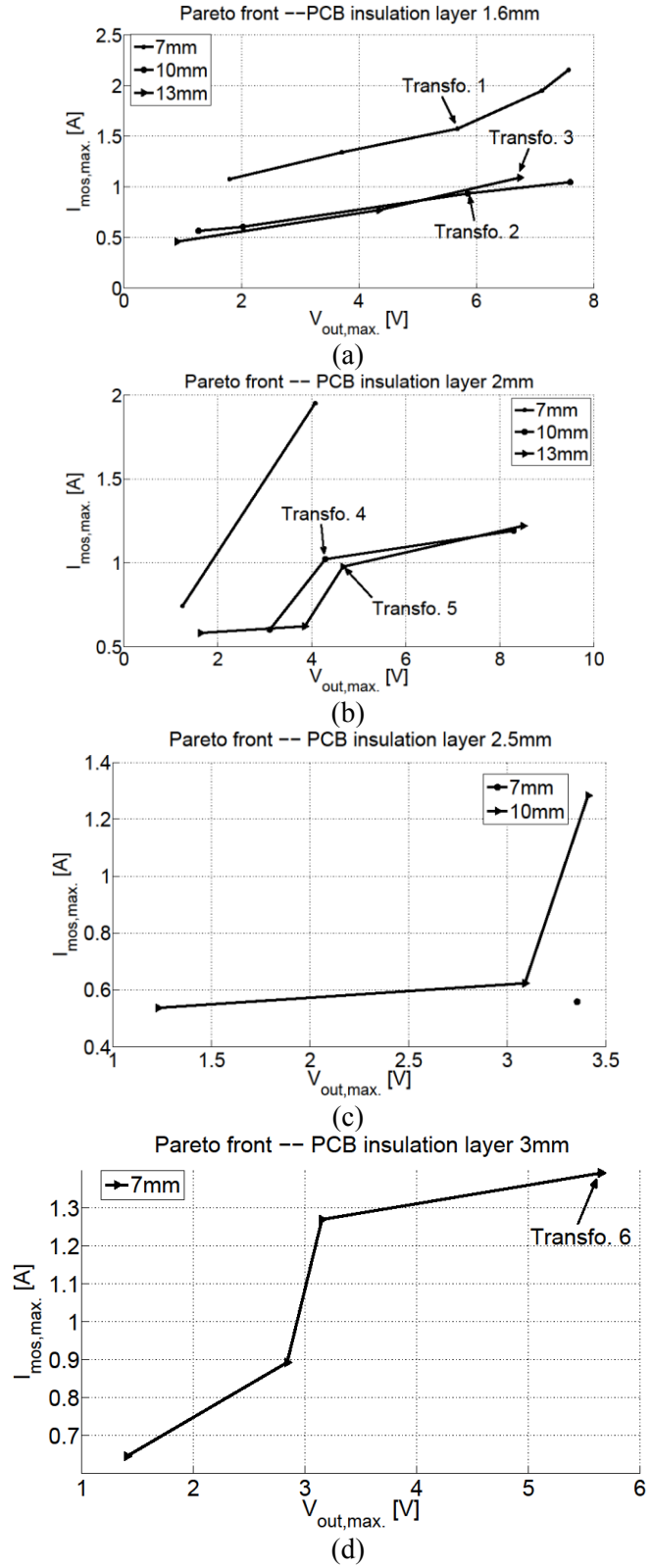
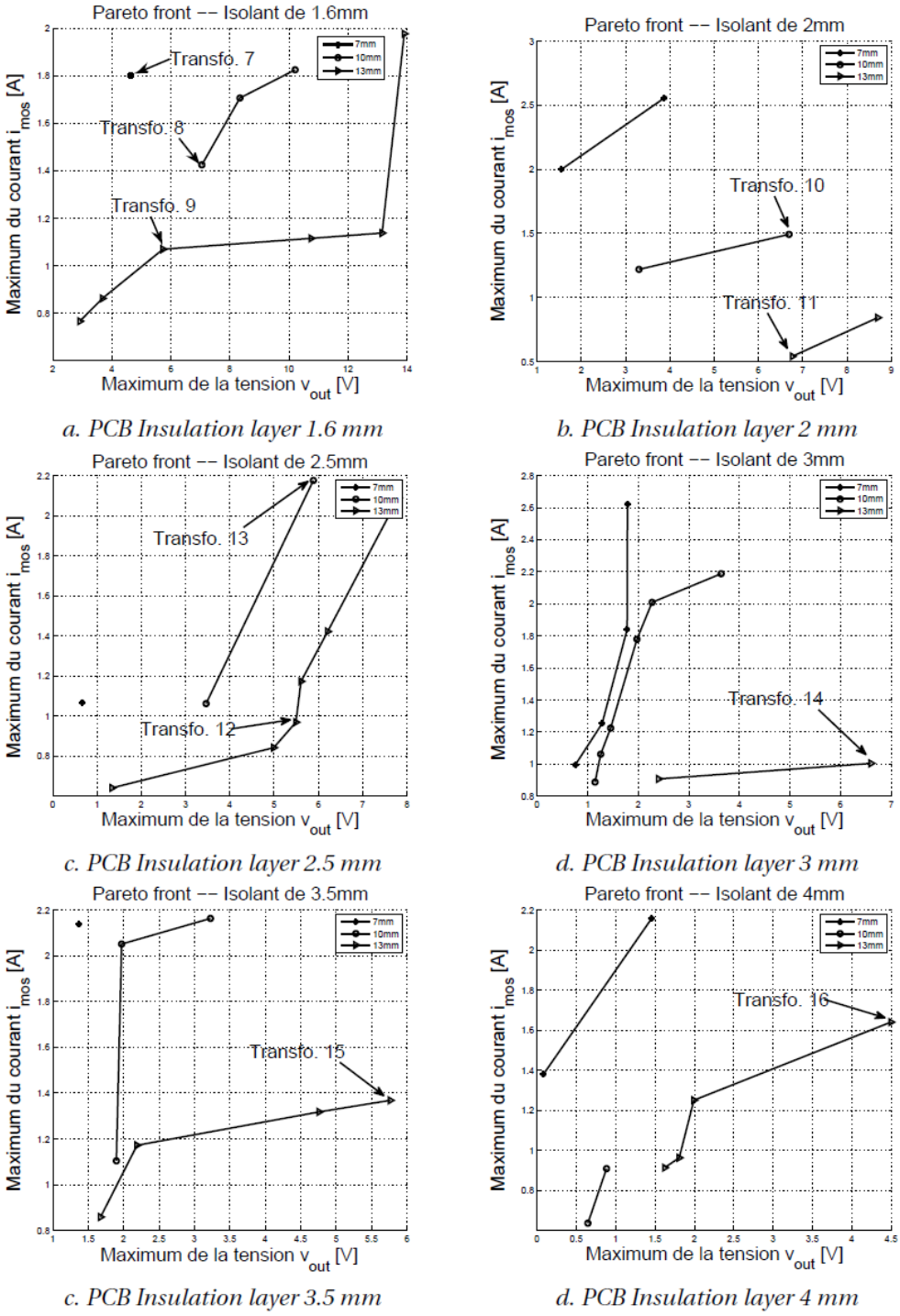


Fig.B.1: Pareto fronts' solutions for double-layer transformer

B.1.2. Mono-layer I planar hard ferrite transformer

Fig. B.2 illustrates Pareto fronts' solutions for mono-layer I planar hard ferrite transformer. And all variables (transformer and electrical circuits) correspond to the six possible chosen solutions are shown in Table B.2 and Table B.3.



a. PCB Insulation layer 1.6 mm

b. PCB Insulation layer 2 mm

c. PCB Insulation layer 2.5 mm

d. PCB Insulation layer 3 mm

c. PCB Insulation layer 3.5 mm

d. PCB Insulation layer 4 mm

Fig.B.2: Pareto fronts' solutions for mono-layer I planar hard ferrite transformer

Table B.2: Optimal solutions (Transfo. 7-11)

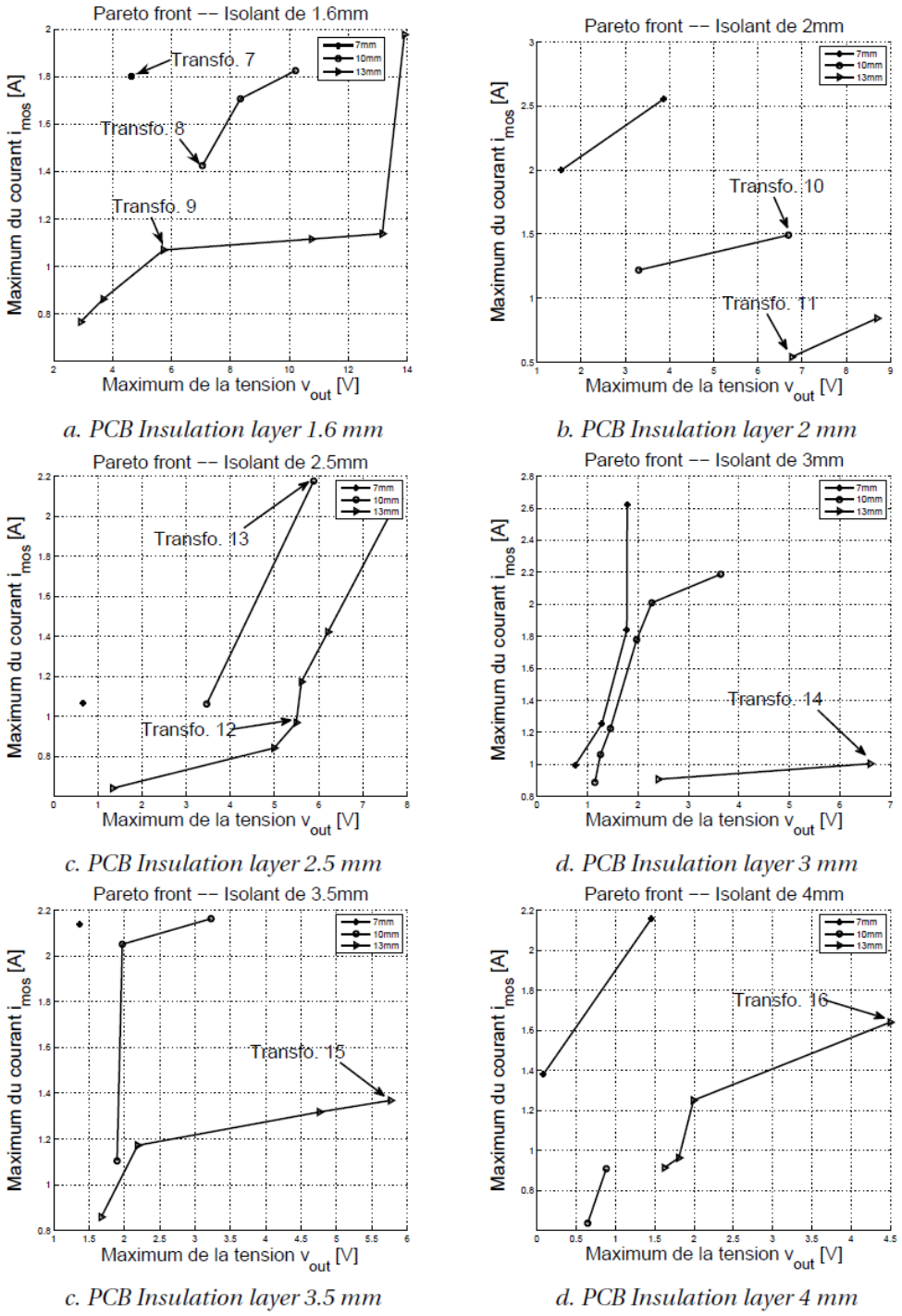
Results	*Transfo.7*	*Transfo. 8*	*Transfo. 9*	*Transfo. 10*	*Transfo. 11*
V_{out}	*5 V*	*7 V*	*5.74 V*	*6.69 V*	*6.76 V*
I_{mos}	*1.8 A*	*1.43 A*	*1.07 A*	*1.49 A*	*0.54 A*
x_1	*0.23 mm*	*0.99 mm*	*0.65 mm*	*0.30 mm*	*0.49 mm*
x_2	*0.42 mm*	*0.51 mm*	*0.37 mm*	*0.63 mm*	*0.78 mm*
x_3	*0.26 mm*	*0.40 mm*	*0.46 mm*	*0.48 mm*	*0.21 mm*
x_4	*0.85 mm*	*0.45 mm*	*0.80 mm*	*0.29 mm*	*0.88 mm*
n_1	*5 turns*	*3 turns*	*4 turns*	*5 turns*	*5 turns*
n_2	*3 turns*	*4 turns*	*5 turns*	*4 turns*	*4 turns*
C_1	*883 pF*	*430 pF*	*225 pF*	*789 pF*	*198 pF*
C_2	*782 pF*	*230 pF*	*287 pF*	*115 pF*	*105 pF*
R_{out}	*17.77 kΩ*	*15.79 kΩ*	*10.53 kΩ*	*5.63 kΩ*	*7 kΩ*

Table B.3: Optimal solutions (Transfo. 12-16)

Results	*Transfo.12*	*Transfo. 13*	*Transfo. 14*	*Transfo. 15*	*Transfo. 16*
V_{out}	*5.49 V*	*5.88 V*	*6.60 V*	*5.76 V*	*4.50 V*
I_{mos}	*0.96 A*	*2.17 A*	*1 A*	*1.36 A*	*1.64 A*
x_1	*0.87 mm*	*0.45 mm*	*0.49 mm*	*0.35 mm*	*0.89 mm*
x_2	*0.38 mm*	*0.39 mm*	*0.79 mm*	*0.61 mm*	*0.67 mm*
x_3	*0.71 mm*	*0.46 mm*	*0.51 mm*	*0.87 mm*	*0.56 mm*
x_4	*0.85 mm*	*0.31 mm*	*0.55 mm*	*0.25 mm*	*0.97 mm*
n_1	*5 turns*	*4 turns*	*5 turns*	*5 turns*	*4 turns*
n_2	*3 turns*	*5 turns*	*5 turns*	*5 turns*	*4 turns*
C_1	*524 pF*	*798 pF*	*489 pF*	*646 pF*	*846 pF*
C_2	*146 pF*	*305 pF*	*300 pF*	*244 pF*	*552 pF*
R_{out}	*19.40 kΩ*	*8.2 kΩ*	*4.19 kΩ*	*1.71 kΩ*	*6.57 kΩ*

B.1.3. Mono-layer I planar soft ferrite transformer

Fig. B.3 illustrates Pareto fronts' solutions for mono-layer I planar soft ferrite transformer. And all variables (transformer and electrical circuits) correspond to the six possible chosen solutions are shown in Table B.4.



a. PCB Insulation layer 1.6 mm

b. PCB Insulation layer 2 mm

c. PCB Insulation layer 2.5 mm

d. PCB Insulation layer 3 mm

c. PCB Insulation layer 3.5 mm

d. PCB Insulation layer 4 mm

Fig.B.3: Pareto fronts' solutions for mono-layer I planar hard ferrite transformer

Table B.4: Optimal solutions (Transfo. 17-22)

Results	*Transfo. 17*	*Transfo. 18*	*Transfo. 19*	*Transfo. 20*	*Transfo. 21*	*Transfo. 22*
V_{out}	*7.76 V*	*6.51 V*	*5.10 V*	*5.35 V*	*5.58 V*	*5.35 V*
I_{mos}	*0.82 A*	*1.44 A*	*3 A*	*1.67 A*	*1.50 A*	*2.80 A*
x_1	*0.84 mm*	*0.64 mm*	*0.34 mm*	*0.67 mm*	*0.99 mm*	*0.47 mm*
x_2	*0.33 mm*	*0.24 mm*	*0.42 mm*	*0.50 mm*	*0.30 mm*	*0.43 mm*
x_3	*0.82 mm*	*0.66 mm*	*0.48 mm*	*0.31 mm*	*0.62 mm*	*0.88 mm*
x_4	*0.32 mm*	*0.72 mm*	*0.89 mm*	*0.28 mm*	*0.65 mm*	*0.32 mm*
n_1	*4 turns*	*4 turns*	*3 turns*	*3 turns*	*4 turns*	*3 turns*
n_2	*3 turns*	*3 turns*	*3 turns*	*5 turns*	*3 turns*	*3 turns*
C_1	*150 pF*	*405 pF*	*534 pF*	*258 pF*	*612 pF*	*557 pF*
C_2	*445 pF*	*176 pF*	*663 pF*	*247 pF*	*184 pF*	*165 pF*
R_{out}	*4.19 kΩ*	*12.92 kΩ*	*4.75 kΩ*	*16.30 kΩ*	*18.48 kΩ*	*9.53 kΩ*

B.2. Pot core planar transformer technology

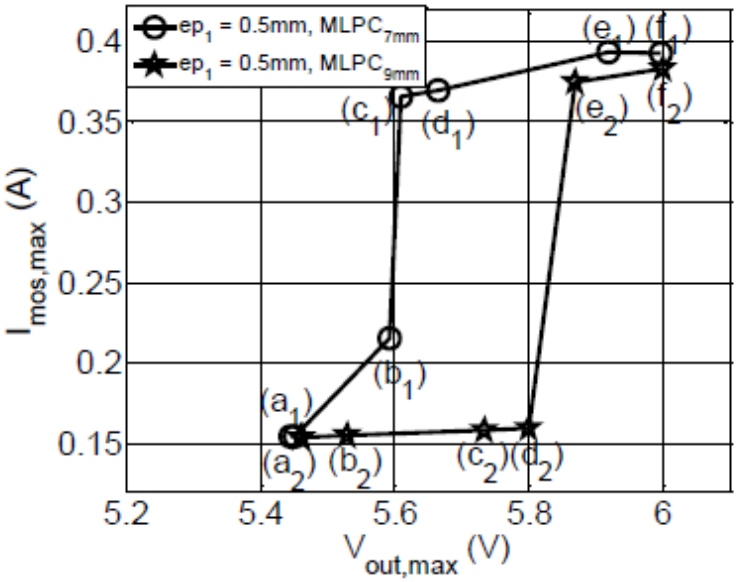


Fig.B.4: Pareto fronts' solutions for pot core planar transformer (ep_1 = 0.5mm: detail in chapter 2)

Fig. B.4 illustrates Pareto fronts' solutions for the selected solutions for pot core planar transformer. Their simulation values are presented in Table B.5.

Table B.5: Simulation results of possible optimal solutions

Solu.	$V_{out,max}$ *(V)*	$I_{mos,max}$ *(A)*	ep_1 *(mm)*	D_F *(mm)*	C_1 *(pF)*	C_2 *(pF)*	R_{out} *(kΩ)*	n_1 *(turns)*	x_1 *(mm)*	n_{layer}
(a_1)	*5.42*	*0.15*	*0.5*	*7*	*110*	*272*	*30*	*2*	*0.335*	*2*
(a_2)	*5.42*	*0.15*	*0.5*	*9*	*110*	*301*	*2.9*	*2*	*0.346*	*2*
(b_1)	*5.59*	*0.22*	*0.5*	*7*	*605*	*1100*	*30*	*2*	*0.312*	*2*
(b_2)	*5.55*	*0.15*	*0.5*	*9*	*200*	*486*	*28.7*	*2*	*0.32*	*2*
(c_1)	*5.62*	*0.355*	*0.5*	*7*	*630*	*1100*	*30*	*2*	*0.34*	*3*
(c_2)	*5.72*	*0.15*	*0.5*	*9*	*110*	*270*	*30*	*2*	*0.32*	*2*
(d_1)	*5.65*	*0.353*	*0.5*	*7*	*640*	*1100*	*30*	*2*	*0.32*	*2*
(d_2)	*5.8*	*0.15*	*0.5*	*9*	*108.6*	*316*	*30*	*2*	*0.32*	*2*
(e_1)	*5.9*	*0.38*	*0.5*	*7*	*800*	*1100*	*30*	*2*	*0.252*	*2*
(e_2)	*5.85*	*0.364*	*0.5*	*9*	*700*	*1200*	*30*	*2*	*0.35*	*2*
(f_1)	*6*	*0.39*	*0.5*	*7*	*800*	*1000*	*30*	*2*	*0.252*	*2*
(f_2)	*5.88*	*0.38*	*0.5*	*9*	*790*	*1200*	*30*	*2*	*0.248*	*2*

Résumé en Français

Conception et optimisation de modules pour onduleurs MMC de moyenne puissance. Commande rapprochée à haute isolation galvanique et packaging 3D.

I. Introduction

L'objectif de cette thèse est de proposer une méthodologie de conception par optimisation d'un système de convertisseur MMC (Modular Multilevel Converter) de moyenne puissance et des fonctions de transmission de puissance et de transmission d'ordres pour drivers d'IGBTs avec une barrière d'isolation pouvant aller jusqu'à 50kV.

II. Optimisation de MMC et architecture de la commande rapprochée

II.1. Descriptions des convertisseurs MMC

Dans les applications industrielles, les onduleurs multi-niveaux apportent une flexibilité en terme de commande et de filtrage sur les charges pilotées (machines électriques, réseaux de transport et de distribution, réseaux embarqués, etc.). Dans les années 2000, le MMC est proposé et est illustré à la Fig. 1a.

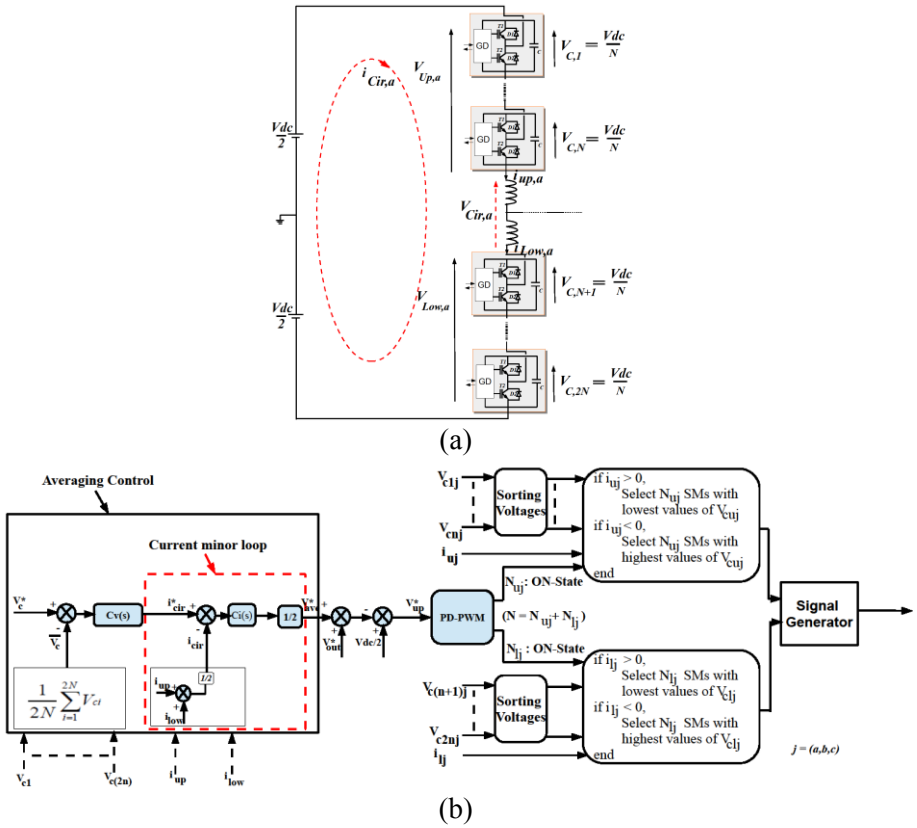


Fig. 1: Le convertisseur MMC et son contrôle interne

Ce convertisseur est composé de trois bras. Dans chaque bras est associé deux demi-bras composés de sous modules élémentaires. Ces sous modules sont constitués d'une cellule de commutation et d'un condensateur. La structure MMC présente beaucoup d'avantages tels que sa modularité mais présente aussi des inconvénients comme la complexité de sa modélisation et de son contrôle dû au grand nombre de modules de puissances (semi-conducteurs) à contrôler.

La structure MMC est illustrée Fig. 1a, son contrôle interne contrôle le courant de circulation ($i_{cir,a}$) pour bien contrôler les tensions aux bornes des inductances et d'équilibrer les tensions des condensateurs dans les sous modules. Le Fig. 1b détaille la méthode de contrôle interne de MMC.

II.2. Pré-dimensionnement de MMC

Les objectifs de l'optimisation: Dans la suite du développement, nous verrons que le maximum du rendement η_{con} est le premier objectif à optimiser et que son volume Vol_{mmc} est le deuxième objectif à minimiser. Pour arriver à déterminer ces objectives, nous avons décrit des modèles de pertes pour les composants, la géométrie de l'inductance et la modèle thermique (sont résumés dans la Fig. 2).

Les variables: les 11 variables sont résumés dans le vecteur de variable $X_{opt.}$

$$X_{opt} = (N_{SM}, T_{semi}, C_{SM}, L_j, N_{hs}, f_c, e, A, S, s\ n_l)^t$$

- $N_{SM} \in \{2, 3, 4, 5, 6 , 7, 8, 9, 10, 11, 12, 13, 14, 15\}$;
- T_{semi}: les semi-conducteurs; $C_{SM} \in [0.1mF, 10mF]$; $L_j \in [0.1mH, 10mH]$;
- $N_{hs} \in \{1, \ldots, 15\}$: les dissipateurs ; $f_c \in \{1kHz, \ldots , 10kHz\}$; et
- *Variables géometries de l'inductance:* $e \in [0, 5mm]$; $A \in [10^{-4}m^2, 100x10^{-4}m^2]$; $S \in [10^{-6}m^2, 36x10^{-4}m^2]$; $s \in [10^{-7}m^2, 16x10^{-6}m^2]$; $n_l \in [1, 200]$ (voir Fig. 2a).

II.3. Résultats d'optimisation

L'organigramme de l'algorithme d'optimisation basé sur un algorithme génétique (AG) est présenté sur la Fig. 2c. Les paramètres de l'AG sont : 50 générations et 20 individus. Les cahiers des charges des convertisseurs sont présentés: $V_{LL,rms}$=2.3kV, $I_{p,rms}$=100A, V_{dc}=3.9kV, S_{out}=398kVA, Cos(φ)=0.95 et m=0.95. Ses résultats d'optimisation (17 solutions) sous la forme de Front de Pareto sont présentés à la Fig. 3a. Le rendement du convertisseur et son volume sont compris entre 97.14% à 97.78% et 160 litres à 220 litres. Les formes d'ondes de tension de sortie, les courants, et les équilibrages des tensions des condensateurs de la solution (A) sont illustrées dans les Fig. 3b-d. Les pertes de cette solution sont réparties suivant : les modules puissances (90% en conductions, 9% en commutation) et 1% de pertes pour les composants passifs.

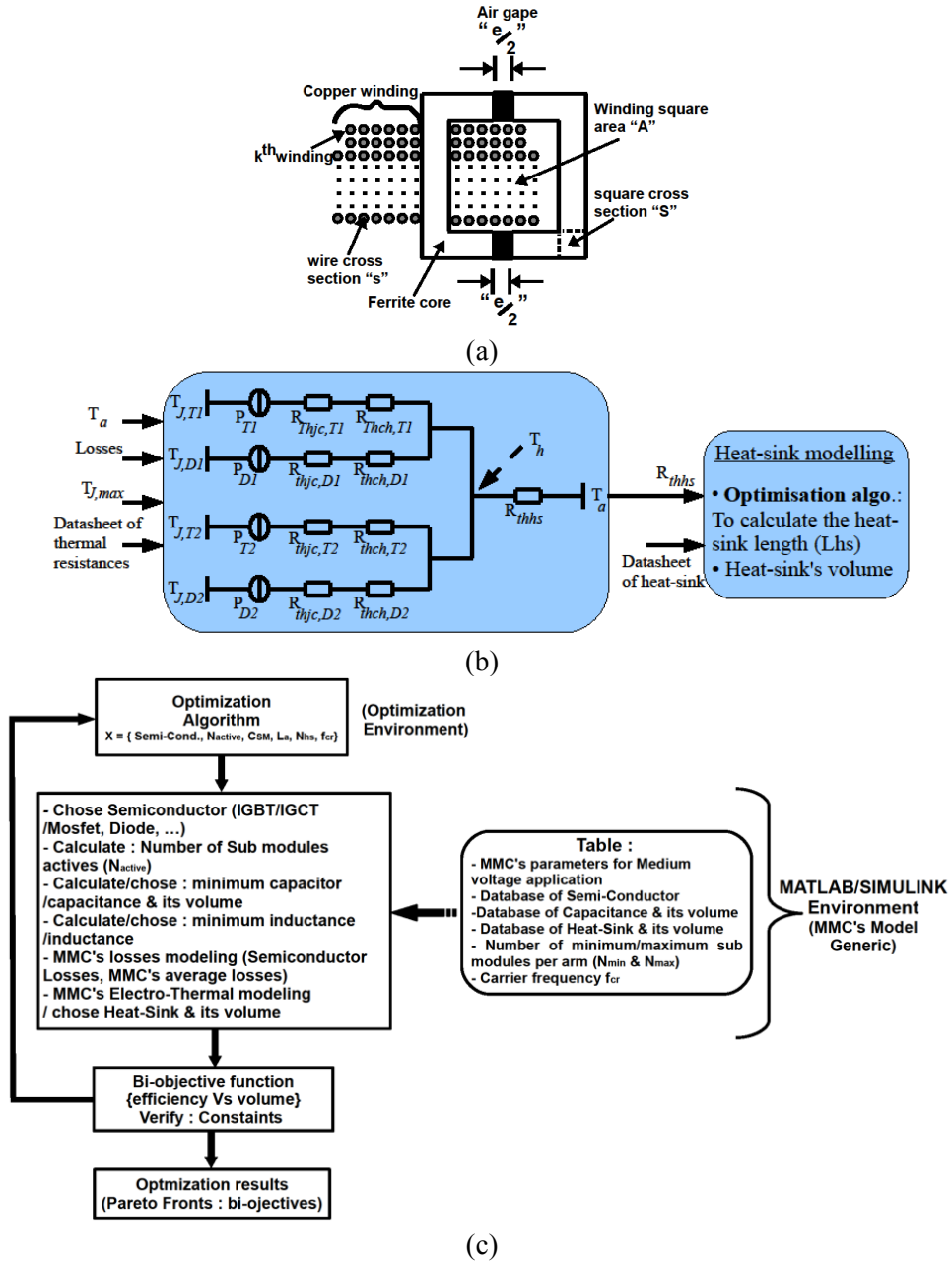


Fig. 2: Outil de pré-dimensionnement de convertisseurs MMC

Dans ce nouveau contexte des applications de moyenne tension, nous proposons d'étudier la potentialité des onduleurs MMC. Cependant, des travaux préliminaires nous conduisent à étudier les systèmes de commande rapprochée pour cette gamme de tension d'isolation mais sur la base de technologies classiques telles que les solutions à base de transformateurs magnétiques (basée sur le circuit imprimé PCB). Notre contribution, pour ce manuscrit, est de proposer un système de transmission d'ordres et de transmission de puissance à très haute isolation galvanique (jusqu'à 40kV) et de l'optimiser à l'aide d'un outil générique de prototypage virtuel.

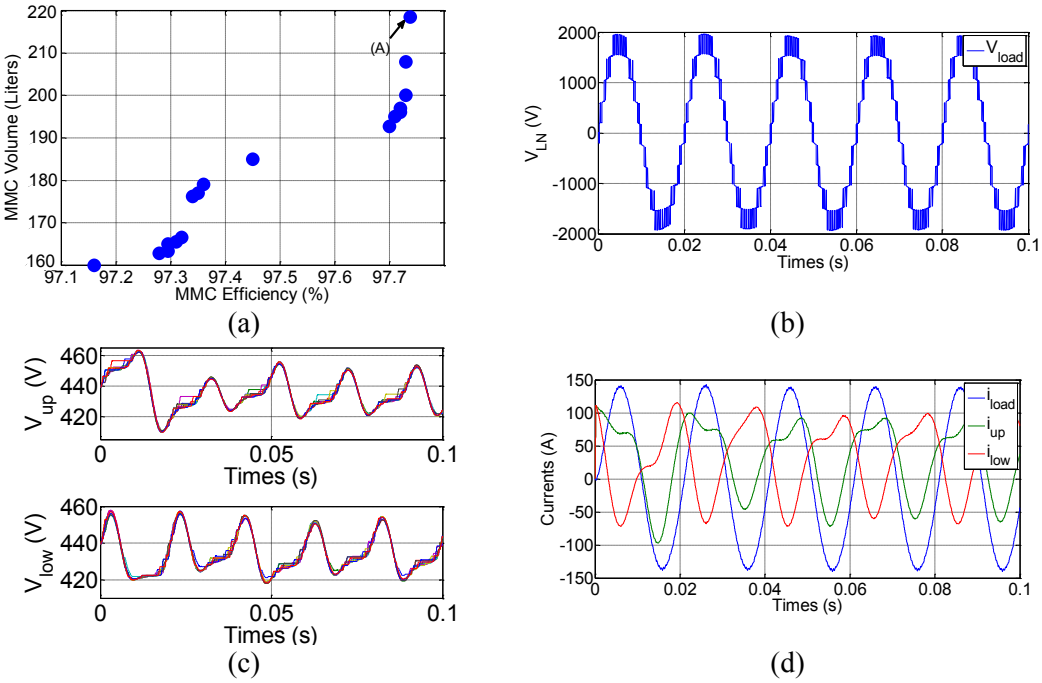


Fig. 3: Les résultats de simulation du convertisseur MMC de 400kVA

II.3. Architecture de la commande rapprochée pour les IGBTs SM-MMC

La nouvelle architecture de commande rapprochée des deux modules de puissances dans le SM-MMC est présentée à la Fig. 4a. Dans le cadre de ces travaux de doctorat, nous nous focalisons sur les fonctions de transmission d'ordres (MLI) et de transmission de puissance isolées. La technologie du transformateur est basée sur une structure planaire : circuits imprimés et matériaux magnétiques (voir la Fig.4b). Le matériau isolant "polystérimide" et l'entrefer du transformateur sont utilisés pour déterminer les niveaux d'isolation galvaniques du système. 1mm d'épaisseur de ce matériau peut maintenir la tension plus grand 40kV sur une longue période de test sans faire apparaitre les problèmes de claquage électrique.

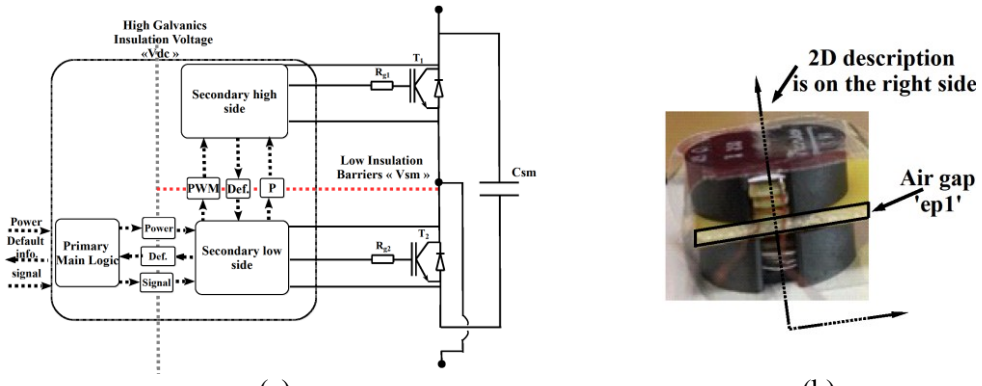


Fig. 4: Nouvelle architecture de commande rapprochées pour bras d'onduleur (ou sub-module MMC).

III. Prototypage virtuel des fonctions de transmission d'ordre et de transmission de puissance

III.1. Circuits électriques des fonctions étudiées

Comme présenté dans la Fig. 5a, la fonction de transmission de puissance est utilisée pour alimenter la partie secondaire de la fonction de transmission d'ordres isolée.

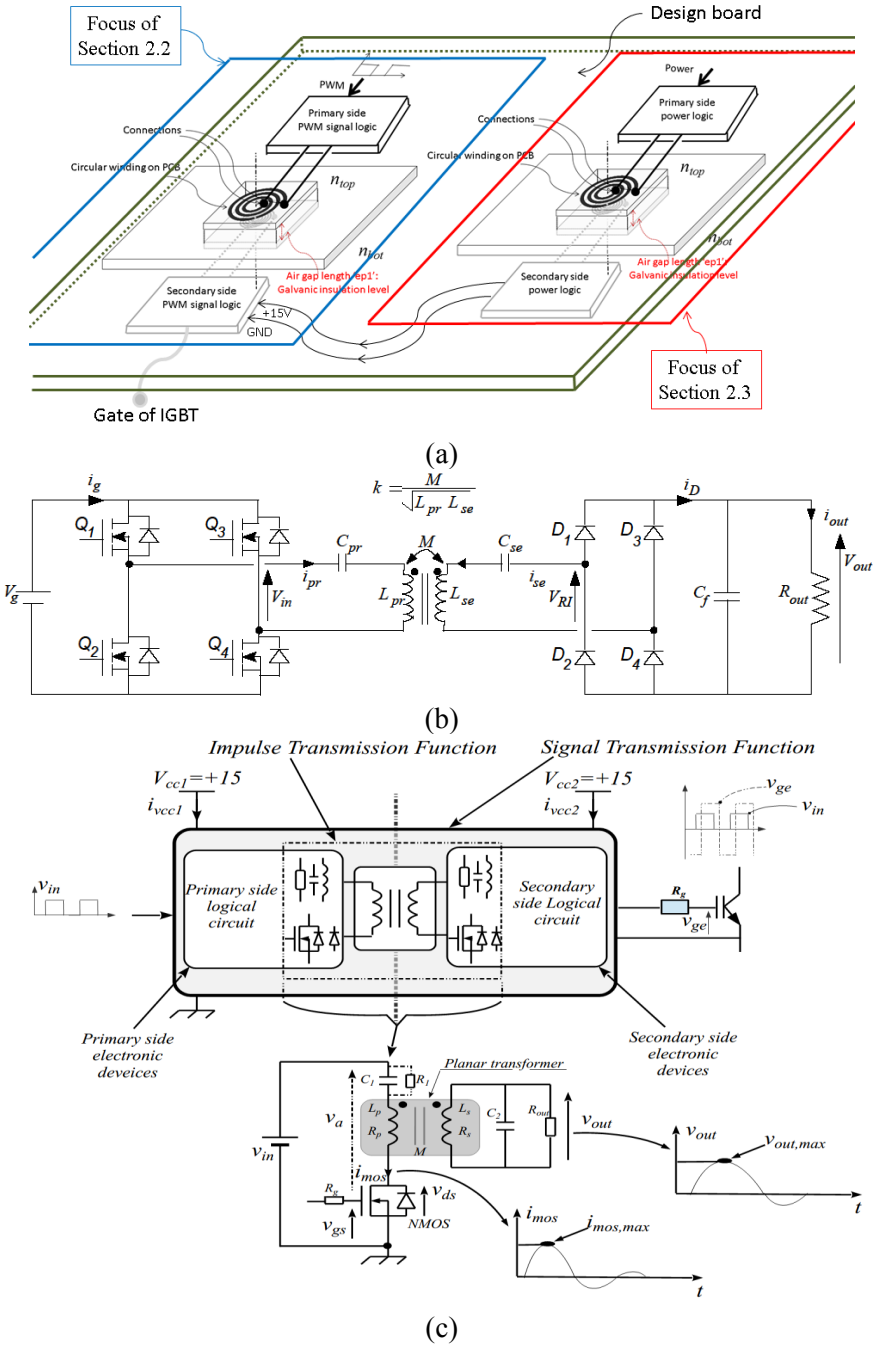


Fig. 5: Circuits électriques des fonctions de transmission puissance et de transmission d'ordre

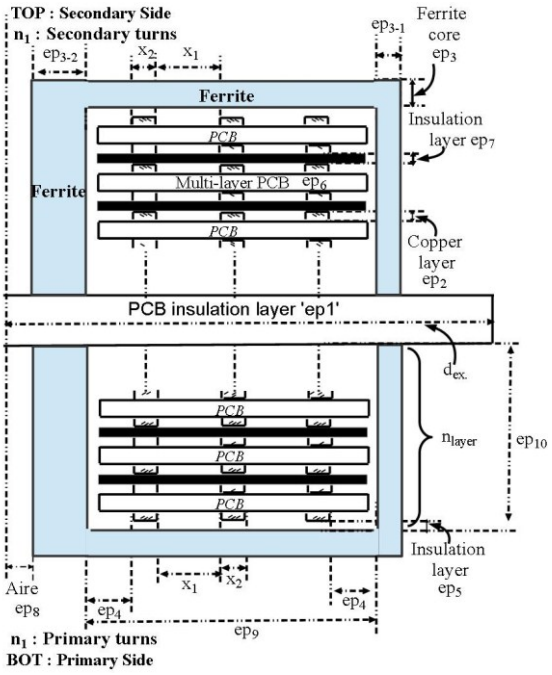
Le convertisseur DC-DC FBSS (full-bridge series-series: voir la Fig. 5b) est proposé pour ce design. Cette topologie permet de considérer les inductances de fuites du transformateur comme avantages pour faire la résonance avec les condensateurs. Nous verrons que le maximum du rendement η_{con} est le premier objectif à optimiser et que le maximum de la puissance sortie P_{out} est le deuxième objectif à minimiser.

Le synoptique de la fonction de transmission d'ordres est données sur la Fig. 5c : nous mettons en évidence la différence entre la fonction de transmission d'impulsion et le circuit logique secondaire qui permet la mise en forme des impulsions en états logiques. En bas de cette figure, nous proposons un circuit électronique de la fonction de transmission d'impulsion. Un MOSFET excite un circuit résonant série au primaire. Un circuit résonant parallèle est mis en œuvre au secondaire. La tension de sortie v_{out} est la grandeur qui permet de transmettre les impulsions. Le courant au primaire i_{mos} est vu comme une grandeur à minimiser et ce afin de minimiser la consommation moyenne du dispositif. Dans la suite du développement, nous verrons que le maximum de la tension v_{out} est le premier objectif à maximiser et que le maximum du courant i_{mos} est le deuxième objectif à minimiser.

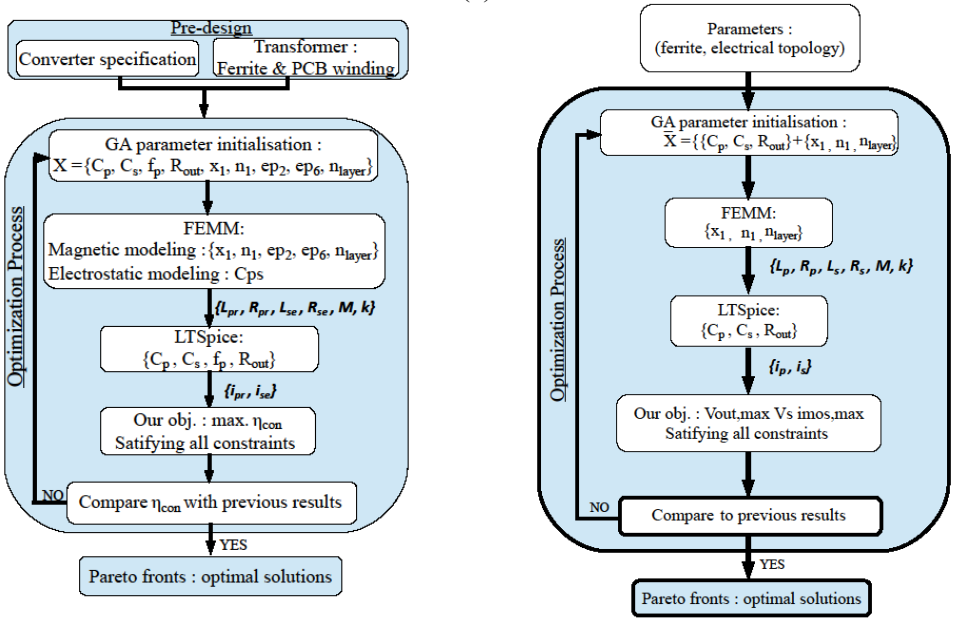
III.2. Description de l'optimisation des fonctions étudiées

Le transformateur est décrit sur la Fig. 6. Les variables géométriques sont $\{n_1, x_1, ep_2, ep_6, n_{layer}\}$. Les paramètres ep_i ($1<i<10$ sauf $i=\{2,6\}$) sont constants et dépendent d'un choix à priori du concepteur comme la tenue en tension du dispositif, les limites technologiques des pistes en cuivre, etc. A l'aide du logiciel éléments-finis FEMM, les paramètres électriques équivalents L_p, R_p, L_s, R_s et M sont calculés. Ensuite, à l'aide du logiciel LTSpice, une simulation transitoire du dispositif est effectuée afin d'estimer les deux objectifs des fonctions étudiées.

A l'aide du logiciel MATLAB, un algorithme génétique bio-bjectif est réalisé (NSGA-II) : il met en œuvre le logiciel LTSpice pour les simulations temporelles et le logiciel FEMM pour les calculs magnétiques éléments finis : Fig.6b-c (b: la partie transmission de puissance et c: la partie transmission d'ordre).



(a)



(b) (c)

Fig. 6: Description de l'optimisation des fonctions étudiées

III.3. Résultats d'optimisation : analyse des fronts de Pareto

Plusieurs scenarios sont évalués à l'aide de l'outil de prototypage virtuel en fonction de la distance d'isolation ep_1 (0.5mm à 3mm) et du diamètre maximum de ferrite (7mm à 22mm). Sur la Fig. 7a et Fig. 7b sont présentés les fronts de Pareto de la fonction de transmission de puissance et de la fonction de transmission d'ordre, respectivement.

Pour réaliser une fonction de transmission de puissance, nous devons choisir une solution avec la puissance de sortie de 2W et le rendement plus grand que 80%. Enfin, ce cahier des charges nous amène à sélectionner la solution optimal (a) (Fig. 7c).

Dans l'optique de réaliser une fonction de transmission d'ordres sur la base de la fonction de transmission d'impulsions, nous devons choisir une solution en prenant en compte des contraintes supplémentaires : la valeur de l'objectif $v_{out;max}$ est très important car la tension v_{out} est l'entrée du circuit de mise en forme de l'impulsion au secondaire. Afin d'avoir un circuit rapide, nous avons mis en œuvre des circuits logiques rapides alimentés en +5V. De ce fait, la tension $v_{out;max}$ doit être comprise entre 4V et 6V. Cette nouvelle contrainte nous amène à choisir la solution (d2) (Fig. 7d).

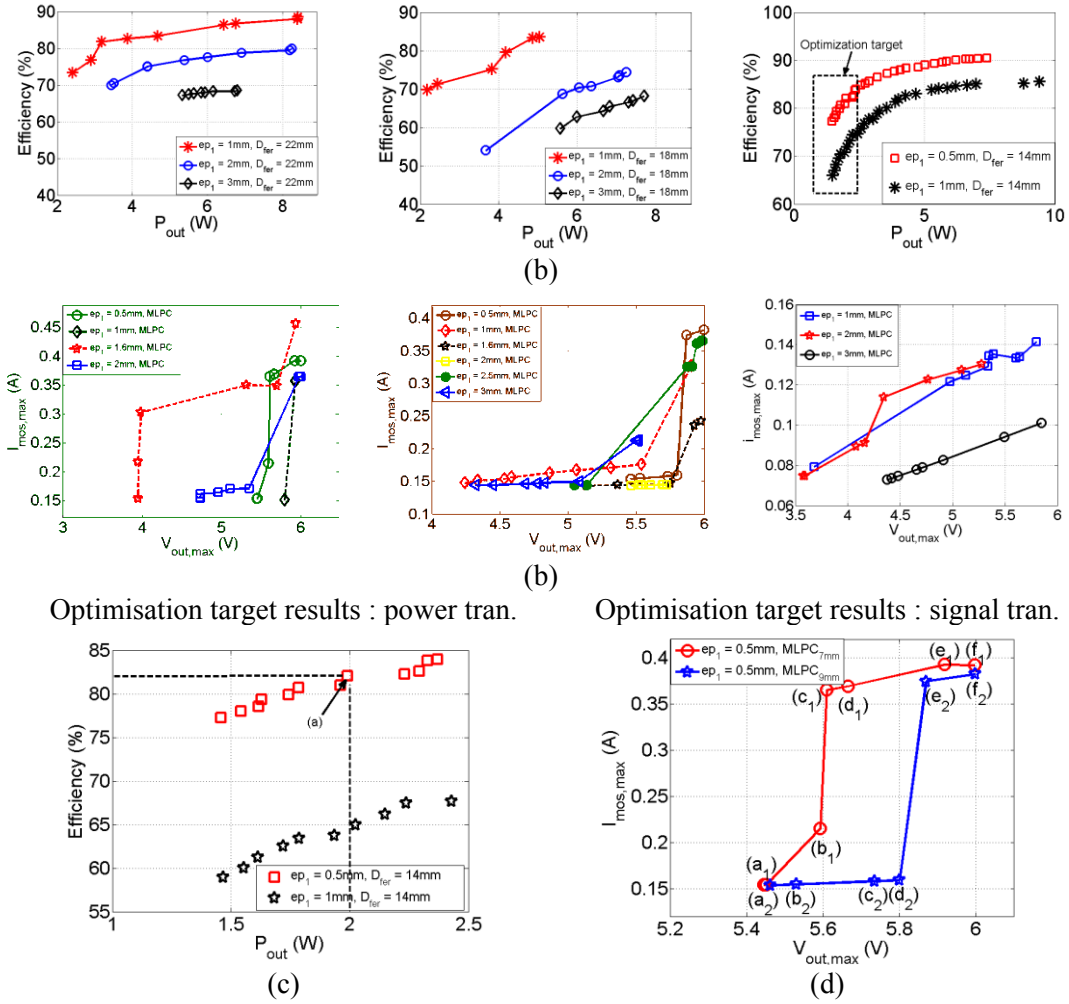
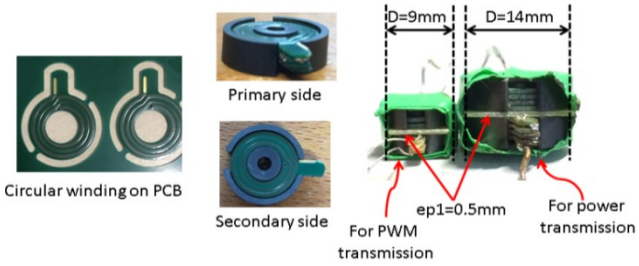


Fig. 7: Résultats d'optimisation des fonctions étudiées

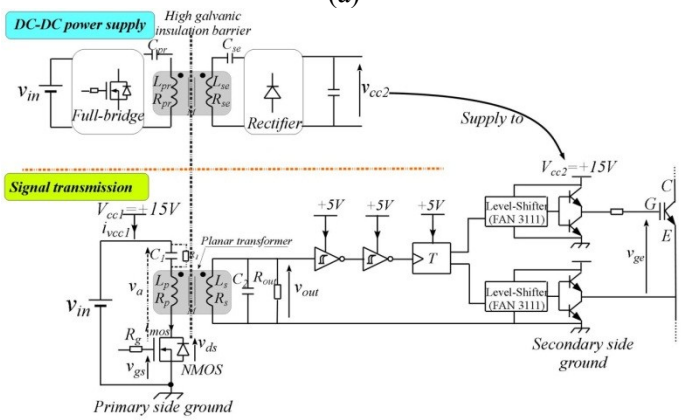
III.4. Validations expérimentales

Afin de valider la démarche de prototypage virtuel, nous avons réalisé un prototype des transformateurs et une carte des fonctions des transmissions et d'attaque de

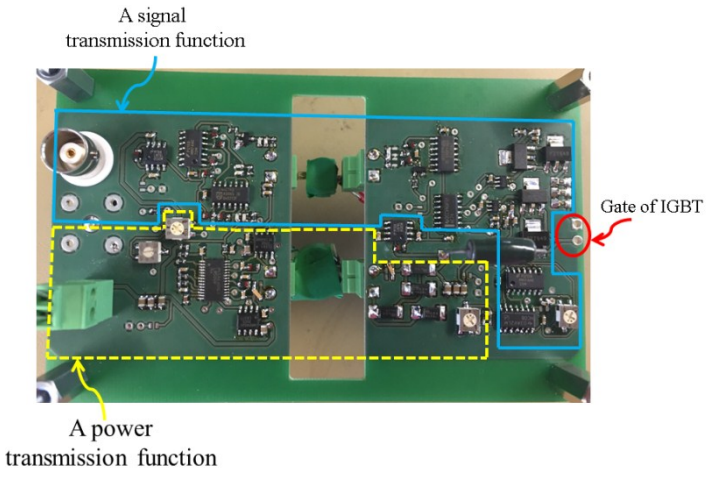
grille. Le schéma est présenté sur la Fig. 8a. Sur la partie “secondaire”, nous avons mis en œuvre le circuit résonant parallèle (C_2 et R_{out}) avec des circuits logiques (Trigger et bascule T) et un circuit intégré de “level-shifter” afin de piloter deux circuits push-pull en technologie bipolaire (FZT849 et FZT949) avec des tensions de 15V. La sortie du driver peut alors piloter des IGBT avec une tension symétrique de +/-15V. Pour finir, afin de proposer des résultats expérimentaux réalistes, nous avons connecté un IGBT 2MBI225VN-120-50 (1200V-225A) en sortie du driver. Sur la Fig. 8b est présentée la carte du prototype.



(a)



(b)



(c)

Fig. 8: Prototype des transformateurs et des fonctions étudiées

Sur la Fig. 9a-b, nous proposons des résultats expérimentaux pour comparer aux résultats de simulation. Nous avons notées que des écarts entre la simulation et l'expérimentation à cause des éléments parasites et des tolérances sur les valeurs des composants. Nous constatons que le driver développé permet bien de piloter la tension grille-émetteur d'un IGBT avec une tension de +/-15V. Nous proposons également de détailler les formes d'ondes lors de l'ouverture et la fermeture de l'IGBT afin de quantifier les temps de propagation. Nous constatons que le temps de propagation est symétrique et qu'il vaut environ 50ns (de V_{ds} du N-MOSFET au V_{ge} de l'IGBT) et environs 140ns pour le début de la carte au primaire à la tension V_{ge} de l'IGBT.

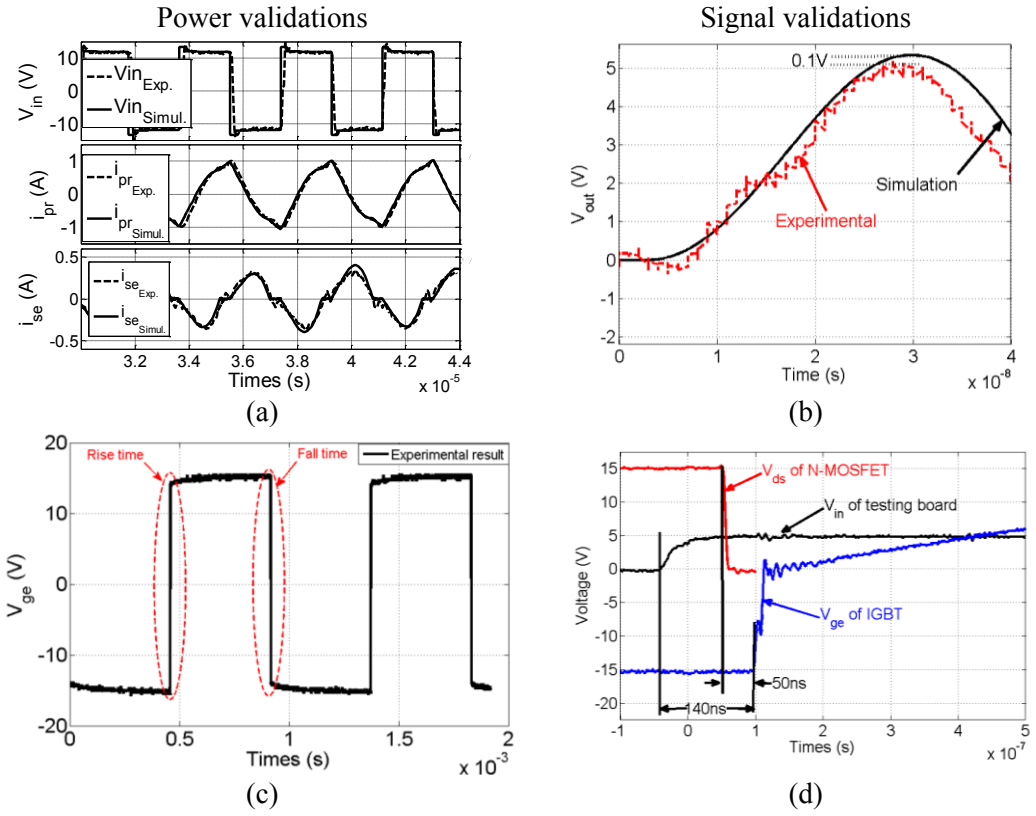


Fig. 9: Résultats expérimentaux d'un driver pour la distance d'isolantion de 0.5mm

IV. Conclusion et perspectives

Dans cette thèse, nous nous focalisons sur la fonction de transmission d'ordres et la fonction de transmission de puissance pour drivers d'IGBT dans un contexte d'une forte tension d'isolation galvanique (jusqu'à 40kV) et plus particulièrement pour les onduleurs de structure multi-niveau de type MMC. Les études sur le matériau isolant et la forme du transformateur sont aussi présentées.

Nous proposons les schémas électriques et une description géométrique d'un transformateur planaire pour répondre à cette problématique. Dans une optique de généricité et d'approche par prototypage virtuel, nous avons développé un outil de dimensionnement basé sur un algorithme génétique qui fait appel à des outils numériques variés (FEMM pour des simulations magnétiques par éléments-finis et LTSpice pour des simulations transitoires rapides).

Les résultats d'optimisation sont analysés succinctement et la prise en compte de contraintes additionnelles nous conduisent à faire un choix de solutions sur les différents fronts de Pareto proposés. La phase de prototypage physique et les résultats expérimentaux sont comparés avec les résultats de simulation pour bien valider notre démarche.

Les nombreuses perspectives sont résumées ci-dessus :

- Etude sur le transformateur pour la tenue en tension : problèmes des points triples des matériaux, claquage électriques, …
- Commande rapprochée intelligente : mesurer la tension de condensateur de chaque SM-MMC, …
- Packaging 3D-MMC : possibilités d'intégrer les composants du driver dans le packaging 3D (voir Fig. 10), …

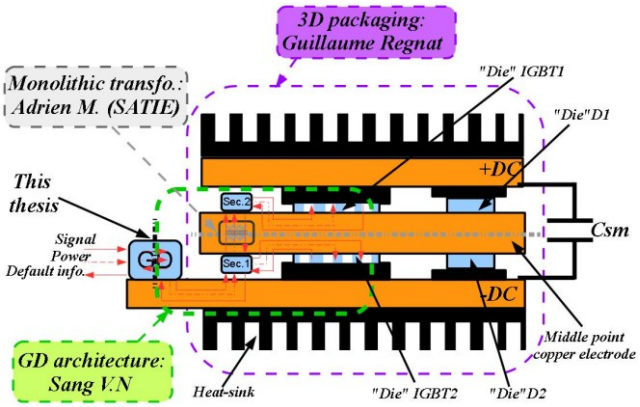


Fig. 10: Packaging 3D pour un SM-MMC

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