Electrical characterization of advanced field-effect transistors : junctionless transistors, carbon nanotubes, and tin dioxide nanowires

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Dissertation for the Degree of Doctor of Philosophy

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Presented by

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August 2014

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Dissertation for the degree of Doctor of Philosophy

Under co-supervision between Korea University (Seoul, South Korea) and Grenoble INP (Grenoble, France)

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Junctionless transistors, carbon nanotube networks, and tin dioxide nanowires

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Content

English Abstract

Low-dimensional nanostructure materials such as carbon nanotubes (CNTs), metal-oxide nanowires, graphene, and molybdenum disulfide (MoS_2) have been intensively investigated as a next electronic candidate to replace complementary metal-oxide-semiconductor (CMOS) devices owing to their high on and off current ratio, field-effect mobility, and electrical conductivity. Two representative approaches have been used, namely, top-down and bottom-up technologies. The former method has been generally used in a commercial company for silicon based mass production since it is extremely well controlled by costly lithography instruments. While the latter one is cost-effective but much difficult to modulate their physical/chemical properties owing to their large sample-to-sample variations. Recently, a hybrid bottom-up/top-down technology with crossbar/CMOS structures for nano-scale memory and three-dimensional (3D) multifunctional nano-electronics were introduced as well, since it provides advantages of ultra high bit scale-density and array-based circuit level integration. To be realized aforementioned concepts for practical applications, a proper device characterization based on device physics should be required. In this dissertation, static and low-frequency noise characteristics of low-dimensional advanced field-effect transistors (FETs), which are independently fabricated by top-down and bottom-up technology, are investigated in terms of different channel materials and device dimensions and structures.

At the beginning of this thesis, the trend of recent CMOS technology to overcome the short channel effects (SCEs) is introduced in terms of strain silicon channel engineering, silicon on insulator (SOI) technique, multi-gate structure, high-κ and metal gate engineering, alternative channel materials and beyond CMOS approaches.

In chapters 2 and 3, various electrical parameter extraction techniques for low-dimensional FETs to evaluate device performances such as split capacitance-to-voltage (CV) technique, Y-function method (YFM), and Maserjian's function including a numerical percolation simulation are introduced. The core carrier transport mechanism that dominates operation here is the field-effect control of 1-dimensional (1D) silicon-channel/nanowire, 2D silicon-channel/nanosheets, and quasi 2D randomly dispersed nanotubes.

The low temperature characteristics of recently developed junctionless transistors (JLTs) will be presented as a possible promising device due to its figure of merits over improved short-channel operation. Based on the principle of device operation of JLTs, two conduction regions can be defined with respect to silicon surface voltage, partially depleted region

and surface accumulation region. But, as silicon channel width is shrunk until quasi-1D nanowire shape, the threshold voltage (V_{th}) and flat-band voltage (V_{FB}) are merged together at room temperature. To properly evaluate electrical parameters in such a low-dimensional silicon based device, this dissertation firstly dealt with low temperature behavior of V_{th} and V_{FB} from quasi 2D planar to 1D nanowire devices. By employing split CV technique at room temperature and dual-gate coupling at low-temperature measurements, various devices parameters, temperature and gate bias characteristics can be studied such as the temperature dependency of V_{FB} and V_{th}, the gate oxide capacitance per unit area (C_{ox}), and the doping concentration N_D, respectively. With account for the position of V_{FB} and their charge based analytical model of JLTs, bulk mobility (μ_B) and low-field mobility in accumulation region (μ_{0_acc}) were separately extracted, respectively. The mobility limitation factors concerning the degradation of μ_B and μ_{0_acc} with gate length in planar and nanowire JLTs have been studied.

1D metal-oxide nanowires (NWs) such as SnO_2, ZnO and CuO materials have been widely studied because of their unique properties such as high surface-to-volume ratio, large aspect ratio, and carrier quantizing effects for electronic applications. Especially, SnO_2 NW-FETs have been suggested as excellent candidates for high performance flexible and transparent NW transistors with low-temperature fabrication process. To improve the reliability of device performance, a post passivation process was suggested with the aim of reducing interface trap density and keeping adsorbents off the surface of metal-oxide NWs. To account for electrostatic coupling through the PMMA passivation layer, an analytical simulation to get the effective gate capacitance has been performed and compared to 1D cylindrical capacitance model (C_{1D}). Channel access resistance (R_{sd}) effects on carrier mobility (μ) and low-frequency noise (LFN) characteristics also described.

The most widely spread device configuration relies on the random network since it is very easy to fabricate with low cost. However, for instance, the effective carrier number is not always to be known since it is easily has been influenced by oxygen molecules, humidity, and light so on. For this reason, proper electrical evaluation techniques have been needed. Static and LFN characterizations in quasi 2D N-type random network thin film transistors (RN-TFTs) based on single-walled CNTs have been presented. For the electrical parameter extraction, YFM was used to suppress R_{sd} influence. The gate-to-channel capacitance (C_{gc}) was obtained by split CV method and compared to 2D metal-plate capacitance model (C_{2D}). In addition, to account for the percolation-dominated quasi-2D RN-TFTs, a numerical percolation simulation was performed with Floyd's algorithm. LFN measurements were also carried out and the results were well interpreted by CNF and correlated mobility fluctuation model (CNF-CMF). Finally, C_{1D} was suggested and applied to provide better consistency between all electrical parameters

based on experimental and simulation results.

Thermoelectric power (TEP) of 2D single-walled CNTs (SWCNTs) thin film networks has been investigated. In particular, SWCNT thin films are considered as attractive candidates to replace traditional transparent conducting oxides (TCOs) such as In_2O_3:Sn, SnO_2:F, or ZnO:Al due to their low cost fabrication, flexibility, non-toxicity. To realize the potential of SWCNT networks as a thermoelectric power generator, a fundamental understanding of the inherent electrical and thermal transport properties is crucial. TEP, precisely tuned ratios of metallic (m-SWCNTs) and semiconducting (s-SWCNTs) in the network has been presented. To qualitatively analysis this, a theoretical model for TEP calculation with account for a junction effect between SWCNTs are introduced and compared with experimental results in a mixed SWCNT networks.

Keywords: Junctionless transistors (JLTs), Carbon nanotubes network, Carrier transport, Low-frequency noise, Numerical simulation, Low-temperature measurement, Percolation effect

1. Introduction

1.1 Overview of Semiconductor Industry

1.2 CMOS Scaling Issues and Short Channel Effect

1.3 Advanced MOSFET technology

1.4 Conclusion and Dissertation Outline

Chapter 1 Abstract

In this introductory chapter, the trend of semiconductor industry is briefly described. With current CMOS (Complementary metal-oxide-semiconductor) scaling issues and various "Short Channel Effects (SCEs)" phenomenon, usually observed in two-dimensional (2D) potential distribution of short channel length, such as hot carrier generation, drain-induced barrier lowering (DIBL), and punch-through etc are discussed in detail. Besides, advanced MOSFET (Metal-Oxide-Semiconductor Field-Effect transistor) technologies and alternative approaches to overcome such SCEs are introduced. At the end, chapter summary and dissertation scopes are presented.

1.1 Overview of Semiconductor Industry

After the first demonstrations of "Bipolar-Junction-Transistor (BJT)" developed by W. Shockley, J. Bardeen, and W. Brattain in 1947 and "Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)" realized by Labate, Kahng and Atalla at Bell Labs by in 1960s,[1-5] a silicon based transistor is dramatically developed as a fundamental building block of integrated circuits (ICs) up to a few tens of nanometer scale device.[4, 6, 7]

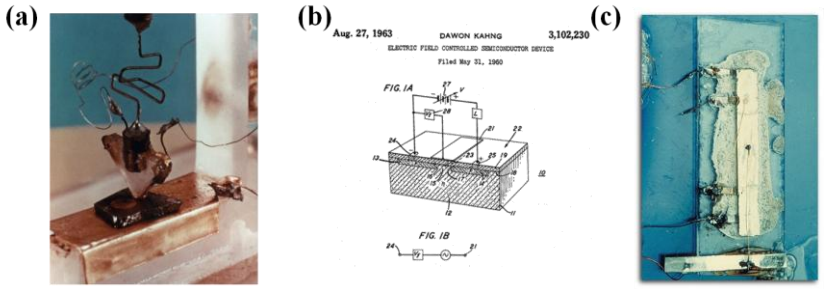

Figure 1-1 Photographs of the firstly developed (a) BJT (in 1947), (b) MOSFET (in 1960), and (c) IC (in 1961), respectively.

Besides, the market demands for high memory density and versatile functionality of ICs are also rapidly increased after the realization of personal computer, smart applications such as iOS and Android based smart phone, a high resolution digital camera, and Nintendo Wii etc. To satisfy these needs, the semiconductor technology has been focused on scaling down its size to follow "Moore's law" reported in 1975, which predicted that the number of transistors on a chip would double about every two years.[8] This scaling down trend has been successfully continued up to 22nm technology referring to ITRS report as seen in Fig 1-2, and recently Intel manufactured a processor containing 1.4 billion transistors in 160mm^2 area as displayed in Fig. 1-3.

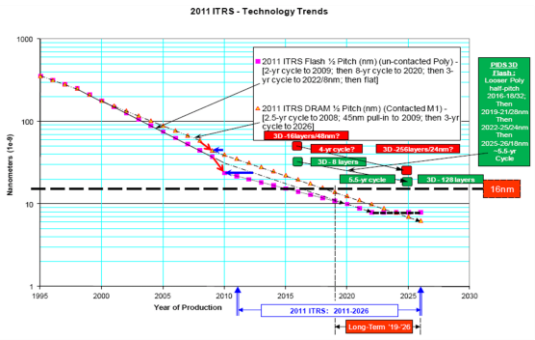

Figure 1-2 2011 International Technology Roadmap of Semiconductors (ITRS)-Dynamic Random Access memory (DRAM) and Flash memory half pitch trends. [http://www.itrs.net/]

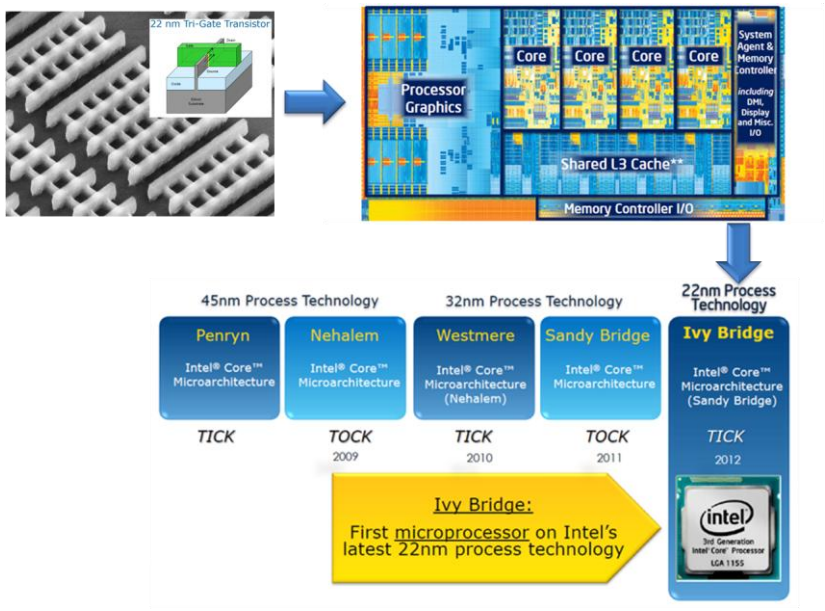

Figure 1-3 Intel's 22nm technology for FinFET structure and Intel core i7-3770K (22nm Ivy Bridge) [http://newsroom.intel.com/docs/DOC-2032]

As the device size is shrunk, it enables to drive many advantages such as increasing an integration density in a chip, enhancing a switching speed, increasing a frequency of amplifier, a lowing power consumption and cost per wafer. Especially, the switching speed enhancement is very important performance in digital and information era. This can be achieved by reduced geometrical effects arisen from the mainly reduction of the gate oxide capacitance ($C_{ox}=\varepsilon_0\varepsilon_r LW/t_{ox}$, where t_{ox} is the oxide thickness, L is the gate length, W is the gate width, and ε_0 and ε_r are the vacuum and the relative permittivity, respectively) by the factor of the scaling ratio, since the circuit RC delay (τ) is directly proportional to on-current ($\tau=C_{ox}V_{DD}/I_{on}$, V_{DD} is the supplying voltage, and I_{on} is the operating current when the gate-to-source voltage (V_{gs}) is equal to V_{DD}). [4, 9, 10] Details of the constant field scaling rule will be discussed in next section.

1.2 CMOS Scaling Issues and Short Channel Effect

The most ideal strategy of MOSFET miniaturization is simply scaled down of all geometrical parameters and drive voltage to sustain the same internal electric field in the channel as in the long channel device to avoid short channel effects (SCEs).[9, 11] For instance, as illustrated in Fig. 1-4, to keep the constant value of vertical an lateral electric field, V_{DD} and various device geometrical factors (W, L, and x_j) have to be reduced with the scaling factor (κ), whereas N_A should be more heavily doped by factor of κ to reduce W_{Dep} to block the punch-through phenomenon.[9, 11] However, this higher doping concentration again leads to threshold voltage raise (V_{th}, see details in Ch.2.2.2.1). Therefore, in order to maintain V_{th} range, t_{ox} must be thin-

ner by the factor of κ to increase the gate controllability. With account for these facts, it can be concluded that all MOSFET parameters are closely interrelated with the scaling factor as summarized in Table 1-1.

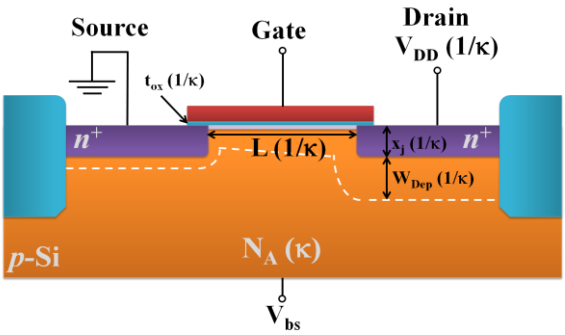

Figure 1-4 Illustration of scaling parameter of MOSFET.

	MOSFET Device/Chip Parameter	Scaling Factor, Constant E-Field
Scaling Parameter	Device Dimension (t_{ox}, L, W, x_j)	1/κ
	Substrate Doping Concentration (N_A/N_D)	κ
	Supply Voltage (V_{DD})	1/κ
Derived Device Parameters	Electric Field (E)	1
	Depletion-Layer Width (W_{Dep})	1/κ
	Gate Oxide Capacitance ($C_{ox}=\varepsilon_0\varepsilon_r A/t_{ox}$)	1/κ
	On Current (I_{on})	1/κ
	Intrinsic Delay Time (τ)	1/κ
	Power Dissipation ($P=V_{DD}\times I_{on}$)	$1/\kappa^2$
Derived Chip Parameter	Transistor Density ($\propto 1/WL$)	κ^2
	Power Density/Area Power Consumption (P/WL)	1
	Clock/Operating Frequency ($I_{on}/C_{ox}V_{DD}$)	κ

Table 1-1 MOSFET scaling parameter derived from constant field scaling. [9, 11]

Device scaling has been successfully followed by constant-field scaling law with κ factor until 2003. However, with decrease of device physical size up to sub tens of nanometer scale, the density and complexity of the integrated circuit (IC) are dramatically increased, and it causes undesired degraded effects, so generally called SCEs, where the gate field no longer has the electrostatic controllability of the channel to turn it off due to the enhanced latter field, eventually leading to the high leakage current and the large power consumption in "stand-by off" state.

Many SCEs have been reported such as drain-induced barrier lowering (**DIBL**),

punch-through, **mobility reduction by gate-induced surface field**, **velocity saturation**, **impact ionization near drain region**, **and hot-carrier injection** etc depending on different physical origins.[9, 12]

1. **Punch through** can be occurred when the sum of junction width of drain (x_{jd}) and source (x_{js}) is merged together, *i.e.*, $x_{jd}+x_{js}\approx L$.[13] In long channel MOSFET that shows usually $x_{jd}+x_{js}\ll L$, the current can only flow provided that the inversion channel is sufficiently formed by V_{gs}. However, as the length of device becomes shorten, the driving current is not depending on V_{gs} but mainly the drain voltage V_D. To minimize this, thinner t_{ox} to enhance the gate controllability, high substrate doping to reduce depletion width, and shallow junction between such as lightly doped drain (LDD) is used. Likewise, **DIBL** is closely related with potential barrier, so called built-in potential at the source and drain interface with channel (p-n junction). Since V_D the strong latter field in short channel MOSFET enables to deplete some portion of the channel, the junction barrier between drain and channel can be lowered, eventually MOSFET can flow the current in advance even before $V_{gs}<V_{th}$.

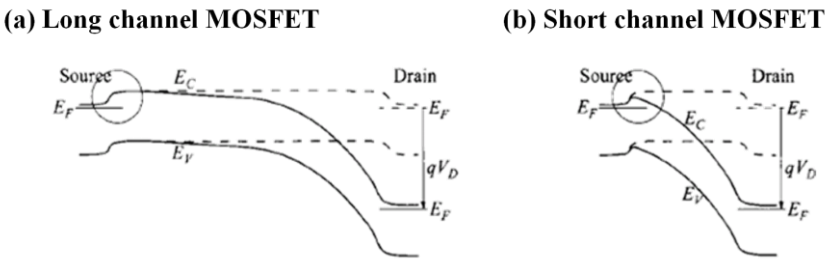

Figure 1-5 Energy-band diagrams at the semiconducting surface from source to drain, for (a) long and (b) short channel MOSFET, respectively.[9]

2. **Mobility reduction by gate-induced surface field** is usually observed in short channel device with thin oxide layer. Since the carrier has to transport into the very thin and confined inversion layer underneath the gate dielectrics with high perpendicular field to the channel, the scattering caused by surface roughness arisen from high gate field can be induced the reduction of the mobility. It is therefore evidently dependent on V_{gs}.[9, 10]

3. **Velocity saturation** is usually observed when the carrier drift velocity (v_d) is saturated up to its maximum drift velocity (v_{dsat}) due to the high electric field to the channel. In fact, the drift velocity ($v_d=\mu E$, where E and μ are the electric field and carrier mobility, respectively) is linearly proportional to E with constant μ below

E_c (E_c is the critical electric field with a value of $\approx 10^4$V/cm at 300K) in long channel device since E is low enough. However, the size of length becomes shorter, v_d is deviates from a linear dependence and eventually is saturated when $E>E_c$. Hence, the velocity saturation effect has to be taken into account in short channel MOSFET ($v_d=\mu E/(1+E/E_c)$ for $E<E_c$, $v_d=v_{dsat}\approx 10^7$cm/s for $E>E_c$).[9]

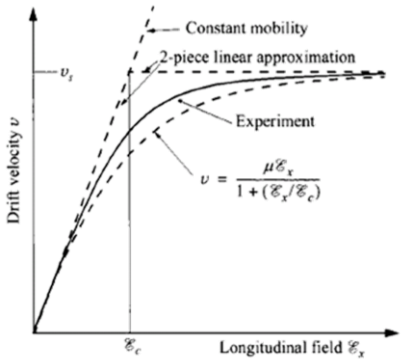

Figure 1-6 Drift velocity (v_d) curves as a function of E for silicon and semiconductor.[9]

4. **Impact ionization near drain region** is occurred especially in N-type MOSFET at the end of pinch off drain region. If electrons have a high kinetic energy in presence of high drain field, it would be accelerated with high gate field and injected into the depletion layer, resulting in generation of electron-hole (e-h) pairs by impact ionization as illustrated in Fig. 1-7. The generated electrons will directly go to drain and add to the current, whereas the majority of generated holes can be moved to substrate and even sources in short channel device. This hole current acts it as a n-p-n bipolar transistor, eventually the substantial leakage current will flow through the substrate.

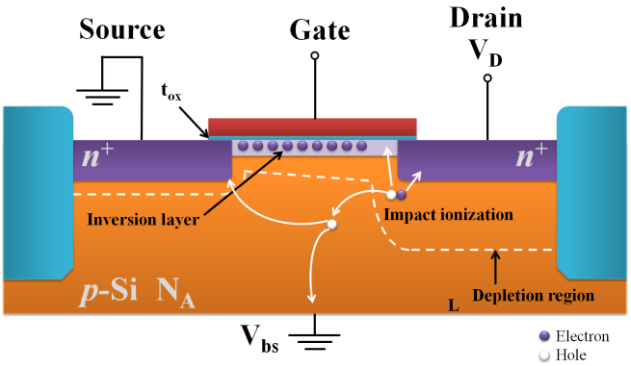

Figure 1-7 Illustration of impact ionization near drain region in N-type MOSFET.

5. **Hot-carrier injection** can be seriously affecting on the reliability of MOSFET. It

happens when the electrons in the channel gain a sufficient kinetic energy in presence of high gate field enough to overcome a silicon-silicon oxide barrier (3.1eV), and they can generate oxide trap charges in dielectric, giving rise to a gate leakage current and trap sites. It will eventually degraded the device performance by increasing V_{th} and impact adversely the gate controllability on the drain current

Finally, various SCEs are introduced. However, in order to sustain the continuation of Moore's law and even more than Moore, many new technologies have been introduced by many researchers such as adopting strained silicon to reduce the effective mass of carriers, thicker high-κ dielectric materials in conjunction with metal gate to shrink the leakage current, and multi-gate structure to have optimum gate controllability to improve device performance and to minimized SCEs. Actually, this trend can be ultimately faced with physical limitations. However, it will be continuing up to the quantum mechanics governed atomic scale by employing alternative break through approaches. In the next sections, advanced MOSFET technologies will be presented to overcome such aforementioned SCEs.

1.3 Advanced MOSFET technology

The physical scaling limitation is almost reached, and particularly the scaling down of t_{ox} will be already interfered by quantum mechanical effects such as tunneling and dark space existence.[6, 7, 9] Furthermore, the fabrication optimization in such extremely small geometrical volume is challenging as well since the tiny statistical deviation arisen from the device process will lead to the serious performance variability even though it associates with few atoms in the channel.[14] To overcome SCEs and sustain continuing scaling trend, many new concept devices and optimized fabrication technologies have been suggested as seen in Fig. 1-8. such as silicon on insulator (SOI), multi-gate structure, tunneling FET, channel doping engineering, source/drain engineering, high-κ dielectric stack engineering, 3-dimensional (3D) structure, channel strain engineering, and alternative channel material such as III-V (for N-type) and Ge (for P-type).[7, 9, 15]

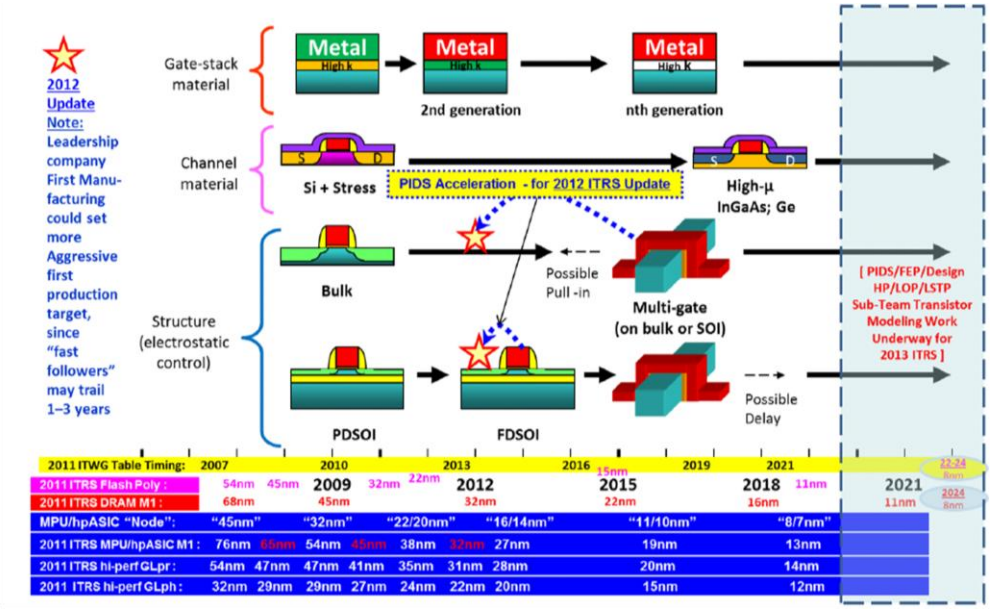

Figure 1-8 2012 ITRS "Equivalent Scaling" process technologies timing Overall Roadmap Technology Characteristics (ORTC) microprocessor unit (MPU)/High-performance ASIC half pitch and gated length trends and timing, and industry "Nodes". [http://www.itrs.net/]

1. **Strained Silicon** in n-type MOSFETs were successfully demonstrated at L<70nm in 2001 to improve the speed of CMOS technology.[16, 17] This can be achieved by placement silicon germanium layer with a lager lattice constant under the active silicon channel as a substrate layer as seen in Fig. 1-9.[16, 18] It induces strain effect in the channel and reduces phonon scattering giving rise to mobility enhancement by modifying the band structure. Especially, the hole mobility also can be improved by increasing fraction of germanium.

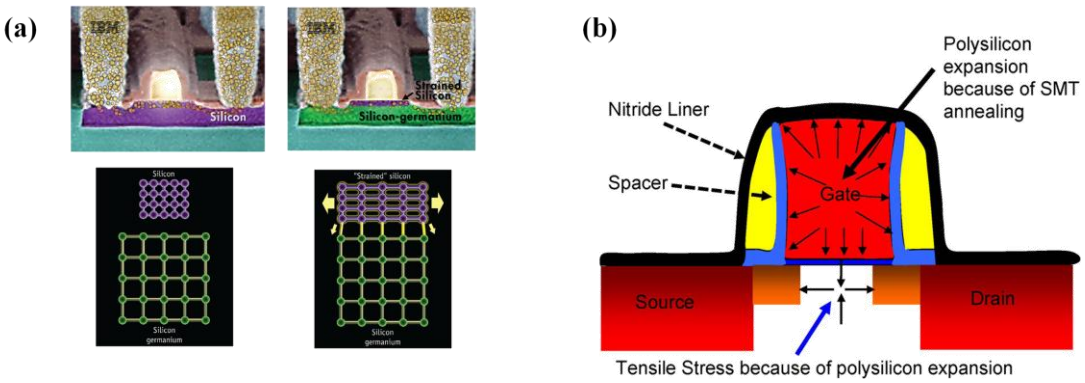

Figure 1-9 Illustration of (a) straining of silicon by means of silicon germanium and (b) mechanism of gate stress memorization technique [17, 18]

2. **Silicon on insulator (SOI)** structure can completely separate a ultrathin film of single crystalline silicon and the bulk substrate by using "Smart Cut" process as shown in Fig. 1-10.[19] It enables to suppress the impact of ionizing radiation ef-

fects by a buried oxide layer, large power consumption arisen from parasitic and leakage currents, and various SCEs by successfully eliminating punch-through possibility. These fact results in performance improvements in terms of speed, but some issues are still remained to be solved since there are self-heating problem, floating body effect, and high fabrication cost per wafer *etc*.[18, 19]

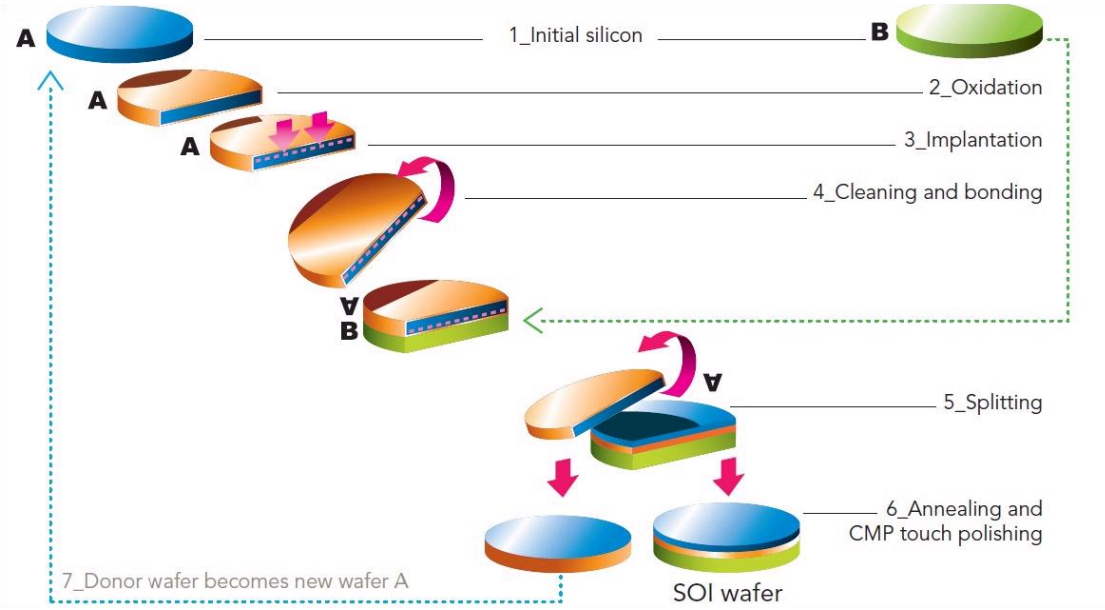

Figure 1-10 Fabrication process of manufacturing ultrathin SOI via Smart Cut process [http://www.soitec.com/en/technologies/smart-cut/]

3. **Multi-gate structure** (double, triple, quadruple, and gate all around structure) has been considering as a further promising candidate to have the larger immunity for SCEs compared to classical single planar gate devices as presented in Fig. 1-11. It enables to provide several advantages such as enhanced gate controllability, increased gate-drive current, reduced subthreshold swing and subsequently suppressed gate leakage current, reinforced pinch off effects, and improved process reliability.[9, 17, 18] Consequently, it gives rise to relaxed channel doping concentration and vertical field to the channel resulting in improved performance and process variability in terms of better mobility and random dopant fluctuation, respectively. However, there are technological and economical challenges to be employed in practical applications such as V_{th} modulation and parasitic capacitance arisen from weak body effect and increased layout density. The fabrication cost and process complexity are also challenging to have a compatibility with conventional bulk planar CMOS devices.

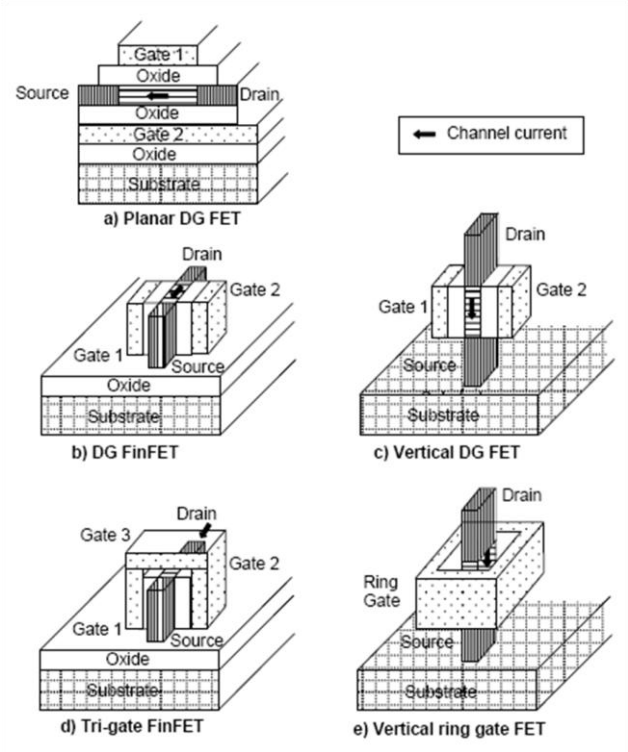

Figure 1-11 Several types of multi-gate MOSFETs structure.[17]

4. **High-κ and metal gate** stack such as hafnium oxide (HfO_2**)** and zirconium oxide (ZrO_2) *etc* as summarized in Fig. 1-12 has been successfully introduced at 45nm node to suppress the rapidly increased gate tunneling current arisen from very thin t_{ox} (less than ≈1nm).[20] Theoretically, it can be achieved by simple capacitance relationship as shown in below expression by ignoring side effects such as leakage current and reliability,

$$\frac{t_{ox}}{\kappa_{ox}} = \frac{t_{high-\kappa}}{\kappa_{high-\kappa}} \quad \text{or simply,} \quad t_{high-\kappa} = \frac{\kappa_{high-\kappa}}{\kappa_{ox}(\approx 3.9)} t_{ox} \qquad (1\text{-}1),$$

where κ_{ox} and t_{ox} (equivalent oxide thickness) are the dielectric constant and thickness of silicon oxide respectively, and $\kappa_{high\text{-}\kappa}$ and $t_{high\text{-}\kappa}$ are that of high-κ materials.[21] It allows to have a thicker dielectric thickness to reduce leakage current while ensuring the same gate controllability. At the same time, in order to circumvent mobility degradation induced by remote Coulomb scattering at the interface and V_{th} pinning, the band-edge work-function metal has to be used as a gate electrode. In addition, the polysilicon depletion effects can be removed by metal gate.[20] However, it contains a high level of interface traps and impurities and thus posing significant performance degradation which should be solved for RF applications.

(a)

Material	Dielectric constant (κ)	Band gap E_G (eV)	ΔE_C (eV) to Si	Crystal structure(s)
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Al_2O_3	9	8.7	2.8[a]	Amorphous
Y_2O_3	15	5.6	2.3[a]	Cubic
La_2O_3	30	4.3	2.3[a]	Hexagonal, cubic
Ta_2O_5	26	4.5	1–1.5	Orthorhombic
TiO_2	80	3.5	1.2	Tetrag.[c] (rutile, anatase)
HfO_2	25	5.7	1.5[a]	Mono.[b], tetrag.[c], cubic
ZrO_2	25	7.8	1.4[a]	Mono.[b], tetrag.[c], cubic

[a]Calculated by Robertson (See Ref. 153).
[b]Mono.=monoclinic.
[c]Tetrag.=tetragonal.

(b)

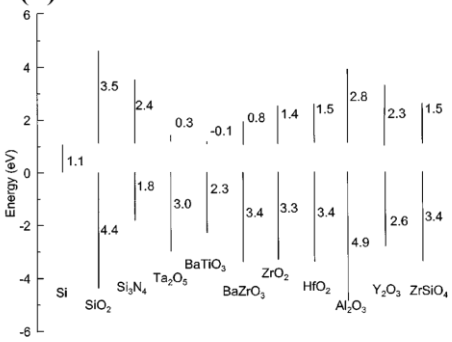

Figure 1-12 (a) Comparison table of relevant properties of potential candidates of high-κ dielectric materials and (b) corresponding band offset calculation result.[21]

5. **Alternative channel material** with high carrier mobility and low effective mass such as III-V semiconductor, GaAs, InP, InGaAs and InAs for n-type and Ge for p-type has been considered as a potential solution to overcome current scaling issues.[22, 23] Especially, combination of III-V (for n-type)/Ge (for p-type) on silicon has been suggested as an ultimate CMOS structure in order to utilize silicon based CMOS platform as presented in Fig. 1-13(a). However, as depicted in Fig 1-13(b), several constrain issues has to be solved to have a compatibility with conventional CMOS technology: (1) high crystalline quality of III-V/Ge MOS on a large size of silicon wafer (2) gate insulator engineering with superior interface quality (3) low channel access resistance (4) total COMS integration (5) ultra thin body Ge/ III-V channels to suppress SCEs.[23, 24]

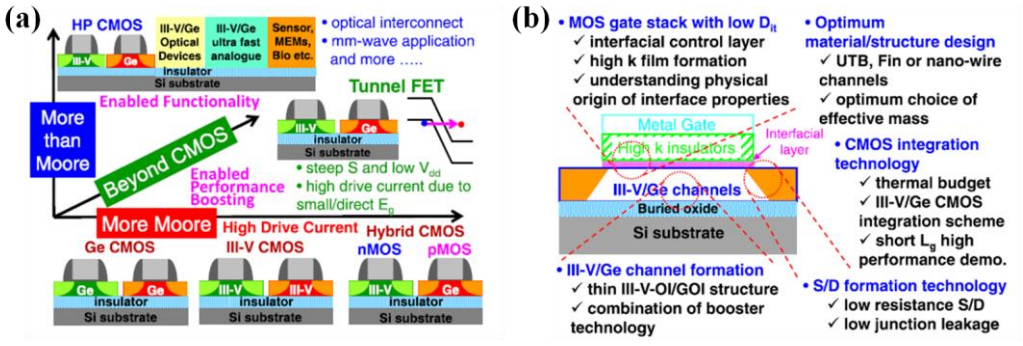

Figure 1-13 (a) Comparison of relevant properties of potential candidates of high-κ dielectric materials and (b) corresponding band offset calculation result.[23]

6. **Beyond CMOS approaches** by using carbon based materials (graphene and carbon nanotubes (CNTs)), semiconducting nanowires, and topological insulators have been widely studied and steadily invested as a possible alternative active channel.[17, 25-32] Even though there are many obstacles to be manufactured for

industrial markets, it still has many interesting properties and even shows superior performances in some points as presented in Fig 1-14.

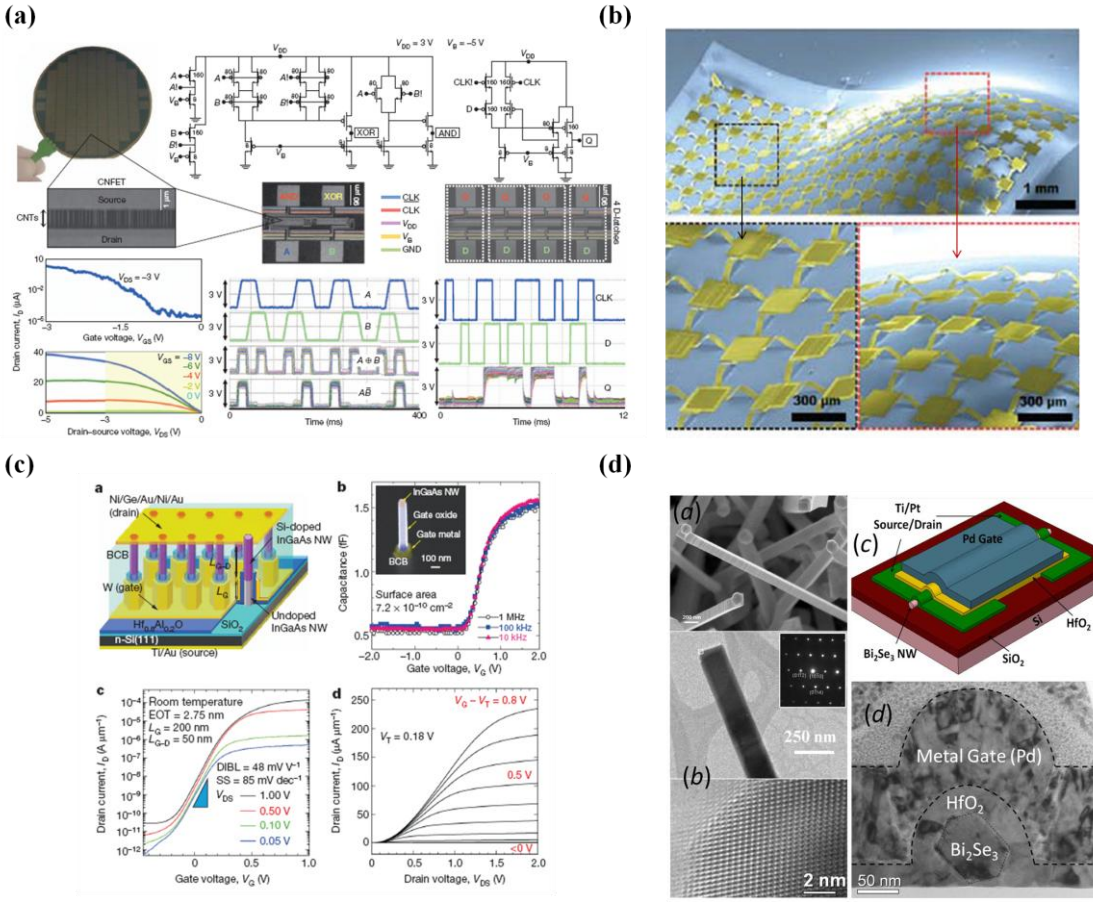

Figure 1-14 (a) Characteristics of CNT-FET subcomponents operating circuit for CNT computer[26] (b) Stretchable logic inverters based on SnO_2 semiconducting nanowires[27] (c) A III–V nanowire channel on silicon for high-performance vertical transistors[30] (d) Topological insulator Bi_2Se_3 nanowire for high performance FETs[32].

To satisfy increased market demands like ultra low power consumption with high device performance with versatile functionality, many efforts have been made and some of them are described in this section in terms of strain channel engineering, SOI technique, multi-gate structure, high-κ and metal gate engineering, alternative channel materials and beyond CMOS approaches. Despite of many hindrances to achieve it, the continuation of scaling trend will eventually keep going via break through techniques.

1.4 Conclusion and Dissertation Outline

The current trend of semiconductor industry and classical constant-field scaling rule are briefly introduced. According to Moore's law, scaling has been successfully applied and drives many advantages. However, it has become more challenging when the device size is shrunk up

to sub tens of nanometer scale, and diverse SCEs were reported. In this chapter, various SCEs phenomenon and the advanced approaches are presented and summarized.

In this dissertation, various electrical characteristics based on I-V, C-V, low frequency noise (LFN), and low temperature environment including numerical simulation for top-down and bottom-up devices are investigated, respectively. As a possible emerging candidate for '*Beyond CMOS*' and '*more than Moore*', heavily doped junctionless transistors (JLTs) are studied and the results are compared to bottom-up nanoscaled devices such as quasi-1D tin-oxide (SnO_2) nanowire FETs and -2D single-walled carbon nanotube (SWCNT) random network thin film transistors. These are not only focusing on the reduction of SCEs but also the replacement of silicon based rigid channel material which could be compatible with other substrates than silicon (flexible substrates) or which could be integrated for low cost addition of new functions in the back-end of line of CMOS.

Chapter 1 introduces the trend of semiconductor industry with current CMOS scaling issues arisen from SCEs and various advanced MOSFET technologies to overcome SCEs.

Chapters 2 and 3 are dealing with the relevant theoretical and technical background for further investigation of this dissertation.

Chapter 2 demonstrates various electrical parameter extraction methodologies based on the fundamental long channel inversion mode N-type MOSFET to provide theoretical and experimental backgrounds for electrical characterization in diverse types of semiconductors in terms of I-V, C-V, and low frequency noise (LFN).

Chapter 3 describes a numerical percolation simulation methodology based on modified Floyd's algorism in two-dimensional (2D) conducting nanowire random network. To account for the linear and non-linear behaviors of a complex 2D random network, a hybrid methodology with SPICE simulator is also presented.

Chapters from 4 to 6 are analyzing various electrical properties in diverse low-dimensional transistors such as JLTs, quasi-1D tin-oxide nanowire (SnO_2-NW) FET, and quasi-2D N-type CNT network, respectively.

Chapter 4 discusses about the low-temperature characteristics (77K~350K) of flat-band (V_{FB}) and low-field mobility (μ_0) of JLTs. Back gate coupling effect on static and LFN also systematically described.

Chapter 5 presents channel access resistance (R_{sd}) effects on mobility and LFN charac-

teristics in a polymethyl methacrylate (PMMA) passivated quasi-1D SnO_2-NW FET.

Chapter 6 covers static and LFN characterizations in quasi-2D N-type random network thin film transistors based on SWCNTs.

Chapter 7 investigates effect of inter-tube junctions on the thermoelectric power (TEP) of mono-dispersed SWCNTs.

Finally, **Chapter 8** concludes all results and discussions in this work.

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2. Electrical characterization of MOSFET

Chapter 2 Abstract

In this chapter, theoretical backgrounds for electrical characterization are described based on the fundamental long channel MOS transistor model. In addition, various electrical parameter extraction methodologies are presented for threshold voltage, low-field mobility, and series resistance etc. Especially, Y function method (YFM) is discussed in detail to exclude the series resistance effect, since it is simple, powerful and provides physically meaningful parameters. Besides, the split capacitance-to-voltage technique based characterization methods are presented here to evaluate intrinsic channel properties such as an effective oxide capacitance (C_{ox}), a channel doping concentration (N_D for N-type or N_A for P-type) and flat band voltage (V_{FB}). Furthermore, to investigate the quality of device interface and the limitation of device performance, low frequency noise (LFN) theoretical models are introduced.

2.1 Introduction

Since metal-oxide-semiconductor field-effect-transistors (MOSFETs) were realized in 1960s,[1-4] it is dramatically developed as a fundamental building block up to nano-scaled device for the digitalization and information technology era.[4-6] Perhaps, this is nearly interacted with our life as a basic unit of integrated chip (IC), for example, personal computer, smart phone, medical instruments, radio frequency (RF) device, power applications, and all electronic devices. It has many advantages as a basic component in a digital and analog circuit such as simple device structure, low-cost of fabrication, the capability of high speed and integration density.[6] (refer to below Intel's transistor roadmap) However, as the size of device is miniaturized, a proper definition of physical device model and a well-matched parameter extraction methodology are required to provide feedback for a device optimization. Although, employing physically sounded and robust device model is more preferable to have a right insight of device characterization, the long channel MOSFET model (SPICE level 1 model) is used for general parameter extraction to avoid a high risk arisen from heavy fitting procedures in here.[7]

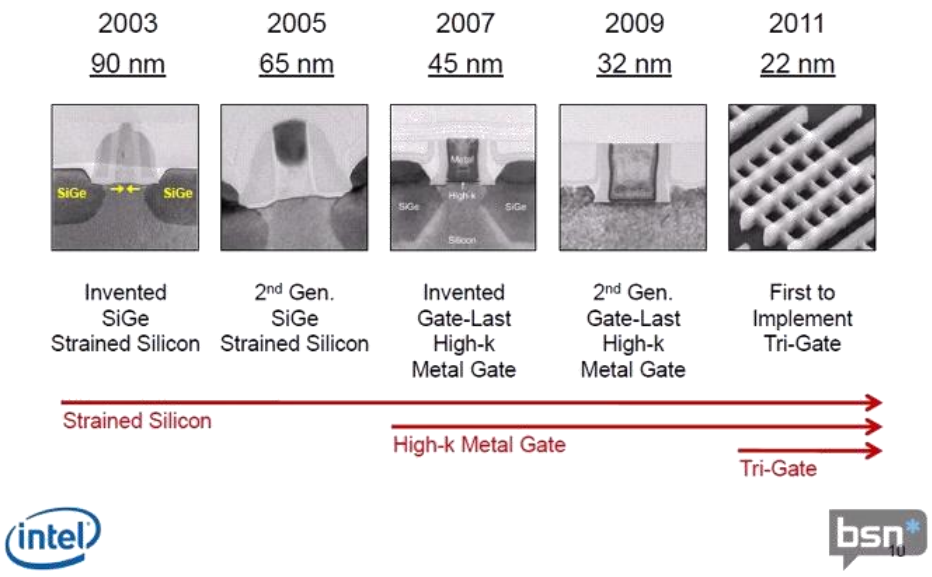

Figure 2-1 Intel's Transistor Leadership over generations: 90nm, 65nm, 45nm, 32nm and 22nm. Three major inventions: SiGe, HKMG (High-κ metal gate) and Tri-Gate structure. [http://www.intel.com, http:// www.brightsideofnews.com]

In this chapter, first the drain current (I_{ds}) will be described depending on the operation regime based on the fundamental MOSFETs operation principle, namely SPICE level 1 model. In addition, though many diverse approaches have been made to extract various electrical parameters such as low-field mobility (μ_0), threshold voltage (V_{th}), and series resistance (R_{sd}), details of Y function method (YFM)[8] will be introduced since it is simple but powerful and

even applicable to not only silicon based device but also one-dimensional (1D) nanowire device,[9, 10] carbon nanotube random networks,[11] organic FET (OFET)[12] without R_{sd} influence. Besides, in order to account for the enhanced transverse field and surface roughness scattering stemming from very thin oxide (t_{ox}) which perturbs the linearity of YFM, modified YFM is also discussed. In fact, there are several ways to get device information from the capacitance-to-voltage (C-V) measurements. Especially, split C-V technique[7] which composes of gate-to-channel capacitance (C_{gc}), gate-to-bulk capacitance (C_{gb}), and total capacitance ($C_g=C_{gc}+C_{gb}$) is described for extraction of the intrinsic channel properties such as doping concentration (N_D for N-type N_A for P-type),[13] V_{FB},[14] V_{th}, C_{ox},[15], capacitance equivalent thickness (CET),[15] and mask length and width reduction (ΔL_m, ΔW_m)[7] respectively since this is relatively less affected by R_{sd} effect compared to I-V. The effective mobility (μ_{eff}) can be determined as well from the measured number of inversion (or accumulation) charges with I-V results.[7] Moreover, as the device size is shrunk, the effective geometrical portion of interfaces faced on channel has to be dramatically increased, and in particular t_{ox} has to be getting thinner, resulting in high transverse field and enhanced surface roughness scattering effects.[7] Hence, LFN characteristics can provide more meaningful information about the interface quality or reliability between channel surface and dielectric layer such as trap energy, distribution and density.[16-18] Representative low frequency noise models such as Hooge's mobility fluctuation model [HMF],[19, 20] McWhorter's carrier number fluctuation model [CNF],[16] and carrier number and correlated mobility fluctuation model [CNF-CMF][18, 21] will be discussed in detail in this section.

2.2 Basic Operation Principle of MOS-FET

The drain current model equations for long n-channel device can be described as a function of gate voltage (V_{gs}) and drain voltage (V_{ds}) with respect to the source, I_{ds} (SPICE level 1 model):

$$I_{ds}(V_{gs},V_{ds}) = \begin{bmatrix} \frac{W_{eff}}{L_{eff}}\mu_{eff}C_{ox}(V_{gs}-V_{th}-\frac{V_{ds}}{2})V_{ds}, V_{ds} \le V_{gs}-V_{th}\ (triode region) \\ \frac{W_{eff}}{2L_{eff}}\mu_{eff}C_{ox}(V_{gs}-V_{th})^2, V_{ds} \ge V_{gs}-V_{th}\ (saturation region) \end{bmatrix} \quad (2\text{-}1)$$

Here, the ratio between the effective channel width and length W_{eff}/L_{eff} is the channel aspect ratio, C_{ox} ($=\varepsilon_0\varepsilon_r t_{ox}^{-1}$, where ε_0 and ε_r are the vacuum and the relative permittivity, respectively) is the gate oxide capacitance per unit area, μ_{eff} ($=\mu_0/[1+\theta_1 V_{gt}+\theta_2(V_{gt}-\Delta V_{th})^2]$, where μ_0 is low-field mobility, ΔV_{th} is the amount of threshold voltage shift arisen from higher transverse field, θ_1 and θ_2 are mobility attenuation factors closely related with phonon scattering due to enhanced

confinement and lager wave function overlap integrals, and scattering by surface roughness at high transverse field, respectively)[7, 8, 18] is the effective mobility, and V_{th} is the charge threshold voltage. In this model, the triode and saturation region can be determined by the over drive voltage, $V_{gt}=V_{gs}-V_{th}$ regime. In fact, higher level of SPICE model surely includes more complex parameters which correlated with V_{gs} and V_{ds}, but this the simplest model Eq. (2-1) still provides essential features of I_{ds}.[5-7]

2.2.1 Drain current model

Further, in the linear regime of Eq. (2-1) can be also described by inversion charge Q_{inv},

$$I_{ds}(V_{gs},V_{ds}) = Q_{inv}(V_{gt})\frac{\mu_{eff}V_{ds}}{L_{eff}^{\ 2}},\ where\ Q_{inv}(V_{gt}) \approx W_{eff}L_{eff}C_{ox}(V_{gt}) \qquad (2\text{-}2).$$

In this region ($V_{ds}\leq V_{gt}$), $I_{ds}(V_{gs},V_{ds})$ behaves as a variable resistance controlled by $Q_{inv}(V_{gt})$ and V_{ds}. Two terms of I_{ds}, $Q_{inv}(V_{gs})$ and $\mu_{eff}V_{ds}/L_{eff}^{\ 2}$ ($=\mu_{eff}(V_{ds}/L_{eff})/L_{eff}=v_d/L_{eff}=1/\tau_d$, where v_d and τ_d are the drift velocity and transmit time from source to drain through the silicon channel, respectively) represent the charges coupled with V_{gt} on silicon substrate and constant transmit time, respectively.[5-7] Thus, this Eq. (2-2) clearly expresses the physical meaning of drain current, the total number of charge per unit time.

When the channel is pinch-off ($V_{ds}\geq V_{gt}$), *i.e.*, $Q_{inv}\approx 0$ at the drain end, V_{ds} can be replaced by V_{gt} since saturation region can be simply found at the V_{ds} position of $\partial I_{ds}/\partial V_{ds}=0$. Hence, the saturation I_{ds} model can be alternatively found as below expression from the linear I_{ds} equation in Eq. (2-1):

$$I_{ds}(V_{gs},V_{ds}) = \frac{W_{eff}}{2L_{eff}}\mu_{eff}C_{ox}(V_{gt})^2 \qquad (2\text{-}3).$$

Indeed, I_{ds} the drain current described in Eq. (2-3) ideally is independent of V_{ds}, however, it is worth mentioning that the effect of V_{ds} in practical case on very short channel device is dramatically increased resulting in drain induced barrier lowering (DIBL), V_{th} roll-off owing to the edge effect, punch-through effect, and weak V_{gs} controllability etc.[5-7]

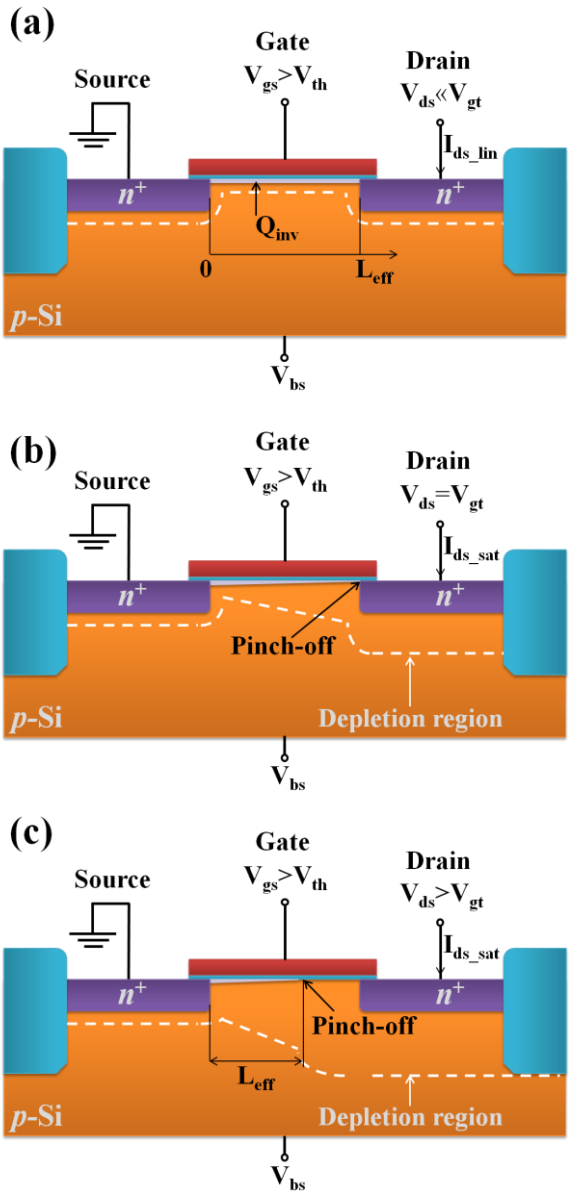

Figure 2-2 Cross-section view of an n-type MOSFET (a) in linear with very small V_{ds}, (b) at onset of saturation (or weak inversion), and (c) deep saturation regime.

Generally, the drain current behavior of $I_{ds}(V_{gs})$ is called to transfer curve. And it is the most basic electrical measurement result. However, it contains many important clues for example, V_{th}, field-effect mobility (μ_{fe}), R_{sd} effect, on and off current ratio, and subthreshold swing (SS) as well. In order to evaluate such parameters, equation (2-1) based mathematical techniques such as drain conductance (g_d) and transconductance (g_m) usually employed by assuming $\theta_2=0$ with small V_{ds} (in the linear regime):

$$g_d = \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{ds}} \approx \frac{G_m V_{gt}}{1+\theta_1(V_{gt})}$$
$$g_m = \frac{\partial I_{ds}(V_{gs}, V_{ds})}{\partial V_{gs}} \approx \frac{G_m V_{ds}}{\left(1+\theta_1(V_{gt})\right)^2} \quad (2\text{-}4),$$

where G_m ($=W_{eff}C_{ox}\mu_0/L_{eff}$) is transconductance parameter. Based on these general relation expressed in Eq. (2-4), a number of papers regarding device characterization methodologies have been published by researchers.[7, 8, 22-27]

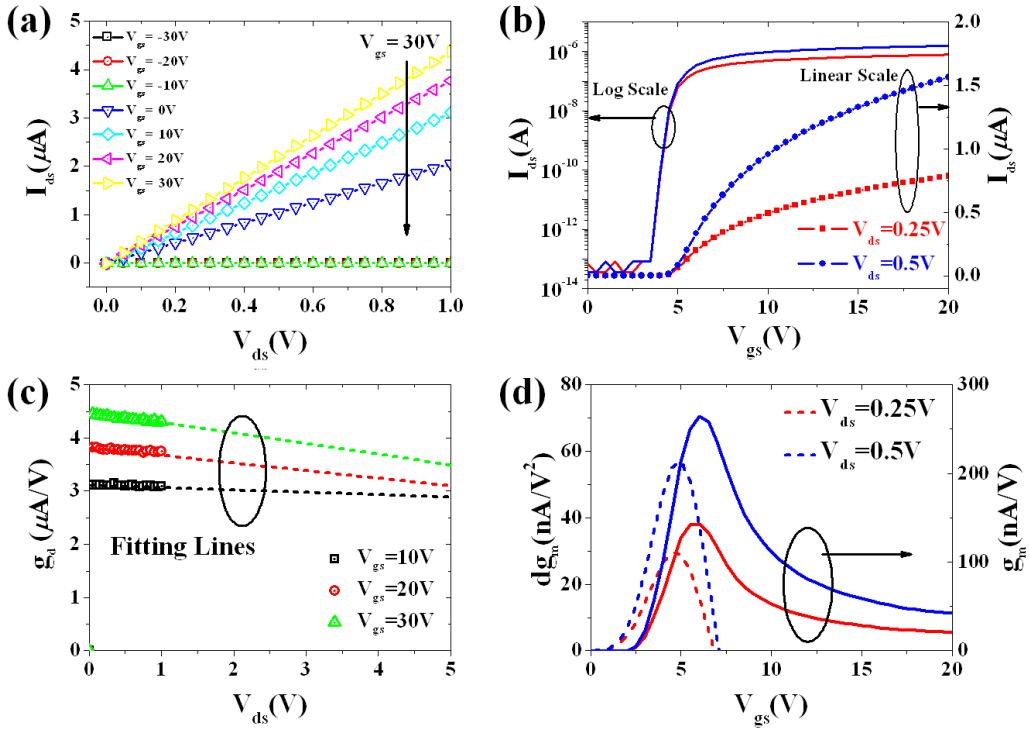

Figure 2-3 Representative examples of (a) output characteristics, (b) transfer curves, (c) drain conductance ($=\partial I_{ds}/\partial V_{ds}$), and (d) transconductance curves ($=\partial I_{ds}/\partial V_{gs}$) of fabricated n-type long channel SnO_2 FET. Detailed electrical analysis will be presented in Chap. 5.

2.2.2.1 Threshold voltage

In the following section, the physical meaning of V_{th} and several V_{th} extraction methods will be examined for n-channel MOSFET. Generally, V_{th} can be fundamentally defined as below expression,[5, 28]

$$V_{th} = V_{FB} + 2\psi_F + \frac{\sqrt{2\varepsilon_{si} q N_A (2\psi_F)}}{C_{ox}}$$
$$= \left(\phi_{ms} - \frac{Q_f}{C_{ox}}\right) + 2\psi_F + \frac{\sqrt{4\varepsilon_{si} q N_A \psi_F}}{C_{ox}} \quad (2\text{-}5),$$

where V_{FB} (=ϕ_{ms}-Q_f/C_{ox}, where ϕ_{ms} and Q_f are the work function difference and the oxide fixed charges between gate material and semiconducting substrate, respectively, representing the built-in potential across MOS system) is the flat-band voltage where the surface potential (Ψ_S) is equal to zero and energy bands in semiconductor are flat, Ψ_F (=E_i-E_{Fp}, E_i and E_{Fp} are intrinsic and p-doped Fermi energy, respectively) is Fermi potential, ε_{si} is the silicon permittivity, respectively), q is the electron unit-charge, and N_A is p-type substrate doping concentration. Thus, V_{th} is the gate induced bias voltage by the amount of $2\Psi_F$ to achieve surface inversion across the oxide and semiconductor surface. In addition, when the substrate bias V_{BS} (or back gate bias) is applied, Eq. (2-5) can be modified as following expression,

$$V_{th} = V_{FB} + 2\psi_F + \frac{\sqrt{2\varepsilon_{si} q N_A (2\psi_F - V_{BS})}}{C_{ox}} \qquad (2\text{-}6).$$

Hence, V_{th} based on Eqs (2-5) and (2-6) can be controlled by substrate doping concentration and V_{BS} with aims of various practical purposes such as a circuit design. (It is worth noting that V_{th} should be modified with accounting for the electrostatic potential distribution arisen from device structure, i.e., multi-gate or FD-SOI) Besides, V_{th} is very critical value for modeling and characterization of MOSEFET since it can be strongly affected on other parameter extraction procedures. However, it is worth noting that V_{th} values of advanced MOSFET cannot be precisely determined by using Eq. (2-6), mainly due to parameter uncertainty and variations arisen from doping concentration, oxide thickness, and the quantity of Q_f, R_{sd} effect etc.[28, 29] It is therefore, V_{th} is ultimately relied on various extraction methods based on direct measurement results with statistical arrangement.

1) **Linear extrapolation method** (LEM) is a representative classical technique to evaluate V_{th} in MOSFET characterization.[5, 18, 26, 27, 30] In this method, V_{th} can be found by the linear extrapolation of drain current I_{ds}-V_{gs} curve at the point of maximum value of $g_m(V_{gs})$. To do this, I_{ds} must be measured as a function of V_{gs} with small V_{ds} to ensure the operation in linear regime. Based on Eq. (2-1) in triode region, V_{th} is corresponding to V_{th_LEM}-$V_{ds}/2$. The main drawbacks of this method are the deviations of straight line of I_{ds}-V_{gs} curve arisen from the subthreshold current before V_{th_LEM} and the presence of high R_{sd} and mobility degradation effects above V_{th_LEM} as plotted in Fig 2-4(a).[5, 27] Thus, it is simple and fast technique used for MOSFET including depletion-mode or buried channel, but it is worth noting that LEM should be strictly used only for linear region with negligible R_{sd} effects.[30]

2) **Second derivative method** (SDM)[26] was originally developed from Eq. (2-1)

with aims of suppression of R_{sd} effects. V_{th} of SDM (V_{th_SDM}) can be determined at V_{gs} point of the maximum value of derivative g_m, max(dg_m) with small V_{ds} ($\partial g_m/\partial V_{gs}=\partial^2 I_{ds}/\partial V_{gs}^2$) as displayed in Fig. 2-4(b). Ideally, $\partial I_{ds}/\partial V_{gs}$ ($V_{gs}>V_{th}$) becomes a step function, resulting in that $\partial g_m/\partial V_{gs}$ has to be delta function.[5, 26, 27] By definition, the value of max(dg_m) should have infinite, however it exhibits just the maximum value at $V_{gs}=V_{th\_SDM}$ in real case since for such a simplified device model expressed in Eq. (2-1). Therefore, V_{th_SDM} can be conveniently computed by such simple procedures, but it tends to be sensitively influenced by I_{ds}-V_{gs} measurement noise, speed, and V_{gs} step.[27]

3) **Constant current method** (CCM) is perhaps the simplest technique to evaluate V_{th}, typically taken from the V_{gs} point corresponding to an arbitrarily chosen constant drain current I_{ds_CCM}, e.g. $I_{ds\_CCM}=(W_{eff}/L_{eff})\times 10^{-7}$.[27, 31] Because of its simplicity, V_{th_CCM} can be quickly obtained in wafer-scale measurement, but it can be sensitively deviated depending on arbitrarily chosen level of I_{ds}.

4) **Second derivative logarithmic method (SDLM)** [27, 32] was proposed to overcome restraints or drawbacks of previously introduced method such as CCM requiring the effective channel aspect ratio and LEM within linear region. By their definition, V_{th_SDLM} can be decided at the V_{gs} point corresponding to the minimum value of second derivative of the logarithm of the drain current. In addition, V_{th_SDLM} indicates the moment at that drift and diffusion currents are equal to each other. However, as similar to SDM, V_{th_SDLM} can be noisy unless drain current measurement system is well organized.

5) Other methods also already reported such as transconductance linear extrapolation method, ratio method, transition method, integral method, Corsi function method, linear cofactor difference operator method, and non-linear optimization etc.[27]

It is inevitable that as the size of device structure is shrunk, undesired parasitic influences such as strong R_{sd} and surface roughness scattering effects might be enhanced when evaluating V_{th} by using aforementioned methods. Thus, it is strongly recommended that a proper V_{th} has to be chosen by comparison of various V_{th} based on several extraction methods. In addition, noting that such extraction methods based on Eq. (2-1) still valid for not only MOSFET device but also low dimensional nano-structure (quasi-1D SnO_2 FET) as displayed in Fig. 2-4.

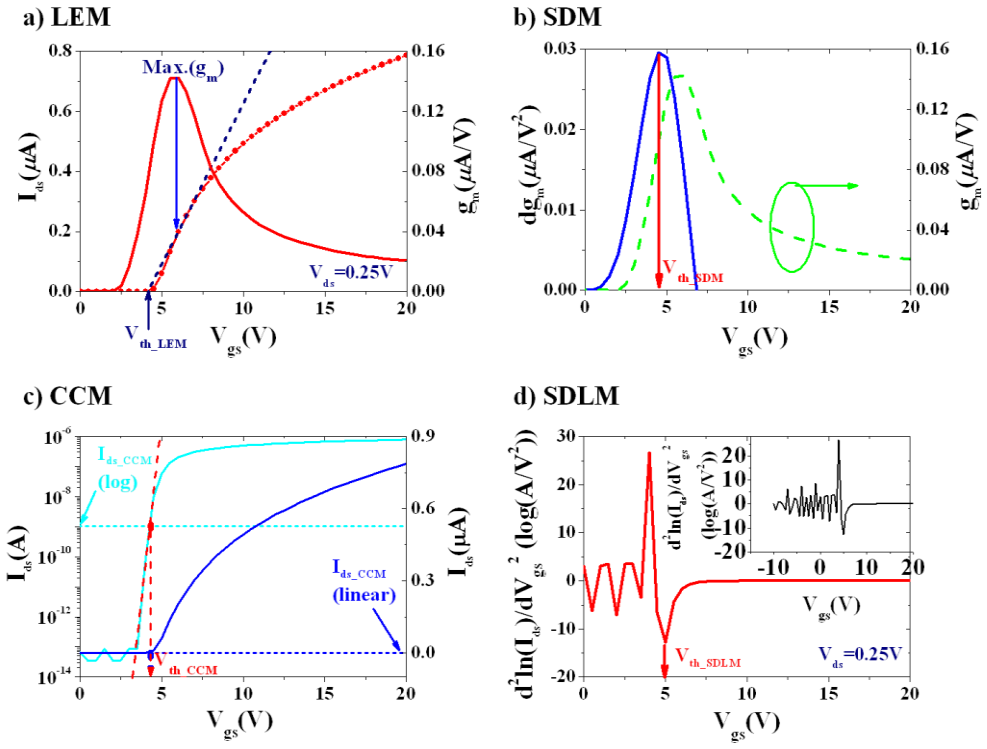

Figure 2-4 Various V_{th} extraction methods for PMMA (polymethyl methacrylate) passivated SnO_2 FET (W_{eff}=42nm and L_{eff}=4.02μm on 150nm Si_3N_4 layer) by using (a) LEM, (b) SDM, (c) CCM, and (d) SDLM

2.2.2.2 Field-effect mobility

Field-effect mobility (μ_{fe}) is one of generally reported mobility values extracted from transfer curve to present device performance. It is roughly derived from transconductance g_m based on I_{ds}–V_{gs} triode model in Eq. (2-1), defined as

$$\mu_{fe} \approx \frac{L_{eff} g_m}{W_{eff} C_{ox} V_{ds}}, \text{where } g_m = \left.\frac{\partial I_{ds}}{\partial V_{gs}}\right|_{V_{ds}=\text{constant}} \approx \frac{W_{eff} C_{ox} V_{ds}}{L_{eff}} \mu_{eff} \qquad (2\text{-}7).$$

In fact, Eq. (2-7) assumed that μ_{eff} is independent of V_{gt}, however it is closely affected by V_{gt} in real device since for strongly enhanced interfacial effects such as channel access resistance, surface roughness scattering etc. Thus, to account for V_{gt} influence on μ_{eff}, μ_{fe}' can be modified as following expression,[5]

$$\mu_{fe}' = \frac{L_{eff} g_m}{W_{eff} C_{ox} V_{ds} \left(1 + \frac{V_{gt}}{\mu_{eff}} \frac{\partial \mu_{eff}}{\partial V_{gs}}\right)} \qquad (2\text{-}8).$$

Finally, various mobility extracted from SnO_2 FET such as μ_0 (extracted by YFM which will be discussed later section), μ_{fe}, and μ_{fe}' are plotted in below Fig. 2-5. The reason for large discrepancy among mobility values compared to μ_0 at high V_{gs} regime can be mainly explained by the

effective V_{ds} arisen from contact resistance effect. Further mobility analysis of PMMA passivated SnO_2 FET in terms of R_{sd} and the electrostatic gate capacitance coupling effects arisen from PMMA layer will be conducted in Chap. 4.

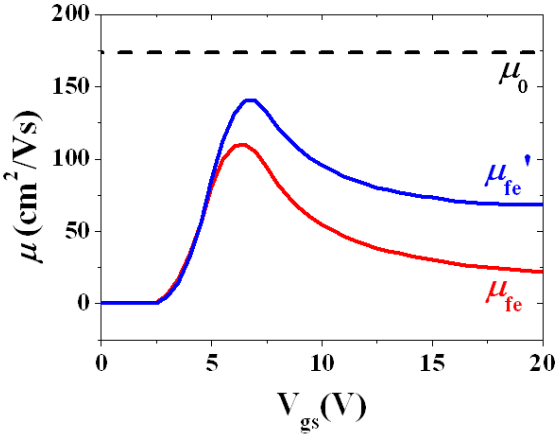

Figure 2-5 Comparison of various mobility values (μ_0, μ_{fe}, and μ_{fe}') in PMMA paasivated SnO_2 FET.

2.2.2.3 Series resistance

One of the issues in advanced MOSFET is the minimization of R_{sd} effects. The influence R_{sd} at the source and drain ends of MOSFET is dramatically enhanced as the channel length scaled down since the fraction of R_{sd} to the channel is relatively increased. Since the total resistance ($R_{tot}=R_{ch}+R_l=V_s/I_m$, where V_s is a constant voltage source and I_m is a measured current, respectively) measured by simple two-probe measurement can be affected by the lead resistance (R_l), the channel resistance (R_{ch}) will be overestimated as demonstrated in Fig. 2-6(a). To avoid this undesired situation, one well known technique namely four-probe measurement method is usually employed to directly determine R_{ch} and R_l. It consists of one constant current source (I_{tot}), one voltage-meter (V_m) which has very large internal resistance ($R_V \approx \infty$), and four electrodes as displayed in Fig. 2-6(b). To determine R_{ch} ($\approx V_m/I_{tot}$) accurately, the two outer and inner probes are used for constant current flowing and voltage measuring, respectively. Besides, two-probe measurement results can be exploited to obtain R_l ($\approx R_{tot}-R_{ch}$) by subtraction R_{ch} from R_{tot}.

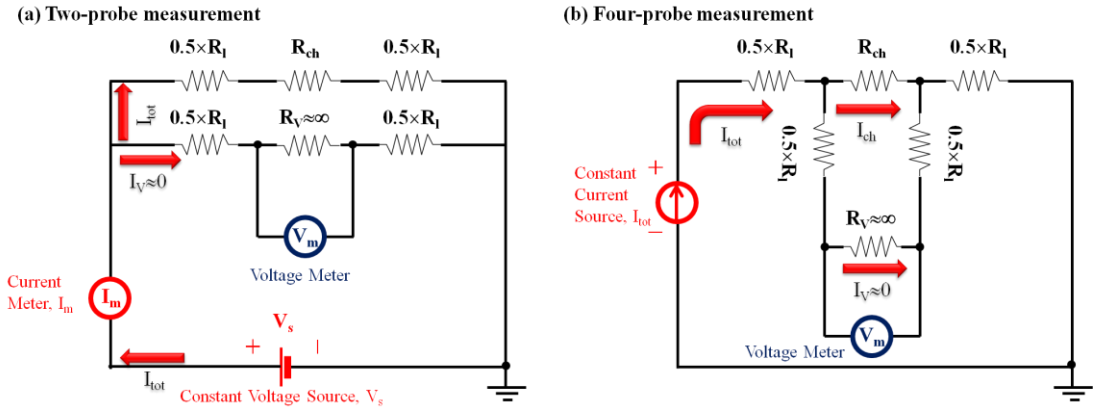

Figure 2-6 (a) Two-terminal and (b) four-prove measurement configurations.

In fact, to properly apply the four-probe measurement concept in three-terminal system such as transistors, a specific test pattern should be needed to get R_{sd} with the aim of separating sheet channel resistance and contact resistance. In addition, more complicated approaches should be required by considering the transistor model to appropriately evaluating R_{sd} since this is primarily for metal based system. Indeed, the effective drain voltage V_{ds}' ($=V_{ds}-I_{ds}\cdot R_{sd}$) to FET channel can be reduced due to the existence of R_{sd} near source and drain region, resulting in under- and/or over-estimation of μ_{fe} and V_{th} as explained previously. To account for R_{sd} effects on the I_{ds}-V_{gs} relation, Eq. (2-1) in linear regime has to be changed to following expression,

$$I_{ds}(V_{gs},V_{ds}) = \frac{W_{eff}}{L_{eff}}\mu_{eff}C_{ox}(V_{gt}-\frac{V_{ds}'}{2})V_{ds}' \approx \frac{W_{eff}}{L_{eff}}\mu_{eff}C_{ox}V_{gt}(V_{ds}-I_{ds}R_{sd}) \qquad (2\text{-}9)$$

$$I_{ds}(V_{gs},V_{ds}) \approx \frac{\frac{W_{eff}}{L_{eff}}\mu_{eff}C_{ox}V_{gt}V_{ds}}{1+\frac{W_{eff}}{L_{eff}}\mu_{eff}C_{ox}V_{gt}R_{sd}} \qquad (2\text{-}10)$$

This is the basic model for the most techniques to determine R_{sd}. However, as the device models are complicated, further improved and alternative techniques have been requested. To do this, many efforts have been made to make theoretical methodologies such as transmission line model (TLM) and YFM (details will be presented in next section) etc. to evaluate the intrinsic properties without R_{sd} influences.[5, 7, 8, 25, 28]

TLM is frequently used for the R_{sd} approximation in many types of transistors even in nano-scaled device.[5, 7, 12, 33, 34] To begin with Eq. (2-10), R_{tot} can be expressed as,

$$R_{tot} = \frac{V_{ds}}{I_{tot}} = \frac{L_{eff}}{W_{eff}\mu_{eff}C_{ox}(V_{gs}-V_{th})} + R_{sd} = \frac{L_m-\Delta L_m}{W_{eff}\mu_{eff}C_{ox}(V_{gs}-V_{th})} + R_{sd} \qquad (2\text{-}11),$$

where L_m is mask design length and ΔL_m mask reduction length, respectively. Further, R_{tot} can be plotted as a function of L_m at least two different lengths for varying V_{gs} values in n-channel MOSFETs as shown in Fig. 2-7.[34] From the interception points of each straight line, ΔL_m and R_{sd} can be safely determined, respectively. In addition, Eq. (2-11) can be further processed to determine μ_{eff} and V_{th} as following,

$$\frac{1}{R_{tot}-R_{sd}}=\frac{W_{eff}\mu_{eff}C_{ox}\left(V_{gs}-V_{th}\right)}{L_{eff}} \qquad (2\text{-}12).$$

From the linear fit of Eq. (2-12), μ_{eff} and V_{th} are safely obtained from the slope and interception points of V_{gs} axis. However, it is worth mentioning that this method assumed that ΔL_m and R_{sd} have a weak dependence of V_{gs}, which might be usually suitable for long channel device since V_{th} can be strongly affected by a high transverse field in short channel devices.

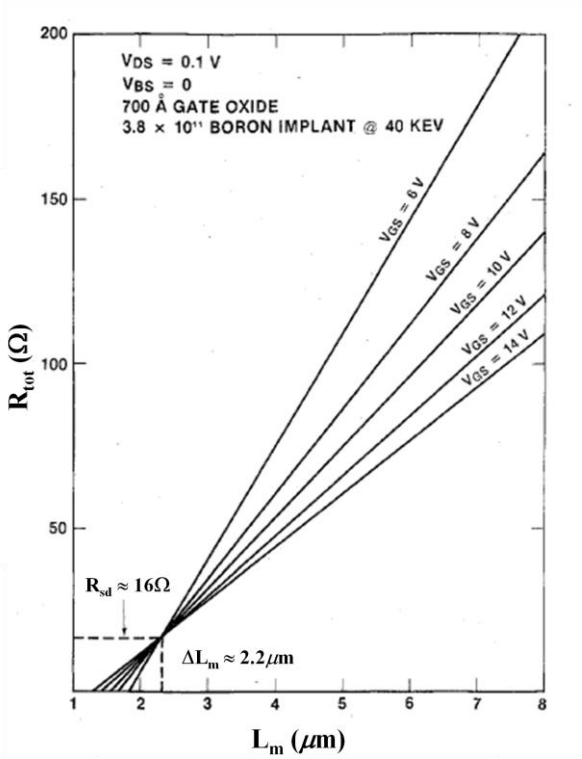

Figure 2-7 Measured total resistance R_{tot} as a function of L_m depending on different V_{gs} values for a set of poly silicon gate n-channel MOSFETs with fixed mask width W_m=200μm with 70nm SiO_2 MOSFET.[34]

2.2.2.4 Subthresholod swing

Miniaturization of MOSFET has brought into dramatic improvement in the switching speed, density, and functionality of CMOS (Complementary metal-oxide-semiconductor) based microprocessor.[35] However, the dramatically increase of leakage current (so called, subthreshold current I_{ds_sub} or I_{off} when $V_{gs}<V_{th}$) which involves with the thermionic and injection of electrons over energy barrier becomes one of urgent issues to be solved, since this limits

the switching performance of transistors from off- to on-state.[28, 35] In fact, I_{ds_sub} has to be zero based on the model in Eq. (2-1), but there is a small diffusion current I_{ds_sub} in subthreshold region, which defined as below,

$$I_{ds\_sub} = \mu_{eff} C_{ox} \frac{W_{eff}}{L_{eff}} (m-1) \left(\frac{k_B T}{q}\right)^2 \exp\left(\frac{qV_{gt}}{mk_B T}\right)\left(1-\exp\left(\frac{-qV_{ds}}{k_B T}\right)\right) \quad (2\text{-}12),$$

where m is the body-effect coefficient ($=\partial V_{gs}/\partial \Psi_S$), k_B is the Boltzmann constant, and T is absolute temperature, respectively.[28, 35, 36] For this reason, the gate induced bias voltage is required to turn the transistor off when operating in subthrshold region. To present this ability, the subthreshold swing (SS) have been derived as,

$$SS = \underbrace{\frac{\partial V_{gs}}{\partial \Psi_S}}_{m} \underbrace{\frac{\partial \Psi_S}{\partial \log_{10} I_{ds\_sub}}}_{n} \approx \left(1+\frac{C_d + C_{it}}{C_{ox}}\right) \ln(10) \left(\frac{k_B T}{q}\right) \quad (2\text{-}13),$$

where n is a factor that characterizes the change of the drain current with Ψ_S, C_d and C_{it} are the depletion and surface state capacitance respectively.[5, 28, 35] Ideally, it is evident that the minimum value of SS in transistors has to be limited by $\approx \ln(10)(k_B T/q)$. However, in the presence of a significant interface trap density ($D_{it}=q^2 C_{it}$), SS can be sensitively degraded by definition. Furthermore, by measuring SS from semi-log plot of transfer curve in subthreshold region as displayed in Fig. 2-8, D_{it} can be obtained from below Eq. (2-14),

$$D_{it} \approx \frac{C_{ox}}{q^2}\left(\frac{q \cdot SS}{\ln(10) k_B T} - \left(1+\frac{C_d}{C_{ox}}\right)\right) \quad (2\text{-}14).$$

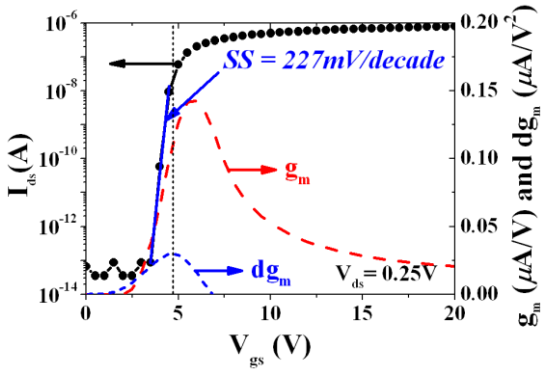

Figure 2-8 Subthreshold characteristic of PMMA passivated SnO_2 FET.

To calculate D_{it}, precise C_{ox} and C_d values are required.

2.3 Y Function Method

In this section, transfer curve based parameter extraction methodology will be discussed mainly about YFM since this is the most simple but powerful and physically meaningful

method for the silicon based MOSFETs,[7, 8] 1D nanowire device,[9, 10] carbon nanotube random networks,[11] and OFETs.[12] In principle, this YFM can be started from drain current model described in Eq. (2-1) and g_m in Eq. (2-4) in linear region, together. By definition, YFM is expressed as below description,[8]

$$YFM = \frac{I_{ds}}{\sqrt{g_m}} = \sqrt{G_m V_{ds}}\,(V_{gs} - V_{th\_YFM}) \qquad (2\text{-}15).$$

It is therefore able to suppress the influence θ_1 by assuming θ_2=0 with small V_{ds} because it is independent of θ_1.[7] In addition, μ_0 and V_{th_YFM} can be extracted by the slope and the intercept of V_{gs} axis of YFM without R_{sd} effects, respectively. It is noted that the θ_1 factor is closely related with R_{sd} effects since it describes the impurity, phonon and lattice scattering.[7, 8] This is a very important feature of YFM for small channel devices. As a representative example, YFM obtained from PMMA passivated SnO_2 FET is displayed in Fig. 2-9. It shows a good linearity with Eq. (2-15) except high V_{gs} regime, which will be further fitted by employing the θ_2 parameter. With the aim of V_{th} comparison between YFM and SDM, each curve of YFM and dg_m are also plotted in the same figures. (See Fig. 2-9(a)) Two V_{th} values are almost similar to each other.

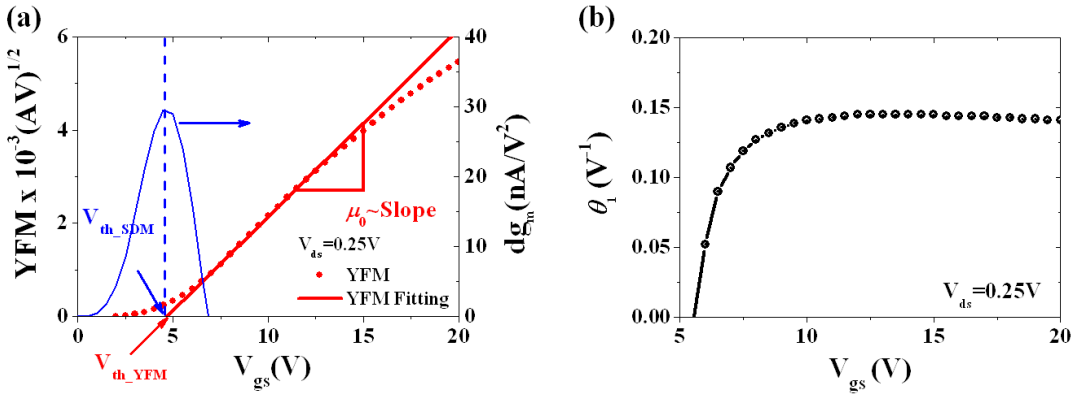

Figure 2-9 (a) YFM and dg_m, and (b) θ_1 curves of PMMA passivated SnO_2 FET as a function of V_{gs}.

Further, the θ_1 ($\approx$0.14V^{-1}) factor can be found at high V_{gs} regime based on inverse of I_{ds} model as plotted in Fig. 2-9(b),[7, 26]

$$\theta_1 = \frac{G_m \cdot V_{ds}}{I_{ds}} - \frac{1}{V_{gt}} \qquad (2\text{-}16).$$

In addition, if the device wafer has several different sets of length splits, R_{sd} and ΔL_m also can be estimated by plotting 1) θ_1 versus G_m for R_{sd}, and 2) $1/G_m$ versus L_m for ΔL_m, respectively, accounting for below relations,[7]

$$\theta_1 = \theta_0 + G_m R_{sd} \qquad (2\text{-}17).$$

$$\frac{1}{G_m} = \frac{L_{eff}}{W_{eff} C_{ox} \mu_0 V_{ds}} = \frac{L_m - \Delta L_m}{W_{eff} C_{ox} \mu_0 V_{ds}} \qquad (2\text{-}18).$$

It is underlined that to successfully exploit Eq. (2-18), μ_0 should remain constant when L_{eff} is decreased.[7]

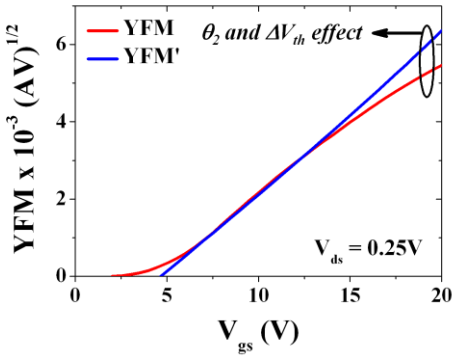

Figure 2-10 Comparison between YFM and YFM′ after consideration of θ_2 and ΔV_{th}.

As the oxide thickness becomes thinner and the length of device shrunk, taking into account of the presence of θ_2 is required in YFM since the transverse field in the channel is dramatically increased to make surface roughness prevail in strong inversion region. Thus, after full consideration of the second attenuation factor θ_2 in mobility model, it is reduced as below,

$$YFM' \approx \frac{I_{ds}}{\sqrt{g_m}} = \frac{V_{gt}\sqrt{G_m V_{ds}}}{\sqrt{1-\theta_2(V_{gt}^{\ 2} - \Delta V_{th}^{\ 2})}} \qquad (2\text{-}19).$$

Moreover, to obtain θ_2 and ΔV_{th}, many extraction technologies have been introduced to solve this difficulty.[7, 8, 24, 25, 32, 37-41] One simple process can be started with V_{th_YFM} and θ_1 evaluated in Eqs (2-15 and 2-16). Extraction of θ_2 and ΔV_{th} is then calculated from Eq. (2-20) expressed in following equation,

$$\sqrt{\frac{G_m V_{gt} V_{ds}}{I_{ds}} - \theta_1 V_{gt} - 1} = \sqrt{\theta_2}(V_{gt} - \Delta V_{th}) \qquad (2\text{-}20).$$

After determination of θ_2 ($\approx 8.0\times10^{-4}$ V^{-2}) and ΔV_{th} ($\approx$-5.22 V) from the slope and linear extrapolation of x-axis based on Eq. (2-20), the newly calculated YFM′ obtained from Eq. (2-19) is plotted together with the previous YFM in Fig. 2-10 for the purpose of comparison. Finally, the straight line of YFM′ is clearly shown after accounting for θ_2 and ΔV_{th}.

2.4 Split C-V Method

The low frequency capacitance–voltage characteristics (or C–V profiling) is a non destructive and electrical analysis tool to investigate on 1) the relationship between the gate and

surface potential ($\partial V_{gs}/\partial \Psi_S$), 2) the determination of charge trapped in interface states in weak inversion, 3) the interface state density in weak inversion, and 4) the bulk dope density of MOSFET or MOSCAP (Metal-Oxide-Semiconductor Capacitor).[42].

Especially, the mobile channel charge density measurement technique, so called the split C-V technique[5, 7, 42] which composes of 1) gate-to-channel capacitance (C_{gc}), 2) gate-to-bulk capacitance (C_{gb}), and 3) total capacitance ($C_g=C_{gc}+C_{gb}$), is frequently employed to provide various intrinsic channel properties such as N_D or N_A, V_{FB}, V_{th}, C_{ox}, CET, and ΔL_m or ΔW_m, respectively.[7]

1) In principle of C_{gb} measurement: A small (usually less than thermal voltage, k_BT/q) AC voltage signal superimposed on DC V_{gs} bias is applied to the gate (G) through the "High" terminal of LCR meter, a small AC current signal is measured at the bulk substrate connected to "Low" terminal of LCR meter, and source (S) and drain (D) are grounded as presented in Fig. 2-11.[7, 42] The Q_{acc} and C_{pd} describe the number of accumulation charges (Q_{acc}) and polysilicon depletion capacitance (C_{pd}), respectively. In accumulation regime, the holes have to be accumulated and saturated underneath the gate, indicating C_{ox} can be directly obtained if the surface area is known. As V_{gs} is increased more than V_{FB}, the holes can be pushed away from the surface resulting in growing depletion region. Further, if V_{gs} is above V_{th}, the inversion channel is created and connected to S and D, *i.e.*, it is grounded. Hence, C_{gb} has to be zero (or parasitic capacitance) since the "Low" terminal cannot feel any small current signal.

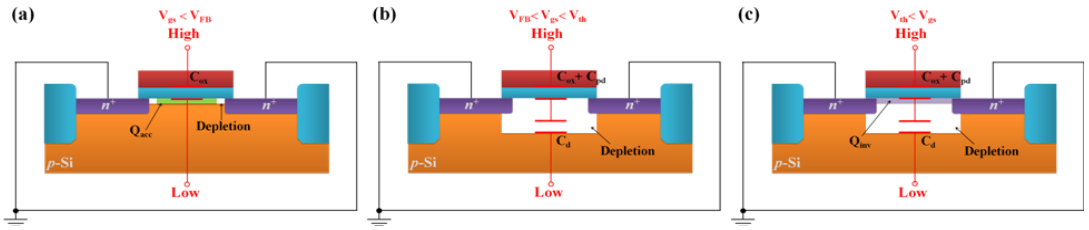

Figure 2-11. Equivalent circuit models for C_{gb} measurement depending on the conduction regimes, (a) accumulation, (b) depletion, and (c) inversion, respectively.[7]

2) In principle of C_{gc} measurement: The gate (G) is connected to the "High" terminal of LCR meter, shorted D and S are connected to the "Low" terminal of LCR meter, and bulk substrate is grounded as shown in Fig. 2-12.[7, 42] In accumulation regime, the capacitance value goes to be zero (or parasitic capacitance) since accumulated holes cannot pass the junction capacitance (C_j) except the case of tunneling conduction between the n-doped S/D and accumulated hole channel. As V_{gs} is increased, the depletion region is extended and the inversion channel is finally created. Thus, C_{gc} is then saturated in inversion regime, C_{ox} can be directly

obtained. Since Q_{inv} can be determined by integrating C_{gc} curves as a function of V_{gs}, the effective mobility can be calculated by following equations,

$$Q_{inv} = \frac{1}{L_{eff} W_{eff}} \int C_{gc}(V_{gs}) dV_{gs} \qquad (2\text{-}21)$$

$$\mu_{eff} = \frac{I_{ds} L_{eff}}{Q_{inv} W_{eff} V_{ds}} \qquad (2\text{-}22).$$

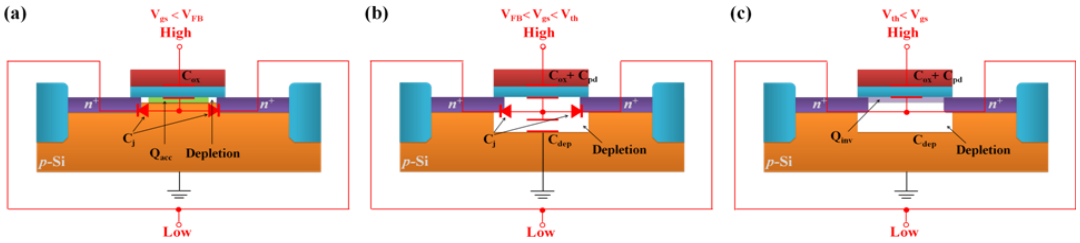

Figure 2-12. Equivalent circuit models for C_{gc} measurement depending on the conduction regimes, (a) accumulation, (b) depletion, and (c) inversion, respectively.[7]

3) In principle of C_{tot} measurement: The gate (G) is connected to the "High" terminal of LCR meter, shorted D, S and bulk substrate are all connected to the "Low" terminal of LCR meter, respectively, as displayed in Fig. 2-13.[7, 42] It can be naturally accepted that C_{tot} is the sum of C_{gb} and C_{gc} since the previous two measurement configurations are superimposed.

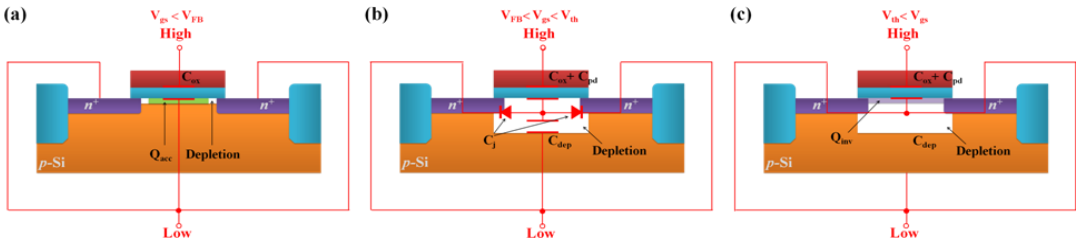

Figure 2-13. Equivalent circuit models for C_{tot} measurement depending on the conduction regimes, (a) accumulation, (b) depletion, and (c) inversion, respectively.[7]

It is recommended that to get rid of the influences arisen from the interface state capacitance and the parasitic capacitance in small devices when estimating C_{ox}, C_{gc} with high frequency (typically in the MHz range) measurement is preferred.[7, 43]

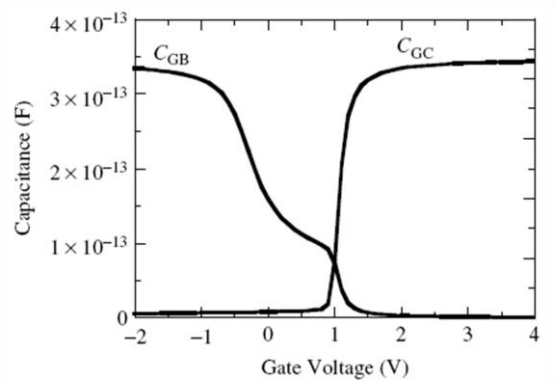

Figure 2-14 Typical split CV (C_{gb} and C_{gc}) curves as a function of V_{gs}.[5]

2.4.1 C_{ox} and CET evaluation based on C_{gc}^{-1}

The estimation of the thickness of oxide capacitance is more and more important as device size is scaled down. In fact, physical measurement of Atomic Force Microscopy (AFM) and optical measurement (ellipsometry) can be used for it, but the former one is not suitable for production line and the latter one can affected by errors arisen from the interfacial layer and the imprecise refraction index of material.[5, 15] Thus to appraise this quick and accurately, various methods have been made, mostly relied on classical C_{gc} vs. V_{gs} measurement.[15, 44] One of advanced technique is $1/C_{gc}$ vs. $1/(V_{gs}-V_{FB})$. In accumulation region of MOS capacitor structure, $C_{gc}(V_{gs})$ can be described by simply two capacitors in series, namely, C_{ox} and C_{sc} (semiconductor capacitor per unit area, $\partial Q_{acc}/\partial \Psi_S$). The relation between all capacitance values can be simply expressed as,

$$\frac{1}{C_{gc}(V_{gs})} \approx \frac{1}{C_{ox}} + \frac{1}{C_{sc}} \approx \frac{1}{C_{ox}} + \frac{\alpha}{(V_{gs} - V_{FB})^n} \qquad (2\text{-}23),$$

where α is a constant and n is an exponent depending on the accumulation layer carrier statistics.[5, 15] Here, the exponent n can be theoretically chosen depending on the charge distribution model; n=1 for a Maxwell-Boltzmann statistics, n=5 for a Fermi-Dirac statistics, n=3 for a statistics taking into account quantum phenomena, respectively.[15] After determination of the exponent n and V_{FB}, C_{ox} can be then readily calculated from the y-axis intercept of Eq. (2-23) and corresponding CET as well. Representative C_{gc} and C_{gc}^{-1} examples for junctionless transistor (JLT) which will be discussed in detail in next chapter are plotted in Fig. 2-15. As seen in Figs 2-15(a) and (b), this technique enables to determine C_{ox} more accurately compared to classical C_{gc} vs V_{tg}.

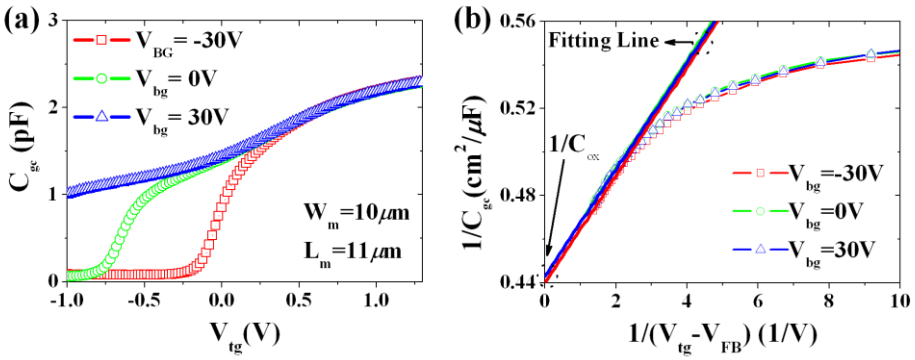

Figure 2-15 (a) $C_{gc}(V_{tg})$ curves of N-type JLT (L_m=11μm with W_m=10μm) depending on V_{bg}, V_{tg} and V_{bg} are top and back gate induced bias respectively and (b) corresponding $1/C_{gc}(V_{tg})$ curves for C_{ox} and corresponding CET extraction in high V_{tg} regime.

2.4.2 V_{FB} and N_D extraction based on C_{gc}^{-2}

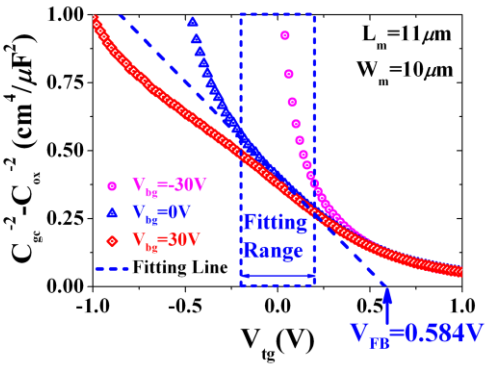

Figure 2-16 $C_{gc}(V_{tg})^{-2}$-C_{ox}^{-2} curves of N-type JLT depending on V_{bg}.

Further, $1/C_{gc}^{2}$ technique can be employed to determine V_{FB} and N_D in partially depletion region with C_{ox} evaluated by Eq. (2-23) as presented in Fig. 2-16. This is given by,

$$\left(\frac{1}{C_{gc}}\right)^2 - \frac{1}{C_{ox}^{\ 2}} \approx \frac{2}{q\varepsilon_{si}N_D}(V_{gs} - V_{FB}) \qquad (2\text{-}24).$$

From the linear slope and the linear extrapolation to V_{gs} axis, N_D and V_{FB} can be easily obtained, respectively. To decide a proper fitting range, dual gate bias mode can be employed. Depending on V_{bg} is increased (positive direction), the partially depleted regime can be extended as plotted in Fig. 2-16. The extracted V_{FB} is quite consistent with theoretical value extracted from Eq. (2-5) or (2-6) and finally all curves are merged together after using actualized V_{FB} values regardless of V_{bg} condition. However, to reduce errors originated from fitting process, Eq. (2-24) can be differentiated as below,

$$\frac{\partial}{\partial V_{gs}}\left(\frac{1}{C_{gc}(V_{gs})^2}\right)=\frac{2}{q\varepsilon_{si}N_D}\Rightarrow N_D=\frac{2}{q\varepsilon_{si}\dfrac{\partial}{\partial V_{gs}}\left(\dfrac{1}{C_{gc}(V_{gs})^2}\right)} \qquad (2\text{-}25).$$

This expression is the same as Maserjian's function after rearrangement of differentiation term in Eq. (2-25). By this way, N_D was simply determined without reliance of V_{FB} and C_{ox} in partially depleted region as presented in Fig. 2-17(a). In addition, to select the extraction position for N_D appropriately, the derivative of C_{gc} (dC_{gc}/dV_{tg}) can be used. Two peaks are clearly appeared in dC_{gc}/dV_{tg} when V_{tg} is increased from negative to positive. The first peak (left side) represents V_{th}, the turn-on voltage from the full depletion to the partially depletion region and the latter one (right side) indicates V_{FB}, respectively. In V_{tg} range between V_{th} and V_{FB}, N_D then be determined properly. Alternatively, the channel doping concentration can be also estimated by using the sheet carrier density ($n_s=[C_{gc}(V_{gs})/q]dV_{gs}$) and t_{si} (the thickness of silicon film) at the position of V_{FB} as seen in Fig. 2-17.

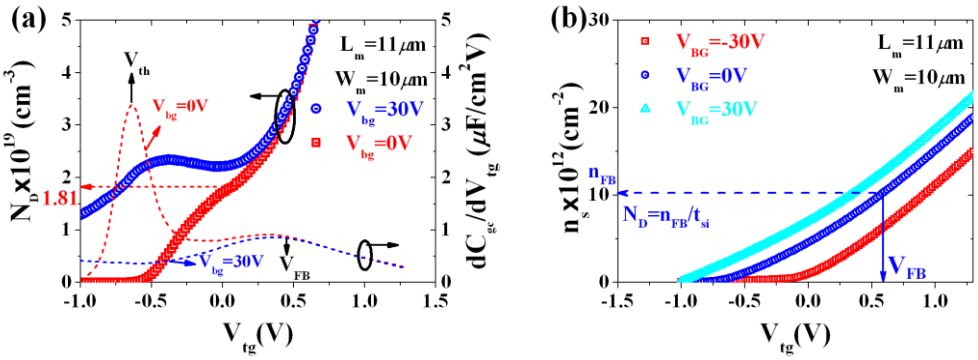

Figure 2-17 (a) N_D based on Eq. (2-25) and dC_{gc}/dV_{tg} (right axis) curves of n-type of JLTs. (b) n_s versus V_{tg} curves for N_D estimation with account for the position of V_{FB}.

Finally, in this section, CV characteristics based on $C_{gc}(V_{gs})$, C_{gc}^{-1}, C_{gc}^{-2} combination with Maserjian's function proves that it can provide useful information about intrinsic channel properties such as C_{ox}, ΔL_m, ΔW_m, V_{FB}, and N_D for the further electrical parameter evaluation.

2.5 Low Frequency Noise Analysis

Low frequency noise (LFN) analysis has gained a great interest to characterize the interface properties with dielectric materials in FETs since it provides information associated with crystalline imperfections, scattering mechanisms or the trapping/de-trapping of the charge carriers at interface layer.[17, 21, 36, 45, 46] This feature is often exploited to assess the post treatment effects such as high-κ or metal passivation, thermal annealing, electrical/thermal stressing and etc.[21, 47, 48]

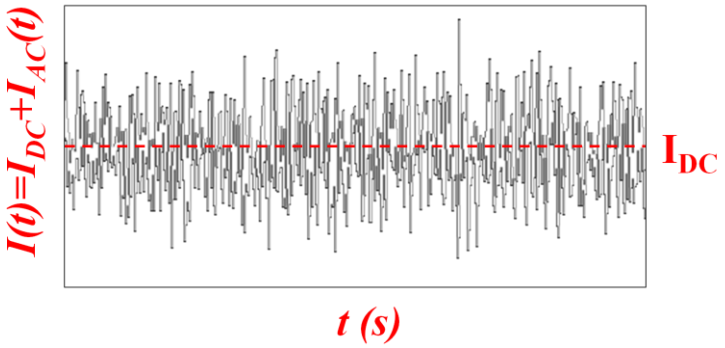

Figure 2-18 A typical transient noise signal is plotted.

Generally, noise can be defined as undesired signal which perturbs the origin signal. Since it disturbs the original messages, the maximum level of noise amplitude can distort the meaning of message, resulting in limiting the varieties of applications. This feature is important in science and engineering since it sets the accuracy limit of an electronic signal or measurement. Figure 2-18 shows a typical randomly fluctuating electronic signal. In principle, this random fluctuation can be stemming from various internal noise sources governing electron transport in a medium if the external noise sources are suppressed enough by a noise filter, a shielding metal box, and a proper layout circuit design. Consequently, it is naturally accepted that the measured noise signal I(t) can be composed of I_{DC} and $I_{AC}(t)$ as illustrated in Fig. 2-18, where I_{DC} and $I_{AC}(t)$ are average value current and randomly fluctuating current in time domain. Indeed, $I_{AC}(t)$ is a random and unpredictable signal, thereby the average value of $I_{AC}(t)$ over a long time will be consequently zero. To process such transient signal physically meaningful, a useful mathematical method was employed so called Fourier transformation which converts time to frequency domain. If we started it briefly from the mathematical probability theory, the mean value and variance in terms of a random variable X can be defined as below,

$$\overline{X} = \int_{-\infty}^{\infty} Xf(X)dX \qquad \text{(2-27) and}$$

$$\text{var } X = \overline{(X-\overline{X})^2} = \overline{X^2} - \left(\overline{X}\right)^2 \qquad \text{(2-28),}$$

where f(X) is a time independent normalized probability density function. (the integration of f(X) over X should be equal to one, $\int_{-\infty}^{\infty} f(X)dX = 1$). Since the noise signals which dealing with are stationary and ergodic, e.g. the distribution for one ensemble over time is equal to the distribution over the whole ensemble at a chosen point in time, the squared power quantity is much suitable to describe noise signals. This is the power spectrum density (PSD) S(f)), which can be obtained from the autocorrelation function R(s) based on Winner-Khintchine the-

orem.[49, 50] (Autocorrelation function refers to the correlation between points with time sequences) Fourier transform of R(s) is a S(f), which can be written as following form,

$$S(f) = FT[R(s)] = 4\int_0^\infty R(s)\cos(2\pi fs)ds \qquad (2\text{-}29),$$

$$R(s) = \overline{X(t)X(t+s)} = \lim_{T\to\infty}\frac{1}{T}\int_0^T X(t)X(t+s)dt = IFT[S(f)] \quad (2\text{-}30).$$

If s is equal to 0 (s=0), it is evident the variance or noise power is a inverse Fourier transform of S(f),

$$\overline{X^2(t)} = \int_0^\infty S(f)df = \lim_{T\to\infty}\frac{1}{T}\int_0^T X^2(t)dt \quad (2\text{-}31).$$

A spectrum analyzer usually measured this quantity (PSD) as a function of frequency (f) or time (t).

Depending on the origins of noise, the PSD shows a different frequency dependent shape as presented in Fig. 2-19(a).

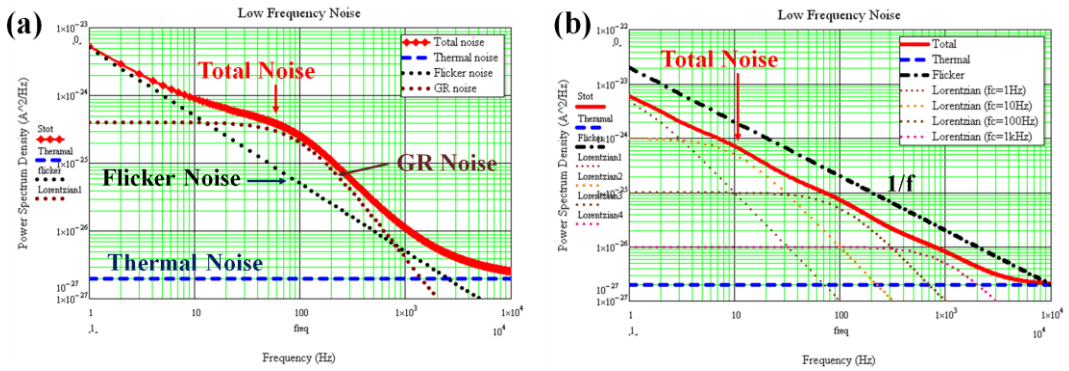

Figure 2-19 (a) Various PSD source for total LFN characteristics and (b) the superposition of four different Lorentzian curves.

1) **Thermal noise** is one of well known fundamental electronic noise sources. This is firstly proposed by Einstein 1906 with Brownian motion of electric charges inside an electrical conductor at thermal equilibrium.[51] After it was experimentally measured and theoretically explained by Jhonson and Nyquist, respectively,[52, 53] it is also called Jhonson or Nyquist noise. In principle, it is approximately white in an ideal resistor (up to 10^{11}-10^{12}Hz), *i.e.* PSD is nearly constant over entire frequency domain. According to theoretical model, the voltage PSD of thermal noise in a piece of resistor (R) at T≠0 was found as,

$$S_V = \frac{\overline{v_n^2}}{\Delta f} = \frac{4k_B TR}{1+(w\tau)^2} \approx 4k_B TR \qquad (2\text{-}32),$$

where $\overline{v_n^2}$ is the average value of noise voltage in a time, w and Δf are the angular frequency (=2πf) and the bandwidth of the measurement system, respectively. Normally, the second term of denominator is negligible in a practical measurement situation, resulting in a constant thermal noise.

2) **Generation-Recombination (GR) noise** is usually observed in semiconductors stemmed from trap sites located in the channel or the gate dielectric oxide layer as impurities or defects. It does indeed randomly capture and emit electric charge carriers (electrons or holes), leading to fluctuate the number of carriers. Hence, it is closely related with fluctuation of carrier mobility, diffusion coefficient, and electric field, and barrier height, space charge region width etc.[21, 36] The PSD of GR noise is found to be,

$$\frac{S_I}{I^2} = \frac{S_N}{N^2} = \frac{\overline{\Delta N^2}}{N^2}\left(\frac{4\tau}{1+(w\tau)^2}\right) \qquad (2\text{-}33),$$

where N is the averaging number of free carriers, ΔN and $\overline{\Delta N^2}$ are the number of fluctuating charge carriers and that of variance, respectively. This shape of PSD is called a Lorentzian and plotted in Figs 2-19(a) and (b). This is only important provided that the Fermi energy is within a few level of k_BT. If the Fermi-level is far from trap energy, the trap influence has to be negligible. But, the trap energy is closed to the Fermi-level, the term of $\overline{\Delta N^2}$ in Eq. (2-33) can be described as below,

$$\frac{1}{\overline{\Delta N^2}} = \frac{1}{N} + \frac{1}{N_{T,\,full}} + \frac{1}{N_{T,empty}} \approx \frac{1}{N} + \frac{4}{N_{T,\,full} + N_{T,empty}} \approx \frac{4}{N_T} \qquad (2\text{-}34),$$

where $N_{T,full}$ and $N_{T,empty}$ are the averaging number of full and empty traps, respectively, by assuming $N >> N_T$ ($N_T = N_{T,full} + N_{T,empty}$).[36] Consequently, we can have a final expression of GR noise,

$$\frac{S_I}{I^2} = \frac{S_N}{N^2} = \frac{N_T}{N^2}\left(\frac{\tau}{1+(w\tau)^2}\right) \quad (2\text{-}35).$$

This is clearly indicating that PSD of GR is proportional to N_T and inversely proportional to N^2. In addition, with a certain distribution of trap energy and spatial position, the PSD can have a shape of 1/f characteristics as displayed in Fig. 2-19(b).[38, 41]

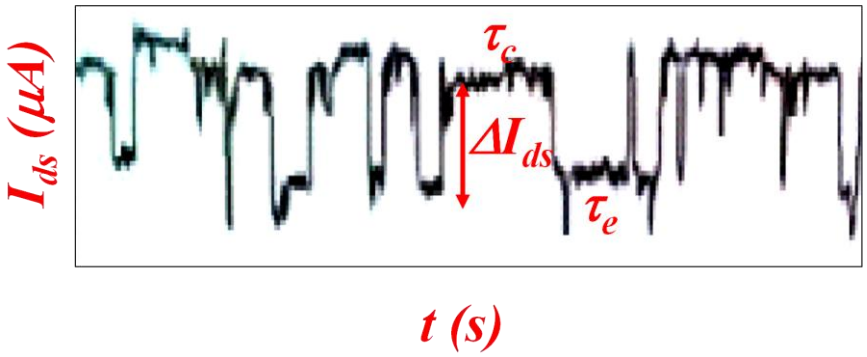

Figure 2-20 Typical I_{ds} as a function of time for RTS noise pattern in JLT. (W_m=L_m=100nm)

3) **Random-Telegraph-Signal (RTS) noise** is sometimes called pop-corn noise, and burst noise, since the shape of this type of noise looks like discrete switching events in the time domain as displayed in Fig. 2-20. Usually, the observation of RTS in small MOSFET devices (surface area under ≈1μm^2) is associated with a few trapping/de-trapping carriers at the interfacial layer between channel and dielectric oxide. For the I_{ds} transition from the low to high state with ΔI_{ds} and Poisson distributed time duration constant τ_e (the emission time) and τ_c (the capture time) arisen from an acceptor like trap, PSD of RTS noise can be written as,

$$S_V = 4A\Delta I_{ds}{}^2 \frac{\tau}{1+(w\tau)^2} \qquad (2\text{-}36),$$

where $\tau = (1/\tau_c+1/\tau_e)^{-1}$ is an effective time constant, $A=\tau\times(\tau_c+\tau_e)^{-1}=f_t(1-f_t)$ is the space mark ratio, f_t is the trap occupancy factor, $f_t=(1+\exp((E_t-E_f)/k_BT))^{-1}$with E_t being the trap energy and E_f the Fermi-level position, respectively.[18] It can be understood by a fluctuation of sheet conductance modulation stemming from carrier number and/or subsequent mobility fluctuation. Accordingly, the relative RTS amplitude can be estimated by assuming the trapping of an electronic unit charge in the channel changes the local conductivity in the linear and saturation regions,[18, 45, 54]

$$\Delta V_{FB} \propto \frac{q}{\Delta W \Delta L C_{ox}} \qquad (2\text{-}37),$$

$$\Delta\sigma = \frac{\partial\sigma}{\partial V_{FB}}\Delta V_{FB} \Rightarrow \frac{\partial\sigma}{\partial V_{gs}} = -\frac{\partial\sigma}{\partial V_{FB}} \qquad (2\text{-}38),$$

$$\frac{\Delta I_{ds}}{I_{ds}} \propto \frac{\Delta\sigma}{\sigma} \propto -\frac{g_m}{I_{ds}}\Delta V_{FB} \propto \frac{g_m}{I_{ds}}\frac{q}{\Delta W \Delta L C_{ox}} \qquad (2\text{-}39).$$

Finally, Eq. (2-39) clearly indicates the RTS amplitude can be varied as a function of V_{ds} and V_{gs} in terms of g_m and I_{ds}. However, further to have a robust applicabil-

ity of this expression, a weighting factor depending on the active area has been proposed to be added to Eq. (2-39). [18, 45, 54, 55]

4) 1/f noise, also called flicker noise, has been observed in a number of natural or artificial systems.[36, 56, 57] This spectrum is inversely proportional to frequency domain in low frequency range (10^{-5} to 10^{7} Hz),

$$S_I \propto \frac{1}{f^{\gamma}} \qquad (2\text{-}40),$$

where γ is a frequency exponent.[17, 19, 21, 36] The parameter of γ has been generally found close to 1 in a condensed matter system including semiconducting transistors in quasi-equilibrium, but usually in the range 0.7 to 1.3.[36] It is thus, there are two representative physical origins in MOSFET (*i.e.*, fluctuations in the carrier mobility or in the number of carriers) of the conductance fluctuations and their corresponding theoretical models, which will be discussed in next section in detail.[36]

2.5.1 Mobility fluctuation model (HMF)

The mobility fluctuations noise model in the drain current was proposed and experimentally proved by F.N. Hooge with following formula,[19, 20]

$$\frac{S_I}{I_{ds}^{\ 2}} = \frac{S_R}{R^2} = \frac{\alpha_H}{Nf} \qquad (2\text{-}41),$$

where N and α_H ($\approx 10^{-5}$) are the total number of mobility fluctuation independent free carriers and the Hooge parameter, respectively.[17] This can be possibly understood provided that the phonon/lattice scattering can only affect on the mobility fluctuations.[58] With a drain current model of MOSFET in the linear regime, it can be simply modified from Eq. (2-41) as,

$$\frac{S_I}{I_{ds}^{\ 2}} = \frac{q\alpha_H}{fW_{eff}L_{eff}Q_{inv}} = \frac{q\alpha_H\mu_{eff}V_{ds}}{fL_{eff}^{\ 2}I_{ds}} \qquad (2\text{-}42),$$

where $Q_{inv} \approx W_{eff}L_{eff}C_{ox}(V_{gs}-V_{th})$. In fact, α_H has been theoretically considered as a universal constant, it perhaps can be influenced by the gate bias dependence or the position of channel under the gate oxide.[36] Although, this equation can be even applicable in subthreshold region, the drain current model in saturation region can be also considered as,

$$\frac{S_I}{I_{ds}^{\ 2}} = \frac{\alpha_H\mu_{eff}2k_BT}{fL_{eff}^{\ 2}I_{ds}} \qquad (2\text{-}43).$$

This clearly means that the I_{ds} normalized PSD is inversely proportional to I_{ds} from subthreshold to strong inversion region. This feature is a big discriminating difference com-

pared to the carrier number fluctuation number model. Further, Eq. (2-42) can be expressed with the ratio of I_{ds}/g_m ($\approx V_{gt}(1+\theta_1 V_{gt})$) with negligible θ_2 effect,

$$S_{V_{gs}} = \frac{S_I}{{I_{ds}}^2}\left(\frac{I_{ds}}{g_m}\right)^2 = \frac{q\alpha_H}{fW_{eff}L_{eff}Q_{inv}}\left(\frac{I_{ds}}{g_m}\right)^2 = \frac{q\alpha_H}{fW_{eff}L_{eff}C_{ox}}V_{gt}\left(1+\theta_1 V_{gt}\right)^2 \qquad (2\text{-}44),$$

where S_{Vgs} is input gate voltage PSD.[17] Evidently, if θ_1 is much less than one, S_{Vgs} may be linearly varied with V_{gt} and it can be alternatively expressed as below in terms of g_m/I_{ds},

$$\frac{S_I}{{I_{ds}}^2} = \frac{q\alpha_H\left(1+\theta_1 V_{gt}\right)}{fW_{eff}L_{eff}C_{ox}}\left(\frac{g_m}{I_{ds}}\right) \approx \frac{q\alpha_H}{fW_{eff}L_{eff}C_{ox}}\left(\frac{g_m}{I_{ds}}\right) \qquad (2\text{-}45).$$

2.5.2 Carrier number fluctuation model (CNF)

The carrier number fluctuation model based on quantum mechanical tunneling transitions of electrons (or holes) between the channel and traps in the oxide layer was proposed by McWorther in 1957.[59] Hence, the trapping and de-trapping of free charges into traps located in the oxide near interface layer can change the interfacial oxide charge (Q_{ox}), which can be equivalently regarded as V_{FB} fluctuation of MOSFET, $\Delta V_{FB}=-\Delta Q_{ox}/(W_{eff}L_{eff}C_{ox})$ (referring to Eqs (2-37) and (2-39)).[17, 54, 60] The fluctuation of drain current can be then expressed in terms of ΔI_{ds} and ΔV_{FB} if μ_{eff} is assumed to be independent of the insulator charges,

$$\Delta I_{ds} = \Delta V_{FB}\frac{\partial I_{ds}}{\partial V_{FB}} = -\Delta V_{FB} g_m \qquad (2\text{-}46).$$

By accounting for the symmetric role of V_{gs} and V_{FB} (referring to Eq. (2-38)) in the charge conservation equations,

$$\frac{S_I}{{I_{ds}}^2} = S_{V_{FB}}\left(\frac{g_m}{I_{ds}}\right)^2 \qquad (2\text{-}47),$$

where S_{VFB} is the flat band voltage spectra density associated with the interface charge fluctuations of spectral density per unit area (S_{Qox}).[17, 36, 54, 60] Further in detail discussions about the meaning of S_{VFB} and S_{Vgs} will be presented next section. To derive S_{VFB} theoretically, first S_{Qox} is defined by combination with the GR noise model only considering for the case of single trap (see Eqs (2-33) and (2-35)),

$$S_{Q_{ox}} = S_{V_{FB}}{C_{ox}}^2 = \frac{q^2}{{W_{eff}}^2{L_{eff}}^2}4\overline{\Delta N_{ox}{}^2}\frac{\tau}{1+(w\tau)^2} \qquad (2\text{-}48),$$

where ΔN_{ox} and $\overline{\Delta N_{ox}{}^2}$ are the number of fluctuating oxide charges and that of variance, respectively.[36] The variance $\overline{\Delta N_{ox}{}^2}$ can be obtained by taking into account for the probability (f_t, already defined GR noise section),

$$\overline{\Delta N_{ox}{}^2} = f_t(E)(1-f_t(E)) \qquad (2\text{-}49).$$

To get a total PSD arisen from all traps in the oxide, we can simply make an integration with a density of traps $N_t(x,y,z,E)$ in volume and energy. Moreover, the product of $f_t(E)\times(1-f_t(E))$ can be approximated by $\approx -k_B T\, df_t(E)/dE$ near the quasi-Fermi level and N_t is considered as a uniform over the gate area. Then it can be reduced as,

$$\left.\begin{aligned} S_{Q_{ox}} &= \frac{q^2}{W_{eff}{}^2 L_{eff}{}^2}\int_{E_V}^{E_C}\int_0^{W_{eff}}\int_0^{L_{eff}}\int_0^{t_{ox}} 4N_t f_t(E)(1-f_t(E))\frac{\tau}{1+(w\tau)^2}\,dxdydzdE \\ &\approx \frac{q^2 k_B T}{W_{eff} L_{eff}}\int_0^{t_{ox}} 4N_t \frac{\tau}{1+(w\tau)^2}\,dz \end{aligned}\right\} \quad (2\text{-}50),$$

where N_t is the volume traps density in the oxide at the quasi-Fermi level, E_C and E_V are the conduction and valence band edge respectively.[36, 59] Since the basic mechanism of this model is that the drain current fluctuations is mainly attributed to the dynamic trapping and de-trapping of the inversion charges under the gate oxide, the tunneling process can be further applied to Eq. (2-50).[17, 36, 59] The trapping time constant τ_{tunnel} is given for electron tunneling from the channel surface (z=0) to a trap located at a distance (z) in oxide layer as,

$$\tau_{tunnel} = \tau_0(E)\exp\left(\frac{z}{\lambda}\right) \qquad (2\text{-}51),$$

where τ_0 and the tunneling length λ are often taken about 10^{-10}s and 10^{-8}cm for silicon-oxide system, respectively.[36, 59] Based on the Wentzel-Kramers-Brillouin theory, λ can be precisely predicted as following form,

$$\lambda = \left(\frac{4\pi}{h}\sqrt{2m^*\Phi_B}\right)^{-1} \qquad (2\text{-}52),$$

where h is Plank's constant, m^* is effective mass of electron, Φ_B is the tunneling barrier height respectively.[36, 59, 61] Finally, S_{VFB} is expressed through Eqs (2-48) and (2-50)~(2-51),

$$S_{V_{FB}} = \frac{S_{Q_{ox}}}{C_{ox}{}^2} = \frac{q^2 k_B T \lambda N_t}{f W_{eff} L_{eff} C_{ox}{}^2} \qquad (2\text{-}53).$$

Additionally, to automatically determine which model is adequate to interpret LFN characteristics between HMF or CNF, the drain current normalized S_I also can be written as by combination with Eqs (2-47) and (2-53),

$$\frac{S_I}{I_{ds}{}^2} = S_{V_{FB}}\left(\frac{g_m}{I_{ds}}\right)^2 = \frac{q^2 k_B T \lambda N_t}{f W_{eff} L_{eff} C_{ox}{}^2}\left(\frac{g_m}{I_{ds}}\right)^2 \qquad (2\text{-}54).$$

Compared to Eq. (2-45) in HMF, CNF model is clearly proportional to $(g_m/I_{ds})^2$ from weak to

strong inversion region by definition as presented in Fig. 2-21.[17, 18, 60]

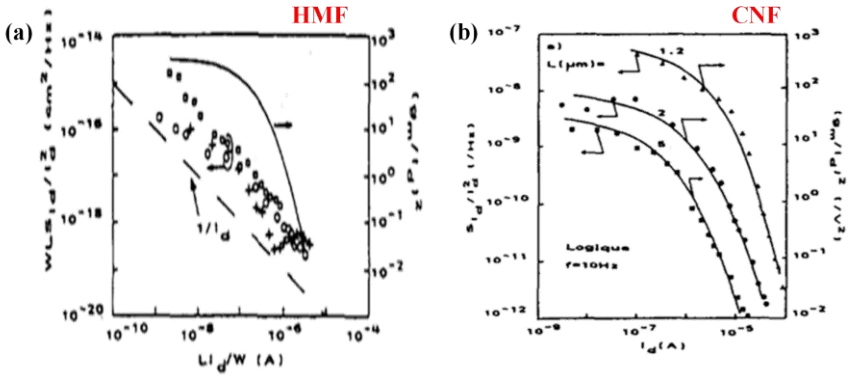

Figure 2-21 Drain current normalized PSD as a function of I_{ds} for (a) P-channel (HMF model) and (b) N-channel (CNF model) MOS device. [18]

Moreover, S_{VFB} actually in Eq. (2-54) is equivalent to S_{Vgs}, however, it is noted by authors in reference [14] that 'ΔI_{ds} in Eq. (2-46) is both induced by inversion charge fluctuations and by mobility fluctuations due the explicit dependence of the mobility on the inversion charge'.[14, 18] To be accounting for this fact, the carrier number with correlated mobility fluctuation model was proposed by G. Ghibaudo in 1991.[17]

2.5.3 Carrier number and correlated mobility fluctuation model

An improve analysis of LFN in MOS transistors based on CNF model was proposed by considering that Q_{ox} may induce a fluctuation of the scattering rate and, therefore, μ_{eff} in the inversion layer.[17] The drain current fluctuation then can be defined as,

$$\Delta I_{ds} = \Delta V_{FB} \left.\frac{\partial I_{ds}}{\partial V_{FB}}\right|_{\mu_{eff}=const} + \Delta \mu_{eff} \left.\frac{\partial I_{ds}}{\partial \mu_{eff}}\right|_{V_{FB}=const} \quad (2\text{-}55),$$

where μ_{eff} is taken from general mobility low ($\mu_{eff}^{-1}=\alpha_C Q_{ox}+\mu_0^{-1}$), α_C is the Coulomb scattering coefficient.[17] Thus, the current fluctuations can be derived from Eq. (2-55),

$$\Delta I_{ds} = -g_m \Delta V_{FB} \mp \alpha_C I_{ds} \mu_{eff} \Delta Q_{ox} \quad (2\text{-}56).$$

The sign of mobility can be decided upon the type of charge trap, negative for acceptor-like or positive for donor-like traps. Based on Eq. (2-56), the drain current normalized S_I then be derived as,

$$\frac{S_I}{I_{ds}^{\ 2}} = S_{V_{FB}} \left(1 \pm \alpha_C \mu_{eff} C_{ox} \frac{I_{ds}}{g_m}\right)^2 \left(\frac{g_m}{I_{ds}}\right)^2 = S_{V_{gs}} \left(\frac{g_m}{I_{ds}}\right)^2 \quad (2\text{-}57).$$

It is clear that if α_C is closed to zero and thus independent of Q_{ox}, the equivalent input gate volt-

age PSD is equal to S_{VFB}. It is the same expression of CNF in Eq. (2-54). On the contrary, if α_C has a high enough, for instance $\alpha_C \approx 10^4$, the slope of the drain current normalized PSD can be varied at strong inversion as displayed in Fig. 2-22.[17, 36]

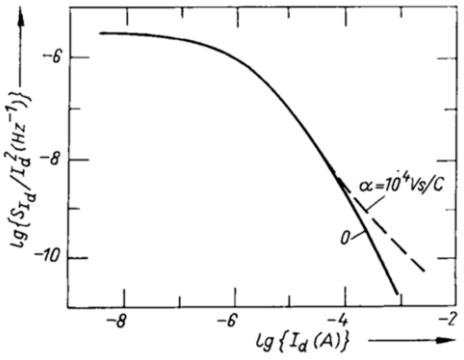

Figure 2-22 Theoretical variation of the I_{ds} normalized PSD in the case of $\alpha_C \approx 0$ and $\alpha_C \approx 10^4$Vs/C, respectively.[17]

2.6 Conclusion

As the size of device is miniaturized, both physical device modeling and parameter extraction become more and more important to provide feedback device information for a performance optimization. To avoid a high risk arisen from heavy fitting procedures, the long channel MOSFET model is in fact used in here for general parameter extraction. Based on basic MOS transistor model, various electrical device parameter extraction methodologies are investigated in terms of V_{th}, μ_{fe}, and R_{sd} etc. Details of YFM are also studied as well. Device characterization methods based the split C-V technique are presented here to evaluate C_{ox}, N_D and the position of V_{FB}, respectively. Furthermore, representative LFN models such as HMF, CNF, and CNF-CMF are theoretically discussed.

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3. Numerical percolation simulation with SPICE simulator

Chapter 3 Abstract

In this chapter, in order to account for the random aspects and percolation phenomena in two-dimensional (2D) conducting nanowire random network, a numerical percolation simulation methodology based on modified Floyd's algorism is presented to find out optimal paths. Besides, to calculate the total resistance, linear and non-linear behaviors of a complex 2D random network, a hybrid methodology with SPICE simulator is also introduced.

3.1 Introduction

Two dimensional (2D) random network thin film transistors (TFTs) have been proposed with the aim of a simple fabrication method and an averaging out the wide device differences arisen from the divergence of the electrical properties of pristine 1D nano-structure.[1-6] Although this approach has overwhelming advantages such as high reproducibility and reliability as a promising candidate for large-scaled, inexpensive, transparent, and flexible electronics, there are urgent needs for better understanding of carrier transport in a random network.[1-4, 6-8] Especially, except for perfectly aligned case, the percolation dominant carrier transport phenomenon has to be accounted for electrical parameter evaluation as displayed in Fig. 3-1.[9, 10] To this end, Flody's algorism[11] based the numerical percolation simulation methodology for 1D conducting nanowires random network will be presented in this section by combination with SPICE simulator for practical application.[9, 10, 12]

Figure 3-1 A representative numerical percolation simulation result for comparison between $L_{mask}=2\mu m$ and $L_{mask}=10\mu m$ with fixed $W_{mask}=5\mu m$ with the fixed nanowire density ($\rho_{NW}=20/\mu m^2$) in random network system.[9]

3.2 Percolation Theory

The concept of percolation in polymerization and gel-formation was statistically studied by Flory and Stockmayer in 1941-1943.[13-15] After Broadbent and Hammersley used the terminology 'percolation process' in 1957 for the first time, when they explained the influence of random aspect on a fluidic system through disordered porous materials.[16] Further, theoretical developments were dramatically carried out to give a better understanding about 'percolation theory' by Domb,[17] Wilson,[18, 19] Fisher and Kadanoff,[20-22] and Madelbrot.[23-25] However, there are many questions still remained to be explained.

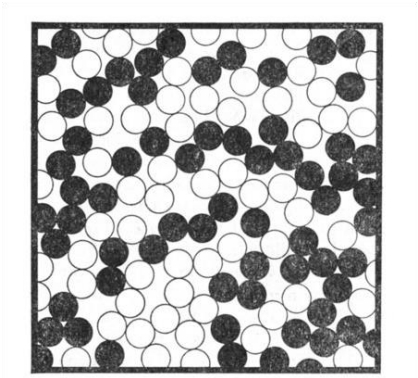


Figure 3-2 Mixture of conducting (black disc) and non-conducting (white disc) grains.[26]

Generally, a percolation model can be defined as a collection of points distributed in space, certain pairs of which are said to be adjacent or linked.[26] There is a simple example to presenting percolation theory, which are dealing with conducting discs as shown in Fig. 3-2. Each disc is distributed as a conducting disc (black) with a probability (p) or non-conducting disc (white) with a probability (1-p), and each event happens independently. With a given p, the probability making a conducting path from top-to-bottom or left-to-right is determined. With a small value of p, a conducting disc percolation path must be rarely happened. However, a conducting disc percolation probability will be increased as p is close to one.

In figure 3-3, there is another example to explain a percolation phenomenon in a two dimensional (2D) system. With a similar trend, the cluster percolating probability is increased as a occupancy probability (p) is increased, ultimately close to one when p is above 0.59.[27] Thus, there must be a critical probability (p_c) in a percolation system, *i.e.* the conducting percolation probability is always zero below p_c or 1 above p_c.[26] Particularly, in a quasi-2D conducting random network system, it might be sensitively depending on a size, a density, an orientation of conducting wires, and a dimension of medium. Thereby, aforementioned parameters will be very important for the device optimization.[2, 4, 9, 12] Additionally, the total conductivity and the transmittance of a conducting wire sheet can be further expected by employing the percolation theory.

In the next section, especially, to account for the random aspects and percolation phenomena in a quasi-2D random network of conducting wires, a simulation methodology will be introduced based on the generation of sets of random arrays followed, for each of them, by the identification of the optimal current paths and their conversion into an equivalent circuit, for SPICE simulation of the I-V characteristics.

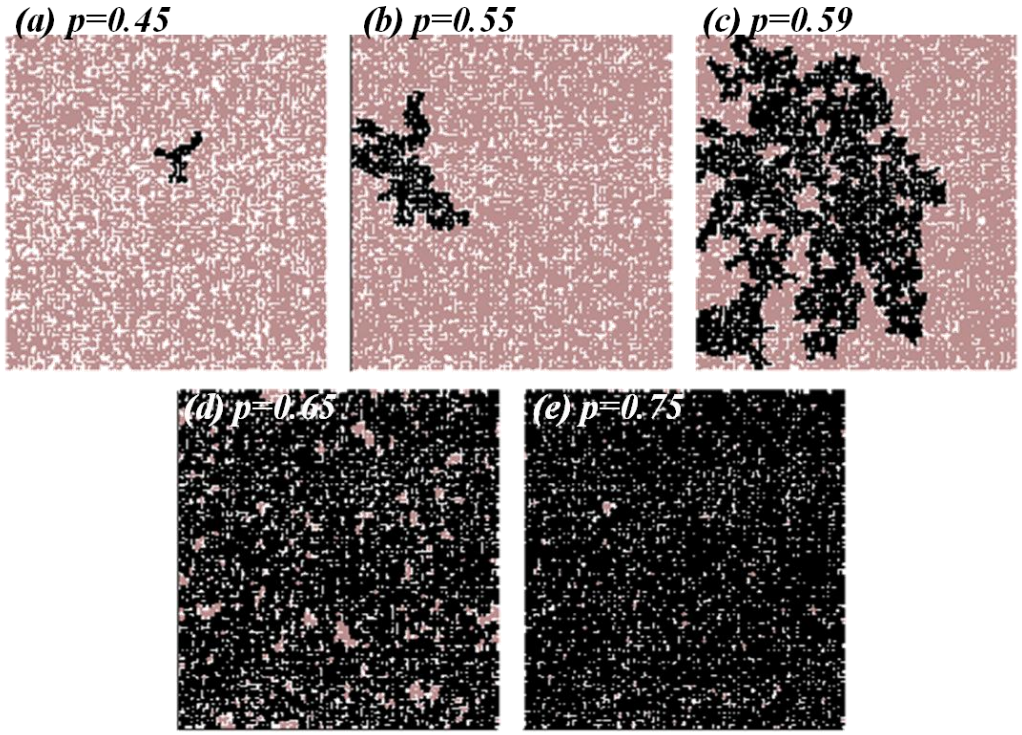


Figure 3-3 Percolation in square lattice with system size L×L=150×150. Occupation probability (a) p=0.45, (b) 0.55, (c) 0.59, (d) 0.65, and (e) 0.75, respectively. From p=0.59, the cluster which percolates from top-to-bottom is observed.[27]

3.3 Numerical Percolation Simulation with Floyd's Algorism

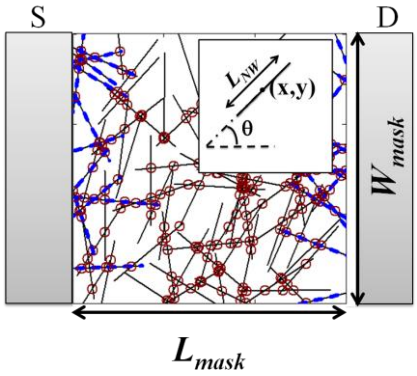


Figure 3-4 A representative realized array set of a 2D RN-CWs with L_{mask}=W_{mask}=3μm with ρ_{CW}=10/μm^2.[10]

A numerical percolation simulation methodology is developed to analyze percolation effects in 2D random networks of homogeneous conducting wires (CWs). The methodology can be extended further to heterogeneous system. For example, the proportion of metallic and semiconducting carbon nanotubes (CNTs) can be modulated if it is needed.[12] In this simulation, however, a 2D random network system of conducting wires (RN-CWs) (black lines in

Fig.3-4) is considered for the aim of simplification. To realize it in a finite 2D system (L_{mask}×W_{mask}; L_{mask} and W_{mask} are active channel mask length and width, respectively), random array sets of center positions (x_i, y_i) and angles to the horizontal axis (θ_i, from -π to π) are generated with a given value of a density of CWs (ρ_{CW}) and the fixed length of CW (L_{CW}=1μm).[10] An example is shown in Fig. 3-4. This method has many advantages for percolation characterizations in terms of the position, the length distribution, and the degree of alignment of one-dimensional CWs.[12] The intersection points (brown circles in Fig. 3-4), which represent junctions between CWs, as well as the distance l_d between adjacent junctions, were then calculated by adjacent matrix technique. Based on matrix information, we can estimate connectivity and optimal path(s) from source electrode (S, left) to drain electrode (D, right) (blue dotted lines in Fig. 3-4) by using modified Floyd's algorithm considering l_d from i^{th} to j^{th} CW. To explain this in detail, let us visit each process step by step as shown in Fig. 3-5.

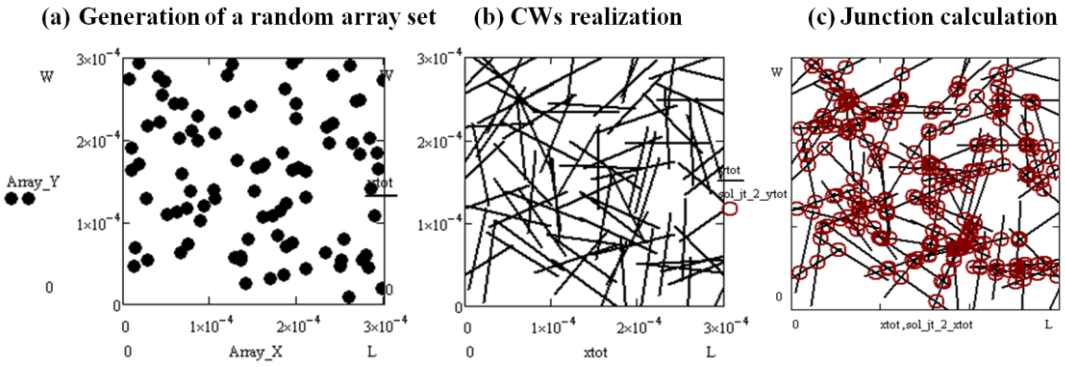


Figure 3-5 One example (L_{mask}=W_{mask}=3μm with ρ_{CW}=10/μm^2) of (a) generation of a random array set of center position (x_i, y_i), (b) CWs realization based on (x_i, y_i, l_i, θ_i), and (c) junction calculation.

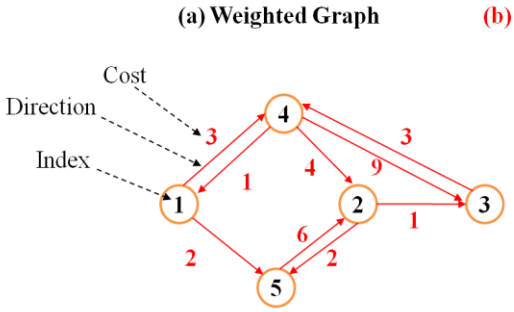
1) **Generation of a random array set** can be accomplished by constructing a parameter list for each segment, for instance, (x_i, y_i, l_i, θ_i) for i^{th} segment.

2) **CWs realization** can be completed by defining the two edges of CW accounting for (x_i, y_i, l_i, θ_i) list.

3) **Junction calculation** between CWs can be then calculated by the iteration of simple linear algebra. The exact solutions have to exist for all lines e.g. CWs provided that any two different CWs are not parallel and the solution is located in CW itself. To precisely determine it, the boundary condition should be precisely examined by the fact that the obtained intersection point is in the ranges of both line segments.

Now, all the matrix information regarding generated CWs in the simulation such as x_i and y_i coordinates for i^{th} CWs, the two edge points of i^{th} CWs, the junction coordinates between

any CWs if they met together is obtained. Hence, it is ready to consider the percolation path probability calculation from light-to-left or top-to-bottom or vice versa depending on user's configuration.[27, 28]



(b) P matrix : Indirect connection through junction position

	1	2	3	4	5
1	0	4	4	0	0
2	4	0	0	3	0
3	4	4	0	0	4
4	0	0	2	0	1
5	4	0	2	3	0

(c) W matrix : Direct connection cost

	1	2	3	4	5
1	0	∞	∞	3	2
2	∞	0	1	∞	2
3	∞	∞	0	3	∞
4	1	4	9	0	∞
5	∞	6	∞	∞	0

Goal

(d) D matrix : The least-expensive cost

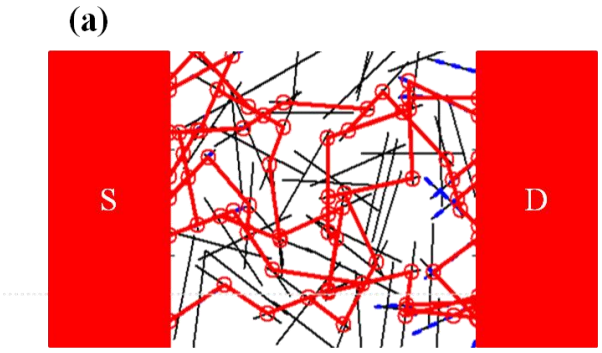
	1	2	3	4	5
1	0	7	8	3	2
2	5	0	1	4	2
3	4	7	0	3	6
4	1	4	5	0	3
5	11	6	7	10	0

Figure 3-6 One simple example of (a) weighted graph, corresponding (b) P, (c) W, and (d) D matrix, respectively.

To this end efficiently, a proper mathematical algorism is needed since computational time and power is exponentially overloaded when the number of CW is increased. For this reason, the modified Flody's algorism is employed in here since it enables to reduce the computational complexity from (n-1)! to n^3, where n is the vertex of adjacent CWs.[11, 28] Indeed, this algorism is designed to solve the least-expensive paths (or shortest paths) among all possible ways with accounting for all junctions in a weighted graph. One simple example is displayed in Fig. 3-6 for better understanding. The term of 'weight' in here means the length between two points. For instance, the distance from point 1 to point 4 can be written in W(1, 4)=3 as seen in Fig. 3-6(c), however, if there is no direct path from i to j index in the weighted graph in Fig. 3-6(a), an infinite value is located in the W matrix cell.[28] Besides, the matrix P is also included to have the junction information of the shortest pathways as presented in Fig. 3-6(b), defined as below expression,[11, 28]

$$matrix\ P = \begin{cases} \max\ index\,(\text{at least one junction exists of the shortest path}) \\ 0\,(\text{no junction exists of the shortest path}) \end{cases}$$

Taking into account for P and W information, the least-expensive cost matrix D (in this case the shortest distance matrix) from i (rows) to j (columns) can be obtained. For example, in case of D(2, 1), there is no direct path but there is indirect path, referred to P(2, 1)=4. Accordingly, the shortest path sequence indeed must be (2, 3, 4, 1) since there is again no direct connection from point 2 to 4 but there is P(2, 4)=3. Hence, the shortest path distance D(2,1)=5 must be the total sum of W(2, 3), W(3,4), and W(4,1).



(b) P_eff =

	0	1	2	3	4	5	6	7	8	9
0	0	13	12	14	14	0	13	13	12	31
1	13	0	6	21	23	12	0	6	6	21
2	13	6	0	14	14	12	0	6	0	21
3	21	21	14	0	0	21	14	14	21	0
4	14	14	14	0	0	14	14	14	14	3
5	0	12	12	14	14	0	12	12	12	31
6	13	0	0	14	14	12	0	0	0	21
7	13	6	6	14	14	12	0	0	6	21
8	13	6	0	14	14	12	0	6	0	21
9	21	21	21	0	3	21	21	21	21	0
10	13	12	12	14	14	0	12	12	12	31
11	13	6	6	14	14	13	0	6	0	21
12	13	6	0	14	14	0	2	6	0	31
13	0	11	12	14	14	0	11	11	12	31
14	13	7	7	4	0	12	7	0	7	21
15	13	11	12	21	14	13	11	11	11	...

(c) Weff =

	0	1	2	3	4
0	0	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
1	$1\cdot10^{20}$	0	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
2	$1\cdot10^{20}$	$1\cdot10^{20}$	0	$1\cdot10^{20}$	$1\cdot10^{20}$
3	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	0	$1.211\cdot10^{-4}$
4	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$7.887\cdot10^{-5}$	0
5	$8.457\cdot10^{-5}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
6	$1\cdot10^{20}$	$8.576\cdot10^{-5}$	$6.81\cdot10^{-5}$	$1\cdot10^{20}$	$1\cdot10^{20}$
7	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
8	$1\cdot10^{20}$	$1\cdot10^{20}$	$6.706\cdot10^{-5}$	$1\cdot10^{20}$	$1\cdot10^{20}$
9	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$8.39\cdot10^{-5}$	$1\cdot10^{20}$
10	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
11	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
12	$1\cdot10^{20}$	$1\cdot10^{20}$	$2.673\cdot10^{-5}$	$1\cdot10^{20}$	$1\cdot10^{20}$
13	$4.213\cdot10^{-5}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$
14	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$2.47\cdot10^{-5}$
15	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	$1\cdot10^{20}$	...

(d) D_eff =

	0	1	2	3	4
0	$6.471\cdot10^{3}$	$4.228\cdot10^{6}$	$2.821\cdot10^{6}$	$8.442\cdot10^{6}$	$7.039\cdot10^{6}$
1	$4.229\cdot10^{6}$	$6.471\cdot10^{3}$	$1.417\cdot10^{6}$	$4.228\cdot10^{6}$	$4.225\cdot10^{6}$
2	$2.825\cdot10^{6}$	$1.419\cdot10^{6}$	$6.471\cdot10^{3}$	$5.634\cdot10^{6}$	$4.23\cdot10^{6}$
3	$8.438\cdot10^{6}$	$4.228\cdot10^{6}$	$5.633\cdot10^{6}$	$6.471\cdot10^{3}$	$1.431\cdot10^{4}$
4	$7.038\cdot10^{6}$	$4.228\cdot10^{6}$	$4.227\cdot10^{6}$	$1.157\cdot10^{4}$	$6.471\cdot10^{3}$
5	$1.194\cdot10^{4}$	$4.227\cdot10^{6}$	$1.415\cdot10^{6}$	$8.441\cdot10^{6}$	$7.037\cdot10^{6}$
6	$2.822\cdot10^{6}$	$1.202\cdot10^{4}$	$1.088\cdot10^{4}$	$4.226\cdot10^{6}$	$2.823\cdot10^{6}$
7	$4.225\cdot10^{6}$	$1.414\cdot10^{6}$	$1.413\cdot10^{6}$	$2.818\cdot10^{6}$	$1.415\cdot10^{6}$
8	$2.821\cdot10^{6}$	$1.419\cdot10^{6}$	$1.081\cdot10^{4}$	$5.633\cdot10^{6}$	$4.23\cdot10^{6}$
9	$7.032\cdot10^{6}$	$2.822\cdot10^{6}$	$5.63\cdot10^{6}$	$1.19\cdot10^{4}$	$1.418\cdot10^{6}$
10	$1.415\cdot10^{6}$	$4.224\cdot10^{6}$	$1.412\cdot10^{6}$	$8.438\cdot10^{6}$	$7.034\cdot10^{6}$
11	$1.415\cdot10^{6}$	$1.415\cdot10^{6}$	$1.414\cdot10^{6}$	$5.629\cdot10^{6}$	$4.226\cdot10^{6}$
12	$1.415\cdot10^{6}$	$2.82\cdot10^{6}$	$8.201\cdot10^{3}$	$7.034\cdot10^{6}$	$5.63\cdot10^{6}$
13	$9.197\cdot10^{3}$	$2.819\cdot10^{6}$	$1.413\cdot10^{6}$	$7.034\cdot10^{6}$	$5.63\cdot10^{6}$
14	$5.628\cdot10^{6}$	$2.818\cdot10^{6}$	$2.817\cdot10^{6}$	$1.412\cdot10^{6}$	$8.069\cdot10^{3}$
15	$1.413\cdot10^{6}$	$2.818\cdot10^{6}$	$1.413\cdot10^{6}$	$5.634\cdot10^{6}$	...

Figure 3-7 (a) Optimal pathways from S to D in a test set of Fig. 3-5, and corresponding (b) P, (c) W, and (d) D matrix, respectively.

Based on such matrix information of RN-CWs, we can now determine the percolation connectivity and estimate the shortest path and/or less resistive path, namely optimal path(s) from S to D (red lines in Fig. 3-7(a)), by using an aforementioned modified Floyd's algorithm with account for the number of junction (N_{jc}), the conducting path resistance (R_{path}), and the total length of a single conduction path (L_{path}) from the i^{th} to the j^{th} CW connected to S and D, respectively (see the blue dotted lines in Fig. 3-7(a)). To have a percolation probability (P_p), we further assumed that generated CWs have a different resistance depending on their effective contribution to the conduction channel length l_d along L_{path}. There is a theoretical model of CNT for this resistance, simply defined as $R_{CW}(l_d)=(4q^2/h)^{-1}(1+l_d/\lambda_{CW})$ in the high gate bias regime, where h and λ_{CW} are the Planck constant and mean free path of CNT as a reference value, respectively.[29] Moreover, all junction resistances R_{jc} are assumed to be identical with a median

value taken from previous experimental results obtained between semiconducting CNTs, $R_{jc}=(0.01q^2/h)^{-1}$.[30] By this manner, P_p was repeatedly computed in terms of L_{mask}, W_{mask}, and ρ_{CW} in 2D finite system, as plotted in Fig. 3-8. The results were well fitted with the modified error function (erf) defined as follows,

$$P=\frac{1}{2}\left(1+erf\left(\frac{x-\rho_{th}}{C}\right)\right),\ erf(x)=\frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}dt \qquad (3\text{-}1),$$

where ρ_{th} and C is the percolation threshold and $\sigma\sqrt{2}$ respectively, where σ is the standard deviation of distribution density. Results clearly indicate that the percolation process is following a standard Gaussian distribution and that there is a much stronger dependency on W_{mask} than L_{mask}.

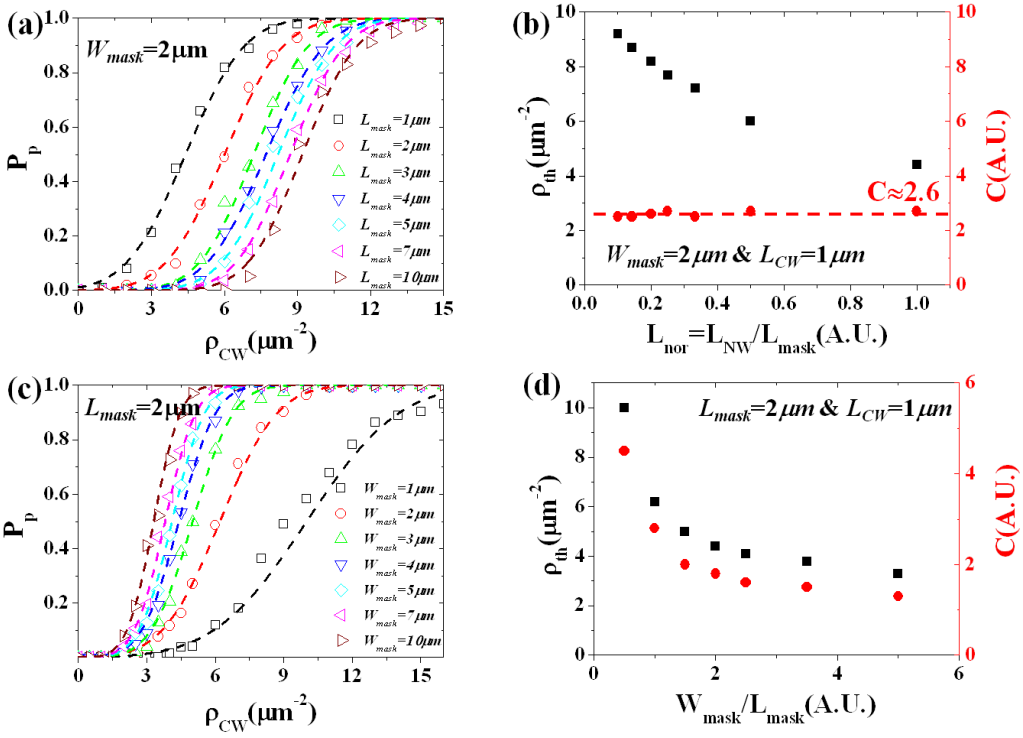


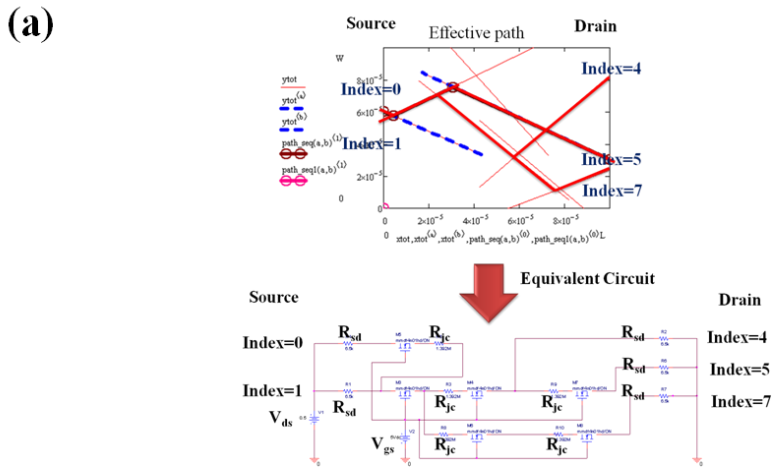
Figure 3-8 Percolation probability (P_p) variation with ρ_{CW} as a function of L_{mask} for fixed W_{mask}=2μm, and (b) corresponding *erf* fitting parameters. Figs (c) and (d) are the same figure as a function of W_{mask} with fixed L_{mask}=2μm.[10]

For further practical applications, we employed SPICE simulator to calculate the total resistance and even the full range of linear and non-linear FET characteristics of 2D random network systems, depending on user-defined models and application-defined criteria.

3.4 SPICE (simulation program with integrated circuit emphasis) Simulation

SPICE simulator developed at the University of California Berkeley in 1971 has been employed for complex circuit analysis including active and passive devices for various purposes of users.[12, 31, 32] To verify the circuit or transistor performance, it is highly required to simulate the designed circuit before device fabrication since it is very easy to access and a powerful tool to find a solution.

Therefore, in order to take advantage of these virtues, numerically generated sets of RN-CWs should be converted to a netlist for SPICE simulator. (In here, Cadence P-spice commercial simulator is employed) As an example, a test set of RN-CWs was generated and its corresponding electrical equivalent circuit was designed to prove the validity of their netlist as presented in Figs 3-9 (a) and (b). P-spice simulation results processed by both netlists show a perfect agreement as seen in Fig. 3-9(c). Accordingly, it enables to further extend the versatility of this simulator tool, such as calculation of the total resistance and even the full range of linear and non-linear FET characteristics of 2D random network systems, depending on user-defined models and application-defined criteria. To demonstrate this, typical $I_{ds}(V_{gs})$ and $I_{ds}(V_{ds})$ FET characteristics, simulated for the generated RN-CWs ($L_{mask}=W_{mask}=3\mu m$) are also plotted in Figs 3-10(a) and (b) for different values of ρ_{CNT}. The linear and non-linear behaviors of test sets of RN-CWs are successfully monitored



(b)

Automatically generated Mathcad netlist

```
X_MN7 N7H NS2 N7T mmdf4n01hd/ON
X_MN5 N5H NS2 N5T mmdf4n01hd/ON
X_MN4 N4H NS2 N4T mmdf4n01hd/ON
X_MN3 N3H NS2 N3T mmdf4n01hd/ON
X_MN1 N1H NS2 N1T mmdf4n01hd/ON
X_MN0 N0H NS2 N0T mmdf4n01hd/ON
V_V2 NS2 0 5Vdc
V_V1 NS1 0 0.05
R_RNS11 NS1 N1H 6.470703125k
R_RNS10 NS1 N0H 6.470703125k
R_RN70 N7T 0 6.470703125k
R_RN50 N5T 0 6.470703125k
R_RN45jc N4T N5H 1.392181581439 39M
R_RN40 N4T 0 6.470703125k
R_RN37jc N3T N7H 1.392181581439 39M
R_RN14jc N1T N4H 1.392181581439 39M
R_RN13jc N1T N3H 1.392181581439 39M
R_RN01jc N0T N1H 1.392181581439 39M
*copyright M.K.JOO
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Pspice netlist

```
* source PERCOLATION
X_M8    N10647 N10215 N10635 mmdf4n01hd/ON
X_M6    N10399 N10215 N10439 mmdf4n01hd/ON
R_R11   N10573 N10647 1.392M
R_R6    N10291 N10399 6.5k
V_V1    N10291 0 0.5
X_M9    N10693 N10215 N10701 mmdf4n01hd/ON
R_R7    N10439 N10303 1.392M
V_V2    N10215 0 5Vdc
R_R12   N10697 N10693 1.392M
R_R8    N10635 0 6.5k
X_M4    N10303 N10215 N10345 mmdf4n01hd/ON
R_R9    N10701 0 6.5k
R_R3    N10291 N10303 6.5k
R_R10   N10345 N10553 1.392M
R_R4    N10573 0 6.5k
X_M7    N10553 N10215 N10697 mmdf4n01hd/ON
X_M5    N10341 N10215 N10573 mmdf4n01hd/ON
R_R5    N10345 N10341 1.392M
```

(c)

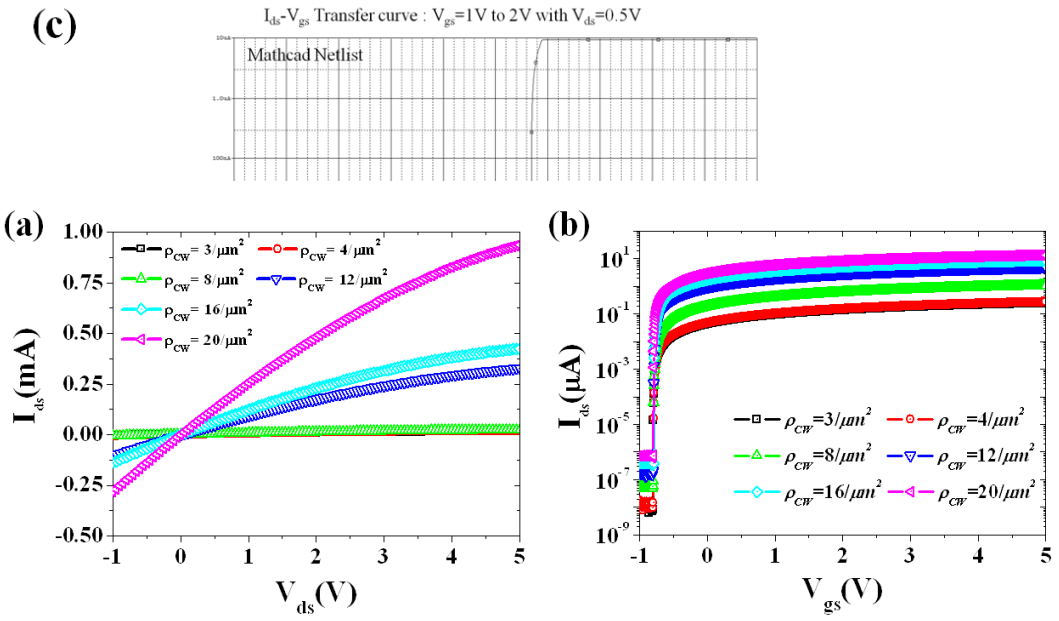

Figure 3-10. SPICE simulation results of output characteristics $I_{ds}(V_{ds})$ and transfer curve $I_{ds}(V_{gs})$ curves depending on different ρ_{CW} (L_{mask}=W_{mask}=3μm)

3.5 Conclusion

We introduced a methodology to simulate 2D random networks of CNTs and, by combination with SPICE simulation, to simulate their electrical properties. This methodology was demonstrated with various geometry factors. Percolation probability was simulated and its dependence to ρ_{CW} was well-fitted with an error function. Moreover, to find out the optimal current paths into complex connectivity patterns, we accounted for a detailed electrical model including the resistivity of each conductive segment in each path, number of junctions, junctions and contact resistances (with parameters l_d, N_{jc}, R_{jc} and the series resistance R_{sd}). Finally, to extend usability and accessibility, a SPICE simulator was employed. To do this, test sets of RNCWs were converted into their equivalent electrical circuits and simulated. This methodology is versatile and can be used for 2D random network systems based on conducting NWs, CNTs, nano-fibers and composites, for many electronic applications such as thin film transistors, bio/gas sensors and transparent electrodes. Given an equivalent model for the elementary nanostructure involved in the network, our methodology permits an electrical study of random networks of such nanostructures which can be directly applied for practical application.

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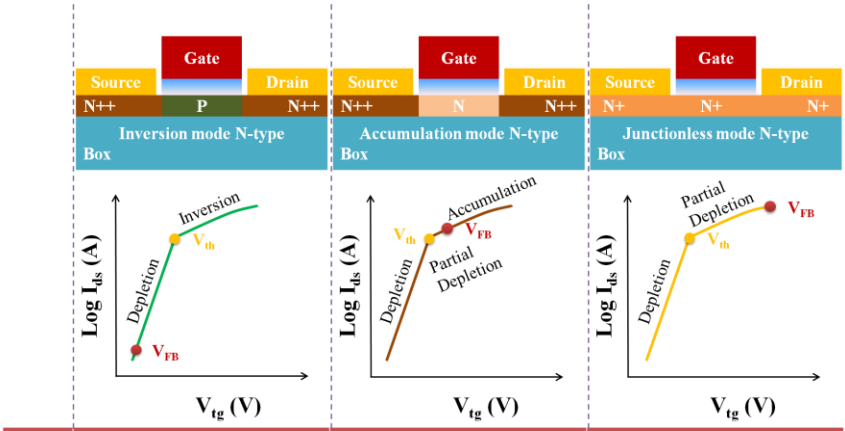
4. Flat-band voltage and low-field mobility analysis of junctionless transistors under low-temperature

Chapter 4 Abstract

This chapter presents the low-temperature characteristics of flat-band (V_{FB}) and low-field mobility in accumulation regime (μ_{0_acc}) of junctionless transistors (JLTs). To this end, split capacitance-to-voltage (CV), dual gate coupling and low-temperature measurements were carried out to systematically investigate V_{FB}, the gate oxide capacitance per unit area C_{ox} and the doping concentration N_D, respectively. With account for the position of V_{FB} and the charge based analytical model of JLTs, bulk mobility (μ_B) and μ_{0_acc} were separately extracted in volume and surface conduction regime, respectively. Finally, the role of neutral scattering defects was found the most limiting factor concerning the degradation of μ_B and μ_{0_acc} with gate length in planar and tri-gate nanowire JLTs.

4.1 Introduction

Junctionless transistors (JLTs) recently gained much interest as a promising candidate device due to its figure of merits over improved short-channel operation such as reduced threshold voltage (V_{th}) roll-off and drain induced barrier lowering (DIBL).[1, 2] For instance, recently scaled tri-gate nanowire JLTs down to 13nm gate length (L_m) were successfully demonstrated with overall good electrical performances.[3] Moreover, in contrast with the inversion-mode (IM) transistors, the majority carriers can carry the current, and an ultra sharp p-n junction between silicon channel and source(S)/drain(D) is no more required because it consists of the constant doping concentration from S to D, *i.e.*, n^+(S)-n^+(silicon channel)-n^+(D). As a result, the cost of device fabrication and the complexity of process can be much reduced compared to IM transistors. However, to successfully realize this junctionless gated resistor as a next generation device to replace IM transistors, a high doping concentration (N_D for N-type and N_A for P-type, respectively) with a good doping uniformity over silicon channel and S/D region are needed to get a desired current level to be employed in practical applications. Moreover, narrow and shallow silicon film thickness (t_{si}) is also required as well to turn this device fully off.[1]



	Inversion Mode	Accumulation Mode	Junctionless Mode
OFF	Surface subthreshold current	Body subthreshold current	Body subthreshold current
ON	Surface inversion channel	Small body current & Surface Accumulation channel	Body current

Figure 4-1 Comparison of conduction mode of advance MOS transistors (Left: Inversion mode, Middle: Accumulation mode, Right: Junctionless mode)

In operation principle of JLTs, three conduction regions can be defined with respect to the top gate voltage (V_{tg}), 1) full depletion region ($V_{tg} \leq V_{th}$), 2) partially depleted region ($V_{th} \leq V_{tg} \leq V_{FB}$), and 3) accumulation region ($V_{FB} \leq V_{tg}$) respectively, where V_{FB} is the flat-band voltage. Particularly, the conduction channel of JLTs in the partially depleted region is the main conduction regime and it is created from the center of neutral silicon body.(See Fig. 4-1) In ad-

dition, when the whole silicon channel is fully opened at V_{FB} condition, the majority carriers can flow through the entire neutral silicon volume with the released surface effects such as surface roughness scattering and high gate field to the channel, since the carriers are subjected to the zero perpendicular field.[1] Even though JLTs operated in volume conduction, it cannot fully prevent the low frequency noise sources stemming from carrier trapping-detrapping in slow traps located in the gate dielectric,[4, 5] these aforementioned features in principle can be regarded as strong advantages of JLTs for high-speed circuit and low-noise applications compared to IM transistors. Besides, if V_{tg} regime is larger than V_{FB}, the majority carriers will be accumulated below the surface of the front gate dielectrics, *i.e.*, similarly to accumulation mode fully depleted silicon on insulator (FD-SOI). Therefore, various electrical basic parameters such as V_{th}, V_{FB}, and N_D or N_A must be important to evaluate the performances of JLTs, especially for the carrier mobility depending on their conduction region.

Focusing on the temperature characteristics of JLTs, although many low- and high-temperature specific properties of JLTs were already studied, the temperature and dual gate (top and bottom) coupling dependence of low-field mobility (μ_0), V_{th} and V_{FB} were not fully investigated yet.[6-10] In particular, it should be noted that the extraction of μ_0 of heavily doped JLTs in accumulation region by employing the Y-Function method (YFM) might be difficult. It is because that the effective contribution of volume conduction to the drain current is increased as the target doping concentration is increased, resulting in insufficient fitting range to determine the second linear slope of YFM.[11, 12] Moreover, field-effect mobility (μ_{fe}) obtained from the maximum value of the transconductance (g_m) was also risky if one wants to use the oxide capacitance per unit area (C_{ox}) when the position of V_{tg} corresponding to the maximum value of $g_m(V_{tg})$ was located in below V_{FB}.

In this chapter, to precisely analyze the fundamental device parameters such as V_{FB}, N_D, a capacitance equivalent thickness (CET), and C_{ox}, split capacitance-to-voltage (CV) measurement was carried out by analyzing the result of gate-to-channel capacitance (C_{gc}). Top and bottom dual gate coupling measurement under low-temperature also performed to identify the position of V_{FB} as function of gate length L_m. Based on the position of V_{FB}, the bulk channel mobility (μ_B), and the low-field mobility in accumulation regime (μ_{0_acc}) were separately determined by taking into account for the charge based analytic model and YFM, respectively. Moreover, to have a better understanding about a scattering mechanism concerning the degradation of μ_{0_acc} in short channel device (below L_m=100nm), a quantitative mobility analysis and the temperature dependence of subthreshold-swing (SS), and series contact resistance at V_{FB} (R_{sd_FB}) are presented.

4.2 Device Fabrication Process and Electrical Measurement Conditions

Fabrication of JLTs: For this study, various channel geometry of N-type devices were fabricated at CEA-LETI on (100) SOI wafers on 145nm thick buried oxide (BOX) with high-κ/metal gate stack. After thinning of silicon body, t_{si} was measured about 9nm by a scanning electron microscope (SEM) and a high resolution transmission electron microscope (HRTEM) images. (See Figs 4-2(a) and (b)) The targeted phosphorous doping concentration for N-type JLTs was $4\sim5\times10^{19}$ cm^{-3}, which is much heavily doped device compared to previously studied in JLTs.[5, 10, 12, 13] With properly chosen implant energy and dose, implantation was performed to the entire silicon body to have a uniform doping concentration. Moreover, additional doping implantation was carried out between silicon channel and S/D to construct S/D extension region for the enhancement of the contact property by reducing a channel access resistance. The gate stack composes of silicon oxide (SiO_2), HfSiON, TiN, and polysilicon layers with the equivalent oxide thickness (EOT≈1.3nm). Three-dimensional device structure and on-mask splits (L_m and mask width (W_m)) are displayed in Figs 4-3(a) and (b), respectively.

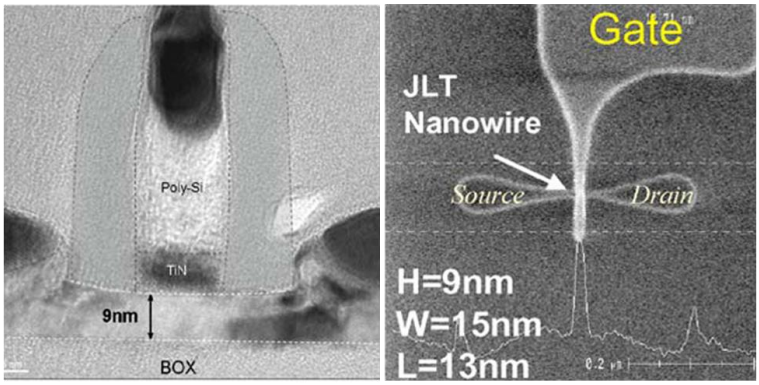


Figure 4-2 Representative (a) TEM and (b) SEM images of cross-sectional tri-gate nanowire JLTs.[3]

Electrical Characterizations: The IV current-to-voltage characteristic depending on V_{tg} and bottom gate potential (V_{bg}) under low-temperature ranging from 77K to 350K were measured from HP 4156a at fixed drain voltage V_{ds}=50mV for varied L_m and W_m. In the split CV technique, $C_{gc}(V_{tg})$ characteristics were obtained by connecting top gate electrode to the "high" terminal with AC small signal amplitude (=50mV) at 500kHz and both S and D electrodes to the "low" terminal by using 4294a while V_{bg} varied from -30V to 30V.[14]

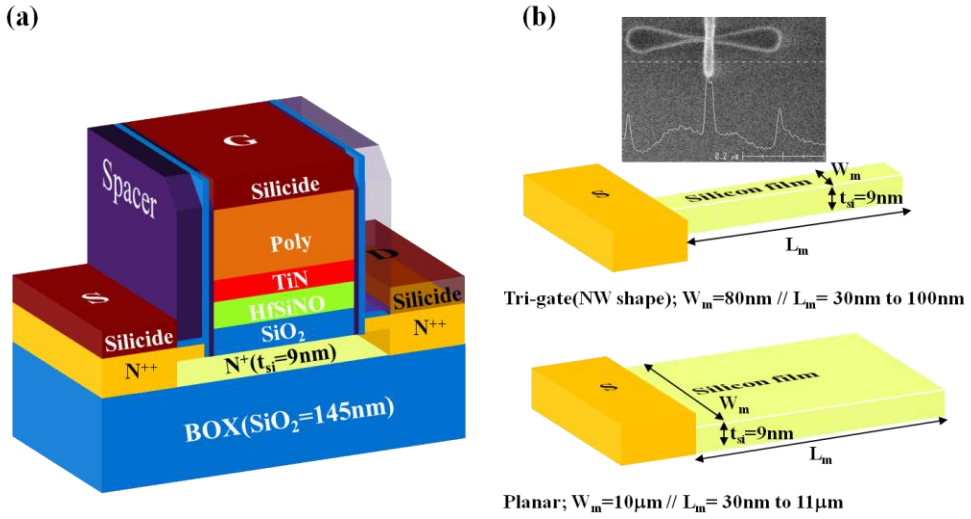


Figure 4-3 (a) Simplified three-dimensional device structure and (b) on-mask splits (L_m and W_m) for planar and nanowire(NW) shape of JLTs with a representative SEM (Scanning Electron Microscope) image of NW JLT

4.3 Experimental Results and Discussion

4.3.1 Split Capacitance-to-Voltage Characteristics of JLTs

To have a fundamental but critical information based on CV characteristics such as V_{FB}, N_D, and CET, $C_{gc}(V_{tg})$ measurement for N-type planar JLTs was performed for a precise device performance evaluation at room temperature. So far, many methods were employed to extract such above stated parameters for bulk silicon, IM, and FD-SOI transistors by measuring the CV curves from depletion to accumulation and/or inversion, and extracting V_{FB}, CET, and doping concentration using Maserjian's function.[15-17] Before deeper analysis of JLTs under low-temperature, a brief discussion and confirmation of above mentioned parameters should be essentially addressed by comparing CV results depending on different methods.

4.3.1.1 C_{ox}, CET, mask channel length and width reduction (ΔL_m and ΔW_m) extraction

Typical $C_{gc\_max}(V_{tg})$ curves of planar JLTs (L_m=150nm to 11μm with W_m=10μm) after elimination of parasitic capacitances taken at the minimum $C_{gc}(V_{tg})$ are plotted in Fig. 4-4(a). Two humps can clearly be seen, indicating the distinct formation of bulk and surface conduction channel, respectively. To get the reduction of channel length (ΔL_m) by assuming that C_{ox} ($=\varepsilon_0\varepsilon_r/t_{ox}$, where t_{ox} is the oxide thickness, ε_0 and ε_r are the vacuum and the relative permittivity, respectively) should be constant, the linear relationship between C_{gc_max} and L_m is considered in this study. As displayed in Fig. 4-4(b), $\Delta L_m \approx 42$nm for long channel ($150\text{nm} \le L_m \le 11\mu\text{m}$) and $\Delta L_m \approx 8$nm for short channel ($30\text{nm} \le L_m \le 100\text{nm}$) were simply computed by the linear extrapola-

tion method, respectively. It is not shown in here though, the reduction of channel width ΔW_m (≈70.4nm, TEM measured mean value is around 65.7nm) was also found from W_m splits. Besides, CET (≈1.69nm by assuming that t_{ox} is uniform over silicon channel) and C_{ox} (≈2.05μF/cm^2) were also estimated based on the effective L_{eff} (=L_m-ΔL_m) and W_{eff} (=W_m+2t_{si}-ΔW_m) as well. This is the most classic and popular approach in IM and FD-SOI transistors. But there is a possibility for overestimation of t_{ox} when it is ultrathin.[16, 18] Hence, to avoid this undesired situation, the improved methods were employed, *i.e.*, the y-axis intercept extrapolation by plotting $1/C_{gc\_eff}(V_{tg})$ vs. $1/(V_{tg}-V_{FB})$, where C_{gc_eff} (=$C_{gc\_max}/W_{eff}L_{eff}$) is C_{gc_max} per unit area.

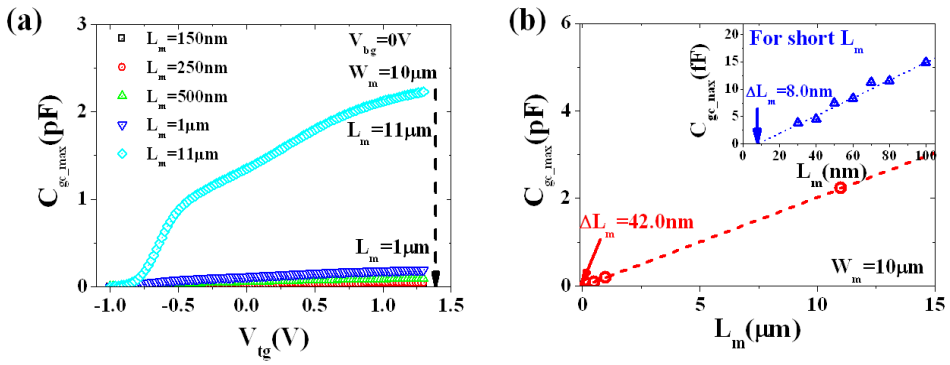


Figure 4-4 (a) Representative $C_{gc\_max}(V_{tg})$ curves for N-type JLTs (L_m=150nm to 11μm with fixed W_m=10μm). (b) C_{gc_max} versus and L_m for extraction of ΔL_m (≈42nm). (Inset: Same data procedures in short channel JLTs (L_m≤100nm) for ΔL_m (≈8nm) evaluation).

4.3.1.2 Improved methodology for C_{ox}, CET, N_D and N_A evaluation in ultra thin body

In accumulation region of JLTs, $C_{gc\_eff}(V_{tg})$ can be described by simply two capacitors in series, namely, C_{ox} and C_{sc} (semiconductor capacitor per unit area). The relation between all capacitance values can be simply expressed as,

$$\frac{1}{C_{gc\_eff}(V_{tg})} \approx \frac{1}{C_{ox}} + \frac{1}{C_{sc}} \approx \frac{1}{C_{ox}} + \frac{\alpha}{(V_{tg}-V_{FB})^n} \quad (4\text{-}1),$$

where α is a constant and n is an exponent depending on the accumulation layer carrier statistics.[16, 18] Although the exponent *n* should be carefully chosen with respect to the system of carrier statistics, here *n*=1 was used as for Boltzmann's statistics, since it provides a safe fitting range to get a linear line in such planar type of $C_{gc\_eff}(V_{tg})$. With aforementioned considerations, C_{ox} can be extracted from the y-axis intercept of Eq. (4-1). Besides, the below theoretical equation was considered to determine V_{FB} in advance as an initial trial,

$$V_{FB} = \Phi_{MS} = \Phi_M - \left[\chi + \frac{E_g}{2} - \frac{k_B T}{q}\ln\frac{N_D}{n_i}\right] \quad (4\text{-}2),$$

where Φ_M, χ, E_g, k_B, T, q, and n_i denote the work function of gate metal, the electron affinity, the Boltzmann constant, the absolute temperature, the electron unit-charge, and the intrinsic carrier concentration, respectively.[12, 19] Calculated V_{FB} values are ranging from 0.57 to 0.58 (V). As displayed in Fig. 4-5(a), it clearly shows a good linearity and well fitted by Eq. (4-1) at very high V_{tg} regime (fully accumulated regime). $1/C_{gc\_eff}$ behaviors and the extracted $1/C_{ox}$ values almost seem to be similar to each other regardless of V_{bg} in accumulation region. Based on these findings, C_{ox} and corresponding CET were found and it was approximately overestimated ≈0.2nm as expected from previous section. This overestimation could be interpreted by the fact that V_{tg} ranged used for $C_{gc}(V_{tg})$ was not sufficient to get a full formation of accumulation layer at front-interface. Indeed, the second plateau in Fig. 4-4(a) can be seen but not very clearly. Hence, to overcome the maximum V_{tg} range limited by the breakdown voltage of the gate dielectrics, $1/C_{gc\_eff}$ method can be considered as an improved method compared to the typical maximum C_{gc_max} calculation for a precise evaluation of C_{ox}, especially for such heavily doped devices.

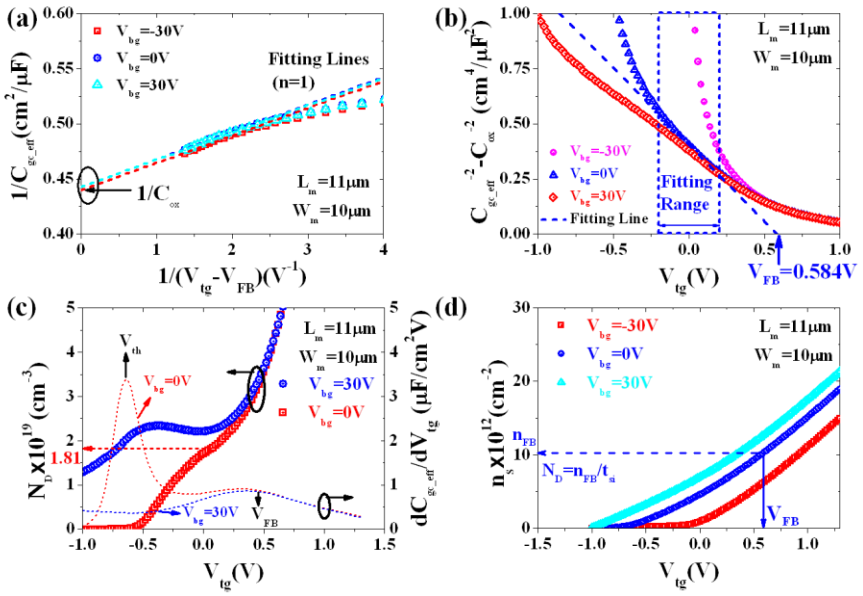


Figure 4-5 (a) $1/C_{gc\_eff}$ of N-type JLTs (L_m=11μm with W_m=10μm) with respect to V_{bg} (-30V to 30V) for C_{ox} and corresponding CET extraction in high V_{tg} regime. (b) $1/C_{gc\_eff}^2$-$1/C_{ox}^2$ of N-type of JLTs for V_{FB} evaluation in partially depleted region (c) N_D based on Eq. (4-4) (left axis) and dC_{gc_eff}/dV_{tg} (right axis) curves of N-type of JLTs. (d) n_s versus V_{tg} curves for N_D estimation with account for the position of V_{FB}.

Further, $1/C_{gc\_eff}^2$ (see Fig. 4-5(b)) technique was employed to determine V_{FB} and N_D in partially depletion region with C_{ox} evaluated by Eq. (4-1).[18] It is defined as below expression,

$$\left(\frac{1}{C_{gc\_eff}(V_{tg})}\right)^2 - \frac{1}{C_{ox}{}^2} \approx \frac{2}{q\varepsilon_{si}N_D}(V_{tg} - V_{FB}) \qquad (4\text{-}3),$$

where ε_{si} is the permittivity of silicon. To decide a proper fitting range, V_{bg} from -30V to 30V was applied. When V_{bg} is increased (positive direction), the partially depleted regime is extended as plotted in Fig. 4-5(b). As a result, it is possible to set a fitting range and determine the position of V_{FB} (≈0.58(V)) without difficulties. The extracted V_{FB} is quite consistent with theoretical value and all curves are merged together after using actualized V_{FB} values regardless of V_{bg} condition. From the linear slope of $1/C_{gc\_eff}{}^2$, N_D was easily obtained. However, to reduce errors originated from fitting process, Eq. (4-3) was differentiated as below,

$$\frac{\partial}{\partial V_{tg}}\left(\frac{1}{C_{gc\_eff}(V_{tg})^2}\right) = \frac{2}{q\varepsilon_{si}N_D} \Rightarrow N_D = \frac{2}{q\varepsilon_{si}\dfrac{\partial}{\partial V_{tg}}\left(\dfrac{1}{C_{gc\_eff}(V_{tg})^2}\right)} \qquad (4\text{-}4).$$

This expression, consequently, is the same as Maserjian's function after rearrangement of differentiation term in Eq. (4-4). By this way, N_D was simply determined without reliance of V_{FB} and C_{ox} in partially depleted region as presented in Fig. 4-5(c). It should be noted that such values should be chosen on the plateau of plots. Moreover, with a small geometry and/or with a low channel doping concentration, it is sometimes difficult to find it. Therefore, to select the extraction position for N_D appropriately, another technique was used to localize V_{th} and V_{FB}, the derivative of C_{gc_eff} (dC_{gc_eff}/dV_{tg}). As presented in Fig. 4-5(c) with the right y-axis, two peaks are clearly appeared in dC_{gc_eff}/dV_{tg} when V_{tg} is increased from negative to positive. The first peak (left side) represents V_{th}, the turn-on voltage from the full depletion to the partially depletion region and the latter one (right side) indicates V_{FB}, respectively. In V_{tg} range between V_{th} and V_{FB}, N_D (≈1.8×10^{19} cm^{-3}) was properly determined, approximately ≈40% of the targeted channel doping concentration (4~5×10^{19} cm^{-3}). This tendency shows a similar trend of the previous results extracted from lower doping concentration.[12] Alternatively, the channel doping concentration can be also estimated by using the sheet carrier density ($n_s=\int[C_{gc\_eff}(V_{tg})/q]dV_{tg}$) and t_{si} at the position of V_{FB} (selected from $1/C_{gc\_eff}{}^2$ results) when V_{bg}=0V as displayed in Fig. 4-5(d). This figure well indicates accumulation/depletion charges induced by V_{bg} In addition, the results were quite comparable to those extracted from Maserjian's function. The tiny differences might be attributed to errors originated from the used values of V_{FB} and/or t_{si}.

Finally, all parameters which handled in this section were summarized in Table 4-1 depending on the used method. Whole analyzing procedures clearly indicates that CV characteristics based on $C_{gc}(V_{tg})$, $C_{gc\_eff}{}^{-1}$, $C_{gc\_eff}{}^{-2}$ including Maserjian's function can provide useful information and it proves the qualification of C_{ox}, ΔL_m, ΔW_m, V_{FB}, and N_D for the further electrical

parameter evaluation.

Method/Parameters	C_{ox} [μF/cm²]	CET [nm]	V_{FB} [V]	N_D [cm⁻³]
Split CV	2.05	1.69	×	×
$1/C_{gc\_eff}$	2.26	1.53	×	×
$1/C_{gc\_eff}^2$ and (Maserjian's Function)	×	×	0.584	1.81×10^{19}
dC_{gc_eff}/dV_{tg}	×	×	0.32	×
$n_s/t_{si}\approx[\int C_{gc\_eff}/qdV_{tg}]/t_{si}$	×	×	×	1.06×10^{19}

Table 4-1 Summarized table of evaluated parameters, C_{ox}, CET, V_{FB}, and N_D depending on different method. (Underlined values will be used for further electrical parameter evaluation)

4.3.2 Low temperature I-V characteristics

In this section, W_m=10μm planar and 80nm tri-gate nanowire N-type JLTs are only considered. Drain current (I_{ds}) as a function of V_{tg} at V_{ds}=50mV for short channel (L_m≤100nm) devices was measured under low-temperature varied from 77K to 350K. Figures 4-6(a) and (b) show the obtained representative linear and log-scaled $I_{ds}(V_{tg})$ of L_m=30nm and 100nm with W_m=10μm, respectively. Interestingly, the temperature (T) independent points, namely, the "zero-temperature-coefficient" (ZTC),[20] were observed in all devices as presented in inset of Fig. 4-6(b). It seems to be contrary to the previously reported N-type nanowire JLTs, however, it can be mainly explained by the higher temperature dependence of V_{th}, $\partial V_{th}/\partial T$ =-1.63mV/K than that of presented devices ($\partial V_{th}/\partial T$ =-0.5mV/K, see Fig. 4-8(a)).[6, 8] In general, ZTC is closely related with the temperature dependence of V_{th} and the carrier mobility, *i.e.*, ZTC can be found when these two factors are increased while T is decreased. This is the case (see Figs 4-8(a) and 4-10(b) for the temperature dependence of V_{th} and the carrier mobility, respectively). In addition, ZTC depending on V_{bg} is also measured as displayed in inset of Fig. 4-6(b). Especially, the point of ZTC is quite similar regardless of L_m at V_{bg}=-30V. If these features were exploited with appropriate dual-gate conditions, it can be utilized for the temperature independent current source/voltage sources. Further dual-gate characteristics of JLTs are presented in the section. 4.3.3.

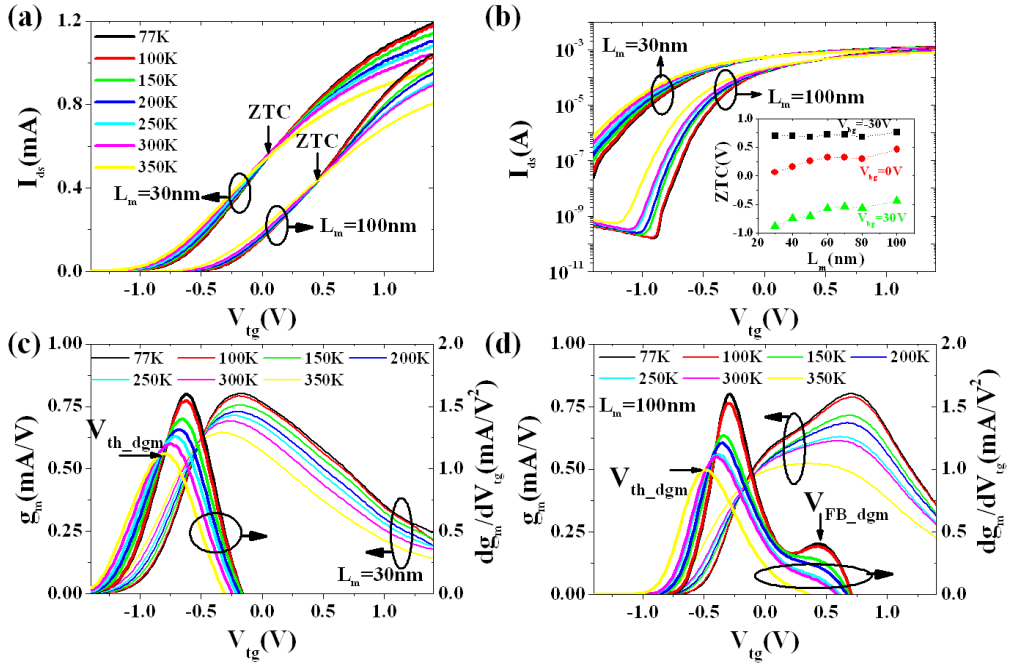


Figure 4-6 The representative (a) linear and (b) log scaled transfer curves in L_m=30nm and 100nm JLTs with varying T (77K to 350K). (Inset: ZTC versus L_m depending on V_{bg}) The temperature dependence of g_m (left axis) and dg_m/dV_{tg} (right axis) of (c) L_m=30nm and (d) L_m=100nm JLTs, respectively.

To investigate the temperature dependence of V_{th} and V_{FB}, the derivative of g_m method (dg_m/dV_{tg}) was used in this study.[12, 19] For instance, according to the Ref. [12], this method can provide relevant information about V_{th} and V_{FB}, and even more accurately than other methods such as the linear extrapolation of $I_{ds}(V_{tg})$ and YFM in this specific case. In principle, it is noted that YFM can provide various electrical parameters such as μ_0 and V_{th} without series resistance R_{sd} effects.[11, 14] However, in the case of such heavily doped JLTs, it is difficult to reach the range of V_{tg} where the deep accumulation slope can be extracted reliably. This is why the classical method was employed alternatively to define the position of V_{th}. Therefore, it should be kept in mind afterwards that V_{th} extracted from dg_m/dV_{tg} method can be influenced by R_{sd}. In the case of L_m=30nm as plotted in Fig. 4-6(c), the only one peak which are representing V_{th} (V_{th_dgm}) can be observed regardless of T. However, in the case of L_m=100nm, the second peak of dg_m/dV_{tg}, which indicates the position of V_{FB_dgm} (≈0.5V at 77K) in Fig. 4-6(d) at very low-temperature condition, is clearly confirmed. This difference can be mainly attributed to the relative large contribution of R_{sd} influence to the carrier conduction in very short channel JLTs. In principle, two peaks in dg_m/dV_{tg} should be observed in JLTs. However, if the degradation of g_m is occurring before the position of V_{FB} owing to several performance limiting factors such as R_{sd}, the high perpendicular gate field and surface roughness scattering, it might be hard to see the second humps in dg_m/dV_{tg}. Another plausible hypothesis to explain this phenomenon

is that S/D extension region can be very close to each other, resulting in strong neutral defect scattering in such short channel JLTs (less than L_m=70nm). In spite of this limitation, it is worth noticing that dg_m/dV_{tg} at low-temperature condition can be considered as an alternative method to evaluate V_{FB} for short channel devices. With account for this tendency, the position of V_{FB_dgm} depending on different T was successfully evaluated, but only for limited condition (L_m≥70nm with T≤150K). Hence, an improved technique was requested to systematically evaluate the position of V_{th_dgm} and V_{FB_dgm} for wide T scope.

4.3.3 Double gate coupling effects at low temperature

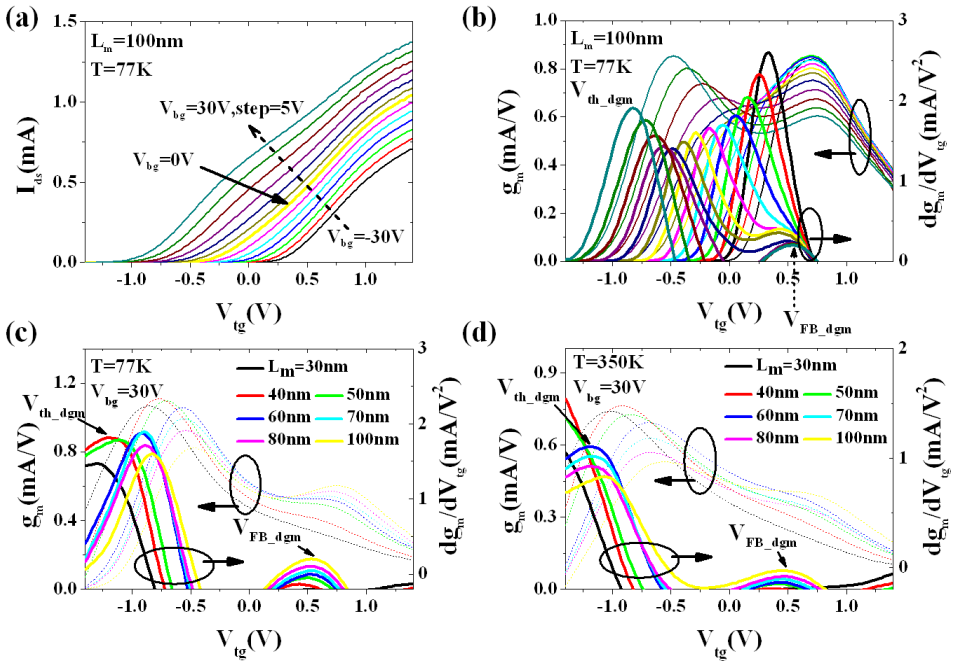


Figure 4-7 (a) Various transfer curves of L_m=100nm JLT at T=77K depending on different V_{bg} (b) g_m (left axis) and dg_m/dV_{tg} (right axis) curves. Same graphs at V_{bg}=30V with (c) T=77K and (d) T=350K with respect to L_m, respectively.

Multi-gate device has been considered as an advanced structure to suppress the short channel effect by enhancing the electrostatic gate controllability.[2, 21] For that reason, V_{tg} and V_{bg} dual gate coupling measurements under low-temperature was employed to evaluate V_{th_dgm} and V_{FB_dgm} versus T and L_m. respectively. In Fig. 4-7(a), representative transfer curves $I_{ds}(V_{tg})$ of L_m=100nm at T=77K are displayed depending on V_{bg} applied from -30V to 30V with 5V step. As usual in previous section, the graphs of g_m and dg_m/dV_{tg} are plotted in Fig. 4-7(b). Compared to Fig. 4-6(d), the position of V_{th_dgm} and V_{FB_dgm} are vividly observed with respect to V_{bg}, respectively. After determination of V_{FB_dgm} at V_{bg}=30V, it is possible to define V_{th_dgm} depending on L_m, T and V_{bg}, respectively (By assuming that V_{FB} dependence on V_{bg} is negligible ow-

ing to the screening effect as seen in Fig. 4-7(b)). Finally, it is safely able to determine V_{th_dgm} and V_{FB_dgm} versus T and L_m using this method over the whole temperature range, as displayed in Figs 4-7(c) and (d). Further V_{FB} and V_{th} dependence on T and V_{bg} including SS will be discussed in the next section.

4.3.4 Temperature dependence of various electrical parameters

4.3.4.1 V_{FB} and V_{th}, and subthreshold swing

The temperature dependence of band gap energy $E_g(T)$ and the intrinsic silicon carrier concentration $n_i(T)$ have been defined as,

$$E_g(T) = E_{g0} - \frac{AT^2}{T+B} \quad (4\text{-}5),$$

$$n_i(T) = n_{i0} T^{\frac{3}{2}} \exp\left(\frac{-qE_g(T)}{2k_B T}\right) \quad (4\text{-}6),$$

where E_{g0} (≈1.17eV), and A (≈4.73×10^{-4}eV/K) and B (≈651K) are fitting parameters and n_{i0} is ≈3.87×10^{16}cm^{-3} K$^{-3/2}$, respectively.[22, 23] In addition, V_{th} and V_{FB} (see Eq. (4-2)) and that of temperature dependence with account for the charge based analytical model of N-type JLTs in the Refs [12, 19, 24, 25] can be expressed as,

$$V_{th} = V_{FB} - \frac{q \cdot N_D \cdot t_{si}}{2}\left(\frac{t_{si}}{4\varepsilon_{si}} + \frac{1}{C_{ox}}\right) \quad (4\text{-}7),$$

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial V_{FB}}{\partial T} = -\frac{1}{2}\frac{\partial E_g(T)}{\partial T} + \frac{k_B}{q}\ln\left(\frac{N_D}{n_i(T)}\right) - \frac{k_B T}{q}\frac{1}{n_i(T)}\frac{\partial n_i(T)}{\partial T} \quad (4\text{-}8).$$

The temperature dependence of V_{th} and V_{FB} should be equal to each other since the second term of Eq. (4-8) is only related with temperature independent components. Consequently, Eq. (4-8) is obtained from Eqs (4-2) and (4-5) ~ (4-7), and it predicts that $\partial V_{th}/\partial T$ might be in the range from -0.16mV/K to -0.36mV/K with N_D evaluated from Maserjian's function. As presented in Fig. 4-8(a), V_{th_dgm} and V_{FB_dgm} of different L_m were found with respect to T. In addition, $\partial V_{th}/\partial T$ and $\partial V_{FB}/\partial T$ were found approximately, -0.5mV/K to -0.6mV/K, respectively, except when T is below 200K. Therefore, they are falling in a similar range of that of theoretical value, while considering the possible influence of R_{sd} and the strong transverse field in such short channel JLTs. Moreover, this tendency is quite consistently observed in all JLTs depending on V_{bg}. The representative data set of L_m=100nm is displayed in Fig. 4-8(b).

The temperature and V_{bg} dependence of SS in L_m=100nm JLTs were evaluated based on $I_{ds}(V_{tg})$ curves as plotted in Figs 4-8(c) and (d). SS has been defined as below,

$$SS = \frac{\partial V_{tg}}{\partial \log[I_{ds}(V_{tg})]} \quad (4\text{-}9).$$

Compared to previously reported IM transistors and JLTs with less targeted N_D ($\approx 1\times10^{19}cm^{-3}$), SS is severely worse at V_{bg}=0V.[10] It might be due to the weaker gate controllability and much enhanced short channel effect than IM transistors or less doped JLTs with the same structure.[24] However, $\partial SS/\partial T$ is almost constant and even little bit less than the theoretical maximum slope (=$k_B$ln(10)/q) regardless of L_m. Besides, there is a chance to improve it by reinforcing the gate controllability such as a multi-gate structure. For instance, SS in Fig. 4-8(d) seems to be less temperature dependent in the dual gate mode compared to the single gate mode. Therefore, although highly doped JLTs can have a poor SS performance owing to reduced electrostatic controllability at low-temperature, they can be advantageously used for high-temperature applications with multi-gate structures.

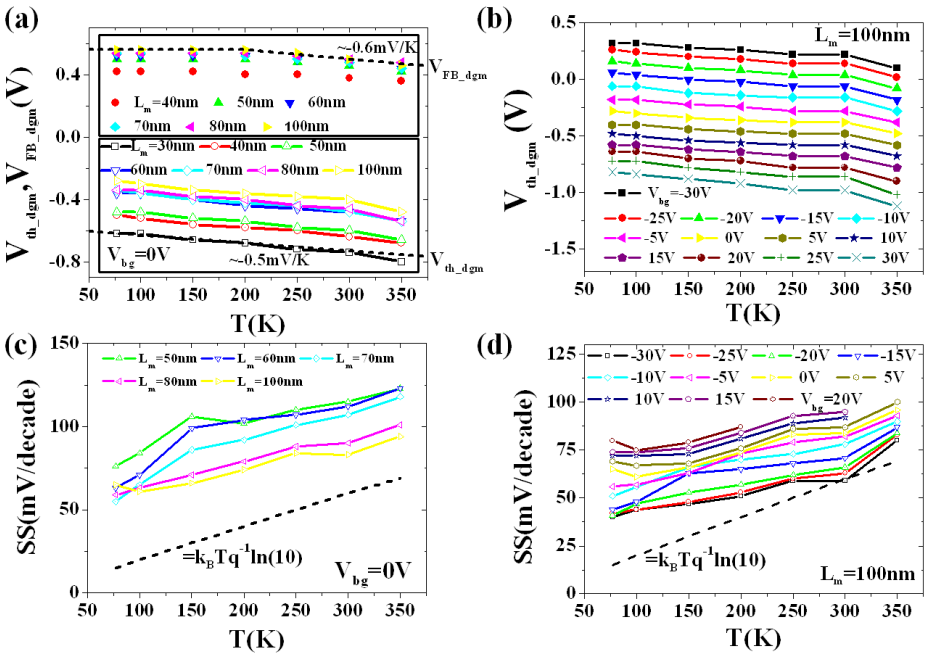


Figure 4-8 (a) The temperature dependence of V_{th_dgm} and V_{FB_dgm} versus L_m and (b) that of V_{bg} dependence in L_m=100nm JLT. (c) The temperature behavior of SS at V_{bg}=0V with respect to L_m and (d) that of V_{bg} reliance in L_m=100nm JLT.

4.3.4.2 Bulk mobility (μ_B) and low-field mobility (μ_{0_acc}) in accumulation region

To have the temperature dependence of μ_0 in JLTs without the influence of mobility degradation factors and R_{sd}, YFM ($=I_{ds}/\sqrt{g_m}$) were widely used previously for mobility evaluation in JLTs.[6, 11, 12] Moreover, the maximum value of g_m was also exploited as it is directly related with μ_{fe} ($\propto g_m$).[8] However, there are some difficulties when applying it for

such highly doped planar JLTs which have two humps in g_m originated from two different conduction mechanisms as previously confirmed in Figs 4-6 and 4-7. For instance, according to Ref. [12], two slopes of YFM can be clearly observed in less doped JLTs compared to such heavily doped JLTs (not shown in here). It is noted that if the second slope of YFM at very high V_{tg} position was not clearly determined owing to the relative large contribution of volume conduction to the total drain current, use of YFM should be carefully applied. This might be the case here. In addition, the position of V_{tg} corresponding to the maximum value of $g_m(V_{tg})$ must be behind V_{FB} if one wants to use C_{ox} for μ_{fe} calculation. Therefore, to evaluate the carrier mobility depending on their conduction region with account for the charge based analytical model, an alternative method with account for the position of V_{FB} was introduced. It is underlined that V_{FB} is important parameter to extract the carrier mobility, namely, μ_B in bulk conduction and μ_{0_acc} in accumulation region, respectively.

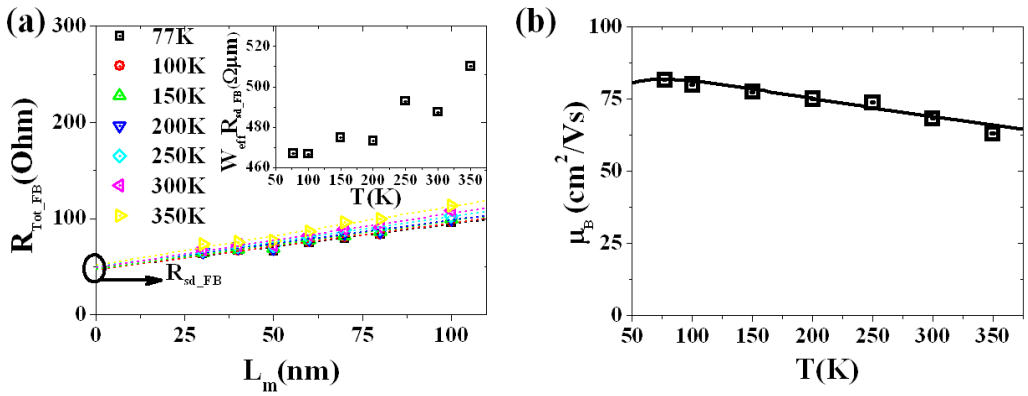


Figure 4-9 (a) The temperature dependence of R_{tot_FB} with respect to L_m. Fitting curves (dotted lines) are plotted together with data (symbols). (Inset: The temperature dependence of W_{eff} normalized R_{sd_FB}) (b) The temperature dependence of μ_B and corresponding fitting curve with account for various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ)

Referring to the Refs [1, 25], the current in partially depleted region (I_{ds_bulk}) can be expressed as follows,

$$I_{ds\_bulk} = \frac{W_{eff}}{L_{eff}} \mu_B q N_D H(V_{tg}) V_{ds}, \text{for} V_{tg} \le V_{FB} \quad (4\text{-}10).$$

where $H(V_{tg})$ is the electrical thickness of the conduction channel ($=t_{si}-t_d$, t_d being the depletion layer thickness). With boundary condition of Eq. (4-10), *i.e.*, when V_{tg} is equal to V_{FB}, the channel should be fully opened, resulting in $H(V_{FB})=t_{si}$. It is noted that I_{ds_bulk} in such region is not depending on C_{ox} but N_D and $H(V_{tg})$. Moreover, the effective V_{ds} should be considered with account for R_{sd} effect to precisely evaluate μ_B in Eq. (4-10). To this end, transfer length method (TLM) was used. In fact, to properly apply TLM, a specific test pattern should be needed to get R_{sd} with the aim of separating sheet channel resistance and contact resistance. However, it is

simply employed in this trial by assuming that JLT can be operated as a gated resistor in this trial. Finally, the total resistance at $V_{tg}=V_{FB}$ (R_{tot_FB}) should have the channel resistance and R_{sd_FB} together and can be expressed by following equation,

$$R_{tot\_FB} = \frac{V_{ds}}{I_{ds\_Bulk}} = \frac{L_{eff}}{W_{eff}\mu_B q N_D t_{si}} + R_{sd\_FB} \quad (4\text{-}11).$$

By this approach, R_{sd_FB} and μ_a are easily obtained from the y-axis intercept of Eq. (4-11) and the slope, respectively. Figure 4-9(a) and inset show the L_m dependence of R_{tot_FB} depending on T and the temperature dependence of the width normalized R_{sd_FB}, respectively. The increase of R_{sd_FB} with increasing T can be understood by the metallic-like behavior of resistivity in the S and D extension regions featuring high doping level.[26] Besides, Fig. 4-9(b) represents the temperature dependence of μ_B extracted from the each slope. In order to study the scattering mechanism of μ_B, it was fitted with empirical mobility model given by,[10, 27]

$$\mu_B^{-1} = \left(\frac{300}{T^{\gamma}}\mu_{ph}\right)^{-1} + \left(T\mu_C\right)^{-1} + \left(\mu_{neu}\right)^{-1} \quad (4\text{-}12),$$

where μ_{ph}, μ_C and μ_{neu} denote the scattering parameters derived from phonon, Coulomb and temperature independent neutral defects scattering, respectively. All fitting parameters are displayed in Table 4-2 and they are well reflecting the temperature dependence of μ_B. (see solid line in Fig. 4-9(b)). It clearly implies that phonon (γ=1) and the presence of temperature independent neutral defects scattering in silicon and/or interface between S and D region can dominantly impact the degradation of μ_B of short channel JLTs in the whole temperature range. Meanwhile, a significant influence of Coulomb scattering on μ_B is not observed in this analysis even at low temperature condition. It means that, although Coulomb scattering component in Table 4-2 looks very small compared to the others, it should be enhanced by temperature lowering. A detailed explanation of the role of various scattering components will be discussed in next paragraph.

Turning to the mobility analysis in accumulation region, the contribution of I_{ds_bulk} to the total current was excluded by assuming that I_{ds_bulk} is constant after V_{FB}. Indeed, g_m generated by the bulk conduction regime will be diminished after V_{FB}. Therefore, the surface channel current in accumulation region (I_{ds_acc}) is able to be determined after subtraction of I_{ds_bulk} at the position of $V_{tg}=V_{FB}$ from the experimentally measured total current (I_{ds_mea}). It is worth mentioning that it is hard to evaluate μ_{0_acc} with two slopes of YFM in such highly doped JLTs unlike in less doped JLTs (Target N_D; 1, 2×10^{19} cm^{-3}).[12, 13] Consequently, I_{ds_acc}, g_m in accumulation region (g_{m_acc}) can be obtained, as a result, YFM will show one slope since the bulk

channel contribution to the total current was fully vanished. YFM in accumulation region is defined as,

$$YFM = \frac{I_{ds\_acc}}{\sqrt{g_{m\_acc}}} = \sqrt{G_m V_{ds}}(V_{tg} - V_{FB}),\ \text{for}\, V_{FB} \le V_{tg} \qquad (4\text{-}13),$$

where G_m ($=\mu_{0\_acc}C_{ox\_eff}W_{eff}/L_{eff}$) is the transconductance parameter.[11, 14]

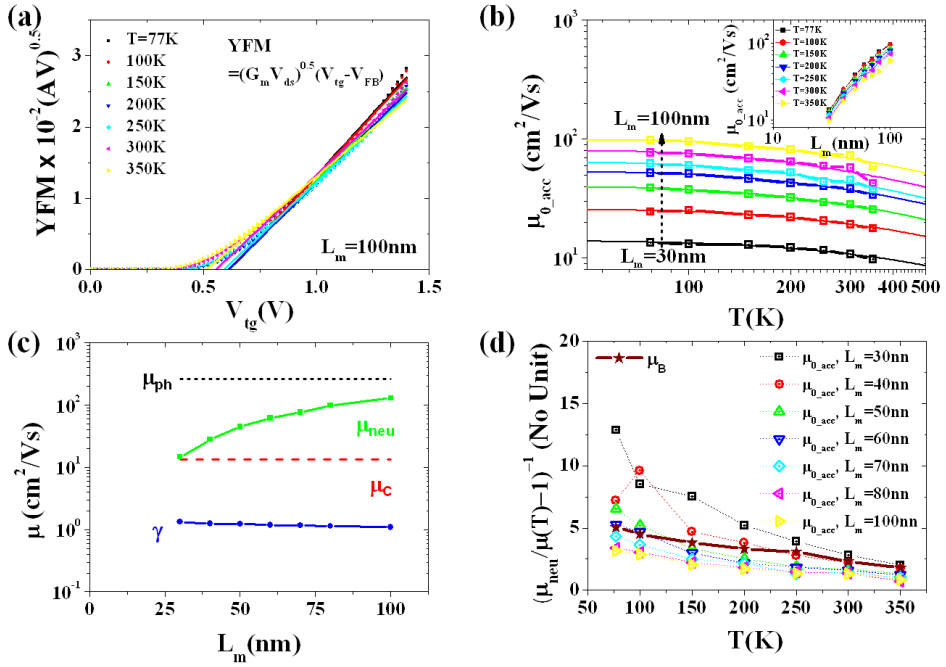


Figure 4-10 (a) The temperature dependence of YFM in accumulation regime in the case of L_m=100nm JLT. (b) μ_{0_acc} as a function of T depending on L_m (Inset: μ_{0_acc} versus L_m with varying T) (c) Various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ) for μ_{0_acc} depending on L_m. (d) The relative ratio of effective μ_{neu} contribution to μ_B and μ_{0_acc}.

The representative YFM curves of L_m=100nm JLT in wide T range are illustrated in Fig. 4-10(a) and it clearly represents only one slope depending on T. Thanks to the usefulness of YFM, the temperature dependence of μ_{0_acc} with respect to different L_m can be obtained from each slope of G_m without any influence of R_{sd}. As plotted in Fig. 4-10(b) and that of inset, the temperature and length dependence of μ_{0_acc} is clearly confirmed, increased with decreasing T and considerably degraded with decreasing L_m, respectively. In addition, to investigate the scattering mechanism of μ_{0_acc}, the behavior μ_{0_acc} is tried to fit depending on L_m by using Eq. (4-12) as well. All fitting lines (see solid lines in Fig. 4-10(b)) are well representing the temperature dependence of μ_{0_acc}. Likewise, in the case μ_B analysis, the role of phonon ($\gamma \approx 1.1 \sim 1.3$) and neutral defects scattering in silicon and/or interface between S/D region are significantly limiting μ_{0_acc} compared to the other scattering mechanisms as seen in Fig. 4-10(c). In fact, one can

expect that Coulomb scattering might be reinforced due to such high channel doping concentration (Target N_D; 4~5×10^{19} cm^{-3}). However, this mobility limitation effect is not evidently observed in this case. Instead, the temperature independent neutral defects scattering, induced by an additional doping implantation nearby S/D region with the aim of reducing channel access resistance, is significantly degrading μ_{0_acc} and μ_B even at room temperature. This explanation can be supported by previously reported studies for lower doping concentration of JLTs (Target N_D=1 and 2×10^{19} cm^{-3}) and bulk silicon channel of short channel devices.[10, 27] Hence, based on these facts, it is possible to conclude that the neutral defects scattering is the most limiting factor in such heavily doped JLTs. In addition, the effective μ_{neu} contribution to μ_B and μ_{0_acc} might be different depending on the location of the scattering source of neutral defects.[27, 28] To see this clearly, Eq. (4-14) is introduced as below, the relative ratio between μ_{neu} and μ_B or μ_{0_acc} depending on T,

$$\left(\frac{\mu_{neu}-\mu_B(T)\text{ or }\mu_{0\_acc}(T)}{\mu_B(T)\text{ or }\mu_{0\_acc}(T)}\right)^{-1}=\left(\frac{\mu_{neu}}{\mu_B(T)\text{ or }\mu_{0\_acc}(T)}-1\right)^{-1} \quad (4\text{-}14).$$

As displayed in Fig. 4-10(d), μ_{neu} is much severely limiting μ_B as compared to μ_{0_acc} when approximately L_m is less than 50nm. One possible explanation is that the location of neutral defects can be much closer to the bulk channel than surface conduction region in such geometry range. Furthermore, few cross points between μ_B and μ_{0_acc} were found when L_m is less than 60nm. It means that μ_{neu} may differently limit μ_B and μ_{0_acc} depending on T regime. In other words, if the device size is scaled down to L_m=60nm, μ_{neu} can play a significant role not only in μ_B but also in μ_{0_acc}. Hence, the device performance of such heavily doped JLTs can be improved by optimizing the process condition of S/D extension region. All fitting parameters for μ_{0_acc} analysis are also reported in Table 4-2.

4.4 Temperature Dependence of Electrical Parameters of Tri-Gate Nanowire JLTs

The temperature dependence of various electrical properties based on tri-gate nanowire JLTs (L_m≤100nm with W_m=80nm (W_{eff}≈9.6nm)) is investigated in this section. Figures 4-11(a) and (b) show the representative linear and log-scaled $I_{ds}(V_{tg})$ curves of the shortest channel of JLTs (L_m=30nm (L_{eff}≈22nm)) at V_{ds}=50mV. The temperature independent ZTC points were measured again in all short channel devices (L_m≤100nm), meaning that V_{th} and the carrier mobility are increased when T is decreased in such JLTs.

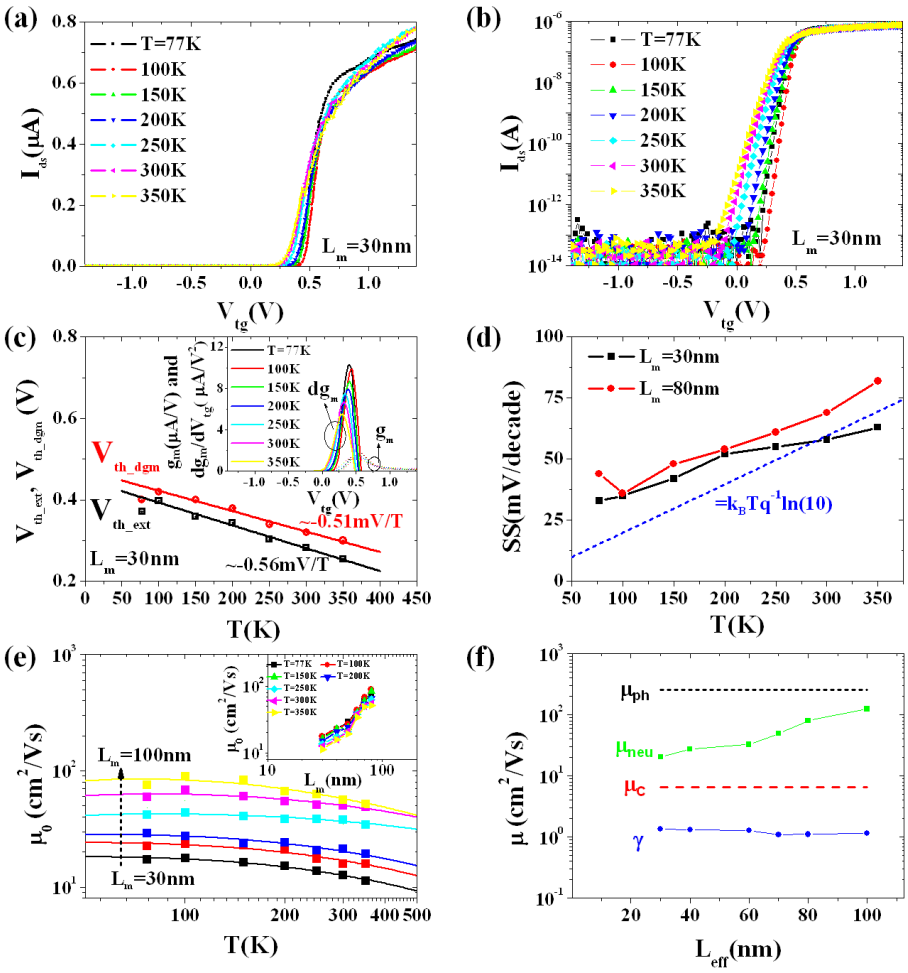


Figure 4-11 The representative (a) linear and (b) log scaled transfer curves as a function of V_{tg} in L_m=30nm tri-gate NW shape JLTs with varying T (77K to 350K). (c) The temperature dependence of V_{th_dgm} and V_{th_ext}. (Inset: g_m and dg_m/dV_{tg} curves) (d) The temperature behavior of SS (e) μ_0 extracted from YFM as a function of T depending on L_m (Inset: μ_0 versus L_m with varying T) (f) Various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ) for μ_0 depending on L_m.

To have the temperature dependence of V_{th} and V_{FB}, the derivative of g_m graphs (dg_m/dV_{tg}) was plotted in inset of Fig. 4-11(c). Although two peaks can be seen in dg_m/dV_{tg} of wide JLTs by varying T and V_{bg} (see Figs 4-6(d) and 4-7(b)), only one peak of dg_m/dV_{tg} was observed in this experiment regardless of T, L_m and V_{bg}. It might be mainly due to the narrow channel width effects.[13] As W_m is scaled down, the bulk channel contribution to the total current is relatively reduced whereas that of accumulation channel is remained (in fact, relatively increased). In other words, the role of side-wall in terms of the gate controllability can be relatively stronger than that of top surface compared to wide JLTs. In addition, the maximum depletion width ($\approx W_{d\_\max} = \sqrt{2\varepsilon_{si} 2V_{fb\_theory} / qN_D}$ ≈8.8nm) generated from each side-wall of tri-gate JLTs is sufficient to turn such devices off. For these reasons, less V_{tg} should be needed to repel depletion regime in tri-gate nanowire JLTs than planar type JLTs. Hence, it is possible

that V_{th} and V_{FB} can be merged, since V_{th} can be increased whereas V_{FB} is not changed.[13] Moreover, it should be noted that large V_{th} and V_{FB} deviations could stem from process-induced random dopant fluctuations in such scaled total silicon volume.[29] This is the reason why it is difficult to define V_{th} and V_{FB} separately. Furthermore, there might be relatively strong R_{sd} effects on V_{th} and V_{FB} than in long channel devices. It means that V_{FB} cannot be seen if overall transfer curve were limited by R_{sd} before V_{FB}. With account for these facts, consequently, it is almost impossible to separately determine V_{th} and V_{FB} based on IV characteristics in such small-scaled devices. Consequently, further electrical parameter analysis in such narrow JLT will be only focused on surface accumulation channel without consideration of bulk conduction regime assuming that V_{th} and V_{FB} are adjacent each other.

The temperature dependence of V_{th} extracted from dg_m/dV_{tg} and linear extrapolation (V_{th_ext}) are displayed together in Fig. 4-11(c). Each slope is found approximately $\partial V_{th\_dgm}/\partial T \approx$-0.51mV/K and $\partial V_{th\_ext}/\partial T \approx$-0.56mV/K, respectively. These values are quite consistent with that of evaluated from wide JLTs ($\partial V_{th\_dgm}/\partial T \approx$-0.5mV/K, see section 4.3.4). Moreover, as discussed previously, the range of V_{th_dgm} is almost similar to that of V_{FB_dgm} evaluated from planar JLTs, indicating that V_{th_dgm} and V_{FB_dgm} can be close to each other.

Besides, the representative temperature behaviors of SS of L_m=30nm and 80nm tri-gate JLTs were also obtained based on $I_{ds}(V_{tg})$ curves by using Eq. (4-9) as presented in Fig. 4-11(d). It shows the enhanced SS values compared to planar type JLTs since there is much strong gate controllability originated from the side-wall as previously studied. In addition, the slope ($=\partial SS/\partial T$) is almost similar to theoretical maximum slope ($=k_B\ln(10)/q$) regardless of L_m. This fact indicates that its improved electrical properties stemmed from tri-gate structure in terms of SS. However, as displayed in Figs 4-11(e) and (f), the temperature dependence of μ_0 extracted from YFM shows much poorer performance compared to that of IM transistors in Ref. [10] and the huge mobility degradation can be seen in inset of Fig. 4-11(e) as well. It is attributed to the high doping concentration in silicon channel and the role of neutral defects scattering in silicon and/or interface between S and D like for μ_B and μ_{0_acc} analysis. Especially, owing to the relatively large portion of S/D extension region in such small volume JLTs, the impact of μ_{neu} on μ_0 can be reinforced, resulting in much inferior mobility property to IM transistors. All fitting parameters for the temperature properties of μ_0 in Fig. 4-11(f) are displayed in Table. 4-2.

L_m(nm)		30	40	50	60	70	80	100
μ_B (cm^2/Vs)	μ_{ph}	260	260	260	260	260	260	260
	μ_C	13.3	13.3	13.3	13.3	13.3	13.3	13.3
	μ_{neu}	97.8	97.8	97.8	97.8	97.8	97.8	97.8
	γ	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Planar μ_{0_acc}	μ_{ph}	260	260	260	260	260	260	260
	μ_C	13.3	13.3	13.3	13.3	13.3	13.3	13.3
	μ_{neu}	14.6	27.9	44.9	62.0	76.6	99.9	128.2
	γ	1.3	1.3	1.2	1.2	1.2	1.1	1.1
Tri-gate NW μ_{0_acc}	μ_{ph}	260	260	-	260	260	260	260
	μ_C	6.7	6.7	-	6.7	6.7	6.7	6.7
	μ_{neu}	20.3	27.4	-	32.7	49.5	80.7	123.8
	γ	1.4	1.3	-	1.3	1.1	1.1	1.1

Table 4-2 Table for various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ) for μ_B, μ_{0_acc}, and μ_0 depending on L_m, respectively

4.5 Conclusion

Low-temperature characteristics of flat-band voltage and low-field mobility in planar and tri-gate nanowire JLTs were investigated based on CV, IV, cryogenic and dual-gate coupling measurements. The position of V_{FB} was determined and compared based on various experimental results and theoretical model, respectively, including the temperature dependence of V_{th}. To present the temperature behavior of low-field mobility, V_{FB} and the charge based analytical model of JLTs were considered with respect to different conduction region and type of JLTs. Finally, the role of neutral defects scattering was found the most limiting factor concerning the degradation with small gate length of low-field mobility in both planar and tri-gate nanowire JLTs. Therefore, the optimized engineering of S/D extension region should be needed in order to improve the JLT performances.

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5. Carrier mobility and low frequency noise characteristics of tin-oxide nanowire FET

Chapter 5 Abstract

In this chapter, channel access resistance (R_{sd}) effects on the charge carrier mobility (μ) and low frequency noise (LFN) in a polymethyl methacrylate (PMMA) passivated tin-oxide nanowire (SnO_2-NW) field effect-transistor (FET) are investigated. To precisely understand for the electrical intrinsic properties of SnO_2 NW-FET, the accurate determinations of R_{sd} and gate-to-channel capacitance (C_{gc}) are required. To this end, a numerical simulation was used to evaluate C_{gc} accounting for the electrostatic gate coupling effects through a PMMA passivation layer and the Y function method (YFM) was employed for direct electrical parameter extractions without R_{sd} influence. Furthermore, to study the interface characteristics between the active channel area and the dielectric layer (SnO_2/Si_3N_4 and/or SnO_2/PMMA), LFN measurements were carried out. The carrier number fluctuation (CNF) noise model was found appropriate to interpret the LFN data provided R_{sd} influence is included.

5.1 Introduction

One-dimensional (1D) metal oxide nanowires (NWs) such as ZnO,[1, 2] SnO_2,[3] In_2O_3,[4] CdO,[5] CuO[6] have attracted much interests because of their unique properties such as high surface-to-volume ratio, large aspect ratio, and carrier quantizing effects for practical applications ranging from electronic/optoelectronic devices to gas sensors.[1-6] Among these metal oxide materials, SnO_2 NWs have been suggested as an excellent candidate for high performance flexible, transparent NW transistors, thin film transistors, and gas sensors with low temperature fabrication process.[7-11] However, the counterpart of such high sensitivity is poor device reliability and stability when used as transistor.[11, 12] To improve the reproducibility of device performance, a polymer and an alumina (Al_2O_3) layer have been employed as passivation layers with the aim of keeping adsorbents off the surface of metal oxide NWs.[13-15] For instance, a PMMA passivation layer has been found efficient in improving electrical properties as displayed in Fig. 5-1, resulting in enhanced carrier mobility, larger on/off current ratio, and significant shift of the threshold voltage (V_{th}).[13-15] However, care should be taken in extracting these parameters. In particular, in such quasi-1D nanostructures, parameters such as μ and D_{it} (interface trap density) between channel and surrounding dielectrics can be considerably under- and/or over- estimated without consideration of R_{sd}. Previously, Na *et al.* considered R_{sd} for μ estimation in SnO_2 NW-FETs, but there are still large deviation in μ behaviours in the high gate bias regime.[14] Moreover, there is a lack of studies on R_{sd} effects on μ and LFN in polymer passivated metal-oxide NW-FETs.

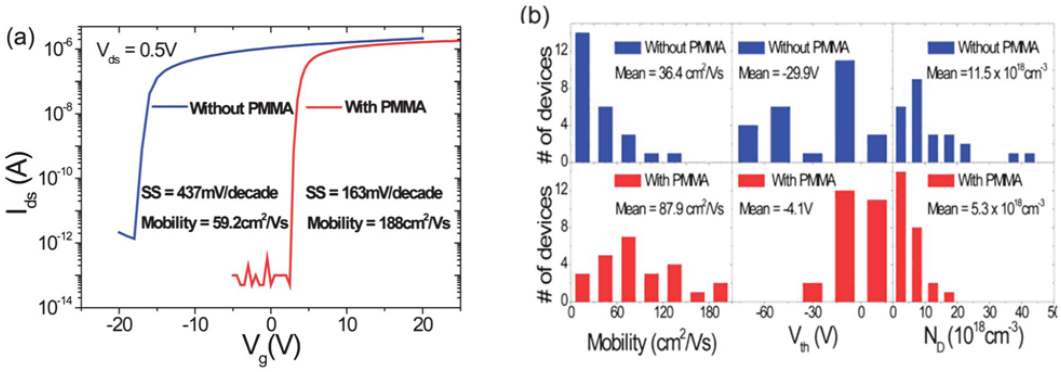

Figure 5-1 (a) Representative transfer curves of SnO_2 NW-FETs and (b) histogram of field effect mobility, V_{th}, and carrier concentration for with and without PMMA passivation layer at V_{ds}=0.5V.[15]

In this chapter, particularly R_{sd} effects on μ and LFN characteristics of PMMA passivated SnO_2 NW-FETs will be focused. In addition, analytical simulations were performed to account for electrostatic coupling effects through the PMMA layer, as they influence the value of C_{gc} and, as a consequence, μ extraction and LFN analysis. Moreover, YFM was employed

to directly evaluate the electrical parameters.[16] Indeed, because it is not influences by R_{sd}, this methodology provides reliable values for V_{th}, mobility, degradation factor (θ), low-field mobility (μ_0), as well as R_{sd}.[16-18] In comparison, the influence of R_{sd}.on the extraction of field effect mobility (μ_{fe}), effective mobility (μ_{eff}) was analyzed.[17] Furthermore, LFN measurements were carried out to assess the reliability and the quality of the interfaces between the active channel area and the dielectric layers. (SnO_2/Si_3N_4 and/or SnO_2/PMMA)[19-21]

5.2 Device Fabrication Process and Electrical Measurement Conditions

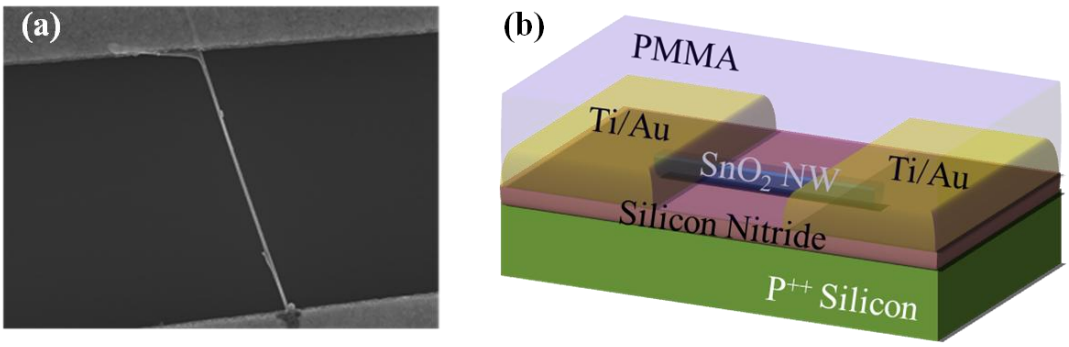

Figure 5-2 (a) FE-SEM image of SnO_2 NWs and (b) a simplified 3D structure of PMMA passivated SnO_2 NW-FET.

Fabrication of SnO_2 NW-FETs: SnO_2 nanowires were synthesized by chemical vapor deposition of Sn metal powders (99.9%) on gold (Au) coated silicon substrates. The metal source was then located at the center of quartz tube in furnace for 30 minutes at 750°C. Argon (Ar) as a carrier gas with a flow rate of 20–50 sccm was flowed through the quartz tube to maintaining air pressure in between 2 and 5 Torr. In detail descriptions for this synthesis method and the crystalline quality of SnO_2 NW are published elsewhere.[22] A piece of Si substrate covered with synthesized SnO_2 NWs was dipped into an isopropyl alcohol (IPA) solution and suspended by sonication. A few droplets of solution containing SnO_2 NWs were dropped on the surface of the Si_3N_4 (=150nm) layer. Selective electron beam (E-beam) patterning of contacts areas at the edges of an individual SnO_2 NW have been proceeded by using a conventional E-beam lithography system (Elphy Quantum, Raith). To make conducting metal electrodes, Ti (20nm) and Au (100nm) were deposited on SnO_2 NWs by an E-beam evaporation process followed by lift-off. Finally, the PMMA (950K C2, MicroChem) passivation layer was spin-coated on several devices with baking process. A FESEM image of a SnO_2 NW-FET is displayed in Fig. 5-2(a). The length (L) and width (W) (≈ diameter) of the NW were estimated to be L =

3.39μm and W = 42nm, respectively. The 3D view of the PMMA passivated SnO_2 NW-FET structure with a back-gate configuration is drawn in Fig. 5-2(b).

Electrical Characterizations: The IV current-to-voltage characteristic depending on V_{gs} was measured from HP 4145B with fixed drain voltage V_{ds}=0.25V. And, LFN measurements were carried out as a function of V_{gs} with frequency ranges from 10Hz to 1kHz. (See Fig 5.3 for LFN measurement system) The drain current of the SnO_2 NW-FET was driven by a homemade battery box. Through a low noise current-to-voltage preamplifier (SR570, Stanford Research Systems Inc.), the drain current was amplified and converted to voltage. The power spectrum density was then directly obtained by a dynamic signal analyzer (HP3562A, Agilent). All the measurements were done in a metal shielding box at room temperature. (T=300K)

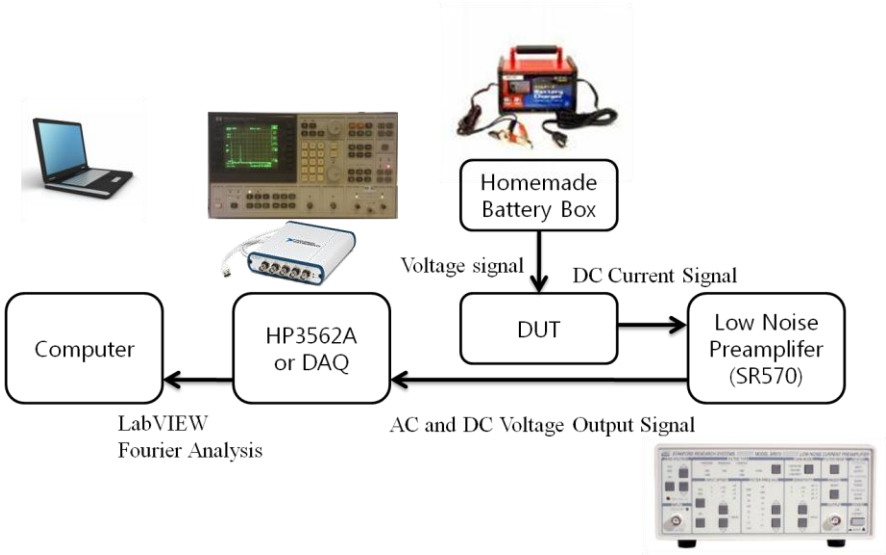

Figure 5-3 The LFN measurement system

5.3 Effective Gate-to-Channel Capacitance Simulation

Many researchers have spent their efforts to improve electrical device performances, however, the use of proper electrical characterization techniques is of prime importance to extract intrinsic properties reliably and de-correlate them from parasitic effects. For instance, it is known from classical silicon (Si) based Metal-Oxide-Semiconductor (MOS) transistors that R_{sd} and C_{gc} are crucial factors for the accurate determination of μ in the high gate bias regime.[20] Thus, before further analysis, the evaluation of the effective C_{gc} will be discussed at first.

Measurement of C_{gc} is a key to the estimation of parameters such as μ, interface trap capacitance, and D_{it} in MOS-FETs.[17, 18, 21] Several research groups have reported that

PMMA passivation layer can give additional electrostatic gate coupling effects to metal-oxide NW-FETs compared to a non-passivated one.[13-15, 23, 24] However, they have not yet accounted for these effects in C_{gc} for μ and LFN analysis. For better parameter interpretations, a preliminary numerical simulation was done to obtain $C_{gc}(V_{gs})$ and $I_{ds}(V_{gs})$ curves depending on V_{gs} taking into account the flat-band voltage (V_{fb}), D_{it}, and R_{sd}. It is worth commenting that the measurement of C_{gc} in such scaled quasi-1D nano-structure is almost impossible without special measurement system environment.[25] To this end, Poisson-equation was solved with a finite-element-method across a two-dimensional (2D) cross-section of the SnO_2 NW-FET using FlexPDE with the actual size of the SnO_2-NW. Various simulation assumptions such as room temperature, material intrinsic μ, and homogeneous SnO_2-NW and dielectric passivation layers were considered in this trial with account for previously reported values. The relative permittivity of SnO_2, PMMA, Si_3N_4 and intrinsic doping concentration of SnO_2 were taken from literature.[26-29] Moreover, quantum correction effects on the charge carrier concentration were considered by means of Hansch's approach[30] which cancels out the carrier density at the interface between dielectric layers and the SnO_2-NW over a quantum distance.

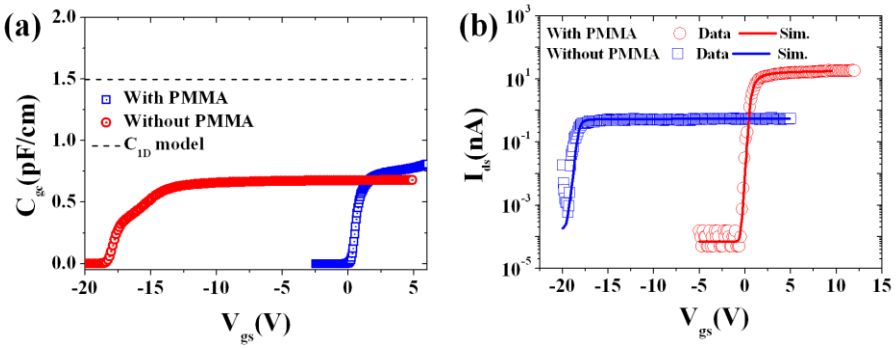

Figure 5-4 (a) Comparison capacitance values between the C_{1D} and simulated $C_{gc}(V_{gs})$ with and without PMMA passivation layer respect to back-gate bias. (b) $I_{ds}(V_{gs})$ of SnO_2 NW-FET with and without PMMA passivation layer at V_{ds}=0.25V.

The simulated $C_{gc}(V_{gs})$ and their corresponding $I_{ds}(V_{gs})$ at V_{ds}=0.25V curves of SnO_2 NW-FET with and without PMMA passivation layer were obtained. Results are presented in Figs 5-4(a) and (b) together with the constant 1D analytical gate capacitance model (C_{1D}) for comparison.[31] C_{1D} is defined as below,

$$\frac{C_{1D}}{L} = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}\left(1+\frac{2t}{d}\right)} \quad [F/cm] \qquad (5\text{-}1),$$

where d is the diameter of NW, ε_0 is the permittivity of free space, ε_r and t are the relative permittivity and the thickness of Si_3N_4, respectively. Previously, Wunnicke has well demonstrated

that the gate capacitance of an embedded NW (C_{1D} here) is almost twice as large as that of a non-embedded NW (back-gate configuration) with SiO_2 dielectrics.[31] The same conclusion was clearly reached here. Indeed, C_{1D} (1.497pF/cm) was approximately twice as large (strictly, 1.85 times) than C_{gc} (0.808pF/cm). This is because the C_{1D} model assumes that the NW is fully wrapped by dielectrics. It is thus not valid for a non-embedded NW-FET. In addition, the C_{1D} model assumes a cylindrical structure, while the real section is rather tetragonal. Hence, the C_{1D} model could lead to underestimate μ by almost a factor two in PMMA passivated devices. Moreover, the electrostatic gate coupling effects in the presence of a PMMA layer to SnO_2-NW were confirmed[13-15, 32] to be nearly 1.35 times larger than without passivation in ambient condition as displayed in Fig. 5-4(a). It is underlined that in order to evaluate the electrical parameters precisely, specific C_{gc} values depending on device structure and passivation materials should be used. Therefore, for further parameter extractions, the above simulated value of C_{gc} in linear region (≈0.808pF/cm) will be used.

5.4 Mobility Analysis

The static measurements were carried out with a semiconductor parameter analyzer (HP4145B). Simulated $I_{ds}(V_{gs})$ curve at fixed drain voltage (V_{ds}=0.25V) after accounting for $C_{gc}(V_{gs})$ from Fig. 5-5(a) is plotted in Fig. 5-5(b). For the sake of comparison, experimental $I_{ds}(V_{gs})$ and $g_m(V_{gs})$ curves of back-gated SnO_2 NW-FET with a PMMA layer are presented in Fig. 5-5(b) with same V_{ds}. Both transfer curves are nearly identical, which indicates that $C_{gc}(V_{gs})$ in Fig. 5-5(a) and the other input parameters such as V_{fb}, D_{it} and R_{sd} can properly reflect the actual device conditions. To illustrate the effectiveness of YFM against other electrical parameter extraction methods, we firstly applied the method generally used for metal-oxide NW-FETs.[12, 14, 15, 23] V_{th} was extracted from the linear extrapolation of drain current at the point of maximum $g_m(V_{gs})$, which was found around ≈0.26V. The μ_{fe} was then determined by, $\mu_{fe}=g_m \cdot L/(V_{ds} \cdot C_{gc})$. The maximum value was estimated to be ≈10.5$cm^2 \cdot V^{-1} \cdot s^{-1}$. However, it is well known from the physics of classical MOS-FET that R_{sd} can severely affect the accuracy of mobility extraction.[14, 16, 17, 33] Therefore, we employed YFM(V_{gs}) to eliminate the R_{sd} influence. It is defined as,

$$YFM(V_{gs}) = I_{ds}/\sqrt{g_m} = \sqrt{G_m \cdot V_{ds}}(V_{gs} - V_{th}) \qquad (5\text{-}2),$$

where $G_m=C_{gc} \cdot \mu_0/L$ is the transconductance parameter.[16] The μ_0 can be considered as an intrinsic mobility in MOS-FET, hence, it can be regarded as the maximum mobility in the device under study since it is not affected by R_{sd} and independent of V_{gs}.

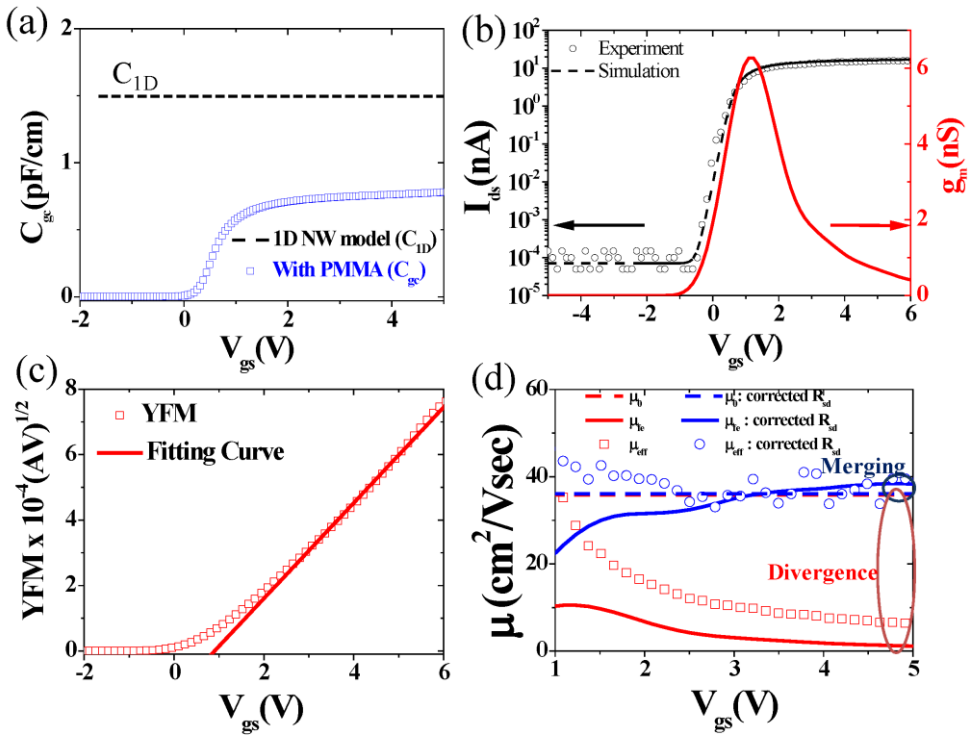

Figure 5-5 (a) Comparison capacitance values between the C_{1D} and simulated $C_{gc}(V_{gs})$ (open rectangular) respect to back-gate bias. (b) $I_{ds}(V_{gs})$ (open circle) and $g_m(V_{gs})$ (line) of SnO_2 NW-FET at V_{ds}=0.25V. Simulated $I_{ds}(V_{gs})$ (dotted circle) is added for comparison. (c) YFM(V_{gs}) curve with linear fitting line. (d) Comparison of various mobility (μ_0, μ_{fe}, μ_{eff}) before and after R_{sd} correction.

Figure 5-5(c) shows good linearity of YFM(V_{gs}) allowing good fit by Eq. (5-2). With this methodology, we can extract μ_0 (≈35.8cm^2·V^{-1}· s^{-1}) from the slope and V_{th} (≈0.90V) by the linear extrapolation to zero of YFM(V_{gs}). In addition, $\theta=\theta_0+\theta_1$, ($\theta_1 \approx G_m \cdot R_{sd}$=1.15V^{-1}, θ_0 and θ_1 are the mobility degradation factors related to channel scattering and R_{sd}, respectively. θ_0 being much smaller than θ_1) and R_{sd} (≈567kΩ·μm) were obtained by simple computation with Eq. (5-3),[16, 17]

$$\theta = \frac{G_m \cdot V_{ds}}{I_{ds}} - \frac{1}{V_{gs}\text{-}V_{th}} \Rightarrow R_{sd} \approx \frac{\theta}{G_m} = \frac{V_{ds}}{I_{ds}} - \frac{1}{G_m \cdot (V_{gs}\text{-}V_{th})} \qquad (5\text{-}3).$$

Although R_{sd} seem huge compared to that of silicon devices (≈100Ω·μm), it is a competitive value compared with previous studies.[11, 34] For instance, Francisco *et al.* reported that R_{sd} between SnO_2-NW and Pt electrode is about 1.1MΩ·μm measured by the four-probe method and that in some cases, the contribution of R_{sd} represented more than 90% of the total resistance. It is clear that R_{sd} is too important to be neglected in such cases.[11, 34]

Finally, we also extracted μ_{eff} from Eq. (5-4), where C_{gcmax} is the maximum C_{gc} value in strong accumulation region. The μ_{eff} is then defined as follows,

$$\mu_{eff} = \frac{I_{ds} \cdot L}{V_{ds} \cdot C_{gc\max} \cdot (V_{gs} - V_{th})} \quad (5\text{-}4).$$

To further analyze R_{sd} influence on mobility in SnO_2 NW-FETs, we used the various mobility parameters, namely μ_0 from YFM, μ_{fe} from $g_m(V_{gs})$ and μ_{eff} from Eq. (5-4) and compared the values extracted before and after R_{sd} correction. As seen in Fig. 5-5(d), there were substantial differences among these mobility values above V_{gs}=1.2V (maximum g_m position). They even diverged as V_{gs} increased. This can be attributed to the large value of R_{sd}, which resulted in a significant reduction of the apparent μ_{fe} and μ_{eff} at high V_{gs} due to its large contribution to the total resistance ($R_{tot} = R_{ch} + R_{sd}$) compared to channel resistance (R_{ch}). It is possible to exclude R_{sd} impact, if R_{sd} can be considered as independent of V_{gs}. Then, $I_{ds}(V_{gs})$ measured in linearly operated region can be modified by using the following equation,

$$I_{ds}' = \frac{I_{ds} \cdot V_{ds}}{V_{ds} - I_{ds} \cdot R_{sd}} = \frac{I_{ds}}{1 - I_{ds} \cdot R_{sd} \cdot V_{ds}^{-1}} \quad (5\text{-}5).$$

The same procedures as above were then followed for mobility extraction and the results are presented in Fig. 5-5(d). After R_{sd} correction, all mobility values were converging towards μ_0 value and the attenuation phenomena at high V_{gs} were fully removed. This implies that the decrease in mobility, observed above V_{gs} point of maximum $g_m(V_{gs})$, was indeed due to R_{sd}. Moreover, we confirmed that YFM gives negligible differences in terms of slopes and V_{th} between before and after the correction of R_{sd}. Hence, YFM can be safely applied to SnO_2 NW-FET for reliable electrical parameter extraction, free from R_{sd} effects, and μ_0 can be regarded as the intrinsic mobility of the channel, nearly independent of V_{gs}.

5.5 Low Frequency Noise Characteristics of SnO_2 NW-FETs

In order to optimize technology for stable operation and evaluate the minimum detectable signal amplitude, it is important to understand the role of charge trapping centers at the interface with dielectric layers.[12, 20, 35] LFN analysis has recently gained interest to characterize the interface properties of the top or the bottom surface of metal-oxide NW-FETs. For this reason, LFN measurements were carried out as a function of V_{gs} between 10Hz to 1kHz at V_{ds}=0.25V. As can be seen in Fig. 5-6(a), the I_{ds} normalized LFN power spectrum density (PSD) shows a 1/f dependency. In previous reports for individual carbon-nanotube (CNT) transistors, R_{sd} was found to affect not only carrier transport, but also the overall LFN characteristics.[32] Similarly, in metal-oxide NW-FETs, R_{sd} contribution is too important to be ignored. To compare the relative contribution of R_{sd} to the total resistance (R_{sd}/R_{tot}) with that of the channel resistance (R_{ch}/R_{tot}) in SnO_2 NW-FET, these ratios were plotted together with respect to I_{ds} in Fig. 5-6(b). The R_{sd} value used in here was extracted by using YFM. At the position where I_{ds} is

≈10nA, the relative ratio was such that $R_{sd}/R_{tot}=R_{ch}/R_{tot}=0.5$. Beyond this current level, R_{sd} overtook R_{ch} in the total resistance.

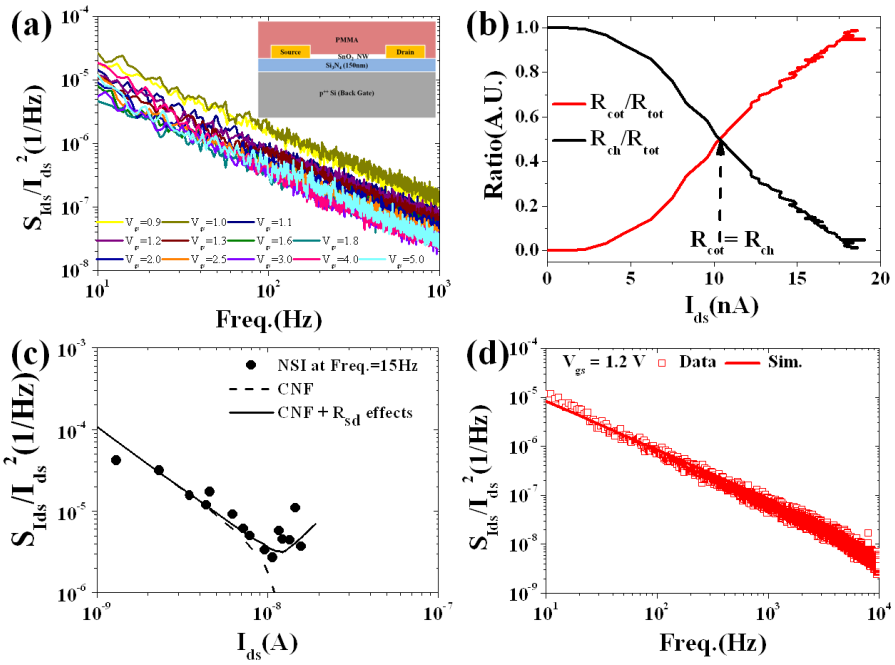

Figure 5-6 (a) I_{ds} normalized LFN for various V_{gs} regimes. (b) Relative contribution to total resistance of series resistance (R_{sd}/R_{tot}) and of the channel resistance (R_{ch}/R_{tot}) with respect to I_{ds}. At I_{ds}≈10nA, $R_{sd}/R_{tot}=R_{ch}/R_{tot}$. (c) Variation of S_{Id}/I_{ds}^2 (circle symbols). Solid line: CNF model. Dotted line: CNF+R_{sd} model. (d) Comparison LFN behaviors between experimental and simulation results.

For the sake of LFN analysis, the I_{ds} normalized LFN-PSD (S_{Ids}/I_{ds}^2) at a given frequency (f=15Hz), is plotted in Fig. 5-6(c). For comparison, $S_{Vfb}\times(g_m/I_{ds})^2$ (see Eq. (5-6)) is also displayed as a function of I_{ds} in the same graph. The correlation of I_{ds} normalized LFN level with $S_{Vfb}\times(g_m/I_{ds})^2$ clearly demonstrates that the CNF mechanism is predominantly observed, which is a trend already observed in SnO_2 NW-FETs.[15] Such correlation is due to the carrier fluctuations associated with the trapping/de-trapping of charge carriers at the interface with the dielectrics. Good correlation was obtained from depletion to strong accumulation region, except for the high I_{ds} regime, above I_{ds}≈10nA. This discrepancy was consistently explained by R_{sd} effects as expected from Fig. 5-6(b). Indeed, the I_{ds} normalized LFN in CNF model is usually given by,

$$\frac{S_{I_{ds}}}{I_{ds}^{\ 2}} = S_{V_{fb}}\left(\frac{g_m}{I_{ds}}\right)^2 = \frac{q^2 k_B T N_{NW}}{L C_{gc\max}^{\ 2} f}\left(\frac{g_m}{I_{ds}}\right)^2 \quad (5\text{-}6),$$

where S_{Vfb} is the flat-band voltage of PSD, q is electron unit-charge, k_BT is the thermal energy and N_{NW} is linear trap density along the NW.[19] However, this CNF model should be modified

to account for R_{sd} effects. To do this, we incorporated the PSD of R_{sd} into the CNF model by the following relation,

$$\frac{S_{I_{ds}}}{I_{ds}^{2}} = S_{V_{gs}}\left(\frac{g_m}{I_{ds}}\right)^2 + \frac{S_{R_{sd}}}{R_{sd}^{2}} R_{sd}^{2}\left(\frac{I_{ds}}{V_{ds}}\right)^2 \quad (5\text{-}7),$$

where S_{Vgs} is the input-referred noise and S_{Rsd} is the channel access resistance noise.[20] As seen in Fig. 5-6(c), this CNF+R_{sd} model of Eq. (5-7), is more applicable to interpret the behavior of LFN than the CNF model itself. R_{sd} normalized noise value (S_{Rsd}/R_{sd}^2) was extracted to be $6.5\times10^{-6}Hz^{-1}$ and the linear density of traps along the nanowire (N_{NW}) lied around $3.0\times10^{7}eV^{-1}\cdot cm^{-1}$. It is worth noting that these values would have been overestimated by about 3.5 times if we had used the C_{1D} model instead of the more realistic simulated value. Furthermore, the LFN results obtained from FlexPDE simulation were also presented as in Fig. 5-6(d). It was well coincided with experimental data, which clearly indicates that the simulation tool employed in this study was quite valid and helpful to understand for the carrier transport of SnO_2 FETs.

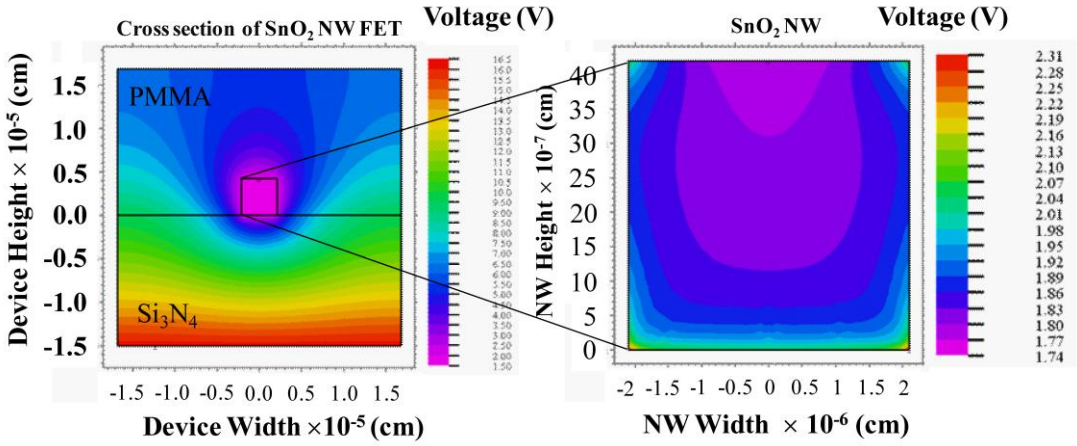

Figure 5-7 Simplified cross-section view of the effective V_{gs} contour in PMMA passivated SnO_2 NW-FET with back-gate configuration (left) and its magnified view in SnO_2-NW region (right) at high V_{gs}.

Based on aforementioned LFN and simulation analysis, this noise behavior consistent with CNF model can be well explained by the surface properties of metal-oxide NWs. It has been demonstrated that there are many oxygen vacancies at the surface of metal-oxide NWs.[8, 14] These vacancies can easily interact with the surrounding ambient gas or water molecules.[8, 14] In case of a polymer passivation, the surface of metal-oxide NWs can be partially populated depending on the back-gate bias. Indeed, as seen in Fig. 5-7, although the bottom interface of SnO_2-NW is dominantly controlling the carrier density, the three other edges of the tetragonal structure can also play an additional role in controlling surface carrier concentra-

tion. These results indicate that the interaction of the PMMA layer with the surface of SnO_2 NW-FET can have visible effects on carrier transport as well as on carrier fluctuations associated with the trapping/de-trapping of charge carriers.

5.6 Conclusion

In conclusion, we investigated R_{sd} effects on μ and LFN in a PMMA passivated SnO_2 NW-FET. The effective C_{gc} was obtained from simulation accounting for real dimensions and electrostatic coupling effects associated with the presence of the PMMA. YFM was employed to directly evaluate the electrical parameters without the influence of R_{sd}. In addition, μ_0 was compared with other mobility values such as μ_{fe} and μ_{eff}. After R_{sd} correction, all mobility values were consistent with the intrinsic μ_0. Finally, LFN was clearly attributed to CNF model provided R_{sd} effects were incorporated and the N_{NW} in SnO_2 NW-FETs with PMMA passivation layer was deduced from LFN analysis. This methodology can be applied to account for R_{sd} with other quasi-1D devices as and other passivation materials.

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6. Charge transport of quasi-2D random network of carbon nano-tube TFTs

Chapter 6 Abstract

Static and low frequency noise (LFN) characterizations in two-dimensional (2D) N-type random network thin film transistors (RN-TFTs) based on single-walled carbon nanotubes (CNTs) are presented in this chapter. For the electrical parameter extraction, the Y-function method (YFM) was used to suppress the series resistance (R_{sd}) influence. The gate-to-channel capacitance (C_{gc}) was directly measured by the split capacitance-to-voltage (CV) method and compared to 2D metal-plate capacitance model (C_{2D}). In addition, to account for the percolation-dominated 2D RN-TFTs, a numerical percolation simulation was performed. LFN measurements were also carried out and the results were well interpreted by the carrier number and correlated mobility fluctuation model (CNF-CMF). Finally, one-dimensional (1D) cylindrical analytical capacitance based model (C_{1D}) was suggested and applied to provide better consistency between all electrical parameters based on experimental and simulation results.

6.1 Introduction

Carbon nanotubes (CNTs) are 1D cylindrical honeycomb nano-structure composed of rolled up one or more graphene sheets. Especially, after first observation of single-walled CNT (SWCNT) by Iijima *et al.* in 1993[1], it has been gained a great attention by researchers due to its unique properties such as a nearly ideal 1D structure (extremely high aspect ratio$\approx 10^8$)[2], high potential to open a quasi-ballistic carrier transport, high mechanical (Young's modulus$\approx$50GPa)[3] and thermal stability (thermal conductivities$\approx 3500 Wm^{-1}K^{-1}$)[4] arisen from strong carbon-to-carbon covalent bonding, and high current carrying capability density up to $J \approx 10^9 A/cm^2$.[5] Despite aforementioned many advantages in an individual CNT-FET, there are many challenges to be overcome as a next generation electronic device. The most urgent issues in present of these are the insufficient current output driven from such extremely small scaled 1D structure and the lack of practical fabrication methods to shrunk device-to-device variation.[6]

Currently, with the aim of a low-cost mass production and an averaging out the wide device differences arisen from the divergence of the electrical properties of pristine CNTs, two dimensional (2D) random network thin film transistors (RN-TFTs) have been proposed.[6-11] This approach can provide high reproducibility and reliability as a promising candidate for large-scaled, inexpensive, transparent, and flexible electronics.[6-9, 11-13] In addition, to enhance the semiconducting performance as FETs by suppressing the effects of metallic CNTs, several experimental trials were made such as perfectly aligned structure, CNTs dispersion with suspension of centrifugation, electrical breakdown, and chemical reaction.[7, 9, 12, 14-19]

In spite of progress in device fabrication and synthesis methods for preferential semiconducting CNTs, there are still lacks of understanding in static and low frequency noise (LFN) characteristic of RN-TFTs. For instance, the field effect mobility (μ_{fe}) in RN-TFTs has been reported in previous work ranging from $\approx 10^{-2}$ to $\approx 10^2 cm^2 \cdot V^{-1} \cdot s^{-1}$ with considering 2D metal-plate capacitance C_{2D} ($=\varepsilon_0 \varepsilon_r / t$, where t is the thickness of dielectrics, ε_0 and ε_r are the vacuum and the relative permittivity, respectively).[7, 8, 11-15, 20-25] This huge variation in RN-TFTs might be attributed to various geometrical and electrical factors such as the number of percolation paths (N_{ch}) in an active channel, mask length (L_{mask}), mask width (W_{mask}), mean length of CNT (L_{CNT}), average nanotube density (ρ_{CNT}), surface roughness and film thickness of random network, degree of CNT alignment, electrical properties of the junction between CNTs and the series resistance (R_{sd}).[11, 23, 24] However, it can be mainly explained by a bad evaluation of the gate-to-channel capacitance (C_{gc}) in percolation-dominant 2D RN-TFTs based on C_{2D} and even inaccurate interpretation for measured capacitance value. Indeed, all the CNTs connected

to source (S) or drain (D) electrode, even outside a current percolation path, can be involved in capacitance-to-voltage (CV) measurement. Hence, it is necessary to obtain a more realistic value of C_{gc}, associated only to the CNTs that dominantly contribute to carrier conduction between S and D, for the accurate parameter evaluation of RN-TFTs without under/over-estimation.

In this study, the various electrical properties based on static and LFN characteristics of N-type 2D RN-TFTs were firstly evaluated with two different capacitance values, the simple C_{2D} plate capacitance model and the experimental C_{gc} directly measured by the split CV method, respectively. For the extraction of static electrical parameters such as low-field mobility (μ_0), mobility attenuation factor (θ) and threshold voltage (V_{th}), Y-function method (YFM) technique was used to alleviate R_{sd} influence.[26, 27] In addition, in order to have a better understanding of percolation effects and random aspects in such complex RN-TFTs, especially for the interpretation of C_{gc}, a 2D finite numerical percolation simulation was also performed. Furthermore, to study the electrical limitations of such RN-TFTs for practical electronics, LFN measurements were carried out and analyzed for different L_{mask} values. Finally, to have a good agreement based on static and LFN results, one-dimensional (1D) analytical capacitance model (C_{1D}) was suggested for an improved interpretation of C_{gc}.[28]

6.2 Device Fabrication Process and Electrical Measurement Conditions

Fabrication of RN-TFTs: To prepare iron catalyst, a mixture of a ferrocene solution and a conventional photoresist (AZ 5214E) was deposited on SiO_2 (400nm)/Si substrates. After photo-lithographic processes, the active channel areas were defined with additional burning process of the photoresist in an oxygen flow of 500sccm (1.5Torr) to eliminate of organic materials. For the growth of single walled CNTs, a homemade radiofrequency (13.56 MHz) remote water assisted plasma enhanced chemical vapor deposition system was employed. Then, the substrates were heated in a quartz tube to 450°C for 300s in a white light from a halogen lamp for nanotube synthesis. To improve the preferential semiconducting CNTs growth ratio, a humid atmosphere was introduced by evaporating water from a canister through a metering valve, resulting in an increase of 5mTorr in the base pressure. For this study, several active channel areas (L_{mask} (=2, 3, 5, 7, 10μm)×W_{mask} =40μm) of RN-TFTs were fabricated. The average diameter (d), length and density of CNTs in such fabricated RN-TFTs (d≈0.8~1.2 nm, L_{CNT}≈1~2μm, ρ_{CNT}≈20/μm^2, respectively) were directly estimated by a conventional scanning electron microscope (SEM, Hitachi, S-5500). The overall thickness of single walled CNT random network can be estimated about 1~2nm (almost mono- or bi-layer) by using SEM image as seen Fig. 6-

1(a). To make S and D electrodes, Ti (10nm)/Au (50nm) were deposited on the grown CNTs by a standard e-beam evaporation system. For a top-gate configuration, alumina (Al_2O_3) dielectric layer (t=50nm) was stacked by atomic layer deposition. Afterwards, conducting metal Ti (10nm)/Au (50nm) was sputtered for the top-gate electrode. Two hundred of individual RN-TFTs on a wafer can be fabricated after one full process. Optical device images of the fabricated RN-TFTs and a simplified cross section view are displayed in Figs 6-1(a) and (b), respectively.

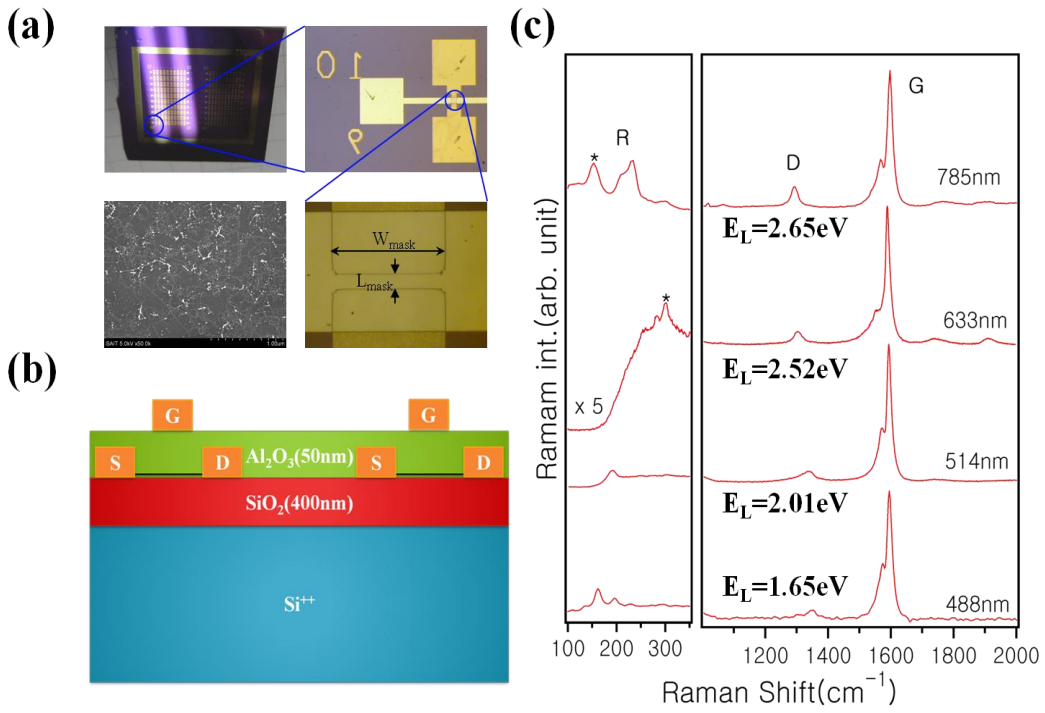


Figure 6-1 (a) Optical images of RN-TFTs and a representative SEM image (Hitachi, S-5500) of synthesized single-walled CNTs (b) A simplified cross section view of fabricated top-gate RN-TFTs. (c) Raman spectra of active channel areas of single-walled CNTs obtained with four different laser excitations ($1.65eV<E_L<2.65eV$). The peaks labeled with * are found to be instrumental artifacts.

To clearly demonstrate the preferentially grown semiconducting quality of single-walled CNTs, Raman spectra of active channel area with four different laser excitations ($1.65eV<E_L<2.65eV$) are displayed as in Fig. 6-1(c). The band in between ~1300 and ~1400cm^{-1} which often called D-band resulted from double-resonance scattering process was observed with low intensity.[29] Besides, the position of Raman peak at ~1590nm which often called the G-band since it is closely related with Raman band of graphite is almost independent of excitation energy. In addition to D and G band, there is unique mode, namely, a radial breathing mode or R-mode, which usually observed in low frequency region (~100 to 300cm^{-1}). With account for this unique band regime, the tube diameter can be evaluated. (w_R~224[cm^{-1}nm]/d_t[nm],

where d_t is the tube diameter and w_R is the wave number)[30] Further device fabrication details related with the quality and the high selective synthesis ratio of semiconducting CNTs can be found in previously published papers. [22, 31, 32]

Electrical Characterizations: Various $C_{gc}(V_{gs})$, $I_{ds}(V_{ds})$ and $I_{ds}(V_{gs})$ with respect to different V_{gs} and V_{ds} were directly measured depending on different L_{mask} by HP 4194a and HP 4155a, respectively. For the split CV method, G was connected to the high terminal with a fixed ac signal amplitude (=25mV) at 10kHz, S and D were connected together to the low terminal while zero bias was applied to the substrate of RN-TFTs.[27, 33] By this technique, the effects of isolated CNTs and parasitic pads capacitance can be efficiently excluded.[23, 33] For LFN noise measurements, Programmable Point-Probe Noise Measuring System (3PNMS) was employed at low frequency (f) range from 10Hz up to 10kHz as a function of V_{gs} and L_{mask}. All static and LFN measurements were done in a metal shielding box at room temperature (T=300K)

6.3 Static Parameter Extraction

6.3.1 Output Characteristic and Transfer Curves of RN-TFTs

Output characteristic $I_{ds}(V_{ds})$ and transfer curves $I_{ds}(V_{gs})$ of RN-TFTs with different L_{mask} were directly measured by HP 4155a at room temperature (T=300K). Figure 6-2(a) shows $I_{ds}(V_{ds})$ curves in case of L_{mask}=3μm depending on different top-gate bias potential (V_{gs}). It well indicates general N-type FET properties and Ohmic behavior near small drain-source voltage (V_{ds}) regime. In addition, typical $I_{ds}(V_{gs})$ depending on different L_{mask} and V_{gs} of top-gate RN-TFTs with fixed V_{ds}=50mV were plotted in Fig. 6-2(b). It clearly confirms also that the overall good N-type semiconducting quality of CNTs in RN-TFTs after Al_2O_3 passivation with the low minimum current level (I_{min}≈100fA) and high ratio between on-current and minimum current level ($I_{on}/I_{min}\geq10^5$, except for L_{mask}=2μm case, where it is still larger than 10^4). As displayed in Fig. 6-2(c), I_{on}/I_{min} ratio is mostly high enough to be regarded as that of semiconducting FETs. Only for L_{mask} values below 3μm, where I_{min} is significantly increased, a certain amount of metallic conductive paths may start to be involved, leading to S-D leakage below threshold. More detailed information about the semiconducting ratio and optical properties of single walled CNTs in RN-TFTs has already been published in Ref. [22, 31, 32].

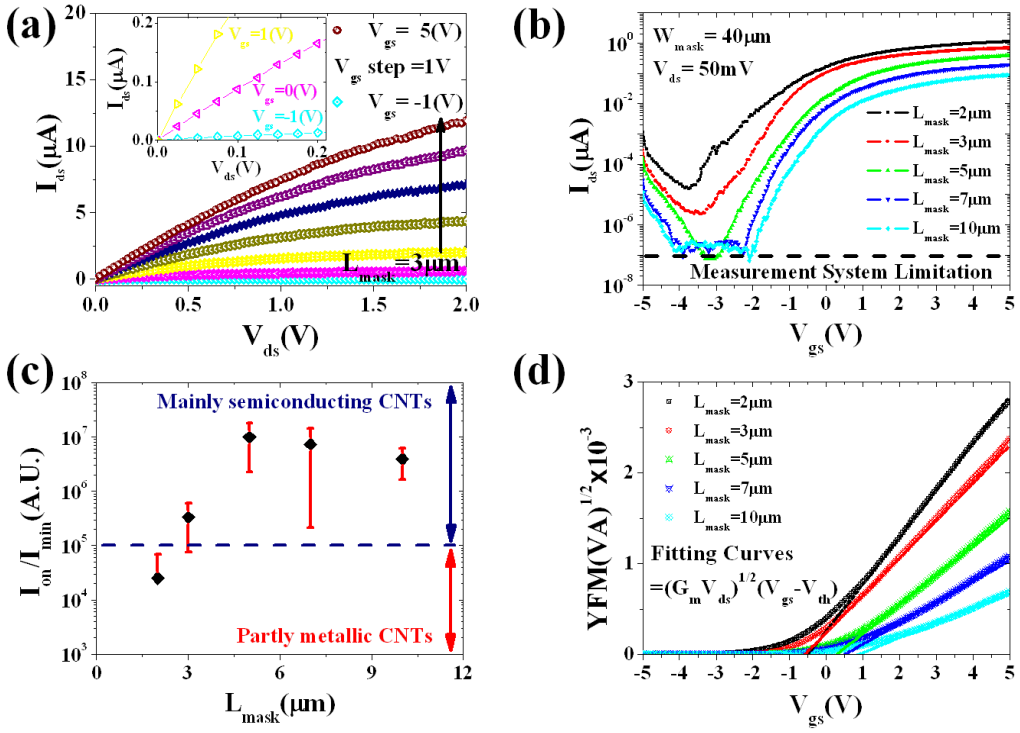


Figure 6-2 (a) Representative output characteristic $I_{ds}(V_{ds})$ curves of RN-TFTs depending on V_{gs} (from V_{gs}=-1V to 5V with V_{gs}=1V step) in case of L_{mask}=3μm. (inset: the magnification view of small V_{ds} region) (b) Typical transfer $I_{ds}(V_{gs})$ curves with respect to different L_{mask} at V_{ds}=50mV (c) I_{on} and I_{min} ratio versus L_{mask} (d) YFM(V_{gs}) (symbols) and corresponding fitting curves (dotted lines) with respect to L_{mask}.

For further electrical parameter evaluation in strong electron accumulation region, the YFM(V_{gs}) technique was used and it defined as follows,[26, 27]

$$YFM(V_{gs}) = I_{ds}/\sqrt{g_m} = \sqrt{G_m \cdot V_{ds}}(V_{gs} - V_{th}) \quad (6\text{-}1),$$

where g_m is the transconductance ($=\partial I_{ds}/\partial V_{gs}$), G_m is the transconductance parameter ($=\mu_0 C_{ox} W_{mask}/L_{mask}$), and C_{ox} is the top-gate oxide capacitance per unit area (F/cm^2). Figure 6-2(d) verifies that YFM(V_{gs}) shows good linearity and is thus in good agreement with Eq. (6-1) in the strong accumulation regime for all L_{msak} values. By this manner, various electrical parameters such as μ_0, θ, V_{th} and R_{sd} can be easily extracted without R_{sd} influence.[26, 27] It is worth noting that C_{ox} is the most important factor to determine the other electrical parameters. Hence, to avoid an under-/over- parameter estimation due to the use in RN-TFTs of the standard plate model C_{2D}, C_{gc} was directly measured by using the split CV method. After C_{gc} evaluation, further static electrical parameters extraction procedures will be followed in the next 6.3.2 section.

6.3.2 Split Capacitance-to-Voltage Curves of RN-TFTs

$C_{gc}(V_{gs})$ curves were directly measured by HP 4194a with V_{gs} ranging from -5V to 5V. Measurements were carried out for different L_{mask}. For the split CV method, the gate pad G was connected to the high terminal with a fixed ac signal amplitude (=25mV) at 10kHz, while S and D were connected together to the low terminal and zero bias was applied to the substrate.[27, 33] By this technique, the parasitic capacitances effects arisen from the isolated CNTs and S and D pads can be efficiently excluded.[23, 33]

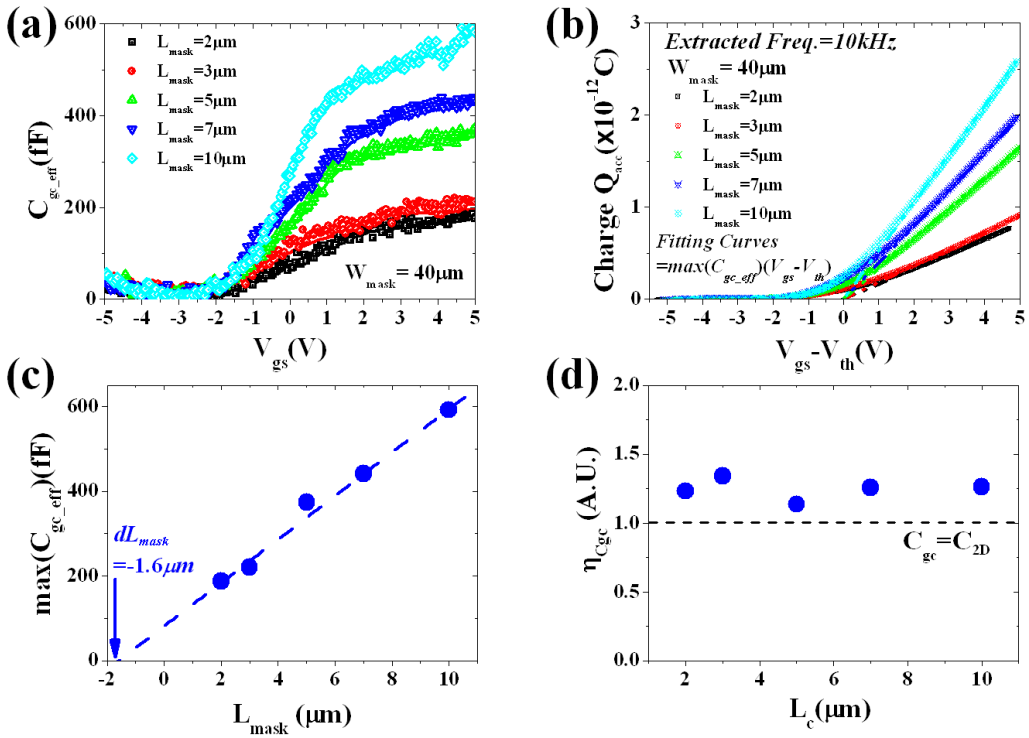


Figure 6-3 (a) $C_{gc\_eff}(V_{gs})$ curves of a top-gate RN-TFTs at f=10kHz (b) $Q_{acc}(V_{gs})$ (symbols) with linear fitting lines ($\approx max(C_{gc\_eff})\times(V_{gs}-V_{th})$, dotted lines) (c) $max(C_{gc\_eff})$ and (d) η_{Cgc} verses L_{mask} and L_C, respectively.

Representative $C_{gc\_eff}(V_{gs})$ curves of a top-gate RN-TFTs, after elimination of the parasitic capacitance taken at the minimum value of $C_{gc}(V_{gs})$, are presented in Fig. 6-3(a). It clearly indicates the formation of the electron accumulation channel for positive V_{gs}. In contrast, the onset of the hole accumulation can only be observed for very negative gate voltages, and cannot be fully reached. Hence, further analysis will focus on the electron accumulation region of CV characteristics. As seen in Fig. 6-3(a), C_{gc_eff} increased with V_{gs} and then saturated at high V_{gs} regime. This plateau corresponds to the maximum coupling capacitance when the electron accumulation is fully formed in the channel. By integrating $C_{gc\_eff}(V_{gs})$ with respect to V_{gs}, the accumulation charge (Q_{acc}) can be calculated. It was well fitted by the linear approximation, $Q_{acc}\approx max(C_{gc\_eff})\times(V_{gs}-V_{th})$, as plotted in Fig. 6-3(b). Moreover, the same method as for con-

ventional silicon based metal-oxide-semiconductor FETs (MOS-FETs) is used in this study to estimate gate length reduction, dL_{cap}, from CV measurements (dL_{mask}=dL_{cap}≈-1.6μm in this approach) as shown in Fig. 6-3(c).[27, 33] The negative dL_{cap} can be explained by an effective conduction length longer than gate length in RN-TFTs as a result of percolation between randomly oriented CNTs. Based on dL_{cap} value, two parameters are introduced in this approach, the effective length in for CV measurements L_C (=L_{mask}-dL_{cap}) and the overestimation factor compared to C_{2D}, η_{Cgc} (=$C_{2D}W_{mask}L_C$/[max(C_{gc_eff})]), indicating how much C_{2D} is overestimated compared to max(C_{gc_eff}). In such devices, an average η_{Cgc} value was found approximately ≈1.22, as displayed in Fig. 6-3(d). However, it is worth mentioning that the linear extrapolation method used in Fig. 6-3(c) should be taken with care for random network systems. Indeed, dL_{cap} can not be the same for all RN-TFTs and max(C_{gc_eff}) values could be easily influenced by percolation effects, with in fact a finite number of percolation channels. In addition, it may lead to a wrong conclusion if one used max(C_{gc_eff}) directly for device parameter extraction, without thorough consideration of dominant current percolation paths in RN-TFTs. In fact, depending on their path resistance (R_{path}), only a few percolation paths in RN-TFTs may dominantly contribute to carrier transport. For instance, even though all the CNTs are activated during CV measurements, they cannot contribute to carrier transport in $I_{ds}(V_{gs})$ if they are just electrically connected to S or D only, or if they construct a considerably resistive path due to the large number of junction (N_{jc}) and its corresponding resistance (R_{jc}) compared to the most conducting current path. Therefore, Q_{acc} in Fig. 6-3(b) can be directly associated to the total number of activated CNTs (N_{CNT}) connected to S or D in CV measurement. However, it is underlined that Q_{acc} cannot be considered as the charge involved in electrical current measurements in percolation-dominant 2D RN-TFTs. Further discussion about an alternative interpretation of max(C_{gc_eff}) in RN-TFTs will be given below in the numerical simulation section (Chapter 6.5). Hence, at first, in absence of any statement, all parameter extractions will be based on C_{2D} and max(C_{gc_eff}) in the following sections.

6.3.3 Electrical Parameter Evaluation

Figure 6-4(a) is displaying together four evaluations of the mobility: the field effect mobility μ_{fe} (=max(g_m)$L_{mask}V_{ds}$/[$C_{ox}W_{mask}$]) and the low-field mobility μ_0, each of them being extracted using either C_{2D} with L_{mask} or max(C_{gc_eff}) with L_C. They are plotted together as a function of L_{mask} and L_C, respectively. It clearly shows that μ_0 increases slightly when L_{mask} or L_C are reduced in both cases. This is because N_{jc} between S and D is decreased and N_{ch} is increased as L_{mask} is decreased. Therefore, if L_{mask} is below the mean free path of CNTs (λ_{CNT}≈1μm),[34] the contribution of R_{jc} could be shrunk, which would result in an enhancement

of the carrier mobility (μ) in RN-TFTs. Moreover, it can be mentioned that μ could be much improved by synthesizing longer or perfectly aligned CNTs in order to diminish the junction effects in the conducting paths.

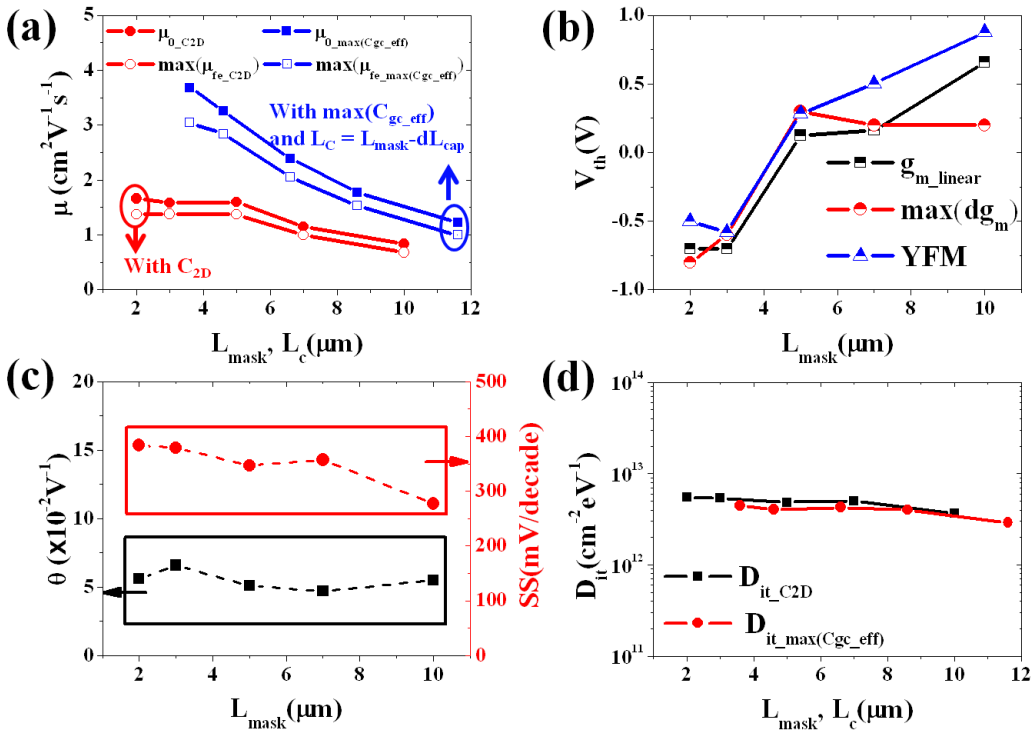


Figure 6-4 (a) μ_0 extracted from C_{2D} with L_{mask} (red lines) and μ_{fe} from max(C_{gc_eff}) with L_C (blue lines), respectively (b) V_{th} versus L_{mask} based on various V_{th} evaluation techniques (c) θ (circle) and SS (rectangular) with respect to different L_{mask} (d) D_{it} extracted from C_{2D} with L_{mask} (rectangular) and max(C_{gc_eff}) with L_C (circle), respectively.

For V_{th} evaluation, three methodologies which are standard for MOS-FETs were applied in this study: 1) linear extrapolation of drain current at the point of maximum $g_m(V_{gs})$, 2) V_{gs} point of the maximum value of derivative g_m, max(dg_m), 3) linear extrapolation to zero of YFM(V_{gs}).[33] The trend of V_{th} variation with respect to L_{mask} is mostly similar regardless of the extraction method as plotted in Fig. 6-4(b). In addition, the mobility attenuation factor at high transverse field θ extracted from YFM(V_{gs})[27, 33] and the subthreshold swing (SS) are also presented in Fig. 6-4(c), respectively. Values of θ are almost independent of L_{mask} (≈0.05[V^{-1}]), which implies that R_{sd} effects might be negligible in such RN-TFTs. Therefore, the overall electrical performances of such RN-TFTs are actually limited by transport in the CNTs placed underneath the gate and at their junctions. Furthermore, the interface trap density (D_{it}) was calculated from SS by using the following equation:[21, 35, 36]

$$D_{it} \approx \left(\frac{SS}{\ln(10) k_B T} - 1 \right) \frac{C_{ox}}{q} \quad (6\text{-}2),$$

where k_BT is the thermal energy and q is the electron unit-charge. As presented in Fig. 6-4(d), D_{it} values were ranging from $\approx 10^{12}$ to $10^{13} cm^{-2} \cdot eV^{-1}$. The gate dielectric was a high-κ Al_2O_3 layer. Extracted D_{it} values will be compared to the surface trap density (N_{st}) evaluated from LFN measurements in the following section (Chapter 6.4).

6.4 Low Frequency Noise Characteristics

LFN measurements have gained great attention to characterize the charge trapping centers in the dielectric layer and the minimum detectable signal amplitude.[20, 37-49] In addition, reduction of LFN level is essential for practical electronics such as high-speed or analog devices.[20, 37, 39-41, 48] To provide a diagnostic of noise sources of RN-TFTs, LFN measurement were carried out as a function of V_{gs} and L_{mask} in the low frequency (f) range, from 10Hz up to 10kHz, in a metal shielding box at room temperature (T=300K). To this end, Programmable Point-Probe Noise Measuring System (3PNMS) was employed. As seen in Fig. 6-5(a), the drain current power spectral density (PSD) was following the 1/f dependency at V_{ds}=50mV in the case of L_{mask}=7μm. With account for high ρ_{CNT}, the total LFN behaviors can be attributed to a large ensemble of Lorentzian noise sources based on individual CNTs and/or junctions between CNTs.[48, 50] Some previous studies have demonstrated that Schottky barriers at the contact between CNTs and S/D electrode have considerable impact on global LFN behavior.[42] However, in such RN-TFTs, Schottky barrier effects were negligible as shown by the Ohmic behavior in N-type output characteristic $I_{ds}(V_{ds})$ in the small V_{ds} region (see Fig. 6-2(a)), by the constant small value of θ regardless of L_{mask} (see Fig. 6-4(c)), and by the corresponding relatively small width-normalized R_{sd} value ($R_{sd} \times W_{mask}$; 40 to 410Ω·cm). Considering these factors, Schottky barrier effects seemed to be insignificant in our LFN analysis.

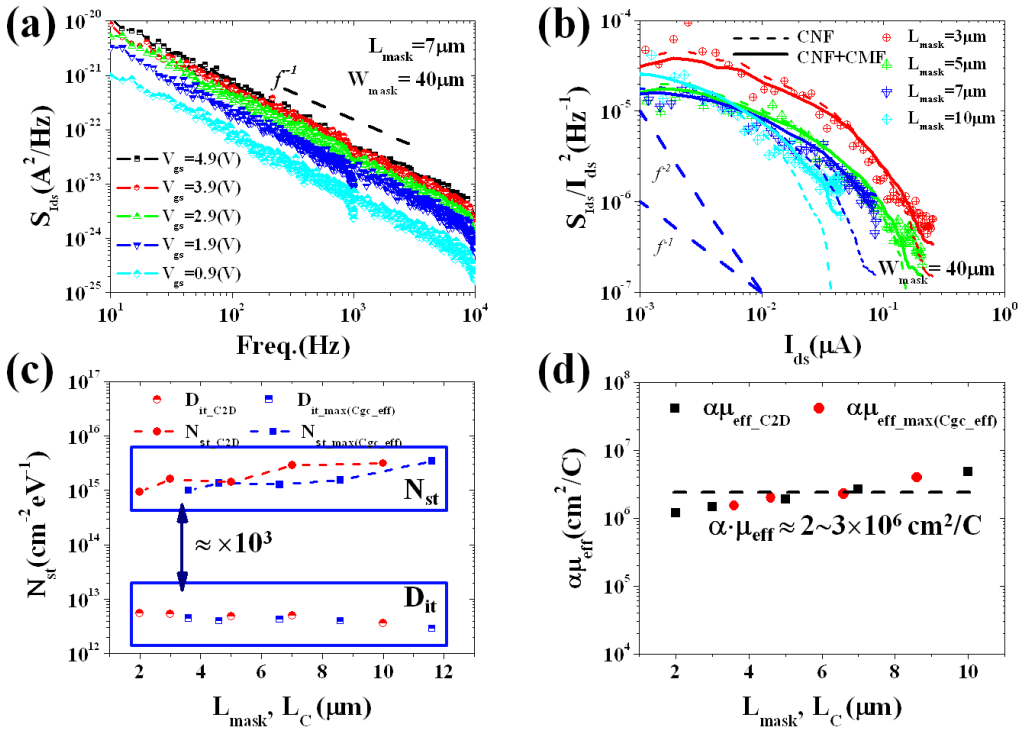


Figure 6-5 (a) LFN-PSD for different V_{gs} at V_{ds}=50mV (L_{mask}=7μm) (b) I_{ds} normalized LFN-PSD at f=10Hz (symbols) with CNF (dotted lines) and CNF-CMF (lines) fitting curves (c) Comparison of N_{st} and D_{it} versus L_{mask} and L_C, respectively (d) $\alpha\cdot\mu_{eff}$ depending on different L_{mask} and L_C, respectively.

The drain current normalized LFN-PSD (S_{Ids}/I_{ds}^2) at a given frequency (f=10Hz) and $S_{Vfb}(g_m/I_{ds})^2$ curves are displayed together as a function of I_{ds} and L_{mask} in Fig. 6-5(b). For the sake of LFN analysis, the carrier number fluctuation noise (CNF) model and the carrier number and correlated mobility fluctuation (CNF-CMF) model were employed in this study. They are defined as follows,

$$\text{CNF: } \frac{S_{I_{ds}}}{I_{ds}^{\ 2}} = S_{V_{fb}}\left(\frac{g_m}{I_{ds}}\right)^2 = \frac{q^2 k_B T N_{st}}{L_{mask} W_{mask} C_{ox}^{\ 2} f}\left(\frac{g_m}{I_{ds}}\right)^2 \quad (6\text{-}3),$$

$$\text{CNF-CMF: } \frac{S_{I_{ds}}}{I_{ds}^{\ 2}} = \left(1+\alpha\cdot\mu_{eff}\cdot C_{ox}\frac{I_{ds}}{g_m}\right)^2 S_{Vfb}\left(\frac{g_m}{I_{ds}}\right)^2 \quad (6\text{-}4),$$

where S_{Vfb} is the flat-band voltage PSD, μ_{eff} $(=\frac{\mu_0}{1+\theta(V_{gs}-V_{th})})$ is the effective mobility ($cm^2\cdot V^{-1}\cdot s^{-1}$), and α is the Coulomb scattering coefficient. The very good consistency between the CNF-CMF model and LFN data clearly demonstrates that noise sources do originate from the trapping-detrapping of carriers by the traps located in the gate dielectric surrounding the surface of CNTs. So far, various dimensions and types of carbon materials have been character-

ized, but as in bulk conductor. As a result, LFN behavior of carbon material has been predicted and explained by Hooge's mobility fluctuation model (HMF=$\frac{S_{I_{ds}}}{I_{ds}^{2}}=\frac{\alpha_H}{Nf}\approx\frac{\mu_{eff}\cdot q\cdot\alpha_H\cdot V_{ds}}{f\cdot L_{mask}^{2}\cdot I_{ds}}$, where α_H is Hooge's constant.)[51] However, HMF cannot be applicable to interpret LFN behavior in such devices as studied here. Especially in the subthreshold region, I_{ds} normalized LFN-PSD data were flattening instead of increasing when I_{ds} is decreased, as it would be the case for HMF. Hence, CNF-CMF is a more proper model to interpret LFN behavior in such RN-TFTs from depletion to accumulation region. In addition, the fact that the LFN contribution from R_{sd} to the total LFN was not visible in the high V_{gs} bias regime is further confirmed, as expected previous section. Based on S_{Vfb} from Eq. (6-4), N_{st} and $\alpha\cdot\mu_{eff}$ were evaluated using either C_{2D} or max(C_{gc_eff}) for different L_{mask} and L_C values, as drawn in Figs 6-5(c) and (d), respectively. Extracted mean values of N_{st} and $\alpha\cdot\mu_{eff}$ lie in the range from 10^{15} to $10^{16}cm^{-2}\cdot eV^{-1}$ and from 10^6 to 10^7 $cm^2\cdot C^{-1}$, respectively. Apparently, N_{st} values seem to be unrealistic compared to advanced silicon based MOS-FETs ($\approx10^{10}cm^{-2}\cdot eV^{-1}$ in high-κ dielectrics). However, considering only that the ratio between the equivalent number of defects per unit surface ($N_{st}k_BT\approx10^{13}cm^{-2}$) and the surface atom density of CNTs based on ρ_{CNT} and carbon to carbon atom distance ($\approx10^{15}cm^{-2}$) is about ~1%, N_{st} range can be plausible. Nevertheless, it is hard to understand why N_{st} is ~10^3 times larger than D_{it} extracted from SS. This big discrepancy could be mainly explained by a bad evaluation of C_{ox}. As discussed in previous section 6.3.2, even if all the CNTs in the active channel are capacitively coupled to the gate, not all of them contribute to dominant current paths in RN-TFTs. Indeed, a few main percolation paths can play a significant role for overall device operation in a 2D RN-TFTs system. Hence, to better understand these percolation phenomena and have an improved interpretation of C_{ox} in such complex 2D RN-TFTs, a finite 2D numerical percolation simulation was employed in this study. Besides, it should be noted that the large value of $\alpha\cdot\mu_{eff}$ might reflect a stronger Coulomb interaction than in silicon based MOSFETs.

6.5 Numerical 2D Percolation Simulation

6.5.1. Numerical simulation methodology

In order to account for the random aspects and percolation phenomena in such RN-TFTs, a homemade simulation methodology was developed based on the generation of sets of random arrays followed, for each of them, by the identification of the optimal current paths and their conversion into an equivalent circuit, for SPICE simulation of the I-V characteristics.

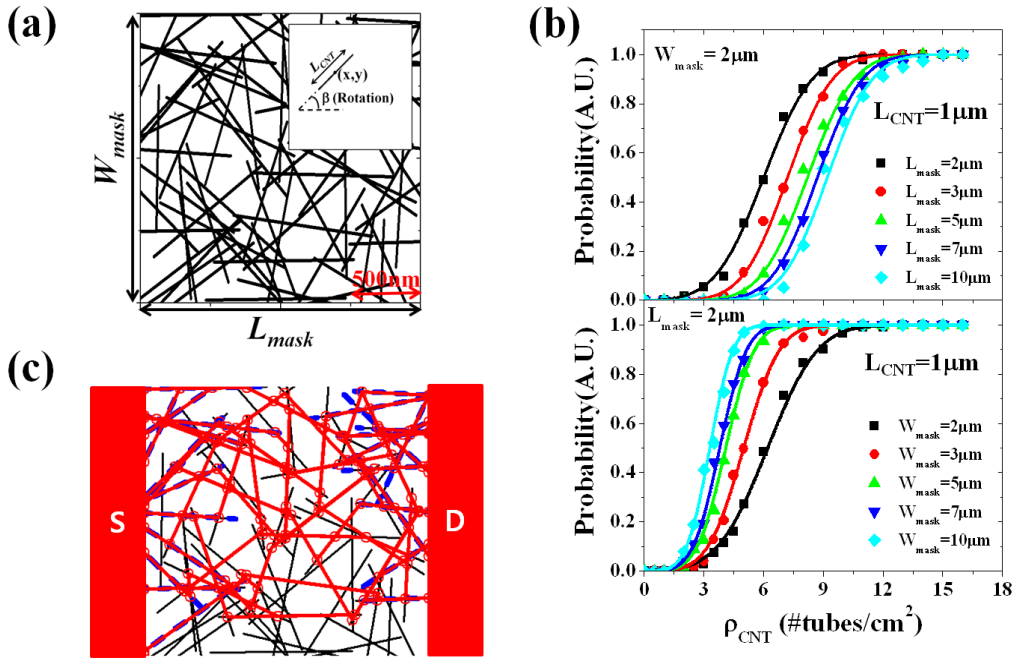


Figure 6-6 (a) A representative randomly generated set of 2D RN-TFTs (in case of L_{mask}=W_{mask}=2μm, ρ_{CNT}=#20/μm^2 and L_{CNT}=1μm) (b) P dependency on ρ_{CNT} as a function of L_{mask} for fixed W_{mask}=2μm (top) and P as a function of W_{mask} for fixed L_{mask}=2μm (bottom) (c) Visualized all possible optimal pathways (red lines) from CNTs directly connected to S to D electrode (blue dotted line) in the case of Figure 6(a). (Junction points between CNTs: small red circles)

In this approach, a certain number of CNTs (black lines in Fig. 6-6(a)), defined by $N_{tot}=\rho_{CNT}\times L_{mask}\times W_{mask}$, were randomly generated by selecting center positions (x_i, y_i) and orientation angles (β_i) in a finite 2D system ($L_{mask}\times W_{mask}$). We varied ρ_{CNT}, L_{mask} and W_{mask} , while L_{CNT}=1μm was kept constant for simplicity A representative set of simulation results was presented in Figs 6-6(a) and (c) (L_{mask}=W_{mask}=2μm, ρ_{CNT}=20/μm^2). Location of all the junctions between CNTs (red circles in Fig. 6-6(c)) and all the distances between two adjacent junctions were calculated by a mathematical matrix technique. Based on this matrix information, we can determine the percolation connectivity and estimate the shortest path and/or less resistive path, namely optimal path(s) from S to D (red lines in Fig. 6-6(c)), by using a modified Floyd's algorithm[52] with account for N_{jc}, R_{path}, and the total length of a single conduction path (L_{path}) from the ith to the jth CNT connected to S and D, respectively (see the blue dotted lines in Fig. 6-6(c)).[52-55] As a first step, to have a percolation probability (P), we further assumed that the CNTs have a different resistance depending on their effective contribution to the conduction channel length (l_d) along L_{path}. This resistance is simply defined as $R_{CNT}(l_d)=(4q^2/h)^{-1}(1+l_d/\lambda_{CNT})$ in the high gate bias regime, where h is the Planck constant.[34] Moreover, all R_{jc} are assumed identical with a median value taken from previous experimental results obtained between semiconducting CNTs, $R_{jc}=(0.01q^2/h)^{-1}$.[56] By this manner, P was repeatedly computed in terms of

L_{mask}, W_{mask}, and ρ_{CNT} in 2D finite system, as plotted in Fig. 6-6(b). The results were well fitted with the modified error function (erf) defined as follows,

$$P = \frac{1}{2}\left(1 + erf\left(\frac{x-\rho_{th}}{\sigma\sqrt{2}}\right)\right),\ erf(x) = \frac{2}{\sqrt{\pi}}\int_0^x e^{-t^2}dt \qquad (6\text{-}5),$$

where ρ_{th} is the percolation threshold, and σ is the standard deviation of distribution density. For more details in percolation results and simulation method, see Ref.[55]. Results clearly indicate that the percolation process is following a standard Gaussian distribution and that there is a much stronger dependency on W_{mask} than L_{mask}. Based on such behaviors, we can readily determine that the fabricated RN-TFTs were quite far from ρ_{th} and that percolation effects need to be accounted. In order to visualize optimal pathways from S to D in the generated set of Fig. 6-6(a), we indicated all the possible smallest resistive (optimal) pathways with red lines in Fig. 6-6(c). It clearly demonstrates that even if all CNTs are connected to each other in an active gate channel area, due to high ρ_{CNT}, the number of CNTs to make the most conducting paths from the i^{th} to the j^{th} CNT connected to S and D is only a small portion of N_{tot}.

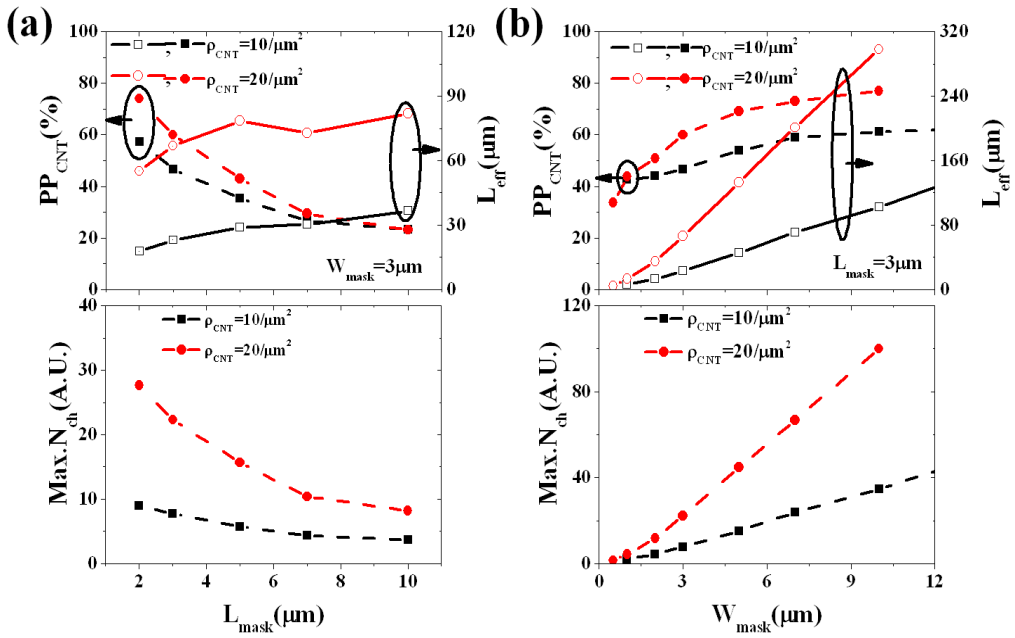


Figure 6-7 (a) PR_{CNT} and corresponding L_{eff} (top), and $Max.N_{ch}$ (bottom) depending on L_{mask} with fixed W_{mask}=3μm (b) Same parameters depending on W_{mask} with fixed L_{mask}=3μm.

Secondly, to have a better picture for percolation phenomenon and interpretation of C_{ox} in such complex 2D random network system, we introduced three indicators. The relative quantity of CNTs that bring high enough contribution to drain current (PR_{CNT}; the number of red sticks in each test set divided by N_{tot}), the total sum of l_d for these PR_{CNT} nanotubes ($L_{eff} = \sum l_d$), and the maximum number of channels ($Max.N_{ch}=L_{eff}/L_{mask}$) that would be ob-

tained by assuming that the CNTs counted in PR_{CNT} are perfectly aligned in the channels. As seen in Fig. 6-7(a), PR_{CNT} is decreased as L_{mask} is increased due to reduced percolation probability P in long channels. In other words, higher ρ_{CNT} should be needed to reach the percolation in longer L_{mask} devices compared to shorter L_{mask} ones. For this reason, PR_{CNT} and $Max.N_{ch}$ are decreased as L_{mask} is increased. On the contrary, as displayed in Fig. 6-7(b), PR_{CNT} is almost linearly increasing as W_{mask} is increased. It can be explained by the fact that if W_{mask} is widened twice, there is twice as much chance to build percolation paths in the channel. Hence, PR_{CNT} and $Max.N_{ch}$ can be increased owing to the increased P. With account for the simulation tendency, we can expect $Max.N_{ch}$ for experimental results assuming that all the CNTs are perfectly aligned and mainly participating to a conduction path. By this approximation, the width density D_W (=$Max.N_{ch}/W_{mask}$) can be readily obtained.

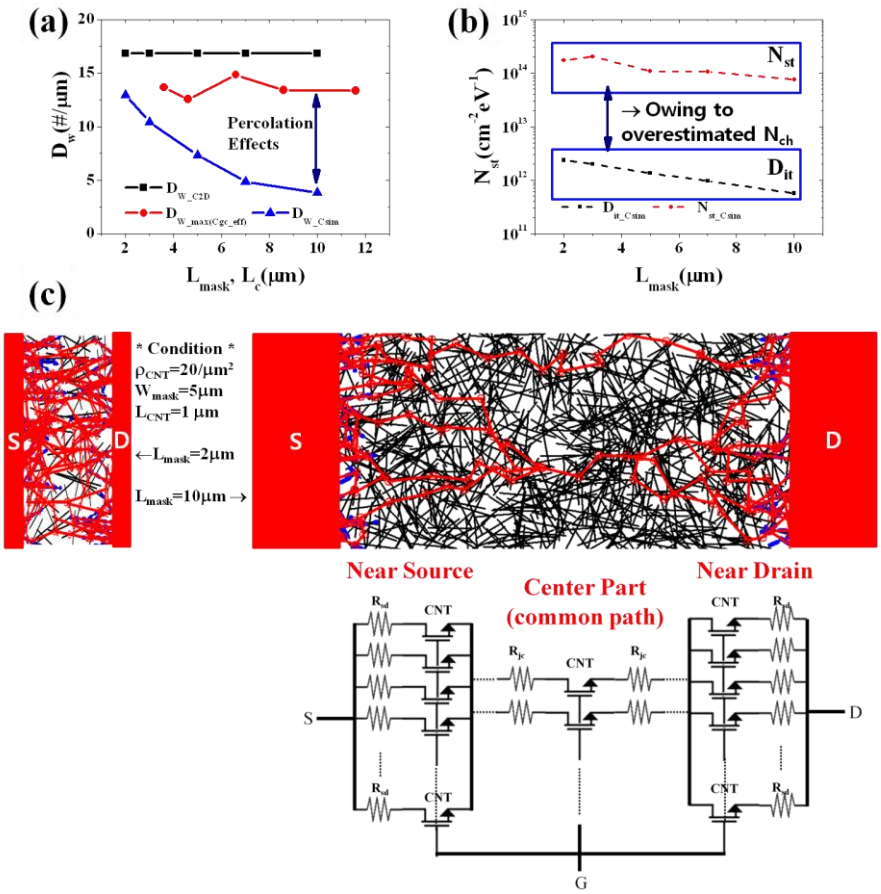


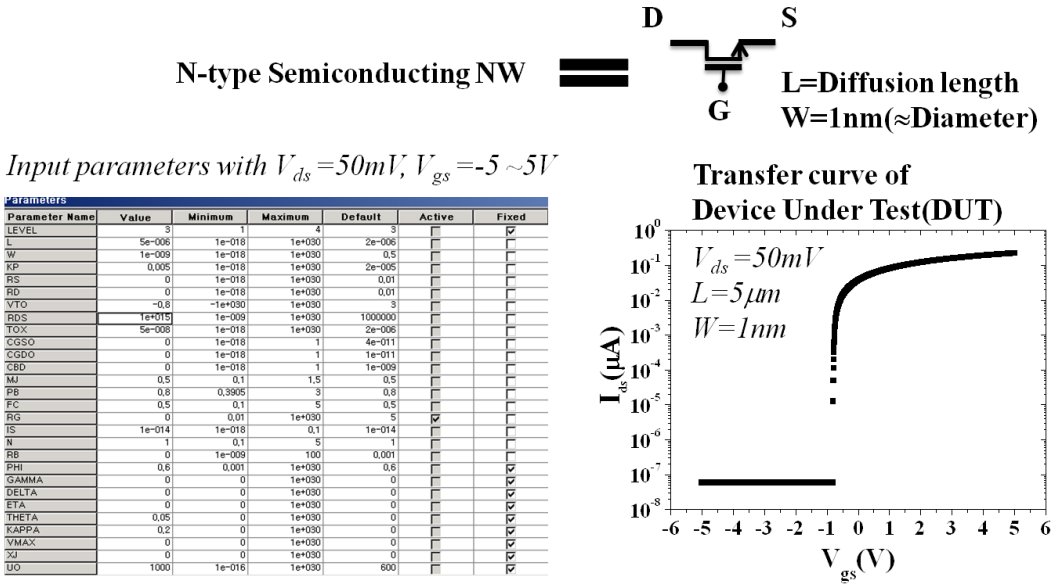
Figure 6-8 (a) D_W based on C_{2D}, max(C_{gc_eff}), and C_{Sim} (b) N_{st} and D_{it} extracted from C_{Sim} (c) Comparison the effective D_{W_Csim} between L_{mask}=2μm and L_{mask}=10μm with fixed W_{mask}=5μm in random network system. (Simplified electrical equivalent circuit was displayed)

For comparison of the D_w values based on C_{2D}, max(C_{gc_eff}) and simulation results, the following relations 1) $D_{W\_C2D}=C_{2D}/C_{1D}$, 2) $D_{W\_max(Cgc\_eff)}=max(C_{gc\_eff})/C_{1D}$, and 3)

D_{W_Csim}=Max.N_{ch}/W_{mask} were used, respectively, as displayed in Fig. 6-8(a). Especially, to obtain the gate coupling capacitance (C_{Sim}) based on the simulation results, D_{W_Csim} was applied to rigorous CNT capacitance model for perfectly aligned system. To confirm the effectiveness of C_{Sim}, N_{st} and D_{it} were recalculated and compared together in Fig. 6-8(b). The discrepancy between the two values was reduced by one decade, but still remains large. It can be attributed to the overestimation of N_{ch} arising from the assumption that all the CNTs are perfectly aligned in the channel and participating to carrier transport. In addition, we counted all possible pathways from S to D regardless of R_{path}. Indeed, if few junctions are more existing compared to the most conducting percolation path, it will not have a significant impact on the total current. Moreover, as displayed in Fig. 6-8(c), there are not many low-resistance conduction paths when L_{mask} is increased. This is due to the fact that current concentrates towards a few optimal and dominant CNT paths, which are shared by the different channels. Therefore, in realistic situation, D_W can be much smaller than in our previous assumption of a perfectly aligned system.

6.5.2. Spice Simulation

SPICE simulator has been employed for complex circuit analysis including active and passive devices for various purposes of users.[53] It is a very efficient, easy to access and powerful tool to find a desired solution. To take advantage of these virtues, we converted the previously generated sets of RN-TFTs into a netlist for SPICE simulator. The aim is to obtain an accurate electrical equivalent circuit of RN-TFTs containing circuit parameter information such as V_{ds} and V_{gs} bias conditions, connectivity among all nodes, a proper model for CNTs including R_{jc}, R_{sd}, l_d of each CNT, and various electrical parameters to reflect desired model. For the sake of simplicity, we adopted an ideal silicon based n-type FETs instead of precise single-walled CNT model. This is sufficient to demonstrate this methodology. (See the below Fig. 6-9)



Parameters

Parameter Name	Value	Minimum	Maximum	Default	Active	Fixed
LEVEL	3	1	4	3		☑
L	5e-006	1e-018	1e+030	2e-006		
W	1e-009	1e-018	1e+030	0,5		
KP	0,005	1e-018	1e+030	2e-005		
RS	0	1e-018	1e+030	0,01		
RD	0	1e-018	1e+030	0,01		
VTO	-0,8	-1e+030	1e+030	3		
RDS	1e+015	1e-009	1e+030	1000000		
TOX	5e-008	1e-018	1e+030	2e-006		
CGSO	0	1e-018	1	4e-011		
CGDO	0	1e-018	1	1e-011		
CBD	0	1e-018	1	1e-009		
MJ	0,5	0,1	1,5	0,5		
PB	0,8	0,3905	3	0,8		
FC	0,5	0,1	5	0,5		
RG	0	0,01	1e+030	5	☑	
IS	1e-014	1e-018	0,1	1e-014		
N	1	0,1	5	1		
RB	0	1e-009	100	0,001		
PHI	0,6	0,001	1e+030	0,6		☑
GAMMA	0	0	1e+030	0		☑
DELTA	0	0	1e+030	0		☑
ETA	0	0	1e+030	0		☑
THETA	0,05	0	1e+030	0		☑
KAPPA	0,2	0	1e+030	0		☑
VMAX	0	0	1e+030	0		☑
XJ	0	0	1e+030	0		☑
UO	1000	1e-016	1e+030	600		☑

Figure 6-9. Various electrical parameter list of N-type silicon semiconducting NW in P-Spice simulator and its corresponding representative transfer curves. (V_{ds}=50mV, silicon channel length and width are 5μm and 1nm, respectively.)

As a reference data, various transfer and output curves of the used model are displayed in the insets of Fig. 6-10 with V_{ds}=50mV, l_d=5μm, d=1nm. Remember, however, that each CNT contributing to the current will feature different parameters, especially in what concerns l_d and V_{ds}. Typical $I_{ds}(V_{gs})$ and $I_{ds}(V_{ds})$ FET characteristics, simulated for the generated RN-TFTs (L_{mask}=W_{mask}=3μm) are plotted in Figs 6-10(a) and (b) for different values of ρ_{CNT}. The linear and non-linear behaviors of test sets of RN-TFTs are successfully monitored.

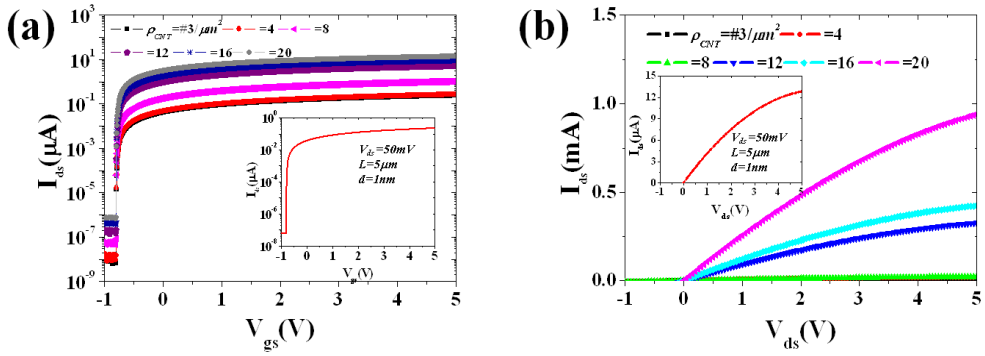


Figure 6-10 SPICE simulation results of (a) transfer curves $I_{ds}(V_{gs})$ and (b) output characteristics depending on different ρ_{CNT} based on l_d.(L_{mask}=W_{mask}=3μm)

A methodology to simulate 2D random networks of CNTs by combination with SPICE simulation was demonstrated to simulate their electrical properties. This methodology was demonstrated with various geometry factors. Percolation probability was simulated and its de-

pendence to ρ_{CNT} was well-fitted with an error function. Moreover, to find out the optimal current paths into complex connectivity patterns, we accounted for a detailed electrical model including the resistivity of each conductive segment in each path, number of junctions, junctions and contact resistances (with parameters l_d, N_{jc}, R_{jc} and R_{sd}). It was then possible to evaluate the percentage of CNTs that effectively contribute to current and the maximum number of conduction pathway(s) for C_{gc} evaluation. Finally, to extend usability and accessibility, a SPICE simulator was employed. To do this, test sets of RN-TFTs were converted into their equivalent electrical circuits and simulated. This methodology is versatile and can be used for 2D random network systems based on conducting NWs, CNTs, nano-fibers and composites, for many electronic applications such as thin film transistors, bio/gas sensors and transparent electrodes. Given an equivalent model for the elementary nanostructure involved in the network, our methodology permits an electrical study of random networks of such nanostructures which can be directly applied for practical application.

6.6 Effective Gate Coupling Capacitance Model

Within previous chapters, static and LFN characteristics were investigated based on different capacitance model, C_{2D}, max(C_{gc_eff}), and C_{Sim}. However, there was still inconsistency between D_{it} and N_{st} regardless of approaches. It can be mainly explained by the overestimated N_{ch}, however, the effective gate coupling capacitance (C_{eff}) in RN-TFTs is still ambiguous. With account for all aspects discussed in previous sections, we can propose that C_{1D} could be a much realistic capacitance model than C_{2D} for the evaluation of C_{ox}, and even more realistic than measured C_{gc} and C_{Sim} in 2D RN-TFT system. This is because the main conduction mechanism in such system was based on 1D semiconducting CNTs (not metallic CNTs) and few percolation pathways were able to dominantly participate to carrier transport through 1D CNTs. Hence, to qualitatively demonstrate this approach, firstly we plotted a simplified schematic of our concept in inset of Fig. 6-11(a). If we consider that screening and coupling effects are bringing a relative small contribution to total effective gate capacitance with a random network configuration, the effective total length (L_{tot}) can be evaluated from max(C_{gc_eff}) and the 1D capacitance C_{1D} ($=2\pi\varepsilon_0\varepsilon_r/\ln(4t/d)$). To this end, we defined six parameters: 1) L_S and C_S; the total sum of length of CNTs ($L_S=\sum_j L_{S_j}$) and its corresponding capacitance ($C_S=\sum_j C_{S_j}$) which are electrically connected to S only, 2) L_D and C_D; as the same definitions for D only ($L_D=\sum_j L_{D_j}$ and $C_D=\sum_j C_{D_j}$), 3) L_{SD} and C_{SD}; as the same definitions for S and D simultaneously only ($L_{SD}=\sum_j L_{SD_j}$ and $C_{SD}=\sum_j C_{SD_j}$), respectively. The sum of these lengths and capacitances

should be equal to L_{tot} ($\approx L_S+L_D+L_{SD}$) and max(C_{gc_eff}) ($\approx C_S+C_D+C_{SD}$), respectively. Note that the capacitance contribution from isolated CNTs can be excluded by employing the split CV method. By this way, C_{eff} in RN-TFTs should be defined by only accounting for L_{SD} and C_{SD} as defined below,

$$C_{eff} = \frac{C_{SD}}{L_{SD}} \approx \frac{1}{L_{SD}}\left(\max(C_{gc\_eff}) \times \frac{L_{SD}}{L_{tot}}\right) \approx \frac{\max(C_{gc\_eff})}{L_{tot}} \approx C_{1D} \quad (6\text{-}6).$$

Secondly, we notice that μ_0 or μ_{fe} should take similar values in RN-TFTs and in 1D CNT-FETs for L_{mask}=2μm, with maximum reported values $\mu_{fe} \approx 10^5 cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature. Indeed, if we use C_{2D} or max(C_{gc_eff}) for μ_{fe} evaluation owing to the large number of N_{ch} resulting from high ρ_{CNT}, the effective impacts of N_{jc} and R_{jc} on μ_0 (or μ_{fe}) can be neglected with the compatible L_{CNT} and λ_{CNT} with L_{mask} in such RN-TFTs. Furthermore, R_{sd} effects were already excluded by YFM technique. Therefore, it is apparent that this severe underestimation of μ_0 (or μ_{fe}) in such RN-TFTs compared to that of 1D CNT-FETs should mainly result from bad C_{ox} evaluation.

Third, the theoretical capacitance range obtained from between Eqs (6-2) and (6-4) to make N_{st} coincided with D_{it} should have following relation,

$$C_{ox} = \left(\frac{SS}{\ln(10)k_BT} - 1\right)\frac{qk_BT}{S_{V_{fb}} L_{mask} W_{mask} f} \approx \frac{C_{1D}}{W_{mask}} \quad (6\text{-}7).$$

Based on this approach, we revisited the previous parameter extraction procedures with C_{1D}. As presented in Figs 6-11(a) and (b), μ_0 and μ_{fe} were found in a range from $0.56\sim1.12\times10^3 cm^2 \cdot V^{-1} \cdot s^{-1}$ and D_{it} and N_{st} were lying approximately around $10^7\sim10^8 cm^{-1} \cdot eV^{-1}$, respectively. Mobility dependence with L_{mask} shows similar trend as in chapter 6.3.3, but the values are more realistic, one or two decade smaller than for 1D CNT-FETs due to junction effects between CNTs in our 2D RN-TFTs. In addition, the big discrepancy between D_{it} and N_{st} is now fully removed. Furthermore, it is a few times larger than N_{st} calculated from LFN amplitude data from previous works on 1D CNT-FETs with high-k dielectrics. This could be another important evidence to prove the effectiveness of this approach. Indeed, when N_{ch} is close to 1, N_{st} in multi-channel should be N_{ch} times smaller to get the same I_{ds}-normalized LFN-PSD. This is basically why LFN has a larger relative impact in small scaled devices than in large-scaled devices in device physics. Therefore, the fact that the value of N_{st} extracted from 2D RN-TFTs were only a few times larger than that of 1D CNT-TFTs means that there might be only a few conduction paths in the channel or LFN stemming from the junctions between CNTs could be added to the total LFN behavior.

Besides, it is worth mentioning that L_{tot} and the experimentally measured ρ_{CNT}' can be estimated by $L_{tot} \approx \max(C_{gc\_eff})/C_{1D}$ and $(L_{tot}/L_{CNT})/(L_{mask} \cdot W_{mask})$, respectively. This could be another alternative method to evaluate the effective ρ_{CNT} based on the split-CV technique incorporated with C_{1D} instead of using an optical image processing method.

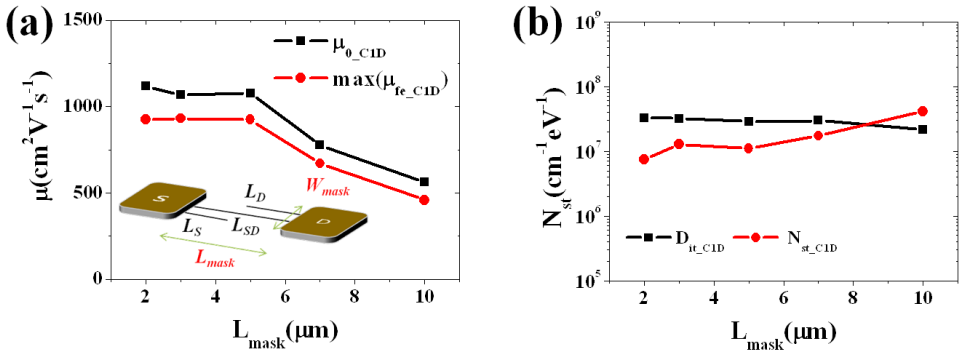


Figure 6-11 μ_0 and μ_{fe} extracted from C_{1D} (inset: simplified device configuration of RN-TFTs for the split CV measurements) (b) Recalculated N_{st} and D_{it} with C_{1D} versus L_{mask}, respectively.

6.7 Conclusion

Static and LFN characterizations of RN-TFTs were presented for different gate lengths in this chapter. To exclude R_{sd} effects, the YFM method was applied for the extraction of electrical parameters such as μ_0, V_{th}, and R_{sd}. To get rid of the capacitance effects originated from isolated CNTs islands and to directly measure C_{gc}, the split CV measurement technique was used. Moreover, to get a better interpretation of C_{gc} in percolation-dominated 2D RN-TFTs, a homemade 2D finite numerical simulation by combination with SPICE simulation was developed. LFN measurements also were carried out and the results were well interpreted by the carrier number fluctuations with correlated mobility fluctuation (CNF-CMF) model. A detailed analysis of N_{st} and $\alpha \cdot \mu_{eff}$ was firstly carried out based on various capacitance models. Finally, a C_{1D} based model was suggested and applied. It provided better consistency between all electrical parameters based on experimental and simulation results. This C_{1D} based model was found the most appropriate model to evaluate the electrical parameters in both static and LFN behaviors in n-type 2D RN-TFTs.

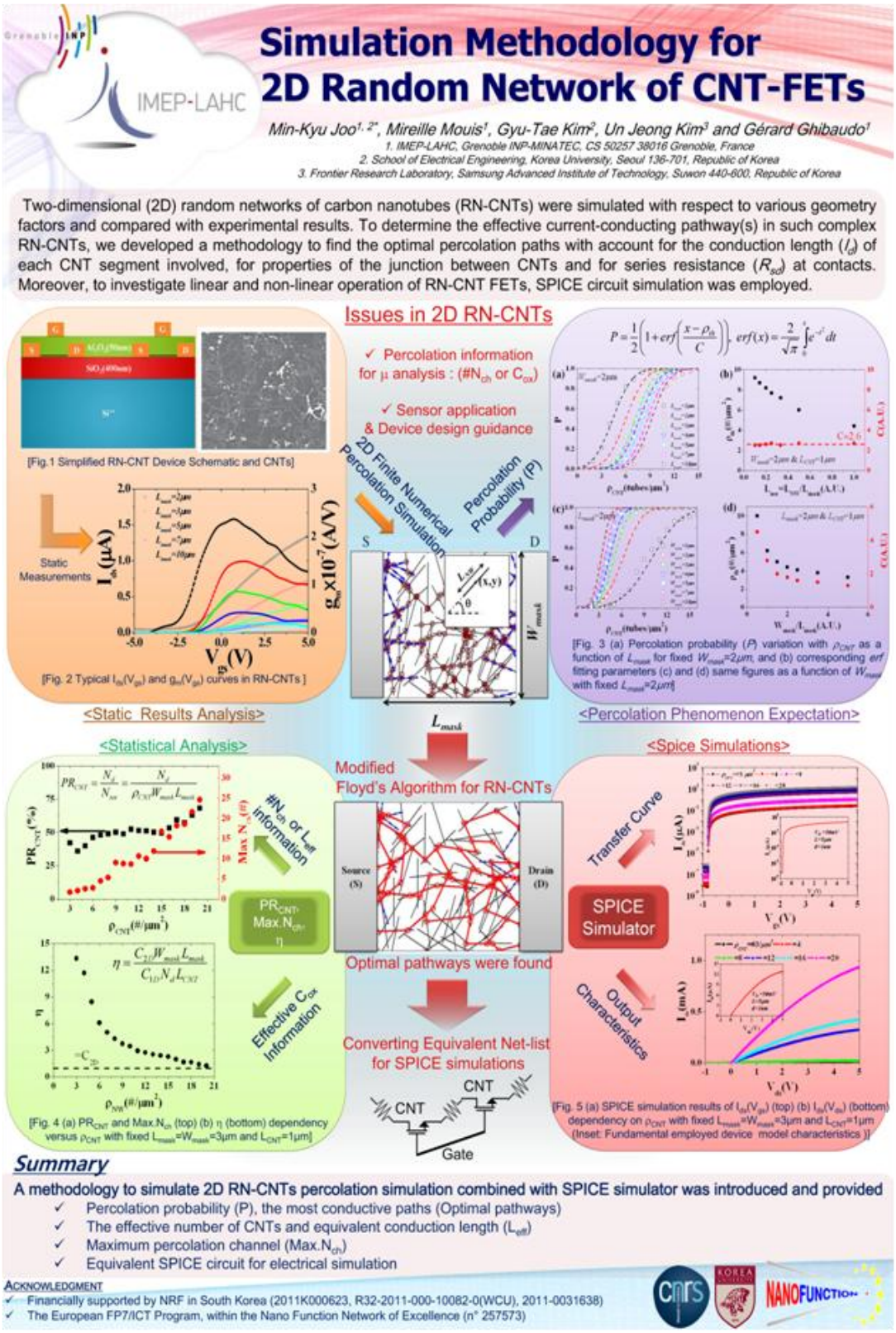


Figure 6-12. Poster for 2013 ULIS conference

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7. Thermoelectric power of single walled carbon nanotube networks

Chapter 7 Abstract

The thermoelectric power (TEP) of single walled carbon nanotube (SWCNT) thin films in pure metallic SWCNT (m-SWCNT) and pure semiconducting SWCNT (s-SWCNT) networks as well as in m- and s-SWCNT mixtures is investigated. The TEP measured on the pure s-SWCNT film (≈88μV/K) is found to be almost seven times higher than that of the m-SWCNTs (≈13μV/K). Moreover, a quasi-linear increase of TEP of the mixed SWCNT networks is observed as the fraction of s-SWCNTs is increased. The experimentally determined relationship between TEP and the fraction of s-SWCNTs in the mixture allows fast and simple quantitative analysis of the s:m ratio in any as-prepared heterogeneous SWCNT network. Furthermore, a semi-empirical model analyzing the effect of the inter-tube junctions is proposed and applied to describe the thermoelectric behavior of the prepared SWCNT networks. The results of calculations match well with the experimental data and clearly demonstrate that the measured TEP of thin SWCNT films is mainly controlled by the inter-tube junctions.

7.1 Introduction

Single walled carbon nanotube (SWCNT) thin film networks have been investigated for use in a variety of applications such as solar cells,[1, 2] field-effect transistors,[3, 4] photovoltaics,[5] flat-panel displays[6], and thermoelectric power generators.[7-9] In particular, SWCNT thin films are considered as attractive candidates to replace traditional transparent conducting oxides (TCOs) such as In_2O_3:Sn, SnO_2:F, or ZnO:Al[10] due to their low cost fabrication, high flexibility, and non-toxicity. In order to fully realize the potential of SWCNT networks for flexible devices, a fundamental understanding of the inherent electrical and thermal transport properties is essential. For this reason, many research groups have considered SWCNT network morphology,[11] chemical dopants,[12, 13] surface defects,[14] tube chiralities,[15] and band structure[15] in their studies. But there are still questions remained to be clarified in the random SWCNT network, especially the effect of inter-tube junctions on the network electrical and thermal transport. In addition, the electronic type of tubes and the ratio between m-SWCNTs and s-SWCNTs in a network can significantly modify its electrical/thermal properties. Therefore, mono-dispersed SWCNTs are expected to improve the electronic homogeneity of the films in terms of performance optimization.

The electrical conductivity of SWCNT thin films with homogeneous electronic type and precisely tuned ratios of m- and s-SWCNTs has been studied by several research groups.[10, 16-18] However, the effect of electronic type on the thermoelectric power (TEP) of thin film s was not reported so far. Moreover, the commonly fabricated entangled SWCNT networks were assumed to be a heterogeneous mixture of m-SWCNTs and s-SWCNTs in a ratio of 1:2. The measured TEP of such films was a result of ensemble effects stemming from both m- and s-SWCNTs. As a consequence, large differences of TEP arising from diverse m:s ratios in heterogeneous SWCNT networks were observed.[19-21] This chapter will mainly describe the thermoelectric properties of the SWCNT thin films of mono-dispersed m- and s-SWCNTs and their mixtures with defined m:s ratios. By considering the role of inter-tube junctions in the TEP, our investigations can contribute to the elucidation of the transport mechanism through SWCNT networks towards optimization of thermoelectric materials based on SWCNT networks.

7.2 Sample Preparation and Measurement Method

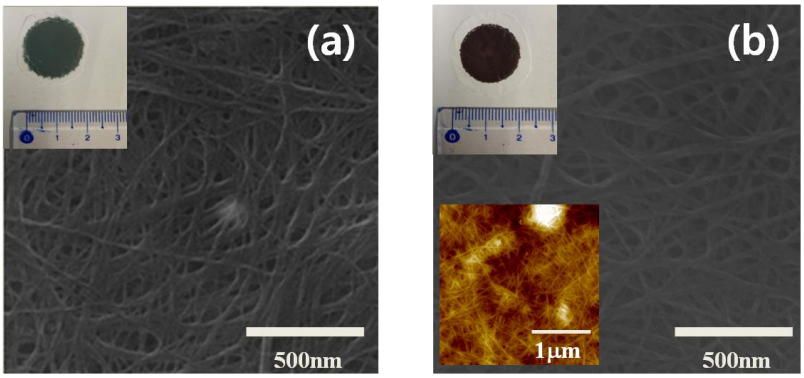

Figure 7-1 Representative SEM images of high-purity (a) m-SWCNT (b) and s-SWCNT thin films, respectively. Insets show their photographs after filtration. Additionally, atomic force microscope image of s-SWCNTs also presented in inset (b).

Sample Preparation: The mono-dispersed m- and s-SWCNTs with a purity higher than 99% used in this study were synthesized by the arc-discharge procedure and purchased in form of dispersion with 1wt% surfactant from NanoIntegris Inc. The separation of SWCNTs into pure electronic types was performed by a density gradient ultracentrifugation. The mean length of the s-SWCNTs was ≈1μm (See an inset of Fig. 7-1(b)), while that of the m-SWCNTs was ≈0.5μm. The average diameter of the both types of tubes was ≈1.4nm. The SWCNT concentration in the both solutions was 0.001 mg/ml. The flexible SWCNT thin films of mono-dispersed m- and s-SWCNTs and their mixtures with varying m:s ratio were prepared by vacuum filtration of 10mL of homogeneous electronic type SWCNT dispersions and 10mL of corresponding mixture using a PC membrane (pore size 0.4μm, Millipore). The surfactant was removed by rinsing several times with de-ionized water. The SWCNT thin films deposited on the membrane were dried at 80℃ for 30min to evaporate water.

Measurement Set-up The surface morphology of the prepared SWCNT thin films was observed by using a scanning electron microscope (SEM, Hitachi S-4800). To confirm the ratio of the m- and s-SWCNTs in the prepared mixtures the UV-vis-NIR absorption spectra (Cary 5000) were analyzed. To measure the electrical conductivity, the SWCNT thin films supported by the PC membrane were cut into narrow strips, typically 10×30 mm. Each sample was then pressure-contacted with four parallel metallic wires to perform the standard four probe measurement at room temperature. Current-voltage (I-V) sweeps were carried out using a Keithley 238 as the current source and a 34401A multi-meter from Hewlett-Packard (HP) for the voltage measurement.

Based on the geometrical factors and the slope of I-V curve, the electrical conductivity of the SWCNT samples was determined. For the TEP measurements, a temperature gradient

(ΔT) was induced along the film stripe by heating one end and leaving the other end to be exposed to air. Two platinum (Pt 100Ω) resistors were clamped with electrical contacts at both ends of the sample to measure temperature. TEP (called also Seebeck coefficient, S) was then calculated from the following expression, $S=-\Delta V/\Delta T$, where ΔV is the thermoelectric voltage induced by ΔT. The error bars represent a variation of single measurements upon different samples of the same kind.

7.3 Optical UV-vis-NIR Range Analysis of Precisely Tuned Ratio of Semiconducting and Metallic SWCNTs

The properties of mono-dispersed m- and s-SWCNT networks will be characterized in detail at first in order to simply exclude the Schottky junction effect between metallic and semiconducting tubes. Figures 7-1(a) and (b) show the SEM images of high purity m- and s-SWCNT thin films deposited on the polycarbonate (PC) membrane, respectively. Their corresponding photographs in insets display the typical green color of the m-SWCNT thin films and the brown color of the s-SWCNT thin films, respectively. The microscopic structure, especially the surface morphology appears very similar for both types of SWCNT films. Long, narrow and interwoven bundles forming uniform, pure, impurity free networks with a high density of inter-tube junctions are clearly visible.

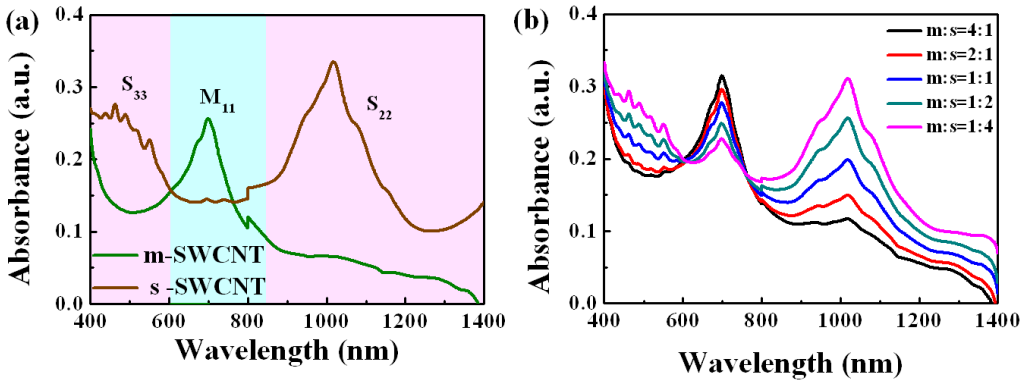

Figure 7-2 (a) The UV-vis-NIR absorbance of the type separated m- and s-SWCNT dispersions and (b) that of the mixtures with varying m:s ratio.

To prove the quality of the homogeneous electronic type, the SWCNT absorption measurement of the purchased dispersions in the UV-vis-NIR range was carried out. The corresponding spectra are presented in Figure 7-2(a). The clearly separated with a deep plateau between the absorption peaks attributed to the electronic transitions between the van Hove singularities for semiconducting tubes S_{22} (900-1270nm) and S_{33} (450-630nm) are characteristic for

mono-dispersed semiconducting samples.[22, 23] Also the high intensity peak M_{11} (600-850nm) without any side bands in the spectrum of metallic tubes indicates high purity samples. Based on these results, we measured the UV-vis-NIR absorption spectra of SWCNT mixtures with tuning the m:s ratio. The systematic changes in the spectra exhibiting two isosbestic points clearly demonstrate the presence of two chemical species showing absorption proportional to their concentration (Fig. 7-2(b)). As a consequence, the ratio of integrated area underneath the M_{11} and the S_{22} absorption bands reflects the m:s ratio in the mixed SWCNT samples.[10, 24] Hence, with account for results of Figs 7-2(a) and (b), the precision of m:s ratio of SWCNT can be clearly confirmed.

7.4 Theoretical Modeling with account for the Effect of Junction TEP in Mono-dispersed SWCNT networks

The TEP expressed by the Seebeck coefficient S and electrical conductivity of the type separated m- and s-SWCNT thin films are presented in Fig. 7-3. The electrical conductivity of our SWCNT films was about 270 S/cm for s-SWCNTs and 300 S/cm for m-SWCNTs, giving a conductivity ratio σ_s/σ_m=0.77. A high TEP was measured for s-SWCNTs (≈88μV/K) and a relatively low for m-SWCNT thin films (≈13μV/K). The literature data reveal that the measured TEP of an individual semiconducting SWCNT and of graphite is ≈42μV/K[25] and ≈10μV/K,[26] respectively. While the TEP of the m-SWCNT network can be comparable with that of graphite, it is underlined that there is a quite big discrepancy between the TEP of the individual s-SWCNT and that of here measured s-SWCNT network. Since the TEP is independent of any geometrical factors, the found deviation range of ≈46μV/K can only be explained by the contribution from the inter-tube junctions. Hence, a special attention to the TEP of junctions was paid for discussing the TEP of the prepared thin SWCNT films.

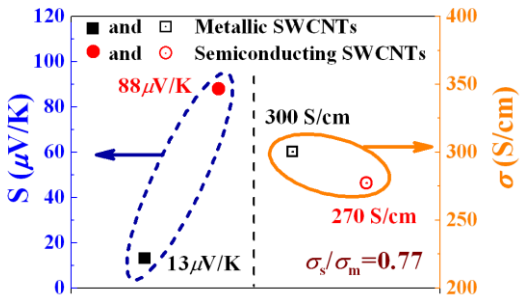

Figure 7-3 The measured TEP and electrical conductivity of the type separated m- and s-SWCNT thin films.

To understand thermoelectric transport through SWCNT thin films we developed a simplified TEP model assuming that a typical mono-dispersed SWCNT thin film is composed of numerous individual or bundled nanotubes with junctions between them which connected in series. Both the tubes and the junctions can contribute to the total TEP. To visualize the real situation of s-SWCNT random network, a numerical simulation was employed. Details of this methodology are explained elsewhere.[27] A representative schematic of randomly generated s-SWCNTs is depicted in Fig. 7-4. (In this simulation, the density of CNTs is $20/\mu m^2$, the length of CNT is 1μm accounting for real CNT dimension, and the film area is defined as 2μm (film width) × 10μm (film length), respectively.) Taking into account the fact that the TEP is independent of geometrical factors, we assume for the sake of simplicity that the chirality (n, m), diameter, and tube length are identical. The TEP generated by an individual s-SWCNT is denoted as S_s, whereas the TEP arising from a junction is described by S_j. According to Kaiser's report,[28] the TEP of hetero-structure material connected in series is weighted by the thermal resistances of each component. Thus, by considering the tubes and junctions separately, the total TEP of the thin film (S_t) can be expressed as:

$$S_t = \frac{1}{R_t}\left(\sum_{i=1} R_s S_s + \sum_{i=1} R_{ji} S_{ji}\right) \qquad (7\text{-}1),$$

$$R_t = \sum_{i=1} R_s + \sum_{i=1} R_{ji} \qquad (7\text{-}2),$$

where R_s and S_s are the thermal resistance and the TEP of s-SWCNT, R_{ji} and S_{ji} are that of i^{th} junctions, and R_t is the total thermal resistance of the conduction path in series as displayed in Fig. 7-4. Furthermore, similar with the Ohms law, the temperature difference (ΔT_d) is proportional to the thermal resistance (R), which can be given by:

$$\dot{Q} = \frac{\Delta T_d}{R} \qquad (7\text{-}3),$$

where $\dot{Q}$ is the thermal current induced by the heat transport. In fact, the heat transport can be contributed by phonons and also by carriers in material. However, in a random network system, the latter one can be dominant due to an extremely small contact area at the inter-tube section and a highly disordered situation. Further, in detail analysis will be presented in later paragraph. Combining Eqs (7-1)~(7-3), S_t can be summarized as:

$$S_t = S_s + \frac{1}{\Delta T}\sum_{i=1}^{n} \Delta T_{ji}\left(S_j - S_s\right) \qquad (7\text{-}4),$$

where ΔT and ΔT_{ji} are the temperature differences of the entire SWCNT network and i^{th} junction, respectively.

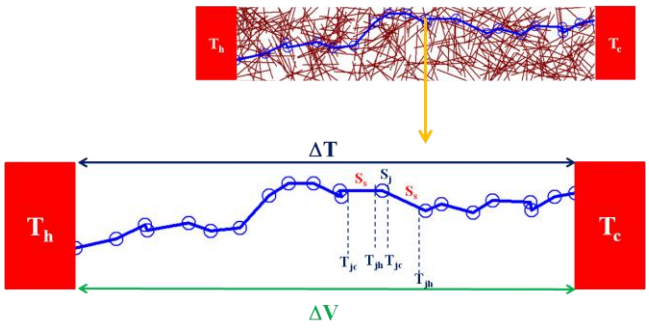

Figure 7-4 A representative random network generated by a numerical simulation (top) and one of dominant paths in s-SWCNT network for TEP calculation (bottom).

Besides, To quantify the junction contribution to the total TEP in detail, we established a specific cell in a SWCNT network which consists of half of two adjacent individual nanotubes with a junction as illustrated in the top of Fig. 7-5. The temperature difference of the cell is ΔT_{sc} and $\eta = \Delta T_j/\Delta T_{sc}$ describes the coefficient related to phonon scattering and electronic tunneling at each junction. By assuming that numerous identical specific cells (N) are connected in series, as in the bottom of Fig. 7-5, the temperature difference of the network can be written as:

$$\Delta T=\eta\Delta T_{sc}N+(1-\eta)\Delta T_{sc}(N+1) \tag{7-5}$$

The first term of Eq. 7-5 represents the sum of temperature drops at each junction and the second term represents the sum of temperature drops along nanotubes in a single path in the network. An additional parameter α was introduced to describe the effect of junctions; it describes a contribution due to the temperature difference arising from all junctions to the total temperature gradient in the network.

$$\alpha = \frac{1}{\Delta T}\sum_{i=1}^{N}\Delta T_{ji} = \frac{\eta\Delta T_{sc}N}{\eta\Delta T_{sc}N+(1-\eta)\Delta T_{sc}(N+1)} = \frac{1}{1+\frac{1-\eta}{\eta}\left(1+\frac{1}{N}\right)} \tag{7-6}$$

After insertion of Eq. (7-6) into Eq. (7-4), the total TEP of the thin films can be expressed as:

$$S_t = S_s + \alpha\left(S_j - S_s\right) \tag{7-7}$$

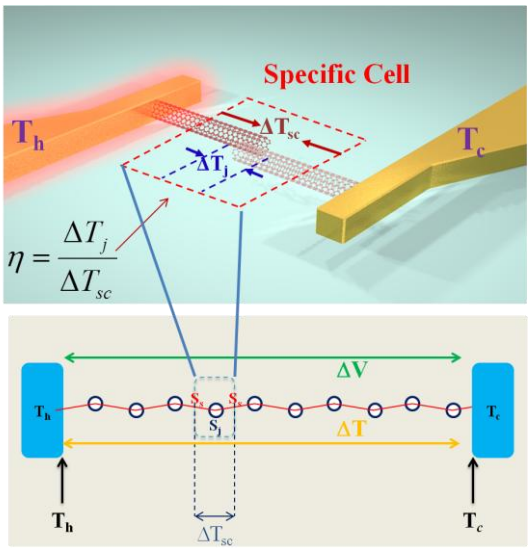

Figure 7-5 Definition of a specific cell (top), and a schematic of the specific cell in one ideal path (bottom), where the whole film composed of such numerous identical cells. Thus, the total TEP is obtained from the contribution of TEP from each cell.

The TEP as an intrinsic property of a material is independent on material dimensions. Therefore, S_t and S_s must be constant in an ideal case when the individual nanotubes and the junctions are identical. Based on Eq. (7-7), the TEP of junctions is a function of η and the number of junctions N in the network. As already mentioned, the TEP of our pure s-SWCNT network achieved value of ≈88μV/K, which is twice as high as the TEP of one individual s-SWCNT (≈42μV/K) at 300K[25] suggesting the contribution of the inter-tube junctions to the measured TEP of the s-SWCNT thin films. We analyzed the dependence of the junction TEP, S_j on the parameter η and the number of junctions N, which are plotted in Fig. 7-6. In our networks the minimum number of junctions estimated through dividing the length of film by the length of individual s-SWCNT is 10^4. It can be clearly seen that the junction TEP does not change with the number of junctions, except for $N < 10$, and only slightly changes for $0.5 < \eta < 0.8$. It is worth to notice that the TEP for one junction was found to be ≈1mV/K; however, this value has no physical meaning in this study since the value of η is likely to be close to 1 (as shown further).

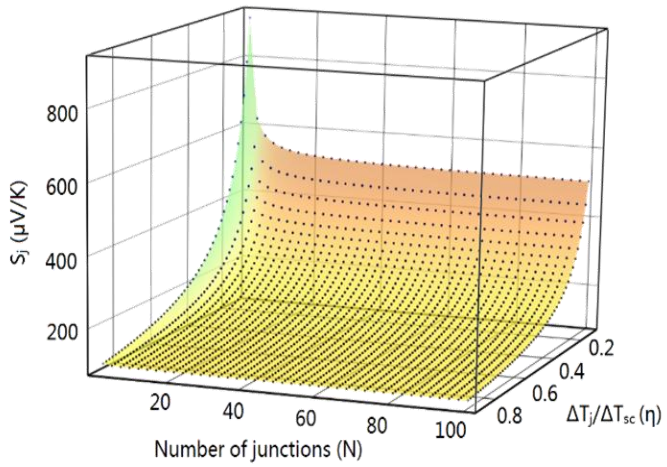

Figure 7-6 The calculated junction TEP as a function of the number of junctions (N) and factor η

The temperature dropping across a single junction associated with phonon scattering and electronic tunneling effect, is determined by the interfacial thermal resistance between nanotubes.[29-31] As reported by Zhong et al,[32] the heat transfer across the interface can be expressed as:

$$\Delta T_j = \frac{Rq}{A} \tag{7-8}$$

where R is the thermal interfacial resistance, A is the area of the interface, and q is the heat flow rate across the interface. Due to the tubular structure of nanotubes, the contact area A is extremely small. The distortion of the nanotube lattice at the contact point results in a dramatically increased phonon scattering. Hence, the heat transport through lattice vibrations along the tube can be severely blocked at the junction. In addition, the high inter-tube barriers localize the majority of carriers at the junction decreasing significantly the electronic heat transport. Both influences increase the thermal interfacial resistance. Based on aforementioned two main effects, we can conclude that the temperature dropping across interface ΔT_j is dominant compared with that of specific cell ΔT_{sc}, the value of η can be close to 1. Taking into account the numerous junctions in the dense SWCNT networks, the junction TEP was estimated to be in the range of 90-120μV/K, while the junction TEP of m-SWCNTs networks was about 13.3-15μV/K.

7.5 TEP Characteristics of Precisely Tuned Ratio of Semiconducting and Metallic SWCNTs

The SWCNT networks can be described as highly conductive quantum wires with tunneling barriers between individual wires.[10] In the mixed type of SWCNTs three types of

junctions composed of m-m, s-s and m-s SWCNTs exist. The junctions of the same electronic type of tubes m-m and s-s are formed through tunneling Ohmic contacts, while the resistance of m-s junctions is expected to be orders of magnitudes higher due to the tunneling Schottky contacts.[33] Therefore, in the network of mixed m- and s-SWCNTs numerous percolation paths are possible for the thermal transport. However, the mobile charge carriers always move via the lowest resistive percolation paths.[27] For this reason, we assume that the conduction in the mixed thin films occurs preferentially through parallel paths of the same electronic type of SWCNTs, and the fraction of percolation paths is similar with the m:s ratio in the mixture. Thus, the TEP in parallel connection mode can be calculated as following equations:

$$S = \frac{1}{\sigma}\sum_{j=1}^{N}\sigma_j S_j \tag{7-9}$$

$$\sigma = \sum_{j=1}^{N}\sigma_j \tag{7-10}$$

where σ_j and S_j are the electrical conductance and TEP of the j^{th} percolated conduction path, and σ is the conductance of the entire thin film. It is known that the electrical conductivity of m- and s-SWCNT networks is dominated by the junction barriers rather than the number of delocalized charge carriers.[10] Furthermore, the transmission probabilities through junctions in s-SWCNTs and m-SWCNTs are comparable, and the electrical conductivity ratio between the s- and m-SWCNT thin films (γ) is commonly determined to be between 0.25 and 1.[33] The electrical conductivity of our SWCNT films was about 270 S/cm for s-SWCNTs and 300 S/cm for m-SWCNTs giving γ equal to 0.77.

Figure 7-7(a) shows the measured TEP of thin SWCNT films containing precisely adjusted fractions of s-SWCNTs in the mixed networks. The results demonstrate that the TEP almost linearly increased concomitantly with the increasing s-SWCNT ratio in the thin film. The solid line represents the calculated TEP by using Eqs (7-9) and (7-10) with the electrical conductivities of mono-dispersed films and their ratio $\gamma = 0.77$. The numerical calculation results show an almost perfect coincidence with the experimental data. For comparison, we calculated the TEP of mixed SWCNT networks taking into account several ratios of electrical conductivities from the range 0.25~1 as suggested for SWCNT networks like bucky papers.[33] The obtained TEP curves as a function of varying fractions of s-SWCNTs are presented in Fig. 7-7(b). Significant deviations from the experimental results are clearly visible. These calculations reveal that the difference of electrical conductivity between m- and s-SWCNT networks plays an important role in the determination of the TEP of mixed SWCNT thin films. Generally, the as-produced SWCNTs consist of a heterogeneous mixture of nanotubes with a ratio of m- and s-SWCNTs being ca.1:2. Therefore, we also calculated the TEP of such commonly fabricated

SWCNT thin films as a function of γ, and plotted the results in Fig. 7-7(c). The calculated values of TEP at the fixed proportion are in the range of 35~62μV/K, which is in a good agreement with our previously measured TEP of a bucky paper (≈40μV/K).[34]

Finally, the TEP values for a series of our artificially mixed SWCNT samples various γ were simulated and plotted in Fig. 7-7(d). The electrical conductivity ratio γ > 0.25 correlates with the previously reported data for SWCNT films.[27, 33] It seems to be that γ = 0.25 is the lowest limit of the conductivity ratio in the real as-prepared heterogeneous SWCNT networks. Using the experimental and simulated data shown in Fig. 7-7(a), the ratio of s- to m-SWCNTs in a mixed network of any SWCNT sample can be estimated from the measured TEP. In fact, such model can be applied to any conducting nanowire networks for theoretical analysis of junction TEP in thermoelectric materials.

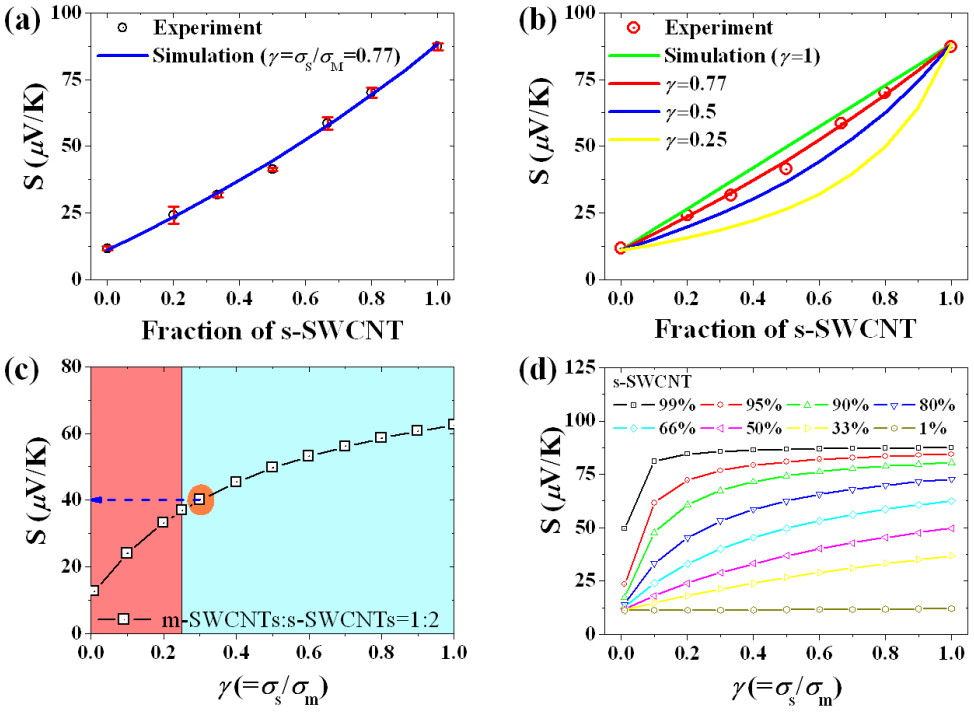

Figure 7-7 (a) The experimental and calculated TEP as a function of the s-SWCNT fraction in the mixed thin films (b) The fitting curves of the TEP in the mixed SWCNT films depending on $\gamma=(\sigma_s/\sigma_m)$ (c) Example of the simulated TEP for a SWCNT film with a m:s ratio equal to 1:2 as a function of γ, (d) and the corresponding fitting curves of TEP versus γ for different fractions of s-SWCNTs in the films.

7.6 Conclusion

The TEP of mono-dispersed m-SWCNT and s-SWCNT thin films was investigated theoretically and experimentally. SWCNT thin films consisting of precisely adjusted ratios of

m- and s-SWCNTs showed a quasi-linear enhancement of TEP with an increasing fraction of s-SWCNTs in the prepared mixtures. The experimental data were supported by theoretical calculations which involved the ratio of pure m- and s-SWCNTs in a network and the ratio of resulting electrical conductivity ($\sigma_s/\sigma_m \approx 0.77$). A theoretical TEP model was developed to demonstrate the junction effect in SWCNT networks and its contribution to the total TEP of SWCNT thin films. The theoretical results show a good agreement with the experimental data, and indicate that the total TEP is dominated by the TEP of the inter-tube junctions. Our proposed model is beneficial for estimation of junction TEP in any type of SWCNT network. The relationship between TEP and the fraction of s-SWCNTs in SWCNT films, determined here, allows a simple estimation of the s:m ratio for any mixed SWCNT film by measuring its TEP.

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8. Conclusion

We have explored various electrical characteristics based on I-V, C-V, low frequency noise (LFN), and low temperature measurement with a numerical simulation for top-down and bottom-up devices, respectively. Particularly, as a possible emerging candidate for more than Moore, heavily doped junctionless transistors (JLTs) fabricated at CAE-LETI on (100) SOI wafers and bottom-up nanoscaled devices such as quasi-1D tin-oxide (SnO_2) nanowire FETs and -2D single-walled carbon nanotube (SWCNT) random network thin film transistors were extensively investigated.

The trend of semiconductor industry with current CMOS (Complementary metal-oxide-semiconductor) scaling issues arisen from short channel effects (SCEs) and advanced MOSFET technologies were briefly described in chapter 1.

In chapter 2, the relevant theoretical backgrounds and various electrical parameter extraction methodologies were introduced with account for the fundamental long channel N-type MOSFET analytical model (SPICE 1 model). Details of the Y-function method (YFM) were also presented as well. Device characterization methods based the split C-V technique were introduced to evaluate oxide capacitance (C_{ox}), doping concentration (N_D for N-type and N_A for P-type) and the position of V_{FB}, respectively. Furthermore, representative LFN theoretical models such as Hooge mobility fluctuation model (HMF), carrier number fluctuation model (CNF), and carrier number fluctuation correlated mobility fluctuation model (CNF-CMF) were discussed.

Chapter 3 demonstrated a numerical percolation simulation methodology based on modified Floyd's algorism taking into account for the random aspects and percolation dominant phenomena in two-dimensional (2D) conducting nanowire random networks. The results were systematically analyzed in terms of several factors such as the resistivity of each conductive segment in each path the number of junctions, and contact resistances. Percolation probability was simulated as well and its dependence to the density of conducting wire (ρ_{CW}) was well-fitted with an error function. Finally, to extend usability and accessibility, a SPICE simulator was employed and demonstrated.

Chapter 4 discussed about the low-temperature characteristics (77K~350K) of flat-band (V_{FB}) and low-field mobility (μ_0) in planar and tri-gate nanowire JLTs. To this end, CV, IV, LFN, cryogenic and dual-gate coupling measurements were carried out. The position of V_{FB} was determined and compared based on various experimental results and theoretical model,

respectively. Moreover, to have an insight into the transport mechanism of JLTs throughout an analysis of the temperature dependence of the low-field mobility, V_{FB} and the charge based analytical model of JLTs were taken into account for the different conduction region and type of JLTs. The role of neutral defects scattering was found the most limiting factor concerning the degradation with small gate length of low-field mobility in both planar and tri-gate nanowire JLTs.

Chapter 5 presented the channel access resistance (R_{sd}) effects on carrier mobility and LFN characteristics in a polymethyl methacrylate (PMMA) passivated quasi-1D SnO_2-NW FET. To this end, the effective gate-to-channel capacitance (C_{gc}) was firstly obtained through 2D Poisson equation numerical simulator accounting for real dimensions and electrostatic coupling effects associated with the presence of the PMMA. In order to directly evaluate the electrical parameters without the influence of R_{sd}, YFM was employed and obtained μ_0 was compared with other mobility values such as the field effect mobility (μ_{fe}) and the effective mobility (μ_{eff}) calculated from transconductance (g_m) and simulated C_{gc} curve respectively. After R_{sd} correction of I-V results, all mobility values were consistent with the intrinsic μ_0 value. Finally, LFN behaviors were clearly attributed to CNF model provided R_{sd} effects were incorporated and the interface surface trap density (N_{NW}) in SnO_2 NW-FETs on Si_3N_4 with PMMA passivation layer was deduced from LFN analysis.

In chapter 6, static and LFN characterizations of random network thin film transistors (RN-TFTs) with different gate lengths were described. To exclude R_{sd} effects, YFM method was firstly applied for the extraction of electrical parameters such as μ_0, V_{th}, and R_{sd}. To get rid of the capacitance effects originated from isolated single-walled carbon nanotube (CNTs) islands and to directly measure C_{gc}, the split C_{gc} measurement technique was employed. Besides, to have a better interpretation of C_{gc} in percolation-dominated 2D RN-TFTs, a homemade 2D finite numerical simulation program by combination with SPICE simulator was demonstrated. LFN measurements also were carried out and the results were well interpreted by CNF-CMF model. A detailed analysis of the surface trap density (N_{st}) and $\alpha \cdot \mu_{eff}$ (α is the Coulomb scattering coefficient) was firstly found based on various capacitance models. Finally, the one-dimensional (1D) cylindrical capacitance C_{1D} based model was suggested and applied. It provided a better consistency between all electrical parameters based on experimental and simulation results.

The TEP of mono-dispersed m-SWCNT (metallic single-walled carbon nanotube) and s-SWCNT (semiconducting single-walled carbon nanotube) thin films was investigated theoretically and experimentally in chapter 7. SWCNT thin films consisting of precisely adjusted rati-

os of m- and s-SWCNTs showed a quasi-linear enhancement of TEP with an increasing fraction of s-SWCNTs in the prepared mixtures. The experimental data were supported by theoretical calculations which involved the ratio of pure m- and s-SWCNTs in a network and the ratio of resulting electrical conductivity. A theoretical TEP model was developed to demonstrate the junction effect in SWCNT networks and its contribution to the total TEP of SWCNT thin films. The theoretical results show a good agreement with the experimental data, and indicate that the total TEP is dominated by the TEP of the inter-tube junctions. Our proposed model is beneficial for estimation of junction TEP in any type of SWCNT network. The relationship between TEP and the fraction of s-SWCNTs in SWCNT films, determined here, allows a simple estimation of the s:m ratio for any mixed SWCNT film by measuring its TEP.

Appendix

A. Real-time impendence and low frequency noise measurement system

Appendix A. A dual analyzer for real-time impedance and noise spectroscopy of nano-scale devices

A simple portable dual analyzer which allows real-time ac-impedance measurements and noise spectroscopic analysis simultaneously was developed by employing one or two DAQ (data acquisition) systems together with a low noise current-to-voltage preamplifier. The input signal composed of numerous selected frequencies of sinusoidal voltages with a DC bias was applied to a device under test (DUT); single-walled carbon nanotube field-effect transistors (SWCNT-FETs). Each frequency component, ranging from 1Hz to 46.4kHz, was successfully mapped to a Nyquist plot using the background of the electrical noise power spectrum. It is clearly demonstrated that this dual analyzer enables the real-time ac-impedance analysis and the frequency response of the carrier transport in the SWCNT-FETs as a DUT.[1]

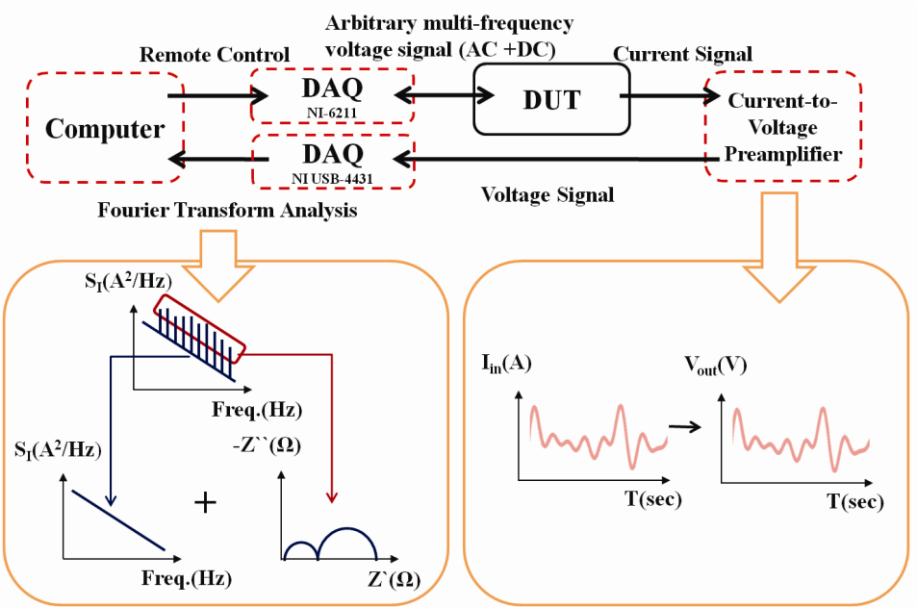

Figure A-1 The simplified schematic of an in-situ Nyquist and electrical noise meter for transient measurements: Two DAQ system can be integrated into one DAQ. The signals of the noise or the impedance can be extracted and optimized by tuning the amplification factors and the measurement range

In this contribution, we introduced a dual analyzer which allows of combined real-time impedance and noise measurements. Fig. A-1 illustrates the layout of the dual analyzer we devised. We used the one or two DAQ systems (NI USB-4431, DAQ-6211), and the low noise current-to-voltage preamplifier (Stanford Research 570). The former is made up of a single-24 bit dc-output-channel and four-24bit dc-input channels with 102.4kS/s sampling rate per channel and the latter is composed of two 16-bit dc-output-channels and thirty two-16 bit dc-input channels with 250kS/s sampling rate per channel. In light of the fact that the digitally generated

electrical signals such as rectangular, saw-tooth or tri-angle waveforms are composed of various sinusoidal waves, the impedance of the sample can possibly be measured in a wide range of frequencies by using the non-sinusoidal waves.[2] To modulate the shapes of the input voltage signal containing the multiple sinusoidal waves, we used a home-built LabVIEW program to control the frequency, the amplitude, the DC offset (0V ~ ±10V), the phase difference and even to extract the electrical noise power spectrum density at each frequency simultaneously. By means of the Fourier transform techniques, the noise spectrum and the Nyquist plot could be successfully separated at a resolution of under 1Hz between 1Hz to 46.4.kHz, enabling the real-time analysis on the kinetics of change carriers in the sample based on an appropriate equivalent circuit model. The frequency resolution and the range are limited by the frequency dependence of the current-to-voltage gain of the preamplifier and the filter function of DAQ. Both could be selected and optimized for the specific samples and the systems.

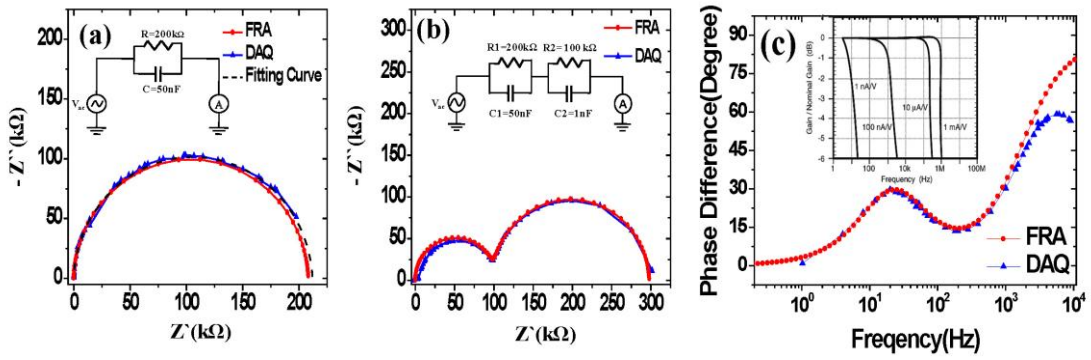

Figure A-2 The Nyquist plots obtained using various methods (FRA(circle), DAQ (triangle)) with (a) a parallel RC circuit and with (b) two different series parallel RC circuits. Inset: The test circuit for one R//C circuit (a) R=200kΩ//C=50nF and two R//C circuits (b) R1=200kΩ//C1=50nF and R2=100kΩ//C2=1nF. (c) The frequency dependence of the phase difference in case of (b) (inset: the frequency dependence of gain of the SR570 preamplifier)

To demonstrate the validity, we applied an arbitrary shaped voltages synthesized with multiple sinusoidal signals consisting of randomly selected frequencies with 1mV ac amplitude to a simple circuit (used as a DUT) in which a resister (200kΩ) and a capacitor (50nF) are connected in parallel (see the inset of Fig. A-2(a)). We also applied a rectangular pulse (200Hz) with 100mV voltage bias. Although the pulse signal has the relatively low power density in the high frequency regions and the possible perturbation problem in the pulse signal, it includes a wide range of frequencies with a large number of data points in a single measurement. In addition, there are not significant differences in the power spectrum between with and without the pulse signal when applying the modulated sinusoidal input signal to a DUT. Fig. A-2(a) shows the Nyquist plots obtained using the dual analyzer as well as that from a conventional FRA(Novocontrol Alpha-AN) measurement. As seen in Fig. A-2(a), both spectra are nearly

identical to each other. We could identify each frequency component of the applied signal based on the phase difference and the magnitude in each cycle. A simultaneous dual measurement took approximately less than 0.8 second, confirming that the response fast enough to characterize the dynamic processes taking place in the order of seconds. The best fit of the Nyquist plot following Eq. (A-1), a mathematical representation of the equivalent circuit model shown in the inset of Fig. A-2(a), gives the values of R=210kΩ, and C=62.5nF which are consistent with those of the resistor and the capacitor used in the DUT.

$$Z = \frac{R}{1 + jwRC} = \frac{R}{1 + (wRC)^2} - j\frac{wR^2C}{1 + (wRC)^2} \qquad \text{(A-1)},$$

where w=2πf, f is a frequency. And the real and imaginary part can be expressed as following,

$$Z' = \frac{R}{1 + (wRC)^2},$$

$$-Z'' = j\frac{wR^2C}{1 + (wRC)^2}.$$

In fact, these values of the resistance and the capacitance are in excellent agreement with those of R=203kΩ and C=66 nF, respectively, determined using the FRA. Such consistency can also be easily confirmed by Fig. A-2(a).

For a further test, we used a DUT consisting of two parallel RC circuits (R1=200kΩ//C1=50nF and R2=100kΩ//C2=1nF) connected in series (see the equivalent circuit model shown in Fig. A-2(b) inset), which may be more relevant to real devices such as fuel cells, and the resulting Nyquist plot is displayed in Fig. A-2(b). The phase difference of each frequency measured from between the DAQ input channels and the FRA is perfectly matched in the frequency range above approximately 10kHz. Considering the total current through DUT in Fig. A-2(b) and the input voltage range of the DAQ NI-USB 4431, the current-to-voltage sensitivity should be selected between 1μA/V and 10μA/V (*i.e.* the frequency range approximately from a few Hz to 10kHz). From this fact, we can conclude the appropriate frequency range could be selected from the flat response region and the limits of the bandwidth could be improved by adopting a proper preamplifier which has a wide range of the flat frequency gain response. The Nyquist plot obtained from the dual analyzer is again found to be completely overlapped with that measured from the other DUT in the frequency range above 1Hz. We attribute the deviation from the DAQ result observed below 1Hz to the low noise current-to-voltage-gain frequency response limitation of the preamplifier we used, which can be further calibrated depending on the relevant frequency range.

We also designed the test circuit for the transient measurement including two parallel RC circuits and the commercial N-type MOSFET (metal-oxide-semiconductor field-effect tran-

sistor) (see Fig. A-3) to control the total resistance of the second circuit by controlling the gate voltage. As the gate voltage increased, the total resistance of the second circuit decreased due to the reduction of the resistance between the source and the drain. Therefore as the gate voltage changed with time, the total impedance of a DUT could be monitored in real-time. The change in the Nyquist plots is due to the change in the total resistance of the second R//C circuit. Depending on the gate bias, the diameter of the first smaller semi-circular arc appeared in the higher frequency region changed with the changes in their total resistance of the second circuit. The fitted values could be collected every one second with our home-made LabVIEW program and the extracted values were in excellent agreement with the transfer curve of the field effect transistor (IRF 630). This result again confirms the application of the real-time monitoring system which can be fast enough to observe the relaxation phenomena using the dual analyzer.

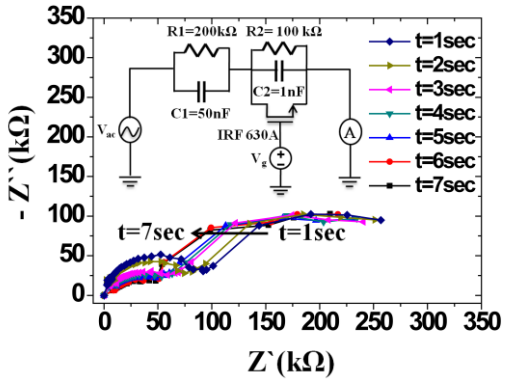

Figure A-3 The transient impedance measurements for the two R//C circuits with a commercial N-type MOS-FET(metal-oxide-semiconductor field-effect transistor), IRF630A, to simulate the change of the total resistance of the second R//C circuit. As the gate voltage varied, the total resistance of the second circuit changed, shifting the second semicircle to the left. Inset: The electrical model for a DUT (R1=200kΩ//C1=50nF and R2=100kΩ//C2=1nF// IRF630A (NMOS))

It is noted however that further optimization is needed to improve a couple of factors for achieving the best performance in a wide frequency range. The distortions in the frequency range below 1Hz and above 10kHz are due to a non-flat frequency response of the current-to-voltage gain of the preamplifier and the input frequency range limitation of our DAQ systems. Both in the low frequency range under 1Hz and the high frequency range over 10kHz frequency regions, the current-to-voltage gain is sharply fluctuated so that the amplitude and the phase are not completely matched. If these undesired factors can be minimized by selecting a proper preamplifier depending on the application, we will be able to be more accurate in a wider frequency range.

Finally, in order to demonstrate the example of the real-time impedance and the noise measurements simultaneously using the dual analyzer, we used SWCNT-FETs as a DUT and recorded the signal. The SWCNT-FETs were fabricated on the silicon substrate with a 300nm

thick silicon oxide layer as a dielectric layer. The single walled carbon nanotubes (SWCNTs) purchased from Hanwha Nanotech (Grade ASP-100F) was dispersed in NMP (1-methyl-2-pyrrolidone) at a concentration of 0.1mg/ml and several droplets of solution were dropped on the surface of the SiO2, and it was rinsed in de-ionized water. And then to make two probe configuration, bi-layer of Ti 20nm and Au 100nm were deposited on the CNT networks.

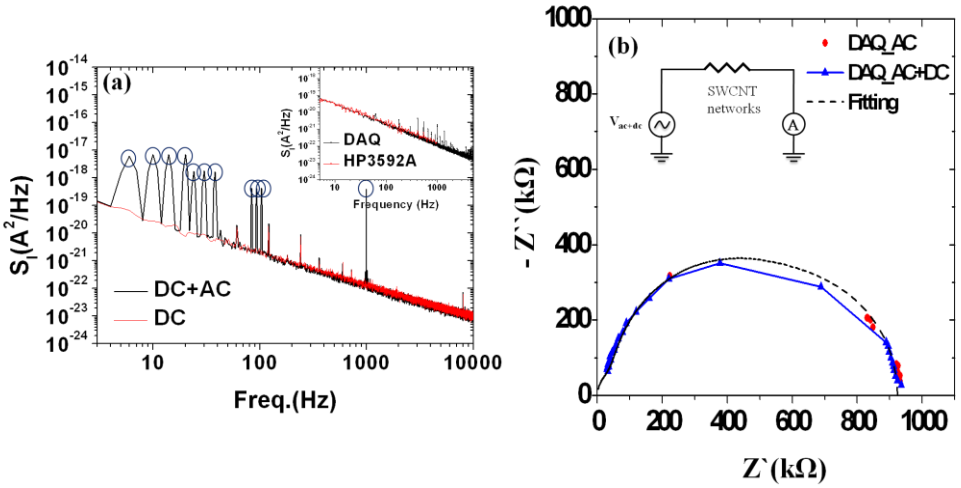

Figure A-4 (a) Comparison of the current power spectra obtained from SWCNT-FET with only DC (2V) bias or both AC and DC (2V). The dark open circles corresponded to the applied AC frequencies for getting the Nyquist plot. The inset shows the noise spectra obtained by each single noise meas-

By applying the AC voltage signals with DC biases we could confirm the validity of the simultaneous measurements of the impedance spectroscopy together with 1/f noise spectrum of the electrical current signal. First of all, to demonstrate the effectiveness of the electrical noise measurement, we compared the results obtained using the conventional noise measurement instrument, the network signal analyzer (HP3562A) with those obtained by using the suggested simultaneous noise measurement technique applying DC (500mV) bias using home-made battery box. As shown in Fig. A-4(a) inset, the two electrical noise spectra are nearly identical, confirming the validity of our dual analyzer. To see the impedance pattern with a noise background more clearly, we used only small numbers of the AC voltage signals which consist of randomly selected frequencies (5Hz, 9Hz, 13Hz, 19Hz, 23Hz, 29Hz, 37Hz, 83Hz, 92Hz, 103Hz, 1,003Hz) at the different DC bias voltage (=2V) in a shielding metal box. Because the power spectrum obtained by applying the mixing frequencies with a DC offset signal to a DUT contains both the impedance and the electrical noise information, we could easily extract each different frequency component using the Fourier transform for a Nyquist plot as indicated by the dark-blue circles and the background of noise power spectrum fitting to the 1/f tendencies. And

Fig. A-4(b) exhibits the impedance spectra obtained based on the background of the FFT. The total resistance (936kΩ) and capacitance (260pF) of the DUT (SWCNT-FETs) between the pads are measured by the HP 4145B and HP 4278A. The total impedance spectrum composed of three R//C parallel parts (1) between the output channel of the DAQ 6211 and the contact pad of the DUT: $R_{sys}//C_{sys} \approx 43.5k\Omega//267.91pF$ (2) between the contact pad and the channel of the DUT: $R_{chan}//C_{chan} \approx 338.2k\Omega//2.714nF$ (3) between the contact pads including parasitic parts: $R_{para}//C_{para} \approx 541.7k\Omega//426.29pF$. The circuit parameter values could be obtained by the best fit using the electrical equivalent circuit model. Based on the results demonstrated above, the dual analyzer we developed is efficient to obtain the information of the noise and the impedance in the device simultaneously. The issues associated with the perturbation in the source signal, the transient effect at the beginning of the perturbation, non-linearity, non-stationary signal and the stability of the response, noise from the measurement equipment itself, noise captured from outside (through ground loops), etc should be taken into account in the practical applications.

In summary, a simple portable dual analyzer allowing transient impedance and electrical noise measurements has been successfully developed. By the proper selection of a preamplifier and a DAQ depending on the system, the fast and the real time impedance spectroscopy with the electrical noise spectroscopy can be optimized

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List of publications

A. Published journals

B. Conference proceedings

C. Conferences

D. Patents

A. Published journals

1. Dae-Young Jeon, So Jeong Park, Mireille Mouis, ***Min-Kyu Joo***, Sylvain Barraud, Gyu-Tae Kim and Gérard Ghibaudo, "Separation of surface accumulation and bulk neutral channel in junctionless transistors", Appl. Phys. Lett. xxx, xxxxxx (2014), http://dx.doi.org/xx.xxxx/x.xxxxxxx (x pages) (**Accepted**)

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C. Conferences

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6. Ho-Kyun Jang, Yong-Hee Choi, Jun-Eon Jin, ***Min-Kyu Joo***, and Gyu Tae Kim, "Dry etching of hafnium-indium-zinc oxide using Cl2/BCl3/Ar gas mixtures", IC AMD 2013 - 8th International Conference on Advanced Materials and Devices – Poster

7. ***Min-Kyu Joo***, Mireille Mouis, Gyu-Tae Kim, Un Jeong Kim and Gérard Ghibau do, "Simulation Methodology for 2D random Network of CNTs Field-Effect Tran sistors", ULIS 2013 - 14th International Conference on ULTIMATE INTEGRATI ON ON SILICON) – Poster

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국문초록 (Korean abstract)

본 논문에서는 차세대 전기 소자로 대두되고 있는 저차원 전계 효과 소자로써, Top-down 공정 방식에 의한 실리콘 Junctionless 트랜지스터와 Bottom-up 공정 방식에 의한 1차원 SnO_2 나노선 및 2차원 탄소나노튜브 랜덤 네트워크 (CNT-RN) 트랜지스터에서의 전기적 특성을 세밀히 분석하였다.

실리콘 Junctionless 트랜지스터에서는 온도 변화에 따른 (77K~350K) 전자 이동도의 특성을 동작 영역별로 구분하여 분석하였다. 투명하고 유연한 미래 전자 소자 구현을 위해 각광받는 1차원 기반의 대표적 물질인 금속 산화물 나노선과 탄소나노튜브의 정밀한 특성 분석을 위해, 1차원 SnO_2 나노선 소자에서 접촉 저항이 전하 이동도 및 저주파 잡음 특성에 미치는 영향을 살펴보았고 2차원 CNT-RN 소자에서 percolation 현상이 유효 정전 용량에 미치는 영향을 분석하기 위해 수치 전산모사 방법이 이용되었다.

Junctionless 트랜지스터는 기존의 일반적인 전자 소자 거동 메커니즘과 달리 완전 공핍 모드, 부분 공핍 모드, 표면 축적 모드로 나뉘며 특히 주된 동작 영역인 체적 전류 부분과 표면 축적 모드의 기준점인 평탄 밴드 전압의 분석 및 정의는 소자 특성 평가에서 매우 중요하다. 따라서 Junctionless 트랜지스터의 성능 평가에 필수적인 문턱 전압, 평탄 밴드 전압, 유효 채널 크기 및 도핑 레벨 등의 수치를 먼저 상온에서의 정전압 특성을 통해 도출한 후 저온에서의 특성 분석을 진행했다. 이 소자에서의 전자 산란 메커니즘을 알아보기 위해, 전하 해석 모델을 기반으로 추출된 채널 길이 100nm 이하의 평면 및 나노선 형태의 Junctionless 트랜지스터에서의 체적 전자 이동도, 저전계 표면 축적 전자 이동도, 문턱 전압, 평탄 밴드 전압의 저온 특성 (77K-350K)을 동작 영역별로 분석하였다. 기존 특성 평가들과는 다르게, 평탄 밴드 전압의 실험적 도출을 위해 소자의 상/하부 기판 커플링 영향이 저온에서 고려되었다. 이를 기반으로 전자의 이동이 포논 산란 영향과 온도 의존성이 없는 중립 결점에 의한 산란에 대해 주로 영향을 받으며 체적 전자 이동도, 저전계 표면 축적 전자 이동도를 결정하게 되는 것으로 보여졌다. 이는 접촉 저항을 줄이기 위해 추가적으로 진행된 S/D 이온 주입 공정에 의해 생성된 결함에 의한 것으로 사료된다.

기존 상용 제품에서 널리 사용되고 있는 실리콘 기반의 소자 제작에 있어서 소형화 공정 기술의 한계를 극복하기 위해 새로운 나노 구조들이 제안되어 왔다. 특

히 1차원 미래 투명/유연 소자로써 SnO_2 나노선을 포함한 산화금속 나노선에 대한 연구 또한 지속되어 왔으나 저차원 소자에서의 전기적 특성 안정화 기술이 기존 실리콘 기반 기술 대비 아직 취약한 것은 사실이다. 이를 극복하기 위해 S/D 이온 주입 및 표면 절연 물질 코팅 공정 등이 시도되고 있지만 이러한 공정 변수들이 1차원 SnO_2 나노선 소자에 미치는 영향에 대한 정밀한 분석이 미흡하였다.

따라서, 고분자 메타크릴산메틸 (PMMA)이 코팅된 1차원 SnO_2 나노선 전계 소자를 제작했고, 소자의 정밀한 전기적 특성 분석에 필수불가결한 1차원 유효 정전용량을 도출하기 위해 수치 전산모사를 수행하였다. 도출된 정전용량의 게이트 반응 특성으로부터 여러 가지 전자 이동도 (저준위 전자 이동도, 유효 전자 이동도, 전계 전자 이동도)의 거동을 반도체 채널-금속간의 접촉 저항을 고려하여 분석하였다. 저차원 나노 구제에서 우세한 영향력을 갖는 접촉 저항은 전자 이동도 거동뿐 아니라 저주파 잡음 특성에도 영향을 주는 것이 확인되었다. 따라서 본 연구에서는 접촉 저항의 영향을 배제하기 위해 YFM (Y-function method) 방법을 이용하였고, 표면 트랩 농도 유추를 위해서는 접촉 저항 영향이 고려된 CNF (carrier number fluctuation) 저주파 잡음 모델을 적용하였다. 이러한 접촉 저항 평가 방법은 저차원 나노 구조 전계 소자에서 널리 적용될 수 있을 것으로 기대된다.

2차원 CNT-RN 전계 소자에서는 정전압 및 저주파 잡음 특성 연구를 진행하였다. 2차원 평면 정전용량 수치 해석 모델과 함께 YFM 방법을 이용하여 정전압 전기 특성을 분석하였는데, 사용된 전자 소자의 불확실한 채널 상태를 고려해볼 때, 고립된 탄소 나노 튜브 및 기생 정전용량의 영향을 배제한 유효 2차원 정전용량 도출의 필요성이 대두되었다. 따라서, 직접 실험을 통해 얻어진 유효한 정전용량 특성을 기반으로 percolation 현상이 2차원 네트워크 전자 소자의 유효 정전용량에 미치는 영향을 밝히기 위한 수치 전산모사를 시행하게 되었다. 수집된 실험 데이터를 근거로, 1차원 정전용량 수치 해석 모델을 2차원 네트워크 소자 분석에 도입하였고 이를 통해 모든 실험 결과에 대해 일관성 있는 결론을 도출했다. 또한 2차원 CNT-RN 소자에서 측정된 저주파 잡음 결과는 기존에 발표된 저주파 잡음 특성 경향과는 다른 CMF (carrier number fluctuation correlated mobility fluctuation) 저주파 잡음 모델로 설명되었고 산화 알루미늄 절연막의 표면 트랩 농도 또한 유추할 수 있었다.

마지막으로 저차원 물질을 이용한 소자의 소형화에 있어서 늘 이슈가 되고 있는 열특성에 대한 분석의 일환으로 정밀하게 분리된 금속성 및 반도체성 2차원 단층 탄소 나노 튜브 박막을 이용한 열전 특성을 분석하며 접촉점에 대한 세밀한 고려가 필요함을 시사하였다. 네트워크 소자를 제작함에 있어서 반도체성 탄소 나노 튜브의 비율이 금속성에 대해 증가함에 따라 Seebeck 계수가 준선형적으로 증가하는

것이 보여졌으며 이에 대한 물리적 분석 방법으로 탄소 나노 튜브간의 접촉점에 대한 고려가 제안되었다. 분석 결과에 따라, 탄소 나노 튜브간의 접촉점이 Seebeck 계수 결정에 주요한 역할을 하는 것으로 밝혀졌으며, 이러한 분석 방법은 다른 1차원 나노 물질로 구성된 percolation 채널 및 전도성 이종 복합체에도 널리 적용될 수 있을 것으로 사료된다.

주요어: Junctionless 트랜지스터, 탄소 나노 튜브, 전자 산란 메커니즘, 저주파 잡음, 수치 전산 모사, 저온 특성, Percolation 효과, 열전 특성, 전기적 소자 성능 추출

Résumé en Français

1. Introduction

After the first demonstrations of "Bipolar-Junction-Transistor (BJT)" in 1947 and "Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)" in 1960s, a silicon based transistor is dramatically developed as a fundamental building block of integrated circuits (ICs) up to a few tens of nanometer scale device.[1-3] Besides, the market demands for high memory density and versatile functionality of ICs are also rapidly increased after the realization of personal computer, smart applications such as iOS and Android based smart phone, a high resolution digital camera, and Nintendo Wii *etc*. To satisfy these needs, the semiconductor technology has been focused on scaling down its size to follow "*Moore's law*" reported in 1975, which predicted that the number of transistors on a chip would double about every two years. This scaling down trend has been successfully continued up to 22nm technology as seen in Fig 1.[1]

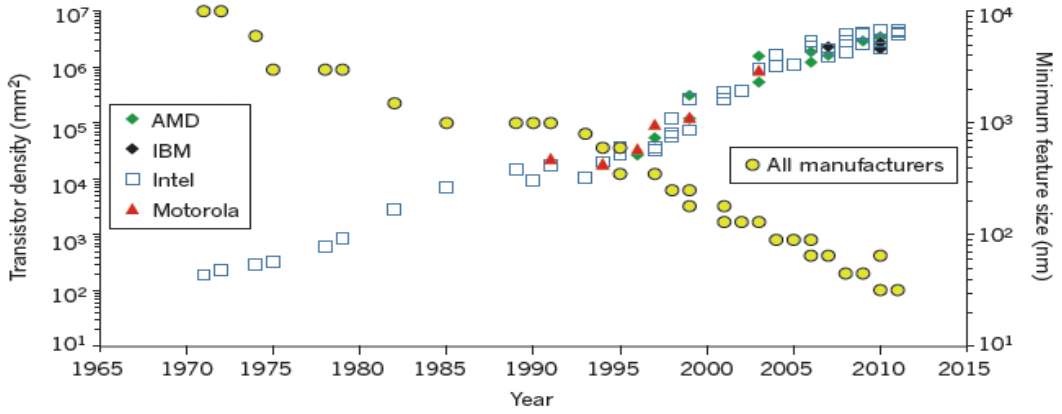


Figure 1 Trend of the gate length miniaturization and the density of transistors in microprocessors over time [1]

However, this scaling trend is almost reached to its physical limitation and is being faced with inevitable problems so called 'short channel effects' (SCEs) that mainly arisen from the weakened gate controllability onto the channel.[4] Furthermore, the fabrication optimization in such extremely small geometrical volume is much challenging since the tiny statistical deviation arisen from the device process will lead to the serious performance variability even though it associates with few atoms in the channel.[5, 6]

In order to overcome such SCEs and sustain keeping such a scaling trend, many new concept devices and optimized fabrication technologies have been suggested as seen in Fig. 2 such as silicon on insulator (SOI), multi-gate structure, tunneling FET *etc*.[4, 7, 8]

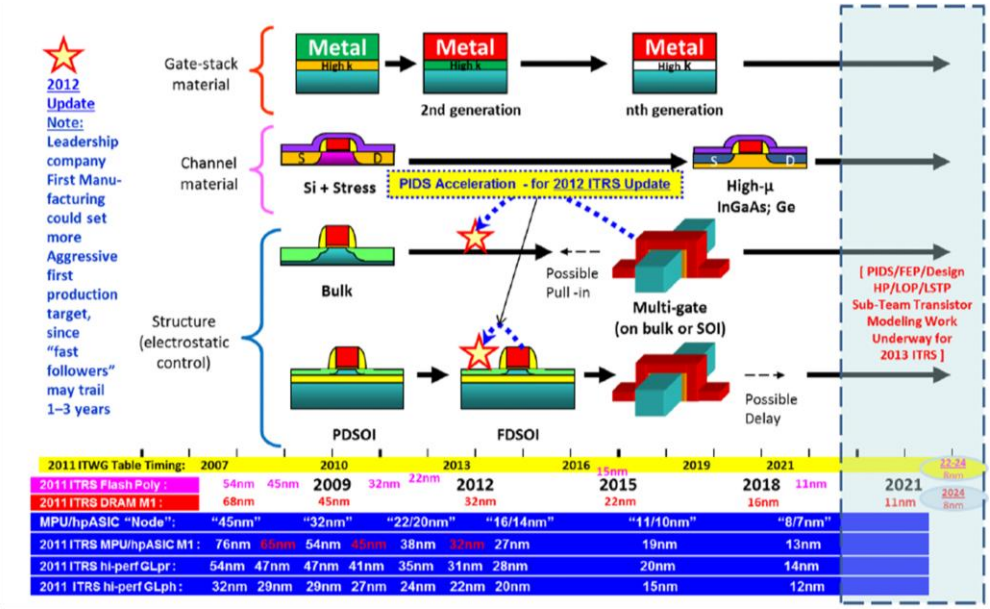


Figure 2 2012 ITRS "Equivalent Scaling" process technologies timing Overall Roadmap Technology Characteristics (ORTC) microprocessor unit (MPU)/High-performance ASIC half pitch and gated length trends and timing, and industry "Nodes". [http://www.itrs.net/]

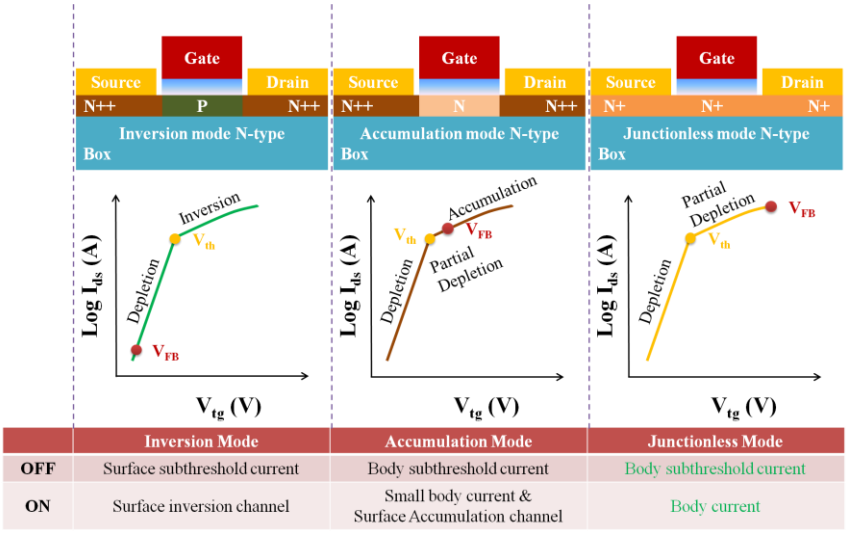
In addition, as a "*Beyond CMOS*" approach, carbon based materials (graphene and carbon nanotubes (CNTs)), semiconducting nanowires, and topological insulators have been widely studied and steadily invested as a possible alternative active channel material, even though there are many obstacles to be manufactured for industrial markets.[9, 10]

In this dissertation, various electrical characteristics based on I-V, C-V, low frequency noise (LFN), and low temperature environment including numerical simulation for top-down and bottom-up devices are respectively investigated. As a possible emerging candidate for "*Beyond CMOS*" and "*more than Moore*" approaches, heavily doped junctionless transistors (JLTs), quasi-1D tin-oxide (SnO_2) nanowire FETs and -2D single-walled carbon nanotube (SWCNT) random network thin film transistors were investigated. These are not only focusing on the reduction of SCEs but also the replacement of silicon based rigid channel material which could be compatible with other substrates than silicon (flexible substrates) or which could be integrated for low cost addition of new functions in the back-end of line of CMOS.

2. Flat-band voltage and low-field mobility analysis of JLTs under low-temperature

Junctionless transistors (JLTs) recently gained much interest as a promising candidate device due to its figure of merits over improved short-channel operation such as reduced threshold voltage (V_{th}) roll-off and drain induced barrier lowering (DIBL).[11, 12] In addition,

in contrast with the inversion-mode (IM) transistors, an ultra sharp p-n junction between silicon channel and source (S)/drain (D) is no more required due to the constant doping concentration from S to D. As a result, the cost of device fabrication and the complexity of process can be much reduced. However, to successfully realize this junctionless gated resistor, a high doping concentration (N_D) with a good doping uniformity over silicon channel and S/D region has to be achieved to get a desired current level for practical applications. Besides, a narrow and shallow silicon film thickness (t_{si}) should be satisfied to turn this device fully off.



	Inversion Mode	Accumulation Mode	Junctionless Mode
OFF	Surface subthreshold current	Body subthreshold current	Body subthreshold current
ON	Surface inversion channel	Small body current & Surface Accumulation channel	Body current

Figure 3 Comparison of conduction mode of advance MOS transistors (Left: Inversion mode, Middle: Accumulation mode, Right: Junctionless mode)

Focusing on the temperature characteristics of JLTs, although many low- and high-temperature specific properties of JLTs were already studied, the temperature (T) and dual gate (top (V_{tg}) and bottom (V_{bg})) coupling dependence of low-field mobility (μ_0), V_{th} and the flat band voltage (V_{FB}) were not yet fully investigated. Especially, it should be noted that the extraction of μ_0 in heavily doped JLTs in accumulation region by employing the Y-Function method (YFM) might be difficult since the volumetric conduction regime has to be relatively reinforced as the target doping concentration is increased, resulting in insufficient fitting range to determine the second linear slope of YFM. Moreover, the field-effect mobility (μ_{fe}) obtained from the maximum value of the transconductance (g_m) was also risky if one wants to use the oxide capacitance per unit area (C_{ox}) when the position of V_{tg} corresponding to the maximum value of $g_m(V_{tg})$ was located in below V_{FB}.

In this study, to decide various fundamental device parameters such as V_{FB}, N_D, a capacitance equivalent thickness (CET) and C_{ox}, the split capacitance-to-voltage (CV) measurement was carried out and the results were deeply investigated. After, to obtain the whole range of T dependence on V_{th} and V_{FB} position of short channel planar and tri-gated nanowire shape

JLTs (less than L_m=100nm), a dual gate mode measurement at low temperature was performed. In addition, to get insight of carrier scattering mechanism, bulk (μ_B) and low-field mobility in accumulation region (μ_{0_acc}) were then separately determined by taking into account for the charge based analytical JLT model. Finally, the temperature dependence of μ_B and μ_{0_acc} were quantitatively analyzed based on modified empirical Matthiessen's rule.

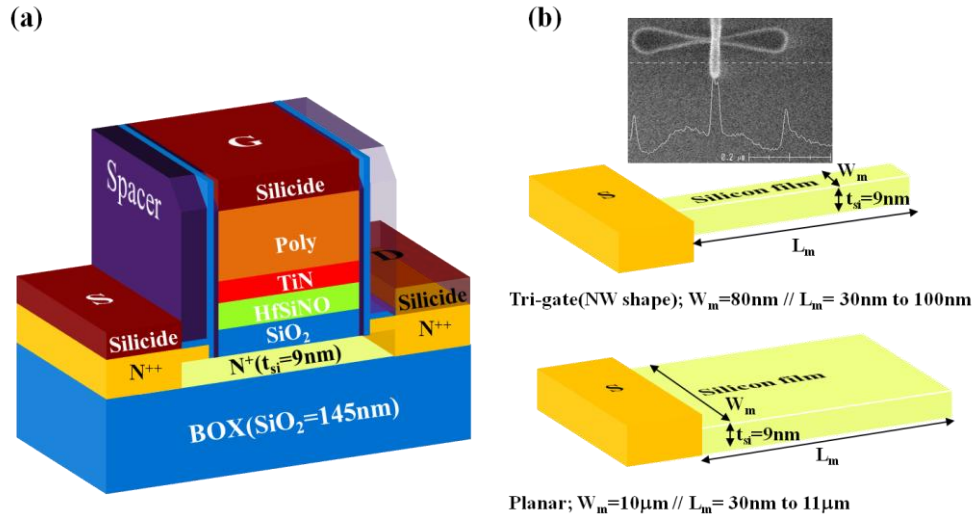


Figure 4 (a) Simplified three-dimensional device structure and (b) on-mask splits (L_m and W_m) for planar and nanowire(NW) shape of JLTs with a representative SEM (Scanning Electron Microscope) image of NW JLT

For this study, various channel geometries of N-type JLTs were fabricated at CEA-LETI on (100) SOI wafers on 145nm thick buried oxide (BOX) with high-κ/metal gate stack as presented in Figs 4 (a) and (b). After thinning of silicon body, t_{si} was measured about 9nm and the targeted N_D was $4\sim5\times10^{19}$ cm^{-3}. Additional doping implantation was carried out between silicon channel and S/D to construct S/D extension region for the enhancement of the contact property by reducing a channel access resistance.[13]

To evaluate the mask reduction length (ΔL_m), capacitance equivalent thickness (CET), and C_{ox}, the gate-to-channel capacitance (C_{gc}) were obtained by the split CV measurement after correction of the parasitic capacitance as displayed in Fig. 5(a). Two humps can be seen in here, indicating the distinct formation of bulk and surface conduction channel, respectively. In addition, by using the linear extrapolation methodology, $\Delta L_m\approx8$nm for short channel JLTs, $\Delta L_m\approx42$nm for long channel, and $\Delta W_m\approx70.4$nm were respectively determined. Besides, CET (≈1.69nm) and C_{ox} ($\approx2.05\mu F/cm^2$) were also estimated.

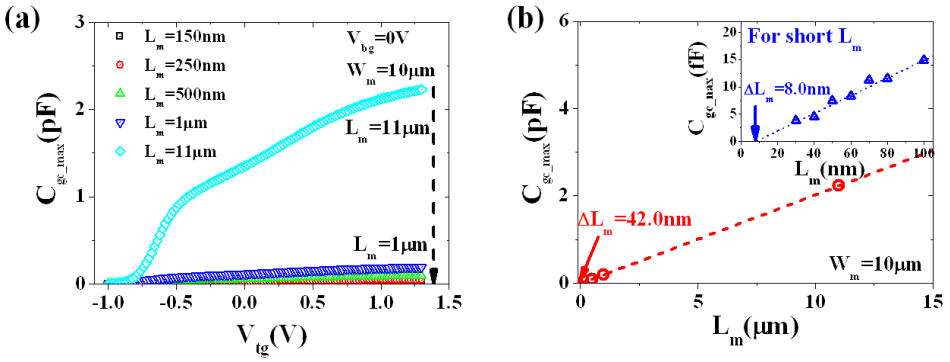


Figure 5 (a) Representative $C_{gc\_max}(V_{tg})$ curves for N-type JLTs (L_m=150nm to 11μm with fixed W_m=10μm). (b) C_{gc_max} versus and L_m for extraction of ΔL_m (≈42nm). (Inset: Same data procedures in short channel JLTs (L_m≤100nm) for ΔL_m (≈8nm) evaluation).

The position of V_{FB} is very meaningful in the operation principle of JLTs. Accordingly, below theoretical equation was firstly considered as an reference value,

$$V_{FB} = \Phi_{MS} = \Phi_M - \left[\chi + \frac{E_g}{2} - \frac{k_B T}{q} \ln \frac{N_D}{n_i} \right] \approx 0.58\,(V) \qquad (1),$$

where Φ_M, χ, E_g, k_B, T, q, and n_i denote the work function of gate metal, the electron affinity, the Boltzmann constant, the absolute temperature, the electron unit-charge, and the intrinsic carrier concentration, respectively.[14, 15] Referring to $C_{gc\_eff}(V_{tg})^{-1}$ and $C_{gc\_eff}(V_{tg})^{-2}$ analytical expressions, more realistic C_{ox} and V_{FB} were respectively determined.[16, 17] The extracted V_{FB} is quite consistent with theoretical value obtained from Eq. (1) and all curves are merged together after using actualized V_{FB} values regardless of V_{bg} as shown in Figs 6(a) and (b). From the linear slope of $C_{gc\_eff}(V_{tg})^{-2}$, the effective N_D can be obtained as well.

Alternatively, the derivative of C_{gc_eff} (dC_{gc_eff}/dV_{tg}) technique for V_{FB} determination and Maserjian's function and the sheet carrier density ($n_s=\int[C_{gc\_eff}(V_{tg})/q]dV_{tg}$) at V_{FB} for the effective N_D estimation were respectively considered as presented in Figs 6(c) and (d). Finally, all parameters were summarized in Table 1. (Underlined values will be used for further electrical parameter evaluation)

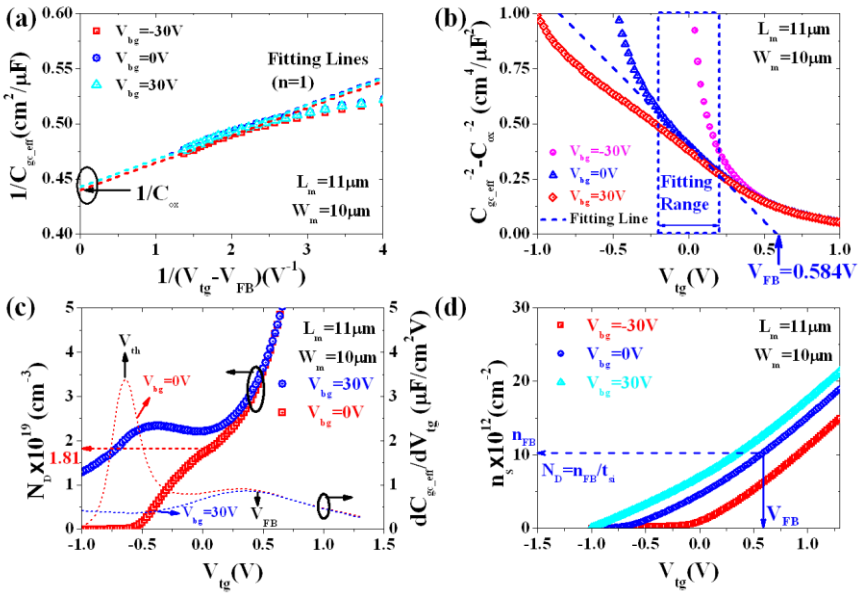


Figure 6 (a) $1/C_{gc\_eff}$ curves (L_m=11μm with W_m=10μm) with respect to V_{bg} (-30V to 30V) for C_{ox} determination (b) $C_{gc\_eff}^{-2}$-C_{ox}^{-2} behaviors for V_{FB} extraction in partially depleted region (c) N_D estimation based on Maserjian's function (left axis) and dC_{gc_eff}/dV_{tg} (right axis) curves (d) n_s versus V_{tg} curves for N_D evaluation at V_{FB}

Method/Parameters	C_{ox} [μF/cm²]	CET [nm]	V_{FB} [V]	N_D [cm⁻³]
Split CV	2.05	1.69	×	×
$1/C_{gc\_eff}$	2.26	1.53	×	×
$1/C_{gc\_eff}^2$ and (Maserjian's Function)	×	×	0.584	1.81×10^{19}
dC_{gc_eff}/dV_{tg}	×	×	0.32	×
$n_s/t_{si}\approx[\int C_{gc\_eff}/qdV_{tg}]/t_{si}$	×	×	×	1.06×10^{19}

Table 1 Summarized table of evaluated parameters; C_{ox}, CET, V_{FB}, and N_D depending on different method.

Figures 7(a) and (b) show the temperature dependence of drain current (I_{ds}) as a function of V_{tg} for short channel (L_m≤100nm) JLTs at V_{ds}=50mV under low-temperature varied from 77K to 350K. Due to the negative temperature dependence of V_{th} and carrier mobility, ZTC (zero temperature coefficients) can be seen in all devices. In addition, to get the temperature dependence of V_{th} and V_{FB}, the derivative of g_m methodology was firstly used as shown in Figs 7(c) and (d), since it provides more relevant value compared to other methods.[15] In the case of L_m=30nm, the only single peak can be observed regardless of T while the second peak of dg_m/dV_{tg} can be clearly confirmed in the case of L_m=100nm, indicating the position of V_{FB_dgm}

(≈0.5V at 77K) at very low-temperature condition. But, this can be applied only for the limited condition (L_m≥70nm with T≤150K) due to the degradation of g_m before V_{FB} and the relative large the series resistance (R_{sd}) effects in such extremely small dimension. Hence, an improved technique has to be requested to systematically evaluate the position of V_{th_dgm} and V_{FB_dgm} for wide scope of T.

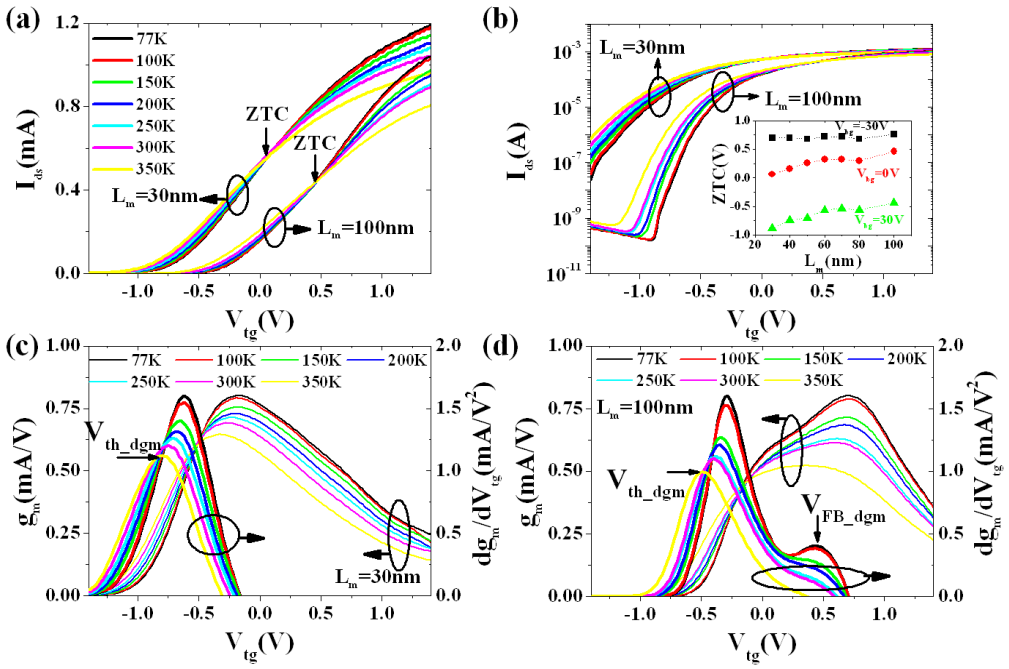


Figure 7 The representative (a) linear and (b) log scaled transfer curves in L_m=30nm and 100nm JLTs with varying T (77K to 350K). (Inset: ZTC versus L_m depending on V_{bg}) The temperature dependence of g_m (left axis) and dg_m/dV_{tg} (right axis) of (c) L_m=30nm and (d) L_m=100nm JLTs, respectively.

To this end, a dual gate coupling mode measurement at low temperature environment was employed and the results are presented in Fig. 8. Compared to Fig. 7(d), the enhancement of the second peak is clearly observed down to 30nm JLTs when positive V_{bg} bias is applied as plotted in Figs 8(b) to (d). Finally, V_{th_dgm} and V_{FB_dgm} depending on T and L_m can be safely determined as seen in Figs 8(c) and (d).

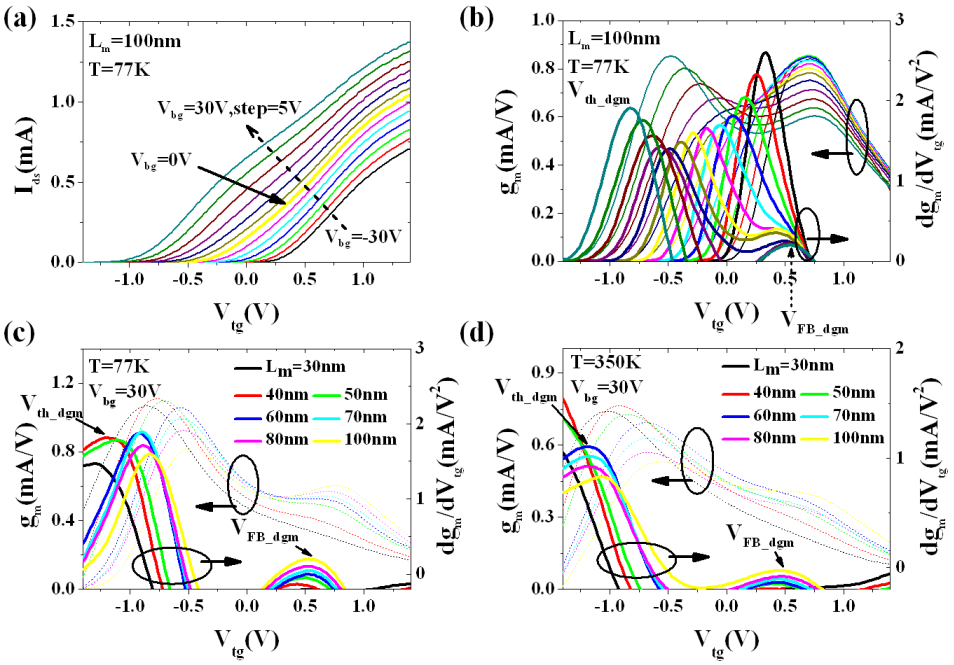


Figure 8 (a) Various transfer curves of L_m=100nm JLT at T=77K depending on different V_{bg} (b) g_m (left axis) and dg_m/dV_{tg} (right axis) curves. Same graphs at V_{bg}=30V with (c) T=77K and (d) T=350K with respect to L_m, respectively.

With account for the analytical expression of V_{th} of JLTs, the temperature dependence of V_{th} and V_{FB} was also estimated as well, [14, 15, 18, 19]

$$V_{th} = V_{FB} - \frac{q \cdot N_D \cdot t_{si}}{2}\left(\frac{t_{si}}{4\varepsilon_{si}} + \frac{1}{C_{ox}}\right) \quad (2),$$

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial V_{FB}}{\partial T} = -\frac{1}{2}\frac{\partial E_g(T)}{\partial T} + \frac{k_B}{q}\ln\left(\frac{N_D}{n_i(T)}\right) - \frac{k_B T}{q}\frac{1}{n_i(T)}\frac{\partial n_i(T)}{\partial T} \quad (3).$$

The temperature dependence of V_{th} and V_{FB} should be equal to each other since the second term of Eq. (2) is only related with temperature independent components. Consequently, Eq. (3) predicts $\partial V_{th}/\partial T \approx -0.36mV/K$ and it is more or less in the similar range compared to that obtained experimentally ($\partial V_{th}/\partial T \approx -0.5mV/K$ and $\partial V_{FB}/\partial T \approx -0.6mV/K$) with account for the possible influence of R_{sd} and the strong transverse field in such short channel JLTs as presented in Fig. 9(a). Moreover, this tendency is quite consistently observed in all JLTs depending on V_{bg}. The representative data set of L_m=100nm is displayed in Fig. 9(b). Additionally, the temperature dependence of subthreshold swing (SS) and that of V_{bg} reliance are also presented as well in Figs 9(c) and (d).

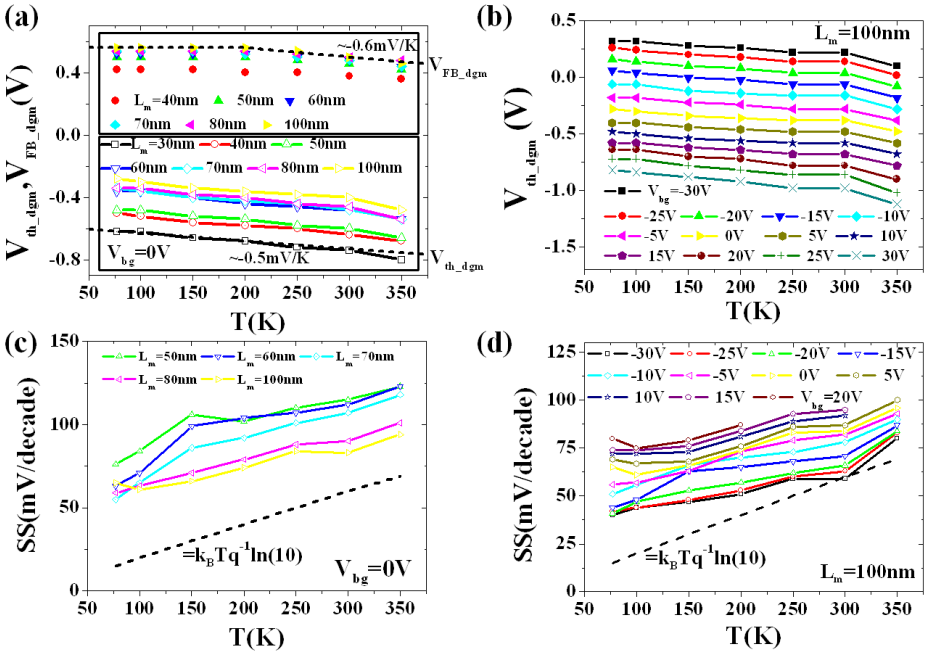


Figure 9 (a) The temperature dependence of V_{th_dgm} and V_{FB_dgm} versus L_m and (b) that of V_{bg} dependence in L_m=100nm JLT. (c) The temperature behavior of SS at V_{bg}=0V with respect to L_m and (d) that of V_{bg} reliance in L_m=100nm JLT.

After the determination of V_{FB} versus T, μ_B(T) and μ_{0_acc}(T) can be separately defined by taking into account for the charge based analytical model of JLT, YFM, and transfer length method (TLM).[11, 20, 21] Before further bulk mobility analysis in detail, TLM method was firstly used to exclude R_{sd} effect in bulk conduction regime (see Fig. 10(a)). The extracted R_{sd} at V_{FB} (R_{sd_FB}) is increased with T as shown in inset of Fig. 10(a), meaning the metallic like behavior of resistivity in S/D extension region.

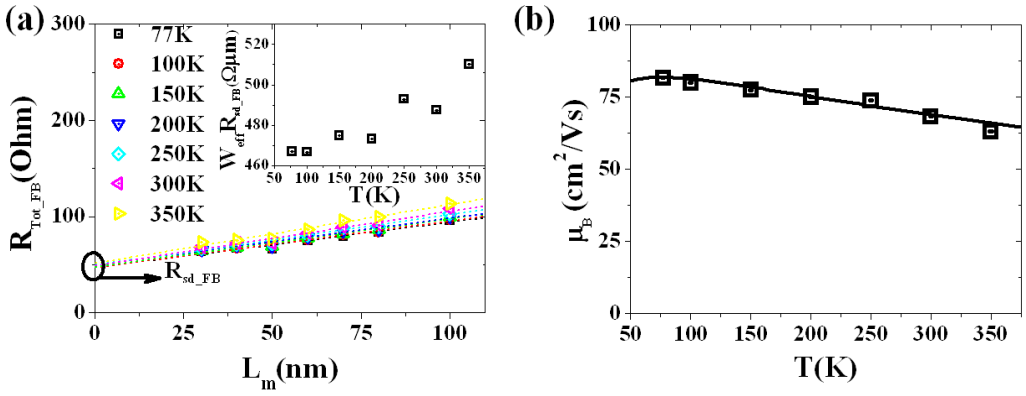


Figure 10 (a) The temperature dependence of R_{tot_FB} with respect to L_m. Fitting curves (dotted lines) are plotted together with data (symbols). (Inset: The temperature dependence of W_{eff} normalized R_{sd_FB}) (b) The temperature dependence of μ_B and corresponding fitting curve with account for various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ)

Besides, Figure 10(b) represents the temperature dependence of μ_B extracted from the each slope of TLM. In order to study the scattering mechanism of μ_B, it was fitted with empirical mobility model given by,[22, 23]

$$\mu_B^{-1} = \left(\frac{300}{T^{\gamma}}\mu_{ph}\right)^{-1} + (T\mu_C)^{-1} + (\mu_{neu})^{-1} \quad (4),$$

where μ_{ph}, μ_C and μ_{neu} denote the scattering parameters derived from phonon, Coulomb and temperature independent neutral defects scattering, respectively. It clearly implies that phonon (γ=1) and the presence of temperature independent neutral defects scattering in silicon and/or interface between S and D region can dominantly impact the degradation of μ_B of short channel JLTs in the whole temperature range. Meanwhile, a significant influence of Coulomb scattering on μ_B is not observed in this analysis even at low temperature condition.

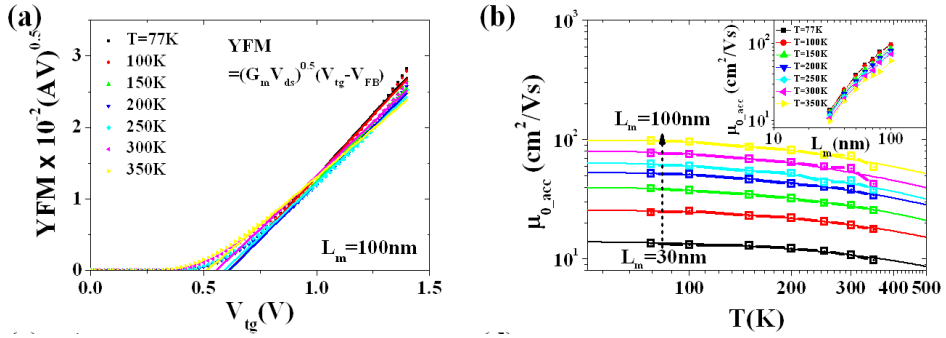


Figure 11 (a) T dependence of YFM in accumulation regime in the case of L_m=100nm JLT. (b) μ_{0_acc} as a function of T depending on L_m (Inset: μ_{0_acc} versus L_m with varying T)

Once, we have the μ_B and corresponding bulk current (I_{ds_bulk}) at V_{FB}, we can easily evaluate the accumulation current (I_{ds_acc}) from the measured total current (I_{ds}).[20] To exclude R_{sd} effect, YFM ($= I_{ds\_acc}/\sqrt{g_{m\_acc}} \approx \sqrt{G_m V_{ds}}(V_{gs} - V_{FB})$ $for\, V_{FB} \le V_{tg}$, where G_m ($=\mu_{0\_acc} C_{ox\_eff} W_{eff}/L_{eff}$) is the transconductance parameter) was employed in here, which clearly shows a good linearity as seen in Fig. 11(a).[21] This is a good indication since there were two slopes in YFM of heavily doped JLTs previously, leading to difficulty to set the second slope of YFM.[15, 23] Thanks to the usefulness of YFM, T dependence of μ_{0_acc} with respect to L_m can be easily obtained. As plotted in Fig. 11(b) and that of inset, T and L_m dependence of μ_{0_acc} are respectively confirmed. Likewise in the case μ_B analysis, the role of phonon ($\gamma \approx 1.1 \sim 1.3$) and neutral defects scattering in silicon and/or interface between S/D region are significantly limiting μ_{0_acc} compared to the other scattering mechanisms. In fact, one can expect that Coulomb scattering might be reinforced due to such high channel doping concentration (Target N_D; $4 \sim 5 \times 10^{19}$ cm^{-3}). However, this mobility limitation effect is not evidently observed in this case. Instead, the temperature independent neutral defects scattering, induced by an additional doping

implantation nearby S/D region with the aim of reducing channel access resistance, is significantly degrading μ_{0_acc} and μ_B even at room temperature. This explanation can be supported by previously reported studies for lower doping concentration of JLTs (Target N_D=1 and 2×10^{19} cm^{-3}) and bulk silicon channel of short channel devices.[22, 23] Hence, based on these facts, it is possible to conclude that the neutral defects scattering is the most limiting factor in such heavily doped JLTs.

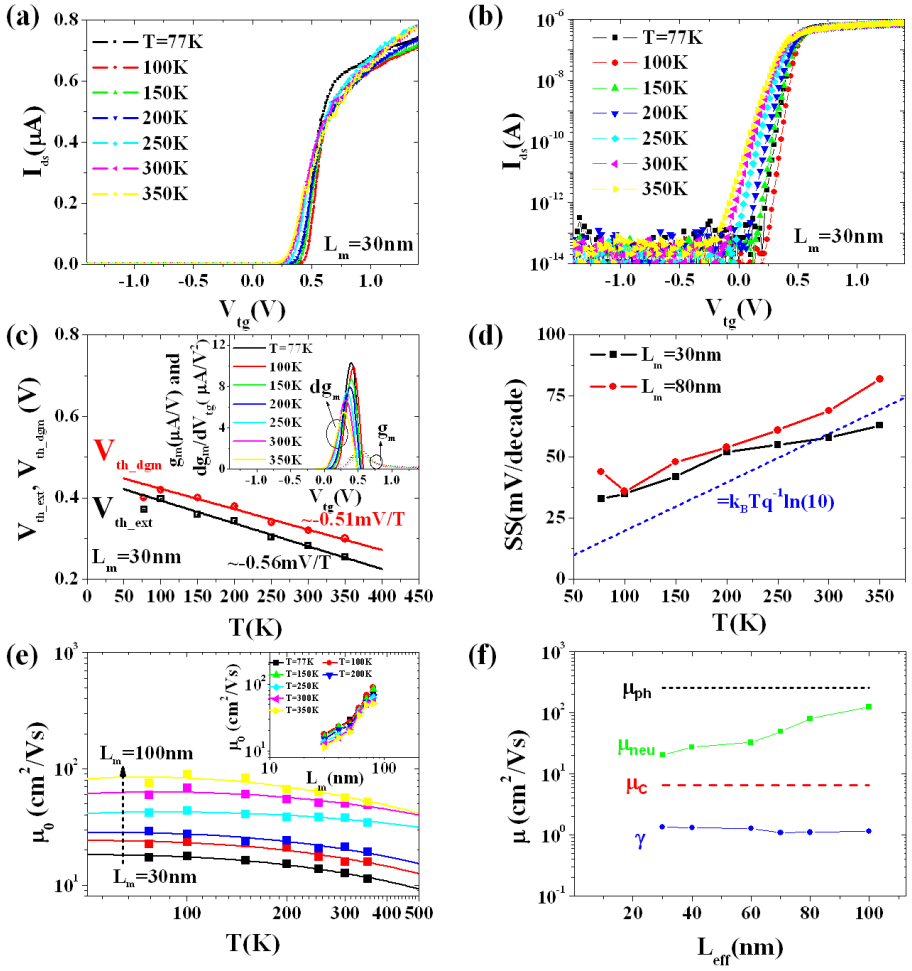


Figure 12 The representative (a) linear and (b) log scaled transfer curves as a function of V_{tg} in L_m=30nm tri-gate NW shape JLTs with varying T (77K to 350K). (c) The temperature dependence of V_{th_dgm} and V_{th_ext}. (Inset: g_m and dg_m/dV_{tg} curves) (d) The temperature behavior of SS (e) μ_0 extracted from YFM as a function of T depending on L_m (Inset: μ_0 versus L_m with varying T) (f) Various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ) for μ_0 depending on L_m.

The temperature dependence of various electrical properties based on tri-gate nanowire shape JLTs (L_m≤100nm with W_m=80nm (W_{eff}≈9.6nm)) was also investigated as well. Figures 12(a) and (b) show the representative linear and log-scaled $I_{ds}(V_{tg})$ curves of the shortest channel of JLTs (L_m=30nm (L_{eff}≈22nm)) at V_{ds}=50mV. The temperature independent ZTC point was observed again in all short channel devices (L_m≤100nm), meaning the negative T dependence

on V_{th} and the carrier mobility in such JLTs. Besides, it shows a better gate controllability compared to planar type JLTs, mainly owing to the enhanced side wall gate effect.[24]

To have T dependence of V_{th} and V_{FB}, the derivative of g_m graphs (dg_m/dV_{tg}) was plotted in inset of Fig. 12(c). Only one peak of dg_m/dV_{tg} was observed in this experiment regardless of T, L_m and V_{bg}. It might be due to the fact that the role of side-wall can be relatively stronger than that of top surface compared to wide JLTs.[24] Consequently, less V_{tg} should be needed to repel depletion regime in tri-gate nanowire JLTs than planar type JLTs, resulting in merging V_{th} and V_{FB} together. Accordingly, V_{th} and V_{FB} cannot be obtained separately due to the enhanced narrow width effect and the relative large R_{sd} effect in such extremely scaled devices.

L_m(nm)		30	40	50	60	70	80	100
μ_B (cm^2/Vs)	μ_{ph}	260	260	260	260	260	260	260
	μ_C	13.3	13.3	13.3	13.3	13.3	13.3	13.3
	μ_{neu}	97.8	97.8	97.8	97.8	97.8	97.8	97.8
	γ	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Planar μ_{0_acc}	μ_{ph}	260	260	260	260	260	260	260
	μ_C	13.3	13.3	13.3	13.3	13.3	13.3	13.3
	μ_{neu}	14.6	27.9	44.9	62.0	76.6	99.9	128.2
	γ	1.3	1.3	1.2	1.2	1.2	1.1	1.1
Tri-gate NW μ_{0_acc}	μ_{ph}	260	260	-	260	260	260	260
	μ_C	6.7	6.7	-	6.7	6.7	6.7	6.7
	μ_{neu}	20.3	27.4	-	32.7	49.5	80.7	123.8
	γ	1.4	1.3	-	1.3	1.1	1.1	1.1

Table 2. Table for various mobility fitting components (μ_{ph}, μ_C, μ_{neu}, and γ) for μ_B, μ_{0_acc}, and μ_0 depending on L_m, respectively

In addition, the representative temperature behaviors of SS of L_m=30nm and 80nm tri-gate JLTs were also determined based on $I_{ds}(V_{tg})$ curves as presented in Fig. 12(d). The slope ($=\partial SS/\partial T$) is almost similar to theoretical maximum slope ($=k_B\ln(10)/q$) regardless of L_m. This fact indicates that its improved electrical properties stemmed from tri-gate structure in terms of SS. However, as displayed in Figs 12(e) and (f), the T dependence of μ_0 extracted from YFM shows much poorer performance compared to that of IM transistors in Ref.[23] and the huge mobility degradation can be seen in inset of Fig. 12(e) as well. It can be attributed to the role of neutral defects scattering in silicon and/or interface between S and D like for μ_B and μ_{0_acc} analysis. Especially, owing to the relatively large portion of S/D extension region in such small volume JLTs, the impact of μ_{neu} on μ_0 can be reinforced, resulting in much inferior mobility property to IM transistors. Finally, all mobility fitting parameters that we used are summarized in Table 2.

In this study, low-temperature characteristics of flat-band voltage and low-field mobility in planar and tri-gate nanowire JLTs were investigated based on CV, IV, cryogenic and dual-

gate coupling measurements. The position of V_{FB} was determined and compared based on various experimental results and theoretical model, respectively, including the temperature dependence of V_{th}. To present the temperature behavior of low-field mobility, V_{FB} and the charge based analytical model of JLTs were considered with respect to different conduction region and type of JLTs. Finally, the role of neutral defects scattering was found the most limiting factor concerning the degradation with small gate length of low-field mobility in both planar and tri-gate nanowire JLTs.

3. Channel access resistance effect on carrier mobility and low frequency noise characteristics of 1D SnO_2 nanowire FET

One-dimensional (1D) metal oxide nanowires (NWs) have attracted much interest because of their unique properties such as high surface-to-volume ratio, large aspect ratio, and carrier quantizing effects for practical applications ranging from electronic/optoelectronic devices to gas sensors.[25-30] Among them, SnO_2 NWs have been suggested as an excellent candidate for high performance flexible, transparent NW transistors, thin film transistors, and gas sensors with low temperature fabrication process.[31-35] However, the counterpart of such high sensitivity is poor device reliability and stability when used as transistor.[35, 36] To improve this, a polymer and an alumina (Al_2O_3) layer have been suggested as passivation layers with the aim of keeping adsorbents off the surface of metal oxide NWs.[37-39] For instance, a polymethyl methacrylate (PMMA) passivation layer has been found efficient in improving electrical properties, resulting in enhanced carrier mobility, larger on/off current ratio, and significant shift of V_{th}.[37-39] However, care should be taken in extracting these parameters. In particular, in such quasi-1D nanostructures, parameters such as μ can be considerably underestimated by R_{sd} influence.

In this study, in particular, R_{sd} effect on μ and LFN characteristics of PMMA passivated SnO_2 NW-FETs was focused. Analytical simulation was performed firstly to account for electrostatic coupling effects through the PMMA layer, as they influence the value of C_{gc} and, as a consequence, μ extraction and LFN analysis. Moreover, YFM was employed to directly evaluate the electrical parameters. Furthermore, LFN measurements were carried out to assess the reliability and the quality of the interfaces between the active channel area and the dielectric layers.

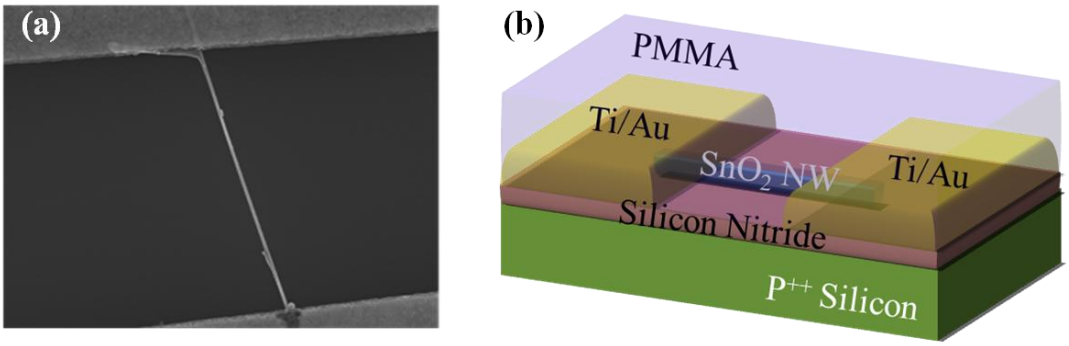


Figure 13 (a) FESEM image of SnO_2 NWs and (b) a simplified 3D structure of PMMA passivated SnO_2 NW-FET.

For this experiment, individual 1D SnO_2 NW-FETs were fabricated on 150nm silicon nitride (Si_3N_4). After, PMMA passivation layer was spin-coated on several devices with baking process. A FESEM image of a SnO_2 NW-FET and 3D view of the PMMA passivated SnO_2 NW-FET structure with a back-gate configuration are displayed in Figs 13(a) and (b), respectively.

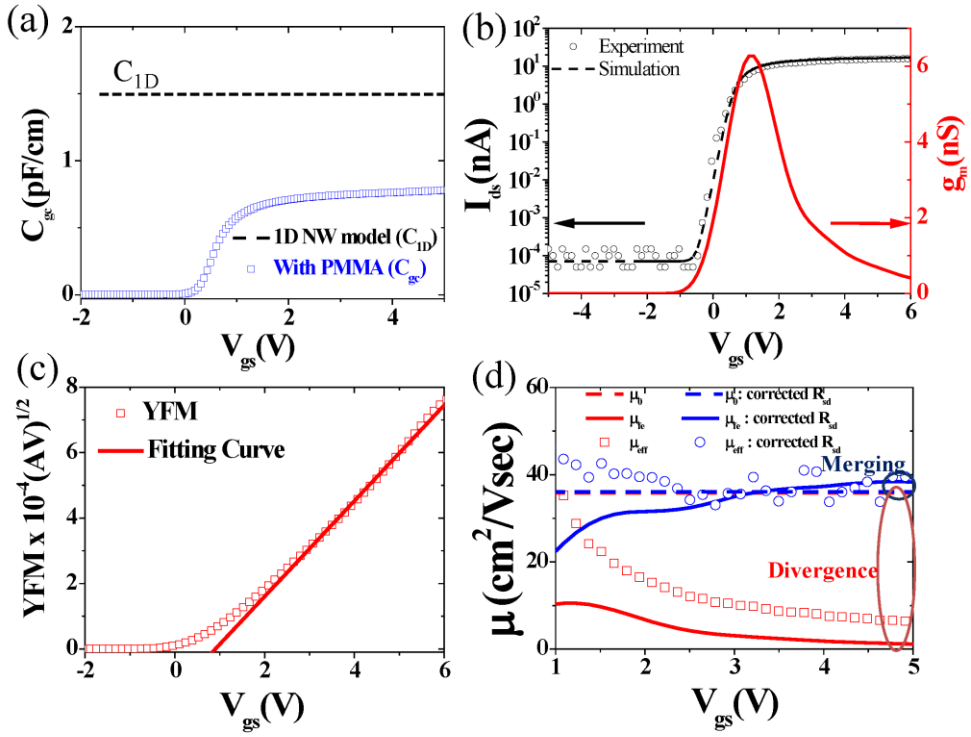


Figure 14 (a) Comparison capacitance values between the C_{1D} and simulated $C_{gc}(V_{gs})$ (open rectangular) respect to back-gate bias. (b) $I_{ds}(V_{gs})$ (open circle) and $g_m(V_{gs})$ (line) of SnO_2 NW-FET at V_{ds}=0.25V. Simulated $I_{ds}(V_{gs})$ (dotted circle) is added for comparison. (c) YFM(V_{gs}) curve with linear fitting line. (d) Comparison of various mobility (μ_0, μ_{fe}, μ_{eff}) before and after R_{sd} correction.

Several research groups have reported that PMMA passivation layer can give additional electrostatic gate coupling effects to metal-oxide NW-FETs compared to a non-passivated

one.[37-41] However, they have not yet accounted for these effects in C_{gc} for μ and LFN analysis. For better parameter interpretations, a preliminary numerical simulation was done to obtain $C_{gc}(V_{gs})$ and $I_{ds}(V_{gs})$ curves depending on V_{gs} taking into account the flat-band voltage (V_{fb}), interface trap density (D_{it}), and R_{sd}. To this end, Poisson-equation was solved with a finite-element-method across a two-dimensional (2D) cross-section of the SnO_2 NW-FET using FlexPDE with the actual size of the SnO_2-NW.

The simulated $C_{gc}(V_{gs})$ and their corresponding $I_{ds}(V_{gs})$ at V_{ds}=0.25V curves of SnO_2 NW-FET with PMMA passivation layer were obtained as presented in Figs 14(a) and (b) together with the constant 1D analytical gate capacitance model (C_{1D}) defined as below for comparison,[42]

$$\frac{C_{1D}}{L} = \frac{2\pi\varepsilon_0\varepsilon_r}{\cosh^{-1}\left(1+\frac{2t}{d}\right)} \quad [F/cm] \tag{5},$$

where d is the diameter of NW, ε_0 is the permittivity of free space, ε_r and t are the relative permittivity and the thickness of Si_3N_4, respectively. It turned out that C_{1D} (1.497pF/cm) was approximately twice as large (strictly, 1.85 times) than C_{gc} (0.808pF/cm). This is because the C_{1D} model assumes that the NW is fully wrapped by dielectrics. Hence, C_{1D} model could lead to underestimate μ by almost a factor two in PMMA passivated devices. Therefore, for further parameter extractions, the simulated value of C_{gc} in linear region (≈0.808pF/cm) will be used.

Simulated $I_{ds}(V_{gs})$ curve at fixed drain voltage (V_{ds}=0.25V) after accounting for $C_{gc}(V_{gs})$ from Fig. 14(a) is plotted in Fig. 14(b). It is almost identical to experimentally obtained $I_{ds}(V_{gs})$, indicating properly chosen simulation parameters. For static parameter analysis, V_{th} was extracted from the linear extrapolation of drain current at the point of maximum $g_m(V_{gs})$ and μ_{fe} was then determined by, $\mu_{fe}=g_m \cdot L/(V_{ds} \cdot C_{gc})$. However, it is well known from the physics of classical MOS-FET that R_{sd} can severely affect the accuracy of mobility extraction.[21, 38, 43, 44] Thereby, we employed YFM(V_{gs}) to evaluate μ_0, V_{th}, and mobility attenuation factor (θ). In addition, R_{sd} was obtained from θ by using below expression,[21, 44]

$$\theta = \frac{G_m \cdot V_{ds}}{I_{ds}} - \frac{1}{V_{gs}\text{-}V_{th}} \Rightarrow R_{sd} \approx \frac{\theta}{G_m} = \frac{V_{ds}}{I_{ds}} - \frac{1}{G_m \cdot (V_{gs}\text{-}V_{th})} \tag{6}.$$

Moreover, the effective mobility (μ_{eff}) was also estimated by following expression,

$$\mu_{eff} = \frac{I_{ds} \cdot L}{V_{ds} \cdot C_{gc\max} \cdot (V_{gs} - V_{th})} \tag{7},$$

where C_{gcmax} is the maximum C_{gc} value in strong accumulation region. To further analyze R_{sd} influence in terms of μ_0 from YFM, μ_{fe} from $g_m(V_{gs})$ and μ_{eff} from Eq. (7), all mobility values

are compared in case of before and after R_{sd} correction. As seen in Fig. 14(d), they are substantially diverged as V_{gs} increased. This can be attributed to the large value of R_{sd}, which resulted in a significant reduction of the apparent μ_{fe} and μ_{eff} at high V_{gs} due to its large contribution to the total resistance ($R_{tot} = R_{ch} + R_{sd}$) compared to channel resistance (R_{ch}). It can be possible to exclude R_{sd} impact, if R_{sd} can be considered as independent of V_{gs}. Then, $I_{ds}(V_{gs})$ measured in linearly operated region can be modified by using the following equation,

$$I_{ds}' = \frac{I_{ds} \cdot V_{ds}}{V_{ds} - I_{ds} \cdot R_{sd}} = \frac{I_{ds}}{1 - I_{ds} \cdot R_{sd} \cdot V_{ds}^{-1}} \quad (8).$$

The same procedures as above were then followed for mobility extraction and the results are presented in Fig. 14(d). After R_{sd} correction, all mobility values are converging towards μ_0 value and the attenuation phenomena at high V_{gs} were fully removed. This implies that the decrease in mobility, observed above V_{gs} point of maximum $g_m(V_{gs})$, was indeed due to R_{sd}. Hence, YFM can be safely applied to SnO_2 NW-FET for reliable electrical parameter extraction, free from R_{sd} effects, and μ_0 can be regarded as the intrinsic mobility of the channel, nearly independent of V_{gs}.

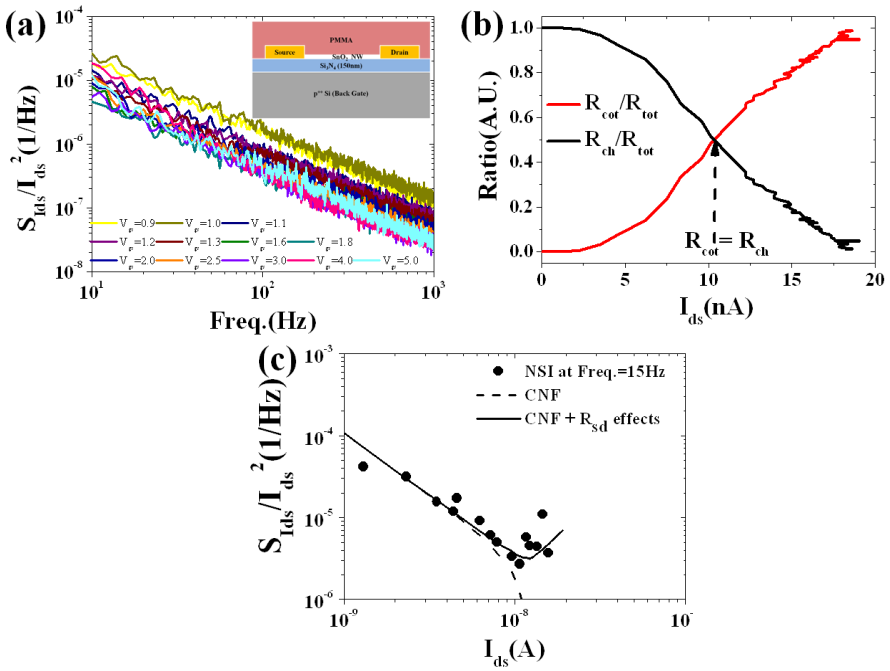


Figure 15 (a) I_{ds} normalized LFN for various V_{gs} regimes. (b) Relative contribution to total resistance of series resistance (R_{sd}/R_{tot}) and of the channel resistance (R_{ch}/R_{tot}) with respect to I_{ds}. At I_{ds}≈10nA, $R_{sd}/R_{tot}=R_{ch}/R_{tot}$. (c) Variation of S_{Id}/I_{ds}^2 (circle symbols). Solid line: CNF model. Dotted line: CNF+R_{sd} model.

Further, to investigate on a trapping/de-trapping mechanism between SnO_2 and surrounding dielectrics, LFN measurement was carried out. As can be seen in Fig. 15(a), I_{ds} nor-

malized LFN power spectrum density (PSD) shows a 1/f dependency. It should be noted that R_{sd} effect in such narrow channel is very important. Thereby, to compare the relative contribution of R_{sd} to the total resistance (R_{sd}/R_{tot}) with that of the channel resistance (R_{ch}/R_{tot}) in SnO_2 NW-FET, these ratios were plotted together with respect to I_{ds} in Fig. 15(b). At the position where I_{ds} is ≈10nA, the relative ratio was such that $R_{sd}/R_{tot}=R_{ch}/R_{tot}=0.5$, and R_{sd} overtook R_{ch} in the total resistance beyond this current level.

For the sake of LFN analysis, I_{ds} normalized LFN-PSD (S_{Ids}/I_{ds}^2) is plotted in Fig. 15(c). The correlation of I_{ds} normalized LFN level with $S_{Vfb}\times(g_m/I_{ds})^2$ clearly demonstrates that the CNF mechanism is predominantly observed. Such correlation is due to the carrier fluctuations associated with the trapping/de-trapping of charge carriers at the interface with the dielectrics. Good correlation was obtained from depletion to strong accumulation region, except for the high I_{ds} regime, above I_{ds}≈10nA. This discrepancy was consistently explained by R_{sd} effects as expected from Fig. 15(b). Indeed, the I_{ds} normalized LFN in CNF model is usually given by,

$$\frac{S_{I_{ds}}}{I_{ds}^{\ 2}} = S_{V_{fb}}\left(\frac{g_m}{I_{ds}}\right)^2 = \frac{q^2 k_B T N_{NW}}{L C_{gc\max}^{\ 2} f}\left(\frac{g_m}{I_{ds}}\right)^2 \quad (9),$$

where S_{Vfb} is the flat-band voltage of PSD, q is electron unit-charge, k_BT is the thermal energy and N_{NW} is linear trap density along the NW.[45] However, this CNF model should be modified to account for R_{sd} effects. To do this, we incorporated the PSD of R_{sd} into the CNF model by the following relation,

$$\frac{S_{I_{ds}}}{I_{ds}^{\ 2}} = S_{V_{gs}}\left(\frac{g_m}{I_{ds}}\right)^2 + \frac{S_{R_{sd}}}{R_{sd}^{\ 2}} R_{sd}^{\ 2}\left(\frac{I_{ds}}{V_{ds}}\right)^2 \quad (10),$$

where S_{Vgs} is the input-referred noise and S_{Rsd} is the channel access resistance noise.[46] Finally, this CNF+R_{sd} model of Eq. (10), is more applicable to interpret the behavior of LFN than the CNF model itself. R_{sd} normalized noise value (S_{Rsd}/R_{sd}^2) was extracted to be $6.5\times10^{-6}Hz^{-1}$ and the linear density of traps along the nanowire (N_{NW}) lied around $3.0\times10^{7}eV^{-1}\cdot cm^{-1}$.

In this study, R_{sd} effect on μ and LFN in a PMMA passivated SnO_2 NW-FET was investigated. The effective C_{gc} was obtained from TCAD simulation accounting for real dimensions and electrostatic coupling effects associated with the presence of the PMMA. YFM was employed to directly evaluate the electrical parameters without the influence of R_{sd}. In addition, μ_0 was compared with other mobility values such as μ_{fe} and μ_{eff}. After R_{sd} correction, all mobility values were consistent with the intrinsic μ_0. Finally, LFN was clearly attributed to CNF model provided R_{sd} effects were incorporated and the N_{NW} in SnO_2 NW-FETs with PMMA passivation layer was deduced from LFN analysis. This methodology can be applied to account for R_{sd} with

other quasi-1D devices as and other passivation materials.

4. Static and LFN characteristics in 2D carbon nanotube random network thin film transistors

Carbon nanotubes (CNTs) are 1D cylindrical honeycomb nano-structure composed of rolled up one or more graphene sheets. It has been gained a great attention by researchers due to its unique properties such as a nearly ideal 1D structure, high potential to open a quasi-ballistic carrier transport, high mechanical and thermal stability. Despite aforementioned many advantages in an individual CNT-FET, there are many challenges to be overcome as a next generation electronic device. The most urgent issues in present of these are the insufficient current output driven from such extremely small scaled 1D structure and the lack of practical fabrication methods to shrunk device-to-device variation.[47]

Currently, with the aim of a low-cost mass production and an averaging out the wide device differences arisen from the divergence of the electrical properties of pristine CNTs, 2D random network thin film transistors (RN-TFTs) have been proposed.[47-52] This approach can provide high reproducibility and reliability as a promising candidate for large-scaled, inexpensive, transparent, and flexible electronics.[47-50, 52-54] In spite of progress in device fabrication and synthesis methods for preferential semiconducting CNTs, there are still lacks of understanding in static and LFN characteristic of RN-TFTs.

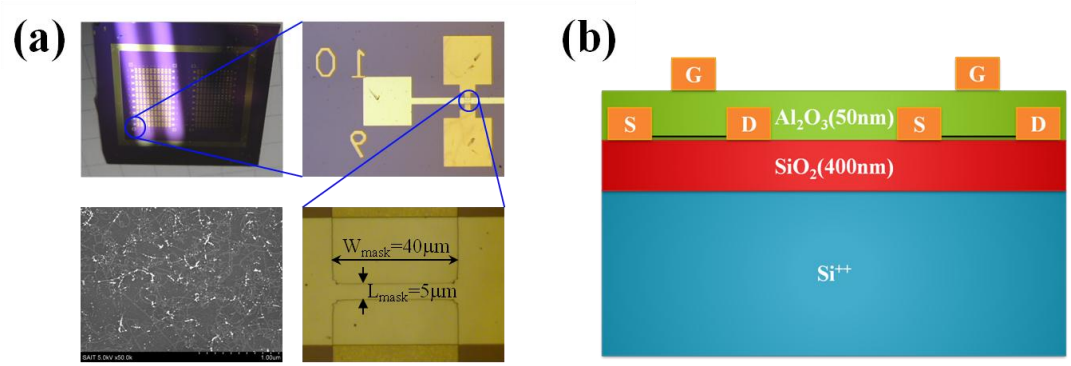


Figure 16 (a) Optical images of RN-TFTs and a representative SEM image of synthesized single-walled CNTs. (b) A simplified cross section view of fabricated top-gate RN-TFTs.

In this study, the various electrical properties based on static and LFN characteristics of N-type 2D RN-TFTs were firstly evaluated with two different capacitance values, the simple 2D plate capacitance model (C_{2D}) and the experimental C_{gc} directly measured by the split CV method, respectively. Besides, to have a better understanding of percolation effects and random aspects especially for the interpretation of C_{gc}, a 2D finite numerical percolation simulation was

also performed. Finally, to have a good agreement based on static and LFN results, C_{1D} analytical model was suggested for an improved interpretation of C_{gc}.

For this research, several RN-TFTs which have L_{mask} (=2, 3, 5, 7, 10μm) with fixed W_{mask} (=40μm) were fabricated by SAIT. Single-walled CNTs were synthesized by water-assisted CH_4 plasma enhanced chemical vapor deposition system on highly doped silicon substrates with 400nm thick BOX. The desired active channel areas were pre-patterned by conventional photo-lithography. The average diameter (d), length and density of CNTs in such fabricated RN-TFTs (d≈0.8~1.2nm, L_{CNT}≈1~2μm, ρ_{CNT}≈20/μm^2, respectively) were directly estimated by SEM image as seen Fig. 16(a). Optical device images of the fabricated RN-TFTs and a simplified cross section view are displayed in Figs 16(a) and (b), respectively.

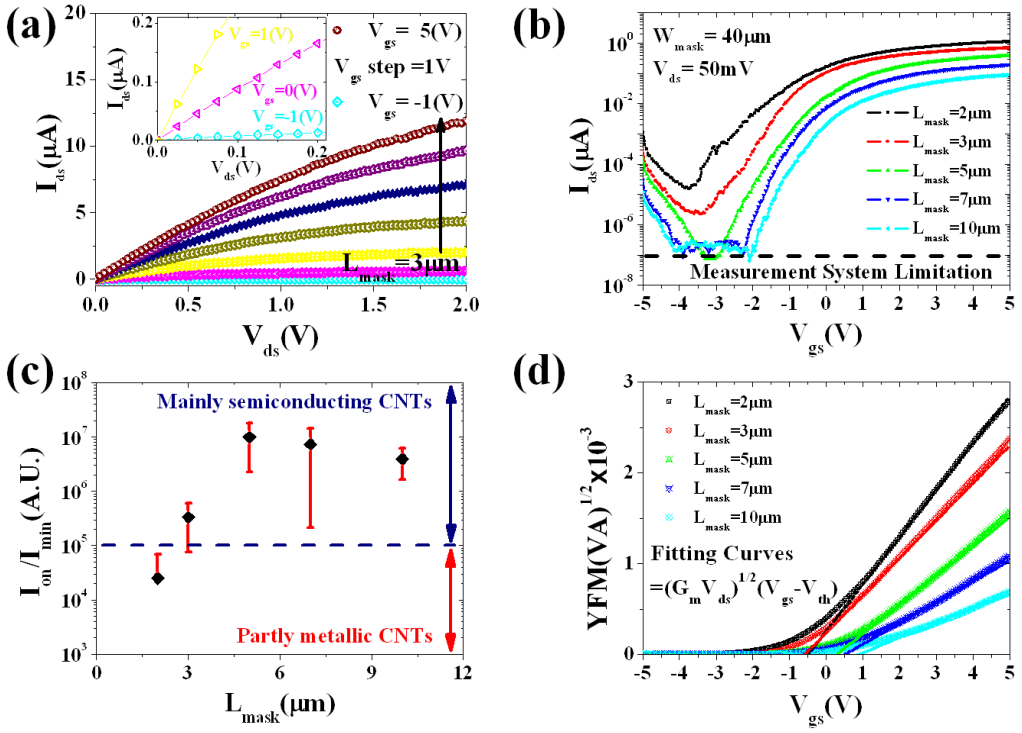


Figure 17 (a) Representative output characteristic $I_{ds}(V_{ds})$ curves of RN-TFTs depending on V_{gs} in case of L_{mask}=3μm. (inset: the magnification view of small V_{ds} region) (b) Typical transfer $I_{ds}(V_{gs})$ curves with respect to different L_{mask} at V_{ds}=50mV (c) I_{on} and I_{min} ratio versus L_{mask} (d) YFM(V_{gs}) (symbols) and corresponding fitting curves (dotted lines) with respect to L_{mask}.

Representative $I_{ds}(V_{ds})$ and $I_{ds}(V_{gs})$ curves are presented in Figs 17(a) and (b). It shows general N-type semiconducting FETs with high on and off current ratio proving the high quality of the semiconducting CNTs except for 2μm case. In this case, a certain amount of metallic paths may start to be involved, leading to large leakage below threshold. (See also Fig. 17(c)) Based on these properties, we can conclude that the transport in such devices is quite surely

limited by CNTs underneath the gate. For further static analysis, YFM was employed as displayed in Fig. 17(d) with C_{2D} but in fact we need actual gate capacitance value to evaluate the electrical parameter of RN-TFTs since this is not the case of 2D film configuration.

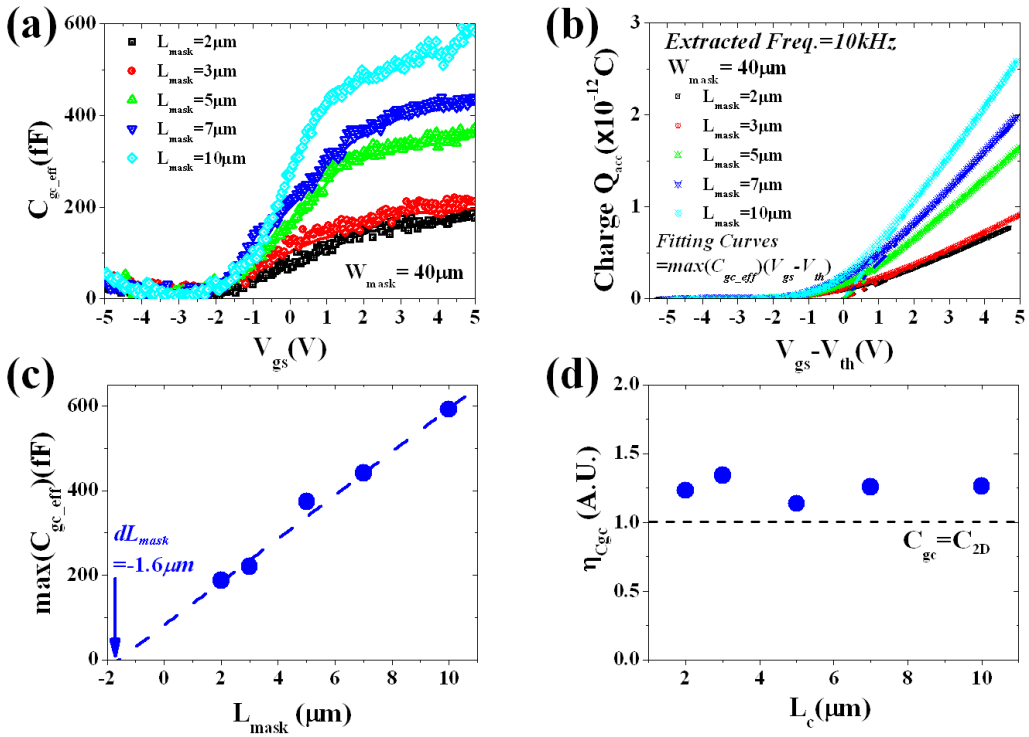


Figure 18 (a) $C_{gc\_eff}(V_{gs})$ curves of a top-gate RN-TFTs at f=10kHz (b) $Q_{acc}(V_{gs})$ (symbols) with linear fitting lines ($\approx max(C_{gc\_eff})\times(V_{gs}-V_{th})$, dotted lines) (c) $max(C_{gc\_eff})$ and (d) η_{Cgc} verses L_{mask} and L_C, respectively.

To this end, the effective C_{gc} of RN-TFTs was directly obtained by the split CV technique to exclude CNT islands and parasitic capacitance arisen from S/D pads as plotted in Fig. 18(a). By integrating C_{gc_eff} with respect to V_{gs}, total accumulation charge was obtained as well. (See Fig. 18(b)) In addition, the negative dL_{mask} was found as shown in Fig. 18(c) but it can be explained by the longer percolation transport length than L_{mask}. Based on these findings, two parameters are introduced in this approach, the effective length in for CV measurements L_C ($=L_{mask}-dL_{cap}$) and the overestimation factor compared to C_{2D}, η_{Cgc} ($=C_{2D}W_{mask}L_C/[max(C_{gc\_eff})]$), indicating how much C_{2D} is overestimated compared to $max(C_{gc\_eff})$. As seen displayed in Fig. 18(d), if C_{2D} value was used for electrical parameter extraction, it can be 1.2 times over- or under-estimated. But, it is worth mentioning that the linear extrapolation method used in Fig. 18(c) should be taken with care for random network systems. Indeed, dL_{cap} can not be the same for all RN-TFTs and $max(C_{gc\_eff})$ values could be easily influenced by percolation effects, with in fact a finite number of percolation channels. In addition, it may lead to a wrong conclusion if one used $max(C_{gc\_eff})$ directly for device parameter extraction, without thorough consideration

of dominant current percolation paths in RN-TFTs. In fact, depending on their path resistance, only a few percolation paths in RN-TFTs may dominantly contribute to carrier transport. Further discussion about an alternative interpretation of max(C_{gc_eff}) in RN-TFTs will be presented after 2D numerical percolation simulation part.

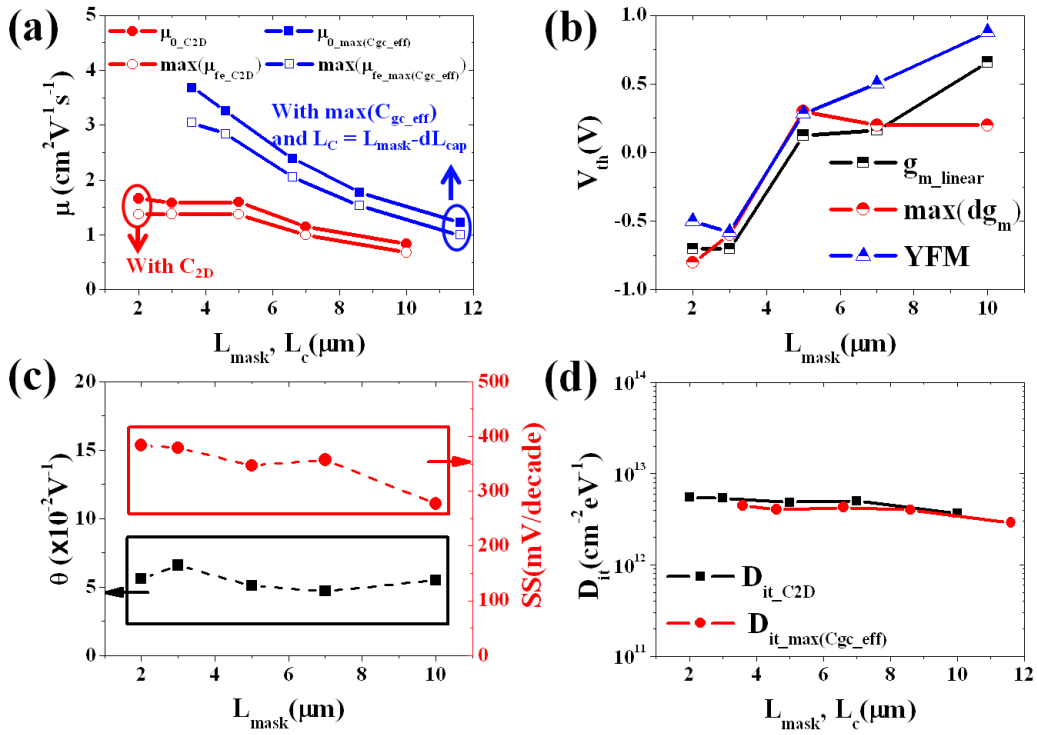


Figure 19 (a) μ_0 extracted from C_{2D} with L_{mask} (red lines) and μ_{fe} from max(C_{gc_eff}) with L_C (blue lines), respectively (b) V_{th} versus L_{mask} based on various V_{th} evaluation techniques (c) θ (circle) and SS (rectangular) with respect to different L_{mask} (d) D_{it} extracted from C_{2D} with L_{mask} (rectangular) and max(C_{gc_eff}) with L_C (circle), respectively.

Figures 19(a)-(d) are displaying carrier mobility, V_{th}, θ, SS and D_{it} values in terms of C_{2D} with L_{mask} and max(C_{gc_eff}) with L_C, respectively. Both mobility behaviors are increased slightly when L_{mask} or L_C is shorten due to reduced the number of junction effect and increased the number of conduction channel. Moreover, it can be mentioned that μ could be much improved by synthesizing longer or perfectly aligned CNTs in order to diminish the junction effects in the conducting paths. For V_{th} evaluation, three methodologies were applied in this study; 1) linear extrapolation of drain current at the point of maximum $g_m(V_{gs})$, 2) V_{gs} point of the maximum value of derivative g_m, max(dg_m), 3) linear extrapolation to zero of YFM(V_{gs}). The trend of V_{th} variation with respect to L_{mask} is mostly similar regardless of the extraction method. In addition, θ and the subthreshold swing (SS) are also respectively presented. D_{it} was also calculated from SS and it will be compared to the surface trap density (N_{st}) extracted from LFN analysis.

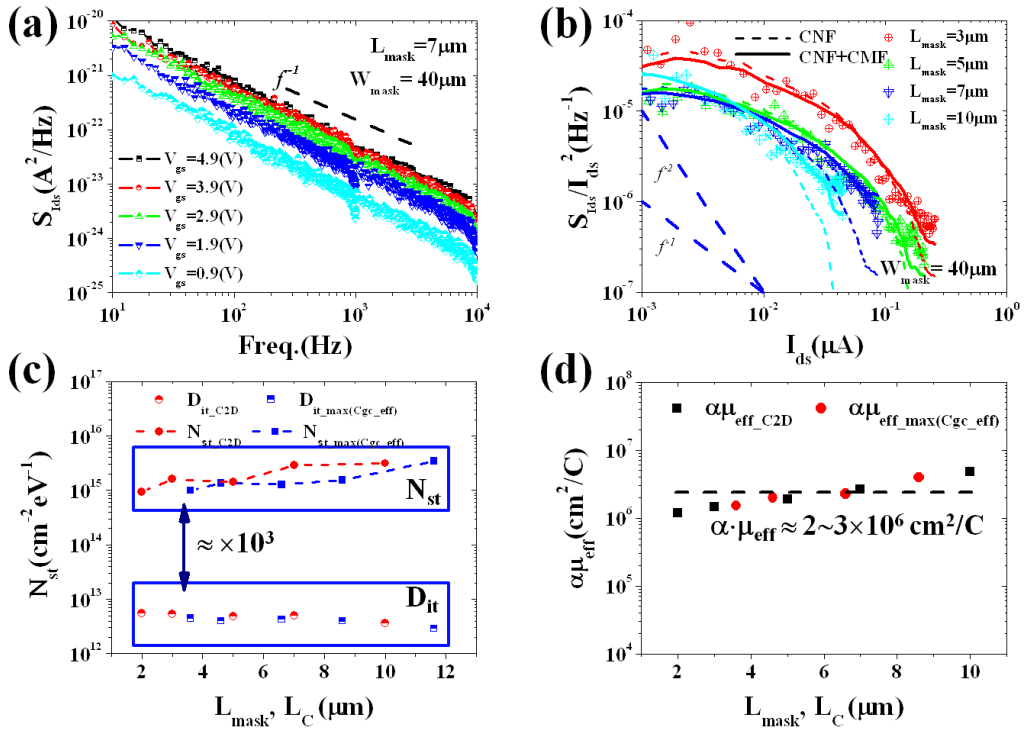


Figure 20 (a) LFN-PSD for different V_{gs} at V_{ds}=50mV (L_{mask}=7μm) (b) I_{ds} normalized LFN-PSD at f=10Hz (symbols) with CNF (dotted lines) and CNF-CMF (lines) fitting curves (c) Comparison of N_{st} and D_{it} versus L_{mask} and L_C, respectively (d) $\alpha\cdot\mu_{eff}$ depending on different L_{mask} and L_C, respectively.

To provide a diagnostic of noise sources of RN-TFTs, LFN measurement was carried out as a function of V_{gs} and L_{mask}. As seen in Fig. 20(a), the drain current power spectral density (PSD) was following the 1/f dependency. The drain current normalized LFN-PSD (S_{Ids}/I_{ds}^2) at a given frequency (f=10Hz) and $S_{Vfb}(g_m/I_{ds})^2$ curves are displayed together as a function of I_{ds} and L_{mask} in Fig. 20(b). For the sake of LFN analysis, the carrier number fluctuation noise (CNF) model and the carrier number and correlated mobility fluctuation (CNF-CMF) model were employed in this analysis. They are defined as follows,

$$\text{CNF:}\quad \frac{S_{I_{ds}}}{I_{ds}^{\,2}} = S_{V_{fb}}\left(\frac{g_m}{I_{ds}}\right)^2 = \frac{q^2 k_B T N_{st}}{L_{mask} W_{mask} C_{ox}^{\,2} f}\left(\frac{g_m}{I_{ds}}\right)^2 \qquad (11),$$

$$\text{CNF-CMF:}\quad \frac{S_{I_{ds}}}{I_{ds}^{\,2}} = \left(1+\alpha\cdot\mu_{eff}\cdot C_{ox}\frac{I_{ds}}{g_m}\right)^2 S_{Vfb}\left(\frac{g_m}{I_{ds}}\right)^2 \qquad (12),$$

where α is the Coulomb scattering coefficient. The very good consistency between the CNF-CMF model and LFN data clearly demonstrates that noise sources do originate from the trapping-detrapping of carriers by the traps located in the gate dielectric surrounding the surface of CNTs. Based on S_{Vfb} from Eq. (12), N_{st} and $\alpha\cdot\mu_{eff}$ were evaluated using both C_{2D} and

max(C_{gc_eff}) for different L_{mask} and L_C values, as drawn in Figs 12(c) and (d), respectively. However, the very big discrepancy between D_{it} and N_{st} was found and 10^{16} range of N_{st} seems to be unrealistic even though it can be possible if we consider the total number of carbon atoms in the network. Referred to Eqs (11) and (12), more realistic C_{ox} and W_{mask} should be required to properly evaluate N_{st}

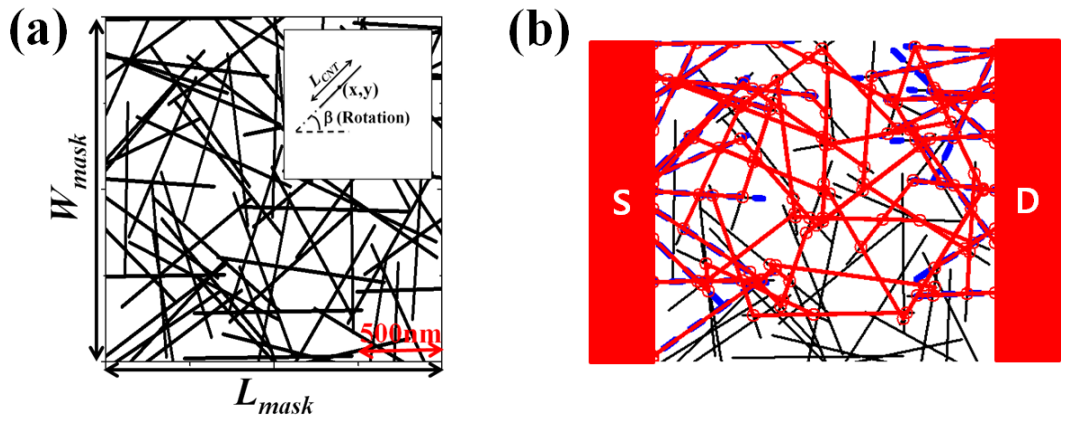


Figure 21 (a) A representative randomly generated set of 2D RN-TFTs (in case of L_{mask}=W_{mask}=2μm, ρ_{CNT}=#20/μm^2 and L_{CNT}=1μm) (b) Visualized all possible optimal pathways (red lines) from CNTs directly connected to S to D electrode (blue dotted line) in the case of Fig. 21(a). (Junction points between CNTs: small red circles)

To have a better picture for percolation phenomenon and interpretation of C_{ox} in such complex 2D random network system, a finite 2D numerical percolation simulation was carried out. With properly chosen CNT density and dimension of channel, a certain number of CNTs were generated by randomly chosen center position and orientation angle as seen Figs 21(a) and (b). The black lines are generated CNTs, the circles are junctions between CNTs, and the red sticks are the all possible the least resistive or shortest paths between S to D calculated by modified Floyd's algorism and adjacent matrix computation.

Based on this approach, the effective number and corresponding length of participated CNTs were obtained, respectively. In here, the number of red stick over total number of CNT (PR_{CNT}), the total sum of effective conduction length (L_{eff}), and the maximum number of channel by assuming perfectly aligned case (Max.N_{ch}) were respectively estimated. Figure 22 demonstrates that PR_{CNT} and Max.N_{ch} are sharply decreased as L_{mask} is increased, while L_{eff} is slightly enhanced. This can be explained by the percolation probability. As the distance from S to D is increased, more CNTs must be needed to maintain the same percolation probability. However, PR_{CNT}, L_{eff} and Max.N_{ch} are more or less linearly increased as W_{mask} is doubled since there is twice as much chance to build percolation paths in the channel. .since it can be considered as an independent event. With account for the simulation tendency, Max.N_{ch} can be esti-

mated for experimental results by assuming that all CNTs are perfectly aligned and mainly participating to a conduction path.

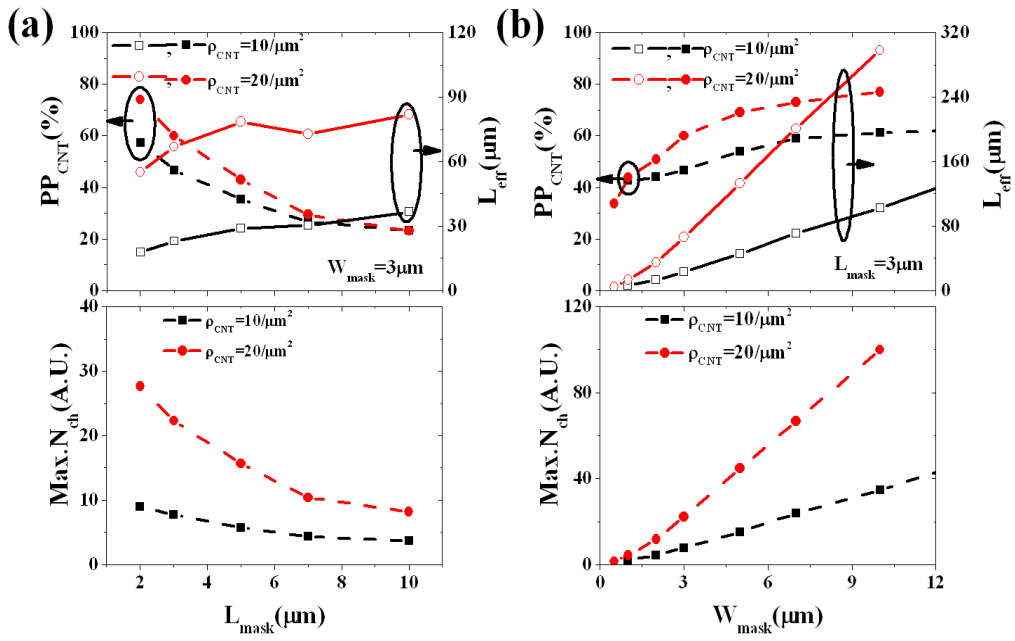


Figure 22 (a) PR_{CNT} and corresponding L_{eff} (top), and Max.N_{ch} (bottom) depending on L_{mask} with fixed W_{mask}=3μm (b) Same parameters depending on W_{mask} with fixed L_{mask}=3μm.

By this approximation, the width density (D_W) can be readily obtained depending on different situation, 1) $D_{W\_C2D}=C_{2D}/C_{1D}$, 2) $D_{W\_max(Cgc\_eff)}=max(C_{gc\_eff})/C_{1D}$, and 3) $D_{W\_Csim}=Max.N_{ch}/W_{mask}$. Especially, to obtain the gate coupling capacitance (C_{Sim}) based on the simulation results, D_{W_Csim} was applied to rigorous CNT capacitance model for perfectly aligned system.[50, 55] To confirm the effectiveness of C_{Sim}, N_{st} and D_{it} were recalculated and compared together in Fig. 23(b). The discrepancy between the two values was reduced by one decade, but still remains large. It can be attributed to the overestimation of N_{ch} arising from the assumption that all the CNTs are perfectly aligned in the channel and participating to carrier transport. In addition, we counted all possible pathways from S to D regardless of path resistance. Moreover, as displayed in Fig. 23(c), there are not many low-resistance conduction paths when L_{mask} is increased. This is due to the fact that current concentrates towards a few optimal and dominant CNT paths, which are shared by the different channels. Therefore, in realistic situation, D_W can be much smaller than in our previous assumption of a perfectly aligned system.

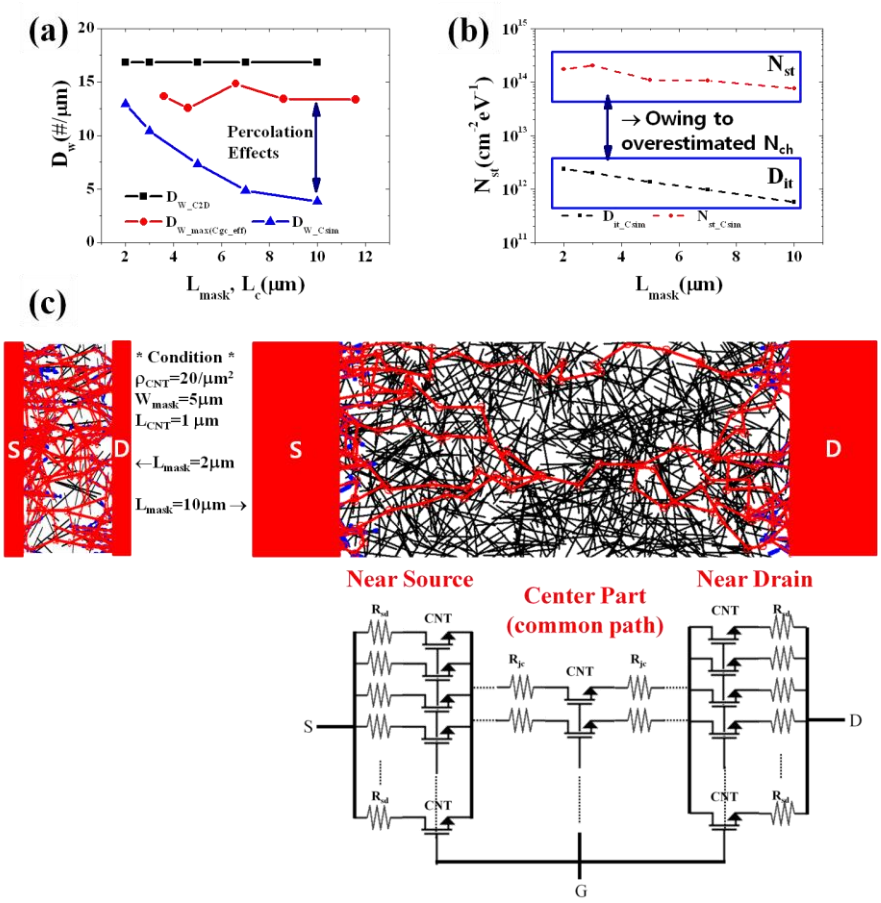


Figure 23 (a) D_W based on C_{2D}, max(C_{gc_eff}), and C_{Sim} (b) N_{st} and D_{it} extracted from C_{Sim} (c) Comparison the effective D_{W_Csim} between L_{mask}=2μm and L_{mask}=10μm with fixed W_{mask}=5μm in random network system. (Simplified electrical equivalent circuit was displayed)

With account for all aspects discussed previous paragraph, C_{1D} analytical model was suggested as a much realistic capacitance model than C_{2D} for the evaluation of C_{ox}, and even better than measured C_{gc} and C_{Sim} in 2D RN-TFT system. This is because the main conduction mechanism in such system was based on 1D semiconducting CNTs and few percolation pathways were able to dominantly participate to carrier transport through 1D CNTs. (See the inset of Fig. 24(a)) Taking into account for the fact that screening and coupling effects are bringing a relative small contribution to total effective gate capacitance with a random network configuration, the effective total length (L_{tot}) can be evaluated from max(C_{gc_eff}) and the 1D capacitance C_{1D}. To this end, six parameters were defined as following expressions; 1) L_S and C_S; the total sum of length of CNTs ($L_S=\sum_j L_{S_j}$) and its corresponding capacitance ($C_S=\sum_j C_{S_j}$) which are electrically connected to S only, 2) L_D and C_D; as the same definitions for D only ($L_D=\sum_j L_{D_j}$ and $C_D=\sum_j C_{D_j}$), 3) L_{SD} and C_{SD}; as the same definitions for S and D simultaneously only ($L_{SD}=\sum_j L_{SD_j}$ and $C_{SD}=\sum_j C_{SD_j}$), respectively. The sum of these lengths and ca-

pacitances should be equal to L_{tot} ($\approx L_S+L_D+L_{SD}$) and max(C_{gc_eff}) ($\approx C_S+C_D+C_{SD}$), respectively. By this way, C_{eff} in RN-TFTs should be expressed by only accounting for L_{SD} and C_{SD} as defined below,

$$C_{eff} = \frac{C_{SD}}{L_{SD}} \approx \frac{1}{L_{SD}}\left(\max(C_{gc\_eff}) \times \frac{L_{SD}}{L_{tot}}\right) \approx \frac{\max(C_{gc\_eff})}{L_{tot}} \approx C_{1D} \quad (13).$$

Secondly, we notice that μ_0 or μ_{fe} should take similar values in RN-TFTs and in 1D CNT-FETs for L_{mask}=2μm, with maximum reported values $\mu_{fe} \approx 10^5 cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature. Indeed, if C_{2D} or max(C_{gc_eff}) was used for μ_{fe} evaluation owing to the large number of N_{ch} resulting from high ρ_{CNT}, the effective impacts of N_{jc} and R_{jc} on μ_0 (or μ_{fe}) can be neglected with the compatible L_{CNT} and λ_{CNT} with L_{mask} in such RN-TFTs. Furthermore, R_{sd} effects were already excluded by YFM technique. Therefore, it is apparent that this severe underestimation of μ_0 (or μ_{fe}) in such RN-TFTs compared to that of 1D CNT-FETs should mainly result from bad C_{ox} evaluation.

Third, the theoretical capacitance range to coincide N_{st} with D_{it} should have following relation,

$$C_{ox} = \left(\frac{SS}{\ln(10)k_BT} - 1\right)\frac{qk_BT}{S_{V_{fb}} L_{mask} W_{mask} f} \approx \frac{C_{1D}}{W_{mask}} \quad (14).$$

Based on this approach, we revisited the previous parameter extraction procedures with C_{1D}. As presented in Figs 6-24(a) and (b), carrier mobility values are more realistic, one or two decade smaller than for 1D CNT-FETs due to junction effects between CNTs in our 2D RN-TFTs. In addition, the big discrepancy between D_{it} and N_{st} is now fully removed. Furthermore, it is a few times larger than N_{st} calculated from LFN amplitude data from previous works on 1D CNT-FETs with high-k dielectrics.

Besides, it is worth mentioning that L_{tot} and the experimentally measured ρ_{CNT}' can be estimated by $L_{tot} \approx \max(C_{gc\_eff})/C_{1D}$ and $(L_{tot}/L_{CNT})/(L_{mask} \cdot W_{mask})$, respectively. This could be another alternative method to evaluate the effective ρ_{CNT} based on the split-CV technique incorporated with C_{1D} instead of using an optical image processing method.

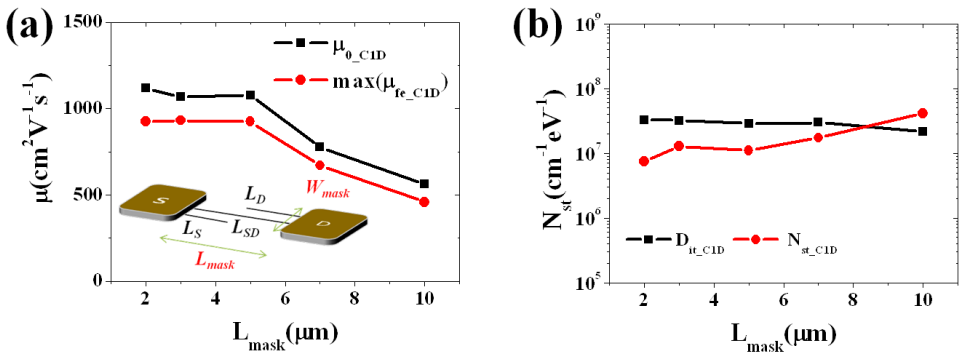


Figure 24 μ_0 and μ_{fe} extracted from C_{1D} (inset: simplified device configuration of RN-TFTs for the split CV measurements) (b) Recalculated N_{st} and D_{it} with C_{1D} versus L_{mask}, respectively.

In this study, static and LFN characterizations of RN-TFTs were presented for different gate lengths. To exclude R_{sd} effect, YFM method was applied for the extraction of electrical parameters. To get rid of the capacitance effects originated from isolated CNTs islands and to directly measure C_{gc}, the split CV measurement technique was used. Moreover, to get a better interpretation of C_{gc} in percolation-dominated 2D RN-TFTs, we employed a 2D finite numerical simulation. LFN measurements also were carried out and the results were well interpreted by the carrier number fluctuations with correlated mobility fluctuation model. Finally, a C_{1D} analytical model was suggested and applied. It provided better consistency between all electrical parameters based on experimental and simulation results.

5. Conclusions

In this thesis, as a top down based advanced FET, JLTs were fabricated by CEA LETI and characterized in terms of CV, IV at low temperature with a dual gate mode. The temperature dependence of various electrical parameters such as V_{th}, V_{FB}, bulk mobility, and low field mobility in accumulation regime were separately presented with account for the charge based analytical JLT model. It turns out that the temperature independent neutral defects and phonon scattering mechanism are the most mobility limiting factor in such heavily doped JLTs. In addition, as a bottom up based transparent and flexible future device, 1D PMMA passivated SnO_2 NW FET was fabricated. To have an electrostatic capacitance with account for PMMA passivation layer, TCAD simulation was firstly carried out. In addition, R_{sd} effects in carrier mobility and LF noise behaviors were successfully demonstrated in here. Lastly, as a carbon based advanced FET, quasi 2D N-type CNT RN-TFTs were fabricated by SAIT. Various electrical measurement results of CV, IV and LFN characteristics in 2D random network thin film transistors were systematically investigated. To have a better picture of percolation dominant carrier transport and corresponding gate capacitance, a 2D finite numerical percolation simulation was

carried out. Finally, to properly evaluate electrical parameters of static and LFN in 2D RN-TFTs, analytical C_{1D} model was suggested.

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