Feasibility of a Direct Sampling Dual-Frequency SDR Galileo Receiver for Civil Aviation

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Résumé

Cette thèse étudie l'intérêt des architectures SDR (Software-Defined Radio) à échantillonnage direct pour des récepteurs Galileo dans le contexte particulier de l'Aviation Civile, caractérisé notamment par une exigence de robustesse à des interférences bien spécifiées, principalement les interférences causées par les signaux DME (Distance Measuring Equipment) ou CW (Carrier Wave).
Le concept de Software Defined Radio traduit la migration toujours plus grande, au sein des récepteurs, des procédés de démodulation d'une technologie analogique à du traitement numérique, donc de façon logicielle. La quasi généralisation de ce choix de conception dans les architectures nouvelles nous a conduit à le considérer comme acquis dans notre travail.
La méthode d'échantillonnage direct, ou Direct Sampling, quant à elle consiste à numériser les signaux le plus près possible de l'antenne, typiquement derrière le LNA (Low-Noise Amplifier) et les filtres RF (Radio Frequency) associés. Cette technique s'affranchit donc de toute conversion en fréquence intermédiaire, utilisant autant que possible le principe de l'échantillonnage passe-bande afin de minimiser la fréquence d'échantillonnage et en conséquence les coûts calculatoires ultérieurs.
De plus cette thèse s'est proposée de pousser jusqu'au bout la simplification analogique en renonçant également à l'utilisation de l'AGC (Automatic Gain Control) analogique qui équipe les récepteurs de conception traditionnelle. Seuls des amplificateurs à gain fixe précéderont l'ADC (Analog to Digital Converter).
Ce mémoire rend compte des travaux menés pour déterminer si ces choix peuvent s'appliquer aux récepteurs Galileo multifréquences (signaux E5a et E1) destinés à l'Aviation Civile. La structure du document reflète la démarche qui a été la notre durant cette thèse et qui a consisté à partir de l'antenne pour, d'étape en étape, aboutir au signal numérique traité par la partie SDR.
Après une introduction détaillant le problème posé et le contexte dans lequel il s'inscrit, le deuxième chapitre étudie les exigences de robustesse aux interférences auquel doit se soumettre un récepteur de navigation par satellites destiné à l'Aviation Civile. Il s'agit de la base qui conditionne toute la démarche à suivre.

Le troisième chapitre est consacré au calcul des fréquences d'échantillonnage. Deux architectures d'échantillonnage sont proposées. La première met en œuvre un échantillonnage cohérent des deux bandes E5a et E1 tandis que la seconde implémente un échantillonnage séparé. Dans les deux cas, la nécessité de filtres RF supplémentaires précédant l'échantillonnage est mise en évidence. L'atténuation minimale que doivent apporter ces filtres est spécifiée.
Ces spécifications sont suffisamment dures pour qu'il ait été jugé indispensable d'effectuer une étude de faisabilité. C'est l'objet du chapitre quatre où une approche expérimentale à base d'un composant disponible sur étagère a été menée.
La problématique de la gigue de l'horloge d'échantillonnage, incontournable ici eu égard à la haute fréquence des signaux à numériser, est étudiée dans le chapitre cinq. Des résultats de simulation sont présentés et un dimensionnement de la qualité de l'horloge d'échantillonnage est proposé.
Dans le chapitre six, la quantification, second volet de la numérisation, est détaillée. Il s'agit très précisément du calcul du nombre minimum de bits de quantification que doit exhiber l'ADC pour représenter toute la dynamique, non seulement du signal utile mais aussi des interférences potentielles.
Au vu des débits de données conséquents mis en évidence dans les chapitres trois et six, le chapitre sept évalue la possibilité de réduire la dynamique de codage du signal à l'aide de fonctions de compression.
Le dernier chapitre est focalisé sur la séparation numérique des bandes E5a et E1 dans l'architecture à échantillonnage cohérent introduite au chapitre deux. Ici aussi l'atténuation minimale que doivent apporter les filtres requis est spécifiée.
Et finalement la conclusion synthétise les résultats obtenus et propose des idées de travaux complémentaires destinés à enrichir les contributions de cette thèse.

Abstract

This thesis studies the relevance of DS (Direct Sampling) SDR (Software-Defined Radio) architectures applied to Galileo receivers in the specific context of Civil Aviation, characterized in particular by strict requirements of robustness to interference, in particular, interference caused by DME (Distance Measuring Equipment) or CW (Carrier Wave) signals.
The Software Defined Radio concept renders the major tendency, inside the receiver, to move the demodulation part from an analog technology to digital signal processing, that is software. The choice of this kind of design is nearly generalized in new receiver architectures so it was considered the case in this work.
The Direct Sampling method consists in digitizing the signal as close as possible to the antenna, typically after the LNA (Low-Noise Amplifier) and the associated RF (Radio Frequency) bandpass filter. So this technique does not use any conversion to an intermediate frequency, using as much as possible the bandpass sampling principle in order to minimize the sampling frequency and consequently the downstream computational costs.
What is more, this thesis aiming at the greatest simplification of the analog part of the receiver, the decision was made to suppress the analog AGC (Automatic Gain Control) which equips the receivers of classical architecture. Only fixed gained amplifiers should precede the ADC (Analog to Digital Converter).
This document exposes the work done to determine if these choices can apply to a multifrequency (E5a and E1 signals) Galileo receiver intended for a Civil Aviation use. The structure of the document reflects the approach used during this thesis. It progresses step by step from the antenna down to the digital signal, to be processed then by the SDR part.
After an introduction detailing the problem to study and its context, the second chapter investigates the Civil Aviation requirements of robustness to interference a satellite navigation receiver must comply with. It is the basis which completely conditions the design process.

The third chapter is devoted to the determination of the sampling frequency. Two sampling architectures are proposed: the first implements coherent sampling of the two E5a and E1 bands while the second uses separate sampling. In both cases the necessity to use extra RF filters is shown. The minimum attenuation to be provided by these filters is also specified.
These requirements are strong enough to justify a feasibility investigation. It is the subject of chapter four where an experimental study, based on a SAW (Surface Acoustic Wave) filter chip available on the shelf, is related.
The issue of the sampling clock jitter, of concern with the Direct Sampling technique because of the high frequency of the signal to digitize, is investigated in chapter five. Some simulation results are presented and a dimensioning of the quality of the sampling clock is proposed.
In chapter six, quantization, a byproduct of digitization, is detailed. Precisely it is the calculation of the number of bits the ADC must have to digitally represent the whole dynamic of, not only the useful signal, but also of the potential interference.
Considering the high binary throughput highlighted in chapters three and six, chapter seven evaluates the possibility to reduce the coding dynamic of the digital signal at the output of the ADC by means of compression functions.
The last chapter is focused on the digital separation of the two E5a and E1 bands in the coherent sampling architecture presented in chapter two. Here also specifications of minimum attenuation are given.
Lastly the conclusions synthesize the contributions of this thesis and proposes ideas for future work to enrich them and more generally the subject of DS-SDR Galileo receivers for Civil Aviation.

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a. Au sens propre comme au figuré :-X

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ADC

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AGC

Automatic Gain Control. iii, v, 5, 17, 18, 121, 126, 141, 151, 153, 184

ARAIM

Advanced Receiver Autonomous Integrity Monitoring System. 6

BAW

Bulk Acoustic Wave. 49, 78

BOC

Binary Offset Carrier. 4, 87

BPSK

Binary Phase Shift Keying. 4, 87

CPW

Coplanar Wave Line. 66

CW

Carrier Wave. iii, v, xviii, xix, 17, 18, 21–23, 30, 31, 40, 124, 128, 129, 132–136, 140, 141, 153, 154, 156–162, 165, 169–174, 177, 178

DC

Direct Current. 14

DC

Direct frequency Conversion. xv, 1–3, 9, 14

DF

Dual-Frequency. xv, 6, 7, 9, 13, 15–17, 23, 24, 28, 115, 151, 183, 185

DLL

Delay-Locked Loop. xvii, 85, 92–94, 96

DME

Distance Measuring Equipment. iii, v, 18, 21–23, 127, 128, 132, 133, 136

DS

Direct Sampling. v, vi, xv, 3–7, 9, 13, 15–17, 23, 24, 28, 87, 115, 151, 183, 185

DSP

Digital Signal Processor. 1, 151

ENAC

École Nationale de l'Aviation Civile. vii

ENC

European Navigation Conference. 8

FIR

Finite Impulse Response. xix, 143–145, 147, 148, 151, 181

FLL

Frequency Locked Loop. 92

FPGA

Field-Programmable Gate Array. 1, 182

GBAS

Ground-Based Augmentation System. 6

GLONASS

Global Navigation Satellite System. 3, 4, 13, 28

GNSS

Global Navigation Satellite System. xv, 1–9, 13–15, 17, 18, 20, 27–30, 39, 87, 89, 90, 100, 117–120, 153, 183, 185

GPS

Global Positioning System. 3–6, 13, 14, 28, 49, 70, 87, 90

GSL

GNU Scientific Library. 92

i.i.d.

Independent and Identically Distributed. 88, 98

ICD

Interface Control Document. 20

IF

Intermediate Frequency. xv, 1–4, 9, 15, 145

IIR

Infinite Impulse Response. 143

ION

Institute Of Navigation. 8

IRNSS

Indian Regional Navigational Satellite System. 3

LNA

Low-Noise Amplifier. iii, v, 118

MOPS

Minimum Operational Performance Specification. 5, 6, 8, 9, 13, 14, 18, 20, 21, 70

MSB

Most Significant Bit. 152–154

NB

Narrow Band. 18

NBI

Narrow Band Interference. 18, 21, 22

NCO

Numerically Controlled Oscillator. 100

OCXO

Oven Controlled Crystal Oscillator. 89, 109

OS

Open Service. 20, 21

PCB

Printed Circuit Board. xvi, xvii, 63, 66–82, 184

PhD

PhilosophiæDoctor. vii, 3, 8, 14, 90

PLL

Phase-Locked Loop. xvii, xviii, 7, 85, 89, 92–96, 98–102, 104–109, 112

PPS

Pulse Per Second. 90

PSD

Power Spectral Density. 22, 91, 121

QPSK

Quadrature Phase Shift Keying. 4, 87

QZSS

Quasi-Zenith Satellite System. 3

RF

Radio Frequency. iii–vi, xv, xvi, 3–9, 15–17, 22, 24, 29–32, 34, 39–41, 43, 49, 83, 87, 115, 118, 120, 122, 132, 136, 141, 143, 145, 151, 153, 154, 158, 160, 176, 177, 183–185

RHCP

Right Hand Circular Polarization. 20

RMS

Root Mean Square. 17, 99, 100

RNSS

Radio Navigation Satellite Service. 20

SAW

Surface Acoustic Wave. vi, 49, 52, 78, 83, 184

SBAS

Satellite-Based Augmentation System. 6, 14, 70

SDR

Software-Defined Radio. iii, v, vi, xv, 1, 3–7, 9, 13, 15–17, 23, 24, 28, 87, 115, 151, 183, 185

SIS

Signal In Space. 20

SMA

SubMiniature version A. 66

SV

Space Vehicle. 20, 91–93

TCXO

Temperature Controlled Crystal Oscillator. 89, 109

THD

Total Harmonic Distortion. 17

TIE

Time Interval Error. 98

VGA

Variable Gain Amplifier. 153

VSWR

Voltage Standing Wave Ratio. xvi, 50–52, 57, 58

1 Introduction

1.1 Background & Motivation

1.1.1 The Software Defined Radio Concept

Software is being increasingly used in new radio equipment designs, and in GNSS (Global Navigation Satellite System) receiver in particular, replacing the hardwired discrete components by programmable processors (FPGA (Field-Programmable Gate Array), DSP (Digital Signal Processor) or even general purpose processors like Intel®Pentium®). These chipsets perform all digital processing tasks such as correlation, acquisition and tracking. This is the SDR (Software-Defined Radio) concept which "globally lead to migrate from the fully transistor to the fully software" [1]. The current boundary between hardware and software in a modern GNSS receiver is typically schematized in figure 1.1 for an architecture with IF (Intermediate Frequency) conversion and in figure 1.2 for a typical architecture with DC (Direct frequency Conversion). An assessment of the performance of the DC architecture for a L1 and E5 receiver is done in [2], showing that it is a cost competitive alternative to the architecture with IF conversion, if the oscillator phase noise is contained.

The advantages of software over hardware are numerous and have been detailed in [3] and [4] for instance. Among all the advantages two stand out: a SDR GNSS receiver is reprogrammable, that is reconfigurable, and it makes use of less discrete components. The ability to reprogram the firmware of the receiver can allow general purpose upgrades such as safety corrections, but also opens the way to specific navigation improvements such as the capacity to cope with evolutions in the requirements, to take benefit of the provision of new services or even to

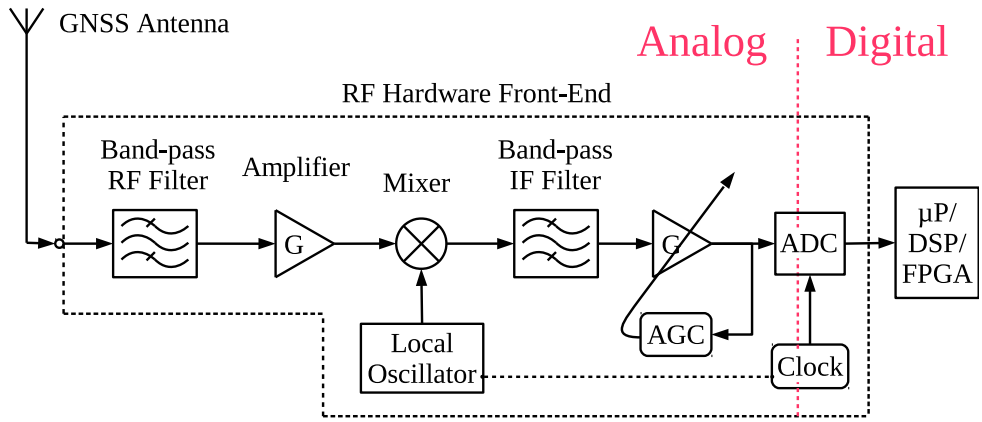

Figure 1.1: Boundary between hardware and software in a modern GNSS IF receiver.

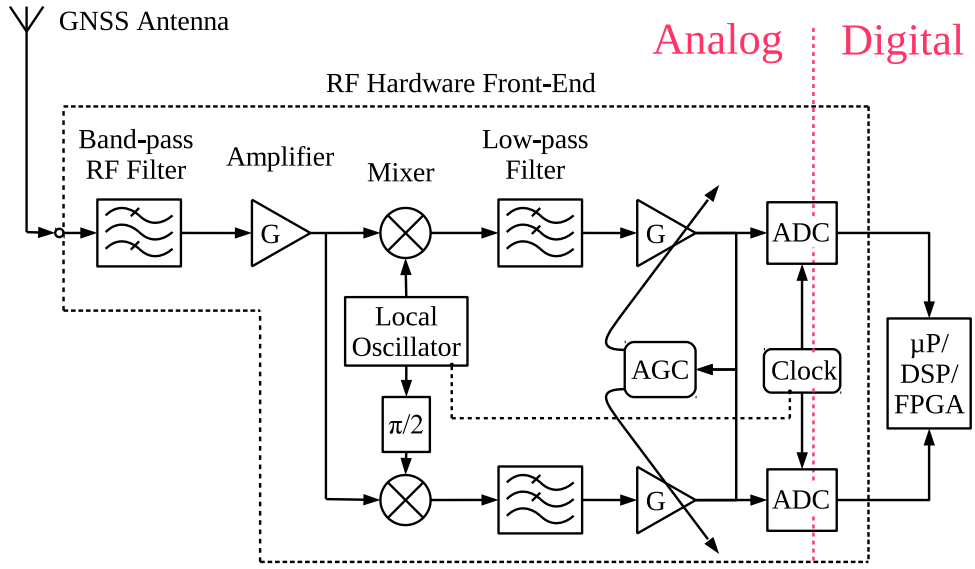

Figure 1.2: Boundary between hardware and software in a modern GNSS DC receiver.

take into account new navigation signals. A dual-frequency E1 and E5a Galileo software receiver could for example achieve benefit in the future of global or regional supplementary navigation signals, as the ones provided by the United States GPS (Global Positioning System) of course, but also the Russian GLONASS (Global Navigation Satellite System), the Chinese BeiDou, the Japanese QZSS (Quasi-Zenith Satellite System) or the Indian IRNSS (Indian Regional Navigational Satellite System). The elimination of sometimes expensive and bulky discrete components by a higher degree of digital integration is an advantage mainly for manufacturers. It provides not only an individual competitive edge but also offers the opportunity of product lines based on the same hardware platform, lowering the global development and production costs.

The first extensive work on the application of the SDR concept to GNSS receivers is [5]. This PhD thesis completely describes the implementation of a software GNSS receiver from the RF (Radio Frequency) front-end to the computation of the position solution. Matlab® codes corresponding to the different signal processing steps can be found in [6] or in [7]. In fact, the SDR concept has so spread through the GNSS community that implementations of SDR GNSS receivers are now freely available, as for example [8], a *GNSS SDR Toolbox for Matlab®*, or [9], an *open-source GNSS software receiver freely available to the research community.*

1.1.2 RF Direct Sampling

Each increase in computing capacity or advance in ADC (Analog to Digital Converter) technology brings the ADC closer to the antenna. Next to disappear should be IF or DC conversion stages as sampling frequencies high enough to allow RF-DS (Direct Sampling) are already available on the market. No more local oscillator nor mixer would be necessary, the signal being sampled at its original spectrum location. A schematic view of this evolution is proposed in figure 1.3.

A reference study on the main technique of this innovative design, RF-DS, is [10]. It presents the more general principle of Bandpass Sampling and details uniform sampling as well as quadrature sampling of a single band. One interesting conclusion is that in the general case, when the band to sample is not located at an integral number of bandwidths from the origin, quadrature sampling should not be applied although it leads to the optimum sampling frequency. The uniform bandpass sampling technique has been applied in the context of GNSS receivers in [11]. It presents a design study of a RF-DS GPS L1 receiver. The work has then be extended to multi-frequency receivers, as in [12] which describes a

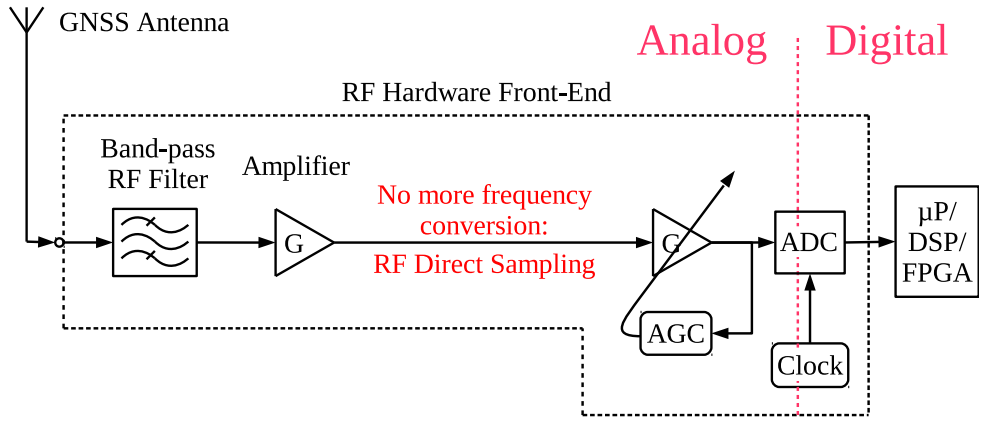

Figure 1.3: A SDR GNSS receiver architecture using Direct Sampling.

prototype processing the GPS L1 and GLONASS L1 bands, in [13], where a RF-DS front-end dedicated to the GPS L1 and L3 bands is shown, or as in [14], which presents the direct digitization of the GPS L1 and L2 bands. More recently a real-time solution up to the output of the decimation stage for a GPS L1 receiver is detailed in [15]. [16] supplements [12], [13], [14] and [15] by an investigation of quadrature sampling applied to single and multiple satellite navigation signals. It shows not only that the minimum required global sampling frequency is less for quadrature sampling than for uniform sampling, but also that the range of available sampling frequencies is greater when using the quadrature technique. In any case, the scientific publications on the subject of RF-DS receivers clearly identify this topic of multi-frequency direct sampling as a major research field, with a focus on the minimization of the sampling frequency as it directly conditions the downstream processing workload.

Coming along with the removal of any form of analog frequency down-conversion, the min to max amplitude of the RF signal at the input of the ADC is proportionally much higher than in the classical architecture. The sampling jitter is then of concern in Direct Sampling receivers as a literature survey has shown it. Among the works dealing with the effect of the sampling jitter on the navigation signals, [17] presents the effect of the jitter on the in-phase and quadrature accumulation of correlations in L1 GPS receivers using either RF Direct Sampling or IF conversion. [18] assesses jitter influence on BPSK (Binary Phase Shift Keying) navigation signals in mutli-frequency receivers and establishes a basic jitter budget. [19] expands [18] to QPSK (Quadrature Phase Shift Keying) and BOC (Binary Offset Carrier)(n,n) signals, showing that the noise due to jitter is the same for QPSK as for BPSK. A last example is [20], which provides jitter effect measurements on the value of the correlation peak

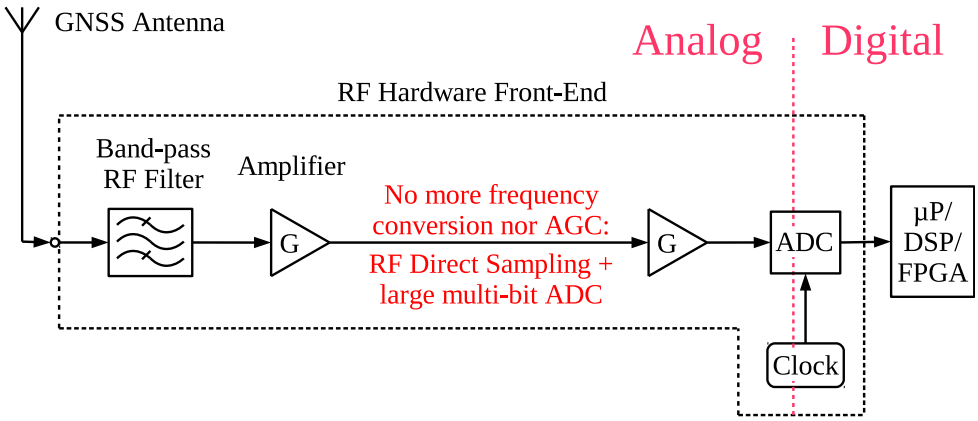

Figure 1.4: RF DS SDR GNSS receiver.

and on the *C/N0* measurement and position accuracy in a RF-DS-SDR real-time GPS L1 receiver. The modelisation of the sampling jitter, its effect on the sampled signals and more generally its impact on the navigation function appear to be also an important research topic.

1.1.3 Removal of the Analog AGC

Finally the analog AGC (Automatic Gain Control) will give way to a digital one i.e. a large multi-bit ADC in light of the upcoming availability of a sufficient number of quantification bits required to linearly quantize the full range of input signal. The need of a variable gain amplifier associated to a control loop will be removed. The RF-DS-SDR GNSS receiver seems to be in view: an antenna, an ADC and a processor, as represented in figure 1.4.

1.1.4 Applicability to Civil Aviation Receivers

Little work has been done to determine if this RF-DS-SDR architecture could apply to GNSS receivers intended for Civil Aviation. In principle the attractive advantages listed could benefit to this kind of receivers application. However, in a field where safety is a priority, prior to use of this new concept, it must be shown that it is compatible with the requirements found in Civil Aviation standardization documents such as, for instance, the Galileo [21] and GPS [22], [23] or [24] MOPS (Minimum Operational Performance Specification) documents.

Independently of the navigation function, as its name suggests, a *Software* Defined Radio GNSS receiver makes extensive use of software processing. It must then be certified according to the Software Considera-

tions in Airborne Systems and Equipment Certification document [25], DO-178 for short. This requires much effort from the manufacturer and it is then an important task to consider in a more general approach of the design of a SDR GNSS receiver for Civil Aviation. Nevertheless, this certification is out of the scope of this thesis and so it will not be considered anymore in this document from now on. However, this point should not be forgotten in a larger context.

1.2 Objectives

It is the objective of this thesis to assess the feasibility of a DS-DF (Dual-Frequency)-SDR Galileo receiver for Civil Aviation and, if possible, to convert the requirements found in the dedicated standards such as [21] into design guidelines.

The reason it was decided to focus on the Galileo constellation is mainly due to the current lack of GPS L5 standard for Civil Aviation receivers while there currently exists an interim version of a MOPS document for a Galileo E1/E5 receiver [21]. It is however anticipated that the analysis presented here will be applicable to future GPS/Galileo E1/L1 and E5a/L5 receivers due to the similarity of these constellations and signals and the commonality of their interference environment.

The targeted context of this thesis being post-2020, where the dual-frequency/multi-constellation GNSS SBAS (Satellite-Based Augmentation System), the multi-frequency/multi-constellation GNSS ARAIM (Advanced Receiver Autonomous Integrity Monitoring System) and potentially the multi-frequency/multi-constellation GNSS GBAS (Ground-Based Augmentation System) will be implemented, the receiver architecture to be designed was naturally dual-frequency and possibly multi-constellation.

To complete this objective, a RF design was conducted from the antenna to the processor with the ideal schematic identified in figure 1.4 on one hand and with the requirements on the other. However, if a real receiver must verify all requirements, this work only addresses the requirements that could be affected by the differences between classical architectures and the RF-DS-DF-SDR design. Indeed, as classical architectures find the ways to be compliant with all requirements, a RF-DS-DF-SDR receiver could use the same solutions, except where it is specifically different.

1.3 Thesis Contribution

The major contributions of this work relate to each major step of the RF-DS-DF-SDR GNSS receiver design. They are summarized below but will be developed all along this document:

- Proposition of two architectures, refined from figure 1.4 to cope with Civil Aviation requirements. The first one allows coherent sampling of both E1 and E5a bands. It requires extra RF filters which are specified. The possible sampling frequencies are also calculated, with a minimum of $F_s = 88.08\,\text{MS/s}$ for extra RF filters meeting their specifications. The second architecture provides Separate Sampling of the E1 and E5a bands. Extra RF filters are also needed and they are specified. The possible sampling frequencies are calculated again, with a minimum of $F_s = 40.22\,\text{MS/s}$ for the E5a band, and $F_s = 40.14\,\text{MS/s}$ for the E1 band, for extra RF filters meeting their specifications,

- Implementation and test of the E1 RF filter required by both architectures to meet the specifications about interference robustness. It is shown that the required extra RF filter is feasible: the minimum required attenuation could be verified nearly everywhere in frequency, even if the behavior in temperature should receive special attention. The group delay variations seem contained in acceptable limits also,

- Analysis of the impact of the sampling jitter on the PLL (Phase-Locked Loop). A model of the sampling clock jitter is built, as a function of the constant c, the parameter which characterizes the quality of the sampling clock. Using the model, simulations are conducted. In light of the simulation results, a limit is set to the value of c to maintain the effect of the sampling clock jitter to an acceptable level. This acceptable level is defined to be 10 dB down from the thermal noise power, for $C/N0_{ref} = 43\,\text{dBHz}$. The limit value of c is found equal to $10^{-20}\,\text{s}$,

- Specification of the quantization operation. It is shown that N, the number of bits required to quantize the whole range of the signal present at the input of the ADC(s), greatly depends on the performance of the required extra RF filters, whether it be for the Separate Sampling architecture or for the Coherent Sampling one. Considering Separate Sampling, up to $N = 20$ bits could be required for the E5a band and up to $N = 18$ bits for the E1 band, in the case of poor quality extra filters. For Coherent Sampling,

the results are similar, up to $N = 20$ bits could be necessary if the extra filters are far from meeting their specifications,

- Evaluation of methods to reduce the binary throughput immediately after the ADC, to lower the workload of signal processing tasks, preserving the signal fidelity for this civil application. In particular, two non-linear functions are tested. The results demonstrate they are not efficient, showing that unless a function with better performance is found, dynamic compression is not a decisive technique to decrease the binary throughput after the ADC(s).

The publications made during this PhD and corresponding to some of these contributions are the following:

- "Digitization Guidelines for a Direct Sampling Dual-Band GNSS Receiver for Civil Aviation", in the proceedings of the ENC (European Navigation Conference) 2011 [26].
- "Effect of Sampling Jitter on Signal Tracking in a Direct Sampling Dual Band GNSS Receiver for Civil Aviation", in the proceedings of the ENC 2012 [27].
- "Matched Quantization and Band Separation in a Direct Sampling Dual Band GNSS Receiver for Civil Aviation", in the proceedings of the ION (Institute Of Navigation) conference GNSS+ 2013 [28].

1.4 Thesis Organization

The dissertation architecture is as follows.

Chapter 2 presents the design constraints specific to Civil Aviation GNSS receivers, focusing on requirements regarding robustness against interference. Interference masks at the antenna port specified in the interim Galileo MOPS document are displayed. They define the maximal power of the interfering signals below which all the minimum performance requirements must be met.

In chapter 3, two Direct Sampling architectures are elaborated from these masks, identifying the essential minimal RF hardware elements. The minimum values of sampling frequencies are also calculated. The two architectures use extra RF filters compared to the simplified design of figure 1.4. They are mandatory to meet the interference threat specific to the Civil Aviation environment.

Then chapter 4 investigates the feasibility of these supplementary filters through prototyping on the E1 band. This work was needed because

of the high performance required from this filters. The possible variation of the transfer function across a range of temperature corresponding to Civil Aviation specifications was tested.

The phenomenon of sampling jitter is presented in chapter 5. Indeed, as the navigation signal carrier frequencies are high at the input of the ADC due to the lack of IF or DC conversion stages, the influence of sampling jitter on signal tracking can not be neglected as in classical architecture so it is assessed in this chapter through simulations.

Then the calculation of the number of quantization bits required to linearly quantize the input signal over the range defined in chapter 2 is made in chapter 6, taking into account the dynamic of interference signals.

In connection with the results produced in chapter 6, methods to minimize the bit rate immediately after the ADC are then evaluated in chapter 7. In particular the use of non-linear functions to compress the dynamic at the output of the quantizer are investigated.

Chapter 8 is focused on the digital separation of the two useful bands, E5a and E1, sampled at the same time in the Coherent Sampling architecture. Each band needs to be isolated by filtering prior to independent signal demodulation.

The conclusions summarize the two proposed architectures that could be used to design a RF-DS-DF-SDR GNSS receiver for Civil Aviation and recalls the main results to be kept in mind to reach the minimum requirements imposed by safety authorities through MOPS documents. Finally proposals for future complementary works are made.

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2 The Specific Design Constraints

This chapter investigates the requirements applicable in the design of a DS-DF-SDR GNSS receiver for Civil Aviation in comparison to classical architectures.

2.1 The Interim Galileo MOPS Document

To be used aboard a civil aircraft, a GNSS receiver must be certified, so that at the minimum it must be compliant with the requirements and test procedures found in the applicable standards [1], [2] or [3]. Similarly the associated antenna must verify the minimum specifications described in [4] and [5] can it be passive, or [6] can it be active.

However, these documents only deal with the GPS L1 frequency band (at the exception of [4] which scope is extended to the GLONASS operating frequencies as an option).

Indeed a designer interested in developing a preliminary dual-frequency E1/E5a receiver has no other choice for the moment than to rely on the interim [1] Galileo MOPS [7] document edited by EUROCAE. This is why [7] is our reference document from now on.

Of course [7] proposes specifications for a Galileo receiver only. However, as the E1/E5a and L1/L5 frequency bands are respectively equal and as the overall navigation function is the same, it can be supposed that the final requirements for each kind of receiver will be similar enough so

1. Since the beginning of this thesis, other versions of this document were issued. Nevertheless, it was decided to set [7] as the reference and not to follow the newer versions as otherwise the base of this work would have change continuously. Future work should recheck the results obtained during this thesis with the up-to-date version of the MOPS document.

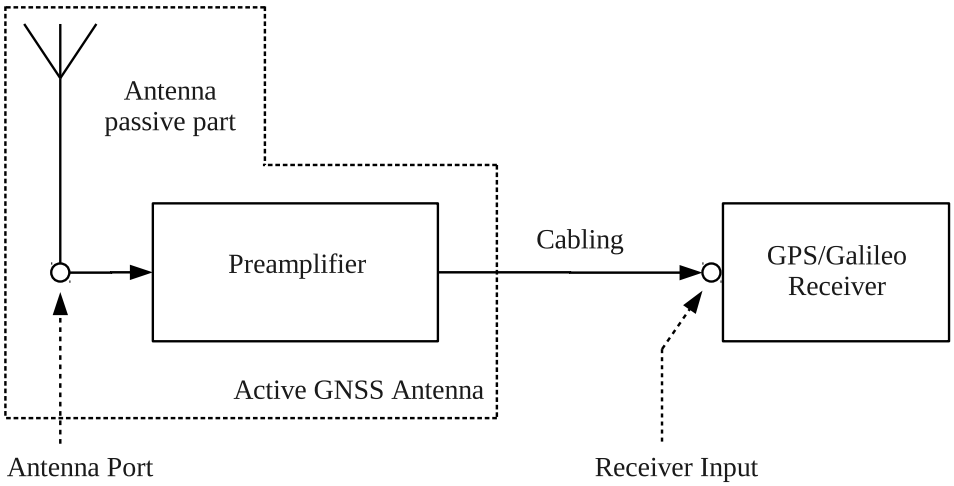

Figure 2.1: Receiver ports definition [7].

that the results obtained during this PhD will be reasonably applicable to a L1/L5 GPS receiver.

At this point it must be noted that the interim Galileo MOPS document not only expresses requirements about the receiver itself but also sets the minimum specifications of the active antenna to be used with [2]. Indeed the antenna/receiver configuration considered in the interim Galileo MOPS document is represented in figure 2.1, illustration which also gives a graphical definition of the antenna port and of the receiver input, two boundary points that will be referred to later in this document.

Taking into account this configuration with an active antenna, the classical GNSS receiver architectures for Civil Aviation can then be refined from figures 1.1 and 1.2 into figures 2.2 and 2.3 [3] respectively. In

2. The specifications of the active antenna are no more in the Galileo MOPS document at the time of this writing. A specific MOPS document is now dedicated to the active antenna.

3. In the architecture with DC, the leakage of the local oscillator through the mixers induce a DC (Direct Current) offset in the baseband. In GNSS receivers, to be able to correctly demodulate the navigation signals, this DC offset must be removed by a notch filter as explained in [8]. This notch filter creates group delay variations in the useful signal band. This is a problem for some Civil Aviation applications, for example GPS/SBAS navigation. The receivers designed to provide this function must meet the requirements found in the GPS MOPS document [3] which specifies less than 150 ns differential group delay variation in the pre-correlation filters. This is a value which may be difficult to achieve with a notch filter in the signal path. It means that no valid implementation of the architecture represented in figure 2.3 may be build for this kind of Civil Aviation GNSS receiver.

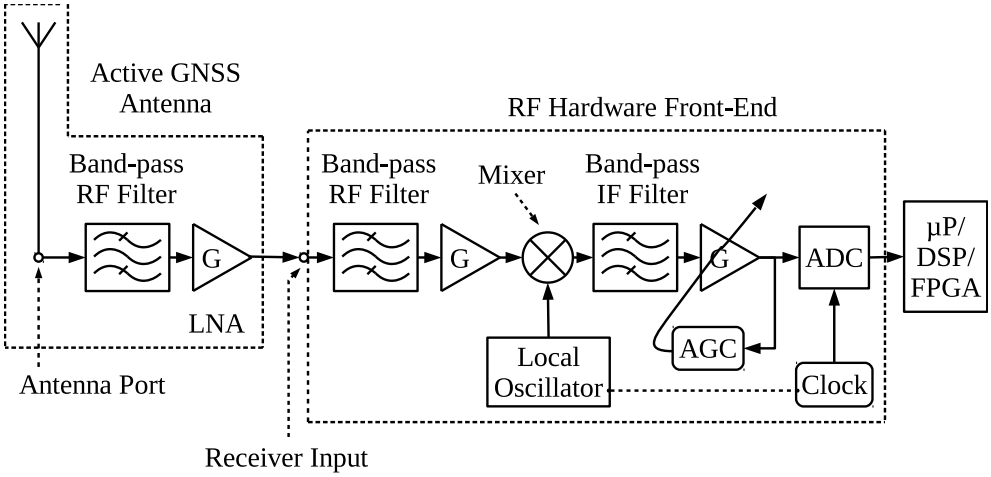

Figure 2.2: Architecture of a Galileo receiver for Civil Aviation, with Intermediate Frequency.

the same way figure 1.4 representing the RF-DS-DF-SDR Galileo receiver architecture turn into the one represented in figure 2.4.

2.2 Comparison with the Classical GNSS Receivers

The standards are written "for equipment manufacturers to design receivers compliant with safety performance requirements established by the civil aviation community" [7]. They are also designed with the existing technical possibilities in mind: a standard setting a level of safety unreachable with the current time or near future technology is useless.

That is why it is interesting to compare the classical GNSS receiver architectures represented in figure 2.2 or in figure 2.3, on which the standard is based, to the Direct Sampling SDR architecture which is envisaged, illustrated in figure 2.4. In the differences lie the points which must be focused on in applying the standard to a RF-DS-DF-SDR Galileo receiver. The common features can be skipped in this study of feasibility, as explained in section 1.2 of the introduction 1.

2.2.1 Absence of Analog Frequency Down-Conversion

In a classical receiver the analog frequency down conversion stage(s) is(are) performed to improve the selectivity, that is to reject the undesired signals picked up by the antenna through selective filtering. Indeed, it is easier to implement bandpass filters with a set bandwidth at a lower IF than directly around the carrier frequency, as the Q factor of the involved

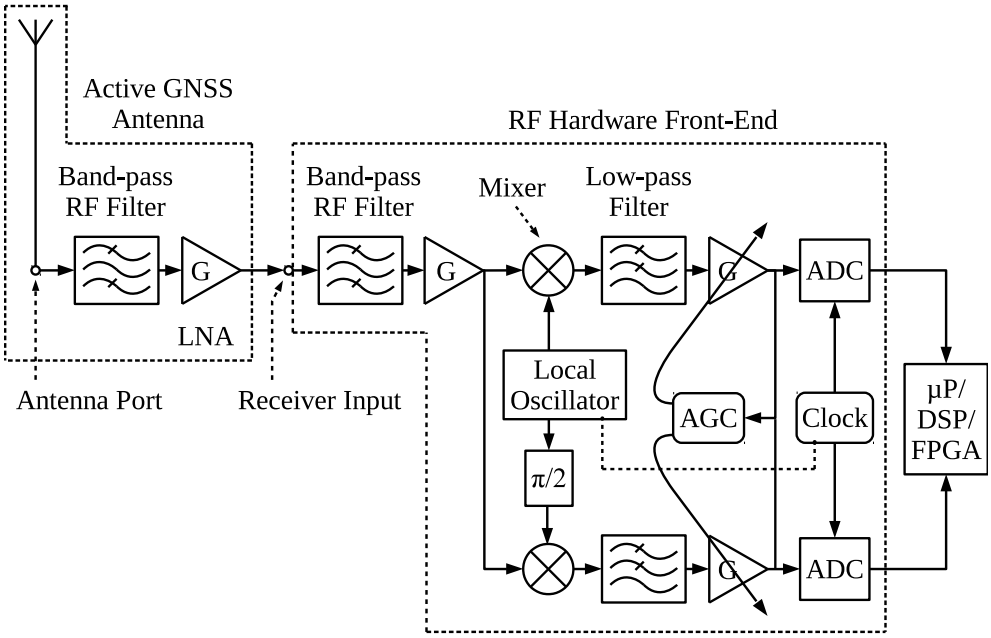

Figure 2.3: Architecture of a Direct Conversion Galileo receiver for Civil Aviation.

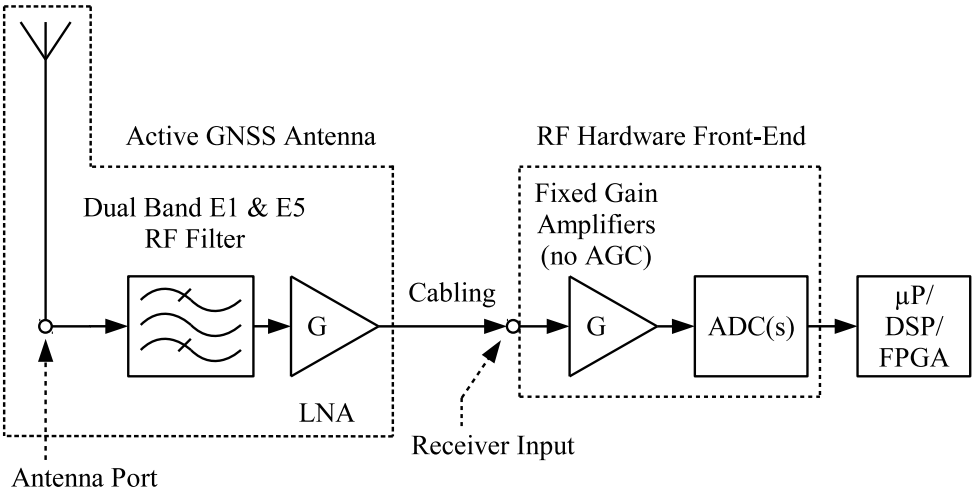

Figure 2.4: RF-DS-DF-SDR Galileo receiver architecture for Civil Aviation.

components decreases with frequency. Consequently, due to predictable difficulty to implement highly selective filters directly around the carrier frequencies, a DS receiver of the kind represented in figure 2.4 must be supposed less robust than classical architectures to out-of-band interferences. So, a first requirement which must be specifically addressed is related to the *Interference environment*.

With RF-DS, the carrier frequency of the signal at the input of the ADC is also much higher than in the classical frequency down-conversion receiver. Thus, the sampling jitter effects, which are usually neglected in the classical architectures, must be characterized even if there is no direct requirement about it in the standard. It should be checked, for example, that the sampling jitter effects do not produce excess pseudorange measurement error in a RF-DS-DF-SDR Galileo receiver in comparison to the 5 m (RMS) bound specified in [7]. “” A third requirement which could be affected is *Demodulation of data and message decoding*: as the useful signal is distorted by the sampling jitter, the phase measurement, in particular, is disturbed and then the demodulation of data is altered.

2.2.2 Absence of AGC

The AGC is used traditionally to adjust in real time the signal amplitude at the input of the ADC to utilize the full quantization scale of the ADC. In this way, the quantization noise is minimized for a set number of quantization bits.

In a GNSS receiver the signal amplitude at the input of the AGC can vary:

- dynamically due to variations in the receiving conditions (presence of interference for example) or in the state of the equipment (modification of the operating temperature).
- statically because of the various installation parameters as the effective antenna gain and cable losses, which differ from aircraft to aircraft.

What is more, the AGC can be used to detect and mitigate some kinds of interference (especially CW (Carrier Wave)). Detection can be performed through monitoring of the loop control voltage variations as explained in [9] or more recently in [10] for instance. Mitigation can take several forms, like digital pulse blanking [9] or minimization of the THD (Total Harmonic Distortion) of the digitized signal [10] (but at the cost of supplementary signal post processing to remove the remaining CW).

In a receiver without AGC, the design of the ADC must then cope with the full range of the input signal (in particular it has to handle

interference power levels up to the maximum level, as will be further elaborated on next). So it has to encompass not only the full interval of the dynamic variations of the signal but also the full range of the antenna gain and cable losses, in order to not require adjustments during installation. In short it must be *aircraft installation independent*. Obviously the final number of quantization bits in this case will be higher than with an AGC.

Thus the requirements of concern here are *Sensitivity and dynamic range*, *Interference environment* again and *Active Antenna Requirements*.

2.3 Interference Environment

Figure 2.5 is a graphical representation of both CW/NB (Narrow Band) and Pulsed interference masks at the antenna port (see figure 2.1) specified in [7]. These masks define the maximal power of the interfering signals below which all the minimum performance required for the receiver shall be achieved. Figure 2.5 concerns the following types of interference

- CW, that is a pure sine wave function,
- NBI (Narrow Band Interference), considered as a Gaussian noise with a rectangular spectral shape with a double sided bandwidth noted BW around a central frequency,
- DME (Distance Measuring Equipment) pulse emitted by the on-board DME transponder and received by the on-board GNSS antenna,
- pulsed interference in $[1555.42, 1595.42]$ MHz, defined by a rectangular pulse width of 125 µs, a bandwidth of 1 MHz and a duty cycle of 1%,
- pulsed interference in $[1315, 1555.42]$ MHz and in $[1595.42, 2000]$ MHz, defined by a pulse width of up to 1 ms, a peak power of 20 dBm and a duty cycle of 10%,
- composite ground DME signal, which is the aggregation of ground DME signals received by the on-board GNSS antenna. The European hotspot is a place in the European sky where the received power of this aggregation is maximum. At the hotspot, the maximum peak power of the received composite ground DME signal can reach -60 dBm, a value calculated by simulation from the interim Galileo MOPS document [7].

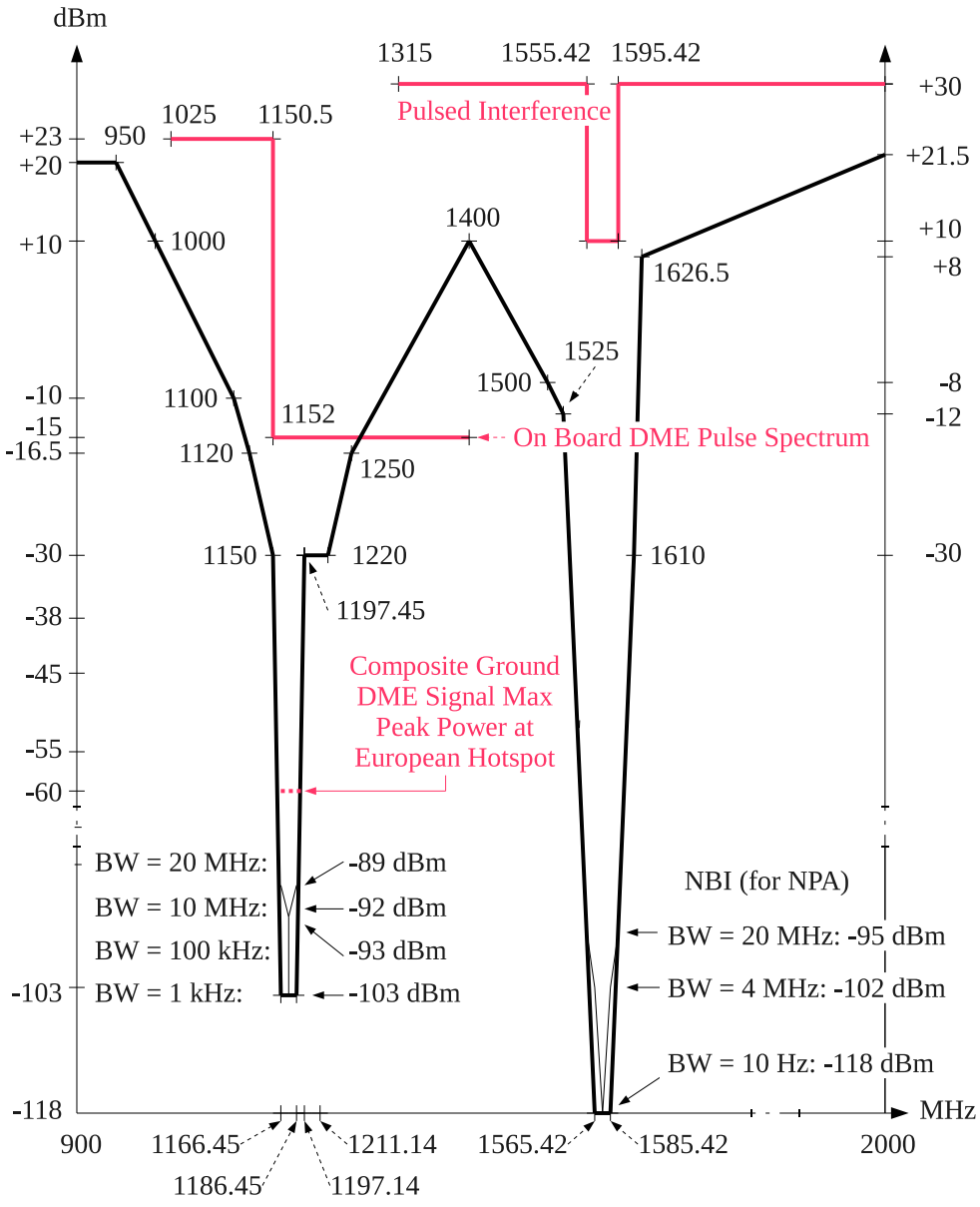

Figure 2.5: Interference masks at antenna port [7].

The high dynamic range, from +30 dBm to −118 dBm, that the receiver has to sustain can immediately be noted. It should also be pointed out that the two bands $[f_{5min}, f_{5max}] = [1166.45, 1186.45]$ MHz and $[f_{1min}, f_{1max}] = [1565.42, 1585.42]$ MHz are considered as the most sensitive parts of the spectrum. As such it is proposed to set the useful E5a and E1 bands to $[1166.45, 1186.45]$ MHz and $[1565.42, 1585.42]$ MHz respectively, because they are not explicitly specified in [7]. The useful (3 dB) bandwidths $B_{5a} = (f_{5max} - f_{5min}) = 20$ MHz and $B_1 = (f_{1max} - f_{1min}) = 20$ MHz can also be defined.

2.4 Sensitivity and Dynamic Range

2.4.1 Galileo Signal levels

The interim Galileo MOPS document [7] relates to the Galileo OS (Open Service) SIS (Signal In Space) ICD (Interface Control Document) [11] for the range of the E1/E5a signal levels the receiver shall acquire and track:

- "The minimum received power on ground is measured at the output of an ideally matched RHCP (Right Hand Circular Polarization) 0 dBi polarized user receiving antenna when the SV (Space Vehicle) elevation angle is higher than 10 degrees" is −155 dBW for E5a and −157 dBW for E1.

- "The (...) maximum received signal power level is, using the same assumptions as for the minimum received power, not expected to exceed 3 dB above the corresponding minimum received power".

Concerning the maximum power level, the interim Galileo MOPS document [7] explicitly takes a margin compared to the Galileo OS SIS ICD: "the receiver shall assume that the maximum power will be 7 dB or less above the corresponding minimum power". This for E1 and E5a. It is the value the designer must consider.

Last but not least regarding navigation signals, [7] also makes the assumption in *RNSS noise* that the equivalent noise represented by other GNSS signals is "low enough compared to other contributing noise and interferences sources" so that it can be ignored [4] in both E1 and E5 bands in the antenna – receiver link budget.

4. However, in [12] and in the latest versions of [7] RNSS (Radio Navigation Satellite Service) noise is no more considered to be negligible and should be included in the link budget.

2.4.2 Noise Level

The interim Galileo MOPS document [7] makes some assumptions about the thermal noise level in *Appendix F GALILEO Signals susceptibility to CW/NBI Radio Frequency Interference*:

- the equivalent temperature of the noise at the antenna input is set to 100 K,
- $T_0 = 290$ K is the standard temperature,
- the actual cable temperature is set to T_0.

Associated with the interference environment illustrated previously, these OS Galileo signals and noise level specifications define the complete dynamic range which should be taken into account at the antenna port during normal operation.

2.5 Active Antenna

As pointed out previously in this chapter, [7] also specifies the requirements for the active antenna to be used on board.

In particular, figure 2.6 illustrates the minimum frequency selectivity required in both E5 and E1 bands.

The preamplifier gain interval is also set to $[26.5, 32.5]$ dB and its maximum noise figure is specified to 4 dB.

At last, not really part of the active antenna but directly related and then specified in the same appendix, the cable loss is supposed to range from 3 to 12 dB maximum.

2.6 CW Interference Masks at Receiver Input

Applying the minimum preamplifier selectivity curve in figure 2.6 to the mask shown in figure 2.5, it is possible to deduce the maximum interference levels at the receiver input, if the input interference is at the mask level, as drawn in figure 2.7. Only the CW masks and the composite ground DME signal max peak power level at the European hotspot remain.

NBI mask is not represented any more because:

- in the E5a band it is exceeded by the composite ground DME signal max peak power at the European hotspot,

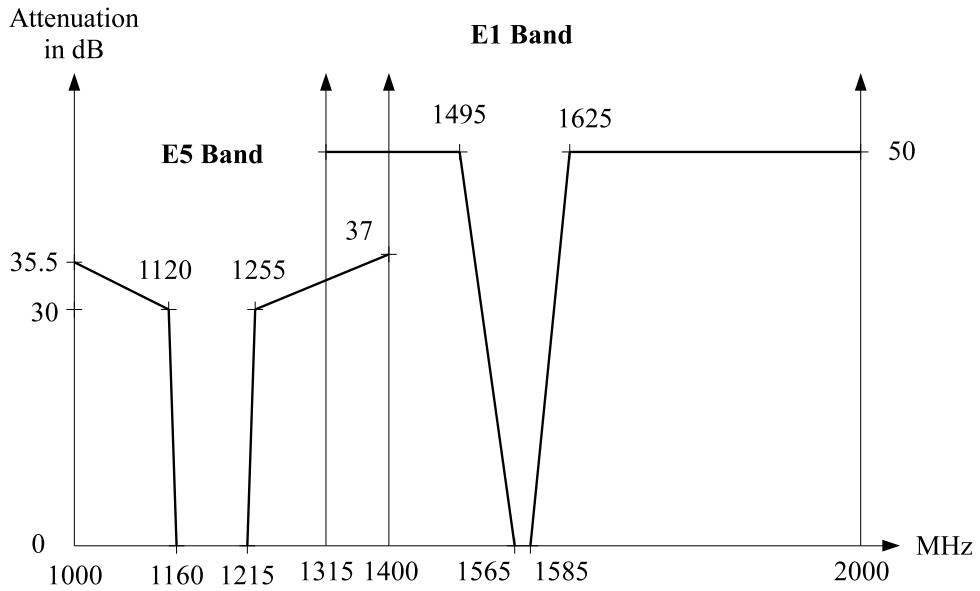

Figure 2.6: Active antenna minimum selectivity [7].

- in the E1 band, when the -95 dBm maximum power (defined for an interference bandwidth equal to 20 MHz) is spread over this 20 MHz bandwidth, it goes down to -168 dBm/Hz, much less than the CW mask. The calculation leading to this result is based on the assumption made in [7], and recalled in section 2.3, that NBI has a rectangular spectral shape with a double sided bandwidth noted BW around a central frequency, so that the PSD (Power Spectral Density) corresponding to a power of P dBm is equal to $P - 10\log_{10}(\text{BW})$ in dBm/Hz.

The on-board DME pulse mask is also not present for different reasons:

- in the $[1025, 1235]$ MHz frequency interval, the mask is above the 1 dB compression point of the preamplifier specified in [7]. It means that an interference at this level causes the saturation of the preamplifier with unpredictable spectral effects. This is true also for classical receiver architectures, where it gets no special processing. So it is proposed to ignore this spectral content in the design of the RF hardware front-end,

- in the $[1235, 1258.49]$ MHz frequency interval, the mask is under the 1 dB compression point of the preamplifier and above the CW mask. However, knowing that the duty cycle of the DME pulse

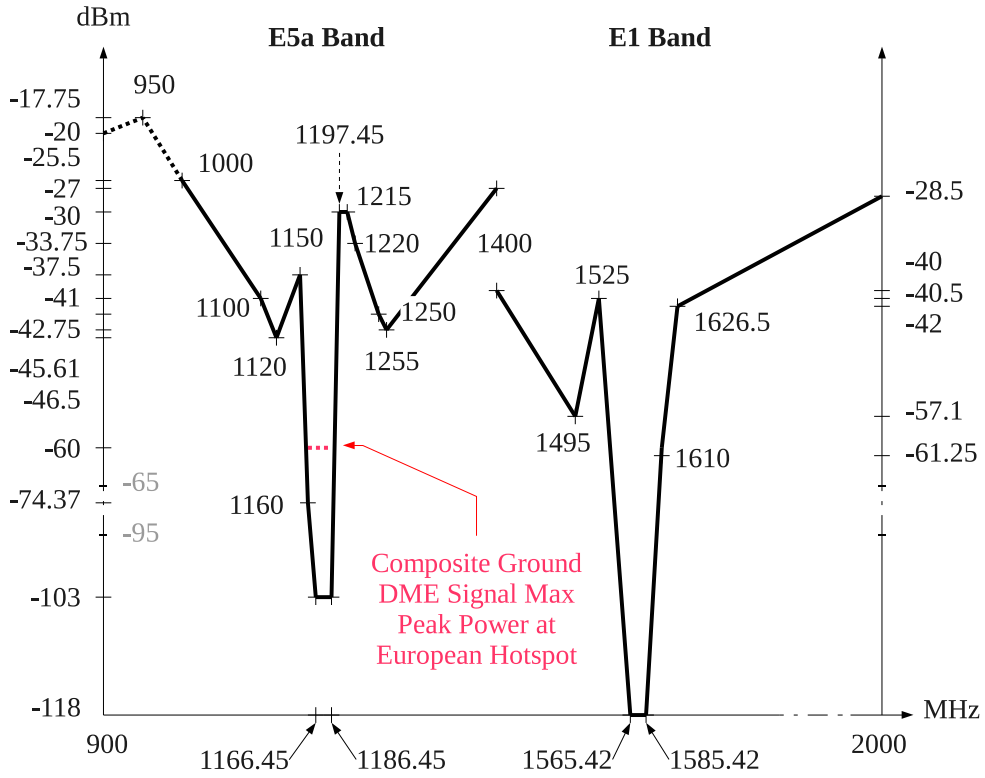

Figure 2.7: Interference mask at receiver input.

threat is less than 0.04% in this interval (a rate of 48 pulse pairs per second for a pulse width of 3.5 µs) and that the on-board DME pulse mask is at most 8.25 dB above the CW mask, it was considered as a weaker issue than the CW mask in this interval. So it is not depicted,

- in the $[1258.49, 1400]$ MHz frequency interval, the on-board DME pulse mask is under the CW mask so it is not drawn.

The pulsed interference mask in the $[1315, 2000]$ MHz frequency interval is not represented as it is also above the 1 dB compression point of the preamplifier and for this reason leads to the same conclusion as for the on-board DME pulse mask in the $[1025, 1235]$ MHz frequency interval.

2.7 Conclusion

In this chapter the differences between classical architectures and a DS-DF-SDR Galileo receiver were listed and their implications explained.

It appeared in particular that the Direct Sampling receiver is a priori less robust to interference than its competitors. As a consequence the interference environment at the receiver input was identified as especially important and so it was deduced from the requirements.

It is represented in figure 2.7. This is the maximum spectral content to be considered at the input of the RF front end of the RF-DS-DF-SDR Galileo receiver architecture represented in figure 2.4. As such it is the starting point of our design process.

2.8 References

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3 Sampling

This chapter deals with the architectures to be implemented in order to sample the Galileo GNSS E1 and E5a signals without degradation of the performance of subsequent processing to retrieve the information they carry. A special attention must be paid to the interference threat presented in chapter 2 and summarized in figure 2.7. In fact, due to its primary importance in Civil Aviation, it is the spectral basis which conditions the sampling approach and leads the design in this chapter. Once the architectures laid down, the sampling frequencies, which should be the lowest possible in order to decrease to a minimum the workload downstream, will be calculated.

3.1 Sampling Strategy

The challenge in sampling multiple bands is to sample the input signals without worsening the interference threat over the E1 and E5a bands, because of aliasing, compared to a traditional receiver. Indeed there is no requirement for current Civil Aviation receivers to provide measurements within specifications in the presence of interference levels higher than the mask specified in-band, provided integrity is ensured. That is to say that, unless demodulation techniques better than the ones used in traditional receivers are found, no increase of the in-band interference levels due to sampling is allowed. As ideal sampling is equivalent to periodic spectral aliasing, it means that no in-band folding of figure 2.7 can be tolerated.

At this point of the study, it can be concluded graphically that a unique solution is to directly digitize the whole $[1166.45, 1585.42]$ MHz

passband as a unique block with no aliasing. This can be realized in two ways:

- by sampling the $[0, 1585.42]$ MHz baseband according to the original Shannon theorem. This leads to a minimum sampling frequency $F_s = 2 \times 1585.42 = 3170.84\,\text{MS/s}$,

- by bandpass sampling the $[1166.45, 1585.42]\,\text{MHz}$ passband as theorized in [1] [1]. The principle of uniform bandpass sampling can be found in appendix A. This gives a quite lower $F_s \in [1056.95, 1166.45]\,\text{MS/s}$ or $[1585.42, 2332.90]\,\text{MS/s}$.

It should be noted that, for the moment, without pre filtering it is not possible to use the concept of bandpass sampling the two bands, based on their respective bandwidth, where both bands are aliased, such that they do not overlap. This technique is presented for GNSS receivers in [3] for a GPS L1 and GLONASS receiver, in [4] for a GPS L1 and L3 receiver, in [5] for a GPS L1 and L2 receiver or in [6] for a GPS L1 and L2 receiver for example. Without modification this technique would cause in-band injection of out-of-band interference levels higher than in-bands floors. The interference threat must be first filtered, before sampling, as it is detailed hereafter.

These values of F_s are of little interest compared to classical architectures at the present time or in the near future, due to the out of reach induced processing workload downstream. Without modification the scheme 2.4 reaches a deadlock. Obviously, if a lower sampling frequency is desired, some extra filtering is needed in order to be able to fold filtered part of the spectrum over the E1 and E5a bands without damage during bandpass sampling. This conclusion leads us to propose two new architectures for our DS-DF-SDR Galileo Receiver for Civil Aviation. In the first one the E5a and E1 bands are sampled coherently (with a single ADC) while this is done separately (with an ADC dedicated to each band) in the second one. Both architectures are detailed in the following of this chapter.

1. Although it is established in [2] that the minimum required global sampling frequency is less for quadrature bandpass sampling than for uniform bandpass sampling, only uniform sampling will be considered in the rest of this thesis. This decision was taken because quadrature sampling, in comparison to uniform sampling, requires not only two ADCs for each signal to digitize but also two different sampling clocks shifted by $f_c/4$, where f_c is the carrier frequency ($f_c = 1176.45\,\text{MHz}$ for the E5a signals and $f_c = 1575.42\,\text{MHz}$ for the E1 signals). These two hardware supplementary requirements make in contrast uniform sampling a wiser choice from the engineering point of view.

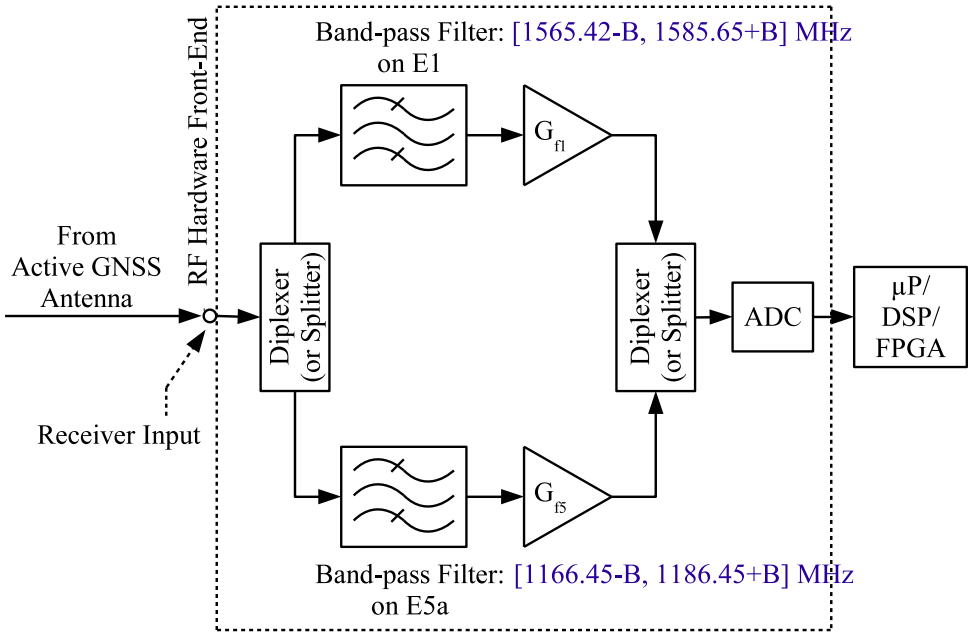

Figure 3.1: Coherent Direct Sampling.

3.2 Coherent Sampling

In this first architecture, sketched in figure 3.1, both bands are digitized at the same time because only one ADC is used. This provides a perfect coherency between the two, as long as the differences in their different RF paths are known and compensated. In particular the sampling jitter is the same on each band.

In this design, the signal received from the active GNSS antenna is first of all split into two paths by either a diplexer or a power splitter [2]. Then, in order to allow as much aliasing as possible to reduce the sampling frequency, RF filters are inserted in each branch which will lower out-of-band mask levels injected in-band below in-band mask levels. Furthermore, out-of-band max levels should be reduced under the lowest in-band mask level, that is -118 dBm as visible in figure 2.7, corresponding to the E1 band max tolerable level. Immediately following the RF filters, fixed gain amplifiers are installed to adapt the level of the signals to the input range of the ADC. Finally, just before digitization, the two separate

2. A diplexer should be used preferably because it provides filtering and adds low loss in the signal path. However, if a cheaper solution is preferred, a power splitter could also be used, at a cost of a loss of 3 dB in the signal path and no filtering capabilities.

signals are mixed back together using here again a diplexer preferably, a power splitter being also possible.

The need to mitigate the interference threat is materialized in this design by the insertion of a distinct filter in each branch. In practice, this filtering operation could be done elsewhere, for example in an improved active GNSS antenna, before the input diplexer or even distributed between the two. Nevertheless, as the requirements on this filtering operation will be clearly identified in the next section, it seems natural to model this operation as a separate filter. What is more, the need for these inserted RF filters is very specific to the Civil Aviation environment. Without the interference robustness requirements, they would be useless. That is the reason why, from now on, they will be noted "extra" RF filters, to emphasize the fact that they are added to satisfy some supplementary requirements in comparison to general purpose GNSS receivers. However this does not imply a final implementation as distinct filters.

3.2.1 Requirements on the Extra RF Filters

The maximum magnitude of the frequency response of the extra RF filters can be found in figure 3.3 [3]. The magnitude of the two transfer functions is drawn in the same figure to ease comparison between them but definitely refer to two distinct physical filters. The magnitude was calculated in this way:

- in-band it is set to 0 dB so that the useful signals are unaltered,
- out-of-band it is equal to −(mask level in figure 2.7) − 118 dBm − 10 dB margin. For instance, at 1100 MHz the CW mask level reaches −41 dBm, the required magnitude of the frequency response of the filter must then be lower than −87 dB so that the resulting mask level at the output of the filter is less than −118 dBm − 10 dB = 128 dBm.

The 10 dB margin calls for special explanation. Let $I_r = [900, 2000]$ MHz be the frequency interval on which the CW interference masks represented in figure 2.7 are defined and $B_r = 1100$ MHz its width. During sampling at F_s, due to periodic spectral aliasing, a frequency point in I_r will be "covered" by at most $n = \lfloor B_r/F_s \rfloor$ copies of other points in I_r. This mechanism is detailed in [1] in the special case of thermal noise, but the principle is the same whatever the nature of

3. The displayed magnitude was calculated without a possible contribution of the filtering capabilities of the diplexer(s), if used. Consequently it should be considered as a lower bound.

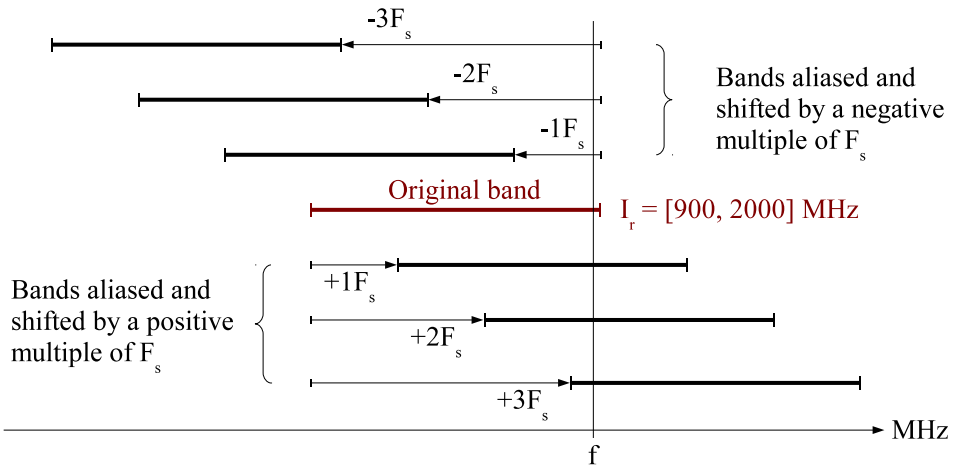

Figure 3.2: Superimposition of multiple spectral aliases at one frequency point.

signal. Figure 3.2 proposes an illustration for $n = 3$. Out-of-band power levels should not be attenuated to only $-118\,\text{dBm}$ then, but to at least $-118-10\log_{10}(n)\,\text{dBm}$. In this way the total contribution of out-of-band threat reinjected in-band by spectral aliasing will remain under the $-118\,\text{dBm}$ limit. An upper bound for n can be found by considering that the total bandwidth of the useful signals is $B_{5a} + B_1 = 40\,\text{MHz}$, which implies that $F_s \geq 80\,\text{MS/s}$ in accordance to the Shannon theorem. It gives $n \leq 13$ and $10\log_{10}(n) \leq 11.14\,\text{dB}$. The value of $10\,\text{dB}$ has been retained for sake of simplicity and considering that practical sampling frequencies will always be greater than $80\,\text{MS/s}$ as it will be shown in the following of this chapter.

3.2.2 Minimum Sampling Frequency

Applying the maximum magnitude of the frequency response of the extra RF filters presented in figure 3.3 to the CW interference mask of figure 2.7 at the receiver input gives the new maximum spectral content to be considered at the input of the ADC. It is drawn in figure 3.4.

It is now possible to calculate the sampling frequencies which allow the aliasing of the useful bands without overlapping for our Galileo receiver for Civil Aviation. The details are in appendix A. If the maximum magnitude of the frequency response of the extra filters could not be reached for some reason, the sampling frequencies were also calculated assuming a supplementary transition bandwidth B_s around each side of the useful bands, as represented in figure 3.5. Indeed, the calculations

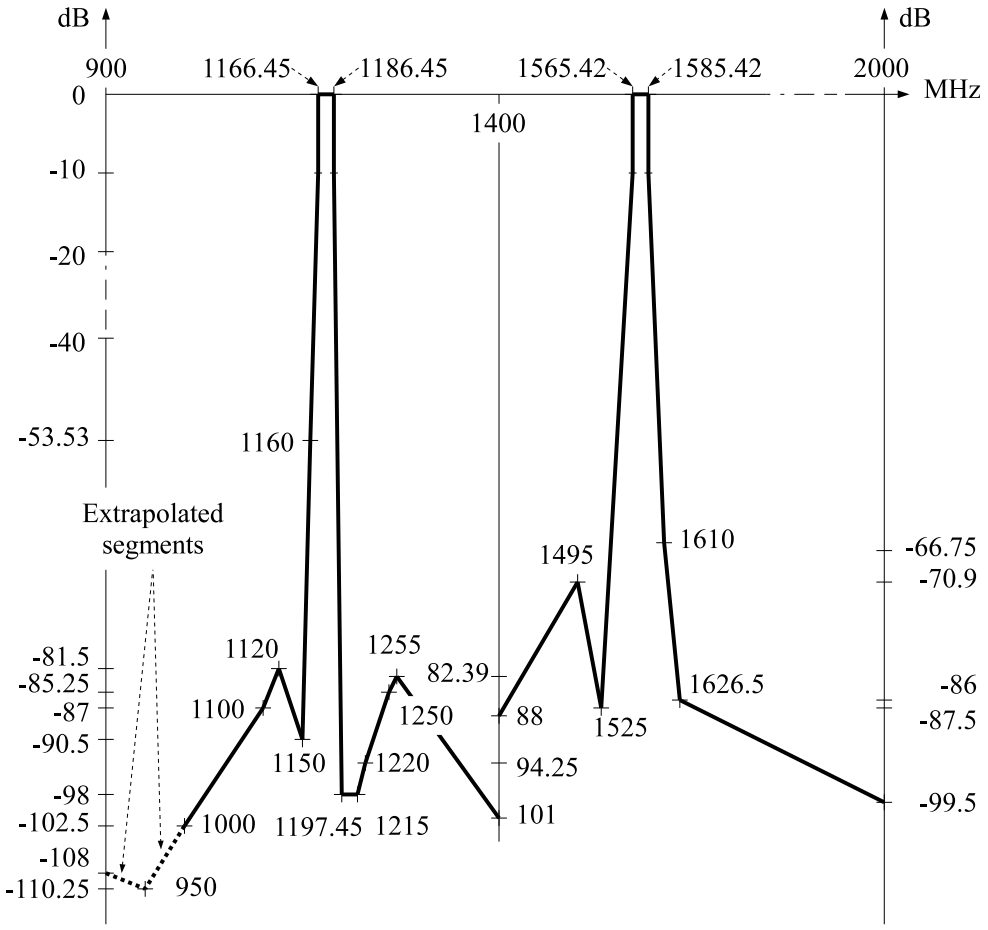

Figure 3.3: Maximum magnitude of the frequency response of the extra RF filters needed before Coherent Sampling.

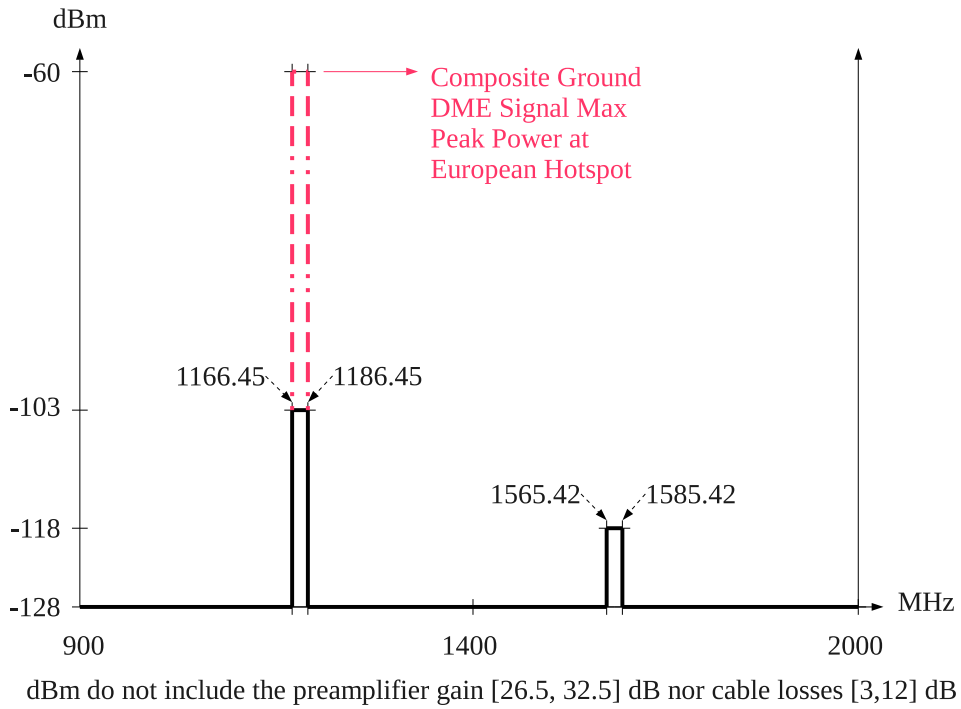

Figure 3.4: Maximum spectral content at the input of the ADC with Coherent Sampling.

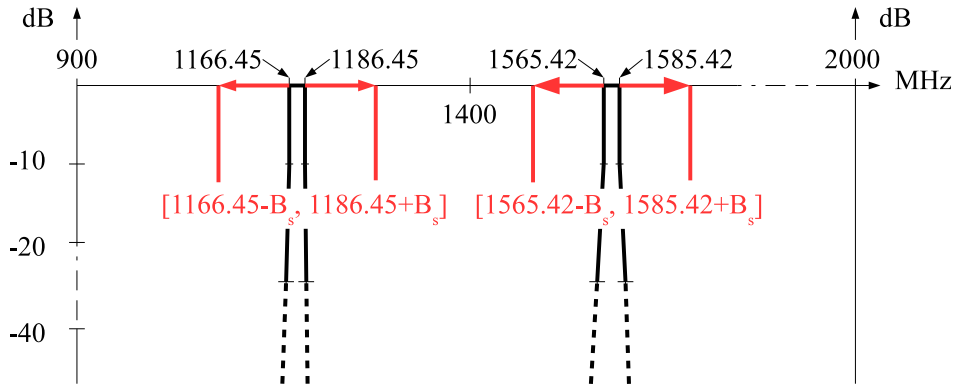

Figure 3.5: Supplementary transition bandwidth B_s around each side of the useful bands.

were conducted using $[f_{5min} - B_s, f_{5max} + B_s]$ and $[f_{1min} - B_s, f_{1max} + B_s]$ in the calculations instead of $[f_{5min}, f_{5max}]$ and $[f_{1min}, f_{1max}]$ strictly.

The results are presented in figure 3.6, in figure 3.7 and in figure 3.8. Figure 3.6 shows, as a function of the transition bandwidth B_s along the x axis, the intervals of possible sampling frequencies on the y axis. Their number and their length decrease with B_s as the solutions become more constrained with a larger spectral occupancy. More synthetic is figure 3.8, which shows only the minimum permitted sampling frequency as a function of B_s. Two bound values are of interest. The first, corresponding to $B_s = 0\,\text{MHz}$, is the minimum minimorum sampling frequency, 88.08 MS/s, which is approximately equal to twice the total bandwidth of the useful signals. The second is the maximum supplementary transition bandwidth, $B_s = 28\,\text{MHz}$, above which there is no sampling frequency which allows to bandpass sample the signals. There is clear evidence here that the narrower the extra RF filters, the lower the minimum required sampling frequency and hence the processing power required downstream. Thus there is an interest in designing filters with the smallest possible transition bandwidth B_s. It could be a challenging task as the quality factor of a filter with $B_s = 0\,\text{MHz}$ already reaches $Q = 1176.45/20 \geq 58$ for the E5a band, the one with the lowest center frequency. Chapter 4 is dedicated to the feasibility of these extra RF filters and presents a larger view on the subject.

The ladder diagram 3.9, introduced in [3], provides a different light on the specific case where the sampling frequency is at its lowest value, 88.08 MS/s, reached for $B_s = 0\,\text{MHz}$. The x-axis is for the sampling frequency, while the y-axis displays the E1 and E5a bands aliased in baseband. The red lines delimit a half period $[0, F_s/2]$ of the spectrum of the sampled signal, which is periodic in F_s. The ascending color strips are

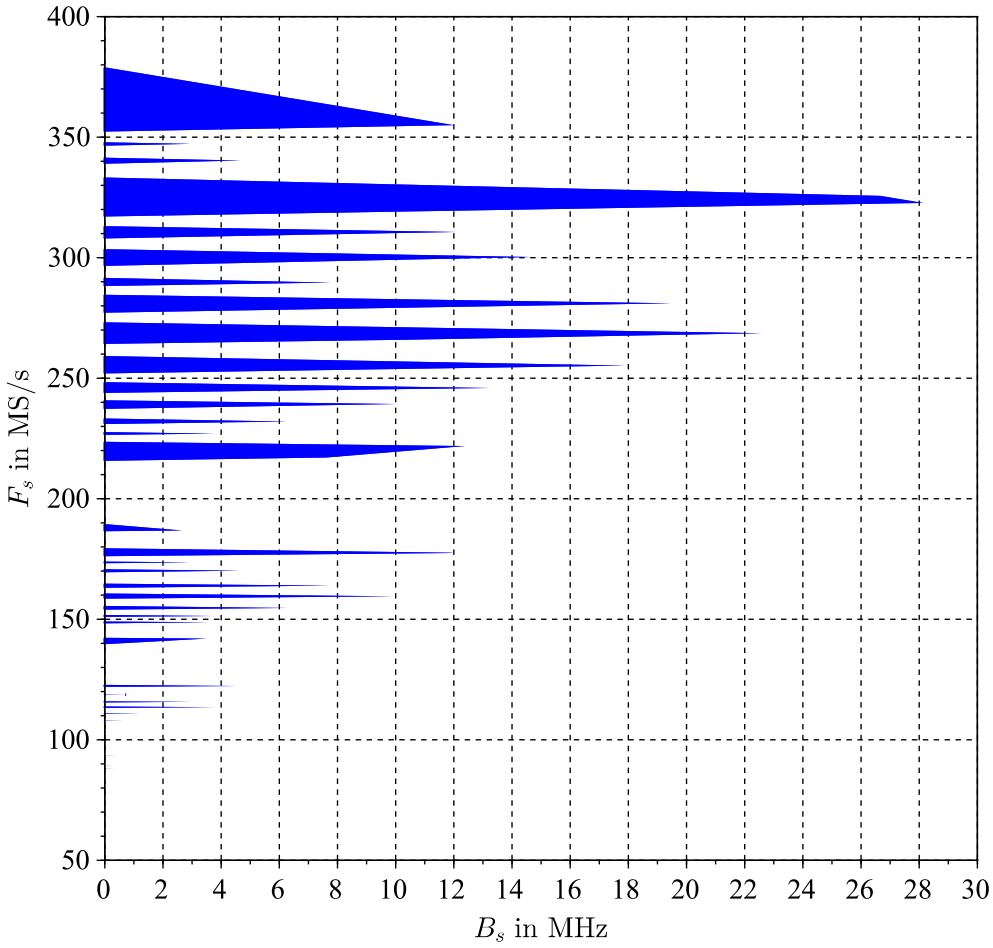

Figure 3.6: Coherent Sampling frequency intervals vs transition bandwidth B_s.

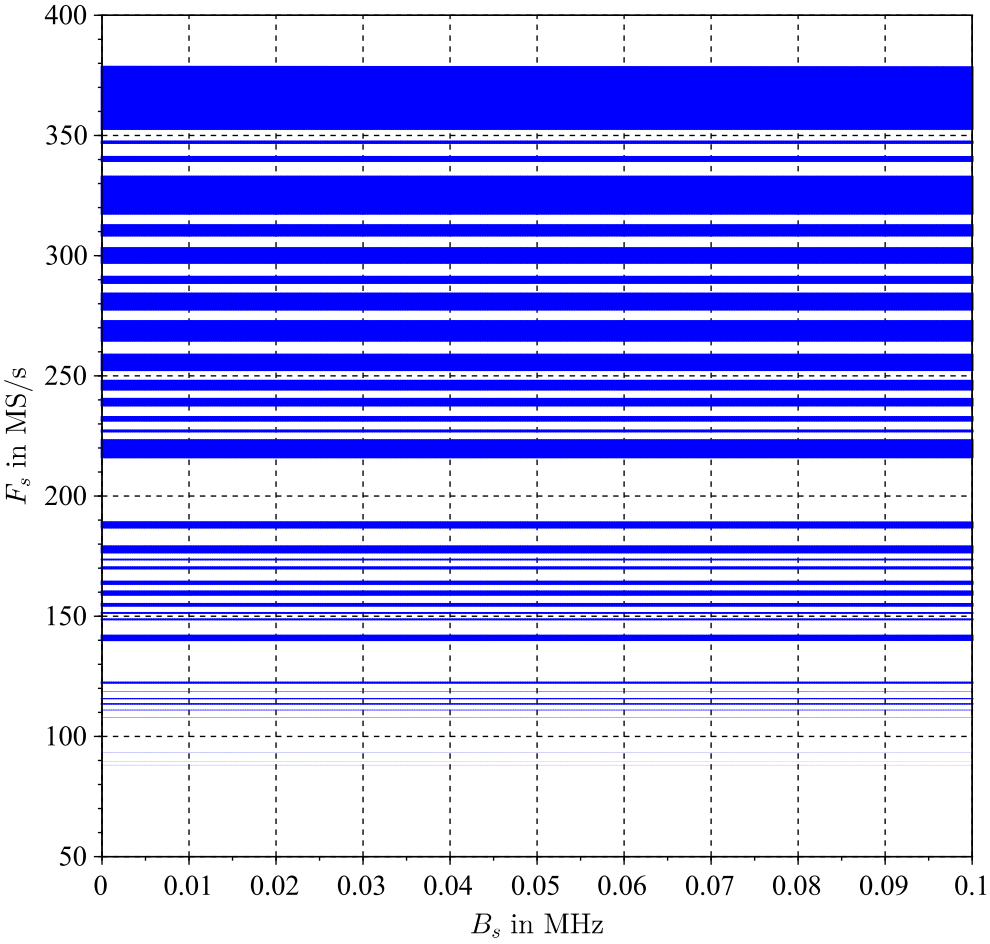

Figure 3.7: Coherent Sampling frequency intervals vs transition bandwidth B_s, close-up.

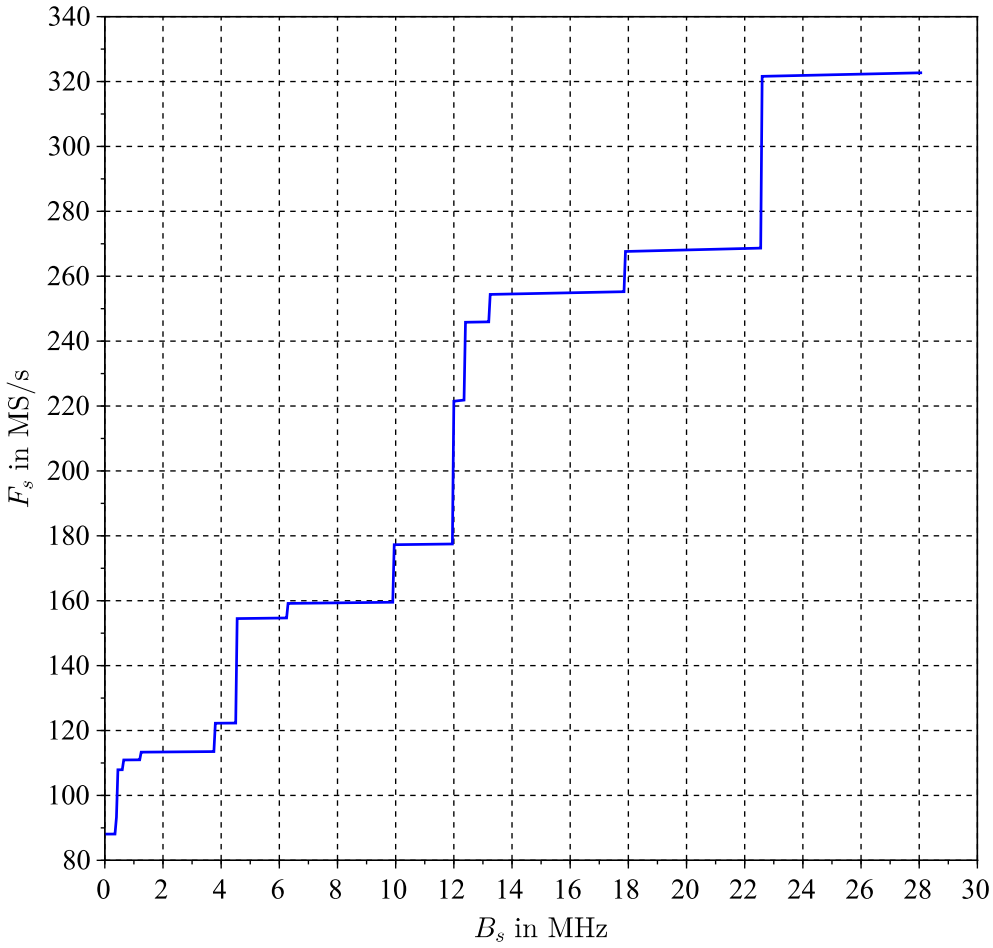

Figure 3.8: Minimum Coherent Sampling frequency vs transition bandwidth B_s.

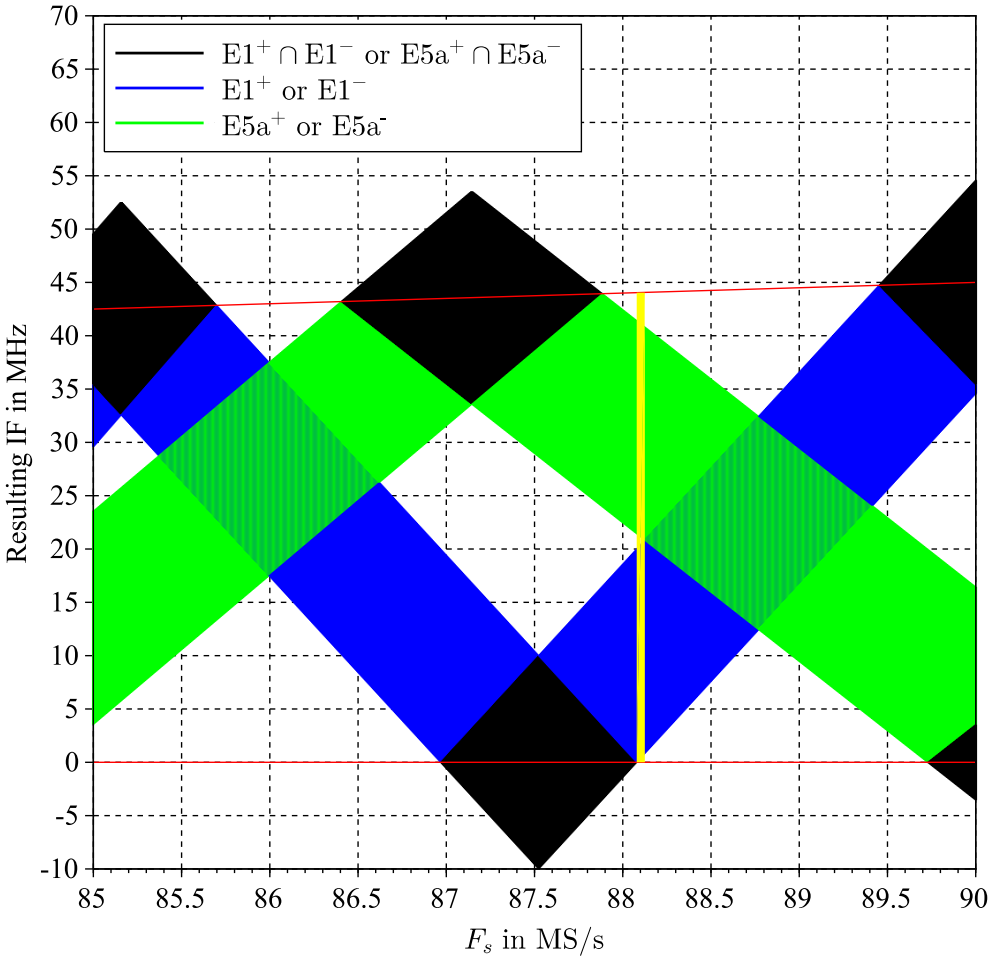

Figure 3.9: Ladder diagram for Coherent Sampling, transition bandwidth $B_s = 0\,\text{MHz}$.

for the negative part of the spectrum of E1 (blue) and of E5a (green), the descending strips being for the positive part. The intersections of the ascending and descending strips, plotted in black, as well as the intersections of the blue and green strips, indicate overlapping of bands, that is forbidden values for the sampling frequency F_s. The interval of permitted sampling frequencies is then the yellow rectangle, where no bands superimpose.

The ratio between the minimum sampling frequencies calculated here and in section 3.1 is greater than 10 which is a real improvement, at the expense of a higher analog Front-End complexity though, but reduced ADC complexity.

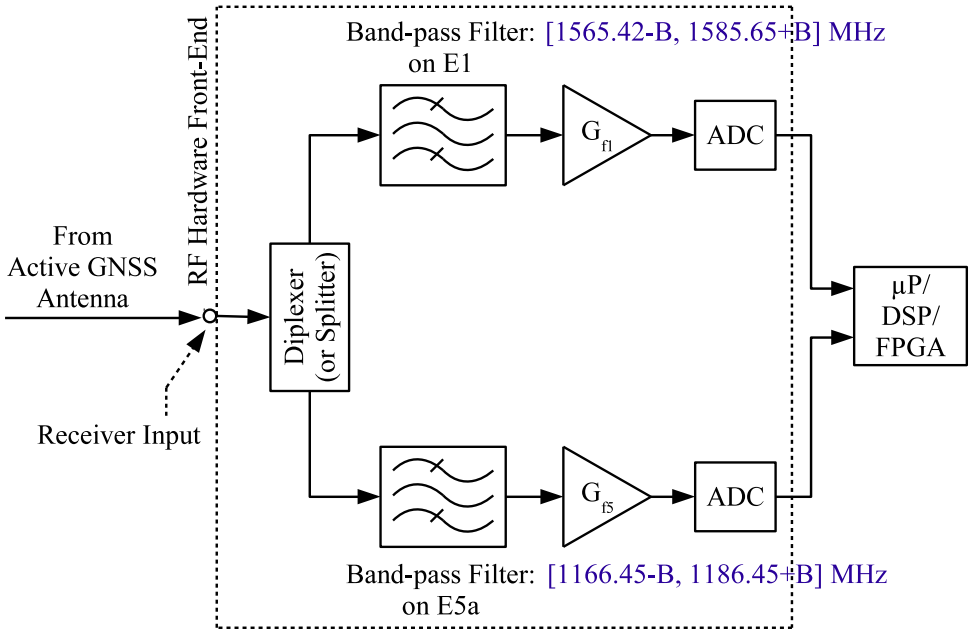

Figure 3.10: Separate Direct Sampling.

3.3 Separate Sampling

The second proposed architecture does not provide coherency, but in return relaxes the need to perfectly compensate for the different RF paths. It is represented in figure 3.10. In this design, the signal received from the active GNSS antenna is also first split into two paths by either a diplexer or a power splitter [4]. Again some extra filters are then needed for the same reason as presented with Coherent Sampling. However, the required minimum selectivity is different because, as each band is sampled separately, it does not matter if during the sampling of the E5a band the E1 band is aliased, and vice versa, because the other band is filtered by the passband filter. Immediately following the extra RF filters, fixed gain amplifiers are used to adjust separately the level of each signal to the input range of its dedicated ADC. Finally, the two signals are digitized individually.

4. A diplexer should be used preferably for the same reasons as in the Coherent Sampling case, but a power splitter could also be used.

3.3.1 Requirements on the Extra RF Filters

The maximum magnitude of the frequency response of the extra RF filters can be found in figure 3.11 [5]. The magnitude of the two transfer functions is drawn in the same figure to ease comparison between them but definitely refer to two distinct physical filters. The magnitude was calculated in this way:

- in-band it is set to 0 dB so that the useful signals are unaltered,
- out-of-band it is equal
  - for the E5a branch filter to −(mask level in figure 2.7) − 103 dBm − 15 dB margin. The output of the filter corresponding to an input at any mask level will then reach at most −118 dBm, 15 dB under the mask level in the E5a band,
  - for the E1 branch filter to −(mask level in figure 2.7) − 118 dBm − 15 dB margin. The output of the filter corresponding to an input at any mask level will then reach at most −133 dBm, 15 dB under the mask level in the E1 band.

The 15 dB margin is included for the same reason as for Coherent Sampling, to take into account the aliasing of the residues of the filtering process. However, as only one band is sampled in each branch, this time the total bandwidth of the useful signal is $B_{5a} = B_1 = 20\,\text{MHz}$, which implies that $F_s \geq 40\,\text{MS/s}$. It gives, using the calculation method detailed in section 3.2.1, $n \leq 28$ and $10\log_{10}(n) \leq 14.47\,\text{dB}$. The value of 15 dB has been retained for sake of simplicity.

3.3.2 Minimum Sampling Frequency

Applying the maximum magnitude of the frequency response of the extra RF filters presented in figure 3.11 to the CW interference mask of figure 2.7 at the receiver input gives the new maximum spectral content to be considered at the input of the ADCs. It is drawn in figure 3.12.

Again it is then possible to calculate the minimum sampling frequency, but for each band separately here, which allows the aliasing of the useful band without overlapping. If the ideal transfer functions of the extra filters could not be reached for some reason, this minimum sampling frequency was also calculated assuming a supplementary transition bandwidth B_s around each side of the useful band.

5. The displayed magnitude was calculated, as for Coherent Sampling, without a possible contribution of the filtering capabilities of the diplexer, if used. Consequently it should be considered as a lower bound too.

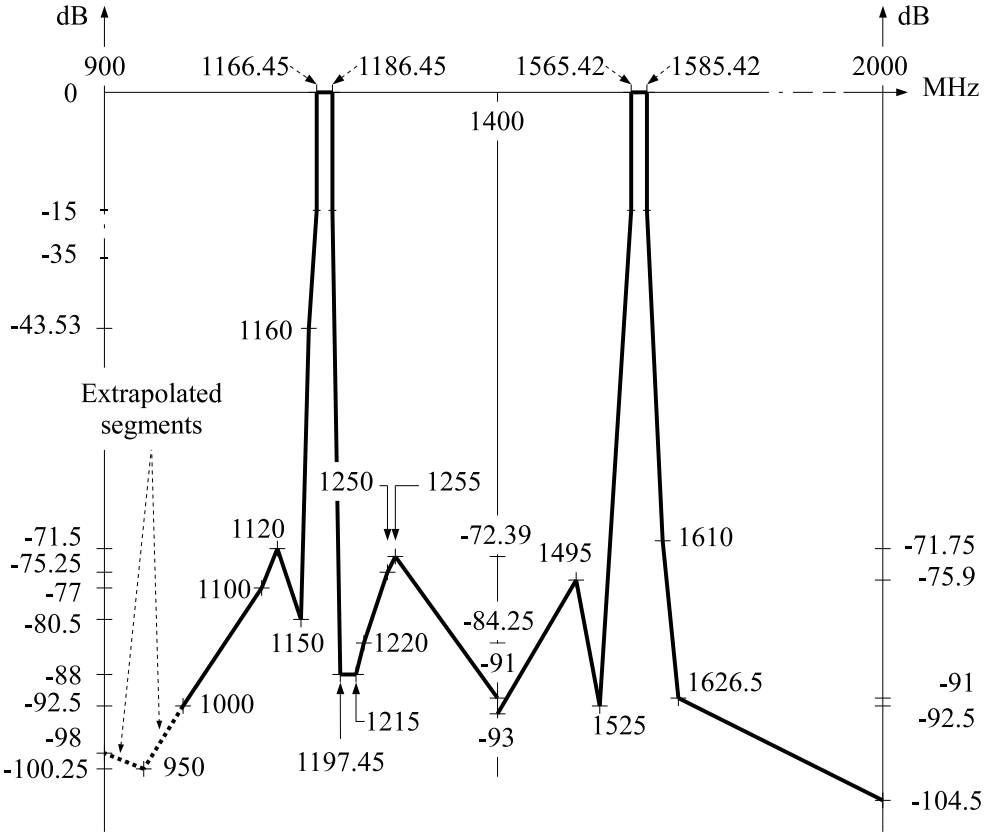

Figure 3.11: Maximum magnitude of the frequency response of the extra RF filters needed before Separate Sampling.

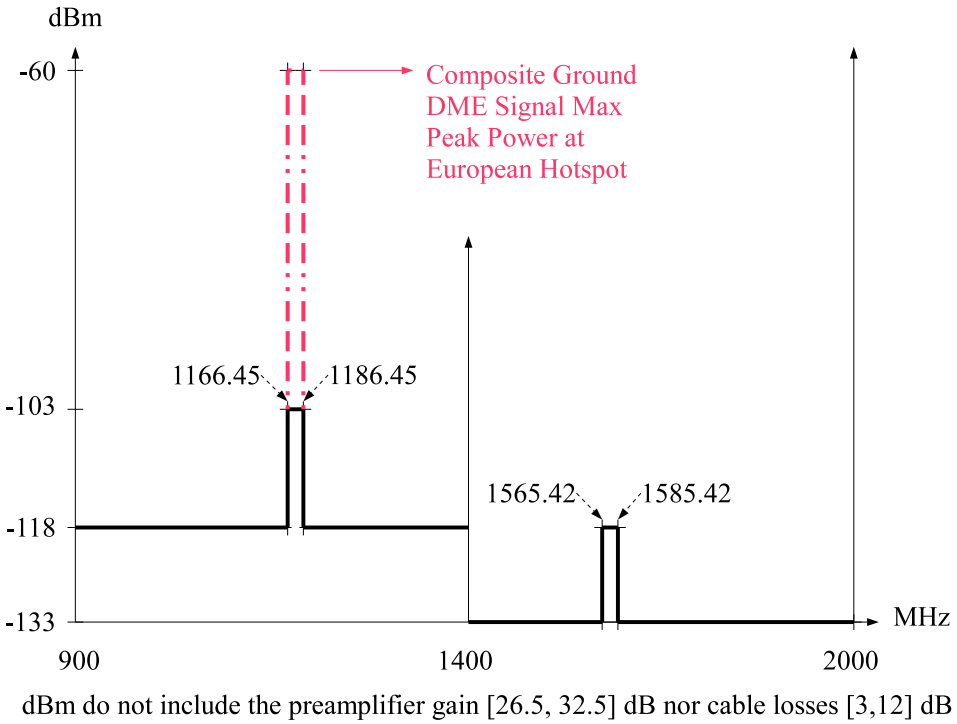

Figure 3.12: Maximum spectral content at the input of the ADCs with Separate Sampling.

The intervals of possible sampling frequencies are presented in figure 3.13 for the E5a band and in figure 3.14 for the E1 band. Each time the top plot displays all the intervals while the bottom plot shows a close-up for sampling frequencies lower than 400 MS/s. Figure 3.15 is a summary of figure 3.13 and 3.14 as only the minimum sampling frequency is traced as a function of the transition bandwidth B_s. Only one bound value is of interest in the Separate Sampling case in comparison to the Coherent Sampling Case. It corresponds to $B_s = 0$ MHz: the minimum minimorum sampling frequency, 40.22 MS/s for the E5a band and 40.14 MS/s for the E1 band, which is approximately equal in each case to the double of the bandwidth of the useful signal. It is interesting to sum the two sampling frequencies, which gives 80.36 MS/s, nearly the same value as in Coherent Sampling. Nevertheless, here the two bands are digitally separated at source, as opposed to the Coherent Sampling architecture where this separation is left to be done, as it is studied in chapter 8.

Here also there is a real improvement in the minimum sampling frequencies calculated in comparison to section 3.1, at the expense of the extra filters as for Coherent Sampling.

3.4 Conclusion

Two Direct Sampling architectures suitable for Civil Aviation use were proposed in this chapter. The first architecture allows the Coherent Sampling of the E5a and E1 bands. It requires extra RF filters which were specified. The slope between the E5a passband upper limit (1186.45 MHz) and the next stopband lower limit (1197.45 MHz) can reach −98 dB. The possible sampling frequencies were also calculated, leading to a minimum of $F_s = 88.08$ MS/s for extra RF filters meeting their specifications. The second architecture provides Separate Sampling of the E5a and E1 bands. Extra RF filters are also needed and they were specified. The requirements are slightly less than for Coherent Sampling, but remain high. The possible sampling frequencies were calculated again, with a minimum of $F_s = 40.22$ MS/s for the E5a band, and $F_s = 40.14$ MS/s for the E1 band, for extra RF filters meeting their specifications. It must now be made sure that the extra RF filters are feasible, for each architecture. This is the subject of the next chapter.

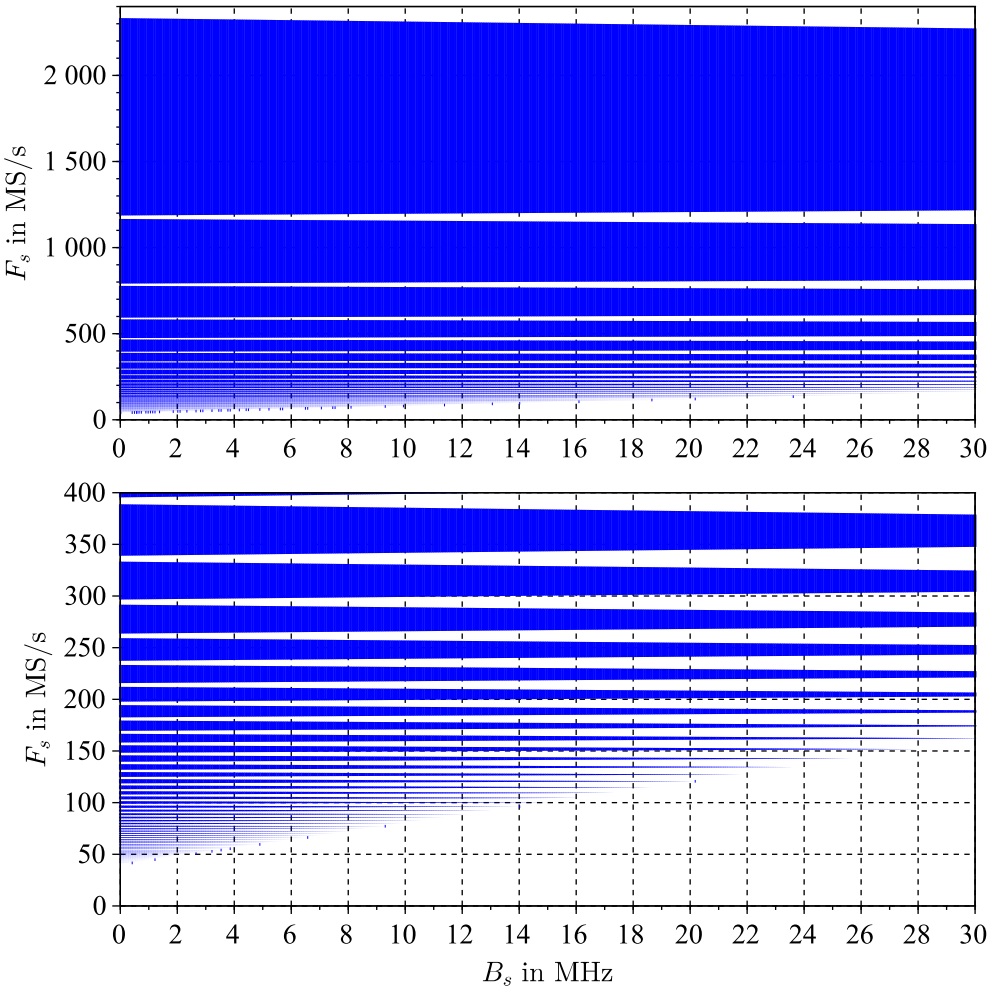

Figure 3.13: Separate Sampling frequency intervals vs transition bandwidth B_s, E5a band.

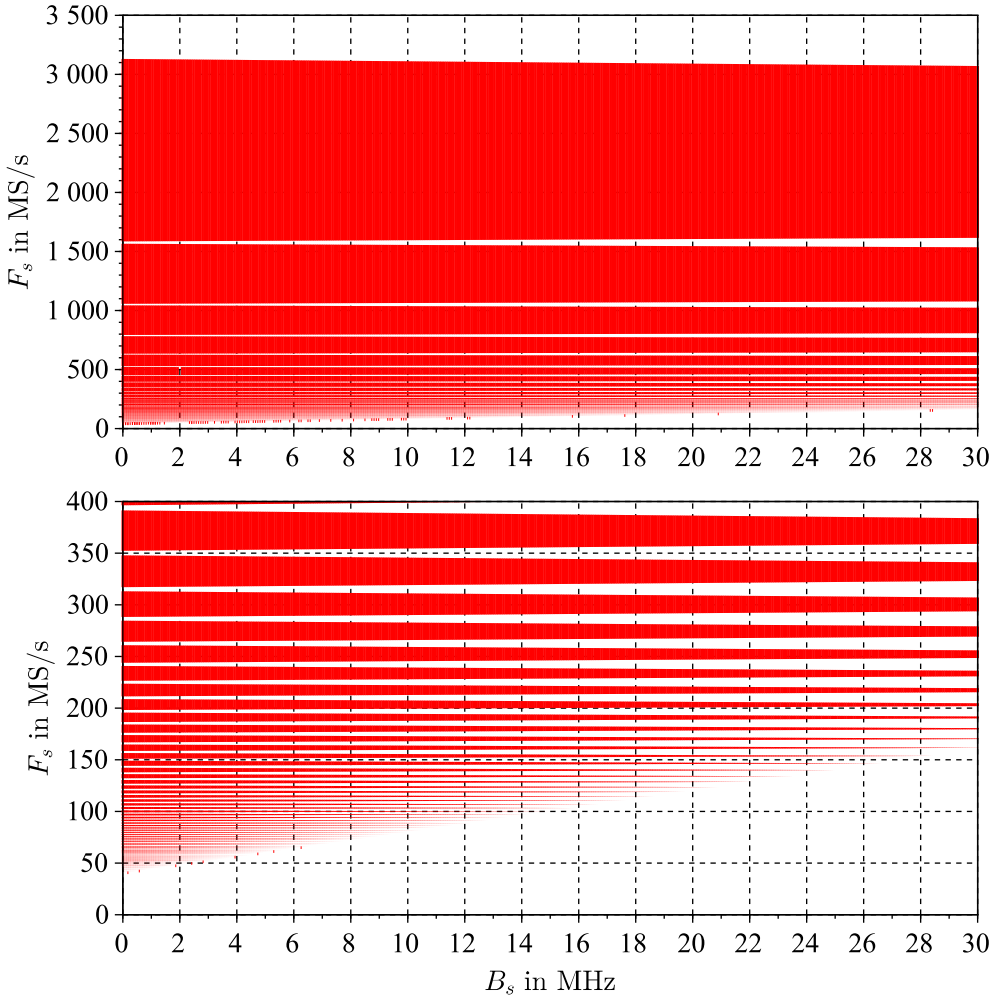

Figure 3.14: Separate Sampling frequency intervals vs transition bandwidth B_s, E1 band.

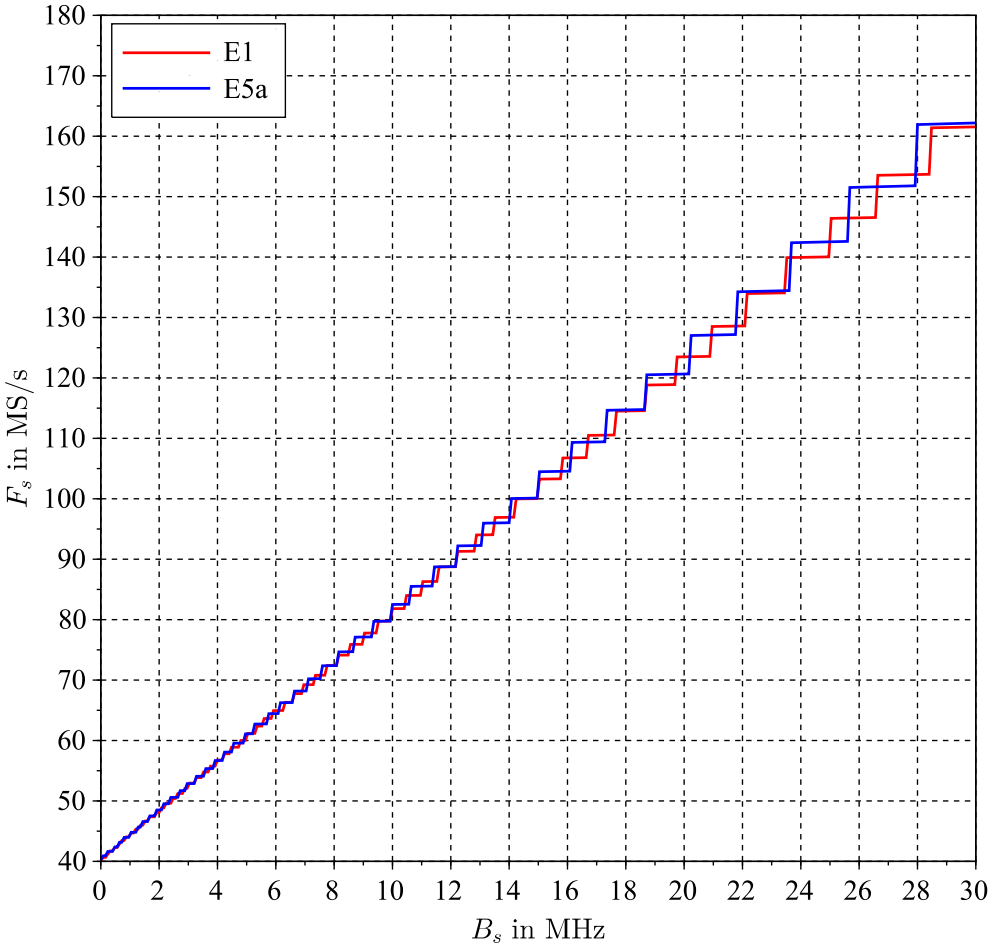

Figure 3.15: Minimum Separate Sampling frequency vs transition bandwidth B_s.

3.5 References

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[3] D. M. Akos, M. Stockmaster, J. B. Y. Tsui, and J. Caschera, "Direct bandpass sampling of multiple distinct RF signals," *IEEE Transactions on Communications*, vol. 47, no. 7, pp. 983–988, Jul. 1999. [Online]. Available: http://dx.doi.org/10.1109/26.774848

[4] J. Thor and D. Akos, "A direct RF sampling multifrequency GPS receiver," in *IEEE Position Location and Navigation Symposium*, 2002, pp. 44–51.

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[6] M. Psiaki, S. Powell, H. Jung, and P. M. Kintner, "Design and practical implementation of multifrequency RF front ends using direct RF sampling," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 10, pp. 3082–3089, Oct 2005.

Feasibility of the Extra RF Filters

4

The extra filters needed by both coherent and separate sampling architectures to satisfy the Civil Aviation robustness specifications against interference show very high slopes between their bandpass and their stopband. Indeed they are so important that one can doubt the feasibility of the filters. Furthermore if they can be realized, it is a risk that their transfer function could not be stable enough vs temperature so that they may not verify the minimum specifications under some various temperature conditions. That is the reason why this chapter investigates the feasibility of these supplementary RF filters through prototyping.

A brief state of the technology has shown at the frequencies of interest, that is around 1176.45 MHz for the E5a band and around 1575.42 MHz for the E1 band, the most adapted technique to design these high order filters is to use SAW (Surface Acoustic Wave) or BAW (Bulk Acoustic Wave) filter elements [1]

Unfortunately most components of this kind are only available through distributors in large quantity (e.g., several thousands), beyond our reach, and we had to be satisfied with what was possible to buy. This fact explains why the work presented here does not follow a top-down approach, from the specification to the realization, but uses a given component that was available.

This component, the SF1186B-2 SAW Filter from RFM®, specifically designed for the GPS L1 band is presented in the first part of this chapter. In the second part the test circuit which was built is presented, with the transfer function which was measured. Then the sensitivity to temperature of this filter is studied in the last part.

1. Other technologies give either too large (distributed element) or expensive (cavity), or both, solutions.

4.1 The SF1186B-2 SAW Filter from RFM®

Its datasheet [1], available in appendix C, gives us the main specifications about this component. Among them, regarding our selectivity objective, the most important are:

- center frequency: 1575.42 MHz.
- 1 dB bandwidth: 15.3 MHz typical. It means that a 3 dB bandwidth around or greater than the targeted one, 20 MHz, can be expected (but needs to be verified).
- passband VSWR (Voltage Standing Wave Ratio): 2.0 maximum.
- insertion loss: 3.5 dB maximum.
- input/output impedance: 50 Ω. As it will be explained later in this chapter this is very helpful in practice because it much simplifies the impedance matching with the connectors.
- temperature coefficient: −30 ppm/°C. This will be discussed in the last section about temperature sensitivity.
- 3.0 x 3.0 x 1.3 mm: a small size, desirable for an embedded system as a Galileo receiver for Civil Aviation.

It is to be noticed that no group delays are specified, although phase response linearity has a proven impact on the final pseudorange measurement error, and so on the final navigation solution.

4.1.1 Performance of One SF1186B-2

4.1.2 S-Parameters

More interesting than the datasheet in our situation, RFM® provides two Touchstone® [2] files [3] and [4] with measurements of the SF1186B-2 S-parameters (Scattering parameters). It is recalled here, from [5], that the S-parameters link the reflected (b) and incident (a) waves at each of the two ports, (1) and (2), of the SF1186B-2 as defined in figure 4.1 and formalized by the matrix equation

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{4.1}$$

As the SF1186B-2 filter is a two-port device, *Touchstone® file* will be equivalently abbreviated as *S2P*[2] *file* in the rest of this chapter.

2. S1P is for a 1-port device, S3P for a 3-port one, etc.

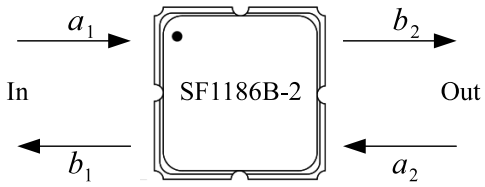

Figure 4.1: Reflected and incident waves at the SF1186B-2 ports [5].

4.1.3 Use of the S-Parameters

The VSWR will be used in place of S_{11}. It is defined in [6] from the reflection coefficient Γ

$$\text{VSWR} = \frac{1+|\Gamma|}{1-|\Gamma|}, \qquad \text{with } \Gamma = \frac{b_1}{a_1} \tag{4.2}$$

The S-parameters have been measured using loads matched to the nominal impedance of the input/output ports of the filter (i.e., 50 Ω), as clarified in the header of the S2P file. In these circumstances, [6] establishes that

$$\Gamma|_{\text{matched load}} = \left.\frac{b_1}{a_1}\right|_{a_2=0} = S_{11} \tag{4.3}$$

The link between $|S_{11}|$ and VSWR is then here finally

$$\text{VSWR} = \frac{1+|S_{11}|}{1-|S_{11}|} \tag{4.4}$$

Concerning $|S_{21}|$, the modulus of the filter transfer function, from now on it is normalized to 0 dB by the addition of the minimum value of the insertion loss (that is in the passband), a quantity defined also in [6] by

$$\text{IL} = -20\log_{10}|S_{21}| \tag{4.5}$$

Finally, instead of the phase of S_{21}, the group delay [7] will be plotted as it is more common in filter theory

$$\tau_d(f) = -\frac{1}{2\pi}\frac{\mathrm{d}\arg\left(S_{21}(f)\right)}{\mathrm{d}f} \text{ in s} \tag{4.6}$$

4.1.4 Wide Frequency Span

The first S2P file [3] corresponds to a wide frequency span. Its content is represented graphically in

- figure 4.2 for the VSWR,

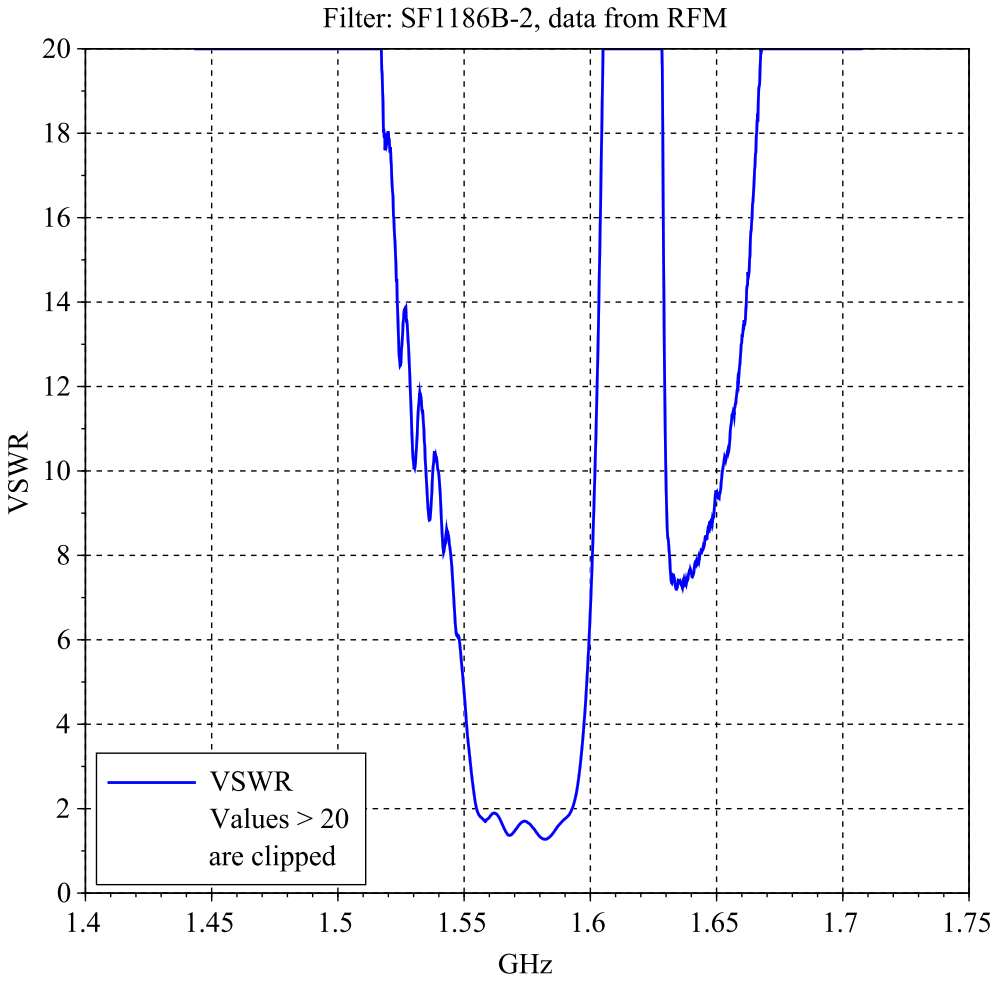

Figure 4.2: VSWR for the SF1186B-2, S2P file from the manufacturer [3].

- figure 4.3 for $|S_{21}|$,
- figure 4.4 for the group delay,
- figure 4.5 for $|S_{12}|$,
- figure 4.6 for $|S_{22}|$.

At this point it is interesting to note that, although the SAW filter is a passive device, that is a reciprocal network, $|S_{21}|$ and $|S_{12}|$ plotted in figure 4.3 and in figure 4.5 respectively, are not exactly equal. This may be due to differences between the internal input and output impedance adaptation circuits which match the device internal input and output impedances to the specified 50 Ω external input/output value. The input and output Smith charts presented in the datasheet [1] support this assumption: they show deviation from 50 Ω and slightly differ one from the

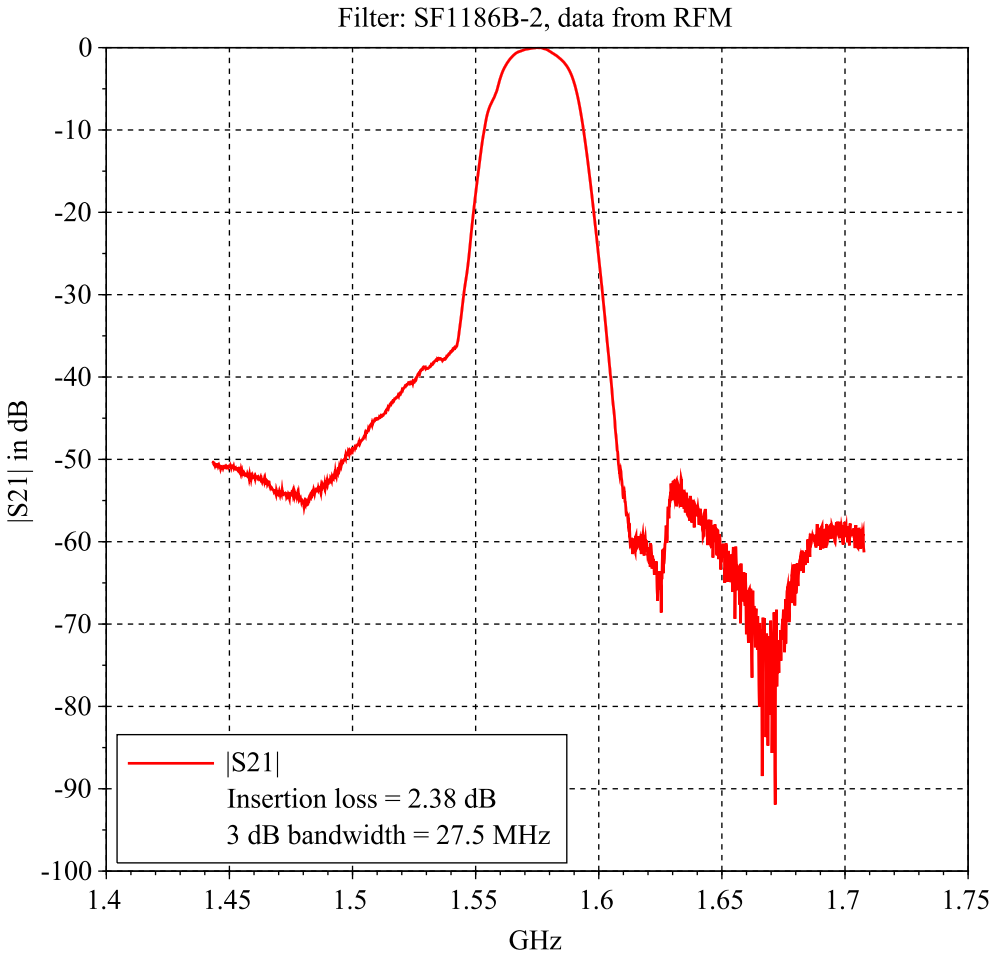

Figure 4.3: $|S_{21}|$ for the SF1186B-2, S2P file from the manufacturer [3].

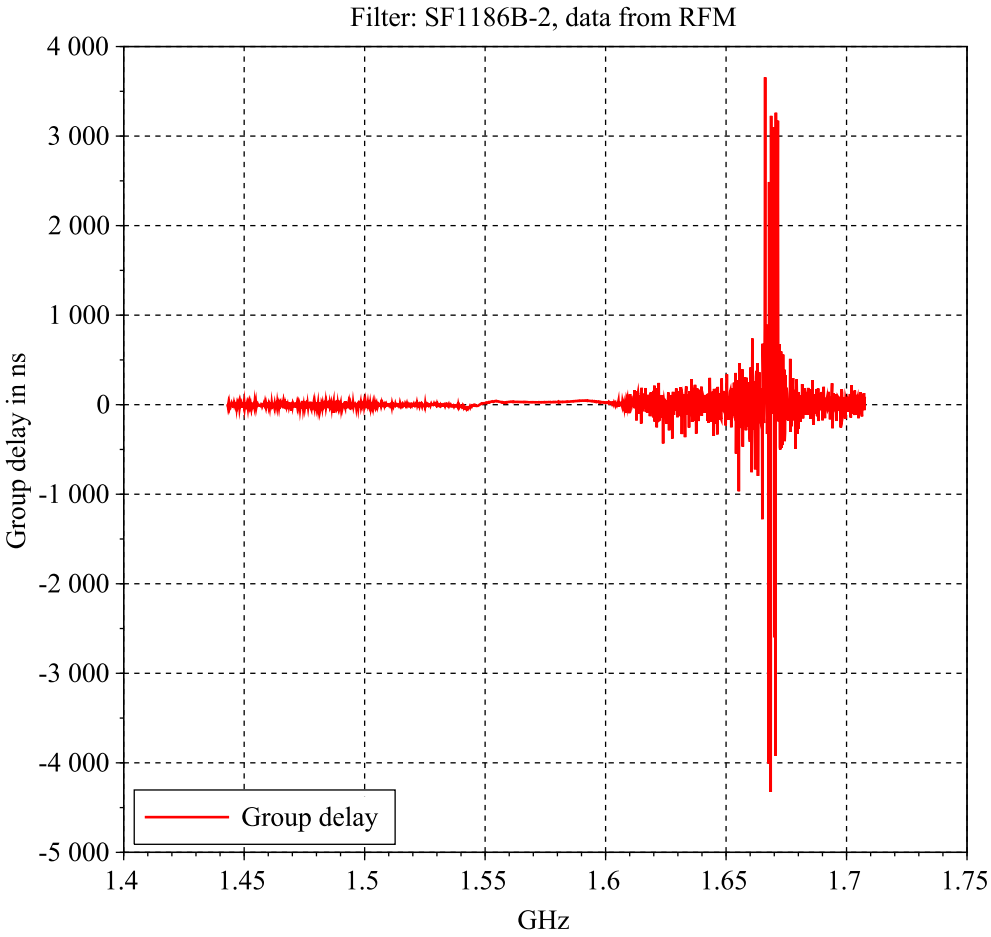

Figure 4.4: Group delay for the SF1186B-2, S2P file from the manufacturer [3].

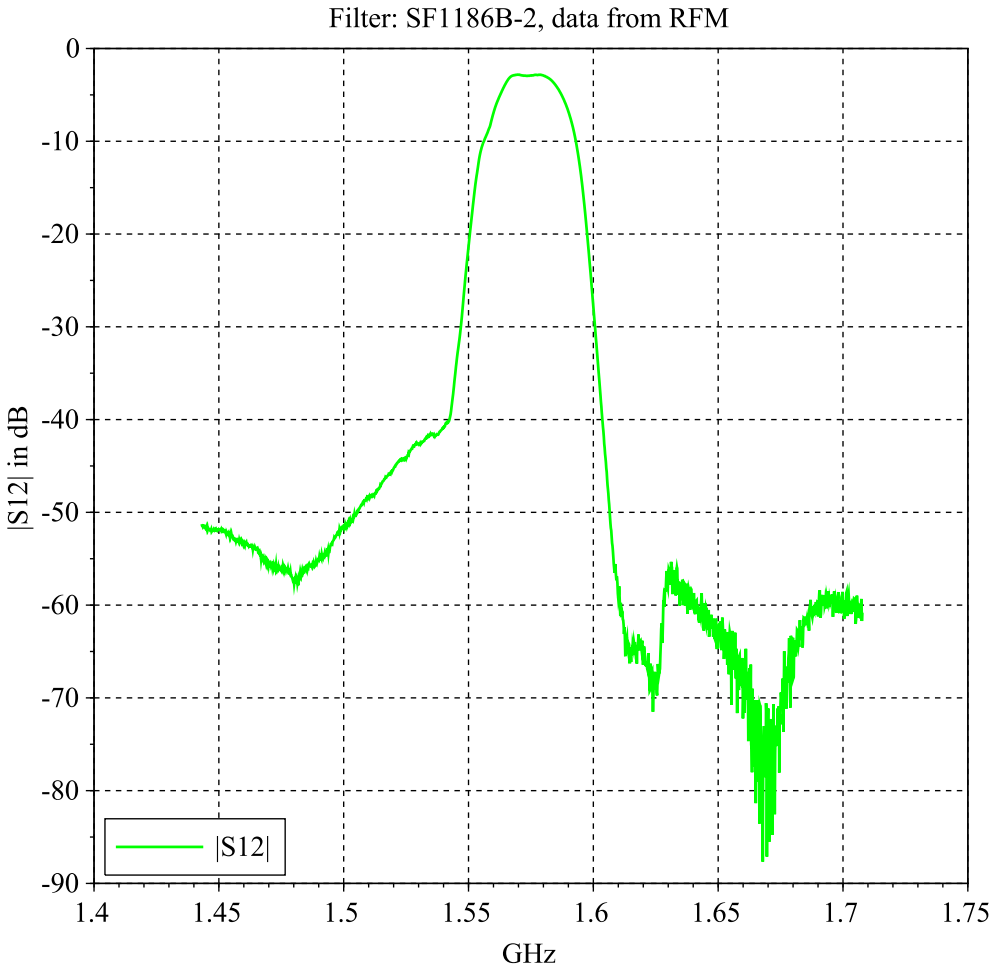

Figure 4.5: $|S_{12}|$ for the SF1186B-2, S2P file from the manufacturer [3].

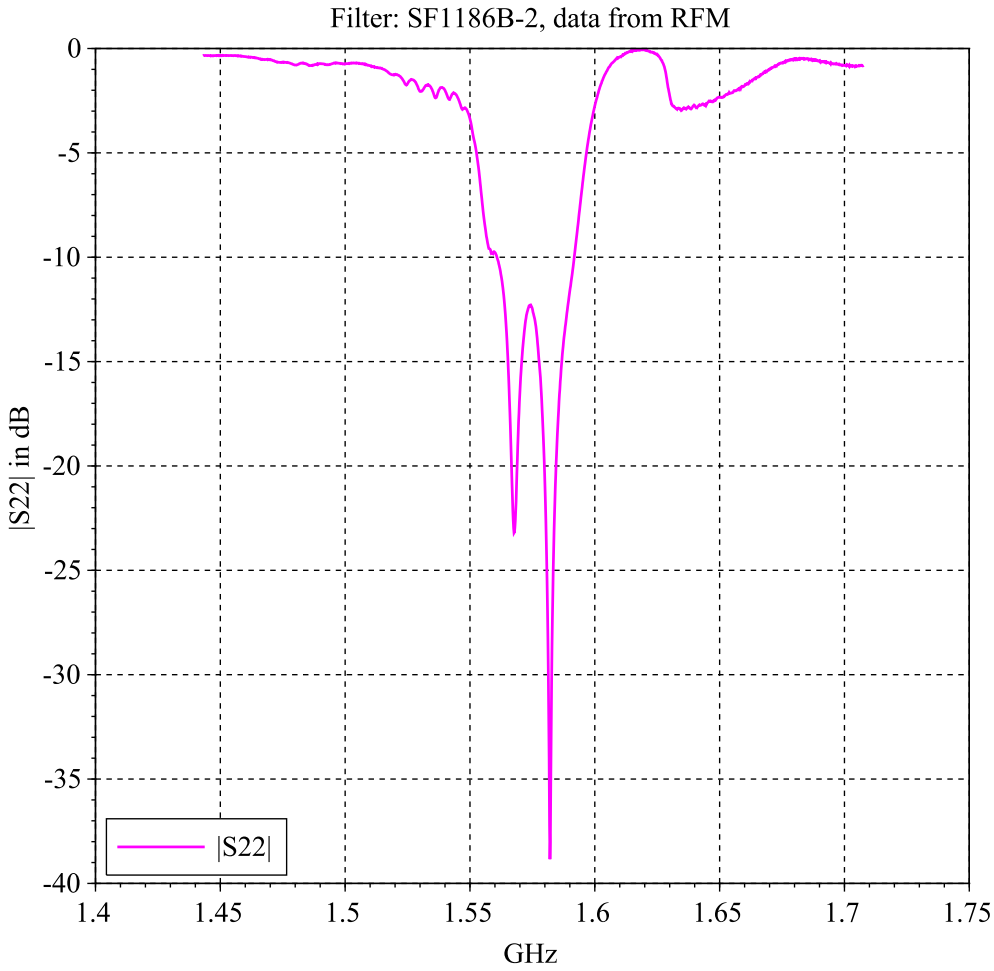

Figure 4.6: $|S_{22}|$ for the SF1186B-2, S2P file from the manufacturer [3].

other. The footnote "Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design." is also a consistent element.

4.1.5 Narrow Frequency Span

The second S2P file [4], focused on a narrower bandwidth, allows a more accurate view on the passband of this filter as it can be seen in

- figure 4.7 for the VSWR,
- figure 4.8 for $|S_{21}|$,
- figure 4.9 for the group delay,
- figure 4.10 for $|S_{12}|$,
- figure 4.11 for $|S_{22}|$.

Figure 4.8 shows that the VSWR is within the specifications, recalled at the beginning of this section. Figure 4.8 confirms that the 3 dB bandwidth is large enough to include the targeted 20 MHz. Last but not least, the group delay appears relatively flat in the passband in figure 4.9, with a range of variation around 20 ns.

In this section all the S-parameters were detailed but for the remaining of this chapter only S_{21}, the filter transfer function, will be focused on as it is the most important characteristic regarding our problem.

4.1.6 Virtual Chain of Two SF1186B-2 in Cascade

Clearly one SF1186B-2 filter alone is not able to reach the minimum required attenuation specified in figure 3.3 or in figure 3.11[3]. However, maybe it is possible with two in cascade as represented in figure 4.12. To investigate this opportunity, two SF1186B-2 were put virtually in cascade, by applying relations[4](4.7) from [7] to the S-parameters given in the two S2P files, one after the other, as illustrated in figure 4.12.

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} = \begin{pmatrix} S'_{11} + \kappa.S'_{12}.S'_{21}.S''_{11} & \kappa.S'_{12}.S''_{12} \\ \kappa.S'_{21}.S''_{21} & S''_{22} + \kappa.S''_{12}.S''_{21}.S'_{22} \end{pmatrix} \quad (4.7)$$

3. For the E1 band the specifications are stronger for Separate Sampling than for Coherent Sampling (due to the 15 dB margin instead of 10 dB), so the Separate Sampling specifications were selected in this chapter in a conservative approach.

4. These relations are valid only if the impedance of the output port of the first element is equal to the impedance of the input port of the second element, which is the case in our situation.

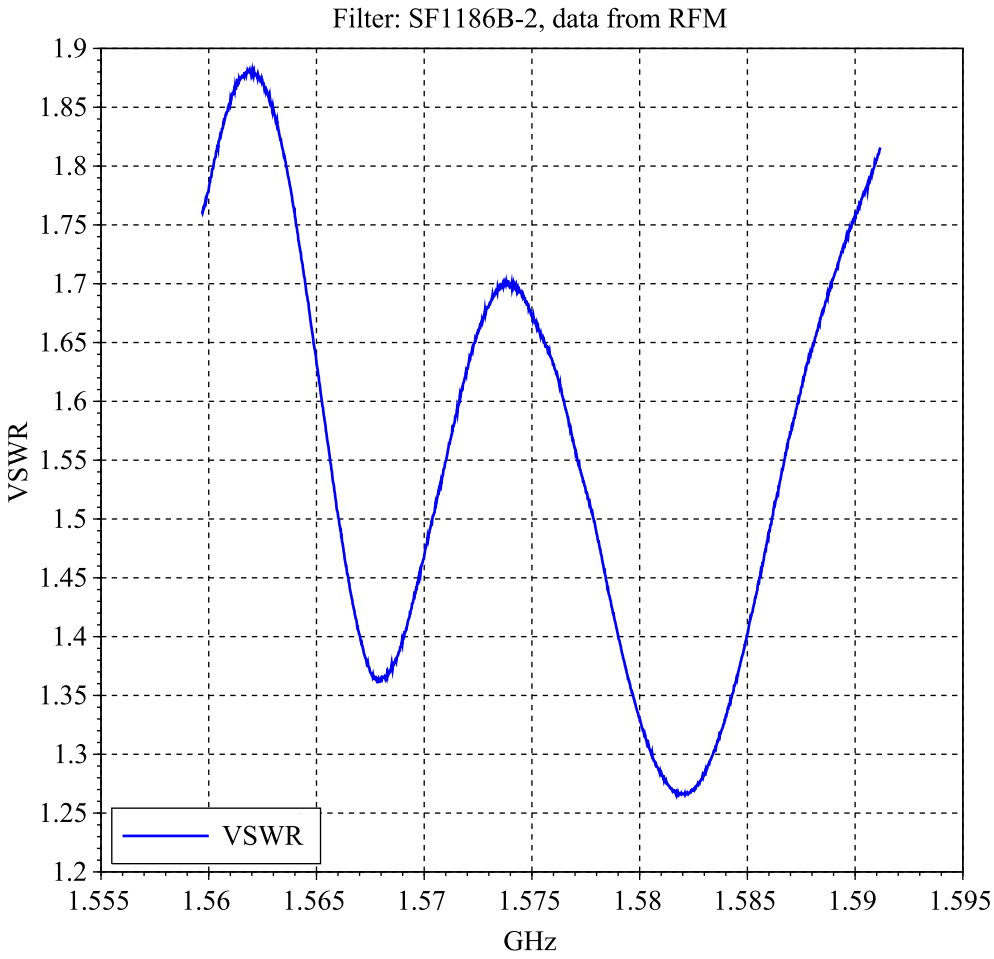

Figure 4.7: VSWR for the SF1186B-2, S2P file from the manufacturer, close-up [4].

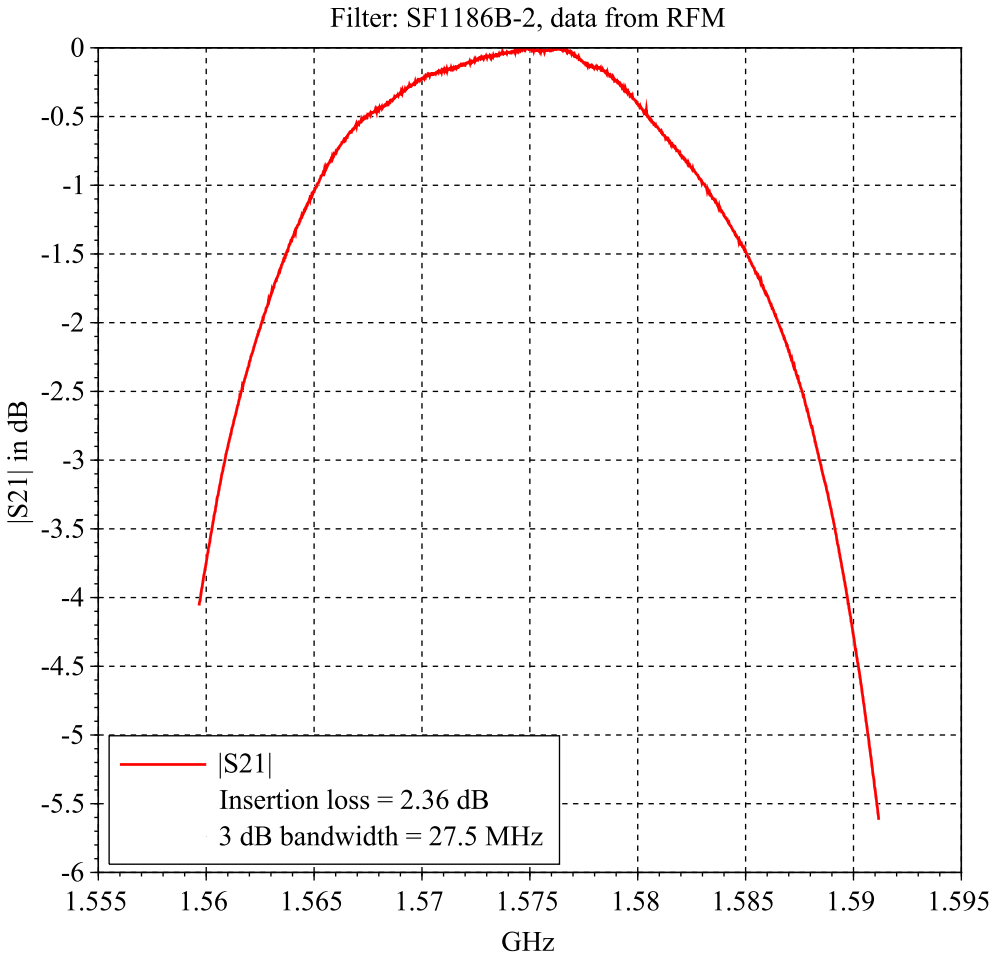

Figure 4.8: $|S_{21}|$ for the SF1186B-2, S2P file from the manufacturer, close-up [4].

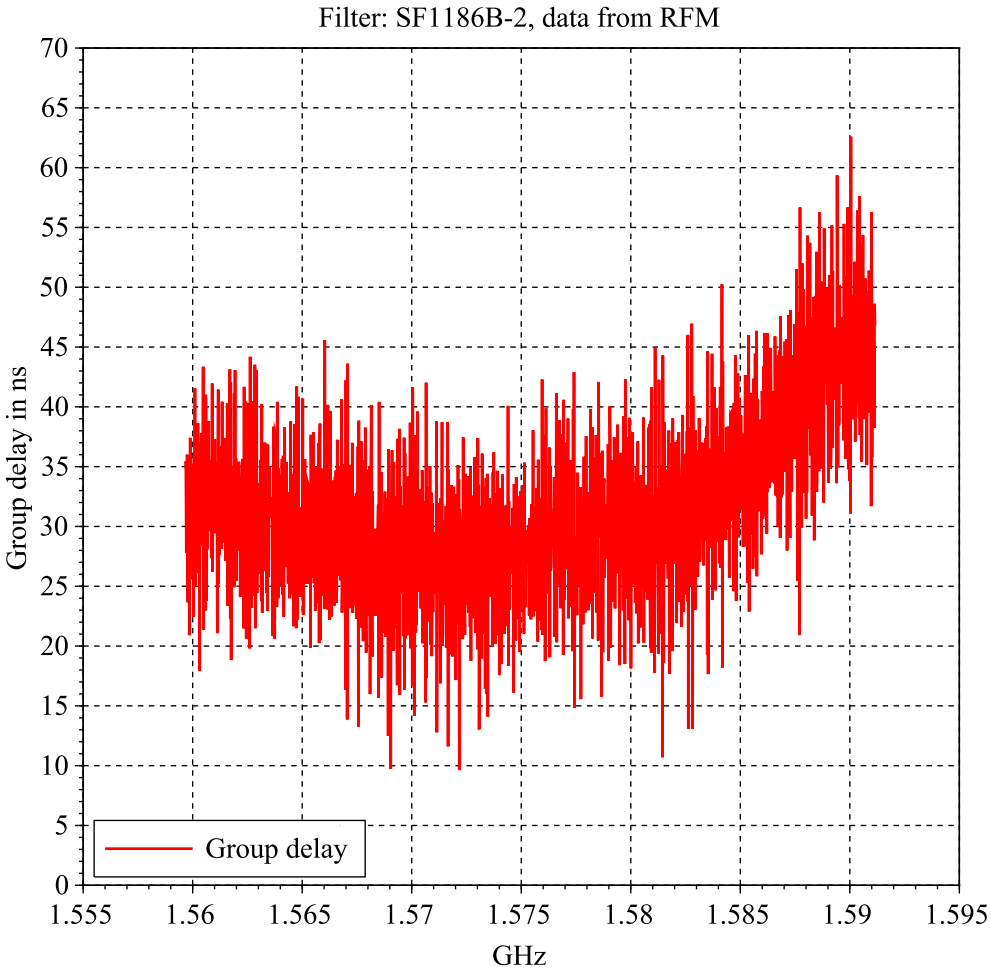

Figure 4.9: Group delay for the SF1186B-2, S2P file from the manufacturer, close-up [4].

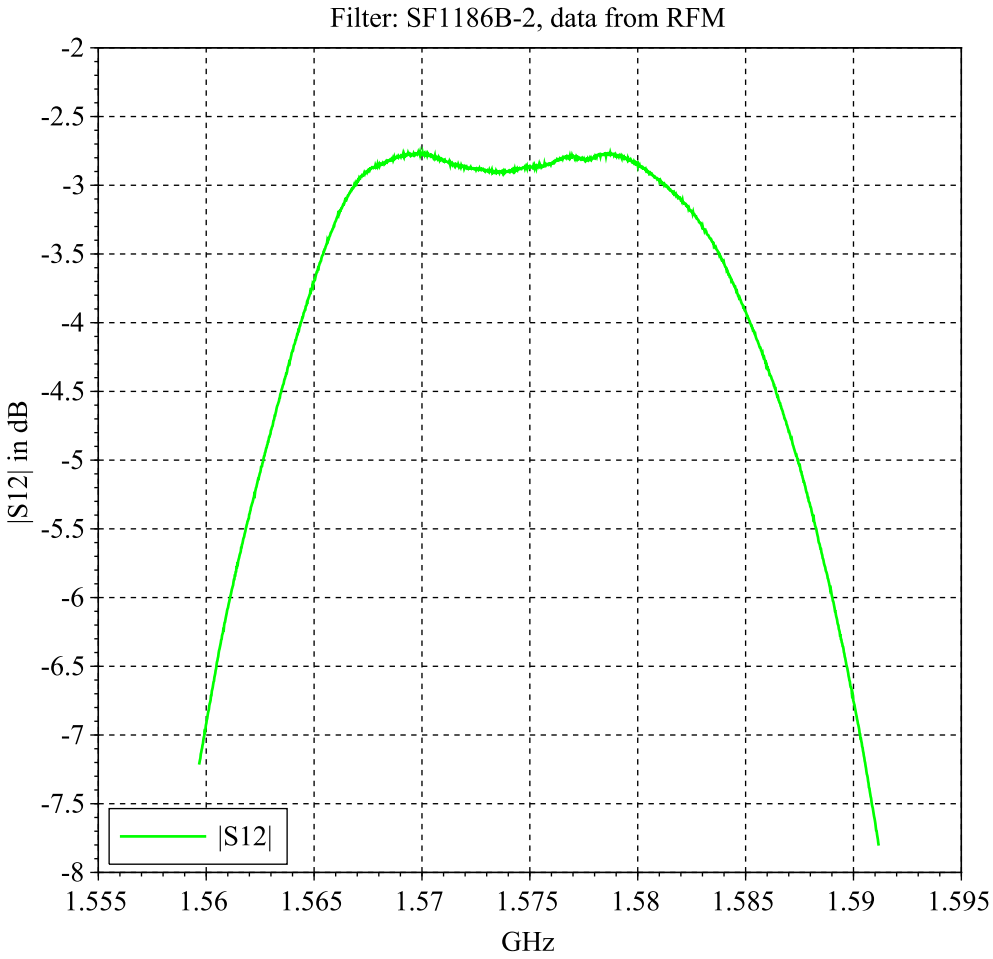

Figure 4.10: $|S_{12}|$ for the SF1186B-2, S2P file from the manufacturer, close-up [4].

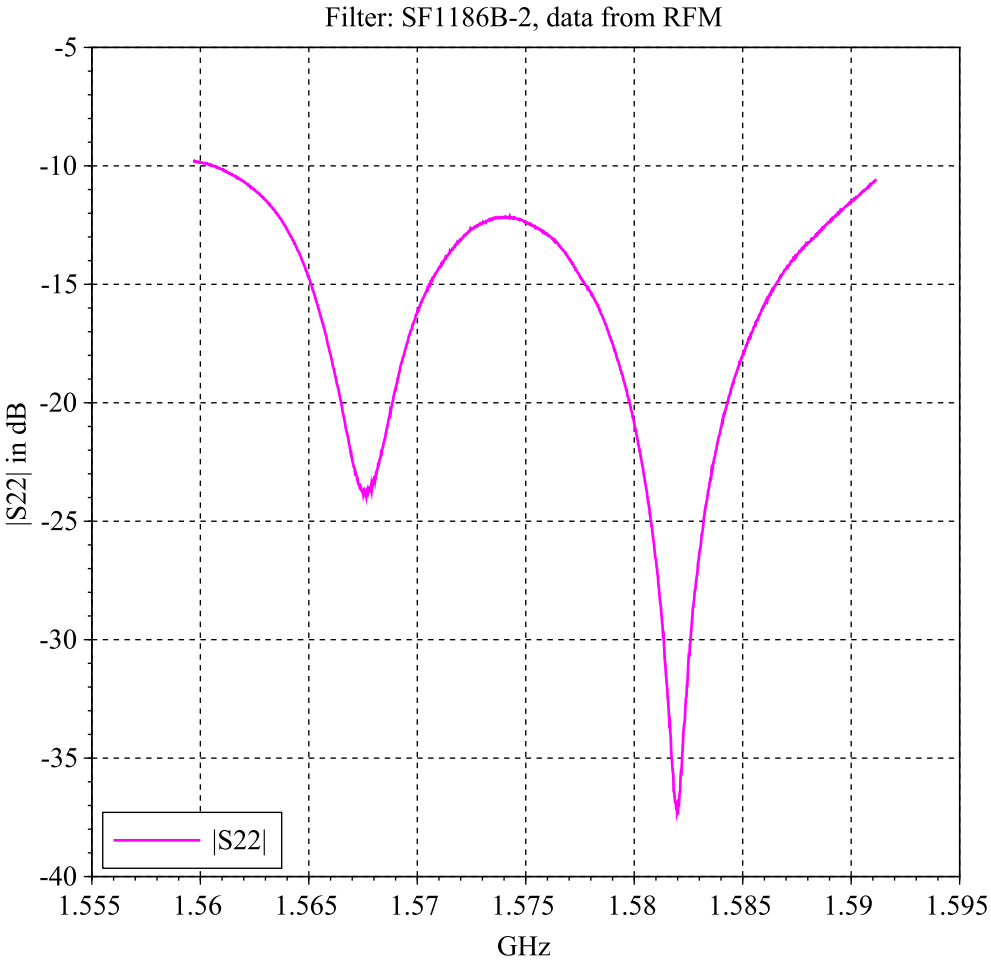

Figure 4.11: $|S_{22}|$ for the SF1186B-2, S2P file from the manufacturer, close-up [4].

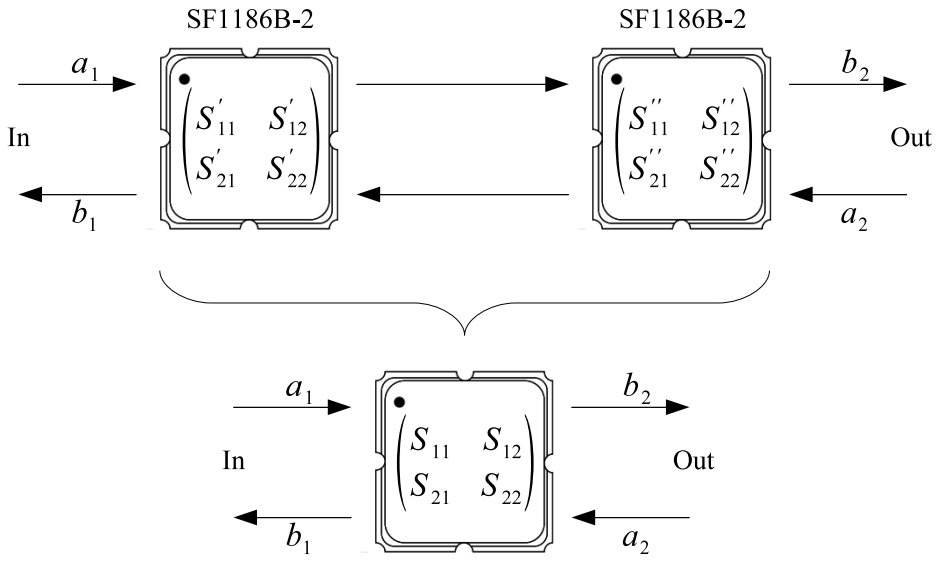

Figure 4.12: Cascade of two SF1186B-2.

with

$$\kappa = \frac{1}{1 - S'_{22}.S''_{11}} \tag{4.8}$$

Figure 4.13 show the resulting $|S_{21}|$ along with the minimum attenuation to be reached, extracted from previously presented figure 3.11. Figure 4.14 is a close-up view on the passband. The results are clearly encouraging as the provided attenuation approaches what is strictly needed and the 3 dB bandwidth is nearly equal to 20 MHz. Although figure 4.13 also points out that the specification is not completely met in the near vicinity of the passband (in the ranges $[\simeq 1550, 1565.42]$ MHz and $[1585.42, \simeq 1600]$ MHz the attenuation is not high enough), it was decided at this stage to not cascade a third filter as it would decrease too much the 3 dB bandwidth. This means that digital filtering will be needed after digitization to complete the specification.

However, figure 4.13 is virtual performance. It needs to be confirmed by physical tests. In this purpose a careful method was adopted rather than to directly proceed to measurements on two SF1186B-2 in cascade: first a PCB (Printed Circuit Board) with only one filter was designed, then two copies were built and tested and finally the two boards were linked in cascade.

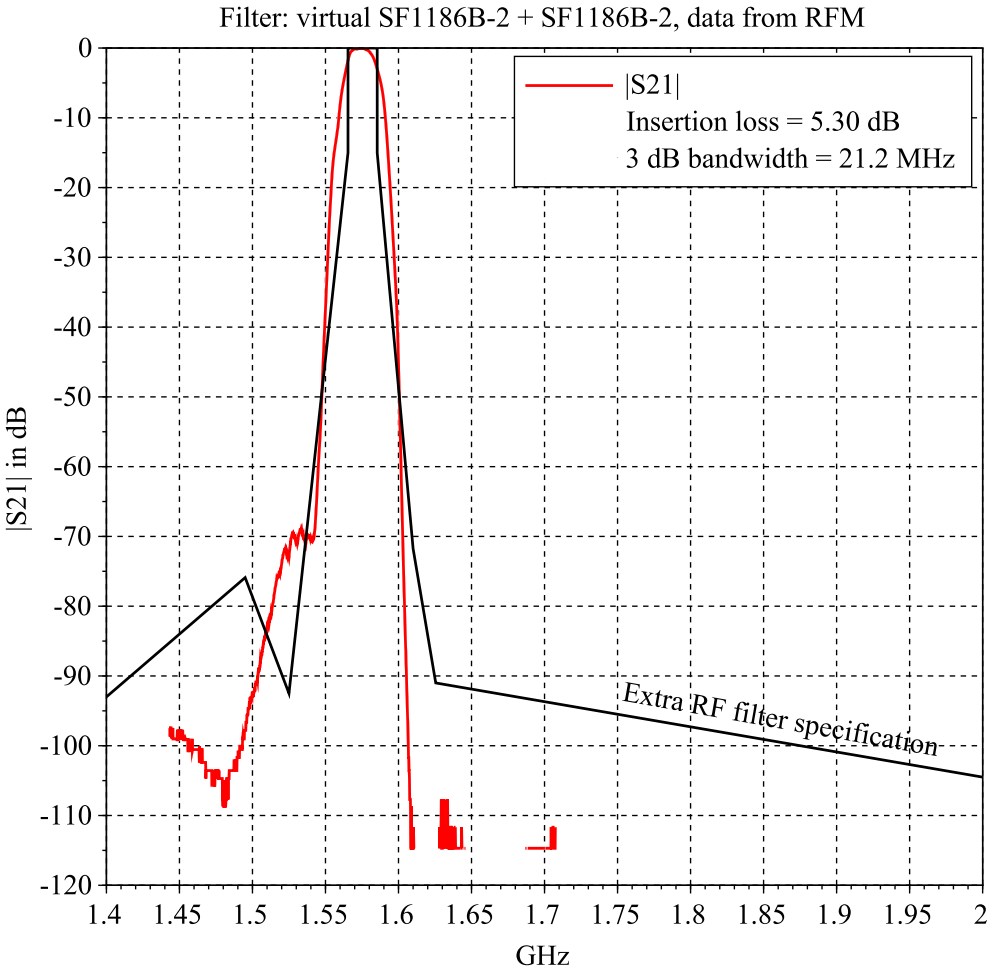

Figure 4.13: $|S_{21}|$ for the virtual chain of two SF1186B-2 in cascade, S2P file from the manufacturer [3].

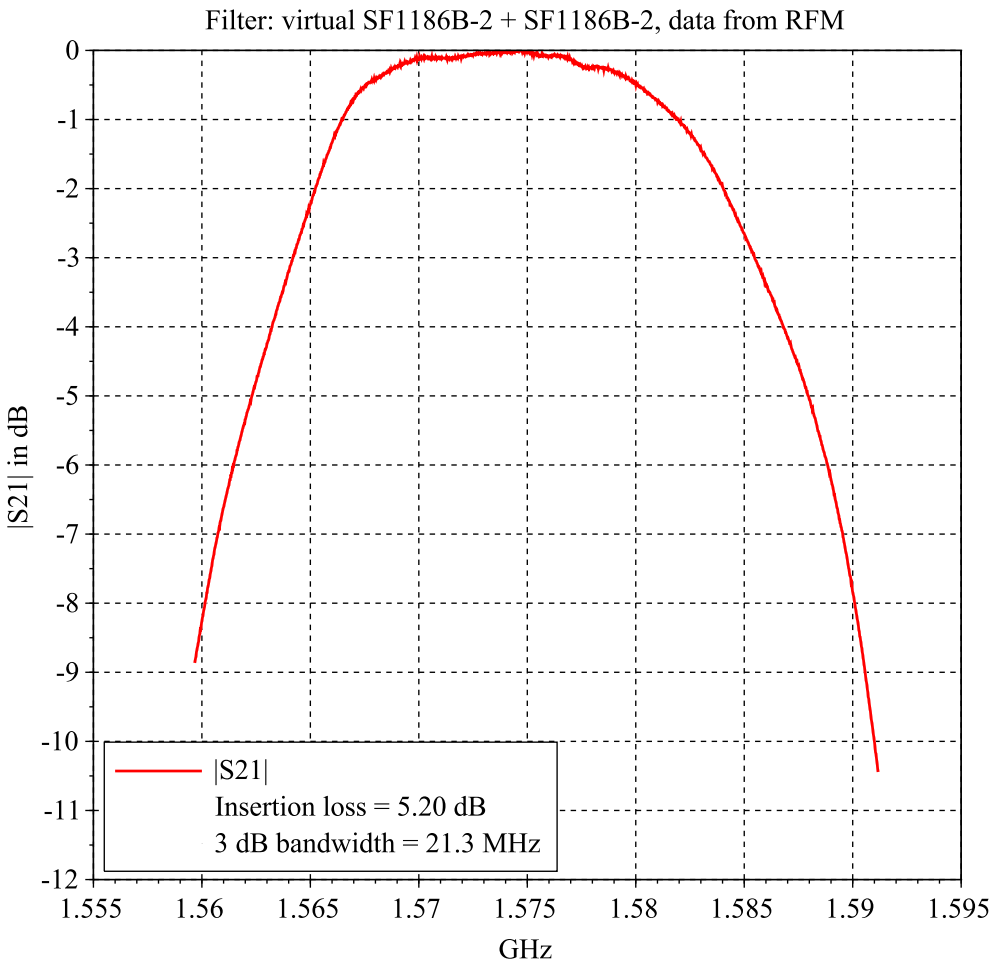

Figure 4.14: $|S_{21}|$ for the virtual chain of two SF1186B-2 in cascade, S2P file from the manufacturer, close-up [4].

4.2 PCB for Testing the SF1186B-2

4.2.1 Design of the PCB

To obtain the best performance from the SF1186B-2 filter, the main challenge is to design a board which matches as best as possible the filter input and output impedance (50 Ω) to the impedance of the SMA (SubMiniature version A) connectors (50 Ω also). To achieve this objective as simply as possible, it was decided to take advantages of the fact that a $\lambda/2$ line, whatever its width, provides the same impedance at its output than at its input. This design is not compact, but the width of the line can be set freely. Indeed as the impedance of the SMA connector is the same as the nominal impedance of the input/output ports of the filter (i.e., 50 Ω), the width of the lines can be set equal to the dimension of the input/output pads of the filter, removing the need to taper the lines to the pads. Concerning the type of the lines, the particular footprint of the SF1186B-2 device [1] (each signal pad is framed symmetrically by two ground pins) leaded naturally to use CPW (Coplanar Wave Line) lines. For its robustness and because it was readily available in the Lab, single-sided 1.562 mm FR-4 epoxy board was selected to build the PCB. The physical length of the line was calculated, by mean of the AppCAD software from Agilent Technologies®, to provide an electrical length of 180 ° at the E1 center frequency, that is 1575.42 MHz. Figure 4.15 proposes a screenshot of this software with the parameters used for this design and the corresponding results. A point to note in this picture is the impedance of the line, Z0 = 61.5 Ω, which is not equal to the impedance of the input/output ports of the filter nor to the impedance of the connector. This has no effect on the performance.

A printout in figure 4.16 and the two pictures shown in figures 4.17 and 4.18 demonstrate how this circuit is designed using $\lambda/2 \simeq 5.82$ cm CPW transmission lines that link and match the SMA connectors to the input and the output of the filter.

4.2.2 Performance of each PCB

The S-parameters of the two boards were measured using a E5071C network analyzer from Agilent Technologies®, pictured in figure 4.19. Figure 4.20 and Figure 4.21 present $|S_{21}|$ for boards #1 and #2 respectively. Both curves are homogeneous, but quite differ in the stopband from the one in figure 4.3 taken from the first S2P file [3]. Figure 4.22 allows a comparison between $|S_{21}|$ measured for board #1 and the values from the S2P file. It is believed that the differences come from our PCB design which is different from the RFM® design. The slight differences

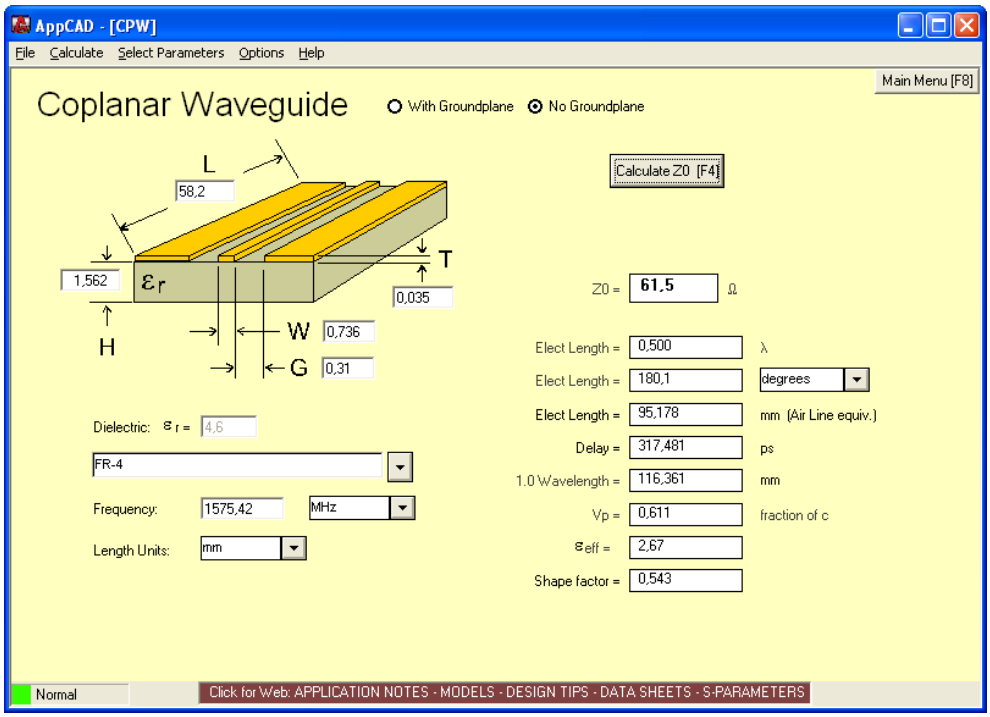

Figure 4.15: Screenshot of the AppCAD software from Agilent Technologies®.

between traces in figure 4.20 and figure 4.21, especially the higher insertion loss of board #2, could be explained by the manufacturing tolerances of the SF1186B-2 filter or by the differences during the manufacturing of the two PCBs themselves.

4.2.3 Virtual Chain of the Two PCBs in Cascade

As shown previously in section 4.1.6, the two boards were virtually linked in cascade using their S-parameters, already presented in section 4.2.2. Figure 4.23 illustrates a very promising $|S_{21}|$, which is under the minimum required attenuation, as presented earlier in figure 3.3, nearly everywhere.

This time again the result must be corroborated by a comprehensive physical test.

4.2.4 Real Chain of the Two PCBs in Cascade

The picture in figure 4.24 shows the two boards linked in cascade over a sheet of microwave absorbing foam. This installation was needed to reach the best attenuation which is displayed in figure 4.25. This fig-

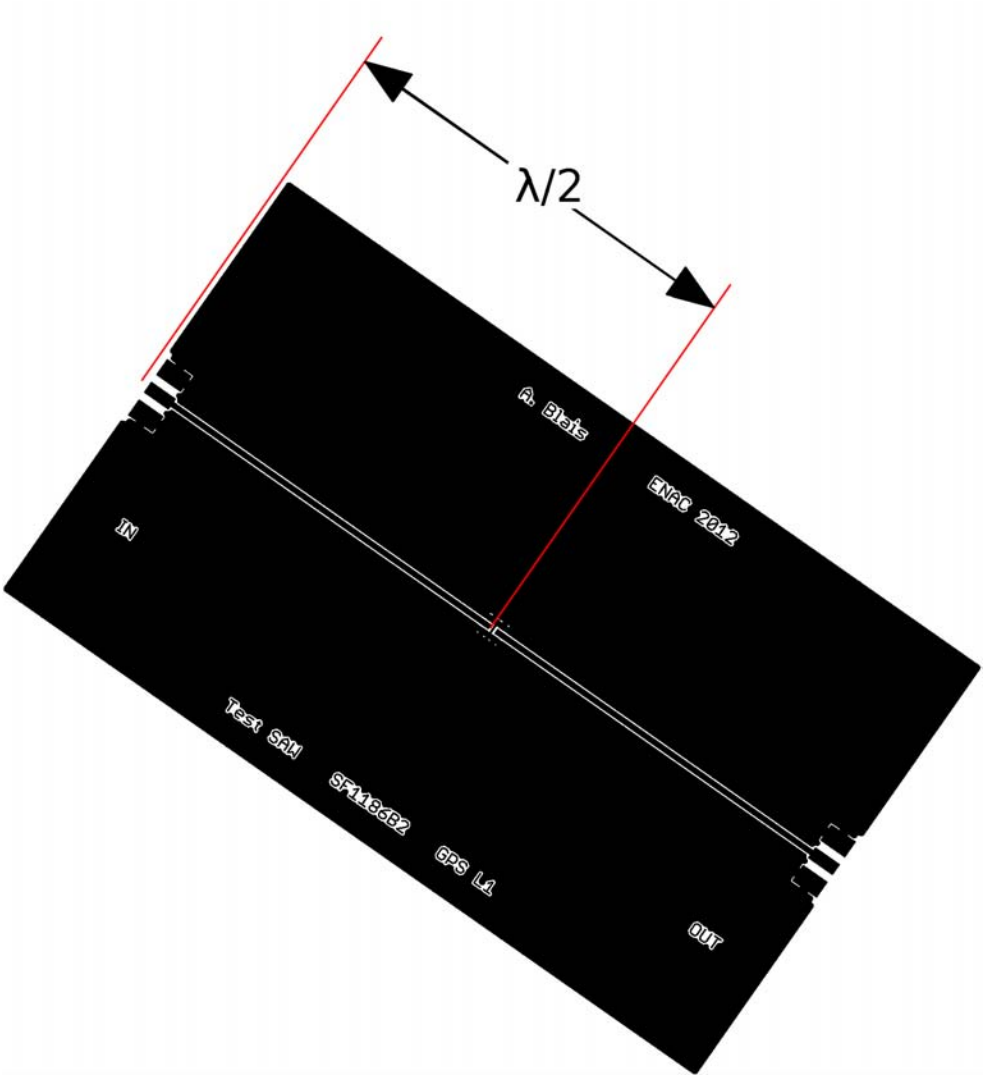

Figure 4.16: SF1186B-2 PCB printout.

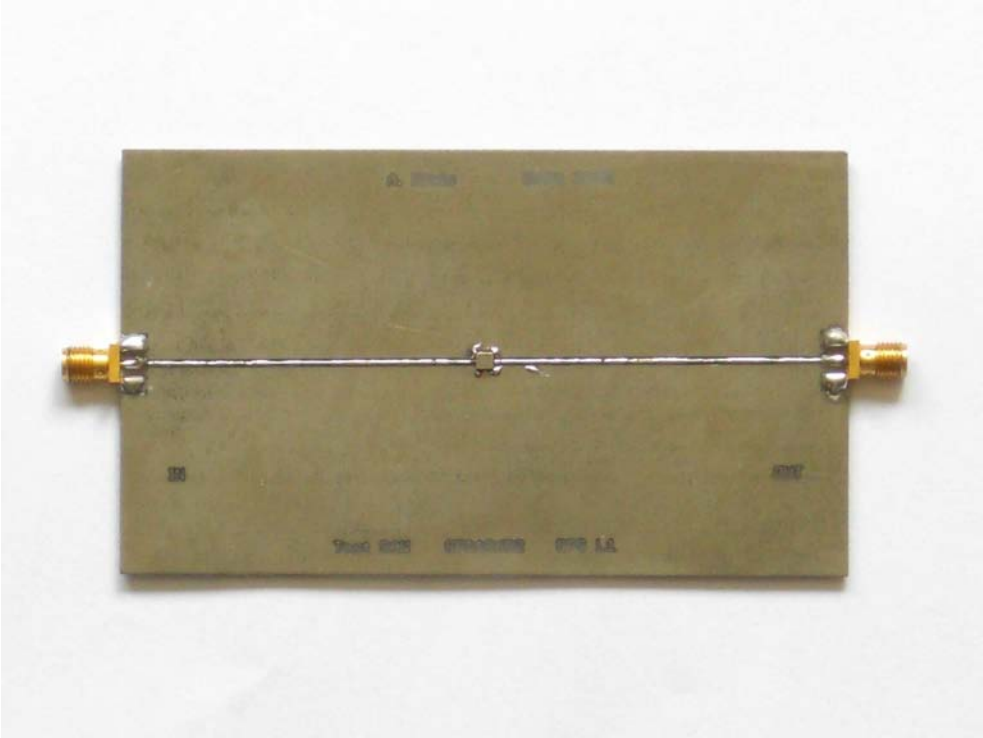

Figure 4.17: SF1186B-2 PCB #1.

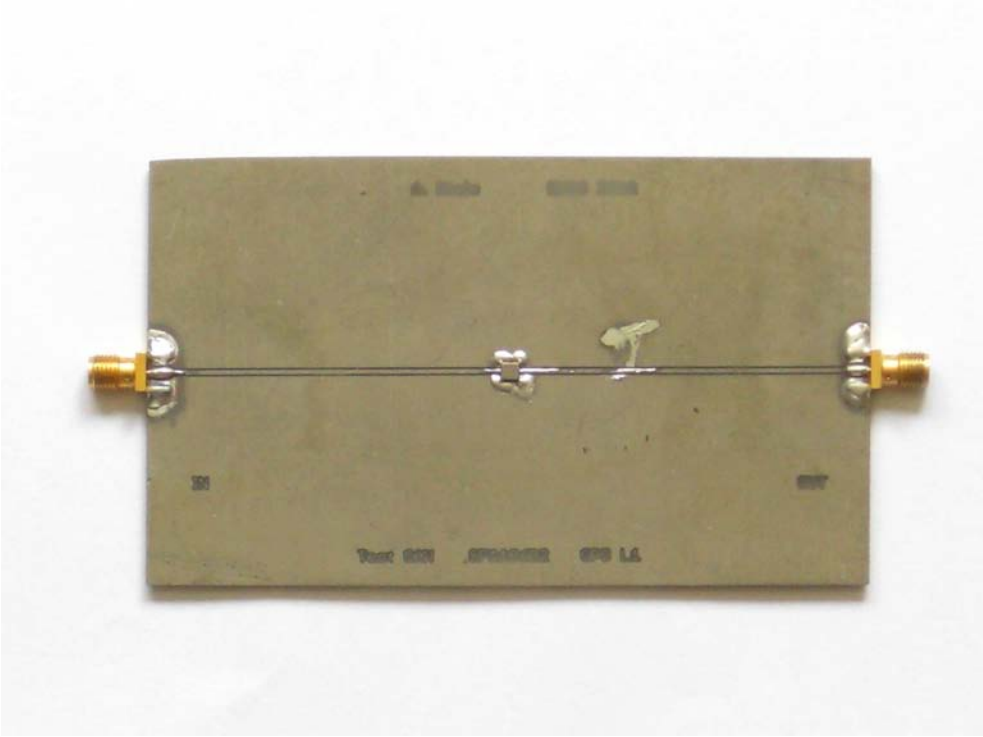

Figure 4.18: SF1186B-2 PCB #2.

Figure 4.19: E5071C network analyzer from Agilent Technologies®.

ure 4.25 is to be compared with figure 4.23 corresponding to the virtual chain of the two PCBs in cascade: the match is excellent. It means that the virtual chaining of the S-parameters is an efficient method to model the expected real performance. It will then be made use of it in the last section of this chapter when it will not be possible to conduct measurement in real condition. What is more figure 4.25 shows that except in the transition bands immediately around the cutoff frequencies, the minimum required attenuation is exceeded. The group delay, plotted in figure 4.26, is not completely flat in the passband but its range of variation is limited to around 25 ns. Although there is no direct requirement about the group delay of the receiver in the Galileo MOPS document [8], this range can be compared to the value specified for the active antenna: its differential group delay shall not exceed 50 ns. A second point of comparison is the requirement found in the GPS MOPS document [9] which specifies less than 150 ns differential group delay variation in the pre-correlation filters for GPS/SBAS receivers. In the light of this elements, the group delay displayed in figure 4.26 seems acceptable.

It must now be verified that the performance established at room temperature is still valid for others.

4.3 Sensitivity to Temperature

Indeed, avionics equipment intended to be installed on board an aircraft must maintain its operational specifications whatever its working conditions, sometimes extreme. It is the purpose of the Environmental

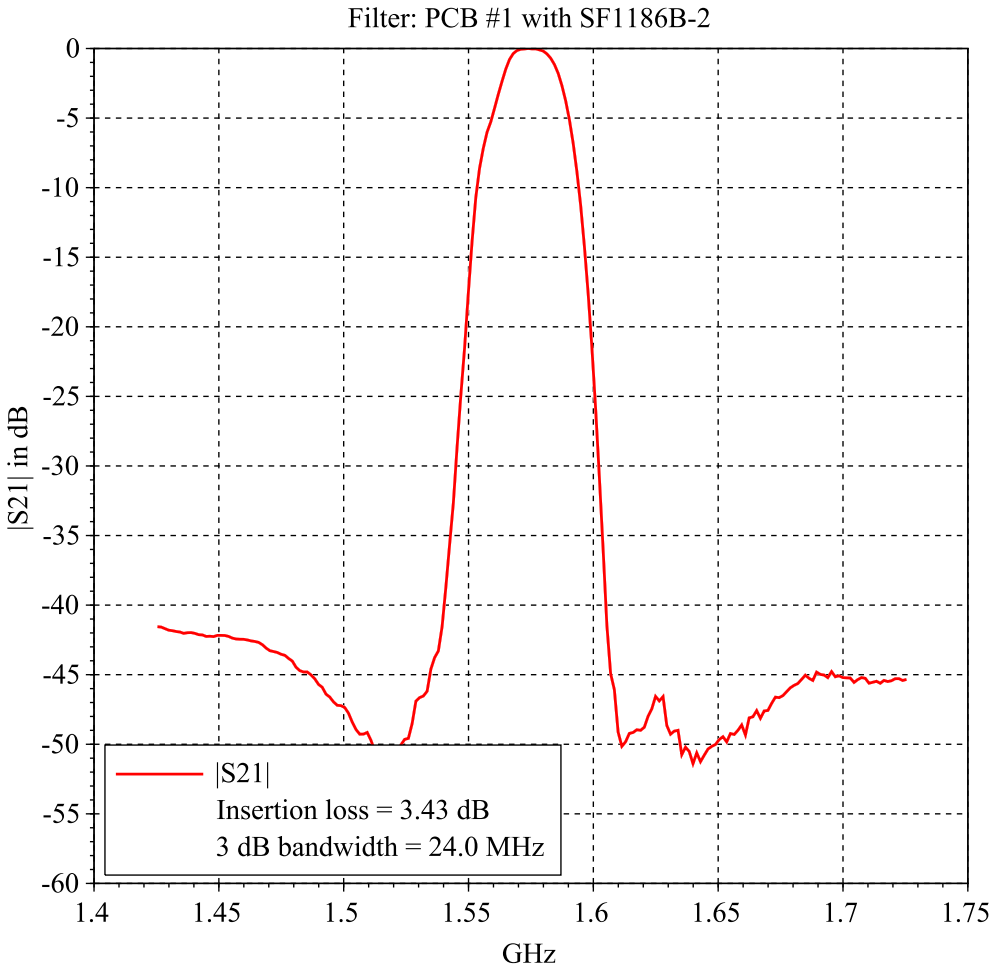

Figure 4.20: $|S_{21}|$ for the SF1186B-2 PCB #1.

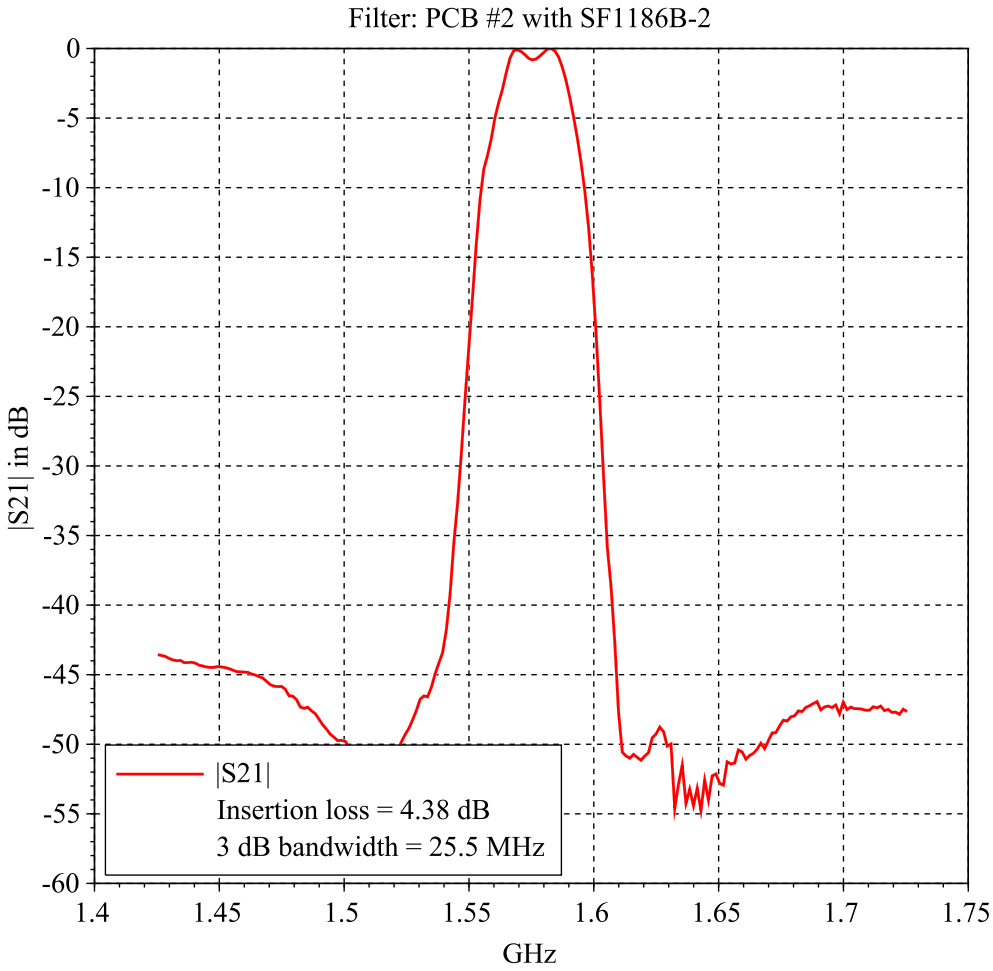

Figure 4.21: $|S_{21}|$ for the SF1186B-2 PCB #2.

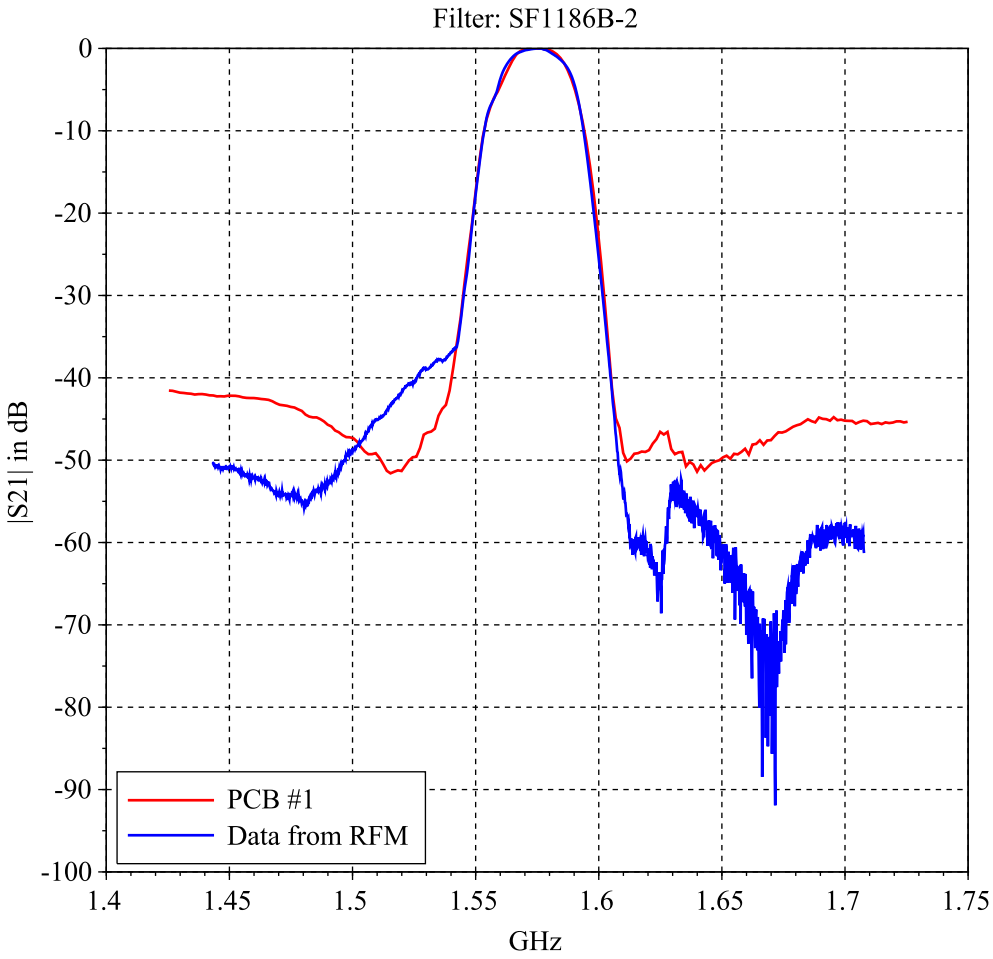

Figure 4.22: Comparison between $|S_{21}|$ measured for PCB #1 and the values from the S2P file [3].

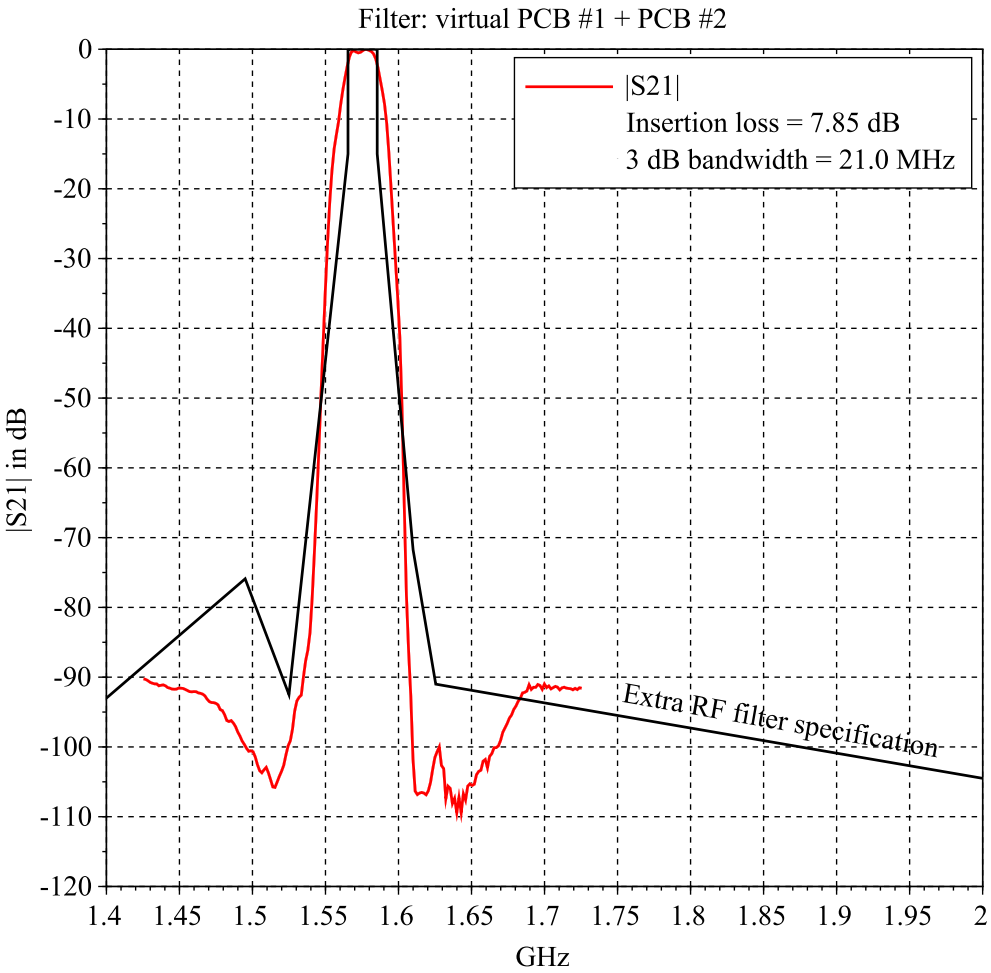

Figure 4.23: $|S_{21}|$ for the virtual chain of PCB #1 + PCB #2 in cascade.

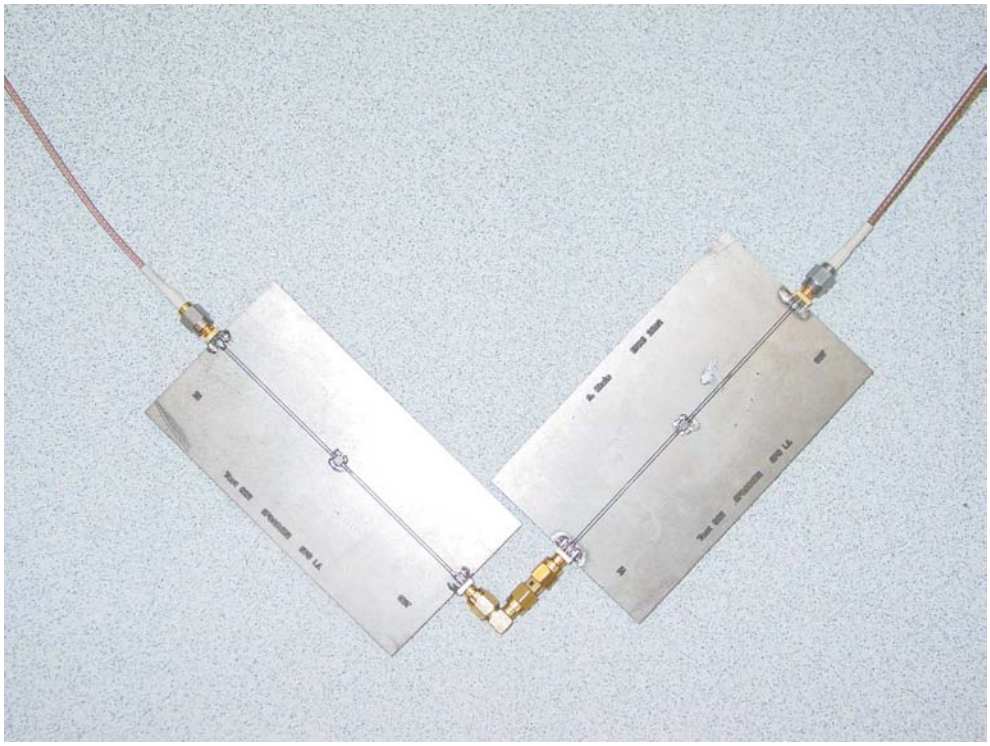

Figure 4.24: Chain of PCB #1 + PCB #2 in cascade.

Conditions and Test Procedures for Airborne Equipment document [10], DO-160 for short, to propose tests to verify this ability of the equipment to ensure its functions under the complete environmental conditions the equipment can encounter. Among all sections of this document, section 4 *Temperature and Altitude* is of concern here, because the characteristics of the filters can change with temperature. Depending on the place (pressurized or not, controlled in temperature or not) in the aircraft where the equipment will be located, the test conditions are more or less severe, possibly reaching an interval of $[-55, +85]\,°C$. An important point to be pointed out here: no forced cooling can be relied upon on board. The designer can only rely on the natural flow of the surrounding air through holes in the equipment case to cool the equipment.

4.3.1 Performance of PCB #1 vs Temperature

Our Lab is not equipped with a temperature test chamber which would be required to test our PCB over the temperature range $[-55, +85]\,°C$. However, using the means at hand, the S-parameters of the PCB #1 were measured at 5 different temperatures. Our test bench was made of the following:

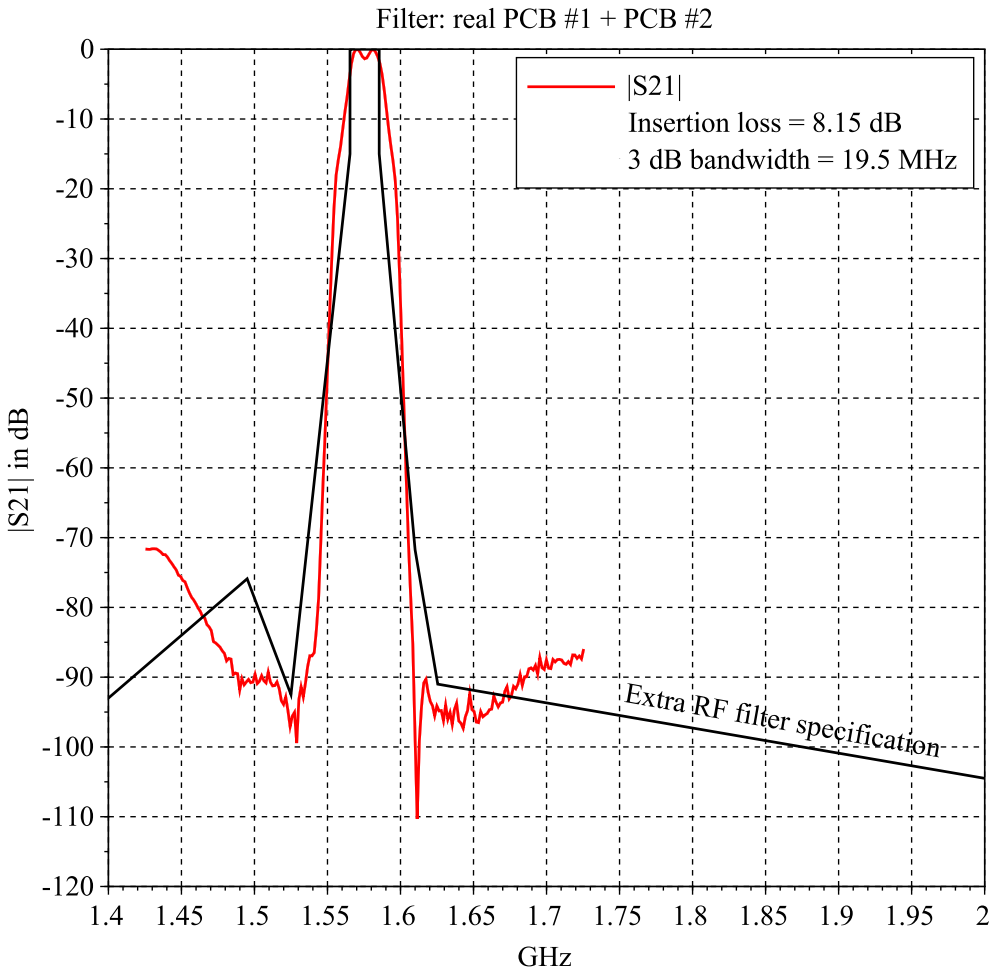

Figure 4.25: $|S_{21}|$ for the chain of PCB #1 + PCB #2 in cascade.

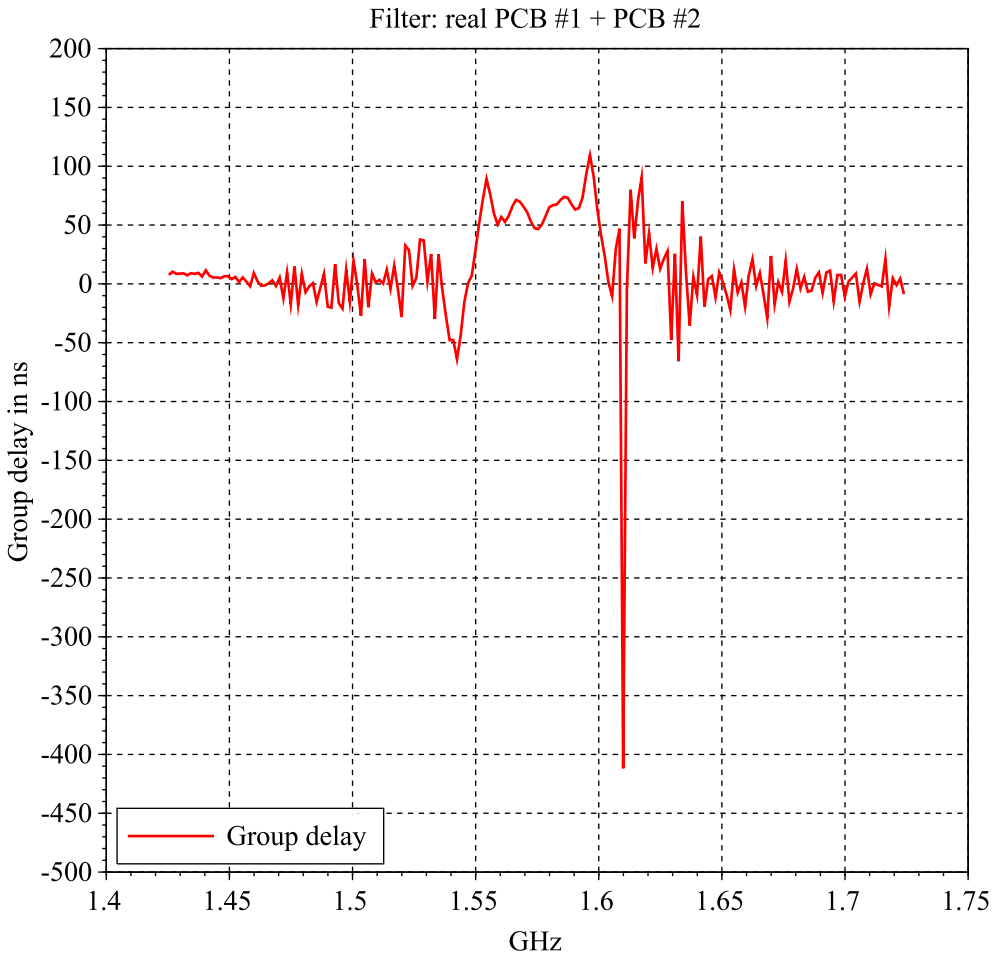

Figure 4.26: Group delay for the chain of PCB #1 + PCB #2 in cascade.

- for temperatures higher than room temperature: the PCB was placed in the center of a cardboard box with two opposite holes. In the upper one hot air was blown at a constant rate, while the size of the lower hole, the output one, was being modulated to set the temperature in the box,
- for temperature lower than in the room: the PCB was introduced in an icebox full of deep-frozen water bottles. The cooling of the board to the minimum temperature took several hours but in counterpart the warming time was also very long, allowing for stable measurements.

Although apparently very limited, these means should provide reliable results as a very long stabilization time was used before each measurement.

Figure 4.27 shows $|S_{21}|$ at the different temperatures for the single PCB n°1. A close-up of the passband is available in figure 4.28. There is a clear shift of more than 5 MHz of the passband. It must be said here that this shift is not only due to the modification of the characteristics of the SF1186B-2 device with temperature, but also to the dilatation of the PCB and the modification of its electrical properties. Furthermore, it is not possible to separate the contribution of the board from the contribution of the filter in this shift. However, it is interesting to note that this observed shift is coherent with the temperature coefficient of $-30\,\text{ppm}/^\circ\text{C}$ given in the datasheet [1]: for a temperature variation of $88 + 10.7 \simeq 100\,^\circ\text{C}$ the theoretical shift equals $-30 * 100 * 1575.42 = -4.7\,\text{MHz}$. Thus it is believed that the main contributor to this shift is the SF1186B-2 filter. In any case, in an industrial process, an other material than FR-4 should be used to build the board. For example, RODGER Corporation RO3000® laminate series could be used as it is much more stable mechanically and electrically in temperature. It also outperforms FR-4 at frequencies of interest from the electrical point of view.

4.3.2 Virtual Chain of the Two PCB in Cascade

Due to our limited means (the icebox was too small), it was not possible at this point to measure $|S_{21}|$ as a function of temperature of the two PCBs in cascade as in section 4.2.4. Only a virtual transfer function could be projected from the S-parameters stored during the tests conducted in section 4.3.1. Figure 4.29 and its close-up 4.30 show the same clear shift of more than 5 MHz of the passband, that is a quarter of the useful bandwidth. This is not acceptable.

To solve this drift in temperature, one solution would be to use filters with a lower temperature coefficient. The SAW (or BAW)

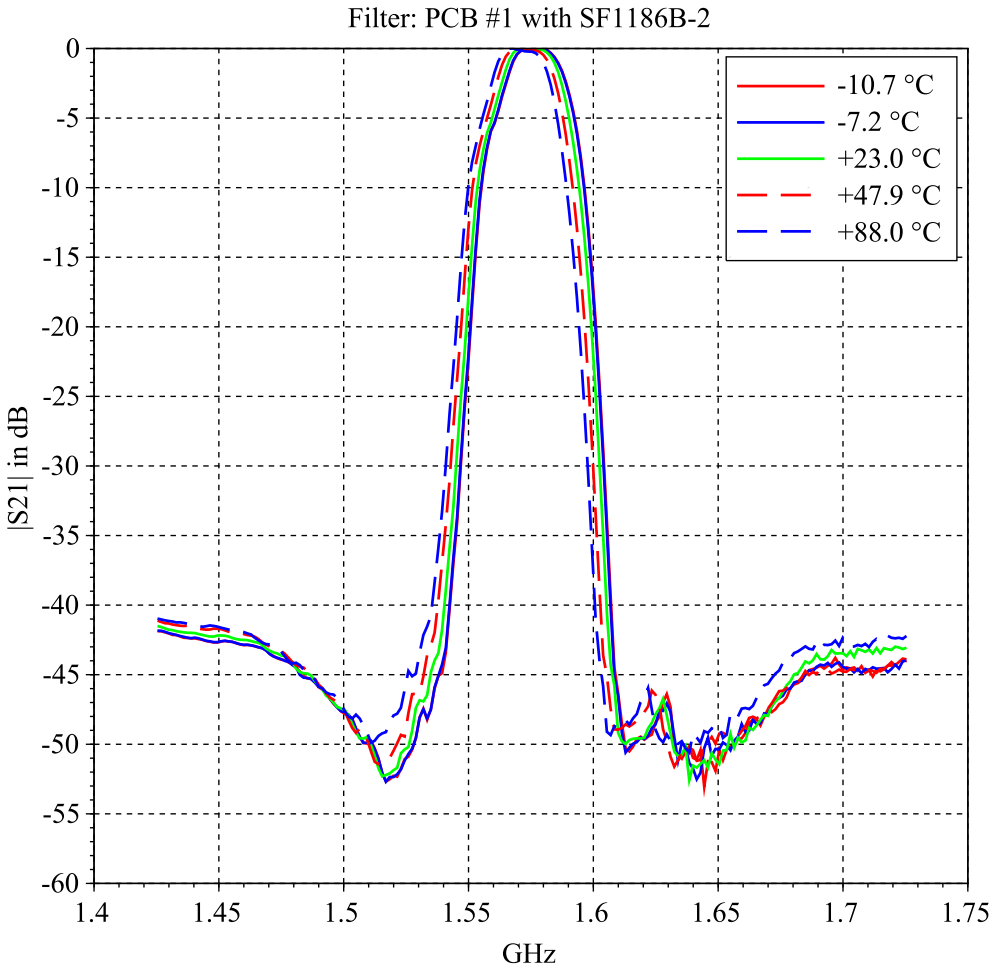

Figure 4.27: $|S_{21}|$ for the SF1186B-2 PCB #1, temperature curves.

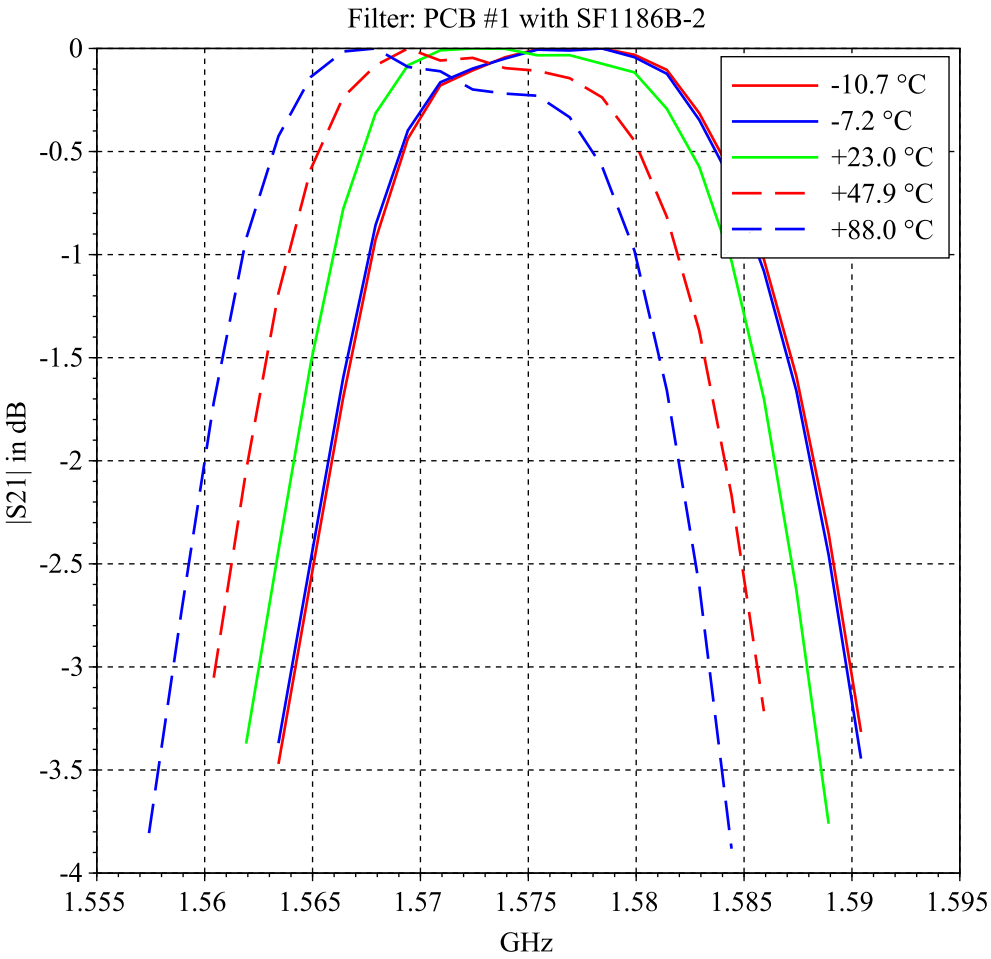

Figure 4.28: $|S_{21}|$ for the SF1186B-2 PCB #1, temperature curves, close-up.

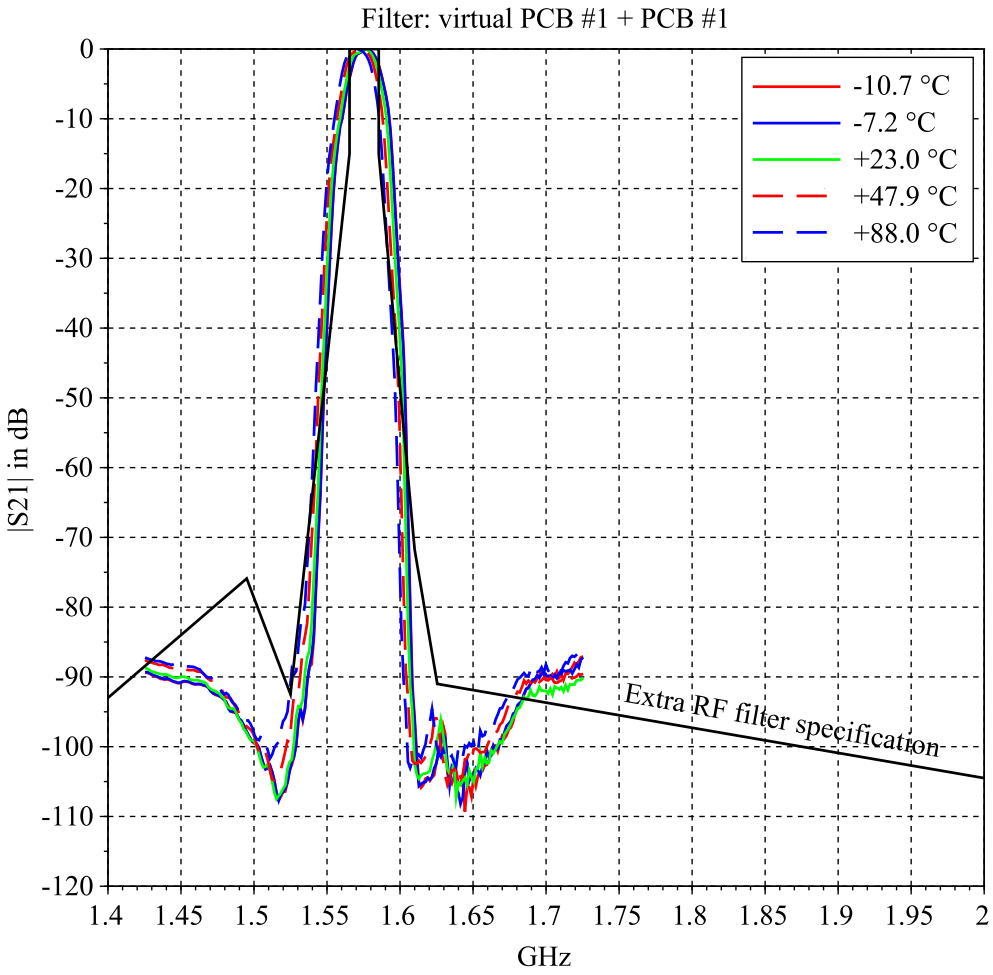

Figure 4.29: $|S_{21}|$ for the virtual chain of two PCBs #1 in cascade, temperature curves.

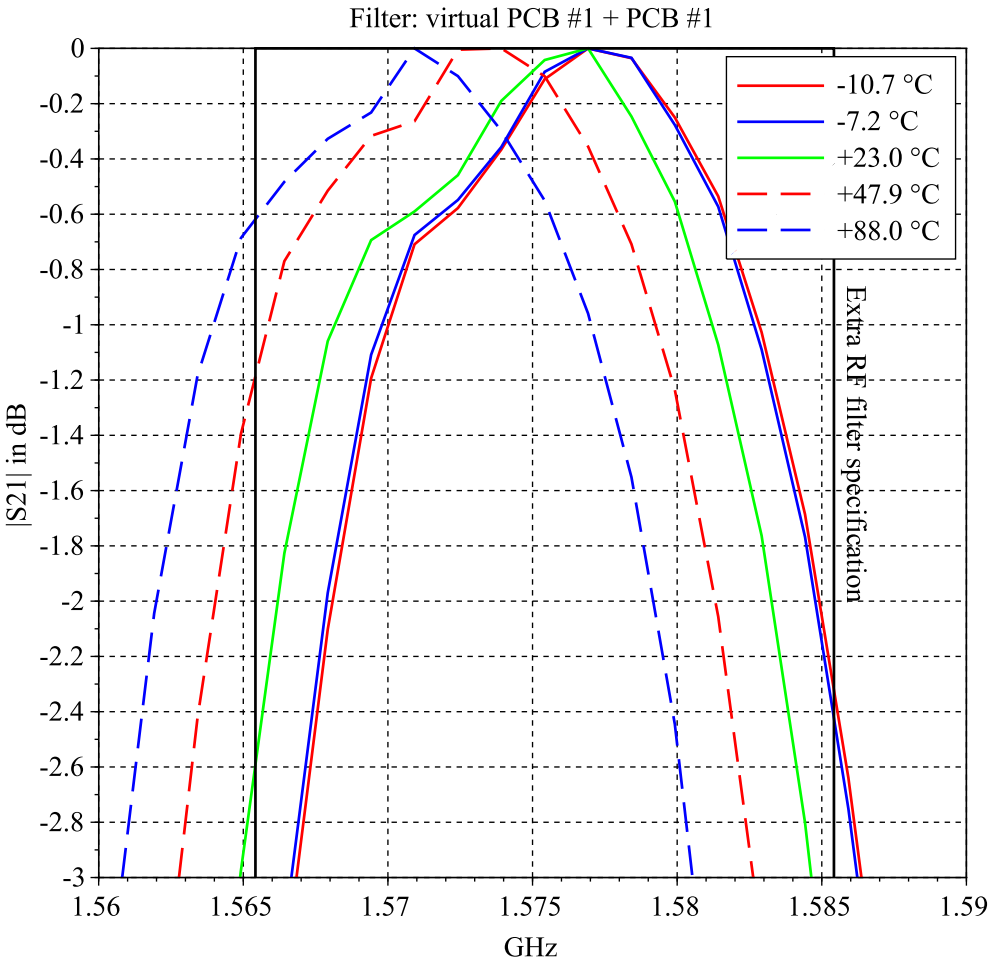

Figure 4.30: $|S_{21}|$ for the virtual chain of two PCBs #1 in cascade, temperature curves, close-up.

technology is limited to a floor of around $-10\,\text{ppm}/^\circ\text{C}$ at the time of this writing, which would decrease the previous theoretical shift to $-10 * 100 * 1575.42 = -1.6\,\text{MHz}$, a more acceptable value. Another solution would be to use a custom-designed filter with a center frequency equals to 1575.42 MHz at the maximum operating temperature, $+85\,^\circ\text{C}$, and to maintain the component at this temperature during operation, heating it more or less as needed.

4.4 Conclusion

In this chapter, the feasibility of the extra RF filters, needed by both coherent and separate sampling architectures proposed in chapter 3, has been assessed. Concerning the E1 band, in the light of the presented measurements, it can be considered that with carefully chosen SAW filters, not imposed as here, the required extra RF filters are feasible: the minimum required attenuation could be verified nearly everywhere in frequency, even if the behavior in temperature should receive special attention. Of course, a digital filter will be required after digitization where the specified attenuation is not completely reached. This point is studied in chapters 7 and 8. The group delay variations seem contained in acceptable limits also. What is more, there is no reason for this conclusion, established for the E1 band, not to be valid for the E5a band. One can anticipate although that, as the transition slopes are steeper as shown in figure 3.3 and 3.11, the order of the needed digital filter will be higher.

4.5 References

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5 Sampling Jitter

This chapter studies the impact of the sampling clock jitter on the signal phase measurement in the receiver. A model of this specific form of jitter is established in the first part of this chapter and simulation results about the phase measurement error at the output of the PLL are then presented in a second and last part. It was decided to focus on the phase tracking function of the receiver as it is much more sensitive than the DLL (Delay-Locked Loop).

5.1 Two Kinds of Jitter

In an ADC, the sampling operation is triggered by the crossing of a threshold by the rising or falling edge of a clock signal, as represented in figure 5.1 where the rising edge is assumed (as in the rest of this chapter) without loss of generality. T_s denotes the sampling period and $\{t_n = nT_s, n \in \mathbf{Z}\}$ the set of ideal sampling times. Due to noise, the clock signal does not cross the threshold at exactly equally spaced $\{t_n\}$ but at some $\{\tilde{t}_n\}$, thus introducing a bias in the sampling operation: this phenomenon is called sampling jitter. Sampling jitter must be taken into account when designing a Direct Sampling Receiver because the sampled frequencies are, by definition, much higher than in classical architectures where digitization occurs at relatively low Intermediate Frequencies. It means that, in Direct Sampling receivers, the slope of the input signal is proportionally so high that a small deviation of the sampling time can induce a large error in amplitude [1] as drawn in figure 5.2. Depending on the type of noise, a distinction is made on the type of the resulting jitter.

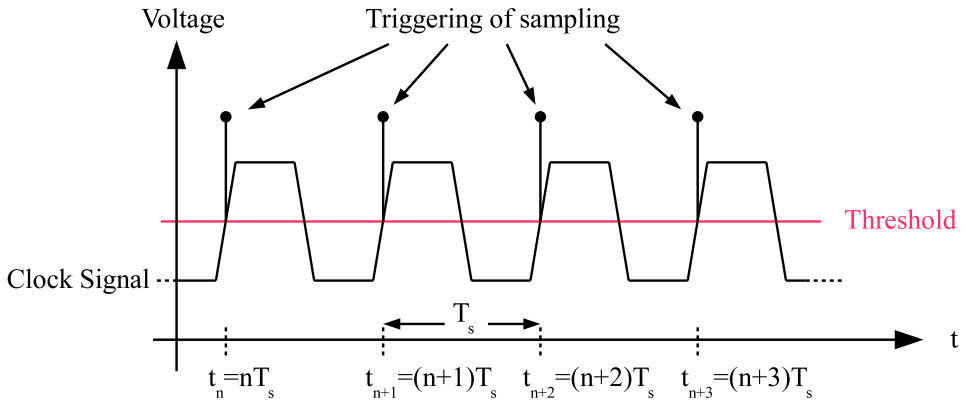

Figure 5.1: Triggering of sampling by threshold crossing of a noise-free clock.

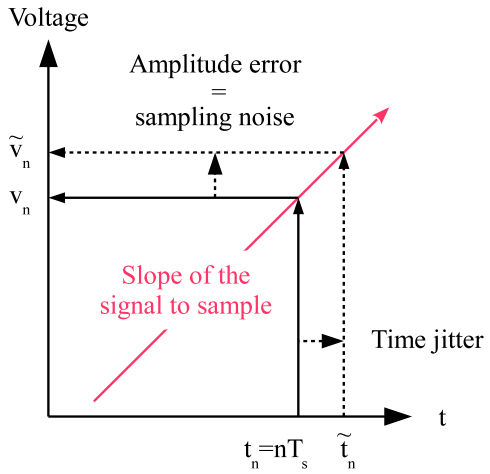

Figure 5.2: Illustration of timing jitter that produces sampled amplitude error [2].

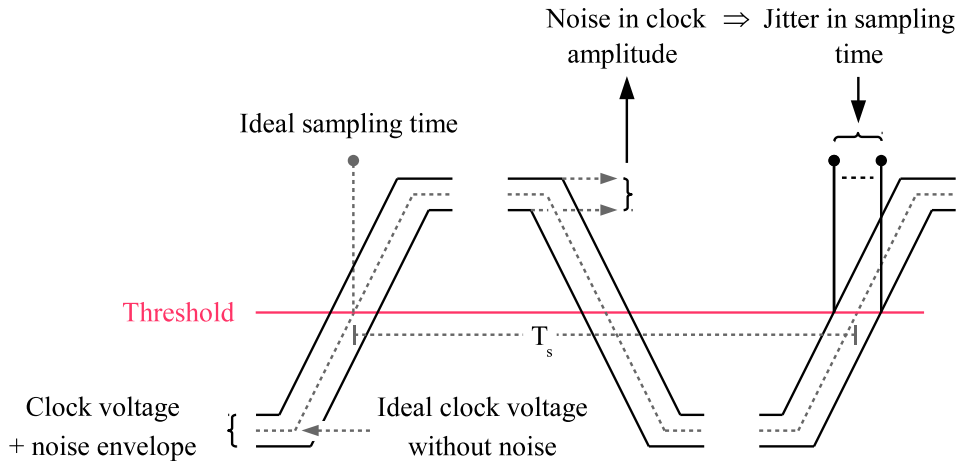

Figure 5.3: Noise on the amplitude of the clock induces jitter in the sampling time.

5.1.1 Aperture Jitter

This jitter is due to the noise which adds to the amplitude of the clock, such as the thermal noise of the ADC. Figure 5.3 shows how this amplitude noise contribution moves the sampling time away from its ideal position, because of the slope of the clock. This type of jitter has been extensively studied in general as in [3] or [4] for example, and in the particular case of GNSS receivers in [5] which uses a simple sinusoidal model for the GNSS signal, in [6] which modifies the former model by assuming a BPSK modulation, in [7] which extends the two previous works to multiple band GNSS software receiver, in [8] where the new QPSK and BOC(n,n) navigation signal types are dealt with and more recently in [9] which provides aperture jitter effect measurements in a RF-DS-SDR real-time GPS L1 receiver. The main result of these later works is that the aperture jitter can be modeled at the correlator output as an additive white noise independent of the other sources of noise. Hence it should be taken into account as a degradation of the link budget. The acceptable limit of this degradation then sets the required performance of the ADC as a consequence. This topic won't be developed in this thesis because it can be considered that the work has been done in the herebefore cited references [5], [6], [7] and [8].

5.1.2 Clock Jitter

The clock, which periodically triggers the ADC, is built on an underlying oscillator which is also subject to electronic noise. Let $x_s(t)$ be the

noiseless ideal periodic signal expected at the output of this oscillator. For example a sinusoidal waveform with fundamental frequency F_s

$$x_s(t) = \sin(2\pi F_s t). \tag{5.1}$$

As $x_s(t)$ is periodic, its phase can be defined

$$\psi(t) = 2\pi F_s t. \tag{5.2}$$

However, instead of this ideal model, the output waveform of a real oscillator should be modeled, as proposed in [10], by

$$x(s(t)) = x_s(s(t)) + y(s(t)) \tag{5.3}$$

where

- $y(.)$ represents the additive distortion in the amplitude domain,
- $s(t) = t + j(t)$ models the distortion in the time domain, with $j(t)$ defined hereafter.

Both perturbations mainly find their origin in the thermal noise which is inherently present in any electronic device. From now on, this chapter will focus on the time perturbation $j(t)$, as $y(.)$ can be taken into account in the aperture jitter presented previously.

5.1.2.1 Clock Phase Jitter Model

As $x_s(t)$ is a periodic signal, the jitter term $j(t)$ can be expressed in a more expressive way as a phase deviation

$$j(t) = \frac{T_s}{2\pi}\phi(t). \tag{5.4}$$

This gives in our example

$$x_s(s(t)) = \sin(2\pi F_s t + \phi(t)). \tag{5.5}$$

Over the time interval $[t_1, t_2]$, the phase deviation results from the motion of numerous i.i.d. (Independent and Identically Distributed) charge carriers, such as the electrons, and thus can be modeled, according to the Central Limit theorem, as a Gaussian random variable [11]. What is more, $\forall t_1, t_2, t_3, t_4$ such that $0 \leq t_1 \leq t_2 \leq t_3 \leq t_4$, the assumption can be made that $\phi(t_2) - \phi(t_1)$ and $\phi(t_4) - \phi(t_3)$ are independent random variables. Thus, by extension, the phase deviation $\phi(t)$ can then be modeled as a Brownian motion or non-stationary Wiener process [12], and described by the following integral [10]

$$\phi(t) = \frac{2\pi}{T_s}\sqrt{c}\int_0^t w(u)du \tag{5.6}$$

where $w \sim \mathcal{N}(0,1)$ and $w(t)$ and $w(t+\tau)$ are independent random variables $\forall t \neq 0$. It must be noted that by nature $\phi(t)$ is an unbounded process. The constant c is the variance of $j(t)$, in units of s. It is a characteristic of the oscillator which can be measured from the oscillator phase spectrum as proposed in [13] or [14]. For modern integrated oscillator [1] c is in $[10^{-19}, 10^{-21}]$ s while TCXO (Temperature Controlled Crystal Oscillator) and OCXO (Oven Controlled Crystal Oscillator) can reach 10^{-25} s as written in [15].

5.1.2.2 Calculation of the Jittered Sampling Time

The objective of this chapter being to assess the effect of the sampling clock jitter on GNSS signal phase measurement, it is necessary to derive a model of the jittered sampling time $\{\tilde{t}_n\}$ from the model of the jittered clock, as proposed in [14]. If a noisy clock as described by equation (5.5) is used to trigger the ADC by threshold crossing (zero for simplicity), crossing $\#n$ will occur at time $\tilde{t}_n$ such that in equation (5.5):

$$2\pi F_s \tilde{t}_n + \phi\left(\tilde{t}_n\right) = 2\pi n. \tag{5.7}$$

The next crossing will occur at time $\tilde{t}_{n+1}$ such that:

$$2\pi F_s \tilde{t}_{n+1} + \phi\left(\tilde{t}_{n+1}\right) = 2\pi (n+1). \tag{5.8}$$

Subtracting the two equations (5.7) and (5.8) yields:

$$\tilde{t}_{n+1} = \tilde{t}_n + T_s - \frac{\phi\left(\tilde{t}_{n+1}\right) - \phi\left(\tilde{t}_n\right)}{2\pi F_s} \tag{5.9}$$

According to equation (5.6):

$$\frac{\phi\left(\tilde{t}_{n+1}\right) - \phi\left(\tilde{t}_n\right)}{2\pi F_s} = \sqrt{c} \int_{\tilde{t}_n}^{\tilde{t}_{n+1}} w(u)du. \tag{5.10}$$

If the time jitter is small in comparison to the period T_s, this integral with fluctuating limits can then be approximated by an integral with constant limits

$$\int_{\tilde{t}_n}^{\tilde{t}_{n+1}} w(u)du \sim \int_0^{T_s} w(u)du \forall n \sim \mathcal{N}\left(0, T_s\right) \forall n \tag{5.11}$$

1. If a synthesizer using a PLL is needed to reach the sampling frequency, from the clock fundamental frequency, the frequency ratio of the PLL should be taken into account to calculate the *final* c: it is increased by the frequency ratio.

as $\phi(t)$ is a Wiener process, that is a process with stationary increments. Thus the jittered sampling times can be generated by using the iterative formula

$$\tilde{t}_{n+1} = \tilde{t}_n + T_s - \Delta T_s,\ \Delta T_s \sim \mathcal{N}\left(0, cT_s\right) \forall n \tag{5.12}$$

with $\tilde{t}_0$ as the initial sample point, set to 0 without loss of generality.

The direct expression of $\tilde{t}_{n+1}$ can be elaborated from equation (5.9), taking into account that $\phi\left(\tilde{t}_{j+1}\right) - \phi\left(\tilde{t}_j\right)$ and $\phi\left(\tilde{t}_{i+1}\right) - \phi\left(\tilde{t}_i\right)$ are independent random variables $\forall i \neq j$ as noted in section 5.1.2.1:

$$\tilde{t}_{n+1} = (n+1)T_s - \Delta T_s^{(n)},\ \Delta T_s^{(n)} \sim \mathcal{N}\left(0, (n+1)cT_s\right). \tag{5.13}$$

Equation (5.13) shows clearly that $\tilde{t}_{n+1}$ is not a stationary process, its variance increasing linearly with time. It is thus believed that it is not possible to write an analytical model of a signal, sampled with this kind of jitter, which could be used to assess the effect of the sampling clock jitter on the receiver performance. It was then decided to proceed by simulation, using equation (5.12) to calculate the actual times at which the signal has to be sampled.

For the sake of completeness, it should be noted, however, that for timing services purposes, the GNSS receiver is able to use the estimated GNSS navigation solution to reduce the drift of its local oscillator with respect to GNSS system time. Then, the clock error, with respect to GNSS time, does not accumulate using clock steering schemes. In that case, the deviation with respect to system time can be modeled as a zero mean gaussian. For PPS (Pulse Per Second) output production for example, this is the error between the actual PPS edge and the absolute correct PPS edge. In the rest of this thesis, only free running GNSS receiver clock schemes will be considered.

5.2 Effect of Sampling Clock Jitter on Signal Phase Measurement

To study the effect of sampling clock jitter on GNSS signal phase measurement, two software modules were developed during this PhD: a L1 C/A signal generator and a software receiver, dedicated to L1 C/A signal processing in a first step. It is noteworthy that the two programs are designed for the L1 C/A signal instead of the E1 signal as many more results are available for the GPS signal, allowing a more reliable validation of the code. Moreover, as the L1 C/A signal is known to be less robust than the other GPS or Galileo civil signals, the results based on it can then be considered as worst bounds.

5.2.1 L1 C/A Signal Generator

This software module has been written, from scratch, in the C language. It is able to generate, directly at the jittered sampling times, a single L1 C/A signal disturbed in amplitude by white noise. The model used for the L1 C/A signal is a derivation of the one found in [16], with a simple Doppler effect implementation

$$\begin{cases} x(\tilde{t}_n) = \sqrt{2C} D_i \left(\lambda(\tilde{t}_n)\right) XG_i \left(\lambda(\tilde{t}_n)\right) \cos\left(\omega_1 \lambda(\tilde{t}_n)\right) + n(\tilde{t}_n) \\ \lambda(t) = (t_d - \tau_d) + (t - t_d)(1 + f_D/f_1) \end{cases} \tag{5.14}$$

where

- x is the composite output signal,
- $\lambda(t)$ is the time of emission (by the SV) of the signal received at time t (by the receiver),
- $\tilde{t}_n$ is the jittered sampling time, modeled in section 5.1.2.2 and characterized by the constant c,
- C is the power of the L1 C/A navigation signal,
- D is the navigation message. In the real L1 C/A signal it is organized in frames of 1500 bits each with a 50 bits/s rate. In this implementation it is absent,
- i is the SV number,
- XG is a SV-unique periodic spreading code, a Gold sequence of 1023 bits for a 1 ms period,
- $\omega_1 = 2\pi f_1$ is the L1 carrier angular frequency, with $f_1 = 1575.42\,\text{MHz}$,
- n is the receiver thermal noise signal, characterized by its single-sided PSD level $N0$,
- τ_d is the propagation delay between the SV and the receiver at time t_d,
- f_D is the Doppler shift observed by the receiver at time t_d. It is constant in time in this implementation,
- t_d is the time at which the signal begins. For the sake of simplicity, it is set automatically to the multiple of 1 ms immediately greater than τ_d.

The following parameters are configurable: *C/N0* ratio, SV number, Doppler shift, propagation delay and constant c. The length of the signal can be set arbitrary. To be noted also, this software module uses the GSL (GNU Scientific Library) to produce highly random numbers for thermal noise and jitter generation.

5.2.2 L1 C/A Software Receiver

This second software module has also been written in the C language, from a previous internal development by *Christophe Macabiau* and *Domnole Boulou*. The initial code has been improved, notably through the use of the GSL for accurate statistical computation, but more important it has been fully instrumented so that all the main acquisition and tracking observables and controls are logged to files. Knowing the SV number, the propagation delay τ and the Doppler shift f_D, this software receiver is able to directly track [2] the signal produced by the L1 C/A signal generator described in section 5.2.1, without a full acquisition step. More exactly, after a transition period where a FLL (Frequency Locked Loop) is used for initial acquisition and then disconnected, tracking is done using a classical dual DLL-PLL architecture. The DLL and PLL models used in this software module are drawn in figures 5.4 and 5.5 respectively. The FLL model is not presented as it is less important, the FLL not being used after the transition period.

The main observables and controls of each loop are systematically plotted as a function of time from the log files, to verify the effectiveness of the tracking. Examples of such plots are presented in figure 5.6 for the DLL and in figure 5.7 for the PLL. The names of the plotted variables are self explanatory. Note that the I and Q channels represent the Integrate and Dump process, this explains the sawtooth shape. Among all these observables and controls, two are more focused on in the rest of this chapter, as they are efficient figures of merit to assess the influence of the sampling clock jitter on signal tracking:

- the signal phase measurement error, as the phase is the most sensitive parameter in signal tracking. The phase measurement error is the difference between the phase of the PLL and the instantaneous phase of the signal produced by the generator, which is known by construction. An example of a plot of the phase measurement error can be found in figure 5.8,

2. It is important to say that, as this software receiver is dedicated to the study of the sampling jitter effect, no pre-correlation filter was implemented so as to directly observe the sampling clock jitter effect.

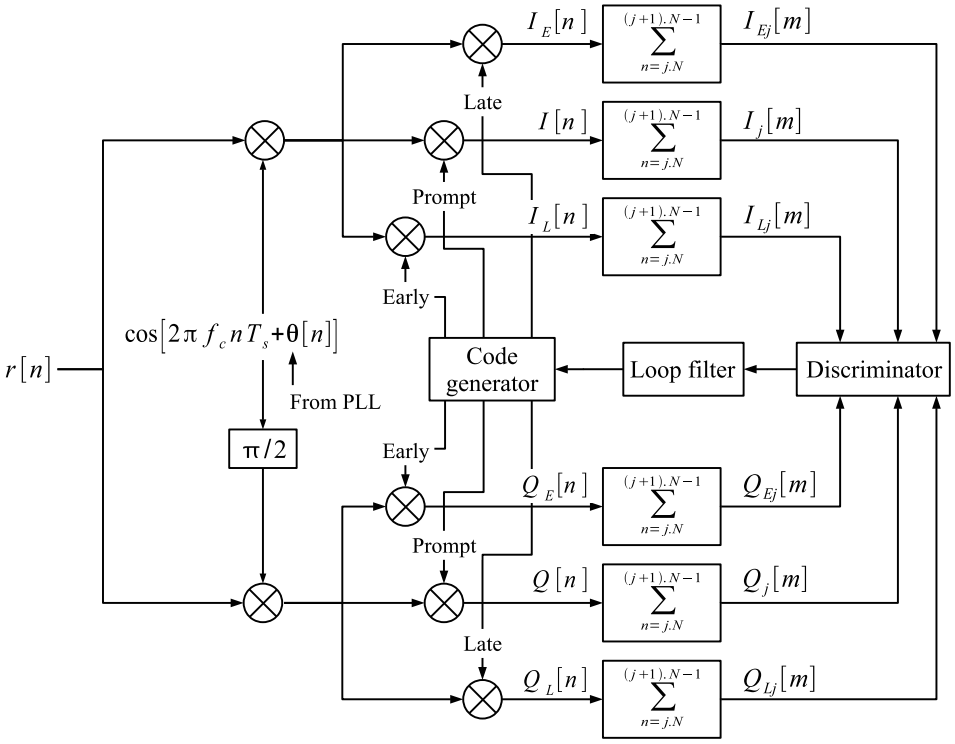

Figure 5.4: DLL model [17].

- the *C/N0* ratio, as it is a global indicator of signal quality. Figure 5.8 also shows an example of a *C/N0* ratio plot.

5.2.3 Simulation Conditions

It must be clarified that each point of the curves shown in the rest of this chapter is the average of at least 2000 measurements counted as follows

1. each run of the signal generator – software receiver pair lasts for 5 s, which corresponds to a minimum of 250 correlator outputs (when the coherent integration time of the receiver $T_p = 20$ ms). To let the PLL enter its steady state, only the last 200 measurements were used,

2. at least 10 independent runs were done with random SV number, Doppler shift and propagation delay.

What is more, unless stated otherwise:

- the sampling frequency is set to $F_s = 40.138$ MS/s,

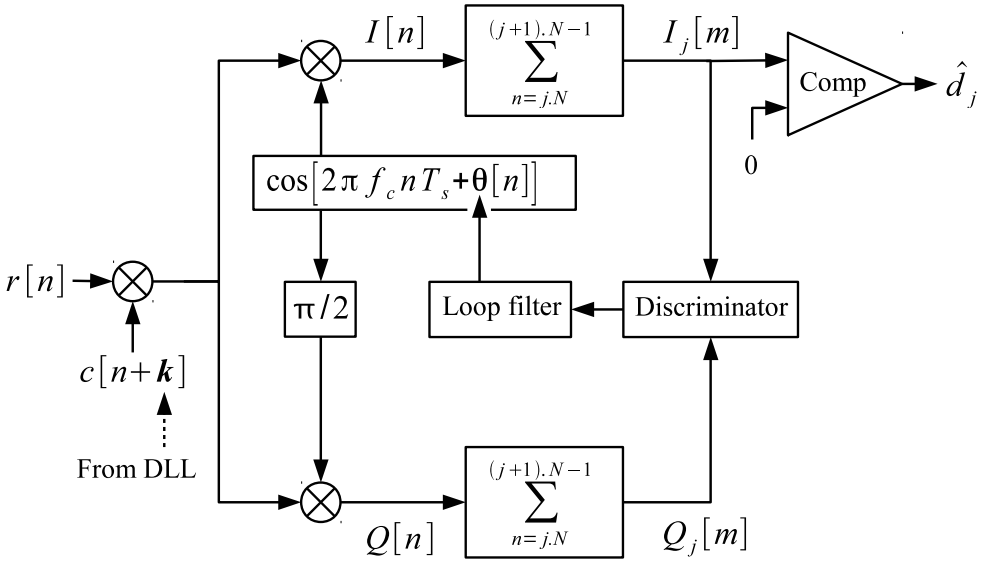

Figure 5.5: PLL model [17].

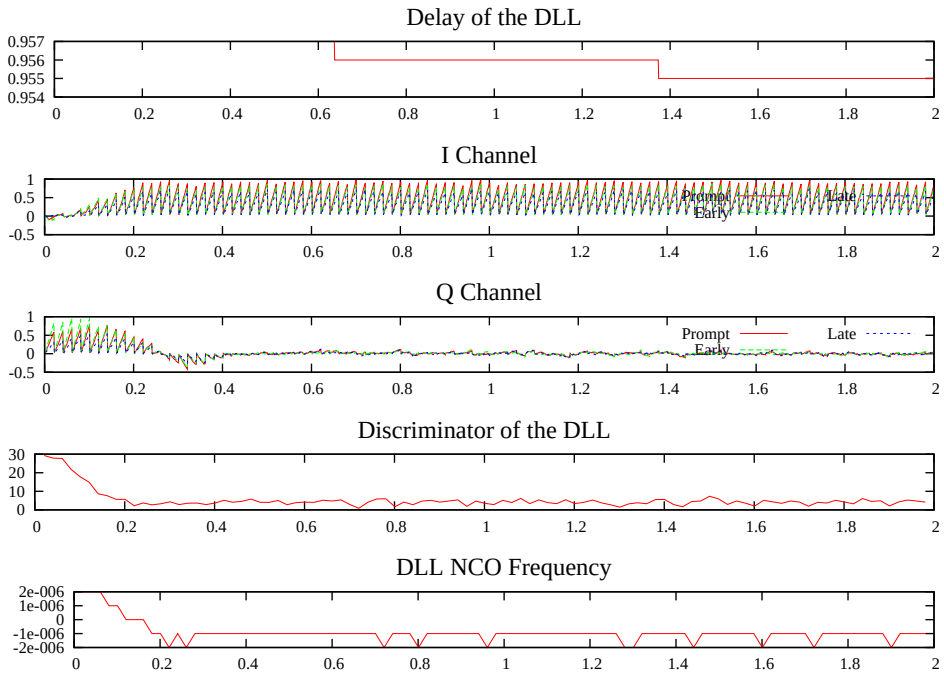

Figure 5.6: DLL observables and controls.

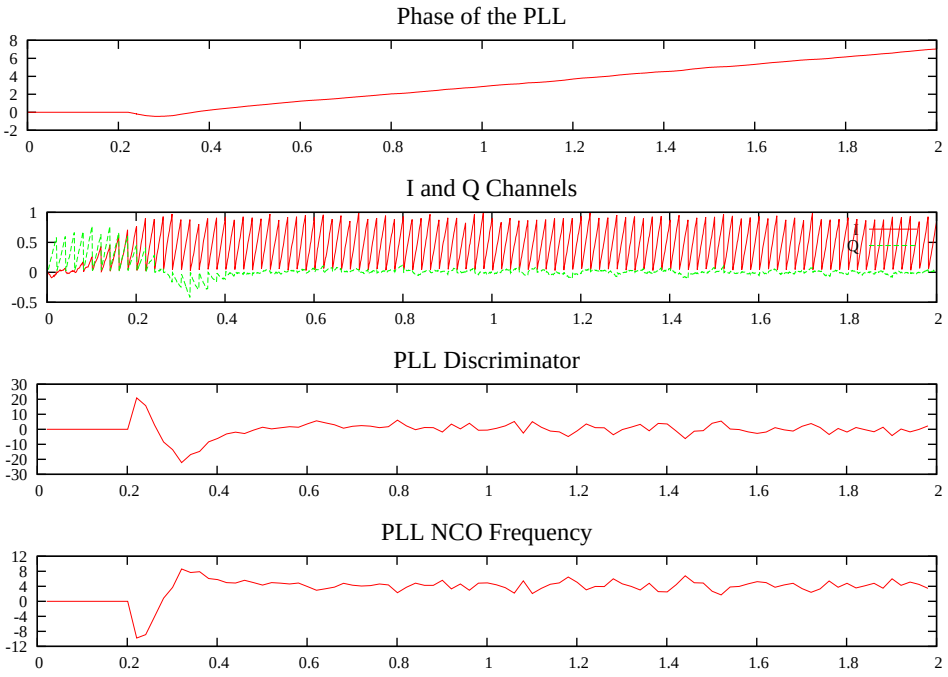

Figure 5.7: PLL observables and controls.

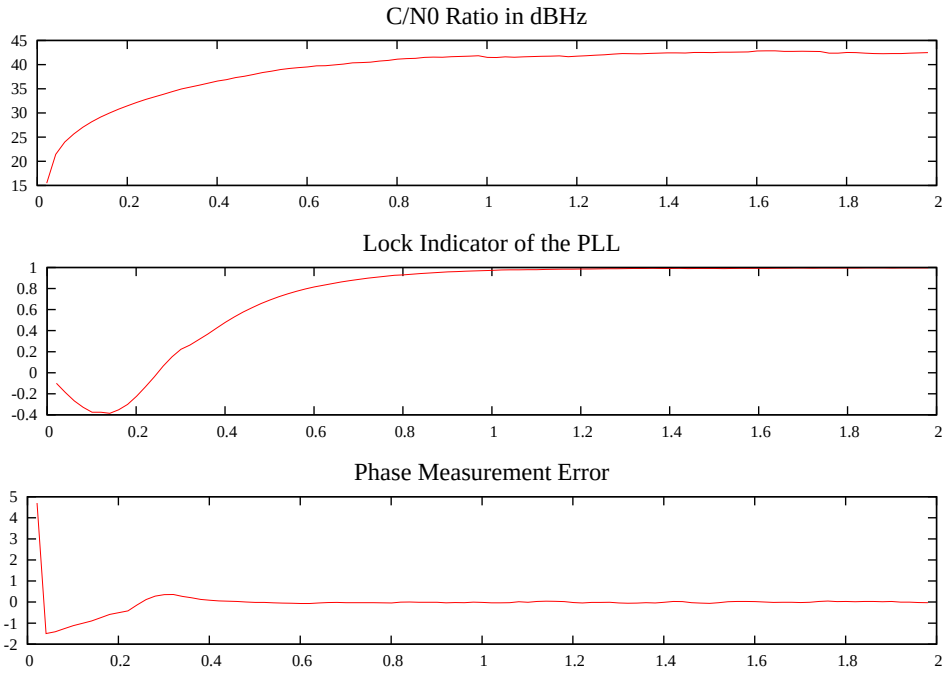

Figure 5.8: Global tracking observables and controls.

- the coherent integration time of the receiver (PLL and DLL) is set to $T_p = 20\,\text{ms}$,
- the noise equivalent bandwidth of the PLL is set to $B_l = 10\,\text{Hz}$.

5.2.4 Signal Generator – Software Receiver Validation

A dry-run was done without jitter to validate the two programs. The phase measurement error standard deviation was measured at the output of the PLL in the *C/N0* range $[24, 56]\,\text{dBHz}$. As a reminder, if $\Delta\phi[n]$ denotes the phase measurement error of the receiver at the output of the PLL at time $t = nT_s$, its variance, that is the squared standard deviation is

$$\sigma_\Delta^2 = E\left[(\Delta\phi[n] - E\left[\Delta\phi[n]\right])^2\right] \text{ in } (\text{rad})^2. \tag{5.15}$$

This statistic is estimated in our software, using N samples $\Delta\phi[n]$, by

$$\hat{\sigma}_\Delta^2 = \frac{1}{N-1}\sum_{\forall i}(\Delta\phi[i] - \hat{\mu}_\Delta)^2 \tag{5.16}$$

where $\hat{\mu}_\Delta$ is the estimator of the expected value $E\left[\Delta\phi[n]\right]$

$$\hat{\mu}_\Delta = \frac{1}{N}\sum_{\forall i}\Delta[i] \tag{5.17}$$

The results are presented in figure 5.9 for three different sampling frequencies. The curves show good accordance to two theoretical bounds found in the scientific literature

$$\sigma_\Delta = \sqrt{\frac{B_l}{C/N0}} \text{ in rad [18]} \tag{5.18}$$

$$\sigma_\Delta = \sqrt{\frac{B_l}{C/N0}\left(1 + \frac{1}{2T_p\,C/N0}\right)} \text{ in rad [19]} \tag{5.19}$$

However a discrepancy can be noted for decreasing sampling frequencies and low *C/N0*. The source(s) of the difference was not found. It could possibly be proposed the hypothesis that, as the signal generator directly calculate a digital signal without band limitation, this is due to aliasing. In any event, as all three curves visibly match the bounds for high values of *C/N0*, it is satisfactory as most of our measurements to come that will be done with no additive noise, that is $C/N0 = 100\,\text{dBHz}$.

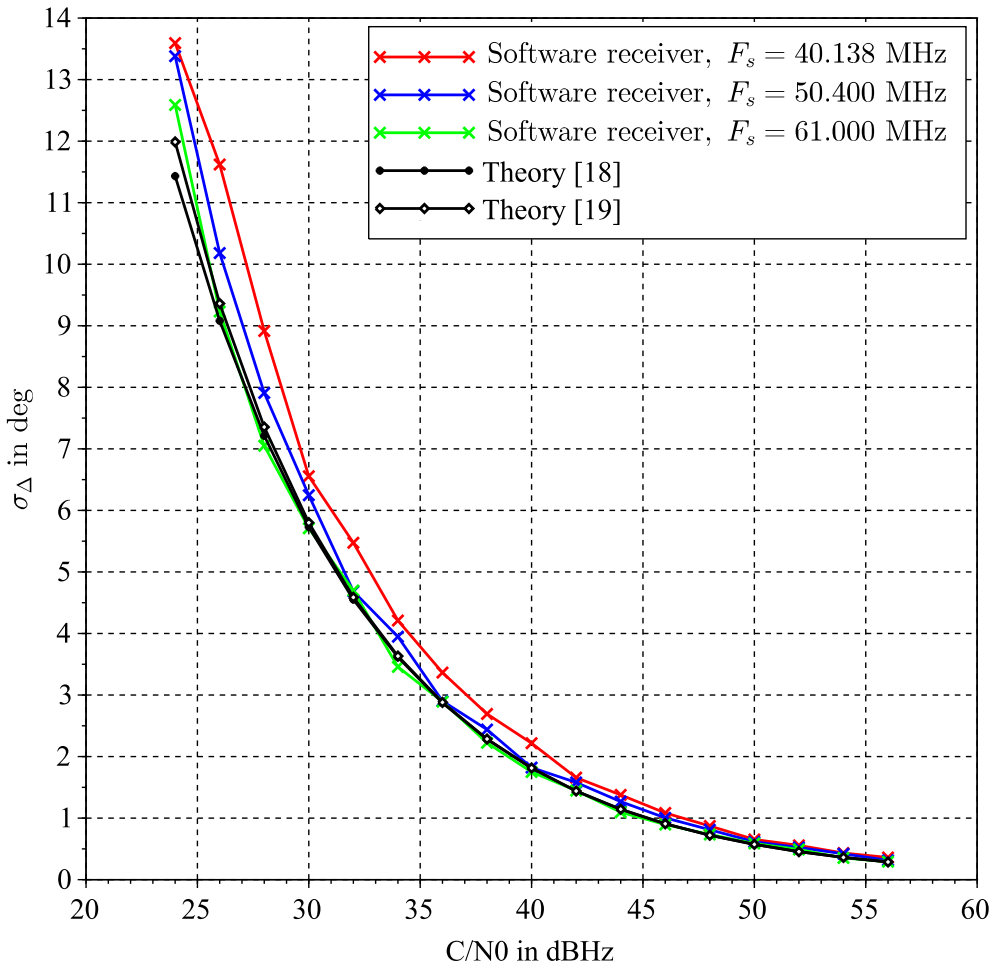

Figure 5.9: Phase measurement error standard deviation, without sampling jitter, vs *C/N0*.

5.2.5 Phase Measurement Error Statistical Characterization

5.2.5.1 Phase Measurement Error Standard Deviation

In section 5.1.2.2, it was established that the phase noise responsible for the sampling clock jitter is a random process which is not stationary. More exactly, it is characterized by a variance which increases linearly as a function of time, see equation (5.13). Hence variance is not a good statistic to define this phase noise or the corresponding sampling clock jitter. In the same way this classical variance (or the standard deviation) is not adapted to describe the phase measurement error at the output of the PLL induced by the sampling clock jitter. Indeed the phase measurement error should be characterized in the same manner as its origin, the phase noise of the clock, by its dynamic.

5.2.5.2 Phase Measurement Error Jitter

A first way to define the variation of the phase measurement error, due to the sampling clock jitter, is through its variance between two successive correlator outputs

$$\sigma_j^2 = E\left[\left(\Delta\phi[n+1] - \Delta\phi[n]\right)^2\right] \text{ in } (\text{rad})^2 \tag{5.20}$$

This is an extension of the TIE (Time Interval Error), a common metrology measurement [20]. Indeed it is the TIE applied to the phase measurement error instead of the signal transition when dealing with a clock or an oscillator. The objective is to measure the effect of a perturbation, the sampling clock jitter, defined by i.i.d. increments of variance c by unit of time. Hence, this variance σ_j^2 is well adapted as it describes the variance of $\Delta\phi$ over a period of time equal to T_p, the fundamental period of the tracking process.

The expected value in equation (5.20) is estimated in our software by the generalization of equation (5.17)

$$\hat{E}\left[\ \cdot\ \right] = \frac{1}{N}\sum_{\forall i}(\ \cdot\ ) \tag{5.21}$$

Instead of the variance described in equation (5.20), its square root will be shown, normalized in degree. This is a kind of phase measurement error standard deviation, in time. Or in other words, a jitter.

To test the signal generator – software receiver pair with respect to this statistic, a dry-run was done without jitter as in section 5.2.4. The phase measurement error jitter between two successive correlator outputs was measured in the *C/N0* range $[24, 56]$ dBHz. The results are plotted

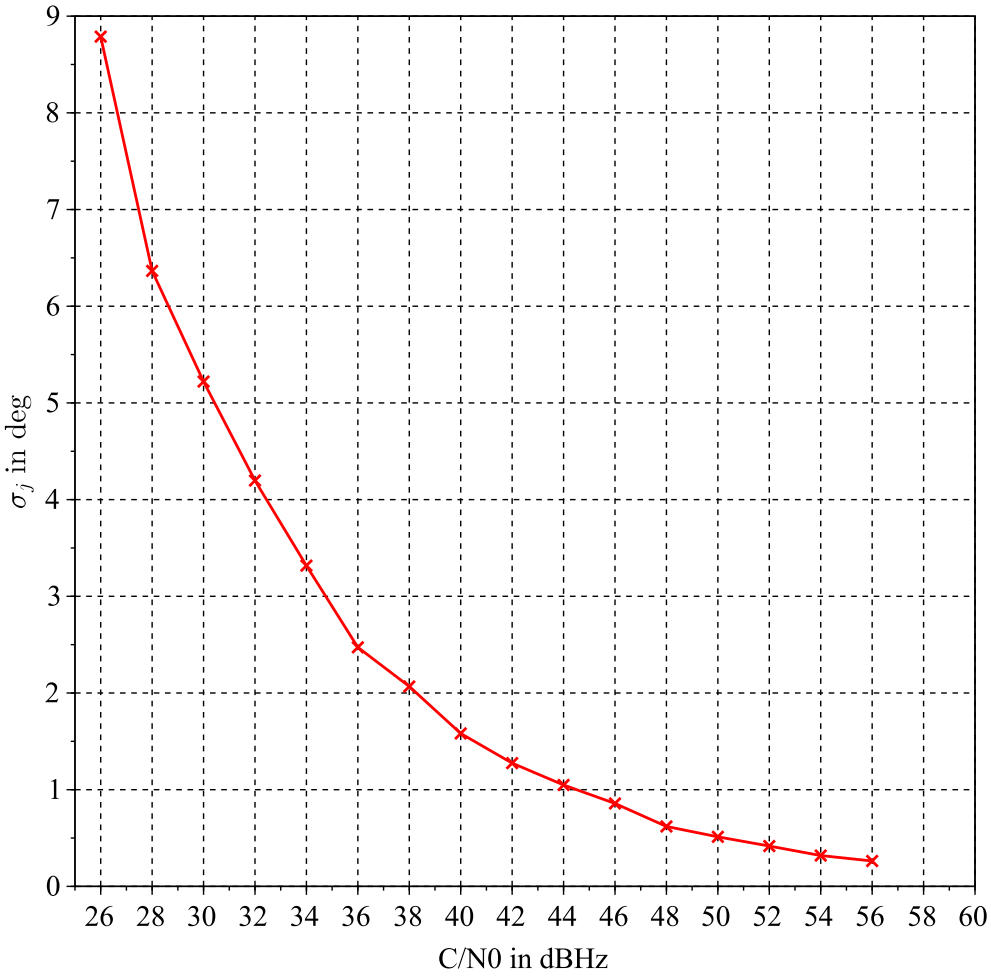

Figure 5.10: Phase measurement error jitter between two successive correlator outputs, without sampling jitter, vs *C/N0*.

in figure 5.10. It can be noticed that the curve for σ_j in figure 5.10 is slightly below the curve for σ_Δ (for $F_s = 40.138\,\text{MS/s}$) in figure 5.9. This means that the samples $\Delta\phi[n]$ and $\Delta\phi[n+1]$ are highly correlated, due to the action of the PLL which is equivalent to a narrow lowpass filter. In any event, as the curve visibly tends toward phase measurement error jitter of 0 for high values of *C/N0*, it is satisfactory as most of our measurements to come will be done here (i.e., with no additive noise, that is $C/N0 = 100\,\text{dBHz}$).

5.2.5.3 Phase Measurement Error Drift

A second interesting statistic for the phase measurement error is its Allan variance. It is well-fitted to define the RMS (Root Mean Square)

drift of this error. This Allan variation is defined, in $(\text{rad/s})^2$, for a GNSS PLL by [19]

$$\sigma_a^2 = \frac{1}{2T_p^2} E\left[\left((\Delta\phi[n+1] - \Delta\phi[n]) - (\Delta\phi[n] - \Delta\phi[n-1])\right)^2\right] \quad (5.22)$$

$$\sigma_a^2 = \frac{1}{2T_p^2} E\left[\left(\Delta\phi[n+1] - 2\Delta\phi[n] + \Delta\phi[n-1]\right)^2\right] \quad (5.23)$$

It is recalled that T_p is the coherent integration time of the receiver, that is the period between two correlator outputs, and as a consequence the operating period of the PLL also. In the remainder of this chapter, the Allan deviation σ_a will preferably be used, normalized by π, which unit is then Hz. A point to be noted, the Allan deviation is homogeneous to the (RMS) first derivative of the phase measurement error jitter developed in section 5.2.5.2.

To test again the signal generator – software receiver pair, with respect to the Allan deviation, a dry-run was done without jitter. The Allan deviation of the phase measurement error at the output of the PLL was measured in the *C/N0* range $[24, 56]$ dBHz. The results are plotted in figure 5.11. The relatively small obtained values should be due to the action of the PLL which shifts over time the NCO (Numerically Controlled Oscillator) phase to match the received signal phase. This phase shift over time is equivalent to a frequency modification, which is measured by the Allan standard deviation. In any event, as the curve visibly tends toward Allan deviation of 0 for high values of *C/N0*, it is satisfactory as most of our measurements to come will be done here (i.e., with no additive noise, that is *C/N0* $= 100$ dBHz).

5.2.6 Phase Measurement Error vs F_s

In the remainder of this chapter, constant $c \in [10^{-23}, 10^{-19}]$ s and the *C/N0* ratio is set to 100 dBHz (except where noted), which is equivalent to a situation free of thermal noise. The value of constant c was limited to 10^{-19} s because beyond this value the PLL regularly looses lock and the calculated statistics are not reliable. This is normally not an issue as even oscillators not controlled in temperature are characterized by a constant c equal or lower than this value, as already written in section 5.1.2.

Figure 5.12 and figure 5.13 present the results for two sampling frequencies. The lowest sampling frequency, 40.138 MS/s, is the minimum sampling frequency which allows the direct sampling of the E1 band in the Separate Sampling architecture, as established in section 3.3 of chapter 3. Figures 5.12 and 5.13 show clearly that the choice of the sampling frequency does not modify the sampling clock jitter effect on the phase

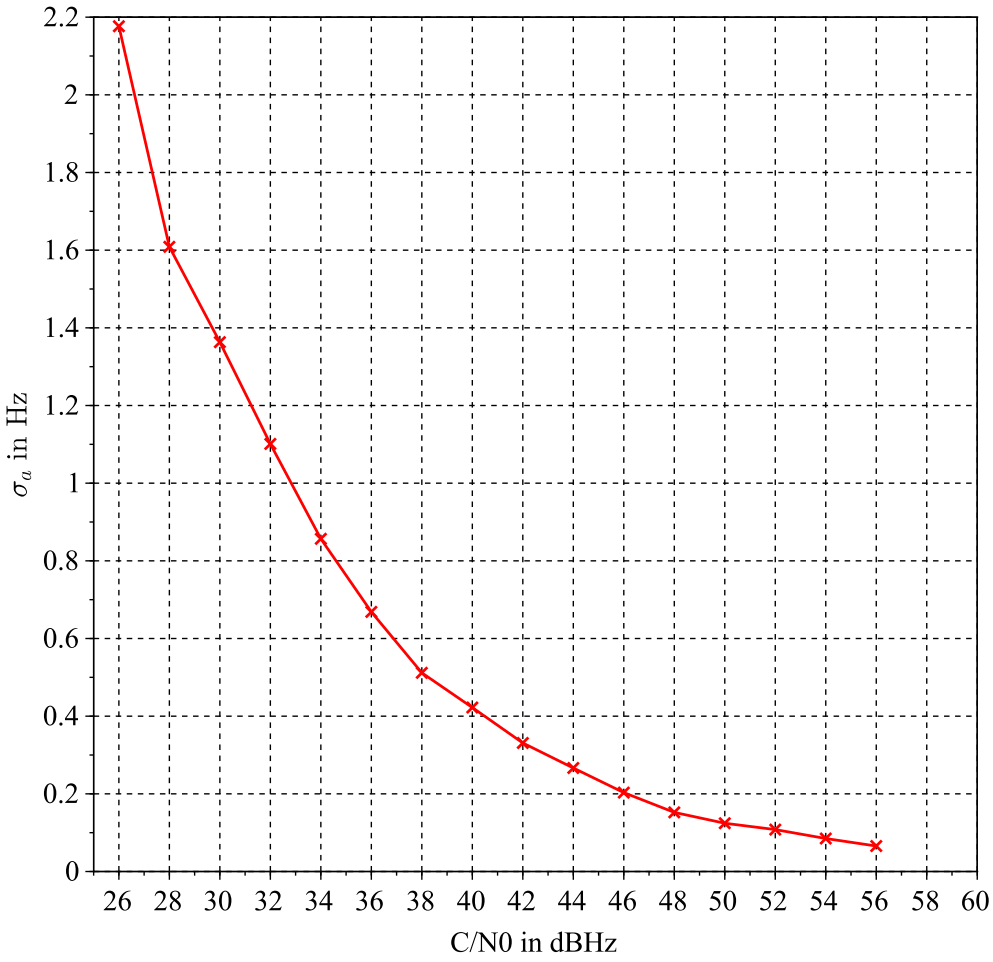

Figure 5.11: Allan deviation of the phase measurement error at the output of the PLL, without sampling jitter, vs *C/N0*.

measurement error. This is due to the fact that during a set coherent integration time T_p, the jitter has the same time to accumulate, whatever the sampling frequency, and then has the same statistics and so produces the same effect. This also means that the results established here for the Separate Sampling architecture also stand for the Coherent Sampling one.

The phase measurement error jitter, visible in figure 5.12, is below 9 ° for values of constant $c \leq 10^{-20}$ s. This value of 9 ° corresponds to the value obtained without sampling clock jitter, with thermal noise only, for $C/N0 \leq 26$ dB, as it can be seen in figure 5.10. Regarding specifically the phase measurement error drift, plotted in figure 5.13, its values are negligible as they do not reach 2 Hz, which is less than the maximum value obtained without jitter, with thermal noise only, for $C/N0 = 26$ dB, as it can be seen in figure 5.11. Hence, at this point, the value of $c = 10^{-20}$ s appears to be an upper limit not to be exceeded when choosing a sampling clock.

5.2.7 Phase Measurement Error vs T_p

The effect of the sampling clock jitter for two different coherent integration times is visible in figure 5.14 and figure 5.15. It appears quite clearly in figure 5.14 that when the coherent integration time is greater, the effect of the jitter is more important as this jitter has much time to accumulate as explained previously. Nevertheless, this effect seems not to be linear: a division by two of the coherent integration time does not imply a division by two of the phase measurement error jitter. Simulations with values of the PLL coherent integration time T_p greater than 20 ms were not considered. The reason is that this is a value which enabled to stand all performance tests in Civil Aviation, providing sufficient performance. According to [21], the possible benefits[3] in increasing T_p are not worth the risk. However, in other application fields where the use of the Galileo pilot signals are envisaged, with a long coherent integration time, this work should be done.

The phase measurement error jitter, visible in figure 5.14, is upper-bounded by the trace corresponding to $T_p = 20$ ms, which was already commented in section 5.2.6. The comment made at that time is then valid for all values of $T_p \leq 20$ ms. That is, for $c \leq 10^{-20}$ s, the effect of the jitter is less than in the situation with thermal noise only, so without sampling clock jitter, for $C/N0 \leq 26$ dB, as it can be seen in figure 5.10. Regarding figure 5.15, as a clear divergence between the two traces appears around $c = 5 \cdot 10^{-22}$ s, no interpretation seems possible.

3. Mainly a smaller phase standard deviation at the output of the PLL.

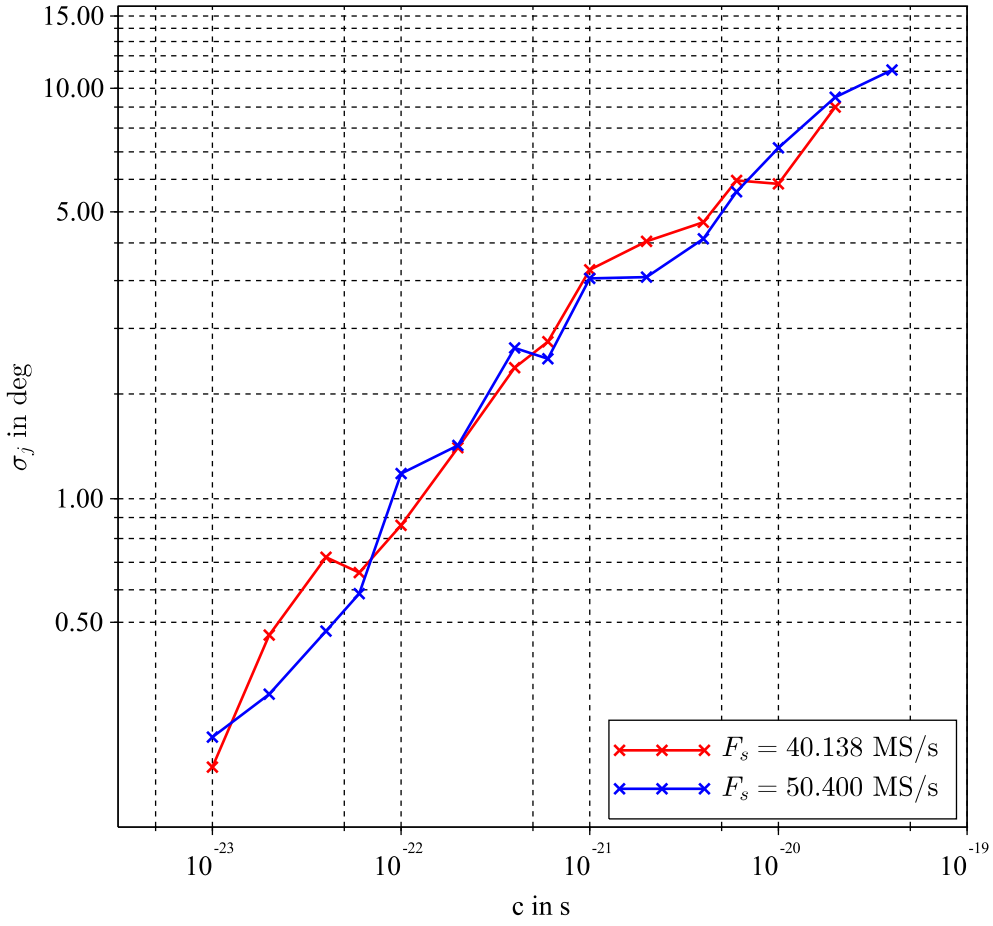

Figure 5.12: Phase measurement error jitter between two successive correlator outputs vs sampling frequency F_s.

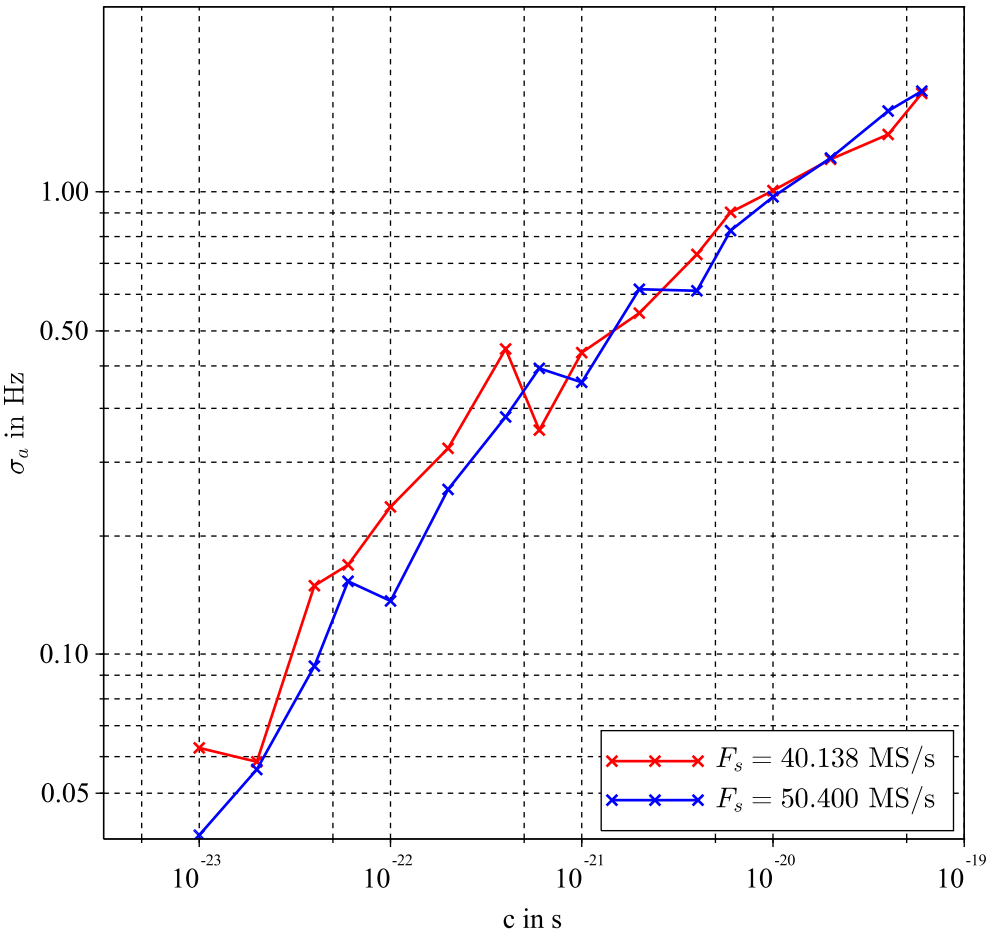

Figure 5.13: Allan deviation of the phase measurement error at the output of the PLL vs Sampling Frequency F_s.

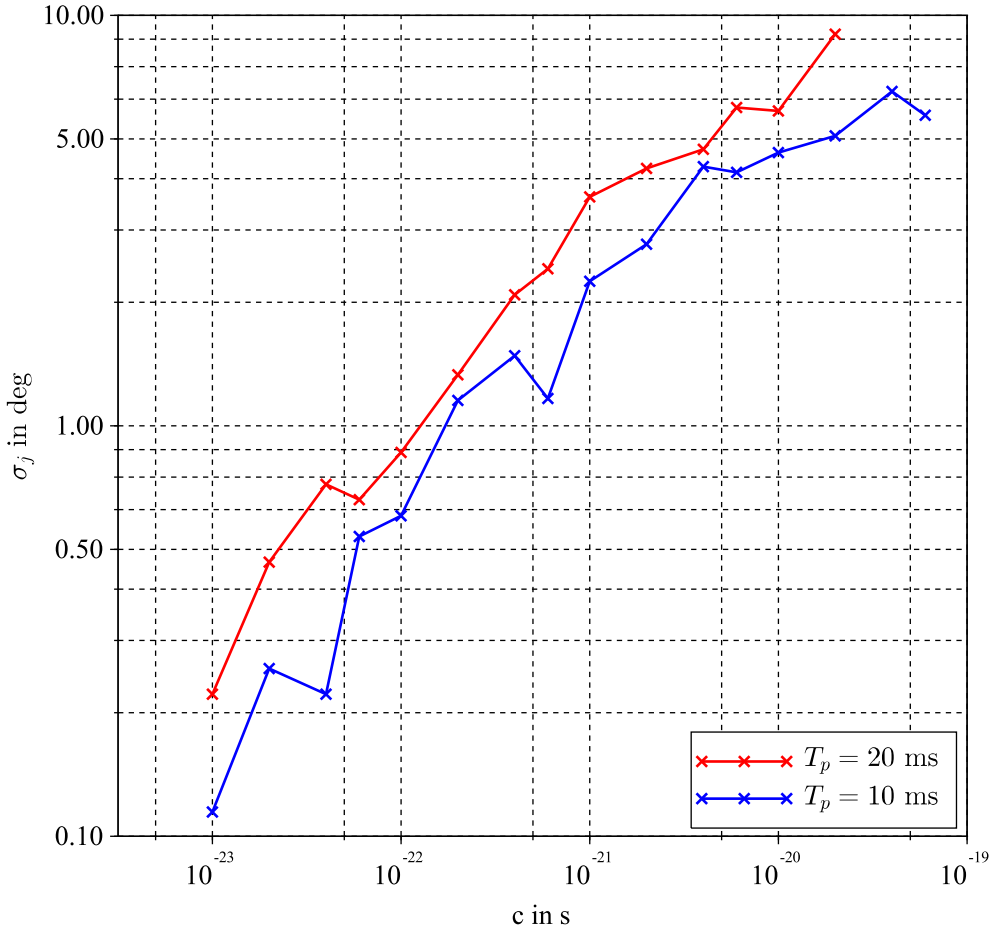

Figure 5.14: Phase measurement error jitter between two successive correlator outputs vs coherent integration time T_p.

In any case, as in section 5.2.6, the values of the phase measurement error drift are negligible here also. Consequently, as in section 5.2.6, the value of $c = 10^{-20}$ s appears to be an upper limit not to be exceeded when choosing a sampling clock.

5.2.8 Phase Measurement Error vs B_l

The effect of the sampling clock jitter was also measured against the noise equivalent bandwidth of the PLL parameter B_l. The results are plotted in figure 5.16 and figure 5.17. Regarding the phase measurement error jitter, represented in figure 5.16, as the two traces cross between $c = 6 \cdot 10^{-22}$ s and $c = 10^{-21}$ s, no simple interpretation seems possible as in section 5.2.7. The situation is worse for the Allan deviation plotted in figure 5.17 as there are several crossings. Some more simulations might

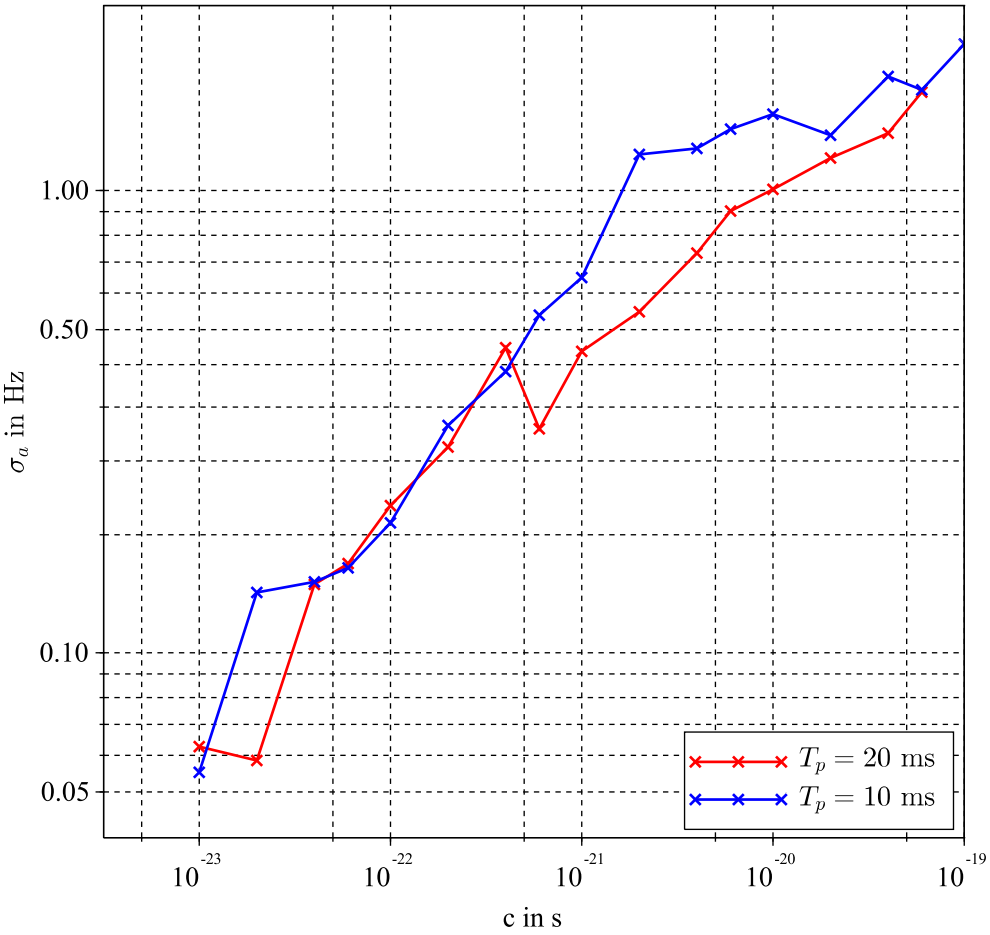

Figure 5.15: Allan deviation of the phase measurement error at the output of the PLL vs coherent integration time T_p.

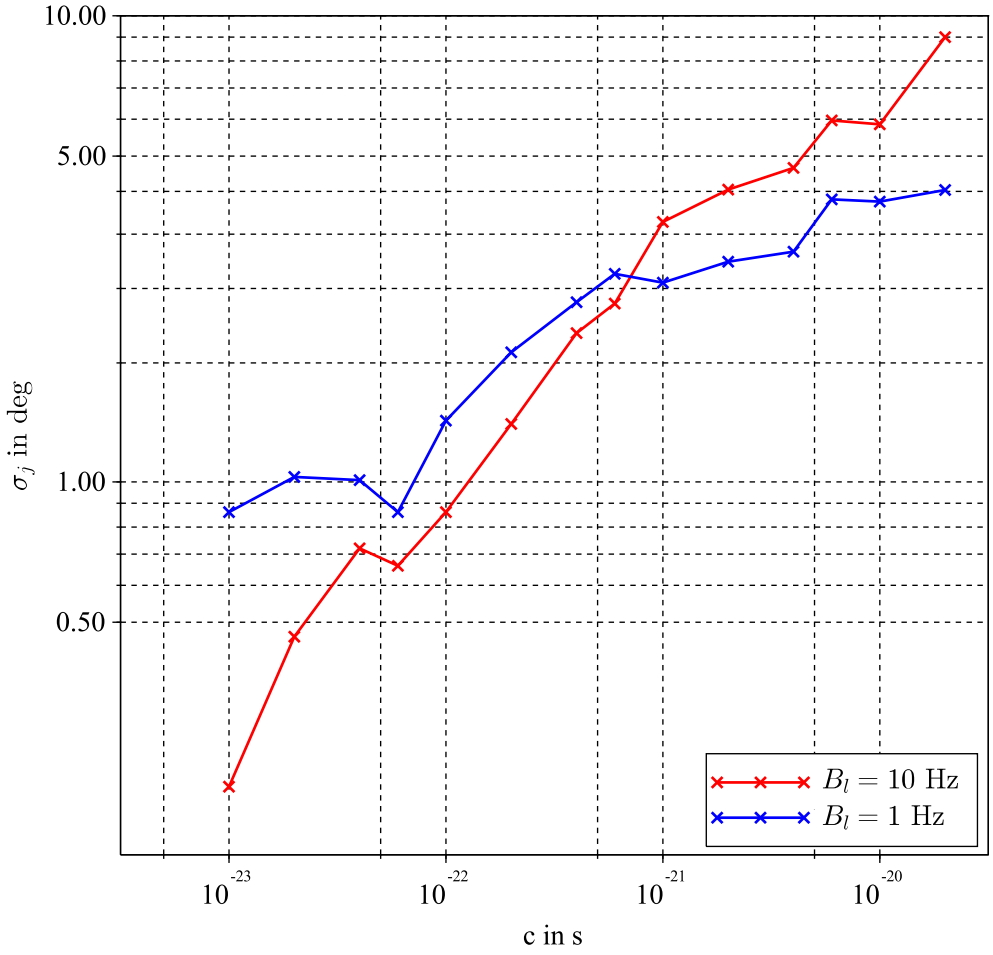

Figure 5.16: Phase measurement error jitter between two successive correlator outputs vs noise equivalent bandwidth of the PLL B_l.

decrease the variance of each plot and help to clarify the situation. In any case, as in sections 5.2.6 and 5.2.7, the values of the phase measurement error drift are negligible here for the integration times of 10 ms and 20 ms simulated. Then, the same recommendation as in sections 5.2.6 and 5.2.7 can be made here, the value of $c = 10^{-20}$ s appears to be an upper limit not to be exceeded when choosing a sampling clock.

5.2.9 *C/N0* Ratio Degradation vs Constant c

From the simulations, the *C/N0* ratio at the correlator output, a classical measure of the quality of the signal, was also estimated. It is plotted in figure 5.18, for the sampling frequencies $F_s = 40.138$ MS/s and $F_s = 50.400$ MS/s, as a function of constant c. It is recalled that the *C/N0* ratio, which takes into account the thermal noise only, indepen-

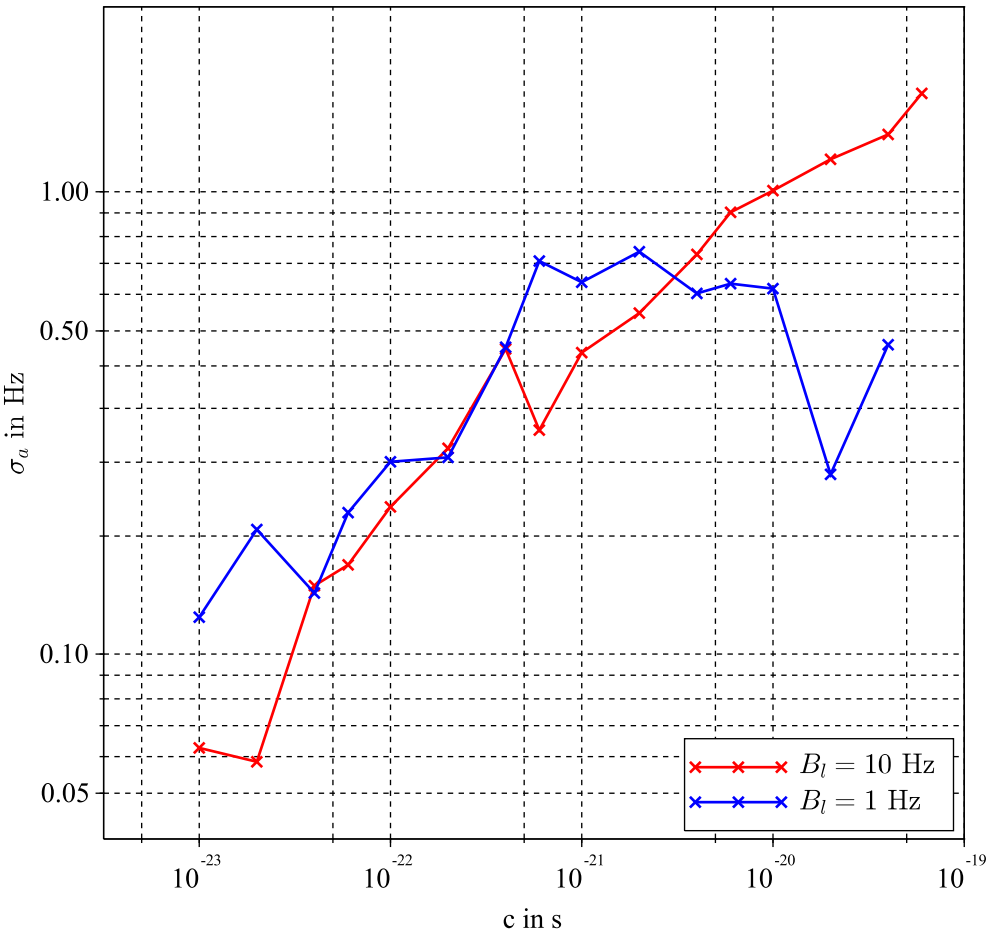

Figure 5.17: Allan deviation of the phase measurement error at the output of the PLL vs noise equivalent bandwidth of the PLL B_l.

dently of the sampling clock jitter, is set at the generator to 100 dBHz by default. It is noted the *initial C/N0*. The difference between this *initial* value of 100 dBHz and the *C/N0* ratio observed at the correlator output shows then the degradation brought by the sampling clock jitter, in terms of an equivalent additive white noise.

Figure 5.18 illustrates that, as already seen in section 5.2.6, the effect of the sampling clock jitter is not a function of the sampling frequency. What is more, the addition of noise (in dB) by the sampling clock jitter seems to be completely linear with c. A model of the *C/N0* ratio degradation over the range $c \in [10^{-23}, 10^{-20}]$ s can be written as:

$$\Delta\left(C/N0\right)_{\mathrm{dB}} \simeq 17 + 2.9 \times 10^{21} c \tag{5.24}$$

However, this relation should be validated by much more simulations at different sampling frequencies, with different coherent integration times T_p and different B_l, the noise equivalent bandwidth of the PLL.

Other simulations were conducted for various *initial C/N0* ratios as presented in figure 5.19. For *initial C/N0* ratios below ~ 44 dBHz, the degradation due to the sampling clock jitter is overcome by the thermal noise effect, for any value of $c < 10^{-19}$ s. It is also interesting to remark that, for all values of $c < 10^{-21}$ s (TCXO and OCXO) and for *initial C/N0* < 56 dBHz (an upper bound for the practical receiving conditions), the effect of the sampling clock jitter is nearly (-1 dB) no more detectable.

5.2.10 Acceptable Sampling Clock Jitter

To set an acceptable limit to the sampling clock jitter effect, it is proposed to use a criteria consistent with the one described in [5]: the sampling clock *jitter noise power is restricted to be* 10 dB *down from the thermal noise power*. This supposes to set a reference *C/N0*. It could logically be set taking into account, for the L1 C/A signal,

- *the minimum received power on Earth is* $C = -158.5$ dBW *measured at the output of a* 3 dB*i linearly polarized antenna (for a minimum satellite elevation angle of* 5 °*)* as cited in [22],
- *the equivalent system input thermal noise power density, N0, (...)* $N0 = -201.5$ dBW/Hz as assessed in [23].

The result is $C/N0_{ref} = 43$ dBHz. So, the *C/N0* ratio due to the sampling clock jitter should not be lower than 53 dBHz. It can be read in figure 5.18 that it corresponds to a value of c slightly greater than 10^{-20} s. This confirms the results found in sections 5.2.6, 5.2.7 and 5.2.8. Clocks with lower values than 10^{-20} s are easily available as explained in section 5.1.2: TCXO and OCXO.

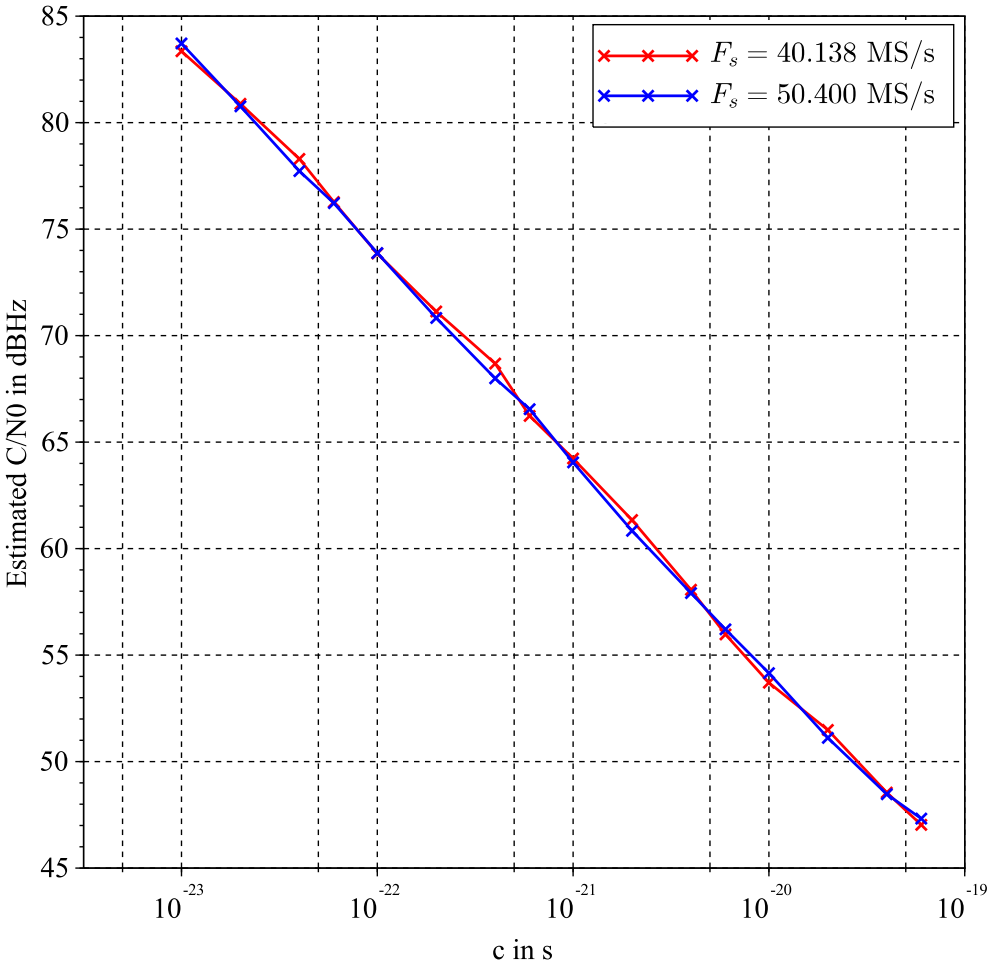

Figure 5.18: *C/N0* degradation vs constant c and sampling frequency F_s.

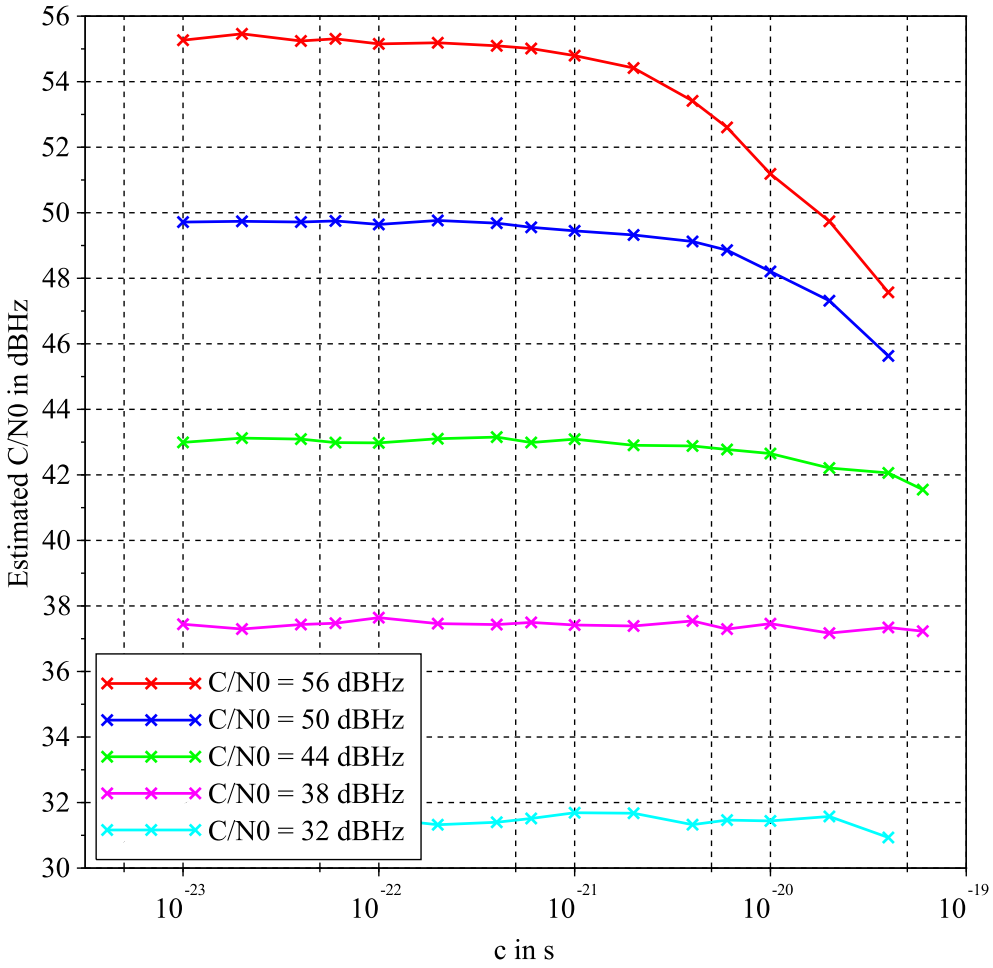

Figure 5.19: *C/N0* degradation vs constant c and initial *C/N0*.

5.3 Conclusion

The effect of the sampling clock jitter on signal tracking has been studied in this chapter. In a first step, a model of the sampling clock jitter was built, showing that it is not a stationary process. It was not possible then to establish a model of the induced phase measurement error. Therefore, it was also not possible to clarify the quantitative contribution of the sampling clock jitter in general. However, simulations were conducted as a function of the constant c, the parameter which characterizes the quality of the sampling clock. It has been shown that the sampling frequency has no influence on the jitter effect, contrary to the coherent integration time which increases the jitter effect as it is increased itself. Regarding the noise equivalent bandwidth of the PLL, it was not possible to clearly explain its impact. The *C/N0* ratio degradation at the output of the correlator was also measured, showing that for $c < 10^{-21}$ s and $C/N0 < 56$ dBHz, the effect of the sampling clock jitter is less than -1 dB. In light of these simulation results, a limit was set to the value of c to maintain the effect of the sampling clock jitter to an acceptable level. This acceptable level was defined to be 10 dB down from the thermal noise power, for $C/N0_{ref} = 43$ dBHz. The limit value of c was found equal to 10^{-20} s. It was finally noted that there is no difficulty to find a clock verifying this limit value of c.

5.4 References

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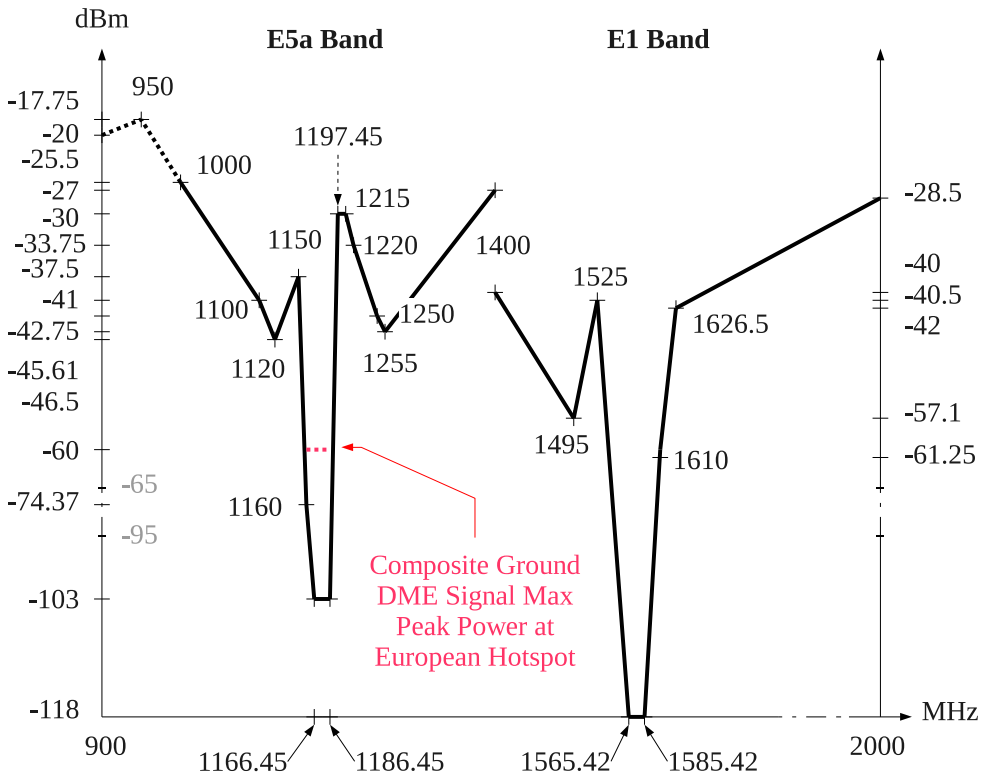
6 Quantization

After sampling, quantization is the second operation to address in order to completely characterize the digitization process which is carried out in a DS-DF-SDR Galileo receiver. As quantization is dimensioned after the amplitude of the signal present at the input of the ADC, and scaled as a function of the maximum amplitude levels, it seems necessary to recall the situation at the receiver input from this point of view. In this purpose, and for easier future referencing, figure 2.7 is cloned here in figure 6.1. The interference mask drawn in figure 6.1 is the maximum spectral content to be considered at the input of the receiver, before any of the extra RF filters specified in chapter 2. These filters are intended to decrease as much as possible the out-of-band levels of the mask before sampling. The level of the signal at the output of the filters, that is at the input of the ADC(s), will of course depend of the real performance of this extra RF filters, and more exactly of their effective bandwidth. This chapter investigates the dimensioning of the quantizer as a function of the real performance of the extra RF filters.

6.1 Quantization Dimensioning

As most ADC chipsets available on the market at the time of writing of this document provide a number of output bits which is an integer, the assumption is made that the number of quantization levels is a power of 2. That is to say that our design will use a mid-rise quantizer of the kind represented in figure 6.2. Should an other type of uniform quantizer be used, the formulas developed in this chapter must be revised and the numerical calculations updated but the results should be very similar to the ones presented hereafter, all the more so when the number of



dBm do not include the preamplifier gain [26.5, 32.5] dB nor cable losses [3,12] dB

Figure 6.1: Interference mask at receiver input.

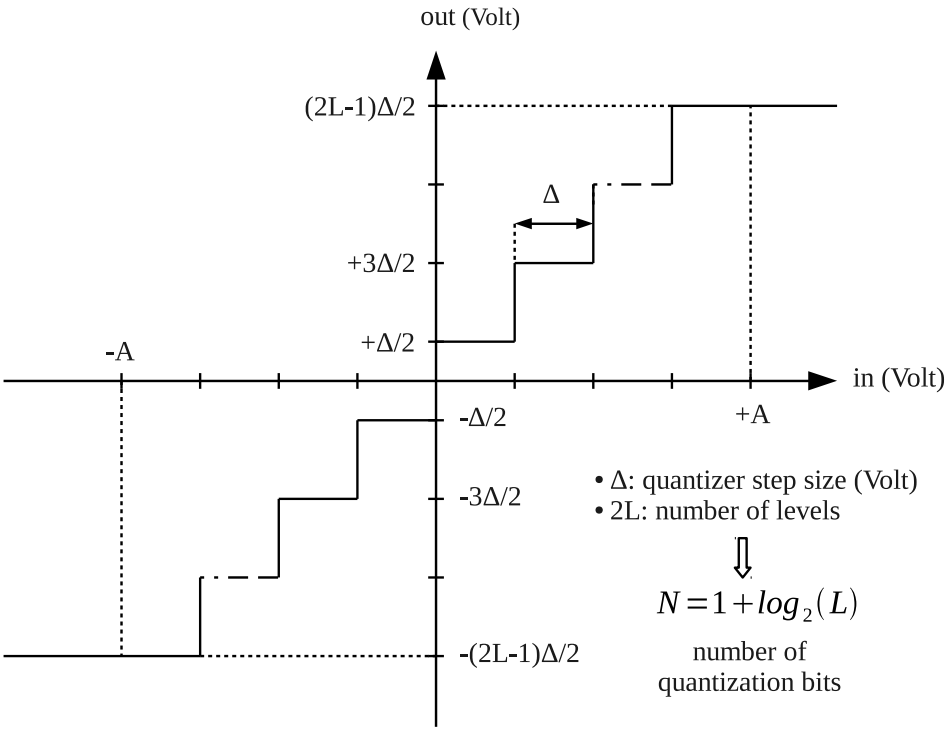


Figure 6.2: Mid-rise uniform quantizer.

levels increases. N denotes the total output bits of the quantizer, that is $2L = 2^N$ is the number of levels. To scale the quantization stage of the ADC(s), two reference amplitude levels must be considered.

6.1.1 Low Reference Amplitude Level

This level sets the minimum number of bits k required to correctly digitize the different Galileo navigation signals in the nominal situation, that is in an interference-free environment. However, interference-free does not mean noise-free. The system noise must be considered at the input of the ADC(s) as well as the useful signals.

6.1.1.1 System Noise Temperature at the Input of the ADC(s)

The calculation of the level of the noise at the input of the ADC(s) requires the noise characteristics of the various elements which take place between the antenna port and the input of the ADC(s). Concerning the active part of the GNSS antenna, [1] specifies

- its noise figure $NF = 4\,\mathrm{dB}$ [1],

1. Its linear value is the noise factor F defined by $NF = 10\log_{10}(F)$.

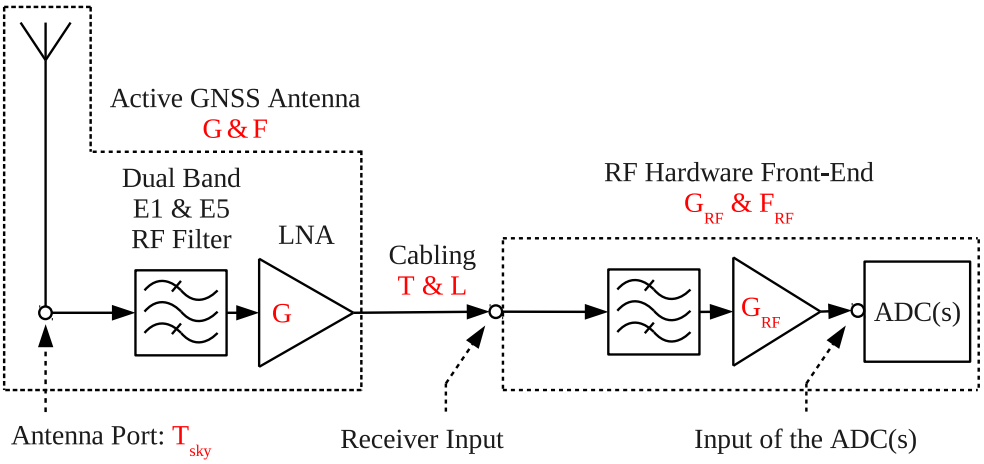


Figure 6.3: Noise model between the antenna port and the input of the ADC(s).

- its LNA (Low-Noise Amplifier) gain $G \in [G_{min}, G_{max}] = [26.5, 32.5]\,\text{dB}$.

Regarding the cabling, [1] assesses

- the actual cable temperature to $T = T0 = 290\,\text{K}$,
- the cable loss $L \in [L_{min}, L_{max}] = [3, 12]\,\text{dB}$.

The noise performance of the elements forming the RF hardware front-end (filters, amplifiers, diplexers and also the ADC(s)) can be globally characterized by a noise factor F_{RF} and a gain G_{RF} without loss of generality. These different parameters are represented in figure 6.3.

The effective noise temperature of each part, as depicted in figure 6.4, can then be defined according to [2]

- T_{act} is the effective noise temperature of the active part (dual-band E1 and E5 RF filter and LNA) of the GNSS antenna

$$T_{act} = (F - 1)\,T0 \tag{6.1}$$

- T_{cab} is the effective noise temperature of the cable

$$T_{cab} = (L - 1)T = (L - 1)\,T0 \tag{6.2}$$

- T_{RF} is the effective noise temperature of the RF hardware front-end

$$T_{RF} = (F_{RF} - 1)\,T0 \tag{6.3}$$

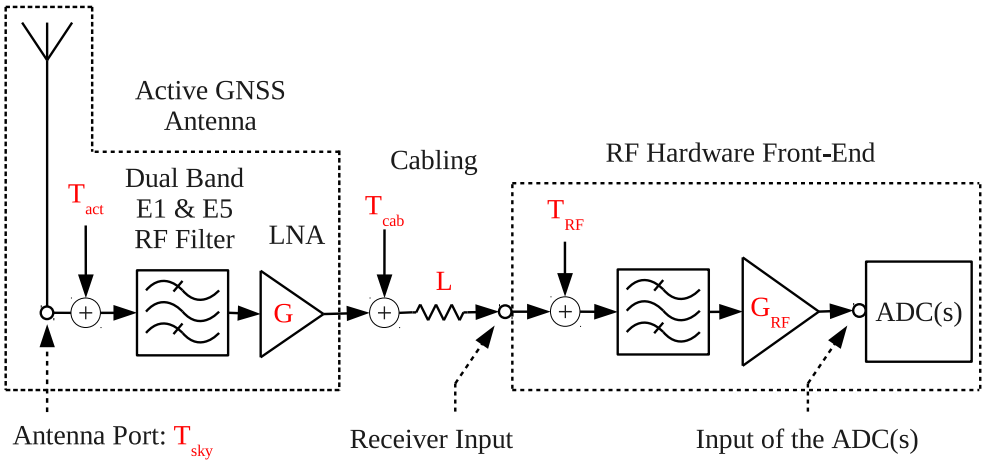


Figure 6.4: Effective noise temperatures between the antenna port and the input of the ADC(s).

These temperatures combine into a system noise temperature at the input of the ADC(s) according to [2] again, as represented in figure 6.5

$$T_{sys} = (((T_{sky} + T_{act})\,G + T_{cab})\,/L + T_{RF}) \times G_{RF} \tag{6.4}$$

6.1.1.2 Comparison Between the Different Noise Contributions

The noise contribution of the sky and of the active GNSS antenna can be compared to the contribution of the cabling through the ratio

$$\frac{(T_{sky} + T_{act})\,G}{T_{cab}} \tag{6.5}$$

That is

$$\frac{(T_{sky} + (F-1)\,T0)\,G}{(L-1)\,T0} \tag{6.6}$$

This ratio is minimum for the pair of values (G_{min}, L_{max}) and reaches $\simeq 16.4\,\text{dB}$. It means that the noise contribution of the cable is always negligible in comparison to the noise introduced upstream, whatever the values of G and L in their respective range. The assumption holds then that the extreme values of the noise at the output of the cable are given simply by the extreme pair of values (G_{min}, L_{max}) and (G_{max}, L_{min}) [2].

2. Normally the noise contribution of the active GNSS antenna is maximum at the output of the cable for (G_{max}, L_{min}) while the noise contribution of the cable is maximum for L_{max}

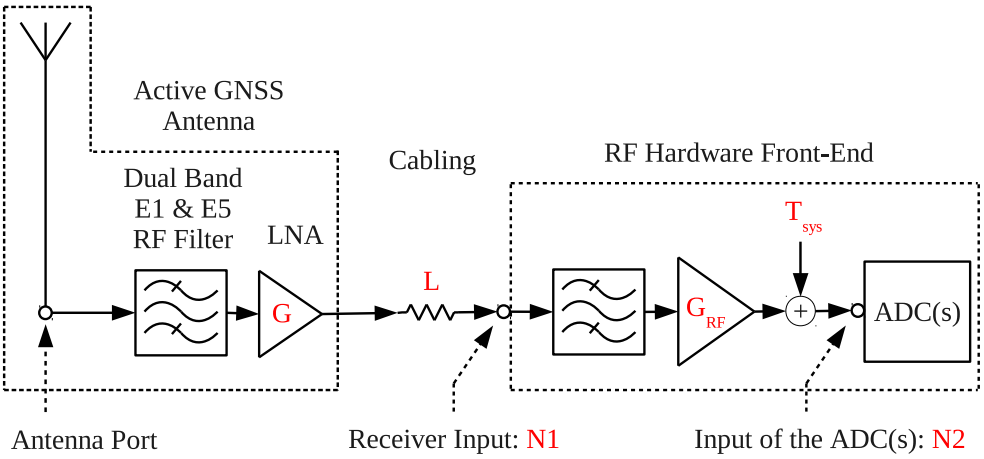


Figure 6.5: System noise temperature at the input of the ADC(s).

An other comparison can be made, between the noise contribution of the RF hardware front-end and the contribution of the active GNSS antenna and of the cabling, through the ratio

$$\frac{\left(\left(T_{sky}+T_{act}\right)G+T_{cab}\right)/L}{T_{RF}} \tag{6.7}$$

That is the ratio

$$\frac{\left(\left(T_{sky}+\left(F-1\right)T0\right)G+\left(L-1\right)T0\right)/L}{\left(F_{RF}-1\right)T0} \tag{6.8}$$

The noise contribution of the RF hardware front-end would reach one-tenth of the other noises for a noise figure $NF_{RF} \simeq 8.0\,\mathrm{dB}$ for the minimum value of the numerator in (6.8), obtained for the minimum value $G_{min}/L_{max} = 14.5\,\mathrm{dB}$. It is believed that this value of NF_{RF} could be difficult to achieve, considering for example the insertion loss of the cascaded filter designed in section 4.2.4 of chapter 4 which reaches 8.15 dB at room temperature (that is a noise figure around the same value). The noise contribution of the RF hardware front-end can not be neglected in comparison to the noise introduced by the upstream parts. However, as F_{RF} could not be assessed at the time of this writing, it was not possible to take it into account. The system noise temperature at the input of the ADC(s) considered from now on is then

$$T_{sys} = \left(\left(T_{sky}+\left(F-1\right)T0\right)G+\left(L-1\right)T0\right)/L \times G_{RF} \tag{6.9}$$

The subsequent results depending on T_{sys} should then be taken as bounds and updated as soon as more accurate data characterizing the noise performance of the RF hardware front-end are available.

6.1.1.3 Power of the Noise at the Input of the ADC(s)

Making the assumption that the different noises are white, the system noise PSD level at the input of the ADC(s) is equal to

$$N2 = k_B T_{sys}$$
$$N2 = k_B \left(\left(T_{sky} + (F-1)\, T0 \right) G + (L-1)\, T0 \right) / L \times G_{RF} \tag{6.10}$$

with $k_B = 1.3806488 \times 10^{-23}$ J/K the Boltzmann constant.

It is interesting to remark that the left term in the outer product in relation (6.10) corresponds to the PSD level of the noise at the receiver input

$$N2 = N1 \times G_{RF} \tag{6.11}$$
$$N1 = k_B \left(\left(T_{sky} + (F-1)\, T0 \right) G + (L-1)\, T0 \right) / L \tag{6.12}$$

As the two Direct Sampling architectures proposed in this thesis not only aim at being *aircraft installation independent* but also do not implement any kind of AGC, they must cope with the full range of preamplifier gain G and cable loss L. The corresponding range of $N1$ is then calculated from (6.12) by replacing G and L by the extreme values (G_{min}, L_{max}) on one hand and (G_{max}, L_{min}) on the other. The result is

$$N1 \in [N1_{min}, N1_{max}] = [-186.7, -171.8]\,\text{dBW/Hz} \tag{6.13}$$

The power of the noise at the input of the ADC(s) is

- For the Coherent Sampling architecture, at the input of the single ADC

$$P_2 = N2 \times (B_1 + B_{5a}) = N1 \times G_{RF} \times (B_1 + B_{5a}) \tag{6.14}$$

  with B_1 and B_{5a} the bandwidth of the useful E1 and E5a bands defined in section 2.3 of chapter 2.

- For the Separate Sampling architecture at the input of each ADC

$$P_2 = N2 \times B_1 = N2 \times B_{5a} \tag{6.15}$$

It is worth writing P_2 as a function of P_1 the power of the noise at the receiver input, because this quantity is independent of the unknown value G_{RF}

$$P_1 = N1 \times (B_1 + B_{5a}) \tag{6.16}$$

$$P_1 \in [P_{1,min}, P_{1,max}] = [-110.7, -95.8]\,\text{dBW} \tag{6.17}$$

It gives

- For the Coherent Sampling architecture

$$P_2 = P_1 \times G_{RF} \tag{6.18}$$

- For the Separate Sampling architecture

$$P_2 = P_1 \times G_{RF}/2 \tag{6.19}$$

At this point the classical assumption is made that the different noises studied herebefore can be modeled as zero-mean Gaussian random processes. This implies $P_1 = \sigma_1^2$ and $P_2 = \sigma_2^2$, σ denoting the standard deviation of the process. The quantizer being dimensioned after amplitude, σ will be used preferably to P in the rest of this chapter.

Aside the definition of P_1 and P_2, it is useful for later reference to define the equivalent power of the noise at the antenna port $P_0 = \sigma_0^2$

- For the Coherent Sampling architecture

$$P_0 = N0 \times (B_1 + B_{5a}) \tag{6.20}$$

- For the Separate Sampling architecture

$$P_0 = N0 \times B_1 = N0 \times B_{5a} \tag{6.21}$$

with $N0 \simeq k_B\,(T_{sky} + T_{act}) = -201.3\,\text{dBW/Hz}$, neglecting the noise of the cable and of the RF hardware front-end brought back to the antenna port. This is reasonable considering the high gain of the preamplifier, $G_{min} = 26.5\,\text{dB}$.

6.1.1.4 Galileo Navigation Signals

It is specified in [1] that the power to be considered at the antenna port for the different Galileo Open Service signals is

- $P_{E5a} = [-155.7, -148.7]\,\text{dBW}$ for the E5a signal,
- $P_{E1} = [-157, -150]\,\text{dBW}$ for the E1 signal.

For an average number of 8 visible satellites, also clarified in [1], this gives a maximum total power of

- $P_{E5a} = -139.7\,\text{dBW}$ for the E5a signals,
- $P_{E1} = -141\,\text{dBW}$ for the E1 signals.

The corresponding ranges at the input of the receiver are calculated by multiplying these values by the extreme ratios G_{min}/L_{max} on one hand and G_{max}/L_{min} on the other, as done for the noise in relation (6.13)

- $P_{E5a} \in [-125.2, -110.2]$ dBW for the E5a signals,
- $P_{E1} \in [-126.5, -111.5]$ dBW for the E1 signals.

Comparing these numbers to the power of the noise at the receiver input given in (6.17), it can be said that the useful navigation signals are completely buried in the noise. As it is not possible to separate each contribution at this point, from now on it must be considered that the signal to quantize is the sum of the useful navigation signals and the noise. Moreover, as the useful signal power is more than ten times weaker than the noise power it is decided to consider that only the noise is to be taken into account to dimension the quantizer.

6.1.1.5 k the Number of Bits in an Interference-Free Environment

The number of bits k required to correctly digitize the useful signal(s) must be calculated to account for the *lowest noise* amplitude at the input of the ADC(s). Writing Δ the quantizer step size and considering that the maximum *lowest noise* amplitude is $n_{2,min}$ in units of volts, then

$$2^k \times \Delta \geq 2n_{2,min} \tag{6.22}$$

It is more relevant to replace $n_{2,min}$ by its expression as a function of the standard deviation $\sigma_{2,min}$ through the *crest factor* c[3]

$$c = \frac{n_{2,min}}{\sigma_{2,min}} \tag{6.23}$$

It gives:

$$2^k \times \Delta \geq 2c \cdot \sigma_{2,min} \tag{6.24}$$

The calculation of the optimum c value, which produces the minimum degradation of the useful signal power at the output of the correlator, is proposed in [3], as a function of the number of quantization levels. Table 6.1 summarizes the values of interest in our case. [4] indicates for example that in aviation grade receivers $k \sim 2{-}4$ bits. For the sake of completeness and clarity, it is to note that in [3], $n_{2,min}$ is noted T, the maximum input threshold, and the results are presented as a function of the ratio of this maximum input threshold to the one-sigma noise level, that is the *crest factor* c.

3. This *crest factor* c is not to be confused with the constant c (introduced in section 5.1.2 of chapter 5) which characterizes the sampling clock jitter. The notation is kept unchanged in both cases because it is generally used in the publications on the related subjects.

k	Minimum Signal Loss (dB)	Optimum *crest factor*
1	1.961	N/A
2	0.549	0.996
3	0.166	1.758
4	0.050	2.345
5	0.015	2.820
6	0.005	3.224
7	0.001	3.591

Table 6.1: Optimum crest factor c vs k [3].

6.1.2 High Reference Amplitude Level

This level sets the full scale of the ADC(s). It corresponds to the total number of bits N of the ADC(s). This high level is obviously a function of the interference mask at the input of the ADC(s), but also of the noise maximum value as it is always present. Again, the proposed architectures aim at being *aircraft installation independent*. It means that this time the high reference level must be calculated with the maximum active antenna gain $G_{max} = 32.5\,\text{dB}$ and the minimum cable loss $L_{min} = 3\,\text{dB}$ to cover the maximum maximorum level of the signal at the input of the ADC(s).

6.1.2.1 Maximum Interference + Noise Level at the input of the ADC(s)

At this point the assumption is made that the CW aggression is limited to one interference at a time per band, as the tests imposed in [1] suggests. It means that, for Coherent Sampling the maximum interference level A_M to be considered is the sum of the maximum amplitudes found in the mask for E5a on the one hand and for E1 on the other. For Separate Sampling it is either the maximum amplitude A_{M5a} found in the mask for E5a for the corresponding ADC or the maximum amplitude A_{M1} found in the mask for E1 for the other ADC.

The high reference level is then the maximum sum of the maximum interference level A_M, A_{M5a} or A_{M1}, multiplied by G_{max}, divided by L_{min} and multiplied by G_{RF}, and of the *highest noise* level, corresponding to $N2_{max}$. Writing A_{max} the generic value for A_M, A_{M1} or A_{M5a} and noting the maximum *highest noise* amplitude $n_{2,max}$, this high reference level equals

$$\sqrt{G_{max}/L_{min}G_{RF}} \times A_{max} + n_{2,max} \text{ in units of volts}$$

This time again the use of the *crest factor* c is more relevant. It is written here equivalently to equation (6.23) by the ratio of the *highest noise* amplitude $n_{2,max}$ to the maximum noise standard deviation $\sigma_{2,max}$

$$c = \frac{n_{2,max}}{\sigma_{2,max}} \tag{6.25}$$

The final expression of the high reference level is then

$$\sqrt{G_{max}/L_{min}G_{RF}} \times A_{max} + c \cdot \sigma_{2,max}$$

6.1.2.2 N the Total Number of Bits of the Quantizer

A graphical representation of the dimensioning values k, the number of bits required to correctly digitize the useful signal(s) in an interference-free environment (i.e. minimum noise), and N, the total output bits of the quantizer considering the maximum signals expected (i.e. maximum noise plus interference), can be found in figure 6.6. The following relation can then be established

$$2^N \times \Delta \geq 2\sqrt{G_{max}/L_{min}} \times A_{max} + 2c \cdot \sigma_{2,max} \tag{6.26}$$

A simple algebraic division between equations (6.26) and (6.24) gives

$$N - k \geq \log_2 \left(\frac{\sqrt{G_{max}/L_{min}G_{RF}} \times A_{max} + c \cdot \sigma_{2,max}}{c \cdot \sigma_{2,min}} \right) \tag{6.27}$$

The replacement of σ_2 by its expression as a function of σ_1 given by equation (6.18) [4] or equation (6.19) produces a final result independent of G_{RF} and valid for the separate sampling architecture as well as for the coherent sampling architecture

$$N - k \geq \log_2 \left(\frac{\sqrt{G_{max}/L_{min}} \times A_{max} + c \cdot \sigma_{1,max}}{c \cdot \sigma_{1,min}} \right) \tag{6.28}$$

Thus, setting k and c, N can be calculated as a function of A_{max} only. As it is detailed hereafter, this level A_{max} is quite dependent of the real transfer functions of the extra filters required in both proposed architectures. In fact, it depends on the effective attenuation brought to the interference mask by the extra filters. However, before studying the influence of the real transfer functions of the extra filters on the

4. It is recalled that $\sigma_1^2 = P_1$ and $\sigma_2^2 = P_2$ as explained in section 6.1.1.3.

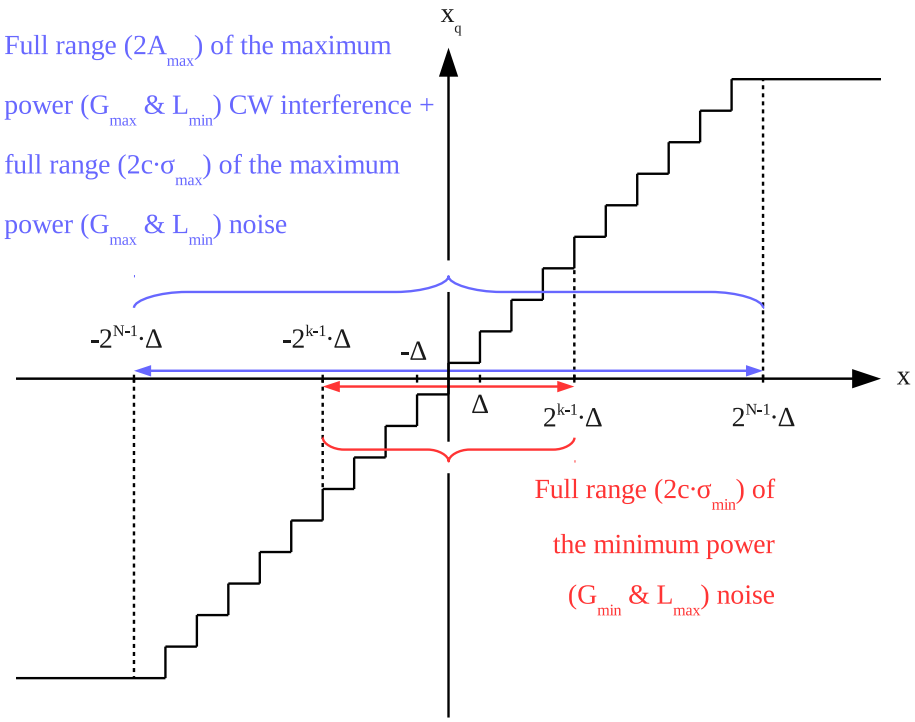


Figure 6.6: Dimensioning values of the quantizer.

value of N, it is interesting to apply equation (6.28) in the case with no interference ($A_{max} = 0$)

$$N - k \geq \log_2\left(\frac{\sigma_{1,max}}{\sigma_{1,min}}\right) = \log_2\left(\frac{N1_{max}}{N1_{min}}\right) \tag{6.29}$$

which gives, under the first assumption made in section 6.1.1.2 that "the extreme values of the noise at the output of the cable are given simply by the extreme pair of values (G_{min}, L_{max}) and (G_{max}, L_{min})"

$$N - k \geq \frac{1}{2}\log_2\left(\frac{G_{max}}{G_{min}} \cdot \frac{L_{max}}{L_{min}}\right) = 2.5 \tag{6.30}$$

Thus the cost of our *aircraft installation independent* receiver: it needs 3 more bits than strictly necessary to quantize the full range of the preamplifier gain and cable loss. Furthermore, it is also the cost of the removal of the AGC. This mechanism would have otherwise automatically taken into account the real values of G and L in a manner that is transparent to the quantizer.

k	Optimum *crest factor*	E5a: $N-k \geq$	E1: $N-k \geq$
1	N/A	N/A	N/A
2	0.996	8.9	2.7
3	1.758	8.1	2.6
4	2.345	7.6	2.6
5	2.820	7.4	2.6
6	3.224	7.2	2.5
7	3.591	7.1	2.5

Table 6.2: $N-k$ for Separate Sampling with ideal filters.

6.2 Quantization with ideal filters

6.2.1 Separate Sampling

If the extra filters used before digitization meet the minimum selectivity drawn in figure 3.11 then the interference mask to be considered at the input of the ADCs is the one represented in figure 3.12. In fact there is nearly no more interference threat, except in-band. It can be read in figure 3.12 that A_{M5a} corresponds to the composite ground DME signal maximum peak power at the European hotspot, -60 dBm and that A_{M1} is equal to the floor of the interference mask for the E1 band, -118 dBm.

A_{max} set in turn to the value of A_{M5a} and A_{M1} [5] in equation (6.28), along with the value of c given in table 6.1, it is possible to calculate $N-k$, for each value of k. Table 6.2 lists the results for k from 1 to 7, for each band. It is recalled that $N-k$ is the difference between the total output bits of the quantizer and the number of bits required to correctly digitize the useful signal(s) in the nominal situation. For the E5a band the DME threat rules the results, while for the E1 band it is only the classical noise indeed. Up to a total of $N=15$ bits can be required for the E5a band and up to 10 bits for the E1 band, for a crest factor of 3.591.

6.2.2 Coherent Sampling

If the extra filters used before digitization meet the minimum selectivity drawn in figure 3.3 then the interference mask to be considered at the input of the ADC is the one represented in figure 3.4. Here also, as the filters have perfectly met the targeted attenuation, there is nearly no more interference threat, except in-band. It can be read in figure 3.4

5. $A_{M5a}=10^{-60/20}$ as it is peak power while $A_{M1}=\sqrt{2}\cdot 10^{-118/20}$ because it is average power.

k	Optimum *crest factor*	$N - k \geq$
1	N/A	N/A
2	0.996	8.4
3	1.758	7.6
4	2.345	7.2
5	2.820	6.9
6	3.224	6.7
7	3.591	6.6

Table 6.3: $N - k$ for Coherent Sampling with ideal filters.

that for the E5a band the maximum threat is also the composite ground DME signal maximum peak power at the European hotspot, −60 dBm, and that it is the floor of its CW interference mask for the E1 band, −118 dBm this time again. At the input of the single ADC the maximum level to be considered is then the coherent sum of both threats, that is $\simeq -63$ dBm [6].

In the same way as for the Separate Sampling case, setting A_{max} to −63 dBm in equation (6.28), along with the value of c given in table 6.1, it is possible to calculate $N - k$, for each value of k. Table 6.3 lists the results for k from 1 to 7. As shown previously for the E5a band in Separate Sampling, the DME threat rules the results. A total of 14 bits may be needed if the useful signal should be quantized with $k = 7$ bits. This is nearly the same value as for the Separate Sampling of the E5a band as the E5a threat completely overcomes the one on the E1 band.

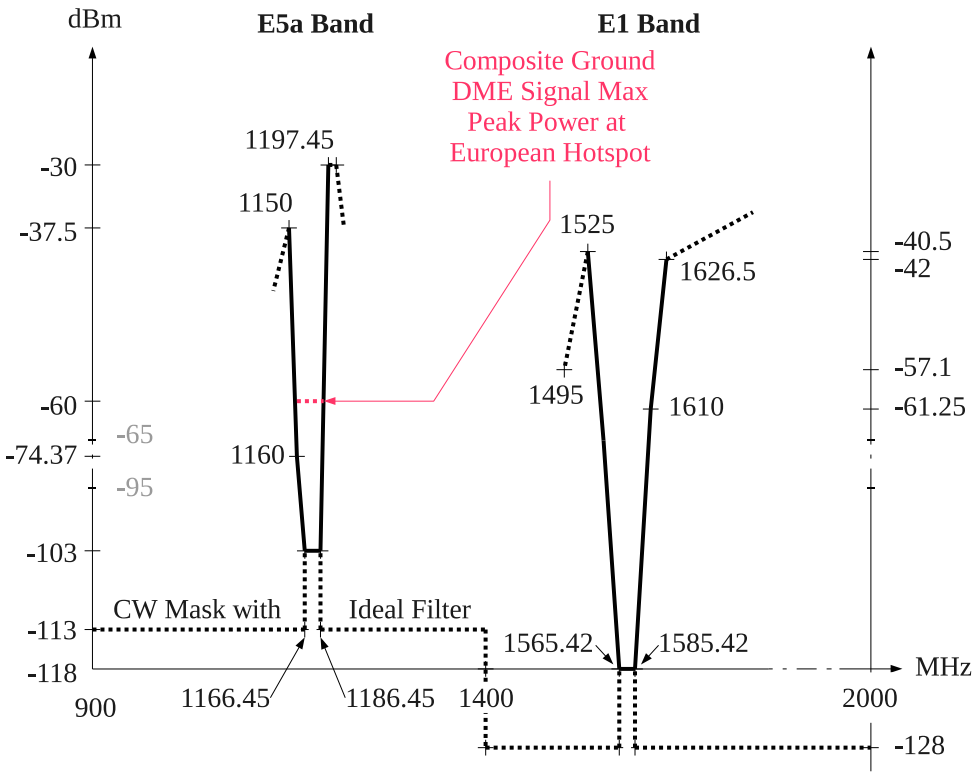
6.3 Quantization after Sub-optimal Filters

If the extra filters are not as selective as required, that is their effective bandwidth is larger than specified, the interference threat can pass through them up to a very high level, which is a function of this actual bandwidth.

6.3.1 Separate Sampling

This time the situation at the input of the ADCs can be as bad as the one presented in figure 6.7, where the whole interference mask has passed through the extra filters. It corresponds to the worst case of filters with an actual bandwidth larger than 47.45 MHz in the E5a band and

6. The DME peak power at the European hotspot has been converted into average power, by subtracting 3 dB, to be consistent with the E1 CW mask in dBm. The peak amplitude value corresponding to the coherent sum is then $A_{max} = \sqrt{2} \cdot 10^{-63/20}$.



dBm do not include the preamplifier gain [26.5, 32.5] dB nor cable losses [3,12] dB

Figure 6.7: CW interference mask at receiver input with sub-optimal filters, Separate Sampling.

101.5 MHz in the E1 band. Figure 6.7 is simply a copy of figure 6.1 which represents the interference situation at the input of the receiver without the extra filters. However, the assumption is made that the analog filters will be selective enough so that it can be considered that the maximum threat for the E1 band is a CW interference which can reach -40.5 dBm at 1626.5 MHz (it corresponds to a transition bandwidth[7] greater than $B_s = 40$ MHz). For the E5a band the maximum threat is a CW interference which can reach -30 dBm at 1197.45 MHz (a transition bandwidth greater than $B_s = 10$ MHz).

Figure 6.8 for the E5a band and figure 6.9 for the E1 band plot the values of $N - k$ against the interference mask. The curves were obtained

7. As defined in section 3.2.2 of chapter 3, the transition bandwidth B_s is the bandwidth of the filter which is in excess on each side of the minimum specified bandwidth. For example, a transition bandwidth of B_s MHz on E5a means that the passband of the filter is $[f_{5min} - B_s, f_{5max} + B_s]$ and its bandwidth equals $B_s + 20 + B_s = 20 + 2B_s$ MHz.

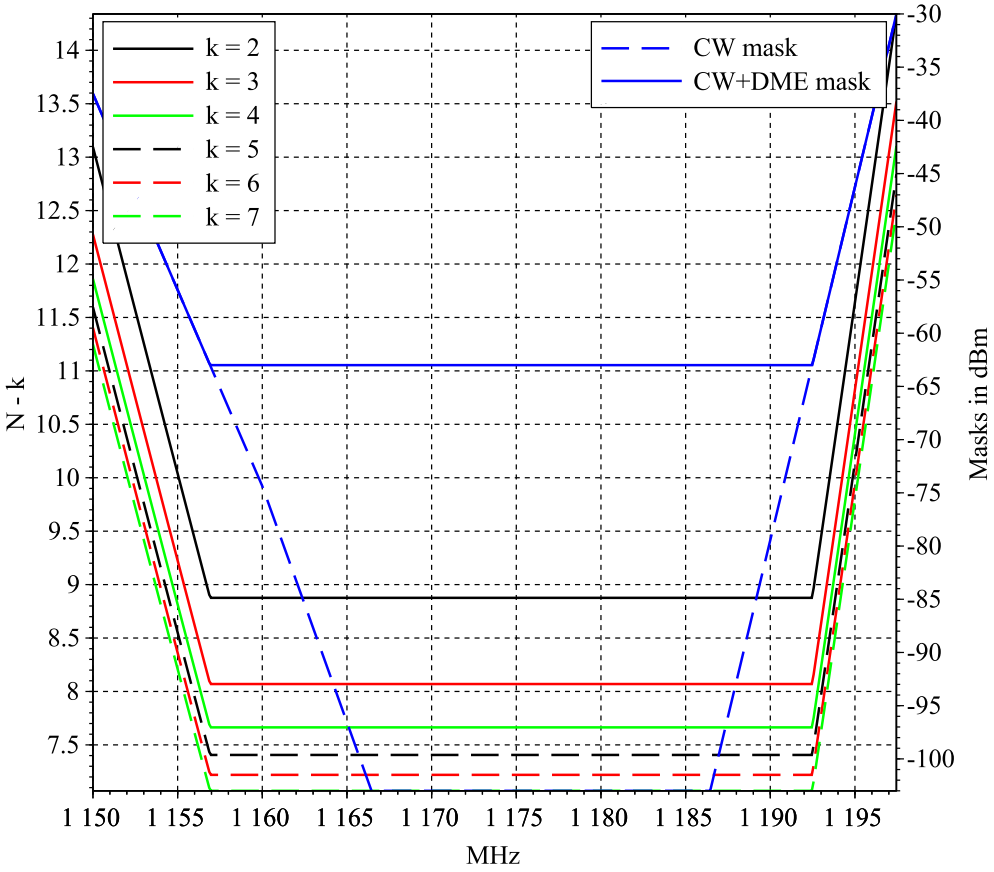


Figure 6.8: $N - k$ for Separate Sampling with sub-optimal filters, E5a band.

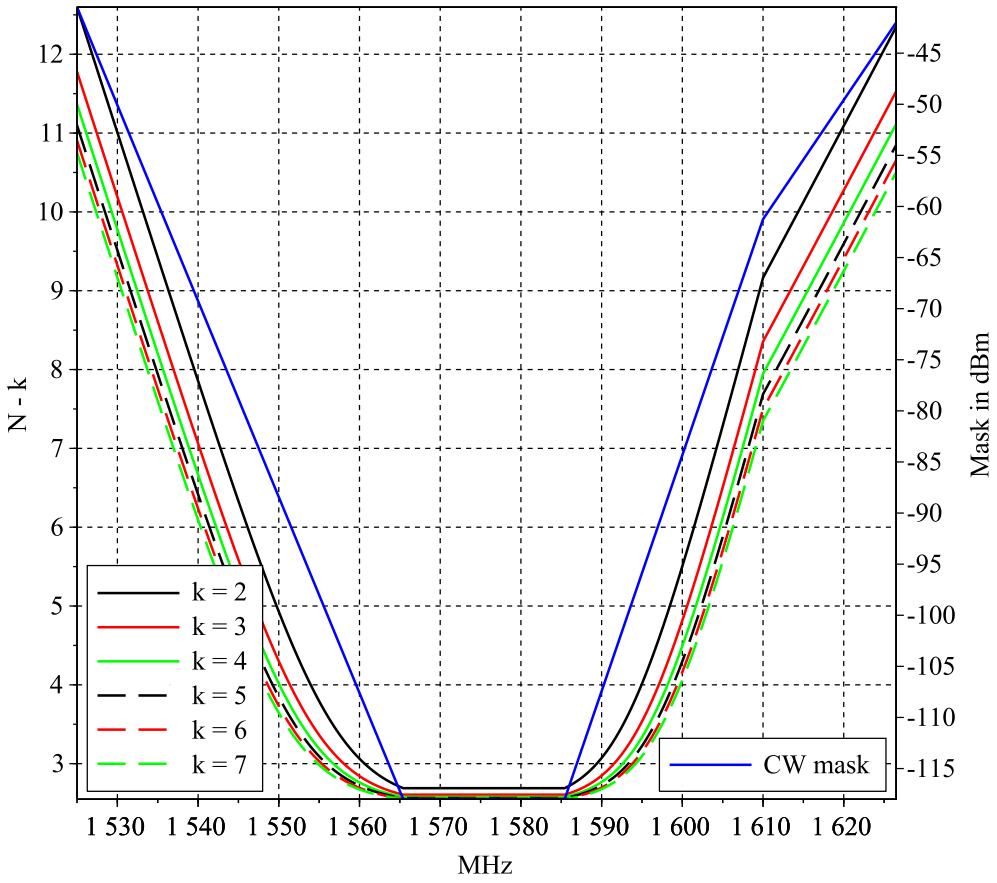


Figure 6.9: $N - k$ for Separate Sampling with sub-optimal filters, E1 band.

applying the following method for each band:

1. The interference mask is first sampled in frequency with 100 points per segment,
2. For each value of k (and the matching *crest factor* c) in table 6.1:
   (a) For each frequency sample of the mask:
      i. The corresponding amplitude A_{max} is calculated,
      ii. $N - k$ is determined using relation (6.28).

Figure 6.8 (and figure 6.9 respectively) reads then in this way: if the bandwidth of the extra RF filter required in the E5a band is larger than $[f_{5min}, f_{5max}] = [1166.45, 1186.45]$ MHz, down to 1155 MHz for example, then the CW+DME interference level could reach ~ -56 dBm at the input of the ADC at this frequency (intersection between the vertical grid line at $f = 1155$ MHz and the blue trace). Thus the total number of quantization bits would be

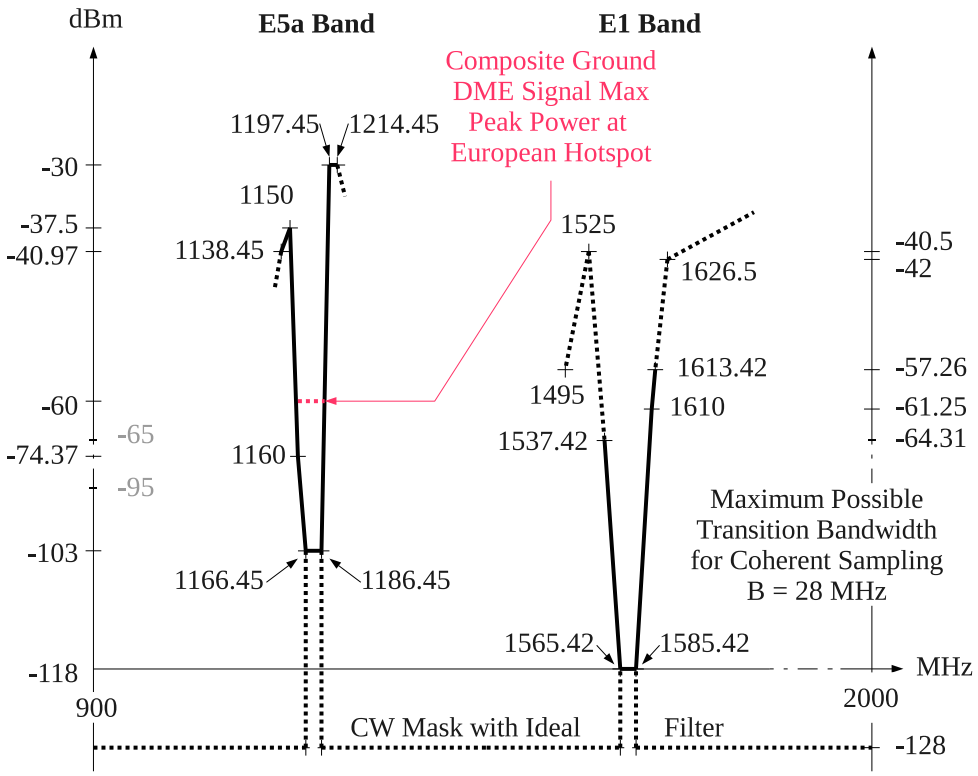
- $N \sim 12.2$ for $k = 2$ as $N - k \sim 10.2$ (intersection between the vertical grid line at $f = 1155$ MHz and the black trace),
- $N \sim 12.4$ for $k = 3$ as $N - k \sim 9.4$ (red trace),
- . . .
- $N \sim 15.3$ for $k = 7$ as $N - k \sim 8.3$ (dash-dotted red trace).

For the worst filters, up to a total of 20 bits could be needed for the E5a band ($N - k \sim 12.3$ for $k = 7$ at 1197.45 MHz) and up to 18 for the E1 band ($N - k \sim 10.7$ for $k = 7$ at 1525 MHz).

6.3.2 Coherent Sampling

At the input of the ADC the situation can be as deteriorated for coherent sampling as the one presented in figure 6.10. Figure 6.10 represents the interference threat at the input of the single ADC after filtering of the interference situation at the input of the receiver (figure 6.1) by the worst extra filters, the ones with the widest transition bandwidth $B_s = 28$ MHz [8]. At the input of the single ADC, the maximum level to be considered is then the coherent sum of both masks as explained previously in section 6.1.2. This sum is represented in figure 6.11 along with the individual masks for comparison. To establish this plot, each interference

8. It was shown in section 3.2.2 of chapter 3 that Coherent Sampling is no more possible for a transition bandwidth $B_s > 28$ MHz.



dBm do not include the preamplifier gain [26.5, 32.5] dB nor cable losses [3,12] dB

Figure 6.10: CW interference mask at receiver input with sub-optimal filters, Coherent Sampling.

mask was shifted from its center frequency ($f_1 = 1575.42$ MHz for E1 and $f_5 = 1176.45$ MHz for E5a) to 0. Thus, the x axis can represent directly the bandwidth of the extra filters, which should ideally be ± 10 MHz, but in reality could be enlarged by a non-zero transition bandwidth B_s at each side. For example, with a transition bandwidth $B_s = 15$ MHz, the total bandwidth of the extra filters being then ± 25 MHz, the maximum interference power to be considered is

- ~ -84 dBm (CW) at the output of the extra filter for the E1 band at $+25$ MHz,
- ~ -30 dBm (CW+DME) at the output of the extra filter for the E5a band at $+25$ MHz,
- ~ -30 dBm (CW+DME) globally at the input of the single ADC for the E1+E5a band at $+25$ MHz.

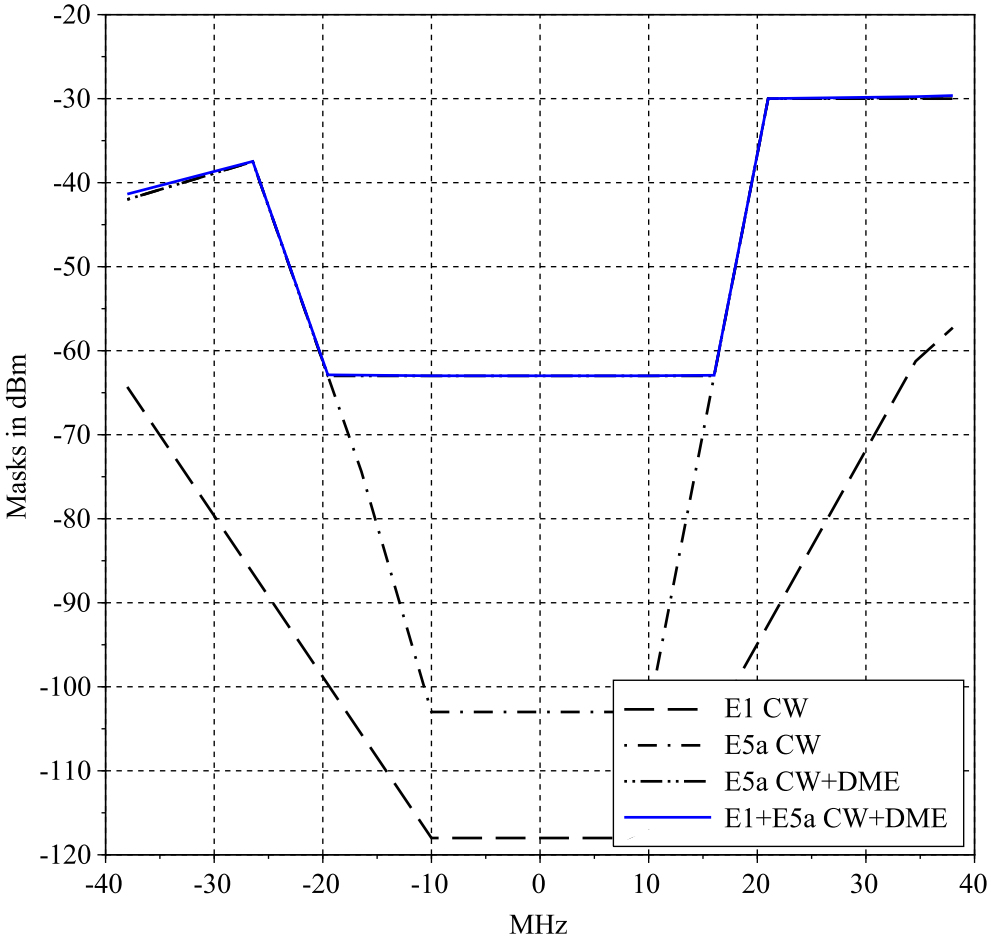


Figure 6.11: Coherent sum of the CW masks for Coherent Sampling with sub-optimal filters.

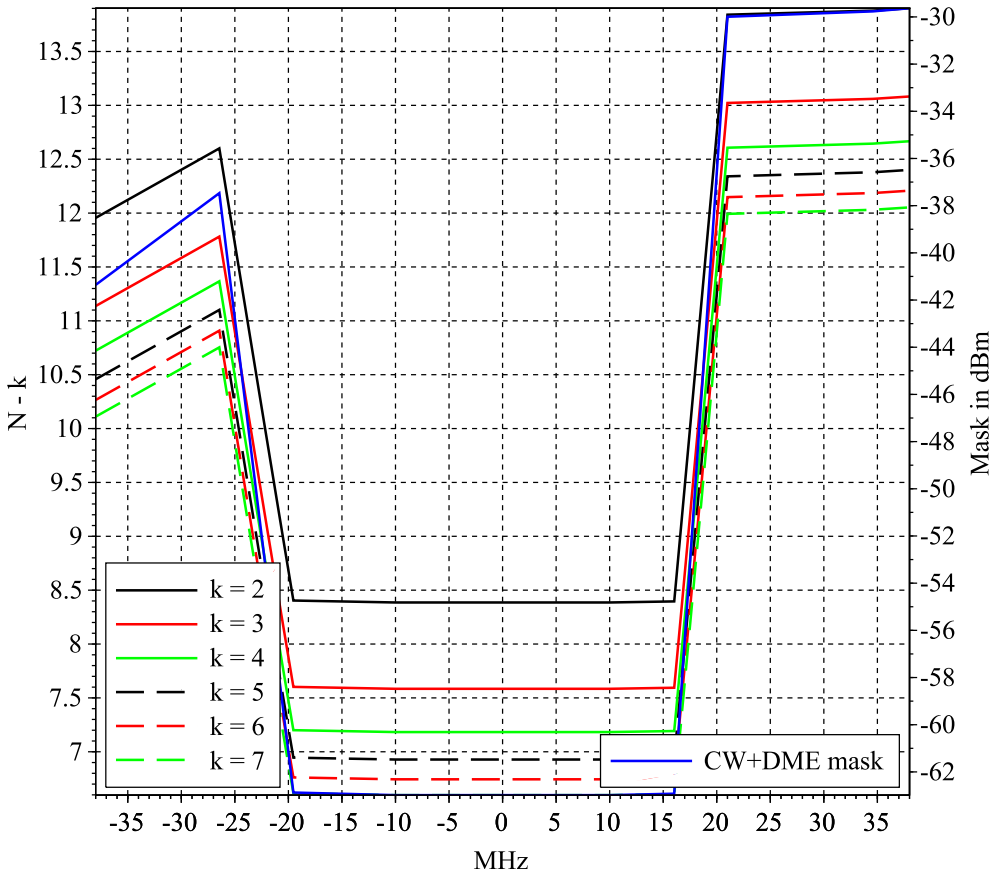


Figure 6.12: $N - k$ for Coherent Sampling with sub-optimal filters, E5a+E1 band.

Figure 6.12 plots the values of $N - k$ against the interference mask. This plot has been elaborated with the same method presented in section 6.3.1 for the Separate Sampling case. Here also up to a total of 20 bits could be required in the worst case ($N - k \sim 12.1$ for $k = 7$ at 38 MHz, that is $B_s = 28$ MHz).

6.4 CW Harmonic Distortion

As a quantizer is not a linear device, when a CW is applied at its input, a number of harmonics appears at its output. Let A be the amplitude of a full scale sine wave at the input of a mid-rise quantizer with $2L$ levels as represented in figure 6.2. Then, as calculated in appendix B, the amplitude of the $(2\nu + 1)^{th}$ harmonic (even harmonics are null) at

the output is

$$A_{2\nu+1} = \frac{2A}{(2\nu+1)\,L\pi}\left(1 + 2\sum_{k=1}^{L-1}\cos\left((2\nu+1)\sin^{-1}(k/L)\right)\right) \qquad (6.31)$$

The problem is that, even if one harmonic is very far in frequency from the original CW interference, due to aliasing it is folded back in the sampled band and possibly in the useful signal band. To be conservative it is decided not to allow any harmonic to be more powerful than the lowest value of the mask. That is, a minimum number of quantization bits $N = \log_2(L) + 1$, for which $P_{2\nu+1} = (A_{2\nu+1})^2/2$ (the power of the $(2\nu+1)^{th}$ harmonic) is lower than the lowest value of the mask $\forall\nu$, is to be used.

6.4.1 Separate Sampling

Figure 6.14 plots the minimum number of quantization bits N required so that no harmonic is more powerful than the floor of the mask, $P_{f5} = -103\,\text{dBm}$. Figure 6.15 presents the results of the same calculations for the E1 band, for which the floor is $P_{f1} = -118\,\text{dBm}$ this time. The method used to build plots 6.15 and 6.14 is as follows. First, the interference masks were sampled in frequency with 100 points per segment. Then, for each sample one by one, an algorithm which implements equation 6.31 was run.

This algorithm is represented in flow chart 6.13. A is equal to the amplitude of the sample and L is set to 2 as an initialization point, because it corresponds to the minimum number of bits, $N = \log_2(L) + 1 = 2$, for a quantizer with a number of quantization levels which is a power of 2. Depending on the band the algorithm is working on, P_f is set accordingly to P_{f5} or P_{f1}. Doing so, at the *Stop* point $N = \log_2(L) + 1$ is the minimum number of quantization bits for each frequency sample of the mask.

Figure 6.14 (and figure 6.15 respectively) reads in this way: if the bandwidth of the extra RF filter required in the E5a band is larger than $[f_{5min}, f_{5max}] = [1166.45, 1186.45]\,\text{MHz}$, down to 1155 MHz for example, then the CW+DME interference level could reach $\sim -56\,\text{dBm}$ at the input of the ADC at this frequency (intersection between the vertical grid line at $f = 1155\,\text{MHz}$ and the blue trace). Thus, the total number of quantization bits must not be less than $N = 6$ (intersection between the vertical grid line at $f = 1155\,\text{MHz}$ and the red trace).

For both bands the values calculated here are always less than the ones calculated in section 6.3.1. In the Separate Sampling architecture, the CW harmonic distortion by quantization is not a limit.

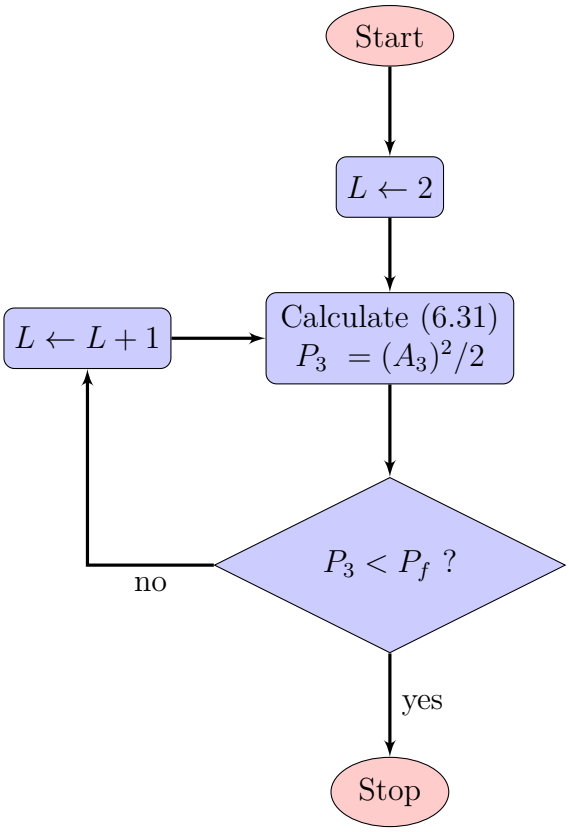


Figure 6.13: Flow chart of the harmonic distortion evaluation process.

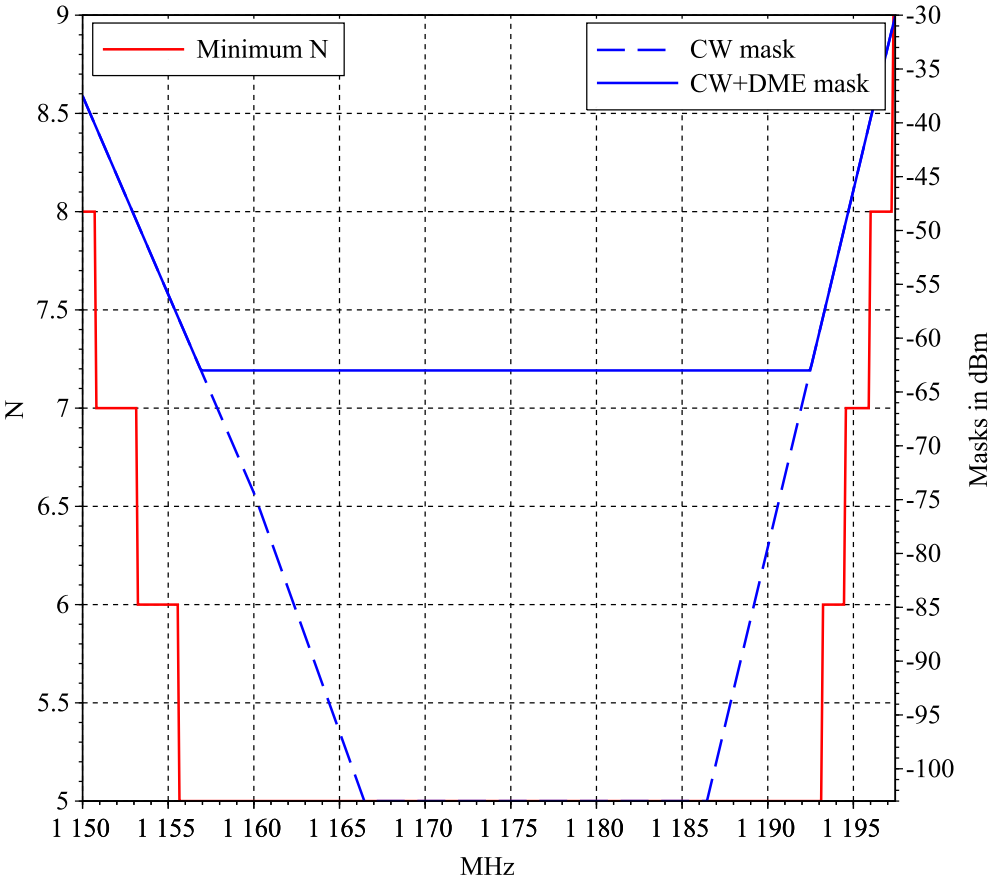


Figure 6.14: Minimum N for Separate Sampling with sub-optimal filters, E5a band.

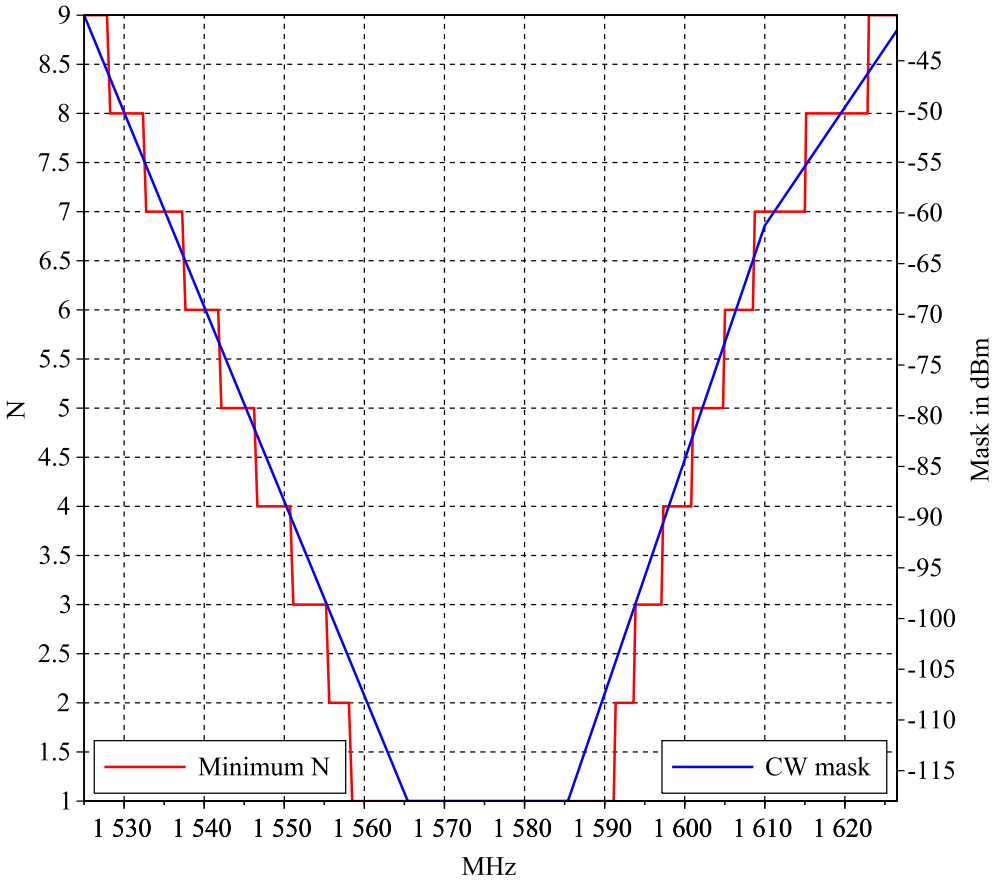


Figure 6.15: Minimum N for Separate Sampling with sub-optimal filters, E1 band.

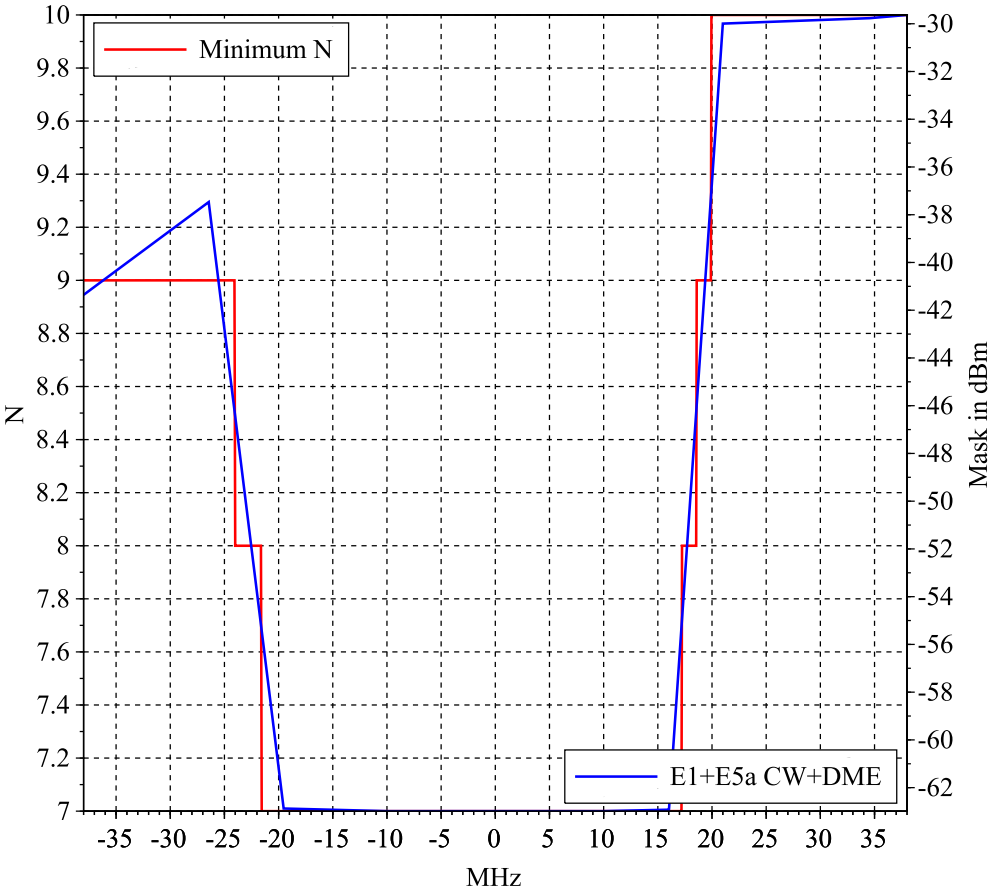


Figure 6.16: Minimum N for Coherent Sampling with sub-optimal filters, E5a+E1 band.

6.4.2 Coherent Sampling

Normally, as stated in section 6.1.2, the sum of two CWs at the input of the single ADC in this case should be considered. Nevertheless, as it can be observed in figure 6.11, the E1 mask is so low in comparison to the E5a mask that the coherent sum of both masks is nearly equal to the E5a mask. That is why the number N of quantization bits is calculated on the basis of one CW only, which power is essentially equivalent to the coherent sum of both masks.

The results are presented in figure 6.16. One can note that N is logically of the same order of magnitude as in the case of the Separate Sampling of the E5a band, but higher as the floor of the mask is $-118\,\mathrm{dBm}$ in this case instead of $-103\,\mathrm{dBm}$.

Here also the calculated values are always lower than the ones calculated in section 6.3.2. In the Coherent Sampling architecture the CW harmonic distortion by quantization is not a limit either.

It should be noted that after quantization the amplitude of a CW which reaches the full scale of the quantizer is lower than before, so that the different interference masks could be slightly reduced according to the attenuation plotted in figure B.2. However, as this attenuation is less than 1 dB as soon as the total number of quantization bits is greater than 3, it is decided to ignore it.

6.5 Conclusion

The number of bits N required to quantize the whole range of the signal present at the input of the ADC(s) was investigated in this chapter. A first result is that the removal of the AGC costs 3 more bits than strictly necessary compared to a classical architecture. Furthermore, it was shown that N greatly depends on the performance of the required extra RF filters, whether it be for the Separate Sampling architecture or for the Coherent Sampling one. Considering Separate Sampling, up to 20 bits could be required for the E5a band and up to 18 bits for the E1 band, in the case of poor quality extra filters. For Coherent Sampling, it has appeared that the interference situation at the input of the single ADC is nearly the same as for the Separate Sampling of the E5a band, because the interference threat in this band completely overcomes the one in the E1 band. So the results are similar, up to 20 bits could be necessary if the extra filters are far from meeting their specifications. It was also calculated that even for the minimum value of N, that is for ideal extra RF filters, quantization never introduces CW harmonics higher than the interference mask.

6.6 References

[1] EUROCAE, *Minimum Operational Performance Specification for Airborne Open Service Galileo Satellite Receiving Equipment*, EUROCAE Std., December 2010.

[2] S. J. Orfanidis, *Electromagnetic waves and antennas*, ECE Department Rutgers University 94 Brett Road Piscataway, NJ 08854-8058, July 2 2014, last accessed 01/05/2015. [Online]. Available: http://eceweb1.rutgers.edu/~orfanidi/ewa/

[3] C. J. Hegarty, "Analytical Model for GNSS Receiver Implementation Losses," *Navigation*, vol. 58, no. 1, pp. 29–44, 2011. [Online]. Available: http://dx.doi.org/10.1002/j.2161-4296.2011.tb01790.x

[4] S. Gunawardena, "GNSS Antenna and Receiver Design Considerations for High Accuracy Applications," InsideGNSS/Novatel Webinar on Precise Positioning Techniques: GNSS Error Sources & Mitigation, December, 15 2014, last accessed 09/03/2015. [Online]. Available: www.insidegnss.com/pdf/Inside_GNSS_Precise_Positioning_webinar_121514_final_secured.pdf

Signal Dynamic Range Compression

7

After digitization, depending on the actual attenuation obtained by the extra RF analog filters to the interference signal, it may be necessary to digitally filter the signal in order to mitigate the remaining interference threat.

If the performance of the extra analog filters are too weak, the order of the digital filters could be proportionally high and then their computational cost could reach high values as it is shown in the first part of this chapter.

The question then arises on the possibility to decrease the binary throughput immediately after the ADC(s), that is the way to discard as many bits as possible, when feasible, as each bit reduced would decrease not only the calculation burden of theses filters but also the processing workload downstream in general. The second and last parts of this chapter focuses on these aspects through the study of signal dynamic range compression methods.

7.1 Calculation Workload Evaluation

7.1.1 FIR Filter Order Estimation

The hypothesis is made here that linear phase FIR (Finite Impulse Response) filters are used to lower the interference level after sub-optimal extra RF analog filters. This choice is interesting because the linear phase property preserves the phase characteristic of the signal, which can not be guaranteed with IIR (Infinite Impulse Response) filters. The following

formula, from [1], was then used to estimate the filter order

$$\hat{M} = \frac{D_\infty(\delta_p, \delta_s) - f(\delta_p, \delta_s) \cdot (\Delta f)^2}{\Delta f} + 1 \tag{7.1}$$

with

$$\begin{aligned} D_\infty(\delta_p, \delta_s) = \big(&0.005309(\log_{10}(\delta_p))^2 + 0.07114\log_{10}(\delta_p) \\ &-0.4761) \times \log_{10}(\delta_s) - \big(0.00266(\log_{10}(\delta_p))^2 \\ &+0.5941\log_{10}(\delta_p) + 0.4278) \end{aligned}$$

and

$$f(\delta_p, \delta_s) = 11.012 + 0.51244\,(\log_{10}(\delta_p) - \log_{10}(\delta_s))$$

The parameters are:

- f_p the normalized [1] passband edge frequency,
- f_s the normalized stopband edge frequency,
- $\Delta f = (f_s - f_p)$ the normalized transition bandwidth,
- δ_p the passband ripple [2],
- δ_s the stopband ripple.

It is noteworthy that, as relation (7.1) is defined for a lowpass filter, f_p and f_s are not the passband frequencies in our case, but their lowpass equivalents. Thus, $f_p = 10\,\text{MHz}/F_s$, that is half of the useful bandwidth B_1 or B_{5a}. However, the order $\hat{M}$ is the same for the corresponding bandpass filter as it is shown hereafter.

Let $h_{lp} \multimap\!\circ\, H_{lp}$ be the impulse response of the FIR lowpass filter and H_{lp} its transfer function

$$h_{lp}[k] = 0 \quad \forall k \notin [0, \hat{M} - 1] \tag{7.2}$$

The corresponding bandpass transfer function can be defined as follows

$$H_{bp}(f) = H_{lp}(f - f_c) + \overline{H_{lp}(-f - f_c)} \tag{7.3}$$

where f_c is the center of the passband. In this way the Hermitian symmetry property is set, so that the resulting impulse response of the filter

1. The normalized frequency is the frequency divided by the sampling frequency.
2. $10\log_{10}(\delta_p) = -10\,\text{dB}$ in the rest of this thesis, to match the 10 dB attenuation step on each side of the passband.

is real-valued. This impulse response is obtained by the inverse Fourier transform

$$h_{bp}[k] = h_{lp}[k]e^{j2\pi f_c kT_s} + \overline{h_{lp}[k]}e^{-j2\pi f_c kT_s} \quad \forall k \tag{7.4}$$

with T_s the sampling period.

$$h_{bp}[k] = 2\Re\left\{h_{lp}[k]e^{j2\pi f_c kT_s}\right\} \quad \forall k \tag{7.5}$$

In the case where h_{lp} is also real-valued

$$h_{bp}[k] = 2h_{lp}[k]\cos\left(2\pi f_c kT_s\right) \quad \forall k \tag{7.6}$$

Using definition (7.2), it is possible to conclude that

$$h_{bp}[k] = 0 \quad \forall k \notin [0, \hat{M} - 1] \tag{7.7}$$

Relation (7.7) shows that the length of the bandpass filter impulse response h_{bp} is equal to the length of the lowpass filter impulse response h_{lp}.

7.1.2 Requirements on Digital Filters

As examples of the digital filtering operations to be performed, figure 7.1 for the E5a[3] band and figure 7.2 for the E1 band represent the minimum attenuation, versus frequency, which is needed to counterbalance the less efficient analog filters, in the Separate Sampling case. It corresponds to the worst case of extra RF filters with an actual bandwidth larger than 47.45 MHz in the E5a band and 101.5 MHz in the E1 band. The attenuation is calculated from figure 6.7 for each band respectively, so that in-band aliasing of an out-of-band threat is attenuated to the minimum in-band mask level, -103 dBm in the E5a band and -118 dBm in the E1 band.

If FIR filters are to be used, figure 7.3 for the E5a band and figure 7.4 for the E1 band give an estimation of the minimum order of the filter vs transition bandwidth B_s. Figure 7.5 for the E5a band and figure 7.6 for the E1 band propose an estimation of the induced calculation workload, versus transition bandwidth B_s.

3. The Fourier transform of a sampled signal, as well as the transfer function of a digital filter, is periodic in F_s (the sampling frequency), as recalled in appendix A by relation A.1. Therefore, it is equivalent to consider any period of the Fourier transform of a sampled signal or of the transfer function of a digital filter. In the remaining of this document, it was decided to work on the period around the original analog carrier frequency ($f_1 = 1575.42$ MHz for E1 or $f_5 = 1176.45$ MHz for E5a), rather than any other period, especially the periods lower in frequency. These periods closer to 0 are sometimes noted *resulting* IF, in reference to the IF conversion process which occurs in an analog receiver. It is believed that, keeping the spectral representation at its original place helps to understand the digital operation which occurs.

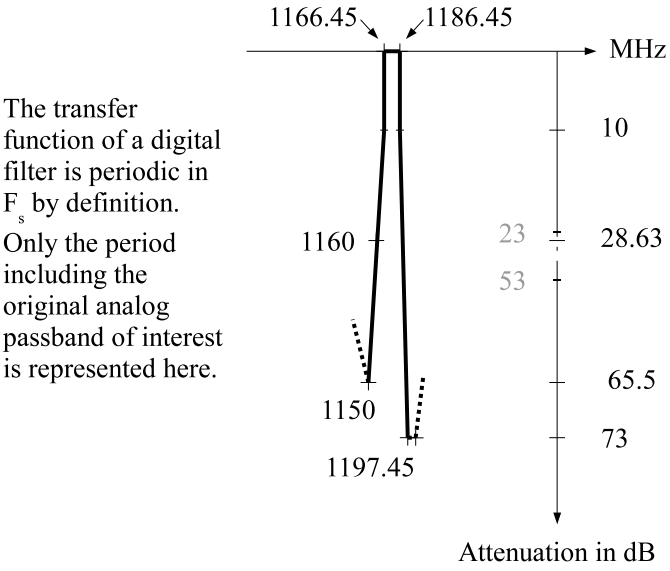


Figure 7.1: Minimum attenuation required at the output of the E5a band ADC, Separate Sampling, when sub-optimal extra RF filtering is used.

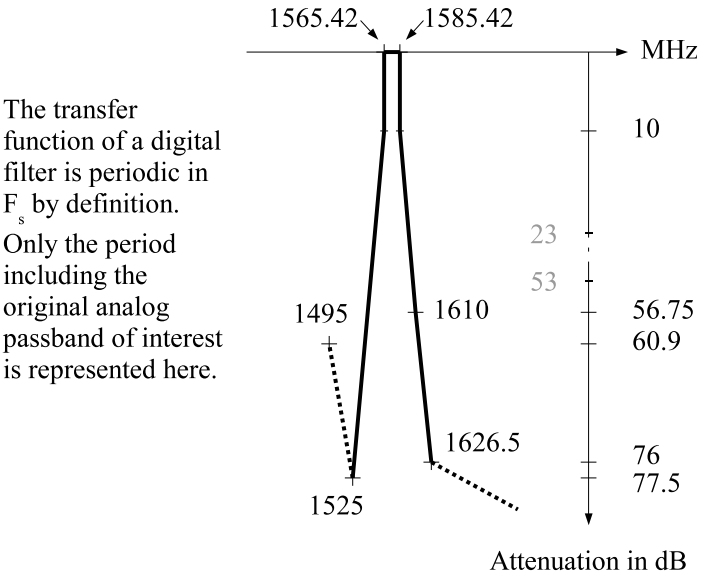


Figure 7.2: Minimum attenuation required at the output of the E1 band ADC, Separate Sampling, when sub-optimal extra RF filtering is used.

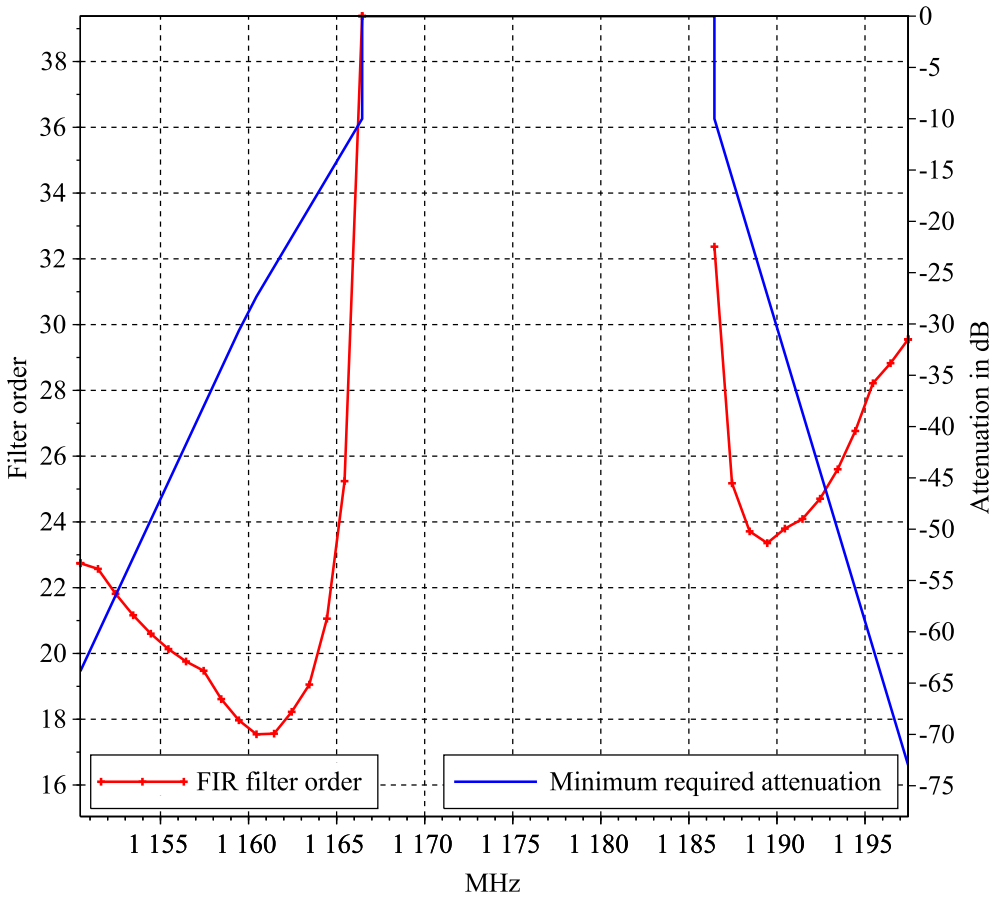


Figure 7.3: Minimum FIR filter order to reach the required attenuation on the E5a band, Separate Sampling.

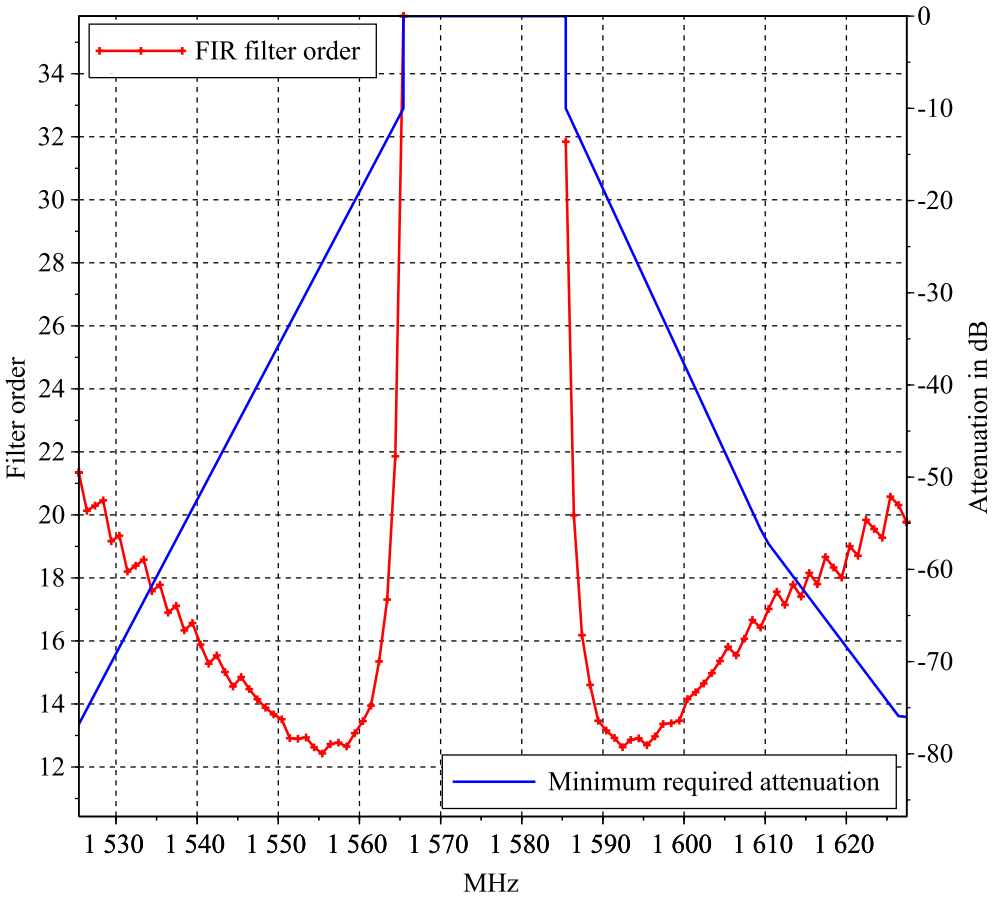


Figure 7.4: Minimum FIR filter order to reach the required attenuation on the E1 band, Separate Sampling.

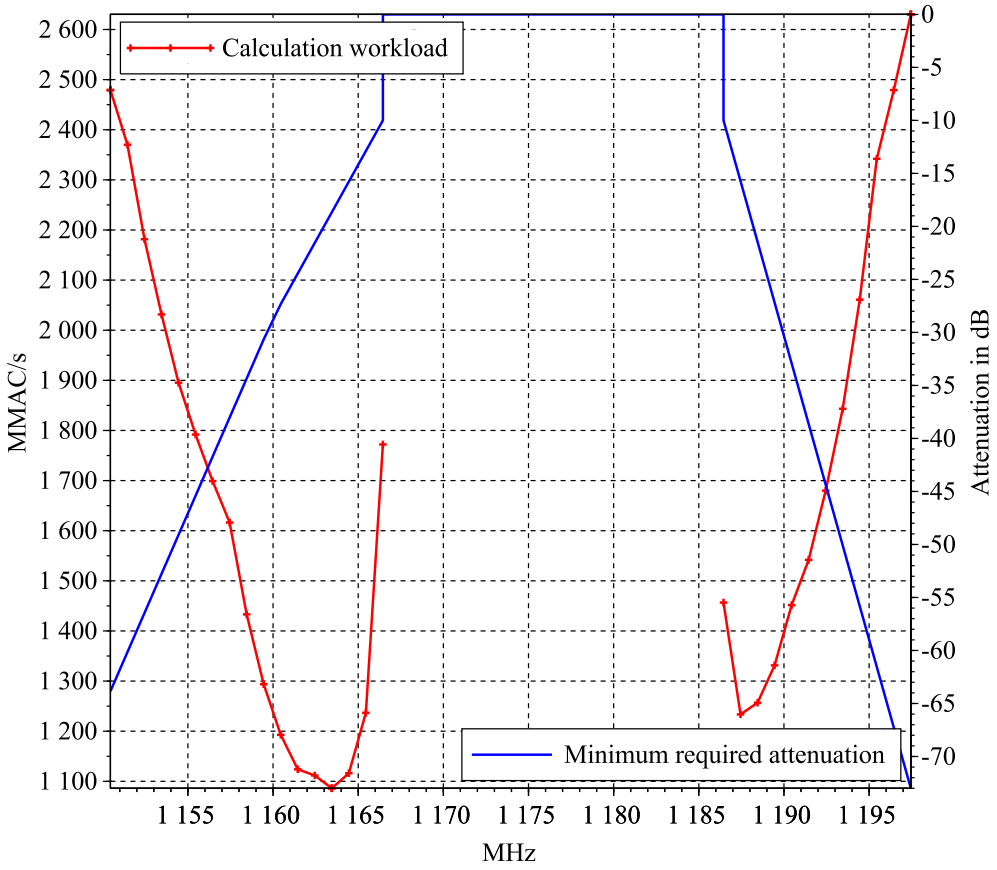


Figure 7.5: Estimated calculation workload on the E5a band, Separate Sampling.

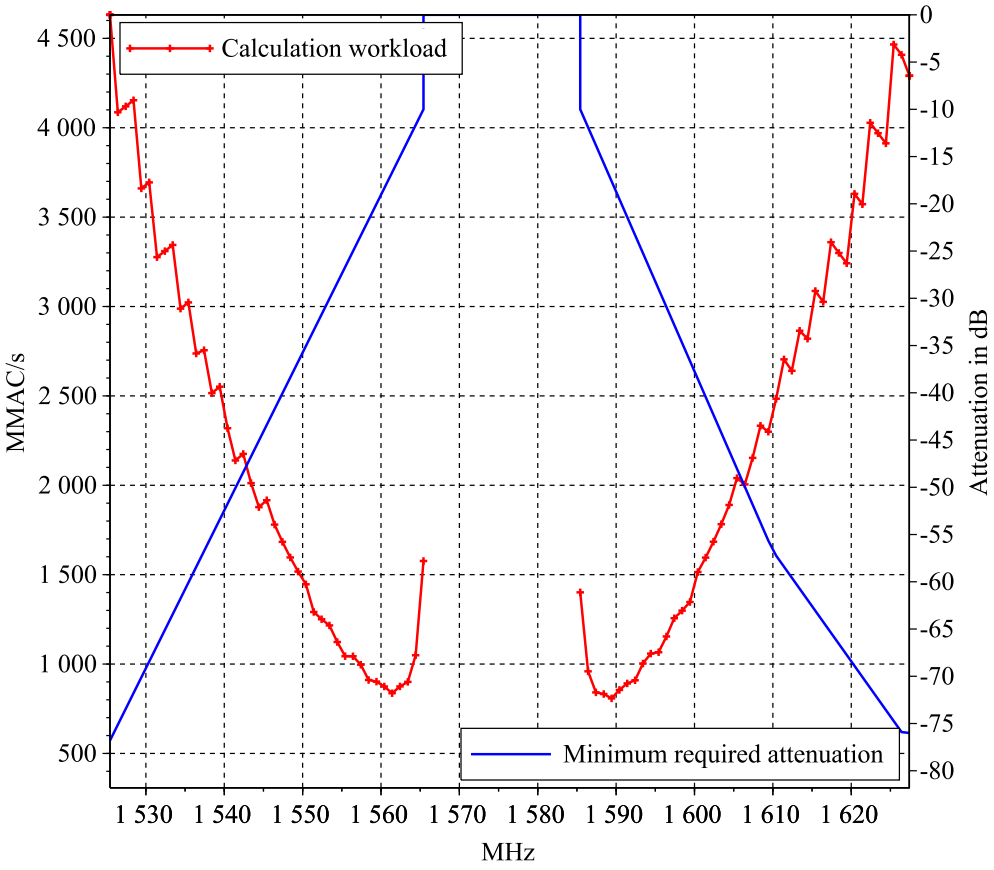


Figure 7.6: Estimated calculation workload on the E1 band, Separate Sampling.

Figure 7.3 (and figure 7.4 respectively) reads in this way: if the bandwidth of the extra RF filter required in the E5a band is larger than $[f_{5min}, f_{5max}] = [1166.45, 1186.45]$ MHz, down to 1155 MHz for example, then the minimum attenuation to be provided by digital filtering is ~ 47 dB at this frequency (intersection between the vertical grid line at $f = 1155$ MHz and the blue trace). Thus the estimated minimum FIR filter order is $\hat{M} = 21$ (intersection between the vertical grid line at $f = 1155$ MHz and the red trace). The same principle stands for figures 7.5 and 7.6, but applied to the estimated calculation workload.

The calculation workload is estimated here by the simple product of the filter order $\hat{M}$ with the minimum sampling frequency, which is a function of the transition bandwidth B_s as presented in chapter 3. So this estimated workload does not take into account the various optimization techniques which could be used in the actual implementation of these FIR filters.

The workload can reach 2630 MMAC/s for the E5a band and 4632 MMAC/s for the E1 band. The MAC unit corresponds to the computation of the product of two numbers and the addition of the result to an accumulator. This unit is used to evaluate the performance of signal processors as for example the Analog Devices TigerSHARC ADSP-TS201S DSP [2], which can reach 4.8, 40-bits GMAC/s.

Compared to this last figure, 2630 MMAC/s or even 4632 MMAC/s seem to be attainable. However, these filtering operations are just the beginning of a long series of signal processing tasks, including the correlation step which is very resource consuming. The more computational resources the filtering consumes, the less remains for other tasks.

Therefore the question of decreasing the number of bits needed to encode the signal before the filtering operation, as it lowers the hardware elementary arithmetic demand, becomes a topic of hight interest.

7.2 Signal Dynamic Range Compression

Three methods were investigated to reduce this number of bits after the ADC for the DS-DF-SDR Galileo receiver. In the first method the receiver measures the real parameters of its installation on board, and then adjusts the data to the minimum number of bits required to encode the signal. The second method is the digital equivalent of the analog AGC as it estimates the mean power of the digital signal, and discards in function as many bits as possible, without degrading the fidelity of the signal. The last method tries to compress in amplitude the dynamic of the signal, preserving as much as possible the useful signal.

7.2.1 Adaptation to Aircraft Installation

Once the receiver is installed in the aircraft, a measurement of the actual antenna gain G_a and of the actual cable losses L_a could be made by a technician [4] who would then be able to set these parameters in the receiver. Knowing G_a and L_a, equation (6.28) is updated

$$N_a - k \geq \log_2 \left(\frac{\sqrt{G_a/L_a} \times A_{max} + c \cdot \sigma_a}{c \cdot \sigma_a} \right) \tag{7.8}$$

with $\sigma_a = \sqrt{N1 \times (B_{5a} + B_1)}$, as detailed in section 6.1.1.3 of chapter 6, and A_{max} is the maximum interference level, as defined in section 6.1.2.1 of chapter 6 also. It is also recalled that c is the *crest factor* of the noise and k is the number of quantization bits devoted to the useful signal in a non-interference environment. N_a is the total number of quantization bits, knowing G_a and L_a.

Under the approximation made in section 6.1.1.2 of chapter 6 that "the noise contribution of the cable is always negligible in comparison to the noise introduced upstream", equation (6.11) can be updated to:

$$N1 \simeq k_B \left(T_{sky} + (F-1)\, T0 \right) G_a/L_a \tag{7.9}$$

which leads finally to

$$N_a - k \geq \log_2 \left(\frac{A_{max} + c \cdot \sqrt{k_B \left(T_{sky} + (F-1)\, T0 \right) \times (B_{5a} + B_1)}}{c \cdot \sqrt{k_B \left(T_{sky} + (F-1)\, T0 \right) \times (B_{5a} + B_1)}} \right) \tag{7.10}$$

For a set number of bit k, N_a really needed could then be calculated and compared to the value of N determined during the design phase, as in sections 6.2 or 6.3 of chapter 6. The ADC(s) implemented in the receiver has N quantization bits. The $N - N_a$ surplus bits can then be thrown away systematically without risk. The bits to discard are the MSBs (Most Significant Bits), as they encode the highest dynamic of the quantizer which corresponds to a signal amplitude higher than the mask. It is remembered that for interference with power higher than the mask, receiver proper operation is not guaranteed, only integrity requirements are to be met.

Table 7.1 gives the bound values of $N_a - k$, that is in the best situation, with ideal analog filters. Comparing table 7.1 with table 6.2, it can be noted that for Separate Sampling 3 MSBs can be discarded systematically

4. Realistically, this would not be acceptable by manufacturers due to the cost of such an operation. However, it seemed interesting to elaborate the reasoning to its end.

k	Optimum *crest factor*	Coherent Sampling E5a+E1: $N_a - k \geq$	Separate Sampling E5a: $N_a - k \geq$	Separate Sampling E1: $N_a - k \geq$
1	N/A	N/A	N/A	N/A
2	0.996	5.9	6.4	0.2
3	1.758	5.1	5.6	0.1
4	2.345	4.7	5.2	0.1
5	2.820	4.4	4.9	0.1
6	3.224	4.2	4.7	0.1
7	3.591	4.1	4.6	0.1

Table 7.1: $N_a - k$ with ideal analog filters.

on E5a and 2 on E1. In the same way, by comparison of table 7.1 with table 6.3, it is deduced that for Coherent Sampling, up to 3 MSBs can be deleted automatically.

As this method is not an *aircraft installation independent* solution and because it appears to be costly for the manufacturers, due to the human intervention, it was no more studied.

7.2.2 Digital AGC

This process is equivalent to an analog AGC, except that it is located after the ADC(s). A simple implementation of a digital AGC can be found in [3] for example. The digital AGC measures in real time the actual mean power of the samples of the signal and consequently calculates the number of bits needed to correctly represent it. The surplus MSBs can then be discarded. The advantage of the digital AGC over the analog one is that is does not require a VGA (Variable Gain Amplifier) in the analog RF front-end, but only simpler fixed-gain amplifiers. However, as N, the number of bits of the quantizer, is definitely set during the design phase (according to the maximum interference threat at the input of the ADC(s)), the signal is systematically quantized with N bits. This is sub-optimal, because most of the times a lot of bits will be discarded after the digital AGC. Indeed, the full dynamic of the quantizer is used only with interference which power reaches or exceeds the mask, that is normally relatively infrequently. Although the digital AGC seemed interesting to study, it was decided not to consider it further in this thesis. An inspiring work for the study of the operation of the digital AGC could be [4], which describes how the (analog) AGC can be used to mitigate CW interference in GNSS receivers.

7.2.3 Dynamic Range Reduction using a Non-Linear Function

This is the third signal dynamic range compression technique envisioned and the subject of the rest of this chapter. The main idea is to compress the amplitude dynamic of the input signal to the ADC (which is supposed corrupted by at most one CW interference) as much as possible so that a maximum number of the MSBs, useless after this operation, can be discarded. Of course the useful signal must be preserved as much as possible, especially when there is no interference. It means that linearity must be preserved as much as possible over the full range of the useful signal. When the interference is present, the compression of the dynamic must not produce other interferences with a level higher than the mask. It must be noted that, as our study is limited to one CW interference, it only applies to the Separate Sampling architecture, because in the Coherent Sampling case one CW interference should be considered per band, that is a total of two, as the assumption is made in section 6.1.2.1 of chapter 6. Nevertheless, the conclusion will show it is not an issue.

7.3 Compression Functions

Two non-linear functions with low computational complexity were considered. Their evaluation was conducted with a tradeoff in mind: they should provide the best compression ratio while not producing harmonics with power higher than the mask.

7.3.1 The Linear-then-Log Function

7.3.1.1 Definition

This function F_{ll} is represented in figure 7.7. Its main advantage is that it is fully linear before the corner value *X0*: if *X0* is set greater than $c \cdot \sigma_{2,max}$ [5], the dynamic compression operation is completely transparent for the useful signal in the nominal situation, i.e. when there is no interference.

5. $\sigma_{2,max}$ is defined in section 6.1.2.1 of chapter 6 as the maximum standard deviation of the noise at the input of the ADC. However, in practice the values at the antenna port have been used in place of the values at the input of the ADC. This choice was made for the reason detailed in section 6.1.1.2 of chapter 6: the noise factor of the RF hardware front-end F_{RF} could not be assessed at the time of this writing, then it was not possible to take it into account. So, in the calculations $\sigma_{2,max}$ has been replaced by σ_0 and the interference masks are directly considered at the antenna port.

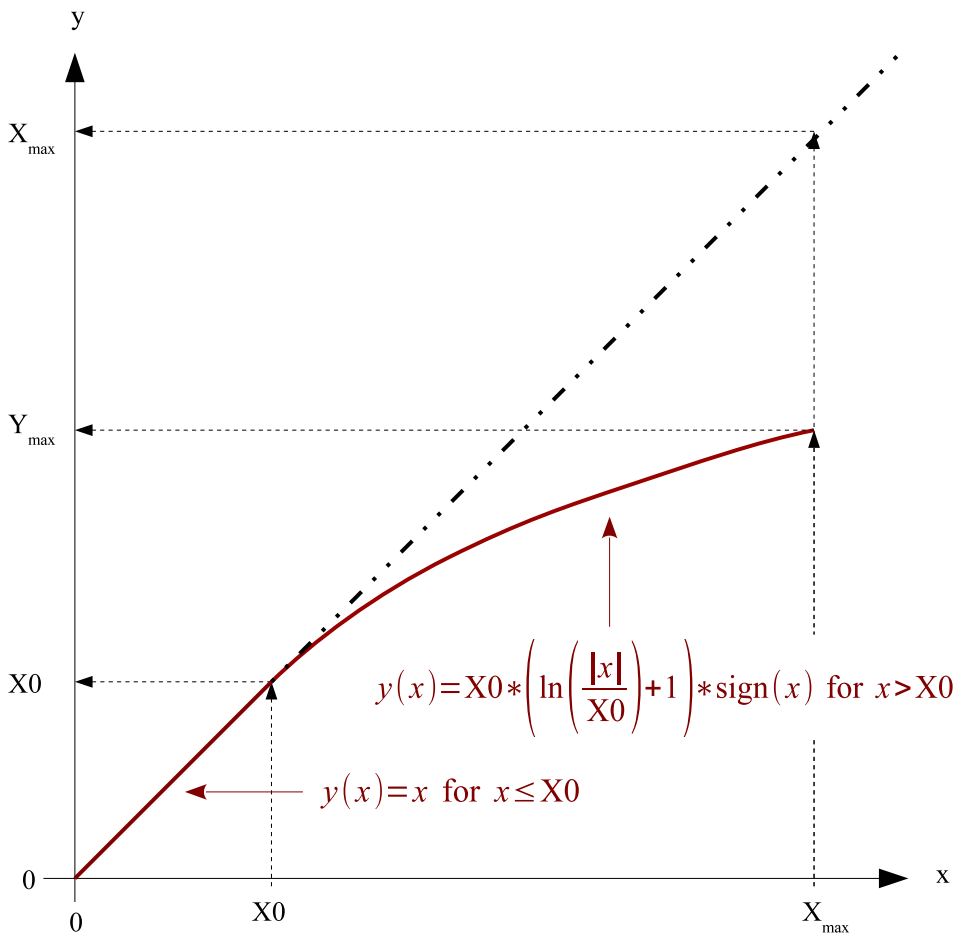


Figure 7.7: The linear-then-log function.

7.3.1.2 Response to a CW

The effect of this function F_{ll} on a CW parametrized by its mean power P, its frequency f_0 and its initial phase ϕ_0 (set to 0 here without loss of generality) was evaluated through the Fourier coefficients of the output signal. Indeed, as the input CW interfering signal $x(t) = \sqrt{2P}\sin(2\pi f_0 t)$ is periodic, the output $y(t) = F_{ll}(x(t))$ is also periodic with the same period and can then be decomposed in a Fourier series as:

$$y(t) = \sum_{n=-\infty}^{+\infty} C_n e^{i2\pi n f_0 t} \tag{7.11}$$

where

$$C_n = f_0 \int_{-\frac{1}{2f_0}}^{\frac{1}{2f_0}} F_{ll}(x(t)) e^{-i2\pi n f_0 t} dt, n \in \mathbb{Z}. \tag{7.12}$$

The single sided power spectrum of y is made of lines located at frequencies nf_0 with power $2(C_n)^2$. It must be noted that even if a harmonic is very far in frequency from the original CW interference, due to aliasing it is folded back in the sampled band and possibly in the most sensitive part of the spectrum, the bandpass of the useful signal. Like in section 6.4 of chapter 6, to be conservative it is decided to not allow any harmonic to be more powerful than the lowest value of the mask, that is $P_{f5} = -103\,\text{dBm}$ for the E5a band and $P_{f1} = -118\,\text{dBm}$ for the E1 band.

7.3.1.3 Performance Evaluation

To measure the performance of this linear-then-log function, the CW interference masks represented in figure 6.7 for the E5a and the E1 bands were sampled in frequency with 100 points per segment. Then, for each sample one by one, the algorithm represented in flow chart 7.8 was run, with P_{mask} set to the power of the sample. *X0* is set to $\sqrt{2P_{mask}}$ as an initialization point, because this value is high enough so that the algorithm will not miss the target value, which is less or equal to $\sqrt{P_{mask}}$ by definition. Depending on the band the algorithm is working on, P_f is set accordingly to P_{f5} or P_{f1}. Doing so, at the *Stop* point *X0* is defined as low as possible (better dynamic compression) but without reinjecting in-band secondary harmonics that are more powerful than the interference mask.

In parallel to the calculation of *X0*, the attenuation supplied by the function F_{ll} is calculated as the ratio between the power of the first harmonic at the output of the function and the power of the CW mask

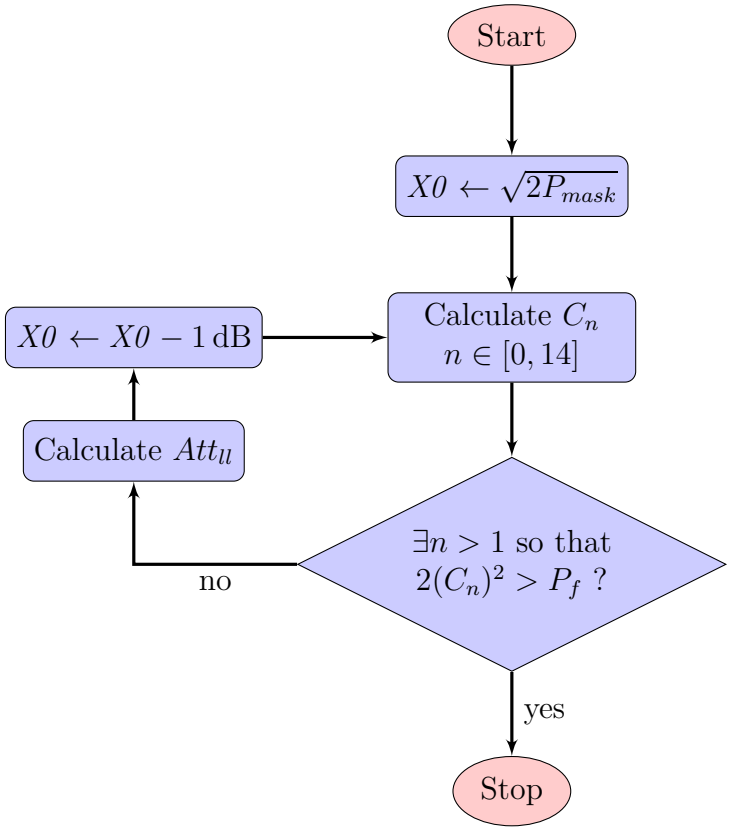


Figure 7.8: Flow chart of the performance evaluation process.

level, P_{mask}, at the input

$$Att_{ll} = \frac{2(C_1)^2}{P_{mask}} \tag{7.13}$$

At the end of the loop, the last calculated attenuation is the maximum attenuation which can be provided by the function for power P_{mask}.

It must be said here for the sake of completeness that the calculations above were done on a CW interference which is not quantized but with a continuous amplitude. It means that the results may be optimistic, especially for small values of k, as it is known that quantization introduces its own share of harmonics. As a consequence also, there was no optimum value for the *crest factor* this time. c was set to 3.591, the value corresponding to $k = 7$, as the assumption is made that the useful signal will be quantized with an ever increasing number of bits in the future.

The results are presented in figures 7.9, 7.11 and 7.13 for the E5a band and in figures 7.10, 7.12 and 7.14 for the E1 band, which will be elaborated on in the next section.

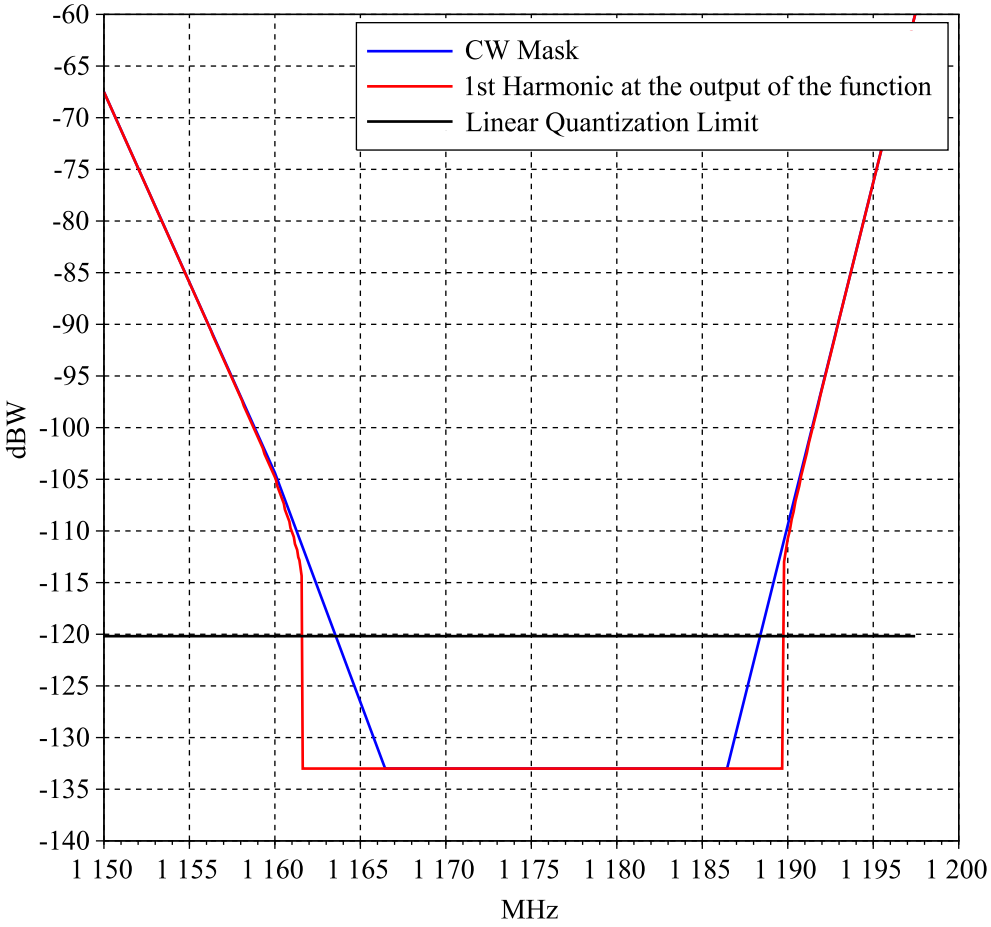


Figure 7.9: Compression effect of the linear-then-log function on the E5a CW interference mask.

7.3.1.4 Full Efficiency Band

The first set of figures 7.9 and 7.10, superimpose the CW interference mask at the input of F_{ll} and the corresponding power of the first harmonic $2(C_1)^2$ at the output, for the E5a and E1 band, respectively.

The linear quantization limit is also plotted. It is the power P_{lin} of a CW which amplitude is equal to the maximum amplitude of the noise at the input of the ADC

$$P_{lin} = \frac{(c \cdot \sigma_{2,max})^2}{2} \tag{7.14}$$

Figure 7.9 (and figure 7.10 respectively) reads in this way: if the bandwidth of the extra RF filter required in the E5a band is larger than $[f_{5min}, f_{5max}] = [1166.45, 1186.45]$ MHz, down to 1155 MHz for example, then the CW interference level could reach ~ -86 dBW at the input of the ADC at this frequency (intersection between the vertical grid line at

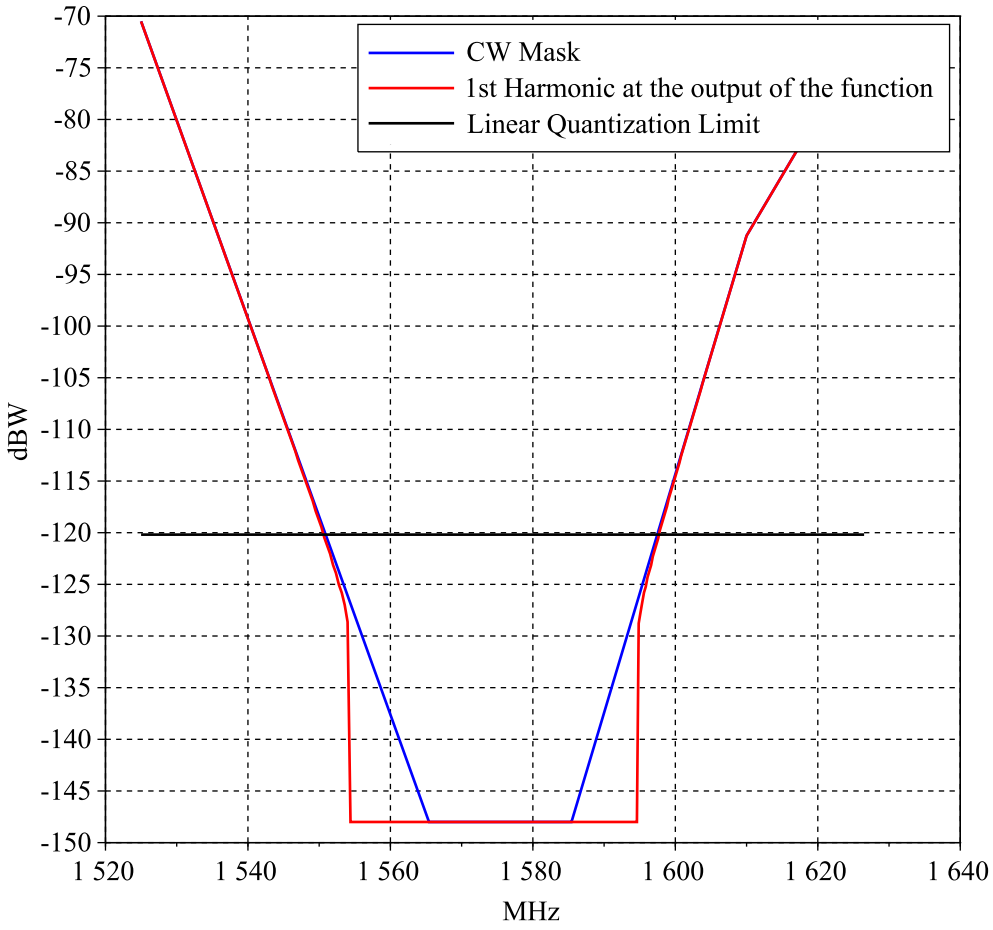


Figure 7.10: Compression effect of the linear-then-log function on the E1 CW interference mask.

$f = 1155\,\text{MHz}$ and the blue trace). As the red trace and the blue one are merged at this frequency (intersection between the vertical grid line at $f = 1155\,\text{MHz}$ and the red trace), it means that the power of the first harmonic at the output of the function is equal to the power of the CW signal at its input. In fact compression is not possible at this frequency: no *X0* satisfies condition $2(C_n)^2 > P_f$ in algorithm 7.8. However, if the bandwidth of the extra RF filter spreads down to only 1165 MHz for example, the CW interference level could reach $\sim -127\,\text{dBW}$ at the input of the ADC at this frequency. This time, the power of the first harmonic is at the floor of the mask, $-133\,\text{dBW}$: an attenuation of $\sim 6\,\text{dB}$ is provided by the function.

From these plots it can be defined the full efficiency band of this function, the band over which after the dynamic reduction there is no more need of filtering because the level of the first harmonic lies under the in-band mask. Graphically it corresponds to the frequency range over which the power of the first harmonic at the output of the function is equal to the floor of the mask, $-133\,\text{dBW}$ for E5a and $-148\,\text{dBW}$ for E1. The data from these plots show that the full efficiency band is equal to $[1162, 1190]\,\text{MHz}$ for E5a and to $[1554, 1594]\,\text{MHz}$ for E1. This result by itself is interesting.

The second set of figures 7.11 and 7.12, represent directly the attenuation provided by the function, Att_{ll} as presented in equation (7.13). The function F_{ll} presented in figure 7.7 provides up to $\sim 21\,\text{dB}$ of attenuation in both E5a and E1 bands at the frequencies indicated in figure 7.11 and 7.12.

7.3.1.5 Quantization Bit Saving

The last set of figures 7.13 and 7.14 show the quantization bit saving offered by the dynamic compression function F_{ll}.

The quantization bit saving can be determined using equation (6.28), recalled here for the sake of simplicity

$$N - k \geq \log_2 \left(\frac{\sqrt{G_{max} L_{min}} \times A_{max} + c \cdot \sigma_{2,max}}{c \cdot \sigma_{2,min}} \right) \qquad ((6.28))$$

N is the total number of bits of the quantizer, k the number of bits needed in the nominal situation when no interference is present, A_{max} the amplitude of the CW interference, G_{max} the maximum gain of the active antenna, L_{min} the minimum cable losses and $\sigma_{2,min}$ and $\sigma_{2,max}$ are the extreme values of the standard deviation of the noise at the input of the ADC.

Let P_{mask} be the power (on the mask) of a CW interference at the input of the function. It is recalled that $2(C_1)^2$ is the power of the corre-

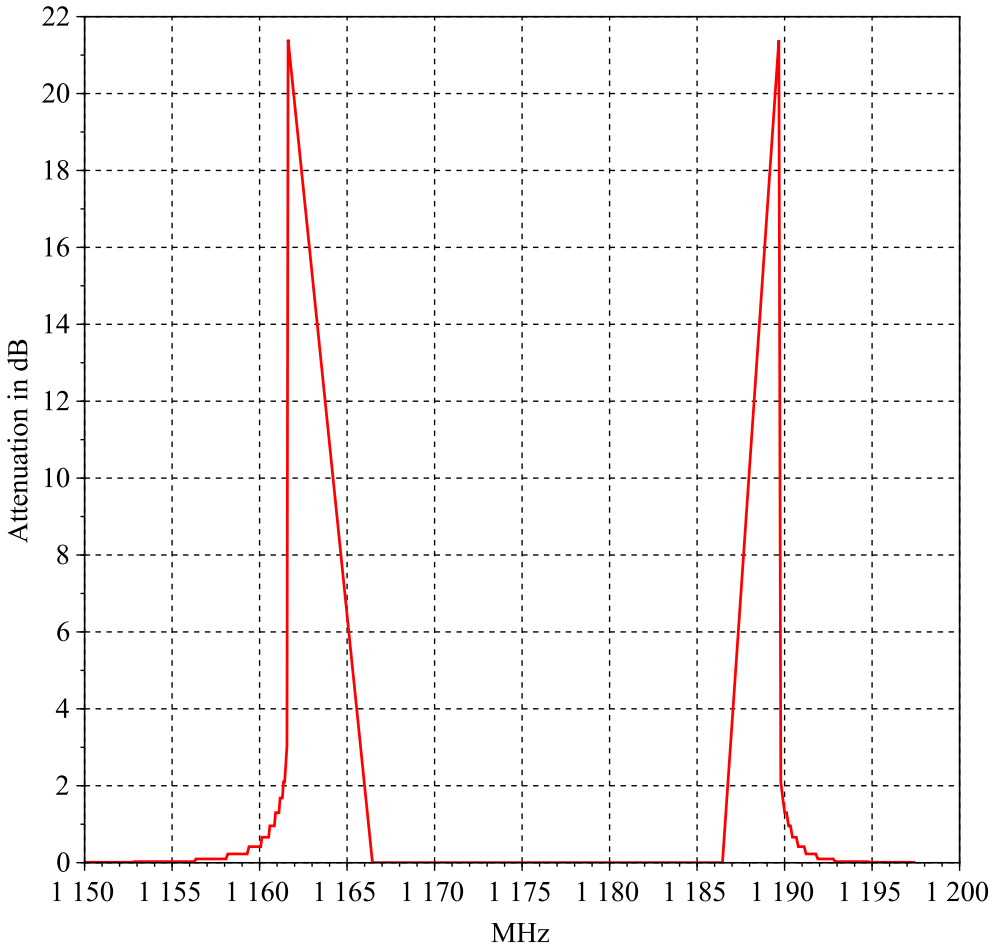


Figure 7.11: Attenuation provided by the linear-then-log function on the E5a CW interference mask.

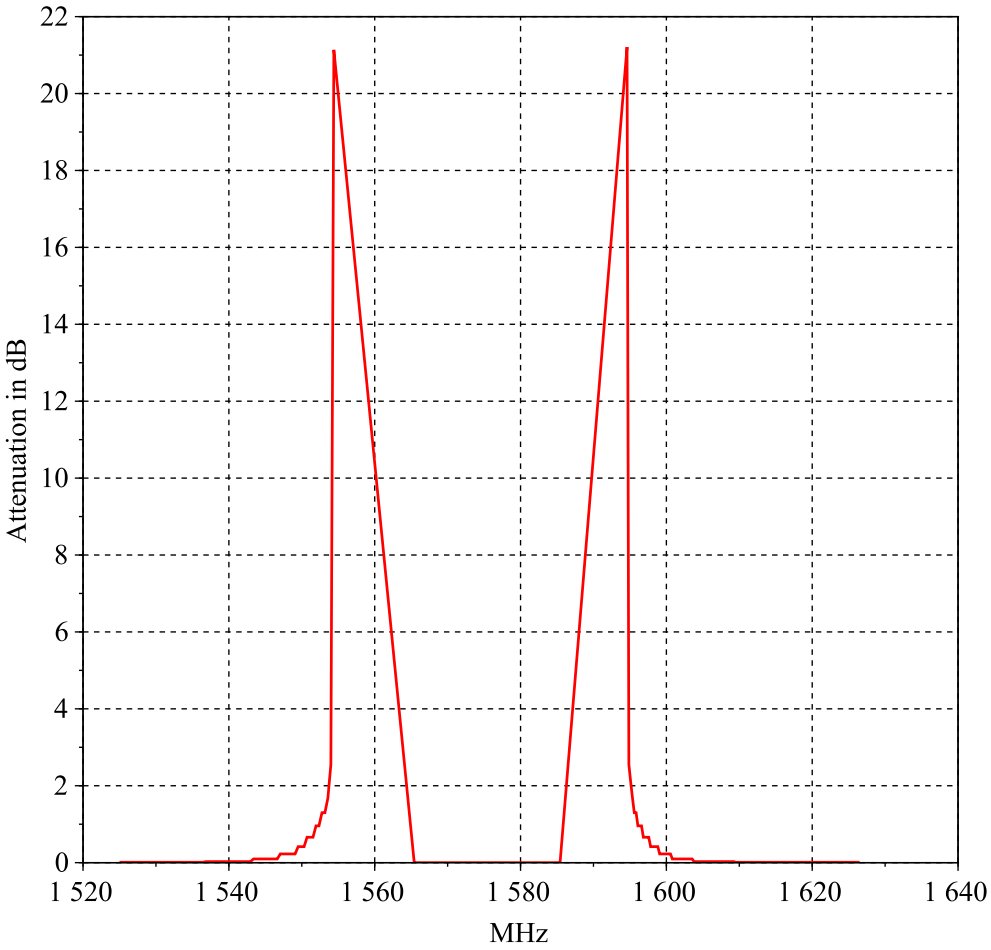


Figure 7.12: Attenuation provided by the linear-then-log function on the E1 CW interference mask.

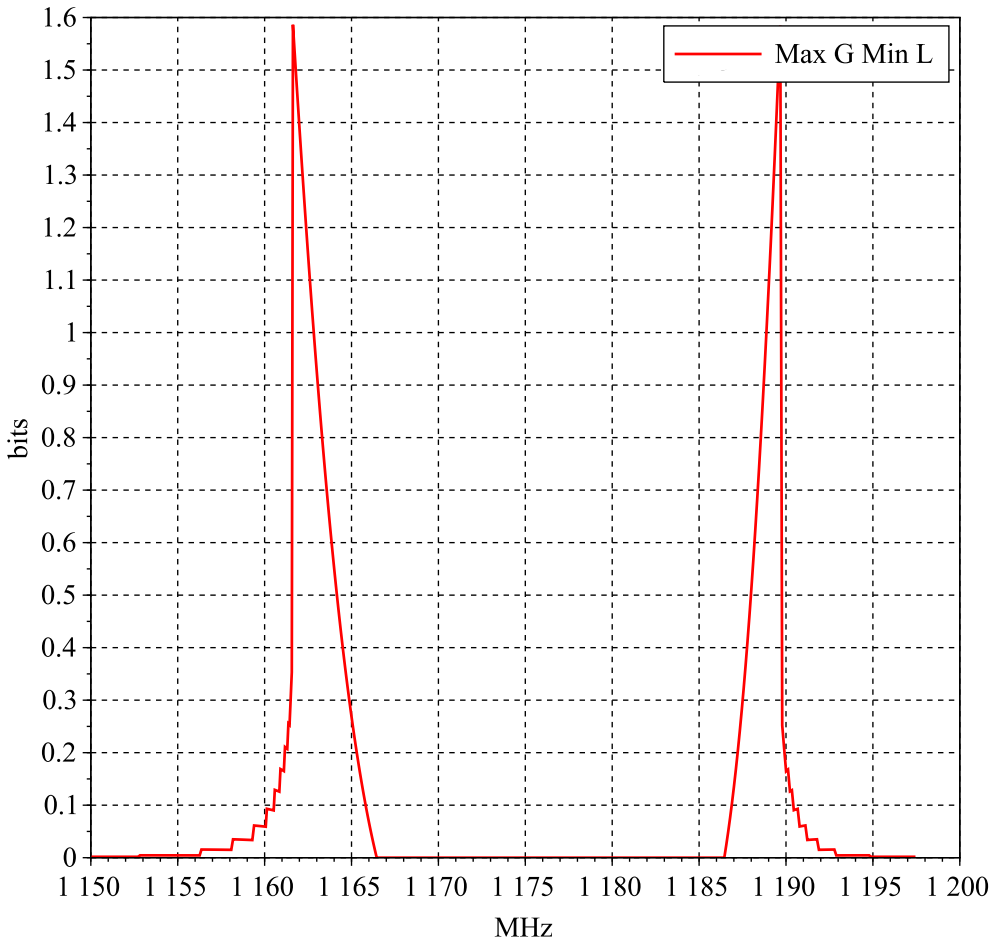


Figure 7.13: Quantization bit saving offered by the linear-then-log function on the E5a band.

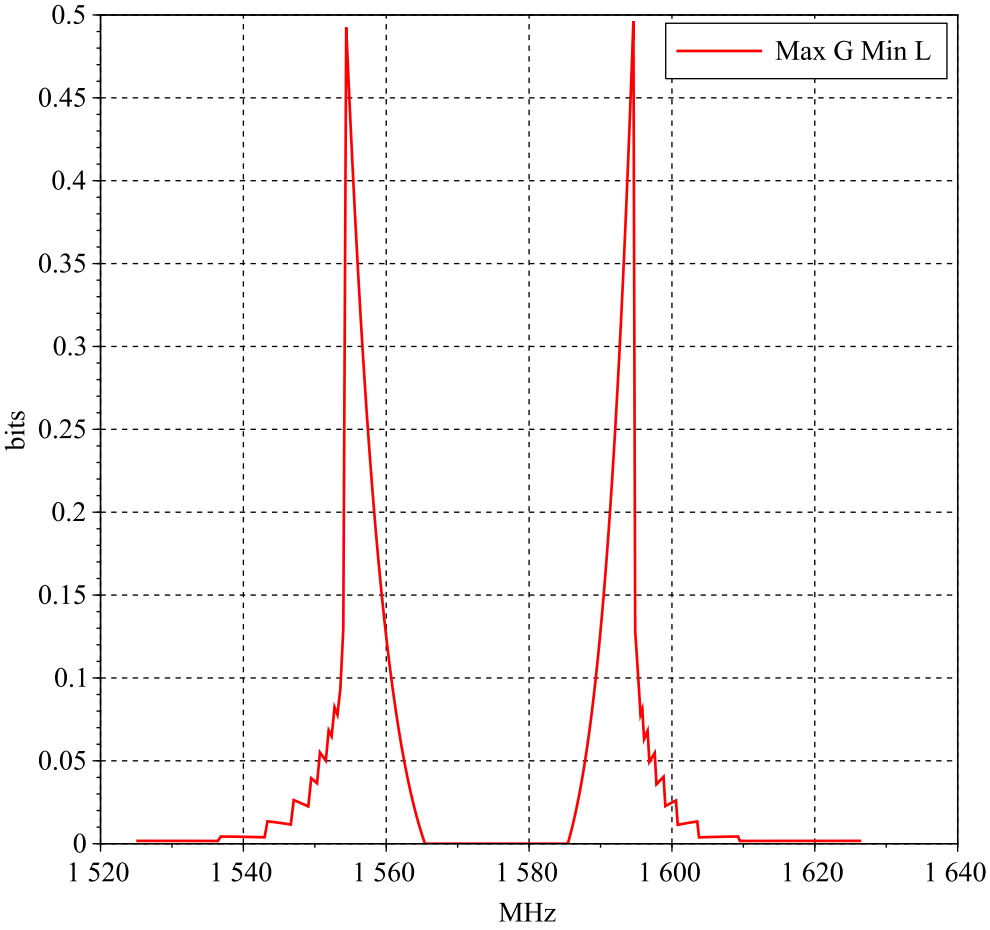


Figure 7.14: Quantization bit saving offered by the linear-then-log function on the E1 band.

sponding first harmonic at the output. Then the quantization bit saving is equal to the difference between the results of equation (6.28) calculated with $A_{max} = \sqrt{2P_{mask}}$ and with $A_{max} = \sqrt{4(C_1)^2}$. This difference is plotted in figures 7.13 and 7.14 for the E5a and E1 band, respectively.

Using the data from figures 7.13 and 7.14, and rounding down (floor), it can be concluded that a quantization bit saving up to 1 bit is possible on the E5a band and no saving can occur on the E1 band. These low results are due to the fact that on the frequency bands where it is possible to compress, the power of the CW is near the power of the noise, so the number of bits is set by the noise almost exclusively. With or without CW, this number changes little.

7.3.1.6 A Major Limitation

The first set of figures 7.9 and 7.10 also show that, in the full efficiency band, the CW interference mask is around or under the linear quantization limit which is set to $c \cdot \sigma_{2,max}$ as stated before: the CW level to compress is the same or smaller than the noise in which the useful signal is buried. This function F_{ll} is efficient (it compresses the interference threat without producing secondary harmonic waves higher then the floor of the mask) where it can not be used (at mask levels which correspond to the useful signal, which should not be compressed). That is why a second function was considered.

7.3.2 The Pure Log Function

7.3.2.1 Definition

The mathematical expression of this function is

$$y(x) = \left(\log_q(1 + |x| \cdot \ln(q))\right) \cdot \text{sign}(x) \tag{7.15}$$

This function, noted F_{pl}, is represented in figure 7.15. It is fully logarithmic, its slope at 0 is equal to 1 and it has a continuous second order derivative, by opposition to F_{ll} which has a discontinuous one at $X0$. This property should induce lower harmonics at the output. However, this is at the expense of linearity: the useful signal, even in the nominal situation, i.e. when there is no interference, will be compressed.

Figures 7.16 and 7.17 allow a graphical comparison between function F_{pl} and function F_{ll}. The better compression ratio of the linear-then-log function appears (for values of $x > 2.5$ in this case where $X0 = 1$), as at the same time the smoother variation of the pure log function is shown.

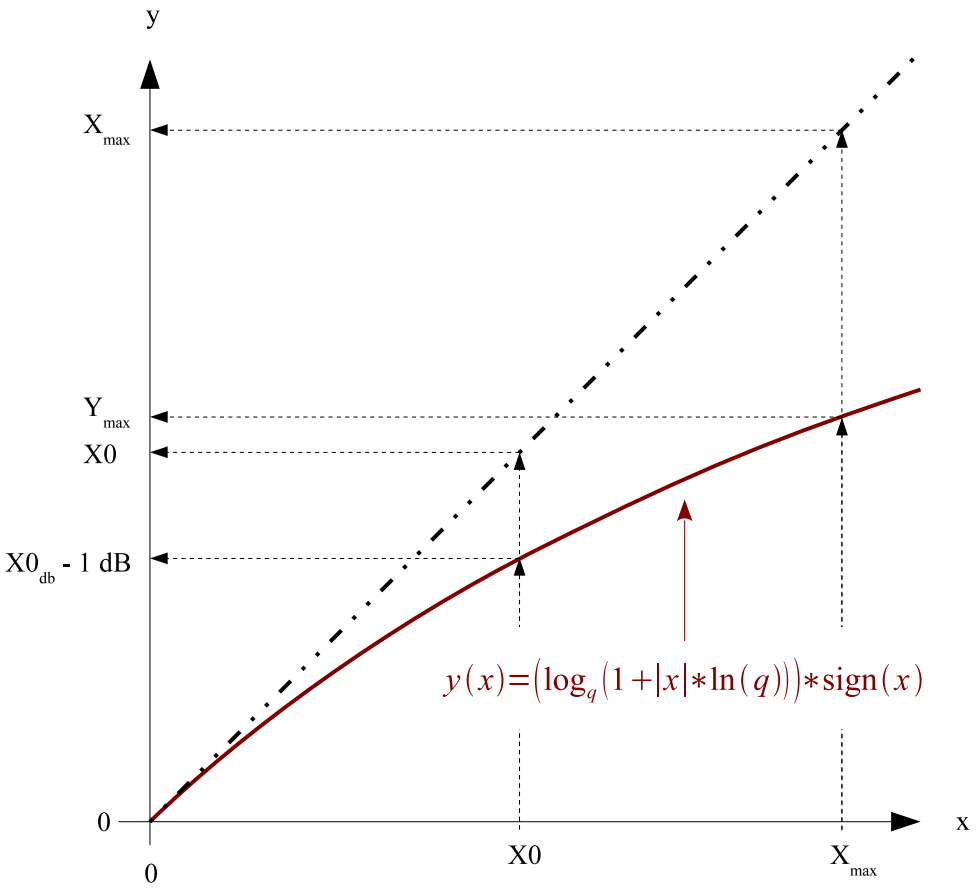


Figure 7.15: The pure log function.

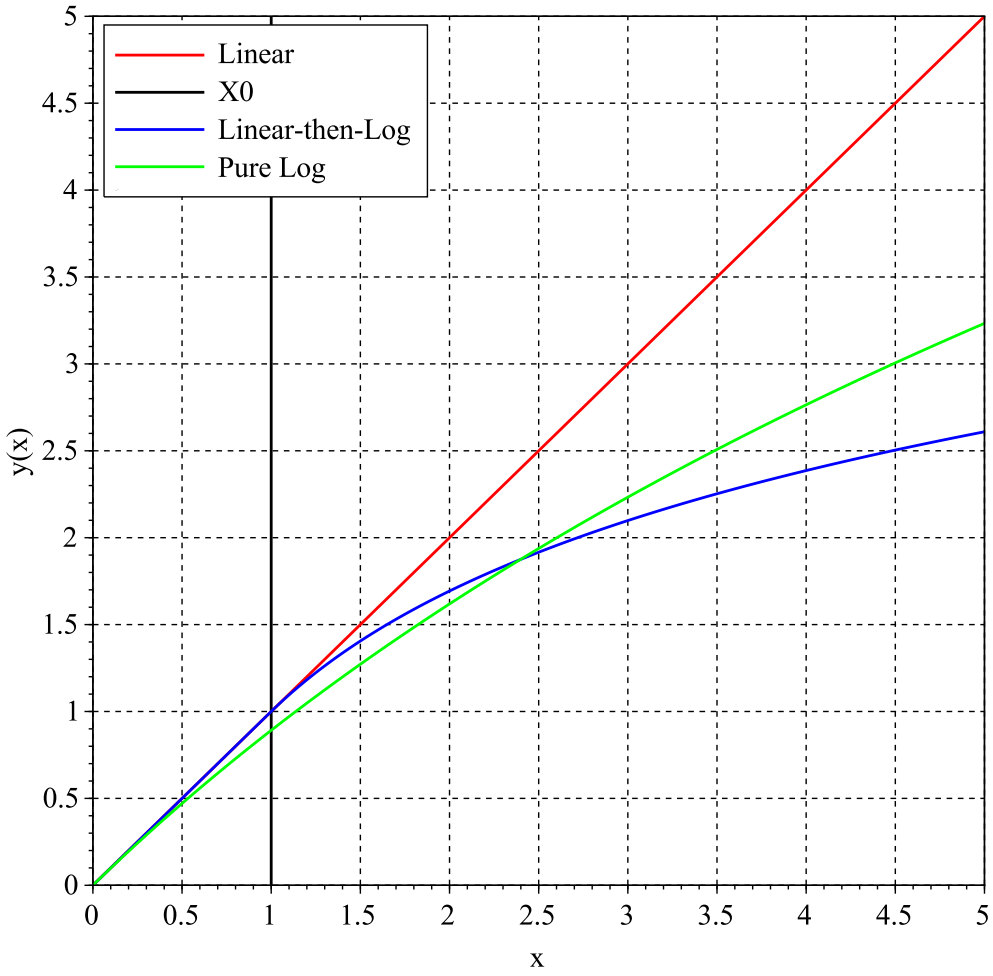


Figure 7.16: Comparison of the two non-linear functions.

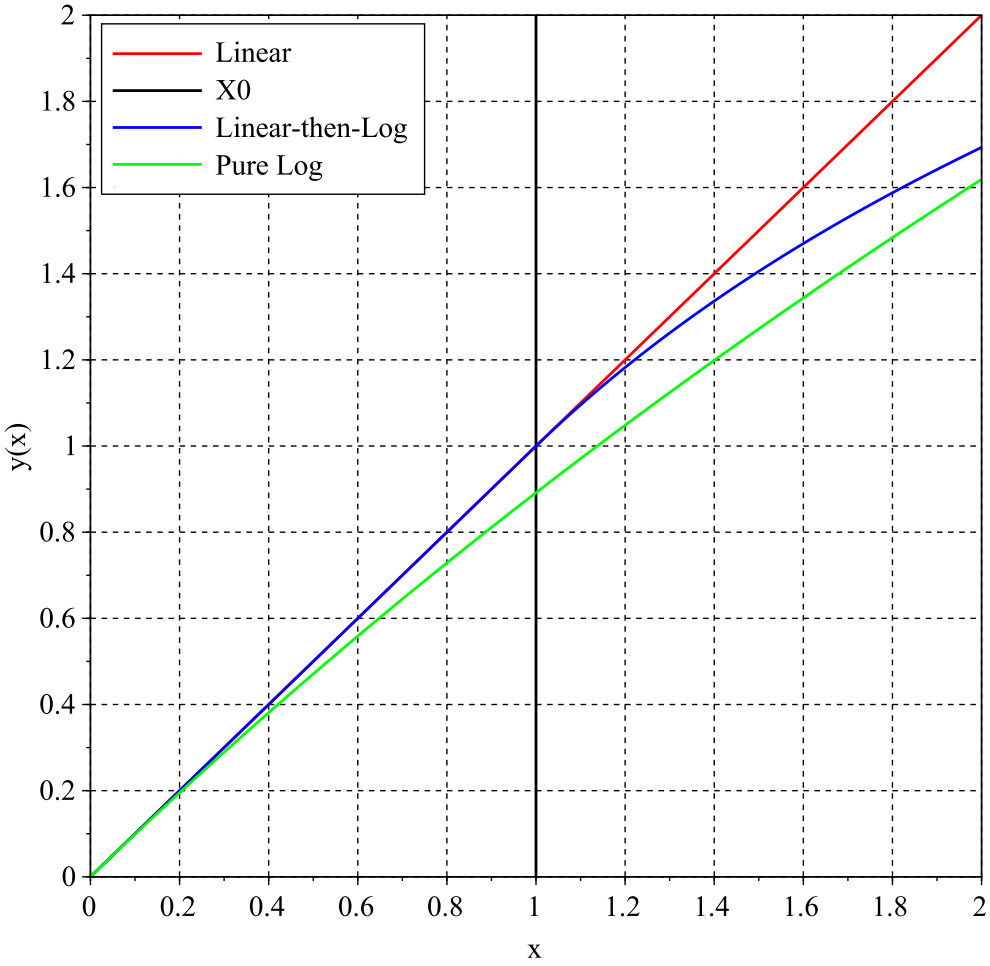


Figure 7.17: Comparison of the two non-linear functions, close-up.

7.3.2.2 Calculation of the Base of the Logarithm q

The corner value $X0$ has the same meaning for the pure log function as for the linear-then-log function, as defined in section 7.3.1.1. $X0$ is the amplitude limit under which the signal is not be compressed. However, the assumption is made that a tolerance margin of less than 1 dB is acceptable in the case of the pure log function. Then, it is possible to calculate the value of parameter q in equation 7.15, as a function of $X0$, as follows.

The corner value $X0$ is defined here as the 1 dB compression point

$$y\left(X0\right) = \log_q\left(1 + X0 \cdot \ln(q)\right) = X0 \cdot 10^{-1/20} \tag{7.16}$$

The logarithm can be expanded in this relation

$$\ln\left(1 + X0 \cdot \ln(q)\right) = \left(X0 \cdot \ln(q)\right) \cdot 10^{-1/20} \tag{7.17}$$

As $10^{-1/20} \simeq 0.89 \simeq 1$ the following approximation stands

$$\ln\left(1 + X0 \cdot \ln(q)\right) \simeq X0 \cdot \ln(q) \tag{7.18}$$

This is the first order Taylor expansion around 0 of $\ln(1 + x) \simeq x$. Extended to the second order it gives

$$\ln\left(1 + X0 \cdot \ln(q)\right) \simeq X0 \cdot \ln(q) - \frac{1}{2}\left(X0 \cdot \ln(q)\right)^2 \tag{7.19}$$

Replacing relation (7.19) in equation (7.16), it can be concluded that [6]

$$\ln(q) = 2/X0 \cdot \left(1 - 10^{-1/20}\right) \tag{7.20}$$

So, setting $X0$ completely define equation 7.15, through $\ln(q)$.

7.3.2.3 Performance Evaluation

The effect of F_{pl} on the CW interference masks was measured as previously for the F_{ll} function. The results are presented in figures 7.18, 7.20 and 7.22 for the E5a band and in figures 7.19, 7.21 and 7.23 for the E1 band, which will be elaborated on in the next section.

7.3.2.4 Full Efficiency Band

From the first set of figures 7.18 and 7.19 the full efficiency band of this pure log function can also be defined, which is equal to $[1161, 1190]$ MHz for E5a and to $[1552, 1596]$ MHz for E1. As expected these are slightly

6. This value is systematically refined by the bisection method.

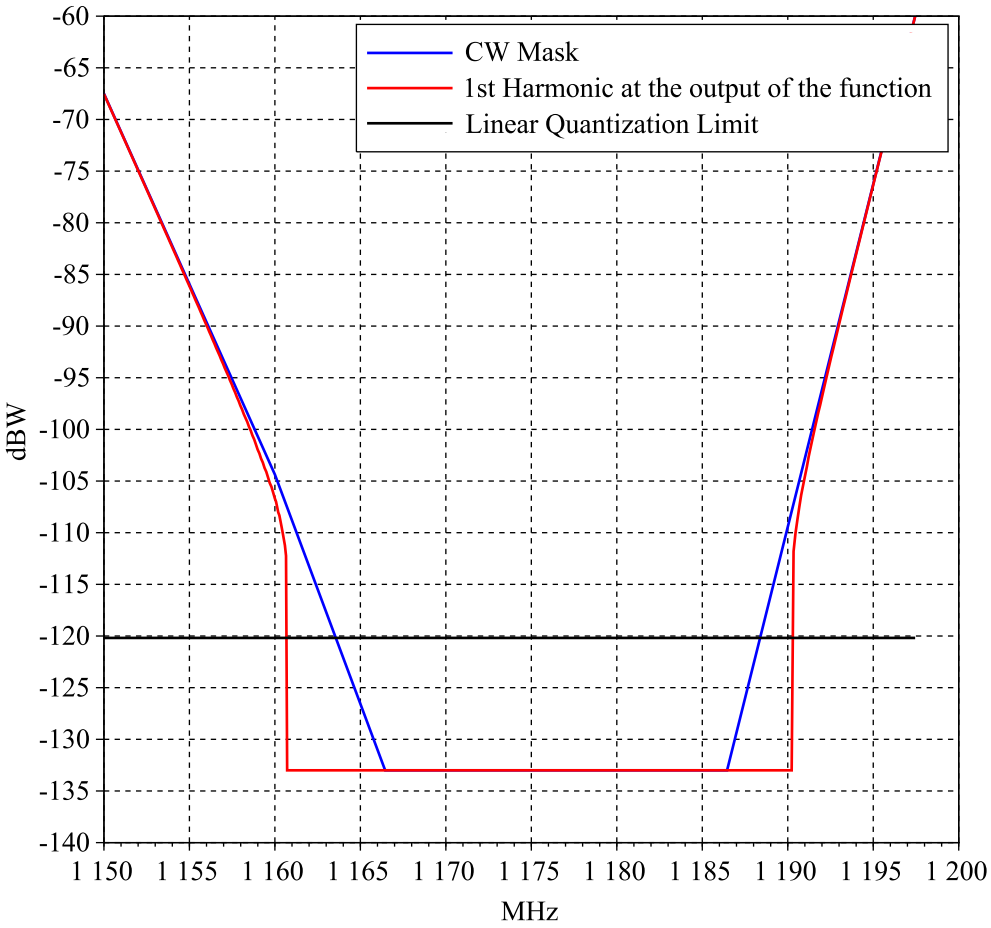


Figure 7.18: Compression effect of the pure log function on the E5a CW interference mask.

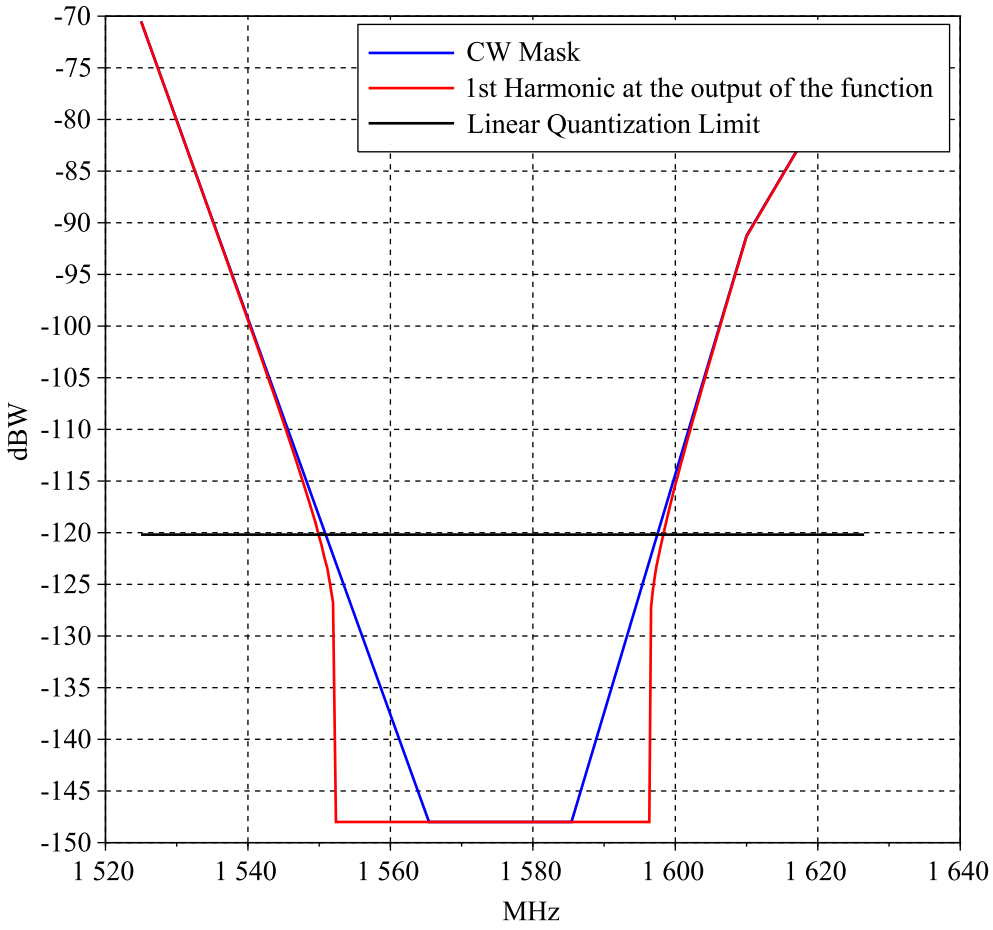


Figure 7.19: Compression effect of the pure log function on the E1 CW interference mask.

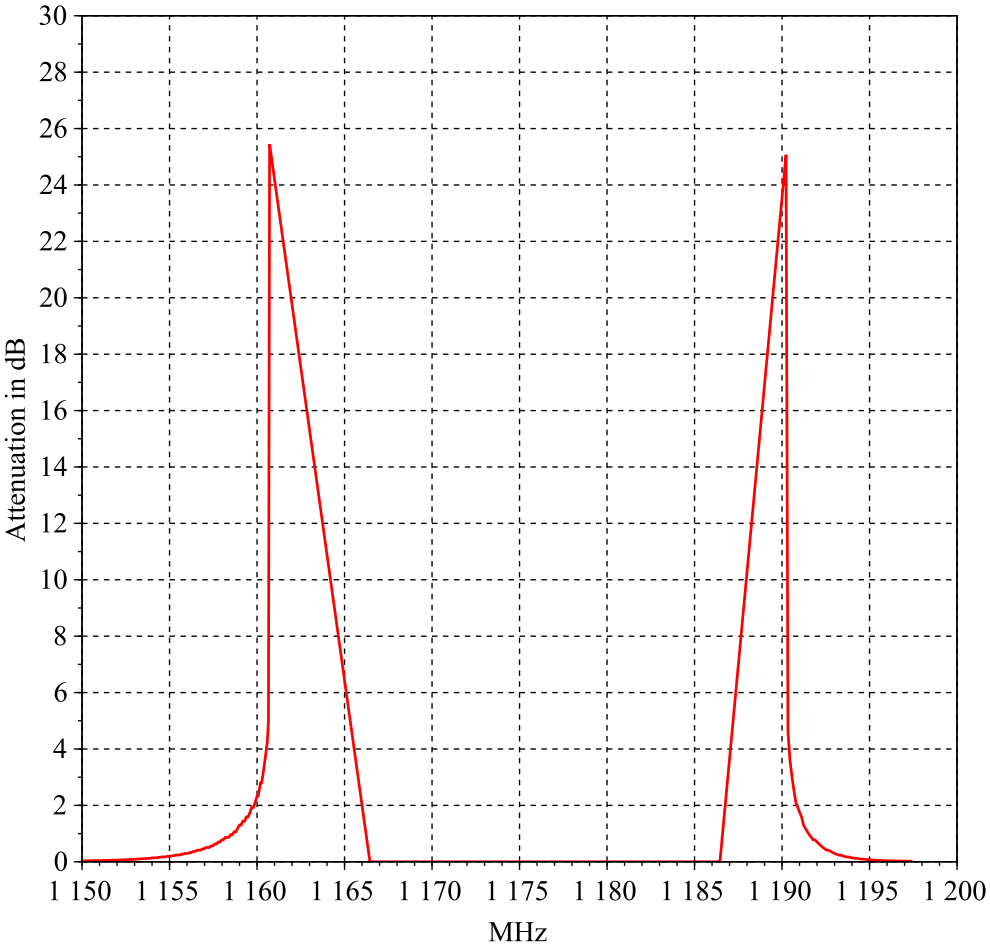


Figure 7.20: Attenuation provided by the pure log function on the E5a CW interference mask.

larger than for the linear-then-log function. This is an improvement, because it means that after the compression of the interference threat by the pure log function, the frequency band over which there is no more need of filtering (because the level of the first harmonic lies under the in-band mask) is larger.

The second set of figures 7.20 and 7.21 represent directly the attenuation provided by the function, Att_{pl}. The function F_{pl} provides up to $\sim 25\,\text{dB}$ of attenuation in both E5a and E1 bands. This is also slightly higher than for the linear-then-log function. Thus, the pure log function provides approximately 3 dB more attenuation than the linear-then-log function. This is better, as after the compression of the interference threat by this pure log function, the filtering operation needed to mitigate the remaining threat will require less selective filters.

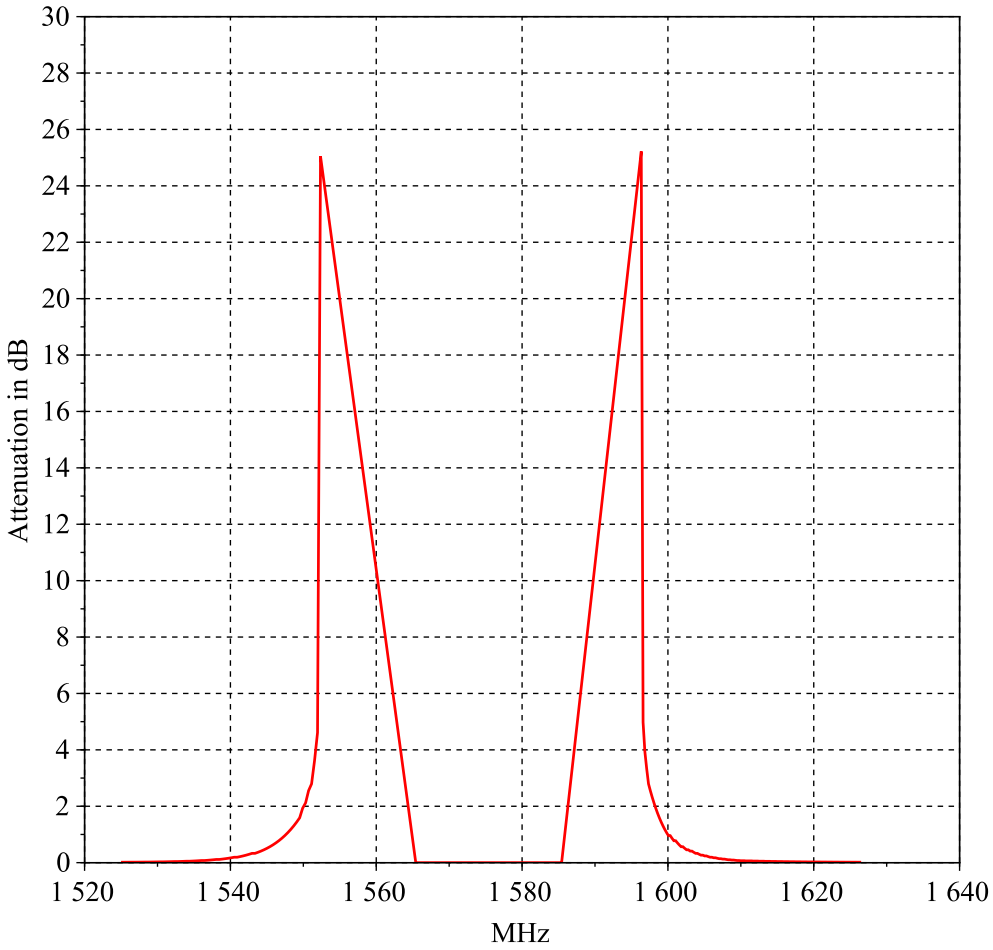


Figure 7.21: Attenuation provided by the pure log function on the E1 CW interference mask.

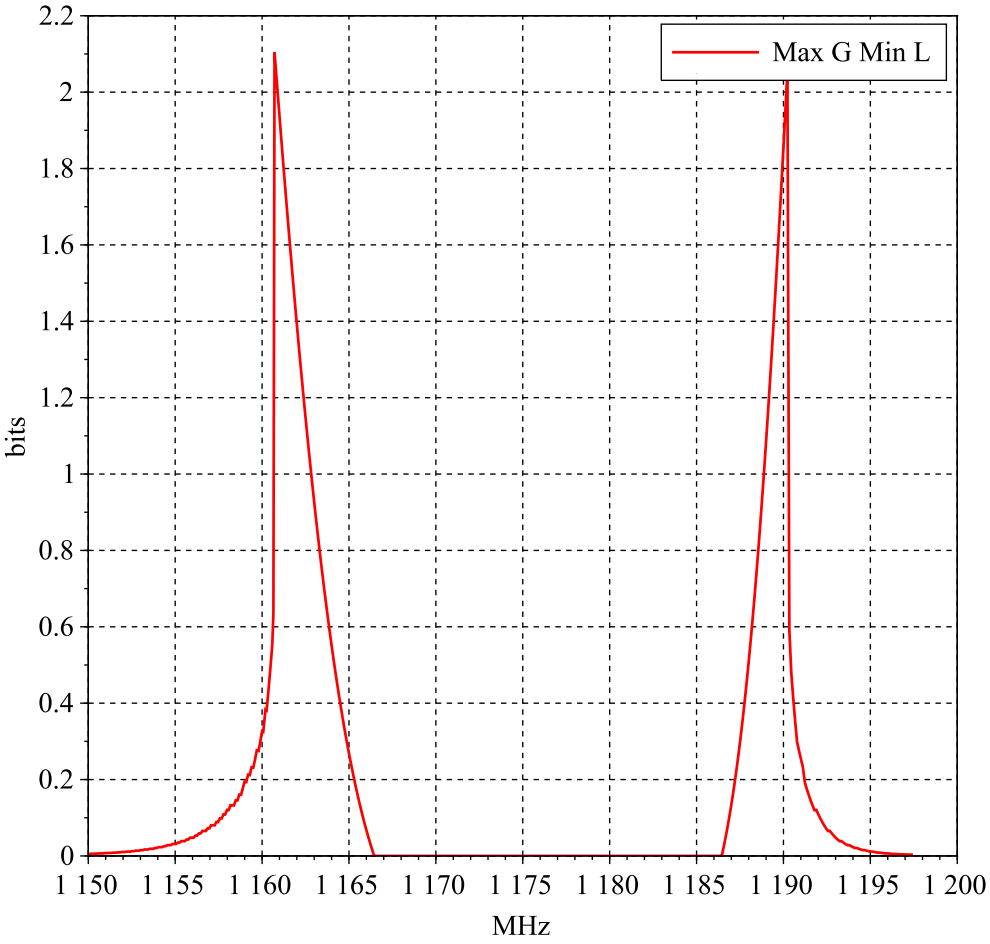


Figure 7.22: Quantization bit saving offered by the pure log function on the E5a band.

7.3.2.5 Quantization Bit Saving

The last set of figures 7.22 and 7.23 show the quantization bit saving offered by the dynamic compression function F_{pl}.

As a direct consequence of the higher attenuation provided by this pure log function, the quantization bit saving is also better than for the function F_{ll}, at least on the E5a band: a quantization bit saving up to 2 bits is possible on the E5a band and no saving can occur on the E1 band. The explanation for these low results is the same as for the function F_{ll}.

7.3.2.6 The Same Major Limitation

As in the case of the F_{ll} function, in the full efficiency band the CW interference mask is around or under the linear quantization limit: the CW level to compress to is the same or smaller than the noise in which

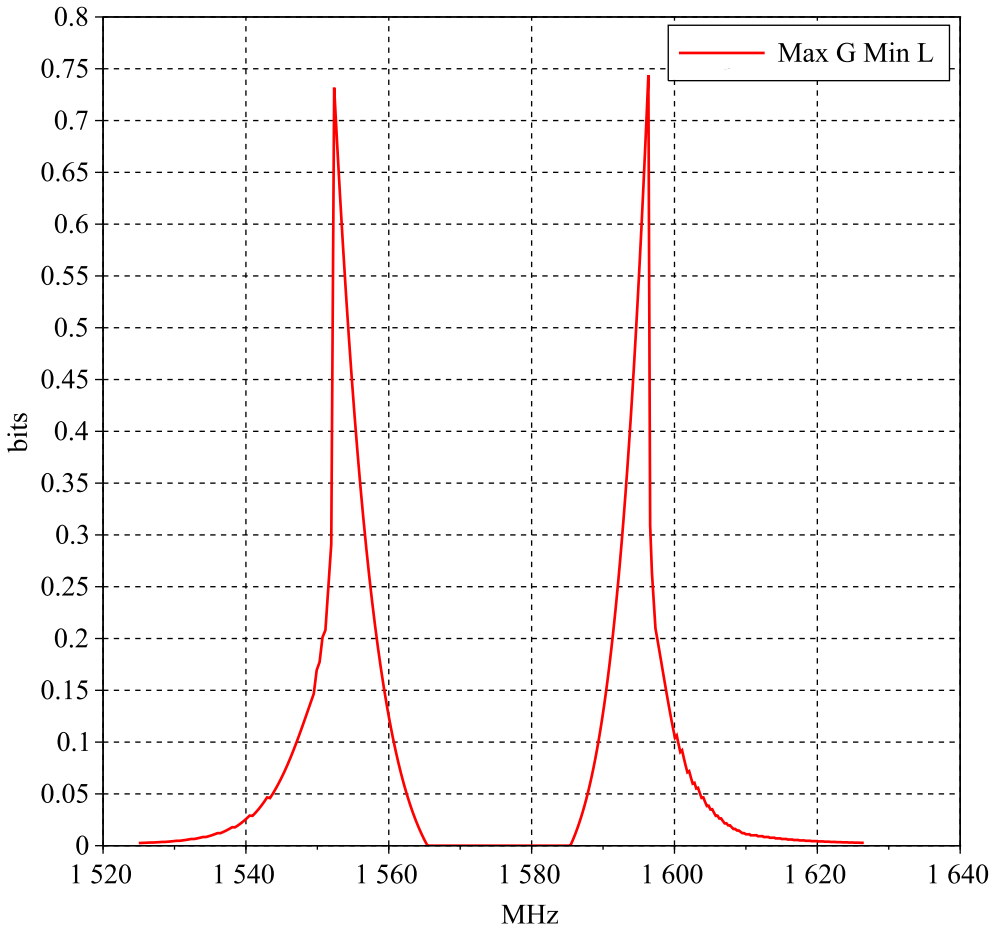


Figure 7.23: Quantization bit saving offered by the pure log function on the E1 band.

the useful signal is buried. The same conclusion reached in section 7.3.1.6 for the F_{ll} function can be drawn: F_{pl} is efficient where it can not be used. Indeed, it compresses the interference threat without producing secondary harmonic waves higher then the floor of the mask, but at mask levels which correspond to the useful signal, which should not be compressed.

7.4 Conclusion

The conclusion of this chapter is that, unless a function with better performance, that is a larger efficiency band, is produced, dynamic compression is not a decisive technique to decrease the binary throughput after the ADC(s). This makes extra RF analog filters with required performance all the more desirable. This fact was already established in chapter 3 about sampling and in chapter 6 about quantization, it is a confirmation once more.

7.5 References

[1] O. Herrmann, R. Rabiner, and D. S. K. Chan, "Practical design rules for optimum finite impulse response low-pass digital filters," *The Bell System TECHNICAL JOURNAL*, vol. 52, no. 6, pp. 769–799, July-August 1973, last accessed 11/06/2014. [Online]. Available: http://www3.alcatel-lucent.com/bstj/vol52-1973/articles/bstj52-6-769.pdf

[2] Analog Devices, "Analog Devices TigerSHARC ADSP-TS201S Data Sheet," December 2006, last accessed 11/06/2014. [Online]. Available: http://www.analog.com/en/processors-dsp/tigersharc/adsp-ts201s/products/product.html

[3] R. G. Lyons. (2011, March) A simple way to add AGC to your communications receiver design. www.embedded.com. Last accessed 09/29/2014. [Online]. Available: http://www.embedded.com/print/4214571

[4] R. Thompson, E. Cetin, and A. G. Dempster, "Use of AGC in Mitigation of Continuous-Wave Interference in GNSS," in *Proceedings of the 2011 Defense Applications of Signal Processing Workshop, DASP 2011*, Sunshine Coast, July 2011.

Extraction of the Useful Bands after Coherent Sampling

8

This last part of the thesis is dedicated to the digital separation of the two bands, E5a and E1, which are sampled at the same time in the Coherent Sampling architecture.

In fact, when a single ADC is used, the flow of the samples at its output must be digitally filtered to isolate the spectrum of each signal, so that they can be demodulated independently.

If necessary, depending on the selectivity of the extra RF analog filters required in front of the ADC, this filtering operation should also complete the attenuation of the interference threat.

8.1 Situation at the Input of the Single ADC

The situation to consider at the input of the ADC in the structure represented in figure 3.1 can be ideal as in figure 3.4 or as bad as the one at the receiver input, represented in figure 6.10, depending on the selectivity of the extra RF analog filters located in front of the ADC. It is decided to study here the worst case to bound the complexity of the filters needed to select on one hand the E5a band and on the other hand the E1 band.

Taking the mask of figure 6.10 at the input of the receiver, and sampling (in the worst case, with a sample frequency of 322.710 MSamples/s for maximum transition filter bandwidth of $B_s = 28$ MHz), the CW mask requirement at the output of the ADC is shown in figure 8.1. It is necessary to recall here that, in the Coherent Sampling architecture, for extra RF filters with a transition bandwidth larger than 28 MHz, there

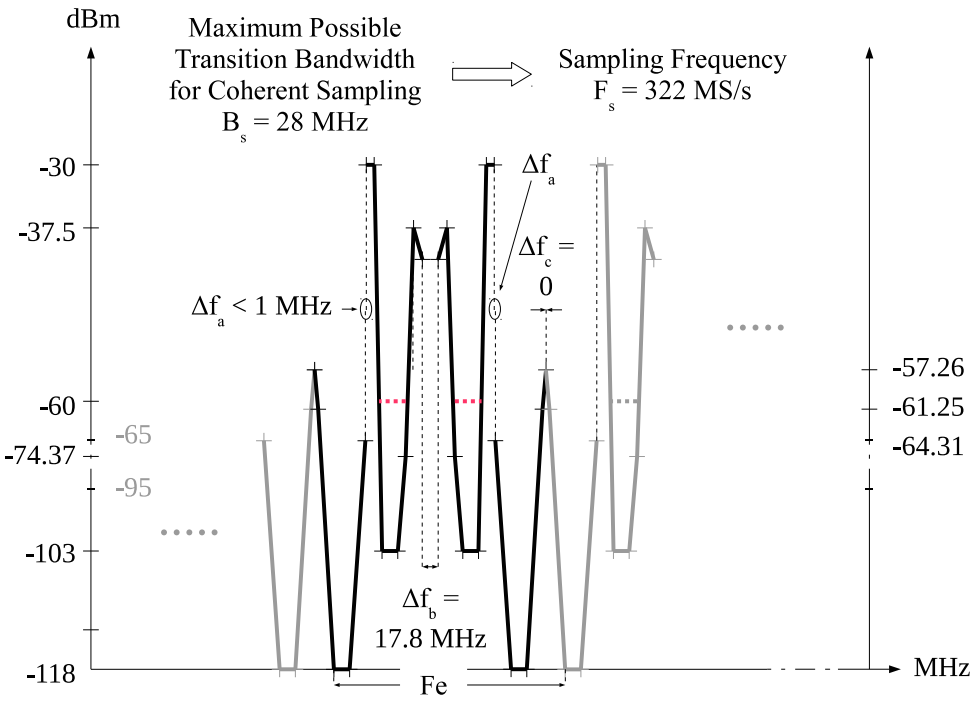


Figure 8.1: Worst sampled CW interference mask at the output of the ADC in Coherent Sampling.

is no sampling frequency which permits the sampling of both E5a and E1 bands without aliasing of the interference threat in the useful bands.

Figure 8.1 presents one period of the spectrum of the sampled signal, in black, along with one other period on each side, in gray. As explained in section 7.1.2 of chapter 7, the Fourier transform of a sampled signal being periodic in F_s (the sampling frequency), it is equivalent to consider any period. That is why there is no absolute location in frequency in figure 8.1, because it is believed it would have little meaning. Δf_a, Δf_b and Δf_c are the values of the spacing between the different aliases of the E5a and E1 bands. They are required to calculate the slope of the attenuation needed to separate each band from the other ones.

The useful band of E5a appears to be the most difficult to extract, from its immediate surrounding, due to the high slope of its interference mask, especially at the right of the useful band: 73 dB over the range $[1186.45, 1197.45]$ MHz $\simeq$ 10 MHz, as shown in figure 6.10. This represents the worst case spectrum that will have to be digitally filtered to

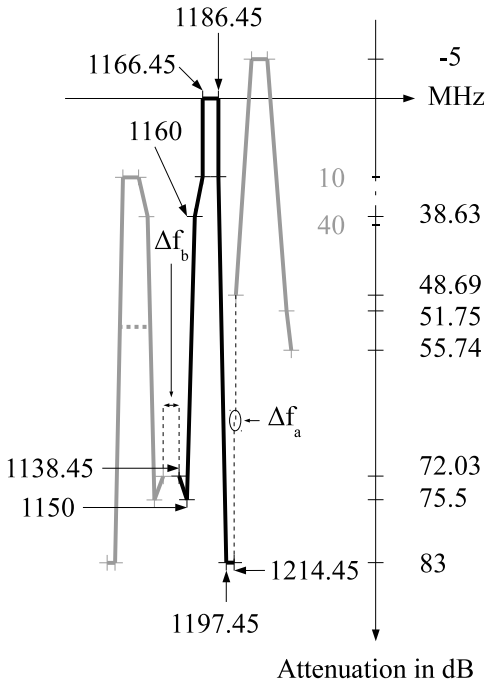


Figure 8.2: Minimum attenuation to be provided at the output of the ADC on E5a, Coherent Sampling.

separate the E5a and E1 signals [1].

8.2 Selectivity of the Digital Separation Filters

The minimum selectivity of the digital filters after the ADC mentioned in the previous section is drawn in black in figure 8.2 for the E5a band and in figure 8.3 for the E1 band.

The design objective was to allow the greatest decimation [2] rate after the filtering operation, in order to decrease the sample rate at the input of the demodulation process as much as possible. It means that, for each band, after the filter it must be possible to alias the band to itself as near as possible without suffering from an out-of-band threat reinjected in-band. These digital filter transfer functions in figure 8.2 and 8.3 were then calculated so that any out-of-band level is attenuated by at least

1. The order of the bands and the distance between them is a by-product of the calculations conducted in appendix A.

2. Decimation, from the spectral point of view, is equivalent to bringing closer the already periodized spectrum. If done without prior band limitation, this can lead to spectral aliasing.

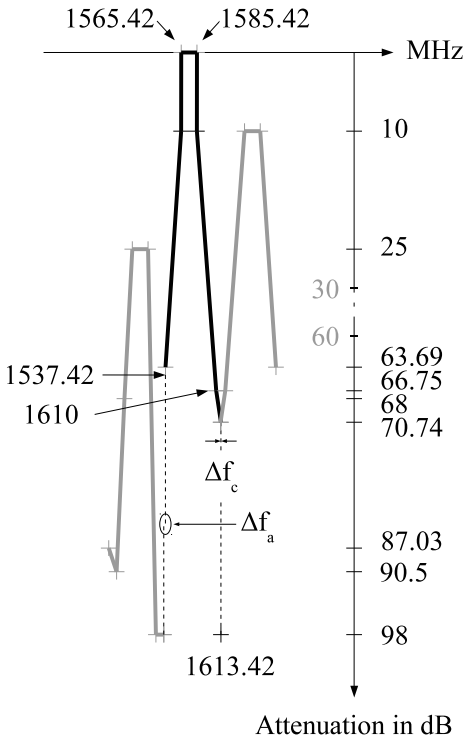


Figure 8.3: Minimum attenuation to be provided at the output of the ADC on E1, Coherent Sampling.

10 dB compared to the minimum in-band mask (−103 dBm in the E5a band and −118 dBm in the E1 band). The traces in gray represent the minimum attenuation which would be required to lower the adjacent bands (in figure 8.1) by at least 10 dB compared to the minimum in-band mask. It appears clearly that this attenuation is always easier to achieve than the one plotted in black, hence its gray color to show it is not significant.

8.3 Calculation Workload Evaluation

If FIR filters are to be used, their order can be estimated using the following formula, from [1]

$$\hat{M} = \frac{-20\log_{10}\left(\sqrt{\delta_p\delta_s}\right) - 13}{14.6\Delta f} + 1 \tag{8.1}$$

The parameters are the same as in section 7.1 of chapter 7:

- f_p the normalized passband edge frequency,
- f_s the normalized stopband edge frequency,
- $\Delta f = (f_s - f_p)$ the normalized transition bandwidth,
- δ_p the passband ripple,
- δ_s the stopband ripple.

This relation, as equation (7.1) from [2], is defined for a lowpass filter. Thus, f_p and f_s are not the passband frequencies in our case, but their lowpass equivalents. The order $\hat{M}$ is the same for the corresponding bandpass filter as shown in section 7.1 of chapter 7. The previous equation (7.1) was not used here as it is not valid when the ratio $\delta_p/\Delta f$ is less than 0.004 which is the case here. When applicable the formula from [2] is more accurate but equation (8.1) gives results of the same order.

As presented in section 7.1 of chapter 7, $f_p = 10\,\text{MHz}/F_s$, that is half of the useful bandwidth B_1 or B_{5a} and $10\log_{10}(\delta_p) = -10$ dB. Regarding the values for f_s and δ_s, they are from figure 8.2 for the E5a band

- $f_s = \left(1197.45 \times 10^6 - f_5 - B_{5a}/2\right)/F_s$,
- $\delta_s = 83$ dB,

and from figure 8.3 for the E1 band

- $f_s = \left(f_1 - B_1/2 - 1537.42 \times 10^6\right)/F_s$,

- $\delta_s = 63.69\,\text{dB}$,

with $F_s = 322.710\,\text{MS/s}$.

For the E5a band equation (8.1) gives $\hat{M} = 1769$, which is very large, and $\hat{M} = 117$ for the E1 band. The calculation workload can also be estimated here by the simple product of the order $\hat{M}$ and of the sampling frequency. It can reach 571 GMAC/s for the E5a band.

8.4 Feasibility of the Filters and Conclusion

This calculated workload of 571 GMAC/s should be compared to the performance of the nowadays processors to assess the feasibility of the Coherent Sampling solution with the less selective analog filters. For example, at the time of this writing, the most powerful FPGA from Xilinx, the Virtex-7 XC7V2000T [3], which can process up to 5335 GMAC/s, seems to offer a sufficient processing power. However, as in section 7.1 of chapter 7, it should be pointed out that this filtering process is only the first of a long series of signal processing and this power ratio of $5335/571 \simeq 10$ may not be as large as it seems. Coherent Sampling seems possible nevertheless from its beginning, the simultaneous sampling of the E5a and E1 bands, to its end, the digital separation of the two bands before their individual navigation processing.

8.5 References

[1] J. Kaiser, "Nonrecursive Digital Filter Design Using the IO-Sinh Window Function," in *IEEE International Symposium on Circuits and Systems*, 1974, pp. 20–23.

[2] O. Herrmann, R. Rabiner, and D. S. K. Chan, "Practical design rules for optimum finite impulse response low-pass digital filters," *The Bell System TECHNICAL JOURNAL*, vol. 52, no. 6, pp. 769–799, July-August 1973, last accessed 11/06/2014. [Online]. Available: http://www3.alcatel-lucent.com/bstj/vol52-1973/articles/bstj52-6-769.pdf

[3] Xilinx, "7 Series FPGAs Overview," July 2013, last accessed 11/06/2014. [Online]. Available: http://www.xilinx.com/support/documentation/data_sheets/ds180_7Series_Overview.pdf

9 Conclusions and Future Work

In the light of the results presented all along this document, this last chapter establishes some conclusions to the thesis and then proposes complementary work to be conducted in order to complete or improve the different contributions.

9.1 Conclusions

The purpose of this thesis was to assess the feasibility of a DS-DF-SDR Galileo receiver for Civil Aviation. From the ideal structure of a RF-DS-SDR GNSS receiver, an active antenna, an ADC and a processor, a design was proposed from the antenna to the processor. The main challenges were not only identified but also studied in depth, and solutions or at least dimensioning bounds were proposed.

In this way two architectures have been considered in a first step to develop the structure of the receiver. In the Coherent Sampling architecture both E5a and E1 bands are digitized simultaneously with a single ADC, while in the Separate Sampling architecture each band is digitized separately with a dedicated ADC. In both cases it was shown that supplementary RF filters were needed before sampling to meet the Civil Aviation requirements regarding robustness to interference. The attenuation to be provided by these filters was produced for the two architectures. Then, as a function of the possible difference between the defined attenuation and the performance of real filters, the minimum sampling frequency F_s was calculated for each architecture. A minimum of $F_s = 88.08\,\text{MS/s}$ was found for the Coherent Sampling receiver, for extra RF filters meeting their specifications. Regarding the Separate Sampling architecture, it has been determined a minimum of $F_s = 40.22\,\text{MS/s}$ for the E5a band

and $F_s = 40.14\,\mathrm{MS/s}$ for the E1 band, for extra RF filters meeting their specifications also.

As it appeared that the required extra RF filters could be hard to synthesize, due to their sharp attenuation profile, a feasibility test was performed on the E1 band, based on a mock-up PCB built around a SAW filter available off-the-shelf and available from the general public. Encouraging results were obtained on the possibility to reach the targeted attenuation and to contain the group delay variations in acceptable limits, even if the stability in temperature was not yet completely satisfactory.

Then the problem of the sampling clock jitter was addressed through simulations, since the frequency of the signal to be sampled was so high in comparison to classical architectures that it could not be neglected. To this purpose, a model of the sampling clock jitter was built, as a function of the constant c, the parameter which characterizes the quality of the sampling clock. To implement the model and to assess the effect of the sampling clock jitter, two programs were also written, a L1 C/A signal generator along with a companion receiver. Focusing on the analysis of the impact of this sampling clock jitter on the phase measurement, a bound value was set to the value of c to maintain the effect of the sampling clock jitter to an acceptable level. This acceptable level was defined to be 10 dB down from the thermal noise power, for $C/N0_{ref} = 43\,\mathrm{dBHz}$. The limit value of c was found equal to $10^{-20}\,\mathrm{s}$, in the range of readily existing clock chips available in the market.

The sizing of the quantization step was then studied and N, the minimum number of bits the ADC should provide, was calculated considering no AGC. This was done not only based on the useful signal, but also taking into account the level of the interference threat after the extra RF filters. The required number of bits can reach high values that might not be on the market for the moment (depending on the real performance of the extra RF filters), putting emphasis on the critical role of the RF filters in the overall receiver dimensioning. Considering Separate Sampling, up to 20 bits could be required for the E5a band and up to 18 bits for the E1 band, in the case of poor quality extra RF filters. For Coherent Sampling, the results are similar, up to 20 bits could be necessary if the extra RF filters are far from meeting their specifications.

In view of the high binary throughput at the output of the ADC, revealed by the calculation of the minimum sampling frequencies together with the calculation of the required number of quantization bits, it was then investigated to compress the dynamic of the digital signal at the output of the ADC by means of non-linear mapping functions. However, under the strict requirement to not worsen the in-band interference

threat, no positive results were found.

The last task considered the separation of the E5a and E1 bands after the ADC and specific to the Coherent Sampling architecture. The minimum attenuation to be provided by the digital filters, as a function of the actual performance of the real RF filters, was established. An evaluation of the computational cost of this filtering process was done, reaching 571 GMAC/s in the worst case. This result was compared to the performance of a signal processor chip [1] available at the time of this writing, 5335 GMAC/s. It was estimated that the available processing power ratio, $5335/571 \simeq 10$, was sufficient, but not necessarily comfortable when taking into account the downstream processing tasks.

As a general technical conclusion to the results recalled herebefore one by one, a DS-DF-SDR Galileo receiver, intended for Civil Aviation, should be feasible. The greatest challenging point being the design and implementation of the extra RF filters as they clearly condition the downstream signal processing complexity.

However, even if feasible, it may be questioned if this kind of receiver will be built in the near future. The well-established position of the proven and secure classical architectures on this small market, in which novelty must be demonstrated compliant, at great expense, to very strict operational and safety requirements, suggests it is not going to happen tomorrow.

When the time comes, it is to be hoped, nevertheless, that the work done during this thesis will help not only the designer, but also the airworthiness authority who will have to certify this kind of equipment.

9.2 Future Work

This work did not aim at being exhaustive, only to open the way. Thus some complementary work should be conducted to complete our knowledge about the Direct Sampling technique applied to GNSS receiver.

A first effort would be to completely characterize the effect of the sampling clock jitter not only on the tracking performance, but also on the general position and navigation solution. This would specify the grade of the clock a receiver needs, greatly helping the designer in its choice.

Another point would be to conceive industrial grade extra RF filters which meet, as much as possible, the specified attenuations, and which hold them over the required temperature range. This done, the complexity of the digital signal processing tasks would be much more defined and the selection of the corresponding processor made easier.

1. The Xilinx Virtex-7 XC7V2000T FPGA.

As a completion result, a first full prototype could then be realized, with the demanding real-time implementation of the digital filtering process.

Appendices

Calculation of the Bandpass Sampling Frequency Intervals

A

This appendix details the methods used to establish the intervals of bandpass sampling frequencies which permit the sampling of the E5a and E1 bands, either coherently or separately. It is based on [1].

$x(t) \multimap\!\circ X(f)$ denotes the time continuous signal to be sampled and $x[n]$, $n \in \mathbb{Z}$ its periodically sampled version, with T_s the sampling period and $F_s = 1/T_s$ the sampling frequency.

The expression of the spectrum $X_s(f) \circ\!\!\sim x[n]$ is in [2]:

$$X_s(f) = \frac{1}{T_s} \sum_{n=-\infty}^{+\infty} X(f - nT_s) \tag{A.1}$$

The spectrum of the sampled signal is made of periodic copies of the spectrum of the continuous signal.

Claude E. Shannon has stated in [3], no information is lost during the sampling operation if there is no overlapping between replicas of $X(f)$. This determines the choice of F_s.

A.1 Separate Sampling

The modulus of the spectrum $|X(f)|$ of the E5a or E1 band is illustrated in figure A.1. Figure A.2 proposes an illustration of the conditions under which the replication of the positive part $|X_+(f)|$ of $|X(f)|$ does not overlap the negative part $|X_-(f)|$. These two conditions can be summarized in:

$$\frac{2f_{max}}{k+1} \leq F_s \leq \frac{2f_{min}}{k}, k \in \mathbb{N}^* \tag{A.2}$$

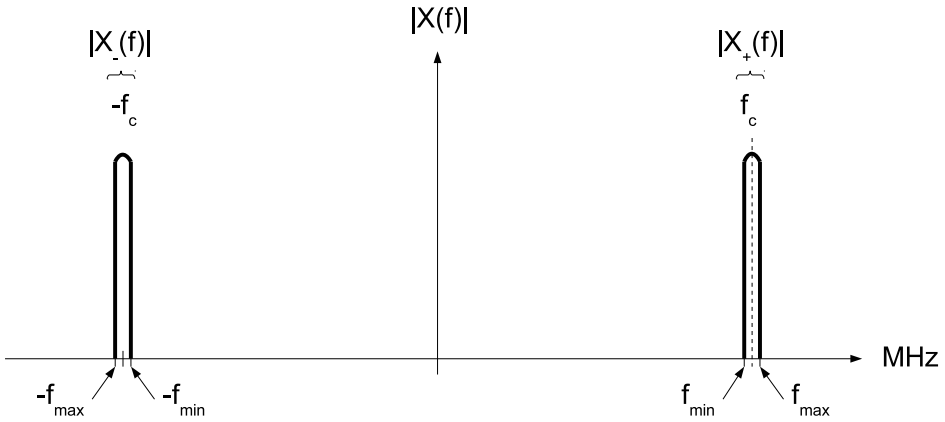


Figure A.1: Modulus of the E5a or E1 spectrum to be sampled.

This implies

$$\frac{2f_{max}}{k+1} \leq \frac{2f_{min}}{k} \tag{A.3}$$

Then, finally

$$0 \leq k \leq \frac{f_{min}}{B} \quad \text{with } B = (f_{max} - f_{min}) \tag{A.4}$$

As the final spectrum is periodic, if the conditions expressed in A.2 are satisfied, indeed no replica of the $|X_+(f)|$ band overlaps any replica of the $|X_-(f)|$ band. Thus, knowing the set of k which verify A.4 it is possible to calculate all the intervals of valid sampling frequency F_s from A.2.

A.2 Coherent Sampling

The modulus of the spectrum $|X(f)|$ obtained by the association of the E5a and E1 bands is illustrated in figure A.3. Figure A.4 proposes an illustration of the conditions under which the replicas of the $E1^+$ band do not overlap the three other ones.

As the final spectrum is periodic, if these conditions are satisfied, they also imply that no replica of the $E1^+$ band overlaps any replica of the three other bands. In turn it is not necessary to verify that any replica of the $E5a^+$, $E5a^-$ or $E1^-$ bands do not overlap any replica of the $E1^+$ band. What is more, as $x[n] \in \mathbb{R}$, $|X_s(f)|$ is even so that it is not necessary to verify that the replicas of the $E1^-$ band do not overlap any $E5a^+$ or $E5a^-$ band replica.

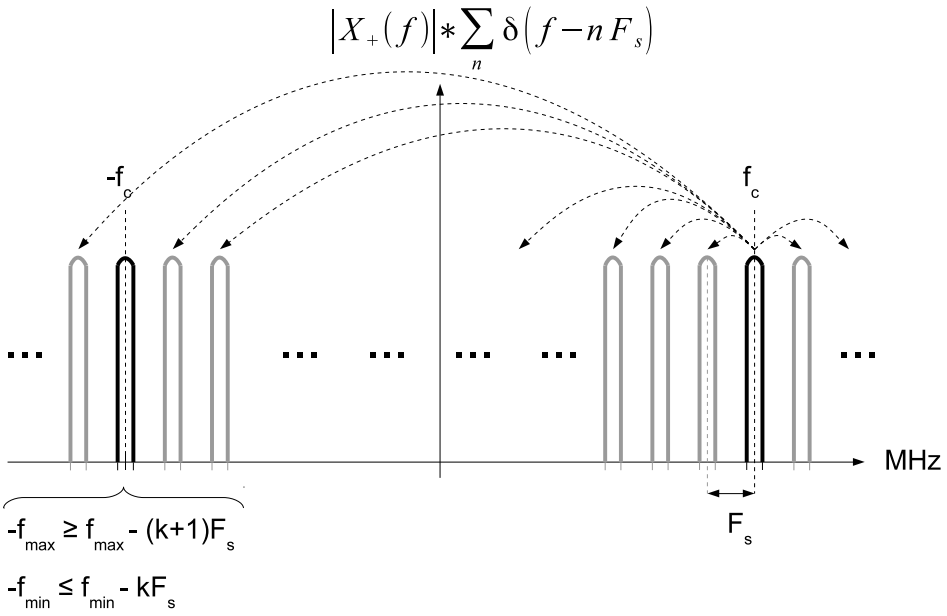


Figure A.2: Replicas of the X_+ band must not overlap the X_- band.

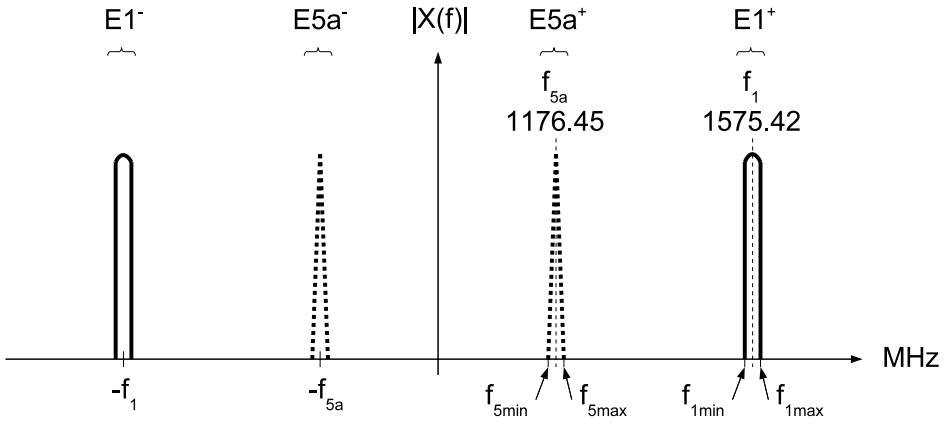


Figure A.3: E5a and E1 bands to be coherently sampled.

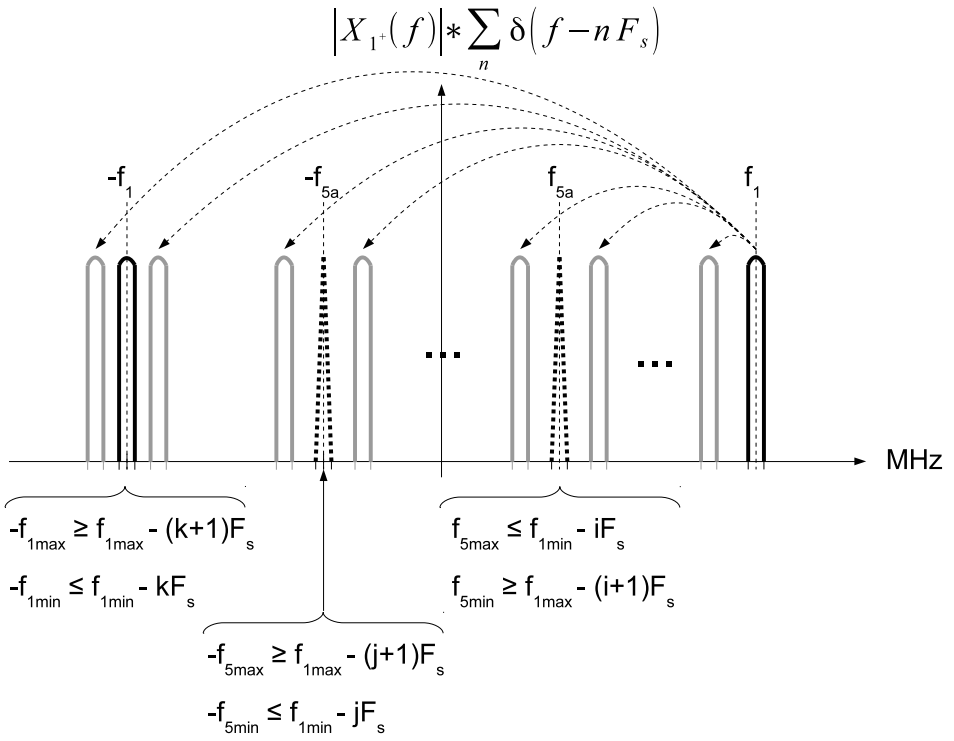


Figure A.4: Replicas of the $E1^+$ band must not overlap other bands.

For the sake of completeness, it remains only to set the conditions under which $E5a^+$ replicas do not overlap $E5a^-$. This situation is illustrated in figure A.5.

A.2.1 $E1^+$ does not overlap $E5a^+$

This happens if and only if

$$\frac{f_{1max} - f_{5min}}{i+1} \leq F_s \leq \frac{f_{1min} - f_{5max}}{i}, \; i \in \mathbb{N} \tag{A.5}$$

Defining $B_1 = (f_{1max} - f_{1min})$ and $B_5 = (f_{5max} - f_{5min})$, this implies

$$0 \leq i \leq \frac{f_{1min} - f_{5max}}{B_1 + B_5} \tag{A.6}$$

Knowing the set of i which verify A.6 it is possible to calculate a first set S_i of intervals of sampling frequencies F_s from A.5.

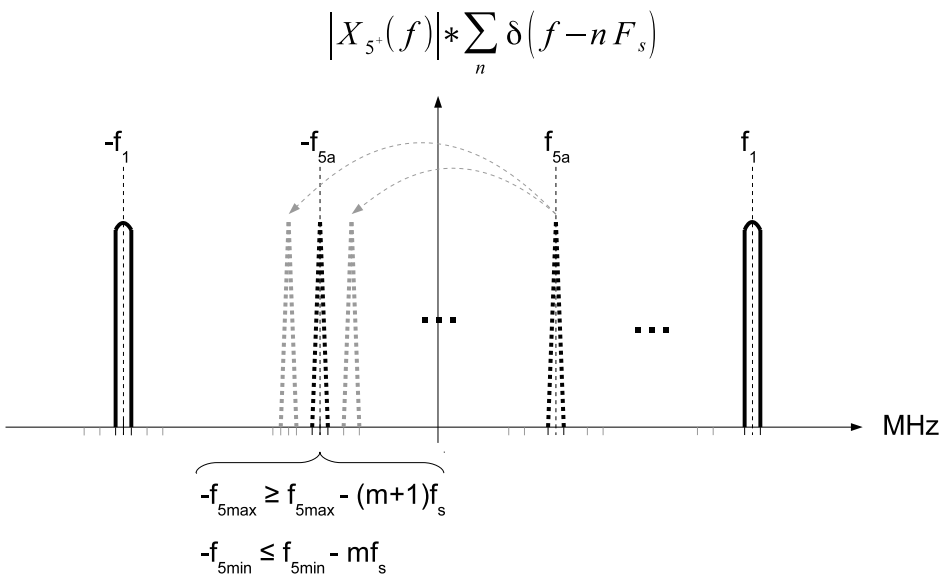


Figure A.5: Replicas of the $E5a^+$ band must not overlap the $E5a^-$ band.

A.2.2 $E1^+$ does not overlap $E5a^-$

This happens if and only if

$$\frac{f_{1max} + f_{5max}}{j+1} \leq F_s \leq \frac{f_{1min} + f_{5min}}{j}, j \in \mathbb{N} \tag{A.7}$$

As previously it implies

$$0 \leq j \leq \frac{f_{1min} + f_{5min}}{B_1 + B_5} \tag{A.8}$$

Again, knowing the set of j which verify A.8 it is possible to calculate a second set S_j of intervals of sampling frequencies F_s from A.7.

A.2.3 $E1^+$ does not overlap $E1^-$

This happens if and only if

$$\frac{2f_{1max}}{k+1} \leq F_s \leq \frac{2f_{1min}}{k}, k \in \mathbb{N} \tag{A.9}$$

It then implies

$$0 \leq k \leq \frac{f_{1min}}{B_1} \tag{A.10}$$

This time also, from the set of k which verify A.10 it is possible to calculate a third set S_k of intervals of sampling frequencies F_s from A.9.

A.2.4 $E5a^+$ does not overlap $E5a^-$

This happens if and only if

$$\frac{2f_{5max}}{m+1} \leq F_s \leq \frac{2f_{5min}}{m}, m \in \mathbb{N} \tag{A.11}$$

This induces

$$0 \leq m \leq \frac{f_{5min}}{B_5} \tag{A.12}$$

Like for the other cases, using the set of m which verify A.12 it is possible to calculate a fourth set S_m of intervals of sampling frequencies F_s from A.12.

A.2.5 Solving for the sampling frequency intervals

The final set S_s of intervals of valid sampling frequencies is simply the intersection of all the sets of intervals:

$$S_s = S_i \cap S_j \cap S_k \cap S_m \tag{A.13}$$

A small optimization in these calculations consists in considering that if there is at least one replica of $E1^+$ before each band $E5a^+$, $E5a^-$ and $E1^-$, then necessarily

$$k > j > i \tag{A.14}$$

It is a realistic assumption as the smallest sampling frequencies being the most interesting ones, as they lower the processing workload downstream, so are the highest values of i, j, k and m. Therefore it is advantageous to calculate the set S_s in this way:

1. Initialize $S_s = \varnothing$
2. Determine the set of i from A.6 and the corresponding first set S_i
3. Determine the set of m from A.12 and the corresponding fourth set S_m
4. For each i:
   (a) Determine the set of $j > i$ from A.8 and the corresponding limited second set $S_{j>i}$
   (b) For each j:
      i. Keep the set of intervals $S_{j \cap i} = S_i \cap S_{j>i}$
      ii. Determine the set of $k > j$ from A.10 and the corresponding limited third set $S_{k>j>i}$

iii. For each k:
   A. Keep the set of intervals $S_{k\cap j\cap i} = S_{j\cap i} \cap S_{k>j>i}$
   B. Build $S_s = S_s \cup (S_m \cap S_{k\cap j\cap i})$

When all possibilities for i, j and k have been exhausted, S_s contains the intervals of valid sampling frequencies.

A.3 References

[1] R. G. Vaughan, N. L. Scott, and D. R. White, "The theory of bandpass sampling," *IEEE Transactions on Signal Processing*, vol. 39, pp. 1973–1984, 1991.

[2] J. G. Proakis and D. K. Manolakis, *Digital Signal Processing*, 4th ed. Prentice Hall, April 2006.

[3] C. Shannon, "Communication in the presence of noise," *Proceedings of the IEEE*, vol. 86, no. 2, pp. 447–457, Feb 1998.

Fourier Series Expansion of a Sine Wave Quantized by a Mid-Rise Uniform Quantizer

B

This appendix presents the calculation of the amplitude harmonics of a sine wave at the output of a mid-rise quantizer. This is an extension of the work done in [1].

Figure B.1 is a representation of one period T of a full scale sine wave at the output of a transfer function of the kind of the one shown in figure 6.2. The initial phase of this sine wave is set to 0 without loss of generality as it appears clearly hereafter. Its angular frequency is noted ω with then $\omega T = 2\pi$.

The quantized sine wave $x_q(t)$ is made of the superposing of L periodic rectangular pairs

$$x_q(t) = \sum_{k=0}^{L-1} s_k(t) \tag{B.1}$$

The k^{th} periodic rectangular pair can be written

$$s_k(t) = \sum_{n=-\infty}^{+\infty} L_k \cdot \Pi_{t_k}(t - T/4 - nT) - L_k \cdot \Pi_{t_k}(t - 3T/4 - nT) \tag{B.2}$$

$\Pi_\delta(t)$ is the function

$$\Pi_\delta(t) = \begin{cases} 1 & \text{if } t \in [-\delta/2, \delta/2] \\ 0 & \text{elsewhere} \end{cases} \tag{B.3}$$

L_k is the amplitude of the two rectangles

$$L_k = \begin{cases} \Delta/2 & \text{if } k = 0 \\ \Delta & \text{if } k > 0 \end{cases} \tag{B.4}$$

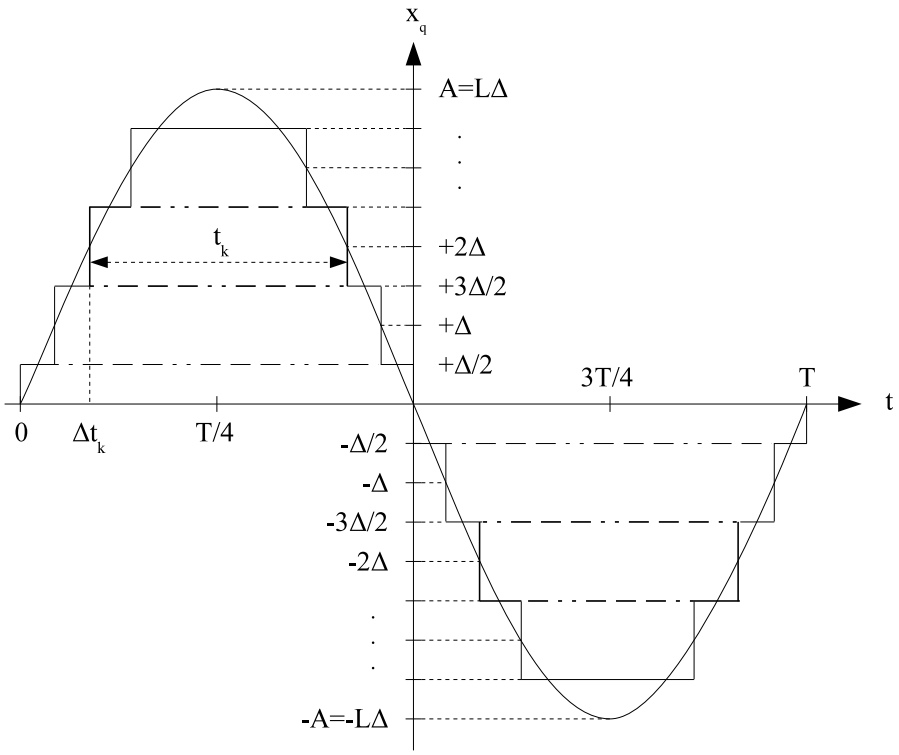


Figure B.1: One period of a sine wave quantized by a mid-rise quantizer.

The width of one rectangle is

$$t_k = T/2 - 2\Delta t_k \tag{B.5}$$

Δt_k, the first crossing time of level $k\Delta$, is defined by

$$A \sin(\omega \Delta t_k) = k\Delta \tag{B.6}$$

That is to say

$$\Delta t_k = \frac{1}{\omega} \sin^{-1}(k/L) \tag{B.7}$$

Each periodic pair can be written as a Fourier series

$$s_k(t) = \sum_{n=-\infty}^{+\infty} c_{n,k} e^{jn\omega t} \tag{B.8}$$

$$c_{n,k} = \frac{1}{T} \int_0^T \left(L_k \cdot \Pi_{t_k}(t - T/4) - L_k \cdot \Pi_{t_k}(t - 3T/4)\right) e^{-jn\omega t} dt \tag{B.9}$$

$$c_{n,k} = \frac{L_k}{T} \int_{\Delta t_k}^{T/2-\Delta t_k} \left(1 - e^{-jn\pi}\right) e^{-jn\omega t} dt$$

It is clear at this point that for n even

$$c_{n,k} = c_{(2\nu),k} = 0 \ \forall k \tag{B.10}$$

For n odd the integration gives

$$c_{n,k} = c_{(2\nu+1),k} = \frac{2L_k}{-j(2\nu+1)\omega T} \left[e^{-j(2\nu+1)\omega t}\right]_{\Delta t_k}^{T/2-\Delta t_k}$$

$$c_{(2\nu+1),k} = \frac{L_k}{-j(2\nu+1)\pi} e^{-j(2\nu+1)\omega T/4} \left(e^{-j(2\nu+1)\omega(T/4-\Delta t_k)} - e^{j(2\nu+1)\omega(T/4-\Delta t_k)}\right)$$

$$c_{(2\nu+1),k} = \frac{2L_k}{(2\nu+1)\pi} e^{-j(2\nu+1)\pi/2} \sin\left((2\nu+1)\omega(T/4 - \Delta t_k)\right)$$

$$c_{(2\nu+1),k} = \frac{2L_k}{(2\nu+1)\pi} (-j)^{2\nu+1} (-1)^{\nu} \cos\left((2\nu+1)\omega \Delta t_k\right)$$

Finally

$$c_{(2\nu+1),k} = \frac{-2jL_k}{(2\nu+1)\pi} \cos\left((2\nu+1)\omega \Delta t_k\right) \tag{B.11}$$

It is to be noted that $c_{(2\nu+1),k}$ is odd itself

$$c_{-(2\nu+1),k} = -c_{(2\nu+1),k} \ \forall\nu, \ \forall k \tag{B.12}$$

So

$$s_k(t) = \sum_{\nu=0}^{+\infty} 2jc_{(2\nu+1),k} \sin\left((2\nu+1)\,\omega t\right)$$

$$s_k(t) = \sum_{\nu=0}^{+\infty} \frac{4L_k}{(2\nu+1)\,\pi} \cos\left((2\nu+1)\,\omega\Delta t_k\right) \sin\left((2\nu+1)\,\omega t\right) \tag{B.13}$$

The amplitude of the $(2\nu+1)^{th}$ harmonic of $x_q(t)$ is obtained by substitution of (B.13) in (B.1)

$$A_{2\nu+1} = \frac{2A}{(2\nu+1)\,L\pi}\left(1 + 2\sum_{k=1}^{L-1} \cos\left((2\nu+1)\sin^{-1}\left(k/L\right)\right)\right) \tag{B.14}$$

Figure B.2 is a plot of the attenuation of the fundamental frequency at the output of the quantizer as a function of the number of quantization bits $N = \log_2(L) + 1$.

The power ratios between the 3^{rd}, 5^{th} and 7^{th} harmonics and the fundamental frequency (at the input of the quantizer) are presented in figure B.3, as a function of N also.

References

[1] A. G. Clavier, P. F. Panter, and D. D. Grieg, "Distortion in a Pulse Count Modulation System," *Transactions of The American Institute of Electrical Engineers*, vol. 66, pp. 989–1005, 1947.

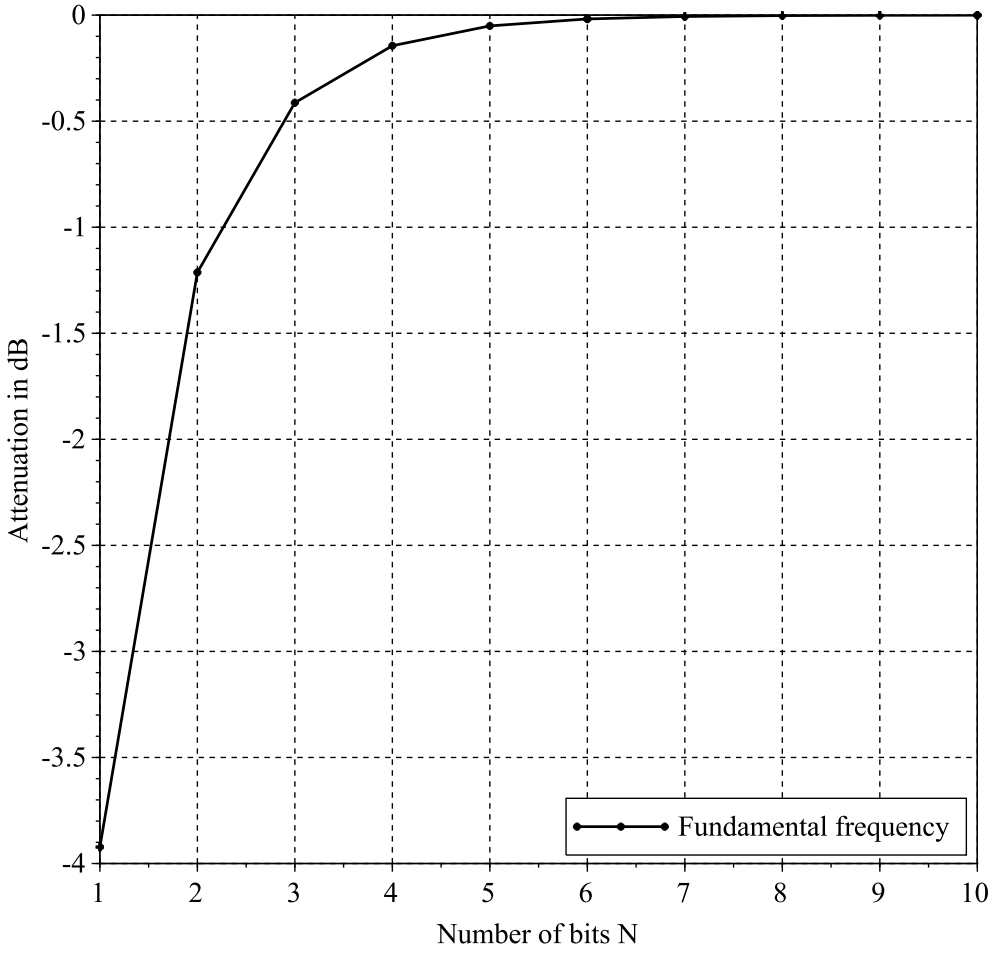


Figure B.2: Attenuation of the fundamental frequency at the output of the mid-rise quantizer vs N.

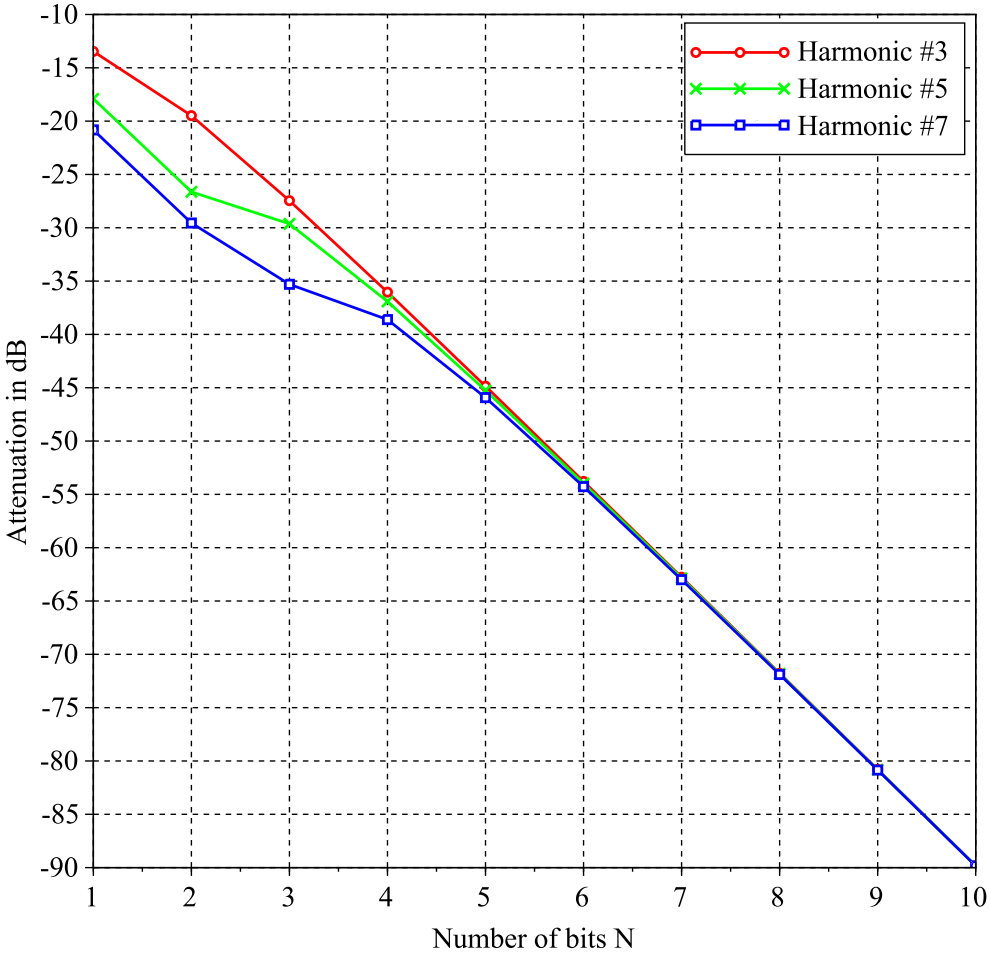


Figure B.3: Power ratios between the first harmonics and the fundamental frequency vs N.

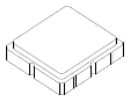
SF1186B-2 Datasheet

RFM

SF1186B-2

1575.42 MHz SAW Filter

- ***Designed for Front End GPS Applications***
- ***Low Insertion Loss***
- ***3.0 x 3.0 x 1.3 mm Surface-Mount Case***
- ***No Matching Circuit Required***
- ***Complies with Directive 2002/95/EC (RoHS)***



SM3030-6

Maximum Ratings at +25°C unless stated otherwise

Rating	Symbol	Value	Units
Maximum Input Signal Level		+10	dBm
Withstanding DC Voltage	WVdc	4	Volts
Operating Temperture Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{STG}	-40 to +105	°C
Lead Soldering Temperature for 10 Seconds	T_{WAVE}	260	°C
Peak Reflow Solder Temp for 40 Seconds	T_{Reflow}	235	°C
Suitable for lead-free soldering - Max Soldering Temperature		260°C for 30 s	

Electrical Characteristics

Characteristic		Sym	Notes	Min	Typ	Max	Units
Center Frequency		f_O	1		1575.42		MHz
1dB Passband width			1	2.046	15.3		MHz
Pass Band Variation Fc ±2.0 MHz					0.1	1.0	dB
Pass Band VSWR					1.4	2.0	
Insertion Loss			1		2.68	3.5	dB
Absolute Attenuation @	850 MHz		1	45	51.2		dB
	1500 MHz		1	40	52.7		
	1535.42 MHz		1	20	38.9		
	1615.42 MHz		1	20	58.8		
	1640 MHz		1	45	59.1		
	1700 MHz		1	50	56.7		
Temperature Coefficient				-30			ppm/°C
Operating Temperature		T_A	1	-40		+85	°C
Single Ended Input / Output, Impedance match		No matching network required for operation at 50 ohms					
Case Style		SM3030-6 3 x 3 mm Nominal Footprint					
Lid Symbolization	y=year, ww=week, s=shift	468 YWWS					
Standard Reel Quantity	Reel Size 7 Inch		6	500 Pieces/Reel			
	Reel Size 13 Inch			3000 Pieces/Reel			

Electrical Connections

Pin #	Description	Pin #	Description
1	Ground	4	Ground
2	Input	5	Output
3	Ground	6	Ground

CAUTION: Electrostatic Sensitive Device. Observe precautions for handling.

Notes:

1. Unless noted otherwise, all specifications apply over the operating temperature range with filter soldered to the specified demonstration board without impedance matching and measured with 50 Ω network analyzer.
2. The design, manufacturing process, and specifications of this filter are subject to change.
3. Either Port 1 or Port 2 may be used for either input or output in the design. However, impedances and impedance matching may vary between Port 1 and Port 2, so that the filter must always be installed in one direction per the circuit design.
4. US and international patents may apply.
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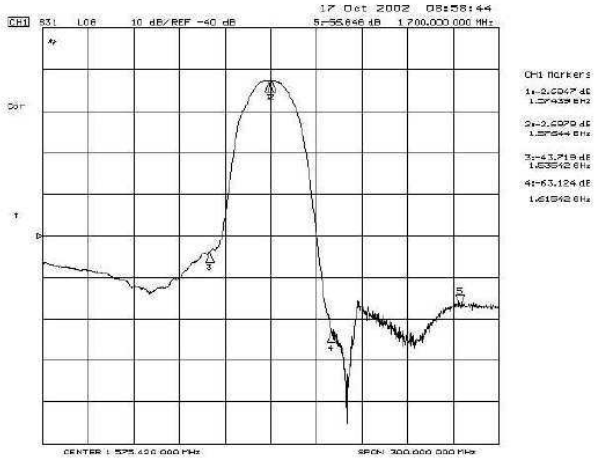
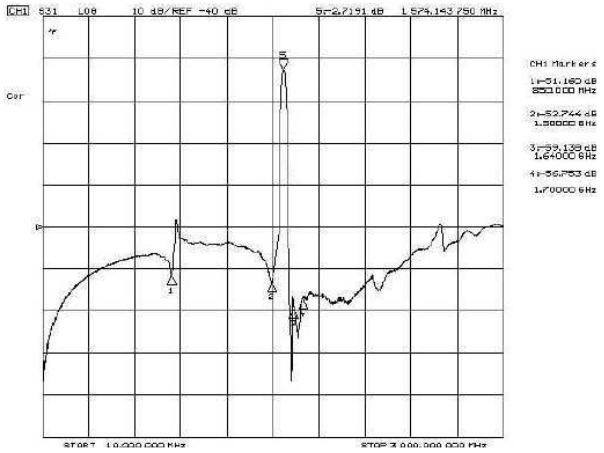
6. Tape and Reel Standard Per ANSI / EIA 481.
7. ©Copyright 1999, RF Monolithics Inc.

Transfer function :

(1) S21 response (span : 300 MHz)

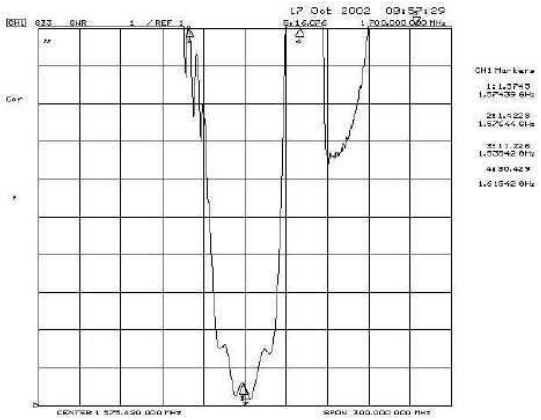


(2) S21 response (span : 3 GHz)

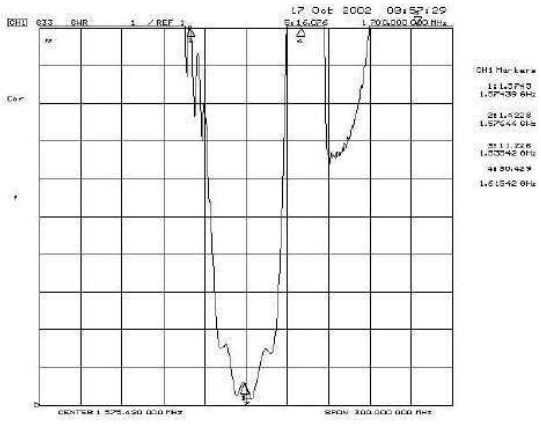


Reflection Functions:

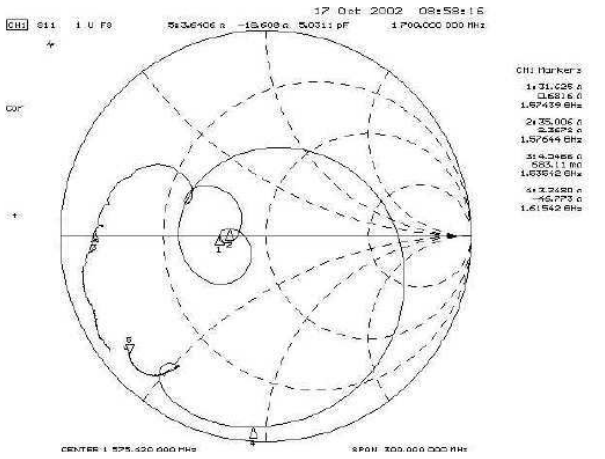
S11

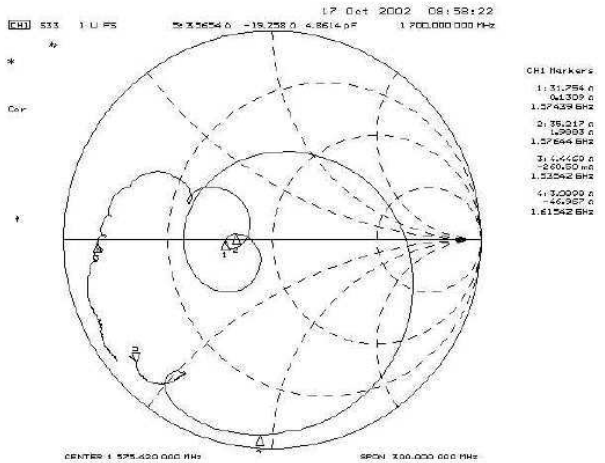


S22

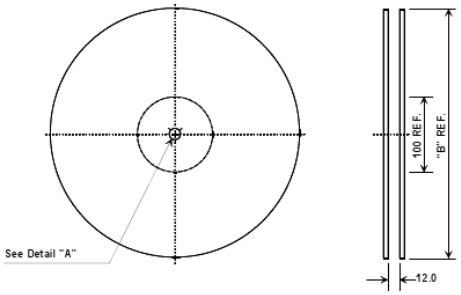


Reflection Functions:

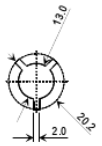




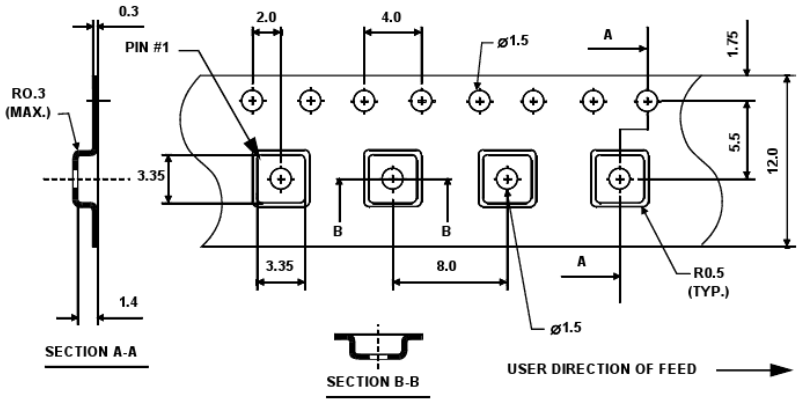
Tape and Reel Specifications



"B" Nominal Size		Quantity Per Reel
Inches	millimeters	
7	178	500
13	330	3000

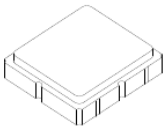


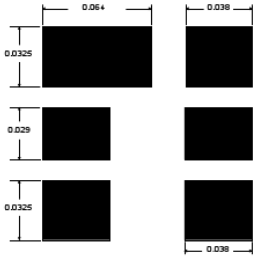
COMPONENT ORIENTATION



SM3030-6 Case

6-Terminal Ceramic Surface-Mount Case
3.0 X 3.0 mm Nominal Footprint





Foot Print Dimensions in Nominal Inches

Case Dimensions						
Dimension	mm			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.87	3.0	3.13	0.113	0.118	0.123
B	2.87	3.0	3.13	0.113	0.118	0.123
C	1.12	1.25	1.38	0.044	0.049	0.054
D	0.77	0.9	1.03	0.030	0.035	0.040
E	2.67	2.80	2.93	0.105	0.110	0.115
F	1.47	1.6	1.73	0.058	0.063	0.068
G	0.72	0.85	0.98	0.028	0.033	0.038
H	1.37	1.5	1.63	0.054	0.059	0.064
I	0.47	0.6	0.73	0.019	0.024	0.029
J	1.17	1.3	1.43	0.046	0.051	0.056

Electrical Connections		
Connection		Terminals
Port 1	Single Ended Input	2
Port 2	Single Ended Output	5
	Ground	All others
Single Ended Operation Only		
Dot indicates Pin 1		

Materials	
Solder Pad Termination	Au plating 30 - 60 µinches (76.2-152 µm) over 80-200 µinches (203-508 µm) Ni.
Lid	Fe-Ni-Co Alloy Electroless Nickel Plate (8-11% Phosphorus) 100-200 µinches Thick
Body	Al_2O_3 Ceramic
Pb Free	

TOP VIEW

BOTTOM VIEW