Conducted EMC modeling and EMI filter design integrated class-D amplifiers and power converters

Roberto Mrad

ÉCOLE CENTRALE LYON

N° d'ordre : ECL 2014-19

Thèse de l'Université de Lyon

Délivrée par l'Ecole Centrale de Lyon

Spécialité : Energie et Systèmes

Soutenue publiquement le 30 Juin 2014

Par

Roberto Mrad

Préparée aux Laboratoires Ampère et INL
Financée par la société ST Microelectronics

Conducted EMC Modeling and EMI Filter Design for Integrated Class-D Amplifiers and Power Converters

Ecole Doctorale

Electronique, Electrotechnique, Automatique

Jury

Rapporteur	Flavio Canavero	Professeur (Politecnico di Torino)
Rapporteur	Jean-Luc Schannen	Professeur (ENSE^3, Grenoble)
Examinateur	Etienne Sicard	Professeur (INSA, Toulouse)
Directeur de thèse	Christian Vollaire	Professeur (Ecole Centrale de Lyon)
Encadrant	Florent Morel	Maitre de conférences (Ecole Centrale de Lyon)
Encadrant	Gaël Pillonnet	Chercheur (CEA, Grenoble)
Invité	Angelo Nagari	Ingénieur (ST Microelectronics, Grenoble)
Invité	Bertrand Lacombe	Ingénieur (SAFRAN Sagem, Massy)

Ecole Doctorale de l'Electronique, l'Electrotechnique et de l'Automatique (EEA)

Abstract

Ecole Centrale de Lyon Doctor of Philosophy

Conducted EMC Modeling and EMI Filter Design
for Integrated Class-D Amplifiers and Power Converters

by Roberto MRAD

English:

Switching power management circuits are widely used in battery powered embedded applications in order to increase their autonomy. In particular, for audio applications, Class-D amplifiers are a widespread industrial solution. These, have a similar architecture of a buck converter but having the audio signal as reference. The switching nature of these devices allows us to increase significantly the power efficiency compared to linear audio amplifiers without reducing the audio quality. However, because of the switching behavior, Class-D amplifiers have high levels of electromagnetic (EM) emissions which can disturb the surrounding electronics or might not comply with electromagnetic compatibility (EMC) standards. To overcome this problem much architecture appeared in the state of the art that reduces the emissions, however, this has never been enough to remove electromagnetic interference (EMI) filters. It is then useful to optimize these filters, thus, it has been set as the goal of this PhD thesis. The latter has been divided to four main axes which can be resumed by the following.

First, this work started by developing a frequency domain modeling method in order to simulate and predict the EMI of Class-D amplifiers in the final application. The method is based on system to block decomposition and impedance matrix modeling and manipulation. After providing all the theoretical background, the

method has been validated on integrated differential Class-D amplifier. The experimental measurements have permitted to validate the method only up to 100 MHz. However, this is sufficient to cover the conducted EMC frequency band.

Second, the EMI at the supply rails of Class-D amplifiers has been treated. As the battery is often the same power supply for all applications in an embedded system, an EMI filter or a decoupling capacitor is needed to prevent the noise coupling by common impedance. Designing this filter needs the knowledge of the battery impedance at the desired frequencies. Therefore the present work dealt also with measuring the high frequency impedance of a battery. Afterwards, an experimental validation has been carried on with a DC-DC converter and a Class-D amplifier.

The developed model allows a virtual test of the switching device in the final application. However, it is more useful if the model is able to help the system integrator in designing filters. Thus, third, the model has been implemented in an optimization loop based on a genetic algorithm in order to optimize the filter response, and also, reduce the additional power losses introduced by an EMI filter. The optimization search space has been limited to the components available on the market and the optimization result is given as component references of the optimal filter referring to the optimal solution found. This procedure has been validated experimentally.

Finally, EMI filters often are constituted by magnetic components such as ferrite beads or inductors with magnetic cores. Thus, introducing the EMI filter in the audio path, adds a nonlinear behavior in the audio frequency band. Designing a high quality EMI filter require taking into account this phenomenon and studying its impact of the original amplifier audio performance. Therefore, the Jiles-Atherton model for magnetic materials has been used for ferrite bead modeling. Hereafter, the impact on the time and frequency domain signals has been simulated and compared to measurements. Finally, the total harmonic distortion (THD) has been computed for different signal amplitudes and compared to the THD measured using an audio analyzer. Accurate results have been obtained on a wide range of signal amplitudes.

As a conclusion, this work aimed to design optimal EMI filters for Class-D amplifiers. Thus, we dealt with improving their EMI response, reducing their additional power losses and evaluating their impact on the audio quality.

Français:

Les convertisseurs de puissance sont largement utilisés de nos jours dans des applications qui demandent une grande autonomie énergétique, comme par exemple ceux qui sont alimentés par des batteries. En particulier, les amplificateurs de type Class-D sont fréquemment utilisés dans les applications audio. Ces amplificateurs commutés ont une architecture ressemblante à celle d'un convertisseur DC-DC, ce qui les permet d'avoir une efficacité énergétique élevée. Cependant, leur inconvénient majeur est la forte émission en perturbations électromagnétiques (EM). Cela peut causer des problèmes de conformité avec les normes de compatibilité électromagnétique (CEM), ou bien perturbé le bon fonctionnement des applications électroniques qui l'entour. Pour cela, ils existent de nombreuses études qui permettent de réduire les émissions d'un amplificateur de Class D. Cependant, cela n'est pas suffisant pour retirer le filtre de CEM. Il est donc nécessaire d'optimisé ces filtres et de faciliter leurs conceptions. Ceci est le but de la présente thèse et il est divisé en quatre grandes parties.

La première partie commence par développer une technique de modélisation dans le domaine fréquentiel. Cette technique qui est basée sur la détermination et la manipulation des matrices d'impédances a comme but de simuler et prédire les perturbations EM générés par un amplificateur de Class D. Tous les aspects théoriques de la méthode ont été développés. Ensuite, une application pratique sur un système de Class D dédié à la téléphonie mobile nous a permis de valider la méthode jusqu'à une fréquence de 100 MHz.

Un amplificateur de Class D est une source de perturbation aussi bien sur les rails d'alimentation que sur les rails de sortie. Pour cela, le filtre de CEM est nécessaire sur les rails de l'alimentation comme il y est en sortie. Néanmoins, un filtre correctement construit doit être conçu en prenant en compte l'impédance de la charge qui est la batterie dans ce cas. Pour cela, la deuxième partie a pour objectif la mesure de l'impédance de la batterie sur la gamme de fréquence considérée. Ainsi, une technique de mesure d'impédance de batterie en utilisant un impédance mètre est développée. Ensuite, une application expérimentale sur un convertisseur DC-DC et une batterie nous a permis de valider la procédure de mesure.

La troisième partie s'est focalisée sur l'optimisation du filtre de CEM. Le modèle fréquentiel développé dans la première partie est intégré dans une boucle d'optimisation

basée sur un algorithme génétique. L'optimisation inclus plusieurs critères dans sa fonction objective qui sont l'augmentation de la capacité du filtre à réduire les émissions EM, la diminution des pertes supplémentaire due à l'utilisation du filtre et finalement le gain du filtre dans la bande de fréquence du signal audio. Cette étude est poursuivie par une validation expérimentale.

La quatrième et la dernière partie étudie et quantifie les impacts du filtre de CEM sur la qualité audio de l'amplificateur. En effet, le filtre de CEM est l'un des chemins propagation du signal audio. Par suite, tout comportement non linéaire du filtre conduit à la distorsion du signal audio. Pour cela, cette partie est dédiée à la modélisation et la simulation des composants passifs contenant un matériau magnétique. En particulier, l'étude s'est focalisée sur la modélisation des perles de ferrite en utilisant le modèle de matériaux magnétiques Jiles-Aterthon. Les résultats de simulations sont comparés avec la mesure dans le domaine temporel et fréquentiel. En plus, le calcul du taux de distorsion harmonique nous a permis de valider le modèle sur une large plage d'amplitude.

Contents

List of Figures

List of Tables

Abbreviations

AA	**A**udio **A**nalyzer
ADS	**A**dvanced **D**esign **S**ystem
CISPR	International Special Committee on Radio Interference
CM	**C**ommon **M**ode
DM	**D**ifferential **M**ode
DUT	**D**evice **U**nder **T**est
EM	**E**lectro**M**agnetic
EMC	**E**lectro**M**agnetic **C**ompatibility
EMI	**E**lectro**M**agnetic **I**nterference
EIS	**E**lectrochemical **I**mpedance **S**pectroscopy
FCC	**F**ederal **C**ommunications **C**ommission
FFT	**F**ast **F**ourier **T**ransform
GA	**G**enetic **A**lgorithm
IA	**I**mpedance **A**nalyzer
IC	**I**ntegrated **C**ircuit
ICEM	**I**ntegrated **C**ircuit **E**lectromagnetic **M**odel
JA	**J**iles-**A**therton
LISN	**L**ine **I**mpedance **S**tabilization **N**etwork
MCM	**M**ulti-**C**arrier **M**odulation
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
PC	**P**ortable **C**omputer
PCB	**P**rinted **C**ircuit **B**oard
PCM	**P**ulse **C**ode **M**odulation
PDM	**P**ulse **D**ensity **M**odulation
PDN	**P**ower **D**istribution **N**etwork
PEEC	**P**artial **E**lement **E**quivalent **C**ircuit
PWM	**P**ulse **W**idth **M**odulation
RLC	Resistance, Inductance, Capacitance

rms	**r**oot **m**ean **s**quare
S	**S**cattering parameters
SC	**S**hort **C**ircuit
SMPS	**S**witched **M**ode **P**ower **S**upply
SMT	**S**urface **M**ounted **T**echnology
SNR	**S**ignal to **N**oise **R**atio
SOC	**S**tate **O**f **C**harge
THD	**T**otal **H**armonic **D**istortion
VCCI	**V**oluntary **C**ontrol **C**ouncil for **I**nterference
VNA	**V**ector **N**etwork **A**nalyzer
WL-CSP	**W**afer-**L**evel **C**hip **S**cale **P**ackage
$\Sigma\Delta$	**Sigma Delta**

Dedicated to those who believed in me...
...to my beloved family

Chapter 1

Introduction

Nowadays, embedded electronic systems became a necessity for every working environment and a companion in everyday life. Most of the time, many devices coexist on the same field or even many functionalities coexist in the same device. Hence, modern electronics offers complex devices that contain various kinds of applications, such as radio communication, navigation, audio, video, automation, control, etc. Therefore, analog and digital signals, high and low frequency signals, high and low power levels, etc., are taking place in the same package, or even more, on the same Printed Circuit Board (PCB). The decrease of the integration scale which is reported for semiconductor scaling by Gordon Moore's law [1], allows us to have more integrated scheme and more compact systems. The electronic applications are then closer and the PCBs are highly packed with electronic components. For instance, Fig. 1.1 shows the PCB of a modern smart-phone, where the electronic components are placed very close to each other. Therefore, due to the modern electronic requirements, Electromagnetic Compatibility (EMC) become a complex issue.

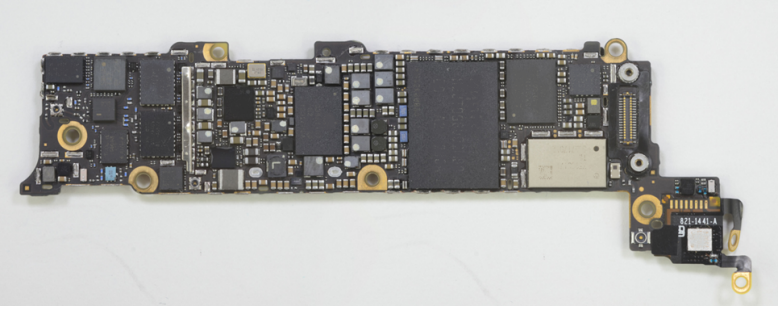


FIGURE 1.1: PCB of a modern smart-phone.

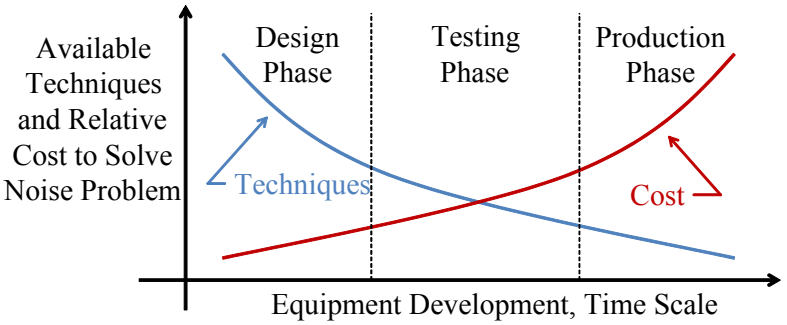


FIGURE 1.2: Product development and noise reduction [5].

1.1 EMC, definition and concern

The EMC of two electronic systems is the fact that the two of them are able to operate in the same ElectroMagnetic (EM) environment, without exchanging any undesirable interference of EM energy. This can be done whether by minimizing the level of unintentional EM emission, whether by maximizing the level of immunity against the unintentional EM emission, whether by limiting the coupling paths. In case of improper EMC, malfunctioning can occur which might lead to safety problems. The noise interference can for example disturb the police, fire and alarm communications, the radio and television broadcasting or even the air traffic control [2, 3]. Therefore, EMC standards were established in many countries such as European countries (CISPR: International Special Committee on Radio Interference), USA (FCC: Federal Communications Commission), Japan (VCCI: Voluntary Control Council for Interference), etc., in order to define the limits for EM emission and immunity. A number of EMC standards is listed in [4].

EMC is a major challenge for designers. The ElectroMagnetic Interference (EMI) can be the reason for a system failure or an important declination of the system performance. Such inconvenience drives the designers to use backup solutions, or to review their products from the early design stages. In both cases, additional time and cost are needed in the production chain. To avoid these functioning and extra cost problems, without forgetting the inconformity to standard risks, it is then necessary to include the EMC at the early stage of development. Knowing that, dealing with EMC in advance allows us a wider choice of available solutions with a lower cost (Fig. 1.2).

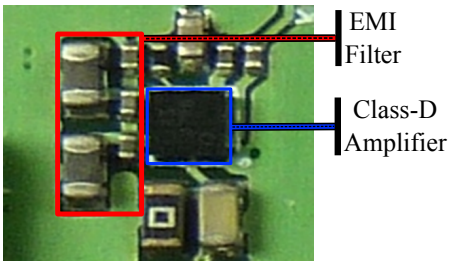


FIGURE 1.3: A Class-D amplifier and its dedicated EMI filter in the final application.

1.2 Problem background

Standalone and portable devices present an interesting solution for many applications and usually they are powered by batteries (or by energy harvesting). Due to the variety of applications in a device, many supply levels are needed. Hence, to fulfill the power requirements of complex devices and for a longer autonomy, power converters and power management circuits are widely used. These components have a high level of EM emissions as they deal with power switching. In general, such circuits are well-filtered to limit the noise leakage onto the supply lines.

Currently the switching Class-D audio amplifier is extensively used in many types of applications, such as televisions, cars, portable computers (PCs), smart-phones, GPS, game pads and others. It is a relevant solution for audio applications because it allows us to increase significantly the power efficiency, comparing to the other amplifier classes [6, 7]. It has a similar architecture as a buck converter but having the audio signal as the reference voltage. However, as any switching circuit, Class-D amplifiers generate high level of EM emissions. A special care is needed to reduce its impact on the surrounding electronics. Many circuit solutions have been created to lower a Class-D EM emissions [8–11], nevertheless, in practical implementations the EMI filter is still mandatory. Fig. 1.3 shows an example of an integrated Class-D amplifier with the corresponding EMI filter. It can be seen that the filter occupy more than twice the area of the Class-D amplifier itself. For some applications, the filter can be even more expensive than the Class-D amplifier itself. EMI filters are bulky and add extra cost to the production. In addition, such filters are challenging to design because their behavior highly depends on parasitic components [12].

The present work is intended to study the EMC of integrated Class-D amplifiers (all the electronic units are integrated on the same silicon die). Generally, they are used in the systems where the primary function is display, audio, telecommunication, transmission, processing, etc., which generate unintentional EM emissions. Therefore, standards such as the EN55022 (Europe) [13] or the FCC-Part-15 Subpart-B (USA) [14] are often applied for these types of devices. According to these standards, the EMC study must be divided into conducted and radiated emissions. These norms define the conducted emission limits in the frequency band [150 kHz, 30 MHz] and the radiated ones in the frequency band [30 MHz, 1 GHz]. Dealing with both might need a long time period which exceed most probably the duration of a PhD thesis. Therefore, the present work focuses only on the conducted emissions generated by Class-D amplifiers.

As mentioned before, treating any EMC problem can be resumed to three different strategies: (i) reducing the emission of the aggressor, (ii) increasing the immunity or the victim or (iii) substituting the perturbation path. Knowing that a combination between strategies can be very efficient. This work focuses on one single strategy which is the coupling path. Usually, Class-D amplifier chips are built by semiconductor manufacturers, afterwards, each system integrator uses the same chip design into its own application. Thus, the amplifier chip is mounted on a different PCB and placed in a different environment for each different application. The coupling path is then dependent from the application itself. Therefore, the passive surrounding of the Class-D amplifier, in particularly the EMI filter, must be correctly designed for each different case. Often, due to the lack of tools, their design is based on experimental tests, which is a long process that lead to suboptimal solutions. In some cases, the previous design is also used for the newer version of the application which is not appropriate. Therefore, a method that predict the disturbances in the final application is then very interesting. Furthermore, an automated design of the EMI filter, using an accurate modeling method can lead to optimal filtering solutions.

EMI filters do not belong to the system main architecture. They are only added for EMC issues. However, as a part of the final application, they have an impact on the system performance. In the case of a Class-D amplifier, the EMI filter can create additional losses in the amplifier itself, thus, decrease the system power efficiency. Moreover, the EMI filter is on the audio path. When using nonlinear filtering

components such as magnetic components, the audio quality can be significantly reduced. Therefore, such phenomena must be carefully treated.

1.3 Objectives and scope of thesis

As a cooperation between four institutes, this PhD thesis have two different sides of objectives. On the first hand, the research laboratories AMPÈRE and INL focus on an innovative, rigorous and a scientific approach to reach the PhD goals. The AMPÈRE laboratory is specialized in the power electronics and in EMC. The INL laboratory is specialized in the analog design of integrated power circuits, in particularly Class-D amplifiers. On the second hand, both companies ST-Ericsson and ST-Microelectronics make sure that this Research and Development (R&D) work agree with the company perspectives. Both companies are worldwide leaders in semiconductor manufacturing, in particular integrated Class-D amplifiers. Therefore, the thesis objectives, which are described by the following, are dissociated as scientific objectives and company objectives.

1.3.1 Scientific objectives

According to the problem background which is presented in the precious section, the scientific objectives are set as follow:

- Develop a modeling approach for Class-D amplifiers which has a high accuracy in the conducted emission frequency band ($[150\,kHz,\ 30\,MHz]$). It must be a predictive method with a short simulation time to be used at the early design stage. The modeling approach should be easily applied on any Class-D application.
- Develop an automated EMI filter design that assist the system integrators while implementing Class-D amplifiers. The automated design must use the modeling approach developed in the previous point, in order to have an accurate filtering solutions. The latter must have realistic component values.
- Improving the EMI filter must not deteriorate any of the system performances. Thus, we must evaluate the impact of the EMI filter on the main function of a Class-D amplifier. In particular, it is required to model the

magnetic components used for EMI suppression and analyze the occurring phenomenon in the audio frequency band.

1.3.2 Company objectives

The above mentioned companies produce integrated Class-D amplifier chips. The analog designers tend to create amplifiers with the lowest possible of EM emissions. However, this is not enough if the amplifier is improperly implemented in the final applications. Therefore, the company objectives can be resumed as follow:

- Develop a tool or a method that helps the system integrators in implementing the Class-D amplifiers. The goal is to assist the company costumers while integrating these circuits in their final application. The method must be accurate and provide the user the best EMC results. The approach need to be predictive, accurate and user friendly. In addition, it is favorable that this method be able to generate filtering solutions dedicated to a given application, without degenerating any of the amplifier original performance provided by the manufacturer.

1.4 Thesis structure

The rest of this report is organized as follow:

Chapter 2 gives a short introduction to Class-D amplifiers. Therefore, it explains some of the functioning principles and reveals the main causes for Class-D amplifier EM emissions. Afterwards, this chapter provide a quick review on the state of the art for EMI reduction regarding Class-D amplifiers.

Chapter 3 develops a frequency domain modeling method in order to simulate and predict the EMI of Class-D amplifiers in the final application. The method which is dedicated for converters with N active conductors, is based on system to block decomposition and impedance matrix modeling and manipulation. After providing all the theoretical background, the method has been validated on two case of studies. The first case is an integrated differential Class-D amplifier followed by an EMI filter and a loudspeaker. The

second case is a DC-DC converter supplied by the battery. Here, the study has required to measure the high frequency impedance of the battery.

Chapter 4 focuses on the automation of the EMI filter design. Therefore, the model has been implemented in an optimization loop based on a genetic algorithm in order to optimize the filter response, and also, reduce the additional power losses introduced by an EMI filter. The optimization search space has been limited to the components available on the market and the optimization result is given as component references of the optimal filter referring to the optimal solution found. Afterwards, an experimental validation has been carried out.

Chapter 5 is intended to study and evaluate the impact of EMI filters on the audio quality of Class-D amplifiers. Thus, it models the EMI suppression components and investigate their behavior in the audio frequency band. For this purpose, the Jiles-Atherton model for magnetic materials has been used for ferrite bead modeling. Hereafter, the impact on the time and frequency domain signals has been simulated and compared to measurements. Finally, the total harmonic distortion (THD) has been computed for different signal amplitudes and compared to the THD measured using an audio analyzer.

Chapter 6 concludes this report by summarizing the main ideas and results. Afterwards, it proposes some of the possible perspectives for this work which are based on some early investigations.

Chapter 2

Class-D Amplifiers from the EMC Point of View

Class-D audio amplifier principles have been invented by Dr. A. H Reeves back in 1947 [15]. First practical designs appeared in the early 60's [15] and after that, Class-D amplifiers kept evolving until today. Nowadays, they are able to provide higher than 95 % of power efficiency [16, 17]. Classical audio amplifiers such as Class-A, Class-B or Class-AB offer the best audio quality [18, 19] comparing to the switching or the hybrid classes, but their power efficiency cannot exceed 78.5 % in theory [17, 20]. Indeed, the Class-D amplifier is mainly used in embedded systems due to its power efficiency, but also, in addition to its smaller chip size, for low power applications it doesn't need a heatsink to dissipate the heat due to the ohmic losses.

2.1 Class-D amplifier basics

A Class-D amplifier can be divided into two major parts: the power stage and the modulator. The power stage is made by power switches (mostly Metal Oxide Semiconductor Field Effect Transistor or MOSFET) which are sized in a manner to handle all the power stress and also to obtain an optimal efficiency at the nominal output power. Its role is to provide the needed power to the loudspeaker. The modulator is an analog or digital design that generates a pulse train according to the audio signal. Its role is to control the power stage. A block diagram of an open loop Class-D audio amplifier is given in Fig. 2.1.

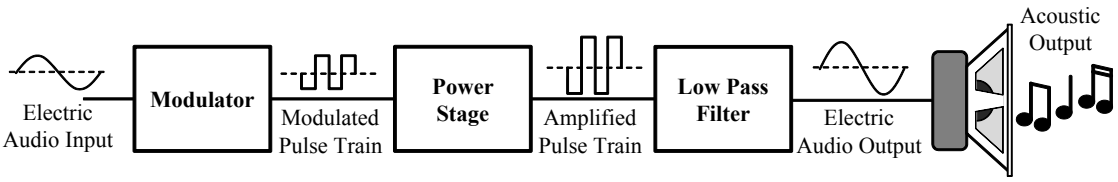


FIGURE 2.1: A block diagram of an open loop Class-D audio amplifier.

2.1.1 Power stages

Two different types of power stages can be distinguished:

The single ended power stage [21, 22]: The single ended power stage is shown in Fig. 2.2 and contains one switching cell. This, contains two MOSFET power switches which can be a N-MOSFET or a P-MOSFET. The output voltage V_{OUT} which is the voltage across the load, can switch between the supply voltage V_S and the reference voltage $0\,V$. Note that most of the single ended topologies enforce a DC current at the load which can be removed by placing a capacitor in series with the speaker.

The differential power stage [16, 23]: Also called H-Bridge power stage, the differential power stage is shown in Fig. 2.3. It contains two switching cells which can switch between V_S and $0\,V$. Thus, the voltage across the load V_{OUT} can switch between V_S, $0\,V$ and $-V_S$.

In both cases the gate drivers are used to ensure that for a single switching cell, the two power switches are never turned on at the same time [24], thus, prevent any short circuit between V_S and $0\,V$ which damaged the amplifier . This can be done by introducing a dead time between turning off one switch and turning on the other one. During the dead time the MOSFET body diode is used as a free-wheeling diode to assure the current flow of the inductor. Therefore, the shortest a dead time is, the better it is because the body diode has higher conduction losses due to it's narrower canal. Also, a longer dead time induce more audio distortion [24].

The switching nature of the power stage allows us to use the power transistors in a "digital mode". In other words, the transistors are used as fully on or fully off, thus, theoretically they behave as short circuits or open circuits, which lead

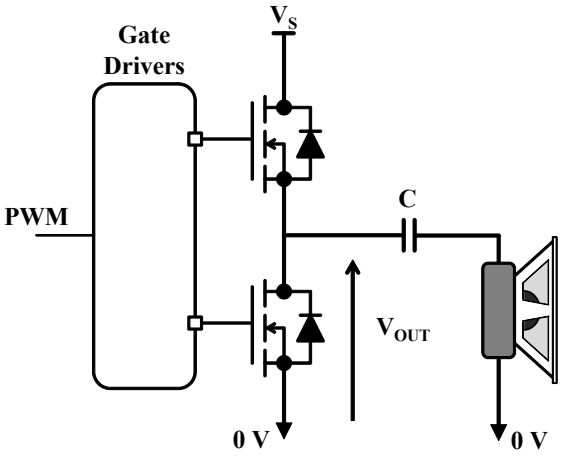


FIGURE 2.2: Single ended power stage.

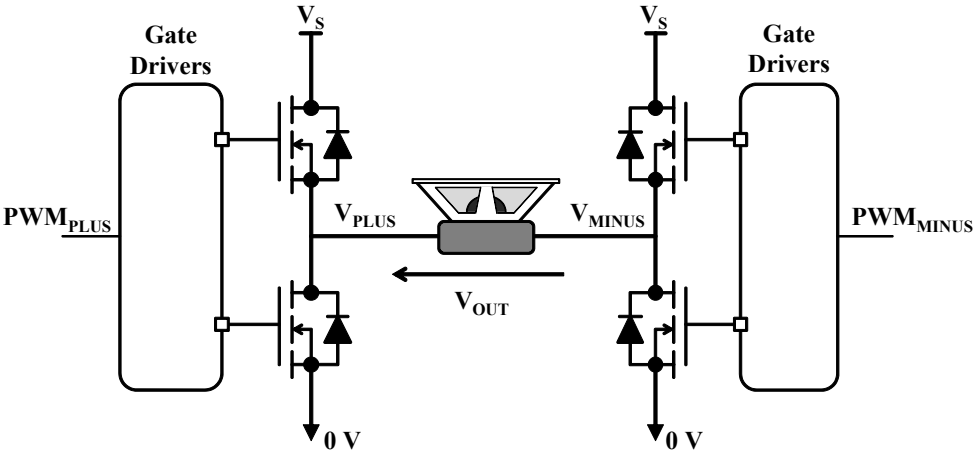


FIGURE 2.3: H-Bridge power stage.

to a 100 % of theoretical power efficiency. In the real world, the electrical units (transistors, diodes, inductors, capacitors, etc.) are not ideal, they have several imperfect properties such as the internal resistance, threshold voltage, leakage current, etc. that create power losses in the amplifier. Therefore, a typical power efficiency of a Class-D amplifier ranges between 80 % and 97 % [17].

Generally, in integrated solutions, the differential topology is used. It allows us to double the voltage across the load, thus, increase four times the amplifier output power for the same supply voltage and the same load impedance. In addition, the capacitor needed at the output of a single ended topology can be problematic in many embedded applications. As the audio frequency band starts from 20 Hz, few μF are needed [17] to stop the DC current without affecting the audio frequency band. Such capacitors are bulky which gives a considerable advantage to the

differential topology.

2.1.2 Modulations

The signal at the output of a switching cell has the same shape as the modulated pulse stream, but with different voltage levels. The modulation type is then in direct relation with the structure of the amplifier output spectrum, which means a significant impact on the amplifier EMC, at frequencies related to the switching frequency. The most common modulation technique is the Pulse Width Modulation (PWM). However, other architectures and techniques also exist such as the Sigma Delta Modulation ($\Sigma\Delta$) [25], Pulse Code Modulation (PCM) [26], Pulse Density Modulation (PDM) [6] etc. A quick review for the PWM is given by the following.

2.1.2.1 The Pulse Width Modulation (PWM)

The PWM [27, 28] can be obtained by comparing the audio signal [$20\,Hz$; $20\,kHz$] to a ramp waveform with a higher frequency, as shown in the example of Fig. 2.4. Generally, the carrier which is a double-sided sawtooth has a frequency at least two times greater than the maximum frequency of the audio frequency band which is $20\,kHz$ [6, 16]. In practical implementations, the carrier frequency is chosen at least ten times greater than $20\,kHz$ for a better audio reconstitution [16]. The switching frequency is then the same as the ramp signal frequency and the pulse widths are modulated according to the audio signal. As a square signal, it has harmonics on the odd multiples of the switching frequency. Thus, the amplifier output spectrum can be described by Fig. 2.5. It contains the audio signal which is illustrated as sinusoidal signal in this figure, the switching frequency and its odd harmonics, in addition to the inter-modulation peaks located around each harmonic. The PWM spectrum components have been deeply studied in [29, 30]. Moreover, additional information concerning the carrier and it's influence on the spectral content of a PWM can be found in [6].

A basic amplifier architecture is shown in Fig. 2.6. The architecture is composed by a comparator that generates the PWM signal according to the ramp and the audio signals. The pulse train is then amplified by the power stage to drive the load. As a nonlinear device, the Class-D amplifier introduces a high amount of distortion

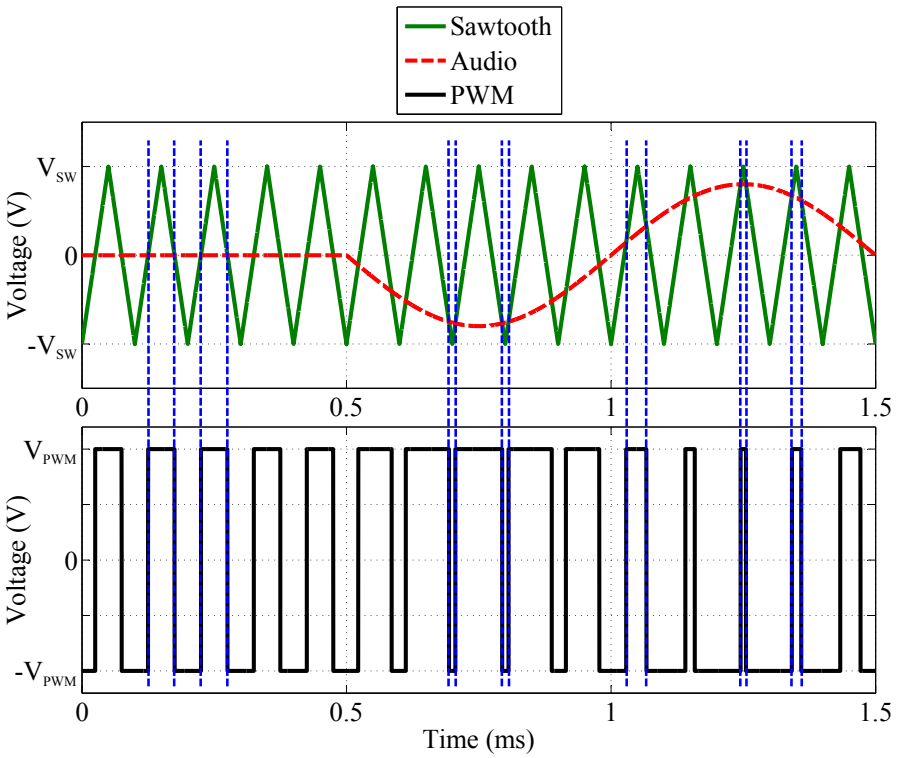


FIGURE 2.4: PWM modulation.

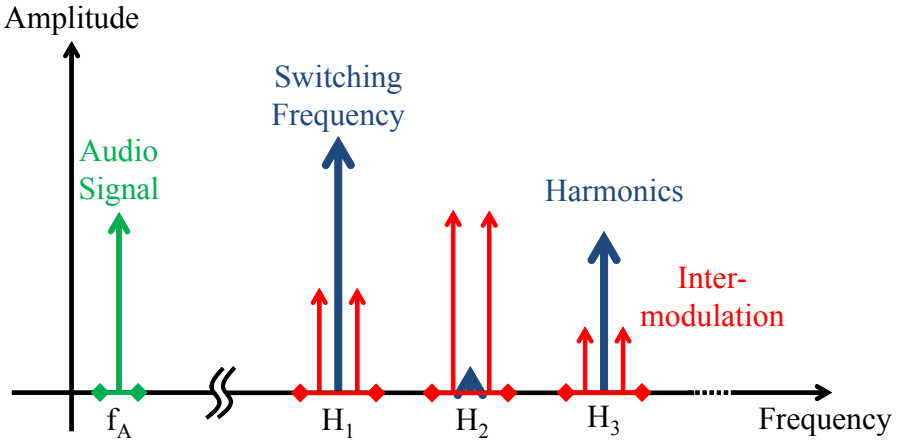


FIGURE 2.5: Spectrum of a PWM signal.

due to the modulation errors, the power switching and others. Moreover, gain variations can occur in case of unstable supply voltage (for example, a battery at different state of charge). Therefore, most of the time a feedback loop is introduced in order to reduce these errors and produce a better audio restitution.

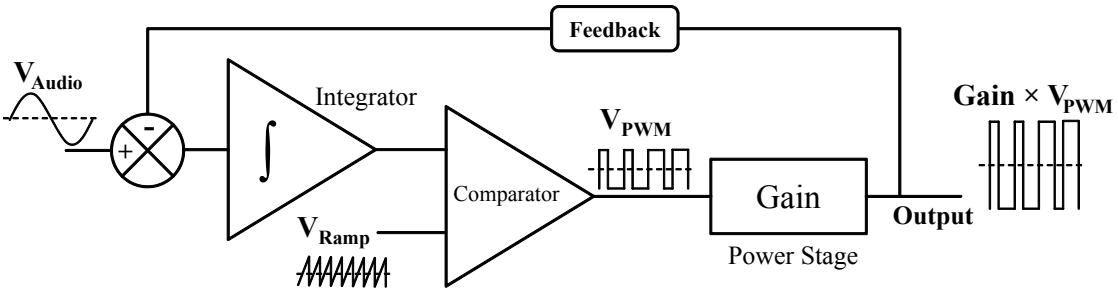


FIGURE 2.6: Basic architecture of a Class-D amplifier [24].

2.1.2.2 PWM for differential Class-D amplifiers

In the case of a differential power stage, an additional modulation feature can be included. The power stage can switch according to a binary or a ternary modulation. Considering an ideal power stage, a description is given by the following.

Binary modulation: The binary modulation [16, 31] is obtained when the two switching cells of an H-Bridge are switching with complementary values ($0\,V$ and V_S). Thus, they switch at the same time as shown in Fig. 2.7. Two modes exist in the case of a differential topology, the first is the Common Mode (CM) which is given by equation (2.1). The second is the Differential Mode (DM) which is given by equation (2.2).

$$V_{CM} = \frac{V_{PLUS} + V_{MINUS}}{2} \tag{2.1}$$

$$V_{DM} = V_{PLUS} - V_{MINUS} \tag{2.2}$$

The output signal which is the same as the DM voltage, keeps the same shape as the original single switch PWM, but it doubles the amplitude by switching between V_S and $-V_S$. The output spectrum is then the same as the one shown in Fig. 2.5, but with double the amplitudes. The CM which is the common voltage referring to the ground, is a DC voltage which is an advantage in term of EMC.

Note that, this architecture presents a major drawback and it is highlighted as follow. In the case of zero audio signal, as can be seen between $0\,ms$ and $0.5\,ms$ in Fig. 2.7, the differential voltage keep switching with $50\,\%$ duty cycle corresponding to a $0\,V$ mean value. Thus, the current in the load is not zero even if the audio

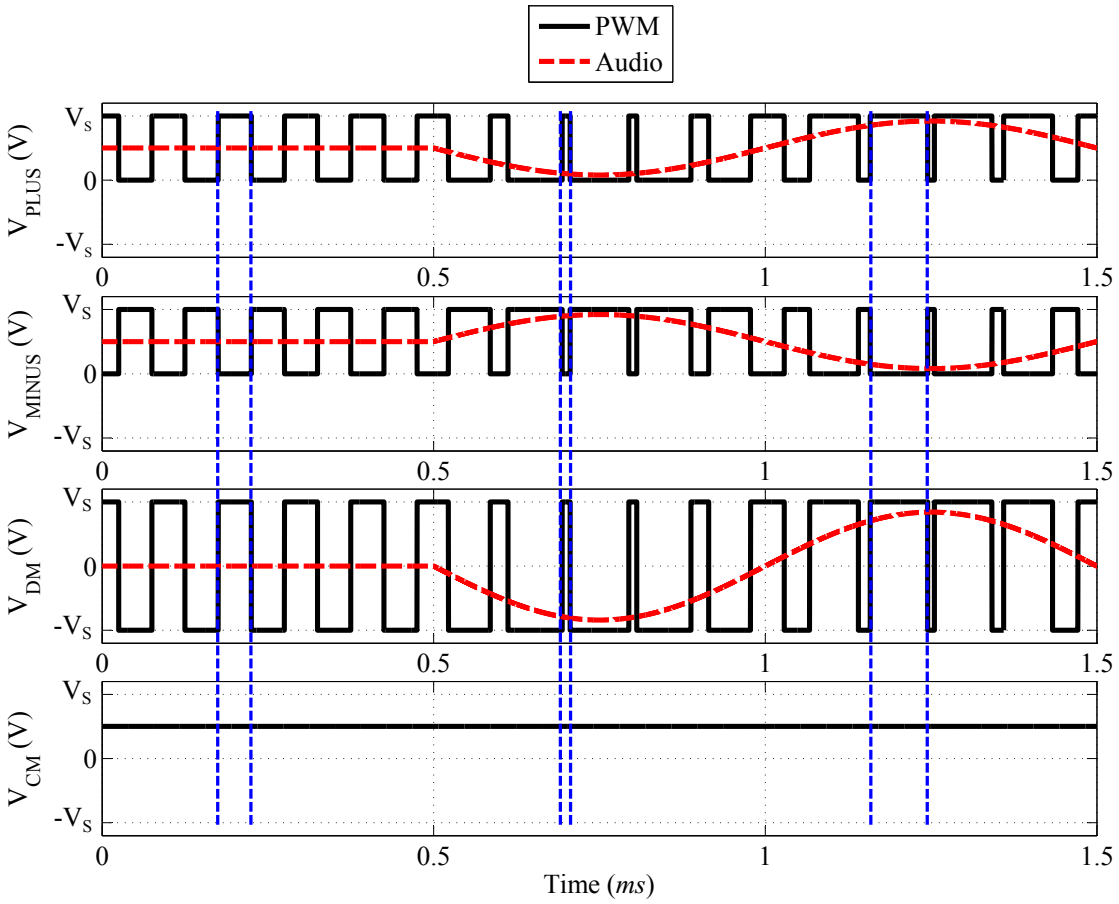


FIGURE 2.7: H-Bridge binary modulation.

signal is equal to zero. Note as well that, for this type of modulation the output voltage or V_{DM} switch with a step of $2 \times V_S$.

Ternary modulation: The ternary modulation [16, 31] is obtained when the two switching cells of an H-Bridge switch at different time as shown in Fig. 2.8. On the first hand, the differential output voltage or V_{DM}, switch between the three available levels: V_S, $0\,V$ and $-V_S$. In this case, two pulses appear on each switching period of the original carrier, which doubles the switching frequency across the load. It implies in the frequency domain a cancellation of the odd harmonics, including their inter-modulations. The output voltage spectrum can be then expressed by Fig. 2.9. On the second hand, the common mode voltage or V_{CM} keeps switching with and without audio signal which is a negative point in term of EMC. However, this topology allows us to have a zero differential output signal in the case of a zero audio input signal. It is highlighted in Fig. 2.8 between

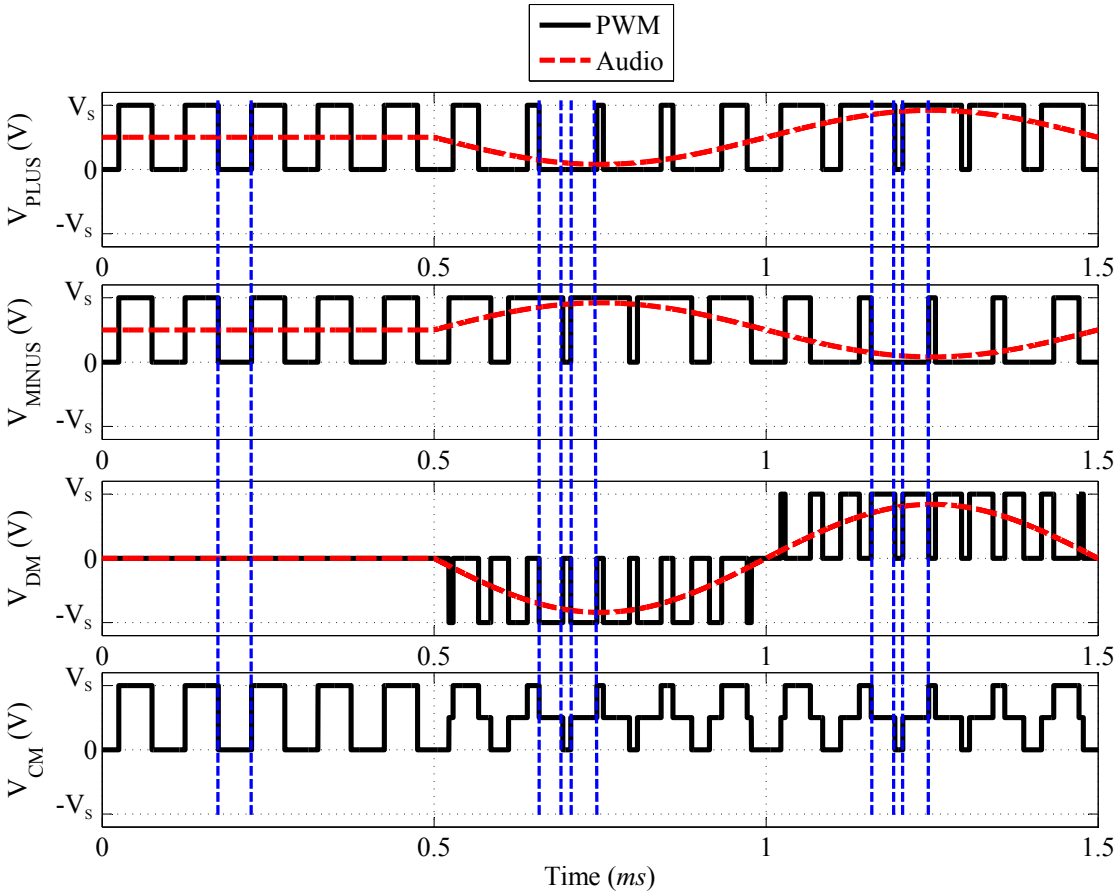


FIGURE 2.8: H-Bridge ternary modulation.

$0\,ms$ and $0.5\,ms$. In addition, the output voltage have a switching step equal to V_S.

As a conclusion, the ternary architecture presents many advantages comparing to the binary architecture. It allows us (i) to remove the odd harmonic in the output spectrum, (ii) to have a zero current in the load in case of a zero audio signal and (iii) to have a low switching step in the output voltage. Therefore, it can be more often found among commercial integrated Class-D amplifiers. Fig. 2.10 shows two architecture examples of a differential Class-D amplifier having a binary and a ternary modulation [27].

2.1.2.3 Self oscillating modulation

The modulation techniques mentioned earlier are not the only existing techniques. By using a closed loop, it is also possible to generate a modulated pulse stream. These techniques can appear under several names such as the self oscillating,

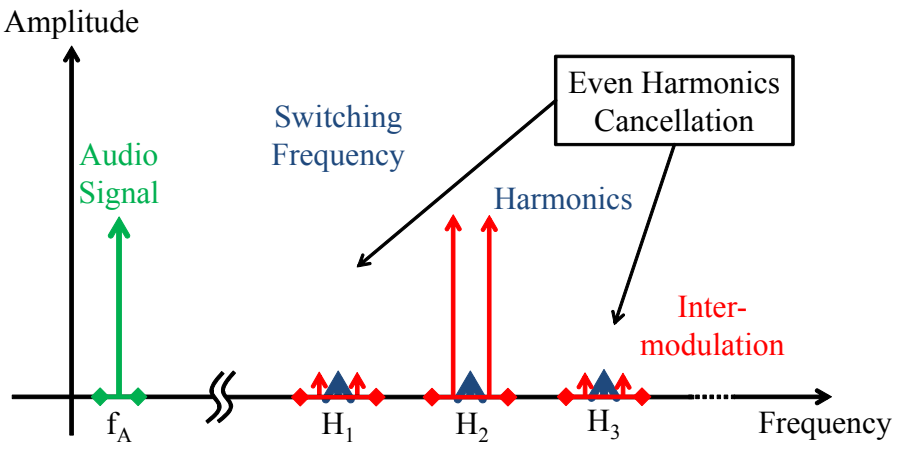


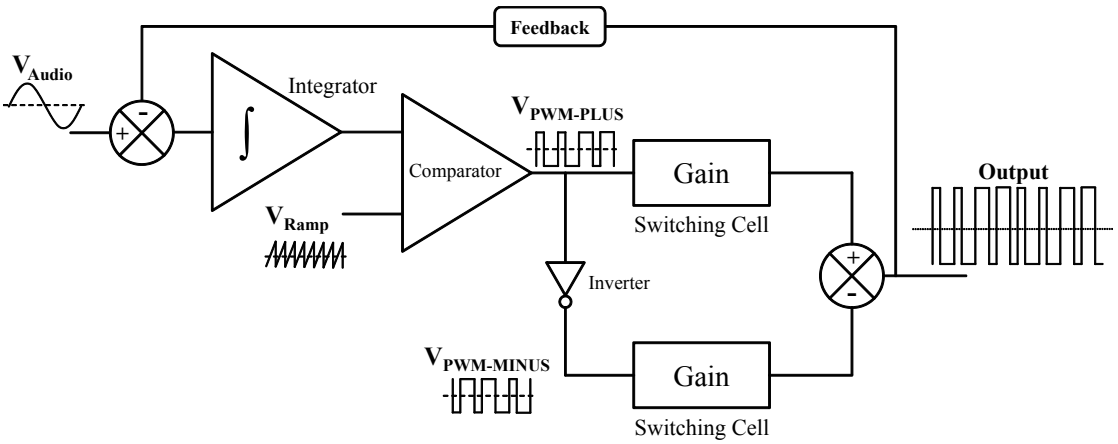
FIGURE 2.9: Ternary modulation output spectrum.

the sliding mode or the bang-bang control. Some of the basics are given in the following:

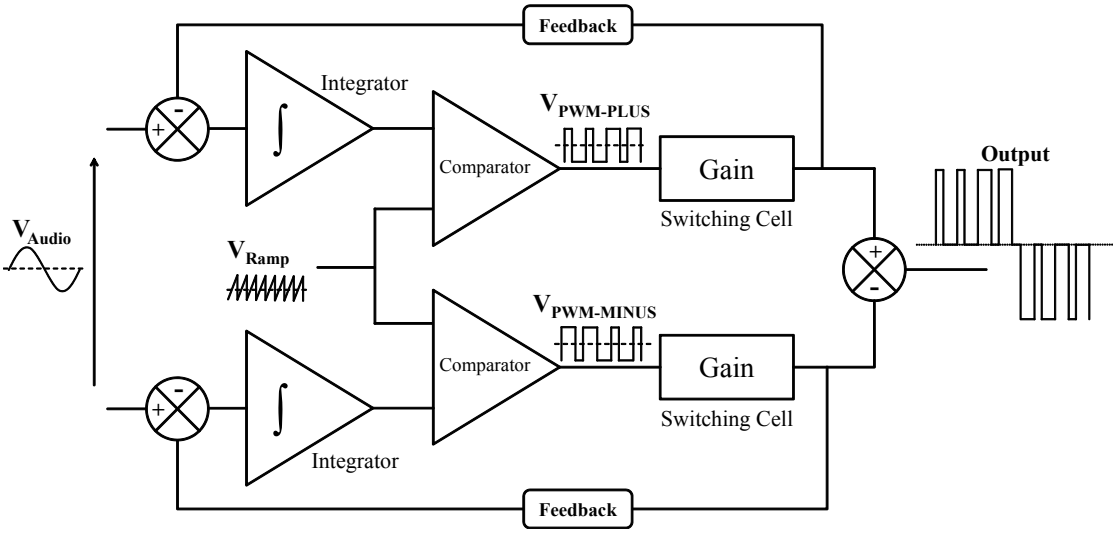
The self oscillating modulation [7, 32, 33] can be obtained by creating an unstable feedback loop that force the system to oscillate. A basic architecture is given in Fig. 2.11. The error signal which is the difference between the input and the output signals is integrated and injected into an hysteresis trigger. By a comparison to $0\,V$, the pulse train is obtained then amplified by the power stage to finally be fed to the speaker.

In such architecture, the switching frequency is dependent from the input signal level. Therefore, for an audio input, the switching frequency keep changing systematically [32] which creates a spread spectrum phenomenon. This allows us to reduce the harmonic power and spread it around the central switching frequency. This is the main advantage of such modulation which lead to some peak reduction, thus, to a certain amount of EMI reduction [34]. The output spectrum can be then described by Fig. 2.12.

Self oscillating techniques can also be used with differential power stages. Thus, generate a binary or a ternary modulation. However, this issue is not developed for conciseness.



(a) Binary modulation



(b) Ternary modulation

FIGURE 2.10: Architecture of a differential Class-D amplifier.

2.2 EM emission of Class-D amplifiers

The switching nature of a Class-D amplifier provides an important advantage, which is the power efficiency. However, the switching behavior is also the source of EMI generated by such an amplifier.

2.2.1 EMI at the output rails

Fig. 2.13 shows the frequency content at the output of a Class-D amplifier. The frequency characteristics of a square signal (Fig. 2.13(a)) contains in the frequency domain (Fig. 2.13(b)) harmonics located on the odd multiples of the switching

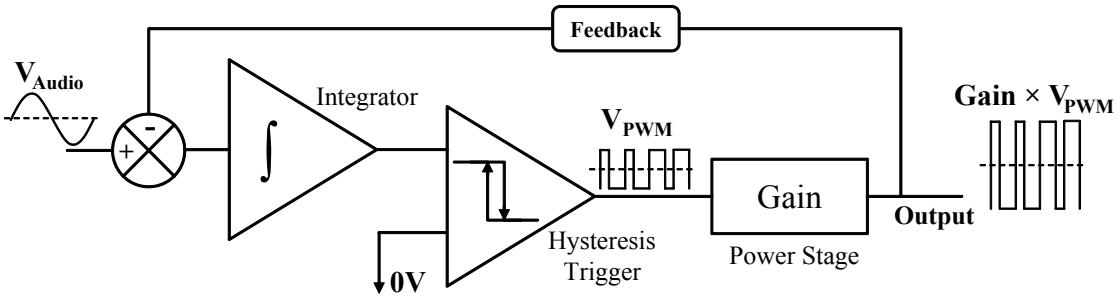


FIGURE 2.11: Basic architecture of a self oscillating Class-D amplifier.

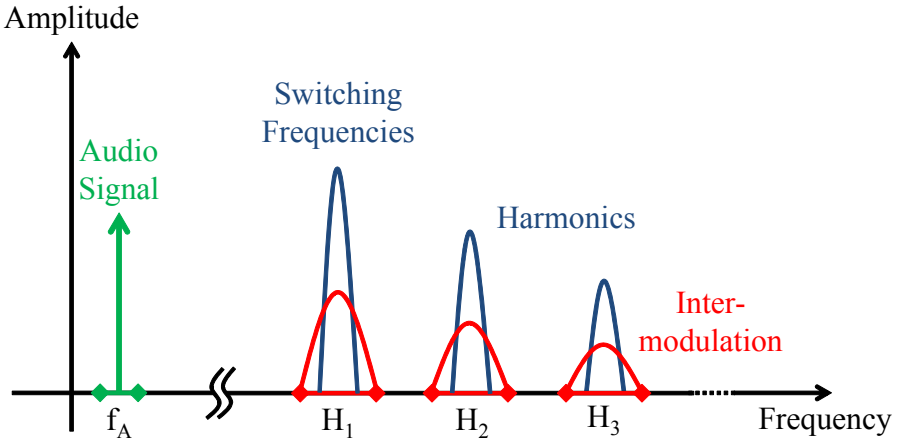


FIGURE 2.12: Self oscillating Class-D amplifier output spectrum.

frequency. These harmonics decrease by a negative slope equal to $-20\,dB/decade$. A real voltage waveform has a certain non-zero rise and fall time [35]. It is then a better approximation to consider the pulse stream as a trapezoidal waveform (Fig. 2.13(c)). This latter presents as well odd harmonics over the frequency band (Fig. 2.13(d)), similar to the case of a square waveform. However, in the case of trapezoidal waveform, the harmonics decrease by a slope of $-40\,dB/decade$ after a corner frequency. If the rise and fall time are equal and called τ_r, the corner frequency can be calculated by equation (2.3).

$$f_c = \frac{1}{\pi\tau_r} \tag{2.3}$$

A switching electronic system contains many parasitic components that can be modeled as inductors and capacitors. These are due to the chip bondings, to the connectors, and many others. Mixing these parasitic components with the high $dv(t)/dt$ of the pulse switching, creates ringings and overshoots on each switching transition of the pulse stream (Fig. 2.13(e)). Indeed, it has an impact on the shape of the frequency spectrum as shown in Fig. 2.13(f).

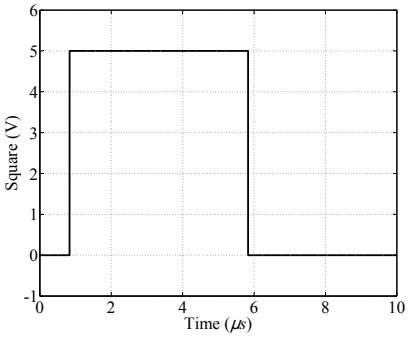
Finally, in the case of a Class-D amplifier, the duty cycle of the square signal is modulated according to the audio signal (Fig. 2.13(g)). Thus, additional peaks appear in the frequency spectrum (Fig. 2.13(h)) which correspond to the inter-modulation (also called side bands) between the carrier and the audio signal.

A Class-D amplifier generates a pulse stream that combines all the above features. In addition, many other features such as the MOSFET body diodes, switching dead time, disparity among component properties and component nonlinearities, etc., affect directly the output signal. Thus, a Class-D amplifier which mix the high power delivery with the complex output spectrum, appear to be a serious source of EM emissions.

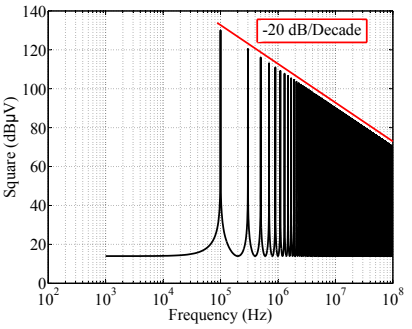
Often, in electronic applications, the Class-D amplifier is placed distant from the speaker load. Thus, the long cables or PCB tracks used for connecting these two, are problematic in EMC. The conducted noise that propagates through long conductors and interfere with the surrounding electronics by inductive or capacitive coupling. Also, if the conductors are sufficiently long they behave as antennas. In this case, the EM emissions propagates in the atmosphere and provoke radiated emissions.

2.2.2 EMI at the supply rails

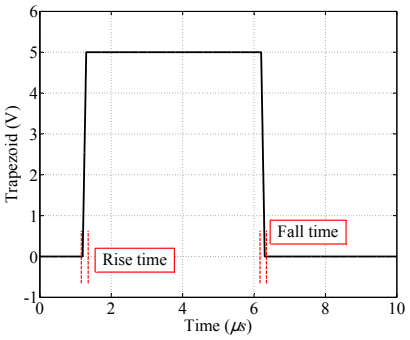
In embedded and portable devices, batteries are the main power supply for the entire device, notably the Class-D amplifier. Because of the parasitic components combined with the power stage switching and other phenomena such as the bus pumping [24] ; some of the perturbations leak to the supply bus. Hence, the voltage variations and the noise generated at the battery level, can disturb other circuits in the embedded system by common impedance coupling. Although, if the battery connections are long, the above stated couplings, crosstalk and radiations can occur. Thus, the Class-D amplifier is not a source of EMI only at the output side, but also at the supply side. This phenomenon exists as well in the case of power converters such as DC to DC converters and it is illustrated in Fig. 2.14.



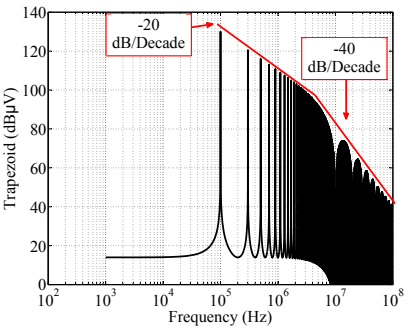
(a) Square signal in the time domain



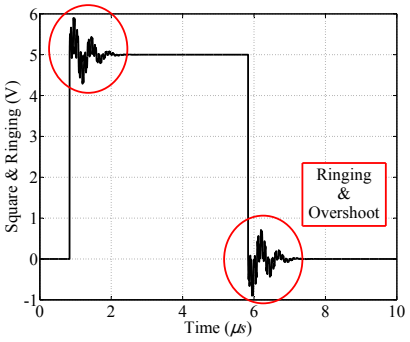
(b) Square signal in the frequency domain



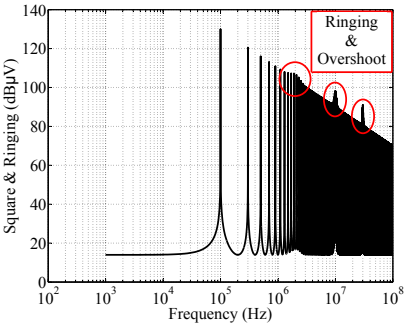
(c) Trapezoid signal in the time domain



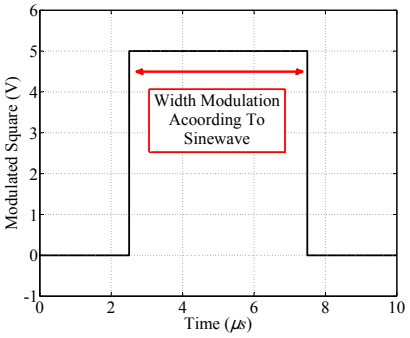
(d) Trapezoid signal in the frequency domain



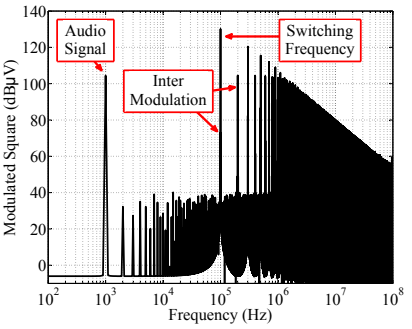
(e) Square signal with ringing in the time domain



(f) Square signal with ringing in the frequency domain



(g) Modulated square in the time domain



(h) Modulated square in the frequency domain

FIGURE 2.13: Frequency content of a Class-D amplifier

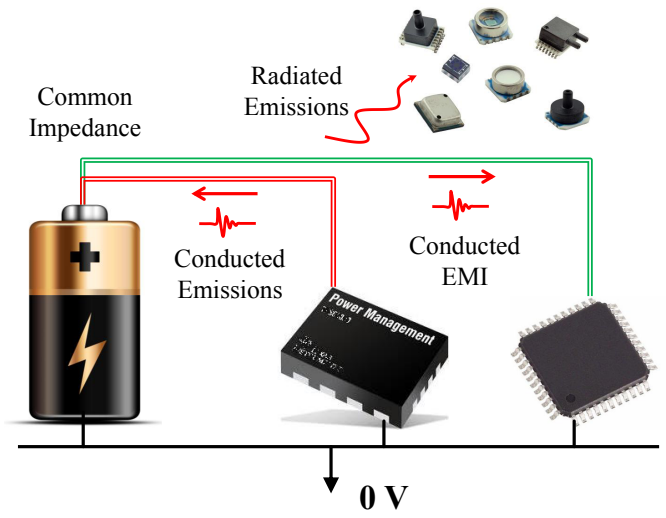


FIGURE 2.14: EMI emissions at the supply level.

2.2.3 EMC solutions

Class-D amplifiers are a serious source of EM emissions which is a crucial problem. Therefore, reducing their emissions has been one of the main interest of electronics designers for many years. For this purpose, numerous circuit design solutions have been created. A quick review is given by the following.

One of the most adopted techniques in power electronics is to control the switching transitions of the power stage [11, 36]. As can be seen from Fig. 2.13(c) and Fig. 2.13(d), the rise and the fall time of the trapezoidal waveform are in a direct relation with the frequency content of their spectrum. The more the rise/fall time is long (slow), the more the corner frequency is low and vise versa. Thus, for $f > \frac{1}{\pi\tau_r}$, a trapezoidal waveform with a long rise/fall time has a frequency spectral content which is lower than the one with a short rise/fall time [37]. This technique is cheep and simple to implement. However, a slow switching time increases the switching losses, thus, a trade-off must be made between the power efficiency and the EMI.

Spread spectrum or dithering, is another technique widely used in power electronics, in particular Class-D amplifiers [8, 38]. As described in section 2.1.2, by creating a random or a quasi-random switching frequency, the noise energy is spread around a central frequency, instead of being localized on a single one. This lead to a reduction of the peaks in the frequency spectra, thus, the reduction of

the EMI. The main drawback of this technique is the negative impact on the audio quality.

Recently, there has been a considerable interest in developing the active filtering technique [39–41]. The idea behind it is to sense the generated noise, then subtract it from the desired signal. This is an effective technique to reduce the EMI. However, it increases the complexity of the system control as well as the power losses of the converter.

The Multi-Carrier Modulation (MCM) [42, 43] is a technique where the audio signal is modulated twice, by two different carriers having two different frequencies. Two PWM signals are obtained, then combined by a logic circuit to deduce a single pulse stream. This latter has a frequency spectral content lower than the one of a single carrier, because the energy is split in two spectral components. This technique drawbacks are the reduced audio quality, the additional power losses and the additional inter-modulation peaks.

The most used EMI suppression method is the passive filtering [3, 12]. Even with the above presented techniques, most of the time, the passive filtering is unavoidable. Many different forms of passive filters exist such as the classical first, second or third order LC filters, the decoupling capacitors, the ferrite beads, the coupled inductors etc. Indeed, they have also a negative impact on the system performance like the audio quality degradation in case of nonlinear behavior [44], or the increase of power losses. However, it is still the most used technique to reduce the EMI.

Circuit design solutions are widely described in the literature as discussed earlier. Each different solution has been theoretically studied and practicably implemented several times. The advantages were highlighted and the disadvantages were discussed and some of them are improved. However, by the author best knowledge, apart [45] no studies in the literature are directly involved in improving the passive environment of a Class-D amplifier, in particular the EMI filters which are the most common EMI suppression methods. Accordingly, this will be the main focus of the present work.

2.3 Characterizing a Class-D amplifier

Eventually, apart the EMC and power efficiency, there exists many criteria in order to evaluate a Class-D amplifier. Some of them are used to evaluate the amplifier power characteristics, some others are used to evaluate the amplifier audio performance in the audio frequency band. Table 2.1 gives important orders of magnitude and few definitions are given in appendix A. Furthermore, more information about characterizing and evaluating a Class-D amplifier can be found in [46].

TABLE 2.1: Order of magnitude for Class-D audio amplifiers [17, 47, 48]

Magnitude	**[Unit]**	**Minimum value**	**Maximum value**
Output power	[W]	0.5	300
Power efficiency at full scale	[%]	80	97
Supply voltage	[V]	2.5	100
Audio frequency	[Hz]	20	24000
Switching frequency	[kHz]	100	3000
Switching Rise/Fall time	[ns]	5	50
Load resistance	[Ω]	2	64
Total Harmonic Distortion	[dB]	50	90
Signal to Noise Ratio	[dB]	80	110
Power Supply Rejection Ratio	[dB]	60	110
Silicon area	[mm^2]	0.1	10
Chip price (PCB not included)	[$]	0.1	15
EMI filter price	[$]	0.5	10

2.4 Summary

To sum up, this chapter has discussed two main axes regarding a Class-D amplifier, the basic concepts and the EMI. First, it has been shown that a these amplifiers are constituted of two main parts which are the modulation and the power stage. The modulation generates a pulse train which is used to drive the switching of the power stage. The latter is composed of power switches that operates as fully on or fully off. This concept allows us to reduce significantly to power losses of the amplifier, thus, obtain a high power efficiency compared to the other amplifier types. Second, it has been shown that the power switching is a major drawback

from the EMC point of view. Thus, Class-D amplifiers are a serious source of EM emissions and can be problematic in many embedded applications.

According to the state of the art, the EMI of Class-D amplifiers is big a concern for electronic engineers. They developed numerous methods and techniques that reduce the emissions of these amplifiers. Fine results have been obtained, however, in industrial applications these techniques are not enough due to the severity of the EMI standards and the complexity of modern electronics. Therefore, EMI filters are always needed to ensure the EMC of Class-D amplifiers.

High performance EMI filters can be obtained by considering the Class-D amplifier in the final application. However, due to the lack of tools, the most common way to do that is the experimental tests on the final application. This procedure is not optimal as it consumes too much time and money. Therefore, next chapter develop an EMI modeling method that helps the system integrators design the EMI filters according to the final application while using simulations.

Chapter 3

EMI Modeling of Class-D Audio Amplifier

The simulation is one of the ultimate tools that allows the electronic designers understand the physics and predict the performance of their design in the real world. The key of making the right simulation is simply choosing the right model. In our case, the model must be able to provide information about the spectral content of a Class-D amplifier, in order to design the right passive environment of the Class-D amplifier chip. To do so, this chapter aims then to to find the most adapted technique for Class-D amplifier modeling. Therefore, the solutions that seem to be adapted for this study are, whether the time domain simulations followed by a Fast Fourier Transform (FFT), whether the frequency domain macro-modeling.

3.1 Time domain simulations

It has been shown over the years that the transient time domain simulations are an effective and reliable tool for all types of electronic needs. In [49], the measurement is used to perform an accurate modeling of a buck converter prototype. A high level of details in parasitic components modeling have been included in order to obtain satisfactory results on the entire conducted emission frequency band. In [50], a detailed model of the electric machine based on geometry information have been made. In [51], the switch of a power converter has been decomposed into several time slots, then modeled by different transfer functions. In [52] the

Partial Element Equivalent Circuit (PEEC) modeling method has been used to extract the parasitic elements of the PCB of a DC-DC converter. The model is implemented in a transient simulation in order to forecast the EM emission. Transient simulations have been also applied in [45] in order to study the EM environment of the Class-D amplifier.

As can be seen, transient time domain simulations are widely used for EMI prediction. However, it cannot be used in our case for many different reasons. First, to obtain a good accuracy at high frequencies, the model must be minutely built. It must include all the parasitic components of the circuit, including those of the imperfect electric units, those of the IC packaging, those of the imperfect conductors and connectors, those of the physical architecture of the system, etc. This can be a long process, especially for designing the passive environment of the amplifier. For each different implementation the passive environment is different and the modeling process must start all over again. Second, one transient simulation can take a very long time which depend usually on the modeling complexity and details. One simulation can take hours, days or even weeks. In the present study, this can be problematic because designing the passive environment might need numerous retake to be accomplished. Third, and from the company point of view, these models cannot be provided to the costumers because of confidentiality reasons. Therefore, it is then more adequate to adopt the frequency macro-modeling technique which will be discussed in the next section.

3.2 Frequency domain modeling

According to our best knowledge the frequency domain modeling has never been applied for any Class-D amplifier system. Therefore, the state of the art presented in this subsection refers to other types of power converters.

In [53] the authors have used two models in the frequency domain composed of lumped components distribution, in order to predict the resonance effect present in the CM noise of a Switched Mode Power Supply (SMPS). This approach will be more complicated if applied on a complex spectral content containing several resonances. In addition, it deals only with the CM noise.

Generally, S (scattering matrix) or Z (impedance matrix) parameters are an interesting tool to create EMI models. If they are correctly determined, it is possible

to achieve a high level of accuracy at high frequencies. References [54, 55] deal with the S-parameters in order to study the performance or the insertion loss of a multi-phase EMI filter. However, in those papers, only a single part of the system is studied which is not optimal as the EMI behavior of a system highly depends on the load impedance and the source emissions. These issues can also be found in [56] where the authors modeled the multi-layer PCB tracks using S and Z parameters in order to study the mode conversion on differential lines.

The article [57] models a multi-conductor cable in order to study the conducted emissions in a propagation path. The distributed parameter circuit model has been adopted in order to create two separate models for the CM and the DM. Afterworlds, the transfer function is used to evaluate the EMI at the load. Some differences can be seen between the experimental and the simulated results. This can be due to the mode conversion which is not taken into account in this approach.

Another model has been presented in [58, 59]. The model consists of two current sources and three impedances to describe the entire system. To determine the five parameters of the model, five equations are needed. Thus, different measurements on different operating conditions are made and the parameters are extracted. Such method has a high level of abstraction and can be interesting to make system level simulations. However, it is less interesting in our case where the main interest is to design the passive environment of the system itself.

In [60] an electric-vehicle-drive system have been modeled using the admittance measurements. Interesting results have been obtained, however, only a CM current calculation is possible. In addition several symmetry approximations have been taken in order to built the model.

An interesting modeling approach was developed in [61, 62] and it has been re-utilized in [63]. It allows to bring out the importance of the coupling paths and study the influence of each sub-system part on the EMI efficiency. Using 2×2 impedance matrices, the different parts of the system were modeled. Hereafter, the common mode currents have been computed and compared to the measurements. Accurate results are shown up to $10\,MHz$. This approach has been also reused in [64, 65]. The authors have increased the matrix dimensions and tried to increase the accuracy. However, the major drawback of these works is still the accuracy at high frequencies and they are only able to study the CM.

The authors in [66] have created a model to compare a balanced and an unbalanced architectures of data transmission on the power line network of spacecraft. The model allows to evaluate the signal transfer function of the data transmission over the frequency band. However, several assumptions have been considered for the sake of simplicity. For example the DC-DC converter input filter has been assumed as two ideal inductances. This can be problematic when studying the EMC because it reduces the accuracy at high frequencies. In addition, only the CM study has been carried out as it contributes mainly to the radiated emissions.

By considering the needs of this study, the modeling approach should meet the following specifications.

1. Accurate at high frequencies, especially in the conducted EMI frequency band.
2. Can be applied on a single-ended or a differential Class-D amplifier.
3. Take into account the DM, the CM and the mode conversion.
4. Bring out the different coupling paths of the system.
5. Can be used at the design stage.
6. Has a fast simulation time.

Thus, none of the above approaches meet the requirements for Class-D amplifiers. Additionally, on each different case in the state of the art, approximations have been taken in order to simplify the model and treat one particular case. Moreover, the articles [60–62, 64, 65] were only using measurements on a prototype which make them less usable at the early design stage. Therefore, next section proposes a new modeling approach that fuse the advantages of the different methods presented earlier.

3.3 Proposed frequency domain modeling

The proposed method is described for systems with N active conductors. The considered power system is segmented into functional sub-circuits which are called blocks. The system is represented by a chain of blocks as shown in Fig. 3.1. In this

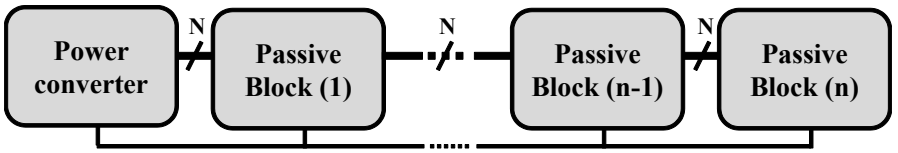


FIGURE 3.1: System decomposition into blocks.

chain, on the one hand there are the active blocks, such as switching amplifiers, power converters, etc. On the other hand, there are the passive blocks such as filter, load, tracks, etc. Note that passive blocks can also be divided into several blocks if needed. This will help improve the design of a given system part, such as filter and PCB layout. However, the below requirements must be verified before any usage of this method:

- No feedback control for the converter coming from the following passive blocks. In the opposite case, output voltages are dependent on the passive circuit which makes the model invalid.
- No significant electromagnetic coupling between blocks. A block impedance matrix is independent from the other blocks. In other words, the block behavior do not change after segmentation.
- Block should be sufficiently short to be considered electrically short (block dimensions $\ll$ wavelength).
- Passive components are used in their linear operating range.

3.3.1 Active blocks model

Active blocks with N active conductors can be modeled with N electric sources and a $2N \times 2N$ impedance matrix as shown in Fig. 3.2. Determining the electric sources and the output impedance matrix cannot be generalized. Each particular circuit has its dedicated set of measurements. Many measurement possibilities can be imagined, such as: open circuit (if possible), loaded, open circuit when loading other ports, etc. Otherwise, a quick review on the noise source impedance extraction is given below.

Some interesting examples of internal impedance extraction of power converters or integrated circuits (IC) can be found in [67–73]. In [67, 68] the presented

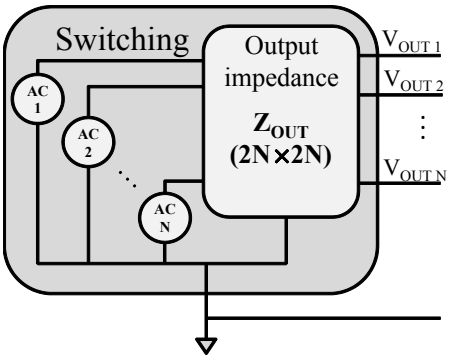


FIGURE 3.2: Active block model.

approach allows us to measure the noise source impedance of an SMPS under operating conditions. The method consist in using two current probes. The first is used to inject a continuous wave with a sweeping frequency and the second is connected to a Vector Network Analyzer (VNA) and used to sense the resultant current in the circuit. Using the voltage image of the current injection and the measured current, it is possible to compute the unknown impedance of the SMPS.

In [69–71] the authors present the Integrated Circuit Electromagnetic Model (ICEM). The model consists of a Power Distribution Network (PDN) and a current noise source. The method starts by measuring the PDN of an IC using a VNA. The PDN is the passive network that connect the different supply and ground pins of the IC. Afterwards, a Resistance, Inductance, Capacitance (RLC) model, equivalent to the PDN is created by fitting. Finally, thanks to the PDN and the current measurement on the IC pin, the internal current noise source is computed.

The authors in [72] propose to make three different measurements of the noise source with three different loading conditions. These allows us to have three different equations which allows the computation of the noise source as well as the real and the imaginary parts of the noise source impedance.

3.3.2 Passive block types and models

Passive blocks are modeled by impedance matrices relating voltages to currents. Two types of blocks can be distinguished ; for simplification, they will be called *Type A* and *Type B* blocks for the rest of this document. *Type A* is intended for the blocks situated in the middle of the chain and can be connected from both sides with $2N + 1$ ports (N inputs and N outputs, plus a ground) as shown in

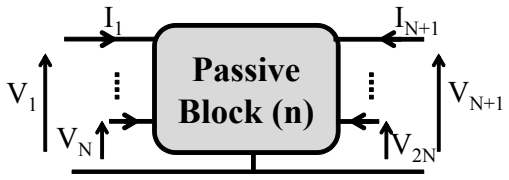


FIGURE 3.3: *Type A* : $2N+1$ ports.

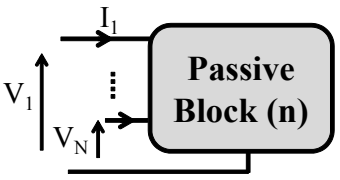


FIGURE 3.4: *Type B* : $N+1$ ports.

Fig. 3.3. *Type B* is intended for blocks situated at the end of the chain and can only be connected from its inputs with $N+1$ ports (Fig. 3.4). More precisely, *Type B* blocks are intended for loads because usually they only have an electrical input, but with other types of physical output (mechanical, thermal and acoustic, etc.).

According to Fig. 3.3, *Type A* blocks have $2N$ voltages and $2N$ currents, so their impedance matrix dimension is $2N \times 2N$ as shown in (3.1).

$$\begin{pmatrix} V_1 \\ \vdots \\ V_{2\,N} \end{pmatrix} = \begin{pmatrix} z_{1\,1} & \cdots & z_{1\,2N} \\ \vdots & \ddots & \vdots \\ z_{2N\,1} & \cdots & z_{2N\,2N} \end{pmatrix} \cdot \begin{pmatrix} I_1 \\ \vdots \\ I_{2N} \end{pmatrix} \tag{3.1}$$

Similar to *Type A* blocks, *Type B* blocks have $N \times N$ impedance matrix because they have N voltages and N currents as shown in (3.2). Note that an impedance matrix of a passive circuit is symmetric with respect to the diagonal due to the reciprocity theorem [74] ($Z_{ij} = Z_{ji}$; $\forall i$; $\forall j$; $i \neq j$).

$$\begin{pmatrix} V_1 \\ \vdots \\ V_N \end{pmatrix} = \begin{pmatrix} z_{1\,1} & \cdots & z_{1\,N} \\ \vdots & \ddots & \vdots \\ z_{N\,1} & \cdots & z_{N\,N} \end{pmatrix} \cdot \begin{pmatrix} I_1 \\ \vdots \\ I_N \end{pmatrix} \tag{3.2}$$

3.3.3 Impedance matrix determination

Impedance matrix determination can be done using several methods and in this work three methods are studied. The first uses measurements with an Impedance Analyzer (IA), the second uses measurements with a VNA and the third uses simulation with Advanced Design System (ADS) program [75].

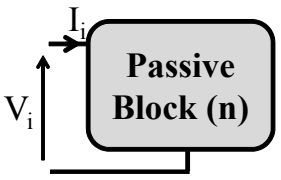


FIGURE 3.5: Z_{ii} measurements.

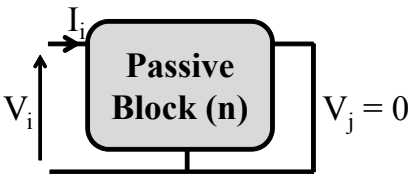


FIGURE 3.6: $Z_{ij_{sc}}$ measurements.

3.3.3.1 Impedance matrix determination by impedance analyzer

Determining an impedance matrix using an IA requires two steps. First of all, diagonal elements are measured. Equation (3.3) and Fig. 3.5 show that z_{ii} is the input impedance of the i port.

$$z_{ii} = \left.\frac{V_i}{I_i}\right|_{I_j=0} \quad ; \quad i \neq j \quad ; \quad j = 1 \ldots (2)N \tag{3.3}$$

In practical term, the IA is connected directly to the i^{th} port to measure z_{ii} when the remaining ports are open circuits ($I_j = 0\,A$; $j \neq i$).

The second step is to measure the off-diagonal elements (z_{ij} ; $i \neq j$). Equation (3.4) shows how to determine the cross elements theoretically.

$$z_{ij} = \left.\frac{V_i}{I_j}\right|_{I_i=0} \quad ; \quad i \neq j \quad ; \quad i = 1 \ldots (2)N \tag{3.4}$$

Nevertheless, it is not possible to apply this in practice with a single port IA and it is delicate to apply with dual-port IA. According to equation (3.4), this method needs a current injection on the j^{th} port and exact voltage amplitude and phase sensing on the i^{th} port with $I_i = 0\,A$. Instead, equation (3.5) gives an alternate user-friendly method for the determination of the cross elements. The proof of (3.5) is given in appendix B.1.

$$z_{ij} = \sqrt{z_{jj}(z_{ii} - z_{ij_{sc}})} \quad ; \quad i \neq j \tag{3.5}$$

Where $z_{ij_{sc}}$ is the impedance measured from the i^{th} port when the j^{th} port is in Short Circuit (SC) (Fig. 3.6), z_{ii} is the i^{th} diagonal element presented by (3.3), z_{ij} is the $i^{th}j^{th}$ element presented in (3.4).

3.3.3.2 Impedance matrix determination by VNA

To determine an impedance matrix of a passive block, first, the scattering matrix is measured. Second, equation (3.6) can be used to convert it to an impedance matrix. More information about this equation and it's application can be found in [76].

$$Z = (I - S)^{-1} \cdot (I + S) \cdot Z_0 \tag{3.6}$$

Z is the impedance matrix, S is the scattering matrix, I is an identity matrix and Z_0 is the characteristic impedance of the VNA (usually 50 Ω).

Note that, a VNA can introduce significant measurement uncertainty. The latter depends on the frequency range, the element type (diagonal or cross element) and the measured impedance level compared to 50 Ω [77–80].

3.3.3.3 Impedance matrix determination by simulation

The advantage of simulation is determining the impedance matrices before construction, so the designer needs to build fewer prototypes. Moreover, the only frequency band limitation is the modeling details, which means the model validity. Otherwise, the band can be chosen by the user. Also, if needed, it is possible to study the influence of the uncertainty and the disparity of the components due to the fabrication procedure [81].

3.3.4 Impedance matrix association

Impedance matrices can be associated in order to obtain one resulting matrix, containing their impedance behavior seen by the converter as shown in Fig. 3.7. The latter shows that there are two types of association. On the one hand, there is the *Type A + Type A* association, and on the other hand, there is the *Type A + Type B* association.

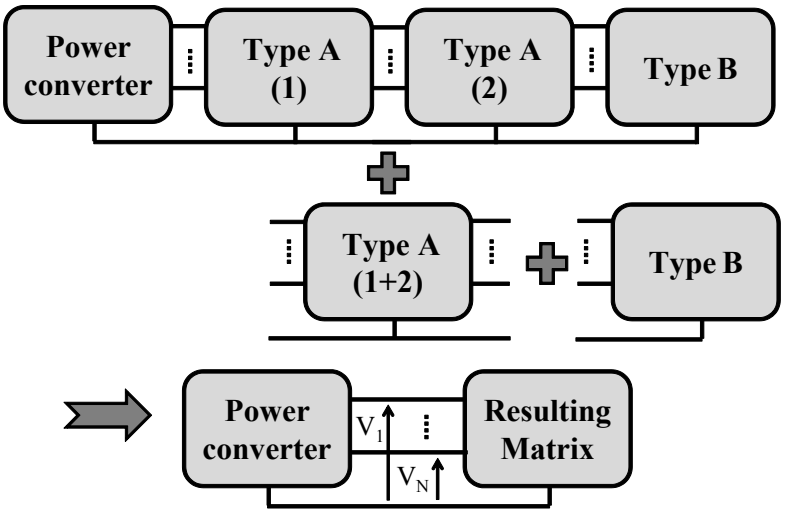


FIGURE 3.7: Block association technique.

3.3.4.1 Association of 2 *Type A* blocks

Two *Type A* blocks are considered to describe this association: The first called k with an impedance matrix Z_k and the second called m with an impedance matrix Z_m. Z_k and Z_m are divided into 4 sub-matrices having the same dimensions $(N \times N)$ as shown in (3.7).

$$Z_k = \left(\begin{array}{c|c} Z_{k11} & Z_{k12} \\ \hline Z_{k21} & Z_{k22} \end{array}\right) \quad ; \quad Z_m = \left(\begin{array}{c|c} Z_{m11} & Z_{m12} \\ \hline Z_{m21} & Z_{m22} \end{array}\right) \tag{3.7}$$

Then, equation (3.8) gives the association method. Note that, the proof of this equation is given in appendix B.2.

$$Z_{km} = \begin{pmatrix} Z_{km11} & Z_{km12} \\ Z_{km21} & Z_{km22} \end{pmatrix} \tag{3.8}$$

with :

$Z_{km11} = Z_{k11} - Z_{k12}(Z_{k22} + Z_{m11})^{-1} Z_{k21}$

$Z_{km12} = Z_{k12}(Z_{k22} + Z_{m11})^{-1} Z_{m12}$

$Z_{km21} = Z_{m21}(Z_{k22} + Z_{m11})^{-1} Z_{k21}$

$Z_{km22} = Z_{m22} - Z_{m21}(Z_{k22} + Z_{m11})^{-1} Z_{m12}$

It is also possible to use the transfer matrix T (matrix that gives the output voltages and currents in terms of the input voltages and currents) for this association. However, it is not used in this work because it add two extra calculation steps which are the Z $\rightarrow$ T and T $\rightarrow$ Z matrix conversions.

3.3.4.2 *Type A* and *Type B* blocks association

To explain how to associate a *Type A* and a *Type B* blocks, we consider first the km block (*Type A* with a $2N \times 2N$ dimension) presented earlier and which is modeled by the impedance matrix Z_{km}. Second, the load block which is modeled by the impedance matrix Z_L (*Type B* with a $N \times N$ dimension). If Z_{kmL} is the resulting impedance matrix, it can be calculated with equation (3.9). Note that the proof of this equation can be found in appendix B.3. The resulting Z_{kmL} is a $N \times N$ impedance matrix.

$$Z_{kmL} = Z_{km\,1\,1} - Z_{km\,1\,2}(Z_L + Z_{km\,2\,2})^{-1} Z_{km\,2\,1} \tag{3.9}$$

In the resulting matrix Z_{kmL}, the diagonal elements $(Z_{ii}; i = 1 \dots N)$ represent the input impedance of the passive blocks seen by the converter. The cross elements $(Z_{ij}\ ;\ i \neq j\ ;\ i = 1 \dots N\ ;\ j = 1 \dots N)$ represent the couplings between the active conductor through the passive system.

3.3.5 Currents and voltages computation

Using the converter model, the *Type A* impedance matrices $(2N \times 2N)$, the *Type B* impedance matrix $(N \times N)$ and the resulting impedance matrix $(N \times N)$, it is possible to compute the currents and voltages at all the system nodes.

First, we start by explaining how to compute the current spectra at the converter output. Fig. 3.8 illustrates this case. After associating all the matrices of the passive blocks, one single impedance matrix called Z_R $(N \times N)$ is obtained. This matrix is a compact model replacing all the passive blocks in terms of impedance seen by the converter. Knowing the output voltages spectra of the converter, the

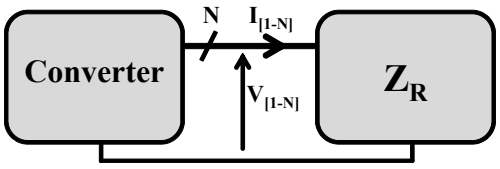


FIGURE 3.8: Current computation at the converter output.

currents spectra can be calculated using equation (3.10).

$$\begin{pmatrix} I_1 \\ \vdots \\ I_N \end{pmatrix} = (Z_R)^{-1} \begin{pmatrix} V_1 \\ \vdots \\ V_N \end{pmatrix} \tag{3.10}$$

Second, we explain how to compute the currents and the voltages at any node in the rest of the system. Fig 3.9 illustrate the case. The chosen node is after the passive block named k. Thus, the matrix $\mathrm{Z}_{[1\to k]}$ $(2N \times 2N)$ is the concatenation of all the *Type A* blocks before the chosen node (see section 3.3.4.1 for concatenation). The passive block $\mathrm{Z}_{[k+1\to n]}$ $(N \times N)$ is the concatenation of all the blocks after the chosen node including the *Type A* and the *Type B* blocks (see section 3.3.4.1 and 3.3.4.2 for concatenation). Therefore, the output voltages ($V_{OUT[1-N]}$) and currents ($I_{OUT[1-N]}$) can be computed using equation (3.11) and (3.12) respectively.

$$\begin{pmatrix} V_{OUT\,1} \\ \vdots \\ V_{OUT\,N} \end{pmatrix} = (I + Z_{[1\to k]22} \cdot Z^{-1}_{[k+1\to n]})^{-1} Z_{[1\to k]21} \cdot Z^{-1}_{[k+1\to n]} \begin{pmatrix} V_{IN\,1} \\ \vdots \\ V_{IN\,N} \end{pmatrix} \tag{3.11}$$

$$\begin{pmatrix} I_{OUT\,1} \\ \vdots \\ I_{OUT\,N} \end{pmatrix} = Z^{-1}_{[k+1\to n]} \begin{pmatrix} V_{OUT\,1} \\ \vdots \\ V_{OUT\,N} \end{pmatrix} \tag{3.12}$$

Where I is a $N \times N$ eye matrix, $Z_{[1\to k]21}$ and $Z_{[1\to k]22}$ are sub-matrices from the $Z_{[1\to k]}$ matrix with a $N \times N$ dimension as explained for equation (3.7) in section 3.3.4.1. Note that, all the computations of this method must be done in the complex form. Note as well that, the proof of equation (3.11) is given in appendix B.4.

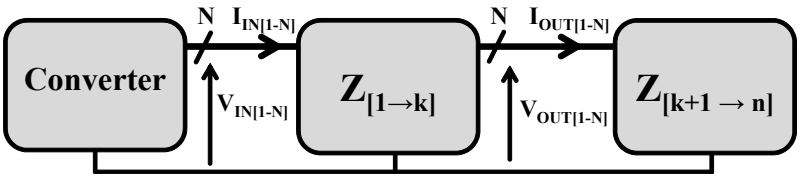


FIGURE 3.9: Currents and voltages computation at a given node after the block named k.

3.4 Experimental application on a Class-D amplifier – *Output side*

The method presented in section 3.3 is applied on a differential Class-D audio amplifier for validation. The chosen amplifier IC is a test chip used in hands-free cell phone applications. It has an H-Bridge power stage controlled by PWM. The maximum output power is $700\,mW$, the supply voltage is $3.6\,V$ similar to the one of a cellphone battery and the switching frequency is $412\,kHz$. In real applications, this amplifier is followed by a passive filter, then a loudspeaker (the load). Note that, this type of amplifiers does not need a filter to reconstitute the audio signal due to the inductive nature of the micro-speakers [82, 83], also because the switching harmonics are outside the audio frequency band. Nevertheless, a filter is only needed for EMC reasons.

The chosen filter is a common structure for Class-D amplifiers and presented in [84]. The filter schematic is shown in Fig. 3.10 and the filter component values are given in Table 3.1.

Two different loads were studied; the first is a loudspeaker used in cell phone applications [85], and the second is a dummy load (Fig. 3.11) that emulates the real speaker. However, for simplicity only the dummy load is used for the rest of this work. The dummy load contains two coils of $15\,\mu H$ and an $8\,\Omega$ resistor (Table 3.2).

The three system parts are mounted on separate printed circuit boards, equipped with SMB connectors for an easy association/disassociation by a simple plug/unplug. Moreover, the boards are designed for an easy currents and voltages sensing on the filter and load inputs as shown in Fig. 3.12.

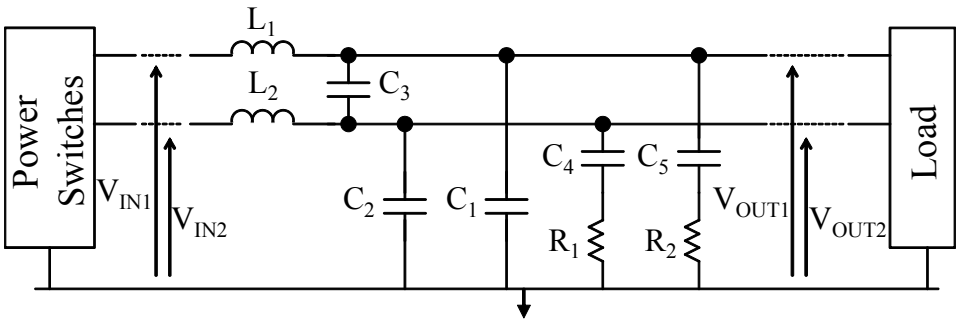


FIGURE 3.10: The filter schematic used.

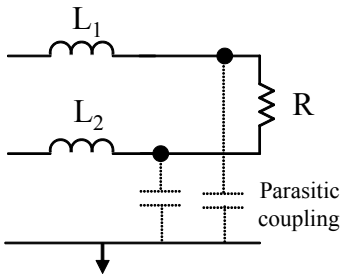


FIGURE 3.11: The dummy load schematic.

TABLE 3.1: Filter components values.

L_1, L_2	$15\mu H$
C_1, C_2	$33nF$
C_4, C_5	$68nF$
C_3	$150nF$
R_1, R_2	22Ω

TABLE 3.2: Dummy load components values.

L_1, L_2	$15\mu H$
R	8Ω

3.4.1 Instrumentation used

This experimental validation was made using the following list of laboratory instruments.

Digital oscilloscope: The Lecroy HRO-64Zi 12-bit digital oscilloscope has been used for all the time domain measurements and acquisition, including the currents and the voltages measurements. The 12-bit are needed to reduce the quantization noise generated by any digital data acquisition. A 12-bit oscilloscope has a $72\,dB$ of dynamical range instead of the $48\,dB$ for the most common 8-bit oscilloscopes. The frequency bandwidth of the used device is $[DC - 400\,MHz]$.

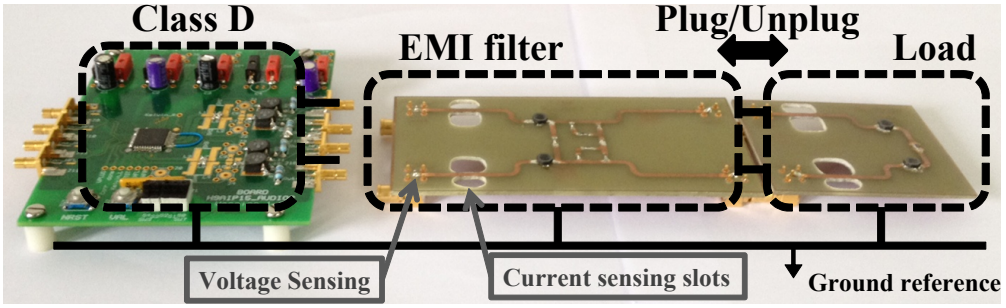


FIGURE 3.12: Class-D amplification system.

Note that no frequency domain measurements with an EMC analyzer have been done because the amplifier voltages must be measured at the same time.

Voltage probe: The Lecroy PP008 passive voltage probe has been used for voltage sensing. Its frequency bandwidth is $[DC - 500\,MHz]$. Note that, a $10\,M\Omega$ resistance in parallel with a $10\,pF$ capacitance is added to the circuit every time this probe is connected. This issue has been taken into account in simulations in order to perform simulations with conditions conditions close to the measurements.

Not that in some cases, the voltage measurements must be made with differential probes to avoid shorting the reference voltage to the ground. However, in the present case this issue can be neglected due to the system architecture.

Current probe: The Tektronix P6022 current probe is used for current sensing. Its frequency bandwidth is $[8.5\,kHz - 100\,MHz]$. Note that, a parasitic impedance equivalent to the circuit of Fig. 3.13 is added every time the probe is connected to the circuit [86]. This issue has also been taken into account in the simulation in order to get closer to the measurement conditions.

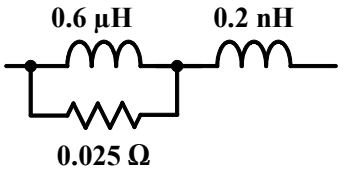


FIGURE 3.13: Current probe equivalent circuit.

Impedance Analyzer: For impedance measurements, the precision impedance analyzer Agilent 4294A have been used. Its frequency bandwidth is $[40\,Hz - 110\,MHz]$.

Vector Network Analyzer: The R&S ZVB8 4 port VNA is used for S parameter measurements. Its frequency bandwidth is $[300\,kHz - 8\,GHz]$.

Anechoic chamber: All the measurements were done in an anechoic chamber in order prevent the environmental EM noise from disturbing the measurement accuracy.

According to these measuring instruments, the study is limited by the current probe bandwidth. Therefore, for the rest of this work all the current and voltages measurements will be showed up to $100\,MHz$ which allows us to validate the method beyond the conducted EMI frequency band. In addition, the chosen input audio signal is a sine wave having a $10\,kHz$ frequency. The main reason of this choice is to avoid any spectral content below this frequency, as we will not be able to evaluate it in the current spectra. Thus, the validation of the method is carried out on the $[8.5\,kHz - 100\,MHz]$ frequency band which is the same as the current probe bandwidth.

3.4.2 Class-D amplifier modeling

The Class-D amplifier in use has to be modeled according to the section 3.3.1. As a differential system, the Class-D amplifier can be then modeled by two voltages sources representing the power switching and a 4×4 impedance matrix representing the converter output impedance.

We started by measuring the Class-D output voltages for the same audio signal, but with different loading conditions in order to evaluate the internal impedance of the converter IC. Therefore, the output voltages have been measured, first with an open circuit output, second with a speaker load, and third with an EMI filter followed by a speaker load. Only two cases are shown in Fig. 3.14 for a better presentation of the results. The spectra are identical over the considered frequency band. Thus, it can be deduced that, the amplifier voltage is independent of the load and the amplifier output impedance is negligible over the considered frequency range. Therefore, the measured voltages at the amplifier output pins can be used for the amplifier modeling and the amplifier can be modeled with two voltage sources that refer to the power stage switching. Note that, the plus and minus voltages of the amplifier outputs must be measured in the same time in order to obtain the correct phase between both of them. Therefore, they have been

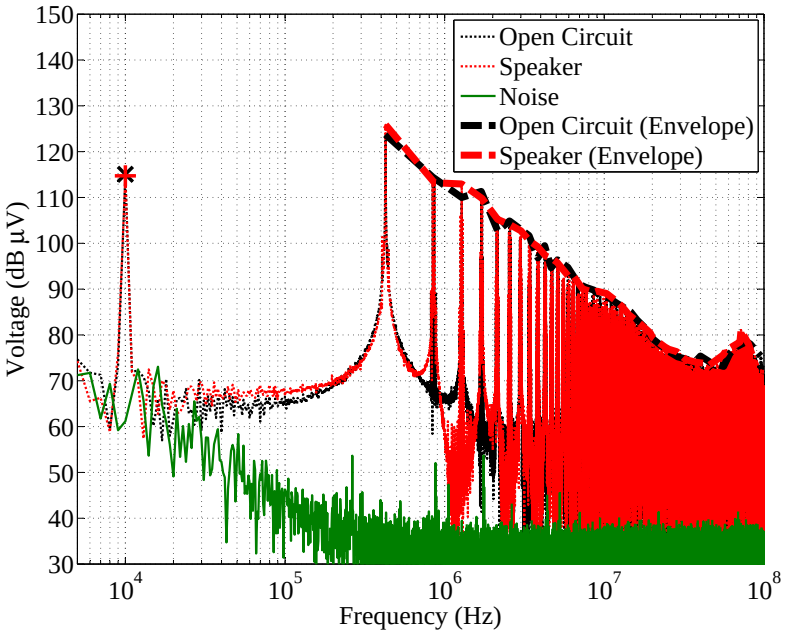


FIGURE 3.14: Amplifier output voltage V_{plus} for two different load conditions.

measured in the time domain at the same time then a FFT is used to compute the equivalent frequency domain spectra.

Note that, determining the two voltage sources of a Class-D amplifier by simulation has been investigated. However, this point is detailed in appendix C.1 for a better uniformity in the document flow.

3.4.3 Filter impedance matrix determination

The studied system is differential, thus, it has 2 active conductors, which means N is equal to 2. As a *Type A* block, the filter is then modeled by a 4×4 impedance matrix. To determine this latter the 3 methods described previously are applied.

3.4.3.1 Filter impedance matrix determination using an IA

The IA is used following the procedure presented in section 3.3.3.1 to measure Z_{ii} $(i = 1 \dots 4)$ and $Z_{ij_{sc}}$ $(i = 1 \dots 4\ ;\ j = 1 \dots 4\ ;\ i \neq j)$. Hereafter, equation (3.5) is used to calculate Z_{ij}. Note that the IA used has a frequency limitation of 110 MHz so the measurements were done in the range of [10 kHz – 110 MHz].

3.4.3.2 Filter impedance matrix determination using a VNA

The 4-port VNA is used to measure the filter scattering matrix. Then, equation (3.6) transforms the measured 4×4 scattering matrix to a 4×4 impedance matrix. In this case, I is a 4×4 eye matrix and Z_0 is 50 Ω. Note that the minimum frequency possible for the VNA used is 300 kHz, so that the measurements are done in the frequency range [300 $kHz - 1$ GHz].

3.4.3.3 Filter impedance matrix determination by simulation

In the simulation program used (ADS), PCB tracks are modeled as strip-lines. PCB material characteristics are taken into account. Components are replaced by the measured component impedance itself or by a specific model provided by the supplier. Filter layout is taken into account and in some cases where the tracks are close to each other, coupling between them is also added using specified strip-line blocks. However, the coupling between components themselves and between components and tracks are not modeled but it might be possible to take them into account [87]. This is the real advantage of the measuring methods shown before (IA and VNA) where these types of couplings are included without any additional effort. As, the frequency band can be defined by the user, it was defined to [10 $kHz - 1$ GHz].

In order to prove the importance of each of the modeling details, four models have been considered. Table 3.3 shows the characteristics of the models which are named "Black model", "Red model", "Blue model" and "Green model" for simplification. These models are simulated and four of the impedance matrix elements are shown in Fig. 3.15. This latter shows the high difference between the model responses at high frequencies which prove the high influence of the parasitic components on the high frequency EMI behavior (beyond 10 MHz). The Green model is the one including the most details in the modeling process, thus, it is considered for the rest of the work.

3.4.3.4 Comparison between IA, VNA and ADS simulation

To compare the results from the above three methods, the impedance results of z_{11} (diagonal elements) are plotted in Fig. 3.16(a) and z_{14} (cross elements) in

TABLE 3.3: ADS filter models.

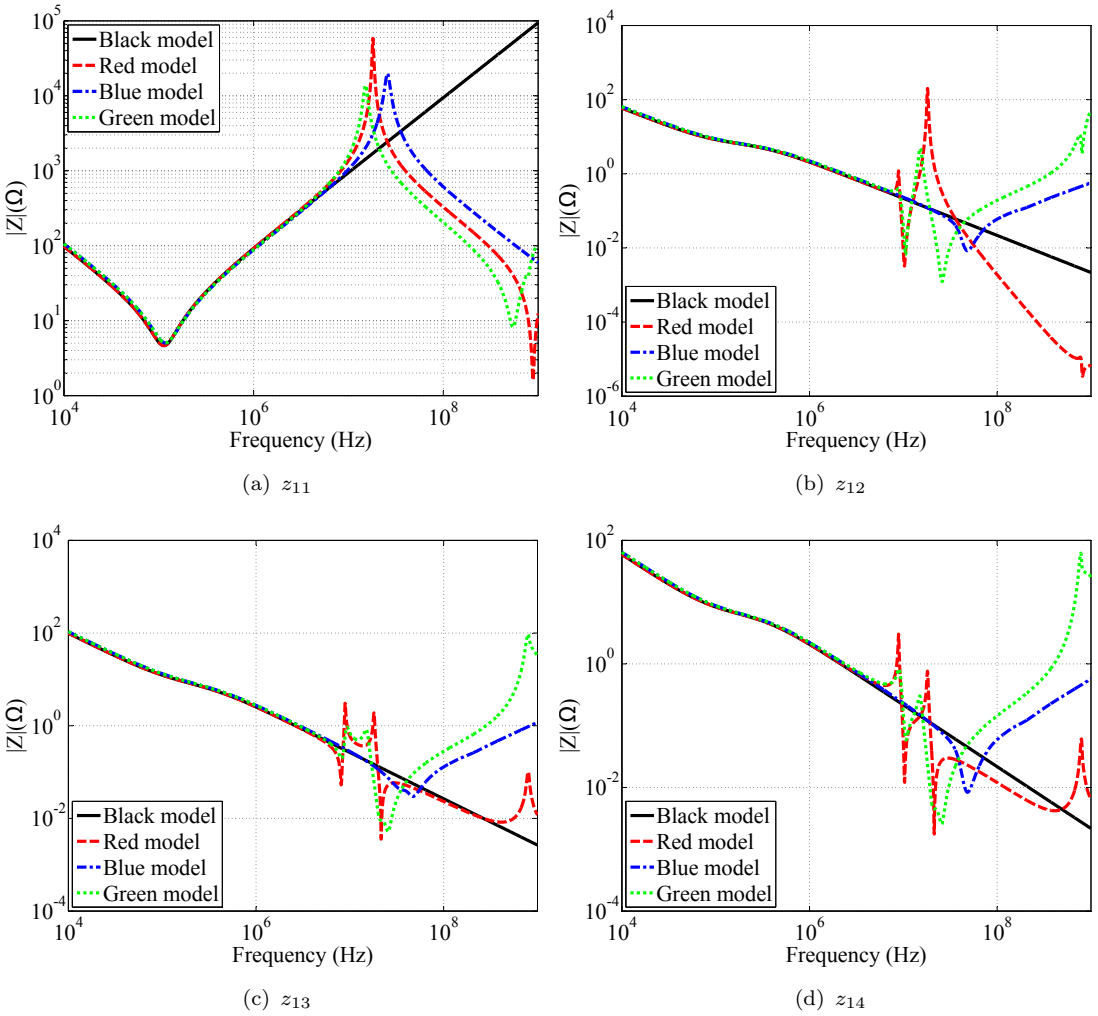
Model name	Ideal component models	Supplier component models	PCB layout taken into account	PCB layout not taken into account
Black model	✓			✓
Red model	✓		✓	
Blue model		✓		✓
Green model		✓	✓	

Fig. 3.16(b). According to Fig. 3.16(a), all three methods give similar results for the diagonal elements. However, Fig. 3.16(b) shows that in the case of IA (grey line) or VNA (black line) measurements, accuracy problem can occur in the cross elements.

In fact, in the case of IA, cross elements are calculated using equation (3.5), where z_{11} is subtracted from $z_{14_{sc}}$. At high frequencies, z_{11} is mainly equal to the filter inductor impedance and PCB stray capacitance ; the capacitors impedances are very small (Fig. 3.10). Likewise, at high frequencies $z_{14_{sc}}$ is approximately equal to Z_{L_1} and the PCB stray capacitance ; the capacitor impedances are very small and C_2, C_4, R_1 are in short circuit (see Fig. 3.17). Hence, it is shown in Fig. 3.18 that z_{11} and $z_{14_{sc}}$ overlap at high frequencies which makes the difference less than the minimal precision of the measuring device (IA).

In the case of VNA measurements, the Z matrix is calculated from the filter S matrix using equation (3.6). Fig. 3.19 shows the measured and simulated s_{14}. This figure shows that s_{14} values are lower then the minimal measuring precision of the VNA in the $[10\ MHz - 100\ MHz]$ frequency range. This measurement error propagates to Z_{14} which can be seen in Fig. 3.16(b).

When using simulation, the impedances show mostly an over estimated resonance effects. In addition, the inductive and capacitive coupling between tracks and components cannot be easily taken into account. However, it shows correct impedance behavior for the entire impedance matrix and over the entire frequency range considered. Moreover, determining an impedance matrix with simulation requires



(a) z_{11} (b) z_{12}

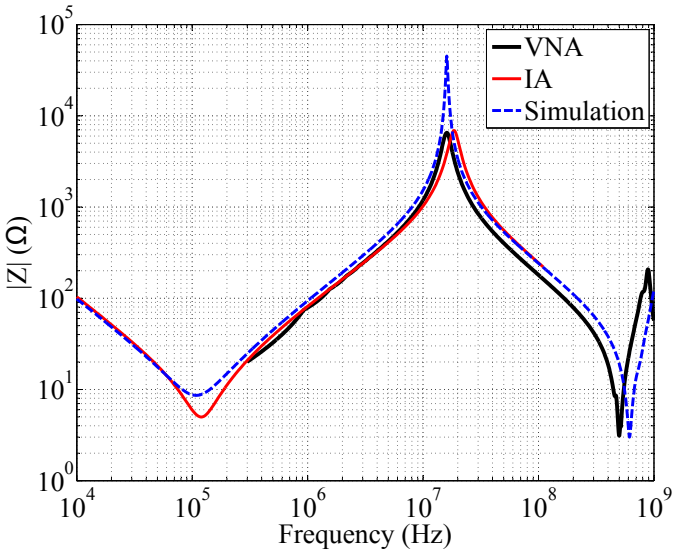
(c) z_{13} (d) z_{14}

FIGURE 3.15: Impedance matrix elements of the models in Table 3.3 using ADS simulation

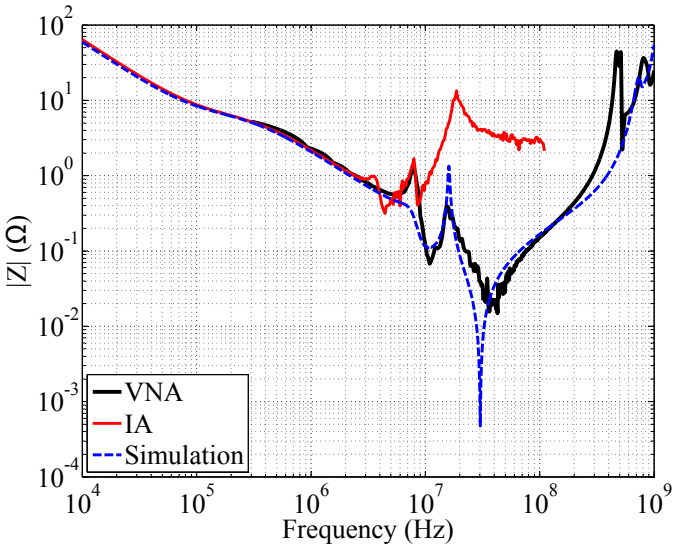
no prototype, which means virtual EMI tests can be performed before production. Therefore, the simulation has been considered as a good solution for this application and the simulated results are used for the rest of this work.

3.4.4 Load impedance matrix

The load is a *Type B* block which means it is modeled by a 2×2 impedance matrix. The three methods presented above are also applied to determine this matrix. These methods have been studied in details in section 3.4.3, thus, the load matrix determination is not developed for the sake of conciseness. However, for a better understanding of impedance matrices, an interesting reasoning on the speaker



(a) z_{11}



(b) z_{14}

FIGURE 3.16: Filter impedance results.

impedance matrix is made in appendix D.1. Furthermore, measurements of the speaker impedance under temperature variations in can be found in appendix D.4.

3.4.5 Currents and voltages computation

Now that the needed impedance matrices have been determined, it it possible to compute the voltages and the currents at all the nodes in the system. First, equation (3.9) has been used in order to concatenate the filter and the load matrices which allow us to obtain the resulting impedance matrix. Afterwards, the

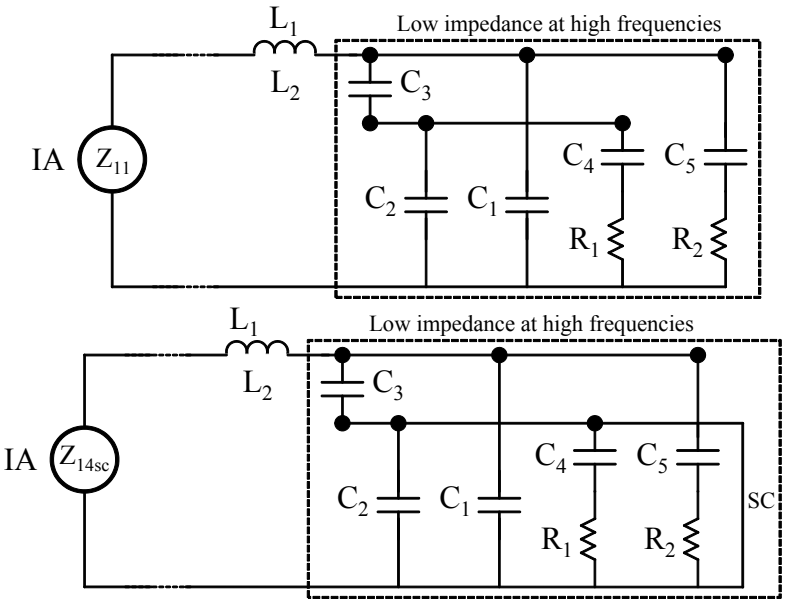


FIGURE 3.17: z_{11} and $z_{14_{sc}}$ impedances seen by the IA

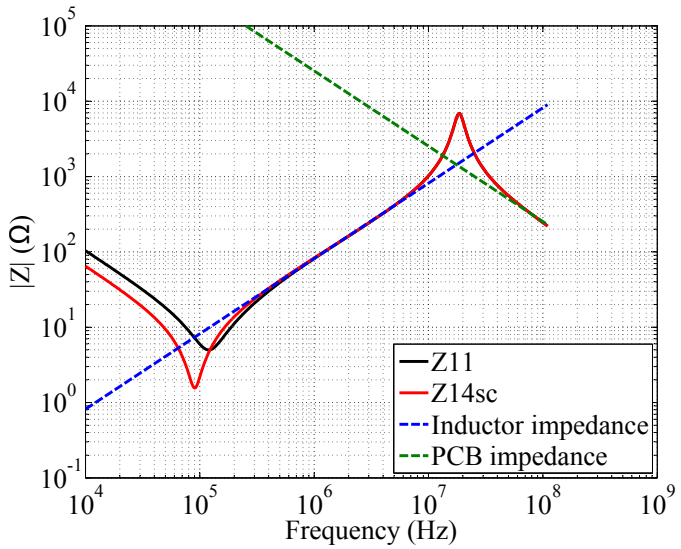


FIGURE 3.18: Filter: Measured z_{11} and $z_{14_{sc}}$ with an IA

equations (3.10), (3.11) and (3.12) were used in order to compute the currents at amplifier output (filter input) and the current and voltages at the filter output (load input). The results are shown in Fig. 3.20, Fig. 3.21 and Fig. 3.22 respectively.

Fig. 3.20 shows that the computed input current have a good accordance with the measured one on the considered frequency range. The only difference between the two spectra is an extra peak in case of measurement at $30MHz$; this is due to the current noise floor. However, in Fig. 3.21 the computed output voltage is in

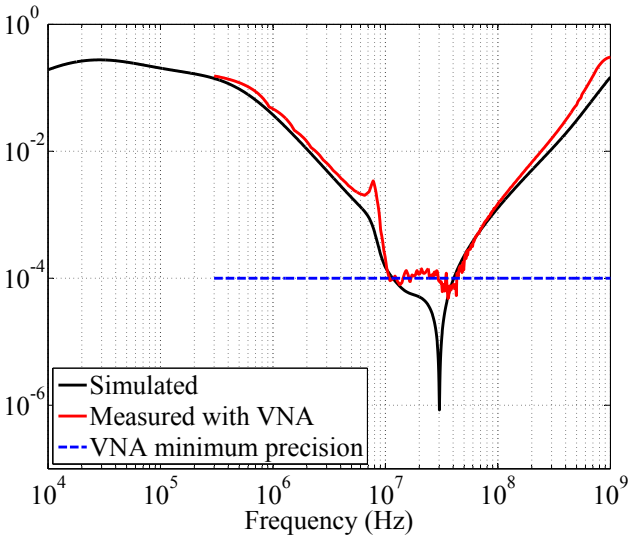


FIGURE 3.19: Filter: VNA minimum precision seen in s_{14}.

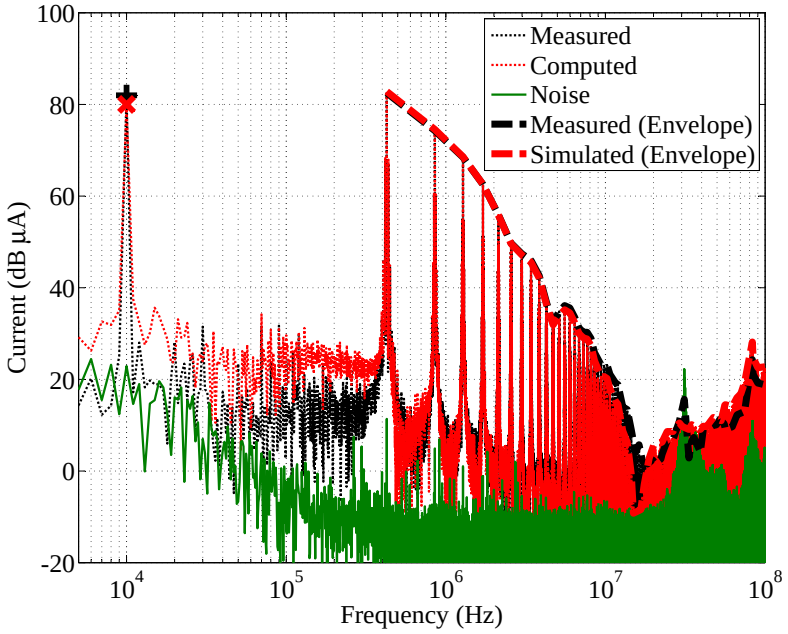


FIGURE 3.20: Input current of the filter $I_{IN_{Plus}}$.

a good agreement with the measured one up to $6MHz$. Beyond this frequency, the voltage spectra is lower than the noise floor. The instrumentation in use does not allow any voltage measurements below $20\,dB\mu V$ $(10\,\mu V)$. Likewise, Fig 3.22 shows that the instrumentation in use do not allow any current measurement below $-6\,dB\mu A$ $(0.5\,\mu A)$, thus the computed current can be compared to the measured one up to $2MHz$. The output voltages and currents cannot be validated beyond $6MHz$ and $2MHz$ respectively, however, according to Fig. 3.20 the method has been validated up to $100\,MHz$.

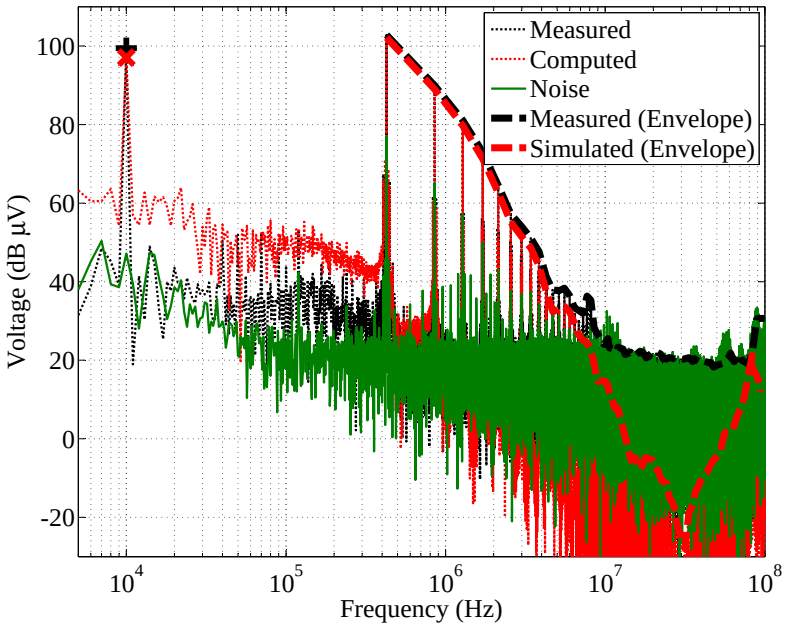


FIGURE 3.21: Output voltage of the filter $V_{OUT_{Plus}}$.

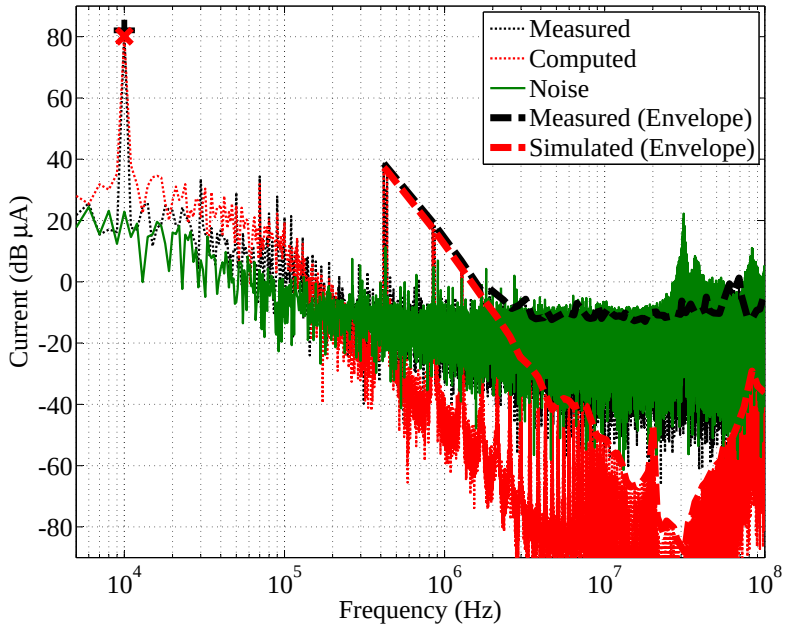


FIGURE 3.22: Output current of the filter $I_{OUT_{Plus}}$.

3.5 Experimental application on a Class-D amplifier – *Supply side*

It has been discussed earlier in section 2.2.2, that a battery used for powering the system, is a EM coupling path. As the battery is connected to all the circuits in a system, it is a common impedance between those, which spread the noise. In order to reduce the perturbations at the battery level, an input filter (e.g. decoupling

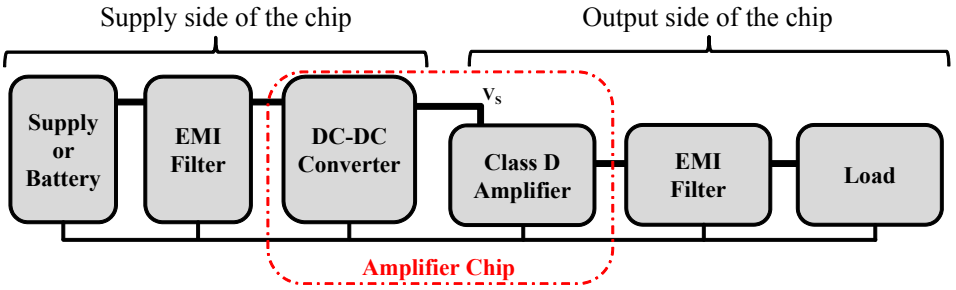
capacitor) is generally included between the converter and the battery. A proper design of the input filter needs the knowledge of the impedances at both sides: the converter input impedance and the battery impedance. However, most of the time, the EMI filter is designed according to the Line Impedance Stabilization Network (LISN) impedance [88–90] instead of the real supply impedance. The LISN is a passive circuit used only when measuring the EM emissions according to the EMC standards, but it is not used in the final application. In [88–90] interesting filters have been designed in order to lower the conducted emissions below the limits of the EMC standards. However, in the final application these filters will behave differently because they were designed according to a LISN. The impedance of a LISN is far different from the real supply impedance which is the battery impedance. These are interesting works which allow a good filter design in order respect the EMC standards. Nevertheless, when the device is not fed by a LISN, the filter design will not guarantee a noiseless power system to prevent any electronic system failure. This issue has been highlighted in [91, 92].

For the above stated reasons, the battery behavior should be considered for EMC simulations in order to predict the conducted emissions at the supply rails. This can easily be done by using the method proposed in section 3.3. For this purpose, lets consider a Class-D amplifier system. A Class-D amplifier can be supplied by a DC-DC converter [27] (boost converter) as shown in Fig. 3.23(a). Accordingly, the case turns to be a single phase (N=1) problem as shown in Fig. 3.23(b). Thus, the DC-DC converter is modeled by one electric source and a 2×2 impedance matrix. The EMI filter is a *Type A* block which means it is modeled by a 2×2 impedance matrix. Finally, the battery is a *Type B* block, thus, a single impedance (1×1 matrix). Applying the method of section 3.3 in this case is an easy task. However, the only challenge is to determine the impedance of the battery which is the goal of this section.

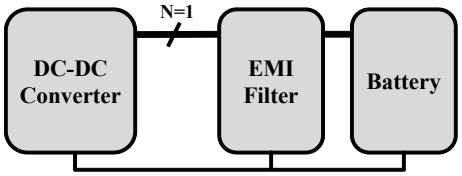
3.5.1 Measurement techniques for batteries

This work has been performed with the help of Sami Tabakh from the Lebanese University.

Traditionally, there exists two major techniques for battery modeling: Electrochemical Impedance Spectroscopy (EIS) and charge/discharge dynamic modeling tests.



(a) Block diagram of a Class-D amplifier system.



(b) Single phase case of study.

FIGURE 3.23: Class-D amplification system.

In battery EIS, just like usual impedance spectroscopy, the battery impedance spectrum is measured by applying an AC voltage and measuring the corresponding current, or vice versa [93, 94]. There are two EIS configurations: galvanostatic and potentiostatic. In galvanostatic configuration, a DC bias current is applied to the battery, and in the potentiostatic configuration, a DC bias voltage, usually equal to the open circuit voltage of the battery under test, is applied to protect the battery from excessive discharge current through the measuring instrument. Thus, the EIS for batteries is implemented by the special instruments such as Solartron instruments. Such instruments operate at very low frequency ranges (from few mHz to some kHz). This is because the phenomena under study such as State Of Charge (SOC), separator evaluation, and other reaction mechanisms are revealed only at low frequencies. Thus, traditional battery EIS are not suitable for EMI diagnosis.

The second traditional battery modeling technique is the charge/discharge or dynamic modeling tests. It is applied on batteries in order to model their performances in terms of voltage, capacity fading, impedance and other parameters during charge cycle intervals and life cycle intervals. The procedure consists of subjecting the battery to charge or discharge DC currents while monitoring some battery aspects such as the open circuit voltage and temperature [95, 96]. These studies do not provide any information about the impedance spectrum and thus are not useful for EMI modeling.

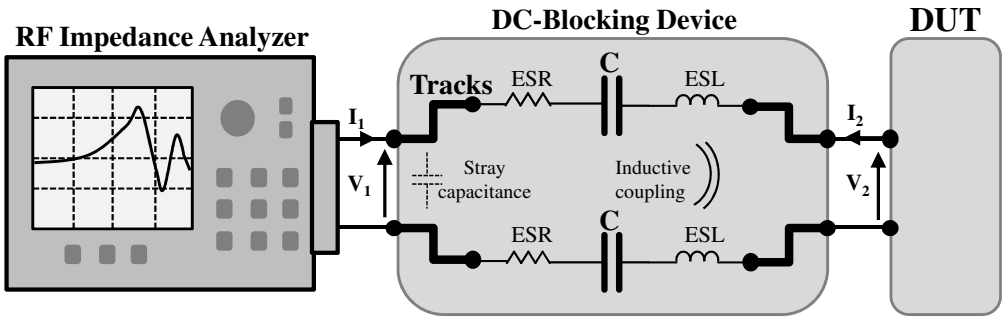


FIGURE 3.24: Measurement set-up principle

For EMC studies, the frequency bandwidth of previously presented instruments is not large enough. Moreover, usually, these devices are not at EMC engineer's disposal. In [91, 92, 97], a Vector Network Analyzer (VNA) is used to make measurements from 40 kHz to 400 MHz. In this case, the battery is considered as a three-pole device (battery plus, battery minus and ground). The measured impedances correspond to the reflection and transmission parameters between the two ports but not to the battery impedance. In the case where the battery is not a three-pole device but just a dipole, the method used in [97] is less adapted. In [98], a dedicated power converter was designed in order to generate current ripples up to 20 kHz. In this work, we use a method with a classic impedance analyzer for a user-friendly battery impedance determination.

3.5.2 Battery impedance measurement with an IA

A battery cannot be directly plugged to an impedance analyzer because a current might flows in the measuring equipment [99]. This current can be destructive for the impedance analyzer. Thus, a "DC block" (a two port block that stop the DC current) should be connected between the impedance analyzer and the battery (Fig. 3.24).

In [100] the batteries impedances were measured up to 40 MHz but the set up which protect the instrument is not presented. In [99], a capacitor is proposed as a DC block and the recommended frequency for the measurement is 1 kHz. However, the blocking capacitor impedance is considered as negligible and a direct measurement is supposed to give the battery impedance. Because of the considered frequency range in the present work, the behavior of capacitors is far from being ideal due to their intrinsic limitations (equivalent series resistance, equivalent series inductance...) and to the stray elements of the small PCB on which the capacitor

is connected. Then the DC block cannot be neglected. Therefore, an alternate technique is adopted and it is explained in the following.

Inspired from section 3.3, the DC block is considered as a 2×2 impedance matrix. Thus, the procedure consists of making three initial measurements with three different Z_{DUT} values in order to identify the impedance of the DC block. Afterwards, the battery impedance can be computed with equation (3.13). The proof can be found in appendix B.5.

$$Z_{comp} = \frac{(Z_{init_1} - Z_{init_3})(Z_{IA} - Z_{init_2})}{(Z_{init_3} - Z_{init_2})(Z_{init_1} - Z_{IA})} Z_{std} \tag{3.13}$$

where Z_{IA} is the impedance of the DC block and the DUT seen by the IA. Z_{init_1}, Z_{init_2} and Z_{init_3} are the required three impedance measurements which are described as follow:

- For Z_{init_1}, Z_{DUT} is an open circuit ($|Z_{DUT}| \to \infty$).
- For Z_{init_2}, Z_{DUT} is a short circuit ($|Z_{DUT}| \to 0$).
- For Z_{init_3}, Z_{DUT} is a known impedance ($Z_{DUT} = Z_{std}$).

Note that Z_{std}, the known impedance, should be close to the expected battery impedance in order to minimize the computation errors of equation (3.13). Note as well that, determining the DC block impedance can be done using the method in section 3.3.3.1. However, the present method is used because it does not require a change of connections between the DC block and the IA which lead to a higher measurement accuracy.

This procedure can be seen as a custom compensation procedure. Indeed, impedance analyzers propose a compensation procedure in order to take into account that the measurement plane can differ from the calibration plane [99]. In the present case, the standard compensation procedure will fail because the DC block impedance is very different from the one of a test fixture or a cable.

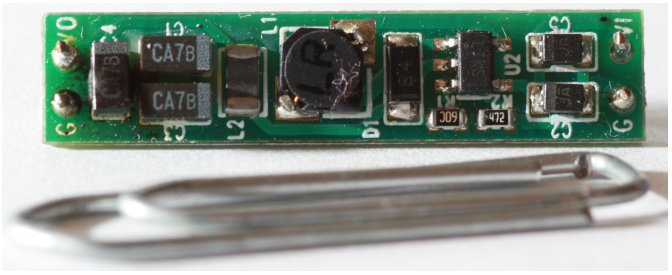


FIGURE 3.25: DC-DC converter used for the experimental validation placed near to a paper clip

3.6 Validation example using a battery and a power converter

For the experimental validation a DC/DC step-up converter VT-0312 (Fig. 3.25) from Musimi was supplied with a Nokia BL-5CA battery dedicated to cell-phones. This converter provides 12 V with an input voltage ranging between 2.7 and 5 V. The maximum input current is 70 mA. The switching frequency is 1.2 MHz. The battery is a lithium-ion with a capacity of 700 mAh. The battery output voltage is 3.7 V.

3.6.1 Battery impedance

As the switching frequency of the converter is 1.2 MHz, thus, the spectra has no content below this frequency. The battery impedance is then measured from 1 MHz to 100 MHz using the procedure of section 3.5.2 and the Agilent E4991a IA [101]. The DC block is constituted of two capacitors of 1 μF mounted on a PCB to avoid any change in the parasitic components and the connectors have been chosen according to the IA and the battery connections.

The procedure has been used to measure a known impedance of a 1 Ω resistor for validation. The results were accurate over the considered frequency band, but they are not shown in this documents for the sake of conciseness. These results can be found in [102].

The battery impedance results are shown in Fig. 3.26. First, we can see that the measured impedance Z_{IA} is different from the battery impedance Z_{Bat}. This means that the DC block impedance is not negligible and it must be considered for the battery impedance measurement. Second, we can see an inductive behavior

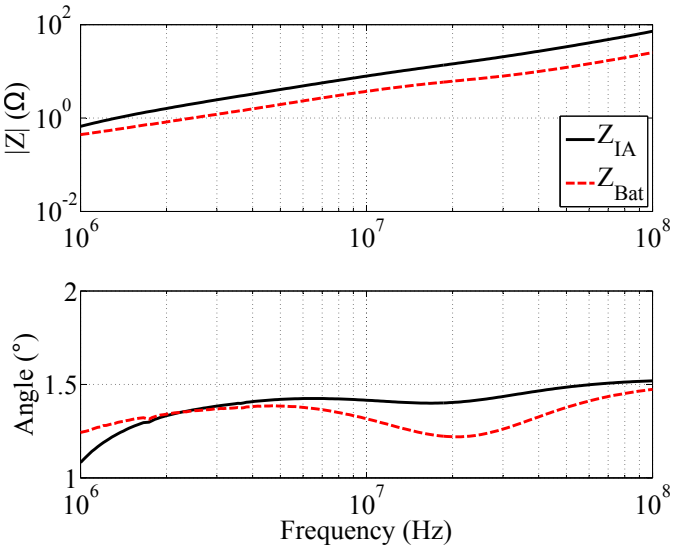


FIGURE 3.26: Battery impedance measurement

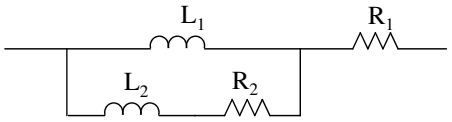


FIGURE 3.27: Battery impedance model

of the battery impedance. This is coherent with the analysis and the results from [98, 100]. The article [100] shows that the impedance does not change when the state of charge changes. It can be supposed that, at high frequencies, the impedance is more related to electrodes and connections than to electrochemical phenomena.

In order to use the battery impedance in a transient simulation, an equivalent circuit model should be established. An equivalent circuit is shown in Fig. 3.27. In this model, L_1 and R_1 model the stray inductance and the resistance of the battery and its connections. L_2 and R_2 are added in order to take into account the skin effect [38, 100]. The elements of the equivalent circuit are calculated by a least-squares error algorithm. The comparison between the equivalent circuit impedance (Z_{mod}) and the measured one (Z_{comp}) in Fig. 3.28 shows that this model describes very well the behavior of the battery under consideration.

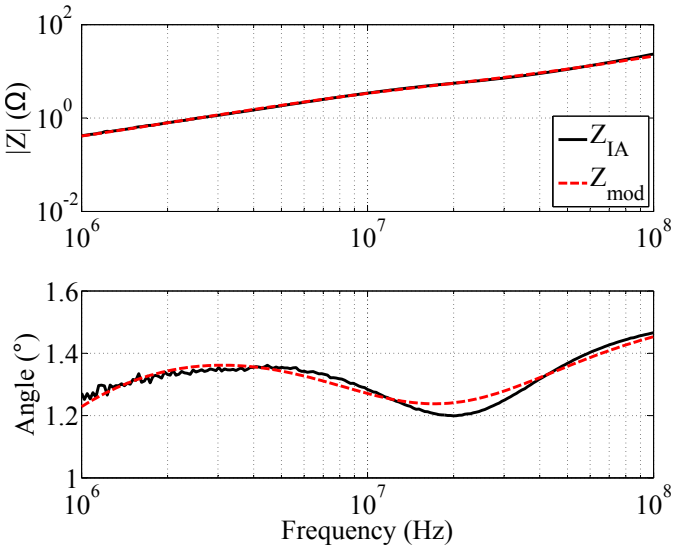


FIGURE 3.28: Battery model results

3.6.2 Voltage computation and battery impedance verification

The DC/DC board was mounted on an another PCB that connects the battery to the converter input, and the load to the converter output. The PCB also have holes around the track connected to the plus pin of the battery in order to easily plug a current probe. In addition, it has pins at the battery plus/minus to sense the voltage with a voltage probe.

The validation was done as follows. First, the bench was placed in an anechoic chamber in order to reduce the environmental perturbations. Second, the current and voltage at the converter input were measured in the time domain, then their spectra were computed using the Fast Fourier Transform (FFT). Finally, the measured current spectrum was multiplied by the measured battery impedance in order to calculate the voltage spectrum. Results are shown in Fig. 3.29.

Results show that the converter switching at 1.2 MHz have harmonics all over the considered frequency band. Fig. 3.29 shows also that the calculated voltage matches with the measured one, at least up to 80 MHz. However, beyond 80 MHz the noise floor is hiding the voltage spectra which prevents the results comparison. Note that the noise is the max of: (i) the voltage noise measured when plugging both pins of the voltage probe to the battery minus pin and (ii) the computed voltage noise which is calculated by multiplying the measured current when the

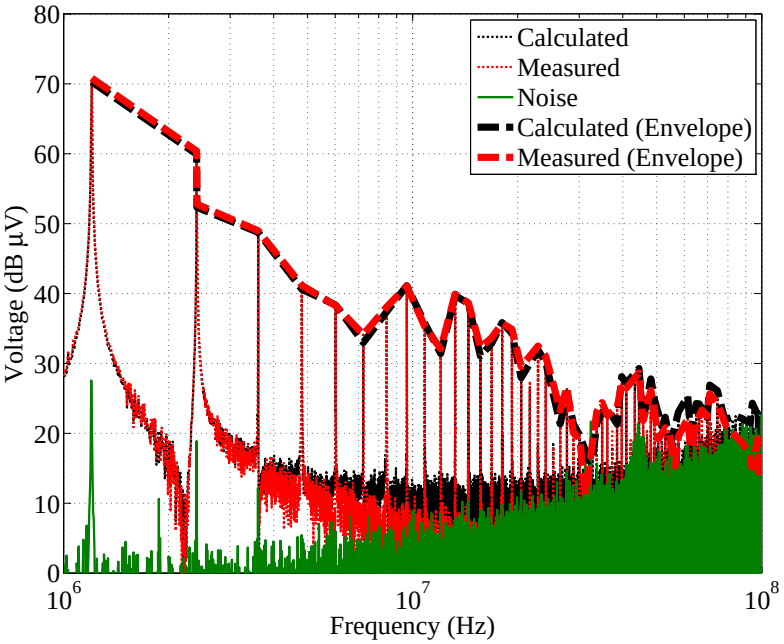


FIGURE 3.29: Magnitude of the battery voltage FFT when feeding the SMPS

current probe is unplugged and kept near the sensing area by the measured battery impedance.

The same procedure has been applied also on the Class-D amplifier used in section 3.4 and the battery used in section 3.6. The results do not allow a battery impedance validation on a wide range of frequencies because of the high noise level of the experiment. However, it is shown in appendix C.2 in order to validate the battery impedance measurements below 1 MHz.

3.7 Chapter conclusion

A new modeling method in the frequency domain has been presented in this chapter. It is used for multi-phase systems which allows us to model single-ended and differential Class-D amplifiers. The approach consists in decomposing the system into functional blocks, where the passive ones are modeled with impedance matrices and active blocks are modeled with AC voltage sources and an impedance matrix if needed. By using multi-port impedance matrices, this approach is able to cover the CM, DM and mode conversion. This chapter has proposed three different methods to determine the impedance matrices which are the measurements by IA or VNA, and the simulation using ADS. A comparison between those was made in order to evaluate their advantages and the drawbacks. Once determined,

the impedance matrices are concatenated in order to obtain a compact model for the system. The impedance matrices and the converter model can be used for current and voltages computation in all the system nodes.

The approach is applied on the output of a differential Class-D amplification system, thus, validated for two active conductors. By a comparison with measurements, the results have showed accurate results up to 100 MHz. Additionally, this approach has been applied on the supply side of a DC-DC converter connected to a battery. This is a single active conductor case. The experimental validation allowed us to validate this technique once again up to 80 MHz due to the high noise floor. The main challenge of this case of study was determining the impedance of the battery. For this purpose, an impedance measurement technique for batteries using an IA have been also developed.

This method can be then used by system integrators in order to make virtual EMI measurements on their systems. This is important feature that allows checking a design before the prototype construction. As a frequency domain model it has a fast simulation time which is a key for EMC design. It is then possible to achieve a higher number of simulations and test more possible solutions. Hence, it will be a great advantage if this approach is implemented in a filter design process. Therefore, the next chapter deals with integrating this method in an optimization process for EMI filter design.

Chapter 4

EMI Filter Design Using a Discrete Optimization Algorithm

The work presented in this chapter has been developed in collaboration with Mr. Moises Ferber (moisesferber@gmail.com) from Ampère laboratory. Mr. Ferber has been involved at two levels. First, his knowledge about the optimizations was helpful for choosing and tuning the used algorithm. Second, he developed the communication needed between ADS and Matlab softwares. Thus, the author would like to thank him gratefully.

The design of EMI filters is not similar to any of the classical high-pass, low-pass, band-pass or other filter types [76]. As EMI filters generally deal with wider frequency bands, each of the parasitics count for their performance [12]. Therefore, they are one more challenging step in the design process. Here, the model developed in the previous chapter can be very useful. It allows us to have a good accuracy in the EMI prediction and it has a short simulation time. Therefore, using this model in a process of EMI filter design is the main goal of this chapter.

When designing EMI filters for Class-D amplifiers, instead EMI, additional problematics are confronted. Here, the filter is placed on the audio path which is the same as the power path. Thus, the filter transfer function must not change the overall amplifier gain in the audio frequency band (see appendix A for definition). Likewise, the EMI filter must not reduce significantly the amplifier power efficiency which is one of the main advantageous characteristics for these amplifiers. The

contribution of EMI filter in increasing the power losses is discussed later on in this chapter.

4.1 State of the art of EMI filter design

In [68, 103–108], the authors use frequency domain models in order to simulate the considered systems and the impedance connected on both sides of the filter are determined. Afterwards, the filter design has been based on the required attenuation in order to meet with the EMC standards. These procedures may lead to sub-optimal solutions. By using these methods we will be able to design a filter with the required EMI attenuation, but it is more complicated to consider other characteristics such as volume, area or electrical consumption, etc. Therefore, the filter design formulated as an optimization problem can be advantageous in order to search for the best trade of the desired characteristics.

A continuous optimization procedure has been applied to EMI filter design for power electronics [109–111], for aerospace applications [112, 113] and for signal processing [114]. Here, the component values are allowed to take any value in a predefined continuous range. However, in some cases, this type of optimization is less well-adapted. Passive filters are constituted of standard components available on the market, such as surface mounted technology (SMT) components. These have well-defined nominal values. Component nominal values given by a continuous optimization are most of the time unavailable from suppliers. Therefore, optimizing the filter according to the available components on the market would be more helpful.

The number of available components on the market, considering all suppliers, is very high. Therefore, an exhaustive search would take a very long time, thus, impractical. Discrete optimization methods are able to explore a very small subset of the design space and find the global optimal or a design which is near to the global optimal.

Previous work such as [115–117], neglect or give less importance to the parasitic effects of components and printed circuit board (PCB) tracks. Nevertheless, this part is essential in high frequency EMI modeling. In [118], the equivalent series resistance, capacitance and inductance of passive components are modeled with lumped circuit elements as an attempt to increase accuracy in EMC analysis and

optimization. However, there is no simple expression that links these parasitic effects to the component nominal value.

The challenges for designing an optimal EMI filter can be then summarized as follow:

- Obtain an optimal trade off between criteria such as EMI attenuation response, power consumption, area on PCB, etc.
- The filter passive components must be available on the market.
- Take into account the filter imperfections in the optimization process.

These challenges have been considered separately in the literature which might lead to an improper filter design [117]. Therefore, developing an optimization process based on the modeling approach presented in chapter 3, will help us to improve the filter design because it permits to overcome the above challenges.

4.2 Proposed filter design methodology

The design of an EMI filter can be divided into two main steps: (i) determine a filter topology, (ii) choose the components. Generally, the filter structure can be found by using common structures in the literature, or in some cases, a complex design can be made following the specifications of the application itself. Once the filter topology is decided upon, the choice of components can be made by experience, by analytical calculation or by optimization which is the chosen solution for this work.

4.2.1 Optimization algorithm

4.2.1.1 Choice of algorithm

The choice of the optimization algorithm is very important [119] in order to make a reliable optimization in a short computation time. By considering the passive components available on the market our problem is discrete, and by considering the several criteria to be optimized (EMI, power losses, etc.) the problem is

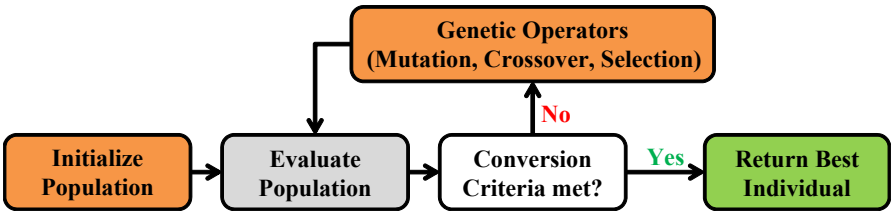


FIGURE 4.1: General diagram of a GA.

also multi-modal. In addition, no initial point can be specified. Furthermore, the fitness function calculation requires simulation data from a different software, thus, it is evaluated externally. Therefore, the Genetic Algorithm (GA) [119, 120] is an appropriate method to be applied on our optimization problem. The general diagram representing the optimization by GAs is shown in Fig. 4.1.

The process is described as follow. An initial population is generated randomly over the input range. Note that a population is a group of solutions proposed by the GA at certain iteration. Afterwards, each individual from the population is tested by simulated in the system model in order to compute the criteria to be optimized. According to the conversion criteria, which are some predefined optimization conditions, the population is evaluated then updated to the next generation using the GA operators (mutation, crossover, selection). At the final iteration, the best individual of the final population is expected to be an improvement relative to the best individual of the initial population.

4.2.1.2 Operators

In the context of this work, the input range is defined as the set of indices of the available passive components. Thus, the mutation operator consists in changing an index of an arbitrary component with a, generally low, probability set by the user. For example, with a probability of 1%, an arbitrary inductor may be changed from a catalog reference Ref_xxx1 to a Ref_xxx2. Fig. 4.2 shows an example of mutation applied to a filter with 3 components to be optimized, in which the inductor was changed.

The crossover operator consists in considering two individuals, each having their components indices, and exchanging an arbitrary index between them, with a probability set by the user. For example, consider two filters called individual 1 and individual 2. These have inductors reference Ref_xxx1 and Ref_xxx2, respectively.

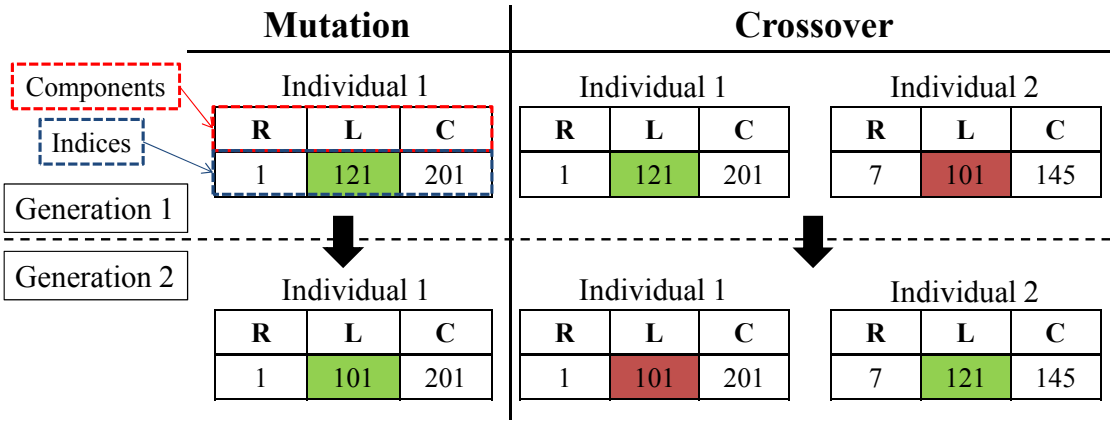


FIGURE 4.2: Mutation and crossover examples.

If the crossover operator is applied, then individual 1 has now an inductor reference Ref_xxx2 instead of Ref_xxx1. Similarly, individual 2 has an inductor of reference Ref_xxx1 instead of Ref_xxx2. Fig. 4.2 shows an example of applying a crossover operator.

The selection operator consists in selecting the individuals with a probability based on the fitness evaluation. Thus, individuals with a better fitness have a higher probability of being selected to be part of the population in the next generation.

4.2.2 Optimization process

The optimization process in development is a combination between the GA and the frequency model developed in chapter 3. Summarized in Fig. 4.3, the process is composed of:

- An iteration loop running on the GA bases and containing
  - A filter model implemented in ADS that defines
    - The filter structure
    - The filter layout
  - The frequency domain model of chapter 3 that defines
    - The source emissions
    - The load impedance
  - The fitness functions that defines
    - The goals

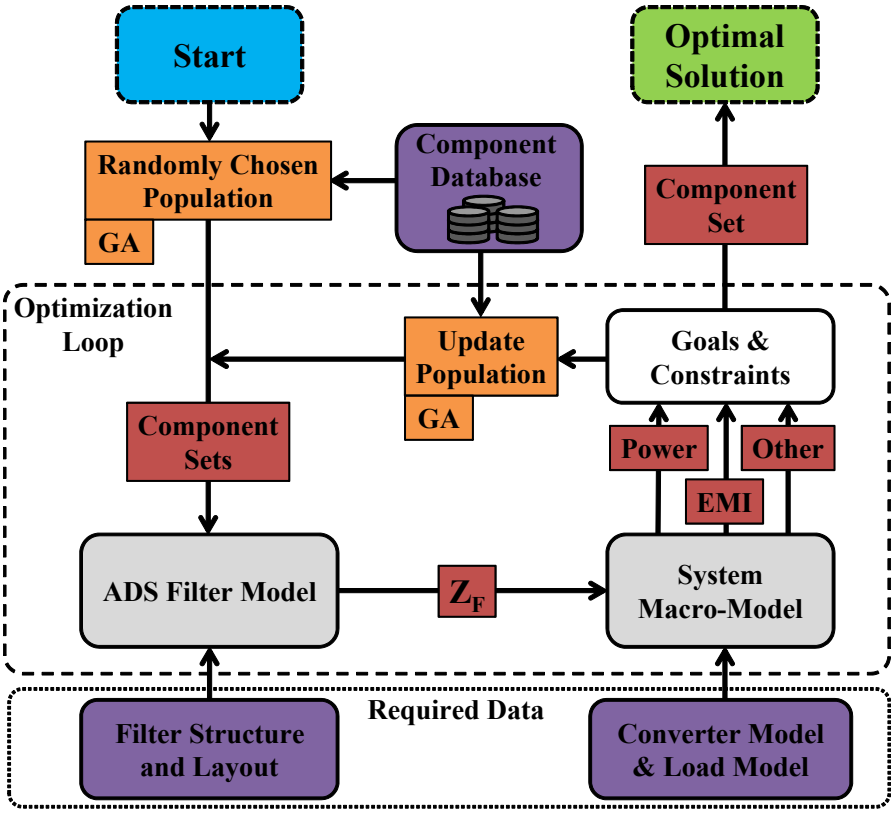


FIGURE 4.3: Optimization application.

  - The constraints

- Passive components database
  - It contains the capacitor and inductor libraries of the suppliers
  - It points to passive component high frequency models that include the component parasitic elements

The data flow of the optimization loop is described as follows. A starting population is generated randomly by the GA. It contains the passive component combinations for EMI filters chosen from the database. This population is transmitted to the ADS filter model in order to generate the population impedance matrices. These are then transmitted to the frequency model that compute the EMI criterion and other criteria if needed. Transmitted to the fitness function, the criteria allow an evaluation of the population according to the predefined goals and constraints. Upon that, the best individual is recorded then the GA updates the population to the next generation. The final iteration is reached when all the conversion criteria are met or when the maximum iteration number is attained. At this point, the final best filter is recorded as the optimal solution found.

4.3 Application to Class-D amplifier

The test chip of the differential Class-D amplifier and the dummy load used in section 3.4 has been reused for optimization. Therefore, the amplifier voltages and the load impedance matrix have been used in the frequency domain model. In order to choose the amplifier voltages, many output spectrum measurements and simulations have been done. Finally, it has been concluded that for low audio signals, this amplifier is considered as operating in the worst EMI conditions. First, an audio signal is needed to include the intermodulation peaks in the amplifier output spectrum. In the opposite case and if the audio signal is equal to zero, the output signal become a square signal with a 50 % duty cycle. Thus, the intermodulation peaks around the even and the odd harmonics disappear. Second, because at low audio signal, the PWM harmonics are the highest over the considered frequency range.

4.3.1 EMI filter and passive components

The filter structure shown in Fig. 3.10 has been chosen for this optimization. The filter presented in [84] has been considered as reference and it's component references are given in Table 4.1. The filter has nine components which include two inductors, two resistors and five capacitors, that correspond to common and differential mode filtering. However, to ensure the symmetrical nature of the filters, thus, avoiding any differential to common mode conversion, and vice versa, some components must be identical. Hence, the problem consists of choosing the components L_1, R_1, C_1, C_3 and C_4, the five parameters to be optimized, knowing that by symmetry R_2, L_2, C_2 and C_5 are automatically chosen.

The chosen filter is made up of SMT components, and some suppliers provide design kits to be used with a given simulation program (ADS in this case). A design kit contains a library of components referring to the supplier's products. Many of them can be included at one time, and so in our study, two libraries have been chosen [121, 122]. The inductors have been chosen from [121] and the capacitors from [122]. Therefore, a database has been created in MATLAB referring to these two libraries to be included in the optimization process. Note that as the footprint of each filter component must be chosen for the layout, the capacitors have been defined as a 1005 (metric) SMT package and the inductors

TABLE 4.1: Reference filter component values [84].

Component	Value	Reference
L_1, L_2	$15\,\mu H$	$CLF7045T-150M$
C_1, C_2	$0.033\,\mu F$	$GRM155R71C333KA01$
C_4, C_5	$0.068\,\mu F$	$GRM155R61A683KA01$
C_3	$0.15\,\mu F$	$GRM155R61A154KE19$
R_1, R_2	$22\,\Omega$	$CPF0402B22RE1$

as a 7045 (metric) SMT package. Thus, 718 capacitors and 8 inductors remain in the search space and the database is sorted according to the component nominal values. By our best knowledge, none of the suppliers provide a design kit for resistors. Therefore, we have measured the impedance of many resistors and we observed that their parasitic components can be neglected over the considered frequency range. Thus, the resistors have been considered as ideal ones but their nominal values have been limited to the values found on the market.

4.3.2 Power losses in Class-D amplifiers due to the EMI filter

An EMI filter can significantly reduce the Class-D amplifier power efficiency. To illustrate this phenomenon, Fig. 4.4 shows a power stage with a given EMI filter. At low or no audio signal, the plus and minus nodes are switching at the same time, so the differential signal is null; no current is driven into the speaker load. Meanwhile, the capacitors are charged and discharged on each period, as shown in Fig. 4.4 by the dashed arrow and the solid arrow, respectively. Therefore, power losses occur in the inductor and capacitor stray resistances, and also, in the MOSFET and PCB parasitic resistor. To verify this issue, power measurements have been made on the supply pin of the used Class-D amplifier chip. First, we determined the power without an EMI filter, and second, we introduced the filter at the amplifier output and we repeated the process. Determining the power was made by multiplying $I_{Bat-rms}$ and $V_{Bat-rms}$ which are respectively, the root mean square (rms) current and voltage measured at the supply bus. $I_{Bat-rms}$ and $V_{Bat-rms}$ were measured by a current and voltage probes connected to a digital oscilloscope. For zero and low audio signal level (lower than $-20\,dB$ full scale), we recorded a $10\,mW$ average value for the power consumption when the amplifier is used without an EMI filter, whereas an average of $50\,mW$ was recorded when

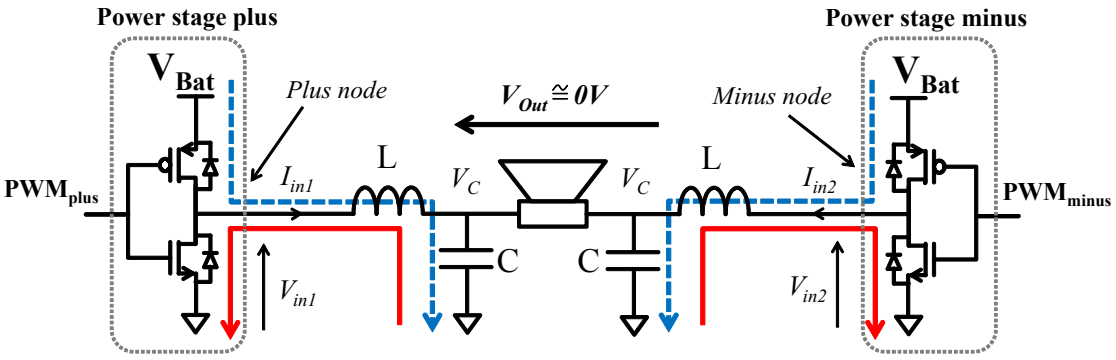


FIGURE 4.4: Class-D amplifier losses due to the EMI filter.

used with an EMI filter. Therefore, due to the EMI filter, the Class-D amplifier consumes 5 times more at low output power.

In [123], it has been shown that in a real audio signal (i.e. Jazz song) the amplitude levels having lower then $-20\,dB$ full scale have more $50\,\%$ samples than the higher amplitudes for a $10\,s$ recording. Thus, it can be deduced that a Class-D amplifier runs more then $50\,\%$ of the time at low signal levels (lower than $-20\,dB$ full scale). To conclude, the EMI filters are able to provoke significant power losses in final applications such as Class-D audio amplifiers. Therefore, it is interesting to include this as a criterion in the optimization process. Hence, the power losses of Class-D are to be computed as follows. Two types of losses have been considered. First, the losses in the power stage and second the losses in the passive parts (filter and load). Both can be taken into account using (4.1)

$$P_{Losses} = P_{PS} \quad + \quad \underbrace{P_{FL} - P_A}_{\text{filter and load losses}} \tag{4.1}$$

where P_{PS} represents the conduction losses in the power stage, P_{FL} represent the power delivered to the filter and the load, P_A is the power in the load at the audio frequency. They can be obtained by equations (4.2), (4.3) and (4.4), respectively.

$$P_{PS} = R_{DSon}(I^2_{in_1-rms} + I^2_{in_2-rms}) \tag{4.2}$$

where R_{DSon} is the power switch on resistor, I_{in_1-rms} and I_{in_2-rms} are the rms input currents of the filter, which are the same as the power stage output currents.

Note that the switching losses has been neglected in P_{PS} because they were supposed independent from the filter. Also, the body diode conduction has been neglected because of the short dead time.

$$P_{FL} = \sum_{k=1}^{n} Real\{V_{in_1}(f_k) \cdot I^*_{in_1}(f_k)\} + Real\{V_{in_2}(f_k) \cdot I^*_{in_2}(f_k)\} \tag{4.3}$$

where V_{in_1} and V_{in_2} are the filter input voltages and k is the index of the frequency vector. Note that P_{FL} also includes the power in the audio band. Therefore, it has been calculated by P_A (4.4) and deduced from the total power loss P_{Losses} in (4.1).

$$P_A = Real\{[V_{Out_1}(f_A) - V_{Out_2}(f_A)] \cdot I^*_{Out_1}(f_A)\} \tag{4.4}$$

where $V_{out_1}(f_A)$ and $V_{out_2}(f_A)$ are the filter output voltages at the audio frequency and $I_{out_1}(f_A)$ is the filter output current at the audio frequency.

4.3.3 Optimization formulation for Class-D amplifiers

The optimization process has been tested twice on two different formulations for the same application. The details are given in the following subsections.

4.3.3.1 Formulation I: Power-loss optimization

The power-loss optimization formulation aims at reducing the system power losses due to the EMI filter. It has therefore been set as the optimization goal. The focus is to design an EMI filter having lower power losses than the reference filter with the same component footprints and the same or lower EMI level.

In fact, minimizing P_{Losses} allows us to optimize the power efficiency of the system. However, this must not deteriorate the filter's EMI behavior or impact on the audio signal by a significant voltage drop in the audio band. Therefore, these two criteria have been included in the fitness function as constraints. If the component set results in the EMI criterion being worse than that of the reference filter, then a high penalty number ($EMI\ Penalty \gg P_{Losses}$) is added to the fitness function. Moreover, if the audio voltage drop is greater than 2.5 % compared to the audio

TABLE 4.2: Power consumption obtained by simulation.

	P_{PS} [mW]	P_{FL} [mW]	P_A [mW]	P_{Losses} [mW]
No filter	3	84.4	82.5	4.9
Reference filter	5.7	139.1	78.8	66
Pow Loss Opt filter	3.7	88.2	79	12.9

TABLE 4.3: Component values and references for the power loss optimized filter.

Component	Value	Reference
L_1, L_2	$22\,\mu H$	$CLF7045T-220M$
C_1, C_2	$0.74\,\mu F$	$GRM155R60J474KE19$
C_4, C_5	$1.2\,pF$	$GRM1535C1H1R2CDD5$
C_3	$0.1\,\mu F$	$GRM155R61H104KE19$
R_1, R_2	$1.6\,\Omega$	$MC0.0625W04021\%1R60$

signal when no EMI filter is used, a high penalty number is also applied to the fitness function. If the opposite is true, then the penalties are set to zero. The fitness function can be then described by (4.5)

$$F_{Pow\,Loss} = P_{Losses} + EMI\ Penalty + Audio\ Penalty \tag{4.5}$$

The EMI criterion is considered worse than the reference filter if any peak in the output current spectrum is higher than the one for the reference filter. Note that the filter's output currents have been considered instead of the voltages because a single-ended current is enough to express the audio signal at $10\,kHz$. However, for the voltages, both are needed to express the audio signal (because of the differential output). In chapter 3, the macro-model has been validated up to $100\,MHz$. However, as the conducted EM emission is studied in this work, the EMI criterion has been set up to $30\,MHz$ since the conducted EMC standards of such systems are defined up to this frequency.

The optimization has been executed and the filter optimal component set obtained. A power consumption comparison is presented in Table 4.2 and the component values and references are given in Table 4.3.

As can be seen in Table 4.2, the lowest P_{Losses} and the highest P_A are obtained when no filter is used. In the opposite case, the highest power losses are obtained when using the reference filter. The latter multiply the amplifier power losses by 13.5 times compared to the No filter case. Thus, the power loss optimization

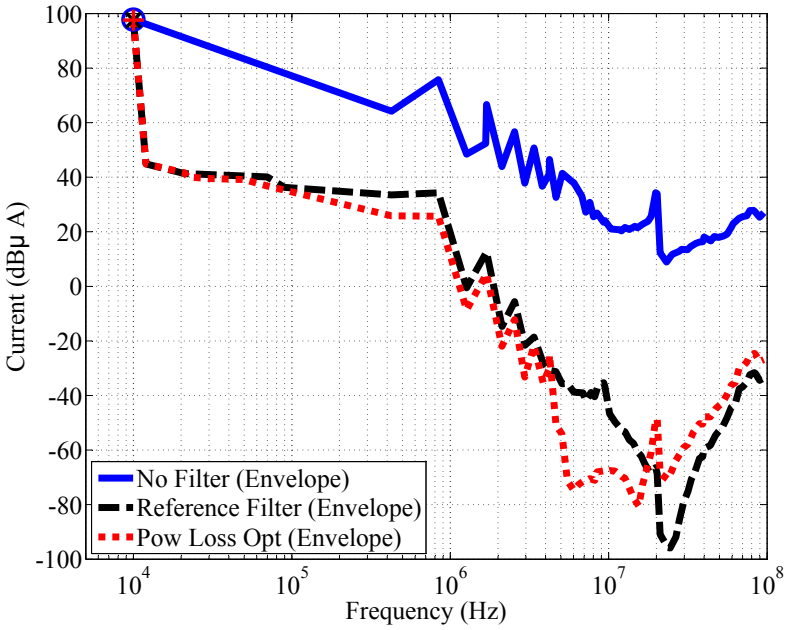


FIGURE 4.5: Output current in the power loss optimization case.

process is very efficient because it has divided the additional power losses due to the EMI filter by more than five ($66/12.9 = 5.1$). The optimal filter has only 2.5 times power losses more than the No filter case.

Fig. 4.5 and Fig. 4.6 shows respectively the output current and voltage in the following cases: No filter, Reference filter and the Power Loss optimized filter. It can be seen that the current spectrum peaks have been lowered about 5 to 10 dB below 4 MHz, about 10 to 20 dB between 5 and 15 MHz. However, the spectrum peaks are higher beyond 15 MHz. In the voltage spectrum, the peaks were lowered up to 20 dB till 15 MHz and increased beyond 15 MHz. Thus, the spectra are better at some frequency bands and worse in others.

4.3.3.2 Formulation II: EMI optimization

The aim of the EMI optimization formulation is to improve the EMI response of the filter compared to the reference one. For this purpose, we considered a maximum upper limit equal the maximum spectrum value of the reference filter and we decided to make an overall minimization of the spectrum peaks according to these EMI limits (Fig. 4.7). Therefore, as an objective we chose to minimize the EMI criterion named Q_{EMI} and we considered the audio and the power losses

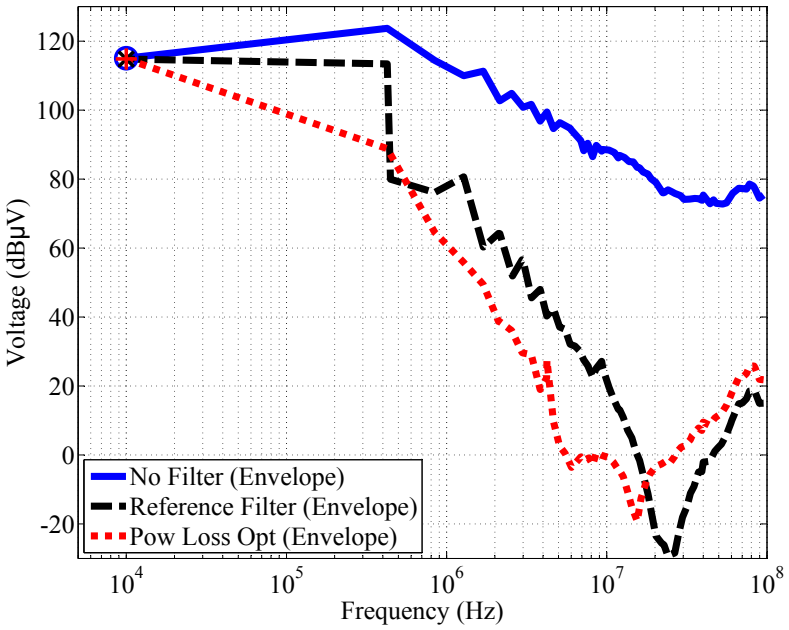


FIGURE 4.6: Output voltage in the power loss optimization case.

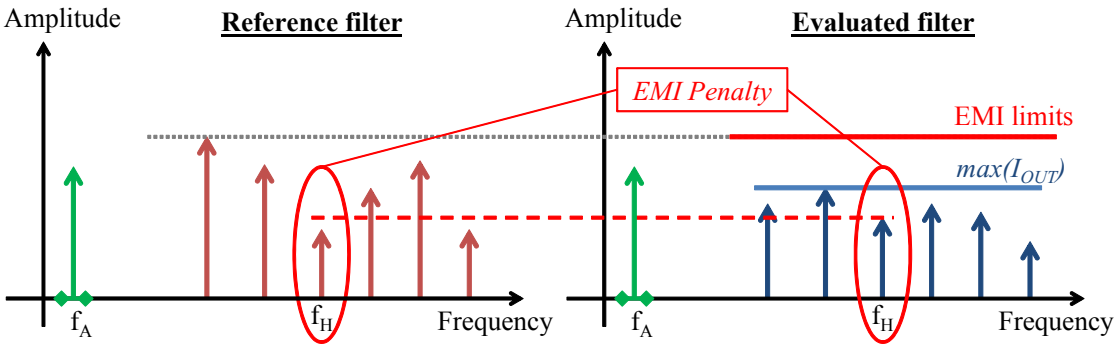


FIGURE 4.7: Calculation of the EMI criterion.

criteria as constraints. The fitness function can be then described by (4.6).

$$F_{EMI} = Q_{EMI} + Losses\ Penalty + Audio\ Penalty \tag{4.6}$$

where Q_{EMI} is given by equation (4.7) and *Losses Penalty* is a penalty applied to the fitness function when the power losses of the filter are higher than those of the reference filter.

$$Q_{EMI} = max\{I_{OUT}(f)\} + EMI\ Penalty \tag{4.7}$$

where the *EMI Penalty* is applied if any peak of the given filter spectrum exceeds the one obtained with the reference filter (see Fig. 4.7).

TABLE 4.4: Component values and references for the EMI optimized filter.

Component	Value	Reference
L_1, L_2	$22\,\mu H$	$CLF7045T-220M$
C_1, C_2	$0.1\,\mu F$	$GRM155R61H104KE19$
C_4, C_5	$0.1\,\mu F$	$GRM155R61H104KE19$
C_3	$0.47\,\mu F$	$LLL153C70G474ME17$
R_1, R_2	$1.3\,\Omega$	$MC0.0625W04021\%1R30$

TABLE 4.5: Power consumption obtained by simulation

	P_{PS} [mW]	P_{FL} [mW]	P_A [mW]	P_{Losses} [mW]
No filter	3	84.4	82.5	4.9
Reference filter	5.7	139.1	78.8	66
EMC Opt filter	4.2	96.5	85.5	15.2

The optimization has been executed and the filter optimal component set is obtained. The component values and references are given in Table 4.4.

First, Fig. 4.8 shows the output current in the case of the EMI optimized filter. Compared to the reference filter, the spectra peaks has been lowered up to $20\,dB$ between $150\,kHz$ and $4\,MHz$, also between $6\,MHz$ and $20\,MHzM$. However, the peaks have exceeded at $5\,MHz$ and beyond $20\,MHz$.

Second, Fig. 4.9 shows the output voltage in the same case. Here, the spectrum peaks were lowered up to $20\,dB$ till $20\,MHz$ and increased beyond this frequency.

Finally, in Table 4.5 a power loss comparison is presented. The EMC optimization with a power loss constraint has also improved to the amplifier power characteristics when used with the EMI filter. The optimized one has divided the power consumption by 4 and it has only 3 times more power consumption than the No filter case.

Note that Both formulation I and II are mono-objective ones that aim to minimize whether the power losses, whether the EMI. However, the multi-objective optimization is not used for the following reason. The power losses of the filter are mainly caused by the switching frequency and it's low order harmonics. Also, the highest spectrum peaks are those of the switching frequency and the low order harmonics. Therefore, reducing the EMI and the power losses consist of attenuating theses harmonics. Hence, both criteria have the same tendency and to Pareto chart can be obtained.

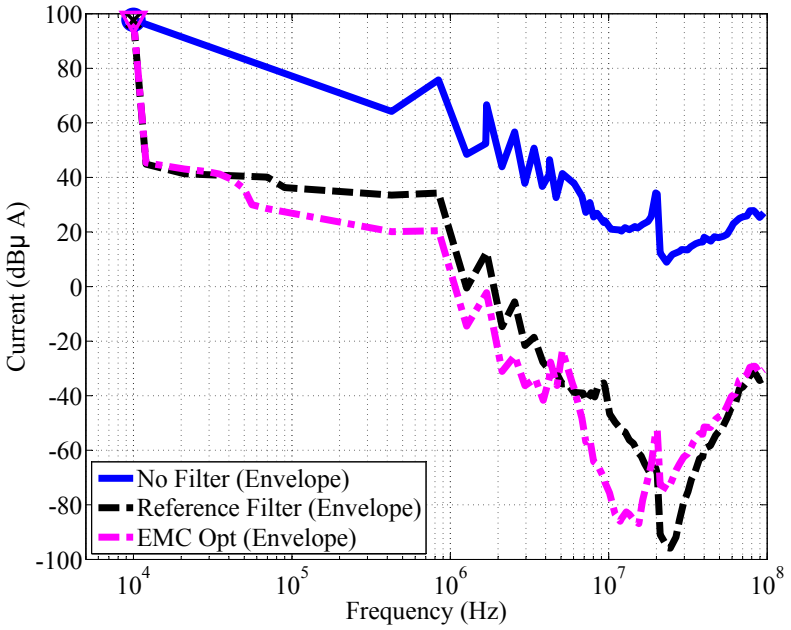


FIGURE 4.8: Output current in the EMI optimization case.

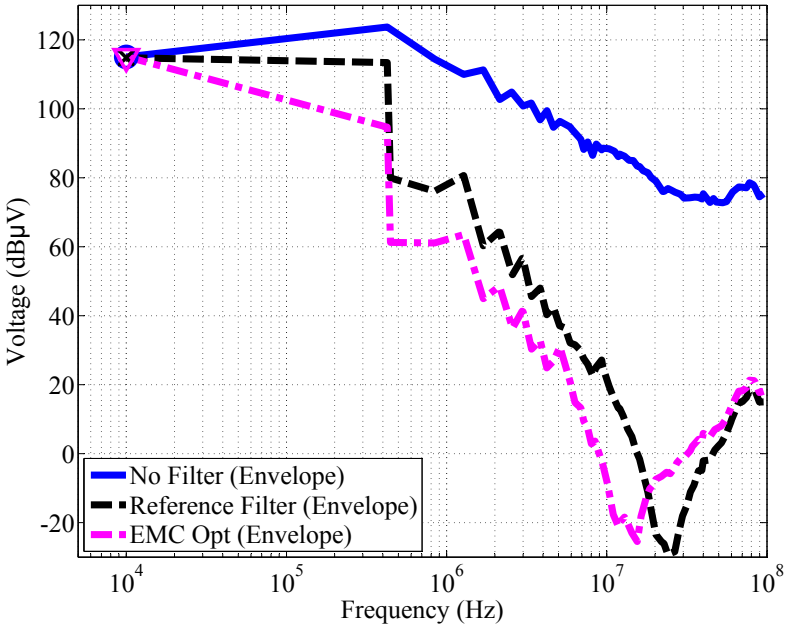


FIGURE 4.9: Output voltage in the EMI optimization case.

As a conclusion, thanks to a good formulation of the power loss criterion, the optimization process allowed us to improve significantly the power losses of the EMI filter compared to the reference one. However, the EMI of the Class-D amplifier has not been improved on the entire frequency band. The output spectra peaks of the optimized filters have been lowered in some frequency bands and increased in others. This must be due to the EMI criterion calculation which needs better formulation. In order to improve the EMI optimization, it is then necessary to calculate the EMI criterion differently. Therefore we propose an another method in the following.

If n is the length of the frequency vector on the considered frequency band, the EMI criterion Q_{EMI} can be calculated using equation (4.8).

$$Q_{EMI} = \underbrace{\left(\sum_{k=1}^{n} \frac{O_k - R_k}{R_k} B_k\right)}_{\text{Term 1}} + \underbrace{\left(\sum_{k=1}^{n} \frac{O_k - R_k}{R_k} \overline{B_k}\right) \cdot EMI\ Penalty \cdot T}_{\text{Term 2}} \tag{4.8}$$

with

$$B_k = \begin{cases} 1 & \text{if } R_k > O_k \\ 0 & \text{if } R_k < O_k \end{cases} \tag{4.9}$$

$$EMI\ Penalty \gg Q_{EMI} \tag{4.10}$$

$$T = \sum_{k=1}^{n} \overline{B_k} \tag{4.11}$$

As shown in Fig. 4.10, the R_k and O_k ($k = 1 \rightarrow n$) are the peak values of the reference and the optimized filters, respectively. Thus, Term 1 in equation (4.8) allows us to calculate the normalized difference between the two spectrum when the optimized filter peaks are lower than the reference ones. Likewise, Term 2 do the same thing but when the peaks of the reference filter are higher than the reference one. In addition, Term 2 multiply this quantity by $T \times EMI\ Penalty$ where T is the number of peaks in the optimized filter that exceed the ones of the reference filter. Hence, Term 1 is negative and Term 2 is positive. Therefore, reducing the EMI can be done by reducing the value of Q_{EMI} toward $-\infty$, knowing that Q_{EMI} is equal to zero if the optimized filter is the same as the reference one.

This formulation have not been tested yet but it will be tested in the future works. In the next section an experimental validation of formulations I and II is carried out in order to evaluate the reliability of the optimization process.

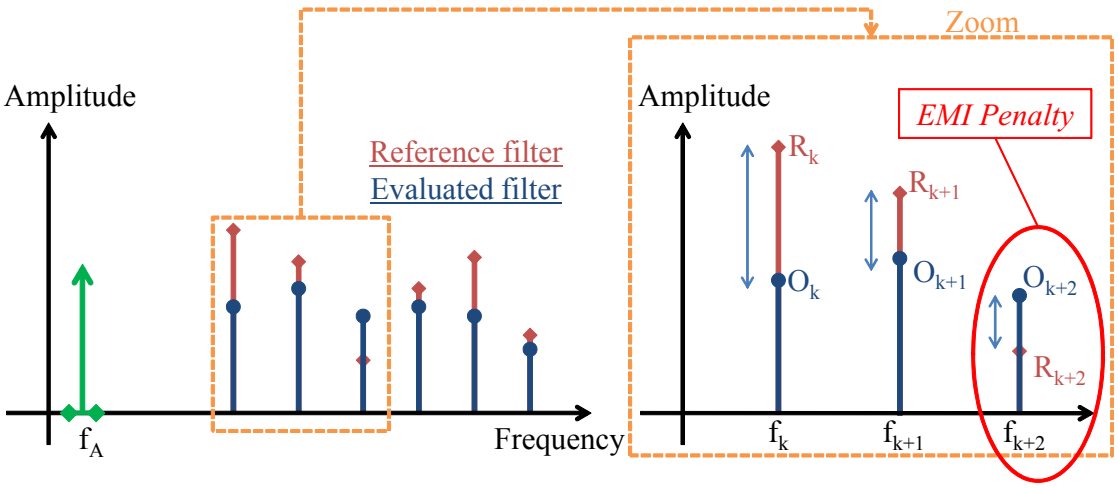


FIGURE 4.10: Another way for calculating the EMI criterion.

Here is an interesting issue that has been observed while developing this optimization process. The optimization process has been lunched several times under formulation I and formulation II configurations. For each formulation and for each execution, we obtained different component references and nominal values for the optimal filters which are not present for conciseness. Some of the component nominal values were obtained in the same order of magnitude such as the inductors, however, for some other components such as resistors (see Fig. 3.10) we obtained very different nominal values (very high in the kilo-Ohms or very low around one Ohm). Here, it will be then interesting to study the influence of these components on the filter performance in order to simplify the filter architecture if possible by removing these components. This would also allows us to reduce the overall area of the filter. This issue would be treated in the future work.

4.4 Experimental Validation

Prototypes for the reference filter as well as the optimized filters have been built and used for measurement with the Class-D amplifier. The filter layout is common for all the filters and is shown in Fig. 4.11. The measurement bench has been placed in an anechoic chamber to reduce the ambient EM noise. The input currents, output voltages and output currents are measured for comparison.

The output current used for the optimization criterion has very low values and the comparison with measurement is not possible. Therefore, Fig. 4.12 compares the

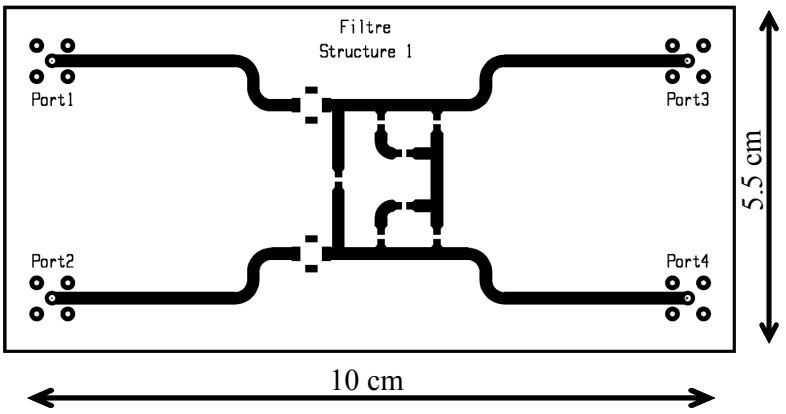


FIGURE 4.11: Filter layout.

measured and computed output voltages of the reference filter instead. It shows good matching between the measured and the computed results with an error lower to $6\,dB\mu V$. However, because the voltage noise floor (around $40\,dB\mu V$) is higher than the measured voltage at frequencies beyond $5\,MHz$, the comparison is also not possible. Therefore, Fig. 4.13 shows the comparison of the measured and simulated input current for the reference filter in order to evaluate the accuracy of the modeling approach in the optimization procedure. Here, the input current has a higher spectrum level than the measurement noise floor at the entire frequency band. Fig. 4.13 shows that the measured and the simulated input current match well up to $100\,MHz$. This proves that the modeling approach is accurate and adequate for the optimization process. As measurement probes have an impact on the spectra results because they add auxiliary parasitic stray components when connected to the circuit, the filters have been optimized in there nominal operating conditions (without the measurement probes), but for the comparison with the measurements the probes have been included in the optimized filter model.

In order to evaluate the optimized filters in the case of measurements, Fig. 4.14 shows the envelopes of the output voltages (voltages on the load) in the following cases. First, where no filter is used, second when the reference filter is used, then where the power optimized filter is used (formulation I) and finally, when the EMC optimized filter (formulation II) is used. It can be seen that no significant variations occur in the audio signal level at $10\,kHz$ (less then $2.5\,\%$) which is due to the audio constraint in the fitness functions. In addition, the spectrum peaks are higher when the EMI filter is not used and a good emission reduction can be obtained when introducing the EMI filter. In particular, the optimized filters offer a significant reduction in the spectrum compared to the reference filter. The

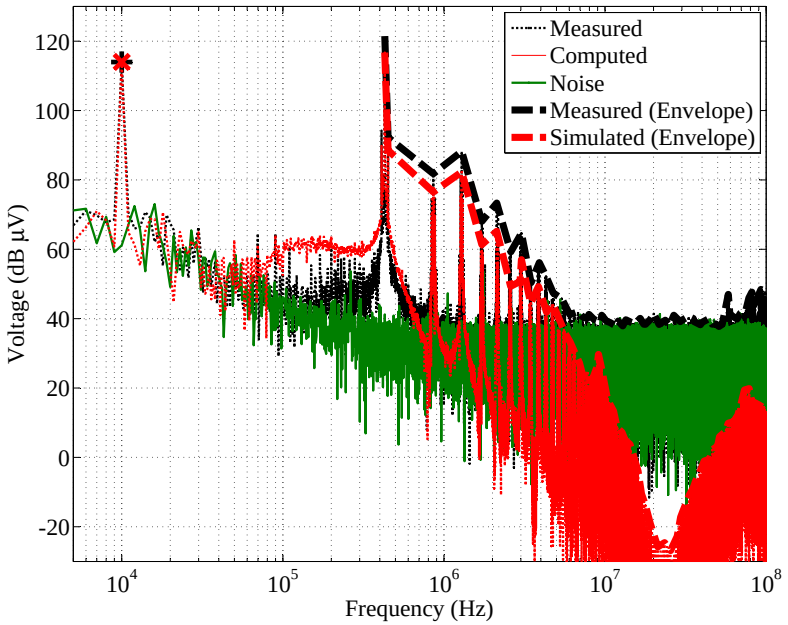


FIGURE 4.12: Filter output voltage.

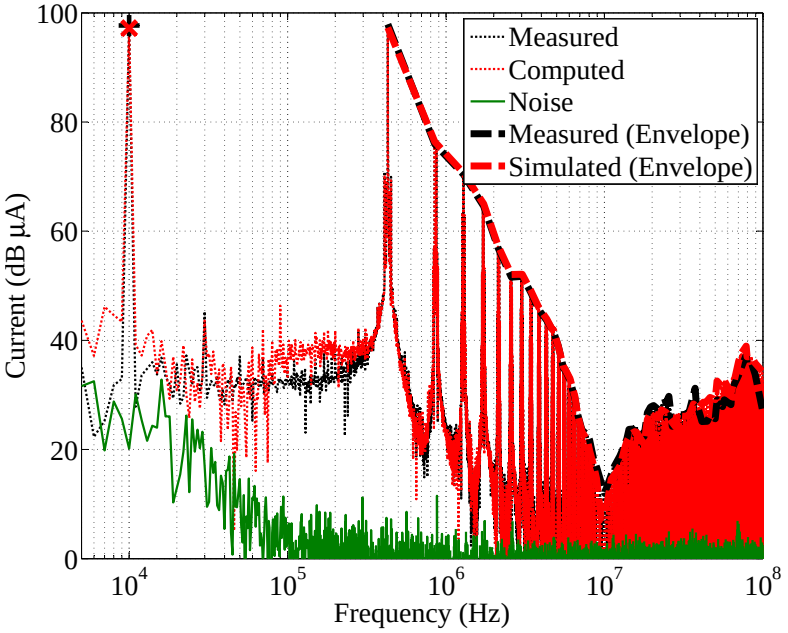


FIGURE 4.13: Filter input current.

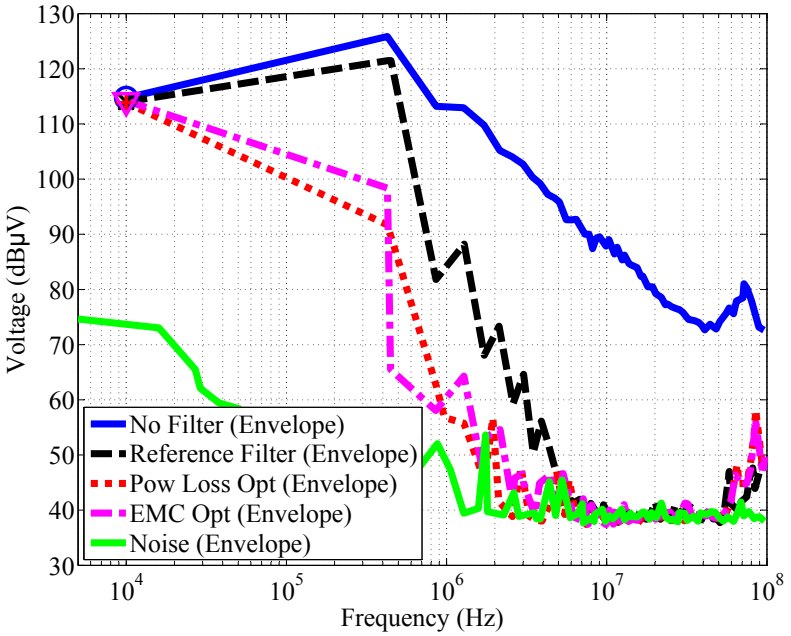


FIGURE 4.14: Measurement comparison of filter's output voltage envelopes.

output spectrum has approximately $20\,dB$ of additional reduction compared to the reference filter which is also been observed in section 4.3.3. Beyond $5\,MHz$ the voltage level is lower than the measurement noise floor, and so no comparison is possible. If we compare both of the optimized filters, we can observe that the power loss optimized filter has a batter EMI response than the EMC optimized one. This can be explained by the following. On one hand, the EMI criterion is not adequately formulated in the fitness function of the EMC optimization and it does not guarantee an efficient EMI improvement on the entire frequency band. On the other hand, the GA algorithm is based on probabilistic operators. It is an algorithm that allows us to find good solutions (global minimal values of the fitness function) but not the absolute ones (absolute minimal values of the fitness function). Note that if a GA optimization process is lunched several times in the same conditions, their is a very small probability that it generates the same solution.

To compare the power dissipation caused by the different filters, the measurement set-up shown in Fig. 4.15 has been used. A current and voltage probes connected to a digital oscilloscope allows us to measure the supply voltage and current for a fix voltage on the load. The audio analyzer (AA) allows us to measure the audio voltage at the load at a predefined audio frequency. Fig. 4.16 plots the results as a percentage of the power losses introduced by the different filters. On the vertical

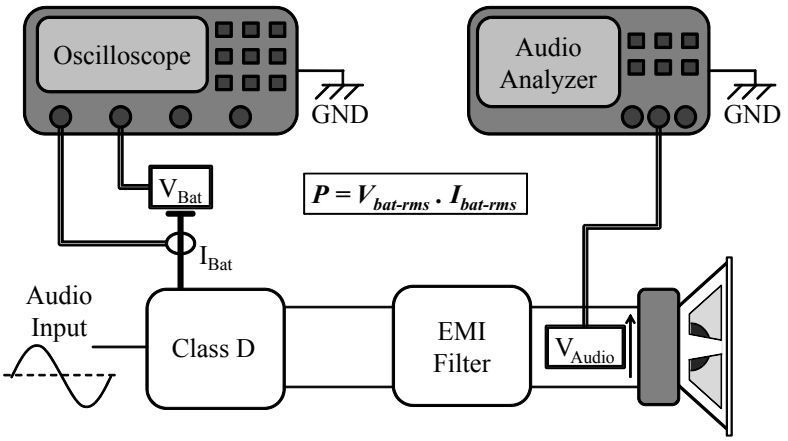


FIGURE 4.15: Bench set-up for the power measurements.

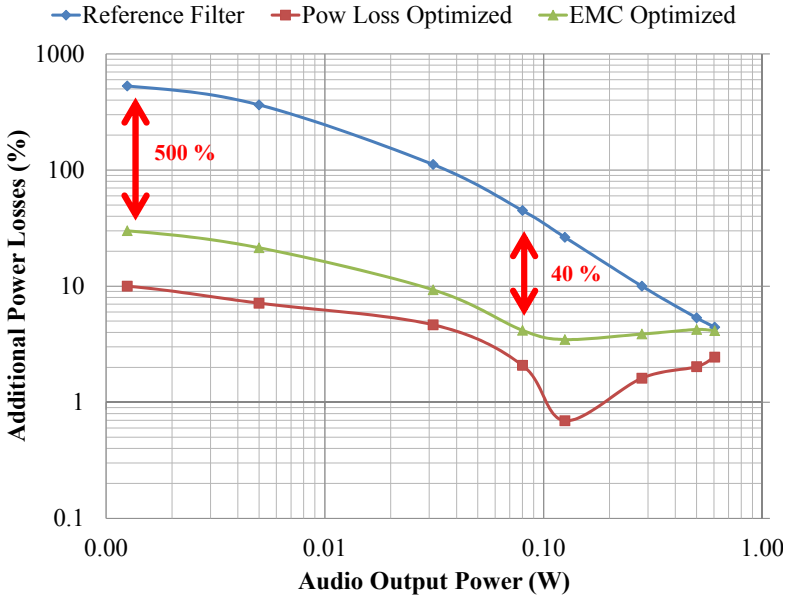


FIGURE 4.16: Power losses introduced by the different EMI filters.

axis, there are the percentage of the additional power loss compared to the no filter case and on the horizontal axis the audio power transmitted to the load. The power loss percentage is calculated using (4.12)

$$P_{comparison} = 100\frac{P_{Filter} - P_{No\,Filter}}{P_{No\,Filter}} \tag{4.12}$$

where P_{Filter} is the power consumption measured at the supply pin when using the EMI filter and $P_{No\,Filter}$ is that measured at the supply pin when no filter is used.

As can be seen in Fig. 4.16 the reference filter can introduce up to 500 % additional

power losses at low audio signal level when compared to the EMC optimized filter, and 520 % when compared to the power loss optimized filter. Thus, it can be deduced that the optimization is efficient and well-formulated, especially in the case of power loss optimization (formulation I). Finally, it can be deduced from Fig. 4.16 that the EMI filter provokes less power dissipation at high signal levels for a Class-D application. This can be explained by the fact that at a high signal level, which means high differential audio signal level, the output currents have less common modes. Thus, the common mode capacitors provoke less power losses as explained in subsection 4.3.2.

4.5 Chapter conclusion

To conclude, the frequency domain model presented and validated in chapter 3 has been implemented in an optimization loop based on a GA. The goal of the optimization is to automate the filter design procedure. By using the supplier passive component libraries, a database has been created to limit the search space to the available components on the market. Accordingly, the optimization results is a list of component references that allow us to obtain an optimal filtering solution with a predefined filter structure and layout.

The optimization has been applied on a Class-D amplifier for validation. We considered (i) the filter capability of reducing the conducted EM emissions, (ii) the additional power losses due to the EMI filter and (iii) the filter capability of transmitting the power to the load at the audio frequency. Two different formulations has been tested and validated experimentally.

In formulation I we aimed to minimize the power losses due to the EMI filter without decreasing the filter EMI performance compared to the reference one. Thus, the EMI has been set as goal and the power losses as constraint. As a result, the optimized filter reduced by more than five times the additional power losses caused by the reference filter. However, the studied spectrum peaks have been lowered at some frequencies and increased at others. Therefore, formulation II has been tested in order to improve the EMI response of the filter.

In formulation II the goal and constraint have been substituted. The optimization aimed then to reduce the EMI, without increasing the power losses. Here, we aimed to reduce the entire spectrum in order to improve the EMI in comparison with

the reference filter. However, similar to formulation I, the considered spectrum has also been lowered at some frequencies and increased at others. In this case, the power losses have been reduced by more than four times the additional power losses caused by the reference filter.

As a conclusion, in both formulations the additional power losses due to the EMI filter has been reduced. Thus, we can deduce that the power loss criterion has been properly formulated and can be efficiently optimized. However, this is not the case of the EMI criterion. In both formulations the EMI have been improved at up to $15\,MHz$ but worsened beyond this frequency. Thus, we deduce that the EMI criterion must be calculated differently. Therefore, we proposed another formulation for the EMI criterion which will be tested in the near future.

The filters obtained by both formulations have been tested experimentally in order to validate the reliability of the optimization. Afterwards, power and spectra measurements have been made and the results are presented and compared. The experimental results showed a good accordance with the simulations. The additional power losses due to the reference EMI filter have been divided by five which agree with the simulations. In addition, the output voltage spectra have showed about $20\,dB$ of peak reduction below $5\,MHz$ which also agree with the measurements. Thus, the developed optimization process is reliable even though the EMI criterion didn't led to the desired results.

Chapter 5

Impact of the EMI Filter on the Amplifier Base-Band

By adding an EMI filter to a system we prevent the EM perturbations from leaking out of or into the system. However, for Class-D amplifiers, this extra function is inserted at the output rails, thus, in the audio path. Here, a nonlinear behavior can have a negative impact on the amplifier quality. Therefore, the use of the EMI suppression components such as the ferrite beads or inductors with magnetic cores introduces additional distortion in the audio restitution chain. The occurring phenomenon is thus studied, modeled and evaluated in this chapter.

5.1 Ferrite beads and Class-D amplifiers

According to [124], the major difference between a ferrite bead and an inductor is the magnetic material, thus, the quality factor, thus, the dissipation capability. In addition, according to [125] (see Fig. 5.1), the bead impedance allow a broadband filtering effect compared to an inductor. Ferrite beads are mainly resistive at high frequencies, thus, they can dissipate the high frequency disturbances as heat (Fig. 5.1). Generally, for the integrated solutions and embedded systems, ferrite beads are frequently used because of their low price and small size. Thereby, in the rest of this chapter we consider ferrite beads, however, the same reasoning can be made for inductors with magnetic cores.

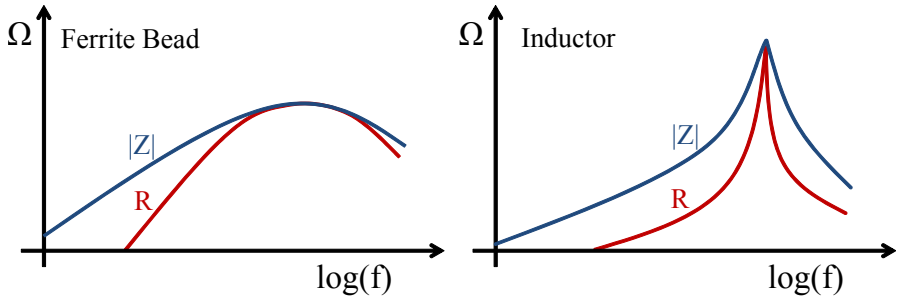


FIGURE 5.1: Ferrite bead impedance (inspired from [125]).

The magnetic material gives the ferrite bead a higher inductance when used in the inductive region (Fig. 5.1) and a higher dissipation capability when used for EMI suppression. However, due to its saturation and hysteresis characteristics, the magnetic material introduces a non-linear effect into the component behavior. Thus, when used with a Class-D amplifier, besides the EMI suppression capability, ferrite beads have a direct impact on the audio signal quality. To verify this issue, a measurement has been made on a given differential Class-D amplifier and it is described as follows. At the output of the Class-D amplifier we have connected two ferrite beads [126] (rated current of $1.3\,A$) as an EMI filter and an $8\,\Omega$ speaker load. Using an AA [127] connected to two measurement points; before and after the beads; we measured the bar-graph and the Total Harmonic Distortion (THD) for a $1\,kHz$ audio signal. The THD definition is given in appendix A. The output power and the audio voltage levels are equal to $100\,mW$ and $900\,mV$ respectively. Thus, the maximum output current is equal to $158\,mA$ which is lower than the component rated current. The results are shown in Fig. 5.2. Knowing that the ferrite beads were chosen for their low THD degradation, they increase the THD from $-69\,dB$ to $-53\,dB$ which is a significant audio quality degradation. Moreover, Fig. 5.2 shows an increase in the odd harmonics and slight variation in the even harmonics. This phenomenon has been barely studied in the literature and the ferrite bead suppliers do not provide the design engineers with the corresponding models. Because the distortion of switch mode audio power amplifiers can have different origins [44], appendix E shows some THD measurements with a linear amplifier which identify that this distortion mechanism is mainly a low frequency phenomenon occurring directly in the audio band and not a high frequency one folding into the audio band.

In previous work [44], the audio distortion of the filter inductors has been modeled.

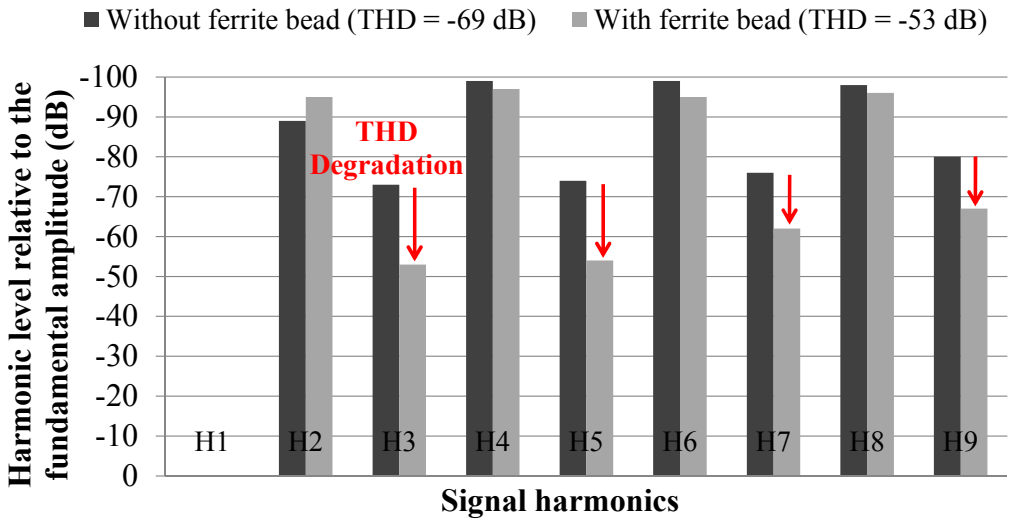


FIGURE 5.2: Example of Class-D THD and bargraph measurement. Note that, the more the bars are high the more the voltage is small since the scale is an inverted *dB* scale.

The authors measured the inductance declination in terms of the polarizing current. The Petersons coefficients corresponding to this declination are then included in the filter transfer function. This model consider then the saturation of the magnetic material, however, the hysteresis is not taken into account. Also, the model has been simulated for three different DUT, but not validated by experimental measurements.

By the authors best knowledge, apart [44], their is no other publications that study this phenomenon in the audio field. The most common model for ferrite beads is a linear one constructed by impedance matching [128, 129]. It is used for EMI simulations but is not able to predict the impact on audio signals. Many other papers deal with modeling the magnetic materials for power electronics issues, such as inductors [130], transformers [131, 132] or electric machines [133, 134]. Therefore, modeling these components for the purpose of audio simulations is a need in order to design EMI filters with a lower impact on audio distortion.

5.2 Ferrite bead modeling

Modeling a ferrite bead can be separated into two parts: magnetic material modeling and physical architecture modeling. Both are discussed in this section and a simulation is shown in order to explain the occurring phenomenon.

The most common magnetic material models including the hysteresis and saturation are:

- D. C. Jiles and D. L. Atherton model [135–137], known as the Jiles - Atherton (JA) model
- John Chan et al. model [138], known as the Chan et al. model
- Ferenc (Franz) Preisach model [139–141], known as the Preisach model
- C. D. Boley and M. L. Hodgdon [142], known as the Hodgdon model

In the present work, the JA and the Chan et al. models have been used due to their accuracy and practical implementation. In addition, they are widely used for ferrite materials [143]. However, only the results of the JA model are presented in this paper as the results from both models are similar. Thus, only an overview on the JA model is explained. Note that one of the possible implementations of the JA model can be found in [144].

5.2.1 Jiles - Atherton model

The JA model, in contrary to many other models in the literature, is based on a physical approach to describe the magnetic hysteresis loop [135]. The main idea behind it is to consider the energy related to the wall (known as Bloch wall) movements of the magnetic domains (known as Weiss Domains) inside a magnetic material. The hysteresis phenomenon is described as a friction force due to the wall movement during the magnetization process [144].

The JA model is related to two mechanisms. The first is the irreversible domain wall motion represented by M_{irr} $[A/m]$. The second is reversible domain wall bending represented by M_{rev} $[A/m]$. The magnetization M $[A/m]$ of the magnetic material can thus be given by (5.1).

$$M = M_{irr} + M_{rev} \tag{5.1}$$

M_{irr} and M_{rev} are described by (5.2) and (5.3), respectively.

$$\frac{\mathrm{d}M_{irr}}{\mathrm{d}H_e} = \frac{(M_{an} - M_{irr})}{k\delta} \tag{5.2}$$

$$M_{rev} = c(M_{an} - M_{irr}) \tag{5.3}$$

where, M_{an} $[A/m]$ is the anhysteretic magnetization given by (5.4). H_e $[A/m]$ is the effective magnetic field given by (5.5). k $[A/m]$ is a parameter linked to the coercive field. If H $[A/m]$ is the external magnetic field and t $[s]$ is the time, δ [dimensionless] would be equal to $+1$ if $\frac{dH}{dt} > 0$ and -1 if $\frac{dH}{dt} < 0$. Finally c [dimensionless] is the reversible coefficient.

$$M_{an}(H_e) = M_{sat}\left[\coth\left(\frac{H_e}{a}\right) - \left(\frac{a}{H_e}\right)\right] \tag{5.4}$$

$$H_e = H + \alpha M_{an} \tag{5.5}$$

with M_{sat} $[A/m]$ is the saturation magnetization, a $[A/m]$ is the shape parameter of M_{an} and α [dimensionless] is the domain interaction parameter.

Thus, (5.1) to (5.5) allow us to deduce the JA equation (5.6) that gives the variation of the magnetization M in terms of the magnetic field H.

$$\frac{dM}{dH} = \frac{(1-c)\frac{dM_{irr}}{dH_e} + c\frac{dM_{an}}{dH_e}}{1 - \alpha c\frac{dM_{an}}{dH_e} - \alpha(1-c)\frac{dM_{irr}}{dH_e}} \tag{5.6}$$

Finally, the magnetic induction B $[T]$ can be related to the magnetization M and the magnetic field H by (5.7)

$$B = \mu_0(H + M) \tag{5.7}$$

where $\mu_0 = 4\pi e^{-7}$ $[H/m]$ is the magnetic permeability of the vacuum.

Each magnetic material has its own hysteresis characteristics. Thus, JA allows us to configure the model for a given magnetic material using the 5 parameters α, a, k, c and M_{sat}. The determination of these parameters has been widely studied and discussed [145–147]. Table 5.1 gives some examples for 3 different magnetic materials [144].

5.2.2 Physical architecture modeling

The ferrite bead is an electric dipole. In the audio frequency band, it can be modeled as shown in Fig. 5.3. The resistor R_{DC} is the DC resistor of the component. The ferrite bead voltage can be then described by (5.8)

TABLE 5.1: JA parameters for three different magnetic materials [144]

Parameter	Ferrite N30	FeSi	Iron powder
α [dimensionless]	$9.77e^{-5}$	$1.31e^{-4}$	$1.83e^{-3}$
a $[A/m]$	20.25	59.5	1642
k $[A/m]$	55.75	99.2	1865
c [dimensionless]	0.9	0.54	0.8
M_{sat} $[A/m]$	$28.2e^4$	$11.5e^5$	$11.2e^5$

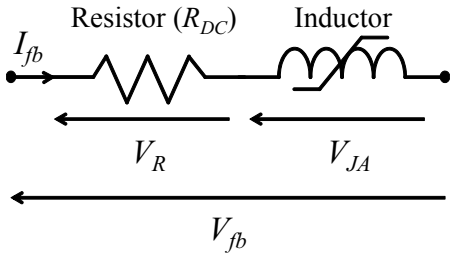


FIGURE 5.3: Ferrite bead model in the audio frequency band.

$$v_{fb}(t) = v_{JA}(t) + R_{DC} \cdot i_{fb}(t) \tag{5.8}$$

where the voltage $v_{JA}(t)$ is the inductive part of the component and can be related to the magnetic induction $B(t)$ using (5.9), $i_{fb}(t)$ is the component current and can be related to the magnetic field $H(t)$ using (5.10).

$$v_{JA}(t) = N \cdot S \cdot \frac{\mathrm{d}B(t)}{\mathrm{d}t} \tag{5.9}$$

$$i_{fb}(t) = \frac{L}{N} \cdot H(t) \tag{5.10}$$

where N is the coil number, S $[m^2]$ is the component effective section, L $[m]$ is the effective component length, and t is the time.

Finally, the relation between $B(t)$ and $H(t)$ given by the JA model, allows us to have the relation between $v_{JA}(t)$ and $i_{fb}(t)$.

This model is implemented and simulated in MATLAB environment. In order to expose the occurring phenomenon, a simulation example for a sinusoidal current and for a ferrite material (see the first column of Table 5.1) is presented. The hysteresis loop is shown in Fig. 5.4 and the voltage results are shown in Fig. 5.5. Note that, the model is validated with measurements in the next section.

As can be seen from Fig. 5.5, for a sinusoidal current, the product $R_{DC} \times I$ keeps the sinusoidal form due to its linearity. However, the hysteresis magnetic loop modeled by the JA model, generates peaks in the voltage V_{JA} (P_1 and P_2 in Fig. 5.5). These are caused by the slope variations in the hysteresis loop ($V_{JA} \propto \frac{\mathrm{d}B(t)}{\mathrm{d}t} \Rightarrow$ high slope $\Leftrightarrow$ high values of V_{JA}). The peaks occur at the current zero crossing (the same as H zero crossing according to equation (5.10)). Therefore, according to equation (5.8) the ferrite bead voltage is the sum of the two voltages V_{JA} and $R_{DC} \times I$. As a result, the ferrite bead voltage is a non-sinusoidal signal containing peaks at the zero crossing of the waveform. The next section shows that this distortion occurs in the audio frequency band and causes audio degradation.

5.3 Measurements and validation

5.3.1 Measurements

The ferrite bead cited in [148] has been used for measurements in order to validate the proposed model. Even though it has a low nominal current ($50\,mA$) which is lower than the usual one for Class-D amplifier applications, this component was chosen because it has a high internal DC resistance R_{DC} (maximum of $1.5\,\Omega$). This allows us to have a high voltage across the ferrite bead, allowing a better Signal to Noise Ratio (SNR) while measuring this voltage (V_{fb}). Notice that in industrial Class-D applications, ferrite beads are chosen with a lower internal DC resistance (around $50\,m\Omega$ for mobile phones) for better efficiency and a higher rated current (around $2\,A$ for mobile phones) for thermal reasons. Thus, it would be interesting to repeat the following work with an another ferrite bead (such as [126]) used in industrial applications, in order to quantify the real distortion caused by these components.

The chosen ferrite bead is mounted on a PCB with an $8\,\Omega$ load similar to a speaker. The schematic is shown in Fig. 5.6. The circuit is powered by a linear amplifier instead of a Class-D one. The main reason for this is to remove the high frequencies of a PWM spectrum and study the impact of the ferrite bead only in the audio frequency band. The signal generator delivers burst pulses of five sinusoidal periods with a frequency of $1\,kHz$. The pulses are separated by a delay of one second to avoid heating the component which would change the magnetic material characteristics. For $V_{in} = 1\,V$, the results of the ferrite bead voltage V_{fb} and current

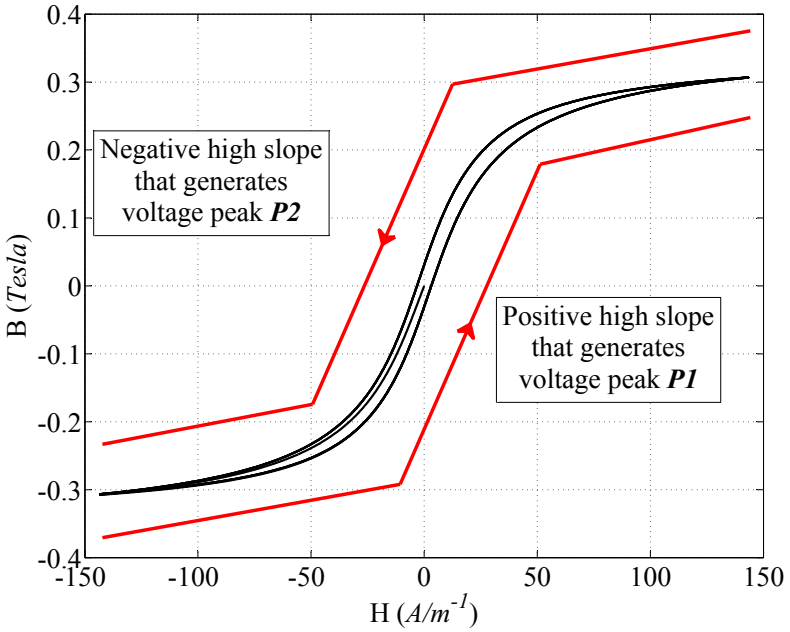


FIGURE 5.4: Hysteresis loop obtained by the JA model and the parameters of the first column in Table 5.1.

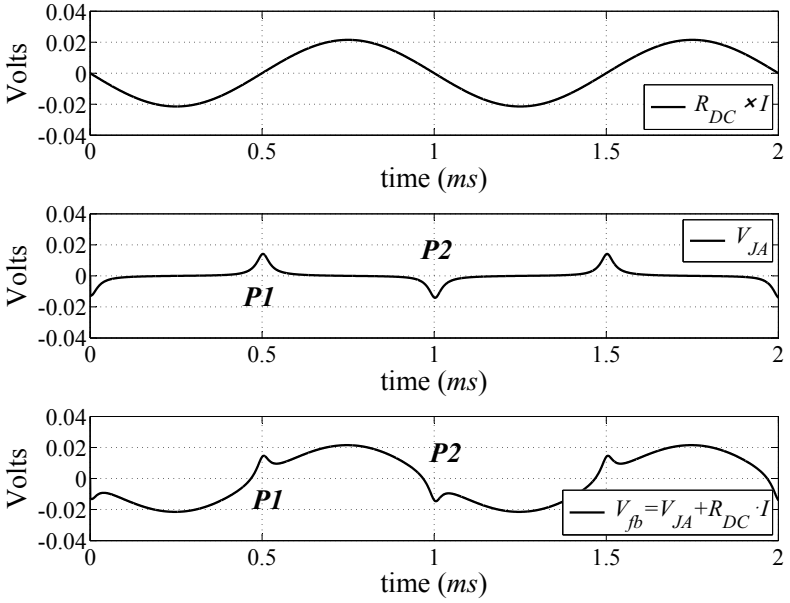


FIGURE 5.5: A simulation example showing the occurring phenomenon.

I are shown in Fig. 5.7. It shows a similar voltage behavior as the one obtained by simulation in Fig. 5.5. This proves that using this model is appropriate for these ferrite beads. Peaks appear at the zero crossing of the signals (around $0\,s$, $0.5\,ms$, $1\,ms$ and $1.5\,ms$). However, slight variations are also seen in the ferrite bead current at the same time as the voltage peaks.

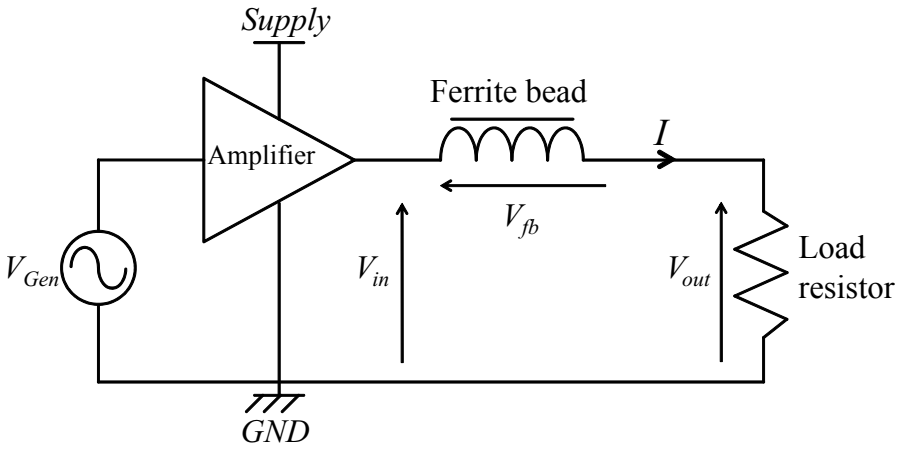


FIGURE 5.6: Measurement schematic.

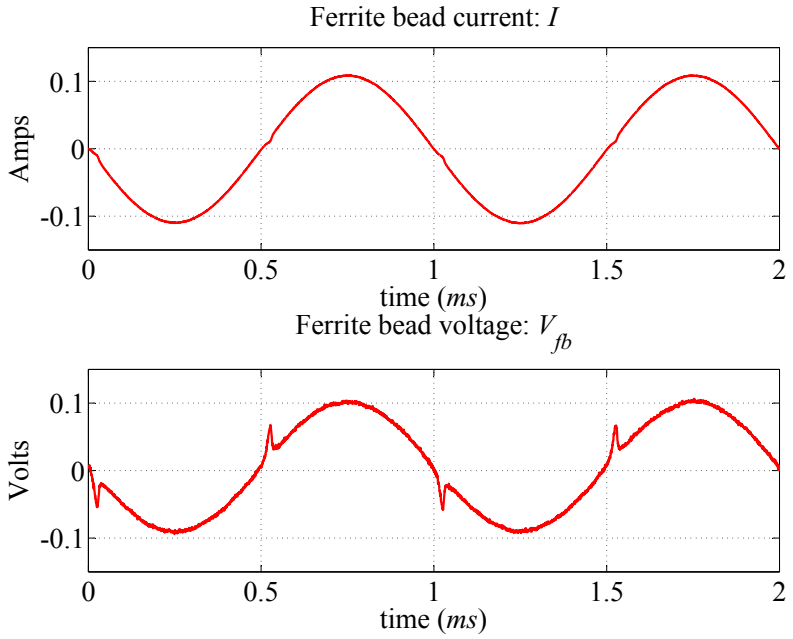


FIGURE 5.7: Measurement results.

5.3.2 Component parameter extraction

To model the ferrite bead [148] used for measurements, the following characteristics are needed: the DC resistance R_{DC}, coil number N, effective section S, effective length and the five parameters of the JA model that characterize the magnetic material. Nevertheless, this information is not given by the component supplier. Therefore, they are obtained as follows.

First, the DC resistance has been measured by an impedance analyzer, thus, $R_{DC} = 1\Omega$.

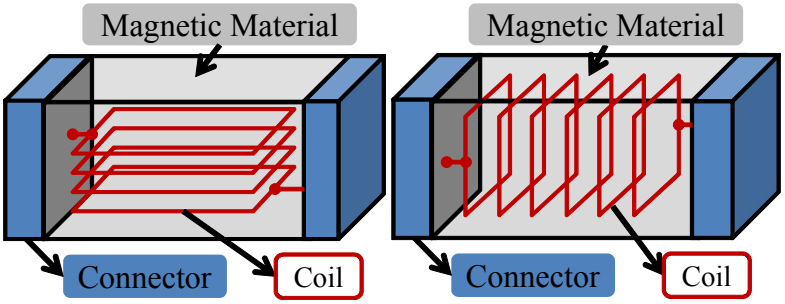


FIGURE 5.8: Ferrite bead physical architectures.

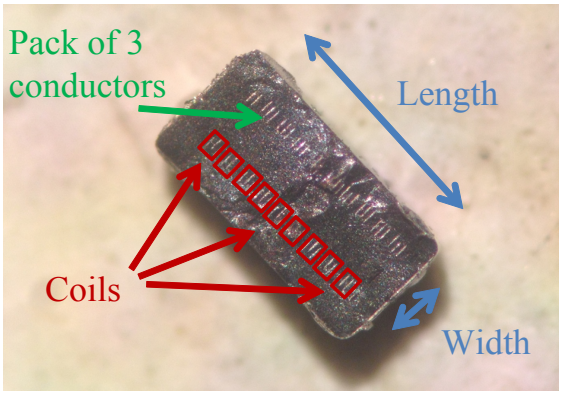


FIGURE 5.9: Ferrite bead broken in two part.

A ferrite bead is a coil developed inside a magnetic material as shown in Fig. 5.8. Thus, the component has been broken in two pieces and seen through a microscope. The picture is shown in Fig. 5.9, and we see that this ferrite bead has the same physical architecture as the right hand architecture in Fig. 5.8. The coil number is $N = 9$ and the coil conductor is a pack of 3 conductors in parallel. It can be seen as well that the effective length is almost that of the component itself and the effective width is almost half that of the component width. Therefore, as the chosen ferrite bead [148] is a 0603 (1608 in metric dimension) SMT package, then according to the data-sheet L and S are $1.6\,mm$ and $0.4 \times 0.4\,mm^2$, respectively. Note that, the effective section is considered as a square section.

The ferrite bead magnetic material reference and characteristics are not given by the supplier. Thus, the 5 parameters of the JA model[1] are unknown. As the material of the beads is ferrite, then to reduce the error due to the hysteresis loop characterization, the five JA parameters were assumed to be the same as

[1]The 3 parameters of the Chan et al. model [138] are also unknown. If the set of parameters for any of the model (JA or Chan et al.) are given, it is possible to compute the parameters of the other one by a parameter identification algorithm

those of known ferrite material found in [144] and presented in the first column of Table 5.1. In conclusion, the required characteristics and parameters for the ferrite bead modeling are summarized in Table 5.2.

TABLE 5.2: Parameters for the ferrite bead under test

Parameter	Value	**Parameter**	Value
α	$9.77e^{-5}$	N	9
a	$20.25\,A/m$	L	$1.6\,mm$
k	$55.75\,A/m$	S	$0.16\,mm^2$
c	0.9	R_{DC}	$1\,\Omega$
M_{sat}	$28.2e^4\,A/m$		

5.3.3 Time domain comparison

The specified model is now used for simulation in MATLAB. The ferrite bead and load are in series connected (see Fig. 5.6). The load has a higher impedance in the audio band and it is a linear component. As the current is imposed by the higher impedance which is the load, it can thus be considered as a perfect sinusoidal waveform. This can also be seen in Fig. 5.7 where the current has a slight variation on the zero crossings. This assumption can be particularly valid in industrial applications as the ferrite beads are chosen with lower DC resistance ($R_{DC} \ll R_{Load}$). The ferrite bead model is fed by a sinusoidal current with an amplitude given by (5.11)

$$I_{Peak} = \frac{V_{in}}{R_{DC} + R_{Load}} \tag{5.11}$$

where the peak value of V_{in} is equal to $1\,V$ similar to the measurements, $R_{Load} = 8.1\,\Omega$ is the measured load resistance and $R_{DC} = 1\,\Omega$. Thus, the amplitude of the simulation current is $0.11\,A$. The latter is higher then the maximum current given in the datasheet which is based on the thermal characteristics of the components. However, as the measurements were made using burst sinusoidal pulses, the thermal limits of the components are higher than for a $50\,mA$ DC current. A current amplitude of $0.11\,A$ is then valid. Therefore, this sinusoidal current feeds the model and generates the ferrite bead voltage which is compared to the measurement in Fig. 5.10. As a result, the simulations are in good agreement with the measurements. However, small differences are observed in the voltage curves.

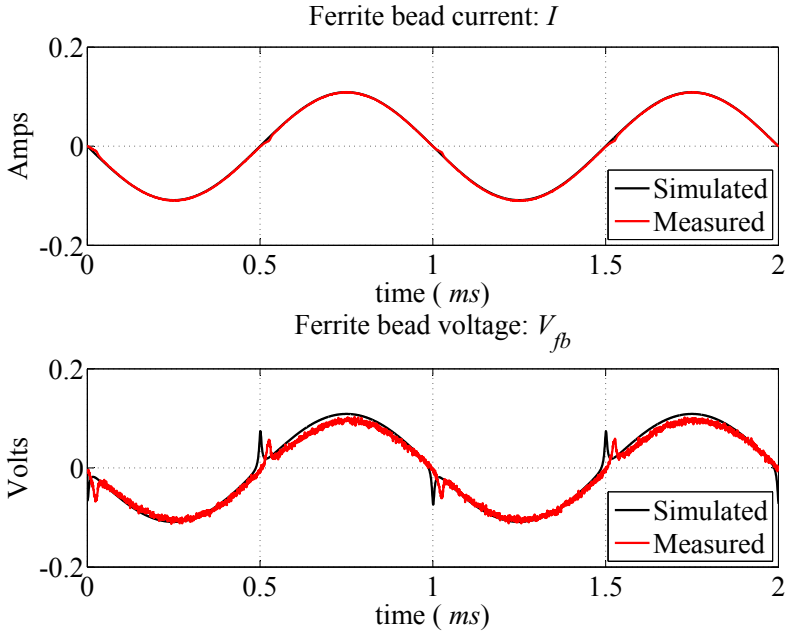


FIGURE 5.10: Ferrite bead current and voltage.

The reasons for this could be the measurement uncertainty or the JA parameters uncertainty which does not refer to the actual magnetic material.

From Fig. 5.6, the output voltage can be given by (5.12)

$$V_{out} = V_{in} - V_{fb} \tag{5.12}$$

Thus, the output voltage across the load contains variations at the zero crossings due to the peaks in the ferrite voltage. As the variations are small and not very visible, the time domain signals are not shown for the sake of simplification.

5.3.4 Frequency domain comparison

A Fast Fourier Transform (FFT) is applied to the time domain signals. The frequency domain results are shown in Fig. 5.11 and Fig. 5.12. Fig. 5.11 shows that the simulated ferrite bead voltage V_{fb} matches the measured one in the frequency domain. It therefore allows an accurate computation of the output voltage V_{out} which is shown in Fig. 5.12. We can see that the fundamental signal is located at $1\,kHz$ and the harmonics are spread over the audio frequency band. There is also an apparition in the odd harmonics of the output signal. This agrees with the case of a Class-D amplifier which is shown in Fig. 5.2. This can be explained

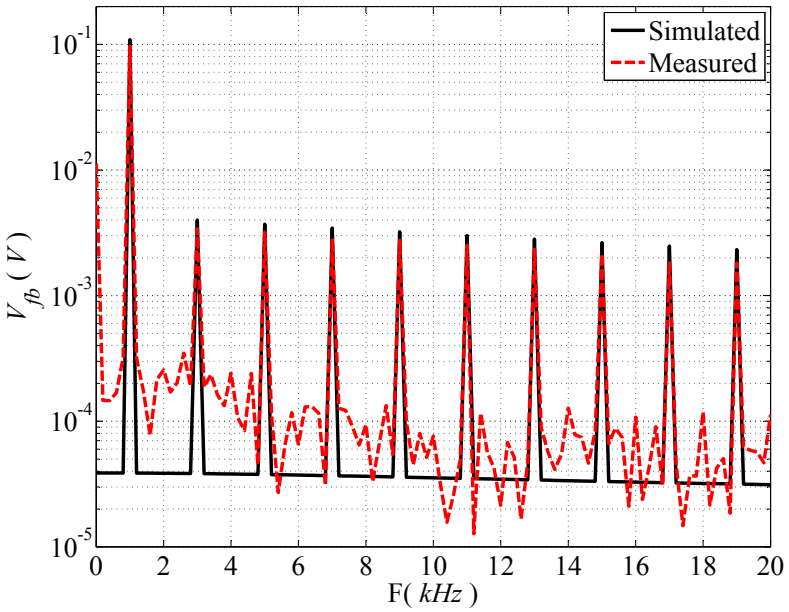


FIGURE 5.11: Measured and simulated ferrite bead voltage.

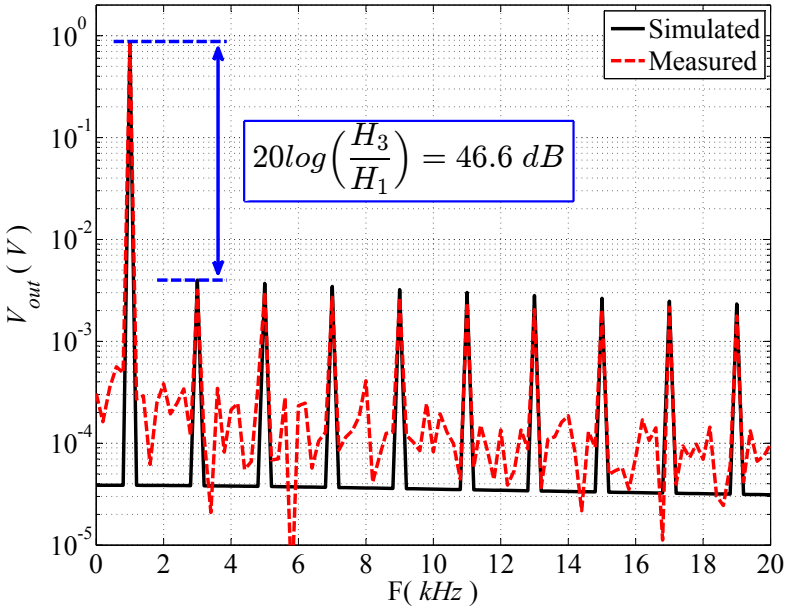


FIGURE 5.12: Measured and simulated output voltage.

by the fact that the hysteresis loop is symmetric around zero [46]. Moreover, the difference of the amplitude levels between the fundamental (H_1) and the third harmonic (H_3) is 46.6 dB which is the same order of magnitude as in the Class-D amplifier case (53 dB) shown in Fig. 5.2. From these results, we can deduce that the ferrite bead nonlinear behavior, due to the magnetic material, is a significant source of audio degradation in the Class-D amplification system.

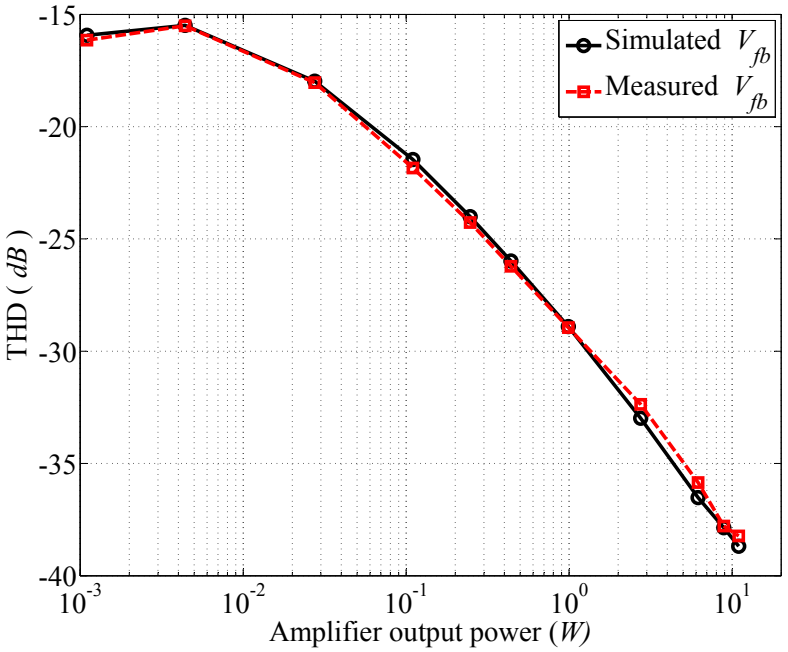


FIGURE 5.13: V_{fb} THD over the audio output power.

5.3.5 THD comparison

The THD is applied in order to characterize the linearity of the audio systems. Using the spectra presented in the previous subsection, it is possible to deduce the THD of the signals. Therefore, it is calculated on each amplitude level and compared to the measured THD.

The measurements performed on the circuit in Fig. 5.6 have been repeated, but with different V_{in} amplitude levels. Eleven voltage levels were chosen in the range of $[100\,mV; 10\,V]$ which correspond to the current levels in the range of $[10.98\,mA; 1.01\,A]$ and to the amplifier output power in the range of $[1.1\,mW; 11\,W]$. No points have been chosen below $100\,mV$ due to the low measurement SNR of V_{fb}. Two measurement points are taken below the component rated current, one point around the rated current and the rest is higher than the rated current. The THD has been calculated for V_{fb}, V_{out} and I at all the amplitudes, including the measured and simulated waveforms. In addition, the THD has been measured at V_{in} and V_{out} using an AA [127] in order to validate the THD calculation procedure. The THD plots over the amplifier output power are shown in Figs. 5.13, 5.14 and 5.15. Note that, the THDs for the simulated V_{in} and the simulated I are not shown because they are assumed to be perfect sinusoidal waves, thus, their THD in the dB scale tends toward $-\infty$.

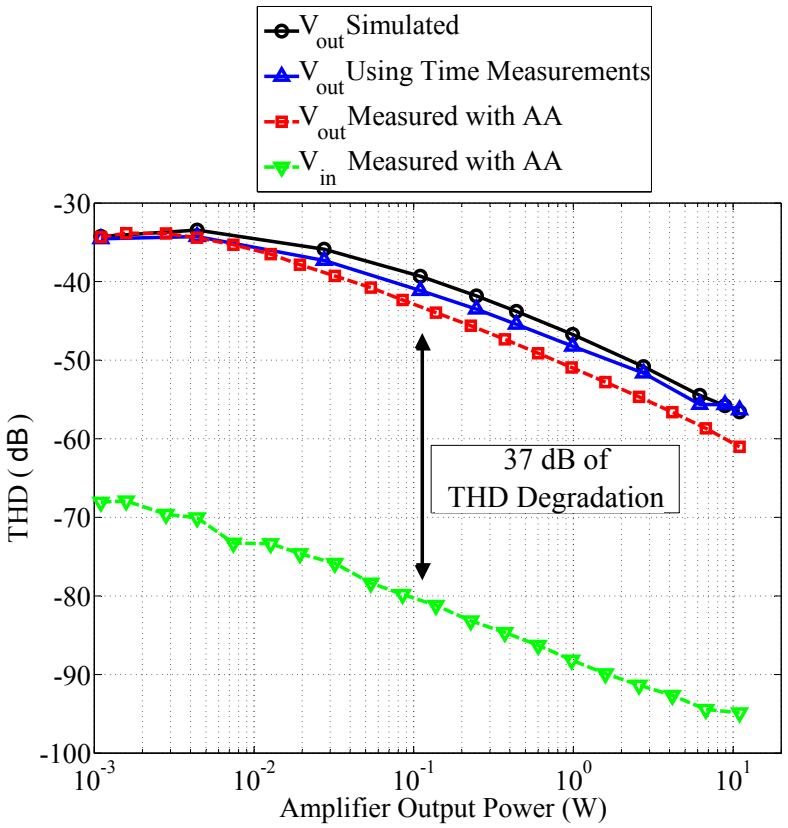


FIGURE 5.14: V_{in} and V_{out} THD over the audio output power.

Fig. 5.13 shows that the simulated THD of V_{fb} matches with the measured one at all the measuring points. Note that, the audio linearity is quantified by the output voltage THD and not the ferrite bead THD. However, the latter demonstrates that the ferrite bead model is accurate over a wide range of amplitudes. Moreover, a higher impact on the signal linearity can be seen in low signal levels than in high signal levels. This can be explained as follows: in V_{fb}, the linear part $R_{DC} \times I$ is greater at high signal levels than the nonlinear part V_{JA}, the signal has therefore a better linearity at high signal levels.

From Fig. 5.14, three conclusions can be made. First, the simulated THD of V_{out} is in a good agreement with both the THD measured using an AA and the THD calculated using the time domain measurements. Second, it shows an increase in the THD of V_{out} compared with the THD of V_{in}, which demonstrates that this ferrite bead is able to deteriorate the signal linearity up to $37\,dB$ for the amplifier in use. Third, even if the current is lower then the ferrite bead nominal current given by the supplier (which is $50\,mA$ in this case), the nonlinear behavior of the magnetic materials generates a significant distortion on the output audio signal.

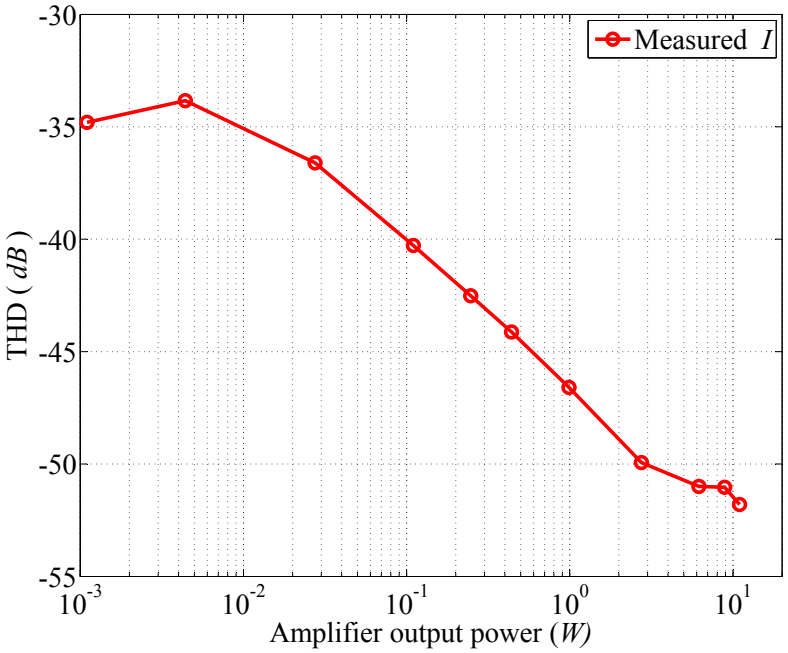


FIGURE 5.15: The current I THD over the audio output power.

For the present case, the rated current $50\,mA$ corresponds to an output power of $20\,mW$.

As the measurements in this paper have been made using a linear amplifier, it proves that the reason for audio degradation is mainly a low frequency phenomenon occurring in the audio frequency band.

Fig. 5.15 shows that the measured current has a noticeable THD which is not as visible in time domain signals. The shape of the current THD is similar to the one of the ferrite bead voltage which allows us to deduce that the current distortion is due to the magnetic materials. Therefore, if a high accuracy is needed from this simulation, the current should not be considered as a perfect sinusoidal waveform. However, this assumption can still be valid if the amplifier is a current source instead of voltage one [149].

In the integrated solutions, Class-D amplifiers are mostly differential systems. Their power stage is made by two switching cells that control the speaker. These generate opposite voltages which create the output audio signal across the speaker load. For such amplifiers, two ferrite beads are needed in the EMI filter. Thus, for the same current in the speaker, the amplifier can have double the effect observed in the case of a single ended amplifier.

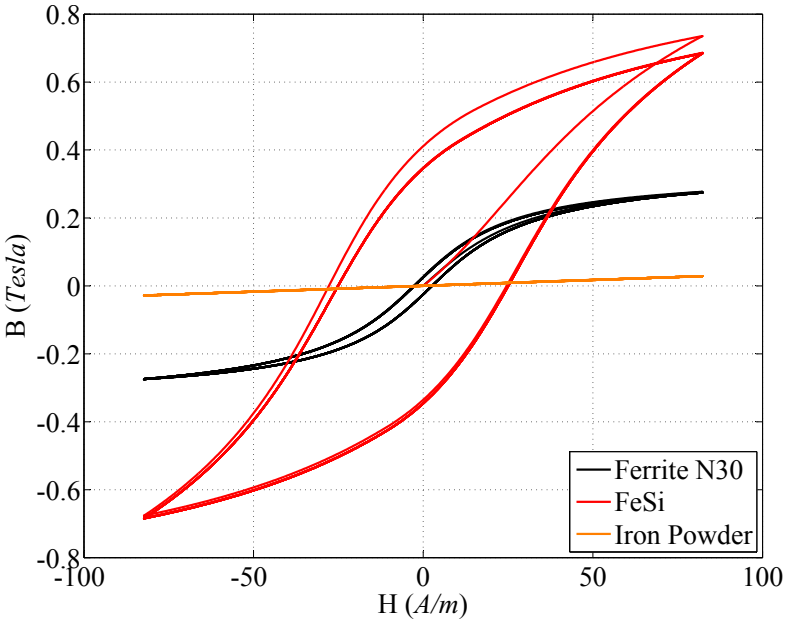


FIGURE 5.16: Hysteresis loops obtained by the JA model and the parameters of Table 5.1.

5.4 Simulating different magnetic materials in ferrite beads

Now that the model has been validated, it can be used for further simulations. What would it be the difference on the signal distortion if we change the magnetic material type? This section deals with this issues and answers this question by the following.

We considered the same ferrite bead [148] and schematic (Fig. 5.6) that we used in the previous sections. Afterwards, for a fixed voltage level on V_{in} equal to $100\,mV$ (which means a current of $11.1\,mA$), we changed the five parameters of the JA model in order to change the material type. Thus, we used the JA parameters of the "Ferrite N30", "Ferrosilicon (Fe-Si)" and "Iron Powder" materials which are available in Table 5.1. Fig. 5.16 starts by comparing the different hysteresis loops obtained by the different magnetic materials. We can see that for a magnetic field of $70\,A/m$ (the bead current is equal to $11.1\,mA$), the Ferrite N30 would be close to the saturation with $B = 0.268\,T$ (at the saturation $B \approx 0.3\,T$), the FeSi would not be saturated with $B = 0.63\,T$ (at the saturation $B \approx 1.3\,T$) and the Iron Powder would not be saturated and is at low magnetization levels with $B = 0.025\,T$ (at the saturation $B \approx 1.2\,T$). These hysteresis loops generate the

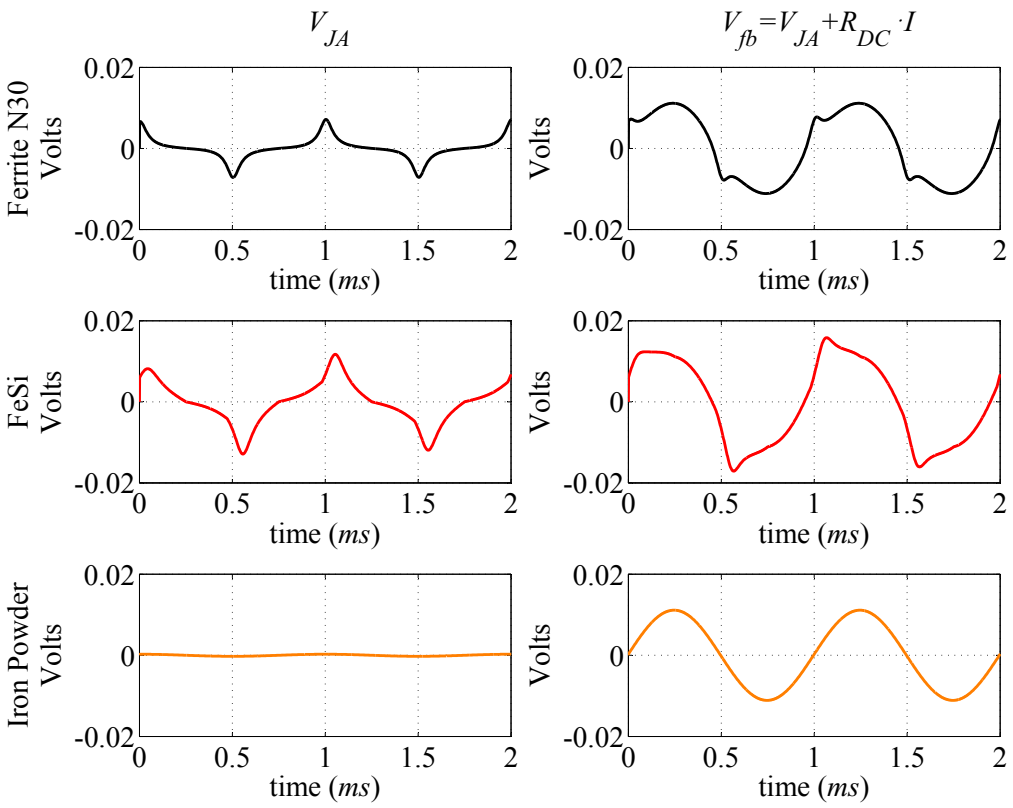


FIGURE 5.17: Bead simulations with the three materials of Table 5.1.

V_{JA} voltages presented in the first column of plots in Fig. 5.17, thus, the bead voltages presented in the second column of plots are obtained. As can be seen, the bead voltages are dissimilar if we change the type of the magnetic material. For a $11.1\,mA$ current, no peaks are observed at the zero crossing of the bead voltage when using the Iron Powder material, however, the peaks are observed in the case of the two other materials. Also, in the FeSi case, the peaks are bigger which must be due to the wider hysteresis loop (bigger coercivity H_c and bigger remnance B_r) compared to the one of the Ferrite N30. In the frequency domain the harmonic amplitudes are then different as shown in Fig. 5.18. In the case of Iron Powder with a low THD level of $-79.5\,dB$, no significant distortion is observed because no hysteresis or saturation are obtained at this current level. However, in the case of Ferrite N30 or FeSi, the hysteresis loop present in the $B(H)$ characteristic induce high level of distortion at the load. In particular, the wide hysteresis loop of the FeSi causes more audio distortion and it is marked with a higher THD of $-29.3\,dB$ compared to the one obtained with Ferrite N30 that generates $-32.7\,dB$ of THD.

We can then conclude that not only the saturation of the magnetic material causes

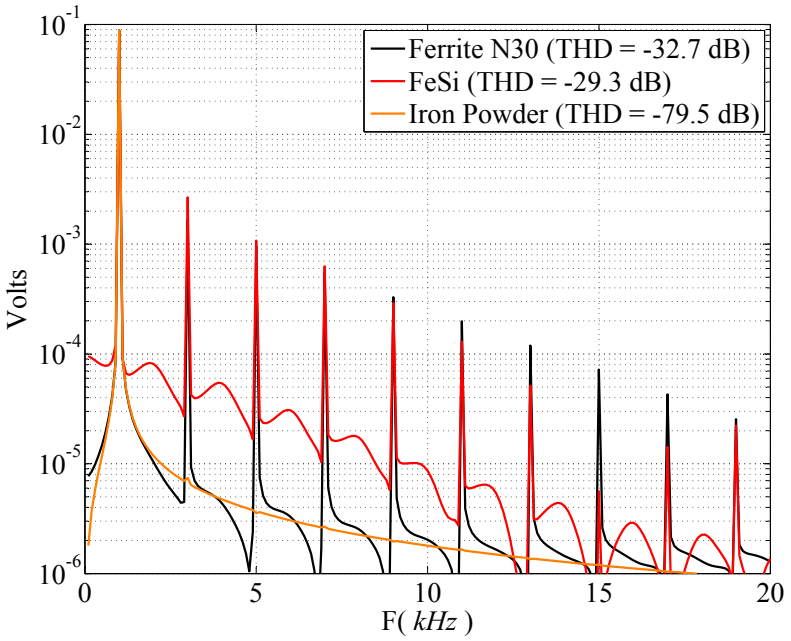


FIGURE 5.18: Frequency domain output voltages with the three materials of Table 5.1.

audio distortion, but also the hysteresis loop. Therefore, in order to obtain a correct audio distortion estimation, it is important to have a high accuracy in the magnetic material modeling. In addition, this section showed that using the magnetic material at low levels of magnetization have a low impact on the audio distortion because the nonlinearities are not present yet in the component behavior. It would be then interesting to test various ferrite material types and evaluate their impact on the audio distortion. However, the only JA parameters that were found in the literature are those of the Ferrite N30.

5.5 Chapter conclusion

To conclude, using the Jiles - Atherton model for magnetic materials and the component physical architecture, a ferrite bead model has been established. It allows us to simulate these components, also, to understand the occurring phenomenon when used in audio applications. The simulation of this model has been compared to a measured $1\,kHz$ sinusoidal signal for validation. The time domain results show the appearance of voltage peaks at the zero crossing of the ferrite bead current and the frequency domain results show an increase of the signal harmonics

all over the audio frequency band. We also observe an apparition of the odd harmonics in the case of a linear amplifier which agrees with the measurement on a Class-D amplifier. Moreover, the THD has been calculated for the simulated and measured signals. A comparison with the THD measurements using an AA shows good agreement over a wide range of amplitudes. The ferrite bead in use can generate up to $37\,dB$ of THD degradation in the audio signal. Finally, the developed model has been used in order to evaluate the impact of three different magnetic materials in the used ferrite bead. Here, we observed three different magnetic behavior that generated different THD levels at the load.

Thanks to this model, the audio system integrators are able to include the audio quality as a new criterion in the procedure of EMI filter design for switching amplifiers.

Chapter 6

Conclusion & Perspectives

6.1 General conclusion

The Class-D amplifiers are an interesting solution for embedded audio applications thanks to their high power efficiency. However, because of their switching nature, these have a high level of EM emissions which often leads to an inconformity with EMC standards or interferences with the surrounding electronics. Numerous circuit solutions have been developed in order to reduce Class-D emissions, nevertheless, EMI filters are still unavoidable. EMI filters are challenging to design because they are highly impacted by parasitic components. Generally, in industrial applications they are designed by expertise or by experimental tests which is not optimal. Therefore, a method or a tool that assist the system integrators in this task is needed. This work has focused then on three main research axes which are: (i) modeling a Class-D amplifier and predicting its conducted EM emissions, (ii) automating the filter design by using the modeling method in an optimization process and (iii) studying the impact of the EMI filter on the amplifier audio performance.

In order to predict the EMI behavior of a Class-D amplifier in the final application, a new modeling method in the frequency domain dedicated to circuits with N-active conductors has been developed in chapter 3. The main idea is to decompose the system into functional blocks. Here, we have on one hand the passive blocks which are modeled by impedance matrices and on the other hand the active ones which are modeled by electric sources and impedance matrices. Hence, by

using some matrix manipulations and calculations, we are able to obtain a compact model which can be used in system level simulation, also, to compute the current and voltage spectra at any node in the system. All the theory have been developed and presented, including three different method for impedance matrices determination that allow us to take into account the circuit imperfections. An experimental application is then carried out on two different cases of study which are a differential Class-D amplifier and a DC-DC converter. First, the Class-D audio amplifier case allowed the method validation on two active conductors up to $100\,MHz$. Second, the DC-DC converter case allowed the method validation for one active conductor. Moreover, in this case the converter was supplied by a battery. Thus, computing the noise spectrum required the knowledge of the battery impedance, Therefore, we proposed a new impedance measurement technique dedicated for batteries.

In chapter 4, the developed frequency model is implemented in an optimization loop. Thus, for a given Class-D amplifier, load and predefined filter structure and layout, the optimization find the optimal EMI filter components. The filter is modeled in ADS and the components are chosen from a sorted database that contains the libraries of components available on the market. As a result, the optimization generates a list of component references that refer to the optimal filter. The developed optimization process take into account the EMI attenuation, the power losses and the audio gain variation due to the EMI filter. Using two different formulations of these objectives, the optimization process has been applied twice on the used Class-D amplifier. In the first, we considered reducing the power losses as an objective and the two other criteria as constraints. In the second, we chose to optimize the EMI and we set the power losses and the audio gain criteria as constraints. As a result, the optimized filter reduced significantly the power losses in both formulations which prove the efficiency and the accuracy in describing this criterion. However, the EMI results were not as expected. The output spectrum peaks have been lowered only on the lower part of the considered frequency band (up to $20\,MHz$). Thus, we deduce that the EMI criterion was not properly formulated which led us to propose an alternative formulation. Finally, in this chapter, the optimized filters have been built then used for EMI and power measurements. The experimental results have showed a good agreement with the simulation which confirm the process reliability.

Generally, EMI filters are constituted of inductors with magnetic cores or ferrite

beads. These are nonlinear components that introduce additional distortion in the audio frequency band. Therefore, chapter 5 dealt with modeling the ferrite beads using the JA magnetic material model and the component physical architecture. The model allowed us to simulate, study and understand the occurring phenomenon, also, to compare the simulated signals to the measured one for validation. Finally, we deduced that the additional distortion due ferrite beads is a low frequency phenomenon occurring in the audio band. This can be seen in the time domain signals as voltages peaks around the current zero crossing, also, in the frequency domain by an increase of the odd harmonics. Finally, the THD of the audio signal has been computed for different amplitudes and compared to the THD measurements using an audio analyzer. These results prove the accuracy of the model over a wide range of amplitudes.

To sum up, a Class-D amplifier is used to amplify an audio signal with a high power efficiency, however, it has a high level of EM emissions. Thus, by using an EMI filter we attenuate the emissions but we increase the power losses and we reduce the audio quality. This work have treated these three aspects. Thus, we modeled accurately the system, we helped designing the EMI filter while taking into account the additional power losses and we studied the impact of the audio signal. As a conclusion, we dealt with all the objectives predefined for this work in section 1.3.

This work resulted in several publications which are listed in appendix G.

6.2 Perspectives

The investigations and research activities performed in this PhD thesis have released some ideas that could be interesting for further research topics and future works.

6.2.1 Speed of edge and EMI filters

In chapter 2 we explained that limiting the speed of edge can reduce the emissions of a Class-D amplifier. However, a longer edge time implies higher switching power losses. Also, EMI filters reduce the EMI and increase the power losses. Both

techniques are most of the time combined together in order to obtain the desired EMI response. However, many questions remain unanswered. Which technique can be more efficient in order to reduce EMI without increasing significantly the amplifier power losses? When using both techniques together, what will be the best trade-off in order to obtain the best EMI and power qualification?

The Class-D amplifier used in this work contains a feature in order to control the speed of edge. Therefore, by measuring the amplifier output voltages with different speeds of edge configurations, also, using the methods developed in chapter 3 and 4, this issue can be deeply investigated. It would be then interesting to publish the results in an application note or in the product datasheet.

6.2.2 Filter structure optimization and area on PCB reduction

In chapter 4 the EMI response and the power losses of the EMI filter has been optimized. However, the filter structure and layout have been predefined before the optimization. The components footprints are then fixed and unchangeable during the optimization. The only degree of freedom is the choice of components from the same package size. Therefore, it would be advantageous to consider the length of PCB tracks into the optimization. This allows more flexibility for choosing the components. Also, it allows us to reduce the overall area on PCB by reducing the package size and the track lengths. Moreover, it would be also advantageous to optimize the filter structure. For example, we can optimize an EMI filter with the minimum number of components, then, after a fixed number of iterations and if the conversion criteria are not met, the optimization process change the structure of the filter by introducing additional components in the structure. Afterwards, the optimization proceed again for choosing the component references. This process carry on until we meet the objectives or we attain the maximum number of components. Note that by reducing the number of components we can also reduce overall area on PCB.

6.2.3 On-chip coupling in differential Class-D amplifiers

The EMI modeling presented in [51] allows the estimation of conducted emissions caused by power electronic switchings. The model is based on configurable partial

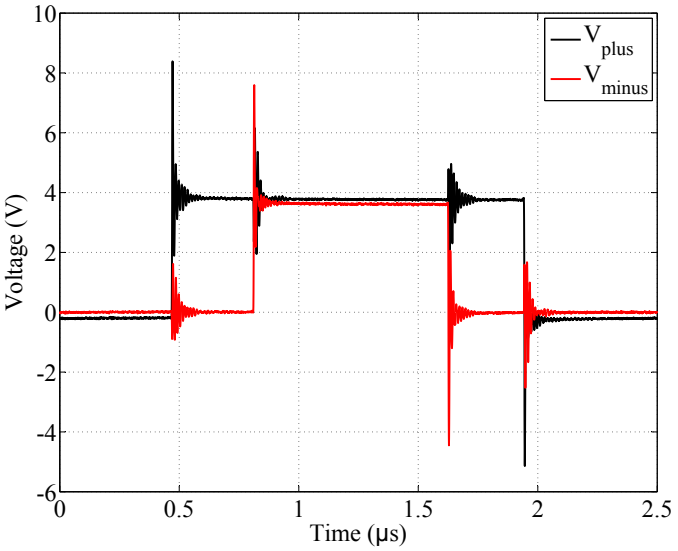


FIGURE 6.1: On-chip coupling.

transfer functions and it has been studied for a single switching cell. However, a differential Class-D amplifier has two switching cells in one power stage. On each switch of a cell, oscillations are induced in the voltage of the other cell. This can easily be seen in case of a ternary modulation because the switching cells do not switch at the same time. Fig. 6.1 shows a measured example on the Class-D amplifier used in chapter 3. Such oscillations can be caused by many factors such as the substrate coupling, on-chip crosstalk, common impedance, etc. Thus, for accurate EMI prediction in differential topologies the coupling between cells must be taken into account. For this purpose, preliminary simulation has been done which are presented by the following.

First, we considered a single switch in the time domain (Fig. 6.2) of both plus and minus signals of the power stage. Second, the FFT is used to transform the time domain signals into the frequency domain (Fig. 6.3). Hereafter, the transfer function (TF) is computed by dividing both signals in the frequency domain (Fig. 6.3). The same TF can be then used to estimate the induced voltage at other switching transitions using equation (6.1). Afterwards, the inverse FFT allows us to obtain the time domain signals.

$$V_{induced}(f) = TF \cdot V_{switch}(f) \tag{6.1}$$

where $V_{induced}$ is the induced voltage, TF is the transfer function and V_{switch} is the switching voltage.

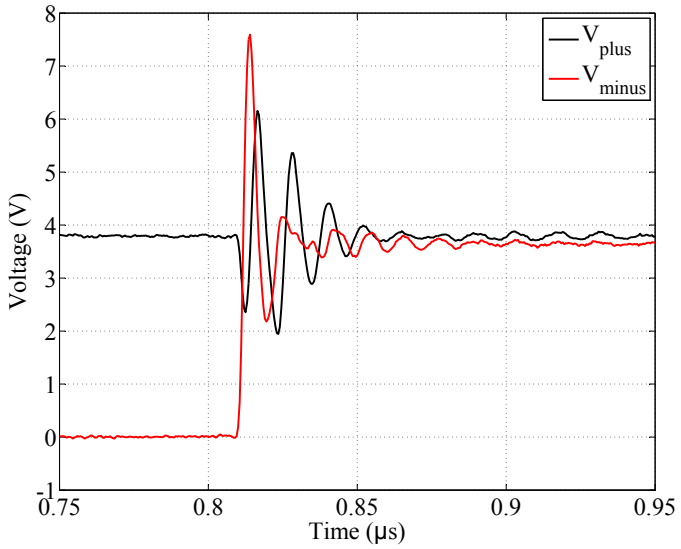


FIGURE 6.2: Single switch in the time domain.

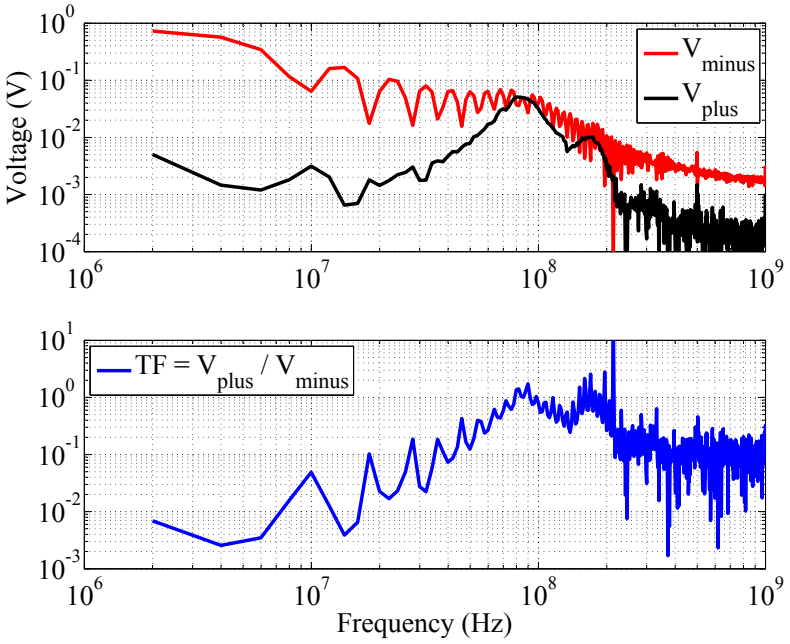


FIGURE 6.3: Single switch in the frequency domain.

Preliminary simulations have been done in order to evaluate this approach. The results presented in Fig. 6.4 and 6.5 shows good agreements between the measurements and simulations. Investigating this approach has stopped at these results, however, these are promising. Such an approach will allow us to obtain a frequency dependent TF that models the coupling between multi-channel converters.

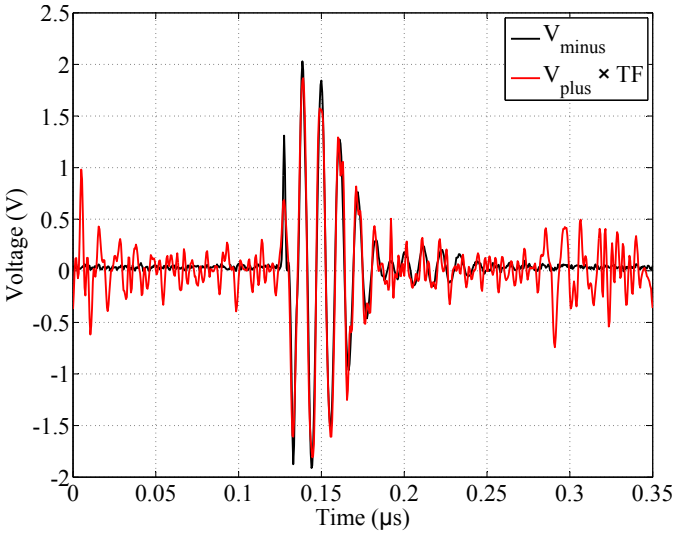


FIGURE 6.4: Coupling in case of a high to low transition.

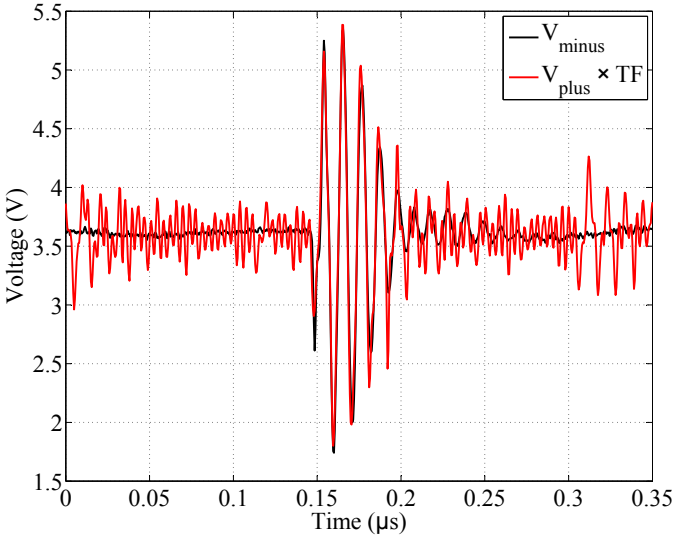


FIGURE 6.5: Coupling in case of a low to high transition.

6.2.4 Investigating the Schottky for free-wheeling diodes

According to [24] the reverse recovery of a MOSFET body diode is one of the causes for EM emissions in a Class-D amplifier. During the switching dead time and after blocking the low side transistor, the lower MOSFET body diode conducts the inductor current. When the high side MOSFET conducts, the low side body diode keep conducting in order to recover all the minority carriers. This reverse recovery current tend to have sharp and spiky shapes which lead to some additional EM emissions. Hence, the Schottky diode can be the key to stop these emissions. Shunting the MOSFET by a Schottky diode will allow us to avoid any conduction on the body diode. As the Schottky threshold voltage is lower than the one of

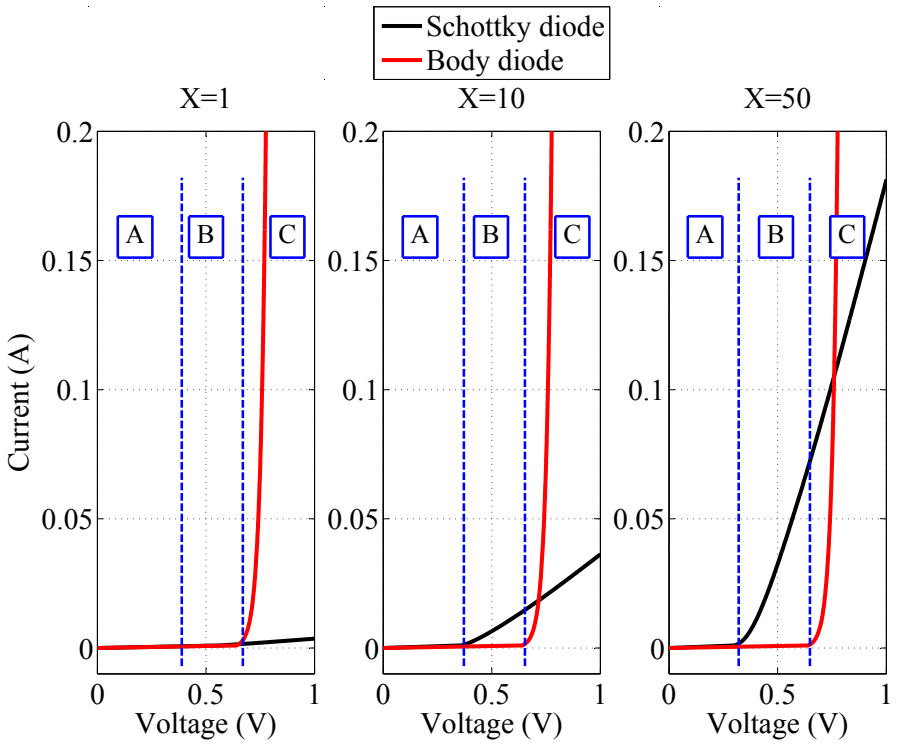


FIGURE 6.6: MOSFET body diode vs. Schottky diode.

a normal PN junction, the Schottky can be then used as the free-wheeling diode instead the body diode of the MOSFET, and thus, remove the reverse recovery current.

Preliminary simulations have been made in order to test the feasibility and the effectiveness of Schottky diodes in a Class-D amplifier power stage. Thus, we have simulated the I(V) characteristics of both diodes (MOSFET body and Schottky diodes). We considered a N-MOSFET and a Schottky diode having 40 % silicon area of the one of the MOSFET. By considering X the number that multiply the Schottky diode silicon area in order to change its characteristics, Fig. 6.6 shows the I(V) characteristics for both diodes for X=1, 10 and 50.

As can be seen from Fig. 6.6, by increasing the area of the Schottky diode we are able to reduce its resistance. In the A zone none of the diodes conducts, in the B zone the Schottky diode conducts and in the C zone both diodes conducts. Thus, by choosing the right Schottky area, we are able to prevent any conduction of the MOSFET body diode. However, in this case, if the needed current is about $10\,mA$ and above, the needed Schottky area is relatively high compared to the transistors which is not appropriate as it increases significantly the power stage cost. We continued our investigation and we discovered that the MOSFET body diode is

not properly modeled in the used design kit. This body diode characteristics are different from the reality. Thus, continuing this study with an accurate body diode model might lead for more interesting results.

6.3 Evaluating ferrite beads with a switching amplifier

Chapter 5 have studied the impact of EMI suppression components on the audio frequency band when used with audio amplifier. Thanks to a linear amplifier, we were able to focus only on the audio frequency band and remove the high frequency content of a Class-D amplifier. It would be then interesting to continue this investigation with a Class-D amplifier in order to identify if any phenomenon that occurs at the switching frequencies can affect the amplifier at any level. Here, the questions that could be answered are: Does the nonlinear high frequency phenomenon fold in the audio band? The losses in magnetic materials, are they significant compared to the losses of the EMI filter? Does the nonlinear behavior of magnetic material affect the EMI of Class-D amplifiers? For this purpose, the magnetic material model should be replaced by a dynamic one in order to consider the audio and the switching frequencies in the study.

Bibliography

[1] G.E. Moore. No exponential is forever: but "forever" can be delayed! [semiconductor industry]. In *Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 2003 IEEE International*, pages 20–23 vol.1, 2003. doi: 10.1109/ISSCC.2003.1234194.

[2] Federal Communication Commission. Understanding the FCC regulations for computers and other digital devices. Office of Engineering and Technology, 1993. Edited and reprinted February 1996.

[3] Tim Williams. *The Circuit Designer's Companion*. Elsevier, second edition, 2005. ISBN 0750663707.

[4] Wikipedia. List of EMC directives. URL http://en.wikipedia.org/wiki/List_of_EMC_directives.

[5] Henry W. Ott. *Noise Reduction Techniques in Electronic Systems*. Wiley-Interscience, second edition, 1988. ISBN 9780471850687.

[6] Karsten Nielsen. *Audio Power Amplifier Techniques With Energy Efficient Power Conversion*. PhD thesis, Department of Applied Electronics, Building 451, Technical University of Denmark, DK-2800 Lyngby, April 1998.

[7] M.A. Rojas-Gonzalez and E. Sanchez-Sinencio. Low-power high-efficiency class D audio power amplifiers. *Solid-State Circuits, IEEE Journal of*, 44 (12):3272–3284, 2009. ISSN 0018-9200. doi: 10.1109/JSSC.2009.2032729.

[8] Xin Ming, Zao Chen, Ze kun Zhou, and Bo Zhang. An advanced spread spectrum architecture using pseudorandom modulation to improve EMI in class D amplifier. *Power Electronics, IEEE Transactions on*, 26(2):638–646, 2011. ISSN 0885-8993. doi: 10.1109/TPEL.2010.2063440.

[9] Mei-Ling Yeh, Wan-Rone Liou, Hsiang-Po Hsieh, and Yu-Jei Lin. An electromagnetic interference (EMI) reduced high-efficiency switching power amplifier. *Power Electronics, IEEE Transactions on*, 25(3):710–718, 2010. ISSN 0885-8993. doi: 10.1109/TPEL.2009.2035622.

[10] F. Guanziroli, R. Bassoli, C. Crippa, D. Devecchi, and G. Nicollini. A 1 W 104 dB SNR filter-less fully-digital open-loop class D audio amplifier with EMI reduction. *Solid-State Circuits, IEEE Journal of*, 47(3):686–698, 2012. ISSN 0018-9200. doi: 10.1109/JSSC.2011.2178930.

[11] P. Balmelli, J.M. Khoury, E. Viegas, P. Santos, V. Pereira, J. Alderson, and R. Beale. A low-EMI 3-W audio class-D amplifier compatible with AM/FM radio. *Solid-State Circuits, IEEE Journal of*, 48(8):1771–1782, 2013. ISSN 0018-9200. doi: 10.1109/JSSC.2013.2259011.

[12] Richard Lee Ozenbaugh and Timothy M. Pullen. *EMI Filter Design*. CRC Press, third edition, 2011. ISBN 9781439844755.

[13] European Committee for Electrotechnical Standardization. Information technology equipment - Radio disturbance characteristics - Limits and method of measurement (CISPR 22:2005, modified). European Standard, 2006. Ref. EN 55022:2006 E.

[14] Federal Communications Commission (FCC). Rules & Regulations - Part 15 - Radio Frequency Devices - Subpart B - Unintentional Radiators. URL http://www.fcc.gov/.

[15] Ben Duncan. *High Performance Audio Power Amplifiers*. Newnes, Jordan Hill, Oxford OX2 8DP, 1996. ISBN 0750626291.

[16] M. Berkhout. Class-D audio amplifiers in mobile applications. In *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, pages 1169 –1172, may 2009. doi: 10.1109/ISCAS.2009.5117969.

[17] Rémy Cellier. *Controle et intégration d'amplificateurs de Classe-D à commande numérique pour la téléphonie mobile*. PhD thesis, Électronique Électrotechnique Automatique (EEA) doctoral school, July 2011.

[18] Shon-Hang Wen and Cheng-Chung Yang. A 5.2mW, 0.0016% THD up to 20kHz, ground-referenced audio decoder with PSRR-enhanced class-AB

16Ω; headphone amplifiers. In *VLSI Circuits (VLSIC), 2012 Symposium on*, pages 20–21, 2012. doi: 10.1109/VLSIC.2012.6243769.

[19] Joongsik Kih, Byungsoo Chang, and Deog-Kyoon Jeong. Class-AB large-swing CMOS buffer amplifier with controlled bias current. *Solid-State Circuits, IEEE Journal of*, 28(12):1350–1353, 1993. ISSN 0018-9200. doi: 10.1109/4.262009.

[20] E. Gaalaas. Class D Audio Amplifiers: What, Why, and How. In *Analog Dialogue*, Jun. 2006.

[21] G. Pillonnet, N. Abouchi, R. Cellier, and A. Nagari. A 0.01%THD, 70dB PSRR single ended class D using variable hysteresis control for headphone amplifiers. In *Circuits and Systems, 2009. ISCAS 2009. IEEE International Symposium on*, pages 1181–1184, 2009. doi: 10.1109/ISCAS.2009.5117972.

[22] K. I. Hwu and Y. T. Yau. Output power enhancement of single-ended class-D amplifier without DC blocking capacitor and negative voltage source required. In *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pages 1251–1256, 2009. doi: 10.1109/APEC.2009.4802824.

[23] D. Cartasegna, P. Malcovati, L. Crespi, K. Lee, L. Murukutla, and A. Baschirotto. An audio 91-dB THD third-order fully-differential class-D amplifier. In *ESSCIRC (ESSCIRC), 2011 Proceedings of the*, pages 91–94, 2011. doi: 10.1109/ESSCIRC.2011.6044922.

[24] Jun Honda and Jonathan Adams. Class D Audio Amplifier Basics. *International Rectifier: Application Note AN-1071*, 2005.

[25] Kyoungsik Kang, Jeongjin Roh, Youngkil Choi, Hyungdong Roh, Hyunsuk Nam, and Songjun Lee. Class-D audio amplifier using 1-bit fourth-order delta-sigma modulation. *Circuits and Systems II: Express Briefs, IEEE Transactions on*, 55(8):728–732, 2008. ISSN 1549-7747. doi: 10.1109/TCSII.2008.922457.

[26] Jinho Noh, Dongjun Lee, Jun-Gi Jo, and Changsik Yoo. A class-D amplifier with pulse code modulated (PCM) digital input for digital hearing aid. *Solid-State Circuits, IEEE Journal of*, 48(2):465–472, 2013. ISSN 0018-9200. doi: 10.1109/JSSC.2012.2224731.

[27] A. Nagari, E. Allier, F. Amiard, V. Binet, and C. Fraisse. An 8Ω ; 2.5W 1%-THD 104dB(A)-dynamic-range Class-D audio amplifier with an ultra-low EMI system and current sensing for speaker protection. In *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, pages 92 –94, feb. 2012. doi: 10.1109/ISSCC.2012.6176883.

[28] Chun Kit Lam, Meng Tong Tan, S.M. Cox, and Kiat Seng Yeo. Class-D amplifier power stage with PWM feedback loop. *Power Electronics, IEEE Transactions on*, 28(8):3870–3881, 2013. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2230027.

[29] Harold S. Black. *Modulation theory*. Van Nostrand, 1953.

[30] P.H. Mellor, S. P. Leigh, and B.M.G. Cheetham. Reduction of spectral distortion in class D amplifiers by an enhanced pulse width modulation sampling process. *Circuits, Devices and Systems, IEE Proceedings G*, 138(4): 441–448, 1991. ISSN 0956-3768.

[31] Gaël Pillonnet. *Intégration d'une chaîne de conversion digitale analogique utilisant la modulation à largeur d'impulsion pour la téléphonie mobile*. PhD thesis, Électronique Électrotechnique Automatique (EEA) doctoral school, november 2007.

[32] G. Pillonnet, R. Cellier, E. Allier, N. Abouchi, and A. Nagari. A topological comparison of PWM and hysteresis controls in switching audio amplifiers. In *Circuits and Systems, 2008. APCCAS 2008. IEEE Asia Pacific Conference on*, pages 668–671, 2008. doi: 10.1109/APCCAS.2008.4746112.

[33] A. Huffenus, G. Pillonnet, N. Abouchi, F. Goutti, V. Rabary, and C. Specq. A phase-shift self-oscillating stereo class-D amplifier for battery-powered applications. In *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pages 769–772, 2010. doi: 10.1109/ISCAS.2010.5537458.

[34] S-E Adami, R. Mrad, F. Morel, C. Vollaire, G. Pillonnet, and R. Cellier. Conducted EMI of integrated switching audio amplifier for mobile phone applications. In *Electromagnetic Compatibility of Integrated Circuits (EMC Compo), 2011 8th Workshop on*, pages 142–147, Nov 2011.

[35] Johannes Huchzermeier. Comparison of electromagnetic interference potential of integrated logic circuits AVC, GTLP, BTL, and LVDS. *Texas Instruments: Application Report*, 2001.

[36] Andreas Karvonen. *MOSFET Modeling Aimed at Minimizing EMI in Switched DC/DC Converters Using Active Gate Control.* PhD thesis, Chalmers University of Technology, Spring 2009.

[37] Clayton R. Paul. *Introduction to Electromagnetic Compatibility.* Wiley-Interscience, second edition, 2006.

[38] Haishi Wang, Bo Zhang, Jiang Sun, and Rui Wang. Application of spread spectrum for EMI reduction in class D amplifier. In *Solid-State and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*, pages 129–131, 2010. doi: 10.1109/ICSICT.2010.5667827.

[39] Xicheng Jiang, Jungwoo Song, Darwin Cheung, Minsheng Wang, and Sasi Kumar Arunachalam. An 8Ω, 1.75W, 95% efficiency, 0.004% THD+N class-D amplifier with a feed-forward ADC and feedback filters. In *Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian*, pages 369–372, 2013. doi: 10.1109/ASSCC.2013.6691059.

[40] J. Biela, A. Wirthmueller, R. Waespe, M.L. Heldwein, K. Raggl, and J.W. Kolar. Passive and active hybrid integrated EMI filters. *Power Electronics, IEEE Transactions on*, 24(5):1340–1349, 2009. ISSN 0885-8993. doi: 10.1109/TPEL.2009.2012404.

[41] Wenjie Chen, Xu Yang, and Zhaoan Wang. An active EMI filtering technique for improving passive filter low-frequency performance. *Electromagnetic Compatibility, IEEE Transactions on*, 48(1):172–177, 2006. ISSN 0018-9375. doi: 10.1109/TEMC.2006.870803.

[42] Michael A.E. Andersen, Arnold Knott, and Gerhard Pfaffinger. Multi carrier modulator for switch-mode audio power amplifiers. In *Audio Engineering Society Convention 124*, May 2008. URL http://www.aes.org/e-lib/browse.cfm?elib=14569.

[43] Theis Christiansen, Toke Andersen, Arnold Knott, Michael A. E. Andersen, and Gerhard Pfaffinger. Multi-carrier modulation audio power amplifier with programmable logic. In *Audio Engineering Society Conference: 37th*

International Conference: Class D Audio Amplification, Aug 2009. URL http://www.aes.org/e-lib/browse.cfm?elib=15227.

[44] Arnold Knott, Tore Stegenborg-Andersen, Ole C. Thomsen, Dominik Bortis, Johann W. Kolar, Gerhard Pfaffinger, and Michael A. E. Andersen. Modeling distortion effects in class-D amplifier filter inductors. In *Audio Engineering Society Convention 128*, May 2010. URL http://www.aes.org/e-lib/browse.cfm?elib=15294.

[45] Y. Onikienko, V. Pilinsky, D. Probity, and V. Shvaychenko. Simulation of electromagnetic environment of class D amplifier. In *Electronics and Nanotechnology (ELNANO), 2013 IEEE XXXIII International Scientific Conference*, pages 396–398, 2013. doi: 10.1109/ELNANO.2013.6552061.

[46] Bob Metzler. *Audio Precision Handbook*. Audio Precision, Inc., second edition, 2005.

[47] Eric Sturtzer. *Modélisation en vue de l'intégration d'un système audio de micro puissance comprenant un haut-parleur MEMS et son amplificateur*. PhD thesis, Électronique Électrotechnique Automatique (EEA) doctoral school, April 2013.

[48] Arnold Knott. *Improvement of out-of-band Behaviour in Switch-Mode Amplifiers and Power Supplies by their Modulation Topology*. PhD thesis, Technical University of Denmark, August 2010.

[49] E. Rondon-Pinilla, F. Morel, C. Vollaire, and J.-L. Schanen. Modeling of a buck converter with a SiC JFET to predict EMC conducted emissions. *Power Electronics, IEEE Transactions on*, 29(5):2246–2260, May 2014. ISSN 0885-8993. doi: 10.1109/TPEL.2013.2295053.

[50] O.A. Mohammed and S. Ganu. FE-circuit coupled model of electric machines for simulation and evaluation of EMI issues in motor drives. *Magnetics, IEEE Transactions on*, 46(8):3389–3392, Aug 2010. ISSN 0018-9464. doi: 10.1109/TMAG.2010.2045746.

[51] S. Hrigua, F. Costa, C. Gautier, and B. Revol. New modeling method based on transfer functions for EMI analysis in power electronic converters. In *Electromagnetic Compatibility (EMC EUROPE), 2012 International Symposium on*, pages 1–6, Sept 2012. doi: 10.1109/EMCEurope.2012.6396839.

[52] P. Musznicki, J.-L. Schanen, B. Allard, and P.J. Chrzan. Accurate modeling of layout parasitic to forecast emi emitted from a dc-dc converter. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 1, pages 278–283 Vol.1, June 2004. doi: 10.1109/PESC.2004.1355756.

[53] A. Hassan, S. Schulze, M. Al-Hamid, and R. Vick. Prediction of the resonance effect of the common mode noise of SMPS. In *EMC Europe 2011 York*, pages 707–711, Sept 2011.

[54] J.-R. Regue, M. Ribo, D. Duran, D. Badia, and A. Perez. Common and differential mode characterization of EMI power-line filters from S-parameters measurements. In *Electromagnetic Compatibility, 2004. EMC 2004. 2004 InternationalSymposium on*, volume 2, pages 610–615 vol.2, Aug 2004. doi: 10.1109/ISEMC.2004.1349868.

[55] Junsheng Wei, D. Gerling, and M. Galek. S-parameters characterization and sequence model of three-phase EMI filter. In *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, pages 1254–1259, Nov 2013. doi: 10.1109/IECON.2013.6699312.

[56] J.H. Hagmann and S. Dickmann. Determination of mode conversion on differential lines. In *Electromagnetic Compatibility - EMC Europe, 2008 International Symposium on*, pages 1–5, Sept 2008. doi: 10.1109/EMCEUROPE.2008.4786825.

[57] Jin Meng, Xiangming Zhang, Anqi Hu, Lei Zhang, and Weiming Ma. Transfer network models for EMI coupling paths characterization of multiconductor cables. In *Electromagnetic Compatibility (APEMC), 2010 Asia-Pacific Symposium on*, pages 301–304, April 2010. doi: 10.1109/APEMC.2010.5475779.

[58] M. Foissac, J.-L. Schanen, and C. Vollaire. "black box" EMC model for power electronics converter. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 3609–3615, Sept 2009. doi: 10.1109/ECCE.2009.5316113.

[59] M. Foissac, J. Schanen, G. Frantz, D. Frey, and C. Vollaire. System simulation for EMC network analysis. In *Applied Power Electronics Conference*

and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE, pages 457–462, March 2011. doi: 10.1109/APEC.2011.5744636.

[60] D. Labrousse, B. Revol, and F. Costa. Common-mode modeling of the association of N -switching cells: Application to an electric-vehicle-drive system. *Power Electronics, IEEE Transactions on*, 25(11):2852–2859, Nov 2010. ISSN 0885-8993. doi: 10.1109/TPEL.2010.2051457.

[61] F. Costa, C. Vollaire, and R. Meuret. Modeling of conducted common mode perturbations in variable-speed drive systems. *Electromagnetic Compatibility, IEEE Transactions on*, 47(4):1012–1021, Nov 2005. ISSN 0018-9375. doi: 10.1109/TEMC.2005.857365.

[62] C. Jettanasen, F. Costa, and C. Vollaire. Common-mode emissions measurements and simulation in variable-speed drive systems. *Power Electronics, IEEE Transactions on*, 24(11):2456–2464, Nov 2009. ISSN 0885-8993. doi: 10.1109/TPEL.2009.2031493.

[63] R. De Maglie, M. Nuber, J. Engstler, and A. Engler. Common mode current calculation in a driver stage for power semiconductor modules. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–8, Sept 2013. doi: 10.1109/EPE.2013.6631731.

[64] J. Espina, J. Balcells, A. Arias, C. Ortega, and N. Berbel. EMI model of an AC/AC power converter. In *Vehicle Power and Propulsion Conference (VPPC), 2010 IEEE*, pages 1–6, Sept 2010. doi: 10.1109/VPPC.2010.5729193.

[65] J. Espina, J. Balcells, C. Ortega, A. Arias, L. De Lillo, and L. Empringham. Common mode model of matrix converter. In *Compatibility and Power Electronics (CPE), 2011 7th International Conference-Workshop*, pages 289–294, June 2011. doi: 10.1109/CPE.2011.5942247.

[66] F. Grassi, S.A. Pignari, and J. Wolf. Channel characterization and EMC assessment of a PLC system for spacecraft DC differential power buses. *Electromagnetic Compatibility, IEEE Transactions on*, 53(3):664–675, Aug 2011. ISSN 0018-9375. doi: 10.1109/TEMC.2011.2125967.

[67] Kye-Yak See and Junhong Deng. Measurement of noise source impedance of SMPS using a two probes approach. *Power Electronics, IEEE Transactions*

on, 19(3):862–868, May 2004. ISSN 0885-8993. doi: 10.1109/TPEL.2004.826520.

[68] V. Tarateeraseth, Kye Yak See, F.G. Canavero, and R.W. Chang. Systematic electromagnetic interference filter design based on information from in-circuit impedance measurements. *Electromagnetic Compatibility, IEEE Transactions on*, 52(3):588 –598, aug. 2010. ISSN 0018-9375. doi: 10.1109/TEMC.2010.2046419.

[69] C. Lochot and J. Levant. ICEM: a new standard for EMC of IC definition and examples. In *Electromagnetic Compatibility, 2003 IEEE International Symposium on*, volume 2, pages 892–897 vol.2, Aug 2003. doi: 10.1109/ISEMC.2003.1236727.

[70] M. Ramdani, J. Levant, and R. Perdriau. ICEM model extraction: a case study. In *Electromagnetic Compatibility, 2004. EMC 2004. 2004 InternationalSymposium on*, volume 3, pages 969–973 vol.3, Aug 2004. doi: 10.1109/ISEMC.2004.1349957.

[71] J. Levant, M. Ramdani, R. Perdriau, and M. Drissi. EMC assessment at chip and PCB level: Use of the ICEM model for jitter analysis in an integrated PLL. *Electromagnetic Compatibility, IEEE Transactions on*, 49(1):182–191, Feb 2007. ISSN 0018-9375. doi: 10.1109/TEMC.2006.888181.

[72] Junichi Miyashita, Masayuki Mitsuzawa, Toshiyuki Karube, Kiyohito Yamasawa, and Toshiro Sato. Measurement of the source impedance of conducted emission using mode separable LISN: Conducted emission of a switching power supply. *Electrical Engineering in Japan*, 139(2):72–78, 2002. ISSN 1520-6416. doi: 10.1002/eej.1154. URL http://dx.doi.org/10.1002/eej.1154.

[73] K. Iokibe, R. Higashi, T. Tsuda, K. Ichikawa, K. Nakamura, Y. Toyota, and R. Koga. Modeling of microcontroller with multiple power supply pins for conducted EMI simulations. In *Advanced Packaging and Systems Symposium, 2008. EDAPS 2008. Electrical Design of*, pages 135–138, Dec 2008. doi: 10.1109/EDAPS.2008.4736018.

[74] K. S. Suresh Kumar. *Electric Circuits and Networks*. Dorling Kindersley India, 2009. ISBN 978-81-317-1390-7.

[75] ADS Advenced Design System. Accessed: 10/03/2014.

[76] David M. Pozar. *Microwave Engineering*. John Wiley & Sons, fourth edition, 2012. ISBN 978-0-470-63155-3.

[77] Agilent. Advanced impedance measurement capability of the RF I-V method compared to the network analysis method. Technical Report Application Note 1369-2, Agilent Technologies, Jul. 2001.

[78] Agilent. Ultra-Low Impedance Measurements Using 2-Port Measurements. Technical Report Application Note 5989-5935EN, Agilent Technologies, Feb. 2007.

[79] Frederic Lafon. *Techniques and methodologies development to take into account EMC constraints in Automotive equipment design*. PhD thesis, INSA de Rennes, 2011.

[80] Xiaoning Ye. De-embedding errors due to inaccurate test fixture characterization. *Electromagnetic Compatibility Magazine, IEEE*, 1(4):75 –78, quarter 2012. ISSN 2162-2264. doi: 10.1109/MEMC.2012.6397064.

[81] Moises Ferber, Christian Vollaire, Laurent Krahenbuhl, Jean-Louis Coulomb, and Joao A. Vasconcelos. Conducted interferences of power converters with parametric uncertainties in the frequency domain. In *Electromagnetic Compatibility (APEMC), 2012 Asia-Pacific Symposium on*, pages 681 –684, may 2012. doi: 10.1109/APEMC.2012.6237869.

[82] 2403 260 00001, 15 × 11 × 3.5 MM RA speaker data sheet. URL http://www.knowles.com/. Accessed: 18/02/2014.

[83] Texas Instruments. *AN-1497 Filterless Class D Amplifiers*. Application Note 1497. May 2006.

[84] MAXIM : MAX9700B Evaluation Kit. URL http://www.maxim-ic.com/products/audio/. Accessed: 18/02/2014.

[85] MEGATRON, NXP Speaker RA11x15x3.5. URL http://www.megatron.ch/en/oem-quality-loudspeakers. Accessed: 18/02/2014.

[86] Instruction manual, P6022 current probe. Technical report, Tektronix, 1993.

[87] S. Zangui, B. Vincent, K. Berger, R. Perrussel, E. Clavel, C. Vollaire, and O. Chadebec. Near-field coupling between EMC filter components. In *Electromagnetic Field Computation (CEFC), 2010 14th Biennial IEEE Conference on*, page 1, may 2010. doi: 10.1109/CEFC.2010.5481672.

[88] H.M. Rebholz, S. Tenbohlen, and W. Kohler. Time-domain characterization of RF sources for the design of noise suppression filters. *Electromagnetic Compatibility, IEEE Transactions on*, 51(4):945–952, Nov 2009. ISSN 0018-9375. doi: 10.1109/TEMC.2009.2031909.

[89] H. Bishnoi, A.C. Baisden, P. Mattavelli, and D. Boroyevich. Analysis of EMI terminal modeling of switched power converters. *Power Electronics, IEEE Transactions on*, 27(9):3924–3933, Sept 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2190100.

[90] A.-M. Sanchez, S.A. Pignari, J.-R. Regue, and M. Ribo. Device modeling for nonstationary conducted emissions based on frequency- and time-domain measurements. *Electromagnetic Compatibility, IEEE Transactions on*, 54(4): 738–746, Aug 2012. ISSN 0018-9375. doi: 10.1109/TEMC.2011.2175931.

[91] M. Reuter, S. Tenbohlen, and W. Kohler. Influence of a traction battery's input impedance on conducted emissions of an automotive HV inverter. In *Electromagnetic Compatibility (EMC EUROPE), 2013 International Symposium on*, pages 229–234, Sept 2013.

[92] M. Reuter, S. Tenbohlen, and W. Kohler. The influence of network impedance on conducted disturbances within the high-voltage traction harness of electric vehicles. *Electromagnetic Compatibility, IEEE Transactions on*, 56(1):35–43, Feb 2014. ISSN 0018-9375. doi: 10.1109/TEMC.2013.2273564.

[93] Andrzej Lasia. Electrochemical impedance spectroscopy and its applications. Technical report, Sherbrook University, 2006. Available online.

[94] S. Buller, M. Thele, R.W.A.A. De Doncker, and E. Karden. Impedance-based simulation models of supercapacitors and Li-ion batteries for power electronic applications. *Industry Applications, IEEE Transactions on*, 41(3): 742–747, may-june 2005. ISSN 0093-9994. doi: 10.1109/TIA.2005.847280.

[95] O. Erdinc, B. Vural, and M. Uzunoglu. A dynamic lithium-ion battery model considering the effects of temperature and capacity fading. In *Clean*

Electrical Power, 2009 International Conference on, pages 383 –386, june 2009. doi: 10.1109/ICCEP.2009.5212025.

[96] Lijun Gao, Shengyi Liu, and R.A. Dougal. Dynamic lithium-ion battery model for system simulation. *Components and Packaging Technologies, IEEE Transactions on*, 25(3):495 – 505, sep 2002. ISSN 1521-3331. doi: 10.1109/TCAPT.2002.803653.

[97] M. Reuter, S. Tenbohlen, W. Kohler, and A. Ludwig. Impedance analysis of automotive high voltage networks for EMC measurements. In *EMC Europe 2011 York*, pages 106–111, sept. 2011.

[98] Jin Wang, Ke Zou, Chingchi Chen, and Lihua Chen. A high frequency battery model for current ripple analysis. In *Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE*, pages 676–680, feb. 2010. doi: 10.1109/APEC.2010.5433598.

[99] Agilent impedance measurement handbook – a guide to measurement technology and techniques. Technical report, Agilent Technologies, 2009. 4th edition.

[100] E. Hoene, S. Guttowski, R. Saikly, W. John, and H. Reichl. RF-properties of automotive traction batteries. In *Electromagnetic Compatibility, 2003. EMC '03. 2003 IEEE International Symposium on*, volume 1, pages 425–428, may 2003. doi: 10.1109/ICSMC2.2003.1428282.

[101] Agilent E4991A RF impedance/material analyzer – data sheet. Technical report, Agilent Technologies, 2011.

[102] M.S. Tabbakh, F. Morel, R. Mrad, and Y. Zaatar. High frequency battery impedance measurements for EMI prediction. In *Electromagnetic Compatibility (EMC), 2013 IEEE International Symposium on*, pages 763–767, Aug 2013. doi: 10.1109/ISEMC.2013.6670512.

[103] V. Tarateeraseth, Kye Yak See, Lin Biao Wang, and F.G. Canavero. Systematic power line EMI filter design for smps. In *EMC Europe 2011 York*, pages 586 –591, sept. 2011.

[104] M. Ali, E. Labouré, F. Costa, and B. Revol. Design of a Hybrid Integrated EMC Filter for a DC-DC Power Converter. *Power Electronics,*

IEEE Transactions on, 27(11):4380 –4390, nov. 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2012.2183387.

[105] K. Raggl, T. Nussbaumer, and J.W. Kolar. Model based optimization of EMC input filters. In *Control and Modeling for Power Electronics, 2008. COMPEL 2008. 11th Workshop on*, pages 1–6, Aug 2008. doi: 10.1109/COMPEL.2008.4634683.

[106] M.L. Heldwein, T. Nussbaumer, and J.W. Kolar. Differential mode emc input filter design for three-phase ac-dc-ac sparse matrix pwm converters. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 1, pages 284–291 Vol.1, June 2004. doi: 10.1109/PESC.2004.1355757.

[107] J.-L. Kotny, T. Duquesne, and N. Idir. EMI filter design using high frequency models of the passive components. In *Signal Propagation on Interconnects (SPI), 2011 15th IEEE Workshop on*, pages 143–146, May 2011. doi: 10.1109/SPI.2011.5898860.

[108] M.C. Caponet, F. Profumo, and A. Tenconi. EMI filters design for power electronics. In *Power Electronics Specialists Conference, 2002. pesc 02. 2002 IEEE 33rd Annual*, volume 4, pages 2027 – 2032, 2002. doi: 10.1109/PSEC.2002.1023112.

[109] Laurent Gerbaud, Baidy Toure, Jean-Luc Schanen, and Jean-Pierre Carayon. Modelling process and optimization of EMC filters for power electronics applications. *COMPEL: The International Journal for Computation and Mathematics in Electrical and Electronic Engineering*, 31(3):747 – 763, 2012.

[110] Yannick Poire, Olivier Maurice, Mohamed Ramdani, M'hamed Drissi, and Alain Sauvage. SMPS Tools for EMI Filter Optimization. In *Electromagnetic Compatibility, 2007. EMC Zurich 2007. 18th International Zurich Symposium on*, pages 505 –508, sept. 2007. doi: 10.1109/EMCZUR.2007.4388306.

[111] V. Verma and B. Singh. Genetic-algorithm-based design of passive filters for offshore applications. *Industry Applications, IEEE Transactions on*, 46(4): 1295–1303, July 2010. ISSN 0093-9994. doi: 10.1109/TIA.2010.2049629.

[112] A. Griffo and J. Wang. Design optimization of passive DC filters for aerospace applications. In *Power Electronics, Machines and Drives (PEMD*

2010), 5th IET International Conference on, pages 1 –6, april 2010. doi: 10.1049/cp.2010.0127.

[113] F. Barruel, J.L. Schanen, and N. Retiere. Volumetric optimization of passive filter for power electronics input stage in the more electrical aircraft. In *Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual*, volume 1, pages 433 – 438 Vol.1, june 2004. doi: 10.1109/PESC.2004.1355784.

[114] S. Dhabal and P. Venkateswaran. An Efficient Nonuniform Cosine Modulated Filter Bank Design Using Simulated Annealing. *Journal of Signal and Information Processing*, 3(3):330 –338, 2012. doi: 10.4236/jsip.2012.33042.

[115] S. Busquets-Monge, J.-C. Crebier, S. Ragon, E. Hertz, D. Boroyevich, Z. Gurdal, M. Arpilliere, and D.K. Lindner. Design of a boost power factor correction converter using optimization techniques. *Power Electronics, IEEE Transactions on*, 19(6):1388 – 1396, nov. 2004. ISSN 0885-8993. doi: 10.1109/TPEL.2004.836638.

[116] S. Mandray, J.-M. Guichon, J.-L. Schanen, S. Vieillard, and A. Bouzourene. Automatic layout optimization of a double sided power module regarding Thermal and EMC constraints. In *Energy Conversion Congress and Exposition, 2009. ECCE 2009. IEEE*, pages 1046 –1051, sept. 2009. doi: 10.1109/ECCE.2009.5316092.

[117] Nico Hensgens, Jesus Oliver, Jose A. Cobos, Stanislav Skibin, and Andreas Ecklebe. Design and multi-objective optimization of EMI input filters. In *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, pages 2506–2513, March 2013. doi: 10.1109/APEC.2013.6520648.

[118] Á. Leibinger and Á. Hajdu. Proposal for scalable models in EMC simulation. *Advances in Radio Science*, 9:329–334, August 2011. doi: 10.5194/1/ars-9-329-2011.

[119] David A Coley. *An Introduction to Genetic Algorithms for Scientists and Engineers*. World Scientific Publishing, 1999. ISBN 98 1-02-3602-6.

[120] Singiresu S. Rao. *Engineering Optimization: Theory and Practice*. John Wiley & Sons, third edition, 1996. ISBN 0-471-55034-5.

[121] TDK: Components Library for Agilent ADS. Accessed: 12/04/2013.

[122] Murata: Components Library for Agilent ADS. Accessed: 12/04/2013.

[123] Patrice Russo, Firas Yengui, Gael Pillonnet, Sophie Taupin, and Nacer Abouchi. Dynamic voltage scaling for series hybrid amplifiers. *Microelectronics Journal*, 44(9):753 – 763, 2013. ISSN 0026-2692. doi: http://dx.doi.org/10.1016/j.mejo.2013.03.016. URL http://www.sciencedirect.com/science/article/pii/S0026269213000864.

[124] Thomas Brander, Alexander Gerfer, Bernhard Rall, and Heinz Zenkner. *Trilogy of magnetics*. WÜRTH ELEKTRONIK, fourth edition, 2009. ISBN 978-3-89929-157-5.

[125] Murata. *Understanding Ferrite Bead Inductors*. Murata. http://www.murata.com/products/emc/knowhow/pdf/23to25e.pdf.

[126] muRata. *BLM15PD121SN1*. Murata Manufacturing Co., Ltd., . URL http://www.murata.com/.

[127] R&S® UPV audio analyzer – data sheet. Technical report, Rohde & Schwarz, 2012.

[128] C. Rostamzadeh, F. Grassi, and F. Kashefi. Modeling SMT ferrite beads for SPICE simulation. In *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on*, pages 530–535, 2011. doi: 10.1109/ISEMC.2011.6038369.

[129] Jianmin Zhang, K. Qiu, Liming Yin, R. Brooks, and B. Chen. Ferrite bead model extraction and its application in high-performance ASIC analog power filtering. In *Electromagnetic Compatibility (EMC), 2011 IEEE International Symposium on*, pages 536–541, 2011. doi: 10.1109/ISEMC.2011.6038370.

[130] T. Sato, K. Watanabe, H. Igarashi, T. Matsuo, T. Mifune, K. Kawano, M. Suzuki, Y. Uehara, and A. Furuya. 3-D optimization of ferrite inductor considering hysteresis loss. *Magnetics, IEEE Transactions on*, 49(5):2129–2132, 2013. ISSN 0018-9464. doi: 10.1109/TMAG.2013.2241413.

[131] A. Rezaei-Zare, R. Iravani, M. Sanaye-Pasand, H. Mohseni, and S. Farhangi. An accurate hysteresis model for ferroresonance analysis of a transformer. *Power Delivery, IEEE Transactions on*, 23(3):1448–1456, 2008. ISSN 0885-8977. doi: 10.1109/TPWRD.2007.916225.

[132] Shun-Tsai Liu, Sy-Ruen Huang, and Hung-Wei Chen. Using TACS functions within EMTP to set up current-transformer model based on the Jiles-Atherton theory of ferromagnetic hysteresis. *Power Delivery, IEEE Transactions on*, 22(4):2222–2227, 2007. ISSN 0885-8977. doi: 10.1109/TPWRD.2007.905809.

[133] Reinhard Woehrnschimmel, Christian Kral, Florian Muellner, Stefan Wild, Harald Neudorfer, and Friedrich Dangl. A combined hysteresis and eddy-current model developed for a wide frequency range in electric machine applications. In *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, pages 3180–3185, 2013. doi: 10.1109/ECCE.2013.6647117.

[134] Liang Cao and Ge Li. Complete parallelogram hysteresis model for electric machines. *Energy Conversion, IEEE Transactions on*, 25(3):626–632, 2010. ISSN 0885-8969. doi: 10.1109/TEC.2010.2047397.

[135] D.C. Jiles and D.L. Atherton. Theory of ferromagnetic hysteresis (invited). *Journal of Applied Physics*, 55(6):2115–2120, 1984. ISSN 0021-8979. doi: 10.1063/1.333582.

[136] P.R. Wilson, J.N. Ross, A.D. Brown, T. Kazmierski, and J. Baranowski. Efficient mixed-domain behavioural modelling of ferromagnetic hysteresis implemented in VHDL-AMS. In *Design, Automation and Test in Europe Conference and Exhibition, 2004. Proceedings*, volume 1, pages 742–743, 2004. doi: 10.1109/DATE.2004.1268957.

[137] A. Raghunathan, Y. Melikhov, J.E. Snyder, and DC. Jiles. Theoretical model of temperature dependence of hysteresis based on mean field theory. *Magnetics, IEEE Transactions on*, 46(6):1507–1510, 2010. ISSN 0018-9464. doi: 10.1109/TMAG.2010.2045351.

[138] J.H. Chan, A. Vladimirescu, X.-C. Gao, P. Liebmann, and J. Valainis. Nonlinear transformer model for circuit simulation. *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, 10(4):476–482, 1991. ISSN 0278-0070. doi: 10.1109/43.75630.

[139] I.D. Mayergoyz. *The Classical Preisach Model of Hysteresis*. Springer New York, 1991.

[140] K. Wiesen and S.H. Charap. Vector Preisach modeling. *Journal of Applied Physics*, 61(8):4019–4021, 1987. ISSN 0021-8979. doi: 10.1063/1.338966.

[141] S. Charap and A. Ktena. Vector Preisach modeling (invited). *Journal of Applied Physics*, 73(10):5818–5823, 1993. ISSN 0021-8979. doi: 10.1063/1.353538.

[142] C.D. Boley and M.L. Hodgdon. Model and simulations of hysteresis in magnetic cores. *Magnetics, IEEE Transactions on*, 25(5):3922–3924, 1989. ISSN 0018-9464. doi: 10.1109/20.42478.

[143] DaMing Zhang and J. Fletcher. Quantification of required multi-segments for accurately computing induced voltage in a ferrite inductor using static and dynamic Jiles-Atherton models. *Magnetics, IEEE Transactions on*, 49(11):5424–5429, Nov 2013. ISSN 0018-9464. doi: 10.1109/TMAG.2013.2271218.

[144] Abdelkader Benabou. Contribution à la caractérisation et à la modélisation de matériaux magnétiques en vue d'une implantation dans un code de calcul de champ, 2002. Université de Lille I.

[145] Emilio Del Moral Hernandez, Carlos S. Muranaka, and José R Cardoso. Identification of the Jiles-Atherton model parameters using random and deterministic searches. *Physica B: Condensed Matter*, 275(1-3):212 – 215, 2000. ISSN 0921-4526. doi: http://dx.doi.org/10.1016/S0921-4526(99)00766-8. URL http://www.sciencedirect.com/science/article/pii/S0921452699007668.

[146] P.R. Wilson, J.N. Ross, and A.D. Brown. Optimizing the Jiles-Atherton model of hysteresis by a genetic algorithm. *Magnetics, IEEE Transactions on*, 37(2):989–993, 2001. ISSN 0018-9464. doi: 10.1109/20.917182.

[147] M. Toman, G. Stumberger, and D. Dolinar. Parameter identification of the Jiles-Atherton hysteresis model using differential evolution. *Magnetics, IEEE Transactions on*, 44(6):1098–1101, 2008. ISSN 0018-9464. doi: 10.1109/TMAG.2007.915947.

[148] muRata. *BLM18HK102SN1D*. Murata Manufacturing Co., Ltd., . URL http://www.murata.com/.

[149] E. Sturtzer, G. Pillonnet, G. Lemarquand, and N. Abouchi. Comparison between voltage and current driving methods of a micro-speaker. *Applied Acoustics*, 73(11):1087 – 1098, 2012. ISSN 0003-682X. doi: http://dx.doi.org/10.1016/j.apacoust.2012.05.008. URL http://www.sciencedirect.com/science/article/pii/S0003682X12001284.

[150] M. Berkhout, L. Dooper, and B. Krabbenborg. A 4 Ω 2.65W class-D audio amplifier with embedded DC-DC boost converter, current sensing ADC and DSP for adaptive speaker protection. *Solid-State Circuits, IEEE Journal of*, 48(12):2952–2961, Dec 2013. ISSN 0018-9200. doi: 10.1109/JSSC.2013.2284692.

[151] Thermonics T-2500E precision temperature forcing system. Technical report, Thermonics.

[152] Agilent 4194A impedance/gain-phase analyzer – data sheet. Technical report, Agilent Technologies.

Appendix A

Definitions

Total Harmonic Distortion: called also THD, it is used to quantify the linearity of an electronic system. It is the sum of powers of the different harmonics over the fundamental frequency power. In audio applications, it is applied in the audio frequency band and used to quantify the capability of the amplifier to reconstitute the original audio signal. Often confusions with the THD+N can happen. N is the noise power and the THD+N is used in order to quantify all types of distortion, including the harmonic distortion, inter-modulation distortion, thermal noise, the power supply hum and so on [46]. The THD or the THD+N are given whether by percentage whether by decibels.

Signal to Noise Ratio: known by SNR, it is used to compare the level of the desired signal over the noise background level. Thus, it is the ratio of the signal power over the noise background power and usually given in decibels. In audio, it is used to identify the minimum measurable audio signal according to the noise level in the audio frequency band.

Power Supply Rejection Ratio: or PSRR, is used to measure the capability of a device to reject the noise introduced by the power supply. The PSRR is given in decibels. It is used when the power supply noise is able to impact the system performance which is the case of power amplifiers. Hence, it is used in the case of audio amplifiers, in particular Class-D amplifiers.

The audio gain is the ratio between the output signal over the input signal. An ideal audio amplifier must have a fixed audio gain on the entire audio frequency band. However, in the real world, engineers tend to have less than $1\,dB$ gain variations in the audio frequency band.

Appendix B

Appendix of Chapter 3: Proofs

B.1 Proof of equation (3.5)

By definition :

$$\begin{aligned}
V_1 &= Z_{1\,1} I_1 + \cdots + Z_{1\,2N} I_{2N} \\
&\vdots \qquad\qquad \vdots \qquad\qquad \vdots \\
V_i &= Z_{i\,1} I_1 + \cdots + Z_{i\,2N} I_{2N} \\
&\vdots \qquad\qquad \vdots \qquad\qquad \vdots \\
V_j &= Z_{j\,1} I_1 + \cdots + Z_{j\,2N} I_{2N} \\
&\vdots \qquad\qquad \vdots \qquad\qquad \vdots \\
V_{2N} &= Z_{N\,1} I_1 + \cdots + Z_{2N\,2N} I_{2N}
\end{aligned} \tag{B.1}$$

If we are interested to measure Z_{ij}, except the i^{th} and the j^{th} ports, we place all the ports to an open circuit ($I_x = 0\ ;\ x = 1 \cdots 2N\ ;\ x \neq i\ ;\ x \neq j$). Thus, (B.1) can be simplified to (B.2) and (B.3).

$$V_i = Z_{i\,i} I_j + Z_{i\,j} I_j \tag{B.2}$$

$$V_j = Z_{j\,i} I_i + Z_{j\,j} I_j \tag{B.3}$$

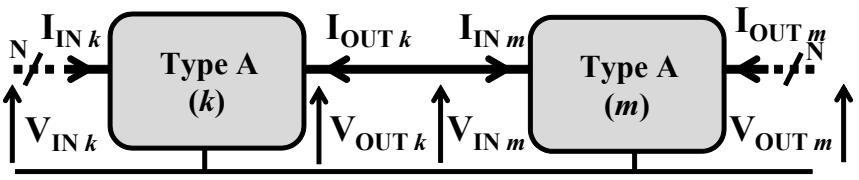


FIGURE B.1: k and m block association.

If we short circuit the j^{th} port, then $V_j = 0$. Thus, equation (B.4) can be obtained from (B.3).

$$I_j = -\frac{Z_{ji}}{Z_{jj}} I_i \tag{B.4}$$

Using (B.4) in (B.2) lead to equation (B.5).

$$\frac{V_i}{I_i} = Z_{ii} - \frac{Z_{ij}Z_{ji}}{Z_{jj}} \tag{B.5}$$

In this case, where the j^{th} port is in short circuit, $\frac{V_i}{I_i}$ is equal to $Z_{ij_{sc}}$. Also, due to the reciprocity theorem [74] $Z_{ij} = Z_{ji}$. Accordingly, we can obtain (B.6) which lead to equation (3.5).

$$Z_{ij}^2 = Z_{jj}(Z_{ii} - Z_{ij_{sc}}) \tag{B.6}$$

B.2 Proof of equation (3.8)

In order to prove equation 3.8, the k and m blocks of section 3.3.4.1 were re-considered (Fig. B.1). In Fig. B.1, V_{IN_k}, V_{OUT_k}, V_{IN_m}, V_{OUT_m}, I_{IN_k}, I_{OUT_k}, I_{IN_m} and I_{OUT_m} are vectors with a dimension equal to N. Those vectors are the voltages or the current for the N ports of k or m blocks.

By definition :

$$\begin{aligned} V_{IN_k} &= Z_{k11} I_{IN_k} + Z_{k12} I_{OUT_k} \\ V_{OUT_k} &= Z_{k21} I_{IN_k} + Z_{k22} I_{OUT_k} \end{aligned} \tag{B.7}$$

$$\begin{aligned} V_{IN_m} &= Z_{m11} I_{IN_m} + Z_{m12} I_{OUT_m} \\ V_{OUT_m} &= Z_{m21} I_{IN_m} + Z_{m22} I_{OUT_m} \end{aligned}$$

Since the block k output is related to the block m input, then :

$$\begin{aligned} V_{OUT_k} &= V_{IN_m} \\ I_{OUT_k} &= -I_{IN_m} \end{aligned} \tag{B.8}$$

When using (B.7) and (B.8) :

$$\begin{aligned} V_{OUT_k} &= -Z_{m11} I_{OUT_k} + Z_{m12} I_{OUT_m} \\ V_{OUT_m} &= -Z_{m21} I_{OUT_k} + Z_{m22} I_{OUT_m} \end{aligned} \tag{B.9}$$

From (B.7) and (B.9) :

$$\begin{aligned} I_{OUT_k} = &-(Z_{k22} + Z_{m11})^{-1} Z_{k21} I_{IN_k} \\ &+(Z_{k22} + Z_{m11})^{-1} Z_{m12} I_{OUT_m} \end{aligned} \tag{B.10}$$

Finally, when using (B.10) in (B.7) and (B.9)

$$\begin{aligned} V_{IN_k} = &[Z_{k11} - Z_{k12}(Z_{k22} + Z_{m11})^{-1} Z_{k21}] I_{IN_k} \\ &+Z_{k12}(Z_{k22} + Z_{m11})^{-1} Z_{m12} I_{OUT_m} \end{aligned} \tag{B.11}$$

$$\begin{aligned} V_{OUT_m} = &Z_{m21}(Z_{k22} + Z_{m11})^{-1} Z_{k21} I_{IN_k} \\ &+[Z_{m22} - Z_{m21}(Z_{k22} + Z_{m11})^{-1} Z_{m12}] I_{OUT_m} \end{aligned} \tag{B.12}$$

The resulting block has V_{IN_k}, I_{IN_k} on the input and V_{OUT_m}, I_{OUT_m} on the output. The resulting impedance matrix is the matrix relating V_{IN_k}, V_{OUT_m} to I_{IN_k}, I_{OUT_m}. Hence, (B.11) and (B.12) permit to deduce equation 3.8.

B.3 Proof of equation (3.9)

In order to prove equation 3.9, the km and L blocks of section 3.3.4.2 were reconsidered (Fig. B.2). In Fig. B.2 $V_{IN_{km}}$, $V_{OUT_{km}}$, V_L, $I_{IN_{km}}$, $I_{OUT_{km}}$ and I_L are vectors with a dimension equal to N. Those vectors are the voltages or the current

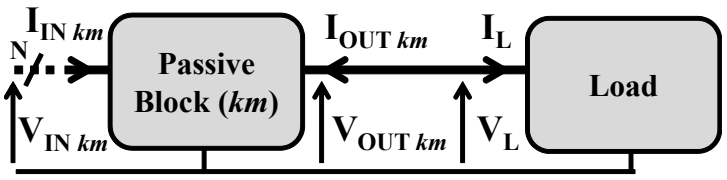


FIGURE B.2: km and L block association.

for the N ports of km or L blocks.

By definition :

$$\begin{aligned} V_{IN_{km}} &= Z_{km11} I_{IN_{km}} + Z_{km12} I_{OUT_{km}} \\ V_{OUT_{km}} &= Z_{km21} I_{IN_{km}} + Z_{km22} I_{OUT_{km}} \end{aligned} \tag{B.13}$$

$$V_L = Z_L I_L \tag{B.14}$$

Since block km output is related to block L input, then :

$$\begin{aligned} V_{OUT_{km}} &= V_L \\ I_{OUT_{km}} &= -I_L \end{aligned} \tag{B.15}$$

When using (B.14) and (B.15) :

$$V_{OUT_{km}} = -Z_L I_{OUT_{km}} \tag{B.16}$$

Using (B.16) in (B.13) :

$$I_{OUT_{km}} = -(Z_L + Z_{km22})^{-1} Z_{km12} I_{IN_{km}} \tag{B.17}$$

Finaly using (B.17) in (B.13) :

$$V_{IN_{km}} = [Z_{km11} - Z_{km12}(Z_L + Z_{km22})^{-1} Z_{km12}] I_{IN_{km}} \tag{B.18}$$

The resulting block has only V_{kmL}, I_{kmL} on the input. The resulting impedance matrix is the matrix relating V_{kmL} to I_{kmL}. Hence, (B.18) permit us to deduce equation (3.9).

B.4 Proof of equation (3.11)

By definition (see Fig. 3.9):

$$V_{IN_{[1-k]}} = Z_{[1-k]\,11}\, I_{IN_{[1-k]}} + Z_{[1-k]\,12}\, I_{OUT_{[1-k]}} \tag{B.19}$$

$$V_{OUT_{[1-k]}} = Z_{[1-k]\,21}\, I_{IN_{[1-k]}} - Z_{[1-k]\,22}\, I_{OUT_{[1-k]}} \tag{B.20}$$

In (B.20), $I_{IN_{[1-k]}}$ and $I_{OUT_{[1-k]}}$ can be replaced using equation (3.10) and (3.12). Thus, equation (3.11) can be computed.

B.5 Proof of equation (3.13)

Inspired from the method of section 3.3, the DC block can be modeled as a two port block as in (B.21).

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} = \boldsymbol{Z_{DC}} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix} \tag{B.21}$$

When a Device Under Test (DUT), having Z_{DUT} as an impedance, is connected to the port 2, $V_2 = -Z_{DUT} I_2$. Then the impedance measured by the impedance analyzer (Z_{IA}) is given by equation (B.22).

$$Z_{IA} = \frac{V_1}{I_1} = Z_{11} - \frac{Z_{12}^2}{Z_{22} - Z_{DUT}} \tag{B.22}$$

Using the impedances Z_{init_1}, Z_{init_2}, Z_{init_3} and Z_{std} (see section 3.5.2) it is possible to deduce (B.23).

$$\begin{aligned} Z_{11} &= Z_{init_1} \\ Z_{12} &= \sqrt{\frac{(Z_{init_1} - Z_{init_2})(Z_{init_1} - Z_{init_3})}{Z_{init_3} - Z_{init_2}} Z_{std}} \\ Z_{22} &= \frac{Z_{init_1} - Z_{init_3}}{Z_{init_3} - Z_{init_2}} Z_{std} \end{aligned} \tag{B.23}$$

Finally, solving equation (B.22) when using (B.23) allows us to a computed Z_{comp} in equation (3.13) which is equal to Z_{DUT}.

Appendix C

Appendix of Chapter 3: Additional Measurements and Simulations

C.1 Class-D amplifier transient simulation

The active block model can be determined whether by measurement whether by simulation. The advantage of the measurements is the accuracy and the certainty of the results. However, in the case of simulations the biggest advantage is obtaining earlier results ; before any prototype construction. Therefore, this point has been investigated, but with a different Class-D amplifier due to the availability of the transient simulation models. The chosen amplifier [27] has a differential output with an output power of $2.5\,W$ and it is preceded by a boost step-up converter in order to supply the power stage.

The IC connections and package model has been added to the transistor level model (Fig. C.1), then, the whole has been simulated in the Cadence® environment. The transistor level model cannot be presented due to the company policy, however, additional information about the amplifier can be found in [27]. The amplifier has a 20 ball Wafer-Level Chip-Scale Package (WL-CSP) with the following dimensions: $1.98 \times 2.80 \times 0.63\,mm$ and a $0.5\,mm$ pitch (Fig. C.2). Accordingly, the IC pins have been modeled as shown in Fig. C.3.

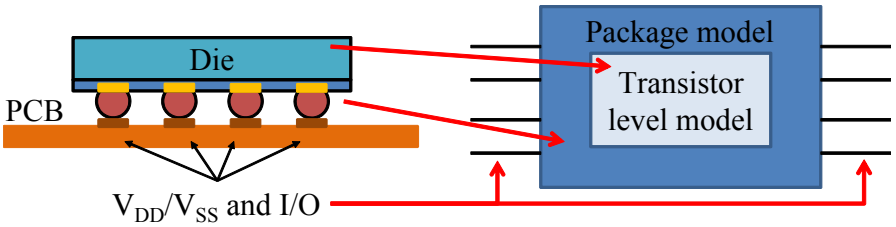


FIGURE C.1: Class-D amplifier transient model.

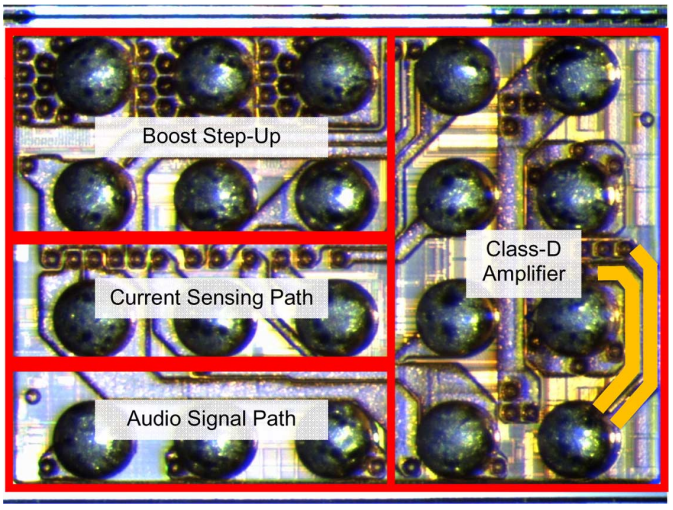


FIGURE C.2: Chip photograph: 20 balls WL-CSP package [27].

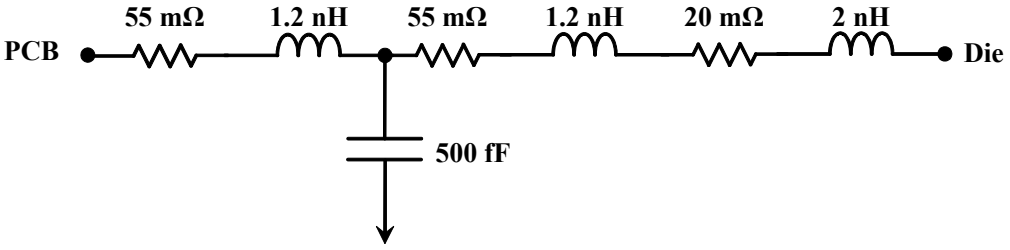


FIGURE C.3: IC pin model according to the package.

The transient simulations were done using a variable time step for a higher accuracy. Afterwards, the Class-D amplifier output voltage has been re-sampled with the same sampling frequency as the one of the measured signal ($2\,GHz$). These are compared in Fig. C.4 up to $100\,MHz$. This latter shows that the difference between the two spectra is less than $6\,dB$ over the considered frequency band which prove that the used models are accurate enough for an early stage EMC investigation of the considered amplifier.

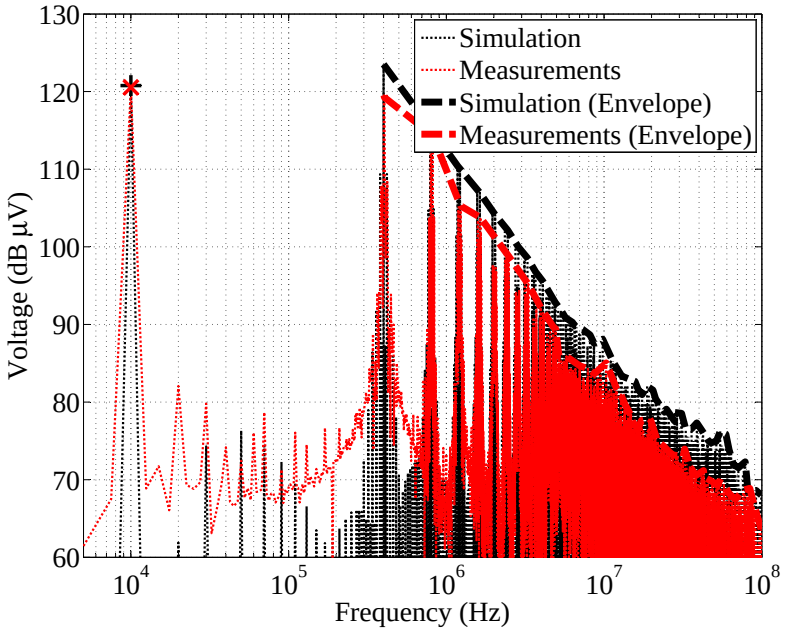


FIGURE C.4: Comparison between the simulated and the measured output spectra.

C.2 EMI computation for a Class-D amplifier powered by a battery

In section 3.6 the battery impedance has been measured and validated in the frequency range $[1\,MHz\ ;\ 100\,MHz]$. This appendix shows the battery impedance measurement and validation using a Class-D amplifier. The goal is to validate the battery impedance below $1\,MHz$. Therefore, the procedure presented in section 3.6 has been also used with the same battery (Nokia BL-5CA), but this time, as a converter we used the Class-D amplifier of section 3.4 instead of the DC-DC converter of section 3.6. Thus, the measured battery impedance is shown in Fig. C.5 and the voltage computation results are shown in Fig. C.6.

On the first hand, Fig. C.5 shows that the battery have a capacitive behavior below $400\,kHz$ and an inductive behavior beyond $400\,kHz$. It can be seen as well that at the lower frequencies (few kHz), the measurement shows noisy curve. This is due to the high impedance of the DC block at these frequencies which reduce the sensibility of the IA for low impedance DUTs. Thus, the impedances Z_{init_1}, Z_{init_2} and Z_{init_3} have close results at the low frequencies which lead to a lower sensibility of the compensation method. In order to increase the sensibility of the procedure at low frequencies, the capacitor values of the DC block should be

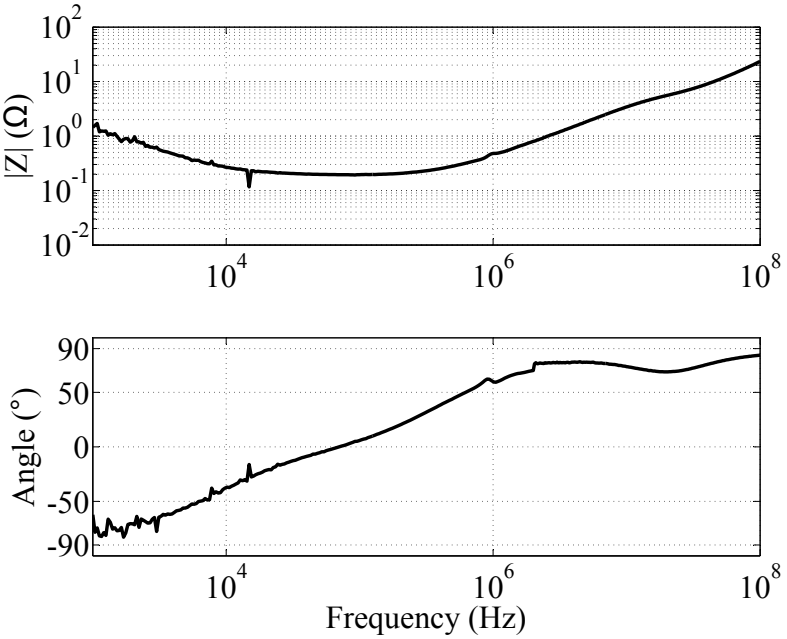


FIGURE C.5: Battery impedance

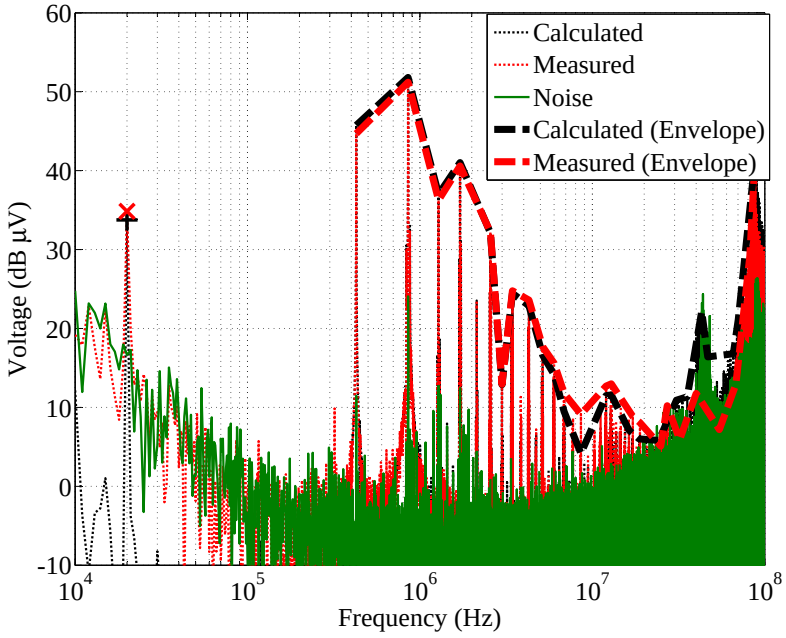


FIGURE C.6: Voltage of the battery when feeding a Class-D amplifier

increased. On the other hand, Fig. C.6 shows that the voltage computation of the Class-D amplifier at the supply level have accurate results on the entire frequency band. The only differences can be seen between $40\,MHz$ and $60\,MHz$ which is due to the high noise level of the measurement.

Appendix D

Appendix of Chapter 3: Speaker Impedance

D.1 Understanding the speaker impedance matrix

The loudspeaker board is considered in this section and it is shown in Fig. D.1. The two SMB connectors are connecting the differential impedance which is the speaker, above the ground plane. By the first reflection, since there is no direct connection between the speaker and the ground, one can assume that z_{11} and z_{22} (diagonal matrix elements) are the parasitic capacitances between the top PCB layer (PCB tracks and the speaker) and the bottom PCB layer (ground plane). Second, one can assume intuitively that z_{12} which is equal to z_{21} (counter diagonal matrix elements), should be identical to the differential impedance which can be approximated to the speaker impedance, but it is not the case. Fig D.2(a) shows the impedance measurement of z_{11}, z_{22} and z_{12}, where z_{11} and z_{22} have a capacitive behavior as expected, however, z_{12} do not have an inductive behavior similar to the speaker (black line of Fig. D.2(b)). This issue is investigated as follows for the purpose of finding the inductive behavior of the speaker into the impedance matrix.

In order to correlate the impedance matrix to the physical architecture of the board, the circuit of Fig. D.3 is considered. This lead to calculate z_{11}, z_{22} and $z_{12_{sc}}$

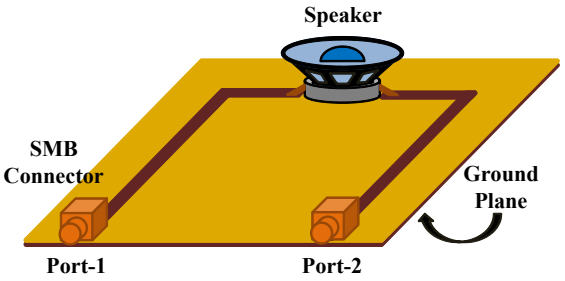
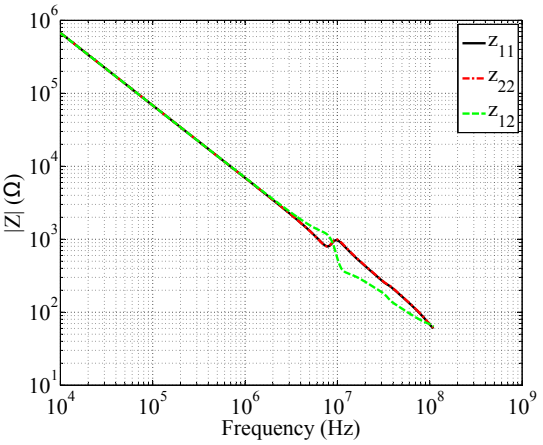
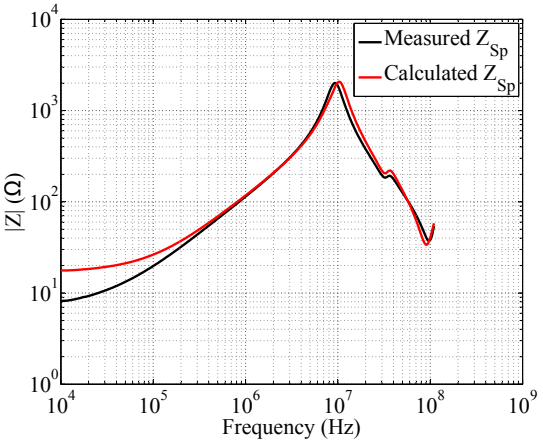


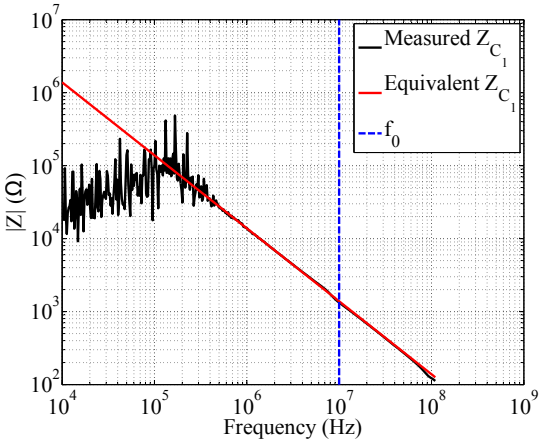
FIGURE D.1: Board of the speaker load



(a) The elements of the load impedance matrix



(b) Speaker Impedance



(c) Impedance of C_1 capacitor

FIGURE D.2: Impedances of the circuit in Fig. D.3

(see section 3.3.3.1) as given in (D.1), (D.2) and (D.3) respectively.

$$z_{11} = (Z_{Sp} + Z_{C_2}) \parallel Z_{C_1} \tag{D.1}$$

$$z_{22} = (Z_{Sp} + Z_{C_1}) \parallel Z_{C_2} \tag{D.2}$$

$$z_{12_{sc}} = Z_{Sp} \parallel Z_{C_1} \tag{D.3}$$

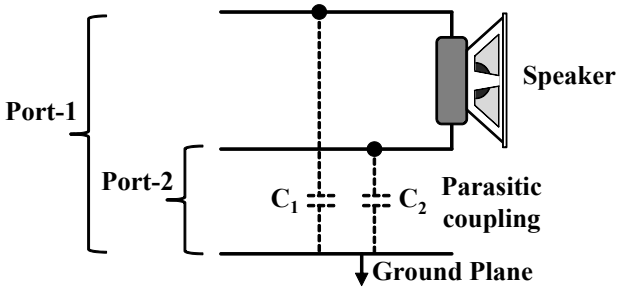


FIGURE D.3: Speaker load equivalent circuit

where Z_{Sp} is the speaker impedance, Z_{C_1} and Z_{C_2} are the impedances of C_1 and C_2 respectively.

Z_{Sp} is measured separately with the IA. Afterwards, using equation (D.3) Z_{C_1} is calculated and plotted in Fig. D.2(c). As the measured Z_{C_1} is noisy at low frequencies, the capacitance C_1 has been calculated using: $Z_{C_1}(f_0) = 1/jC_1\omega_0$, where $\omega_0 = 2\pi f_0$. Finally, due to the physical symmetry of the circuit, C_1 is equal to C_2 (equal to $11.5\,pF$).

Now that Z_{C_1} and Z_{C_2} are known, using equation (D.1) and the measured z_{11}, it is possible to recalculate Z_{Sp}. The comparison with the measured Z_{Sp} is made in Fig. D.2(b). It can be seen that the measured and the calculated Z_{Sp} match at high frequencies. However, small differences can be seen at low frequencies. These can be explained by the fact that more parasitic components exist in the circuit which are not taken into account in the model of Fig. D.3.

As a conclusion, the impedance matrix contains all the needed information about the impedance behavior of the circuit, even though they are implicit. Nevertheless, the desired impedance behavior cannot be directly read from the matrix elements without a minimum knowledge on the circuit architecture.

D.2 Speaker impedance measurements under temperature variations

Referring to [150], the temperature variation of a loudspeaker implies an impedance variation in the audio frequency band. This can affect the audio performance of the amplifier as well as the amplifier output power. Therefore, in this section we

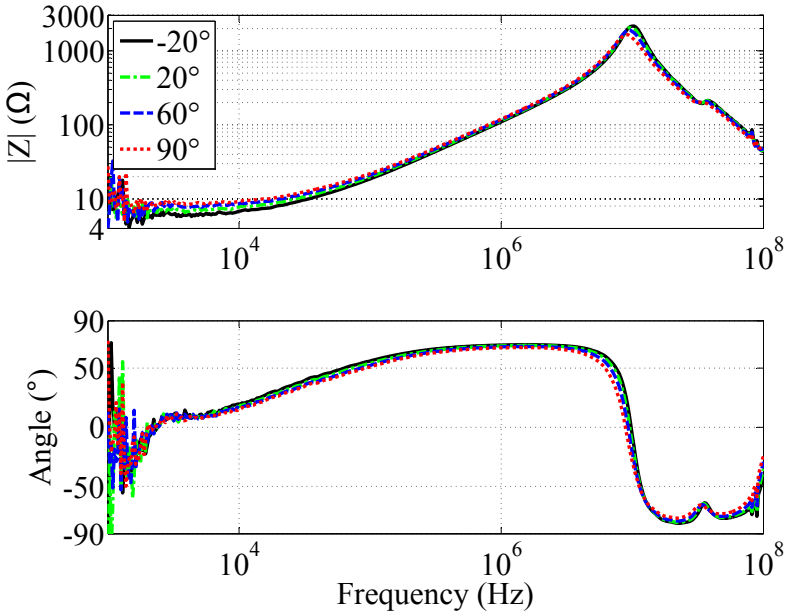


FIGURE D.4: Speaker impedance measurements under temperature variations.

are interested to evaluate the effect of the temperature variation on the EMI by measuring the loudspeaker impedance.

A dedicated PCB for speaker impedance measurement has been placed in temperature forcing system [151] in order to control its temperature. Afterwards, using the Agilent 4194A IA [152] the impedance of a cellphone loudspeaker [85] has been measured at four different temperatures. The results are plotted in Fig. D.4. The four temperature points were chosen according to the temperature specification of a cellphone, generally in the range of $[-20\,°\mathrm{C}\,;\ 90\,°\mathrm{C}]$.

As can be seen from Fig. D.4, at low frequencies ($< 300\,kHz$) the impedance of a loudspeaker has significant variations due to the temperature variations. When the temperature changes from $-20\,°\mathrm{C}$ to $90\,°\mathrm{C}$, the loudspeaker impedance changes from $6\,\Omega$ to $8\,\Omega$ at $4\,kHz$. This means that the output power can have $25\,\%$ variations for a $4\,kHz$ audio signal at extreme temperature variations. However, at high frequencies ($> 300\,kHz$) the impedance of a loudspeaker is less susceptible to the temperature variations. The worst case is seen at $10\,MHz$ where the impedance changes from $2165\,\Omega$ to $1657\,\Omega$. Thus, for a fixed voltage noise level the current will change for less than $2.5\,dB\mu A$ which is tolerable.

Appendix E

Appendix of Chapter 5: THD Measurements on a Linear Amplifier

This work has been performed with the help of Kevin El Haddad from the Lebanese University.

A linear amplifier allows us to remove the frequency spectral content of the switching of a Class-D amplifier. Hence, we can identify if the distortion caused by the ferrite bead is a phenomenon occurring in the audio frequency band. This investigation has been carried out with THD measurements before and after a ferrite bead placed at the output of a linear amplifier. The measurement bench used is shown in Fig. E.1 and it is constituted of an audio analyzer (AA), signal generator, linear amplifier, ferrite bead (rated current of 2 A and a DC resistor of $50\,m\Omega$) and an $8\,\Omega$ load resistor.

Fig. E.2 and Fig. E.3 show the THD measurements according to the signal amplitude and signal frequency respectively. In Fig. E.2, the measurements were done using a $1\,kHz$ sinusoidal signal with an amplitude sweep from $1\,mV$ to $7\,V$. In Fig. E.3, the measurements were done using a $200\,mV$ sinusoidal signal with a frequency sweep from $20\,Hz$ to $10\,kHz$. Both measurements use 9 harmonics in the THD computation.

Note that Fig. E.3 shows measurements up to $10\,kHz$ only, since all the harmonics become out of band when the signal frequency exceeds $10\,kHz$. Note also that both

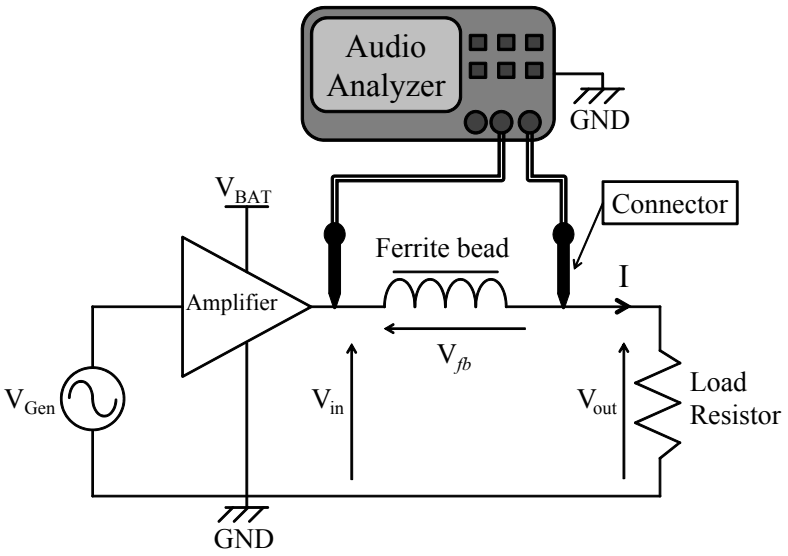


FIGURE E.1: THD measurements of a linear amplifier and a ferrite bead.

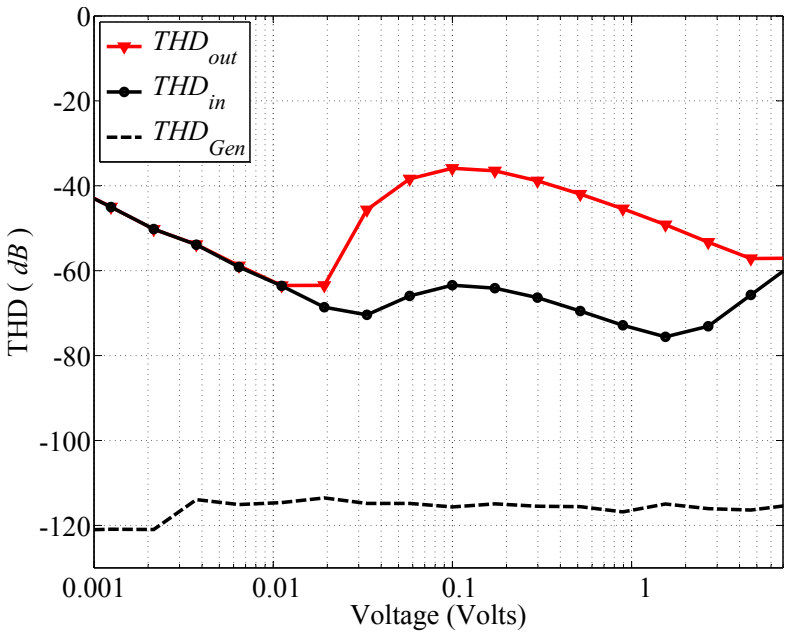


FIGURE E.2: THD measurements according to the signal amplitude at $1\,kHz$.

of the measurements were configured to use 9 harmonics in the THD computation.

In Fig. E.2 and Fig. E.3, THD_{Gen} is the THD of the original signal delivered by the generator. THD_{in} and THD_{out} are respectively the THD for V_{in} and V_{out} (see Fig. E.1). THD_{in} is then the THD before the ferrite bead and THD_{out} is the one after the ferrite bead. Therefore, the difference between THD_{in} and THD_{out} is the harmonic distortion due to the ferrite bead.

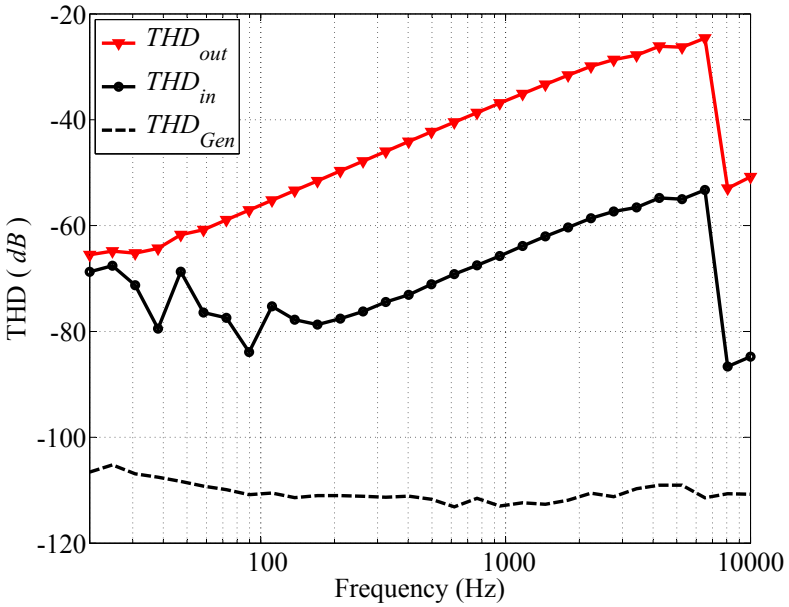


FIGURE E.3: THD measurements according to signal frequency with $V_{in} = 200\,mV$.

As can be seen from Fig. E.2, the ferrite bead increases the signal THD in the amplitude range $[10\,mV \;\; , \;\; 7\,V]$, thus, in the current range $[1\,mA \;\; , \;\; 737\,mA]$ which is lower than the component rated current $(2\,A)$. However, below $10\,mV$ (correspond to $1\,mA$) the amplifier output noise does not allow any comparison. In this case the signal harmonics are below the amplifier noise floor. Thus, the power of the harmonics has a fixed level that corresponds to the noise power. When increasing the audio signal, the fundamental power increase but the harmonic power remains unchangeable. Considering the THD definition (see appendix A), the THD corresponds then to a the negative slope until the harmonics become higher than the noise floor.

Fig. E.3 shows that the ferrite bead increases the THD on the entire frequency range. However, in this case the THD decreases suddenly after $6.5\,kHz$. This can be explained by the fact that some of the significant harmonics become out of band, thus, they are attenuated by the audio filter which is embedded in the AA. Note that, beyond $10\,kHz$ all the signal harmonics are out of the audio band, therefore, the frequency sweep has been made between $20\,Hz$ and $10\,kHz$.

As a result, the ferrite bead increases the THD at all the frequencies and a wide range of signal levels. The deterioration caused by the ferrite bead can reach $-35\,dB$ even with the absence of the high frequency spectral content of a Class-D

amplifier. As a conclusion, the ferrite bead distortion is a low frequency phenomenon occurring in the audio frequency band.

Annexe F

French Report
Summarized Version

F.1 Introduction

De nos jours, le développement des systèmes électroniques portables, alimentés par des batteries, est contraint par la nécessité de fabriquer des circuits électroniques avec un bon rendement. En effet, la consommation de ces circuits est directement liée à l'autonomie de l'appareil. En conséquence, les convertisseurs électroniques de puissance sont largement utilisés. Pour les applications audio, les amplificateurs commutés, nommés aussi Classe D [6], présentent un bon compromis entre la qualité audio et le rendement énergétique. Pour cela, ils sont fréquemment utilisés dans des systèmes portables ou embarqués. Cependant, leur fort niveau d'émissions électromagnétiques est souvent problématique dans les applications finales. Cela peut causer le dysfonctionnement des applications électroniques à proximité ou des problèmes de conformité aux normes de compatibilité électromagnétique (CEM). La résolution d'un problème de CEM consiste à prendre une ou plusieurs des actions suivantes : Diminuer les émissions de l'agresseur, augmenter l'immunité de la victime ou réduire le couplage. Dans le but de réduire les émissions des amplificateurs de Classe D, de nombreuses solutions au niveau de l'architecture ou la commande ont été développées [8–11]. Cependant, un filtre CEM sur les chemins de propagation des perturbations reste nécessaire pour obtenir une réduction suffisante des émissions conduites ou rayonnées.

La conception d'un filtre CEM n'est pas similaire à celle des filtres classiques. Généralement, un filtre CEM doit couvrir une large bande de fréquences, c'est pourquoi il est fortement influencé par les éléments parasites [12]. De plus, un filtre CEM est encombrant et coûteux en comparaison avec l'amplificateur lui-même. Aussi, dans le cas d'un amplificateur de Classe D, les filtres CEM dégradent la qualité sonore de l'amplificateur à cause des non linéarités des composants utilisés. Souvent (par manque d'outils adaptés), la conception de ces filtres est basée sur des essais expérimentaux. Cette technique n'est pas optimale car elle augmente le coût et la durée de la production. Pour cela des techniques de simulation qui peuvent assister les intégrateurs lors de la phase de conception sont très avantageuses. Cela est donc le but de cette thèse.

Les amplificateurs de Classe D sont généralement utilisés dans des applications qui ont comme fonction principale l'affichage, l'audio, la transmission, etc. Ce type d'application est soumis à des normes de CEM comme l'EN55022 en Europe [13] ou le FCC-part 15-subpart B aux Etats Unis [14]. Ces normes sont divisées en deux parties : les perturbations conduites dans la bande de fréquence [150 kHz ; 30 MHz] et les perturbations rayonnées [30 MHz ; 1 GHz]. Ce travail de thèse est focalisé sur les perturbations conduites et donc la bande de fréquence [150 kHz ; 30 MHz].

F.1.1 Objectifs de la thèse

En tant que collaboration entre quatre instituts, les objectifs de cette thèse sont divisés en deux parties. D'une part les deux laboratoires Ampère et INL attendent une approche rigoureuse, innovante et scientifique pour atteindre les objectifs. Le laboratoire Ampère est spécialisé en électronique de puissance et en CEM. Tandis que l'INL est spécialisé en conception analogique des convertisseurs intégrés d'énergie. D'autre part, les deux entreprises ST Ericsson et ST Microelectronics souhaitent que ce travail de recherche soit en accord avec leurs intérêts et perspectives. Les deux entreprises sont des fabricants de circuits intégrés y compris les amplificateurs de Classe D. Les objectifs sont alors divisés en objectifs scientifiques et objectifs d'entreprise.

F.1.1.1 Objectifs scientifiques

En se basant sur les problématiques présentées dans l'introduction, les objectifs scientifiques sont décrits comme suit :

- Développer une approche de modélisation des amplificateurs de Classe D dédiée à l'étude de la CEM. L'approche doit avoir une grande précision dans la bande de fréquences des perturbations conduites et pouvoir être utilisée dans la phase de conception de produit. De plus, l'approche doit avoir un temps de simulation court et pouvoir être facilement appliqué à tout type d'amplificateur de Classe D.
- Employer l'approche développée dans le point précédent dans une boucle d'optimisation pour assister les intégrateurs dans la conception de leurs filtres CEM. La solution fournie par le processus d'optimisation doit être réalisable en pratique.
- L'introduction d'un filtre de CEM dans une application d'amplification audio ne doit pas détériorer les performances audio de l'amplificateur. Pour cela, l'impact du filtre sur la fonction principale de l'amplificateur devra être évaluée. En particulier, nous devons modéliser les effets non linéaires des composants magnétiques et évaluer leur impact sur la distorsion du signal audio de sortie.

F.1.1.2 Objectifs industriels

Les concepteurs au sein des deux entreprises citées précédemment tendent de développer des amplificateurs de Classe D avec le moins possible d'émission EM. Cependant, cela n'est pas suffisant si l'amplificateur est mal intégré dans l'application finale. Pour cela, les buts industriels peuvent être résumés comme suit : Développer un outil ou une méthode qui peut assister les intégrateurs de systèmes à implémenter les amplificateurs de Classe D. Le but est d'assister les clients des entreprises à intégrer correctement ces circuits au moment de la conception du produit final. Par suite, la méthode doit être précise, prédictive et facile à utiliser.

F.1.2 Structure du rapport

Le reste du rapport est organisé comme suit.

La section F.2 donne une introduction concise sur le mode de fonctionnement d'un amplificateur de Classe D. Ensuite, les causes d'émission EM d'un amplificateur Classe D et les solutions existantes de réduction des émissions sont brièvement discutées.

La section F.3 présente l'approche de modélisation développée qui est une approche dédiée aux convertisseurs à n conducteurs actifs. Ensuite, une application sur deux cas pratiques sera présentée. Le premier cas est en sortie de l'amplificateur et le deuxième est du côté des rails d'alimentation.

La section F.4 présente un processus d'optimisation qui utilise le modèle de la section F.3. L'optimisation a comme but d'améliorer les trois critères considérés pour ce système qui sont : la réduction des émissions EM de l'amplificateur, la réduction des pertes dues à l'utilisation du filtre et le gain du filtre dans la bande audio. Cette section se termine par une validation expérimentale des résultats.

La section F.5 présente une étude, une modélisation et une quantification de la distorsion audio causée par les composants magnétiques dans un filtre CEM. Le matériau magnétique est modélisé par le modèle de Jiles-Aterthon. Ensuite ce modèle est employé pour la modélisation du composant. Enfin, une simulation temporelle permet de retrouver la cause de distorsion du signal audio. Cette démarche a été validée par des mesures expérimentales.

La section F.6 conclut le rapport et donne des perspectives à ce travail de recherche.

F.2 Les bases et la CEM des amplificateurs de Classe D

Un amplificateur de Classe D est divisé en deux parties [6] : l'étage de puissance et le modulateur. L'étage de puissance est constitué de transistors de puissances qui sont conçus généralement pour avoir le maximum de rendement à la puissance nominale. Son rôle est de fournir la puissance à la charge. Le modulateur est un circuit analogique qui génère un train d'impulsions modulées en fonction du signal

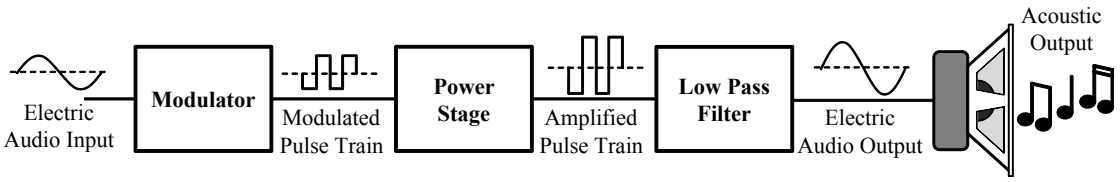


FIGURE F.1: Schéma de base d'un amplificateur de Classe D en boucle ouverte.

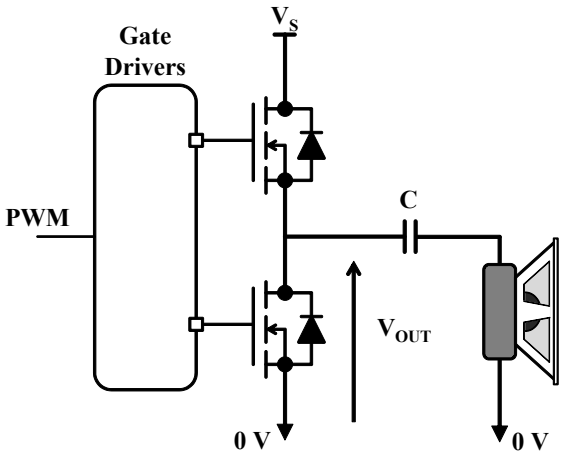


FIGURE F.2: Étage de puissance avec une cellule de commutation.

audio. Son rôle est de contrôler l'étage de puissance. Le schéma de base d'un amplificateur de Classe D en boucle ouverte est donné dans la figure F.1.

F.2.1 Étage de puissance

Il existe deux types d'étages de puissance. Le premier est constitué d'une seule cellule de commutation. Le deuxième est constitué de deux cellules de commutations. Il est aussi nommé « pont en H ». Les deux étages de puissance sont présentés dans les figures F.2 et F.3 respectivement. Dans les deux cas, les commandes de grilles sont utilisées pour introduire un temps mort qui assure que les deux transistors de puissance d'une même cellule de commutation ne conduisent jamais en même temps. Le cas échéant, un court-circuit se produirait entre l'alimentation et la référence ce qui risque d'endommager l'amplificateur.

L'étage de puissance est utilisé « en commutation ». En effet, les transistors de puissance sont utilisés soit en amorçage complet soit en blocage complet. Dit autrement, dans le cas idéal, les transistors sont à tension nulle ou courant nul ce

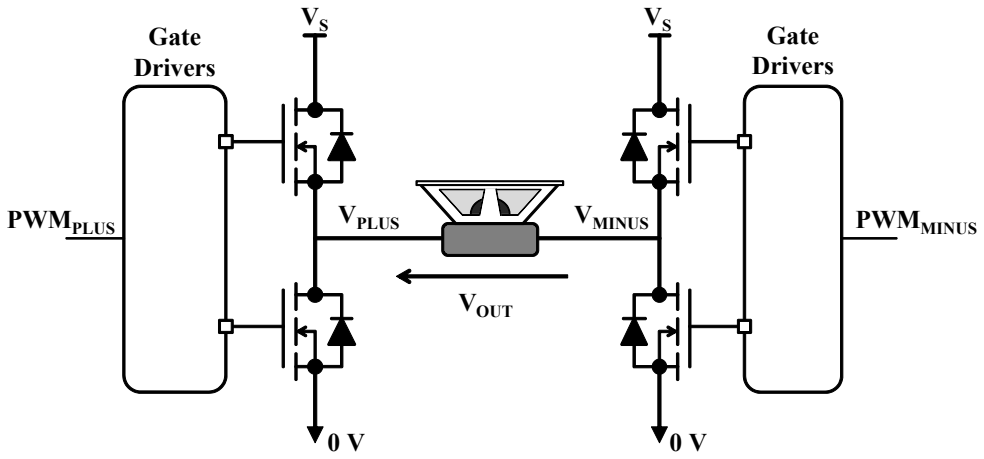


FIGURE F.3: Étage de puissance avec deux cellules de commutations.

qui implique un rendement théorique de 100 %. Néanmoins, en réalité le rendement varie entre 80 et 97 % à cause des imperfections des composants [16, 17].

En général, dans les solutions intégrées, le pont en H est utilisé car il permet de doubler la tension aux bornes de la charge, ce qui permet d'avoir quatre fois la puissance pour la même tension d'alimentation et la même impédance de charge. De plus, le pont en H permet de ne pas inclure la capacité encombrante utilisée dans le cas d'une seule cellule de commutation pour supprimer la composante continue du courant dans la charge.

F.2.2 Modulation

Il existe plusieurs types de modulations pour un amplificateur de Classe D mais seule la Modulation en Largeur d'Impulsions (MLI) est développée dans cette partie. Une MLI [27, 28] est obtenue en comparant le signal audio avec un signal triangulaire (figure F.4). La porteuse qui est le signal triangulaire a une fréquence théoriquement au moins deux fois plus élevée que celle de la fréquence maximale de la bande audio (20 kHz). En pratique, la fréquence de la porteuse est au moins dix fois plus grande que 20 kHz pour améliorer la qualité sonore de l'amplificateur. Dans le cas idéal et pour un signal sinusoïdal, le spectre de la MLI est donné dans figure F.5.

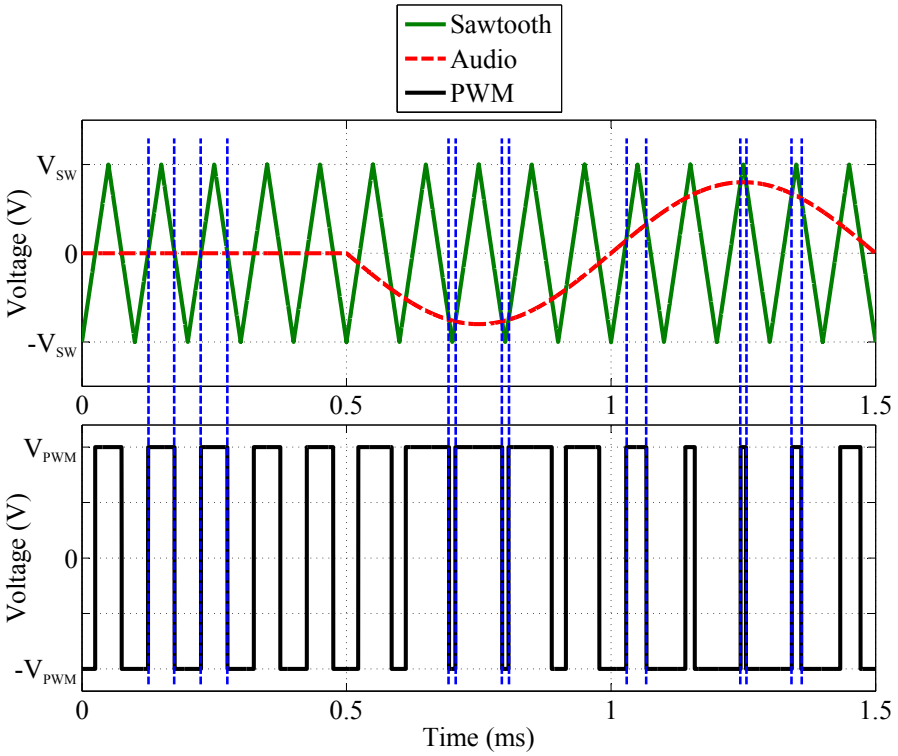


FIGURE F.4: Exemple d'une modulation MLI.

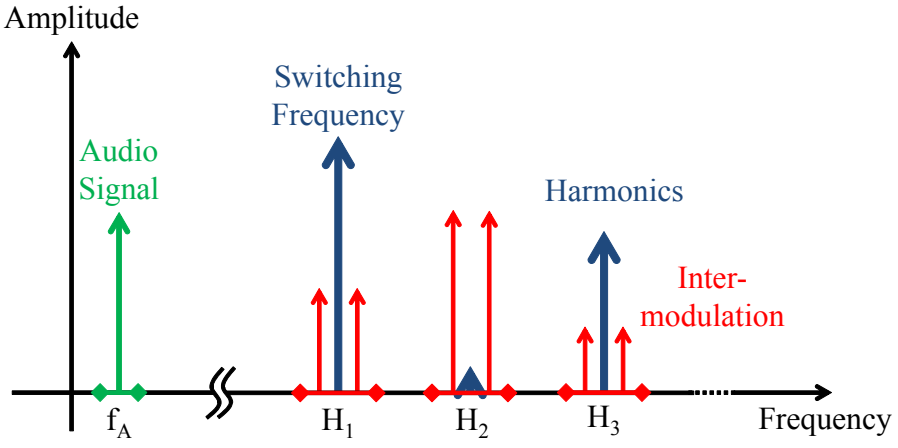


FIGURE F.5: Spectre idéal d'une MLI.

F.2.3 MLI différentielle

Dans le cas d'un étage de puissance constitué de deux cellules de commutation, la MLI peux avoir deux formes : binaire ou ternaire [17]. Dans le cas binaire, les sorties plus et minus commutent en même temps mais de manière complémentaire. Dans le cas ternaire, les deux sorties commutent à des instants différents. Un exemple est

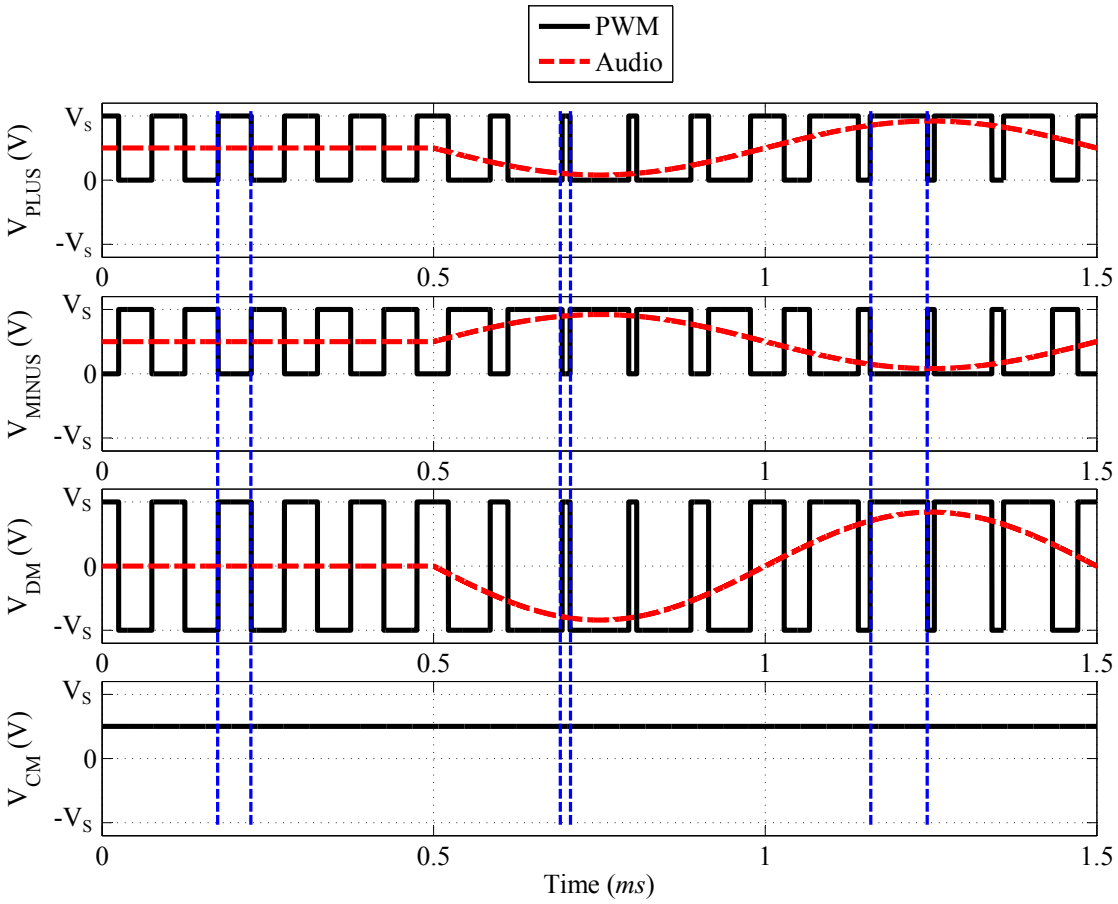


FIGURE F.6: Modulation binaire.

donné dans la figure F.6 pour le cas d'une modulation binaire et dans la figure F.7 pour le cas d'une modulation ternaire.

La modulation ternaire présente plusieurs avantages par rapport à la modulation binaire. Premièrement, en ternaire la commutation a une amplitude de V_s aux bornes de la charge. En binaire, l'amplitude d'une commutation est de deux fois V_s aux bornes de la charge. Deuxièmement, dans le cas d'un signal audio nul, il est possible d'avoir un courant nul dans la charge dans le cas ternaire alors cela n'est pas possible dans le cas binaire. Finalement, il est possible d'annuler les harmoniques impaires aux bornes de la charge. Le seul avantage que présente la modulation binaire est le courant de mode commun nul. Malgré cet avantage, la modulation ternaire est plus souvent employée.

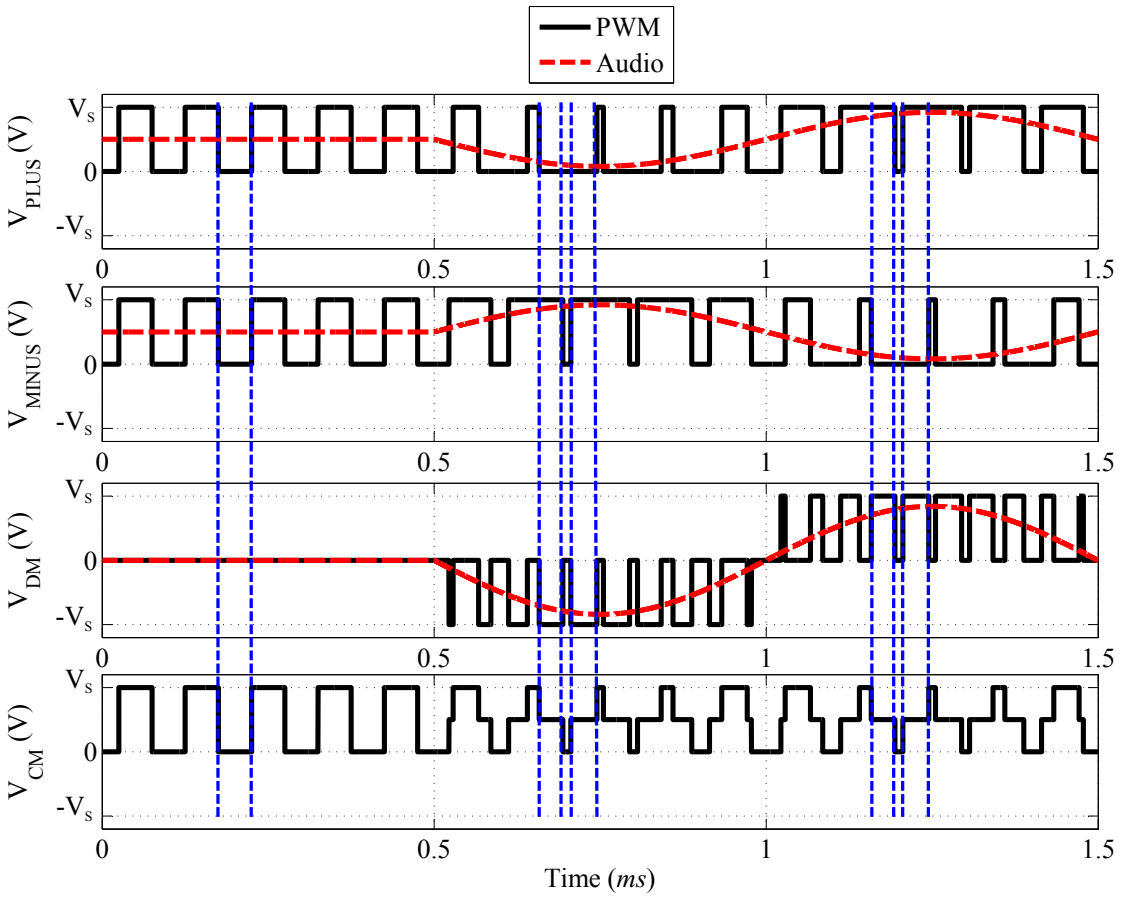


FIGURE F.7: Modulation ternaire.

F.2.4 Émission EM d'un amplificateur de Classe D

La commutation est à l'origine du rendement élevé d'un amplificateur de Classe D. Néanmoins, la commutation est aussi la cause des fortes émissions de cet amplificateur. Un signal carré a par défaut dans le domaine fréquentiel des harmoniques impaires qui décroissent avec une pente négative de -20 dB/décade (figure F.8(b)). Dans le cas réel, le signal ressemble plus à un signal trapézoïdal car le temps d'une commutation n'est pas nul. Par suite, dans le domaine fréquentiel, les harmoniques impaires décroissent avec une pente négative de -40 dB/décade après une fréquence nommée « fréquence de coude » (figure F.8(d)). De plus, dans le cas réel, un circuit commutant comporte des composants capacitifs ou inductifs parasites qui génèrent des oscillations à chaque commutation. Dans le domaine fréquentiel, cela est traduit par des pics supplémentaires aux fréquences de ces oscillations (figure F.8(f)). Dans le cas d'un amplificateur de Classe D, le signal carré est modulé par rapport au signal audio. Donc, autour de chaque harmonique (pair et impaire) des pics

d'intermodulation apparaissent (figure F.8(h)). Si on considère d'autres aspects dans un système réel comme les temps morts, la non-linéarité des composants, les diodes parasites des MOSFET... on peut conclure que le spectre de sortie d'un amplificateur est complexe. L'amplificateur de Classe D module donc la puissance avec un spectre complexe, ce qui fait de ce circuit une source de perturbations EM.

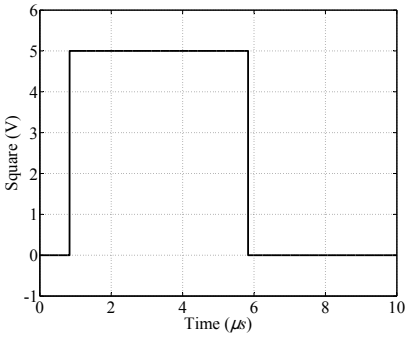
Un amplificateur de Classe D n'est pas seulement une source de perturbations sur les rails de sorties, mais aussi sur les rails de l'alimentation. En effet, généralement, dans les dispositifs portables, la batterie est la seule source d'énergie. Il y a donc une alimentation commune à toutes les applications dans ce dispositif, y compris l'amplificateur de Classe D. À cause des éléments parasites, les commutations et d'autres phénomènes comme par exemple le « pompage de la charge », l'amplificateur de Classe D génère des perturbations conduites aux bornes de la batterie qui aussi ont un couplage avec avec d'autres circuits par impédance commune. Ce point peut être résumé dans la figure F.9.

F.2.5 Caractérisation d'un amplificateur de Classe D

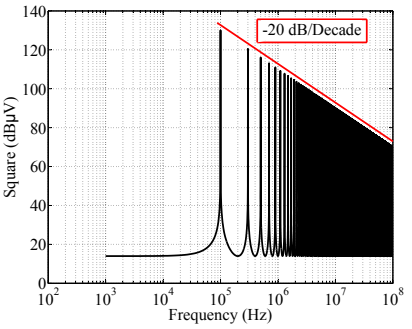
Mis à part la CEM et le rendement énergétique, il existe plusieurs critères pour évaluer un amplificateur de Classe D. Il y a ceux qui sont dédiés à la qualité audio et d'autres à la qualité énergétique. Le tableau F.1, donne quelques ordres de grandeurs en relation avec un amplificateur de Classe D.

F.3 Modélisation des amplificateurs de Classe D du point de vue de la CEM

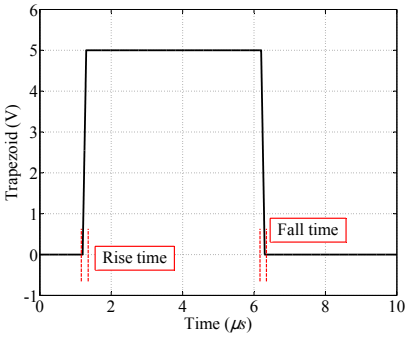
La simulation est un moyen qui permet d'optimiser le filtre CEM efficacement et avec un coût réduit. Cependant, pour avoir une simulation fiable il faut trouver un modèle adapté. Pour la CEM, les modèles adaptés sont, soit les modèles dans le domaine temporel suivis d'une FFT [49], soit les modèles dans le domaine fréquentiel. Vu le temps nécessaire pour concevoir et simuler un modèle temporel, un modèle fréquentiel est avantageux. Cependant, les modèles trouvés dans la littérature ne sont pas adaptés au besoin de cette étude. Pour cela un modèle



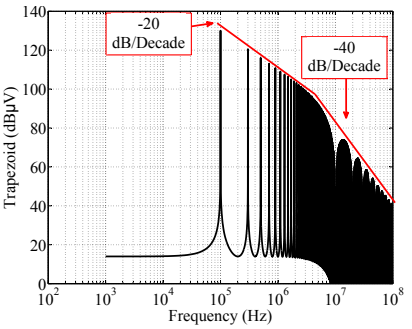
(a) Signal carré dans le domaine temporel



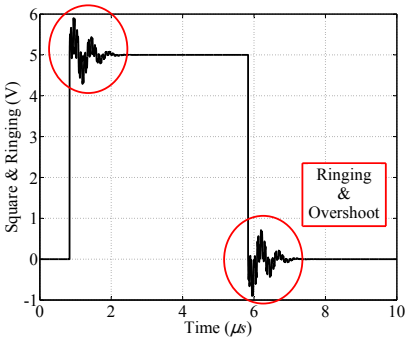
(b) Signal carré dans le domaine fréquentiel



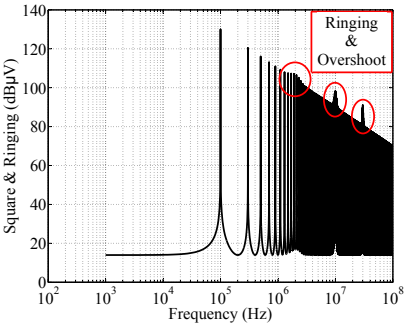
(c) Signal Trapézoïdal dans le domaine temporel



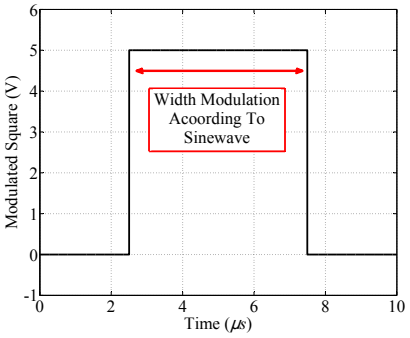
(d) Signal Trapézoïdal dans le domaine fréquentiel



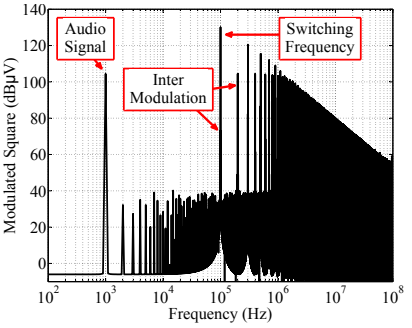
(e) Signal carré avec oscillations dans le domaine temporel



(f) Signal carré avec oscillations dans le domaine fréquentiel



(g) Signal carré en MLI dans le domaine temporel



(h) Signal carré en MLI dans le domaine fréquentiel

FIGURE F.8: Contenu fréquentiel d'un amplificateur de Classe D

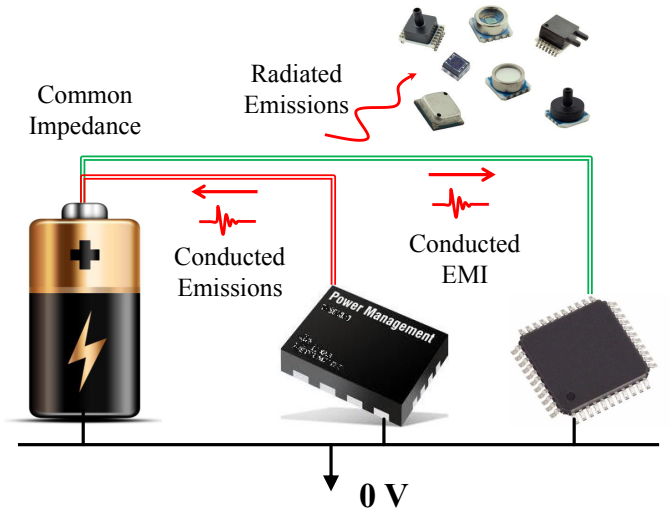


FIGURE F.9: Émissions EM au niveau des rails de sorties.

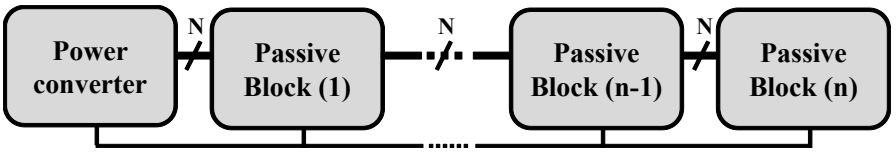


FIGURE F.10: Modèle proposé.

fréquentiel plus adapté a été développé. Les spécifications du modèle sont données ci-dessous.

1. Précision en haute fréquence en particulier dans la bande des émissions conduites.
2. Applicabilité sur un amplificateur de Classe D avec une ou deux cellules de commutations (pont en H).
3. Prise en compte du mode commun (MC), du mode différentiel (MD) et du transfert de mode.
4. Mise en évidence des chemins de couplages.
5. Utilisation possible en phase de conception.
6. Temps de simulation court.

Pour répondre à ces spécifications nous proposons le modèle présenté dans la figure F.10. Il consiste à décomposer un système à N-conducteurs actifs en blocs.

TABLE F.1: Ordre de grandeur d'un amplificateur de Classe D. [17, 47, 48]

Amplitude	[Unité]	**Valeur minimale**	**Valeur maximale**
Puissance de sortie	[W]	$0,5$	300
Rendement à puissance maximale	[%]	80	97
Tension d'alimentation	[V]	$2,5$	100
Fréquence audio	[Hz]	20	24000
Fréquence de commutation	[kHz]	100	3000
Temps de monté/descente	[ns]	5	50
Impédance de la charge	[Ω]	2	64
Taux de distorsion harmonique	[dB]	50	90
Rapport signal sur bruit	[dB]	80	110
Taux de réjection de l'ondulation de l'alimentation	[dB]	60	110
Surface du substrat	[mm^2]	$0,1$	10
Coût de puce (Carte non inclue)	[$]	$0,1$	15
Coût du filtre CEM	[$]	$0,5$	10

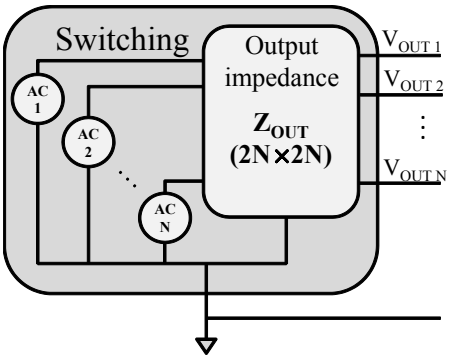


FIGURE F.11: Modèle des blocs actifs.

D'une part, on identifie les blocs actifs comme les convertisseurs de puissances ou les amplificateurs de Classe D. D'une autre part, on identifie les blocs passifs comme les filtres, le haut-parleur, les pistes... Les blocs actifs sont modélisés par des sources de tensions et une matrice d'impédances équivalente à l'impédance de sortie du convertisseur (figure F.11). Les blocs passifs sont modélisés par des matrices d'impédances $2N \times 2N$ s'ils sont situés au milieu de la chaîne et par des matrices d'impédances $N \times N$ s'ils sont situés à l'extrémité de la chaîne. Les

blocs passifs peuvent être concaténés pour former une seule matrice d'impédances équivalente. L'ensemble des matrices permet de calculer les spectres de tensions ou de courants à tous les nœuds du système. Cette méthode n'est applicable que si le système en question répond aux conditions suivantes :

1. Aucune boucle de réaction n'est présente au niveau des blocs passifs suivant le convertisseur.
2. Aucun couplage important n'existe entre les blocs. Dit autrement, le comportement d'impédance d'un bloc ne change pas après découpage.
3. Les blocs doivent être électriquement courts (dimensions $\ll$ longueur d'onde).
4. Les composants passifs sont utilisés dans une plage pour laquelle ils peuvent être considérés linéaires.

F.3.1 Identification des paramètres du modèle

L'identification des paramètres du modèle consiste d'une part à déterminer les sources de tensions et la matrice d'impédances du convertisseur et d'autre part les matrices d'impédances des différents blocs passifs. Plusieurs méthodes existantes dans la littérature peuvent être utilisées pour la détermination du modèle du convertisseur (source et impédance de sortie) [67–73]. Les blocs passifs peuvent être déterminés par simulation ou par mesure. Les méthodes étudiées dans ce travail sont soit la mesure à l'aide d'un analyseur d'impédance, soit la mesure à l'aide d'un VNA, soit la simulation avec le logiciel Advanced Design System (ADS) [75].

La détermination d'une matrice d'impédances à l'aide d'un analyseur d'impédance se fait en deux parties. La première est la mesure des éléments de la diagonale en les mesurant directement sur les ports en question. La deuxième est le calcul des éléments croisés à l'aide de l'équation F.1.

$$z_{ij} = \sqrt{z_{jj}(z_{ii} - z_{ij_{sc}})} \quad ; \quad i \neq j \tag{F.1}$$

Où z_{ij} est l'élément croisé à déterminer, z_{ii} et z_{jj} sont les éléments i et j de la diagonale et $z_{ij_{sc}}$ est l'impédance mesure du port i quand le port j est en court-circuit.

La détermination d'une matrice d'impédances à l'aide d'un VNA se fait aussi en deux parties. La première est la mesure des paramètres S à l'aide du VNA. La deuxième consiste à convertir la matrice S en une matrice d'impédances à l'aide de l'équation F.2.

$$Z = (I - S)^{-1} \cdot (I + S) \cdot Z_0 \tag{F.2}$$

Où Z est la matrice d'impédances à déterminer, S est la matrice à convertir, I est une matrice d'identité de la même dimension que S et Z et Z_0 est l'impédance caractéristique du VNA.

La détermination de la matrice d'impédances à l'aide d'un logiciel de simulation, pourra demander des niveaux différents de complexité du modèle selon la bande de fréquences désirée. Plus la fréquence maximale désirée est élevée, plus le modèle aura besoin de détails pour avoir une précision acceptable.

F.3.2 Association de matrices d'impédances

Deux types d'association de matrices peuvent être distingués.

- Une association de deux matrices de dimensions $2N \times 2N$. Ceci conduit à une matrice qui a la même dimension.
- Une association d'une matrice de dimension de $2N \times 2N$ avec une autre de dimension de $N \times N$/ Le résultat est alors une matrice de dimension $N \times N$.

Pour associer deux matrices de dimension $2N \times 2N$ nommées k et m, on les divise en quatre sous-matrices de dimension $N \times N$ comme présenté dans l'équation F.3. On applique ensuite l'équation F.4 pour obtenir la matrice équivalente.

$$Z_k = \left(\begin{array}{c|c} Z_{k\,11} & Z_{k\,12} \\ \hline Z_{k\,21} & Z_{k\,22} \end{array}\right) \quad ; \quad Z_m = \left(\begin{array}{c|c} Z_{m\,11} & Z_{m\,12} \\ \hline Z_{m\,21} & Z_{m\,22} \end{array}\right) \tag{F.3}$$

$$Z_{km} = \begin{pmatrix} Z_{km\,11} & Z_{km\,12} \\ Z_{km\,21} & Z_{km\,22} \end{pmatrix} \tag{F.4}$$

avec :

$Z_{km\,11} = Z_{k\,11} - Z_{k\,12}(Z_{k\,22} + Z_{m\,11})^{-1} Z_{k\,21}$

$Z_{km\,12} = Z_{k\,12}(Z_{k\,22} + Z_{m\,11})^{-1} Z_{m\,12}$

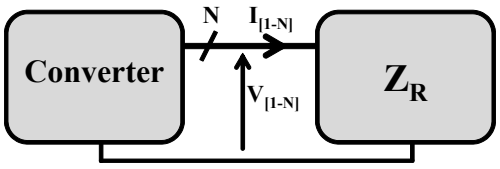


FIGURE F.12: Calcul du spectre du courant à la sortie du convertisseur.

$Z_{km\,2\,1} = Z_{m\,2\,1}(Z_{k\,2\,2} + Z_{m\,1\,1})^{-1} Z_{k\,2\,1}$
$Z_{km\,2\,2} = Z_{m\,2\,2} - Z_{m\,2\,1}(Z_{k\,2\,2} + Z_{m\,1\,1})^{-1} Z_{m\,1\,2}$
L'autre type d'association (matrice de dimension $2N \times 2N$ avec une autre de dimension $N \times N$) se fait en utilisant l'équation F.5. Ici on associe la matrice d'un bloc appelé km $(2N \times 2N)$ avec une charge L $(N \times N)$.

$$Z_{kmL} = Z_{km\,1\,1} - Z_{km\,1\,2}(Z_L + Z_{km\,2\,2})^{-1} Z_{km\,2\,1} \tag{F.5}$$

F.3.3 Calcul des spectres de tensions et de courants

Une fois les matrices associées, on obtient une seule matrice résultante de dimension $N \times N$ nommée Z_R (figure F.12). L'équation F.6 permet donc de calculer les spectres des courants à la sortie du convertisseur.

$$\begin{pmatrix} I_1 \\ \vdots \\ I_N \end{pmatrix} = (Z_R)^{-1} \begin{pmatrix} V_1 \\ \vdots \\ V_N \end{pmatrix} \tag{F.6}$$

Les spectres de tensions et de courants sur les autres nœuds du système peuvent être aussi calculés par les équations F.7 et F.8 respectivement. Ici on considère un nœud après un bloc nommé k (figure F.13).

$$\begin{pmatrix} V_{OUT\,1} \\ \vdots \\ V_{OUT\,N} \end{pmatrix} = (I + Z_{[1\to k]22} \cdot Z^{-1}_{[k+1\to n]})^{-1} Z_{[1\to k]21} \cdot Z^{-1}_{[k+1\to n]} \begin{pmatrix} V_{IN\,1} \\ \vdots \\ V_{IN\,N} \end{pmatrix} \tag{F.7}$$

$$\begin{pmatrix} I_{OUT\,1} \\ \vdots \\ I_{OUT\,N} \end{pmatrix} = Z^{-1}_{[k+1\to n]} \begin{pmatrix} V_{OUT\,1} \\ \vdots \\ V_{OUT\,N} \end{pmatrix} \tag{F.8}$$

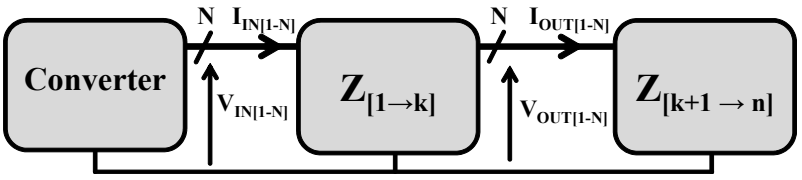


FIGURE F.13: Calcul du spectre de tensions et de courants après un bloc nommé k.

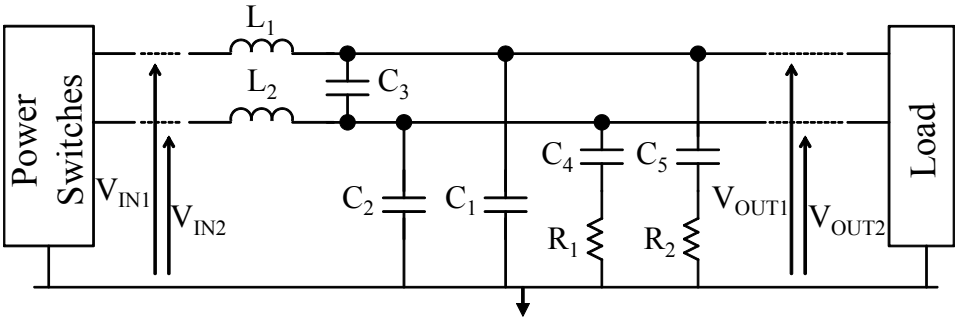


FIGURE F.14: Filtre utilisé.

F.3.4 Validation expérimentale avec un amplificateur de Classe D

Une application expérimentale est nécessaire pour valider l'approche. Pour cela, on a considéré un amplificateur de Classe D monté sur une carte de test. L'amplificateur est dédié à des applications de téléphonie mobile avec une puissance de sortie de 700 mW, une fréquence de découpage de 412 kHz et une tension d'alimentation de 3,6 V. On a considéré un filtre CEM existant dans la littérature [84] (figure F.14) dédié à des amplificateurs de Classe D et une charge équivalente à un haut-parleur (figure F.15) qui est généralement utilisée dans le processus de validation d'un amplificateur de Classe D. Les valeurs nominales des composants du filtre et de la charge sont montrées dans les tableaux F.2 et F.3 respectivement. Les différents blocs sont donc montés sur des cartes séparés pour valider le processus d'association comme il est montré dans la figure F.16.

F.3.5 Détermination du modèle des différentes parties du système

Pour déterminer le modèle de l'amplificateur de Classe D, on commence par mesurer les spectres de sortie de l'amplificateur avec différentes charges : circuit ouvert,

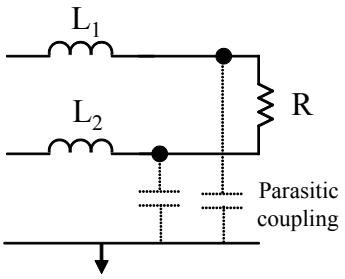


FIGURE F.15: Charge utilisée pour les tests.

TABLE F.2: Valeurs nominales des composants du filtre.

L_1, L_2	15	μH
C_1, C_2	33	nF
C_4, C_5	68	nF
C_3	150	nF
R_1, R_2	22	Ω

TABLE F.3: Valeurs nominales des composants de la charge.

L_1, L_2	15	μH
R	8	Ω

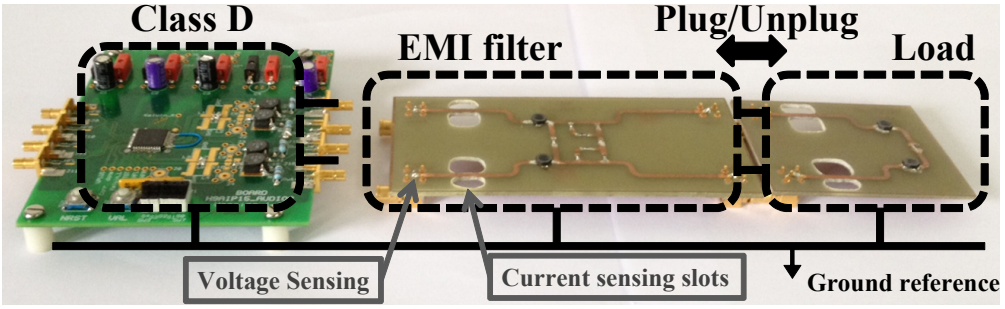


FIGURE F.16: Application de l'approche sur un amplificateur de Classe D.

haut-parleur et finalement le filtre et le haut-parleur ensemble. Les résultats sont montrés dans la figure F.17. Cette dernière montre que le spectre de sortie de l'amplificateur est indépendant de la charge mise à sa sortie. Donc on peut conclure que, sur cette bande de fréquences, l'impédance de sortie de l'amplificateur est négligeable devant celle du filtre et de la charge. Par suite le modèle peut être réduit à seulement deux sources de tension.

Les matrices d'impédances du filtre et de la charge ont été déterminées par mesure (Analyseur d'impédance et VNA) et par simulation. Une impédance de la diagonale est montrée dans la figure F.18(a) et une impédance croisée est montrée dans la figure F.18(b). On peut voir que les trois méthodes donnent des résultats concordants pour les éléments de la diagonale. Cependant, des différences peuvent être identifiées pour les éléments croisés. Cela est dû à la précision minimale des

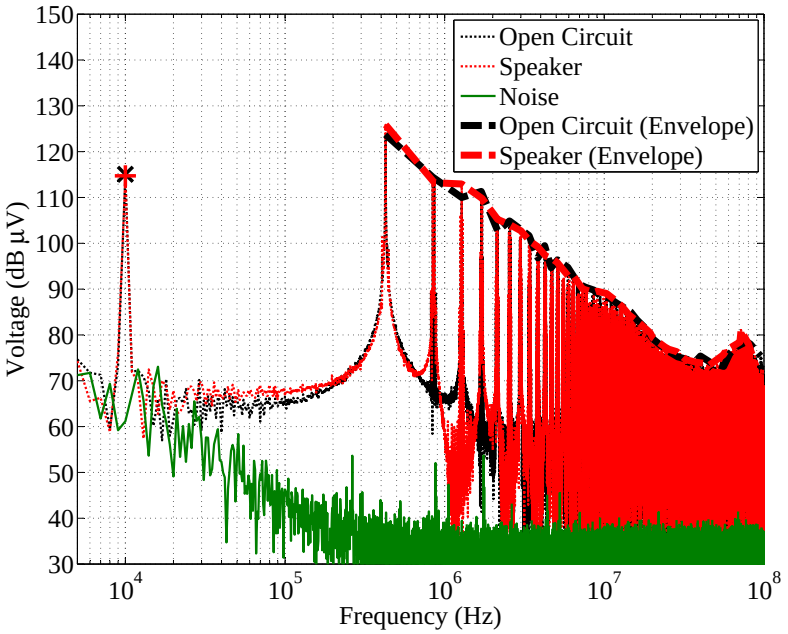


FIGURE F.17: Tension de sortie de l'amplificateur avec deux charges différentes.

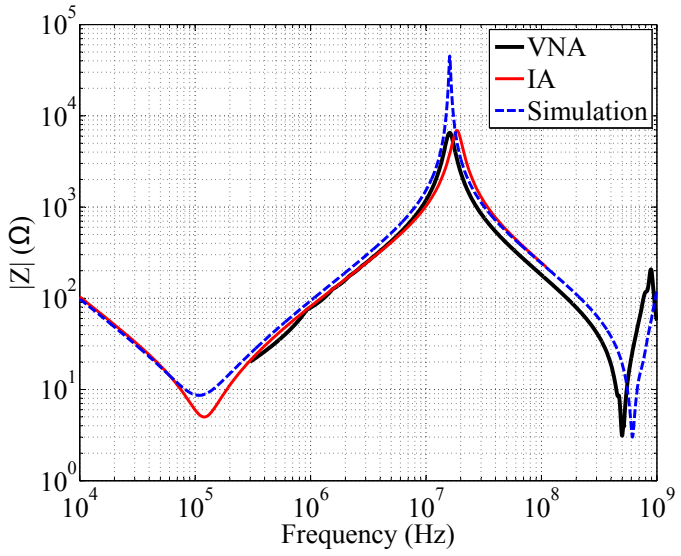
instruments de mesures qui induisent des incertitudes dans les données qui sont traitées par les calculs numériques.

Les matrices d'impédances étant déterminées, elles sont utilisés pour le calcul des spectres de tension et de courant à la sortie de l'amplificateur et à la sortie du filtre. Les résultats sont montrés dans les figures F.19, F.21 et F.20.

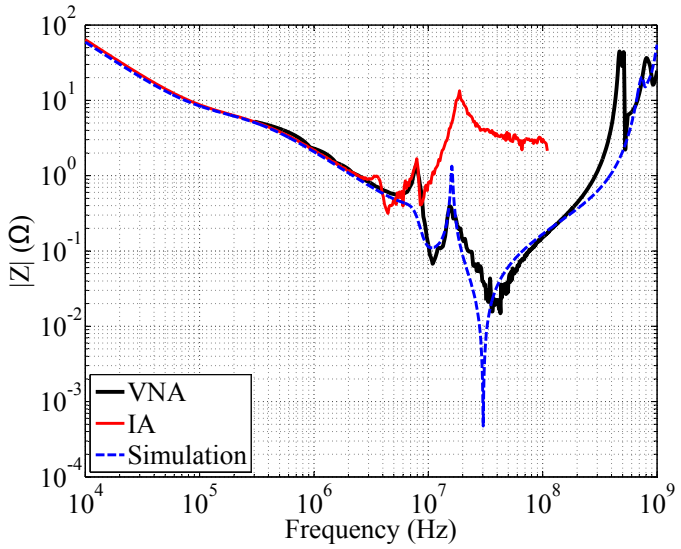
La figure F.19 montre que les spectres mesuré et calculé se superposent jusqu'à 100 MHz. On peut donc déduire que la méthode est précise jusqu'à cette fréquence. Cependant, dans les figures F.20 et F.21, la comparaison n'est possible que sur une partie de la bande de fréquence car le niveau des spectres est inférieur à celui du bruit de mesure.

F.3.6 Exemple de validation sur une batterie et un convertisseur DC-DC

Pour valider expérimentalement cette technique, un convertisseur DC-DC (Musimi VT-0312) et une batterie de téléphone portable (Nokia BL-5CA) ont été utilisés. Comme la fréquence de découpage du convertisseur est de 1,2 MHz, l'impédance de la batterie a été mesurée de 1 MHz à 100 MHz. Les résultats de mesures sont montrés dans la figure F.22.



(a) z_{11}



(b) z_{14}

FIGURE F.18: Impédances du filtre.

Comme la figure F.22 montre que les impédances mesurée et calculée ne sont pas identiques. Cela montre alors que l'impédance du quadripole utilisé pour protéger l'analyseur d'impédance de la tension continue produite par la batterie n'est pas négligeable. Cette figure montre aussi que cette batterie est inductive sur cette bande de fréquence. Ce résultat n'est pas évident a priori.

Pour s'assurer que l'impédance calculée est valide, une validation expérimentale a été effectuée. Le convertisseur mentionné ci-dessus a été utilisé avec la même batterie. Ensuite, le courant dans le domaine temporel a été mesuré à l'aide d'un oscilloscope, puis le spectre fréquentiel a été déduit en utilisant une FFT. En

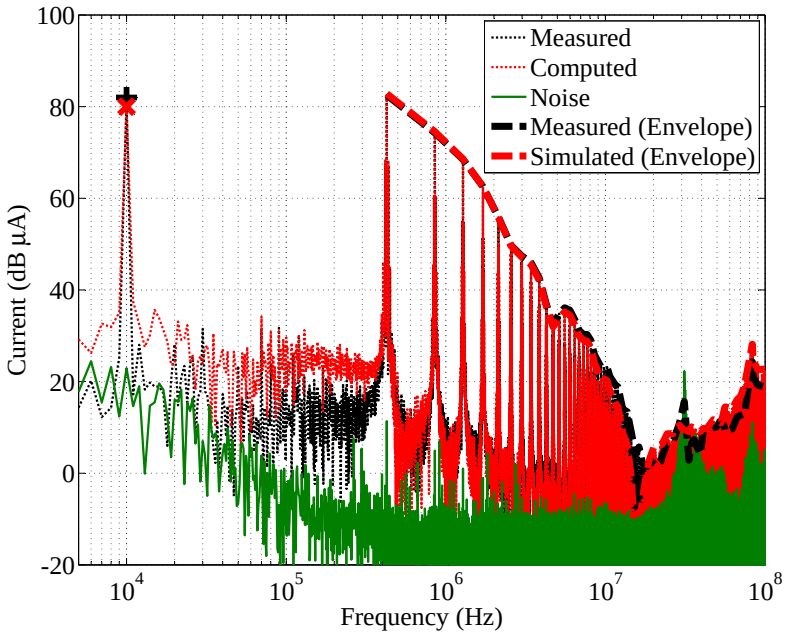


FIGURE F.19: Courant d'entrée du filtre $I_{IN_{Plus}}$.

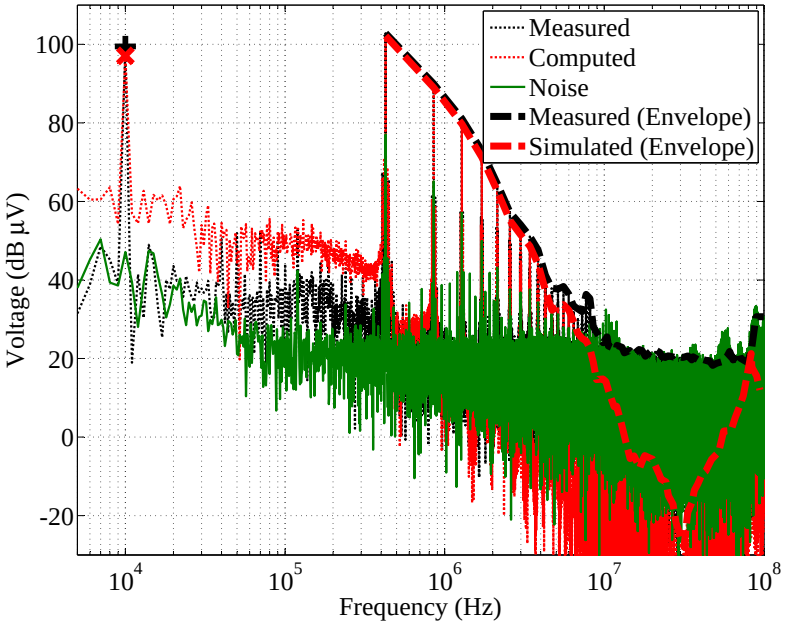


FIGURE F.20: Tension de sortie du filtre $V_{OUT_{Plus}}$.

multipliant ce spectre par l'impédance de la batterie, le spectre de la tension aux bornes de la batterie a été obtenu. La comparaison avec le spectre de la tension mesurée est montrée dans la figure F.23.

On remarque que les deux spectres se superposent jusqu'à 80 MHz. Au-dessus de cette fréquence le niveau de bruit ne permet pas de comparer. On conclut alors que l'impédance mesurée de la batterie est valide au moins jusqu'à 80 MHz.

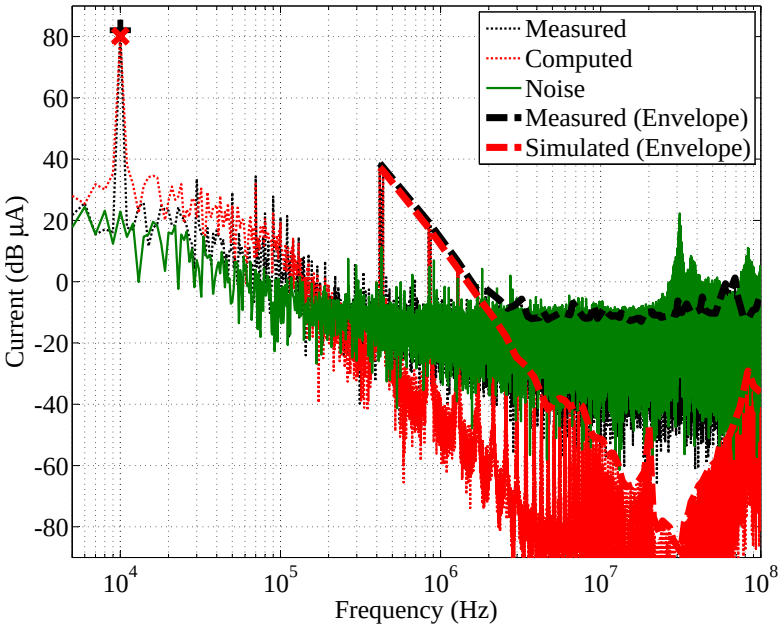


FIGURE F.21: Courant de sortie du filtre $I_{OUT_{Plus}}$.

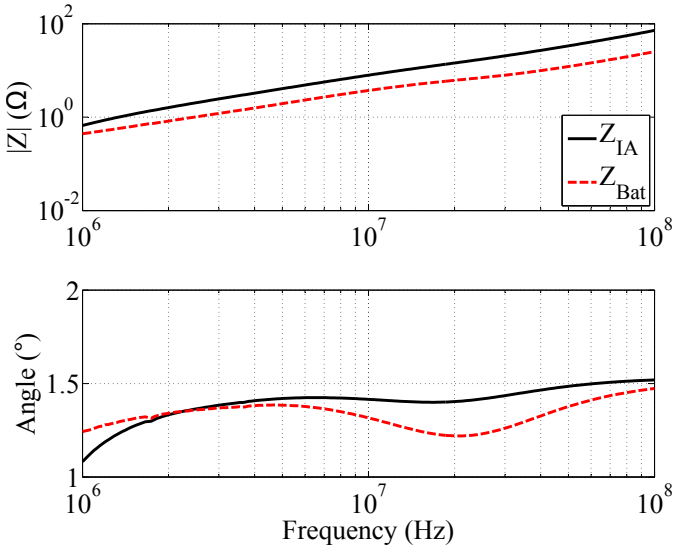


FIGURE F.22: Impédance de la batterie

F.4 Optimisation discrète du filtre CEM

La conception d'un filtre CEM n'est pas une simple tâche. Celle-ci est fortement impactée par les éléments parasites. Les méthodes classiques de design de filtre sont souvent insuffisantes pour la CEM, ce qui mène les ingénieurs à faire des mesures expérimentales répétitives sur une multitude de prototypes. De plus, dans le cas d'un amplificateur de Classe D pour la téléphonie mobile, en plus de la CEM il existe d'autres critères qu'il faut considérer comme le rendement énergétique de l'amplificateur, la qualité du signal audio et la surface occupée sur un PCB.

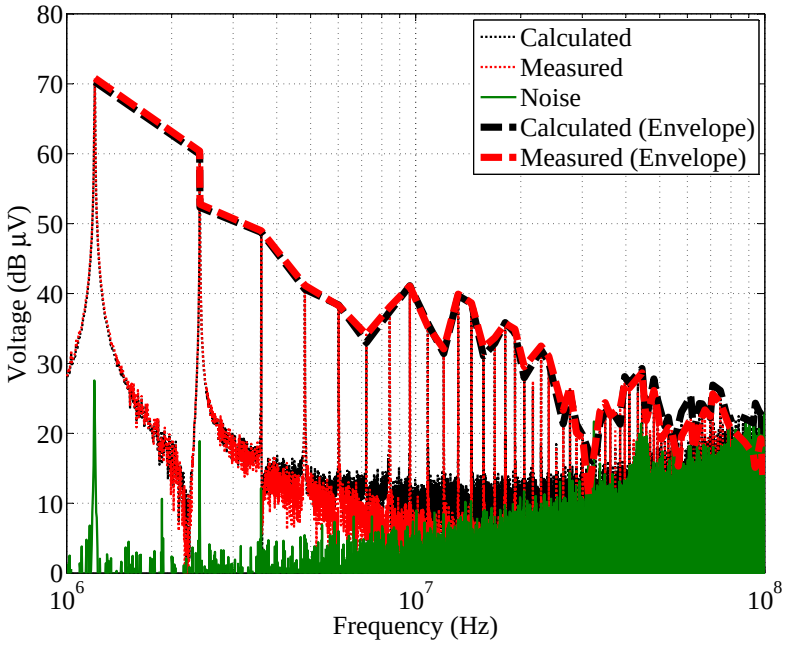


FIGURE F.23: Amplitude de la tension aux bornes de la batterie

Cela rend cette tâche lourde et longue. On propose donc dans ce paragraphe une méthode alternative basée sur le modèle fréquentiel déjà développé et sur un algorithme d'optimisation.

Pour comprendre l'impact du filtre CEM sur le rendement énergétique d'un amplificateur de Classe D, on considère le cas de la figure F.24. Pour un signal audio nul, les tensions MLI du bras positif et négatif sont égales et donc aucun courant ne traverse la charge. On peut remarquer alors qu'à chaque période, les capacités sont chargées à travers l'interrupteur du haut et déchargées à travers l'interrupteur du bas comme l'indiquent les flèches. Cela engendre des pertes dans les résistances parasites des inductances, des interrupteurs de puissances et des capacités pour une puissance utile qui est nulle. En général, pour un enregistrement audio (chansons ou autre), la plupart du temps (plus que 50 % du temps total), les niveaux du signal sont inférieurs à -20 dB du niveau maximal du même enregistrement. Ce qui nous permet de déduire qu'un filtre de CEM pourra avoir un impact significatif sur le rendement d'un amplificateur de Classe D.

F.4.1 Méthodologie de design du filtre

La méthode proposée pour la conception d'un filtre CEM est divisée en deux parties : (i) la détermination de la topologie de filtre et (ii) le choix des composants.

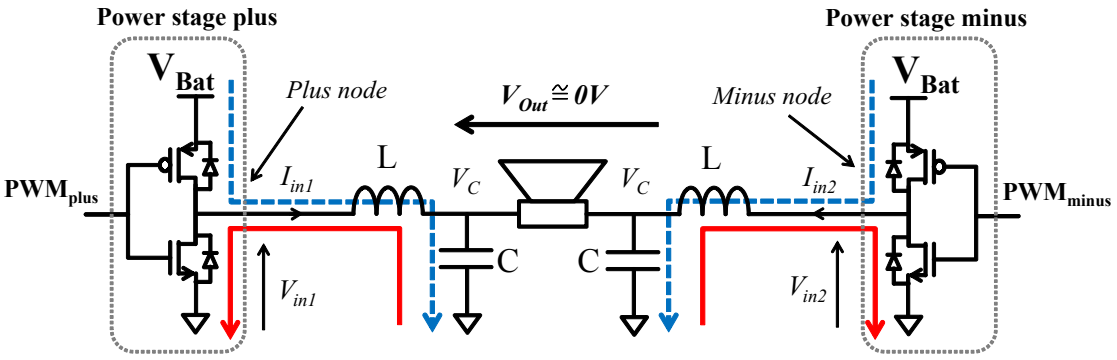


FIGURE F.24: Circulation de courants dûs au filtre CEM.

En général, les structures classiques présentes dans la littérature répondent aux besoins de la plupart des applications. Une fois la structure fixée, les composants sont choisis par optimisation. Le choix de l'algorithme d'optimisation est très important. Vu que les composants présents sur le marché sont discrets, nous avons choisi de faire une optimisation discrète basée sur un algorithme génétique.

F.4.2 Processus d'optimisation

Le processus d'optimisation développé est une combinaison entre l'algorithme génétique et le modèle fréquentiel développé dans les paragraphes précédents. Le processus est décrit dans la figure F.25. Il est composé :

- d'une boucle d'optimisation basée sur un algorithme génétique contenant :
  - un modèle de filtre implémenté dans le logiciel ADS qui définit :
    - la structure du filtre ;
    - le routage du filtre ;
  - un modèle fréquentiel développé précédemment qui définit
    - les émissions de la source ;
    - l'impédance de la charge ;
  - la fonction objectif qui définit :
    - les objectifs ;
    - les contraintes ;
- d'une base de données de composants passifs qui :

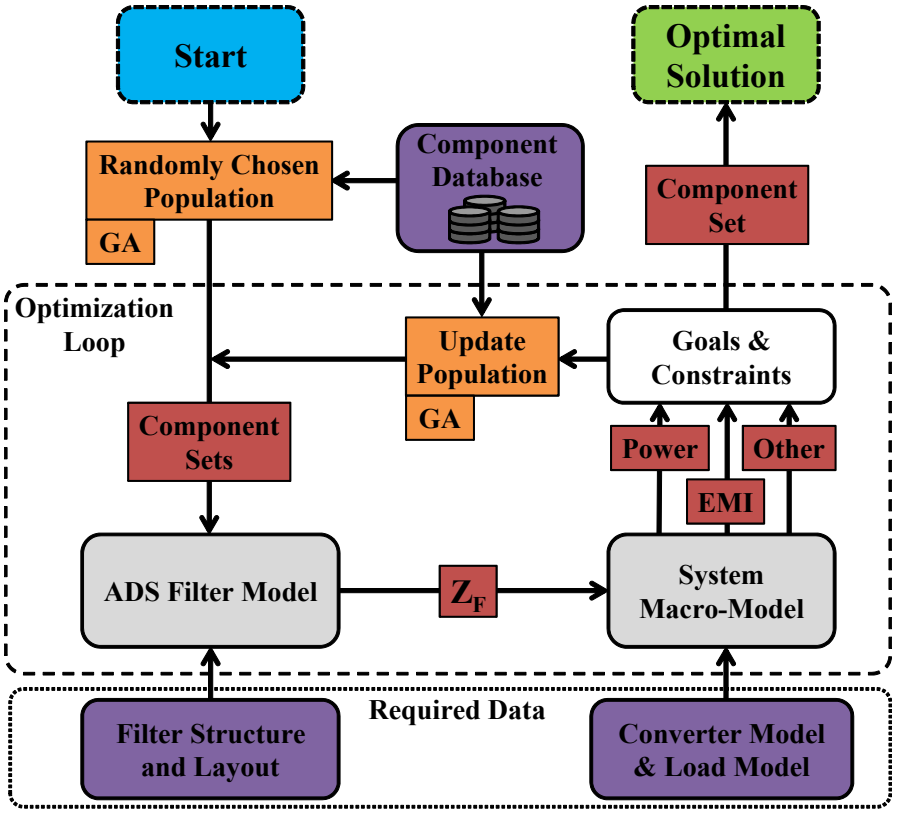


FIGURE F.25: Processus d'optimisation.

- contient des librairies de capacités et d'inductances de différents constructeurs ;
- pointe sur des modèles haute fréquence des composants passifs.

Dans la figure F.25, la succession des opérations est la suivante. Une population initiale est générée aléatoirement par l'algorithme génétique : les composants sont choisis de la base de données. Chaque individu de cette population correspond à un jeu de composants définissant un filtre. Cette population et la géométrie des pistes du filtre implémentée dans ADS permettent de calculer le modèle du filtre avec les différents individus afin de générer une matrice d'impédances pour chaque filtre. Ces matrices sont ensuite intégrées au modèle fréquentiel afin de calculer les spectres de tensions, de courants, et aussi les critères d'optimisation (pertes, atténuation du signal audio...) pour chaque individu. Finalement, l'algorithme génétique génère une nouvelle population à partir de la base de données en se basant sur la fonction objectif. À la dernière itération, le meilleur filtre sera considéré comme le filtre optimal.

TABLE F.4: Référence des composants du filtre optimal.

Composant	Valeur nominale	Référence
L_1, L_2	22 μH	$CLF7045T-220M$
C_1, C_2	0,74 μF	$GRM155R60J474KE19$
C_4, C_5	1,2 pF	$GRM1535C1H1R2CDD5$
C_3	0,1 μF	$GRM155R61H104KE19$
R_1, R_2	1,6 Ω	$MC0.0625W04021\%1R60$

F.4.3 Application à un amplificateur de Classe D

L'amplificateur de test utilisé précédemment est réutilisé ici pour évaluer cette méthode d'optimisation. Le pire des cas pour les émissions électromagnétiques a été identifié et les spectres de tensions correspondant ont été utilisés pour l'optimisation. La structure du filtre présentée dans la figure F.14 a été choisie pour l'optimisation. Celle-ci a neuf composants dont deux inductances, deux résistances et cinq capacités. Cependant, la symétrie physique du filtre permet de réduire le nombre de variable à cinq. Les composants CMS considérés dans l'optimisation sont ceux de deux constructeurs de composants passifs. Les *design kits* relatifs à ces composants sont fournis par les constructeurs. La base de données correspondante à ces deux librairies a été construite dans Matlab.

F.4.4 Formulations pour le processus d'optimisation

Deux formulations différentes ont été faites pour le même amplificateur. Dans ce résumé une seule formulation est présentée. Celle-ci a comme but de minimiser les pertes dans le filtre de CEM tout en gardant le niveau des émissions EM sous un seuil donné et aussi sans atténuer le signal audio dans la bande des fréquences audio. Ce filtre optimisé ne doit pas être plus encombrant que le filtre de référence. Pour cela, on a fixé les tailles des différents composants du filtre et le routage de la carte.

L'optimisation est exécutée et le résultat est la liste des références des composants du filtre optimal (tableau F.4). Les performances du filtre qui minimise les pertes sont données dans le tableau F.5 ; les émissions EM sont données dans les figures F.26 et F.27.

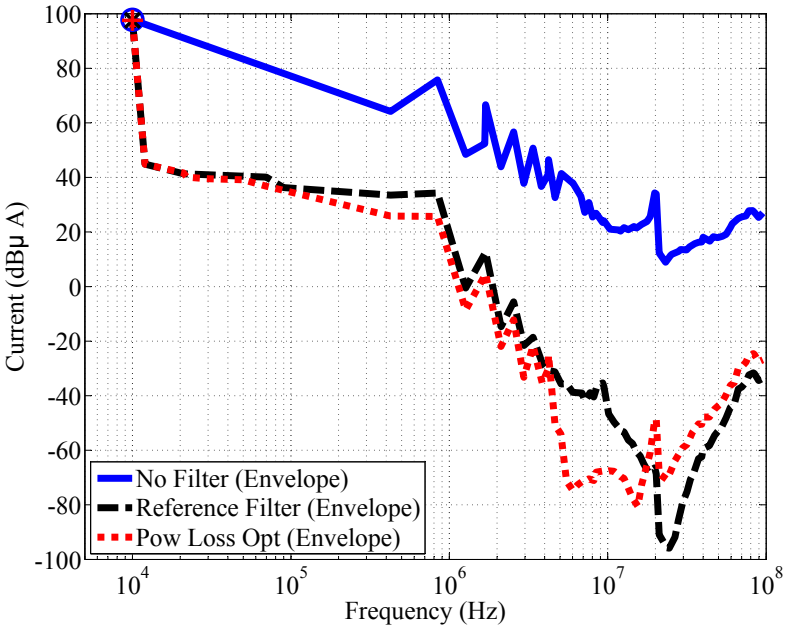


FIGURE F.26: Courants de sortie du filtre.

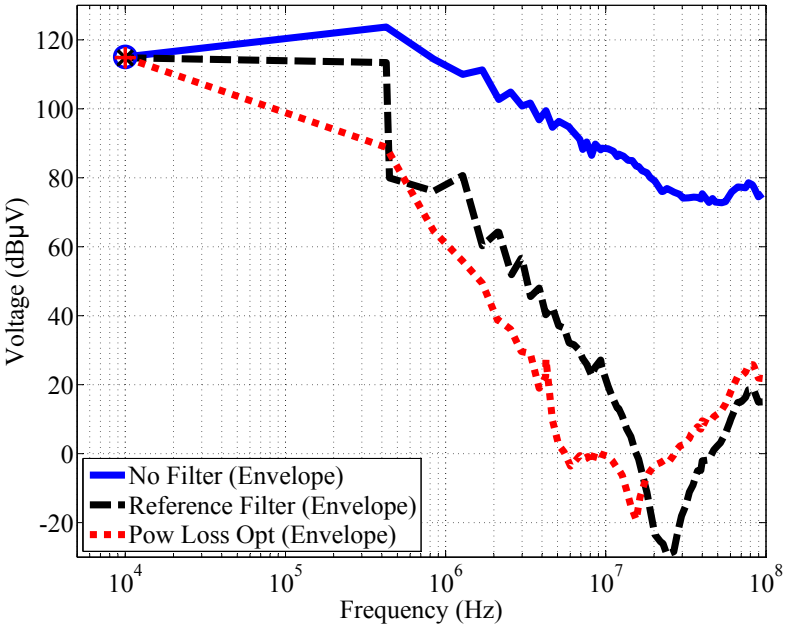


FIGURE F.27: Tensions de sortie du filtre.

TABLE F.5: Comparaison des puissances et pertes pour différents filtres

	P_{PS} [mW]	P_{FL} [mW]	P_A [mW]	P_{Losses} [mW]
Sans de filtre	3	84,4	82,5	4,9
Avec filtre de référence	5,7	139,1	78,8	66
Avec filtre CEM optimal	4,2	96,5	85,5	15,2

Étant donné que P_{PS} représente les pertes de puissances dans l'étage de puissance, P_{FL} est l'énergie transmise à l'ensemble filtre plus charge, P_A est la puissance utile du signal audio dans la charge et P_{Losses} représente la totalité des pertes dans l'étage de puissance, le filtre et la charge, le tableau F.5 montre que le filtre de référence augmente de 13 fois les pertes de l'amplificateur de Classe D par rapport au cas où il n'y a pas filtre. Cependant, le filtre optimal permet de réduire ces pertes à seulement 2,5 fois les pertes obtenues dans le cas où aucun filtre n'est utilisé.

Les figures F.26 et F.27 montrent que le filtre optimal permet d'améliorer les spectres de tension et courant de sortie du filtre jusqu'à 20 MHz. Les pics avec le filtre de référence sont plus élevés que ceux du spectre obtenu avec le filtre optimal. Cependant entre 20 et 30 MHz le filtre de référence présente de meilleures performances. Ceci prouve que le critère des émissions EM devra être amélioré. La gamme de fréquences supérieures à 30 MHz n'est pas considérée dans l'optimisation.

F.4.5 Validation expérimentale

Le filtre optimal a été construit puis évalué par la mesure. Dans un premier temps, la méthode de modélisation a été modélisée une nouvelle fois. Les simulations ont été comparées aux mesures des spectres des tensions de sortie et des courants d'entrée. Les comparaisons des enveloppes des spectres du courant d'entrée et de la tension de sortie sont montrées dans les figures F.28 et F.29. Ces figures montrent que la simulation et la mesure se se superposent sur toute la bande des fréquences considérées, sauf pour les plages pour lesquelles le niveau du spectre est inférieur à celui du bruit de mesure.

Après avoir démontré que la méthode de modélisation est convenable pour cette optimisation, la figure F.30 compare les enveloppes des spectres de tension de sortie

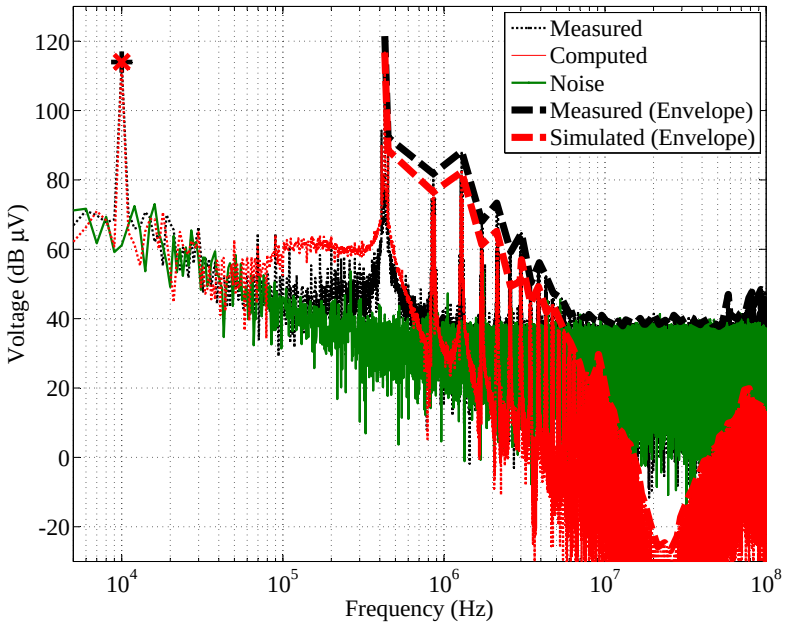


FIGURE F.28: Tensions de sortie du filtre.

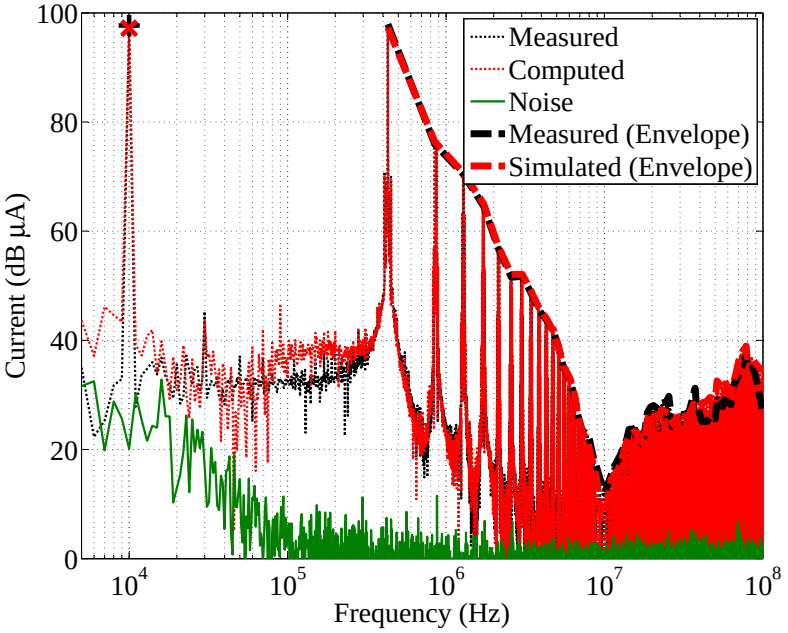


FIGURE F.29: Courant d'entrée du filtre.

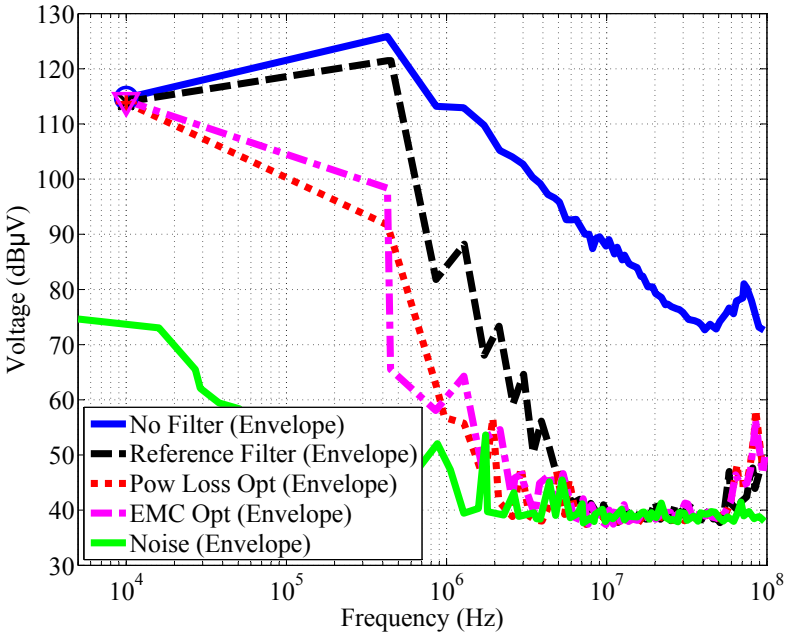


FIGURE F.30: Enveloppes des spectres de sorties des différents filtres

du filtre. Ici, on peut voir que le filtre optimisé a permis de réduire significativement les émissions jusqu'à 7 MHz. Au-dessus de cette fréquence, la comparaison n'est encore une fois pas possible à cause de niveau de bruit de mesure.

La figure F.31 montre une comparaison des performances énergétiques obtenues avec différents filtres. Cette figure montre, pour différents filtres, les pertes relatives par rapport au cas où aucun filtre n'est utilisé. On peut déduire de ces résultats que le filtre de référence génère 5 plus de pertes que le filtre optimal. Cela montre que le critère de calcul de puissance est bien formulé et que l'optimisation est efficace pour optimiser le filtre CEM.

F.5 Impact du filtre de CEM sur le signal audio de l'amplificateur

En ajoutant un filtre de CEM à la sortie d'un amplificateur de Classe D, on empêche les perturbations EM de se propager pour perturber les systèmes à proximité. Cependant, ce filtre ajouté sur le chemin de propagation du signal audio est souvent composé d'éléments de filtrages non-linéaires que sont les composants magnétiques. Ces non-linéarités modifient la forme du signal audio et créent des distorsions harmoniques dans la bande audio (un exemple est donné dans

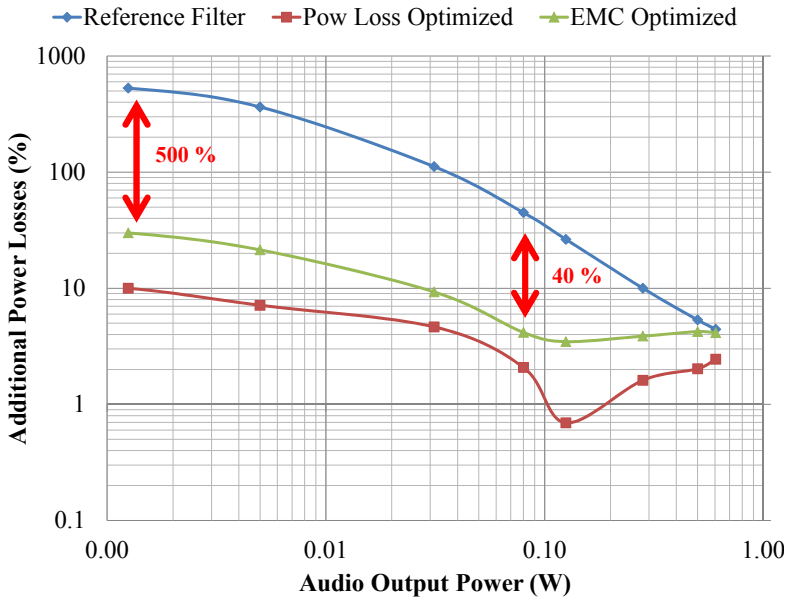


FIGURE F.31: Pertes introduites par différents filtres.

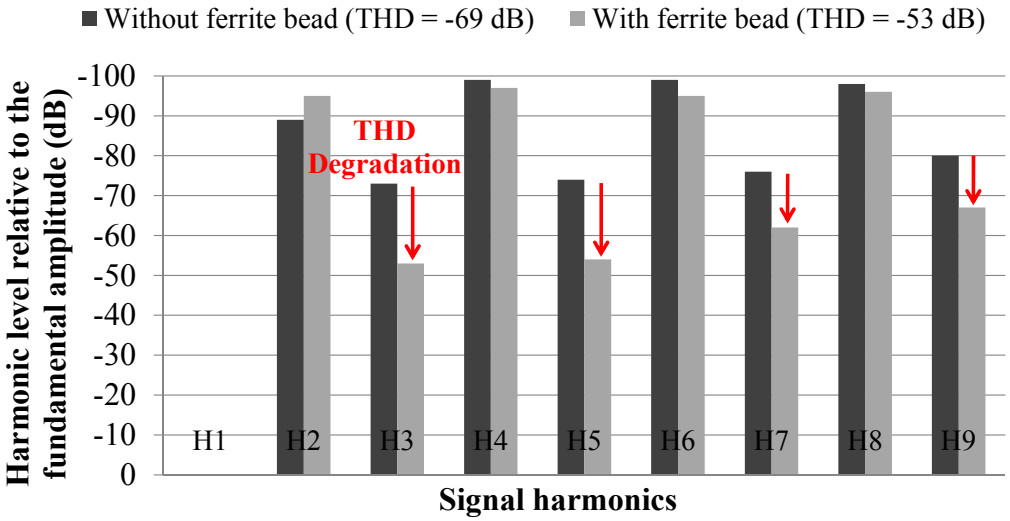


FIGURE F.32: Exemple de mesure du bargraph et du taux de distorsion harmonique (THD) d'un amplificateur de Classe D avec et sans perles de ferrites.

la figure F.32). Dans le cas des téléphones portables, en général les composants magnétiques choisis sont des perles de ferrites car l'allure de leur impédance en fonction de la fréquence présente des caractéristiques intéressantes [124, 125]. Dans cette partie, on s'intéresse à modéliser ces composants et évaluer leurs impacts sur le signal audio. Ce travail étudie particulièrement les perles de ferrites mais il est possible d'appliquer cela sur les inductances qui incluent un cœur magnétique.

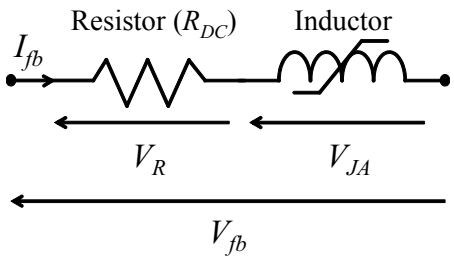


FIGURE F.33: Modèle d'une ferrite dans la bande audio.

F.5.1 Modélisation d'une perle de ferrite

Une perle de ferrite peut être modélisée dans la bande audio par le modèle donné dans la figure F.33. Le modèle est composé par la résistance DC et d'une inductance qui modélise le bobinage, le matériau magnétique utilisé dans le composant et son architecture physique. La tension aux bornes de ce dipôle est donnée par l'équation (F.9) où V_{JA} est donnée par l'équation (F.10) et I_{fb} est donné par l'équation (F.11).

$$v_{fb}(t) = v_{JA}(t) + R_{DC} \cdot i_{fb}(t) \tag{F.9}$$

$$v_{JA}(t) = N \cdot S \cdot \frac{\mathrm{d}B(t)}{\mathrm{d}t} \tag{F.10}$$

$$i_{fb}(t) = \frac{L}{N} \cdot H(t) \tag{F.11}$$

Où B est l'induction magnétique, H est le champ magnétique, N est le nombre de spires, S est la surface effective du circuit magnétique et L la longueur effective du composant.

La relation entre B et H est donnée par le modèle du matériau magnétique. Ici, elle a été modélisée par le modèle de Jiles-Atherton (JA). Dans ce modèle un matériau magnétique est caractérisé par 5 paramètres. Ce modèle permet de modéliser le phénomène d'hystérésis du matériau magnétique ainsi que sa saturation.

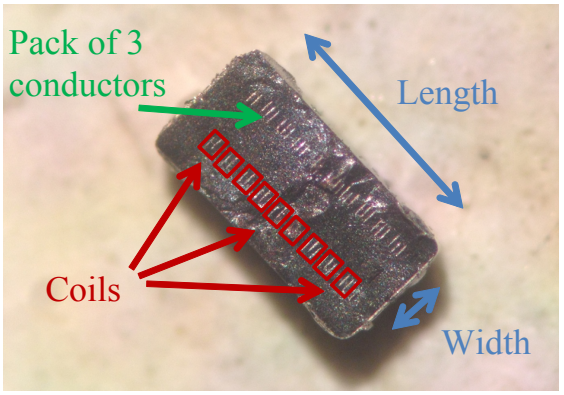


FIGURE F.34: Perle de ferrite casée en deux.

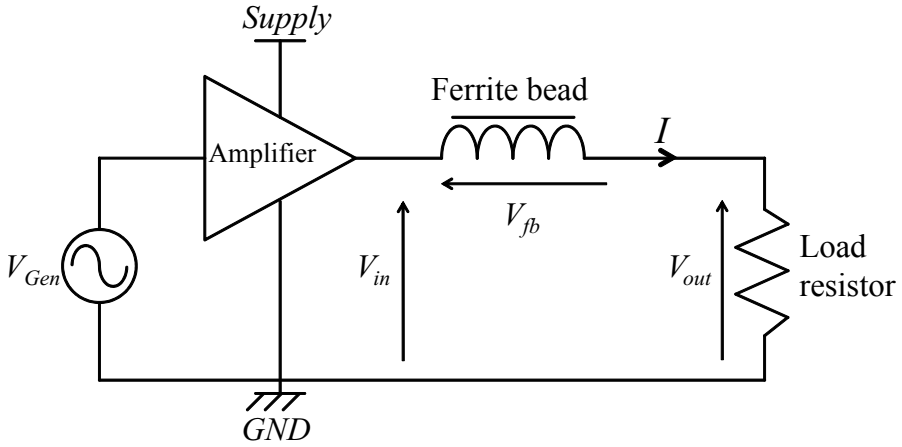


FIGURE F.35: Circuit de validation.

F.5.2 Application expérimentale

Ce modèle est utilisé pour modéliser une perle de ferrite pour validation. Pour cela, les paramètres suivants doivent être connus : R_{DC}, N, L, S et les 5 paramètres du modèle de JA. R_{DC} a été mesurée par un analyseur d'impédance. Les paramètres N, L et S ont été déterminés en cassant un composant et en le regardant dans un microscope comme montré dans la figure F.34. Finalement les paramètres du modèle JA ont été trouvés dans la littérature pour un matériau de type ferrite pour s'approcher au mieux du matériau utilisé dans ce composant.

La perle de ferrite modélisée est placée dans le circuit montré dans la figure F.35 et alimentée par un amplificateur linéaire pour éliminer le contenu fréquentiel en haute fréquence d'un amplificateur de Classe D et donc se focaliser sur la bande audio. Le circuit considéré a été simulé et mesuré pour évaluer les performances du modèle établi. Dans le domaine temporel, les tensions simulées et mesurées

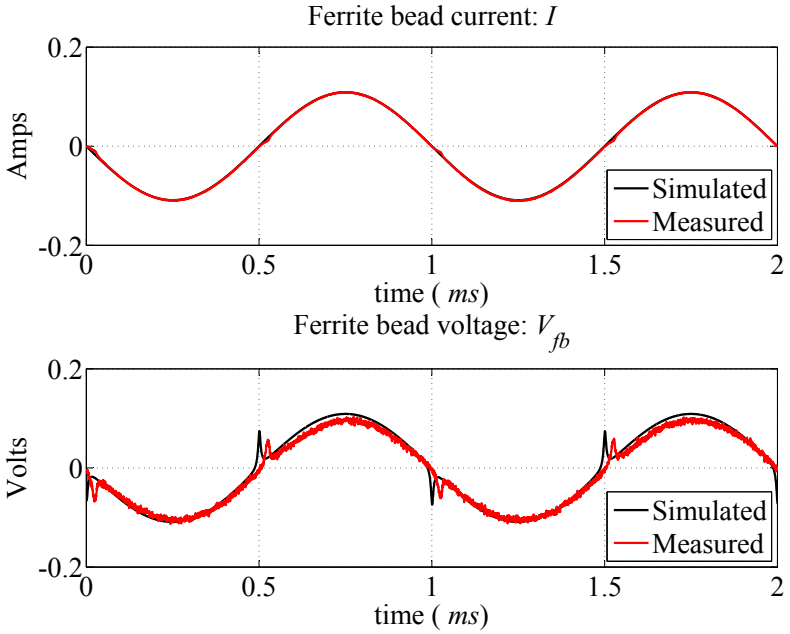


FIGURE F.36: Courant et tension de la ferrite.

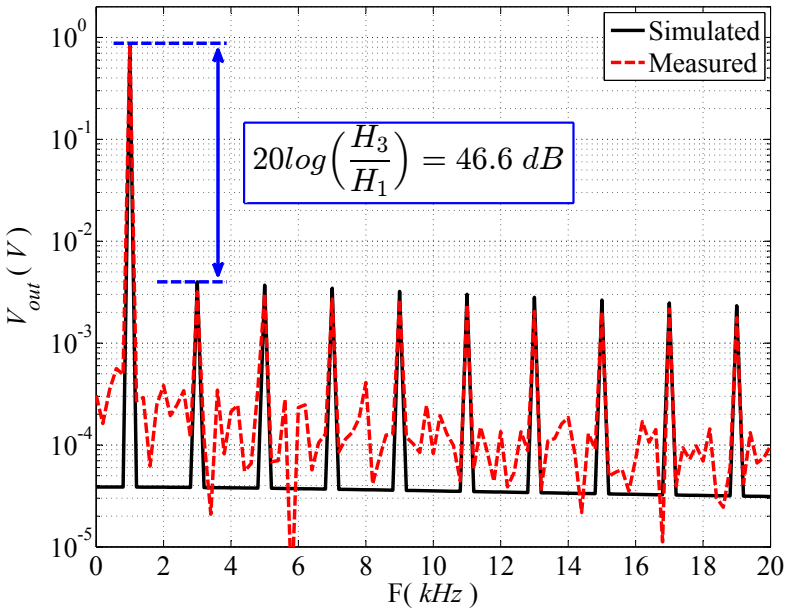


FIGURE F.37: Tension à la charge.

aux bornes de la ferrite concordent (figure F.36). La non-linéarité du matériau magnétique se traduit par des pics de tensions qui apparaissent à chaque passage à zéro du signal d'origine qui est une sinusoïde à 1 kHz. Dans le domaine fréquentiel, les tensions mesurées et simulées à la charge sont comparées. Les résultats obtenus sont satisfaisants (figure F.37). On peut voir qu'il y a une augmentation des harmoniques impaires ce qui crée une augmentation du THD.

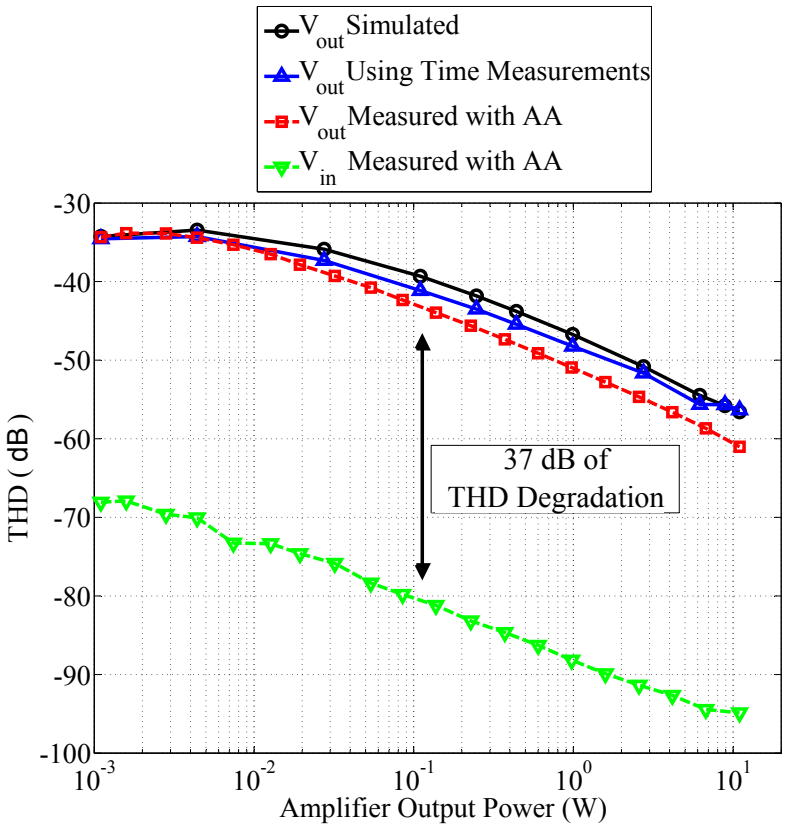


FIGURE F.38: THD à la sortie de l'amplificateur et à la charge.

Finalement, des tests ont été menés avec différents niveaux de tension de l'amplificateur linéaire entre 100 mV et 10 V. La tension aux bornes de la charge a été simulée. Ceci a permis de calculer le THD pour chaque amplitude. La courbe de THD obtenue a été comparée à la mesure de THD faite à l'aide d'un analyseur audio (figure F.38). On peut tirer deux conclusions de cette figure. Premièrement, le THD mesuré et simulé sont en bonne concordance pour les différents niveaux de tensions ce qui permet de valider le modèle sur une large plage de tension. Deuxièmement, le THD obtenu après la ferrite (à la charge) est beaucoup plus élevé que celui obtenu avant la ferrite (à la sortie de l'amplificateur) ce qui montre que la ferrite étudiée peut réduire significativement la qualité du signal d'un amplificateur audio qui se traduit dans ce cas par une détérioration de 37 dB du THD.

F.6 Conclusion

Les amplificateurs à découpage, nommés aussi amplificateurs de Classe D, sont particulièrement intéressants grâce à leur rendement énergétique élevé. Cependant leur fort niveau d'émissions électromagnétiques les rend critiques dans les applications finales à cause des normes sévères de CEM. Malgré tous les efforts pour réduire leurs émissions, le filtre CEM reste la solution la plus utilisée. Les filtres CEM sont difficiles à concevoir parce qu'ils sont fortement impactés par les éléments parasites. Pour cela leur conception est souvent faite par des mesures répétitives. Cela n'est pas optimal. En conséquence, ce travail de recherche a été focalisé sur le développement des outils qui peuvent être utilisés pour la conception des filtres CEM à des phases précoces du développement. Le travail a donc été divisé en trois grandes parties. La première est le développement d'un modèle de CEM pour étudier la CEM des amplificateurs de Classe D. La deuxième est l'utilisation du modèle développé dans une boucle d'optimisation pour améliorer le comportement des filtres. La dernière est consacrée à la dégradation de la qualité audio causée par le filtre CEM.

Annexe G

List of Publications

- R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, P. Lombard, and A. Nagari,"N-conductor passive circuit modeling for power converter current prediction and EMI aspect," Electromagnetic Compatibility, IEEE Transactions on, vol. 55, no. 6, pp. 1169-1177, Dec 2013.

- R. Mrad, M. Ferber, F. Morel, G. Pillonnet, C. Vollaire, J. Vasconcelos, and A. Nagari,"Discrete optimization and frequency domain macromodeling used for EMI filter design," Electromagnetic Compatibility, IEEE Transactions on, 2014 (submitted).

- R. Mrad, G. Pillonnet, F. Morel, C. Vollaire, and A. Nagari,"Predicting the impact of magnetic components used for EMI suppression on the base-band of a power amplifier," Electromagnetic Compatibility, IEEE Transactions on, 2014 (submitted).

- R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, and D. Labrousse,"Differential passive circuit modelling with pentapole impedance matrices - application to an integrated audio switching amplifier for portable devices," in EMC Europe 2011 York, Sept 2011, pp. 304-309.

- R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, and A. Nagari, "Conducted EMI prediction for integrated class D audio amplifier," in Electronics, Circuits and Systems (ICECS), 2011 18^{th} Workshop on, Nov 2011, pp. 142-147.

- R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, P. Lombard, and A. Nagari, "Approche de modélisation des chemins de propagation des perturbations

conduites pour des systèmes à deux conducteurs actifs," in Actes du 16ème Colloque International et Exposition sur la Compatibilité Électromagnétique, Rouen, France, Apr. 2012.

- R. Mrad, F. Morel, G. Pillonnet, C. Vollaire, and A. Nagari, "Integrated class-D audio amplifier virtual test for output EMI filter performance," in Ph.D. Research in Microelectronics and Electronics (PRIME), 2013 9th Conference on, June 2013, pp. 73-76.

- M. Tabbakh, F. Morel, R. Mrad, and Y. Zaatar, "High frequency battery impedance measurements for EMI prediction," in Electromagnetic Compatibility (EMC), 2013 IEEE International Symposium on, Aug 2013, pp. 763-767.

- K. El Haddad, R. Mrad, F. Morel, G. Pillonnet, and A. Nagari, "Ferrite bead effect on Class-D amplifier audio quality," in 17th IEEE Mediterranean Electrotechnical Conference, Apr. 2014 (in press).

- M. Ferber, R. Mrad, F. Morel, C. Vollaire, G. Pillonnet, A. Nagari, and J. ao A. Vasconcelos, "Discrete optimization of EMI filter using a genetic algorithm," in International Symposium on Electromagnetic Compatibility - Tokyo, June 2014 (in press).