

Réalisation, caractérisation et modélisation de nanofils pour application RF

Chuan-Lun Hsu

▶ **To cite this version:**

Chuan-Lun Hsu. Réalisation, caractérisation et modélisation de nanofils pour application RF. Autre. Université de Grenoble, 2013. Français. NNT : 2013GRENT046 . tel-00951398

HAL Id: tel-00951398
https://theses.hal.science/tel-00951398

Submitted on 24 Feb 2014

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Nano-Electronique et Nano-Technologies**

Arrêté ministériel : 7 août 2006

Présentée par

« Chuan-Lun HSU »

Thèse dirigée par **« Philippe BENECH »** et
codirigée par **« Gustavo ARDILA »**

préparée au sein du **Laboratoire IMEP-LAHC**
dans **l'École Doctorale EEATS Electronique, Electrotechnique, Automatique et Traitement du Signal**

Réalisation, Caractérisation et Modélisation de Nanofils pour Application RF

Thèse soutenue publiquement le **«21 Novembre 2013»**,
devant le jury composé de :

M. Bruno ALLARD
Professeur des universités, Lyon, Président
M. Laurent PICHON
Professeur des universités, Rennes, Rapporteur
Mme Valérie VIGNERAS
Professeur des universités, Bordeaux, Rapporteur
M. Philippe BENECH
Professeur des universités, Grenoble, Directeur de thèse
M. Gustavo ARDILA
Maître de conférences, Grenoble, Co-directeur de thèse

Resume

Les composants nano électroniques ont fait l'objet d'intérêt marqué, au sein de la communauté des concepteurs de circuits radiofréquence au cours de ces dernières années. Non seulement ils peuvent présenter des caractéristiques intéressantes, mais ils offrent la perspective d'améliorations de la miniaturisation des composants les plus avancés. Les nanotubes de carbone et les nanofils conducteurs sont attendus comme pouvant potentiellement constituer des blocs utilisables dans les futurs circuits aux très faibles dimensions. Les conducteurs métalliques sont utilisés depuis longtemps pour réaliser des composants passifs dans les circuits intégrés radio fréquence, cependant très peu de travaux ont été menés sur des conducteurs ayant des dimensions nanométriques et fonctionnant dans le domaine millimétrique. L'objectif de cette thèse est d'exploré les propriétés RF de conducteurs métalliques aux dimensions nanométriques et la possibilité de les intégrés dans des circuits utilisant des technologies CMOS.

Dans cette thèse, des lignes de transmission et des antennes intégrées sur puce, utilisant des nanofils conducteurs, ont été conçues et réalisées en utilisant un processus de fabrication "top-down". Les caractéristiques en terme de transmission de signal ont été observées expérimentalement dans le domaine millimétrique par la mesure de paramètres *S*. Deux types de lignes ont été conçus : des lignes micro-ruban de faible épaisseur et des lignes coplanaires. Les caractéristiques en fonction de la fréquence du signal d'excitation ont été analysées. Différents paramètres comme la largeur, l'épaisseur, le nombre de nanofils et la distance entre les nanofils ont été étudiés. De plus, un modèle de propagation basée sur des ondes quasi-TEM a été proposé pour obtenir une compréhension fine du comportement physique des nanofils. Par ailleurs, une étude approfondies concernant les techniques d'épluchage (de-embedding) a été menée afin d'améliorer la précision des mesures. En parallèle, des antennes dipôle et IFA, utilisant des nanofils, ont été réalisées pour tester la transmission sans ligne de propagation. Différentes dimensions de conducteurs et différents types de substrats ont été utilisés pour étudier leurs propriétés et obtenir les meilleures performances.

Abstract

Nano-electronic devices have attracted much attention for the radio frequency engineering community in recent years. They not only exhibit compelling characteristics but show promises to enhance the miniaturization of modern devices. Carbon nanotubes and conducting nanowires are believed to be potential building blocks for ultra-small chip of the future. Metallic wires have long been utilized as the passive components in the RF integrated circuit but there are very few studies on their nanoscale counterpart particularly up to millimeter-wave frequencies. The focus of this thesis is to explore RF properties of metallic nanowires and their potentials to be integrated in CMOS communication technology.

In this thesis, transmission lines and on-chip antennas integrated with metallic nanowires were developed enabled by top-down fabrication processes. The signal transmission properties of such devices were characterized well into the mm-wave regime based on two-port *S*-parameters measurement. Two types of nano-transmission lines were designed: thin film microstrip lines and coplanar waveguides. Their transmission characteristics as a function of frequencies were analysed. Different parameters like the linewidth, thickness, number of nanowires, and the distance between the wires were examined. In addition, a quasi-TEM propagation model was proposed to provide a further insight into the physical behaviours of the nanowires. Moreover, a comprehensive study regarding the de-embedding techniques was carried out in order to improve measurement accuracy. Meanwhile, on-chip dipoles and planar meander-line inverted–F antenna were implemented to test the wireless signal transmission of the metallic nanowires. Various wires dimensions and substrates were designed to exploit their characteristics thus facilitating better transmission.

Acknowledgment

I would like to express my appreciation to Prof. Philippe Benech for his invaluable guidance over the last three years, which was very important in strengthening my knowledge in electromagnetic theory and RF device characterization. I also wish to thank Dr. Gustavo Ardila for his many suggestions and insight. It would not have been possible to realize all these test devices without him. Next, I heartily thank Mr. Nicolas Corrao and Mr. Jean-Luc Thomassin for their timely technical assistance which was essential to the completion of this thesis work. Special thanks to the technical staffs of PTA in CEA-Leti for their supports on the cleanroom equipment. I am also grateful to the external collaborators: the laboratory of IMEL in Demokritos for having fabricated the dipole antennas on porous Si substrates and VTT Technical Research Centre of Finland for having measured the nanodevices from 140 up to 210 GHz. I also extend my appreciation to all the colleagues and members at the laboratory of IMEP-LAHC for the good humour and a nice working environment. And last but not least, I would like to thank the members of the jury: Prof. Bruno Allard, Prof. Laurent Pichon and Prof. Valérie Vigneras for their encouragement, comments and questions.

This research has received funding from the European Community's Seventh Framework Programme (FP7/2007-2013) under grant agreement NANOFUNCTION n°257375.

Table of Contents

Resume ..... **i**
Abstract ..... **ii**
Acknowledgment ..... **iii**
Table of Contents ..... **iv**
List of Tables ..... **vii**
List of Figures ..... **viii**

1 Introduction **1**

1.1 Overview of Nano-electronics in Radio-Frequency Technology 1
1.1.1 Nano-transmission Lines 2
1.1.2 Nano-antenna 4
1.1.3 High-Frequency Characterization 6
1.2 Motivation 9
1.3 Objective 10
1.4 Scope of This Work 10
1.5 Outline 11

2 Parameters Extraction of Submicron Thin Film Microstrip Lines **13**

2.1 Test Structure Fabrication 13
2.2 Scattering Parameter Measurement 15
2.2.1 *S*-parameters Basics 15
2.2.2 Measurement Setup 16
2.2.3 De-embedding Procedure 17
2.2.4 Preliminary Results 18
2.3 Modelling 19
2.3.1 Implementation of a Lumped Circuit Model 19
2.3.2 ADS Momentum Simulation 20
2.3.3 Theoretical and Experimental Comparison 21
2.3.4 Full Circuit Model 23
2.4 Results and Discussion 23
2.4.1 Extraction of Transmission Line Parameters 24
2.4.2 Preliminary Validation 24
2.4.3 The Impact of Pad Residual Capacitance 25

2.5 Conclusion..... 27

3 Characterization of Metallic Nanoscale Transmission Lines up to mm-wave Frequencies..... 29

3.1 Single Aluminium Nano-lines..... 29

3.1.1 Test structure Fabrication..... 30
3.1.2 Scattering Parameters Measurement..... 31
3.1.3 Simulation Based on Quasi-TEM Model..... 32
3.1.4 Parasitics Subtraction..... 34
3.1.5 Results and Discussion..... 37
3.1.6 Alternative Extraction of Parasitics..... 46

3.2 Single and Multiple Gold Nano-lines..... 50

3.2.1 New Test Structure Design and Fabrication..... 50
3.2.2 Scattering Parameters Measurement..... 51
3.2.3 DC Resistance Measurement..... 52
3.2.4 Verification of the New Subtraction Method..... 53
3.2.5 Results and Discussion..... 54

3.3 140-210 GHz Characterization..... 69
3.4 Conclusion..... 70

4 Nanocale On-chip Integrated Millimeter Wave Antennas on Various Substrates..... 73

4.1 Past Work in On-chip Integrated Antennas for Millimeter Wave Applications..... 74
4.2 Design of the Test Structures..... 75

4.2.1 On-Chip Dipole Antennas Integrated on Standard Silicon and Porous-Silicon Substrate (Test set No.1)..... 75
4.2.2 On-Chip Dipole Antennas Integrated on High-Resistivity Silicon Substrate (Test set No.2)..... 76
4.2.3 On-Chip Planar Inverted-F Antennas Integrated on High-Resistivity Silicon Substrate (Test set No.3)..... 77

4.3 Fabrication and Characterization..... 78

4.3.1 Test Structure Fabrication..... 78
4.3.2 On-chip Antenna Characteristics..... 80
4.3.3 Characterization Method..... 82

4.4 Results and Discussion..... 82

4.4.1 Test set No.1: Dipole Antennas Integrated on Porous-Silicon and Standard Silicon Substrate..... 83
4.4.2 Test set No.2: Dipole Antennas Integrated on Oxide-Isolated High-Resistivity Silicon Substrate..... 86
4.4.3 Test set No.3: PIFA Integrated on Oxide-Isolated High-Resistivity Silicon Substrate..... 88

4.5 Conclusion..... 90

5 Conclusion 93

5.1 Metallic Nano-Transmission Line Characteristics 93
5.2 On-chip Nano Antenna Characteristics 94
5.3 Validity of the Model 95
5.4 Accuracy of the Measurement and Extraction..... 96
5.5 Possible Future Work 97

Appendix A: Antenna Basics 99

A1. Basic Parameters 99
A2. Dipole Antenna 100
A3. Inverted-F Antenna..... 100

References 101

List of Tables

Table 3.1 Geometric parameters of the lines in CPW configuration..... 30
Table 3.2 Discrepancy between simulation results and measurements for sample No.2. 41
Table 3.3 Geometric parameters of the gold lines in CPW configuration..... 51
Table 3.4 Discrepancy between simulation and measurements for sample Nos. A1, B1 and C1 using L2-L3 dataset. 61

Table 4.1 Geometric parameters of the on-chip dipole antennas (Test set No.1)..... 76
Table 4.2 Geometric parameters of the on-chip dipole antennas (Test set No.2)..... 77
Table 4.3 Geometric parameters of the on-chip inverted-F antennas (Test set No.3)..... 78
Table 4.4 Summary of the experimental result from Test set No.1..... 85
Table 4.5 Summary of the experimental result from Test set No.2..... 86
Table 4.6 Summary of the experimental result from Test set No.3..... 90

List of Figures

Figure 1.1 Conventional transmission line model [25] 3
Figure 1.2 Equivalent circuit model for a carbon nanotube [25]..... 3
Figure 1.3 Cu resistivity as a function of linewidth, taking into account the grain boundary and interface electron scattering [30] 4
Figure 1.4 Cross-sectional scanning electron micrograph showing typical CMOS 7S interconnections with tungsten local interconnections and six levels of copper wiring [42]. ... 5
Figure 1.5 Generic view of 1) left side: microstrip line 2) right side: coplanar waveguide. They are potential platforms for characterizing nanowires, in which the central conductor can be replaced by the intened test sample. 6
Figure 1.6 Generic view of a coplanar waveguide integrated with a nanowire. The tapered design RF signal pads can be seen. 7
Figure 1.7 Equivalent circuit model of a test platform with a CNT.. 8
Figure 1.8 Estimated contact resitance and conductivity of Pt NWs [61]..... 9

Figure 2.1 Fabrication steps of the TFML structure..... 14
Figure 2.2 Photo of a fabricated 200 µm-long TFML and pads..... 15
Figure 2.3 Close look at the transition between the line and the pad.. 15
Figure 2.4 A two-port network [63]. 15
Figure 2.5 The standards used in the calibration. 17
Figure 2.6 Schematic explanation of the effect of de-embedding. 17
Figure 2.7 De-embedding structures for the TFML. The left photo shows a open device and the right one is a short device 17
Figure 2.8 Comparison of the magnitiude of S_{11} before and after de-embedding 19
Figure 2.9 Comparison of the magnitiude of S_{21} before and after de-embedding 19
Figure 2.10 Ilustration of the equivalent circuit model in a TFML structure..... 20
Figure 2.11 ADS Momontum user interface showing the simulation setup for TFML 21
Figure 2.12 Substrate defination interface in Momentum 21
Figure 2.13 Resistance per unit length vs frequency..... 22
Figure 2.14 Inducance per unit length vs frequency 22

Figure 2.15 Capacitance per unit length vs frequency 22
Figure 2.16 Circuit model of the complete test strucutre, line and the pads 23
Figure 2.17 Real part of *Zc* for the measured and simulated TFMLs..... 24
Figure 2.18 Imaginary part of *Zc* for the measured and simulated TFMLs 24
Figure 2.19 Attentuation for the measured and simulated TFMLs 24
Figure 2.20 Phase constant for the measured and simulated TFMLs..... 24
Figure 2.21 Real (left) and imaginary part (right) of *Zc* for the measured and simulated 200 µm-long TFML 25
Figure 2.22 Attenuation (left) and phase constant (right) for the measured and simulated 200 µm-long TFML 25
Figure 2.23 Experimental and simulated S_{11} of l = 200 µm 25
Figure 2.24 Experimental and simulated S_{21} of l = 200 µm 25
Figure 2.25 Experimental and simulated S_{11} of l = 500 µm 26
Figure 2.26 Experimental and simulated S_{21} of l = 500 µm 26
Figure 2.27 Variation of real part of *Z*c as a result of capacitive parasitic residue 26
Figure 2.28 Variation of imaginary part of *Z*c as a result of capacitive parasitic residue 26
Figure 2.29 Variation of attentuation as a result of capacitive parasitic residue..... 27
Figure 2.30 Variation of phase constant as a result of capacitive parasitic residue 27

Figure 3.1 SEM image of a nano-size Al wire embedded in a CPW structure 30
Figure 3.2 Contact between the nano-size wire and the pad 31
Figure 3.3 Top view of the Al wire 31
Figure 3.4 Thru de-embedding test structure..... 31
Figure 3.5 Complete test device with GSG probes 32
Figure 3.6 Equivalent quasi-TEM circuit model for the intrinsic CPW device 32
Figure 3.7 ADS Momentum interface showing the simulation setup of a CPW structure..... 33
Figure 3.8 Two port network of the thru de-embedding test structure..... 34
Figure 3.9 Circuit model of the CPW devices at low frequencies..... 35
Figure 3.10 Measured and simulated impedance of the CPW devices with l = 17 µm at low frequencies..... 35
Figure 3.11 Parasitic circuit model of the CPW device 36
Figure 3.12 Comparison of S_{11} for sample No.2, l = 192 µm..... 37
Figure 3.13 Comparison of S_{21} for sample No.2, l = 192 µm..... 37
Figure 3.14 De-embedded S_{11} magnitude from sample No.3..... 38
Figure 3.15 De-embedded S_{11} phase from sample No.3..... 38
Figure 3.16 De-embedded S_{21} magnitude from sample No.3..... 38
Figure 3.17 De-embedded S_{21} phase from sample No.3..... 38

Figure 3.18 Comparison of S_{11} for sample No.1, l = 192 µm..... 39
Figure 3.19 Comparison of S_{21} for sample No.1, l = 192 µm..... 39
Figure 3.20 Comparison of S_{11} for sample No.2, l = 192 µm..... 39
Figure 3.21 Comparison of S_{21} for sample No.2, l = 192 µm..... 39
Figure 3.22 Comparison of S_{11} for sample No.3, l = 192 µm..... 39
Figure 3.23 Comparison of S_{21} for sample No.3, l = 192 µm..... 39
Figure 3.24 Measured and simulated *Zc* of sample No.4 40
Figure 3.25 Measured and simulated γ of sample No.4..... 40
Figure 3.26 Measured and simulated *Zc* of sample No.1 41
Figure 3.27 Measured and simulated γ of sample No.1..... 41
Figure 3.28 Measured and simulated *Zc* of sample No.2 41
Figure 3.29 Measured and simulated γ of sample No.2..... 41
Figure 3.30 Measured and simulated *Zc* of sample No.3 42
Figure 3.31 Measured and simulated γ of sample No.3..... 42
Figure 3.32 Measured and simulated *Zc* of sample No.2 with l = 192 µm. Case 1: left contact contributes to 25% of the total contact impedance. Case 2: left contact contributes to 75% of the total contact impedance 43
Figure 3.33 Measured and simulated γ of sample No.2 with l = 192 µm. Case 1: left contact contributes to 25% of the total contact impedance. Case 2: left contact contributes to 75% of the total contact impedance. 43
Figure 3.34 Open de-embedding test structure (empty device)..... 43
Figure 3.35 Extracted coupling impedance from the open devices. L4 open: open device with l= 492 µm. L3 open: open device with l= 192 µm. L2 open: open device with l= 92 µm..... 44
Figure 3.36 Circuit model of the coupling impedance *Zco* 44
Figure 3.37 Extracted and simulated Re(*Zc*) of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling. 45
Figure 3.38 Extracted and simulated Im(*Zc*) of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling. 45
Figure 3.39 Extracted and simulated α of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling. 45

Figure 3.40 Extracted and simulated β of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling 45
Figure 3.41 Contact resistance estimated from the two line method and the circuit model for sample No.1; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm 47
Figure 3.42 Contact reactance estimated from the two line method and the circuit model for sample No.1; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm 47
Figure 3.43 Contact resistance estimated from the two line method and the circuit model for sample No.2; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm 48
Figure 3.44 Contact reactance estimated from the two line method and the circuit model for sample No.2; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm 48
Figure 3.45 Comparison between S_{11} raw data and reconstructed from the two line method using the contact impedance extracted L3-L4 and L2-L3 as well as the directly obtained from circuit model 48
Figure 3.46 Comparison between S_{21} raw data and reconstructed from the two line method using the contact impedance extracted L3-L4 and L2-L3 as well as the directly obtained from circuit model 48
Figure 3.47 Measured and simulated *Zc* of sample No.4 49
Figure 3.48 Measured and simulated γ of sample No.4 49
Figure 3.49 Measured and simulated *Zc* of sample No.1 49
Figure 3.50 Measured and simulated γ of sample No.1 49
Figure 3.51 Measured and simulated *Zc* of sample No.2 49
Figure 3.52 Measured and simulated γ of sample No.2 49
Figure 3.53 SEM image of two parallel nano Au wires embedded in a CPW structure 50
Figure 3.54 Contact between the nano-size wires and the pad 51
Figure 3.55 Top view of an Au wire 51
Figure 3.56 Complete test device with 50 µm pitch GSG probes 52
Figure 3.57 The test device with the probes at lower magnification 52
Figure 3.58 Total DC resistance of three different sample types. 52
Figure 3.59 Extracted contact impedance using the two line method 53
Figure 3.60 Circuit model of a Au nano-transmission line with contact impedance 53
Figure 3.61 Measured and simulated *Zc* of sample No.F1 54
Figure 3.62 Measured and simulated γ of sample No.F1 54
Figure 3.63 Measured and simulated *R* and *L* of sample No.F1 55
Figure 3.64 Measured and simulated *G* and *C* of sample No.F1 55
Figure 3.65 Extracted contact impedance Z_L 55

Figure 3.66 Measured and simulated *Zc* of sample No.C1 with different pad designs 55
Figure 3.67 Measured and simulated γ of sample No.C1 with different pad designs 55
Figure 3.68 Measured and simulated *R* and *L* of sample No.C1 with different pad designs... 56
Figure 3.69 Measured and simulated *G* and *C* of sample No.C1 with different pad designs.. 56
Figure 3.70 Coupling impedance between 50 µm pitch signal pads at different distances. L4 open: open device with l = 492 µm. L3 open: open device with l = 192 µm. L2 open: open device with l = 92 µm. 56
Figure 3.71 Measured and simulated *Zc* of sample No.B1 with and without removal of coupling effect 57
Figure 3.72 Measured and simulated γ of sample No.B1 with and without removal of coupling effect 57
Figure 3.73 Measured and simulated *R* and *L* of sample No.B1 with and without removal of coupling effect 57
Figure 3.74 Measured and simulated *G* and *C* of sample No.B1 with and without removal of coupling effect 57
Figure 3.75 Measured Re(*Zc*) of sample Nos.B1, B2[a] and B5[a] (from top to bottom). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included. 58
Figure 3.76 Measured Im(*Zc*) of sample Nos.B1, B2[a] and B5[a] (from bottom to top). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included. 58
Figure 3.77 Measured α of sample Nos.B1, B2[a] and B5[a] (from top to bottom). 58
Figure 3.78 Measured β of sample Nos.B1, B2[a] and B5[a] (from top to bottom). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included. 58
Figure 3.79 Measured *R* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included. 59
Figure 3.80 Measured *L* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included. 59
Figure 3.81 Measured *C* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included. 59
Figure 3.82 Measured *G* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included. 59
Figure 3.83 Measured Re(*Zc*) of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included 60
Figure 3.84 Measured Im(*Zc*) of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included 60

Figure 3.85 Measured α of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included. 60
Figure 3.86 Measured β of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included. 60
Figure 3.87 Measured *R* of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included. 60
Figure 3.88 Measured *Zc* of sample Nos.B1 and B1'. Sample No.B1: single line, linewidth= 200 nm, gap distance = 20 µm. Sample No.B1' and Sample No.B1', repeat: single line, linewidth= 200 nm, gap distance = 12 µm 61
Figure 3.89 Measured γ of sample Nos.B1 and B1'. Sample No.B1: single line, linewidth= 200 nm, gap distance = 20 µm. Sample No.B1' and Sample No.B1', repeat: single line, linewidth= 200 nm, gap distance = 12 µm 61
Figure 3.90 Measured *Zc* of sample Nos.A2[a] and A2'[a]. Sample No.A2[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 20 µm. Sample No.A2'[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 12 µm. 62
Figure 3.91 Measured γ of sample Nos.A2[a] and A2'[a]. Sample No.A2[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 20 µm. Sample No.A2'[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 12 µm. 62
Figure 3.92 Measured Re(*Zc*) of sample Nos.B2[a], B2[b], B2[a] and B5[b] 63
Figure 3.93 Measured Im(*Zc*) of sample Nos.B2[a], B2[b], B2[a] and B5[b] 63
Figure 3.94 Measured α of sample Nos.B2[a], B2[b], B2[a] and B5[b] 63
Figure 3.95 Measured β of sample Nos.B2[a], B2[b], B2[a] and B5[b] 63
Figure 3.96 Measured *R* of sample Nos.B2[a], B2[b], B2[a] and B5[b] 63
Figure 3.97 Measured *L* of sample Nos.B2[a], B2[b], B2[a] and B5[b] 63
Figure 3.98 Measured *C* of sample Nos.B2[a], B2[b], B2[a] and B5[b] 64
Figure 3.99 Measured *G* of sample Nos.B2[a], B2[b], B2[a] and B5[b] 64
Figure 3.100 Measured Re(*Zc*) of sample Nos.A2[a], A2[b], A2[a] and A5[b] 64
Figure 3.101 Measured Im(*Zc*) of sample Nos.A2[a], A2[b], A2[a] and A5[b] 64
Figure 3.102 Measured α of sample Nos.A2[a], A2[b], A2[a] and A5[b] 64
Figure 3.103 Measured β of sample Nos.A2[a], A2[b], A2[a] and A5[b] 64
Figure 3.104 Measured *C* of sample Nos.A2[a], A2[b], A2[a] and A5[b] 65
Figure 3.105 Magnitude of S_{21} for sample No.C1 66
Figure 3.106 Magnitude of S_{21} for sample No.B1 66
Figure 3.107 Magnitude of S_{21} for sample No.A1 66
Figure 3.108 Magnitude of S_{21} from the empty open structures and when probes are in the air. L4 open: open device with l = 492 µm. L3 open: open device with l = 192 µm. L2 open: open device with l = 92 µm. 66

Figure 3.109 Comparison of de-embedded *Zc* for sample No.B1 67
Figure 3.110 Comparison of de-embedded γ for sample No.B1 67
Figure 3.111 Comparison of de-embedded *Zc* for sample No.A1 67
Figure 3.112 Comparison of de-embedded γ for sample No.A1 67
Figure 3.113 Comparison of de-embedded *Zc* for sample No.A2^{b} 68
Figure 3.114 Comparison of de-embedded γ for sample No.A2^{b} 68
Figure 3.115 Comparison of *Zc* between different sample types. Dotted lines are the corresponding simulated results. 69
Figure 3.116 Comparison of γ between different sample types. Dotted lines are the corresponding simulated results. 69
Figure 3.117 Comparison of *Zc* between different sample types 69
Figure 3.118 Comparison of γ between different sample types..... 69
Figure 3.119 Experimental *Zc* of sample No.2 up to 210 GHz 70
Figure 3.120 Experimental γ of sample No.2 up to 210 GHz 70

Figure 4.1 Geometry of an on-chip dipole antenna on top of the dielectric layer (blue) and silicon substrate (grey) 76
Figure 4.2 Schematic of a dipole pair facing each other at a distance *R* 76
Figure 4.3 Geometry of an asymmetric on-chip dipole antenna on top of the dielectric layer and silicon substrate 77
Figure 4.4 The layout of an inverted-F antenna with ground planes on top of the dielectric layer and silicon substrate 78
Figure 4.5 Photo of a dipole pair with pads integrated on oxide-coated high-R Si wafer..... 79
Figure 4.6 Photo of a single dipole with pads integrated on oxide-coated high-R Si wafer ... 79
Figure 4.7 Photo of an asymmetric dipole with pads (sample No.2C)..... 80
Figure 4.8 Photo of a PIFA pair with pads integrated on oxide-coated high-R Si wafer 80
Figure 4.9 Photo of a single PIFA with pads integrated on oxide-coated high-R Si wafer..... 80
Figure 4.10 SEM image showing the connection between the pads and the antennas..... 80
Figure 4.11 Experimental *S*-parameters of the dipoles on the porous silicon substrate. S_{11} is situated at upper level while S_{21} is at the lower level. Open represents the open device. 84
Figure 4.12 Experimental *S*-parameters of the dipoles on the low-R silicon substrate. S_{11} is situated at upper level while S_{21} is at the lower level. Open represents the open device. 84
Figure 4.13 Measured and simulated *S*-paramters up to 210 GHz for sample Nos.1A and 1D on the porous silicon..... 85
Figure 4.14 The experimental phase of S_{21} up to 210 GHz for sample No.1A 85
Figure 4.15 Experimental *S*-parameters of the dipoles on high- resitivity silicon substrate ... 86
Figure 4.16 Experimental *S*-parameters of the dipoles on high- resitivity silicon substrate ... 86

Figure 4.17 The experimental phase of S_{21} up to 110 GHz for sample No.2A^2 87
Figure 4.18 Simulation setup of an dipole pair in ADS Momemtum..... 88
Figure 4.19 Measured and simulated S_{11} up to 210 GHz for sample Nos.2A^2 and 3A^1 88
Figure 4.20 Experimental *S*-parameters of sample Nos.4A^1, 4A^2 and 4A^3 on high resistivity silicon substrate 89
Figure 4.21 Experimental *S*-parameters of sample Nos.4B^1, 4B^2 and 4B^3 on high resitivity silicon substrate 89
Figure 4.22 Experimental *S*-parameters of sample Nos.4C^1, 4C^2 and 4C^3 on high resitivity silicon substrate 90
Figure 4.23 Experimental *S*-parameters of sample Nos.4D^1, 4D^2 and 4D^3 on high resitivity silicon substrate 90
Figure 4.24 The phase of S_{21} for sample Nos.4C^1 and 4C^2..... 90

Chapter 1

Introduction

1.1 Overview of Nano-electronics in Radio-Frequency Technology

The remarkable research progress in nanotechnology opens up new opportunities for designing novel electronic devices. The integration with nanoscale components not only enables the miniaturization of the device but increases the capabilities of electronic systems. The aim of nano-electronics is to take advantages of the properties of nanoscale matter that are distinctly different from macroscopic properties. Researches have been pursued worldwide to find nano-solutions in the fields of signal processing, energy harvesting, wireless communication and biomedical sensing just to name a few [1] [2].

In semiconductor electronics, the size of the transistor has a sustained exponential scaling into nanoscale dimension (known as Moore's law). The performance and the integration density were significantly improved over the last thirty years. According to the recent versions of ITRS Update, the pace of downsizing is less aggressive due to the economic crisis and physical barrier in technology. The logic CMOS will encounter eventually its shrinking limitation in 20-30 years [3]. The fundamental challenge is the risk of dielectric breakdown as the thickness of the silicon dioxide insulator is merely a few atomic layers [4]. The implementation of nanotechnology provides alternative technological solution for replacing current planer bulk CMOS. Nanowires (NWs) [5] [6] and carbon nanotubes (CNTs) [7] [8] are recognized as potential candidates to substitute the macroscopic silicon components in contemporary transistors. With such quasi-one-dimensional structures, a transistor can operate near the ballistic limit (no scattering along its length) thus achieving extremely high mobility. Recently, CNT field effect transistors (FET) with a sub-10 nm channel length have been demonstrated, having at least more than four times improvement in performance compared to state-of–the-art silicon circuits [9].

The advancement in nanoscale transistors has made it possible to turn the focus of research to high frequency electronic devices [10] [11]. The advantages found in nanotubes and nanowires such as high carrier mobility, high saturation velocity and high cut-off frequency are expected to be especially suitable for high frequency operation. The recent studies [12] [13] [14] on the use of CNT-based and silicon nanowire based field-effect transistors up to terahertz regime shed light on their analogue RF applications. As the size of the active devices approaches nano-metric dimension, to retain the circuit speed expected from miniaturization, the interconnect technology must be developed to be suitable for these new device concepts. It is natural to think of using nanotubes and nanowires themselves as high frequency interconnects in the integrated circuit. They may play an important role in the design of future micro and nano-electronics system for transmitting signal between components and connecting

devices. Above that, the concept of nano-antenna based on nanotubes and nanowires for wireless communication has been proposed to connect nano-electronic devices and the macroscopic world, making possible potentially high density circuitry in an advanced miniaturized system [15].

1.1.1 Nano-transmission Lines

Today, on-chip transmission lines for silicon monolithic integrated millimeter-wave (mm-wave) circuits are fabricated out of metals like copper and aluminium. The dimension of the linewidth and wire thickness is no less than 1 μm in the most advanced back end of line (BEOL) CMOS technology, thereby ensuring a low conductor loss and a good impedance match [16]. As in all technology scaling scenarios, metal losses increase significantly especially when the linewidth and thickness come close to a critical value of 100 nm. The DC metal conductivity degrades due to surface and grain boundary scattering. Wires are also more vulnerable to electro-migration [17]. In this regard, metallic carbon nanotubes outperform metallic nanowires. They exhibit ballistic flow of electrons with an electron mean free path of several microns and are capable to carry large current densities [18]. On the other hand, due to the lack of sufficient control over quality and geometry during fabrication, metallic nanowires may have more advantages than carbon nanotubes from a practical point of view. At this stage, CNTs may appear to receive more attention than nanowires. But there is an increasing interest in investigating metallic nanowires regarding their RF interconnect application.

Electrical Properties of Carbon Nanotubes

Carbon nanotubes are formed of sheets of graphite rolled into cylinders. The diameter is varying from 0.4 to 100 nm with lengths up to 1 mm [19]. Depending on the direction in which CNTs are rolled up, they demonstrate either metallic or semiconducting properties. Metallic CNTs have been considered as a promising interconnect material for the future. CNTs can also be categorized into single-walled (SWCNT) and multi-walled (comprising multiple concentric cylindrical shells) nanotubes (MWCNT). Both of them show excellent high current carrying capacity and thermal conductivities. For SWCNTs, it has been demonstrated that ballistic transport can be more easily achieved of the order of a micron. Therefore, they are a preferable candidate for interconnect application to MWCNTs [20]. The DC electrical properties of SWCNTs can be found in [21]. The resistance of a CNT is a function of the bias voltage and the length. For a nanotube with a short length, under small biases, the quantum resistance limit (or ballistic transport) can be reached. A CNT of a typical diameter of 1-2 nm exhibits high resistance per unit length. The minimum resistance of a single SWCNT is $h/4e^2$, which is approximately 6 kΩ. Several groups have demonstrated the resistance approaching this value experimentally [22]. Such performance shows insignificant improvement over metal interconnects. To overcome the large resistance associated with their small radius, it is natural to consider using bundles of carbon nanotubes. Their potential to surpass the performance of metal interconnects has been discussed in [23].

Concerning AC signals, the electrical properties of CNTs are not yet well understood experimentally. The pioneering work of Burke provides a qualitative description for the electrical model of CNTs at high frequencies [24]. They introduced the Luttinger liquid-based transmission-line model to account dynamic RF responses of a SWCNT over a metallic ground plane. While a traditional transmission line is modelled as a circuit having a magnetic inductance (L_M) and an electrostatic capacitance (C_E) as shown in Figure 1.1, the Luttinger liquid-based model includes an additional kinetic inductance L_K and a quantum capacitance C_Q (Figure 1.2) [25]. Furthermore, it has been theoretically demonstrated that the kinetic inductance can be 10,000 times larger than the magnetic inductance. The estimated L_K of a SWCNT is in the order of 16 nH/μm. On the other hand,

the quantum capacitance is 100 aF/μm, about the same order of magnitude as the electrostatic capacitance [26]. The very high inductance per unit length results in an electromagnetic slow-wave propagation with a phase velocity in the order of $c_0/100$ to $c_0/50$, where c_0 is the speed of light in free space [27]. This phenomenon of slow waves makes CNTs very appealing in RF applications as the reduction of transmission wavelength can leverage the miniaturization capability in RF integrated circuit design.

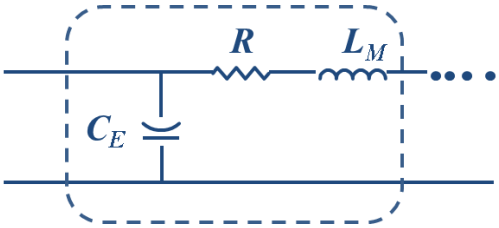


Figure 1.1 Conventional transmission line model [25]

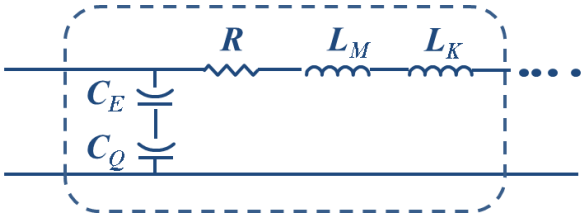


Figure 1.2 Equivalent circuit model for a carbon nanotube [25]

Electrical Properties of Metallic Nanowires

While research in metallic nanowires at high frequencies is still in its early stage, their DC properties have been studied for many years thanks to the remarkable advancement in CMOS technology. Copper was first introduced as interconnecting wires at the 220 nm technology node in the late 1990s [28]. It has a good conductivity among all the metals. Nevertheless, about 10 years later, the industry was facing performance limit due to the conductivity as wires must be even smaller. Processors using 32 nm technology node have already gone into mass production since 2010. The width and thickness of the lowest level of interconnects have scaled below 100 nm.

Nanoscale metallic wires can be obtained with different approaches. They can be fabricated either via physical deposition and e-beam lithography or chemical synthesis. For lithographically fabricated copper wires, it is known that the electrical resistivity is higher than bulk copper when the lateral dimension is scaled below 100 nm. Nanowires patterned by lithography are typically polycrystalline and have rough surfaces. Such nanowires suffer from surface and grain-boundary scattering thus giving rise to high resistivity [17]. Different models were proposed to evaluate which of these mechanisms is more dominating. The resistivity in nanoscale wires has been observed to be much greater than the bulk value as can be seen in Figure 1.3 [29] [30]. Chemically synthesized NWs, on the other hand, due to the single crystalline nature, exhibit much lower resistivity than that of polycrystalline NWs. Studies on the fabrication and characterization of single crystal silver, gold and copper nanowires with diameters of the order of 10 nm have been reported recently [31] [32]. These wires show a resistivity only twice as higher as that of bulk metals. They are also free of energy dissipation and void diffusion and have high failure current densities. Hence, in the domain of interconnects, they are quite attractive.

Just like CNTs, AC characteristics of metallic NWs were first studied theoretically. Similar transport properties were proposed to estimate the conductance, capacitance and inductance of metallic nanowires [25]. It was shown that metal nanowires do possess an appreciable kinetic inductance as in the case of CNTs if their cross section is reduced to the same order as that of CNTs. While the

magnetic inductance arises from the motions of charges or current, the kinetic inductance originates from the kinetic energy of the electrons. It is then intrinsic to any conductors. Its importance depends on the number of subbands or the current-carrying mode (M) in the energy band of the material. For a conventional transmission line, M is large enough that C_Q and L_K can be ignored whereas in the case of a CNT, the number of modes is only two. M is approximately equal to the number of half-wavelengths (electronic) that fit into the cross section. For copper wires, this quantum effect becomes increasingly pronounced when the cross section scales below 10 × 10 nm [25]. Based on Boltzmann's equation and Maxwell's equations, Hanson [33] derived a general expression for the spatially dispersive conductivity, which leads to a common form of intrinsic distributed impedance of CNTs and solid NWs. Their C_Q and L_K were evaluated from GHz up to THz frequencies. He concluded that for a solid metal wire with diameter equals to 10 nm, its resistance is approximately two orders of magnitude smaller than that of a CNT (The grain boundary and surface scattering effects were ignored) but the kinetic inductance is at least three orders of magnitude smaller. The quantum capacitance can be almost neglected. Obviously, slow wave propagation effect is not as significant in metallic nanowires as in CNT. The fact is that the electron relaxation time of a CNT is about 20 times longer than that of a metallic nanowire (the electron relaxation time is the time that an electron resides in a given quantum state before changing state as a result of collision with another particle or intrinsic excitation). This makes L_K acquire a greater significance at moderate frequencies at the order of ~100 GHz. In addition, in most of the reported models [25] [34], the skin effect was ignored. For example, the skin depth of copper is 300 nm at 60 GHz. It seems to be a plausible assumption that the skin effect is less effective in metallic nanowires, although it has never been proven experimentally.

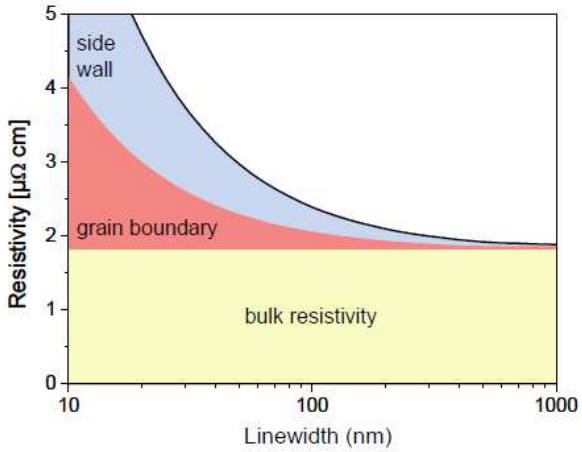


Figure 1.3 Cu resistivity as a function of linewidth, taking into account the grain boundary and interface electron scattering [30]

1.1.2 Nano-antenna

A critical unsolved problem in nanotechnology is how to make electrical contact from nano-devices to the macroscopic world. For future nano-systems consisting of a high-density circuitry, it is technologically challenging if each nano-device has to be connected lithographically. One potential solution is to use wireless interconnects [34]. If nanotubes or nanowires can act as antenna, it is possible to achieve short range data transfer such as wireless inter-chip and intra-chip communication while maintaining high complexity and density of nano-systems.

The feasibility of using a CNT as an antenna has been studied over the past years [27] [34] [35] [36]. Perhaps the most discussed configuration is dipole antenna. Due to the slow wave propagation effect, the wavelength of the electromagnetic wave propagating in a CNT is considerably smaller than that of the free-space. With this unique characteristic, CNT nano-antenna can be brought into resonance in the low terahertz regime [27]. In the case of metal nanowires, depending on the used

metallic material, similar phenomena can be found but only at optical frequencies or above [37]. Considering a carbon nanotube dipole with its half-length equal to 1 μm, the first resonance in the air is at 1300 GHz (phase velocity = $0.017c_0$) whereas a perfectly conducting metallic dipole with the same size would resonate at 75000 GHz [38].

However, it is clear that there are several issues to be addressed to make nano-antenna a reality. Nano-scale antennas have much lower gain and radiation efficiency than conventional wire antennas which is a characteristic of small size antennas. For instance, for a single wall carbon nanotube dipole having a diameter of 2.712 nm and a length of 10 μm, the antenna efficiency is at the order of 10^{-5} to 10^{-6} at the frequency from 10 to 450 GHz whereas the antenna efficiency of a copper dipole with a radius larger than a few microns is close to 1, behaving almost like a perfect conductor [38]. This is a result of the input mismatching between the CNT and the free space and the associated high conductor losses at this size. The radiation properties of metallic nanowires and carbon nanotubes for antenna applications in the GHz to THz range have been discussed in [39]. For a small radius dipole below 100 nm in radius, the working frequency needs to be increased to maintain a certain radiation efficiency. It was estimated that a copper dipole having a diameter of 80 nm can maintain radiation efficiency up to 50% if excited at 1 THz. Otherwise If a working frequency of 10 GHz is required, the radius of a copper dipole must be 750 nm. Alternatively, one can consider materials with better conductivity, such as MWCNTs or superconducting materials.

Another possible configuration of nanoscale antennas is the nanoelectronics-based integrated antennas. Over the past 40 years, wireless carrier frequencies have increased from 400 MHz in early improved mobile telephone systems (IMTS) to 5.8 GHz in today's IEEE 802.11a WiFi network. At millimeter-wave frequencies (>30 GHz) the size of an antenna becomes comparable to the size of a typical integrated circuit, thus enabling the use of on-chip antennas. Furthermore, the integration of antennas with the RF circuit has been recently received a lot of attention at 60 GHz thanks to the unlicensed bandwidth [40] [41]. These antenna elements are typically integrated at Metal 6 (copper), the top layer in the back end of the line (BEOL). A representative cross-section image of copper interconnects is shown in Figure 1.4 [42]. Considering a dipole configuration, a good performance with respect to gain can be obtained using a 30 μm wide and 632.5 μm long wire for a quarter wave length radiating element. A more detailed literature review will be provided in Chapter 4 regarding the state-of-the-art of on chip integrated antennas.

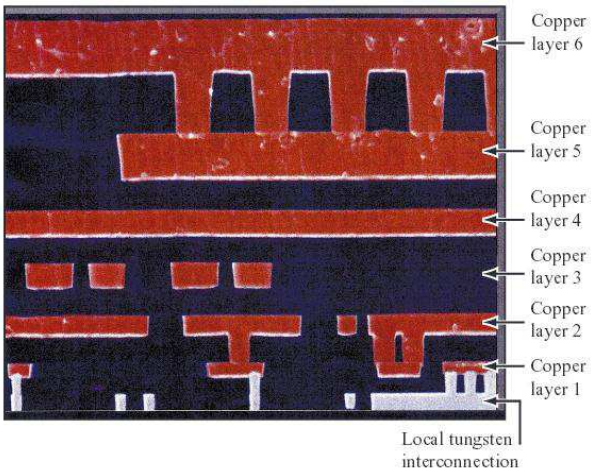


Figure 1.4 Cross-sectional scanning electron micrograph showing typical CMOS 7S interconnections with tungsten local interconnections and six levels of copper wiring [42].

There is no doubt that the technological progress in integrated circuits will facilitate the communication technology at frequencies up to 60 GHz, most likely to surpass several hundred GHz, and moving into the terahertz range by 2020 [43]. In this context, the exploration on nanoscale

antennas is appealing for they allow an extreme miniaturization. They are compatible with nano-electronic devices and at the same time suitable to operate at high frequencies. Above all, only at higher frequencies, the wavelength is reasonably small to enable efficient on-chip nano-antennas to be integrated on semiconductor substrates. In fact, this new class of antenna concept has recently been introduced into optical interconnect applications [44]. Zhou et al. [45] developed a prototype on-chip dielectric nano-antenna having a linewidth and thickness below 1 μm and length below 10 μm and tested it from 190 to 200 THz. As for millimeter-wave wireless interconnect applications, the applicability of submicron or deep submicron designs has yet to be demonstrated to understand their capability and limitation. Theoretically, using existing technology it should be possible to design small low-loss metallic antennas with reasonable performance. Hence they can be integrated into a single chip although it is certain that the issue of the transition from classical antennas to nano-antennas needs to be worked out in detail.

1.1.3 High-Frequency Characterization

An established approach to study integrated RF passive components such as transmission lines and antennas is to measure the scattering parameters (*S*-parameters). Almost all high-frequency characterizations for nanowires or nanotubes carried out to date are through two-port *S*-parameters measurement. The test sample can be integrated as a bridging component into a RF device which is compatible with on-wafer measurement for instance, a microstrip line or a coplanar waveguide as shown in Figure 1.5 [46] [47] [48]. Nanostructures can replace the central conductor as the signal line. Appropriate procedures can then be applied to de-embed the contribution of the platform or RF pads and thus move the reference plane just before the test device [49]. Such measurement setup makes the extraction of transmission characteristics of nano-metric scale devices possible. However, given the small dimension of nanowires, it is difficult to have a reliable measurement. New issues emerge such as impedance mismatching, reliability of the contact, pad parasitics and small signal level from the nanostructures. They most often have a strong influence on the accuracy of measurement result.

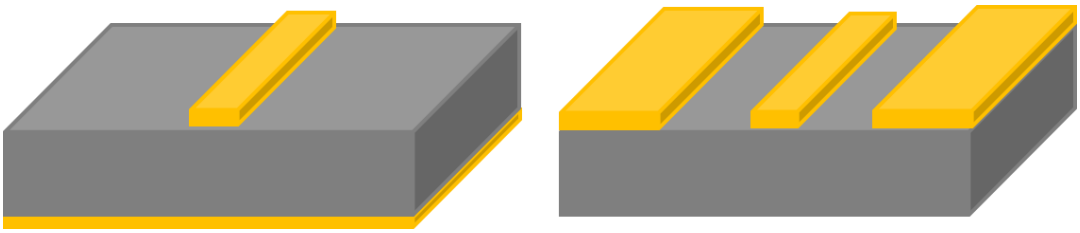


Figure 1.5 Generic view of 1) left side: microstrip line 2) right side: coplanar waveguide. They are potential platforms for characterizing nanowires, in which the central conductor can be replaced by the intened test sample.

Contact and Interface Effect

One inescapable problem that needs to be addressed in the measurement of nanoscale devices is the contact and interface effect. Fortunately, these effects can be approximated by lumped elements equivalent circuits. However, the determination of exact quantity is challenging due to that fact these effects become comparable to the signal being propagated in nanoscale devices. The accuracy of the measurement becomes critically important.

Most of the time, nanowires and nanotubes are in contact with RF pads by using clean room techniques including deposition of metallic layers (either sputtering or evaporation) and definition of patterns on a photoresist (E-beam or photolithography) [31] [50]. Inevitably, there exists contact impedance at the connection. According to the type of contact, it may have a significant contribution

to the total impedance. In the case of CNTs, contact impedance is typically modelled as a parallel RC circuit in series [26] [47]. Interface effect stands for the physical discontinuity between the pad and the nanowire. The width of a RF pad compatible with on-wafer probes is typically 50 μm or more which is at least three orders of magnitude larger than a nanowire. Such step change will cause a discontinuity in signal transmission. This effect is generally simulated as a shunt capacitance. Sometimes it is in series with an inductance on both sides [51]. The significance of discontinuity to the overall RF response depends on the characteristics of the line. In general, for a low-loss transmission line, it is important to determine the contribution from the interface [52]. Therefore, the design of RF pads needs to be carefully considered to facilitate obtaining a good measurement. They should exhibit minimum loss and transmission to be discerned easily [53]. In addition, the connection between the nanowire and the pads should avoid abrupt change in dimension. A common solution is to use a tapered design, in which the width of the pad decreases gradually towards the nanowire as shown in Figure 1.6 [47] [48].

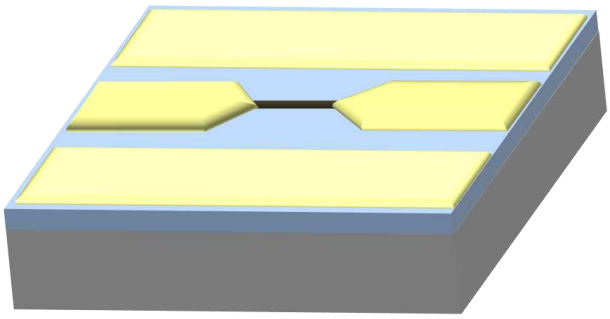


Figure 1.6 Generic view of a coplanar waveguide integrated with a nanowire. The tapered design RF signal pads can be seen.

Removal of RF Pads Effect

The essential challenge while characterizing a nanowire or nanotube is the impedance mismatching [36]. These nanostructures exhibit very high impedance as compared to the 50 Ω impedance of all RF test equipment. This leads to inefficient RF energy feeding to the test material. Besides, due to the high losses, the transmission signal is limited. This characteristic will introduce significant inaccuracy while de-embedding pad parasitics.

A vast literature exists today on de-embedding methods for transmission line characterization thanks to the advancing interconnect technology in RF circuits. These methods either use equivalent two-port analysis or lumped-component approximations. Some are proven to be more accurate than the others up to millimeter-wave frequencies [54] [55] [56], thus are already extensively adopted in the RF community. However, whether they are reliable or not for de-embedding nano-scale devices up to few hundred gigahertz remains open to question. Early works of several groups have employed the "open" de-embedding method to remove pad parasitics [57] [58]. This de-embedding method can be expressed in a simple algebraic form:

$$Y_{dut} = Y_{mea} - Y_{gap} \tag{1-1}$$

where Y_{dut} denotes the intrinsic admittance parameters (Y-parameters) of device under test (DUT, in this case, it is the nanowire), Y_{mea} denotes the measured admittance of the whole device (including the platform and the nanowire) and Y_{gap} is the admittance of the empty device (just the platform without the nanowire). The admittance parameters can be calculated from *S*-parameters. The concept of the method is based on an assumption of a circuit model. The pad parasitics leading to the DUT can be

solely described by a parallel admittance which can be determined by the measured admittance from the empty device. Consequently, the intrinsic response of the nanowire can be obtained through subtracting this admittance.

Another technique to extract the intrinsic response is to build a full circuit model to describe the *S*-parameters of an empty device, and then deduce new circuit elements that could be added to the model helping the fitting to the *S*-parameters of the device with the nanostructure [59]. The advantage of this approach is that we can understand better the effect of designed RF pads, avoiding the error that might be introduced due the approximation inherited in de-embedding methods. The downside is the number of unknown circuit elements involving in the fitting process. Figure 1.7 demonstrates an equivalent circuit model of a CNT integrated with a coplanar waveguide [47]. To reduce the amount of unknown lumped elements, Kim et al. [48] applied a full-wave model based on ADS Momentum (from Agilent) to simulate the empty device. The capacitance due to the coupling effect (C_{PS}) can be extracted by fitting to the *S*-parameters of the empty device. Depending on the physical properties of the contact and RF pads, circuit representation needs to be optimized to best describe a nanowire in contact with the RF pads in such a way that its intrinsic characteristics can be accurately extracted. Clearly, the validation of a model requires many tests and preferable on samples of different configurations and fabrication processes.

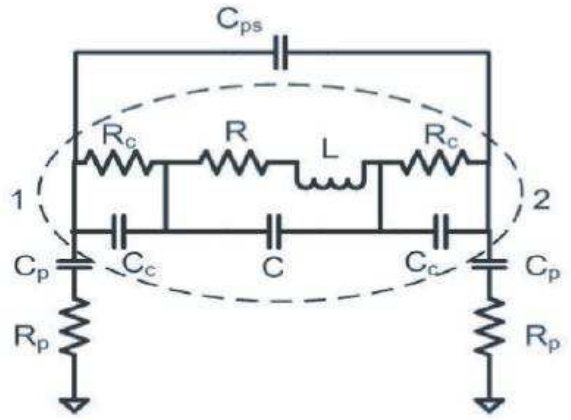


Figure 1.7 Equivalent circuit model of a test platform with a CNT. The dotted circle represents the circuit elements invoked when a CNT is placed between the pads. *C*p and *R*p denote the capacitance and resistance of the RF pads, *C*ps denotes the parasitic capacitance of the signal pad coupling, *R*c and *C*c denote the contact resistance and capacitance between the CNT and the pads, and *R*, *L*, *C* are the resistance, inductance, capacitance of the CNT [47].

Circuit Modelling of Nano-transmission Lines

Once the parasitic effect is removed from the signal, it is then possible to estimate the electrical properties of the nano-transmission lines. A representation for the lumped circuit model of a CNT itself consists of kinetic inductance along with an intrinsic resistance. The quantum capacitance is sufficiently small so it is not expected to be measurable [60]. Because of the much larger impedance than 50 Ω, the validation of each circuit element in a CNT has proven to be extremely difficult. Plombon et al. [26] has demonstrated that the resistance of an individual SWCNT is in the range of 10 to 30 kΩ/μm and L_K is around 8 to 43 nH/μm based on several measurements up to 20 GHz. Given the limited accuracy in measuring a single CNT, the multiple CNTs configuration is in fact a more appropriate solution to study their transport characteristics. Measurements of parallel arrays of CNTs were performed that yielded more stable and consistent results. They found that the total inductance of CNT bundles is consistent with a scaling of $L_{eff} \sim L_K/N$ (N is the number of CNTs). The extracted R_{bundle} is on the same order with the dc resistance.

High frequency characterization of metallic nanowire remains very little explored. From the result presented in [61], the contact resistance and conductivity of a single 300-nm-diameter platinum nanowire were extracted up to 50 GHz. Quantum effects (the concept of L_K and C_Q) were neglected and the contact was assumed to be an ohmic contact. Figure 1.8 plots the estimated contact resistance and conductivity from the *S*-parameters. Their result left out the extraction of physical meaningful transmission properties of nanowires. The major issues facing were primarily accuracy of the calibration and measurement noise at high frequencies.

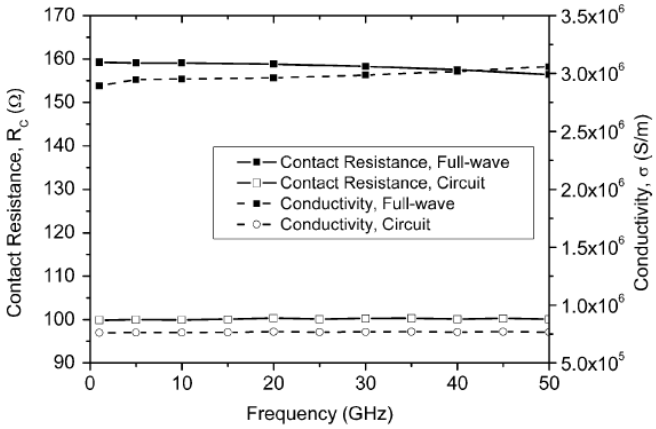


Figure 1.8 Estimated contact resitance and conductivity of Pt NWs [61]

1.2 Motivation

The high-frequency nano-electronics will continue to be one of the most dynamic research fields in nanotechnology. Experimental implementations are only starting. The challenge in nanoscale measurements has led to a slow progress in delivering the advancement. However, the characterization of the nanostructure properties is of paramount importance to establish the relationship between the functionality and their characteristics. Most studies reported in this domain are about carbon nanotubes. Little effort has been placed on metallic nanowires in both theoretical and experimental aspects. Nevertheless, metallic wires have long been the conventional material for passive devices applications. The distributed passive devices such as transmission lines in a silicon technology are typically built at the top two metallic layers in the back-end-of-the-line (BEOL). The minimum thickness is normally no less than 1 µm. As the continuous scaling of active components extends its capability well into mm-wave range, there is a need to develop high quality passive components to complement the integration density forming a system in a package. Making use of lower metallization layer to design passive component is a potential solution for this can bring together integrated RF circuitry in a compact way. Contrary to conventional transmission lines, the transmission properties of such thin-film RF module are not fully understood. Nanowires made of the same material may have dissimilar properties due to the influence of crystal structure, surface condition and aspect ratio. It is clear that much work is needed to explore full potential and limitation of nanoscale metallic lines all the way up to mm-wave frequencies.

Another scalable and cost-effective solution for nano and micro-electronic components integration is miniaturized on-chip antennas. The downscaling of circuit elements below 100 nm for complete system interaction on chip will apply to radiation elements eventually. Due to the lack of accurate model and characterization, the dimensional scaling of integrated antenna particularly at mm-wave frequencies is rarely investigated. The possibility to use nanoscale metallic on-chip antennas as building blocks for next-generation devices has motivated this study.

1.3 Objective

The objective of this thesis is to characterize the electrical properties of metallic nanowires for millimeter-wave transmission lines and antenna applications. The study is intended for exploring the transmission characteristics of metallic nanowires over a broadband of gigahertz frequencies with experimental and theoretical approach. The goal is to establish a relationship between their electrical performance and the geometrical and structural characteristics.

1.4 Scope of This Work

The nanowires fabricated in this study were defined by patterning metallic film using top-down lithography-nano-machining processes. In this way, alignment and positioning of nanowires can be specified and controlled. Nanowires were realized into transmission lines and on-chip antennas for characterizing their transmission up to 220 GHz. Such prototypes were made on standard silicon substrates because of familiar processing techniques. The minimum produced linewidth is on the order of 10 nm. But excessive metal loss may make characterization of such single wires unrealistic. Here, various linewidths ranging from 2 µm down to 50 nm and thickness from 200 to 50 nm were designed, evidencing the transition from the classical to the submicron and deep submicron wire regime. To develop a reliable test platform for characterising nano-transmission lines, two types of vehicles were tested: microstrip line and coplanar waveguide. The characterization was done through *S*-parameters measurement. From which, transmission line and antenna characteristics can be extracted. Theoretical modelling was also performed to verify the accuracy of the measurement and provide a physical understanding of the results. The simulation was carried out using ADS Momentum and ADS circuit simulation tools from Agilent.

Various transmission line de-embedding methods were reviewed. It is also the aim of this work to provide a systematic extraction procedure for nano-transmission lines and to dispel ambiguous data. Considerable focus was placed on the techniques for determining parasitics. Contact impedance and line to pad transition were taken into consideration in the extraction scheme. For the first time, a complete analysis was reported regarding transmission characteristics with line dimensions in the previously inaccessible regimes up to mm-wave frequencies. It is clear that excessive metal loss will make single nanoscale metallic wires inaccessible for technological applications. Multiple line devices and their relationship to the electrical parameters were characterized.

On the first try, the attempt was to evaluate the potential of metallic miniaturized antennas integrated on silicon substrate. To realize antennas with reasonable performance, the linewidth was constrained to at least 1 µm. But the thickness can be designed closer to nano-meter regime. The signal transmission of this type of antenna occurs predominantly inside the substrate. The work was therefore restricted to short distance intra-chip communication. The determined transmission gain between an antenna pair from two-port *S*-parameters measurement was only in the central forward direction. The input impedance may give an approximation about radiation capacity. The study is useful both to understand how nano-antennas differ from traditional antennas and to provide useful guidelines for designing integrated nano-antennas.

1.5 Outline

The thesis is organized as follows. First, characterization of submicron Al thin film microstrip line will be presented in Chapter 2. The analysis will reveal specific problems linked to characterization of nano-scale components integrated in a micro-scale test vehicle. In Chapter 3, a simple CPW test structure will be proposed to characterize Al and Au nano-transmission lines. The transmission characteristics of various line dimensions and device structures will be plotted and discussed. Inadequacies in the de-embedding techniques will be identified to improve the accuracy of transmission line measurement. Next, in Chapter 4, on-chip dipoles and planar inverted-F antennas integrated on different substrates will be used to evaluate the performance of nanoscale wires for wireless communication. The measured antenna characteristics in relation to the dimensional scaling will be presented. Finally, the key findings obtained in this work will be summarized in Chapter 5. Some potential future work will also be pointed out.

Chapter 2

Parameters Extraction of Submicron Thin Film Microstrip Lines

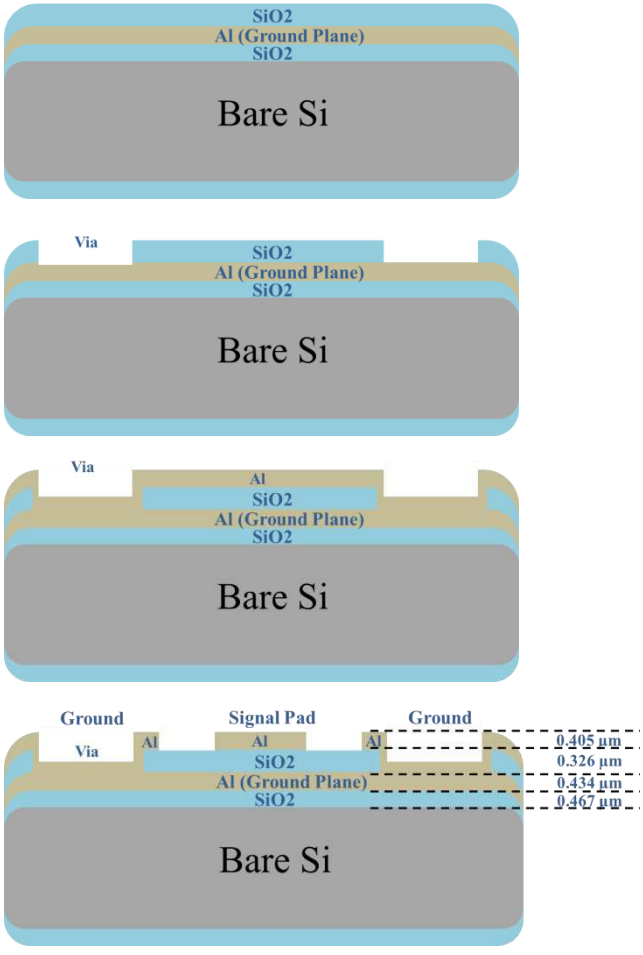
In this chapter, metallic nanoscale wires integrated into microstrip line feature will be tested. Microstrip lines are extensively used for transmitting signals in Si-based monolithic microwave integrated circuit (MMICs). Typically, in current CMOS technology, microstrip lines are realized at the top metal layer in the back end of the line (BEOL) with its thickness in the order of a few microns. However, the feasibility of using lower level metal layer in BEOL with smaller thickness and linewidth is very little explored since intuitively the conduction loss is an issue. One special advantage of microstrip lines is low substrate losses. The ground metallization can confine electromagnetic waves within the dielectric layer. Therefore, transmission performance will not suffer from lossy substrates such as low-resistivity silicon wafers [62]. As an initial approach for nanowires characterization, microstrip line structure can be an attractive vehicle.

The chapter starts by introducing the fabrication processes. Next, the characterization method will be presented. Preliminary *S*-parameters results will then be given. In the following section, an equivalent-circuit model based on transmission line theory will be used. ADS Momentum simulation will be also included for reference. The extracted experimental and theoretical transmission parameters of the lines will be presented and discussed. Finally, a modified circuit model will be introduced to accommodate the parasitic effect, allowing a more accurate prediction for the intrinsic electrical properties of the line over a wide range of frequencies.

2.1 Test Structure Fabrication

The thin-film microstrip line (TFML) structures of this study were fabricated on standard low resistivity silicon substrates. First, a 0.5 μm LPCVD silicon dioxide layer was deposited on both sides of silicon wafers for signal isolation. On top of it, a 0.5 μm thick aluminum (Al) layer as the ground plane of the device was realized by sputtering. A PECVD silicon oxide (ε_r = 3.9, tan δ_ε = 0.001) of 0.3 μm was deposited to serve as a dielectric layer for the TFML. Next, photolithography and a buffered oxide etching (Silox Vapox III) were used to pattern via holes. Silox Vapox III is a commercial buffered oxide etchant from Transene Company. It provides great etching selectivity between aluminium and SiO_2 layers. Its etch rate is about

250 nm/min. To define the microstrip area, the ground pads and the signal pads, an Al film (σ = 3.77 × 10^7 S/m) with thickness of 0.5 µm was sputtered and patterned with lithography. The photoresist was Shipley S1813 (about 0.5 µm). The exposed area was etched using Al wet etchant at 45ºC. This etchant consists of several different acids with the dominant one being H_3PO_4. The etch rate is about 300 nm/min. It should be noted that a good control of etch time is very important. Since wet etch is an isotropic process, the etchant would also attack the sidewall of the protected area, resulting in the undercut or even complete removal of Al lines. The process time should then be long enough to remove all the open area but not over-etch the Al lines. After photoresist stripping in acetone, the TFML structure and the pads can be obtained. A schematic drawing of each fabrication step is presented in Figure 2.1. The final structure layout can be seen in Figure 2.2 and a closer look at the transition before the line and the pad is shown in Figure 2.3. There are three kinds of line length (l) in this study including 100, 200 and 500 µm. Tapered signal pads were designed to minimize signal discontinuity, although they were not optimized for 50 Ω. Note that the pads are compatible with the two-port network *S*-parameter measurement which will be discussed later. The distance between the signal and the ground pad is 100 µm (Figure 2.2). The accurate thickness of the TFML was observed by scanning electronic microscopy (SEM). Values are presented in Figure 2.1 next to the illustration of the side view. It should be mentioned that due to the limitation of the photolithography process, only lines with linewidth larger than 1 µm can be realized.



Deposition of the isolation layers, the ground plane and the dielectric layer

Via hole oxide etching in Silox Vapox III

Deposition of the Al layer for the pads and the microstrip line

Wet etching to define the pads and microstrip line area

Figure 2.1 Fabrication steps of the TFML structure. The measured linewidth is 1.28 µm.

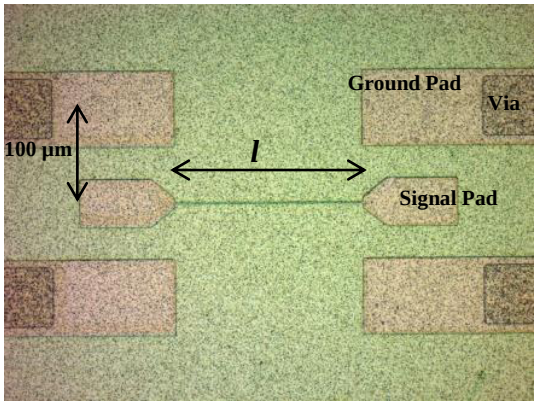


Figure 2.2 Photo of a fabricated 200 µm-long TFML and pads

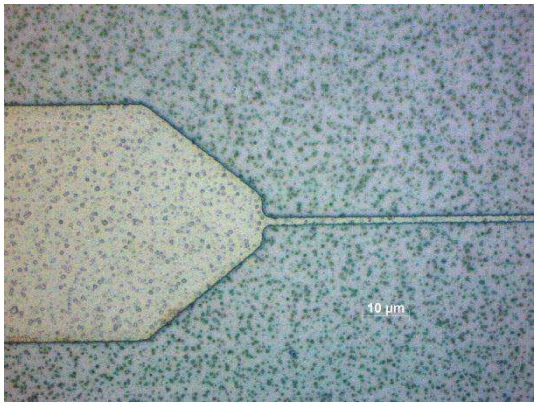


Figure 2.3 Close look at the transition between the line and the pad. Note that the pad and the line are in the same layer.

2.2 Scattering Parameter Measurement

Two-port scattering parameter (*S*-parameters) measurement is applied for examining the high-frequencies conduction of the transmission lines as a function of frequency. From *S*-parameters, it is possible to derive transmission line parameters, namely characteristic impedance (Zc) and propagation constant (γ) over a wide frequency band. They are the two essential physical parameters that characterize transmission lines. Characteristic impedance is comparable to the resistance that determines the amount of current that flows in a DC circuit whereas propagation constant describes the change of amplitude and phase of wave during the transmission. In the case of a lossy line, Zc and γ are complex number. In which, the real component of γ is called attenuation constant (α), representing losses during signal propagation. The imaginary component is called phase constant (β), which determines the speed of the propagation wave ($v = \omega/\beta$).

2.2.1. *S*-parameters Basics

RF signals are sent out from both ports. Some part of the signal bounces back. Some of it scatters and transmits to another port and some of it disappears as losses. *S*-parameters quantify how RF signal transmits through a device from one port to another. A typical two-port network is shown in Figure 2.4 [63]:

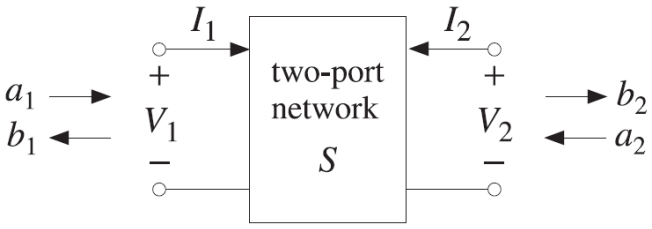


Figure 2.4 A two-port network [63]. Typically, port 1 is considered as the input port and port 2 is considered as the output port

A set of *S*-parameters is a mathematical matrix that relates the outgoing waves b_1, b_2 to the incoming waves a_1, a_2 as

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \cdot \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2-1}$$

Looking at the *S*-parameter coefficients individually, we have:

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \qquad S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0}$$
$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \qquad S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \tag{2-2}$$

S_{11} is equivalent to the input reflection coefficient and S_{21} is the forward transmission coefficient. Since test structures in this work consist entirely of symmetric passive components, the network is reciprocal. This also means $S_{11} = S_{22}$ as well as $S_{21} = S_{12}$. Apart from *S*-parameters, a linear two-port network can also be characterized by a number of equivalent circuit parameters, such as *ABCD* matrix (transfer matrix), impedance and admittance matrix. One can convert to another by using adequate equations.

2.2.2. Measurement Setup

The *S*-parameters of the TFML devices were measured using ANRITSU ME7808C Broadband Vector Network Analyzer (VNA) and a semi-automatic Cascade S300 station. The tests were conducted from 1 to 65 GHz using RF probes in GSG configuration with a pitch of 100 µm provided by Cascade Microtech. The VNA was calibrated using the Cascade Impedance Standard Substrate (ISS, 104 –783). Specifically, three types of standards were utilized, including thru, short and load, as shown in Figure 2.5. The material of this substrate is alumina. Load-Reflect-Reflect-Match (LRRM) calibration method was applied by using a commercially available software package WinCal from Cascade Microtech. LRRM has proven to offer the best accuracy and repeatability. It is also the least sensitive approach to the placement of the probe over the pad [16]. The details of this calibration procedure can be found in [64]. After the calibration, the reference plane is at the end of the probe tips, meaning that all errors up to the probe tips are removed. The calibration was verified on the thru standard within the general recommended limits of ± 0.1dB up to 65 GHz before testing. Each measurement was made with 201 frequency points using 128 averages in a 100 Hz resolution IF bandwidth. The settings for IF bandwidth and averaging determine the effective noise. IF bandwidth is roughly proportional with the reciprocal of the sweep time. Point-by-point feature was adopted for averaging. This means additional measurements, in this case 128 data points, at each given frequency point are taken at once. In this way, the displayed data can be fully optimized during a single sweep. Generally, reducing IF bandwidth and increasing the point averaging can both minimize the noise although the sweep time is compromised. The chuck was electrically connected to the ground probes. Three test samples with different line lengths and the de-embedding structures were measured.

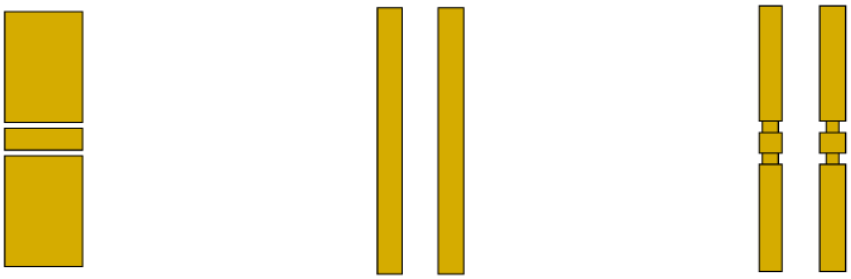


Figure 2.5 The standards used in the calibration. From left to right, thru, short and load are shown.

2.2.3. De-embedding Procedure

De-embedding is the act of removing the reference plane close to the device under test (DUT, in this case, it is the nanowire). A schematic explanation is shown in Figure 2.6. After the calibration, the reference plane is situated at the end of the probe tips. However, the RF pads used to access the DUT are inherent in the measurement. This could sometimes alter entirely the measured characteristics, especially when the device is small.

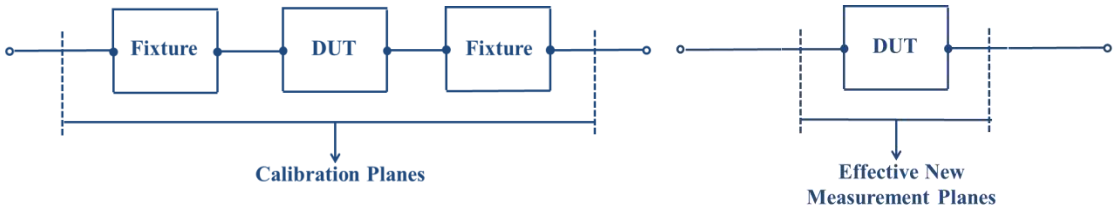


Figure 2.6 Schematic explanation of the effect of de-embedding. Left: the reference plane is at the end of probe tips and in front of the fixtures (RF pads) after calibration. Right: New reference plane is created after de-embedding the error boxes of the fixtures [65].

There are many de-embedding schemes for removing the effects of test fixtures from device measurements. Each fixture needs to be first modelled. Then, appropriate techniques can be selected for de-embedding process. That said, the most difficult part is to create an accurate model. Generally, an initial fixture model can be derived by an observation of its physical structure. To account the actual behaviour of these fixtures, measurements made on de-embedding structures are required [66]. The de-embedding structures designed in this test include open and short, as shown in Figure 2.7. The fabrication process is the same as that describe in Section 2.1.

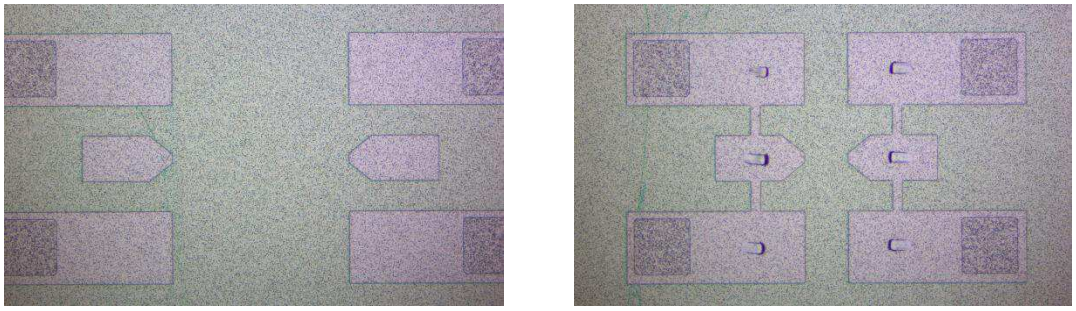


Figure 2.7 De-embedding structures for the TFML. The left photo shows a open device and the right one is a short device

The de-embedding technique used in this work is short-open method, which is given by [67]:

$$Y_{dut} = (Z_{meas} - Z_{short})^{-1} - (Z_{open} - Z_{short})^{-1} \quad (2\text{-}3)$$

where Z_{open}, Z_{short} are the two-port impedance parameters measured on the open and short devices. Z_{meas} is the measured two-port impedance of the device and Y_{dut} are the *Y*-parameters after de-embedding. The admittance is then converted to *S*-parameters. This type of purely lumped de-embedding technique can remove the effects of shunt capacitance and series losses of the RF pads. From the *S*-parameters, the transmission line parameters: characteristic impedance *Zc* and propagation constant γ can be evaluated as [68]:

$$Zc = \pm Z_0 \cdot \sqrt{\frac{(1+S_{11})^2 - (S_{21})^2}{(1-S_{11})^2 - (S_{21})^2}} \quad (2\text{-}4)$$

and

$$\gamma = -\frac{1}{l} \cdot ln\left(\left(\frac{1-(S_{11})^2 + (S_{21})^2}{2 \cdot S_{21}} \pm K\right)^{-1}\right) \quad (2\text{-}5)$$

where Z_0 is the impedance of the measurement system (50 Ω in our case), *l* is the length of the NW and *K* is defined as follows:

$$K = \left(\frac{(1-(S_{21})^2 + (S_{11})^2)^2 - (2 \cdot S_{11})^2}{(2 \cdot S_{21})^2}\right)^{1/2} \quad (2\text{-}6)$$

Note that the plus and minus symbols in Equations (2-4) and (2-5) are used for correcting unrealistic values. For instance, propagation constant should never be negative.

2.2.4. Preliminary Results

Figure 2.8 and Figure 2.9 show the measured *S*-parameters in magnitude before and after de-embedding. One can immediately identify the bad measurement from the reflection coefficients, S_{11}. The measurement of l = 100 µm suffers from the bad contact when landing the probes onto the pads. It is relevant to mention that the thickness of the pads is rather thin (about 0.4 µm) for the probe tips. Very often, the tips penetrated through the pads and touching the underlying oxide. Poor probe-pad contact introduces additional parasitics. In response to this, reflection coefficient appears significantly different from the others. Despite the bad probing characteristics, the transmission coefficients S_{21} behave quite well as shown in Figure 2.9. As expected, the longer the line, the higher the insertion loss (insertion loss is defined as $-20\log_{10}|S_{21}|$). Besides, the insertion loss increases with increasing frequency. It can be seen that the pad design is not optimal. For one, the parasitics of the pads is much larger than the intrinsic device signal. This might introduce additional errors and uncertainties after de-embedding.

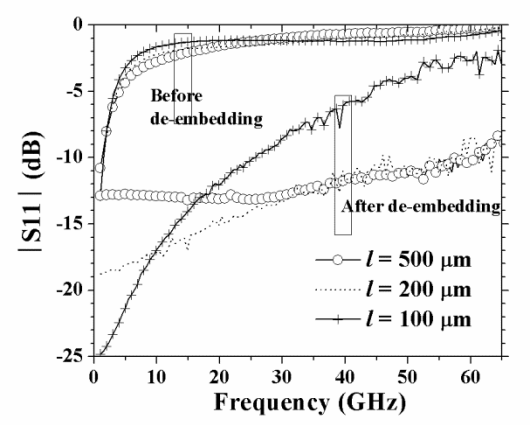


Figure 2.8 Comparison of the magnitiude of S_{11} before and after de-embedding

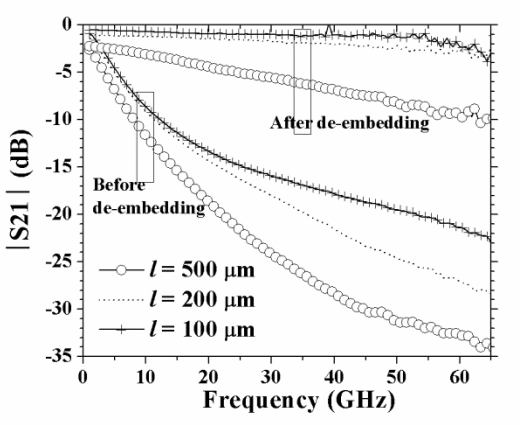


Figure 2.9 Comparison of the magnitiude of S_{21} before and after de-embedding

2.3 Modelling

As mention earlier, a transmission line can be modelled as a two-port network if the line is uniform along its length. Its behaviour can be described by two parameters: characteristic impedance (*Zc*) and propagation constant (γ). Typically, a transmission line has its constants of resistance (*R*), inductance (*L*), capacitance (*C*) and conductance (*G*) per unit length lumped together. They are distributed along the length and cannot be separated individually [69]. Therefore, a transmission line can also be modelled as a distributed circuit model. This conventional transmission line model will be used as a first approach for the simulation of nanoscale transmission lines, and the assessment of its applicability will be described in the next section.

2.3.1. Implementation of a Lumped Circuit Model

A TFML can be described by an equivalent-circuit model as shown in Figure 2.10 if a quasi-TEM propagation is satisfied. Note that the light blue layer represents the SiO_2 sandwiched between the conductors where the propagation takes place. *R*, *L*, *C*, and *G* per unit length depend on the properties of the materials and the geometrical dimension of the microstrip line. Similar to *Zc* and γ, the quantity of these elements is irrelevant to the line length. F. Schnieder and W. Heinrich have implemented a closed-form model to determine individually the circuit elements with a sufficient accuracy [62]. The approximation is particularly suitable for small dimension conductors. In this work, only the quasi-static analysis was considered and the distributed elements of these lines were calculated based on the close-form formulas developed by them. There are two reasons why this model was chosen: (1) The close-form formulas provide an understanding to the impact of each physical parameters to the transmission properties of the line, (2) The model is valid for a broad frequency range, starting from DC, medium frequency up to the beginning of the skin effect region. Once *R*, *L*, C and *G* circuit elements are obtained, theoretical *Zc* and γ can be estimated using the following equations:

$$Zc = \sqrt{\frac{(R + j \cdot \omega \cdot L)}{(G + j \cdot \omega \cdot C)}} \tag{2-7}$$

$$\gamma = \alpha + j \cdot \beta = \sqrt{(R + j \cdot \omega \cdot L)(G + j \cdot \omega \cdot C)} \tag{2-8}$$

To verify the model, the calculation result will be compared with the measurement. Also, results from ADS Momentum are included for comparison. The simulation set up will be explained in the next section.

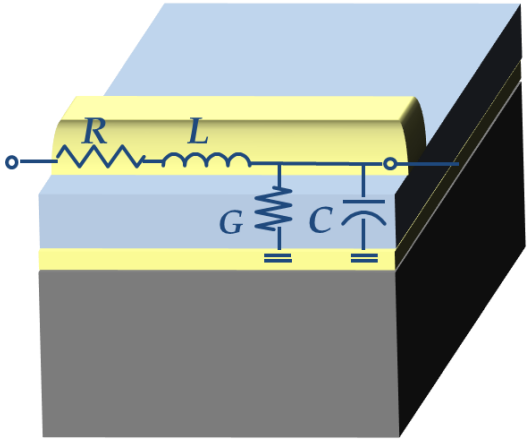


Figure 2.10 Ilustration of the equivalent circuit model in a TFML structure

2.3.2. ADS Momentum Simulation

Momentum is one of the features in Agilent ADS simulator, as shown in Figure 2.12. It uses Method of Moments (MoM) to computes *S*-parameters for RF passives, high-frequency interconnects and parasitic modelling. It is based on 2D component layouts and provides users a 3D perspective of current flow in conductors or slots and far-field radiation patterns. The defined patterns in the layout are first meshed with rectangular and triangular cells. Each cell is described by an equivalent circuit. The current can then be solved by applying Maxwell's equation and Kirchoff voltage laws in the equivalent network [70]. One of the important advantages of using MoM is that it consumes less time to simulate microwave components compare to full 3-D simulators. Another benefit is that it accepts arbitrary design geometries, including multi-layer structures. To simulate a thin-film microstrip line, a centre conducting strip was created. The layout of the device can also be found in Figure 2.11. Notice that RF pads were omitted from simulation. Meanwhile, single port was selected to excite the either side of the conductor. The dielectric layers and the ground plane in the thin-film microstrip line structure can be generated using the substrate definition interface demonstrated in Figure 2.12. With this setup, *S*-parameter as a function of frequency can be obtained.

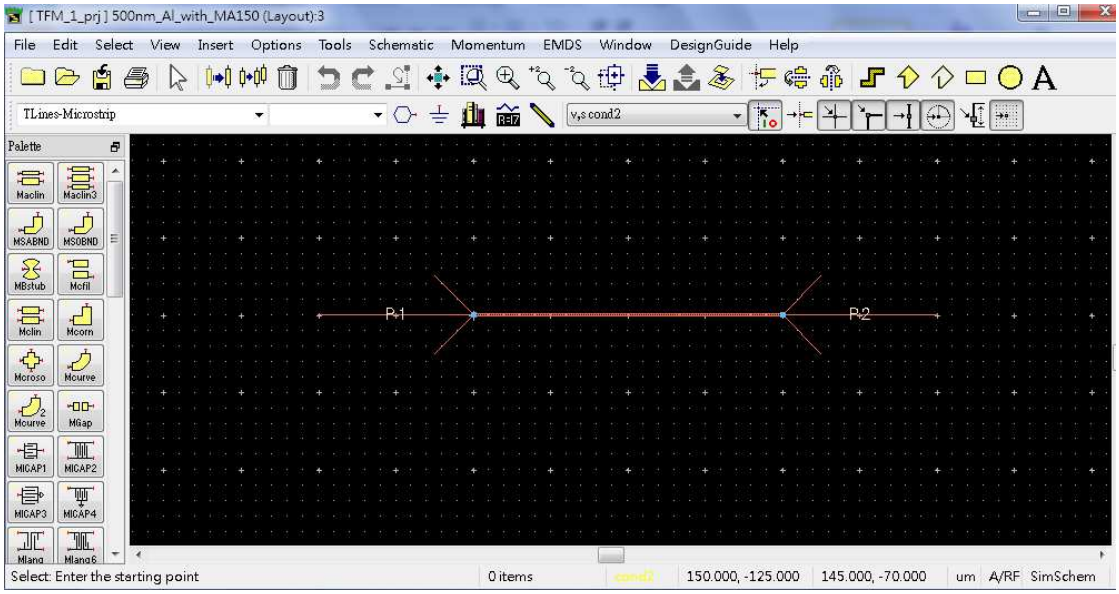


Figure 2.11 ADS Momontum user interface showing the simulation setup for TFML

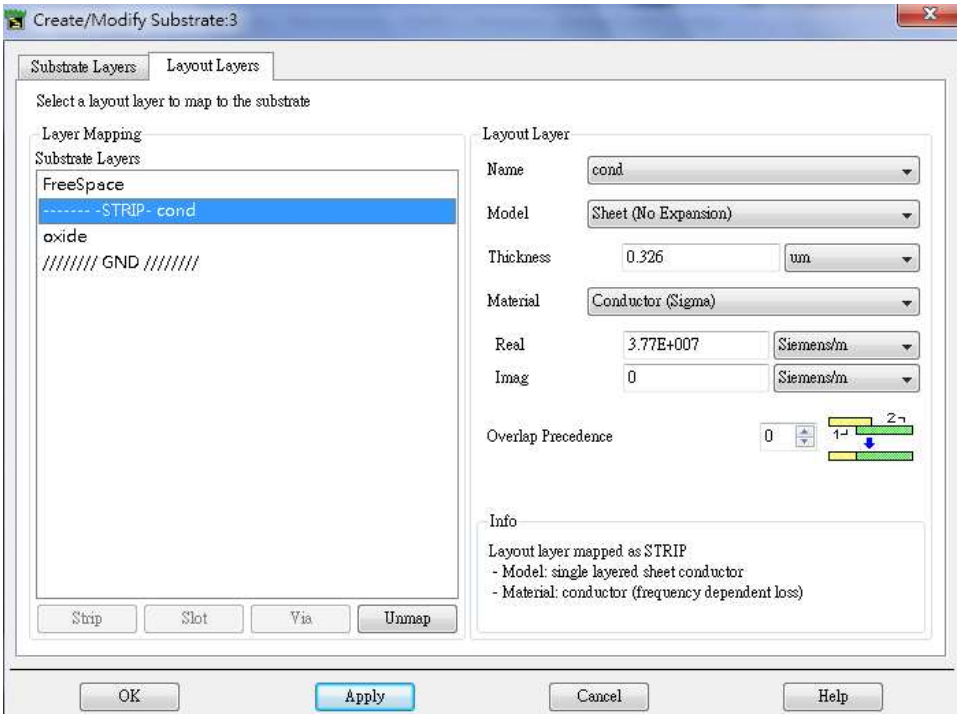


Figure 2.12 Substrate defination interface in Momentum

2.3.3. Theoretical and Experimental Comparison

The experimental *R*, *L*, *G* and *C* can be calculated from *Zc* and γ using the Equations (2-7) and (2-8). Then, the following equations can be derived:

$$R = \mathrm{Re}\{\gamma \cdot Zc\} \qquad L = \mathrm{Im}\{\gamma \cdot Zc\}/\omega$$

$$G = \mathrm{Re}\{\gamma/Zc\} \qquad C = \mathrm{Im}\{\gamma/Zc\}/\omega \tag{2-9}$$

Figure 2.13 and Figure 2.14 present theoretical and experimental *R* and *L* per-unit length up to 65 GHz. It can be seen that above 15 GHz, *R* extracted from the measurement of l = 100 µm appears different from the others but corresponds well to Schneider and Heinrich's theoretical value. *R* approximated from the close-form formula gradually increases with increasing frequency. This means that the physical behaviour of the line in the frequency band of analysis is within the medium frequency region. As for the inductance, the actual values are very cohesive and fit well with Schneider's model. We can see that *L* decays as the frequency increases. Meanwhile, ADS Momentum as a whole has an inferior performance in determining *R* and *L*.

Figure 2.15 shows that there is significant discrepancy between the measurement and the simulation. The capacitance is underestimated by the model. It can be seen that the values from l = 200 and 500 µm are almost identical. This suggests that such additional capacitance inherent in the measurement is not a random phenomenon. A possible source for this inconsistency is likely due to inadequacy while de-embedding pad parasitics. Note that the capacitance extracted from l = 100 µm is significantly higher than the others. This is probably caused by poor probe-to-pad contact as mentioned earlier.

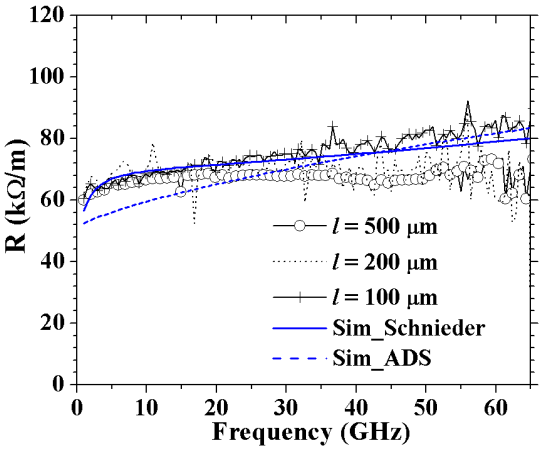


Figure 2.13 Resistance per unit length vs frequency

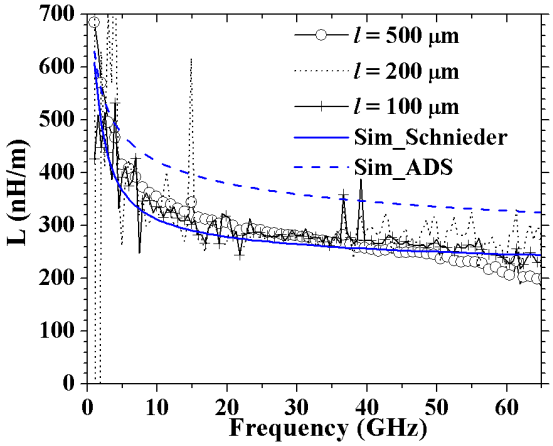


Figure 2.14 Inducance per unit length vs frequency

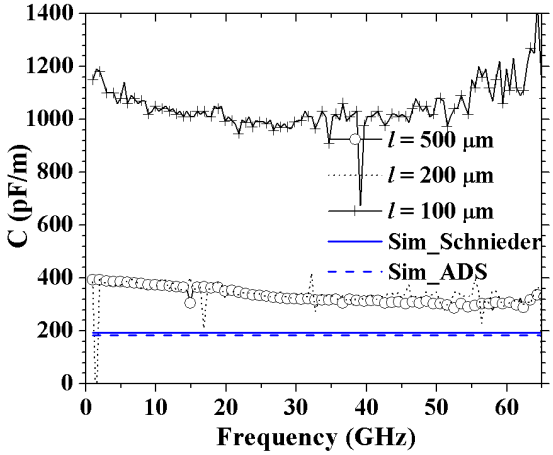


Figure 2.15 Capacitance per unit length vs frequency

2.3.4. Full Circuit Model

As it appears that the de-embedding lacks accuracy, it is necessary to identify the source of uncertainty. Several authors have reported the issue of step discontinuity when characterizing submicron-thick small microstrip lines at millimeter-wave frequencies [52] [71] [72]. They have observed that the determination of transmission line parameters is very sensitive to parasitic effect at the transmission line end. The open end leads to scattered electrical field. To account for this effect, additional circuit elements need to be considered at the transition between line and pad. Typically, step discontinuity can be described by a circuit structure with two equivalent series inductances and one shunt capacitance. At the first attempt, the network model of the discontinuous effect is simulated with a shunt capacitance *C*d, shown in Figure 2.16. Such assumption was also utilized in [54]. The two-port T network is equivalent to the contribution of a transmission line.

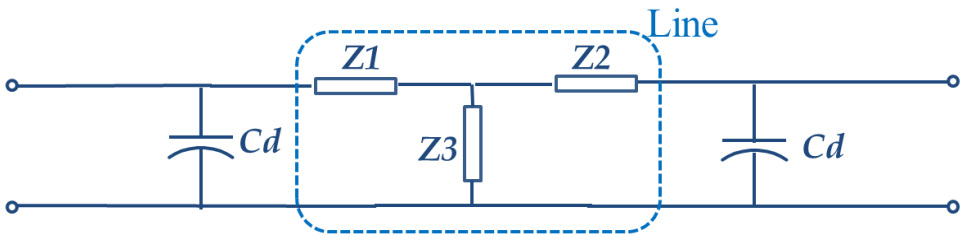


Figure 2.16 Circuit model of the complete test strucutre, line and the pads

*Z*1, *Z*2 and *Z*3 are calculated using:

$$Z1 = Z2 = j \cdot Zc \cdot \tan\left(\frac{l \cdot \beta_c}{2}\right) \tag{2-10}$$

$$Z3 = \frac{-j \cdot Zc}{\sin(l \cdot \beta_c)} \tag{2-11}$$

where *Zc* is characteristic impedance given by Equation (2-7) and *βc* is obtained using:

$$\beta_c = \omega \cdot \sqrt{(L + \frac{1}{j \cdot \omega} \cdot R) \cdot (C + \frac{1}{j \cdot \omega} \cdot G)} \tag{2-12}$$

An optimized *Cd* can be found through the fitting process in ADS simulator that minimizes the difference between the measured and simulated transmission line parameters. Results will be presented in the following section.

2.4 Results and Discussion

In this section, the extracted result and the theoretical prediction will be first presented. The properties of the TFMLs will then be revealed. An attempt to validate the full circuit model points out the limitation of the de-embedding technique. In the last section, the sensitivity of transmission parameters to parasitic residue will be addressed.

2.4.1. Extraction of Transmission Line Parameters

The experimental characteristic impedance and propagation constant of the lines with l = 200 and 500 µm are presented in Figure 2.17 to Figure 2.20. The simulated values from close-form approximation (Section 2.3.1) and ADS Momentum are included for comparison. It should not be surprising that the measurement differs significantly from the simulation. This is actually a direct result of the higher capacitive component found in Section 2.3.3. It can be seen that the extracted *Zc* are much lower than the theoretical ones while the losses and phase constant show the contrary. These results suggest that new elements must be added to the simulation to better represent the measurement.

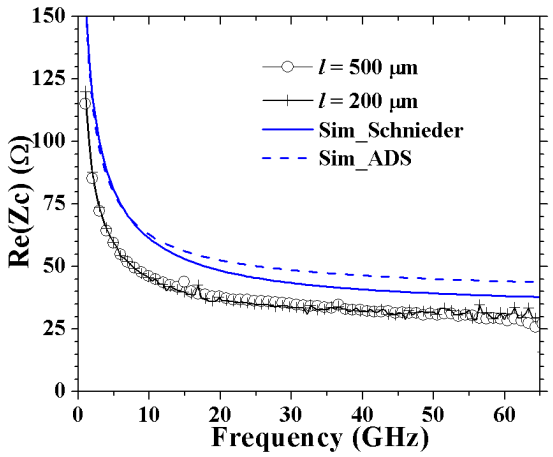


Figure 2.17 Real part of *Zc* for the measured and simulated TFMLs

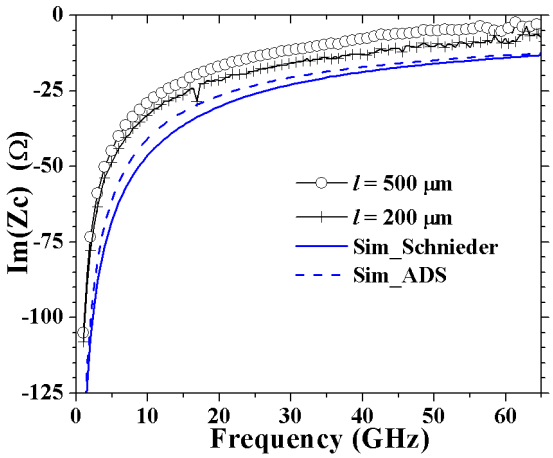


Figure 2.18 Imaginary part of *Zc* for the measured and simulated TFMLs

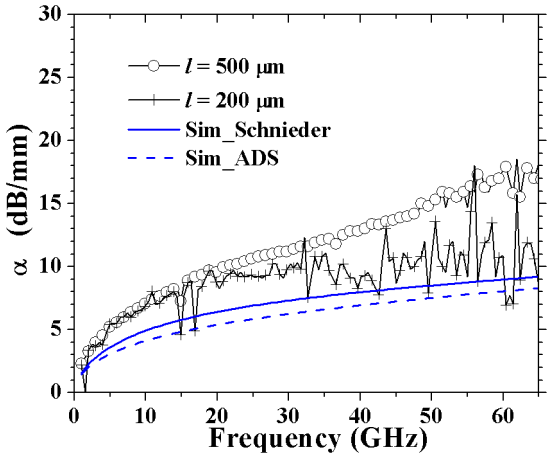


Figure 2.19 Attentuation for the measured and simulated TFMLs

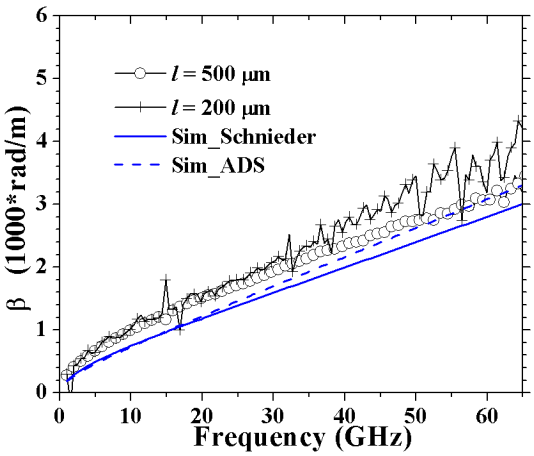


Figure 2.20 Phase constant for the measured and simulated TFMLs

2.4.2. Preliminary Validation

Let us therefore reconsider the model with the additional circuit element described in Section 2.3.4. Figure 2.21 and Figure 2.22 demonstrate the fitting result to the extracted *Zc* and γ from the measurement of l = 200 µm. The best fitting was obtained by applying a *Cd* value being 14 fF. The remarkable agreement gives confidence to the assumption of lumped *Cd*. A significant correction in *Zc* is noticeable with the addition of *Cd* across the frequency range. The attenuation constant α shows similar trends and approaches the experimental value. In

other words, the extracted transmission line parameters can be erroneously determined because of capacitive parasitic.

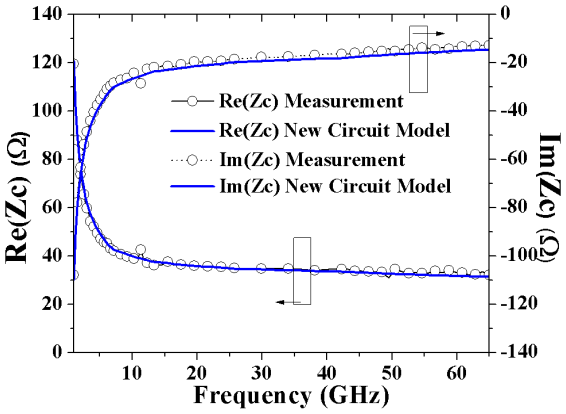


Figure 2.21 Real (left) and imaginary part (right) of *Zc* for the measured and simulated 200 µm-long TFML

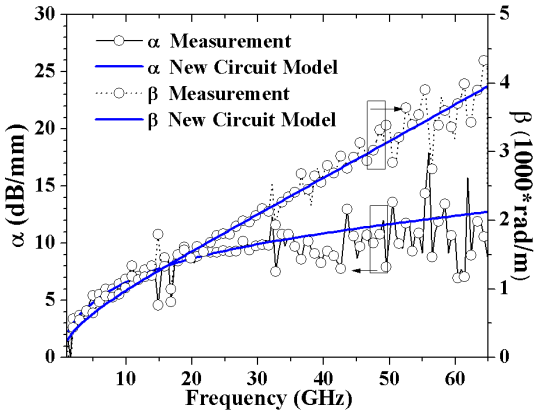


Figure 2.22 Attenuation (left) and phase constant (right) for the measured and simulated 200 µm-long TFML

2.4.3. The Impact of Pad Residual Capacitance

Having identified the problem which plagues measurements, it would be interesting to see how parasitic capacitance can adversely affect the measured characteristics. The parasitic contribution can be isolated from the line by comparing the raw *S*-parameters (calibrated only) to the simulated ones. Next, similar step can be applied to search for the best fitted *Cd* although in this case *Cd* represents the pad and the pad-line discontinuity lumped together. Figure 2.23 to Figure 2.26 show the fitting result for two sets of measurements (l = 200 and 500 µm). A good agreement up to 65 GHz is found for both cases by lumping a capacitive component of about 640 fF. With this knowledge, we can discuss the level of uncertainty in the measurement due to the capacitive parasitic residue.

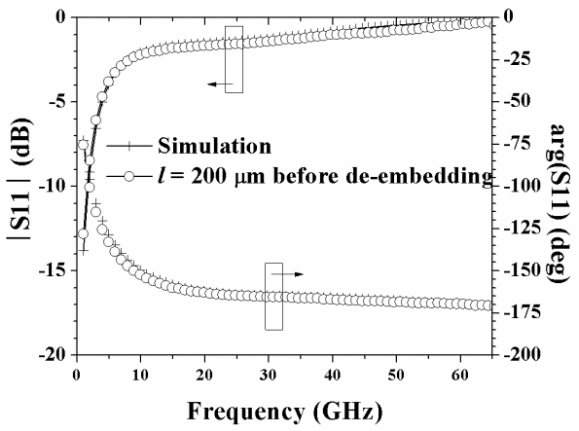


Figure 2.23 Experimental and simulated S_{11} of l = 200 µm

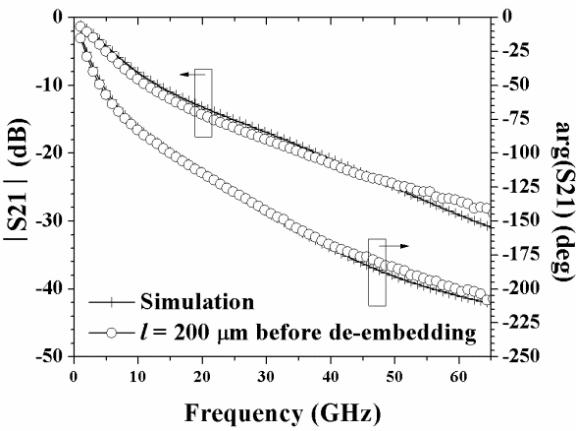


Figure 2.24 Experimental and simulated S_{21} of l = 200 µm

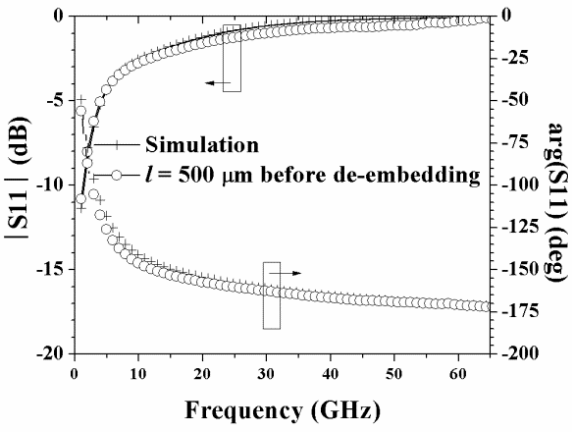


Figure 2.25 Experimental and simulated S_{11} of l = 500 µm

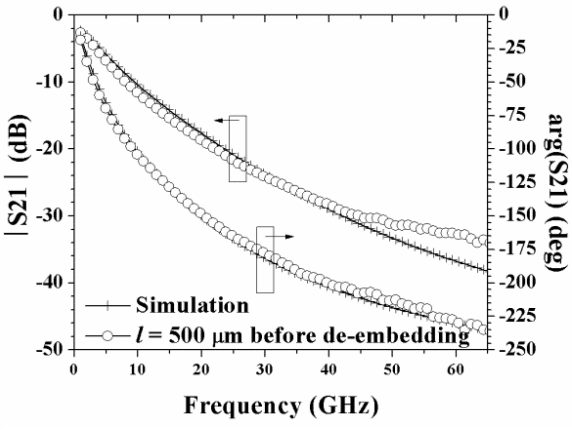


Figure 2.26 Experimental and simulated S_{21} of l = 500 µm

Figure 2.27 to Figure 2.30 demonstrate the sensitivity of the extracted transmission line parameter in response to capacitive parasitic residue in percentage. Two line lengths were considered in the simulation: 200 and 500 µm using close-form approximation. Sim_Schnieder denotes the theoretical prediction of the intrinsic line, therefore the ideal case. To simulate the effect of residue, a quantity of capacitance was deliberately included at both ends of the line. Therefore, the dataset of l = 200 µm, error = 5% represents a 200 µm-long intrinsic line embedded with a shunt capacitance of 32 fF (as 5% out of 640 fF) at both ends of the transmission line. The results show that even a small quantity of capacitance can lead to an erroneous reading deviating from an ideal case. Moreover, the shorter the line is, the more offset can be observed.

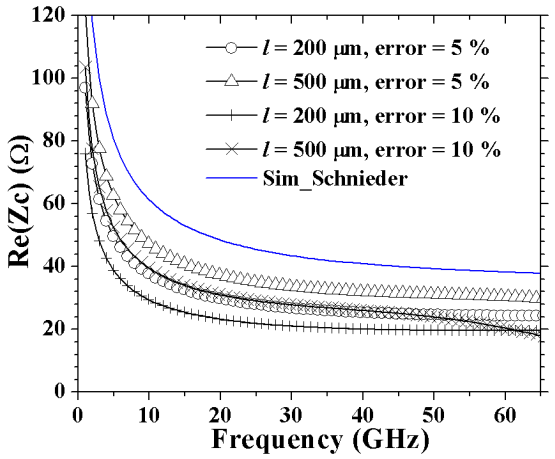


Figure 2.27 Variation of real part of *Zc* as a result of capacitive parasitic residue

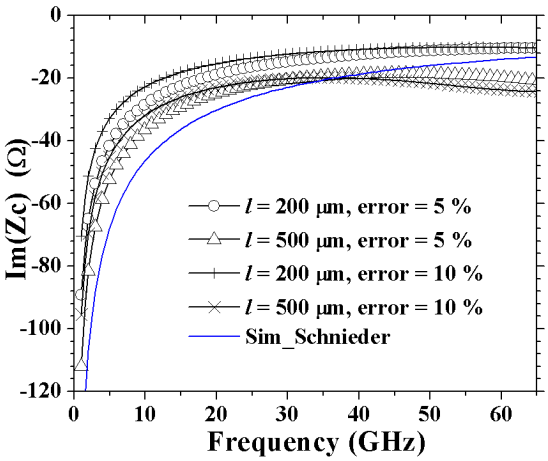


Figure 2.28 Variation of imaginary part of *Zc* as a result of capacitive parasitic residue

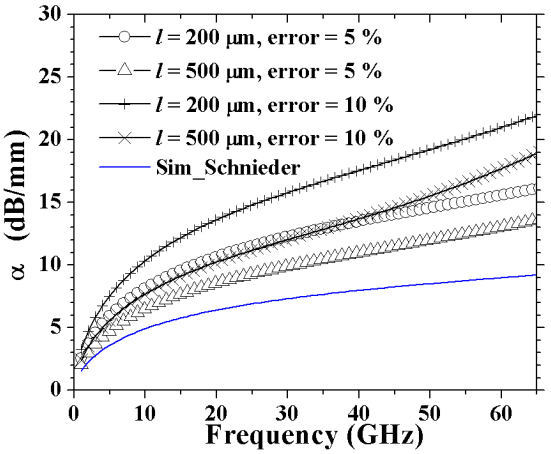


Figure 2.29 Variation of attentuation as a result of capacitive parasitic residue

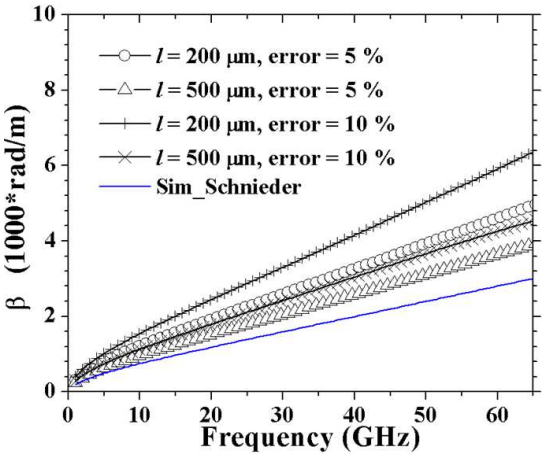


Figure 2.30 Variation of phase constant as a result of capacitive parasitic residue

2.5 Conclusion

The fabrication, characterization and modelling of submicron Al thin-film microstrip lines up to 65 GHz have been presented in this chapter. Microstrip lines have advantages over other types of transmission lines, because of its low substrate loss, making them natural candidate to be a characterization platform for nanowires. The closed-form expressions were used to estimate the RLCG circuit elements. Unlike traditional transmission lines, such TFML structure has significant attenuation and its characteristic impedance shows strong dependence on frequency at the lower frequency region. The extracted transmission line parameters from measured and simulated results suggested that capacitive parasitics remain embedded in the measurement data after de-embedding. The accuracy of transmission line characteristics is significantly undermined. The capacitive component is most likely attributed to the electrical discontinuity between pad and line. The effect of this parasitic residue was examined using sensitivity analysis. Unfortunately, the dimension of the line is not entirely at nano-metre level due to technological constraints. In the following chapter, another type of characterization platform: coplanar waveguide will be tested. Transmission lines characteristics with both linewidth and thickness down to 100 nm will be presented.

Chapter 3

Characterization of Metallic Nanoscale Transmission Lines up to mm-wave Frequencies

In this chapter, we will continue on the path of characterization nanoscale transmission lines. A new structure will be applied as a test platform for aluminium and gold lines and the frequency range is extended up to 210 GHz. The cross-sectional area of the wires is at the lower range of nanometric scale. The fabrication, measurement and modelling of nanoscale metallic lines will be presented. The aim of the work is to understand the high-frequency transmission properties of nano-lines in relation to the line geometry (linewidth, thickness and length) and device configuration (single or multiple lines structures). At the same time, the presented results are intended to establish a reliable characterization scheme.

The chapter is divided into three parts. Section 3.1 is dedicated to the characterization of single aluminium nano-lines up to 100GHz. Another test set comprised of single and multiple gold nano-lines will be examined in Section 3.2. These nano-lines are realized on conventional oxide-isolated silicon substrate. Different methodologies will be tested to extract intrinsic frequency-dependent transmission line properties. Their sources of uncertainty are pointed out. Eventually, a modified de-embedding procedure is adopted that has successfully improved the accuracy of transmission line measurements. The extracted intrinsic transmission line parameters of these nano-line devices are then compared and discussed in detail. In Section 3.3, the measured characteristics of the nano-lines up to 210 GHz are presented. The chapter will then be concluded with a summary of important characteristics of the nano-lines, which can be utilized wisely while designing passive components. Meanwhile the guidelines for designing a robust characterization platform are given.

3.1 Single Aluminium Nano-lines

To study the electrical properties of nanowires at high frequencies, they need to be integrated into a micron size platform in order to be compatible with the test equipment. A coplanar waveguide (CPW) was designed that consists of contact pads to test the nanoscale lines. It also serves as the ground planes for signal propagation. One of the main advantages of CPW is that all conductors lie on the same plane. There is no need for via holes as the TFML structure in Chapter 2. It is known that aluminium has a good conductivity and excellent adhesion to the SiO_2 layer; hence it is a good starting point as a metallic nano-line material.

Section 3.1 starts with the device fabrication and description of the measurement setup. Next, a quasi-TEM model is presented to simulate wave propagation in the transmission lines which is employed throughout the whole chapter. A step-by-step method to subtract parasitics from the pads and contacts will be proposed. Later the source of uncertainty and level of inaccuracy of the methodology will be pointed out and therefore further improvement is required. At the end of the section, an alternative method for de-embedding with enhanced accuracy will be addressed. The new method will be used in Section 3.2 for the new test structures that yield more accurate measurements.

3.1.1. Test structure Fabrication

The test device includes an individual Al metal line embedded in the middle of a CPW structure (the two ground planes and RF pads) as shown in Figure 3.1. Table 3.1 summarizes the geometric parameters of the devices-under-test (DUT). The reason for these choices of dimension is to cover the range from micro- to nano-scale wires. Nanoscale characterization requires high precision. A conventional micro-transmission line can be a perfect complement to visualize the accuracy of measurement as well as the validity of model.

The substrate is a standard silicon wafer (resistivity: 5-10 Ω.cm) with a 500 nm thick SiO_2 layer on the front and back side. The Al wire for sample Nos.1-3 were fabricated by electron beam lithography (EBL) and lift-off method. First, line features were patterned in JBX-6300FS Electron Beam Lithography System with PMMA 950 K 4% (0.3 µm thick) as resist. Next, an Al layer was deposited by evaporation with a deposition rate of 0.1 nm/s. After a subsequent lift-off process in acetone, Al lines can be obtained. The line for sample No.4 was fabricated in a single step together with the CPW structure.

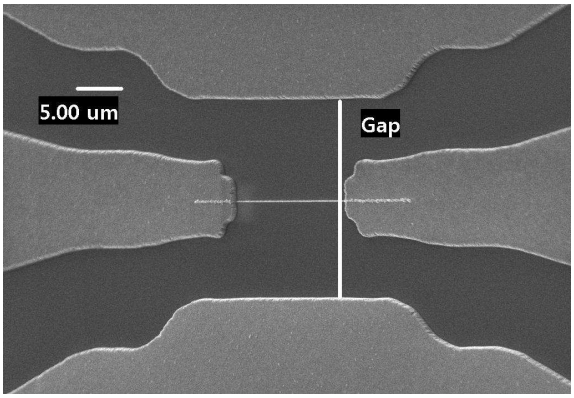


Figure 3.1 SEM image of a nano-size Al wire embedded in a CPW structure

Table 3.1 Geometric parameters of the lines in CPW configuration. The gap distance is 20 µm.

Sample No.	Linewidth (µm)	Thickness (nm)
1	1	50
2	0.5	100
3	0.1	100
4	8	500

To define the CPW structure, standard lithography was applied using AZ5412E as resist (1.3 µm thick), followed by evaporation of a 500 nm thick Al layer (deposition rate: 2 nm/s) and lift-off process. It should be mentioned that Al layer is much thicker than that of sample Nos.1-3. It is to avoid RF probes penetrating through the structure during the measurement. In

addition, before the Al deposition, the samples were treated with 25 second of argon bombardment. It is to clean the surface and remove the oxide layer. The size of the whole CPW structure depends on the length of the line (*l*). To ensure a fair assessment, five different lengths were chosen for evaluation (*l* = 17, 42, 92, 192 and 492 µm). A part of the signal pad with 100 µm in length was designed to be a tapered shape as shown in Figure 3.1. The distance between the two ground planes (gap) is fixed at 20 µm. Figure 3.2 shows a scanning electron microscopy (SEM) image of sample No.3 connected to the pad. It is worthy to mention that the nanostructure obtained by this approach is polycrystalline and has a rough surface, as can be seen in Figure 3.3. The devices for de-embedding were fabricated at the same time. Figure 3.4 shows the thru de-embedding device which will be used extensively in this chapter.

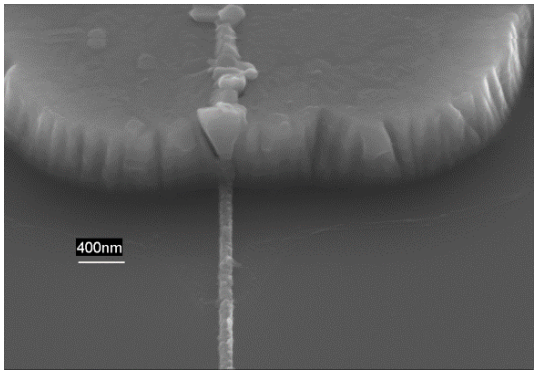


Figure 3.2 Contact between the nano-size wire and the pad

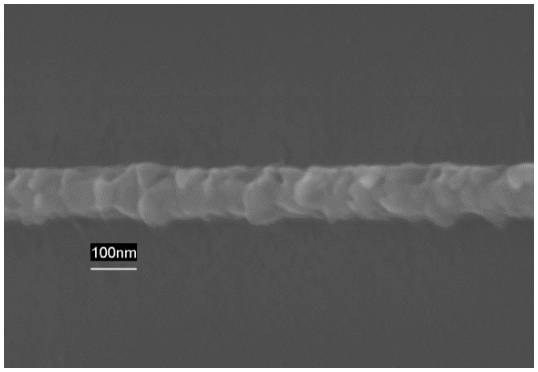


Figure 3.3 Top view of the Al wire

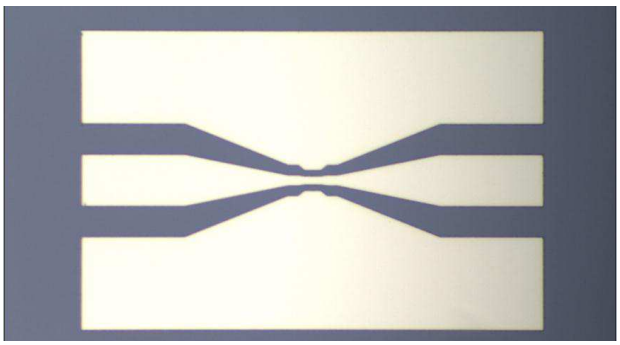


Figure 3.4 Thru de-embedding test structure

3.1.2. Scattering Parameters Measurement

The procedure for the *S*-parameters measurement is similar to what has been described in Section 2.2.2, but here the test frequency is from 1 to 100 GHz. Figure 3.5 demonstrates the top view while probing on the CPW structure.

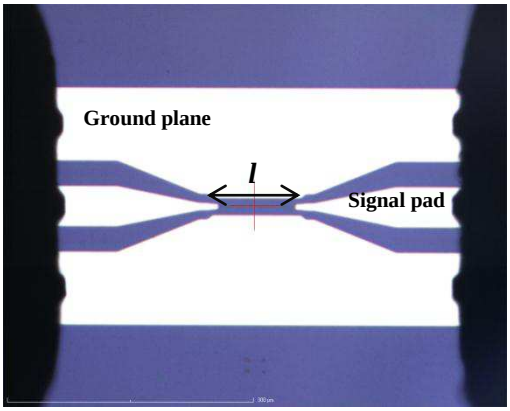


Figure 3.5 Complete test device with GSG probes

3.1.3. Simulation Based on Quasi-TEM Model

In the literature, the transmission properties of metallic CNTs are described based on the Luttinger liquid theory, in which, an additional kinetic inductance L_K and a quantum capacitance C_Q are introduced to account the effect of quantum transport. Since quantum effects have never been experimentally observed in metallic wires, a classical transmission line theory will be applied without invoking new concept as a first approach. A conventional CPW on a dielectric substrate with a centered strip conductor and two infinite ground planes at the sides supports a quasi-TEM mode propagation [73]. As mentioned in Chapter 2, a traditional transmission line can be described by a RLGC model. In common practical cases, CPW is designed on top of multiple dielectric layers therefore has more complicated lumped-elements expressions in the transmission line theory. To account the physical parameters related to the fabrication processes while still satisfying a quasi-TEM mode, a general circuit representation is used, as shown in Figure 3.6

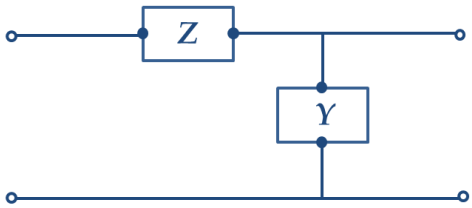


Figure 3.6 Equivalent quasi-TEM circuit model for the intrinsic CPW device

where Z is the total impedance per unit length of the longitudinal circuit and Y is the total shunt admittance per unit length. The relationship between the distributed circuit components and the transmission line parameters can be expressed as follows:

$$\gamma = \sqrt{Z \cdot Y} \qquad Zc = \sqrt{\frac{Z}{Y}} \tag{3-1}$$

The frequency dependent Z and Y are obtained using close-form approximation and ADS Momentum simulation, respectively. This method is simple and computationally efficient but valid only for quasi-TEM mode analysis.

Model Elements Evaluation with Close-Form Approximation

The total series impedance is given by:

$$Z = R \cdot + j \cdot \omega \cdot L \tag{3-2}$$

where R is the conductor loss per unit length and L is the inductance per unit length. R and L in relation to the physical parameters of the CPW devices can be estimated by the close-form formulas found in [74]. Their variations as a function of frequency are also covered in the description. While the close-form expression is known to be quite accurate up to the millimeter wave frequencies for modern monolithic microwave integrated circuit (MMIC) coplanar lines, it is limited to devices with a single-layer substrate [73]. For CPW devices with multilayer dielectrics, such as in our case, it is more difficult to obtain a simple expression of circuit component for the substrate (Y).

Model Elements Evaluation with Simulation Tool

A complementary simulation based on full-wave electromagnetic modelling using ADS Momentum was implemented to estimate the shunt component Y. In ADS Momentum, CPW structures can be simulated as two coupled slot lines (representing the distance between the ground planes and the signal line) as can be seen in Figure 3.7. Coplanar mode was selected for signal excitation at either side of the slot lines. Notice that the RF pads were omitted from the simulation. Using the simulated S-parameters, Zc and γ can be derived. Next, using Equation (3-1), we can obtain Y. The simulated Z, on the other hand, is not valid for this application due to the fact that the signal line can only be considered as a perfect conductor in the simulation setup. The estimated Z from the close-form approximation is more realistic to describe the designed CPW devices than the one simulated here.

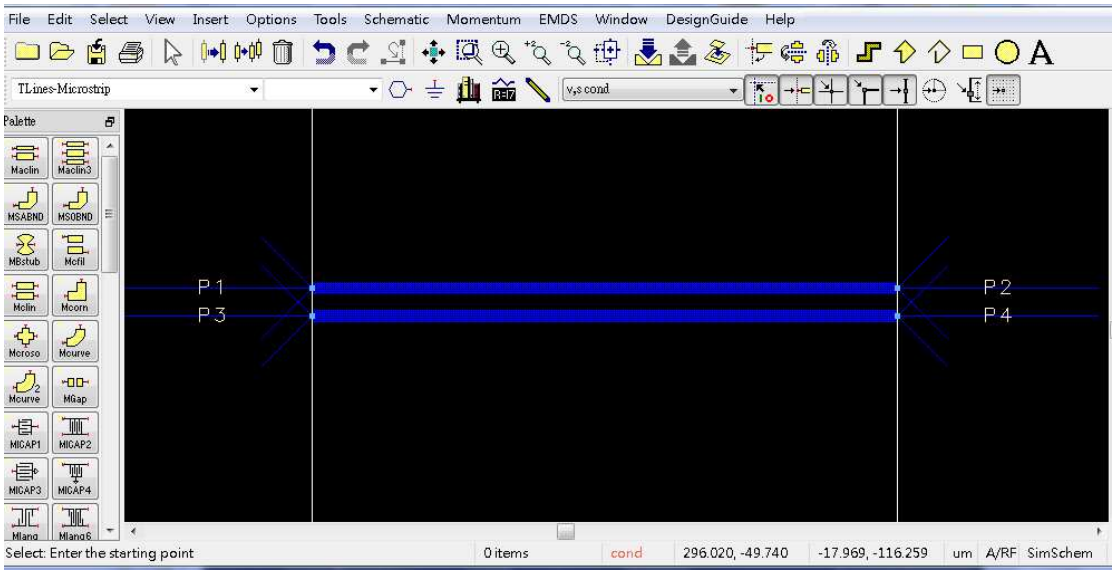


Figure 3.7 ADS Momentum interface showing the simulation setup of a CPW structure

3.1.4. Parasitics Subtraction

Pad Parasitics Subtraction

The "thru-only de-embedding" method was applied in this study to remove the effect of the pads. It only requires a thru test structure [75]. This method belongs to a cascade-based technique. A thru test structure can be represented by two identical two-port networks in series, as shown in Figure 3.8.



Figure 3.8 Two port network of the thru de-embedding test structure

Their *S*-parameters can be derived from

$$S_{11p} = S_{22p} = \frac{S_{11t} + S_{22t}}{2 + S_{21t} + S_{12t}} \tag{3-3}$$

$$S_{12p} = S_{21p} = \sqrt{\frac{1}{2} \cdot (S_{12t} + S_{21t}) \cdot \left(1 - {S_{11p}}^2\right)} \tag{3-4}$$

where S_{xxt} denotes the measured *S*-parameters of the thru pattern and S_{xxp} denotes the *S*-parameters of the pad. The de-embedding is performed by converting the *S*-parameters into an *ABCD*-matrix and then followed by a matrix operation as

$$T_{dut} = {T_p}^{-1} \cdot T_m \cdot {T_p}^{-1} \tag{3-5}$$

where T_p is the *ABCD*-matrix of the input and output pad and T_m is the measured *ABCD*-matrix of the CPW device. T_{dut} is the *ABCD*-matrix after de-embedding which can be also converted to *S*-parameters. Finally, the transmission line parameters, characteristic impedance *Zc* and propagation constant γ are evaluated using the formulas described in Section 2.2.3. Such de-embedding procedure is directly applied on sample No.4. Since the line was made in a single step with the CPW structure, there is no need to address the contact impedance.

Contact Impedance Removal

In the case of Sample Nos.1-3, the contact between the line and the pad is not perfect. It is necessary to characterize contact impedance for obtaining the intrinsic response of the device.

1) Low-Frequency Impedance Measurement

To identify the contact impedance, the electrical conductance of the CPW devices was examined at lower frequencies. The impedance measurement was performed using an Agilent 4284A LCR Meter. The frequency sweep was set from 4 kHz to 1 MHz. The offset, DC bias current and DC bias voltage were set to zero and the amplitude level of the oscillated input voltage was 1 mV. The measurement was carried out with Karl-Suss PM5 wafer probe station. The probes were also provided by Karl-Suss (single tip, PH120 Precision Probe Manipulator).

Two probes were placed separately on the signal input and output pad to measure mean current crossing the wire. 50 data points were acquired per sweep. Before the measurement, open-short calibration technique was employed. The impedance of the device was obtained automatically in a form of resistance and reactance. In such frequency range, it can be expected that there is no wave propagation inside those CPW devices with l = 17 µm. Hence, the line can be assumed as a pure resistor. An equivalent circuit model was suggested to estimate the impedance of the device, shown in Figure 3.9. Such model has a physical basis and is consistent with those proposed by other authors [26] [76]. The impedance of the circuit model can be simulated in ADS from Agilent. Not knowing the resistance of the wire, the bulk Al conductivity, 3.77×10^7 S/m was used for an initial estimation. In addition, the contact impedance was assumed to be identical at the two sides of the wire which is the case when a perfect alignment is achieved.

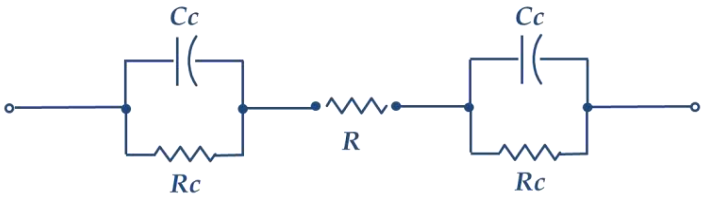


Figure 3.9 Circuit model of the CPW devices at low frequencies

2) Evaluation of Contact Impedance Using Circuit Modelling

Figure 3.10 shows the measured and simulated results for two representative devices, sample Nos.2 and 3 with l = 17 µm. A good agreement is obtained by fitting a constant value for *Rc* and *Cc* in both devices across the entire frequency range. In the case of sample No.2, *Rc* is 4.3 MΩ and *Cc* is 199.84 fF whereas for sample No.3, *Rc* is 29.3 MΩ and *Cc* is 106.9 fF. The assumed metal losses of the wires are 9 and 45 Ω for sample Nos.2 and 3, respectively. Such values have negligible contribution in the model. In fact, during the fitting process, it can be noticed that the variation of *R* has no effect on the overall impedance in this frequency range and the resulting impedance is primarily dominated by *Rc* and *Cc*. Most importantly, *Rc* is considerably large, suggesting that there is a dielectric component at the contact between the line and the pad. This could be attributed to the remaining native aluminium oxide layer formed on the surface of the Al wire before the fabrication of the CPW structure. It is possible that the argon treatment is not sufficient. The fit value of sample No.3 demonstrates a smaller capacitance and a higher loss at the contact than that of sample No.2. This can be understood physically since the contact surface area between the sample No.3 and the pad is about five times smaller.

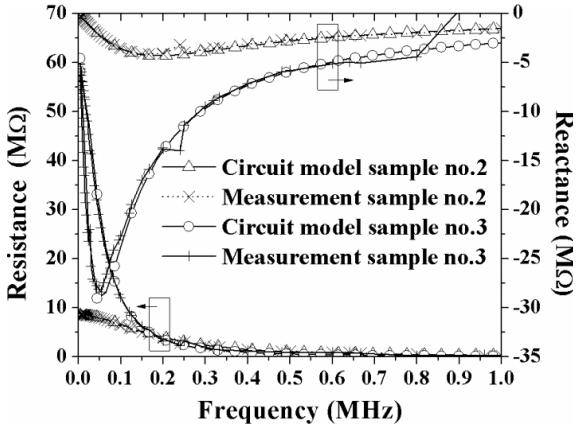


Figure 3.10 Measured and simulated impedance of the CPW devices with l = 17 µm at low frequencies

3) Subtraction of Contact Impedance

Having obtained the circuit elements of the contact, we can proceed to extract the intrinsic properties of the CPW devices at high frequencies. The new de-embedding scheme based on the cascade configuration is modified, as shown in Figure 3.11

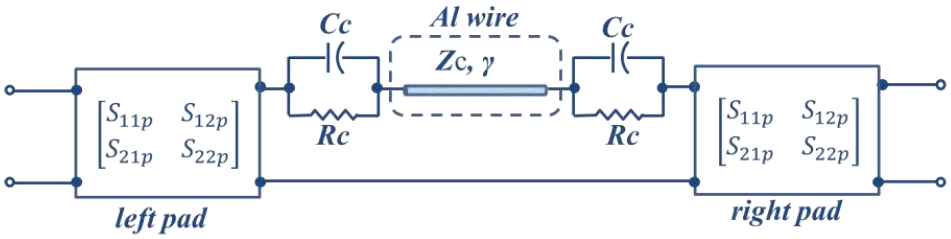


Figure 3.11 Parasitic circuit model of the CPW device

The contact impedance can be included in the two-port network by using an *ABCD*-matrix as

$$T_c = \begin{bmatrix} 1 & \dfrac{Rc}{1 + j \cdot \omega \cdot Rc \cdot Cc} \\ 0 & 1 \end{bmatrix} \tag{3-6}$$

where ω is the angular frequency. *Rc* and *Cc* are taken from the low frequency measurement and modelling. Then, to subtract the pads and the contacts, we perform the next matrix operation:

$$T_{dut} = {T_c}^{-1} \cdot {T_p}^{-1} \cdot T_m \cdot {T_p}^{-1} \cdot {T_c}^{-1} \tag{3-7}$$

T_{dut} represents the intrinsic performance of the CPW device in *ABCD*-matrix. Finally, it is converted to *S*-parameters and the transmission line parameters, *Zc* and γ can be calculated [68].

4) Validation at High Frequencies

To confirm whether the extraction method of contact impedance remains valid at high frequencies, the *S*-parameters of a simulated intrinsic device (calculated using the quasi-TEM model described in Section 3.1.3) with addition of the contact impedance obtained from the low-frequency measurement at both sides of the line were compared to the measured *S*-parameters up 100 GHz de-embedded by the thru without contact impedance subtraction. The above *S*-parameters can be derived using

$$T_1 = T_c \cdot T_{simu} \cdot T_c \tag{3-8}$$

$$T_2 = {T_p}^{-1} \cdot T_m \cdot {T_p}^{-1} \tag{3-9}$$

where T_p is the *ABCD*-matrix of the input and output pad, T_c is *ABCD*-matrix of the estimated contact impedance and T_m is the measured *ABCD*-matrix of the CPW device. T_1 and T_2 are then converted to *S*-parameters. If these two *S*-parameters are similar to each other, it implies that *Rc* and *Cc* determined at low frequencies (from 4 kHz up to 1 MHz) remain applicable at high frequencies (from 1 GHz up to 100 GHz). As an example, Figure 3.12 and Figure 3.13 show the comparison of the derived *S*-parameters for the case of sample No.2 with l = 192 µm. The quasi-TEM model without addition of contact impedance is also included for comparison. It can be observed that the theoretical results are in a very good agreement with experimental

data when RcCc model has been taken into account, particularly at lower frequency region. This indicates that this circuit model describes adequately the contact impedance. Furthermore, as there is no significant difference above 70 GHz between the quasi-TEM model datasets with and without RcCc model (less than 5% in the magnitude of S_{11} and S_{21}), it infers that the effect of contact impedance can be ignored when the frequency is sufficiently high.

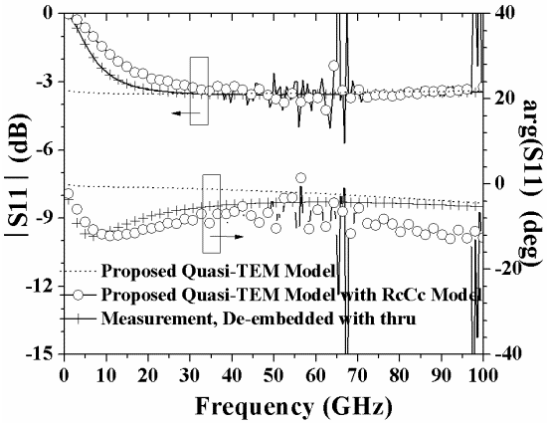


Figure 3.12 Comparison of S_{11} for sample No.2, l = 192 µm

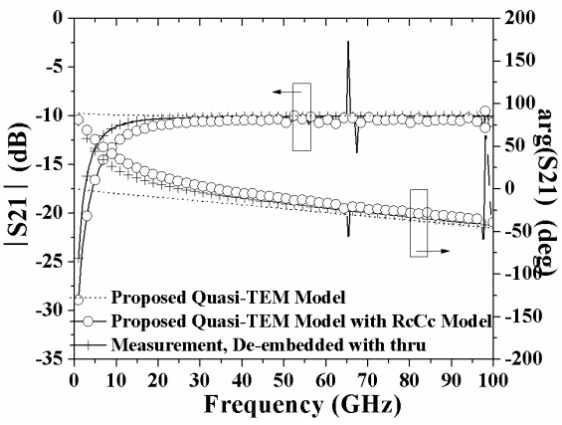


Figure 3.13 Comparison of S_{21} for sample No.2, l = 192 µm

3.1.5. Results and Discussion

The results are examined as follows. First, the raw measurement (calibrated) as well as de-embedded data will be shown, illustrating the impact of parasitics subtraction. The extracted transmission line parameters in relation to different line geometries will be presented. Simultaneously, the level of credibility of the extracted characteristics will be discussed in detail. In addition, several factors are identified that could influence the accuracy of the de-embedded data.

De-embedded *S*-parameters

Figure 3.14 to Figure 3.17 show the magnitude and phase of the experimental S_{11} and S_{21} from sample No.3 with different lengths obtained using the modified de-embedding technique. Sample No.3 was chosen for examination since it has the smallest cross-sectional area among all the samples (the thickness and the linewidth closer to 100 nm). It can be found that the magnitude of S_{11} tends to be closer to zero as the length of the line increases. The responses are very similar between those devices with the wire length above 92 µm. The retum loss is less than -2 dB (at least 80% of the incident power is reflected to the source). The reflection is nearly like an open device. On the other hand, S_{21} shows obvious dependence on the length of the nano-line. Insertion loss (insertion loss is defined as $-20\log_{10}|S_{21}|$) rises with the increase of the length but is slightly reduced with increasing frequency. More than a 30 dB insertion loss is observed when the line length reaches 492 µm. That is less than 3% of the incident power is transmitted through the line. S_{21} exhibits a series capacitive component probably because the contact impedance is under-de-embedded, leaving a residual capacitance.

One can notice noise in the vicinity of 65 GHz. The sources of error are likely due to drift of the calibration and the poor probe to pad contact. The significant degradation of signal to noise ratio is a result of the nature of the measurement system. Our broadband VNA combines the 40 MHz to 65 GHz output from a stand-alone VNA and the 65 GHz to 110 GHz output from a millimeter-wave module. There is increasing power loss due to the cable

assemblies when operating the stand-alone VNA closer to 65 GHz. In addition, the cut-off frequency of the waveguide in the millimeter-wave module is around 70 GHz. To obtain a clearer signal trace, it is often necessary to re-calibrate the VNA to improve the signal to noise ratio.

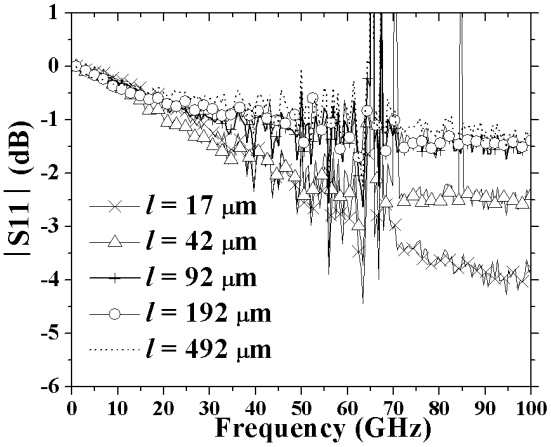


Figure 3.14 De-embedded S_{11} magnitude from sample No.3

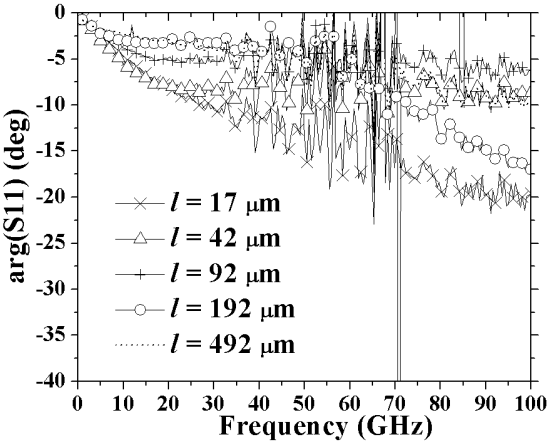


Figure 3.15 De-embedded S_{11} phase from sample No.3

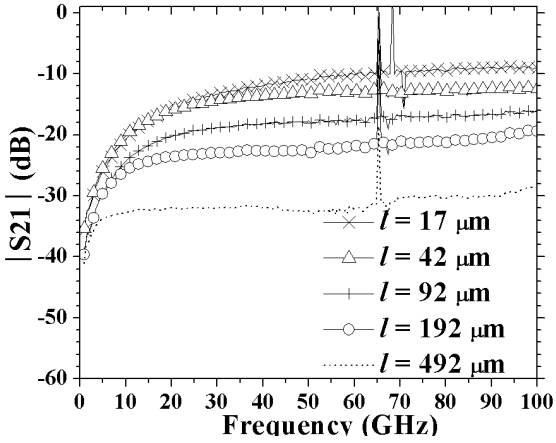


Figure 3.16 De-embedded S_{21} magnitude from sample No.3

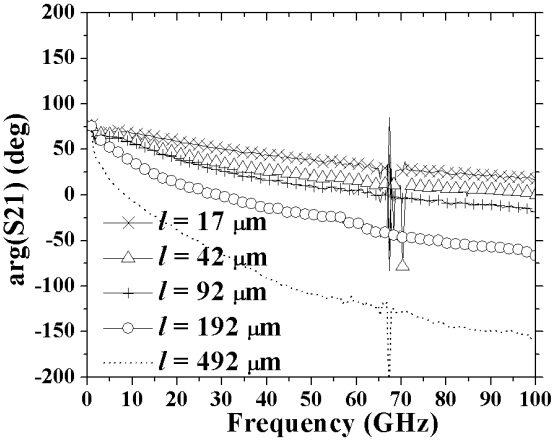


Figure 3.17 De-embedded S_{21} phase from sample No.3

Figure 3.18 to Figure 3.23 show the comparison of the experimental S_{11} and S_{21} from sample Nos.1 to 3 with l = 192 µm based on difference levels of parasitic subtraction. Three datasets are compared: raw *S*-parameters without de-embedding (calibrated), *S*-parameters de-embedded with a thru and *S*-parameters first de-embedded with a thru and followed by subtraction of contact impedance. It can be observed that the pads contribute significantly to the transmission and their loss is not negligible. In the case of sample Nos.1 and 2, an offset of signal level in magnitude for both S_{11} and S_{21} below 40 GHz can be seen after the subtraction of contact impedance. The correction however, is not so much noticeable for sample No.3. The simple fact is that the extracted contact impedance based on a circuit model and low frequency ac measurement will present certain level of errors which inevitably leads parasitic residues.

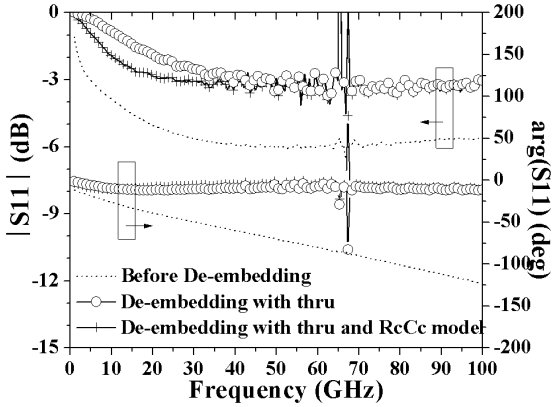


Figure 3.18 Comparison of S_{11} for sample No.1, l = 192 µm

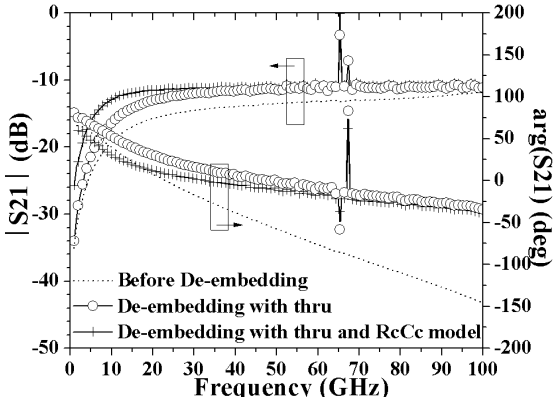


Figure 3.19 Comparison of S_{21} for sample No.1, l = 192 µm

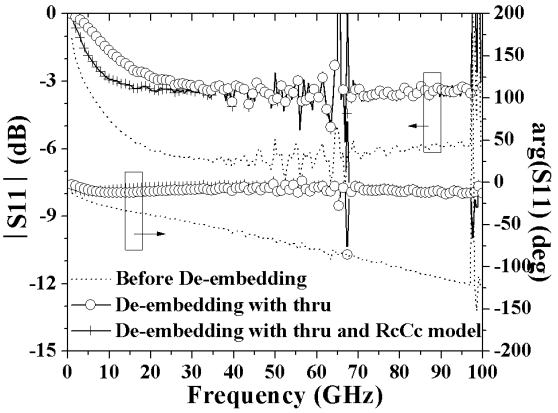


Figure 3.20 Comparison of S_{11} for sample No.2, l = 192 µm

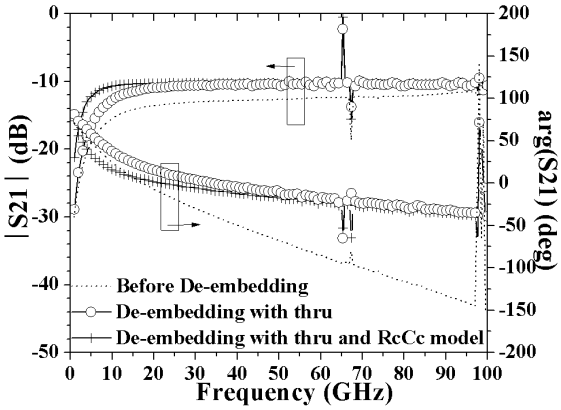


Figure 3.21 Comparison of S_{21} for sample No.2, l = 192 µm

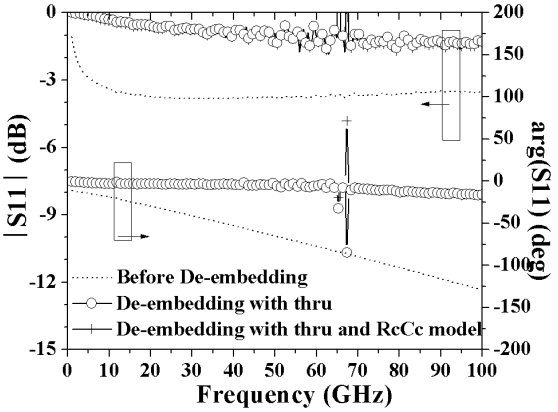


Figure 3.22 Comparison of S_{11} for sample No.3, l = 192 µm

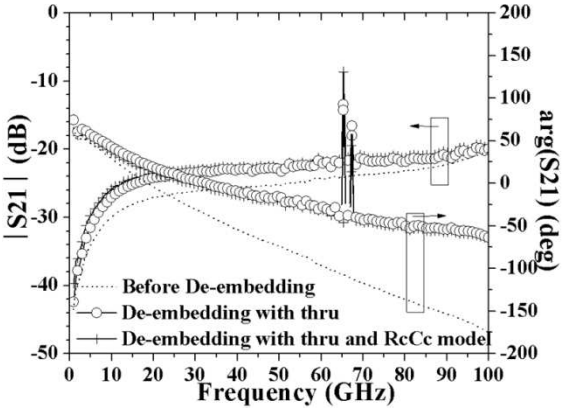


Figure 3.23 Comparison of S_{21} for sample No.3, l = 192 µm

Extracted Transmission Line Characteristics

With the proposed calculation approach, it is possible to calculate the characteristic impedance (Zc) and propagation constant (γ) of the samples using the corresponding line geometry and physical parameters.

Figure 3.24 to Figure 3.31 show the frequency dependence of Re(Zc), Im(Zc), α and β of the intrinsic CPW devices. The simulated and measured results are compared. Each type of

sample has three sets of extracted experimental data from different line lengths (l = 92, 192 and 492 μm), ensuring a more reliable assessment. It should be mentioned that the datasets of l = 17 and 42 μm are too noisy to be presented. The simulated results are shown in solid line. It can be observed that sample No.4, having a relatively large linewidth and thickness, exhibits reasonably well-matched characteristic impedance and attenuation below 5 dB/mm at the maximum frequency, as seen in Figure 3.24 and Figure 3.25. The model agrees sufficiently well with the experimental data, indicating that the thru-only method is appropriate for subtracting pad parasitics. The bulk Al conductivity, 3.77×10^7 S/m was used in the calculation. One can see that the imaginary characteristic impedances of the datasets diverge slightly from each other at high frequencies, probably resulted from the error produced by the de-embedding method. l = 492 μm exhibits the largest offset of 9 Ω at 90 GHz compared to the theoretical value. It is known that the error is a function of the DUT size since the reference plane is established at the center of the thru test structure [75].

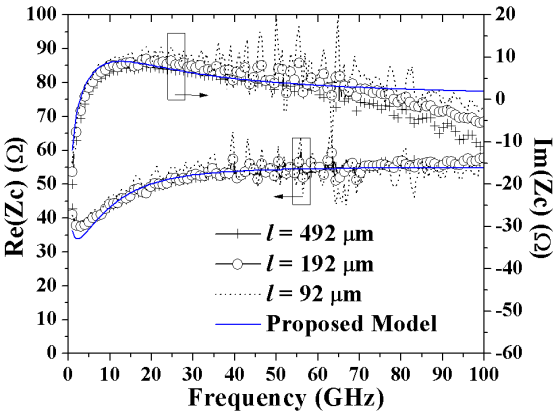


Figure 3.24 Measured and simulated *Zc* of sample No.4

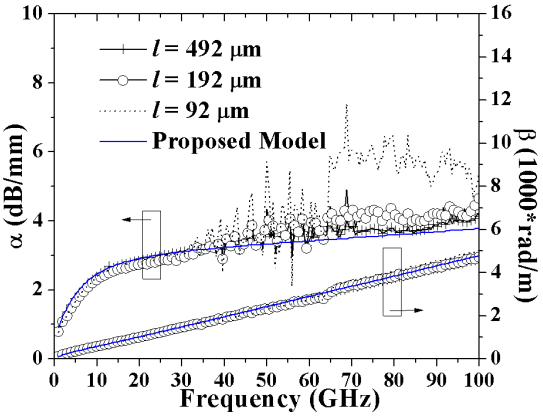


Figure 3.25 Measured and simulated γ of sample No.4

The measured characteristic impedances of sample Nos.1 and 2 decay gradually with increasing frequencies. The same trend is found in the model, as shown Figure 3.26 and Figure 3.28. In the close-form formulas, while calculating R and L, the Al conductivity was intentionally decreased to 1.6×10^7 S/m to meet the extra conductor losses observed in the measurement. In this way, the model gives the best fit in the propagation constant as well as the characteristic impedance. The comparison of the imaginary Zc shows obvious inconsistency between the datasets in the low frequency region. Take sample No.1 for example, the Im(Zc) of l = 92 μm is two times more than that of l = 492 μm at 15 GHz. Based on the analysis from the previous section, this type of error present at low frequencies is most likely due to contact impedance residue. For the same reason, we can also observe in Figure 3.27 and Figure 3.29, an apparent divergence in α below 30 GHz. Despite the mismatch, overall trend in relation to the frequency can be identified at the mid and high frequency range. These two samples have similar transmission line properties as their cross-sectional areas are the same. The attenuation rises with increasing frequency and reaches 30 dB/mm at 100 GHz.

At high frequencies, one can notice that certain dataset shows less agreement with the theoretical value. The source of error is probably due to poor probe-to pad-contact. Table 3.2 summarizes the discrepancy between the simulation results and measurement for sample No.2. In the case of sample No.2, for a single frequency, f = 90 GHz, the difference between datasets can reach 19% for α and 8% for β when l = 492 μm and 192 μm are chosen for comparison. Although it is less noticeable visually, it should be mentioned that the difference

for Re(*Zc*) and Im(*Zc*) is 14% and 11%. Meanwhile, l = 492 µm demonstrates the best agreement with the model having less than 5% error in α, β and Re(*Zc*). This corresponds with the sensitivity analysis in Chapter 2. Transmission lines with longer lengths are less susceptible to parasitic residue, hence yielding more precise result. Nevertheless, the prediction for the imaginary impedance is less satisfactory; the discrepancy reaches as much as 35%. The accuracy and the repeatability of the measurement in general can be improved by re-probing or frequent cleaning of probe tips.

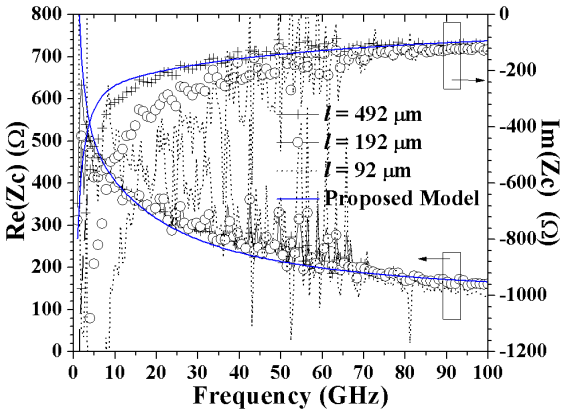


Figure 3.26 Measured and simulated *Zc* of sample No.1

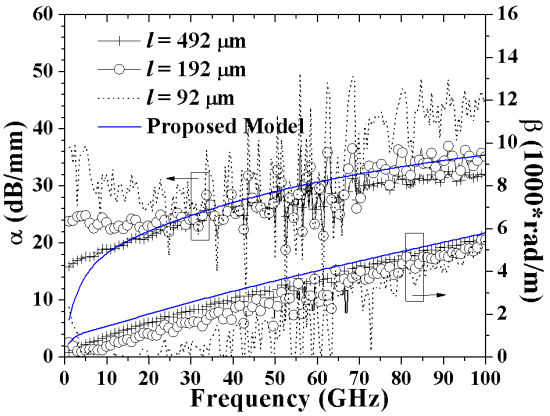


Figure 3.27 Measured and simulated γ of sample No.1

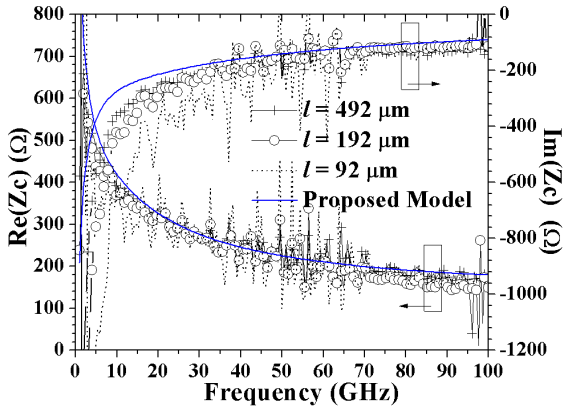


Figure 3.28 Measured and simulated *Zc* of sample No.2

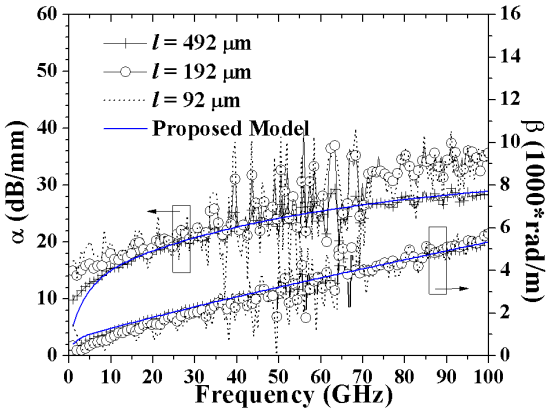


Figure 3.29 Measured and simulated γ of sample No.2

Table 3.2 Discrepancy between simulation results and measurements for sample No.2. The variation of α is estimated as $\frac{\alpha_{mea}-\alpha_{simu}}{\alpha_{simu}}$. The other parameters are calculated in the same manner.

% variation	30 (GHz)				60 (GHz)				90 (GHz)			
	Re(Zc)	Im(Zc)	α	β	Re(Zc)	Im(Zc)	α	β	Re(Zc)	Im(Zc)	α	β
l = 92 µm	-7.0	60.2	6.6	-17.1	-13.6	49.2	-0.3	3.5	-10.6	33.4	16.7	-9.2
l = 192 µm	-4.5	20.7	6.9	-10.7	-8.5	15.7	7.8	0.6	-18.3	19.9	21.6	-1.9
l = 492 µm	-1.8	15.6	-1.1	-2.0	3.0	24.9	-4.3	0.1	-5.3	35.4	-1.2	-3.2

In the case of sample No.3 with both linewidth and thickness close to 100 nm, the absolute characteristic impedance goes down to 450 Ω at 100 GHz. Similarly, it can be seen that in Figure 3.30 and Figure 3.31, there is a discrepancy between the experimental and simulated Im(*Zc*) and α with inconsistency between datasets below 30 GHz. Notice that l = 492 µm has a rather ambiguous α and β at high frequencies compared to the other datasets.

The excessive losses in this line result in a very small transmission signal, making it difficult to extract an accurate attenuation constant. A more detailed analysis of this phenomenon will be delivered in Section 3.2.5. Considering the other two devices with shorter lengths, the percentage difference between them in α and β is less than 5% at 90 GHz. One can observe that the attenuation becomes considerably large over the whole frequencies, reaching 80 dB/mm at 100 GHz. It is interesting to note that the phase constant β is higher than the other sample types, indicating that there is slower wave propagation in this structure. Meanwhile, α is underestimated by the model over the whole bandwidth. Disagreement can also be seen in β in the high-frequency region. The discrepancy between the measured and simulated α is 25% and 18% for β at 90 GHz when l = 192 μm is chosen. The slow wave propagation phenomena was described in [77] for the general lossy transmission line case. The author derived the transmission parameters in the complex plane and found that the phase velocity in a lossy transmission line is always less or equal to that in the ideal case. Important or not, the physical effects associated to general losses are always covered in the conventional transmission line theory. The discrepancy between the theoretical and actual value could suggest two things: 100 nm is a critical dimension. The conductivity drops considerably lower than to 1.6×10^7 S/m or there is new concept associated with quantum effects that should be considered. Such observation will be elaborated further in Section 3.2 by using the new test structures.

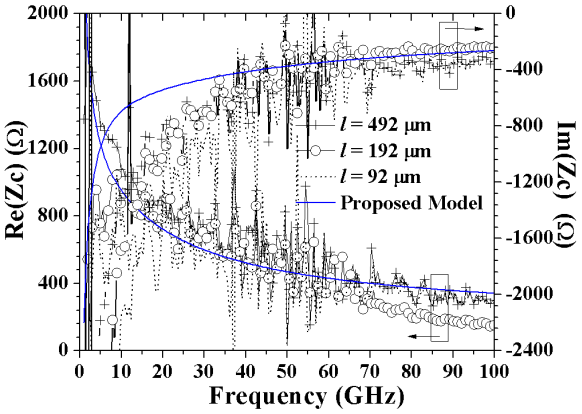


Figure 3.30 Measured and simulated *Zc* of sample No.3

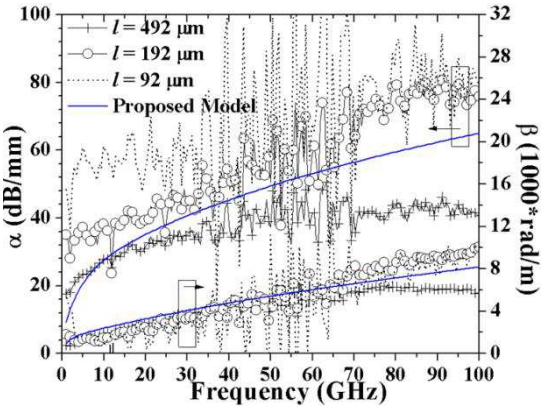


Figure 3.31 Measured and simulated γ of sample No.3

Impact of Misalignment on Extracted Parameters

Let us discuss the level of uncertainty that can possibly degrade the accuracy in this de-embedding procedure. The apparent difference between the experimental results below 30 GHz could be due to the error in the estimated contact impedance. The assumption that the contact impedances at both sides are identical could potentially introduce errors in the extraction since there is always certain degree of misalignment. Figure 3.32 and Figure 3.33 demonstrate the effect of misalignment to the extracted transmission line parameters of sample No.2 with l = 192 μm. In the case of perfect alignment, each contact contributes to 50% of the total impedance in the low frequency measurement. Case 1 assumes that the left contact is responsible for 25% of the total impedance and 75% from the right one. Case 2 is with the reversed order. The corresponding *Rc* and *Cc* can be estimated using the method described in Section 3.1.4. The transmission line parameters for each case can then be obtained. Six data points are selected from each dataset, namely 15, 30, 45, 60, 75 and 90 GHz. The result without contact impedance correction and the developed model are also

included for comparison. The maximum variation between the perfect alignment and the cases of misalignment for both *Zc* and γ is observed at 15 GHz. The percentage difference is less than 5% for Re(*Zc*) at other frequencies. The same applies to Im(*Zc*), except at 15 GHz, a variation up to 10% can be seen for both cases. As for γ, the misalignment can affect the derived result as much as 9% in α and 13% in β at 15 GHz. This readily explains why there was a significant variation in the extracted results between devices from the same design below 30 GHz in the previous section. Such correction, however, is necessary since the accuracy is improved by making the experimental datasets shift closer to the theoretical value.

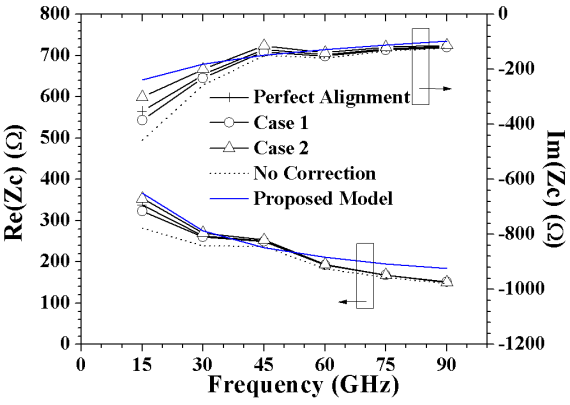


Figure 3.32 Measured and simulated *Zc* of sample No.2 with *l* = 192 µm. Case 1: left contact contributes to 25% of the total contact impedance. Case 2: left contact contributes to 75% of the total contact impedance

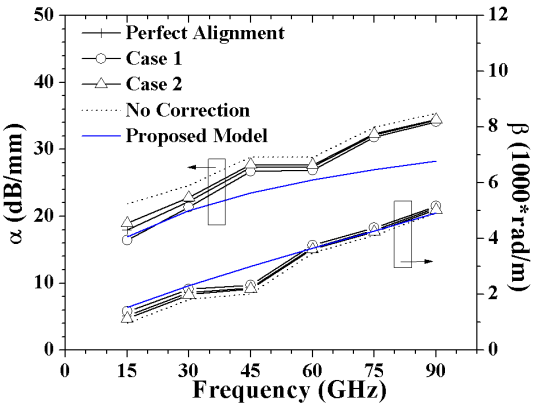


Figure 3.33 Measured and simulated γ of sample No.2 with *l* = 192 µm. Case 1: left contact contributes to 25% of the total contact impedance. Case 2: left contact contributes to 75% of the total contact impedance.

Impact of Signal Pad Coupling on Extraction Parameters

Another important issue worthy to be addressed is the signal pad coupling. Several authors have reported the significance of such effect while characterizing nanoscale devices at high frequencies and therefore it should be subtracted [26] [48] [53]. The length of the nano-devices under test in those studies is typically less than 10 µm. The capacitive coupling between signal pads should naturally be taken into consideration in circuit analysis. Based on the calculation here, the minimum wire length is 92 µm for having a clear transmission line behavior in the frequencies of interest; thereby the coupling effect is initially omitted in the proposed de-embedding procedure. To evaluate the uncertainty caused by such assumption, it is useful to estimate the coupling impedance using the *S*-parameters measurement of an empty CPW device as shown in Figure 3.34.

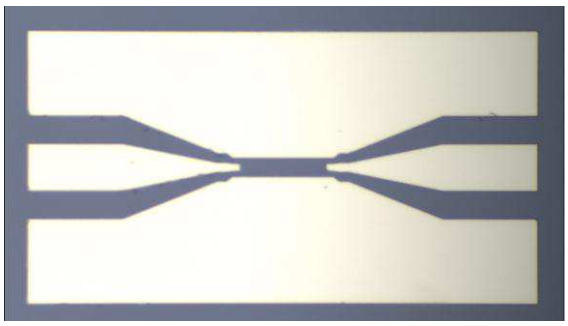


Figure 3.34 Open de-embedding test structure (empty device)

The coupling impedance can be extracted from the following procedures [26] [78]:

$$T^{co} = {T_p}^{-1} \cdot T_{open} \cdot {T_p}^{-1} \tag{3-10}$$

$$Z_{co} = {T_{12}}^{c0} \tag{3-11}$$

T_{open} represents the measured *ABCD*-matrix of the open device T_p is the *ABCD*-matrix of the input and output pad. Z_{co} represents the coupling impedance between signal pads. Figure 3.35 shows the extracted Z_{co} of empty devices with different distances (L2, L3 and L4, each represents l = 92, 192 and 492 µm, respectively). A circuit model is included for analysis to provide a better physical understanding (Figure 3.36). It simply consists of two parallel RC circuits in series, representing the capacitive coupling and corresponding loss within the two different layers, the SiO_2 layer and the silicon substrate. As can be seen in the figure, the extracted coupling reactance, Im(Z_{co}) changes from capacitive to slightly inductive with increasing frequency while the circuit model demonstrates a lossy capacitive pad coupling mechanism in the whole frequency range. The inductive component could suggest that there may be another mode of signal propagation. During the fitting process, it was found that the further the distance between the signal pads is, the smaller the values of C_{ox} and C_{Si} are, meaning a weaker capacitive coupling.

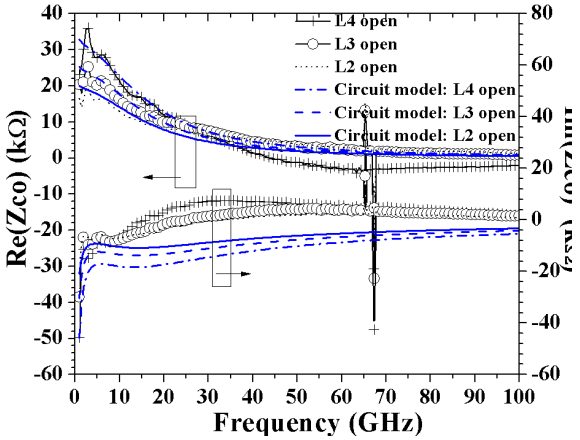


Figure 3.35 Extracted coupling impedance from the open devices. L4 open: open device with l= 492 µm. L3 open: open device with l= 192 µm. L2 open: open device with l= 92 µm.

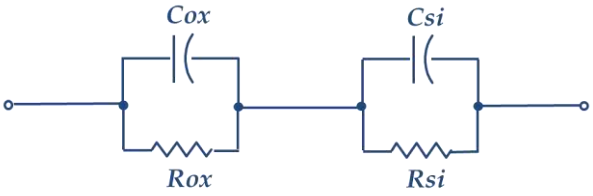


Figure 3.36 Circuit model of the coupling impedance *Zco*

Assuming such coupling exists and remains unchanged when there is a nanowire placed in between the CPW structure, we can subtract it as following:

$$T_{in} = {T_c}^{-1} \cdot {T_p}^{-1} \cdot T_m \cdot {T_p}^{-1} \cdot {T_c}^{-1} \tag{3-12}$$

$$Y_{dut} = Y_{in} - Y_{co} \tag{3-13}$$

Y_{dut} represents the admittance of an intrinsic CPW device. Y_{in} is the admittance of the measurement after subtraction of pads and contact impedances. Finally, Y_{dut} is converted to *S*-

parameters and Zc and γ of the intrinsic device can be obtained. As an example, Figure 3.37 to Figure 3.40 show the transmission line parameters for sample Nos.2 and 3 with l = 192 µm after subtraction, labelled as "De-embedding2". The result without removal of parasitic coupling labelled as "De-embedding1" and the developed model are also shown for comparison. In the plot of α, it can be noticed clearly that the difference between with and without elimination of coupling impedance increases as the frequency increases. After the subtraction, the attenuation increases by 30.7% and 10.0% for sample Nos.3 and 2 at 90 GHz, respectively. As for Re(Zc), Im(Zc) and β, no apparent dependence on the frequency is found in terms of the differences in percentage. The fluctuation of the trace rather reflects the fluctuation in the extracted coupling reactance. According to this result, it is acknowledged that the existence of lossy capacitive coupling between the signal pads. The removal of this coupling parasitic is undoubtedly physically meaningful although in practice, it is difficult to determine the actual value. Above all, the measurement of an open device is very sensitive and prone to calibration errors. At this moment, it is unknown whether the attempt of subtraction improves accuracy or the contrary in this test result. Further examination will be presented in Section 3.2.

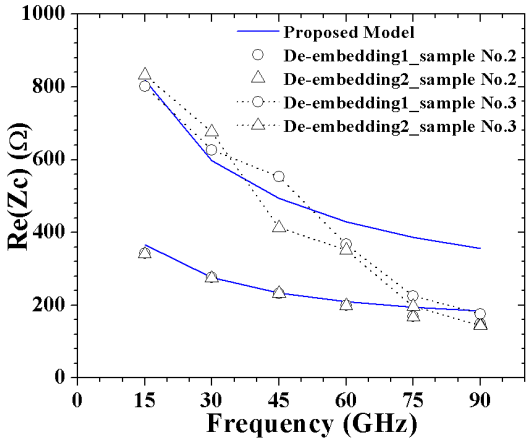


Figure 3.37 Extracted and simulated Re(Zc) of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling.

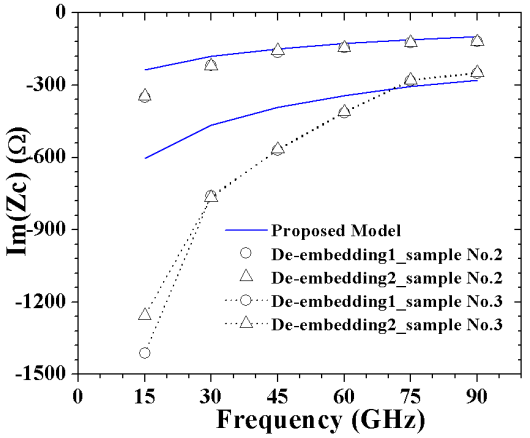


Figure 3.38 Extracted and simulated Im(Zc) of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling.

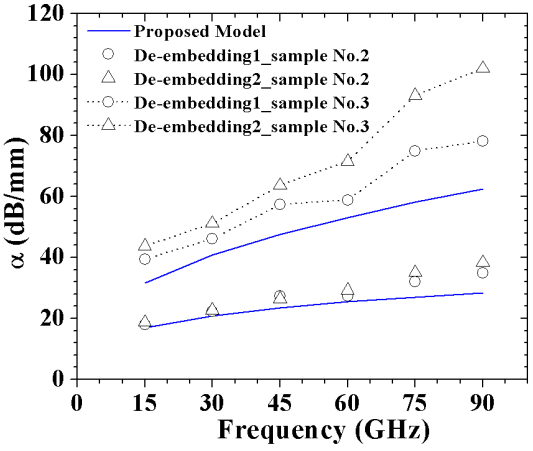


Figure 3.39 Extracted and simulated α of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling.

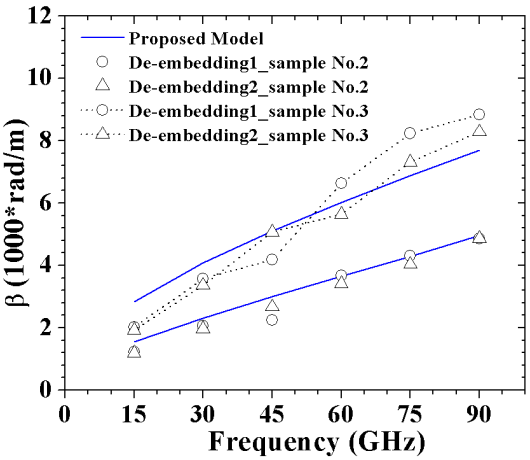


Figure 3.40 Extracted and simulated β of sample No.2 and 3 with l = 192 µm. De-embedding1: first de-embedded with a thru and followed by subtraction of contact impedance. De-embedding2: first de-embedded with a thru, followed by subtraction of contact impedance and parasitic pad coupling

3.1.6. Alternative Extraction of Parasitics

It appears that the accuracy of the extracted parameters is very sensitive to the estimated contact impedance, especially at low frequencies. In the following section, an alternative solution is developed that excludes a direct estimation of the contact impedance.

Methodology

A popular de-embedding technique for transmission lines at mm-wave frequencies is the two line method [54]. This method makes use of two uniform and symmetric transmission lines of the same dimension but with arbitrary length. The intrinsic transmission line properties can be extracted through two-port network de-embedding. The detailed description and derivation will be omitted here but can be found in [54]. Such method assumed that parasitic contribution can be modelled solely by a lumped parallel admittance. In principle, the two line method is also applicable for a lumped series impedance assumption. The proposed solution resembles the one suggested by [54]. However, the thru-only method is added to remove pad parasitic. Assuming the contact impedance is identical for both lines and can be expressed as a series impedance lumped at both sides of the transmission line, it is possible to correct the contact impedance with the two line method. Under this assumption, we obtain:

$$\begin{aligned} T'_{l2} \times T'_{l1} &= T_c \cdot T_{l2} \cdot T_c \times {T_c}^{-1} \cdot {T_{l1}}^{-1} \cdot {T_c}^{-1} \\ &= T_c \cdot T_{l2-l1} \cdot {T_c}^{-1} \\ &= T'_{l2-l1} \end{aligned} \tag{3-14}$$

where $T_{l2\text{-}l1}$ is the *ABCD*-matrix of an intrinsic transmission line of length L2−L1. T_c is *ABCD*-matrix of the contact impedance and T_{l2} and T_{l1} are the measured *ABCD*-matrix of the CPW device with line length being L2 and L1. T'_{l2} and T'_{l1} are the *ABCD*-matrix after de-embedding with a thru. In which, we also have:

$$T_c = \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix}; \text{ and therefore } {T_c}^{-1} = \begin{bmatrix} 1 & -Z_L \\ 0 & 1 \end{bmatrix} \tag{3-15}$$

Z_L represents the series contact impedance. $T'_{l2\text{-}l1}$ can be expressed as a series combination of the intrinsic transmission line and the parasitic contact impedance:

$$Z'_{l2-l1} = Z_{l2-l1} + \begin{bmatrix} Z_L & 0 \\ 0 & -Z_L \end{bmatrix} \tag{3-16}$$

$Z_{l2\text{-}l1}$ represents the *Z*-parameters of the intrinsic impedance. By connecting $Z'_{l2\text{-}l1}$ in series with a port-swapped version of itself, thus cancelling out the effects of the contact impedance:

$$Z_{l2-l1} = \frac{Z'_{l2-l1} + swap(Z'_{l2-l1})}{2} \tag{3-17}$$

Note that $swap\left(\begin{bmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{bmatrix}\right) \equiv \begin{bmatrix} a_{22} & a_{21} \\ a_{12} & a_{11} \end{bmatrix}$. Next, the *Z*-parameters are transformed to *S*-parameters. We can then extract the characteristic impedance (*Zc*) and the propagation constant (γ). Given that $Z_{l2\text{-}l1}$ is symmetric, Z_L can be calculated from:

$$\begin{bmatrix} Z_L & 0 \\ 0 & -Z_L \end{bmatrix} = \frac{Z'_{l2-l1} - swap(Z'_{l2-l1})}{2} \tag{3-18}$$

Contact Impedance Estimation

The experimental results from Sample Nos.1 and 2 will be used for preliminary examination. Their contact impedance can be extracted by the method mentioned above, as shown in Figure 3.41 to Figure 3.44. For each sample type, since there are three sets of measurement from different lengths (L4 = 492 µm, L3 = 192 µm and L2 = 92 µm), the de-embedding can be performed with three combinations (L2-L3 = 100 µm, L3-L4 = 300 µm and L2-L4 = 400 µm). The contact impedances evaluated from Section 3.1.4 based on the low-frequency measurement are included in the datasets to establish a reference point. It can be seen that both the modelled and experimental results reveal a strong capacitive behaviour. The contact resistance derived from the circuit model (Figure 3.9) at this frequency range is negligible whereas the ones extracted from Equation (3-18) shows the contrary. There is an additional resistive component in the contact impedance composition. Ideally, the contact impedances obtained from the three datasets should be not far from each other. The difference between datasets is probably due to the measurement uncertainty. Some even exhibit non-physical negative resistance at high frequencies. If the proposed de-embedding technique is valid, we should be able to accurately reconstruct the *S*-parameter of the original measurement using only the extracted values for *Zc*, *γ*, and Z_L. When plotted next to the raw *S*-parameters of sample No.2 with L3 (Figure 3.45 and Figure 3.46), the *S*-parameters reconstructed using Z_L from L2-L3 differ significantly at mm-wave frequency range. In contrast, the one with L3-L4 is relatively close to the raw measurement. Hence, it is reasonable to say that this negative resistance given by the extracted Z_L is rather an erroneous reading. In addition, it is also possible to see the discrepancy at low frequencies in magnitude between the raw *S*-parameters and those ones reconstructed using Z_L given by low frequency measurement and circuit modelling. This implies that the contact reactance is slightly underestimated by the method derived in Section 3.1.4 which is also readily evident in Figure 3.42 and Figure 3.44.

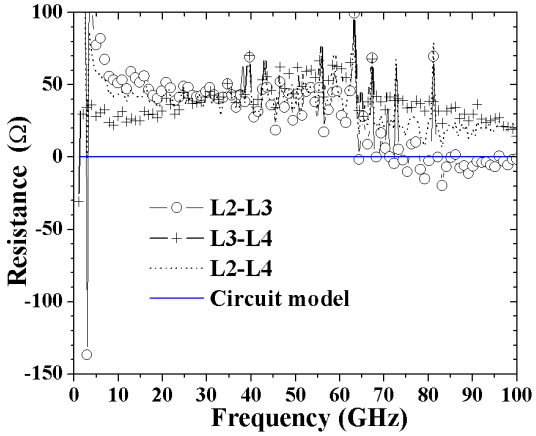


Figure 3.41 Contact resistance estimated from the two line method and the circuit model for sample No.1; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm

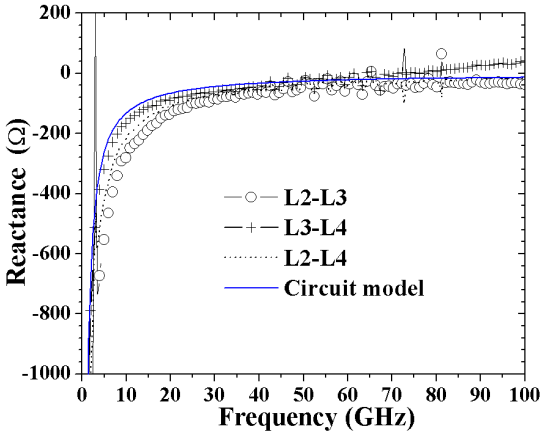


Figure 3.42 Contact reactance estimated from the two line method and the circuit model for sample No.1; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm

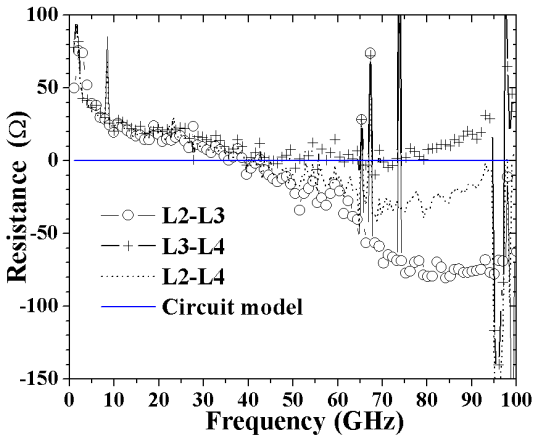


Figure 3.43 Contact resistance estimated from the two line method and the circuit model for sample No.2; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm

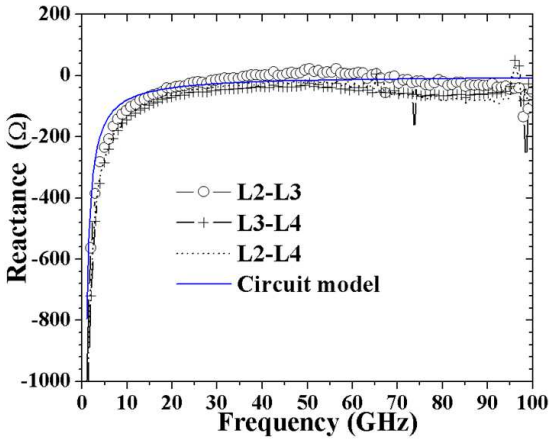


Figure 3.44 Contact reactance estimated from the two line method and the circuit model for sample No.2; where L4 = 492 µm, L3 = 192 µm and L2 = 92 µm

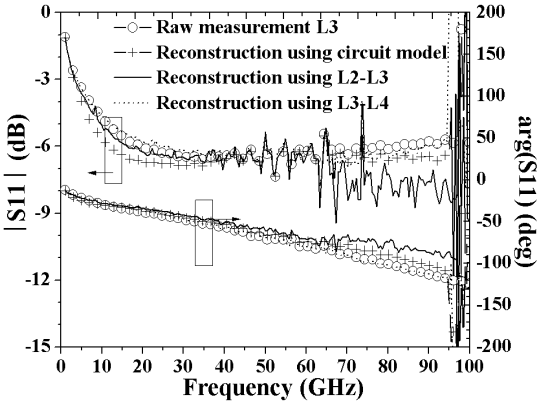


Figure 3.45 Comparison between S_{11} raw data and reconstructed from the two line method using the contact impedance extracted L3-L4 and L2-L3 as well as the directly obtained from circuit model

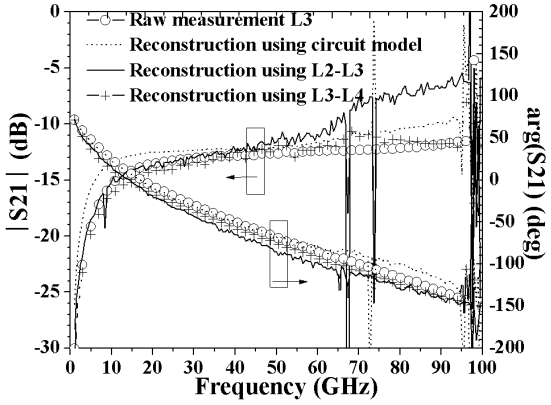


Figure 3.46 Comparison between S_{21} raw data and reconstructed from the two line method using the contact impedance extracted L3-L4 and L2-L3 as well as the directly obtained from circuit model

Parameter Extraction

Figure 3.47 to Figure 3.52 show the frequency dependence of Re(Zc), Im(Zc), α and β of the intrinsic CPW devices de-embedded with the new method. The simulated and measured results are compared. Each type of the sample has three sets of extracted experimental data from different combinations of lines (L2-L3 = 100 µm, L3-L4 = 300 µm and L2-L4 = 400 µm). The simulated results are shown in solid line. One can notice that the traces are much smoother and the variation between datasets is minimized compared to the results we reported previously. It is in fact more likely that these datasets de-embedded with the new method are more accurate. For one, better agreement with the proposed quasi-TEM model observed in the case of sample No.2 gives confidence to the accuracy of this de-embedding procedure. If considering the case of L2-L3, the discrepancy of imaginary characteristic impedance has minimized to 9.3 and 8.4% at 30 and 60 GHz, respectively as opposed to 20.7 and 15.7% as presented in Table 3.2 for the case of l = 192 µm. When examining the results from sample No.1, mismatch between datasets is also noticeable in particular at the lower frequencies. The imaginary characteristic impedance extracted from L2-L3 is underestimated due to over-de-embedding of contact reactance. Note that in Figure 3.42, the derived contact reactance from L2-L3 is higher than the others. The attenuation is lower than the model predicted across the

whole frequencies. It appears that the accuracy of the model deteriorates in this particular case. This issue will further be discussed in Section 3.2. Meanwhile, in the case of sample No.3, the extracted values have significant error, therefore cannot be reliably analysed.

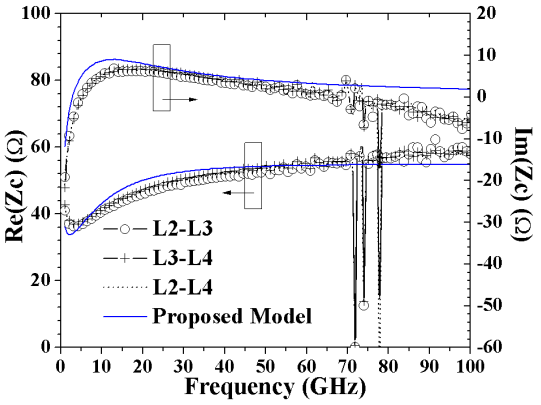


Figure 3.47 Measured and simulated *Zc* of sample No.4

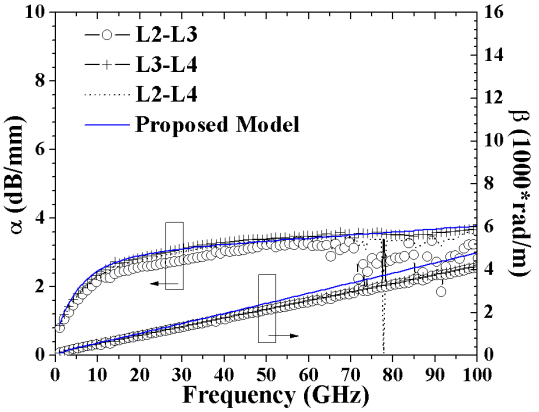


Figure 3.48 Measured and simulated γ of sample No.4

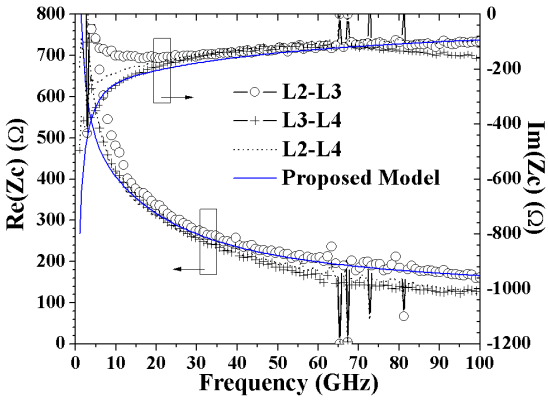


Figure 3.49 Measured and simulated *Zc* of sample No.1

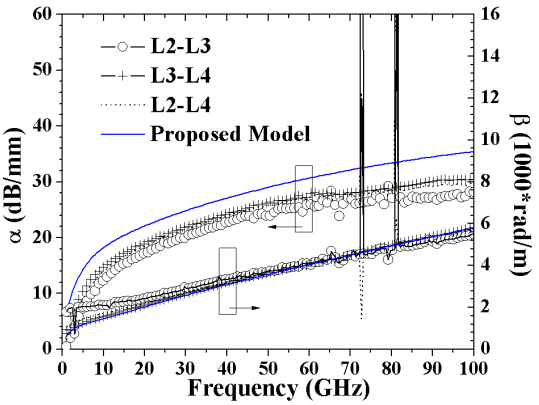


Figure 3.50 Measured and simulated γ of sample No.1

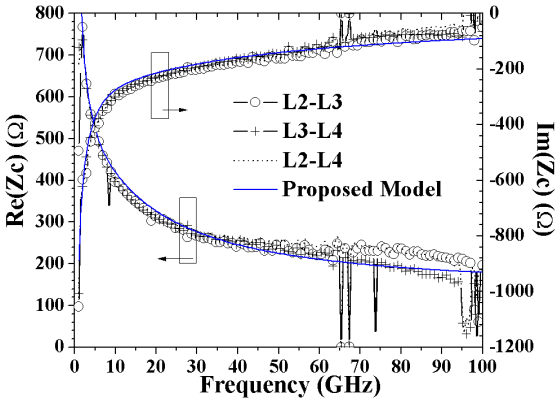


Figure 3.51 Measured and simulated *Zc* of sample No.2

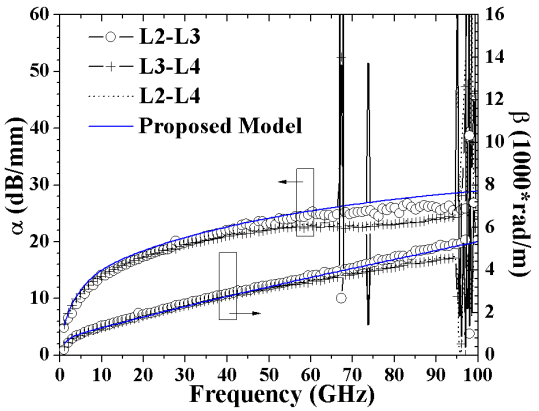


Figure 3.52 Measured and simulated γ of sample No.2

3.2 Single and Multiple Gold Nano-lines

The proposed new de-embedding procedure is much less sensitive to measurement errors and parasitic residues, making it adequate for high-frequency characterization. In the following section, similar tests will be implemented but using gold nanowires. This is to avoid oxidation, thus minimizing the influence of contact impedance. A new CPW structure with a smaller occupied area will first be demonstrated which helps improve the accuracy of measurement. Next, the transmission properties of different device configuration will be investigated, including single and multiple lines devices. The effect of gap size and distance between nanowires will also be studied. The idea of putting several nanowires in parallel is to resolve excessive metal loss due to dimensional scaling. However, parallel combination of nanowires will result in different signal propagation properties, such as decrease in effective inductance. Besides, paralleling nanowires may interact with each other. It is worthwhile to examine how the transmission characteristics of a parallel nanowire system scale with the numbers of wires. At the end of this section, inadequacy of this de-embedding procedure is eventually revealed. It will be shown that de-embedding method should be adapted according to the frequency range to ensure a more accurate interpretation of measurement result.

3.2.1. New Test Structure Design and Fabrication

The fabrication steps are similar to those described in Section 3.1.1. However, gold (Au) was used as the material for the lines instead of aluminium. For better adhesion on the oxide-coated Si substrate, it is necessary to deposit a thin layer of Chromium (Cr) before Au deposition. Table 3.3 summarizes the geometrical parameters of all the devices-under-test (DUT). Some devices include parallel multiple lines in the same signal path. The material for the CPW structures remains aluminium. They were designed either to be compatible with 50 µm-pitch or 100 µm-pitch GSG probes. Two gap distances were chosen: 12 and 20 µm. Figure 3.53 shows two 50 nm wide Au wires embedded in a CPW structure. It can be seen that in Figure 3.54 the signal pads lie over the line, ensuring a sufficient contact area. Compared to Al nanowires, the surface of these Au nanowires is much smoother, as can be observed in Figure 3.55.

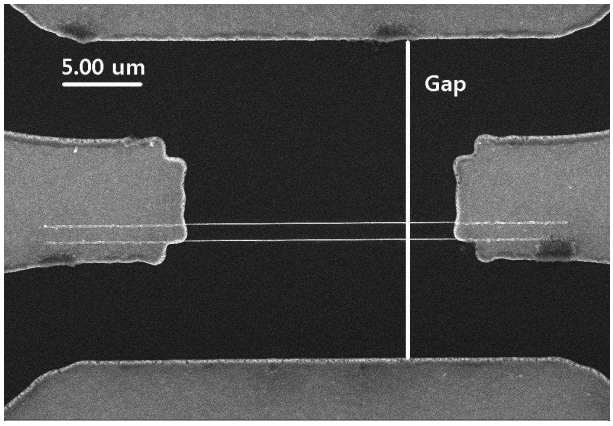


Figure 3.53 SEM image of two parallel nano Au wires embedded in a CPW structure

Table 3.3 Geometric parameters of the gold lines in CPW configuration

Sample No.	Linewidth (μm)	Thickness (μm)	Single/Multiple line	Interline distance (μm)	Gap (μm)
A1	0.1	0.1	X 1		20
A1'	0.1	0.1	X 1		12
A2[a]	0.1	0.1	X 2	0.2	20
A2'[a]	0.1	0.1	X 2	0.2	12
A2[b]	0.1	0.1	X 2	1	20
A5[a]	0.1	0.1	X 5	0.2	20
A5[b]	0.1	0.1	X 5	1	20
B1	0.2	0.1	X 1		20
B1'	0.2	0.1	X 1		12
B2[a]	0.2	0.1	X 2	0.2	20
B2[b]	0.2	0.1	X 2	1	20
B5[a]	0.2	0.1	X 5	0.2	20
B5[b]	0.2	0.1	X 5	1	20
C1	1	0.05	X 1		20
D1	0.1	0.05	X 1		20
E1	0.05	0.05	X 1		20
E2	0.05	0.05	X 2	1	20
F1	8	0.5	X 1		20

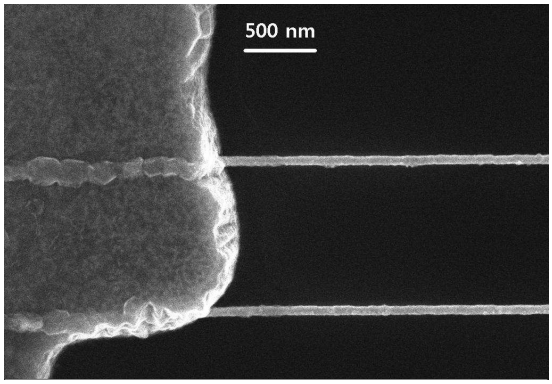


Figure 3.54 Contact between the nano-size wires and the pad

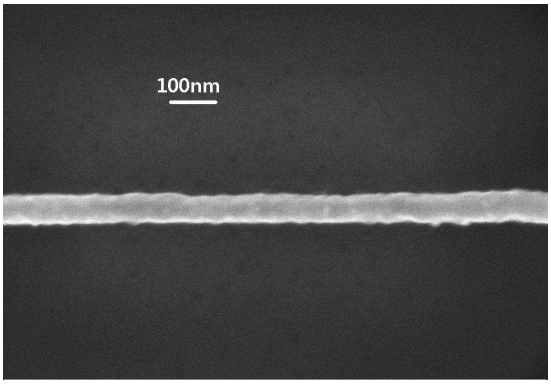


Figure 3.55 Top view of an Au wire

3.2.2. Scattering Parameters Measurement

The experimental setup and the measurement procedure resemble those described in Section 2.2.2, except that the measured frequency ranges from 1 to 110 GHz and the configuration of the GSG probes is for 50 μm-pitch RF pads. Figure 3.56 and Figure 3.57 show the top view of the test device with the probes under optical microscope.

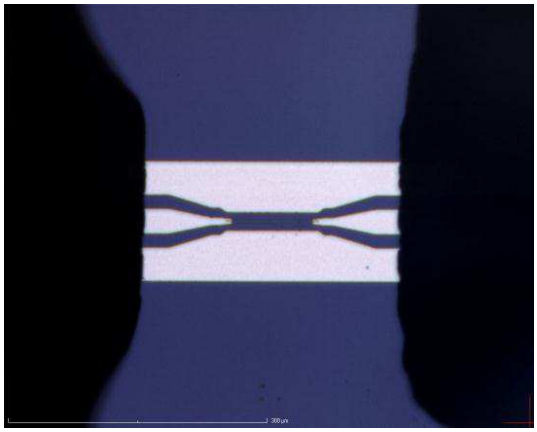


Figure 3.56 Complete test device with 50 µm pitch GSG probes

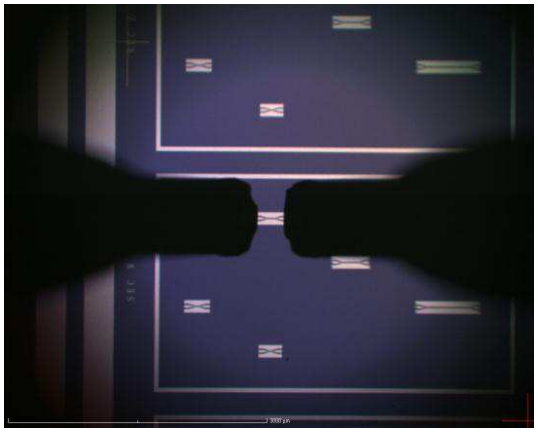


Figure 3.57 The test device with the probes at lower magnification

3.2.3. DC Resistance Measurement

I–V measurements were conducted on an HP 4155 semiconductor parameter analyser. The DC resistance was measured at different applied currents in the range of 100~700 µA with a compliance voltage at 2 V. The measurement was carried out with Karl -Suss PM5 wafer probe station. The probes are also provided by Karl -Suss (single tip, PH120 Precision Probe Manipulator). Two probes were placed separately on the signal input and output pad to measure the total resistance. 25 data points were acquired. Three sample types were selected for testing (sample Nos.C1, D1 and E1). The measured resistance with respect to different line lengths is plotted in Figure 3.58. Note that the obtained value is a sum of the resistance consisting of probe to pad contacts, pads, pad to line contacts, and the line itself. It is possible to isolate the line resistance using the measured resistance of different lengths although the extracted resistance per unit length is very sensitive to measurement errors. However, the result suggests that the contact between the line and pad is an ohmic contact (purely metal to metal). And based on the linear fitting, such contact impedance should be less than 40 Ω and the conductivity is about 2.4×10^7 S/m in the case of Sample No.D1 (the bulk gold conductivity is 4.2×10^7 S/m).

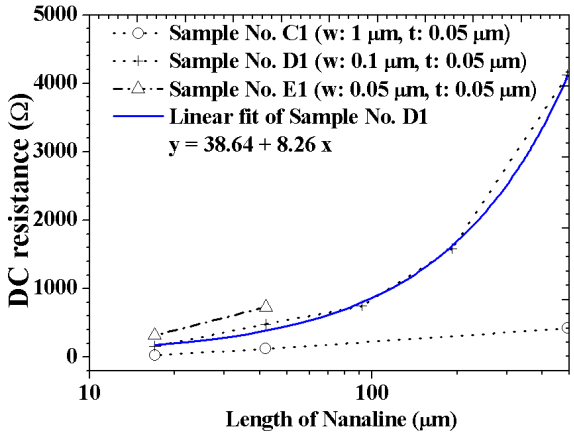


Figure 3.58 Total DC resistance of three different sample types. w and t denote the linewidth and thickness of the lines.

3.2.4. Verification of the New Subtraction Method

The method described in Section 3.1.6 for the extraction of transmission line parameters will be applied on these new samples. The contact impedance can also be estimated. The extracted contact impedance Z_L is an approximation for the actual impedance. Figure 3.59 shows the contact impedance of sample Nos.B1 and C1. The impedance indicates a capacitive behaviour with a positive resistance. In an attempt to understand the physical behaviour of the extracted contact impedance, simulation is performed using the circuit model in Figure 3.60. The best fit is obtained by tuning the individual circuit elements using $R1$ = 15 Ω, $R2$ = 34 Ω, $C1$ = 0.34 fF, $C2$ = 300 fF for sample No.C1. In case of sample No.B1, $R1$ = 63 Ω, $R2$ = 280 Ω, $C1$ = 0.16 fF, $C2$ = 108 fF were obtained. The R2C2 model accounts for the variation of contact resistance as a function of frequency. The roles of each element are as follows. $R2$ has a strong influence on the maximum value for both the resistance and the reactance whereas $C2$ is responsible for the frequency where the maximum value occurs. At very high frequencies, the contact resistance is approximated by $R1$. $C1$ represents the influence of signal discontinuity at the transition between the line and the pad as was discussed in Chapter 2. The addition of such component is to optimize the resistance at high frequencies. As the value of C1 is relatively small, the effect of such capacitance can be neglected. Therefore, the assumption that the contact impedance can be modelled solely by a lumped series admittance is not violated, the new proposed de-embedding method should be valid for these samples. It is interesting to note that the estimated contact impedance is found to be somewhat larger than that obtained in DC measurement.

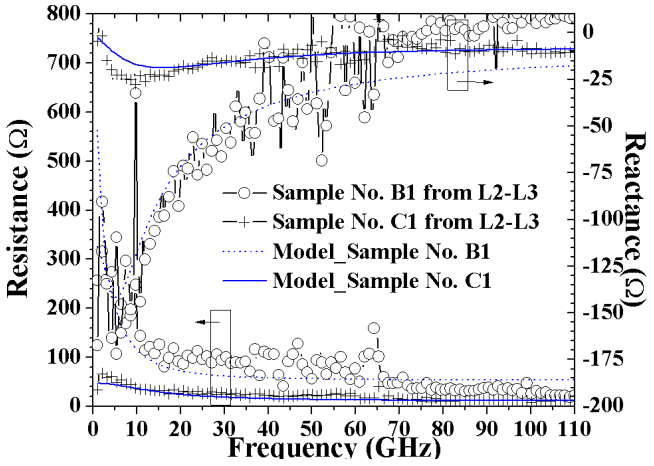


Figure 3.59 Extracted contact impedance using the two line method

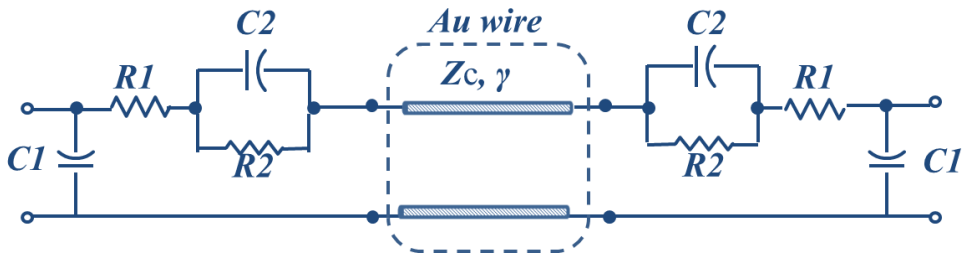


Figure 3.60 Circuit model of a Au nano-transmission line with contact impedance

3.2.5. Results and Discussion

The results are examined as follows. First, it will be demonstrated that the smaller CPW structure combined with the 50 µm-pitch GSG probes yields better measurement results. Then, the coupling effects between signal pads will again be addressed and the possibility to improve the de-embedding will be discussed. The extracted characteristics of the nano-lines in relation to their geometry and structure will be shown. Later, the physical limitations impeding the de-embedding method will be revealed. The fundamental technique is then extended to be more elaborate in order to maintain an accurate measurement well into mm-wave regime.

Impact of Pad Design on Extracted Parameters

Figure 3.61 to Figure 3.64 show the frequency dependence of *Zc*, γ and distributed parameters *R*, *L*, *G* and *C* of sample No.F1 de-embedded with the new method. The simulated and measured results are compared. The geometry of sample No.F1 is identical to that of sample No.4 in Section 3.1, representing a conventional micro-scale transmission line. It was fabricated at the same layer as the CPW structure with linewidth and thickness being 8 and 0.5 µm, respectively. There are three sets of extracted experimental data from different combinations of lines (L2-L3 = 100 µm, L3-L4 = 300 µm and L2-L4 = 400 µm). The simulated results are shown in solid line. It is not surprising to see that the estimation for the contact impedance is close to zero, as shown in Figure 3.65. The improvement using the 50 µm-pitch pads and probes can be noticed from the better agreement with the proposed model compared to those results obtained from the 100 µm-pitch setup (Figure 3.47 and Figure 3.48). It is in fact more likely that this set of measurement has better accuracy. For one, Im(*Zc*) should approach zero at high frequencies. For a low loss transmission line, when the frequency increases to a certain level, where $R \ll \omega L$ and $G \ll \omega C$. *Zc* can be simplified to $\sqrt{L/C}$ which is purely real.

As shown in Figure 3.63, the closed-form formula depicts the increasing resistance across a broad frequency range. Such increase is related to the initial stage of skin effect since the linewidth is larger than the skin depth (0.32 µm at 65 GHz with a conductivity being 3.77 × 10^7 S/m). There is observable deviation between the theoretical and experimental values at high frequencies. The conductance value simulated in ADS Momentum agrees very well with the experiment. By contrast, the model does not capture the frequency dependence of inductance and capacitance above 20 GHz.

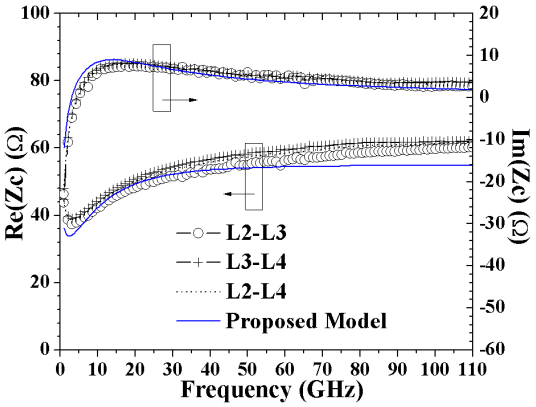


Figure 3.61 Measured and simulated *Zc* of sample No.F1

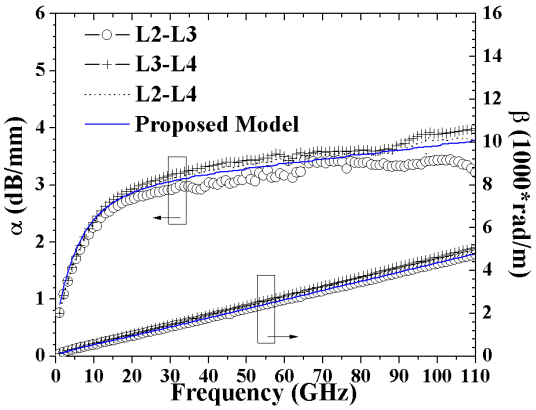


Figure 3.62 Measured and simulated γ of sample No.F1

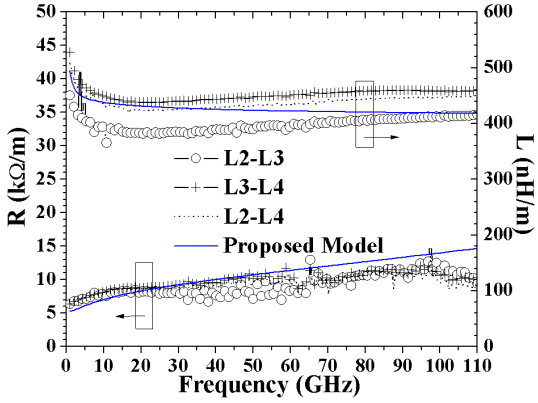


Figure 3.63 Measured and simulated *R* and *L* of sample No.F1

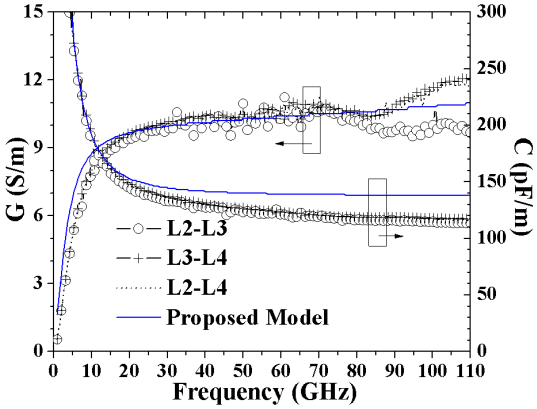


Figure 3.64 Measured and simulated *G* and *C* of sample No.F1

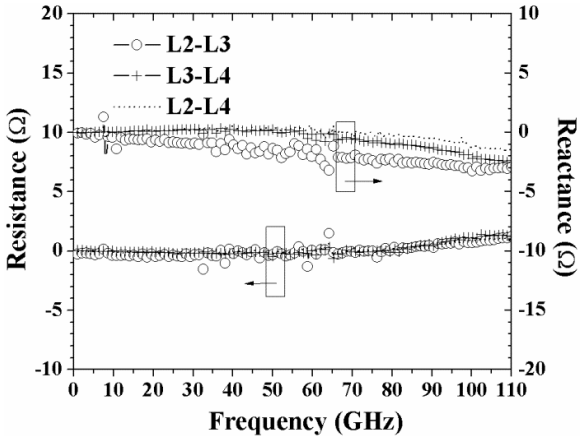


Figure 3.65 Extracted contact impedance Z_L

Figure 3.66 to Figure 3.69 further demonstrate the improvement in accuracy using 50 µm-pitch probes and pads. The dataset of L2-L3 from sample No.C1 is used for illustration. The best indicator to evaluate the measurement accuracy is the extracted *R*, *L*, *G* and *C*. It is evident that the measurement with 50 µm pitch test set is much closer to the theoretical value and yields physically reasonable characteristics. This implies that reducing the size of the pads and the implementation of smaller pitch GSG probes helps to improve the accuracy of the measurement. In other words, parasitics from the test set should be minimized despite the availability of de-embedding techniques. Note that the Au conductivity applied in the simulation is 1.9×10^7 S/m which is 16% higher than that of Al nanowires.

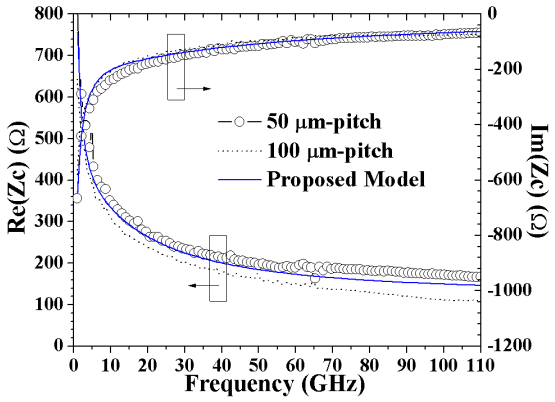


Figure 3.66 Measured and simulated *Zc* of sample No.C1 with different pad designs

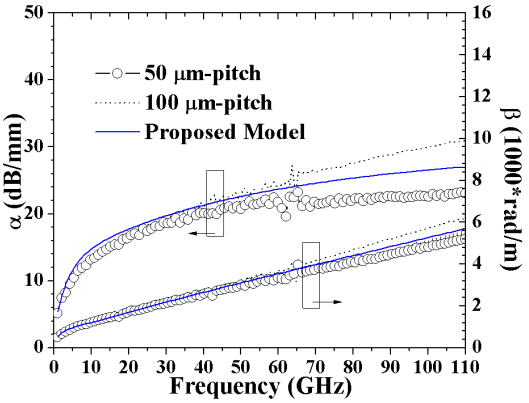


Figure 3.67 Measured and simulated *γ* of sample No.C1 with different pad designs

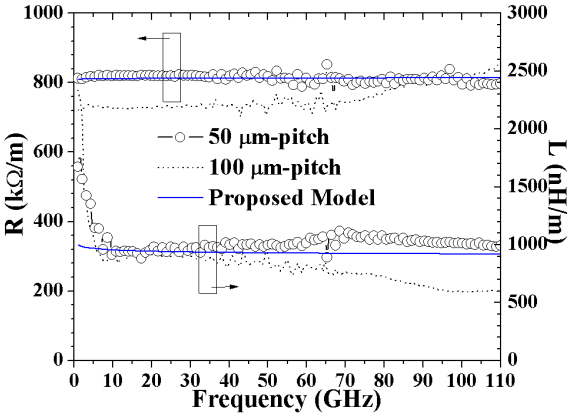


Figure 3.68 Measured and simulated *R* and *L* of sample No.C1 with different pad designs

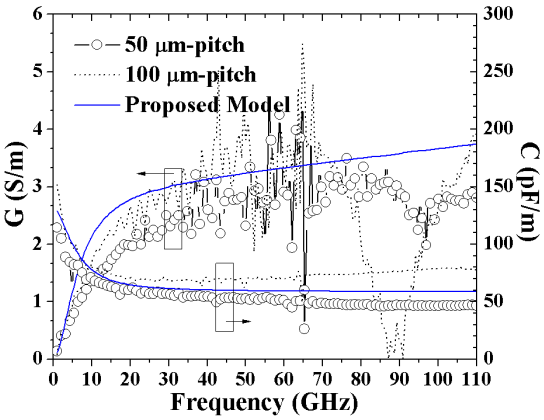


Figure 3.69 Measured and simulated *G* and *C* of sample No.C1 with different pad designs

Impact of Signal Pad Coupling on Extraction Parameters

In Section 3.1.5, the issue of signal pad coupling was revealed. Due to the substantial uncertainty presents in the result, it was difficult to determine if the de-embedding technique should be adjusted to account for this parasitics. In this section, the path will be continued to analyse this effect to the test result. Figure 3.70 shows the extracted Z_{co} of 50 µm-pitch CPW empty devices of various separation distances using the method described in Section 3.1.5. These empty devices show similar behaviours as those of 100 µm-pitch ones (Figure 3.36). However, the capacitive coupling effect is less pronounced between these signal pads. Considering the curve of Im(Z_{co}) with l = 92 µm, it tends to be slightly inductive at above 36 GHz. As mentioned earlier, it is likely that there is another mode of propagation excited between the pads, which will offset Im(Z_{co}), making it significantly less capacitive. At 110 GHz, a small inductance of approximately 3 nH can be derived.

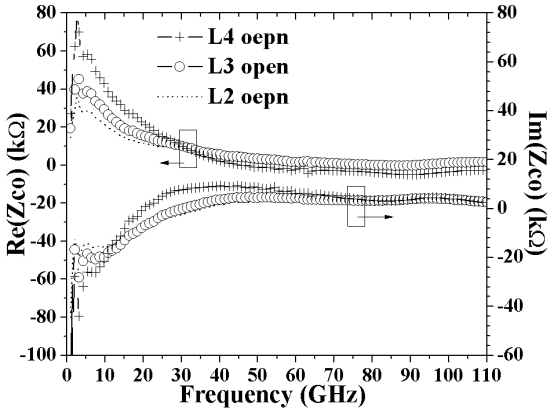


Figure 3.70 Coupling impedance between 50 µm pitch signal pads at different distances. L4 open: open device with l = 492 µm. L3 open: open device with l = 192 µm. L2 open: open device with l = 92 µm.

To determine whether it is necessary to consider such parasitics, it is helpful to verify the accuracy of the extracted parameters after subtraction. As an example, we take sample No.B1 having the linewidth and thickness being 0.2 and 0.1 µm using only the dataset of L2-L3 for verification (Figure 3.71 to Figure 3.74). The observation is similar to that in Section 3.1.5 in which the major difference between with and without subtraction of Y_{12} (coupling admittance between the signal pads) lies in the attenuation constant. Here at 90 GHz, an increase of 15% in α is obtained and the discrepancy between the extracted and simulated data is minimized from 8.4 to 4.6%. A noticeable difference can be observed in *R* and *L* as shown in Figure

3.73. The result after the removal of Y_{12} seems more reliable. For one, R and L are less sensitive to the frequency, and correspond better to the simulation. Since there is a noticeable improvement in the extracted result, it is reasonable to believe that the removal of signal pad coupling should be included in the de-embedding technique.

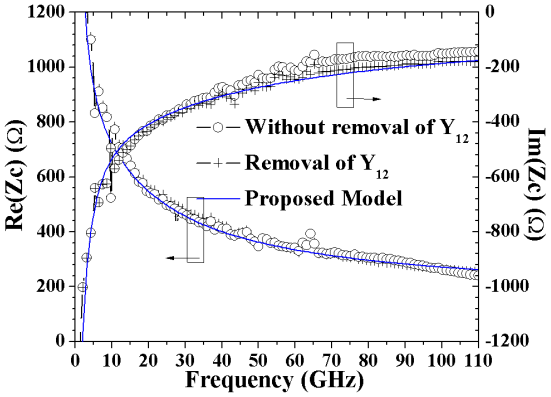


Figure 3.71 Measured and simulated *Zc* of sample No.B1 with and without removal of coupling effect

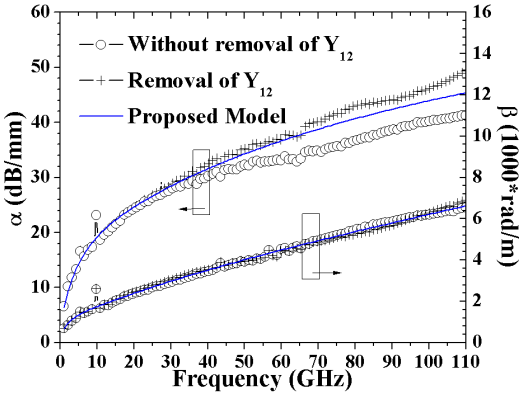


Figure 3.72 Measured and simulated γ of sample No.B1 with and without removal of coupling effect

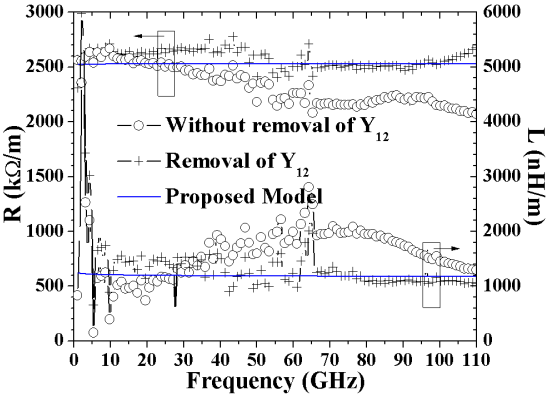


Figure 3.73 Measured and simulated *R* and *L* of sample No.B1 with and without removal of coupling effect

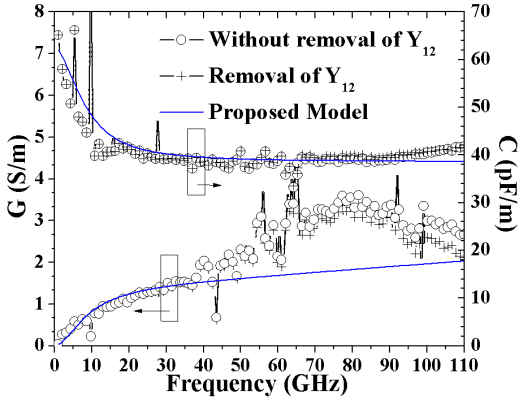


Figure 3.74 Measured and simulated *G* and *C* of sample No.B1 with and without removal of coupling effect

Performance Comparison of Single and Multiple Nano-lines

The discussion in the previous section completes the de-embedding procedure which will be applied to the test structures. Apart from single nano-lines, multiple nano-lines will also be characterized. The performance of single and multiple nano-lines for a given dimension will be compared in the following section. It is important to see how the transmission line parameters scale with number of nano-lines (*N*). The information is helpful not only to provide a design rule for passive RF components but to identify limitation in the measurement setup. The sets of measurement in this analysis are from sample Nos.A1 and B1. The linewidths of these samples are 0.1 and 0.2 µm, respectively with the same thickness of 0.1 µm.

The first set of data presented is from sample No.B1. Sample Nos.B2[a] and B5[a] refer to two and five nano-lines carrying currents in a parallel path with the identical cross-section as sample No.B1. The interline distance is 0.2 µm. Figure 3.75 to Figure 3.78 show the measured and simulated *Zc* and γ. In each figure, there are three groups of traces, sample Nos.B1, B2[a] and B5[a]. Three datasets extracted from different pairs of nanolines (L2-L3, L3-L4 and L2-L4) are included for every group. Quasi-TEM model for the single transmission line is added as a reference. Each group has a distinct trace so it is easy to distinguish one

from another. Sample No.B5[a] having the most amounts of metal lines naturally has the lowest characteristic impedance and propagation constant. The result extracted from multiple nano-lines either from sample No.B2[a] or B5[a] demonstrates a consistent trend. As for the single line, the dataset associated with the measurement of L4 (L3-L4 and L2-L4) shows a significant deviation in *Zc* from the model, in particular at frequencies above 30 GHz. This could be attributed to small transmission signal given from L4. The only well-behaved curve is from L2-L3 which agrees sufficiently well with the model. For better understanding the performance of these structures, one should consider the effective distributed RLGC parameters of the devices (from Figure 3.79 to Figure 3.82). It is interesting to note that *R* is nearly constant at all frequencies, meaning that these lines do not suffer from skin effect. Besides, the effective resistance of multiple lines is simply the resistance of a single nano-line divided by the number of lines (*N*). As for *L* and *C*, not surprisingly, we observe a reduction in inductance and an increase in capacitance per unit length as *N* increases. However, it appears that the devices with multiple lines are not simply the parallel combination of the circuit for a single line. Due to the proximity between the nano-lines, there is coupling effect between the lines, introducing mutual inductance and capacitance. As a consequence, the total effective inductance and capacitance do not scale linearly with *N*. The higher effective capacitance is naturally accompanied by higher dielectric loss, thereby higher *G*.

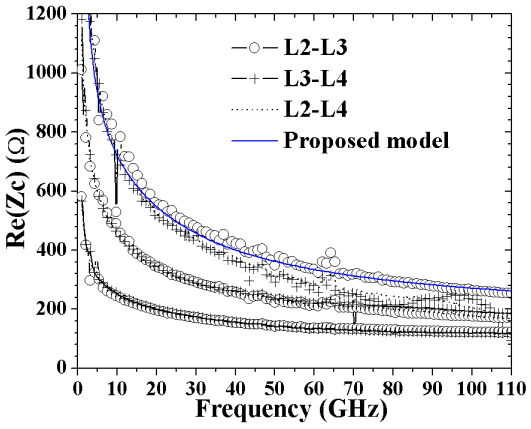


Figure 3.75 Measured Re(*Zc*) of sample Nos.B1, B2[a] and B5[a] (from top to bottom). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included.

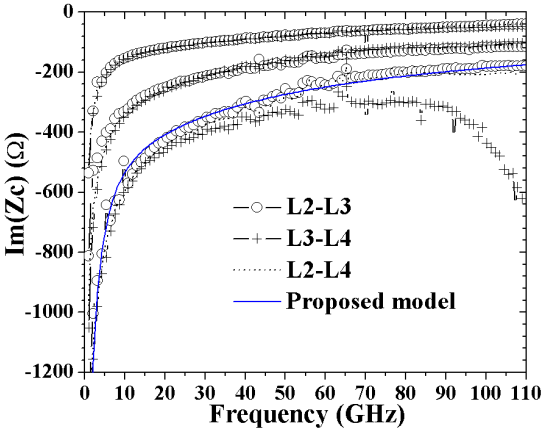


Figure 3.76 Measured Im(*Zc*) of sample Nos.B1, B2[a] and B5[a] (from bottom to top). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included.

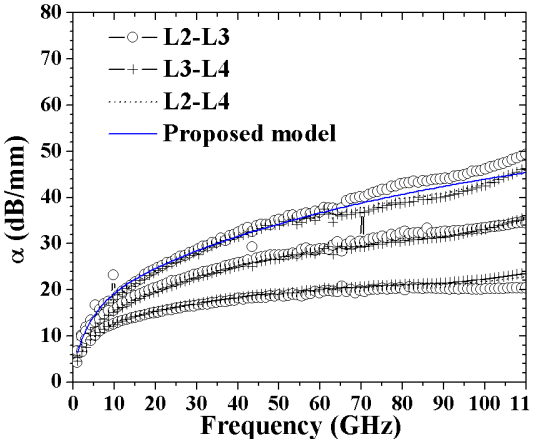


Figure 3.77 Measured α of sample Nos.B1, B2[a] and B5[a] (from top to bottom). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included.

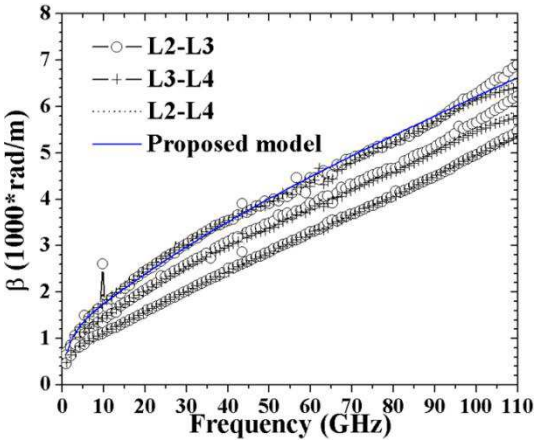


Figure 3.78 Measured β of sample Nos.B1, B2[a] and B5[a] (from top to bottom). Each sample type has three datasets (L2-L3, L3-L4 and L2-L4). The proposed model for sample No.B1 is included.

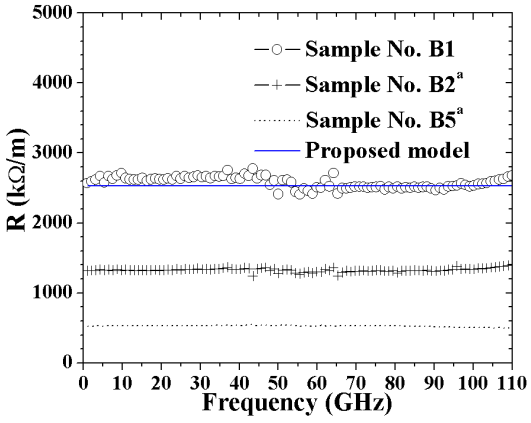


Figure 3.79 Measured *R* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included.

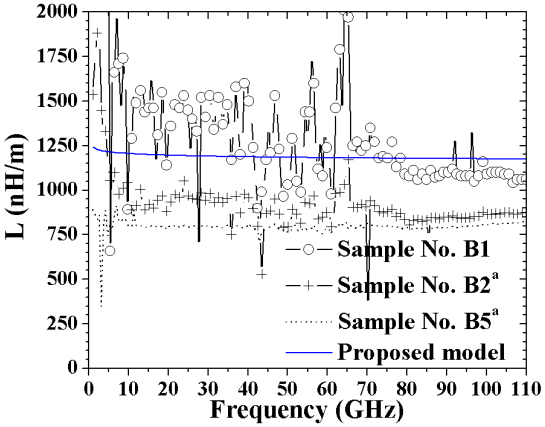


Figure 3.80 Measured *L* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included.

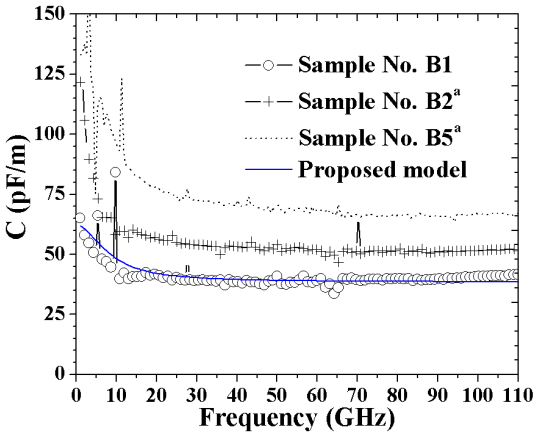


Figure 3.81 Measured *C* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included.

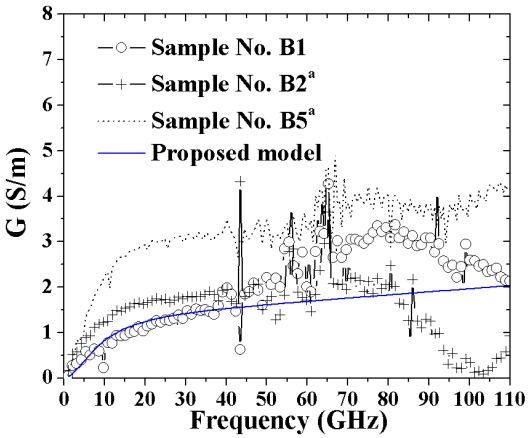


Figure 3.82 Measured *G* of sample Nos.B1, B2[a] and B5[a]. The proposed model for sample No.B1 is included.

Another set of measurement is sample No.A1 (0.1 µm thick and wide). Likewise, Sample Nos.A2[a] and A5[a] refer to two and five nano-lines with the identical cross-section as Sample No.A1 (Figure 3.83 to Figure 3.87). A similar problem arises in certain datasets. We begin to see distortion in trace at high frequencies even for those ones of L2-L3. When examining measurement data, it can be seen that *Zc* at the frequency above 60 GHz for sample No.A1 and No.A2[a] are not reliable. Yet, the plots of α and β from sample No.A2[a] still provide a trustable reference. It should be noted that for better illustration, the datasets of L3-L4 and L2-L4 from these two sample types are intentionally omitted. The proposed model for the single line device agrees well with the experimental data up to 40 GHz. If the line still respects the conventional transmission line theory, the model is a good indication of what should be expected at the frequencies above. Consequently, the extracted *R* is plagued by the inaccurate *Zc* and γ after calculation (Figure 3.87). It is relevant to mention that the estimated metal conductivity is 1.9×10^7 S/m. Such Au line reaches up to 5000 kΩ per unit length, presumably remaining constant at all measured frequencies.

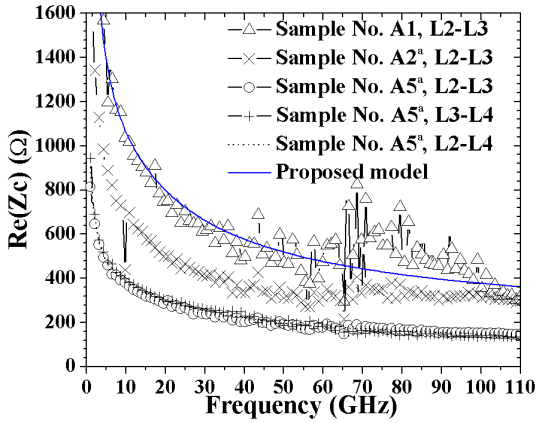


Figure 3.83 Measured Re(*Zc*) of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included.

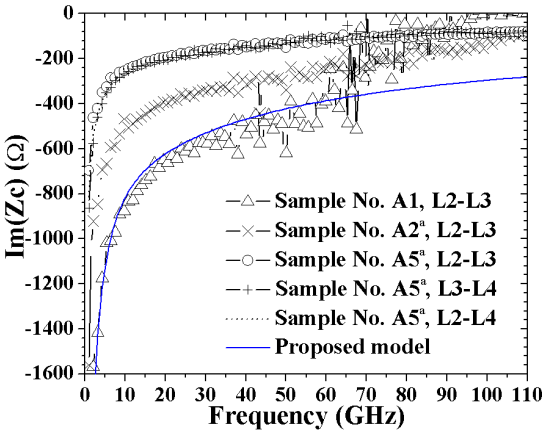


Figure 3.84 Measured Im(*Zc*) of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included.

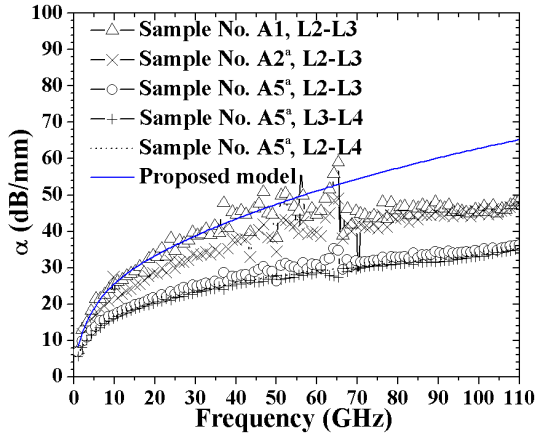


Figure 3.85 Measured α of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included.

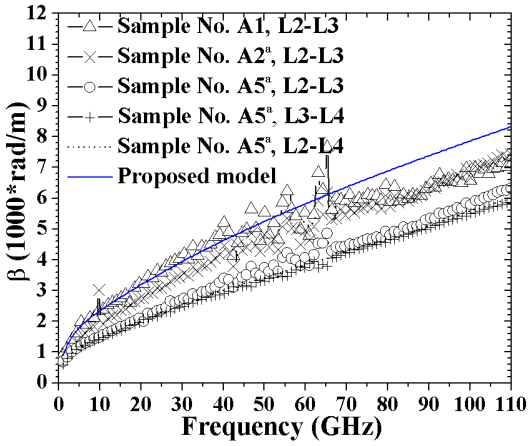


Figure 3.86 Measured β of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included.

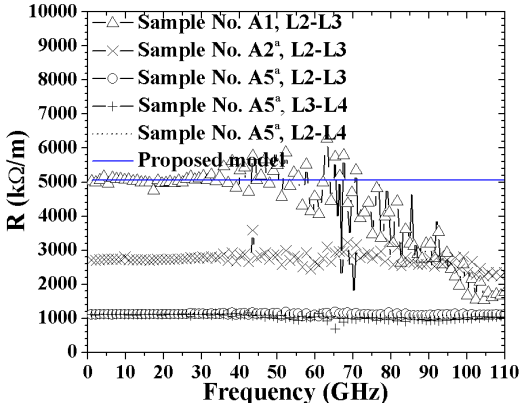


Figure 3.87 Measured *R* of sample Nos.A1, A2[a] and A5[a]. The proposed model for sample No.A1 is included.

Table 3.4 summarizes the discrepancies between the simulation results and measurement for sample Nos.A1, B1 and C1. Only the datasets from L2-L3 are taken into account. The new de-embedding procedure yields a significantly improved accuracy comparing to the result presented in Table 3.2. Within approximately 5% error for all the four parameters is achieved in the case of sample No.B1. In particular, the extracted Im(*Zc*) shows dramatic improvement when the proposed technique is used. The model agrees less with the result obtained from sample No.C1, especially at mm-wave range. This is in agreement with what

was observed earlier in Section 3.1.6 in the case of sample No.1. A good indication to examine the accuracy of the model is the correspondence of RLGC elements. Figure 3.69 (it can be found in Section 3.2.5) shows that the percentage difference between the theoretical and actual values in capacitance could reach as much as 20% at 110 GHz. It is likely that the mesh density was set too low for the slot lines in ADS Momentum. In addition, sample No.A1 exhibits unusually large discrepancy at 90 GHz. This is related to the trace distortion which was discussed earlier. This issue will be address later.

Table 3.4 Discrepancy between simulation and measurements for sample Nos. A1, B1 and C1 using L2-L3 dataset. The variation of α is estimated as $\frac{\alpha_{mea}-\alpha_{simu}}{\alpha_{simu}}$. The other parameters are calculated in the same manner.

% variation	30 (GHz)				60 (GHz)				90 (GHz)			
	Re(Zc)	Im(Zc)	α	β	Re(Zc)	Im(Zc)	α	β	Re(Zc)	Im(Zc)	α	β
Sample No. C1	6.3	8.2	-5	-2	9.8	11.1	-4	-5	16.7	18.8	-8	-8
Sample No. B1	5.2	3.3	0.4	2	0.4	-2.8	0.5	-0.6	-2.7	-3.9	4.6	-2
Sample No. A1	-6.4	6.6	1.6	2.5	-0.9	0.2	-13	-4.9	34.3	-92.6	-25	-15

Impact of Gap Distance on Extraction Parameter

For coplanar wave guides, the electromagnetic field is mainly concentrated between the ground planes and the central conductor. Depending on the choice of slot width (distance between the signal line and ground plane), the transmission line characteristic can be modified [79]. In this study, two types of gap distance are considered in the design: 12 and 20 µm. The gap is defined as the distance between the two ground planes (see Figure 3.53). The effect of gap distance is evaluated and plotted in Figure 3.88 to Figure 3.91 for sample Nos.B1 and A2[a] and only the traces of L2-L3 are taken into consideration. With a smaller gap, a noticeable shift of curve can be found in the real part of characteristic impedance, approximately 10% at the range around 90 GHz. Other parameters show less than 5% percentage difference, which is within the uncertainty range of the original measurement. As a reference, a repeatability test is performed on a second device for sample type No.B1'. If ignoring jitter in the signal, the maximum variation is 5% in all parameters. Similar behaviour, perhaps obscured by the distortion in the trace at mm-wave range, is observed in the two line device for sample type No.A2[a]. The result implies that the gap distance seems to have only a mild influence on the transmission line characteristics.

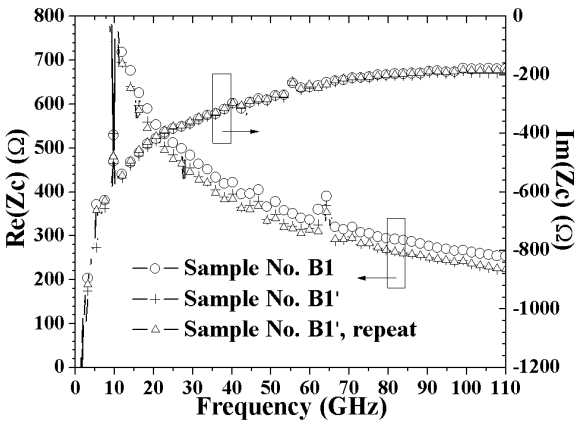


Figure 3.88 Measured *Zc* of sample Nos.B1 and B1'. Sample No.B1: single line, linewidth= 200 nm, gap distance = 20 µm. Sample No.B1' and Sample No.B1', repeat: single line, linewidth= 200 nm, gap distance = 12 µm

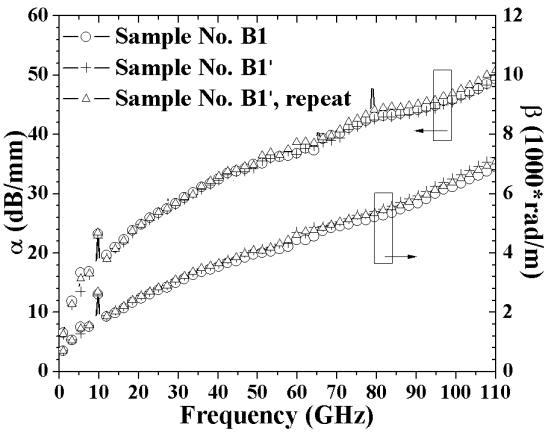


Figure 3.89 Measured γ of sample Nos.B1 and B1'. Sample No.B1: single line, linewidth= 200 nm, gap distance = 20 µm. Sample No.B1' and Sample No.B1', repeat: single line, linewidth= 200 nm, gap distance = 12 µm

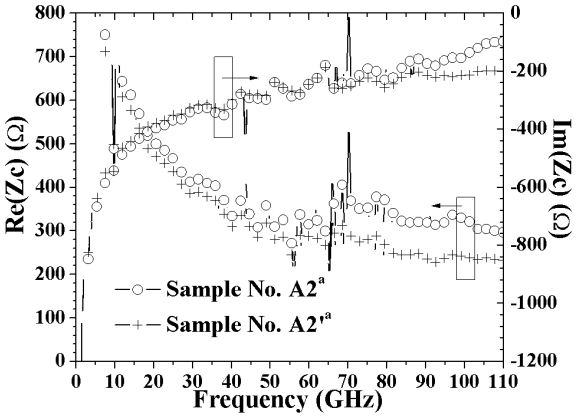


Figure 3.90 Measured *Zc* of sample Nos.A2[a] and A2'[a]. Sample No.A2[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 20 µm. Sample No.A2'[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 12 µm.

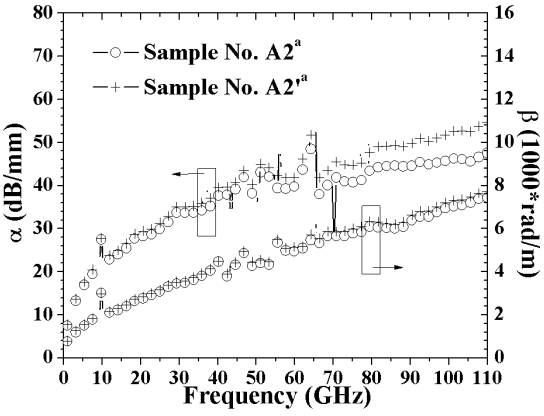


Figure 3.91 Measured γ of sample Nos.A2[a] and A2'[a]. Sample No.A2[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 20 µm. Sample No.A2'[a]: double line, linewidth = 100 nm, interline distance = 200 nm, gap distance = 12 µm.

Impact of Inter-line Distance on Extraction Parameters

It was shown that impact of gap distance is rather minor. Another interesting design factor in multiple line devices is the separation distance between the lines. Figure 3.92 to Figure 3.99 show the influence of interline distance to the extracted *Zc* and γ. This set of data is based on nano-lines with linewidth being 0.2 µm and thickness 0.1 µm and only the traces of L2-L3 are taken into consideration. Sample Nos.B2[a] and B5[a] refer to two and five nano-lines with interline distance being 200 nm whereas Sample Nos. B2[b] and B5[b] are with 1000 nm. As show in Figure 3.94, the increase in interline distance introduces more attenuation but such effect is only found for the device with five nano-lines. Specifically, more than 30 % of change is seen at 90 GHz. When examining closely, Re(*Zc*) and Im(*Zc*) are both slightly lower across the frequency range. At 30 GHz, the differences are approximately 12% and they become less and less significant at frequencies above this point. We can also consider RLCG parameters to further interpret the result (from Figure 3.96 to Figure 3.99). The observed increase in α can be attributed to the increase in dielectric loss (*G*) which is associated with the comparatively higher effective capacitance. The effective inductance has dropped substantially but this only begins to have influence on *Zc* and γ at high frequencies since *R* is dominant in the frequency of analysis. In fact, at low frequencies, *Zc* can be approximated be $\sqrt{R/G}$. At the high frequencies, the expression for *Zc* becomes $\sqrt{(R + j\omega L)/(j\omega C)}$. With this knowledge, it is then possible to explain the variation of *Zc*. Further supporting the impact of interline distance on transmission characteristics, Figure 3.100 and Figure 3.104 show another set of data using multiple nano-lines with linewidth and thickness being 0.1 µm. The result indicates that the influence of a wider separation distance is more significant when linewidth is smaller. For instance, lower characteristic impedances are readily evident at low frequencies. The difference reaches 20% at 30 GHz. It should be noted that the accuracy of Sample No.A2[a] appears less accurate than Sample No. A2[b] at mm-wave frequencies. The simple fact is that the trace for Re(*Zc*) appears discontinuous at the 65 GHz, the transition frequency of our measurement system.

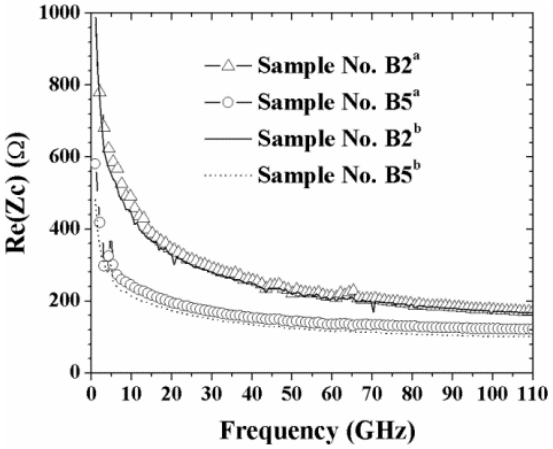


Figure 3.92 Measured Re(*Zc*) of sample Nos.B2[a], B2[b], B2[a] and B5[b]

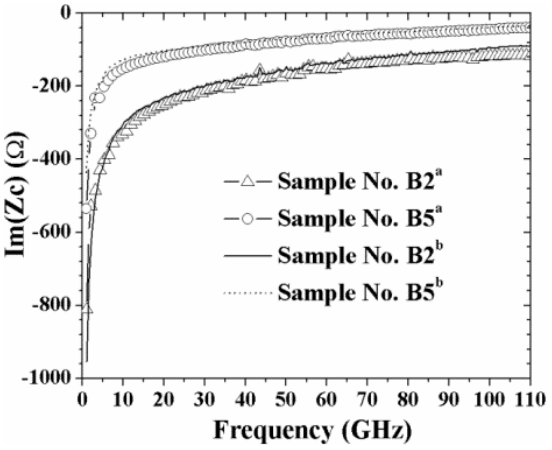


Figure 3.93 Measured Im(*Zc*) of sample Nos.B2[a], B2[b], B2[a] and B5[b]

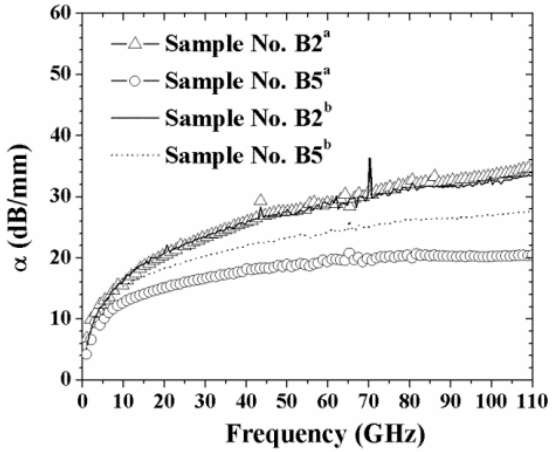


Figure 3.94 Measured *α* of sample Nos.B2[a], B2[b], B2[a] and B5[b]

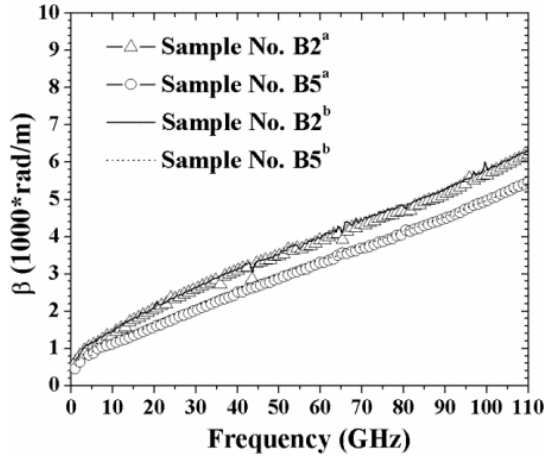


Figure 3.95 Measured *β* of sample Nos.B2[a], B2[b], B2[a] and B5[b]

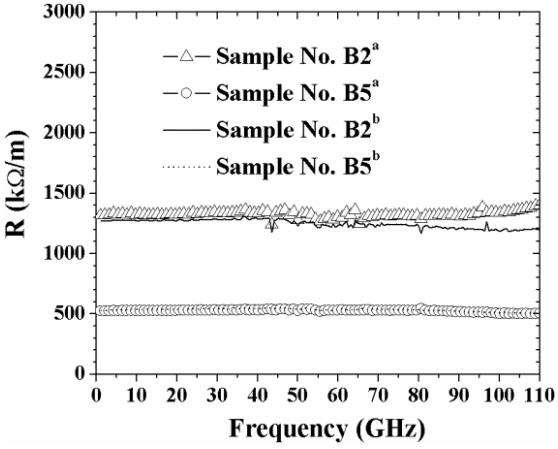


Figure 3.96 Measured *R* of sample Nos.B2[a], B2[b], B2[a] and B5[b]

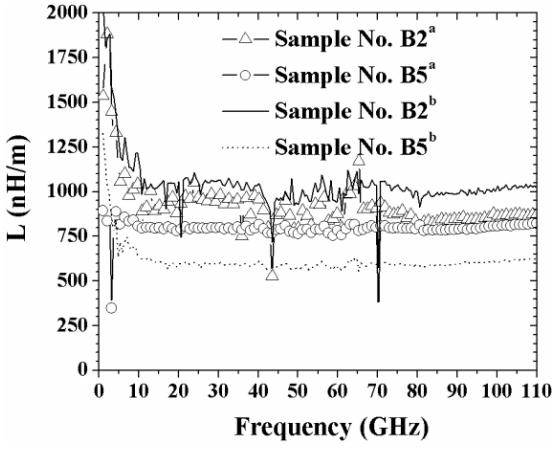


Figure 3.97 Measured *L* of sample Nos.B2[a], B2[b], B2[a] and B5[b]

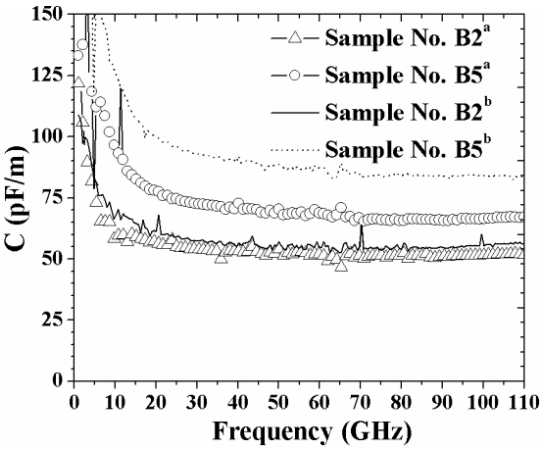


Figure 3.98 Measured *C* of sample Nos.B2[a], B2[b], B2[a] and B5[b]

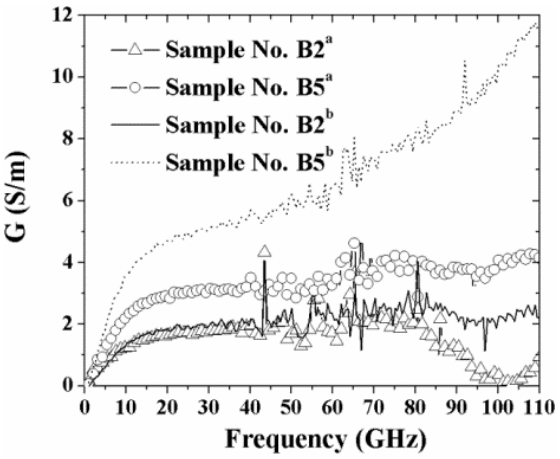


Figure 3.99 Measured *G* of sample Nos.B2[a], B2[b], B2[a] and B5[b]

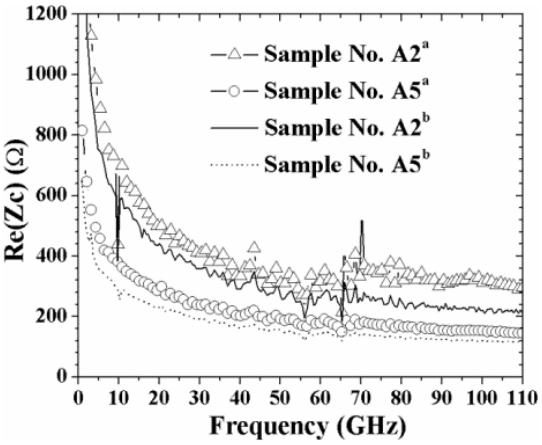


Figure 3.100 Measured Re(*Zc*) of sample Nos.A2[a], A2[b], A2[a] and A5[b]

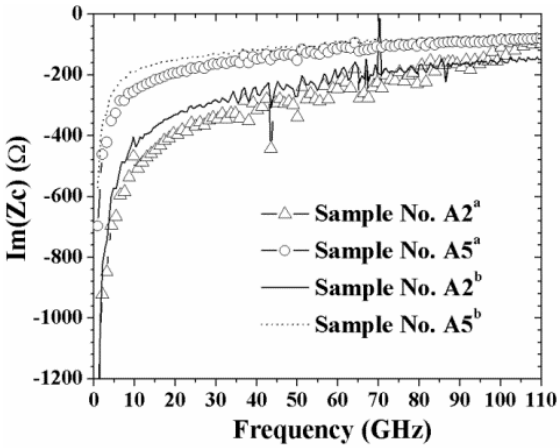


Figure 3.101 Measured Im(*Zc*) of sample Nos.A2[a], A2[b], A2[a] and A5[b]

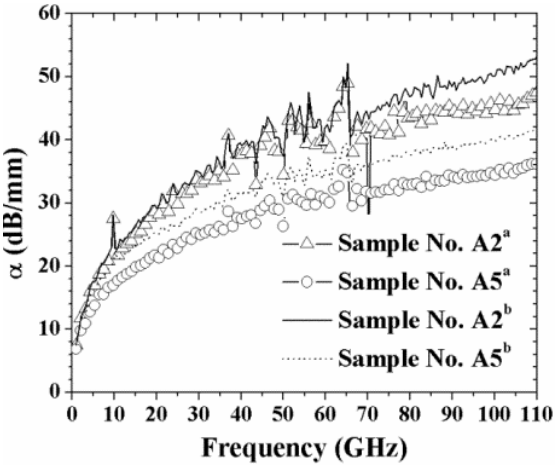


Figure 3.102 Measured α of sample Nos.A2[a], A2[b], A2[a] and A5[b]

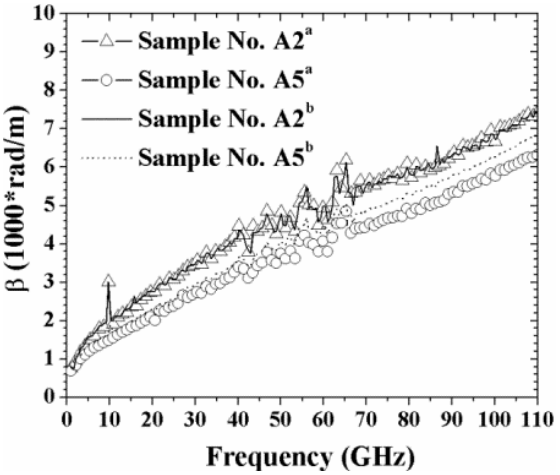


Figure 3.103 Measured β of sample Nos.A2[a], A2[b], A2[a] and A5[b]

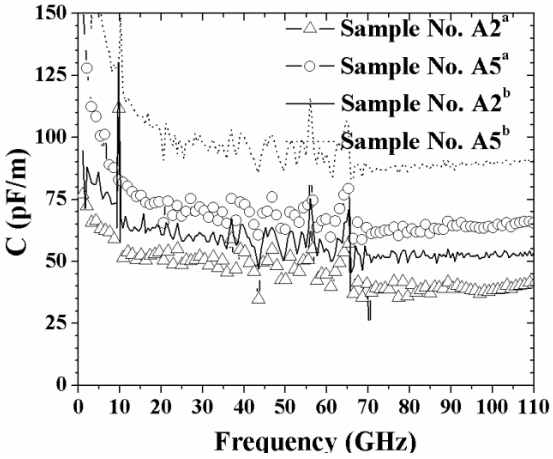


Figure 3.104 Measured *C* of sample Nos.A2[a], A2[b], A2[a] and A5[b]

Based on this analysis, we can see that the multi-line devices are favourable for signal transmission. They have less metal losses and better impedance matching with the test equipment. Although it is true that the attenuation remains far more than that of the actual state-of-the-art classic line, (the attenuation of a microstrip line in 65 nm technology node is typically lower than 2 dB/mm at 100 GHz), it was shown that α can be effectively minimized with increasing the numbers of nano-line (a decrease by 50% was seen with five parallel nano-lines at 100 GHz) Most importantly, the multi-line devices provide more freedom of design because the transmission characteristics can be controlled by changing the numbers of nano-lines, the distance between lines as well as the linewidth which makes them an attractive alternative to conventional CPW structure.

Limitation of the Extraction Procedure

It seems that the degradation of accuracy found in the extracted parameters is not due to the limitation of measurement system. One of the best indicators to identify the source of error is *S*-parameters. Figure 3.105 to Figure 3.107 shows the magnitude of S_{21} parameter taken directly from the measurement of the test samples along with the simulated ones. It should be noted that the pads are not taken into account in the simulation which explains slightly less losses. In the case of sample No.C1, the measured *S*-parameters follow the simulated ones for all the lines of different lengths (L2, L3 and L4). However, this is not the case for sample Nos.B1 and A1. We can see that the measured data from L4 deviates from the theoretical value. It could even be argued that the deviation is observed for sample No.A1 in L3. In principle, transmission line properties do not depend on line length. There seems to be no reason why the simulation agrees well in the case of sample No.C1 but fails to satisfy the others. In Figure 3.108, the magnitudes of S_{21} parameters of the open structures from different lengths are compared. We also include the measurement with the probes in the air out of contact with the substrate. The result implies that there is propagation of signal between pads. Most importantly, the level of this receiving signal becomes comparable to the L4 measurements of sample Nos.B1 and A1 at high frequency region. It is likely that the transmission signal given by these lines is so small that the contribution from the test structure parasitics becomes equally important. In consequence, it is difficult to isolate the signal coming from the intrinsic device. Besides, the treatment of the two line method requires subtracting the RF response of another line and the contact impedance. Although not explicitly demonstrated here, it is relevant to mention that the extracted contact impedance Z_L

includes error and it becomes increasingly intolerable as the size of nano-line decreases. In the next section, thru-only de-embedding technique will be reconsidered which improves the degree of accuracy at mm-wave frequency.

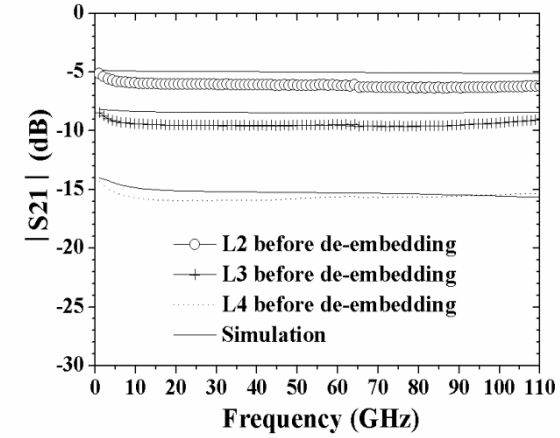


Figure 3.105 Magnitude of S_{21} for sample No.C1

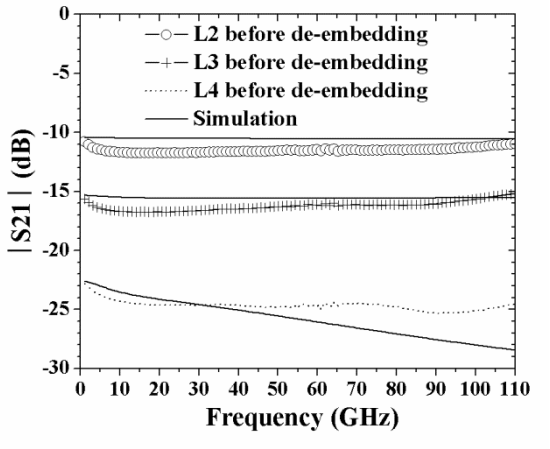


Figure 3.106 Magnitude of S_{21} for sample No.B1

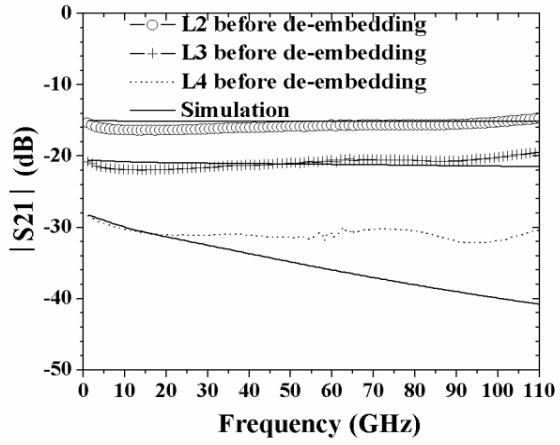


Figure 3.107 Magnitude of S_{21} for sample No.A1

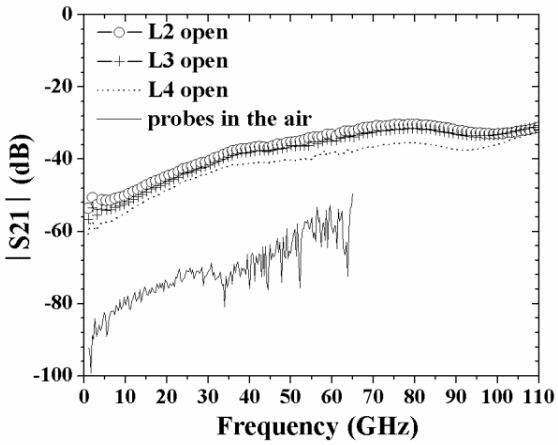


Figure 3.108 Magnitude of S_{21} from the empty open structures and when probes are in the air. L4 open: open device with l = 492 µm. L3 open: open device with l = 192 µm. L2 open: open device with l = 92 µm.

Other De-embedding Technique

Unfortunately, the measurement errors will always be present either from calibration or instrumentation. The error can propagate to all the *S*-parameters through the de-embedding calculus. In particular when insertion loss is large, even a small measurement error can obscure the device characteristics. It has been shown that the validity of the technique, summarized earlier, is limited by the small transmission signal. To minimize over de-embedding, we reconsider thru-only method to examine the precision. In Section 3.1.5, the misfit between the measurement and the model was quantified. While the analysis concerned the de-embedding inaccuracy due to the underestimation of contact impedance below 30 GHz, at the frequencies beyond, the contact impendence residue has negligible effect on both *Zc* and γ. Figure 3.109 to Figure 3.114 compare the extracted *Zc* and γ. L2-L3 refers to the de-embedded result using modified two line method while L3 represents the one de-embedded with thru-only method. It should not be surprising to observe some discrepancy at lower frequencies in sample No.B1 (linewidth and thickness equal to 0.2 and 0.1 µm, respectively.).

On the other hand, we see that the trace of L3 closely follows that of L2-L3 and the model at frequencies above 70 GHz. As for sample No.A1 (linewidth and thickness equal to 0.1 μm), the high-frequency characteristics are plagued by errors in L2-L3. In contrast, the trace of L3 maintains a continuous frequency-dependent curve above 70 GHz, despite of the observable disagreement with the model. The extracted result shows that the propagation delay ($v = \omega/\beta$) is longer and has far more attenuation than the theoretical values. This actually corresponds to the claim in Section 3.1.5 when evaluating the 100 nm wide Al nanowire (sample No.3). Here, the misfits between the model and the extracted α and β are about 13.0% and 12.5% at 90 GHz, respectively (In Section 3.1.5, α is 25% and 18% for β were found at 90 GHz when l = 192 μm for sample No.3). Figure 3.114 (showing the case of two nano-lines with the same dimension as sample No.A1) further supports the limited precision of extracted α and β at high frequencies using two line method when the linewidth scales down to 100 nm. One gets 8.8% and 10.9% less in α and β at 100 GHz, respectively comparing to the values de-embedded with thru-only method. This result clearly reveals that according to the frequency range, different de-embedding procedures should be applied while characterizing nano-transmission line.

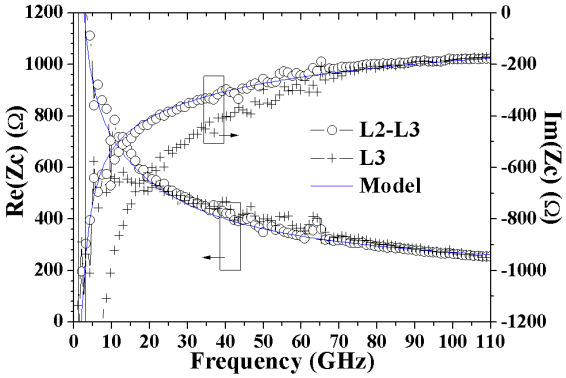


Figure 3.109 Comparison of de-embedded *Zc* for sample No.B1

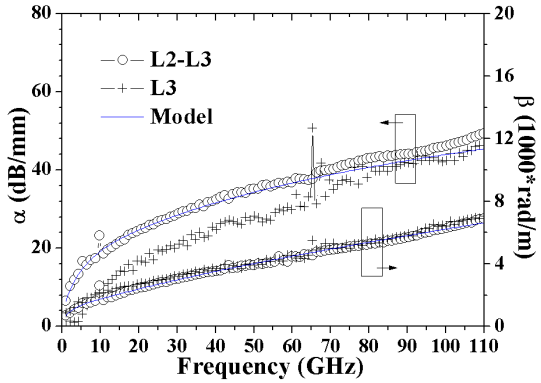


Figure 3.110 Comparison of de-embedded γ for sample No.B1

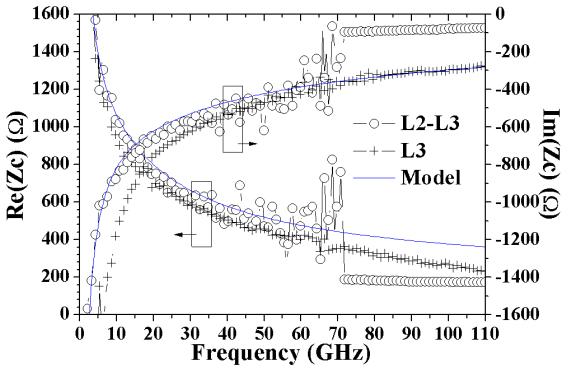


Figure 3.111 Comparison of de-embedded *Zc* for sample No.A1

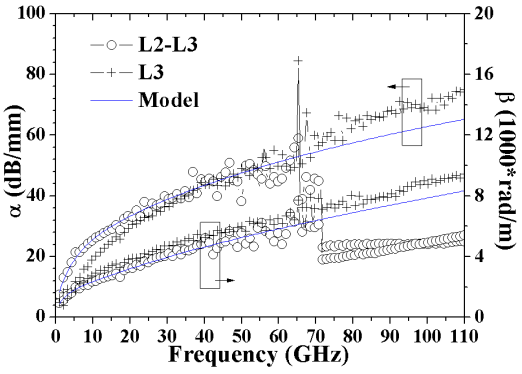


Figure 3.112 Comparison of de-embedded γ for sample No.A1

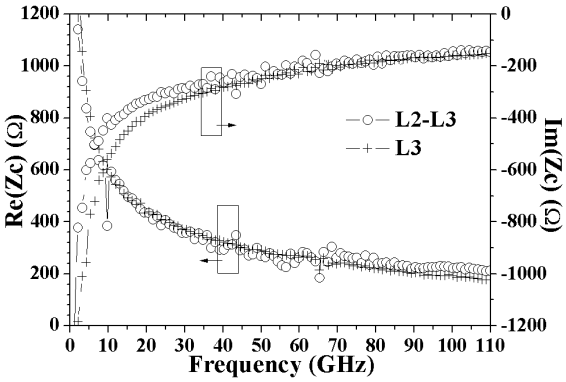


Figure 3.113 Comparison of de-embedded *Zc* for sample No.A2[b]

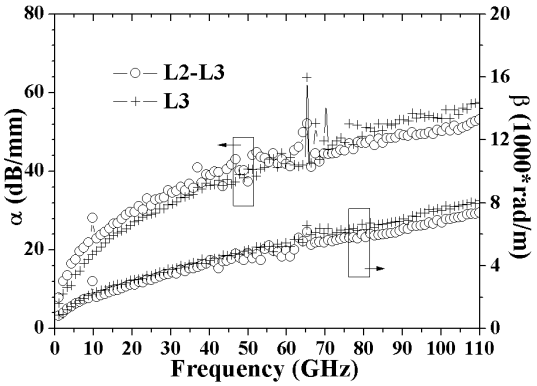


Figure 3.114 Comparison of de-embedded γ for sample No.A2[b]

Having gained the insight from the new analysis, we revisit the measurement and perform the extraction using thru-only de-embedding method, only to confirm the previous statement. The results of the single-line devices with different dimension are plotted in Figure 3.115 and Figure 3.116. Only the frequency range above 65 GHz is examined this time. Sample No. F1, having a dimension closer to typical transmission lines in the advanced RF-CMOS technology is included for establishing a point of reference. Theoretical values are included for comparison, shown in dotted line. Narrow conductors, like sample Nos.B1 and A1 show that their propagation delays ($v = \omega/\beta$) are much longer and the characteristic impedances are far more frequency-dependent than those of the wider lines. The high resistance has made the nanowire slower compared to conventional transmission lines. Good agreement can be seen between the model and the actual values, except for sample No.A1. At 90 GHz, its Re(*Zc*) is 27.8% lower than the simulation while α and β are 13.0% and 12.5% higher, respectively. Im(*Zc*), on the other hand, matches perfectly with the theoretical value. It is likely that elements like inductance/capacitance associated with quantum transport effect need to be added to physically interpret the additional latency and losses in sample No.A1. However, it is true that they might not be as impressive as in the case of a CNT [27].

An interesting design problem is: can we make use of the appearance of slow wave while avoiding high conduction losses by utilizing a multiple nanowire system? Let us examine the performance of a parallel combination of nanowires and a single wire having the same amount of conductor. Sample No.A2[b] and B1 will be a perfect example (Figure 3.117 and Figure 3.118). Sample No.A1 is included for comparison. If comparing sample Nos.A1 and B1, 39.5% increase in β can be observed at 90 GHz. Yet, the increase is only 5.6% if two nanowires of the same dimension as sample No.A1 are used instead (sample No.A2[b]). Its attenuation is effectively reduced but still higher than Sample No.B1 by 16%. A reasonable trade-off may be made to achieve desired circuit performance.

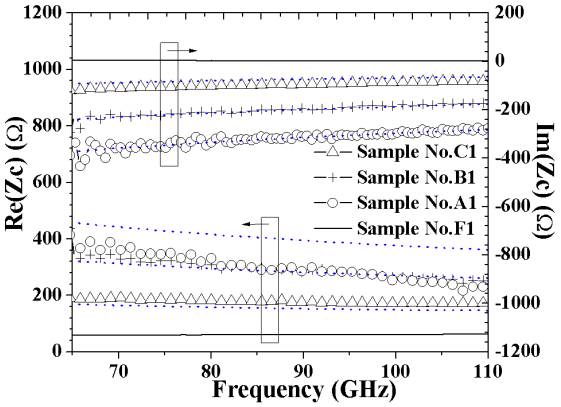


Figure 3.115 Comparison of *Zc* between different sample types. Dotted lines are the corresponding simulated results.

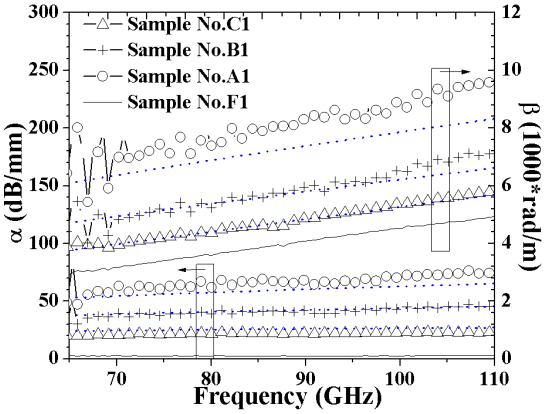


Figure 3.116 Comparison of γ between different sample types. Dotted lines are the corresponding simulated results.

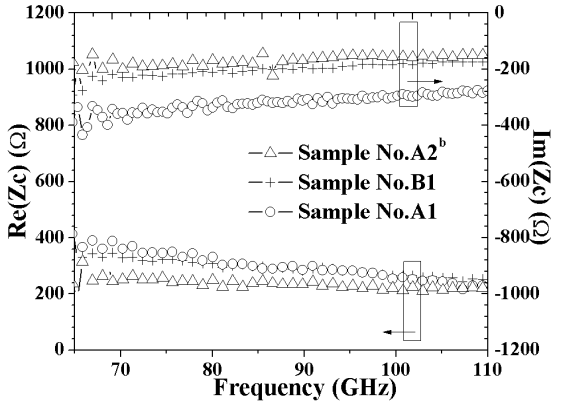


Figure 3.117 Comparison of *Zc* between different sample types

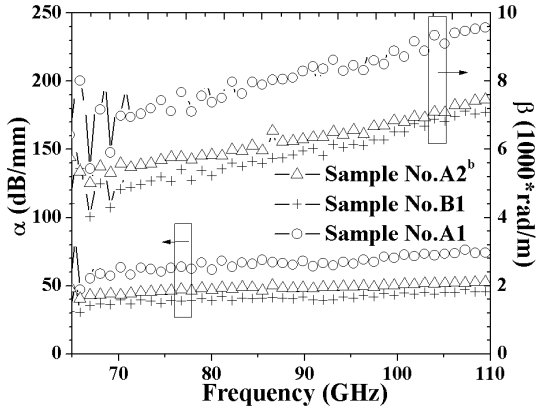


Figure 3.118 Comparison of γ between different sample types

3.3 140-210 GHz Characterization

Having performing a thorough characterization up to 110 GHz, it would be interesting to see how these nano-transmission lines behave at even higher frequencies. New measurement was carried out in VTT technical research centre in Finland using 140-210 GHz measurement setup. This included an HP 8510B VNA from Agilent as well as a millimeter-wave VNA extension module provide by Oleson Microwave Labs. The measurements were calibrated using the LRRM algorithm provided by the WinCal software from Cascade Microtech, and the standards from Picoprobe (WR-5, for G-band). The RF probes were with GSG configurations and 100 µm pitch provided from Picoprobe. Each measurement was made with 401 data points using 3 for averaging factor in a 10 kHz IF bandwidth.

As can be seen in Figure 3.119 and Figure 3.120, the transmission lines behave in a similar manner above 140 GHz. The attenuation tends to saturate at high frequencies and the phase velocity remains constant all along the frequency. It is interesting to note that the imaginary *Zc* approaches zero while real *Zc* is independent of frequency. This indicates that the characteristic impedance is determined by *L* and *C*. In a sense, the high frequency will make the metallic nanowires behave like conventional transmission lines at low frequency.

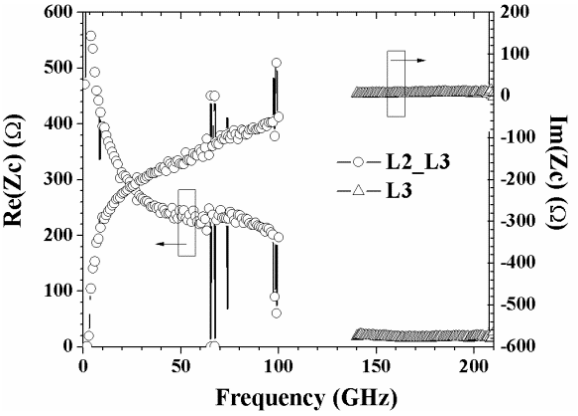


Figure 3.119 Experimental *Zc* of sample No.2 up to 210 GHz

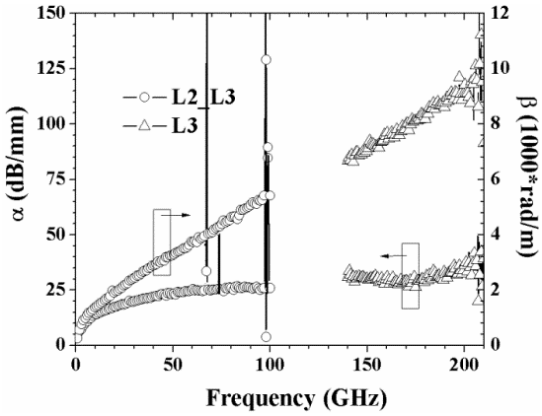


Figure 3.120 Experimental γ of sample No.2 up to 210 GHz

3.4 Conclusion

In this chapter, the broadband transmission characteristics of individual and multiple metallic nanowires were reported by means of a CPW platform on a standard silicon substrate. Different linewidth ranging from 8 µm to 100 nm and thickness from 500 to 100 nm were analysed. Most of these nanowires exhibit characteristic impedances much higher than 50 Ω. Some interesting properties were found. It was observed that the characteristic impedance of a single nano-line reduces as increasing frequency. At a certain frequency above (about 140 GHz), *Zc* approaches to a fixed value, behaving as a loss less line. This also means that the issue of impedance mismatching can be overcome by increasing operating frequency. Naturally, this frequency depends on *R*, *L*, *C* and *G* of the nanoline. Meanwhile, attenuation increases with increasing frequency. However, it appears that attenuation becomes less frequency-dependent above 140 GHz. The corresponding loss parameter *R* is a fixed value across the frequency range, suggesting that skin effect is ineffective. Perhaps the most important observation is the phase velocity. The dimensional scaling results in a significant latency in wave propagation. The proposed model agrees very well with the experiments, suggesting that quasi-TEM propagation prevails in these nanowire devices. However, the apparent discrepancy observed between the theoretical and experimental values was observed for the smallest nanowire having a linewidth and thickness below 100 nm. It is likely that quantum transport effect (L_K and C_Q) begins to manifest in the nanowire with such critical cross-sectional area.

Due to the high resistivity, nanowires should be only reserved for short-distance transmission. Multiple nano-line devices were then proposed to alleviate the technological challenge raised due to high conductor losses. It was found that RLGC parameters scale effectively with the numbers of nanowires (*N*). The effective *R* remains irrelevant to the frequencies and decreases almost linearly as *N* increases. The characteristic impedance and attenuation can therefore be improved. Specifically, in the case of a 100 nm wide and thick nano Au wire, it was observed that the attenuation was reduced from 60 to 30 dB/mm at 100 GHz by just adding four more wires in parallel. Such characteristic makes multiline device competitive to the state-of-the-art lines. On the other hand, the phase constant clearly drops when more wires are included. That is to say the slow wave propagation effect becomes less impressive in a parallel nanowire system. In addition, mutual interaction exits between parallel nanowires. By increasing the distance between the wires, it is also possible to reduce

the characteristic impedance at the cost of an increase in the attenuation. If taking into account all the design parameters (the linewidth, thickness and the numbers of nanowires, the interline distance), one can imagine possible applications such as phase shifters or nano-resonators by implementing metallic nanoscale transmission lines. As it turns out that the physical behaviour of metallic nanowires are quite similar to those of metallic CNTs.

Another focus in this chapter is to develop a de-embedding technique that could leverage the accuracy of the extracted transmission line characteristics. Due to extremely small transmission signal and high impedance mismatch attributed to nanowires, parasitic effects need to be handled with care. In this chapter, the effects of contact impedance and pad-to-pad coupling were discussed. As the importance of parasitics depends strongly on the frequency response, it is suggested that different de-embedding procedures should be used according to the frequency of analysis. Nevertheless, to achieve a successful nanoscale RF characterization, test structures should be designed to avoid parasitics. This includes minimizing the pad-line discontinuities, pad-to-pad coupling, and extra substrate loss as well as contact impedance.

Chapter 4

Nanocale On-chip Integrated Millimeter Wave Antennas on Various Substrates

Integration of antennas with RF electronics on one chip has received great attention since the past ten years. It has been regarded as a potential solution to resolve the bottleneck for signal transmission in future development of ultra-large scale integration (ULSI) or system-on-chip [80]. The RF clock distribution using integrated antennas was developed by Floyd et al. It largely reduces the chip area used in interconnection and virtually eliminates the dispersion problem [81]. The concept of using integrated antennas is also extended to wireless chip area network, namely data communication between chips (inter-chip) or within a chip (intra-chip) [82]. Thanks to the recent development in silicon-based monolithic integrated millimeter-wave circuits, small antennas can be integrated with a system on a single chip using standard CMOS technology, such as 60 GHz application. As the operating frequency of RF circuits continues to increase, CMOS transceiver design has already been implemented in the 90-170 GHz range [83]. RF signals will require an antenna size that is comparable to its wavelength. As an example, a quarter-wave antenna for operating frequency at 90 GHz is only about 240 μm long when integrating on silicon. The lengths are easily scaled. But to be compatible with a miniaturized system, all dimensions must be scaled. This means that the thickness and width of antennas should also be close to nano-metric scale. Integrated antennas can benefit from the increasing processing capability to be compatible with nanoscale communication networks. However, integration with such miniaturized antenna has not yet come in to the picture due to the fact that antenna performance deteriorates severely because of losses in metal layer as well as in the conventional silicon substrate (resistivity = 5~10 Ω-cm) [41]. These are the fundamental limitations of material characteristics for operation at RF frequencies. Different solutions were proposed for minimizing substrate losses, such as integration with high resistivity silicon substrate [84] or Si-on-quartz (SOQ) [85]. However, little work has been carried on miniaturized on-chip antenna with a target frequency above 60 GHz. In this work, the effect of small and thin metal lines on wireless signal transmission in various kinds of substrates will be examined to understand their characteristics and limitations. The research was made using dipoles and planar inverted–F antenna (PIFA), two most commonly used and easily implemented planar antennas, in the frequency range of 1-110 GHz and 140-210 GHz. This study is meant to provide a glance of the state-of-the-art and evaluate the potential in dimensional scaling with regard to short-distance wireless communication.

4.1 Past Work in On-chip Integrated Antennas for Millimeter Wave Applications

Previous researchers have reported on-chip antennas using CMOS process for operating in the 60 GHz band for wireless personal area network (WPAN) applications. In 2008, Guo and Chuang have realized a planar meander-line inverted–F antenna on standard silicon substrate [40]. The antenna was fabricated with a 0.18-µm CMOS process. The chip size was given as 0.815×0.706 mm^2. The transmission gain was measured with a probe station and network analyser. The maximum gain they found was -15.7 dB at 60 GHz. Using Ansoft HFSS simulator, a radiation efficiency of 10% was obtained. At the same year, Hsu et al. reported a CPW-Fed Yagi antenna using standard 0.18 µm CMOS technology [86]. The maximum power gain was measured as -10.6 dBi at 60 GHz (dBi is the unit for the relative power gain of an antenna compared with a lossless isotropic source. The negative power gain suggests that it probably includes conductor, substrate or impedance matching loss [87]. More information about the antenna power gain can be found in Appendix A). The simulated antenna radiation efficiency was about 10%. The chip size was 1.1×0.95 mm^2. With the same technology, these same authors have also implemented a triangular monopole antenna, reported a maximum gain of -9.4 dB with radiation efficiency of 12% [88]. In 2012, Titz et al. presented the design and measurement of a 350 µm long IFA and a 1 mm long dipole antenna integrated at Metal 6 in the BEOL (Figure 1.4) having thickness less than 1 µm with 130 nm CMOS technology. Their individual radiation pattern was measured. A maximum gain of -8 dBi and -14 dBi were obtained, respectively. The simulated efficiency was found to be 10% [89]. The radiation efficiency is relatively poor, which unfortunately is the typical performance reported to date. For comparison, typical radiation efficiency for antennas in free space is in the order of 70% or more. Not to mention that the physical dimension (width and thickness) of these antennas is far from nanoscale level. The lossy substrate is mainly responsible for the power dissipation, making them less competitive than chip-to-board transition or low loss transmission lines.

The electromagnetic coupling can be performed via waves radiated into space and waves guided by layered media. Therefore, by optimizing the properties of the substrate, it is possible to maximize the antenna gain and minimize the substrate loss. Depending on applications, small-size antennas are also capable for short-range wireless-interconnections. They should be designed to launch effectively surface waves rather than space wave for short distance communication. Zhang has evaluated the gain for intra-chip communication in the frequency domain from 10 to 110 GHz for a 1 mm long monopole antenna pair using aluminium layer of 2 µm thickness and 10 µm width on both low and high resistivity silicon substrate. They have observed a high S_{21} window close to -20 dB in 15 to 30 GHz and 25 to 60 GHz at a separation distance of 5 mm on the high resistivity Si substrate [90]. On the contrary, poor antenna characteristic was found on the low-resistivity Si. Through time-domain analysis, they further concluded that surface wave was the dominant path of the received signal. For the similar application, Triantafyllou et al. demonstrated a -10 dB in S_{21} for a 2 mm long dipole pair fabricated on SOI silicon substrate (on top of a high resistivity silicon substrate) at a distance of 2.5 mm [91]. These antennas were fabricated in Metal 6 in the BEOL with linewidth close to 10 µm in 130 nm CMOS technology. The antenna was designed resonating at 30 GHz. The wave propagation mechanism for intra-chip communication has been investigated by Yan and Hanson [92]. It was found that with a

guiding layer, surface wave propagation can be effectively enhanced to achieve higher gain. In the work of He et al., a 0.36 mm thick diamond layer was inserted between the silicon substrate and the heat sink [93]. The transmission gain of a 2 mm long and about 2 µm thick dipole pair on a 100 Ω-cm Si substrate can reach -6.8 dB at 26 GHz with a separation distance of 1 mm. It is interesting to note that they have observed no obvious gain improvement between the dipole pair with different widths (5, 10, 30 and 100 µm) when frequency exceeded 30 GHz.

Indeed, no realization of metallic nanoscale on-chip antennas for millimeter-wave frequencies was found in the literature since they are considered intuitively poor antenna candidates. While the applications below and around 60 GHz were well explored, the picture for the frequency above remains sketchy. The utility and value of these nanoscale antennas remains open for discussion. After all, as the CMOS device dimension continues to scale down, operating speeds and cut-off frequencies of CMOS devices will exceed 100 GHz in the near future, this will inevitably apply for antennas and other radiation elements in integrated circuits for on-chip and chip-to-chip communication [94].

4.2 Design of the Test Structures

Two kinds of antenna architecture were adopted in this study. They are dipoles and inverted-F antennas (The basics of dipole and inverted-F can be found in Appendix A). The dimensions of the antennas were designed to cover a wide range of frequencies from 20 up to 140 GHz. Those operating at lower frequencies (below 60 GHz) can provide a reference to compare with the performance of the state-of-the-art on-chip antennas. Considering the strong attenuation in low-resistivity silicon substrate, different types of integrated substrate were implemented to better observe the characteristic of nanoscale antennas. The details are described in the following section.

4.2.1. On-Chip Dipole Antennas Integrated on Standard Silicon and Porous-Silicon Substrate (Test set No.1)

Dipole antennas are preferred for wireless chip area networks since they can minimize the noise and interference signal generated by other circuits, making them a proper candidate for short distance signal transmission between ultra-large-scale integrated circuits (ULSIs). Figure 4.1 shows the geometry of the designed on-chip planar dipole fed by a slot line. For dipoles, the total length ($L = 2 \cdot Ld + Ls$) is about a half wavelength of the operating frequency. Dipoles are easily controlled and realisable antennas. It is known that the distance of the gap (*Ls*) and the length and the width of the feed line (*Lt* and *Wt*) have a strong influence on the impedance match of the antenna [95] [96]. In principle, they should contribute only a slight variation in the resonant frequency.

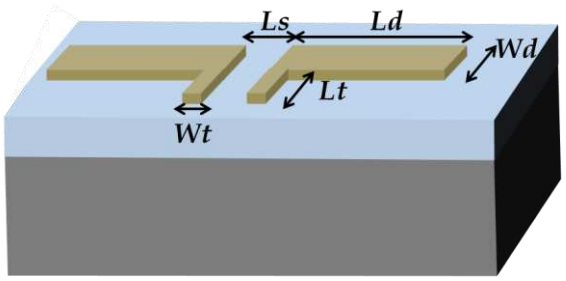


Figure 4.1 Geometry of an on-chip dipole antenna on top of the dielectric layer (blue) and silicon substrate (grey)

In this test set, the intention is to characterize small-size dipole antennas integrated on porous silicon substrate. Porous Si substrate technology has been demonstrated to improve the performance of transmission lines up to the mm-wave range as result of its low dielectric losses [97]. Porous silicon layer can be locally formed with a thickness reaching up to 200 μm. Two sets of dipoles were designed. Most importantly, it is compatible with standard CMOS processes, making it attractive to be integrated with RF passive devices. Each has two dipoles facing each other with a separation distance *R* (Figure 4.2). The geometry parameters are summarized in Table 4.1. In addition, another test set with the same design was fabricated on a standard silicon substrate of low resistivity (1-10 Ω.cm). The fabrication was realized in the Institute of Microelectronics (IMEL), NCSR Demokritos, Athens. It should be noted that this cooperation was within the framework of Nanofunction (Network of Excellence).

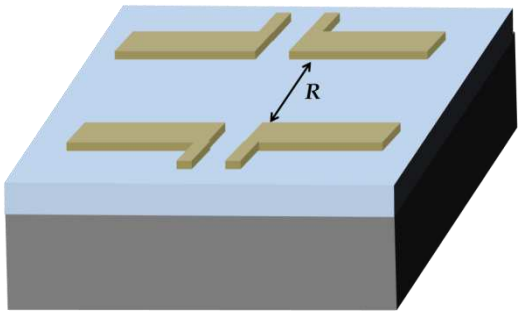


Figure 4.2 Schematic of a dipole pair facing each other at a distance *R*

Table 4.1 Geometric parameters of the on-chip dipole antennas (Test set No.1)

Sample No.	Ld (μm)	Wd (μm)	Lt (μm)	Wt (μm)	Thickness (μm)	Ls (μm)	R (μm)
1A	1000	4	20	5	0.25	50	1000
1B	1000	3	250	50	0.25	50	1000
1C	500	2	80	50	0.25	50	1000
1D	400	2	93	5	0.25	50	7000

4.2.2. On-Chip Dipole Antennas Integrated on High-Resistivity Silicon Substrate (Test set No.2)

Dipole antennas with even smaller geometries were further implemented on oxide–isolated high resistivity silicon to examine antenna properties. The operation range was designed closer to millimetre wave range. The antenna structure was first tested in ADS Momentum,

providing an estimation of transmission performance. The geometric parameters of the designed pairs are listed in Table 4.2. It can be noticed that the thickness of these dipoles is 0.1 µm. The arm length varies from 400 to 200 µm. The separation distance was reduced to 700 µm to improve the transmission gain. An asymmetric dipole (sample No.2C) was included to study the effect of different excitation positions. The geometric configuration is illustrated in Figure 4.3. Meanwhile, the impact of length and width of the feed line was examined.

Table 4.2 Geometric parameters of the on-chip dipole antennas (Test set No.2)

Sample No.	Lds (µm)	Ldg (µm)	Wd (µm)	Lt (µm)	Wt (µm)	Thickness (µm)	Ls (µm)	R (µm)
2A[1]	400	400	2	40	2	0.1	14	700
2A[2]	300	300	2	40	2	0.1	14	700
2B	300	300	2	90	2	0.1	14	700
2C	300	100	2	40	2	0.1	14	700
3A[1]	300	300	1	40	2	0.1	14	700
3A[2]	200	200	1	40	2	0.1	14	700
3B	300	300	1	40	1	0.1	14	700

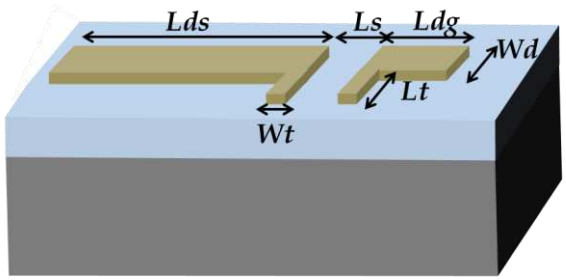


Figure 4.3 Geometry of an asymmetric on-chip dipole antenna on top of the dielectric layer and silicon substrate

4.2.3. On-Chip Planar Inverted-F Antennas Integrated on High-Resistivity Silicon Substrate (Test set No.3)

Another popular planar on-chip antenna is the planar inverted-F antenna (PIFA). It has been widely applied within the mobile phone market. The length of the PIFA is about a quarter wavelength of operating frequency. This provides the possibility to further reduce the size of the antenna at high frequencies. The layout of the designed inverted-F antenna is presented in Figure 4.4. Basically, a PIFA consists of a single line next to a ground plane and connected with a short circuiting line, and a feed line. A similar design has already been adopted by other authors [98]. Such configuration is compatible with GSG probes, at the same time minimizing the radiation loss and coupling between the ground pads. It is noted that the distance between the feed line and the shorted line (*Ldg*) and their length (*Lt*) play an important role on impedance matching. Table 4.3 summarizes the geometric parameters of the tested antennas.

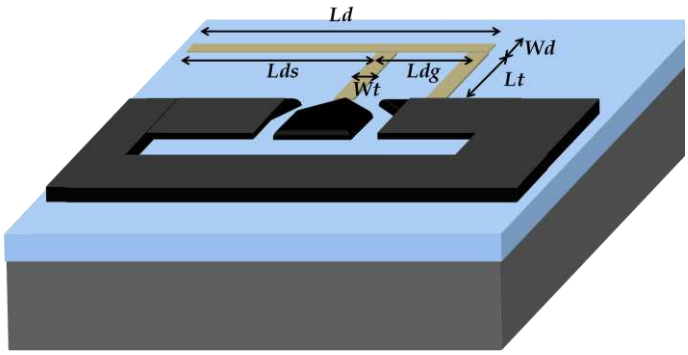


Figure 4.4 The layout of an inverted-F antenna with ground planes on top of the dielectric layer and silicon substrate

Table 4.3 Geometric parameters of the on-chip inverted-F antennas (Test set No.3)

Sample No.	Ld (μm)	Lds (μm)	Ldg (μm)	Wd (μm)	Lt (μm)	Wt (μm)	Thickness (μm)	R (μm)
4A[1]	500	400	100	2	100	2	0.1	700
4A[2]	400	300	100	2	100	2	0.1	700
4A[3]	300	200	100	2	100	2	0.1	700
4B[1]	500	300	200	2	100	2	0.1	700
4B[2]	400	200	200	2	100	2	0.1	700
4B[3]	300	100	200	2	100	2	0.1	700
4C[1]	500	400	100	2	40	2	0.1	700
4C[2]	400	300	100	2	40	2	0.1	700
4C[3]	300	200	100	2	40	2	0.1	700
4D[1]	500	400	100	1	100	2	0.1	700
4D[2]	400	300	100	1	100	2	0.1	700
4D[3]	300	200	100	1	100	2	0.1	700

4.3 Fabrication and Characterization

4.3.1. Test Structure Fabrication

Test set No.1: Dipole Antennas Integrated on Porous-Silicon and Standard Silicon Substrate

The porous silicon substrate was prepared as follows. First the porous Si membrane was locally formed on a highly-Boron doped silicon substrate with an adequate mask. The details can be found in [99]. The thickness of the membrane is 150 μm with an estimated permittivity close to 3.5. Next, a 500 nm thick TEOS silicon oxide (Tetraethylorthosilicate) was deposited on top of it. The antenna structures and the RF pads consist of a single Aluminum (Al) layer with 250 nm thickness. The E-gun evaporator was used for metal deposition. They were fabricated through standard lithography and lift-off method. The dimension of the RF pads was 100 μm in length and 50 μm in width with a distance between pads being 50 μm. They are designed for 100 μm-pitch GSG probes. In addition, another batch of antennas was

realized on a low-resistivity silicon wafer. Just like the porous silicon substrate, a TEOS layer with 500 nm thickness was deposited for signal isolation. It should be noted that the thickness of the Si substrate is around 500 µm. Therefore, after the formation of the porous silicon layer, there should remain approximately 350 µm thick silicon underneath.

Test set Nos.2 and 3: Antennas Integrated on Oxide-Isolated High-Resistivity Silicon Substrate

A commercially available high-resistivity silicon wafer was used as substrate for this test set of antennas. The specifications are P-type, Boron doped with a minimum resistivity over 2000 Ω.cm and a thickness around 525 µm. A 500 nm PECVD oxide was first deposited before fabricating the antenna patterns. Unlike the procedure mentioned earlier, antennas were fabricated in a separated step before defining the RF pads. Electron beam lithography (EBL) and lift-off method (PMMA 950 K 4%, 0.3 µm thick) were applied to achieve the 100 nm thick Cr-Au dipoles and PIFA structures (90 nm thick Au over 10 nm thick Cr). After this process, we proceeded to realize the RF pads by standard lithography and lift-off method (AZ5412E as resist, 1.3 µm thick). The RF pads consist of a single Al layer with 500 nm thickness. Figure 4.5 to Figure 4.9 show the top view of the fabricated dipole antennas and PIFA under optical microscope. The antennas were designed in pairs and placed parallel to each other at a specific distance *R*. As can be seen in the figures, the tapered transition adopted in the signal pads is to minimize the effect of discontinuity. In the case of the dipole antennas, the tapered design is also necessary for the ground pads allowing a closer distance between the arms (*Ls*). The RF pads arrangement is GSG configuration with the pitch being 50 µm. Given the large surface area of the ground plane, the RF pads of the PIFA are compatible with 50 µm as well as 100 µm pitch GSG probes. Figure 4.10 shows the connection between the RF pads and the antenna. A considerable overlap between the two components can be seen at the contact. Meanwhile, there is a noticeable step change due to different metal thickness. Note that the marks observed on the pads are due to the probing.

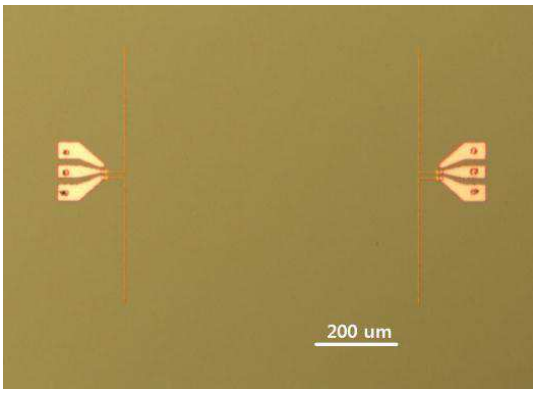


Figure 4.5 Photo of a dipole pair with pads integrated on oxide-coated high-R Si wafer

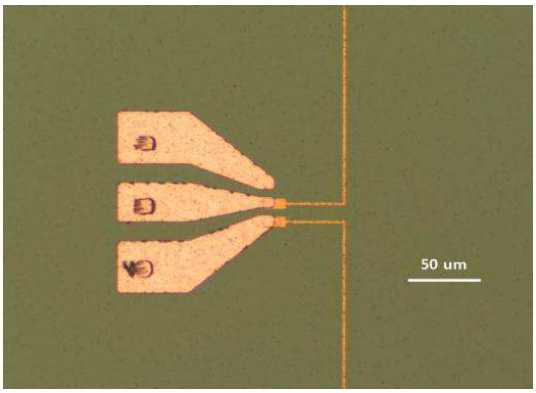


Figure 4.6 Photo of a single dipole with pads integrated on oxide-coated high-R Si wafer

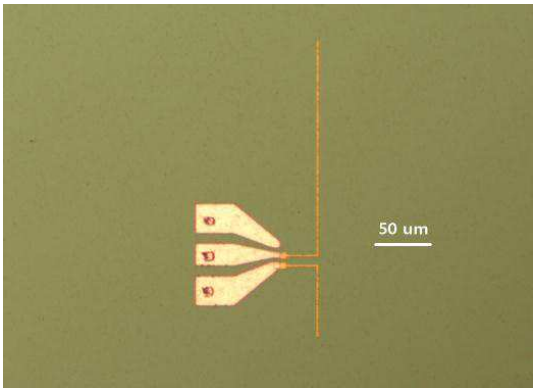


Figure 4.7 Photo of an asymmetric dipole with pads (sample No.2C)

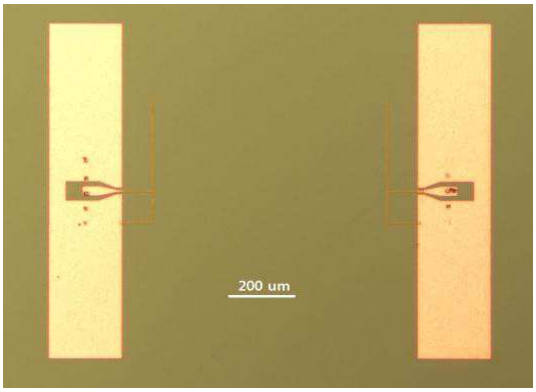


Figure 4.8 Photo of a PIFA pair with pads integrated on oxide-coated high-R Si wafer

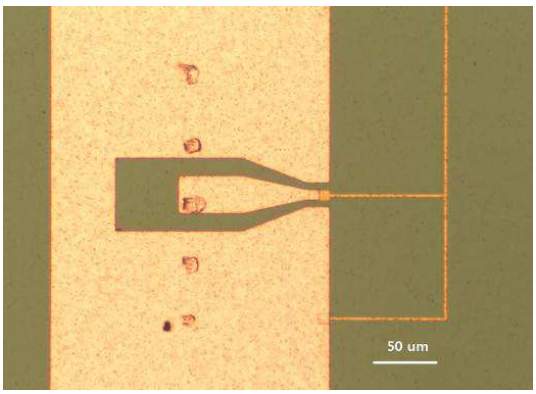


Figure 4.9 Photo of a single PIFA with pads integrated on oxide-coated high-R Si wafer

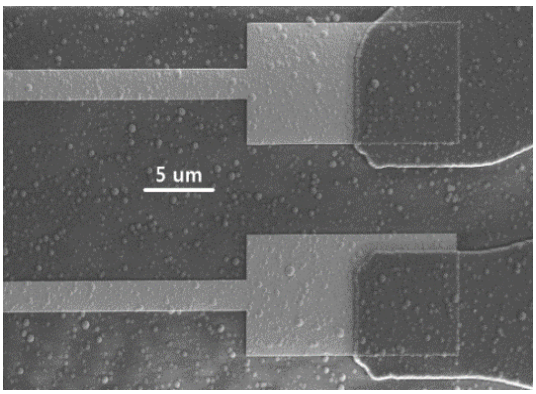


Figure 4.10 SEM image showing the connection between the pads and the antennas

4.3.2. On-chip Antenna Characteristics

Propagation Mechanism

An on-chip communication system with a multi-layer structure is known to have different wave propagation components: surface waves by the air-wafer surface, space waves via the air and guided waves within the layers [90]. Of all these components, the propagation channels through the surface wave and guided layer is expected to be most critical. The excitation of the surface wave can be either advantageous or disastrous, depending whether it can contribute to the main beam radiation. In some applications such as inter-chip communication or WPAN applications, surface wave power is even treated as losses, and it becomes increasingly important as the substrate thickness increases. Otherwise, it is a natural candidate for transmission enhancement in an intra-chip system. Through an optimization of the dielectric structure, more energy can be carried by surface waves, therefore contributing to the receiving signal. Yet, special attention needs to be paid to avoid destructive interference between the multiple wave components [92]. As the frequency increases, different modes of surface waves can be excited, namely TE and TM modes. The cut-off frequencies of these modes depend on the thickness and dielectric constant of the substrate, and can be evaluated using the equations below [91]:

$$\boldsymbol{fc = \frac{nc_0}{2d\sqrt{\varepsilon_r - 1}} \quad n = 0, 1, 2, \ldots for\ TM_n\ modes} \tag{4-1}$$

$$\boldsymbol{fc = \frac{(2n-1)c_0}{4d\sqrt{\varepsilon_r - 1}} \quad n = 1, 2, \ldots for\ TE_n\ modes} \tag{4-2}$$

where c_0 is the speed of light, d and ε_r are the thickness and the relative dielectric constant of the substrate. Considering a silicon substrate with a standard thickness of 525 µm, we can expect to see TE_1, TM_1, TE_2 and TM_2 in the frequency band of our analysis. Specifically, they occur at 43, 86, 130 and 172 GHz, respectively.

Radiation Efficiency

Radiation efficiency is a measure to tell how well an antenna can convert the receiving power to radiation power. There are several definitions of radiation efficiencies associated with antennas. In general, the overall efficiency is given as [87]

$$\boldsymbol{e_{total} = e_r e_{cd}} \tag{4-3}$$

where e_{total} is total efficiency, e_r is reflection (mismatch) efficiency and e_{cd} is antenna radiation efficiency. e_r and e_{cd} are calculated as follows:

$$\boldsymbol{e_r} = 1 - |S_{11}|^2 \tag{4-4}$$

$$\boldsymbol{e_{cd} = \frac{R_r}{R_r + R_L}} \tag{4-5}$$

where R_r denotes the radiation resistance and R_L is the loss resistance. Note that this equation only considers the losses within the antenna structure. The loss resistance consists of conduction and dielectric losses. e_{cd} can be difficult to compute but it can be determined by measuring the radiation pattern. Radiation patterns are graphical representations of electrometric power distribution in free space. Although the radiation pattern is not available in this work, an attempt was made to estimate the radiation resistance R_r to gain further insight into the capability of a single on-chip antenna irrespective of whether the radiation is in the air or inside the substrate. Assuming the feed line and the antenna are properly matched, the antenna impedance at the terminal can be given as:

$$\boldsymbol{Z_A = R_A + j \cdot X_A} \tag{4-6}$$

where R_A and X_A are the antenna resistance and reactance at the terminal, respectively. At resonance, the imaginary part would disappear. Then Equation (4-6) becomes $Z_A = R_A$. Since the term R_A is the sum of R_r and R_L, we get

$$\boldsymbol{Z_A = R_r + R_L} \tag{4-7}$$

With *S*-parameters measurement, the input impedance Z_{in} at the terminal can be determined using:

$$|S_{11}| = \frac{Z_{in} - Z_s}{Z_{in} + Z_s} \tag{4-8}$$

where Z_S is impedance towards the source (50 Ω in our case). We know that Z_{in} is also the impedance towards the antenna, hence should be equivalent to $R_r + R_l$ according to Equation (4-7). R_l can be roughly estimated by calculating the resistance of the conductor assuming that other losses such as dielectric losses are negligible. R_r can thus be obtained which can be an indicator of the antenna resonance efficiency.

4.3.3. Characterization Method

Antenna Transmission Gain Definition

Two-port *S*-parameters measurement is the most extensively used method to evaluate the transmission performance of integrated antenna pairs. An antenna pair placed face-to-face with a distance *R* can be tested immediately on the probe station. One antenna is used as a transmitting antenna and another as a receiving antenna. From free-space Friis power transmission formula, the maximum antenna power gain (in the central forward direction of the antenna) is given by [100]:

$$GtGr = G^2 = \left(\frac{Pr}{Pt}\right)\left(\frac{4\pi R}{\lambda}\right)^2 = |S_{21}|^2\left(\frac{4\pi R}{\lambda}\right)^2 \tag{4-9}$$

where G_t and G_r are the power gain of the transmitting and receiving antenna, respectively. In our case, G_t is equal to G_r since the two antennas are identical. $\boldsymbol{\lambda}$ is the free space wavelength at the operating frequency. This equation is valid for a free space environment. Typically, the figure of merit used to evaluate intra-chip antenna characteristics is G_a, known as the antenna transmission gain. It is calculated from two-port *S*-parameters, expresses as [101]:

$$Ga = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)} = GtGr\left(\frac{\lambda}{4\pi R}\right)^2 e^{-2\alpha R} \tag{4-10}$$

α represents the propagation losses in a lossy substrate. G_a also includes the mismatch losses S_{11} and S_{22}. If the impedance of the antennas matches with that of the test equipment, the transmission gain can be approximated by $|S_{21}|^2$ since $(1 - |S_{11}|^2)(1 - |S_{22}|^2) \approx 1$.

Description of the Measurement Setup

The on-wafer measurement consists of two range of frequency bandwidth. All the devices were tested at the IMEP-LAHC laboratory from 1 to 110 GHz. The test set Nos. 1 and 3 were further tested in VTT Technical Research Centre of Finland, Helsinki. The frequency range covers from 140 to 210 GHz. The procedure of the measurement is described in Chapter 3.

4.4 Results and Discussion

In the following section, the experimental *S*-parameters and the corresponding extracted antenna parameters are presented. Their characteristics with respect to the physical

parameters will be discussed. In addition, the simulated results obtained from ADS Momentum are compared

4.4.1. Test set No.1: Dipole Antennas Integrated on Porous-Silicon and Standard Silicon Substrate

Figure 4.11 and Figure 4.12 show the measured *S*-parameters as a function of frequency from test set No.1 on two different substrates. The *S*-parameters were de-embedded with an open device. The parasitics of the RF pads can then be subtracted. It is believed that the open de-embedding should be sufficient since the series resistance of the pads can almost be neglected as compared with the antenna structure. Note that an open device consists of the RF pads without any antenna structures. In the figures, S_{11} results are plotted next to S_{21}, located at the upper region of the graph. The resonance frequency can be identified where the phase of S_{11} is zero. For the same antenna design, it can be observed that the resonance frequency (denoted as f_0) is significantly higher on the porous silicon substrate than on the standard low-R silicon substrate. For example, sample No.1A demonstrates a resonance frequency about four times higher on the porous silicon substrate, as listed in Table 4.4. This is primarily attributed to the lower permittivity of porous silicon. We can refer to a simple estimation of f_0 for an integrated half wave length dipole based on the physical parameters, given by [102]:

$$f_0 = 0.47 \frac{c_0}{L\sqrt{\epsilon_{eff}}} \tag{4-11}$$

where c_0 is the speed of light and L is the total length of the dipole. ε_{eff} accounts the effective permittivity of the traveling wave. We know that the electromagnetic wave generated from the dipole travels inside the substrate as well as in the air. The relationship between the effective permittivity, the geometry and material parameters of an on-chip dipole can be found in [103]:

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[\left(1 + 12\frac{h}{w}\right)^{-1/2} + 0.04\left(1 - \frac{w}{h}\right)^2\right] \tag{4-12}$$

ε_r is the relative dielectric constant of the substrate. w is the width of the conductor while h is the thickness of the substrate. When h is much larger than w, ε_{eff} can be approximated as $\frac{\epsilon_r+1}{2}$. Using Equation (4-11), we can estimate the effective permittivity of sample No.1A on the porous silicon (denoted as 1A-P-Si), being about 2.2. As a consequence, we obtain a relative dielectric constant of about 3.4, which is not too far from our expected ε_r for the porous silicon layer (ε_r = 3.5). This also suggests that the silicon substrate below the porous silicon layer has little effect on the wave propagation. It is relevant to mention that the relative dielectric constant of silicon is about 12. In the case of 1A-Si, the estimated ε_{eff} is over 30. Such non-physical result in fact indicates that the resonance frequency is underestimated. A shift of the resonance peak was noticed towards lower frequencies of about 6 GHz after de-embedding with an open device while a shift of 1 GHz was observed for dipoles on the porous silicon substrate. This infers that the uncertainty introduced due the de-embedding is more pronounced on a lossy substrate.

Compared to sample No.1A, sample No.1B has a feed line of larger surface area. It was supposed to yield better impedance matching to compensate the reduction in conductor width. However, based on the calculated Z_{in}, this improvement is only observed on the low-R silicon

substrate. In addition, f_0 has been slightly modified. It can be seen that decreasing the dipole width from 4 to 3 µm has resulted in a drop by 10 dB in insertion loss on the porous silicon substrate but a less significant value by 3 dB on low-R silicon substrate was found.

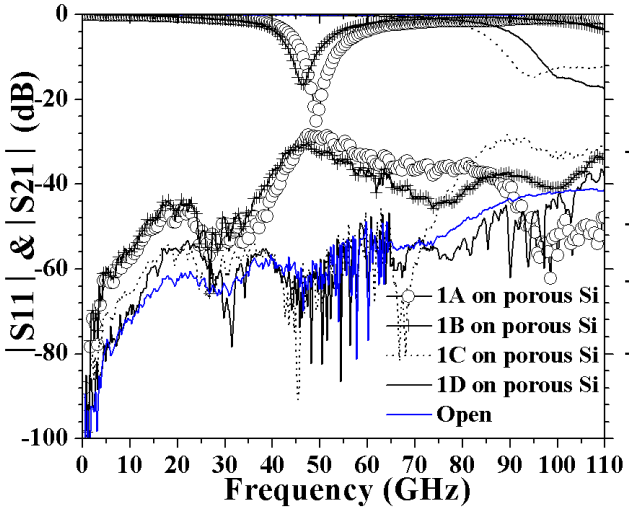


Figure 4.11 Experimental *S*-parameters of the dipoles on the porous silicon substrate. S_{11} is situated at upper level while S_{21} is at the lower level. Open represents the open device.

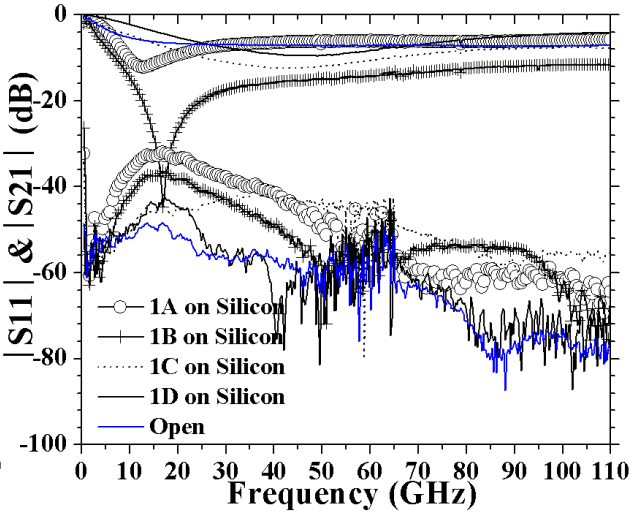


Figure 4.12 Experimental *S*-parameters of the dipoles on the low-R silicon substrate. S_{11} is situated at upper level while S_{21} is at the lower level. Open represents the open device.

Concerning sample No.1C, the length of the dipole has been reduced by half of the value from sample No.1A. It is not surprising to see that the resonance frequency increases by a factor of 2. The measured resonance frequency of 1D-P-Si is not obtained within the maximum range of the equipment which is 110 GHz as it has even shorter dipole length (L = 850 µm) while the one of 1C-P-Si is located at 105.9 GHz. The attempt to scale down the dipole linewidth may increase the conduction loss but it can be somewhat compensated through the reduction of dipole length. If R_L reduces while Z_{in} increases, this leads to an increase in radiation resistance. In a sense, the size reduction may be actually desirable if geometry of the dipole and feed line is optimized. The estimated radiation resistance is about 61.9 % of the total impedance for 1C-P-Si whereas for 1B-P-Si, it is 40.8 %. Although 1B-P-Si indeed has better reflection efficiency, the overall efficiency is lower. It is thus reasonable to see that at the same separation distance R, the transmission gain of 1C-P-Si is higher despite having a much smaller occupied area (wd = 2 µm, L = 1050 µm).

Over the whole frequency range, there is no sharp resonance dip found for 1C-Si and 1D-Si. The bandwidth of the antennas on Si is in general greater than those on porous silicon. Note that the bandwidth here is defined as the frequency range where $|S_{11}|$ is larger than -10 dB. Although the return loss may appear acceptable, 1C-Si shows a G_a value of -42.0 dB at a separation distance of 1 mm. This is attributed to the lossy substrate. After about 15 GHz, the transmission on low-R silicon substrate is heavily attenuated. This characteristic prohibits antenna applications at high frequencies. In contrast, porous silicon substrates, which demonstrate significant lower losses can be a good candidate for inter-chip antenna application at millimeter-wave frequencies. It should be noted that due to the huge distance between the pairs of 1D-Pi-Si and 1D-Si (7 mm), the insertion loss is almost identical to that of an open device from 30 to 110 GHz.

In principle, sample No.1C should have worse matching than sample No.1D due to the longer dipole length if the effect of feed line is deliberately ignored. Likewise, a feed line with a wider linewidth was designed in order to improve the matching. Interesting enough,

there is improvement in return loss only on low-R silicon substrate which is consistent to what we have discussed before. It is readily apparent that the dipoles fabricated on the porous silicon substrate are relatively insensitive to the different design of feed lines because of the high resistivity nature of porous silicon. This behaviour has also been observed in [85].

Table 4.4 Summary of the experimental result from Test set No.1. The values of S_{11} and S_{21} in the table were taken at the resonance frequency

Sample No.	1A-P-Si	1A-Si	1B-P-Si	1B-Si	1C-P-Si	1C-Si	1D-P-Si	1D-Si
f_0 (GHz)	49.2	12.8	46.2	16.9	105.9	42.9	>110	46.8
$\|S_{11}\|$ (dB)	-25.2	-12.3	-16.6	-44.7	-12.6	-12.5		-9.5
$\|S_{21}\|$ (dB)	-29.1	-33.7	-38.8	-36.4	-33.2	-42.5		-62
bandwidth (>10 dB, GHz)	6.6	8.5	4.9	>100	>20.3	40.5		x
Zin (Ω)	55.8	82.0	67.4	50.6	80.6	81.1		100.4
e_r (%)	99.7	94.1	97.8	100.0	94.5	94.4		88.8
R_L (Ω)	30.8	27.5	39.9	37.1	30.7	28.0		24.5
e_{cd} (%)	44.8	66.5	40.8	26.7	61.9	65.5		75.6
Ga (dB)	-29.1	-33.2	-38.6	-36.4	-32.7	-42.0		-61.0

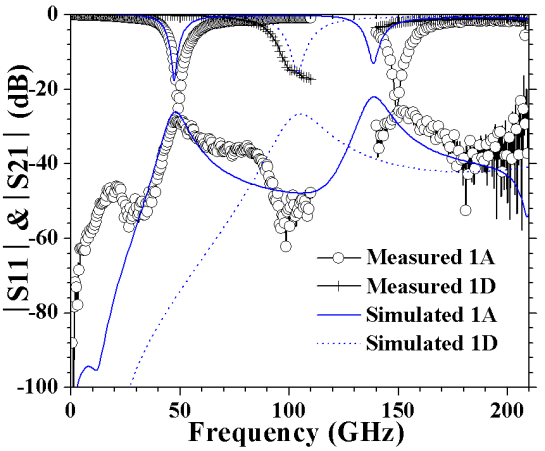


Figure 4.13 Measured and simulated *S*-paramters up to 210 GHz for sample Nos.1A and 1D on the porous silicon

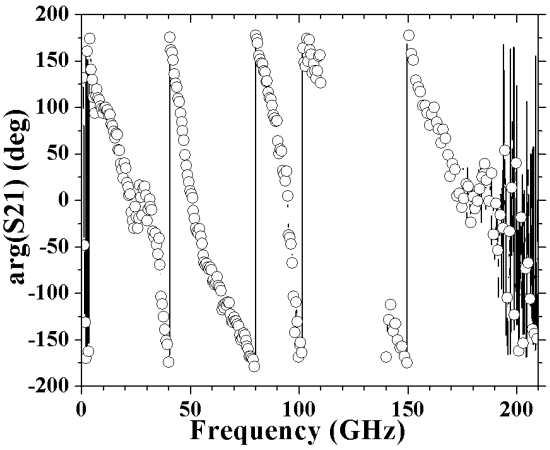


Figure 4.14 The experimental phase of S_{21} up to 210 GHz for sample No.1A

Figure 4.13 shows the measured and simulated *S*-parameters for 1A-P-Si and 1D-P-Si up to 210 GHz. Besides the primary resonance peak at 49.2 GHz, another sharp resonance peak is observed at 145 GHz. The performance of the antenna is reasonably good. The return loss and insertion loss are -14.9 dB and -30.0 dB, respectively. The measured phase response of S_{21}, shown in Figure 4.14, is linear or nearly linear, suggesting that there is a dominant mode supporting the signal propagation. This is usually more desirable. Otherwise, if there are multiple wave components in the field, the signal will be distorted due to frequency dispersion [92]. The resonance frequency of 1D-P-Si is out of the measured frequency range but it is expected to occur between 110 to 140 GHz. Both measured and simulated data show similar trends, although there is discrepancy in the level of magnitude and f_0 is underestimated.

4.4.2. Test set No.2: Dipole Antennas Integrated on Oxide-Isolated High-Resistivity Silicon Substrate

Figure 4.15 and Figure 4.16 show the measured *S*-parameters of the test dipoles. It can be seen that the transmission gain increases slowly in the frequency range between 30 to 60 GHz for all the dipoles. This shows that the surface wave begins to dominate the field. The wave component could be TE_1 mode since its cut-off frequency is at 43 GHz (derived from Section 4.3.2). Above this range, a high S_{21} window can be seen which favours signal transmission [90]. Table 4.5 lists the experimental *S*-parameters results of the dipoles. Likewise, the effective permittivity can be estimated using Equation 4-11. If sample No.$2A^2$ is considered, we can obtain ε_{eff} equal to 6, which makes the dielectric constant of the high-R silicon wafer being about 11.

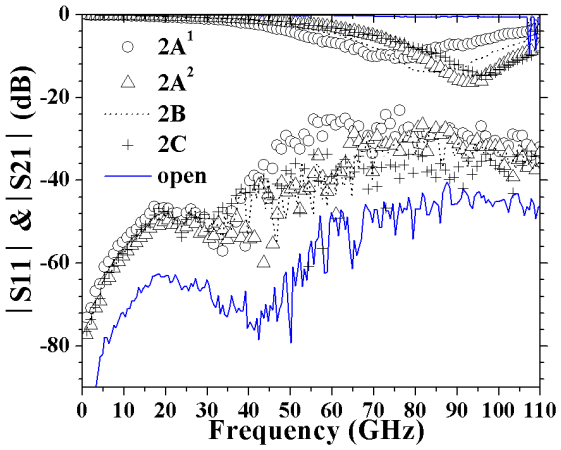


Figure 4.15 Experimental *S*-parameters of the dipoles on high-resitivity silicon substrate

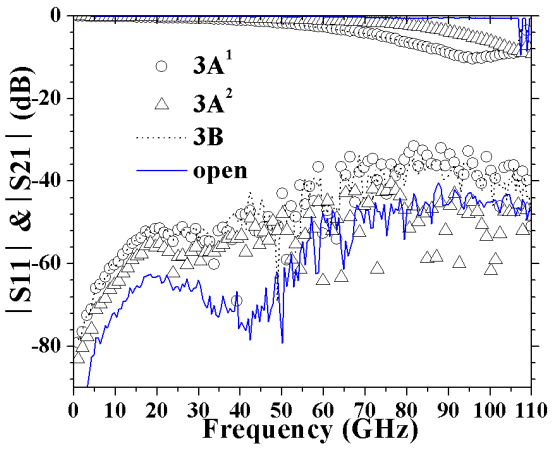


Figure 4.16 Experimental *S*-parameters of the dipoles on high-resitivity silicon substrate

Table 4.5 Summary of the experimental result from Test set No.2

Sample No.	$2A^1$	$2A^2$	2B	2C	$3A^1$	$3A^2$	3B
f_0 (GHz)	77.8	93.7	86.6	96.8	100.5	>110	98.6
$\|S_{11}\|$ (dB)	-10.0	-16.4	-13.8	-14.5	-9.9		-8.8
$\|S_{21}\|$ (dB)	-25.9	-31.9	-33.9	-33.7	-41.3		-40.2
bandwidth (>10 dB, GHz)	x	23.5	22.9	21.5	x		x
Zin (Ω)	96.2	67.8	75.7	73.2	97.0		107.0
e_r (%)	90.0	97.7	95.8	96.5	89.8		86.8
R_L (Ω)	59.7	46.6	53.2	46.7	85.8		91.0
e_{cd} (%)	37.9	31.3	29.7	36.2	11.5		15.0
Ga (dB)	-25.0	-31.7	-33.5	-33.4	-40.4		-39.0

Sample No.$2A^1$ has the highest gain among all the tested structures. When separated by a distance of 700 µm, the 814 µm long and 2 µm wide dipole pair shows a transmission gain of -25.0 dB at 77.8 GHz. Radiation loss accounts for 37.9% of the total input impedance. It is obvious that the conduction losses increase significantly as result of the small metallization thickness (0.1 µm). When the dipole size reduces down to 614 µm, f_0 can reach about 93.7 GHz as observed in sample No.$2A^2$. The gain degrades by 6.7 dB although we get a better impedance matching at resonance with a broad impedance bandwidth. Only 31.3% of the total

impedance takes parts in the radiation. In addition, it appears that the feed line should be made as short as possible to have a better matching. Sample No.2B has a feed line twice as long as that of sample No.2A[2]. It can be noticed that the impedance is slightly worse and the resonance frequency has shifted. Sample No.2C is an asymmetric dipole, having one arm being 300 µm and another shorted one being 100 µm. It has a similar performance as sample No.2A[2], if not better. This type of design is in favour of size reduction without sacrificing too much the performance.

The dipole width of Sample No.3A[1] is scaled down to 1 µm. This has led to a larger impedance mismatching and a slight increase in resonance frequency. It is not surprising to see that the transmission gain decreases substantially since the proportion of the total power could dissipate in radiation falls to 11.5%. Further decreasing the linewidth of the feed line could make the antennas more compactible for integrating with nano-devices. Sample No.3B, having its feed line width reduced to 1 µm, has a poorer matching. Yet, the energy that could possibly distribute to radiation is about 15 %. The transmission gain is as good as sample No.3A[1]. Figure 4.17 shows the experimental phase of S_{21} of sample No.2A[2]. The phase has a linear profile above 65 GHz. Therefore, at resonance, the signal transmission between the two dipoles occurs through a dominant mode.

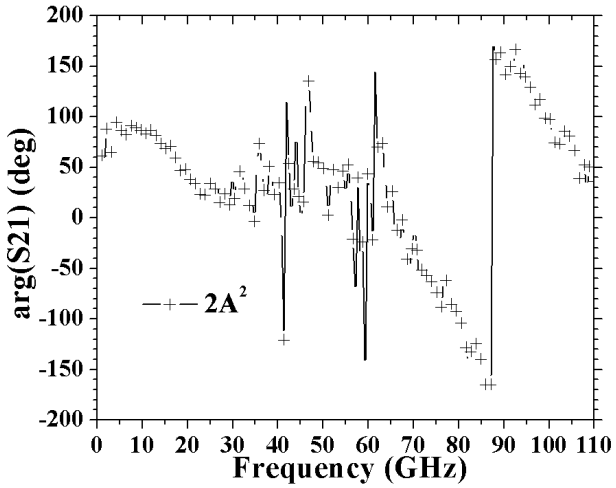


Figure 4.17 The experimental phase of S_{21} up to 110 GHz for sample No.2A[2]

The simulation was performed up to 210 GHz for sample Nos. 2A[2] and 3A[1] using ADS Momentum. A demonstration of simulation setup can be seen in Figure 4.18. As shown in Figure 4.19, the theoretical resonance frequency is approximately the same as the experimental one within an error of 1%. However, there is noticeable discrepancy in the magnitude of S_{11} at resonance by as much 14.0% for sample No.2A[2] and 18.1% for sample No.3A[1]. Due to the size of the antenna, only the first resonance frequency appears in the frequency band of analysis.

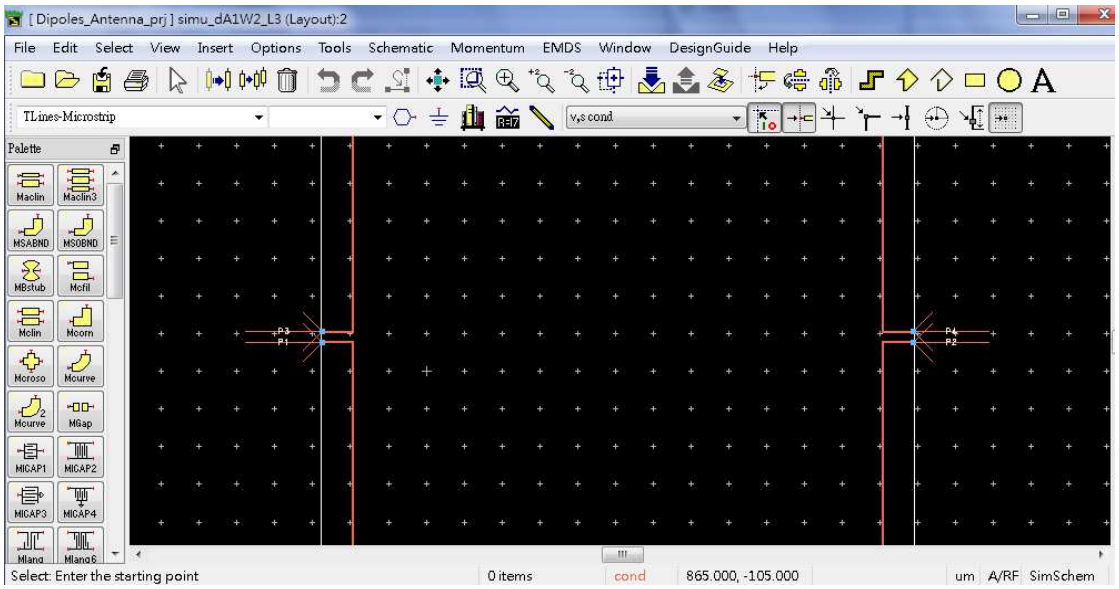


Figure 4.18 Simulation setup of an dipole pair in ADS Momemtum

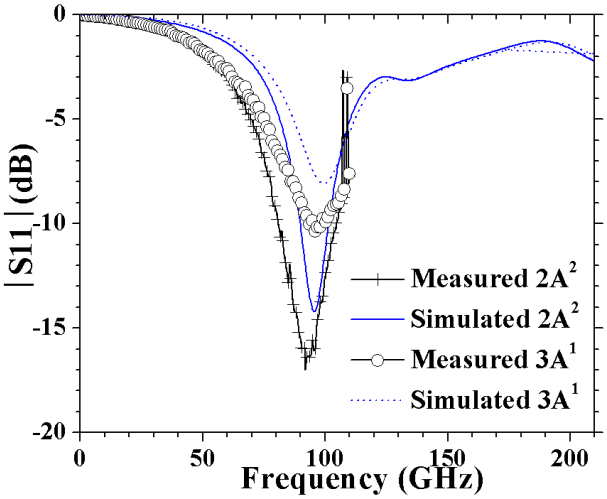


Figure 4.19 Measured and simulated S_{11} up to 210 GHz for sample Nos.$2A^2$ and $3A^1$

4.4.3. Test set No.3: PIFA Integrated on Oxide-Isolated High-Resistivity Silicon Substrate

Figure 4.20 to Figure 4.23 shows the experimental *S*-parameters of the planar inverted-F antennas with various dimensions up to 210 GHz. Each figure contains three traces representing different antenna length (500, 400 and 300 µm). It is important to emphasize that no de-embedding procedure was applied since the ground plane was embedding with the RF pads. It would be more ideal if we could isolate the probing pads from the ground planes. Unfortunately, no such test structure was available in our experiment. Hence, the analysis is based on the CPW line, the ground plane and the PIFA itself as a whole component. Similar to the on-chip dipoles, a significant increase of transmission coefficient S_{21} is observed from 30 to 50 GHz which corresponds to the excitation of TE_1 mode. Likewise, there is a high S_{21} window above 50 GHz. Besides, ripples can be observed in the frequency response of S_{21}. This is likely due to the appearance of parasitic propagation modes near to the RF pads. The

origin of this phenomenon is unknown. But it is most probably related to the behaviour of high resistivity silicon substrate as this issue did not come about on low resistivity Si. It is known that oxidized high resistivity substrate suffers from parasitic surface conduction (PSC) effect due to the accumulation of charges beneath SiO_2/Si interface [104].The crosstalk between the pads could potentially interfere with the main propagated signal. The effect is particularly pronounced in this case because the ground plane occupies a large surface area. Despite of this, we can identify the contribution of the antenna by comparing its signal level with that of the open structure. One can see that above 140 GHz, S_{21} is very little affected by the addition of the antenna. It appears that signal transmission is mainly attributed to pad-to-pad coupling. Further supporting this observation, although Sample No.4B^3 exhibits a resonance frequency at 170.4 GHz, the impact of the antenna to S_{21} is almost negligible.

In general, the transmission gain of the PIFA is relatively good considering their limited size. Table 4.6 lists the results of all test PIFAs. Sample No.4A^1 has a length of 500 µm. with the corresponding gain being about -28.9 dB. When line length reduces to 400 µm as demonstrated by sample No.4A^2, f_o is increased by 22.8% while the gain and impedance matching are only slightly suffered. It was found that the impedance matching can be easily controlled by changing the length of the feed and shorted line or optimizing the space between them. If we examine sample No.4B^1, we see that increasing the distance between feed and shorted lines from 100 to 200 µm has reduced slightly the reflection coefficient. But by doing so, the gain is sacrificed and the resonance frequency is also affected. On the other hand, the impedance matching is substantially improved when the feed line length reduces by half as observed in sample Nos.4C^1 and 4C^2. The determination of transmission gain in relation to different features is difficult due to the rapid fluctuation in signal with frequency. Non-linear profile in the phase can be observed as shown in Figure 4.24, suggesting interference of multiple signal propagations.

Figure 4.23 shows the *S*-parameters of sample No.4D in various lengths. These samples have almost the same feature as sample No.4A series except that the width of the radiating element (*Wd*) was reduced to 1 µm. As expected, the reflection coefficient is higher. Similar transmission gain, if not better, can be obtained when operating at resonance while the resonant frequency is slightly affected.

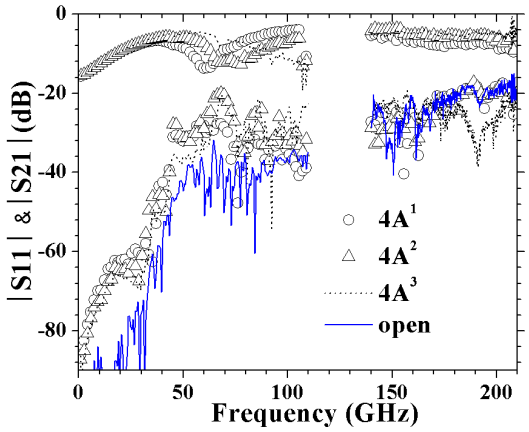


Figure 4.20 Experimental *S*-parameters of sample Nos.4A^1, 4A^2 and 4A^3 on high resistivity silicon substrate

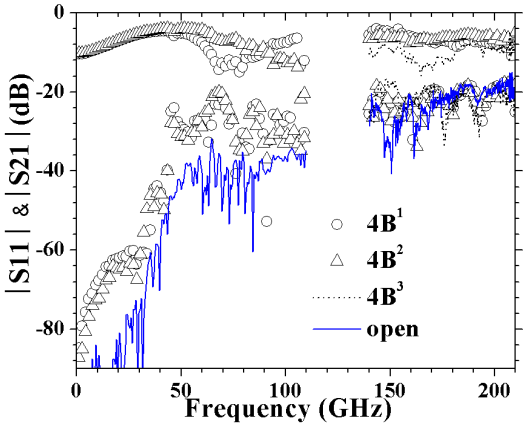


Figure 4.21 Experimental *S*-parameters of sample Nos.4B^1, 4B^2 and 4B^3 on high resitivity silicon substrate

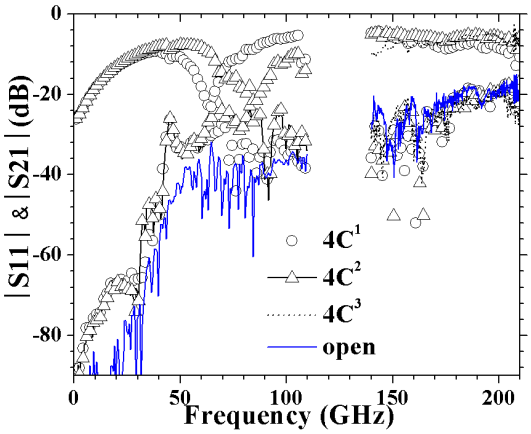


Figure 4.22 Experimental *S*-parameters of sample Nos.4C[1], 4C[2] and 4C[3] on high resitivity silicon substrate

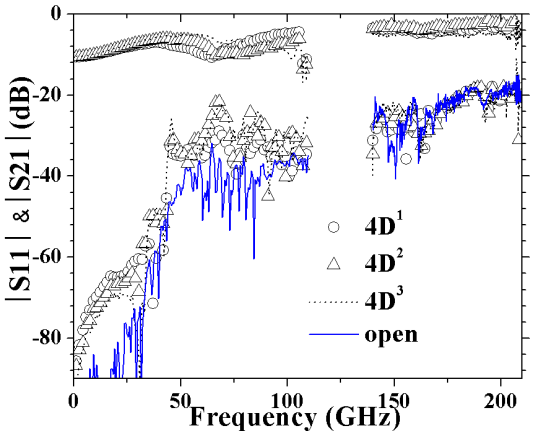


Figure 4.23 Experimental *S*-parameters of sample Nos.4D[1], 4D[2] and 4D[3] on high resitivity silicon substrate

Table 4.6 Summary of the experimental result from Test set No.3. The values of S_{11} and S_{21} in the table were taken at the resonace frequency

Sample No.	4A[1]	4A[2]	4A[3]	4B[1]	4B[2]	4B[3]	4C[1]	4C[2]	4C[3]	4D[1]	4D[2]	4D[3]
f_0 (GHz)	62.6	81.1	110-140	78.4	110-140	170.4	64.2	84.9	110-140	65.3	80.6	110-140
$\|S_{11}\|$ (dB)	-13.8	-11.3		-14.5		-14.8	-23.6	-21.3		-10.6	-10.0	
$\|S_{21}\|$ (dB)	-29.3	-30.8		-35.6		-19.6	-31.4	-26.7		-30.0	-30.3	
bandwidth (>10 dB, GHz)	14.2	21.3		26.7		25.6	35.4	40.3		6.5	x	
Zin (Ω)	75.7	87.4		73.2		72.2	57.1	59.4		91.9	96.2	
Ga (dB)	-28.9	-30.1		-35.3		-19.3	-31.4	-26.6		-29.2	-29.4	

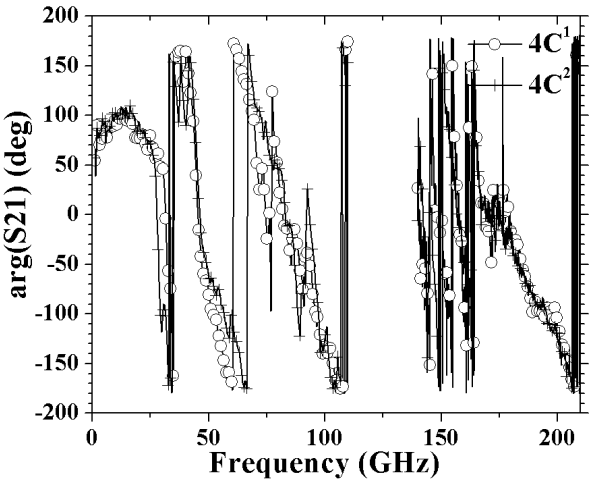


Figure 4.24 The phase of S_{21} for sample Nos.4C[1] and 4C[2]

4.5 Conclusion

The transmission characteristics of nanoscale on-chip antennas were investigated up to 210 GHz. Dipoles and inverted-F antenna pairs were considered in this study. Various dimensions were tested. The thickness of these antennas ranged from 250 down to 100 nm with minimum length and linewidth being 300 µm and 1 µm, respectively. The antenna pairs were integrated

on a single chip with a separation distance about 1000 µm or less. They were realized on three kinds of substrates, including oxide-coated low resistivity Si wafer and oxide coated high resistivity Si wafer as well as porous silicon coated Si wafer. Two-port *S*-parameter measurement was applied for characterization. Apart from the reflection and transmission coefficient, some basic antenna parameters were also examined resonance frequency, transmission gain, input impedance and bandwidth. Although no radiation pattern was measured, the radiation loss was estimated for evaluating the efficiency of the antennas.

It was shown that a low loss substrate is essential for millimeter-wave antenna application. Signal suffers severe attenuation above 40 GHz for those antennas realized on standard silicon substrates. Overall, integration with high resistivity Si substrate has better performance than porous silicon coated Si substrate in terms of transmission gain. Besides, the high dielectric constant of silicon allows considerable size reduction without an over increase in operating frequency. The transmission gains obtained with these miniaturized antennas are not so far from the typical values with a state-of-the art micro-sized antennas (less than -20 dB). In the case of the dipole test structure, a transmission gain of -25 dB at 77.8 GHz can be achieved with a 814 µm long, 2 µm wide and 100 nm thick dipole pair at a separation distance of 700 µm. Further decreasing the arm length to support even higher operating frequency leads to a reduction of radiation efficiency. It was demonstrated that the transmission gain was degraded to -31.7 dB at 93.7 GHz if the length of the dipole decreased to 614 µm although the reflection efficiency was improved. The feed line should be designed as short as possible for better matching. Its width can be scaled down at the same order as the dipole since the gain is little affected. However, the reflection coefficient is sacrificed. Thanks to the surface wave, signal transmission is significantly enhanced and demonstrates a single path propagation.

The inverted-F antennas appear to be a rather suitable feature for on-chip miniaturized antennas. The transmission gain is less sensitive to the size reduction, either for the length or the linewidth. The operating frequency remains inversely scale with the length. A transmission gain of -26.6 dB at 84.9 GHz can be achieved with a 400 µm long, 2 µm wide and 100 nm thick PIFA pair at a separation distance of 700 µm. The impedance matching can be significantly improved by shrinking the length of feed line and shorted line without sacrificing the gain. At the frequency above 140 GHz, the coupling between the signal pads is dominating the signal transmission. In consequence, the implementation of the antenna appears ineffective. It was observed that the phase and magnitude of S_{21} fluctuate rapidly with frequency, indicating the signal suffers from the interference of multi-mode propagation. This issue is probably due to the accumulation of charges at the SiO_2/Si interface, a well-known characteristic of SiO_2-passivated high resistivity silicon reported by several authors. This problem can be mitigated by depositing a polysilicon layer between Si and SiO_2 [105] [106].

Chapter 5

Conclusion

Nanowires reveal an enormous and yet undiscovered opportunities for the RF engineering community. Research continues on the design, modelling and measurement techniques to uncover their interesting properties. In this context, the central question of this thesis was discussed: what are the electrical transmission properties as a function of nano-metric geometry and frequency in metallic nanowires at millimeter-wave frequency? The transmission characteristics of metallic nanowires were evaluated from two aspects:

1) By exciting the nanowires in transmission line modes. Nanowires were integrated in micro-scale test structures that are compatible with the test equipment. Their electrical characteristics as transmission lines on silicon substrates were extracted.
2) By exciting the nanowires in antenna modes. Nanowires were realized as both transmitting and receiving on-chip antennas. Wireless transmission characteristics of the integrated nanoscale antennas in Si chips were extracted.

Two features of nanowire-integrated transmission lines were characterized including microstrip lines and coplanar waveguide using characteristic impedance and propagation constant. RLGC lumped element model was utilized to understand the transmission lines behaviour in relation to the frequencies. Two types of on-chip antennas were designed including dipoles and planar inverted-F antennas. Some basic antenna parameters including resonance frequency, transmission gain and input impedance as well as radiation loss were evaluated. We now summarize the answer to the central question according to the applications.

5.1 Metallic Nano-Transmission Line Characteristics

In the case of CPW structures, although being far from 50 Ω, both real and imaginary characteristic impedances of the nano-transmission lines decrease sharply with increasing frequency (1 to about 70 GHz), providing a wide range of characteristic impedance. At high frequencies (above 140 GHz), the impedance approaches to certain values corresponding to those of low-loss approximation. Moreover, the smaller the conductor, the higher the frequency where this fact occurs. The change of substrate loss as a function of frequency translates into the change of signal attenuation. In addition, substrate loss is reduced by decreasing the linewidth of nanowires. However, such reduction in substrate loss cannot compensate the excessive conductor loss due to downsizing. The conductor loss was shown to be constant across the frequency range, implying that skin effect is ineffective. It was found that the conductivity of gold metallic nanowires was about 55% lower than its bulk

counterpart. And its resistance at AC per unit length was approximately 20% higher than the one at DC. The result also showed that just like CNTs, high resistance makes metallic nanowires slower compared to the conventional transmission lines. An additional increase in phase constant was observed for nanowires with linewidth and thickness scaling down to 100 nm. This could be attributed to the increase in kinetic inductance although its quantity has a minor significance.

It has been observed that microstrip line structures have two advantages over CPW structures: low substrate loss and flexibility in controlling characteristic impedance. As the silicon substrate is shielded by a ground plane, the transmission resides only in the SiO_2 layer, thus minimizing the conduction loss. Besides, the thickness of the oxide layer can be reduced to the same order as that of the conductor in such a way that characteristic impedance can be adjusted closer to 50 Ω. Although it is also possible to control the characteristic impedance of a coplanar waveguide, it is more technologically challenging. These factors indeed make microstrip lines an ideal vehicle to characterize nanowires. However, in practice, there are additional considerations in realizing a desirable test platform. First, grounding microstrip lines requires via holes. It was also found that the ground plane underneath should be as far away from the RF GSG pads as possible to avoid huge parasitic capacitance. These requirements will make the fabrication process more difficult than that of CPW structures. This is the reason why the central results in this study were derived predominately from CPW test platform.

Multiple parallel transmission line configurations were investigated. The concept is the same as using CNT bundles to reduce losses and impedance. Unlike CNTs which can be densely packed, metallic nanowires have a practical limit which is imposed by fabrication of the very narrow interline distance. It was found that the more the number of nano-lines in the signal path, the lower impedance and the conductor loss although slow wave propagation effect is compromised as observed in this study. An advantageous aspect is that paralleling combination results in different performance on the effective lumped element *L* and *C*. For example, by varying the distance between lines and the gap, one can fine tune the effective *L* and *C*. This provides RF circuit designers various choices of miniature transmission lines for desired characteristics. However, special attention must be paid to the associated rising substrate losses.

5.2 On-chip Nano Antenna Characteristics

In this part of the work, the capabilities of current silicon technologies were studied to allow the implementation of nanoscale on-chip antennas with acceptable performances. Metallic wires with thickness down to 100 nm and minimum feature size of 1 µm were designed in dipole and planar inverted-F antenna structures. The length of these devices was devoted to systems working at mm-wave frequencies. The minimum arm length of the dipole and PIFA structure is 300 µm, allowing an operating frequency to be over 110 GHz on a high resistivity Si substrate. Obviously, the radiation efficiency of a small antenna can hardly compete with a classical antenna. It was shown that a half-wavelength dipole operating at 100 GHz with linewidth of 1 µm suffers from severe ohmic losses. The resulting radiation efficiency was very poor. Other characteristics observed due to dimensional scaling include larger bandwidth and higher input impedance. The impedance matching or reflection efficiency can be improved by reducing the length of feed line for both kinds of antennas. An input return loss of -23.6 dB at 64.2 GHz can be achieved for a 500 µm long, 2 µm wide and 100 nm thick

PIFA structure accompanied by a 40 µm long feed line on a SiO_2-coated high resistivity Si substrate.

As the communication of the integrated antenna pair occurs mostly through the Si substrate, a high resistivity substrate is indispensable for operating at mm-wave frequency. It was demonstrated that the transmission gain can be significantly improved by using porous silicon and high resistivity substrates. The maximum transmission gain is -25 dB at 77.8 GHz with a 814 µm long, 2 µm wide and 100 nm thick dipole pair at a separation distance of 700 µm on a high resistivity Si chip. PIFA test structures are actually quite favourable for size reduction for the effect of the wire dimension on the performance is not overly important. The transmission gain of a 400 µm long, 1 µm wide and 100 nm thick PIFA pair at a separation distance of 700 µm is about -29.4 dB at 80.6 GHz which does not have a big difference comparing to the 2 µm wide pair.

Surface waves were found to be an important contributor to signal propagation in short-distance applications. In the integrated dipole antennas, the signal transmission was actually assisted by the generation of TE_1 surface wave, demonstrating a single path propagation. Likewise, the enhancement in signal level in the PIFA test device was observed although the receiving signal was somewhat corrupted due to multipath propagation. Therefore when designing integrated small antennas, it is suggested to make use of surface waves as a vehicle to improve transmission either within dielectric layers or over the air. This can allow more flexibility to modulate the trade-off between the size and the radiation efficiency.

Constrained by limited radiation efficiency, nanoscale antennas require a careful optimization of arrangement of metal shapes and dielectric regions to suit a specific application. It is true that there is still a long way to make presently realized on-chip nano-antennas into a possible real-world implementation. More research is needed to address issues like required external power, heating and the risk of crosstalk with circuits.

5.3 Validity of the Model

It was shown that both the thin film microstrip lines and the nanowire-integrated CPWs satisfied quasi-TEM behaviour. Their distributed circuit elements namely *R*, *L*, *G* and *C* can be derived from close-form expressions and ADS Momentum simulator. The measured results from different nano-lines show high correlation with the theoretical circuit model up to 110 GHz. According to the description of close-form formula, the conductor loss of the selected nanowires with linewidth lower than 1 µm remains below the DC limit in the frequency of analysis, from which, it is possible to derive the conductivity of the metallic nanowires assuming the resistivity of the ground plane is negligible. Meanwhile, the inductance curve of the nanowires saturates towards its DC limits since the current distribution is uniform inside the conductor. One of the limitations in these approximate solutions is the assumption that the signal and ground conductor has the same thickness. That said, no deterioration in accuracy in the test devices was observed, possibly because the signal conductor thickness dominates the behaviour. The expressions for capacitance and conductance in the case of the thin film microstrip line were taken from a convention microstrip line model. It appears that it still yields a good accuracy for submicron dimensions. ADS Momentum provides a close prediction of lumped impedance in the multi-layered substrate. Special attention should be paid to the mesh setting. The number of cell in transverse direction for the conductor should be at least three.

One of the general limitations for the models is the negligence of quantum transport effect. If the transverse dimension continues to scale down, this approximation will be violated. In this case, additional circuit elements may need to be taken into account. Most likely, the metallic nanowires may possess kinetic inductance and quantum capacitance which conventional TEM model ignores. It was noticed that there was a deviation from the model when the linewidth scales close to 100 nm. An additional limitation lies in the quasi-TEM propagation assumption. This can be violated if the actual wavelength becomes comparable to the dimension of the pads and transmission lines. Higher order modes are probable to be excited and interact with the first fundamental mode, which may adversely affect propagation characteristics.

The models adopted in this work provide a very efficient estimation for the lumped circuit elements in metallic nano-transmission lines. Compared to other commercially available simulators such as HFSS and CST, nanoscale mesh cells typically result in large memory consumption and overall computational time becomes excessively long. Here, the close-form expressions may be lengthy but can be easily implemented in ADS simulator.

5.4 Accuracy of the Measurement and Extraction

The experimental determination of transmission line parameters requires precise knowledge of test structure and contact impedance. Their contribution to the RF responses as a function of frequency has been systematically explored in Chapter 3. And they are believed to be quite important, therefore needed to be removed. However, each subtraction step introduces some errors and uncertainties which propagate to the parameter in the calculation. That is why an accurate approximation of parasitics is critically important for a successful de-embedding. It was found that contact impedance dominates the uncertainty in transmission line measurement at the lower frequency region (lower than 70 GHz). Two-line method was shown to be the most efficient way to eliminate contact impedance. However, it tends to over-de-embed nanolines with feature size below 100 nm above 70 GHz. It is because that the captured contact impedance is not within the uncertainty range of the original measurement. Therefore such subtraction should be omitted at this frequency range. In addition, the coupling between the signal pads needs to be removed from the measurement. It is important that this effect never dominates the overall signal. Otherwise, the accuracy of the extraction would be degraded.

Measurement invariably has an uncertainty interval. This interval is the result of many causes. One source of uncertainty is caused by poor contact when landing the probes onto the pads. Fortunately, this can be rapidly identified if the *S*-parameters are not symmetrical as the system is a reciprocal network. Adequate force should be applied to break through the naturally formed layer of Al_2O_3 covering the pads, but not too strong to penetrate them. Random errors were occasionally observed in the measurement, most often occurred at mm-wave frequency regime. They can be rapidly recognized as noise and repeatability problem, such as the calibration drift. Finally, the uncertainty may be increased due to unwanted temperature variation in the instrumentation. However, such influence is hardly perceptible in the measurement.

5.5 Possible Future Work

A well-known characteristic of research is that it is never finished. The research presented here could lead to more questions. They can be categorized as follows:
Concerning nano-transmission line characterization, several points can be further elaborated:

1) How can the accuracy of the measurement be improved?
2) What are the remaining parameters to be considered in the model?
3) What is the limitation in terms of scaling in feature size?

It was shown that the accuracy of the measurement was greatly influenced by the test vehicle. The strong coupling between the signal pads hindered the extraction of parameters at mm-wave frequency. It is known that pad parasitic removal is more difficult to achieve when the pad is large and the device is small. Unfortunately, the feature size of the RF pads is limited by the probe tips. It must be large enough to accommodate the contact as well as the overtravel to ensure a successful probing. Despite of this, one can reduce the pad parasitic reactance by utilizing a low-loss substrate, for instance high resistivity Si and porous silicon substrates, thus improving the accuracy of the de-embedding method.

The model proposed in this work did not consider the quantum effect. The model should take into account extra circuit elements such as kinetic inductance and quantum capacitance. These influences are probably not very significant in the metallic nanowires under test. However, their modelling would allow a clear picture of the influence on dimensional scaling. In addition, the model did not cover the case of multiple lines transmission. Parallel line mutual coupling should be included in the circuit modelling. The prediction of multiple line characteristics is vital. It can provide interesting data to RF circuit designers. Particularly, the influence of structural parameters for instance gap and interline distance to the overall performance of a transmission line. Moreover, it is a key to study nanowires with feature size lower than 50 nm. Since characterization of single nanowires is too sensitive to parasitic and noise, multiple parallel nanowires would be a better choice for the tested components. From this, it follows that how far can we continue to scale down the feature size of nanowires while still have a reliable measurement? With the test setup in this work, the limitation was encountered at a critical size of 100 nm. To answer this question, more experimental work will be required. There would be more uncertainties in the extracted *S*-parameters. In any case, it should be interesting to see what the limits are on the development of traditional RF transmission line.

One part that is not fully finished in the study of nanoscale integrated antennas is the radiation pattern measurement. The question here is how these antennas will perform via radiation in the air? The properties of the antennas such as the gain and radiation efficiency should be understood thoroughly before the realization of a wireless communication system. Furthermore, the design of the antenna must be optimized to be more suitable for radiation in the air. This can involve the modification of the antenna structures and the choice of different substrates.

Appendix A

Antenna Basics

A1. Basic Parameters

There are many parameters affects the performance of an antenna. Apart from radiation efficiency, input impedance and transmission gain discussed in Section 4.3, directivity and gain are just as important. The directivity of an antenna is defined as "the ratio of the radiation intensity from the antenna in given direction to the radiation intensity averaged over all directions". Most often, the direction of directivity is not specified. In such case, the direction of the maximum radiation intensity is implied and the maximum directivity is given by:

$$D_{max} = \frac{4\pi U_{max}}{P_r} \tag{A-1}$$

where D_{max} is the maximum directivity, $U_{\max}$ is the maximum radiation intensity and P_r is the total radiated power. D is a dimensionless quantity. It is generally expressed in dBi since the definition of directivity also implies "the ratio of the radiation intensity of a nonisotropic source in a given direction over that of an isotropic source". Note that radiation intensity of an isotropic source is:

$$U_i = \frac{P_r}{4\pi} \tag{A-2}$$

which leads to

$$D_{max} = \frac{U_{max}}{U_i} \tag{A-3}$$

The directivity of an isotropic source is unity. A more directive antenna means an antenna with a more focused radiation main beam. Its maximum directivity will always be greater than unity. In other words, directivity gives an indication of the directional properties of the antenna as compared with those of an isotropic source.

The gain, on the other hand, is a parameter that measures the directivity of a given antenna. It is defined as "the ratio of the intensity, in a given direction, to the radiation intensity that would be obtained if the power accepted by the antenna were radiated isotropically". Its relationship to the directivity can be derived as follows:

$$G = \frac{4\pi U}{P_{in}} = e_{cd} \cdot \frac{4\pi U}{P_r} = e_{cd} \cdot D \tag{A-4}$$

where P_{in} is the input power received by the antenna and e_{cd} is the radiation efficiency which was mentioned in Section 4.3.2. The relative gain is another definition for antenna

gain, which is defined as the power gain ratio in a specific direction of an antenna to the power gain ratio of a reference antenna in the same direction. The input power must be the same for both antennas.

$$G_{relative} = G_{ref} \frac{P_{max}}{P_{max}|_{ref}} \quad \text{(A-5)}$$

The reference gain could be a dipole, horn or isotropic lossless antenna whose power gain is already known. The information presented in this section could be found in [87].

A2. Dipole Antenna

A dipole is a very basic antenna structure consisting of two split wires, not necessarily of equal length. Unlike monopole antennas, a dipole antenna does not require a ground plane. When we drive an alternating current into the dipole, the two wires produce alternating electric and magnetic fields, thus generating the radiation. The amount of radiation will be proportional to the dipole current. The current distribution also determines the radiation pattern. The most commonly used antenna is the half-wave length dipole. "Half-wave" term means that the length of this dipole antenna is equal to a half-wavelength at the frequency of operation. Such dipole is also in resonant at integral multiples of its resonant frequency. The following reasons make half-wavelength dipole very popular: 1) A reasonable directivity about 2.15 dB. 2) Its radiation pattern is omnidirectional which is required by many applications (omnidirectional means that the radio wave power radiates uniformly in all directions in one plane). The maximum power radiates in horizontal directions, dropping to zero directly above and below the antenna. 3) The input impedance is not sensitive to the radius and is about 73 Ω, which is well matched with a standard transmission line of characteristic impedance 75 or 50 Ω.

A3. Inverted-F Antenna

The Inverted F antenna is a variant of the monopole where the top section has been folded down so as to be parallel with the ground plane. This parallel section introduces capacitance to the input impedance of the antenna, which is compensated by implementing a shorted line connected to the ground plane. The ground plane serves as a perfect energy reflector and acts as the other part of the dipole. In general, the required ground plane length is roughly one quarter ($\lambda/4$) of the operating wavelength. Its dominant resonance occurs at around one-quarter of the operating wavelength. The advantages of an inverted-F antenna include reduction in size, reduction in backward radiation and moderate high gain in both vertical and horizontal polarizations. The last feature is very useful in certain wireless communications where the antenna orientation is not fixed.

References

[1] V. Ermolov, M. Heino, A. Karkkainen, R. Lehtiniemi, N. Nefedov, P. Pasanen, Z. Radivojevic, M. Rouvala, T. Ryhanen, "Significance of nanotechnology for future wireless devices and communications," *IEEE 18th International Symposium on Personal, Indoor and Mobile Radio Communications (PIMRC),* pp. 1-5, 2007.

[2] R. Hinchet, J. Ferreira, J. Keraudy, G. Ardila, E. Pauliac-Vaujour, M. Mouis, L. Montes, "Scaling rules of piezoelectric nanowires in view of and energy harvester integration," *Proceeding of International Electron Devices Meeting* , pp. 6.2.1 - 6.2.4 , 2012.

[3] H. Iwai, "Roadmap for 22 nm and beyond," *Microelectronic Engineering,* vol. 86, pp. 1520-1528, 2009.

[4] P. S. Peercy, "The drive to miniaturization," *Nature,* vol. 406, no. 6799, pp. 1023-1026, 2000.

[5] Y. Cui, Z. Zhang, D. Wang, W. U. Wang, C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Letter,* vol. 3, pp. 149-152, 2003.

[6] W. Lu, P. Xie, C. M. Lieber, "Nanowire transistor performance limits and applications," *IEEE transactions on Electron Devices,* vol. 55, pp. 2859-2876, 2008.

[7] A. Javey, J. Guo, Q. Wang, M. Lundstrom, H. Dai, "Ballistic carbon nanotube field-effect transistors," *nature,* vol. 424, pp. 654-657, 1999.

[8] S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, Ph. Avouris, "Carbon nanotubes as Schottky barrier transistors," *Physical Review Letters,* vol. 89, p. 106801, 2002.

[9] A. D. Franklin, M. Luisier, S.-J. Han, G. Tulevski, C. M. Breslin, L. Gignac, M. S. Lundstrom, W. Haensch, "Sub-10 nm carbon nanotube transistor," *Nano Letters,* vol. 12, no. 2, pp. 758-762, 2012.

[10] J. Guo, S. Hasan, A. Javey, G. Bosman, M. Lundstrom, "Assessment of high frequency performance potential of carbon nanotube transistors," *IEEE Transactions on Nanotechnology,* vol. 4, no. 6, pp. 715-721, 2005.

[11] R. Wang, J. Zhuge, R. Huang, Y. Tian, H. Xiao, L. Zhang, C. Li, X. Zhang, Y. Wang, "Analog/RF performance of Si nanowire MOSFET and the impact of process variation," *IEEE Transactions on Electron Devices,* vol. 54, no. 6, pp. 1288-1294, 2007.

[12] P. J. Burke, "AC performance of nanoelectronics: towards a ballistic THz nanotube transistor," *Solid-State Electronics,* vol. 40, pp. 1981-1986, 2004.

[13] C. Rutherglen, D. Jain, P. J. Burke, "Nanotube electronics for radio frequency applications," *Nature Nanotechnology,* vol. 4, pp. 811-819, 2009.

[14] S. Cho, K. Kim, B. Park, I. Kang, "Non-quasi-static modeling of silicon nanowire

metal–oxide–semiconductor field-effect transistor and its model verification up to 1 THz," *Japanese Journal of Applied Physics,* vol. 49, no. 110206, 2010.

[15] P. J. Burke, "Carbon nanotube devices for GHz to THz applications," *Proceedings of International Semiconductor Device Research Symposium,* pp. 314 - 315 , 2003.

[16] T. Quémerais, L. Moquillon, J. Fournier, P. Benech, "65-, 45-, and 32-nm aluminium and copper transmission-line model at millimeter-wave frequencies," *IEEE Transactions on Microwave Theory and Techniques,* vol. 8, pp. 2426-2433, 2010.

[17] C. Durkan, M. E. Welland, "Size effects in the electrical resistivity of polycrystalline nanowires," *Physical Review B: Condensed Matter and Materials Physics,* vol. 61, p. 14215–14218, 2000.

[18] C. T. White, T. Todorov, "Quantum electronics - nanotubes go ballistic," *Nature,* vol. 411, pp. 649-651, 2001.

[19] F. Kreupl, A. P. Graham, M. Liebau, G. S. Duesberg, R. Seidel, E. Unger, "Carbon nanotubes in interconnect applications," *Microelectronic Engineering,* vol. 64, pp. 399-408, 2002.

[20] N. Srivastava, K. Banerjee, "Performance analysis of carbon nanotube interconnects for VLSI applications," *Proceedings of IEEE/ACM International Conference on Computer-Aided Design,* pp. 383 - 390, 2005.

[21] A. Raychowdhury, K. Roy, "A circuit model for carbon nanotube interconnects: comparative study with Cu interconnects for scaled technologies," *Proceedings of IEEE/ACM International Conference on Computer Aided Design,* pp. 237 - 240, 2004.

[22] P. L. McEuen, J. Park, "Electron transport in single-walled carbon nanotubes," *Materials Research Society Bulletin,* vol. 29, pp. 272-275, 2004.

[23] A. Nieuwoudt,Y. Massoud,, "Evaluating the impact of resistance in carbon nanotube bundles for VLSI interconnect using diameter-dependent modeling techniques," *IEEE Transactions on Electron Devices,* vol. 53, pp. 2460 - 2466, 2006.

[24] P. J. Burke, "An RF circuit model for carbon nanotubes," *Proceedings of the 2002 2nd IEEE Conference on,* pp. 393 - 396, 2002.

[25] S. Salahuddin, M. Lundstrom, S. Datta, "Transport effects on signal propagation in quantum wires," *IEEE Transactions on Electron Devices,* vol. 52, pp. 1734-1742, 2005.

[26] J. J. Plombon, K. P. O'Brien, F. Gstrein, V. M. Dubin, "High-frequency electrical properties of individual and bundled carbon nanotubes," *Applied Physics Letters,* vol. 90, p. 063106, 2007.

[27] P. Russer , N. Fichtner , P. Lugli , W. Porod , J. A. Russer, H. Yordanov, "Nanoelectronics-based integrated antennas," *IEEE Microwave Magazine,* vol. 11, pp. 58-71, 2010.

[28] S. I. Association, International Technology Roadmap for Semiconductors: 1999 Edition, Austin, TX: International SEMATECH, 1999.

[29] W. Steinhögl, G. Schindler, G. Steinlesberger, M. Engelhardt, "Size-dependent resistivity of metallic wires in the mesoscopic range," *Physical Review B,* vol. 66, no. 075414, 2002.

[30] "International Technology Roadmap for Semiconductors," 2007. [Online]. Available: http://public.itrs.net, 2007.

[31] C. Wang, Y. Hu, C. M. Lieber, S. Sun, "Ultrathin Au nanowires and their transport

properties," *Journal of the American Chemical Society,* vol. 130, p. 8902–8903, 2008.

[32] N. Kharche, S. R. Manjari, Y. Zhou, R. E. Geer, S. K. Nayak, "A comparative study of quantum transport properties of silver and copper nanowires using first principles calculations," *Journal of Physics: Condensed Matter,* vol. 23, no. 085501, 2011.

[33] G. W. Hanson, "A common electromagnetic framework for carbon nanotubes and solid nanowires-spatially dispersive conductivity, generalized Ohm's law, distributed impedance, and transmission line model," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, no. 1, pp. 9-20, 2011.

[34] P. J. Burke, S. Li, Z. Yu, "Quantitative theory of nanowire and nanotube antenna performance," *IEEE Transactions on Nanotechnology,,* vol. 5, pp. 314 - 334, 2006.

[35] P. Russer, N. Fichtner, "Nanoelectronics in radio-frequency technology," *IEEE Microwave Magazine,* vol. 11, pp. 119-135, 2010.

[36] S. Demoustier, E. Minoux, M. Le Baillif, M. Charles, "Review of two microwave applications of carbon nanotubes: nano-antennas and nano-switches," *Comptes Rendus Physique,* vol. 9, p. 53–66, 2008.

[37] P. Russer , N. Fichtner , P. Lugli , W. Porod , J. A. Russer, H. Yordanov, "Monolithic integrated antennas and nanoantennas for wireless sensors and for wireless intrachip and interchip communication," *Proceedings of European of Microwave Conference,* pp. 703 - 706, 2010.

[38] G. W. Hanson, "Fundamental transmitting properties of carbon nanotube antennas," *IEEE Transactions on Antennas and Propagation,* vol. 53, pp. 3426 - 3435, 2005.

[39] G. W. Hanson, "Radiation efficiency of nano-radius dipole antennas in the microwave and far-infrared regimes," *IEEE Antennas and Propagation Magazine,* vol. 50, no. 3, pp. 66 - 77, 2008.

[40] P. -J. Guo, H. -R. Chuang, "A 60-GHz Millimeter-wave CMOS RFIC-on-chip meander-line planar inverted-F antenna for WPAN applications," *Proceeding of Antennas and Propagation Society International Symposium,* pp. 2522 - 2525, 2007.

[41] F. Gutierrez , S. Agarwal , K. Parrish, T. S. Rappaport, "On-chip integrated antenna structures in CMOS for 60 GHz WPAN systems," *Proceedings of IEEE Global Telecommunications Conference,* pp. 1-7, 2009.

[42] T. N. Theis, "The future of interconnection technology," *IBM J. Research and Development,* vol. 44, no. 3, pp. 379-390, 2000.

[43] T. S. Rappaport, F. Gutierrez, T. Al-Attar, "Millimeter-wave and terahertz wireless RFIC and on-chip antenna design: tools and layout techniques," *Proceedings of IEEE GLOBECOM Workshops,* pp. 1-7, 2009.

[44] P. Bharadwaj, B. Deutsch, L. Novotny, "Optical antennas," *Advances in Optics and Photonics,* vol. 1, p. 438–483, 2009.

[45] H. Y. Zhou, X. Chen, D. S. Espinoza, A. Mickelson, "Nanoscale optical dielectric rod antenna for on-chip interconnecting networks," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, pp. 2624 - 2632, 2011.

[46] L. Gomez-Rojas , S. Bhattacharyya , E. Mendoza , D. C. Cox , J. M. Rosolen, S. R. Silva, "RF response of single-walled carbon nanotubes," *Nano Letters,* vol. 7, no. 9, p. 2672–2675, 2007.

[47] S. C. Jun , X. M. H. Huang , S. Moon , H. J. Kim , J. Hone , Y. W. Jin, J. M. Kim,

"Passive electrical properties of multi-walled carbon nanotubes up to 0.1 THz," *New Journal of Physics*, vol. 9, p. 265, 2007.

[48] K. Kim, T. M. Wallis, P. Rice, C.-J. Chiang, A. Imtiaz, P. Kabos, D. S. Filipovic, "Modeling and metrology of metallic nanowires with application to microwave interconnects," *Proceedings of IEEE International Microwave Symposium Digest (MTT-S),* pp. 1292 - 1295, 2010.

[49] T. M. Wallis, K. Kim, D. S. Filipovic, P. Kabos, "Nanofibers for RF and beyond," *IEEE Microwave Magazine,* vol. 12, pp. 51 - 61, 2011.

[50] Z. Zou, J. Kai, C. H. Ahn, "Electrical characterization of suspended gold nanowire bridges with functionalized self-assembled monolayers using a top-down fabrication method," *Journal of Micromechanics and Microengineering,* vol. 19, no. 5, p. 055002, 2009.

[51] B. C. Wadell, Transmission line desigh handbook, Norwood: Artech House, Inc., 1991.

[52] J. E. Post, "On determing the characteristic impedance of low-loss transmission lines," *Microwave and Optical Technology Letters,* vol. 47, no. 2, pp. 176-180, 2005.

[53] F. R. Madriz, J. R. Jameson, S. Krishnan, X. Sun, C. Y. Yang, "Circuit modeling of high-frequency electrical conduction in carbon nanofibers," *IEEE Transactions on Electron Devices,* vol. 53, pp. 1557 - 1561, 2009.

[54] A. M. Mangan , S. P. Voinigescu , M.-T. Yang, M. Tazlauanu, "De-embedding transmission line measurements for accurate modeling of IC designs," *IEEE Transactions on electron Devices,* vol. 53, pp. 235 - 241, 2006.

[55] Y. Tretiakov, J. Rascoe, K. Vaed, W. Woods, S. Venkatadri, T. Zwick, "A new on-wafer de-embedding technique for on-chip RF transmission line interconnect characterization," *Proceedings of IEEE Automatic RF Techniques Group (ARFTG) Conference,* pp. 69 -72, 2004.

[56] H. Ito, K. Masu, "A simple through-only de-embedding method for on-wafer S-parameter measurements up to 110 GHz," *Proceedings of IEEE MTT-S Internation Microwave SYmposium Digest,* pp. 383-386, 2008.

[57] D. Gu, T. M. Wallis, P. Blanchard, S. -H. Lim, A. Imtiaz, K. A. Bertness, N. A. Sanford, P. Kabos, "De-embedding parasitic elements of GaN nanowire metal semiconductor field effect transistors by use of microwave measurements," *Applied Physics Letters,* vol. 98, no. 223109, 2011.

[58] P. Rice, T. M. Wallis , S. E. Russek , P. Kabos, "Broadband electrical characterization of multiwalled carbon nanotubes and contacts," *Nano Letters,* vol. 7, p. 1086–1090, 2007.

[59] F. R. Madriz, J. R. Jameson, S. Krishnan, X. Sun, C. Y. Yang, "Test structure to extract circuit models of nanostructures operating at high frequencies," *Proceedings of IEEE International Conference on Microelectronic Test Structures,* pp. 138-140, 2009.

[60] C. Rutherglan , D. Jain, P. J. Burke, "RF resistance and inductance of massively parallel single walled carbon nanotubes: direct, broadband measurements and near perfect 50 Ω impedance matching," *Applied Physics Letters,* vol. 93, pp. 083119-1-083119-3, 2008.

[61] K. Kim, T.M. Wallis, P. Rice, D. Gu, S. H. Lim, A. Imtiaz, P. Kabos, D.S. Filipovic,, "High-frequency characterization of contact resistance and conductivity of platinum nanowires," *IEEE Transactions on Microwave Theory and Techniques,* vol. 59, pp.

2647 - 2654, 2011.

[62] F. Schnieder, W. Heinrich, "Model of thin-film microstrip line for circuit design," *IEEE Transactions on Microwave Theory and Techniques,* vol. 49, pp. 104 - 110, 2001.

[63] S. J. Orfanidis, "Electromagnetic Waves and Antennas," November 2002. [Online]. Available: http://www.ece.rutgers.edu/~orfanidi/ewa/.

[64] L. Hayden, "An enhanced Line-Reflect-Reflect-Match calibration," *ARFTG Microwave Measurements Conference, San Francisco, CA.,* p. 143–149, 2006.

[65] Anritsu, "Application Note: Embedding/De-embedding," May 2002. [Online]. Available: http://downloadfile.anritsu.com/RefFiles/en-US/Services-Support/Downloads/Application-Notes/Application-Note/11410-00278B.pdf.

[66] Agilent, "Application Note 1364-1: De-embedding and Embedding S-Parameter Networks Using a Vector Network Analyzer," May 2004. [Online]. Available: http://literature.agilent.com/litweb/pdf/5980-2784EN.pdf.

[67] M. C. A. M. Koolen, J. A. M. Geelen, M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high-frequency characterization," *Proceedings of the Bipolar Circuits and Technology Meeting,* pp. 188 - 191, 1991.

[68] M. -H. Cho, G. -W. Huang, C. -S. Chiu, K. -M. Chen, A. -S. Peng, Y. -M. Teng, "A cascade Open-Short-Thru (COST) de-embedding method for microwave on-wafer characterization and automatic measurement," *IEICE Transactions on Electronics,* Vols. E88-C, no. 5, p. 845–850, 2005.

[69] Y. Huang, K. Boyle, Antennas from Theory to Practice, Singapore: John Wiley and Sons, 2008.

[70] M. Upmaka, "More Momentum Questions," 22 October 2002. [Online]. Available: www.ieee.li/pdf/viewgraphs/planar_em.pdf.

[71] Z. Wang, M. Jamal Deen, "Accurate modeling of thin-film resistor up to 40GHz," *Proceeding of 32th European Solid-State Device Research Conference,* pp. 307-310, 2002.

[72] J. P. Thakur, A. K. Pandey, A. Kedar, K. K. Gupta, H. P. Vyas, "Modelling of GaAs-MMIC microstrip line up to 40 GHz," *International Journal of RF and Microwave Computer-Aided Engineering,* vol. 14, p. 475–482, 2004.

[73] V. Milanovic, M. Ozgur, D. C. DeGroot, J. A. Jargon, M. Gaitan, M. E. Zaghloul, "Characterization of broad-band transmission for coplanar waveguides on CMOS silicon substrates," *IEEE Transactions on Microwave Theory and Techniques,* vol. 96, no. 5, p. 042109, 2010.

[74] W. Heinrich, "Quasi-TEM description of MMIC coplanar lines including conductor loss effects," *IEEE Transactions Microwave Theory and Techeniques,* vol. 41, pp. 45-52, 1993.

[75] T. E. Kolding, "On-wafer calibration techniques for giga-hertz CMOS measurements," *Proceeding in IEEE Internation Conference on Microelectronic Test Structures,* vol. 12, pp. 105-110, 1999.

[76] L. Nougaret, G. Dambrine, S. Lepilliet, H. Happy, N. Chimot, V. Derycke, J. P. Bourgoin, "Gigahertz characterization of a single carbon nanotube," *Applied Physics Letters,* vol. 96, p. 042109, 2010.

[77] E. Gago-Ribas, C. Dehesa-Mart, M. J. Gonzalez-Morales, "Complex analysis of the

lossy-transmission line theory: a generalized smith chart," *Turkish Journal of Electrical Engineering & Computer Sciences*, vol. 14, pp. 173-194, 2006.

[78] J. -Y. Kim, M. -K. Choi, S. Lee, "A "Thru-Short-Open" de-embedding method for accurate on-wafer RF measurements of nano-scale MOSFETs," *Journal of Semiconductor Technology And Science*, vol. 12, no. 1, pp. 53-58, 2012.

[79] R. N. Simons, Coplanar Waveguide Circuits, Components, and Systems, John Wiley & Sons, Inc., 2001.

[80] A. B. M. H. Rashid, S. Watanabe, T. Kikkawa, "Characteristics of integrated antenna on Si for on-chip wireless interconnect," *Journal of Applied Physics*, vol. 42, pp. 2204-2209, 2003.

[81] B. A. Floyd, C-M. Hung, K. O. O, "Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers and transmitters," *Journal of solid-state circuits*, vol. 37, pp. 543-52, 2002.

[82] Y. P. Zhang, Z. M. Chen, "Propagation mechanisms of radio waves over intra-chip channels with integrated antennas: frequency-domain measurements and time-domain analysis," *Transaction on Antennas and Propagation*, vol. 55, no. 10, pp. 2900-2906, 2007.

[83] E. Laskin, M. Khanpour, S. T. Nicolson, A. Tomkins, A. Cathelin, D. Belot, S. P. Voinigescu, "Nanoscale CMOS transceiver design in the 90-170-GHz range," *Transaction on Microwave Theory and Techniques*, vol. 57, no. 12, pp. 3477-3490, 2009.

[84] A. B. M. H. Rashid, S. Watanabe, T. Kikkawa, "High transmission gain integrated antenna on extremly high resistivity Si for ULSI wireless interconnet," *Electron Device Letters*, vol. 23, no. 12, pp. 731-733, 2002.

[85] K. T. Chan, A. Chin, Y. B. Chen, Y. -D. Lin, T. S. Duh, W. J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-Quartz," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 40.6.1 - 40.6.4, 2001.

[86] S. -S. Hsu, K. -C. Wei, C. -Y. Hsu, H. -R. Chuang, "A 60-GHz millimeter-wave CPW-fed Yagi antenna fabricated by using 0.18-µm CMOS technology," *Electron Device Letters*, vol. 28, pp. 625 - 627, 2008.

[87] C. A. Balanis, Antenna Theory: Analysis and Design, New York: John Wiley and Sons, 2005.

[88] P. -C. Kuo, S. -S. Hsu, C. -C. Li, C. -Y. Hsu, H. -R. Chuang, "A 60-GHz Millimeter-wave triangular monopole antenna fabricated using 0.18-µm CMOS technology," *International Conference on Innovative Computing Information and Control*, p. 237, 2008.

[89] D. Titz, F. B. Abdeljelil, S. Jan, F. Ferrero, C. Luxey, P. Brachat, G. Jacquemod, "Design and characterization of CMOS on-chip antennas for 60 GHz communications," *Radioengineering*, vol. 21, p. 324, 2012.

[90] Y. P. Zhang, A. M. Chen, M. Sun, "Propagation mechanisms of radio waves over intra-chip channels with integrated antennas: frequency-domain measurements and time-domain analysis," *IEEE Transactions on Antennas and Propagation*, vol. 55, pp. 2900 - 2906, 2007.

[91] A. Triantafyllou, PhD thesis, Grenoble University, "Etude, réalisation et caractérisation

d'interconnexions radiofréquences pour les circuits intégrés silicium des générations à venir," 2006.

[92] L. Yan, G. W. Hanson, "Wave propagation mechanisms for intra-chip communications," *Transactions on Antennas and Propagation,* vol. 57, no. 9, pp. 2715-2724, 2009.

[93] X. He, J. Li, M. Zhang, S. Qi, "Improvement of integrated dipole antenna performance using diamond for intra-chip wireless interconnection," *International Conference on IC Design and Technology,* pp. 248 - 251, 2010.

[94] P. Russer, J. A. Russer, F. Mukhtar, P. Luglit, S. Wane, D. Bajou, W. Porod, "Integrated antennas for RF sensing, wireless communications and energy harvesting applications," *Internatonal Workshop on Antenna Technology,* pp. 1 - 4, 2013.

[95] X. N. Low, Z. N. Chen, "A UWB dipole antenna with enhanced impedance and gain performance," *Transactions on Antennas and Propagation,* vol. 57, pp. 2959 - 2966, 2009.

[96] V. Deepu, S. Mridula, R. Sujith, P. Mohanan, "Slot line FED dipole antenna for wide band applications," *Microwave and Optical Technology Letters,* vol. 51, p. 826–830, 2009.

[97] H. Issa, P. Ferrari, E. Hourdakis, A. G. Nassiopoulou, "On-chip high-performance millimeter-wave transmission lines on locally grown porous silicon areas," *Transactions on Electron Devices,* vol. 58, no. 11, p. 3720–3724, 2011.

[98] M. H. Barakat, F. Ndagijimana, C. Delaveaud, "On the design of 60 GHz integrated antennas on 0.13 μm SOI technology," *Proceeding of Antennas and Propagation Society International Symposium,* pp. 2526 - 2529, 2007.

[99] M. Capelle, J. Billoué, P. Poveda, G. Gautier, "RF performances of inductors integrated on localized p+-type porous silicon regions," *Nanoscale research letters,* vol. 7, no. 1, p. 523, 2012.

[100] H. -R. Chuang, L. -K. Yeh, P. -C. Kuo, K. -H. Tsai, H. -L. Yue, "A 60-GHz millimeter-wave CMOS integrated on-chip antenna and bandpass filter," *IEEE Transactions on Electron Devices,* vol. 58, no. 7, pp. 1837 - 1845, 2011.

[101] K. K. O, K. Kim, B. A. Floyd, J. L. Mehta, Y. Hyun, C. M. Hung, D. Bravo, T. O. Dickson, X. L. Guo, R. Li, N. Trichy, J. Caserta, W. R. Bomstad II, J. Branch, D. J. Yang, J. Bohorquez, S. Eunyoung, G. Li, A. Sugavanam, J. J. Lin, J. Chen, J. E. Brewer, "On-chip antennas in silicon ICs and their application," *IEEE Transactions on Electron Devices,* vol. 52, no. 7, pp. 1312 - 1323, 2005.

[102] W. L. Stutzmann, G. A. Thiele, Antenna Theory and Design, ISBN 0-471-02590-9, New York: John Wiely & Sons, 1981.

[103] H. W. Johnson, M. Graham, High Speed Digital Design, ISBN 0133967241, Prentice Hall PTR, 1993.

[104] K. B. Ali, C. R. Neve, A. Gharsallah, J. -P. Raskin, "Impact of crosstalk into high resistivity silicon substrate on the RF performance of SOI MOSFET," *Journal of Telecommunications & Information Technology,* vol. 2010, p. 93, 2010.

[105] H. S. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, J. A. C. Stewart, "Low-loss CPW lines on surface stabilized high-resistivity silicon," *IEEE Microwave Guided Wave Letter,* vol. 9, p. 395–397, 1999.

[106] D. Lederer, J. P. Raskin, "New substrate passivation method dedicated to HR SOI wafer fabrication with increased substrate resistivity," *IEEE Electron Device Letter*, vol. 26, no. 11, pp. 805-807, 2005.