Variability of low frequency fluctuations in sub 45nm CMOS devices-Experiment, modeling and applications

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Papers


Conferences


Low frequency (LF) noise and fluctuations in MOS devices has been the subject of intensive research during the past years. The LF noise is becoming a major concern for continuously scaled down devices, since the 1/f noise increases as the reciprocal of the device area. Excessive low frequency noise and fluctuations could lead to serious limitation of the functionality of the analog and digital circuits. The 1/f noise is also of paramount importance in RF circuit applications where it gives rise to phase noise in oscillators or multiplexors. The development of submicronic CMOS technologies has led to the onset of new type of noises, i.e. random telegraph signals (RTS), yielding large current fluctuations, which can jeopardize the circuit functionality.

However, the statistical variability in the transistor characteristics is one of the major challenges for upcoming technological nodes. The detailed knowledge of variability sources is extremely important for the design and manufacturing of variability resistant devices. Whereas the impact of random dopants, line edge roughness and oxide thickness variations is relatively well understood, the role of the polysilicon or metal gate material has only lately been investigated in simulations and experimental confirmation and quantification of its contribution is still lacking. In addition, the study of LFN variability behavior and maybe its relation with the other factors of device variations has never been done.

Therefore, the research challenges and objectives of this thesis are centered towards the studies of low frequency fluctuations and noise in 32 nm CMOS technologies and beyond. More specifically, the objectives of the LF noise investigation is summarized in the following points: i) Detailed LF noise characterization of new CMOS technologies featuring high-κ metal gate stacks, channel pockets etc, ii) change of LF noise parameters from different technologies and iii) impact of LF noise or RTS fluctuations as a variability sources for analog and digital circuits. The first objective addresses the origin of the LF fluctuations in CMOS devices in terms of trap density and defect localization in the gate dielectric and along the channel for various architectures (pocket, Ge channel, FD-SOI etc). The second objective considers the LF noise variability resulting from huge dispersion of noise sources from device to device; this is conducted owing to statistical measurements of LF noise characteristics as a function of device area and technological splits. The third issue is focused on the impact of LF noise or RTS fluctuations on the operation of elementary circuits (inverter, SRAM cell) regarded as temporal variability source.
Concerning the first objective mentioned above, the achievements of this work are summarized as follows: we developed a generic MOSFET compact CNF/CMF low frequency model based on a single equation for all operation regions with two physical parameters, namely the square root of the flat-band voltage spectral density fluctuations $\sqrt{SV_{fb}}$ related to the oxide trap density and $\Omega=\alpha_{sc}\cdot\mu_{eff}\cdot C_{ox}$ related to the effective Coulomb scattering coefficient $\alpha_{sc}$, the effective mobility $\mu_{eff}$ and the gate oxide capacitance $C_{ox}$. Both parameters can be extracted experimentally from a plot of $\sqrt{SV_{fb}}$ versus $I_d/g_m$ in linear and/or non-linear operation regions. The knowledge of these two parameters for a given CMOS technology provides a full description of the input gate voltage noise versus gate and drain voltages, and by turn of the drain current 1/f noise $S_{Id}$ for any bias conditions.

It is worth noting that the obtained constant value of the product $\alpha_{sc}\cdot\mu_{eff}$ as a function of gate voltage, it clearly means that: (i) the conventional assumption of a constant $\alpha_{sc}$ in the CNF/CMF model is not adequate, since in that case $\alpha_{sc}\cdot\mu_{eff}$ should decrease at strong inversion because $\mu_{eff}$ degrades due to surface roughness scattering, and (ii) the reduction of the Coulomb scattering coefficient $\alpha_{sc}$ at strong inversion due to screening would also not be consistent with a constant $\alpha_{sc}\cdot\mu_{eff}$ product.

The second objective of the thesis is the analysis of LFN in CMOS bulk technology nodes manufactured in STMicroelectronics the last 12 years. The above results can be summarized by plotting the volumetric trap density $N_t$ versus equivalent oxide thickness of the investigated n- and p-MOS devices to have an idea about the evolution of LFN through almost all bulk technology nodes. The results shows that in both n-MOS and p-MOS devices from the 28nm technology node the oxide trap density $N_t$ remains almost constant with the channel length $L$ for all the “flavors” measured, i.e. $N_t$ remains almost unchanged with channel length for this technology node except of the device with different oxide thickness, GO2. The different types of devices measured in this technology node are RVT, standard threshold voltage device, LVT, low threshold voltage device, SLVT, super low threshold voltage device, HPA special device for analog applications with no pockets inside the channel and finally the device with higher oxide thickness, GO2. The above observation was the moving force to plot the $N_t$ values from all the technology nodes versus the equivalent oxide thickness and see the impact of EOT on the volumetric trap density.

Finally, we have investigated the evolution of the effective Coulomb scattering coefficient $\alpha'=\alpha_{sc}\cdot\mu_{eff}$ with the equivalent oxide thickness for all the measured devices. The parameter $\alpha'$ has been extracted from the experimental noise data using the CNF/CMF model. For both
types of devices $\alpha'$ remains almost constant through the evolution of the equivalent oxide thickness. Furthermore, the parameter $\alpha'$ is higher in the p-MOS devices as expected.

The LFN analysis in CMOS bulk devices is much more complicated than some people believe. As we have seen from the results of all technology nodes, our compact model is applied in most of the cases but there are still few ones where the model does not work properly. At this point, several questions give rise: What are the criteria to distinguish the CNF from the extended CNF/CMF model? Why in some cases the one or the other model applies and not in every case? What is the physical phenomenon that distinguishes the two models? All these questions need to be answered. Even though we have achieved until now to understand many issues regarding LFN, much more need to be done. A rather new idea is to consider that the two noise terms in CNF/CMF model are uncorrelated. What does that mean? It means that the physical phenomenon is the same, trapping/detrapping of carriers into slow oxide traps but the result is divided into two parts, the one affecting the carrier number within the channel and the other affecting the carrier mobility. This idea we believe that needs more investigation in order to fully understand the LFN mechanisms and the physics behind these mechanisms.

On the other hand, the historical figures describing the volumetric trap density $N_t$ for n- and p-MOS devices give us some new insights about LFN in MOSFETs. Starting from n-MOS devices, it is clear that for this type of devices the process affects seriously the $N_t$ values. We cannot conclude any empirical rule connecting $N_t$ values with EOT. The technology process plays a more important role than the equivalent oxide thickness as was previously believed. The situation is simpler for p-MOS devices. The impact of the technology for this type of devices is diminished compared to n-MOS. We can conclude that $N_t$ is inversely proportional to $EOT^2$. The general rule of circuit designers that p-MOS devices are less noisy than the n-MOS was until now true. However, for the 28nm technology node this rule is not applied, i.e. p-MOS devices are more noisy than n-MOS devices.

The second part of the thesis includes the LF noise variability resulting from huge dispersion of noise sources from device to device; this is conducted owing to statistical measurements of LF noise characteristics as a function of device area and technological splits. The low frequency noise variability is analyzed in detail. Initially, we try to clarify the meaning of LFN variability in terms of its connection with a widely known phenomenon, the RTS noise. Then we continue with a representative example on how this phenomenon can become a major drawback in the functionality of digital circuits. Our approach to explain and model the LFN variability in CMOS bulk and FD-SOI technology nodes is based on a model
already known which describes the RTS noise. This model can explain and predict the LFN variability behavior of the 28nm bulk CMOS devices with accuracy and in detail. We extended this model in the 28nm FD-SOI technology node in order to take into account other parameters such as the correlated mobility factor and the impact of the second interface. We have incorporated these parameters in the standard bulk model, trying to understand how the second interface introduced in FD-SOI affects the LFN variability behavior of the transistors. We developed an LFN variability model which incorporates for the first time the impact of the correlated mobility fluctuations in LFN variability. The comparison between the simulation data and the experimental results showed that the role of the back interface in the overall LFN variability of the devices is not strong. This result was anticipated since the equivalent oxide thickness of the back interface is much smaller than the front one. Further analysis in this domain should be carried out in order to verify the validity of the simulation model.

In addition, a thorough investigation of the LFN variability through CMOS bulk technology nodes has been performed for the first time. The results reveal that the LFN variability shows better control for 28nm technology for both n- and p- MOS devices. Interestingly, these results are well correlated with the diminution of the static parameter variability (mismatch of threshold voltage). In addition, the experimental results revealed that the LFN variability is a more complicated phenomenon and it is highly associated with the process characteristics of the transistors and not only with the quality of the interface.

The final part of this thesis deals with the research challenge of the impact of LF noise and RTS fluctuations as a variability sources on analog and digital circuits. We present a detailed characterization and modeling of the low frequency noise characteristics of CMOS inverters. The LF noise model has been developed within the carrier number fluctuations scheme of MOS transistor excess noise, using the concept of flat band voltage or threshold voltage power spectral density. It allows us to describe accurately the load current and output voltage LF noise characteristics as a function of input voltage obtained on inverters from a 45nm bulk CMOS technology.

The developed LF noise modelling approach could constitute a useful tool for analyzing the impact of time domain fluctuations on the static and dynamic operation of CMOS inverters in VLSI circuits. In particular, it could be used for predicting the influence of dynamic fluctuations due to carrier trapping-detrapping on static noise margin and dynamic stability in SRAM cells.
The impact of the dynamic variability due to low frequency fluctuations on the operation of CMOS inverters, which constitute the basic component of SRAM cell, has been investigated. The experimental methodology to characterize the effect of dynamic variability in a CMOS inverter is first established based on fast I-V measurements of the load current following the application of a ramp input voltage $V_{in}(t)$. It is shown that, for small ramp rise times, the load current characteristics $I_{DD}(V_{in})$ exhibit a huge sweep-to-sweep dispersion due to the low frequency noise. The impact of such dynamic variability sources on the inverter’s output characteristics $V_{out}(V_{in})$ is finally demonstrated, revealing a 20% noise margin reduction for the smallest inverter cell.
Τίτλος διατριβής

«Μελέτη θορύβου χαμηλών συχνοτήτων σε CMOS διατάξεις κάτω από 45 nm, αναλυτικά και συμπαγή μοντέλα θορύβου και εφαρμογές»

Περίληψη

Η μελέτη του θορύβου στις ηλεκτρονικές διατάξεις αποτελεόταν και συνεχίζει να αποτελεί ένα σημαντικό εργαλείο ελέγχου της ποιότητάς τους. Μέσω της ανάλυσης του θορύβου χαμηλών συχνοτήτων μπορούμε να εξάγουμε συμπεράσματα για την ποιότητα της διεπιφάνειας των ηλεκτρονικών διατάξεων και όχι μόνο. Τα τελευταία χρόνια με τη συνεχιζόμενη μείωση των διαστάσεων των τρανζίστορ η μελέτη του θορύβου χαμηλών συχνοτήτων έγινε πιο σημαντική καθώς αυτός αυξάνει με τη μείωση της επιφάνειας των διατάξεων. Ο θόρυβος χαμηλών συχνοτήτων, μαζί με τις διακυμάνσεις τις οποίες εισάγει μπορεί να οδηγήσει στην ανώμαλη λειτουργία αναλογικών και ψηφιακών κυκλωμάτων. Επίσης είναι ιδιαίτερα σημαντικός για κυκλώματα ραδιοσυχνοτήτων καθώς δημιουργεί θόρυβο φάσης σε ταλαντοτές. Η ανάπτυξη κυκλωμάτων σε CMOS νανο-τεχνολογίες οδήγησε στη δημιουργία νέων τύπων θορύβου π.χ. RTS (random telegraph signals), που έχουν ως αποτέλεσμα μεγάλες διακυμάνσεις στο ρεύμα που μπορούν να οδηγήσουν σε δυσλειτουργίες των ηλεκτρονικών κυκλωμάτων.

Από την άλλη πλευρά, η στατιστική μεταβλητότητα (variability) στις χαρακτηριστικές ρεύματος-τάσεως των τρανζίστορ αποτελεί μια από τις μεγαλύτερες προκλήσεις για την εξέλιξη της νανο-τεχνολογίας. Η αναλυτική γνώση των πηγών μεταβλητότητας είναι εξαιρετικά σημαντική για την σχεδίαση και κατασκευή ηλεκτρονικών διατάξεων νέας τεχνολογίας. Κάποιες από αυτές όπως η επίδραση τυχαίων προσμίξεων (random dopants), η τραχύτητα της επιφάνειας (line edge roughness) και οι μεταβολές του πάχους του οξειδίου (oxide thickness variations) είναι πολύ καλά κατανόητες σήμερα, σε αντίθεση με το ρόλο του πολυκρυσταλλικού πυριτίου ή του μετάλλου της πύλης, γι’ αυτό τα τελευταία χρόνια ξεκίνησε η ευρεία μελέτη τους.

Συνεπώς, το θέμα της έρευνας της παρούσης διδακτορικής διατριβής επικεντρώνεται στη μελέτη του θορύβου χαμηλών συχνοτήτων και των διακυμάνσεων στη CMOS τεχνολογία 32 nm και χαμηλότερα. Πιο συγκεκριμένα, οι στόχοι της εργασίας ήταν: α) ο αναλυτικός χαρακτηρισμός του θορύβου χαμηλών συχνοτήτων σε νέες CMOS τεχνολογίες και η ανεύρεση της προέλευσης του θορύβου χαμηλών συχνοτήτων δηλαδή πυκνότητα παγίδων και
τοπικές ατέλειες στο διηλεκτρικό της πύλης και κατά μήκος του καναλιού για διάφορες αρχιτεκτονικές τρανζίστορ (pocket, Ge channel, FD-SOI κ.α.) β) οι διαφορές των παραμέτρων του θορύβου χαμηλών συχνοτήτων από τεχνολογία σε τεχνολογία, που οφείλονται στην τεράστια διασπορά των πηγών θορύβου από τρανζίστορ σε τρανζίστορ στην στο ίδιο πλακίδιο πυριτίου γ) η επίδραση του θορύβου και των διακυμάνσεων RTS ως πηγές μεταβλητήτης για αναλογικά και ψηφιακά κυκλώματα.

Όσον αφορά τον πρώτο στόχο αυτής της διατριβής, δηλαδή τη μελέτη του θορύβου χαμηλών συχνοτήτων, τα αποτελέσματα της έρευνας συνοψίζονται ως εξής: Πραγματοποιήθηκε εκτενής μελέτη του θορύβου χαμηλών συχνοτήτων σε τρανζίστορ MOSFET n και p καναλιού με διηλεκτρικό πύλης υψηλής ηλεκτρικής επιδεκτικότητας και μετάλλου (high-k/metal gate) και μήκος καναλιού από 1,8 μμ έως 26,4 nm. Τα αποτελέσματα έδειξαν ότι ο θόρυβος χαμηλών συχνοτήτων 1/f αυτών των τρανζίστορ ερμηνεύεται με το μοντέλο των διακυμάνσεων του αριθμού των φορέων και της συσχετιζόμενης ευκινησίας του ρεύματος απαγωγού σε όλες τις περιοχές λειτουργίας τους, δηλαδή από την ασθενή έως την ισχυρή αναστροφή και από την γραμμική περιοχή έως τον κόρο. Επίσης, διαπιστώθηκε ότι το γινόμενο του συντελεστή σκέδασης Coulomb και της ενεργού ευκινησίας των φορέων παραμένει σταθερό για ένα μεγάλο εύρος ρευμάτων απαγωγού. Τέλος, παρατηρήθηκε μια μη γραμμική αύξηση της τετραγωνικής ρίζας της φασματικής ισχύος του θορύβου της πύλης με την διαφορά της τάσης της πύλης από την τάση κατωφλίου, η οποία διαπιστώθηκε με την σκέδαση επιφανειακής τραχύτητας (surface roughness scattering). Τα συνολικά αποτελέσματα οδήγησαν στη δημιουργία ενός πιο ολοκληρωμένου μοντέλου θορύβου των χαμηλών συχνοτήτων, που επιτρέπει την πρόβλεψη της τύμητας του θορύβου σε υπολοιπές τεχνολογίες, κατασκευάζοντας μονάχα τις χαρακτηριστικές εισόδου. Τα αποτελέσματα αυτά μπορούν να χρησιμοποιηθούν για τη δημιουργία εργαλείων κυκλωματικής προσομοίωσης.

Μελετήσαμε τον θόρυβο χαμηλών συχνοτήτων της τεχνολογίας συμπαγούς πυριτίου 28nm για διάφορα τρανζίστορ με διαφορετική τάση κατωφλίου, διαφορετική αρχιτεκτονική του καναλιού και διαφορετικό πάχος οξειδίου. Τα αποτελέσματα έδειξαν ότι η πυκνότητα των παγίδων του διηλεκτρικού πύλης κοντά στη διεπιφάνεια παραμένει σχεδόν αμετάβλητη με το μήκος του καναλιού για όλα τα τρανζίστορ εκτός αυτού με μεγαλύτερα μήκη παγίδων οξειδίου. Τα αποτελέσματα αυτά μας παρότρυναν να επεκτείνουμε την μελέτη του θορύβου χαμηλών συχνοτήτων και στις υπόλοιπες τεχνολογίες συμπαγούς πυριτίου. Έτσι, παρουσιάσαμε μια αναλυτική περιγραφή του θορύβου χαμηλών συχνοτήτων και σε τεχνολογίες συμπαγούς πυριτίου (bulk) των τελευταίων 12 ετών κατασκευασμένες στην εταιρεία STMicroelectronics.
Τα πειραματικά αποτελέσματα ερμηνεύθηκαν από το μοντέλο διακύμανσης φορέων και της συσχετιζόμενης ευκινησίας του ρεύματος απαγωγού. Το γεγονός αυτό μας επέτρεψε να απεικονίσουμε την χρονική και τεχνολογική εξέλιξη της πυκνότητας των παγίδων διηλεκτρικού με το πάχος οξειδίου. Για τα αποτελέσματα έδειξαν ότι με τη σμίκρυνση των διαστάσεων των τρανζίστορ την πυκνότητα των παγίδων διηλεκτρικού αυξάνεται από $2 \times 10^{16}$/eV/cm$^3$ εώς $5-7 \times 10^{17}$/eV/cm$^3$ όταν το πάχος οξειδίου μειώνεται από 12nm για την τεχνολογία 250nm σε 1,4nm για την τεχνολογία 28nm και για τρανζίστορ εγκάρσιου πεδίου διαύλου τύπου n. Ενώ για τα τρανζίστορ εγκάρσιου πεδίου διαύλου τύπου p, της πυκνότητας παγίδων διεπαφής αυξάνεται από $7,45 \times 10^{15}$/eV/cm$^3$ εώς $6,38 \times 10^{17}$/eV/cm$^3$ όταν το πάχος οξειδίου μειώνεται από 15nm για την τεχνολογία 250nm σε 1,7nm για την τεχνολογία 28nm.

Επίσης, μελετήσαμε την εξάρτηση του γινόμενου του συντελεστή Coulomb και της ενεργού ευκινησίας των φορέων, $\alpha' = \omega_c \mu_{\text{eff}}$, με το πάχος οξειδίου για όλες τις τεχνολογίες και τύπους τρανζίστορ. Η παράμετρος $\alpha'$ είναι χαρακτηριστική του μοντέλου που εισάγαμε για την ερμηνεία του θορύβου χαμηλών συχνοτήτων σε τρανζίστορ εγκάρσιου πεδίου διαύλου τύπου n και p. Διαπιστώσαμε ότι η παράμετρος $\alpha'$ που εξάγαμε από τα πειραματικά δεδομένα με το μοντέλο που δημιουργήσαμε παραμένει σταθερή με το πάχος οξειδίου και για τους δύο τύπους τρανζίστορ με ελαφρώς μεγαλύτερες τιμές για τα τρανζίστορ τύπου p, όπως αναμέναμε γι' αυτόν τον τύπο τρανζίστορ.

Το συνολικό συμπέρασμα της μελέτης του θορύβου χαμηλών συχνοτήτων σε όλες τις τεχνολογίες συμπαγούς πυριτίου μας έδειξε ότι είναι ένα θέμα πιο πολύπλοκο απ' ότι κάποιοι θεωρούν. Το μοντέλο που δημιουργήσαμε εφαρμόζεται σχεδόν σε όλες τις περιπτώσεις παρόλα αυτά υπάρχουν κάποιες στις οποίες δεν λειτουργεί. Εύλογα, λοιπόν, μπορούν να αναδυθούν κάποια ερωτήματα, όπως : με ποια κριτήρια μπορούμε να ξεχωρίσουμε το παλιότερο μοντέλο από το καινούριο; Γιατί σε ορισμένες περιπτώσεις το ένα ή το άλλο μοντέλο λειτουργούν και όχι σε όλες; Ποια είναι τα φυσικά φαινόμενα που διαχωρίζουν τα δύο μοντέλα; Παρόλο που έχουμε καταφέρει πολλά όσον αφορά την κατανόηση του μηχανισμού του θορύβου χαμηλών συχνοτήτων υπάρχει πολλά ζητήματα ακόμη που χρήζουν εκτενότερης μελέτης. Μια σχετικά καινούρια ιδέα είναι να θεωρήσουμε τους δύο όρους στο μοντέλο των διακυμάνσεων του αριθμού των φορέων και της ευκινησίας του ρεύματος απαγωγού μη συσχετιζόμενους (uncorrelated). Αυτό θα σήμαινε ότι το φυσικό φαινόμενο που προκαλεί το θόρυβο χαμηλών συχνοτήτων παραμένει το ίδιο αλλά διαχωρίζεται σε δύο μέρη, το ένα, επηρεάζει τον αριθμό των φορέων και το άλλο την ενεργή ευκινησία. Θεωρούμε ότι αυτή η ιδέα χρειάζεται περισσότερη μελέτη.
Από την άλλη πλευρά, η μελέτη της εξέλιξης της πυκνότητας παγίδων διηλεκτρικού με το πάχος οξειδίου για τους δυο τύπους τρανζίστορ, n και p, απέδειξαν ότι η μελέτη του θορύβου χαμηλών συχνοτήτων εξαρτάται πολύ περισσότερο, απ’ ότι θεωρούσαμε έως τώρα, από την διαδικασία κατασκευής των τρανζίστορ, ειδικότερα για τα τρανζίστορ τύπου n. Τα αποτελέσματα απέδειξαν ότι η πυκνότητα παγίδων διηλεκτρικού για τρανζίστορ τύπου n μεταβάλλεται από μία τεχνολογία σε μία άλλη παρότι το πάχος οξειδίου παραμένει το ίδιο. Ο λόγος είναι ο διαφορετικός τρόπος κατασκευής της κάθε τεχνολογίας ο οποίος επηρεάζει την ποιότητα της διεπαφής μεταξύ της πύλης και του καναλιού και κατά συνέπεια μεταβάλλει τον αριθμό των παγίδων διηλεκτρικού. Αντίθετα, για τα τρανζίστορ τύπου p μπορούμε να συμπεράνουμε ότι η πυκνότητα παγίδων διηλεκτρικού είναι αντιστροφώς ανάλογη του πάχους οξειδίου και δεν εξαρτάται ιδιαίτερα από την τεχνολογία της κάθε τεχνολογίας. Ο γενικός κανόνας των σχεδιαστών κυκλωμάτων ότι τα τρανζίστορ τύπου p είναι λιγότερο θορυβώδη σε σχέση με τα τύπου n έχει σωστό για τις τεχνολογίες μέχρι της τεχνολογίας 28nm όπου φαίνεται ότι παρουσιάζουν το ίδιο επίπεδο θορύβου.

Το δεύτερο μέρος της διατριβής περιλαμβάνει τη μελέτη της μεταβλητότητας του θορύβου χαμηλών συχνοτήτων. Η μελέτη αυτή πραγματοποιήθηκε με στατιστικές μετρήσεις του θορύβου χαμηλών συχνοτήτων σε σχέση με την επιφάνεια των τρανζίστορ και των διαφορετικών τεχνολογιών. Η μεταβλητότητα του θορύβου μελετήθηκε εκτενώς σε αυτή τη διατριβή. Αρχικά, προσπαθήσαμε να εξηγήσουμε την έννοια της μεταβλητότητας του θορύβου χαμηλών συχνοτήτων μέσω του φαινομένου RTS. Στη συνέχεια παρουσιάσαμε ένα χαρακτηριστικό παράδειγμα της επίδρασης του φαινομένου της μεταβλητότητας του θορύβου στη λειτουργία μιας μνήμης SRAM. Η μεταβλητότητα του θορύβου στις τεχνολογίες συμπαγούς πυριτίου και FD-SOI ερμηνεύθηκε με βάση ενός μοντέλου που βασίζεται στο θόρυβο RTS. Με βάση αυτό το μοντέλο, έχουμε καταφέρει να ερμηνεύσουμε και να προβλέψουμε με ακρίβεια και λεπτομερώς τη μεταβλητότητα του θορύβου σε τρανζίστορ συμπαγούς πυριτίου της τεχνολογίας 28nm. Επεκτείναμε αυτό το μοντέλο στην τεχνολογία 28nm FD-SOI λαμβάνοντας υπόψη και άλλες παραμέτρους όπως η επίδραση της ευκινησίας των φορέων και της δεύτερης διεπιφάνειας σε αυτή την τεχνολογία. Η μελέτη της μεταβλητότητας του θορύβου στην τεχνολογία 28nm FD-SOI ξεκίνησε με την εισαγωγή της δεύτερης διεπιφάνειας στον κατασκευαστή. Στη συνέχεια, για πρώτη φορά, εισάγαμε την επίδραση της ευκινησίας των φορέων και της δεύτερης διεπιφάνειας σε αυτή την τεχνολογία. Η μελέτη της μεταβλητότητας του θορύβου στην τεχνολογία 28nm FD-SOI ξεκίνησε με την εισαγωγή της δεύτερης διεπιφάνειας στο μοντέλο της τεχνολογίας συμπαγούς υποστρώματος. Στη συνέχεια, για πρώτη φορά, εισάγαμε την επίδραση της ευκινησίας των φορέων στο αρχικό μοντέλο. Η σύγκριση των πειραματικών δεδομένων με αυτούς των προσομοιώσεων απέδειξε ότι η δεύτερη διεπιφάνεια έχει ασθενή επίδραση στη συνολική συμπεριφορά της μεταβλητότητας του θορύβου για τα τρανζίστορ της τεχνολογίας FD-SOI. Το αποτέλεσμα
αυτό ίσως να οφείλεται στην μικρότερη τιμή της χωρητικότητας του μονωτή της πίσω πύλης σε σχέση με αυτή της πάνω πύλης. Η περαιτέρω ανάλυση του φαινομένου σε αυτό τον τύπο τεχνολογίας πρέπει να πραγματοποιηθεί προκειμένου να ελεγχθεί η ισχύς του μοντέλου προσομοίωσης.

Επιπλέον, για πρώτη φορά πραγματοποιήθηκε μια λεπτομερής έρευνα για τη μεταβλητότητα του θορύβου χαμηλών συχνοτήτων σε συνάρτηση των διάφορων τεχνολογιών συμπαγώς πυριτίου. Τα αποτελέσματα αποκαλύπτουν ότι η μεταβλητότητα του θορύβου συμπαγώς πυριτίου και της πάνω πύλης σε σχέση με τη δύο πεδίου τύπου του CMOS. Αυτά τα αποτελέσματα συσχετίζονται με τη μείωση της στατικής κατασκευής των τρανζίστορ (αναντιστοιχία της τάσης αντιστοιχία της τάσης κατωφλίου, mismatch). Επίσης, τα πειραματικά αποτελέσματα αποκάλυψαν ότι η μεταβλητότητα είναι ένα πιο περίπλοκο φαινόμενο και συνδέεται ιδιαίτερα στα χαρακτηριστικά της διαδικασίας κατασκευής των τρανζίστορ και όχι μόνο στην ποιότητα της διεπαφάνειας.

Το τελευταίο μέρος αυτής της διατριβής αφορά μια σύγχρονη ερευνητική πρόκληση, δηλαδή την αντικτυποποίηση του φαινομένου χαμηλών συχνοτήτων σε συνάρτηση των διακυμάνσεων RTS ως πηγές μιας μεταβλητότητας για τις αναλογικές και ψηφιακές εφαρμογές κυκλωμάτων. Παρουσιάσαμε έναν λεπτομερή χαρακτηρισμό και μοντελοποίηση του θορύβου χαμηλών συχνοτήτων στους CMOS αντιστροφέες (inverters). Το μοντέλο θορύβου αναπτύχθηκε με βάση τη διακύμανση του αριθμού των φορέων των τρανζίστορ χρησιμοποιώντας την έννοια της φασματικής πυκνότητας ισχύος στη διακύμανση της τάσης επίπεδων ζωνών ή της τάσης κατωφλίου. Αυτή η παραδοχή μας επέτρεψε να περιγράψουμε με ακρίβεια τον θόρυβο χαμηλών συχνοτήτων της τάσεως εξόδου, αλλά και του ρεύματος φορτίου ως συνάρτηση της τάσεως εισόδου από έναν αντιστροφέα CMOS της τεχνολογίας των 45nm. Αυτή η προσέγγιση για την ερμηνεία του θορύβου χαμηλών συχνοτήτων σε CMOS αντιστροφέες θα μπορούσε να αποτελέσει ένα χρήσιμο εργαλείο για την επίδραση των χρονικών διακυμάνσεων RTS στη στατική και δυναμική λειτουργία τους. Και, θα μπορούσε να χρησιμοποιηθεί για την πρόβλεψη της επίδρασης που θα έχουν οι δυναμικές διακυμάνσεις λόγω περίπλοκης αποστολής φορέων στη στατική κατασκευή των τρανζίστορ (static noise margin) και της δυναμικής σταθερότητας των κυκλωμάτων SRAM.

Η επίδραση της δυναμικής μεταβλητότητας λόγω των χαμηλών συχνοτήτων διακυμάνσεων στη λειτουργία των αναστροφών CMOS, που αποτελούν το βασικό συστατικό των κυκλωμάτων SRAM, ερευνήθηκε στα πλαίσια αυτής της εργασίας. Η πειραματική μεθοδολογία για να χαρακτηρίσει η επίδραση της δυναμικής μεταβλητότητας σε έναν
αναστροφέα CMOS βασίστηκε στις μετρήσεις του ρεύματος φορτίου, μετά από την εφαρμογή μιας τάσης εισόδου σε διαφορετικές χρονικές περιόδους. Με αυτόν τρόπο αποδείξαμε ότι, για τους μικρούς χρόνους ανάδου της τάσης εισόδου, οι χαρακτηριστικές του ρεύματος φορτίου σε συνάρτηση με την τάση εισόδου παρουσιάζουν μια τεράστια διασπορά εξαιτίας του θορύβου χαμηλών συχνοτήτων. Η επίδραση τέτοιων δυναμικών πηγών μεταβλητότητας στα χαρακτηριστικά της τάσης εισόδου του αναστροφέα αποκαλύπτει μια μείωση στο περιθώριο θορύβου της τάξης του 20% για το μικρότερο αναστροφέα που μετρήθηκε.
Table of contents

Acknowledgments ........................................................................................................... i
Scientific Publications ................................................................................................. ii
English abstract ........................................................................................................... iii
Greek abstract .............................................................................................................. viii
French abstract ........................................................................................................... 145
Table of contents .......................................................................................................... xiv

Chapter 1: Introduction ..................................................................................................... 1
1.1 Device scaling ........................................................................................................... 2
1.2 Impact of scaling on the device LFN and electrical properties ................................... 3
1.3 Beyond the conventional technology ..................................................................... 6
1.4 Proposed nanoscale bulk and FD-SOI MOSFET ...................................................... 11
1.5 Objectives and challenges of thesis ...................................................................... 16
1.6 Outline of thesis .................................................................................................... 18
References ................................................................................................................... 20

Chapter 2: Low frequency noise in bulk MOSFETs ...................................................... 24
2.1 LFN as a characterization tool .............................................................................. 25
2.2 LFN models .......................................................................................................... 26
  2.2.1 Carrier number fluctuations model ............................................................... 26
  2.2.2 Hooge mobility fluctuations model ............................................................... 29
  2.2.3 Carrier number with correlated mobility fluctuations model ....................... 30
2.3 Development of new LFN compact model for nanoscale bulk MOSFETs ............. 32
2.4 Noise measurement setup ..................................................................................... 34
2.5 Experimental verification of the LFN compact model ............................................. 36
  2.5.1 Linear region ................................................................................................. 37
  2.5.2 Non linear region .......................................................................................... 40
  2.5.3 Generic CMF LF noise compact model ........................................................ 44
2.6 Experimental LFN measurements in bulk n- and p-MOSFETs of different technology
   nodes ......................................................................................................................... 44
  2.6.1 CMOS 0.25µm ............................................................................................. 45
  2.6.2 CMOS 0.18µm ............................................................................................. 47
  2.6.3 CMOS 0.12µm ............................................................................................. 49
## Table of contents

2.6.4 CMOS 90nm ........................................................................................................... 52  
2.6.5 CMOS 65nm ........................................................................................................ 54  
2.6.6 CMOS 45nm ........................................................................................................ 57  
2.6.7 CMOS 28nm ........................................................................................................ 59  
2.6.7.1 CMOS 28nm GO2 ............................................................................................. 60  
2.6.7.2 CMOS 28nm RVT ............................................................................................ 61  
2.6.7.3 CMOS 28nm SLVT .......................................................................................... 63  
2.6.7.4 CMOS 28nm HPA ......................................................................................... 65  
2.6.7.5 Comparison CMOS 28nm .............................................................................. 67  
2.7 Comparison of LFN in CMOS bulk technology nodes ........................................... 68  
2.8 Conclusions ............................................................................................................ 73  
References ..................................................................................................................... 75  

Chapter 3: Low frequency noise variability in bulk and FD-SOI MOSFETs ............ 77  
3.1 Origin of the LFN variability .................................................................................... 78  
3.2 Impact of the LFN variability on circuit operation .................................................. 81  
3.3 Statistical analysis of the LFN variability ............................................................... 82  
3.4 Experimental results of the LFN variability measurements ................................... 87  
   3.4.1 CMOS 28nm Bulk devices ................................................................................. 87  
   3.4.2 CMOS 28nm FD-SOI devices ......................................................................... 91  
3.5 Experimental results of the LFN variability in bulk n- and p- MOSFETs of different  
   technology nodes ........................................................................................................ 101  
3.6 Development of the LFN variability model ............................................................ 104  
   3.6.1 Bulk Transistors .............................................................................................. 104  
   3.6.2 FD-SOI Transistors ....................................................................................... 107  
      3.6.2.1 FD-SOI Transistors $V_b=0V$ ................................................................ 113  
      3.6.2.2 FD-SOI Transistors $V_b=\pm10V$ ............................................................ 115  
3.7 Conclusions ............................................................................................................ 118  
References ..................................................................................................................... 119  

Chapter 4: Low frequency noise in CMOS inverters ............................................... 120  
4.1 Background of CMOS inverters ............................................................................ 121  
4.2 Proposed LFN model in nanoscale bulk CMOS inverters .................................... 123  
4.3 Experimental measurements in 40nm CMOS bulk inverters ............................. 127  

xv
Table of contents

4.4 Model verification........................................................................................................... 128
4.5 Dynamic variability of CMOS inverters........................................................................132
4.6 Conclusions.......................................................................................................................137
References............................................................................................................................139

Chapter 5: Summary and future work ................................................................. 141
  5.1 Summary..........................................................................................................................142
  5.2 Future work.......................................................................................................................144
Chapter 1: Introduction

1.1 Device scaling................................................................. 2
1.2 Impact of scaling on the device LFN and electrical properties... 3
1.3 Beyond the conventional technology................................. 6
1.4 Proposed nanoscale bulk and FD-SOI MOSFETs............... 11
1.5 Objectives and challenges of thesis.................................. 16
1.6 Outline of thesis............................................................... 18
References............................................................................ 20
Chapter 1
Introduction

1.1 Device scaling

During its short history, the electronics industry has gone through a development that was never seen before. The electronics industry developed in a number of steps. First, the very basics of the industry started in 1901, with the introduction of the radio. The next step was when in 1948 the Bell Telephone Laboratories invented the transistor [1]. The invention of the transistor was a major breakthrough in the evolution of electronics industry. The reason was simple, it is easy to produce it in mass scale and it is the basic component of integrated circuits which are the heart of modern electronic circuits. There are several types of transistors nowadays, BJT, JFET, MOSFET, IGFET and others, but the most important of them in terms of usage is the MOSFET. A potential barrier controlled by the gate field modulates the current flow from source to drain that is the main operation of MOSFETs. Its simplicity, together with the fact that it is available in complementary n-FET and p-FET versions, is the underlying basis for the success of CMOS technology.

The CMOS technology is the basis of the electronic market. As the electronic market, we define all the products that use integrated circuits, TVs, stereos, computers, mobile phones, cars etc. However, as the year passes the needs of the market are changing. So today people demands for fast, low power and as small electronic circuits as possible. In order to fulfill the needs of the market, but also the global energy supply problem, the CMOS technology evolved by diminishing the MOSFET area. This procedure is known as device scaling.

The semiconductor industry ability to follow Moore’s law [2] has been the engine of a virtuous cycle: through transistor scaling, one obtains a better performance-to-cost ratio of products, which induces an exponential growth of the semiconductor market. This in turn allows further investments in semiconductor technologies which will fuel further scaling. According to the ITRS roadmap, an organization created by the biggest semiconductor industries in order to ensure cost-effective advancements in the performance of the integrated circuit, the scalability of MOSFETs will follow the trend showing in Fig. 1.1 [3]. The graph is showing the minimum gate length of a MOSFET versus the possible year of production. The minimum length of a transistor was diminished from 130 to 28 nm in almost 20 years. But what do we really earn from reducing the dimensions of a MOSFET?
The idea of scaling the MOS transistors is to reduce the physical dimensions by the same amount while increasing the body doping and reducing the applied voltage to cause the depletion regions within the devices to scale as much as the other dimensions. The most important result of scaling down the transistors is increase of the circuit density and speed [4-5]. In practice, these benefits result in sophisticated computers of faster operation, in mobile phones functioning for longer times with a simple battery and in all the countless applications of electronic industry that are a part of our everyday life. The question that arises is if all these benefits do not introduce any constraints or problems to the functionality of the devices. The answer to this question will be analyzed in the next sub-chapter.

![Diagram](image)

Fig. 1.1: The minimum gate length of a MOSFET versus the possible year of production.

### 1.2 Impact of scaling on the device electrical and LFN properties

As everything in real life, the scaling down of the transistors has some positive aspects which were developed above, but also some negative one’s. A MOSFET device is considered to be short when the channel length $L$ is in the same order of magnitude as the depletion-layer widths ($X_j$) of the source and drain junction as shown in Fig. 1.2. As the technology scaling reaches channel lengths less than $1\mu m$, some secondary effects, which did not exist for long channel devices, are playing now a key role on the functionality of MOSFETs. We will present the most important effects of the device scaling on the electrical and LFN properties of the MOSFET.
The most important results of the device scaling on the electrical properties of MOSFETs are summarized as follows:

1. **Loss of electrostatic control of the channel**: When the gate length is downsizing, the lateral electric field increases resulting in loss of the threshold voltage control by the gate and gives rise to a phenomenon called in literature Short Channel Effect (SCE). In the saturation region, the main electrostatic effects are the DIBL (Drain Induced Barrier Lowering), which is included in the subthreshold slope and in the threshold voltage roll-off and the channel length modulation (CLM) [6, 7]. This effect is due to the drain biasing which creates a depleted area instead of inversion charge at the drain side.

2. **Power Consumption**: As the transistor becomes smaller, the gate oxide thickness follows as well. The thin oxide between the gate and the channel permits direct tunneling of carriers through the gate, creating a leakage current that increases the power consumption of the device.

3. **Carrier Transport**: As the channel length becomes smaller, due to the lateral extension of the depletion layer into the channel region and to the increase of the longitudinal electric field, the carriers transport into the channel is affected by the surface scattering, velocity saturation and impact ionization. All these phenomena reduce the carrier mobility thus the “ON” current of the device and degrade its performance [8-9].

4. **Series Resistance**: As device dimensions are scaled down, the on-resistance ($R_{on}=V_{dd}/I_{on}$) of the device is improved (reduced) and it becomes important to limit the source/drain series resistance ($R_{series}$) to be a small fraction of $R_{on}$ to satisfy the device performance requirements. While device performance has increased for each technology node, it has been difficult to scale down $R_{series}$ for sub-100nm generations. $R_{series}$ is expected to be ~20% of the total Ron [3], a significant fraction, yet no known solutions are available to meet or limit these.
projections. Therefore, $R_{\text{series}}$ reduction presents one of the biggest challenges for continued aggressive CMOS scaling.

The main objective of this thesis is to investigate the impact of the transistor scaling on the low frequency noise (LFN). At this point, we would like to emphasize what we will call noise in this thesis. In Fig. 1.3, we plotted the measured voltage of a device versus time. Noise is the current (or voltage) variations around the expected DC value, the dotted black line in Fig. 1.3.

![Fig. 1.3: The measured voltage of a device versus time.](image)

It should be noted that the noise is not an external phenomenon as the crosstalk and the electromagnetic radiation that can affect the performance of a device or a circuit and at the same time, it can be eliminated with proper shielding and layout design. Internal noise in an electronic device is a random, spontaneous perturbation of a deterministic signal inherent to the physics of the device. It cannot be eliminated, but it can be reduced. This work will be focused on the study of a particular type of noise called low frequency or flicker or $1/f$ noise. The LFN is the noise in which the spectrum is inversely proportional to the $1/f^\gamma$ with $\gamma$ close to one. This type of noise appears on the low-frequency part of the spectrum.

Shrinking of the transistor area jeopardizes the LFN behavior of the device. Today it is well known that the miniaturization of the devices has lead to an increase of low frequency noise [10]. The gate voltage power spectral density is inversely proportional to the device area and, therefore, shrinking of the device area increases the LFN level. Furthermore, as the transistor dimensions lie in the micro-nano scale region, a new type of noise called random telegraph noise (RTS) appears. This type of noise is connected with the LFN, as it has the same origin, with the main difference being the carrier trapping/detrapping in a single oxide trap near the gate dielectric/silicon interface. The so-called LFN variability, which is based on
Chapter 1. Introduction

RTS, is the difference in noise level from different devices on the same wafer. The variability is a major concern for the new technology nodes, since it rises as the area of the device becomes smaller (see details in Chapter 3).

1.3 Beyond the conventional technology

In order to overcome all the problems appearing in the evolution of the semiconductor technology, a number of issues should be addressed. In the present thesis, we address the most important of them and refer to the reasons that the conventional technology probably will be left behind.

As the device dimensions become progressively smaller, the design of MOSFETs has been governed by the scaling criteria proposed by Dennard et al. [11] in the early of 1970’s. This scaling concept was based on the assumption that if the doping, the dimensions and the voltages are scaled down with the same factor, then the electric field configuration of the scaled device will be the same as for the large one. However, constant field scaling results in two inherent problems, the built-in potentials do not scale because they are tied to the silicon band gap energy, which does not change (except by changing to a different semiconductor). Furthermore, the sub-threshold slope cannot be scaled (except by lowering the temperature), since it is primarily determined by the thermodynamics of the Boltzmann distribution of carriers. Consequently, the threshold voltage cannot be scaled too far, or else leakage currents will become excessive. Both of these limitations cause deviations from simple scaling theory as the supply voltages approach 1V.

The changes in the structure of a MOSFET from the time that it was discovered till the late 1960’s were tremendous. The gate metal was replaced by a polysilicon gate which could serve as a mask for self-aligned formation of the source and drain, Figs. 1.4 and 1.5 [12]. In this way parasitic gate-to-source and gate-to-drain capacitances associated with gate overlap could be controlled. Sidewall spacers were added to allow the source and drain to be set at the proper distance under the gate edge which also made possible the introduction of the lightly doped drain structure (LDD) as shown in Fig. 1.6 [13]. The shallow, lightly doped part of the drain and source served to reduce the maximum electric field. The deeper heavily doped part minimized the resistance. The gate and the source/drain diffusions were silicided, to reduce further the sheet series resistance [14]. The introduction of ion implantation (rather than simple surface-originated diffusion) allowed for the tailoring of vertical doping profiles – which was critical for preventing latch-up and punch-through and for setting the threshold voltage. Shallow trench isolation (STI) was introduced to permit tighter packing of structures
and to replace the standard LOCOS isolation technique. STI is created early during the semiconductor device fabrication process, before transistors are formed. The key steps of the STI process involve etching a pattern of trenches in the silicon, depositing one or more dielectric materials (such as silicon dioxide) to fill the trenches and removing the excess dielectric using a technique such as chemical-mechanical planarization.

![Figure 1.4: Al gate metal](Image)

![Figure 1.5: Poly-Si gate metal](Image)

![Figure 1.6: Sidewall spacers, LDD](Image)

![Figure 1.7: halo implants](Image)

It was at the 1990’s when the SCE began to create real problems. The scaling down of the gate length created an unaccepted rise of the lateral electric field, which in consequence led to threshold voltage degradation. At that time, it was the channel engineering that should be changed. Channel engineering is mostly intended to control threshold voltage and prevent punch-through. Increasing channel doping reduces the width of the depletion region thus minimizing the SCE. Halo (or pocket) implants were introduced [15] to control short channel effects by reducing the width of the depletion region and to increase device resistance to punch-through. The doping profile should be changed as well. A super-steep retrograde doping profile [16] in the channel serves for a better control of threshold voltage while keeping mobility high due to low surface doping (Fig. 1.7). All these were not enough in order to enter the 90 nm technology node and going down. Rotated substrate and strain/stress techniques were introduced to boost the performance of the devices in the below 90 nm area. [17-18].
After the channel, source and drain engineering, the gate stack should be changed to meet the demands of newer technology nodes. SiO\textsubscript{2} has been preferred as gate insulator from the early stages of CMOS technology, because it was easy to deposit and offered very good isolation from the channel. Furthermore, the oxide thickness played a key role in the performance improvement of the MOSFET. There were two reasons to reduce the oxide thickness. The first one had to do with the “ON” current state of the device: By reducing the oxide thickness, the “ON” current is becoming higher. The second one was the control of the threshold voltage roll off and by consequence the sub-threshold leakage current. Thus, the shrinking down of the gate oxide thickness was an important factor in order to improve the performance of the device.

The problem appeared when the oxide thickness became too small. Manufacturing very thin oxides is not an easy task. Oxide breakdown is another limiting factor. If the oxide is too thin, the electric field in the oxide can be so high as to cause destructive breakdown. Yet another limiting factor is the long-term operation at high field, especially at elevated chip operating temperatures, breaks the weaker atomic bonds at the Si/SiO\textsubscript{2} interface, thus creating oxide charge and $V_{th}$ shift. $V_{th}$ shift causes change in the circuit behavior and raises unwanted reliability concerns.

The most serious limiting factor of the scaling down of the oxide thickness was the direct tunneling leakage current due to the thin gate oxide thickness. As a result of decreased thickness, gate leakage current obviously grows, increasing power consumption of the entire chip, which is an undesirable effect for battery powered mobile systems. It is estimated that gate leakage current increases approximately 30 times every technology generation, as opposed to 3–5 times increase of channel leakage current [19]. Apart from leakage current, the reduction of gate-oxide thickness increases the susceptibility of the device to boron penetration from the poly-Si gate into the channel. Gate-induced drain leakage (GIDL) is another significant leakage mechanism, resulting from depletion at the drain surface below the gate-drain overlap region. Replacing silicon dioxide with silicon oxynitride (SiO\textsubscript{x}N\textsubscript{y}) was the most widely used solution to this problem [20]. The introduction of silicon oxynitride for gate insulator was accompanied with two important penalties, the NBTI degradation for p-channel MOSFET and the degradation of the LFN [21].

The continued downscaling of CMOS devices beyond the 65-nm technology node required, among many new technology features, high-$\kappa$ gate dielectrics to achieve small (~1 nm) equivalent oxide thickness (EOT) while maintaining low gate leakage current [22]. Often, a high-$\kappa$ dielectric has good insulating properties and creates high capacitance (hence
Chapter 1. Introduction

the term “high-k”) between the gate and the channel. Both of these are desirable properties for high performance transistors. “κ” is an engineering term for the ability of a material to hold electric charge. Think of a sponge. It can hold a lot of water. Wood can hold some but not as much. Glass cannot hold any at all. Similarly, some materials can store charge better than others, hence has a higher “κ” value. In addition, because high-k materials can be thicker than silicon dioxide, while retaining the same desirable properties, they greatly reduce leakage. Intensive research has been devoted to find and optimize high-κ dielectric materials for integration with CMOS technology. The implementation of the high-κ dielectrics in MOS transistors faced several challenges such as mobility degradation, increased low-frequency noise and threshold-voltage shifts and instabilities. These problems are related to the high density of traps and fixed charges contained in the bulk or at the interfaces of the high-κ stack. Fixed charges and charged traps give rise to Coulomb scattering and is one reason behind the lower mobility in high-κ transistors compared to the ones using SiO₂. Other sources of scattering responsible for the mobility degradation include remote low-energy surface optical (SO) phonons arising from the polarization of the high-κ dielectric, remote surface roughness and crystallization.

After all the technology innovations and solutions that have been invented to continue implementing new devices with improved characteristics, why do we have to change the conventional technology? What are the physical limits that prevent us to continue scaling down the devices with the existing technology? We will try to refer to the most important limiting factors that led us to the introduction of new devices architecture.

Many reviews have been written about future prospects for Si MOS Field-Effect transistors (MOSFETs) and CMOS limiting factors [23]. We are going to discuss the issues presented in the new technology nodes and perhaps the limiting factors to continue scaling down the conventional MOSFETs.

In a conventional bulk-Si MOSFET, as the scaling down process is continuing, the doping concentration of the channel should be increased as the source drain junctions distance is decreased in order to avoid electrostatic coupling of the junctions beneath the channel surface. The higher doping level results in degraded low-field mobility thus lower “ON” current. Furthermore, as the dimensions of the device are becoming smaller, the manufacturing process cannot control the exact placement of the dopants giving rise to statistical variations. The so called variability is going to be a major constraint to continue diminishing the transistor.
The gate oxide thickness is another parameter we have to take into account for submicron technology nodes. The semiconductor industry has found solutions to the gate leakage current increase as the gate oxide thickness is becoming small by replacing the SiO$_2$ with new materials as mentioned above. However, is it possible to continue shrinking down the device as well as the oxide thickness? The answer is probably not. The direct tunneling current and the boron penetration through the gate oxide to the channel will play an important role to the 28 nm and beyond technology nodes.

The voltage issue is another factor that influences the scaling of CMOS. Voltage scaling is limited on several fronts. The built-in junction voltages are set by the 1.1 eV bandgap of Si which does not scale. Consequently, as the applied voltages are scaled down toward 1 V, the internal fields do not automatically scale as desired. A similar difficulty occurs in trying to scale the threshold voltage, which is tied to the no scaling behavior of the sub-threshold slope and its influence on the “OFF” current. At very low values, the supply voltage is also fundamentally limited by the need for sufficient gain to provide logic functionality.

The manufacturing factor is an important issue as well. In order to minimize subsurface channel leakage current, the depth of the source and drain junctions must be reduced as the channel length is reduced. The formation of ultra-shallow junctions is a significant technological challenge (DIBL control), particularly because low sheet resistances are needed for high transistor drive current.

Although most of the non-scaling effects that have been described have the potential of halting CMOS scaling at the point at which they cause circuits to cease functioning, that is not the most important scaling limit. The most significant scaling limit is created by the power dissipation associated with the various leakage mechanisms. This limit depends on the application, since different applications can tolerate different amounts of static leakage power, so that there is no single end to scaling, but rather there are different optimum ends to scaling for different applications. High-power, high-performance servers can accept much higher static leakage dissipation than portable battery-powered devices and so the former can be more aggressively scaled than the latter.

Let us proceed with the introduction of the most popular solutions to replace the conventional bulk CMOS technology. Thin-body MOSFET structures such as the ultra-thin body (UTB) transistor as shown in Fig. 1.8 [24], and the double-gate transistor or FinFET [25] as shown in Fig. 1.9, are distinctly different from their bulk-Si counterpart in that no current conduction path between the source and drain is far removed from a controlling gate electrode. The gate voltage can therefore effectively control the electric potential throughout
the channel, without the need for high-channel dopant concentration. The depth of the source and drain junctions is naturally limited to the thin body thickness, so that formation of ultra-shallow source and drain junctions is not an issue. Thus, some of the issues for scaling bulk-Si MOSFETs can be circumvented through the adoption of thin-body transistor structures. The choice between one of them is based on the demands. Either way each one of these solutions has both advantages and disadvantages as well. It is not the purpose of this thesis to analyze these devices.

![Ultra-Thin Body Fully Depleted Silicon On Insulator MOSFET](image1)

**Fig. 1.8:** Ultra-Thin Body Fully Depleted Silicon On Insulator MOSFET

![Double-Gate MOSFET](image2)

**Fig. 1.9:** At the left 2-D representation of Double Gate MOSFET while the 3-D is on the right.

### 1.4 Proposed nanoscale bulk and FD SOI MOSFETs

Below we address the proposed nanoscale bulk and eventually Fully Depleted Silicon On Insulator (FD-SOI) MOSFETs that can continue the scaling process in the semiconductor industry.

The main challenge in 32/28 nm bulk CMOS technology node was the gate leakage issue, as already mentioned in previous sections. The gate leakage current originates from the scaling down of the oxide thickness. There are three main issues to the device functionality when the oxide thickness is becoming small. The first one is the transistor drivability degradation through the reduction of the “ON” current ($I_{ON} \sim 1/t_{ox}$). The second one is the
Chapter 1. Introduction

transistor control degradation because of the enormous raise of the electric field inside the channel. The third one is the transistor variability degradation. The matching performance of the device is proportional to the oxide thickness.

There were many steps to do in order to solve the problem of the gate stack. In order to alleviate all these problems, the gate stack changed from the standard pure poly/SiON to the high-\( \kappa \)/metal gate. At first, the process engineers tried to change the standard poly/SiON gate stack with a Poly/high-\( \kappa \) one. The gate current leakage was reduced, but other problems appeared. One of them was the threshold voltage instability during operation. Fermi pinning in the gate oxide interface caused high threshold voltages. Defects and charges within the gate stack can cause large instabilities at the\( V_{th} \) of the device [26-27]. Then we had carrier mobility degradation caused by scattering by the SO phonons [28]. Another issue was the degradation of the reliability. Bias Temperature Instability (BTI) is a degradation phenomenon in MOS Field Effect Transistors (MOSFETs), known since the late sixties for SiO\(_2\) dielectrics [29-30]. It is now commonly admitted that under a constant gate voltage and an elevated temperature, a build up of charges occurs either at the interface Si/SiO\(_2\) or in the oxide layer, leading to the reduction of MOSFET performance. Unlike SiO\(_2\), the high-\( \kappa \) dielectrics, such as Hf-based dielectrics, present serious instabilities after negative and positive bias temperature stresses. Finally, but not least, the LFN degradation was very strong. Today, it is known that the 1/f noise magnitude and effective oxide trap density in the high-\( \kappa \) dielectric transistors are one to two orders of magnitude higher than those in SiO\(_2\) and SiON devices [31–32].

The next step was the introduction of the Poly/high-\( \kappa \)/SiON gate stack which managed to solve some of the issues previously discussed. With this kind of gate stack, it has been managed to have a carrier mobility and reliability recovery, but the Fermi pinning was still there. Finally, the solution was found in the metal/high-\( \kappa \)/SiON gate stack. The proposed 28 nm technology node device to overcome all the issues from the scaling down of the devices has the following characteristics. The gate first stack consists of TiN as metallization and Hf-based dielectric as gate oxide with an equivalent oxide thickness (EOT) 14 Å and 17 Å for the n- and p-MOS transistors, respectively. The passage from polysilicon materials to other types for the construction of the gate stack introduced new integration scheme. Today, there are two different approaches to create the gate stack in MOSFETs, the gate first and the gate last. The gate first is the simpler one because it is very close to the conventional one. The metal gate is introduced early in the fabrication of the transistor with the thermal annealing, almost at 1000°C. In the gate last approach the procedure is completely different, the metal is deposited
after the annealing of source/drain avoiding thus the exposure to high temperatures. The metal gate is TiN based insertion layer with lanthanum and aluminum as “dopants” for respectively n- and p-MOS transistors in order to modulate the work function. The abandon of polysilicon for gate stack made the co-integration of the work function for n- and p-MOS transistors difficult, which is achieved by simply implanting of “donors” or “acceptors” respectively. In order to alleviate these problems two possibilities were possible. The first was the use of a metal with a work function close to the one of silicon. We are talking about materials with quasi-midgap which allows obtaining a “symmetric” threshold voltage which works well for both n- and p-MOS devices. The second one is concerning the use of two different metals one for n-MOS and another for p-MOS. The high-κ material is Hf-based and it helps to silicate for material thermal stability and interfacial layer thickness control. The use of nitrogen helps to further increase thermal (delays crystallization) and interfaces stability. The interfacial layer between the channel and the gate oxide was used for mobility control and stabilization of high-κ/channel interface. The channel is bulk Si for n-MOS transistors and SiGe for p-MOS transistors for threshold voltage adjustment and boost of performance.

At the same time, a new technology introduced side by side with the bulk one, the so-called Fully Depleted Silicon On Insulator which we address at the following and probably will be the technology for the future ahead.

We would like to make a short, but necessary, introduction to the Silicon On Insulator (SOI) technology. We are not going to enter into details which are not the purpose of this thesis, but we will give important aspects of SOI technology.

Fig. 1.10: The passage from Bulk like MOSFET to Partially Depleted Silicon On Insulator and finally to Fully Depleted Silicon On Insulator.
In Fig. 1.10, we have shown the various SOI transistors and the main differences from their Bulk “ancestor”. In the Partially depleted option, the Body is made thick and the inversion region is not extended over the full depth of the Body. The “floating” body boosts the performance, but introduces some drawbacks such as the history and kink effect. Planar Fully Depleted Silicon on Insulator (FD-SOI) technology relies on an ultra-thin layer of silicon over a Buried Oxide (commonly called box). Two flavors of buried oxide can be used: standard thickness (typically 145 nm) or ultra-thin BOX, for example 10 – 25 nm (UTBOX, Ultra-Thin Buried Oxide). FD-SOI solves, with less process complexity, scaling, leakage and variability issues to further shrink CMOS technology beyond 28 nm. FD-SOI offers the following major benefits:

- **The excellent electrostatic control** of the transistor, intrinsic to FD-SOI, acts as a performance booster and enables lower $V_{DD}$ (therefore lower power consumption) while reaching remarkable performance. From a physical point of view, the very thin silicon layer enables the silicon under the transistor gate (the body of the transistor) to be fully depleted of charges. The gate can now very tightly control the full volume of the transistor body. That makes it much better behaved than a Bulk CMOS transistor, especially as supply voltage gets lower and transistor dimensions shrink.

- In addition, **FD-SOI does not require doping in the channel**. Therefore, it reduces the random dopant fluctuation, thus drastically cutting transistor threshold ($V_{th}$) variability. In particular, this enables stable, dense and high-yielding SRAM, functional at very low $V_{DD_{min}}$ (even in near- or sub-threshold mode with a good SNM). Simulations and early silicon data predict that at 22 nm node, 6T SRAM macros on FD-SOI could reach 6-sigma yield at $V_{DD}$ as low as 0.5-0.6 V [33].

- **FD-SOI is intrinsically Low Leakage** and regains **good control of Short Channel Effects**. One consequence is the ability to aggressively shrink the gate length, making it easier to fit devices into smaller and smaller pitches and therefore increase the logic density to continue Moore’s law.

These characteristics are mostly consequences of using Ultra-Thin Body devices, as these require no channel doping (and therefore do not suffer from Random Dopant Fluctuation, which is rapidly becoming a major problem for Bulk CMOS) and exhibit excellent electrostatic control of the channel. This in turn translates as: excellent $V_{th}$ variability [34], (low DIBL) –which is a performance boost factor especially at low $V_{DD}$, limited Short
Channel Effects, very good Sub-threshold Slope and minimum junction capacitance and diode leakage.

In addition, an FD-SOI process can be significantly simpler than a Bulk process aimed at the same technology node: the absence of halo doping / pocket implants is an example of simplification, simpler STI (Shallow Trench Isolation) is another one. Use of an ultra-thin BOX may typically be envisaged for some or all of the following reasons: relaxing of silicon thinness requirements (thus limiting need for a continually thinner transistor body at subsequent CMOS nodes like 16 nm-11 nm-8 nm), even better transistor characteristics for some parameters (notably those related to electrostatic control of the channel), ability to locally remove top silicon and BOX to reach the base silicon and co-integrate devices on SOI and devices on Bulk, with only a small step (20-30 nm) between an SOI zone and an uncovered Bulk zone, ability to implant back-planes under the BOX, also to bias them (BOX acting as transistor back-gate). This may be used for shifting $V_{th}$ or for implementing low power design techniques extremely similar to body biasing in Bulk CMOS technologies.

The proposed 28 nm FD-SOI technology node has the following characteristics [35]. The devices are fabricated on substrates with silicon, overlayer of 12nm on top of a 25nm Burried-Oxide (BOX). Final SOI thickness is 7nm after process steps shown in Fig. 1.11.

![Fig. 1.11: 28nm FD-SOI front-end process flow.](image)

FDSoI technology allows a hybrid scheme co-integrating both bulk and SOI devices on the same die. Thin box is opened for bulk parts with NOSOI mask [36]. Thanks to an excellent transistor electrostatic control with FDSoI, physical gate length of devices scaled down up to 24nm (Fig.1.12). Leveraging FDSoI back-side gate capability, a Ground-Plane (GP) implantation has been developed to adjust transistors $V_{th}$. Actually, the GP for logic devices is gate-type whereas the GP of SRAM devices is opposite, in order to adjust
accurately threshold voltage for the entire devices suite. HK/MG process is adjusted to control $V_{th}$ of thin and thick gate oxide devices simultaneously for both n- and p- MOSFETs.

Fig. 1.12: TEM cross-section of n-MOS device with channel length 24nm and 7nm thin SOI.

1.5 Objectives and challenges of thesis

On one hand, low frequency (LF) noise and fluctuations in MOS devices has been the subject of intensive research during the past years. The LF noise is becoming a major concern for continuously scaled down devices, since the 1/f noise increases as the reciprocal of the device area. Excessive low frequency noise and fluctuations could lead to serious limitation of the functionality of the analog and digital circuits. The 1/f noise is also of paramount importance in RF circuit applications where it gives rise to phase noise in oscillators or multiplexors. The development of submicronic CMOS technologies has led to the onset of new type of noises, i.e. random telegraph signals (RTS), yielding large current fluctuations, which can jeopardize the circuit functionality.

On the other hand, the statistical variability in the transistor characteristics is one of the major challenges for coming technological nodes. The detailed knowledge of variability sources is extremely important for the design and manufacturing of variability resistant devices. As can be seen in Fig. 1.13 we plotted the drain current versus gate voltage for a rather small n-MOS device from the 28 nm bulk technology node, the dispersion in drain current values is almost two decades. Whereas the impact of random dopants, line edge roughness and oxide thickness variations is relatively well understood, the role of the polysilicon or metal gate material has only lately been investigated in simulations and experimental confirmation and quantification of its contribution is still lacking [37-38]. In addition, the study of how LFN variability behaves and maybe connects with the other factors
of device variations has never been done. In Fig. 1.14 we are showing an example of the impact of LFN variability by plotting the drain current noise power spectral density versus frequency for n-MOS large and small area (35 dies measured). It can be clearly seen that the noise level is enhanced by 2-3 decades going from the large to the small area device. Fig. 1.15 shows the expected impact of the trap-related noise contribution on Vdd reduction in SRAM design versus technology evolution [39]. As can be seen from Fig. 1.15 the impact of LFN variability in the basic standard cells such as SRAM and DRAM it would be significant for the new technology nodes.

![Graph](image)

**Fig. 1.13:** Drain current versus gate voltage for nMOS device with W/L=1/0.03 μm from 28nm Bulk technology node.

![Graphs](image)

**Fig. 1.14:** The drain current noise versus frequency for nMOS device with a large area at left and for a small one at the right.
Chapter 1. Introduction

Therefore, the research challenges and objectives of this thesis are centered towards the studies of low frequency fluctuations and noise in 32 nm CMOS technologies and beyond. More specifically, the LF noise will be investigated with three objectives: i) the detailed LF noise characterization of new CMOS technologies featuring high-κ metal gate stacks, channel pockets etc, ii) the change of LF noise parameters from different technologies and iii) the impact of LF noise and RTS fluctuations as variability sources for analog and digital circuit applications. The first objective will address the origin of the LF fluctuations in CMOS devices in terms of trap density and defect localization in the gate dielectric and along the channel for various architectures (pocket, Ge channel, FD-SOI etc). The second item will consider the LF noise mismatch resulting from huge dispersion of noise sources from device to device; this will be conducted owing to statistical measurements of LF noise characteristics as a function of device area and technological splits. The third issue will focus on the impact of LF noise or RTS fluctuations on the operation of elementary circuits (inverter, SRAM cell) and regarded as temporal variability source.

1.6 Outline of thesis

The outline of the thesis is the following: In chapter 2, we emphasize in the reasons why LFN is used as a diagnostic tool of the quality of the interface. We refer to the most important models from the literature and then we suggest a new compact model, which can explain the LFN behavior of the nanoscale bulk devices. A detailed analysis of the noise measurement setup will follow, which is of paramount importance in order to fully understand the
mechanisms behind low frequency noise. Our new compact model is verified by comparison with experimental results. We investigate the LFN behavior from 0.25 μm down to 28 nm bulk CMOS technology nodes for both n- and p- MOS devices. For 28nm node, we investigate the behavior of different architecture devices in terms of oxide thickness and channel doping. Thus, we will better understand the impact of new technology breakthroughs in the LFN behavior of the MOSFETs. Finally, we will present for the first time the evolution of LFN through STMicroelectronics CMOS technology nodes in terms of volumetric oxide trap density versus oxide thickness and analyze the effect of each technology process.

The third chapter is entitled low frequency noise variability in bulk and FD-SOI MOSFETs. We will start from the physical origin of the LFN variability and its impact on various circuits operation. We will make a short introduction to the statistical analysis of LFN parameters. Then, we will present the results of the measurements from five bulk technology nodes and from the 28nm FD-SOI technology node. Following, we will present a comparison of the data results and the simulation of the proposed model to explain LFN variability.

The fourth chapter concerns the LFN investigation of an elementary CMOS circuit as the inverter is. We develop the theory behind the basic functionality of CMOS inverters and make a short review of LFN on that circuit. We propose a model to explain the LFN behavior of the inverters, which is compared with experimental results. In addition, we extend our analysis in time domain measurements, the so-called dynamic variability. The impact of RTS on the basic functionality of CMOS inverters from direct measurements of voltage and current characteristics in different time durations is investigated for the first time.

Finally, in chapter 5 we conclude our work and make some suggestions for future investigations concerning LFN and LFN variability in CMOS technology nodes.
References


Chapter 2: Low frequency noise in bulk MOSFETs

2.1 LFN as a characterization tool .......................................................... 25
2.2 LFN models ....................................................................................... 26
   2.2.1 Carrier number fluctuations model ............................................ 26
   2.2.2 Hooge mobility fluctuations model ........................................... 29
   2.2.3 Carrier number with correlated mobility fluctuations model .... 30
2.3 Development of new LFN compact model for nanoscale bulk MOSFETs .... 32
2.4 Noise measurement setup ................................................................. 34
2.5 Experimental verification of the LFN compact model ................. 36
   2.5.1 Linear region .......................................................... 37
   2.5.2 Non linear region ....................................................... 40
   2.5.3 Generic CMF LF noise compact model ................................ 44
2.6 Experimental LFN measurements in bulk n- and p-MOSFETs of different technology nodes ......................................................... 44
   2.6.1 CMOS 0.25µm ........................................................... 45
   2.6.2 CMOS 0.18µm ........................................................... 47
   2.6.3 CMOS 0.12µm ........................................................... 49
   2.6.4 CMOS 90nm ............................................................. 50
   2.6.5 CMOS 65nm ............................................................. 52
   2.6.6 CMOS 45nm ............................................................. 57
   2.6.7 CMOS 28nm ............................................................. 59
      2.6.7.1 CMOS 28nm GO2 .............................................. 59
      2.6.7.1 CMOS 28nm RVT ............................................. 61
      2.6.7.1 CMOS 28nm SLVT ........................................... 62
      2.6.7.1 CMOS 28nm HPA ............................................. 64
      2.6.7.1 Comparison CMOS 28nm .................................... 66
2.7 Comparison of LFN in CMOS bulk technology nodes .............. 67
2.8 Conclusions ...................................................................................... 72
References ............................................................................................... 74
Chapter 2

Low frequency noise in bulk MOSFETs

2.1 LFN as a characterization tool

First, we address the use of low frequency noise as a diagnostic tool for the quality and reliability characterization of MOSFETs. In particular, the present work is focused on the 1/f low frequency noise (LFN), whereas other types of noise that appeared in the devices such as thermal noise, shot noise or generation-recombination noise are out of the scope of the present thesis.

Today, it is well known that LFN can be used as a characterization tool for the quality and the reliability of the devices [40-43]. It is obvious that the level of noise has a direct impact on the device quality. If the noise level is high, then the normal functionality of the device is degraded. For this reason, investigation of the mechanisms creating carrier fluctuations is of paramount importance for the improvement of the transistor performance. Only when we are able to explain in detail the physical phenomenon behind the LFN, we will be able to further improve the performance of MOSFETs. Of course, low frequency noise has been investigated extensively over the last 50 years, several issues have already been addressed, but there are still open questions that need to be answered.

On the other hand, the LFN can give important information about the reliability of the MOSFET. There is a direct link between the physical phenomenon creating the LFN in devices and the quality of the interface between the gate dielectric stack and the channel. The quality of the interface is related with the number of imperfections, often called traps, which are created during the production of the transistor. These traps are responsible for the lifetime limitations of the device, which is the request of reliability analysis. The question which arises is why the noise is used in the present task for reliability studies, instead of the classical static and dynamic electrical stress methods. Noise measurements are used as a complementary experimental technique to clarify the degradation mechanisms of the device under various bias stress conditions. The noise spectroscopy can give information about the spatial distribution of traps within the gate dielectric. Furthermore, the noise experimental technique is not destructive, in contrast to the techniques based on the device degradation under bias stress conditions. However, the main drawback of the noise spectroscopy as a primary method to analyze the quality of the interface is that noise measurements take a very long time.
Chapter 2: Low frequency noise in bulk MOSFETs

2.2 LFN models

The origin of the 1/f noise in MOS transistors has been debated for several decades. In spite of the extensive efforts to identify the physical origin of the current fluctuations, a universally accepted model for simulating 1/f noise is still lacking. There are two main theories which accept that the origin of 1/f noise originates from fluctuations of the channel conductivity (eq. 2.1):

$$\sigma = q \cdot N \cdot \mu$$  \hspace{1cm} (2.1)

where $\sigma$ is the channel conductivity, $q$ is the elementary electron charge, $N$ is the concentration of mobile charge carriers and $\mu$ is the mobility of the carriers. Based on this assumption, several models were developed: the Carrier Number Fluctuations (CNF), the Hooge Mobility Fluctuations (HMF) and the Carrier Number with Correlated Mobility Fluctuations (CNF/CMF) model. Below we describe briefly the aforementioned models for the 1/f noise.

2.2.1 Carrier Number Fluctuations Model

Following McWhorter theory [44], we describe the carrier number fluctuations model. The basic concept of the CNF model in MOSFETs is the trapping and detrapping of inversion layer electrons or holes (for n- and p- MOS, respectively) into slow oxide traps located nearby the Si-SiO$_2$ interface. What does this really means in terms of noise? It means that when a charge is trapped into a trap in the oxide, the oxide charge is changing and therefore the flat band voltage changes according to the formula [45]:

$$\delta V_{fb} = -\frac{\delta Q_{ox}}{C_{ox}}$$  \hspace{1cm} (2.2)

where $\delta V_{fb}$ is the flat band voltage fluctuation, $\delta Q_{ox}$ is the oxide charge change and $C_{ox}$ is the gate oxide capacitance per unit area. Taking into account the gate charge conservation equation, we have:

$$V_g = V_{fb} + \psi_s - \frac{Q_t + Q_d + Q_{it}}{C_{ox}}$$  \hspace{1cm} (2.3)
where $\psi_s$ is the surface potential, $Q_i$ is the inversion charge, $Q_d$ is the depletion charge and $Q_{it}$ is the fast interface state charge. By differentiating eq. (2.3), the following relationship between the oxide charge and the inversion charge is obtained:

$$
\delta Q_i = \frac{c_i}{c_{ox}+c_d+c_{it}+c_i} = \frac{c_i}{c_{ox}+c_d+c_{it}+c_i} \cdot (C_{ox} \cdot \delta V_{fb}) \quad (2.4)
$$

where $C_i = dQ_i/d\psi_s$, $C_d = dQ_d/d\psi_s$, $C_{it} = dQ_{it}/d\psi_s$ are the inversion, depletion and fast interface capacitances, respectively. Eq. (2.4) simply states that a change in the oxide charge results in a change of the inversion charge through Eq. (2.2).

Let us proceed now to the calculation of the drain current fluctuation valid in the linear region of operation. The drain current fluctuation can be easily derived by differentiating the drain current:

$$
\delta I_d = \frac{dI_d}{dQ_i} \cdot \delta Q_i = \frac{dI_d}{dV_g} \cdot \frac{dV_g}{d\psi_s} \cdot \frac{d\psi_s}{dQ_i} \cdot \delta Q_i . \quad (2.5)
$$

By using equations (2.2), (2.3) and the formula for the transconductance $g_m = dI_d/dV_g$, it is obtained:

$$
\delta I_d = g_m \cdot \delta V_{fb} . \quad (2.6)
$$

Therefore, the drain current spectral density, using Eq. (2.2), is given by:

$$
S\delta I_d = g_m^2 \cdot SV_{fb} = g_m^2 \cdot \frac{SQ_{ox}}{W.Lc_{ox}^2} , \quad (2.7)
$$

where the charge spectral density and the gate oxide capacitance are expressed in units per device area.

At this point, it would be much enlightening to explain the details of Eq. (2.7). From Eq. (2.3) it is clear that $V_{fb}$ and $V_g$ play a symmetric role in the validity of the conservation equation, meaning that any change in $V_{fb}$ can be equivalently translated into a change in $V_g$ such as $SV_g = S_{1b}/g_m^2$,

$$
\delta V_{fb} = -\delta V_g . \quad (2.8)
$$
From Eq. (2.8) is now clear that the so called equivalent input gate voltage spectral density is the flat band voltage spectral density of the MOSFET. The concept of the equivalent input gate voltage spectral density sometimes can be very disturbing and annoying because of the fact that it does not have any physical meaning, but it is more a mathematical notion. The gate voltage cannot fluctuate intrinsically. This term can describe the fluctuations that one has to induce in the gate voltage to create the same noise in drain current.

We can now try to calculate the volumetric trap density, which is the main physical value evaluated from LFN measurements. It is of paramount importance to understand that the spectral density of the oxide charge and eventually of the flat band voltage depends directly from the physical mechanisms of the trapping process.

There are two possibilities for the trapping mechanisms, either by tunneling [46] or thermally activated processes [47]. For a tunneling process, the trapping probability decreases exponentially with oxide depth $x$, such that the flat band voltage spectral density takes the form:

$$
S_{Vfb} = \frac{q^2 kT \lambda N_t}{W_L C^2_{ox} f}
$$

(2.9)

where $kT$ is the thermal energy, $\lambda$ is the tunneling attenuation distance (~0.1nm), $N_t$ is the volumetric trap density (/eV/cm$^3$) and $f$ is the frequency. The time constant characterizing each trap depends exponentially on the trap depth $x$ into the oxide according to the following equation:

$$
\tau(x) = \tau_s \exp\left(\frac{-x}{\lambda}\right)
$$

(2.10)

where $\tau_s$ is a time constant. From Eq. (2.10) we can conclude that the oxide traps which are close to the interface are the most fast and those which are deeper in the gate oxide are the slower ones, attributing to $1/f$ noise.

In the case of a thermally activated process, the trapping probability decreases exponentially with the cross section activation energy $E_a$ and the time constant is given by:

$$
\tau(E_a) = \tau_0 \exp\left(\frac{E_a}{kT}\right)
$$

(2.11)

where $\tau_0$ is a constant. The flat band voltage spectral density is given by:
Chapter 2: Low frequency noise in bulk MOSFETs

\[ SV_{fb} = \frac{q^2k^2T^2N_{it}}{WLC_{ox}^2f\Delta E_a} \]  \hspace{1cm} (2.12)

where \( \Delta E_a \) is the amplitude of the activation energy dispersion and \( N_{it} \) is the oxide trap surface states density (/eV/cm²).

It is noticed that the results for the volumetric trap density given by Eqs. (2.9) and (2.12) are based on the uniformity of the traps near the interface. In fact, the 1/f spectra result from Eqs. (2.10)- (2.11) with uniform distribution of the time constants. If the trap distribution near the interface is not uniform, then the spectra deviate from 1/f to 1/f\(^\gamma\) with \( \gamma \) close to unity. The variations of the \( \gamma \) values versus the gate polarization can give us information about the trap distribution.

### 2.2.2 Hooge Mobility Fluctuations Model

This model has been proposed by Hooge, according to which the 1/f noise is not due to fluctuations arising from surface states [48]. According to Hooge [49], the fluctuations of the drain current arise from fluctuations of the carrier mobility possibly through a fluctuation of the scattering cross section entering the collision probability [50].

The drain current spectral density is given from equation [51]:

\[ \frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWL^2} \int_0^L \frac{dy}{Q_i(y)} \]  \hspace{1cm} (2.13)

where \( \alpha_H \) is the Hooge parameter and \( Q_i(y) \) is the inversion charge per surface. Depending on the region of functionality, the expression of the inversion charge in Eq. (2.13) can vary. In the ohmic region of operation where the channel is uniform, the inversion charge is practically constant and Eq. (2.13) gives:

\[ \frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{fWLQ_i} \cdot \]  \hspace{1cm} (2.14)

Note that in the HMF model, \( S_{Id}/I_d^2 \) should vary as \( 1/Q_i \) so as \( 1/I_d \). In the strong inversion region, the inversion charge reduces to:

\[ Q_i \approx C_{ox} \cdot (V_g - V_{th}) \cdot \]  \hspace{1cm} (2.15)
Thus, from Eq. (2.14), we can conclude that the normalized drain current spectral density is inversely proportional to the gate voltage of the device.

### 2.2.3 Carrier number with Correlated Mobility Fluctuations Model

At present, we have described the two major theories explaining the flicker noise in MOSFETs. The first one was the carrier number fluctuations theory which is based on the charge trapping model of McWhorter and the second one on the empirical model of Hooge which accepts bulk and no surface phenomenon. A unified model, which incorporates both the number fluctuations and the correlated surface mobility fluctuations (CNF/CMF) mechanism, has been developed by Hung [52] and Ghibaudo [53]. The latter is attributed to the Coulomb scattering effect of the fluctuating oxide charge.

This unified model is based on the assumption that the oxide charge can induce not only fluctuations to the number of carriers in the channel but in the mobility of carriers as well, through fluctuations of the scattering rate. The oxide charge fluctuations will give rise to a change in the mobility, thus creating an extra drain current fluctuation according to the equation:

\[
\delta I_d = \delta V_{fb} \cdot \frac{\partial I_d}{\partial V_{fb}} |_{\mu_{eff}=cst} + \delta \mu_{eff} \cdot \frac{\partial I_d}{\partial \mu_{eff}} |_{V_{fb}=cst} \tag{2.16}
\]

Considering the effective mobility based on the Matthiesen rule, it is obtained:

\[
\frac{1}{\mu_{eff}} = \frac{1}{\mu_{eff,0}} + \alpha_{sc} \cdot Q_{ox} \tag{2.17}
\]

where \(\mu_{eff,0}\) is either a constant or a function of the inversion charge, the electric field or the gate voltage, including thus the influence of the diffusion mechanisms on the effective mobility. The term \(\alpha_{sc}Q_{ox}\) is the limiting mobility factor by the oxide charge. The parameter \(\alpha_{sc}\) is the so-called Coulomb scattering coefficient (V.s/C).

In linear region of operation, the drain current is given by:

\[
I_d = \frac{W}{L} \cdot \mu_{eff} \cdot |Q_i| \cdot V_d \tag{2.18}
\]

where \(V_d\) is the drain voltage. Using Eqs. (2.17) and (2.18), it is obtained:

\[
\delta I_d = -g_m \cdot \delta V_{fb} + \alpha_{sc} \cdot \mu_{eff} \cdot I_d \cdot \delta Q_{ox}, \tag{2.19}
\]
where the sign of mobility term is chosen negative for acceptor-like traps or positive for donor-like traps [51]. Now, the normalized spectral drain current density can be derived from (2.19):

\[
\frac{S_{ld}}{I_d^2} = (1 \pm \alpha_{sc} \cdot \mu_{eff} \cdot C_{ox} \cdot \frac{I_d}{g_m} \cdot (\frac{g_m}{I_d})^2 \cdot SV_{fb}
\]  

(2.20)

and for the gate voltage spectral density:

\[
SV_g = (1 \pm \alpha_{sc} \cdot \mu_{eff} \cdot C_{ox} \cdot \frac{I_d}{g_m})^2 \cdot SV_{fb}
\]  

(2.21)

From Eq. (2.20), we can conclude that if the Coulomb scattering coefficient is \(\alpha_{sc}=0\), then the normalized drain current spectral density is reduced to the carrier number fluctuations model described with Eq. (2.7) and from Eq. (2.21) \(SV_g \approx SV_{fb}\). In this case, \(S_{ld}/I_d^2\) is varying as the \((g_m/I_d)^2\) only when \(SV_{fb}\) is independent of the polarization, which implies that the volumetric and energetic distribution of the traps in the gate oxide is uniform. For large values of \(\alpha_{sc}\), the second term in the parenthesis of Eq. (2.20) plays an important role for the normalized drain current spectral density.

At strong inversion, following a first order mobility degradation law of the form [52]:

\[
\mu_{eff} = \frac{\mu_0}{[1 + \theta_1 (V_g - V_{th})]} \cdot
\]  

(2.22)

the drain current and the transconductance are given by:

\[
I_d = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot \frac{(V_g - V_{th})}{[1 + \theta_1 (V_g - V_{th})]} \cdot V_d
\]  

(2.23)

\[
g_m = \frac{W}{L} \cdot C_{ox} \cdot \mu_0 \cdot \frac{1}{[1 + \theta_1 (V_g - V_{th})]^2} \cdot V_d
\]  

(2.24)

From Eq. (2.21), using Eqs. (2.22)- (2.24), it is obtained:

\[
SV_g = SV_{fb} \cdot [1 \pm \alpha_{sc} \cdot \mu_0 \cdot C_{ox} \cdot (V_g - V_{th})]^2
\]  

(2.25)

It is noticed that Eqs. (2.7), (2.20) and (2.21) are valid in the ohmic region of operation. The extension of the CNF/CMF model in the non-ohmic region of operation is described in the
next paragraph, where we have developed a new CNF/CMF compact model valid in all regions of operation.

### 2.3 Development of new LFN compact model for nanoscale bulk MOSFETs

The drain current noise of MOSFET, operating in the non-linear region, can be obtained by integrating the power spectral density of the local sheet conductivity fluctuations along the channel:

\[
\sigma = \mu_{\text{eff}} \cdot Q_i \cdot \cdot \cdot \quad (2.26)
\]

The drain current fluctuation due to variation of the sheet conductivity at a position \((x,y)\) over a small area \(dx.\,dy\) in the channel can be written as [56-58]:

\[
\frac{\delta I_d}{I_d} = \frac{\delta \sigma}{\sigma} \cdot \frac{dx}{W} \cdot \frac{dy}{L} \cdot \quad (2.27)
\]

Then using equations (2.16) and (2.19), we obtain:

\[
\frac{\delta I_d}{I_d} = \left[ \frac{1}{\sigma} \cdot \frac{\partial \sigma}{\partial V_{fb}} + \alpha \cdot \mu_{\text{eff}} \cdot C_{ox} \right] \cdot \delta V_{fb} \cdot \frac{dx}{W} \cdot \frac{dy}{L} \quad (2.28)
\]

from which the normalized drain current noise can be calculated:

\[
\frac{S_{I_d}}{I_d^2} = \int_0^W \int_0^L \left[ \frac{1}{\sigma} \cdot \frac{\partial \sigma}{\partial V_{fb}} + \alpha \cdot \mu_{\text{eff}} \cdot C_{ox} \right]^2 \cdot SV_{fb} \cdot \frac{dx}{W} \cdot \frac{dy}{L} \quad (2.29)
\]

Accounting for current continuity along the channel, we have for the drain current:

\[
I_d = W \cdot \mu_{\text{eff}} \cdot Q_i \cdot \frac{dU_c}{dx} \quad (2.30)
\]

With \(U_c\) being the quasi-Fermi level shift, then from (2.29) we obtain:

\[
\frac{S_{I_d}}{I_d^2} = SV_{fb} \cdot \frac{\int_0^{V_d} \left( \frac{1}{\sigma} \cdot \frac{\partial \sigma}{\partial V_{fb}} + \alpha_{sc} \cdot \mu_{\text{eff}} \cdot C_{ox} \right)^2 \cdot \mu_{\text{eff}} \cdot Q_i \cdot dU_c}{\int_0^{V_d} \mu_{\text{eff}} \cdot Q_i \cdot dU_c} \quad (2.31)
\]

At strong inversion, the correlated mobility factor is dominant, i.e.:
Chapter 2: Low frequency noise in bulk MOSFETs

\[
\frac{1}{\sigma} \cdot \frac{\partial \sigma}{\partial V_{fb}} \ll \alpha_{sc} \cdot \mu_{eff} \cdot C_{ox} \quad (2.32)
\]

and Eq. (2.31) is written as:

\[
\frac{S_{Id}}{I_d^2} \approx \frac{S_{V_{fb}}}{2 \cdot \mu_{eff} \cdot Q_i \cdot dU_c} \cdot (\alpha_{sc} \cdot \mu_{eff} \cdot C_{ox})^2 \quad (2.33)
\]

Assuming that the product \( \alpha_{sc} \cdot \mu_{eff} \) is constant, Eq. (2.23) yields for the gate voltage noise spectral density \( S_{V_g} \) in the strong inversion limit:

\[
S_{V_g} \approx (\alpha_{sc} \cdot \mu_{eff} \cdot C_{ox} \cdot \frac{I_d}{g_m})^2 \cdot S_{V_{fb}} \quad (2.34)
\]

As a result, equation (2.21) can be recovered from Eq. (2.34) after adding the weak inversion offset \( S_{V_{fb}} \), justifying by turn its physical origin.

The above theoretical analysis clearly demonstrates that, for all operation regions, a generic MOSFET compact CNF/CMF low frequency model can be constructed based on the single equation:

\[
\sqrt{S_{V_g}} = \sqrt{S_{V_{fb}}} \cdot (1 + \Omega \cdot \frac{I_d}{g_m}) \quad (2.35)
\]

with two physical parameters, namely \( \sqrt{S_{V_{fb}}} \) related to the oxide trap density using Eq. (2.9) and \( \Omega = \alpha_{sc} \cdot \mu_{eff} \cdot C_{ox} \) related to the effective Coulomb scattering coefficient \( \alpha_{sc} \), the effective mobility \( \mu_{eff} \) and the gate oxide capacitance \( C_{ox} \). Both parameters can be extracted experimentally from a plot of \( \sqrt{S_{V_g}} \) versus \( I_d/g_m \) in linear and/or non-linear operation regions. The knowledge of these two parameters for a given CMOS technology provides a full description of the input gate voltage noise versus gate and drain voltages, and by turn of the drain current 1/f noise \( S_{Id} \) for any bias conditions.

It is worth noting that to obtain a constant value for the product \( \alpha_{sc} \cdot \mu_{eff} \) as a function of gate voltage, it clearly means that: (i) the conventional assumption of a constant \( \alpha_{sc} \) in the CNF/CMF model is not adequate, since in that case \( \alpha_{sc} \cdot \mu_{eff} \) should decrease at strong inversion because \( \mu_{eff} \) degrades due to surface roughness scattering, and (ii) the reduction of the Coulomb scattering coefficient \( \alpha_{sc} \) at strong inversion due to screening [59-60] would also not be consistent with a constant \( \alpha_{sc} \cdot \mu_{eff} \) product. This is in physical agreement with the
experimental findings of the pioneering work by Sun and Plummer [61] reporting a Coulomb scattering law of the form:

\[
\mu_{\text{eff}} = \frac{\mu_{\text{eff},0}}{1 + \alpha_{\text{sc}} \mu_{\text{eff}} Q_i}.
\] (2.36)

In contrast, the conventional Coulomb scattering law formulated using Matthiesen’s rule (i.e. Eq. 2.17), would result in a non constant \(\alpha_{\text{sc}} \mu_{\text{eff}}\) product.

### 2.4 Noise measurement setup

We would like at this subparagraph to clarify some issues about the noise measurements which we think that are still not clear. First, there are two schools of thoughts concerning the physical value, voltage or current, used to analyze the low frequency noise mechanisms in MOSFETs. In this work, we measure the drain current fluctuations of the device. The reason is because we can use a programmable current amplifier in order to magnify the noise signal and thus we are more confident about the measurements and we are able to make automatic measurements.

The noise measurements in MOSFETs is a complex task. The reason is simple and nowadays well known in the scientific community: the signal to be measured is very weak. Thus, the noise system should be very well shielded to avoid any environmental and internal disturbances affecting the measurement. With the term internal fluctuations, we define all the disturbances induced to the signal from the measuring equipment. The protection from environmental disturbances includes the proper shielding of the whole equipment from electromagnetic radiation. This can be accomplished using a Faraday cage. The internal disturbances that can “pollute” the measurement are a much more complicated task to do. This issue is addressed below where we describe analytically the measurement system.

The electronic and software used in this system has been developed to comply with the basic requirements that an automatic LFN measuring system should meet. The system features a low-noise point probe wafer level contacting, shows no computer generated noise and provides a programmable data acquisition and storage. Fig. 2.1 presents a schematic diagram of the noise system [62-63].
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.1: A schematic diagram of the programmable biasing amplifier used as a current amplifier for the drain current and for biasing the gate of a MOSFET.

This system is constituted from a double-input programmable biasing amplifier, PBA. Both inputs of the PBA can be remotely biased and the current flowing through Input 1 is measured with the software controlled DC-gain selection, assuring the optimal device noise signal/system noise ratio. Input 2 provides $V_g$ with no current measured option. Both inputs are triaxial with guard for the probes outer shells. All the functions of the PBA are computer-controlled including the function of the spectrum analyzer. Thus, the user can define the specific parameters of the measurements, such as gate and drain biases, measurement frequency bandwidth and all the specific data for the spectrum analyzer to perform the FFT delivering the measured spectra.

LFN measurements were performed using a PBA I/V converter for drain current fluctuation amplification and an HP 89410A FFT analyzer to compute the power spectral density (PSD). Drain current noise measurements were carried out in linear and non-linear regions of operation. The drain voltage $V_d$ was fixed to 50 mV for measurements in linear region and the gate voltage varied from weak to strong inversion. In the non-linear region, the gate voltage was fixed below and above threshold and the drain voltage was varied from linear to saturation regime. Added system noise from LNA was subtracted from measured spectrum with software. The experimental frequency bandwidth is 10Hz–100 kHz.

The method of our analysis includes the following steps: First we treat the data with software applying two filters. The first one on drain current: 1) Mean (m) and standard deviation ($\sigma$) of the whole distribution of $I_d$ are calculated. 2) Values of $I_d$ outside the $m \pm 3\sigma$ interval are rejected and consequently all the corresponding spectrum. 3) Mean (m) and standard deviation ($\sigma$) of the new distribution are calculated. 4) Iterative filter is applied down
to no other value is rejected. The second is applied on $S_{ld}$ (Power Spectral density): 1) Log ($S_{ld}$) is calculated. 2) For each frequency, mean ($m$) and standard deviation ($\sigma$) of the whole distribution of Log ($S_{ld}$) are calculated. 3) Values of Log ($S_{ld}$) outside the $m$$\pm$$3\sigma$ interval are rejected. 4) Mean ($m$) and standard deviation ($\sigma$) of the new distribution of Log ($S_{ld}$) are calculated. 5) Iterative filter is applied down to no other value is rejected.

After the statistical analysis of the data, the $1/f$ noise behavior for each measured die is identified. Then the median value of the distribution is calculated and again is tested for $1/f$ spectrum form. Finally, the drain current power spectral density for each polarization is calculated taking the median value of the product $f$$\times$$S_{ld}$ at a frequency in the range of 10-30 Hz. This value is used to analyze low frequency noise in this work.

The next step of the LFN analysis is to identify the noise model that best fits to the experimental data. In order to identify the model which is applicable to our data, we plot in log-log scale the normalized drain current noise versus drain current and we check the validity of the CNF, HMF and CNF/CMF models. The HMF model has been verified by plotting the drain current noise versus the square of drain current according eq. (2.14). The analysis is divided into to two parts, linear and non-linear regions.

2.5 Experimental verification of the LFN compact model

The proposed new LFN compact model is verified by comparison with experimental results. Electrical measurements were performed on n- and p-MOS transistors issued from 28nm bulk CMOS technology. The gate stack consists of TiN as metallization and Hf-based dielectric as gate oxide, with an equivalent oxide thickness (EOT) 1.4 and 1.7 nm for the n- and p-MOS transistors, respectively. For n-MOS transistors, there is a layer of La between the metal and the gate oxide and an interfacial layer between the oxide and the gate channel. For p-MOS transistors, there is another layer of Al that does not exist in the gate stack of n-MOS. In addition, the channel between the two types of transistors is not the same, for n-MOS devices the channel is purely Si but for p-MOS is SiGe in order to boost the mobility and reduce the threshold voltage. The channel length ($L$) is lying in the range of 0.03 – 1.803 $\mu$m and the channel width ($W$) is 0.9 $\mu$m. Static characterization was performed in order to obtain the transfer ($I_{d}$$-$$V_{g}$) and output ($I_{d}$$-$$V_{d}$) characteristics and then extract the needed parameters. LFN measurements were performed using the noise system described in paragraph 2.4. The drain voltage was fixed to $V_{d}$$=\pm$50mV for measurements in linear region of operation and the gate voltage varied from weak to strong inversion. In the non-linear region, the gate voltage
was fixed below and above threshold and the drain voltage varied from linear to saturation. For each device geometry, a minimum of 10 dies were measured, and the median value for each polarization was obtained and analyzed. Results for typical device geometry are presented in Fig. 2.2.

Fig. 2.2: Drain current noise power spectral density versus frequency for n-MOS with channel length of 0.453μm and width 0.9μm for $V_g=0.7\,V$ and $V_d=50\,mV$. 10 dies were measured represented by grey lines and the median spectrum is calculated shown by red line. Both the measured and the median spectra are 1/f-like, blue line on the graph.

2.5.1. Linear region

First, we verified that the type of LFN appeared in the measured devices is 1/f-like. Figure 2.3 shows the medium spectrum of 10 dies from n- (A, B) and p- (C, D) MOS devices of various areas, measured in the linear region of operation for various gate voltages. It is clearly seen that the spectra show 1/f behavior with $\gamma$ close to unity for both types of devices and all bias conditions. The spikes appeared at the frequency of 50 Hz and its harmonics are caused by the power line.

In Fig. 2.4 (A) and (B), we plot the $\gamma$ factor for all the measured devices, n- and p- MOS transistors in linear region of operation respectively. It can be seen from the figure that the $\gamma$ factor is almost constant for all the measured geometries and bias conditions and very close to unity. Thus, we have taken it equal to unity in order to calculate the volumetric trap density for all the geometries as already noted in subparagraph (2.2.1).

In Fig. 2.5, we plot the normalized drain current noise spectral density at 1 Hz versus drain current $I_d$ for the above n- and p-MOS devices. It is seen from the plot that the CNF/CMF model expressed from eq. (2.20) can explain adequately the noise results. Similar results were obtained for all the measured areas. Using eq. (2.9), we can calculate the volumetric trap
density $N_t$. Typical values of $N_t$ are presented in Fig. 2.6 for both n- and p-channel MOSFETs with different channel lengths. The values of $N_t$ in the p-channel devices are slightly higher compared to the n-channel devices, probably because of the different channel type (SiGe) and gate stack used to formulate p-channel devices. Note also that $N_t$ is almost constant for all measured devices indicating a uniform distribution of traps in the gate interface and allowing us to select whatever geometry we want to characterize the technology.

![Figure 2.3: Drain current noise power spectral density versus frequency in linear region of operation for n-MOS with width 0.9μm and channel length of 0.03 and 1.803μm respectively (A)-(B) and p-MOS with width 0.9μm channel length of 0.453 and 0.156μm respectively (C)-(D).](image)

![Figure 2.4: $\gamma$ factor versus gate voltage for n- and p- MOS (A) and (B) respectively for all the measured geometries in linear region of operation, $V_d = \pm 50$ mV.](image)
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.5: Normalized drain current noise power spectral density versus drain current at \( f = 1 \text{Hz} \) in linear region of operation for n-MOS [1] with width 0.9 \( \mu \text{m} \) and channel length of 0.03 \( \mu \text{m} \), black points, and 1.803 \( \mu \text{m} \), green points, and p-MOS [2] with channel length of 0.156 \( \mu \text{m} \), black points, and 0.453 \( \mu \text{m} \), green points, respectively. The red straight line is the CNF/CMF model and the blue straight line the CNF model.

Fig. 2.6: Volumetric trap density as a function of the gate length and constant width of 0.9\( \mu \text{m} \) for n-MOS (red points) and p-MOS (black points).

For the CNF/CMF model, the gate voltage noise spectral density is given by eq. (2.21). According to this relationship, the plot of \( \sqrt{S_{gV}} \) versus \( I_d/g_m \) is expected to be linear. In fact, this is verified for long and short channel p- and n-channel MOSFETs as shown in Fig. 2.7. For all channel lengths measured, a linear relationship between \( \sqrt{S_{gV}} \) and \( I_d/g_m \) is observed, indicating clearly that the product of the Coulomb scattering coefficient and the effective carrier mobility \( \alpha_{sc}\mu_{\text{eff}} \) is constant in the drain current range from weak to strong inversion, i.e. \( \alpha_{sc} \) cannot be considered as constant since \( \mu_{\text{eff}} \) is gate voltage dependent but not
exclusively due to surface roughness scattering. The above analysis is extended in the non-linear region verifying the validity of our new compact model.

![Graphs](image)

Fig. 2.7: Variation of $\sqrt{S_{V_g}}$ as a function of $I_d/g_m$ for n-channel MOSFETs (1, 2) and p-channel MOSFETs (3, 4), measured at $V_d = \pm 50$ mV and $f = 1$ Hz.

### 2.5.2. Non-linear region:

First, we verified the findings of gamma $\gamma$ values close to unity in linear region of operation and in the non linear too. In Fig. 2.8, we plot the gamma factor versus drain voltage for n- and p-MOS device with W/L=0.9/0.473μm. Is is clearly seen from Fig. 2.8 that the gamma factor has values very close to one in this region of operation. These findings were found in all the measured geometries n- and p-MOS transistors.

The investigation for the dependence of $\sqrt{S_{V_g}}$ on $I_d/g_m$ was extended in all regions of the transistor operation. This is demonstrated in Figs. 2.9 and 2.10 for n-channel and p-channel MOSFETs, respectively and with different channel lengths. In these figures, families of data points were obtained for different constant values of $V_g$ (below and above threshold) and various drain voltages (from linear to saturation region). Similarly to the linear region, it is clearly shown that all the data points lie on straight lines, demonstrating that the functional dependence of Eq. (2.21) versus $I_d/g_m$ also applies to the non-linear region when varying $V_d$. 
Chapter 2: Low frequency noise in bulk MOSFETs

Therefore, eq. (2.21) can be used to fit the data of Figures 2.9 and 2.10, providing two parameters, namely $\sqrt{S_{Vfb}}$ from the y-axis intercept and $\alpha_{\mu} \mu_{\text{eff}} C_{\text{ox}} \sqrt{S_{Vfb}}$ from the slope, respectively.

Fig. 2.8: $\gamma$ factor versus drain voltage for n- and p- MOS (A) and (B) respectively with W/L=0.9/0.473\(\mu\)m in linear region of operation for different gate voltages from the ohmic to saturation.

![Fig. 2.8](image)

Fig. 2.9: Variations of $\sqrt{S_{V/g}}$ as a function of $I_d/g_m$ for n-channel MOSFETs with W = 0.9 \(\mu\)m and different channel lengths measured at f = 1Hz and various drain voltages from linear to saturation region (0 - 1V) and gate voltages $V_g$ below and above threshold.

![Fig. 2.9](image)
Fig. 2.10: Variations of $\sqrt{S_{V/g}}$ as a function of $I_d/g_m$ for p-channel MOSFETs with $W = 0.9 \mu m$ and different channel lengths measured at $f = 1Hz$ and various drain voltages from linear to saturation region (0 - 1V) and gate voltages $V_g$ below and above threshold.

Fig. 2.11 shows the gate length dependence of the parameters $\sqrt{S_{V/g}}$ and $\alpha_{sc} \mu_{eff} C_{as} \sqrt{S_{V/g}}$ for n- and p- type devices extracted applying Equation (2.35) to data in the linear and non-linear regions of operation. Note that despite they have been extracted from different operation regions they take similar values, indicating that Equation (2.35) provides a consistent physical picture of the noise data both in linear and non-linear regions. The parameter $\alpha_{sc} \mu_{eff} C_{as} \sqrt{S_{V/g}}$ is found almost constant with gate length and close to $10^{-4}V/\sqrt{Hz}$ for n- and p-type devices.

In order to verify further the validity of our model, we present in Figure 2.12 typical variations of $\sqrt{S_{V/g}}$ versus $I_d/g_m$ obtained from Equation (2.31) when varying $V_d$ from 0 to 1V and for different gate voltages, while assuming a constant $\alpha_{sc} \mu_{eff} (=2\times10^6 \text{ cm}^2/\text{C})$ and $\sqrt{S_{V/g}} = 1.2\times10^5 \text{ V}/\sqrt{Hz}$. Note the very good linearity of the simulated data points, inferring the behavior of the experimental results of Figure 2.7. The solid line in Figure 2.11 shows the straight line obtained using Equation (2.21) with the same parameters, demonstrating therefore, the validity of Equation (2.21) from a modeling viewpoint.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.11: Variations of $\alpha_{sc} \mu_{eff} C_{ox} \sqrt{S_{Vfb}}$ and $\sqrt{S_{Vfb}}$ with gate length for n-channel (1, 2) and p-channel (3, 4) devices.

Fig. 2.12: Typical variations of $\frac{S_{V}}{I_d/g_m}$ as a function of $I_d/g_m$ obtained from Equation (2.31) (symbols) when varying $V_d$ from 0 to 1 V and for various gate voltages ($V_g = 0.55, 0.7, 1.2$ V) for a transistor with $L = 1.8 \, \mu m$, measured at $f = 1$Hz. The solid line shows the straight line given from Equation (2.21) with parameters $\alpha_{sc} \mu_{eff} (=2\times10^6 \, cm^2/V)$ and $\sqrt{S_{Vfb}} = 1.2\times10^{-5} \, V/\sqrt{Hz}$. 
2.5.3 Generic CMF LF noise compact model

The above experimental and theoretical analysis clearly demonstrate that, for all operation regions (see Figures 2.7, 2.8, 2.9) a generic MOSFET compact CNF/CMF LF noise model can be constructed based on a single equation:

\[
\sqrt{SV_g} = \sqrt{SV_{fb}} \cdot (1 + \Omega \frac{I_d}{g_m}) \tag{2.37}
\]

with two physical parameters, namely \( \Omega = \alpha_{sc} \mu_{eff} C_{ox} \) related to the effective Coulomb scattering coefficient \( \alpha_{sc} \mu_{eff} \) and gate oxide capacitance and \( \sqrt{S_{yp}} \) related to the oxide trap density. Both parameters can be extracted experimentally from a plot of \( \sqrt{SV_g} \) versus \( I_d / g_m \) in linear and/or non-linear operation regions. The knowledge of these two parameters for a given CMOS technology provides a full description of the input gate voltage noise versus gate and drain voltages, and by turn of the drain current 1/f noise \( S_{Id} \) for any bias conditions. Therefore, Equation (2.37) gives an accurate and continuous description of the 1/f noise in MOSFETs for all operation regions in a single-piece formulation.

2.6 Experimental LFN measurements in bulk n- and p-MOSFETs of different technology nodes

Detailed investigation of the LFN was performed on different types of bulk n- and p-MOS transistors and from seven technology nodes of STMicroelectronics. Table 2.1 summarizes the type of the gate metal, the type of the gate dielectric and the oxide thickness. In type of devices GO1, the gate stack is polysilicon with SiO\(_2\)/SiON for gate oxide, with thickness varying from 12 to 1.4 nm in the technology nodes from 0.25 \( \mu \text{m} \) to 45 nm. In the 28 nm technology node, high-\( \kappa \)/metal gate stack with TiN for metallization and Hf-based dielectric as gate oxide was introduced and the equivalent oxide thickness is 1.4/1.7 nm for n- and p-MOS devices, respectively. In the type of devices GO2, the devices are characterized according to the \( V_{dd} \) used. We measured devices with different dimensions (W, L) from both types.

It is important at this point to clarify the reason why we have done an extensive analysis of almost all the CMOS technology nodes from STMicroelectronics. The overall behavior from seven technology nodes of the volumetric trap density and the normalized drain current noise has never been done in a single work. In literature, there were many works about transistors from different technology nodes and their noise behavior, but a complete comparison of these
parameters from seven technology nodes from the same foundry was never made. In addition, a thoroughly investigation of the 28nm technology node had carried out since it was one of the goals of this thesis. For this reason we tested several different devices of the 28nm CMOS technology node that were different in not only the gate stack, n- and p-MOS, but also in the channel architecture, transistors with different type of channel, threshold voltage and oxide thickness. We would like at this point to underline that we will present results concerning the minimum gate length of each technology node but these apply to other geometries as well.

Table 2.1 Description of the gate stack for different CMOS technology nodes

<table>
<thead>
<tr>
<th>Technology</th>
<th>Node</th>
<th>GO1</th>
<th>GO2_1.8V</th>
<th>GO2_3.3V</th>
<th>Gate</th>
<th>Oxyde</th>
</tr>
</thead>
<tbody>
<tr>
<td>H7A</td>
<td>0.25μm</td>
<td>120</td>
<td></td>
<td></td>
<td>Poly</td>
<td>SiO₂</td>
</tr>
<tr>
<td>H8S</td>
<td>0.18μm</td>
<td>32</td>
<td></td>
<td>70</td>
<td>Poly</td>
<td>SiO₂</td>
</tr>
<tr>
<td>H9A</td>
<td>0.12μm</td>
<td>23</td>
<td></td>
<td>85</td>
<td>Poly</td>
<td>SiON</td>
</tr>
<tr>
<td>C090</td>
<td>90nm</td>
<td>21</td>
<td></td>
<td>65</td>
<td>Poly</td>
<td>SiON</td>
</tr>
<tr>
<td>M55</td>
<td>65nm</td>
<td>18</td>
<td></td>
<td>65</td>
<td>Poly</td>
<td>SiON</td>
</tr>
<tr>
<td>C040</td>
<td>45nm</td>
<td>17</td>
<td>14/17</td>
<td>34</td>
<td>Metal</td>
<td>SiON</td>
</tr>
<tr>
<td>C028</td>
<td>28nm</td>
<td>14/17</td>
<td></td>
<td></td>
<td>Metal</td>
<td>High-K</td>
</tr>
</tbody>
</table>

2.6.1 CMOS 0.25μm

The main process issues of this technology node are the replacement of PBL with STI for isolation structure and oxide + nitride spacers. The gate stack for both n- and p-MOS devices is polysilicon with SiO₂ for gate oxide. The oxide thickness for both devices is 120Å and V_{dd} is 5V.

The drain current noise spectral density versus frequency for p-MOS and n-MOS with W/L=10/0.45μm and various gate voltages are shown in Figs. 2.13 (A) and (B), respectively in the linear region of operation. As can be seen, the spectra show 1/f behavior for both n- and p-MOS devices, which is the first step of the LFN analysis. In Fig. 2.14 are shown the normalized drain current noise versus drain current for the devices of Fig. 2.13. As can be seen from the figures, the CNF/CMF model better explains the experimental results (data point on the figures) for both n- and p-MOS devices. The same behaviour was observed on all the measured geometries and for both types of transistors, n- and p-MOS. The validity of the CNF/CMF model is further verified by plotting \( \sqrt{S_{V_s}} \) as a function of \( I_d/g_m \) in Figs. 2.15(A) and (B) for n-MOS [A] and p-MOS [B], respectively. Note that the variation of \( \sqrt{S_{V_s}} \) with \( I_d/g_m \) follows equation (2.35).
Fig. 2.13: Drain current power spectral density versus frequency for n-MOS [A] and p-MOS [B] devices from the 0.25μm technology node with channel width W=10μm and channel length L=0.45μm, various gate polarization in linear region of operation V_d=±100mV, respectively. The red straight line is the 1/f-like spectrum.

Fig. 2.14: Normalized drain current noise spectral density versus drain current for n-MOS [A] and p-MOS [B] devices in linear region of operation V_d=±100mV at f=1Hz, respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.15: Square root of gate noise voltage spectral density $\sqrt{S_{V_g}}$ versus $I_d/g_m$ at f=1Hz for n-MOS [A] and p-MOS [B] in linear region of operation V_d=±100mV, respectively.
2.6.2 CMOS 0.18μm

The main process issues of this technology node are the introduction of double gate oxide transistors (GO1 and GO2), pocket implants and CoSi2 for salicidation. The gate stack for both n- and p-MOS devices is polysilicon with SiO2 for gate oxide. The oxide thickness for GO1 and GO2 is 32 and 70Å, respectively. Vdd for GO1 and GO2 is 1.8 V and 3.3 V, respectively.

In Fig. 2.16, we plot the drain current noise spectral density versus frequency for n-MOS, GO1&GO2 [A-B] and p-MOS, GO1&GO2 [C-D] devices with (W/L)_{GO1}=10/0.18μm and (W/L)_{GO2}=10/0.34μm, for various gate voltages, in the linear region of operation V_{d,GO1}=±50mV and V_{d,GO2}=±100mV. It can be seen that all spectra show 1/f behavior.

![Fig. 2.16: Drain current power spectral density versus frequency for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D], from 0.18μm technology node with (W/L)_{GO1}=10/0.18μm and (W/L)_{GO2}=10/0.34μm, various gate voltages and in linear region of operation V_{d,GO1}=±50mV and V_{d,GO2}=±100mV. The red straight lines are the 1/f-like spectra.](image)

In Fig. 2.17, we plot the normalized drain current noise spectral density versus drain current of the above devices. As can be seen the CNF/CMF model can better explain the experimental results for both GO1 and GO2 p-MOS devices. In contrast, the noise in n-MOS...
devices is better explained with the CNF model, as shown in Fig. 2.18, where the plots of \( \sqrt{S_{V_g}} \) versus \( I_d/g_m \) are plotted for n-MOS [A] and p-MOS [B], respectively. Figure 2.18(A) shows that in n-MOS devices the plot of \( \sqrt{S_{V_g}} \) versus \( I_d/g_m \) is not linear, indicating that the LFN can be better interpreted with the CNF model. For p-MOS devices, the linearity of \( \sqrt{S_{V_g}} \) as a function of \( I_d/g_m \) is more clearly seen.

Fig. 2.17: Normalized drain current noise spectral density versus drain current at \( f=1\text{Hz} \) for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D] devices respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.18: Square root of gate noise voltage spectral density \( \sqrt{S_{V_g}} \) versus \( I_d/g_m \) at \( f=1\text{Hz} \) for n-MOS GO1&GO2 [A] and p-MOS GO1&GO2 [B] with \((W/L)_{GO1}=10/0.18\mu\text{m}\) and \((W/L)_{GO2}=10/0.34\mu\text{m}\), respectively.
2.6.3 CMOS 0.12μm

The main process issues of this technology node are the poly pre-doping, the SiON for gate dielectric with Rapid Thermal annealing process (RTN) and spike anneal for junction activation. The gate stack for both n-MOS and p-MOS devices is polysilicon with SiON for gate oxide. The oxide thickness for GO1 and GO2 is 23 and 85Å, respectively. V_dd for GO1 and GO2 is 1.2 and 3.3V, respectively.

In Fig. 2.19, we plot the drain current noise versus frequency for n-MOS GO1 [A] and GO2 [B], p-MOS GO1 [C] and GO2 [D] devices with (W/L)_{GO1}=10/0.13μm and (W/L)_{GO2}=10/0.35μm. The LFN spectra for all gate bias voltages are 1/f-like. In Fig. 2.20, we plot the normalized drain current noise spectral density versus drain current for the same devices. It is clearly seen that the CNF/CMF model can better explain the experimental results for p-MOS both GO1 and GO2 and for n-MOS GO1 devices. On the contrary, the n-MOS GO2 device is better explained with the CNF model as shown in Fig. 2.21 by plotting $\sqrt{S/V_g}$ as a function of $I_d/g_m$. Fig. 2.21 shows that in the n-MOS GO2 device the plot of $\sqrt{S/V_g}$ versus $I_d/g_m$ is not linear, indicating that the LFN can be better interpreted with the CNF model.

![Figure 2.19: Drain current power spectral density versus frequency for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D] devices, from 0.12μm technology node with channel width 10 μm and channel length 0.13 and 0.35μm respectively, various gate polarization in linear region of operation $V_{dd,GO1}=\pm 50$mV and $V_{dd,GO2}=\pm 100$mV. The red straight line is the 1/f -like spectrum.](image)
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.20: Normalized drain current noise versus drain current at f=1Hz for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D] devices respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.21: Square root of gate noise voltage spectral density $\sqrt{S_V}$ versus $I_d/g_m$ at f=1Hz for n-MOS GO1&GO2 [A] and p-MOS GO1&GO2 [B] with (W/L)_GO1=10/0.13μm and (W/L)_GO2=10/0.35μm, respectively.

2.6.4 CMOS 90nm

The main process issues of this technology node are the offset spacers for p-MOS lateral control and double source-drain engineering to reduce tunneling mechanisms. The gate stack for both n- and p-MOS devices is polysilicon with SiON for gate oxide. The oxide thickness
for GO1 and GO2 is 21 and 65 Å, respectively. $V_{dd}$ for GO1 and GO2 is 1.2 and 3.3 V respectively.

In Fig. 2.22, we plot the drain current noise power spectral density versus frequency for n-MOS GO1 [A] and GO2 [B], p-MOS GO1 [C] and GO2 [D] devices with $(W/L)_{GO1}=10/0.1 \mu m$ and $(W/L)_{GO2}=1/1.2 \mu m$. The LFN spectra for all gate bias voltages are 1/f-like. In Fig. 2.23, we plot the normalized drain current noise power spectral density versus drain current for the same devices. The CNF/CMF model can better explain the experimental results for both n-MOS and p-MOS GO1 and GO2 devices. It is clearly seen from Fig. 2.24 that the n-MOS and p-MOS devices show linear behavior of $\sqrt{S_{V_{g}}}$ as a function of $I_{d}/g_{m}$ verifying our previous statement.

![Fig. 2.22: Drain current power spectral density power spectral density versus frequency for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D] devices, from 90nm technology node with (W/L)$_{GO1}=10/0.1 \mu m$ and (W/L)$_{GO2}=1/1.2 \mu m$, and various gate polarization in linear region of operation $V_{d,GO1}=\pm 50 \text{mV}$ and $V_{d,GO2}=\pm 100 \text{mV}$. The red straight line is the 1/f spectrum.](image-url)
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.23: Normalized drain current noise power spectral density versus drain current at f=1Hz for n- MOS GO1&GO2 [A-B] and p- MOS GO1&GO2 [C-D] devices respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.24: Square root of gate noise voltage spectral density $\sqrt{S_{V_g}}$ versus $I_d/g_m$ at f=1Hz for n-MOS GO1&GO2 [A] and p-MOS GO1&GO2 [B] with $(W/L)_{GO1}=10/0.1\mu m$ and $(W/L)_{GO2}=1/1.2\mu m$, respectively.

2.6.5 CMOS 65nm

The main process issues of this technology node are the rotated substrate, 1st generation of stress, NiSi for silicided material and plasma nitridation. The gate stack for both n- and p-MOS devices is polysilicon with SiON for gate oxide. In this particular technology, we have
measured a third device named HV from the initiative of high voltage. The oxide thickness for GO1, GO2 and HV is 18, 65 and 150Å, respectively. $V_{dd}$ for GO1, GO2 and HV is 1.2, 3.3 and 5V, respectively.

In Figures 2.25-2.26, we plot the drain current noise power spectral density versus frequency for n-MOS and p-MOS GO1, GO2 & HV[A,B,C] respectively, with $(W/L)_{GO1}=10/0.06\mu m,(W/L)_{GO2}=0.6/0.38\mu m$ and $(W/L)_{HV}=9/0.9\mu m$. As can be seen, the LFN spectra for all gate bias voltages are 1/f-like.

![Fig. 2.25: Drain current power spectral density versus frequency for n-MOS GO1, GO2 & HV[A,B,C] from 65nm technology node with $(W/L)_{GO1}=10/0.06\mu m$, $(W/L)_{GO2}=0.6/0.38\mu m$ and $(W/L)_{HV}=9/0.9\mu m$, and various gate polarization in linear region of operation $V_{d,GO1}=50mV$ and $V_{d,GO2-HV}=100mV$. The red straight line is the 1/f spectrum.](image-url)
Fig. 2.26: Drain current power spectral density versus frequency for p-MOS GO1, GO2 & HV [A,B,C] from 65nm technology node with (W/L)\(_{GO1}=10/0.06\, \mu m\), (W/L)\(_{GO2}=0.6/0.38\, \mu m\) and (W/L)\(_{HV}=9/0.9\, \mu m\), and various gate polarization in linear region of operation \(V_{d,GO1}=-50\, mV\) and \(V_{d,GO2-HV}=-100\, mV\). The red straight line is the 1/f spectrum.

In Figures 2.27 and 2.28, we plot the normalized drain current noise power spectral density versus drain current for the n-MOS and p-MOS devices, respectively. Figure 2.27 shows that both CNF and CNF/CMF models explain the experimental data of n-MOS devices and, therefore, we have to check the linearity between \(\sqrt{S_{Vg}}\) and \(I_d/g_m\) to conclude which model is valid.

From Fig. 2.29 we can clearly see that there is no linearity between \(\sqrt{S_{Vg}}\) and \(I_d/g_m\) in the n-MOS devices GO1, GO2 & HV. Therefore, the CNF model better explains the experimental results. From Figs. 2.28-2.30, we can conclude that for p-MOS devices the CNF/CMF model can explain the experimental results.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.27: Normalized drain current noise power spectral density versus drain current at f=1Hz for n- MOS GO1, GO2 & HV [A,B,C]. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.28: Normalized drain current noise power spectral density versus drain current at f=1Hz for p- MOS GO1, GO2 & HV [A,B,C]. The black straight line is the CNF model and the dotted line the CNF/CMF.
Fig. 2.29: Square root of gate noise voltage spectral density \( \sqrt{S_{Vg}} \) versus \( I_d/g_m \) at \( f=1\text{Hz} \) for n-MOS GO1, GO2 & HV [A,B,C] with \((W/L)_{GO1}=10/0.06\mu\text{m}, \ (W/L)_{GO2}=0.6/0.38\mu\text{m} \) and \((W/L)_{HV}=9/0.9\mu\text{m}, \) respectively.

Fig. 2.30: Square root of gate noise voltage spectral density \( \sqrt{S_{Vg}} \) versus \( I_d/g_m \) at \( f=1\text{Hz} \) for p-MOS GO1, GO2 & HV [A,B,C] with \((W/L)_{GO1}=10/0.06\mu\text{m}, \ (W/L)_{GO2}=0.6/0.38\mu\text{m} \) and \((W/L)_{HV}=9/0.9\mu\text{m}, \) respectively.
Chapter 2: Low frequency noise in bulk MOSFETs

2.6.6 CMOS 45nm

The main process issues of this technology node are the SACVD less compressive material for STI fill, stress memory technique to boost n-MOS carrier mobility, laser annealing for SD, poly gate dopants activation enhancement, ultra-high tensile thanks to multi-step UV cure solution and 2nd generation of stress. The gate stack for both n-MOS and p-MOS devices is polysilicon with SiON for gate oxide. The oxide thickness for GO1 and GO2 is 17 and 32Å, respectively. \( V_{dd} \) for GO1 and GO2 is 1.1 and 1.8V, respectively.

In Fig. 2.31, we plot the drain current noise power spectral density versus frequency for n-MOS GO1 [A] and GO2 [B], p-MOS GO1 [C] and GO2 [D] devices with \((W/L)_{GO1}=9/0.04\mu m\) and \((W/L)_{GO2}=9/0.634\mu m\). As can be seen, the LFN spectra for all gate bias voltages are \(1/f\)-like.

In Fig. 2.32, we plot the normalized drain current noise power spectral density versus drain current for the same devices. As can be seen, the CNF/CMF model can better explain the experimental results for both n-MOS and p-MOS GO2 devices. Figure 2.33 shows that in the n-MOS and p-MOS GO2 devices the plots of \( \sqrt{SV_g} \) versus \( I_d/g_m \) show linear behavior, indicating that the LFN data can be better interpreted with the CNF/CMF model. On the contrary, the noise data in GO1 devices can be better explained with the CNF model. The plot of \( \sqrt{SV_g} \) versus \( I_d/g_m \) is not linear, indicating that the CMF component is negligible.

Fig. 2.31: Drain current power spectral density versus frequency for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D] devices, from 45nm technology node with \((W/L)_{GO1}=9/0.04\mu m\) and \((W/L)_{GO2}=9/0.634\mu m\), and various gate polarization in linear region of operation \( V_{d,GO1}=\pm 50\text{mV} \) and \( V_{d,GO2}=\pm 100\text{mV} \). The red straight line is the \(1/f\) spectrum.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.32: Normalized drain current noise power spectral density versus drain current at \( f=1\text{Hz} \) for n-MOS GO1&GO2 [A-B] and p- MOS GO1&GO2 [C-D] devices respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.33: Square root of gate noise voltage spectral density \( \sqrt{\text{S}_{\text{Vg}}} \) versus \( I_d/g_m \) at \( f=1\text{Hz} \) for n-MOS GO1&GO2 [A-B] and p-MOS GO1&GO2 [C-D] with \((W/L)_{GO1}=9/0.04\mu m\) and \((W/L)_{GO2}=9/0.634\mu m\), respectively.
2.6.7 CMOS 28nm

The main process issues of this technology node have been discussed in paragraph 2.5, as well as the behavior of GO1 devices. At this point, we will investigate the GO2 devices and the various threshold voltage devices (RVT, SLVT and HPA). The flavors LVT and SLVT describe devices that are having different threshold voltages from the standard device, RVT. The LVT has a lower and the SLVT a super lower threshold voltage than the standard device, RVT, of the technology node. In order to create different threshold voltages devices some process characteristics should changed such as the channel doping and the pocket concentration. The HPA flavor was designed particularly for analog design purposes and does not have any pockets inside it. The oxide thickness for GO2 is 32/34Å, for n-MOS and p-MOS devices, respectively. The oxide thickness of all other flavors, RVT, SLVT and HPA is the same as the standard GO1 device of the technology meaning 14/17Å, for n-MOS and p-MOS devices, respectively. V_{dd} for GO2 is 1.8V and for all the others 1V. We will present the results from each flavor n- and p- MOS devices with the nominal and a larger channel length and then we will make a comparison of all to see if there are any differences in the LFN behavior. Once more, we underline that the geometries were chosen randomly and the results apply for the tested widths and lengths.

2.6.7.1 CMOS 28nm GO2

In Fig. 2.34, we plot the drain current noise power spectral density versus frequency for n-MOS and p-MOS GO2 [A,B] respectively, with (W/L)_{GO2}=4.5/0.915μm. As can be seen, the LFN spectra for all gate bias voltages are 1/f-like.

In Fig. 2.35, we plot the normalized drain current noise power spectral density versus drain current for the same devices, n-MOS [A] and p-MOS [B], respectively. As can be seen from Fig. 2.35, for both devices the CNF/CMF model explains better the experimental data. This is further verified by checking the linearity between √{S_{Vg}} and I_{d}/g_{m}. From Fig. 2.36 it is clearly seen that the plots of √{S_{Vg}} versus I_{d}/g_{m} are linear for both n-MOS and p-MOS devices. Thus, the CNF/CMF model better explains the experimental results.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.34: Drain current power spectral density versus frequency for n-MOS GO2 [A] and p-MOS GO2 [B] devices, from 28nm technology node with \((W/L)_{GO2}=4.5/0.915\mu m\) and various gate polarization in linear region of operation \(V_{d,GO2}=\pm 100mV\). The red straight line is the \(1/f\) spectrum.

Fig. 2.35: Normalized drain current noise power spectral density versus drain current at \(f=1Hz\) for n-MOS GO2 [A] and p-MOS GO2 [B] devices with \((W/L)_{GO2}=4.5/0.915\mu m\), respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.36: Square root of gate noise voltage spectral density \(\sqrt{S_{Vg}}\) versus \(I_d/g_m\) at \(f=1Hz\) for n-MOS GO2 [A] and p-MOS GO2 [B] with \((W/L)_{GO2}=4.5/0.915\mu m\), respectively.
2.6.7.2 CMOS 28nm RVT

In Fig. 2.37, we plot the drain current noise power spectral density versus frequency for n-MOS and p-MOS RVT, with \((W/L)_{\text{RVT}}=0.9/0.03\mu m\) [A-C] and \((W/L)_{\text{RVT}}=9/0.273\mu m\) [B-D] respectively. As can be seen, the LFN spectra for all gate bias voltages are \(1/f\)-like.

In Fig. 2.38, we plot the normalized drain current noise power spectral density versus drain current for the same devices, n-MOS [A] and p-MOS [B], respectively. As can be seen from Fig. 2.38, for both devices the CNF/CMF model better explains the experimental data except for n-RVT with \((W/L)_{\text{RVT}}=0.9/0.03\mu m\) where the two models can equally explain the LFN behavior. This is further verified by checking the linearity between \(\sqrt{S_{V_g}}\) and \(I_d/g_m\). From Fig. 2.39 it is clearly seen that the plots of \(\sqrt{S_{V_g}}\) versus \(I_d/g_m\) are linear for p-MOS and n-MOS large area devices but not for the small area n-MOS device. Thus, the CNF/CMF model better explains the experimental results except for the n-RVT with \((W/L)_{\text{RVT}}=0.9/0.03\mu m\) which is better explained by the CNF model.

Fig. 2.37: Drain current power spectral density versus frequency for n- and p-MOS RVT devices, from 28nm technology node with \((W/L)_{\text{RVT}}=0.9/0.03\mu m\) [A-C] and \((W/L)_{\text{RVT}}=9/0.273\mu m\) [B-D], and various gate polarization in linear region of operation \(V_{d,RVT}=\pm 50mV\). The red straight line is the \(1/f\) spectra.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.38: Normalized drain current noise power spectral density versus drain current at f=1Hz for n-MOS RVT [A] and p-MOS RVT [B] devices with (W/L)_{RVT}=0.9/0.03 and 9/0.273\,\mu m respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.

Fig. 2.39: Square root of gate noise voltage spectral density $\sqrt{S_{Vg}}$ versus $I_d/g_m$ at f=1Hz for n-MOS RVT [A] and p-MOS RVT [B] with (W/L)_{RVT}=0.9/0.03 and 9/0.273\,\mu m, respectively.

2.6.7.3 CMOS 28nm SLVT

In Fig. 2.40, we plot the drain current noise power spectral density versus frequency for n-MOS and p-MOS SLVT, with (W/L)_{SLVT}=0.9/1.803\,\mu m [A-C] and (W/L)_{SLVT}=0.9/0.03\,\mu m [B-D] respectively. As can be seen, the LFN spectra for all gate bias voltages are 1/f-like.

In Fig. 2.41, we plot the normalized drain current noise power spectral density versus drain current for the same devices, n-MOS [A] and p-MOS [B], respectively. As can be seen from Fig. 2.41, for both devices the CNF/CMF model explains better the experimental data. This is further verified by checking the linearity between $\sqrt{S_{Vg}}$ and $I_d/g_m$. From Fig. 2.42 it is clearly seen that the plots of $\sqrt{S_{Vg}}$ versus $I_d/g_m$ are linear for p-MOS and n-MOS devices. Thus, the CNF/CMF model better explains the experimental results.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.40: Drain current power spectral density versus frequency for n- and p-MOS SLVT devices, from 28nm technology node with \((W/L)_{SLVT}=0.9/1.803\mu m\) [A-C] and \((W/L)_{SLVT}=0.9/0.03\mu m\) [B-D], and various gate polarization in linear region of operation \(V_{d,\text{RVT}}=\pm50mV\). The red straight line is the 1/f spectra.

Fig. 2.41: Normalized drain current noise power spectral density versus drain current at \(f=1Hz\) for n-MOS SLVT [A] and p-MOS SLVT [B] devices with \((W/L)_{SLVT}=0.9/1.803\) and \(0.9/0.03\mu m\) respectively at \(f=1Hz\). The black straight line is the CNF model and the dotted line the CNF/CMF.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.42: Square root of gate noise voltage spectral density $\sqrt{S_{V_g}}$ versus $I_d/g_m$ at $f=1\text{Hz}$ for n-MOS SLVT [A] and p-MOS SLVT [B] with $(W/L)_{SLVT}=0.9/1.803$ and 0.9/0.03μm, respectively.

2.6.7.4 CMOS 28nm HPA

In Fig. 2.43, we plot the drain current noise power spectral density versus frequency for n-MOS and p-MOS HPA, with $(W/L)_{HPA}=0.9/0.903\mu m$ [A-C] and $(W/L)_{HPA}=0.9/0.09\mu m$ [B-D] respectively. As can be seen, the LFN spectra for all gate bias voltages are 1/f-like.

In Fig. 2.44, we plot the normalized drain current noise power spectral density versus drain current for the same devices, n-MOS [A] and p-MOS [B], respectively. As can be seen from Fig. 2.44, for both devices the CNF/CMF model explains better the experimental data. This is further verified by checking the linearity between $\sqrt{S_{V_g}}$ and $I_d/g_m$. From Fig. 2.45 it is clearly seen that the plots of $\sqrt{S_{V_g}}$ versus $I_d/g_m$ are linear for p-MOS and n-MOS devices. Thus, the CNF/CMF model better explains the experimental results.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.43: Drain current power spectral density versus frequency for n- and p-MOS HPA devices, from 28nm technology node with (W/L)$_{HPA}$=0.9/0.903µm [A-C] and (W/L)$_{HPA}$=0.9/0.09µm [B-D], and various gate polarization in linear region of operation $V_{d,\text{RVT}}=\pm50$ mV. The red straight line is the 1/f spectra.

Fig. 2.44: Normalized drain current noise power spectral density versus drain current at $f=1$ Hz for n-MOS HPA [A] and p- MOS HPA [B] devices with (W/L)$_{HPA}$=0.9/0.903 and 0.9/0.09µm respectively. The black straight line is the CNF model and the dotted line the CNF/CMF.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.45: Square root of gate noise voltage spectral density $\sqrt{S_{V_g}}$ versus $I_d/g_m$ at $f=1$Hz for n-MOS HPA [A] and p-MOS HPA [B] with (W/L)$_{HPA}$=0.9/0.903 and 0.9/0.09$\mu$m, respectively.

2.6.7.5 Comparison CMOS 28nm

The above results can be summarized and analyzed by plotting the volumetric trap density $N_t$ and the product of Coulomb scattering coefficient with effective mobility $\alpha'=\alpha_{sc}\cdot\mu_{eff}$ versus channel length of the investigated flavors n- and p-MOS devices from 28nm technology node.

Fig. 2.46 [A-B] shows that there is no difference between the three flavors of different $V_{th}$ - RVT, LVT and SLVT - indicating no effect in the volumetric oxide trap density by changing the threshold voltage of a device. In contrast, it can be seen from Fig. 2.46 [A-B] that there is a small reduction in $N_t$ for devices with different gate oxide GO2.

Fig. 2.46: Evolution of the volumetric trap density $N_t$ with the channel length for all measured n-MOS [A] and p-MOS [B] devices from the 28nm technology node.

In particular, the GO2 devices present a smaller $N_t$ values underlying the impact of oxide thickness on the gate oxide trap density which will be verified in the global evolution of $N_t$ versus oxide thickness later on. Finally, it should be mentioned at this point that the impact of
SiGe in the channel of all p-MOS transistors and for all the measured flavors is a small raise of oxide trap density as mentioned in paragraph 2.5.

In Fig. 2.47 [A-B] we plot the evolution of the effective Coulomb scattering coefficient $\alpha' = \alpha_{sc} \mu_{eff}$ with the channel length for all the measured devices, n- and p-MOS, from 28nm technology node. The parameter $\alpha'$ has been extracted from the experimental noise data using the CNF/CMF model. From the graph one can clearly see that for both types of devices $\alpha'$ remains almost constant for all the channel length and the different flavors of the technology node. There is a small increase for GO2 n- and p- MOS devices.

### 2.7 Comparison of LFN in CMOS bulk technology nodes

The above results can be summarized by plotting the volumetric trap density $N_t$ versus the equivalent oxide thickness of the investigated n-MOS and p-MOS devices to have an idea about the evolution of LFN through almost all bulk technology nodes. Figure 2.46 shows that in both n-MOS and p-MOS devices from 28nm technology node the oxide trap density $N_t$ remains almost constant with the channel length $L$ for all the “flavors” measured, i.e. $N_t$ remains almost unchanged with channel length for this technology node except of the device with different oxide thickness, GO2. That observation was the moving force to plot the $N_t$ values from all the technology nodes versus the equivalent oxide thickness and see the impact of EOT in the volumetric trap density. It is underlined that in all cases the volumetric trap density was calculated from Eq. (2.9) using the flat band voltage spectral density extracted from the experimental data of $S_{id}/I_d^2$ versus $(g_{m}/I_d)^2$ for all the technology nodes and devices.
using the CNF model and the noise data below threshold voltage where the CNF model best fits the experimental data.

Figure 2.48 presents the evolution of the volumetric trap density $N_t$ with scaling down the oxide thickness for all n-MOS devices. This figure shows that $N_t$ tends to diminish as the oxide thickness is augmented. One can say that this is expected, as in thicker oxides the number of traps near the gate interface is reduced. However, more careful examination of the results of Fig. 2.48 shows that for gate dielectric of the same thickness, the dielectric quality is different in the various technology nodes.

For example, for the technology nodes CMOS 90nm/GO2 and CMOS 65nm/GO2 with $t_{ox}=65\text{Å}$, the dielectric trap density changes by a factor of five. This can be better understood by plotting in Fig. 2.49 the normalized drain current noise spectral density as a function of the normalized drain current for these devices. From this figure is clear that the normalized noise level is different in these devices although they have the same oxide thickness. The impact of the technology process is clearly indicated in this example. Figure 2.50 presents another example of devices with oxide thickness 120Å from the technology node CMOS 0.25µm GO1 and 150Å from the technology node CMOS 65nm HV. From this figure is clear that these devices, even though they have similar equivalent oxide thicknesses, there is a difference in noise level by one order of magnitude explaining the difference in $N_t$. 

Fig. 2.48: Evolution of the volumetric trap density $N_t$ with scaling down the equivalent oxide thickness for all measured n-MOS devices.

For example, for the technology nodes CMOS 90nm/GO2 and CMOS 65nm/GO2 with $t_{ox}=65\text{Å}$, the dielectric trap density changes by a factor of five. This can be better understood by plotting in Fig. 2.49 the normalized drain current noise spectral density as a function of the normalized drain current for these devices. From this figure is clear that the normalized noise level is different in these devices although they have the same oxide thickness. The impact of the technology process is clearly indicated in this example. Figure 2.50 presents another example of devices with oxide thickness 120Å from the technology node CMOS 0.25µm GO1 and 150Å from the technology node CMOS 65nm HV. From this figure is clear that these devices, even though they have similar equivalent oxide thicknesses, there is a difference in noise level by one order of magnitude explaining the difference in $N_t$. 

68
Fig. 2.49: Normalized drain current power spectral density versus normalized drain current for CMOS 90nm/GO2 and CMOS 65nm/GO2 with (W/L) =1/1.2 -0.6/0.38, respectively.

Fig. 2.50: Normalized drain current power spectral density versus normalized drain current for CMOS 0.25µm/GO1 and CMOS 65nm/HV with (W/L) =10/0.45 -9/0.9µm, respectively.

In Fig. 2.51, we present the evolution of the volumetric trap density N_t with the equivalent oxide thickness for all p-MOS devices. The graph shows that there is a tendency N_t to diminish as the equivalent oxide thickness is increased following a rule of N_t~1/EOT^2. However, there are still some cases not following this general rule and need to further
Chapter 2: Low frequency noise in bulk MOSFETs

investigation. Starting from the impact of high-k/metal gate in the 28nm technology node, the graph shows that there is a huge difference in $N_t$ level between CMOS 45nm/GO1 and CMOS 28nm/GO1 although the oxide thickness is almost the same. The answer can be found in Fig. 2.52 where we plot the normalized drain current noise spectral density versus normalized drain current for these devices. From the graph is clear that there is almost a decade of difference in the noise level between the two devices, with higher value for the 28nm technology node. This is expected because of the different gate stack used in the 28nm technology node, which today is well known that increases the noise level.

Fig. 2.51: Evolution of the volumetric trap density $N_t$ with scaling down the equivalent oxide thickness for all measured p-MOS devices.

Figure 2.53 presents another example of irregularities in the $N_t$ values. We plot the normalized drain current noise spectral density versus normalized drain current for devices from the technology nodes CMOS 45nm/GO2 and CMOS 0.18μm/GO1 with the same oxide thickness and CMOS 28nm/GO2 with oxide thickness slightly higher. It is shown that the devices from the technology nodes of 0.18μm and 28nm have the same noise level, but different oxide thickness, which explains the different $N_t$ values. The device from 45nm technology node has almost one decade lower noise level, which explains the smaller $N_t$ value in Fig. 2.51.
Finally, in Fig. 2.54 we plot the evolution of the effective Coulomb scattering coefficient $\alpha' = \alpha_{sc} \mu_{eff}$ with the equivalent oxide thickness for all the measured devices. The parameter $\alpha'$ has been extracted from the experimental noise data using the CNF/CMF model. From the graph one can clearly see that for both types of devices $\alpha'$ remains almost constant through the evolution of the oxide thickness. Furthermore, the parameter $\alpha'$ is higher in the p-MOS devices as expected.
Chapter 2: Low frequency noise in bulk MOSFETs

Fig. 2.54: Variation of $\alpha' = \alpha_{sc} \mu_{eff}$ with equivalent oxide thickness for all the measured devices where the CNF/CMF model fits better the experimental results.

2.8 Conclusions

From the above analysis, it is obvious that the LFN analysis in CMOS bulk devices is much more complicated than some people believe. The overall results obtained from all technology nodes show that the developed compact noise model is applied in most of the cases but there are still few ones where the model does not work properly. At this point, several questions give rise: What are the criteria to distinguish the CNF from the extended CNF/CMF model? Why in some cases the one or the other model applies and not in every case? What is the physical phenomenon that distinguishes the two models? All these questions need to be clarified. Even though we have achieved till now to understand several issues regarding LFN, much more need to be done. A rather new idea is to consider that the two terms in CNF/CMF model are uncorrelated. What does that mean? It means that the physical phenomenon is the same, trapping/detrapping of carriers into slow oxide traps but the result is divided into two parts, the one affects the carrier number within the channel and the other affects the carrier mobility. This issue we believe that needs more investigation in order to fully understand the LFN mechanisms and physics.

On the other hand, the historical figures describing the volumetric trap density $N_t$ for n- and p-MOS devices give us some new insights about LFN in MOSFETs. Starting from Fig. 2.48 for n-MOS devices, it is clear that for this type of devices the process affects significantly the $N_t$ values. We cannot conclude for an empirical rule connecting $N_t$ values with $t_{ox}$. The technology process plays a more important role than the oxide thickness as was previously believed. The situation is simpler for p-MOS devices as shown in Fig. 2.51, where we plot the same graph for p-MOS devices. The impact of the technology for this type of
devices is diminished compared to n-MOS. From Fig. 2.51, we can conclude that $N_t$ is inversely proportional to $EOT^2$. The general rule of circuit designers that p-MOS devices are less noisy than the n-MOS was till now true. However, for the 28nm technology node this rule is not applied, i.e. p-MOS devices are noisier than n-MOS devices.
Chapter 2: Low frequency noise in bulk MOSFETs

References


Chapter 3: Low frequency noise variability in bulk and FD-SOI MOSFETs

3.1 Origin of the LFN variability ................................................. 77
3.2 Impact of the LFN variability on circuit operation ................. 80
3.3 Statistical analysis of the LFN variability ............................. 81
3.4 Experimental results of the LFN variability measurements ..... 86
  3.4.1 CMOS 28nm Bulk devices ........................................ 86
  3.4.2 CMOS 28nm FD-SOI devices ...................................... 90
3.5 Experimental results of the LFN variability in bulk n- and p-
  MOSFETs of different technology nodes ............................... 100
3.6 Development of the LFN variability model .......................... 103
  3.6.1 Bulk Transistors .................................................... 103
  3.6.2 FD-SOI Transistors ................................................ 107
    3.6.2.1 FD-SOI Transistors $V_b=0V$ ............................... 113
    3.6.2.2 FD-SOI Transistors $V_b=\pm10V$ ......................... 115
3.7 Conclusions ....................................................................... 116
References ............................................................................. 118
Chapter 3
Low frequency noise variability in bulk and FD-SOI MOSFETs

3.1 Origin of the LFN variability

This chapter is aimed to define the LFN variability and investigate its origin. LFN variability is the difference in LFN level from device-to-device of the same geometry on the same wafer but different dies, Fig. 3.1. As can be seen from Fig. 3.1 the dispersion of the drain current noise is enhanced by 2-3 decades from large to small area n-MOS devices. The same results were obtained for p-MOS devices as well. The difference in drain current noise level from die-to-die devices of the same area is the key concept of LFN variability. In this thesis, we present the results and analysis of LFN variability from device-to-device measurements of different dies on the same wafer.

As we have shown in Chapter 2, for almost all the tested technologies, the LFN origin is due to carrier number with correlated mobility fluctuations (CNF/CMF). The classical CNF model is based on the summation of individual traps each one producing an RTS signature. Today it is generally believed that the RTS noise is associated with the origin of LFN variability. We will try at this point to clarify and understand the causes of LFN variability.
through the standard LFN model and RTS noise. According to the CNF/CMF model, which is summarized in Eq. (2.35), the first parameter which we expect that can explain LFN variability is the volumetric trap density $N_t$. In the same way that doping fluctuations (number of channel doping) is one of the major DC parameter variability, the number of traps from die-to-die can fluctuate enough to cause dispersion in the LFN level of the devices. A rapid analysis of LFN variability induced by $N_t$ could be the following. For large area devices (100 µm²), and considering a trap density of $10^{18}$ /cm³/eV, several thousands of traps are present in each device. From die to die, the variation of $N_t$ in a well control process induce a “small” spread because the number of traps can not vary a lot. For a small area device, (minimum Width and Length), the volume is sufficiently small to have only few traps inside it. Thus, the LFN variability is much higher because the variation of the traps that contribute to the drain current fluctuations is large. Can the LFN variability phenomenon be explained only from the fluctuations of the number of traps from die-to-die? We are going to explain in details the answer to that question at the following paragraphs.

In Fig. 3.2, we plot the time and frequency domain trace of LFN (A) - (B) and RTS, (C) – (D), respectively. From Fig. 3.2, it can be concluded that the corresponding spectrum for flicker noise is the sum of many RTS fluctuators or in more detail the sum of Lorentzian spectra that eventually give the 1/f spectrum. The detailed analysis of RTS noise in MOSFETs was extensively investigated in the past years [65-70]. It is not the purpose of this thesis to repeat all that is already known in the scientific community. Nevertheless, it would be quite informative to express the RTS noise with simple equations in order to have the basic background to understand the proposed LFN variability model later on. From Fig. 3.2 (D), it can be concluded that the drain current spectral density of an RTS which exhibits a Lorentzian spectrum would be given by the equation [65]:

$$ S_{I_d} = 4 \cdot A \cdot A \cdot \frac{\tau}{1+\omega^2 \cdot \tau^2} $$

(3.1)

where $1/\tau = 1/\tau_c + 1/\tau_e$ is an effective time constant, the capture and emission times are evaluated according to the Shockley-Read-Hall statistics [78-79] as $\tau_c=1/(\sigma \cdot n_s \cdot v_{th})$ and $\tau_e=1/(\sigma \cdot n_1 \cdot v_{th})$ where $n_s$ is the surface carrier concentration, $n_1$ is the surface carrier concentration when the Fermi level $E_f$ equals the trap energy $E_t$ and $\sigma$ is the cross section of the trap including the activated process. $\tau = \tau_s \cdot \exp(x/\lambda)$ where $\tau_s$ is a constant, $x$ is the trap distance into the dielectric and $\lambda$ is the tunneling attenuation distance. $A = \tau/(\tau_c + \tau_e) = f_t (1-f_t)$ is the space mark ratio, $\omega=2 \cdot \pi \cdot f$ is the angular frequency and $f_t$ is the trap occupancy factor, $f_t=1/[1+\exp[(E_t-E_f)/kT]]$ with $E_t$ being the trap energy and $E_f$ the Fermi level position. Eq.
(3.1) is just a formula to describe a Lorentzian like behavior and thus is the basis for the overall explanation of RTS noise or better of LFN variability. The drain current RTS amplitude can be calculated assuming that the trapping of an elementary charge $q$ in the channel changes the local conductivity. It is easy to show that, in a first order approximation, the relative drain current RTS amplitude reads [65]:

$$ \frac{\Delta I_d}{I_d} = \frac{g_m}{I_d} \cdot \frac{q}{W \cdot L \cdot C_{ox}} $$

Equations (3.1-3.2) explain the basic characteristic of a single RTS trap and thus can be used to develop a model explaining the LFN variability, which originates from the activation of many RTS fluctuators. It is underlined that, according to Eqs. (3.1)-(3.2) of the basic RTS theory, we can make some useful remarks concerning the LFN variability behavior. The
quantities that we expect to play an important role in the LFN variability behavior of the devices are the volumetric trap density of the gate interface, as we already mentioned, the equivalent oxide capacitance, the transconductance to drain current ratio and finally the fluctuations of the characteristics of the traps such as the energy level, the cross section and the time constants relate to each one of them. Each factor can affect the LFN variability in a different way, according to our proposed model and analysis of the experimental results presented below.

Here, we try to give a different perspective of the way for examining the RTS noise and its impact on circuit behavior. In order to evaluate the impact of RTS on the circuit behavior, as it is generally accepted nowadays, we perform time domain measurements on many geometries, from large to small ones and with different bias conditions for both drain and gate voltages. In addition, statistical analysis should be performed to verify the RTS behavior meaning that the previous work should be applied to many dies on the same wafer. It is clear that this procedure is time consuming and very complicated to analyze in terms of data size. We propose a different way to analyze LFN variability direct from LFN measurements which is faster, it has the same level of reliability since the frequency and time domain footprints are correlated and finally it is much easier in terms of analysis and time spent to do it. First, we refer below an example of the impact of RTS on CMOS circuits in order to better understand the importance of this phenomenon.

3.2 Impact of the LFN variability on circuit operation

The impact of the LFN variability and in particular of RTS on CMOS digital circuits is well known nowadays [71-74]. We present here the impact of LFN variability on a standard digital cell like SRAM [75]. In order to illustrate the impact of the LFN variability on the digital circuit operation, the butterfly characteristic of a SRAM cell has been simulated with nominal dimension 28nm CMOS devices with an average trap density $N_{it}=10^{11}/cm^2$, Fig. 3.3. Since SRAM cell is operated at high frequency, LFN and RTS fluctuations behave as quasi-static events, resulting in dispersion of the threshold voltage from device to device given by Eq. 3.3 [75].

$$V_t = V_{t0} + \sum_{k=0}^{N_{itot}} qAmp_{k}\frac{Amp_{k}}{W.L.C_{ox}}$$

(3.3)

where $V_t$ and $V_{t0}$ is the threshold voltage after and before the trapping/detrapping of a carrier into a trap, $N_{itot}$ is the total number of traps following a Poisson law describing the $\Delta V_t$.
distribution, \( \text{Amp}_k \) is the RTS random amplitude modulation given by \( \text{Amp}=10^\alpha \) with \( \alpha=0 \) to 0.25, \( W \) and \( L \) is the channel width and length and \( C_{ox} \) the equivalent oxide capacitance.

Such \( V_t \) dispersions are nearly Gaussian with standard deviation \( \sigma_{V_t} \), and give rise to a static noise margin reduction of the cell when a large statistical number of samples (here \( 4 \times 10^6 \) transistors) are simulated, Fig. 3.3. It is clear from Fig. 3.3 that the difference in static noise margin (SNM) from the maximum, average and minimum threshold voltage simulated may cause dysfunctions of this basic standard cell. We underline at this point that the values of \( \sigma_{V_t} \) found from this simulation were calculated for a very large number of transistors, 4 millions and that is why it may be elevated.

![Fig. 3.3: Circuit simulation of inverter characteristic CMOS area=400nm², \( t_{ox,eff}=2\text{nm} \), \( N_n=10^{11}/\text{cm}^2 \), Number of transistors=\( 4 \times 10^6 \). The green, blue and red lines correspond to maximum, average and minimum threshold voltage \( V_t \).](image)

### 3.3 Statistical analysis of the LFN variability

After the introduction of the origin and impact of the LFN variability, we explain how the frequency domain measurements were performed and how we can characterize the LFN variability behavior of any CMOS technology node. As previously mentioned, the frequency domain behavior of a device is simply the transformed time domain expression through the Fast-Fourier transform. We can characterize the LFN variability behavior of a technology node from standard LFN tests. We have to measure the spectra of many different area devices from different dies on the same wafer. The arising question is which physical quantities have to be investigated statistically and in addition which criteria have to be used for such a decision.

First, the term statistical analysis implies that we have to calculate the median and the standard deviation from a distribution of data in order to decode their behavior. The problem
that appears is which quantity has to be investigated statistically. A simple answer to this question is the drain current noise at a fixed frequency and gate voltage. However, it seems that it is not enough since with this choice the following two issues appear.

The first one is that we measure the LFN of a device for a fixed gate voltage. Thus, when we analyze the power spectral density of the drain current at a fixed frequency and gate voltage, we will encounter the variations of the drain current itself within the LFN. When we measure a device of a given geometry at a fixed gate voltage, the drain current from device-to-device from different dies is varying. In particular, the variation is expected to be large for small area devices compared to large ones. Thus, the study of the drain current noise at a fixed frequency and gate voltage is expected to result in misleading conclusions, not related with the LFN variability itself and the static parameters variation. For this reason, we decided to investigate the normalized drain current noise, avoiding in this way the variations of the drain current in the LFN variability behavior of a MOSFET.

The second issue concerns the choice of the frequency. In Fig. 3.4, we plot the drain current noise versus frequency of a small n-MOS from the 28nm bulk technology node and a normalized drain current around 10nA. It can be concluded from Fig. 3.4 that the dispersion in the drain current noise remains almost the same for all frequencies till the cut off frequency of the current amplifier used in the measurement equipment. We have calculated the standard deviation of the $S_{dd}$ dispersion at the two different frequencies of 10 and $10^3$ Hz and we found almost the same values, Fig. 3.4. In our investigations of the LFN variability, we used the noise data at the frequency of 10Hz.

![Fig. 3.4: Drain current noise PSD as a function of frequency for n-MOS bulk with (W/L)=0.072/0.03μm for at least 45 dies and L/W*Ln≈10nA.](image)

When analyzing the normalized drain current power spectral density dispersion, we noticed that its distribution for a large number of samples does not have a normal behavior from a statistical point of view. In Fig. 3.5, we plot the histogram of the normalized and of the
logarithm of the normalized drain current power spectral density at 10Hz for a small and a large area n-MOS devise from 28nm CMOS bulk technology node. The normalized drain current power spectral density does not show normal behavior for the large and small area devices, Fig. 3.5 (A-B). In contrary, the distributions in logarithmic representation of the normalized drain current power spectral density dispersion present a normal behavior for large and small areas n-MOS, Fig. 3.5 (C-D). From Figs. 3.6-3.7, it can be clearly seen that the logarithm of the normalized drain current noise shows Gaussian behavior for all types of devices small and large area, Bulk and FD-SOI and this is the reason for choosing this quantity to perform statistical analysis.

![Histograms](image-url)

Fig. 3.5: Histogram of the distribution of the normalized drain current power spectral density for n-MOS at f=10Hz in (A) with W/L=9/9.003μm and in (B) with W/L=0.072/0.03μm and in (C) and (D) for the logarithm of the normalized drain current power spectral density for at least 45 dies.
Let us make a small parenthesis in the flow of this chapter and try to define with simple words the importance of the above remark. There are several ways to define the “normal distribution” formally, but the simple intuitive idea of it is that in a normal distribution, things tend towards the mean – the closer value to the mean, the more frequent it can be seen and the values on either side of the mean at any particular distance are equal. A normal (Gaussian) distribution is one where the data are evenly distributed around the mean in a very regular way, which when plotted as a histogram will result in a bell shaped curve. In Figs. 3.5-3.7 the normality was tested using Origin Lab software normality test and the results can be seen in the sub-images in Fig. 3.5.

Fig. 3.6: Histogram of the distribution of the normalized drain current power spectral density for n-MOS FD-SOI at f=10Hz with Area of 0.027 and 8.127 μm² in (A) and (B), respectively and for n-MOS bulk with Area of 81.027 and 0.017 μm² in (C) and (D), respectively.
Fig. 3.7: Histogram of the distribution of the normalized drain current power spectral density for p-MOS FD-SOI at f=10Hz with W/L=9/0.903 and 0.9/0.03 μm in (A) and (B), respectively and for p-MOS bulk with W/L=9/0.12 and 0.9/0.03 μm in (C) and (D), respectively.

The third issue concerns the procedure for deciding the constant gate voltage used for statistical investigation of the LFN variability. The question is if there is any difference for analysing the noise data obtained at a constant gate voltage below or above threshold voltage. In Fig. 3.8, we plot the standard deviation of the logarithm of the normalized drain current noise versus gate voltage for large and small area devices from the 28nm Bulk and FD-SOI technology node, with back gate in FD-SOI grounded. It can be concluded from Fig. 3.8 that the standard deviation of the logarithm of the normalized drain current noise remains constant for all gate biases and all types of transistors. For this reason, we have investigated the logarithm of the normalized drain current noise at a fixed gate voltage, giving a normalized drain current around 10nA for all the technologies measured.
3.4 Experimental results of the LFN variability measurements

The experimental results of the LFN variability measurements are presented in two parts. First, we present the experimental results from the 28nm bulk CMOS technology node manufactured in STMicroelectronics@Crolles. We characterized various threshold voltage and different oxide thickness n- and p-MOS devices, as already explained in Chapter 2, paragraph 2.6. We investigate the LFN variability behavior of these devices. Thereafter, we repeat this task for the FD-SOI 28nm CMOS technology node. Different architectures of n- and p-MOS devices from different process splits of the technology node have been characterized with various back gate polarizations. Finally, a historical evolution of the LFN variability in the last five bulk CMOS technology nodes will be presented.

3.4.1 CMOS 28nm Bulk transistors:

In Fig. 3.9, we plot the drain current noise spectra versus frequency for n- MOS bulk large (A) and small (B) area devices and for p- MOS bulk large (C) and small (D) area devices, respectively for a fixed normalized drain current around \( \frac{L}{W} \cdot I_d \approx 10 \text{nA} \) from the 28nm technology node. The impact of the device area on LFN variability is revealed clearly in this way. The small area n- and p- MOS devices show large dispersion in the drain current noise spectra. Indeed, decreasing the device area from 4.887 to 0.0216 \( \mu \text{m}^2 \) for n-MOS and from 8.127 to 0.0216 \( \mu \text{m}^2 \) for p-MOS, the LFN variability is enhanced by 2-3 decades, where the spectrum changes from 1/f to Lorentzian-like behavior. This was the first proof of the impact of RTS on the LFN variability, the change of the type of spectra and it was the basis of our LFN variability model. The same behavior was observed for all measured devices.
In Fig. 3.10, we plot the standard deviation of the normalized drain current noise versus gate voltage for n- (A) and p- (B) MOS LVT devices. It can be seen that the standard deviation remains constant for all gate polarizations, small and large area devices. The same results obtained for all the measured devices. That was the reason why we investigated the LFN variability in bulk devices in a fixed normalized drain current below threshold voltage as we mentioned in details in paragraph 3.3.

Fig. 3.9: Drain current noise PSD as a function of frequency for n-MOS bulk with (W/L)=0.72/0.03 and 9/0.903μm in (A) and (B), respectively and for p-MOS bulk with (W/L)=0.72/0.03 and 9/0.903 μm in (C) and (D), respectively for at least 45 dies and L/W*I_d~10nA.

Fig. 3.10: Standard deviation of the logarithm of the normalized drain current noise versus the gate voltage at f=10Hz for n-MOS LVT (A) and p-MOS LVT (B) 28nm CMOS bulk large and small area devices, respectively.
In Fig. 3.11, we plot the normalized drain current noise versus area for different threshold voltage and gate oxide thickness n-MOS devices and fixed normalized drain current around 10nA at a fixed frequency of 10Hz. It can be seen that all the measured devices show similar dispersion characteristics and furthermore the median normalized noise level is almost the same for all the flavors, LVT, RVT and GO2. In Fig. 3.11 (D), we plot the standard deviation of the normalized drain current noise versus the square root of area for the mentioned devices. It can be concluded that all the measured devices present almost the same behavior in terms of standard deviation values. Thus, we decided to compare the experimental results with the simulation model for the LVT n-MOS device, since the LFN variability behavior remains the same for the devices with different architecture.

The same results were reproduced for the p-MOS devices, Fig. 3.12. From the plotted data, we can conclude that the LFN variability behavior of p-MOS devices follows the same pattern as for n-MOS. There are no important differences in the dispersion of the normalized noise level between the different measured flavors, Fig. 3.12 (A-C). We should keep in mind that
the normalized drain current noise was not exactly the same in all cases; it is not possible to achieve the same normalized drain current for all the geometries. Thus, it is normal that in some cases the median noise level is changing. The standard deviation behavior of the different flavors p-MOS devices, Fig. 3.12 (D), is almost identical. The standard deviation for GO2 devices shows a little better control of LFN variability.

Fig. 3.12: Normalized drain current noise at a fixed frequency of 10Hz versus area for p-MOS 28nm CMOS LVT(A), RVT (B) and GO2 (C) and for a fixed normalized drain current around 10nA , respectively and the standard deviation of the logarithm of the normalized drain current noise versus the inverse of the square root of area in (D). The black straight line is the median value.

From Figs. 3.11-3.12, it can be summarized that there are no important differences in LFN variability behavior from different flavors of the same type devices and from different type, n- and p-MOS devices as well. This characteristic is verifying our LFN variability model, the device type is not taken into account when the LFN variability is simulated. It assumes that the transconductance to drain current ratio, the volumetric trap density with the specific characteristics of each trap and the gate oxide thickness play a significant role in LFN variability. These are not the only factors that can influence the LFN variability behavior of the devices. The process of the CMOS technology can also affect the LFN variability behavior. It seems that for the measured devices, n- and p-MOS, these parameters may be
different in some cases, such as in LVT, RVT and GO2 devices with different oxide thickness, as well as between n- and p-MOS devices. However, the overall LFN variability behavior remains very similar because of the similar values of volumetric trap density, as we have seen in Chapter 2, transconductance to drain current ratio but also because of the process which is almost identical in all cases.

3.4.2 CMOS 28nm FD-SOI transistors:

The FD-SOI LFN variability analysis is held in parallel with the development of the new technology node in the process and R&D level. We present the results from three different wafers, which incorporate the evolution of the technology node from the R&D to the production level. In our analysis, we investigate the evolution of LFN variability in FD-SOI devices and thus, in some cases it is accompanied with basic LFN analysis in order to better understand the impact of this technology node on the overall LFN variability behavior of the MOSFETs.

The first measured wafer (called CPK) is represented in the graph of Fig. 3.13. The devices are fabricated on silicon substrates with 25nm thick Burried-Oxide (BOX). The Si film thickness is 7nm after process steps. The gate stack is close with the one of the 28nm bulk technology node. This was the first wafer introduced in this technology. We measured different areas devices, n- and p-MOS.

![Fig. 3.13: Schematic diagram of a FD-SOI device with no back gate bias possibility. The back gate contact was literally at the back of the device thus, any bias would apply to the whole wafer.](image-url)
In Fig. 3.14, we plot the standard deviation of the logarithm of the normalized drain current noise versus gate voltage for n- and p-MOS devices from the wafer CPK with back gate polarization grounded $V_b=0V$. It can be concluded from Fig. 3.14 that the standard deviation remains almost constant for all the gate bias polarizations, as already observed in bulk devices. For this reason, we have investigated the LFN variability at a fixed gate voltage giving a normalized drain current around 10nA.

In Fig. 3.15, we plot the normalized drain current noise at a fixed frequency of 10Hz versus area for n-MOS (A) and p-MOS (B) 28nm CMOS FD-SOI large and small area devices, respectively. Back gate polarization grounded $V_b=0V$.

In Fig. 3.16, we plot the standard deviation of the normalized drain current noise versus the

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Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

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Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

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Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

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In Fig. 3.15, we plot the normalized drain current noise at a fixed frequency of 10Hz versus area for n-MOS (A) and p-MOS (B) 28nm CMOS FD-SOI large and small area devices, respectively. Back gate polarization grounded $V_b=0V$.

In Fig. 3.15, we plot the normalized drain current noise at a fixed frequency of 10Hz versus area for n-MOS (A) and p-MOS (B) 28nm CMOS FD-SOI large and small area devices, respectively. Back gate polarization grounded $V_b=0V$.

In Fig. 3.16, we plot the standard deviation of the normalized drain current noise versus the
square root of area for the mentioned n- and p- MOS devices and in addition for the n- and p- MOS from 28nm bulk technology node. First for FD-SOI transistors, it seems that the p- MOS devices show slightly larger values compared to the n-MOS. However, the FD-SOI devices seem to control a slightly better the LFN variability compared to their bulk ancestors since they show smaller values of standard deviation for both n- and p- MOS transistors. These results can be further supported in view of Fig. 3.16 (B), where we plot the standard deviation of $\Delta V_{th}$ as a function of the inverse square root of the device area for the mentioned devices. From Figs. 3.15-3.16, it can be concluded that the LFN variability behavior for both devices follows the static matching performance even though they are not identical phenomena except of their dependence in equivalent oxide capacitance.

![Fig. 3.16: Standard deviation of the normalized drain current noise at a fixed frequency of 10Hz versus area for n- and p-MOS (A) 28nm CMOS FD-SOI wf CPK and 28nm Bulk for a fixed normalized drain current around 10nA, respectively. In (B) comparison of standard deviation of $\Delta V_{th}$ as a function of the inverse square root of the device area between the same devices, the results for n- and p- MOS were identical.](image)

After the first introduction of FD-SOI technology node, many process variations were introduced. In Fig. 3.17, we represent these additions to the initial wafer CPK analyzed previously. FD-SOI technology allows a hybrid scheme co-integrating both bulk and SOI devices on the same die. Thin box is opened for bulk parts with NOSOI mask. Leveraging FD-SOI back-side gate capability, a Ground-Plane (GP) implantation has been developed to adjust transistors $V_{th}$. Actually, the GP for logic devices is gate-type whereas the GP of SRAM devices is opposite, in order to adjust accurately threshold voltage for the entire devices suite. HK/MG process is adjusted to control $V_{th}$ of thin and thick gate oxide devices simultaneously for both n- and p- MOSFETs. In order to arrive at these process characteristics of FD-SOI technology node we characterized the impact of almost each one process step in
LFN variability behavior of n- and p-MOS transistors. Thus, we investigated the LFN variability of different wafers compared to the reference, wf JRG, having the following characteristics: 1) wf #09 with opposite type of GP compared to the gate type, 2) wf #10 with final annealing of the gate stack, 3) wf #18 with Poly silicon for gate stack, 4) wf #07 without BOX and 5) wf #19 single gate TiN for n- and p-MOS devices. The back gate polarization for all the splits was \( V_{\text{b}} = 0 \text{V} \).

Fig. 3.17: Schematic diagram of an Ultra Thin Body (FD) and BOX SOI.

The analysis of these wafers started with the investigation of the LFN behavior. In Fig. 3.18, we plot the normalized drain current noise versus drain current for the mentioned wafers n- and p-MOSFET with \((W/L) = 1/1\mu\text{m}\). From Fig. 3.18 (A) for n-MOS, it can be concluded that the LFN level for all the splits remains almost the same except for a small increase of noise level for wf #18, indicating the impact of polysilicon gate in the LFN behavior of the devices. On the other hand, for p-MOS, Fig. 3.18 (B), the noise level is even more dispersed for the different splits with higher values again for wf #18 and smaller for wf #19. These results alone cannot help us to fully understand the LFN behavior of the devices. Therefore, in Fig. 3.19 we plot the transconductance to drain current ratio versus drain current for n- and p-MOS transistors. From Fig. 3.19, it can be seen that the transconductance to drain current ratio remains unchanged for n- and p-MOS devices and for all the measured wafers. The LFN level difference appeared in different splits can be attributed to the different quality of the gate interface since the oxide thickness and the transconductance to drain current ratio are the same. Based on these observations we calculated the volumetric trap density of the front interface from the LFN results, considering the CNF model and using Eq. 2.9, Fig. 3.20. We can now create a more solid opinion concerning the results of Fig. 3.18. The \( N_t \) values for n-
MOS, for the front interface, can be explained from the difference in the normalized drain current noise with higher $N_t$ values for wf #18 according to the higher noise level observed in this wafer. The $N_t$ values for p-MOS are more dispersed as the LF noise level is, Fig. 3.18. The overall conclusion from this graph is that wf #18 in both cases presents the worst values in volumetric trap density and in noise level considering that the transconductance to drain current ratio and the oxide thickness remains constant for all the splits.

Fig. 3.18: Normalized drain current noise versus drain current for n-MOS (A) and for p-MOS (B) for all the JRG wafers.

Fig. 3.19: Transconductance to drain current ratio of the front interface versus drain current for n-MOS (A) and for p-MOS (B) for all the JRG wafers.
Fig. 3.20: Volumetric trap density versus measured wafer JRG for n- (A) and for p-MOS (B), respectively.

In Fig. 3.21, we plot the standard deviation of the logarithm of the normalized drain current noise and the standard deviation of $\Delta V_{th}$ as a function of the inverse square root of the area for n- (A)-(C) and p- (B)-(D) MOS devices from the measured splits and the results from the CPK wafer. From the results of the volumetric trap density, we expected the LFN variability behavior of wf #18 to be different from all the others since its $N_t$ values were higher than the others. However, the $N_t$ values are not the only factor that affects the LFN variability behavior as we already have seen earlier in this Chapter. From Fig. 3.21, it can be concluded that the LFN variability, indeed follows the LFN behavior and the trend of the static parameter mismatch, (C)–(D) for n- and p-MOS devices, showing the worst result for the wf #18 while all the others splits behave quite similarly. The results for CPK are almost the same as the reference wafer #09 which indicates that the GP do not influence the LFN variability.

In addition, we can conclude from the above analysis that the different architecture splits measured does not affect the LFN variability behavior of the devices. The causes of LFN variability as they have been presented through the RTS and CNF/CMF noise phenomena seems that they are the main factors that explains the LFN variability behavior of the devices. Thus, the changes introduced in these splits such as the GP introduction to adjust the threshold voltage and the no BOX wafer analyzed do not influence the LFN variability. Thereafter, we have to take into account all these findings from the above investigation when we are going to propose the LFN variability model.
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

Fig. 3.21: Comparison of the standard deviation of the logarithm of the normalized drain current noise as a function of the inverse square root of the area between the different splits of lot JRG for n- (A) and p- (B) MOS devices, respectively and for a fixed normalized drain current \( L/W*I_d = 10 \text{nA} \). In (C)–(D) comparison of standard deviation of \( \Delta V_{th} \) as a function of the inverse square root of the device area between the same devices.

As mentioned in the introduction, the last analysis for the 28nm FD-SOI technology node concerns the effect of the back gate bias on the LFN variability. The measured devices have very similar structure with split JRG \( \text{wf#09} \).

First, we have investigated the static parameters such as the drain current dependence versus front and back gate voltage polarizations and the transconductance to drain current ratio of the two interfaces versus back gate polarization. Afterwards, the LFN variability measurements were performed and a comparison with the simulated data carried out in order to verify which simulation model best describes the experimental results. The LFN variability in FD-SOI included measurements of n- and p-MOS devices for back gate bias \( V_b = 0 \text{V} \) and only n-MOS for back gate bias of \( V_b = \pm 10 \text{V} \). In addition, the measurements for back gate bias of \( V_b = \pm 10 \text{V} \) do not include results from below to above threshold voltage polarization.
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

Fig. 3.22: Static characteristics for n-MOS FD-SOI device from the 28nm CMOS technology node with (W/L)=1/0.03μm. In (A) is plotted the drain current versus gate voltage for different back gate biases, in (B) the drain current versus back gate voltage for different front gate polarizations and in (C)–(D) the square of the transconductance to drain current ratio for front and back interface, respectively.

In Fig. 3.22, we plot the static characteristics of an n-MOS FD-SOI device from the 28nm CMOS technology node with (W/L)=1/0.03μm for various front and back gate polarizations. It can be seen from Figs. 3.22 (A)-(B), the change of the threshold voltage of the device for different back gate polarizations, negative and positive. The \( \frac{g_m}{I_d} \) of the front, Fig. 3.22 (C), do not change with the back gate polarization. The \( \frac{g_m}{I_d} \) of the back, Fig. 3.22 (D), is enhanced by one decade going from negative to positive back gate bias. The reason why we investigate the transconductance to drain current noise ratio for the two interfaces is because from the above discussion these quantities influence significantly the LFN variability behavior of MOSFET.

In Fig. 3.23, we plot the dispersion of the normalized drain current noise at the fixed frequency of 10Hz versus device area for back gate polarization \( V_b=0 \)V and front gate, from
below to above threshold n- and p-MOS devices from the 28nm FD-SOI CMOS technology node. In Figs. 3.23 (A) and (C), it can be seen the difference in median noise level for n-MOS devices when the front gate bias changes from below to above threshold and the normalized drain current from around 10nA to 10μA. The median noise level is enhanced almost by one decade from sub-threshold to above threshold region of operation. The same behavior observed for p-MOS devices, Figs. 3.23 (B) and (D). In addition, the noise dispersion values show similar behavior for the two types, n- and p-MOS devices for both regions of operation.

![Fig. 3.23: The dispersion of the normalized drain current noise for a fixed frequency 10Hz versus the device area for back gate polarization V_b=0V and front gate bias below, V_g=0.2V, threshold for n- and p-MOS from the 28nm FD-SOI CMOS technology node (A-B) and above, V_g=0.8V, threshold in (C-D), respectively. The normalized drain current was for below threshold front gate bias around 10nA and for above threshold around 10μA.](image)

In Fig. 3.24, we plot the experimental results of the dispersion of the normalized drain current noise versus area for n-MOS devices from the 28nm FD-SOI CMOS technology node for back gate polarization of V_b=-10V (A) and V_b=+10V(B), respectively. As can be seen from Fig. 3.24, the dispersion level is almost the same for the two cases. In contrary, the
median noise level is enhanced by almost three decades going from $V_b=10\text{V}$ to $V_b=-10\text{V}$ back gate polarization.

![Fig. 3.24](A) ![Fig. 3.24](B)

Fig. 3.24: The dispersion of the normalized drain current noise for a fixed frequency 10Hz versus the device area for back gate polarization $V_b=\pm 10\text{V}$ for n-MOS from the 28nm FD-SOI CMOS technology node (A-B), respectively. The normalized drain current was for $V_b=-10\text{V}$ back gate bias around 10nA and for $V_b=+10\text{V}$ back gate bias around 10μA.

In Fig. 3.25, we plot the standard deviation of the normalized drain current noise versus the inverse of the square root of the device area for n- (A) and p- (B) MOS devices from the 28nm FD-SOI CMOS technology node for back gate polarizations $V_b=0$ and $V_b=\pm 10\text{V}$ and front gate from below to above threshold for n-MOS and for $V_b=0\text{V}$ and two front gate biases for p-MOS devices. The conclusion from these figures is that the standard deviation for all the biases and types of transistors remains almost unchanged.

![Fig. 3.25](A) ![Fig. 3.25](B)

Fig. 3.25: Standard deviation of the logarithm of the normalized drain current noise versus the inverse of the square root of area for n- (A) and p- (B) MOS devices from the 28nm FD-SOI technology node. The results for n-MOS includes back gate polarizations $V_b=0$, +10 and -10V and for $V_b=0\text{V}$ front gate polarizations from below to above threshold. In contrary, the p-MOS devices was investigated only for $V_b=0\text{V}$ and front gate bias from below to above threshold.
From Figs. 3.23-3.25 it can be concluded that the LFN variability behavior of FD-SOI technology node is not much different from their bulk ancestor. First, for back gate polarization grounded it seems that there is a difference when we investigate the median noise level behavior below and above threshold. However, this result is expected since from Chapter 2 we verified that in the strong inversion region of operation the correlated mobility factor is strong. This change in median noise level does not affect the variability behavior of the devices, since in Fig. 3.25 we showed that the standard deviation values for all the polarizations conditions remains the same. The difference in the variability behavior for FD-SOI devices revealed from the results of Fig. 3.24 for back gate polarization $V_b=±10V$. The median noise level appeared in Fig. 3.24 cannot be interpreted from the changes only of the static parameter, Fig. 3.22 (C) and (D). The second interface plays an additional role to the overall LFN variability behavior of the devices. The experimental results for different back gate polarization led us to the introduction of an LFN variability model that takes into account the second interface of FD-SOI devices as well as the correlated mobility fluctuations from the two interfaces.

### 3.5 Experimental of the LFN variability in bulk n- and p-MOSFETs of different technology nodes

In chapter 2, we presented an extensive investigation of the LFN behavior of n- and p-MOS transistors from different technology nodes manufactured in STMicroelectronics@Crolles the last 20 years. We extended this analysis for the first time in the LFN variability characterization of the last five bulk CMOS technology nodes. The aim of this work was to investigate the behavior of the LFN variability versus the downsizing of the gate oxide thickness and the different technology process steps. For the later, we studied the effect of the technology process for devices with the same gate oxide thickness but from different technology nodes or from devices of the same node but with different gate oxide thickness. The technology nodes investigated were the 0.12μm, 90nm, 65nm, 45nm and 28nm CMOS bulk. The devices measured were the standard n- and p-MOS from each technology node and in addition some special devices with thicker oxide thickness designated for different applications. The specific features of each technology process are already analyzed in Chapter 2, paragraph 2.6.

The standard deviation of the normalized drain current noise follows a scaling law as a function of the inverse square root of the device area, Fig. 3.26. The LFN variability behavior is better for devices with thinner gate oxide thickness and larger $N_i$ values but at the same
time it shows some irregularities when devices of the same technology node but different oxide thickness are compared. For example, in 28nm technology node we measured an n-MOS device with $t_{ox}=14\text{Å}$ and one with $t_{ox}=34\text{Å}$. It can be seen from Fig. 3.26 (A) that the LFN variability for the two devices is the same eventhough the equivalent oxide thickness is much different indicating the impact of the process on the LFN variability behavior of the transistor. The same trend is observed for p-MOS devices from the same technology nodes, Fig. 3.26 (B). Another example of this trend is the device with gate oxide thicker than that of the 65nm node, $C065nm_{150}\text{Å}$, without showing higher values of standard deviation for p-MOS transistors, as expected due to the lower value of oxide capacitance. In contrary, the results show that the worst case behavior was from the oldest technology node and in particular from 0.12μm technology node. This trend is not applied for n-MOS where the devices, except the one from 28nm technology node, seem to follow the trend with the gate oxide thickness.

A conclusion obtained from Fig. 3.26 is that the 28nm technology node shows better control of LFN variability compared to previous ones. In addition, the LFN variability is enhanced as the gate oxide thickness is augmented, the area of the device is diminished and the $N_t$ is increased. It can also be noted that the LFN variability for p-MOS transistors were better controlled compared to n-MOS for older technology nodes. This tendency is lost for the newer technology nodes of 45 and 28nm. Nevertheless, we have to take into account the process characteristics of each technology node for the characterization of LFN variability.

Fig. 3.26: Comparison of the logarithm of the normalized standard deviation of the drain current noise as a function of the inverse square root of the area between 28nm, 45nm, 65nm, 90nm and 0.12μm CMOS bulk technologies for (A) n- and (B) p- MOS devices, respectively for a fixed normalized drain current $L/W*I_d\approx10\text{nA}$ and a fixed frequency of 10Hz.
It should also be noted that such a strong reduction of LFN variability is well correlated to the diminution of the static parameter variability (mismatch of threshold voltage $V_{th}$) as shown in Fig. 3.27 for n-MOS and p-MOS devices from 28nm, 45nm, 65nm, 90nm and 0.12μm node technologies. Those improvements in LFN variability and static $V_{th}$ mismatch can be attributed to the increase of gate oxide capacitance following the technology down scaling (EOT reduction), which, in both cases, strongly attenuate the impact of oxide charge or depletion charge fluctuations in flat band and threshold voltage variations. It is noted that the two phenomena, matching and LFN variability, have different origin and the only resemblance is their dependence on the gate oxide capacitance.

Fig. 3.27: Comparison of standard deviation of $\Delta V_{th}$ extracted from $A_{\Delta V_{th}}$ of the minimum gate length transistor as a function of the inverse square root of the device area between 28nm, 40nm, 65nm, 90nm and 0.12μm CMOS bulk technologies for (A) n- and (B) p- MOS devices.

Finally, a comparison of the new technology node introduced side by side with the 28nm bulk CMOS was made. In Fig. 3.28, we present the comparison of the latest devices from the 28nm CMOS FD-SOI and bulk technology node. It can be concluded that the LFN variability is better controlled in FD-SOI technology for both n- and p- MOS devices. This result it could be an extra advantage of the FD-SOI technology node compared to the bulk one and it could be attributed to the better control of the channel that FD-SOI technology provides.

In view of the results of LFN variability from the last five CMOS bulk technology nodes, an overall conclusion is the impact of the oxide thickness and the volumetric trap density. There are others parameters that influence the LFN variability, but these factors seem to play the most important role to the phenomenon. Finally, the process can restrain the LFN variability, as we have seen for different technologies having the same oxide thickness.
3.6 Development of LFN variability model

Below we present the development of the LFN variability in two parts, first with the bulk and then with the FD-SOI devices.

3.6.1 Bulk transistors

As can be seen from Figs. 3.29 (A) and (C), in both n- and p-MOS devices, for large area devices the sample-to-sample noise level dispersion is found to be much smaller than one order of magnitude, while for small area devices a huge noise level dispersion is noticed. In addition, the median value of the normalized noise level in log scale, black straight line in Fig. 3.29, is relatively constant with the area for all devices, indicating no specific short/narrow channel effects. It should be mentioned that the noise level variation from device-to-device cannot be interpreted by the variation of the static device parameters. Indeed, the \((g_m/I_d)^2\) was plotted in Fig. 3.29 (B) and (D) for n- and p- MOS devices, respectively and found to vary by less than 20-30% from sample-to-sample and from large to small area.
Fig. 3.29: Normalized drain current noise at a fixed frequency of 10Hz, (A) and (B), and square root of the ratio of the transconductance to drain current, (C) and (D), versus area for n- and p-MOS devices, respectively. For at least 45 dies measured and L/W*I_d=10nA. In (A) and (C) the median black line is the median value of the normalized drain current noise PSD.

The Monte-Carlo theoretical model used to simulate LFN variability from device-to-device is based on the superposition of many RTS fluctuators according to Eq. 3.4. In this model, Poisson distributed numbers of traps are randomly generated in the gate dielectric with a uniform distribution in energy and space for each device [75-77]:

\[
\frac{S_{ld}}{I_d^2} = \frac{q^2}{(WLCS_{ox})^2} \cdot \left( \frac{g_m}{I_d} \right)^2 \cdot \sum_{k=1}^{N_{tot}} \left[ 4A_k \cdot \frac{\tau_k}{1+\omega^2\tau_k^2} \cdot Amp_k^2 \right]
\]  

(3.4)

where \(N_{tot}\) is the random number of traps in the gate oxide for the energy range swept by the Fermi level, which obeys a Poisson distribution with average value \(<N_{tot}>=W.L.t_{ox}.N_t.\Delta E_f\). \(N_t\) is the oxide trap volume density and \(\Delta E_f\) the Fermi level excursion. \(\tau_k\) refers to the effective time constant of the kth trap and is expressed as a function of capture and emission time as \(1/\tau_k = 1/\tau_c + 1/\tau_e\). \(A_k = (\tau_k/(\tau_c + \tau_e) = f_k.(1-f_k)\) is a weighting factor related to the space-mark ratio of each RTS, \(f_k\) is the trap occupancy factor \(f_k=1/\{1+\exp[(E_{ik}-E_f)/kT]\}\) with \(E_{ik}\) being
the kth trap energy and \( E_f \) the Fermi level position. Eq. (3.4) is simply the summation of the impact from many RTS fluctuators based on equation (3.1).

From equation 3.4, we can regenerate the normalized drain current noise PSD from the trapping of an elementary charge \( q \) in a region of the channel which changes the local conductivity, the first two terms in the equation 3.4, and the summation of all RTS fluctuators randomly generated into the gate-oxide interface. We are able by this way to calculate the drain current noise dispersion at a fixed frequency and the standard deviation of the logarithm of the normalized drain current noise of every measured device and thus fully analyze the LFN variability behavior. The experimental results presented in paragraphs 3.4.1 and 3.5 verify the validity of Eq. (3.4). Once again, we underline at this point that our model can explain the LFN variability behavior of a technology node from simple LFN full wafer measurements of different geometry devices, thus faster and much easier to analyze than RTS full wafer measurements. As we present in the experimental verification paragraph we studied the implementation of this model in the sub-threshold region because the standard deviation of the experimental data were constant for all gate bias from sub to above threshold regions. We have not taken into account at this stage the impact of the correlated mobility fluctuations in LFN variability.

We compared the experimental data obtained from the 28nm bulk CMOS technology node LVT n- and p- MOS devices with the simulation results produced from the Monte–Carlo simulation of Eq. 3.4 using the static and LFN parameters of Table 3.1. The parameters of Table 3.1 extracted from experimental measurements except the carrier concentration and the cross section of the traps. In Figs. 3.30 (A-B), we plot the experimental data and simulation results of the dispersion of the normalized drain current noise versus device area for n-MOS LVT transistors from the 28nm CMOS bulk technology node. As can be seen from Fig. 3.30, we were able to reconstruct the noise current dispersion of the experimental data using only four simulation parameters the volumetric trap density with the specific characteristics of each trap, the transconductance to drain current ratio, the amplitude modulation factor of each RTS and the equivalent oxide capacitance. The cross section \( \sigma \) and carrier concentration \( n_s \) values used in this simulation are the standard values from literature. Furthermore, the Monte-Carlo simulation using Eq. (3.4) was able to fit the measured standard deviation of the logarithm of the normalized drain current noise, Fig. 3.30 (C).
Table 3.1: Static and noise parameters for n-MOS from the 28nm CMOS technology node used for simulating the LFN variability.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Data</th>
<th>Simulation</th>
<th>Experiment</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N_t$ (eV/cm³)</td>
<td>1.00E+18</td>
<td>36</td>
<td>1.00E-17</td>
</tr>
<tr>
<td>$g_m$ (V)</td>
<td>2.00E+16</td>
<td>2,00E+16</td>
<td>1.00E+01</td>
</tr>
<tr>
<td>$n_s$ (cm⁻³)</td>
<td>0.2</td>
<td>0.2</td>
<td>0.2</td>
</tr>
<tr>
<td>$V_g$ (V)</td>
<td>14</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>$t_{ox}$ (Å)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Fig. 3.30: Normalized drain current noise at a fixed frequency of 10Hz versus area for n-MOS 28nm CMOS data (A) and simulation (B) for a fixed normalized drain current around 10nA, respectively. The black straight line is the median value. The standard deviation of the logarithm of the normalized drain current noise versus the inverse of the square root of area in lin-lin axis for n-MOS LVT 28nm CMOS devices data and simulation in (C).

Finally, in Fig. 3.31 we plot the evolution of the LFN variability versus the inverse square root of device area for the volumetric trap density in (A) and the oxide thickness in (B). All the other parameters used for simulation were constant in order to evaluate the impact only of $N_t$ and $t_{ox}$. It can be concluded from Fig. 3.31 (A) that the LFN variability is enhanced when the volumetric trap density is augmented, while the oxide thickness stays constant. The same tendency is observed for the oxide thickness, Fig. 3.31 (B). This behavior is in agreement with the experimental results of the historical evolution of LFN variability, Fig. 3.26.
findings show the validity of the developed model in a qualitative way, since they follow the trend of the experimental results.

Fig. 3.31: Standard deviation of the logarithm of the normalized drain current noise versus the inverse square root of device area for the volumetric trap density in (A) and the oxide thickness in (B). All the other parameters used for simulation kept constant.

3.6.2 FD-SOI transistors

The analysis of LFN variability in FD-SOI devices is a more complicated task compared to their bulk ancestors. In SOI instead of one interface, bulk devices, there are two interfaces, the so-called front and back, that can influence the noise behavior of the devices, Fig. 3.32. In FD-SOI technology, we have the impact of the back interface in the channel conductivity. The fluctuations in the current can be attributed to carriers interacting with the front and/or back interface traps. A detailed analysis of LFN behavior in 28nm FD-SOI technology node can be found in [82]. We developed a LFN variability model for FD-SOI devices that includes both interfaces and in addition, it takes into account the correlated mobility factor [82-83] which we believe plays a crucial role in these devices. It seems that the LFN is changing with the back gate polarization and we believe that this enhancement is caused from the correlated mobility fluctuations from the two interfaces. The impact of LFN variability should be investigated for different back gate biases in order to verify the impact of the back interface and the correlated mobility factors in LFN variability. We modify the classical bulk model by including all these additional factors step-by-step, starting with comparative analysis in the subthreshold and above threshold regions of operation for $V_{bs}=0$V and finally, we investigate the impact of back gate bias in the above model.
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

Fig. 3.32: Schematic representation of front and back interface in FD-SOI MOSFETs.

It is important at this point to underline that all the static parameters we used for SOI LFN variability simulation were calculated from the standard Poisson equation for SOI devices and are listed in Table 3.2 for various front gate voltages, drain voltage 50mV, back gate bias 0 and ±10V, respectively for n-MOS devices. We kept the volumetric trap density of the two interfaces, the cross section of the traps and the amplitude of the RTS constant for all the simulations, Table 3.3. The correlated mobility factor $\alpha_{1-2} \mu_{1-2}$ of the two interfaces was changed according to the different polarizations conditions. The value of $\alpha_{1-2}$ was taken from [82] for the front and back interface and the different back gate polarizations. The front equivalent oxide thickness was $t_{ox}=1.4\text{nm}$, the Si film thickness was $t_{si}=7\text{nm}$ and the back equivalent oxide thickness $t_{BOX}=25\text{nm}$.

Table 3.2: Static parameters for back gate bias 0 and ±10V extracted from drift-diffusion model. $n_{s1-2}$ are the carrier concentration of front and back interface, respectively.

<table>
<thead>
<tr>
<th>$V_g$(V)</th>
<th>$V_d$(V)</th>
<th>$N_{s1}$(eV/cm$^3$)</th>
<th>$N_{s2}$(eV/cm$^3$)</th>
<th>$\alpha_{s1} \mu_{s1}$</th>
<th>$\alpha_{s2} \mu_{s2}$</th>
<th>$\sigma_{1}$($\text{cm}^2$)</th>
<th>$\sigma_{2}$($\text{cm}^2$)</th>
<th>Amp$_1$</th>
<th>Amp$_2$</th>
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</thead>
<tbody>
<tr>
<td>0</td>
<td>0.2</td>
<td>9E+17</td>
<td>2E+17</td>
<td>2,E+06</td>
<td>4,E+05</td>
<td>4E-17</td>
<td>1E-17</td>
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<td>0.1</td>
</tr>
<tr>
<td>0</td>
<td>0.8</td>
<td>9E+17</td>
<td>2E+17</td>
<td>2,E+06</td>
<td>4,E+05</td>
<td>4E-17</td>
<td>1E-17</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>10</td>
<td>0.2</td>
<td>9E+17</td>
<td>2E+17</td>
<td>4,E+05</td>
<td>2,E+06</td>
<td>2E-06</td>
<td>1E-17</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>9E+17</td>
<td>2E+17</td>
<td>4,E+05</td>
<td>2,E+06</td>
<td>2E-06</td>
<td>1E-17</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>-10</td>
<td>0.7</td>
<td>9E+17</td>
<td>2E+17</td>
<td>2,E+06</td>
<td>4,E+05</td>
<td>1E-17</td>
<td>1E-17</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>-10</td>
<td>1.4</td>
<td>9E+17</td>
<td>2E+17</td>
<td>2,E+06</td>
<td>4,E+05</td>
<td>1E-17</td>
<td>1E-17</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

Table 3.3: Noise parameters for back gate bias 0 and ±10V and two front gate polarizations from below to above threshold from experimental results and [82]. The volumetric trap density for each interface was taken from [82]. $\sigma_{1-2}$ the cross section of the traps for front and back interface, Amp$_{1-2}$ is the amplitude modulation factor for each trap, respectively.
In Fig. 3.33, we plot the simulated results for the carrier concentration (A-B) and the transconductance to drain current ratio \(\frac{g_m}{I_d}\) (C) versus Si film thickness depth of the two interfaces for back gate \(V_b=0\) grounded and two front gate \(V_g\) voltages, below and above threshold, respectively. These static parameters are essential in order to perform the Monte Carlo simulations and calculate the time constant and the amplitude of each RTS fluctuator. It can be seen from Fig. 3.33 (A) that the carrier concentration for gate voltage polarization below threshold remains almost constant through all the Si film thickness. In contrary, the scene for strong inversion region is completely different, with carrier concentration values changing by almost two decades going from the front to the back interface limits. The ratio \(\frac{g_m}{I_d}\), Fig. 3.33 (C), is enhanced by a factor of 10 going from the front to the back interface through all drain current values, from linear to strong inversion region of operation.

In Fig. 3.34, we plot the simulated results for the carrier concentration (A-B) and the transconductance to drain current ratio \(\frac{g_m}{I_d}\) (C) versus Si film thickness depth of the two interfaces for back gate bias 10\(V\) \(V_b=10\) and two front gate \(V_g\) voltages, below and above threshold, respectively. It can be seen from Fig. 3.34 (A) that the carrier concentration for gate voltage polarization below threshold changes compared to the one with \(V_b=0\), the carrier concentration maximum is displaced to the back interface. For front gate polarization above threshold, Fig. 3.34 (B), the majority of carriers are at the front interface. The ratio of the \(\frac{g_m}{I_d}\), Fig. 3.34 (C), for the two interfaces is almost 10 going from the front to the back interface, as it was for back gate polarization 0\(V\) but with smaller absolute values.

Finally, in Fig. 3.35, we plot the carrier concentration and the \(\frac{g_m}{I_d}\) ratio of the two interfaces for \(V_b=-10\) and two gate voltages polarization 0.7 and 1.4\(V\) versus Si film thickness depth of the two interfaces. For gate voltage below threshold, 0.7\(V\), the carriers are displaced at the front interface and few of them gathered at the back one, Fig. 3.35 (A). The same results obtained for gate voltage above threshold, Fig. 3.35 (B), with different absolute values of carrier concentration. The \(\frac{g_m}{I_d}\) ratio, Fig. 3.35 (C), follows the same tendency as for \(V_b=0\) and 10\(V\), meaning that the front over back interface \(\frac{g_m}{I_d}\) ratio is around ten times higher.
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

Fig. 3.33: Simulation results of carrier concentration (A-B) and transconductance to drain current ratio (C) for back gate bias grounded and gate voltage 0.2V and 0.8V, respectively.

Fig. 3.34: Simulation results of carrier concentration (A-B) and transconductance to drain current ratio (C) for back gate bias 10V and gate voltage 0.2V and 1V, respectively.
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

Fig. 3.35: Simulation results of carrier concentration (A-B) and transconductance to drain current ratio (C) for back gate bias -10V and gate voltage 0.7V and 1.4V, respectively.

The investigation of the carrier concentration and the transconductance to drain current ratio of the two interfaces for different back and front gate polarizations revealed several issues. First, for back gate polarization $V_b=0V$ the simulation results showed that: (i) the carrier concentration for below threshold front gate polarization is almost the same at the two interfaces and the transconductance to drain current ratio is enhanced one decade going from the back to the front interface and (ii) for front gate bias above threshold the carrier concentration of the front interface is almost thirty times higher than the one of the back and the transconductance to drain current ratio has the same dependence between the two interfaces as for front gate bias below threshold voltage. For back gate polarization $V_b=10V$ the simulation results showed that (iii) for front gate bias below threshold $n_{s2}\approx 40n_{s1}$ while the transconductance to drain current ratio follows the same tendency as for $V_b=0V$ but with ten times smaller absolute values and (iv) for front gate bias above threshold, $n_{s2}\approx n_{s1}$ while the transconductance to drain current ratio follows the below threshold dependency. Finally, for back gate polarization $V_b=-10V$ the simulation results showed that (v) for front gate bias below threshold $n_{s1}\approx 10^{14}n_{s1}$, while the transconductance to drain current ratio follows the same tendency as for $V_b=0V$ with the same absolute values and (vi) for front gate bias above threshold $n_{s1}\approx 10^{14}n_{s1}$ but the absolute values are enhanced six decades compared the below
threshold voltage and the transconductance to drain current ratio follows the dependency and absolute values for \(V_b=0\) V.

The above findings of the static parameters playing an important role in LFN variability, suggest the need to modify the standard LFN variability model developed for bulk devices. Since the carrier concentration and the transconductance to drain current ratio is changing with different back gate bias, probably the LFN and LFN variability would be affected. We have to take into account the correlated mobility fluctuations in order to explain the median noise level change, which is observed with different back gate biases and inspect their impact in LFN variability behavior of FD-SOI devices. Using the static parameters from simulation results, Table 3.2, and the noise parameters from experimental results and [82], Table 3.3, we were able to study the impact of the developed model in the two regions of operation, from weak to strong inversion for various back gate polarizations.

The proposed LFN variability model considers the impact of the two interfaces on the overall LFN variability behavior of the FD-SOI devices. According to this model, the LFN variability is due to fluctuations induced from carriers interacting with both interfaces as well with correlated mobility fluctuations from the two interfaces. We assume that the two interfaces are uncorrelated. The drain current noise would originate from Eq. 3.4 with the addition of the second interface and the correlated mobility factor from each one according to the following formula:

\[
\frac{S_{i_d}}{I_d^2} = \frac{q^2}{(W.L.C_{ox,1})^2} \left( \frac{g_{m,1}}{I_d} \right)^2 \sum_{k=1}^{N_{tot,1}} 4A_{\kappa,1} \cdot \frac{\tau_{\kappa,1}}{1+\omega^2\tau_{\kappa,1}^2} \cdot \text{Amp}_{\kappa,1,1}^2 \cdot \left(1 + \alpha_{\kappa,1,1}C_{ox,1,1} \cdot \left\frac{I_d}{g_{m,1}} \right)^2 \right) + \frac{q^2}{(W.L.C_{ox,2})^2} \left( \frac{g_{m,2}}{I_d} \right)^2 \sum_{k=1}^{N_{tot,2}} 4A_{\kappa,2} \cdot \frac{\tau_{\kappa,2}}{1+\omega^2\tau_{\kappa,2}^2} \cdot \text{Amp}_{\kappa,2,1}^2 \cdot \left(1 + \alpha_{\kappa,2,1}C_{ox,2,1} \cdot \left\frac{I_d}{g_{m,2}} \right)^2 \right)
\]

where \(N_{tot,1,2}\) is the random number of traps in the gate and back oxide for the energy range swept by the Fermi level, \(C_{ox,1,2}\) are the equivalent oxide capacitances, \(g_{m,1,2}/I_d\) the transconductance to drain current ratio, \(\text{Amp}_{\kappa,1,2}\) the amplitude of the \(k\)-th RTS and \(\tau_{\kappa,1,2}\) the effective time constant of the \(k\)th trap of front and back oxide, \(\alpha_{\kappa,2,1}\) the product of the Coulomb scattering coefficient with the effective mobility for each interface, respectively. We investigate the developed model for different back gate bias \(V_b=0\) and \(\pm 10\) V.
3.6.2.1 FD-SOI transistors $V_b=0$V

Using the static and LFN parameters from Tables 3.2-3.3, we were able to compare the results of this model for front gate polarizations below and above threshold and back gate grounded, $V_b=0$V. The first comparison was to simulate the model without the correlated mobility factors from the two interfaces, CNF_1_2 version and the second was the complete model with the correlated mobility factors from the two interfaces, CNF_CMF_1_2 version for the different polarizations conditions, front and back gate biases. The two versions were distinguished by just putting the Coulomb scattering coefficient equal to zero for the CNF_1_2 version.

In Fig. 3.36, we plot the normalized drain current noise at 10Hz for back gate polarization $V_b=0$V and front gate below threshold for normalized drain current around 10nA for simulation model with and without correlated mobility fluctuations and experimental results. It can be concluded from Fig. 3.36 that the median noise level for the two simulated versions of Eq. (3.5) does not change and it is around the level we observed from experimental measurements, Fig. 3.36 (C). In addition, the noise level dispersion is the same for the two versions, Fig. 3.36 (D). This behavior was expected since we know that the correlated mobility factor influence the noise level in the above threshold voltage region of operation.
In Fig. 3.37, we plot the normalized drain current noise at 10Hz for back gate polarization $V_b=0V$ and front gate above threshold for normalized drain current around 10μA for simulation model with and without correlated mobility fluctuations and experimental results. It can be concluded from Fig. 3.37 that the median noise level for the two simulated versions is not exactly the same, but is enhanced for the CNF_CMF_1_2 version since in this region of operation the correlated mobility factor strongly influences the noise level of the device. The experimental results from Fig. 3.36 (C) show that the median noise level is much more close to the one predicted from CNF_CMF_1_2 version of Eq. 3.5. The standard deviation values show very close values for the two versions of the model.

![Fig. 3.37: Normalized drain current noise versus device area at f=10Hz for $V_b=0V$ and $V_g$ above threshold voltage for simulation versions of the model CNF_1_2 (A), CNF_CMF_1_2 (B) and experimental results in (C). Standard deviation of the logarithm of the normalized drain current noise versus the inverse square root of device area in (D).](image)

From Figs. 3.36-3.37 it can be concluded that the impact of the correlated mobility factors from the two interfaces introduced in Eq. (3.5) is higher for the above threshold voltage front gate polarization. Once more, we underline that this behavior was expected from the analysis of LFN in Chapter 2, where we verified that the mobility fluctuations factor is important in this region of operation. It seems that the correlated mobility factor influences only the
median noise level and not the LFN variability, as we already have seen in Bulk and FD-SOI devices where the standard deviation values remains constant for different gate voltage polarizations.

### 3.6.2.2 FD-SOI transistors $V_b=\pm 10V$

The analysis of LFN variability in FD-SOI devices for $V_b=0V$ showed that the correlated mobility factor is important in order to find the correct median noise level value, but it does not add any additional dispersion to the noise level. Thus, for $V_b=\pm 10V$ we will investigate the complete model with the correlated mobility fluctuations, version CNF_CMF_1_2.

In Fig. 3.38, we plot the normalized drain current noise at 10Hz for back gate polarization $V_b=-10V$ and front gate below threshold for normalized drain current around 10nA for simulation with and without correlated mobility fluctuations and experimental results in (A-B). In (C)-(D) we plot the same parameters but for $V_b=10V$ and front gate above threshold. It can be concluded from Fig. 3.38 that the median noise level from the experimental results are close to the simulated data for both cases.

![Fig. 3.38: Normalized drain current noise versus device area at f=10Hz for V_b=-10V and Vg below threshold voltage and V_b=10V and Vg above threshold voltage for simulation results in (A)-(C) and experimental data in (B)-(D), respectively.](image-url)
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

Finally, we present in Fig. 3.39 the standard deviation of the logarithm of the normalized drain current noise versus the inverse of the square root of device area for the discussed polarizations conditions for $V_b=\pm 10\text{V}$ for simulation results. The standard deviation values are the same for the two polarization conditions as is expected from the experimental results, Fig. 3.25.

From the above analysis, it is clear that the LFN variability behavior of FD-SOI technology node cannot be explained only from the addition of the second interface. We have to take into account the impact of the correlated mobility factor from the two interfaces, in order to correctly predict the median noise level of the devices. The experimental and simulation results revealed that the correlated mobility factor does not influence the LFN variability in terms of dispersion level. That was the reason for not including the correlated mobility factor in the standard Bulk model, since it does not change the LFN variability behavior of the devices but only corrects the median noise level for different front gate polarizations.

3.7 Conclusions

The low frequency noise variability was analyzed in detail in this Chapter. Initially, we tried to clarify the meaning of LFN variability in terms of its connection with a widely known phenomenon, the RTS noise. Then we continued with a representative example on how this phenomenon can become a major drawback in the functionality of digital circuits, as had been demonstrated in paragraph 3.2 Our approach to explain and model the LFN variability in CMOS bulk and FD-SOI technology nodes started from a model already known which describe the RTS noise. This model managed to explain and predict the LFN variability behavior of 28nm bulk CMOS devices accurately and in detail. We extended this model for
the FD-SOI technology node in order to take into account others parameters such as the correlated mobility factor and the impact of the second interface. We incorporated this idea in the standard bulk model and tried to understand how the second interface introduced in FD-SOI affects the LFN variability behavior of the transistors. We developed an LFN variability model which incorporates for the first time the impact of the correlated mobility fluctuations in LFN variability. The comparison between the simulation data and the experimental results showed that the role of correlated mobility fluctuations is important for the prediction of the median noise level but not for the LFN variability in terms of standard deviation values. The LFN variability seems to depend from the volumetric trap density, the characteristics of each trap, the oxide thickness and the transconductance to drain current ratio. Further analysis in this domain should be carried out in order to verify the validity of the simulation model for FD-SOI devices.

In addition, a thorough investigation of the LFN variability through CMOS bulk technology nodes has been done for the first time. The results reveal that the LFN variability shows better control for 28nm technology for both n- and p- MOS devices. For all the measured technologies, LFN variability is enhanced with the diminution of the device area, the equivalent oxide thickness and the increase of the volumetric trap density $N_t$. Furthermore, n- and p-MOS devices tends to have the same LFN variability behavior for the latest technology nodes which did not applied for the oldest where p-MOS devices control better LFN variability. This tendency is following the $N_t$ evolution with the equivalent oxide thickness found in Chapter 2. Interestingly, these results are well correlated to the diminution of the static parameter variability (mismatch of threshold voltage).
Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs

References


Chapter 3 – Low frequency noise variability in bulk and FD-SOI MOSFETs


Chapter 4: Low frequency noise in CMOS inverters

4.1 Background of CMOS inverters…………………………………… 121
4.2 Proposed LFN model in nanoscale bulk CMOS inverters…… 123
4.3 Experimental measurements in 40nm CMOS bulk inverters… 127
4.4 Model verification……………………………………………………... 128
4.5 Dynamic variability of CMOS inverters…………………………. 132
4.6 Conclusions…………………………………………………………….. 137
References………………………………………………………………. 139
Chapter 4

Low frequency noise in CMOS inverters

4.1 Background of CMOS inverters

A CMOS inverter circuit is shown in Fig. 4.1. It consists of two opposite types of transistor, n- and p- MOS, also known as complementary pair, the “C” at the beginning of the word CMOS, with their gates connected together at the input $V_{in}$. The inverter output voltage $V_{out}$ is taken from the common drain terminal of the pair. The inverter cell is the basis for CMOS logic circuits. The detailed analysis of its static and dynamic functionality is out of the purpose of this thesis. In contrary, some basic information about inverter’s operation would be of paramount importance in order to understand the LFN noise behavior of this basic standard cell.

![Fig. 4.1: A schematic diagram of the standard CMOS inverter cell with all the used terminals.](image)

In Fig. 4.2, we plot the most important DC characteristics of a CMOS inverter, the output versus input voltage $V_{out}-V_{in}$ curve known as Voltage Transfer Characteristic (VTC), the load current versus input voltage $I_{VDD}-V_{in}$ and the unity gain line $V_{out}=V_{in}$. The VTC which can decode the basic operation of the cell is divided in three regions noted on the graph by A, B and C. **Region A:** When the input voltage is at logic level “0” or just “low” and $V_{in}$ is smaller than the threshold voltage of n-MOS device then n-MOS is in cut-off region and it’s “OFF”
and the p-MOS is in triode region thus \( V_{\text{out}} \) is pulled at \( V_{\text{DD}} \) and \( I_{\text{VDD}} \) is low. **Region B:** When \( V_{\text{in}} \) is larger than the threshold voltage of the n-MOS, the situation is changing, n-MOS goes to saturation and p-MOS in triode region of operation, the \( I_{\text{VDD}} \) is starting raising till the moment that \( V_{\text{out}} = V_{\text{in}} = V_{\text{DD}}/2 \) and the two transistors are in saturation and then we have the maximum load current. At the same time the \( V_{\text{out}} \) is starting lowering via current through n-MOS. **Region C:** When \( V_{\text{in}} \) is smaller than \( V_{\text{DD}} - |V_{\text{th},p}| \) the n-MOS is in triode region the p-MOS in saturation, this is the region where \( I_{\text{VDD}} \) is starting to diminish and \( V_{\text{out}} \) reaching the “0” state. The final state where \( V_{\text{in}} \) is larger than \( V_{\text{DD}} - |V_{\text{th},p}| \) the n-MOS is in triode and the p-MOS is saturation the \( V_{\text{out}} \) is “0” and the \( I_{\text{VDD}} \) too.

![Fig. 4.2: An example of voltage transfer characteristic (blue line) \( V_{\text{out}} \) and load current \( I_{\text{VDD}} \) (red line) versus input voltage \( V_{\text{in}} \) of a CMOS inverter. The green line is the unity gain line \( V_{\text{out}} = V_{\text{in}} \).](image)

A very useful parameter of the CMOS inverter is the so-called midpoint or threshold voltage \( V_{M} \) which is defined by the point where the voltage transfer intersects the unity gain line. The circuit is designed in such a way so the midpoint voltage to be almost equal to \( V_{\text{DD}}/2 \). In general, the values of \( V_{\text{in}} \) inside region B of Fig. 4.2 are the most critical for the normal functionality of the circuit. Imagine a situation where the inverters midpoint is been displaced to larger or smaller values than the nominal one. Then the switching of the inverter from state “0N” to “OFF” is taking in place in a false input voltage. Thus, it can create serious problems to the functionality of the circuit.
4.2 Proposed LFN model in nanoscale bulk CMOS inverters

The CMOS inverter constitutes the basic element in digital VLSI circuits as logic NOT gate or in static random access memory (SRAM). With the scaling down of CMOS technologies, the operation of the CMOS inverter becomes more subjected to static and dynamic fluctuations due to device parameter variability as well as to low frequency (LF) and random telegraph noise (RTN), which scale as the inverse of the device area [85-89]. These huge fluctuations might jeopardize the CMOS inverter functioning and could reduce the static noise margin in SRAM cell [90].

In MOS devices, it is generally accepted that the LF noise originates either from carrier number fluctuations (CNF) or from Hooge mobility fluctuations (HMF), as we already analyzed in Chapter 2. In small area devices, RTN could even dominate giving rise to strong variability in LF noise in CMOS devices. In this chapter, we address for the first time the detailed characterization and modeling of the LF noise in a CMOS inverter, considered as a whole device. We will first develop a theoretical model for the LF noise in a CMOS inverter within the carrier number fluctuations scheme [90].

The load current $I_{VDD}$ conducted in the CMOS inverter, schematically represented in Fig. 4.1, can be obtained by equating the conservation of the drain currents of the p-MOS, $I_p$, and the n-MOS, $I_n$, transistors as,

$$I_{VDD}(V_{in}, V_{out}) = I_n(V_{in}, V_{out}) = I_p(V_{in}, V_{out}) \quad (4.1)$$

For each channel, the drain current can be calculated in the gradual channel approximation, using the common source voltage reference, as,

$$I_d(V_{gs}, V_{ds}) = \int_0^{V_{ds}} \frac{W}{L} \cdot \mu_{eff}(E_{eff}) \cdot Q_i(V_{gs}, U_c) dU_c \quad (4.2)$$

where $V_{gs}$ is the gate-to-source voltage, $V_{ds}$ is the drain-to-source voltage, $U_c$ is the quasi-Fermi level shift along the channel, $W$ is the channel width, $L$ the channel length, $\mu_{eff}$ the effective mobility depending on the effective electric field, $E_{eff} = (\eta Q_i + Q_d)/\varepsilon_{si}$ ($\eta \approx 0.5$ for electrons and $\eta \approx 0.33$ for holes) through the universal mobility law [91-92] ($Q_d$ being the depletion charge). The inversion charge $Q_i$ can be calculated using the Lambert W function (LW) approximation as [93],
where $\frac{kT}{q}$ is the thermal voltage, $V_{th}$ is the threshold voltage, $n$ is the subthreshold ideality factor, $n = \frac{C_{ox}}{(C_{ox} + C_d)}$, $C_{ox}$ is the gate oxide capacitance and $C_d$ the depletion capacitance.

Drain induced barrier lowering effect can be introduced in Eq. 4.3 by shifting $V_{th}$ of the amount $DIBL \times V_{ds}$, DIBL being in V/V.

According to Fig. 4.1, $V_{in} = V_{gs}$ and $V_{out} = V_{ds}$ for the nMOS, whereas $V_{in} = V_{DD} - V_{gs}$ and $V_{out} = V_{DD} - V_{ds}$ for the pMOS, $V_{DD}$ being the supply voltage. In Eq.4.2, $V_{th}$, $W$, $L$ and $\mu_{eff}(E_{eff})$ have to be particularized for each n- and p- MOS devices according to the design and technology parameters.

The calculation of the excess LF noise in a CMOS inverter can be carried out using two approaches: i) a circuit one considering the current noise elements in each transistors and appropriately combining them, and, ii) a global one considering the inverter as a whole device and evaluating the overall noise.

In the circuit approach, the load current noise (power spectral density) $S_{IVDD}$ is simply obtained by adding the drain current noise power spectral density of each transistor, supposed to be stochastically independent, such that,

$$S_{IVDD}(V_{in}, V_{out}) = S_{I_n}(V_{in}, V_{out}) + S_{I_p}(V_{in}, V_{out}) \quad (4.4)$$

The output voltage noise $S_{Vout}$ can be derived by adding the drain current noise divided by the square of the corresponding output conductance, $g_{dn} = \frac{\delta I_n}{\delta V_{out}}$ and $g_{dp} = \frac{\delta I_p}{\delta V_{out}}$, of each transistor such as,

$$S_{Vout}(V_{in}, V_{out}) = \frac{S_{I_n}(V_{in}, V_{out})}{g_{dn}(V_{in}, V_{out})^2} + \frac{S_{I_p}(V_{in}, V_{out})}{g_{dp}(V_{in}, V_{out})^2} \quad (4.5)$$

It should be noted that $S_{Vout}$ cannot be obtained by dividing the load current noise $S_{IVDD}$ by the square of the global inverter output conductance, $g_{out} = \frac{\delta I_{dd}}{\delta V_{out}}$, because $g_{out}$ cancels out when $I_{VDD}$ passes through a maximum and, by turn, would lead to unphysical result (see below).
In the global approach, one must specify the LF fluctuation sources in each transistor before proceeding to the overall LF noise calculation. In this context, we are considering here, that the LF noise in MOS transistor mainly stems from carrier number fluctuations (CNF) due to trapping-detrapping at the channel-gate dielectric interface. In this case, the CNF can be accounted for by considering the flat band voltage or equivalently the threshold voltage fluctuation concept. Therefore, the load current noise can be derived by adding the contribution of $I_{VDD}$ fluctuations due to independent $V_{th}$ fluctuations in n and p transistors such that,

$$S_{I_{VDD}}(V_{in}, V_{out}) = \left(\frac{\partial I_{VDD}}{\partial V_{tn}}\right)^2 \cdot S_{Vtn} + \left(\frac{\partial I_{VDD}}{\partial V_{tp}}\right)^2 \cdot S_{Vtp} \quad (4.6)$$

where $S_{Vtn,p}$ are the threshold voltage power spectral density of the n- and p- MOS transistors, given for flicker noise by Eq. (2.9).

Similarly, the output voltage noise can directly be obtained from the output voltage fluctuations as,

$$S_{V_{out}}(V_{in}, V_{out}) = \left(\frac{\partial V_{out}}{\partial V_{tn}}\right)^2 \cdot S_{Vtn} + \left(\frac{\partial V_{out}}{\partial V_{tp}}\right)^2 \cdot S_{Vtp} \quad (4.7)$$

Fig. 4.3 shows typical output voltage $V_{out}$, load current $I_{VDD}$ and dynamic conductance, $g_{dn}$, $g_{dp}$ and $g_{out}$, characteristics as a function of the input voltage $V_{in}$, obtained using the inverter model of Eqs. (4.1)-(4.3) with the parameters indicated in Fig. 4.3 caption. Note that, as expected, $I_{VDD}$ passes through a maximum and that, in contrast to $g_{dn}(V_{in})$ and $g_{dp}(V_{in})$, $g_{out}(V_{in})$ goes to zero, when $V_{out}=V_{DD}/2$.

Fig. 4.4 displays typical LF noise characteristics for the load current $S_{I_{VDD}}$ and the output voltage $S_{V_{out}}$, for a given frequency $f=10Hz$, as a function of input voltage $V_{in}$, obtained using the LF noise model of Eqs. (4.5)-(4.7). As expected, the load current noise follows the variation of $I_{VDD}$ with $V_{in}$, since the LF noise is nearly proportional to $I_{VDD}^2$, but not exactly (see below), and, so passes through a maximum versus $V_{in}$. The output voltage noise, $S_{V_{out}}$, calculated with both Eqs. (4.5) and (4.7) shows identical results, inferring the equivalence of those equations for $S_{V_{out}}$ LF noise evaluation. Moreover, $S_{V_{out}}$ exhibits a bell-shaped curve versus $V_{in}$ reaching a maximum when $V_{out}=V_{DD}/2$. The $S_{V_{out}}(V_{in})$ characteristic obtained wrongly using the output conductance from $S_{V_{out}}(V_{in})=S_{I_{VDD}}/g_{out}^2$, is also shown in Fig. 4.4(b) (dashed line), clearly demonstrating an infinite and unphysical singularity when $V_{out}=V_{DD}/2$. 

125
Chapter 4– Low frequency noise in CMOS inverters

Fig. 4.3: Typical a) $V_{\text{out}}(V_{\text{in}})$, b) $I_{\text{VDD}}(V_{\text{in}})$, and, c) $g_{\text{ds}}(V_{\text{in}})$, $g_{\text{dp}}(V_{\text{in}})$ and $g_{\text{out}}(V_{\text{in}})$ characteristics obtained with the inverter model of Eqs (4.1)-(4.3) with the parameters: $C_{\text{ox}}=1.8 \mu \text{F/cm}^2$, $n=1.7$, $W_n=3.24 \mu \text{m}$, $W_p=4.5 \mu \text{m}$, $L_n=L_p=40 \text{nm}$, $V_{\text{tn}}=V_{\text{tp}}=0.52 \text{V}$, $\mu_{\text{eff}}(V_{\text{gs}}=V_{\text{th}})=120 \text{cm}^2/\text{Vs}$, DIBL=120mV/\text{V}.

Fig. 4.4: Typical a) $S_{\text{IVDD}}(V_{\text{in}})$ and b) $S_{\text{Vout}}(V_{\text{in}})$ characteristics obtained with the inverter LF noise model of Eq. 4.5 (symbols) and Eq. 4.8 (solid line) with the same parameters of Fig. 4.3 and LF noise parameters: $N_{\text{in}}=2 \times 10^{17}/\text{eV/cm}^3$, $N_{\text{ip}}=10^{17}/\text{eV/cm}^3$, $\lambda_{\text{n}}=\lambda_{\text{p}}=0.1 \text{nm}$, $f=10\text{Hz}$.

An interesting plot when analyzing the LF noise in MOSFET is the normalized current noise, as a function of current in log-log scale. This is illustrated in Fig. 4.5 where $S_{\text{IVDD}}/I_{\text{VDD}}^2$...
is plotted versus $I_{VDD}$ with $V_{in}$ being the parametric variable. As can be seen, two branches appear which correspond to the dominance of the subthreshold region of each transistor in the inverter operation. This feature can be clarified by plotting the noise component of the n- and p- MOS devices given, in first approximation, by $(g_{mn}/I_n)^2 . S_{Vtn}$ and $(g_{mp}/I_p)^2 . S_{Vtp}$, respectively, where $g_{mn,p} . dI_{n,p}/dV_{in}$ stand for their transconductance. However, note that this approximation does not work perfectly at high load current values when both devices are in the on-state. It is also worth mentioning that these two branches could be merged only if the static and LF noise characteristics of n- and p- MOS devices would be identical, which is of course not the case in practice.

![Diagram](image)

Fig. 4.5: Typical variation of $S_{IVDD}/I_{VDD}^2$ with load current $I_{VDD}$ (solid line) and corresponding variations of $(g_{mn}/I_n)^2 . S_{Vtn}$ and $(g_{mp}/I_p)^2 . S_{Vtp}$ (dashed lines). Same parameter are used as in Fig. 4.4.

### 4.3 Experimental measurements in 45nm CMOS bulk inverters

Electrical and noise measurements were performed on two inverters using n- and p- MOS transistors issued from 45 nm bulk CMOS technology [94]. The gate stack consists of Poly/SiON for both transistors. The channel length (L) in both inverters for n- and p- MOS devices is 40nm. The channel width (W) is 4.5 and 0.45μm for p-MOS, 3.24 and 0.32μm for n-MOS. Static characterization was performed in order to obtain the output voltage $V_{out}$ and load current $I_{VDD}$ characteristics as a function of the input voltage $V_{in}$. In order to determine the load current sensitivity to the threshold voltage of each transistor we have changed the body bias $V_{PWELL}$ and $V_{NWELL}$ of the n- or p- MOS device in Fig. 4.1, respectively, and measured the corresponding $I_{VDD}(V_{in})$ curves.

LFN measurements were performed using the system described in paragraph 2.4. Load current and output voltage noise measurements of the inverters were carried out as a function
of the input voltage $V_{in}$. In addition, drain current noise measurements of individual n- and p-MOS transistors of the inverters were carried out as a function of the input voltage $V_{in}$ in order to calculate the gate dielectric trap density according to Eq. 2.9. Added system noise from LNA was subtracted from measured spectrum with software. The experimental bandwidth is 10 Hz up to 100 kHz.

4.4 Model verification

Fig. 4.6 shows representative spectra for the load current noise $S_{iVDD}$ measured at given DC load current $I_{VDD} \approx 5 \mu A$ on large and small width CMOS inverters. Except at high frequencies where the spectra are filtered by the current amplifier of the measurement system, they exhibit a global 1/f behavior.

Fig. 4.6: Typical spectra for the load current noise $S_{iVDD}$ obtained on CMOS inverters with parameters: $C_{ox}=1.8 \mu F/cm^2$, $n=1.7$, $W_n=3.24 \mu m$ or $0.32 \mu m$, $W_p=4.5 \mu m$ or $0.45 \mu m$, $L_n=L_p=40 nm$, $V_{tn} \approx V_{tp}=0.52 V$, $I_{VDD} \approx 5 \mu A$.

Fig. 4.7 shows typical $V_{out}(V_{in})$, $I_{VDD}(V_{in})$, and, $g_{dn}(V_{in})$, $g_{dp}(V_{in})$ and $g_{out}(V_{in})$ experimental characteristics obtained on a CMOS inverter with large width ($W_n=3.24 \mu m$ and $W_p=4.5 \mu m$). Note the overall good agreement with the modeling characteristics reported in Fig. 4.3 which have been obtained after proper calibration of drain current model of Eqs (4.2) and (4.3) on measured $I_d(V_{gs},V_{ds})$ curves taken on individual transistors. However, $g_{out}(V_{in})$ cannot be precisely described around $V_{DD}/2$ due to inaccurate determination of the experimental derivative.

Fig. 4.8 gives typical LF noise $S_{iVDD}(V_{in})$ and $S_{iVDD}/I_{VDD}^2(I_{VDD})$ experimental characteristics (symbols) taken at $f=10 Hz$ and obtained on the same type of CMOS inverter.
with large width ($W_n=3.24\ \mu m$ and $W_p=4.5\ \mu m$). Note also the very good overall consistency with the pure modeling results of Figs 4.4 and 4.5. In Fig. 4.8 (c) are also shown typical drain current noise $S_{\text{Id}}/I_d^2(I_d)$ characteristics measured directly on individual n-MOS transistors of the studied CMOS inverters. As can be seen, the $S_{\text{Id}}/I_d^2(I_d)$ characteristics match well with those of the load current noise (Fig. 4.8b) and are well interpreted by the carrier number fluctuations noise model used in Eqs. 4.6 and 2.9, despite some uncertainties in the experimental data. The trap densities used for the modeling are indicated in Fig. 4.8 caption and are close to those directly extracted from individual transistor measurements.

![Fig. 4.7: Typical a) $V_{\text{out}}(V_{\text{in}})$, b) $I_{V\text{DD}}(V_{\text{in}})$, and, c) $g_{\text{dn}}(V_{\text{in}})$ $g_{\text{dp}}(V_{\text{in}})$ and $g_{\text{out}}(V_{\text{in}})$ experimental characteristics obtained on a CMOS inverter with parameters: $C_{\text{ox}}=1.8\mu F/cm^2$, $n=1.7$, $W_n=3.24\mu m$, $W_p=4.5\mu m$, $L_n=L_p=40\text{nm}$, $V_{\text{in}}=V_{\text{tp}}=0.52V$, $\mu_{\text{eff}}(V_{g\text{s}}=V_{\text{th}})=120\text{cm}^2/\text{V.s}$, DIBL=120mV/V.](image-url)
Chapter 4– Low frequency noise in CMOS inverters

Fig. 4.8: Typical a) $S_{IVDD}(V_{in})$ and b) $S_{IVDD}/I_{VDD}^2(I_{VDD})$ experimental (symbols) and modeled (lines) characteristics obtained on a CMOS inverter with parameters: $C_{ox}=1.8\mu F/cm^2$, $n=1.7$, $W_n=3.24\mu m$, $W_p=4.5\mu m$, $L_n=L_p=40nm$, $V_{tn} \approx V_{tp}=0.52V$, $\mu_{eff}(V_{gs}=V_{th})=120cm^2/V_s$, DIBL=120mV/V. Fitting noise parameters: $N_{tn}=2\times10^{18}/eV/cm^3$, $N_{tp}=6\times10^{17}/eV/cm^3$, $\lambda_n=\lambda_p=0.1nm$, $f=10Hz$. c) Typical $S_{nd}/I_{d}^2(I_{d})$ characteristics from experiment (symbols) and theoretical (solid line) using CNF model as obtained on individual n-MOS transistor (same parameters as in a and b).

In order to achieve a direct modeling of the load current noise and infer the validity of Eq. 4.6, we have determined experimentally the load current sensitivity to the threshold voltage of each transistor, $\delta I_{VDD}/\delta V_{tn,p}$. To this end, we have changed the body bias $V_b$ of the n- or p-MOS device, respectively, and measured the corresponding $I_{VDD}(V_{in})$ curves as illustrated in Fig. 4.9(a). Then, taking into account the body factor $K_b$, measured separately on individual transistor, and, the $V_{th}$ shift, $\delta V_{tn,p}=-K_{bn,p}\delta V_b$, we have evaluated the $\delta \ln(I_{VDD})/\delta V_{tn,p}$ characteristics shown in Fig. 4.9(b). Finally, the modeled load current noise $S_{IVDD}(V_{in})$ and
$S_{VDD}/I_{VDD}^2(I_{VDD})$ characteristics have been calculated using Eq. 4.6 after tuning the $S_{Vtn}$ and $S_{Vtp}$ noise parameters (lines in Fig. 4.8), allowing by turn a very good fitting of the load current LF noise results to be achieved.

Fig. 4.9: a) Influence of body bias $V_b$ on $I_{VDD}(V_{in})$ characteristics: $V_b=0$ (symbols), $V_b=-0.1V$ on n-MOS (red line) and $V_b=-0.1V$ on pMOS (blue line). b) Sensitivity of load current, $\delta \ln(I_{dd})/\delta V_{tn,p}$, to body bias applied on n-MOS or p-MOS.

Similarly, the influence of the body bias of each transistor on the $V_{out}(V_{in})$ characteristics has been used to evaluate the sensitivity $\delta V_{out}/\delta V_{in,p}$ and, by turn, to calculate the $S_{Vout}(V_{in})$ noise characteristic using Eq. 4.8 with the same $S_{Vtn}$ and $S_{Vtp}$ noise parameters found for fitting the $S_{VDD}(V_{in})$ curves [symbols in Fig. 4.10(a)]. The modeling result given by Eq. 4.5 and drain current model of (4.2)-(4.3) is also shown in Fig. 4.10(a) (line). Note the very good agreement between the experimental and modeled results, emphasizing the overall consistency of the proposed inverter noise model.

In order to confirm the validity of this approach based on load current noise measurements, we have also directly measured the output voltage noise $S_{Vout}$ as a function of $V_{in}$ [see Fig. 4.10(b)]. As can be seen from Fig. 4.10(b), there is a good agreement between directly measured $S_{Vout}(V_{in})$ data and those deduced from load current noise measurements, which definitively infers the reliability of our procedure.
Chapter 4–Low frequency noise in CMOS inverters

4.5 Dynamic variability of CMOS inverters

Finally, we have investigated the impact of dynamic variability due to low frequency fluctuations on the dynamic operation of CMOS inverters. First, we explain the term of dynamic variability. Then we establish the experimental methodology to characterize the effect of dynamic variability in a CMOS inverter. Finally, we present typical results illustrating the impact on the inverter’s load current and, by turn, on the inverter’s output characteristics $V_{out}(V_{in})$.

The miniaturization of CMOS technologies leads to increasing variability of device parameters as we already developed in Chapter 3 of this thesis. Static variability in paired or close transistors is well known to limit the functionality of analog circuits [95], as well as the operation of logic circuits such as SRAM cells, by reducing their static noise margin (SNM) [96]. The static noise margin in SRAM cell is defined as the maximum tolerable DC noise voltage at a storage node that does not cause a read disturbance, and it is the length of the side of the largest square that can fit into the “eyes” of the butterfly curves, see Fig. 4.11. The scaling down of CMOS devices is also leading to a huge increase in low frequency noise (LFN) and random telegraph noise (RTN) due to the dynamic trapping–detrapping of carriers in the gate dielectric. These fluctuations result in a new source of time dependent parameter variation, called dynamic variability, which becomes nowadays a serious concern for static and dynamic SRAM cell functioning [90]. It is important to clarify at this point that for

Fig. 4.10: a) Typical experimental (symbols) and modeled (line) $S_{V_{out}}(V_{in})$ characteristics for a CMOS inverter with parameters: $C_{ox}=1.8\mu F/cm^2$, $n=1.7$, $W_n=3.24\mu m$, $W_p=4.5\mu m$, $L_n=L_p=40nm$, $f=10Hz$. b) Comparison between directly measured output voltage noise (symbols) and deduced from load current noise (line) for a CMOS inverter with parameters: $C_{ox}=1.8\mu F/cm^2$, $n=1.7$, $W_n=0.32\mu m$, $W_p=0.45\mu m$, $L_n=L_p=40nm$, $f=10Hz$. 

4.5 Dynamic variability of CMOS inverters

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dynamic variability, we have investigated the time dependent parameter variation of CMOS inverters, i.e. the LFN and RTS which are the only physical quantities of a MOSFET that are time dependent [97].

Fig. 4.11: a) SRAM Schematic diagram b) SNM definition graphical representation

Electrical measurements were performed on inverters (Fig. 4.12) using n- and p- MOS transistors issued from a 45nm bulk CMOS technology [94]. The gate stack consists of Poly/SiON for both transistors. The channel length (L) is 40nm for both n- and p- MOS devices. The channel width (W) is 4.5 and 3.24μm for p- and n- MOS, respectively. Dynamic measurements of the load current $I_{DD}(t)$ were performed as function of the input ramp voltage $V_{in}(t)$ with various rise times.

Fig. 4.12: Schematic of a CMOS inverter circuit with input voltage ramp $V_{in}(t)$.

For this purpose, we used the Agilent B1500 Semiconductor Device Analyzer with the embedded module B1530 Waveform Generator/Fast I-V measurement Unit. Load current measurements were preferred to $V_{out}(t)$ recording because of their better reliability at small
time constant. The input was biased with a ramp voltage $V_{in}(t)$ using the Agilent waveform generator B1530 (see Fig. 4.12), varying from 0 to the supply voltage $V_{DD}$ and for different ramp durations. The $V_{DD}$ was ranging from 0.8 to 1.3V with 1.1V being the nominal value for this technology node. The output of the waveform generator was connected to $V_{DD}$ in order to measure $I_{DD}$ vs time. The $N_{well}$ terminal of the p-MOS device was biased to $V_{DD}$ using the Agilent B1500 source monitor unit. The $P_{well}$ of the n-MOS device and source terminals were grounded. The $V_{out}$ terminal was left floating (no charge) [97].

In order to study the dynamic variability of the inverter response, we repeated several times (up to 50 sweeps) the $I_{DD}(t)$ measurements for different rise times of the input voltage $V_{in}(t)$, i.e. $t_r = 10\mu s$, 100$\mu$s and 1ms. Then, we extracted the input voltage value, $V_{incc}$ corresponding to a constant load current chosen at roughly half maximum load current of ascending edge (e.g. here $I_{cc}=50\mu A$ for $V_{DD}=1.1V$) for each sweep, allowing to evaluate the $V_{incc}$ statistical distribution and associated standard deviation for the 50 sweeps. It is emphasized at this point that we measured one single inverter 50 times and then treated the measured data. We have investigated the impact of different time sweeps on the load current characteristic of the inverter cell.

Figures 4.13(a) and 4.13(b) show typical dynamic $I_{DD}(V_{in})$ characteristics as obtained on an inverter subjected to 50 sweeps with ramp input voltage $V_{in}(t)$ having 10$\mu$s and 1ms rise times, respectively. A zoom of the 50 $I_{DD}(V_{in})$ curves around the $I_{cc}$ current range is displayed in Fig. 4.14 for three rise times. These figures clearly show that, for the shortest rise time ($t_r=10\mu$s), there exists a huge dynamic variability of the load current characteristics stemming from the low frequency noise (LF) inherent to the load current of the transistor’s inverter [90]. Indeed, for short rise time, the fast I-V measurements are strongly subjected to LF fluctuations with frequencies lower than the reciprocal rise time, resulting in significant current variations from sweep-to-sweep. In contrast, for larger rise times, the LF fluctuations in the $I_{DD}(t)$ signal are filtered at lower frequencies by a better time averaging process, yielding smaller sweep-to-sweep load current dispersions. This is also illustrated by the histograms of the constant current input voltage, $V_{incc}$, reported for various rise times and supply voltages in Fig. 4.15.
Fig. 4.13: Load current $I_{DD}$ versus input voltage $V_{in}$ after 50 sweeps for (a) 10$\mu$s and (b) 1ms rise time.

Fig. 4.14: Load current $I_{VDD}$ versus input voltage $V_{in}$ after 50 sweeps for various rise times $t_r$ ($V_{DD}=1.1V$).

Fig. 4.15: Histograms of constant current input voltage $V_{incc}$ for various rise times $t_r$ and supply voltages $V_{DD}$.

In order to quantify the dynamic variability, the standard deviation of the constant current voltage distribution, $\sigma_{Vincc}$, has been calculated for all the cases and is plotted as a function of rise time in Fig. 4.16. Indeed, $\sigma_{Vincc}$ decreases as the rise time increases due to a better filtering of LF noise impact, which results in a lower dynamic variability. It is also worth
Chapter 4– Low frequency noise in CMOS inverters

noting that $\sigma_{V_{incc}}$ is relatively independent of the supply voltage, even though the load current noise strongly depends on $V_{DD}$ [90]. This is because the load current variations have been translated into constant current input voltage fluctuations, which mainly reflect the LF noise in the transistor’s threshold voltages [90] and, therefore, are nearly independent of the load current level.

Fig. 4.16: Variation of dynamic standard deviation $\sigma_{V_{incc}}$ with rise time $t_r$ for various supply voltages $V_{DD}$.

Since, in a CMOS inverter the load current passes through a maximum around $V_{in}\approx V_{DD}/2$, the knowledge of the horizontal shift of the $I_{DD}(V_{in})$ curves detected by the $V_{incc}$ variation enables to predict the corresponding change in the output characteristics of the inverter $V_{out}(V_{in})$. To this end, it suffices to displace horizontally the $V_{out}(V_{in})$ curves with the same amount of $V_{incc}$ shift.

In Fig. 4.17, for the worst case scenario of $\pm 3\sigma_{V_{incc}}$ ($\sigma_{V_{incc}}\approx 15\text{mV}$), we have evaluated the impact of the dynamic variability on the inverter’s output characteristics for a 10µs rise time and the smallest cell geometry ($W=0.45-0.32\text{µm}$ and $L=0.04\text{µm}$), presenting the feature of 10 times more LF noise [90]. As can be seen from the figure, the output characteristic of the inverter is significantly disturbed by such a level of dynamic variability due to low frequency fluctuations, resulting in a huge SNM reduction of about 20%.
The impact of the low frequency fluctuations on the dynamic operation of CMOS inverters has been investigated. The experimental methodology to characterize such LF noise-induced dynamic variability has been based on fast I-V measurements of the load current characteristics, with applying a ramp input voltage $V_{in}(t)$. It has been found that, for small rise times, the load current characteristics $I_{DD}(V_{in})$ demonstrate a huge sweep-to-sweep dispersion inherent to the inverter transistors’ low frequency noise. The impact of such LF fluctuation-induced dynamic variability on the inverter’s output characteristics $V_{out}(V_{in})$ has been presented, yielding a 20% noise margin reduction for the smallest inverter cell, which could only aggravate for future CMOS technologies.

4.6 Conclusions

We have presented a detailed characterization and modeling of the low frequency noise characteristics of CMOS inverters. The LF noise model has been developed within the carrier number fluctuations scheme of MOS transistor excess noise using the concept of flat band voltage or threshold voltage power spectral density. It allowed us to describe accurately the load current and output voltage LF noise characteristics as a function of input voltage obtained on inverters from a 45nm bulk CMOS technology.

This LF noise modelling approach could constitute a useful tool for analyzing the impact of time domain fluctuations on the static and dynamic operation of CMOS inverters in VLSI.
circuits. In particular, it could be used for predicting the influence of dynamic fluctuations due to carrier trapping-detrapping on static noise margin and dynamic stability in SRAM cells.

The impact of the dynamic variability due to low frequency fluctuations on the operation of CMOS inverters, which constitute the basic component of SRAM cell, is investigated. The experimental methodology to characterize the effect of dynamic variability in a CMOS inverter is first established based on fast I-V measurements of the load current following the application of a ramp input voltage $V_{in}(t)$. It is shown that, for small ramp rise times, the load current characteristics $I_{DD}(V_{in})$ exhibit a huge sweep-to-sweep dispersion due to the low frequency noise. The impact of such dynamic variability sources on the inverter’s output characteristics $V_{out}(V_{in})$ is finally demonstrated, revealing a 20% noise margin reduction for the smallest inverter cell.
Chapter 4– Low frequency noise in CMOS inverters

References


Chapter 5: Summary and future work

5.1 Summary.................................................................142

5.2 Future work.............................................................144
Chapter 5: Summary and future work

5.1 Summary

In the present thesis, first we have investigated the LFN behavior of various CMOS bulk technologies from 0.25µm down to 28nm. In particular, we developed a new compact model for low frequency noise fluctuations based on the carrier number with correlated mobility fluctuations (CNF/CMF) model. Thus, we were able to calculate the drain current noise behavior of the measured devices using only two parameters, the flat band voltage power spectral $S_{Vfb}$ and the product of the Coulomb scattering coefficient with the effective mobility $\alpha_{sc} \cdot \mu_{eff}$ in all regions of operation, from linear to saturation. These parameters can be extracted from the slope (the factor $\alpha_{sc} \cdot \mu_{eff}$) and the intercept with the vertical axis (the parameter $S_{Vfb}$) of the plot $(S_{Vfb})^{1/2}$ versus $(I_d/g_m)$. We have demonstrated that this model is accurate and valid in the case of devices from the 28nm CMOS bulk technology node, n- and p-MOS as well. Thus, it could be used for modeling the LFN in circuit simulators.

On the other hand, we have characterized the LFN properties in the following CMOS bulk technology nodes manufactured in STMicroelectronics@Crolles the last 12 years: 0.25µm, 0.18 µm, 0.12 µm, 90 nm, 65nm, 45nm and 28nm. Thereafter, we were able to develop a figure showing the relation between the volumetric trap density and the equivalent oxide thickness of n- and p- MOS devices. These historical figures managed to clarify some aspects of LFN confused or not well understood in the scientific community. First, it has been shown that the LFN behavior of n- or p-MOS devices with different threshold voltages is not differentiated. The volumetric trap density of n-MOS devices is increased with the diminution of the equivalent oxide thickness and the increase of the volumetric trap density $N_t$. It become clear the impact of process characteristics on the LFN behavior of n-MOS devices. In addition, the results for p-MOS devices revealed very similar trends. The volumetric trap density of p-MOS devices is almost inversely proportional to $t_{ox}^{-2}$, indicating the strong effect of oxide thickness on the volumetric trap density, compared to the process factor which is dominant for n-MOS devices. Furthermore, the general circuit designers rule that the p-MOS devices are less noisy compared to the n-MOS is applied down to the 28nm technology node, where the two types of devices present the same volumetric trap density.

In the next step, the low frequency noise variability was investigated. A theoretical model has been developed to explain the LFN variability behavior of 28nm CMOS bulk technology node. The Monte-Carlo simulation model, used to simulate LFN variability in bulk devices is
based on the superposition of many RTS fluctuators according to Eq. 3.2, demonstrating that the LFN variability behavior can be reconstructed in devices from the 28nm CMOS bulk technology node. We used this model as a basis in order to characterize the LFN variability behavior of a new technology introduced in 28nm node, the FD-SOI. We implemented the impact of the second interface in the standard bulk approach. Based on the results from references [82-83] of Chapter 3, we introduced for the first time in the standard CNF/RTS LFN variability approach the correlated mobility factor. We simulated the different approaches, with and without the correlated mobility factor, and analyzed their behaviors for different front and back gate polarizations. We verified that the LFN variability behavior for FD-SOI devices does not change when different front gate biases below and above threshold are applied, at the same back gate polarization. The correlated mobility factor corrects the median noise level and not the noise dispersion. Such a result was expected, since the correlated mobility factor strongly affects the overall noise behavior of a device in the above threshold region of operation. In addition, the back gate polarization seems not to change the noise dispersion since it was found the same between back gate polarization 0 and ±10V. The comparison between simulation and experimental results demonstrated that the model including the correlated mobility factor of the front interface can better explain the LFN variability behavior of the devices.

An extensive analysis of the LFN variability through CMOS bulk technology nodes has been done for the first time. The LFN variability is improved with the reduction of the equivalent oxide capacitance and the increase of the volumetric trap density for both n- and p-MOS transistors. The impact of process in LFN variability was manifested for devices with the same equivalent oxide thickness but from different technology nodes that showed different LFN variability control. The results revealed that the LFN variability shows better control for 28nm technology for both n- and p- MOS devices. It should also be noted that such a strong reduction of LFN variability is well correlated to the diminution of the static parameter variability, mismatch of threshold voltage $V_{th}$ for the measured technologies. Those improvements in LFN variability and static $V_{th}$ mismatch can be attributed to the increase of gate oxide capacitance following the technology down scaling (EOT reduction), which, in both cases, strongly attenuate the impact of oxide charge or depletion charge fluctuations in flat band and threshold voltage variations.

In the final step, we studied the impact of the LFN and LFN variability on the functionality of a standard CMOS digital circuit, the CMOS inverter. First, we have presented a detailed characterization and modeling of the low frequency noise characteristics of CMOS inverters
manufactured from devices of the 45nm CMOS bulk technology node in STMicroelectronics@Crolles. The LFN model used to explain the noise behavior of the CMOS inverter was based on the carrier number fluctuations scheme of MOS transistor excess noise, using the concept of the flat band voltage or threshold voltage power spectral density. Thus, we were able to accurately describe the load current and output voltage low frequency noise characteristics as a function of input voltage obtained on inverters from 45nm bulk CMOS technology node.

The LF noise model developed to explain the LF noise characteristics of the inverters was used as step to characterize the LFN variability impact on this basic digital circuit. In other terms, we used the LF noise model to analyze the influence of time domain fluctuations on the static and dynamic operation of the standard cell. In particular, the impact of the dynamic variability due to low frequency fluctuations has been investigated. The experimental results demonstrated that for small ramp rise times of input voltage $V_{\text{in}}(t)$, the load current characteristics $I_{\text{DD}}(V_{\text{in}})$, exhibit a huge sweep-to-sweep dispersion due to the low frequency noise. The impact of such dynamic variability sources on the inverter’s output characteristics $V_{\text{out}}(V_{\text{in}})$ is finally demonstrated, revealing a 20% noise margin reduction for the smallest inverter cell.

### 5.2 Future work

Apart from the above studies performed within the frame of this thesis, there are open questions regarding the low frequency noise, the LFN variability and its impact on the functionality of circuits. Regarding the CNF/CMF approach, investigation is needed to clarify if the mobility factor is correlated or not with the carrier number. In the LFN variability research subject of FD-SOI devices, a full analysis is required to clarify the impact of each interface on the overall LFN variability behavior and develop a model explaining in detail the dispersion of noise level from device-to-device in this technology node. The LFN and LFN variability analysis should be carried out for the new technology nodes bulk (20nm) and FD-SOI (14nm) which are expected to introduce new process techniques, for example Gate last for the 20nm bulk CMOS technology node. In addition, we believe that the dynamic variability impact issue proposed through the LFN characterization of the CMOS inverters and the dynamic measurements can be expanded. The idea of dynamic characterization of the CMOS inverters can be done in the basic MOS transistors as well. In this way, we would be able to form a more solid opinion about the phenomenon of dynamic variability and it would be possible to develop a model explaining its behavior.
**Résumé**

D’une part, les fluctuations et le bruit basse fréquence (BF) dans les dispositifs MOS ont été le sujet de recherche intensive durant ces dernières années. Le bruit BF devient une inquiétude majeure pour la réduction continuelle de la dimension des transistors car le bruit 1/f augmente comme l’inverse de la surface des transistors. Le bruit BF et les fluctuations en excès pourraient constituer une limitation sérieuse du fonctionnement des circuits analogiques et numériques. Le bruit 1/f est également d’importance primordiale pour les applications de circuit RF où il provoque le bruit de phase dans les oscillateurs ou les multiplexeurs. Le développement des technologies submicroniques CMOS a conduit à l’observation d’un nouveau type de bruits, i.e. signaux télégraphiques aléatoires (RTS), entrainant de grandes amplitudes de fluctuations à l’heure actuelle, qui peuvent compromettre la fonctionnalité des circuits.

D’autre part, la variabilité statistique dans les caractéristiques de transistor est l’un des défis principaux pour les prochaines générations technologiques. La connaissance détaillée des sources de variabilité est extrêmement importante pour la conception et la fabrication des dispositifs résistants à la variabilité. Comme indiqué sur la Fig. 1, nous avons tracé le courant de drain en fonction de la tension de grille pour des dispositifs n-MOS plutôt petits de la technologie 28 nm. On constate que la dispersion des valeurs de courant de drain est presque deux décades. Cela résulte de l’impact des dopants aléatoires, de la rugosité de bord des lignes et les variations d'épaisseur d'oxyde, qui est plutôt bien compris, ainsi que du rôle du matériau de grille, en poly silicium ou en métal seulement, qui n’a été que récemment étudié dans les simulations. La confirmation et la quantification expérimentales de la contribution du bruit et des fluctuations BF manquent toujours. En outre, l'étude de la variabilité du bruit BF et de sa relation avec les autres facteurs des variations des dispositifs n'a été jamais effectuée. Sur la Fig. 2, nous montrons un exemple de l'impact de la variabilité de bruit BF en traçant la densité spectrale de puissance de bruit de drain avec la fréquence pour un dispositif n-MOS de grande et de petite surface (35 échantillons mesurées). On peut clairement voir que la dispersion de bruit est augmenté par 2 ou 3 décades allant de la grande à la petite surface. La Fig. 3 montre l'incidence prévue de la contribution liée au bruit de piégeage sur la réduction de $V_{dd}$ lors la conception de SRAM avec l'évolution technologique. De même qu’on a pu voir de la Fig. 3, l'impact de la variabilité due au bruit BF sur les cellules standards SRAM et DRAM pourrait être significatif pour les nouvelles technologies.
Fig. 1 : Variation du courant de drain avec la tension de grille pour des dispositifs n-MOS avec W/L=1/0.03μm pour une technologie CMOS bulk 28nm.

Fig. 2 : Variation du bruit du courant de drain avec la fréquence pour des dispositifs n-MOS avec une vaste surface à gauche et pour petite à droite.

Fig. 3 : Impact des non-idiéaltés (mesurés en termes de \(V_{\text{dd}}\)) sur les marges de conception des cellules SRAM pour différentes technologies CMOS soulignant le rôle croissant du bruit BF (RTN).

Par conséquent, les défis de recherches et les objectifs de cette thèse sont centrés vers les études des fluctuations basses fréquences et du bruit dans les technologies CMOS 32nm et au-delà. Plus spécifiquement, le bruit BF sera étudié avec trois objectifs : i) la caractérisation détaillée du bruit BF des nouvelles technologies CMOS comportant des grilles avec high-k/métal, des poches de canal etc., ii) le changement des paramètres de bruit BF des différentes
technologies et iii) l'impact du bruit BF et des fluctuations RTS en tant que sources de variabilité pour des applications de circuit analogique et numérique. Le premier objectif adressera l'origine des fluctuations de BF dans des dispositifs CMOS en termes de densité de piège et de localisation des défauts dans le diélectrique de grille et avec la longueur du canal pour différentes architectures (poché, canal de germanium, FD-SOI etc.). La deuxième partie considérera la variabilité du bruit BF résultant de la dispersion énorme des sources de bruit de dispositif à dispositif ; ceci sera conduit grâce à des mesures statistiques des caractéristiques de bruit de BF en fonction de la surface des dispositifs et des générations technologiques. Le troisième objectif se concentrera sur l'impact du bruit de BF ou des fluctuations RTS sur le fonctionnement des circuits élémentaires (inverseur, cellule SRAM) et considérés en tant que source temporelle de variabilité. Nous allons aborder ces trois questions une après l’autre dans les paragraphes suivants.

Nous allons adresser dans les détails les accomplissements de ce travail relatif au premier objectif mentionné au-dessus. Nous avons créé un modèle de bruit basse fréquence générique (modèle CNF/CMF) du transistor MOS basé sur une équation simple valable pour toutes les régions d'opération à savoir:

$$\sqrt{SV_g} = \sqrt{SV_{fb}} \cdot (1 + \Omega \cdot \frac{I_d}{g_m})$$  \(1\)

avec deux paramètres physiques, $\sqrt{SV_{fb}}$ qui est lié à la densité de piège d'oxyde en utilisant l’Eq. (2.9) et $\Omega=\alpha_{sc} \cdot \mu_{eff} \cdot C_{ox}$ qui est relié au coefficient coulombien de diffusion $\alpha_{sc}$, la mobilité effective $\mu_{eff}$ et la capacité $C_{ox}$ d'oxyde de grille. Les deux paramètres peuvent être extraits expérimentalement à partir du tracé $\sqrt{SV_g}$ versus $I_d/g_m$ dans les régions d'opération linéaires et/ou non linéaires. La connaissance de ces deux paramètres pour une technologie donnée fournit une description complète du bruit d’entrée de tension de grille avec les tensions de grille et de drain, et, par suite, du bruit BF de courant de drain $S_{I_d}$ pour toutes les conditions polarisées.

Il faut noter que, pour obtenir une valeur constante pour le produit $\alpha_{sc} \cdot \mu_{eff}$ en fonction de la tension de grille, cela signifie clairement que : (i) l'acceptation conventionnelle d'un $\alpha_{sc}$ constant dans le modèle CNF/CMF n'est pas appropriée, puisque dans ce cas $\alpha_{sc} \cdot \mu_{eff}$ devrait diminuer en inversion forte puisque $\mu_{eff}$ se dégrade en raison des collisions de surface, et (ii) la réduction du coefficient coulombien en inversion forte n’est également pas compatible à un produit constant de $\alpha_{sc} \cdot \mu_{eff}$. En revanche, ce comportement est accord physique avec les
résultats expérimentaux des travaux de Sun et Plummer rapportant un coefficient coulombien qui respecte une loi de mobilité de la forme :

\[
\mu_{\text{eff}} = \frac{\mu_{\text{eff},0}}{1 + \alpha_{\text{sc}} \mu_{\text{eff}} Q_1}.
\]

(2)

Au contraire, un coefficient coulomb conventionnel qui suivrait une loi de Matthiesen aurait comme conséquence un produit non constant de \(\alpha_{\text{sc}} \mu_{\text{eff}}\).

Le nouveau modèle du bruit BF proposé est vérifié par comparaison avec des résultats expérimentaux. Des mesures électriques ont été effectuées sur des transistors n- et p-MOS de la technologie CMOS 28nm. La grille se compose de TiN comme métallisation et du diélectrique à base de HfO\(_2\) pour oxyde de grille, avec une épaisseur équivalente d'oxyde (EOT) 1,4 et 1,7nm pour les transistors n- et p-MOS, respectivement. Pour les transistors n-MOS, il y a une couche de La entre le métal et l'oxyde high-k de grille et une couche d’oxyde interfacial entre l’oxyde high-k et le canal de grille. Pour les transistors p-MOS, il y a une autre couche d'Al qui n'existe pas dans l’empilement de grille du n-MOS. En outre, le canal entre les deux types de transistors n'est pas identique, parce que, pour les dispositifs n-MOS, le canal est purement du Si, mais, pour le p-MOS, il est en SiGe afin d’adapter le V\(_{\text{th}}\) et d'amplifier la mobilité. La longueur de canal (L) s'étage entre 0,03 et 1,803\(\mu\)m et la largeur de canal (W) est de 0,9\(\mu\)m. La caractérisation statique a été exécutée afin d'obtenir les caractéristiques de transfert (I\(_d\)-V\(_g\)) et de sortie (I\(_d\)-V\(_d\)) et pour extraire les paramètres nécessaires. Des mesures de bruit BF ont été effectuées utilisant le système de bruit décrit dans le paragraphe 2.4. La tension de drain a été fixée à V\(_d\)=±50mV pour des mesures dans la région linéaire et la tension de grille a été variée entre la faible à la forte inversion. Dans la région non linéaire, la tension de grille a été fixée au-dessous et au-dessus de la tension de seuil et la tension de drain a été variée de région linéaire à celle de saturation. Pour chaque géométrie, 10 échantillons ont été mesurés et la valeur moyenne pour chaque polarisation a été obtenue et analysée.

A. Région linéaire

Pour le modèle CNF/CMF, la densité spectrale de bruit de tension de grille est indiquée par l'éq. (1). Selon ces relations, on s'attend à ce que le tracé de \(\sqrt{S V_g}\) avec I\(_d\)/g\(_m\) soit linéaire. En fait, ceci est vérifié pour les canaux longs et courts et les p- et n- MOSFETs suivant les indications de la Fig. 4. Pour toutes les longueurs de canal mesurées, on observe des relations linéaires entre \(\sqrt{S V_g}\) et I\(_d\)/g\(_m\), indiquant clairement que le produit du coefficient de diffusion de Coulomb et de mobilité effective \(\alpha_{sc} \mu_{\text{eff}}\) des porteurs est constant dans la gamme de
tension de drain de la faible à la forte inversion, i.e. $\alpha_{sc}$ ne peut pas être considéré comme constante puisque $\mu_{eff}$ dépend de la tension de grille en raison de la diffusion sur les rugosités. L'analyse au-dessus est étendue dans la région non linéaire vérifiant la validité de notre nouveau modèle.

![Diagram](image)

**Fig. 4 :** Variation de $\sqrt{SV_g}$ en fonction de $I_d/g_m$ pour les transistors MOS à canal n (1, 2) et les transistors MOS à canal p (3-4), mesuré à $V_d = 50$mV et $f = 10$ Hz.

**B. Région non linéaire :**

L'analyse de la dépendance de $\sqrt{SV_g}$ avec $I_d/g_m$ a été étendue à toutes les régions de fonctionnement du transistor. Ceci est démontré sur les schémas 5 et 6 pour les transistors n- et p-MOS, respectivement et avec différentes longueurs de canal. Dans ces données, des familles des points de référence ont été obtenues pour différentes valeurs constantes de $V_g$ (au-dessous et au-dessus du seuil) et diverses tensions de drain (de la région linéaire à la saturation). De même, en région linéaire, on montre clairement que tous les points de référence se trouvent sur des lignes droites, démontrant que la dépendance de l'Eq. (1) avec $I_d/g_m$ s'applique également à la région non linéaire en variant $V_d$. Par conséquent, l'Eq. (1) peut être employée pour ajuster les données des schémas 5 et 6, fournissant deux paramètres, à savoir de l'interception sur l'axe des y, $\sqrt{S_{fb}}$, et de la pente $\alpha_{sc}\mu_{eff}C_{ox}\sqrt{S_{fb}}$, respectivement.

Nous présentons sur le schéma 7 les variations typiques de $\sqrt{SV_g}$ avec $I_d/g_m$ obtenues à partir de l'équation (1) en variant $V_d$ de 0 à 1V et pour différentes tensions de grille, tout en supposant un $\alpha_{sc}\mu_{eff}$ constant ($=2\times10^6$ cm$^2$/C) et $\sqrt{SV_{fb}} = 1.2\times10^5$V/$\sqrt{\text{Hz}}$. Notez les linéarités très bonnes des points de référence simulés, expliquant le comportement des données expérimentales des Figs. 5-6. La ligne continue sur le schéma 7 montre la droite obtenue en
Fig. 5 : Variations de $\sqrt{SV_g}$ en fonction de $Id/g_m$ pour des transistors MOS à canal n avec $W$ = 0,9$\mu$m et différentes longueurs de canal mesurés à $f$ = 10Hz et diverses tensions de drain de la région linéaire à la saturation (0-1V) et de la tension de grille au-dessous et au-dessus du seuil.

Fig. 6 : Variations de $\sqrt{SV_g}$ en fonction de $Id/g_m$ pour des transistors MOS à canal p avec $W$ = 0,9$\mu$m et différentes longueurs de canal mesurés à $f$ = 10Hz et diverses tensions de drain de la région linéaire à la saturation (0-1V) et de la tension de grille au-dessous et au-dessus du seuil.
utilisant l'équation (1) avec les mêmes paramètres, démontrant donc, la validité de l'équation (1) du point de vue de la modélisation.

Fig. 7 : Variations typiques de $\sqrt{SV_g}$ en fonction de $I_d/g_m$ obtenues à partir de l'équation (1) (symboles) quand $V_d$ variable de 0 à 1 V et pour différentes tensions de grille ($V_g=0,55-0,7-1,2$ V) pour un transistor avec $L=1,8\mu$m à $f=10$ Hz. La ligne continue montre la droite donnée par l'équation (1) avec les paramètres $\alpha_{sc} \mu_{eff} (=2\times10^6 \text{ cm}^2/\text{C})$ et $\sqrt{S_{\text{ph}}}=1.2\times10^5 \text{ V} / \sqrt{Hz}$.

**Comparaison du bruit BF dans les technologies CMOS bulk**

La deuxième étude a porté sur l'analyse du bruit BF dans les technologies CMOS Bulk fabriquées à STMicroelectronics ces 12 dernières années. Les résultats au-dessus peuvent être récapitulés en traçant la densité volumique de piége $N_t$ avec l'épaisseur équivalente d'oxyde des dispositifs étudiés n- et p- MOS pour avoir une idée de l'évolution du bruit BF pour presque toutes les technologies CMOS bulk. Le schéma 8 prouve que dans les dispositifs n- et p- MOS de la technologie 28nm le $N_t$ reste presque constant avec la longueur de canal $L$ pour toutes les variantes mesurées. Le $N_t$ reste également pratiquement inchangé avec la longueur de canal pour les technologies mesurées à l'exception du dispositif avec l'épaisseur d'oxyde différente, GO2. Les différents dispositifs des variantes mesurées pour cette technologie sont les suivants : RVT, dispositif avec une tension de seuil standard, LVT, dispositif avec une tension de seuil plus basse que le standard, SLVT, dispositif avec une tension de seuil beaucoup basse que le standard, HPA dispositif spécial pour les applications analogiques sans poche à l'intérieur du canal et finalement le dispositif avec une épaisseur d'oxyde différente, GO2. La motivation de l'étude était de tracer les valeurs de $N_t$ pour toutes les technologies en fonction de l'épaisseur équivalente d'oxyde afin d'analyser l'impact du $t_{ox}$ sur la densité volumique de piége. Il faut souligner que dans tous les cas la densité volumique de piége a été
calculée à partir de l'Eq. (3) en utilisant la densité spectrale de tension de bande plate extraite à partir des données expérimentales de $S_{d}/I_{d}$ avec $(g_{m}/I_{d})^2$ pour tous les dispositifs des technologies, utilisant le modèle CNF.

$$SV_{fb} = \frac{q^2 kT \lambda N_t}{W L C_{ox}^2 f}$$

(3)

où le $kT$ est l'énergie thermique, le $\lambda$ est la distance d'atténuation tunnel (~0.1nm), $N_t$ est la densité volumique de piège (/eV/cm$^3$) et $f$ est la fréquence.

**Fig. 8 :** Évolution du $N_t$ avec la longueur de canal pour tous les dispositifs mesurés n-MOS [A] et p-MOS [B] de la technologie 28nm CMOS bulk.

Le schéma 9 présente l'évolution du $N_t$, la densité volumique de piège, avec la réduction de l'épaisseur équivalente d'oxyde pour tous les dispositifs n-MOS. Ces données prouvent que $N_t$ tend à diminuer alors que l'épaisseur d'oxyde est augmentée. Cela indique que, pour les oxydes plus épais, le nombre de pièges près de l'interface de grille est réduit. Cependant, un examen plus soigneux des résultats de la Fig. 9 prouve que pour les diélectrique de grille de même épaisseur, la qualité diélectrique est différente dans les diverses technologies.

**Fig. 9 :** Évolution du $N_t$ avec la réduction de l'épaisseur équivalente d'oxyde pour tous les dispositifs n-MOS mesurés.
Par exemple, pour les technologies CMOS 90nm/GO2 et CMOS 65nm/GO2 avec tox=65Å, la densité volumique de piège change d’un facteur 5. Ceci peut mieux être compris en traçant dans la Fig. 10 la densité spectrale de bruit de courant de drain normalisée en fonction du courant de drain normalisé pour ces dispositifs. De ces données, il est clair que le niveau de bruit normalisé est différent dans ces dispositifs bien qu’ils aient la même épaisseur d'oxyde. L'impact des procédés technologiques est clairement indiqué dans cet exemple. Le schéma 11 présente un autre exemple de dispositifs avec une épaisseur d'oxyde de 120Å pour du CMOS 0.25µm/GO1 et de 150Å pour une technologie CMOS/65nm/HV. De ces données, il est clair que ces dispositifs, quoi qu’ils aient une épaisseur d'oxyde semblable, il existe une différence dans le niveau de bruit normalisée d’un ordre de grandeur expliquant la différence dans le $N_t$.

**Fig. 10 :** Bruit BF du courant de drain normalisé en fonction du courant de drain normalisé pour des n-MOS de technologies CMOS 90nm/GO2 et CMOS 65nm/GO2 avec (W/L) =1/1,2 -0,6/0,38µm, respectivement.

**Fig. 11 :** Bruit BF du courant de drain normalisé en fonction du courant de drain normalisé pour des n-MOS de technologies CMOS 0,25µm/GO1 et CMOS 65nm/HV avec (W/L) =10/0.45 -9/0,9µm, respectivement.

Dans la Fig. 12, nous présentons l'évolution de $N_t$ avec l'épaisseur équivalente d'oxyde pour tous les dispositifs p-MOS. Le graphique prouve qu'il y a une tendance à diminuer le $N_t$ à
mesure que l'épaisseur d'oxyde augmente selon une loi empirique de la forme $N_t \sim 1/t_{ox}^2$.

Cependant, il reste quelques cas qui ne suivent pas cette règle générale et ont besoin d'étude supplémentaire. À partir de l'introduction de la grille de high-k/métal dans la technologie 28nm, le graphique prouve qu'il y a une différence notable dans le niveau de $N_t$ entre le CMOS 45nm/GO1 et le CMOS 28nm/GO1 bien que l'épaisseur d'oxyde soit presque identique. La réponse peut être trouvée dans le Fig. 13 où nous traçons le bruit BF du courant de drain normalisée avec le courant de drain normalisé pour ces dispositifs. Du graphique, il est clair qu'il y a presque une décennie de différence de niveau de bruit médian entre les deux dispositifs, avec une valeur plus élevée pour la technologie 28nm. Ceci est prévu en raison de la grille différente utilisée dans la technologie 28nm, qui est aujourd'hui bien connue et qui est responsable des augmentations du niveau de bruit.

**Fig. 12** : Évolution de $N_t$ avec l'épaisseur équivalente d'oxyde pour tous les dispositifs p-MOS mesurés.

**Fig. 13** : Bruit BF du courant de drain normalisé avec le courant de drain normalisé pour des p-MOS du CMOS 45nm/GO1 et du CMOS 28nm/GO1 avec (W/L) =1/1,2 -0,6/0,38µm, respectivement.
Le schéma 14 présente un autre exemple des irrégularités en valeurs de $N_t$. Nous traçons le bruit de courant de drain normalisé avec le courant de drain normalisé pour les dispositifs des technologies CMOS 45nm/GO2 et CMOS 0,18μm/GO1 avec la même épaisseur d'oxyde et CMOS 28nm/GO2 avec une épaisseur d'oxyde légèrement plus haut. Cela montre que les dispositifs de la technologie 0,18μm et de 28nm ont le même niveau de bruit médian, mais une épaisseur d'oxyde différente, ce qui explique les différentes valeurs de $N_t$. Le dispositif de la technologie 45nm a un niveau de bruit plus faible de près d'une décennie, ce qui explique la valeur plus petite de $N_t$ dans fig. 11.

**Fig. 14 :** Bruit BF de courant de drain normalisé avec le courant de drain normalisé de p-MOS du CMOS 45nm/GO2, CMOS 0,18μm et du CMOS 28nm/GO2 avec (W/L) =9/0.634 - 10/0.18 – 4.5/0.915μm, respectivement.

En conclusion, dans Fig. 15 nous traçons l'évolution de $\alpha'=\alpha_{sc}.\mu_{eff}$ avec l'épaisseur équivalente d'oxyde pour tous les dispositifs mesurés. Le paramètre $\alpha'$ a été extrait à partir des données expérimentales de bruit utilisant le modèle CNF/CMF. Du graphique on peut clairement voir que pour les deux types de dispositifs, $\alpha'$ reste presque constant avec l'évolution de l'épaisseur équivalente d'oxyde. En outre, le paramètre $\alpha'$ est plus élevé dans les dispositifs p-MOS comme cela est expecté.

**Fig. 15 :** Variation de $\alpha'=\alpha_{sc}.\mu_{eff}$ avec l'épaisseur d'oxyde pour tous les dispositifs mesurés où le modèle CNF/CMF ajuste mieux les résultats expérimentaux.
De l'analyse au-dessus, il apparaît que l'étude du bruit BF dans les dispositifs CMOS est plus complexe que ce que l'on pourrait croire. Comme nous avons vu au travers des résultats obtenus sur toutes les technologies, le modèle compact que nous avons développé est applicable à la plupart des cas mais il reste quelques situations où le modèle ne fonctionne pas parfaitement. A ce stade, plusieurs questions demeurent : Quels sont les critères pour distinguer le modèle CNF du modèle étendu de CNF/CMF ? Pourquoi dans certains cas l'un ou l'autre modèle s'applique-t-il et pas dans tous les cas ? Quel est le phénomène physique qui distingue les deux modèles? Toutes ces questions doivent être répondues. Bien que nous ayons réalisé beaucoup d'études pour mieux comprendre ce sujet du bruit BF, il n'en reste pas moins que certains points restent encore incompris. Une idée originale serait de considérer que les deux termes dans le modèle de CNF/CMF ne soient pas corrélés. Cela signifierait que le phénomène physique est identique, mais que le piégeage/dépiégeage des porteurs dans l'oxyde affecterait de manière dé-corrélée le nombre de porteurs et le mécanisme de diffusion coulombien. Nous pensons que cette hypothèse est réaliste mais elle demande davantage d'étude afin d'être confirmée.

D'autre part, les données historiques décrivant la densité volumique de piège \( N_t \) pour les dispositifs n- et p-MOS, nous proposent quelques nouvelles pistes sur le sujet du bruit BF dans les transistors MOS. En effet, à partir de la Fig. 9 pour les dispositifs n-MOS, il est clair que pour ce type de dispositifs, les procédés technologiques affectent beaucoup plus les valeurs de \( N_t \). Nous ne pouvons en conclure aucune règle empirique reliant des valeurs de \( N_t \) au \( t_{ox} \). Les procédés technologiques jouent un rôle plus important que l'épaisseur équivalente d'oxyde contrairement à ce qui est généralement supposé. La situation est plus simple pour les dispositifs p-MOS selon les indications de la Fig. 12, où nous avons tracé le même graphique que pour les dispositifs n-MOS. L'impact de la technologie pour ce type de dispositifs est moindre par rapport au n-MOS. De la Fig. 12, nous pouvons conclure que le \( N_t \) est inversement proportionnel à \( t_{ox}^2 \). La règle générale des concepteurs de circuit selon laquelle les dispositifs p-MOS sont moins bruyants que le n-MOS était jusqu' à maintenant vraie. Cependant, pour la technologie 28nm, cette règle n'est plus valable, les dispositifs p-MOS sont plus bruyants que les n-MOS.

La deuxième partie de notre travail a considéré la variabilité du bruit BF résultant de la dispersion énorme des sources de bruit de dispositif à dispositif ; ceci sera effectué aux moyens de mesures statistiques des caractéristiques du bruit BF en fonction de la surface des dispositifs et des nœuds technologiques.
L'impact de la variabilité du bruit BF et en particulier du RTS sur les circuits numérique CMOS est bien connu de nos jours. Nous voudrions présenter ici l'impact que la variabilité du bruit BF peut avoir sur une cellule numérique standard comme la mémoire SRAM. Afin d’illustrer l'impact de la variabilité du bruit BF sur l'opération d’un circuit numérique, le caractèreistique papillon d’une cellule SRAM a été simulée avec les dispositifs nominaux de la technologie 28nm CMOS avec une densité de piège moyenne $N_{it}=10^{11}/cm^2$, Fig. 16. Puisque la cellule SRAM est utilisée à la haute fréquence, les fluctuations du bruit BF et RTS se comportent en tant qu'événements quasi-statiques, ayant pour résultat la dispersion de la tension de seuil d’un dispositif à un autre dispositif donné par l’Eq. 4.

\[
V_t = V_{t0} + \sum_{k=0}^{N_{it\text{tot}}} \frac{q\text{Amp}_k}{W.L.C_{ox}}
\]  

(4)

où $V_t$ et $V_{t0}$ sont la tension de seuil avant et après piégeage, $N_{it\text{tot}}$ est le nombre total de pièges donné selon une loi de Poisson, Amp $k$ est la modulation d'amplitude du RTS donnée par Amp$=10^a$ avec $a=0$ à 0,25 décrivant la distribution de $V_t$, W et L est la largeur et la longueur de canal et $C_{ox}$ la capacité équivalente d'oxyde.

De telles dispersions de $V_t$ sont presque gaussiennes avec une déviation standard $\sigma_{V_t}$ et provoquent une réduction énorme de la marge de bruit statique de la cellule quand un grand nombre statistique de transistors témoins (ici $4\times10^6$) sont simulés, Fig. 16. Il est clair de la fig. 16 que la différence dans la marge de bruit statique (SNM) de la tension de seuil maximale, moyenne et minimale simulée peut causer des dysfonctionnements de cette cellule de base.

Ensuite, nous allons présenter le modèle de variabilité de bruit BF que nous avons développé selon deux étapes, commençant par les dispositifs bulk et puis continuant avec les dispositifs FD-SOI.
**Transistors Bulk:**

Dans la Fig. 17 nous avons tracé le bruit de courant de drain normalisé pour une fréquence fixe de 10Hz avec la surface du dispositif. Comme on peut le voir sur la Fig. 17 (a) et (c) pour les dispositifs n- et p-MOS, respectivement, la dispersion du niveau de bruit BF médian d'échantillon à échantillon est trouvée plus petite d'un ordre de grandeur, alors que pour la plus petite géométrie, une dispersion énorme de niveau du bruit BF est notée. En outre, la valeur moyenne du niveau de bruit BF médian normalisé en échelle log, ligne droite noire dans la Fig. 17, est relativement constante avec la surface pour tous les dispositifs, n'indiquant pas d'effets de canal court. Il est à noter que la variation du niveau de bruit BF de dispositif à dispositif ne peut pas être interprétée par la variation des paramètres statiques des dispositifs. En effet, le \((g_{m}/I_d)^2\) a été tracé dans la Fig. 17 (b) et (d) pour des dispositifs n- et p- MOS, respectivement, et ne montre pas des variations supérieures à 20-30% d'un échantillon à l'autre et de la grande à la plus petite surface. Au contraire, la dispersion du niveau de bruit BF a été d'une manière satisfaisante comprise par la non-uniformité des distributions énergiques et spatiales des pièges dans l’oxyde. Un modèle dans lequel ce non uniformité est pris en considération sera discuté plus loin.

![Fig. 17](image)

Fig. 17 : Bruit de courant de drain normalisé à une fréquence fixe de 10Hz, (a) et (b), et carré du rapport entre la transconductance et le courant de drain, (c) et (d), en fonction de la surface pour les dispositifs n- et p-MOS, respectivement, pour au moins 45 échantillons mesurés et \((L/W)*I_d≈10nA\). En (a) et (c) la ligne noire est la valeur moyenne du bruit de courant de drain normalisé.
Le modèle Monte Carlo théorique employé pour simuler la variabilité du bruit BF de dispositif à dispositif est basé sur la superposition de beaucoup de fluctuateurs RTS selon l'Eq. 5. Dans ce modèle, le nombre de pièges distribué avec une loi de Poisson est aléatoirement généré dans le diélectrique de grille avec une distribution uniforme en énergie et dans l'espace pour chaque dispositif :

\[
\frac{S_{I_d}}{I_d^2} = \frac{q^2}{(W \cdot L \cdot C_{ox})^2} \cdot \left( \frac{g_m}{I_d} \right)^2 \cdot \sum_{k=1}^{N_{tot}} [4A_k \cdot \frac{\tau_k}{1+\omega^2 \cdot \tau_k^2} \cdot \text{Amp}_k^2]
\]  

(5)

où \(N_{tot}\) est le nombre total aléatoire de pièges dans l'oxyde de grille pour la gamme d'énergie balayée par niveau de Fermi, qui obéit à une loi de Poisson avec valeur moyenne \(\langle N_{tot}\rangle = W \cdot L \cdot C_{ox} \cdot N_t \cdot \Delta E_f\). Le \(N_t\) est la densité volumique de pièce d'oxyde et \(\Delta E_f\) l'excursion d'énergie autour du niveau Fermi. \(\tau_k\) est la constante de temps et est exprimée en fonction du temps de capture et d'émission comme \(1/\tau_k = 1/\tau_c + 1/\tau_e\). Les temps de capture et d'émission sont évalués selon la statistiques de Shockley-Read-Hall comme \(\tau_c = 1/(\sigma_c n_s \cdot v_{th})\) et \(\tau_e = 1/(\sigma_e n_1 \cdot v_{th})\) où le \(n_s\) est la concentration surfacique des porteurs, \(n_1\) est la concentration des porteurs quand \(E_f\) est égal au niveau de l'énergie du piège et \(\sigma\) est la section de capture du piège comportant un terme activé. \(\sigma_k = \sigma_s \cdot \exp(x_k/\lambda)\) où les \(\tau_s\) est la constante de surface, \(x_k\) est la distance du piège dans le diélectrique et \(\lambda\) est la distance d'atténuation tunnel. \(A_k = \tau_k/\tau_c\) est un facteur de pondération lié au rapport d'occupation de chaque RTS, \(f_k\) est le facteur d'occupation du piège \(f_k = 1/\{1+\exp[(E_k-E_f)/kT]\}\) avec \(E_k\) étant l'énergie de \(k\)th pièce et \(E_f\) la position du niveau de Fermi. L'amplitude du RTS du courant de drain peut être évaluée en considérant que le piègeage d'une charge élémentaire \(q\) dans une région du canal change la conductivité locale. On peut montrer ainsi que, dans une approximation d'ordre un, l'amplitude relative du RTS de courant de drain est donnée par :

\[
\frac{\Delta I_d}{I_d} = \frac{g_m}{I_d} \cdot \frac{q}{W \cdot L \cdot C_{ox}} \cdot \text{Amp}_k
\]

(6)

\(\text{Amp}_k\) est la variation aléatoire de l'amplitude de fluctuateurs de chaque RTS obéissant une loi exponentielle selon Takeuchi et al. Par conséquent, nous supposons ici que \(\text{Amp}=10^\alpha\) avec \(\alpha\) étant un nombre aléatoire choisi arbitrairement entre 0 et 0,25 pour chaque pièce.

A partir de l'équation 5, nous pouvons simuler le bruit du courant de drain normalisé dû au piégeage d'une charge élémentaire \(q\) dans une région du canal qui fait changer la conductivité locale, les deux premiers termes dans l'équation 5, et l'addition de tous les fluctuateurs de RTS aléatoirement produits à l'interface grille-oxyde. Nous pouvons de cette façon calculer la dispersion réelle du bruit de courant de drain normalisé à une fréquence fixe et le logarithme
du bruit du courant de drain normalisé pour chaque dispositif mesuré et analyser ainsi entièrement le comportement de la variabilité du bruit BF de chaque technologie. Ainsi, ce modèle permet d’expliquer le comportement de la variabilité du bruit BF mesurée sur des dispositifs de technologies différentes plus rapidement et plus facilement qu’avec des mesures de RTS. Nous allons présenter dans le paragraphe suivant la vérification expérimentale de cette étude dans la région au-dessus de la tension de seuil parce que la déviation standard du logarithme du bruit BF du courant de drain est constante pour toutes les polarisations de grille, au-dessous et au-dessus de la tension de seuil. Nous n'avons pas pris en compte à ce stade l'impact des fluctuations corrélées de mobilité sur la variabilité du bruit BF.

**Transistors FD-SOI:**

L'analyse de la variabilité du bruit BF dans les dispositifs FD-SOI est une tâche plus compliquée comparée à leurs ancêtres bulk. Dans le SOI, au lieu d'avoir une seule interface comme dans les dispositifs bulk, il y a deux interfaces actives, à l'avant et l’arrière, qui peuvent influencer le comportement du bruit BF dans les dispositifs, Fig. 18. Dans la technologie FD-SOI, nous pouvons avoir l'influence de l'interface arrière sur la conductivité du canal. Les fluctuations du courant de drain peuvent être attribuées soit aux porteurs interagissant avec les pièces de l'interface avant, soit avec ceux de l’interface arrière ou les deux à la fois. L'analyse détaillée du bruit BF de ces dispositifs n'est pas le but de cette thèse. Nous avons développé un modèle de variabilité du bruit BF pour les dispositifs FD-SOI qui inclut les deux interfaces et, en outre, il prend en considération le facteur corrélé de mobilité dont nous pensons qu'il joue un rôle essentiel dans ces dispositifs. L'impact de la variabilité du bruit BF devra être aussi bien étudié non seulement dans la région sous le seuil mais aussi dans l'inversion forte, où les fluctuations corrélées de mobilité sont importantes sur le niveau total de bruit. Enfin, l'effet de la polarisation arrière devra être pris en considération dans le comportement de la variabilité du bruit BF pour la technologie FD-SOI. Ainsi, l'analyse est divisée en 3 parties ; la première est l'introduction de la deuxième interface dans le modèle standard de variabilité du bruit BF. La deuxième concerne l'addition du facteur corrélé de mobilité que nous allons introduire pour la première fois dans le modèle classique de variabilité du bruit BF. La troisième partie traite de l'effet de la polarisation arrière. Nous allons présenter tous ces prolongements du modèle classique point par point dans ces différentes parties en commençant par faire une analyse comparative entre les régions sous la tension de seuil et en forte inversion et, en conclusion, nous étudierons l'impact de la polarisation arrière dans les modèles au-dessus.
Fig. 18 : Représentation schématique des deux interfaces dans les transistors FD-SOI.

L'étape finale, au sujet de l'étude de modélisation sur le comportement de la variabilité du bruit BF pour la technologie 28nm FD-SOI sera l'introduction du modèle de CNF/CMF pour les deux interfaces. Selon ce modèle la variabilité du bruit BF est due aux fluctuations induites par les porteurs agissant sur l'un ou sur l'autre des deux interfaces, aussi bien avec des fluctuations corrélées de mobilité des deux interfaces. Nous allons appeler ce modèle dorénavant CNF_CMF_1_2. Le bruit du courant de drain normalisé est alors donné par:

\[
\frac{S_{I_d}}{I_d} = \frac{q^2}{(W.L.C_{ox,1})^2} \left( \frac{g_{m,1}}{I_d} \right)^2 \sum_{k=1}^{N_{ox,1}} \left[ 4A_{k,1} \tau_{k,1} I_d \frac{\tau_{k,1}}{1 + \omega^2 \tau_{k,1}^2} \text{Amp}_{k,1}^2 (1 + \alpha_1 u_1 C_{ox,1} \frac{I_d}{g_{m,1}})^2 \right] + \\
\frac{q^2}{(W.L.C_{ox,2})^2} \left( \frac{g_{m,2}}{I_d} \right)^2 \sum_{k=1}^{N_{ox,2}} \left[ 4A_{k,2} \tau_{k,2} I_d \frac{\tau_{k,2}}{1 + \omega^2 \tau_{k,2}^2} \text{Amp}_{k,2}^2 (1 + \alpha_2 u_2 C_{ox,2} \frac{I_d}{g_{m,2}})^2 \right]
\]

(7)

Nous avons étudié le comportement des modèles au-dessus, pour les dispositifs FD-SOI, dans deux étapes. La première est relative à l'analyse dans la région d'opération, au-dessous et au-dessus de la tension de seuil avec une polarisation arrière à la masse, \(V_b=0\)V. La deuxième est pour une polarisation arrière ±10V et une tension de grille avant au-dessous et au-dessus de la tension de seuil. Ainsi, nous pouvons déterminer comment le nouveau facteur de ces modèles a contribué au comportement global de la variabilité du bruit BF pour les dispositifs FD-SOI. Les paramètres statiques requis pour faire ces simulations ont été extraits à partir du modèle standard de dérive-diffusion.

La vérification expérimentale du modèle de variabilité du bruit BF que nous avons développé est effectuée selon deux parties. D'abord, nous allons présenter les résultats expérimentaux de la technologie du nœud 28nm bulk CMOS de STMicroelectronics (Crolles). Nous avons caractérisé des dispositifs avec différentes tensions de seuil et épaissseurs d'oxyde, des n- et p-MOS. Nous allons étudier le comportement de la variabilité du bruit BF de ces dispositifs et enfin nous allons présenter une comparaison qualitative avec les
résultats de simulation. Ensuite, nous répéterons cette tâche pour la technologie CMOS FD-SOI 28nm.

**Transistors Bulk 28nm CMOS:**

Dans la Fig. 19, nous avons tracé la déviation standard du bruit du courant de drain normalisé avec la tension de grille pour des transistors n- (A) et p- (B) MOS LVT de la technologie 28nm CMOS. On peut voir que la déviation standard demeure constante pour toutes les polarisations de grille, et pour les petites et grandes géométries. Les mêmes résultats ont été obtenus pour tous les dispositifs mesurés. C'est la raison pour laquelle nous avons étudié la variabilité du bruit BF des dispositifs pour un courant de drain fixé au-dessous de la tension de seuil.

![Fig. 19 : Déviation standard du logarithme du bruit du courant de drain normalisé avec la tension de grille pour n-MOS LVT (A) et p-MOS LVT (b) de la technologie 28nm CMOS.](image)

<table>
<thead>
<tr>
<th>$N_t$/eV/cm$^3$</th>
<th>$(g_m/Id)/(V^3)$</th>
<th>$\sigma$/cm$^2$</th>
<th>$n_s$/cm$^3$</th>
<th>Amp</th>
<th>$V_t$/V</th>
<th>tox/Å</th>
</tr>
</thead>
<tbody>
<tr>
<td>1,00E+18</td>
<td>36</td>
<td>1,00E-17</td>
<td>2,00E+16</td>
<td>1,00E-01</td>
<td>0.2</td>
<td>14</td>
</tr>
</tbody>
</table>

Tableau 1 : Paramètres statiques et de bruit BF employés pour simuler avec le modèle de variabilité de l'Eq. (5). La densité volumique de piège et $(g_m/Id)$ ont été pris à partir des données expérimentales.

Dans la Fig. 20, nous avons tracé le bruit du courant de drain normalisé avec la surface pour différents dispositifs n-MOS ayant diverses épaisseurs d'oxyde et tensions de seuil. Le courant de drain normalisé est fixé autour de 10nA et la fréquence est égale à 10Hz. On peut voir que tous les dispositifs mesurés montrent des caractéristiques semblables en dispersion et le niveau de bruit médian est presque le même pour toutes les cas, LVT, RVT et GO2. Dans la Fig. 20 (D), nous avons tracé la déviation standard du courant de drain normalisé avec la
racine carrée de la surface pour les dispositifs mentionnés. On peut conclure que tous les dispositifs mesurés se comportent presque de la même manière en termes de valeur de la déviation standard. Ainsi, nous avons décidé de comparer les résultats expérimentaux avec la simulation pour le dispositif n-MOS LVT, puisque le comportement de la variabilité du bruit BF ne change pas entre les différents dispositifs. Les mêmes résultats ont été reproduits pour les dispositifs p-MOS, Fig. 21. Des données tracées, nous pouvons conclure que le comportement de la variabilité du bruit BF des dispositifs p-MOS suit le même modèle que pour le n-MOS.

Fig. 20: Bruit BF de courant de drain normalisé à une fréquence fixe de 10Hz avec la surface pour des n-MOS 28nm CMOS avec basse tension de seuil LVT (A), tension de seuil standard RVT (B) et oxyde plus épais GO2 (C) et pour un courant de drain normalisé autour de 10nA, respectivement. La ligne droite noire est la valeur moyenne. La déviation standard du logarithme de courant de drain normalisé avec l'inverse de la racine carrée de la surface en axe lin-lin pour des n-MOS, LVT, RVT et GO2 28nm CMOS en (D).

Il n'y a aucune différence importante dans la dispersion du niveau de bruit entre les différents dispositifs mesurés, Fig. 21. Nous devrons garder à l'esprit que le bruit du courant de drain normalisé n'est pas exactement le même dans tous les cas ; en effet, nous n'avons pas pu...
conserver le même courant de drain normalisé pour toutes les géométries. Le comportement de la déviation standard des différents dispositifs p-MOS, Fig. 21 (D), est presque identique. Des Figs. 20-21, on peut conclure qu'il n'y a aucune différence importante dans le comportement de la variabilité du bruit BF des différents types de dispositifs et des différentes architectures de dispositif. Cette caractéristique est bien vérifiée par notre modèle de variabilité du bruit BF qui ne prévoit pas et ne prend pas en considération le type de dispositif ou d'architecture en simulant la variabilité du bruit BF. Elle suppose que les seuls paramètres jouant un rôle significatif dans la variabilité du bruit BF sont le \( \left( \frac{g_m}{I_d} \right) \), la densité volumique de pièges avec les caractéristiques spécifiques de chaque piège et l'épaisseur d'oxyde de grille. Il semble que pour les dispositifs mesurés, n- et p-MOS, ces paramètres peuvent être différents dans certains cas, comme l'épaisseur d'oxyde différente entre les dispositifs LVT,

![Diagram](image.png)

Fig. 21: Bruit BF de courant de drain normalisé à une fréquence fixe de 10Hz avec la surface pour des p-MOS 28nm CMOS avec basse tension de seuil LVT (A), tension de seuil standard RVT (B) et oxyde plus épais GO2 (C) et pour un courant de drain normalisé autour de 10nA, respectivement. La ligne droite noire est la valeur moyenne. La déviation standard du logarithme de courant de drain normalisé avec l'inverse de la racine carrée de la surface en axe lin-lin pour des p-MOS, LVT, RVT et GO2 28nm CMOS en (D). 

164
RVT et GO2 aussi bien entre le n- et p-MOS mais le comportement global de la variabilité du bruit BF reste très semblable en raison des valeurs similaires de la densité volumique de piège, \((g_m/I_d)\) et la capacité équivalent d'oxyde.

Nous allons continuer la comparaison des données expérimentales obtenues à partir de la technologie CMOS bulk 28nm pour les dispositifs n- et p- MOS LVT avec les résultats de simulation obtenus à partir de la simulation de Monte Carlo de l'Eq. 5 en utilisant les paramètres du tableau 1. Dans la Fig. 22 (A-B), nous avons tracé les données et les résultats de simulation de la dispersion du bruit BF de courant de drain normalisé avec la surface des dispositifs pour les transistors n-MOS LVT de la technologie 28nm. La densité volumique de piège et \((g_m/I_d)\) ont été extraits des mesures expérimentales. Comme on peut le voir sur la Fig. 22, nous pouvons reconstruire la dispersion réelle du bruit des données expérimentales en utilisant seulement trois paramètres à savoir la densité volumique de piège, \((g_m/I_d)\) et le facteur de modulation d'amplitude RTS. Les autres paramètres utilisés dans cette simulation

![Graphique A](image1)

![Graphique B](image2)

![Graphique C](image3)

**Fig. 22:** Bruit BF du courant de drain normalisé à une fréquence fixe de 10Hz avec la surface pour des n-MOS du 28nm CMOS (A) et simulation (B), pour un courant de drain normalisé autour de 10nA, respectivement. La ligne droite noire est la valeur moyenne. La déviation standard du logarithme du courant de drain normalisé avec l'inverse de la racine carrée de la surface en axe lin-lin pour des n-MOS LVT 28nm CMOS et simulation en (D).
ont des valeurs standards de la littérature. En outre, la simulation de Monte Carlo utilisant l’Equ. (5) peut ajuster la déviation standard du logarithme du courant de drain, Fig. 22 (C). Le modèle théorique de Monte Carlo que nous avons développé pour simuler la variabilité du bruit BF des dispositifs CMOS bulk peut reproduire le comportement de la variabilité du bruit BF des dispositifs mesurés et ainsi, donner une description globale du phénomène.

**Transistors 28nm FD-SOI CMOS:**

La variabilité du bruit BF dans le FD-SOI a inclus des mesures sur des dispositifs n- et p-MOS avec une tension de grille arrière polarisée à $V_b=0V$ et une tension de grille avant en-dessus et au-dessous de la tension de seuil et avec seulement des n-MOS pour la polarisation arrière à $V_b=\pm10V$. En outre, les mesures pour la polarisation arrière à $V_b=\pm10V$ ne contiennent pas de résultats au-dessous de la tension de seuil.

Dans la Fig. 23, nous avons tracé la dispersion du bruit BF de courant de drain normalisé à une fréquence fixe de 10Hz avec la surface des dispositifs pour la polarisation arrière $V_b=0V$ et la polarisation de la tension de grille avant, en-dessus de la tension de seuil et au-dessus pour les dispositifs n- et p-MOS de la technologie 28nm CMOS FD-SOI. Dans les Figs. 23 (A) - (C), on peut voir la différence sur le niveau de bruit médian pour les dispositifs n-MOS quand la polarisation de la grille avant change d’en-dessous vers au-dessus de la tension de seuil et le courant de drain normalisé autour de 10nA en 10μA. Le niveau de bruit médian est augmenté presque d’une décennie pour les deux types, n- et p- MOS pour les deux régions d'opération. Les données expérimentales pour les deux types de dispositifs montrent que la dispersion du bruit ne change pas pour le polarisation de grille avant en dessous a au-dessus de la tension de seuil mais le niveau médian du bruit augment significamment.

Dans la Fig. 24, nous avons tracé les résultats expérimentaux de la dispersion du bruit BF de courant de drain normalisé avec la surface pour les dispositifs n-MOS de la technologie 28nm CMOS FD-SOI pour des polarisations arrières $V_b=-10V$ (A) et $V_b=+10V$ (B), respectivement. Comme on peut le voir sur la Fig. 24, le niveau de dispersion est presque le même pour les deux cas. Le niveau de bruit médian change comme nous l’avons prévu par la simulation et du changement des paramètres statiques que la simulation et l’expérience avaient montré. Des Figs. 23-24 et des résultats de simulation, on peut conclure que le meilleur modèle pour décrire le comportement de la variabilité du bruit BF de la technologie FD-SOI
est le CNF_CMF_1_2 qui est plus détaillé. Il semble que l'influence de la deuxième interface est un rôle mineur dans le comportement de la variabilité du bruit BF des dispositifs FD-SOI.

Fig. 23 : Dispersion du bruit BF de courant de drain pour une fréquence fixe 10Hz avec la surface des dispositifs pour la polarisation arrière $V_b=0V$ et la polarisation de grille avant en-dessous, $V_g=0.2V$, (A-B) et au dessus, $V_g=0.8V$, (C-D) de la tension de seuil pour les n- et p-MOS de la technologie 28nm FD-SOI CMOS, respectivement. Le courant de drain normalisé était avec une polarisation de grille avant en-dessous de la tension de seuil autour de 10nA et avec une polarisation de grille avant au-dessus la tension de seuil autour de 10μA.

En outre, l'impact de la deuxième interface n'affecte pas beaucoup le comportement global de la variabilité du bruit BF avec les différentes polarisations de grille arrière et avant.

Dans la fig. 25, nous avons tracé la déviation standard du logarithme du courant de drain normalisé avec l'inverse de la racine carrée de la surface pour les dispositifs n- (A) et p-(B) MOS de la technologie 28nm FD-SOI CMOS pour les polarisations arrières $V_b=0$ et $V_b=\pm10V$ et pour des tensions de grille avant en dessous et au dessus de la tension de seuil pour le n-MOS et pour $V_b=0V$ et pour deux polarisations de grille avant pour le p-MOS. La conclusion de ces données est que la déviation standard pour toutes les polarisations et les types de transistors demeure presque inchangée.
Fig. 24 : Dispersion du bruit BF de courant de drain pour une fréquence fixe 10Hz avec la surface des dispositifs pour la polarisation arrière \( V_b = \pm 10 \text{V} \) pour des n-MOS de la technologie 28nm FD-SOI CMOS (A-B), respectivement. Le courant de drain normalisé était pour \( V_b = -10 \text{V} \) autour de 10nA et pour \( V_b = +10 \text{V} \) autour de 10μA.

Fig. 25 : Déviation standard du logarithme du courant de drain avec l'inverse de la racine carrée de la surface pour les dispositifs n- (A) et p- (B) MOS de la technologie 28nm FD-SOI. Les résultats pour le n-MOS inclut les polarisations de la grille arrière \( V_b = 0, +10 \text{ et } -10 \text{V} \) et des polarisations de la grille avant en dessous et au dessus de la tension de seuil. Au contraire, les dispositifs p-MOS ont été étudiés seulement pour \( V_b = 0 \text{V} \) et avec une polarisation de la grille avant en dessous et au-dessus de la tension de seuil.

La conclusion générale de la comparaison des résultats expérimentaux avec les données de simulation est que la contribution de la deuxième interface dans le modèle de variabilité du bruit BF n'est pas assez significative pour expliquer le comportement des transistors MOS de la technologie 28nm FD-SOI CMOS. Nous devons tenir compte de l'impact du facteur corrélé de mobilité dans la modélisation de variabilité du bruit BF. En outre, les données de simulation prouvent que l'interface arrière n'influence pas le comportement global de la variabilité du bruit BF de ces dispositifs.
Nous avons présenté une étude détaillée du comportement du bruit BF des transistors n- et p-MOS des différents nœuds technologique fabriqués à STMicroelectronics (Crolles) durant les 20 dernières années. Nous avons prolongé cette analyse pour la première fois dans la caractérisation de la variabilité du bruit BF des 5 derniers nœuds technologique bulk CMOS. Le but de ce travail était d'étudier le comportement de la variabilité du bruit BF avec la réduction de taille, de l'épaisseur d'oxyde de la grille et des différentes étapes des procédés de la technologie. Finalement, nous avons étudié l'effet des procédés de la technologie pour des dispositifs avec la même épaisseur d'oxyde de grille mais pour différents nœuds ou des dispositifs du même nœud mais avec une épaisseur d'oxyde différente. Les nœuds technologiques étudiés étaient le 0.12μm, 90nm, 65nm, 45nm et le 28nm CMOS bulk. Les dispositifs mesurés étaient le n- et p-MOS standard de chaque nœud et en outre quelques dispositifs spéciaux avec une épaisseur d'oxyde plus épaisse requise pour différentes applications.

La déviation standard du logarithme du courant de drain suit une loi quasi-linéaire en fonction de la racine carrée inverse de la surface des dispositifs, Fig. 25. La variabilité du bruit BF se comporte mieux pour les dispositifs avec une épaisseur d'oxyde plus mince et des valeurs de N, plus élevée mais en même temps elle montre quelques irrégularités pour les dispositifs d'épaisseur d'oxyde semblable mais d'un nœud technologique différent. Par exemple, pour les dispositifs p-MOS Fig. 25 (b) avec une épaisseur d'oxyde plus élevée, C065nm_150 Å, qui ne présente pas les valeurs les plus élevées de la déviation standard comme prévu en raison de la valeur plus petite de la capacité d'oxyde. Au contraire, les résultats prouvent que le comportement de pire cas est obtenu pour la technologie la plus ancienne et en particulier le 0.12μm. Cette tendance ne s'applique pas pour le n-MOS où les dispositifs, excepté celui de la technologie 28nm, semblent suivre une tendance liée à l'épaisseur d'oxyde.

Une conclusion générale de Fig. 25 est que la technologie 28nm montre un meilleur contrôle de la variabilité du bruit BF comparé à la précédente. En outre, les dispositifs p-MOS ont de plus petites valeurs de déviation standard comme cela peut être vu de la comparaison avec l'axe de la Fig. 25 (A) et (B). Ceci peut être attribué aux différentes étapes de procédés employées pour fabriquer les dispositifs p-MOS, particulièrement dans les nouvelles technologies. En conclusion, nous devons prendre en considération les caractéristiques de procédés de chaque technologie dans la caractérisation de la variabilité du bruit BF et non seulement l'épaisseur d'oxyde de la grille.
Fig. 25 : Comparaison de la déviation standard du logarithme du bruit de courant de drain normalisé en fonction de la racine carrée inverse de la surface pour les technologies 28nm, 45nm, 65nm, 90nm et 0,12μm bulk CMOS et pour les n-(A) et p-(B) MOS, respectivement et pour un courant de drain normalisé fixe $L/W*|I_d|\approx 10nA$.

Il également important de noter qu'une réduction si forte de la variabilité du bruit BF est bien corrélée avec la diminution de la variabilité statique des paramètres (« mismatch ») de la tension de seuil $V_{th}$ suivant les indications de la Fig. 26 pour les dispositifs n- et p-MOS des technologies 28nm, 45nm, 65nm, 90 nm et 0.12μm. Ces améliorations de la variabilité du bruit BF et du « mismatch » de $V_{th}$ peuvent être attribuées à l'augmentation de la capacité d'oxyde avec l'évolution de la technologie (réduction d'EOT), qui, dans les deux cas, atténuent fortement l'impact des fluctuations de charge d'oxyde ou de charge de déplétion dans les variations de la tension de bandes plates et de la tension de seuil. Nous voudrions à ce moment souligner que les deux phénomènes, « mismatch » et variabilité du bruit BF, ont une origine physique différente mais sont tous les deux fortement dépendant de la capacité d'oxyde.

La variabilité du bruit BF a été analysée dans les détails. Au début nous avons essayé de clarifier la signification de la variabilité du bruit BF en lien avec un phénomène largement connu, le bruit RTS. Ensuite, nous avons donné un exemple représentatif sur la façon dont ce phénomène peut devenir un inconvénient important dans la fonctionnalité des circuits numériques. Notre approche pour expliquer et modéliser la variabilité du bruit BF dans des technologies CMOS bulk et FD-SOI a commencé à partir d'un modèle déjà connu, ce décrit le bruit de RTS. Ce modèle est parvenu à expliquer et prévoir le comportement de la variabilité du bruit BF de la technologie 28nm avec précision et dans les détails. Nous avons prolongé ce modèle pour la technologie 28nm FD-SOI afin de tenir compte d'autres paramètres tels que le
facteur corrélé de mobilité et l'impact de la deuxième interface. Nous avons incorporé ces éléments dans le modèle bulk standard et avons essayé de comprendre comment la deuxième interface présente dans le FD-SOI affecte le comportement de la variabilité du bruit BF des transistors. Nous avons développé un modèle de variabilité du bruit BF qui incorpore pour la première fois l'impact des fluctuations corrélées de mobilité dans la variabilité. La comparaison entre les données de simulation et les résultats expérimentaux a prouvé que le rôle de l'interface arrière dans la variabilité globale du bruit BF des dispositifs n'est pas fort. C'est un résultat que nous avions anticipé puisque l'épaisseur équivalente d'oxyde de l'interface arrière est beaucoup plus petite que celle de l'avant. Une analyse plus approfondie dans ce domaine devrait être effectuée afin de vérifier la validité de la modélisation.

En outre, une étude complète de la variabilité du bruit BF pour les technologies bulk CMOS a été faite pour la première fois. Les résultats indiquent que la variabilité du bruit BF présente un meilleur contrôle pour les dispositifs n- et p- MOS de la technologie 28nm. De manière intéressante, ces résultats sont bien corrélés avec la diminution de la variabilité statique des paramètres comme le « mismatch » de la tension de seuil. En outre, les résultats expérimentaux ont indiqué que la variabilité du bruit BF est un phénomène plus compliqué et qu'elle est fortement associée aux caractéristiques de procédés technologiques des transistors et non seulement à la qualité de l'interface.

La partie finale de cette thèse est consacrée au dernier défi de recherche, à savoir l'impact du bruit BF et des fluctuations RTS en tant que sources de variabilité pour les applications de circuit analogique et numérique. Au début, nous avons créé un modèle détaillé pour décrire
les fluctuations du bruit BF dans les inverseurs CMOS dans le cadre des fluctuations du nombre de porteurs, CNF. Le courant de charge $I_{VDD}$ qui circule dans l'inverseur CMOS, schématiquement représenté dans la Fig. 27, peut être obtenue en égalisant la conservation des courants de drain des transistors n- et p-MOS comme suit,

$$I_{VDD}(V_{in}, V_{out}) = I_n(V_{in}, V_{out}) = I_p(V_{in}, V_{out})$$  \(8\)

Pour chaque canal, le courant de drain peut être calculé dans l'approximation graduelle de canal, utilisant la référence de tension de source commune selon,

$$I_d(V_{gs}, ds) = \int_0^{V_{ds}} \frac{W}{L} \cdot \mu_{eff}(E_{eff}) \cdot Q_i(V_{gs}, U_c) dU_c$$  \(9\)

où $V_{gs}$ est la tension de grille-source, $V_{ds}$ est la tension de drain-source, $U_c$ est le décalage de du quasi-niveau de Fermi du canal, $W$ est la largeur de canal, $L$ la longueur de canal, $\mu_{eff}$ la mobilité effective dépendant du champ électrique effectif, $E_{eff}=(\eta Q_i+Q_d)/\varepsilon_s$ (généralement 0.5 pour les électrons et 0.33 pour les trous) ($Q_d$ étant la charge de dépletion). La charge d'inversion $Q_i$ peut être calculée en utilisant l'approximation de la fonction de Lambert W comme,

$$Q_i = C_{ox}.n.\frac{kT}{q}.L.W. \left( \frac{qV_{gs}-qV_{th}}{n.kT} - \frac{qU_c}{kT} \right)$$  \(10\)

où $kT/q$ est la tension thermique, $V_{th}$ est la tension de seuil, $n$ est le facteur d'idéalité, $n=C_{ox}/(C_{ox}+C_d)$, $C_{ox}$ est la capacité d’oxyde et $C_d$ est la capacité déplétion. Le « Drain induced barrier lowering effect” (abaissement de barrière coté drain) peut être introduit dans l’Eqt. 10 en décalant $V_{th}$ de la valeur DIBL×$V_{ds}$, avec DIBL en V/V.

![Fig. 27 : Schéma de principe d’un inverseur CMOS avec tous les terminaux utilisés.](image)

Selon la Fig. 27, $V_{in}=V_{gs}$ et $V_{out}=V_{ds}$ pour le n-MOS, tandis que $V_{in}=V_{DD}-V_{gs}$ et $V_{out}=V_{DD}-V_{ds}$ pour le p-MOS, $V_{DD}$ étant la tension d'alimentation. Dans l’Eqt.9, $V_{th}$, $W$, $L$ et $\mu_{eff}(E_{eff})$
doivent être particularisés pour les dispositifs n- et p-MOS selon les paramètres de conception de chaque technologie.

Dans l'approche globale, on doit spécifier les sources de fluctuations BF dans chaque transistor avant de procéder au calcul global du bruit BF. Dans ce contexte, nous considérons ici, que le bruit BF dans le transistor MOS provient principalement des fluctuations du nombre de porteurs (CNF) dues au piégeage-dépiégeage à l'interface du diélectrique de grille. Dans ce cas, le modèle CNF peut être expliqué en considérant le concept de fluctuation de la tension de bande plate ou d'une manière équivalente de la tension de seuil. Par conséquent, le bruit du courant de charge \( I_{VDD} \) peut être dérivé en ajoutant la contribution due aux fluctuations indépendantes de \( V_{th} \) dans les transistors n- et p-MOS tels que,

\[
S_{I_{VDD}}(V_{in}, V_{out}) = \left( \frac{\partial I_{VDD}}{\partial V_{tn}} \right)^2 \cdot S_{Vtn} + \left( \frac{\partial I_{VDD}}{\partial V_{tp}} \right)^2 \cdot S_{Vtp}
\]  (11)

où \( S_{Vtn,p} \) représente la densité spectrale de puissance de la tension de seuil des transistors n- et p-MOS.

De même, le bruit de la tension de sortie peut directement être obtenu à partir des fluctuations de la tension de sortie comme,

\[
S_{V_{out}}(V_{in}, V_{out}) = \left( \frac{\partial V_{out}}{\partial V_{tn}} \right)^2 \cdot S_{Vtn} + \left( \frac{\partial V_{out}}{\partial V_{tp}} \right)^2 \cdot S_{Vtp}
\]  (12)

Des mesures électriques et du bruit BF ont été effectuées sur deux inverseurs utilisant des transistors n- et p-MOS de la technologie bulk CMOS 45nm. L’empilement de grille se compose de poly/SiON pour les deux transistors. La longueur de canal (L) dans les inverseurs pour les dispositifs n- et p-MOS est de 40nm. La largeur de canal (W) est de 4,5 et 0,45\( \mu \)m pour le p-MOS, de 3,24 et 0,32\( \mu \)m pour le n-MOS. La caractérisation statique a été exécutée pour obtenir la tension de sortie \( V_{out} \) et le courant \( I_{VDD} \) en fonction de la tension d'entrée \( V_{in} \).

Afin de déterminer la sensibilité du courant \( I_{VDD} \) à la tension de seuil de chaque transistor on a changé la polarisation \( V_{PWEll} \) et \( V_{NWEll} \) de la Fig. 27 pour les dispositifs n- et p-MOS, respectivement, et on a mesuré les courbes correspondantes \( I_{VDD}(V_{in}) \). On a mesuré le bruit du courant de charge \( I_{VDD} \) et de la tension de sortie \( V_{out} \) de l’inverseur en fonction de la tension d’entrée \( V_{in} \). En outre, on a mesuré le bruit du courant de drain de chaque transistor séparément en fonction de la tension d’entrée \( V_{in} \).

La Fig. 28 donne les caractéristiques \( S_{I_{VDD}}(V_{in}) \) et \( S_{I_{VDD}/I_{VDD}^2}(I_{VDD}) \) expérimentales typiques du bruit BF (symboles) prises à \( f=10Hz \) et obtenues sur le même type d’inverseur.
CMOS avec une grande largeur ($W_n=3.24\mu m$ et $W_p=4.5\mu m$). Notez également la très bonne compatibilité globale avec les résultats de modélisation purs. Dans la Fig. 28 (C), on montre également des mesures de bruit BF du courant de drain de transistor n-MOS $S_{d}/I_d^2(I_d)$ mesurées directement sur différents transistors n-MOS des inverseurs CMOS étudiés. Comme cela peut être vu, les caractéristiques $S_{d}/I_d^2(I_d)$ s'accordent bien avec celles du bruit BF du courant de drain et sont bien interprétées par le modèle de bruit des fluctuations du nombre de porteurs utilisé dans les Eqs 11 et 3, en dépit de quelques incertitudes dans les données expérimentales. Les densités de piège utilisées pour la modélisation sont indiquées dans la légende de la Fig. 28 et sont proches de celles directement extraites à partir des mesures sur les transistors.

Fig. 28. Caractéristiques typiques a) $S_{IVDD}(V_{in})$ et b) $S_{IVDD}/I_{VDD}^2(I_{VDD})$ expérimentales (symbole) et du modèle (lignes) obtenues pour l’inverseur étudié avec les paramètres $C_{ox}=1.8\mu F/cm^2$, $n=1.7$, $W_n=3.24\mu m$, $W_p=4.5\mu m$, $L_n=L_p=40nm$, $V_{tn}=V_{tp}=0.52V$, $\mu_{eff}(V_{gs}-V_{th})=120cm^2/Vs$, DIBL=120mV/V. Les paramètres de bruit sont : $N_n=2\times10^{18}/eVcm^3$, $N_p=6\times10^{17}/eVcm^3$, $\lambda_n=\lambda_p=0.1nm$, $f=10Hz$. c) Caractéristiques typiques de $S_{d}/I_d^2(I_d)$ expérimentales (symbole) et du modèle (lignes) avec le modèle CNF obtenues pour les transistors n-MOS individuels (mêmes paramètres quand a et b).
Afin de réaliser une modélisation directe du bruit BF du courant de charge et vérifier la validité de l'Eq. 11, nous avons déterminé expérimentalement la sensibilité réelle du courant de charge à la tension de seuil de chaque transistor, δI_{VDD}/δV_{tn,p}. A cet effet, nous avons changé la polarisation V_b du dispositif n- ou p- MOS, respectivement, et avons mesuré les courbes correspondantes I_{VDD}(V_{in}) comme illustré dans la Fig. 29 (a). Puis, prenant en considération le facteur de substrat K_b, mesuré séparément sur les transistors individuels, et, le décalage de V_{th}, δV_{tn,p}=-K_{bn,p}·δV_b, nous avons évalué le caractéristiques δln(I_{VDD})/δV_{tn,p} montrées dans la Fig. 29 (b). En conclusion, le bruit modélisé S_{I_{VDD}}(V_{in}) et les caractéristiques S_{I_{VDD}^2}/I_{VDD}^2 ont été calculés en utilisant l'Eq. 11 après ajustement des paramètres S_{Vin} et S_{Vip} (lignes dans la fig. 28), permettant ainsi d’obtenir une très bonne description du bruit.

![Diagramme 1](image1.png) ![Diagramme 2](image2.png)

Fig. 29. a) Influence de la tension de substrat V_b sur les caractéristiques I_{VDD}(V_{in}) : V_b=0 (symboles), V_b=-0.1V n-MOS (ligne rouge) et V_b=-0.1V p-MOS (ligne bleu). b) Sensibilité du courant de charge, δln(I_{dd})/δV_{tn,p}, en fonction de la tension de substrat appliquée sur n- et p-MOS.

De même, l' influence de la polarisation de substrat de chaque transistor sur les caractéristiques de V_{out}(V_{in}) a été employée pour évaluer la sensibilité δV_{out}/δV_{tn,p} et, donc, pour calculer le bruit caractéristique S_{V_{out}}(V_{in}) en utilisant l'Eq. 12 avec les mêmes paramètres de bruit pour S_{Vin} et S_{Vip} qui ont été trouvés pour ajuster les courbes de S_{I_{VDD}^2}/I_{VDD}^2 (symboles dans la Fig. 30 (a)). Le résultat de modélisation donné par l’Eq. 15 et le modèle de courant de drain des Eqs. (11) - (12) est également montrés dans la Fig. 30 (a) (ligne). Notez la très bonne concordance entre les résultats expérimentaux et modélisés, souliignant la cohérence globale du modèle de bruit d'inverseur proposé.

Afin de confirmer la validité de cette approche basée sur les mesures de bruit de courant de charge, nous avons également directement mesuré le bruit S_{V_{out}} de la tension de sortie en fonction de V_{in} en utilisant un amplificateur de tension [voir la Fig. 30 (b)]. Comme cela peut
être vu de la Fig. 30 (b), il y a une bonne concordance entre les données directement mesurées de $S_{V_{\text{out}}}(V_{\text{in}})$ et celles déduites des mesures de bruit de courant de charge réelles, ce qui confirme définitivement la fiabilité de notre procédure.

En conclusion, nous avons étudié l'impact de la variabilité dynamique dû aux fluctuations basses fréquences sur le fonctionnement dynamique des inverseurs CMOS. D'abord, nous avons expliqué ce qu'est la variabilité dynamique. Puis, nous avons établi la méthodologie expérimentale pour caractériser l'effet de la variabilité dynamique dans un inverseur CMOS. En conclusion, nous avons présenté des résultats typiques illustrant l'impact sur le courant de charge de l'inverseur réel et, donc, sur les caractéristiques de sortie de l'inverseur $V_{\text{out}}(V_{\text{in}})$.

La miniaturisation des technologies CMOS mène à la variabilité croissante des paramètres des dispositifs comme nous l’avons déjà discuté au chapitre 3 de cette thèse. La variabilité statique dans les transistors qui sont appareillés ou proches est bien connue pour limiter la fonctionnalité des circuits analogiques, aussi bien que le fonctionnement des circuits logiques tels que les cellules SRAM en réduisant leur marge de bruit statique (SNM). La marge de bruit statique (SNM) de la cellule SRAM est définie comme la tension de bruit DC maximum tolérable sur un nœud de stockage qui ne cause pas une perturbation de lecture, et c'est la plus grande longueur du côté qui peut s'insérer dans les courbes papillons, voir Fig. 31. La réduction de la surface des dispositifs CMOS conduit également à une augmentation énorme
du bruit basse fréquence et du bruit aléatoire du télégraphiste (RTN) dû au piégeage-dépiégeage dynamique des porteurs dans le diélectrique de grille. Ces fluctuations sont par conséquence une nouvelle source de variation dépendant du temps des paramètres, appelée variabilité dynamique, qui devient de nos jours une préoccupation pour le fonctionnement statique et dynamique des cellules SRAM. C’est pourquoi il est important de clarifier l’impact de la variabilité dynamique qui résulte de la variation dépendant du temps des paramètres des inverseurs CMOS, et notamment le rôle du bruit BF et du RTN qui sont les seules valeurs physiques dans un transistor MOS qui dépendent du temps.

Fig. 31. a) Schéma de principe d’une cellule SRAM b) Représentation graphique de la définition de la SNM.

Des mesures électriques ont été effectuées sur les inverseurs (Fig. 27) utilisant des transistors n- et p-MOS provenant d’une technologie bulk CMOS 45nm. L’empilement de la grille se compose de poly/ SiON pour les deux transistors. La longueur de canal L) est 40nm pour les dispositifs n- et p-MOS. La largeur de canal (W) est 4,5 et 3,24μm pour le p- et le n-MOS, respectivement. Des mesures dynamiques du courant $I_{DD}(t)$ ont été exécutées en fonction d’une rampe de tension d’entrée $V_{in}(t)$ avec divers temps de montée.

Fig. 32. Schéma d’un circuit inverseur CMOS avec la rampe de la tension d’entrée $V_{in}(t)$. 

177
À cet effet, nous avons employé un analyseur de dispositif de semi-conducteur Agilent B1500 avec le générateur de signal du module B1530 et avec des mesures IV rapides. Des mesures de courant ont été préférées à celles de Vout(t) en raison de leur meilleure faisabilité pour les plus petites constantes de temps de montée. La tension d’entrée a été polarisée avec une tension V_{in}(t) de rampe en utilisant le générateur Agilent B1530 (voir la Fig. 32), variant de 0 à la tension d'alimentation V_{DD} et pour différentes durées de rampe. Le V_{DD} s'étendait de 0,8 à 1,3V avec 1,1V étant la valeur nominale pour cette technologie. La sortie du générateur a été reliée à V_{DD} afin de mesurer I_{DD} avec le temps. Le terminal du Nwell du dispositif p-MOS a été polarisé à V_{DD} utilisant l'unité de moniteur de source d'Agilent B1500. Le Pwell du dispositif n-MOS et les terminaux de source ont été connectés à la masse. Le terminal V_{out} a été laissé flottant (aucune charge).

Afin d'étudier la variabilité dynamique de la réponse de l'inverseur, nous avons répété plusieurs fois (jusqu'à 50) les mesures I_{DD} (t) pour différents temps de montée de la tension d'entrée V_{in}(t), c.-à-d. t_r = 10µs, 100µs et 1ms. Puis, nous avons extrait la valeur de la tension d'entrée, V_{inc}, correspondant à un courant constant de charge choisi à une valeur correspondant à la moitié du courant de charge maximum sur le front croissant (par exemple ici I_{cc}=50µA pour V_{DD}=1,1V). Pour chaque balayage, nous avons évalué la distribution statistique de V_{inc} et sa déviation standard associée et cela pour les 50 balayages. Nous voudrions souligner à ce moment que nous avons mesuré le même inverseur 50 fois et traité alors les données mesurées. Nous avons alors étudié l'impact de différents temps de montée du balayage sur la caractéristique du courant de charge de l'inverseur.

Les schémas 33 (a) et (b) montrent des caractéristiques dynamiques typiques I_{DD} (V_{in}) obtenues sur un inverseur soumis à 50 fois la même rampe de tension d'entrée de rampe V_{in}(t) ayant des temps de montée de 10µs et 1ms, respectivement. Un zoom des 50 courbes I_{DD} (V_{in}) autour de la gamme du courant I_{cc} est montré dans la Fig. 34 pour trois temps de montée. Ces données indiquent clairement que, pendant le temps de montée le plus court (t_r=10µS), il existe une variabilité dynamique significative des caractéristiques du courant de charge provenant du bruit basse fréquence (BF) inhérent au courant de chaque transistor de l'inverseur. En effet, pour les temps de montée courts, les mesures IV rapides sont fortement soumises aux fluctuations BF avec des fréquences plus basses que l'inverse du temps de montée, ayant pour résultat des variations typiques de balayage à balayage. En revanche, pour de temps de montée plus grands, les fluctuations BF dans le signal I_{DD}(t) sont filtrées aux fréquences inférieures par un processus de moyennage, résultant en de plus petites dispersions du courant de charge de balayage à balayage. Ceci est également illustré par les
histogrammes de la tension d'entrée à courant constant, \( V_{\text{incc}} \), reportée pour différents temps de montée et tensions d'alimentation dans la Fig. 35.

![Histogrammes de la tension d'entrée à courant constant](image.png)

**Fig. 33.** Courant \( I_{\text{DD}} \) avec la tension d'entrée \( V_{\text{in}} \) après 50 balayage pour (a) 10\( \mu \text{s} \) et (b) 1ms de temps de montée.

![Courant \( I_{\text{DD}} \) avec la tension d'entrée \( V_{\text{in}} \) après 50 balayages](image.png)

**Fig. 34.** Courant \( I_{\text{VDD}} \) avec la tension d'entrée \( V_{\text{in}} \) après 50 balayages pour différents temps de montée \( t_{r} \) (\( V_{\text{DD}}=1,1\text{V} \)).

![Histogrammes des tensions d'entrée \( V_{\text{incc}} \) pour différents temps de montée \( t_{r} \) et tensions d'alimentation \( V_{\text{DD}} \)](image.png)

**Fig. 35.** Histogrammes des tensions d'entrée \( V_{\text{incc}} \) pour différents temps de montée \( t_{r} \) et tensions d'alimentation \( V_{\text{DD}} \).
Afin de mesurer la variabilité dynamique, la déviation standard de la distribution de la tension à courant constant, \( \sigma_{\text{Vincc}} \), a été calculée pour tous les cas et est tracée en fonction du temps de montée dans la Fig. 36. En effet, \( \sigma_{\text{Vincc}} \) diminue avec l’augmentation du temps de montée en raison du meilleur filtrage de l’impact du bruit BF, qui a comme conséquence une variabilité dynamique inférieure. Il est également à noter que \( \sigma_{\text{Vincc}} \) est relativement indépendant de la tension d'alimentation, quoique le bruit réel en courant dépende fortement de \( V_{\text{DD}} \). C’est parce que les variations réelles ont été traduites en fluctuations de tension d'entrée à courant constant, qui reflètent principalement le bruit BF dans les tensions de seuil des transistors et sont, en conséquence, presque indépendantes du niveau du courant de charge.

![Fig. 36. Variation de la déviation standard dynamique \( V_{\text{Vincc}} \) avec le temps de montée \( t_r \) pour différentes tensions d'alimentation \( V_{\text{DD}} \).](image)

Puisque, dans un inverseur CMOS, le courant de charge passe par un maximum autour de \( V_{\text{in}} =V_{\text{DD}}/2 \), la connaissance du décalage horizontal des courbes \( I_{\text{DD}}(V_{\text{in}}) \) détecté par la variation de \( V_{\text{Vincc}} \) permet de prévoir le changement correspondant des caractéristiques de sortie de l'Inverseur \( V_{\text{out}}(V_{\text{in}}) \). À cet effet, il suffit de déplacer horizontalement les courbes de \( V_{\text{out}}(V_{\text{in}}) \) avec la même quantité du décalage de \( V_{\text{Vincc}} \).

Dans la Fig. 37, pour le scénario de pire cas avec \( \pm 3\sigma_{\text{Vincc}} \) (\( \sigma_{\text{Vincc}} \approx 15\text{mV} \)), nous avons évalué l’impact de la variabilité dynamique sur les caractéristiques de sortie de l’inverseur pendant un temps de montée 10\( \mu \text{s} \) et pour la plus petite géométrie de cellules (\( W=0,45-0,32\mu \text{m} \) et \( L=0,04\mu \text{m} \)), présentant une caractéristique de bruit BF 10 fois plus forte. Comme on le peut voir sur les données, la caractéristique de sortie de l'Inverseur est sensiblement perturbée par un tel niveau de variabilité dynamique due aux fluctuations basses fréquences, ce qui entraîne une réduction énorme de SNM d’environ 20%.
Fig. 37. Décalage dynamique prévu de la caractéristique de sortie d’un inverseur $V_{\text{out}}(V_{\text{in}})$ à 3 fois la déviation standard ($\sigma V_{\text{inc}}=15\text{mV}$) pour la plus petite surface de cellules ($W=0,4\mu\text{m}$ et $L=0,04\mu\text{m}$, $V_{\text{DD}}=0,8\text{V}$).

L’impact des fluctuations basses fréquences sur le fonctionnement dynamique des inverseurs CMOS a été étudié. La méthodologie expérimentale pour caractériser une telle variabilité dynamique due au bruit BF a été basée sur les mesures IV rapides des caractéristiques de courant de charge, après avoir appliqué une rampe sur la tension d'entrée $V_{\text{in}}(t)$. On a pu constater que, pour de petits temps de montée, les caractéristiques $I_{\text{DD}}(V_{\text{in}})$ de courant montrent une dispersion énorme de balayage à balayage inhérente au bruit basse fréquence des transistors de l'inverseur. L’impact d’une telle variabilité dynamique causée par la fluctuation BF sur les caractéristiques de sortie de l'inverseur $V_{\text{out}}(V_{\text{in}})$ a été présenté, conduisant à une réduction de la marge de bruit de 20% pour la plus petite cellule d'inverseur, qui ne pourrait que s'aggraver pour les futures technologies CMOS.

Nous avons présenté une caractérisation et une modélisation détaillées des caractéristiques de bruit basses fréquences des inverseurs CMOS. Le modèle de bruit BF a été développé dans le cadre des fluctuations du nombre de porteur du bruit excédentaire des transistors MOS, en utilisant le concept de densité spectrale de puissance de la tension de bande plate ou de la de tension de seuil. Il nous a permis de décrire exactement les caractéristiques de bruit BF du courant de charge en fonction de la tension d'entrée obtenue sur des inverseurs 45nm d'une technologie bulk CMOS.

Ce modèle de bruit BF pourrait constituer un outil utile pour analyser de l'impact des fluctuations dans le domaine temporel sur le fonctionnement statique et dynamique des inverseurs CMOS dans les circuits VLSI. En particulier, il pourrait être employé pour prévoir l'influence des fluctuations dynamiques dues au piégeage-dépiégeage des porteurs sur la marge de bruit statique et à la stabilité dynamique des cellules SRAM.
L'impact de la variabilité dynamique due aux fluctuations basses fréquences sur le fonctionnement des inverseurs CMOS, qui constituent la composante de base de la cellule SRAM, a été étudié. La méthodologie expérimentale pour caractériser l'effet de la variabilité dynamique dans un inverseur CMOS a d'abord été établie aux moyens de mesures IV rapides du courant de charge suivant l'application d'une rampe de tension d'entrée \( V_{in}(t) \). On a montré que, pour des petits temps de montée, les caractéristiques \( I_{DD}(V_{in}) \) du courant de charge montrent une dispersion énorme de balayage à balayage due au bruit basse fréquence. L'impact de telles sources dynamiques de variabilité sur les caractéristiques de sortie de l'inverseur \( V_{out}(V_{in}) \) a été finalement démontré, indiquant une réduction de la marge de bruit de 20% pour la plus petite cellule d'inverseur.