Universal Digital Radio Transmitter for Multistandard Applications

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Par

Jorge Gutiérrez León

Universal Digital Radio Transmitter for Multistandard Applications

Emetteur Radio Numérique Universel pour des Applications Multistandard

Thèse dirigée par Jean-Luc Gautier et Myriam Ariaudo

Soutenue le 7 novembre 2008 devant la commission d’examen :

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Abstract

A new low power, wideband wireless transmitter able to convert any RF signal into a constant envelope signal enabling the use of a nonlinear and efficient power amplifier is presented. In the transmitter architecture, two normalized phase signals and the envelope are separated and processed separately. A 1-bit 2nd order ΣΔ modulator codes the envelope. Quantization noise is attenuated by a S&H interpolator introducing notches at multiples of the sampling frequency. Phase and Envelope signals are recombined and upconverted directly to radio frequencies using a novel full-digital, wideband quadrature modulator. This mixer takes advantage of the 1-bit ΣΔ output. As both LOs and envelope signals are represented by two-level signals, the product of these signals (XOR function) leads to a two-level signal, which can be used as command signal in the multiplexors. Phase signals or theirs complements that are generated by a simple Inversion Block are passed through this multiplexor at the rate of driving signals. This enables to implement a high frequency, wideband mixer instead of a more complex three-input modulator. This IQ mixer is very simple to implementate as it uses only CMOS logic gates. The generation of the quadrature clock signals in the mixer is obtained by carefully design of two paths to avoid mismatch to assure an error less than 1° (only demonstrated in simulation) and the use of SR flip-flops to generate correctly the complementary signal prior to the divide-by-two circuit. Two asynchronous 9-bit DACs eliminate the 10-bit high-speed digital adder at the output of the IQ modulator and the 10-bit DAC before the PA, saving power and relaxing adder design constraints. Each DAC is divided into two full binary-weighted DACs of 4 and 5 bits. This topology enables to reduce the size ratios between the most and least significant bits related to a classic 9-bit binary-weighted structure (16 instead of 256). To test the speed and the gain control of the stand-alone DAC over 45 dB, a prototype DAC is designed in 0.13 µm BiCMOS technology from STMicroelectronics together with a 1.4 GHz 9-bit CMOS ROM-less direct digital frequency synthesizer (DDFS). Over the output power range, measurements show a SFDR>25 dB with a power dissipation of 25 mW at the maximum differential output power of -3 dBm (R_L=50 Ω).

The whole transmitter is designed and implemented and a prototype transmitter is built in 0.13 µm BiCMOS STMicroelectronics process. This low cost single chip digital radio transmitter demonstrates a data rate of 1.8 GHz. The image level is measured to be -12 dBc at this sampling frequency. Dynamic range in the transmitter is 35 dB for sampling frequencies lower than 800 MHz and 25 dB for higher sampling frequencies up to 1.8 GHz. For a two-tone signal, the maximum single-ended output power is -31dBm for each tone and the power dissipation is about 35 mW.

This architecture enables flexible and software-defined transmitter. Sampling frequency in the ΣΔ coder can be varied to adapt to different communications standards in terms of in-band and out-of-band noise requirements and variable LO frequencies can be used. Moreover, the transmitter can adapt dynamically the output power to the power amplifier depending of the required transmitted power at the output of the PA.

The transmitter has demonstrated its potential for use as a universal transmitter for applications targeting any frequency band and modulation schema up to 900 MHz (carrier frequency) and occupies a die area of 300x320 μm^2. The generated differential signal can be easily amplified by a switched-mode Power Amplifier (PA) in an efficient way because it presents constant-envelope and the PA can work in the saturation zone, which represents its optimal operation point.

La ciencia no es poderosa a pesar de su abstracción sino justamente por ella

Ernesto Sabato

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La thèse et finie...
Vive la thèse!!!!

Contents

LIST OF TABLES 13

LIST OF FIGURES 15

LIST OF ABBREVIATIONS 21

INTRODUCTION 25

CHAPTER 1 STATE-OF-ART OF LINEARIZATION TECHNIQUES 29

1.1 INTRODUCTION 29

1.2 POWER AMPLIFIER CHARACTERISTIC PARAMETERS 29

1.2.1 Power Parameters 29

1.2.1.1 Power Gain (Gp) 32

1.2.1.2 Efficiency (η) 32

1.2.1.3 Power Added Efficiency (PAE) 32

1.2.2 Linearity 33

1.2.2.1 AM-to-AM Distortion 33

1.2.2.2 AM-to-PM Conversion 34

1.2.2.3 Intermodulation Distortion (IMD) 35

1.2.2.4 Transmitter Performances Parameters 36

1.2.2.5 Modulation Parameters 38

1.2.2.6 Basic Techniques for RF Power Amplifiers 39

1.2.3 Trade-off Efficiency/Linearity 39

1.3 REVIEW OF AMPLIFIER TRANSMITTER ARCHITECTURES 41

1.3.1 Classic Linearization Techniques 41

1.3.1.1 LINC: LInear Amplification with Nonlinear Components 41

1.3.1.2 CALLUM: Combined Analog Locked Loop Universal Modulator 42

1.3.1.3 DOHERTY Amplifier 43

1.3.1.4 EER: Envelope Elimination and Restoration 45

1.3.2 Emerging Linearization Techniques 46

1.3.2.1 LIST: LInear amplification employing Sampling Techniques 46

1.3.2.2 Bandpass ΣΔ Modulation of the RF signal 48

1.3.2.3 Radio Frequency Pulse-Width Modulation (RF-PWM) 48

1.3.2.4 RF-PWM: Modulation Click 49

1.3.2.5 Envelope ΣΔ Modulation 49

1.3.3 Summary of Linearization Techniques 50
1.4 OVERALL AIM 51
1.4.1 Multistandard Architecture 51
1.4.1.1 Evolution of Wireless Communication Systems 51
1.4.1.2 Transmission Power Control 52
1.4.2 Low Cost and Low Complexity: Toward Full Digital Transmitters 53
1.5 CONCLUSION 53
CHAPTER 2 MULTISTANDARD TRANSMITTER ARCHITECTURE 59
2.1 INTRODUCTION 59
2.1.1 IQ Imbalance of Quadrature Modulator 60
2.1.2 Differential Delay in EER-type Systems 63
2.1.3 Proposed Transmitter Architecture 64
2.2 BASEBAND SIGNALS IN THE TRANSMITTER 66
2.2.1 Envelope/Phase Generation 66
2.2.2 Phase Channel 66
2.2.3 Envelope Channel 68
2.3 SIGMA-DELTA MODULATION 69
2.3.1 Principle of Operation of ADC 70
2.3.1.1 Quantization Noise 70
2.3.1.2 Signal to Noise Ratio 72
2.3.2 Oversampled Converters 73
2.3.3 ΣΔ Noise-Shaping ADC 74
2.4 QUANTIZED NOISE LIMITATION IN ΣΔ CODERS 76
2.4.1 In-Band Noise Reduction Techniques 77
2.4.1.1 Increment of Oversampling Ratio 77
2.4.1.2 High Order ΣΔ Modulators 77
2.4.1.3 Zeros in Frequency 78
2.4.2 Out-Band Noise Reduction Techniques 78
2.4.2.1 Basics of Zero Order Hold (ZOH) Interpolator 80
2.4.2.2 Simulation of the Performances of the Interpolation Filter 82
2.5 FREQUENCY PLAN 83
2.6 QUADRATURE MODULATOR 85
2.6.1 Digital Quadrature Modulator 85
2.6.2 Output Combiner 87

2.6.2.1 10-bit Digital Adder 87
2.6.2.2 Analog Combiner 88
2.7 CONCLUSION 89

CHAPTER 3 DESIGN AND TEST OF THE DIGITAL-TO- ANALOG CONVERTER _ 93

3.1 INTRODUCTION 93
3.2 DIGITAL-TO-ANALOG CONVERSION 93
3.2.1 Basic Operation 93
3.2.2 Figures of Merit 94
3.2.2.1 Static Performances 94
3.2.2.2 Frequency-domain Performances 96
3.2.3 DAC Architectures 96
3.2.3.1 Resistor-String DAC Architecture 96
3.2.3.2 R-2R Ladder DAC 97
3.2.3.3 Charge Redistribution Architecture 98
3.2.3.4 Current-Steering DAC 99
3.2.3.4.1 Binary-Weighted Architecture 100
3.2.3.4.2 Thermometer-Coded Architecture 100
3.2.3.4.3 Segmented Architecture 101
3.2.3.5 Trade-off between Linearity-Complexity and Silicon Area 101
3.2.3.6 Proposed DAC 102
3.3 DAC CIRCUIT DESIGN 104
3.3.1 Description of the Technology 104
3.3.1.1 Back-end Main Features 105
3.3.1.2 CMOS Transistors 105
3.3.1.3 Bipolar Transistors 105
3.3.2 Architecture of Designed DAC 106
3.3.3 Wide-Dynamic Range Current Mirror 107
3.3.4 Bias Circuit 108
3.3.5 Cascode Current Source 110
3.3.6 Switches 112
3.3.7 Interface Circuit 114
3.3.8 DAC Simulations 117
3.4 DAC TEST 118
3.4.1 DDFS Circuit Design 118

3.4.2 Whole Implementation of the DAC 124
3.5 FABRICATED CHIP 124
3.6 MEASUREMENTS RESULTS VS. SIMULATION RESULTS 126
3.7 CONCLUSION 128

CHAPTER 4 DESIGN AND TEST OF THE MULTISTANDARD TRANSMITTER 131

4.1 INTRODUCTION 131
4.2 REPRESENTATION 132
4.3 DATA AND SET-RESET FLIP-FLOPS 132
4.3.1 Data Flip-Flop Basic Structure 133
4.3.1.1 Data Flip-Flop Use in the Transmitter 133
4.3.1.1.1 Path Synchronization 133
4.3.1.1.2 Zero-Order Hold Interpolation 133
4.3.1.1.3 Frequency Divider 133
4.3.1.2 Design of the Data Flip-Flop 134
4.3.1.2.1 Yuan-Svensson Structure 134
4.3.1.2.2 Glitch-Free Fast DFF 134
4.3.1.3 Simulation and Comparison of the two Designed Flip-Flops 135
4.3.2 Set Reset Flip-Flop Basic Structure 136
4.3.2.1 Use of the SRFF in the Transmitter: Generation of Complementary Signals 137
4.3.2.2 Simulation Results 138
4.4 QUADRATURE DIGITAL UP-CONVERTER 139
4.5 CLOCK SIGNALS GENERATION 143
4.6 SIMULATION RESULTS OF THE TX 145
4.7 TEST SET-UP 151
4.8 SIMULATION VS. MEASUREMENTS RESULTS (COMPLETE TX) 153
4.9 CONCLUSION 160

CONCLUSION 165

FUTURE DIRECTIONS 167

APPENDIX A 171
A.1 TYPES OF IMPLEMENTATION 171
A.1.1 Standard CMOS 171
A.1.2 Pseudo-NMOS 172
A.1.3 Pass-Transistor Logic 172

List of Tables

TABLE 1.1: MODULATIONS AND ASSOCIATED PAPR 38
TABLE 1.2: LAN AND PAN MAIN FEATURES 52
TABLE 1.3: WIRELESS STANDARDS AND RADIO SYSTEMS 52
TABLE 3.1: MINIMUM ENVELOPE BANDWIDTH VS. DELAY IN EDGE 64
TABLE 3.2: MINIMUM ENVELOPE BANDWIDTH VS. DELAY IN CDMA2000 64
TABLE 2.3: MINIMUM ENVELOPE BANDWIDTH VS. ACPR 69
TABLE 3.4: SPURIOUS EMISSION LIMITS IN UMTS 82
TABLE 3.5: COMMAND SIGNAL 86
TABLE 3.1: THERMOMETER CODE (3BITS) 101
TABLE 3.2: ELECTRICAL PARAMETERS FOR HIGH-SPEED BIPOLAR TRANSISTORS 105
TABLE 3.3: FEATURES OF THE DESIGNED DDFS (POST-LAYOUT SIMULATIONS) 124
TABLE 3.4: FEATURES OF THE DESIGNED DAC 129
TABLE 4.1: MSB FLIP OPERATION (3 BITS) 132
TABLE 4.2: GENERATION OF THE 4 CONTROL BITS 144
TABLE 4.3: FEATURES OF THE FABRICATED TX 159

List of Figures

FIGURE 1.1: PA OPERATION 30

FIGURE 1.2: POWER AMPLIFIER SCHEMA (TRANSISTOR WITH VOLTAGES AND CURRENTS) 30

FIGURE 1.3: P_{OUT} VS. P_{IN} 33

FIGURE 1.4: AM-TO-PM CONVERSION 34

FIGURE 1.5: INTERMODULATION PRODUCTS 35

FIGURE 1.6: 3RD ORDER INTERCEPTION POINT 36

FIGURE 1.7: EVM MEASUREMENT 37

FIGURE 1.8: ACPR MEASUREMENT 37

FIGURE 1.9: CREST FACTOR AND PEAK TO AVERAGE POWER RATIO 38

FIGURE 1.10: EFFICIENCY DEPENDENCE ON PAPR 40

FIGURE 1.11: LINC TRANSMITTER 42

FIGURE 1.12: SIGNAL VECTORS IN LINC 42

FIGURE 1.13: CALLUM TRANSMITTER 43

FIGURE 1.14: DOHERTY TRANSMITTER 44

FIGURE 1.15: INSTANTANEOUS EFFICIENCY OF THE DOHERTY SYSTEM 44

FIGURE 1.16: EER BASIC PRINCIPLE 45

FIGURE 1.17: LIST:IQ PATHS CODED Δ 47

FIGURE 1.18: IQ PATHS CODED ΣΔ 47

FIGURE 1.19: RF-ΣΔ BASIC PRINCIPLE 48

FIGURE 1.20: BANDPASS ΣΔ 48

FIGURE 1.21: RF-PWM BASIC PRINCIPLE 49

FIGURE 1.22: ENVELOPE CODING BASIC PRINCIPLE 49

FIGURE 2.1: HOMODYNE TRANSMITTER 59

FIGURE 2.2: EER TRANSMITTER (SIMPLIFIED SCHEMA FOR ALIGNMENT IMPACT STUDY) 59

FIGURE 2.3: IQ MODULATOR 60

FIGURE 2.4: IQ UP-CONVERTER OUTPUT SPECTRUM 62

FIGURE 2.5: INITIAL TRANSMITTER ARCHITECTURE 64

FIGURE 2.6: AMPLITUDE AND PHASE GENERATION AND SEPARATION 66

FIGURE 2.7: PHASE FILTERING (ONLY ONE PHASE PATH CONSIDERED) 67

FIGURE 2.8: ENVELOPE FILTERING (ONLY ONE PHASE PATH CONSIDERED) 68
FIGURE 2.9: TIME AND FREQUENCY DOMAINS OF THE ENVELOPE AND THE FILTERED ENVELOPE 68
FIGURE 2.10: ADC OUTPUT SPECTRUM 70
FIGURE 2.11: INPUT-OUTPUT CHARACTERISTIC OF A 3-BIT QUANTIZER 71
FIGURE 2.12: UNIFORM DISTRIBUTION FUNCTION OF THE QUANTIZATION NOISE 71
FIGURE 2.13: OUTPUT SPECTRUMS OF NYQUIST RATE AND OVERSAMPLED CONVERTERS 73
FIGURE 2.14: SIMPLIFIED SCHEMA OF A FIRST-ORDER ΣΔ 74
FIGURE 2.15: NOISE SHAPING IN ΣΔ CODERS 75
FIGURE 2.16: OUTPUT OF 2^{ND} ORDER ΣΔ MODULATOR 76
FIGURE 2.17: SHAPED NOISE PSD FOR L=1,2,3 78
FIGURE 2.18: OUTPUT (RED CURVE) AND FILTERED (BLUE CURVE) SPECTRA 79
FIGURE 2.19: OUTPUT (RED CURVE) AND FILTERED (BLUE CURVE) TIMED SIGNALS 79
FIGURE 2.20: S&H UPSAMPLING (N=3) 80
FIGURE 2.21: IMPULSE RESPONSE OF S&H 80
FIGURE 2.22: NORMALIZED MAGNITUDE OF S&H FREQUENCY RESPONSE (N=2,4,8) 81
FIGURE 2.23: S&H FILTERING 81
FIGURE 2.24: SIMPLIFIED SCHEMA FOR ARCHITECTURE SIMULATIONS WITH INTERPOLATION FILTERING 82
FIGURE 2.25: REQUIRED ATTENUATION OF THE OUTPUT BPF 83
FIGURE 2.26: NON ALIASING IN ΣΔ CONVERSION WITH $F_{LO}=2F_{\Sigma\Delta}$ 84
FIGURE 2.27: SIMPLIFIED QUADRATURE MODULATOR WITH 3-INPUT MIXERS 85
FIGURE 2.28: SIMPLIFIED QUADRATURE MODULATOR WITH TWO-INPUT MIXERS 87
FIGURE 2.29: 10-BIT DIGITAL ADDER WITH DAC 88
FIGURE 2.30: PROPOSED ANALOG COMBINER 88
FIGURE 2.31: PROPOSED TRANSMITTER ARCHITECTURE 90
FIGURE 3.1: IDEAL TRANSFER FUNCTION (DAC) 94
FIGURE 3.2: ZERO-ORDER-HOLD DAC 94
FIGURE 3.3: THE INL ERROR 95
FIGURE 3.4: THE DNL ERROR 95
FIGURE 3.5: THE DNL ERROR 96
FIGURE 3.6: RESISTOR-STRING DAC ARCHITECTURE 97
FIGURE 3.7: R-2R LADDER DAC 98
FIGURE 3.8: CHARGE REDISTRIBUTION DAC 98
FIGURE 3.9: CURRENT-STEERING DAC 99
FIGURE 3.10: DIVISION OF THE WHOLE DAC INTO 2 SUB-DACS 102

Figure 3.11: Architecture of the designed DAC 106

Figure 3.12: Current Mirror 107

Figure 3.13: Current Mirrors Simulation for L=0.13, 0.2 μm 108

Figure 3.14: Bias circuit 108

Figure 3.15: Bias circuit Simulation for 16 and 256 current ratios (differential error) 109

Figure 3.16: Bias circuit Simulation for 256 current ratios (I_{REF}=80 μm) 110

Figure 3.17: Cascode current source 110

Figure 3.18: Current sources (differential error) 111

Figure 3.19: Switches and load resistors 112

Figure 3.20: Switches operation @4GHz (Ion=50 μA) 113

Figure 3.21: Switches operation @4GHz (Ion=50 μA) with Interface Circuit 113

Figure 3.22: Current cell of the interface block with the level shifter 114

Figure 3.23: Current mirror for the interface block 115

Figure 3.24: Interface Circuit Output Voltages for stimuli signals @ 500 MHz, 1GHz and 2 GHz 116

Figure 3.25: Collector currents of the bipolar x256 switches for I_{REF}=40μA) @ 2GHz 116

Figure 3.26: DNL and INL errors for the simulated 9-bit DAC 117

Figure 3.27: Single-Ended Output Power Spectra (f_{SIN}=100MHz sampled at 3 GHz on the left plot and 8 GHz on the right plot) for ILSB=100nA&40uA 118

Figure 3.28: DDFS architecture 119

Figure 3.29: Simulation results of the DDFS together with the DAC 119

Figure 3.30: Implementation of XOR with transmission-gate logic (eqns. 3.26-3.29) 120

Figure 3.31: Implementation of DAC8 121

Figure 3.32: Implementation of Z (eqn. 3.31) 121

Figure 3.33: Implementation of DAC$_7$ 121

Figure 3.34: Implementation of DAC$_6$ 122

Figure 3.35: Implementation of DAC$_5$ and DAC$_2$ 122

Figure 3.36: Implementation of DAC$_4$ and DAC$_1$ 123

Figure 3.37: Implementation of DAC$_3$ and DAC$_0$ 123

Figure 3.38: Stand-alone DAC and DAC with DDFS layouts 124

Figure 3.39: PCB Integrated Circuit 125

Figure 3.40: Chip-on-board 125

Figure 3.41: Single-ended output power @ 100 MHz clock 126

Figure 3.42: Single-ended output power @ 1.4 GHz clock frequency 126

FIGURE 3.43: SFDR @ 1.4 GHZ CLOCK FREQUENCY 127
FIGURE 3.44: DISSIPATED POWER OF DDFS 127
FIGURE 3.45: DISSIPATED POWER OF THE DAC @1.4 GS/S 128
FIGURE 4.1: TRANSMITTER ARCHITECTURE 131
FIGURE 4.2: MODIFIED YUAN-SVENSSON DFF 134
FIGURE 4.3: GLITCH REDUCTION AND CONSUMPTION GAIN FOR THE MODIFIED FDFF 135
FIGURE 4.4: DFF VS. FDFF (TIME DOMAIN AND CURRENT CONSUMPTION RATIO CCR) 136
FIGURE 4.5: DESIGN OF THE SR FLIP-FLOP 137
FIGURE 4.6: COMPENSATION OF THE DELAY INTRODUCED BY AN INVERTER 137
FIGURE 4.7: GENERATION OF THE COMPLEMENTARY SIGNALS WITH A COMPENSATION DELAY OF 108° (TIME) 138
FIGURE 4.8: GENERATION OF THE COMPLEMENTARY SIGNALS WITH A COMPENSATION DELAY OF 108° (FREQUENCY) 139
FIGURE 4.9: QUADRATURE DIGITAL UP-CONVERTER 140
FIGURE 4.10: XOR GATE USED IN IQ TRANSMITTER 140
FIGURE 4.11: MUX USED IN IQ TRANSMITTER 141
FIGURE 4.12: 9-BIT INVERSION DATA CONVERTER (INV.) 141
FIGURE 4.13: 2-INPUT NOR IN INVERTER 142
FIGURE 4.14: 3-INPUT NOR IN INVERTER 142
FIGURE 4.15: 2-INPUT NAND IN INVERTER 142
FIGURE 4.16: 3-INPUT NAND IN INVERTER 143
FIGURE 4.17: XOR IN INVERTER 143
FIGURE 4.18: ΣΔ CLOCK GENERATION 144
FIGURE 4.19: QUADRATURE CLOCK SIGNALS GENERATOR IMPLEMENTATION 144
FIGURE 4.20: FFT (MAGNITUDE AND PHASE) OF PHASE SIGNALS AND THEIRS COMPLEMENTS 146
FIGURE 4.21: FFT (MAGNITUDE) OF THE INTERPOLATED 1-BIT ΣΔ CODED ENVELOPE (20 MHZ SINE-WAVE) 147
FIGURE 4.22: DIVISION OF THE CLOCK SIGNAL (FACTORS 2, 4, 8, AND 16) 147
FIGURE 4.23: FFT OF THE QUADRATURE SIGNALS CLK_{LOI} AND CLK_{LOQ} 148
FIGURE 4.24: FFT OF THE QUADRATURE SIGNALS $CMDI_0/CMDQ_0$ AND THE COMPLEMENTARY DRIVING SIGNALS 148
FIGURE 4.25: FFT OF THE IQ MIXER OUTPUTS I_{LO} AND Q_{LO} 149
FIGURE 4.26: NORMALIZED FFT OF THE TRANSMITTER OUTPUT 150
FIGURE 4.27: SPECTRA OF THE SINGLE-ENDED OUTPUT SIGNALS FOR I_{REF}=250NA AND 45µA (EXTRACTED LAYOUT) 150

Figure 4.28: Block diagram of the fabricated chip and Test Set-Up 151
Figure 4.29: Layout of the proposed transmitter and chip package TQFP 152
Figure 4.30: Layout of the PCB with RF signals (TOP SIDE) 152
Figure 4.31: Layout of the PCB with RF signals (BOTTOM SIDE) 153
Figure 4.32: Test Chip: Maximum Single-Ended Output Power @100 MHz 154
Figure 4.33: Maximum Single-Ended Output Power @100 MHz (Extracted Layout Simulation) 154
Figure 4.34: Test Chip: Maximum Single-Ended Output Power @900 MHz 155
Figure 4.35: Maximum Single-Ended Output Power @900 MHz (Extracted Layout Simulation) 155
Figure 4.36: Test Chip: Single-Ended Output Power for I_{REF}=20 µA @400 MHz 156
Figure 4.37: Test Chip: Output Power for I_{REF}=20 µA @900 MHz 157
Figure 4.38: Test Chip: Two-tones (40 MHz) Output Power for I_{REF}=20 µA @900 MHz (Wide-Band test) 158
Figure 4.39: Test Chip: In-band Spectrum for I_{REF}=20 µA @900 MHz (Wide-Band test) 158
Figure 4.40: Dissipated power of the transmitter @1.8GHz 159
Figure F.1: Proposed solution with pre-filtering 169
Figure A.2: Standard CMOS logic 171
Figure A.3: Pseudo-NMOS logic 172
Figure A.4: Pass-transistor logic 172
Figure A.5: Transmission-gate 173

List of Abbreviations

ACPR: Adjacent Channel Power Ratio

ADC: Analog-to-Digital Converter

ADS: Advanced Design System

AMPS: Advanced Mobile Pone System

BiCMOS: Bipolar CMOS

BW: BandWidth

CALLUM: Combined Analogue Locked Loop Universal Modulator

CDMA (WCDMA): Code Division Multiple Access (Wideband CDMA)

CF: Crest Factor

CMOS: Complementary Metal Oxide Semiconductor

COB: Chip On Board

COFDM: Coded OFDM

CORDIC: COrdinate Rotation Digital Computer

CW: Continuous Wave

DAC: Digital-to-Analog Converter

DDFS: Direct Digital Frequency Synthesizer

DFF: Data Flip-Flop

DNL: Differential NonLinearity

DR: Dynamic Range

DSB-SC: Double SideBand Supressed Carrier

DSP: Digital Signal Processing

EDGE: Enhanced Data Rates for GSM evolution

EER: Envelope Elimination and Restoration

ELDO: ELectronique DOuce

EVM: Error Vector Magnitude

DVB: Digital Video Broadcasting

FFT: Fast Fourier Transform

FPGA: Field Programmable Gate Array

GPRS: Gaussian Minimum frequency Shift Keying
GSM: Global System for Mobile communications
HPSK: Hybrid Phase Shift Keying
IEEE: Institut of Electrical and Electronics Engineers
IMD: Intermodulation Distortion
INL: Integral NonLinearity
IP(3): Interception Point (3rd Order)
IRR: Image Rejection Ratio
LAN: Local Area Network
LINC: LInear amplification with Nonlinear Components
LIST: LInear amplification employing Sampling Techniques
LO: Local Oscillator
LSB: Least Significant Bit
MSB: Most Significant Bit
NTF: Noise Transfer Function
OFDM: Orthogonal Frequency Division Multiplexing
OR: Oversampling Ratio
ORR: Oscillator Rejection Ratio
PA: Power Amplifier
PAE: Power Added Efficiency
PAN: Personal Area Network
PAPR: Peak to Average Power Ratio
PCB: Printed Circuit Board
PDM: Pulse Position Modulation
PEP: Peak Envelope Power
PLL: Phase Locked Loop
PLS: Post-Layout Simulation
PSD: Power Spectral Density
PWM: Pulse Width Modulator
QAM: Quadrature Amplitude Modulation
QPSK: Quadrature Phase Shift Keying
RCF: Raised-Cosine Filter
RF: Radio Frequency
RMS: Root Mean Square
ROM: Read-Only Memory

SFDR: Spurious Free Dynamic Range
SMPS: Switching Mode Power Supply
SNR: Signal to Noise Ratio
SRFF: Set-Reset Flip-Flop
STF: Signal Transfer Function
TG: Transmission Gate
TQFP Thin Quad Flat Pack
UMTS: Universal Mobile Telecommunication System
VCO: Voltage Controlled Oscillator
WLAN: Wireless LAN
ZOH: Zero Order Hold

Introduction

The coming of Information technology is characterized by the use of high data rates. The advance of technologies makes that the wireless terminals must handle not only with voice and data but also more complex functionalities such as music, video, camera, DVB, high bit rate data transmission etc.

One important aspect is that proliferation of various standards pushes for multistandard operation. Thus, users would have to buy a new handset whenever a new standard is deployed. To avoid this, portable devices have to handle with different wireless communication systems in the same device as for example, mobile terminals handles 2G and 3G (and further 4G) communication systems which can represent different frequency bands. This is caused because cellular handsets no longer become obsolete with changing standards. The coexistence of different standards involves, in theory, to increase the number of building blocks in these handsets and to switch these blocks in function of the transmitted signal. This solution leads to the increasing size of the wireless terminals by adding additional circuitry. Increase in demand for low-cost, small-form-factor and flexible transmitters, makes this approach redundant since it increases cost and that does not enable flexibility in the terminals. Therefore, it is desirable (from a consumption, cost and complexity point of view) to share the same functional block with different systems reducing the integrated modules. This way, the adaptability and interoperability between different systems are total, designs are more compact and costs are saved.

The main difficulty comes from the fact that additional services result in the use of more and more complex modulation schemes to be handled in the system. Effectively, to overcome the increasing demand of high data rate service development, and according to severe spectrum constraints, moderns wireless communication systems (3G, WLAN…) use high spectral efficiency modulation (nonlinear modulations) such as HPSK for WCDMA and CDMA2000, $3\pi/8$ shifted 8PSK for EDGE, COFDM for 802.11a/g whose the main disadvantage is the non constant envelope of the modulated signal. For mobile handset or other wireless system where autonomy is a major constraint, the RF power amplifier remains a critical point because it dominates the power consumption. Indeed, for a current cellular terminal 2.5 G, it represents more than 60% of the supply DC average power consumption. It is well known that for such component, maximum efficiency is given when the Power Amplifier (PA) is operating in compressed, nonlinear mode. This characteristic is used with profit for constant envelope modulated RF signal, without introducing significant distortion. But, these new modulation schemes demand linear amplification because modulations are no longer only in phase but also in amplitude and the PA needs to have linear behaviors not to clip these signals. Moreover the effect of non-linear amplifiers in the frequency domain appears as a widening of the original spectrum causing interferences for users in adjacent channel and impairment such as Inter-modulation products, AM-to-AM conversion and many others distortions

Thus, it becomes evident that such complex modulations require linear RF power amplifier which are necessary less efficient. Poor efficiency to meet linearity requirements in the transmitter such as Adjacent Channel Power Ratio (ACPR) and Error Vector Magnitude (EVM) involves high power consumption and therefore heat dissipation. The dissipated power limits the talk time. This is even more critical for high Peak-to-Average Power Ratio (PAPR) signals and the efficiency drastically drops. There is thus, a trade-off between power consumption and linearity. A clear need to develop transmitter solutions enable to use high linear (for both amplitude and phase information) and at the same time high efficiency power amplifiers appears in the design of new 3G and further transmitters.

Another problem to be solved in the design of the multistandard transmitter is power control requirements used fundamentally in CDMA systems, this is vital for capacity and performance in cellular communication systems where all users transmit on the same frequency and high interference is always present due to frequency reuse. CDMA systems require a power control of about 80 dB. Power amplifier alone handles about 35 dB, a need of a system extending the power range to the 80 dB total transmitters dynamic range seems to be essential.

In the perspective of a flexible transmitter, our aim was to use as much as possible a digital approach because it offers several advantages over of analog implementations. Indeed the advantages are the easy predictability of digital blocks, the more reliability and more immunity to environmental factors and frequency agility, all of that added to less consumption and size reduction. Digital signal processing enables software-defined transmitters to control the radio functions.

The goal of this research is the design and silicon integration of a low cost single chip digital radio transmitter covering multiple RF standards and Local Area Networks (in fact any standard up to a carrier frequency of about 2.5 GHz such as GSM, EDGE, CDMA2000, WCDMA, IEEE 802.11b/g WiFi, 802.15.4 ZigBee and so on), with a dynamic range of about 45 dB to support all the communication standards and application that require linear and efficient amplification since there is a need of a good solution for multimode transmitter.

This work is organized as follows:

Chapter 1 discusses the basic concepts of Power Amplifiers (PA) and the main parameters are presented. The Classical PA design techniques are excellent for systems where information is only carried by phase signal (such as GSM). However, in modern communications, information is also carried in the amplitude. There is a trade-off between linearity and efficiency in the design of PA. Several transmitter architectures that use nonlinear and high efficiency PA are presented. However, in the context of multistandard transmission, a new transmitter topology must be used.

In chapter 2, the proposed transmitter architecture for efficient amplification of varying envelope signals is presented. This transmitter is based upon a homodyne IQ transmitter and the Envelope Elimination and Restoration (EER) technique. Baseband IQ signals are upconverted directly to the RF avoiding multiple synthesizers as in heterodyne systems. Our method uses the separation of the envelope and phase signals and recombination before the power amplifier, with the use of a bandpass filter at the output to restore the RF signal and to filter the noise. We present disadvantages and limitations of the classical methods and the solutions to avoid them in the perspective of a digital transmitter. Our fully digital topology represents the best trade-off to use for multistandard purposes because of its simplicity, wide bandwidth (there is no feedback system from output to input and the coder is wide band) and reconfigurability.

Chapter 3 reviews the basic operation and parameters of one of the main building block in the transmitter: a Digital-to-Analog Converter (DAC). Two DACs are placed at the output of the IQ modulator to add in current and convert two orthogonal 9-bit digital RF-upconverted signals into a differential analog output signal with 45 dB gain control to drive the power amplifier in the transmitter. The study and design of the chosen structure for the 9-bit high-speed DAC are presented together with the main advantages with regards to a classical binary conversion. The description of the design methodology of the building blocks and the 9-bit sine wave generator for the high-speed DAC test at high frequencies are presented. Finally, simulation and measurement results from the prototype built in 0.13 µm BiCMOS are shown.

Chapter 4 focuses on the design, silicon integration and test of the multistandard transmitter architecture built in 0.13 µm BiCMOS from STMicroelectronics. In this chapter we propose one of the main contributions of this research: a novel wideband, high-speed, digital Quadrature Up-Converter. Simulation results and test set-up and measurements results from the prototype built are discussed in this chapter.

Chapter 1 State-of-Art of Linearization Techniques

1.1 Introduction

This chapter discusses the basic concepts of Power Amplifiers (PA) and the main parameters are presented. The classical PA design techniques are excellent for systems where information is only carried by phase signal (such as GSM). However, in modern communications, information is also carried in the amplitude. In this case, the performance of the transmission depends on the dynamic of the signal compared to the linearity characteristics of the PA. Indeed, there is a trade-off between linearity and efficiency in the design of PA. Next sections will present some linearization techniques that use nonlinear and high efficiency PA. However, in the context of multistandard transmission, none of them can be used. So we precise the context in which we work to design a new linearized transmitter.

1.2 Power Amplifier Characteristic Parameters

Firstly, the main figures of merit that characterize a PA in terms of power, consumption and linearity are presented in following paragraphs.

1.2.1 Power Parameters

From a thermodynamical point of view, a power amplifier acts as a power converter. This converter allows the continuous energy (from the battery) to be transformed on alternate energy, which is added to the energy contained in the RF signal injected in the input of the device. The sum of input powers is then equal to the output powers.

$$P_{in} + P_{DC} = P_{out} + P_{diss} \qquad (1.1)$$

This expression indicates that the energy supplied (P_{DC}) is not entirely transferred to the load and that a part is dissipated (P_{diss}) by the active device or by the resistive elements situated around the power transistors (ballast or stabilization resistors) as shown in Fig. 1.1

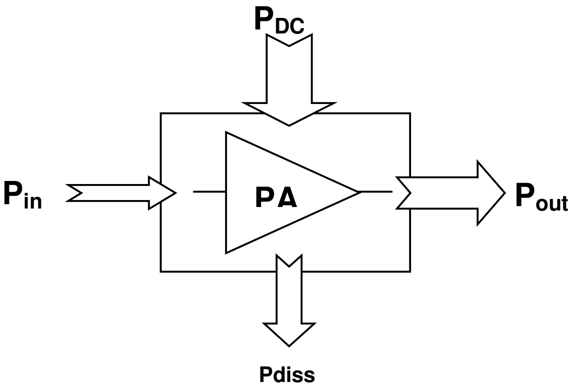

Figure 1.1: PA operation

To define the main parameters associated to the transistor we take into account the voltages and currents in the transistor when an input signal is applied to a simplified schema of a power amplifier (Fig. 1.2). The transistor is fed through two power choke inductors (L_{RF}) that separate the DC component from the RF current. The inductors present high impedance at RF frequency.

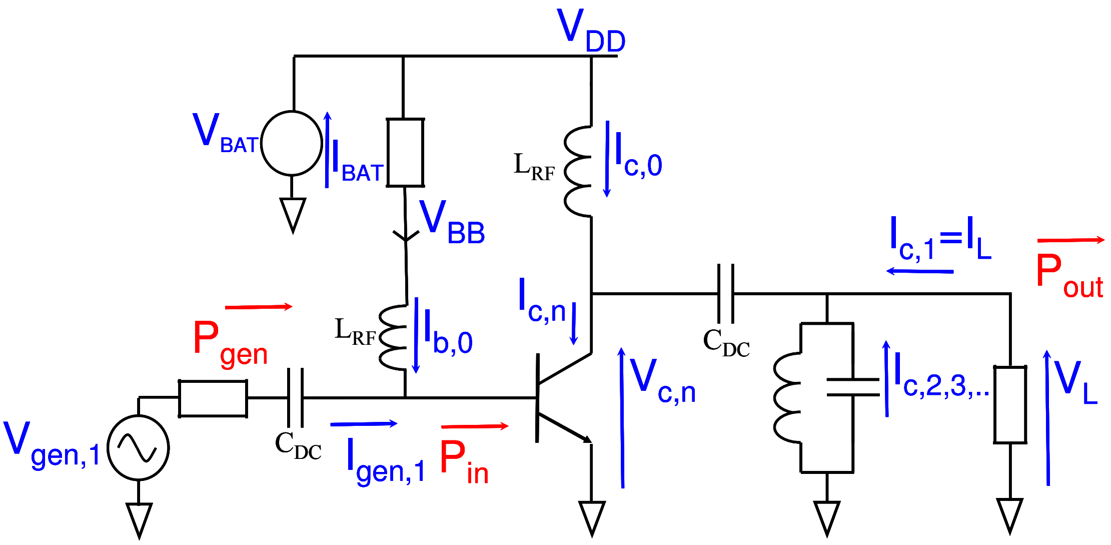

Figure 1.2: Power Amplifier schema (transistor with voltages and currents)

At the transistor output, tuned impedance with value Z_L is presented for the fundamental frequency and performs short-circuit for the harmonics. To isolate both the load and the RF input from the DC component, two capacitors (C_{DC}) are used between the source/load and the transistor.

Taking into account the nonlinearities of the device and the Fourier development, we can write the mathematical expression of the current and collector's voltage, in the case of a sinusoidal RF input signal (eqns. 1.2-1.4).

$$V_{gen,1} = V_{gen} \cos(\omega_{RF} t) \tag{1.2}$$

$$I_c = I_{c,0} + I_{c,1} \cos(\omega_{RF} t + \varphi_1) + I_{c,2} \cos(2\omega_{RF} t + \varphi_2) + I_{c,3} \cos(3\omega_{RF} t + \varphi_3) + ... \tag{1.3}$$

$$V_c = V_{DD} - V_{c,1} \cos(\omega_{RF} t) \tag{1.4}$$

The collector's voltage and current are filtered to recover the fundamental component (ω_{RF}). The expressions for the load voltage and current are:

$$I_L = I_{c,1} \cos(\omega_{RF} t) \tag{1.5}$$

$$V_L = -V_{c,1} \cos(\omega_{RF} t) \tag{1.6}$$

The generic expression for the dissipated power in the load is (refers to Fig. 1.2):

$$P_{out} = (V_{L,rms})^2 \operatorname{Re}\left\{\frac{1}{Z_L}\right\} = (I_{L,rms})^2 \operatorname{Re}\{Z_L\} \tag{1.7}$$

where $I_{L,rms}$ and $V_{L,rms}$ define the root-mean square values of the current and voltage at the load (as defined in eqns. 1.8-1.9).

$$V_{L,rms} = \sqrt{\frac{1}{T_{rf}} \int_0^{T_{rf}} V_L^2 dt} \tag{1.8}$$

$$I_{L,rms} = \sqrt{\frac{1}{T_{rf}} \int_0^{T_{rf}} I_L^2 dt} \tag{1.9}$$

The supply power (P_{DC}) represents the DC power (eqn. 1.10). It is the contribution of two static components: the first consumed by the base, the second consumed by the collector.

$$P_{DC} = P_{B,0} + P_{C,0} = V_{BB} I_{b,0} + V_{DD} I_{c,0} \tag{1.10}$$

If we sum the contributions of all the currents pulled in the battery and we suppose that V_{DD} is directly connected to the battery, the equation above can be rewritten as:

$$P_{DC} = V_{BAT} I_{BAT} \tag{1.11}$$

where

$$V_{BAT} = V_{DD} + V_{BB} \tag{1.12}$$

All these equations allow us to define the next electric parameters of the power amplifier.

1.2.1.1 Power Gain (Gp)

The power gain (G_p) at the fundamental frequency is defined as the ratio of the output power and input power. It can be expressed as (refers to Fig. 1.2):

$$Gp = \frac{P_{out}}{P_{In}} \tag{1.13}$$

where P_{out} is the power delivered to the load by the amplifier, and P_{In} is the input power at the working RF frequency.

1.2.1.2 Efficiency (η)

The power efficiency is the quantity that relates output power at RF and DC power consumption and it is defined as:

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{V_L I_L}{V_{BAT} I_{BAT}} \tag{1.14}$$

This figure of merit is the measure of the effectiveness of the PA to convert the battery-stored energy into transmitted energy at the load.

1.2.1.3 Power Added Efficiency (PAE)

To take into account the PA power gain, the notion of power-added efficiency is introduced, and it is defined by equation below:

$$PAE = \frac{P_{out} - P_{In}}{P_{DC}} \tag{1.15}$$

If we consider the expressions in eqns. 1.13-1.14, eqn. 1.15 can be expressed as

$$PAE = \eta - \frac{P_{out}}{G_p P_{DC}} = \eta \left(1 - \frac{1}{G_p} \right) \tag{1.16}$$

1.2.2 Linearity

Non-constant envelope modulated signal requires linear power amplifier, which are inherently less efficient, otherwise the signal will be exposed to impairments (inter-modulation product, AM-to-AM, and AM-to-PM distortion). In particular, such a signal degradation introduced by nonlinear amplification, creates in the frequency domain a widening of the original spectrum causing interferences for users in adjacent channel, which is not tolerable.

Several parameters allow an estimation of the linearity of a power amplifier and are presented in next paragraphs.

1.2.2.1 AM-to-AM Distortion

If we represent the transfer characteristic of the power amplifier (output power versus input power at a given working frequency) several areas can be differentiated (Fig. 1.3).

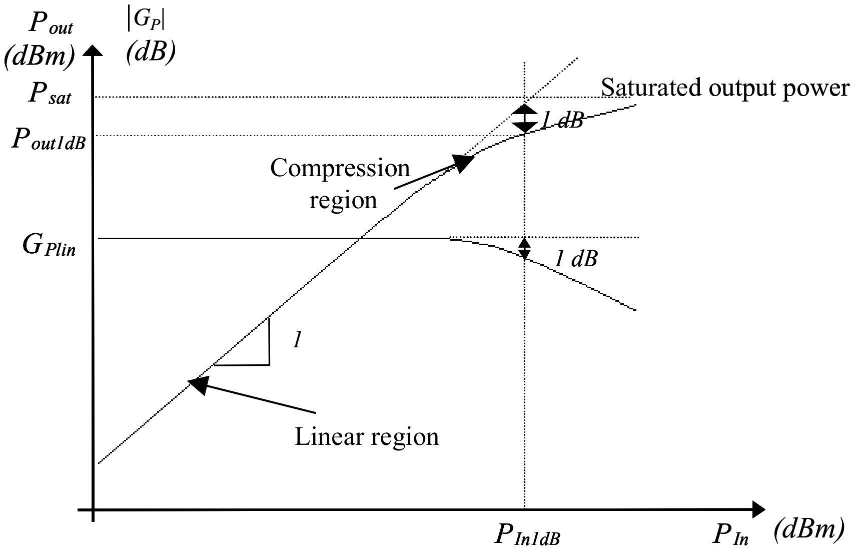

Figure 1.3: P_{out} vs. P_{In}

P_{sat} defines the saturation output power, P_{out1dB} is the output power 1 dB compression point and P_{In1dB} the input power 1 dB compression point.

Throughout the linear response of a power amplifier, level changes in input result in equal changes in output for a fixed gain (G_{Plin}).

$$P_{out}(dBm) = G_{Plin}(dB) + P_{In}(dBm) \tag{1.17}$$

As the power of the input signal increases, a point is reached where the amplifier becomes nonlinear and it is said to enter in AM-to-AM compression. The 1dB compression is the point where the amplifier gain falls 1dB (P_{1n1dB}). If the input level is increased, the output power becomes almost constant and reaches its maximal value (P_{sat}), this zone corresponds to a strongly nonlinear response.

1.2.2.2 AM-to-PM Conversion

Measurements of amplitude-modulation-to-phase-modulation (AM-to-PM) conversion are also useful in characterizing the nonlinear behaviour power amplifiers. AM-to-PM conversion is a measure of the undesired phase shifts that occur as a result of any amplitude variations in a system. In communications systems, unwanted phase modulation can be caused by unintentional amplitude variations such as power-supply ripple, thermal drift, or multipath fading. Variations can also result from the type of modulation used in the system. An ideal amplifier would have no interaction between its phase response and the level of the input (Fig. 1.4).

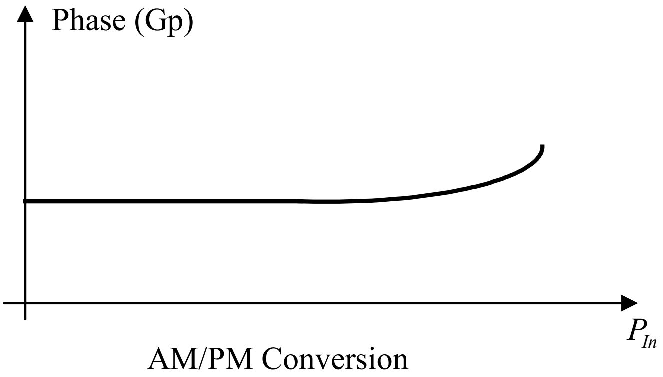

Figure 1.4: AM-to-PM Conversion

AM-to-PM conversion is critical in systems based on phase modulation, such as quadrature phase shift keying (QPSK). Phase distortion can cause signal degradation both in analog and digital domains. AM-to-PM conversion is usually defined as the change in output phase for a 1-dB increment in the input power of an amplifier, expressed in degrees/dB.

1.2.2.3 Intermodulation Distortion (IMD)

A real-valued, non-linear and memory less function can be expanded into a power series as:

$$V_{out}(t) = a1.V_{In}(t) + a2.V_{In}^{2}(t) + a3.V_{In}^{3}(t) + ... \tag{1.18}$$

where *ai* are complex-valued coefficients (we have to consider both magnitude (AM-to-AM) and phase (AM-to-PM) changes. $V_{out}(t)$ is the output signal and $V_{In}(t)$ is the input signal. If one sinusoid is applied as input signal:

$$V_{In}(t) = V_{In}.\cos(\omega_{RF}.t) \tag{1.19}$$

Eqn. 1.18 can be written, thus, as follows:

$$\begin{aligned} V_{out}(t) = & \frac{a2}{2}V_{In}^{2} + \left(a1V_{In} + \frac{3}{4}a3V_{In}^{3} \right)\cos(\omega_{RF}.t) + \frac{a2}{2}V_{In}^{2}V_{In}^{2}\cos(2\omega_{RF}.t) + \\ & + \frac{a3}{4}V_{In}^{3}\cos(3\omega_{RF}.t) + ... \end{aligned} \tag{1.20}$$

where multiples of the fundamental signal appear at the output being referred as harmonics**.**

The gain at the fundamental frequency is written in eqn. 1.21. From this expression, if $a3 < 0$, gain compression appears at the output.

$$G = \frac{V_{out}(\omega_{RF})}{V_{In}} = a1 + \frac{3}{4}a3V_{In}^{2} \tag{1.21}$$

When applying two tones of frequencies f_1 and f_2 with power values P_{In1} and P_{In2} at the input of the power amplifier, the output spectrum looks like Fig. 1.5. The two largest signals are the amplified signals and the smaller signals are the intermodulation products (3rd order, 5th order…).

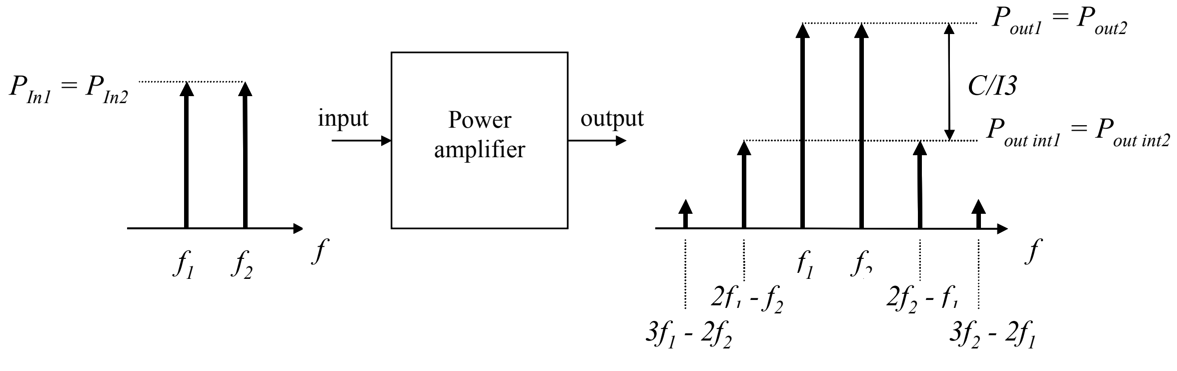

Figure 1.5: Intermodulation products

A parameter used to characterize the distortion is the C/I3, which is the difference between the carrier power and the 3rd order intermodulation products (3rd order, 5th order…).

$$C/I(dB) = 10\log\left(\frac{P_{out1}(mW)}{P_{out\,\mathrm{int}\,1}(mW)} = P_{out1}(dBm) - P_{out\,\mathrm{int}\,1}(dBm)\right) \tag{1.22}$$

Its value depends on the characteristic of the PA that is the third-order interception point (IP3). As the input power level of P_{In1} and P_{In2} increases, the third-order tones increase at 3-dB/dB rate and the desired output tones increase at a 1-dB/dB rate.

The IP3 point (O for output and I for input in Fig. 1.6) is the theoretical output signal level at which the third-order tones would reach the same amplitude level as the desired input tones.

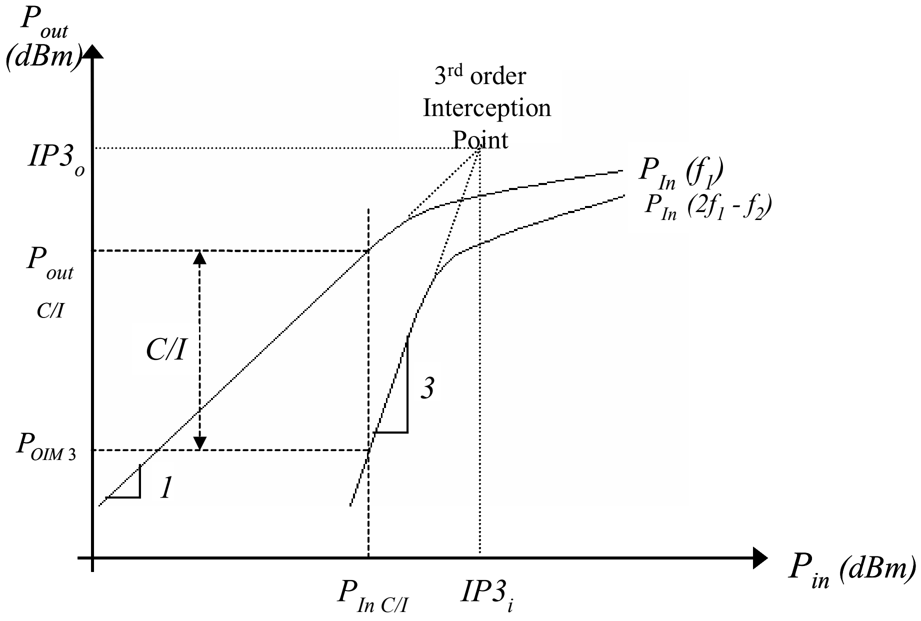

Figure 1.6: 3rd Order interception Point

1.2.2.4 Transmitter Performances Parameters

One of the parameters used to qualify the performances of a radio transmitter or receiver is the Error Vector Magnitude (EVM). The measure of EVM defines the maximum error (Euclidean distance) between the ideal constellation points and the received constellation after the signal is transmitted and is usually defined in % (Fig. 1.7). Another important test parameter to characterize the distortion of a communication system is the Adjacent Channel Power Ratio (ACPR). ACPR is defined as the ratio between the integrated power in the main channel with a bandwidth equal to the RF bandwidth and the integrated power (in a given bandwidth) of the adjacent channel defined at a given offset frequency (Fig. 1.8). ACPR definition depends strongly on the modulation schema employed. Each transmission standard defines different ACPR values and defines differences in testing this parameter.

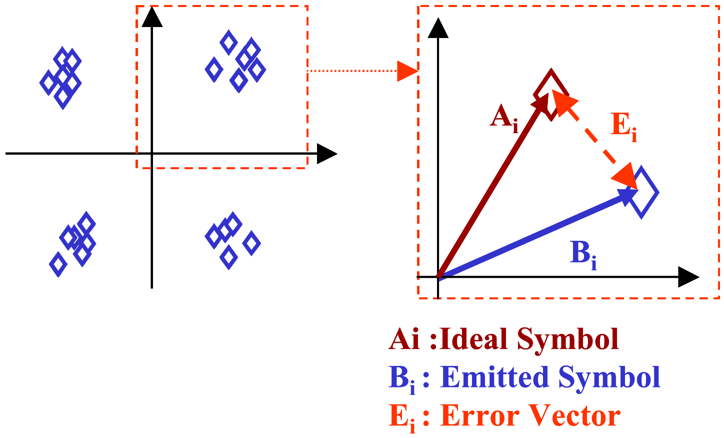
A_i
E_i
B_i
Ai :Ideal Symbol
B_i : Emitted Symbol
E_i : Error Vector

Figure 1.7: EVM measurement

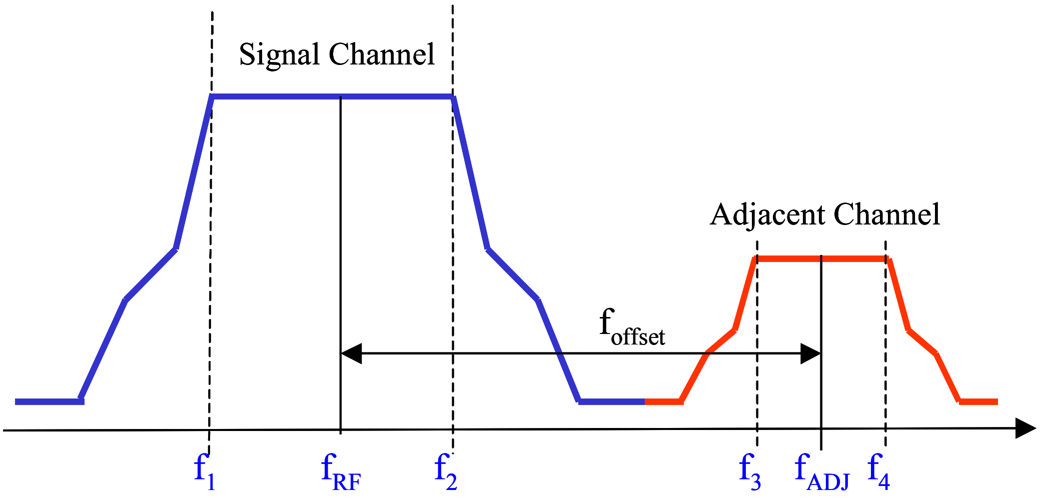
Signal Channel
Adjacent Channel
f_{offset}
f_1
f_{RF}
f_2
f_3
f_{ADJ}
f_4

Figure 1.8: ACPR measurement

Since the subsystem that introduces the maximum level of distortion in the transmitter is the power amplifier, this measure checks directly the non-linearity of the PA. Those unwanted signals would degrade the quality in the other users' signal bandwidth by causing interference and distortion (eqn. 1.23).

$$ACPR_{(dB)} = 10.\log\left\{\frac{\int_{f_1}^{f_2} DSP_{signal\ \ channel}}{\int_{f_3}^{f_4} DSP_{adjacent\ \ channel}}\right\} \tag{1.23}$$

1.2.2.5 Modulation Parameters

Depending on the modulation, the envelope of the signal can vary. Several parameters have been defined and can be used to quantify this variation.

The Crest Factor (CF) is equal to the peak amplitude of a waveform divided by the Root Mean Square (RMS) power. It is expressed in dB as follows:

$$CF = 10\log\left(\frac{P_{out,\max}}{P_{out,rms}}\right) \tag{1.24}$$

For a sine wave the crest factor is 1.414 (3 dB). The Peak to Average Power Ratio (PAPR) defined in eqn. 1.25, can be seen as the normalization of a given amplitude modulation crest factor by the crest factor of a sine wave. If PAPR is higher than zero the signal has a varying envelope (see Fig. 1.9).

$$PAPR = 20\log\left(\frac{1}{\sqrt{2}}\frac{V_{L,\max}}{V_{L,rms}}\right) = 20\log\left(\frac{V_{L,\max}}{\overline{V_L}}\right) = 10\log\left(\frac{1}{2}\frac{P_{out,\max}}{P_{out,rms}}\right) = CF - 3dB \tag{1.25}$$

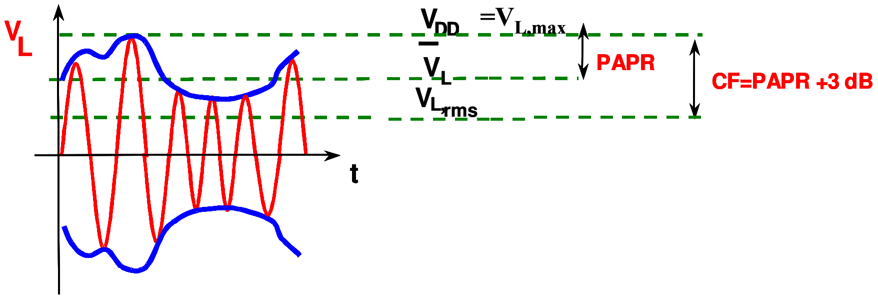

Figure 1.9: Crest Factor and Peak to Average Power Ratio

Tab. 1.1 below gives the PAPR of some wireless communication systems:

System	Modulation	PAPR (dB)
GSM	GMSK	0
EDGE	8PSK	3
CDMA2000	HPSK	4-10
UMTS	HPSK	4.5 (Unicode)
802.11a/g	OFDM	16

Table 1.1: Modulations and associated PAPR

1.2.2.6 Basic Techniques for RF Power Amplifiers

This section reviews the basic techniques for RF power amplification. RF power amplifiers are commonly divided into two main categories [Soka97]:

- Linear amplifiers: A, B and C
- Switching-mode power amplifiers: D, E, F and S

Linear amplifiers are equivalent to a voltage controlled current source. The output current is proportional to input current. The amplification is inherently linear (transistor spends most of time in the linear region in Fig. 1.3) and efficiency varies from 50% of a Class-A to 85% of a Class-C when amplifying constant-envelope signals such as sinusoids are used. However, efficiency is degraded drastically when amplifying non-constant envelope signals.

Switching-mode power amplifiers are equivalent to a switch in which transistor operates alternately open (off) and short-circuit (saturated). Transistor spends little time in the amplification region (see Fig. 1.3) avoiding oscillations. The main benefit of this kind of amplifiers is the high efficiency. Only during switching transitions current and voltages exist simultaneously. The rest of the time, either the current flowing in the transistor is zero (transistor off) or the voltage is near zero (transistor on). The output signals (current and voltage) are square-waves. In the saturated PA, the output power of the RF output transistor is directly proportional to the voltage supply. This family of power amplifiers is, thus, inherently nonlinear and is well adapted to the amplification of signals with no amplitude modulation (constant-envelope signals).

1.2.3 Trade-off Efficiency/Linearity

PAPR (or CF) can be used to make an evaluation of the maximal efficiency (η_{max}) of the PA in the case of varying envelope signals. In the case of a linear amplifier, the output power on a load Z_L is given by eqn. 1.26:

$$P_{out} = |V_{L,rms}|^2 \operatorname{Re}\left\{\frac{1}{Z_L^*}\right\} \tag{1.26}$$

If we use the CF expression, we can define the RMS load voltage as:

$$V_{L,rms} = \frac{V_{L,\max}}{10^{\frac{CF}{20}}} \tag{1.27}$$

By using eqns. 1.14 and 1.27 we can write:

$$\eta = \frac{\left(\frac{V_{L,\max}}{10^{\frac{CF}{20}}}\right)^2 \mathrm{Re}\left\{\frac{1}{Z_L^*}\right\}}{P_{DC}} \tag{1.28}$$

We obtain maximal efficiency when the load voltage is equal to the DC collector voltage (assumed to be equal to V_{BAT}) as written in eqn. 1.28:

$$\eta_{\max} = \frac{\left(\frac{V_{BAT}}{10^{\frac{CF}{20}}}\right)^2 \mathrm{Re}\left\{\frac{1}{Z_L^*}\right\}}{P_{DC}} \tag{1.29}$$

If we use the PAPR to rewrite the equation above, it yields:

$$\eta_{\max,Mod} = \frac{\left(\frac{V_{BAT}}{10^{\frac{PAPR+3dB}{20}}}\right)^2 \mathrm{Re}\left\{\frac{1}{Z_L^*}\right\}}{P_{DC}} = \frac{\left(\frac{V_{BAT}}{10^{\frac{3dB}{20}}}\right)^2 \mathrm{Re}\left\{\frac{1}{Z_L^*}\right\}}{P_{DC}} \frac{1}{10^{\frac{PAPR}{10}}} = \frac{\eta_{\max,cw}}{10^{\frac{PAPR}{10}}} \tag{1.30}$$

where $\eta_{\max,cw}$ is the maximal efficiency of the amplifier excited by a sine wave. In our calculation, we have considered that the DC current consumed by the amplifier does not change with the signal modulation (only valid for biased Class-A PA).

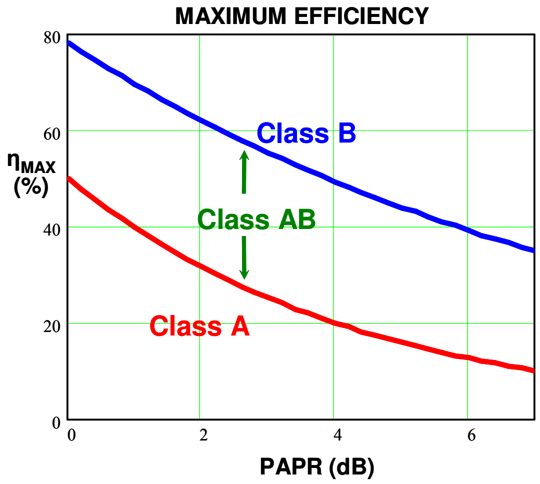

Figure 1.10: Efficiency dependence on PAPR

The trade-off between efficiency and linearity depends on the performance of the system (ACPR, EVM). High PAPR affects the power amplifier performance (see Fig 1.10) [Arno06PhD].

There is thus, a clear need to develop PA solutions which allow using high linear (for both amplitude and phase information) and at the same time high efficiency power amplifiers. These solutions are called Linearization Techniques.

1.3 Review of Amplifier Transmitter Architectures

In this chapter prior research of the Linearization Techniques is first presented. Linearization techniques are split into two categories: Classic techniques such as LINC, CALLUM, DOHERTY and EER and a second group called Emerging Linearization Techniques using sampling techniques.

1.3.1 Classic Linearization Techniques

In this kind of linearization techniques, the signal to amplify is modified to eliminate the amplitude modulation, which is sensitive to PA nonlinearities. This constant-envelope signal, which is insensitive to AM-AM distortion, can be amplified by a high efficiency nonlinear PA (Class D, E, F). The envelope is restored on the PA load through the recombination of two phase-modulated signals (LINC and CALLUM) or through the modulation of the supply voltage of the PA (EER). DOHERTY technique includes two PAs that amplify either the peaks or the rest of the input signal.

1.3.1.1 LINC: LInear Amplification with Nonlinear Components

This schema avoids the non-linear characteristic of the power amplifier by feeding it with a constant envelope signal. Two signals with equal amplitude (Fig. 1.12) are generated from the input signal in the signal component separator. These signals are amplified separately in highly power efficient amplifiers and finally recombined to form an amplified replica of the input signal (Fig. 1.11). This method is able to (theoretically) reach an ideal 100% efficiency at all envelope levels of the output signal but, in practice, the linearity and efficiency depend on the linearity of the signals synthesizer and the matching of the two signal paths. The signal separator can perform the separation directly to the RF signal [Cox$_1$75], [Rusta76] or to the baseband signal, with sampling frequency about 15 higher than the bandwidth of the input signal and the need of digital sampling techniques [Casa90], [Hetz91].

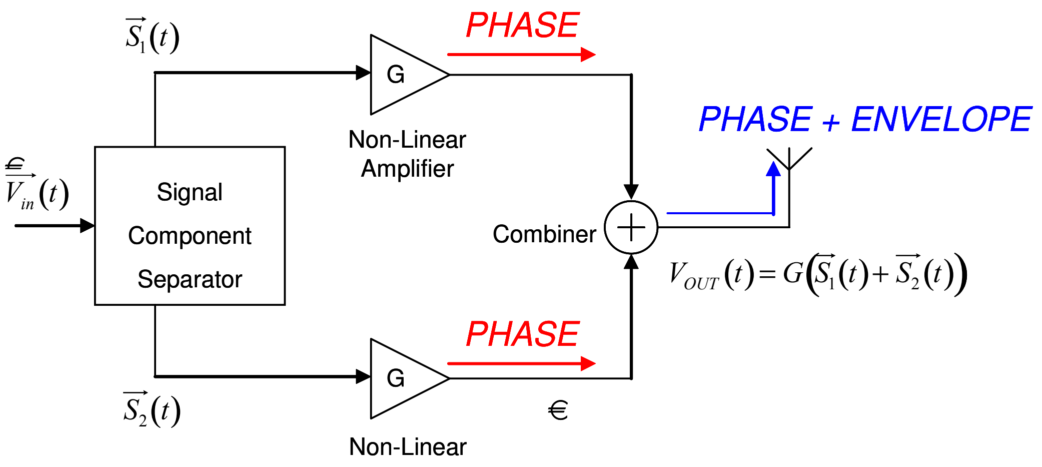
$\vec{S}_1(t)$
PHASE
G
Non-Linear
Amplifier
PHASE + ENVELOPE
$\vec{V}_{in}(t)$
Signal
Component
Separator
Combiner
$V_{OUT}(t)=G(\vec{S}_1(t)+\vec{S}_2(t))$
PHASE
G
$\vec{S}_2(t)$
Non-Linear

Figure 1.11: LINC transmitter

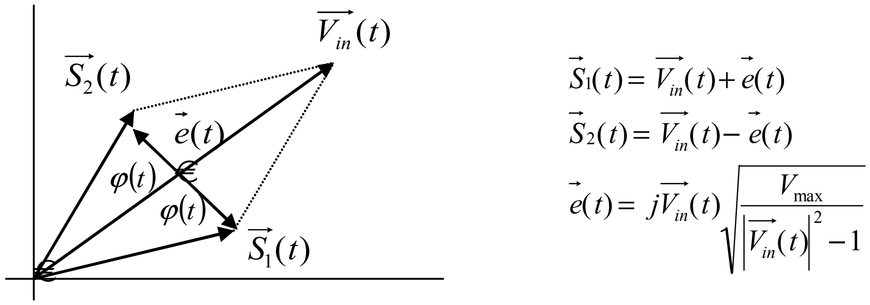
$\vec{V}_{in}(t)$
$\vec{S}_2(t)$
$\vec{e}(t)$
$\varphi(t)$
$\varphi(t)$
$\vec{S}_1(t)$
$\vec{S}_1(t)=\vec{V}_{in}(t)+\vec{e}(t)$
$\vec{S}_2(t)=\vec{V}_{in}(t)-\vec{e}(t)$
$\vec{e}(t)=j\vec{V}_{in}(t)\sqrt{\frac{V_{\max}}{\left|\vec{V}_{in}(t)\right|^2}-1}$

Figure 1.12: Signal vectors in LINC

The implementation of this technique presents two main problems. The mismatch between the constant envelope signals is difficult to compensate because there is no feedback system. In [Casa$_2$90] and [Casa93], the impact of this mismatch on a two-tone signal and a QAM modulation is studied. In [Sund95] and [Tomi89] compensation methods are presented.

In order to enhance the efficiency in LINC transmitters a solution is proposed in [Zhan02] which uses a power-recycling network. In actual implementations, maximum amplitude differential gain tolerated is between 0.1 and 0.5 dB and between 0.4° and 2° for differential phase gain. The efficiency is degraded by the output combiner (insertion losses of 1 dB mean a degradation of 20%).

1.3.1.2 CALLUM: Combined Analog Locked Loop Universal Modulator

This technique is a Cartesian-feedback-based VCO-driven RF synthesizer [Bate92] and it can be considered as a particular implementation of a Cartesian feedback [Petr83]. The amplifier outputs are combined and coupled to a IQ demodulator to recover the quadrature Cartesian components of the baseband signals.

These signals together with the baseband inputs are used to generate the error signals for the VCOs. Two constant-envelope signals drive two power amplifiers and are combined at the output (similar to the previous method). The main difference with regard to the LINC technique is that the signal separation is generated by a Phase Locked Loop (PLL) [Jenn99].

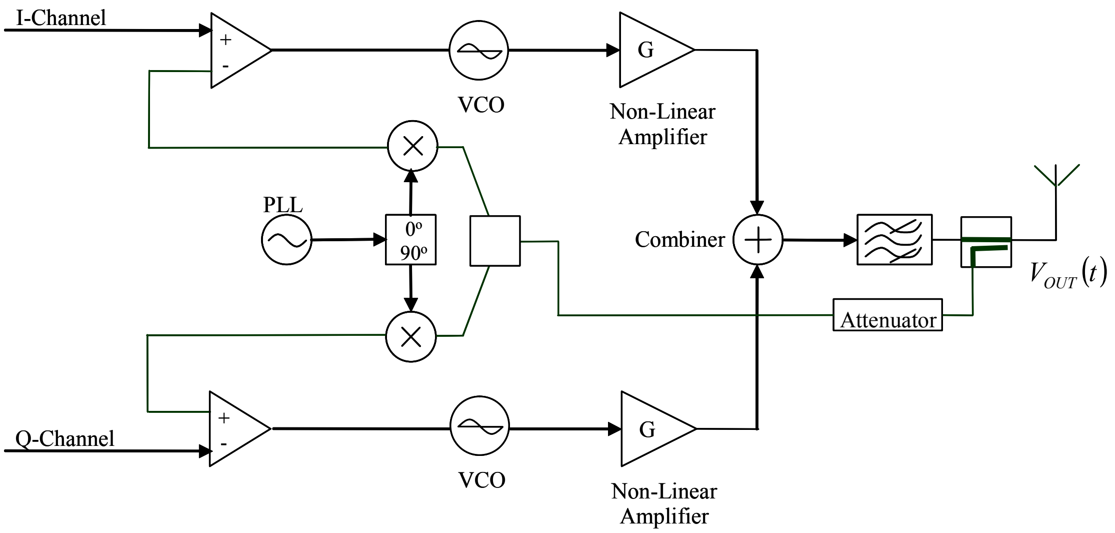

Figure 1.13: CALLUM transmitter

The PLL corrects the mismatch between two paths. This PLL involves the study of the stability. A major obstacle in the design of such a system is the stability of the feedback loop.

The efficiency of the CALLUM system depends on the linearity of the mixers and VCO (need of frequency synchronization) and as the LINC system, total efficiency is related to the output efficiency combiner. This technique suffers from the limitations of a feedback system (typically used for narrow-band systems).

1.3.1.3 DOHERTY Amplifier

The motivation of this technique [Dohe36] was to propose a high efficient solution for amplitude modulated signals. This technique combines two PAs of equal capacity through quarter-wave lines (Fig. 1.14).

Operation can be divided into three regions [Raab87] and can be considered as an active load pull system. For low amplitudes the main PA (biased in Class-B) is linear (acting as a voltage source) and sees a 100-Ohm load being the auxiliary PA (Class-C) cut-off appearing as an open-circuit. As the signal amplitude increases, the main PA saturates and the auxiliary is driven out cut off becoming active. At peak power, both PAs are saturated delivering each of them half of the system output power and the load impedances seen are 50 Ohm.

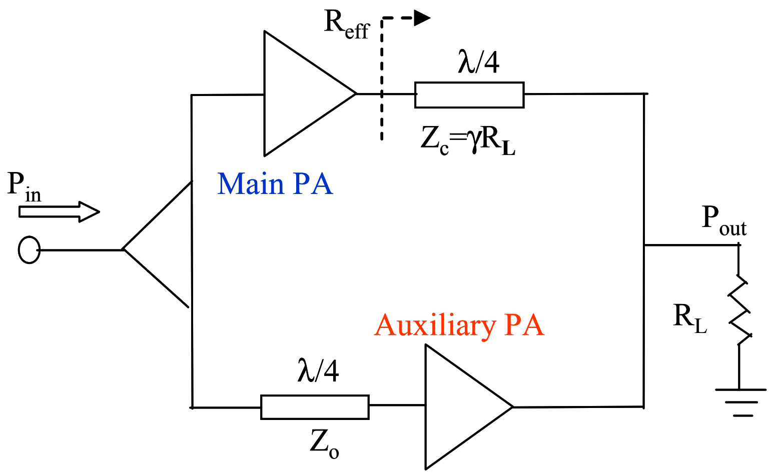

Figure 1.14: Doherty transmitter

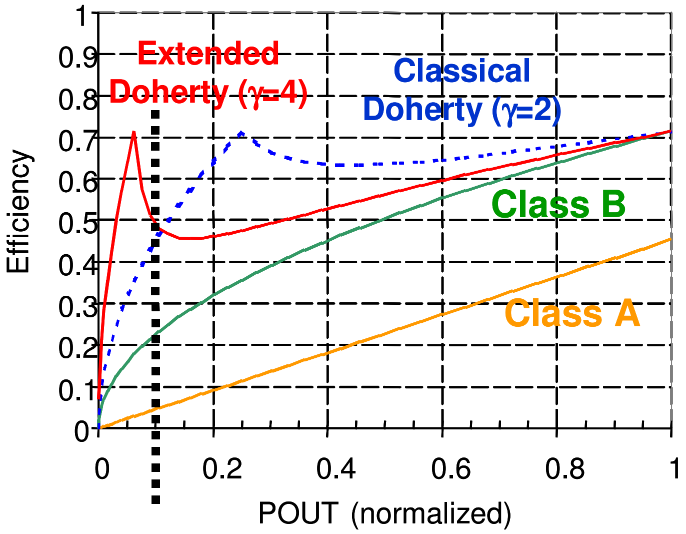

Figure 1.15: Instantaneous efficiency of the Doherty system

The efficiency of this system grows linearly as the input signal increases. When the auxiliary power amplifier becomes active, efficiency falls. Maximum efficiency is achieved at Peak Envelope Power (PEP). Efficiency is higher than a Class-B power amplifier over a wide power range [Iwam01]. The use of other power-division ratios (extended Doherty) allows the lower efficiency peak to be shifted leftward (see Fig. 1.15).

Although the Doherty-type amplifier has many advantages such as high efficiency at medium power levels or possibility to employ these techniques together with other linearization techniques [Yang03], it has also some disadvantages. This system does not lend easily to small size implementations because of the design of the transmission lines for RF frequencies. Moreover the use of a 3 dB signal splitter wastes one-half of the input signal power at low input levels, resulting in lower global efficiency.

1.3.1.4 EER: Envelope Elimination and Restoration

EER is a technique that increases linearity and power efficiency simultaneously. The basic principle of the EER technique relies on the fact that any bandlimited signal can be regarded as an amplitude modulation of a constant amplitude phase signal as shown in Fig. 1.16. The phase signal and envelope signal can be amplified individually and combine both after amplification [Kahn52]. The schematic in Fig. 1.16 shows an EER technique with limiter and envelope detector to extract the phase and envelope information, respectively. The limiter, shown at the bottom left of Fig. 1.16, eliminates the envelope and thus makes it possible for a high-efficient nonlinear PA.

The envelope of the input signal is detected with an envelope detector in the top signal path. The envelope is input to a modulator. The output signal of the modulator changes the supply voltage of an amplifier. Finally, the envelope modulates the final RF power amplifier and creates an amplified replica of the input signal at the output. EER can be employed to a complete transmitter or a single PA. If EER technique is used to design a transmitter, a DSP is typically utilized to generate the envelope and phase information. EER reaches good linearity with high efficiency.

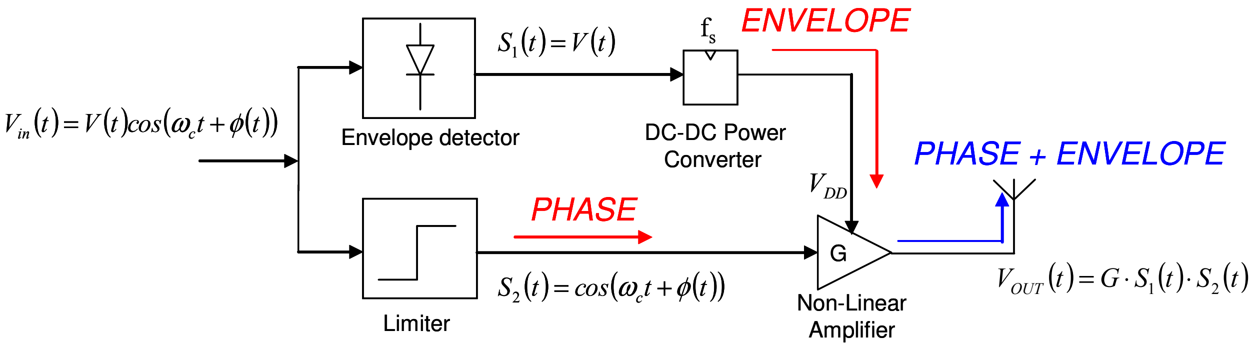

Figure 1.16: EER basic principle

There are two main drawbacks in EER systems:

- Differential delay between the amplitude and phase paths.

In an EER system, the phase and magnitude paths are amplified separately, differences between the group delay in the envelope and carrier channels (differential delay) results in imperfect reconstruction of the output signal and therefore distortion. An important delay source is the transition frequency of MOS transistors in the switching mode power supply, they are large and they have a very important gate capacitance value, that is to say, it takes the transistor long time to react to the rising front of an impulsion. But the principal source of differential delay is the large output low-pass filter of the Switching Mode Power Supply (SMPS).

- Limited bandwidth of the system that should be used to modulate the PA supply.

The EER system uses an envelope detector, which is a circuit, which (ideally) takes the absolute value of its input, and then passes the result through a low pass filter. The output of this low pass filter is the required envelope signal. The absolute value operation, being non-linear, generates some new frequency components. It is the purpose of the low pass filter to separate the wanted from the unwanted components generated by the non-linear operation. This filtered signal drives the envelope modulator (SMPS). This modulator uses a sampling frequency, which depends strongly on the bandwidth of the signal to modulate. Sampling theory requires this switching frequency to be at least twice the highest modulation frequency required. In practice, it is usually seen that a factor of ten is required to minimize the effects of filter ripple components.

One technique to improve the linearity in EER systems has been presented in [Raab98]. A feedback system of the phase and amplitude signals from the RF output is used. With typical dc-dc converters, the switching frequency (usually below 20 MHz) is not high enough to allow rapid modulation of the supply voltage for many RF amplifier communication purposes. However, several works have been published at low frequencies and linearity requirements are matched. In [Raab98], a buck dc-dc converter is switched at 150 kHz and the maximum efficiency reached is 56%. In [Wang04], a buck hybrid dc-dc converter with a bandwidth of 16 MHz is proposed. The efficiency of this system is 66%. More recently in [Pino08], a new chip for envelope-reconstruction purposes has been presented with a switching frequency of 130 MHz. The SMPS modulates a WCDMA signal with a PAE of 46%.

1.3.2 Emerging Linearization Techniques

This group of techniques produces binary (digital) signals that encode RF signals with time varying envelope by employing digital modulation. These architectures use either pulse width modulation (PWM) or pulse density modulation (PDM) being the Sigma-Delta (ΣΔ) the most popular. These techniques employ high efficiency nonlinear power amplifier. The quantized noise produced at the Sigma-Delta has to be removed at the output by a band-pass filter to extract the useful signal [Jaya98].

1.3.2.1 LIST: LInear amplification employing Sampling Techniques

“Linear amplification” corresponds to the constant envelope amplification and “sampling techniques” refers to the sampling of Δ coder [$\text{Cox}_2$75]. In this first technique (Fig. 1.17), I/Q paths are coded by a delta (Δ) coder in a two levels signal and then translated to the RF frequency. These paths are constant envelope signals and are amplified before being combined.

Reconstruction of the linear signal is achieved by the output bandpass filter which performance is usually less critical than combiner's in LINC. Bandpass filtering is related to the Δ decoding which uses low pass filtering in the baseband. Global consumption is increased by the employ of two Δ coders and two amplifiers. The linearity of these methods depends on the matching of the two signal paths (like the rest of systems using different paths), the error in the coder, the pulling effect of the VCOs and the switching loss in the power amplifier.

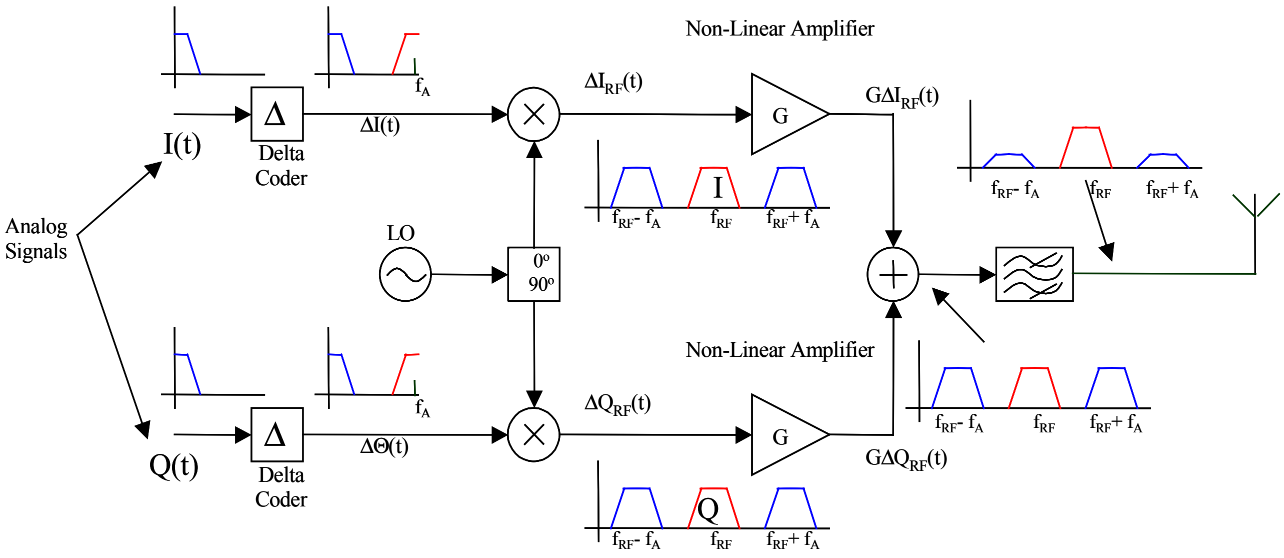
Non-Linear Amplifier
f_A
$\Delta I_{RF}(t)$
$G\Delta I_{RF}(t)$
Δ
Delta Coder
ΔI(t)
G
I(t)
I
f_{RF}- f_A
f_{RF}
f_{RF}+ f_A
Analog Signals
LO
0º
90º
Non-Linear Amplifier
f_A
$\Delta Q_{RF}(t)$
Δ
Delta Coder
ΔΘ(t)
G
Q(t)
$G\Delta Q_{RF}(t)$
Q

Figure 1.17: LIST:IQ paths coded Δ

The second technique uses ΣΔ modulators instead of delta ones and a single PA after the recombination of two paths [Wang02].

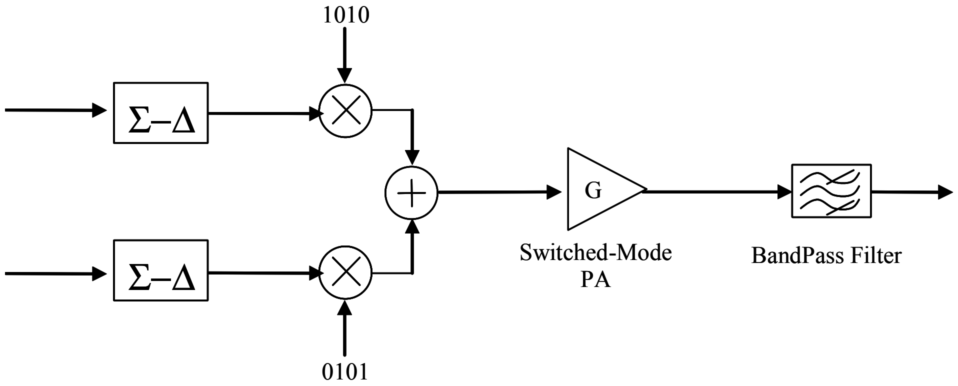
1010
Σ–Δ
Σ–Δ
G
Switched-Mode PA
BandPass Filter
0101

Figure 1.18: IQ paths coded ΣΔ

To keep the constant envelope signal after the recombination of the two signals, two masks are used before the recombination: 1010 for I path and 0101 for Q path. It can introduce losses of information added to the quantification noise of the ΣΔ. In [Jern06] a quadrature digital-RF converter is proposed as implementation.

1.3.2.2 Bandpass ΣΔ Modulation of the RF signal

These transmitters use 1-bit bandpass sigma-delta modulation to produce a binary signal representing an analog radio frequency (RF) signal. This signal is fed into a switching-mode power amplifier (hence the signal is constant-envelope).

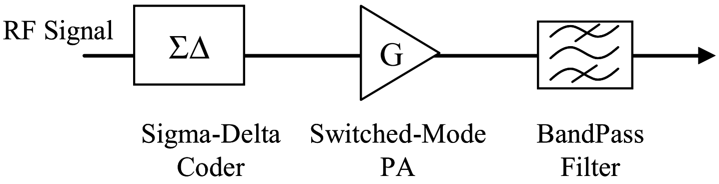

Figure 1.19: RF-ΣΔ basic principle

The advantages of this architecture are its simplicity and the need of few elements but the realization of a high frequency bandpass ΣΔ (the order is twice higher than the low pass model). The main disadvantages are the important switching losses in the amplifier due to the sigma-delta sampling frequency, which is four times the RF frequency [Keyz01], and the dissipated power in the coder. A reduction of the sampling frequency seems to be necessary. The low-frequency envelope signal is coded rather than the RF signal. Another solution consists in keeping the signal being digital at the input of the ΣΔ and to convert to the analog domain before amplification [Rode03], [Keto04].

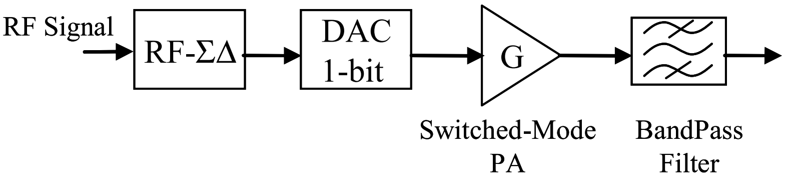

Figure 1.20: Bandpass ΣΔ

1.3.2.3 Radio Frequency Pulse-Width Modulation (RF-PWM)

The width of a train of pulses can be varied to produce a modulated carrier at the repetition frequency. When switching transistors generate the pulse train, high efficiency operation is possible. Radio-frequency pulse-width modulation (RF-PWM) produces a 1-bit signal at a rate twice the RF frequency ($f_s = 2f_{RF}$). In spite of being a very non-linear coding technique, PWM produces spurious easily removed with a simple, band-pass output filter, as spurious are located in the vicinity of the harmonics of the carrier [Raab73].

The overall efficiency is in practice degraded by the switching losses of the PA and the dissipated power is proportional to the square of the sampling frequency. This method of RF-PWM is limited to small percentage bandwidths.

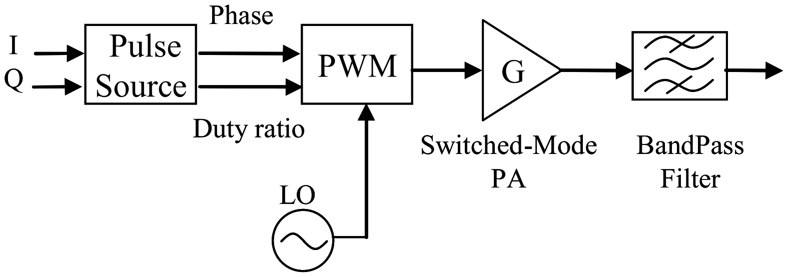
Phase
I
Q
Pulse Source
PWM
G
Duty ratio
LO
Switched-Mode PA
BandPass Filter

Figure 1.21: RF-PWM basic principle

1.3.2.4 RF-PWM: Modulation Click

This technique is based upon the modulation click [Loga84] but the principle is translated at RF. This method generates a pulse-width signal clocked at a frequency slightly higher than the highest frequency in the band of interest [Wagh02]. Even if this technique is highly nonlinear, the spectral content of this binary signal includes the source's spectrum and the modulation products but the latter does not overlap with the former, as is customary in PWM systems. The output of this system is distortionless up to the switching frequency.

1.3.2.5 Envelope ΣΔ Modulation

An improved EER transmitter is shown in Fig. 1.22. Sigma-Delta modulation is applied to the signal envelope rather than the RF signal. Then, the digitized envelope with no low-pass filter is directly modulated on the carrier [Wang03].

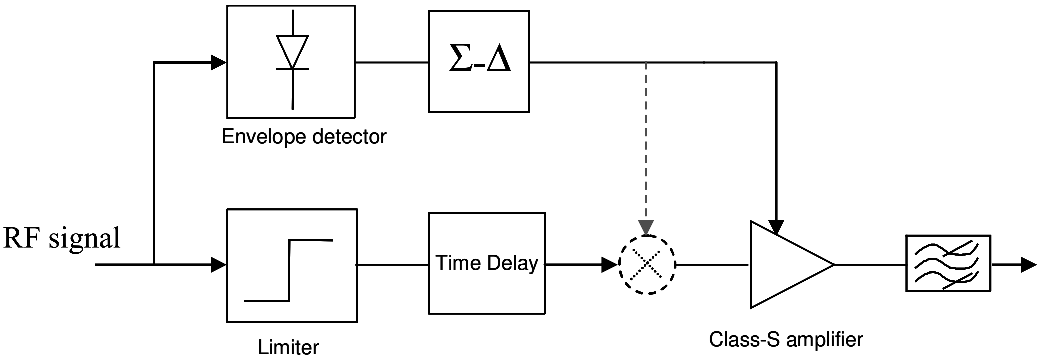
Σ-Δ
Envelope detector
RF signal
Time Delay
Limiter
Class-S amplifier

Figure 1.22: Envelope coding basic principle

The combination between phase and envelope can be done in two different ways. First solution consists in injecting the coded envelope through the DC supply. A second possibility, in dot in the figure and not simulated in the paper, proposes the multiplication of the phase and envelope signals before amplification. This topology takes advantages of relatively low oversampling ratio and low speed digital circuitry. In this architecture the sampling requirements for the sigma delta coder are reduced with regard to the previous method because the signal to code is low frequency (baseband).

1.3.3 Summary of Linearization Techniques

In this chapter, a variety of techniques have been presented. They are divided into two types of architectures, each of them with advantages and disadvantages.

Classic transmitter topologies are quite difficult to implement and they represent a challenge to designers that must take care of the signal separation and the difficulties with gain and phase matching in both paths and band limitation.

LINC has the inconvenient of the difficult to implement signal separator (in size and accuracy), high sensitivity to the mismatch of the two paths and high losses in the recombination at the output of the nonlinear power amplifiers. Ideally high efficiency is reached.

CALLUM suffers from bandwidth limitation due to the feedback, mismatch between the two paths and high losses in the output combiner. Moreover, coupling of the VCOs limits the performance of the total system. This technique occupies high silicon area and it is quite difficult to implement. The theoretical efficiency is quite high and this technique is applied to the whole transmitter.

DOHERTY-type technique is limited by the difficulty of small size implementation at RF frequencies and the losses in the 3-dB split signal. It is not destined to wideband transmitter due to the bandlimited strips lines. However, this method keeps high constant linearity values over a wide power range.

Finally, EER has the main disadvantages of limited bandwidth of the envelope modulator and phase and envelope alignment leading this method not suitable for wideband purposes.

Methods employing sampling techniques are interesting in case of envelope coding (low frequency signal) rather than directly coding of the RF signal, which increase complexity in the topologies and are poor efficiency solutions. In addition, theses techniques allow the use of digital techniques, which increase the reconfigurality of the transmitters.

1.4 Overall Aim

Our objective is the implementation of a wideband transmitter able to support all the communication standards and applications that require linear and efficient amplification since there is a need of a good solution for multimode transmitter.

We think that the desired transmitter has to represent the trade-off of all the factors mentioned in the previous section of this chapter being the best solution a combination of several techniques.

In the perspective of wideband transmitter, we will not consider the use of feedback (from output to input) systems or bandlimited coders. The separation of phase and envelope signals seems to be the best solution in order to increase simultaneously the linearity and efficiency of the system but we have to solve the alignment problem between the envelope and phase signals. Low simplicity and high efficiency involves coding the low frequency envelope instead of the RF signal. The drawback of this approach is that a band pass filter has to be used in the transmitter increasing the insertion losses in the system.

1.4.1 Multistandard Architecture

The proliferation of modern communication systems toward higher data rates with the same wireless device require designs that work across multiple standards. The handset no longer becomes obsolete with changing standards. The coexistence of different standards involves, in theory, to increase the number of building blocks in this handsets and to switch this blocks in function of the transmitted signal. However, it is desirable (from a consumption, cost and complexity point of view) to share the same functional block with different systems reducing the integrated modules. However, in addition to this sharing capability, it would be extremely interesting to implement a single transmitter chain able to transmit the desired signal whatever the communication standard is. This way, the adaptability and interoperability between different systems are total, designs are more compact and costs are saved. Before going on introducing the main characteristics of our transmitter architecture we present some details about the continuous evolution of communication standard which are helping us to understand the importance of new multistandard topologies.

1.4.1.1 Evolution of Wireless Communication Systems

This section explains the basics concepts of cellular radio systems in order to understand the design constraints in multistandard architectures. The aim is only to show (with no detailed explanation) the main characteristics of the different systems and their evolution in time. In this summary table, rates correspond to maximum values, in symbol transferred per second (Ms/s) and bit per second (Mbs/s).

Standard	**RF Frequency**	**Modulation**	**Bit Rate (/s)**
802.15.1 – Bluetooth	2.4 GHz	GFSK	1Ms / 1Mb
802.15.4 – Zigbee	2.4GHz	OQPSK	0.06Ms / 0.25 Mb
802.15.3a – UWB	3-10 GHz	PPM	-/+ 500Mb
IEEE 802.11b – WiFi	2.4 GHz	PSK	11 Ms / 11 Mb
IEEE 802.11g – WiFi	2.4 GHz	OFDM	20 Ms / 54 Ms
IEEE 802.11a	5 GHz	OFDM	20 Ms / 54 Mb

Table 1.2: LAN and PAN main features

As far as Local Area Networks (LAN) and Personal Area Networks (PAN) concern, we summarize the main characteristics in Tab. 1.3. As we can see in Tab. 1.2, new communication systems trend to increase bit rate and complexity of the modulation schemes and frequency bands, resulting in more challenging designs.

	Radio Systems	**RF Frequency**	**Modulation**	**Bit Rate (/s)**
1G	NMT /AMPS / TACS	0.9 GHz	FM	-
	CTI	0.9 GHz	FM	-
2G	GSM / DCS	0.9/1.8 GHz	GMSK	0.27 Ms/0.01Mb
	CDMAone (IS-95)	0.9/1.8 GHz	QPSK	1.2Ms / 0.1 Mb
	D-AMPS(IS54)/TDMA(IS136)	0.9/1.8 GHz	π/4 DQPSK	0.05Ms/0.01Mb
	DECT	1.8 GHz	GFSK	1Ms / 1Mb
2.5G	GPRS	0.9 GHz	GMSK	0.27 Ms / 0.1Mb
	EDGE	0.9/1.8 GHz	8 PSK	0.27 Ms / 0.38 Mb
3G	UMTS (WCDMA)	2 GHz	QPSK	3.8 Ms / 2Mb
	UMTS HSDPA	2 GHz	16 QAM	3.8 Ms / 10 Mb
	CDMA2000	0.9/1.8 GHz	QSPSK	1.2Ms / 0.3 Mb
	TD-CDMA (UTRA TDD)	2GHz	QPSK	1.2Ms / 2Mb

Table 1.3: Wireless standards and radio systems

1.4.1.2 Transmission Power Control

Transmission power control is used fundamentally in CDMA systems and is vital for capacity and performance in cellular communication systems where all users transmit on the same frequency and high interference is always present due to frequency reuse. Internal interference generated by the system is the most significant factor in determining system capacity and quality of service (QoS).

The basic intent is to control the transmission power in such a way that the interference between users is limited while maintaining link conditions. These conditions are continuously changing as the mobile station moves.

Control power is performed to alleviate the called ‘near-far effect’ (in which the near user can overpower the far user) in such a way that the received mean powers of different mobile stations are equal in the base station, taking into account the varying conditions in the link (such as fading, attenuation…). Uplink (from mobile station to base station) power control is critical for the capacity of CDMA system [Gilh91]. The requirement of the dynamic range of uplink power control can be of the order of 80 dB. Our transmitter, in the perspective of multistandard has to perform this power control. Power amplifier alone handles about 35 dB, a need of a system extending the power range to the 80 dB total transmitter dynamic range seems to be essential [3GPP01].

1.4.2 Low Cost and Low Complexity: Toward Full Digital Transmitters

In addition to integration cost savings, fewer components in the system lead to lower complexity. The topology and design are more compact than if several transmission chains are considered. Thus, we think that a digital approach offers several advantages over of analog implementations because of the easy predictability of digital blocks, the more reliability and more immunity to environmental factors and frequency agility, all of that added to less consumption and size reduction. Moreover, this digital transmitter would be suitable for wideband communications because of the non-limitation in bandwidth of the digital components.

1.5 Conclusion

A good understanding of the main parameters which enable to characterize power amplifiers is essential to know the limitations and trade-off existing in the design of PAs for actual communications systems. To overcome this limitation, several techniques have been studied and presented in this chapter, each of them with its advantages and drawbacks.

It is evident that a good solution for multimode transmitters is necessary nowadays for new emerging standards. The best solution should be a combination of several techniques. A topology based on sampling techniques would lead to a simple and reconfigurable solution. Phase and envelope separation in which two paths are processed separately and amplitude is eliminated simplifies the design of the blocks and lower frequencies (so lower consumption) are possible due to baseband sampling. In the perspective of a wideband transmitter, no feedback system, which limits the bandwidth, will be considered. Finally, one solution reducing silicon area would be preferred.

Our objective in this research is the implementation of a wideband transmitter able to support all the communication standards and applications that require linear and efficient amplification. The proposed transmitter architecture is presented and studied in chapter 2.

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Chapter 2 Multistandard Transmitter Architecture

2.1 Introduction

In this section, we propose a new architecture for efficient amplification of varying envelope signals. This technique is based upon a homodyne IQ transmitter and the EER technique. Fig. 2.1 shows a homodyne transmitter in which the baseband IQ signals are upconverted directly to the RF avoiding multiple synthesizers as in heterodyne systems.

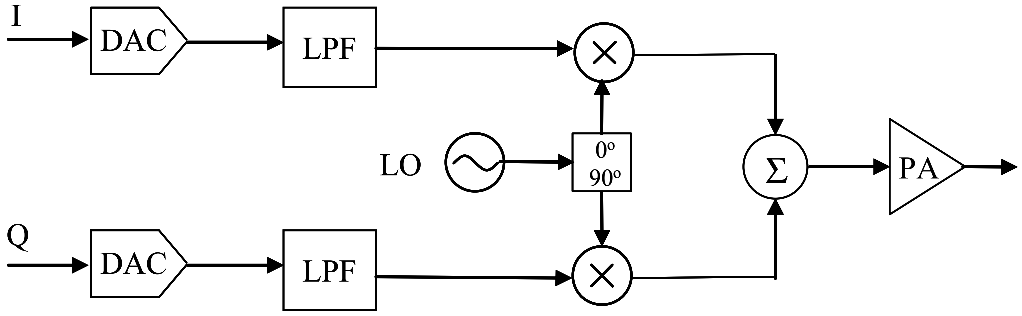
I
DAC
LPF
LO
0°
90°
Σ
PA
Q
DAC
LPF

Figure 2.1: Homodyne transmitter

In Fig. 2.2, the block schema of an EER transmitter is depicted. This method uses the separation of the envelope and phase signals by the means of respectively an envelope detector and a limiter and recombination through the power supply of the power amplifier (modelled as an ideal multiplier).

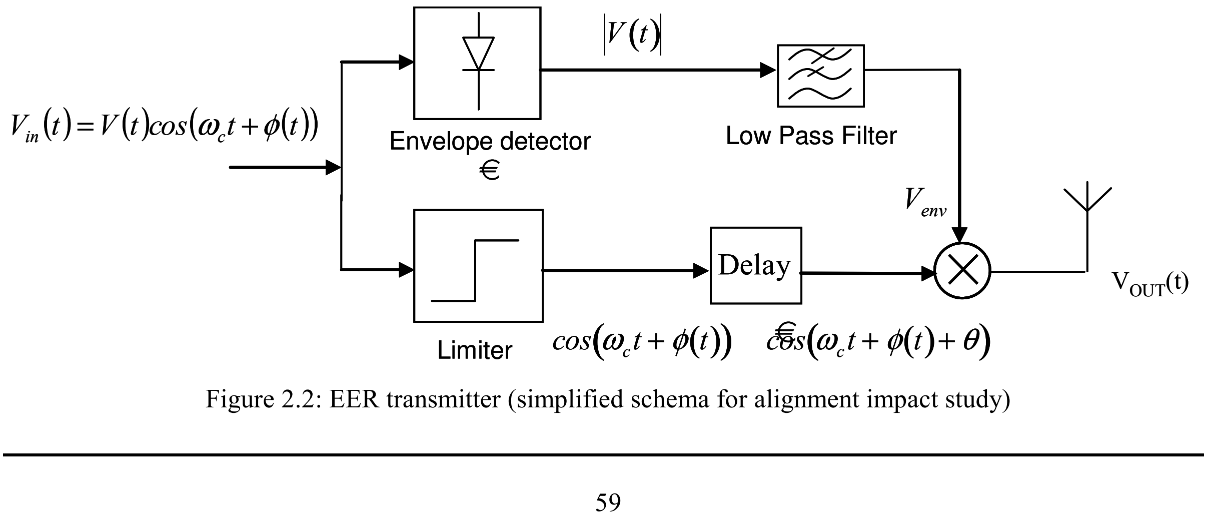
$|V(t)|$
$V_{in}(t)=V(t)cos(\omega_c t+\phi(t))$
Envelope detector
€
Low Pass Filter
V_{env}
Delay
$V_{OUT}(t)$
Limiter
$cos(\omega_c t+\phi(t))$
$cos(\omega_c t+\phi(t)+\theta)$

Figure 2.2: EER transmitter (simplified schema for alignment impact study)

The main drawbacks of these techniques are:

- IQ imbalance of quadrature modulator.
- Differential delay between the two paths leading to an imperfect recombination in EER transmitters.

They are described in the following sections.

2.1.1 IQ Imbalance of Quadrature Modulator

The solution explored in this work is a homodyne transmitter. The baseband phase signals, together with the coded envelope are converted to RF by a quadrature modulator.

A conventional IQ modulator is shown in Fig. 2.3.

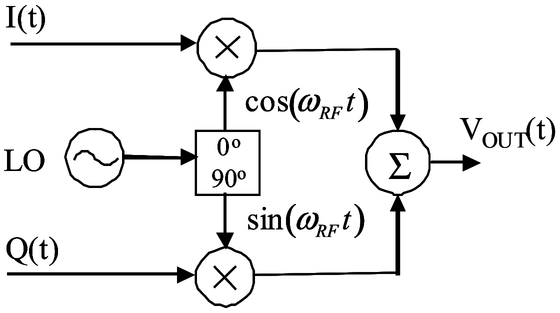

Figure 2.3: IQ Modulator

The IQ modulator output can be written as:

$$V_{OUT}(t) = I(t)\cos(\omega_{RF} t) - Q(t)\sin(\omega_{RF} t) = A(t)\cos(\omega_{RF} t + \varphi(t)) \tag{2.1}$$

where

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2.2}$$

and

$$\varphi(t) = \arctan\left(\frac{Q(t)}{I(t)}\right) \tag{2.3}$$

Assuming sine-wave baseband signals of pulsation ω_{BB}, the output of an ideal converter is a pure single tone signal of pulsation $\omega_{BB} + \omega_{RF}$. The major drawback of this structure is the high sensitivity to mismatches:

- Mismatch between gain and phase of the two signals paths.
- Mismatch between gain and phase of local oscillator signals.

Mismatch of the IQ signals are defined in eqns. 2.4-2.5.

$$I(t) = G\cos(\omega_{BB}t + \phi) + D \tag{2.4}$$

$$Q(t) = \sin(\omega_{BB}t) \tag{2.5}$$

where G is the gain error, ϕ is the phase error and D the DC offset error.

Mismatch of LO quadrature signals in the modulator can be written:

$$CLK_{LOI} = C\cos(\omega_{RF}t + \theta) + E \tag{2.6}$$

$$CLK_{LOQ} = \sin(\omega_{RF}t) \tag{2.7}$$

where C is the gain error, θ is the phase error and E the DC offset error.

These errors in the converter result in a mix of the image and the desired signal. Using eqns. 2.3-2.7, the expression of the output signal as a function of the input signals is detailed.

$$\begin{aligned} V_{OUT}(t) &= I(t).CLK_{LOI}(t) - Q(t).CLK_{LOQ} \\ &= [G\cos(\omega_{BB}t + \phi) + D].[C\cos(\omega_{RF}t + \theta) + E] + \sin(\omega_{BB}t).\sin(\omega_{RF}t) \\ &= \frac{1}{2}[CG\cos(\theta + \phi) + 1]\cos(\omega_{RF}t + \omega_{BB}t) - \frac{CG}{2}\sin(\theta + \phi)\sin(\omega_{RF}t + \omega_{BB}t) \\ &\quad + \frac{1}{2}[CG\cos(\theta - \phi) - 1)]\cos(\omega_{RF}t - \omega_{BB}t) - \frac{CG}{2}\sin(\theta - \phi)\sin(\omega_{RF}t - \omega_{BB}t) \\ &\quad + DC\cos(\omega_{RF}t + \theta) + EG\cos(\omega_{BB}t + \theta) + ED \end{aligned} \tag{2.8}$$

This expression shows two spurious signals at frequencies nearby the desired signal (see Fig. 2.4).

- LO leakage at frequency ω_{RF} with a power equal to:

$$P_{leakage\_LO} = (CD)^2 \tag{2.9}$$

- Image signal at frequency $\omega_{RF}-\omega_{BB}$ with a power of

$$P_{image}=\frac{1}{4}\left[C^2G^2-2CG\cos(\theta-\varphi)+1\right] \tag{2.10}$$

The desired signal at the desired frequency f_{RF} has a power value written in the following expression:

$$P_{signal}=\frac{1}{4}\left[C^2G^2+2CG\cos(\theta+\varphi)+1\right] \tag{2.11}$$

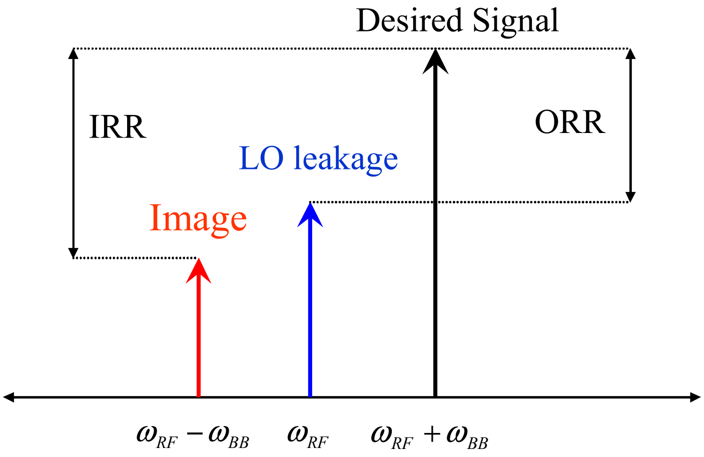

Figure 2.4: IQ up-converter Output Spectrum

The Image Rejection Ratio (IRR) is defined as the ratio of the RF signal level to the image frequency, which is usually expressed in dBc [Wind04] and is one of the important parameters in IQ transceivers.

$$IRR=10\log\left(\frac{C^2G^2-2CG\cos(\theta-\varphi)+1}{C^2G^2+2CG\cos(\theta+\varphi)+1}\right) \tag{2.12}$$

The Oscillator Rejection Ratio (ORR) is the ratio of the LO leakage signal to the desired signal in dBc.

$$ORR=10\log\left(\frac{4C^2D^2}{C^2G^2+2CG\cos(\theta+\varphi)+1}\right) \tag{2.13}$$

where D is the DC offset defined in eqn. 2.4 and the phase error in quadrature baseband signals.

In spite of the difficult realization of 90° phase shifters in direct-conversion architectures, phase imbalance of 1-2° and amplitude imbalance of 1-2% are achievable, resulting in LO and image signals of -30 to -40 dBc which involve an acceptable spurious level in present communication standards [Raza97]. The design of a new full digital IQ transmitter with a simple 90° phase shifter is proposed instead of a classic IQ transmitter in § 2.6. This modulator is one of the major contributions of this work.

2.1.2 Differential Delay in EER-type Systems

The proposed transmitter is based on the EER technique. One of the most important drawbacks of EER-type systems is the desynchronization of the different paths. In an EER system, the phase and magnitude paths are amplified separately, differences between the group delay in the envelope and carrier channels (differential delay) results in imperfect reconstruction of the output signal and therefore distortion. The mismatch effect between envelope and phase signals produces noise in the transmitted symbols and constellation rotation, causing significant spectral regrowths as shown in next equations.

For the ideal case, the transmitted signal is:

$$\begin{aligned} V_{out}(t) &= V_{env}(t)V_{phase}(t) = V_{env}(t)\cos(\omega_{RF}t+\phi(t)) \\ &= V_{env}(t)\cos(\phi(t))\cos(\omega_{RF}t) - V_{env}\sin(\phi(t))\sin(\omega_{RF}t) \\ &= I(t)\cos(\omega_{RF}t) - Q(t)\sin(\omega_{RF}t) \end{aligned} \tag{2.14}$$

If a differential delay θ exists between the two signal paths, then the transmitted signal can be written as:

$$\begin{aligned} V_{out}^{'}(t) &= V_{env}(t)\cos(\omega_{RF}t+\phi(t)+\theta) \\ &= V_{env}(t)\left[\cos(\phi(t))\cos\theta - \sin(\phi(t))\sin\theta\right]\cos(\omega_{RF}t) \\ &\quad -V_{env}\left[\sin(\phi(t))\cos\theta + \cos(\phi(t))\sin\theta\right]\sin(\omega_{RF}t) \\ &= \left[I(t)\cos\theta - Q(t)\sin\theta\right]\cos(\omega_{RF}t) - \left[Q(t)\cos\theta + I(t)\sin\theta\right]\sin(\omega_{RF}t) \\ &= I^{'}(t)\cos(\omega_{RF}t) - Q^{'}(t)\sin(\omega_{RF}t) \end{aligned} \tag{2.15}$$

Thus, as we can see in eqn. 2.15, the constellation is rotated by an angle θ related to the ideal constellation expressed as ideal baseband signals $I(t)$ and $Q(t)$.

A study is done to determine the impact of this desynchronization in communications standards. The schema considered is shown in Fig. 2.2 based on an EER transmitter and the input signal is supposed to be already upconverted to RF for simplicity. The aim is to study the maximum tolerated delay in this type of systems and the relation with the needed bandwidth in the envelope path. The topology depicted in Fig. 2.2 is simulated with ADS for different input signals. When no mismatch is considered in the transmitter, the minimum envelope bandwidth is about two times the bandwidth of the RF signal (see eqn. 2.25). If a differential delay θ is introduced in the system, the needed envelope bandwidth must be increased for the same linearity performances to compensate for the phase error as shown in Tabs. 2.1-2.2, for EDGE and CDMA2000 standards. In a real topology where the envelope bandwidth is kept constant, the maximum tolerated delay decreases and is inversely proportional to the bandwidth of the RF signal.

EDGE					
Delay (µs)	0	0.5	1	1.5	2
BW (kHz)	500	600	800	1000	1500

Table 2.1: Minimum Envelope Bandwidth vs. Delay in EDGE

CDMA2000					
Delay (ns)	0	10	20	30	40
BW (MHz)	2.5	3	3.5	4	4.5

Table 2.2: Minimum Envelope Bandwidth vs. Delay in CDMA2000

In order to relax the bandwidth constraint in EER-type systems and to reduce the mismatch effect in this type of topologies, a wideband envelope coder based on a Sigma-Delta modulation is employed in our proposed transmitter architecture.

2.1.3 Proposed Transmitter Architecture

We consider a new transmitter architecture. This method uses the separation of the envelope and phase signals and recombination before the power amplifier, with the use of a bandpass filter at the output to restore the RF signal and to filter the noise. This technique is depicted in Fig. 2.5.

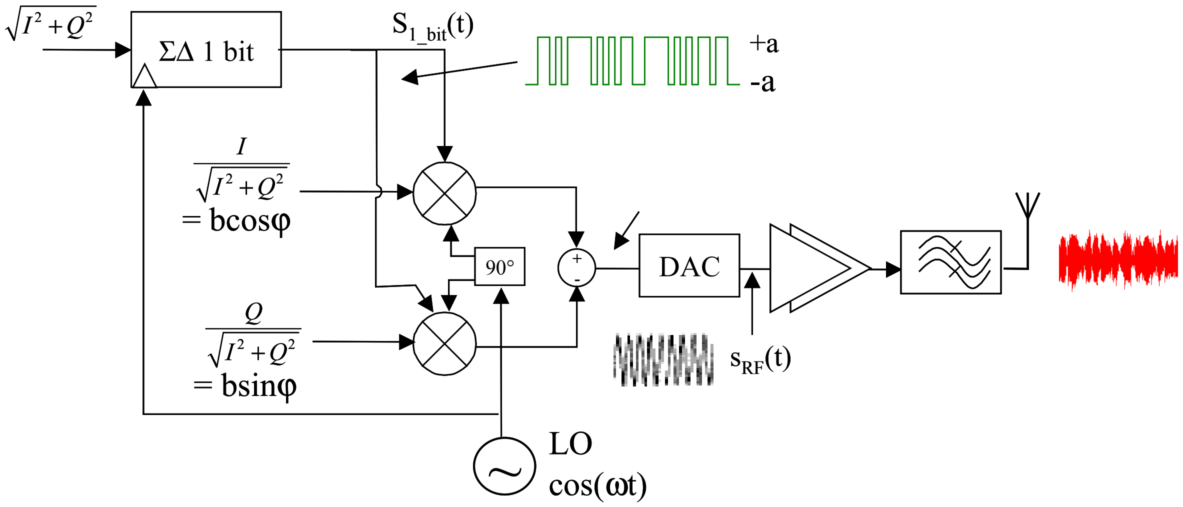

Figure 2.5: Initial Transmitter Architecture

This novel architecture involves an important evolution of the EER method. As it is known, any baseband signal can be split into its envelope and phase components (eqn. 2.16). The approach is quite different from a classic EER method as two quadrature phase signals are employed and recombination is done by a combiner instead of using the drain of the power amplifier to inject the filtered coded envelope (Class-S amplifier and LC filter). Here, the ΣΔ modulator is used to code the envelope and no filter is placed at the output of the modulator as in EER systems. The separation of the signal is neither into Polar Components nor Cartesian. More exactly, it can be considered like a conventional IQ transmitter where IQ signals are normalized by the envelope (only phase information) and the mixers before amplification restore the envelope.

$$S_{BB}(t) = I(t) + jQ(t) = \left(\sqrt{I(t)^2 + Q(t)^2}\right)\left(\frac{I(t)}{\sqrt{I(t)^2 + Q(t)^2}} + j\frac{Q(t)}{\sqrt{I(t)^2 + Q(t)^2}}\right) \tag{2.16}$$

The baseband signal ($I(t) + jQ(t)$) is splitted into its envelope ($\sqrt{I(t)^2 + Q(t)^2}$) and phase ($I(t)$ and $Q(t)$ normalized by the envelope) components, then, the envelope is coded with a pulse density modulator 1-bit Sigma-Delta. The output of this coder can be expressed as:

$$S_{1-bit}(t) = \mathrm{a}\sum_{\mathrm{i,k}} \Pi_{\alpha_i T_{\Sigma\Delta}}\left(t - k\alpha_i T_{\Sigma\Delta}\right) = aMod\left(t, \alpha_i T_{\Sigma\Delta}\right) \tag{2.17}$$

where $\Pi_{\alpha_i T_{\Sigma\Delta}}(t)$is the rectangular function of duration $\alpha_i T_{\Sigma\Delta}$. Parameter α_i depends on the coded value of the envelope x_i and is greater or equal to 1.

$$\alpha_i = F(x_i) \tag{2.18}$$

$T_{\Sigma\Delta}$ is the sigma delta sampling period. For simplicity this signal is rewritten as a signal with amplitude a and phase function $Mod(t, \alpha_i T_{\Sigma\Delta})$.

The coded envelope and the constant amplitude (equal to b) phase signals are upconverted to RF frequency by the IQ modulator (local oscillator) and recombined in order to obtain a constant envelope signal $S_{RF}(t)$ (see Fig. 2.5). As we can see in eqn. 2.19, output signal is phase-modulated with constant amplitude.

$$\begin{aligned} S_{RF}(t) &= \left[\mathrm{a}\left(\mathrm{b}\cos(\omega t)\cos\varphi - \mathrm{b}\sin(\omega t)\sin\varphi\right)\right]Mod\left(t, \alpha_i T_{\Sigma\Delta}\right) \\ &= \mathrm{abcos}\left(\omega t + \varphi + Mod\left(t, \alpha_i T_{\Sigma\Delta}\right)\right) \end{aligned} \tag{2.19}$$

The benefit of this transmitter is the generation of a constant envelope signal, which is amplified by any type of power amplifier in an efficient way. The noise from the ΣΔ coder is removed by a bandpass filter before transmission. This topology represents the best trade-off to use for multistandard purposes because of its simplicity, wide bandwidth (there is no feedback system from output to input and the coder is wide band) and reconfigurability.

2.2 Baseband Signals in the Transmitter

In this section, every block in the transmitter is described.

2.2.1 Envelope/Phase Generation

In order to avoid degradations related to the envelope detector and a limiter, digital generation is preferred. Data bit stream is mapped to generate complex symbols (QAM in Fig. 2.6).

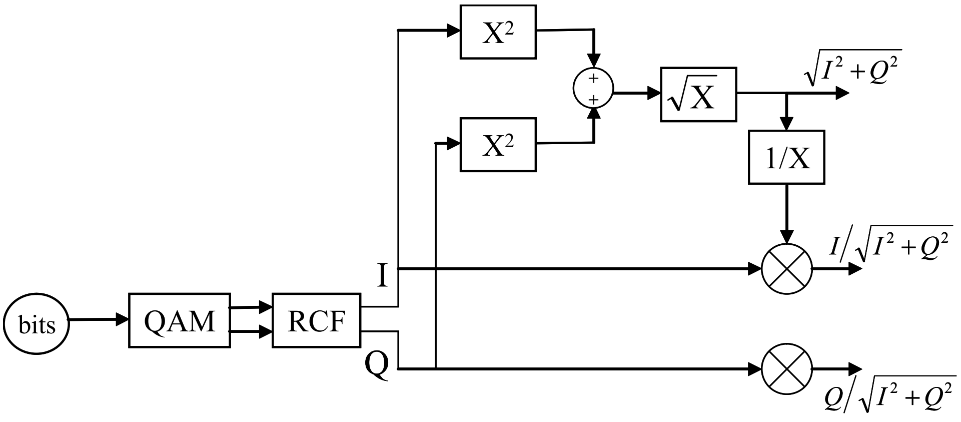

Figure 2.6: Amplitude and phase generation and separation

Then, this signal is upsampled and filtered by a Raised-Cosine transmit Filter (RCF in Fig. 2.6) to generate an IQ signal. Envelope and phase separation is calculated mathematically by using IQ signals. Complex algorithms based on CORDIC cores (Xilinx) and implemented in FPGA enables to calculate the square root. This baseband digital processing consists in modulating digital input data into an amplitude vector and in-phase and quadrature vectors normalized by the amplitude. As the square root is a nonlinear operation, envelope and phase signals are bandwidth wider than the respective complex signal. It has been shown and proved in precedent works that the envelope and phase signals can be quantized using 9-bit. That represents the minimum number of levels needed to respect the Error Vector Magnitude (EVM) requirements for the new standards [Hibo06PhD].

2.2.2 Phase Channel

The major problem of this part of the architecture is the wide bandwidth of these signals. It involves the necessity of a low-pass filter.

The effect of this phase filtering is detailed in next paragraphs. (see Fig. 2.7).

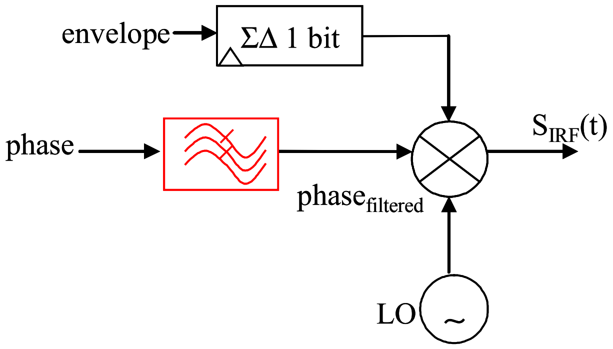

Figure 2.7: Phase Filtering (only one phase path considered)

This filter is modelled by a rectangular function in the frequency domain with amplitude equal to 1 and with cut-off frequency f_{ph}. In the time domain this expression represents a sinus cardinal.

$$\Pi_{f_{ph}}(f) = TF\{2f_{ph}\sin c(2\pi f_{ph}t)\} \tag{2.20}$$

If we consider an ideal multiplier with unfiltered phase signal, the output signal can be expressed as (only one path is considered):

$$S_{IRF}(t) = phase(t).envelope(t).lo(t) \tag{2.21}$$

The Fourier Transform of the expression in eqn. 2.21 yields to:

$$S_{IRF}(f) = Phase(f) * Envelope(f) * LO(f) \tag{2.22}$$

However, when phase filtering is considered, we obtain:

$$\begin{aligned} S_{IRF}(f) &= Phase_{filtered}(f) * Envelope(f) * LO(f) = \\ &= \left[Phase(f).\Pi_{fph}(f)\right] * Envelope(f) * LO(f) \end{aligned} \tag{2.23}$$

Inverse Fourier Transform (TF^{-1}) of eqn. 2.23 enables to calculate the expression of the transmitted phase signal as a function of the ideal spectrum of $phase(t)$ and $envelope(t)$.

$$S_{IRF}(t) = envelope(t).lo(t).phase(t) * \left(2f_{ph}\sin c(2\pi f_{ph}t)\right) \tag{2.24}$$

The impact of filtering phase can be seen as the convolution of the continuous time signal with a sinus cardinal.

As it is shown in [Hibo06PhD], the minimum bandwidth needed to match the mask requirements in 802.11a after phase filtering is about 70 MHz. For UMTS case, the estimated minimum bandwidth is about 25 MHz. It is important to note the importance of anti-alias filters in this kind of architectures to turn unlimited phase signals into bandlimited signals.

2.2.3 Envelope Channel

The same problem of unlimited band is presented in this path (Fig. 2.8). Envelope filtering involves the convolution of the time signal with a sinus cardinal.

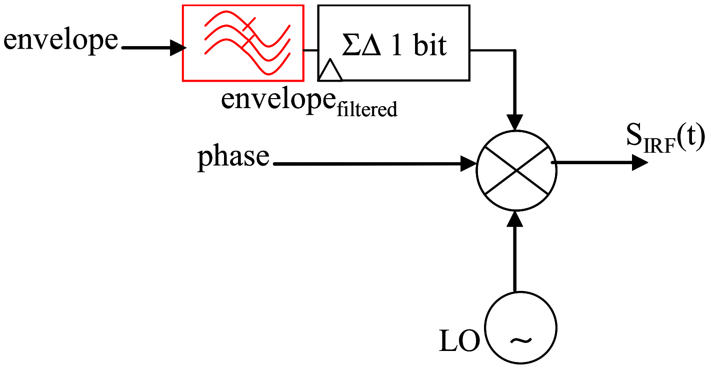

Figure 2.8: Envelope Filtering (only one phase path considered)

As an evolution of the EER transmitter, our architecture uses an envelope detector (digitally implemented in this research), which is a circuit that (ideally) takes the absolute value of its input, and then passes the result through a low-pass filter (same filter as in Fig. 2.7). The output from this low pass filter is the required envelope signal (see Fig. 2.8). As we can see in Fig. 2.9, high frequencies are attenuated.

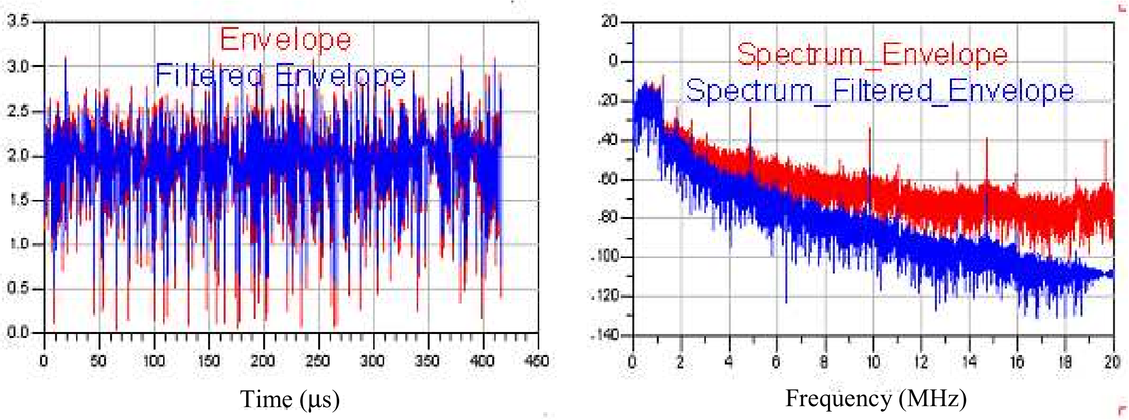

Figure 2.9: Time and frequency domains of the envelope and the filtered envelope

The absolute value operation, being non-linear, must generate some new frequency components. Among them are those of the wanted envelope but this signal is wider than the baseband signal. It is the purpose of the low-pass filter to separate the wanted from the unwanted components generated by the absolute value operation to limit the envelope bandwidth. This filtered signal drives the envelope modulator (1-bit ΣΔ). This modulator samples the input bandwidth at a frequency, which is a multiple factor (Oversampling Ratio, OR) of this input bandwidth so if the signal has wide bandwidth, the performance of the modulator decreases drastically as, for a constant sampling frequency in the coder, the corresponding OR drops-off.

We want to study the effect of the filtered envelope signal on ACPR performance under several standard specifications (EDGE, CDMA, UMTS and 802.11a) due to filtering, there will be phase shifts and attenuation of the high-frequency components of the envelope signal that result in improper reconstruction of the output signal, and hence distortion. We intend to obtain the minimum signal envelope bandwidth (BW_{env}) so as to match the ACPR requirements**.**

Different signals are simulated with ADS and the results are summarized in Tab.2.3.

	EDGE	**CDMA2000**	**UMTS**	**802.11a**
BW_{ENV}	500kHz	5MHz	10MHz	40MHz
ACPR (dBc)	-35@200kHz	-46@900kHz	-34@5MHz	-32@20MHz

Table 2.3: Minimum envelope bandwidth vs. ACPR

The required minimum occupied bandwidth of the envelope of a signal (if only filtering effect is considered) is about twice the RF signal bandwidth.

$$BW_{ENV} \cong 2.BW_{RF} \tag{2.25}$$

2.3 Sigma-Delta Modulation

After being converted into the digital domain, envelope signal is coded by a 1-bit full-digital ΣΔ modulator to convert the envelope into a two-level signal (see Fig. 2.5). This 1-bit binary signal enables the use of a simple IQ mixer as will be explained in § 2.6.

Before detailing the principle of operation of this important functional block in the transmitter, a brief explanation of the Analog-to-Digital Converter (ADC) is given in following paragraphs in order to better understanding of the procedure utilized in this work.

2.3.1 Principle of Operation of ADC

In a classic transmitter chain, the baseband signal is filtered by an anti-alias filter to limit its spectral components. This filter leads to a bandlimited signal with bandwidth between [-BW, BW]. This analog signal is converted in the digital domain by an ADC with sampling frequency f_s, resulting in a signal whose spectrum, together with the quantification noise, is depicted in Fig. 2.10. The noise is normally modelled by a white noise (uniform Power Spectral Density PSD). The in-band noise power determines the ADC resolution and is defined by the Signal to Noise Ratio (SNR). Before introducing the oversampled converters, two important parameters must be defined:

- Quantization noise
- Signal to Noise Ratio (SNR)

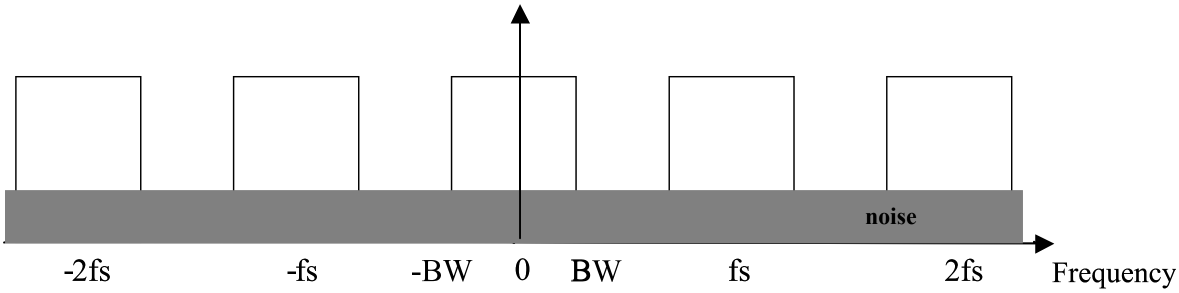

Figure 2.10: ADC output spectrum

2.3.1.1 Quantization Noise

Quantization is a correspondence between the continuous input voltage signals and the discrete output values called quantization levels. The smallest step is the quantization level Δ, which is a function of the data converter's number of bits B and the amplitude range of the converter.

$$2V_{\max} = \Delta 2^{B} \tag{2.26}$$

In uniform quantization, which is the most used type, we have:

$$\begin{cases} x_i - x_{i-1} = \Delta \\ x_i^{'} - x_{i-1}^{'} = \Delta \\ e = x_i^{'} - x_i \end{cases} \tag{2.27}$$

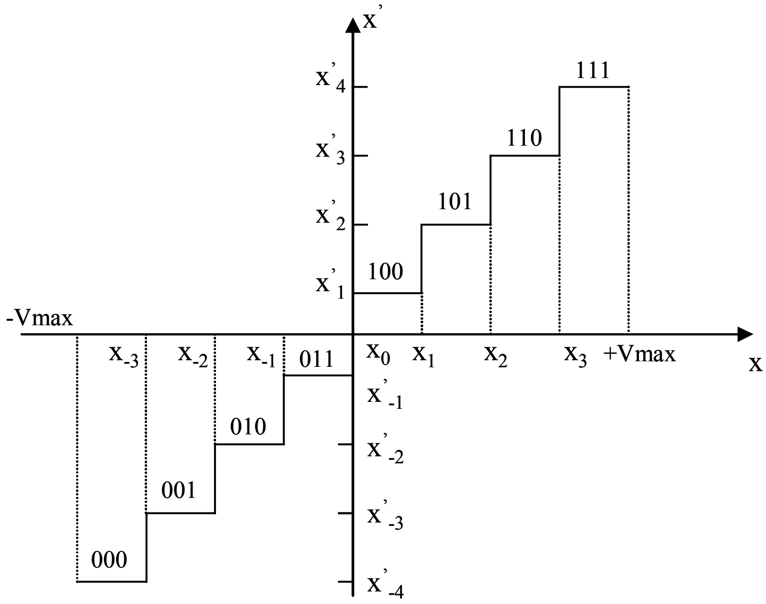

Figure 2.11: Input-Output characteristic of a 3-bit quantizer

The difference between the quantized signal and the input signal is called quantization noise (*e* in eqn. 2.27). Quantization noise is inherent to the quantization process, this noise is supposed to be additive, wideband and independent of the input signal when the number of levels is high enough (usually greater than 16). In the case of the studied quantizer in Fig. 2.11, the noise uniform distribution function is illustrated in the following figure:

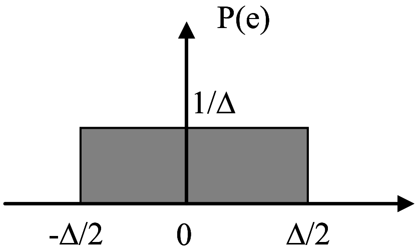

Figure 2.12: Uniform distribution function of the quantization noise

The variance in this case can be expressed:

$$\sigma^2{}_e = \frac{1}{\Delta} \int_{-\Delta/2}^{+\Delta/2} P(e)^2 \, de = \frac{\Delta^2}{12} \tag{2.28}$$

Assuming that the random process will not change its statistical properties with time (a stationary ergodic process is considered), noise power P_e is equal to the variance.

$$P_e = \int_{-fs/2}^{+fs/2} \Phi_e(f)\, df = \frac{\Delta^2}{12} \qquad (2.29)$$

The hypothesis of white noise involves PSD function over the band frequency $[f_s/2, f_s/2]$ of a value:

$$\Phi_e(f) = \frac{\Delta^2}{12 f_s} \qquad (2.30)$$

2.3.1.2 Signal to Noise Ratio

Signal to Noise Ratio (SNR) illustrates the spectral purity of a signal over a given frequency band W and is defined as the ratio of the signal power to the noise power.

$$\mathrm{SNR} = \frac{\text{Signal Power}}{\text{Noise Power}} = \frac{\int_{-W}^{W} |X(f)|^2 df}{\int_{-W}^{W} \Phi_e(f)\, df}. \qquad (2.31)$$

This concept is related to the data converter's number of bits number B. Using eqns. 2.26 and 2.29, the quantization noise power is:

$$P_e = \frac{\Delta^2}{12} = \frac{V_{max}{}^2}{3.2^B} \qquad (2.32)$$

To compute the SNR, a full-scale (maximum amplitude equal to V_{max}) continuous sine wave is considered. Hence, the signal power is $V_{\max}^2/2$.

$$SNR = \frac{3}{2} 2^{2B} \frac{V_{\max}^2}{V_{\max}^2} \qquad (2.33)$$

Eqn. 2.33 in dB allows giving the well-known expression of the SNR for sinus waves taking into account a quantizer with fixed number of bits. For each extra bit of resolution in the ADC, there is an improvement of about 6 dB in SNR.

$$\mathrm{SNR} \approx 1,76 + 6,02\mathrm{B} \qquad (2.34)$$

2.3.2 Oversampled Converters

In Nyquist rate converters, signal is sampled at twice the maximum input frequency (Shannon Theorem) and the noise falls near the interest band signal.

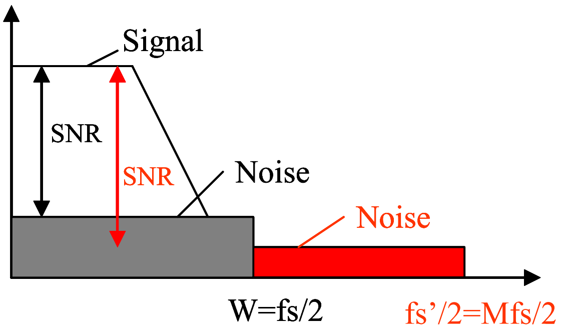

Figure 2.13: Output spectrums of Nyquist rate and oversampled converters

Generally, converters sample the input signal at a higher rate than the Nyquist frequency ($f_s' = Mf_s$) where M is the oversampling ratio. The goal is to change the frequency distribution of the noise power reducing the fraction of the noise power falling in the band of interest [-W, W] as shown in Fig, 2.13.

The noise power in the case of an oversampled converter can be computed as:

$$P_e^{over} = \int_{-f_s/2}^{+f_s/2} \Phi_e^{over}(f)df = \frac{2W\Delta^2}{12 f_s'} = \frac{\Delta^2}{12M} \qquad (2.35)$$

where $\Phi_e^{over}(f)$ is the PSD function of the oversampled converter.

To decrease the noise power, either the number of bits B is increased leading a more complex system or oversampling ratio M, which implies an overconsumption. For every increment in M of a factor of two, the SNR improves about 3dB.

$$\text{SNR} \approx 1{,}76 + 6{,}02\text{B} + 10\log(M) \qquad (2.36)$$

In addition of oversampling, ADCs can be designed to incorporate noise shaping obtaining high in-band resolution [Aziz96]. The aim is to maximize the SNR in the band leaving the signal undisturbed (signal transfer function STF) and attenuate the noise in the signal band pushing it to high frequencies (noise transfer function NTF). This process is called Sigma-Delta modulation (ΣΔ).

2.3.3 ΣΔ Noise-Shaping ADC

In this work, the proposed architecture employs a 1-bit ΣΔ modulator to code the digital baseband envelope signal to a switched-mode (two levels) signal.

The sigma-delta modulator attempts to force the output signal to the input signal in such a way that the modulator output, averaged over a period of time, approximates the input. In the case of a 1-bit coder, if the input signal is close to zero DC, half period time the modulator output will be 1's, half -1's. Higher is the input level, more quantity of 1's outputs the coder and inversely for negative values.

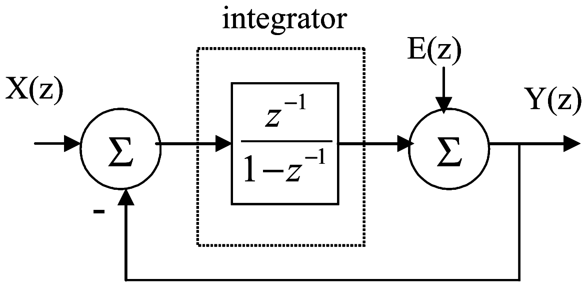

Figure 2.14: Simplified schema of a first-order ΣΔ

Fig. 2.14 shows the block diagram of a first-order sigma-delta modulator, which is chosen to study the ΣΔ modulation for its simplicity. It consists of an integrator (corresponding to the *sigma* term), a quantizer with a noise spectrum E(z) and a substractor (corresponding to the *delta* term) as main blocks.

The modulator input-output characteristic can be represented by the Z-functions as a function of the input signal X(z), output signal Y(z) and the quantization noise E(z) with statistical properties described in § 2.3.1.2.

$$\mathrm{Y}(\mathrm{z}) = \mathrm{z}^{-1}\,\mathrm{X}(\mathrm{z}) + \left(1 - \mathrm{z}^{-1}\right)\mathrm{E}(\mathrm{z}) \tag{2.37}$$

Eqn. 2.37 determines the two different transfer functions: Signal Transfer Function (STF) and Noise transfer Function (NTF).

$$STF(\mathrm{z}) = \frac{Y(\mathrm{z})}{\mathrm{X}(\mathrm{z})} \tag{2.38}$$

$$NTF(\mathrm{z}) = \frac{Y(\mathrm{z})}{\mathrm{E}(\mathrm{z})} \tag{2.39}$$

$$\begin{cases} STF(z) = z^{-1} \\ NTF(z) = 1 - z^{-1} \end{cases} \tag{2.40}$$

Input signal is only delayed throughout the system while a filter whose Z-function is NTF (see Fig. 2.15) shapes noise. A simply generalization can be done for a L-order coder (L integrators) resulting in:

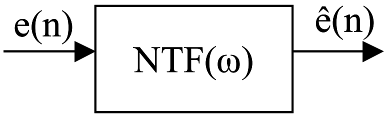

Figure 2.15: Noise shaping in ΣΔ coders

$$\begin{cases} STF(z) = z^{-L} \\ NTF(z) = (1 - z^{-1})^{L} \end{cases} \tag{2.41}$$

The normalize digital pulsation ω in radians is defined as

$$\omega = \frac{2\pi f}{f_{\Sigma\Delta}} \tag{2.42}$$

where $f_{\Sigma\Delta}$ is the sampling frequency of the ΣΔ coder. Then, we can define:

$$z = e^{j\omega} \tag{2.43}$$

We are interested in the determination of the magnitude of the filtered noise by the NTF function. Combining eqns. 2.23-2.25, 2.33 and 2.36 with the statistical properties of quantization noise (see § 2.3.1.2), we obtain the Power Spectral Density (PSD) of the shaped noise:

$$\Phi_{\hat{e}\hat{e}}(e^{j\omega}) = \sigma_e^2 \left| NTF(e^{j\omega}) \right|^2 \tag{2.44}$$

and consequently:

$$\left| NTF(e^{j\omega}) \right|^2 = NTF(e^{j\omega}).NTF(e^{j\omega})^* = \left(1 - e^{-j\omega}\right)\left(1 - e^{j\omega}\right) = (2\sin((\omega/2))^2 \tag{2.45}$$

It can be shown for the case of an L-order modulator:

$$\left|NTF(e^{j\omega})\right|^2 = NTF(e^{j\omega}).NTF(e^{j\omega})^* = \left(1-e^{-j\omega}\right)^L\left(1-e^{j\omega}\right)^L = (2\sin((\omega/2))^{2L} \quad (2.46)$$

and using eqn. 2.42, we have the expression of the PSD of the shaped noise:

$$\Phi_{\hat{e}\hat{e}}(e^{j\omega}) = \sigma_e^2(2\sin((\omega/2))^{2L} \quad (2.47)$$

As it has been depicted in Fig. 2.13, if no shaping filter is utilized, noise power remains constant over the entire range of frequencies. As a result of filtering, noise is pushing from the band signal to high frequencies representing the main problem associated to this type of architectures based on ΣΔ coders because of the spurious limitations imposed by communication standards. In § 2.4, we consider the study of the noise problem in ΣΔ converters.

2.4 Quantized Noise Limitation in ΣΔ Coders

The output signal of a ΣΔ converter is composed of a delayed version of the input signal (the loop filter acts as a low pass filter) and the quantized noise, pushed by a L-order high pass filter into high frequencies. The main drawback limiting the integration of ΣΔ converters in transmitter architectures is the noise shaping (detailed in § 2.3.3). Each communication standard specifies strict requirements with regard not only to out-of-band spurious emissions but also to the adjacent channels. The limitation for the quantization noise close to the carrier (in-band noise) is determined by the spectrum mask requirements.

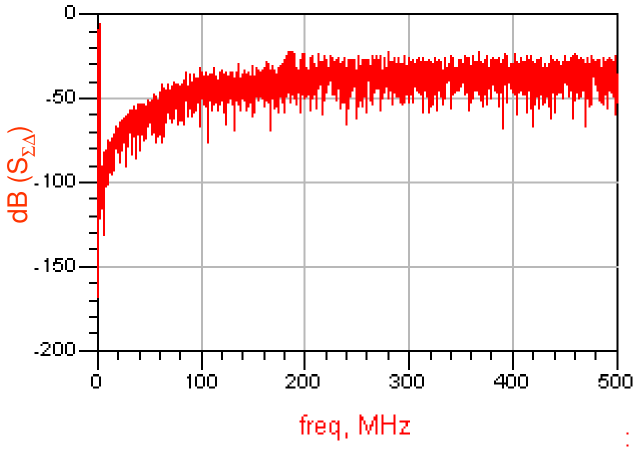

Figure 2.16: Output of 2nd order ΣΔ modulator

Very high levels of quantization noise are generated out-of-band (Fig. 2.16) and these unwanted emissions are reduced by the post-PA filtering in the system (see Fig. 2.5). However, in order to reduce the complexity and insertion losses of this filter, noise attenuation techniques providing spurious suppression must be explored.

2.4.1 In-Band Noise Reduction Techniques

Many solutions are possible to reduce in-band noise maximizing the SNR (eqn. 2.31). One simple form is to increase the sampling frequency (Oversampling Ratio) in the coder. Another means is to use higher order ΣΔ modulator. An alternative consists in placing one or more zeros of the NTF at selected frequencies. Use of multi-bit coders or low-pass filtering at the output (leading to multi-level signals) is not considered to attenuate the quantization noise.

2.4.1.1 Increment of Oversampling Ratio

Oversampled converters extend the band where the quantization noise falls. Upsampling the envelope signal is rather simple to perform for signals not demanding wide bandwidths like in EDGE or CDMA systems (see Tab. 2.2). However, for Orthogonal Frequency-Division Multiplexing (OFDM) envelope signals have bandwidths larger than 40MHz (see eqn. 2.23) and increasing the oversampling ratio results in high sampling frequencies leading to an important overconsumption which is a major limitation for low-power radio transmitters (power consumption being proportional to the square of the sampling frequency). Moreover, clock frequency in the converter is limited by the semiconductor technologies. The proposed architecture takes advantage of coding the low frequency envelope at a low rate.

2.4.1.2 High Order ΣΔ Modulators

The order of a ΣΔ modulator can be increased further to achieve high SNR and reduce the in-band noise floor. PSD of the noise modulator output is plotted in Fig. 2.17 and compared with the order of the ΣΔ converter (L=1, 2, 3).

Frequency is normalized by the sampling frequency ($f_{\Sigma\Delta}$). It can be seen that noise power increases proportionally with the modulator order and is mostly concentrated at high frequencies. However, noise is reduced at low frequencies and the SNR is maximized. At low frequencies, noise power is inversely proportional to the order of the modulator. From DC to $f_{\Sigma\Delta}$ /3, noise slope is 6 dB/octave for L=1, 12 dB/octave for L=2 and 18 dB/octave for L=3. For frequencies greater than f_s/3, the noise in modulator increases with the order. High order ΣΔ converters (L>3) suffer from stability problems and are only conditionally stable. The order of the modulator must be chosen carefully and it represents a trade-off between low in-band noise, high out-of-band quantization noise, stability and implementation complexity.

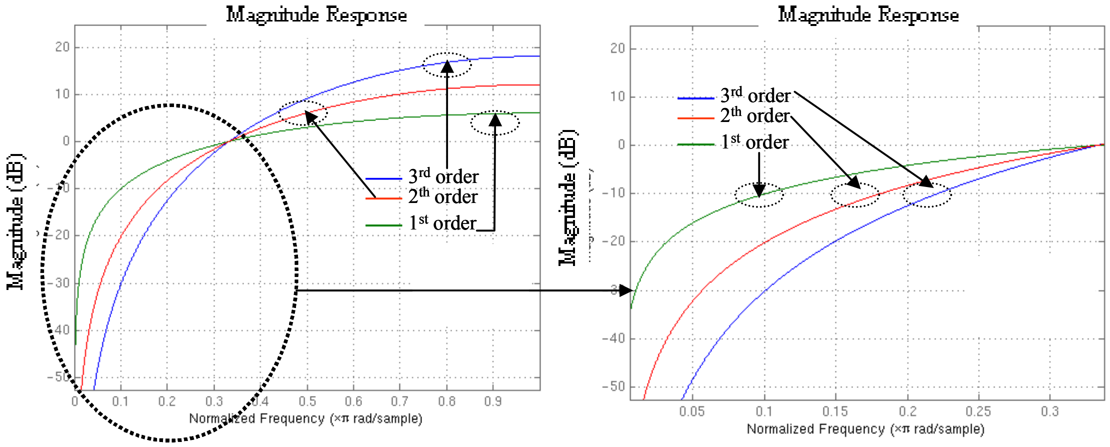

Figure 2.17: Shaped Noise PSD for L=1,2,3

2.4.1.3 Zeros in Frequency

To improve the shaping of the quantization noise, zeros of the noise transfer function can be placed at notch frequencies (f_z) of interest (eqn. 2.48

$$NTF(z) = 1 - 2\cos\left(\frac{2\pi f_z}{f_{\Sigma\Delta}}\right) z^{-1} + z^{-2} \tag{2.48}$$

This technique is detailed in [Nors97]. The notch position is related to the sampling frequency. Normally this frequency is located at the receive band of a given standard. The number of notch frequencies would be dependent of the number of standards we intend to transmit. This leads in a non-reconfigurable system because the notch frequencies cannot be modified dynamically if the sampling frequency is kept unchanged. This method results in Chebyshev-type noise transfer functions, which are more difficult to implement because additional feedback coefficients are required. However, this technique may be useful when a single communication standard is considered.

2.4.2 Out-Band Noise Reduction Techniques

To fulfill the strict requirements of spurious emissions, our architecture relies on the post-PA bandpass filtering. Filtering before the power amplifier (ideal square root cosine filter utilized in simulation in Fig. 2.18) leads to a non-constant envelope signal as depicted in Fig. 2.19. OFDM signal is used as stimuli.

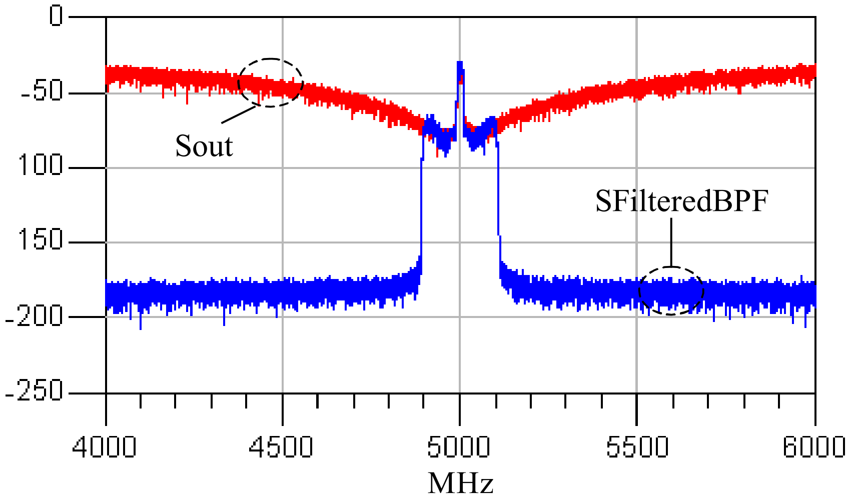

Figure 2.18: Output and filtered spectra

To reduce the out-of-band noise of ΣΔ coder, we propose to use a sample and hold (S&H) interpolator at the output. The interpolation filter up-samples the output coder at a rate $Nf_{\Sigma\Delta}$, where N is the interpolator Oversampling Ratio. The simplest interpolator is a Zero-Order Hold; its sinc function has nulls at integer frequencies of the ΣΔ frequency filtering the digital images.

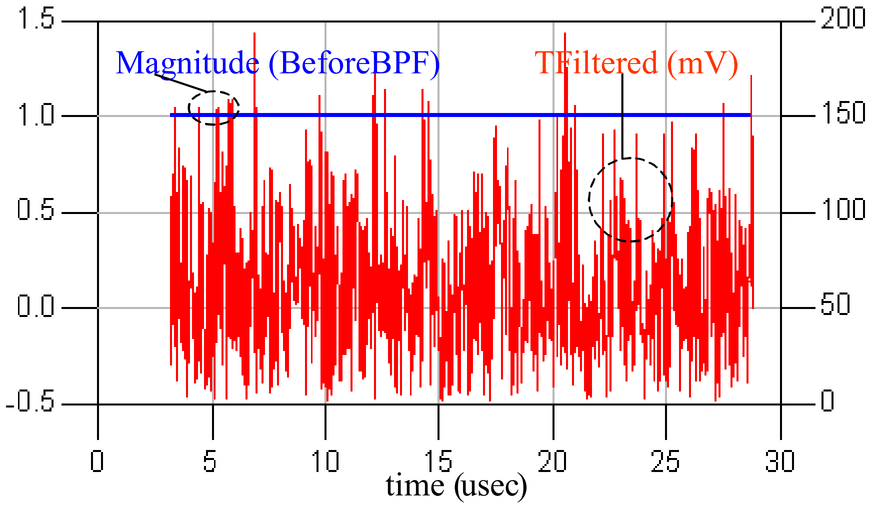

Figure 2.19: Output and filtered timed signals

2.4.2.1 Basics of Zero Order Hold (ZOH) Interpolator

The operation principle of the interpolator can be considered as follows. The interpolator upsamples the input signal by a factor N and inserts N-1 zero-valued samples between two consecutive original samples. A FIR (finite impulse response) filter reduces the output harmonics. This combination results in a simple digital interpolation as shown in Fig. 2.20.

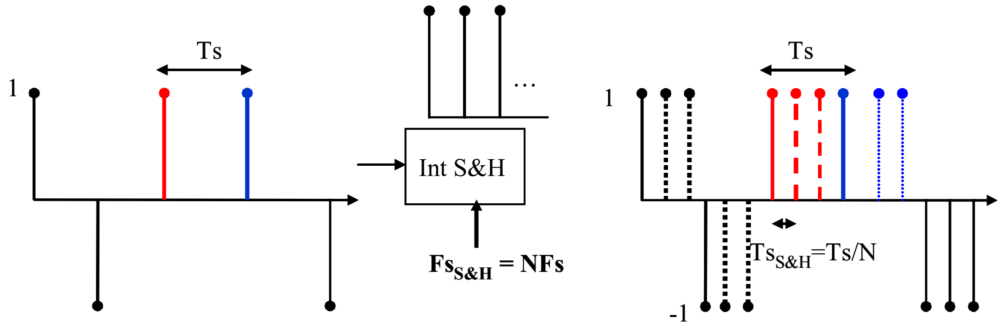

Figure 2.20: S&H Upsampling (N=3)

The impulse response of the S&H interpolator is plotted in Fig. 2.21.

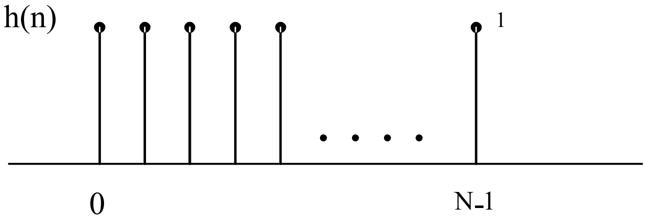

Figure 2.21: Impulse response of S&H

The transfer function of the interpolator is expressed as:

$$H(z) = \sum_{i=0}^{N-1} h[n]\,z^{-i} = \sum_{i=0}^{N-1} z^{-i} = \frac{1-z^{-N}}{1-z^{-1}} \qquad (2.49)$$

This filter exhibits sin(x)/x roll off function (sinc) in the frequency domain placing N-1 zeros at the integer multiples. The frequency operation of this filter applied to a ΣΔ signal is shown in Fig. 2.23 where $H_{\Sigma\Delta}(f)$ represents the output spectra of the ΣΔ coder, $H_F(f)$ is the transfer function of the interpolation filter and $H_{\Sigma\Delta\text{-Int}}(f)$ is the spectrum of the upsampled sigma-delta signal. The example is depicted for a 4x interpolator filter (N=4).

The filtered images and quantization noise are plotted in light colours in Fig. 2.23. Since the magnitude of the S&H interpolator is known (see Fig. 2.22), we can estimate the attenuation introduced by the filter. A study of this attenuation is done in next section. In addition of the signal, ΣΔ images lie near the nulls and are attenuated.

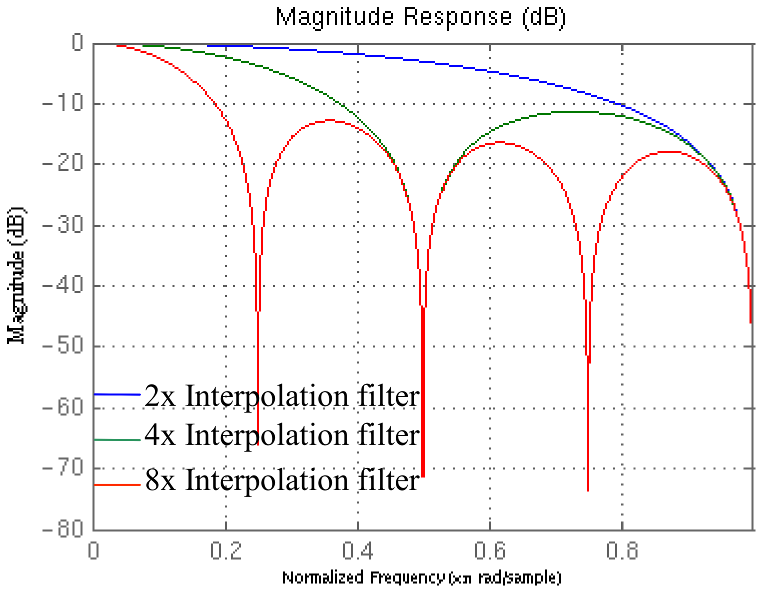

Figure 2.22: Normalized magnitude of S&H frequency response (N=2,4,8)

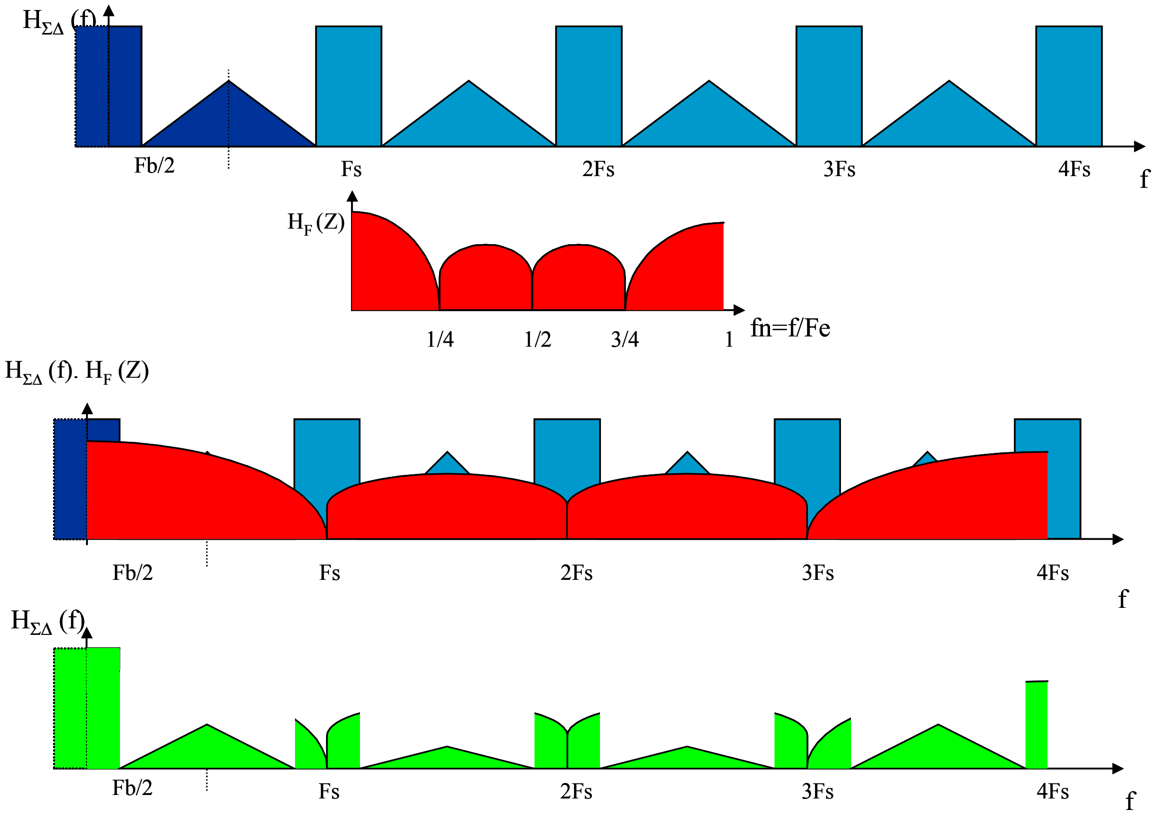
$H_{\Sigma\Delta}$ (f)
Fb/2
Fs
2Fs
3Fs
4Fs
f
H_F (Z)
1/4
1/2
3/4
1
fn=f/Fe
$H_{\Sigma\Delta}$ (f). H_F (Z)
Fb/2
Fs
2Fs
3Fs
4Fs
f
$H_{\Sigma\Delta}$ (f)
Fb/2
Fs
2Fs
3Fs
4Fs
f

Figure 2.23: S&H filtering

2.4.2.2 Simulation of the Performances of the Interpolation Filter

We can study the interpolation filter performances in the case of a WCDMA signal driving the transmitter. The diagram block schema utilized for ADS simulation is shown in Fig. 2.24. In UMTS standard is required that the power of any spurious emission shall not exceed the values shown below [UMTS].

Band	Maximum Level	Measurement Bandwidth
< 1 GHz	-36 dBm	100 kHz
> 1 GHz	-30 dBm	1 MHz

Table 2.4: Spurious emission limits in UMTS

The topology is simulated for the worst case of emission power. Simulations are obtained in the case of the 24 dBm maximum output power defined by the UMTS standard. To determine the noise for spurious emissions at the output of the IQ mixer, the output spectrum is integrated over the measurement bandwidth required in the standard (see Tab. 2.4) at different frequency offsets from the 1.92 GHz carrier. The output bandpass filter performs the additional filtering in the transmitter after the power amplifier (see Fig. 2.5). The interpolation filter is implemented to relax the constraints of the BPF. We want to determine the required attenuation of this filter as a function of the interpolation factor to fit the mandatory emission levels of the standard.

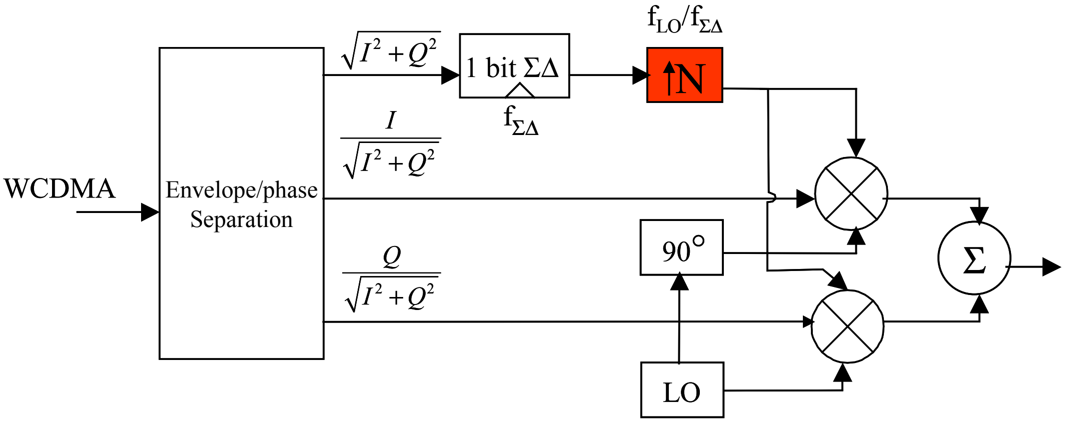
$f_{LO}/f_{\Sigma\Delta}$
$\sqrt{I^2+Q^2}$
1 bit ΣΔ
$f_{\Sigma\Delta}$
↑N
$\frac{I}{\sqrt{I^2+Q^2}}$
WCDMA
Envelope/phase Separation
$\frac{Q}{\sqrt{I^2+Q^2}}$
90°
Σ
LO

Figure 2.24: Simplified schema for architecture simulations with interpolation filtering

Three different cases are considered in the simulations. Firstly, no interpolation filtering is performed at the output of the ΣΔ coder which operates at the RF frequency of 1.92 GHz. Secondly a 2x interpolation is performed and the coder operates at 960 MHz. Finally, a 4x interpolation filter is placed at the output of the coder and its frequency is 480 MHz. The simulation results are depicted in Fig. 2.25.

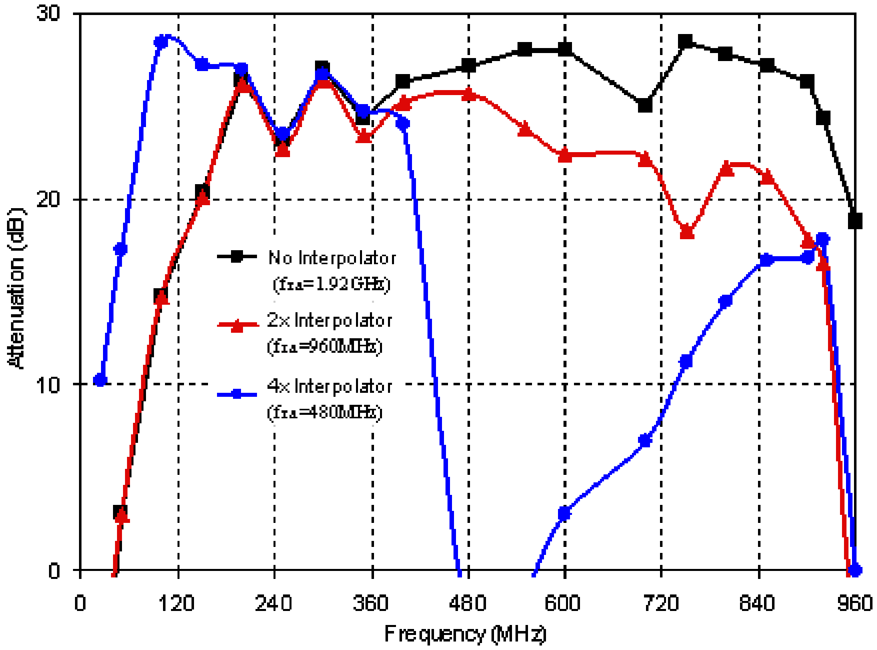

Figure 2.25: Required attenuation of the output BPF

At low frequencies offset the quantization noise is only function of the 1-bit coder frequency and the interpolation filter does not remove any noise and its maximum level is located at about $f_{\Sigma\Delta}/3$. The BPF must attenuate about 28 dB for a 4x interpolation and 26 dB for the 1x and 2x interpolations.

At higher frequencies the noise starts to be filtered and the interpolation effect is clearly shown Fig. 2.25. As the interpolation filter attenuates the images of the repeated spectrum at the output of the ΣΔ coder with a sinc roll-off, the high frequencies are attenuated and the minimum attenuation of the PBF remains lower than 20 dB for frequencies higher than 480 MHz for the 4x interpolator. However, the required attenuation is higher in the case of lower order interpolators (25 dB for 2x filter). When no interpolation is performed, the BPF needs an attenuation of about 28 dB over the frequency range. The in-band noise level depends on the number of bits in the coder and the sampling frequency. However the use of the interpolation filter is helpful at higher frequencies than $f_{\Sigma\Delta}/3$ because of the anti-image effect. In this range of frequencies, the required attenuation of the output BPF is reduced of about 8 dB if a 4x interpolation filter is employed.

2.5 Frequency Plan

In the transmitter, four clock signals can be considered. Master frequency (CLK_{MASTER}) Sigma-delta frequency ($CLK_{\Sigma\Delta}$), in-phase local oscillator clock (CLK_{LOI}) and quadrature local oscillator clock (CLK_{LOQ}). As it is shown in Fig. 2.5, the initial idea was to operate the ΣΔ coder at the same rate of the local oscillator due to its simplicity in implementation, however, the frequencies in the system must be carefully chosen to minimize out-of-band spurious signals and prevent images and quantization noise aliasing. The 1-bit ΣΔ frequency spectrum repeats itself at multiples of $f_{\Sigma\Delta}$ .To solve the problem associated to the upconversion of this digital signal, LOs frequencies of the coder must be an integer of the ΣΔ frequency. LOs clock signals are derived from a master frequency by a divide-by-two circuit.

As a consequence, next relations between these frequencies can be written:

$$f_{master} = 2 f_{LO} \tag{2.50}$$

$$f_{LO} = N f_{\Sigma\Delta} \ , \ N = 1, 2, 3... \tag{2.51}$$

$$f_{\Sigma\Delta} = \frac{f_{master}}{2N}, \ N = 1,2,3... \tag{2.52}$$

If the relation in eqn. 2.48 is respected, the quantized noise does not degrade the in-band SNR because no aliasing is produced as plotted in Fig. 2.26. For simplicity, N in eqn.2.38 is considered to be an even integer. In the implementation, sigma-delta sampling frequency $f_{\Sigma\Delta}$ is generated by a 2N frequency divider. It is preferable to operate the 1-bit modulator at a lower frequency and place an interpolator at the output to upsample the coded envelope.

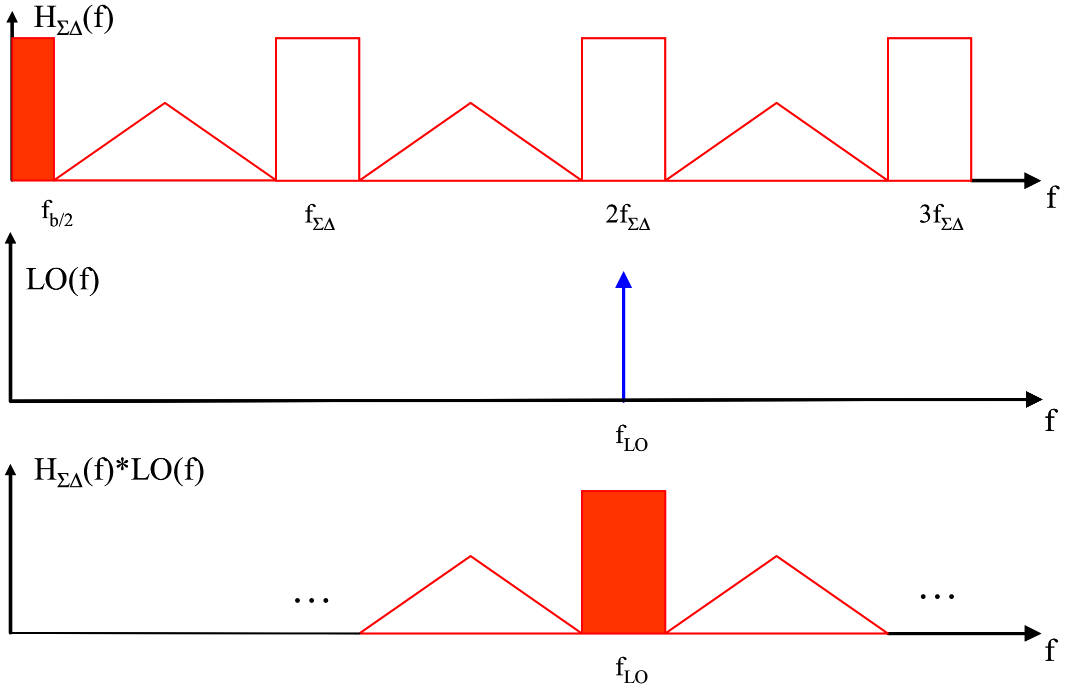

Figure 2.26: Non aliasing in ΣΔ conversion with $f_{LO}=2f_{\Sigma\Delta}$

2.6 Quadrature Modulator

As it is shown in Fig. 2.5, the quadrature modulator mixes the interpolated 1-bit ΣΔ envelope signal with the normalized I_n/Q_n phase signals and the local oscillators CLK_{LOI} and CLK_{LOQ}.

A classical quadrature modulator is described in 2.1.1. The immediate solution would be to implementate a classical analog modulator with two three-input mixers [Baut00] as depicted in Fig. 2.27. This quite simple solution is limited by the use of two B-bit DACs which have to work at a relatively high frequency in order to avoid the alias of the phase signals with the ΣΔ envelope path. Moreover, this analog topology is band-limited so an alternative transmitter design must be explored.

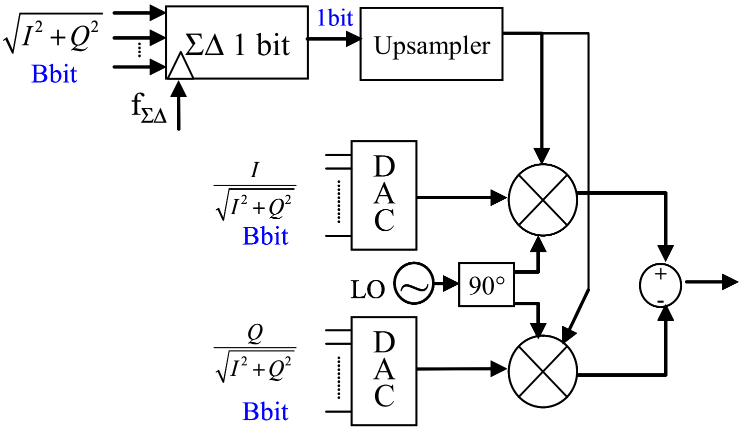

Figure 2.27: Simplified Quadrature Modulator with 3-input mixers

2.6.1 Digital Quadrature Modulator

One of the main goals in this work is to design a digital architecture as far as possible in the transmitter chain. We present here a new idea enabling to perform an IQ transmitter in the digital domain.

A digital multiplication of the phase signals (I and Q) with the two-level ΣΔ (coded 0/1) would result in a loss of half of the information. It is necessary to operate a +/- 1 multiplication. Delay in digital multiplication is long. The quadrature up-converter is supposed to work at high frequencies (LO frequencies up to 2 GHz), digital multipliers operating at GS/s clock frequencies result in high power consumption because they are implemented as a cascade of add and shifts. It is important to avoid the use of digital multipliers in the final architecture.

Since the output of the ΣΔ is a 1-bit signal having only values of 1, -1 and the LOs signals are either 1 or -1, the multiplication of these three signals depends on the product of the envelope and LOs. If both signals have the same value (either 1 or -1) then the output equals I_n (or Q_n). If both signals are complementary values, the output is $-I_n$ (or $-Q_n$) so a circuit performing the phase inversion is needed (see Tab. 2.5).

Signals in the transmitter are represented in two's-complement arithmetic. To negate a two's complement number, all the bits (9 in our study) must be inverted (one's complement), then '1' is added to the result and overflow is ignored. On possible solution of implementation is to use a 9-bit adder. One simpler conversion of a binary number into its two's-complement is to start at the least significant bit and copy all the '0s' until the first '1' is reached and copied. Then, the remaining bits are flipped.

The proposed topology (§ 4.4) provides a converter with simplified structure than the 9-bit adder, requiring fewer elements (five 2-input NOR gates, two 3-input NORs, four 2-input NANDs and nine XORs) than a 9-bit adder and the maximum propagation delay is limited to the passage of one NOR and one NAND gates.

ΣΔ	**LO**	**Command**
-1	-1	Not Invert
-1	1	Invert
1	-1	Invert
1	1	Not Invert

Table 2.5: Command Signal

Tab. 2.5 corresponds to the truth table of a logic exclusive OR function. So, the command signal (CMD), which determines wether the phase signals are inverted or not at the output is calculated like the XOR of the envelope and LO signals.

$$CMD_I = E_{\Sigma\Delta} \oplus LO \tag{2.53}$$

$$CMD_Q = E_{\Sigma\Delta} \oplus LO_{90} \tag{2.54}$$

Therefore the result of the multiplication of the three signals can be written as:

$$I_{LO} = (I_n.\overline{CMD_I}) + (-I_n.CMD_I) \tag{2.55}$$

$$Q_{LO} = (Q_n.\overline{CMD_Q}) + (-Q_n.CMD_Q) \tag{2.56}$$

The implemented IQ modulator using only multiplexors, XOR and NOR gates (as it will be presented in chapter 4) is plotted in Fig. 2.28.

By choosing a simple selection of +/- I_n and +/- Q_n, one can implement a very simple full-digital, wideband quadrature modulator and eliminate the power consumption of the high-speed digital mixer leading to a low-power system. The quadrature LOs are digitally generated with a phase-error less than 1° to minimize the imperfectly rejected image effect as it will be described in chapter 4.

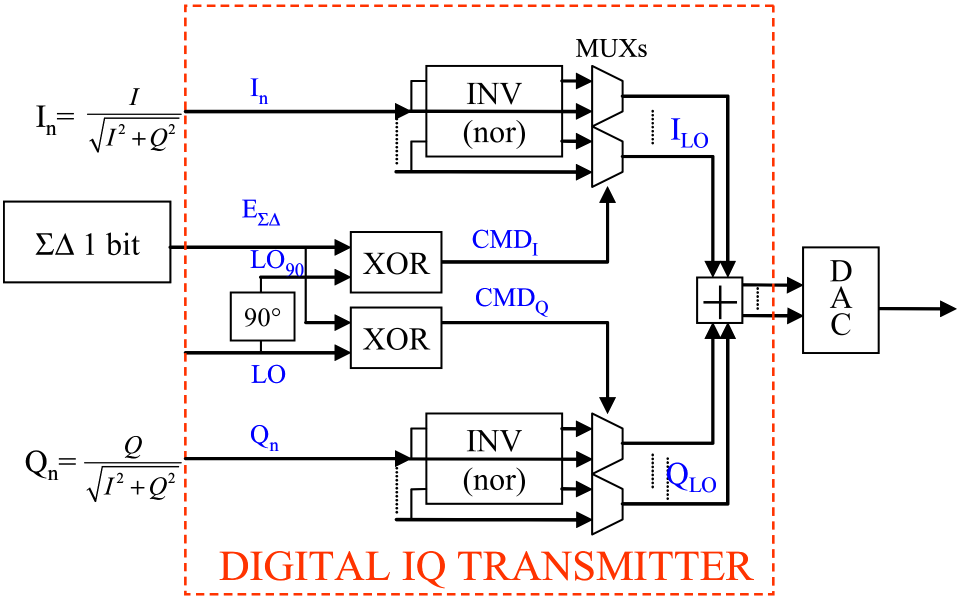

Figure 2.28: Simplified Quadrature Modulator with two-input mixers

2.6.2 Output Combiner

The output combiner is one of the most critical blocks in the quadrature converter. Output of the IQ transmitter is the sum of both 9-bit high frequency RF signals I_{LO} and Q_{LO}. This digital adder must be designed to operate at twice the frequency of the upconverted signal; it means that the digital combiner has to operate at GS/s. To take into account the overflow when adding the two digital signals, a 10-bit adder must be considered.

2.6.2.1 10-bit Digital Adder

Designing a 10-bit adder operating at GS/s is not a simple task. There are two main parameters to be studied in the design of this adder: speed and power consumption. Speed is determined mainly by the propagation delay, which is defined by the critical path in a full-adder chain. This time depends on the supply voltage, the number of bit in the adder and the topology chosen, being the structure based on the Transmission Gate (TG) the fastest (for V_{DD}=1.2 V). We can estimate the delay of a 10-bit adder lower than 0.5 ns in actual technologies. If the operating frequency is targeted to 4 GS/s, it involves a maximum latency time of about 0.25 ns, which implies carefully design. Power consumption depends linearly on the operating frequency. Even if the power dissipation of a 10-bit adder is relatively not very important even at GS/s (about 3 mW for power supply of 1.2 V in a TG implementation [Hibo06PhD]), for low-power applications, the overall power has to be minimized as much as possible. In order to study how to implement such an adder, we take into account the DAC placed at its output. This circuit converts the 10-bit digital signal into an analog signal to drive the PA with a gain control depending on the transmitted power. It would be easier to integrate both functions in the DAC avoiding the use of a difficult to design and power consuming adder.

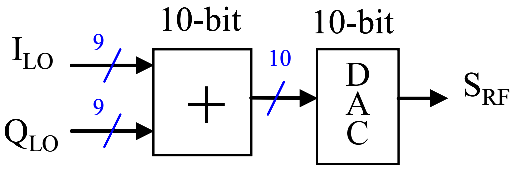

Figure 2.29: 10-bit Digital Adder with DAC

2.6.2.2 Analog Combiner

The idea proposed in this work is to replace both the 10-bit digital adder and the 10-bit DAC by two 9-bit DACs. Fig. 2.30 shows our proposed solution; the signals are combined in current mode in the analog domain (outputs of two 9-bit asynchronous DACs) at the load by simply shorting one output to another at the same rate of the analog signals in an asynchronous way.

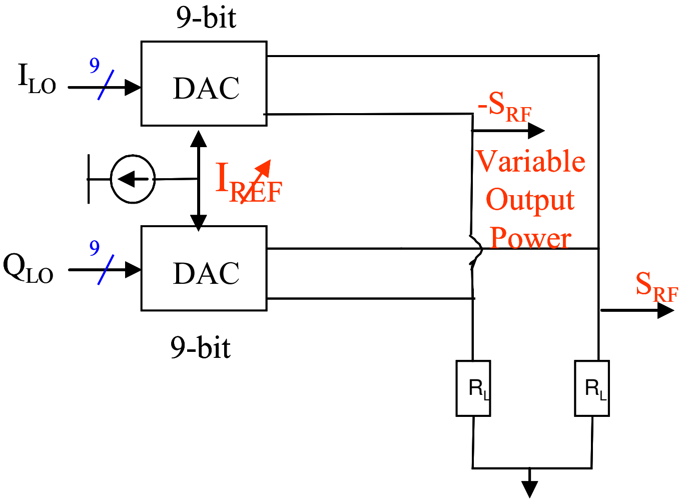

Figure 2.30: Proposed Analog Combiner

One of the principal challenges in the design of this analog combiner is the dynamic power range needed at the output. The output power has to be varied about 45 dB to meet the power control requirements of CDMA systems. To implement such a gain control system, a variable reference current is used in each DAC as it will be explained in chapter 3. As one of the main goals of the transmitter is to assembly this circuit with a RF power amplifier, the chosen DAC architecture is based upon a differential topology as shown in Fig. 2.30 and no single-to-differential circuit is needed to drive the differential power amplifier. This topology takes advantage of the architecture in Fig. 2.29 because of the power and design savings of the high-speed adder and the reduction in the complexity of the design of the DAC (which is 9-bit instead of 10-bit).

The structure in Fig. 2.30 is inherently differential and wideband, which avoids the use of a bandlimited single-to-differential circuit at the input of the power amplifier. Moreover the power dissipation of the two DACs is the same as in the case of a single DAC (Fig. 2.30) since for a given output power, each DAC delivers half of the output power and 9-bit are needed instead of 10-bit.

2.7 Conclusion

A novel transmitter architecture is presented in this chapter. This technique employs phase and envelope separation (EER-type system) and direct RF conversion architecture. Envelope is coded by a noise shaping 1-bit coder and the phase signals are normalized by the envelope signal. This topology employs differential architecture and avoids the single-to-differential circuit at the input of the power amplifier. The recombination before the power amplifier leads to an envelope-constant signal. This signal can be amplified by no matter what power amplifier in an efficient way.

Quantization noise of the signal generated by the ΣΔ modulator is attenuated by a Sample-and-Hold interpolator placed at the output of this coder to introduce notch at multiples of the sampling frequency.

The proposed transmitter architecture is depicted in Fig. 2.31. This topology uses a full-digital differential wideband quadrature modulator, which enables to perform the up-conversion of the three paths in a simple way. This IQ transmitter is simplified replacing the high consuming digital multipliers by logic gates and a set of multiplexors. The combination at the output of this modulator is performed by two asynchronous 9-bit Digital-to-Analog Converters instead of extremely difficult to design high-speed 10-bit adder. This modification enables to perform the dynamic control required for CDMA standards. This transmitter is wideband because no bandlimited circuits are employed in the implementation. In the perspective of a universal transmitter and to meet requirements of modern communication systems, a gain control is set-up in the output combiner.

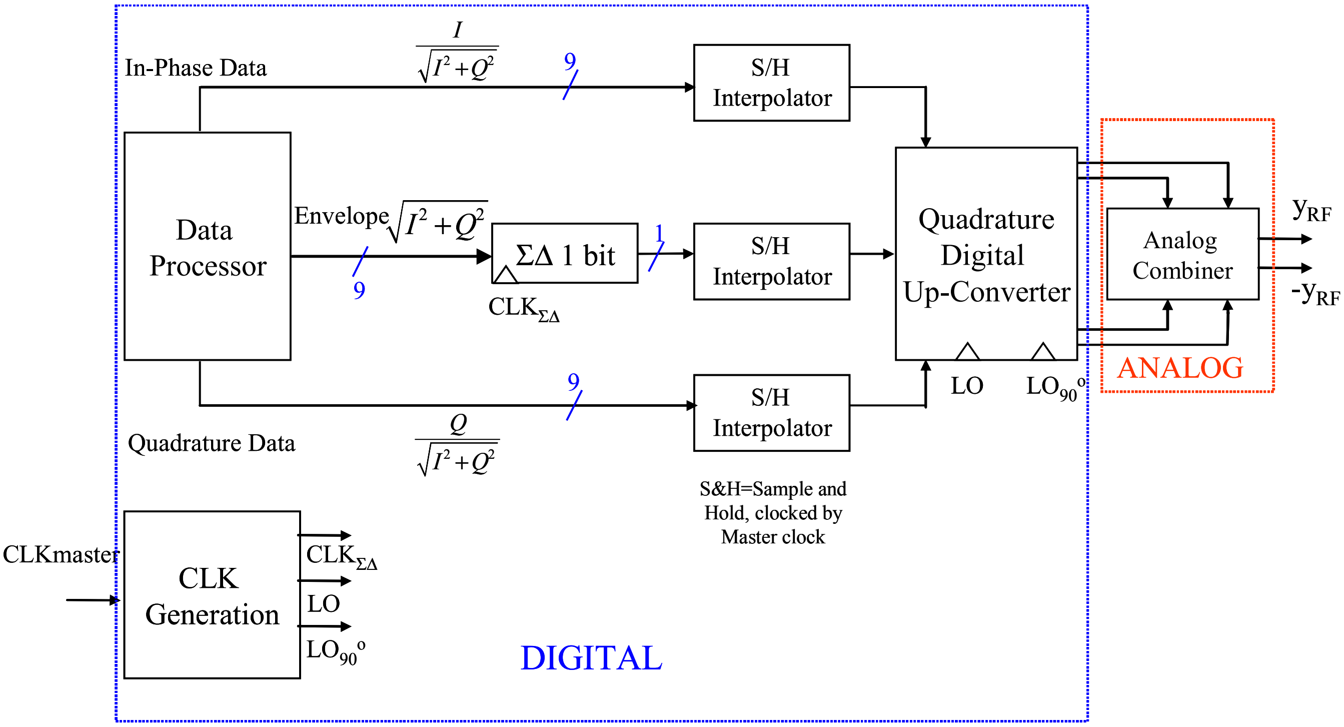
In-Phase Data
$\frac{I}{\sqrt{I^2+Q^2}}$
9
S/H Interpolator
Data Processor
Envelope $\sqrt{I^2+Q^2}$
9
ΣΔ 1 bit
1
CLK$_{\Sigma\Delta}$
S/H Interpolator
Quadrature Digital Up-Converter
Analog Combiner
y_{RF}
$-y_{RF}$
ANALOG
LO
LO$_{90°}$
9
S/H Interpolator
Quadrature Data
$\frac{Q}{\sqrt{I^2+Q^2}}$
S&H=Sample and Hold, clocked by Master clock
CLKmaster
CLK Generation
CLK$_{\Sigma\Delta}$
LO
LO$_{90°}$
DIGITAL

Figure 2.31: Proposed transmitter architecture

Chapter 3 will focus on the study and design of the 9-bit Digital-to-Analog-Converter performing the high-speed addition of the two upconverted RF signals and the 45 dB control gain of the transmitter.

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Chapter 3 Design and Test of the Digital-to-Analog Converter

3.1 Introduction

The purpose of this chapter is the study, design and test of a 9-bit high-speed Digital-to-Analog Converter (DAC). Two DACs are placed at the output of the IQ modulator to add in current and convert two orthogonal 9-bit digital RF-upconverted signals into a differential analog output signal with 45 dB gain control to drive the power amplifier in the transmitter.

This chapter is organized as follows. Next section reviews the basic operation and parameters of a DAC. Secondly, a brief overview of different approaches of digital-to-analog converters is presented. The chosen structure together with the main advantages with regards to a classical binary conversion and the description of the design methodology of the building blocks will be explained in § 3.3. The problem of the high-speed test of the converter at high frequencies will be considered in § 3.4. The fabricated chip is shown in § 3.5. Simulation and results from the prototype built in 0.13 µm BiCMOS are discussed in § 3.6. Finally, in § 3.7 the conclusion will be drawn.

3.2 Digital-to-Analog Conversion

3.2.1 Basic Operation

Digital-to-analog converters fundamentally convert digital data into analog voltage or current. The discrete analog output signal is a representation of a limited number of discrete digital input codes. The ideal transfer function is plotted in Fig. 3.1. These output values V_{out} represent a fraction of the full-scale analog voltage V_{FS} determined by the digital input code b_i where $i = 0 : N-1$. Most Significant Bit is called MSB (b_{N-1} in Fig. 3.1) and Least Significant Bit is called LSB (b_0 in Fig. 3.1). For a DAC, 1 LSB corresponds to the step between successive analog outputs.

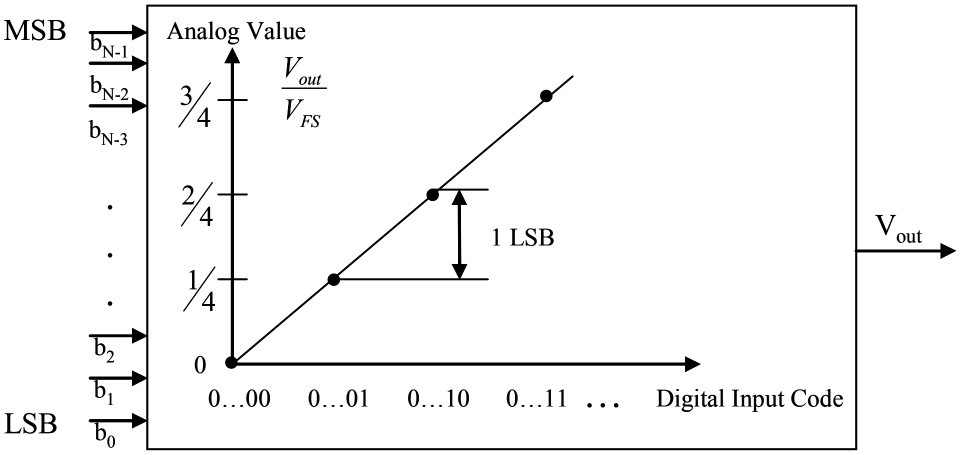


Figure 3.1: Ideal Transfer Function (DAC)

Traditional DACs produce sample-and-hold (S&H) waveforms. The output signal is held in time at the current value until the next input value is latched, resulting in a piecewise constant output as depicted in Fig. 3.2.

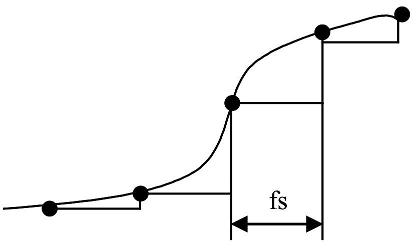


Figure 3.2: Zero-order-hold DAC

This is a Zero-Order-Hold operation and has an effect on the frequency response of the reconstructed signal. Frequency response of such zero-order-hold was presented and studied in § 2.6.1.2.

3.2.2 Figures of Merit

Several parameters are used to characterize the DACs performances. These figures of merit are used to evaluate the quality of the DACs. They can be divided into two types: static performances, and frequency performances.

3.2.2.1 Static Performances

Some performance metrics are used to characterize the DAC static behavior limiting the DAC performances at low frequencies. The main static performances are the Integral NonLinearity

(INL) and the Differential NonLinearity (DNL). INL error is defined to be the deviation of the output characteristic of a DAC from the ideal transfer function (see Fig. 3.3). INL values are defined for each digital input code and thus the INL can be plotted as a function of the input code. DNL error is defined as the difference between the actual step width and the ideal value of 1 LSB (Fig. 3.4). Thus, an ideal converter has a differential nonlinearity of 0 for all digital input codes, whereas a converter with maximum DNL of 0.5 LSB has step sizes varying from 0.5 LSB to 1.5 LSB. If $|DNL(x_i)|<1$ LSB for all input codes, the DAC is guaranteed to be monotone with no missing codes. A DAC's monotonicity is guaranteed when its analog output increases or remains constant with an increasing input signal.

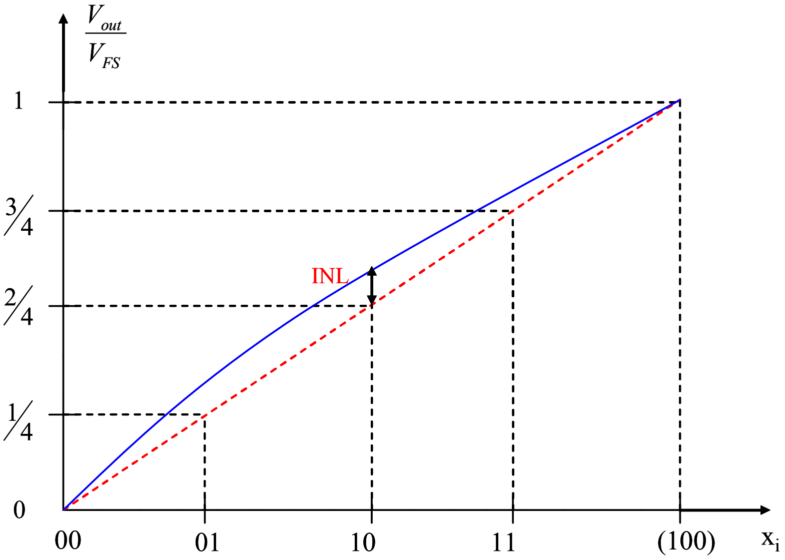


Figure 3.3: The INL error

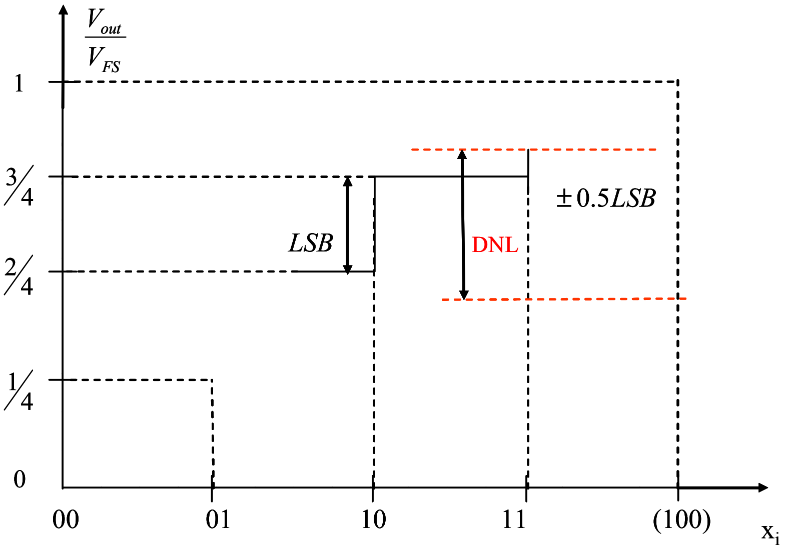


Figure 3.4: The DNL error

3.2.2.2 Frequency-domain Performances

In high-speed applications, the DAC performance is basically limited by the dynamic behaviour. In that case, the DAC is better characterized by frequency-domain performances. Sinusoidal test signals are often used to characterize the DAC performances. The most common specification is SFDR (Spurious Free Dynamic Range), which measures, usually in dB, the non-linearity of the DAC. It is defined as the ratio of the signal power (P_{Signal}) to the maximum of the spurious (P_{Spur_max}) generated by harmonic distortion (eqn. 3.1). Only spurious within the Nyquist band ($f_s/2$) are considered (Fig. 3.5).

$$SFDR = \frac{P_{Signal}}{P_{Spur\_max}} \tag{3.1}$$

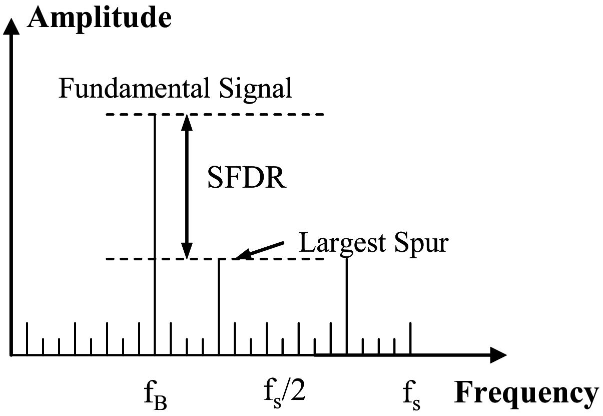


Figure 3.5: The DNL error

3.2.3 DAC Architectures

This section discusses briefly the most common DAC architectures. Several topologies can be used to build a DAC: architectures in voltage mode, current mode and charge-redistribution mode. In voltage mode, a reference voltage is divided into different voltage levels by using resistors. In current mode, output current varies with the input bits. In charge-distribution mode, capacitors are used in charge distribution to control the output levels. The advantages and drawbacks of each of them are examined in next sections.

3.2.3.1 Resistor-String DAC Architecture

This architecture is simple. The DAC is implemented as a voltage divider. 2^N resistors of equal sizes are needed in a resistor string to generate 2^N voltage levels (N-bit DAC) together with 2^{N+1}

switches (Fig. 3.6). The encoder maps an N-bit input signal onto a word with a single active bit. The operational amplifier sum all these current and convert them into an output voltage. This topology is inherently fast and monotonic and uses switches easy to implement in MOS technologies.

However, this architecture is not adapted to DACs with high resolution because of the exponentially growth of resistors and switches in the implementation. It results in a slow topology because of the bandlimited encoder.

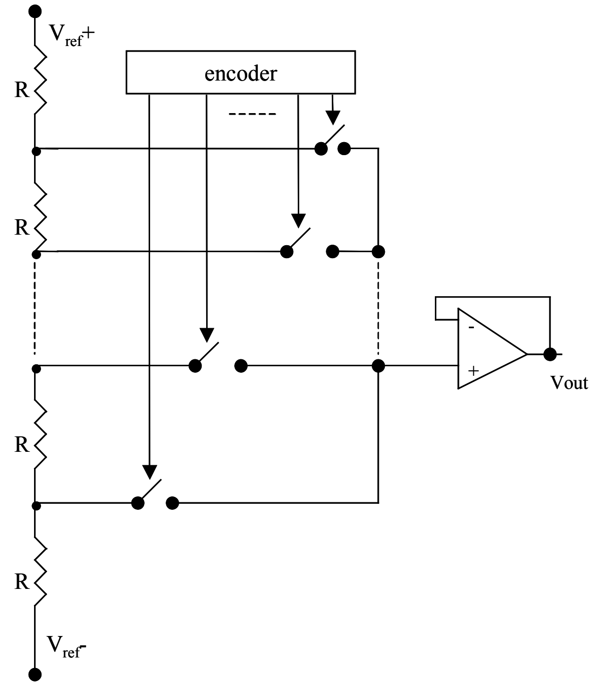


Figure 3.6: Resistor-string DAC architecture

3.2.3.2 R-2R Ladder DAC

The R-2R ladder is a binary-weighted (the weight of a bit is a power of two) DAC that uses a cascaded structure of resistors of values R and 2R. A R-2R ladder DAC is depicted in Fig. 3.7, where the output signal can be expressed as follows: (a mode of operation in voltage is considered and equal currents flow through all switches).

$$V_{out} = \frac{R_f}{R} . V_{ref} . \left[\frac{\sum_{k=0}^{N-1} b_k . 2^k}{2^N} \right] \tag{3.2}$$

The bits are switched between 0 and V_{ref} and depending on the input word, V_{out} varies between these two values. Indeed, contribution of each bit to the analog output is proportional to its binary weight. This architecture is simple due to only two possible resistor values. However this technique is limited by the resistors tolerance that produces output errors. The output depends on how accurately is matched one resistor to others. As in the precedent example, output operational amplifier bandwidth limits the speed of this kind of architectures.

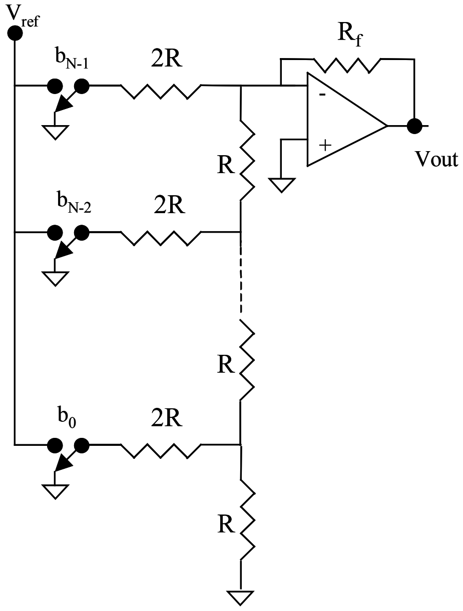


Figure 3.7: R-2R ladder DAC

3.2.3.3 Charge Redistribution Architecture

This architecture is based on the switched-capacitor technique [Host77] and is shown in Fig. 3.8.

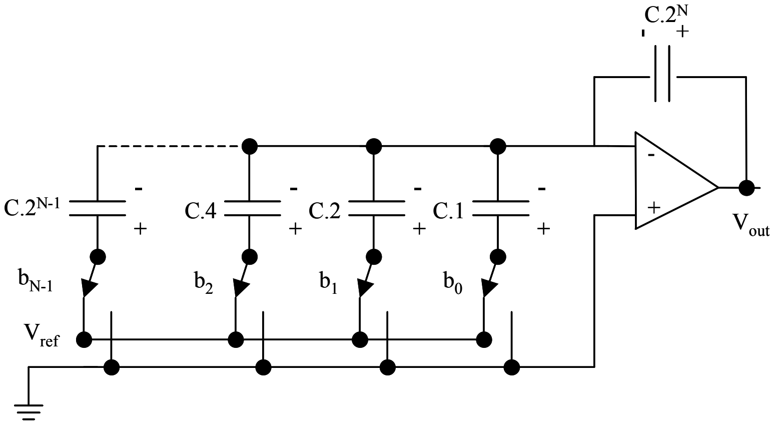


Figure 3.8: Charge redistribution DAC

Samples of charge proportional (binary weighted in Fig. 3.8) to the unit capacitor value C, the reference voltage V_{ref} and the digital input word, are sampled into an array of input capacitors during one phase. During the other clock phase, the charge stored in the capacitor array is integrated onto the integrating capacitor to generate an output proportional to the input code.

Limitations are the difficult matching of capacitors (mismatch in practical implementation), the switching-on resistance, complexity of the control logic and timing. Furthermore, this topology occupies most area than other implementations.

3.2.3.4 Current-Steering DAC

The current-steering DAC is based on the switched-current technique [Toma93] and is illustrated in Fig. 3.9. The reference source is replicated by each weighted current source. Input bits (b_k) control the switches that steer the current of the current source to the differential output where two load resistances convert it to a voltage signal. The same mismatch problem in passive components (resistors and capacitors) explained in the previous section is now replaced by a mismatch problem concerning only active components. For an ideal current-steering DAC the k_{th} current source are related to the reference source (I_{LSB}) as follows

$$I_k = w_k . I_{LSB} \tag{3.3}$$

where w_k is the integer weight of the current source.

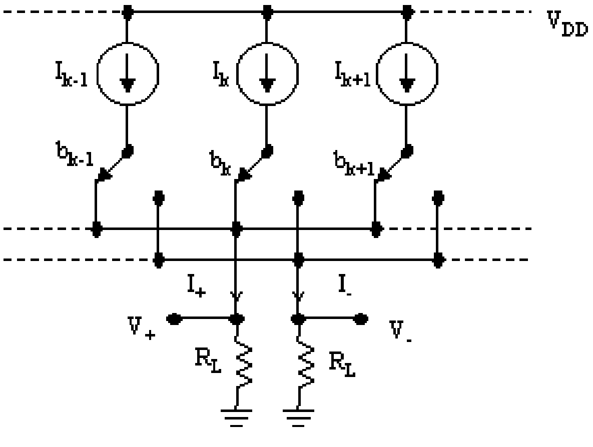


Figure 3.9: Current-steering DAC

The positive, negative and differential current at the output can be expressed as:

$$I_+ = \sum_{k=0}^{N-1} b_k . I_k = \sum_{k=0}^{N-1} b_k . w_k . I_{LSB} \tag{3.4}$$

$$I_- = \sum_{k=0}^{N-1} \overline{b_k} I_k = \sum_{k=0}^{N-1} I_k - I_+ = \sum_{k=0}^{N-1} w_k I_{LSB} - \sum_{k-0}^{N-1} b_k w_k I_{LSB} \tag{3.5}$$

$$I_{diff} = I_+ - I_- = 2.\sum_{k=0}^{N-1} b_k . w_k . I_{ref} - \sum_{k=0}^{N-1} w_k . I_{LSB} \tag{3.6}$$

The performance of the current-steering DAC depends on how the integer weight w_k in eqn. 3.3 is implemented. The possible architectures for the implementation are:

- The binary weighted architecture where

$$w_k = 2^k \text{ for k = 0...N - 1} \tag{3.7}$$

- The thermometer coded architecture where

$$w_k = 1 \text{ for k = 0...N - 1} \tag{3.8}$$

- The segmented architecture is a hybrid architecture composed of precedent implementations.

3.2.3.4.1 Binary-Weighted Architecture

In the binary-weighted architecture, every switch steers a current which value is twice the value of the previous bit (see eqn. 3.7) and are often the repetition in parallel of a unit reference cellule. The input bits control directly the switches and no decoding is necessary. It leads to a small-required area and very simple architecture. This technique uses N current sources delivering binary-weighted so large currents flow into the MSB bits when coding high values. In addition, a large DNL error is presented in this architecture at half-scale transition since a single source switches off/on while the N-1 other switches on/off. This is the case at the MSB transition 011…111 to 100…000 causing an important glitch [Hung98].

3.2.3.4.2 Thermometer-Coded Architecture

In this architecture, unary current sources (see eqn. 3.8) are used. Every current source has a weight of 1LSB so 2^{N-1} sources are needed to implement a N-bit converter. The switches are not commanded directly by the N-bit input word but by a thermometer conversion of the input digital codes (2^{N-1}-bit word) (see Tab. 3.1).

Binary			**Thermometer Code**						
B_2	B_1	B_0	T_6	T_5	T_4	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	0	1
0	1	0	0	0	0	0	0	1	1
0	1	1	0	0	0	0	1	1	1
1	0	0	0	0	0	1	1	1	1
1	0	1	0	0	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1

Table 3.1: Thermometer Code (3bits)

The advantages of this topology are a good DNL error and small dynamic switching errors since for a LSB change at the input, only a single current source must be switched. The presence of a thermometer coder limits this architecture in terms of complexity and consumption. This coder together with the 2^N current source elements lead to a converter large in silicon area.

3.2.3.4.3 Segmented Architecture

This architecture represents a hybrid of the before mentioned topologies combining the best of both architectures. For a N-bit converter, the DAC is divided in two sub-DACs. One M-bit DAC with M LSBs bits controlling directly the switches using M binary-weighted source currents and the second DAC with N-M MSBs bits input a thermometer coder leading to the use of 2^{N-M} unitary sources. This topology combines good linearity relative to the thermometer code part and simplicity and minimization of chip area as in binary architectures. Increased area of this topology over a simple current architecture is one of the main disadvantages of this architecture if small size consideration is taken into account. Moreover, the thermometer coder employed in the implementation limits in practice the high-speed performances of the DAC.

3.2.3.5 Trade-off between Linearity-Complexity and Silicon Area

As it has been shown, a large amount of different implementations of a DAC are possible. Due to process tolerances and area considerations, techniques using resistor-string or charge redistribution are discarded to implement the 9-bit high-speed DAC. A solution based on current sources seems to be the most appropriated to our purposes. In the perspective of a simple and high-speed DAC, a solution employing some degree of binary weighting in the current sources is considered. A full binary-weighted DAC would be the best implementation in terms of area occupation and small complexity; however this topology is limited by the large DNL error. A segmented architecture represents the trade-off between linearity and area. However, the realization of the high-resolution thermometer coder is not easy at GS/s. As the main constraint of our system is to achieve high-speed to convert the RF IQ signals a structure based on binary-weighted current sources is chosen [Deve06]. The matching of the MSB current source transistor must be extremely accurate in this kind of topologies, and is the DNL limiter for the entire digital-to-analog converter. Such error would be unacceptable for linear applications. To reduce this linearity issue and the large ratios in size of the transistors from the MSBs current sources to the LSBs ones, a new structure is proposed in next section consisting in dividing the whole DAC in two binary-weighted sub-DACS. This improved binary weighted current source solution represents the best trade-off between speed, linearity and consumption.

3.2.3.6 Proposed DAC

One important aspect to be taken into count in the choice of the DAC architecture is that the converter must be able to convert high-speed signals with a power variation of about 45 dB to meet CDMA output power requirements. It seems evident that the use of topologies based on passive components would involve the switching of resistors or capacitors of different values to perform this gain control. Thus, a solution employing current sources is preferred instead. The main drawback of a classical binary structure is the high factor between the most significant bit current and the least-significant bit (256 in a 9-bit DAC application). As a consequence the non-linearities grow, and the frequency is limited because of the use of big size transistors for design.

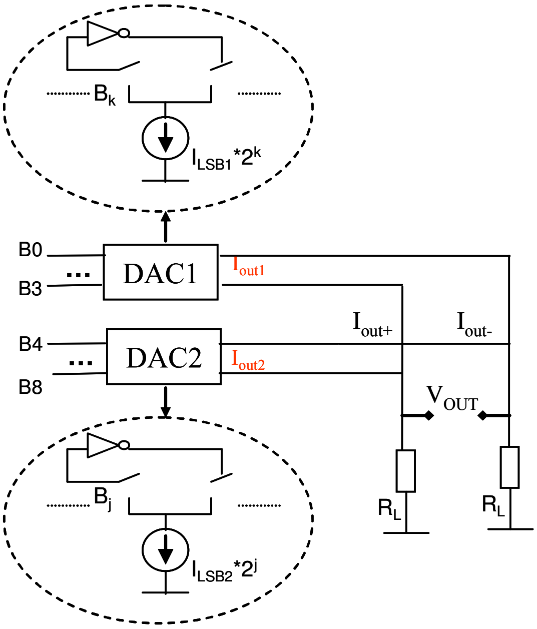


Figure 3.10: Division of the whole DAC into 2 sub-DACs

To overcome this, we propose to reduce the size ratios of the transistors by splitting the basic structure in two identical DACs with smaller sizes than the whole DAC (Fig. 3.10). As it is shown, a differential architecture is preferred to cancel the important glitches associated to a binary-architecture. Since the glitches constitute a common-mode error, they would be entirely removed in the differential output if the two outputs were perfectly matched (Fig. 3.10).

The first DAC (4-bit) is driven by the four least significant bits:

$$I_{OUT1} = \sum_{n=0}^{n=3} 2^n . B_n . I_{LSB1} \tag{3.9}$$

The five most significant bits drive the 5-bit DAC and the expression of the output current can be written as:

$$I_{OUT2} = \sum_{n=0}^{n=4} 2^n . B_{n+4} . I_{LSB2} \tag{3.10}$$

If the least significant current is chosen as (eqn. 3.11):

$$I_{LSB2} = 2^4 . I_{LSB1} \tag{3.11}$$

Then, the output current of the second DAC becomes

$$I_{OUT2} = \sum_{m=0}^{m=4} 2^{m+4} . B_{m+4} . I_{LSB1} = \sum_{n=4}^{n=8} 2^n . B_n . I_{LSB1} \tag{3.12}$$

Applying the superposition principle, we get:

$$I_{OUT} = I_{OUT1} + I_{OUT2} = \sum_{n=0}^{8} 2^n . B_n . I_{LSB1} \tag{3.13}$$

which is the expression of a 9-bit full binary-weighted DAC.

Reference currents for two DACs are obtained from an external source current I_{REF}. To maximize the accuracy between the current flowing into the two conversion blocks and reduce the transistors size we choose (see Fig. 3.13):

$$I_{LSB1} = \frac{I_{REF}}{4} \tag{3.14}$$

$$I_{LSB2} = 4.I_{REF} \tag{3.15}$$

The implementation of the two sub-DACs is simple. A control gain is performed in the sub-DACS, which means that the reference current is varied of about 45 dB and this gain control is one of the most important features of the target DAC. The 5-bit converter is a replica of the 4-bit DAC with the addition of one current branch. The only difference is the value of the current flowing into each one. The maximum transistor size ratios are 16 for the case of the 4-bit DAC and 32 for the 5-bit one which are respectively 16 and 8 times less than the 256 ratio in the case of a 9-bit binary DAC, thus the mismatch between current sources is reduced.

3.3 DAC Circuit Design

In this section, the design of the 9-bit DAC is illustrated. The fundamental building blocks are described in detail. The Digital-to-Analog Converter circuit has been designed using a 0.13 µm BiCMOS process from STMicroelectronics. A brief overview of the main characteristics of this technology is given in § 3.3.1.

3.3.1 Description of the Technology

Complementary Metal-Oxide-Semiconductor (CMOS) processes are popular for implementing integrated circuits. This is mainly due to the easy and low cost implementation of digital circuits with very power efficiency and thus, low power consumption. To implement the high-speed, 9-bit, 45 dB power control DAC, it is necessary to design high-speed switches and very accurate current sources. BiCMOS technology offers extremely high-speed bipolar transistor suitable for fast current steering. In addition, current sources with bipolar transistors have high Early voltages and present higher output impedance. It enables to stabilize some critical nodes since the variation of the current with the voltage is less important than in CMOS devices (short-channel effect) leading to high precision current sources. In definitive, BiCMOS technologies afford the use of high-speed bipolar transistor with highly integrated CMOS.

SiGeC BiCMOS process is a high performance technology mainly dedicated for optical communications systems driving data rates up 40 Gbit/s and for single-chip solutions for wireless and broadband communications systems. High density CMOS is required to perform complex digital signal processing. The integration of a SiGeC bipolar transistor with f_T of 160 GHz in a 0.13 µm HCMOS process is carried out. The compatibility with basic CMOS devices is full preserved.

3.3.1.1 Back-end Main Features

- Back-end with 6 metal levels.
- Damascene Copper for metal 1 to last.
- Metal 1 to last but one metal: tight pitch levels for routing on this copper.
- Last Metal: Thick copper, preferred layer for power, clock, busses and major interconnect signal distribution.

3.3.1.2 CMOS Transistors

Three transistor families with different threshold voltages (Vt_n for NMOS transistors and Vt_p for PMOS transistors) are included with a power supply of 1.2 V with extension to 2.5 V.

- CMOS devices with 2 nm of gate oxide thickness (GO1) are designed for 1.2 V applications.
    - 1.2 V High-Speed (HS) 0.13 µm CMOS (Vt_n=380 mV and Vt_p=390 mV)
    - 1.2 V Low-Leakage (LL) 0.13 µm CMOS (Vt_n=500 mV and Vt_p=480 mV)
    - 1.2 V Ultra-Low-Leakage (ULL) 0.13 µm CMOS (Vt_n=570 mV and Vt_p=590 mV)

- CMOS devices with 5 nm of gate oxide thickness are designed for 2.5 capable I/O's.

3.3.1.3 Bipolar Transistors

Two SiGe-C NPN bipolar transistors are available in this process with different emitter base breakdown voltage (BVCEO) for RF and Optical Communications applications: a high-speed transistor with BVCEO of about 1.7 V and a high voltage transistor with BVCEO of about 3 V. In this research, high-speed type is considered.

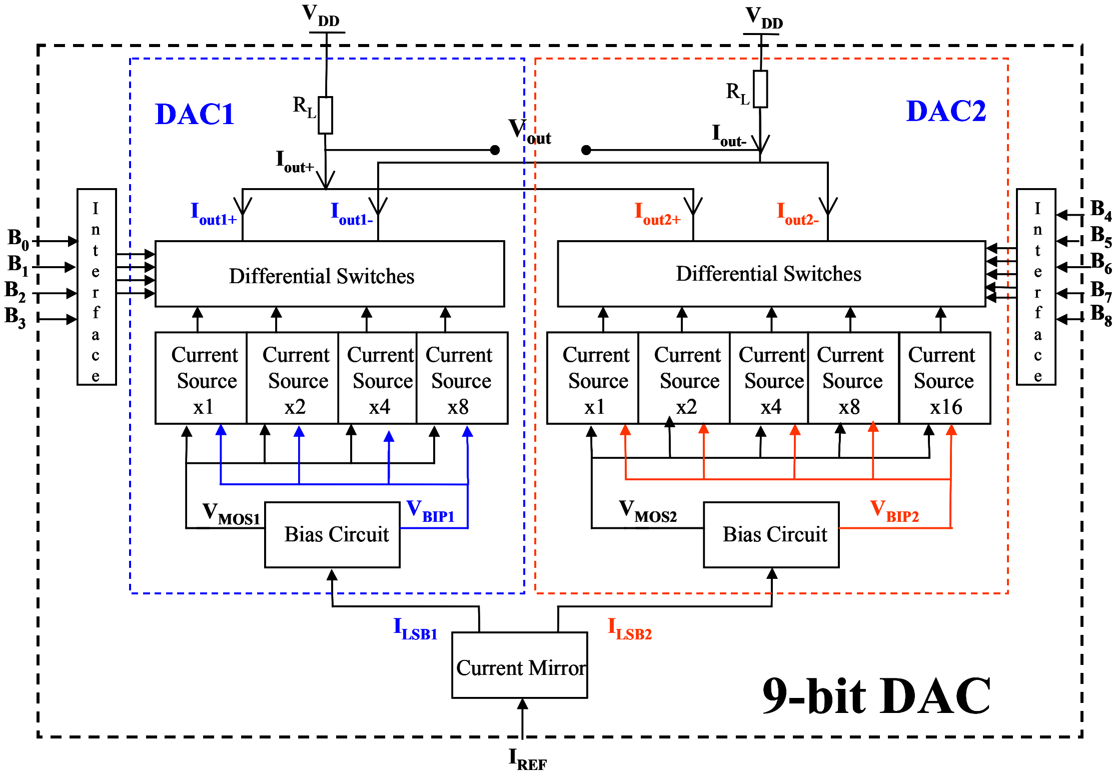
Parameters	TYP.	Units
Current gain	650	
Early voltage	>70	V
Collector emitter Breakdown voltage	1.75	V
Maximum cut-off Frequency (f_T)	160	GHz
Maximum fmax	160	GHz

Table 3.2: Electrical parameters for high-speed bipolar transistors

Main electrical parameters for high-speed NPN bipolar transistors are summarized in Tab. 3.2. For our purposes, High-Speed (HS) 1.2 V CMOS transistors and high-speed NPN bipolar transistors are used in this application since the high-DAC must replicate and steer the current at the rate of GS/s.

3.3.2 Architecture of Designed DAC

In next sections, the main building circuits of the designed DAC are presented. The converter is composed of a wide-dynamic current mirror to generate the two reference currents to vary the output currents of both sub-DACs (4-bit DAC1 and 5-bit DAC2 in Fig. 3.11).



V_DD
V_DD
DAC1
R_L
V_out
R_L
I_out-
DAC2
I_out+
I_out1+
I_out1-
I_out2+
I_out2-
B_0
B_1
B_2
B_3
Interface
Differential Switches
Differential Switches
Interface
B_4
B_5
B_6
B_7
B_8
Current Source x1
Current Source x2
Current Source x4
Current Source x8
Current Source x1
Current Source x2
Current Source x4
Current Source x8
Current Source x16
V_MOS1
Bias Circuit
V_BIP1
V_MOS2
Bias Circuit
V_BIP2
I_LSB1
I_LSB2
Current Mirror
9-bit DAC
I_REF

Figure 3.11: Architecture of the designed DAC

The bias circuit generates the required bias voltage for the gate of the MOS and the base of the bipolar transistors of the cascode current sources, as it will be detailed in § 3.3.3 and 3.3.4. The current sources replicate the least-significant currents I_{LSB1} and I_{LSB2} by a factor of 1, 2, 4, 8 for DAC1 and 1, 2, 4, 8, 16 for DAC2. The differential switches steer the current from one output to another depending of the input word B. The output currents are added in the resistors and converted to the output voltage V_{out}. Additional circuitry is necessary to adapt the 1.2 V CMOS digital part (binary signals $B_{1...8}$) and the BiCMOS part operating at a supply V_{DD}=2.5 V. For NMOS and PMOS transistors, sizes will be given as Width/Length (W/L) and for the bipolar transistors as the length of the emitter (L_E), all of them expressed in µm. For simplicity, when length parameter of a MOS transistor is not expressed, we consider that it is sized with the minimum length (L_{min}) of the chosen technology (0.13 µm).

3.3.3 Wide-Dynamic Range Current Mirror

Since the targeted DAC has a dynamic variation of 45 dB, the bias circuit that generates the reference current for the two DACs must be capable of such variation. According to eqns. 3.14-3.15, the current mirror performs a divide-by-4 operation to bias the DAC1 and multiply-by-4 to bias the DAC2. These ratios represent the best trade-off for a correct precision in both currents. This circuit is the well-known architecture called cascode current mirror [Gray93] as illustrated in Fig. 3.12.

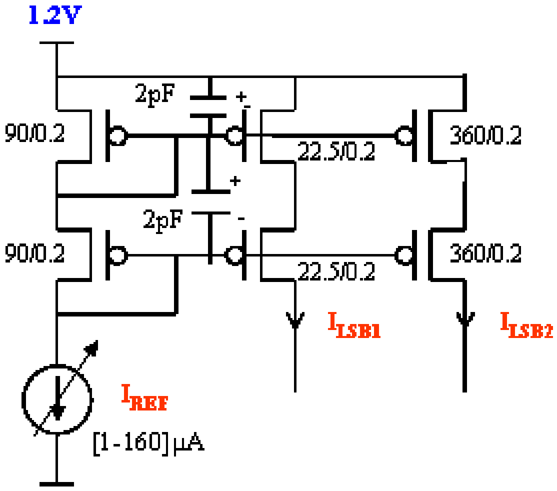


Figure 3.12: Current Mirror

High output impedance is highly needed so as there is no change in the source current due to changes in the output node voltage. PMOS transistors are sized for high precision for I_{REF} between 1 µA and 160 µA. Greater current levels would require larger devices and more parasitic capacitances. The large dynamic range of I_{REF} involves about 45 dB current control and transistors operate at 1.2 V. Two capacitors of 2 pF are placed to fix the critical nodes of the circuit and improve current accuracy by reducing the drain-to-source voltage variation. The topology in Fig. 3.12 is simulated using ELDO for a variable reference current I_{REF}. This architecture, which divides the output current value by a factor of 4 to generate I_{LSB1} and uses a x4 current mirror to generate I_{LSB2} (:4x4 notation in Fig. 3.13) is compared to the same current mirror where I_{LSB1} is a replica of I_{REF} and I_{LSB2} is generated by a x16 current mirror (x1x16). Both topologies are simulated for two different values of transistor length. Minimum technological value lengths of 0.13 µm and 0.2 µm are used for transistor sizing. In Fig. 3.13 the current ratios between I_{LSB1} and I_{LSB2} (theoretical value of 16) are shown for the four possible configurations. Short channel devices worsen mirror accuracy increasing the error in the current replica operation. Since channel modulation factor λ is inversely proportional to length L, transistors are not sized to L_{min} but to 0.2 μm. As we can see in Fig. 3.13, the accuracy (in the entire current range) is better in the case of the configuration which divides and multiplies the reference current by a factor of four (:4x4) than in the case where I_{LSB1} is equal to I_{REF}.

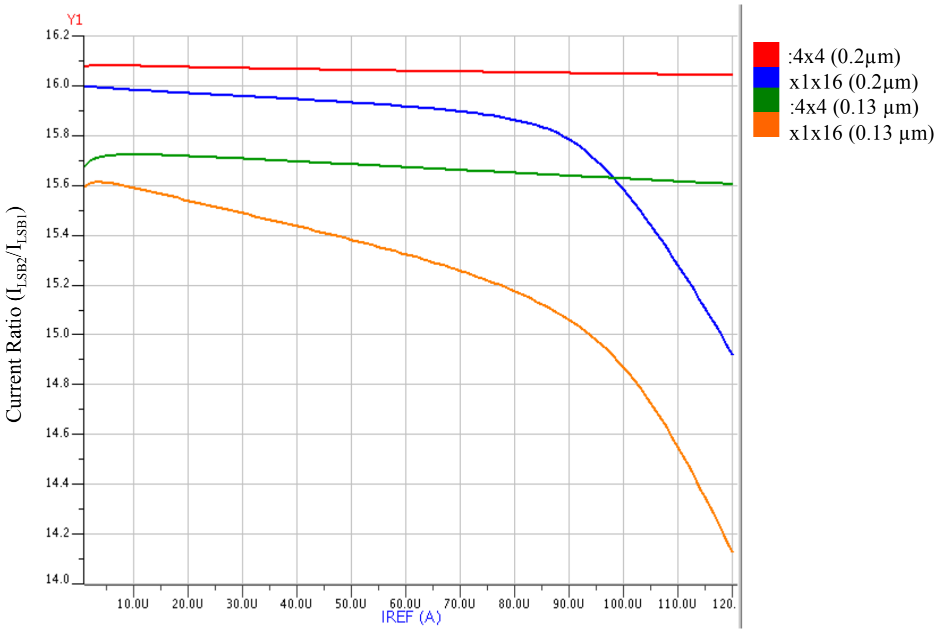


Figure 3.13: Current Mirrors Simulation for L=0.13, 0.2 μm

3.3.4 Bias Circuit

The bias circuit generates the required gate and base bias voltages for the cascode current cell transistors as depicted in Fig. 3.14.

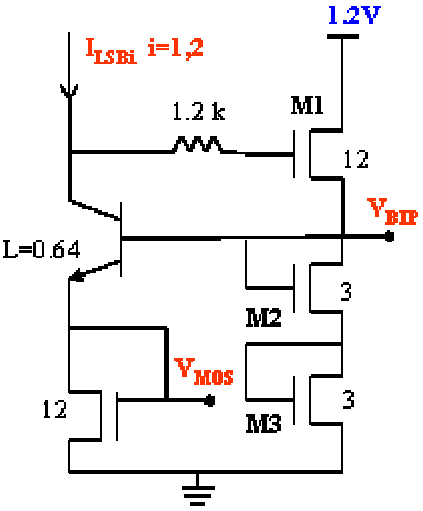


Figure 3.14: Bias circuit

This architecture (called BC in this work) is simulated in ELDO and compared with a classic topology without transistors M1, M2 and the 1.2 kΩ resistor and the results are shown in Fig. 3.15. Results corresponding to the worst case for each sub-DAC (x16 and x256 current ratios) are considered in our simulations. The differential error is used as decision parameter and is defined as:

$$Er(x)=\frac{x'-x}{x}.100\,(\%) \tag{3.16}$$

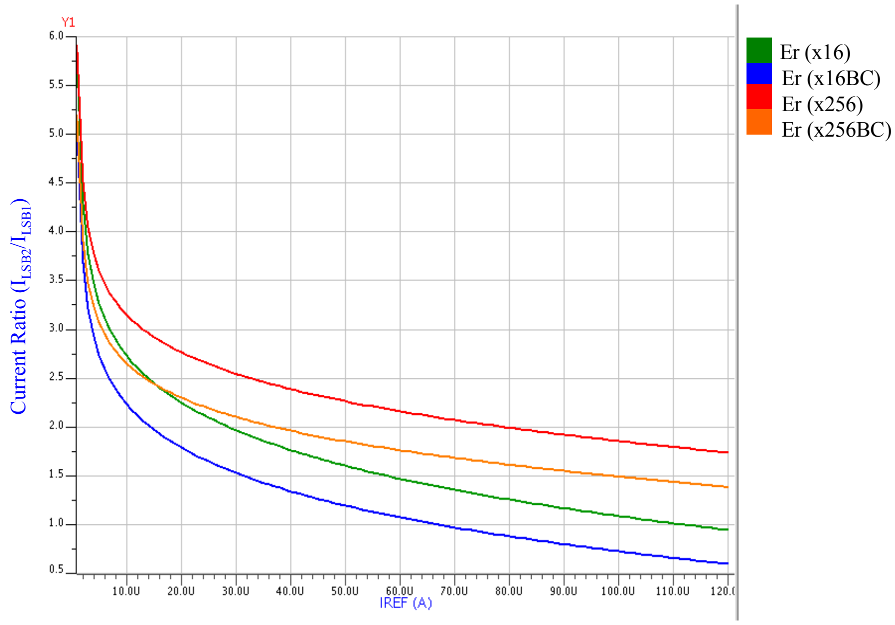


Figure 3.15: Bias circuit Simulation for 16 and 256 current ratios (differential error)

The differential error is reduced by about a factor 1.25 when the bias circuit in Fig. 3.14 is used improving the accuracy of the global converter.

Another parameter to consider is the speed of the conversion, which depends on the regulation of voltages V_{BIP} and V_{MOS}. A step current with period of 1 ns, is used as stimuli and enables us to characterize the high-speed operation of the DAC as a function of the bias circuit design. The impact on the current, which handles with the greatest value of current (x256) is simulated and the results are shown in Fig. 3.16.

This topology enhances the output characteristic of a classic current mirror (accuracy and higher speed operation). Placing a resistor in the gate of transistor M1 regulates bias voltage V_{BIP}. N-type diodes M2 and M3 help to the regulation of the output voltage as well helping to a high-speed operation in the converter

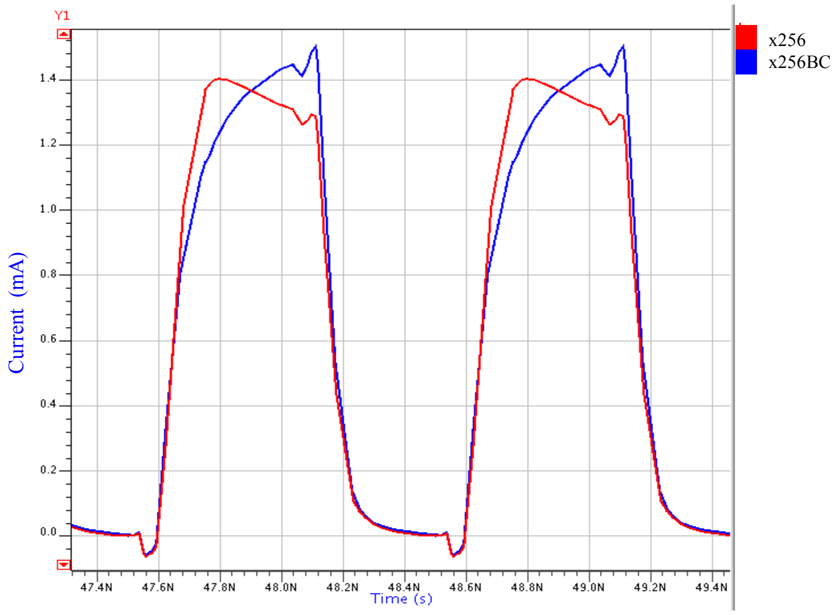


Figure 3.16: Bias circuit Simulation for 256 current ratios (I_{REF}=80 µm)

3.3.5 Cascode Current Source

The cascode configuration of the current cell presents high output impedance that enhances the static linearity of the converter and it is plotted in Fig. 3.17. In order to have the same conditions in all the current cells, the ratio current/width has to be constant.

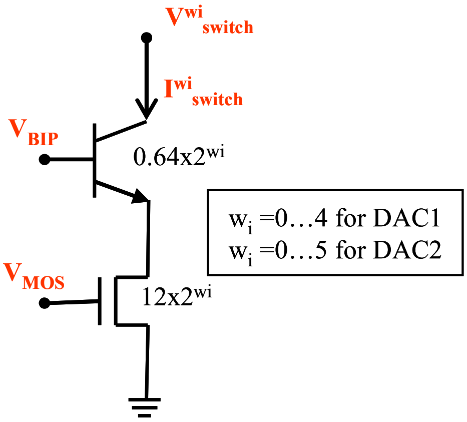


Figure 3.17: Cascode current source

The transistor sizes are related to the value of the current flowing through the current source, which depends on the weight of the cell ($I^{w_i}_{switch}$), and are expressed as

$$I^{w_i}_{switch} = 2^{w_i}.I_{LSB1} \text{ with } w_i = 0...4 \text{ for DAC1} \qquad (3.17)$$

$$I_{switch}^{w_i} = 2^{w_i}.I_{LSB2} \text{ with } w_i = 0...5 \text{ for DAC2} \tag{3.18}$$

with I_{LSB1} and I_{LSB2} given by eqns. 3.14-3.15.

To demonstrate the operation of these cascode current sources, this circuit (together with the wide-dynamic range current mirror and the bias circuit presented in previous sections) is simulated using ELDO. All the nine current sources are considered in our simulations (x1…x256) and the differential error is calculated to study the accuracy of this sources. Simulation results are shown in Fig. 3.18.

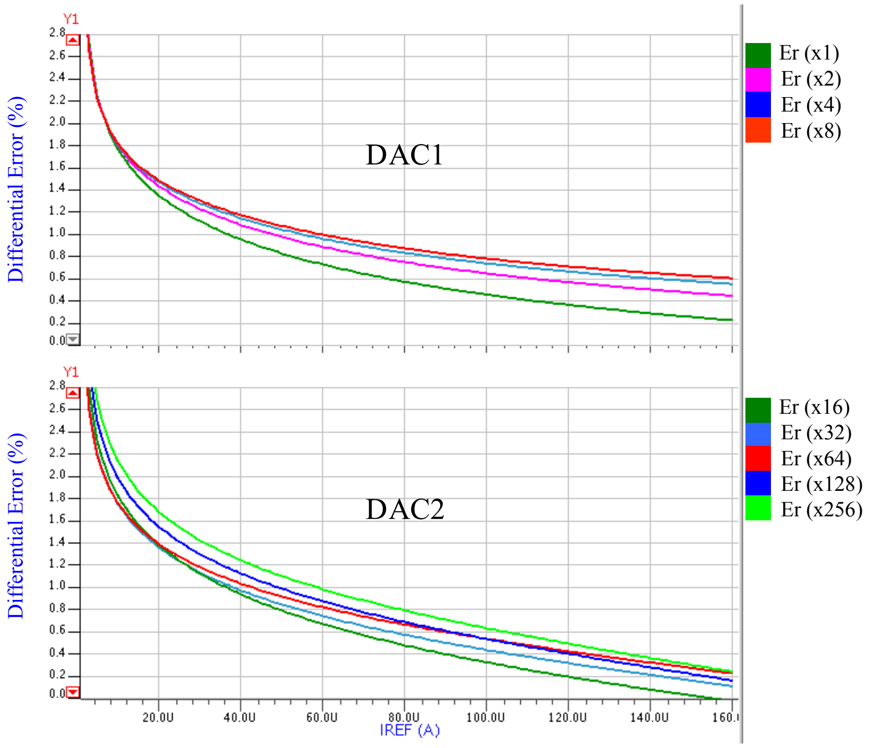


Figure 3.18: Current sources (differential error)

As it is shown in Fig. 3.18, the differential error of the current ratio is minimized for the case of the 5-bit DAC2. In effect, as explained before, wide-dynamic ratio generates with great accuracy the I_{LSB2} current (x16 ratio). This is important since if the differential error in the x16 current source is reduced the accuracy in the sources representing the Most Significant Bits in the converter will be increased and thus the global accuracy. The differential error remains lower than 2 % for current values greater than 10 µA. Better matching is achieved by letting the smallest transistors become the unit size and building the larger transistors from multiple parallel copies of the unit device. In layout, a current source with weight w_i is implemented as the multiplication in parallel of 2^{wi} sources to increase the matching between the current cells.

3.3.6 Switches

The switches steer the current to the positive or negative output. The load resistances convert this current into a voltage. For the correct function of the DAC, it is crucial that the currents always flow into only one output. That is to say, there is only one transistor turned on while the other is turned off. If CMOS logic (PMOS transistors) is used to implement the switching function, the PMOS transistors would be very sensitive to the cross of the controlling signals *DATA* and its complement. It happens that both transistors are turned on or off simultaneously degrading the dynamic performance of the converter. To avoid this and improve the speed of operation of the pair of switches, high-speed bipolar transistors are placed instead of PMOS transistors. Furthermore, bipolar switches will require small voltage difference (30 mV) in the controlling signals to be turned on-off.

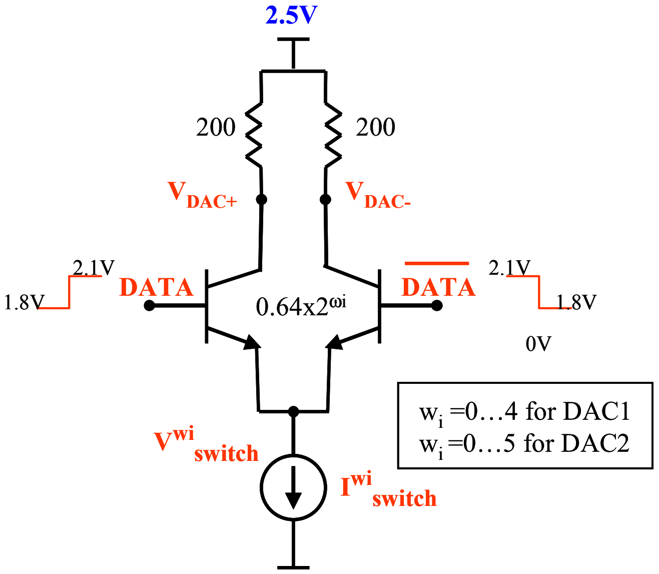


Figure 3.19: Switches and load resistors

Bipolar switches are sized to correct operation in the range of currents of the converter (I^{wi}_{switch} in Fig. 3.14). As for the case of the sizing of the transistors of the current cells, bipolar sizes are adapted to the current flowing through the devices. Fig. 3.15 illustrates the pair of switches with the loads switching a current source with a generic weight w_i of the DAC. To ensure that the bipolar transistor is in the cut-off region when turned off and in the saturation region when turned on, driving signals of about 300 mV (1.8 V for '0' logic value and 2.1 V for '1' logic value) are input to the base of the transistors. The commanding signals are the outputs of the interface circuit detailed in § 3.3.6.

The 200 Ω load resistors are connected to the power supply and convert the total currents of the nine cells into an output differential voltage. To correct bias the cascode current cell and the bipolar switches, power supply of 2.5 V is required. The interface circuitry performs the level-shifter of the 1.2 V driving signals assuring the correct biasing of the bipolar switches. The topology depicted in Fig. 3.19 is simulated with ELDO. The stimuli signals are respectively two ideal pulses and the output of the implemented interface circuit of time duration of 250 ps and are expressed as Stimuli and its complementary StimuliB in Figs. 3.20-3.21. The current value steered by the switches is 50 µA. For simplicity, we express in both figures the current flowing in one switch as I_Switch and the complementary current of the other switch as I_SwitchB.

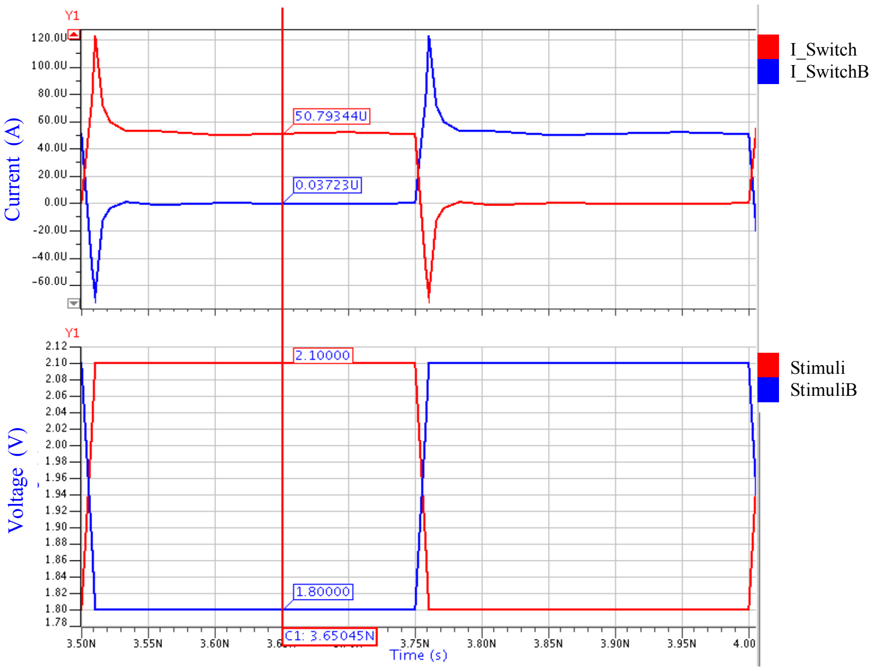


Figure 3.20: Switches operation @4GHz (Ion=50 µA)

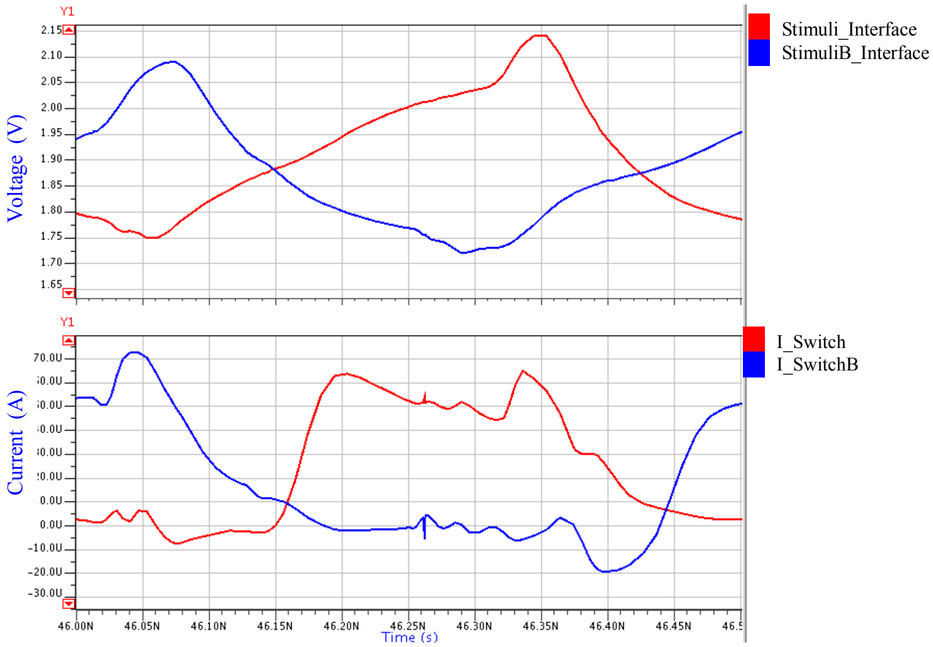


Figure 3.21: Switches operation @4GHz (Ion=50 µA) with Interface Circuit

High-speed operation of the bipolar switches is proved. The current is switched from one output to the other at the rate of the stimuli signal (4 GHz). When one switch is on the other is off assuring the perfect operation of the pair of switches. However, even when the stimuli signal is generated by the interface circuit and then limited in frequency (see Stimuli_Interface and StimuliB_Interface signals in Fig. 3.21), the switches performances are limited by the interface speed. In next section, the interface circuit is studied and designed to improve the high-speed operation of the converter.

3.3.7 Interface Circuit

This circuit interfaces the 1.2 V CMOS logic part of the architecture (referred as $B_{0:8}$ in Fig. 3.11) with the 2.5 V operation of the BiCMOS DAC. The CMOS logic signals are rail-to-rail (supply to ground) signals. Differential bipolar stages require only about 300 mV switching voltage. CMOS signals cannot be applied directly to the base of the bipolar transistors so the interface circuit converts the rail-to-rail (1.2 V) signal into 300 mV in this design.

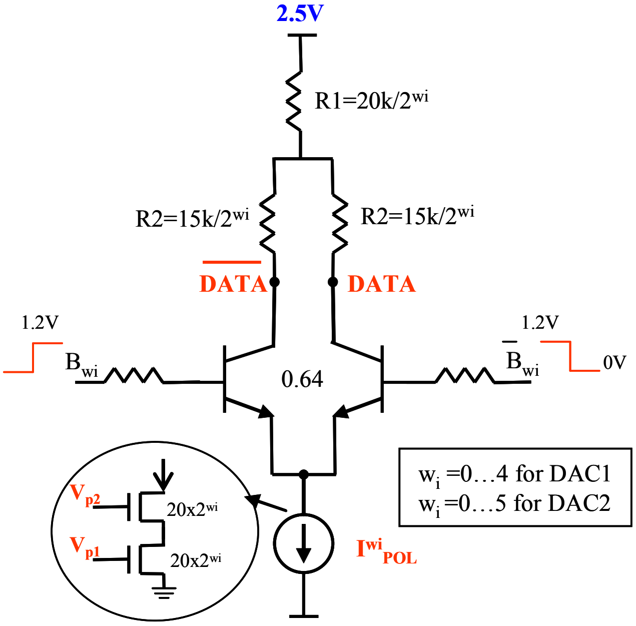


Figure 3.22: Current cell of the interface block with the level shifter

The schematic of a generic current cell with the level-shifter of the interface circuit is shown in Fig. 3.22. Complementary output signals DATA and $\overline{\text{DATA}}$ have amplitudes of 300 mV and are the driving signals of the bipolar switches in Fig. 3.19. The current mirror which replicates this 20 µA (eqn. 3.23) reference current (I_{POL}) is composed of two NMOS transistors where the gate and the drain are connected together (n-type diode) and sized with length larger than L_{min} size to reduce the channel-length modulation as shown in Fig. 3.23.

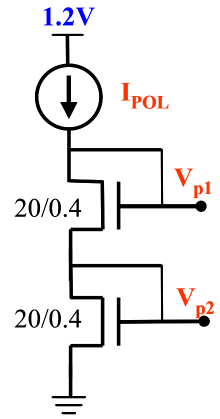


Figure 3.23: Current mirror for the interface block

The '0' logic value is represented with a 1.8 V signal and the '1' value with an amplitude of 2.1 V (see eqns. 3.18-3.21). To do this, resistors are used to shift the logic value. Resistor R1 and R2 are designed according to:

$$2.5 - I_{POL}{}^{w_i} R1 = 2.1 \tag{3.19}$$

$$2.1 - I_{POL}{}^{w_i} R2 = 1.8 \tag{3.20}$$

with

$$I_{POL}{}^{w_i} = 2^{w_i} . I_{POL} \text{ with } w_\text{i} = 0...4 \text{ for DAC1} \tag{3.21}$$

and

$$I_{POL}{}^{w_i} = 2^{w_i} . I_{POL} \text{ with } w_\text{i} = 0...5 \text{ for DAC2} \tag{3.22}$$

Bias current value for the least significant current cell is

$$I_{POL} = 20\,\mu\text{A} \tag{3.23}$$

Therefore, R1 and R2 can be written as:

$$R1 = \frac{0.4}{(20\mu\text{A}).2w_i} \quad (\Omega) \tag{3.24}$$

$$R2 = \frac{0.3}{(20\mu\text{A}).2w_i} \quad (\Omega) \tag{3.25}$$

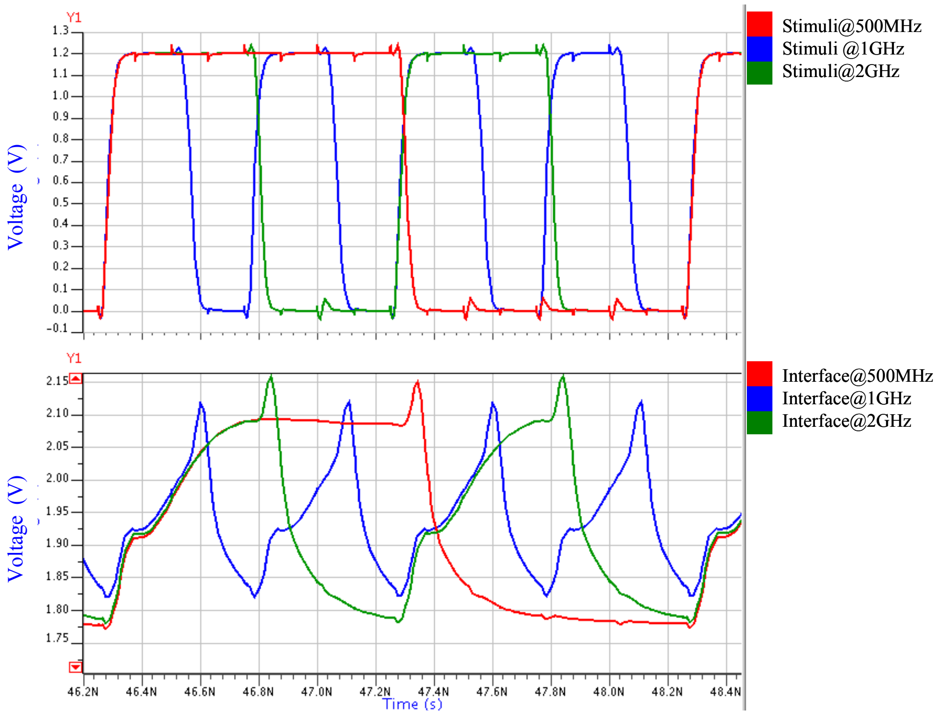


Figure 3.24: Interface Circuit Output Voltages for stimuli signals @ 500 MHz, 1GHz and 2 GHz

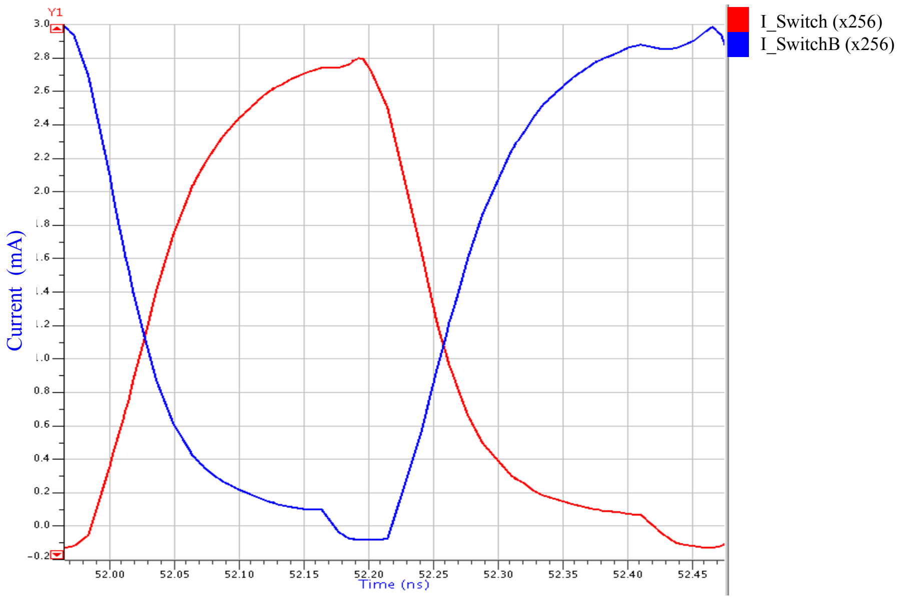


Figure 3.25: Collector currents of the bipolar x256 switches for I_{REF}=40µA) @ 2GHz

The performance of the interface circuit is studied using ELDO simulations. Three stimuli signals of frequencies 500 MHz, 1 GHz and 2 GHz and amplitude of 1.2 V are input to the interface circuit and the results are shown in Fig. 3.24. Even if at the higher frequency the interface output is quite distorted, the bipolar switches keep on working correctly. They need only a small voltage difference in the command signals and are less sensitive to the edge of the driving signals (Interface signals) than MOS switches. The collector currents for switches which steer the x256 current (256 times I_{LSB1}) are depicted in Fig. 3.25 for a stimulus of 2 GHz (minimum time duration of 250 ps) and I_{REF} equal to 40 µA (I_{LSB1}=10 µA). Both current are complementary which proves that the bipolar switches steer the proportional current (in this case x256 I_{LSB1} or x16 I_{LSB2}) from one of the inputs at the time assuring the correct operation of the converter at high frequencies.

3.3.8 DAC Simulations

Finally, the whole designed DAC is simulated in this section. The DAC is composed of all the building blocks presented in § 3.3. A static study is performed to obtain the INL and DNL errors. A ramp is generated and fed to the 9-bit DAC using ELDO. The INL and DNL errors are shown in Fig. 3.26.

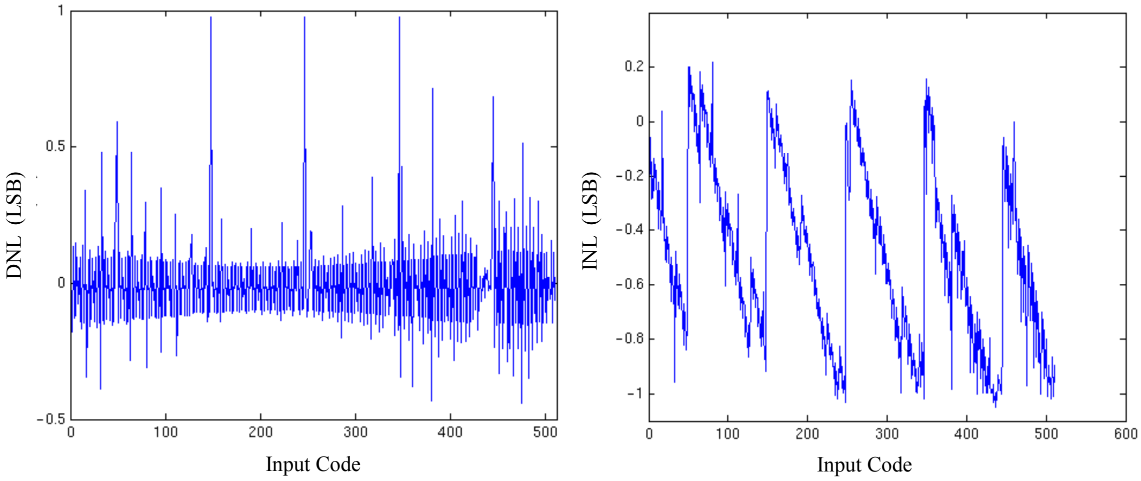


Figure 3.26: DNL and INL errors for the simulated 9-bit DAC

As shown in Fig. 3.26, the INL and DNL errors are lower than 1 LSB for all the input codes. The DAC is said to be monotone with no missing codes.

Now, we will study the dynamic performance of the designed DAC. A continuous wave test is performed. The purpose is to prove the 45 dB gain control and estimate the linearity of the converter in terms of the SFDR parameter. Two input signals are fed to the test circuit. The first stimuli is a full-scale, 100 MHz sinusoid sampled and converted by an ideal 9-bit ADC available in the ELDO *mgclib* library and operating at a frequency of 3 GHz. A second stimulus, a sine wave of 800 MHz is sampled at 8GHz.

In Fig. 3.27, single-ended output power spectra for I_{LSBmax}=40 µA and I_{LSBmin}=100 nA are shown for both stimuli.

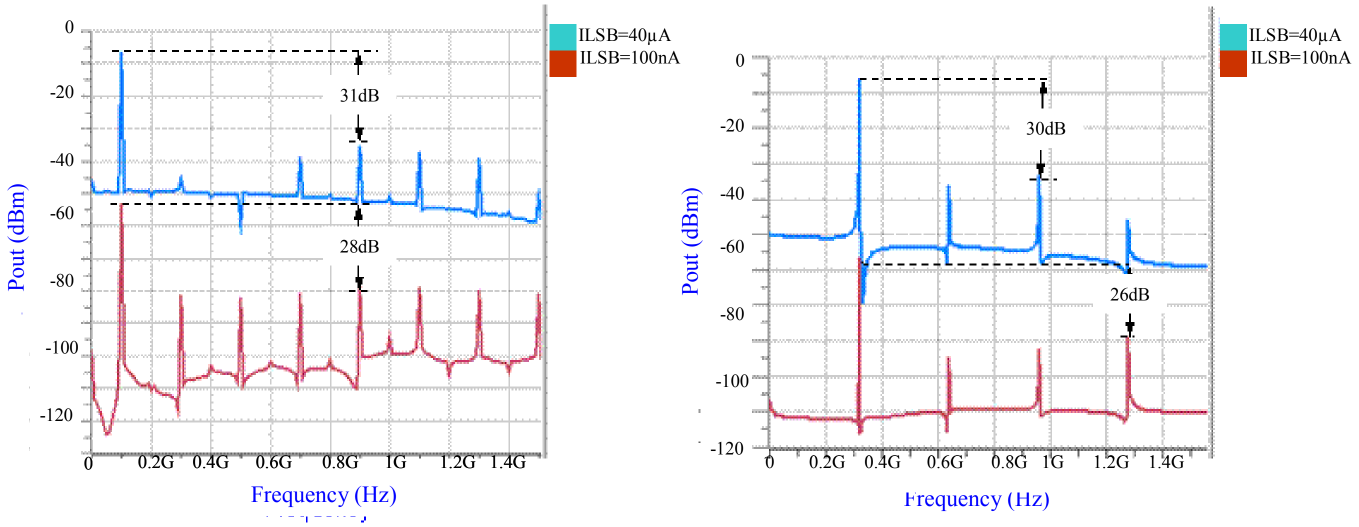


Figure 3.27: Single-Ended Output Power Spectra (f_{sin}=100MHz sampled at 3 GHz on the left plot and 8 GHz on the right plot) for ILSB=100nA&40uA

The differential output power is varied of about 45 dB (from -52 dBm to -6 dBm) with a SFDR greater than 26 dB.

3.4 DAC Test

In order to dynamically test the 9-bit DAC described in § 3.3, a sine-wave generator is considered in this section. . In the design of the DDFS circuit, the proper logic type (see Appendix A) will be chosen in function of the required performances of each building block. Standard CMOS is used for implementing complex logic functions for its simplicity. Transmission-gates are preferred for multiplexors and XOR-gates.A 1.4 GHz 9-bit CMOS Read Only Memory-less Direct Digital Frequency Synthesizer (DDFS) is designed. Logic CMOS gates have been used instead of area consuming ROM (sine look-up table) to convert phase word into sine wave amplitude directly [Turn06]. This circuit allows verifying the targeted 45 dB gain control of the designed DAC

3.4.1 DDFS Circuit Design

This circuit uses a traditional DDFS architecture [Tier71] with a phase accumulator and a phase-to-sine converter to drive the 9-bit DAC of § 3.3 (see Fig. 3.28).

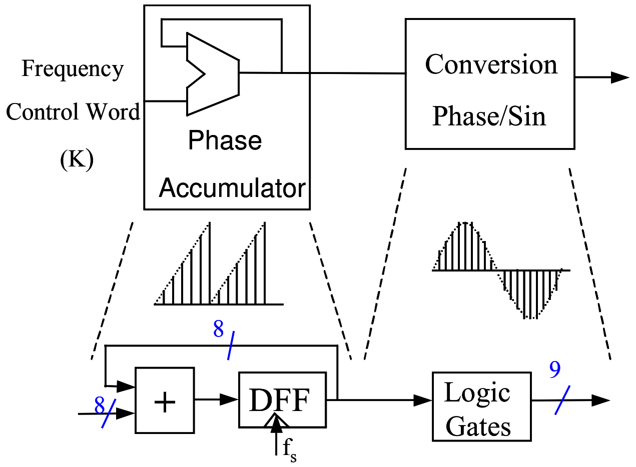

Frequency
Control Word
(K)
Phase
Accumulator
Conversion
Phase/Sin
8
8
+
DFF
f_s
Logic
Gates
9

Figure 3.28: DDFS architecture

The phase accumulator in this design is composed of an 8-bit carry-skip adder with the structure similar to the used for the design of the Sigma-Delta converter [Hibo06PhD]. The outputs of the adder have Data Flip-Flops (DFFs) and the output bits feedback and sum with the increment that is the frequency control word (K). The 8-bit ramp output is truncated so that the six most significant bits denoted as S_7 to S_2 are used for phase conversion.

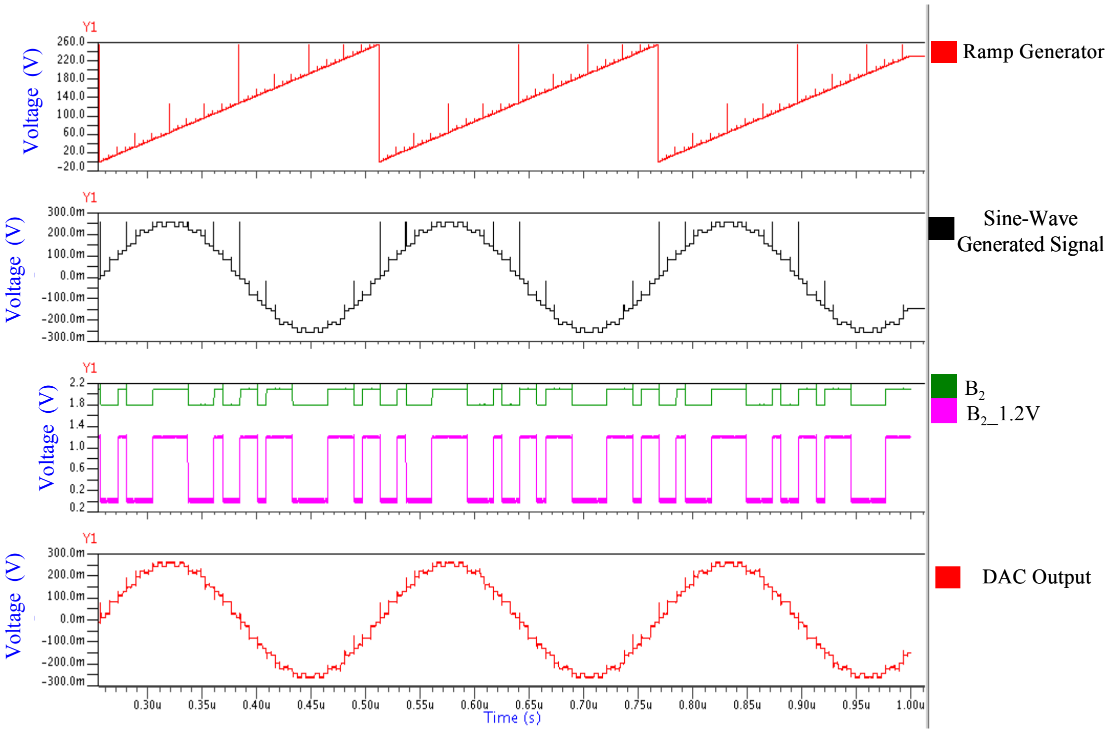


Figure 3.29: Simulation results of the DDFS together with the DAC

The design of this phase converter is converted into a sine wave by using logic gates. In this research, we take the proposed algorithm in [Turn06] and we adapt it to our application. The logic expressions given there are simplified to an easy implementation and an extension to a 9-bit output word is applied. Also, the 9-bit are binary weighted instead of different weights (fine binary and coarse bits with a weight of 16) used in the before mentioned paper. For additional information about the conversion algorithm refers to [Turn06PhD].

In Fig. 3.29, the main curve obtained in simulation of the DDFS (ramp generator, DDFS output and bit B_2 at the input and the output of the DDFS, respectively $B_{2\_1.2V}$ and B_2) is illustrated together with the DAC output. Logic functions are implemented using standard CMOS, which is more flexible for implementing general logic functions. Due to the different carrier drift velocities in NMOS and PMOS transistors, width ratio (W_{PMOS}/W_{NMOS}) is determined by simulation to be about 1.8, leading to symmetrical rise and fall times. For implementing multiplexors and XOR-gates, transmission gates, leading to simpler circuits are preferred. The logic functions used for this converter and their implementations are illustrated below (Figs. 3.30-3.37).

$$A = S_5 \oplus S_6 \tag{3.26}$$

$$B = S_4 \oplus S_6 \tag{3.27}$$

$$C = S_3 \oplus S_6 \tag{3.28}$$

$$D = S_2 \oplus S_6 \tag{3.29}$$

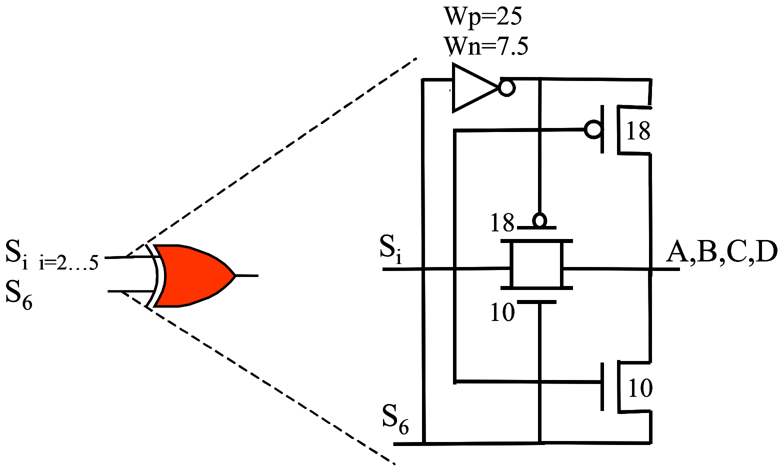


Figure 3.30: Implementation of XOR with transmission-gate logic (eqns. 3.26-3.29)

$$DAC_8 = \overline{S_7} \tag{3.30}$$

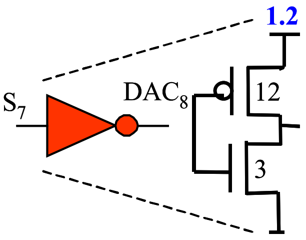

1.2
S_7
DAC_8
12
3

Figure 3.31: Implementation of DAC8

$$Z = (A + BC).\overline{S_7} \tag{3.31}$$

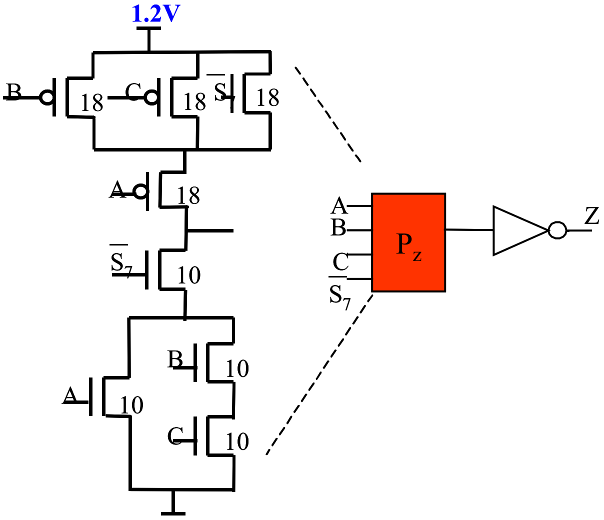

1.2V
B
18
C
18
$\overline{S}$
18
A
18
$\overline{S_7}$
10
B
10
A
10
C
10
A
B
C
$\overline{S_7}$
P_z
Z

Figure 3.32: Implementation of Z (eqn. 3.31)

$$DAC_7 = ((\overline{A + BC}).S_7 + \overline{S_7}) \oplus Z \oplus DAC_8 = (\overline{(A + BC).S_7}) \oplus Z \oplus DAC_8 \tag{3.32}$$

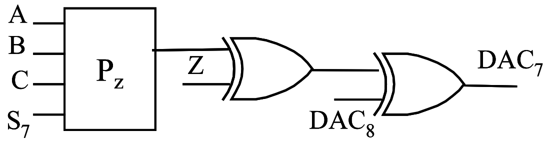

A
B
C
S_7
P_z
Z
DAC_8
DAC_7

Figure 3.33: Implementation of DAC_7

$$DAC_6 = ((B \oplus C) + A) \oplus S_7 \tag{3.33}$$

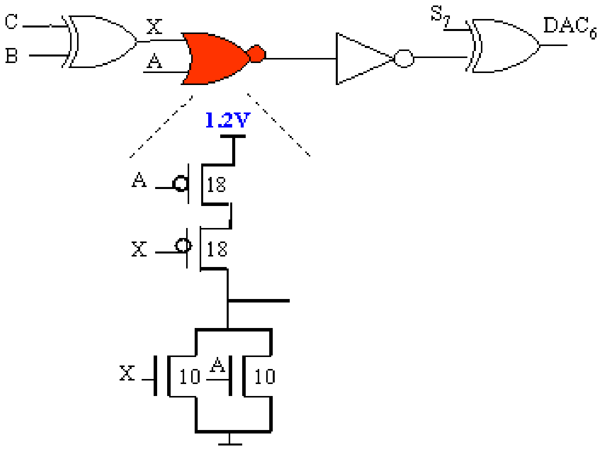

C
B
X
A
S7
DAC6
1.2V
A
18
X
18
X
10
A
10

Figure 3.34: Implementation of DAC_6

$$DAC_5 = \overline{(\overline{A}C + \overline{B})} \oplus S_7 \tag{3.34}$$

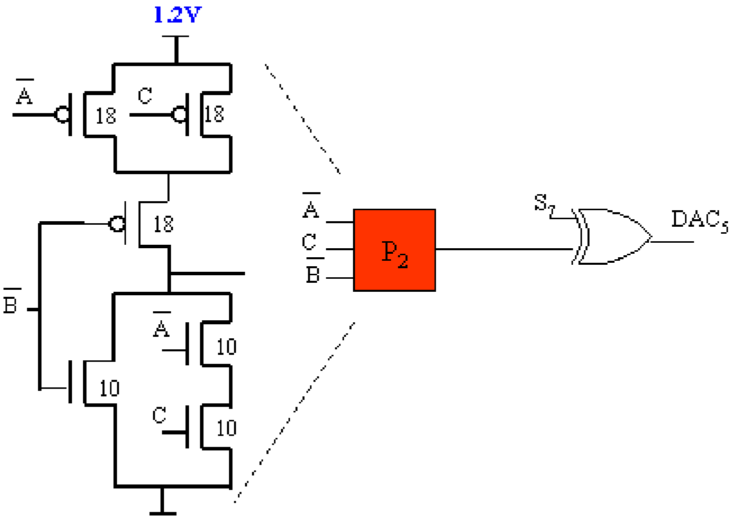

1.2V
$\overline{A}$
18
C
18
18
$\overline{B}$
$\overline{A}$
10
10
C
10
$\overline{A}$
C
$\overline{B}$
P2
S7
DAC5

Figure 3.35: Implementation of DAC_5 and DAC_2

$$DAC_4 = ((\overline{\overline{A}\overline{B} + \overline{C}}) + (\overline{A + B}).D) \oplus S_7 \tag{3.35}$$

$$DAC_3 = ((\overline{\overline{A}\overline{B} + \overline{D}}) + (\overline{A}\overline{C} + AB)) \oplus S_7 \tag{3.36}$$

$$DAC_2 = DAC_5 \tag{3.37}$$

$$DAC_1 = DAC_4 \tag{3.38}$$

$$DAC_0 = DAC_3 \tag{3.39}$$

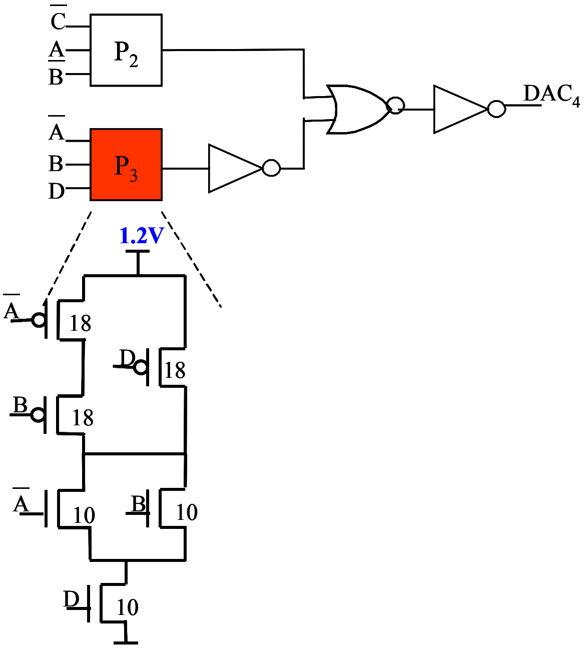

C
A
B
P2
A
B
D
P3
DAC4
1.2V
A
18
D
18
B
18
A
10
B
10
D
10

Figure 3.36: Implementation of DAC_4 and DAC_1

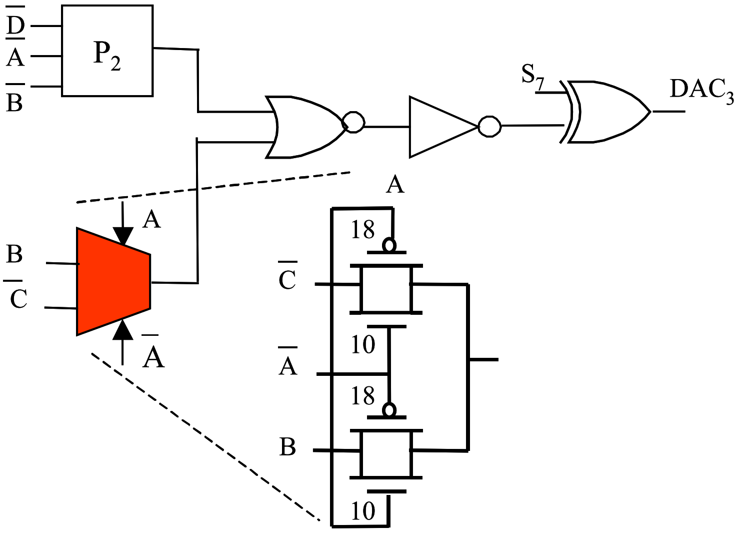

D
A
B
P2
S7
DAC3
A
B
C
A
A
18
C
10
A
18
B
10

Figure 3.37: Implementation of DAC_3 and DAC_0

The main simulation results of the designed DDFS are (Post-Layout Simulations PLS of circuit shown in Fig. 3.38):

Resolution	f_{min}	f_{max}	Sampling Frequency	SFDR	Dissipated Power
9 bits	390kHz	10.93MHz	1.4GHz	27.5dB	3.5mW (1.2 V)

Table 3.3: Features of the designed DDFS (post-layout simulations)

3.4.2 Whole Implementation of the DAC

In addition of the 9-bit DAC and the test circuit, the total circuit needs a cascade of two inverters (input buffer) and 8 DFFs. The DFFs are placed before the adder to synchronize the input bits to the adder. The input buffer is designed in such a way to be able to accept a given load (fan out). The buffer is composed of two stages, each of them being loaded by an increasing load. A trade-off between the resistance Ron and the capacitance Cgs must be considered. Transistor sizes are gradually increased in a way that the delay increases less fast than the load ratio. Transistor sizes are: 12/3 µm and 25/7 µm. This input buffer receives the clock signal and outputs a logic signal.

3.5 Fabricated Chip

A test chip was fabricated in STMicroelectronics 0.13 µm BiCMOS process to demonstrate the performance of the DAC. The chip includes the synchronization Data Flip-Flops (DFFs), the level shifters to interface logic transmitter with a supply voltage of 1.2 V and the 2.5 V DAC and the digital-to-analog conversion block together with the DDFS block. DAC circuit is 160x160 µm^2 in size and with the DDFS block for dynamic test, final circuit is 160x220 µm^2 (see Fig. 3.38).

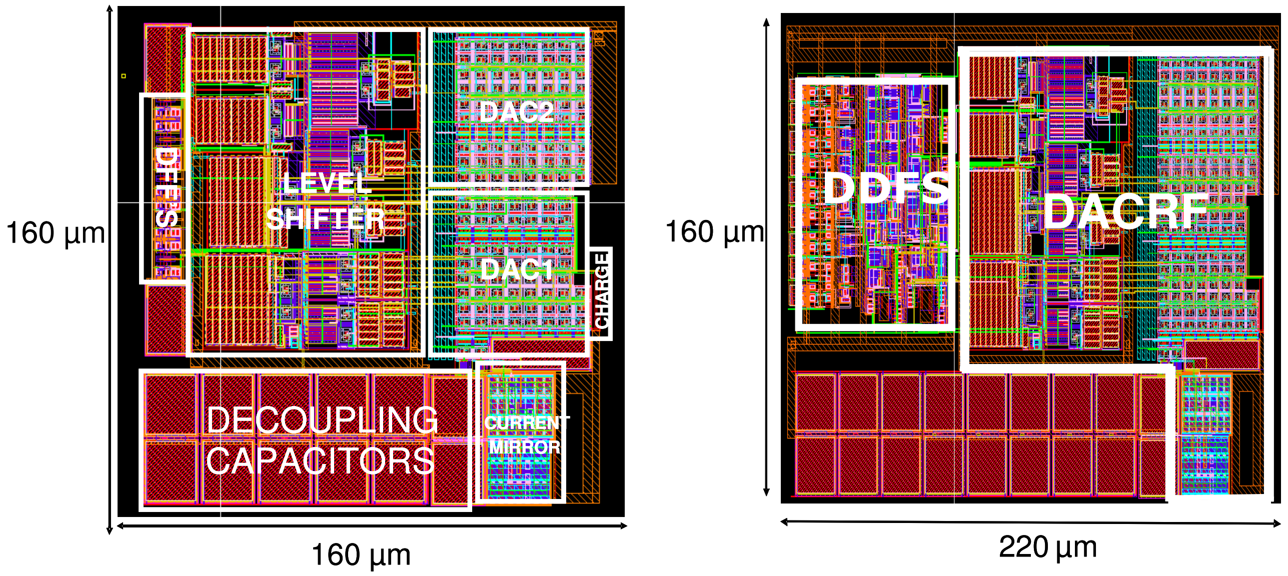


Figure 3.38: Stand-alone DAC and DAC with DDFS layouts

The die is directly mounted on and electrically interconnected to its final circuit board (Chip-on-

Board COB) leading to shorter interconnection paths. Multiple ground pads on the chip were bonded to reduce the parasitic inductance. To minimize the effect of the parasitic inductances and resistors of the bounding, 20 pF decoupling capacitors are placed near each supply circuit. The PCB is a 2-layer Rogers RO4350 board. The PCB integrated circuit used for the circuit test is shown in Fig. 3.39. The clock and differential output strips have been calculated to be adapted to 50 Ohms. A 200 Ω to 50-Ω impedance converter is used on a wide frequency range. Fig. 3.40 illustrates the bonding of COB.

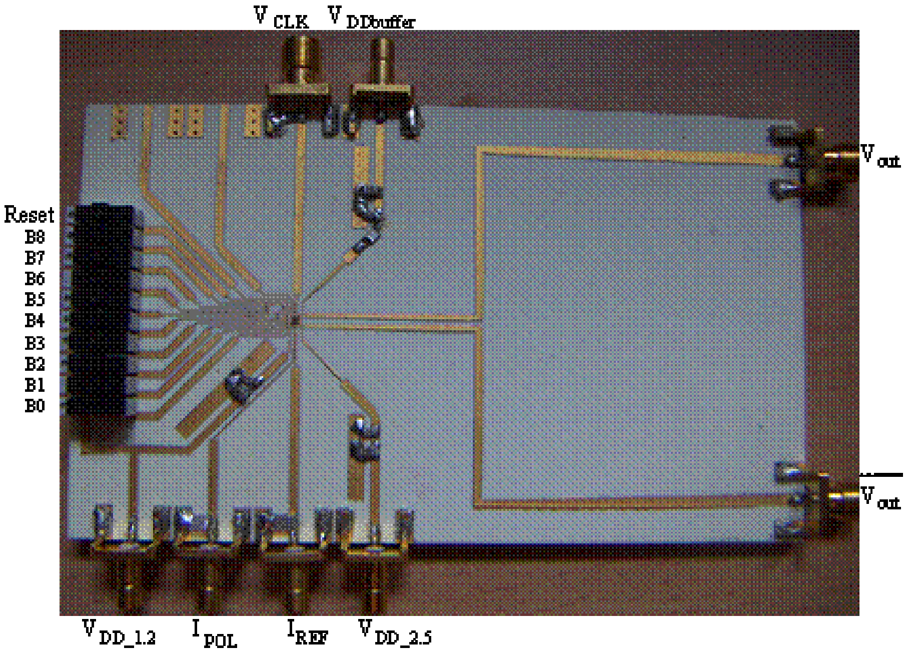

V CLK
V DDbuffer
Reset
B8
B7
B6
B5
B4
B3
B2
B1
B0
V out
$\overline{V}$ out
V DD_1.2
I POL
I REF
V DD_2.5

Figure 3.39: PCB Integrated Circuit

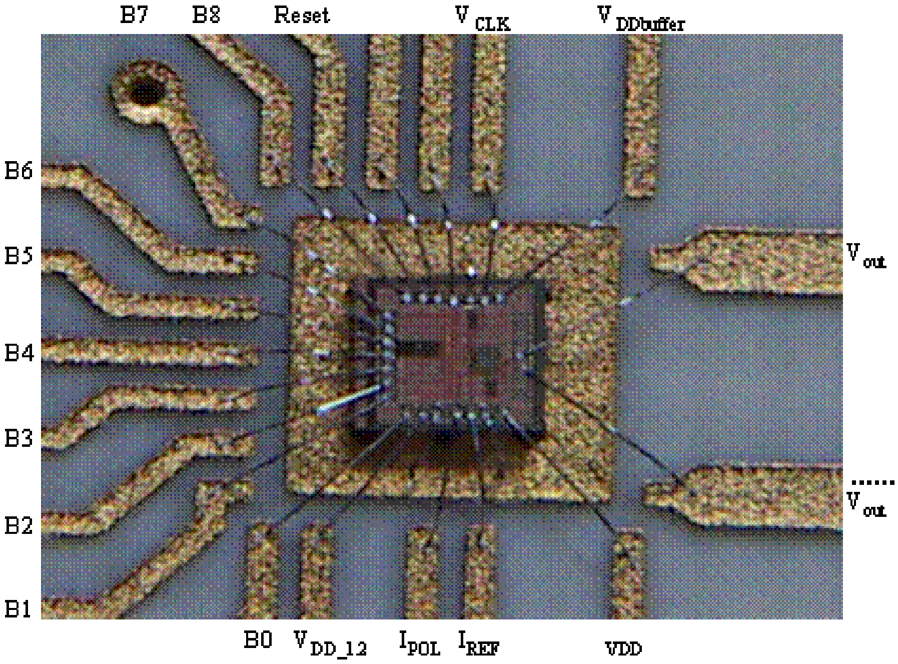

B7
B8
Reset
V CLK
V DDbuffer
B6
B5
B4
B3
B2
B1
V out
$\overline{V}$ out
B0
V DD_1.2
I POL
I REF
VDD

Figure 3.40: Chip-on-board

3.6 Measurements Results vs. Simulation Results

We present in this section the comparison between the simulation results obtained after parasitic extraction of the layout and the measurement results of the DAC with the sine-wave generator. In our simulations, the parasitic related to the PCB are also included. Figs. 3.41-3.42 show the single-ended output power measured (50 Ω load) at the minimum frequency (f_{out}=390 kHz with f_{clk}=100 MHz) and at the maximum frequency (f_{out}=10.93 MHz with f_{clk}=1.4 GHz) synthesized sine waveforms after conversion by the DAC. They are compared to the simulations results obtained by ELDO simulation tool. The results are plotted over gain control (variable reference current I_{REF}).

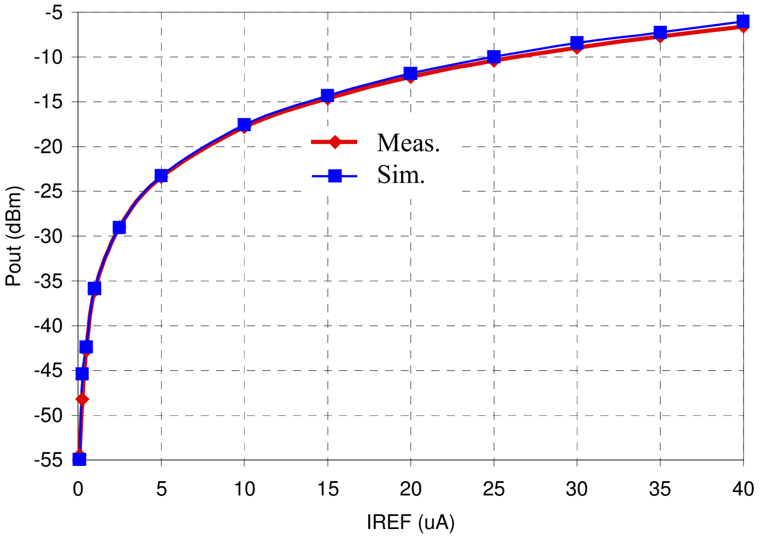


Figure 3.41: Single-ended output power @ 100 MHz clock

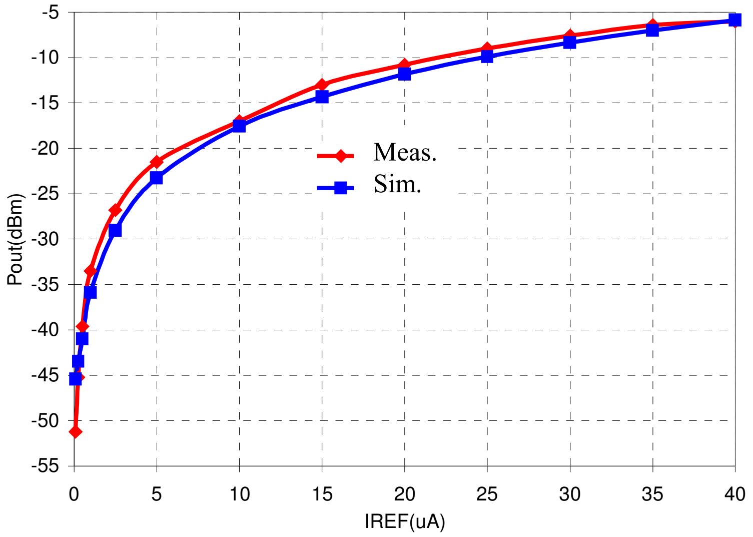


Figure 3.42: Single-ended output power @ 1.4 GHz clock frequency

Beyond an output power of -6.4 dBm (reference current value of 35 µA), the output power enters the saturation region. The DAC converts the digital input signal adjusting its output power from -

51 dBm to -6 dBm (R_L=50 Ω), which means a power variation of 45 DB. A SFDR plot over output power clocked at 1.4 GHz is illustrated in Fig. 3.43.

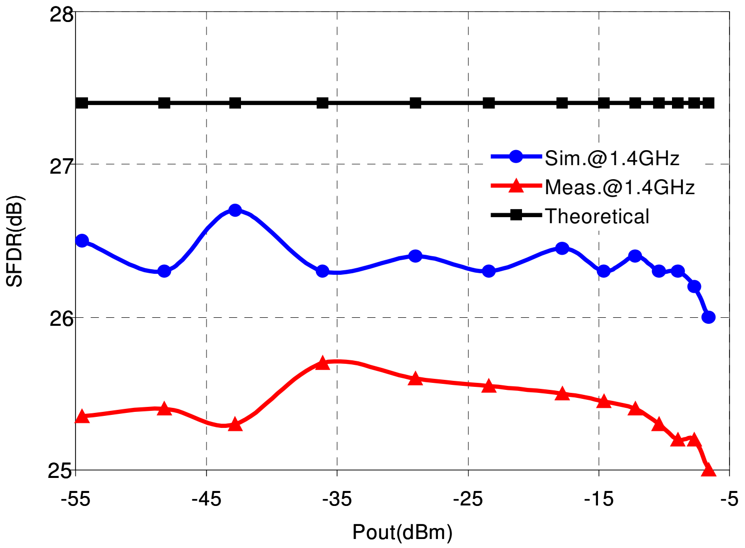


Figure 3.43: SFDR @ 1.4 GHz clock frequency

The DDFS generator allows measuring the performances of the DAC for a dynamic input. It synthesizes a variable frequency sine signal. SFDR is measured by taking the difference of the main signal tone and next highest tone in a band from DC to Nyquist frequency being the best SFDR of 27.3 dB (theoretical value). The designed DAC converts the digital input signal with an SFDR>25 dB over 45 dB power control at the highest test-demonstrated frequency. The circuit has been demonstrated to operate at 1.4 GHz. This frequency limitation comes from the DDFS chip.

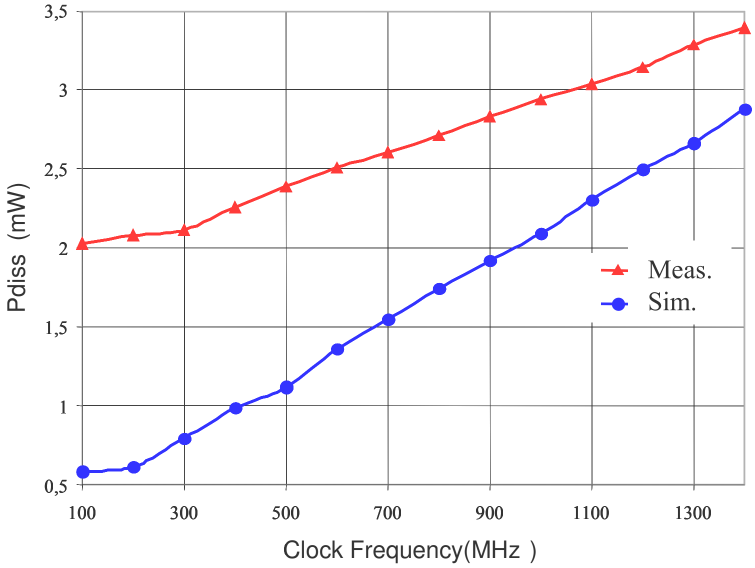


Figure 3.44: Dissipated power of DDFS

This chip can synthesize sine waves at the before mentioned maximum clock frequency so we are not able to provide measured results at higher frequencies. If the consumption of the sine wave generator is considered, dissipated power over frequency is illustrated in Fig. 3.44.

Power dissipation in the chip is depicted in Fig. 3.45 at a clock frequency of 1.4 GS/s.

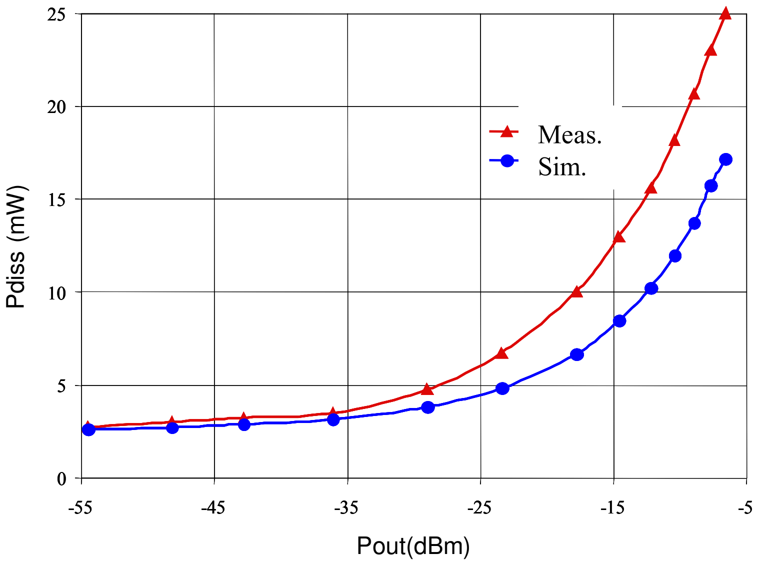


Figure 3.45: Dissipated power of the DAC @1.4 GS/s

The circuit dissipates 25 mW for the maximum single-ended output power of -6 dBm (-3 dBm differential output power).

We designed a 9-bit RF DAC with a gain control of 45 dB in 0.13 µm BiCMOS technology from STMicroelectronics. This converter operates at a demonstrated maximum frequency of 1.4 GHz (limited by the sine wave generator). Over the output power range the DAC shows a SFDR>25 dB. This chip dissipates less than 25 mW for a differential output power of -3 dBm (R_L=50 Ω). The DAC circuit has an area of 160x160 µm^2 considering only the DAC block (DFF, level shifters and conversion block) and an area of 160x220 µm^2 if the 9-bit Rom-less direct digital frequency synthesizer, which consumes less than 3.5 mW at the maximum frequency of 1.4 GHz is considered.

3.7 Conclusion

In this chapter, the design and test of a 9-bit DAC are illustrated. The DAC is designed in 0.13 µm BiCMOS technology from STMicroelectronics. The converter is divided into two full binary-weighted DACs of 4 and 5 bits. This topology allows to reduce the size ratios between the most and least significant bits related to a classic 9-bit binary-weighted structure (16 instead of 256). A cascade current mirror generates the two reference currents to vary the output currents of both sub-DACs. A bias circuit generates the required bias voltage for the gate of the MOS and the base of the bipolar transistors of the wide-dynamic current mirror. This current mirror has a dynamic current of 45 dB.

These reference currents are replicated by a factor 1, 2, 4, 8 for DAC1 (4-bit) and 1, 2, 4, 8, 16 for DAC2 (5-bit) by the BiCMOS current sources. The differential bipolar switches steer the current from one output to another depending on the control bits which are shifted in level from rail-to-rail 1.2 V signals to 300 mV signals by a bipolar level-shifter. The output currents are added in the 200 Ohms resistors and converted to the output voltage.

To test the speed and the gain control of our circuit over 45 dB, we have designed on the chip a 1.4 GHz 9-bit CMOS ROM-less direct digital frequency synthesizer (DDFS). Logic gates have been used instead of area consuming Rom (sine look-up table) to convert phase word to sine wave amplitude directly. Logic functions are implemented using standard CMOS. For implementing multiplexors and XOR-gates, transmission gates are preferred because of the simplicity.

The converter, together with the sine wave generator is designed and tested. Chip-on-board is employed as test technique. The PCB is designed also to the correct test of this circuit.

Measurement results show good correlation with post-layout simulations. They show a gain control of 45 dB and an operating maximum frequency of 1.4 GHz. This frequency limitation comes from the DDFS chip. This chip can synthesize sine waves at the fore mentioned maximum clock frequency so we are not able to provide measured results at higher frequencies. Over the output power range the DAC shows a SFDR>25 dB. This chip dissipated less than 25 mW for a differential output power of -3 dBm (R_L=50 Ω). DDFS dissipates about 3.5 mW at the maximum frequency of 1.4 GHz. The DAC circuit has an area of 160x160 μm^2 and 160x220 μm^2 if the DDFS chip is considered.

Main parameters of the designed DAC are illustrated in Tab. 3.4:

Resolution	**f_{max}**	**Pout$_{max}$ (differential)**	**Power Control**	**SFDR**	**Power Dissipation**	**Power Supply**	**Techno.**	**Die Size**
9 bit	1.4GS/s	-3dBm	45dB	>25dB	<25mW	1.2&2.5V	BiCMOS	160x160 μm^2

Table 3.4: Features of the designed DAC

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[Zimm97] R. Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic", *IEEE Journal of Solid-State Circuits*, vol. 32, no 7, p.1079-1090, July 1997.

[Raba00] J.M. Rabaey, A. Chandrakasan, B. Nikolic, "Designing combinational logic gates in CMOS", *Digital integrated circuits*, University. of Berkeley, Prentice Hall, 2000.

Chapter 4 Design and Test of the Multistandard Transmitter

4.1 Introduction

This chapter will focus on the design and test of the multistandard transmitter architecture proposed and studied in chapter 2 (Fig. 4.1). The analog combiner at the output is composed of two 9-bit Digital-to-Analog Converters that have been studied in detail in chapter 3. The description of the design methodology of the rest of blocks is considered. We note that the digital 1-bit ΣΔ modulator has been studied and designed in [Hibo06PhD] and so, is not considered in the de sign description of the transmitter.

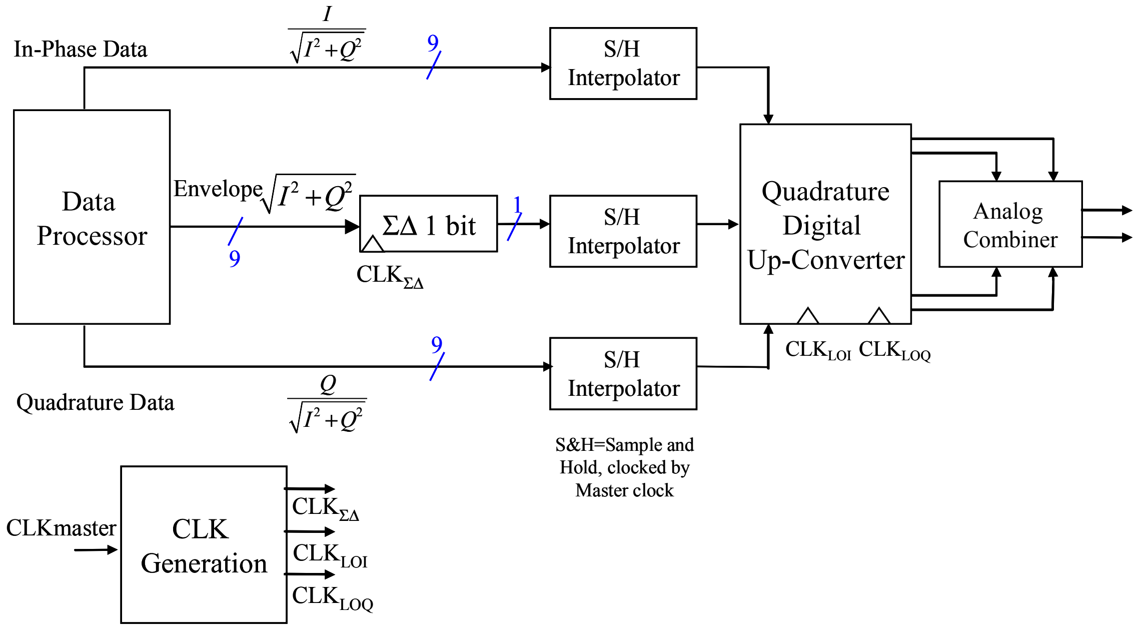
In-Phase Data
$\frac{I}{\sqrt{I^2+Q^2}}$
9
S/H Interpolator
Data Processor
Envelope $\sqrt{I^2+Q^2}$
9
ΣΔ 1 bit
$CLK_{\Sigma\Delta}$
1
S/H Interpolator
Quadrature Digital Up-Converter
Analog Combiner
CLK_{LOI} CLK_{LOQ}
9
S/H Interpolator
Quadrature Data
$\frac{Q}{\sqrt{I^2+Q^2}}$
S&H=Sample and Hold, clocked by Master clock
CLKmaster
CLK Generation
$CLK_{\Sigma\Delta}$
CLK_{LOI}
CLK_{LOQ}

Figure 4.1: Transmitter Architecture

Chapter 4 is organized as follows. Firstly, a general consideration about the convenience of representation of the numbers in the transmitter is given in § 4.2. Secondly, designs of the different Data and Set Reset flip-flops are described in § 4.3. Design methodology of the quadrature digital up-converter is explained in detail in § 4.4. Circuitry providing different clock signals on the chip is shown in § 4.5. Simulation results are discussed in § 4.6. Test set-up and measurements results from the prototype built in 0.13 µm BiCMOS are discussed in § 4.7-4.8. Finally, in § 4.9 the conclusion is drawn.

4.2 Representation

In the transmitter considered in this research, Sigma-Delta modulator needs the numbers to be in a two's complement format because a digital subtraction is performed in the circuit. IQ paths also demand for the inversion of the input bit stream for the mixing operation. For the correct operation of these blocks, 9-bit IQ signals are coded into two's complement. Negating a number (whether negative or positive) is done by inverting all the bits and then adding 1 to that result.

As we can see, in positive numbers MSB=0 and in negative numbers MSB=1. In two's complement, a single representation of 0 code exists and leads to an unsymetric code (there is no +4 representation for 3 bits). If we consider that the format of the three signals at the output of the analog to digital block conversion is straight binary, an inversion of the respective MSBs is thus necessary to code the signals into two's complement representation. The two's complement format is kept at the input of the analog combiner. The analog combiner performs an unsigned binary conversion so the MSB of the signals at its input has to be flipped again (see Tab. 4.1).

Unsigned Binary Format		Two's Complement Format	
0	**0**00	**1**00	-4
1	**0**01	**1**01	-3
2	**0**10	**1**10	-2
3	**0**11	**1**11	-1
4	**1**00	**0**00	0
5	**1**01	**0**01	+1
6	**1**10	**0**10	+2
7	**1**11	**0**11	+3

Table 4.1: MSB flip operation (3 bits)

4.3 Data and Set-Reset Flip-Flops

This section gives information about the principle of operation of the different flip-flops used in the architecture. Two main types of flip-flops are considered and presented: Data Flip-Flops

(DFF) and Set-Reset Flip-Flops (SRFF). DFF is a simple block when designed for low-speed applications, as it will be explained. However, we intend to use this circuit for different purposes in our topology so high-speed, low-glitch DFFs must be explored. In addition, when complementary signals are generated, the use of an inverter involves a non-negligible delay at high operation frequencies. DFFs are detailed in § 4.3.1. SRFF implemented in the transmitter are described in § 4.3.2.

4.3.1 Data Flip-Flop Basic Structure

The principle of operation of this circuit is quite simple. DFF has two inputs, D (for data) and CLK (for clock). In this circuit, when the clock goes up (when a leading edge type is considered), D is transferred to the output, when it goes down the output remains unchanged. The output Q stores the data until the next leading edge. The output is delayed one clock count. The flip-flop considered in this work has a reset signal (R) to force the Q signal to zero.

4.3.1.1 Data Flip-Flop Use in the Transmitter

This simple circuit works in different configurations in the proposed architecture.

4.3.1.1.1 Path Synchronization

The DFF is used as path synchronization. The three low-frequency digital paths are synchronized at the master frequency at the input of the circuit. It avoids the indeterminate state to be present and enables to buffer the three signals (envelope and IQ).

4.3.1.1.2 Zero-Order Hold Interpolation

As it is described in § 2.4.2, the 1-bit envelope signal is oversampled by a DFF clocked at the master frequency and the signal is filtered with a sinc roll-off. In this application, the DFF is interpreted as a zero-order hold (1-bit DAC).

4.3.1.1.3 Frequency Divider

Toggle DFF is used in the architecture to divide the master frequency by a power of two in order to clock the ΣΔ coder at lower frequency. The frequency divider configuration is also employed in a divide-by-2 configuration to generate the local oscillator signals in the quadrature modulator.

4.3.1.2 Design of the Data Flip-Flop

In the design of the data flip-flop, two different structures are explored. A classic Yuan-Svensson topology and one modification introduced to reduce the glitch at high frequencies and thus the current consumption.

4.3.1.2.1 Yuan-Svensson Structure

A dynamic flip-flop based on the Yuan-Svensson model is completed with an output inverter to obtain the complementary output signal Q. Extra reset (R) is connected to initiate the flip-flop avoiding unstable states (Fig. 4.2). This simple edge-triggered flip-flop was chosen for speed reasons and the ease of only one clock line. The implementation of such a 9-transistor DFF is studied in [Yuan89]. Due to the high-frequency limitations of this model, this flip-flop is only used for low-speed purposes (path synchronization). The main disadvantage of this structure is the conflicting requirements in size of the transistors depending on the state transitions, leading to a very difficult optimization. This circuit works well in a toggle configuration but in a more general configuration glitch can occurs. Therefore, this limits the high-speed operation of this topology [Huan96].

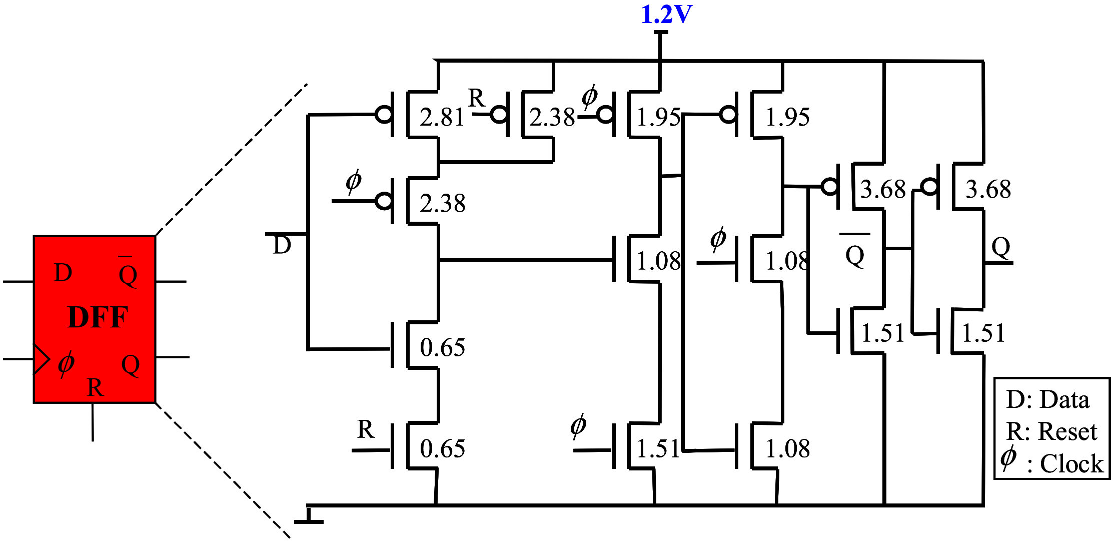

Figure 4.2: Modified Yuan-Svensson DFF

4.3.1.2.2 Glitch-Free Fast DFF

One possible solution to avoid this speed limitation is to place the switch transistors closer to ground and include three additional transistors as shown in Fig. 4.3 [Huan96]. Glitch transitions are reduced and higher-speed operation is possible. The 18-transistor glitch-free Fast Data Flip Flop (FDFF) is shown in Fig. 4.3.

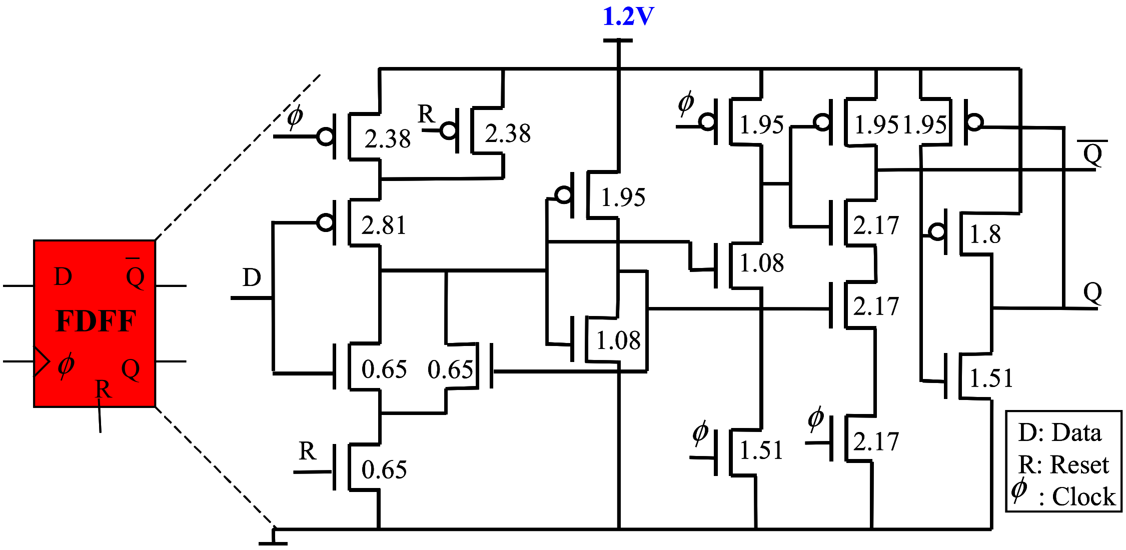
1.2V
D
$\overline{Q}$
FDFF
ϕ
Q
R
D
ϕ
2.38
R
2.38
2.81
1.95
0.65
0.65
1.08
R
0.65
ϕ
1.95
1.95
1.95
1.08
2.17
2.17
1.8
ϕ
1.51
ϕ
2.17
1.51
$\overline{Q}$
Q
D: Data
R: Reset
ϕ : Clock

Figure 4.3: Glitch reduction and consumption gain for the modified FDFF

This implementation is used in the overall transmitter for high-speed purposes (processing of upconverted RF signals).

4.3.1.3 Simulation and Comparison of the two Designed Flip-Flops

Structures in Figs. 4.2-4.3 are simulated using ELDO tool and results about general operation (glitch reduction in the case of the modified DFF) and current consumption are illustrated in Fig. 4.4. Current consumption ratio (CCR) is defined as the ratio between the DC currents of the DFF and the FDFF.

$$CCR = \frac{I_{DC\_DFF}}{I_{DC\_FDFF}} \tag{4.1}$$

Both flip-flops operate at a maximum frequency of 8 GS/s (obtained in a divide-by-2 toggle configuration) and the current consumption ratio between the Yuan-Svensson model and the modified FDFF is about 2 at high frequencies.

The Yuan-Svensson topology is chosen for low-speed purposes in the transmitter such as synchronization of the three-baseband paths at the input of the circuit. The glitch-free fast DFF is employed in high-speed applications such as interpolation of the IQ and envelope signals.

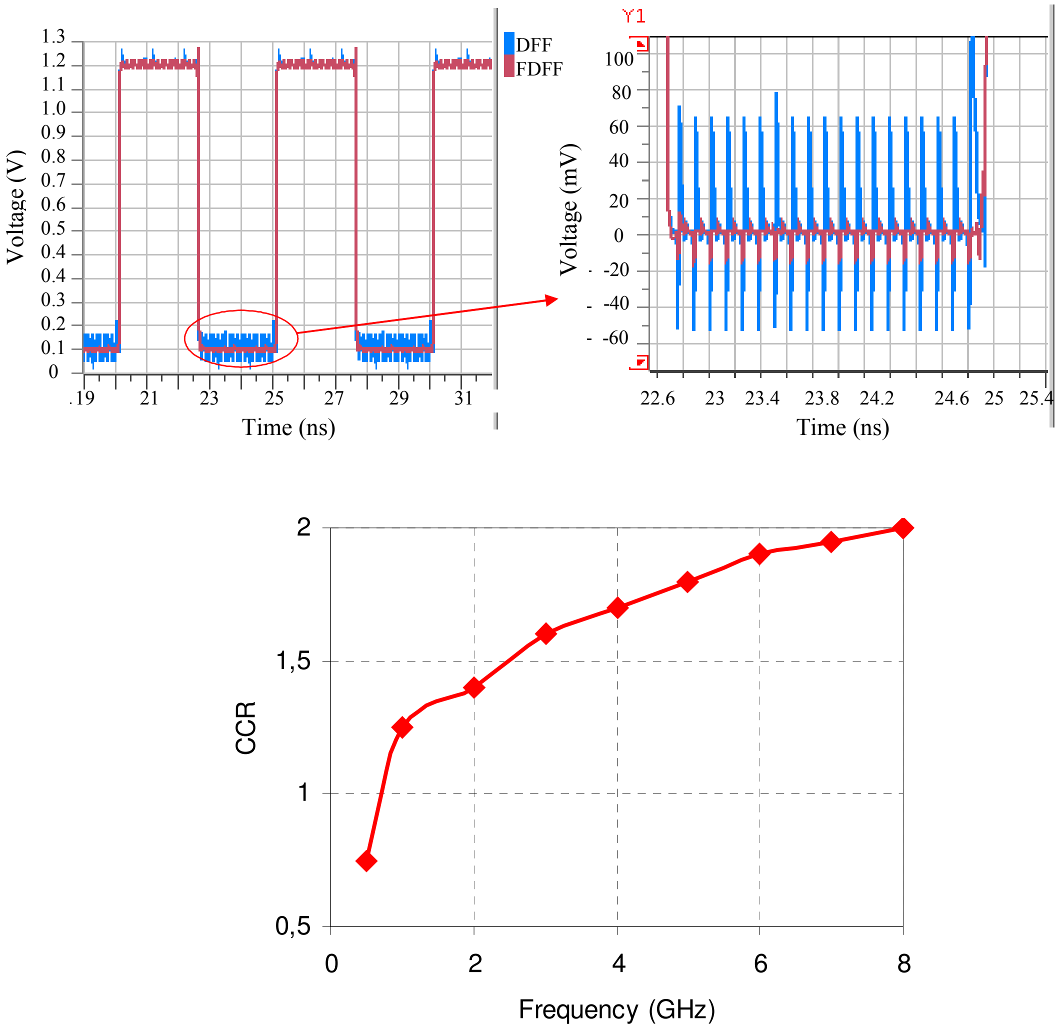

Figure 4.4: DFF vs. FDFF (time domain and current consumption ratio CCR)

4.3.2 Set Reset Flip-Flop Basic Structure

Another common type of flip-flop is the Set Reset asynchronous Flip-Flop (SRFF). Effectively, when one input (S) is pulsed high while the other (R) is being held low then the Q output is forced high. In our application, this flip-flop is used as an asynchronous generator for complementary signals. Basic structure with transistor sizing is shown in Fig. 4.5. This flip-flop is composed of four simple 2-input NAND gates and inverters for signal buffering. In the design of the NAND gate it is important to careful transistor sizing of M1 and M2 (see Fig. 4.5). Critical delay in a NAND gate corresponds to the high to low transition (Td_{HL}), which is related to the conduction of series NMOS transistors. Taking into account the Elmore model [Raba03], the delay of this 2-input NAND gate can be expressed as:

$$Td_{HL}=R1C1+(R1+R2)C2 \tag{4.2}$$

where R1/R2 and C1/C2 are the equivalent resistors and capacitances, respectively, of transistors M1 and M2. The solution adopted in the design of this high-speed gate to reduce the propagation delay upon the expression written in eqn. 4.2 is to size transistor M2 smaller than M1.

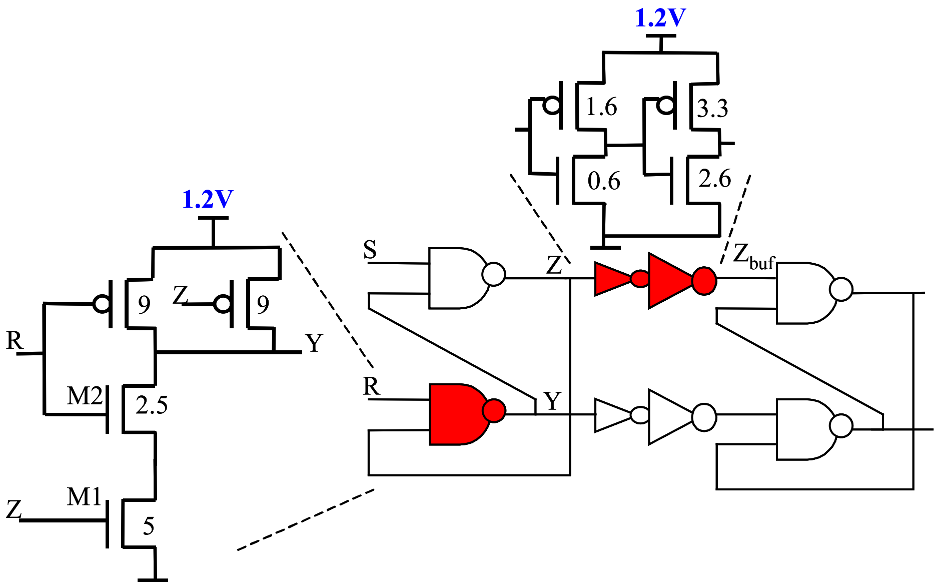

Figure 4.5: Design of the SR flip-flop

4.3.2.1 Use of the SRFF in the Transmitter: Generation of Complementary Signals

Set Reset flip-flop is used to compensate for the delay introduced by the CMOS inverter in the generation of complementary signals even at frequencies of GS/s. Our proposed solution is based on a differential architecture. The generation of complementary signals (phase offset of 180°) is considered. If a simple inverter is used, the data signal will be present at the output after a certain period of time as a consequence of the delay introduced by the inverter (t_d). The inverter delay is determined by the driven current, the non-linear capacitances of the intrinsic transistors and the interconnect capacitances. Such a delay involves limitations to the performance of the generation of complementary signals at high frequencies because this delay is no longer negligible with regard of the signal period. In order to compensate for the delay introduced by the inverter, a SR flip-flop is placed after the inverter as shown in Fig. 4.6.

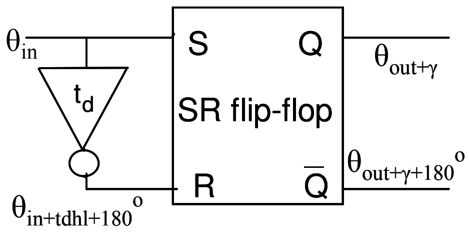

Figure 4.6: Compensation of the delay introduced by an inverter

4.3.2.2 Simulation Results

The SR flip-flop is simulated in ELDO. The simulation results shown below correspond to the complementary signal generation. An ideal inverter (macromodel) with a variable delay is used to generate the complementary signal of a clock frequency at 4 GHz (Vclk in Fig. 4.7).

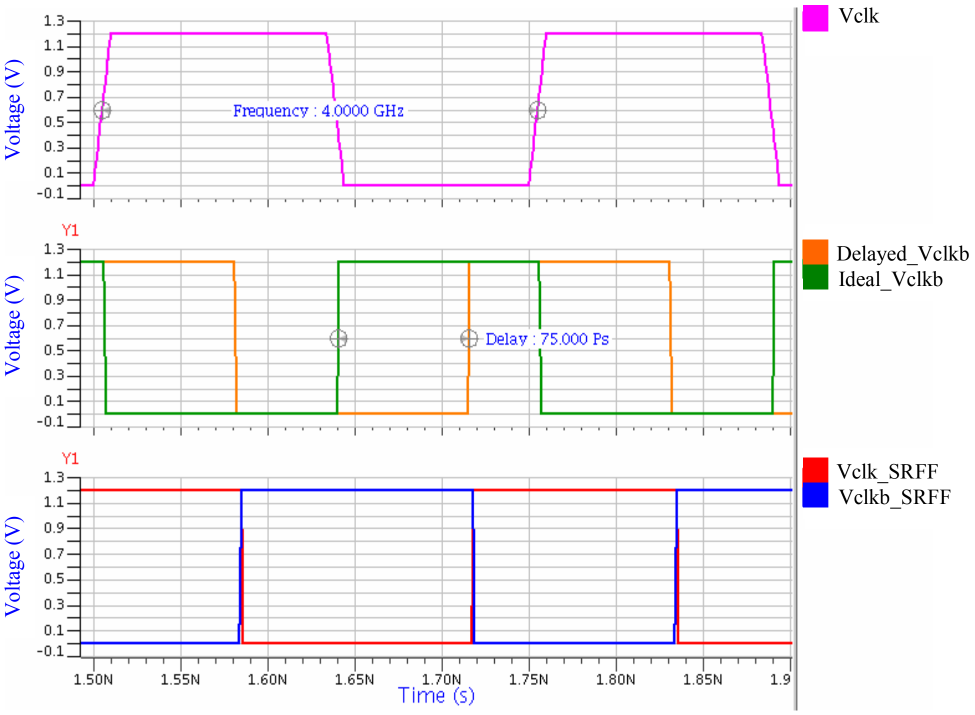

Figure 4.7: Generation of the complementary signals with a compensation delay of 108° (time)

The delay introduced by the inverter is $\phi_{inverter}$. Thus, the phase of the output signal (Delayed_Vclkb) of the inverter can be expressed as:

$$\phi_{Delayed\_Vclkb} = \phi_{Vclk} + 180^{\circ} - \phi_{inverter} \tag{4.3}$$

This signal has a phase error of $\phi_{inverter}$ with regard to the ideal complementary signal (Ideal_Vclkb).

The complementary output signals at the output of the SR flip-flop can be written as:

$$\phi_{Vclk\_SRFF} = \phi_{Vclk} + 180^{\circ} - \phi_{inverter} \tag{4.4}$$

$$\phi_{Vclkb\_SRFF} = \phi_{Vclk} + 180^{\circ} - \phi_{inverter} - 180^{\circ} = \phi_{clk} - \phi_{inverter} \tag{4.5}$$

The delay parameter is set to 0.3.Tclk in this example (108°). The output signal of the inverter (Delayed_Vclkb) is plotted in Fig. 4.7. This signal is delayed by 75 ps (or 108° in Fig. 4.8) related to the ideal signal Ideal_Vclkb.

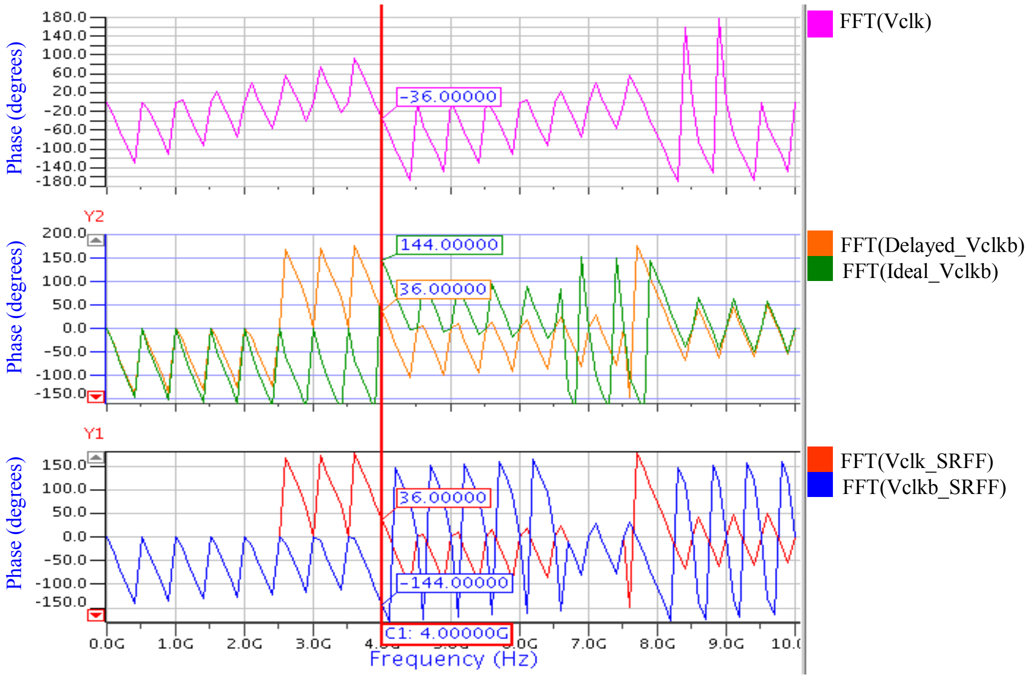

Figure 4.8: Generation of the complementary signals with a compensation delay of 108° (frequency)

When compensation delay method (SR flip-flop) is employed, output signals (Vclk_SRFF and Vclkb_SRFF in Figs. 4.7-4.8) are perfectly complementary (phase shift of 180°).

When no SR flip-flop is used (no delay compensation), the generated output signals are shifted from the ideal 180° from a quantity equal to the propagation delay of the inverter. When the SR flip-flop is used, the delay introduced by the inverter is compensated at 4 GHz, resulting in perfectly complementary signals (phase shifting of 180°) no matter the delay of the inverter is.

4.4 Quadrature Digital Up-Converter

A classical IQ modulator consists of two multipliers (mixers) whose outputs are combined and a signal splitter whose outputs are in quadrature (shifted by 90°). In order to perform the multiplication between the phase signals and the envelope at the rate of the clock frequencies (CLK_{LOI} and CLK_{LOQ}) we replace the digital multipliers operating at GS/s clock frequencies, which result in high power consumption, by a simpler selection of the phase signals or the two's complement (see § 2.6.1).

If both the 1-bit ΣΔ output and the LOs signals have a transition, then the non-inverted phase signal is routed to the output, else, the inverted phase signal is selected (the driving signals are the XOR between the up-sampled ΣΔ output and the LOs signals). The quadrature LOs are digitally generated with an error less than 1° in phase matching to minimize the imperfectly rejected image effect as explained in § 2.1.1.

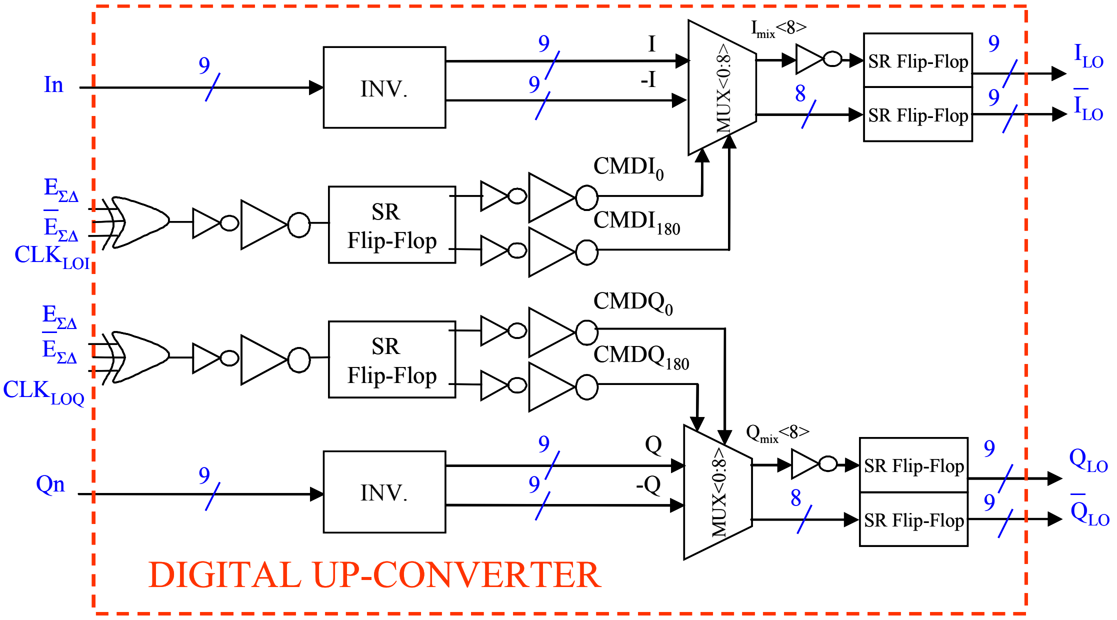
In
9
INV.
9
I
9
-I
I_{mix}<8>
MUX<0:8>
SR Flip-Flop
SR Flip-Flop
8
9
9
I_{LO}
$\overline{I}_{LO}$
$E_{\Sigma\Delta}$
$\overline{E}_{\Sigma\Delta}$
CLK_{LOI}
SR Flip-Flop
$CMDI_0$
$CMDI_{180}$
$E_{\Sigma\Delta}$
$\overline{E}_{\Sigma\Delta}$
CLK_{LOQ}
SR Flip-Flop
$CMDQ_0$
$CMDQ_{180}$
Qn
9
INV.
9
Q
9
-Q
Q_{mix}<8>
MUX<0:8>
SR Flip-Flop
SR Flip-Flop
8
9
9
Q_{LO}
$\overline{Q}_{LO}$
DIGITAL UP-CONVERTER

Figure 4.9: Quadrature Digital Up-Converter

The block diagram of the full-digital IQ modulator is shown in Fig. 4.9. The modulator core is composed essentially of two XOR gates, a set of digital multiplexors (MUX) and a block (called INV. in Fig. 4.9) performing the inversion of the phase signals. SR flip-flop generates the differential signals and inverters buffer the signals. The inverters at the output of the multiplexors converts the two's complement signals into unsigned signals (I_{LO} and Q_{LO}) to drive the analog combiner.

The 3-input XOR gate is designed using transmission-gates and the transistor sizing is shown in Fig. 4.9.

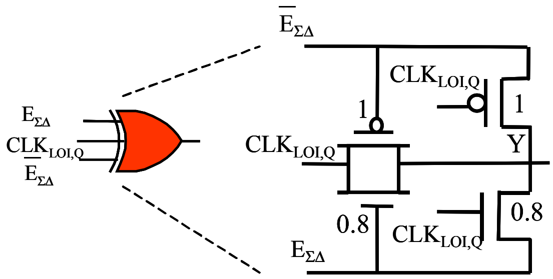
$E_{\Sigma\Delta}$
$CLK_{LOI,Q}$
$\overline{E}_{\Sigma\Delta}$
$\overline{E}_{\Sigma\Delta}$
$\overline{CLK}_{LOI,Q}$
1
1
$CLK_{LOI,Q}$
Y
0.8
0.8
$CLK_{LOI,Q}$
$E_{\Sigma\Delta}$

Figure 4.10: XOR gate used in IQ transmitter

The set of multiplexors are designed as transmission gates and 4 inputs are needed as shown in Fig. 4.11. The inverter and SR flip-flop designs were illustrated in Fig. 4.5.

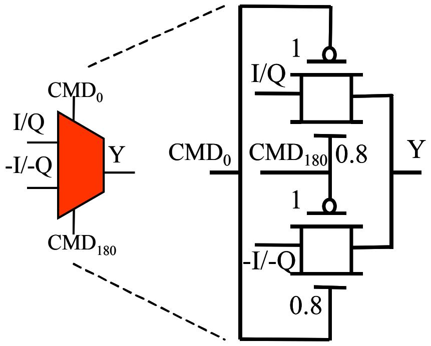
CMD0
I/Q
-I/-Q
Y
CMD180
1
I/Q
CMD0
CMD180
0.8
Y
1
-I/-Q
0.8

Figure 4.11: MUX used in IQ transmitter

The inversion block (INV.) is shown in Fig. 4.12. This circuit is composed of 23 logic gates; five 2-input NOR (NOR2 in the layout), two 3-input NOR (NOR3), two 2-input NAND (NAND2), three 3-input NAND (NAND3), two inverters and 9 XOR. The alternative solution of using a 9-bit carry-skip adder is not only more complex to implement (18 XOR, 21 MUX, about 32 inverters, one NOR2, NOR3 and NOR4) but also occupies more silicon area. Even if the signals to convert (phase signals) are baseband and speed criterion in this application is not critical, reduction of the propagation time delay is desirable. The total converter propagation delay is the contribution of the delays of one NOR gate and one NAND gate, which is intrinsically lower than a conventional 9-bit adder, leading to a simpler architecture and less expensive digital topology.

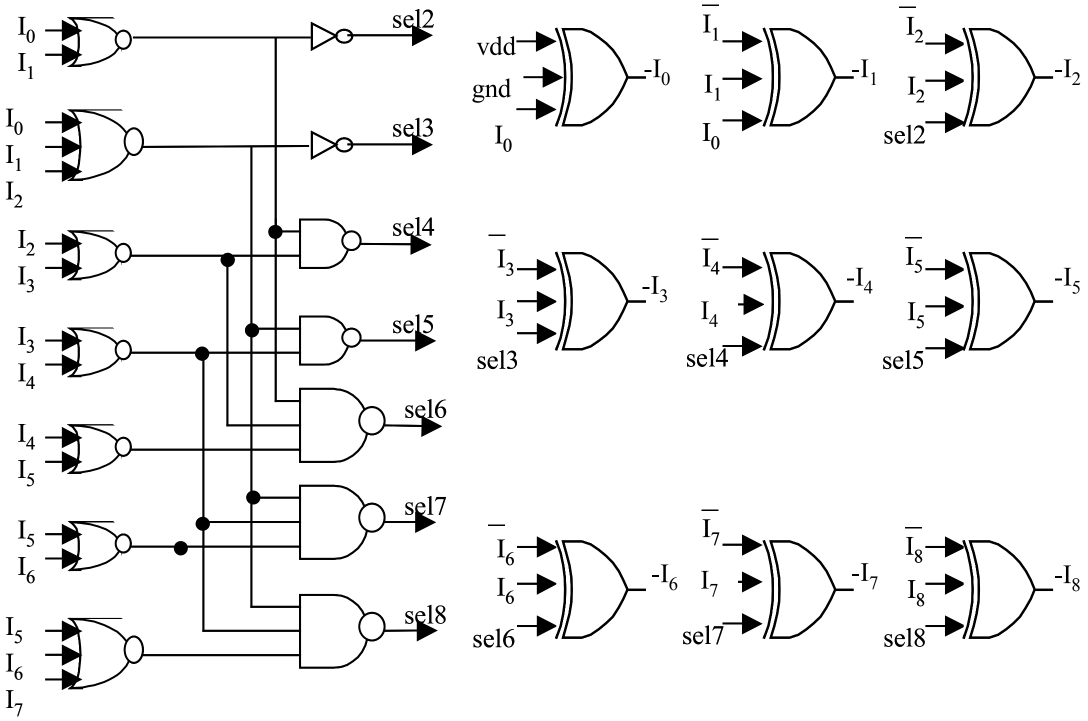
I0
I1
sel2
I0
I1
I2
sel3
I2
I3
sel4
I3
I4
sel5
I4
I5
sel6
I5
I6
sel7
I5
I6
I7
sel8
vdd
gnd
I0
-I0
I1
I1
I0
-I1
I2
I2
sel2
-I2
I3
I3
sel3
-I3
I4
I4
sel4
-I4
I5
I5
sel5
-I5
I6
I6
sel6
-I6
I7
I7
sel7
-I7
I8
I8
sel8
-I8

Figure 4.12: 9-bit Inversion data converter (INV.)

In next figures, the designs of the building blocks of the inverter in Fig. 4.12 are plotted (see Figs. 4.13-4.17). Transistors are sized for high-speed operation (low parasitic capacitors).

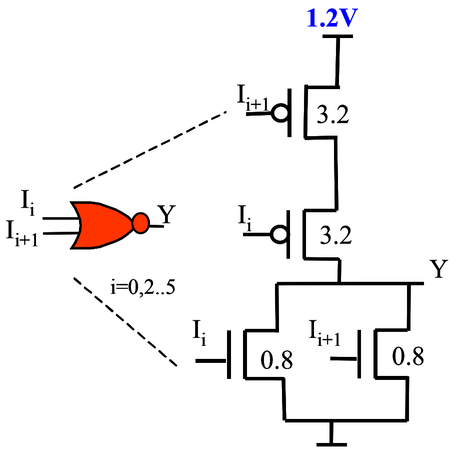
1.2V
I_{i+1}
3.2
I_i
I_{i+1}
Y
I_i
3.2
Y
i=0,2..5
I_i
0.8
I_{i+1}
0.8

Figure 4.13: 2-input NOR in Inverter

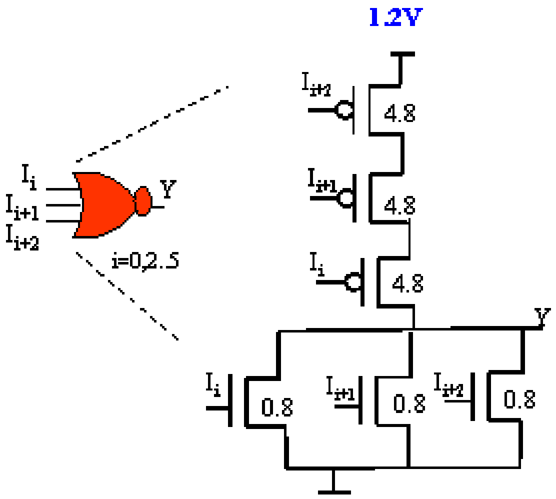
1.2V
I_{i+2}
4.8
I_{i+1}
4.8
I_i
4.8
I_i
I_{i+1}
I_{i+2}
Y
i=0,2..5
Y
I_i
0.8
I_{i+1}
0.8
I_{i+2}
0.8

Figure 4.14: 3-input NOR in Inverter

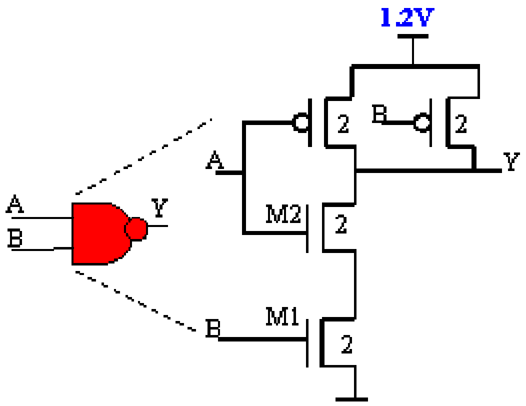
1.2V
2
B
2
A
Y
A
B
Y
M2
2
M1
B
2

Figure 4.15: 2-input NAND in Inverter

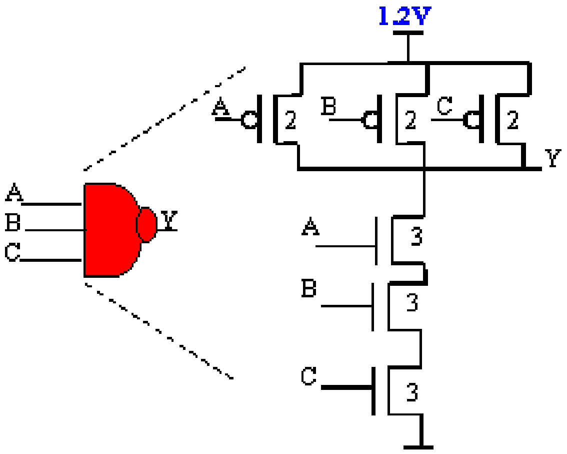

Figure 4.16: 3-input NAND in Inverter

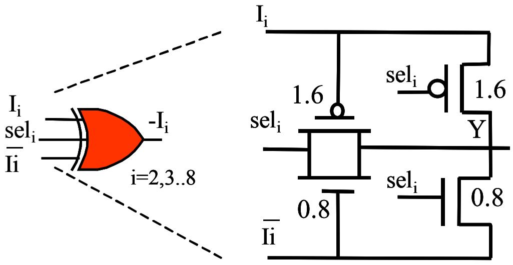

Figure 4.17: XOR in Inverter

4.5 Clock Signals Generation

In this section, the design of the clock circuitry, which generates the different clock signals on the chip, is illustrated in detail.

Firstly, the generation of the ΣΔ coder frequency is considered. As before mentioned and shown in Fig. 2.26, the 1-bit ΣΔ frequency spectrum repeats itself at multiples of $f_{\Sigma\Delta}$. To resolve the problem associated to the upconversion of this digital signal, master frequency must be an integer of the ΣΔ frequency. This frequency is derived from the external master frequency by 4 divide-by-two circuits (only N between 1 and 4 are considered in implementation of eqn. 2.52).

The four DFFs are operated in a toggle configuration. Four NMOS switches are connected between Q outputs and the output. Four bits (S_0, S_1, S_2, S_3) drive these switches. The command bits are generated by 2-input NOR gates (the same gate designed in Fig. 4.13). The inputs of the NOR gates are two control signals (A, B) that are external to the circuit and allows to change dynamically the ΣΔ modulator frequency. The operation of these signals (A and B in Fig. 4.18) is shown in Tab. 4.2:

A	B	S_3	S_2	S_1	S_0	$f_{\Sigma\Delta}$
0	0	1	0	0	0	$f_{master}/2$
0	1	0	1	0	0	$f_{master}/4$
1	0	0	0	1	0	$f_{master}/8$
1	1	0	0	0	1	$f_{master}/16$

Table 4.2: Generation of the 4 control bits

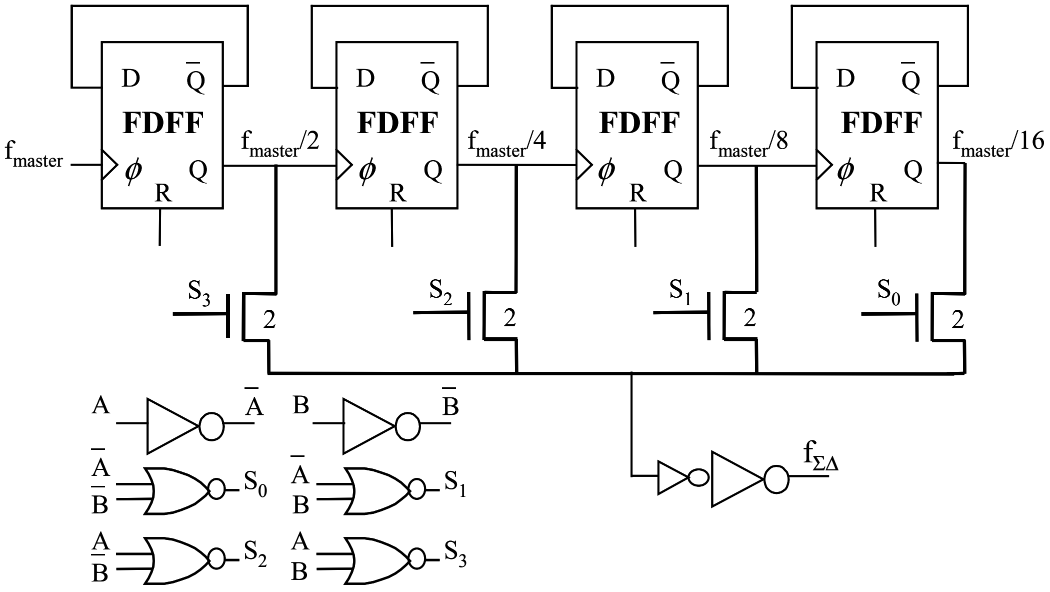
D
Q̄
FDFF
ϕ
Q
R
f_{master}
$f_{master}/2$
$f_{master}/4$
$f_{master}/8$
$f_{master}/16$
S_3
S_2
S_1
S_0
2
A
Ā
B
B̄
S_0
S_1
S_2
S_3
$f_{\Sigma\Delta}$

Figure 4.18: ΣΔ clock generation

Secondly, the quadrature clock generator circuit to generate the quadrature clock signals (CLK_{LOI} and CLK_{LOQ}) from the input master frequency is explained in this paragraph. This generator uses a Set Reset flip-flop to compensate for the propagation delay of the input inverter. The output signals OUT and OUT_{180} are perfectly complementary even at GS/s frequencies. The divide-by-2 DFF circuits at the output generate the quadrature RF signals CLK_{LOI} and CLK_{LOQ} with a phase error less than 1° to be used in the digital mixer. The designed topology is plotted in Fig. 4.19.

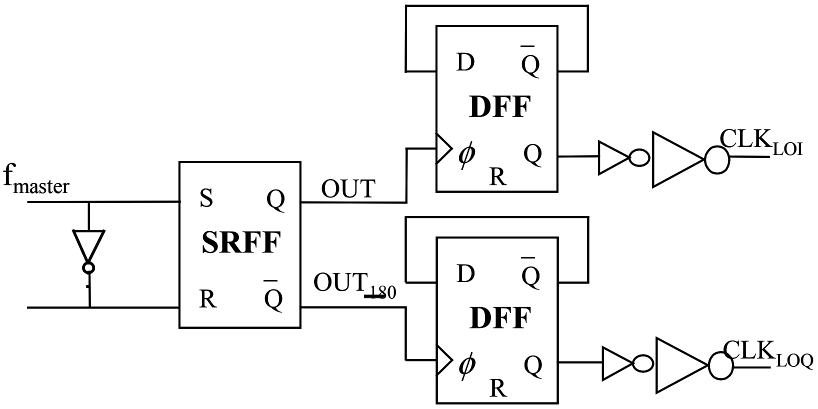
f_{master}
S
Q
SRFF
R
Q̄
OUT
OUT_{180}
D
Q̄
DFF
ϕ
Q
R
CLK_{LOI}
CLK_{LOQ}

Figure 4.19: Quadrature Clock Signals Generator Implementation

4.6 Simulation Results of the TX

To demonstrate the operation of the IQ modulator with the output combiner and the clock signal circuitry, transistor-level simulations of the two topologies are simulated in ELDO. A QAM modulation scheme is chosen to simulate this architecture. Baseband quadrature signals can be written in the time domain as:

$$I(t) = I_{norm}(t)Env(t) = \cos(2\pi f_{ph})\cos(2\pi f_{env}t) \tag{4.6}$$

$$Q(t) = Q_{norm}(t)Env(t) = \sin(2\pi f_{ph})\cos(2\pi f_{env}t) \tag{4.7}$$

where $I_{norm}(t)$ and $Q_{norm}(t)$ are constant-envelope phase signals and $Env(t)$ is considered as the amplitude information. In the frequency domain eqns. 4.6-4.7 can be expressed as:

$$\begin{aligned} I(f) &= \frac{1}{2}\left[\delta(f-f_{ph})+\delta(f+f_{ph})\right]*\frac{1}{2}\left[\delta(f-f_{env})+\delta(f+f_{env})\right]= \\ &= \frac{1}{4}\left[\delta(f-(f_{ph}-f_{env}))+\delta(f+(f_{ph}-f_{env}))\right]+\frac{1}{4}\left[\delta(f-(f_{ph}+f_{env}))+\delta(f+(f_{ph}+f_{env}))\right. \end{aligned} \tag{4.8}$$

$$\begin{aligned} Q(f) &= \frac{1}{2j}\left[\delta(f-f_{ph})-\delta(f+f_{ph})\right]*\frac{1}{2}\left[\delta(f-f_{env})+\delta(f+f_{env})\right]= \\ &= \frac{1}{4j}\left[\delta(f-(f_{ph}-f_{env}))-\delta(f+(f_{ph}-f_{env}))\right]+\frac{1}{4j}\left[\delta(f-(f_{ph}+f_{env}))-\delta(f+(f_{ph}+f_{env}))\right] \end{aligned} \tag{4.9}$$

These signals modulate the amplitude of two quadrature carrier signals as follows:

$$s(t) = I(t)\cos(2\pi f_{RF}t) - Q(t)\sin(2\pi f_{RF}t) \tag{4.10}$$

Using the properties of the Fourier Transform, eqn. 4.10 can be rewritten as:

$$S(f) = \frac{1}{2}\left[I(f-f_{RF})+I(f+f_{RF})\right]-\frac{1}{2j}\left[Q(f-f_{RF})+Q(f+f_{RF})\right] \tag{4.11}$$

Using eqns. 4.8-4.10, eqn. 4.11 yields to:

$$\begin{aligned} S(f) = {} & \frac{1}{4}\left[\delta(f-(f_{RF}+f_{ph}-f_{env}))+\delta(f+(f_{RF}+f_{ph}-f_{env}))\right] \\ & +\frac{1}{4}\left[\delta(f-(f_{RF}+f_{ph}+f_{env}))+\delta(f+(f_{RF}+f_{ph}+f_{env}))\right] \end{aligned} \tag{4.12}$$

Time domain expression of eqn. 4.12 gives:

$$s(t) = \frac{1}{2}\left[\cos\left(2\pi\left(f_{RF} + f_{ph} + f_{env}\right)t\right) + \cos\left(2\pi\left(f_{RF} + f_{ph} - f_{env}\right)t\right)\right] \qquad (4.13)$$

This modulation is similar to a Double-SideBand Supressed Carrier (DSB-SC) transmission in which, frequencies are symmetrically spaced from the carrier frequency. In this case, the carrier frequency is equal to $f_{RF} + f_{ph}$.

The simulation results are shown for a single-tone 2 MHz (f_{ph}) sine-wave phase signals I_{norm} and Q_{norm}, normalized to the 20 MHz (f_{env}) sine-wave envelope, with a clock master frequency of 4 GHz and a LO frequency of 2 GHz.

First of all, signals at the input of the IQ transmitter are generated (see Fig. 4.9). I_{norm} and Q_{norm} phase signals are converted by an ideal 9-bit ADC with a sampling frequency of 100 MHz. These signals drive the 9-bit data inverter (INV.) to generate $-I_{norm}$ and $-Q_{norm}$ with a phase error lower than 1° (see Fig. 4.20).

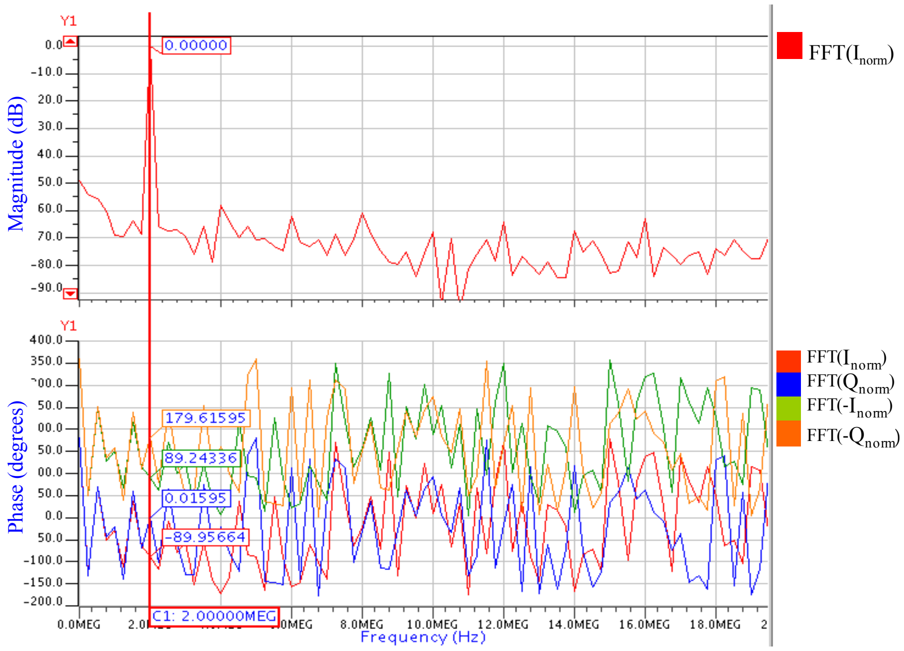

Figure 4.20: FFT (magnitude and phase) of phase signals and theirs complements

Envelope signal is digitized by a 9-bit 100 MHz ADC, coded by a 1-bit ΣΔ modulator operating at a frequency $f_{\Sigma\Delta}$ (500 MHz in this example) and then oversampled by a factor of 4 to a frequency of 2 GHz (Fig. 4.21).

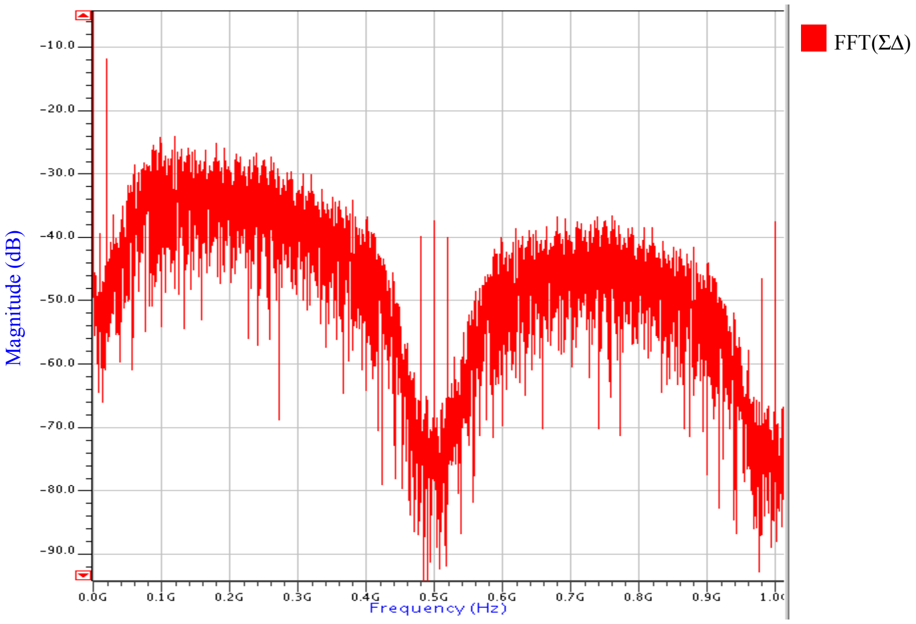

Figure 4.21: FFT (magnitude) of the interpolated 1-bit ΣΔ coded envelope (20 MHz sine-wave)

The frequency of the coder is set as a function of the external A and B switches. In this example, A is set to logic ‘1’ and B to logic ‘0’ (see Tab. 4.2). The circuitry used to generate this frequency has been detailed in Fig. 4.18. The different signals at the output Q of the FDFF are depicted in Fig. 4.22.

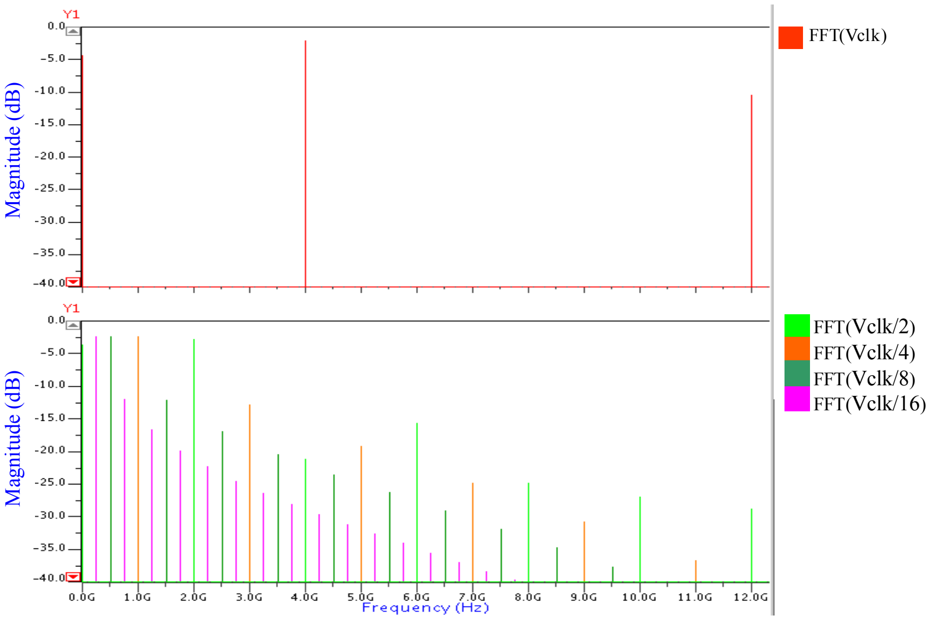

Figure 4.22: Division of the clock signal (factors 2, 4, 8, and 16)

Finally, the generation of the quadrature signals CLK_{LOI} and CLK_{LOQ} is considered. Employing the circuit given in Fig. 4.19, phase error of the generated signals is smaller than 1° even at the maximum considered frequency of 2 GHz (Fig. 4.23). This great phase accuracy results extremely important for the correct high-speed operation of the digital transmitter developed in this research.

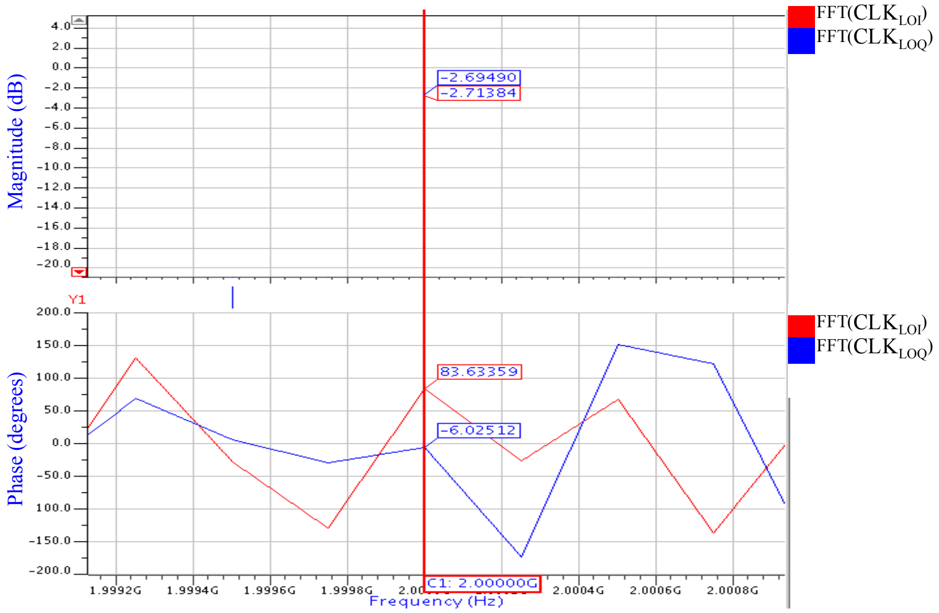

Figure 4.23: FFT of the quadrature signals CLK$_{LOI}$ and CLK$_{LOQ}$

The interpolated 1-bit sigma-delta signal and the LOs signals are mixed in the IQ transmitter, resulting in CMDI$_0$, CMDI$_{180}$, CMDQ$_0$, CMDQ$_{180}$ signals shown in Fig. 4.9. Output spectra of those signals are depicted in Fig. 4.24 after simulation of the topology. The output of this XOR-operation is the result of the product (convolution in frequency domain) of two 1-tone signals. The phase offset between the quadrature signals (CMDI$_0$ and CMDQ$_0$) remains about 90° with an error lower than 1°. The complementary signals are properly generated with the correct 180° phase shift by the inverter in series with the SR flip-flop.

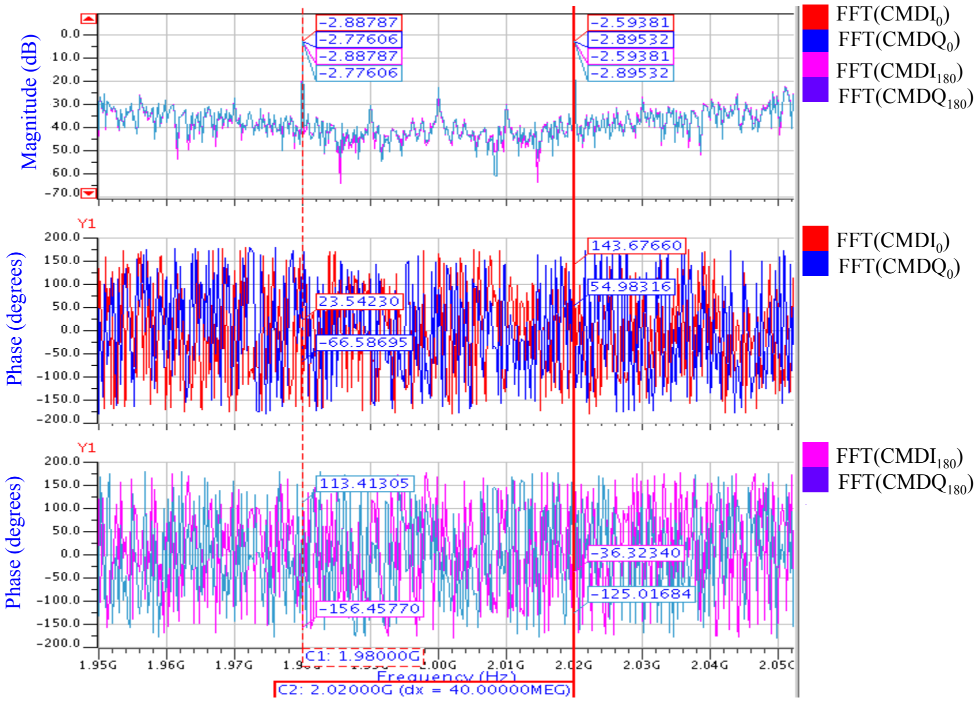

Figure 4.24: FFT of the quadrature signals CMDI$_0$/CMDQ$_0$ and the complementary driving signals

The control signals drive the multiplexors in the IQ mixer. If there is inversion (CMDs signals equal to logic ‘1’ or electric 1.2 V), then the multiplexors output $-I_{norm}$, else, I_{norm} is passed (the same for Q path). This “mixing” operation is clocked by the driving signals, resulting, at the output (I_{LO} and Q_{LO}) in the mixing of the three paths involved in the transmitter (IQ streams, envelope and LO).

I_{LO} and Q_{LO} are double-band signals as shown in Fig. 4.25. The output signal of the transmitter will be the sum of these signals, leading to a single-band signal (suppression of one band if no mismatch is presented in the transmitter). SR flip-flops at the output are responsive of the generation of the complementary signals to drive the differential analog combiner.

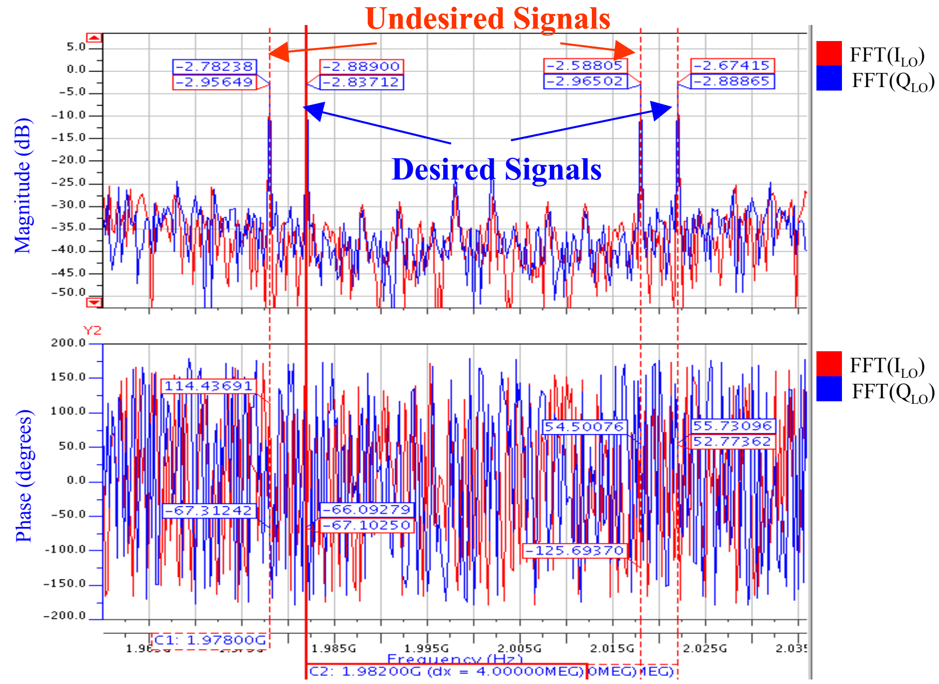

Figure 4.25: FFT of the IQ mixer outputs I_{LO} and Q_{LO}

The output of the analog combiner (Fig. 4.26) contains the desired signal in addition to the out-of-band shaped quantization noise from the 2nd order, 1-bit ΣΔ modulator. In this case, there are no image or LO spurs inside the signal bandwidth. In practice, due to mismatch in layout, spurs signals are not completely removed and appear at the output.

Resistor Capacitors (RC) extracted simulations of the IQ transmitter are shown in Fig. 4.28. The resulting output voltage has a spurious tone at the frequency of 1.98 GHz. The plot shows the 45 dB dynamic gain of the combiner. Reference currents in the DACs are varied from 250 nA to 45 µA. For simplicity, only the extreme values are shown in the graph.

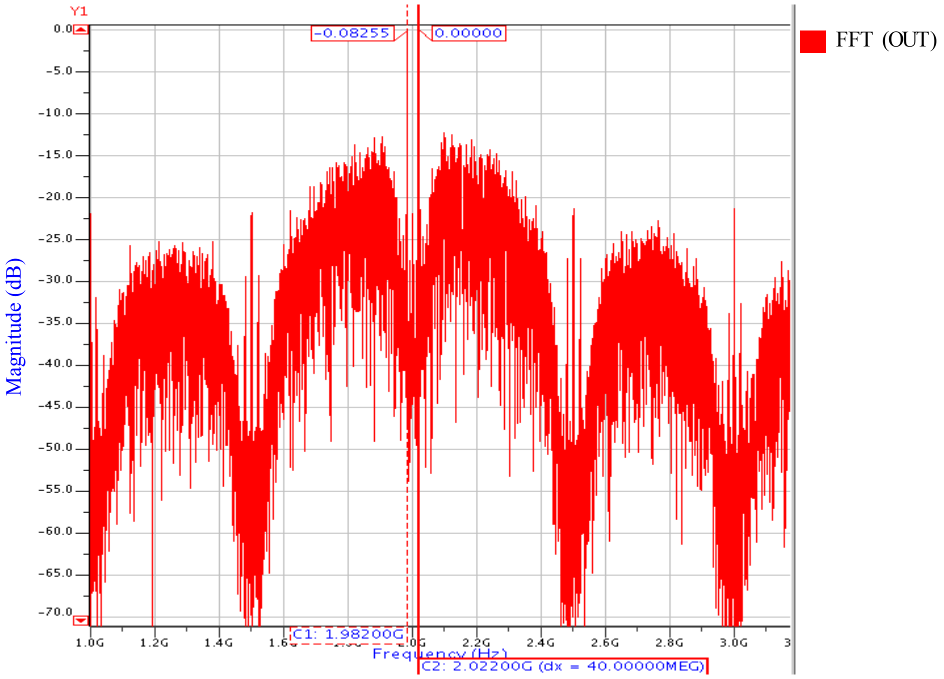

Figure 4.26: Normalized FFT of the transmitter output

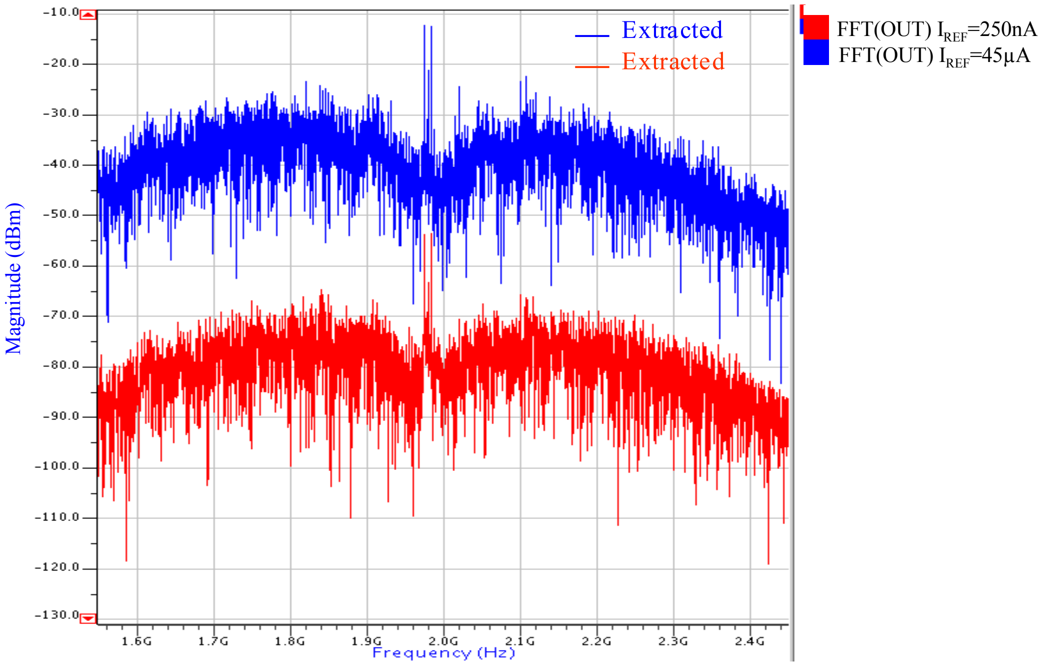

Figure 4.27: Spectra of the single-ended output signals for I_{REF}=250nA and 45µA (Extracted Layout)

4.7 Test Set-Up

The transmitter chip was fabricated in STMicroelectronics’s 0.13 µm BiCMOS process to demonstrate the performance of the proposed transmitter architecture. The chip was mounted in a 48-pin slug down plastic Thin Quad Flat Pack (TQFP) and soldered on the PCB. The PCB is a standard 3-layer FR4 board.

A block diagram of the fabricated chip is shown in Fig. 4.28. Envelope and phase rest patterns signals were generated with Agilent ADS and loaded into two IQ modulation generators AMIQ (Rohde&Schwarz). The AMIQs is programmed to deliver the phase and envelope signals to three external 9-bit analog-to-digital converters (Texas Instruments). These signals were digitized and clocked at 100 MHz, which is the maximum clock frequency of the AMIQs. The ADC output buffer is powered by 3.3 V supply and the ADCs output 3 V rail-to-tail straight binary data.

Combinational logic in the transmitter uses 1.2 V power supply. Thus, there is a need to adapt the 3 V output level to the 1.2 V level in the circuit. A two-resistor voltage divider is included to interface the ADC output and the input of the chip.

The input bit stream paths time constants need to be short to insure sharp-edged digital signals. The values of the resistors are set to 1 kΩ and 1.5kΩ to reduce the value of the RC product. Twenty seven transmission lines, containing the normalized I and Q signals, together with the Envelope, are designed for a characteristic impedance of about 100 Ω and route the three signals to the input circuit.

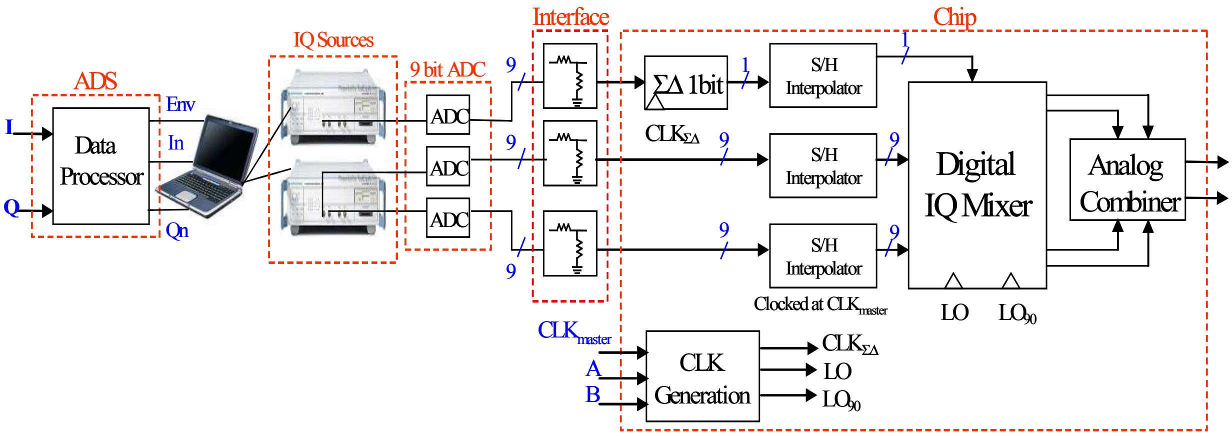
ADS
I
Q
Data Processor
Env
In
Qn
IQ Sources
9 bit ADC
ADC
ADC
ADC
9
9
9
Interface
Chip
ΣΔ 1bit
1
1
CLK$_{\Sigma\Delta}$
9
9
9
9
S/H Interpolator
S/H Interpolator
S/H Interpolator
Clocked at CLK$_{master}$
Digital IQ Mixer
Analog Combiner
LO
LO$_{90}$
CLK$_{master}$
A
B
CLK Generation
CLK$_{\Sigma\Delta}$
LO
LO$_{90}$

Figure 4.28: Block diagram of the fabricated chip and Test Set-Up

This circuit includes the ΣΔ coder, interpolation filters, signal buffers, digital up-converter and analog combiner. The layout of this proposed transmitter and the TQFP chip package used are shown in Fig. 4.29.

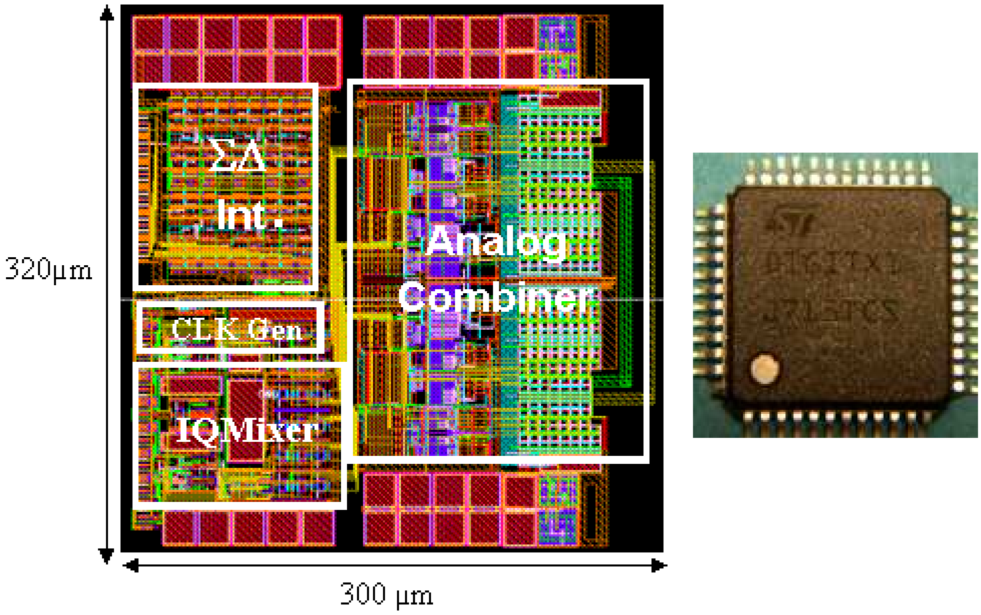
ΣΔ
Int.
CLK Gen
IQMixer
Analog
Combiner
320µm
300 µm

Figure 4.29: Layout of the proposed transmitter and chip package TQFP

Attention is paid in the layout of the PCB to separate the low frequency digital circuitry data bit stream $I/Q/E$ and power supplies VDD_{buffer}, VDD, $VPOL_I$, $VPOL_Q$, $VREF_I$ and $VREF_Q$ from the RF signals $Vout$, $\overline{Vout}$ and CLK_{master} to minimize coupling. Different layers are provided to the digital and RF circuits (see Figs. 4.30-4.31).

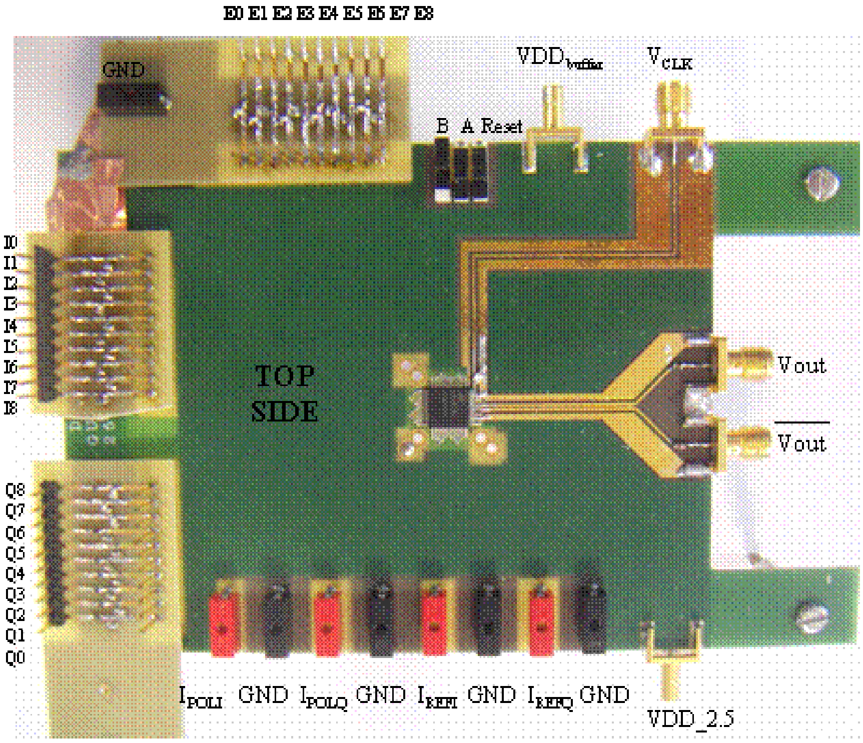
E0 E1 E2 E3 E4 E5 E6 E7 E8
GND
VDD_buffer
V_CLK
B A Reset
I0
I1
I2
I3
I4
I5
I6
I7
I8
TOP SIDE
Vout
$\overline{Vout}$
Q8
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0
I_POLI GND I_POLQ GND I_REFI GND I_REFQ GND
VDD_2.5

Figure 4.30: Layout of the PCB with RF signals (TOP SIDE)

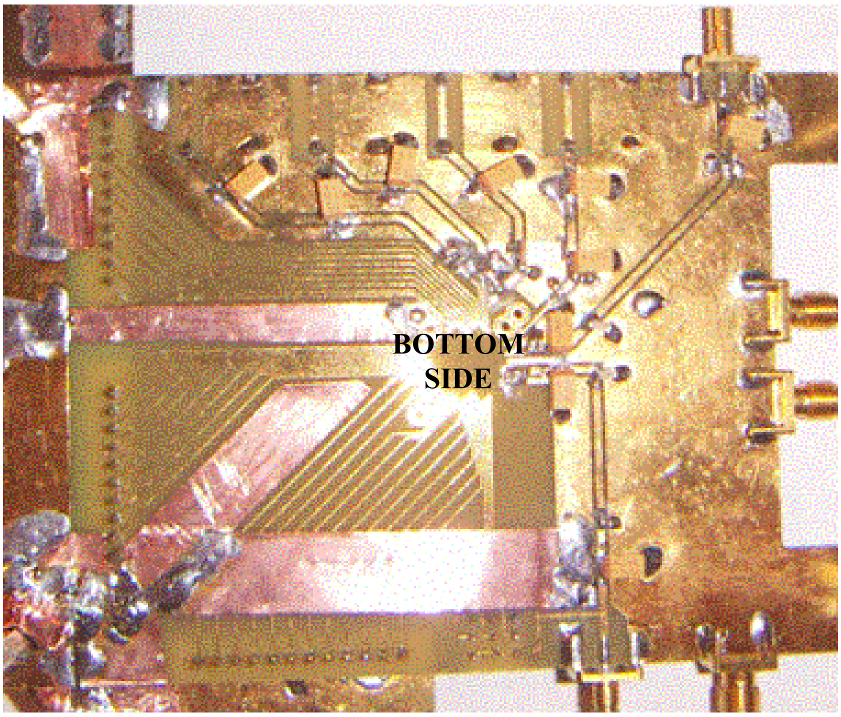

Figure 4.31: Layout of the PCB with RF signals (BOTTOM SIDE)

4.8 Simulation vs. Measurements Results (Complete TX)

Output spectra plots for two 1 MHz sine-wave phase input signals and a 3 MHz sine-wave envelope input signal are shown in following figures. All the figures correspond to the differential output power signal. They show the spectrum for two-tone separated by twice the envelope frequency (6 MHz).

Figs. 4.32-4.35 show the output spectra at the maximum differential output power reached at a maximum total current of 45 μA for both DACs in the output combiner.

$$I_{REF1} = I_{REF2} = \frac{I_{REF}}{2} = \frac{45\mu A}{2} = 22.5\mu A \qquad (4.14)$$

Two different values of carrier frequencies are considered: 100MHz and 900 MHz. Simulation results are also plotted to compare with the test chip results.

For simulation time reasons, we show only the lower and higher RF frequencies in the system. At the maximum output power value, measured levels of images are less than -15 dBc. However, simulation of the extracted layout of the whole transmitter at low frequency (100 MHz) gives image levels of –22 dBc.

Amplitude and phase mismatches between IQ signals and an imprecise 90° LO phase shift within the IQ modulator together with layout mismatch could cause this finite image rejection. This unwanted signals could be critical in the case of complex output signals.

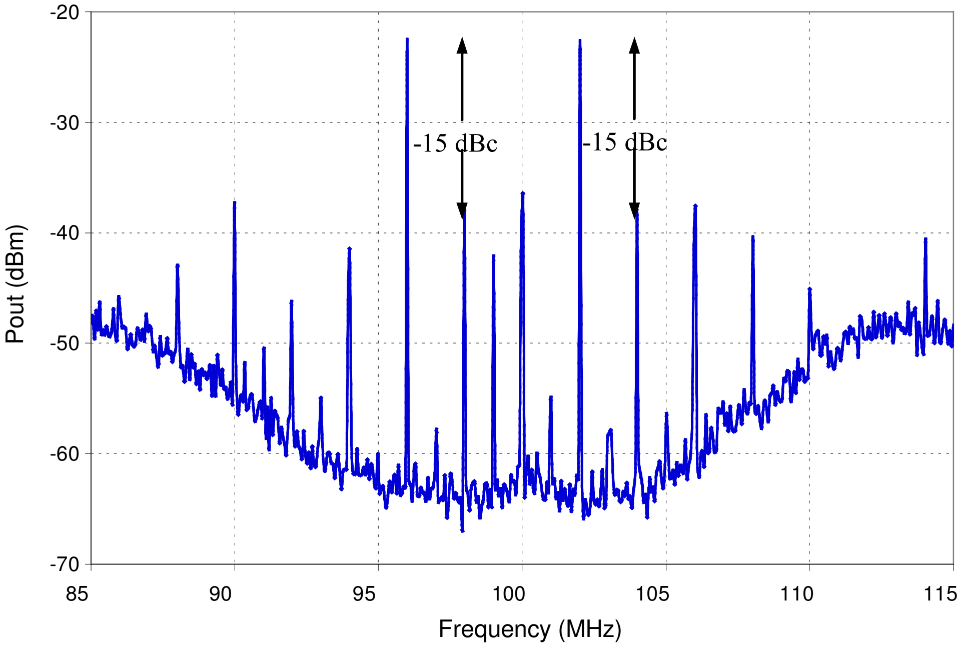

Figure 4.32: Test Chip: Maximum Single-Ended Output Power @100 MHz

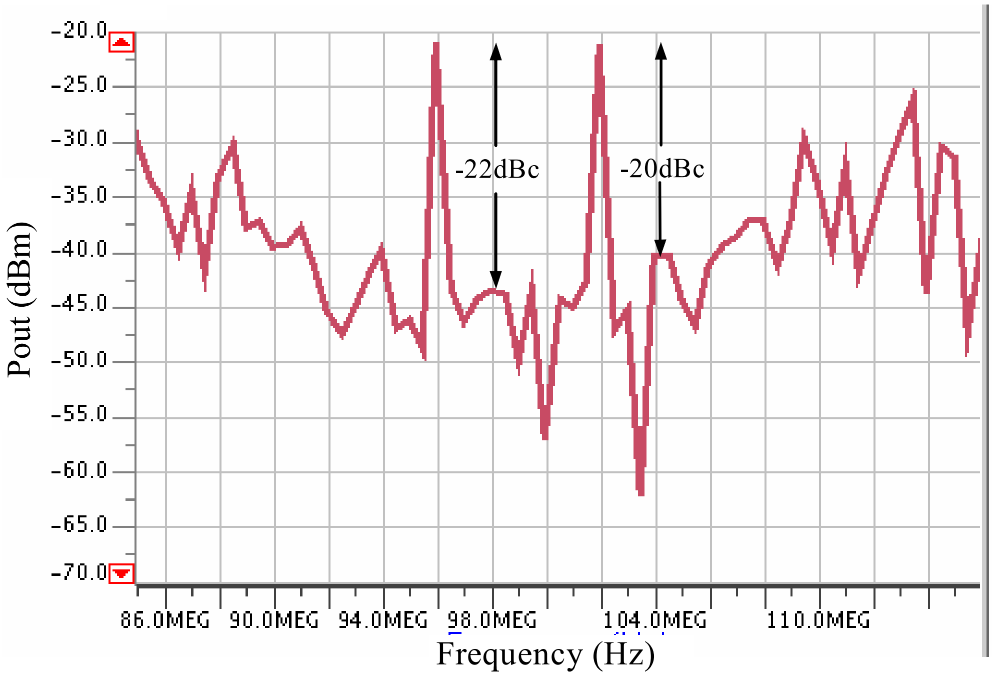

Figure 4.33: Maximum Single-Ended Output Power @100 MHz (Extracted Layout Simulation)

Maximum output power dependence with frequency is evidenced from results shown in Figs 4.32.4.35. Output power provided by the chip is higher at low RF frequencies.

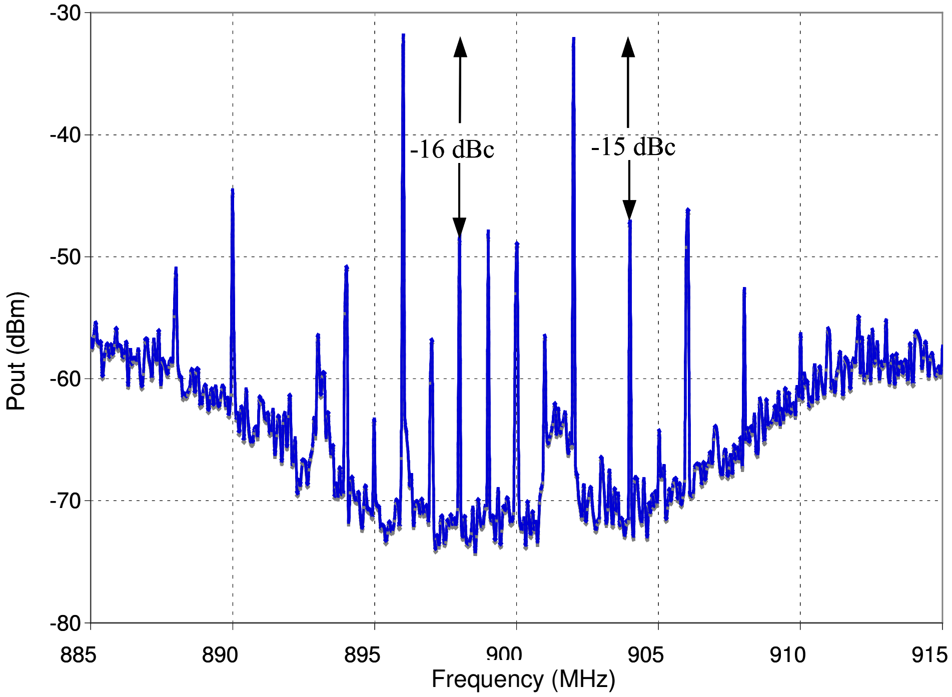

Figure 4.34: Test Chip: Maximum Single-Ended Output Power @900 MHz

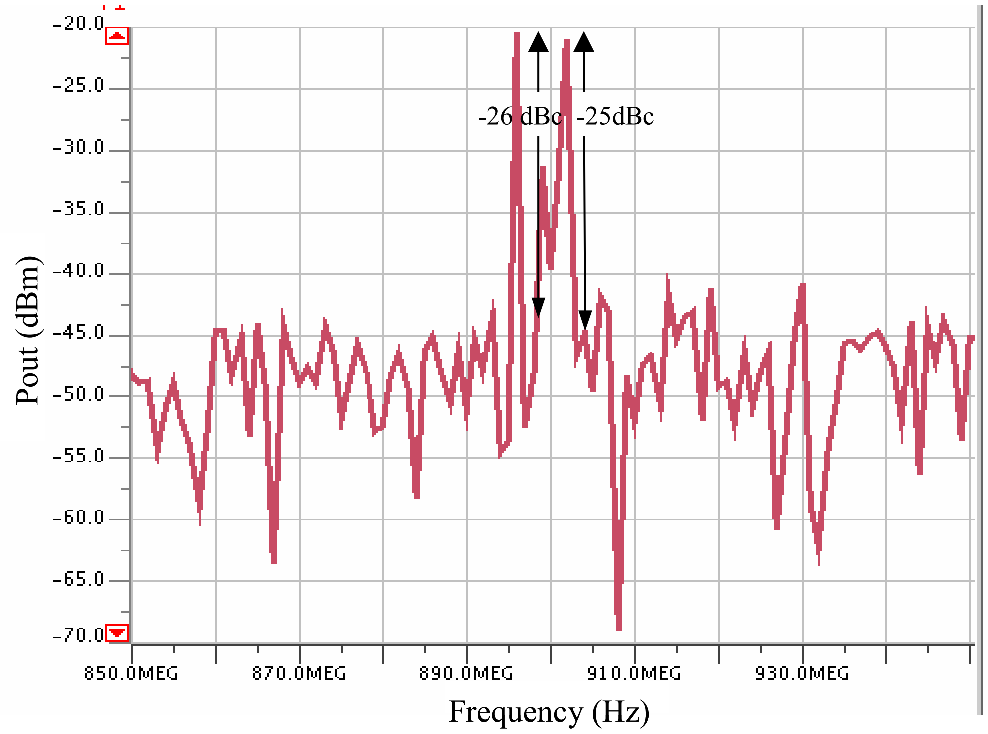

Figure 4.35: Maximum Single-Ended Output Power @900 MHz (Extracted Layout Simulation)

The single-ended output power of each signal tone decreases from -21 dBm (see Figs. 4.32-4.33) at a carrier frequency of 100 MHz to -31 dBm at maximum LO frequency of 900 MHz as shown in Fig. 4.34. This provides evidence of a saturation effect at high frequencies. This limitation (which is only remarked in measurements) is attributed to layout imperfections, especially in the high-frequency output combiner design.

It is interesting to compare these power values with those shown in chapter 3 with the use of a sine-wave generator and a single DAC. In Fig. 3.42, a maximum single-ended output power value of –6 dBm was shown for a single tone signal. Thus, it implies that for a two-tone signal a single-ended output power of –9dBm should be found for each peak. In our transmitter simulations, each peak power is more than 10 dB lower, obtaining –21 dBm instead. It means that the noise power is about ten times higher than the signal power (SNR≈ -10 dB). This is the reason why we obtain lower power values than for the single DAC case in chapter 3.

Minimum output power in the transmitter for each peak is about -55 dBm. This represents about 34 dB control gain for sampling frequencies lower than 800 MHz and 24 dB for sampling frequencies greater than 800 MHz.

From now to on, measurements will be done at a total current value of 20 µA to overcome the output power saturation with frequency at maximum current. The corresponding single-ended output power is about 3 dB lower than the maximum output power depicted in Figs. 4.32-4.35. Measurements results for LO frequencies of 400 MHz and the maximum of 900 MHz are shown in Figs. 4.36-4.37. Control current in the analog combiner is 20µA for different sampling frequencies in the ΣΔ coder. Interpolation ratios (Div. in Figs. 4.36-4.37) in the interpolation filter have values 2, 4, 8, 16.

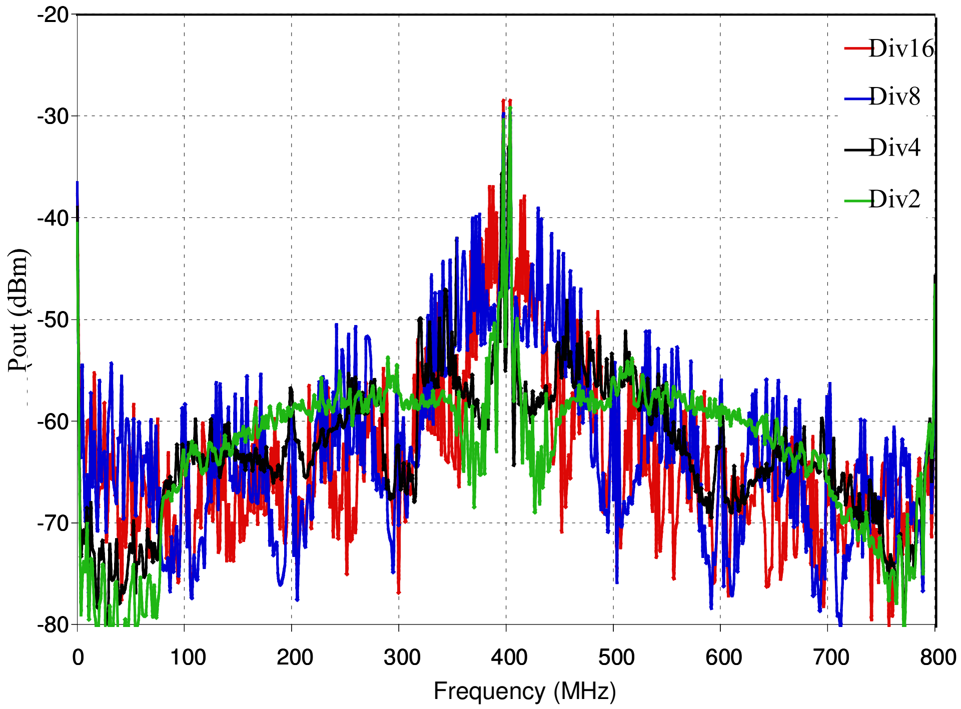

Figure 4.36: Test Chip: Single-Ended Output Power for I_{REF}=20 µA @400 MHz

Due to the relatively low sampling frequency (800 MHz in Fig. 4.36), transmitter performances are better in terms of out-of-band noise for low interpolation ratios as for ratios larger than 8 the ΣΔ coder is forced to operate at its minimum demonstrated frequency of about 40 MHz (boundary frequency determined by the dynamic flip-flops operation). Sinc roll-off is visible in Figs. 4.36-4.37 with the introduction of spectral zeros at multiples of the sampling frequency of the 1-bit ΣΔ modulator.

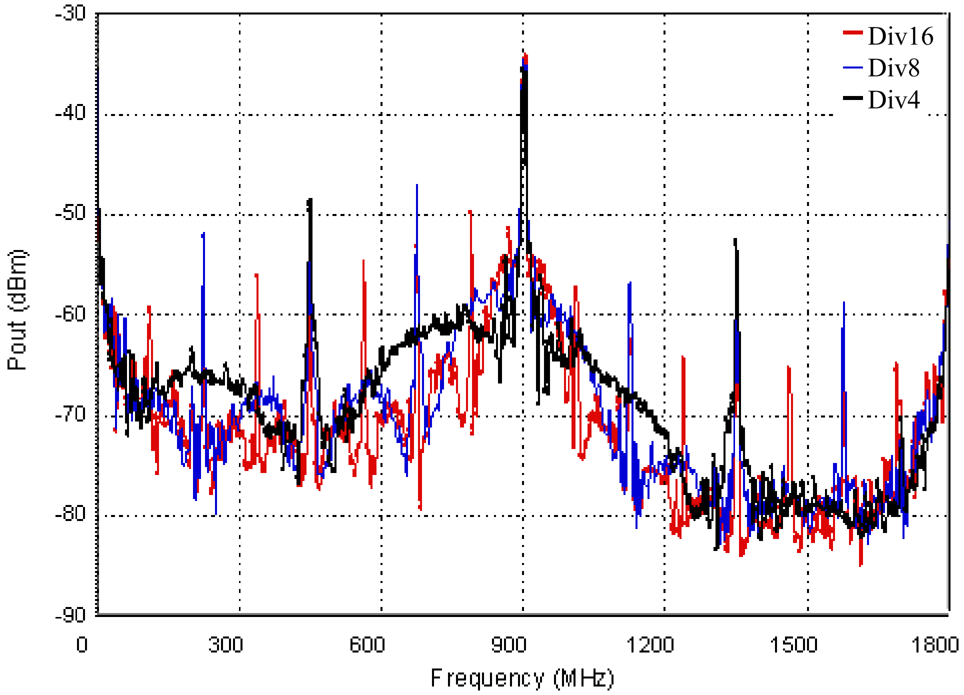

Figure 4.37: Test Chip: Output Power for I_{REF}=20 μA @900 MHz

Transmitter performances when handling with wide-band signals (envelope frequency is 20 MHz) are shown in Figs. 4.38-4.39. 20 MHz sine-wave envelope signal is ΣΔ-coded and phase signals are 2 MHz sine waves. The three signals are sampled at the input of the circuit at a rate of 100 MHz.

The output spectrum represents a two-tone signal with a bandwidth of 40 MHz. Results are shown for a DAC control current of 20 μA. Image levels are -12 dBc (see Fig. 4.37). This represents 3 dB of degradation with regard to results shown in Fig. 4.34. This could be due to the larger distortion caused by the low oversampling ratio in the conversion of the envelope signal by the input 9-bit ADC which values 2.5.

As shown in Figs. 4.37-4.38 for a sampling frequency of 1.8 GHz and a LO frequency of 900 MHz, the results demonstrate how the sampling frequency of the ΣΔ coder should be decreased when the transmitter handles with high RF frequencies to attenuate the out-of-band quantization noise generated by the envelope modulator. However, this causes the degradation of the in-band

SNR.

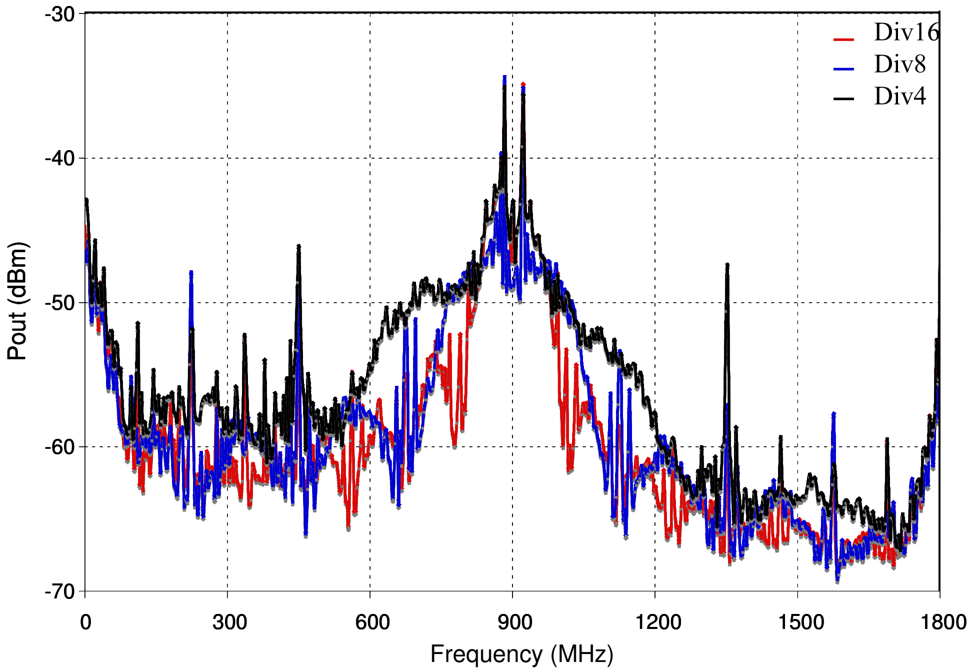

Figure 4.38: Test Chip: Two-tones (40 MHz) Output Power for I_{REF}=20 μA @900 MHz (Wide-Band test)

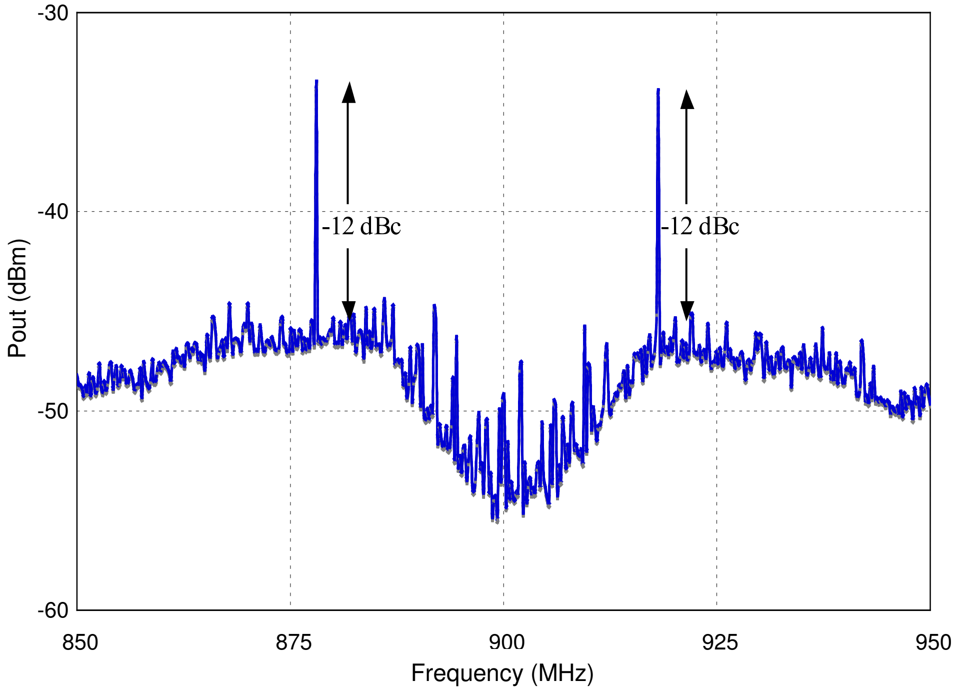

Figure 4.39: Test Chip: In-band Spectrum for I_{REF}=20 μA @900 MHz (Wide-Band test)

Hence, we think that in a definitive transmitter implementation, the minimum sampling frequency in the ΣΔ modulator could be software-defined to meet the mask requirements for a given standard, using adaptively this technique to introduce spectral zeroes to attenuate a portion of the total quantization noise. Finally, the dissipated power of the whole transmitter is illustrated in Fig. 4.40. The total dissipated powers both in the CMOS logic (1.2 V supply) at the maximum sampling frequency of 1.8 GHz and in the two DACs (2.5 V supply) are taken into account.

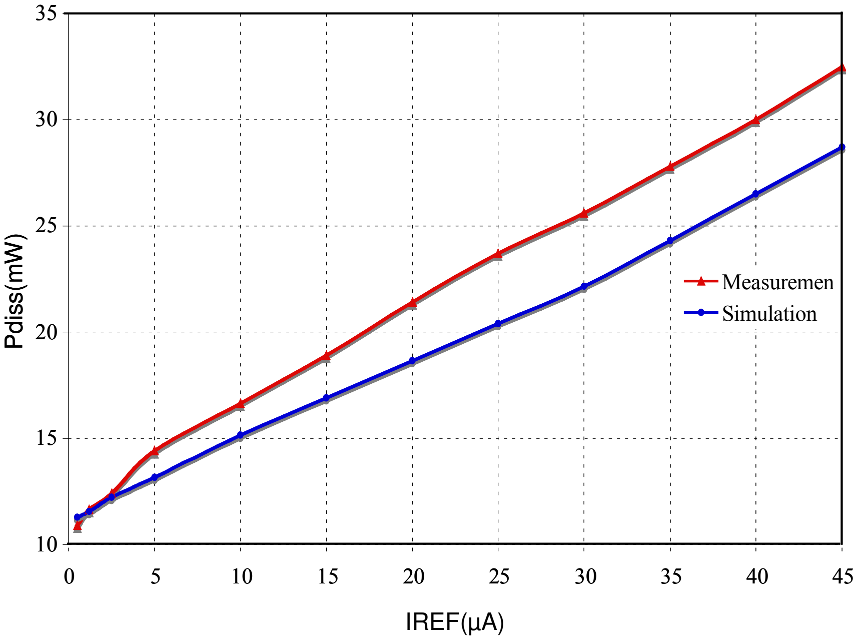

Figure 4.40: Dissipated power of the transmitter @1.8GHz

As we can see in Fig. 4.40 at low control currents in the DACs, total dissipation power is mainly determined by the CMOS logic part of the transmitter. If we consider results depicted in Fig. 3.40 in chapter 3, the contribution due only to the 1.2 V logic circuitry is about 10 mW. The maximum dissipated power obtained in the chip measurement of the multistandard transmitter is less than 35 mW at the maximum test-demonstrated sampling frequency of 1.8 GS/s. The maximum dissipated power of the analog combiner is about 25 mW, which is similar to the value obtained for the stand-alone DAC measured in chapter 3 (see Fig. 3.41). In Tab. 4.3, we summarize the main characteristics of the built prototype in 0.13 μm BiCMOS process.

(** Power of each output peak is only considered*)

f_{max}	**$Pout_{max}$ (differential)***	**Power Control**	**IRR**	**Power Dissipation**	**Power Supply**	**Techno.**	**Die Size**
1.8GS/s	-28dBm	23dB	<-15dBc	<35mW	1.2&2.5V	BiCMOS	300x320μm^2

Table 4.3: Features of the fabricated TX

4.9 Conclusion

In this chapter, the design and test of the studied multistandard, multiband transmitter have been detailed. This architecture employs phase and envelope separation similar to the EER technique. The separation is performed by ADS simulation tool. One main difference relate to the EER-type systems is that IQ phase signals are normalized by the envelope. The three signals are quantized by three 9-bit ADCs driving our built prototype. The representation of the three bit streams in the circuit is in two’s complement. IQ and envelope signals are synchronized and upsampled in baseband by DFFs. Both low (Yuan-Svensson structure) and high-speed (glitch-free) flip-flops are designed depending on the application. For high-speed purposes the flip-flop is glitch-free reducing the power consumption by a factor of two relating to the low frequency flip-flop.

A 2nd order 1-bit ΣΔ modulator codes the envelope. The noise introduced by the noise shaping coder is filtered at high frequencies (out-of-band noise) by a high-speed flip-flop (Zero-Order Hold Interpolator).

A novel full digital, low power and wideband quadrature mixer performs recombination of the three signals and frequency upconversion. This mixer takes advantage of the 1-bit. Effectively, as both LOs and envelope signals are represented by two-level signals, the product of these signals (XOR function) leads to a two-level signal, which can be used as command signal in the multiplexors (see Fig. 4.10). Phase signals or theirs complements that are generated by a simple Inversion Block (see Fig. 4.13) are passed through this multiplexor at the rate of driving signals. This allows to implement a high frequency, wideband mixer instead of a more complex three-input modulator. This IQ mixer is very simple to implementate as it uses only CMOS logic gates.

The generation of the quadrature clock signals in the mixer is obtained by carefully design of two paths to avoid mismatch to assure an error less than 1° (only demonstrated in simulation) and the use of SR flip-flops to generate correctly the complementary signal prior to the divide-by-two circuit.

The topology is fully digital and the quadrature and differential RF signals are converted into the analog domain and added in a new proposed analog combiner (see Fig. 4.1). This combiner performs a power control of 45 dB to meet CDMA standard requirements in simulation. However, measurement results in § 4.8 give evidence of a saturation effect at high control current in the analog combiner. The maximum output power is reduced with regard to the continuous wave case in chapter 3. It is due to mismatches caused by the layout, the quantization noise of the three external 12-bit ADCs at the input of the circuit and the used of a ΣΔ coder, which has inherently low coding efficiency due to the large amount of quantization noise. The total transmitted power has two contributions: the desired signal and the quantization noise.

For sampling frequencies in the transmitter lower than 800 MHz, dynamic range is about 35 dB dropping to 25 dB at higher sampling frequencies, which is much lower than the targeted 45 dB. This could be due to layout imperfections or underestimation of the parasitic effects in both the circuit and the board. Moreover, the RF signal driven to the analog combiner is not only composed of the desired stimulus but also of a large amount of quantization noise provided by the envelope coder. In fact, this noise power is ten times higher than the stimulus signal power and thus is also amplified in the analog combiner. This amount of noise power produces a signal power loss of about 10 dB, which involves an inefficient system. In next section, we present an enhanced system to relax this noise constraint enabling to reduce the noise power before amplification in the analog combiner.

When three continuous wave signals are fed into the circuit, the transmitter can be seen as a single-band converter with two tones in the desired band spaced of twice the envelope signal and one undesired band. In measurements, image signals are attenuated 15 dB (instead of 25 dB obtained in simulation), which represents an unacceptable reject level in modern communications. Some improvements should be done in the layout because this imperfection has been only remarked in measurement. Even if the use of SR flip-flops assure a correct quadrature generation of LOs signals, both phase signals must be designed as symmetrical as possible to achieve an acceptable rejection level.

One important result is that when high operating frequencies are used in the transmitter (sampling frequencies higher than 800 MHz), it is interesting to reduce the sampling frequency of the ΣΔ coder by a factor, which is a power of two and upsampling the 1-bit output signal. The measurement results were shown in Fig. 4.36-4.38. The sampling frequency in the ΣΔ modulator must be high enough to meet the in-band requirements of a given standard. The upsampling filter (Zero Order Hold) introduces a sinc roll-off and attenuates the image signals (out-of-band noise), which is one of the major problems of the ΣΔ-type systems. The optimized interpolation factor for sampling frequencies greater than 800 MHz is found to be 8 and represents the best trade-off between complexity and in-band requirements.

To prove the wideband performance of the proposed transmitter, a 20 MHz sine wave signal was employed as envelope signal. The transmitter can be considered as a single-band mixer. At the output there are the desired band which consists in a two-tone signals with each tone separated of 40 MHz from the other. The image rejection in this case is measured to be about -12 dBc, which is 3dB lower than for a narrower case (3 MHz envelope instead of 20 MHz). This degradation of the image level rejection could be explained as follows; for the wideband case, the maximum sampling frequency of both the external ADCs and AMIQ modulator is limited to 100 MHz. The 20 MHz envelope signal is sampled at this quite low rate and the Oversampling Ration is not high enough (2.5) so the quantization noise is increased related to the narrow band case, degrading the overall transmitter performances.

As far as consumption concerns, we must separate two contributions to the total consumption. Power dissipated in the 1.2 V power supply and the power dissipated in the 2.5 V power supply. At the maximum single-ended output power (-31 dBm for each of two tones) and the maximum sampling frequency of 1.8 GHz (carrier frequency of 900 MHz), measurement results indicate that the power dissipated in the 1.2 V part of the circuit is about 10 mW and the total power dissipation is about 35 mW, which is coherent with the measurements of the stand-alone DAC in chapter 3 (about 25 mW at peak output power). It is important to remark that the ΣΔ coder operated at a frequency which is 8 times lower than the maximum sampling frequency of 1.8 GS/s. Obviously, if the interpolation factor was reduced, the contribution due to the power dissipation would be much higher.

This RF differential and upconverted signal can be easily amplified by a switched-mode PA in an efficient way because it presents constant-envelope and the PA can work in the saturation zone.

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[Huan96] Q. Huang, R. Rogenmoser, “Speed optimization of edge-triggered CMOS circuits for gigahertz single-phase clocks“, *IEEE Journal of Solid-State Circuits*, vol. 31, no. 3, p. 456-465, Mars 1996.

[Raba03] J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Designing combinational logic gates in CMOS"*, Digital integrated circuits, University. of Berkeley, Prentice Hall*, 2003.

[Yuan89] J. Yuan and C. Svensson, "High speed CMOS circuit technique", *IEEE J. Solid State Circuits*, vol. 24, no. 1, pp. 62-70, February 1989.

Conclusion

To overcome the trade-off existing in actual communication systems in the design of both high efficient and linear multimode transmitters, we proposed in this research a new wideband transmitter able to convert any RF signal with non-constant envelope into a constant envelope signal enabling the use of a nonlinear and efficient power amplifier. The design and silicon integration in a 0.13 µm STMicroelectronics BiCMOS process of a low cost single chip digital radio transmitter with a dynamic range of about 45 dB (to perform power control of CDMA-type systems) and able to support all the communication standards and applications that require linear and efficient amplification has been detailed.

In the developed architecture, phase and envelope are separated (EER-type system) in three paths and processed separately. The low frequency envelope is coded by a 2^{nd} order noise-shaping 1-bit coder (Sigma-Delta modulator) and phase signals are normalized by the envelope signal. The three signals are quantized by three 9-bit ADCs driving our built prototype. Quantization noise of the signal generated by the ΣΔ modulator is attenuated by a Sample-and-Hold interpolator placed at the output of this coder to introduce notch at multiples of the sampling frequency. The representation of the three bit streams in the circuit is in two's complement. IQ and envelope signals are synchronized and oversampled in baseband by DFFs.

Phase and Envelope signals are recombined and upconverted directly to radio frequencies using a novel full-digital, wideband quadrature modulator. This mixer takes advantage of the 1-bit ΣΔ output. As both LOs and envelope signals are represented by two-level signals, the product of these signals (XOR function) leads to a two-level signal, which can be used as command signal in the multiplexors. Phase signals or theirs complements that are generated by a simple Inversion Block are passed through this multiplexor at the rate of driving signals. This enables to implement a high frequency, wideband mixer instead of a more complex three-input modulator. This IQ mixer is very simple to implementate as it uses only CMOS logic gates. The generation of the quadrature clock signals in the mixer is obtained by carefully design of two paths to avoid mismatch to assure an error less than 1° (only demonstrated in simulation) and the use of SR flip-flops to generate correctly the complementary signal prior to the divide-by-two circuit

The combination at the output of this modulator is performed by two asynchronous 9-bit Digital-to-Analog Converters (DAC) instead of extremely difficult to design high-speed 10-bit adder. The DAC is designed in 0.13 µm BiCMOS technology from STMicroelectronics. The converter is divided into two full binary-weighted DACs of 4 and 5 bits. This topology enables to reduce the size ratios between the most and least significant bits related to a classic 9-bit binary-weighted structure (16 instead of 256). To test the speed and the gain control of the stand-alone DAC over 45 dB, we have designed on the chip a 1.4 GHz 9-bit CMOS ROM-less direct digital frequency synthesizer (DDFS). Logic gates have been used instead of area consuming ROM (sine look-up table) to convert phase word to sine wave amplitude directly. Logic functions are implemented using standard CMOS. For implementing multiplexors and XOR-gates, transmission gates are preferred because of the simplicity. Measurement results show good correlation with post-layout simulations. They show a gain control of 45 dB and an operating maximum frequency of 1.4 GHz. This frequency limitation comes from the DDFS chip. This chip can synthesize sine waves at the before mentioned maximum clock frequency so we are not able to provide measured results at higher frequencies. Over the output power range the DAC shows a SFDR>25 dB. This chip dissipates less than 25 mW for a measured differential output power of -3 dBm (R_L=50 Ω). DDFS dissipates about 3.5 mW at the maximum frequency of 1.4 GHz. The DAC circuit occupies an area of 160x160 μm^2 and 160x220 μm^2 if the DDFS chip is considered.

Concerning the measurements of the full transmitter (refer to § 4.8), very promising results were obtained. When three continuous wave signals are fed into the global circuit, the transmitter can be seen as a single-band converter with two tones in the desired band spaced of twice the envelope signal and one undesired band. In measurements, image signals are attenuated 15 dB (instead of 25 dB obtained in simulation), which represents an unacceptable reject level in modern communications. The image rejection in the case of a wideband envelope signal is measured to be about -12 dBc, which is 3 dB lower than for a narrower case (3 MHz envelope instead of 20 MHz). This degradation of the image level rejection could be explained as in the wideband case, the maximum sampling frequency of both the external ADCs and AMIQ modulator is limited to 100 MHz. The 20 MHz envelope signal is sampled at this quite low rate and the Oversampling Ratio (OR) is not high enough (2.5) so the quantization noise is increased related to the narrow band case, degrading the overall transmitter performances. Some improvements should be done in the layout because this imperfection has been only remarked in measurement. Even if the use of SR flip-flops assure a correct quadrature generation of LOs signals both phase signals must be designed as symmetrical as possible to achieve an acceptable rejection level. For sampling frequencies in the transmitter lower than 800 MHz, dynamic range is about 35 dB dropping to 25 dB at higher sampling frequencies, which is much lower than the targeted 45 dB. This could be due to layout imperfections or underestimation of the parasitic effects in both the circuit and the board. Moreover, the signal driven to the analog combiner is not only composed of the stimulus signal but also it contains a large amount of noise power. Actually, noise power is about ten times higher than the stimulus signal power and thus the amplified stimulus power is reduced by 10 dB with regard to a noise-less input signal, resulting in a less efficient system.

When high operating frequencies are used in the transmitter (sampling frequencies higher than 800 MHz), it is interesting to reduce the sampling frequency of the ΣΔ coder by a factor, which is a power of two and upsampling the 1-bit output signal. The sampling frequency in the ΣΔ modulator must be high enough to meet the in-band requirements of a given standard. The upsampling filter (Zero Order Hold) introduces a sinc roll-off and attenuates the image signals (out-of-band noise), which is one of the major problems of the ΣΔ-type systems. The optimized interpolation factor for sampling frequencies greater than 800 MHz is found to be 8 and represents the best trade-off between complexity and in-band requirements.

As far as consumption is concerned, we must separate two contributions to the total consumption. Power dissipated in the 1.2 V power supply and the power dissipated in the 2.5 V power supply. At the maximum single-ended output power (-31 dBm for each of two tones) and the maximum sampling frequency of 1.8 GHz (carrier frequency of 900 MHz), measurement results indicate that the power dissipated in the 1.2 V part of the circuit is about 10 mW and the total power dissipation is about 35 mW. It is important to note that the ΣΔ coder is operated at a frequency 8 times lower than the maximum sampling frequency of 1.8 GS/s. When the interpolation factor is reduced, the contribution due to the power dissipation becomes much higher.

This architecture enables flexible and software-defined transmitter. Sampling frequency in the ΣΔ coder can be varied to adapt to different communications standards in terms of in-band and out-of-band noise requirements and variable LO frequencies can be used. Moreover, the transmitter can adapt dynamically the output power to the power amplifier depending of the required transmitted power at the output of the PA.

The transmitter has demonstrated its potential for use as a universal transmitter for applications targeting any frequency band and modulation schema up to 2 GHz (in simulation) or 900 MHz (in measurements) and occupies a die area of 300x320 μm^2. The generated differential signal can be easily amplified by a switched-mode Power Amplifier (PA) in an efficient way because it presents constant-envelope and the PA can work in the saturation zone, which represents its optimal operation point.

Future Directions

One area of research is to push the dynamic range performance to be 45 dB. One can improve the layout of the circuit and the PCB to avoid the saturation of the DACs at high control currents. The transmitter performances are determined by the path mismatches. Thus, it is evident that a more carefully layout would improve the overall transmitter performances and would allow correcting these mismatches.

Another main area of research is to reduce the quantization noise as much as possible. As it was shown in § 4.8 SNR of the resulting amplified signal is about –10 dB, which shows that the noise power is ten times higher than the stimulus power. Our architecture depends strongly on the output bandpass filter at the output of the power amplifier and the 1-bit ΣΔ modulator. The filter has to be very frequency selective to meet the noise requirements of the different communications standards and has non-negligible insertion losses. The major advantage of the use of the ΣΔ coder is that the signal that drives the power amplifier is constant-envelope, so. It is amplified in an efficient way by a switched-mode PA. The other advantage of the use of this coder is that it simplifies the recombination operation and the product between the three signals becomes a phase selection and thus is not limited in frequency. However, the 1-bit ΣΔ coder adds a large amount of quantization noise to the transmitted signal so the coding efficiency of the system is very low (loss of 10 dB with regard to a noise-less RF signal). The coding efficiency is an important figure of merit, which represents the input signal portion contained in the output pulse of the envelope modulator [Choi07]. It can be defined as:

$$\eta_{Mod} = \frac{P_s}{\Delta_a^2} \tag{F.1}$$

with P_s being the power of the non-coded signal and expressed as:

$$P_s = \int_{-fb/2}^{f_b/2} \Phi_p(f)\, df \tag{F.2}$$

where Δ_a^2 is the power of the two-level pulse train of amplitude Δ_a.

$\Phi_p(f)$ is the power spectral density of the pulse train and the baseband signal is centered at zero with bandwidth f_b.

To compute the overall transmitter efficiency, three efficiencies must be considered: envelope modulator coding efficiency (η_{Mod}), PA (η_{PA}) and bandpass filter efficiency (η_{BPF}).

$$\eta_{Overall\_System} = \eta_{Mod}.\eta_{PA}.\eta_{BPF} \tag{F.3}$$

The improvement in the global efficiency can be performed by increasing only either the transmitter or bandpass filter efficiency because the PA efficiency is already at its maximum due to the use of a switched-mode PA. The use of a very efficient PA is minimized by the losses in the output filter and the drop of efficiency in the 1-bit ΣΔ-type transmitter as the PA amplifies not only the desired signal but also the quantization noise. It would be interesting to study the impact on the overall transmitter efficiency if the constant-envelope signal is firstly filtered before feeding the PA (Fig. 4.41). Obviously, it will not be longer a constant-envelope and the PA has to work in back-off degrading its efficiency (see Fig. 1.10). A trade-off must be found between the bandwidth of the bandpass filter and the maximum tolerated efficiency drop in the PA so as parameter $\eta_{Overall\_System}$ gets higher. Even if PA efficiency is lower because in this case the signal to be amplified has non-constant envelope, the PA has to amplify less noise power than in the precedent case and also the coding efficiency of the transmitter is higher because this pre-filtering can be seen as a multi-bit quantizer instead of a 1-bit ΣΔ coder. Moreover, frequency requirements and complexity of the output bandpass filter are relaxed improving its performances and reducing the insertion losses.

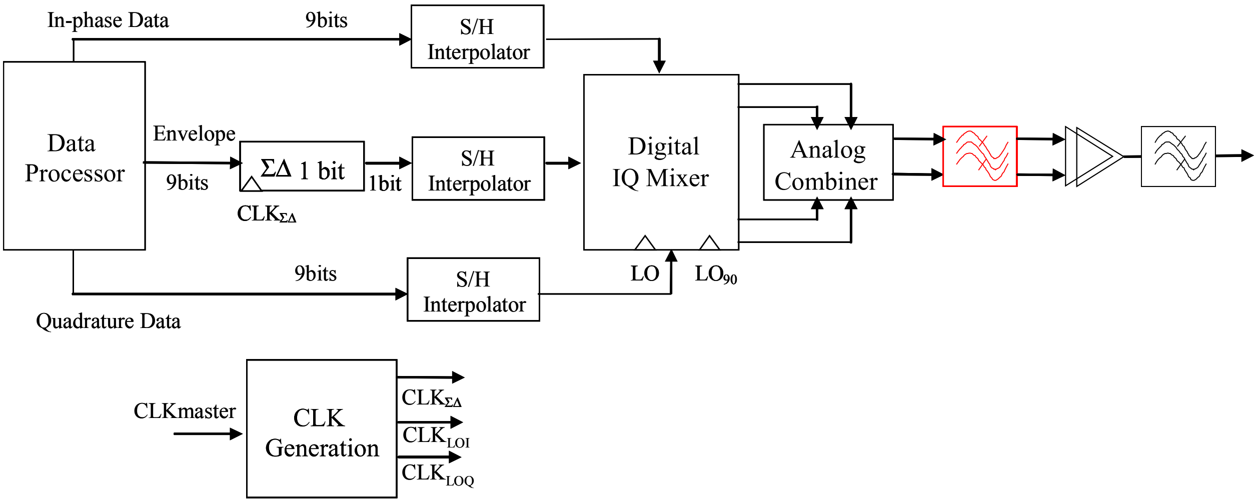
In-phase Data
9bits
S/H Interpolator
Data Processor
Envelope
9bits
ΣΔ 1 bit
1bit
CLKΣΔ
S/H Interpolator
Digital IQ Mixer
Analog Combiner
9bits
S/H Interpolator
LO
LO90
Quadrature Data
CLKmaster
CLK Generation
CLKΣΔ
CLKLOI
CLKLOQ

Figure F.1: Proposed solution with pre-filtering

This solution is worth using when PAPR of the resulting filtered signal at the input of the PA is much lower than the corresponding PAPR of the signal at the input of the circuit. For low PAPR signals, technique depicted in Fig. F.1 is similar to amplify directly this signal by conventional homodyne architecture.

[Choi07] J. Choi, J. Yim, J. Yang, J. Kim, J. Cha, D. Kang, D. Kim, B. Kim, " A ΣΔ-Digitized polar transmitter", *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no.12, December 2007.

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Appendix A

A.1 Types of Implementation

This section gives an introduction to the most important existing static logic styles. At every point of time (except during the switching transients) each gate output is connected to either the power supply or ground via a low-resistive path. The outputs of the gates being at all time the value of the Boolean function implemented by the circuit. The type of implementation chosen represents a trade-off between size of circuit, speed and consumption. The size of the circuit depends on the number of the transistor used in implementation and theirs size. Propagation delay is determined by the transistors size and the number of series transistors. Finally, consumption is divided into a static consumption (negligible) and dynamic consumption, which dominates. This dynamic power dissipation is due to the switching activity and the node capacitances (gate, diffusion and wire capacitances). The proper choice of one or another technique is influenced by the desired circuit performances. Three main types of implementation of static combinational logic can be considered: standard CMOS, pseudo-NMOS and pass-transistor logic [Zimm97].

A.1.1 Standard CMOS

Standard CMOS logic (Fig. A.2) is composed of two dual networks (NMOS and PMOS) performing an inverse function.

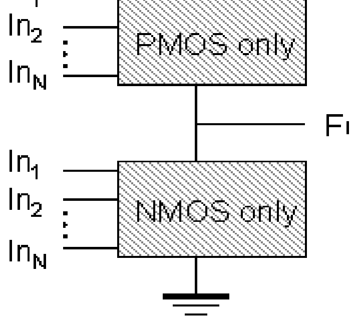

Figure A.2: Standard CMOS logic

A.1.2 Pseudo-NMOS

Another technique called pseudo-NMOS is derived from the previous standard CMOS in order to reduce power dissipation and global size. The PMOS network in Fig. A.2 is replaced by a single PMOS load in Fig. A.3. To implement the same logic function, N+1 transistors are used instead of 2N of the previous technique.

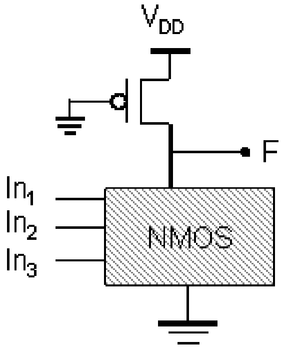

Figure A.3: Pseudo-NMOS logic

The main drawback of this technique is that due to the conflict between the on-PMOS and the active NMOS network for a high input, the output is different from ground causing static power dissipation. The value of the output will be function of the on resistances of the PMOS load and the NMOS network. Improved loads increasing the complexity are proposed in [Raba03].

A.1.3 Pass-Transistor Logic

Pass-transistor logic uses N transistors and has ideally no static consumption (Fig. A.4).

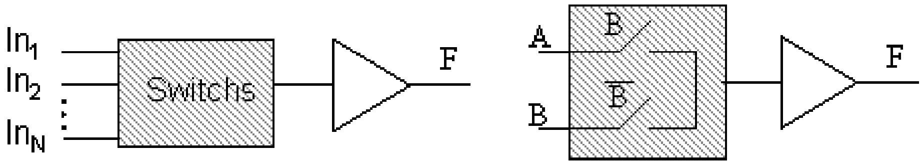

Figure A.4: Pass-transistor logic

Input signals are not only applied to the gate as in standard CMOS but also to the source/drain of the transistors. NMOS and PMOS networks are not dual.

This logic reduces the size and consumption of the circuit. However, output levels have a shift equal to the threshold voltage (V_t) causing a static consumption to appear. To improve this, signal buffering is needed to recover the signal level at the output, which increases the power dissipation of the system. Furthermore, implementing logic functions is not evident as in standard CMOS.

One possible alternative to the problem of the shift V_t is the use of transmission-gates as depicted in Fig. A.5. Voltages are applied to the source/drain and a combination of NMOS pass transistors and PMOS pass networks are used. This logic is often used for implementing multiplexors and XOR-gates.

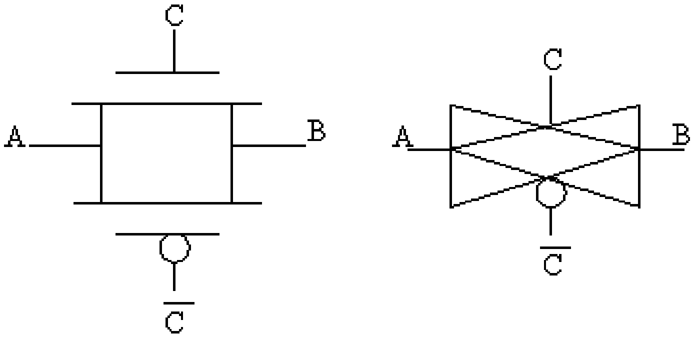

Figure A.5: Transmission-gate

[Raba03] J. M. Rabaey, A. Chandrakasan, B. Nikolic, "Designing combinational logic gates in CMOS", *Digital integrated circuits, University. of Berkeley, Prentice Hall*, 2003.

[Zimm97] R .Zimmermann, W. Fichtner, "Low-power logic styles: CMOS versus pass-transistor logic", *IEEE Journal of Solid-State Circuits*, vol. 32, no 7, p.1079-1090, July 1997.