Power-flow control and power-quality enhancement in interconnected distribution networks

Maialen Boyra

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Maialen BOYRA

Sujet:

Contrôle de flux de puissance et amélioration de la qualité de l'énergie dans les réseaux de distribution interconnectés

(Power-flow control and power-quality enhancement in interconnected distribution networks)

Soutenue le 3 Octobre 2012 devant les membres du jury:

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A mi familia.
A Cédric.

Remerciements

J'écris ces pages quelques jours après ma soutenance, dans la pénombre, assise au chaud dans le canapé de mon appartement de Malakoff. Aujourd'hui j'ai éprouvé une expérience qui m'a rappelé la thèse. Et je vais essayer d'expliquer pourquoi...

Je suis partie du travail (à Massy) à 19h. J'avais RDV à 20h donc j'ai pris le temps nécessaire sachant que je suis à vélo, que la nuit tombait et qu'il commençait à pleuvoir légèrement. Pas de problème pour la pluie : j'ai des habits et des sacoches imperméables. Pas de problème pour la nuit non plus : j'ai une lumière frontale et une sur le vélo. En étant bien équipés, nous pouvons faire n'importe quel voyage. Juste après partir je me suis aperçue que les freins faisaient un bruit aigu. J'ai vérifié et j'ai vu qu'il manquait un patin. Pas de problème... J'ai encore le frein arrière et la moitié du frein avant. Rien, à part ce bruit désagréable, ne m'empêchait de continuer. De cette façon, je traverse Verrières-le-Buisson et Anthony et j'arrive au Parc de Sceaux (à mi chemin des 11 km qui me séparent de chez moi). Parc de Sceaux est un bel endroit même s'il pleut des cordes ! Déviation. Je suis la déviation... Et, allez-hop ! Ca devait arriver: mon pneu crève. C'est la roue arrière. Et j'ai oublié mon portable à la maison ce matin... Je ne peux plus prévenir la personne qui m'attend à 20h. Patience, ce n'est que la loi de Murphy. J'ai appuyé le vélo dans un banc, j'ai enlève la roue arrière, j'ai enlevé la chambre. J'ai mis la nouvelle chambre et... comme par hasard, impossible de remettre le pneu à sa place. Patience Maialen. La pluie tombe, il est nuit, j'ai les mains et le blouson tout sales, mais il ne faut pas abandonner. J'essaie, j'essaie, j'essaie... J'ai mal aux doigts d'essayer. J'entends des personnes qui courent sous la pluie, j'entends des vélos qui passent par le chemin d'à côté. Il y a des personnes qui promènent leur chien... Et personne ne s'arrête pour m'offrir son aide. La pluie tombe et j'ai les mains endolories. Finalement, je réussi à emboiter le pneu. Super ! Il ne reste qu'à gonfler la chambre. Fu, fu, fu... Fu! Il y a un problème... La pompe ne fonctionne pas bien, l'air s'échappe. Et maintenant ? Comment vais-je retourner à la maison ? Dégoutée, je décide de rentrer à pied. A 5 km/h je serai à la maison dans environ une heure. Au bout de quelques centaines de mètres je décide de réessayer. Je me dis que, même pas trop gonflé, il faut que je réussisse à le gonfler moyennement pour arriver à destination. Je répète le procédé : décrocher les sacoches, sortir la pompe et fu, fu, fu... fu, fu, fu... Vas-y Maialen, un peu plus d'effort !!! Et une fois plus. Fu, fu, fu !!! Cette fois-ci il y a deux cyclistes qui s'approchent pour demander de l'aide. Je suis très reconnaissante mais je décline leur aide poliment parce que je ne veux pas les déranger sous la pluie. En plus, je suis proche de mon but. Fu, fu, fu !!! Je ferme la valve et allez-hop !!! C'est partie. Je peux repartir. La roue ne semble pas se dégonfler. Youhou !!! Quelle joie ! Je peux continuer tranquillement. Bien sûr, je ne suis pas arrivée à l'heure à mon RDV, mais la personne qui m'attendait n'était pas énervée. Elle était plutôt préoccupée de mon retard.

En rentrant chez moi j'ai eu ce sentiment que j'avais souvent pendant la thèse. Malgré les difficultés, il ne faut jamais capituler. Il faut être persévérant, tester des nouvelles solutions et ne

pas hésiter à demander de l'aide (même si je ne l'ai pas toujours fait). Après tout, peu importe si l'on arrive trempé et sale. L'important c'est d'y arriver, d'apprendre et d'en tirer les bonnes conclusions. Dans mon chemin je me demandais si je n'aurais pas dû prendre un autre chemin (la route plutôt que la Coulée Verte), si je n'aurais pas dû vérifier si la pompe marchait bien, si je ne devrais pas acheter une VTT au lieu d'un vélo de route, si je n'aurais pas dû enchainer le vélo à un arbre et rentrer en bus... J'ai aussi beaucoup douté de mes compétences. Comment est possible que j'ai mis plus d'une demi-heure à mettre le pneu dans la jante ? Pour quoi je n'ai plus de force pour gonfler la chambre? Est-ce que j'oublié de faire quelque chose ? Ce sont des questions que nous nous posons tous pendant la thèse. Mais, face aux questions, face à l'incertitude, face aux peurs, face aux mauvais moments, il faut toujours voir les choses de façon positive et apprendre à relativiser (merci Stéphanie pour ce bon conseil). La fin arrive toujours !! Peut-être nous ne voyons pas la forme exacte de la fin. Nous ne connaissons pas le résultat... Mais, il faut se dire que, tous les chemins ménent quelque part. Je me rappelle souvent de cet extrait d'Alice au Pays de Merveilles où le lapin demande à Alice vers où elle se dirige.... Elle lui répond qu'elle ne sait pas. Et le lapin réplique : *si tu ne sais pas où tu vas, tous les chemins sont bons.*

Tout ce discours juste pour dire que, la thèse est un chemin long et difficile et que il est très important d'être bien entouré. Pendant ces années de thèse j'ai croisé des personnes exceptionnelles. Personnes qui m'ont beaucoup appris et aidé sur le plan technique, personnes avec lesquelles j'ai philosophée, j'ai ri, j'ai pleuré, j'ai chanté, j'ai vu des *télénovelas*, j'ai dansé, j'ai cuisiné des plats inimaginables, j'ai voyagé, j'ai partagé de bons moments, j'ai fait du sport, j'ai fait la fête.... A Supélec, au CNAM, à la maison, mes amis en France, au Pays Basque, en Catalogne, en Espagne, en Suède, en Angleterre, à Hawaii, au Venezuela, et partout dans le monde, ma famille naturelle et d'adoption, mes rapporteurs et examinateurs, mes collègues chez Alstom et à l'INES... J'ai même peur de commencer à lister toutes les personnes de crainte d'oublier quelqu'un. Pour cela, il sera peut-être mieux d'en rester-là. UN GRAND MERCI A TOUS !!!

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Acronyms

ACRONYMS	Description
AC	Alternating Current
ADALINE	Adaptive Linear Neural Netwok
ADAPS	Autonomous Demand Power System
ALOF	Adaptive Linear Optimal Combiner
ANF	Adaptive Notch Filter
ANN	Artificial Neural Network
APF	Active Power Filter
B2B	Back-to-back
BSES	Back-up Stored Energy System
CIGRE	Conseil International des Grands Réseaux Électriques
CSC	Current Source Converter
DC	Direct Current
DDSRF-PLL	Decoupled Double SRF-PLL
DER	Distributed Energy Ressources
d-FACTS	Distribution FACTS
DFIG	Doubly Fed Induction Generator
DFT	Discrete Fourier Transform
DG	Distributed generation
DSC	Delayed Signal Cancellation
DSOGI	Dual Second Order Generalized Integrator
d-SSSC	Distribution SSSC
d-STATCOM	Distribution STATCOM
DVCC	Dual Vector Current Control
DVR	Dynamic Voltage Restorer
EKF	Extended Kalman Filter
EMC	Electromagnetic Compatibility
EPLL	Enhanced Phase Locked Loop
FACTS	Flexible AC Transmission System
FBD	Fryze-Buchnolz-Depenbrock
GTO	Gate Turn-Off Thyristor
HV	High Voltage
HVAC	High Voltage AC
HVDC	High Voltage Medium Current
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated Gate Bipolar Transistor
IGCT	Insulated Gate-Commutated Thyristor
IPFC	Interline Power Flow Controller
ISC	Instantaneous Sequence Component
KF	Kalman Filter

ACRONYMS	Description
LF	Loop Filter
LPC	Loop Power Flow Controllers
LPF	Low Pass Filter
LV	Low Voltage
MAF	Moving Average Filter
MMC	Modular Multilevel Converter
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MRF-PLL	Multiple Reference Frame-PLL
MV	Medium Voltage
MVDC	Medium Voltage Direct Current
OCS	Operation Control System
OHL	Over-head line
OPF	Optimal Power Flow
P	Active power
PCC	Point of Common Coupling
PD	Phase Detector
PES	Power and Energy Society
PhD	Philosophy Doctor
PI	Proportional-Integral
PLL	Phase-locked-loop
PNSC	Positive-Negative Sequence Calculator
PSF	Positive Sequence Filter
PST	Phase Shift Transformer
PWM	Pulse Width Modulation
Q	Reactive power
RDFT	Recursive Discrete Fourier Transform
SRF	Synchronous Reference Frame
SRF-PLL	Synchronous Reference Frame-PLL
SSI	Sinusoidal Signal Integrator
SSSC	Static Series Synchronous Compensator
STATCOM	Static Synchronous Compensator
STS	Static Transfer Switch
SVC	Static VAR Compensator
SVF	Space Vector Filter
SVR	Static Voltage Regulator
TCPAR	Thyristor Controlled Phase Angle Regulator
TCPST	Thyristor Controlled Phase Shift Transformer
TCSC	Thyristor Controlled Series Capacitor
TCSR	Thyristor Controlled Series Reactor
TCVR	Thyristor Controlled Voltage Regulator
THD	Total Harmonic Distortion
TIC	Information and Communication Technologies
TSSC	Thyristor Switched Series Capacitor
TSSR	Thyristor Switched Series Reactor
UHV	Ultra High Voltage
UPFC	Unified Power Flow Controller
UPLC	Unified Power Line Conditioner
UPQC	Unified Power Quality Conditioner

ACRONYMS	Description
UPS	Uninterruptible Power Supply
VCO	Voltage Controlled Oscillator
VSC	Voltage Source Converter
WLSE	Weighted Least Square Estimation

Summary in French

Introduction Générale

1. Vers les Réseaux Intélligents (Smartgrids)

Les réseaux électriques des pays industrialisés (tout particulièrement en Europe et aux États-Unis) ont été construits il y a plus d'un demi-siècle et demandent, par conséquent, à être modernisés et/ou remplacés [2].

Lors de leur conception leur architecture et fonctionnement étaient basés sur une structure verticale et compacte: au sein de chaque région, une seule société propriétaire gérait les réseaux de transport et de distribution (voir Fig.S1.1(a)). Ces réseaux électriques, construits selon les spécifications de l'époque, tendent à devenir, aujourd'hui, obsolètes.

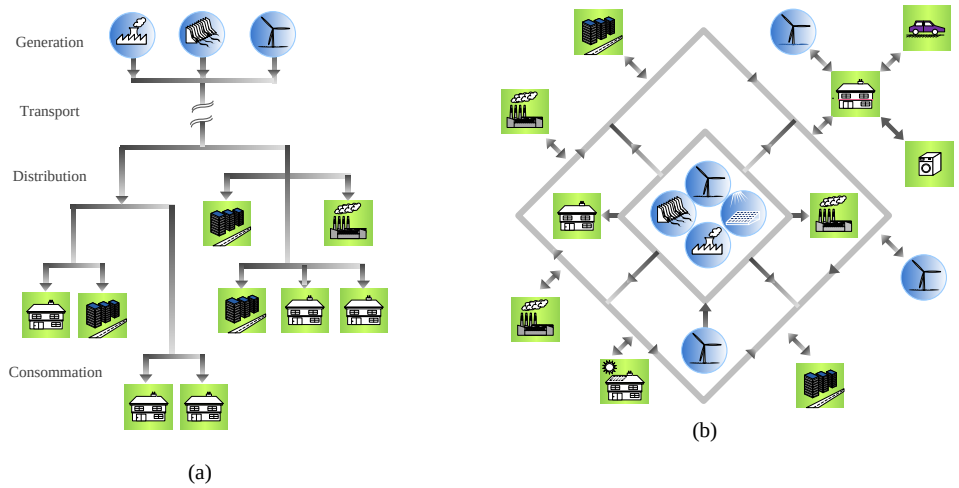


Figure S1.1: a) Structure verticale d'un réseau électrique, (b) Structure possible des réseaux électriques futurs.

Les changements émergeants et les développements des dernières décades conduisent à une nouvelle architecture: les Réseaux Intelligents ou, dans son terme anglophone, *Smartgrids* [3, 4].

La structure et l'opération des Réseaux Intelligents ne sont pas encore bien définies, mais il est clair que les Réseaux du Futur devront être flexibles, accessibles, fiables et économiques. Ainsi, il est essentiel que la recherche, le développement, et le déploiement des Réseaux Intelligents soient menés d'une façon cohérente en tenant compte des facteurs techniques, commerciaux et régulateurs [4].

Cette thèse traite de ces futurs Réseaux Intelligents et, plus concrètement, des réseaux de distribution intelligents.

2. Les réseaux de distribution du futur

Sous le nouveau paradigme des futurs réseaux électriques, des changements se produiront à toutes les échelles. Néanmoins, ces changements seront spécialement observés au niveau de la distribution, qui avait originalement été conçue selon un principe de *fit-and-forget* (fournir-et-oublier). La génération distribuée (DG), le stockage, la gestion de la demande, les infrastructures de mesure avancées, la distribution automatisée, les flux de puissance bidirectionnels et l'amélioration de la qualité de l'énergie représentent, par exemple, des changements au niveau de la distribution qui requerront une activité financière et de recherche significative [5]. En revanche, comme l'évolution des futurs réseaux de transport n'entre pas dans les objectifs de cette thèse, elle ne sera pas traitée dans le reste du manuscrit.

Il est impossible de parler de la structure des réseaux de distribution sans parler de la structure générale du réseau électrique traditionnel. En raison de la disponibilité technologique historique, le réseau électrique est fondamentalement AC et est classifié en trois niveaux fondamentaux: **le transport** (150-800 kV), **la répartition** (30-150 kV), et **la distribution** (<30 kV). La Fig.S1.2 montre un réseau électrique traditionnel. Celui-ci est structuré verticalement, les sources d'énergie sont centralisées, les flux de puissance sont prédictibles (d'amont à aval), et les opérateurs du réseau veillent au bon fonctionnement du système.

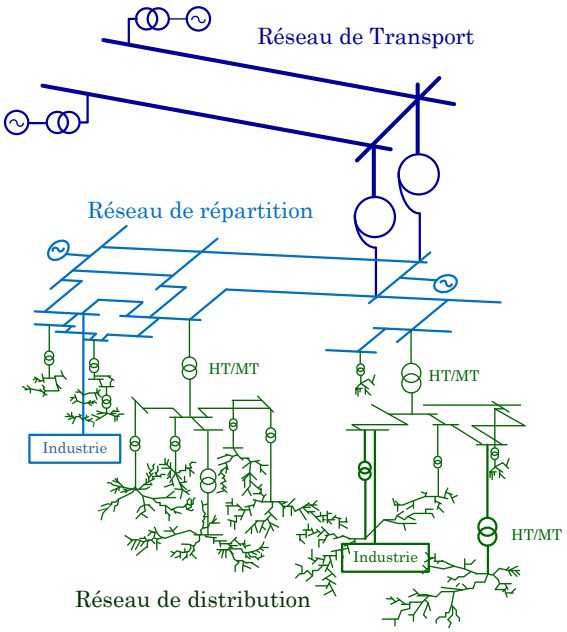


Figure S1.2: Structure du réseau électrique traditionnel (depuis [6])

2.1. Structure des réseaux de distribution

Pendant de longues années les réseaux de distribution ont été de simples terminaisons passives des réseaux de répartition. Traditionnellement les réseaux de distribution étaient peu surveillés et automatisés. La veille et le contrôle se développent maintenant.

Selon les cas, les réseaux de distribution peuvent être radiaux ou bouclés (voir Fig.S1.3):

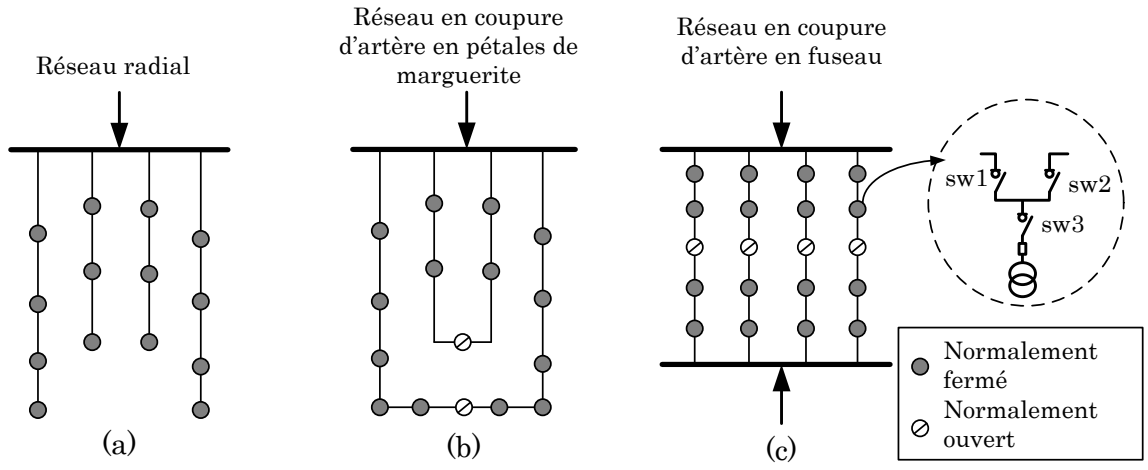


Figure S1.3: Structures radiales (a) et bouclées (b et c) des réseaux de distribution.

- **Les réseaux radiaux** présentent une structure arborescente avec des ramifications où les groupements de charges se connectent en forme de souches (ou clusters).
- **Les réseaux bouclés** incorporent des interrupteurs d'émergence qui sont normalement ouverts mais qui permettent d'établir des liaisons avec d'autres départs en cas de défaut d'intervention. Si les départs proviennent du même poste source, le réseau est un réseau de distribution en *coupure d'artère en boucles ou pétales de marguerite* (Fig.S1.3(b)) et, si les départs raccordés appartiennent à des postes sources différents, le réseau est un réseau en *coupure d'artère en fuseau* (Fig.S1.3(c)).

2.2. L'impact de la génération distribuée sur les réseaux de distribution

L'introduction massive des sources de génération distribuée est un des changements les plus importants et attendus dans les réseaux de distribution intelligents [7, 8]. L'intérêt pour la génération distribuée est bien justifié par les avantages qu'elle offre. D'un côté, comme la génération distribuée peut être proche des centres de consommation, le coût du transport, les pertes, et la demande de puissance réactive sont réduits. D'un autre côté, comme la taille des installations est plus petite, il est plus facile de trouver des emplacements pour leur implantation et les coûts d'investissement et de construction sont plus restreints.

Cependant, malgré les nombreux avantages de la génération distribuée, une pénétration trop importante de celle-ci aurait un impact (positif ou négatif, selon le cas) sur les facteurs suivants [9, 7]:

- Les profils de tension.
- Les systèmes de protection et de coordination.
- Les niveaux de court-circuit.
- La qualité de l'énergie et la fiabilité.
- Les pertes et les congestions.
- La stabilité.

2.3. Solutions pour mitiger l'impact de la génération distribuée sur les réseaux de distribution

Les effets adverses des réseaux de distribution peuvent être mitigés de plusieurs façons complémentaires:

- Le respect et développement des normes de connexion et des grid-codes.
- La gestion de la demande.
- L'utilisation des FACTS [1] de distribution et des appareils custom-power (voir Appendice A).
- La commande coordonnée de la génération distribuée.
- Le changement de la structure des réseaux de distribution.

  Cette thèse se concentre sur ce dernier point. Une topologie maillée offre des bienfaits appréciables par rapport à une topologie radiale. Si le maillage est fait de façon appropriée, c'est-à-dire, si le nombre et la disposition des points de raccordement sont bien sélectionnés, les bienfaits d'avoir une topologie maillée sont intensifiés par les avantages de la génération distribuée [10, 11, 12]: réduction des pertes, amélioration des profils de tension, report des investissements grâce à une utilisation plus optimale des ressources, amélioration de la stabilité etc.

  Le maillage des réseaux de distribution présente les désavantages suivants : (a) les niveaux de court-circuit augmentent, (b) la régulation de la tension via des régleurs en charge doit être révisée, et (c) la coordination des systèmes de protection devient compliquée.

1. FACTS: Flexible AC Transmission System

Parmi les multiples développements attendus, cette thèse privilégie la solution qui consiste à mailler les réseaux de distribution. Si les points d'interconnexion du réseau de distribution sont soigneusement sélectionnés il est possible d'augmenter la pénétration de DG, d'obtenir une distribution des flux de puissance plus homogène, de réduire les pertes, d'améliorer les profils de tension, de retarder les investissements et de renforcer la stabilité du réseau.

Même si cette solution peut paraître irréaliste pour l'instant, il faut garder à l'esprit que les réseaux de distribution tendront sûrement à émuler les réseaux de transport fournissant des services similaires et, pourquoi pas, avec des topologies et modes opératoires identiques.

3. Les objectifs de la thèse

Afin de proposer des solutions qui faciliteront une migration vers de réseaux de distribution plus maillés, les deux objectifs majeurs de cette thèse sont:

- L'étude d'une solution capable de moduler le flux de puissance (actif et réactif indépendamment) entre deux réseaux de distribution.
- Par ailleurs, la solution évaluée doit aussi être capable d'améliorer la qualité de l'énergie dans un des réseaux ou d'empêcher la propagation des perturbations d'un réseau à l'autre.

Le double défi de contrôler le flux de puissance et la qualité de l'énergie peut être satisfait simultanément par des appareils statiques d'électronique de puissance (s'adresser à l'Appendice A pour une description approfondie de ce type de solutions). Mais, parmi la grande sélection d'appareils disponibles, une configuration particulière, la topologie universelle, semble très adaptée pour répondre à ce challenge. La topologie universelle est née de l'association des topologies série (e.g. SSSC, DVR) et parallèle (e.g. STATCOM) et elle prend différents noms en fonction de l'application pour laquelle elle est utilisée. Ainsi, elle est connue comme Unified Power Flow Controller (UPFC), Unified Power Quality Conditioner (UPQC) ou Unified Power Line Conditioner (UPLC).

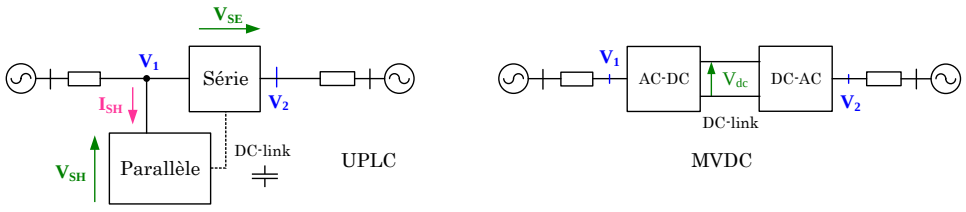


Figure S1.4: Illustration schématique d'un UPLC et d'un MVDC.

L'UPFC est utilisé dans les réseaux de transport pour contrôler le flux de puissance et régler la tension au point de connexion avec le réseau (côté parallèle). L'UPQC est utilisé dans les réseaux de distribution pour protéger les charges sensibles et dépolluer le réseau des émissions harmoniques et

réactifs produits par ces charges. Finalement, l'UPLC est un nom générique utilisé pour un appareil avec topologie universelle qui peut effectuer les fonctions typiques des UPFCs et des UPQCs.

Compte tenu des capacités exceptionnelles de l'UPLC, l'ambition principale de cette thèse réside à explorer le potentiel et l'intérêt de l'utiliser pour interconnecter deux réseaux de distribution. Pour donner une réponse structurée à ce projet les sous-objectifs suivants ont été établis:

- Evaluer le dimensionnement et la conception d'un UPLC.
- Modéliser l'UPLC en vue de sa commande.
- Analyser et développer des structures de commande de l'UPLC, spécialement dédiées à travailler dans des environnements perturbés. L'étude des méthodes de synchronisation et d'estimation des séquences symétriques instantanées est aussi envisagée.
- Valider des approches de commande développées en simulation.

Il ne faut néanmoins pas oublier que l'UPLC n'est pas le seul appareil à pouvoir combiner les fonctions de contrôle de flux de puissance et d'amélioration de la qualité électrique. Il existe, également, un appareil appelé Medium Voltage Direct Current (MVDC) qui, avec une topologie AC-DC-AC, est capable de réaliser les mêmes fonctions ou similaires (voir Fig.S1.4). En conséquence, un objective stratégique de cette thèse est la comparaison de l'UPLC, appareil privilégié dans cette thèse, avec le MVDC.

4. Plan de la thèse

Le manuscrit de thèse est scindé en quatre grandes parties:

- La **PARTIE I**, la partie actuelle, décrit, le contexte de cette thèse et introduit les objectifs principaux.
- La **PARTIE II** presente les travaux existants en matière d'interconnexion de réseaux de distribution, détaille l'UPFC, l'UPQC, l'UPLC et le MVDC et compare le UPLC avec le MVDC.
- La **PARTIE III** présente une étude approfondie sur l'UPLC, s'adressant aux sujets de la conception, dimensionnement, modélisation et commande d'un UPLC en régime perturbé.
- Finalement, la **PARTIE IV** synthétise les conclusions principales et les perspectives de travail futur.

5. Appareils statiques d'électronique de puissance pour l'interconnexion des réseaux de distribution

Cette thèse est essentiellement basée sur l'hypothèse que les réseaux de distribution futurs seront, au moins légèrement, maillés, et qu'il faudra des appareils statiques d'électronique de puissance pour redistribuer les flux de puissances et pour faire face aux problèmes liés à la qualité de l'énergie.

La redistribution des flux de puissance pourrait être faite suivant des critères de nature diverse. Par exemple, minimiser les pertes, minimiser les déviations de la tension, éviter le renversement du flux, éviter la saturation de certaines lignes et transformateurs etc.

Dans le cadre de cette thèse, deux topologies d'appareils ont été considérées comme les mieux adaptées et les plus souples pour interconnecter des réseaux de distribution : la topologie *universelle* et MVDC.

5.1. La topologie universelle : l'UPFC, l'UPQC et le UPLC

La topologie universelle (Fig.S1.4(a)) est composée de deux convertisseurs AC/DC raccordés par leur côté DC. Un des convertisseurs est connecté en *shunt* avec la ligne et l'autre est connecté en *série*. Comme la topologie universelle est naturellement très flexible, elle offre la possibilité d'utiliser la même structure pour des applications diverses. Cette souplesse a donné lieu à trois dénominations différentes qui correspondent à la même topologie mais à des applications différentes:

- **L'Unified Power Flow Controller (UPFC)**

  L'UPFC (Fig.S1.5) est un appareil FACTS de topologie universelle utilisé dans les réseaux de transport principalement pour la régulation de puissance et de tension. Cependant, il pourrait aussi être utilisé pour l'amortissement d'oscillations dynamiques et pour améliorer la stabilité transitoire du système électrique.

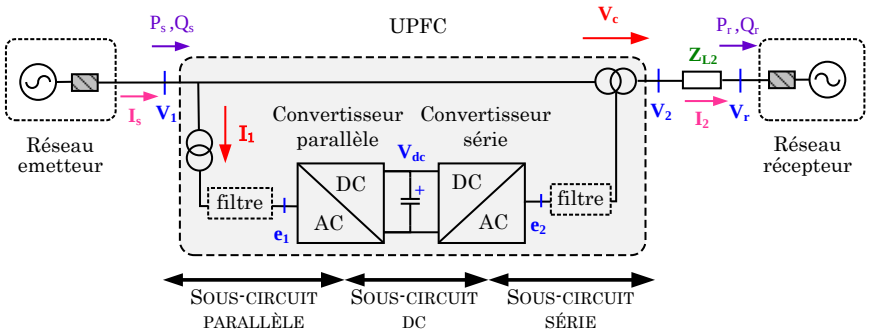


Figure S1.5: Représentation unifilaire d'un UPFC.

L'opération de base de l'UPFC peut être comprise en observant la Fig.S1.6, où le convertisseur série, représenté comme une source de tension AC parfaite, injecte une tension $\mathbf{V_r}$ qui est

ajouté à la tension $\mathbf{V_1}$ pour faire varier $\mathbf{V_2}$ selon le flux de puissance souhaité. Les équations (S1.1) et (S1.2) indiquent comment les puissances P_r et Q_r au point de réception peuvent être affectées en jouant avec la magnitude et l'angle de la tension $\mathbf{V_2}$.

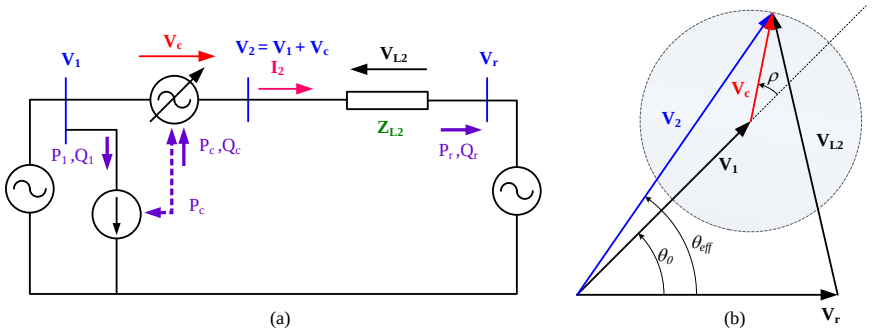


Figure S1.6: Principe d'opération de l'UPFC : (a) Diagramme unifilaire simplifié, (b) Diagramme vectoriel.

$$P_r = \frac{V_2 V_r}{X_L} \sin\delta \tag{S1.1}$$

$$Q_r = \frac{V_2 V_r \cos\delta - {V_r}^2}{X_L} \tag{S1.2}$$

Pour le cas illustré dans la Fig.S1.6, où la ligne est purement réactive (X_L), les zones de P_r et Q_r ont été cartographiées dans la Fig.S1.7. Les zones contrôlables de P_r et Q_r dépendent de l'angle de transmission entre les deux réseaux, θ_0, et de la magnitude maximale de la tension série injectée $V_{c(max)}$. D'après la figure, quand $\theta_0 = 0$ il est possible de fournir une puissance réactive négative mais, au-fur-et-à-mesure que θ_0 augmente, la zone atteignable commence à tourner et il devient impossible de garantir $Q_r < 0$. La seule façon d'augmenter l'étendue de la zone d'opération est d'augmenter la tension série maximale. Cette propriété pourrait constituer un inconvénient de l'UPFC.

- **L'Unified Power Quality Conditioner (UPQC)**

  L'UPQC [13, 14, 15] est un appareil de type custom-power qui sert à compenser les problèmes liés à la qualité de l'énergie dans les réseaux de distribution. Normalement, le bras en parallèle s'occupe de compenser les harmoniques de courant et le facteur de puissance d'une charge proche tandis que le bras en série est chargé de compenser les creux de tension qui peuvent nuire les charges sensibles (voir Fig.S1.8). Généralement les niveaux de tension et de puissance des UPQC ne sont pas comparables à ceux des UPFC (des centaines de kVA versus des centaines de MVA, respectivement).

- **L'Unified Power Line Conditioner (UPLC)**

  L'UPLC est un nom générique attribué aux appareils qui peuvent réaliser les fonctions des UPFC et des UPQC de façon combinée. Cet appareil a été introduit par [14, 16] mais, en vue des difficultés de dimensionnement et de commande, il pourrait être plutôt considéré

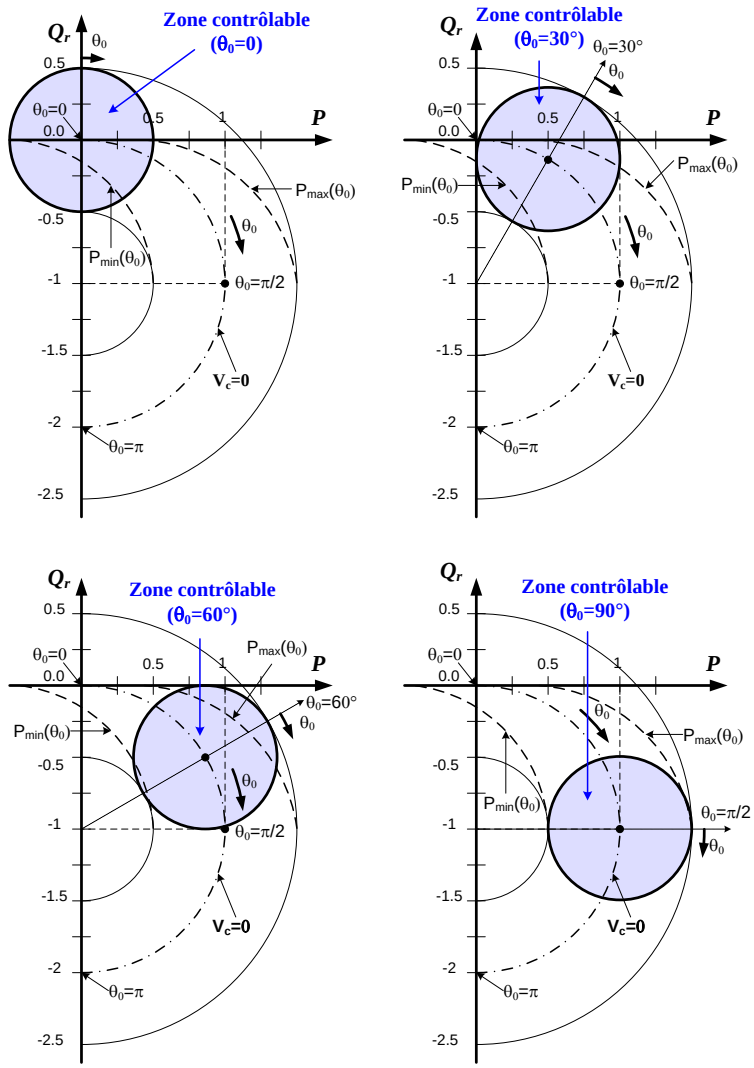


Figure S1.7: Aires contrôlables de de P_r et Q_r en termes de θ_0, ρ, et $V_{c(max)}$ (valeurs normalisés).

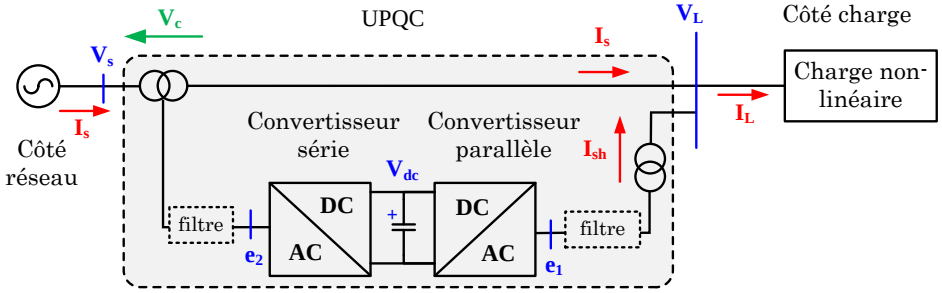


Figure S1.8: Représentation unifilaire d'un UPQC.

comme un concept théorique que comme un appareil réalisable/intéressant dans la pratique. Cependant, dans le reste du manuscrit le nom UPLC sera utilisé pour dénommer un appareil quelconque avec topologie universelle.

5.2. Le MVDC (Medium Voltage Direct Current)

Le MVDC est le équivalent du très connu HVDC (High voltage Direct Current) et la topologie AC-DC-AC lui permet de dissocier deux réseaux AC totalement, comme il est indiqué dans la Fig.S1.9. Le HVDC est de plus en plus étendue dans le monde, avec plus de 100 projets en opération ou en phases avancées de réalisation [17, 18].

Contrairement au HVDC, le MVDC n'est pas encore utilisé pour le transport de l'énergie électrique, ni pour l'interconnexion des réseaux, au niveau de la distribution. Cependant, des MVDCs peuvent être trouvés dans des applications spécifiques (par exemple, dans le secteur maritime ils sont utilisés pour la distribution de l'électricité dans les plateformes marines, et pour l'interconnexion des bateaux au port). Le VSC-MVDC [2] est totalement réversible et est capable de travailler dans tous

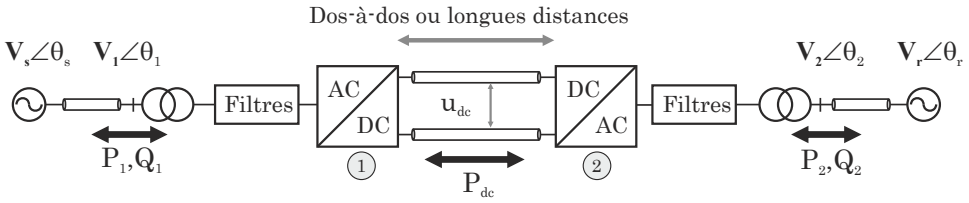


Figure S1.9: Diagramme schématique unifilaire d'un MVDC.

les quatre quadrants de PQ. Ce fait constitue un avantage signifiant par rapport aux CSC-MVDC [3] et aux UPLCs (voir Fig.S1.7).

6. Comparaison entre l'UPLC et le MVDC

L'UPLC et le MVDC peuvent être comparés selon plusieurs points de vue. Dans cette thèse, les deux appareils ont été comparés en fonction de leur structure, des caractéristiques de l'interconnexion, des objectifs réalisables, et de leur taille.

6.1. Avantages et désavantages de l'UPLC et du MVDC

La comparaison détaillée étant fournie dans le manuscrit principal, les principaux avantages et inconvénients sont résumés dans le Tableau S1.1 .

Table S1.1: Tableau comparative entre un UPLC et un MVDC.

	Caractéristiques	**UPLC**	**MVDC**

2. VSC: Voltage Source Converter
3. CSC: Current Source Converter

	Caractéristiques	**UPLC**	**MVDC**
Structure	Possibilité d'éloigner les convertisseurs	• Possible mais unintéressant (dans la pratique seulement une application *dos-à-dos* est économique): - 5 lignes sont nécessaires (3 AC + 2 DC)	• Possible: - Les deux options (*dos-à-dos* ou éloignés), sont possibles. - Seulement 2 lignes DC sont nécessaires dans l'interconnexion.
	Protections et fiabilité	• Possible de court-circuiter l'appareil connecté en série avec un système de protection (cher). • Le transformateur série est un élément sensible et doit être traité avec précaution.	• Normalement, impossible de court-circuiter l'appareil (seulement si la connexion est *dos-à-dos*). • Une redondance est nécessaire pour assurer la continuité du service.
	Symétrie et réversibilité	• Pas symétrique. • La réversibilité dépend de l'angle de transport et la valeur de la tension injectée en série.	• Symétrique. • Possibilité d'opérer dans les 4 quadrants de PQ (la réversibilité ne dépend pas de l'angle de transport).
Caractéristiques de l'interconnexion	Distance d'interconnexion	• Si la distance d'interconnexion est courte, il est possible de choisir une connexion dos-à-dos. Dans ce cas, la taille des appareils dépendra de l'angle de transport et du ratio x/r des lignes. Pour un ratio x/r=1, l'UPLC sera plus petit par rapport au MVDC si l'angle entre les points d'interconnexion est petit. • Si la distance d'interconnexion est longue, l'évaluation devient plus compliquée parce qu'il faut comparer différents scénarios. - L'UPLC ne peut pas être séparé tandis que le MVDC peut l'être ou non. - Les avantages de séparer les deux convertisseurs du MVDC sont que les deux convertisseurs peuvent travailler de façon autonome sans avoir besoin de communiquer entre eux et qu'il n'y a besoin que de deux lignes DC d'interconnexion.	
	Connexion synchrone/asynchrone	• Seulement connexions synchrones.	• Connexions synchrones et asynchrones.
	Angle de transport	• Normalement, si l'angle de transport est petit, l'UPLC est plus réduit que le MVDC. • La réversibilité de l'UPLC dépend de l'angle de transport.	• La réversibilité du MVDC est indépendante de l'angle de transport.
	Propriétés de lignes/câbles	• Les câbles AC ont plus de pertes que les câbles DC (effet des peaux, courants de Foucault dans l'écran, courants capacitifs de fuite . . .)	
Fonctions réalisables	Flux de puissance	• Les zones contrôlables de P et Q dépendent de l'angle de transport et de la tension série injectée.	• Opération dans les quatre quadrants.

	Caractéristiques	**UPLC**	**MVDC**
	• Compensation des creux de tension. • Régulation de la tension. • Compensation de flicker, des harmoniques, des déséquilibres.	• Les deux appareils permettent d'effectuer les mêmes fonctions. Dans tous les cas il est possible d'adopter une stratégie *active* ou une stratégie *passive*. - La stratégie *active* consiste à vouloir compenser la perturbation au point de mesure. - La stratégie *passive* consiste à éviter que la perturbation se propage à l'autre réseau.	
Taille		• En résumé, la taille des appareils dépendra de plusieurs paramètres: - De la distance d'interconnexion. - De la configuration utilisée (*dos-à-dos* ou séparée). - L'angle de transport. - Les types de lignes (aériennes ou câbles). • Dans le cas particulier d'une topologie dos-a-dos, avec une distance d'interconnexion courte, et un ratio x/r autour de l'unité, l'UPLC est plus petit qu'un MVDC.	

6.2. Comparaison en termes de taille : un exemple indicatif

D'après la Fig.S1.10, dans le cas d'un MVDC toute la puissance active qui est transférée du réseau émetteur au réseau récepteur doit traverser le bus DC. Ainsi, $P_1 = P_2 = P_{dc-MVDC}$. Cependant, dans le cas de l'UPLC, seul une partie de la puissance active totale transférée traverse le bus DC. La puissance qui circule par le bus DC ($P_{dc-MVDC}$ et $Pdc-UPLC$) est un paramètre important qui déterminera considérablement la taille des appareils. Un autre paramètre important, qui vient s'ajouter à la puissance active transférée, et qui déterminera aussi la taille des appareils est la puissance réactive que chacun des convertisseurs doit injecter.

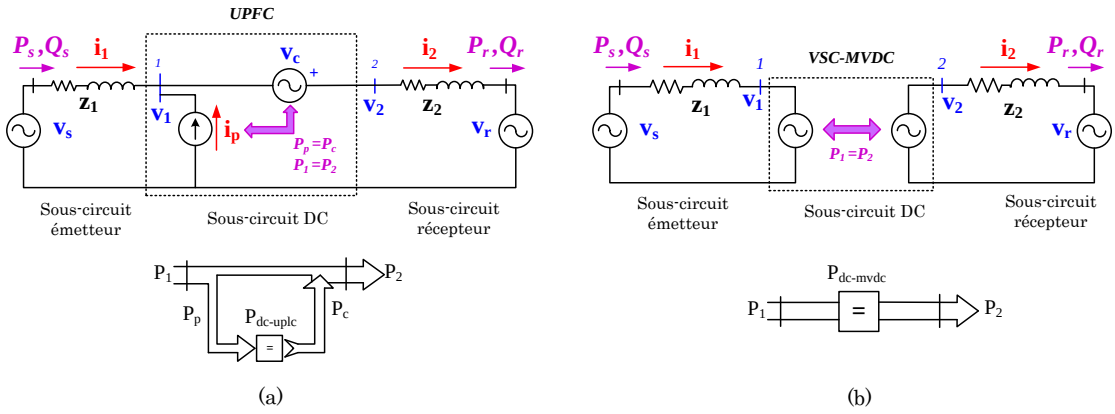


Figure S1.10: Transfert de puissance active dans l'UPLC (a) et dans le MVDC (b).

Afin d'obtenir un ordre de grandeur de la différence de taille entre un UPLC et un MVDC, un cas particulier a été étudié. L'objectif de cette analyse est de déterminer le ratio entre la puissance

active qui traverse le bus DC d'un MVDC et celle qui traverse le bus DC d'un UPLC dans différentes conditions.

$$\text{DC-power ratio} = \frac{P_{dc-MVDC}}{P_{dc-UPLC}} \tag{S1.3}$$

La comparaison a été effectuée considérant le cas de la Fig.S1.11 où $Q_s = 0$, $Q_r = 0$, et P_{r0} indique la puissance active qui arrive au réseau récepteur quand l'appareil est court-circuité. Après une

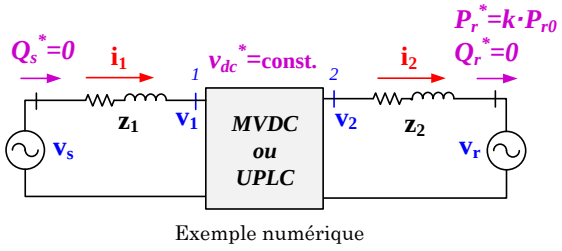


Figure S1.11: Représentation du cas d'étude.

batterie de simulations, dans lesquelles les valeurs de k, θ_0 et de x/r ont fait l'objet de variation, il est possible de conclure que:

- Le ratio $P_{dc-MVDC}/P_{dc-UPLC}$ est plus petit que l'unité jusqu'à une valeur limite de θ_0. Par exemple, dans la Fig.S1.12(a), où $k = 1.5$, la valeur limite de θ_0 est de 90 degrés (pour $x/r = 1$). Cela veut dire que, l'UPLC sera relativement plus petit que le MVDC si la différence d'angle entre les deux réseaux se maintient en dessous de 90 degrés. De façon similaire, comme tracée dans la Fig.S1.12(b), la valeur limite de θ_0 pour le cas où $k = -1.5$ est de 60 degrés (pour $x/r \to +\infty$).

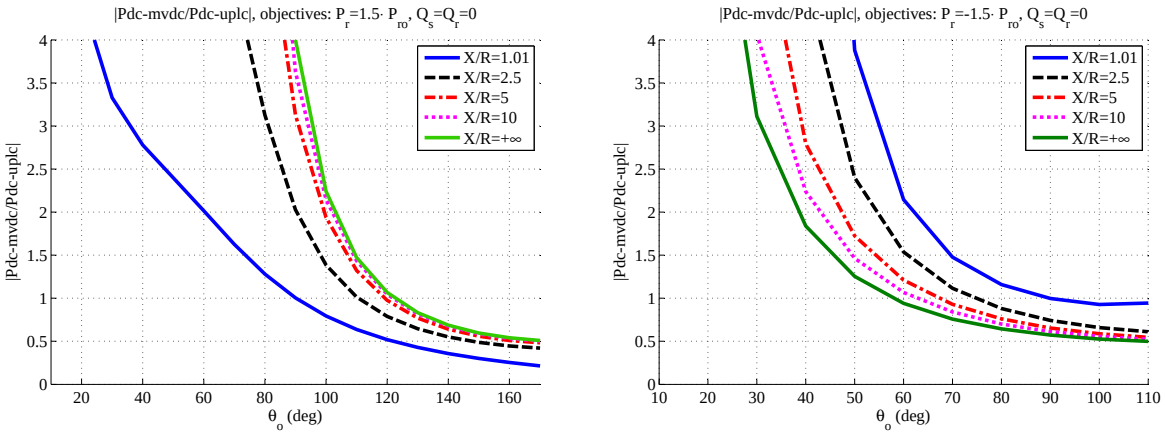


Figure S1.12: (a) Les ratios de $|P_{dc-MVDC}/P_{dc-UPLC}|$ pour $k = 1.5$, (b) Les ratios de $|P_{dc-MVDC}/P_{dc-UPLC}|$ pour $k = -1.5$

Partie II. L'UPLC pour l'interconnexion des réseaux de distribution

Malgré les avantages irréfutables du MVDC, dans cette thèse l'UPLC a été finalement sélectionné pour être étudié plus profondément. Ce choix est justifié par le fait que les dimensions de l'UPLC peuvent être inférieures à celles du MVDC sous certaines conditions. L'objectif de la deuxième partie de la thèse consiste à analyser et à comprendre les implications d'intégration d'un UPLC dans les réseaux de distribution. Il faut garder à l'esprit que jusqu'à maintenant seulement trois UPFC ont été installés dans le monde (deux aux États-Unis et un en Corée) et, ceux-ci, au niveau de transport. Pour installer un UPLC au niveau de la distribution, il faut considérer des aspects additionnels. Par exemple:

- Dans les réseaux de distribution il y a normalement plus de câbles que dans les réseaux de transport (spécialement dans les zones très peuplées).
- Dans les réseaux de distribution la qualité de l'énergie est manifestement inférieure à celle des réseaux de transport [19]. Ainsi, le nombre de creux de tension et d'harmoniques est typiquement supérieur.
- La structure, la topologie, et l'opération des réseaux de distribution est différente de celles des réseaux de transport (ils sont généralement opérés radialement, il y a différents types de connexions à terre etc.).

La partie III du manuscrit évalue et débat des aspects liés au dimensionnement et à la commande d'un UPLC qui sert à interconnecter des réseaux de distribution. Le dimensionnement et la modélisation de l'UPLC sont traités dans le manuscrit principal.

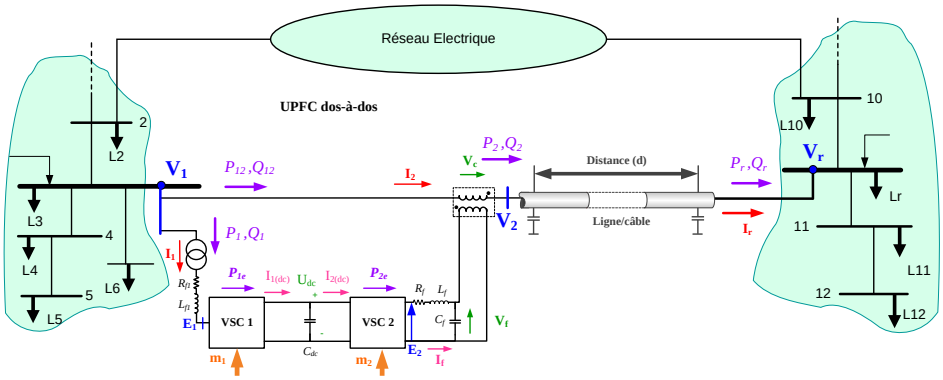


Figure S2.1: Représentation unifilaire d'un UPLC qui interconnecte deux réseaux de distribution.

1. Commande vectorielle orientée à la référence synchrone positive (avec ligne RL)

Dans le cas de signaux multi-phase, comme c'est les cas des systèmes triphasés, la sélection du type de commande dépend du cadre de travail qui est choisi (naturel, statique ou rotatif). Les références rotatives synchrones (SRFs), en particulier, sont très utilisées dans les systèmes électroniques raccordés aux réseaux parce qu'elles transforment des signaux alternatifs en signaux alternatifs en signaux constants. De plus, la plupart des travaux liés aux UPFC considèrent des SRFs [20, 21, 22, 23, 24, 25, 26, 27, 28]. Ceci dit, dans cette thèse des cadres rotatifs synchrones (dq) seront utilisés.

L'objectif final de cette thèse est de développer une structure de commande capable de contrôler un UPLC connecté à un câble dans un régime perturbé. Cependant, avant de s'attaquer à ce défi, le premier pas (chapitre III.3) sera de développer et de valider la commande sélectionnée dans un système idéal et avec une ligne RL.

Le modèle de l'UPLC peut être représenté, de façon compacte, par l'expression:

$$\dot{\mathbf{x}} = \mathbf{A}(\omega)\mathbf{x} + g(\mathbf{x}, \mathbf{u}) + \mathbf{D}\ \mathbf{d} \tag{S2.1}$$

où $\mathbf{x}$ représente le vecteur d'état, $\mathbf{x} = [i_{2d}, i_{2q}, v_{fd}, v_{fq}, i_{fd}, i_{fq}, i_{1d}, i_{1q}, u_{dc}]^t$, $\mathbf{u}$ représente le vecteur des commandes, $\mathbf{u} = [m_{2d}, m_{2q}, m_{1d}, m_{1q}]^t$, $\mathbf{d}$ symbolise le vecteur des perturbations, $\mathbf{d} = [v_{1d}, v_{1q}, v_{rd}, v_{rq}]^t$, $\mathbf{A}(\omega)$ est la matrice d'état, ω indique la fréquence angulaire de la référence, et $\mathbf{D}$ est la matrice des perturbations.

Le modèle de l'UPLC présente une structure multi-variable avec des relations nonlinéaires entre les variables d'état et les variables de commande. Le système représenté par l'équation (S2.1) contient 9 variables d'état, 4 variables de commande, et 4 perturbations. Cependant, pour simplifier le contrôle du système il est possible de diviser toute la commande en deux sous-parties (Fig.S2.2): la commande de la partie série, et la commande de la partie parallèle.

La commande de la partie série est en charge de la fonction principale, la modulation de flux de puissance, et la partie parallèle est essentiellement en charge de la tenue en tension de la liaison DC et, éventuellement, de l'injection d'énergie réactive.

Les deux sous-modèles sont représentés par les équations suivantes et par la Fig.S2.2:

$$\text{Series subsystem} \Longrightarrow \left\{ \dot{\mathbf{x}}_{\mathbf{se}} = \mathbf{A}_{\mathbf{se}}\ \mathbf{x}_{\mathbf{se}} + k_2 \cdot x_{sh(2)} \cdot \mathbf{u}_{\mathbf{se}} + \mathbf{D}_{\mathbf{se}}\ \mathbf{d}_{\mathbf{se}} \right. \tag{S2.2}$$

$$\text{Shunt subsystem} \Longrightarrow \begin{cases} \dot{\mathbf{x}}_{\mathbf{sh(1)}} & = \mathbf{A}_{\mathbf{sh}}\ \mathbf{x}_{\mathbf{sh(1)}} + k_1 \cdot x_{sh(2)} \cdot \mathbf{u}_{\mathbf{sh}} + \mathbf{D}_{\mathbf{sh}}\ \mathbf{d}_{\mathbf{sh}} \\ \dot{x}_{sh(2)} & = \dfrac{k_1}{c'_{dc}}\ \mathbf{u}_{\mathbf{sh}}{}^{\mathbf{t}} \cdot \mathbf{x}_{\mathbf{sh(1)}} - \dfrac{k_2}{c'_{dc}}\ \mathbf{u}_{\mathbf{se}}{}^{\mathbf{t}} \cdot \mathbf{x}_{\mathbf{se(5:6)}} \end{cases} \tag{S2.3}$$

où $\mathbf{x}_{\mathbf{se}} = [i_{2d}, i_{2q}, v_{fd}, v_{fq}, i_{fd}, i_{fq}]^t$, $\mathbf{u}_{\mathbf{se}} = [m_{2d}, m_{2q}]^t$, $\mathbf{d}_{\mathbf{se}} = [v_{1d}, v_{1q}, v_{rd}, v_{rq}]^t$, $\mathbf{x}_{\mathbf{sh}} = [\mathbf{x}_{\mathbf{sh(1)}}\ x_{sh(2)}]^t$, $x_{sh(2)} = u_{dc}$, $\mathbf{x}_{\mathbf{sh(1)}} = [i_{1d}, i_{1q}]^t$, $\mathbf{u}_{\mathbf{sh}} = [m_{1d}, m_{1q}]^t$, $\mathbf{d}_{\mathbf{sh}} = [v_{1d}, v_{1q}]^t$.

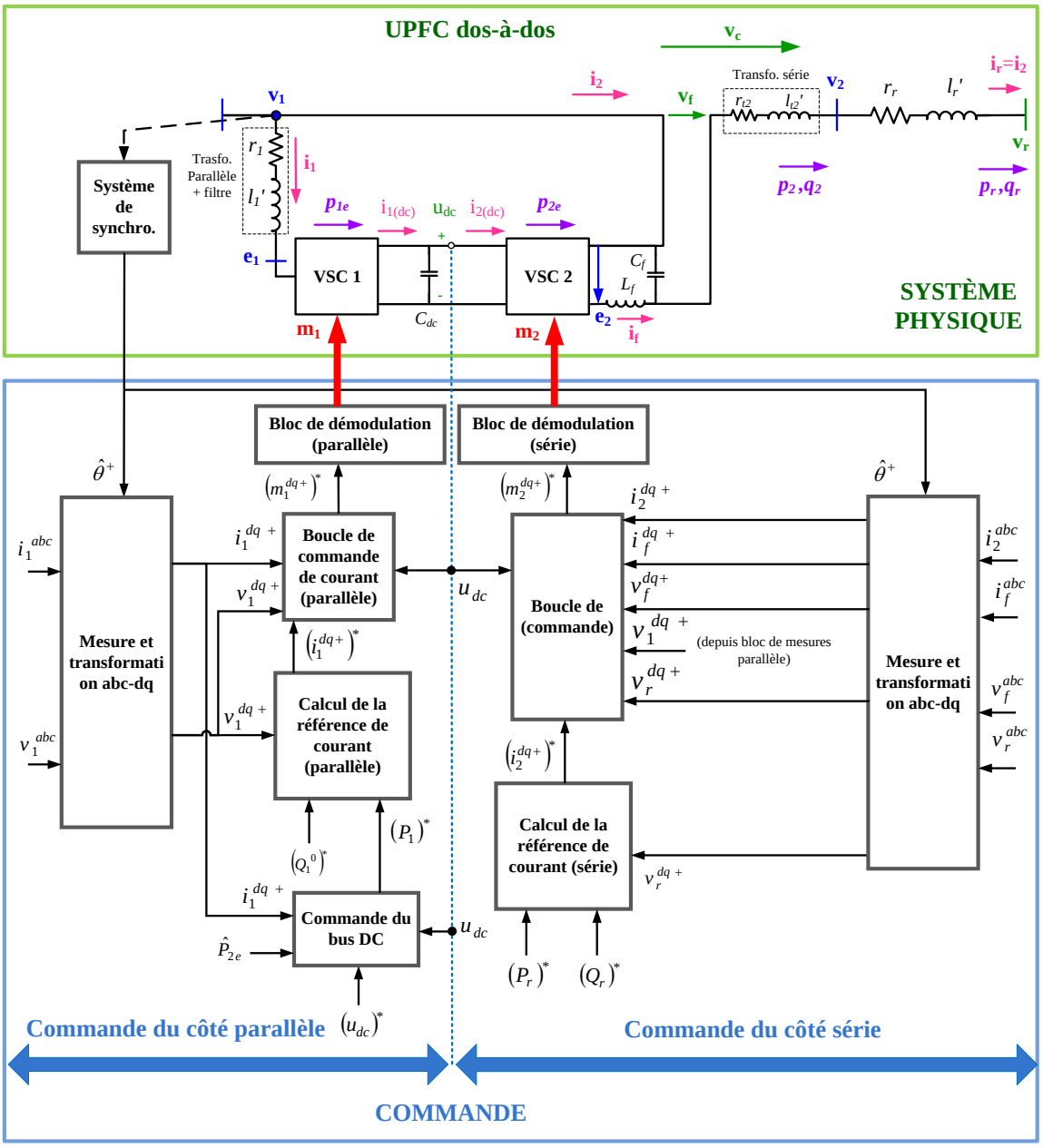


Figure S2.2: Structure de commande d'un UPLC connecté à une ligne RL et orienté selon une SRF.

Comme il peut être observé, la dynamique de $\mathbf{x_{se}}$ dépend de $\mathbf{x_{sh(1)}}$ et, la dynamique de $x_{sh(2)}$ dépend de $\mathbf{x_{sh(1)}}$, $\mathbf{x_{se(5:6)}}$, $\mathbf{u_{sh}}$ et de $\mathbf{u_{se}}$. Une manière de régler le problème lié aux relations croisées est de contrôler $x_{sh(2)} = u_{dc}$ très lentement par rapport aux autres variables d'état. De cette façon, un découplage temporel est obtenu.

1.1. Commande série d'un UPLC connecté à une ligne RL

La commande de la partie série, qui est illustrée dans la Fig.S2.3, est dissocié en deux niveaux: une commande globale et une commande locale (avec trois contrôleurs locaux).

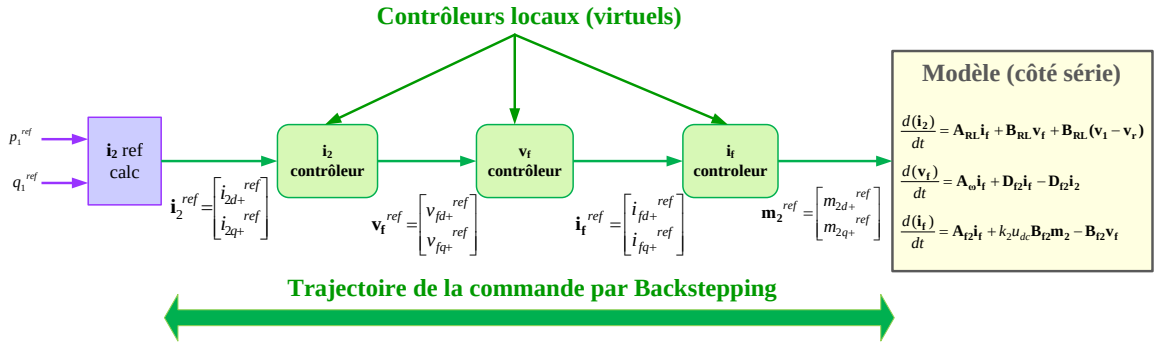


Figure S2.3: Concept de *Backstepping* appliqué à la commande de la partie série.

La **commande globale** du système série, qui est basée sur une philosophie de contrôle de type Backstepping, est en charge de générer des références virtuelles de commande pour les états intermédiaires du système. Elle découpe un problème de commande complexe dans une série de sous-systèmes plus simples à commander. Ce concept peut être compris en regardant la structure des équations de la partie série (les formes développées des matrices présentes dans les équations suivantes peuvent être trouvées dans l'Appendice E), qui se trouvent sous la forme particulière de *strict-feedback*:

$$\frac{d\,\mathbf{i_2}}{dt} = \mathbf{A_{RL}} \cdot \mathbf{i_2} + \mathbf{B_{RL}} \cdot \mathbf{v_f} + \mathbf{B_{RL}} \cdot (\mathbf{v_1} - \mathbf{v_r}) \qquad \mathbf{i_2} \rightarrow \mathbf{i_2}^{ref} \implies \mathbf{v_f}^{ref} \tag{S2.4}$$

$$\frac{d\mathbf{v_f}}{dt} = \mathbf{A}_{\omega}\ \mathbf{v_f} + \mathbf{D_{f2}}\ \mathbf{i_f} - \mathbf{D_{f2}}\ \mathbf{i_2} \qquad \mathbf{v_f} \rightarrow \mathbf{v_f}^{ref} \implies \mathbf{i_f}^{ref} \tag{S2.5}$$

$$\frac{d\mathbf{i_f}}{dt} = \mathbf{A_{f2}}\ \mathbf{i_f} + k_2 \cdot u_{dc} \cdot \mathbf{B_{f2}}\ \mathbf{m_2} - \mathbf{B_{f2}}\ \mathbf{v_f} \qquad \mathbf{i_f} \rightarrow \mathbf{i_f}^{ref} \implies \mathbf{m_2}^{ref} \tag{S2.6}$$

- Suivant les équations S2.4, S2.5, et S2.6, le contrôleur local plus amont est en charge de calculer la référence $\mathbf{v_f}^{ref}$ à partir de la référence $\mathbf{i_2}^{ref}$, qui a été calculée en fonction des puissances souhaitées dans le réseau récepteur.
- Ensuite, le contrôleur intermédiaire est en charge de calculer la référence $\mathbf{i_f}^{ref}$ à partir de la référence $\mathbf{v_f}^{ref}$.
- Et, finalement, le contrôleur local plus aval se chargera de calculer la référence $\mathbf{m_2}^{ref}$ à partir de la référence $\mathbf{i_f}^{ref}$.

Les **contrôleurs locaux** ont été conçus à partir de la théorie de la stabilité de Lyapunov, utilisant une fonction quadratique de Lyapunov du type:

$$V(\mathbf{e}) = \frac{1}{2}\mathbf{e}^{\mathrm{T}}\mathbf{e} \tag{S2.7}$$

où $\mathbf{e}$ représente l'erreur de suivi, $\mathbf{e} = \mathbf{x}^{ref} - \mathbf{x}$.

De façon générale, pour un système générique de la forme:

$$\dot{\mathbf{x}} = f(\mathbf{x}) + g(\mathbf{x})\mathbf{u} \tag{S2.8}$$

Les contrôleurs locaux prendront la forme:

$$\mathbf{u} = g(\mathbf{x})^{-1}\left[+\mathbf{k_0 e} + \mathbf{k_1}\cdot sgn(\mathbf{e}) - f(\mathbf{x}) + \dot{\mathbf{x}}^{ref}\right] \tag{S2.9}$$

Et, plus précisement:

$$\mathbf{v_f^{ref}} = \mathbf{B_{RL}}^{-1}\left\{\mathbf{K_{i2-0}}\ \mathbf{e_{i2}} + \mathbf{K_{i2-1}}\cdot sgn\left(\mathbf{e_{i2}}\right) + \frac{d\mathbf{i_2}^{ref}}{dt} - \mathbf{A_{RL}}\ \mathbf{i_2} - \mathbf{B_{RL}}\ (\mathbf{v_1} - \mathbf{v_r})\right\} \tag{S2.10}$$

$$\mathbf{i_f^{ref}} = \mathbf{D_{f2}}^{-1}\left\{\mathbf{K_{vf-0}}\ \mathbf{e_{vf}} + \mathbf{K_{vf-1}}\cdot sgn\left(\mathbf{e_{vf}}\right) + \frac{d\mathbf{v_f}^{ref}}{dt} - \mathbf{A}_{\omega}\ \mathbf{v_f} + \mathbf{C_{f2}}\ \mathbf{i_2} + \mathbf{B_{RL}}^{\mathrm{T}}\ \mathbf{e_{i2}}\right\} \tag{S2.11}$$

$$\mathbf{m_2^{ref}} = \frac{k_2}{u_{dc}}\ \mathbf{B_{f2}}^{-1}\left\{\mathbf{K_{if-0}}\ \mathbf{e_{if}} + \mathbf{K_{if-1}}\cdot sgn\left(\mathbf{e_{if}}\right) + \frac{d\mathbf{i_f}^{ref}}{dt} - \mathbf{A_{f2}}\ \mathbf{i_f} + \mathbf{B_{f2}}\ \mathbf{v_f} + \mathbf{D_{f2}}^{\mathrm{T}}\ \mathbf{e_{vf}}\right\} \tag{S2.12}$$

Cette structure de commande, avec les contrôleurs locaux proposés, a été testée et validée en simulations en SimPowerSystems sous de multiples conditions (conditions nominales et creux de tension) et avec des convertisseurs *réels*. Dans toutes les situations simulées elle a montré une bonne dynamique de suivi ($\approx 1.2ms$).

Cependant, cette technique a montré un point faible au moment de vérifier sa robustesse paramétrique. En fait, les contrôleurs locaux ont été développés en considérant des modèles continus. Mais, comme dans la réalité le système n'est pas continu (il est échantillonné à $10\mu s$ et la MLI du convertisseur à un période de $200\mu s$) il n'est toujours pas possible d'augmenter les gains du système arbitrairement sans avoir du *chattering* (le chattering est un mouvement de zig-zag autour de la surface de glissement).

Les seules solutions pour éviter le chattering sont:

(i) réduire les périodes d'échantillonnage, ce qui n'est pas toujours possible, ou

(ii) remplacer la fonction *sign* par des fonctions plus *douces* (la fonction saturation ou *tanh*, par exemple). Cette deuxième alternative peut générer une erreur statique.

1.2. Commande parallèle d'un UPLC connecté à une ligne RL

La dynamique de la partie parallèle est représentée par les équations de courant parallèle et de la tension DC.

- Les équations de courant parallèle sont données sous la forme suivante:

$$\frac{d\ \mathbf{i_1}^{(dq+)}}{dt} = \mathbf{A_{1(dq+)}}\cdot\mathbf{i_1}^{(dq+)} + \mathbf{B_1}\cdot\mathbf{v_1}^{(dq+)} - \mathbf{B_1}\cdot\mathbf{e_1}^{(dq+)} \tag{S2.13}$$

où $\mathbf{i_1}$ symbolise les variables d'état contrôlées, $\mathbf{m_1}$ est le vecteur de commande, et $\mathbf{v_1}$ se comporte comme une perturbation.

Dans l'équation (S2.13) le vecteur de commande $\mathbf{m_1}$ est multiplié par u_{dc}, qui est une autre variable d'état. Il peut être trivialement démontré qu'il y a un couplage entre les dynamiques des courants et de la tension DC.

- L'expression de u_{dc} vient donnée par:

$$\frac{d\ u_{dc}}{dt} = \frac{1}{c'_{dc}\ u_{dc}}[p_{1e} - p_{2e}] \quad \text{or,} \qquad \dot{z} = \frac{d\ (u_{dc})^2}{dt} = \frac{2}{c'_{dc}}[p_{1e} - p_{2e}] \tag{S2.14}$$

La dynamique de u_{dc} dépend de la différence de puissances actives p_{1e} et p_{2e} qui, en même temps, dépendent de u_{dc}, de $\mathbf{m_1}$ et des courants ($p_e = \mathbf{e}\cdot\mathbf{i} = k\cdot u_{dc}\cdot[\mathbf{m^t}\cdot\mathbf{i}]$). Selon l'expression (S2.14), les courants parallèles sont aussi impliqués dans la dynamique de u_{dc}.

Une méthode simple pour découpler les boucles de courant de la tension DC est d'avoir recours à un découplage temporel, de façon similaire à un bouclage en cascade. Dans cette structure, la boucle de courant doit avoir une dynamique très rapide (au moins 10 fois plus rapide) par rapport à la dynamique de la boucle de tension, comme montré dans la Fig.S2.4.

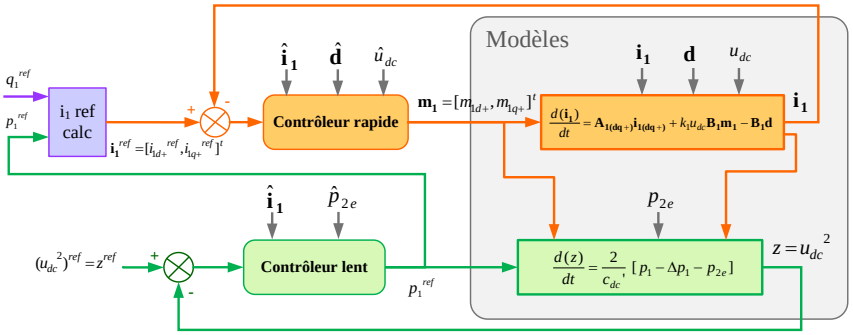


Figure S2.4: Diagramme de la structure de commande parallèle.

Dans cette structure de commande, les lois de commande utilisent des contrôleurs classiques de type PI qui prennent les formes suivantes:

$$\mathbf{m_1}^{ref} = \frac{1}{k_1 u_{dc}}\mathbf{B_1}\left[-\mathbf{k_{p_{i1}}}\boldsymbol{e_{i1}} - \mathbf{k_{i_{i1}}}\int \boldsymbol{e_{i1}}dt - \frac{d\mathbf{i_{i1}}^{ref}}{dt} + \mathbf{A_1}\cdot\mathbf{i_1} + \mathbf{B_1}\cdot\mathbf{v_1}\right] \tag{S2.15}$$

$$p_1{}^{ref} = \frac{c_{dc}{}'}{2}\left(\dot{z}^{ref} + k_{p_z}\varepsilon_z + \frac{k_{p_z}}{T_{i_z}}\int \varepsilon_z dt\right) + \Delta p_1 + p_{2e} \tag{S2.16}$$

La structure de commande du côté shunt a été validée dans des conditions nominales, face aux creux de tension, et face aux erreurs paramétriques.

2. Commande vectorielle orientée à la référence synchrone positive (avec câble)

Le chapitre précédent (Chapitre III.3) porte sur la commande d'un UPLC connecté à une ligne aérienne de type RL. Ce type de lignes est souvent rencontré au niveau du transport. Cependant, dans la distribution, il est fréquent de trouver des câbles. Surtout quand, pour des raisons techniques, esthétiques, ou environnementales, il n'est pas possible de tirer des lignes aériennes.

Dans ce chapitre, quelques particularités de la commande d'un UPLC connecté à un câble sont traitées. Le chapitre est composé de deux parties : une première partie où la commande d'un UPLC connecté à un câble est présentée et une deuxième partie où l'utilisation d'un observateur est examinée.

2.1. Commande d'un UPLC connecté à un câble

Un câble peut être modélisé de façons très différentes en fonction de la précision et du niveau de complexité souhaité. Le modèle peut prendre en compte des paramètres en blocs ou distribués et des paramètres constants ou variables, par exemple. Dans cette étude, le câble est modélisé comme un enchainement de sections de type, comme illustré dans la Fig.S2.5 Pour une longueur de 15 km, 3 sections permettront de représenter proprement des phénomènes fréquentiels jusqu'à 2500 Hz.

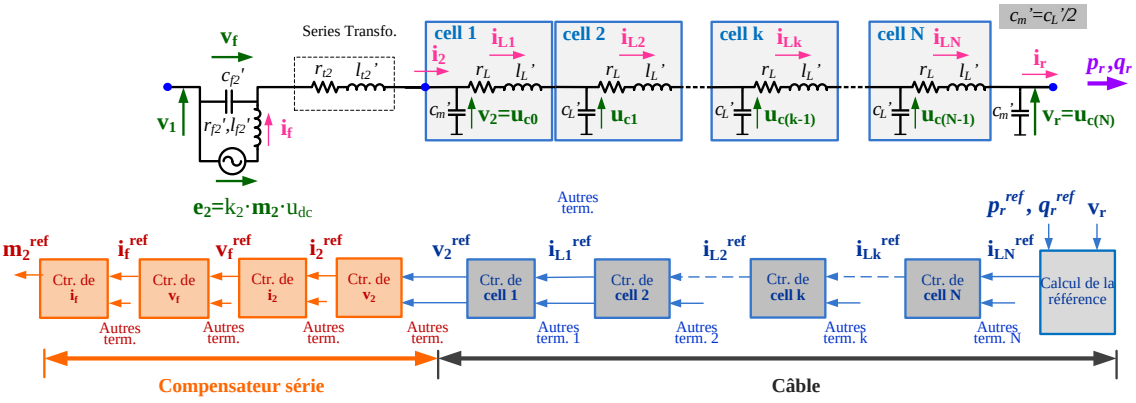


Figure S2.5: Représentation de la commande de la partie série de l'UPLC connecté à un câble de N sections π.

Le modèle de chacune de ces cellules est donné par les expressions suivantes:

$$\frac{d\mathbf{i_{Lk}}}{dt} = \mathbf{A_L}\ \mathbf{i_{Lk}} + \mathbf{B_L}\ \mathbf{u_{c(k-1)}} - \mathbf{B_L}\ \mathbf{u_{ck}} \tag{S2.17}$$

$$\frac{d\mathbf{u_{c(k-1)}}}{dt} = \mathbf{A}(\omega)\ \mathbf{u_{c(k-1)}} + \mathbf{D_L}\ \mathbf{i_{L(k-1)}} - \mathbf{D_L}\ \mathbf{i_{Lk}} \tag{S2.18}$$

Le modèle du câble présente une structure en chaîne qui s'avère très appropriée pour une commande de type Backstepping comme celle présentée dans le chapitre précédent. La structure de

cette commande est représentée dans la Fig.S2.5.

L'expression des lois de commande virtuelles associées au câble de la Fig.S2.5 est:

$$\mathbf{u_{c(k-1)}}^{ref} = \tag{S2.19}$$
$$\mathbf{B_L}^{-1}\left\{\mathbf{k_{u-0}}\ \mathbf{e_{i_{Lk}}} + \mathbf{k_{u-1}}\ sgn\left(\mathbf{e_{i_{Lk}}}\right) + \frac{d\mathbf{i_{Lk}}^{ref}}{dt} - \mathbf{A_L}\ \mathbf{i_{Lk}} + \mathbf{D_L}^{\top}\ \mathbf{e_{u_{c(k-2)}}}\right\} + \mathbf{u_{ck}}$$
$$\mathbf{i_{L(k-1)}}^{ref} = \tag{S2.20}$$
$$\mathbf{D_L}^{-1}\left\{\mathbf{k_{i-0}}\ \mathbf{e_{u_{c(k-1)}}} + \mathbf{k_{i-1}}\ sgn\left(\mathbf{e_{u_{c(k-1)}}}\right) + \frac{d\mathbf{u_{c(k-1)}}^{ref}}{dt} - \mathbf{A_\omega}\ \mathbf{u_{c(k-1)}} + \mathbf{B_L}^{\top}\ \mathbf{e_{i_{L(k)}}}\right\} + \mathbf{i_{Lk}}$$

where $\mathbf{e_{i_{Lk}}} = \mathbf{i_{L(k-1)}}^{ref} - \mathbf{i_{Lk}}$ and $\mathbf{e_{u_{c(k-1)}}} = \mathbf{u_{c(k-1)}}^{ref} - \mathbf{u_{c(k-1)}}$. Ce concept de commande a été validé par des simulations sur Simulink. Il présente un excellent suivi de la référence dans des conditions diverses (nominales et face aux creux de tension). Il faut toutefois préciser qu'il reste encore à vérifier le concept sur SimPowerSystems en utilisant des convertisseurs *réels*. Cette validation est sujette aux problèmes liés aux périodes d'échantillonnage et de commutation des interrupteurs.

2.2. La nécessité d'utiliser un observateur

Dans la pratique, la stratégie de commande présentée ci-dessus, a deux inconvénients principaux:

i) Comme le câble est maillé, il n'est pas possible de mesurer directement les états intermédiaires du câble ($\mathbf{u_{c(k)}}$ et $\mathbf{i_{L(k)}}$).

ii) Il faut mesurer la valeur de la tension et du courant à l'autre bout du câble. Cependant, comme le réseau récepteur se trouve éloigné (dans ce cas à 15 km) il y aura toujours un délai introduit par les capteurs, par le temps de traitement dex signaux, par le temps de propagation etc.

Il est pourtant possible de s'affranchir de ces difficultés grâce aux observateurs. Dans le cadre de cette thèse, un observateur de type Kalman a été choisi comme approche préliminaire. L'observateur de Kalman, aussi connu comme Filtre de Kalman, calcule le gain $\mathbf{K}$ de façon à minimiser la variance de l'erreur d'estimation. Par conséquent, le filtre de Kalman est bien adapté pour travailler dans des systèmes qui présentent des mesures bruitées ou de bruit dans le procédé.

Dans le cas d'un câble connecté à un UPLC, l'estimation de tous les états intermédiaires du câble ainsi que de la tension et du courant au point de réception ($\mathbf{v_r}$ et $\mathbf{v_r}$) est un véritable défi (Fig.S2.6). Des simulations en Simulink ont montré les résultats suivants:

- Dans la première simulation la tension $\mathbf{v_r}$ subit un changement en échelon en même temps que $\mathbf{i_r}$ est modulé. L'observateur est capable d'estimer le changement de $\mathbf{v_r}$ avec un retard inférieur à 1 ms.

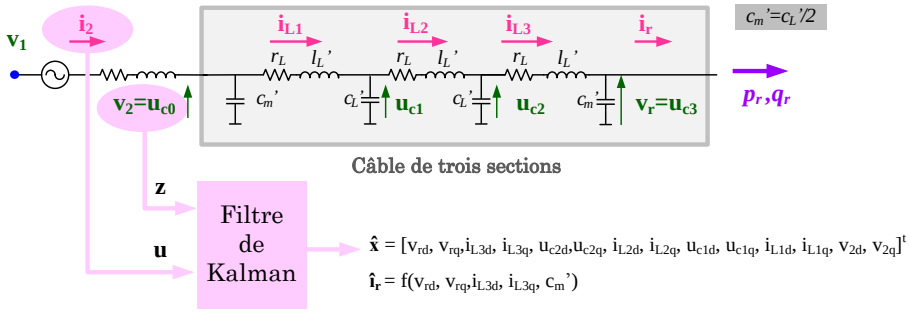


Figure S2.6: Application du filtre de Kalman à un câble de trois sections.

- Dans la deuxième série de simulations les $\mathbf{i_2}$ et $\mathbf{v_2}$ sont bruités. Dans ce cas, si la variance des bruits est bien estimée, l'observateur arrive à bien estimer les variables d'état.
- Enfin, dans la troisième série de simulations, des erreurs paramétriques ont été simulées. Dans ce cas, comme $\mathbf{i_r}$ est estimé en boucle ouverte à partir de $\mathbf{i_{L3}}$, la performance se réduit au fur et à mesure que les erreurs paramétriques augmentent. Cependant, la performance de l'observateur reste acceptable pour des erreurs en dessous de 20 %.

3. Commande de l'UPLC sous un régime déséquilibré

L'opération d'un UPFC sous un régime déséquilibré n'est pas encore traité dans la littérature. Probablement, le fait que le niveau de déséquilibre dans les réseaux de transport soit plus réduit que dans les réseaux de distribution, explique le manque d'études à ce sujet. Cependant, la commande des convertisseurs connectés en parallèle (STATCOMS et HVDC, par exemple) soumis aux tensions déséquilibrées a déjà été abordée par des chercheurs [29, 30, 31, 32, 33]. De ce fait, il est possible de s'inspirer d'études existantes pour proposer des stratégies de commande pour des UPFCs en régime déséquilibré.

3.1. Implications des déséquilibres et différents modes de génération de références

Quand un ensemble de tensions ou de courants contient une séquence négative, l'ensemble est déséquilibré. L'existence d'une séquence négative de tension ou de courant a deux conséquences principales:

- D'un côté, si un système de référence rotatif synchrone est utilisé, les projections des tensions et des courants ne seront plus des valeurs constantes mais des valeurs alternatives avec une fréquence d'oscillation de 2ω.
- D'un autre côté, les puissances (active et réactive) contiendront un terme constant et deux

termes sinusoïdaux (un sinus et un cosinus) comme:

$$\begin{aligned} p(t) &= \bar{p} + \tilde{p}_{2\omega} = \bar{p} + p_{c2} \cdot \cos(2\omega t) + p_{s2} \cdot \sin(2\omega t) \\ q(t) &= \bar{q} + \tilde{q}_{2\omega} = \bar{q} + q_{c2} \cdot \cos(2\omega t) + q_{s2} \cdot \sin(2\omega t) \end{aligned} \tag{S2.21}$$

Dans les cas d'un UPLC, un déséquilibre de tension aura une influence différente en fonction de sa localisation. D'ailleurs, les valeurs des références envoyées aux contrôleurs devront être adaptées au résultat désiré.

Par exemple, quand un déséquilibre de tension se produit en $\mathbf{v_1}$, et que le déséquilibre est compensé par le compensateur série, le déséquilibre aura une répercussion double dans la tension DC. La liaison DC subira des injections/absorptions de puissance active avec une oscillation à double fréquence des deux côtés du bus DC (Fig.S2.7).

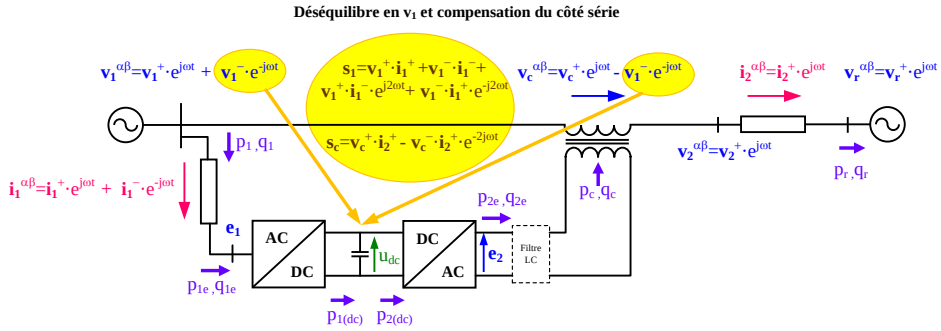


Figure S2.7: Description des variables sous déséquilibre de tension en $\mathbf{v_1}$.

Quand le déséquilibre de tension se produit dans le réseau récepteur ($\mathbf{v_r}$), cela se répercute différemment en fonction de la stratégie de génération de références suivie (Fig.S2.8). Trois possibilités peuvent être envisagées:

a) Garantir une puissance (active et réactive) constante dans le réseau récepteur. Cela implique que les courants pourraient être déséquilibrés.

b) Garantir un courant $\mathbf{i_2}$ équilibré. Cela implique que les puissances P_r et Q_r auraient une composante oscillante.

c) Garantir une puissance série injectée constante. Ceci permet d'extraire une puissance active constante du bus DC. Cette possibilité est compliquée à réaliser.

3.2. Stratégies de commande existantes sous régimes déséquilibrés

Les stratégies existantes peuvent être classifiées en deux grands groupes:

i) **Les stratégies vectorielles.** Et, parmi les stratégies vectorielles (les plus étendues), deux approches peuvent être soulignés:

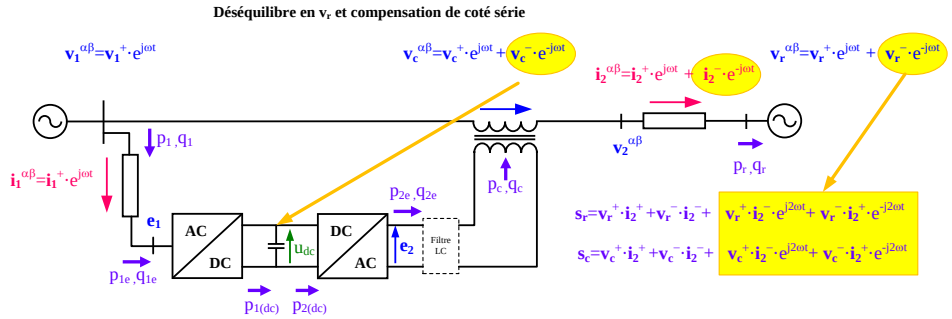


Figure S2.8: Description des variables sous un déséquilibre de tension en $\mathbf{v_r}$.

a.- les stratégies vectorielles qui utilisent des **projections des signaux dans des SRFs** (LIPO),

b.- les stratégies vectorielles qui utilisent les **séquences symétriques instantanées de signaux** (DVCC).

ii) **Les stratégies scalaires.**

Ces méthodes sont brièvement décrites ultérieurement.

- **Stratégies vectorielles utilisant des projections de signaux dans des SRFs (LIPO)**

  Ces types de stratégies utilisent une SRF (positive) ou deux SRFs (positive et négative) et toutes les tensions et les courants sont projetés sur ces références rotatives [34, 30, 29]. Quand les tensions et les courants sont équilibrés, les projections sur les axes d et q sont des valeurs constantes. Si les références sont aussi des valeurs constantes, des contrôleurs classiques de type PI peuvent être utilisés. Cependant, si les tensions ou les courants sont déséquilibrés, ou si les références ne sont pas des valeurs constantes, il faut recourir aux contrôleurs capables de suivre des valeurs alternatives.

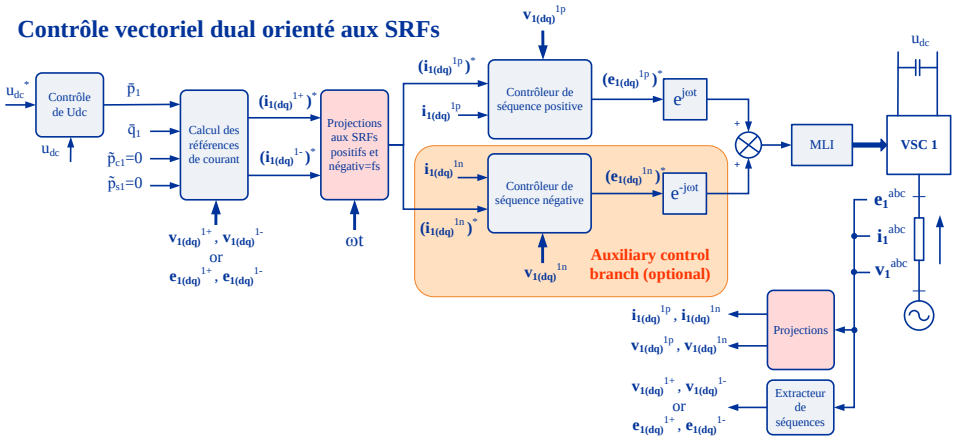


Figure S2.9: Structure de commande duale utilisant des projections des signaux sur une SRF positive et une SRF négative (de [30]).

La Fig.S2.9 montre la structure de contrôle qui utilise les projections de la tension et du courant sur des SRFs. Par la suite cette méthode (Fig.S2.9) sera appelée méthode LIPO.

- **Stratégies vectorielles qui utilisent les séquences symétriques des signaux (DVCC)**

  Une alternative à l'utilisation des projections consiste à extraire la séquence positive et négative des tensions et des courants et à utiliser des boucles de commande séparées pour chaque séquence, comme illustré dans la Fig.S2.10. L'avantage principal de cette stratégie est qu'il n'y a pas besoin de contrôleurs très puissants pour faire le suivi de la référence. Cependant, cette structure présente un inconvénient important: les systèmes d'extraction de séquences induisent un délai considérable (entre 5-20 ms). Par la suite, dans cette thèse, cette méthode (Fig.S2.10) sera appelée DVCC.

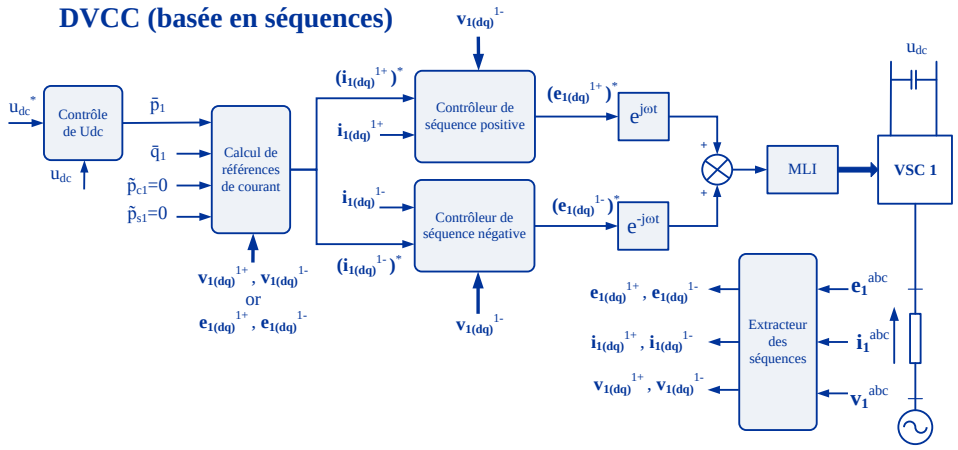


Figure S2.10: Structure de commande duale utilisant des séquences positives et négatives de signaux (de [31]).

- **Stratégies scalaires**

  En comparaison avec les stratégies vectorielles, les stratégies scalaires sont très peu courantes. Elles ne requièrent pas d'extracteurs de séquences mais elles nécessitent des systèmes de synchronisation monophasés (un pour chaque phase), des systèmes d'identification de creux, et des contrôleurs capables de suivre des signaux oscillants [29].

Le Tableau S2.1 schématise les avantages et les désavantages des trois stratégies:

3.3. Comparaison (par simulation) des méthodes vectorielles

Comme complément au Tableau S2.1, les méthodes vectorielles (LIP0 et DVCC) ont été comparées sur SimPowerSystems pour un convertisseur connecté en parallèle avec le réseau ($F_{sw} = 4950\ Hz$ et $T_s = 10\ \mu s$). Pour les simulations, trois cas ont été comparés : (i) un cas avec des valeurs nominales et $\mathbf{v_1}$ équilibré, (ii) un cas avec un déséquilibre constant de 0.2 pu en $\mathbf{v_1}$, et (iii) un cas avec un creux de tension de type D.

Table S2.1: Comparaison de stratégies de commande pour des systèmes déséquilibrés.

Structure de commande	Avantages	Désavantages
Utilisation des projections de **v** et **i** sur les SRFs (LIPO)	• Les séquences de la tension sont seulement nécessaires pour le calcul de la référence (et pas toujours).	• Besoin de contrôleurs capables de suivre des signaux alternatifs. • Besoin des systèmes de synchronisation pour les SRFs.
Utilisation des séquences positives et négatives indépendamment (DVCC)	• Des contrôleurs capables de suivre des signaux alternatifs ne sont pas nécessaires. • Chaque séquence est contrôlée indépendamment.	• Besoin d'extracteurs de séquences. • Besoin d'autant de boucles de contrôle que de composantes/séquences principales dans le réseau. • Besoin de systèmes de synchronisation.
Contrôle scalaire	• L'extraction de séquences n'est pas nécessaire.	• Besoin de contrôleurs capables de suivre des signaux alternatifs. • Besoin d'un bloc d'identification de perturbations. • Besoin de systèmes de synchronisation (pour chaque phase).

D'après les simulations, les deux méthodes, la méthode LIPO et la méthode DVCC, sont équivalentes dans des conditions idéales. C'est-à-dire, quand les séquences symétriques sont instantanément connues (pour le cas DVCC) et quand les contrôleurs peuvent suivre fidèlement les consignes alternatives (pour le cas de LIPO).

3.4. Limites des contrôleurs de type $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$ pour l'utilisation dans des structures projetées sur un SRF positive

En présence de déséquilibres, les contrôleurs de type PI ne sont plus adaptés dans les structures qui utilisent les projections des signaux sur des SRFs. Et, dans la littérature, des contrôleurs résonants ont été ajoutés aux PIs [30, 29] afin d'assurer le suivi des références alternatives.

Cependant, en vue de la puissance théorique des contrôleurs de type $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$ présentés dans le Chapitre III.3, ce type de contrôleurs a été testé pour la commande d'un UPLC connecté à une ligne RL en présence de déséquilibres (utilisant la méthode de LIPO).

Les simulations ont démontré que, les contrôleurs de type $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$ sont seulement acceptables si les périodes d'échantillonnage et de la MLI sont très réduites (en dessous de 100 μs). Il a été prouvé que les gains des contrôleurs peuvent être augmentés si le modèle de simulation discret se rapproche de sa version continue. Dans ce cas, ils pourraient être utilisés pour des régimes déséquilibrés. L'amélioration de ce désagrément se trouve dans les axes d'amélioration de la thèse.

3.5. Simulation d'un UPLC connecté à un câble utilisant une structure duale basée sur l'extraction de séquences

Dans la section précédente il a été observé que, sous un régime déséquilibré, les contrôleurs de type $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$ ne sont pas valables dans les structures orientés dans les SRFs (sauf si les temps d'échantillonnage sont réduits). La raison réside dans le fait qu'il n'est pas possible d'augmenter les gains des contrôleurs sans provoquer de *chattering* ou sans avoir des erreurs statiques de suivi.

Cependant, il est toujours possible d'utiliser la structure de commande globale de génération de trajectoires introduite dans le Chapitre III.4 si une structure duale basée sur l'extraction des séquences est utilisée. Cette structure, qui est illustrée dans la Fig.S2.11, permet d'utiliser des gains inférieurs et d'assurer le suivi de toutes les références virtuelles intermédiaires.

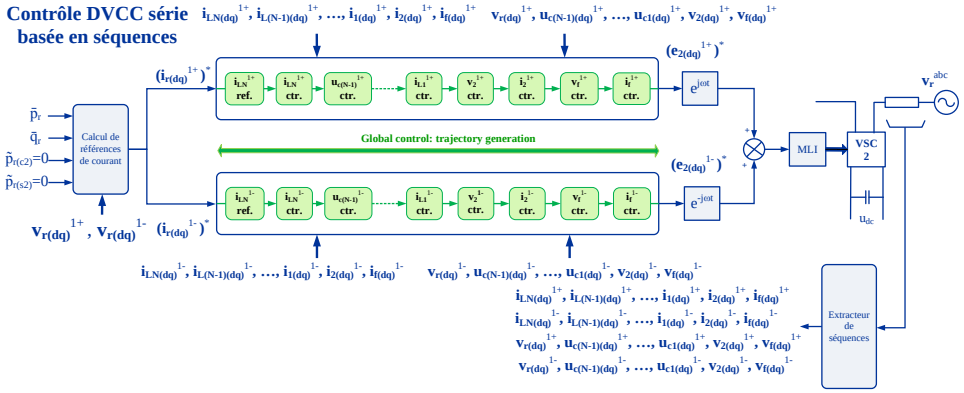


Figure S2.11: Structure de commande de la partie série utilisant la méthode DVCC.

Les simulations ont prouvé que cette structure duale présente des résultats satisfaisants dans des conditions *idéales*. C'est-à dire, quand les convertisseurs sont modélisés selon le modèle moyenné, les périodes d'échantillonnage sont courtes (de l'ordre de la μs), et les extracteurs de séquences sont instantanés.

Le résultat obtenu est un très bon résultat préliminaire. Cependant, il faudra éventuellement améliorer les contrôleurs afin de pouvoir se rapprocher des conditions plus réelles.

4. Méthodes de synchronisation et d'extraction des séquences. Comparaison.

Toutes les stratégies de commande précédentes sont basées sur l'hypothèse que les méthodes de synchronisation et d'extraction de séquences sont idéales, c'est à dire instantanées et totalement fiables. L'objectif de ce chapitre est de dévoiler les vraies caractéristiques des méthodes de synchronisation et d'extraction de séquences. Pour cela, une revue qui comprend les méthodes de synchronisation et d'extraction de séquences les plus importantes a été réalisée en premier (présen-

tée schématiquement dans la Fig.S2.12). Cette revue a permis de comprendre les méthodes de synchronisation et d'extraction de séquences et de sélectionner les méthodes les plus intéressantes de par leur simplicité, leur rapidité, leur robustesse face aux perturbations (harmoniques, creux de tension, variations de fréquence...), le nombre d'opérations du microprocesseur et leur précision. Il faut préciser que, comme les méthodes de synchronisation cherchent à trouver l'angle de la séquence positive du signal d'entrée, beaucoup des méthodes de synchronisation servent aussi à extraire les séquences symétriques, mais pas toutes.

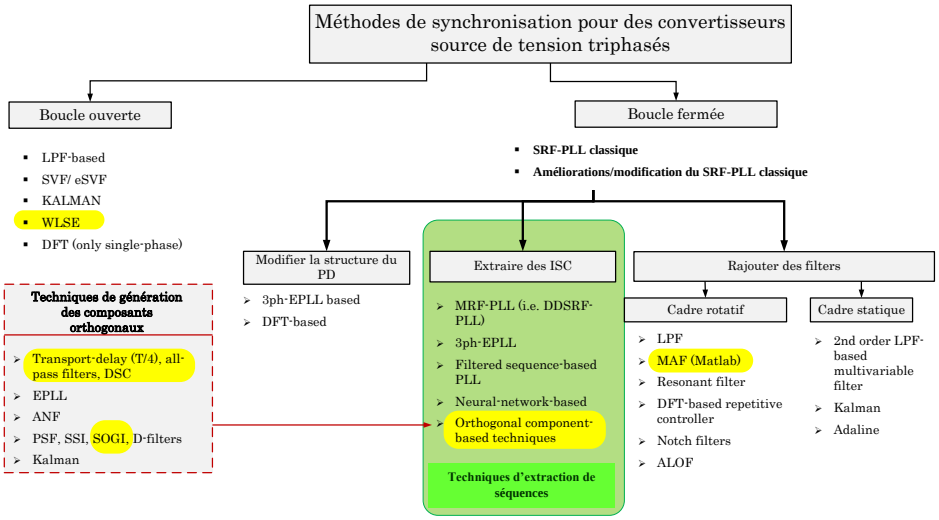


Figure S2.12: Classification of synchronization methods for three-phase VSC.

4.1. Comparaison de quatre techniques d'extraction de séquences

Dans cette thèse, quatre techniques d'extraction de séquences ont été sélectionnées pour réaliser une comparaison entre elles:

- La **PLL proposée par Matlab/SimPowerSystems (mPLL)**. Il s'agit fondamentalement d'une PLL classique qui a un filtre MAF (Moving Average Filter) à la sortie de la transformée de Park.
- L'algorithm **WLSE** (Weighted Least Square Estimation).
- La méthode **DSOGI-FLL** (Double Second Order Generalized Integrator - Frequency Locked Loop) et,
- La méthode **DSC** (Delayed Signal Cancellation).

Les descriptions de ces méthodes sont fournies dans le manuscrit principal. Après plusieurs simulations, les quatre méthodes ont été classifiées dans le Tableau S2.2. Comme il peut être observé, il n'est pas possible de déterminer une méthode optimale parce que toutes les méthodes

présentent des avantages et des inconvénients. Néanmoins, pour la conception de la structure de commande il faut toujours compter avec un délai minimum de 5 ms pour les cas les plus idéaux. Dans le cas d'un réseau perturbé il faut considérer un délai minimum de 20 ms.

Table S2.2: Tableau comparatif d'extracteurs de séquences.

Aspects	Double m-PLL	DSOGI-FLL	WLSE	DSC
Nb. de paramètres	2	2	3	0
Temps de convergence (conditions idéales)	20 ms (avec filtre)	$\approx$ 10 ms (sans filtre)	$\approx$ 10 ms (sans filtre)	5 ms (sans filtre)
Temps de convergence (conditions perturbées)	• Sans filtre: - • Avec filtre: 20 ms	• Sans filtre: $\geq$ 100 ms • Avec filtre: $\approx$ 30 ms	• Sans filtre: $\geq$ 100 ms • Avec filtre: $\approx$ 30 ms	• Sans filtre: - • Avec filtre: 20 ms
Précision des estimations	DÉFICIENTE (oscillations)	• BONNE sans filtre (sensible à Δf) • DÉFICIENTE avec filtre (erreurs d'estimation)	BONNE	BONNE (mais sensible à Δf)
Estimation de fréquence	Intégrée	Intégrée	Pas intégrée (possible)	Pas intégrée (possible)
Implémentation	A besoin d'un nombre d'échantillons intégral dans une période (peut être résolu)	-	-	A besoin d'un nombre d'échantillons intégral dans une période (peut être résolu)

Conclusions

L'UPLC est un appareil complexe qui est amené à être intégré dans un système électrique complexe. Par conséquent, avant de se décider pour l'implantation d'un tel dispositif électronique, il est extrêmement important d'étudier l'intérêt de l'installer, d'analyser toutes les conditions possibles auxquelles il pourrait être confronté, d'évaluer la structure de commande la plus appropriée, de réaliser un pré-dimensionnement raisonnable, et de vérifier que la structure de commande proposée, conjointement au dimensionnement, est capable d'assurer un fonctionnement satisfaisant sous des régimes nominaux et dégradés.

Le nombre d'articles scientifiques publiés est très important (plus d'une centaine d'articles qui traitent de l'UPFC et de l'UPQC ont été repérés). Mais, paradoxalement, seul trois UPFC ont été installés dans le monde. Le cas de l'UPQC est analogue: seul une société productrice d'UPQCs existe. Ce nombre très limité de cas réels suggère qu'il existent des barrières empêchant l'installation massive d'UPFCs et d'UPQCs. Un des objectifs principaux de cette thèse a été d'offrir une vision critique sur l'intérêt réel d'utiliser un UPLC pour l'interconnexion des réseaux de distribution en MT.

Suite au travail réalisé, les conclusions et perspectives de travail futur peuvent être mise en valeur:

- A propos de la **multifonctionnalité de l'UPLC**, les conclusions suivantes peuvent être énoncées :

  i) Comme l'UPLC est censé interconnecter deux réseaux de distribution, **la fonction principale de l'UPLC doit être le contrôle de flux de puissance**.

  ii) **En second lieu, il est conseillé de contrôler $\mathbf{v_1}$ (en régime permanent)** dans une plage de valeurs définie par les normes en vigueur, équilibrée, et libre d'harmoniques. La régulation *active* de la tension au point PCC ne sera possible que si la taille du compensateur parallèle reste abordable. D'ailleurs, si la puissance du compensateur parallèle augmente, la fréquence de commutation devra être réduite, limitant la capacité de filtrage harmonique de l'appareil.

  iii) D'autre part, l'UPLC permet aussi la compensation d'autres types de perturbations mais, en fonction de la magnitude et de la nature de la perturbation, **la compensation des problèmes liés à la qualité de l'énergie et, en même temps, le contrôle des flux de puissance peut se réveler peu intéressant**. Par exemple, pour compenser des creux de tension avec le compensateur série, la capacité d'injection de tension du compensateur série doit être augmentée. Cela implique qu'en régime nominal, les convertisseurs travailleront à un indice de modulation très bas qui demandera l'installation des filtres importants. Quand les points d'opération divergent notablement (comme c'est le cas des

creux de tension), la complexité de l'appareil et sa conception augmentent. Dans ce cas, l'appareil doit être surdimensionné pour pouvoir être utilisé occasionnellement.

iv) En ce qui concerne la **compensation des phénomènes liés à la qualité de l'énergie en régime permanent**, deux aspects doivent être considérés:

- La taille des convertisseurs augmente d'un ratio $\sqrt{1+THD_x{}^2}$, pour la compensation d'harmoniques de tension/courant et de $\sqrt{1+(X^-/X^+)^2}$, pour la compensation des déséquilibres de tension/courant.
- La puissance du convertisseur ne doit pas dépasser un seuil de quelques MWs afin de pouvoir compenser des harmoniques d'ordre élevé. Par exemple, les filtres actifs connectés à la MT présentent des fréquences de découpage équivalentes de 1 kHz à 5 kHz pour des puissances de quelques MWs. Ces fréquences de découpage sont seulement possibles si des topologies multiniveaux sont utilisées.

v) Finalement, à l'écart des considérations purement techniques, **il est aussi important d'évaluer le côté contractuel** vis-à-vis d'une possible installation d'un UPLC. Dans le cas où il y aura plusieurs départs au même PCC, il faut évaluer qui prendra en charge un appareil multi-fonctions connecté à un bus PCC commun et si, il est prêt à payer pour un tel service.

- Par rapport au **dimensionnement et à la conception de l'UPLC** il est important d'indiquer que les dimensions, les types de composants, les topologies et l'architecture d'un UPLC dépendent énormement des fonctions qui veulent être réalisées, de l'endroit où l'appareil va être installé et des conditions auxquelles l'appareil sera confronté. Dans ce travail une procedure de dimensionnement basique est décrite en soulignant les points qui doivent être adaptés dans chaque cas.

- Par rapport aux **structures de commande de l'UPLC adaptées aux environments perturbés**, les points suivants peuvent être évoqués:

  - La structure de commande proposée (qui consiste en une **stratégie de génération de trajectoires couplées à des contrôleurs de type** $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$) se révèle être une bonne technique de régulation sous conditions idéales (sources de tension moyennées et petites périodes d'échantillonnage). Mais, quand la période d'échantillonnage est augmentée à plus de $1-10\mu s$ ou quand le découpage des convertisseurs est pris en compte, il a été constaté qu'il n'est pas possible d'augmenter les gains des contrôleurs au-delà d'un plafond sans subir du *chattering* ou sans avoir une erreur statique de suivi. Pour éviter le *chattering* la fonction *signum* a été remplacée par une fonction lissante similaire à la fonction saturation qui peut être modulée par le paramètre δ. L'utilisation de cette fonction permet d'augmenter les gains en détriment de l'erreur de suivi, qui se manifestera. Et, comme les contrôleurs locaux sont enchainés, cette erreur de suivi entraînera une mauvaise performance de la chaîne de commande globale.

    L'augmentation des gains des contrôleurs est normalement nécessaire quand le système

est déséquilibré et une structure de commande orientée vers les SRF peut être utilisée. Dans ces cas, si les gains ne sont pas augmentés, les contrôleurs ne peuvent pas garantir un bon suivi de la référence. Ainsi, la seule solution disponible pour contourner le problème est de réduire la période d'échantillonnage. Mais, cette solution n'est pas toujours possible.

- L'analyse des structures de commande vectorielle pour des conditions déséquilibrées (l'une orientée vers les SRFs et l'autre basée sur l'extraction des séquences symétriques instantanées) a montré que, si les contrôleurs et les systèmes de mesure sont idéaux, les deux structures étudiées sont équivalentes. Cependant, dans la réalité:

  - **Les structures qui utilisent les projections des tensions et des courants sur des SRFs (simples ou duales) nécessitent des contrôleurs capables de suivre des références oscillantes.** Dans la littérature, des contrôleurs de type résonant ont été proposés pour cet objectif. Le seul problème des contrôleurs résonants est qu'il faut qu'ils s'adaptent en fonction des variations de fréquence. Comme alternative aux contrôleurs résonants, dans cette thèse des contrôleurs de type $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$ ont été proposés mais, il faudra encore améliorer leurs performances afin qu'ils puissent être utilisés dans des environnements discrets. Si ces contrôleurs sont optimisés pour travailler en discret ils constitueraient une option très intéressante.

  - **Les structures duales qui utilisent les séquences symétriques instantanées des tensions et des courants,** ne requièrent pas de contrôleurs spécialement puissants mais des méthodes d'extraction de séquences très rapides et fiables. Comme il a pu être vérifié dans le Chapitre III.6, la méthode plus rapide qui existe, la DSC, a un retard de 5 ms quand les signaux sont équilibrés et sans harmoniques. Si le réseau est très perturbé (comprenant des variations de fréquence), l'extraction de séquences prendra un minimum de 30 ms.

    En résumé, pour pouvoir utiliser des structures de commande basées sur des séquences symétriques, il faut intégrer les retards des extracteurs de séquences dans la conception de la commande.

- La **comparaison entre un UPLC et un MVDC** a démontrée que, en règle générale, le MVDC présente plus d'avantages que l'UPLC. Cependant, sous quelques conditions particulières (i.e. une différence de phase faible ($< 60°$) entre les deux réseaux interconnectés) les dimensions de l'UPLC peuvent être substantiellement reduites (en fonction de la différence d'angle) par rapport au MVDC. En conséquence, l'avantage majeur de l'UPLC par rapport au MVDC résiderait dans sa taille. Un deuxième avantage de l'UPLC par rapport au MVDC réside dans la possibilité de pouvoir le court-circuiter.

Perspectives et travaux futurs

- **Association des différentes fonctions.**

  Du fait que l'association des fonctions *contrôle de flux* et *amélioration de la qualité de l'énergie* ne semble pas être économiquement intéressant dû au surdimensionnement de l'appareil nécessaire, ce travail a été principalement axé sur le contrôle du flux de l'UPLC.

  Cependant, en s'abstrayant des intérêts purement économiques, une conception et une commande de l'UPLC capable de satisfaire tous ces objectifs peut être envisagée dans un travail futur. Par exemple, ce travail pourrait s'orienter vers l'analyse de topologies des convertisseurs avancées (type multiniveaux) et des filtres associés. Bien évidemment, la commande rapprochée de ces structures et les stratégies de compensation devraient aussi être étudiées et implémentées.

  Par ailleurs, il pourrait être très intéressant de rencontrer tout les acteurs possiblement impliqués dans un tel projet (consommateurs pollueurs, opérateurs de réseaux, distributeurs etc.) afin d'éclaircir l'intérêt d'installer un UPLC pour l'interconnexion des réseaux de distribution.

- **Conception et dimensionnement de l'UPLC.**

  L'UPLC est un appareil complexe, sa conception et son dimensionnement dépendent des fonctions spécifiées, de la performance souhaitée et des conditions auxquelles l'appareil sera confronté. Ainsi, il y a plusieurs aspects qui peuvent être encore approfondis et analysés. Entre autres:

  - L'étude d'une structure constituée de trois UPLCs monophasés. Cette structure permettrait de contrôler chaque phase indépendemment.
  - La substitution du filtre parallèle en L par un filtre LCL et son dimensionnement associé.
  - L'analyse des characteristiques du transformateur série.
  - L'analyse (topologie, calcul de pertes, choix de type d'interrupteurs, type de refroidissement, volume, prix etc.) des convertisseurs.
  - L'étude du disjoncteur de bypass série (commande et dimensionnement).
  - L'étude de protections de l'appareil.
  - L'évaluation globale du prix et du volume de l'appareil.

- **Structure de commande de l'UPLC.**

  - Le dévéloppemment des modèles discrets pourront être envisagés afin d'améliorer des contrôleurs de type $C(\mathbf{e}) = k_1 + k_2 sign(\mathbf{e})$ et pouvoir travailler dans un environnement

discret. En outre, les retards introduits par les méthodes d'extraction de séquences devront être intégrés dans la synthèse des régulateurs.

- Dans cette thèse la modélisation et la commande de l'UPLC a été réalisée en utilisant des coordonnés rotatives dq. Le principal avantage d'utiliser des coordonnées en dq est que, quand le système est parfaitement équilibré, les projections de tensions et de courants dans le SRF sont constantes, de sorte que les contrôleurs doivent seulement s'occuper des signaux constants. Cependant, il faut mentionner que la précision et la robustesse de la méthode de synchronisation sélectionnée aura une influence conséquente dans la précision des projections dq.

  Ainsi, comme perspective de travail futur, **l'utilisation d'un cadre statique $\alpha\beta$ de travail est proposée**. L'avantage de travailler dans les coordonnées $\alpha\beta$ est que les méthodes de synchronisation pour synthétiser les signaux de retour ne sont pas nécessaires. Naturellement, des méthodes de synchronisation et d'extraction de séquences seront nécessaires pour générer des références appropriées dans des conditions perturbées.

- L'amélioration des oscillations du bus DC dans des conditions déséquilibrées est un autre aspect qu'il faudra réexaminer dans des travaux futurs. Dans cette thèse des méthodes de minimisation des oscillations de bus *classiques*, utilisées dans les actionneurs électriques (drives) ont été testées. Cependant, dans ces méthodes la puissance active demandée par la charge est plutôt constante, tandis que, dans l'UPLC la puissance active demandée par le compensateur série a une composante oscillante à 2ω.

- Il pourrait également être très intéressant d'élargir les travaux existants (i.e comparaisons) autour des méthodes de synchronisation et d'extraction des séquences à un spectre plus large de solutions.

- **Simulations.**

  La taille de l'UPLC dépend de plusieurs facteurs, parmi lesquels se trouve la différence d'angle (angle de transport) entre les deux réseaux qui vont être reliés. Ainsi, pour évaluer la faisabilité de l'installation d'un UPLC, il est indispensable de réaliser des simulations dynamiques qui serviront à estimer les changements de l'angle de transport dans un large spectre de situations. Ceci dit, il faut préciser que, pour réaliser des simulations dynamiques de systèmes électriques comportant de l'électronique de puissance, il faut des outils puissants de simulation en temps réel qui coûtent chers et ne sont pas toujours facilement disponibles.

  En ce qui concerne les simulations dynamiques d'un UPLC intégré dans un système électrique, il est aussi important de développer des algorithmes au niveau amont (distribués ou centralisés) qui fourniront des références de puissance, tension etc. aux UPLC et aux autres appareils électroniques du réseau. Ces algorithmes pourraient être basés sur l'optimisation des différents paramètres. Par exemple, la minimisation des déviations de tension, la minimisation des pertes, la prévention de la saturation des transformateurs et des lignes etc.

- **Comparaison entre l'UPLC et le MVDC.**

  Dans ce travail, la comparaison de la taille d'un UPLC et d'un MVDC a été réalisée en comparant la puissance active qui traverse le bus DC de chaque appareil en conditions égales. Même si la puissance active qui transite par le bus DC donne une idée assez représentative de la taille de l'appareil, elle n'est qu'un indicateur. Pour cette raison, il serait intéressant d'étendre la comparaison en considérant le prix, le volume et les spécifités des composants. Par exemple, des éléments comme l'interrupteur de bypass ou le transformateur série pourraient augmenter le côut de l'UPLC et devraient être inclus dans le calcul final du prix et du volume de l'UPLC.

Part I

General Introduction

Context and Objectives

Chapter I.1

Towards Smartgrids

A large percentage of the electrical systems of industrialized countries (specially in Europe and in USA) where built about half a century ago and they are now ageing [2]. As a consequence, if the efficiency and reliability of the power system is to be guaranteed, the existing assets will need to be progressively updated or replaced.

When the current electrical networks were originally designed, their architecture and operation was based on a vertical and bundled structure where, region by region, a single utility owned and managed the generation, the transmission, and the distribution (see Fig.I.1.1(a)). The present electric power system was therefore build following a set of specifications that are now becoming out-of-date.

The main characteristics of the former (but still prevailing) electric power system are:

- Large-capacity power plants are in charge of generating the bulk power that is consumed by load-centers.
- In order to minimize losses, power is transmitted at high voltages through the transmission network. Transmission grids are usually meshed and buses are monitored and controlled in order to provide a stable operation of the whole system.
- Finally, distribution networks are in charge of suppling electrical power from the transmission level directly to the loads, and their main role is to accomodate the voltage to consumption levels. In contrast with transmission grids, distribution grids are not actively controlled (and neither monitored) and their structure is often radial or open-looped.

For the last decades, emerging changes and developments are leading to a new paradigm of electricity networks, also known as *Smartgrids* [3, 4]. Even if the the structure and operation of *Smartgrids* is still to be defined, the following lines gather some important trends that have been identified and highlights the most characteristic features of the *Smartgrids* of the future: flexibility, accessibility, reliability, and cost-efficiency.

- **Flexibility.**

  In many countries of the world, the electricity sector has been deregulated and the vertical structure of utilities has been unbundled (Fig.I.1.1(b)). This means that, any player can take part into the electricity business (as generator, consumer, aggregator, retailer or others) and

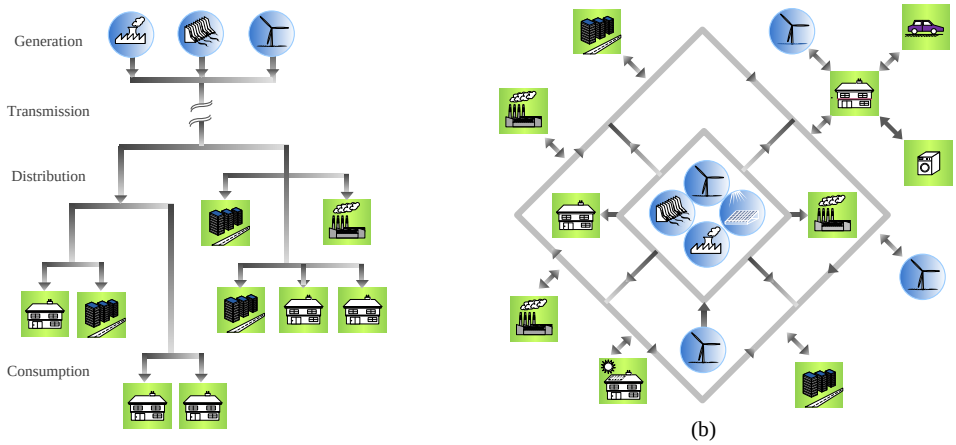


Figure I.1.1: (a) Vertical structure of a electrical power system, (b) Possible structure of the future power system.

that inter-regional energy trading is now possible. Moreover, new alternatives to stimulate active participation of loads, such as demand-side management, are being studied and fostered.

Thus, the electrical grid of the future must be **flexible** to accomodate to these changes and to be able to assimilate the upcoming challenges.

- **Accessibility.**

  Following the need of reducing green-house gas emissions, generation technologies based on renewable energies are priorized by a vast majority of governmental policies (at least in industrialized countries). Unfortunately, renewable energy sources are often distant from consumption zones and thus, the produced energy needs to be consumed locally or transmitted over large distances. Offshore windfarms constitute an emblematic example of such situations. Additionaly, the intermittency of renewable energy sources makes the dispatch of these sources more complex.

  The electrical grid of the future needs therefore to be **accessible** to every network users, granting them connection access in a broad range of conditions.

- **Reliability.**

  In modern electric power systems the penetration of distributed generation (DG) is increasingly growing. DG is generally connected to the distribution level and it is usually of renewable origin, presenting the typical problems associated to renewable sources (i.e. intermittency, grid-code compliance, instability, etc.). On the other hand, in such a complex system information and communication technologies (TICs) will have a very relevant role, providing a link between the high level control layer of the system and the lowest level physical layer.

  The electrical grid of the future needs to be **reliable**, assuring and improving security and quality of supply, consistent with the demands of the digital age with resilience to hazards (e.g. cybernetic incursions) and uncertainties.

- **Cost-efficiency.**

  Finally, the electricity grid of the future needs to be **economic**, providing best value through innovation, efficient energy management, competition and regulation.

Such a high-level characterization of *Smartgrids*, while helpful at the strategic level, leaves plenty of room for confusion and interpretations [3]. It is therefore essential that research, development and deployment takes place in a coherent way that addresses technical, commercial and regulatory issues [4]. If nothing is done, without a deep reflection and a clear action plan, this renewal will become a bare replacement programme, based on obsolete technologies.

Under the new paradigm of the electrical power system, changes will be experienced at all the layers (see Fig.I.1.2) and at all the physical levels (i.e. transmission and distribution). But many changes will be specially observed at the distribution level, which was designed according to a *fit-and-forget* approach, with radial topologies and uni-directional power flows. Distributed generation, storage, demand response, advanced metering infrastructures, distribution automation, two-way power flow, and enhancement of power quality, for example, represent some of the subjects that will require further investment in research and development activities [5].

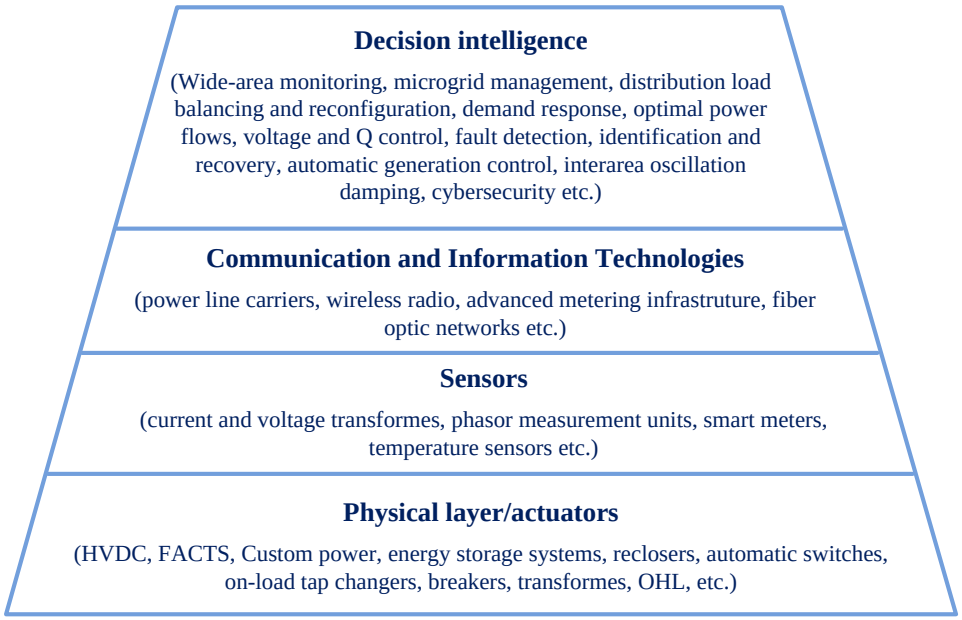


Figure I.1.2: Smartgrid layers (from [3]).

This PhD is inscribed in the frame of *Smartgrids* and specially focuses on **smart distribution grids**. In order to portray the context and introduce the objectives of this PhD (in Chapter I.3), the next chapter (Chapter I.2) describes the structure of actual distribution grids and discusses the most relevant challenges that will need to be faced in the transition towards the distribution grids of the future.

Chapter I.2

Present and future distribution networks

In the traditional power network paradigm, the role of distribution grids is merely passive, with unidirectional power flows, "simple" protection systems and a low level of automation. However, this paradigm is about to change due to governmental directives that encourage a large scale penetration of renewable-origin DG and the use of load management techniques. In the context of smartgrids, distribution grids will become more active, more secure, with better quality levels, multidirectional power flows, and complex control and protection systems. The objective of the current chapter is to provide a clear overview on the distribution grids of today, to introduce the challenges that are presented ahead, and to highlight some of the solutions that are foreseen to overcome these shortcomings.

The chapter begins with a general description of the traditional electric power system and continues with a more comprehensive development of distribution grids, where characteristics and architectures of present distribution grids are explained. The impacts of DG in distribution grids are discussed next, finishing with a list of solutions to a large penetration of DG in distribution.

One of the proposed solutions, that consists in meshing distribution networks, seems to be a good alternative to alleviate the problems related to DG penetration. The advantages and drawbacks that this solution presents are also dealed with, knowing that, the hypothesis of an interconnected distribution network is at the heart of this PhD.

1. The electrical grid of today

The structure of the electrical grid of today is the result of a rapid industrialization, technological disponibility, and a series of historical events. The first electrical distribution system, which was developped and promoted by Thomas Edison in the 1880's, was a DC system. By that time, efficient DC transformers did not exist and DC sources had to adapt their voltage level to each dedicated use: lighting systems and DC motors, at that time. Moreover, in order to avoid losses in cables, sources had to be located near consumption zones. George Westinghouse, a smart business man, identified the potential of some contemporary inventions such as polyphasic machines (by Nicola Tesla) and AC transformers (by Lucien Gaulard and John Dixon Gibbs) for AC transmission and bought the patents. The opposed positions of Edison and Westinghouse regarding DC or AC distribution ended in an open debate called *the battle of currents*. The settlement of the conflict is well known today, as the approach of Westinghouse has been predominant over the years. The reason of the success of AC was that AC transformers provide the flexibility of adapting any voltage levels of the electrical

power. This fact is essential when power is transmitted over long distances (which is often the case) because resistive losses in lines and cables are proportional to the square of the flowing current. Thus, for the same transmitted power, if voltage is increased, current decreases and resistive losses reduce as a result.

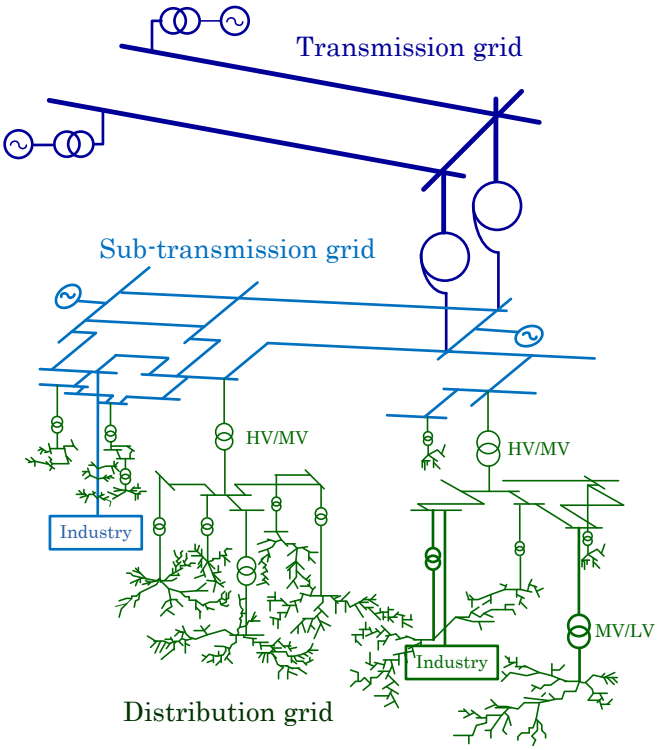


Figure I.2.1: Structure of the electrical grid (from [6])

It is therefore pretty clever to increase the level of the voltage for transmitting it to far-away consumption centers and then, lower it progressively until reaching the voltage required at power demand areas. Following this reasoning, the structure of the traditional electrical grid has been hierarchized in the following levels (Fig.I.2.1):

- **The transmission network**. Transmission networks ensure bulk power delivery from large power plants to main demand zones by means of a meshed grid operated at high voltage levels (150-800 kV). In France the transmission network is operated at 400 kV and 225 kV but ultra-high-voltage (UHV) levels of up to 1000 kV are being deployed in countries such as China, where electrical demand is increasing at astonishing rates. The transmission and sub-transmission networks have a centralized control with a basic data network.
- **The sub-transmission network**. It is an intermediate level between the transmission network and the distribution network that operates at voltage levels between 30 kV and 150 kV. In France the sub-transmission network operates at 90 kV and 63 kV.
- **The distribution network**. The distribution network is a passive termination of the sub-

transmission grid that is in charge of delivering power directly to the customers (except for very big customers that are directly connected to the sub-transmission network). The distribution network is further divided into two categories [1]:

- **the medium-voltage grid (MV)**, with voltage levels higher than 1 kV, and
- **the low-voltage (LV)** grid, with voltage levels lower than 1 kV.

As it is observed in Fig.I.2.1, the traditional electrical grid has a vertical structure where sources of power are centralized, power flows are predictable (downhill) and they are managed and controlled by system operators.

Transmission and sub-transmission networks are usually meshed in order to form a large power pool that increases reliability and security of supply (Fig.I.2.2). Since every bus is supplied by different lines, the loss of just one line would not produce an outage (if n-1 criteria is used, for example). However, interconnected networks do also contribute to higher fault currents and their control and protection systems are more complex than those of simple radial networks. Due to its meshed topology, automation technology is more present in transmission networks than in distribution networks. Still, in the frame of Smartgrids, there are many key developpments such as advanced control devices (FACTS, HVDC and storage), advanced protection, advanced sensing and measurement devices, and improved interfaces and decision support that will need to be developped. [5].

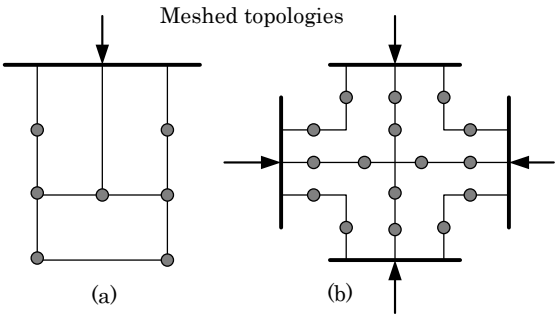


Figure I.2.2: Common transmission network topologies

Distribution networks are passive-ends of sub-transmission grids. Traditionally, little online monitoring and automated-control of distribution networks has been done, although this scenario is changing. This conventionally *fit-and-forget* approach, with a low level of automation, can be explained as follows:

- **The extent of distribution networks.** Just in Europe, more than 5.000.000 km of MV and LV lines exist, in opposition to 230.000 km of transmission lines [2]. The huge proportions of distribution assets imply that

1. voltage ranges and denominations vary from country to country

  - it is very expensive to equip the whole distribution system with measuring devices and remote-controlled actuators,
  - a large, hazard-proven and efficient communication system is needed, together with rather powerful decision-making tools.

- **The power quality of customers.** According to the development level of a country, different relevance is confered to the power quality of customers. In this way, industrialized countries are more careful with outage rates and they include redundancy schemes in critical zones. Switches in redundant systems may be remotely or manually operated.
- **Unidirectional power flows**. Unidirectional power flows make the operation and the protection of distribution network relatively simple, without the need of a very active actuation. However, with the advent of distributed generation, the traditional distribution scheme needs to be revisioned.

2. MV distribution grid architectures [6]

Historically there has always been a considerable difference between rural and urban distribution grid layouts. In France, for example, until late 80's rural distribution grids were purely radial and used OHLs. Moreover, double derivations where not systematically accounted for (see Fig.I.2.3 for understanding the main radial and looped configurations). At the beginning of 90's utilities became aware of the importance of increasing power quality and established new structural changes for rural distribution networks. The main adopted changes were based on (i) shortening the average distance of feeders (to about 35 km), (ii) using underground cables in the departs of the substations to reduce failure rates due to atmospheric phenomena, and (iii) defining looped configurations.

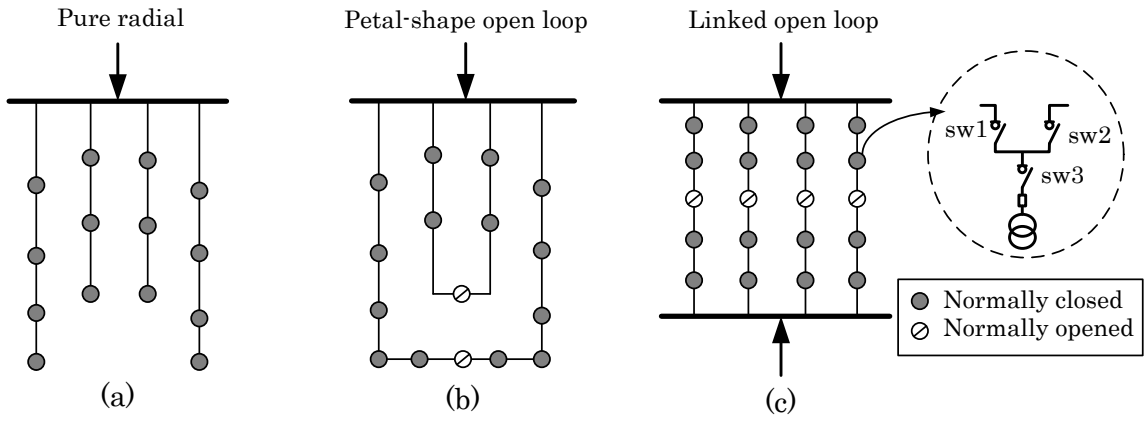


Figure I.2.3: Radial and looped distribution grid architectures

Urban and highly populated areas are mostly undergrounded due to space, aesthetical and safety

reasons. As it has been mentioned preceedingly, undergrounded cables have lower fault-rates but their repair-time is higher. In order to avoid unacceptable performance indexes, undergrounded distribution grids are usually redundant. This is, each load can be supplied by more than one conductors. The following options are observed [6, 10, 12]:

i) **Purely Radial systems**

Purely radial systems are tree-like systems where loads are clustered and supplied *vertically* from a single feeder. Among radial architectures two main possibilities are observed according to the reliability level aimed at.

- Radial topology with single-derivation (Fig.I.2.4(a)). This option is rarely used in undergrounded configurations because it does not provide any auxiliary path to an outage or interruption.
- Radial topology with double-derivation (Fig.I.2.4(b)). It is a simple way of having two supply paths. This solution is rather expensive because two feeders are needed (a main feeder and an auxiliary feeder), but it can be an interesting option for very high load densities and it is easily automatisable. In this configuration, if the source is lost, all the charges are also lost, but the good point is that it is easy to change to a linked arrangement (looped).

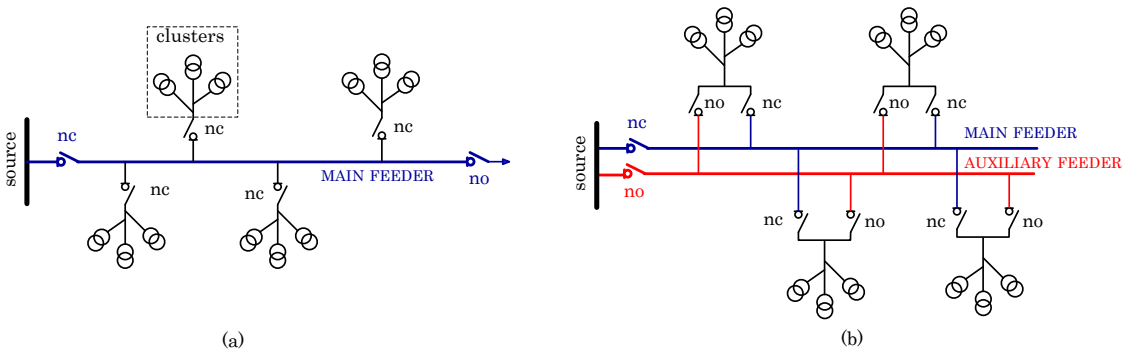


Figure I.2.4: Radial configuration with single derivation (a) and with double derivation (b)

ii) **Looped configurations**.

A looped topology consists in installing emergency ties (either at the end of the main feeder or at laterals) that will ensure an auxiliary path for energy supply. Looped configurations are usually less expensive than double-derivations but they are more complicated to automate because the automaton needs to identify the topology at each instant. Two types of looped configurations are mostly used:

- Linked open loop networks . Service restoration is guaranteed by connecting two sources at the end of their main feeders (Fig.I.2.3(c)). In French literature this configuration is also known as *réseau en coupure d'artère en fuseau*.

- Petal-shape open loop networks . The emergency tie is performed connecting two feeders(Fig.I.2.3(b)) that come from the same source. In French literature this configuration is also known as *réseau en coupure d'artère en boucles ou pétales de marguerite*.

iii) **Meshed systems**.

A meshed topology allows multiple security configurations and it is well-adapted for very large urban centers where a high reliability level is essential. Each intersection is equipped with switches that allow various configurations.

In traditional distribution systems meshed configurations are rare but they offer well known advantages [10]:

- reduction of power losses,
- better voltage profiles,
- greater flexibility and ability to cope with load growth, and
- improvement of power quality due to the fault level increase at each bus.
- Additionally, pertinent interconnections can provide optimally distributed power flows that can contribute to deferment of investments.

It is also important to mention that the forementioned advantages can turn into disadvantages if a careful choice of the number and placement of interconnections is not made. For example, if a weak lateral is involved in an tie-link it can saturate fast or provoke higher losses.

Nevertheless, meshed networks present a more complex planning and operation, and higher short-circuit currents that could imply the substitution of the existing protection and switching systems.

3. The impact of distributed generation in distribution grids

The introduction of distributed generation (DG) in the electrical grid is considered as one of the major changes in the path towards smarter grids. For the last decades, many research efforts have been conducted to study the impact of DG according to the nature of the DG, the connection equipment, the location and the density of DG [7].

The interest on DG is justified by the large amount of advantages that it provides [8]. On one hand, since DG is installed close to consumption centers, transmission costs, losses and reactive power demand at the subestation are reduced. On the other hand, due to their reduced size, it is easier to find locations for installations and their investment cost and time of construction are lower than for large-scale power plants. Finally, since DG is often of the renewable type (except for combined heat and power units or diesel generators, for instance) it participates to a ecologically suistainable grid development.

Nevertheless, in spite of its numerous advantages, a large penetration of DG impacts the electrical grid in the following ways [9, 7]:

- **Voltage profile.** DG is often installed in places where the wind blows or the sun hits the most. These locations might not be the most optimal places to connect DG. Rural areas with long length and small section feeders, for example, are frequently too weak to evacuate the produced power. Injection of active power during periods of low consumption can lead to local overvoltages in the grid. Analogously, during periods of high consumption voltage levels can decrease. The standard solution is then to add more transformers, lines and cables to the grid [35].
- **Protection systems and coordination.** DG inverses power flow directions and therefore impacts on the protection plan, that is designed to be operated under unidirectional power flows. DG requires a complex protection and coordination system.
- **Short-circuit levels.** DG increases short-circuit levels, which means that protections and switching devices must be adapted to these new short-circuit levels. A good aspect of increasing short-circuit levels is, however, that power quality problems are attenuated.
- **Power quality and reliability.** On the one hand, DG is interfaced by power-electronics equipments that inject harmonics to the grid. On the other hand, voltage transients can appear as distributed generators are connected and disconnected. The ride-through behaviour of each type of DG is regulated by system operators by means of grid-codes [36]. Moreover, when variable loads or generators (wind farms) are connected to weak points, phenomenona such as flicker can occur. A low power quality level of the grid can lead to maloperation of grid-connected components and can have an impact on reliability.
- **Losses and congestions.** Losses and congestion depends on the location, distribution, quantity and operation of connected generators and loads. Depending on the time of the year or the day, certain configurations may be either beneficial or harmful.
- **Stability.** In presence of large scale DG penetration, the stability of the grid must be regarded as an important study point, mostly in weak grids and microgrids. Obverse that an instantaneous power-balance between generation and consumption must always be guaranteed.

4. Mitigating the impact of distributed generation

There are various ways of mitigating the adverse effects of distributed generation and, in many cases, these solutions are complementary:

4.1. Grid-code and interconnection standard compliance

An important step for improving power quality and stability in distribution grids is the development of grid-codes and interconnection standards that embrace all possible technologies and scenarios. Then, the second step is to establish laws and recommendations so that a satisfactory operation of DG is guaranteed.

4.2. Demand-side management

Demand-side management allows modulating loads so generation and consumption are well coordinated. For example, in a high-wind and naturally low consumption scenario home appliances (e.g. washing machines and water heaters) can be programmed to start working in order to avoid overvoltages in lines or wind generator shut-down. The other way around, in a low-wind and high consumption scenario, non-critical appliances can be curtailed or delayed in order to reduce the amount of load.

4.3. The use of distribution-FACTS and Custom Power devices

Distribution FACTS (d-FACTS), MVDC and custom-power devices are static power-electronics-based apparatus that can provide numerous auxiliary services and power-quality enhancement functions. Depending on their topology and control, they can regulate voltages, control power flows, damp oscillations, limit short-circuit currents, filter harmonic currents, compensate for voltage sags, unbalances and flicker, generate reactive power etc. (for more information refer to Appendix A). The main problems associated to these kind of devices are their relatively high price, which is not yet low enough to install these equipments in a large scale, and the lack of conviction and experience of utilities in their convenience and reliability. Actually, proving the economical viability and reliability of these apparatus is a key point for their wide-scale development.

4.4. Coordinated control of DG

In stead of using d-FACTS to control bus voltages, the reactive power at the output of DG can be also controlled in order to obtain reference voltages at selected buses [8, 7, 37]. Additionally, the active power generated by DG could also be used for frequency control (primary, secondary or tertiary regulation). As for d-FACTS, distributed generators can be controlled by the distribution system operator in a centrally coordinated or distributed (locally) way.

4.5. Use of storage devices

The combination of energy storage devices and DG can produce a totally controlled power output at the point of common coupling with the grid (PCC). In this way, DG can be assimilated to

a conventional fully-controllable power plant. The energy storage device could provide different fonctions such as smoothing the profile (in the case of small deviations from the previsions or unexpected generation loss), shifting the generation curve according to different strategies (peak-shaving or arbitrage, for example), or frequency regulation [38].

4.6. Changing the structure of the distribution grid

The presence of DG changes drastically the characteristics of existing radial networks, that are migrating from a passive to an active operation. As it was mentioned in section 2., a *passive* meshed configuration offers meaningful benefits in comparison with radial networks. Moreover, if the ties are properly selected and the number and location of DG are correctly chosen, the base benefits of a meshed configuration are improved by the presence of DG. *Active* meshed networks join the potential beneficial aspects of DG with the potential advantages of meshed architectures: reduction of losses, improvement of voltage profiles, deferment of investments resulting from a reduced equipment explotation (conductors and transformers), improvement of stability etc.

In [10, 11, 12, 39] an intensive work has been developped in order to unveil the interest of operating distribution grids in a meshed configuration. The obtained results can be summarized as follows:

- Actual distribution networks are partially meshed due to the existing looped configurations but they are radially operated under normal conditions.
- Weakly meshed networks have the potentiality of accomodating much more DG than radial configurations.
- In general, changing from an open looped to a closed looped network is positive from the DG integration point of view. However, the interconnections must be carefully chosen in order to avoid negative effects (higher losses, saturation of lines etc.). Thicker meshes cannot be chosen randomly and they have to be meticulously planned according to the generation and load allocation. It must be noted that the thicker the mesh is, the higher the fault withstand capability of such network is.
- Short circuit level, voltage regulation, and protection coordination are the main disadvantages of meshed distribution networks:

  (i) **Short circuit levels** can increase to intolerable values that would lead to change the switchgear. Short circuit current limiters could provide a solution to this short-circuit current increase.

  (ii) **Voltage regulation** via the transformer tap-changer must be revised because multi-directional power flows may cause maloperation of tap changers. On the other hand, meshed configurations naturally contribute to a better homogeneization of voltage profiles. In anyway, DG can also be operated to contribute to voltage control.

(iii) **protection coordination** becomes a complex issue to solve in meshed networks with DG penetration.

- Meshed distribution networks can be a valid option to improve the capability of distribution networks to accomodate DG but it needs to be accompanied by revolutionary changes in the present distribution network concept.

5. On the hypothesis of weakly meshed MV distribution grids

This work is fundamented on the hypothesis that the MV distribution grids of the future will be meshed (at least weakly). But, as it has been mentioned in the preceding section, it is not possible to switch instantaneously to a meshed configuration. There are still plenty aspects to analyse and develop:

■ **Choice of the optimal locations for the grid-ties.**

Rather than blindly closing the existing emergency switches, the optimal location of interconnections must be assessed considering the situation and power of DG and loads, their generation/consumption profiles, expected losses and voltage deviations, geographical features, deployment costs etc.

■ **Deployment of monitoring and communication infrastructures.**

In order to guarantee a satisfacty operation of meshed distribution grids it will be necessary to monitor and control the voltages, phase-angles and powers at the main buses [35]. This will not be possible without installing the appropriate measuring equipment at the required points. Additionally, a widely spread communication and information infrastructure is needed to transmit the information to/from to the control centers.

■ **Power-flow control.**

In electrical grids power follows the laws of physics (i.e. the lowest impedance path). But the natural paths followed by powers may not always suit system operators and they might want to modify them according to a particular need. Power flows and voltage profiles can be modified in two different ways:

a.- The **traditional way**, normally used in transmission systems, consists on modifying the active and reactive power outputs of grid-connected power plants.

b.- The traditional control way can be complemented by the use of **static power electronics apparatus** (TCSC, HVDC, SSSC, UPFC, SVCs, STATCOMs etc.) that can modulate the power through the lines and regulate the voltage at a particular bus [40, 41, 42, 43, 44].

■ **Power quality assessment and mitigation.**

A high penetration of DG will impact the power quality level of distribution networks (radial or meshed). It is therefore important to evaluate the causes, nature, frequency, and propagation of power quality perturbations in meshed distribution networks in order to identify and implement the possible solutions. As shown in Fig.I.2.5 the power quality of distribution networks can be improved in different ways: acting at the source of disturbance, improving the design of the network, using mitigation equipment, or improving the immunity of the sensitive equipment.

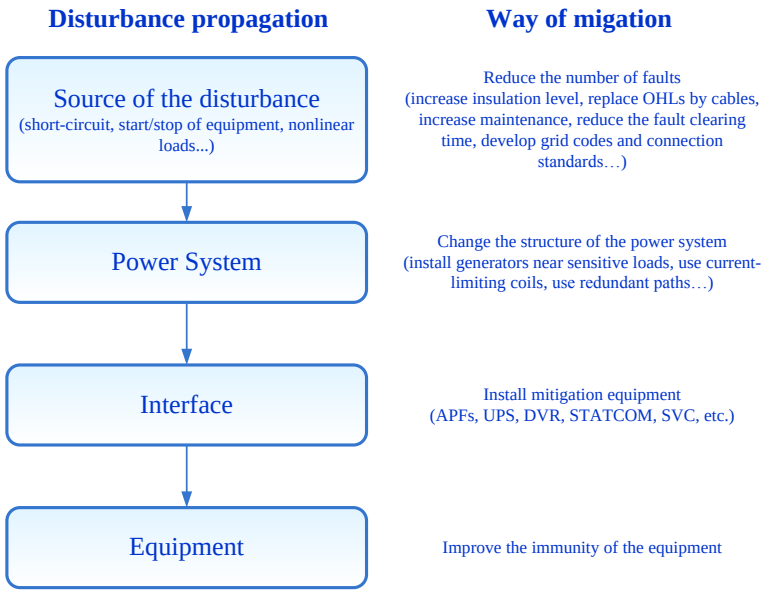


Figure I.2.5: Power quality disturbance propagation and mitigation ways (from [45])

■ **Development of control algorithms.**

The objective of system operators is to guarantee a reliable and efficient operation of distribution grids. For this purpose, it is necessary to develop centralized or distributed control algorithms that will be able to calculate the dispatching of the generators and the reference signals for the static power electronics devices. For example, system operators may want to

- avoid saturation of certain lines and transformers, avoid power reversal
- enhance the transient stability of the system,
- damp the dynamic oscillations of the system,
- control frequency variations,
- minimize power losses, minimize voltage deviations in grid buses,
- force power transactions between neighbouring areas, or priorize storage or consumption at selected points.

■ **Redesign of the protection plan.**

A very important aspect to analyse in meshed distribution grids is the protection plan. In order to mesh distribution grids the whole protection plan, which was originally designed for a radial operation, must be re-designed. Among others, anti-islanding algorithms must be developped in order to guarantee a safe operation of the network.

- **Development of adapted regulatory framewors, markets and business models.**

  The integration of DG and demand-side management in interconnected distribution grids will require the development of regulatory policies and standards, business models, and markets that will enable the participation of all the network participants (prosumers, service providers, DGs etc.) [46].

Chapter I.3

Objectives

The preceding chapter has explained that the migration towards *active* meshed distribution networks will entail intense research activities at different levels. The required research areas, which are described in Chapter I.2, are illustrated in Fig.I.3.1. With the whole spectra of tasks in mind, the **higher-level objectives** of this PhD can be formulated as:

① To study a solution that can modulate the power-flow (active and reactive powers independently) between two distribution grids.

② Additionally, the evaluated solution must be able to mitigate the power quality disturbances in one of the distribution grids or avoid their propagation from one grid to the other.

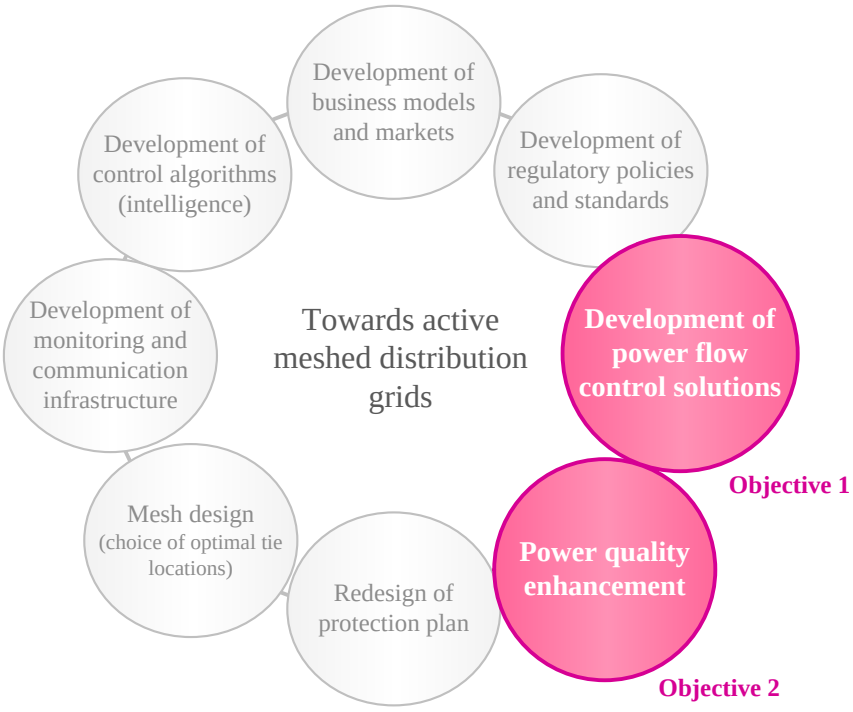


Figure I.3.1: Necessary tasks to migrate towards active meshed distribution grids. Main objectives of this PhD.

The dual challenge of controlling power-flow and power quality simultaneously may be addressed by static power electronics apparatus. So far, and as it is exhaustively explained in Appendix A, a great deal of VSC-based power electronics devices exist. The existing static power electronics apparatus can be classified according to different criteria. For example, they can be classified according to the functions that they can address, to their power or voltage level, to their topology etc.

Fig.I.3.2 shows a general classification of the most characteristic static power electronics apparatus in terms of their system level, their topology and their functions. As it can be observed, each of the topologies (i.e. series, shunt, universal and AC-DC-AC topologies) finds its counterpart at the transmission and at the distribution level. Of course, the design and control challenges at transmission or at distribution levels are rather different but the essential topology remains the same.

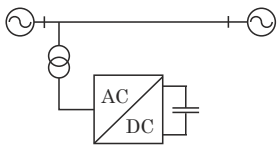
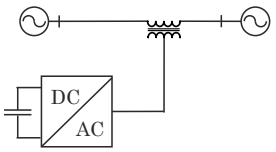
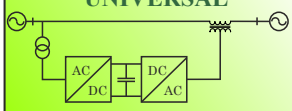
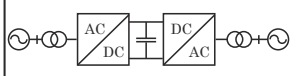
Name		Topology	Preferred Tasks	
Transmission	Distribution		Transmission	Distribution/Power quality
STATCOM	d-STATCOM or Shunt APF	SHUNT 	Voltage control/ reactive power regulation Oscillation damping	Flicker compensation Voltage regulation/ reactive power compensation Current harmonic filter
SSSC	DVR	SERIES 	Power flow (reactive) control Transient stability Oscillation damping	Sag/swell compensation
UPFC	**UPQC**	**UNIVERSAL** 	**STATCOM+SSSC**	**Shunt APF + DVR**
HVDC	MVDC	AC-DC-AC 	Power flow control Transmission of power over long distances/ interconnection of remote energy sources Interconnection of asynchronous grids Voltage control/ reactive power regulation Transient stability Oscillation damping	Connection of distributed generation and loads. Interconnection of distribution grids. Active power filtering, fire-wall for voltage sags.

Figure I.3.2: Comparison table of static power electronics devices.

As it can be obseved in Fig.I.3.2, from the large choice of static power-electronics based apparatus

there is one particular configuration, known as *univeral topology*, that offers a remarkable flexibility to address multiple functions. The universal topology is the product of merging a series-connected device with a shunt-connected device and it takes different names according to its application. In transmission grids, when used for power-flow control and voltage regulation, it is known as Unified Power Flow Controller (UPFC) and, in distribution grids, when used for compensating for current harmonics and voltage sags at the end of the line it is known as Unified Power Quality Controller (UPQC).

A closer look at the capabilities of the UPFC and the UPQC shows that the universal topology may be a very appropriate structure for interconnecting distribution grids. It has actually a great capacity to satisfy the above mentioned objectives of power-flow and power quality. The generic name given to this very versatile apparatus is Unified Power Line Conditioner (UPLC) [14, 16].

Considering the outstanding theoretical capabilities of the UPLC to satify the higher-level objectives of this PhD, **the main ambition of this PhD is to explore the real interest and potential of a UPLC when used for interconnecting MV distribution grids**. Thus, this PhD manuscript aims at performing a comprehensive analysis of the ensemble UPFC/UPQC/UPLC featuring the advantages, disadvantages, challenges, and barriers that characterize this static power electronic device. Or, in other words, the goal of this work consists in answering questions of the type: "What is the real interest of using a UPLC to interconnect MV distribution grids?","In which conditions is a UPLC interesting and in which it is not?", "What can it be done with a UPLC?", "What functions should the UPLC address?", "What are the barriers and limitations of using this apparatus?", "Where are the challenges?".

In order to develop a structured answer to these interrogations a set of sub-objectives have been established:

- **To evaluate the sizing and design of the UPLC**.

  It is important to identify the different design options in terms of components and topologies, to determine a general sizing procedure that will allow to evaluate the rough dimensions of the components, and to recognise the key challenges in UPLC design.

- **To develop UPLC models to be used in the synthesis of the control laws**.

  Since this PhD is oriented towards a system approach it is necessary to developp UPLC models that are suitable for power-flow and control applications. In addition, models of adjacent components (e.g. lines and cables) shall be developped.

- **To analyse and develop UPLC control structures that are well adapted for working in distorted grid environments**.

  Since the UPLC will be located at the distribution level and in a high DG penetration scenario, control approaches suitable to cope with unbalances, harmonics and voltage sags must be evaluated. Moreover, the need of observers, that will serve to estimate voltage and current values at distant ends is also previewed.

In relation with the subject of working at distorted environments, synchronization methods and sequence extraction techniques capable of providing a fast and reliable information are needed. These techniques also need to be carefully evaluated.

- **To validate the developped control approaches by means of a representative set of simulations**.

  All the developments proposed along the manuscript must be correctly validated in simulations. Unfortunately, the construction of a reduced scale prototype is out of the scope of this project.

The UPLC constitutes a central part of this work. However, the existance of other flexible static power electronic apparatus that could also serve for analogous purposes must not be misregarded. Such is the case of the MVDC, the medium-voltage equivalent of the HVDC. The MVDC is also a remarkable multi-purpose apparatus that can address the same (or similar) functions as the UPLC (see Fig.I.3.2). For this reason, **a strategic objective of this PhD is to perform an exhaustive comparison between the UPLC and the MVDC**. This comparison shall provide selection criteria for system developpers in preliminar planning stages.

Consequently, this document is divided in the following parts:

- **PART I**, the present part, describes the context of this work and introduces its main objectives.
- **PART II** presents the existing experiences on interconnecting distribution grids with static power electronic devices, describes the UPFC/UPQC/UPLC and the MVDC, and it provides a comprehensive comparison between the UPLC and the MVDC.
- **PART III** goes through the design, dimensioning, modeling, and control of UPLC when used for interconnecting distorted distribution grids.
- And finally, **PART IV** gathers the main conclusions and future work perspectives extracted through the document.

Part II

Power Electronics devices for distribution network interconnection

OUTLINE OF PART II

Part II is divided as follows:

- **Chapter II.1** describes two out of the few found works on the interconnection of MV distribution grids. One of the experiences is proposed by the CRIEPI, in Japan, and consists of meshing the 6.6 kV grid with MVDCs. The other work deals with the interconnection of distribution grids with SSSCs.
- **Chapter II.2** introduces and describes two candidate devices that may be used for distribution grid interconnection: (i) the universal topology, including the UPFC, the UPQC and the UPLC, and (ii) the MVDC.
- **Chapter II.3** discusses the advantages and disadvantages of each of these topologies in terms of the structure of the apparatus, the interconnection characteristics and the attainable objectives. In order to quantify the size difference of these apparatus in different conditions, an indicative case study is also proposed.

Chapter II.1

Existing experiences on interconnecting MV distribution networks with power electronics equipment

In meshed distribution grids, power-electronics based equipments may provide essential functions such as voltage support, short-circuit current limiting, power-flow control or power-quality enhancement. Literature observes a myriad of studies addressing the use of FACTS and HVDC in transmission networks. Many studies dealing with distribution FACTS (d-FACTS) have also been tackled by the research community but, as a general trend, studies regarding d-FACTS cover connection issues of DG (grid-code and power quality compliance) [47] rather than power flow control.

Projects dealing with interconnection of MV distribution grids by static power-electronics equipment are rare, but two initiatives have been identified:

1. Autonomous Demand Area Power System (ADAPS) (from [1])

The Autonomous Demand Area Power System (ADAPS) is a concept developped by The Central Research Institute of Electric Power Industry (CRIEPI) in Japan [1]. The ADAPS concept is motivated by the large-scale penetration of distributed generation (including fuel-cells and photovoltaics) expected in Japan. The 6.6 kV power distribution system of Japan is centered in urban areas with high power demand densities and a massive DG insertion would generate power flow congestions and voltage fluctuations in distribution lines.

Fig.II.1.1(b) shows the future utility power system envisioned by the CRIEPI, where the ADAPS are integrated. The ADAPS is defined as the segment that includes the distribution system at 6.6 kV and a primary system at 66 kV. Fig.II.1.1(a) illustrates and example of ADAPS configuration and its related communication network structure. The meshed structure is controlled by means of back-to-back MVDC devices named *Loop Power Flow Controllers (LPC)* by the authors. The whole system is controlled by an *operation control system (OCS)* and the communication network consists of sensors, demand/supply interfaces, optical fibers, media converters and hubs.

Fig.II.1.2 depicts the 6.6 kV test-system built at *Akagi Testing Center*. It consists of some feeders and three LPCs (the yellow hexagones). The main feeder of the system consists of three sections devided by sensors and each section is connected with another feeder by a LPC. Sections two and three have a load and a generator.

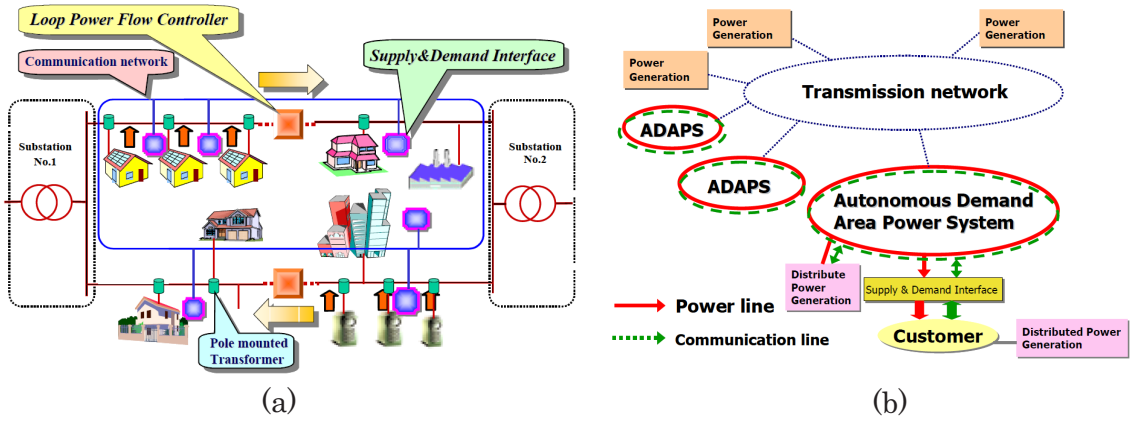


Figure II.1.1: (a) Configuration of ADAPS (from [1]) (b) Expected future power system (from [1]).

The LPC is a MVDC that enables simultaneous control of power flow and terminal voltage at both power line sides. The two power lines can be connected together by the LPC even though voltages and phases between two lines are quite different. As a result, a looped or meshed configuration can be chosen in the demand area. Additionally, because the fault current of the looped network can be isolated by LPCs, reliability of protection and safety are assured.

The CRIEPI has made extensive research, development and testing on ADAPS. Some important features of their work are presented in a series of articles:

- In [48], a transformerless LPC that uses *HVDC-Light* technology is presented. The main characteristic of *HVDC-Light* technology is that converters are two-level converters where IGBT switches are connected in series in order to attain high voltages. The interest of removing the transformer consists in reducing the overall volume of the installation, which is critical in distribution systems. However, it must be mentioned that the use of a MVDC as a looping device can be a rather expensive solution because the full power flows through both converters.
- In [49] and in [50] methods for calculating the optimal and distributed control commands for the LPCs are addressed. The objective function used for calculating the active and reactive power references is a combination between the minimization of transmitted losses and the minimization of the voltage deviation error. The distributed control coefficients are obtained by a least-squares method.

2. D-SSSC for looped or meshed distribution grids

In [51, 52, 53] the use of a distribution static series synchronous compensator (d-SSSC) for distribution grid interconnection is analysed. The DC-side of the d-SSSC is just composed of a capacitor and, for this reason, it can only inject reactive power. The d-SSSC behaves as a variable reactance

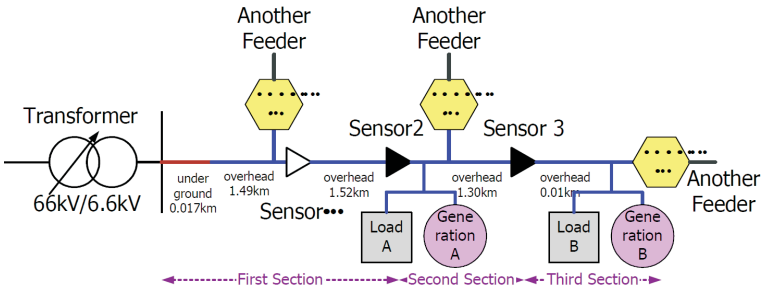


Figure II.1.2: Test-bench for ADAPS.

connected in series with the grid and its main objective is to either control active or reactive power (but not both at the same time).

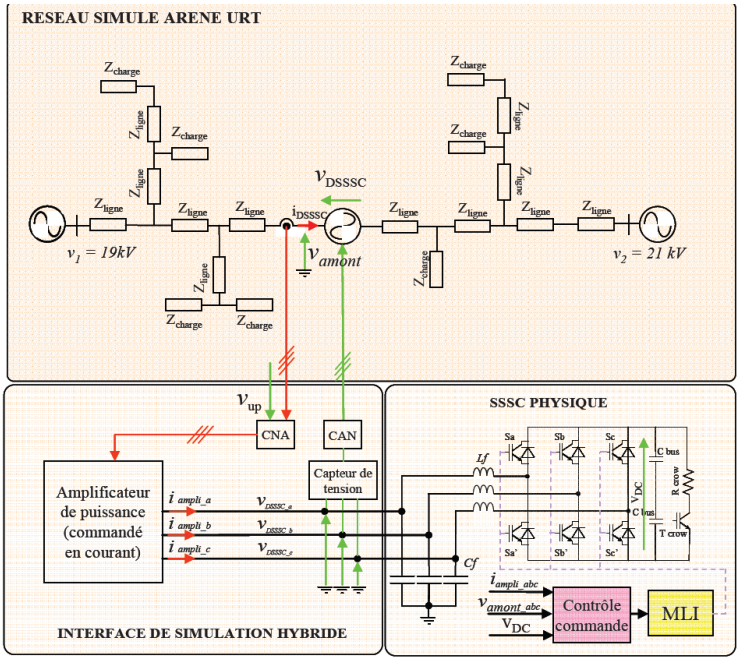


Figure II.1.3: Hybrid test-bench used in [51].

An interesting feature of the work developped in [51, 53] is the use of the d-SSSC for limitation of short-circuit currents. The authors of [51, 53] present two different approaches to limit short-circuit currents:

(i) The first approach is based on control and it requires that a high voltage is injected in order to cancel short-circuit currents. One of the challenges comes from the need of charging the DC-bus voltage to a suitable value when the fault is detected.

(ii) The second approach consists in stopping the switched commutation when a fault is identified and thus making the apparatus behave as a rectifier. During the short-circuit the current will flow through the diodes and will charge the DC-bus until the maximum accepted value.

Another good feature of the PhD work of [51] is that simulations was validated in a hybrid test-bench (Fig.II.1.3) that is composed of three parts:

1. A real-time emulating network (ARENE RT) where the physical description and the simulation of the network is done;
2. An interface that:
   - converts line currents from the simulation into power signals to the VSC and inversely,
   - it digitalizes the measurements taken at the VSC and integrates them into the real-time simulator
3. The physical converter, which is a three-phase VSC with a DC-input and a LC filter.

Short-circuit current limiting approaches, but applied in UPQC devices, have also been tackled in [54, 55].

Chapter II.2

Candidate topologies for MV distribution grid interconnection

The previous chapter indicates some device proposals for MV distribution grid interconnection that have been found in literature: a medium voltage back-to-back device [48] and a distribution SSSC [52, 51, 53]. One fundamental difference between these approaches is that the first one can independently control active and reactive power, while the second can only control either active or reactive power.

Due to the lack of studies on MV distribution grid interconnection by means of power electronics equipment, the author of this PhD has found inspiration on solutions already used at transmission level, which is actually meshed. However, the structure, operation and characteristics of transmission and distribution networks are essentially different and some aspects must be accounted for when choosing the most adequate power electronics devices:

- Transmission lines are predominantly inductive (the X/R ratio is around 10) but distribution lines and cables have a much higher resistive component (the X/R ratio can be as small as 0.5). Basic FACTS theory has been developped considering that lines are inductive and that the voltage profile is rather uniform. According to those premises, active power is controlled by varying the transmission angle between two buses, and reactive power is controlled by varying the magnitude of a voltage at a node. In distribution grids, the presence of a resistive component further increases the coupling between active and reactive powers. For this reason, in this PhD, devices that can control active and reactive power independently have been prioritized.

- The power quality level at transmission and at distribution level is different. On one hand, most of the polluting charges and generators are connected at distribution level. On the other hand, short-circuit powers at distribution level are lower than at transmission level so power quality phenomena has a higher impact and propagation at distribution level. This means that, power electronics devices connected at the distribution level must avoid adding pollution to the grid, must avoid sudden disconnections and, if possible, must help to increase the overal power quality level of the distribution network. For this reason, the selected apparatus must also contemplate the possibility of compensating for power quality issues.

After this reflection, two candidate topologies have been selected: the **universal topology**

(UPFC, UPQC and UPLC) and the **AC-DC-AC topology**. It must be noted that other topologies that can control active and reactive power independently also exist (a STATCOM with battery or a SSSC with battery, for example). However, these options need batteries or external active power sources that require frequent maintenance and that loose efficiency along the time.

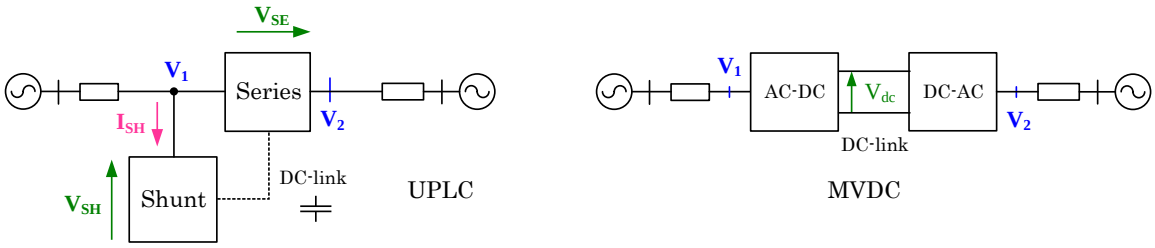


Figure II.2.1: Conceptual representation of universal FACTS and AC-DC-AC topology

The universal topology is composed of a series-connected device and a shunt-connected device that are interconnected by their DC-sides by a DC-link. Depending on the use that is given to this topology, three power-electronics devices share the same structure:

(i) The **Unified Power Flow Controller (UPFC)** is a FACTS device that is primarily used for power-flow control and voltage regulation in transmission networks.

(ii) The **Unified Power Quality Conditioner (UPQC)** is a custom-power device that serves at the same time to protect sensitive loads from voltage sags coming from the supply-side, and to filter the current harmonics absorbed by polluting loads.

(iii) The **Unified Power Line Conditioner (UPLC)** is a generic name given to a device that integrates the functionalities of the UPFC and the UPQC.

The **AC-DC-AC** topology is a well-known configuration that is used for different applications in the electrical grid. The conceptual representations of the universal topology and the AC-DC-AC topology are depicted in Fig.II.2.1. The following sections provide a deeper description of these architectures.

1. The Unified Power Flow Controller (UPFC)

The UPFC was first proposed by Gyugyi [56, 57] and by Ooi [56, 57] in the early 90s as the ultimate FACTS device because it can control various grid parameters (voltage, impedance and angle) at a time. Ever since, the UPFC has been considered as the most flexible FACTS device and it has been tackled in more than 100 publications. Research on UPFC is very prolific and many different aspects have been addressed. Ideally, UPFC is a very interesting actuator and it may have an important place in future transmission networks [42]. In the meantime, only three installations exist in the world [58, 59, 60, 61, 62, 63, 64].

The principal function of UPFC is power flow regulation (active and reactive powers) but, thanks to its great versatibility, it can simultaneously address other objectives. In **steady-state** it can be used for power flow regulation (power sharing between lines and loop-flow control for instance) and voltage regulation (linked to reactive power). In **dynamic environments** it can be used to damp low-frequency dynamic oscillations (e.g. inter-area oscillations and subsynchronous resonances) and for transient stability enhancement.

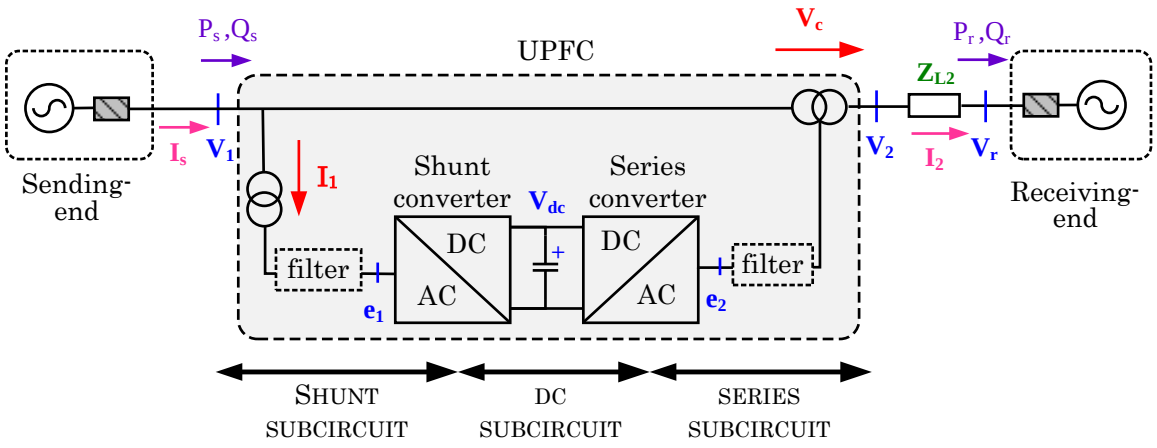


Figure II.2.2: One-line representation of UPFC

1.1. UPFC description

Fig.II.2.2 presents a simplified one-line diagram of a UPFC where its main components can be appreciated. The UPFC is composed of three inter-related subcircuits: the series subcircuit, the shunt subcircuit and the DC subcircuit.

1.1.1. The series subcircuit

The series subcircuit is, in certain way, the heart of the UPFC because it is the subcircuit that guarantees its main function: power-flow control. The series subcircuit consists of (a) a series transformer, (b) a series filter that gets ride of switching harmonics and softens the output voltage of the VSC, and (c) a VSC that chops the DC-voltage as to get a proper fundamental voltage. The working principle of the series subcircuit can be understood looking at Fig.II.2.3,where, for simplicity, an inductive line has been considered.

The series subcircuit injects a voltage in series with the line ($\mathbf{V_c}$) that, in turn, modifies the voltage at terminal 2 ($\mathbf{V_2}$). As it is observed in expressions (II.2.1) and (II.2.1) (already derived in chapter A), the active and reactive power at the receiving-end can be affected controlling the magnitude and angle of $\mathbf{V_2}$. In this way, by injecting $\mathbf{V_c}$, $\mathbf{V_2}$ can take any of the values inside the coloured circle of Fig.II.2.3(b). Note that the radius of the circle is given by the maximum magnitude of the injected voltage (V_{c-max}).

The magnitudes and phase-angle difference between $\mathbf{V_c}$ and $\mathbf{I_2}$ determine the active and reactive powers that the series subcircuit need to inject in the line in order to produce the desired $\mathbf{V_c}$. In the case of a SSSC, $\mathbf{V_c}$ is always injected in quadrature with $\mathbf{I_2}$ to avoid active power consumption/injection. In the case of a UPFC, since $\mathbf{V_c}$ can take any arbitrary angle values, active power is needed. And, it is the shunt-side subcircuit that provides the series subcircuit with the required active power.

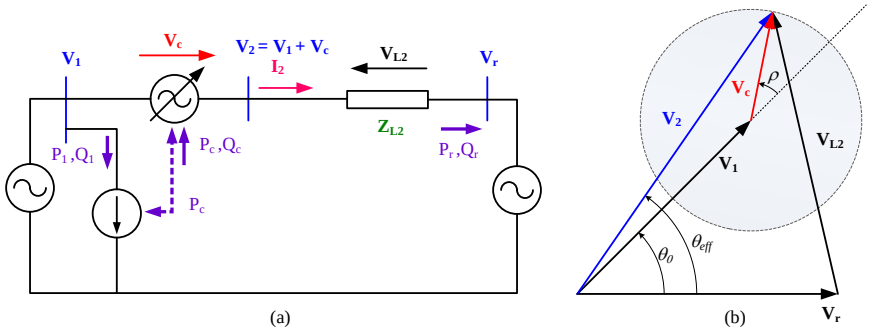


Figure II.2.3: Working principle of the UPFC: (a) Simplified one-line diagram, (b) vector diagram

$$\mathbf{P_r} = \frac{V_2 V_r}{X_L} \sin\delta \tag{II.2.1}$$

$$\mathbf{Q_r} = \frac{V_2 V_r \cos\delta - {V_r}^2}{X_L} \tag{II.2.2}$$

Depending on how $\mathbf{V_c}$ is controlled, the series subcircuit can emulate different operation modes [40]: (i) voltage-regulation ($\mathbf{V_c} = \pm\mathbf{\Delta V}(\rho = 0)$), (ii) series-reactive compensation ($\mathbf{V_c} = \mathbf{V_q}$), (iii) phase angle regulation (phase shift), or (iv) multifunction power flow control. These operating modes are depicted in Fig.II.2.4.

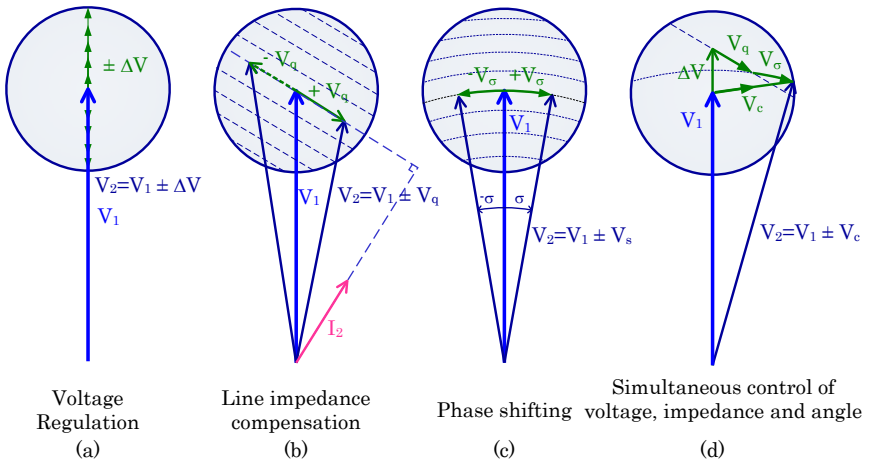


Figure II.2.4: Basic operation modes of the UPFC: (a) Voltage regulation, (b) Line impedance compensation, (c) Phase-shifting, (d) Simultaneous control of voltage, impedance and angle

1.1.2. The shunt subcircuit

The injection angle of $\mathbf{V_c}(\boldsymbol{\rho})$ can take any values in the $0 \leq \rho \leq 2\pi$ range. This means that, every time that line current is not in quadrature with the injected voltage, the series subcircuit needs to inject or absorb active power. If the DC-side voltage source is a mere capacitor, active power needs to be supplied/consumed by the capacitor at expenses of the voltage between its terminals. This operation way is only acceptable when the active power is demanded only for short time intervals or when the DC-side capacitor is very large (which is not usually advisable because it is a bulky and expensive component). The active power can also be produced or stored in a battery, but this solution presents drawbacks such as the loss of efficiency with time and the need of regular maintenance. The UPFC offers an ingenious solution based on providing the required active power by another VSC that is connected to a nearby bus. This auxiliary function is performed by the shunt subcircuit.

The shunt subcircuit is very similar to the series subcircuit with the difference that it is connected in parallel with the line. Like the series subcircuit, it is normally composed by a **shunt-connected transformer** (unless a multilevel VSC topology is used), a **shunt filter** for assuring a smooth absorbtion/injection current and a **VSC** connected to the DC-link. When the shunt branch current ($\mathbf{I_1}$) is in phase with the fundamental voltage at the output of the shunt-VSC ($\mathbf{E_1}$), the shunt subcircuit absorbs/sinks active power. This active power, attenuated by the losses of the converter, the DC-link and the filter, is absorbed or sinked by the series subcircuit in order to respond to power flow demands. If the control of the UPFC is perfect (ideal), active power demanded/generated by the series branch is instantaneously supplied/absorbed by the shunt branch and thus, the DC-link voltage does not suffer from any fluctuations. In the reality, DC-bus voltage varies during transients. Variations depend on the value of the capacitor and the quality of the control system.

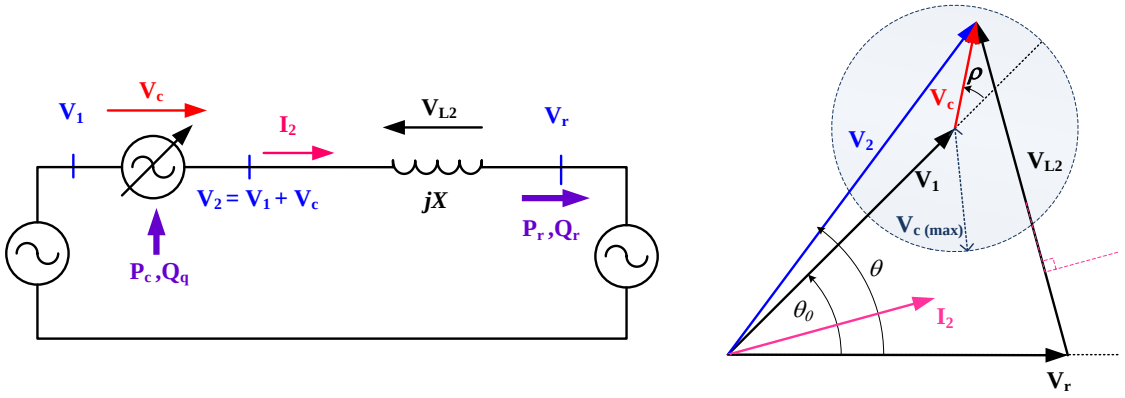
Besides providing the necessary active power, the shunt subcircuit can additionaly address other functions such as injection/absorbtion of reactive power or regulation of $|\mathbf{V_1}|$.

1.1.3. The DC subcircuit

The DC subcircuit is normally composed of a DC capacitor, which value should be as small as possible to reduce the volume and cost of the overall device. Since the value of the DC capacitor is usually small, the control of the shunt converter must have a good transient response to avoid high voltage deviations (and depletion) in the DC-link when sudden power demand is required by the series converter. In UPFC both VSC converters are connected in back-to-back and thus, the distances between converters are kept small. The reason is that UPFC is not intented for long distance power transmission, as is sometimes the case of HVDC.

1.2. Power-flow controllable areas

In order to have a better understanding of how active and reactive powers are independently controlled and which are the reachable limits, a simple case (depicted in Fig.II.2.5(b)) will be developed. In this case, to help the comprehension, the transmission line is considered to be a pure reactance ($\mathbf{Z_{L2}} = jX$) and the development is made considering a single-phase case with root-means-square (RMS) values.



(a) (b)

Figure II.2.5: (a) Simplified one-line diagram of a UPFC with a purely reactive line, and (b) corresponding vector diagram

The apparent power at the receiving-end is given by equation (II.2.3), where it is observed that the apparent power can be divided into two parts: the apparent power when no compensation is applied ($V_c = 0$), $\mathbf{S_{r0}}$, and the apparent power generated due to the addition of a series voltage, $\Delta\mathbf{S_r}$, (see equation (II.2.3)).

$$\mathbf{S_r} = \mathbf{V_r}\mathbf{I_2}^* = \mathbf{V_r}\left[\frac{\mathbf{V_1} + \mathbf{V_c} - \mathbf{V_r}}{\mathbf{j}X}\right]^* = \underbrace{\mathbf{V_r}\left[\frac{\mathbf{V_1} - \mathbf{V_r}}{\mathbf{j}X}\right]^*}_{\mathbf{S_{r0}}} + \underbrace{\mathbf{V_r}\left[\frac{\mathbf{V_c}}{\mathbf{j}X}\right]^*}_{\mathbf{\Delta S_r}} \tag{II.2.3}$$

Defining the voltage vectors in accordance with the vector diagram of Fig.II.2.5, as in eq.(II.2.4), and considering that $\mathbf{V_1}$ and $\mathbf{V_r}$ have the same magnitude, ($|\mathbf{V_1}| = |\mathbf{V_r}| = V$) the expressions of $P_r(\theta_0, \rho)$ and $Q_r(\theta_0, \rho)$ can be obtained.

$$\begin{cases} \mathbf{V_1} = V\ e^{\,\mathbf{j}\theta_0} \\ \mathbf{V_r} = V \\ \mathbf{V_c} = V_c\ e^{\,\mathbf{j}(\theta_0+\rho)} \end{cases} \tag{II.2.4}$$

Accordingly, $P_r(\theta_0, \rho)$ and $Q_r(\theta_0, \rho)$ are expressed as:

$$P_r(\theta_0, \rho) = P_{r0}(\theta_0) + \Delta P_r(\rho) = \frac{V^2}{X}\sin(\theta_0) + \left[\frac{VV_c}{X}\sin(\theta_0 + \rho)\right] \tag{II.2.5}$$

$$Q_r(\theta_0, \rho) = Q_{r0}(\theta_0) + \Delta Q_r(\rho) = \frac{V^2}{X}\left[\cos(\theta_0) - 1\right] + \left[\frac{VV_c}{X}\cos(\delta_0 + \rho)\right] \tag{II.2.6}$$

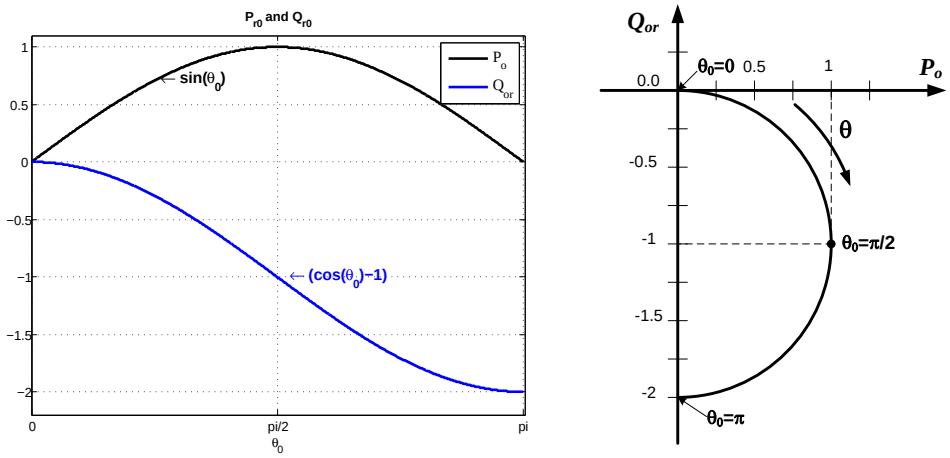
Equations (II.2.5) and (II.2.6), provide an interesting information. Indeed, both real and reactive power expressions can be divided into two sub-expressions or terms. The first term exclusively depends on θ_0 and it represents the power transmission in an uncompensated case. The second term includes ρ and represents the part of the power flow that can be influenced by a compensating device (i.e. UPFC).

After some operations, the relationship between natural power flows is obtained (without normalizing):

$$\{P_{r0}(\theta_0)\}^2 + \{Q_{r0}(\theta_0) + 1\}^2 = \left\{\frac{V^2}{X}\right\}^2 \tag{II.2.7}$$

and after normalizing by V^2/X,

$$\{P_{r0}{}^{\text{norm}}(\theta_0)\}^2 + \{Q_{r0}{}^{\text{norm}}(\theta_0) + 1\}^2 = 1 \tag{II.2.8}$$



(a) (b)

Figure II.2.6: Transmittable P and Q in function of θ_0 when $V_c = 0$ (normalized values)

In a similar way, after some manipulations, the relationship between P_r and Q_r (equations (II.2.5) and (II.2.6), respectively, is obtained (without normalizing):

$$\{P_r(\theta_0, \rho) - P_{r0}(\theta_0)\}^2 + \{Q_r(\theta_0, \rho) - Q_{r0}(\theta_0)\}^2 = \left\{\frac{V_{cmax}V}{X}\right\}^2 \tag{II.2.9}$$

and after normalizing by V^2/X,

$$\{P_r^{\text{norm}}(\theta_0,\rho) - P_{r0}^{\text{norm}}(\theta_0)\}^2 + \{Q_r^{\text{norm}}(\theta_0,\rho) - Q_{r0}^{\text{norm}}(\theta_0)\}^2 = \left\{\frac{V_{cmax}}{V}\right\}^2 \tag{II.2.10}$$

Relationship (II.2.9) shows that the controllable area $P_r(\theta_0,\rho)$ and $Q_r(\theta_0,\rho)$ is a circle which center $(P_{r0}(\theta_0), Q_{r0}(\theta_0))$ varies according to the transmission angle θ_0. For a particular transmission angle value, each specific operating point is given by the value of ρ and $|V_c|$, that will always be inside the circle of radius V_{cmax}/V. Fig.II.2.7 shows the controllable areas for four different values of the transmission angle θ_0. In these drawings the injected voltage is half the magnitude of the line (phase) voltage $V_{cmax} = 0.5V$ or $V_{cmax} = 0.5$ (normalized).

As depicted in Fig.II.2.7, the controllable area of a UPFC depends on two parameters: (i) the transmission angle (θ_0), and (ii) the maximum series injected voltage. This fact can constitute a significant drawback comparing with the MVDC, which controllable area extends to the four quadrants independently of the transmission angle. In reality, when the line is not purely inductive and the voltages at both ends vary, the analysis gets more complex, but the interested reader may refer to [65, 66, 67, 68, 69, 70] for further knowledge on the subject.

2. The Unified Power Quality Conditioner (UPQC)

An UPQC is a custom-power device with universal topology that gathers the functionalities of series-connected and shunt-connected compensating devices in a single apparatus. By mid-late 90s active power filter (APF) technology was a relatively mature subject [71, 72, 73, 74]. The acquired knowledge on series and shunt APFs was wisely integrated by [13, 14, 15], who proposed an interesting combination of shunt and series APF that they named UPQC.

The UPQC shares the same topology with the UPFC, but their applications areas and functionalities are rather different. As mentioned in previous sections, the UPFC is entitled for transmission applications (power-flow control, transient stability enhancement, dynamic oscillation damping, loop-flow control, voltage regulation ...), while the UPQC is designed for addressing power quality issues at MV and LV distribution levels. Additionally, the UPFC is connected between two grid buses, while the UPQC is usually connected at the end of a distribution line, at the point of common coupling (PCC) with sensitive and/or polluting loads. Also, because one operates at transmission levels and the other at distribution levels, the power and voltage levels are much higher for UPFC than for UQPC (in the order of tenths of MVAs to kVAs, respectively). Ratings and characteristics of components, converter topologies, protections and control of an UPFC are very different. For example, at lower voltage levels a classical two-level VSC may be satisfactory and, depending on the power rating, a high switching frequency may be allowed.

Fig.II.2.8 depicts a one-line schematic representation of a UPQC and, as it is observed, the basic structure is exactly the same as a UPFC. In most of the cases the shunt-branch is placed at the load side to avoid current harmonics getting across the series filter. Only in some rare cases [15, 75] the

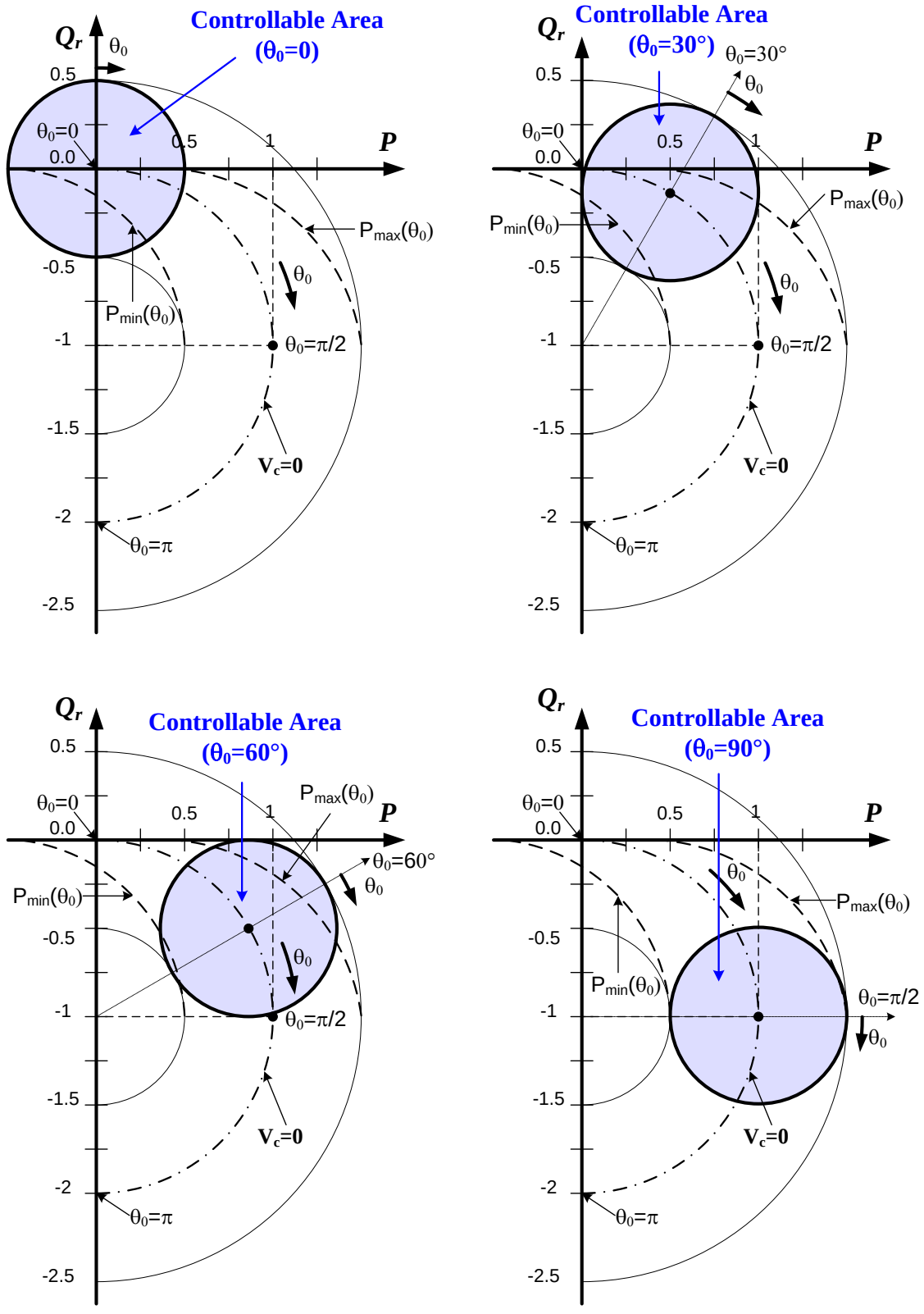


Figure II.2.7: Controllable P_r and Q_r0 areas in terms of θ_0, ρ and V_{cmax}. Normalized values.

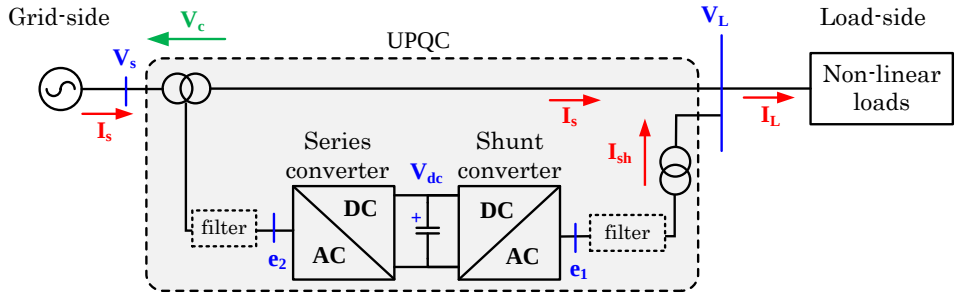


Figure II.2.8: One-line representation of a UPQC.

shunt-branch has been found upstream the series filter. In those uncommon cases, the upstream shunt APF is in charge of providing active power to the series-branch and the downstream shunt structure (active or passive) is in charge of compensating for harmonic currents and/or reactive power.

The shunt APF (usually located close to the load) can perform the following functions:

- As for the UPFC, the imperative function of the shunt APF is to keep the DC voltage constant. In other words, it absorbs/injects the active power that the series APF requires to inject the demanded series voltage. In the case of DVRs, for example, there is not a shunt APF so the injected voltage is often in quadrature with the line current in order to avoid the depletion of the DC capacitor [76].

- Another important function of the shunt APF is to compensate for the current harmonics drawned by nonlinear loads (including negative and zero sequence). It provides the distorted current component absorbed by the nonlinear load so the current absorbed from the grid is balanced and harmonic free.

- Additionally, the shunt APF can compensate for the reactive power required by the load providing a unity power factor. In certain cases, in order to minimize the rating of the shunt APF the power-factor correction function is performed by a parallel SVC or switched capacitor [77].

The latest trend in shunt APF seems to be to combine it with passive filters, SVC or hybrid filters [16]. In this way, the passive filter takes care of the main known harmonic components (usually the lowest frequencies) and the active filter gets in charge of the rest of the spectrum.

The series-branch is mainly used to avoid voltage perturbations that come from the grid-side and affect the load (i.e. balanced and unbalanced voltage sags, harmonic voltages, unbalanced voltages, voltage flicker). It is used as a DVR with the difference that DVRs do not usually have an active power storage other than the DC capacitor. It can also be used as an harmonic isolator, blocking high frequency harmonic currents that flow from the source [14].

Generally, the series-side is only used at transient states so its service is very limited. For this

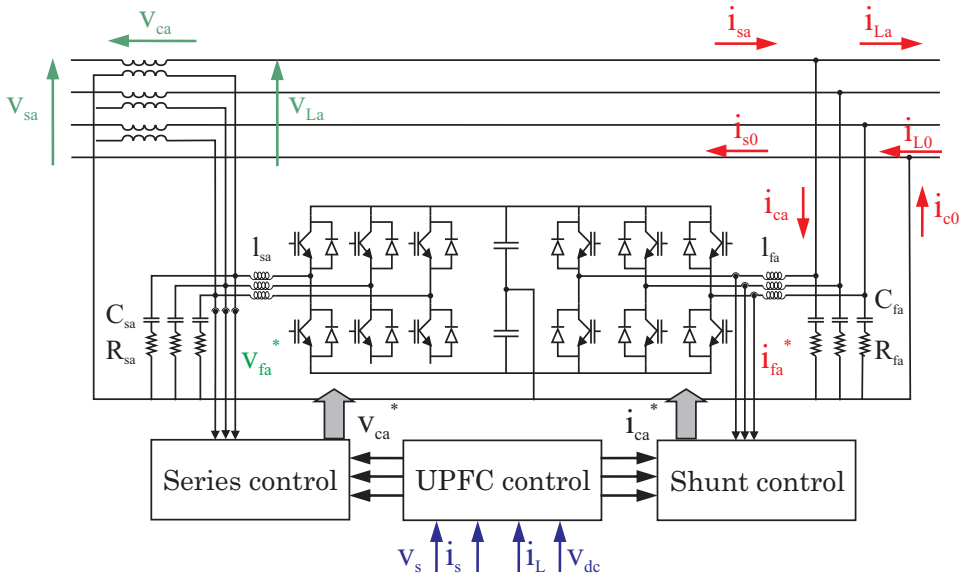


Figure II.2.9: Three-phase four-wire UPQC with DC middle-point connection

reason, some publications study the way of sharing the power-factor compensation function between the series and shunt converters [78].

Inversely to the transmission level, in the LV distribution level there are many nonlinear single-phase loads distributed on four-wire, three-phase systems, such as computers, commercial lightning etc. Hence, active filters can be three-phase 3-wire or three-phase 4-wire. Single-phase loads that are supplied by a three-phase mains with neutral conductor can cause excessive neutral current, harmonic and reactive power burden and unbalance. In those cases, three-phase 4-wire APFs are usually attempted [72]. The fourth wire can be connected to the middle point of the DC-link between two equal capacitors (as shown in Fig.II.2.9) or a fourth converter branch can be added. The three-phase three-wire option of the UPQC can be easily deduced from Fig.II.2.9.

The functions performed by the UPQC are the same as the ones attributed to shunt APFs and DVRs. For this reason, identical perturbation identification and control methods are applied. Most of these methods are mature now (at research level).

Due to space limitation, a deeper development is not provided here, but further information and conceptual studies on UPQC are available at [16, 15, 14, 79, 80, 75]. A review on UPQC control strategies is presented in [81]. A different an creative way of controlling the UPQC is presented in [82] under the name of *iUPQC*, where the shunt-controller is controlled to have an ideal voltage and the series-controller to have an ideal source current.

3. The Unified Power Line Conditioner (UPLC)

The UPLC has basically the same structure and topology as UPQC and UPFC. The difference is that it gathers the fonctionalities of UPQC and UPFC in the same apparatus. In literature, it is

rare to find publications on UPLC and, most of the publications are published by the same authors [14, 16], that were actually who proposed it. Fig.II.2.10 summarizes in a table the most important functions that an UPLC can address.

UPLC	
Series converter	Shunt converter
UPQC	
• Compensation of voltage harmonics, including negative and zero sequences (and voltage flicker) • Compensation of voltage sags • Suppression of harmonic currents through the power line (harmonic isolation)	• Compensation of current harmonics, including negative and zero sequences (and current flicker) • Reactive power compensation • DC-link voltage regulation
UPFC	
• Power flow control • Transient stability enhancement • Dynamic oscillation damping	• Regulation of the terminal voltage of the line, controlled bus (reactive power)

Figure II.2.10: UPLC functions as a combination of UPQC and UPFC

The concept of the UPLC is well explained and developped in chapter 6 of [16] and the interested reader is strongly encouraged to read it. Here, just some rough guidelines are provided. In [16], two possible configurations for the UPLC are evaluated (Fig.II.2.11).

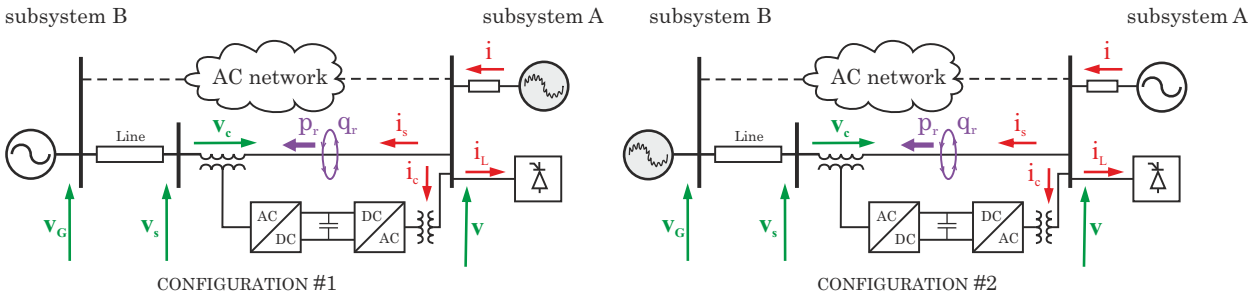


Figure II.2.11: UPLC configurations: # 1 and # 2

One of the configurations, named configuration #1, considers that both the distorted voltage and nonlinear loads are in the same bus. The objective of the shunt converter is then to compensate for the distortion introduced by the nonlinear loads, to correct the power factor, and to keep DC-link voltage constant. The series converter is in charge of guaranteing a distortion-free and balanced voltage at v_s, and of controlling power flow.

The other configuration, named configuration #2, considers that the nonlinear load is close to the shunt-branch and that the distorted voltage is at the other side, in subsystem B. In this case, the shunt converter takes care of the distortion and reactive power consumed by nonlinear loads, and keeps DC-link voltage constant. Thus, the series-side converter is in charge of controlling power

flow and of ensuring a perfect voltage at the load.

It is interesting to note that, when dealing with power-flow control, [14, 16] do not control the power at the other side of the line (v_G) (as it was proposed in section 1. of this chapter) but the power in between v and v_c (check Fig.II.2.11). The author of this PhD believes that this approach is not totally correct because, what it is interesting is to control the power delivered to subsystem B at the point of v_G. It must be accounted that the series compensator will inject/absorb power and that the controlled powers would be modified.

Another aspect not discussed in [14, 16] is the ability of UPLC to compensate for voltage sags. This option is mentioned as a possibility but it is not developped. In this point, it must be mentioned that, in the UPLC, is not evident to compensate for voltage sags using the series compensator.

In a certain way, one could see the UPLC more as a concept than a device with real application potentialities. Actually, in the beginning of this PhD the UPLC was considered as a very interesting device that could be suitable to interconnect MV distribution grids while at the same time tackling power quality problems. However, there are some practical constraints to the association of UPFC and UPQC.

- The UPQC needs a minimal switching frequency to be able to compensate for higher order harmonics. For example, in order to compensate harmonic voltages and currents up to 1 kHz PWM converters with a switching frequency of 10 kHz, or more, are needed [16]. The required high switching frequency limits the use of the UPLC to lower power applications. One interesting aspect to analyse is how to migrate to higher power levels without losing active filtering capability. Probably by optimizing converter topologies (i.e. multilevel) and modulation techniques.

- The UPLC would not be connected at the end of a LV distribution line. The UPLC would be most probably connected between two MV distribution buses. In a MV distribution bus there are several loads connected and, the rating of these loads/generators is usually much higher than those loads connected at LV (e.g. wind farms, arc furnaces). Moreover, the short-circuit impedance at MV levels is substantially lower and the voltage level is higher (kV range). These aspects have a big influence on the rating of the UPLC, which would be relatively high in comparison to a UPQC.

The control approach of [16] is based on p-q theory. PQ theory provides an interesting method for controlling the UPLC. This control theory, however, does have some shortcomings. For example, it uses many low-pass filters, that can give rise to instabilities between control functions and limit the overal dynamics of the device. It is worth mentioning that, the authors of [16], who were at the origin of p-q theories, have made a remarkable work applying these theories to UPLC.

4. The MVDC (Medium voltage Direct Current (AC-DC-AC))

The MVDC is the medium-voltage equivalent of the well-known, HVDC and, as it can be observed in Fig.II.2.12, it has an AC-DC-AC topology. The HVDC is very expanded around the world, with more than 100 projects in operation or in advanced planning stages [17, 18]. MVDC is not as widely used as HVDC but it can be found in some niche applications related to naval industry (in the electrical distribution of boats and in the interconnection of boats to harbour infrastructures [83]). On the contrary to HVDC, MVDC is not currently used for bulk-power transmission or asynchronous interconnections between distribution grids. For this reason, the following lines provide an overview of HVDC considering that the knowledge on HVDC can be further translated to MVDC.

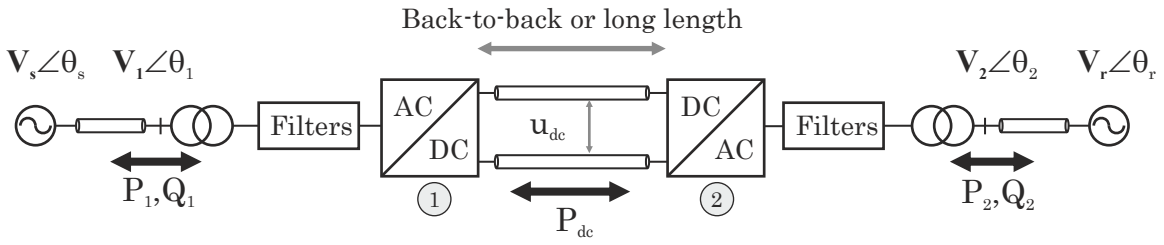


Figure II.2.12: Schematic view of an MVDC

As it often happens with FACTS, two main HVDC technologies are found in the market: line-commutated HVDC and force-commutated HVDC (Fig.II.2.13). Both technologies cohabitate and tackle different power and voltage ratings.

i) **Line-commutated HVDC that use thyristors (CSC-HVDC).** Over the years much experience has been accumulated on CSC-HVDC (also known as *HVDC-Classic*) and it is considered a mature technology for high power (around 1000 MW) installations. So far, the largest construction of the world, the Xiangjiaba-Shangai HVDC, will supply 6400 MW at 800 kV for 2071 km. In spite of their high power and voltage handling capability, they present a series of well known drawbacks:

   – they require a relatively strong synchronous voltage source in order to commutate,

   – the available short-circuit capability at the point of connection should be at least twice the converter rating and,

   – since they consume reactive power they need an external reactive power source (i.e. capacitive bancs) and any surplus or deficit in reactive power must be accomodated by the ac system.

   Nonetheless, an interesting advantage of CSC-HVDC is their natural short-circuit limiting capability due to DC-side inductors.

ii) **Force-commutated VSC that use GTOs, IGBTs or IGCTs (VSC-HVDC).** Since the late 90's VSC-HVDC technology (also known as *HVDC-Light*) is acquiring a lot of interest

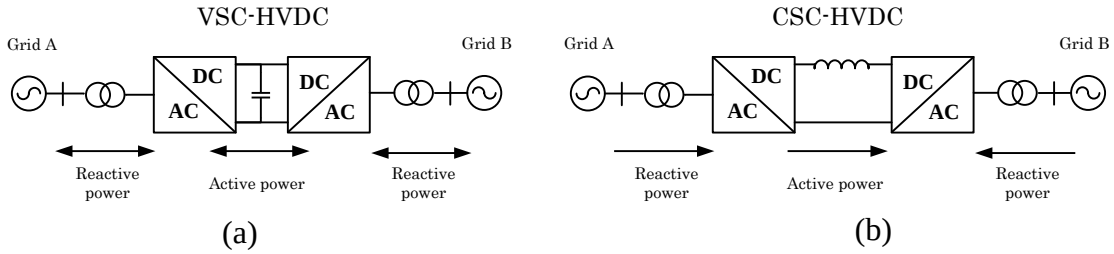


Figure II.2.13: Schematic view of a CSC-HVDC and a VSC-HVDC

because it overcomes many of the drawbacks of CSC-HVDC: (a) it can work in weak-grids, (b) it does not need any reactive power supply, and (c) it can generate active and reactive powers independently [84].

Moreover, their use can be spread to other applications other than bulk-power transmission. Some of these applications include 1) connection of isolated remote loads, 2) power supply to islands, 3) infeed to city centers, 4) remote small-scale generation, 5) offshore generation and deep-sea crossings, and 5) multiterminal systems.

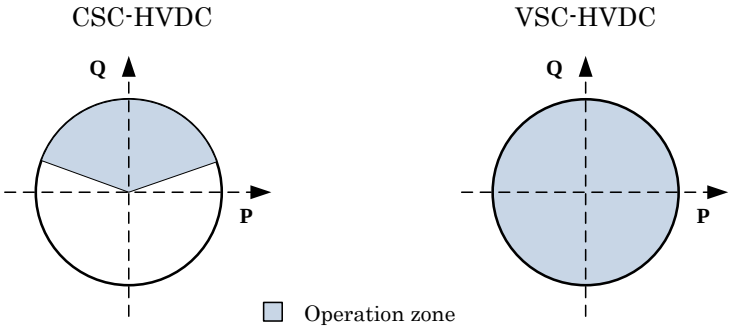


Figure II.2.14: Control areas of CSC-HVDC and VSC-HVDC

As illustrated in Fig.II.2.14, the VSC-HVDC is totally reversible and can attain any of the four PQ quadrants. This constitutes a substantial advantage in comparison with CSC-HVDC (that can not provide capacitive power) or UPFC, which controlable areas change depending on the transmission angle.

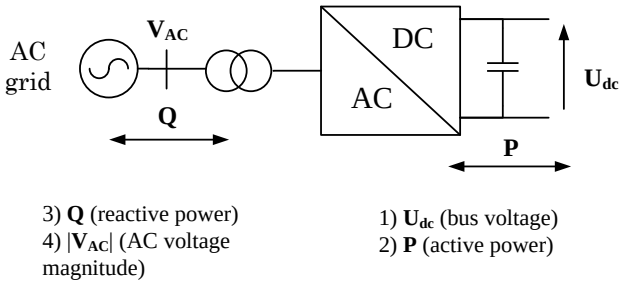


Figure II.2.15: Control objectives of a VSC-HVDC

In a VSC-HVDC operating in a vector-oriented control mode, each of the converters offers two degrees of freedom, which makes a total of four control parameters (Fig.II.2.15):

1. the active power at one of the terminals
2. the voltage magnitude or the reactive power at one of the terminals
3. the voltage magnitude or the reactive power at the other terminal
4. the DC-bus voltage

Together with the STATCOM, the HVDC can be considered as one of the most promising power-electronics devices. This success results from the high flexibility that HVDC presents. Up to now, HVDC is the only existing solution for asynchronous grid interconnection and, for long distance bulk-power transmission, the cost effectiveness of DC transmission is justified above a threshold distance known as *break-even distance*. Moreover, new multilevel voltage topologies, notably modular multilevel topologies (MMC), are facilitating the transition of VSC-HVDC towards higher voltage and power ratings.

Chapter II.3

Comparison betweeen MVDC and UPLC: two candidate devices

The UPLC and the MVDC are two candidate devices for the interconnection of distribution grids. Although other devices such as STATCOMs, SSSCs or PSTs can be selected, in this work the UPLC and MVDC have been prefered because they are static devices that can handle active and reactive power independently.

Both UPLC and MVDC present very good characteristics, and the choice of one topology or the other depends on many different factors. The following section discusses the advantages and disadvantages of each of these apparatus regarding their structure, the characteristics of the interconnection, and the attainable objective functions.

1. UPLC and MVDC: advantages and disadvantages

The advantages and disadvantages are discussed in terms of structure of the apparatus, characteristics of the interconnection, objective functions, and size.

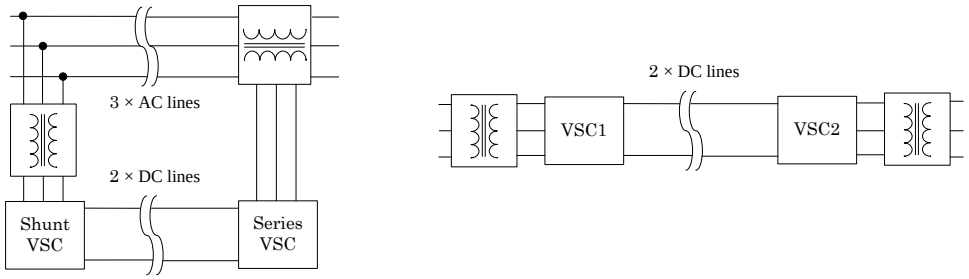
1.1. The structure of the apparatus

- Capacity of separating the converters apart

Regarding the structure of the apparatus, one of the most characteristic differences between MVDC and UPLC is the capacity of separating the converters apart. Theoretically, both devices can either work in back-to-back or *splitted* configuration (when converters are placed at a certain distance one from the other). The MVDC has two DC lines in the intermediate stage while the UPLC presents five lines: 3 AC lines + 2 DC lines (Fig.II.3.1). Obviously, five lines constitute a higher cost than the two lines and thus, in some cases (when the converters are separated and far), the configuration of the UPLC is not cost-competitive.

- Reliability and protection circuits

Reliability and protection circuits constitute another differentiation point between UPLC and MVDC. UPLC offers the possibility of short-circuiting the series device (i) to protect the equipment from high currents, and (ii) to guarantee the continuation of the service even when electronic components come into failure. These protection systems must account for the special particularity



(a) UPLC (b) MVDC

Figure II.3.1: Illustration of *splitted* UPLC and MVDC

of series-connected transformers, which secondary cannot be let in open circuit. The series-connected transformer behaves like a current-transformer and, if the secondary is let open, the magnetomotive force (mmf) becomes unbalanced, the transformer comes into saturation, and the full phase voltage appears accross the secondary winding. An example of a protection circuit placed at the secondary of the series transformer is delineated in Fig.II.3.2.

The MVDC does not offer the possibility of short-circuiting the apparatus so, if a default occurs, the line connection is lost. For this reason, every MVDC device is equipped with redundant components.

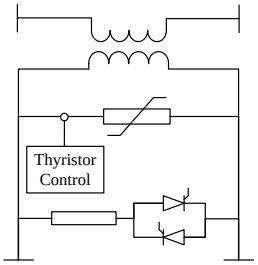


Figure II.3.2: Example circuit of a series protection

- Symmetry and reversibility

The MVDC is symmetric, which means that the device is completely reversible and that power can flow in any of the four PQ quadrants (Fig.II.3.3). On the contrary, UPLC can only reverse power flow if the dimensions of the apparatus are sufficiently large and the transmission angle (θ_0) is small.

-Size

In this manuscript it is assumed that the distance between distribution grids is rather short ($\ll 25\ km$) and that, consequently, devices are connected in back-to-back. The assumption of a back-to-back connection makes it easier to compare the sizing between UPLC and MVDC. Furthermore, the similar topology of the UPLC and the doubly-fed induction generator (DFIG) suggests that there could be a significant size difference between UPLC and MVDC when they are connected back-to-back. In DFIG, the active power flowing through the back-to-back converter is only a small

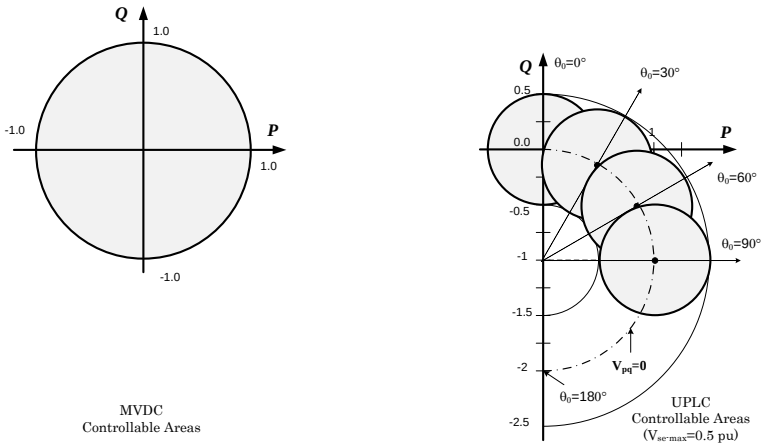


Figure II.3.3: VSC-MVDC and UPLC controllable areas

percentage (around 30%) of the active power flowing through an equivalent fully-fed machine, and it is proportional to the slip. Since the size of the apparatus is a very important parameter, an exercise has been developped in the next section II.3.2. to establish the relative size between both devices.

1.2. Characteristics of the interconnection

Regarding the characteristics of the interconnection, four aspects can be considered: (i) the interconnection distance, (ii) the synchronous/asynchronous nature of the interconnection, (iii) the transmission angle between grids, and (iv) the characteristics of the line/cable.

- Interconnection distance

The interconnection distance constitutes a very important parameter when comparing MVDC and UPFC. In this case, similar issues to HVAC-HVDC apply.

When the interconnection distance is short, and considering that devices are connected in back-to-back, the example of section II.3.2. provides indicative guidelines to choose the apparatus with the lowest sizing. According to this example, for a unity x/r ratio, the size of these devices depends upon the transmission angle. When transmission angles are small, the UPLC requires lower ratings than the MVDC. On the contrary, when transmission angles are high, the MVDC becomes more cost-effective.

When the interconnection distance is long, the comparison between UPLC and MVDC becomes less evident and additional parameters need to be evaluated. For example, when the interconnection distance is long, two options are possible taking into account that UPLC can only be connected back-to-back: (a) to use a back-to-back MVDC, or (b) to split the converters of the MVDC.

The advantages of splitting the converters of the MVDC are the following:

- Both converters can work independently without any communication between them. The UPLC, on the contrary, needs to know the voltage and current information at the receiving-end. The UPLC can get this information directly, by measuring, or by an observer.

- The interconnection is done by two DC cables in stead of three, which means a lower material cost. Moreover, DC cables have lower dielectric losses (due to negligible capacitive leakage current), lower resistive losses (due to the absense of skin effect), and lower Foucault currents in the shield.

- Synchronous/asynchronous nature of the interconnection

The UPLC cannot interconnect asynchronous grids while the MVDC can.

- Transmission angle between grids and characteristics of the line/cable

In the case of the UPLC, the nominal transmission angle between grids establishes the dimensions of the apparatus and the reversibility of the power-flow. The reversibility of the MVDC and its dimensions, however, are independent of the transmission angle.

The impedance characteristics (x/r ratio) and the length of the line/cable influence the dimensions of the apparatus, as it is proven in section II.3.2..

On the other hand, it must be considered that losses in DC lines/cables are generally lower than losses in AC lines/cables. This difference becomes an important parameter when the interconnection distance is long and a splitted configuration is used in the MVDC.

1.3. Objectives and functions

UPLC and MVDC can both control active and reactive powers independently. However, the MVDC is able to work in any of the four PQ quadrants (Fig.II.3.3), while controllable regions of the UPLC depend on the transmission angle and the maximum series injected voltage (Fig.II.3.3). This point represents an essential difference between UPLC and MVDC.

In addition to power flow, UPLC and MVDC may attain power quality enhancement functions. Indeed, their similarity with existing custom-power devices (e.g. STATCOM and DVR) is evident. UPLC can work as an UPQC and the MVDC is like two STATCOMs linked by their DC link. The capability of addressing power flow and power quality functions simultaneously would give an added value to these devices. However, some questions and challenges arise:

- **Apparatus design and sizing challenges**

  On the one hand, a difference must be done between steady-state power quality disturbances and transient events. When it comes to sizing, it is easier to design component ratings for compensating for steady-state phenomena than to design components that need to operate adequately either in steady-state or under transient events. A challenging example, for instance, is the sizing of the series compensator for controlling power flow in steady-state, and

for compensating for voltage sags during transients. In the steady-state the injected voltage is low and thus, DC-link voltage is just a small portion of the grid phase-voltage. However, when a deep voltage-sag occurs, a high DC-voltage is needed in order to inject a high series voltage. Two options can be envisaged:

- **One option** is to always work at a high DC-link voltage. One major shortcoming of this method is that the modulation index in the steady-state is very low, which produces a high THD (total harmonic distortion) at the outputs of the converter and thus, large filters are needed. A solution to this drawback may be to use a multilevel converter with a high definition level. In any case, the series-compensator capacity would be under-used and the components over-dimensioned.
- **The second option** is to work at a low DC-link voltage in the steady-state and to charge the bus voltage as fast as a voltage sag is detected. This option is interesting because it avoids working at a low modulation index during the steady-state. The main drawback of this approach is that the voltage sag must be identified very fast (in some ms) and that bus voltage must be charged fast enough as to compensate for the sag (tenths of ms)).

On the other hand, specificities of power quality compensation approaches must be considered in the design stage. For example, active current filtering is widely used at the low voltage. At low voltage and power ratings, the switching frequency of the converter can be rather high (as high as 10 kHz) because switching losses at those voltage levels are kept in an acceptable range. These high switching frequencies enable the compensation of harmonic frequencies up to 1 kHz [16]. However, in the MV range switching frequencies cannot go as high as 10 kHz because switching losses would be too high. Some authors propose multilevel active power filters in order to obtain a higher equivalent switching frequency at higher voltage levels [85].

- **Dealing with active power components**

  The primary function of the UPLC and the MVDC is to control power-flow. And, in order to perform this function, it is essential to have a stable DC-link voltage without many fluctuations. If power quality compensation is achieved using the shunt-branch (e.g. harmonic current compensation), it must be taken into account that the absorption or injection of active power components will affect the DC-link voltage (and therefore the power-flow control performance). Two possibilities can be considered:

  - The first possibility is to use a large capacitor that does not fluctuate very much when active power components are absorbed/injected. Nevertheless, to over-rate the DC capacitor is not an efficient solution from the weight-volume-cost point of view.
  - The second possibility is to compensate for power-quality phenomena without using active power components, just using the available reactive power. This is the case of STATCOMs or SVCs that are used as voltage regulators.

The abovementioned challenges must be taken into account in order to make a decision on whether it is worth to integrate power-quality and power-flow functions in the same apparatus or not. In many cases, it may be more interesting to have separate apparatus to deal with each of the searched functions.

The following sections discuss the role of UPLC and MVDC regarding some of the most extended power quality perturbations: voltage sag compensation, voltage regulation, flicker, current harmonic compensation and unbalance compensation.

1.3.1. Voltage sag compensation and current limitation

As explained in section A.3., voltage related phenomena can be characterized according to its magnitude and time duration.

Steady-state magnitude deviations in the $90\% - 110\%$ range are considered as voltage variations and, voltage sags are transient deviations of $10\% - 90\%$ from the nominal voltage magnitude for a limited duration of time (< 1 min). When the voltage magnitude goes below 10%, it is considered as an interruption. This classification can be observed in Fig.A.18.

Usually, voltage sags and voltage variations are not compensated in the same way. As discussed in section A.3., voltage sags may be compensated by DVRs and voltage regulation can be done with SVCs or STATCOMs.

In this section, voltage sag compensation and current limitation are grouped together. The reason is that, they are inter-related because a voltage sag produces a current increase and thus, if the voltage sag is compensated, the current is limited.

There are two different points of view when considering voltage compensation. The first method, which can be seen as an *active* approach, aims at restoring the voltage at the connection point. The objective of the second method, which in certain way can be considered *passive*, is to avoid the propagation of the voltage sag through the grid-tie by limiting the current that flows towards the receiving-end.

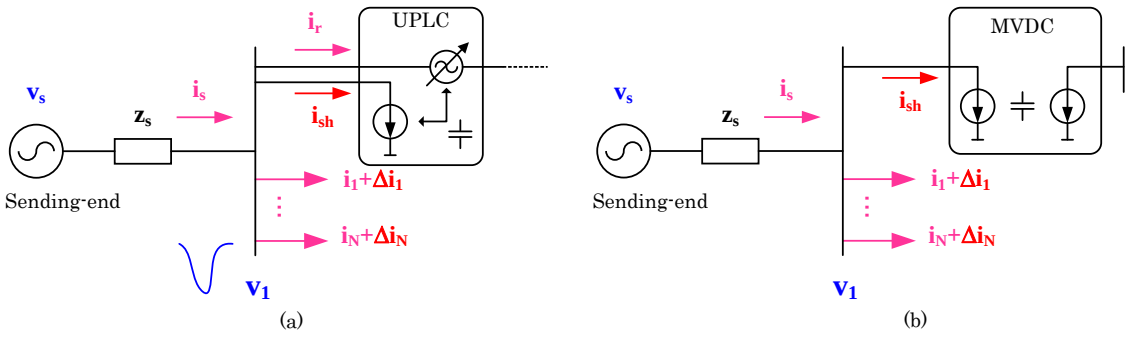


Figure II.3.4: UPLC and MVDC connection to a main feeder

- **Active compensation of voltage sags**

Voltage sags are produced by faults or events such as, motor starts, that consume a current that is 3-10 times higher than the nominal current. This phenomenon can be understood by looking at Fig.II.3.4 and by observing the following expression

$$\mathbf{v_1} = \mathbf{v_s} - \mathbf{z_s}\mathbf{i_s} \tag{II.3.1}$$

The voltage at the connection point $|\mathbf{v_1}|$ depends on the currents consumed by charges and the strength (the magnitude of the source impedance $|\mathbf{z_s}|$) of the upstream grid. When the grid is strong, this is, the value of the short-circuit impedance is low, the voltage at the connection point does not suffer from big deviations when the load current changes. However, when the grid is weak, any variations of currents produce variations of voltage at point 1. Considering load variations as $\Delta\mathbf{i_k}$, the source courrent can be characterized by the expression

$$\mathbf{i_s} = \mathbf{i_{sh}} + \sum_{k=1}^{N} \mathbf{i_k} + \sum_{k=1}^{N} \Delta\mathbf{i_k} \tag{II.3.2}$$

where N is the total number of loads/generators.

Expressions (II.3.1) and (II.3.2) show that, when the shunt current supplied by the UPLC/MVDC is the same as the sum of the variations of load currents but with opposite sign, ($\mathbf{i_{sh}} = -\sum_{k=1}^{N} \Delta\mathbf{i_k}$), the voltage at the connection point $\mathbf{v_1}$ comes back to the nominal value.

These equations proof that it is theoretically possible to use shunt-connected devices to compensate for voltage-sags. However, in most of the cases, the short-circuit currents that create voltage sags are very high and it is not realistic to dimension a static compensator for this purpose. Fig.II.3.5 depicts one of these cases where the short-circuit occurs in one of the neighbouring feeders of the compensating device.

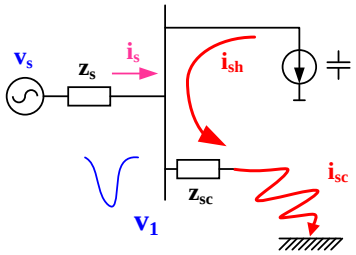


Figure II.3.5: Voltage sag due to a short-circuit in the main feeder

It must be noted that, in the preceeding theoretical development, the current injected by the shunt-branches can be active and/or reactive. Despite the capability of shunt-branches of providing active and reactive power, it is usually preferable to only provide reactive power. This way, DC-link voltage of the compensating device is not compromised. If active power is injected by the shunt-devices, the receiving-end needs to provide it, therefore having an impact on the receiving-end.

Due to sizing constraints, shunt-branches are not adapted for compensating *actively* for voltage sags. Nevertheless, they are very extended for voltage regulation applications where so large current ratings are not required. Moreover, since UPLC just has one shunt-branch, normally, it can only *actively* compensate for voltage sags occuring at the point of the shunt-branch connection. In any case, a solution that consists in using the series-branch of the UPLC as a current source can also be contemplated as an alternative to the aforementioned constraint (Fig.II.3.6). However, from the control point of view, this alternative is only possible if the line is very short and the line impedance values are perfectly known.

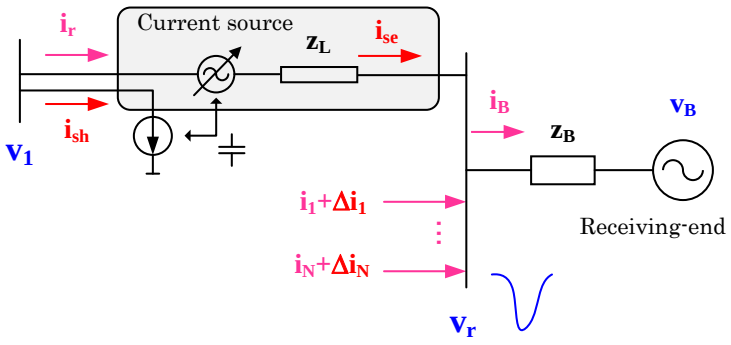


Figure II.3.6: Active voltage sag compensation by the series-branch of the UPLC

On the other hand, the symmetry and splitting capacity of MVDC is a significant advantage in this case, enabling compensation of voltage sags at either side.

- **Blocking of voltage sags**

The second option, before denominated *passive*, consists of making the necessary actions so that the effects of the voltage sag in one of the ends are not felt in the opposite end.

When the device is an UPLC, the action constists in injecting the voltage that makes the current stay in the nominal range, as shown in Fig.II.3.7. If the current before the voltage sag is

$$\mathbf{i_r}^0 = \frac{\mathbf{v_1}^0 + \mathbf{v_c}^0 - \mathbf{v_r}^0}{\mathbf{z_L}} \tag{II.3.3}$$

and the sending-end voltage, for example, suffers a voltage sag ($\Delta\mathbf{v_1}$) such that,

$$\mathbf{i_r} = \frac{\mathbf{v_1} + \mathbf{v_c} - \mathbf{v_r}}{\mathbf{z_L}} = \frac{(\mathbf{v_1}^0 - \Delta\mathbf{v_1}) + (\mathbf{v_c}^0 + \Delta\mathbf{v_c}) - \mathbf{v_r}^0}{\mathbf{z_L}} \tag{II.3.4}$$

from equation (II.3.4) it is deduced that, if $\Delta\mathbf{v_c} = \Delta\mathbf{v_1}$, the current at the receiving-end will remain without any significant variations after the transient period ($\mathbf{i_r} = \mathbf{i_r}^0$).

An attentive look at Fig.II.3.7 shows that the magnitude of the compensating series voltage ($|\mathbf{v_c}|$) is higher than the maximum series voltage represented by the radius of the grey circle. In general, when voltage sags are deep, a large series injected voltage is required. This means that,

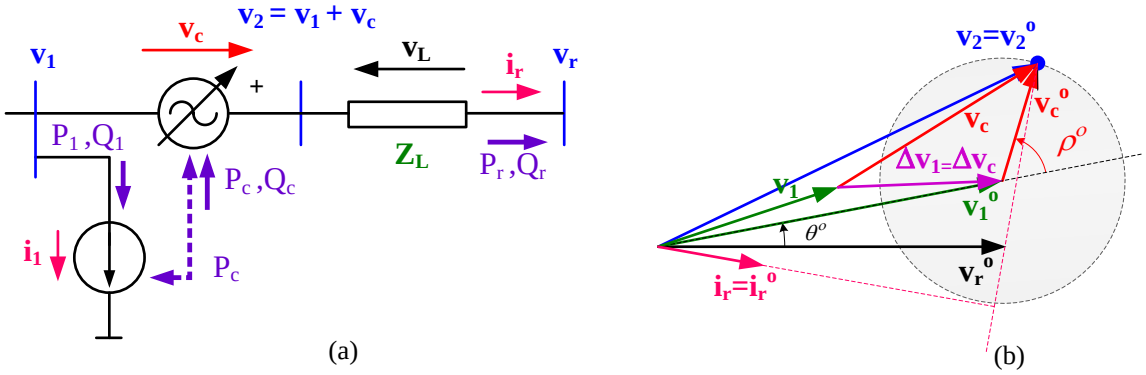


Figure II.3.7: Voltage sag due to a short-circuit in the main feeder

if the current through the interconnection line is to be limited, a large series voltage rating is needed. Nevertheless, the current rating of the series device is not affected very much (except for the transient) since it is kept in between nominal values.

On the other hand, when a voltage sag occurs, the current rating of the shunt-branch ($|\mathbf{i_1}|$) needs to be updated because the injected active power (P_c) increases (due to the augmentation of the injected voltage), the voltage at the connection point ($|\mathbf{v_1}|$) decreases, and the current throught the interconnection ($\mathbf{i_r}$) is kept constant. This statement is justified by the following expressions

$$P_c \uparrow = \Re\{\mathbf{v_{c\uparrow}} \cdot \mathbf{i_{r=}^*}\} = \Re\{\mathbf{v_{1\downarrow}} \cdot \mathbf{i_{1\uparrow}^*}\} \tag{II.3.5}$$

where the values are in per-unit.

When the device is a MVDC, a similar phenomenon occurs. In this case, the active power through the DC-link is kept constant, but the current rating at the sending-end ($|\mathbf{i_1}|$) needs to be increased due to the voltage sag at ($\mathbf{v_1}$). This fact is verified in Fig.II.3.8 and in the following equation

$$P_{dc-link} = \text{const.} = \Re\{\mathbf{v_{1\downarrow}} \cdot \mathbf{i_{1\uparrow}^*}\} \tag{II.3.6}$$

where the losses at the transformer and the filter of the shunt-branch have been neglected and values are expressed in per-unit.

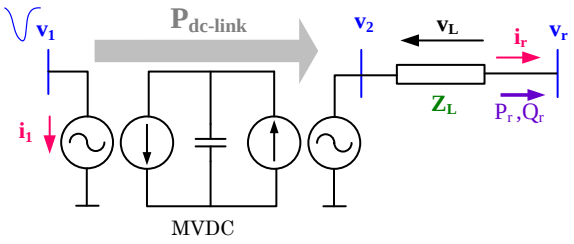


Figure II.3.8: Schematic representation of MVDC when there is a fault in the sending-end

Summarizing, both UPLC and MVDC can compensate for voltage sags. If an *active* compensation approach is selected, the current ratings of the shunt-branches need to be adapted to provide

very high currents. In most of the cases this approach is not feasible, unless the required injection current is found in an acceptable range. Moreover, UPLC can only compensate for voltage sags happening at one of its sides. On the contrary, the selection of a *blocking* approach has two implications: (a) in the case of a UPLC, the voltage rating of the series device and the current rating of the shunt-branch need to be increased, and (b) in the case of a MVDC, the current ratings of both shunt-branches need to be increased.

In any case, the sizing and control of these apparatus when voltage sag compensation capability is included, is rather complex. The design and operation complexity comes from the cohabitation of steady-state power-flow control functions and voltage sag compensation functions. For example, in the case of the UPLC, a higher series injected voltage is needed during voltage sags. This means that the required DC voltage during sag conditions is also higher. Two possibilities can be previewed: (i) to work always at a higher DC voltage, which implies that the modulation index at steady-state is lower and thus, the THD_v index increases, or (ii) to charge the DC-link voltage as soon as a voltage sag has been identified, which may not be sufficiently fast.

1.3.2. Voltage regulation

Voltage regulation is based on the same concept as *active* power compensation. The only difference lies in the magnitudes of voltage deviations that, in this case, are much lower than the magnitudes of voltage sags (in the $\pm 10\%$ range). This concept will not be further developped here because it has already been addressed in the earlier section but, it must be highlighted that voltage regulation by means of FACTS or d-FACTS devices is a very common and extended function worldwide.

1.3.3. Flicker, harmonics, and unbalance compensation

Flicker is an impression of fluctuating brightness from a light source due to low frequency variations (around 8 Hz) in the supply voltage. Flicker is created by an amplitude modulation of the supply voltage caused, in turn, by an amplitude modulated current produced by repetitive processes such as electrical arc furnaces, welding machines, wind turbines, heat pumps, and air compressors, to mention a few.

Current harmonics are those current components that oscillate at multiples of the grid frequency. Current harmonics are produced by nonlinear loads and devices and they interact with the system impedance distorting the voltage wave. According to the standard EN 50160, total harmonic distortion must be below 8% ($THD_v < 8\%$) in distribution systems with voltages below $35kV$ [86].

Unbalances are caused by an uneven three-phase current consumption. Standard EN 50160 limits voltage unbalance to 2% (negative sequence to positive sequence component ratio) for normal systems.

Flicker, harmonics and unbalances can be compensated by the shunt-branches of the UPLC and MVDC in a similar manner as voltage sags. As it is depicted in Fig.II.3.9, the shunt current

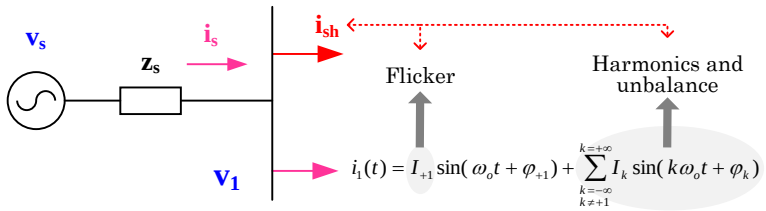


Figure II.3.9: Flicker, harmonics and unbalance compensation by means of a shunt-device

must compensate for every current distortion that deviates from a pure sinusoidal wave. This is done by injecting the same amount of distortion as the load generates. In this way, the voltage at the PCC is not perturbated.

As it has been mentioned before, it is preferable that the shunt compensator only injects reactive power not to affect DC-voltage. It is nevertheless possible to inject active power if this action is considered in the converter control and knowing that it will have an influence on the receiving-end.

Table II.3.10 summarizes all the concepts compared above. As it can be observed, the choice between UPLC or MVDC depends on the particular characteristics of the application and the location of the apparatus. In general terms, MVDC offers a better flexibility than UPLC due to its symmetry and natural decoupling capabilities. However, under certain conditions (small phase-difference between interconnection points), UPLC may be more cost-effective than MVDC. Moreover, it offers the possibility of short-circuiting the series-side.

Regarding simultaneous power-flow and power-quality control capabilities, it can be concluded that, theoretically, it is possible to join several functionalities together. However, it requires a complex design (e.g. dimensioning) and control.

2. Size comparison between MVDC and UPFC: an indicative case

The earlier section has evaluated the advantages and disadvantages of UPLC and MVDC according to different aspects. It is clear that, an essential parameter when choosing between UPLC and MVDC is size, and therefore, cost. An exhaustive comparison between ratings of UPLC and MVDC is complicated to perform because the size of an apparatus depends on the particular topology of the apparatus, the characteristics of the components, and the used control strategy.

In this section, and indicative size relationship between UPLC and MVDC is proposed, based on active powers flowing through the DC-links of UPLC and MVDC. The active power flowing throught the DC-link is chosen as an indicator because the DC-link power establishes the minimum rating requirement for converters and transformers. This minimum rating can be increased by additional reactive power or power quality requirements.

Of course, the DC-power ratio is an indicator of the size relationship between UPLC and MVDC, and needs to be considered as a relevant feature. Nevertheless, it is not the only condition to evaluate. Another relevant aspect, for example, is the use of a series transformer in the UPLC,

	Features	UPLC	MVDC
Structure	Capacity of separating converters	Possible to split converters but not cost-effective. 3 AC lines + 2 DC lines (5 lines) are needed. In reality, only back-to-back application.	Possible to split converters Only 2 DC lines are needed Two possibilities: back-to-back and splitted
	Protection circuits and reliability	Possible to short-circuit the series device with a protection system. The line is not lost in case of a failure. Care must be taken with the series transformer.	Not possible to short-circuit the apparatus Redundancy is needed if continuation of service is required
	Symmetry and reversibility	Not symmetric. Reversibility depends on transmission-angle and maximum series injected voltage.	Symmetric 4 quadrants operation: reversibility does not depend on transmission angle
Characteristics of interconnection	Interconnection distance	If distance is short and a back-to-back configuration is chosen, the size of the apparatus depends upon the transmission angle and the x/r ratio. For a x/r=1, the UPLC is smaller than the MVDC provided that transmission angle is also small. If the distance is long, the evaluation is more difficult because: ➢ UPLC cannot be splitted appart. ➢ MVDC can be splitted appart: (i) there is no need of communication between converters, (ii) there are just 2 lines instead of 5.	
	Synchronous or asynchronous connection	Only synchronous interconnection.	Synchronous and asynchronous interconnection.
	Transmission angle	In general, if the transmission angle and the interconnection distance are small, the UPLC is smaller than the MVDC. The UPLC is reversible depending on the transmission angle.	The reversibility of MVDC is independent of the transmission angle (4 quadrant operation).
	Line/cable characteristics	AC cables have higher losses than DC cables (skin effect, Foucault currents in the shield, capacitive leakage currents ...)	
Objective functions	Power flow	Reachability areas depend on the transmission angle and the maximum series injected voltage.	4 quadrant operation.
	Voltage sag compensation	If an active compensation strategy is chosen: ➢ A higher current rating is needed in the shunt-branch. ➢ Reactive current injection is prefered (not to affect DC-link voltage). ➢ For voltage sags in the receiving-end, the series-branch can be used as a current source (but this option is more complex). If a passive compensation is chosen: ➢ The voltage rating of the series device and the current rating of the shunt device need to be updated.	If an active compensation strategy is chosen: ➢ an extremely high current rating is needed in the shunt-branches. ➢ Reactive current injection is prefered (not to affect DC-link voltage). ➢ Shunt-branches can be used for compensation at both sides. If a passive compensation is chosen: ➢ The current rating of the shunt devices need to be updated.
	– Voltage regulation – Flicker, harmonics and unbalance compensation	The same considerations as for active voltage-sag compensation apply but, the current ratings are expected to be lower.	
Size		The size of the apparatus depends on various parameters: ➢ The interconnection distance. ➢ The use of a back-to-back or a splitted configuration. ➢ The transmission angle. ➢ The nature of the interconnection lines/cables. In the particular case of a back-to-back topology in a short distance interconnection, and with a unity x/r ratio, the UPLC is smaller than the MVDC for small transmission angles.	

Figure II.3.10: UPLC and MVDC comparative table

which dedicated design requirements and special protections imply a non negligible cost.

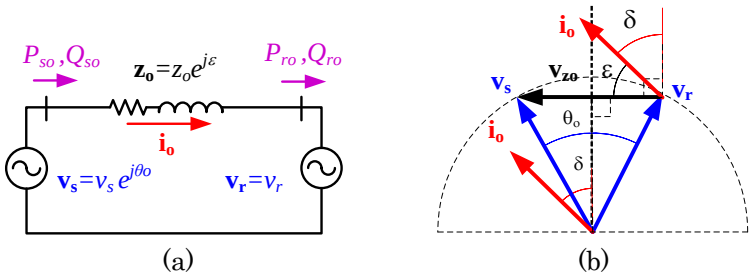


Figure II.3.11: Base case representation

The following lines present a simplified analytical study that will provide guidelines to help with the selection between MVDC and UPLC. This study, however, must be considered as a particular example that highlights some important trends.

1. The proposed analysis begins defining a base-case. The base-case represents the interconnection of two distribution grids by a lumped RL line when the apparatus is inactive, as shown in Fig.II.3.11. The base-case provides the natural active and reactive power-flows (P_{so}, Q_{so}, P_{ro} and Q_{ro}) for each couple of transmission-angle (θ_0) and x/r ratios.

2. The next step is to define the objectives that power-flow controllers must achieve, assuming that they are placed in the middle of the interconnection line. The choice of a middle-point location is arbitrary but it does not change the main conclusions obtained at the end of the procedure. Notwithstanding, the location of the apparatus has and influence on the undefined areas that are further explained in paragraph II.3.2.5.1..

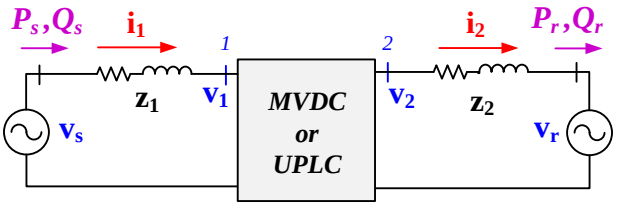


Figure II.3.12: Single-phase diagram of a MVDC/UPLC placed at the middle of the interconnection line

Since each of the converters has two degrees of freedom (i.e. magnitude and angle of the output voltage), four objectives can be addressed in total: v_{dc}, P_r, Q_r and Q_s.

As it can be observed, the fact of fixing the objectives in a particular way, limits the generality of the exercise, but it is sufficiently representative to extract general conclusions on the size difference of both apparatus. Considering these objectives, interesting results have been obtained by evaluating a series of scenarios in which the value of k (where $P_r^* = k \cdot P_{r0}$), the transmission-angle (θ) and the x/r ratio are changed.

The following sections provide a detailed explanation of the followed procedure.

2.1. Base-case description

Fig.II.3.11(a) depicts the selected base-case, where $\mathbf{v_s}$ represents the sending-end voltage phasor, $\mathbf{v_r}$ represents the receiving-end voltage phasor, and $\mathbf{z_0}$ stands for the lumped (RL) impedance of the interconnection. Note that bold symbols stand for vectors. The base-impedance can be characterized in terms of the magnitude (z_0) and the load impedance-angle (ϵ) or load-angle (δ). The relationship between ϵ and δ is $\epsilon = pi/2 - \delta$, where $\epsilon = \arctan(X/R)$ and $\delta = \arctan(R/X)$. The vector-diagram of a general base-case is shown in Fig.II.3.11(b).

The expressions of the active and reactive powers in the base-case are common expressions that can be found in any power system text-books:

$$P_{r0} = \frac{v_r}{z_0}[v_s \sin(\theta_0 + \delta) - v_r \sin\delta] \tag{II.3.7}$$

$$Q_{r0} = \frac{v_r}{z_0}[v_s \cos(\theta_0 + \delta) - v_r \cos\delta] \tag{II.3.8}$$

2.2. MVDC model

As it is observed in Fig.II.3.13, the MVDC decouples the line into three sub-circuits. The intermediate sub-circuit, corresponding to the DC-link, establishes a connection between the other two sub-circuits. Under a no-loss assumption, active powers coming in and out of terminals 1 and 2 of the MVDC are the same, which simplifies the calculation of unknown voltages $\mathbf{v_1}$ and $\mathbf{v_2}$. These two voltages can be calculated by analyzing each of these subcircuits.

The first step is to calculate $\mathbf{v_2}$ and $\mathbf{i_2}$ based on given reference powers $P_r{}^*$ and $Q_r{}^*$. Subsequently, the knowledge of $\mathbf{v_2}$ and $\mathbf{i_2}$ leads to P_2 and, since $P_1 = P_2$, P_1 is automatically deduced. Then, it is just a matter of resolving the sending-end sub-circuit and calculating for $\mathbf{v_1}$ and $\mathbf{i_1}$.

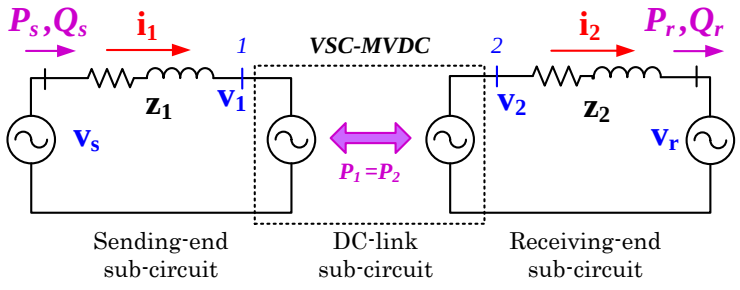
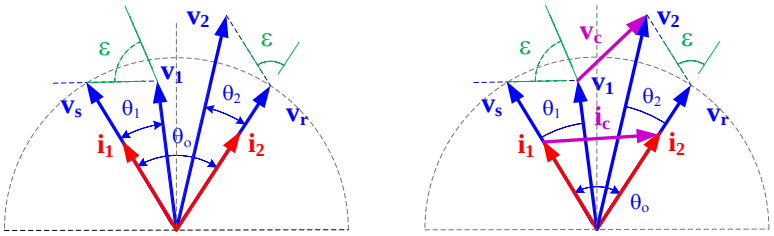


Figure II.3.13: Single-phase diagram of a MVDC placed at the middle of the interconnection line

2.2.1. Receiving-end sub-circuit

In the receiving-end sub-circuit two unknown variables need to be found: $\mathbf{v_2}$ and $\mathbf{i_2}$ (see Fig.II.3.14(a)). These values are obtained by solving the following equation system:

$$\begin{cases} P_r = \mathfrak{Re}\{\mathbf{v_r}\mathbf{i_2}^*\} \\ Q_r = \mathfrak{Im}\{\mathbf{v_r}\mathbf{i_2}^*\} \\ \mathbf{v_2} - \mathbf{z_2}\mathbf{i_2} = \mathbf{v_r} \end{cases} \tag{II.3.9}$$



(a) MVDC (b) UPLC

Figure II.3.14: Vector diagrams of MVDC and UPLC

2.2.2. DC-link sub-circuit: transfer of active power

The DC-link interconnects the sending- and the receiving-end subcircuits and, if internal losses of MVDC are neglected, the active power coming in and out of the MVDC is kept constant. The relationship is formally written as:

$$\begin{cases} P_2 = \mathfrak{Re}\{\mathbf{v_2}\mathbf{i_2}^*\} \\ P_1 = P_{dc_m vdc} = P_2 \\ P_1 = \mathfrak{Re}\{\mathbf{v_1}\mathbf{i_1}^*\} \end{cases} \tag{II.3.10}$$

2.2.3. Sending-end sub-circuit

The procedure to find $\mathbf{v_1}$ is similar to that used to calculate $\mathbf{v_2}$. The only difference is that the powers objectives are not located at the same point. The power references are $P_1{}^*$ (that is calculated previously) and $Q_s{}^*$. Thus, the equation system to solve is:

$$\begin{cases} P_1 = \mathfrak{Re}\{\mathbf{v_1}\mathbf{i_1}^*\} \\ Q_s = \mathfrak{Im}\{\mathbf{v_s}\mathbf{i_1}^*\} \\ \mathbf{v_s} - \mathbf{z_1}\mathbf{i_1} = \mathbf{v_1} \end{cases} \tag{II.3.11}$$

The solutions of the equation system (II.3.11) are not single, there are two sets of solutions. Both sets of solutions must be evaluated and it must be decided whether the results are reasonable or not (physically feasible solutions, real numbers ...). When faced to two feasible results, a possible criterion can be to choose the value of $\mathbf{v_1}$ that makes the apparent power at point 1 minimum.

Sometimes, the equation set (II.3.11) does not have a solution. Then, it is said that an *undefined area* has been found. This issue is further discussed in section II.3.2.5.1..

When the apparatus is directly connected at the sending-end, the above equation system becomes:

$$\begin{cases} \mathbf{v_s} = \mathbf{v_1} \\ P_1 = P_{dc_m vdc} = P_s = \mathfrak{Re}\{\mathbf{v_s}\mathbf{i_1}^*\} \\ Q_s = \mathfrak{Im}\{\mathbf{v_s}\mathbf{i_1}^*\} \end{cases} \tag{II.3.12}$$

In this particular case, the apparatus is connected to a stiff source and thus, undefined areas do not appear.

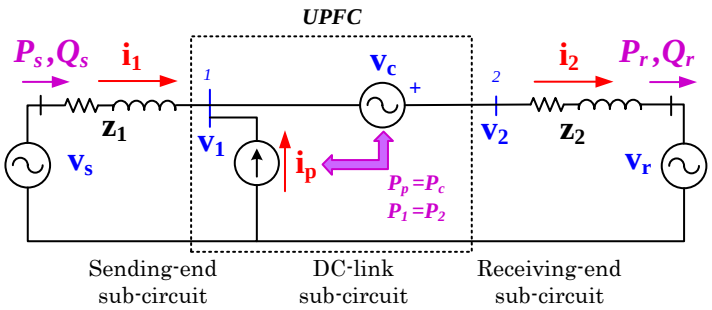


Figure II.3.15: Single-phase diagram of a UPLC placed at the middle of the interconnection line

2.3. UPFC model

Similar to the MVDC, the UPLC can also be divided into three-subcircuits, as illustrated in Fig.II.3.15. The intermediate sub-circuit presents changes in comparison to MVDC, but the sending- and receiving-end subcircuits are the same.

In the intermediate subcircuit, the voltage injected/absorbed by the series compensator ($\mathbf{v_c}$) is the difference between $\mathbf{v_2}$ and $\mathbf{v_1}$ and, the current provided/sinked by the shunt branch is the difference between $\mathbf{i_2}$ and $\mathbf{i_1}$.

$$\begin{cases} \mathbf{v_c} = \mathbf{v_2} - \mathbf{v_1} \\ \mathbf{i_p} = \mathbf{i_2} - \mathbf{i_1} \end{cases} \tag{II.3.13}$$

where the calculation of $\mathbf{v_2}$, $\mathbf{v_1}$, $\mathbf{i_2}$ and $\mathbf{i_1}$ is the same as MVDC.

2.4. DC-power ratio calculation and installed apparent power

The size difference between the MVDC and the UPLC is determined by the ratio between the active powers that flow through the DC links of the MVDC and the UPLC as described by the following expression:

$$\text{DC-power ratio} = \frac{P_{dc-MVDC}}{P_{dc-UPLC}} \tag{II.3.14}$$

In fact, DC power is selected because it establishes the minimum power requirement of devices independently of their reactive power and power quality needs.

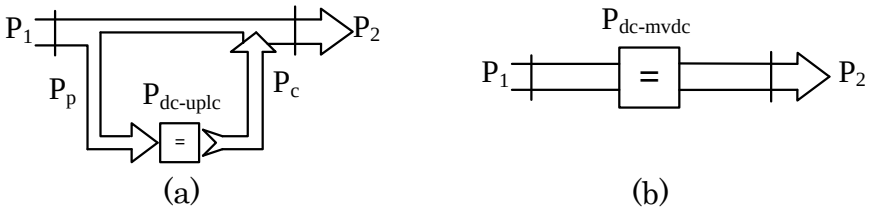


Figure II.3.16: Active power tranfer in UPLC

Fig.II.3.16(a) illustrates that the active power flowing through the DC-link of the UPLC ($P_{dc-UPLC}$) is the active power injected/absorbed by the series converter. This power is, indeed, provided/consumed by the shunt converter. So, depending on the phase separation between $\mathbf{v_1}$ and $\mathbf{v_2}$ and the x/r ratio, $P_{dc-UPLC}$ takes different values.

The active power flowing through the DC-link of the MVDC ($P_{dc-MVDC}$) is equal to the transmitted active power at terminal 1 (P_1). This means that, all the active power transmitted towards the receiving-end will cross the converters and transformers of the MVDC (Fig.II.3.16(b)).

At a first sight, one could say that $P_{dc-UPLC}$ is lower than $P_{dc-MVDC}$, thinking that it is only a part of the whole transmitted power, as shown in Fig.II.3.16. However, the following example will proof that this is only the case under certain conditions. In order to unveil these conditions, a numerical example is proposed next.

2.5. A numerical example

The present example offers an insight of the size proportion of the two devices and some of the operational limits that may be encountered.

Each of the evaluated apparatus offers four degrees of freedom (two per converter), which enables the control of four objectives (Fig.II.3.17). In this particular example, the four objectives have been chosen as follows

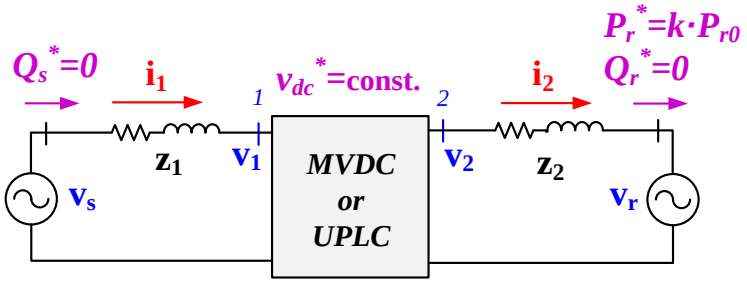
1) $P_r{}^* = k \cdot P_{r0}$. The function of coefficient k is to modulate the active power reference at the receiving-end. It multiplies P_{r0}, which is the active power that flows towards the receiving-end

when no apparatus is connected.

2) $Q_r{}^* = 0$. The reactive power at the receiving-end is chosen to be null, providing a unity power factor.

3) $Q_s{}^* = 0$. The sending-end reactive power is chosen to be null, yielding a unity power factor.

4) $v_{dc} = \{\text{const.}\}$. The fourth objective is transparent in this exercise and it consists of maintaining the DC-link voltage constant.



Numerical example

Figure II.3.17: Representation of the numerical example with the fixed objectives

In order to work with a normalized system, all the values have been transformed to per-unit values (represented by lower case symbols). The base-values used to convert the system are $V_{base} = V_r = V_s$ and $Z_{base} = Z_0$. The voltage magnitudes at both ends (V_r and V_s) and the impedance magnitude (Z_0) are considered to be constant. Moreover, for the ease of calculations, this exercise considers a single-phase system.

The exercise constists in calculating the DC-power ratio (DC-power ratio $= P_{dc-MVDC}/P_{dc-UPLC}$) in different scenarios. These scenarios are defined by the values of the transmission angle (θ), the x/r ratio, and the value of the k coefficient). Observe that, there is a different base case for each value of x/r and θ_0.

But, before going further with the example, it is important to explain a phenomenon that limits the value of k to a specific range: the existance of undefined areas. For certain values of k (and in certain θ_0 and x/r conditions) it is not possible to resolve the sending-end sub-system: it has no solution. This is called an undefined area. This means that it is not possible to choose arbitrary values of k, they need to be in an admissible range.

2.5.1. Undefined areas

The existence of undefined areas is also reported in [87], where a physical explanation to this phenomenom is provided. According to [87], undefined areas exist because it is not possible to transmit random power values through the system. Under certain conditions, terminal 1 cannot provide the required P_{dc} to terminal 2. The authors of [87], have also checked the influence of the

location of the UPLC in the formation of undefined areas, concluding that, if the UPLC is connected to a stiff system (if $\mathbf{z_1} = 0$), undefined areas do not appear.

Fig.II.3.18 depicts the frontier values of k (k_{max}) in terms of θ_0 and x/r. The undefined areas are those above and below the curves that stand for each x/r ratio. The two thick blue lines envelope all the x/r curves. This means that, above and below these curves solutions do not exist for x/r ratios in the $0 \leq x/r \leq +\infty$ range. The illustrated x/r ratios correspond to some characteristic overhead-line types: $x/r = +\infty$ represents a purely reactive line, $x/r = 10$ represents a typical transmission line, $x/r = 1$ represents a typical distribution line, and $x/r = 0$ represents a purely resistive line. A capacitive behaviour of the line has not been simulated.

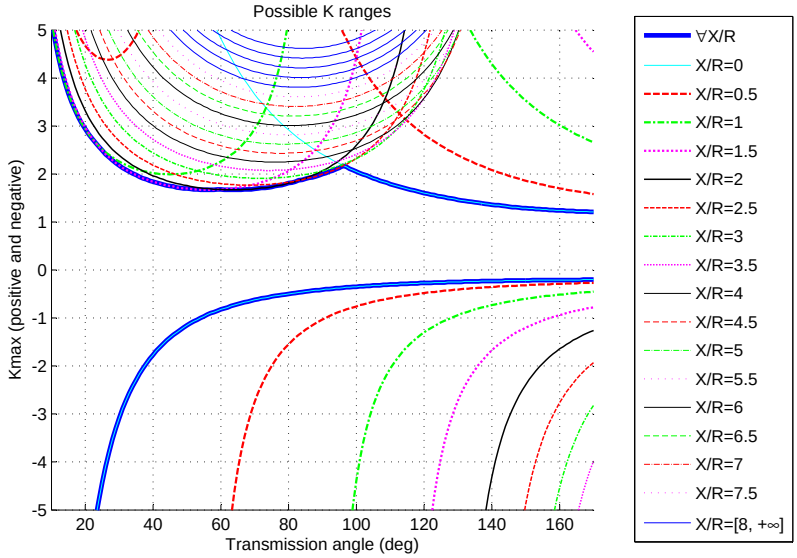


Figure II.3.18: Admissible k ranges

Fig.II.3.18 testifies that k cannot take any arbitrary values because there is a risk of finding an undefined zone. Some indicative k ranges for low values of x/r are:

- For $x/r \geq 0$, $-0.2 \leq k \leq 1.2$.
- For $x/r \geq 0.5$, $-0.27 \leq k \leq 1.6$.
- For $x/r \geq 1$, $-0.45 \leq k \leq 2.6$.

2.5.2. Results

For x/r values above unity, it is feasible to use positive k values as high as 2.6. In this exercice, k has been chosen to be 1.5 arbitrarily, meaning that the active power flowing throught the receiving-end will be 50% higher than it was without any compensation. After several iterations with diverse positive x/r ratios and transmission angles ranging from 10° to 170°, Fig.II.3.19 is obtained. As it was mentioned in section II.3.2.2.3., the solutions of the receiving-end subcircuit are double and, if

both solutions are rational, a criterion must be selected to choose between them. In this case, the solution that minimizes the absolute value of the apparent power at terminal 1 ($\min\{|S_1 = v_1 \cdot i_1|\}$) has been selected.

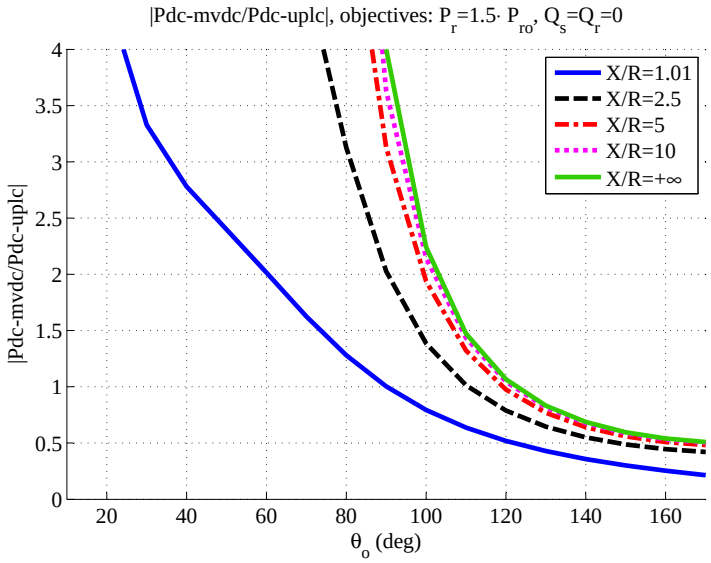


Figure II.3.19: $|P_{dc-MVDC}/P_{dc-UPLC}|$ ratios for $k = 1.5$

The curves of Fig.II.3.19 show that, for values $x/r \geq 1$, provided that the transmission angle is kept below 90 degrees, the relative size of the UPLC is smaller than the MVDC. When $x/r = 1$ and $\theta_0 = 90°$, $|P_{dc-MVDC}/P_{dc-UPLC}| = 1$. But, when $x/r = 1$ and $\theta_0 = 60°$, $|P_{dc-MVDC}/P_{dc-UPLC}| = 2$, which means that the relative dimension of the MVDC doubles the UPLC.

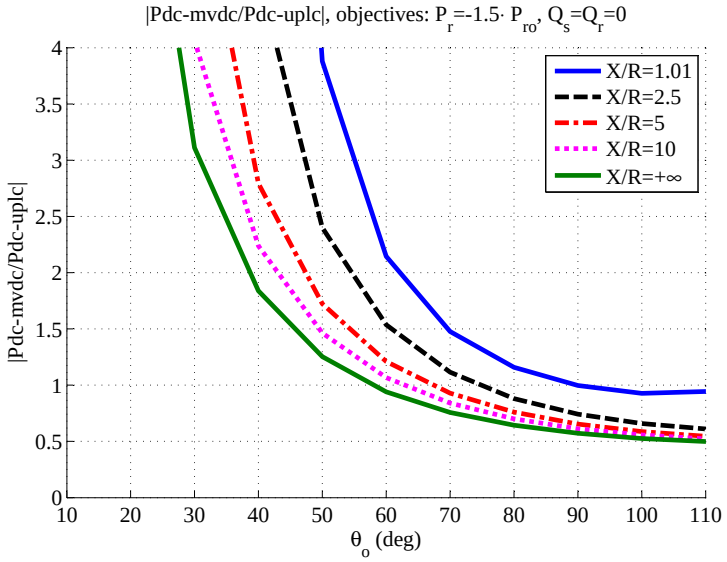


Figure II.3.20: $|P_{dc-MVDC}/P_{dc-UPLC}|$ ratios for $k = -1.5$

The above developments have demonstrated that, for positive values of k there is a limit θ_0 angle

above which the MVDC is smaller than the UPLC. The same trend is followed for negative values of k. For example Fig.II.3.20 displays the results corresponding to $k = -1.5$ and transmission angles between 10 and 110 degrees (in this case it is not possible to go beyond 110 degrees for $x/r = 1$ because solutions do not exist).

This experience has proven that the value of the nominal transmission angle (θ_0) between grids and the x/r ratio determines, to a great extent, the size relationship between UPLC and MVDC. The next sections will address this issue, discussing the value of the transmission angle betweeen two distribution grids and typical x/r ratios of over-head lines and cables.

3. Transmission angle between two MV distribution grids

The phase-angle difference between two distribution grids is discussed based on Fig.II.3.21. Fig.II.3.21 is a simplified representation of two radial distribution networks that are connected to the same sub-transmission substation ($\mathbf{v_s}$). The transformers, lines, and cables that are found between the upperstream voltage source ($\mathbf{v_s}$) and the interconnection points ($\mathbf{v_1}$ and $\mathbf{v_2}$) are modeled by two lumped impedances ($\mathbf{z_1}$ and $\mathbf{z_2}$). It must be noted that, for simplicity, in the vector diagrams, a pure reactive impedance has been considered.

The voltage (magnitude and phase) at each connection point depends on the equivalent impedance between the voltage source and the connection point (magnitude and angle), and on the current that is absorbed/injected at the connection point as in

$$\mathbf{v_1} = \mathbf{v_s} - \mathbf{z_1} \cdot \mathbf{i_1} \text{ , and } \quad \mathbf{v_2} = \mathbf{v_s} - \mathbf{z_2} \cdot \mathbf{i_2} \tag{II.3.15}$$

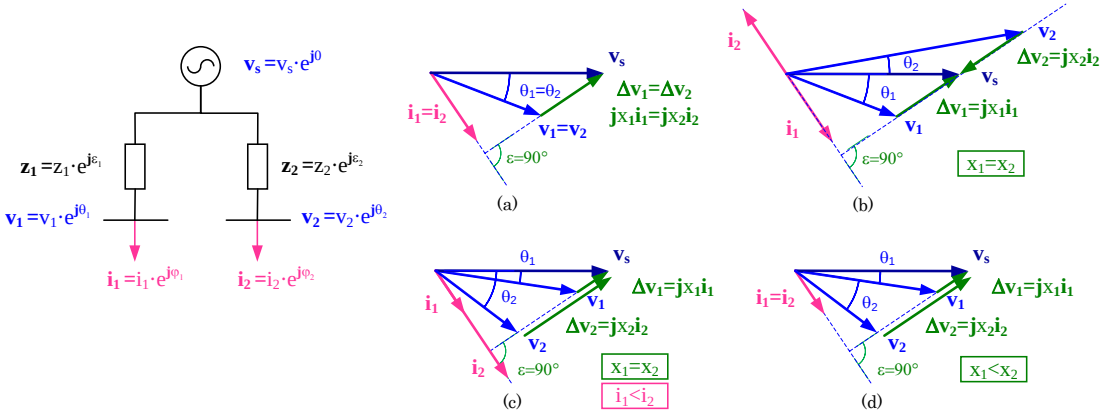


Figure II.3.21: Voltage and phase angle difference in two radial branches

The following conclusions can be extracted:

i) If both branches are equal, this is, $\mathbf{z_1} = \mathbf{z_2}$ and $\mathbf{i_1} = \mathbf{i_2}$, then the phase difference is null.

This situation is depicted in Fig.II.3.21(a). This case is an ideal case, but it can happen that both branches and their loading level are quite similar. In that case, the phase difference ($\Delta\theta = \theta_1 - \theta_2$) may not be large.

ii) If one of the branches is much loaded than the other one (considering that current just changes in magnitude), or if one of the impedances is higher than the other one (also in magnitude), a phase-angle difference will appear. This situation is depicted in figures Fig.II.3.21(c) and Fig.II.3.21(d) and, the bigger this difference is, the bigger the phase displacement will be.

iii) The phase angle of the currents also has an impact of the transmission angle between interconnection points. For example, in Fig.II.3.21(b), the current of branch 1 behaves as a load, while the current of branch 2 behaves as a generator. This is one of the worst cases regarding phase difference.

The forementioned conclusions are just qualitative considerations that discuss the influence of differential loading and impedance on the phase-angle between two connection points. However, they do not quantify the phase-angle in between two MV distribution grids. It is actually not possible to provide a precise phase-angle range for a generic case because it can have a large deviation from case to case. Nonetheless, some examples, based on a MV distribution network benchmark model proposed by the CIGRE Task Force C6.04.02 [88, 89] are proposed next. The proposed benchmark and the slightly modified version are further described in appendix D.

- The **first example** (Fig.II.3.22) shows the base-case (case 0), which has no dispersed generation and nominal load values. As it can be observed, the phase-difference between nodes 2 and 8, is not even of 1 degree ($\theta_2 - \theta_8 = -0.8$).
- In the **second example** (case 1) a 20 MW load, such an arc furnace or similar, has been installed in bus 8. This large load slightly saturates the transformer between lines 1-8 and increases the angle difference between nodes 2 and 8 to around 3.4 degrees ($\theta_2 - \theta_8 = 3.4$ and $\theta_2 - \theta_{10} = 3.52$).
- The **third example** (case 2), which is not too realistic but gives an idea of the phase-difference, consists in connecting the 20 MW load at bus 10 (at the end of the grid). In this case, the largest phase-difference is obtained: $\theta_2 - \theta_8 = 8.43$ and $\theta_2 - \theta_{10} = 16.69$. It is also observed that the transmission lines, cables and transformers in the path are all extremely overloaded.
- Finally, the **last example** (case 3) represents the case when, a 20 MW industry is connected in bus 8 and, in the same time, a wind-farm of the same size is connected in bus 2 (assuming unity power factor). In this example the phase-difference attains values around 7 degrees: $\theta_2 - \theta_8 = 7.51$ and $\theta_2 - \theta_{10} = 7.63$

According to these particular examples the phase displacement from bus 2 to 8 is kept well below 90 degrees even in case 3, when a large industry is connected at the end of a very low capacity line.

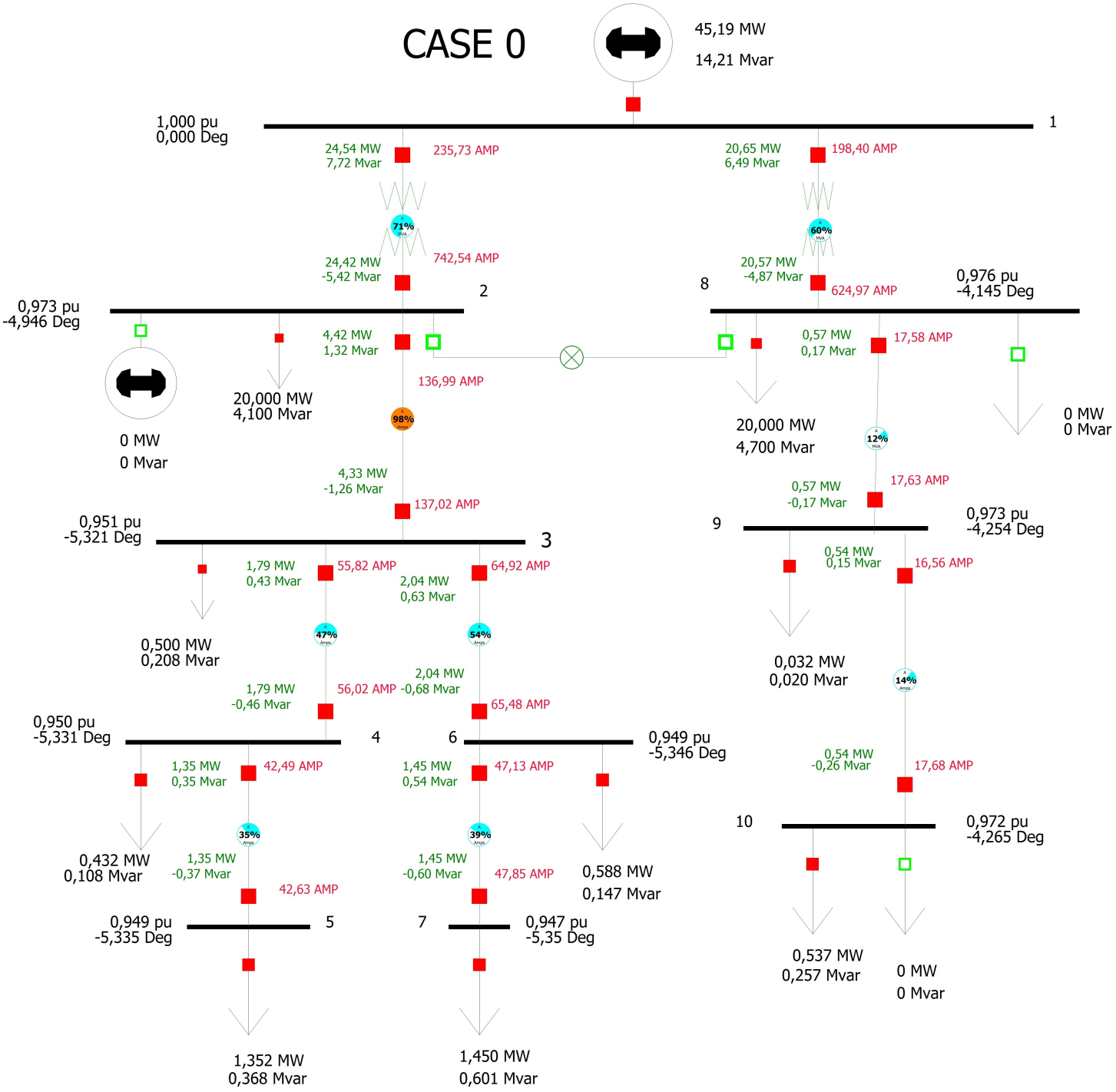
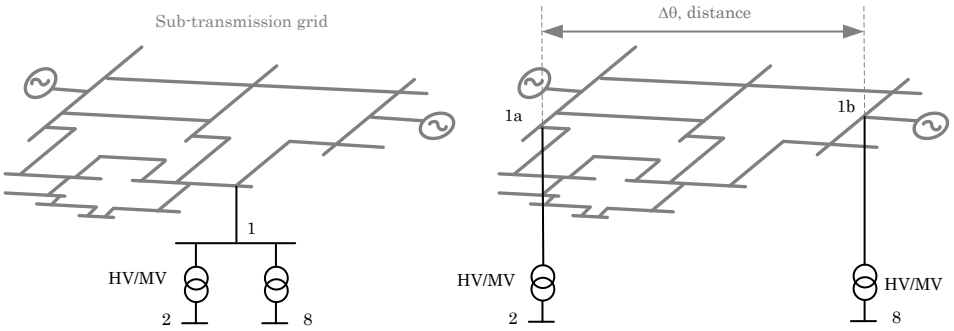


Figure II.3.22: Benchmark example: case 0 (the red-filled squares denote *closed* circuit-breakers while green-empty squares denote *opened* circuit-breakers)

In these cases it has been assumed that both grids are arborescent and connected to the same subtransmission point. Other results may be found if distribution grids are connected to different points of the subtransmission grid because there would already be a phase shift in the input of the feeding transformers (Fig.II.3.23).



(a) Connection at the same point

(b) Connection at different points

Figure II.3.23: Different connection points of distribution grids

This discussion can be concluded stating that, when deciding between UPLC or MVDC for distribution-grid interconnection, a comprehensive phase-angle difference must be done for each specific case. In the preceding examples the influence of the interconnection in the phase difference has not been taken into account considering that the interconnection itself has not an impact on the phase-angle difference. In reality, the fact of interconnecting the grids will generally lower this phase difference and, in a real design case, all the possible scenarios (with variable loads/DG and with/without interconnection) must be evaluated.

The schematic diagram of Fig.II.3.24 represents two interconnected grids. Without interconnection ($\mathbf{i_k} = \mathbf{0}$), an increment of $\mathbf{i_2}$ will provoque the angle of $\mathbf{v_2}$ (θ_2) to lagg further, increasing the phase-difference between the two grids. However, with an interconnection, grid 1 can provide as much $\mathbf{i_k}$ current as to compensate for the increase of $\mathbf{i_2}$, reequilibrating the phase-difference between the connection points.

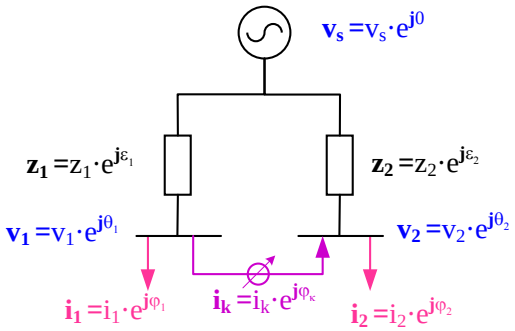


Figure II.3.24: Schematic interconnection of two distribution grids

4. x/r ratios and impedances of distribution lines and cables

Impedances and x/r ratios in distribution grids can take a wide range of values depending on their nature (line or cable), the material used as a conductor (copper or aluminium), the isolating

materials and the construction type, conductor surface ....

As a rule of thumb, values of $x/r = 10$ are generally used for transmission applications, and values of $x/r = 1$ are often assigned in distribution studies. Table II.3.25 provides some characteristic values of distribution lines and cables, where it is observed that the x/r ratio can go from 0.25, for very resistive cables with small conductor areas, to 1.5, for less resistive conductors.

	Overhead lines (1-50 kV)				Cables (1-50 kV)			
	r ' (Ω/km)	x ' (Ω/km)	c ' (nF/km)	x/r (pu)	r ' (Ω/km)	x ' (Ω/km)	c ' (nF/km)	x/r (pu)
z_1=z_2	0.3-0.9	0.35	5	0.39-1.17	0.1-0.4	0.1-0.15	170-250	0.25-1.5
z_0	0.3-0.5	1.5		3-5	0.9-1.2	1.5-1.7		1.25-1.89

Figure II.3.25: Orientative impedance values in the 1-50 kV range

5. Conclusions: Comparison between UPLC and MVDC

UPLC and MVDC are candidate devices for interconnection of MV distribution grids because they can independently control the active and reactive power flows that flow across a line. Additionally, their structures make it possible to control other power quality objectives, even if this option may not be always interesting.

Regarding the structure of the apparatus, the MVDC presents two great advantages in comparison to UPLC. The first one is that it can be splitted apart and thus, it may be a more cost-effective option for long distance interconnection. However, since the objective is not bulk-power transmission, it is assumed that distribution grids are not located very far one to the other. The second advantage lies in its symmetry, which allows it to work in the four PQ quadrants and reverse the power flow independently of the angle-difference between the interconnection points. The UPLC, on its part, presents other two notable advantages: (1) the possibility of short-circuiting the series-side compensator without loosing the interconnection, and (2) a smaller size for certain transmission-angle and x/r ratio conditions.

As far as interconnection characteristics concern, MVDC presents better properties when interconnection distance is long because it is not limited to work in back-to-back mode, as is the case of UPLC. On the other hand, MVDC is the only feasible alternative if the interconnection is asynchronous. MVDC is also the only alternative when the phase difference between the interconnection points exceeds a threshold value. However, if the interconnection distance is short, the transmission angle is small, and the interconnected grids are synchronous, UPLC may be a less bulky and cheaper option than the MVDC.

With respect to the attainable objectives and functions, the need of gathering power-flow and power-quality functions is questioned. In fact, the sizing, design and operation complexity of the apparatus are significantly increased when performing power quality enhancement.

Anyhow, if power-quality compensation functions are considered, both apparatus can attain the same objectives but in slightly different ways due to the lack of symmetry of the UPLC. In this case, the symmetry and splitting capability of MVDC constitutes an interesting feature because it provides the opportunity of directly connecting each of the shunt-branches to the sending and receiving ends. Provided that the interconnection distance is very short, the series VSC of the UPLC can work in association with the line impedance to operate as an equivalent current source. But, due to the control control challenges, this option is regarded more as a concept than as a real solution.

In regards of size, the results obtained from a particular case study have shown that:

- It is preferable to install the UPLC close to one of the interconnection points in order to avoid the such called *undefined areas*. This will be usually the case.
- For each particular x/r ratio, a threshold phase-difference value exists below which, the UPLC is smaller than the MVDC (or, at least, the active power flowing through the DC link of the UPLC is smaller than that flowing through the DC link of the MVDC). For an indicative x/r value of 1, which is quite common in distribution grids, the threshold angle is set around 90 degrees.

After a qualitative and quantitative analysis on the phase-angle difference between two distribution grids, the following conclusions are obtained:

- Considering that both grids are connected to the same point of the sub-transmission grid, the phase-angle difference depends on the loading difference between the grids and the impedances between the sub-transmission grid to the interconnection point. So, if both grids are very similar (almost symmetrical), and the loadings are balanced, the phase difference will not be very big.
- If each of the grids is connected to a different point of the sub-transmission grid, then the phase-angle difference may be higher.
- An example case obtained from a CIGRE benchmark has shown that, even in adverse conditions, the phase angle difference does not even reach 10 degrees.

To conclude, it is possible to say that, in spite the remarkable flexibility offered by MVDC, in some particular conditions the UPLC may be a more cost effective solution than the MVDC. These conditions can be summarized as:

i) The interconnected grids are synchronous.

ii) The phase-angle difference between the interconnection points is kept small (<90 degrees) in all operating conditions.

Part III

UPLC for distribution network interconnection

OUTLINE OF PART III

The aim of Part III is to analyze and understand the implications of integrating a UPLC in MV distribution grids. Until now, the few UPFC installed around the world (only three) [58, 59, 60, 61, 62, 63, 64], and the study-cases proposed in the literature, are all UPFC devices connected at the transmission level. However, when the UPLC is connected to the distribution level additional aspects must be accounted for. For example,

- in distribution grids there is **a higher amount of cables** than in transmission grids (e.g. close to densely populated urban areas),
- in distribution grids **the power quality level is lower** [19] (voltage sags occur more often and the unbalance and THD levels are generally higher), and
- **the structure, topology, and operation of distribution grids is different** (e.g. distances are shorter, they are radially operated, different neutral-regimes can exists, in general they are less monitored and automatized).

In Part III the above mentioned aspects are evaluated and discussed for the case of a UPLC used for the interconnection MV distribution grids.

- **Chapter III.1** evaluates sizing and design aspects of a UPLC, proposing a design procedure for calculating the magnitudes of each of the components of the UPLC. This design procedure, which is mainly oriented to power-flow control in steady-state conditions, provides the base-size of the apparatus. Additionally, as a complement to the fundamental size calculation, Chapter III.1 provides guidelines to readjust the design of the UPLC such that different types of power quality phenomena are compensated.
- **Chapter III.2** presents the models of the different parts of a UPLC (series-side subsystem, shunt-side subsystem, and DC-link) and of the cable that links the UPLC with a MV distribution grid.
- **Chapter III.3** proposes a control approach for a UPLC connected to a RL line. The proposed control approach is a vector oriented control but, in this case, instead of using typical PI controllers, an alternative control structure is presented. The suggested control is an inbricated control structure that is based on a higher level trajectory generation strategy that establishes virtual tracking references to lower order controllers. This control structure has been designed according to Lyapunov stability theorems.
- **Chapter III.4** deals with two issues:

  1.- It proposes a control structure for a UPLC connected to a cable. This control structure is based on the same control philosophy that is introduced in Chapter III.3.

2.- Due to the difficulty of measuring the voltage and current values at the receiving-end, and of obtaining the intermediate states of the cable, a Kalman-type observer is proposed in order to overcome these barriers.

The valididy of the proposed approaches has been verified by simulations in Matlab/Simulink under parametrical uncertainties and balanced voltage sags.

- **Chapter III.5** discusses the problem of working under an unbalanced environment. Indeed, up to present, this problem has just been addressed in shunt- or series-connected devices, but not in UPLC. In this chapter, two different types of vector-oriented techniques have been analysed: (a) SRF-oriented techniques, and (b) sequence-based techniques. The advantages and disadvantages of these techniques are discussed through simulation examples.

- **Chapter III.6** provides a consequential work on synchronization and sequence extracting techniques. The chapter starts by presenting a comprehensive overview on synchronization and sequence extraction techniques. Then, four different methods are selected and compared in simulation. Chapter III.6 constitutes a solid analysis that will help to evaluate the suitability of sequence-based and vector-oriented techniques in real applications.

- Finally, **Chapter III.7** explains some practical implementation issues that have been encountered during the preceding chapters.

Chapter III.1

UPFC sizing and design

Conceptually, UPLC is a remarkable apparatus because it can gather power-flow and power-quality functionalities in the same device. However, this sublime feature presents substantial challenges when designing and sizing the components of the apparatus, as it is discussed at the end of the chapter.

The main objective of Chapter III.1 is to explain the procedure that has been followed, and the assumptions that have been established, to define a case study and select the values of the components of the UPLC and of the surrounding system. For this design, a steady-state operation, where only power flow is controlled, has been considered.

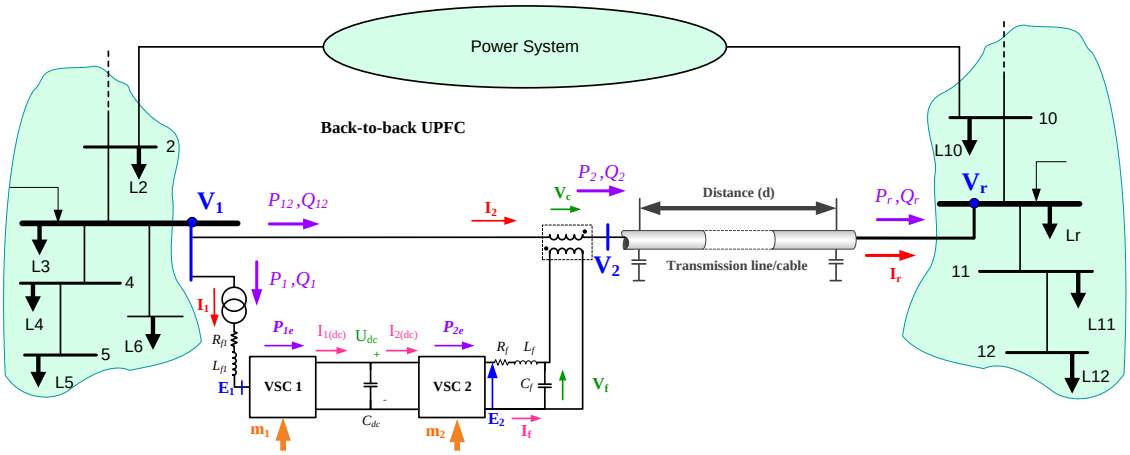


Figure III.1.1: UPLC interconnecting two MV distribution grids

The design procedure is divided in two parts: (a) the definition of the case-study (specifying the need), and (b) the evaluation of the apparatus characteristics and the design of its components:

- First, the case-study is defined. In this stage, parameters such as the type of interconnection line and its electrical properties, the interconnection distance, the phase-angle difference (transmission angle) between interconnection points, the maximum value of the nominal series injected voltage, and the grounding type of the grid, are set up.
- In the apparatus design stage, the properties of UPLC components are evaluated and adequate ratings are calculated based on the previously defined specifications. Observe that the purpose of this sizing exercise is not to design components for a constructive use but for software simulations.

1. Case-study definition. System description and considered assumptions.

The UPLC that is to be dimensioned interconnects two MV distribution grids as shown in Fig.III.1.1, and it is located at the 20 kV voltage level, which is the most extended distribution voltage level in France [6]. The UPLC is dimensioned to work in steady-state (i.e. if voltage sags occur or if the line-current ratings are exceeded the series-side compensator is bypassed), and it is principally dedicated to power-flow control.

Before defining the characteristics and values of UPLC components, it is necessary to define a working case (Fig.III.1.2). In this working case, nominal values and conditions of the surrounding power system are defined. Notably, the characteristics and distance of the interconnection line, the nominal transmission angle, the maximum series injected voltage under nominal conditions, and the grounding type of the MV distribution system.

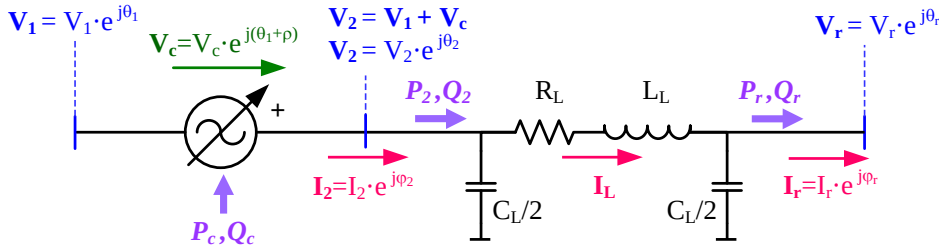


Figure III.1.2: System description for UPLC dimensioning issues.

1.1. The characteristics of the line that interconnects the grids.

One of the first steps before starting the sizing example is to define the type of line (or cable), and the distance of the interconnection.

1.1.1. Type of line/cable.

Approximative impedance ranges of MV lines and cables are gathered in Fig.II.3.25. However, the characteristics of lines and cables vary substantially from one case to the other depending on their nature (line or cable), voltage level, conductor material (copper or aluminium), conductor section and constructive characteristics (solid conductor or stranded conductor), isolation material, and layout (shielded or not), among others.

Several cable constructors such as, General Cable [90], Nexans [91], NKT Cables [92], and ABB [93], offer a wide range of MV lines and cables and their catalogues are available online. In this exercise, a particular cable from Nexans (**IEC 60502-2 / NF C 33-220 12/20 kV Al 3x185**) has been chosen. This cable is designed to operate at 20 kV, and it has an aluminium conductor of 185 mm^2. The main electrical properties of this cable are reproduced in Table III.1.1.

Table III.1.1: Electrical characteristics of the chosen cable

Electrical characteristics	Values
Nominal operation voltage U_0/U	12/20 kV
AC resistance @ 90 $°C$ (trefoil formation)	0.211 Ω/km
Nominal inductance	0.4 mH/km
Maximal admissible current (open-air) @ 30 $°C$ (trefoil formation)	353 A
Maximal admissible current (grounded) @ 30 $°C$ (trefoil formation)	356 A

1.1.2. Interconnection distance.

Assuming that both grids are connected to the same point of the subtransmission grid (Fig.II.3.24(a)), the distance between the interconnection points is expected to be relatively short. In this case, a distance of 15 km is selected. Observe that, in the MV distribution grid benchmark example of [88, 89] the total length of the lines and cables of sub-network 1 is 15 km. Also, in the french MV distribution grid the average distance of main distribution feeders is around 10-30 km [6].

1.2. Phase-angle difference between interconnection points $\Delta\theta$=θ_1-θ_r and maximum injected series voltage in nominal conditions.

The nominal phase-angle difference between the interconnection points constitues a very important factor to account for in the design stage of the UPLC because it has an influence on the magnitude of the current that flows through the cable. Lines and cables have a maximum current rating, which is given by their thermal capacity, that must not be exceeded. In the case of the selected cable the maximum allowed current is around 350 A, as shown in Table III.1.1.

In Fig.III.1.3(a), the current magnitude of the cable (modelled as a single π-section) is monitored without considering any series voltage injection for phase differences from 0 to 180 degrees. As it can be observed, the current magnitude reaches the 350 A limit at around 4.6 degrees. This means that the transmission angle between both grids cannot go beyond 4.6 degrees when the series-connected apparatus is bypassed or, in other words, it is not possible to join these two points with the chosen cable if the phase-angle difference is higher than 4.6 degrees.

When a series voltage is injected, the current increases for certain ρ angles, which means that the nominal phase-angle difference must be far below 4.6 degrees if the current limits are to be satisfied. So, the second step of the study-case definition is to set the nominal phase-difference between interconnection points and the maximum series injected voltage.

In order to establish an adequate pair of values for $\Delta\theta_{\text{nom}}$ and $V_{\text{c-max}}$ that certifies that the cable current is always below the maximal current rating, several simulations have been performed. Finally, after some iterations, the current values of Fig.III.1.4 are obtained for $V_c = 1000\ V$ and

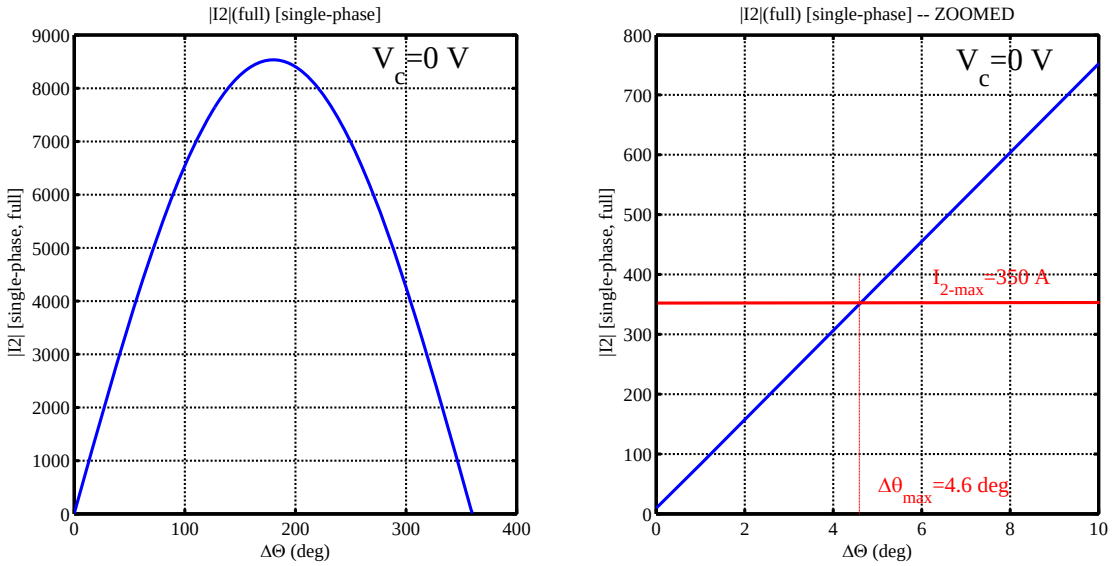


Figure III.1.3: Current magnitude through the cable in terms of transmission angle when $V_c = 0$.

$\Delta\theta = 1°$. The current circle depicted in Fig.III.1.4 represents the locus of the current values that can be obtained when $V_c \leq 1000\ V$ for any ρ values (d-axis is inlined with the V_1 vector).

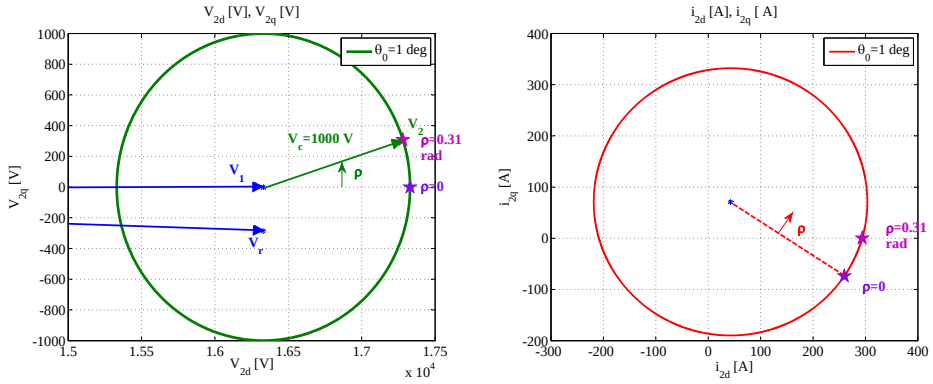


Figure III.1.4: (a) V_2 when $V_c = 1000\ V$ and $0 \leq \rho < 2\pi$, and (b) Current resulting from V_c injection.

A maximal V_c value of 1000 V is considered to be a reasonable value because it is not too small nor too big in relation with the phase voltage (around 1/16-th of the phase voltage) and does not imply a huge rating of the series compensator. A transmission angle $\Delta\theta$ (θ_0) of 1° is rather low but, considering the characteristics of the interconnection, it is not possible to increase it further. The only way to increase the nominal $\Delta\theta$ is to assume a longer interconnection distance or another type of cable (even more resistive).

Additionally, Fig.III.1.5 shows the magnitudes of the currents for $0 \leq \rho < 2\pi$ when $V_c = 1000\ V$ and for different transmission angles. As it is observed, when $\Delta\theta = \theta° = 1°$, the current magnitude reaches a maximum value of 344 A (continuous black curve).

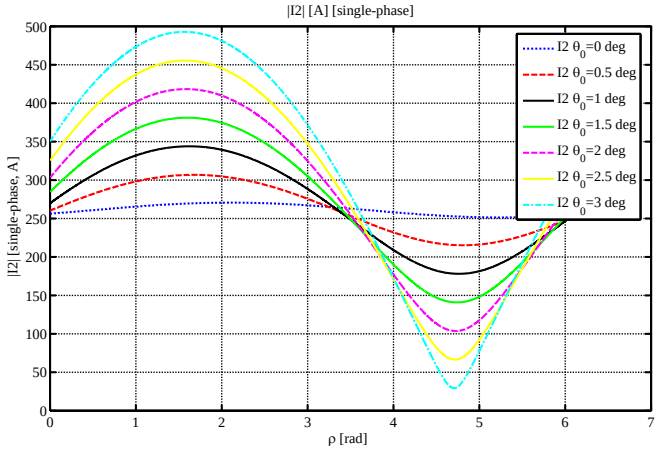


Figure III.1.5: Current magnitudes resulting from $V_c = 1000V$ injection for different values of transmission angles (θ_0).

1.3. Grounding type of the MV distribution network.

Nowadays, different types of grounding methods exist. The grounding type of a distribution grid is often a national decision, since it conditions many aspects of the whole system. The chosen grounding method has an influence on the ratings of materials and components, on insulation and protection coordination, on power quality, and on human safety, for example.

Four main grounding systems are used worlwide [6, 94]: (1) the ungrounded or isolated grounding, (2) the impedance grounding, (3) the resonant grounding, and (4) the effective or solid grounding. These grounding techniques are graphically represented in Fig.III.1.6.

Ungrounded or isolated neutral	**Impedance grounding**	**Resonant grounding**	**Effective or solid grounding**
Not grounded (Transformer secondary in Δ or Y)	Grounded (Transformer secondary in Y)		
Three-wires			Four-wires
HT/MT	HT/MT, Z_n	HT/MT, Petersen Coil (L_p)	HT/MT
• Germany • Belgium • Italy • Japan • Norway	• Belgium • France • UK • Irland • Japan • Sweden	• Germany • Finland • Norway	• USA • Canada

Figure III.1.6: Grounding types and countries where they are used.

Each of the presented grounding types has advantages and disadvantages. The **ungrounded case**, for example, presents very low fault currents in single-line to ground (SLG) faults (unless

long distance cables are used). However, these topology presents two shortcomings: (a) low fault currents are difficult to detect, and (b) overvoltages on the unfaulted phases may require enhanced insulation requirements. The **solidly grounded case** is the opposite to the ungrounded case. In the solidly grounded case fault-currents are very large, but overvoltages are minimized. The **impedance grounding** and the **resonant grounding** are compromise solutions in between the ungrounded case and the solidly grounded case. The objective of the impedance grounding is to limit fault currents and overvoltages to an acceptable limit by means of an impedance located between the neutral connection and the ground. Similarly, the resonance grounding uses an inductance (known as Petersen Coil) that is tuned with the homopolar capacitance of the system to offer an impedant resonance peak when faults occur. In this way, if a SLG fault occurs, the fault current is null.

The grounding type of the MV distribution grid is a very important fact to consider during the design stage of the UPLC. Indeed, the grounding type influences the way in which the apparatus is internally wired and externally connected to the grid. For example, if the UPLC is connected to a three-phase four-wire system, homopolar voltages and currents need to be controlled.

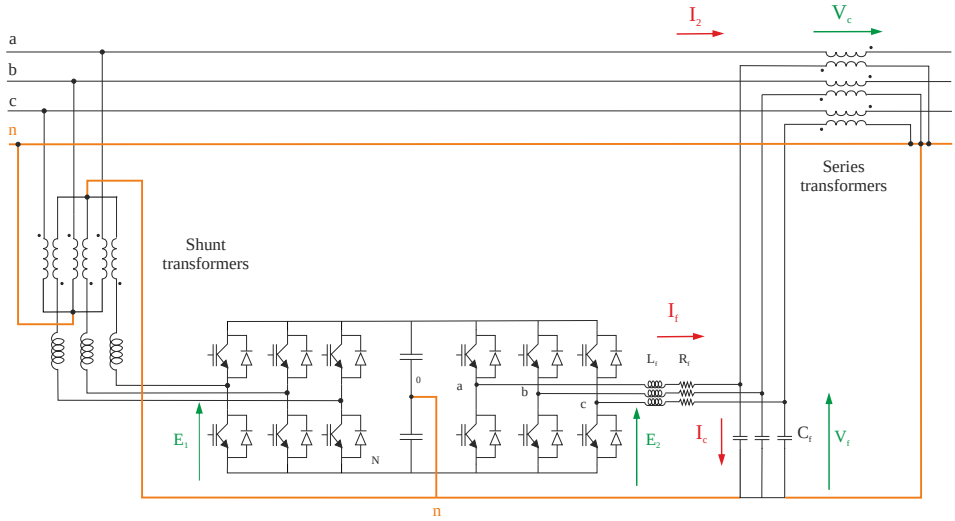


Figure III.1.7: UPLC connected to a 3-phase 4-wire system (solidly grounded)

In Fig.III.1.7, the three-phase diagram of an UPLC connected to a three-phase four-wire system is presented, where the following points can be observed:

- The neutral points of transformers and filters are connected to the neutral conductor. This is only possible when Y-type connections are used (and a neutral conductor exists).
- The neutral point needs to be connected either to: (i) the electrical middpoint of the DC-link (using splitted capacitors as shown in Fig.III.1.7), or (ii) to a fourth branch of the converter (Fig.III.1.8). The four-legged converter topology has a better controllability than the split-capacitor topology. However, the conventional three-legged topology is usually prefered because of its lower number of semiconductor devices [16].

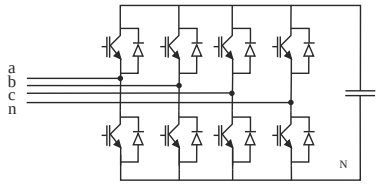


Figure III.1.8: Four-legged VSC.

In three-phase three-wire systems the control of zero sequence components is not necessary (at least during normal conditions) and thus, the wiring of Fig.III.1.7 can be simplified by eliminating the neutral wires from the power circuit. This action includes the elimination of the electrical midpoint of the DC bus, and the ungrounding of the Y-connected LC filters and transformers. Otherwise, a low-impedance path for zero sequence components would be formed through the ground, close to the outputs of the VSC [16]. Additionally, since the neutral points of the transformers must not be grounded, it is possible to use delta transformer connections.

In this work, a three-phase three-wire connection has been assumed and thus, the power circuit of Fig.III.1.9 has been used. This means that the used wiring system does not allow for zero-sequence component compensation.

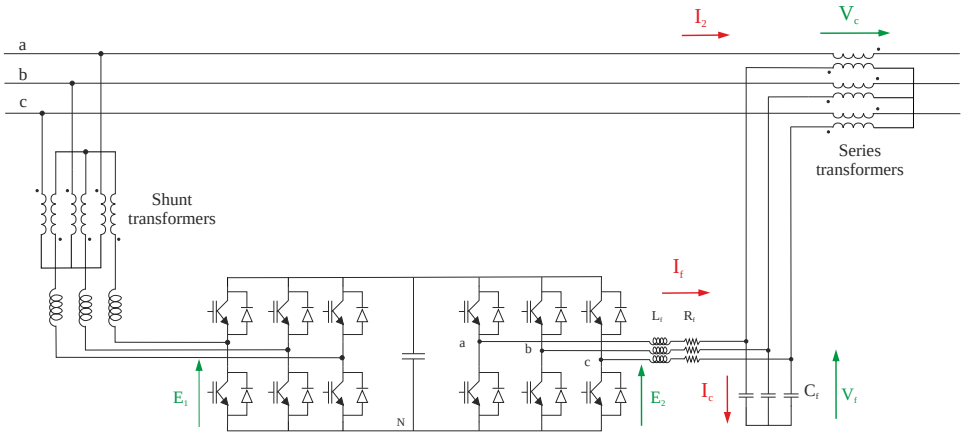


Figure III.1.9: UPLC connected to a 3-phase 3-wire system

1.4. Case-study

After the abomentioned evaluations and calculations, the case study is defined:

- The UPLC interconnectes two MV (20 kV) distribution grids that have a nominal phase-angle difference of $\Delta\theta = 1°$.
- The interconnection line is a $d = 15\ km$ cable with the electrical characteristics of Table III.1.1.

- The maximal voltage that can injected by the series device under nominal conditions is $V_c = 1000\ V$. This voltage can be injected with any angles ($0 \leq \rho < 2\pi$).
- The UPLC is connected to a three-phase three-wire system and thus, it does not have zero-sequence component compensation capacity.

2. Design and characteristics of series-side elements

The series-side of the UPLC is composed by a series-transformer, a series-filter and a VSC, as shown in Fig.III.1.10. In this section the main characteristics and ratings of these elements is defined.

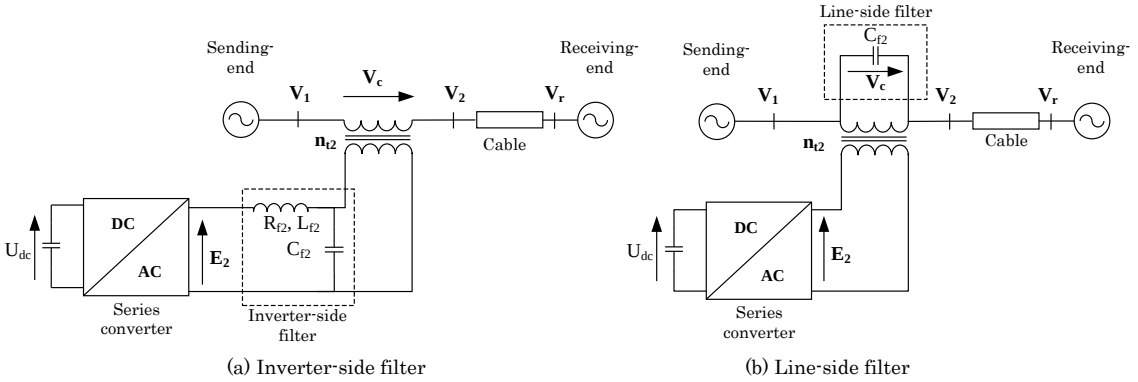


Figure III.1.10: Single-line representation of (a) Inverter-side filter, and (b) Line-side filter.

2.1. Series transformer

The voltage generated by the series VSC is usually connected to the line by means of a filter and of a series transformer. Some publications that use a multilevel converter topology [95, 96] have proposed the elimination of the series transformer, but this may be a risky alternative since the transformer provides galvanic isolation.

The series transformer does not behave as a regular power transformer, but rather as a current transformer. For this reason, some considerations must be taken into account in the design stage:

2.1.1. Magneto-motive-force balance.

The secondary circuit of a current transformer must never be open-circuited because high overvoltages, that can lead to serious transformer damage, can be induced in the secondary winding. These overvoltages are generated because, when an unbalance of the magneto-motive force occurs (observe that $\mathbf{I_2} = \mathbf{0}$), the core flux increases up to saturation level:

$$N_1\mathbf{I_1} - N_2\mathbf{I_2} = \Re_c\mathbf{\Phi_c} \tag{III.1.1}$$

where $\mathbf{\Phi_c} = \hat{\Phi} e^{j\omega t}$, is the core flux.

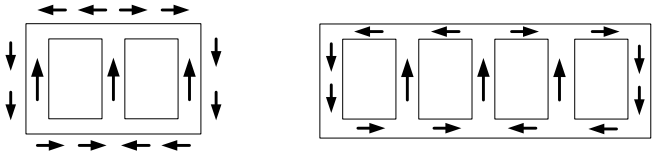
The elevated rate of the flux derivative induces, in turn, a strong voltage at the secondary winding.

$$\mathbf{E_2} = N_2 \frac{d\mathbf{\Phi_c}}{dt} = j\omega N_2 \mathbf{\Phi_c} \tag{III.1.2}$$

For this reason, if any faults occur, it is necessary to short-circuit the secondary winding instead of opening it. An example of a short-circuiting system for the secondary is illustrated in Fig.II.3.2. The protective device is composed of a set of anti-parallel thyristors that short-circuit the secondary winding according to the command signals of a thyristor control block. The control block is often driven by a varistor.

2.1.2. Magnetic circuit type.

The alternating current flowing through each phase-winding of the transformer induces an alternating flux that flows throughout the transformer core. If the transformer is fed with a balanced three-phase voltage set, the sum of the three-phase voltages and fluxes is zero. On the contrary, if the input voltages are not balanced, the sum of the induced fluxes may not cancel and an homopolar flux may flow through the core. If a three-limbed transformer is used, the homopolar flux finds a closed-loop path through the air resulting in a much smaller magnetizing reactance and provoking a large voltage drop at the transformer terminals. For this reason, three-limbed three-phase transformers are not adequate for dealing with unbalanced voltages. If unbalanced voltages are to be addressed, two solutions can be evaluated: (i) to use a five-limbed transformer as in Fig.III.1.11(b), or (ii) to use three separated single-phase transformers. In general, three separate single-phase transformers are used.



(a) 3-limbed 3-phase transformer (b) 5-limbed 3-phase transformer

Figure III.1.11: Homopolar flux in three-phase transformers (a) Three-limbed, and (b) Five-limbed

2.1.3. Transformer coupling type.

Series transformers can be connected to the line in **star/open** or **delta/open** winding configuration (converter side/line side) [97]. When the neutral point of the star/open configuration is grounded, it allows the injection of positive-, negative-, and zero-sequence voltages, whereas the delta/open configuration and the star/open configuration without grounding does not allow for zero-sequence

voltage injection. Although the star/open configuration is usually prefered, the delta/open configuration makes a better use of the DC-link voltage [98].

2.1.4. Flux-linkage at switch-on instants.

If the series device is suddenly activated, which is the case of dynamic voltage restorers (DVRs), there is a chance that the flux-linkage ($\psi = N\phi$) reaches a very high value (as high as double the nominal flux-linkage value). This effect is produced because the value of the initial flux-linkage depends on the value of the initial injected voltage. If the switch-on takes place near a zero-crossing of the series voltage, the flux-linkage will reach twice the steady-state value [99, 100].

The most straightforward and extended solution is to rate the series injection transformer to be able to handle twice the steady-state flux-linkage rating [97]. However, other solutions, such as appling form-factors to the injected voltage in order to minimize the flux offset, have also been proposed [99].

In the case of a UPFC this effect is not as pronounced as in DVRs because the series voltage can be injected smoothly and the device is operated continuously.

2.1.5. Voltage drop across the transformer.

The series transformer is connected in series with the line and, as sketched in Fig.III.1.12, the line current flows through the transformer windings inducing a voltage drop. This voltage drop exists even if the output of the converter is null.

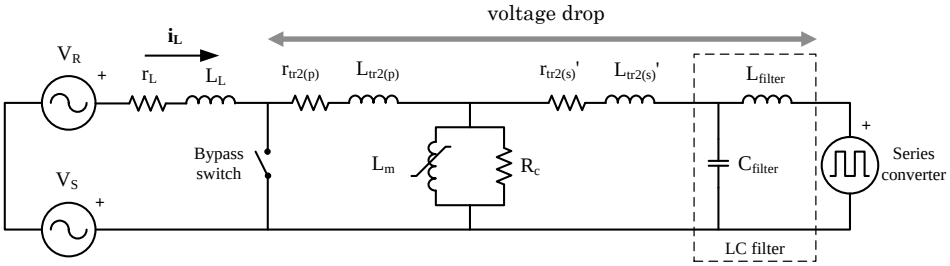


Figure III.1.12: Single-phase representation of the series-side compensator in series with the line

When the UPLC is not in operation, it is possible to use a bypass-switch that short-circuits the whole series device. Additionally, in the case of DVRs, this bypass switch must be able to open fast enough in order to compensate correctly for voltage sags.

In any case, it is advisable to minimize the transformer leakage impedance and the filter inductance in order to avoid large voltage drops and to make a better use of the converter capacity. Series injection transformers must be specially designed to avoid voltage drops. In [97], for instance, a leakage impedance value of 0.01 *pu* is proposed. This value is an extremely low value comparing to a regular power transformer (≈ 0.15 *pu*).

2.1.6. Series transformer design

Considering the abovementioned aspects, in this work, **three single-phase series transformers**, connected in **Y/open configuration** have been selected. The primary voltage of the transformer (line side) has already been established to 1000 V, and the leakage impedance of the transformers is assumed to be $z_k = 10\%$. The missing steps in order to define the characteristics of the transformer are:

- **To define a turns-ratio for the series transformers.**

  If $n_t < 1$ then, according to

  $$n_t = \frac{N_{prim}}{N_{sec}} = \frac{V_{prim}}{V_{sec}} = \frac{I_{sec}}{I_{prim}} \tag{III.1.3}$$

  the current at the secondary is lower than the current at the primary, and the voltage at the secondary is higher than the voltage at the primary. If $n_t > 1$, the opposite occurs. On the one hand, a $n_t < 1$ turns-ratio requires a converter topology that is able to produce higher voltages at the secondary, probably a multilevel topology or a topology with semiconductor switches connected in series. On the other hand, a $n_t > 1$ turns-ratio needs a converter topology that is able to handle higher current values (with switches in parallel, for instance).

  Finally, The turns ratio, $n_{t2} = N_{prim}/N_{sec}$, of the series transformer (T_2) is chosen to be the unity ($n_{t2} = 1/1 = 1$). In this manner, the primary voltage is the same as the secondary voltage, and the line current is the same as the secondary current. The secondary will have a maximum voltage level of 1000 V and a maximum current level of 350 A. At the same time, the DC-link voltage would be charged slightly higher than 2000 V ($U_{dc} \approx 2000$ V). These values are reasonable for a typical two level converter with single IGBT switches. This decision is regarded as a good trade-off for voltage and current levels at the secondary.

- **To define the nominal power of the series transformer.**

  The nominal power of the transformer is obtained by calculating all the possible operation points of the UPLC and obtaining the required apparent power of the series device. This is, the maximum series voltage ($V_c = 1000$ V) is injected with ρ values within 0-2π and the maximum apparent power is obtained using equation

  $$S_c = |\mathbf{S_c}| = \frac{|\mathbf{V_c} \cdot \mathbf{I_2}^*|}{2} \tag{III.1.4}$$

  where $\mathbf{V_c}$ and $\mathbf{I_2}$ are peak-valued phasors corresponding to the injected series voltage and line current, respectively, and S_c is the apparent-power per-phase.

  Fig.III.1.13 shows the apparent powers that need to be provided by the series compensator in order to be able to inject a series voltage of $V_c = 1000$ V with any ρ angles. The figure shows the values for different transmission angles. For $\Delta\theta = 1°$, the maximum apparent power needed is 171.6 kVA (per phase). Accordingly, the nominal apparent power of the

series transformer is chosen to be $S_{tr2} = 171.6\ kVA$ (per phase).

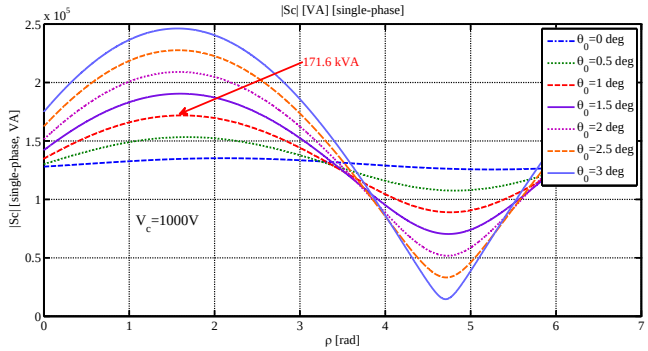


Figure III.1.13: Magnitudes of the apparent power needed by the series compensator to inject $V_c = 1000\ V$ at any ρ angles.

■ **To define the impedances of the series transformer.**

The impedances of the series transformer are calculated assuming that the leakage impedance of the transformer is 0.1 pu of the transformer base impedance and that $x/r = 20$. The calculation procedure is described in Appendix E and the values are presented in Table III.1.2.

Table III.1.2: Main characteristics of series transformers

Features	Values
Transformer coupling	3× 1ph transformers in Y/open
Turns ratio, $N_t = N_{(prim)}/N_{(sec)}$	$n_{t2} = 1$
Nominal power (per phase)	$S_{c-tr2} = 171.6\ kVA$
Voltages ($\hat{V}_{prim}/\hat{V}_{sec}$)	$1000\ V/1000\ V$
Total leakage impedance	$Z_{tr2} = 10\%$
Magnetizing reactance and core losses	$X_m = R_c = 1000 \cdot X_{tr2}$

2.2. Series VSC

Until now, the use of a three-phase VSC has been assumed, which is, indeed, the type of VSC used in this work. With a three-phase VSC it is necessary to define the connection type of transformer secondary windings and to decide the existance of a neutral-point wire. Before continuing with the design aspects of the three-phase VSC, it is worth mentioning the possibility of using a different converter configuration as such of Fig.III.1.14. This configuration uses as separate single-phase UPLC for each of the *abc* phases, providing a high control flexibility that includes zero-sequence component compensation. The main drawback of this configuration is the higher number of components used. On the ongoing paragraphs, some aspects of the chosen three-phase VSC for the series-side are developped.

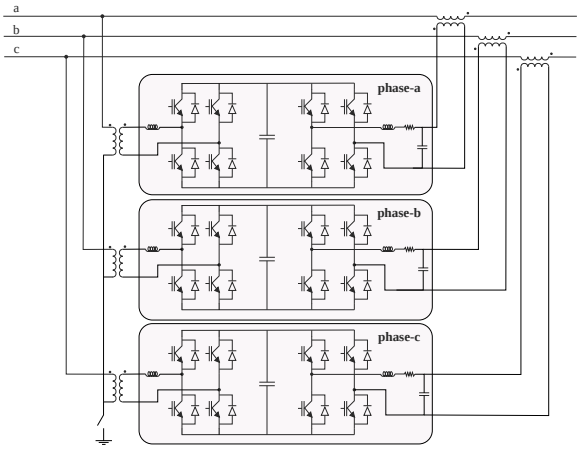


Figure III.1.14: UPLC composed of three separate single-phase units

2.3. Series VSC design

Since the maximum series injected voltage is $\hat{V}_{c(prim)} = 1000\ V$ and the turns-ratio of the transformer is chosen to be the unity, $n_{t2} = 1$, the maximum voltage at the secondary of the series transformer is also $\hat{V}_{c(sec)} = 1000\ V$. Following a similar reasoning, if the maximum current at the primary (given by cable specifications) is $I_{2(max)} = 350\ A$, the current at the secondary of the transformer is also around 350 A.

This means that, the series VSC must be able to generate a phase voltage slightly higher than 1000 V (on account of losses) and must withstand a nominal current slightly higher than 350 A. These values are considered to be low enough to use a typical two-level three-phase converter structure like the one depicted in Fig.III.1.15. Then, if a PWM-type modulation is used, the voltage at the DC side must be slightly higher than $U_{dc} \geq 2000\ V$ as it is deduced from the plots of Fig.III.2.20(b).

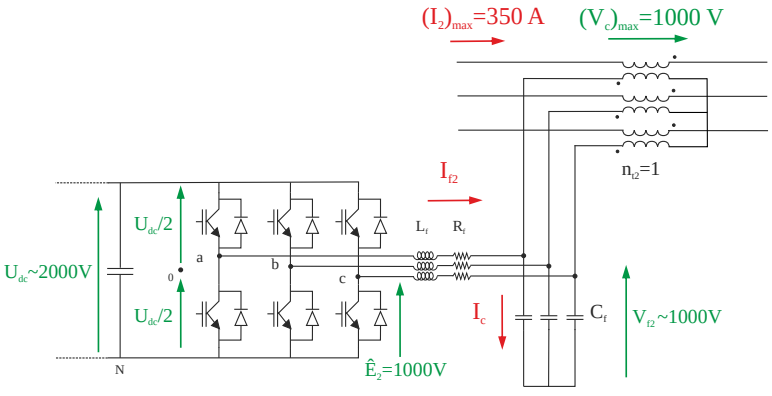


Figure III.1.15: Two-level VSC with IGBTs connected in series with the line

The analytic expression of the fundamental phase voltage at the output of the converter

(assuming scalar PWM modulation) is given by expression

$$\hat{e}_2 = \frac{1}{2} \cdot m \cdot U_{dc} \text{ ,when} \qquad m \leq 1 \tag{III.1.5}$$

where m stands for the amplitude modulation index, $m = \hat{v}_{ref}/\hat{v}_{tri}$, that is in the $0 \leq m \leq 1$ range when operating in the linear region. Further information on PWM modulation can be found in Appendix E.

The existing IGBT families (600 V, 1200 V, 1700 V, 3300 V, 4500 V, and 6500 V) also corroborate the feasibility of the selected values. Usually, the U_{dc} value must not be higher than half the nominal V_{ce} voltage of the IGBT. Hence, IGBTs from the 4500 V family can be selected. For example, the brand Hitachi commercializes 4500 V IGBTs with a collector current capacity of 800 A and 1200 A.

Regarding the switching frequency of the converter, a compromise value of $f_{sw} = 99 \cdot 50 = 4950\ Hz$ ($m_f = 99$) has been chosen for the study case, not too high (to avoid switching losses) and not too low (not to loose accuracy). In any way, a comprehensive switching-loss analysis should be done in order to establish an optimal switching frequency value.

2.4. Series filter

The goal of the series filter is to attenuate the switching harmonics generated by the series VSC. The series filter can be located either on the line-side or in the inverter side, as shown in Fig.III.1.10. A comprehensive comparative study can be found in [101]:

- The major **advantages of the inverter-side filter** are that it is located at the low-voltage side of the series transformer and that it is closer to the harmonic source. Since the filter is placed between the harmonic source and the transformer, it serves as a low-impedance path for undesired harmonics, preventing them from entering the transformer. The **drawbacks of the inverter-side filter** are the induced voltage drop and phase-shift that modifies the output voltage of the VSC. This fact complicates the control of the series VSC because it is necessary to compensate for this voltage drop and phase-shift.
- From a control point of view the line-side filtering scheme is not as troublesome as the inverter-side scheme, and it does not provoke a voltage-drop in the line. The main **disadvantages of the line-side filtering scheme** are that the filter is located at the high voltage side of the system, that the filter capacitor may create resonances in the line, and that the harmonics penetrate the transformer. As a result, the transformer must be rated to withstand harmonic voltages and currents and therefore, its rating is higher. A design procedure for the line-side filter is presented in [101].

It must be noted that, the higher or lower voltage sides depend on the chosen transformer turns ratio. Accordingly, some of the abovementioned points are only true when $n_t > 1$.

Despite a higher design difficulty (two variables instead of one), the inverter-side filter is probably the most commonly used filtering scheme. For this reason, in this work a LC-type inverter-side filtering scheme has been selected. Regarding inverter-side filter design methods, two interesting methods have been identified [102, 98]. The method of [102] is a very complete and exhaustive method but, since it requires a laborious procedure, in this work, the design method of [98] has been prefered due to its simplicity and good results.

2.4.1. Design of an inverter-side filter according to [98]

The design proposed in [98] is based on two points: (i) the fact that the reactive power generated by the filter capacitor must be absorbed by the inverter and thus, by limiting the value of the filter capacitor, the inverter rating is limited, and (ii) the cutting frequency of the filter.

- **The first step of this procedure** is to choose the cutting frequency of the filter. The relation between the cutting frequency of the filter, L, and C is given by

$$LC = \frac{1}{{\omega_c}^2} \tag{III.1.6}$$

  A rule of thumb is to choose the cutting frequency of the LC filter 10 times lower than the inverter switching frequency. The reason is that, as previously mentioned, the first switching harmonics appear at the switching frequency. The values of L and C must satisfy equation (III.1.6), and they can take any pair of values as long as they fulfill equation (III.1.6). However, there are some design constraints that must be taken into account. The value of L, for example, must be the lowest as possible to limit the voltage-drop at the converter output. Consequently, if the value of L is low, the value of C will be high and, a large capacitor creates a large amount of reactive power that must be absorbed by the inverter. Hence, the value of C must be limited in order to limit the nominal converter power. The choice of L and C is thus a compromise between the converter power and voltage drop.

- **The second step of this procedure** consists of calculating the value of C by defining the reactive power that is to be exchanged by the inverter and the filter.The reactive power exchanged by the converter and the filter is given by equation

$$Q_{exchanged} = \frac{\hat{E}(\omega_1)^2}{2 \cdot \|Z(j\omega_1)\|} = \frac{\hat{E}(\omega_1)^2}{2} \cdot \frac{C\omega_1}{\|1 - LC{\omega_1}^2\|} = \frac{\hat{E}(\omega_1)^2}{2} \cdot C\omega_1 \left(\frac{1}{\|1 - k^2\|} \right) \tag{III.1.7}$$

  where $LC = \frac{1}{{\omega_c}^2}$, $k = \omega_1/\omega_c$, ω_1 is the fundamental frequency, and $\hat{E}(\omega_1)$ is the peak value of the fundamental voltage at the output of the converter.

The maximum value of the capacitor is given by:

$$C_{max} = \frac{2 \cdot Q_{exchanged} \cdot \|1 - k^2\|}{\hat{E}(\omega)^2 \omega_1} \tag{III.1.8}$$

Finally, following the calculation procedure detailed in Appendix E, the series filter values are obtained: $C_{f2} = 108\ \mu F$, $L_{f2} = 956\ \mu H$, $R_{f2} = 0.001\ \Omega$.

2.4.2. Verification of the calculated values

Standard EN 50160, which applies for public distribution systems with voltages below 35kV, specifies limits for the voltage Total Harmonic Distortion (THD_v), as well as for individual voltage harmonic components up to the 25th order. The total harmonic distortion, considering all harmonics up to 40th order, is limited to 8%. The individual voltage harmonic limits are presented in Table.E.3 of Appendix E.

The filter values calculated in the preceding paragraphs have been validated simulating the system of Fig.III.1.15 with the MATLAB toolbox *SimPowerSystems*, and extracting the THD_v values and the individual voltage harmonic components at the filter output. The obtained results are summarized in Table III.1.3.

As it is observed, the THD_v values are below 8% for all the analyzed values of the amplitude modulation index except for $m = 0.1$. If individual voltage components are regarded, this filter does not comply with the limits imposed for harmonics $h = 9$ and $h = 11$ when $m = 0.1$, which coincide with the resonance/cutting frequency of the filter. In spite of this deficiency, the filter values have been validated because for most of the modulation indexes the harmonic values are well below the limits specified by the standard.

Table III.1.3: EN 50160 standard compliance of the series filter.

m	THD_v (V_f)	$\Delta V_L/E_1$	$\forall\ V_f(h)$ comply with EN50160?
1	1.74%	−5%	✓
0.8	0.59%	−5.6%	✓
0.6	1.02%	−6.3%	✓
0.4	1.51%	−7.8%	✓
0.2	2.81%	−12%	✓
0.1	9.43%	−20%	FAIL $h_9 = 3.7\% > 1.5\%$ $h_{11} = 8.38\% > 3.5\%$ $h_{13} = 1.01\% < 3.0\%$

3. Design and characteristics of shunt-side elements

The shunt-side of the UPLC works mainly as an auxiliary system that gives support to the series-side compensator by keeping the DC-link voltage constant. In order to keep the DC voltage constant, it must provide or absorb the active power that is required/disposed by the series-side. This means that, the minimum rating of the shunt-side elements is given by the maximum active power that flows through the DC-link in nominal conditions.

Besides DC voltage support, the shunt-compensator can also absorb or inject reactive power from the grid connection point (at V_1). If reactive power is to be generated, then the rating of the shunt-side elements must be increased.

As depicted in Fig.III.1.16, there are several parameters to estimate and specify in the shunt-branch. Without going very far, it is necessary (i) to establish the type of VSC that is going to be used, (ii) to define the turns-ratio of the transformer, (iii) to estimate the operating powers of the devices, (iv) to calculate the best value of the total impedance, and (v) to distribute the total impedance value between the transformer and the filter.

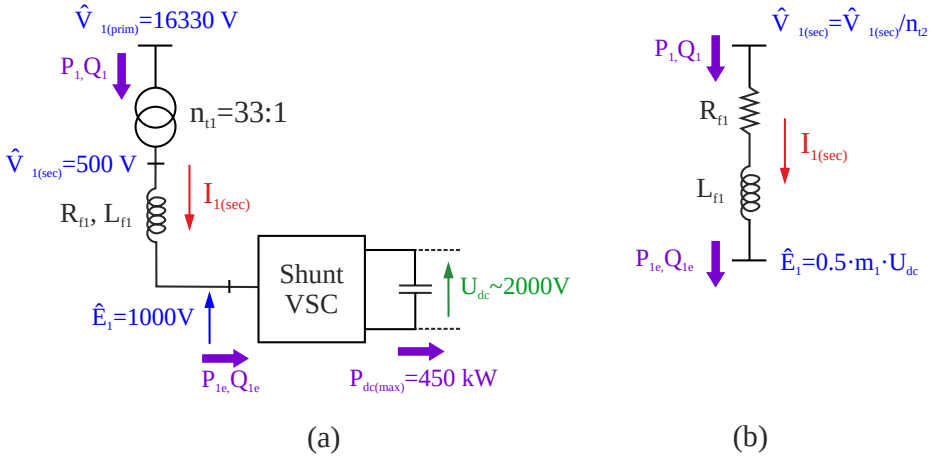


Figure III.1.16: One-line representation of shunt-side

3.1. VSC definition.

In this case, the VSC is the same as the one used in the series side: a typical two-level three-phase VSC with $f_{sw} = 4950\ Hz$ (Fig.III.1.17). Considering that $U_{dc} = 2000\ V$, it is possible to establish the maximum peak phase-voltage at the output of the converter $\hat{E}_{1-max} = 1000\ V$ (when $m_1 = 1$). This value is relevant for the next steps.

3.2. Shunt transformer turns-ratio definition.

The turns-ratio of the shunt transformer determines the reactive power capacity of the shunt-branch. This is, if the turns-ratio is selected such that the voltage at the secondary of the

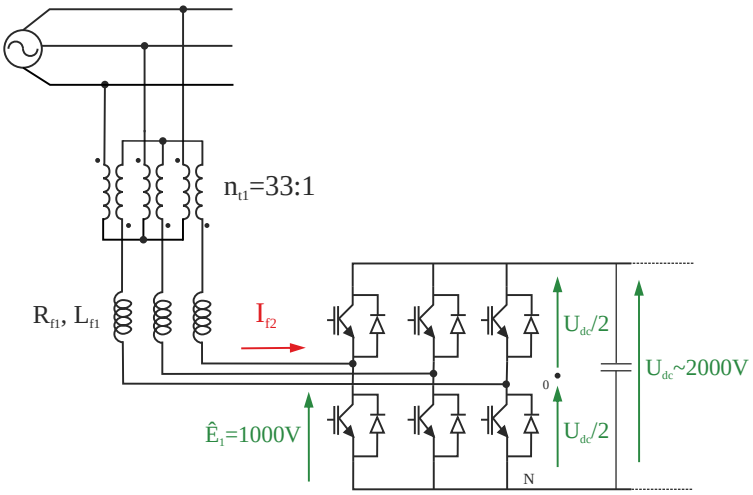


Figure III.1.17: Two-level VSC with IGBTs connected in shunt with the line

transformer is the same as the voltage at the output of the converter ($\hat{V}_{1(sec)} = \hat{E}_1 = 1000\ V$), the shunt-side will not have any reactive power compensation capacity. In a similar manner, if $\hat{V}_{1(sec)} > \hat{E}_1$, then the shunt-branch can only absorb reactive power (inductive) and if $\hat{V}_{1(sec)} < \hat{E}_1$, the shunt-branch can either absorb or inject reactive power. This statement can be better understood observing the following equations, that have been deduced based on Fig.III.1.16.

$$\left[P_1 - \left(\frac{1}{2}\frac{\hat{V}_1^2}{Z_1}cos\epsilon\right)\right]^2 + \left[Q_1 - \left(\frac{1}{2}\frac{\hat{V}_1^2}{Z_1}sin\epsilon\right)\right]^2 = \left(\frac{1}{2}\frac{\hat{V}_1\hat{E}_1}{Z_1}\right)^2 \tag{III.1.9}$$

$$\left[P_{1e} - \left(-\frac{1}{2}\frac{\hat{E}_1^2}{Z_1}cos\epsilon\right)\right]^2 + \left[Q_{1e} - \left(-\frac{1}{2}\frac{\hat{E}_1^2}{Z_1}sin\epsilon\right)\right]^2 = \left(\frac{1}{2}\frac{\hat{V}_1\hat{E}_1}{Z_1}\right)^2 \tag{III.1.10}$$

Expressions (III.1.9) and (III.1.10) indicate that active and reactive powers at the secondary of the transformer (P_1, Q_1) and at the output of the shunt inverter (P_{1e}, Q_{1e}) depend on several parameters: (i) the magnitude of the voltage at the secondary of the transformer ($\hat{V}_{1(sec)}$), (ii) the magnitude of the voltage at the output of the inverter ($\hat{E}_1$), (iii) the magnitude of the shunt impedance, that includes transformer and filter impedances (Z_1), and (iv) the impedance angle (ϵ).

The maximum value of $\hat{E}_1$ is known, $\hat{E}_{1-max} = 1000\ V$, and the impedance angle is $\epsilon = \pi/2$ when the impedance is purely inductive (in reality ϵ is mostly inductive). Fig.III.1.18 plots graphically equations (III.1.9) and (III.1.10) for different values of $\hat{V}_{1(sec)}$ and a purely inductive impedance. From these plots, the following points can be observed:

i) The only way of having $Q_1 < 0$ (capacitive) is to select $\hat{V}_{1(sec)} < \hat{E}_1$. However, the smaller $\hat{V}_{1(sec)}$ is selected, the smaller the available $P_1 - Q_1$ surface area becomes.

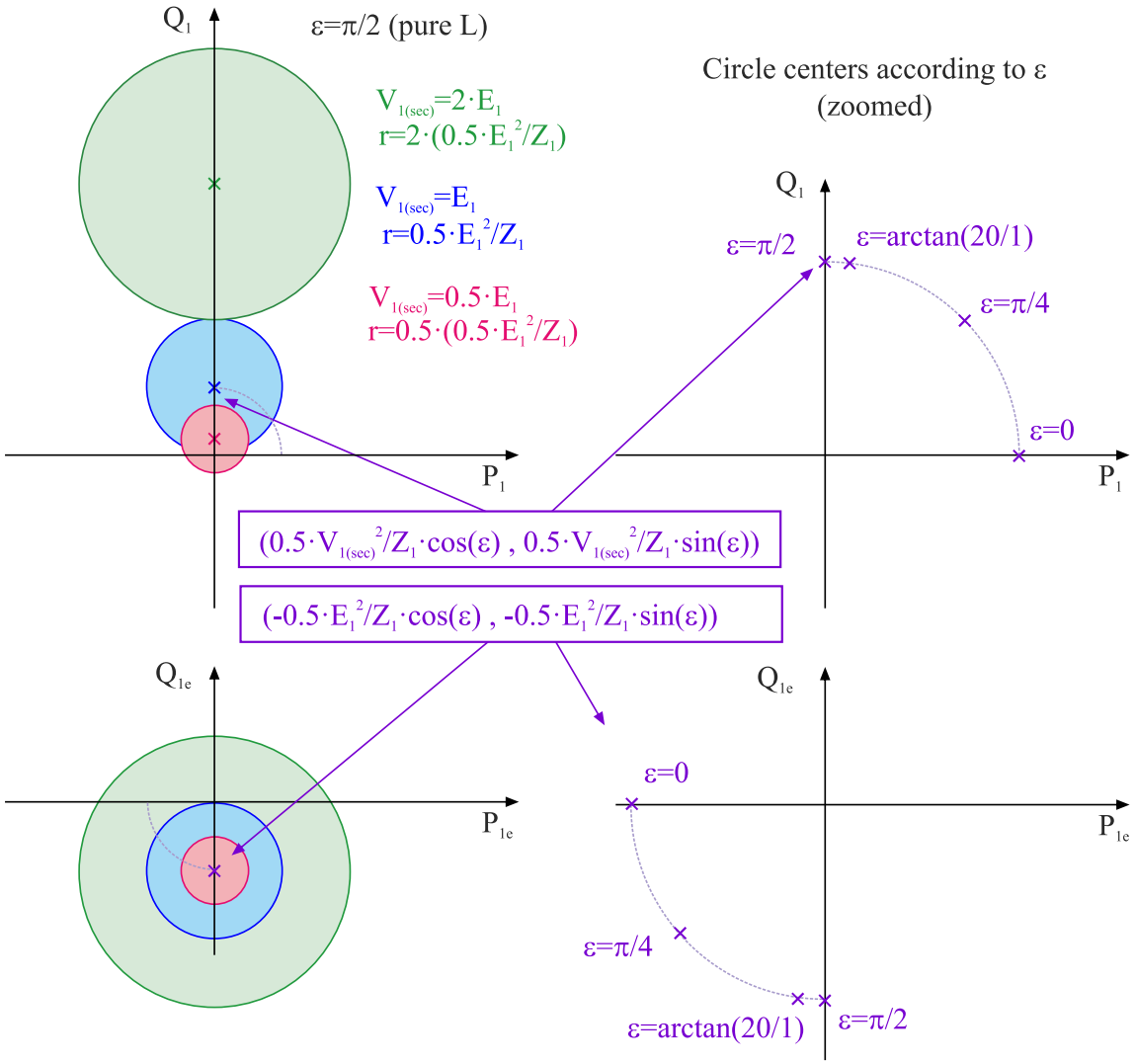


Figure III.1.18: Shunt-side power areas according to $V_{1(sec)}$

ii) Oddly, when $\hat{V}_{1(sec)} < \hat{E}_1$ is selected, Q_{1e} is always negative $Q_{1e} < 0$.

iii) When $\epsilon = \pi/2$ (pure inductance), the centers of the circles are located in $P_{1(0)} = 0$ and $P_{1e(0)} = 0$ but, when ϵ changes the centers move drawing a circunference. When $\epsilon = 0$ (pure resistance), for example, $Q_{1(0)} = 0$ and $Q_{1e(0)} = 0$.

In this work, it has been decided that the shunt actuator has the capacity of injecting reactive power (capacitive) to the grid with the objective of rising the voltage at the connection bus. For this reason, the voltage at the secondary of the transformer is selected to be smaller than the voltage at the output of the inverter ($\hat{V}_{1(sec)} < \hat{E}_1$). The ratio has been arbitrarily chosen to be a half ($(\hat{V}_{1(sec)} = 0.5 \cdot \hat{E}_1 = 500\ V)$). This selection yields the turns-ratio of the shunt transformer,

$$n_{t1} = \frac{16330}{500} = 33 \tag{III.1.11}$$

which is quite high.

3.3. Total shunt impedance definition.

Once the turns-ratio of the transformer is specified, the magnitude of the total shunt-branch impedance can be calculated. The total impedance is obtained from the expression of the maximum active power value flowing throught the converter, that is extracted from equation (III.1.10):

$$P_{1e(max)} = \left(-\frac{1}{2}\frac{\hat{E}_1^2}{Z_1}cos\epsilon\right) + \left(\frac{1}{2}\frac{\hat{V}_1\hat{E}_1}{Z_1}\right) \tag{III.1.12}$$

And, from (III.1.12), the value of Z_1 is calculated:

$$Z_1 = \frac{1}{2}\frac{\hat{E}_1}{P_{1e(max)}}\left[\hat{V}_1 - \hat{E}_1 cos\epsilon\right] \tag{III.1.13}$$

In equation (III.1.13) there are only two unknown variables to define:

- **The impedance angle ϵ**

  The reactance of the impedance is assumed to be 20 times higher than the resistance (similar to transformers). Thus, $\epsilon = atan(20/1) = 87.13\ deg$.

- **The maximum active power coming into the converter $P_{1e(max)}$**

  For this calculation it is assumed that there are no losses in the series path, in the DC-link, and in the converters. The maximum active power absorbed/injected by the series compensator is calculated by analysizing all the operating states of the series compensator when the maximum voltage is injected. This is, by injecting $V_c = 1000\ V$ with $0 \leq \rho \leq 2\pi$ and calculating the resulting powers (P_c and Q_c). As depicted in Fig.III.1.19, the maximum active power injected is $P_{c-max} = 150\ kW$ (per phase). Thus, summing the three phases up, $P_{dc-max} = 3 \cdot 150 = 450\ kW$).

Finally, from equation (III.1.13), the total value of Z_1 is calculated: $Z_1 = 1.5\ \Omega$. The way in which the total shunt impedance is splitted between the transformer and the filter is specified in Appendix E.

3.4. Verification of designed values.

The validity of the chosen solution has been verified by simulating the shunt-branch in *SimPowerSystems* and by comparing current harmonic levels with the values provided by standard IEEE 519-1992, which are supplied in Fig.E.4 of Appendix E. Since the short-circuit level of the chosen case-study is not known, current harmonics and TDD ($TDD = THD_i$) have been compared to the worst case. In all the cases, even at $m_1 = 0.1$, current harmonics are well below the limits established by the standard. This result is expected because the inducance value is high.

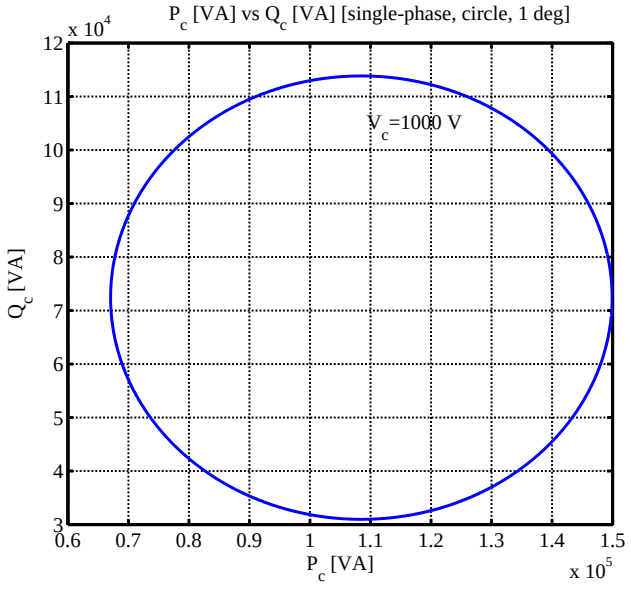


Figure III.1.19: Active and reactive powers needed by the series compensator to inject $V_c = 1000\ V$ at any ρ angles

4. Design and characteristics of the DC-link

DC-link voltage depends on the active power balance between the series-side and the shunt-side. In steady state, the active power demanded by the series-compensator is the same as the one provided by the shunt-compensator ($P_{1e} = P_{2e}$) and hence, the DC-link voltage remains without changes. However, if in all of a sudden the series-compensator demands active power, the shunt-compensator does not react instantaneously and the DC voltage decreases (or increases, depending if the series compensator demands or provides active power). DC-voltage variations depend on two factors: (i) the reaction speed of the shunt control loop, and (ii) the value of the DC capacitor (C_{dc}). In the next lines the procedure that has been used to calculate C_{dc} is described.

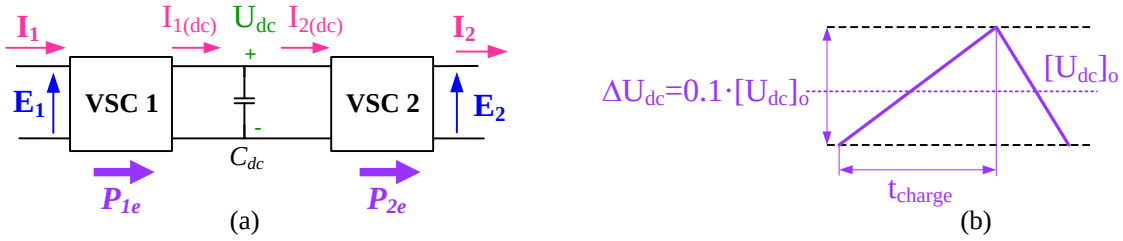


Figure III.1.20: (a) DC-link with converters, (b) DC voltage increment

The dynamics of the DC-link can be modelled looking at DC current relationships and, in

turn, the active power balance:

$$I_{1(dc)} - I_{2(dc)} = C_{dc}\dot{U}_{dc} \tag{III.1.14}$$

$$P_{1e} - P_{2e} = U_{dc} \cdot I_{1(dc)} - U_{dc} \cdot I_{2(dc)} = C_{dc} \cdot U_{dc} \cdot \dot{U}_{dc} \tag{III.1.15}$$

And the small signal version of the power balance equation yields,

$$\Delta P_{1e} - \Delta P_{2e} = C_{dc} \cdot \Delta U_{dc} \cdot [\dot{U}_{dc}]_0 + C_{dc} \cdot [U_{dc}]_0 \cdot \Delta\dot{U}_{dc} \tag{III.1.16}$$

Assuming that the shunt-compensator has not reacted yet ($\Delta P_{1e} = 0$), that the steady-state voltage does not vary ($[\dot{U}_{dc}]_0 = 0$), and that a 10% of voltage change is allowed in a t_{charge} period of time, $\Delta\dot{U}_{dc} = (0.1 \cdot [U_{dc}]_0)/t_{charge}$, the value of C_{dc} can be calculated:

$$\|\Delta P_{2e}\| = C_{dc} \cdot [U_{dc}]_0 \cdot \frac{0.1 \cdot [U_{dc}]_0}{t_{charge}} \qquad \Rightarrow \qquad C_{dc} = \frac{\|\Delta P_{2e}\|}{0.1 \cdot {[U_{dc}]_0}^2} \tag{III.1.17}$$

Then, it is just necessary to establish t_{charge}, $\|\Delta P_{2e}\|$ and $[U_{dc}]_0$, which have been selected to be $t_{charge} = 1\ ms$, $\|\Delta P_{2e}(3ph)|| = 3 \cdot 150 = 450\ kW$, and $[U_{dc}]_0 = 2000\ V$. And the value of C_{dc} yields $C_{dc} = 1125\ \mu F$.

The calculated capacitor value guarantees that, when the maximum active power is demanded, $P_{2e-max}(3ph) = 450\ kW$, and before that the shunt-compensator reacts, the DC voltage will increase of a 10% of the nominal value (this is, 200 V) in a 1 ms time. After consulting several constructor datasheets [103, 104, 105, 106], a capacitor value below 3000 μF seems a reasonable value .

Sometimes, it is necessary to model a fictitious resistance connected in parallel with the DC-link [107]. The objective of this resistance is to model the power losses of the converters for simulations. The calculation of this resistance is done assuming a percentage of power losses in the converters. An efficiency of $\eta \approx 98\%$ is a rather common rate, meaning that the losses in the inverter are around 2%. Since the maximum active power flowing througth the DC-link is known ($P_{dc-max} = 450\ kW$), the fictitious loss-resistance is calculated according to equation,

$$R_{dc} = \frac{{U_{dc}}^2}{2 \cdot P_{conv-loss}} = \frac{{U_{dc}}^2}{2 \cdot (1-\eta) \cdot 3 \cdot P_{conv(1ph)}} = 222\ \Omega \tag{III.1.18}$$

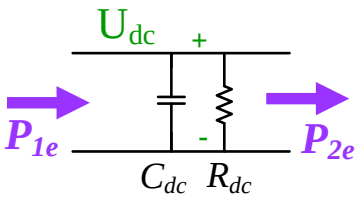


Figure III.1.21: Fictitious R_{dc} connected in the DC-link

5. UPLC sizing for power quality enhancement and related design trade-offs

The design procedure described above corresponds to a nominal operating state where power-flow is controlled dynamically. In the previous procedure voltages and currents are considered balanced and distortion-free. However, the UPLC is also able to compensate for harmonics, unbalances and voltage sags. In the next paragraphs the aspects that should be considered to update the base-rating of the UPLC according to power-quality objectives are discussed.

5.1. Steady-steate harmonic voltage and current compensation

Steady-state harmonic compensation does not add much complexity to the apparatus design, but little changes in relation to the nominal design are required. On the one hand, the rating of the components need to be updated in order to handle the additional harmonics components and, on the other hand, the filter design must be reviewed in order to let the compensation harmonics pass through the filters.

Harmonic voltage compensation corresponds to the series sub-circuit, and harmonic current compensation corresponds to the shunt sub-circuit. For the series sub-circuit, the new rating for the voltage is given by

$$\hat{V}_{c(r)} = \sqrt{\hat{V}_{c(1)}^2 + \sum_{h=2}^{M} \hat{V}_{c(h)}^2} \tag{III.1.19}$$

where M is the highest harmonic order to be compensated, the subscript r stands for *rated*, and the subscript 1 denotes the fundamental value.

This new voltage rating is multiplied by the rated current, to obtain the updated rated apparent power of the series-devices

$$S_{c(r)} = \frac{\hat{V}_{c(r)} \cdot \hat{I}_{2(r)}}{2} = \frac{\hat{V}_{c(1)} \cdot \hat{I}_{2(1)}}{2} \cdot \sqrt{1 + \frac{\sum_{h=2}^{M} \hat{V}_{c(h)}^2}{\hat{V}_{c(1)}^2}} = S_c(1) \cdot \sqrt{1 + {THD_v}^2} \tag{III.1.20}$$

Equation (III.1.20) demonstrates that the rating of series components, when it comes to compensate for voltage harmonics, must be multiplied by a coefficient that depends on the THD_v value of the signal that is to be compensated.

Similarly, the rating of the shunt-components depends on the THD_i value of the compensating signal. The new current rating is defined as

$$\hat{I}_{1(r)} = \sqrt{\hat{I}_{1(1)}^2 + \sum_{h=2}^{M} \hat{I}_{1(h)}^2} \tag{III.1.21}$$

and the apparent power rating of the shunt-devices gets

$$S_{1(r)} = \frac{\hat{V}_{1(r)} \cdot \hat{I}_{1(r)}}{2} = \frac{\hat{V}_{1(1)} \cdot \hat{I}_{1(1)}}{2} \cdot \sqrt{1 + \frac{\sum_{h=2}^{M} \hat{I}_{1(h)}^2}{\hat{I}_{1(1)}^2}} = S_1(1) \cdot \sqrt{1 + {THD_i}^2} \qquad \text{(III.1.22)}$$

Thus, the apparent power of the series and shunt-devices need to be updated by a factor $\sqrt{1 + {THD_v}^2}$ and $\sqrt{1 + {THD_i}^2}$, respectively. It must be mentioned that THD_i levels of some home appliances can have pretty high THD_i levels. Computers, for example, can reach $THD_i = 220$ %, and low consumption lamps can emit $THD_i = 95\%$, at low voltage levels [108].

Besides updating the components of the UPLC device, it is also necessary to review the design of the filters to guarantee that the harmonic components that are to be compensated are not damped by the filters. In general, it is necessary to higher the bandwidth of the filters, which is obtained by decreasing the values of the inductances and the capacitances.

5.2. Steady-state voltage and current unbalance compensation

For voltage and current unbalance compensation the same reasoning followed in the preceding section is followed. The new voltage rating when voltage unbalance is compensated is,

$$\hat{V}_{c(r)} = \sqrt{\hat{V}_{c(1+)}^2 + \hat{V}_{c(1-)}^2} \qquad \text{(III.1.23)}$$

where $\hat{V}_{c(1+)}$ stands for the injected fundamental positive sequence voltage, and $\hat{V}_{c(1-)}$ stands for the injected fundamental negative sequence voltage.

And the new rating for the current rating, when compensating for unbalanced currents gets,

$$\hat{I}_{1(r)} = \sqrt{\hat{I}_{1(1+)}^2 + \hat{V}_{1(1-)}^2} \qquad \text{(III.1.24)}$$

where $\hat{I}_{1(1+)}$ stands for the injected fundamental positive sequence current, and $\hat{I}_{1(1-)}$ stands for the injected fundamental negative sequence current.

Thus, the updated series-side and shunt-side ratings get

$$S_{c(r)} = \frac{\hat{V}_{c(r)} \cdot \hat{I}_{2(r)}}{2} = \frac{\hat{V}_{c(1+)} \cdot \hat{I}_{2(1+)}}{2} \cdot \sqrt{1 + \left[\frac{\hat{V}_{c(1-)}}{\hat{V}_{c(1+)}}\right]^2} \qquad \text{(III.1.25)}$$

$$S_{1(r)} = \frac{\hat{V}_{1(r)} \cdot \hat{I}_{1(r)}}{2} = \frac{\hat{V}_{1(1+)} \cdot \hat{I}_{1(1+)}}{2} \cdot \sqrt{1 + \left[\frac{\hat{I}_{1(1-)}}{\hat{I}_{1(1+)}}\right]^2} \qquad \text{(III.1.26)}$$

The apparent power of the series and shunt-side devices need to be updated by a factor that depends on the unbalance level that is to be compensated.

5.3. Voltage sag compensation

It is rather complex to design an apparatus that is able to control power-flow during nominal conditions and compensate for voltage sags during transients. In order to clarify this statement an example is proposed. This example, which is illustrated in Fig.III.1.22, discusses the incompatibility of addressing both functions with the same apparatus design. Two design approaches are hereby compared.

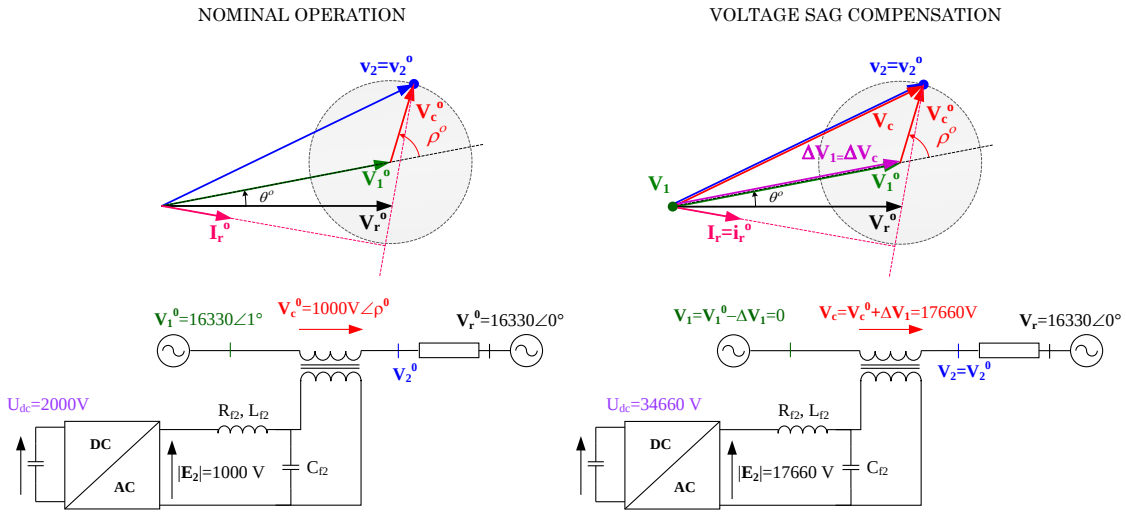


Figure III.1.22: Example: nominal and voltage sag operation of the series-branch

- **In the first design approach**, the apparatus is designed to operate satisfactorily during steady-state conditions. In these conditions, the series compensator can inject a maximum voltage of $\hat{V}_c^0 = 1000\ V$ and the DC-bus voltage is charged to ${U_{dc}}^0 = 2000\ V$. This means that, when the modulation index is the unity (${m_2}^0 = 1$), the phase voltage at the output of the inverter is $\hat{E}_2^0 = 1000\ V$. Moreover, depending on the operating point, the modulation index can vary from $0 - 1$.

- **In the second design approach**, the apparatus is designed to compensate for voltage sags (and, indirectly, for power flow control). If the worst case is regarded, this is, when the voltage at the sending-end is zero ($\hat{V}_1 = 0\ V$), the maximum voltage that the series-compensator must inject is $\hat{V}_c = \hat{V}_c^0 + \Delta\hat{V}_1 = 17660\ V$. But this voltage can only be generated if the DC-bus voltage is, at least, double $U_{dc}^0 = 34660\ V$. If DC-bus voltage is charged up to 34660 V, when the apparatus works in steady state, the modulations index drops to less than $m_2^0 = 2 \cdot 1000/34660 = 0.05$, which is an extremely low value for a nominal operating point. Such modulation index generates a high voltage distortion that requires the update of the filter components. Furthermore, in this approach, the full capacity of the apparatus is only used during deep voltage sag conditions, which do not occur frequently. Thus, component capacities are under-used and the apparatus performance is degraded during nominal operation.

As it is observed, with the first approach it is not possible to compensate for voltage sags of more than 1000 V, but it works adequately under nominal conditions. The second approach compensates deep voltage sags, but is not well adapted to work under nominal conditions. Obviously, non of the solutions provides an optimal performance. With the second approach, the design of the filters, the transformer and the DC capacitor becomes quite complicated because they need to be adapted to very divergent conditions. A similar thing occurs with the shunt-side. During nominal conditions the current magnitude that must be absorbed by the shunt-branch corresponds to rated values. But, when a voltage sag occurs, the series compensator requires a much higher current to be absorbed from the shunt-branch. These extreme operating conditions make it complicate to design the passive elements of the system.

5.3.1. Conclusion

A UPLC is a versatil apparatus that can theoretically attain a large variety of functions. However, when it comes to the sizing and design of the apparatus, it is necessary to define, specify and bound aspects such as the particular characteristics of the insertion site, the objectives that can be achieved, the operation range, and the behaviour that the device will have under steady-state and transient conditions.

Chapter III.1 proposes a design procedure for an UPLC that is mostly dedicated to control power-flow in steady-state (during transient states, the series-side is assumed to be bypassed). This constrainted design approach yiels a reasonable size of the device but it constitutes a limitation when transients or power-quality phenomena are to be compensated. As a complement to the presented analysis, the considerations that must be done in order to achieve additional objectives are discussed:

i.- **For steady-state harmonics or unbalance compensation**, the size increase depends on the THD or unbalance rate that is to be compensated. The greater the THD or unbalance rate is, the higher the UPLC size will be. Another important consideration comes from the switching frequency of the converters. If the harmonic order to be compensated increases, the switching frequency needs also to be increased, generating further losses.

ii.- **For transient events**, such as voltage sags, the size of the apparatus also needs to be updated according to the depth of the voltage fault. In this case, the apparatus needs to be over-dimensioned just for a sporadic use. This fact presents a problem in the design and in the steady-state performance of the device. It may therefore not be judicious to join power-flow and voltage-sag compensation in the same device.

The conclusion is that a good trade-off does not exist between both design approaches (i.e. steady-state and transient): either power-flow is controlled, or either voltage-sags are compensated. The same apparatus cannot integrate both functions without loosing overal performance and without over-dimensioning the components. The only possible solution consists in using two multilevel converters with a very high number of levels that allow the removal

of the filters (or almost). The main drawback of this solution is that all the components of the UPLC need to be overdimensioned and the apparatus would become too expensive for an occasional use.

Chapter III.2

Modelling of UPLC

As for other devices connected to the power system, the mathematical modelling of the UPLC requires a comprehensive knowledge of fundamental power system concepts. With the aim of enhancing the knowledge and the understanding of non specialist readers, these essential concepts have been adequatly summarized and described in Appendix B. Appendix B provides the reader with a valuable compendium of four relevant topics:

- It introduces the notion of phasor and it presents the various ways of representing three-phase signals in different frames; the natural *abc* frame, the static $\alpha\beta 0$ frame, and arbitrary frequency rotating frames (e.g. *dq*). The conversion between different frames is also described.
- It explains the decomposition of three-phase signals into symmetrical components, and provides generic expressions, in terms of symmetrical components, of three-phase signals in the *abc* frame and in phasor form.
- It portrays the the basic ideas of the most well-known power theories (i.e. The Generalized Non-Active Power Theory and The PQ theory).

The per-unit conversion procedure that has been followed in this PhD work is described in Appendix E.

The specialist reader may skip Appendix B and Appendix E if he/she feels acquainted with the abovementioned concepts. The upcoming chapter starts by exposing the considered modelling assumptions, and continues by presenting the models of different parts of the UPLC.

A one-line representation of the whole UPLC model in per-unit system is illustrated in Fig.III.2.1. The complete UPLC model can be subdivided into three main parts: (i) the series-side model, which includes the overhead-line or cable, the series transformer, the series filter, and the series-side converter, (ii) the shunt side-model, where the transformer and the filter are joint together, and (iii) the DC-link.

- The **series-side model** can be modelled with two levels of abstraction. The **highest level of abstraction** considers that the voltage provided by the converter and the filter, $\mathbf{v_f}$, are totally ideal (sinusoidal). This type of modelling is useful to understand the influence of the series-injected voltage in the line current. In this case, two options have been observed: (1) the series-injection model when a RL line is used, and (2) the series-injection model when a cable is used. For completing the second option the model of a generic N π-section cable is provided thereby. The **lower level of abstraction** is that

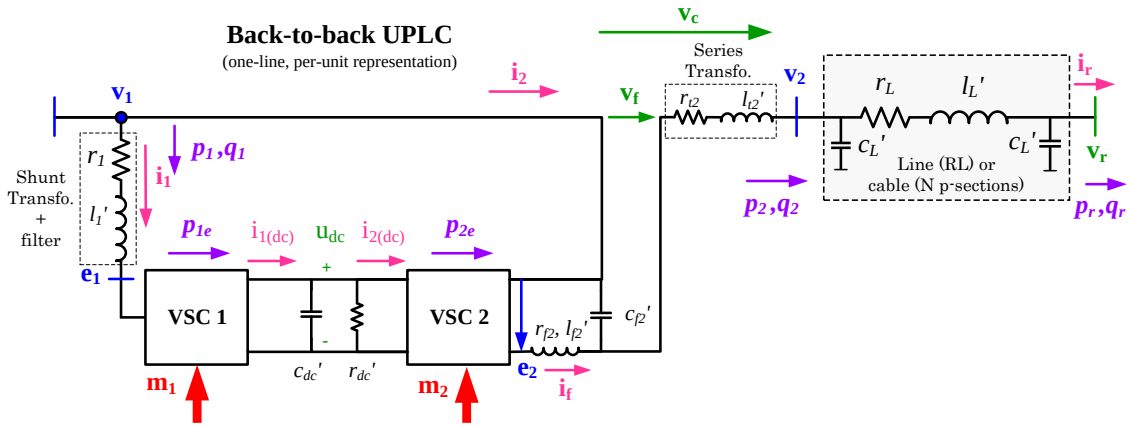


Figure III.2.1: One line representation of the whole UPLC model

where the influence of series filter is considered. The model of the series filter is therefore described to be included in the most ideal model.

- The **shunt-side model** considers the summation of the transformer and the filter impedance and treats them as a single impedance. This impedance is located between two voltage terminals: one is connected to the grid, $\mathbf{v_1}$, and the other is connected to the shunt-side converter, e_1.
- The **DC-link** can be modelled following different approaches. On the one hand, it is possible to model the losses on the converters and DC components by a lumped resistance connected in parallel with the DC capacitor [107]. On the other hand, it is possible to model the input and output powers of the DC link with different levels of detail according to the number of reference frames considered [109, 31, 33, 32].

1. Modelling assumptions

The models that will be subsequently presented, consider the following assumptions:

- The models are developped in continuous-time.
- The discrete nature of the VSC is not taken into consideration. The PWM-based VSC is described as an average model (modelling of converters is further explained in section 7.).
- The series-side filter (r_{f2}, l'_{f2}, c'_{f2}) and the series-side transformer (r_{t2}, l'_{t2}, c'_{t2}) are included in the model. The shunt-side transformer (r_{t1}, l'_{t1}) and filter (r_{f1}, l'_{f1}) are considered together as r_1, l'_1.
- All the parameters, excluding frequency and time, are expressed in per-unit values, and represented by lower-case symbols. The per-unit conversion has been explained in Appendix B.

- For limiting the volume of the set of equations, the models are only presented in the fundamental positive rotating frame ($d_{1+}q_{1+}$). The models in the negative rotating frame ($d_{1-}q_{1-}$) are obtained by changing the sign of ω_1 in the expressions corresponding to the positive rotating frame. The models in the static $\alpha\beta$ frame are obtained by making the coupling between rotating axis zero ($\omega_1 = 0$).
- The zero-sequence is not considered in the models because a three-phase three-wire apparatus connection has been assumed.
- The condensed notation of the type $\mathbf{x}^{(\alpha\beta)}$ or $\mathbf{x}^{(dq)}$ that makes use of bold symbols corresponds to a vector of components $\mathbf{x}^{(\alpha\beta)} = [x_\alpha \; x_\beta]^t$ and $\mathbf{x}^{(dq)} = [x_d \; x_q]^t$. Depending on the case, the same condensed notation can represent the same thing but in a different format (complex form): $\mathbf{x}^{(\alpha\beta)} = x_\alpha + jx_\beta$ and $\mathbf{x}^{(dq)} = x_d + jx_q$.
- The matrices and other details of the models are specified in Appendix 3..

2. Modelling of the series injection with RL line

In this model the series injection branch is modelled as an ideal voltage source (higher abstraction level), and the interconnection line is a RL line. The objective of this model is to analyze the impact of the series voltage injection in the currents, and thus, powers, flowing through different points of the circuit.

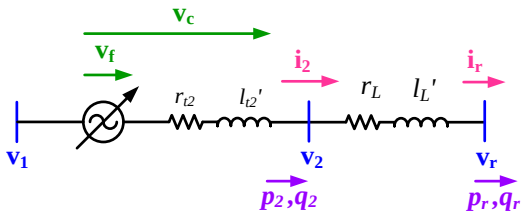


Figure III.2.2: One-line diagram of the series injection with a RL line

As a first example, the models in static ($\alpha\beta$), positive rotating ($dq+$), and negative rotating (dq-) frames are presented but, in the rest of the developments, just the models in the positive rotating frame will be presented. The other two models can be deduced from the positive rotating frame model by:

(i) Making the couplings between rotating axis zero. This is, making the all non-diagonal terms zero, for obtaining the model in static $\alpha\beta$ frame.

(ii) Changing the sign of all the ω terms, for obtaining the model in the negative rotating frame.

The model in static $\alpha\beta$ coordinates is

$$\frac{d\,\mathbf{i_2}^{(\alpha\beta)}}{dt} = \mathbf{A_{RL(\alpha\beta)}} \cdot \mathbf{i_2}^{(\alpha\beta)} + \mathbf{B_{RL}} \cdot \mathbf{v_f}^{(\alpha\beta)} + \mathbf{B_{RL}} \cdot (\mathbf{v_1}^{(\alpha\beta)} - \mathbf{v_r}^{(\alpha\beta)})$$

$$\frac{d}{dt}\begin{bmatrix} i_{2_\alpha} \\ i_{2_\beta} \end{bmatrix} = \begin{bmatrix} -r_{se}/l'_{se} & 0 \\ 0 & -r_{se}/l'_{se} \end{bmatrix} \begin{bmatrix} i_{2_\alpha} \\ i_{2_\beta} \end{bmatrix} + \begin{bmatrix} 1/l'_{se} & 0 \\ 0 & 1/l'_{se} \end{bmatrix} \begin{bmatrix} v_{f_\alpha} \\ v_{f_\beta} \end{bmatrix} + \begin{bmatrix} 1/l'_{se} & 0 \\ 0 & 1/l'_{se} \end{bmatrix} \begin{bmatrix} v_{1_\alpha} - v_{r_\alpha} \\ v_{1_\beta} - v_{r_\beta} \end{bmatrix} \tag{III.2.1}$$

where $r_{se} = r_{t2} + r_L$ and $l'_{se} = l'_{t2} + l'_L$.

And, the model in $dq+$ coordinates is

$$\frac{d\,\mathbf{i_2}^{(dq+)}}{dt} = \mathbf{A_{RL(dq+)}} \cdot \mathbf{i_2}^{(dq+)} + \mathbf{B_{RL}} \cdot \mathbf{v_f}^{(dq+)} + \mathbf{B_{RL}} \cdot (\mathbf{v_1}^{(dq+)} - \mathbf{v_r}^{(dq+)})$$

$$\frac{d}{dt}\begin{bmatrix} i_{2_{d+}} \\ i_{2_{q+}} \end{bmatrix} = \begin{bmatrix} -r_{se}/l'_{se} & \omega \\ -\omega & -r_{se}/l_{se}{}' \end{bmatrix} \begin{bmatrix} i_{2_{d+}} \\ i_{2_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_{se} & 0 \\ 0 & 1/l'_{se} \end{bmatrix} \begin{bmatrix} v_{f_{d+}} \\ v_{f_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_{se} & 0 \\ 0 & 1/l'_{se} \end{bmatrix} \begin{bmatrix} v_{1_{d+}} - v_{r_{d+}} \\ v_{1_{q+}} - v_{r_{q+}} \end{bmatrix} \tag{III.2.2}$$

Finally, the model in $dq-$ coordinates is

$$\frac{d\,\mathbf{i_2}^{(dq-)}}{dt} = \mathbf{A_{RL(dq-)}} \cdot \mathbf{i_2}^{(dq-)} + \mathbf{B_{RL}} \cdot \mathbf{v_f}^{(dq-)} + \mathbf{B_{RL}} \cdot (\mathbf{v_1}^{(dq-)} - \mathbf{v_r}^{(dq-)})$$

$$\frac{d}{dt}\begin{bmatrix} i_{2_{d-}} \\ i_{2_{q-}} \end{bmatrix} = \begin{bmatrix} -r_{se}/l'_{se} & -\omega \\ \omega & -r_{se}/l_{se}{}' \end{bmatrix} \begin{bmatrix} i_{2_{d-}} \\ i_{2_{q-}} \end{bmatrix} + \begin{bmatrix} 1/l'_{se} & 0 \\ 0 & 1/l'_{se} \end{bmatrix} \begin{bmatrix} v_{f_{d-}} \\ v_{f_{q-}} \end{bmatrix} + \begin{bmatrix} 1/l'_{se} & 0 \\ 0 & 1/l'_{se} \end{bmatrix} \begin{bmatrix} v_{1_{d-}} - v_{r_{d-}} \\ v_{1_{q-}} - v_{r_{q-}} \end{bmatrix} \tag{III.2.3}$$

As it is observed, in rotating coordinates a coupling, ω, between axes occurs. This coupling has a different sign according to the rotating direction of the frame.

Alternatively, it is possible to represent these models in the frequency domain using Laplace operators. Fig.III.2.3 shows a compact representation of the series-side with a RL cable. In this figure both axes (d and q) have been lumped in a single-line diagram, where the bold-symbols represent $\mathbf{x} = x_d + jx_q$ type vector signals.

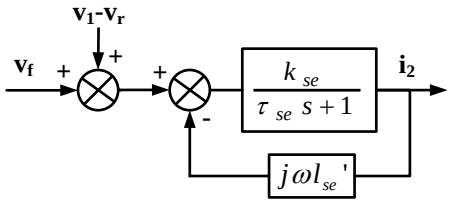


Figure III.2.3: Series side model with RL in the frequency domain

3. Modelling of the series injection with a cable

The series-injection model provides the value of $\mathbf{i_2}$, having the ideal injected series voltage, $\mathbf{v_f}$, as input, and $\mathbf{v_1}$ and $\mathbf{v_2}$ as perturbations (Fig.III.2.4). The cable model developped next provides the value of $\mathbf{v_2}$, and has $\mathbf{i_2}$ as input.

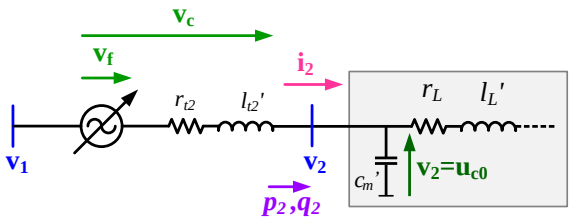


Figure III.2.4: One-line diagram of the series injection with a cable

The model equations in positive rotating frame are,

$$\frac{d\,\mathbf{i_2}^{(dq+)}}{dt} = \mathbf{A_{t2(dq+)}} \cdot \mathbf{i_2}^{(dq+)} + \mathbf{B_{t2}} \cdot \mathbf{v_f}^{(dq+)} + \mathbf{B_{t2}} \cdot (\mathbf{v_1}^{(dq+)} - \mathbf{v_2}^{(dq+)})$$

$$\frac{d}{dt}\begin{bmatrix} i_{2_{d+}} \\ i_{2_{q+}} \end{bmatrix} = \begin{bmatrix} -r_{t2}/l'_{t2} & \omega \\ -\omega & -r_{t2}/l_{t2}{}' \end{bmatrix} \begin{bmatrix} i_{2_{d+}} \\ i_{2_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_{t2} & 0 \\ 0 & 1/l'_{t2} \end{bmatrix} \begin{bmatrix} v_{f_{d+}} \\ v_{f_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_{t2} & 0 \\ 0 & 1/l'_{t2} \end{bmatrix} \begin{bmatrix} v_{1_{d+}} - v_{2_{d+}} \\ v_{1_{q+}} - v_{2_{q+}} \end{bmatrix} \quad \text{(III.2.4)}$$

4. Cable modelling

Cables can be modelled in very different ways according to the frequency range of interest and the required level of accuracy. The following lines provide basic information on mathematical modelling of cables for simulations.

4.1. General aspects

A cable can be described as a succession of infinitisimal length units composed by a distributed resistance, inductance, conductance and a capacitance, as shown in Fig.III.2.5.

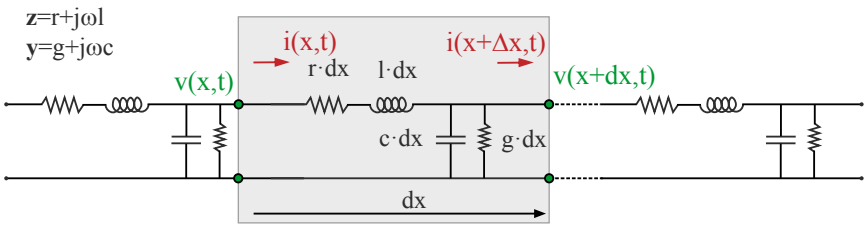


Figure III.2.5: Differential sections of a cable

The current and the voltage along the line are a function of the distance x and the time t. The voltage and current difference between points x and dx can be written as,

$$\begin{aligned} v(x+dx,t) - v(x,t) &= -\frac{\partial v}{\partial x}dx \\ i(x+dx,t) - i(x,t) &= -\frac{\partial i}{\partial x}dx \end{aligned} \tag{III.2.5}$$

where,

$$\begin{aligned} \frac{\partial v}{\partial x}dx &= -\left(ri + l\frac{di}{dt}\right)dx \\ \frac{\partial i}{\partial x}dx &= -\left(gv + c\frac{dv}{dt}\right)dx \end{aligned} \tag{III.2.6}$$

As it can be observed from equations (III.2.6), voltage and current equations are a coupled system of partial differential equations.

- The **distributed resistance**, r, expressed in [Ω/unit length], represents the losses in the conductor. Its value depends mainly on the resistivity and the cross-section of the conductor, but other factors such as temperature, or frequency (skin effect) also influence it.
- The **distributed inductance**, l, designed in [H/unit length], represents the self and mutual flux-linkage of the cable with itself and with the surrounding cables. The disposition of the cables in trefoil or plain configurations have an impact on the inductance value.
- The **distributed capacitance**, c, expressed in [C/unit length], represents the capacitance between the conductor and the shield, and between phases. Capacitance is usually much larger in cables than in overhead-lines (OHLs) due to the existance of a shield.
- Finally, the **distributed conductance**, g, expressed in [S/unit length], accounts for real power loss between conductors or between conductors and ground. This power loss is due to leakage currents at the dielectric material. Conductance is usually neglected in power system studies because it is a very small component of the shunt admitance.

Many cable models consider that the distributed parameters of the cable are constant but, in reality, they are frequency dependent (i.e. $r(\omega)$, $l(\omega)$, $g(\omega)$, $c(\omega)$). Notably, the skin effect, which gives rise to a lower current density at the conductor core when frequency increases, has a substantial effect on the resistance of the cable.

Depending on the expected accuracy and required simulation conditions, cable modelling can be either a rather simple or a very complex issue. Regarding modelling trends, three classifications can be made: (i) models that assume the parameters constant, and models that account for the frequency dependency of parameters, (ii) models that use lumped paramenters, and models that use distributed parameters, and (iii) models for steady-state studies, and

models for transient studies. In Fig.III.2.6 this classification is graphically illustrated.

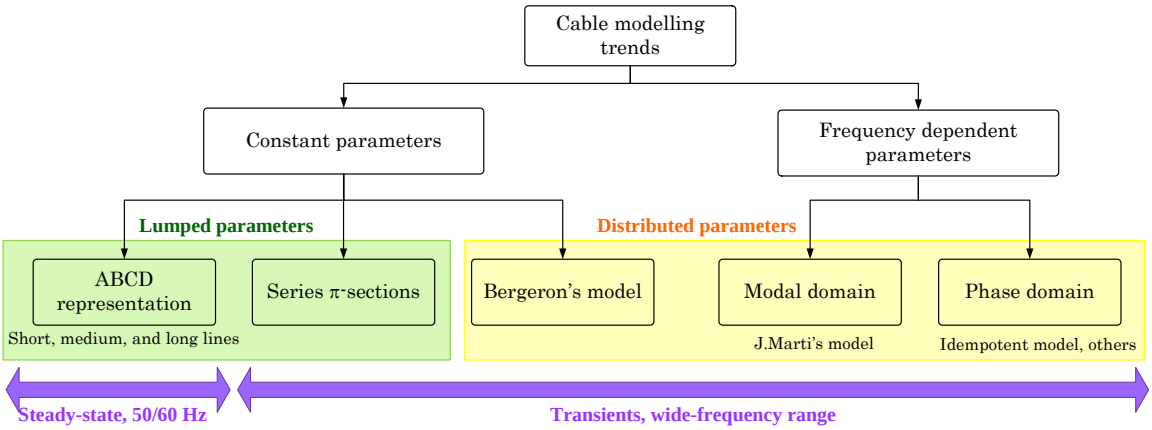


Figure III.2.6: Classification of cable modelling trends [110].

4.1.1. Steady-state modelling of cables

In case of stationary and harmonic signals, it is possible to solve the coupled system of partial differential equations presented in (III.2.6) by using a complex transformation. This is, considering that the voltage and current expressions as:

$$\begin{aligned} v &= \Re\{V(x)e^{j\omega t}\} \\ i &= \Re\{I(x)e^{j\omega t}\} \end{aligned} \tag{III.2.7}$$

Then, the partial derivatives can be written as ordinary differential equations as variables $V(x)$ and $I(x)$ only depend on x:

$$\begin{aligned} \frac{dV(x)}{dx} &= -(r + j\omega l)I(x) = -\mathbf{z}I(x) \\ \frac{dI(x)}{dx} &= -(g + j\omega c)V(x) = -\mathbf{y}V(x) \end{aligned} \tag{III.2.8}$$

where $\mathbf{z}$ and $\mathbf{y}$ are the distributed impedance and admittances $\mathbf{z} = r + j\omega l$ and $\mathbf{y} = g + j\omega c$, respectively.

The separation of variables is obtained by differentiating both equations and combining them with equations (III.2.7), which yields:

$$\begin{aligned} \frac{d^2V(x)}{dx^2} &= \mathbf{zy}V(x) = \gamma^2 V(x) \\ \frac{d^2I(x)}{dx^2} &= \mathbf{zy}I(x) = \gamma^2 I(x) \end{aligned} \tag{III.2.9}$$

where $\gamma = \sqrt{\mathbf{zy}} = \sqrt{(r + j\omega l)(g + j\omega c)}$ $[m^{-1}]$ is known as the propagation constant. The propagation constant γ can also be expressed as $\gamma = \alpha + j\beta$, where α stands for the damping

factor. In lossless lines $\alpha = 0$.

The general solutions of equations (III.2.9) are

$$\begin{aligned} V(x) &= C_1 e^{-\gamma x} + C_2 e^{+\gamma x} \\ I(x) &= \frac{C_1}{Z_v} e^{-\gamma x} - \frac{C_2}{Z_v} e^{+\gamma x} \end{aligned} \tag{III.2.10}$$

where Z_v [Ω] is the surve or wave impedance.

Alternatively, equations (III.2.10) can also be written in terms of hyperbolic functions as,

$$\begin{aligned} V(x) &= K_1 \cosh(\gamma x) - K_2 \sinh(\gamma x) \\ I(x) &= \frac{K_2}{Z_v} \cosh(\gamma x) - \frac{K_1}{Z_v} \sinh(\gamma x) \end{aligned} \tag{III.2.11}$$

where $K_1 = C_1 + C_2$ and $K_2 = C_1 - C_2$.

If the sending-end point is located as $x = 0$ and the receiving-end is considered in $x = L$, where L is the line distance between the receiving- and the sending-end, then:

$$\begin{aligned} V_s &= V_{(x=0)} = K_1 \\ I_s &= I_{(x=0)} = \frac{K_2}{Z_v} \end{aligned} \tag{III.2.12}$$

These changes allow re-writting equations (III.2.11) in a two-port form as,

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} = \begin{bmatrix} \cosh(\Gamma) & Z_v \sinh(\Gamma) \\ \dfrac{1}{Z_v} \sinh(\Gamma) & \cosh(\Gamma) \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} \tag{III.2.13}$$

or in a PI-model form as,

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} \cosh(\Gamma) & Z_v \sinh(\Gamma) \\ \dfrac{1}{Z_v} \sinh(\Gamma) & \cosh(\Gamma) \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} = \begin{bmatrix} 1 + \dfrac{\mathbf{Z'Y'}}{2} & \mathbf{Z'} \\ \mathbf{Y'} + \dfrac{\mathbf{Z'Y'^2}}{4} & 1 + \dfrac{\mathbf{Z'Y'}}{2} \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} \tag{III.2.14}$$

where $\mathbf{Z'} = Z_v \sinh(\Gamma)$ and $\mathbf{Y'} = \dfrac{2}{Z_v} \tanh(\Gamma/2)$.

If the length of the cable, L, is small in comparison with the traveling wave-length, λ, the traveling time of the electromagnetic wave can be neglected. The wavelength of the travelling wave is given by equation

$$\lambda = \frac{v_{line}}{f} = \frac{1}{f\sqrt{lc}} = \frac{v_{\text{light}}}{f\sqrt{\mu_r \varepsilon_r}} \tag{III.2.15}$$

where l and c are the distributed inductance and capacitance values, v_{light} denotes the speed of the light in vacuum ($3 \cdot 10^8$ m/s), μ_r is the relative permeability of the dielectric (where $\mu_0 = 4\pi \cdot 10^7$ H/m), and ε_r is the relative dielectric constant (where $\varepsilon_0 = 8.854 \cdot 10^{-12}$ F/m).

According to equation (III.2.15), the length of the travelling wave depends on the constructive characteristics of the cable and on its frequency. For low frequencies the wavelength is high and thus, if the cable is short, it is possible to neglect the traveling time of the wave. However, if the cable is long, this approximation may not be possible even for low frequencies.

When the travelling time of the electromagnetic wave is neglected, equations (III.2.13) become:

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} = \begin{bmatrix} 1 + \dfrac{\mathbf{ZY}}{2} & \mathbf{Z} \\ \mathbf{Y} + \dfrac{\mathbf{ZY}^2}{4} & 1 + \dfrac{\mathbf{ZY}}{2} \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} \tag{III.2.16}$$

where $\mathbf{Z} = \mathbf{z}L = (r + j\omega l)L$ and $\mathbf{Y} = \mathbf{y}L = (g + j\omega c)L$.

The simplified equations are obtained by neglecting the higher-order terms of the Taylor series of $\sinh(\Gamma)$ and $\tanh(\Gamma/2)$:

$$\begin{aligned} \mathbf{Z}' &= Z_v \sinh(\Gamma) = Z_v \cdot \left(\Gamma + \underbrace{\frac{\Gamma^3}{3!} + \frac{\Gamma^5}{5!} + \cdots}_{=0} \right) \approx Z_v \cdot \Gamma = \mathbf{Z} \\ \mathbf{Y}' &= \frac{2}{Z_v} \tanh(\frac{\Gamma}{2}) = \frac{2}{Z_v} \cdot \left(\frac{\Gamma}{2} \underbrace{- \frac{\Gamma^3}{6} + \frac{\Gamma^5}{15} + \cdots}_{=0} \right) \approx \frac{2}{Z_v} \cdot \frac{\Gamma}{2} = \mathbf{Y} \end{aligned} \tag{III.2.17}$$

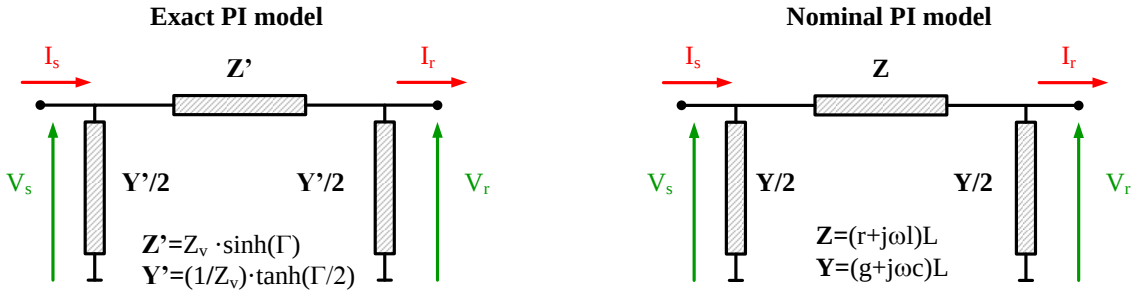


Figure III.2.7: Exact and nominal PI-model representation.

For steady-state modelling of lines and cables ABCD type modelling is often used. If fundamental frequencies are considered (i.e. 50/60 Hz), the ABCD parameters can take different expressions according to the lenght of the line. Thus, ABCD modelling for fundamental grid frequencies is usually classified into three groups [111]: (a) **short-lines ($<$ 80 km)**, (b) **medium lines (80-250 km)**, and (iii) **long-lines ($>$ 250 km)**. In short-lines the capacitive behaviour of the cable is usually neglected and the cable is modelled as a RL line (however the model for medium-length lines could also be adopted). In medium-length lines the cable is modelled as a π-section and it is assumed that the input is instantly obtained at the output. In long cables the travelling time of the wave is considered. Table III.2.1 summarizes the values of ABCD parameters for each of these cases. More information on these models can be found in [111].

Table III.2.1: Summary of ABCD parameters

Parameter	A=D	B	C
Units	per unit	Ω	S
Short line (<80 km)	1	$\mathbf{Z}$	0
Medium line, nominal π-circuit (80-250 km)	$1+\mathbf{YZ}/2$	$\mathbf{Z}$	$\mathbf{Y}\,(1+\mathbf{YZ}/4)$
Long line, equivalent π-circuit (>250 km)	$\cosh(\gamma L) = 1+\mathbf{Y'Z'}/2$	$Z_v \sinh(\gamma L) = \mathbf{Z'}$	$(1/Z_v)\sinh(\gamma L) = \mathbf{Y'}\,(1+\mathbf{Y'Z'}/4)$
Lossless line (r=g=0)	$\cos(\beta L)$	$jZ_v \sin(\beta L)$	$j(1/Z_v)\sin(\beta L)$

4.1.2. Transient modelling of cables

For transient modelling, different alternatives are possible [110]:

- **To use a chain of π-sections.**

  This is one of the most simple ways of modelling a cable for transient simulations. It consists of multiplying the ABCD matrices together:

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^N \begin{bmatrix} V_r \\ I_r \end{bmatrix} \tag{III.2.18}$$

  The frequency range in which this model is accurate depends on the number of chained π-sections. According to [110], a pretty good approximation to determine the proper number of sections is given by equation,

$$f_{max} = \frac{N \cdot v}{8 \cdot L} \tag{III.2.19}$$

  where N is the number of π-sections, v is the propagation speed of the wave, and L is the length of the cable. The advantage of this type of model is that intermediate voltage and current measures are available during simulations.

- **To use Bergeron's model.**

  Bergeron's model is a simple, constant frequency parameter method based on travelling wave theory, which is well described in [112]. Bergeron's model is roughly equivalent to using an infinite number of PI sections except that the resistance is lumped (i.e. 1/2 in the middle of the line and 1/4 at each end). In the EMTDC program, the line model separates the propagation into low and high frequency paths. This allows the transmission losses to be accurately represented at the fundamental frequency, and to have increased losses at higher frequencies. In Matlab/SimPowerSystems for example, the distributed line model is based on Bergeron's model.

  Bergeron's travelling wave model is deduced starting from the propagation equations presented in (III.2.6) but assuming a lossless line ($r = g = 0$). Then, following the

procedure described in [112] the distributed series resistances are included in the model.

The final model is illustrated in Fig.III.2.8, where:

$$i_{sr}(t) = \frac{1}{Z_v + R/4} v_s(t) + I'_s(t-\tau) \tag{III.2.20}$$

and,

$$\begin{aligned} I'_s(t-\tau) = &-\frac{Z_v}{Z_v + R/4}[v_r(t-\tau) + (Z_v - R/4) i_r s(t-\tau)] \\ &- \frac{R/4}{(Z_v + R/4)^2}[v_s(t-\tau) + (Z_v - R/4) i_s r(t-\tau)] \end{aligned} \tag{III.2.21}$$

In equations (III.2.20) and (III.2.21) I'_s and I'_r are the current History terms and $\tau = L/v = L\sqrt{lc}$ is the travelling time of the wave.

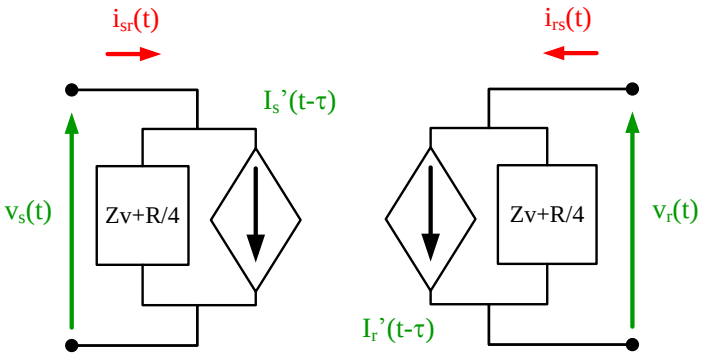


Figure III.2.8: Bergeron's transmission line model.

- **To use frequency-dependent models.**

  Frequency-dependent models are devoted for simulations that require a very high accuracy, but their complexity (and simulation time) is also much higher than series π-sections. Two main modelling trends are observed: (a) frequency-dependent models in the modal domain, and (b) frequency-dependent models in the phase-domain. Detailed information can be found in [112].

4.2. N π-sections cable model

In this PhD work, the chained π-section cable model has been selected. The reasons to select this model are: (i) the capacity modelling transient conditions, (ii) it its simplicity, and (iii) the accessibility to all the intermediate state variables.

Coming back to the studied case, the approximative speed of the travelling wave in the chosen cable is

$$v = \frac{1}{\sqrt{lc}} = 98 \cdot 10^6 \ m/s \tag{III.2.22}$$

According to equation (III.2.19), and as shown in Fig.III.2.9, if a three π-section cable is selected, frequencies of up to $f_{max} = 2450\ Hz$ can be accurately represented. This frequency range, that is around half the switching frequency of the converter, is considered to be sufficiently high for our studies.

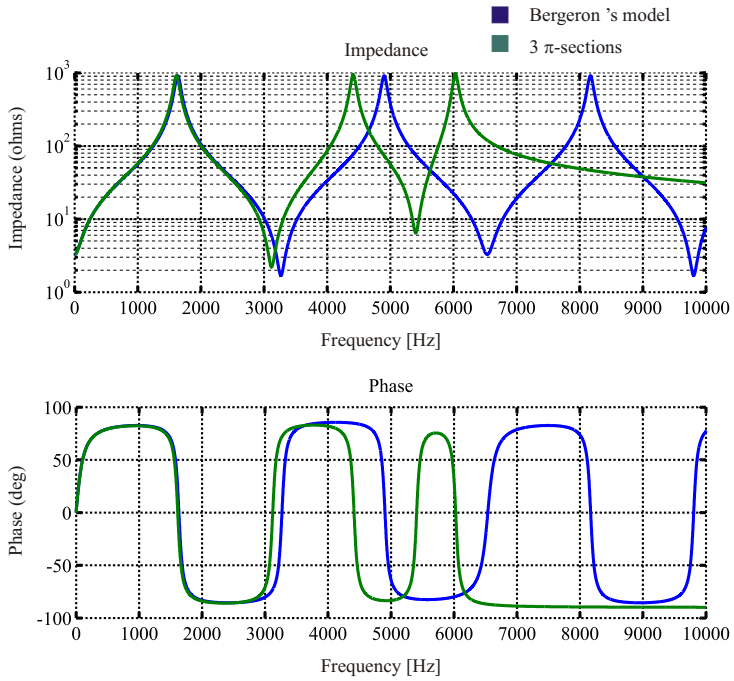


Figure III.2.9: Cable impedance modelled with (i) 3 π-sections, and (ii) Bergeron's distributed model

4.2.1. One cell modelling

The development of the full-cable model starts by modelling a single cable cell. The such defined cable cell does not exactly correspond to a π section, but rather to a Γ section, as illustrated in Fig.III.2.10.

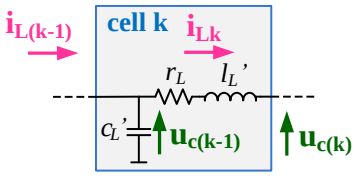


Figure III.2.10: Representation of one cell of the cable

Each of these cells can be represented by two sets of equations ($dq+$ coordinates):

$$\mathbf{f_{k(1)}}^{dq+} = \frac{d\mathbf{i_{Lk}}^{(dq+)}}{dt} = \mathbf{A_{L(dq+)}}\ \mathbf{i_{Lk}}^{(dq+)} + \mathbf{B_{L(dq+)}}\ \mathbf{u_{c(k-1)}}^{(dq+)} - \mathbf{B_{L(dq+)}}\ \mathbf{u_{ck}}^{(dq+)}$$
$$\mathbf{f_{k(2)}}^{dq+} = \frac{d\mathbf{u_{c(k-1)}}^{(dq+)}}{dt} = \mathbf{A}(\omega)_{\mathbf{(dq+)}}\ \mathbf{u_{c(k-1)}}^{(dq+)} + \mathbf{D_{L(dq+)}}\ \mathbf{i_{L(k-1)}}^{(dq+)} - \mathbf{D_{L(dq+)}}\ \mathbf{i_{Lk}}^{(dq+)} \tag{III.2.23}$$

Or, in unfolded form:

$$\frac{d}{dt}\begin{bmatrix} i_{Lk_{d+}} \\ i_{Lk_{q+}} \end{bmatrix} = \begin{bmatrix} -r_L/l'_L & \omega \\ -\omega & -r_L/l_L' \end{bmatrix}\begin{bmatrix} i_{Lk_{d+}} \\ i_{Lk_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_L & 0 \\ 0 & 1/l'_L \end{bmatrix}\begin{bmatrix} u_{c[k-1]_{d+}} \\ u_{c[k-1]_{q+}} \end{bmatrix} - \begin{bmatrix} 1/l'_L & 0 \\ 0 & 1/l'_L \end{bmatrix}\begin{bmatrix} u_{ck_{d+}} \\ u_{ck_{q+}} \end{bmatrix}$$
$$\frac{d}{dt}\begin{bmatrix} u_{c[k-1]_{d+}} \\ u_{c[k-1]_{q+}} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} u_{c[k-1]_{d+}} \\ u_{c[k-1]_{q+}} \end{bmatrix} + \begin{bmatrix} 1/c'_L & 0 \\ 0 & 1/c'_L \end{bmatrix}\begin{bmatrix} i_{L[k-1]_{d+}} \\ i_{L[k-1]_{q+}} \end{bmatrix} - \begin{bmatrix} 1/c'_L & 0 \\ 0 & 1/c'_L \end{bmatrix}\begin{bmatrix} i_{Lk_{d+}} \\ i_{Lk_{q+}} \end{bmatrix}$$

4.2.2. Cable modelling as a chain of cells

A cable is a chained structure composed of subsequent cells which can be expressed as,

$$\begin{aligned} d(\mathbf{i_{LN}})/dt &= \mathbf{f_{N(1)}} \\ d(\mathbf{u_{c(N-1)}})/dt &= \mathbf{f_{N(2)}} \\ &\vdots \\ d(\mathbf{i_{Lk}})/dt &= \mathbf{f_{k(1)}} \\ d(\mathbf{u_{c(k-1)}})/dt &= \mathbf{f_{k(2)}} \\ &\vdots \\ d(\mathbf{i_{L1}})/dt &= \mathbf{f_{1(1)}} \\ d(\mathbf{u_{c0}})/dt = \dot{\mathbf{v}}_{\mathbf{2}} &= \mathbf{f_{1(2)}} \end{aligned} \tag{III.2.25}$$

where N is the total number of sections.

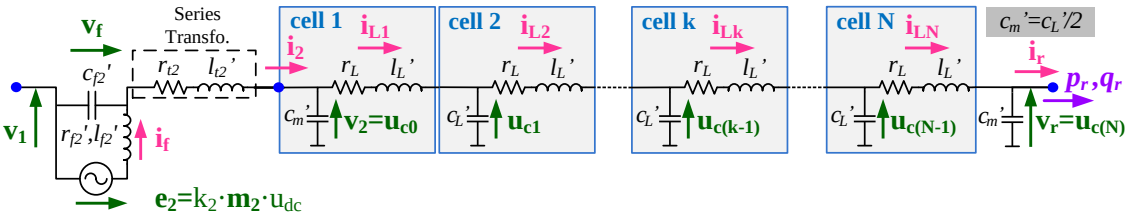


Figure III.2.11: Series injection side with N cell cable

This chained structure is depicted in Fig.III.2.11. It must be mentioned that the capacitor value used in the last expression, $\mathbf{f_{1(2)}}$, is $c_m{}'$ instead of $c_L{}'$, where $c_m{}' = c_L{}'/2$.

In the case of a $N = 3$ section cable, the structure of the cable presents the state model

equations of Fig.III.2.12. From this expression the following points are highlighted:

- When modelled as subsequent π-sections, the cable presents a linear structure, where current $\mathbf{i_2}$ acts as an input, and the voltage at the receiving-end, $\mathbf{v_r}$, acts as a perturbance.
- There are two states for each cable cell, which makes a total of $2N$ states. Thus, in the case of a 3 section cable 6 states will appear.
- Couplings with the term ω appear for every state.

It must be observed that some formulations are repetead, $\mathbf{v_2} = \mathbf{u_{c0}}$, $\mathbf{v_r} = \mathbf{u_{cN}}$, $\mathbf{i_2} = \mathbf{i_{L0}}$, $\mathbf{i_r} = \mathbf{i_{L[N+1]}}$.

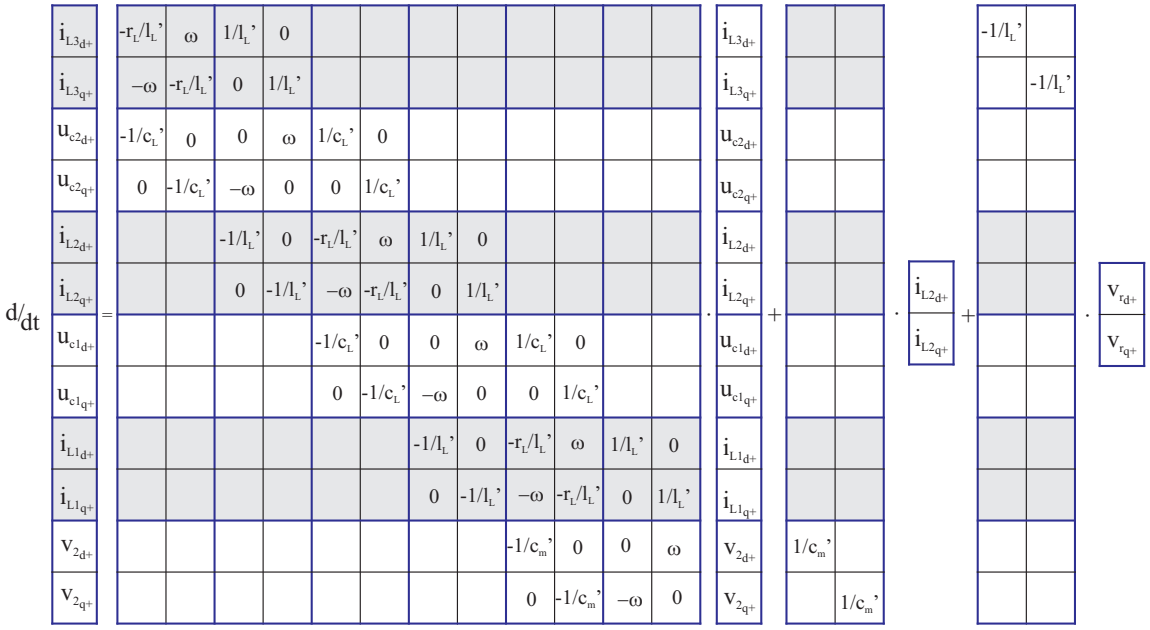


Figure III.2.12: State-Space equations of a three-cell cable

5. Modelling of the series filter

The series filter is basically a LC type filter (Fig.III.2.13), which resistance is inherent to the inductance.

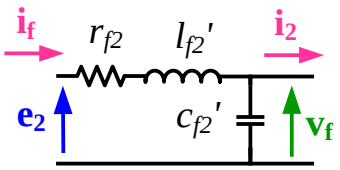


Figure III.2.13: One-line diagram of the series LC filter.

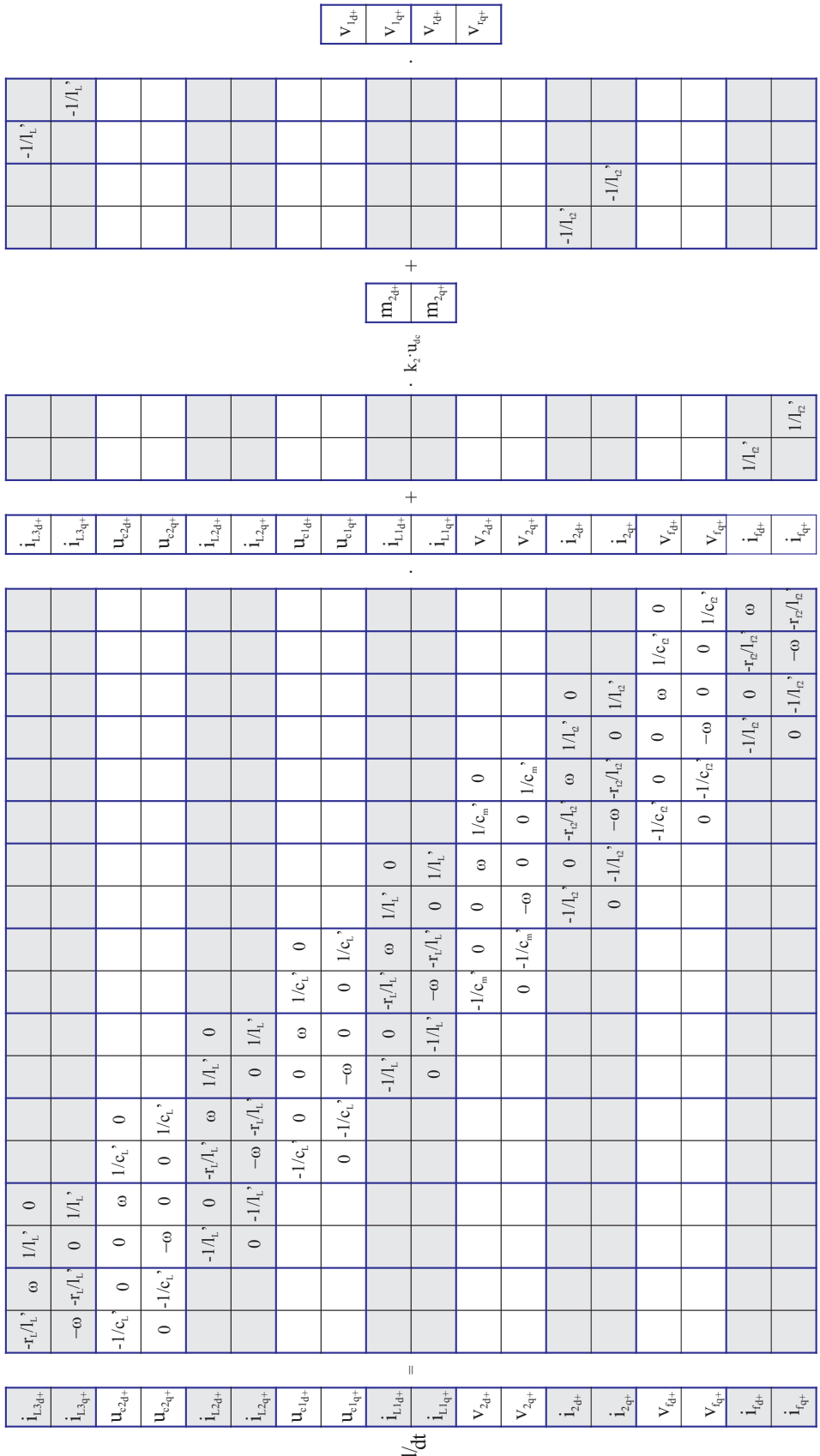


Figure III.2.14: State space equations of the series side with 3-cell cable.

The model of this filter in positive rotating frame, including the resistance of the inductance, yields

$$\begin{aligned}\frac{d\mathbf{v_f}^{(dq+)}}{dt} &= \mathbf{A}_\omega\ \mathbf{v_f}^{(dq+)} + \mathbf{D_{f2}}\ \mathbf{i_f}^{(dq+)} - \mathbf{D_{f2}}\ \mathbf{i_2}^{(dq+)} \\ \frac{d\mathbf{i_f}^{(dq+)}}{dt} &= \mathbf{A_{f2}}\ \mathbf{i_f}^{(dq+)} + \mathbf{B_{f2}}\ \mathbf{e_2}^{(dq+)} - \mathbf{B_{f2}}\ \mathbf{v_f}^{(dq+)}\end{aligned} \tag{III.2.26}$$

Or, in unfolded form:

$$\frac{d}{dt}\begin{bmatrix} v_{f_{d+}} \\ v_{f_{q+}} \end{bmatrix} = \begin{bmatrix} 0 & \omega \\ -\omega & 0 \end{bmatrix}\begin{bmatrix} v_{f_{d+}} \\ v_{f_{q+}} \end{bmatrix} + \begin{bmatrix} 1/c'_L & 0 \\ 0 & 1/c'_L \end{bmatrix}\begin{bmatrix} i_{f_{d+}} \\ i_{f_{q+}} \end{bmatrix} - \begin{bmatrix} 1/c'_{f2} & 0 \\ 0 & 1/c'_{f2} \end{bmatrix}\begin{bmatrix} i_{2_{d+}} \\ i_{2q+} \end{bmatrix}$$

$$\frac{d}{dt}\begin{bmatrix} i_{f2_{d+}} \\ i_{f2_{q+}} \end{bmatrix} = \begin{bmatrix} -r_{f2}/l'_{f2} & \omega \\ -\omega & -r_{f2}/{l_{f2}}' \end{bmatrix}\begin{bmatrix} i_{f2_{d+}} \\ i_{f2_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_{f2} & 0 \\ 0 & 1/l'_{f2} \end{bmatrix}\begin{bmatrix} e_{2_{d+}} \\ e_{2_{q+}} \end{bmatrix} - \begin{bmatrix} 1/l'_{f2} & 0 \\ 0 & 1/l'_{f2} \end{bmatrix}\begin{bmatrix} v_{f_{d+}} \\ v_{f_{q+}} \end{bmatrix}$$

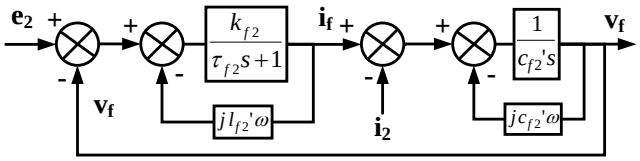


Figure III.2.15: Series LC filter model in the frequency domain.

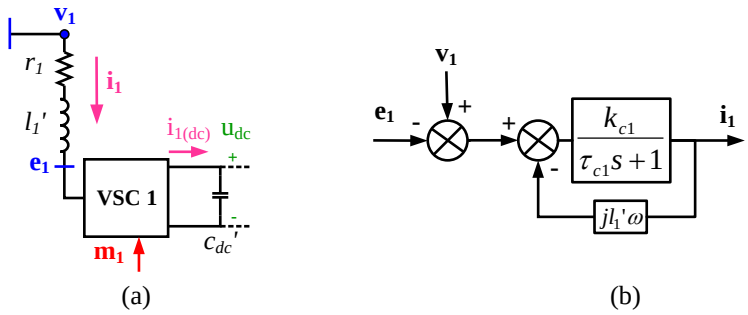


Figure III.2.16: (a) One-line diagram of the shunt-side, (b) Compact representation of the shunt-side model in the frequency domain.

The state-space representation of the complete series-side model using a three-cell cable is presented in Fig.III.2.14. Alternatively, the compact representation in Laplace domain of the series LC filter is illustrated in Fig.III.2.15, where $k_{f2} = 1/r_{f2}$ and $\tau_{f2} = l'_{f2}/r_{f2}$.

6. Modelling of the shunt-branch

For the modelling of the shunt-branch the transformer and filter impedances have been associate together yielding $r_1 = r_{t1} + r_{f1}$ and $l_1{}' = l_{t1}{}' + l_{f1}{}'$, as in Fig.III.2.16(a). The compact

representation of this model in the frequency domain can also be appreciated in Fig.III.2.16(b), where $k_{c1} = 1/r_{c1}$ and $\tau_{c1} = l'_{c1}/r_{c1}$.

The equations in the positive rotating frame are:

$$\frac{d\ \mathbf{i_1}^{(dq+)}}{dt} = \mathbf{A_{1(dq+)}} \cdot \mathbf{i_1}^{(dq+)} + \mathbf{B_1} \cdot \mathbf{v_1}^{(dq+)} - \mathbf{B_1} \cdot \mathbf{e_1}^{(dq+)}$$

$$\frac{d}{dt}\begin{bmatrix} i_{1_{d+}} \\ i_{1_{q+}} \end{bmatrix} = \begin{bmatrix} -r_1/l'_1 & \omega \\ -\omega & -r_1/{l_1}' \end{bmatrix} \begin{bmatrix} i_{1_{d+}} \\ i_{1_{q+}} \end{bmatrix} + \begin{bmatrix} 1/l'_1 & 0 \\ 0 & 1/l'_1 \end{bmatrix} \begin{bmatrix} v_{1_{d+}} \\ v_{1_{q+}} \end{bmatrix} - \begin{bmatrix} 1/l'_1 & 0 \\ 0 & 1/l'_1 \end{bmatrix} \begin{bmatrix} e_{1_{d+}} \\ e_{1_{q+}} \end{bmatrix} \tag{III.2.28}$$

7. Modelling of the converters

Voltage source converters are inherently discrete since their operation is based on switching power semiconductor devices. However, it is perfectly possible to model VSCs using approximated continuous-time models [113]. VSCs can therefore be modelled following exact (considering the switching instants of the valves) or continuous-time approaches. The next paragraphs will briefly describe the main features of these approaches:

7.1. Exact modelling approach of VSC

An exact linear time varying model of a VSC has been proposed in [113], for example. In this approach VSC is modelled as a linear network with a topology that changes depending on the state of six (ideal) switching devices. According to this modelling approach:

- the system is piecewise linear;
- switchings occur at predefined times given by the modulation strategy.

Consequently, over each interval during which the switches do not change their state, the circuit equations may be solved using standard linear techniques. Concatenating many such solutions permits the evolution of the state variables to be determined as a function of the switching times and the initial conditions of the circuit. To employ this solution technique, the system differential equations must be expressed in either *abc* or $\alpha\beta$ reference frame. *dq*-frame modelling does not lend itself to such an approach since the *dq*-frame equations are not piece-wise linear in nature.

Considering the VSC representation and name convention illustrated in Fig.III.2.17, phase voltages $E_{aN}(t)$, $E_{bN}(t)$, and $E_{cN}(t)$, are obtained in terms of switch-states:

$$\begin{bmatrix} E_{aN}(t) \\ E_{bN}(t) \\ E_{cN}(t) \end{bmatrix} = \begin{bmatrix} S_a(t) \\ S_b(t) \\ S_c(t) \end{bmatrix} \cdot \frac{U_{dc}(t)}{2} \tag{III.2.29}$$

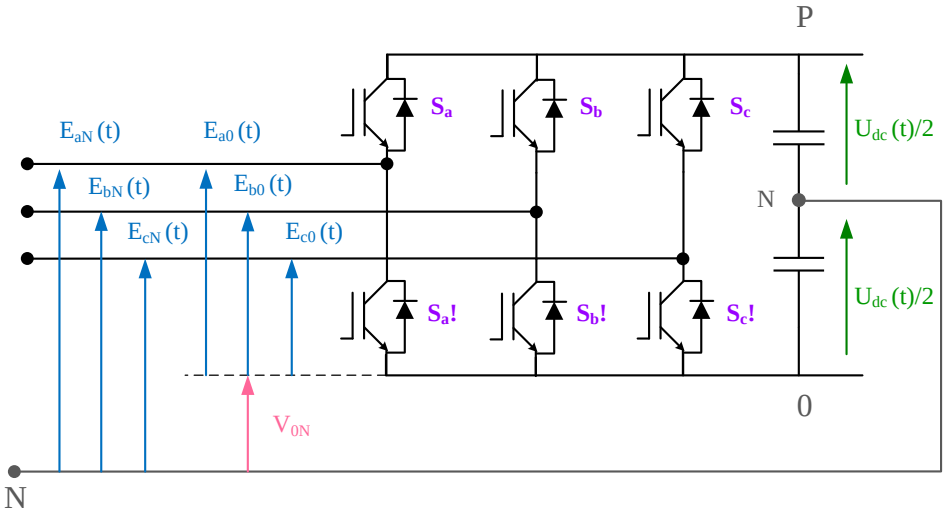


Figure III.2.17: Representation of a three-phase VSC

where $S_a(t)$, $S_b(t)$ and $S_c(t)$ represent the gating signals applied to the three upper switches. When the upper switch is conducting (either the IGBT or the free-wheeling diode) the gating signal is "1" and, when it is not, the gating signal worths "-1". The lower switch will adopt the complementary value of the upper signal.

Since the gating signals can get two values ("1" or "-1") and there are three switches, 8 possible switch combinations exist (2^3). The voltage values in the $\alpha\beta$-frame can be easily obtained by multiplying the *abc*-frame voltage vector by the Clarke (or Concordia transform).

$$\begin{bmatrix} E_\alpha(t) \\ E_\beta(t) \end{bmatrix} = k_c \cdot T_{cl} \cdot \begin{bmatrix} E_{aN}(t) \\ E_{bN}(t) \\ E_{cN}(t) \end{bmatrix} = k_c \cdot T_{cl} \cdot \begin{bmatrix} S_a(t) \\ S_b(t) \\ S_c(t) \end{bmatrix} \cdot \frac{U_{dc}(t)}{2} \tag{III.2.30}$$

where T_{cl} stands for Clarke's transform,

$$T_{cl} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{III.2.31}$$

and k_c can take two values. When $k_c = 1$, *Clarke*'s Transformation matrix (magnitude invariant) is used and when $k_c = \sqrt{3/2}$ *Concordia*'s Transformation (power invariant) matrix is used.

The resulting vector diagram in the $\alpha\beta$-plane is depicted in Fig.III.2.18. Fig.III.2.18(a) delineates the 8 possible voltage space-vectors (including the two zero-voltage vectors, {1,1,1} and {-1,-1,-1}) in the $\alpha\beta$ plane. By combining all the switching states appropriately, it is possible to generate any vector located within the hexagon of Fig.III.2.18(a). For instance, the vector $[v_\alpha, v_\beta]$=$(1/3) \cdot k_c \cdot U_{dc}$, 0 can be obtained by switching {-1,-1,-1} and {1,-1,-1} equally long

times.

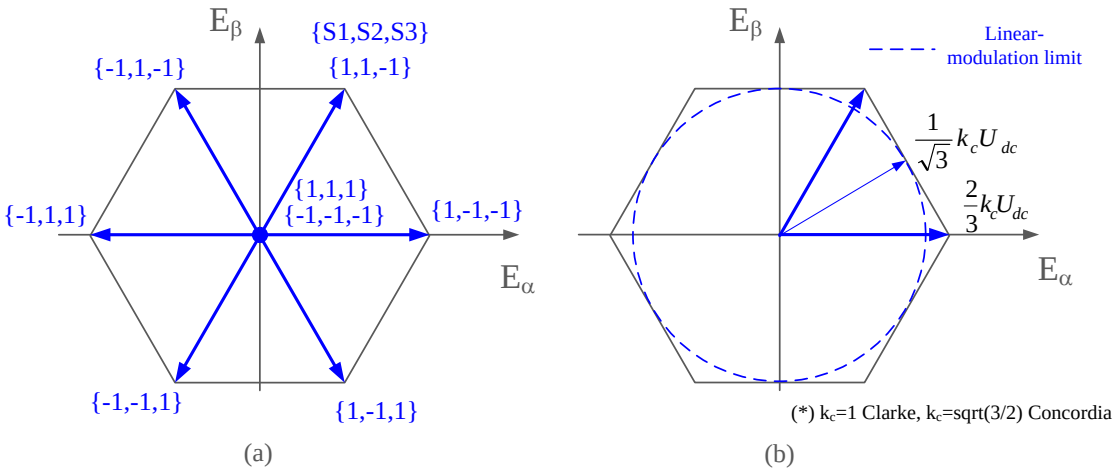


Figure III.2.18: Representation of the converter voltage space vectors

Fig.III.2.18(b) shows the maximum magnitude of the vectors located at the vertices of the hexagon. The function that calculates the activation sequence and the combination of the switches is called *modulation*. The blue-dotted circle is the limit of the *linear modulation* zone. Beyond the blue-dotted circle the *overmodulation-zone* is entered. As this results in distorted voltage waveforms, overmodulation should not be used in steady-state.

$$R_{\text{ linear region }}(radius) = \frac{\sqrt{3}}{2} \cdot ||\mathbf{e}_{max}|| = \frac{1}{\sqrt{3}} \cdot k_c \cdot U_{dc} \tag{III.2.32}$$

where

$$||\mathbf{e}_{max}|| = \frac{2}{3} \cdot k_c \cdot U_{dc} \tag{III.2.33}$$

In Fig.III.2.19, for instance, the sine-PWM modulation principle is illustrated. In this type of modulation the switching instants of the valves are calculated by comparing a voltage reference signal to a triangle or saw-tooth carrier wave. When the value of the reference signal is higher than the carrier signal, the valve is switched-on (S_i="1") and, when the value of the reference signal is below the carrier signal, the valve is switched-off (S_i="-1"). This operating mode yields a square-shaped output at the AC side of the converter.

7.2. Continuous-time modelling of VSC using time-averaging techniques

From Fig.III.2.19 it is easily found that the mean value of the square-shaped voltage during each carrier-period (T_s) is:

$$\{mean[E_{iN}]\}_j = \frac{1}{2}\left(\frac{\{E_i^{ref}\}_j}{v_{TRI-max}}\right) U_{dc} = \frac{1}{2}\{m_i\}_j U_{dc} \tag{III.2.34}$$

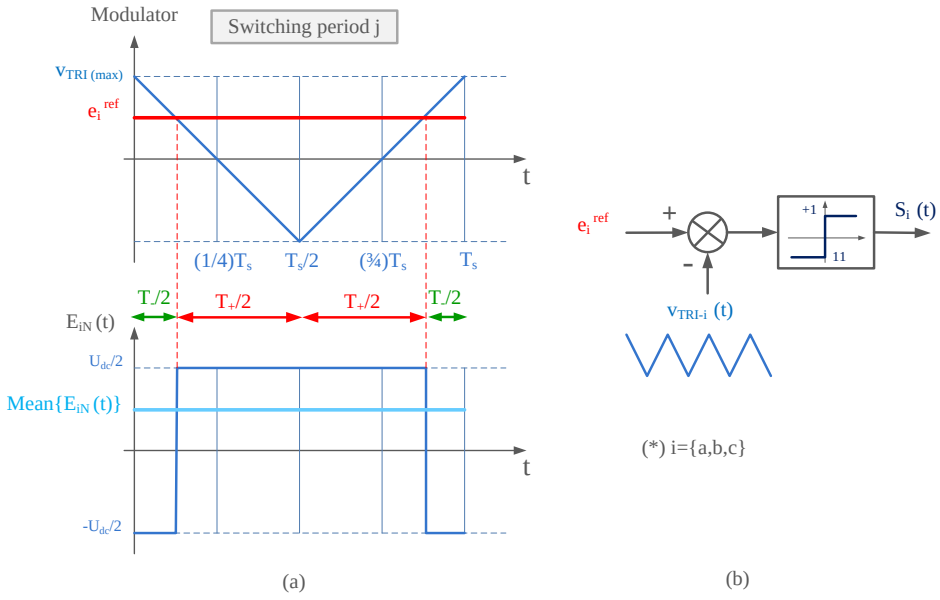


Figure III.2.19: Details of sin-PWM modulation.

where i stands for any of the three phases $i = a, b, c$, j represents the analysed carrier-period, and $\{m_i\}_j$ stands for the amplitude modulation index at the j carrier-period.

Considering that the frequency of the modulating signal (reference signal) is much lower than the frequency of the carrier signal, it is possible to assume that the reference signal is almost constant during each carrier period. In that case, equation (III.2.34) can be used to represent the average phase-voltage at each carrier-period.

As it can be observed in Fig.III.2.20, where the modulating signals has been depicted 15 times larger than the carrier period, the average values of the square-shaped phase-voltages (averaged over T_s) can be approximated to the fundamental of the square-shaped phase-voltage. Continuous-time modelling techniques use this approximation to model the VSC as:

$$E_{iN}(t) = \frac{1}{2} m_i(t) U_{dc} \tag{III.2.35}$$

where i stands for any of the three phases $i = a, b, c$.

It is worth mentioning that, when using equation (III.2.35), the switching harmonics are neglected. When a two-level three-phase converter as the one of Fig.III.1.15 is modulated with a sin-PWM modulation the output voltage of the converter ($e_{iN}(t) = e(t)$) is an squared waveform as the one depicted in Fig.III.2.20(b). If the frequency modulation index ($m_f = f_{sw}/f_1$) is high, and an FFT of the squared waveform is performed, the harmonic spectrum shown in Fig.III.2.21 is obtained. The harmonics in the converter output voltage waveform appear as sidebands centered around the switching frequency and its multiples, that is, around harmonics m_f, $2m_f$, $3m_f$ etc. This pattern holds true for all values of the modulation index, m, in the linear range ($0 \leq m \leq 1$) [114].

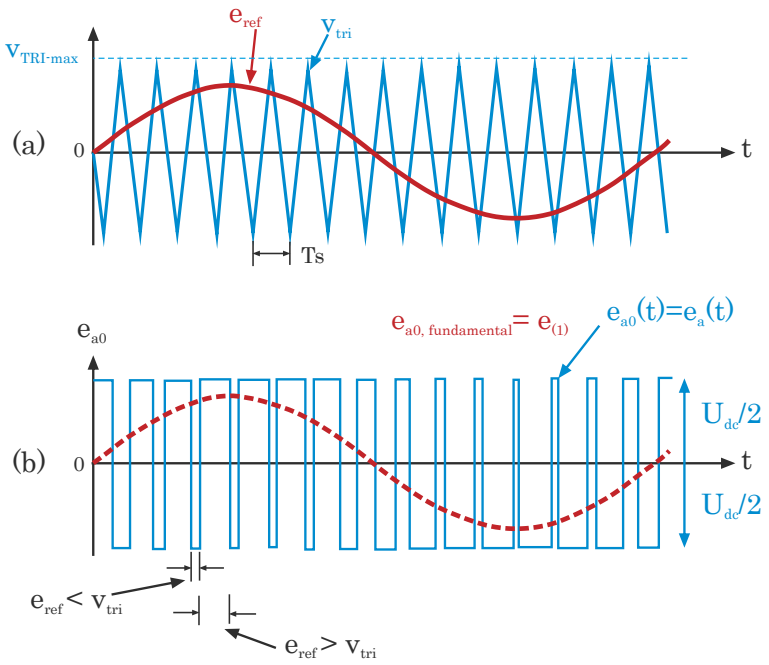


Figure III.2.20: Representation of the converter voltage space vectors.

Theoretically, the frequencies at which voltage harmonics occur can be indicated as

$$f_h = (q \cdot m_f \pm k) \cdot f_1 \tag{III.2.36}$$

where the fundamental frequency corresponds to $h = 1$. For odd values of q, harmonics exist only for even values of k and, for even values of q, harmonics exist only for odd values of k. If m_f is chosen to be an odd integer, even harmonics dissapear from the output voltage waveform of the converter. Furthermore, if m_f is selected to be a multiple of 3, triplen harmonics will dissapear from line-to-line output voltages.

Hence, the choice of the switching frequency is a trade-off between two factors:

i) The higher the switching frequency is, the higher the switching harmonics orders are. Higher order harmonics are easier to filter with low-pass filters.

ii) The shortcoming of a high switching frequency is that the switching losses of the converter increase with higher switching frequencies.

It is also worth mentioning that the standard sin-PWM modulation method is not the most efficient in terms of U_{dc} voltage use, as it can be observed in Fig.III.2.22. The attainable voltage radius when sin-PWM modulation is used is $R_{sin-PWM} = 0.5 \cdot k_c \cdot U_{dc}$. However, if SVM-PWM modulation is used, or a third-harmonic is added to sin-PWM it is possible to increase the modulation zone to $R_{SVM-PWM} = (1/\sqrt{3}) \cdot k_c \cdot U_{dc}$, which is larger in a 1.15 ratio.

Continuous-time representations are typically used for the development of converter control

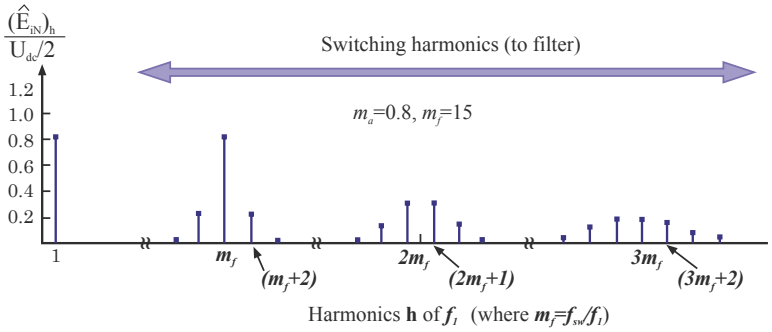


Figure III.2.21: PWM signals, from [114]

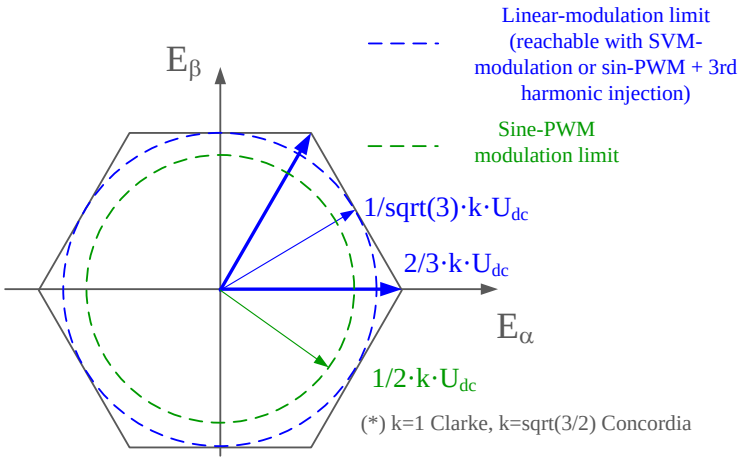


Figure III.2.22: Reachable zones with different modulation strategies.

strategies and they yield an elegant set of three differential equations that represent the VSC operation with reasonable accuracy under most conditions. There are, however, several limitations to this modelling approach, that is not able to [113]:

1) represent the inherent discrete nature of VSC switchings, limiting the closed loop performance of the VSC;

2) account for the effect that harmonics have on the steady-state fundamental frequency behaviour of the VSC;

3) model resonances, occurring between the AC and DC sides of the VSC, as well as those betwqeen the AC system and the VSC controls;

4) calculate AC and DC side harmonic injections generated by the converter switchings.

7.3. Continuous-time modelling of VSC: the modelling approach followed in this PhD

Since the continuous-time modelling approach is a priori sufficient for the design of the control loops, in this PhD this approach has been selected. In full-parameter values the relationship

between the AC and DC-side of the converters, as previously explained, is

$$\mathbf{E} = \frac{1}{2} \cdot \mathbf{m} \cdot U_{dc} \tag{III.2.37}$$

where $\mathbf{E}$ is the voltage vector at the AC-side of the converter (peak, single-phase value), $\mathbf{m}$ is the modulation index vector, and U_{dc} is the DC-link voltage. In this equation an scalar PWM modulation (sin-PWM) has been assumed. But, if a SVM-PWM modulation is desired, the term $1/2$ needs to be replaced by the term $1/\sqrt{3}$. Moreover, the time-dependency term has been omitted for simplicity.

The translation to per-unit values yields,

$$\begin{aligned} \frac{\mathbf{E}}{V_b} &= \frac{1}{2} \cdot \mathbf{m} \cdot \frac{U_{dc}}{V_b} = \frac{1}{2} \cdot \frac{U_{b(dc)}}{V_b} \cdot \mathbf{m} \cdot \frac{U_{dc}}{U_{b(dc)}} \\ \mathbf{e} &= k \cdot \mathbf{m} \cdot u_{dc} \end{aligned} \tag{III.2.38}$$

where $k = 0.5 \cdot U_{b(dc)}/V_b$. For the shunt converter, $k_1 = 0.5 \cdot U_{b(dc)}/V_{bII}$ and, for the series converter $k_2 = 0.5 \cdot U_{b(dc)}/V_{bIII}$. Subscript **1** stands for the shunt-side converter and subscript **2** stands for the series-side converter.

$$\mathbf{e_1} = k_1 \cdot \mathbf{m_1} \cdot u_{dc} \tag{III.2.39}$$

$$\mathbf{e_2} = k_1 \cdot \mathbf{m_2} \cdot u_{dc} \tag{III.2.40}$$

Sometimes, it is interesting to model the delay-time associtated to the switching period (T_{sw}), the control ($\tau_{ctr-delay}$), the measurements ($\tau_{meas-delay}$), and delays of statistical nature ($\tau_{stat-delay}$). These delays can be modeled as a first-order equation as,

$$\begin{aligned} \frac{d\ \mathbf{m}^{(dq+)}}{dt} &= -\frac{1}{\tau_{conv}}\mathbf{m}^{(\mathbf{dq+})} + \frac{1}{\tau_{conv}}\mathbf{m}'^{\ (\mathbf{dq+})} \\ \frac{d}{dt}\begin{bmatrix} m_{d+} \\ m_{q+} \end{bmatrix} &= \begin{bmatrix} -1/\tau_{conv} & 0 \\ 0 & -1/\tau_{conv} \end{bmatrix} \begin{bmatrix} m_{d+} \\ m_{q+} \end{bmatrix} + \begin{bmatrix} 1/\tau_{conv} & 0 \\ 0 & 1/\tau_{conv} \end{bmatrix} \begin{bmatrix} m'_{d+} \\ m'_{q+} \end{bmatrix} \end{aligned} \tag{III.2.41}$$

where the value of τ_{conv} is $\tau_{conv} = T_{sw}/2 + \tau_{ctr-delay} + \tau_{meas-delay} + \tau_{stat-delay}$. Fig.III.2.23 models these delays in the frequency domain.

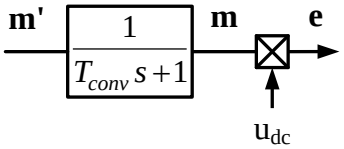


Figure III.2.23: Compact representation of the converter and the modeled delay in the frequency domain

8. Modelling of the DC-link

The modelling of the DC-link starts by describing the current equations at the DC-link:

$$i_{1(dc)} - i_{2(dc)} = c'_{dc}\frac{du_{dc}}{dt} + \frac{1}{r_{dc}}u_{dc} \tag{III.2.42}$$

Multiplying both sides of equation (III.2.42) by the DC-link voltage u_{dc}, active powers coming in and out of the DC-link are obtained:

$$p_{1(dc)} - p_{2(dc)} = u_{dc}i_{1(dc)} - u_{dc}i_{2(dc)} = c'_{dc}u_{dc}\frac{du_{dc}}{dt} + \frac{1}{r_{dc}}u_{dc}^2 \tag{III.2.43}$$

Another way of writing (III.2.43) is to define a new variable $z = {u_{dc}}^2$, that yields a linear-shaped equation. Unfortunately, if the equation is further developped, it is observed that the powers depend on voltages and currents and thus, the equation is not trully linear.

$$p_{1(dc)} - p_{2(dc)} = u_{dc}i_{1(dc)} - u_{dc}i_{2(dc)} = \frac{c'_{dc}}{2}\frac{dz}{dt} + \frac{1}{r_{dc}}z \tag{III.2.44}$$

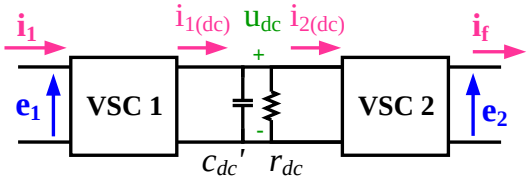


Figure III.2.24: One-line diagram of the DC-link model

Equations (III.2.43) and (III.2.44) provide the relationship between the DC-side parameters of the DC-link. However, for control purposes, it is more interesting to adapt this expression in order to associate AC-side parameters with DC-side parameters. This connection is made by assuming that converters are lossless (losses are modelled separately by means of r_{dc}) and thus, $p_{1(dc)} = p_{1e}$, and $p_{2(dc)} = p_{2e}$. It must be reminded that these equivalences are in per-unit:

$$\begin{aligned} \frac{P_{1e}(3ph)}{3 \cdot S_{bII(1ph)}} = \frac{3 \cdot P_{1e}(1ph)}{3 \cdot S_{bII(1ph)}} = \frac{P_{1(dc)}}{S_{b(dc)}} \quad &\Rightarrow \quad p_{1e} = p_{1(dc)} \\ \frac{P_{2e}(3ph)}{3 \cdot S_{bIII(1ph)}} = \frac{3 \cdot P_{2e}(1ph)}{3 \cdot S_{bIII(1ph)}} = \frac{P_{2(dc)}}{S_{b(dc)}} \quad &\Rightarrow \quad p_{2e} = p_{2(dc)} \end{aligned} \tag{III.2.45}$$

This assumption allows reformulating equation (III.2.44) as

$$p_{1e} - p_{2e} = p_{1(dc)} - p_{2(dc)} = \frac{c'_{dc}}{2}\frac{dz}{dt} + \frac{1}{r_{dc}}z \tag{III.2.46}$$

Therefore, the only thing left to do is to define the expressions of p_{1e} and p_{2e}. According to (B.50), and ignoring homopolar components, these terms can be expressed in a generic form as:

$$\begin{aligned} p_{1e} &= \Re\{\mathbf{s_{1e}}(t)\} = \Re\left\{\mathbf{e_1}(t)\mathbf{i_1}(t)^*\right\} = \\ &= \Re\left\{\left[\sum_{h=1}^{\infty} \mathbf{e_{1_{(h+)}}} e^{jh\omega_1 t} + \mathbf{e_{1_{(h-)}}} e^{-jh\omega_1 t}\right]\left[\sum_{k=1}^{\infty} \mathbf{i_{1_{(k+)}}} e^{jk\omega_1 t} + \mathbf{i_{1_{(k-)}}} e^{-jk\omega_1 t}\right]^*\right\} \\ p_{2e} &= \Re\{\mathbf{s_{2e}}(t)\} = \Re\left\{\mathbf{e_2}(t)\mathbf{i_2}(t)^*\right\} = \\ &= \Re\left\{\left[\sum_{h=1}^{\infty} \mathbf{e_{2_{(h+)}}} e^{jh\omega_1 t} + \mathbf{e_{2_{(h-)}}} e^{-jh\omega_1 t}\right]\left[\sum_{k=1}^{\infty} \mathbf{i_{2_{(k+)}}} e^{jk\omega_1 t} + \mathbf{i_{2_{(k-)}}} e^{-jk\omega_1 t}\right]^*\right\} \end{aligned} \tag{III.2.47}$$

8.1. DC-link model when only the positive fundamental sequence is present

Considering an ideal case where only the positive fundamental sequence is present, from (B.58), the DC-link can be modelled as,

$$\begin{aligned} p_{1e}(t) - p_{2e}(t) &= [e_{1d_{(1+)}} i_{1d_{(1+)}} + e_{1q_{(1+)}} i_{1q_{(1+)}}] - [e_{2d_{(1+)}} i_{2d_{(1+)}} + e_{2q_{(1+)}} i_{2q_{(1+)}}] = \\ &= \frac{c'_{dc}}{2}\frac{d\ {u_{dc}}^2}{dt} + \frac{1}{r_{dc}}{u_{dc}}^2 \end{aligned} \tag{III.2.48}$$

Equation (III.2.48) can be further detailed by specifying the voltage at the AC side in terms of modulation index and DC-voltage $\mathbf{e} = k \cdot \mathbf{m} \cdot u_{dc}$. In this way,

$$\begin{aligned} p_{1e}(t) - p_{2e}(t) &= k_1 \cdot u_{dc} \cdot [m_{1d_{(1+)}} i_{1d_{(1+)}} + m_{1q_{(1+)}} i_{1q_{(1+)}}] \\ &\quad - k_2 \cdot u_{dc} \cdot [m_{2d_{(1+)}} i_{2d_{(1+)}} + m_{2q_{(1+)}} i_{2q_{(1+)}}] = \\ &= c'_{dc} u_{dc} \frac{d\ u_{dc}}{dt} + \frac{1}{R_{dc}}{u_{dc}}^2 \end{aligned} \tag{III.2.49}$$

Finally,

$$\begin{aligned} \frac{d\ u_{dc}}{dt} &= -\frac{1}{c'_{dc}}\frac{1}{r_{dc}c'_{dc}} u_{dc} \\ &\quad + \frac{k_1}{c'_{dc}}[m_{1d_{(1+)}} i_{1d_{(1+)}} + m_{1q_{(1+)}} i_{1q_{(1+)}}] \\ &\quad - \frac{k_2}{c'_{dc}}[m_{2d_{(1+)}} i_{2d_{(1+)}} + m_{2q_{(1+)}} i_{2q_{(1+)}}] \end{aligned} \tag{III.2.50}$$

8.2. DC-link model when the positive and negative fundamental sequences are present

Considering that also the negative fundamental sequence is present, converter powers become,

$$\begin{aligned} p_{1e}(t) &= \bar{p}_{1e} + p_{1e_{(c2)}}\cos(2\omega_1 t) + p_{1e_{(s2)}}\sin(2\omega_1 t) \\ p_{2e}(t) &= \bar{p}_{2e} + p_{2e_{(c2)}}\cos(2\omega_1 t) + p_{2e_{(s2)}}\sin(2\omega_1 t) \end{aligned} \tag{III.2.51}$$

where

$$\begin{aligned} \bar{p}_{1e} &= e_{1d_{(1+)}}i_{1d_{(1+)}} + e_{1q_{(1+)}}i_{1q_{(1+)}} + e_{1d_{(1-)}}i_{1d_{(1-)}} + e_{1q_{(1-)}}i_{1q_{(1-)}} \\ \bar{p}_{2e} &= e_{2d_{(1+)}}i_{2d_{(1+)}} + e_{2q_{(1+)}}i_{2q_{(1+)}} + e_{2d_{(1-)}}i_{2d_{(1-)}} + e_{2q_{(1-)}}i_{2q_{(1-)}} \\ p_{1e_{(c2)}} &= e_{1d_{(1-)}}i_{1d_{(1+)}} + e_{1q_{(1-)}}i_{1q_{(1+)}} + e_{1d_{(1+)}}i_{1d_{(1-)}} + e_{1q_{(1+)}}i_{1q_{(1-)}} \\ p_{2e_{(c2)}} &= e_{2d_{(1-)}}i_{2d_{(1+)}} + e_{2q_{(1-)}}i_{2q_{(1+)}} + e_{2d_{(1+)}}i_{2d_{(1-)}} + e_{2q_{(1+)}}i_{2q_{(1-)}} \\ p_{1e_{(s2)}} &= e_{1q_{(1-)}}i_{1d_{(1+)}} - e_{1d_{(1-)}}i_{1q_{(1+)}} - e_{1q_{(1+)}}i_{1d_{(1-)}} + e_{1d_{(1+)}}i_{1q_{(1-)}} \\ p_{2e_{(s2)}} &= e_{2q_{(1-)}}i_{2d_{(1+)}} - e_{2d_{(2-)}}i_{2q_{(1+)}} - e_{2q_{(1+)}}i_{2d_{(1-)}} + e_{2d_{(1+)}}i_{2q_{(1-)}} \end{aligned} \tag{III.2.52}$$

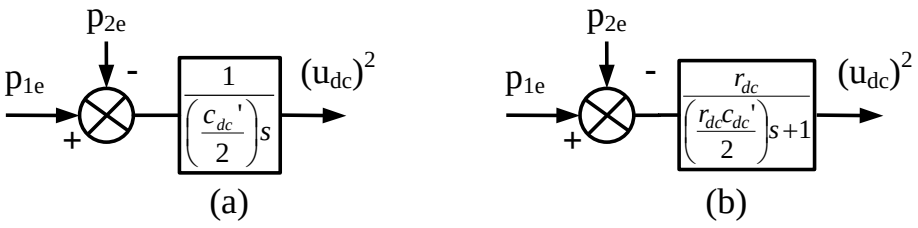


Figure III.2.25: Compact representation of the DC-link in the frequency domain

Once the expressions of $p_{1e}(t)$ and $p_{2e}(t)$ are known, it is possible to deduce $\dot{u}_{dc}$ for unbalanced conditions in the same way as it has been done for balanced conditions. Equation (III.2.51) explains the oscillations at double the fundamental frequency that the DC-link voltage suffers under unbalance voltages and currents.

Fig.III.2.25 shows two possible representations of the DC-link model (yielding ${u_{dc}}^2$) in the frequency domain. The first one, Fig.III.2.25(a), does not take into consideration the losses in the converters. The second one, Fig.III.2.25(b), does.

Chapter III.3

Positive SRF-oriented control of a UPLC connected to a RL line

When working with multi-phase signals, the selection of a working frame (natural, static or rotating) is directly linked with the used control approach. Among the possible working-frames the positive synchronous reference frame (SRF) is the most popular working frame among the UPFC research community. The main reason of this success is probably that it transforms alternating signals into constant signals and thus, PI-type controllers, which are familiar for electric power engineers, can be used. Following the same trend observed in the literature, in this chapter, also a positive SRF has been chosen. The innovative point of this work, however, is that, inversely to the approaches already evaluated in the bibliography [20, 21, 22, 23, 24, 25, 26, 27, 28], this control approach does not use PI controllers. It uses a control structure that is composed of a global trajectory generation control and local Lyapunov-based controllers.

As depicted in Fig.III.3.1, the control of the UPLC can be divided in two main sub-control structures: the series-side control and the shunt-side control. The series-side control is in charge of the main function of the UPLC, power-flow control, while the shunt-side control provides an essential support function: DC-link voltage control.

- On account of the concatenated structure of the series-side model, which becomes even longuer when a cable is considered, a Backstepping-type philosophy is proposed for the series-side control. Backstepping is a recursive control design procedure that is very well adapted for chained structures. It breaks the design problem of the full system into a sequence of lower order design problems [115, 116]. Thus, each subsystem is associated to a virtual control law. The most common approach is to associate the Backstepping method to Lyapunov design techniques, but any other feedback control types can also be used. In this work, two approaches have been tested in the local controllers: (i) to use Lyapunov-based controllers, and (ii) to use PI-type controllers. The first option can be used at any working-frames while the second option can only be used with SRFs.
- The shunt-side control concept is based on a time-based decoupling between the shunt-current and the DC-voltage dynamics, where the DC-voltage control loop provides the active power reference to the shunt-current control loop.

The main objective of the chapter is to present, describe and analyse the control approach of a UPLC that is connected to a lumped RL line. This first chapter will establish the basis

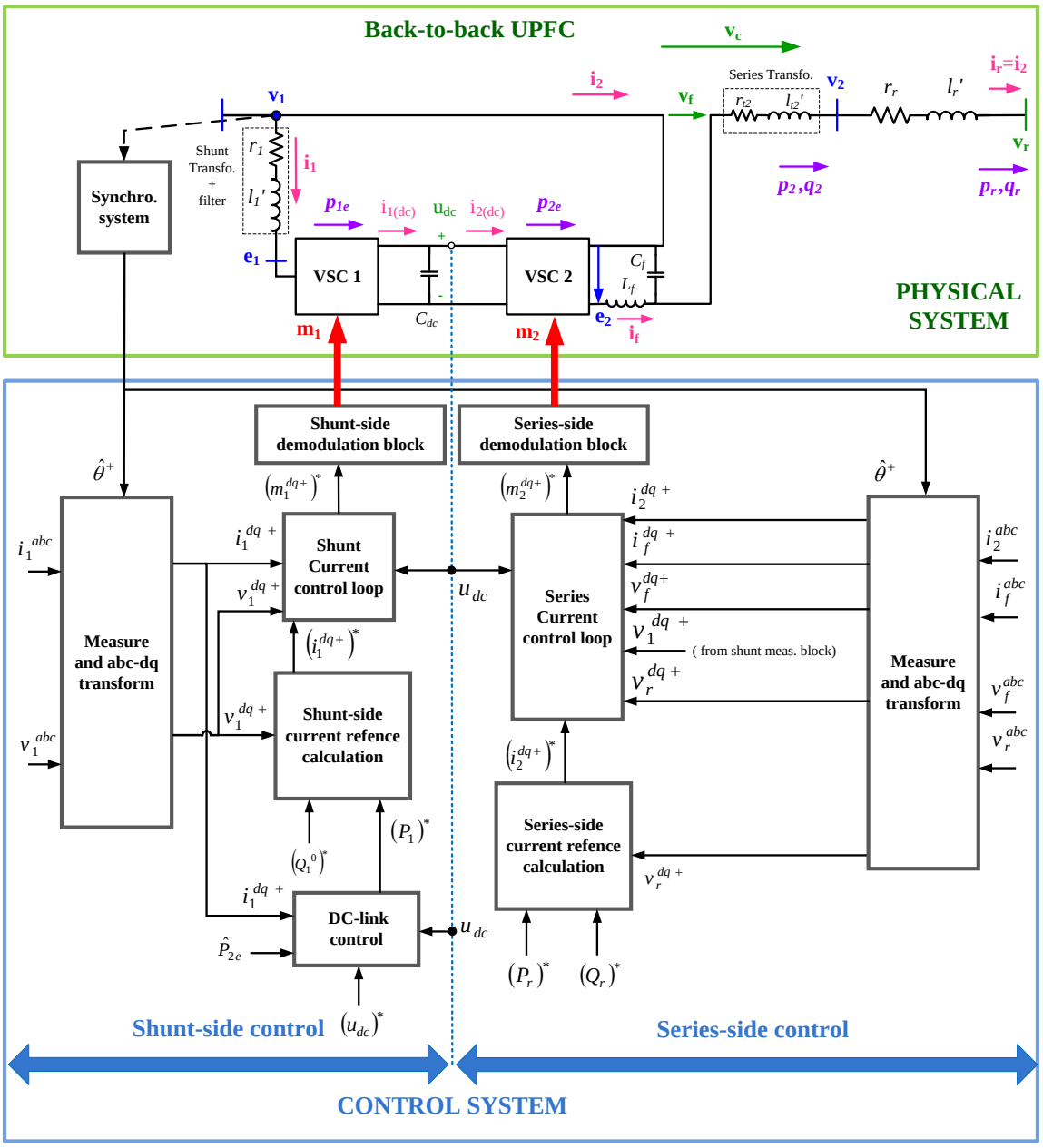


Figure III.3.1: Control structure of the positive SRF-oriented control of a UPLC connected to a RL line

for subsequent chapters where the addition of a cable and the performance under unbalanced conditions are discussed. The efficiency of the proposed control is tested by simulations in the *SimPowerSystem* toolbox of Matlab. These simulations will evidence the main advantages and shortcomings of the proposed control method and the selected working frame.

In the following sections, the analysis of the model structure, the reference selection, the series-side control, the shunt-side control, and the simulation results are described and discussed.

1. Analysis of the UPLC model structure and reference choice

The model of the UPLC can be represented by the following compact expression

$$\dot{\mathbf{x}} = \mathbf{A}(\omega)\mathbf{x} + g(\mathbf{x}, \mathbf{u}) + \mathbf{D}\ \mathbf{d} \tag{III.3.1}$$

where $\mathbf{x}$ is the state-vector, $\mathbf{x} = [i_{2d}, i_{2q}, v_{fd}, v_{fq}, i_{fd}, i_{fq}, i_{1d}, i_{1q}, u_{dc}]^t$, $\mathbf{u}$ is the input vector, $\mathbf{u} = [m_{2d}, m_{2q}, m_{1d}, m_{1q}]^t$, $\mathbf{d}$ denotes the perturbation vector, $\mathbf{d} = [v_{1d}, v_{1q}, v_{rd}, v_{rq}]^t$, $\mathbf{A}(\omega)$ is the state matrix, ω indicates the angular frequency of the rotating frame, and $\mathbf{D}$ is the perturbation matrix. For simplicity, in the following lines the positive fundamental rotating frame is represented by dq labels (instead of $dq(1+)$).

The model of the UPLC presents a multivariable structure with nonlinear relationships between the state-variables and the input-variables. At a first glance, this system, which contains 9 state variables, 4 inputs, and 4 perturbations, may result complex. However, it is possible to deal with it if the system is divided in smaller subsystems, as shown in Fig.III.3.2, and as expressed in the next equations:

$$\text{Series subsystem} \Longrightarrow \left\{ \dot{\mathbf{x}}_{\mathbf{se}} = \mathbf{A}_{\mathbf{se}}\ \mathbf{x}_{\mathbf{se}} + k_2 \cdot x_{sh(2)} \cdot \mathbf{u}_{\mathbf{se}} + \mathbf{D}_{\mathbf{se}}\ \mathbf{d}_{\mathbf{se}} \right. \tag{III.3.2}$$

$$\text{Shunt subsystem} \Longrightarrow \begin{cases} \dot{\mathbf{x}}_{\mathbf{sh(1)}} & = \mathbf{A}_{\mathbf{sh}}\ \mathbf{x}_{\mathbf{sh(1)}} + k_1 \cdot x_{sh(2)} \cdot \mathbf{u}_{\mathbf{sh}} + \mathbf{D}_{\mathbf{sh}}\ \mathbf{d}_{\mathbf{sh}} \\ \dot{x}_{sh(2)} & = \dfrac{k_1}{c'_{dc}}\ \mathbf{u}_{\mathbf{sh}}{}^{\mathbf{t}} \cdot \mathbf{x}_{\mathbf{sh(1)}} - \dfrac{k_2}{c'_{dc}}\ \mathbf{u}_{\mathbf{se}}{}^{\mathbf{t}} \cdot \mathbf{x}_{\mathbf{se(5:6)}} \end{cases} \tag{III.3.3}$$

where $\mathbf{x}_{\mathbf{se}} = [i_{2d}, i_{2q}, v_{fd}, v_{fq}, i_{fd}, i_{fq}]^t$, is the series-side state-vector, $\mathbf{u}_{\mathbf{se}} = [m_{2d}, m_{2q}]^t$ is the series-side input vector, $\mathbf{d}_{\mathbf{se}} = [v_{1d}, v_{1q}, v_{rd}, v_{rq}]^t$ is the series-side perturbation vector, $\mathbf{x}_{\mathbf{sh}} = [\mathbf{x}_{\mathbf{sh(1)}}\ x_{sh(2)}]^t$, is the shunt-side state vector, $\mathbf{u}_{\mathbf{sh}} = [m_{1d}, m_{1q}]^t$ is the shunt-side input vector, and $\mathbf{d}_{\mathbf{sh}} = [v_{1d}, v_{1q}]^t$ are the shunt-side perturbations. Additionally, the shunt state-vector is further divided into $\mathbf{x}_{\mathbf{sh(1)}} = [i_{1d}, i_{1q}]^t$, and $x_{sh(2)} = u_{dc}$.

Equations (III.3.2) and (III.3.3) show that the dynamics of $\mathbf{x}_{\mathbf{se}}$ and $\mathbf{x}_{\mathbf{sh(1)}}$ depend on $x_{sh(2)}$, and that the dynamics of $x_{sh(2)}$ depend on $\mathbf{x}_{\mathbf{sh(1)}}$, $\mathbf{x}_{\mathbf{se(5:6)}}$, $\mathbf{u}_{\mathbf{sh}}$, and $\mathbf{u}_{\mathbf{se}}$. A simple way of dealing with these cross-coupled terms is to control the DC-link voltage, $x_{sh(2)}$, very slowly comparing to $\mathbf{x}_{\mathbf{se}}$ and $\mathbf{x}_{\mathbf{sh(1)}}$. In this way, the $\mathbf{x}_{\mathbf{se}}$ and $\mathbf{x}_{\mathbf{sh(1)}}$ control loops can consider u_{dc} as a constant variable. Considering different time-scales allows decoupling the system into fast and slow modes.

The following sections describe the proposed series and shunt control strategies comprehensively. But, before going further, it is necessary to select which objectives are to be controlled. In the next section the selection of the controlled objectives is discussed.

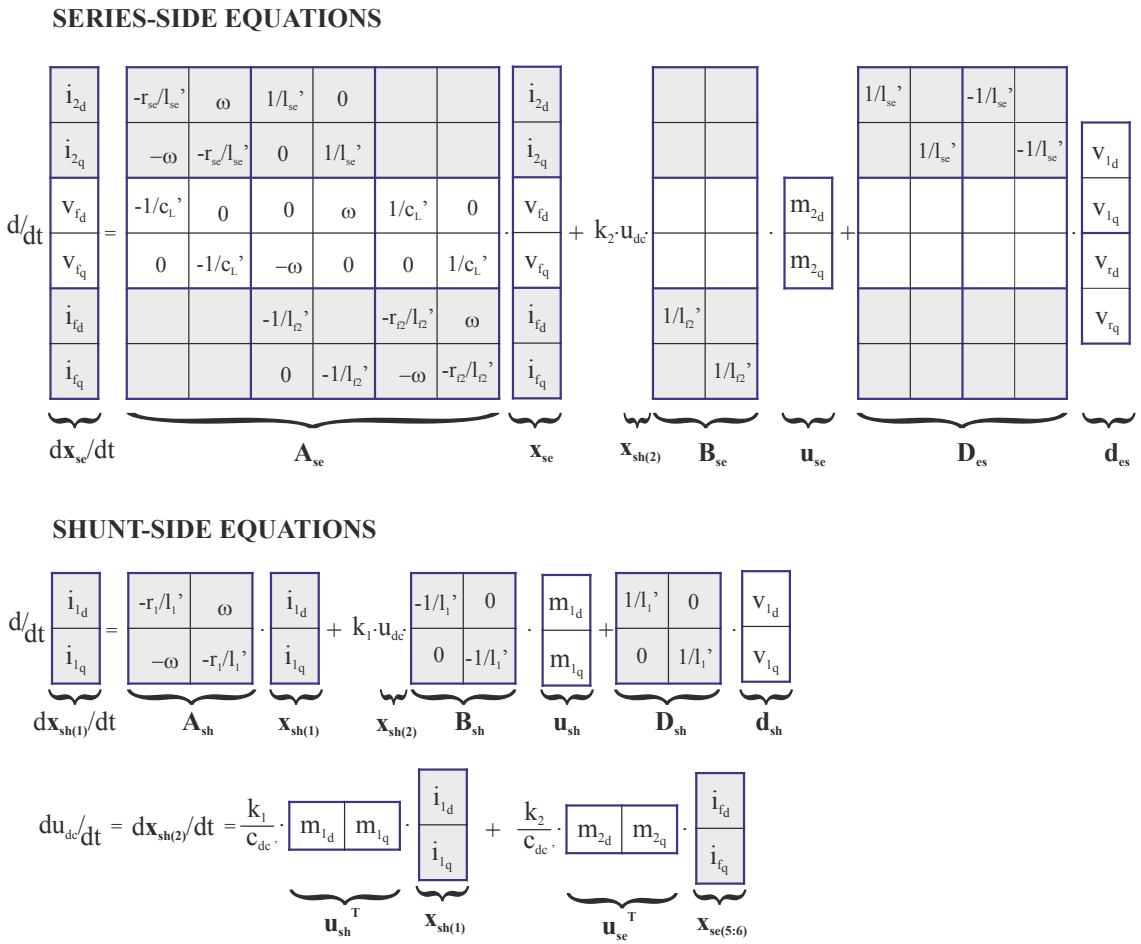


Figure III.3.2: Series- and shunt-side model equations

2. Selection of controlled objectives

The model equations given by (III.3.1) present four control inputs (m_{2d}, m_{2q}, m_{1d}, m_{1q}) that correspond to the modulation signals of the series and shunt converters in the d and q axis. This makes a total of four controllable objectives. But, which should be the controlled objectives? Since each of the converters can control two objectives, two controlled objectives correspond to the series-side, and two controlled objectives correspond to the shunt-side.

In Fig.III.3.3 the possible controllable objectives have been highlighted in yellow. The main function of the UPLC, which is the power-flow control, is performed by the series-side. In this regard, two options are possible:

a) **To control the active and reactive powers, p_r and q_r, at the receiving-end.**

This option assumes that the system operator provides the power references that must be supplied to the receiving grid. The advantage of this choice is that the voltage at the receiving-end is not a control variable (it can be measured or estimated) and thus, the calculation of the reference line currents is straightforward. The disadvantage of this

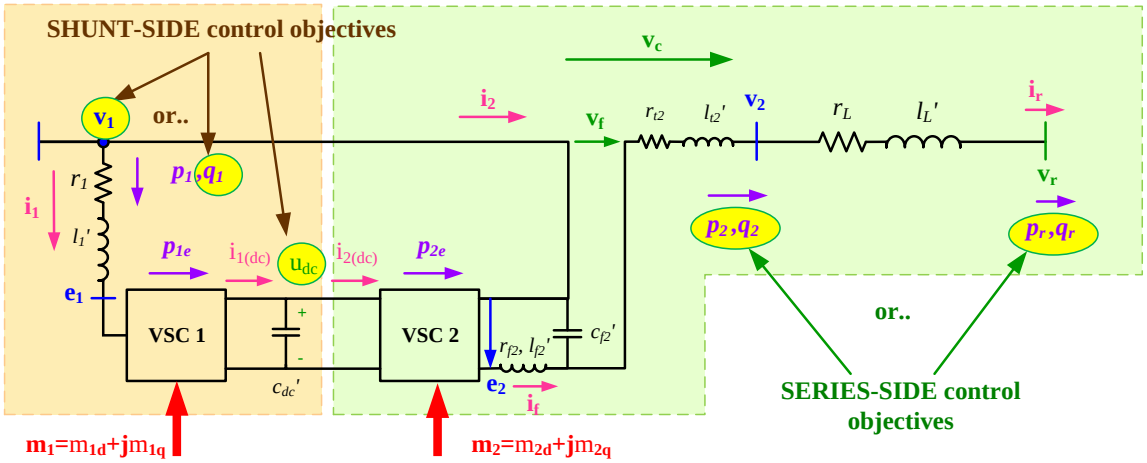


Figure III.3.3: Controllable objectives of a UPLC that is oriented to the positive SRF

reference selection is that, if the system operator does not provide the instant value of the voltage at the receiving-end, it is necessary to estimate it.

b) **To control the active and reactive powers, p_2 and q_2, at terminal 2.**

This option also assumes that the system operator can provide the power references at this point, which implies that the UPLC is included in their Optimal Power Flow (OPF) algorithm. The main shortcoming of this method is that, in this case, both $\mathbf{v_2}$ and $\mathbf{i_2}$ are to be controlled in the same time in order to yield p_2 and q_2.

The shunt-side converter is essentially in charge of regulating the DC-link voltage. However, besides the DC-link control, the shunt-side converter can control another objective. In this regard, two options are possible:

(i) to control the reactive power, q_1, at the connection point or,

(ii) to control the magnitude of the voltage at the connection point.

Both objectives are linked one to the other and the choice between one or the other depends on the preferences of the client. In this work, q_1 has been chosen as a control objective. Actually, if $\|\mathbf{v_1}\|$ is to be controlled, it is just necessary to add a cascaded loop that calculates ${q_1}^{ref}$ out of $\|\mathbf{v_1}\|^{ref}$.

3. Series-side control

3.1. Introduction to the series-side control

The series-side control, which is depicted in Fig.III.3.4, is divided in two control levels: a global control scheme and three local controllers.

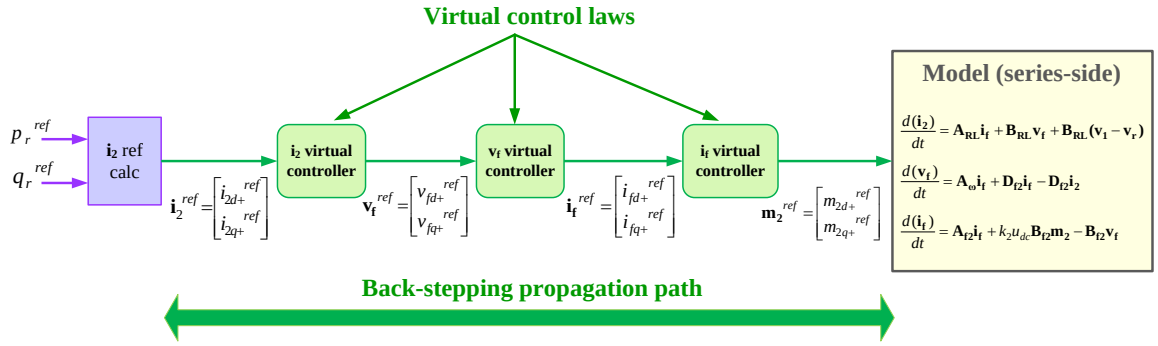


Figure III.3.4: Block diagram representing the Backstepping method applied to the series-side.

The global control scheme, which is based on Backstepping philosophy, is in charge of generating virtual control trajectories for the intermediate states of the system. It divides the control of a complex system into chain of smaller controlled subsystems. The working mechanism of the global control scheme can be understood by looking at the equations of the series-side (see below). These equations have a chained structure where the control input of a higher subsystem represents the reference signal of a lower subsystem (the developped form of the matrices can be found in Appendix E):

$$\frac{d\,\mathbf{i_2}}{dt} = \mathbf{A_{RL}} \cdot \mathbf{i_2} + \mathbf{B_{RL}} \cdot \mathbf{v_f} + \mathbf{B_{RL}} \cdot (\mathbf{v_1} - \mathbf{v_r}) \qquad \mathbf{i_2} \rightarrow \mathbf{i_2}^{ref} \implies \mathbf{v_f}^{ref} \tag{III.3.4}$$

$$\frac{d\mathbf{v_f}}{dt} = \mathbf{A_\omega}\ \mathbf{v_f} + \mathbf{D_{f2}}\ \mathbf{i_f} - \mathbf{D_{f2}}\ \mathbf{i_2} \qquad \mathbf{v_f} \rightarrow \mathbf{v_f}^{ref} \implies \mathbf{i_f}^{ref} \tag{III.3.5}$$

$$\frac{d\mathbf{i_f}}{dt} = \mathbf{A_{f2}}\ \mathbf{i_f} + k_2 \cdot u_{dc} \cdot \mathbf{B_{f2}}\ \mathbf{m_2} - \mathbf{B_{f2}}\ \mathbf{v_f} \qquad \mathbf{i_f} \rightarrow \mathbf{i_f}^{ref} \implies \mathbf{m_2}^{ref} \tag{III.3.6}$$

The global control for the series-side of the UPLC is described as follows :

- **Highest level control (3rd level)**

  The highest level controller is in charge of tracking $\mathbf{i_2}^{ref}$ according to equation (III.3.4), where $\mathbf{v_f}$ acts as a virtual control input. The first step is therefore to calculate a feedback control law that guarantees that the sybsystem (III.3.4) is stable and that it converges to the reference value $\mathbf{i_2}^{ref}$. Then, the obtained $\mathbf{v_f}^{ref}$ will be used as a reference for the 2nd controller.

- **Intermediate control (2nd level)**

  The intermediate controller borrows the virtual control input of the 3rd controller and uses it as a reference value. In this case, the reference value is $\mathbf{v_f}^{ref}$. Then, a feedback control law will assure that the intermediate subsystem is stable and that it tracks correctly the referece value. Analogous to the preceding step, the control law will yield a virtual control input that will serve as a reference for the next controller.

- **Lowest level control (1st level)**

  Finally, the lowest level controller will take the reference values from the preceding sub-

system (i.e. $\mathbf{i_f}^{ref}$) and an appropriate feedback control law will synthetize the values of the modulating signals $\mathbf{m_2}^{ref}$.

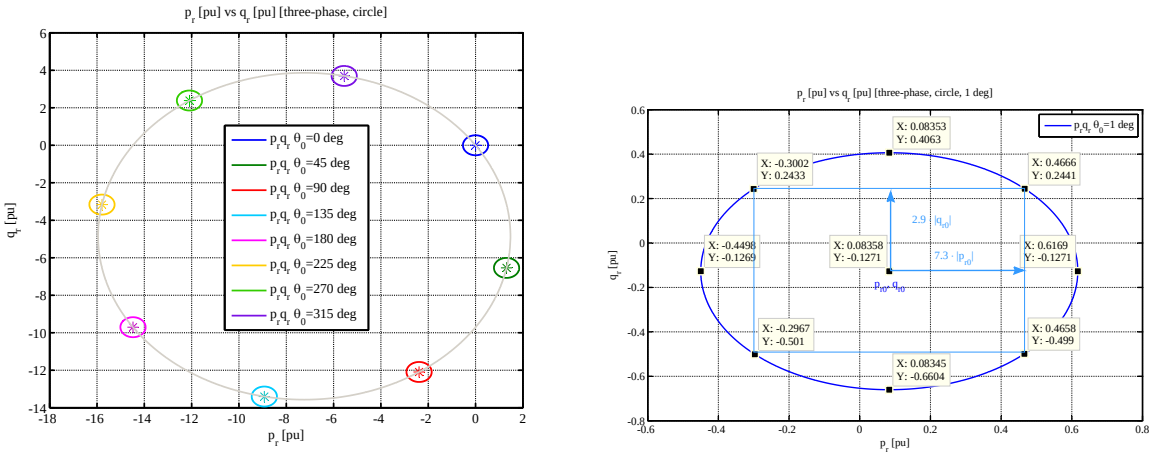
3.2. Reference calculation and power reachability areas

Before describing the control methods in depth, it is important to explain how the higher level references are calculated and what are the admissible ranges of this references. Indeed, it is not possible to ask for arbitrary values of p_r and q_r due to size limitations of the device.

The series control loop does not directly track p_r and q_r. It tracks the receiving-end currents $\mathbf{i_r}$. In the case of a RL line, the receiving-end currents are the same as the currents that flow through the line and through the primary winding of the series transformer ($\mathbf{i_2} = \mathbf{i_r}$). The reference line currents are calculated from the reference active and reactive powers using the following expression:

$$\begin{bmatrix} {i_{2d}}^{ref} \\ {i_{2q}}^{ref} \end{bmatrix} = \begin{bmatrix} {i_{rd}}^{ref} \\ {i_{rq}}^{ref} \end{bmatrix} = \frac{1}{{v_{rd}}^2 + {v_{rq}}^2} \cdot \begin{bmatrix} v_{rd} & v_{rq} \\ v_{rq} & -v_{rd} \end{bmatrix} \begin{bmatrix} {p_r}^{ref} \\ {q_r}^{ref} \end{bmatrix} \tag{III.3.7}$$

Then, it is necessary to know what is the range of values that the active and reactive powers can reach. The achievable active and reactive powers at the receiving-end depend on the transmission-angle between grids and the maximum series injected voltage. Fig.III.3.5(a) shows how the attainable receiving-end power areas move depending on the transmission angle. The big grey circumference represents the receiving-end powers when the UPLC is off and, the smaller coloured circles represent the attainable $p_r - q_r$ areas when the maximum series voltage (i.e $v_c = 0.06\ pu = 1000\ V$) is injected.



(a) (b)

Figure III.3.5: (a) Receiving-end power reachability areas in terms of the transmission angle (b) Power reachability area when $\theta_0 = 1\ deg$

As mentioned in the chapter dedicated to the dimensioning of the device, the transmission

angle must be kept around $\theta_0 = 1\ deg$ not to exceed the current limits of the line. FigIII.3.5(b) outlines the reachable p_r-q_r area when the transmission angle is 1 deg and the maximum injected voltage is 1000 V. As it can be noticed, the reference powers can theoretically span $p_r = p_{r0} \pm 7.3 \cdot |p_{r0}|$ and $q_r = q_{r0} \pm 2.9 \cdot |q_{r0}|$, where $p_{r0} = 0.08358\ pu \approx 1\ MW$ and $q_{r0} = -0.1271\ pu \approx 1.525\ MVAr$ (three-phase powers). These limits must be taken into account when providing the power references at the receiving-end.

3.3. Global control based on Lyapunov Theory

In the abovementioned introduction the global and local (virtual) control strategies for the series-side have been briefly introduced. The objective of this section is to provide a deeper description on how to design these control laws. Lyapunov theory, for example, is a very interesting tool to design the feedback control laws of the local controllers.

In the following lines, the fundamentals of Lyapunov's Theory are first introduced. Then, Lyapunov theory is used to deduce the control law of a local controller and, finally, the global control law is designed by linking the subsequent local controllers as explained before. It will be demonstrated that it is possible to design a global control law that is globally stable by independently designing stable local controllers based on Lyapunov's theory.

3.3.1. The fundamentals of Lyapunov theory

The local (virtual) control laws can be designed according to Lyapunov's theories, a Russian mathematician and engineer who laid the foundations of the stability theory of equilibrium points. According to these theories an equilibrium point is stable if all solutions starting at a nearby points stay nearby; otherwise it is unstable. Moreover, an equilibrium point is asymptotically stable if all solutions starting at nearby points not only stay nearby, but also tend to the equilibrium point as time approaches infinity [115].

Lyapunov developped a vast stability theory but here only one of its basic theorems (and one of the most known) is enunciated. This theorem is devoted to the case of autonomous systems [115]:

Theorem 1 *Let $x = 0$ be an equilibrium point for $\dot{x} = f(x)$ and $D \subset R^n$ be a domain containing $x = 0$. Let $V : D \to R$ be a continuously differentiable function such that*

$$V(0) = 0 \quad and \quad V(x) > 0 \quad in \quad D - 0 \tag{III.3.8}$$

$$\dot{V}(x) \leq 0 \quad in \quad D \tag{III.3.9}$$

Then, $x = 0$ is stable. Moreover, if

$$\dot{V}(x) < 0 \quad in \quad D - 0 \tag{III.3.10}$$

then $x = 0$ is asymptotically stable.

A continuously differentiable function $V(x)$ satisfying (III.3.8) and (III.3.9) is called a *Lyapunov function*. A function $V(x)$ satisfying condition (III.3.8) is said to be *positive definite*. If it satisfies the weaker condition $V(x) \leq 0$ for $x \neq 0$, is said to be positive semidefinite. A function $V(x)$ is said to be *negative definite* or *negative semidefinite* if $-V(x)$ is positive definite or positive semidefinite, respectively. According to these definitions, it is possible to rephrase Lyapunov's theorem to say that *the origin is stable if there is a continuously differentiable positive definite function $V(x)$ so that $\dot{V}(x)$ is negative semidefinite, and it is asymptotically stable if $\dot{V}(x)$ is negative definite.*

A class of scalar functions for which sign definiteness can be easily checked is the class of functions of the quadratic form

$$V(x) = x^T P x = \sum_{i=1}^{n} \sum_{j=1}^{n} p_{ij} x_i x_j \tag{III.3.11}$$

where P is a real symmetric matrix. In this case, $V(x)$ is positive definite (positive semidefinite) if and only if all the eigenvalues of P are positive (nonnegative).

It is therefore possible to design a control law that guarantees the convergence of the tracking error based on Lyapunov's stability theorem. In order to design this control law, it is necessary to first select a positive definite Lyapunov function. In this particular case, the selected Lyapunov function is a common quadratic function of the form:

$$V(\mathbf{e}) = \frac{1}{2}\mathbf{e}^{\mathrm{T}}\mathbf{e} \tag{III.3.12}$$

where $\mathbf{e} = \mathbf{x}^{ref} - \mathbf{x}$ is the tracking error vector and $\mathbf{x}^{ref}$ is a solution of the system.

In order to assure the convergence of the controlled system, the control law needs to be designed such that the derivative of $V(\mathbf{e})$ is negative:

$$\dot{V}(\mathbf{e}) = \mathbf{e}^{\mathrm{T}}\dot{\mathbf{e}} \leq 0 \tag{III.3.13}$$

For example, the control law can be chosen such that $\dot{\mathbf{e}} = -\mathbf{k_1}\mathbf{e}$ (where $\mathbf{k_1}$ is a positive definite matrix), the derivative of the Lyapunov function will also be negative:

$$\dot{V}(\mathbf{e}) = -\mathbf{e}^{\mathrm{T}}\mathbf{k_1}\mathbf{e} \leq 0 \tag{III.3.14}$$

Consequently, if $\dot{\mathbf{e}} = -\mathbf{k_1}\mathbf{e}$, the error will decay exponentially to zero.

Another possibility, that adds robustness to the controlled system in a similar way to sliding-

mode control, is to add a $-\mathbf{k_2} \cdot sgn(\mathbf{e})$ term to the error derivative,

$$\dot{\mathbf{e}} = -\mathbf{k_1}\mathbf{e} - \mathbf{k_2} \cdot sgn(\mathbf{e}) \tag{III.3.15}$$

$$\dot{V}(\mathbf{e}) = -\mathbf{e}^{\mathrm{T}}\mathbf{k_1}\mathbf{e} - \mathbf{e}^{\mathrm{T}}\mathbf{k_2} \cdot sgn(\mathbf{e}) \leq 0 \tag{III.3.16}$$

which also yields a negative $\dot{V}(\mathbf{e})$.

Thus, the action law of the local controllers will look like $\mathbf{u}_{\text{local ctr.}} = -\mathbf{k_1}\mathbf{e} - \mathbf{k_2} \cdot sgn(\mathbf{e})$. The coefficients of $\mathbf{k_1}$ influence the dynamics of the system and the coefficients of $\mathbf{k_2}$ influence the robustness of the system.

- **Shortcomings of the proposed approach in real systems**

In an ideal system with no switching devices or delays, it is possible to prove that there is a minimum value of $\mathbf{k_2}$ above which the robustness is assured for bounded modeling and parametrical deviations. This minimum value of $\mathbf{k_2}$, $\mathbf{k_{2(min)}}$ is determined by the upper bound of the system variations [115]. This means that, in an ideal system with no switching devices, if the values of $\mathbf{k_2}$ can be chosen arbitrarily large, the control law will always succeed to make the error zero no matter the nature of the variations of the system.

In reality, due to the imperfections of switching devices, delays, and sampling times, the use of a *signum* function may generate an undesirable effect known as chattering. Chattering is a repetitive zig-zag motion around the sliding surface that results in low control accuracy, high heat losses in electrical circuits, and high wear of moving mechanical counterparts [115]. Moreover, it may excite unmodelled high-frequency dynamics.

However, it is possible to reduce or eliminate chattering by replacing the *signum* function (sgn) by other smooth functions such as the *saturation* function (sat) or the *hyperbolic tangent* (tanh) [117, 118]. Fig.III.3.6 depicts some of these possible switching functions.

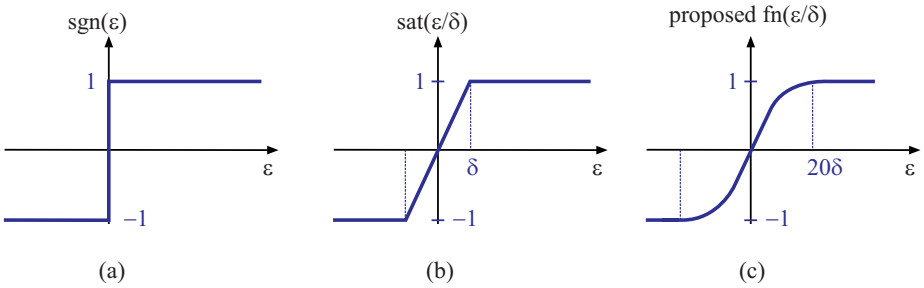


Figure III.3.6: Switching functions

In this work the *signum* function has been replaced by a smooth function of the form:

$$\text{Proposed function} = \frac{e}{|e| + \delta} \tag{III.3.17}$$

The slope of the proposed function and of the saturation function can be adapted by the variable δ, that will be chosen as small as possible (until chattering occurs). It is very important to have the smallest δ as possible because δ prevents the error trajectories from reaching the origin. The error will achieve a point near the origin but it will not reach the origin, creating a steady-state error. The smaller δ is, the smaller will be the boundary near the origin where the error trajectories will stabilize [115].

Summarizing, when the system is not ideal (which is always in today's digitalized systems), it is not possible to use the *signum* function because it creates chattering. A solution to reduce or eliminate chattering is to use softer functions that do not present a discontinuity at the origin. The problem that arises is that there is a trade-off between the reduction of chattering and the steady-state error. The smaller the slope of the switching functions is, the less chattering there is, but the bigger is the steady-state error. In some special cases, it may be possible to reduce the steady-state error by using an integral action [115].

3.3.2. Local (virtual) controller design based on Lyapunov Theory

Before introducing the Backstepping design procedure, the design of the intermediate virtual control laws is explained based on a particular example. This example will serve to understand how these virtual control laws are designed based on Lyapunov's stability theorems.

For this example, a system of the form

$$\dot{\mathbf{x}} = f(\mathbf{x}) + g(\mathbf{x})\mathbf{u} \tag{III.3.18}$$

has been chosen, where $\mathbf{x} \in R^n$ is the state-vector, $\mathbf{u} \in R^p$ is the control input, f and g are sufficiently smooth functions in a domain $D \in R^n$, and $g(\mathbf{x})$ is invertible.

The aim of the local controller is to track the reference $\mathbf{x}^{ref}$ (which is a solution of the system) or, what is the same, to make the tracking error zero:

$$\mathbf{e} = \mathbf{x}^{ref} - \mathbf{x} \to 0 \tag{III.3.19}$$

The first step in order to design the control law is to define a *Lyapunov function*. In this particular case, the following quadratic *Lyapunov function* is chosen.

$$V(\mathbf{e}) = \frac{1}{2}\mathbf{e}^{\mathrm{T}}\mathbf{e} \tag{III.3.20}$$

The derivative of the proposed *Lyapunov function* is

$$\dot{V}(\mathbf{e}) = \mathbf{e}^{\mathrm{T}}\dot{\mathbf{e}} \tag{III.3.21}$$

If the control law is chosen such that $\dot{\mathbf{e}} = -\mathbf{k_0}\mathbf{e} - \mathbf{k_1} \cdot sgn(\mathbf{e})$ (where $\mathbf{k_0}$ and $\mathbf{k_0}$ are positive

definite matrices), then the derivative of the proposed *Lyapunov function* will be negative:

$$\dot{V}(\mathbf{e}) = \mathbf{e}^{\mathrm{T}}\dot{\mathbf{e}} = -\mathbf{e}^{\mathrm{T}}\mathbf{k_0}\mathbf{e} - \mathbf{e}^{\mathrm{T}}\mathbf{k_1} \cdot sgn(\mathbf{e}) < 0 \tag{III.3.22}$$

$$\dot{V}(\mathbf{e}) \leq 0 \tag{III.3.23}$$

The expression of the control input that guarantees a negative derivative of the *Lyapunov function* is obtained from the following equality:

$$\dot{V}(\mathbf{e}) = \mathbf{e}^{\mathrm{T}}\dot{\mathbf{e}} = \mathbf{e}^{\mathrm{T}}(\dot{\mathbf{x}}^{ref} - \dot{\mathbf{x}}) = -\mathbf{e}^{\mathrm{T}}\mathbf{k_0}\mathbf{e} - \mathbf{e}^{\mathrm{T}}\mathbf{k_1} \cdot sgn(\mathbf{e}) \tag{III.3.24}$$

$$\dot{V}(\mathbf{e}) = \mathbf{e}^{\mathrm{T}}\dot{\mathbf{e}} = \mathbf{e}^{\mathrm{T}}[\dot{\mathbf{x}}^{ref} - (f(\mathbf{x}) + g(\mathbf{x})\mathbf{u})] = -\mathbf{e}^{\mathrm{T}}\mathbf{k_0}\mathbf{e} - \mathbf{e}^{\mathrm{T}}\mathbf{k_1} \cdot sgn(\mathbf{e}) \tag{III.3.25}$$

From where:

$$\mathbf{u} = g(\mathbf{x})^{-1}\left[+\mathbf{k_0}\mathbf{e} + \mathbf{k_1} \cdot sgn(\mathbf{e}) - f(\mathbf{x}) + \dot{\mathbf{x}}^{ref}\right] \tag{III.3.26}$$

Expression (III.3.26) guarantees that the tracking error will converge to zero since it assures that the derivative of the proposed Lyapunov function will be negative.

3.3.3. Backstepping design procedure

Once that the local (virtual) controller design based on Lyapunov theory has been introduced, the Backstepping design procedure is explained next. Backstepping procedure is often used to stabilize *strict-feedback* systems of the form [115]:

$$\begin{cases} \dot{\mathbf{x}} & = f_0(\mathbf{x}) + g_0(\mathbf{x})\mathbf{z_1} \\ \dot{\mathbf{z}}_\mathbf{1} & = f_1(\mathbf{x}, \mathbf{z_1}) + g_1(\mathbf{x}, \mathbf{z_1})\mathbf{z_2} \\ \dot{\mathbf{z}}_\mathbf{2} & = f_2(\mathbf{x}, \mathbf{z_1}, \mathbf{z_2}) + g_2(\mathbf{x}, \mathbf{z_1}, \mathbf{z_2})\mathbf{z_3} \\ & \vdots \\ \dot{\mathbf{z}}_{\mathbf{k-1}} & = f_{k-1}(\mathbf{x}, \mathbf{z_1}, \cdots, \mathbf{z_{k-1}}) + g_{k-1}(\mathbf{x}, \mathbf{z_1}, \cdots, \mathbf{z_{k-1}})\mathbf{z_k} \\ \dot{\mathbf{z}}_\mathbf{k} & = f_k(\mathbf{x}, \mathbf{z_1}, \cdots, \mathbf{z_k}) + g_k(\mathbf{x}, \mathbf{z_1}, \cdots, \mathbf{z_k})\mathbf{u} \end{cases} \tag{III.3.27}$$

where $x \in^n$, and f_0 to f_k vanish at the origin. The reason for referring to such systems as *strict-feedback* is that nonlinearities f_i and g_i in the $\dot{z}_i$ equations $(i = 1, \cdots, k)$ depend only on $x, z_1, \cdots, z_i$; that is, on the state variables that are *fed-back*. Additionally, it is assumed that

$$g_i(x, \cdots, z_i) \neq 0 \qquad for \;\; 1 \leq i \leq k \tag{III.3.28}$$

over the domain of interest. This is, $g_i(x, \cdots, z_i)$ is invertible for $(1 \leq i \leq k)$.

In this section the Backstepping procedure will be explained for a particular case where $k = 2$,

which matches with the series-side model. This is,

$$\begin{cases} \dot{\mathbf{x}} & = f_0(\mathbf{x}) + g_0(\mathbf{x})\mathbf{z_1} \\ \dot{\mathbf{z}}_1 & = f_1(\mathbf{x}, \mathbf{z_1}) + g_1(\mathbf{x}, \mathbf{z_1})\mathbf{z_2} \\ \dot{\mathbf{z}}_2 & = f_2(\mathbf{x}, \mathbf{z_1}, \mathbf{z_2}) + g_2(\mathbf{x}, \mathbf{z_1}, \mathbf{z_2})\mathbf{u} \end{cases} \tag{III.3.29}$$

where $\mathbf{u}$ is the global control input, and $\mathbf{z_1}$ and $\mathbf{z_2}$ are the intermediate virtual control variables.

The recursive procedure starts with the *higher* sub-system (the furthest from the *true* control input),

$$\dot{\mathbf{x}} = f_0(\mathbf{x}) + g_0(\mathbf{x})\mathbf{z_1} \tag{III.3.30}$$

where $\mathbf{z_1}$ is viewed as the virtual control input.

FIRST STEP

The **first step** is to obtain a state-feedback control law, $\mathbf{z_1}$, which will guarantee that $\mathbf{x}$ converges to the established reference $\mathbf{x}^{ref}$. Following the guidelines of section 3.3.2., it is possible to deduce a virtual control law of the form

$$\mathbf{z_1} = \mathbf{z_1}^{ref} = g_0(\mathbf{x})^{-1}\left[+\mathbf{k_{x(0)}}\ \mathbf{e_x} + \mathbf{k_{x(1)}} \cdot sgn(\mathbf{e_x}) - f_0(\mathbf{x}) + \dot{\mathbf{x}}^{ref}\right] \tag{III.3.31}$$

by using a quadratic Lyapunov function V_0 such that

$$V_0(\mathbf{e_x}) = \frac{1}{2}\mathbf{e_x}^{\mathrm{T}}\mathbf{e_x} \tag{III.3.32}$$

where $\mathbf{e_x} = \mathbf{x}^{ref} - \mathbf{x}$.

Thus, the proposed local controller satisfies the stability conditions enunciated by Lyapunov, which means that the $\mathbf{e_x}$ will converge to zero:

$$\dot{V}_0(\mathbf{e_x}) = \mathbf{e_x}^{\mathrm{T}}\left(\mathbf{k_{x(0)}}\ \mathbf{e_x} + \mathbf{k_{x(1)}} \cdot sgn(\mathbf{e_x})\right) \leq 0 \tag{III.3.33}$$

SECOND STEP

The **second step** is to is to obtain a state-feedback control law, $\mathbf{z_2}$, which will guarantee that $\mathbf{z_1}$ converges to the established reference $\mathbf{z_1}^{ref}$. This time, the proposed *Lyapunov function* is a composed of the previous *Lyapunov function* ($V_0(\mathbf{x})$) plus a quadratic function that depends on $\mathbf{e_{z1}}$. The new proposed *Lyapunov function* is then

$$\begin{aligned} V_1(\mathbf{e_x}, \mathbf{e_{z1}}) &= V_0(\mathbf{e_x}) + \frac{1}{2}\mathbf{e_{z1}}^{\mathrm{T}}\mathbf{e_{z1}} \\ &= \frac{1}{2}\mathbf{e_x}^{\mathrm{T}}\mathbf{e_x} + \frac{1}{2}\mathbf{e_{z1}}^{\mathrm{T}}\mathbf{e_{z1}} \end{aligned} \tag{III.3.34}$$

with a derivative

$$\begin{aligned}\dot{V}_1(\mathbf{e_x},\mathbf{e_{z1}}) &= \mathbf{e_x}^{\mathrm{T}}\dot{\mathbf{e}}_\mathbf{x} + \mathbf{e_{z1}}^{\mathrm{T}}\dot{\mathbf{e}}_\mathbf{z1}\\ \dot{V}_1(\mathbf{e_x},\mathbf{e_{z1}}) &= \mathbf{e_x}^{\mathrm{T}}\left[\mathbf{x}^{ref} - f_0(\mathbf{x}) - g_0(\mathbf{x})\mathbf{z_1}^{ref} + g_0(\mathbf{x})\mathbf{e_{z1}}\right]\\ &\quad + \mathbf{e_{z1}}^{\mathrm{T}}\left[\mathbf{z_1}^{ref} - f_1(\mathbf{x},\mathbf{z_1}) - g_1(\mathbf{x},\mathbf{z_1})\mathbf{z_2}\right]\end{aligned} \tag{III.3.35}$$

Please observe that in expression (III.3.35) the term $\mathbf{z_1}$ has been splitted in two terms: $\mathbf{z_1}^{ref}$ and $\mathbf{e_{z1}}$ ($\mathbf{z_1} = \mathbf{z_1}^{ref} - \mathbf{e_{z1}}$).

In order to guarantee an asymptotic tracking of $\mathbf{e_{z1}}$ the derivative of $V_1(\mathbf{e_x},\mathbf{e_{z1}})$ needs to be negative. In this case $\dot{V}_1(\mathbf{e_x},\mathbf{e_{z1}})$ is defined such that,

$$\begin{aligned}\dot{V}_1(\mathbf{e_x},\mathbf{e_{z1}}) &= \mathbf{e_x}^{\mathrm{T}}\left(\mathbf{k_{x(0)}}\ \mathbf{e_x} + \mathbf{k_{x(1)}}\cdot sgn(\mathbf{e_x})\right)\\ &\quad + \mathbf{e_{z1}}^{\mathrm{T}}\left(\mathbf{k_{z1(0)}}\ \mathbf{e_{z1}} + \mathbf{k_{z1(1)}}\cdot sgn(\mathbf{e_{z1}})\right) \le 0\end{aligned} \tag{III.3.36}$$

The derivative of $V_1(\mathbf{e_x},\mathbf{e_{z1}})$ will be negative if $\mathbf{k_{x(0)}}$, $\mathbf{k_{x(1)}}$, $\mathbf{k_{z1(0)}}$, and $\mathbf{k_{z1(1)}}$ are definite positive.

The expression of the intermediate control law $\mathbf{z_2}$ is obtained by equating (III.3.35) and (III.3.36) and by extracting the term $\mathbf{z_2}$:

$$\begin{aligned}&\mathbf{z_2} = \mathbf{z_2}^{ref} =\\ &= g_1(\mathbf{x},\mathbf{z_1})^{-1}\left[+\mathbf{k_{z1(0)}}\ \mathbf{e_{z1}} + \mathbf{k_{z1(1)}}\cdot sgn(\mathbf{e_{z1}}) - f_1(\mathbf{x},\mathbf{z_1}) + \dot{\mathbf{z}}_\mathbf{1}^{ref} + g_0(\mathbf{x})^{\mathrm{T}}\mathbf{e_x}\right]\end{aligned} \tag{III.3.37}$$

In (III.3.37) the term $g_0(\mathbf{x})^{\mathrm{T}}\mathbf{e_x}$ means that the dynamics of both subsystems are not totally decoupled.

It must also be noted that in expression (III.3.37) the time derivative of $\mathbf{z_1}$ is given by expression:

$$\begin{aligned}\dot{\mathbf{z}}_\mathbf{1}^{ref} &= \frac{d\mathbf{z_1}^{ref}}{dt} = \frac{\partial \mathbf{z_1}^{ref}}{\partial t} + \frac{\partial \mathbf{z_1}^{ref}}{\partial \mathbf{x}}\dot{\mathbf{x}}\\ &= g_0{}^{-1}\ddot{\mathbf{x}}^{ref} + \frac{\partial \mathbf{z_1}^{ref}}{\partial \mathbf{x}}\left(f_0(\mathbf{x}) + g_0(\mathbf{x})\mathbf{z_1}\right)\end{aligned} \tag{III.3.38}$$

THIRD STEP

Finally, the control input $\mathbf{u}$ is calculated in the **third step**. As in the previous step, the proposed function of *Lyapunov* is an extension of $V_1(\mathbf{e_x},\mathbf{e_{z1}})$:

$$\begin{aligned}V_2(\mathbf{e_x},\mathbf{e_{z1}},\mathbf{e_{z2}}) &= V_1(\mathbf{e_x},\mathbf{e_{z1}}) + \frac{1}{2}\mathbf{e_{z2}}^{\mathrm{T}}\mathbf{e_{z2}} =\\ &= \frac{1}{2}\mathbf{e_x}^{\mathrm{T}}\mathbf{e_x} + \frac{1}{2}\mathbf{e_{z1}}^{\mathrm{T}}\mathbf{e_{z1}} + \frac{1}{2}\mathbf{e_{z2}}^{\mathrm{T}}\mathbf{e_{z2}}\end{aligned} \tag{III.3.39}$$

and its derivative is

$$\begin{aligned}\dot{V}_2(\mathbf{e_x},\mathbf{e_{z1}},\mathbf{e_{z2}}) &= \mathbf{e_x}^{\mathrm{T}}\dot{\mathbf{e}}_\mathbf{x} + \mathbf{e_{z1}}^{\mathrm{T}}\dot{\mathbf{e}}_{\mathbf{z1}} + \mathbf{e_{z2}}^{\mathrm{T}}\dot{\mathbf{e}}_{\mathbf{z2}}\\ \dot{V}_2(\mathbf{e_x},\mathbf{e_{z1}},\mathbf{e_{z2}}) &= \mathbf{e_x}^{\mathrm{T}}\left[\mathbf{x}^{ref} - f_0(\mathbf{x}) - g_0(\mathbf{x})\mathbf{z_1}^{ref} + g_0(\mathbf{x})\mathbf{e_{z1}}\right]\\ &\quad + \mathbf{e_{z1}}^{\mathrm{T}}\left[\mathbf{z_1}^{ref} - f_1(\mathbf{x},\mathbf{z_1}) - g_1(\mathbf{x},\mathbf{z_1})\mathbf{z_2}^{ref} + g_1(\mathbf{x},\mathbf{z_1})\mathbf{e_{z2}}\right]\\ &\quad + \mathbf{e_{z2}}^{\mathrm{T}}\left[\mathbf{z_2}^{ref} - f_2(\mathbf{x},\mathbf{z_1},\mathbf{z_2}) - g_2(\mathbf{x},\mathbf{z_1},\mathbf{z_2})\mathbf{u}\right]\end{aligned} \tag{III.3.40}$$

In this case $\dot{V}_2(\mathbf{e_x},\mathbf{e_{z1}},\mathbf{e_{z2}})$ is defined such that,

$$\begin{aligned}\dot{V}_2(\mathbf{e_x},\mathbf{e_{z1}},\mathbf{e_{z1}}) &= \mathbf{e_x}^{\mathrm{T}}\left(\mathbf{k_{x(0)}}\ \mathbf{e_x} + \mathbf{k_{x(1)}}\cdot sgn(\mathbf{e_x})\right)\\ &\quad + \mathbf{e_{z1}}^{\mathrm{T}}\left(\mathbf{k_{z1(0)}}\ \mathbf{e_{z1}} + \mathbf{k_{z1(1)}}\cdot sgn(\mathbf{e_{z1}})\right)\\ &\quad + \mathbf{e_{z2}}^{\mathrm{T}}\left(\mathbf{k_{z2(0)}}\ \mathbf{e_{z2}} + \mathbf{k_{z2(1)}}\cdot sgn(\mathbf{e_{z2}})\right) \le 0\end{aligned} \tag{III.3.41}$$

The expression of the global control input $\mathbf{u}$ is finally obtained by equating (III.3.40) and (III.3.41) and by extracting the term $\mathbf{u}$:

$$\begin{aligned}&\mathbf{u} =\\ &= g_2(\mathbf{x},\mathbf{z_1},\mathbf{z_2})^{-1}\left[+\mathbf{k_{z2(0)}}\ \mathbf{e_{z2}} + \mathbf{k_{z2(1)}}\cdot sgn(\mathbf{e_{z2}}) - f_2(\mathbf{x},\mathbf{z_1},\mathbf{z_2}) + \dot{\mathbf{z}}_\mathbf{2}^{ref} + g_1(\mathbf{x},\mathbf{z_1})^{\mathrm{T}}\mathbf{e_{z1}}\right]\end{aligned} \tag{III.3.42}$$

Observe, once again, the term $g_1(\mathbf{x},\mathbf{z_1})^{\mathrm{T}}\mathbf{e_{z1}}$ that couples the dynamics of $\mathbf{z_2}$ and $\mathbf{z_1}$. Additionally, in expression (III.3.42), the time derivative of $\mathbf{z_2}$ is given by expression:

$$\dot{\mathbf{z}}_\mathbf{2}^{ref} = \frac{d\mathbf{z_2}^{ref}}{dt} = \frac{\partial \mathbf{z_2}^{ref}}{\partial t} + \frac{\partial \mathbf{z_2}^{ref}}{\partial \mathbf{x}}\dot{\mathbf{x}} + \frac{\partial \mathbf{z_2}^{ref}}{\partial \mathbf{z_1}}\dot{\mathbf{z}}_\mathbf{1} \tag{III.3.43}$$

The chosen control laws guarantee that the global system is stable, since $\dot{V}_2 < 0$. Moreover, the desired performances can be modified by adjusting matrices $\mathbf{k_{(0)}}$ and $\mathbf{k_{(1)}}$. The matrix $\mathbf{k_{(0)}}$ determines the dynamics of the system and $\mathbf{k_{(1)}}$ define the robustness of the system against variations in f, g and unmodelled perturbations.

3.3.4. Virtual control expressions of the local series controllers

Coming back to the series-side control, the control concepts described above can be applied to equations (III.3.4)-(III.3.6), which are repeated below:

$$\begin{cases}\frac{d\ \mathbf{i_2}}{dt} = [\mathbf{A_{RL}}\cdot\mathbf{i_2} + \mathbf{B_{RL}}\cdot(\mathbf{v_1} - \mathbf{v_r})] + \mathbf{B_{RL}}\cdot\mathbf{v_f}\\ \frac{d\ \mathbf{v_f}}{dt} = [\mathbf{A}_\omega\ \mathbf{v_f} - \mathbf{D_{f2}}\ \mathbf{i_2}] + \mathbf{D_{f2}}\ \mathbf{i_f}\\ \frac{d\ \mathbf{i_f}}{dt} = \mathbf{A_{f2}}\ \mathbf{i_f} - \mathbf{B_{f2}}\ \mathbf{v_f} + k_2\cdot u_{dc}\cdot\mathbf{B_{f2}}\ \mathbf{m_2}\end{cases} \tag{III.3.44}$$

Based on the preceding development the virtual control laws become:

$$\mathbf{v_f^{ref}} = \mathbf{B_{RL}}^{-1}\left\{\mathbf{K_{i2-0}}\ \mathbf{e_{i2}} + \mathbf{K_{i2-1}}\cdot sgn\left(\mathbf{e_{i2}}\right) + \frac{d\mathbf{i_2}^{ref}}{dt} - \mathbf{A_{RL}}\ \mathbf{i_2} - \mathbf{B_{RL}}\ \left(\mathbf{v_1} - \mathbf{v_r}\right)\right\} \tag{III.3.45}$$

$$\mathbf{i_f^{ref}} = \mathbf{D_{f2}}^{-1}\left\{\mathbf{K_{vf-0}}\ \mathbf{e_{vf}} + \mathbf{K_{vf-1}}\cdot sgn\left(\mathbf{e_{vf}}\right) + \frac{d\mathbf{v_f}^{ref}}{dt} - \mathbf{A}_{\omega}\ \mathbf{v_f} + \mathbf{C_{f2}}\ \mathbf{i_2} + \mathbf{B_{RL}}^{\mathrm{T}}\ \mathbf{e_{i2}}\right\} \tag{III.3.46}$$

$$\mathbf{m_2^{ref}} = \frac{k_2}{u_{dc}}\ \mathbf{B_{f2}}^{-1}\left\{\mathbf{K_{if-0}}\ \mathbf{e_{if}} + \mathbf{K_{if-1}}\cdot sgn\left(\mathbf{e_{if}}\right) + \frac{d\mathbf{i_f}^{ref}}{dt} - \mathbf{A_{f2}}\ \mathbf{i_f} + \mathbf{B_{f2}}\ \mathbf{v_f} + \mathbf{D_{f2}}^{\mathrm{T}}\ \mathbf{e_{vf}}\right\} \tag{III.3.47}$$

3.4. Performance of the global controller based in Lyapunov theory

The next lines provide the results obtained from the simulation of this control structure under nominal conditions, balanced voltage sags, and parametrical uncertainties.

3.4.1. Tracking performance under nominal conditions

Under nominal conditions this control allows a perfect tracking of ${p_r}^{ref}$ and ${q_r}^{ref}$. As it can be observed in Fig.III.3.7, the time constant of the current loop is around $\tau_{i2} = 1.2\ ms$ and there are not big cross-couplings between the d and q axis projections. The time constant of the current loop can be further decreased by increasing the gains of the controllers. However, these gains cannot be increased infinitively due to the switching times of the converters and the sampling times of the simulation.

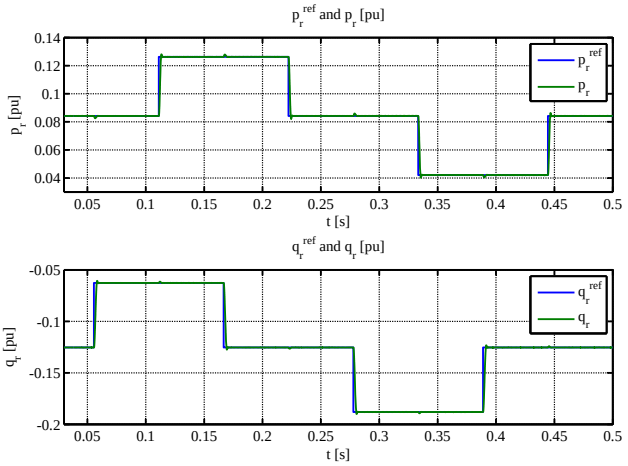


Figure III.3.7: p_r and q_r tracking under normal conditions

3.4.2. Control performance under balanced voltage sags

When a voltage-sag occurs, the magnitude of the current that flows through the line increases. When that happens, two options are possible:

- **Option 1: To bypass the series-side converter as soon as the voltage-sag is detected, as depicted in Fig.III.3.8.**

  According to this option the series-side of the UPLC only operates under nominal conditions. When the line current reaches a specified limit, which in this case is $\|i_{2(max)}\| = 350\ A = 0.24\ pu$, the bypass-switch switches on preventing the series-side converter from injecting any voltages. Thus, while the bypass-switch is on, the series-branch does not consume any power. However, from the moment when the voltage sag occurs to the moment when the switch activates there can be a strong active power demand from the series-side. This period of time is very critical for the regulation of the DC-link voltage, specially if the voltage sag is very steep.

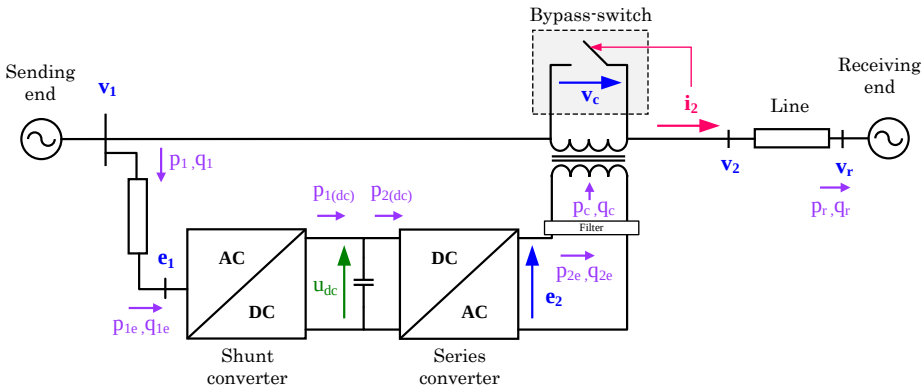


Figure III.3.8: One-line simplified schema of UPLC with bypass-switch

Fig.III.3.9 shows the values of p_r and q_r when a 30% voltage sag occurs in $|\mathbf{v_r}|$. As it can be observed, the voltage sag is detected at 0.14 s and the the bypass switch opens 0.05 s after the sag is over. During the time where the the bypass switch is closed the line current increases until the limit given by system conditions. During this time, the components of the apparatus are in *stand-by* mode and are not subjected to any additional stress. However, the line needs to stand a very high current (around 40 times the thermal limit)).

The results are similar when the voltage sag occurs at $\mathbf{v_1}$. These results are depicted in section 4.5.1..

- **Option 2: To dimension the series-side converter to be able to compensate for the voltage-sag.**

  The second option is to provide the series-branch with the capability of compensating for the sag, guaranteeing the tracking of the line current as in normal operation. In the

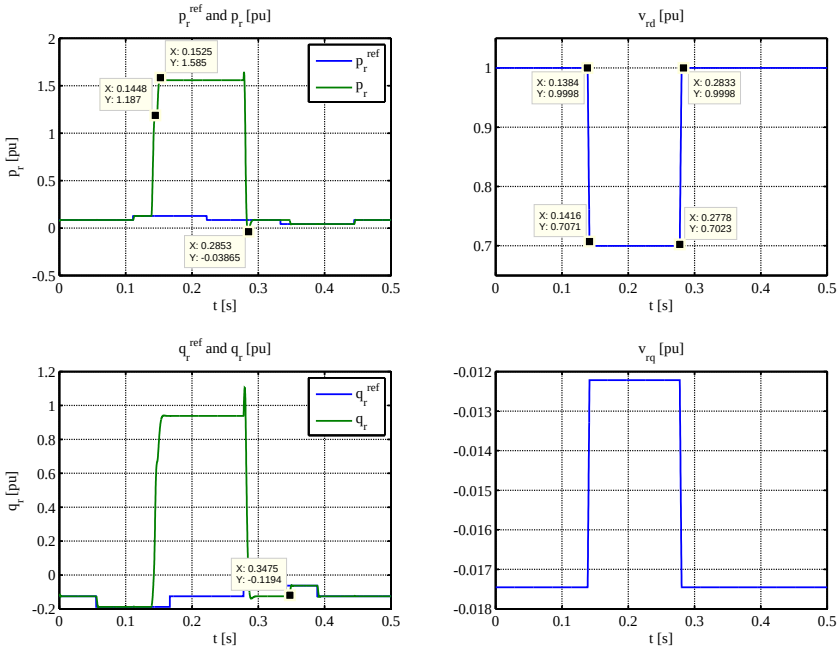


Figure III.3.9: p_r and q_r under a 30% voltage sag in v_r (series-side bypassed)

current case, the design of the UPLC is not adapted for such operation. However, it is possible to rise the voltage at the DC-link to about $u_{dc} = 12\ kV = 6\ pu$ in order to compensate for $\|\mathbf{v_1}\|$ and $\|\mathbf{v_r}\|$ sags of up to 30%. In this case, since the design of the UPLC has not been optimized for this operation, the waveforms are less filtered than in nominal operation.

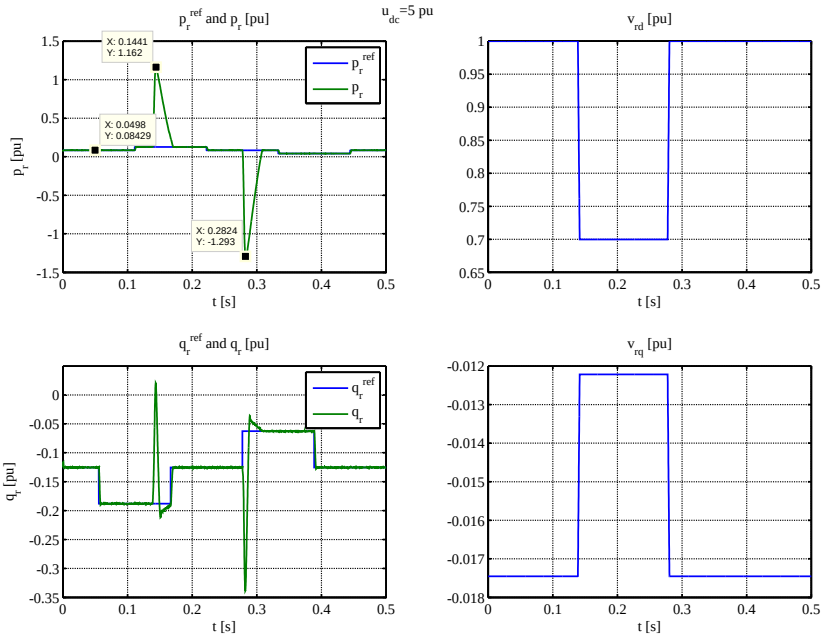


Figure III.3.10: p_r and q_r under a 30% voltage sag in v_r (series-side bypassed)

Fig.III.3.10 presents the tracking of p_r and q_r when the DC-link voltage is high enough to compensate for a 30% sag in $\mathbf{v_r}$. As it can be observed, the line current increases very fast when the fault occurs and the controller cannot force it to track the reference. The controller takes around 0.03 s to re-establish the current to its reference. These spikes can be minimized by increasing the gains of the controller and by reducing the simulation sampling time. However, in practice it is not possible to push these gains further due to the already low simulation sampling time (10 μs) and the switching period of the converters (200 μs).

3.5. Robustness against parametrical uncertainties

The term $\mathbf{k_2} \cdot sgn(\mathbf{e})$ of the controllers is entitled to increase the robustness of the closed-loop system against parametrical and modelling uncertainties. If there were no switching devices nor delays, an arbitrarily large value of $\mathbf{k_2}$ would guarantee the robustness of the system face to bounded uncertainties. However, as it was explained in section 3.3.1., when switching devices and delays exist, there is a trade-off between the values of $\mathbf{k_2}$, chattering, and steady-state errors.

Fig.III.3.11 shows a simulation case where the sampling time is $T_s = 10\ \mu s$ and the switching frequency of the converters is $f_s = 4950\ Hz$. Due to the switching limitations, it is not possible to higher the values of $\mathbf{k_2}$ above certain limits. Or, if the values of $\mathbf{k_2}$ are higher, also δ must be increased, which would generate a steady-state error in presence of uncertainties. In this case, three parametrical deviation cases are depicted: an ideal case where the estimated model parameters match the real parameters, a case where all the estimated parameters are 20% higher than the real parameters, and a case where the estimated parameters are 20% lower than the real parameters.

As it is observed, in Fig.III.3.11 the current follows the reference but, when the predicted parameters do not match real parameters, a steady-state error appears. In order to check that the sampling time and the switching of the converters has an influence on this steady state error, a second simulation is launched. In the second simulation, the sampling time is lowered to $T_s = 0.1\ \mu s$ and the converters are ideal. This fact enables highering the values of $\mathbf{k_2}$, therefore reducing the static tracking errors. Observe that the time scales of the simulation are not the same. The controller of the second example is much faster than the controller of the first example.

It can be concluded that, the higher the sampling time and the switching frequency is, the higher can be chosen the value of $\mathbf{k_2}$, and the higher it will be the robustness against parametrical variations.

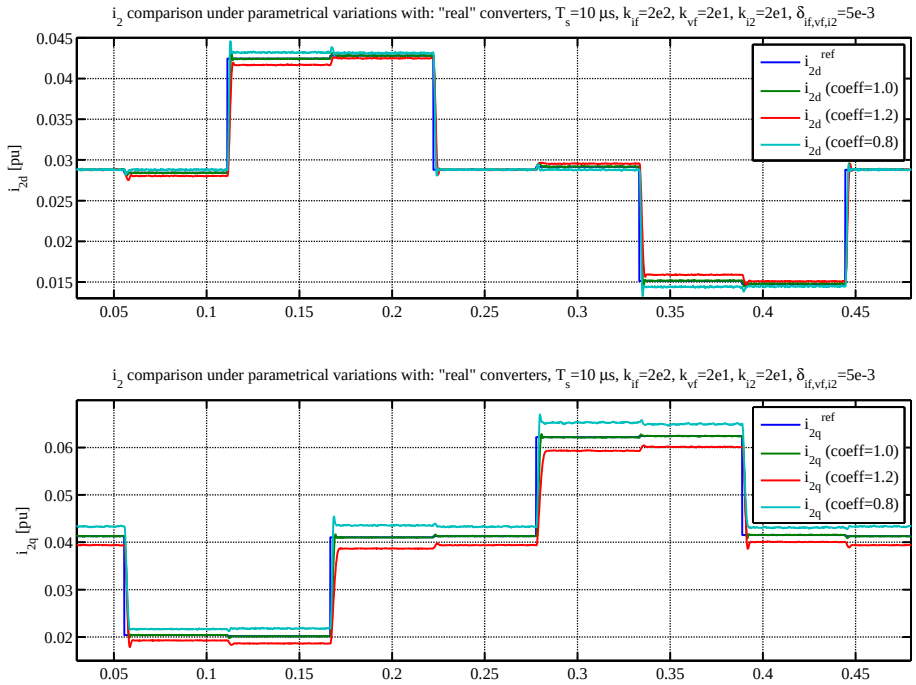


Figure III.3.11: i_2 tracking under parametrical variations with Lyapunov-based local controllers (switching converters)

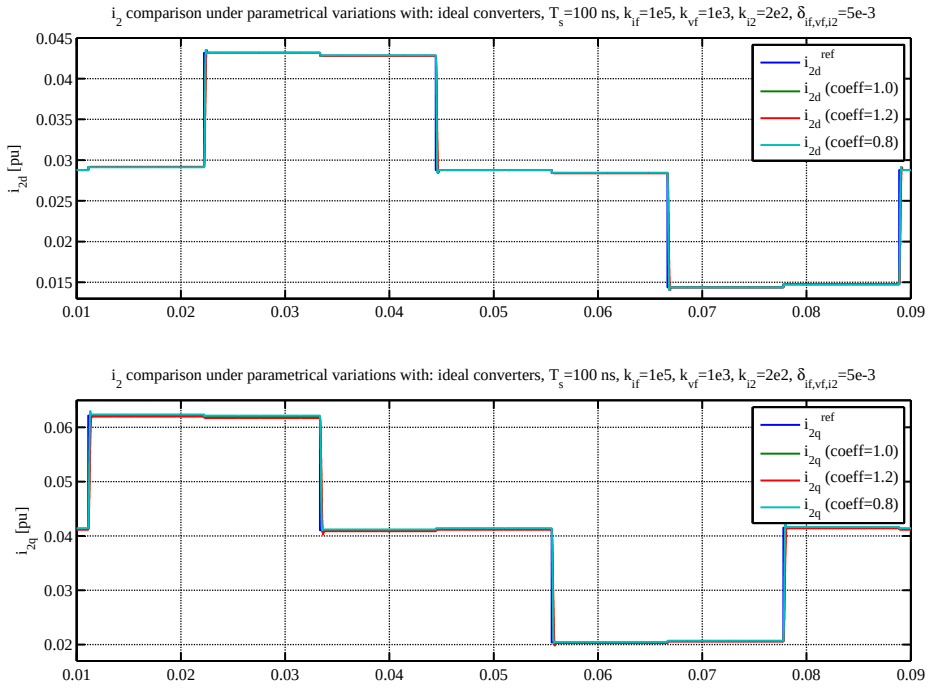


Figure III.3.12: i_2 tracking under parametrical variations with Lyapunov-based controllers (ideal converters)

3.6. Comparison of Lyapunov-based controllers and PI controllers

The local controllers used in the frame of the global trajectory generation philosophy depicted in Fig.III.3.4 can be of any type. In the foregoing sections local controllers of the form $u_c = \mathbf{k_1}\ \mathbf{e} + \mathbf{k_2} \cdot sgn(\mathbf{e})$ have been used due to their analytically verifiable stability and robustness properties. However, any other types of controllers can be used.

Since PI controllers are rather familiar to the power community, this option has also been tested in simulations. In this section , the robustness of PI controllers is tested by making the same parametrical changes than in the preceding section. The robustness of PI controllers face to ±20% parametrical changes is striking. As it can be remarked in Fig.III.3.13 there are no steady-state errors in the simulated cases. The integrative part of the PI controller succeeds to compensate for all the existing errors.

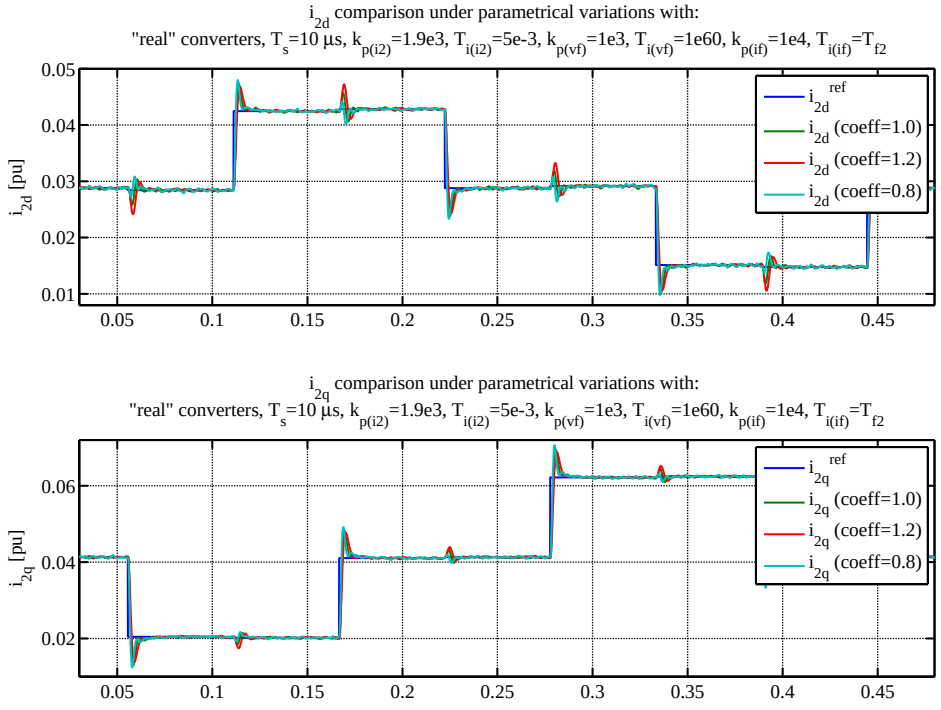


Figure III.3.13: i_2 tracking under parametrical variations with PI-type controllers (switching converters)

Despite the good results obtained by PI controllers, in the following work the first option is kept. The reason is that $u_c = \mathbf{k_1}\ \mathbf{e} + \mathbf{k_2} \cdot sgn(\mathbf{e})$ -type controllers have less overshoot (for the same rise-time), less cross-coupling, and can track oscillating signals, which could be useful for situations where the current references are not constant (in the case of dynamic damping oscillation, for example).

4. Shunt-side control

Before introducing the shunt-side control, the structure of the shunt-side model will be briefly analysed. Shunt-side dynamics are modelled by the shunt-current and the DC-voltage equations. These equations were already introduced in a previous chapter but are repeated here as a reminder.

- **Shunt-current equations**

$$\frac{d\,\mathbf{i_1}}{dt} = \mathbf{A_1}\cdot\mathbf{i_1} + \mathbf{B_1}\cdot\mathbf{v_1} - \mathbf{B_1}\cdot k_1\cdot\mathbf{m_1}\cdot u_{dc} \tag{III.3.48}$$

$$\frac{d}{dt}\begin{bmatrix} i_{1_d} \\ i_{1_q} \end{bmatrix} = \begin{bmatrix} \text{-}r_1/l_1' & \omega \\ \text{-}\omega & \text{-}r_1/{l_1}' \end{bmatrix}\begin{bmatrix} i_{1_d} \\ i_{1_q} \end{bmatrix} + \begin{bmatrix} 1/l_1' & 0 \\ 0 & 1/l_1' \end{bmatrix}\begin{bmatrix} v_{1_d} \\ v_{1_q} \end{bmatrix} - \begin{bmatrix} 1/l_1' & 0 \\ 0 & 1/l_1' \end{bmatrix}\cdot k_1\begin{bmatrix} m_{1_d} \\ m_{1_q} \end{bmatrix}\cdot u_{dc}$$

  where $\mathbf{i_1}$ represents the controlled state-vector, $\mathbf{m_1}$ is the input-vector, and $\mathbf{v_1}$ behaves as the perturbation vector.

  In equation (III.3.48), the input-vector is multiplied by u_{dc}, which is another controlled state variable. Thus, it is easily observed that there is a cross-coupling between the dynamics of the shunt-current and the DC-voltage.

- **DC-link voltage equation**

$$\frac{d\,u_{dc}}{dt} = \frac{1}{c_{dc}'\,u_{dc}}[p_{1e} - p_{2e}] \quad \text{or,} \qquad \dot{z} = \frac{d\,(u_{dc})^2}{dt} = \frac{2}{c_{dc}'}[p_{1e} - p_{2e}] \tag{III.3.49}$$

  The dynamics of the DC-link voltage depend upon the difference of powers that are absorved/provided by the series and shunt converters (p_{2e} and p_{1e}). In the same time, these powers depend on the DC-link voltage, u_{dc}, the modulation index, $\mathbf{m}$, and the AC currents ($p_e = \mathbf{e}\cdot\mathbf{i} = k\cdot u_{dc}\cdot[\mathbf{m^t}\cdot\mathbf{i}]$). This means that, once again, shunt-currents are directly involved in the expression of u_{dc}.

4.1. Control concept of the shunt-side system

A simple way of decoupling the shunt-current and DC-voltage control loops is to decouple both control loops in the time base, analogous to a cascaded loop. The shunt-current controller is tuned to have fast dynamics, and the DC-link controller is designed to yield slow dynamics, as depicted in Fig.III.3.14.

4.2. Reference calculation in the shunt-side system

The shunt-current controller is in charge of tracking a current reference value. As a result, it outputs a modulating signal for the converter switches. The current references are calculated from the power references. Two possibilites can be foreseen:

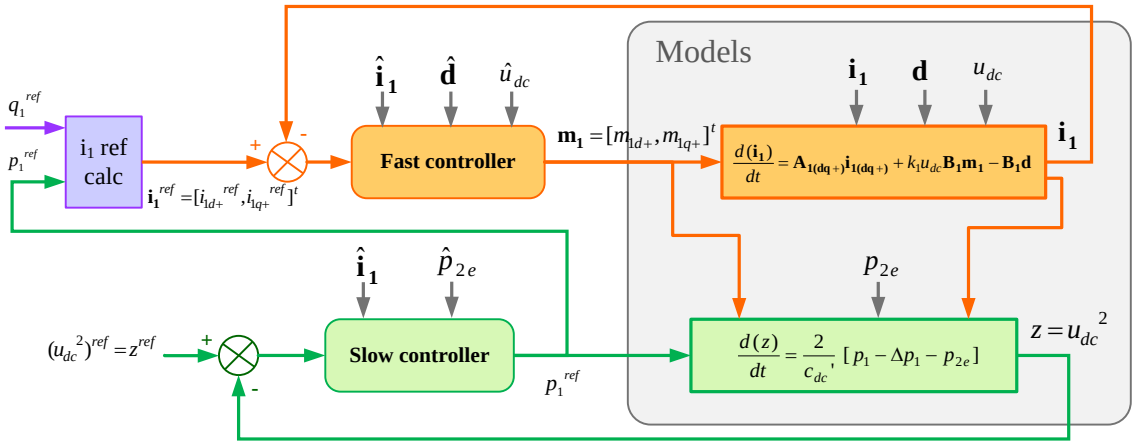


Figure III.3.14: Diagram of the shunt control structure

■ **Option 1:** The first alternative consists of calculating the current references from the active power at the converter input, p_{1e}, and the reactive power at the connection point, q_1, as:

$$\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} = \frac{1}{e_{1d}v_{1d} + e_{1q}v_{1q}} \cdot \begin{bmatrix} v_{1d} & v_{1q} \\ e_{1q} & -e_{1d} \end{bmatrix} \begin{bmatrix} p_{1e} \\ q_1 \end{bmatrix} \tag{III.3.50}$$

The advantage of this reference calculation way is that one of the inputs is the active power at the converter, p_{1e}. Since the term p_{1e} appears explicitly in DC-link voltage equations, the DC-voltage controller can be easily designed to provide this reference. However, the main disadvantage of this expression is that the voltages at the converter output, e_{1d} and e_{1q}, need to be used. These voltages are highly chopped and they introduce high frequency components in the current reference, complicating the tracking of the current. For this reason, a second alternative is proposed.

■ **Option 2:** The second option, which is used in this work, consists of using the active power at the connection point instead of the active power at the converter output. In this way, the use of e_{1d} and e_{1q} is avoided:

$$\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} = \frac{1}{v_{1d}^2 + v_{1q}^2} \cdot \begin{bmatrix} v_{1d} & v_{1q} \\ v_{1q} & -v_{1d} \end{bmatrix} \begin{bmatrix} p_1 \\ q_1 \end{bmatrix} \tag{III.3.51}$$

The only disadvantage of this method is that the DC-link voltage equation needs to be slightly modified in order to design the DC-voltage controller.

4.3. Reference limits in the shunt-side system

The shunt-side references cannot take any arbitrary values. Their limits are given by the particular design of the apparatus.

- **The possible reactive power reference values at the connection point,** q_1, are limited by the choice of the shunt transformer ratio, the shunt impedance, and the DC-bus voltage. In the present case, the reference values of q_1 and p_1 must always be located inside the circle depicted in Fig.III.3.15, which is determined by the particular design explained in a Chapter III.1. These limits must always be accounted for when selecting the reference values of q_1 in order to avoid the maloperation of the device.

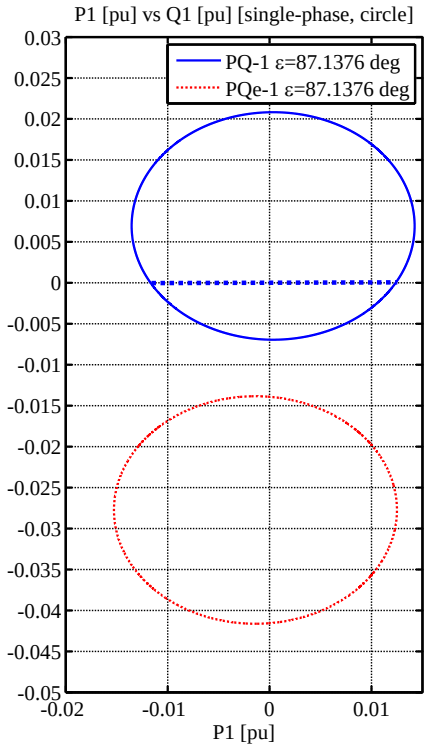


Figure III.3.15: Reachable P_1, P_{1e}, Q_1, and Q_{1e} areas

- **The active power reference at the connection point,** p_1, is indirectly given by the active power demanded/provided by the series-side converter, P_c and Q_c. The reachable areas of P_c and Q_c have already been depicted in Fig.III.1.19 and, according to the graph, the maximum injected active power is 150 $kW/phase$ = 0.0125 pu. Under disturbed conditions, the power demanded by the series-side converter may exceed this value. In that case, since the apparatus is designed to work in nominal conditions, the shunt-side branch would not be able to provide the required active power and the DC-link voltage may suffer from untolerable fluctuations. In order to avoid this type of eventualities, it is necessary to overdimension the apparatus. The over-rating must be done according to the expected disturbances.

- **The DC-link voltage reference** has been designed to be u_{dc} = 1.25 pu. In the simulations, this value can be increased in order to proof that the control strategies work correctly under distorted conditions that were not considered in the dimensioning stage. When u_{dc} is increased, however, the signals are not optimally filtered.

4.4. Shunt-current control

As discussed in the previous section, the shunt-current control loop must be much faster than the DC-voltage control loop.

The control law for the shunt-current is deduced from the expression of the universal controller. The *universal* controller could be defined as that controller that can force all the error dynamics of a system to zero. This controller could be described in the continuous form as:

$$k^n \frac{d^{(n)}}{dt^n}(e) + k^{n-1}\frac{d^{(n-1)}}{dt^{n-1}}(e) + \cdots + k^1 \frac{d}{dt}(e) + k\ e + \\ + k_1 \int e dt + k_2 \iint e dt + \cdots + k_n \underbrace{\int \cdots \int}_{n} e dt = 0 \tag{III.3.52}$$

Thus, the control law is deduced by assuming that the error dynamics follows the sub-trajectory

$$k^1 \frac{d}{dt}(e) + k\ e + k_1 \int e dt = 0 \tag{III.3.53}$$

Which actually yields a regular PI controller:

$$\frac{d\boldsymbol{e_{i1}}}{dt} = \frac{d\mathbf{i_{i1}}^{ref}}{dt} - \frac{d\mathbf{i_{i1}}}{dt} = -\mathbf{k_{p_{i1}}}\boldsymbol{e_{i1}} - \mathbf{k_{i_{i1}}} \int \boldsymbol{e_{i1}} dt \tag{III.3.54}$$

where, $\boldsymbol{e_{i1}} = [\varepsilon_{i1d}\ \varepsilon_{i1q}]^t$, $e_{i1d} = {i_{1d}}^{ref} - i_{1d}$, $\varepsilon_{i1q} = {i_{1q}}^{ref} - i_{1q}$, $\mathbf{k_{p_{i1}}} = diag(k_{p_{i1}}, k_{p_{i1}})$, and $\mathbf{k_{i_{i1}}} = diag(k_{i_{i1}}, k_{i_{i1}})$.

Substituting $\frac{d\mathbf{i}_{i1}}{dt}$ for (III.3.48) in (III.3.54):

$$\frac{d\mathbf{i_{i1}}^{ref}}{dt} - (\mathbf{A_1}\cdot\mathbf{i_1} - \mathbf{B_1}\cdot\mathbf{v_1} + \mathbf{B_1}\cdot k_1 \cdot \mathbf{m_1}\cdot u_{dc}) = -\mathbf{k_{p_{i1}}}\boldsymbol{e_{i1}} - \mathbf{k_{i_{i1}}} \int \boldsymbol{e_{i1}} dt \tag{III.3.55}$$

And solving for $\mathbf{m_1}$, $\mathbf{m_1}^{ref}$ is obtained:

$$\mathbf{m_1}^{ref} = \frac{1}{k_1 u_{dc}}\mathbf{B_1}\left[-\mathbf{k_{p_{i1}}}\boldsymbol{e_{i1}} - \mathbf{k_{i_{i1}}} \int \boldsymbol{e_{i1}} dt - \frac{d\mathbf{i_{i1}}^{ref}}{dt} + \mathbf{A_1}\cdot\mathbf{i_1} + \mathbf{B_1}\cdot\mathbf{v_1}\right] \tag{III.3.56}$$

Observe that, in equation (III.3.56), u_{dc} is used as a divider. It is extremely important that u_{dc} varies slowly in relation to the shunt-current, and that it does not reach zero. Otherwise, the shunt-current loop will destabilize. In this case, the shunt-current bandwidth is defined as $\omega_{b(i1)} = 3125\ rad/s$, which is around a tenth of the switching frequency. This value could further be highered up to half the switching frequency.

4.5. DC-link voltage control

As mentioned in the preceding section, DC-link voltage equations need to be adapted in order to bring the term p_1 to sight and to design a DC-voltage control. Taking equation (III.3.49) as a base-point, it is possible to rewrite it in terms of $\mathbf{v_1}$ and $\mathbf{i_1}$:

$$p_{1e} = \Re\{\mathbf{e_1 i_1}^*\} = \Re\{(\mathbf{v_1} - \mathbf{z_1 i_1} - l_1' \frac{d\mathbf{i_1}}{dt})\mathbf{i_1}^*\} = \\ = (v_{1d} i_{1d} + v_{1q} i_{1q}) - r_1({i_{1d}}^2 + {i_{1q}}^2) - l_1'(\frac{di_{1d}}{dt} i_{1d} + \frac{di_{1q}}{dt} i_{1q}) = p_1 - \Delta p_1 \tag{III.3.57}$$

where, $p_1 = v_{1d} i_{1d} + v_{1q} i_{1q}$ and $\Delta p_1 = r_1({i_{1d}}^2 + {i_{1q}}^2) + l_1'(\frac{di_{1d}}{dt} i_{1d} + \frac{di_{1q}}{dt} i_{1q})$. For the DC-voltage controller design, the derivative terms are considered zero, emulating the steady-state operation. Thus, for the controller design $\Delta p_1 = r_1({i_{1d}}^2 + {i_{1q}}^2)$. The DC-link voltage equation becomes:

$$\dot{z} = \frac{d\ (u_{dc})^2}{dt} = \frac{2}{c_{dc}'}[p_1 - \Delta p_1 - p_{2e}] \tag{III.3.58}$$

where the active power demanded by the series converter, p_{2e}, is considered as a disturbance of the system.

For the DC-voltage regulation a proportional-integral type controller is chosen. The error dynamics, ε_z, are defined accordingly:

$$\dot{\varepsilon}_z = \dot{z}^{ref} - \dot{z} = -k_{p_z}\varepsilon_z - \frac{k_{p_z}}{T_{i_z}} \int \varepsilon_z dt \tag{III.3.59}$$

Then, substituting the expression of $\dot{z}$ in III.3.59,

$$\dot{\varepsilon}_z = \dot{z}^{ref} - \frac{2}{{c_{dc}}'}[p_1 - \Delta p_1 - p_{2e}] = -k_{p_z}\varepsilon_z - \frac{k_{p_z}}{T_{i_z}} \int \varepsilon_z dt \tag{III.3.60}$$

it is possible to extract the term p_1, which will be the reference for the shunt-current reference calculating block:

$${p_1}^{ref} = \frac{{c_{dc}}'}{2} \left(\dot{z}^{ref} + k_{p_z}\varepsilon_z + \frac{k_{p_z}}{T_{i_z}} \int \varepsilon_z dt \right) + \Delta p_1 + p_{2e} \tag{III.3.61}$$

The values of the PI controller must be chosen such that the closed-loop dynamics of the DC-link is much slower than the shunt-current dynamics. As a rule of thumb, a ratio of ten is chosen. Since the closed-loop dynamics of the shunt-current loop have been chosen to be 10 times slower than the converter switching frequency, DC-link dynamics needs to be at least 100 times smaller than the switching frequency. Considering that the switching frequency of the converters is $w_{PWM} = 2\pi \cdot 4950 = 31102\ rad/s$, the closed loop dynamics of z have been chosen to be below 311 rad/s.

4.5.1. Shunt-side control validation

The u_{dc} control loop must face a large spectrum of situations in which it must regulate the DC-link voltage to the pre-defined value, both under nominal and disturbed conditions.

When working under "nominal" conditions (i.e. when all the voltages and currents are balanced and inside the design range), the series-side converter will demand/provide a variable active power from/to the DC-link ($p_{2e} = p_{2(dc)}$). The waveform of p_{2e} depends on the reference values of the receiving-end powers, p_r and q_r, that will entail different values of injected powers, p_c and q_c. For the simulations ${p_r}^{ref}$ and ${q_r}^{ref}$ are chosen to follow a rectangular wave-shape where the base-values, p_{ro} and q_{ro} (the values of p_r and q_r when the UPLC is switched off), are increased and decreased of 50%. The waveform of the reactive power at the connection point, ${q_1}^{ref}$, is also assumed to be rectangular and with an amplitude of ± 0.005 pu under nominal conditions.

Considering that the maximal active power that can be provided by the shunt-branch is $p_{dc(max)} = 0.0125$ pu, under nominal conditions, the design of the shunt-branch is sufficiently well adapted to provide the required active power to the series-branch. Under disturbed conditions, this is, when there are voltage sags in the sending- or receiving-ends, when the transmission-angle between both grids augments suddenly, when the unbalance level increases, or when a short-circuit occurs, for example, saturation problems may occur due to the limited rating of the apparatus. Indeed, the design presented in Chapter III.1 is oriented towards a nominal operation and does not take into account the eventual disturbations of the surrounding grid.

In these simulations, the behaviour of the DC-voltage control loop is presented under nominal conditions, and when a voltage sag of 20% occurs (the remaining voltage is 80%). The robustness of the proposed approach under parametrical uncertainties has also been simulated. The presented simulations have been simulated using the Matlab/Simulink *SimPowerSystems* toolbox using commutated voltage sources.

■ **Shunt-side control under nominal conditions**

In Fig.III.3.16 a full set of system variables, including DC-voltage deviations, is provided under nominal conditions.

As it is observed, the active powers at the DC-link are highly chopped. Since the measure of $p_{2(dc)}$ participates in the DC-voltage control equations, it may introduce high frequency components in the control loop. This approach, that uses the measure of $i_{2(dc)}$ as a feedforward term in the control loop, has also been used by other authors [119, 120]. However, it is not an easy task to measure the current at the DC-link due to its high current derivative. Moreover, the current sensor installation becomes complicated as the inverter power rating becomes large [121]. Some authors [122] use load estimation techniques instead of using current sensors at the DC-link. The improvement of this aspect is observed in the perspectives of this PhD.

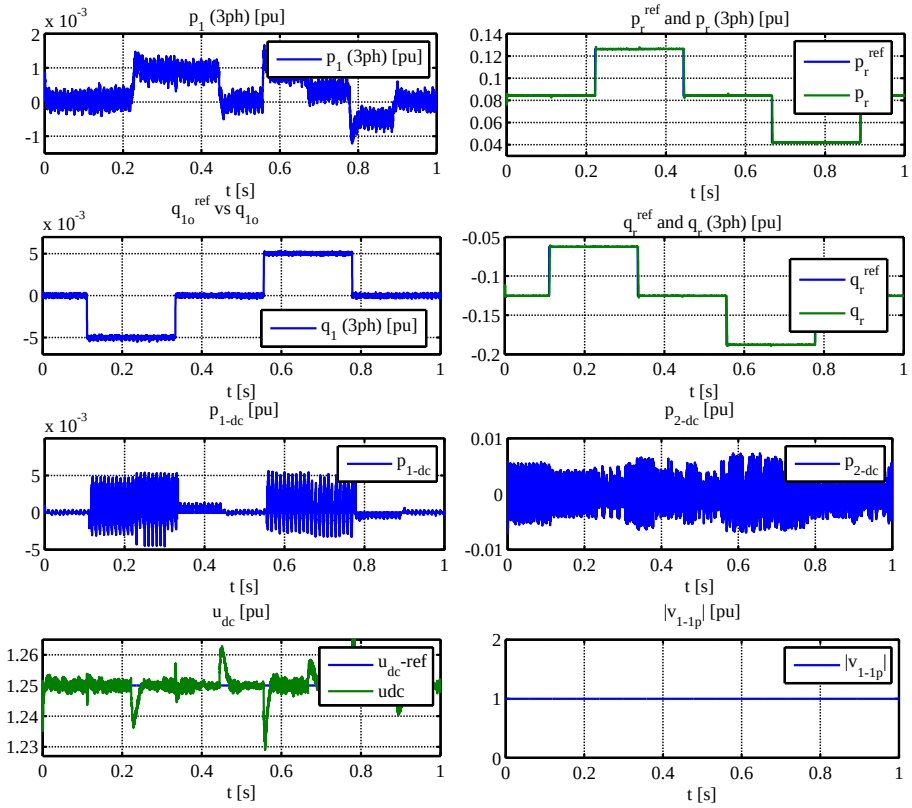


Figure III.3.16: u_{dc} voltage and other relevant signals when the series-side converter is on and the shunt-side reactive power is being tracked (nominal conditions).

The reactive power reference is perfectly tracked with a current ripple of 10%, and the largest DC-voltage deviation is of around 3%, which is a pretty acceptable excursion. The DC-voltage ripple could be further diminished by increasing the bandwidth of the controller but simulations have proven that this alternative reduces the stability of the DC-link in presence of sudden disturbances.

■ **Shunt-side control under $\|\mathbf{v_1}\|$ sags**

As aforementioned, when a voltage sag occurs at $\mathbf{v_1}$ two alternatives are possible: (a) to bypass the series-side converter, or (b) to charge the DC-link voltage to a higher value in order to be able to inject the necessary voltage to block the progression of the sag towards the receiving-end.

• **Option A: Bypassing the series-side**

While the series-converter is bypassed, the series-converter becomes inactive and it does not act on the DC-voltage. During that time, line current are not controlled and a natural power (with a high magnitude) flows towards the receiving-end. As it has been graphed in Fig.III.3.17, the active power revearses and the reactive power becomes capacitive.

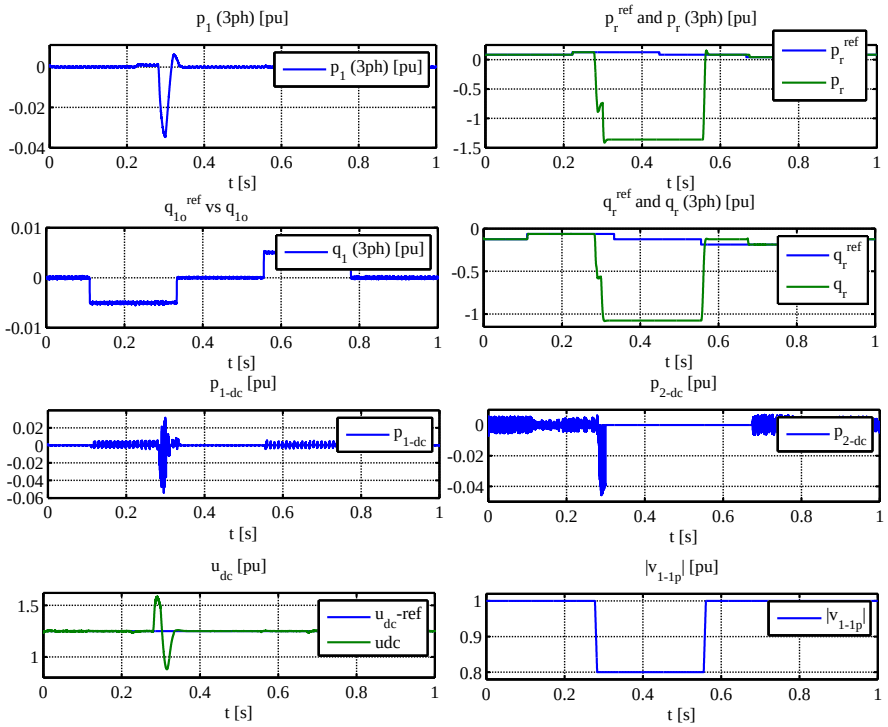


Figure III.3.17: u_{dc} voltage and other relevant signals when a 20% magnitude sag occurs in $|\mathbf{v_1}|$ and the series circuit is bypassed.

After the voltage-sag happens and before it is detected, there is a transient period during which the bypass-switch is still open, and where the current can increase very fast depending on slope of the sag. This transient period, that goes from the start of the voltage-sag $t_{sag-start} = 0.278\ s$ to its detection $t_{detect} = 0.30\ s$, can be observed in Fig.III.3.17. The abrupt $p_{2(dc)}$ injection provoques a high magnitude oscillation (around 56% peak-to-peak) in the DC-link voltage. In this case the problem could be solved by increasing the active power rating of the shunt-side converter and the value of DC-capacitor.

- **Option B: Charging u_{dc} to be able to inject enough series voltage**

  Fig.III.3.18 shows the performance of the DC-voltage control loop. In this case the DC-voltage deviation is smaller (around 28%) than in the preceding case. In any case, the difference of these two methods lies in the way that they generate the "perturbating" power, $p_{2(dc)}$, and this fact depends in a great manner on the control method used in the series-side. As mentioned before, the current ripple (peak-to-peak) increases to 35%.

■ Influence of parameter variations in the DC-voltage control

The proposed DC-link control must be robust against parametrical variations. In this regard, different simulation tests have been performed to check, in an informal way, the robustness of the control loops when the parameters differ from the design values.

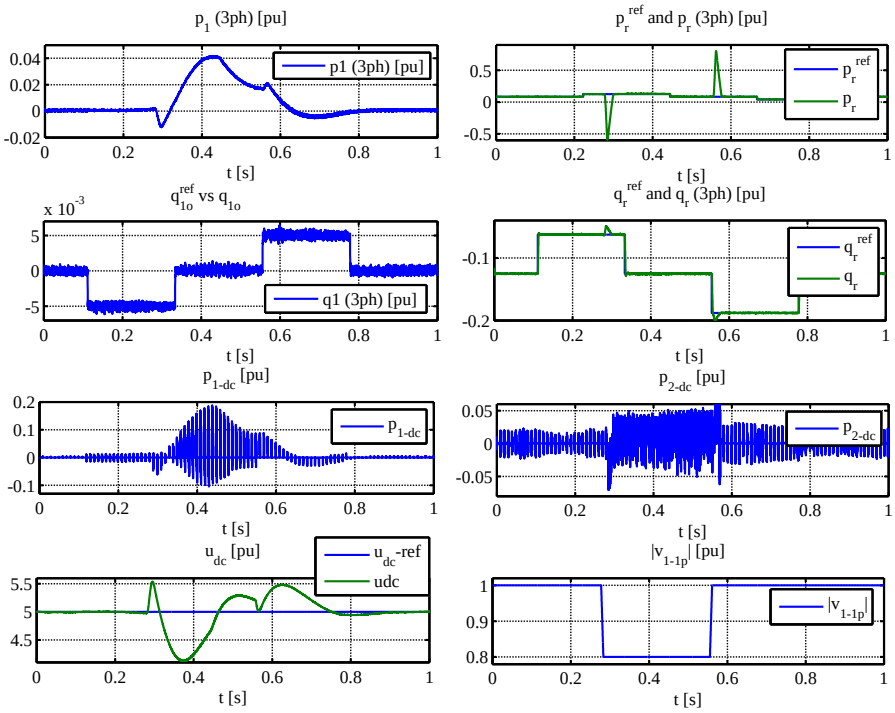


Figure III.3.18: u_{dc} voltage and other relevant signals when a 20% magnitude sag occurs in $|\mathbf{v_1}|$ but the DC-link voltage is high enough ($u_{dc} = 6\ pu$) as to ride-through it.

Fig.III.3.19, for example, shows the DC-link voltage during nominal conditions (with the same ${p_r}^{ref}$, ${q_r}^{ref}$, and ${q_1}^{ref}$ as in Fig.III.3.16) but changing the values of r_1, l'_1, and c'_{dc} of $\pm 50\%$ of the nominal values (all at the same time).

It can be observed that, even when the values are reduced to a half of the nominal value, the u_{dc} is well regulated. When the parameters are increased u_{dc} has a smaller ripple because the filtering properties of the DC-link and the shunt filter are also increased.

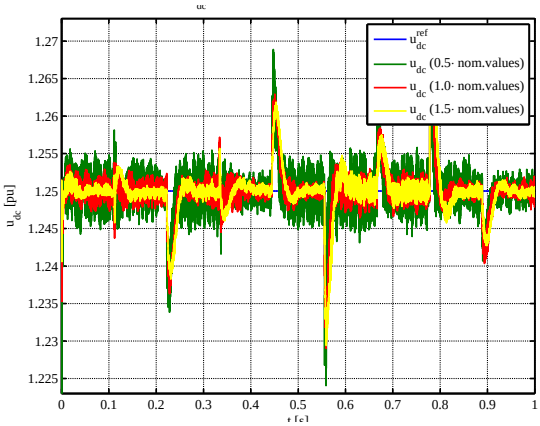


Figure III.3.19: u_{dc} voltage with different parametrical errors of R_1, L_1 and c'_{dc}.

5. Conclusions

This chapter describes the control of a UPLC connected to a lumped RL line where all the variables are refered to a positive SRF. All the developments assume that the synchronization system is ideal, without any errors, noise or delays.

The UPLC presents a multivariable structure with nonlinear relationships between state-variables and control inputs. Despite the complexity of the system, it is possible to simplify the control structure by dividing the system into smaller subsystems with different dynamics. The DC-link voltage, for example, appears multiplying the control inputs of the current sub-systems. If the DC-voltage is controlled very slowly, an effective decoupling is obtained between u_{dc} and the currents.

- The proposed series control consists of a global control law that establishes the virtual control trajectories of intermediate sub-systems. Each of the subsystems is virtually controlled by a local controller. The local controller can be designed according to any methods but, in this work, two approaches have been tested: (i) a Lyapunov-based design, and (ii) PI controllers.

  (i) The designed Lyapunov-based controller presents the form $\mathbf{u_c} = -\mathbf{k_0}\mathbf{e} - \mathbf{k_1} \cdot sgn(\mathbf{e})$. This structure is **theoretically** (in continuous systems) very robust against parametrical and modelling uncertainties and it can track oscillating references.

  However, **when the system is discrete**, a phenomenon called *chattering* can appear. One of the solutions to avoid chattering is to substitute the *signum* function by smoothing functions such as the *saturation* function. The only drawback of using these softer functions is that the error will not always converge to zero. The error trajectory can get trapped somewhere near the origin provoking a steady-state error.

  The proposed series control has been tested in simulation under nominal conditions, voltage sags, and parametrical uncertainties (unbalances will be later tested). In all the cases, the proposed controllers track the reference values correctly (except for parametrical uncertainties, where a small tracking error exists due to the discrete nature of the simulation system). For the simulations where voltage sags occur, it has been necessary to charge the DC-link voltage in order to provide the UPLC with the capacity of compensating for these disturbances. In the case that this is not possible, it is also possible to bypass the series-side.

  (ii) Simulation results have shown that PI controllers are robust under a given set of parametrical uncertainties and that the tracking error converges to zero in all the cases. The main drawback of PI controllers is that they can only track constant references. For this reason, in the rest of the work Lyapunov-based controllers are used.

- The proposed shunt control has also been tested in simulation under nominal conditions,

voltage sags, and parametrical uncertainties. In this case, the major encountered difficulty has been the limited dimensioning of the UPLC, that has been dimensioned too tightly. For being able to react against a wide variety of disturbances it is necessary to overdimension the shunt-side of the UPLC or to higher the capacity of the DC-link.

Chapter III.4

Positive SRF-oriented control of a UPLC connected to a cable

The preceding chapter has dealt with the control of a UPLC that is connected to an overhead RL line. However, cables can constitute an interesting alternative to over-head lines (OHLs) in cases where, for technical, environmental, aesthetical, or economic reasons, the lay out of OHLs is not possible. Some examples are highly populated areas and cities, underwater connections, and historical cites. In general, OHLs are usually prefered to cables due to their lower cost (at HVs cables are 3-5 times more expensive than OHLs and, at VHVs this ratio can be in the order of 10-20 at times) [123] and repair times. But, despite their higher cost, since they are buried, cables are not affected by atmospherical phenomena (e.g. wind, storms, ice) making their fault-rate much lower. It is not straightforward to decide whether it is more interesting to lay OHLs or cables but, as it has been observed, cables are more and more popular in MV rural and semi-rural distribution systems [123].

In this chapter, the control of a UPLC connected to a cable is described. As presented in chapter III.2, a cable can be modelled in many different ways considering lumped or distributed, constant or variable, parameters. The choice of a modelling approach depends on the accuracy and the complexity level aimed at. In this work the chosen 15 km cable is modelled by three π-sections in series, which allows representing frequency responses of up to 2500 Hz precisely. The structure of the model, described in chapter III.2, presents a perfect chained configuration to be controlled with Backstepping philosophy.

The present chapter is divided in two main parts:

- **In the first part of the chapter** the application of Backstepping philosophy (chained trajectory generation) to the control of a UPLC with a cable is described. Since the shunt-side control of the UPLC is kept unchanged in comparison to the case with a RL line, only the series-side control is explained and discussed.
- **In the second part of the chapter** the necessity of using an observer is introduced. The use of an observer is justified by two arguments:
  - i) On the one hand, the intermediate states of the cable are not directly measurable so, if a control is to be implemented, these states need to be observed.
  - ii) On the other hand, considering that the cable is 15 km long, it is not practical, from the control point of view, to measure the voltage and current at the end of the cable because the measured signals would arrive delayed and corrupted by noise.

1. Series UPLC control connected to a cable

In Fig.III.4.1, the one-line diagram of a UPLC connected to a cable, and its associated control, are depicted. In the figure, the series-side of the UPLC is represented by an ideal voltage source, a LC filter, and a series transformer. The cable is generically represented by N π-sections connected in series.

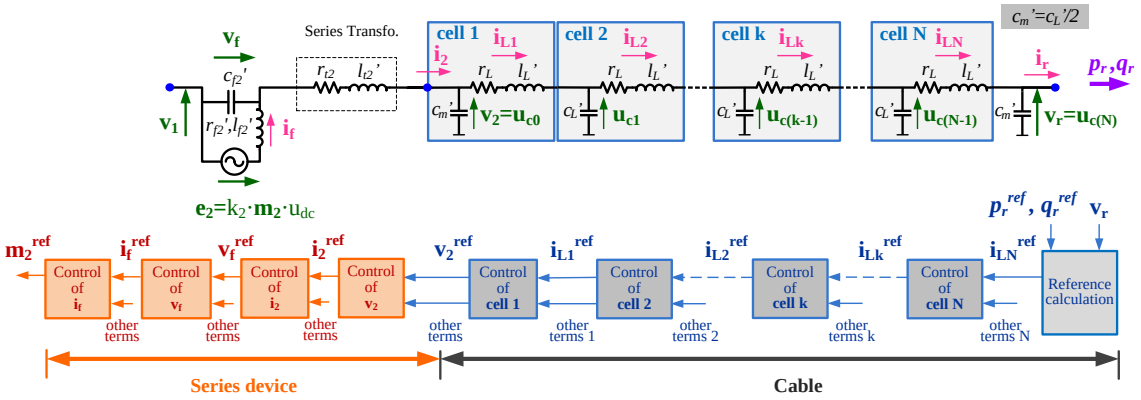


Figure III.4.1: Control structure (trajectory generation) of the series-side of the UPLC connected to a N-section cable

Since the model of the cable, that was detailed in chapter III.2, has a chained structure, the Backstepping control structure introduced in the preceding chapter is also appropriate in this case. Starting from the last cell, the trajectory generation control establishes a succesive series of virtual control inputs that serve as reference signals to consecutive control blocks. Thus, the global control strategy has a modular structure where an identical local structure is assigned to each of the cable cells.

1.1. Series-side reference calculation

The first step is to calculate the current reference vector of the last cell ($\mathbf{i_{LN}}^{ref}$). The current reference vector of the N-th cell is calculated from the current reference vector at the receiving-end ($\mathbf{i_r}^{ref}$), which is calculated from the required p_r and q_r powers.

- The current reference vector at the receiving-end, $\mathbf{i_r}^{ref}$, is obtained by the expression

$$\begin{bmatrix} {i_{rd}}^{ref} \\ {i_{rq}}^{ref} \end{bmatrix} = \frac{1}{{v_{rd}}^2 + {v_{rq}}^2} \cdot \begin{bmatrix} v_{rd} & v_{rq} \\ v_{rq} & -v_{rd} \end{bmatrix} \begin{bmatrix} {p_r}^{ref} \\ {q_r}^{ref} \end{bmatrix} \tag{III.4.1}$$

- Then, the current reference vector for the last cell is calculated by assuming that the derivative of the voltage at the receiving-end is zero:

$$(\mathbf{i_{LN}})^{\mathbf{ref}} = (\mathbf{i_r})^{\mathbf{ref}} + c_m' \frac{d\mathbf{v_r}}{dt} - \mathbf{Y_m}\ \mathbf{v_r} = (\mathbf{i_r})^{\mathbf{ref}} - \mathbf{Y_m}\ \mathbf{v_r} \tag{III.4.2}$$

where $\mathbf{Y_m} = [0\ \omega c'_m\ ;\ -\omega c'_m\ 0]$;.

1.2. Local control structure associated to each cable cell

The local control structure associated to each cable cell can be of many different types but, in this work, the philosophy explained in section 3.3., which combines a trajectory generation technique with the Lyapunov stability theorem, has been followed.

For simplicity, the local control structure of every cable cell has been chosen to be identical, except for the first cell, where matrix $\mathbf{D_L}$ must be replaced by $\mathbf{D_m}$ (c'_L is replaced by c'_m). Each of these cells can be represented by the set of equations

$$\frac{d\mathbf{i_{Lk}}}{dt} = \mathbf{A_L}\ \mathbf{i_{Lk}} + \mathbf{B_L}\ \mathbf{u_{c(k-1)}} - \mathbf{B_L}\ \mathbf{u_{ck}} \tag{III.4.3a}$$

$$\frac{d\mathbf{u_{c(k-1)}}}{dt} = \mathbf{A}(\omega)\ \mathbf{u_{c(k-1)}} + \mathbf{D_L}\ \mathbf{i_{L(k-1)}} - \mathbf{D_L}\ \mathbf{i_{Lk}} \tag{III.4.3b}$$

Then for every cable cell, the following procedure is followed:

a) First, the virtual control, $\mathbf{u_{c(k-1)}}^{ref}$, for equation (III.4.3a) is calculated in order to track $\mathbf{i_{Lk}}^{ref}$.

a) Then, the virtual control of equation (III.4.3a) is used as a reference for equation (III.4.3b) and the current reference for the next cell, $\mathbf{i_{L(k-1)}}^{ref}$, is calculated.

The afore mentioned procedure is graphically represented in Fig.III.4.2.

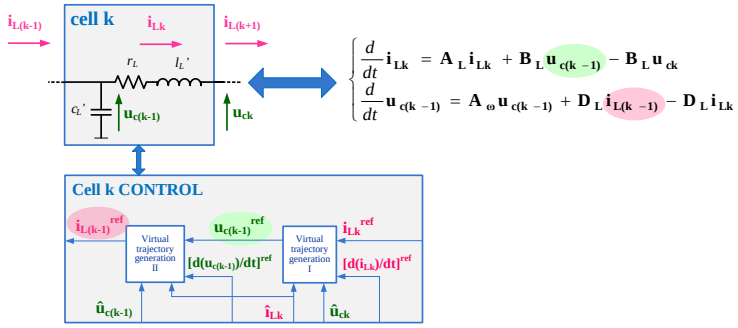


Figure III.4.2: Model and associated control (trajectory generation) of a cell k

The expressions of the virtual control laws of each cell can be obtained following the guidelines

of section 3.3.:

$$\mathbf{u_{c(k-1)}}^{ref} = \tag{III.4.4}$$
$$\mathbf{B_L}^{-1}\left\{\mathbf{k_{u-0}}\ \mathbf{e_{i_{Lk}}} + \mathbf{k_{u-1}}\ sgn\left(\mathbf{e_{i_{Lk}}}\right) + \frac{d\mathbf{i_{Lk}}^{ref}}{dt} - \mathbf{A_L}\ \mathbf{i_{Lk}} + \mathbf{D_L}^{\mathrm{T}}\ \mathbf{e_{u_{c(k-2)}}}\right\} + \mathbf{u_{ck}}$$

$$\mathbf{i_{L(k-1)}}^{ref} = \tag{III.4.5}$$
$$\mathbf{D_L}^{-1}\left\{\mathbf{k_{i-0}}\ \mathbf{e_{u_{c(k-1)}}} + \mathbf{k_{i-1}}\ sgn\left(\mathbf{e_{u_{c(k-1)}}}\right) + \frac{d\mathbf{u_{c(k-1)}}^{ref}}{dt} - \mathbf{A_\omega}\ \mathbf{u_{c(k-1)}} + \mathbf{B_L}^{\mathrm{T}}\ \mathbf{e_{i_{L(k)}}}\right\} + \mathbf{i_{Lk}}$$

where $\mathbf{e_{i_{Lk}}} = \mathbf{i_{L(k-1)}}^{ref} - \mathbf{i_{Lk}}$ and $\mathbf{e_{u_{c(k-1)}}} = \mathbf{u_{c(k-1)}}^{ref} - \mathbf{u_{c(k-1)}}$.

1.3. Control structure associated to the series device

The control structure (global and local) associated to the series device is very similar to the control structure of a UPLC connected to a RL line. The only change consists of substituting $\mathbf{A_{RL}}$, $\mathbf{B_{RL}}$, and $\mathbf{v_r}$ in equation (III.3.45) by $\mathbf{A_{t2}}$, $\mathbf{B_{t2}}$, and $\mathbf{v_2}$, respectively (matrix definitions in Appendix E).

$$\begin{cases} \vdots \\ \frac{d\mathbf{i_{L1}}}{dt} = \mathbf{A_L}\ \mathbf{i_{L1}} + \mathbf{B_L}\ \mathbf{v_2} - \mathbf{B_L}\ \mathbf{u_{c1}} \\ \frac{d\mathbf{v_2}}{dt} = \mathbf{A}(\omega)\ \mathbf{v_2} + \mathbf{D_L}\ \mathbf{i_2} - \mathbf{D_L}\ \mathbf{i_{L1}} \\ \frac{d\ \mathbf{i_2}}{dt} = [\mathbf{A_{t2}} \cdot \mathbf{i_2} + \mathbf{B_{t2}} \cdot (\mathbf{v_1} - \mathbf{v_2})] + \mathbf{B_{t2}} \cdot \mathbf{v_f} \\ \frac{d\ \mathbf{v_f}}{dt} = [\mathbf{A_\omega}\ \mathbf{v_f} - \mathbf{D_{f2}}\ \mathbf{i_2}] + \mathbf{D_{f2}}\ \mathbf{i_f} \\ \frac{d\ \mathbf{i_f}}{dt} = \mathbf{A_{f2}}\ \mathbf{i_f} - \mathbf{B_{f2}}\ \mathbf{v_f} + k_2 \cdot u_{dc} \cdot \mathbf{B_{f2}}\ \mathbf{m_2} \end{cases} \tag{III.4.6}$$

These changes yield,

$$\mathbf{v_f^{ref}} = \mathbf{B_{t2}}^{-1}\left\{\mathbf{K_{i2-0}}\ \mathbf{e_{i2}} + \mathbf{K_{i2-1}} \cdot sgn\left(\mathbf{e_{i2}}\right) + \frac{d\mathbf{i_2}^{ref}}{dt} - \mathbf{A_{t2}}\ \mathbf{i_2} - \mathbf{B_{t2}}\ (\mathbf{v_1} - \mathbf{v_2}) + \mathbf{D_m}^{\mathrm{T}}\ \mathbf{e_{v2}}\right\} \tag{III.4.7}$$

$$\mathbf{i_f^{ref}} = \mathbf{D_{f2}}^{-1}\left\{\mathbf{K_{vf-0}}\ \mathbf{e_{vf}} + \mathbf{K_{vf-1}} \cdot sgn\left(\mathbf{e_{vf}}\right) + \frac{d\mathbf{v_f}^{ref}}{dt} - \mathbf{A_\omega}\ \mathbf{v_f} + \mathbf{C_{f2}}\ \mathbf{i_2} + \mathbf{B_{t2}}^{\mathrm{T}}\ \mathbf{e_{i2}}\right\} \tag{III.4.8}$$

$$\mathbf{m_2^{ref}} = \frac{k_2}{u_{dc}}\ \mathbf{B_{f2}}^{-1}\left\{\mathbf{K_{if-0}}\ \mathbf{e_{if}} + \mathbf{K_{if-1}} \cdot sgn\left(\mathbf{e_{if}}\right) + \frac{d\mathbf{i_f}^{ref}}{dt} - \mathbf{A_{f2}}\ \mathbf{i_f} + \mathbf{B_{f2}}\ \mathbf{v_f} + \mathbf{D_{f2}}^{\mathrm{T}}\ \mathbf{e_{vf}}\right\} \tag{III.4.9}$$

In these equations $\mathbf{v_2}$ and $\mathbf{i_2}$ are given by the virtual control of the first cable cell:

$$\mathbf{v_2}^{ref} = \mathbf{B_L}^{-1} \left\{ \mathbf{k_{u-0}}\ \mathbf{e_{i_{L1}}} + \mathbf{k_{u-1}}\ sgn\left(\mathbf{e_{i_{L1}}}\right) + \frac{d\mathbf{i_{L1}}^{ref}}{dt} - \mathbf{A_L}\ \mathbf{i_{Lk1}} + \mathbf{D_L}^{\mathrm{T}}\ \mathbf{e_{u_{c(1)}}} \right\} + \mathbf{u_{c1}} \tag{III.4.10}$$

$$\mathbf{i_2}^{ref} = \mathbf{D_m}^{-1} \left\{ \mathbf{k_{i-0}}\ \mathbf{e_{v_2}} + \mathbf{k_{i-1}}\ sgn\left(\mathbf{e_{v_2}}\right) + \frac{d\mathbf{v_2}^{ref}}{dt} - \mathbf{A}_{\omega}\ \mathbf{v_2} + \mathbf{B_L}^{\mathrm{T}}\ \mathbf{e_{i_{L(1)}}} \right\} + \mathbf{i_{L1}} \tag{III.4.11}$$

1.4. Conclusions after simulations

The proposed control strategy, which consists on a global trajectory generation philosophy with Lyapunov-based local controllers, has been proven in simulations to be appropriate for the series-side control of a UPLC connected to a 3 π-section cable. These simulations have been performed in Simulink using an analytic model of the UPLC that considers ideal VSCs. This choice reduces the computational burden of the simulations and allows the use of higher controller gains without chattering.

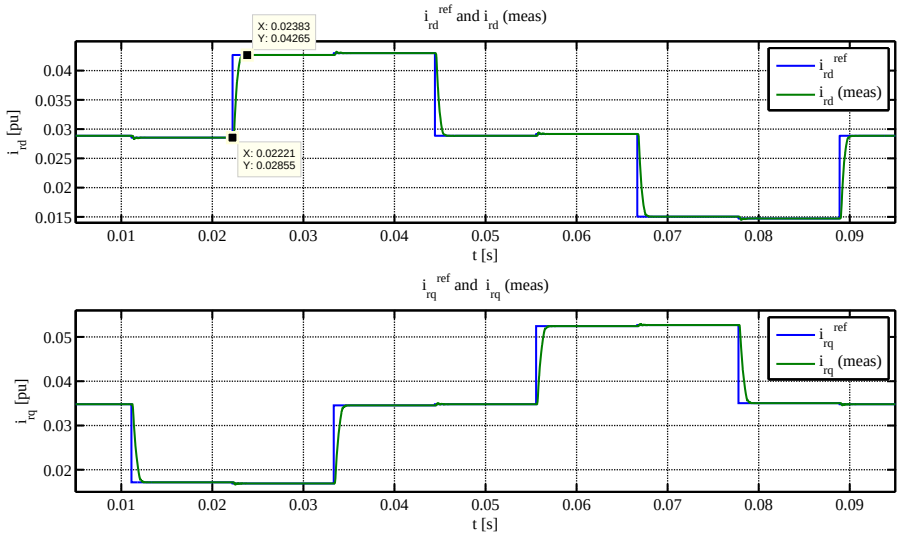


Figure III.4.3: Tracking results of $\mathbf{i_r}$ with a 3 π-section cable.

Fig.III.4.3 shows that $\mathbf{i_r}$ is perfectly tracked with a delay of just 1 ms and with no cross-couplings. This control strategy has also been successfully with a higher number of cells (5 max.) The simulations regarding voltage sags, unbalances, and parametrical uncertainties are not shown hereby because they are similar to those of the preceding chapter with a RL line. The drawn conclusions are therefore analogous, except for some additional details :

- In order to guarantee a good operation of the system it is adviced that the gains related to the cable controllers are the same. These gains must be lower than the gains related

to the control of $\mathbf{v_f}$ and $\mathbf{i_f}$ (the $\mathbf{i_f}$ controller must have the highest gain).

- It has been observed that there is a gain limitation for the $\mathbf{i_f}$ controller (the highest gains) that is given by the sampling time and the switching frequency of the converters. Moreover, if the number of cells is increased (for the same cable distance), all the gains need to be augmented.
- In the case that the converters are modelled as continuous voltage sources it is possible to increase the controller gain by reducing the simulation sampling time. However, if switching converters are used, it is necessary to increase the switching frequency of the converters. This fact leads to a practical limitation of this control method: it is only feasible to use this control method for a certain switching frequency, sampling time, and number of cells.

2. On the need of an observer

In practice, the above-described series control presents two shortcomings:

- Even if the cable has been modelled as a sequence of π-sections, in reality, it is not possible to physically obtain the intermediate states of the cable ($u_{c(k)}$ and $l_{L(k)}$) for the control expression. The shield of the cable only allows to measure voltages and currents at both ends of the cable.
- It is possible to measure voltages and currents at the far-end of the cable. However, there is always a communication delay between the measurement point and the device. The amount of delay can be expressed as [124]:

$$\tau = \tau_f + \tau_p + \frac{L}{R} + \theta \tag{III.4.12}$$

where τ is the total link delay, τ_f is the fixed delay associated with the transducers, processing and multiplexing, τ_p is the link propagation delay, L is the amount of data transmitted, R is the data rate of the link, and θ is the associated random delay jitter.

This means that, the communication delay not only depends on the type of communication link, but also in other aspects such as the time that the emitter and the receiver take to accommodate signals, or the protocol used to transmit the information. Table III.4.1 displays some indicative values of delays proposed by [124]. These values are just indicative values that have been calculated considering a set of assumptions. However, they provide an approximative idea of the relative delay diffference between propagation mediums.

Fortunately, there is a solution that overcomes the shortcomings related to distance measurement: the use of observers. Observers are *estimation* systems that are able to estimate the states of the observed system by measuring the inputs and the outputs of the system [125].

Table III.4.1: Delay calculations associated with various communication links according to [124]

Communication link	Associated delay (one way) [ms]
Fiber optic cables	≈ 100-150
Digital microwave links	≈ 100-150
Power line (PLC)	≈ 150-350
Telephone lines	≈ 200-300
Satellite link	≈ 500-700

When the system and the measurements are perturbed with noise, which is common in real systems, the Kalman observer (better known as *Kalman Filter*) presents an efficient alternative to the classical closed-loop observer (known as Luenberger Observer). The Kalman filter is an optimal closed-loop observer where the Kalman gain is computed iteratively to minimize the variance of the estimated error.

2.1. Observing the cable states by the Kalman Filter

In this work, the Kalman filter is used for estimating the states of a 3 π-section cable because the cable model presents a linear structure that can, eventually, be distorted by noise. The one-line diagram of the cable, including the state names, is presented in Fig.III.4.5. The Kalman filter measures the voltage and current at the cable-side terminals of the UPLC, $\mathbf{v_2}$ and $\mathbf{i_2}$, and estimates the state variables $\hat{\mathbf{x}}_{\mathbf{kal}} = [v_{rd}\ v_{rq}\ i_{L3d}\ i_{L3q}\ u_{c2d}\ u_{c2q}\ i_{L2d}\ i_{L2q}\ u_{c1d}\ u_{c1q}\ i_{L1d}\ i_{L1q}]^t$.

The current at the receiving-end is estimated in open-loop by the equation

$$(\mathbf{i_r})^{\mathbf{ref}} = (\mathbf{i_{LN}})^{\mathbf{ref}} - c'_m \frac{d\mathbf{v_r}}{dt} + \mathbf{Y_m}\ \mathbf{v_r} = (\mathbf{i_{LN}})^{\mathbf{ref}} + \mathbf{Y_m}\ \mathbf{v_r} \tag{III.4.13}$$

where $\mathbf{Y_m} = [0\ \omega c'_m\ ;\ -\omega c'_m\ 0]$. For this calculation, the derivative of $\mathbf{v_r}$ is assumed to be zero.

One of the characteristics of the Kalman filter is that it is implemented in discrete time. For this reason, in order to use the Kalman algorithm, it is necessary to discretize the continuous-form Kalman equations. In this work, the equations have been discretized using a dedicated Matlab function (called *c2d*) and choosing the zero-order hold option.

$$\begin{cases} \dot{\mathbf{x}}_{\mathbf{kal}}(t) &= \mathbf{A_{kal}}\ \mathbf{x_{kal}}(t) + \mathbf{B}\ \mathbf{u_{kal}}(t) \\ \mathbf{z_{kal}}(t) &= \mathbf{C_{kal}}\ \mathbf{x_{kal}}(t) \end{cases} \xrightarrow{Discretize} \begin{cases} \mathbf{x_{kal(k+1)}} &= \mathbf{F_{kal}}\ \mathbf{x_{kal(k)}} + \mathbf{G}\ \mathbf{u_{kal(k)}} \\ \mathbf{z_{kal(k)}} &= \mathbf{H_{kal}}\ \mathbf{x_{kal(k)}} \end{cases}$$

The continuous-time equations used in the Kalman filter are presented in Fig.III.4.4. For simplicity, in these equations, the dynamics of $\mathbf{v_r}$ are considered to be zero but, if known,

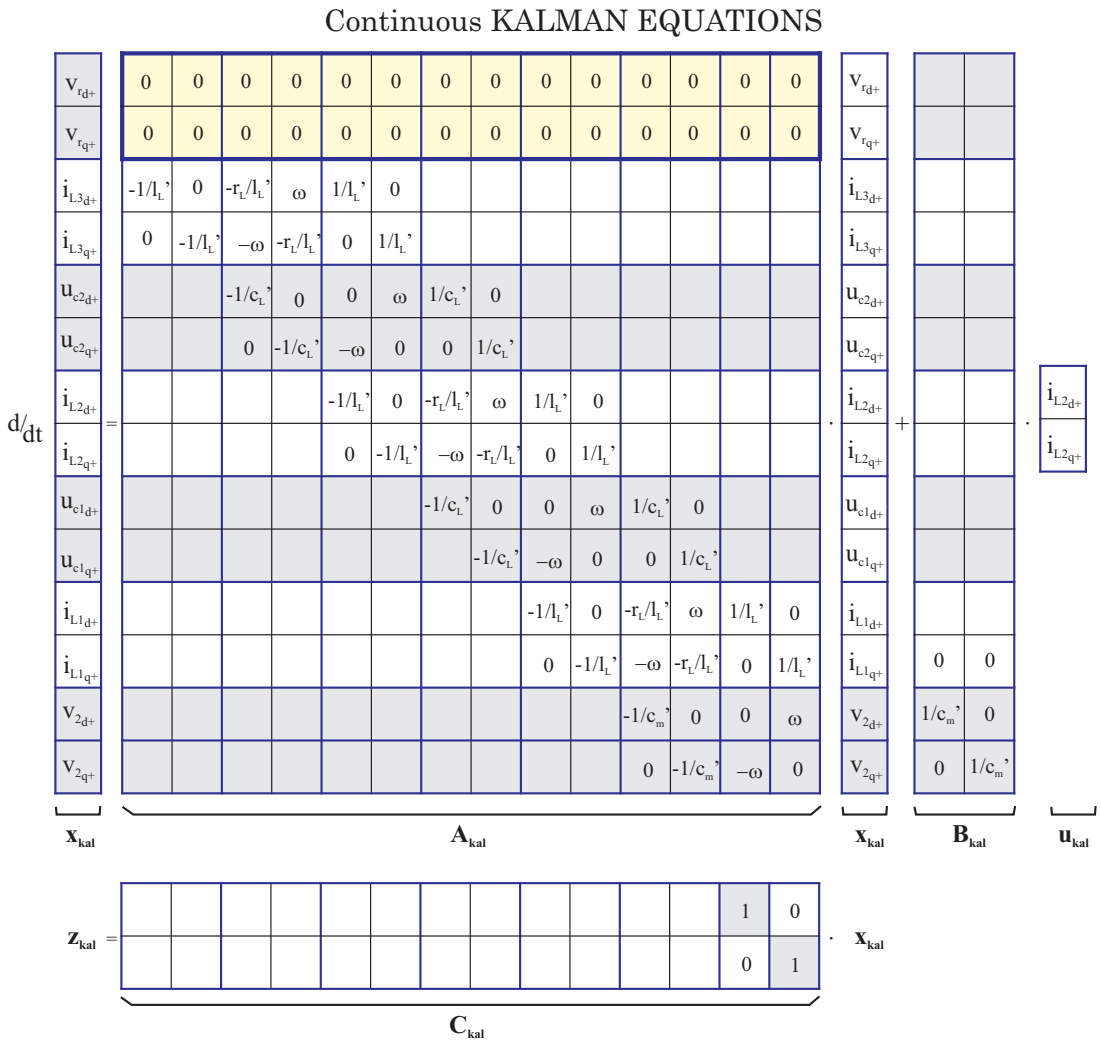


Figure III.4.4: Continuous Kalman equations for the 3 π-section cable (empty cells stand for zeros).

other dynamic behaviour could have been considered.

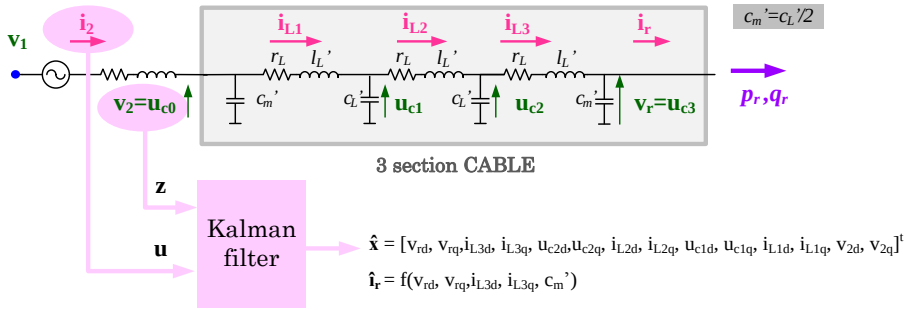


Figure III.4.5: Kalman filter application to the 3 π-section cable.

Once the discretized matrices **F**, **G**, and **H** are obtained, it is just necessary to estimate the process and measurent error covariance matrices, **Q** and **R**, respectively. The convergence

speed of the filter is defined by the measurement noise and process noise.

2.2. Results

The performance of the observer is verified by simulating three types of deviations from nominal conditions:

- **In the first case** a step change of $\mathbf{v_r}$ is simulated while the reference of $\mathbf{i_r}$ is being followed. The objective of this trial is to check that the proposed Kalman filter is able to observe $\mathbf{v_r}$ and $\mathbf{i_r}$ even when they are changing.
- **In the second case** the measures of $\mathbf{v_2}$ and $\mathbf{i_2}$ are assumed to be noisy. In this case, the reference of $\mathbf{i_r}$ is also being tracked.
- **In the third case**, parametrical deviations in the cable parameters are assumed.

In all these simulations the controlled objectives, p_r and q_r, change their reference in steps emulating a nominal operation.

2.2.1. Changes in $\mathbf{v_r}$

In this test the voltage at the receiving-end suffers a sudden drop of 0.05%. As shown in Fig.III.4.6, the Kalman filter is able to estimate this jump with a small delay ($< 1\ ms$). Also, in the transition instants of the voltage drop the receiving-end currents suffer a steep spike that the filter cannot follow. However this occurs only during a very short time.

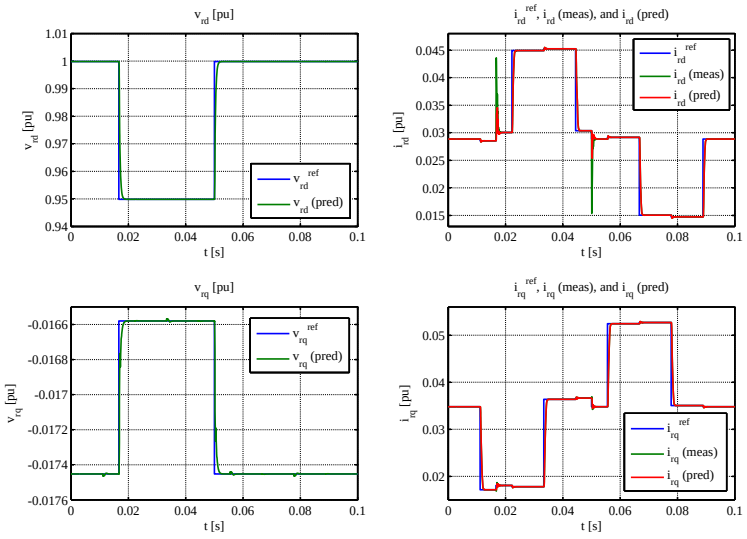


Figure III.4.6: Measured and predicted values of $\mathbf{v_r}$ and $\mathbf{i_r}$ when $\mathbf{v_r}$ changes.

2.2.2. Measuring noise in $\mathbf{v_2}$ and $\mathbf{i_2}$

In this test, the measurement signals used by the Kalman filter to estimate the receiving-end voltage and current values are polluted by a gaussian noise. The variance of the measurement noise is assumed to be $\sigma_{noise} = E[(x - E(x))^2] = 1 \cdot 10^{-4}$. As it can be observed in Fig.III.4.6, the predictions made by the Kalman filter are slightly polluted by noise but the variance of this noise is kept low (smaller than $1 \cdot 10^{-6}$).

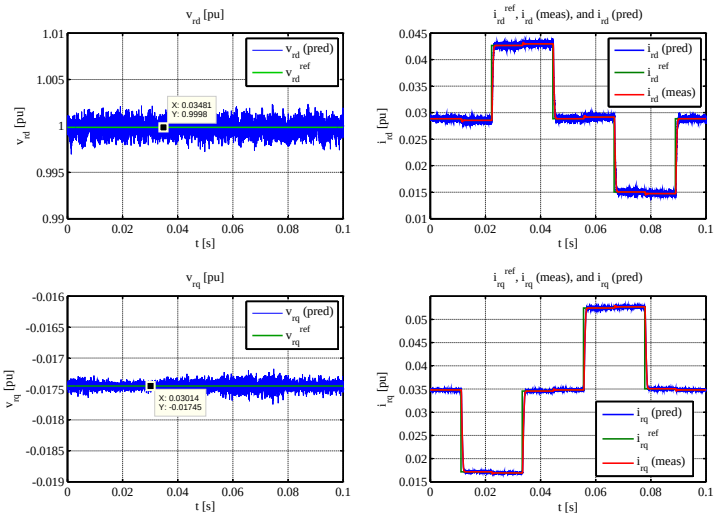


Figure III.4.7: Measured and predicted values of $\mathbf{v_r}$ and $\mathbf{i_r}$ when the measures are polluted with a $\sigma = 1 \cdot 10^{-4}$ noise.

The measurement error covariance matrix ($\mathbf{R}$) must be adjusted according to the estimated measurement noise. In some cases, the measurement noise may change during time but, in many cases, it is possible to estimate the magnitude of the measurement noise offline.

2.2.3. Parametrical changes in cable parameters

The last trial is to verify that the Kalman filter can estimate the receiving-end values even when the parameters of the cable are not perfectly known. For the present study, all the cable parameters have been considered to suffer the same percentage of variation. After several simulations with different variation percentages the following conclusions can be drawn:

(i) A parameter variation of the cable implies a constant prediction error in all the variables except for $\mathbf{v_r}$, where the error is variable, as shown in Fig.III.4.8. Logically, the higher the parameter variation is, the higher the prediction error will be. For parametrical changes in the range of $\pm 20\%$, the prediction errors are acceptable, as it is observed in Table III.4.2. It can also be commented that the estimation errors in $\mathbf{v_r}$ are higher than in $\mathbf{i_r}$, specially at the peaks. For parametrical changes above $\pm 20\%$ the estimation error begins to be unacceptable.

Table III.4.2: Prediction errors due to parametrical errors (considering nominal $p_r - q_r$ profile)

Parametrical error [%]	Maximum prediction error [%]			
	v_{rd}	v_{rq}	i_{rd}	i_{rq}
+20%	0.3%	24.6%	0.7%	7%
−20%	0.3%	38.2%	0.1%	5%

(ii) A parametrical error in the capacitance of the last cell, or a prediction error in $\mathbf{v_r}$, influences the calculation of the reference, that will deviate from the adequate value according to equation III.4.13.

(iii) Closed-loop simulations with the Kalman filter have shown that, for parametrical deviations in the range of ±20%, there are prediction errors but the control does not loose stability.

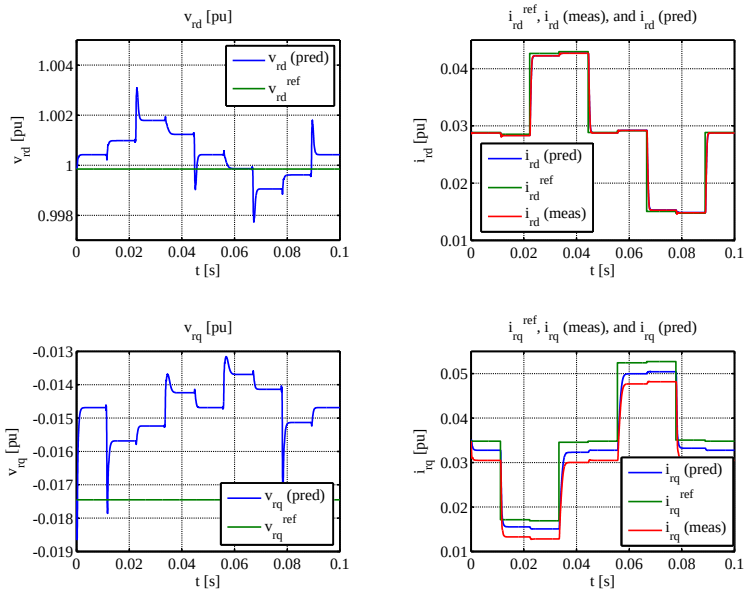


Figure III.4.8: Measured and predicted values of $\mathbf{v_r}$ and $\mathbf{i_r}$ with a parametrical error of +20%.

3. Conclusions

In this chapter a control strategy, based on a global trajectory generation and Lyapunov-based controllers, has been proposed for the series-side of the UPLC when connected to a 3 π-sections cable. This control philosophy can also be applied to a higher number of cable cells provided that sufficiently high controller gains can be chosen. The performance of the control has been successfully tested in simulations where the converters are modelled as ideal voltage sources. Simulation results present a good tracking behaviour even in presence of voltage sags, unbalances, and parametrical uncertainties.

The only limitation of the proposed method is the impossibility of selecting arbitrarily high values of the controller gains. For low sampling and switching frequencies, or for a high number of cable cells, it may not be possible to select sufficiently high gain values.

Additionally, it is also necessary to estimate the states of the cable for a practical implementation of the proposed control structure. The states of the cable have been estimated by means of a Kalman filter. After a set of open- and closed-loop simulations that include the Kalman filter, the following conclusions can be extracted:

- The predictions provided by the Kalman filter can follow step changes of $\mathbf{v_r}$ and $\mathbf{i_r}$ without error. The time constant is small, around $\tau = 1\ ms$.
- The Kalman filter can predict $\mathbf{v_r}$ and $\mathbf{i_r}$ even when the measurements, $\mathbf{v_2}$ and $\mathbf{i_2}$ are noisy. The only difficulty is to estimate the variance of the measurement noise.
- The Kalman filter presents static prediction errors when the cable parameters are not precisely known but, if the errors are in the $\pm 20\%$ range, the closed-loop control is stable.
- Since $\mathbf{i_r}$ is calculated according to equation (III.4.13), the value of $\mathbf{i_r}^{ref}$ is not correct when there are parametrical errors in c'_m or prediction errors in $\mathbf{v_r}$.

As demonstrated by simulations, the Kalman filter is sensitive to uncertainties of the system parameters. In order to overcome this difficulty and enhance the capabilities of classical observers, some authors [126] have proposed advanced state controllers such as high-gain controllers [115], sliding-mode controllers [127], and nonlinear extended state observers [128]. The design and application of advanced controllers is left for future work.

Chapter III.5

UPFC control strategy under unbalanced voltages

In the preceding chapters, the control of a UPLC under balanced conditions has been addressed. However, in distribution grids, the unbalance level is higher than at transmission level due to the proximity and higher density of nonlinear loads, and due to weaker connection points.

When unbalances occur, an interesting subject of reflection is how the device should behave and how this unbalance impacts the control and the performance of the apparatus. In the first two sections of this chapter these two aspects are discussed:

- The **first section** describes the implications of unbalanced voltages and currents on SRF projections and on powers. Indeed, unbalances induce second order oscillations on both SRF projections and on powers. The analytical expressions that explain this effect are therefore provided.
- The **second section** discusses different strategies that could be followed to generate the references. In general, two possibilities are highlighted: to generate the references to obtain constant active and reactive powers at a chosen point, or to generate balanced currents.

Then, once the objectives are clear, it is necessary to decide the control structure that will be used. As for other applications, two structure families can be used: **(i) vector-oriented structures**, and **(ii) scalar structures**. These control structures have already been proposed for the shunt-side converter control under unbalances. For this reason, in the **third section** these control structures, that are applied to the shunt converter, are simulated and compared. As a conclusion, it is observed that the compared vector-oriented strategies (the one oriented to SRFs (LIPO), and the one that separates the symmetrical sequences (DVCC)) are equivalent if the sequence extracting techniques are ideal and if adequate control laws are selected. Additionally, it is also highlighted the necessity of developping a method to estimate the oscillating active power references that must be provided to the shunt reference block.

In the **fourth section** the limitations of the controllers proposed in chapters III.3 and III.4 are demonstrated when a single positive SRF is used and when unbalances are present. These limitations are related to the need of increasing the controller gains while operating in a discrete environment. It is shown that it is only possible to increase the controller gains if the sampling times are reduced and the controllers are represented with a continuous model.

Finally, in the **fifth section** a dual sequence-based control structure is proposed, which is suitable to be used with the controllers proposed in chapters III.3 and III.4. The good performance of this structure under unbalances is proven in simulations that include a three-section cable. It must be mentioned that the dual sequence control structure is extremely dependent on the type of the sequence extractors used. In this chapter the concept of using a dual sequence control structure with a cable is validated assuming ideal conditions, this is, ideal converters and ideal sequence extractors. However, in order to complement the present chapter, in the next chapter some sequence extracting techniques are evaluated in order to assess the suitability of DVCC technique when used with real sequence extracting techniques.

1. On the implications of voltage unbalances on SRF projections and on powers

When the grid voltages and currents are balanced, the use of a single SRF provides a satisfactory performance, as demonstrated in Chapter III.3. In such case, the tracked references are constant, as the projections of the voltages and currents in the SRFs (dq axes) are.

When the grid voltages are unbalanced, the tracked references may not be constant anymore. The nature of the references is different depending on the objective that is to be minimized. Knowing that unbalanced voltages and currents can generate oscillating power components, in some cases it may be prefered to guarantee constant powers (which does not imply balanced currents). In other cases, balanced currents may be prioritized. The decision is left upon the system operator.

In order to clarify these concepts, an illustrative example is shown in Fig.III.5.1. In the left hand-side of the figure a vector diagram is presented where a generic phasor, $\mathbf{x}(t)$, is depicted. This phasor can be decomposed into a positive sequence phasor, $\mathbf{x}^{+}(t)$, that rotates in the anti-clockwise direction, and a negative sequence phasor, $\mathbf{x}^{-}(t)$, that rotates in the clockwise direction. The geometric sum of the positive and the negative phasor yields the generic phasor $\mathbf{x}(t)$. If the phasor $\mathbf{x}(t)$ is projected into the axis of the positive-sequence phasor (or either into the negative-sequence phasor axis), a second-order harmonic is observed in the $d^{+}q^{+}$ axes, as represented in Fig.III.5.1(b). This example helps understanding what happens when a single SRF is used and unbalanced voltages (or harmonics) occur.

But, when negative sequence voltages and currents occur, it is not only the $d^{+}q^{+}$ projections that oscillate, unbalances also affect the expression of powers. As it can be observed in equation (III.5.1), the expression of power is divided into constant terms ($\bar{\mathbf{s}}$), and alternating terms ($\tilde{\mathbf{s}}$). If the unbalances are fundamental [1], then the alternating power components will

1. when used with sequences, the term fundamental means that the sequence turns at the same frequency as the fundamental grid frequency

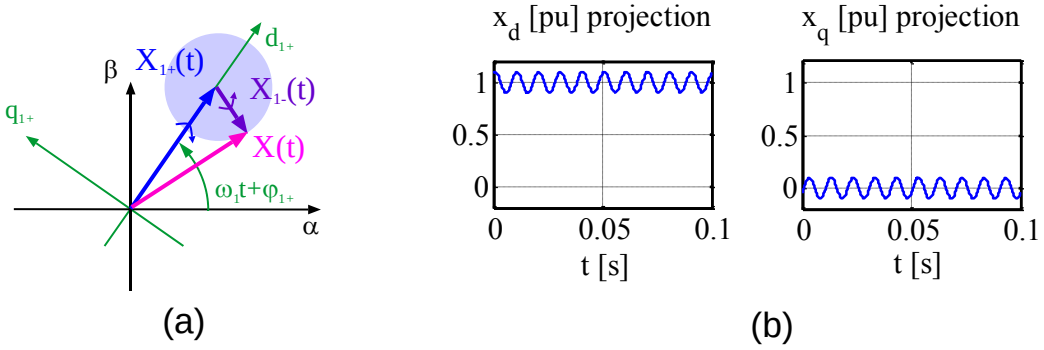


Figure III.5.1: (a) Example of a positive SRF with an unbalanced vector in the $\alpha\beta$ frame (b) Phasor projections in the d and q axis.

oscillate at double the fundamental frequency.

$$\begin{aligned}\mathbf{s}(t) &= p(t) + \mathbf{j}q(t) = \mathbf{v}(t)\cdot\mathbf{i}(t)^* \\ &= \left[\mathbf{v_{(1+)}}\cdot e^{j\omega_1 t} + \mathbf{v_{(1-)}}\cdot e^{-j\omega_1 t}\right]\cdot\left[\mathbf{i_{(1+)}}\cdot e^{j\omega_1 t} + \mathbf{i_{(1-)}}\cdot e^{-j\omega_1 t}\right]^* \\ &= \left[\mathbf{v_{(1+)}}\cdot\mathbf{i_{(1+)}} + \mathbf{v_{(1-)}}\cdot\mathbf{i_{(1-)}}\right] + \left[\mathbf{v_{(1+)}}\cdot\mathbf{i_{(1-)}}\cdot e^{j2\omega_1 t} + \mathbf{v_{(1-)}}\cdot\mathbf{i_{(1+)}}\cdot e^{-j2\omega_1 t}\right] \\ &= \bar{\mathbf{s}} + \tilde{\mathbf{s}}\end{aligned} \tag{III.5.1}$$

where $\mathbf{v_{(1+)}} = v_{d(1+)} + jv_{q(1+)}$, $\mathbf{v_{(1-)}} = v_{d(1-)} + jv_{q(1-)}$, $\mathbf{i_{(1+)}} = i_{d(1+)} + ji_{q(1+)}$, and $\mathbf{i_{(1-)}} = i_{d(1-)} + ji_{q(1-)}$.

The expressions of powers (p and q), that are deduced in appendix B, are composed of a constant term and two oscillating terms: a cosinusoidal term, and a sinusoidal term.

$$\begin{aligned}p(t) &= \bar{p} + \tilde{p}_{2\omega} = \bar{p} + p_{c2}\cdot\cos(2\omega t) + p_{s2}\cdot\sin(2\omega t) \\ q(t) &= \bar{q} + \tilde{q}_{2\omega} = \bar{q} + q_{c2}\cdot\cos(2\omega t) + q_{s2}\cdot\sin(2\omega t)\end{aligned} \tag{III.5.2}$$

where ω stands for the fundamental grid frequency.

The expressions of $\bar{p}$, p_{c2}, p_{s2} are defined as

$$\begin{bmatrix}\bar{p}\\ p_{c2}\\ p_{s2}\end{bmatrix} = \begin{bmatrix} v_{d_{(1+)}} & +v_{q_{(1+)}} & +v_{d_{(1-)}} & +v_{q_{(1-)}} \\ v_{d_{(1-)}} & +v_{q_{(1-)}} & +v_{d_{(1+)}} & +v_{q_{(1+)}} \\ v_{q_{(1-)}} & -v_{d_{(1-)}} & -v_{q_{(1+)}} & +v_{d_{(1+)}}\end{bmatrix}\cdot\begin{bmatrix} i_{d_{(1+)}}\\ i_{q_{(1+)}}\\ i_{d_{(1-)}}\\ i_{q_{(1-)}}\end{bmatrix} \tag{III.5.3}$$

and the expressions of $\bar{q}$, q_{c2}, and q_{s2} are defined as

$$\begin{bmatrix}\bar{q}\\ q_{c2}\\ q_{s2}\end{bmatrix} = \begin{bmatrix} v_{q_{(1+)}} & -v_{d_{(1+)}} & +v_{q_{(1-)}} & -v_{d_{(1-)}} \\ v_{q_{(1-)}} & -v_{d_{(1-)}} & +v_{q_{(1+)}} & -v_{d_{(1+)}} \\ -v_{d_{(1-)}} & -v_{q_{(1-)}} & +v_{d_{(1+)}} & +v_{q_{(1+)}}\end{bmatrix}\cdot\begin{bmatrix} i_{d_{(1+)}}\\ i_{q_{(1+)}}\\ i_{d_{(1-)}}\\ i_{q_{(1-)}}\end{bmatrix} \tag{III.5.4}$$

2. The impact of the voltage unbalance location on the UPLC and the selected objectives

Considering that negative sequences produce fluctuating terms in powers and in SRF projections, the presence of a negative sequence voltage has a different implication in the UPLC depending on the location of the unbalance. Voltage unbalances can occur at $\mathbf{v_1}$ (Fig.III.5.2), at $\mathbf{v_r}$ (Fig.III.5.4), or at both.

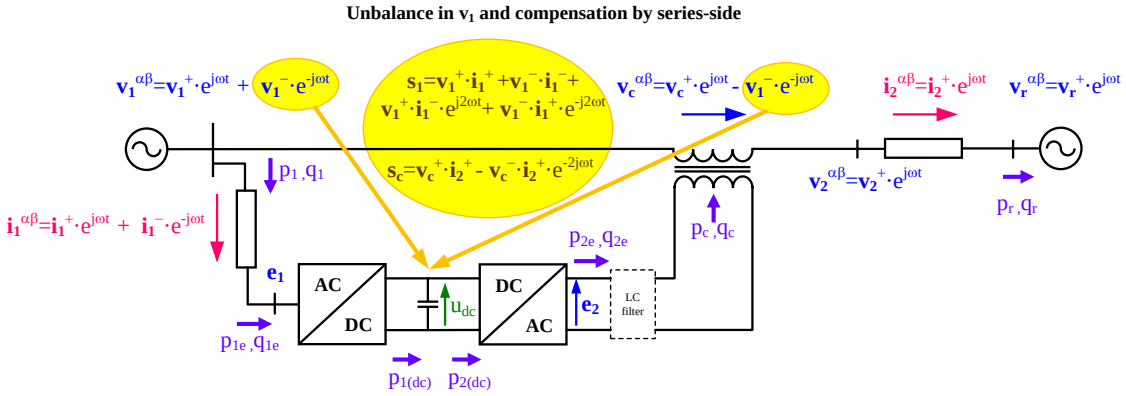


Figure III.5.2: Schematic view on a single-phase diagram of variables under an unbalance in $\mathbf{v_1}$.

2.1. Impact of unbalances at v_1

If the unbalance occurs at $\mathbf{v_1}$, and assuming that the series compensator completely compensates for it, as shown in Fig.III.5.2, the unbalance will *doubly* impact the DC-link voltage. On the one hand, the unbalance at $\mathbf{v_1}$ will generate an active power ripple at double the fundamental frequency component at the shunt-converter. On the other hand, the series compensator will try to compensate for the unbalance generated in $\mathbf{v_1}$ and will inject the same amount of unbalance to the grid. Since the series-side compensator compensates for the voltage unbalance, the line currents will keep balanced. This means that the series-side converter will also suffer from an oscillating active power component. As a result of the alternating active powers at both sides of the DC-link, the DC voltage will fluctuate according to expression

$$\begin{aligned} \dot{u_{dc}}^2 &= \frac{2}{c'_{dc}}\left[p_{1e} - p_{2e}\right] \approx \frac{2}{c'_{dc}}\left[p_1 - p_c\right] \\ \dot{u_{dc}}^2 &\approx \frac{2}{c'_{dc}}\left[(\bar{p}_1 - \bar{p}_c) + (p_{1_{(c2)}} - p_{c_{(c2)}}) \cdot \cos(2\omega_1 t) + (p_{1_{(s2)}} - p_{c_{(s2)}}) \cdot \sin(2\omega_1 t)\right] \end{aligned} \tag{III.5.5}$$

where, for simplicity, the power losses due to series- and shunt-side filters have been neglected.

For the shunt-side converter, two strategies are possible regarding active power transfer [29]: (a) to keep a constant DC-link voltage reducing voltage oscillations as much as possible, or (b) to maximize the exchanged power. In this case, the first option is preferable because the series-side converter performance depends on it.

In respect of the shunt-side reactive power, the reactive power could be used to keep the voltage level at the positive-sequence reference values compensating for the unbalance in $\mathbf{v_1}$. This option would solve, in a great manner, the problems derived by unbalances in $\mathbf{v_1}$. Nevertheless, this feature can only be used if the the dimensions of the apparatus enable it (which depends of the strength of the grid at the connection point and the source of the unbalance). This option has not been addressed in this work considering that, if the UPLC is connected close to the HV/MV substation the required size of the apparatus would be unreasonable. However, the study for cases where the UPLC is placed in weaker points and nearer from polluting loads is left for future work.

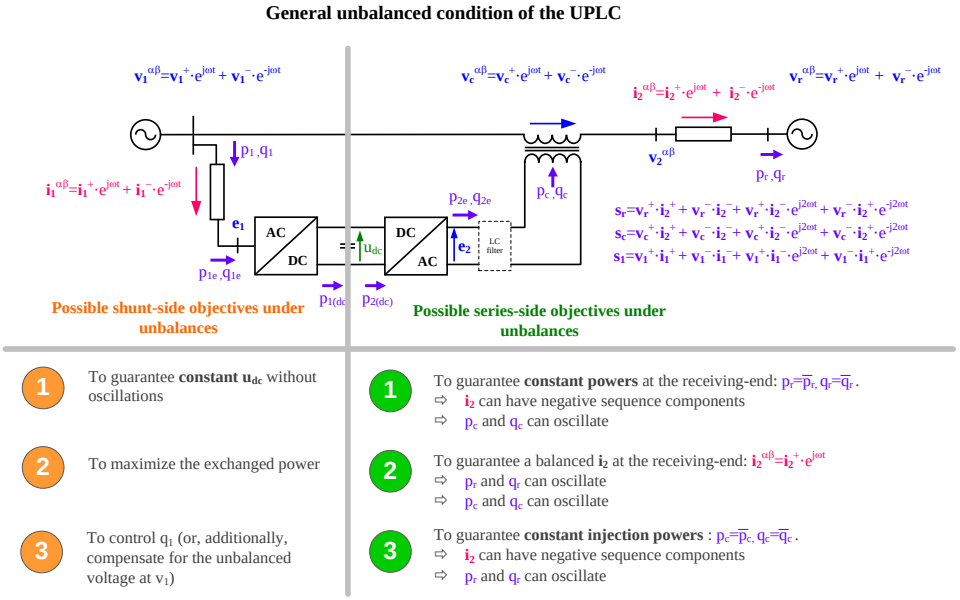


Figure III.5.3: Review of possible objectives under unbalanced conditions.

2.2. Impact of unbalances at v_r

If the unbalance occurs at $\mathbf{v_r}$, it is first necessary to review the receiving-end current reference calculation strategy. Fig.III.5.3 and Fig.III.5.4 depicts the most general unbalanced case (with no harmonics) with a proposal of possible objectives that could be controlled. According to the proposed list, it is not possible to obtain a globally optimal solution since there will always be aspects that are not possible to improve.

For the series-side, three possible approaches are proposed.

- The **first approach** consists in guaranteing constant powers, without any oscillations, at the receiving-end. This approach implies that line currents may not be balanced (this depends on whether $\mathbf{v_r}$ is balanced or not) and that series injected powers will also oscillate. If series injected powers oscillate, they will induce an oscillating component in the DC bus.

If a single SRF is used, the current references can be calculated using

$$\begin{bmatrix} i_d \\ i_q \end{bmatrix}^{ref} = \begin{bmatrix} v_d & +v_q \\ v_q & -v_d \end{bmatrix}^{-1} \cdot \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} \tag{III.5.6}$$

And, if the voltage sequences are available, the reference current sequences can be calculated using

$$\begin{bmatrix} i_{d_{(1+)}} \\ i_{q_{(1+)}} \\ i_{d_{(1-)}} \\ i_{q_{(1-)}} \end{bmatrix}^{ref} = \begin{bmatrix} v_{d_{(1+)}} & +v_{q_{(1+)}} & +v_{d_{(1-)}} & +v_{q_{(1-)}} \\ v_{q_{(1+)}} & -v_{d_{(1+)}} & +v_{q_{(1-)}} & -v_{d_{(1-)}} \\ v_{d_{(1-)}} & +v_{q_{(1-)}} & +v_{d_{(1+)}} & +v_{q_{(1+)}} \\ v_{q11-)} & -v_{d_{(1-)}} & -v_{q_{(1+)}} & +v_{d_{(1+)}} \end{bmatrix}^{-1} \cdot \begin{bmatrix} \bar{p} \\ \bar{q} \\ p_{c2} \\ p_{s2} \end{bmatrix} \tag{III.5.7}$$

where the oscillating powers are considered zero: $p_{1(c2)} = 0$ and $p_{1(s2)} = 0$.

- The **second approach** consists in establishing balanced line currents. This choice implies that, if $\mathbf{v_r}$ is unbalanced, receiving-end powers will oscillate. As in the previous case, series injected powers will oscillate, provoking second harmonic oscillations in the DC-link voltage. This approach also requires symmetrical sequence extractors for line current reference calculation. These references can be calculated using

$$\begin{bmatrix} i_{d_{(1+)}} \\ i_{q_{(1+)}} \end{bmatrix}^{ref} = \begin{bmatrix} v_{d_{(1+)}} & +v_{q_{(1+)}} \\ +v_{q_{(1-)}} & -v_{d_{(1-)}} \end{bmatrix}^{-1} \cdot \begin{bmatrix} \bar{p} \\ \bar{q} \end{bmatrix} \quad and \quad \begin{bmatrix} i_{d_{(1-)}} \\ i_{q_{(1-)}} \end{bmatrix}^{ref} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \tag{III.5.8}$$

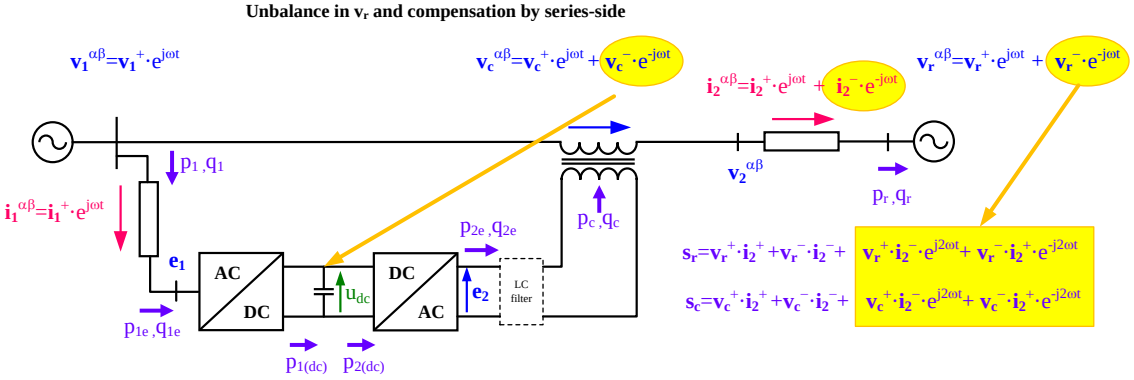


Figure III.5.4: Schematic view on a single-phase diagram of variables under an unbalance in $\mathbf{v_r}$.

- The **third approach** consists in forcing the series-injected powers to have constant values. In this way, no oscillation will be induced in the DC-link. The shortcoming of this method lies in the difficulty of calculating the line current reference signals.

In some of these cases, the positive and negative sequences of voltages and currents are needed for the current reference calculation. These sequences must be calculated by means of a sequence extractor.

3. Existing solutions for the shunt-side control under unbalances

Dealing with unbalanced voltages is not an easy task. Until now, this problem has not been addressed for UPFCs or SSSCs (probably because the unbalance level at transmission level is usually low), but some work exists on shunt-connected devices such as STATCOMs, active power filters, electrical drives, and HVDCs [29, 30, 31, 32, 33]. In these works, the problem of unbalances is addressed from the shunt-side converter point of view, as illustrated in Fig.III.5.5. And, generally, the active power demanded at the opposite side, $p_{2(dc)}$, is considered constant.

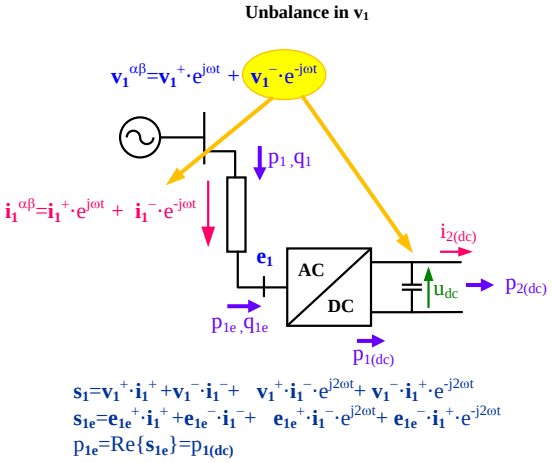


Figure III.5.5: Case studied in existing publications regarding voltage unbalances.

Among the evaluated works, two main approaches are observed: (i) vector-oriented strategies, and (ii) scalar strategies.

3.1. Vector-oriented strategies

Vector-oriented strategies are probably the most common control strategies used to deal with unbalances. Also inside this category, two families of methods can be considered: (a) strategies that project voltage and current values into SRFs, and (ii) strategies that deal with positive and negative sequences independently. Both techniques present advantages and disadvantages.

3.1.1. Strategies that project voltage and current values into SRFs

This family of methods uses one or two SRFs (positive and negative), to where all the voltage and current values are refered [34, 30, 29]. When the system voltages and currents are completely balanced, the projections of voltages and currents in the SRFs are constant values. Likewise, the tracked current references are also constant values. In this case, the classical vector control oriented to the positive SRF (using the popular PI controllers, for example) is

enough. However, when voltage unbalances or harmonics occur, the values projected into the SRFs contain oscillating components and it may also be necessary to track oscillating current references.

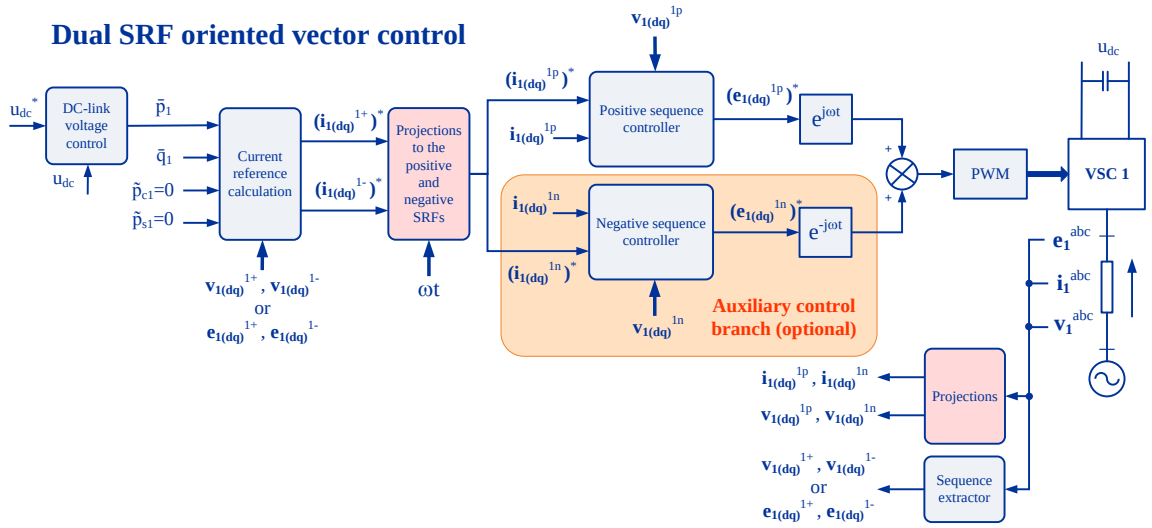


Figure III.5.6: Dual control structure using positive and negative frame projections (from [30]).

In Fig.III.5.6, for example, the control structure proposed in [30] is presented. In the figure bold variables stand for vectors (e.g $\mathbf{x_{(dq)}} = x_d + \mathbf{j}x_q$), $\mathbf{x}^{1+}$ and $\mathbf{x}^{1-}$ are the positive- and negative-sequence vectors, and $\mathbf{x}^{1p}$ and $\mathbf{x}^{1n}$ are the phasor projections into the positive and the negative SRFs, respectively:

$$\begin{aligned}\mathbf{x}_{(\alpha\beta)} &= \mathbf{x_{dq}}^{1+} \cdot e^{j\omega_1 t} + \mathbf{x_{dq}}^{1-} \cdot e^{-j\omega_1 t} \\ &= e^{j\omega_1 t}\left[\mathbf{x_{dq}}^{1+} + \mathbf{x_{dq}}^{1-} \cdot e^{-j2\omega_1 t}\right] = e^{j\omega_1 t} \cdot \mathbf{x_{dq}}^{1p} \\ &= e^{-j\omega_1 t}\left[\mathbf{x_{dq}}^{1+} \cdot e^{j2\omega_1 t} + \mathbf{x_{dq}}^{1-}\right] = e^{-j\omega_1 t} \cdot \mathbf{x_{dq}}^{1n}\end{aligned} \tag{III.5.9}$$

As it can be observed, this control structure is just an adaptation of the classical single positive SRF oriented control. The difference lies in three main points:

i) **The reference calculation block.** In the proposed structure the reference calculation method of equation (III.5.7), where the oscillating active powers are set to zero, is selected. Nevertheless, it would be also possible to choose equation III.5.6, which does not require any voltage sequence calculation.

ii) **An auxiliary control loop.** Besides the main positive control loop, [30] proposes the use of an auxiliary control loop oriented to the negative SRF. However, in [29] this additional loop is not considered necessary.

iii) **The type of controller.** When using this type of control structure, the controllers should be able to track oscillating current references. In [30] and [29], for example, an association of a PI controller and a resonant term ($C(s) = PI(s) + R(s)$) is proposed.

$R(s)$ can be defined as

$$R(s) = \frac{k_r}{s^2 + {\omega_r}^2} \qquad or \qquad R(s) = \frac{k_r s}{s^2/{\omega_r}^2 + s/(Q_f \omega_r) + 1} \tag{III.5.10}$$

where k_r is the resonant gain, ω_r is the resonating frequency (usually $\omega_r = 2 \cdot \omega_1$), and Q_f is the quality factor of the filter. The main disadvantage of using resonant controllers is that it is necessary to make them frequency-adaptive in order to operate in weak networks. Nevertheless, any other control structure suitable to track oscillating signals could also be used. Without looking too far, the controllers of the form $C(e) = k_1 + k_2 \cdot sgn(e)$ proposed in the preceeding chapters, are capable of tracking oscillating signals. However, as it will be shown shortly, this method presents some limitations.

As it can be observed in Fig.III.5.6, this control structure just needs the extraction of the symmetrical sequences of the voltage for the reference calculation block (and not in the feedback loops). And, if equation equation III.5.6 is used, no sequence needs to be extracted. This fact constitutes a substantial advantage comparing to the strategy that is presented next, where the voltage and current symmetrical sequence components are needed all along the control process.

3.1.2. Strategies that deal with positive and negative sequences independently

The preceeding strategy requires controllers that are able to track oscillating signals and thus, that have a high bandwidth. An alternative solution to this shortcoming is to separate the voltage and current signals into positive and negative sequences (assuming that there are not harmonics or homopolar components) and deal with them independently, as shown in Fig.III.5.7. This method, that has been proposed in [31, 33], requires fast and reliable sequence extractors. In [31], for example, notch filters are used in order to extract the negative oscillating component from the positive SRF projections. Since the time constant of notch filters exceeds one grid period, they are not well adapted for transient conditions. In [29], the Delay Signal Cancellation (DSC) technique is proposed due to the very low delay time that this extraction technique presents. However, as it will be discussed in the next chapter, the DSC technique offers some disadvantages.

3.2. Scalar strategies

Scalar control strategies like the one shown in Fig.III.5.8 constitute an alternative method for controlling converter currents without the necessity of using phasors. As it can be observed in Fig.III.5.8, in order to calculate the current references in the *abc* frame, it is necessary to establish a desired power factor (φ_{pf}), to measure the phase-angles of the grid-voltages (ϕ_{abc}), and to estimate their respective magnitudes by a disturbance identification block. The use of single-phase synchronization methods is, nevertheless, unavoidable.

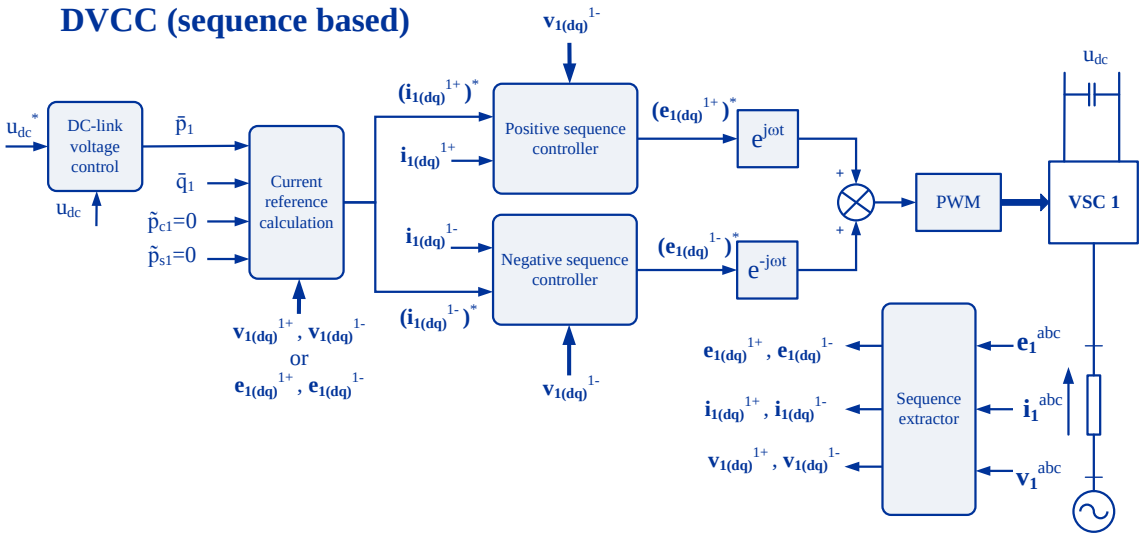


Figure III.5.7: Dual control structure using separate positive and negative sequences (from [31]).

In [29] resonant controllers are proposed for the control, but any other control method that is able to track oscillating signals can be used instead.

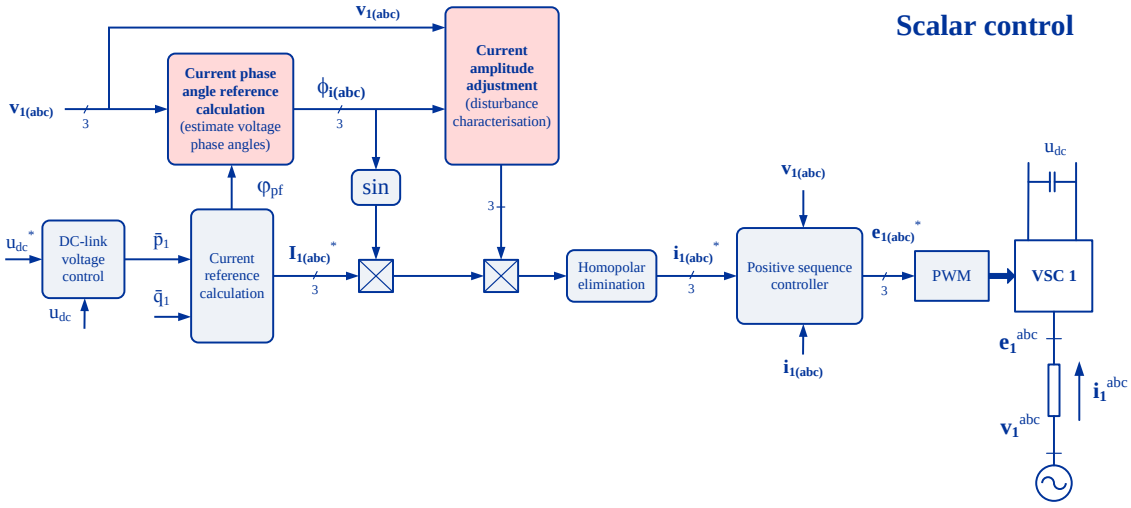


Figure III.5.8: Scalar control structure (from [29]).

3.3. Comparison between unbalance-dealing control approaches

The evaluated control methods present different advantages and disadvantages:

- All of them need some type of **synchronization technique**. This means that, without exceptions, the good performance of these methods depends on the reliability of the used synchronization technique.
- The particular controller structure of each of these categories has not been discussed but,

methods that use the projections of voltages and currents into SRFs, and scalar methods require controllers that have the ability of **tracking alternating signals**. Methods that use separate control loops for each sequence do not need to track alternating signals but they may require to increase the **number of sequence-control loops** if the voltages are significantly polluted with other harmonic orders.

- In particular, methods that rely on sequence extraction techniques tend to be more sensitive due to the inherent delays that sequence extraction techniques introduce. Some of these sequence extraction techniques will be explained and compared in chapter III.6.

In Table III.5.1 a comparison between the presented control techniques is provided.

Table III.5.1: Comparison of control strategies under unbalances

Control structure	Advantages	Disadvantages
Using the projections of v and i on SRFs	• The symmetrical sequences of the voltages are just needed for the current reference calculation (and not always).	• Needs controllers that can **track alternating signals**. • Needs a **synchronization technique** for identifying the position of the SRFs.
Using independent control loops for the positive and negative sequences	• Does not need controllers that can track alternating signals. • Each sequence is independently controlled.	• Needs **sequence extracting techniques**. • Needs as many **sequence control loops** as sequence components exist (if they are reasonably high) in the signal. • Needs a **synchronization technique** for identifying the position of the SRFs.
Using scalar control techniques	• Does not require sequence extraction techniques.	• Needs controllers that can **track alternating signals**. • Needs a **voltage disturbance identification block**. • Needs a **synchronization technique** for identifying the phase-angles of the voltage phases.

In complement to the comparison Table III.5.1 the presented vector-oriented methods have been compared in simulation using *SimPowerSystems* using switching converters ($F_{sw} = 4950\ Hz$ and $T_s = 10\ \mu s$). In these simulations the legend DVCC stands for the sequence separation method used in [31] and the legend LIPO stands for the dual SRF oriented method used in [30]. In all the simulation cases the reference values of q_1 and the perturbation $i_{2(dc)}$ of Fig.III.5.9 have been considered.

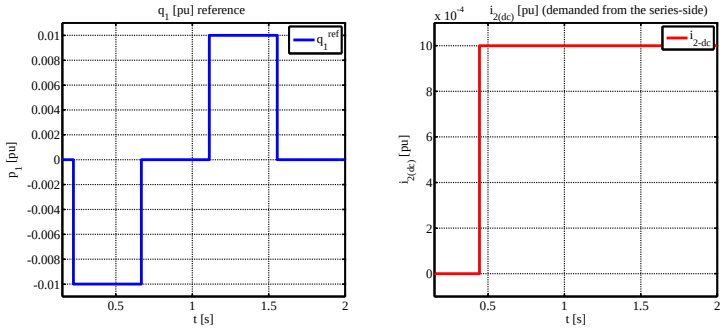


Figure III.5.9: References used in the simulations of Fig.III.5.10.

In Fig.III.5.10, the results of three simulation cases are provided:

- **Case I:** A nominal case where the voltage $\mathbf{v_1}$ is balanced.
- **Case II:** A case where the voltage $\mathbf{v_1}$ suffers a steady-state unbalance of 0.2 pu.
- **Case III:** A case where a voltage sag of type D (with 60° jump) occurs from 0.665s-1.556s. The values that caracterize this type of sag are provided in [129].

After this set of simulations, the following conclusions can be extracted:

- Both vector oriented methods, LIPO and DVCC improve the DC-link voltage oscillations in comparison with the classical positive SRF oriented method presented in chapter III.3.
- These simulations have highlighted the necessity of using a low-pass filter in the input of the current reference calculating block in order to obtain a constant $\bar{p}_1^{ref}$ value. In this case a second-order Butterworth filter has been used.
- When a 0.2 pu steady-state unbalance is present, both methods yield similar results. The higher oscillation levels correspond to changes in reactive power demands. When a type D voltage sag is applied, both methods yield similar results also (the green curves and the cyan curves are overlapped).

As a conclusion, it could be stated that both methods, LIPO and DVCC, are equivalent provided that the voltage and current sequences are instantaneously known and that all the controllers can perfectly track the reference signals.

The main assumption of these control solutions is that the demanded DC power is constant. However, in the case of a UPLC, the series-side converter will always demand/absorb an

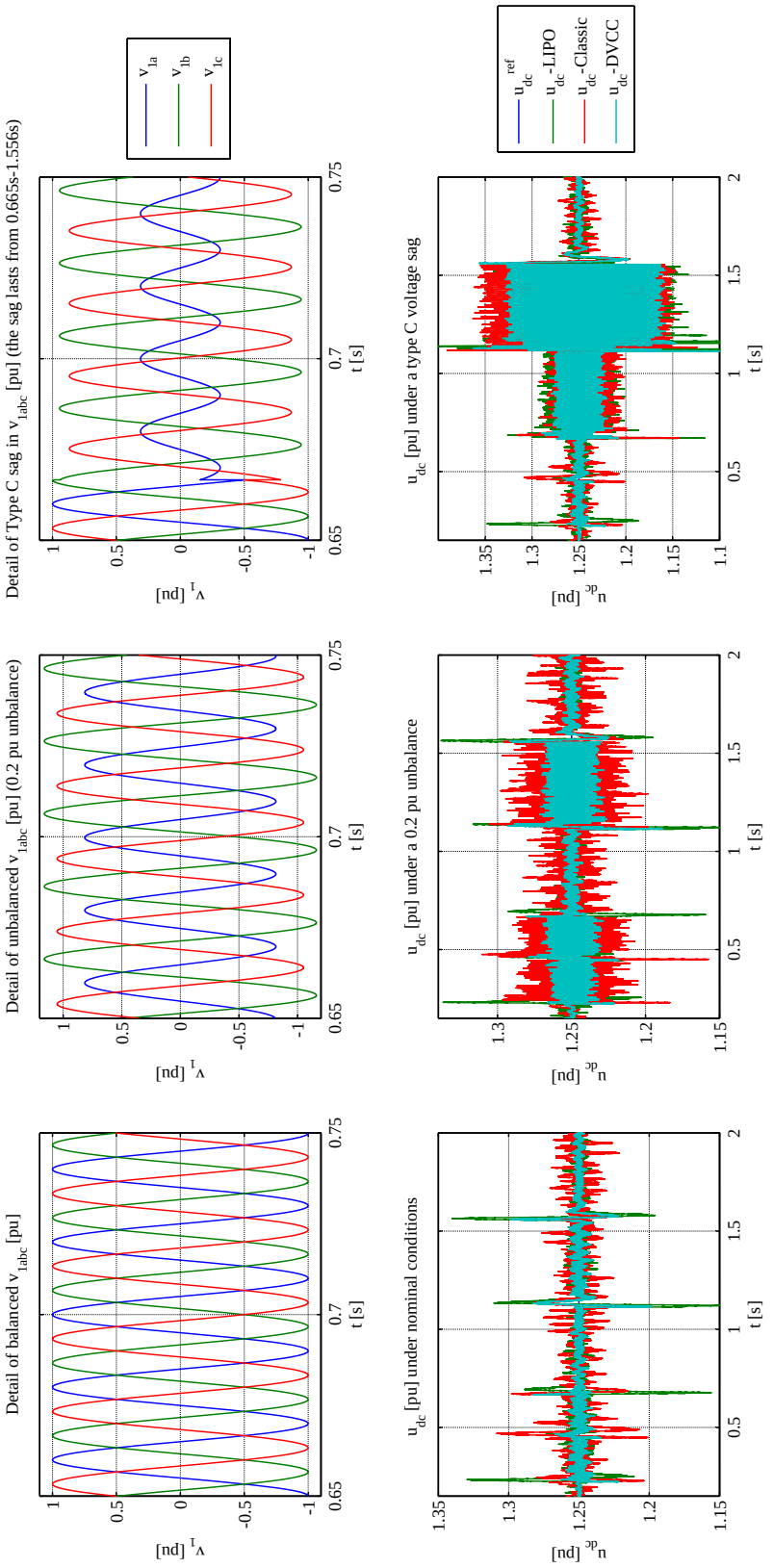


Figure III.5.10: Comparison DC-link voltage under nominal, steady-state unbalances, and unbalanced sags (type D).

oscillating active power when unbalances are present. Then, the proposed solutions will not be totally effective. The proposed solutions can only be effective if it is possible to deduce the oscillating powers at terminal one (${p_{1(s2)}}^{ref}, {p_{1(c2)}}^{ref}$) from the oscillating powers demanded by the series converter ($p_{c(s2)}, p_{c(c2)}$):

$$p_{c(s2)}, p_{c(c2)} \Longrightarrow {p_{1(s2)}}^{ref}, {p_{1(c2)}}^{ref} \tag{III.5.11}$$

The calculation of ${p_{1(s2)}}^{ref}$ and ${p_{1(c2)}}^{ref}$ can be rather difficult, specially during transient states, because it is necessary to identify the power losses of all the UPLC chain. For this reason, in this work, the reference calculation approach presented in equation (III.5.7) has been selected. In this case, the oscillating power references has been fixed to zero (${p_{1(s2)}}^{ref} = 0$ and ${p_{1(c2)}}^{ref} = 0$). However, as it will be observed in the simulations, DC fluctuations can not be totally reduced.

4. Limitations of the proposed controllers when using a positive SRF oriented control structure under unbalanced conditions

Considering that the controllers proposed in chapters III.3 and III.4 can follow oscillating signals, it is legitime to think that the classical control structure presented in Fig.III.5.6, oriented to a single positive SRF, is good enough for the control of the series-side of the UPLC under unbalanced conditions. However, this control structure ($C(e) = k_1 + k_2 \cdot sgn(e)$) presents some practical limitations related to its numerical implementation. The controller gains are limited due to the switching frequency of the converters and to the sampling times.

In order to highlight the limitations of the proposed controllers when using a single positive SRF and unbalanced voltages are present, two sets of simulations have been launched in SimPowerSystems.

- **In the first set of simulations**, the whole UPLC connected to a RL line has been simulated in *SimPowerSystems* including the real converters. In these simulations the references are the ones traced in Fig.III.5.11 and the reference calculating strategy is based on guaranteeing balanced line currents (without negative sequence components).

  Three sub-cases have been evaluated: (i) nominal conditions without unbalances, (ii) a 5% unbalance in $\mathbf{v_1}$, and (iii) a 5% unbalance in $\mathbf{v_r}$.

  In this first set of simulations an interesting phenomenon has been observed: in order to be able to follow the line currents without any oscillations it is necessary to increase the gains of the series-side controllers. The problem here is that it is not practically possible to increase infinitively the gain of the controllers due to the switching limitations mentioned in section 3.3.1..

  The result of the simulation, where the series controller gains have been increased as much as possible (without decreasing the sampling nor the switching times), is presented

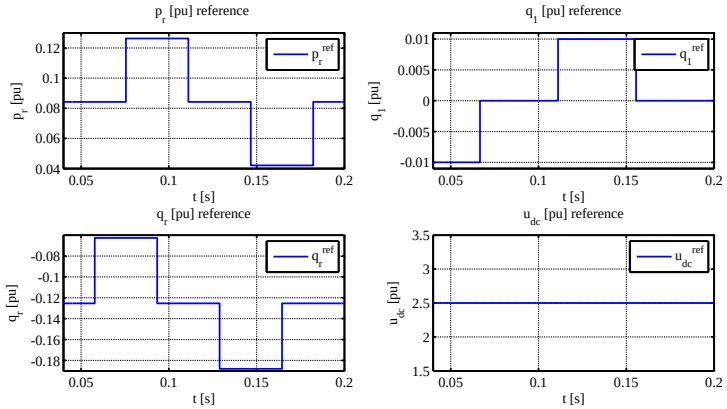


Figure III.5.11: References used for the simulation of unbalances using a positive SRF.

in Fig.III.5.12. As it can be observed, the line current tracks the reference with a pretty high oscillation ($\approx 0.01pu$ peak-to-peak).

- In order to check that, in an ideal case (without converter switchings and with very small sampling times) the controller gains could be further highered and the current references could be perfectly tracked, a **second set of simulations** has been launched in *SimPowerSystems*. In this set of simulations the series-side converter is ideal (but not the shunt), and the sampling times have been lowered. Certainly, the use of an ideal converter enables increasing the series-controller gains such that a perfect tracking is obtained, as reproduced in Fig.III.5.13.

  When a cable is connected to the UPLC, the same phenonomenon is observed with the difference that, the sampling times need to be much smaller than in the case of an RL line.

The above-presented examples allow extracting the following conclusion:

When voltage unbalances are present, and a single positive-sequence-oriented SRF is used, the proposed controllers can theoretically track the reference line currents without oscillations. However, in order to do so, the series controller gains need to be further increased. Due to switching devices and the discrete nature of computations, it is not always possible to increase infinitely the series controller gains. For this reason, in a real simulation that considers the commmutation of the series converter it is not always possible to guarantee a perfect tracking under unbalances.

In the next section it will be demonstrated that, using the same controllers, a control structure that deals with positive and negative sequence components separately can guarantee a perfect tracking of the series-side reference signals (even in the case of a cable).

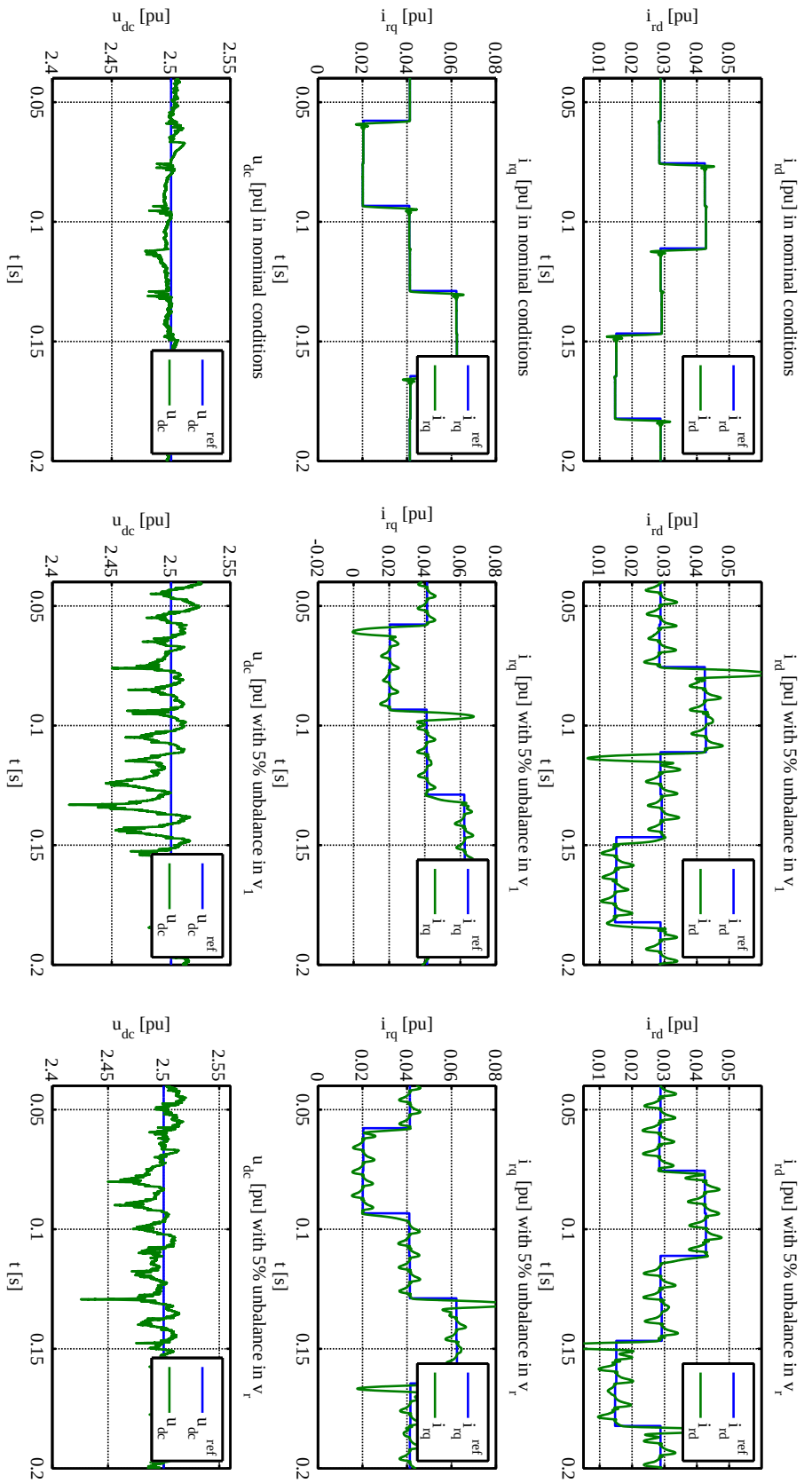


Figure III.5.12: Comparison of line currents and DC-link voltage under nominal and unbalanced conditions (first example).

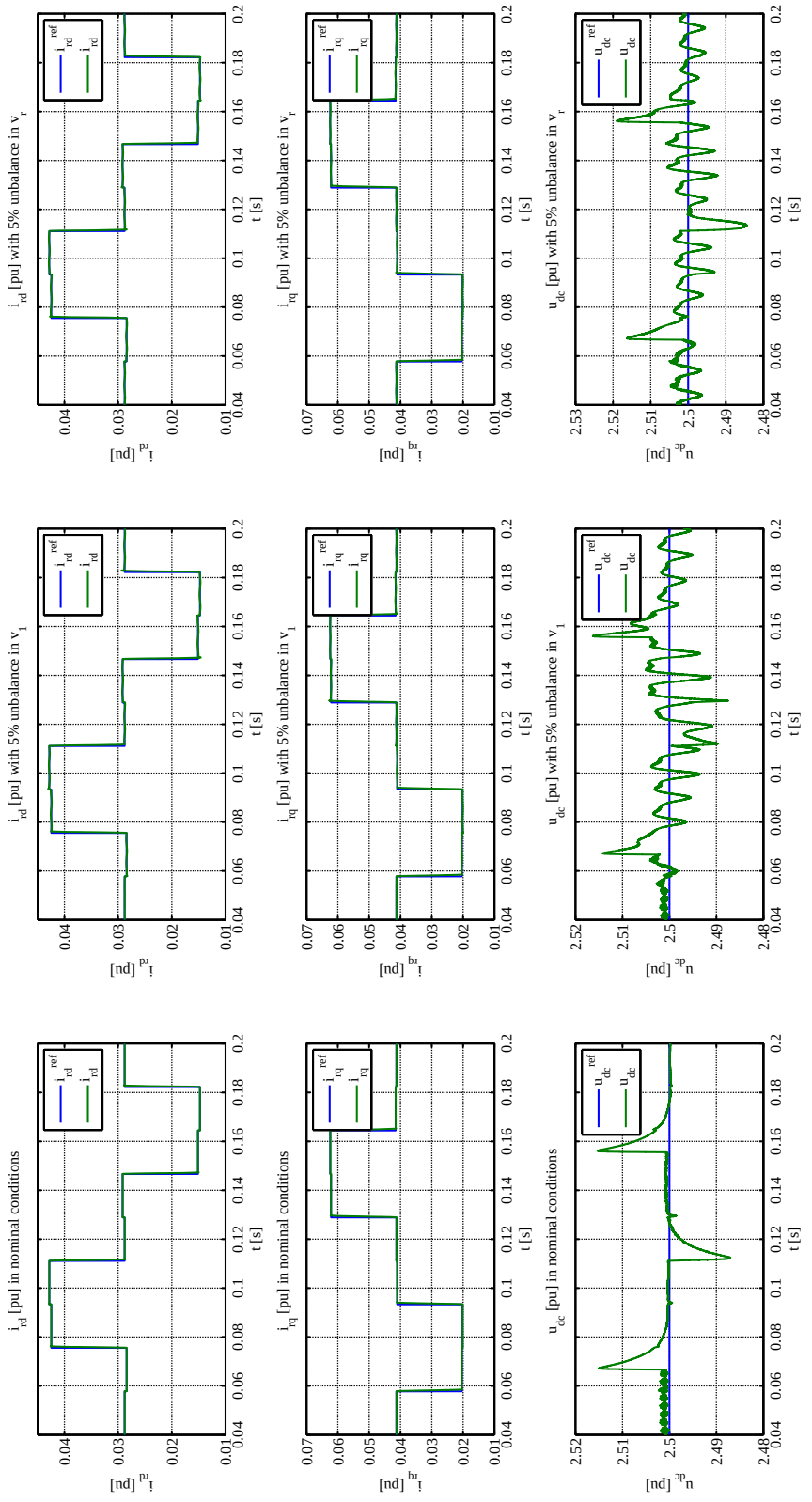


Figure III.5.13: Comparison of line currents and DC-link voltage under nominal and unbalanced conditions (second example).

5. Dual sequence-based structure for UPLC operation under unbalances

The control approach based on a trajectory generation strategy that uses chained Lyapunov-based controllers, as explained in chapters III.3 and III.4, is naturally able to track oscillating signals. However, the previous chapter has highlighted the unsuitability of this control method when used in a single positive SRF structure. This chapter proposes a dual sequence-based control structure that deals with the positive and negative sequences independently, as shown in Fig.III.5.14, and that allows using the proposed controllers ($C(e) = k_1 + k_2 \cdot sgn(e)$). The main advantage of this structure is that the references can be tracked easily without increasing controller gains.

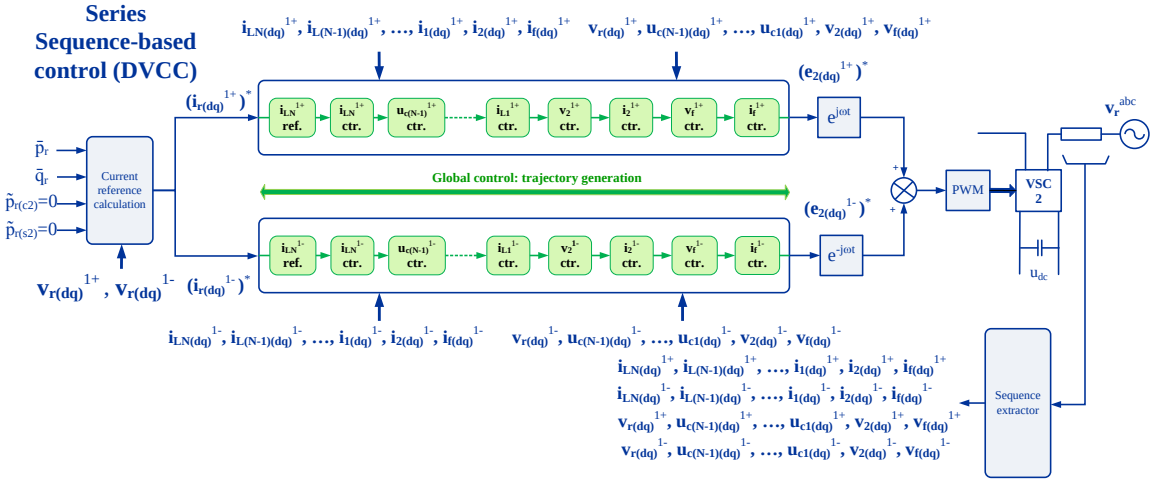


Figure III.5.14: Separate sequence-based control (DVCC) of the series side.

The performance of the method has been tested in simulation with a UPLC connected to a three-section cable. The simulations have been performed in Simulink considering ideal converters. The ${p_r}^{ref}$, ${q_r}^{ref}$ and ${q_1}^{ref}$ reference values are the same as in Fig.III.5.11 but with an augmented time-scale ($\times 5$). The line current references have been calculated to yield a constant power at the receiving-end.

The results of this set of simulations are shown in Fig.III.5.15. As it is observed, the power references are perfectly tracked and there is no oscillating active power components. As it is expected, in the case of unbalances in $\mathbf{v_r}$ oscillating reactive power components do appear but the active components are kept to zero. As demonstrated in Fig.III.5.15 a control structure that deals with symmetrical sequences independently yields very good results in ideal conditions. This is, when the converters are ideal, the sampling times are small, and the sequence extractors are instantaneous. It must be mentioned that the simulations have been performed including the Kalman filter and using the complete control structure depicted in Fig.III.5.16.

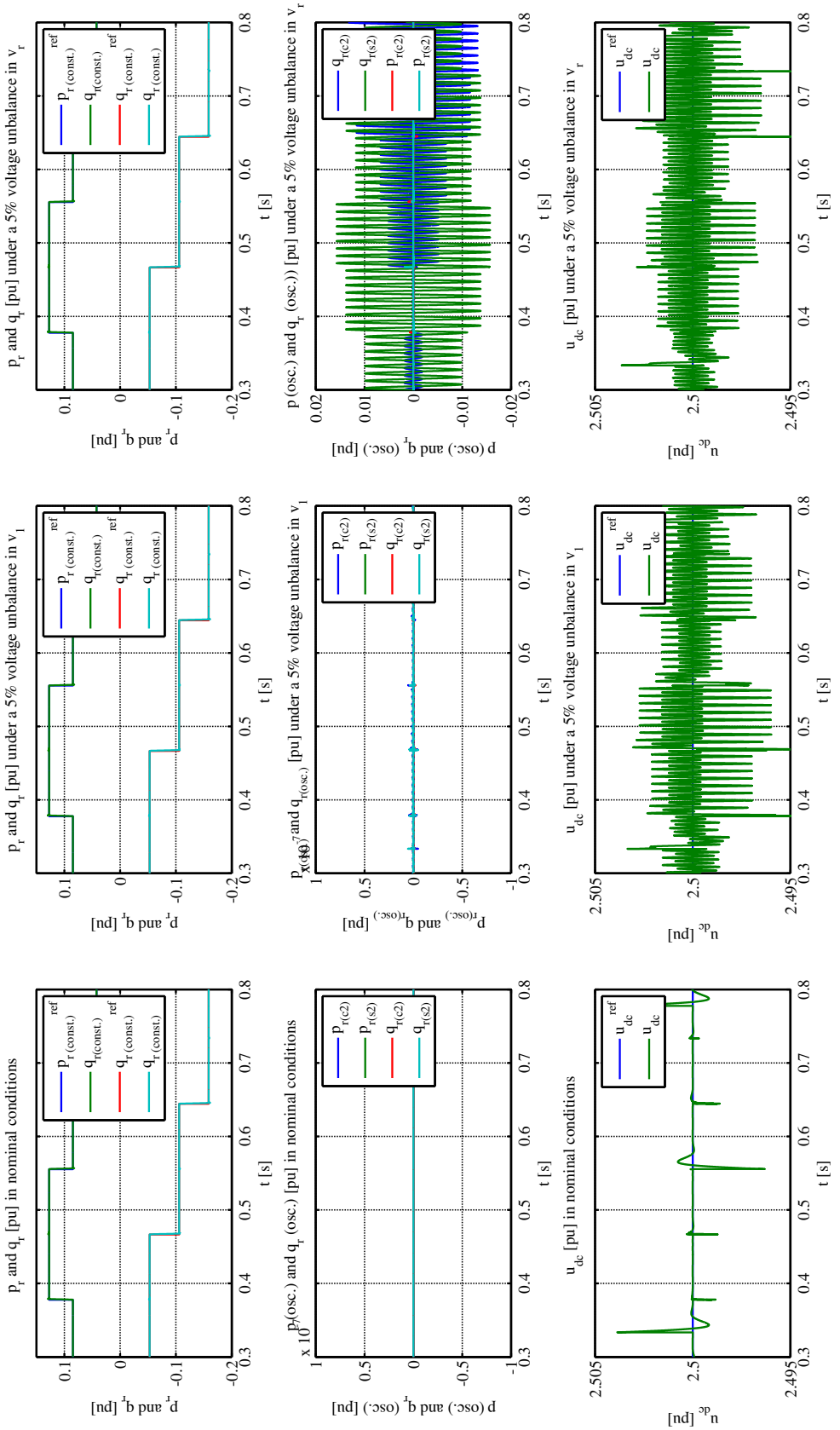


Figure III.5.15: Dual sequence oriented control of UPLC with cable (Simulink, $T_s = 1\ \mu s$).

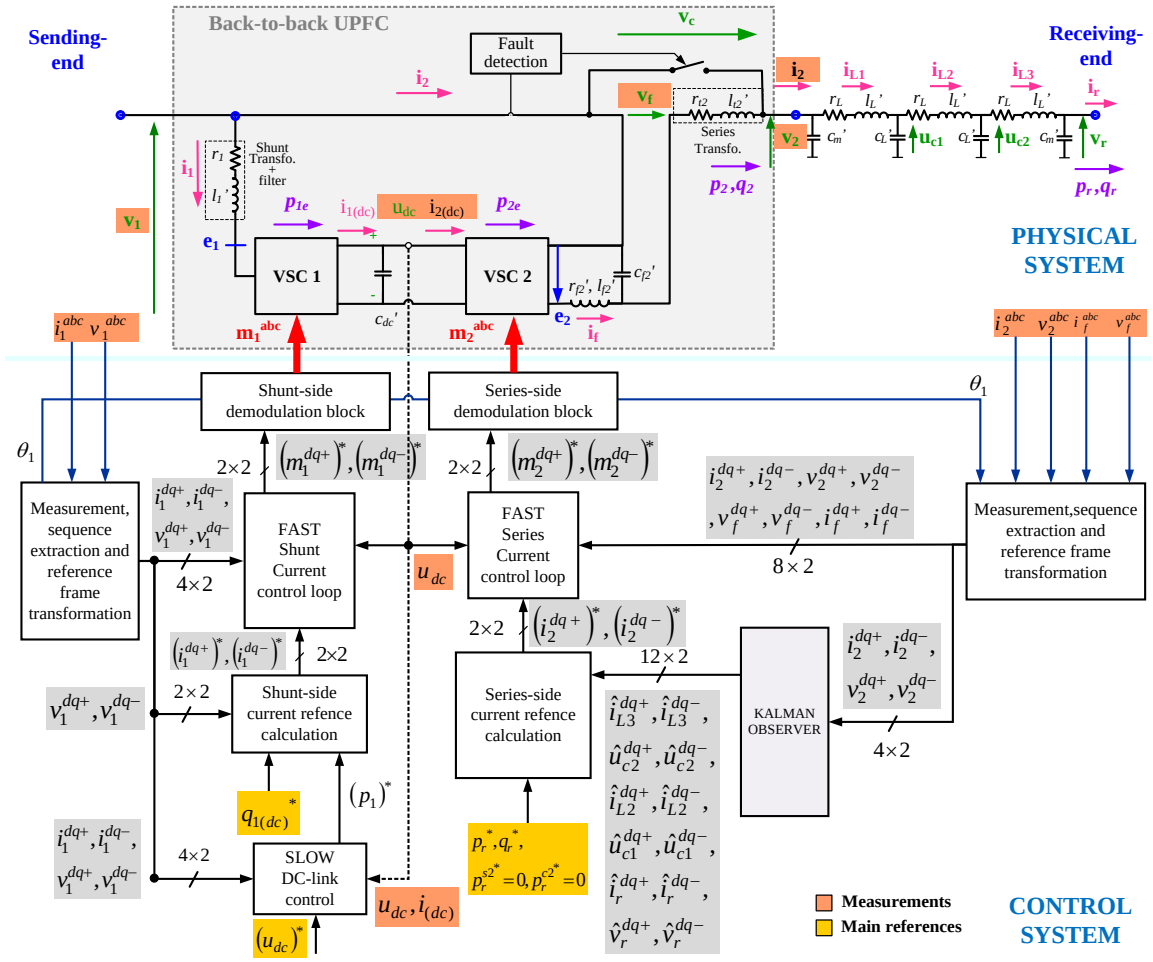


Figure III.5.16: General control structure of the UPLC using separate sequences (and including the observer).

6. Conclusions

The operation of UPFC under unbalanced conditions has not been broadly treated in literature, probably because the UPFC is mainly intented for transmission grids and, at transmission level the unbalances are less common than in distribution grids. However, the subject of unbalances has been already tackled in other types of shunt-connected FACTS devices and HVDCs and some of these approaches can be extended to the UPLC.

- **Implications of unbalances and reference generation approaches.**

  The implications of unbalanced voltages and currents are double. On the one hand, their projections on SRFs present a second harmonic component. On the other hand, the powers present oscillating terms that fluctuate at the double of the fundamental frequency.

  The last point brings to surface an interesting aspect: which strategy must be followed to generate the series-side references in the presence of unbalances? In general terms,

the receiving-end current references can be generated following two different criteria:

(1) to guarantee constant active powers at the receiving-end, or

(2) to generate balanced receiving-end currents.

Depending on the option that is selected, the reference signals may not be constant.

- **Oscillations on the DC-link.**

  The oscillating active powers induce oscillating voltages at the DC-link. Up to present, the existing shunt-side control solutions assume that the demanded power at the opposite side of the DC-link, $p_{2(dc)}$, is constant. Thus, the proposed reference-generation strategies are based on forcing the oscillating active powers at the shunt-side converter to zero. In UPLCs, this method is not effective anymore because the active power demanded by the series-converter is not constant. However, the reference generation expression is still usefull if the values of the oscillating active power references can be calculated. In order to do so, it is necessary to calculate the oscillating active powers demanded by the series converter and the losses in the power chain.

- **Control structures.**

  Among the existing control approaches, two main trends exist to deal with unbalanced voltage conditions: (i) vector-oriented structures, and (ii) scalar structures. In this chapter vector-oriented structures, which are more popular, have been evaluated. Vector-oriented techniques can be classified into to families:

  (a) control structures that use the projections of voltages and currents on SRFs (one or two SRFs), and

  (b) control structures that deal with symmetrical sequences independently (i.e. DVCC).

  Both vector control approaches are equivalent under ideal conditions:

  - The positive SRF oriented control needs powerful controllers that can track oscillating signals even under discrete environments. Moreover, this control method just needs sequence extractors for generating balanced reference currents.
  - The dual sequence-based control structure does not need high gains but needs instantaneous sequence extracting techniques. Additionally, if other frequency components are present in the signal, supplementary sequence control loops would be needed.

- **Limitations of the proposed Lyapunov-based control structure.**

  Regarding the series-side control of the UPLC, the control strategy presented in preceding chapters, which uses $C(e) = k_1 + k_2 \cdot sgn(e)$ type controllers, should be theoretically capable of tracking fluctuating reference signals. Because it is theoretically a very powerful control tool, this control method should be able to operate correctly in any of the proposed control structures: either in SRF oriented structure or in sequence-based structures. However, simulations have shown that these controllers present some

shortcomings when they are implemented in a discrete environment. They need a very small sampling time in order to increase their gains and operate efficiently.

As a solution to this problem, a dual sequence-based controller (DVCC) has been proposed and simulated. The dual sequence-based control structure provides satisfactory results for the control of a UPLC connected to a three-section cable (using $C(e) = k_1 + k_2 \cdot sgn(e)$ type controllers). However, it must be noted that the simulations presented in this chapter consider ideal converters (continuous model) and sequence extracting techniques. These simulations have been performed including the Kalman filter, that has been adapted to operate in the positive and in the negative sequences. The complete control structure can be observed in Fig.III.5.16.

Chapter III.6

Synchronization techniques and sequence extraction methods. A performance comparison between selected methods

All the above-presented control methods, even those based on scalar structures, need a synchronization technique. And, additionally, some of them, require instantaneous symmetrical sequence (ISC) extractors. In the preceding chapters, synchronization and sequence extracting techniques have been considered ideal and thus, their influence on the control performance could not be observed. However, properties such as dynamics, accuracy, or immunity against harmonics, can have a considerable influence on the overall control structure of the UPLC. In fact, the delay time of the synchronization method and of the sequence-extractors should be accounted for in the control structure if a proficient performance is to be attained.

The main objective of this chapter is to compare different sequence-extracting techniques (that also serve as synchronization strategies) providing a closer picture of the real properties and characteristics of these methods. This comparison is very useful to evaluate which sequence-extracting method is the most suitable for a particular application. Moreover, a clear knowledge of the features of synchronization techniques helps estimating how the preceding control structures must be adapted.

The chapter begins with an introduction to synchronization and sequence extracting techniques. After the introduction, a general overview of these techniques is provided establishing a difference between open-loop and closed-loop structures. Then, from the whole assortment of possible solutions, four sequence extracting techniques are selected, their working principles are described, and a comparison is made.

1. Introduction to synchronization methods and sequence extracting techniques

- **A grid synchronization technique** is basically a method that provides the intantaneous phase-angle of a grid signal, which can be either a voltage or a current (see Fig.III.6.1). Generally, the synchronization technique provides the angle of the fundamental positive sequence. Very often, the word PLL (phase-locked-loop) is erroneously used to refer to grid synchronization techniques but, it must be clarified that a PLL is just an specific (closed-loop) type of grid synchronization method.

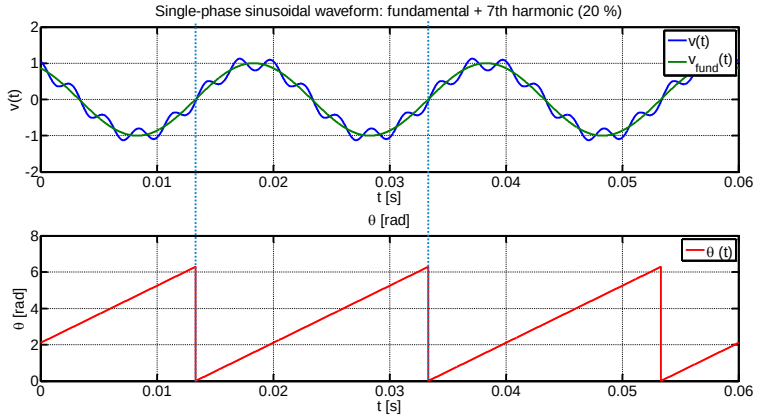


Figure III.6.1: An example of a single-phase wave composed of a fundamental and 20 % of 7th harmonic plotted together with the phase-angle of the fundamental.

- **A sequence extraction technique** is a method that is able to dissociate the positive, negative and zero sequences of a signal. Usually, for control purposes just the fundamental (50/60 Hz) sequence components are of interest but, depending on the application (active filtering or power quality monitoring, for example), also harmonics and interharmonics can be extracted. One of the main challenges in sequence and harmonics extraction techniques is the response speed and the accuracy, specially when used for control purposes. For monitoring purposes or steady-state compensation algorithms, the dynamics of the extraction process is not a critical parameter, but the accuracy becomes more relevant.

Synchronization methods are not new. The first single-phase phase-locked loops (PLLs) were presented by Appleton [130] and Bellescize [131] as early as 1923 and 1932, respectively. For the late 1970's the theoretical foundations of single-phase PLLs were well established [132, 133, 134, 135] but they could only be comprehensively implemented until the development of integrated circuits (IC) [136].

The first PLLs were mostly dedicated to telecommunication systems and they were designed to detect zero-crossings, which means that they had an intrinsic delay of half a cycle. When line-commutated converters appeared, the existing PLL technology could still be used because the firing angle unit of thyristor valves also uses zero crossings as a reference. However, with the arrival of force commutated converters (VSC), the former PLL methods became obsolete because they need a continuous tracking of the voltage phase angle.

The literature on synchronization methods and sequence extracting techniques for VSC is prolific. A possible classification of synchronization methods is presented in Fig.III.6.2, where they are divided into (i) **open-loop methods**, and (ii) **closed-loop methods**. The main difference between open- and closed-loop methods is that open-loop methods estimate the magnitude, phase and frequency of the incoming signal *straight-ahead*, whereas in closed-loop methods the phase-angle is updated constantly through a feedback loop.

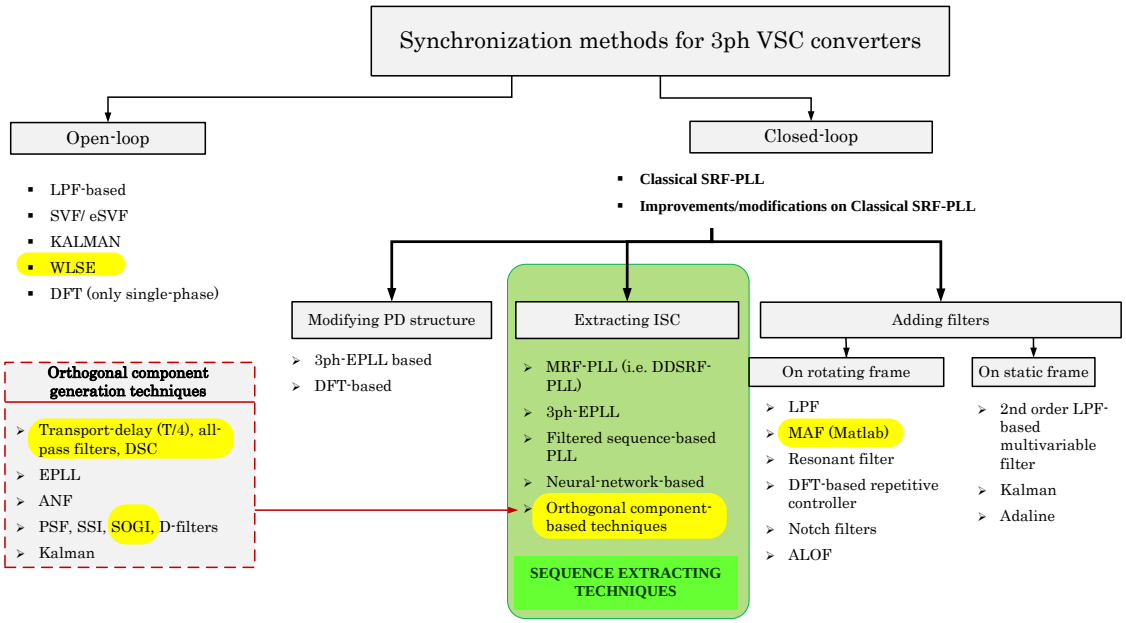


Figure III.6.2: Classification of synchronization methods for three-phase VSC.

2. Open-loop synchronization and ISC extracting techniques

In open-loop methods the phase-angle is directly estimated without the need of feeding the estimated phase-angle back. In most of the cases, these methods are filter-type or recursive identification algorithms and their performance depends on their capability of filtering distorted signals and adapting to frequency changes and phase jumps. An important feature of these methods is that, since they are not looped, they require an external frequency estimation module.

The main open-loop approaches are based on Discrete Fourier Transform (DFT), Kalman Filters (KF), Weighted Least Squares Estimation algorithm (WLSE), Artificial Neural Networks (ANN), Low Pass Filters (LPFs), and Space Vector Filters (SVFs). As a complement of these lines, the basic concepts and references of these methods have been gathered in appendix C.

3. Closed-loop synchronization and ISC extracting techniques

Closed-loop methods operate in a closed-loop structure that regulates an error signal to zero. The most popular and widespread closed-loop synchronization method is the synchronous-rotating frame PLL (SRF-PLL), that can be observed in Fig.III.6.3(b). The SRF-PLL became popular in the late 90's [137, 138, 139, 140]. Afterwards, other names have also been given to the SRF-PLL. For example, [141, 142] re-named the SRF-PLL as pq-PLL, arguing that the Power Theory made the concept of SRF-PLL easier to understand. But, in the ongoing paragraphs, the SRF-PLL appellation is used.

The SRF-PLL is similar to the classical single-phase PLL (see appendix C) and it is also

composed of a phase-detector (PD), a loop-filter (LP), which is usually a PI regulator, and a voltage-controlled oscillator (VCO), that is an integrator. The main difference between the single-phase and the three-phase PLL resides in the PD. The PD stage of the SRF-PLL is composed by Clarke's transform followed by a Park's transform. The Clarke's transform converts the input signal from the natural *abc* frame to the static $\alpha\beta$ frame, and Park's transforms converts the $\alpha\beta$ signal into a rotating frame that turns synchronously with the fundamental components of the positive sequence.

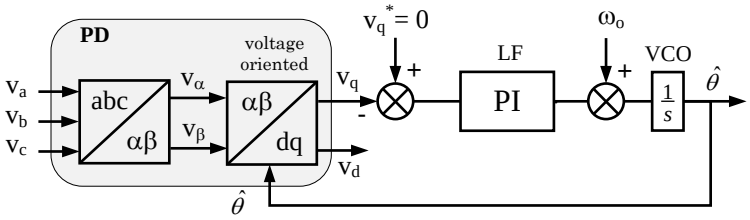


Figure III.6.3: (a) Vector diagram of a voltage phasor in different frames, and (b) Voltage-oriented SRF-PLL

As a detail, it can be mentioned that the SRF-PLL can be either (i) voltage-oriented or (ii) flux-oriented. In the voltage-oriented version the regulator sets the quadrature component of the voltage (v_q) to zero, while in the flux-oriented version it is the direct compontent (v_d) that is controlled to be null.

The main disadvantage of the classical SRF-PLL is that, when the grid voltage is distorted or unbalanced, it cannot guarantee a good filtering characteristic and a fast response at the same time. A low cutting-frequency of the loop-filter ensures a damped output at the cost of a longer transient time. With a higher bandwidth the SRF-PLL synchronizes quickly to the grid but most of the distortions of the input signal are transfered to the output.

This problem is specially pronounced in the case of unbalances, where the negative sequence is projected as a second-harmonic in the positive rotating coordinates. Since the second harmonic is very near the fundamental, it is difficult to filter it effectively without loosing considerable bandwidth.

During decades, a lot of effort has been consacrated by researchers to resolve the inherent incompatibility between fast dynamics and distortion immunity of the SRF-PLL. The proposed solutions can be divided into three main groups: (a) to modify the structure of the PD, (b) to filter the outputs of the PD, or (c) to inject a the positive sequence at the input of the PD.

3.1. Solutions that modify the structure of the PD

Some authors propose diverse ways to modify the structure of the PD. [143], for example, proposes a DFT-PLL for aircraft applications in which the PD includes a DFT algorithm. This use of DFT is quite innovative. On the other hand, [144, 145] propose two adaptations of the single-phase EPLL (see appendix C) for three-phase systems.

3.2. Solutions that use filters at the outpout of the PD

Since the effect of unbalance and harmonic distortion gets reflected in the *dq* components supplied by Park's transform, some authors propose the use of filters at the output of the PD. These filters will get rid of the non-dc components of *dq* projections. Most of the filters are located at the rotating-frame as depicted in Fig.III.6.4(a), but there are also some spare cases that introduce filters in an intermediate static stage like in Fig.III.6.4(b).

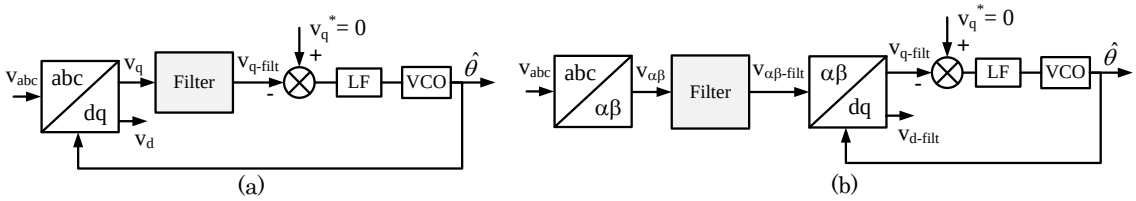


Figure III.6.4: Filters in SRF-PLL loops: (a) in the rotating-frame, and (b) in the static-frame

In the rotating frame, solutions based on LPFs [146, 147, 148], moving average filters (MAFs) [149, 147, 150] (used in the standard PLL block of Matlab SimPowerSystems toolbox), resonant filters [151, 147], DFT-based repetitive controllers [152, 147], notch-filters [146] and adaptive linear optimal filters (ALOF) [153], among others, have been used.

3.3. Solutions that use a positive sequence as input of the PD

An interesting solution, other than filtering the looped input (e.g. the quadrature component), is to extract the positive sequence from the grid-voltage and feed this sequence to the classical SRF-PLL as illustrated in fig.III.6.5. This approach allows having a distortion-free input at the PLL that will, in turn, enable tuning the PLL with a higher bandwidth. Many different alternatives have been proposed for extracting the instantaneous symmetrical components (ISC) online. It must be noted that, often, the methods used for extracting ISC with monitoring purposes are too slow for control applications.

3.3.1. ISC extraction methods

The following points overview some attractive online ISC extracting solutions.

- **Multiple reference frame based PLL (MRF-PLL)**.

  The use of multiple reference frames allow extracting the ISC separately. Two similar approaches can be observed: the decoupled double synchronous reference frame PLL (DDSRF-PLL) [148, 154] and the multiple reference frames of [155]. These methods extract positive and negative sequences by means of two reference frames rotating at the same angular speed in the positive and in the negative direction. The couplings between rotating axes are removed by decoupling networks and the magnitudes of the sequences

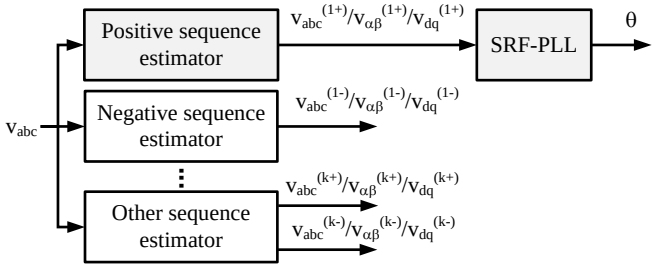


Figure III.6.5: Diagram including parallel sequence extractions and a SRF-PLL

are obtained by LPFs. These methods give excellent results in unbalanced networks but are not as performant face to strong harmonic distortion [156].

- **Three-phase EPLL**.

  In [145, 157] an EPLL-like method is proposed for online calculation of ISC. The suggested technique is mathematically derived based on an optimization problem (using Gradient Descent Algorithm) and is able to estimate magnitudes, phase-angles and frequency of ISC. This method exhibits longer transient times than other fast digital algorithms such as those based on FFT. This constitutes a limitation for those applications which require very fast transient periods. On the other hand, it has a relatively large structure which adds additional complexity. However, the authors provide design guidelines to reduce its complexity and implementation cost. The proposed solution is specially adapted for those applications which require accurate estimation of parameters in unbalanced conditions.

- **Filtered-sequence based PLL**.

  [150] proposes a variable-frequency grid-sequence detector based on a quasi-ideal low-pass filter stage and a PLL (Fig.III.6.6). The structure includes the use of Park transformations (Park and inverse-Park) and moving average filters. This solutions has shown a very good performance face to strongly distorted grid conditions showing a remarkable advantage in comparison with other more sophisticated positive-sequence detectors: its simplicity. [158] also proposes a positive sequence extraction technique based on sequential frequency-adaptive LPF filters.

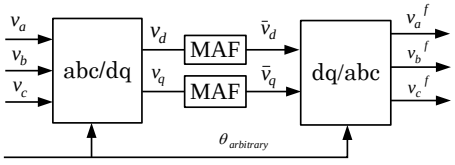


Figure III.6.6: Positive sequence extraction by means of MAF filters

- **Neural-network-based PLL**.

  Adaptive linear neural-network extractors (ADALINE) show easy synthesis and pro-

gramming and a fast response [159, 160]. These methods need an external frequency input.

- **Orthogonal component-based techniques**.

  Symmetrical sequence components can be extracted based on orthogonal components of the input voltages. In the static frame [161, 162], the fundamental positive and negative sequences can be obtained based on expressions

$$v^{+}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & s_{90} \\ -s_{90} & 1 \end{bmatrix} v_{\alpha\beta} \qquad v^{-}_{\alpha\beta} = \frac{1}{2}\begin{bmatrix} 1 & -s_{90} \\ s_{90} & 1 \end{bmatrix} v_{\alpha\beta} \tag{III.6.1}$$

  where s_{90} is the 90 degree phase-shift operator ($s_{90} = e^{j\pi/2}$). These equations can also be expressed in the natural *abc* frame [163, 164].

  This method is largely used for ISC calculation and different approaches exist. The main difficulty of the positive/negative sequence calculator (PNSC) relies on the ability of calculating quadratute signals under frequency variable conditions. Some orthogonal component calculation techniques are: all-pass filters [165], one-fourth of a period delayed signal used in Delayed Signal Cancellation method (DSC) [166, 146], EPLLs [164, 161], ANFs [163], Dual Second Order Generators (DSOGI) [161, 162], Positive Sequence Filter (PSF)/ Sinusoidal Signal Integrator (SSI) [167, 156], Kalman filters [168].

- **Kalman.**

  [169] proposes an ISC extracting technique based on complex Kalman filter. This method needs an external frequency input.

4. Selected synchronization and ISC techniques

With the overview on synchronization and ISC extraction methods in mind, four ISC extraction methods (that also serve as synchronization methods) have been selected for comparison:

(1) a PLL approach that includes a MAF filter at the output of the PD (since it is the approach used in the PLL proposed by the Matlab SymPowerSys Toolbox, the name **mPLL** will be used from now on),

(2) a WLSE algorithm,

(3) a DSOGI-FLL, and

(4) a DSC.

These methods have been chosen for their simplicity and their apparent good performances.

From the selected methods, the mPLL and DSOGI-FLL are closed-loop approaches and the WLSE and the DSC are open-loop approaches. The main advantage of mPLL and DSOGI-FLL is that the frequency identification is included in their structure so they do not need any

external frequency calculation block. Inversely, the weak point of the WLSE and the DSC is that they need an additional frequency estimator. In the following sections each of these methods are briefly described.

4.1. The Double Matlab-PLL (mPLL)

As it has been previously mentioned, one of the most relevant shortcomings of the classical SRF-PLL is that, if unbalances occur, it is necessary to decrease the bandwidth of the PLL loop substantially (below $2\omega_1$). This problem may be solved by filtering the outputs of the PD (the Park transform). In this way, the projections of the negative sequence on the positive rotating frame would be totally filtered. MAFs are appropriate candidates for performing this kind of filtering, since they have a linear phase response [170]. For obtaining satisfactory results, the length of the MAF must vary according to the grid period and the number of samples contained in a grid period must be an integer number.

This solution is the one available in the SimPowerSystems toolbox of Matlab and is further explained in [149]. Here, this method is denominated *mPLL*. The graphical illustration of the mPLL is depicted in Fig.III.6.7(b), where a voltage-oriented approach has been selected.

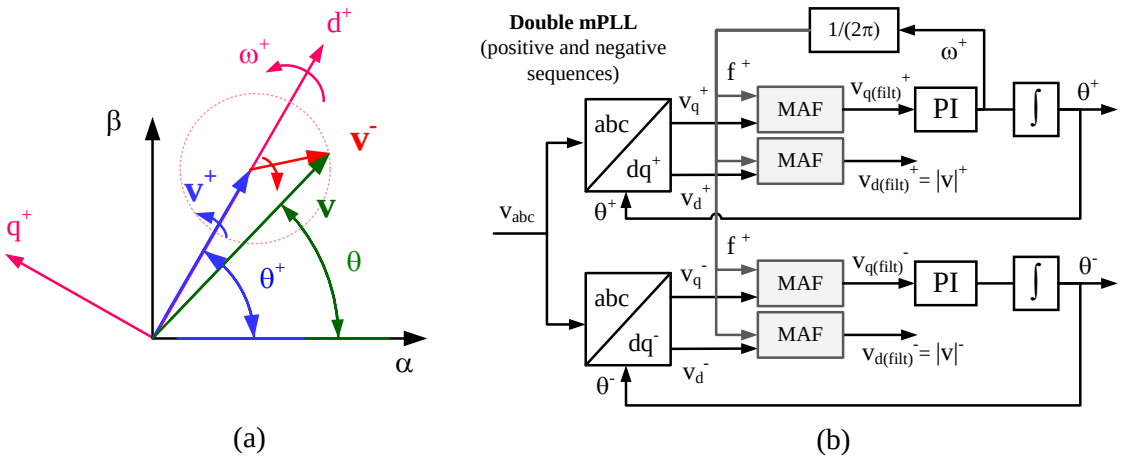


Figure III.6.7: Representation of the mPLL.

Moreover, based on this idea, if v_d^+ is also filtered with a MAF, it is possible to extract the magnitude of the positive sequence, as shown in Fig.III.6.7(a). For obtaining the negative sequence and angle, it is just necessary to reformulate the Park transform in order to reproduce a negative rotating SFR (abc/dq^-). These last changes are not included in the SimPowerSystems toolbox and are proposals of the author. Indeed, the proposed solution is similar to the DDSRF-PLL proposed by [148, 154] but it is simpler (but less effective) since it does not consider the coupling matrices between SRFs.

4.2. The Weighted Least Squares Estimation (WLSE)

As its name reveals, the WLSE is derived from a weighted least squares estimation algorithm that includes a covariance resetting technique. This open-loop synchronization and sequence extraction method has been proposed in [171, 172] claiming that is a fast technique that requires very little computational burden.

4.2.1. Principle of the WLSE method

Assuming that the input voltage is just composed of a positive sequence voltage and a negative sequence voltage, it can be expressed as:

$$\mathbf{v}_{\alpha\beta}(t_i) = \mathbf{v}^{+}_{\mathbf{dq}}(t_i) \cdot e^{j\omega t_i} + \mathbf{v}^{-}_{\mathbf{dq}}(t_i) \cdot e^{-j\omega t_i} \tag{III.6.2}$$

where $\mathbf{v}_{\alpha\beta}(t_i) = v_\alpha(t_i) + jv_\beta(t_i)$, $\mathbf{v_{dq}}^{+}(t_i) = v_d^{+}(t_i) + jv_q^{+}(t_i) = \|\mathbf{v}^{+}(t_i)\| \cdot e^{j\varphi^{+}(t_i)}$, $\mathbf{v_{dq}}^{-}(t_i) = v_d^{-}(t_i) + jv_q^{-}(t_i) = \|\mathbf{v}^{-}(t_i)\| \cdot e^{j\varphi^{-}(t_i)}$, ω is the fundamental voltage, and t_i is the time at instant i.

In order to present the algorithm, it is possible to represent equation (III.6.2) in a compact form:

$$\mathbf{y}(t_i) = \mathbf{H}(t_i)\mathbf{x}(t_i) \tag{III.6.3}$$

where

$$\mathbf{H}(t_i) = \begin{bmatrix} \cos(\omega t_i) & -\sin(\omega t_i) & \cos(\omega t_i) & \sin(\omega t_i) \\ \sin(\omega t_i) & \cos(\omega t_i) & -\sin(\omega t_i) & \cos(\omega t_i) \end{bmatrix} \tag{III.6.4}$$

$$\mathbf{x}(t_i) = \begin{bmatrix} v_d^{+}(t_i) & v_q^{+}(t_i) & v_d^{-}(t_i) & v_q^{-}(t_i) \end{bmatrix}^t \tag{III.6.5}$$

$$\mathbf{y}(t_i) = \begin{bmatrix} v_\alpha(t_i) \\ v_\beta(t_i) \end{bmatrix} \tag{III.6.6}$$

The objective of the WLSE algorithm is to minimize a cost function J chosen such that

$$J[\mathbf{x}(t_i)] = \sum_{j=0}^{i} \lambda^{i-j} \left[\mathbf{y}(t_j) - \mathbf{H}(t_j)\mathbf{x}(t_j)\right]^t \cdot \left[\mathbf{y}(t_j) - \mathbf{H}(t_j)\mathbf{x}(t_j)\right] \tag{III.6.7}$$

where λ is the forgetting factor. The solution $\hat{\mathbf{x}}(t_i)$ that minimizes the cost function $J[\mathbf{x}(t_i)]$ is obtained by the least-squares algorithm that is graphically illustrated in the flowchart of Fig.III.6.8.

As it can be observed in the flowchart, if the estimation error is larger than a given threshold ϵ, the error covariance $\mathbf{P}(t_{i-1})$ is resetted to the initial covariance value, $\pi_0\mathbf{I_4}$. The covariance resetting is done when a sudden voltage or phase-jump occurs. For that reason, in order to avoid a frequent resetting, the threshold must not be set too low. The authors of [171, 172] advise a value of ϵ between 20%-40% of the nominal voltage value.

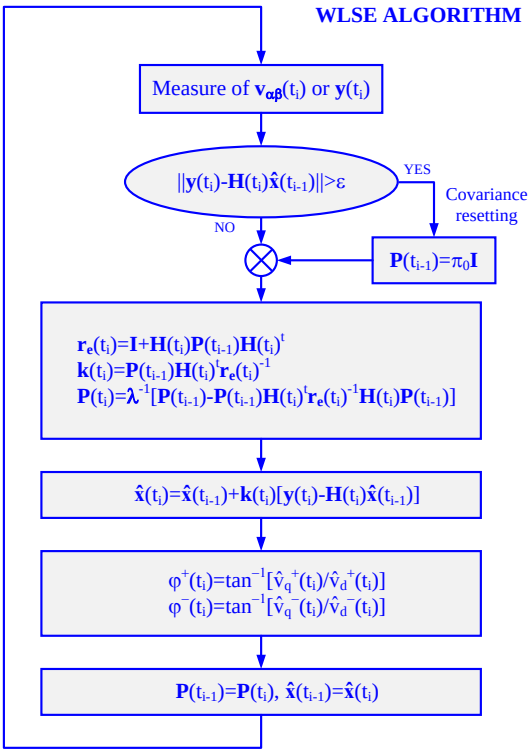


Figure III.6.8: WLSE algorithm.

The noise immunity of the WLSE algorithm can be modulated with the forgetting factor λ. Usually, a large value of λ (close to unity) increases the immunity of the algorithm against harmonic disturbances at the cost of a longer convergence time. Appart from λ, the convergence time of the algorithm is also influenced by the sampling time, T_s, and the initial error covariance, π_0. The convergence time reduces when the sampling time reduces or when the initial error covariance increases [171, 172].

4.3. The Delayed Signal Cancellation (DSC)

The Delayed Signal Cancellation [146, 173, 160, 166] method is one of the most straightforward methods to extract symmetrical sequences. It just needs the quadrature components of the input signal. The positive and negative symmetrical sequences are calculated using equation (III.6.1), that is also known as the Positive/Negative Sequence Calculation (PNSC) method. This equation is rewritten here:

$$\mathbf{x}^+_{\alpha\beta}(t) = \frac{1}{2}\left[\mathbf{x}_{\alpha\beta}(t) + \mathbf{j}\cdot\mathbf{x}_{\alpha\beta}(t - T_1/4)\right] \tag{III.6.8}$$

$$\mathbf{x}^-_{\alpha\beta}(t) = \frac{1}{2}\left[\mathbf{x}_{\alpha\beta}(t) - \mathbf{j}\cdot\mathbf{x}_{\alpha\beta}(t - T_1/4)\right] \tag{III.6.9}$$

As it can be observed, equation (III.6.8) is really simple, and it just needs the quarter-period delayed signal of the grid phasor. Under ideal conditions, this method is one of the most

simple and fast method that can be implemented. Additionally, the delay time of the method is just $T_1/4$. Unfortunately, as for the rest of the sequence extracting techniques, this methods also presents shortcomings when the environmental conditions are not ideal:

- **Grid frequency and discrete implementation.**

  In a discrete implementation, the delayed signal is calculated by delaying the input signal an integer number of samples as,

$$\mathbf{x}^{+}_{\alpha\beta}(kT_s) = \frac{1}{2}\left[\mathbf{x}_{\alpha\beta}(kT_s) + \mathbf{j}\cdot\mathbf{x}_{\alpha\beta}(kT_s - n_dT_s)\right] \tag{III.6.10}$$

$$\mathbf{x}^{-}_{\alpha\beta}(kT_s) = \frac{1}{2}\left[\mathbf{x}_{\alpha\beta}(kT_s) - \mathbf{j}\cdot\mathbf{x}_{\alpha\beta}(kT_s - n_dT_s)\right] \tag{III.6.11}$$

  where T_s is the sampling time, and n_d is the number of delayed samples, that is expressed as $n_d = \frac{T_1}{4T_s}$ (T_1 is the fundamental grid period). Ideally, n_d must be an integer number. However, if one grid-period does not contain an integer number of samples (for instance when the grid frequency varies), the value of n_d must be adjusted to the nearest integer number. This approximation can lead to errors in the calculation of the symmetrical components. In any case, it is possible to reduce these errors by using averaging techniques [166].

- **Harmonic filtering.**

  If the input signal contains harmonics, the PNSC equations cannot block them and the estimations of the positive and negative fundamental components may contain estimation errors. However, not all the harmonics propagate in the same way. The following expression illustrates this effect:

$$\hat{\mathbf{x}}^{+}(t) = \frac{1}{2}\left[\sum_{n=1}^{\infty}\mathbf{x}^{n+}e^{\mathbf{j}nw_1t} + \sum_{m=1}^{\infty}\mathbf{x}^{m-}e^{-\mathbf{j}mw_1t}\right] \tag{III.6.12}$$

$$+\frac{1}{2}\,e^{\mathbf{j}\pi/2}\left[\sum_{n=1}^{\infty}\mathbf{x}^{n+}e^{\mathbf{j}n(w_1t-\pi/2)} + \sum_{m=1}^{\infty}\mathbf{x}^{m-}e^{-\mathbf{j}m(w_1t-\pi/2)}\right] \tag{III.6.13}$$

$$\hat{\mathbf{x}}^{-}(t) = \frac{1}{2}\left[\sum_{n=1}^{\infty}\mathbf{x}^{n+}e^{\mathbf{j}nw_1t} + \sum_{m=1}^{\infty}\mathbf{x}^{m-}e^{-\mathbf{j}mw_1t}\right] \tag{III.6.14}$$

$$+\frac{1}{2}\,e^{-\mathbf{j}\pi/2}\left[\sum_{n=1}^{\infty}\mathbf{x}^{n+}e^{\mathbf{j}n(w_1t-\pi/2)} + \sum_{m=1}^{\infty}\mathbf{x}^{m-}e^{-\mathbf{j}m(w_1t-\pi/2)}\right] \tag{III.6.15}$$

  where upperscript n denotes positive sequence harmonics, m stands for negative-sequence harmonics, $\hat{\mathbf{x}}^{+}$ is the estimated positive (fundamenal) component, and $\hat{\mathbf{x}}^{-}$ is the estimated negative (fundamenal) component.

  Reorganizing the equations, it is possible to obtain the relationships between each of the

input harmonic components and the estimated fundamental positive/negative sequences.

$$\hat{\mathbf{x}}^{+}(t) = \sum_{n=1}^{\infty} \underbrace{\left[\frac{1+e^{-\mathbf{j}(n-1)\pi/2}}{2}\right]}_{\mathbf{C}_\alpha} \mathbf{x}^{n+} e^{\mathbf{j}nw_1 t} + \sum_{m=1}^{\infty} \underbrace{\left[\frac{1+e^{\mathbf{j}(m+1)\pi/2}}{2}\right]}_{\mathbf{C}_\beta} \mathbf{x}^{m-} e^{-\mathbf{j}mw_1 t} \quad \text{(III.6.16)}$$

$$\hat{\mathbf{x}}^{-}(t) = \sum_{n=1}^{\infty} \underbrace{\left[\frac{1+e^{-\mathbf{j}(n+1)\pi/2}}{2}\right]}_{\mathbf{C}_\gamma} \mathbf{x}^{n+} e^{\mathbf{j}nw_1 t} + \sum_{m=1}^{\infty} \underbrace{\left[\frac{1+e^{\mathbf{j}(m-1)\pi/2}}{2}\right]}_{\mathbf{C}_\delta} \mathbf{x}^{m-} e^{-\mathbf{j}mw_1 t} \quad \text{(III.6.17)}$$

where, coefficients $\mathbf{C}_\alpha$, $\mathbf{C}_\beta$, $\mathbf{C}_\gamma$, and $\mathbf{C}_\delta$ represent the relationships between the input harmonics of the signal and the estimated fundamental sequences.

The values of coefficients $\mathbf{C}_\alpha$, $\mathbf{C}_\beta$, $\mathbf{C}_\gamma$, and $\mathbf{C}_\delta$ have been classified in Table III.6.1 according to the harmonic orders contained in the input signal. Table III.6.1 proofs that, when only fundamental components exist ($n = 1$ and $m = 1$), the fundamental negative sequence component does not have any effect on the positive sequence estimation and that the fundamental positive sequence does not have any effect on the negative sequence calculation. However, this is not the case for other harmonic orders. For example, positive-rotating harmonics of the type $(4n + 1)$ will appear integraly in the positive sequence fundamental, distorting the estimation of the positive fundamenal component.

Table III.6.1: Harmonic propagation coefficients in DSC

Harmonic order (modulus)	C_α	C_β	C_γ	C_δ
4n (0,4,8,12,...)	$(1/\sqrt{2})\ e^{\mathbf{j}\pi/4}$	$(1/\sqrt{2})\ e^{\mathbf{j}\pi/4}$	$(1/\sqrt{2})\ e^{-\mathbf{j}\pi/4}$	$(1/\sqrt{2})\ e^{-\mathbf{j}\pi/4}$
4n+1 (1,5,9,13,...)	1	0	0	1
2(2n+1) (2,6,10,...)	$(1/\sqrt{2})\ e^{-\mathbf{j}\pi/4}$	$(1/\sqrt{2})\ e^{-\mathbf{j}\pi/4}$	$(1/\sqrt{2})\ e^{\mathbf{j}\pi/4}$	$(1/\sqrt{2})\ e^{\mathbf{j}\pi/4}$
4n-1 (3,7,11,...)	0	1	1	0

As it is clearly observed in Table III.6.1, the DSC cannot block the harmonics of the input signal and thus, if the input signal is highly distorted, the estimation of the fundamental positive and negative sequences will not be accurate. One possible solution to avoid this problem is to first extract the fundamental component of the input signal and use it as an input in PNSC equations.

The next presented method, which is known as DSOGI-FLL, is able to extract the fundamental component of the input signal and to generate the quadrature component. Moreover, thanks to a closed frequency loop, it can calculate the grid frequency.

4.4. The Double Second Order Generalized Integrator associated to a FLL (DSOGI-FLL)

The DSOGI-FLL, that is proposed by [162, 161], is based on the same principle as the DSC and it also calculates the positive and negative sequences of the input signal based on equations (III.6.1) (PNSC equations). The difference between the DSC and the DSOGI-FLL is that, in the DSOGI-FLL, the input signal is filtered and that the quadrature signal is obtained by means of a double-order equation. The fundamental principle of the DSOGI-FLL is graphically presented in Fig.III.6.9, where q is represents the 90° lagging signal ($q = -\mathbf{j} = e^{-\mathbf{j}\pi/2}$).

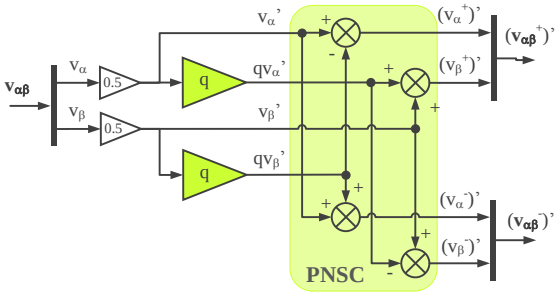


Figure III.6.9: Simplified diagram of the DSOGI.

Once the essence of this sequence extraction technique is presented, two relevant aspects must be regarded. On the one hand, it is necessary to generate a 90° phase-shift of the **fundamental** component of the input signal. On the other hand, it is necessary to guarantee that the 90° phase-shift is kept even if the frequency changes. These aspects are discussed next. The diagram of the SOGI-QSG is presented in Fig.III.6.10.

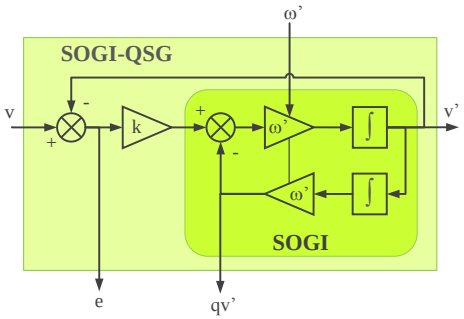


Figure III.6.10: Schematic diagram of the SOGI-QSG.

4.4.1. Extraction of the fundamental component of the input signal and generation of a 90° phase-shifted version of the fundamental component

One of the most important aspects of the DSOGI-FLL is to generate the quadrature signal that corresponds to the fundamental frequency component of the input signal. In this method, the extraction of the fundamental component and its 90° phase-shifted signal are obtained by

using a couple of second order equations:

$$D(s) = \frac{v'(s)}{v(s)} = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2} \tag{III.6.18}$$

$$Q(s) = \frac{qv'(s)}{v(s)} = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \tag{III.6.19}$$

where ω' is the resonance frequency and k is the damping factor.

The bode-plots corresponding to these transfer functions are depicted in Fig.III.6.11 for different values of k. As it can be observed, these equations act as band-pass filters, selecting the fundamental component of the input signal. The lower the value of k is, the narrower is the filter bandwidth. Unfortunately, lower values of k generate a longer time response. A critically-damped response is obtained when $k = \sqrt{2}$, as it can be observed in Fig.III.6.11. It is interesting to appreciate that the phase-angles of $D(s)$ and $Q(s)$ always present a 90° phase-displacement.

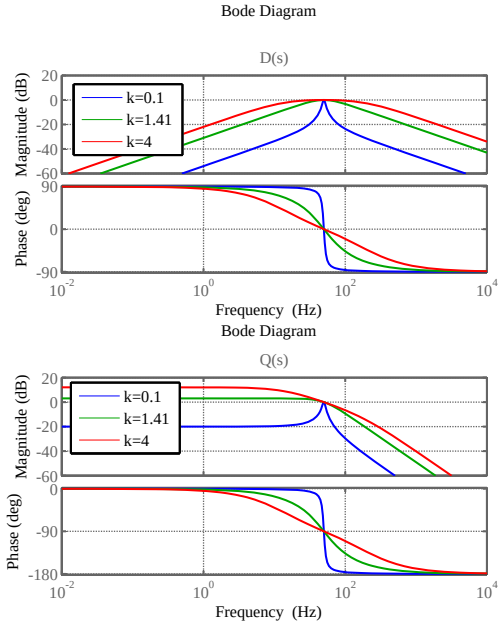


Figure III.6.11: Bode diagrams of D(s) and Q(s).

4.4.2. Frequency estimation

One of the main disadvantages of equations (III.6.18) is that, if the fundamental frequency of the input signal (ω) is not in agreement with the center frequency of the filter (ω') the outputs of the quadrature signal generator (SOGI-QSG) will not be correct.

The following equations provide the distortion factor of the input signal (**D** and **Q**) when this

occurs [162]:

$$\mathbf{v}' = \mathbf{D} \cdot \mathbf{v} \Leftrightarrow \begin{cases} |\mathbf{D}| & = \dfrac{k\omega\omega'}{\sqrt{(k\omega\omega')^2 + (\omega^2 - \omega'^2)^2}} \\ \angle\mathbf{D} & = \tan^{-1}\left(\dfrac{\omega'^2 - \omega^2}{k\omega\omega'}\right) \end{cases} \tag{III.6.20}$$

and,

$$\mathbf{qv}' = \mathbf{Q} \cdot \mathbf{v} \Leftrightarrow \begin{cases} |\mathbf{Q}| & = \dfrac{\omega'}{\omega}|\mathbf{D}| \\ \angle\mathbf{Q} & = \angle\mathbf{D} - \pi/2 \end{cases} \tag{III.6.21}$$

where v' represents the fundamental component of the input signal.

Actually, when the input signal contains harmonics, **D** and **Q** act as damping factors for these harmonics.

In order to avoid the distortion of the input signal and to make the filter frequency-adaptative, a frequency locked-loop (FLL) is proposed to track the frequency changes. This FLL, which is depicted in Fig.III.6.12, is very similar to a conventional SRF-PLL, but the quadrature component $-qv'$, is used as feedback signal. The FLL guarantees the frequency adaptivity of the DSOGI-QSG.

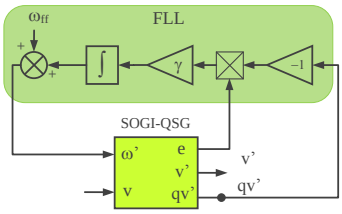


Figure III.6.12: Schematic diagram of the FLL loop.

The whole DSOGI-FLL setup can be observed in Fig.III.6.13.

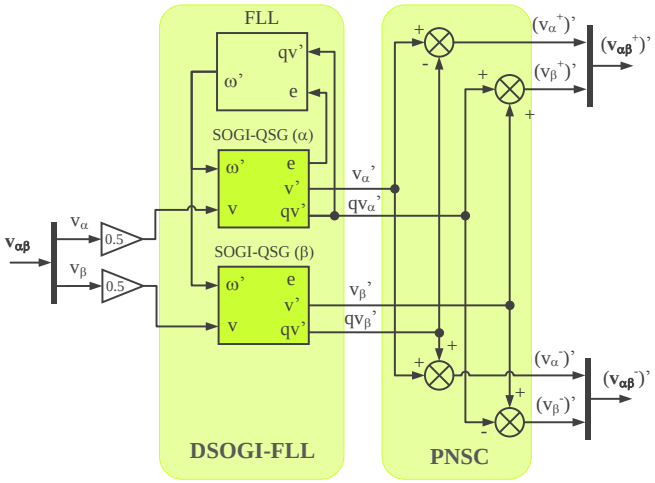


Figure III.6.13: Schematic diagram of DSOGI-FLL.

5. Comparison between selected ISC extraction techniques

The objective of the present section is to provide a comparison of the previously presented techniques under different conditions. It is not easy to provide an absolute comparison of these methods because there are plenty aspects that can be compared and the relevance of each aspect must be ponderated according to the specific needs of each user. Some important aspects that have been evaluated are:

- **Design simplicity.**

  Regarding design simplicity, the DSC technique is the most simple since it does not require any design parameters. Then, the mPLL and the DSOGI-FLL, just need the selection of two parameters:

  * In the case of the mPLL, the proportional and integral gains of the PI controller (K_p and K_i) must be chosen. Guidelines to choose this parameters can be found in [139, 138, 137].

  * In the case of the DSOGI-FLL, k and γ must be selected. The value of k determines the width of the band-pass filter. The smaller the value of k is, the narrower the bandwidth is at the cost of a higher settling time. The value of γ influences the dynamics of the FLL loop. A higher γ produces a faster response with a larger overshoot.

  Finally, the WLSE is the method that requires more parameters, requiring the selection of three design values: the forgetting factor λ, the initial covariance error π_0, and the resetting threshold ϵ. The immunity of the WLSE technique in distorted environments depends essentially on the value of the forgetting factor, which must be in the $[0, 1]$ range. When λ is close to 1, the algorithm damps the harmonics very well but its response time is slower. As an important observation, it must be mentioned that the value of the sampling time T_s influences the dynamics and accuracy of the output signals.

- **Dynamics and immunity against harmonic distortion.**

  The DSC technique has always a delay time of 5 ms (@ 50 Hz) and is highly sensitive to harmonics. Since it cannot be tuned, nothing can be done to increase the immunity of the filter against harmonics. The only possible solution is to add a MAF to the outputs of the DSC. The addition of a MAF filter results in an increase of the convergence time from 5 ms to 20 ms but yields very accurate and damped results.

  Regarding the mPLL, it also needs a MAF filter at the outputs of the v_d component because, since two SRFs are used, the positive and negative sequences are mutually projected in the complementary SRF. This is, the positive sequence appears in the negative SRF as a double frequency component and vice-versa. This means that, if the MAF filter has a length of one grid period, the delay-time of mPLL will be in the neighbourhood of 20 ms.

The DSOGI-FLL and the WLSE can adapt their convergence times and their immunity against disturbances by means of their design parameters. Nevertheless, it is not possible to achieve a good damping and a fast response at the same time. As it will be presented in the next paragraphs, if the ISC extractors are located in very distorted environments, it may be interesting to tune these extractors to have a fast response and to add MAF filters at their outputs instead of lowering the convergence time of the WLSE and the DSOGI-FLL.

- **Frequency variations and phase-jumps.**

  All of the selected methods can be adapted to work in frequency variable environments. However, one important difference can be observed between them: the mPLL and the DSOGI-FLL can calculate the frequency autonomously, while the WLSE and the DSC need an external frequency calculation module. In [172] a frequency estimation procedure for the WLSE is proposed. However, this method has already been tested in simulation and it is just valid for slow frequency changes.

  On the other hand, when working in discrete environments (which nowadays is always), the mPLL and the DSC are sensitive to frequency variations since their accuracy depends on the synchronism of the grid period and the sampling time. If a grid period does not contain an integer number of samples, estimation errors will occur. This errors will be higher for lower sampling rates.

  For looped ISC extraction methods (mPLL and DSOGI-FLL), phase-jumps are perceived as frequency variations. For this reason, closed-loop methods are not so performant when phase-jumps occur. However, it must be mentioned that, the other methods also need a frequency estimator and, in many cases, this frequency estimator will also be sensitive to phase jumps.

5.1. Evaluation of dynamics and immunity against harmonic distortion.

As it has been mentioned before, the DSC technique has an invariable delay time of 5 ms. However, it is also possible to tune the other methods in order to yield fast response times. In Fig.III.6.14, the ISC extraction methods are tuned to have short convergence times in the order of 5 ms-10 ms. In this figure, the module of the positive sequence suffers a sudden change at 0.2223s (from 1 pu to 0.7 pu without phase-jump) and the outputs of the evaluated methods are not filtered. Two simulations have been performed: (a) one without harmonics (left column), and (b) one with harmonic distortion (right column). In the harmonic case, the THD is around 11%. The order, magnitude, and angle of the harmonic components are presented in Table III.6.2. From these simulations, the following remarks can be done:

i) The projection of the positive sequence, which oscillates at 100 Hz, is appreciated in the negative sequence estimation of the mPLL. This facts suggests that it is compulsory to low-pass filter the v_d component of the mPLL in order to obtain the magnitude of the

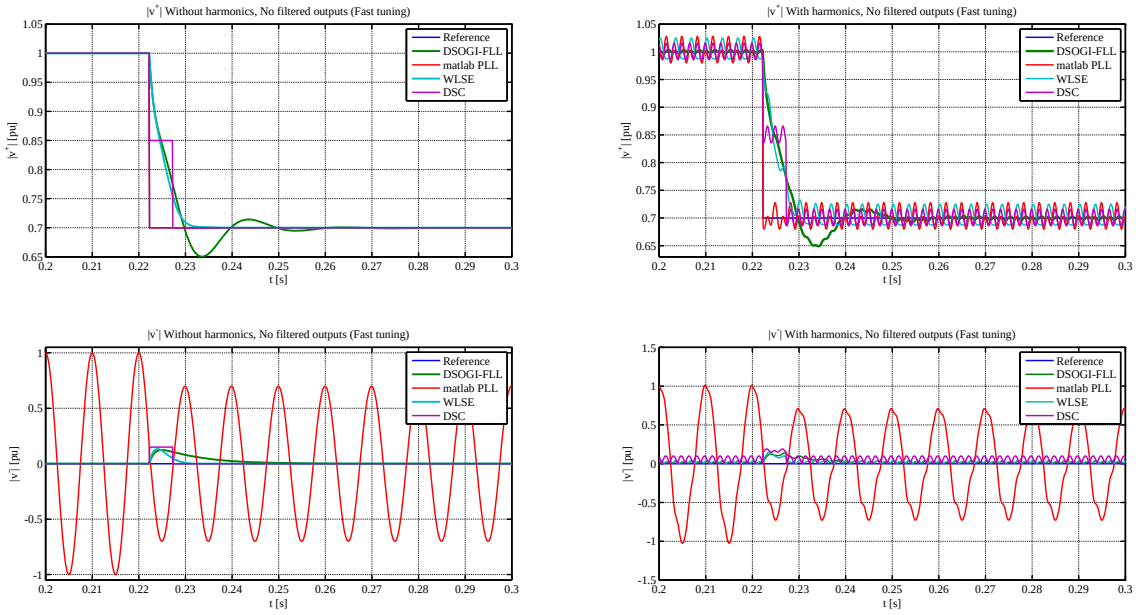


Figure III.6.14: The trade-off between dynamics and robustness against harmonics. Simulations WITHOUT filters and a fast tunning. The magnitude of the positive sequence changes from 1 *pu* to 0.7 *pu* without phase-jumps.

Table III.6.2: Harmonic components of the input signal of Fig.III.6.14

	Modulus (pu)	Angle (deg)
-5	0.05	+70
+7	0.05	+125
-11	0.02	+45
+13	0.02	+90

ISCs. From now on a MAF filter is added to the outputs of the mPLL.

ii) The convergence time of the DSOGI-FLL and the WLSE is around 10 *ms*. It can also be observed that the response of the DSOGI-FLL is underdamped with an overshoot of around 0.05 *pu*.

iii) In all the methods there is a coupling between the estimated positive and negative sequences. It is observed that, at $t = 0.2223$ *s* a non-zero value of the negative sequence is detected for around a 5-20 *ms* time.

iv) Regarding the distorted case, it can be observed that non of the methods is able to filter these harmonics.

In order to evaluate how a slower tuning of the WLSE and DSOGI-FLL can improve the filtering capability of these ISC extraction techniques, a second set of simulations has been performed with *slower* dynamics. Since the DSC and the mPLL need a MAF, these two methods are not included in the simulation results. The results of this simulation are shown

in Fig.III.6.15 and, as it can be observed, the harmonics are considerably reduced but the response time becomes 10 times higher (around 100 ms).

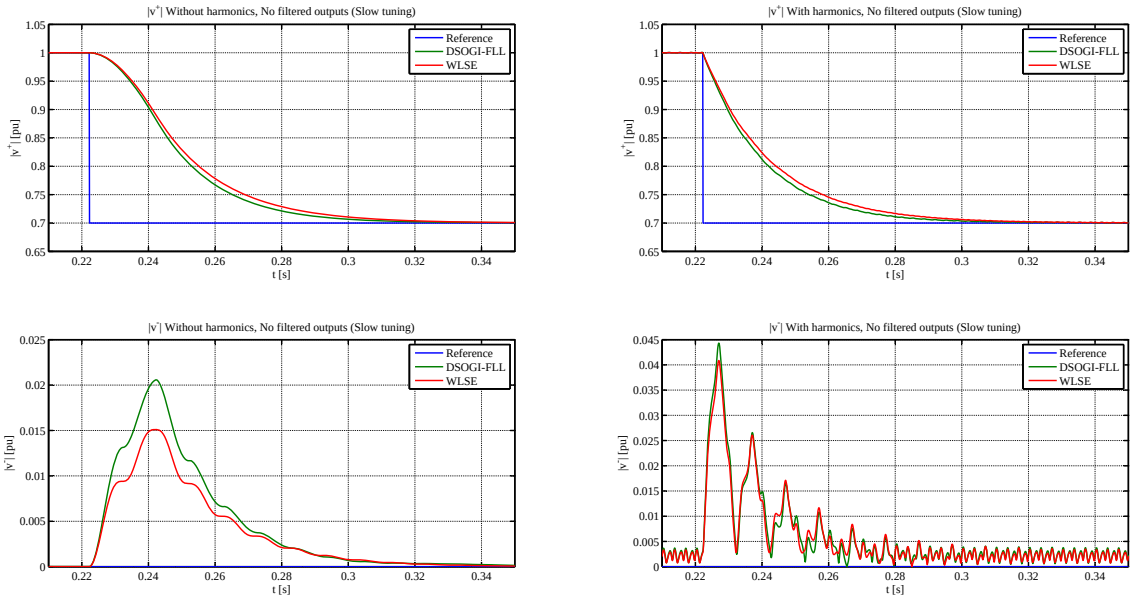


Figure III.6.15: The trade-off between dynamics and robustness against harmonics. Simulations WITHOUT filters and a slow tunning. The magnitude of the positive sequence changes from 1 pu to 0.7 pu without phase-jumps.

After this evaluation, it is deduced that it is probably more interesting to tune the extractors with fast dynamics and to filter the outputs. The simulation results after adding MAF filters to the outputs of the extractors are provided in Fig.III.6.16. From Fig.III.6.16 the following conclusions are extracted:

- All the extractors present delay times above 20 ms but below 40 ms.
- Except for the DSOGI-FLL, the harmonics do no longer impact the estimation of the sequence magnitude. In DSOGI-FLL, the average value of the harmonic components contained in the negative sequence is not zero and thus, the harmonics appear as a constant deviation from the real value. Unfortunately, the only solution to this deviation is to make the band-pass filter of the DSOGI more selective narrowing its bandwidth but increasing the response time.

Seen the good results obtained by adding a MAF filter at the outputs of the ISC extractors, the rest of the analysis will consider these filters at the output of the extractors.

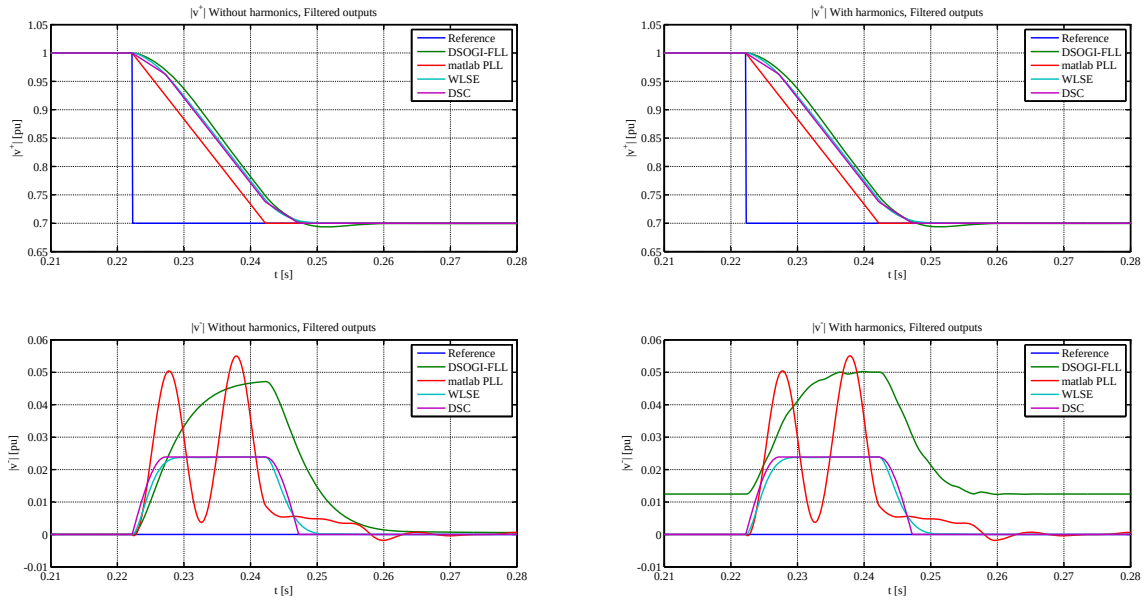


Figure III.6.16: The trade-off between dynamics and robustness against harmonics. Simulations WITH filters and a fast tunning. The magnitude of the positive sequence changes from 1 *pu* to 0.7 *pu* without phase-jumps.

5.2. Phase-jumps and frequency variations.

5.2.1. Phase-jumps

Phase-jumps and frequency variations are closely related. In closed-loop synchronization methods, the phase-jumps are interpreted as frequency variations by the estimator.

When a phase-jump occurs, a transient estimation error occurs in closed-loop systems. This error can be observed in Fig.III.6.17 for mPLL and DSOGI-FLL. In this simulation, first the positive sequence suffers a 0.3 *pu* deep with a phase jump of 60° (from 0.222*s* to 0.448*s*) and after this deep, the negative sequence suffers a swell of 0.2 *pu* and a phase jump of 30ř (from 0.555*s* to 0.777*s*). As it can be noticed, the mPLL has a remarkable transient error while the error of the DSOGI-FLL is lower. This figure also highlights that the negative sequence estimation of the mPLL is not satisfactory in comparison to the other methods, it oscillates too much. The DSC and the WLSE cannot be taken into account because their frequency input is the real frequency.

The frequency estimation error made by the mPLL and the DSOGI-FLL is depicted in Fig.III.6.18.

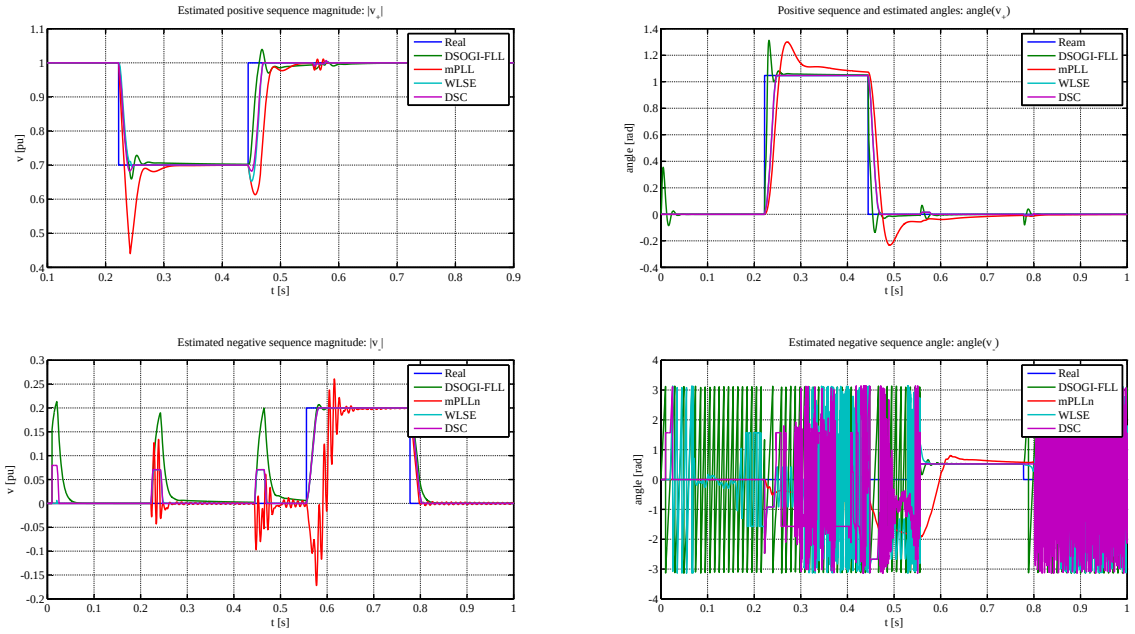


Figure III.6.17: Comparison between sequence extraction methods with: (i) No harmonics, (ii) sequence magnitude changes ($|\Delta \mathbf{v}^+| = 0.3\ pu$ and $|\Delta \mathbf{v}^-| = 0.2\ pu$) (iii) phase jumps ($\Delta\varphi^+ = 60\ deg.$ and $\Delta\varphi^- = 30\ deg.$).

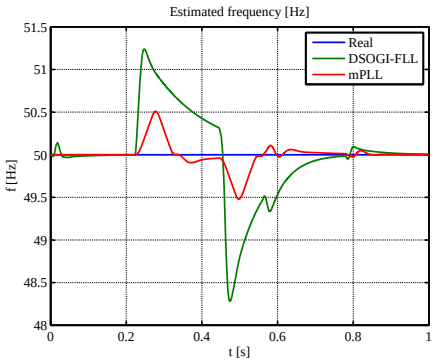


Figure III.6.18: Frequency estimated by DSOGI-FLL and mPLL: (i) No harmonics, (ii) sequence magnitude changes ($|\Delta \mathbf{v}^+| = 0.3\ pu$ and $|\Delta \mathbf{v}^-| = 0.2\ pu$) (iii) phase jumps ($\Delta\varphi^+ = 60\ deg.$ and $\Delta\varphi^- = 30\ deg.$).

5.2.2. Frequency variations

When the frequency varies (but there are no phase-jumps), similar results are obtained. In Fig.III.6.19 the simulation results when the frequency varies from 50 Hz to 55 Hz are depicted. As it can be observed, the worst results are given by the mPLL, followed by the DSOGI-FLL and the DSC. The WLSE provides very good results. The sequence magnitude and phase estimation errors obtained in this simulation come from two sources:

– The mPLL and the DSOGI-FLL have closed-loop structures and the frequency estimation is not instantaneous. An erroneous frequency estimation impacts on the feedback of the

phase-angle in the mPLL and on the location of the bandpass filter in the DSOGI-FLL. The respective frequency estimations of the mPLL and of the DSOGI-FLL are plotted in Fig.III.6.20.

– As the frequency increases, the number of samples included in a grid-period is not an integer number so estimation errors occur. That is why the DSC technique is impacted by grid variations.

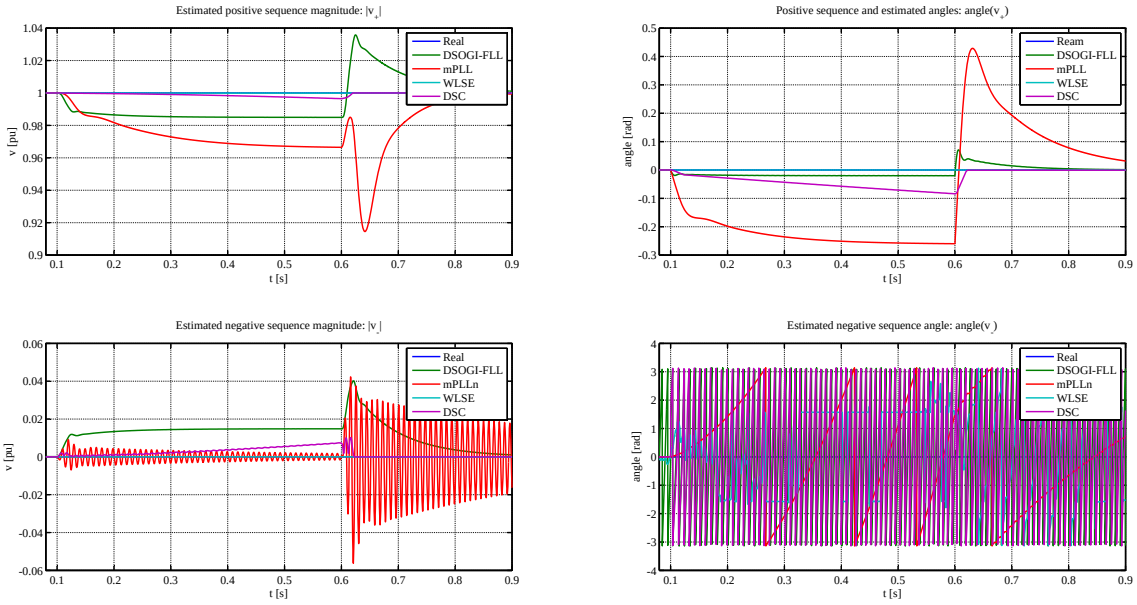


Figure III.6.19: Comparison between sequence extraction methods with: (i) No harmonics, (ii) No sequence magnitude changes, (iii) No phase-jumps (iv) frequency variation (5 Hz in 0.5 s).

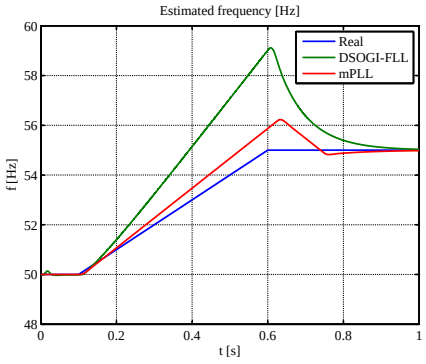


Figure III.6.20: Frequency estimation by DSOGI-FLL and mPLL.

5.3. Simulation conclusions

The preceding simulations demonstrate that each of the selected ISC extraction techniques present advantages and disadvantages. The most relevant characteristics of these methods are

summarized in Table III.6.3 and, as it is observed,

- The global features of the **double m-PLL** are good but it does not correctly estimate the symmetrical sequences. This is a very important point and thus, the mPLL may not be a good choice as ISC extractor. However it must be mentioned that this approach can be improved by including the decoupling procedure presented in [174, 148].
- Globally, the **DSOGI-FLL** provides very good results except when the grid is very distorted. However, if the response time of the extractor is not an important issue, this technique is very interesting because it includes a fast and accurate frequency estimator. Moreover, its discrete implementation does not present special difficulties.
- The **WLSE** also provides very good results. The main drawback of this technique is that the frequency estimation is not integrated. The authors of [172] propose a frequency estimation technique but, unfortunately, it does not work well when the frequency variations are large. If the proposed technique is further improved, the WLSE could become a very powerful ISC extraction method.
- Similarly to the **DSC** one of the main drawbacks of the DSC is that it needs an external frequency estimator. On the other hand, when the number of samples contained in a grid period is not an integer number, the DSC presents estimation errors. Nevertheless, averaging techniques exist to reduce these estimation errors due to the asynchronous sampling frequency [166].

6. Conclusions

Synchronization techniques and ISC extraction methods constitute a very important function in VSC control structures. Although three-phase or one-phase synchronization techniques are always needed, ISC extraction methods are not always essential. The need of ISC extraction methods depends on the type of control structure that is implemented.

This chapter has first presented an overview of different synchronization techniques and ISC extraction methods. In general, synchronization methods can be divided into **open-loop** and **closed-loop** solutions, depending on whether the phase-angle is retro-feeded or not. The main difference between both families is that closed-loop methods can naturally adapt to frequency variations while open-loop methods need external frequency estimators.

One of the most relevant issues in synchronization and sequence extraction techniques is the ineluctable trade-off between a good filtering characteristic and a fast convergence time. It has been demonstrated that it is not possible to obtain high dynamics and high disturbance damping capability. And, the studied cases (mPLL, DSOGI-FLL, WLSE and DSC) corroborate this statement. If the voltage grid is not distorted, the DSC technique yields the fastest convergence time (5 ms) and, the DSOGI-FLL and the WLSE can be as fast as 10 ms. The mPLL needs a minimum convergence time of 20 ms at any conditions. However, if the grid

voltage is very distorted, non of the techniques can go below 20 ms. The comparison between the selected techniques has been summarized in Table III.6.3.

One conclusion that can be drawn from this study is that, if the grid is very distorted, a sequence-based control technique may not be adequate due to the long delay-times ($\approx 20\ ms$) introduced by the sequence extractors. The only possibility is to design a dedicated control structure that takes into account the introduced delays. On the other hand, if the grid is strong and it is not distorted, a DSC could be perfectly used in a DVCC control structure.

Research on synchronization methods is rather mature and the assortment of possibilities is very large. Another conclusion may be that, acknowledged the advantages and disadvantages of each method, it is up to users to decide which is the method that better fits their needs.

Table III.6.3: Selected ISC extractors: comparison table

Aspects	Double m-PLL	DSOGI-FLL	WLSE	DSC
Nb. of design parameters	2	2	3	0
Convergence time (ideal conditions)	20 ms (with filter)	$\approx 10\ ms$ (without filter)	$\approx 10\ ms$ (without filter)	5 ms (without filter)
Convergence time (distorted conditions)	• Without filter: - • With filter: 20 ms	• Without filter: $\geq 100\ ms$ • With filter: $\approx 30\ ms$	• Without filter: $\geq 100\ ms$ • With filter: $\approx 30\ ms$	• Without filter: - • With filter: 20 ms
Accuracy of the estimations	POOR (oscillations)	• GOOD without filter (sensitive to Δf) • POOR with filter (estimation errors)	GOOD	GOOD (but sensitive to Δf)
Frequency estimation	Integrated	Integrated	Not integrated (possible)	Not integrated (possible)
Discrete implementation	Needs integer number of samples in a grid period (can be solved	-	-	Needs integer number of samples in a grid period (can be solved

Chapter III.7

Practical implementation and simulation issues

All along this manuscript simulations in Simulink and SimPowerSystems have been alternated with the aim of displaying one particular feature or the other. The objective of this lines is to describe the differences between *Simulink* and *SimPowerSystems*, to explain the encountered difficulties and to clarify which simulations have been done in each case.

1. Simulation approaches: Simulink and SimPowerSystems

Usually, when the performance of a control structure is to be validated, the most judicious procedure is to validate it by means of a set of different simulations starting from the most idealistic case to end in the case that is closest to the reality.

The **Matlab/Simulink simulation tool** provides a very flexible and powerful environment to simulate *mathematically-expressed* models. The simulations in Matlab/Simulink are the best starting point to validate a model and its control because the models correspond exactly to the mathematical expression given by the user. Moreover, it is possible to subsequently increase the mathematical complexity of these models including aspects such as delay-times. In the case where switching converters and power-electronic devices are present, Matlab/Simulink does not enable (at least in an easy way) the modelling of these switching devices. For this reason, in Matlab/Simulink, switching converters are modeled by a controllable continuous voltage source. The simulations in Matlab/Simulink can be regarded as the first step in the validation of a control structure.

Then, specialized simulation **Matlab toolboxes such as SimPowerSystem**, enable the construction of the model based on *physical* components. In *SimPowerSystems*, switching converters can be modelled either as ideal voltage sources (as in Simulink) or either as real switched sources. So, the next step after the validation on Matlab/Simulink is to build the equivalent model in SimPowerSystems using ideal voltage sources. Then, if the SimPowerSystem model that uses ideal voltage sources is ratified, the ideal voltage sources can be substituted by *real* voltage sources. In this last stage, it is important that all the simulation parameters (e.g. sampling times, switching frequencies etc.) are the closest to the reality as possible.

After validating all the simulation stages, and if the results are satisfactory, the control structure must be validated in a laboratory prototype and, finally, in a real implementation. The

whole procedure is depicted in Fig.III.7.1.

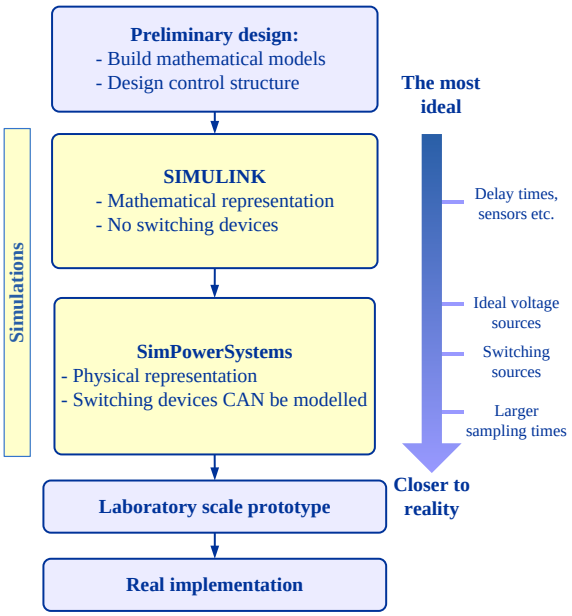


Figure III.7.1: Simulation procedure for control structure validation.

2. Encountered difficulties

In this work, the first stage of the validation, which is the simulation in Simulink, has been performed for all the analysed cases. This is, simulations have been conducted with (a) the UPLC connected to a RL line, and (b) with the UPLC connected to a cable. Moreover, two control approaches have been tested in normal, unbalanced, and sagged conditions: (i) the vector control oriented to the positive SRF, and (ii) the dual vector control.

The second stage of the validation, which is the simulation in *SimPowerSystems*, has successfully been implemented in a UPLC connected to a RL line, also for the above-mentioned control approaches, and under balanced and unbalanced conditions. However, further effort must be commited to the simulations of a UPLC connected to a cable in *SimPowerSystems*. In Table III.7.1 a summary of the simulations that have been performed is provided.

As it can be observed, the simulations of the UPLC and the cable could not be implemented in *SimPowerSystems*. The encountered obstacles are the limited discrete time of the simulations, the chained structure of the cable, and the characteristics of the sequence extractors:

– **Discrete sampling times.**

  The switching times of the converters and the sampling times of the simulation limit the performance of the selected control type. As it was discussed in section 3.3.1., when delay times exist, a phenomenom called chattering can occur. This problem can be solved by substituting the signum function by other smoother functions. The problem is that, in

Table III.7.1: Performed simulations

	Simulink: • Ideal converters • Ideal measurements and sequence extractors	**SimPowerSystems:** • Real converters • Real sequence extractors
UPLC+RL	✓	✓
UPLC+Cable	✓	×

this case, the chattering dissapears but an steady-state error occurs.

Two solutions can be expected: (i) either to reduce all the sampling and switching times, which is not realistic, or (ii) to improve the control in order to migrate towards discrete structures without any problem.

– **The chained structure of the cable.**

The chained structure of the cable aggravates the problems derived from a discrete sampling time. If the inner controllers of the global trajectory generation control do not work well (chattering or tracking errors), it is to be expected that the overall control will not work well.

– **The sequence extractors.**

As it has been analyzed in the preceding chapter, the sequence extractors yield a minimum delay time of 5 ms (in the best of the cases) when the grid-voltage conditions are ideal. If the grid is very distorted, the delay time can increase to 30 ms-100 ms. These delay times are too large for the control structure and should be considered in the design stage.

Part IV

General Conclusions

Chapter IV.1

Conclusions

The UPLC is a complex device that must be integrated into a complex power system. Thus, before deciding upon its installation, it is essential to perform an all-embracing analysis to:

- Evaluate whether the location of the UPLC is the appropriate or not. This can be done by checking that the goals defined by the system-operator can be fulfilled, that the stability and the losses of the system are satisfied in all conditions, that it is possible to lay an interconnection cable in that zone etc.
- Define the higher-level control algorithms and the communication structure between the system operator and the device.
- Based on the customer requirements and the standards currently in force, identify the functions that the device must/can address (in steady-state, in transient, and in degraded operation mode) and all the range of conditions to which it will be confroted.
- Make a preliminary design of the device in order to assess the cost, the required components, topologies and materials.
- Select a convenient control structure that will be able to achieve the required functions with the specified performances and validate it in simulations or prototypes.
- Estimate the cost of the solution and anticipate the challenges and the risks that can be encountered.
- Compare the UPLC-based solution with other possible solutions such as the MVDC.

Such a comprehensive analysis requires an important research effort at different levels of abstraction. In the literature, some of these questions have been tackled giving rise to a myriad of publications, both on UPFC and on UPQC. Some publications model the UPFC as an ideal actuator and propose *advanced* power-system-level control approaches based on linearized (e.g based on Phillips-Heffron models) or nonlinear methods. Other types of publications have dealt with the local control of the UPFC but, in general terms, they assume a balanced grid, a connection to a L or RL line, and a pretty ideal component modelling (e.g. without filters, not considering transformer couplings and grouding types etc.).

The vast volume of research articles that have been published along the last decades could indicate that the UPFC/UPQC/UPLC is a mature static power electronics device that is largely deployed worlwide. However, a closer look at the existing devices shows that, from the late 90s and up to now only three UPFC have been installed in the world. When looking at

UPQC a similar thing occurs. So far, just one company that commercialises UPQC has been found [175].

This low number of commissioned projects and commercialised products suggests that there are practical barriers that limit the installation of UPFCs and UPQCs around the world. Charmed by the theoretical potential of UPLC for interconnecting MV distribution grids while addressing power quality phenomena, but seriously thrilled by the low rate of real deployments, one of the objectives of this work has been to provide a critical view on the real interest of using a UPLC for the interconnection of MV distribution grids. The extracted conclusions are summarized in the following points.

1. Capability of the UPLC of addressing multiple functions. Can the UPLC tackle power-flow and power-quality functions simultaneously?

From a theoretical point of view the UPLC can address power-flow and power quality functions simultaneously. Notwithstanding, not all the functions have the same relevance and thus, their impact on the design characteristics, size, and control of the UPLC must be evaluated in order to decide upon their implementation:

(i) Since the UPLC is used for interconnecting two distribution grids, the **primary function of the UPLC must necessarily be power-flow control**.

(ii) After power-flow control, the **secondary objective may be voltage regulation at the shunt-side PCC** in steady-state conditions. The magnitude of the voltage $\mathbf{v_1}$ shall be controlled such that it is in the normative range ($\pm 10\% V_n$), balanced, and harmonic free. In this case, it is the shunt-side converter that provides the necessary reactive power to regulate the voltage at the PCC.

An *active* control of $\mathbf{v_1}$ can only be performed if the size of the shunt-device does not increase beyond unacceptable limits (these limits are defined by the maximum cost that the customer is ready to pay). The size of the shunt-device will depend on factors such as the strength of the grid at the PCC and the nature of the distortion source. If the UPLC is connected close to a HV/MV substation, for instance, the grid at the PCC will be stronger than if the UPLC is connected at the end of a long distribution feeder. And when the grid at the PCC is strong, it requires higher shunt-side converter ratings to regulate the voltage at the PCC.

Besides cost and volume, an additional shortcoming of having high power ratings at the shunt-side is that the switching frequency must be lowered to avoid excessive switching losses and thus, the active filtering capability of the device is lowered. The only way of guaranteing filtering capability at higher powers is to switch to multilevel converter topologies.

(iii) Besides steady-state power-flow control and voltage regulation, the compensation of transient disturbances is also possible but, depending on the magnitude of the disturbance, **the simultaneous compensation of sudden perturbations and power-flow control may not be interesting**. This is the case of merging power-flow and voltage-sag compensation capabilities, for example.

If a sudden voltage sag occurs, the dimensions of the shunt-side converter must be significantly highered (comparing to the steady-state voltage regulation case) and, depending on the study-case, it may be too expensive to compensate for voltage-sags by the shunt-converter.

Another possibility is not to compensate for the the voltage sag *actively* but to try to inject a series voltage so the receiving-end does not perceive the voltage sag. This second alternative is also challenging from the design point of view because the series converter, transformer and associated filters must be designed to work at very different operating points. Under nominal conditions the converters would work at very low modulation indexes that require large filters and, during sudden voltage sags, the modulation index would increase to the maximum.

(iv) For steady-state power quality compensation, this is, for current/voltage harmonics and unbalance compensation, two aspects must be considered:

- The size of the converters increases by a ratio of $\sqrt{1+THD_x{}^2}$, for voltage/current harmonic compensation, or by $\sqrt{1+(\frac{X^-}{X^+})^2}$ for voltage/current unbalance compensation (the variable X stands for voltage or current).
- The power of the converter must be low enough to allow for high switching frequencies. Usually, active filters connected to MV levels have an installed power of few MWs and present multilevel structures that commutate at frequencies between 1.2 kHz and 5 kHz [85].

The preceding lines discuss the technical possibilities of merging power-flow and power quality functions in the same device. But, besides the technical aspect, it is also important to assess whether there is an interest from the utility-side to install devices that offer these functions. It must be noted that active power filters, STATCOMs, and DVRs are typically connected in the neighourhood of a polluting/sensitive load or generator. Usually custom-power apparatus are located where there is a need and not anywhere between two distribution grids.

Power quality compensation (performed by the shunt-side of the UPLC) makes only sense when the source of the power quality disturbance is connected to the same PCC as the UPLC, it is well known, and there is a real interest by the system, power-plant or industrial-site operator to compensate for the originated perturbations. For example, a wind-farm that that needs to comply with the grid-code imposed by the distribution operator or an arc-furnace that generates flicker.

However, it must be also considered that the polluting-client is not the only client connected to that PCC. As it can be observed in Fig.IV.1.1, the power-plant or industry will not be the only load connected to the same bus, there will also be other branches leading to other grid ramifications. These ramifications will also contribute to the deviations of $\mathbf{v_1}$.

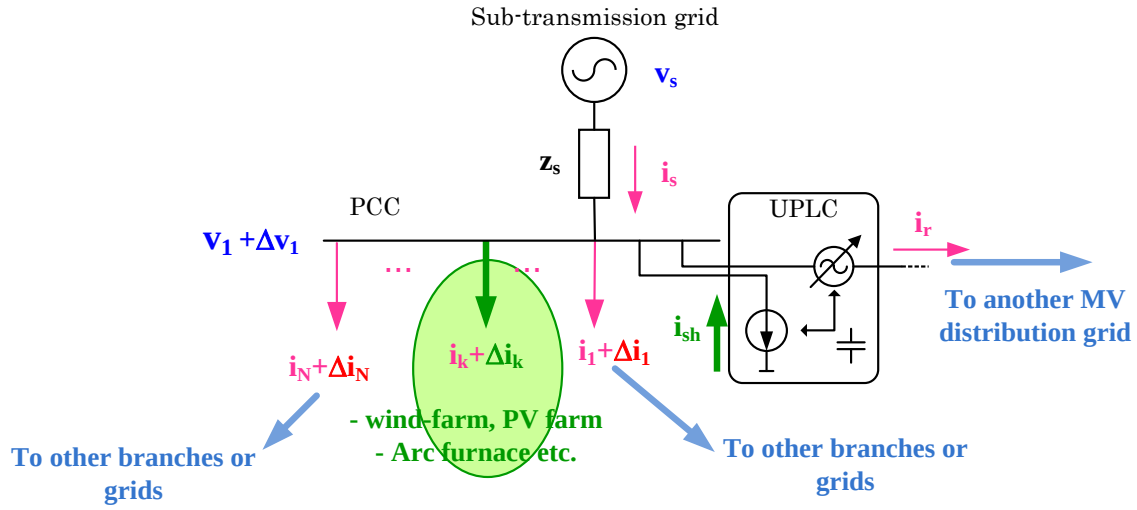


Figure IV.1.1: Detail of the shunt-side connection of the UPLC.

Thus, considering that not only the client that is directly connected to the PCC reduces the power quality level, who would be in charge of paying for the cost of improving the quality level at that PCC? The client that is directly connected to that PCC or the distribution system operator? Considering that the UPLC would need to compensate for all the disturbances coming from all the feeders connected to the PCC, and considering that the dimensions of such device could be rather high, is the distribution system operator ready to pay for a UPLC that guarantees the power quality compensation function?

After evaluating these questions it has been concluded that, unless there is a real need of improving the power quality level at the PCC of the UPLC *globally*, it is more interesting to compensate locally for the power quality disturbances generated by each polluting client.

2. Sizing and design of the UPLC.

The sizing and design of the UPLC is closely linked to the the functions that are to be attained, to the performances that are expected, and to the specific conditions of the surrounding grid. The sizing calculations made in this work are just oriented to the steady-state power-flow control of the UPLC, but the reflexions that have been made during the sizing procedure have lead to important conclusions and observations:

- The power flowing through the interconnection line cannot be arbitrarily be augmented due to the thermal limitations of the interconnection. This means that, in steady state,

the magnitude of the injected series voltage is limited to the maximal current that the interconnection line or cable can stand.

- The grounding type of the distribution grid has an impact on the wiring and coupling structure of the UPLC. In solidly-grounded systems a four-wired structure can be used instead of the traditional three-wire structure.
- Moreover, depending on how the homopolar components are handled, it is necessary to define whether the transformers and the filters are connected in delta or star (with or without grounding), whether the DC-bus is splitted in two equal capacitors, or whether four-legged converters are used.
- Regarding the filters the following considerations must be accounted for:
  - The **series-side filters** must smoothen the voltage at the output of the converter in order to inject a clean voltage in series with the line. Two options are possible: to use a line-side filter or to use a converter-side filter. Usually the second option is preferred because it is closer to the harmonic source, it is usually located a the low-voltage side and the harmonics do not enter the transformer. The main drawback of converter-side filters is that the voltage drop and phase-shift must be compensated.
  - The **shunt-side filters** can be L or LCL filters. The design of the L filter is simpler than LCL filter but there is a trade-off between the value of the filtering impedance, its filtering characteristic, the voltage drop, and the transformation ratio of the transformer. If a high value of the inductance is chosen, the filtering characteristic is better but the converter saturates at certain operating points, requiring a lower voltage value at the secondary of the tranformer.
- As for any other active power filters, the nominal voltage and current ratings of the UPLC must be increased by a multiplying factor if current/voltage harmonics and unbalances are to be compensated (in steady-state). As mentioned above, this factor depends on the total harmonic distortion and the unbalance rate that must be compensated. It is also important to note that the harmonic filtering capability of the device depends on the switching frequency of the converter, which cannot go beyond the limit imposed by the switching losses (and thus, the cooling capability).

3. Control structures for operating the UPLC in distorted environments.

- The proposed control structure, that consists of a **higher-level trajectory generation strategy coupled to Lyapunov-based controllers**, has shown to provide good results (i.e convergence speed, tracking error, robustness against transient disturbances etc.) when averaged voltage source models are used. But, when the sampling period is highered or switching converters are considered, the performed simulations have shown that it is

not possible to higher the gains of the controllers above a certain threshold without suffering from chattering.

A solution to avoid chattering is to replace the *sign* function by a softer function such as the *saturation* function. Unfortunately, the use of the *saturation* function reduces the chattering but creates a steady-state error. If only one controller was used, a steady-state error could be acceptable depending on the application. However, since the controllers are chained, the steady-state errors propagate through the chain inducing an unacceptable behaviour.

When the grid voltages are balanced, the voltage and current projections are constant so the controller gains do not need to be large. However, when unbalances occur and a SRF-based control structure is used, a second order oscillation appears in the projected voltages and currents. As a result, it is necessary to increase the controller gains:

- In the case of a UPLC connected to a RL line, and when switching converters are used, it is possible to increase the gains until a certain limit. Since the gains cannot be increased as much as necessary, the tracking performance gets affected. If the converters are modelled as continuous voltage sources, it is possible to reduce the sampling time in order to higher the gains and obtain a perfect tracking, but this solutions does not solve the real problem.
- In the case of the UPLC connected to a cable, the problem is more critical because there are too many chained elements and it is not possible to increase the gains without getting an undesired behaviour.

- The analysis of single and dual vector-oriented control structures under unbalanced conditions has shown that, assuming that the controllers and the measurement systems are ideal, both approaches are equivalent. However, the reality is that:

  a.- Dual or single SRF oriented control strategies need controllers that are able to track oscillating signals. In literature, resonant controllers have been chosen for this purpose. The problem of resonant controllers is that it is necessary to make them frequency-adaptive. In this work, the Lyapunov-based controller has been used with the same aim but, as abovementioned, it was not possible to increase the controller gains sufficiently in order to yield a satisfactory behaviour. If the Lyapunov-based controller is further improved, it can be a very good candidate to replace resonant controllers.

  b.- Dual sequence-based control structures do not need controllers that can track oscillating signals but, they require fast sequence-extracting methods.

- The evaluated synchronization and sequence extraction methods have shown that there is always a trade-off between the robustness and the dynamics of the selected method. As it has been observed in Chapter III.6, the fastest sequence extracting method that exists, the DSC, has a minimum delay time of $5ms$ when no harmonic distortion nor frequency

changes are present in the grid. If the grid is strongly polluted and the frequency can vary, sequence extracting methods present an approximate delay time of $30ms$. This means that, if sequence extracting methods are used, these delays must be taken into consideration in the synthesis of the control.

4. Comparison between the UPLC and the MVDC.

The **comparison between an UPLC and a MVDC** has demonstrated that, in general terms, the MVDC presents more advantages than a UPLC. However, there are some particular conditions under which the UPLC can be dimensioned to be substantially smaller than the MVDC (i.e. small phase-angle difference between interconnected grids). As a consequence, the major advantage of the UPLC with respect to the MVDC would lie in the difference of size. A second advantage of the UPLC with respect of the MVDC is that it can be bypassed.

Chapter IV.2

Future work perspectives

1. Merging power-flow and power-quality functions.

In this work a priority has been given to the control of power flow considering that the interest of compensating for power-quality is not evident. Specially for transient perturbations and steady-state power quality compensation when the range of voltage and power increases. It must be observed that the UPLC will probably be connected to a strong PCC (near to a HV/MV substation), requiring high installed powers.

As a future work perspective, and if the price of the device does not constitute a drawback, it is possible to extend the design of the UPLC to include advanced converter architectures such as modular multilevel topologies. The fact of migrating towards multilevel topologies presents a double advantage:

- it allows to work at radically different modulation indexes without degrading the quality of the voltage output and with minimal filter requirements.
- it increases the equivalent switching frequency of the converter, enabling the compensation of higher order harmonics.

Additionally, regarding the interest of joining power-flow and power-quality functions, another future work perspective is to meet power utilities in order to unveil the interest of merging these functions and to find realistic case studies.

2. Sizing and design of the UPLC.

Due to its complexity, there are many aspects in the design of the UPLC that can be further analyzed and studied. All depends on the functions that must be guaranteed, the performance that is expected, the external conditions and the price that the client is ready to pay. Some proposals for future work are:

- To study the use of one single-phase UPLC structure per phase. This would enable the control each of the phase separatately.
- The replacement of the L-type filter of the shunt-side by a LCL-type filter. This change would reduce the voltage drop at the filter impedance enabling to higher the voltage at the secondary of the transformer. Moreover, it would reduce the sharp voltage derivatives

at the secondary of the transformer. Furthermore, an adequate procedure to estimate the filter values must be developped.

- The analysis of the series transformer (e.g. the saturation phenomenon) and define the characteristics that the series transformer must satisfy.
- The study of different VSC topologies (i.e. multilevel topologies) and a comprehensive design of each of the VSC devices (number and type of switches in series/parallel, evaluation of losses, type of cooling, volume etc.).
- The study of the bypass switch. What characteristics should it have? How must it be operated? How should it be rated? What would be its volume and cost?
- What should be the protections of the device like?
- The evaluation of the cost and the volume of the whole solution.

3. Control structures for operating the UPLC in distorted environments.

Regarding the control of the UPLC the following future work is proposed:

- Considering the problem of increasing controller gains when working in a discrete environment, **the Lyapunov-based controllers must be adapted in order to work in a discrete environment**. This implies that discrete models of the UPLC must be developped and an according control type must be designed.
- In this work the modelling and the control of the UPLC has been performed based on dq coordinates. The main advantage of using dq coordinates is that, when the systems is perfectly balanced, the projections of voltages and currents in the SRF are constant and thus, the controllers just need to deal with constant signals. However, it must be taken into account that the accuracy and robustness of the selected synchronization method will influence the reliability of the dq projections.

  As a future work perspective, the **use of a $\alpha\beta$-type static frame is proposed**. The advantage of an $\alpha\beta$ frame is that no synchronization method is needed to synthetize the voltages and currents of the feedback signals. Of course, synchronization and sequence extracting techniques will always be required for the reference generation under distorted conditions, but their dynamics is not so critic as when the signals are used for feedback.

  The challenge of using an $\alpha\beta$ frame stands in the type of used controllers, which must be able to track alternating signals. It is therefore very important to develop discrete and robust controllers that are able to track alternating signals.
- In this work, synchronization and sequence extracting techniques have been considered ideal in the case of the UPLC connected to a cable. However, if dual sequence based

control structures are used, it is necessary to integrate the delay times introduced by the sequence extracting modules in the controller design. The consideration of the delay introduced by sequence extracting techniques in the control design of a UPLC connected to a RL/cable shall be investigated in future work.

- The minimization of the oscillations of the DC-link when unbalances occur is also an issue that can be further improved. In this work, the classical oscillation minization methods used in drive applications have been applied with the difference that, in drive applications, the demanded power is constant. In the case of a UPLC, if an unbalance occurs, the power demanded by the series-side will also have an oscillating component. The improvement of this aspect could also constitute a future work subject.
- Regarding synchronization and sequence extracting methods it would be very interesting to extend the study that has been made in this PhD to the main existing methods, and to complete it with a true implementation. This would allow to have a comparison of the main synchronization trends under the same study conditions.

4. Simulations.

- In order to verify that the designed structure and the control of the UPLC are correct, dynamic simulations, that consider a wide range of operating points, must be performed. In the frame of this PhD, static simulations have been done using different static power-flow simulation tools (POWERWORLD and AMPL) but, it is considered that the study must be extended to dynamical simulations. It is worth mentioning that, in order to perform simulations of power systems that contain power-electronics apparatus powerful simulation tools are needed (e.g. real-time simulators).
- Additionally, in relation with the dynamical simulation of a UPLC inserted in a power system, it is also important to develop higher-level control algorithms (distributed or centralized) that will provide the power and voltage references to the UPLC. These algorithms could be based on optimizing different grid parameters. For example, minimization of voltage deviations, minimization of losses, avoiding saturation of critical transformers and lines, etc.

5. Comparison between the UPLC and the MVDC.

The size of a UPLC is smaller than a MVDC when the transmission angle between the interconnected grids is below a certain threshold, as it has been evaluated in section II.3.2.5.. However, for this comparison only the relationship between the active powers flowing through the DC-links of the UPLC and the MVDC has been evaluated. Thus, the presented analysis shall be mainly considered as an indicator rather than a definitive conclusion.

It could be interesting to make a component-by-component comparison between both devices.

This comparison could evaluate the difference in price, volume, effiency, reliability, and performance between the UPLC and the MVDC. This comparison is not possible without a deep evaluation of the MVDC. It is therefore suggested to perform an evaluation of the MVDC similar to that performed in this PhD for the UPLC.

List of publications

Journals

[1] **M. Boyra**, G. Bergna, J.-L. Thomas, "Les technologies de liaisons à courant continu pour l'interconnexion des réseaux électriques du pourtour méditerranéen, Le rêve de Thomas Edison se réalise ...", *Revue de l'Electricité et de l'Electronique (REE)*, no.5, pp. 38-57, November 2011.

[2] **M. Boyra**, J.-L. Thomas, "A review on synchronization methods for grid-connected three-phase VSC under unbalanced and distorted conditions", *EPE Journal* (To be submitted)

International conferences

[4] **M. Boyra**, J.-L. Thomas, A. Benchaib, "Robust control of UPFC for MV distribution grid interconnection under unbalanced conditions", *14th European Conference in Power Electronics and Applications (EPE'11)*, Birmingham, UK, August 30-Sep. 1, 2011.

[5] **M. Boyra**, J.-L. Thomas, "A review on synchronization methods for grid-connected three-phase VSC under unbalanced and distorted conditions", *14th European Conference in Power Electronics and Applications (EPE'11)*, Birmingham, UK, August 30-Sep. 1, 2011.

[6] G. Bergna, **M. Boyra**, J.H. Vivas, "Evaluation and proposal of MMC-HVDC control strategies under transient and steady-state conditions", *14th European Conference in Power Electronics and Applications (EPE'11)*, Birmingham, UK, August 30-Sep. 1, 2011.

[7] G. Bergna, **M. Boyra**, J.H. Vivas, "Novel control strategies of Modular Multilevel Converters (MMC) - An evaluation and comparison of control and modulation scheme", *CIGRE International Symposium on The electric Power System of the Future*, Bologna, Italy, Sep. 13-15, 2011.

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Appendices

OUTLINE OF APPENDICES

On the one hand, appendices A, B, and C represent an interesting compendium of concepts that have been collected during this PhD. The presented subjects provide complementary information in form of book chapters in order to facilitate the understanding of certain parts of the PhD manuscript.

- **Appendix A** provides a general review on static power electronics devices that are connected to the electric power system, this is, FACTS and Custom Power.
- **Appendix B** deals with fundamental power engineering concepts such as representation frames, symmetrical components or power theories. A short section including the frequencies induced from PWM modulation is included as well.
- **Appendix C** describes some basic synchronization methods that can be helpful to understand Chapter III.6.

On the other hand, appendices D and E provide some additional information on the study cases presented during the PhD manuscript.

- **Appendix D** presents the MV benchmark model that has been chosen and the changes that have been made in order to reduce the number of nodes. Some screenshoots corresponding to the exercise performed in Section II.3.3. are also illustrated.
- **Appendix E** details different procedures that have been followed during the modeling and design stages of the UPLC (e.g. per-unit conversion, filter calculation etc.) and provides diverse values obtained from these methodes, from standards, and from calculations (e.g. model matrices, parameter values etc.).

Appendix A

Power electronics in electrical power systems

In this PhD the UPLC and the MVDC have been proposed as suitable devices for distribution grid interconnection. This proposal would have not been possible without a prior analysis of the existing grid-connected static power electronic devices. Appendix A presents a complete overview on FACTS and Custom Power devices that could perfectly be considered as an introduction (or complementary information) to Part II.

1. Introduction

The evolution of power-electronics converters for electric grid applications is closely related to the state-of-the art of power semiconductor technologies, available manufacturing technologies, and existing topologies (multilevel converter topologies, in particular). From the 50s to

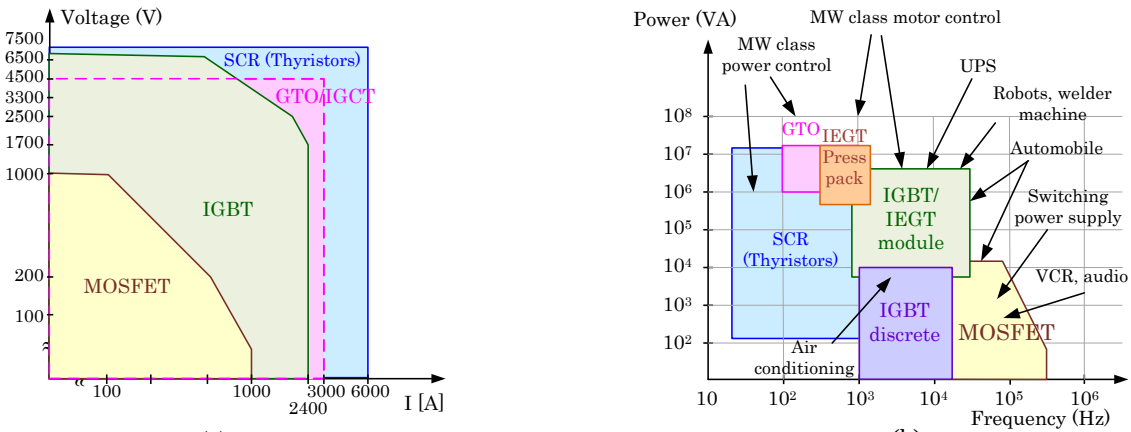


Figure A.1: (a) Voltage and current semiconductor limits (from [176]) (b) Power and frequency ranges of semiconductor applications (from [177]).

the 70s mercury-arc valves, the predecessors of modern solid-state switches, were largely used. However, this technology had several technological limitations and, during the 70s they were fast replaced by thyristors, which offered a higher reliability, lower cost, stronger nature and lower maintenance. Thyristors were only conceived for line-commutated applications and, during the 80s, fully-controlled solid-state switches emerged: GTOs (Gate Turn-Off Thyristors) and IGBTs (Insulated Gate Bipolar Transistors). The difference among GTOs and IGBTs

was in the technology (the GTO is based on thyristor technology while IGBTs are based on transistor technology), and in their voltage and current ranges. In general, GTOs were used in higher power applications while IGBTs were reserved for lower power applications. Notwithstanding, during late 90s a new age bloomed with the arrival of IGCTs (Integrated Gate-Commutated Thyristor) and HV-IGBTs (High Voltage-IGBTs), which enabled the transition towards even higher voltage and current ratings [178, 179]. Power and frequency ranges of different semiconductor devices can be observed in Fig.A.1.

Thanks to the constant development of power semiconductor devices, the presence of power electronics in electric grids is progressively increasing. The applications of power-electronics-based apparatus are multiple and can be found at any power system levels: at the transmission level and at the distribution level (Fig.A.2).

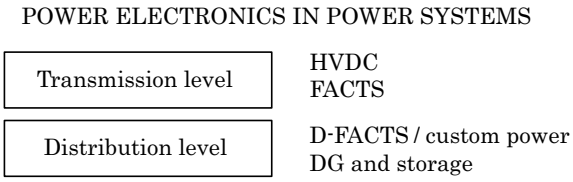


Figure A.2: Power electronics in power systems

Power electronics at transmission level

The electric power system is a unique system that needs an all-instant balance between generation and load. In order to preserve an exact equilibrium at every moment, the power system is continuously being reconfigured by system operators. Traditionally, the electrical power system has been operated by means of mechanical actuators such as tap changers, phase shifters, and discrete reactors and capacitors. However, the main drawback of mechanically switched actuators lies in their slow dynamics, which has induced power engineers and system operators to work with large security margins and redundancies. Moreover, it is not adviced to often use mechanical solutions because they tend to wear out quickly [180, 181].

Today, the electrical demand worlwide is persistently growing, but generation and transmission assets do not expand at the same rate due to the difficulties to acquire new rights-of-way and to update existing assets. Besides, due to deregulation of electric markets, open access shall be given to every network participant. As a result, transmission networks are overloaded, and the availability and reliability of electrical power are reduced. In some regions, the interconnection of neighbouring grids can solve some of the arising problems but this is not always the case. In particular, technical problems such as power-flow, system oscillations and inter-area oscillations are expected in large AC systems with synchronous connections. And, if the systems include long distance transmission, additional voltage and stability problems can be observed. Furthermore, when the synchronous system is very large, the advantages of the interconnection diminish [42].

Static power-electronics converters provide an interesting alternative to mechanically switched

actuators because they do not have any moving counterparts, so they do not wear easily, they proceed at high speeds, and they can tackle applications where traditional technologies are incompetent (e.g. power transmission along long lines, connection of non-synchronized grids or power enhancement). At transmission level, HVDC and FACTS are the most popular power-electronics-based apparatus. The main role of HVDC and FACTS is to enchance controllability, and increase power transfer capability and stability.

Power electronics at distribution level

At distribution level, three types of power-electronics equipments can be found:

a) Equipment necessary to connect Distributed Energy Ressources (DER) and storage to the grid. For example, converters for wind-turbines or DC-AC converters for photovoltaic pannels [9, 182, 183].

b) Consumer-side electronics. For example, rectifiers in an aluminium smelter plants or arc-furnaces.

c) Custom-power equipment used for compensating or mitigating power-quality phenomena.

The first two categories will not be further developed in this chapter because they are considered as a part of generation and load technologies. Reversely, a full section is devoted to custom-power.

In spite of the great potential and numerous possible applications that they offer, power electronics devices are still not broadly used in electrical systems. Some of the barriers observed to a wide development of power electronics apparatus are their high cost, the apprehension of power utilities in regard of their reliability, the lack of long-run experiences, and an insufficient benefit-cost balance . Before making any power electronics deployment decision, system planners should perform a whole battery of studies in order to assess the real interest of power electronics integration: impact studies, new functionalities, architectures, components, integration studies, coordination studies, fault-mode studies, protection system studies etc. [51].

Power electronics devices can be sorted according to several classifications. The following sections explain and describe some major concepts and converter topologies that will serve to give a clear overview of power electronics in electrical grids.

2. HVDC and FACTS

When systems are meshed, as is the case of transmission networks, electric power follows the laws of physics, e.g. current will always follow the lowest impedance path. This fact can lead to a bunch of undesirable effects such as line congestion, loop-flows and stability problems. In order to explain the behaviour of power when it flows through parallel corridors, an illustrative example is depicted in Fig.A.3. In the example, both lines are purely inductive but for one of the lines the impedance value is doubled. Only 1/3 of the power flows through the line

with the highest impedance while 2/3s flow through the line with the lowest impedance. This means that the line with the lowest impedance will tend to be congested (and thus the overal loading will be limited) even if the highest impedance line has still available power capacity. When lines are congested, it might be difficult to ensure that there is a perfect balance between generation and load. Then, saturated lines may provoke secondary effects, such as line-tripping or instabilities, in the grid.

The solution to this problem does not come from adding a new line because this measure would further decrease the impedance of the overloaded line, and the high-impedance line would still be under-used. The solution to this problem is to force the power to flow through the light-loaded line. HVDC and FACTS devices can, indeed, control/impose the current to circulate through a particular line. Moreover, thanks to their high dynamics, they can also be used for damping oscillations, transient and dynamic stability, fault limiting, and voltage stability. Another problem closely related to overloading of interconnected systems is voltage regulation. FACTS devices can also control the voltage at a bus node by injecting or absorbing reactive power locally.

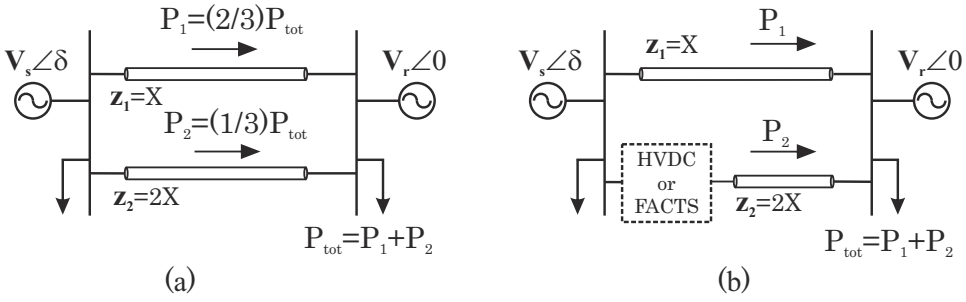


Figure A.3: (a) Two uncontrolled parallel paths (b) One controlled path

But, before going forward, the definition of FACTS according to the IEEE PES Task Force of the FACTS Working Group shall be given: *Flexible AC Transmission Systems (FACTS) are alternating current transmission systems incorporating power-electronics based and other static controllers to enhance controllability and increase power transfer capability.* The High Voltage Direct Current (HVDC) device is not classified as a FACTS because it is not an AC-transmission but a DC-transmission system. Nevertheless, their architectures and control modes are very similar.

Main FACTS families

It must be noted that, the term FACTS is not a single apparatus, but rather a large collection of devices that serve for different purposes. It may be considered that FACTS are composed of basic building blocks that are arranged in different configurations. As shown in Fig.A.4, three main types of FACTS are observed: series-connected controllers, shunt-connected controllers, and combined shunt-series (also known as *universal topology*) controllers. Series-connected controllers inject a variable voltage in series with the line. Shunt-connected controllers inject/absorb a variable current in a point of the line and combined shunt-series controllers are

an association of both options.

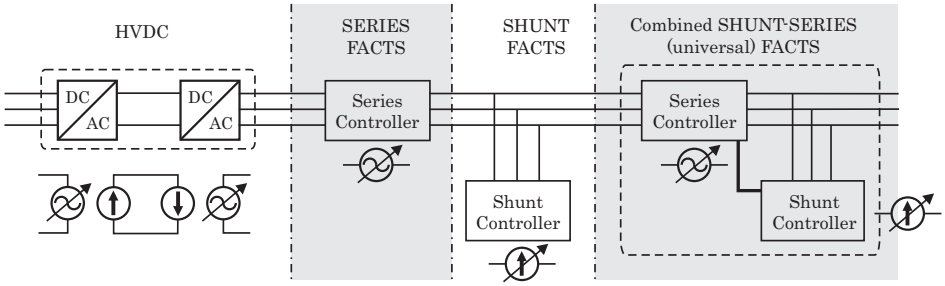


Figure A.4: Main types of FACTS and HVDC

Principles of power delivery

In order to understand how FACTS work, it is helpful to recall some basic principles of power delivery. The explanation is based on the representative example of Fig.A.5. The illustration presents two bus nodes (the sending-end and the receiving-end) linked by a purely inductive line. Both voltages are separated by a transmission angle δ. If no control is performed, the power flowing towards the receiving-end is given by the following equations:

$$\mathbf{S_r} = \mathbf{V_r} \cdot \mathbf{I}^* = V_r \cdot \left(\frac{V_s \; e^{j\delta} - V_r}{jX_L} \right)^* \tag{A.1}$$

$$\mathbf{S_r} = P_r + jQ_r = \left(\frac{V_s V_r}{X_L} \; \sin\delta \right) + j \left(\frac{V_s V_r \; \cos\delta - {V_r}^2}{X_L} \right) \tag{A.2}$$

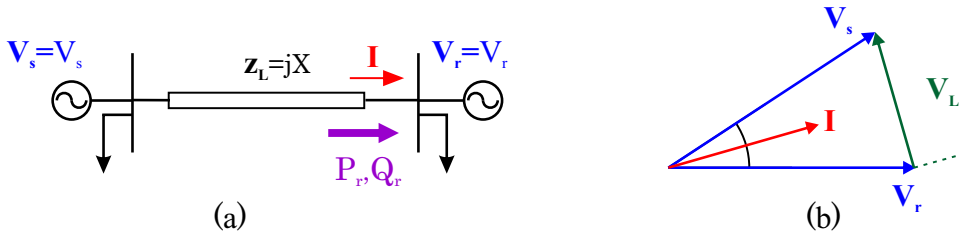


Figure A.5: (a) Purely inductive short-line representation (b) Associated vector-diagram

And thus, for a purely inductive line, (A.3) and (A.4) provide the expressions of the active and reactive powers, respectively.

$$\mathbf{P_r} = \frac{V_s V_r}{X_L} \; \sin\delta \tag{A.3}$$

$$\mathbf{Q_r} = \frac{V_s V_r \; \cos\delta - {V_r}^2}{X_L} \tag{A.4}$$

FACTS controllers act by modifying one or more of the parameters that compose equations (A.3) and (A.4): V_r, V_s, X_L and/or δ. Some FACTS make use of solid-state semiconductor switches to modify the value of the fundamental current that crosses through a capacitor or an

inductor. The obtained effect is equivalent to change the value of that capacitor or inductor dynamically. Other FACTS are based on converters. These converters have the ability of producing a switched voltage or current waveform with custom magnitude and phase angle. The next subsections provide a review and description of FACTS types and HVDC and further explain how FACTS controllers manage to vary these parameters. As it will be later explained in section 4., in this manuscript only voltage sourced converters (VSC) are addressed and therefore, all subsequent drawings that imply converters correspond to VSC.

2.1. Series-connected FACTS

Series-connected FACTS inject a voltage in series with the line in order to induce a change in the current that flows through the line. In principle, all series controllers inject a voltage in series with the line. Even a variable impedance multiplied by the line current, represents an injected series voltage. If the injected voltage is in quadrature with the line current, the series controllers only supplies or absorbs reactive power. In the rest of the cases active power consumption/injection will also be involved.

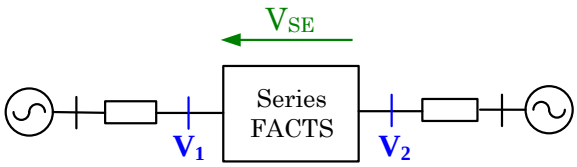


Figure A.6: Symbolic representation of series-connected FACTS

Probably the most simple way of understanding the operation principle of a series-connected FACTS is to assimilate it to a variable reactance. This variable reactance adds to the existing inductive reactance (effective reactance) and influences the value of the line current as shown in (A.5) and (A.6). Depending in the nature of the inserted reactance, the effective reactance can be lower or higher than the original line reactance and thus, more or less current will circulate, respectively. Fig.A.7 depicts a line compensated by a series-connected variable reactance and its associated vector-diagram. From the vector-diagram it is remarked that the insertion of a variable reactance is equivalent to inject a voltage in quadrature with the line. The injected voltage is always proportional to the line-current (where the proportionality constant is, indeed, X_c).

$$\mathbf{I_0} = \frac{\mathbf{V_s} - \mathbf{V_r}}{jX_L} \tag{A.5}$$

$$\mathbf{I} = \frac{\mathbf{V_s} - \mathbf{V_r}}{j(X_L - X_c)} = \frac{\mathbf{V_s} - \mathbf{V_r}}{jX_{eff}} \tag{A.6}$$

The most well-known series FACTS devices are the following:

- **Thyristor-switched Series Capacitor (TSSC) and Thyristor-switched Series Re-**

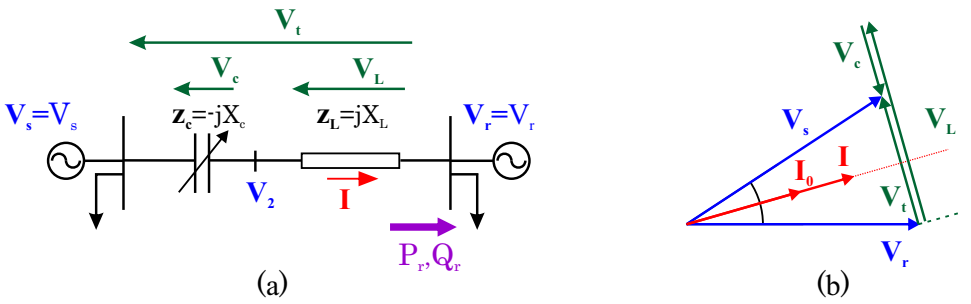


Figure A.7: (a) Variable capacitive reactance in series with the line (b) Associated vector-diagram

actor (TSSR).

As depicted in Fig.A.8, TSSC and TSSR are composed of several capacitances and/or inductances that are connected in series and that are switched on and off sequentially in a stepped manner.

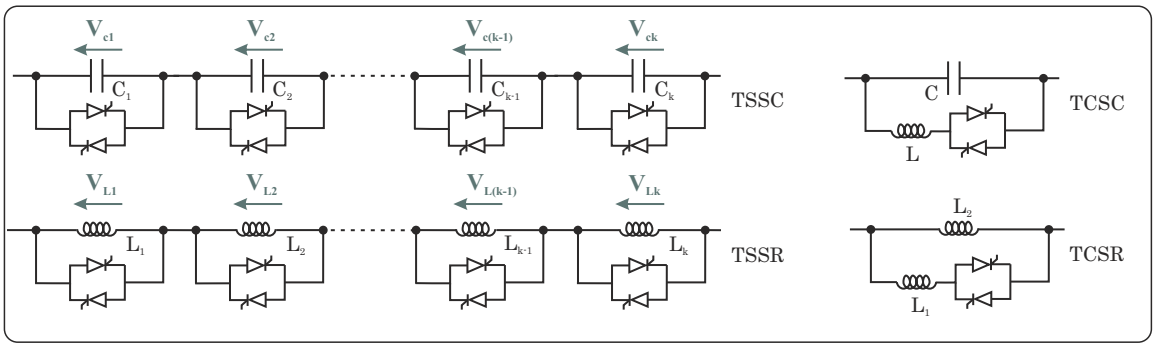


Figure A.8: TSSC, TSSR, TCSC and TCSR

• Thyristor-controlled Series Capacitor (TCSC) and Thyristor-controlled Series Reactor (TCSR).

The difference between TSSC/TSSR and TCSC/TCSR is that the later can smoothly control the value of the reactance while the first group can only control the reactance in discrete steps. Thyristor-controlled devices can also be mixed with thyristor-switched devices to refine the precision of switched devices.

Fixed series compensation is widely used to improve the stability in long distance transmissions and a huge number of applications are already in application. If system conditions become more complex, TCSC is used. TCSC has already been used in different projects for load-flow control, stability improvement and to damp oscillations in interconnected systems [42, 184, 185, 186, 187].

• Static Synchronous Series Compensator (SSSC).

The schematic view of the SSSC is presented in Fig.A.9 and it is basically composed of a VSC (a capacitor plus a converter), a filter and a series transformer. Normally, the SSSC is not connected to an external active power source such as a battery or an energy storage, but it is

also a possible option. When there is not an energy source other than the DC-link capacitor, the SSSC only injects reactive power not to deplete the energy stored in the capacitor. The advantage of the SSSC in comparison to TCSC/TCSR lies in its flexibility, because it can generate any voltage independendently of the line current value, and its higher speed. When an external energy source is available, then the flexibility is even larger, because the SSSC can inject any voltage value (within the ratings) with no angle restriction, analogous to a UPFC.

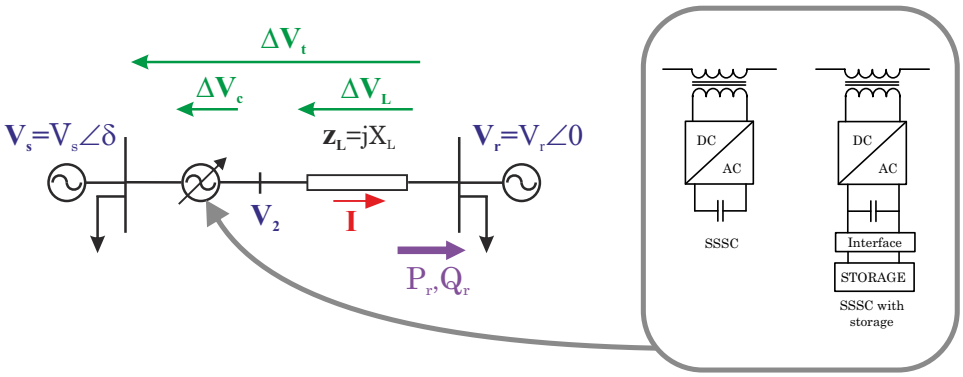


Figure A.9: SSSC

SSSS is mainly a *concept* FACTS. Up to date, real experiences are not abundant and, in most of the cases, the SSSC is an operation mode of an UPFC. The first real SSSC (that was actually a configurable UPFC) was commissioned in the late 90s in Eastern Kentucky by AEP [58, 59]. After this first experience, other two convertible UPFCs followed: one convertible SSSC was constructed in the state of New York by 2004 as a result of a collaborative project between NYPA, EPRI and Siemens T&D [60, 61]. Another convertible UPFC was installed in Korea by KEPCO in 2003 [62, 63, 64]. Lately, a project for constructing a prototype SSSC in the Spanish 220 kV power system has been presented [188].

2.2. Shunt-connected FACTS

As in the case of series FACTS, shunt FACTS may be variable impedance, variable current source, or a combination of these. In principle, all shunt FACTS inject current into the system at the point of connection. Even a variable shunt impedance connected to the line voltage causes a variable current flow and hence represents injection of current into the line. As long as the injected current is in phase quadrature with the line voltage, the shunt device only supplies or consumes variable reactive power. However, any other phase relationship will involve handling of real power as well.

The working mechanism of shunt-connected FACTS can be easily understanded based on the simplified example of Fig.A.11. Fig.A.11 represents a variable impedance that is connected at the end of an inductive line (L_s) and is supplied by a strong source (E). The system can

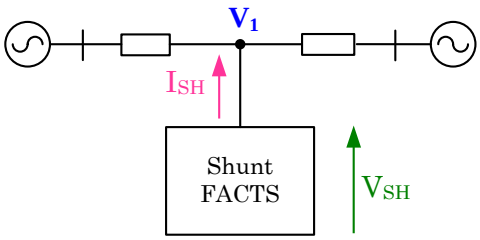


Figure A.10: Symbolic representation of shunt-connected FACTS

be described by two equations:

$$\mathbf{V} = \mathbf{E} - jX_L\mathbf{I} \tag{A.7}$$

$$\mathbf{V} = jX_L\mathbf{I} \qquad \mathbf{V} = -jX_c\mathbf{I} \tag{A.8}$$

The voltage at the connection point (V) is given by the intersection point betweeen equations (A.7) and (A.8). Thus, changing the value of the impedance at the terminals it is possible to get the desired V value. If the impedance adopts an inductive behaviour, V falls in the first quadrant (it lowers the voltage), and if it adopts a capacitive behaviour, V falls in the second quadrant (the voltage at the terminals is increased).

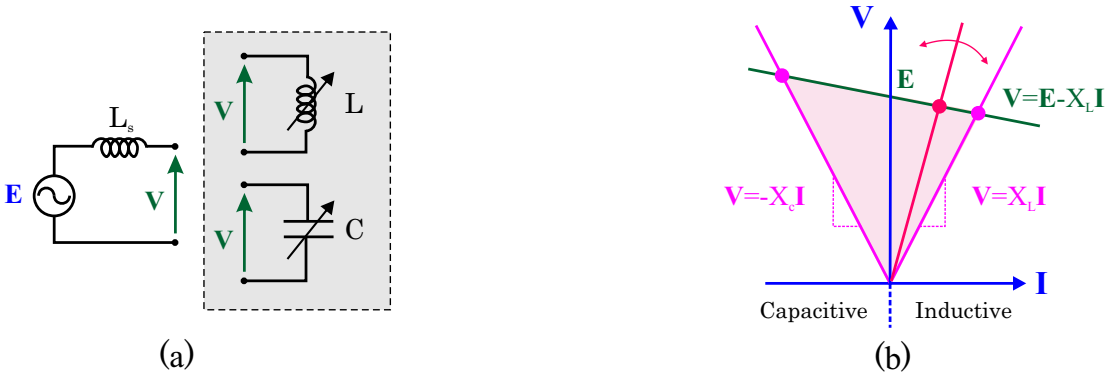


Figure A.11: Shunt compensator principle

The main shunt connected FACTS are the Static Var Compensator (SVC) and the Static Synchronous Compensator (STATCOM):

• **Static VAR Compensator (SVC)**

SVC is a general term given for thyristor-controlled or thyristor-switched reactors (TCR or TSR), thyristor-switched capacitors (TSC), or a compination of them (Fig.A.12). SVC is based on thyristors without gate turn-off cabability (so they have a delay time of at least one grid-cycle) and it includes separate equipment for leading and/or lagging VARs: TCRs and TSRs absorbe reactive power (inductive impedance) and TCSs supply reactive power (capacitive impedance). SVC is considered by some as a cost-efficient alternative to STATCOM, although

this may not be the case if the comparison is made according to the required performance and not only according to the MVA size.

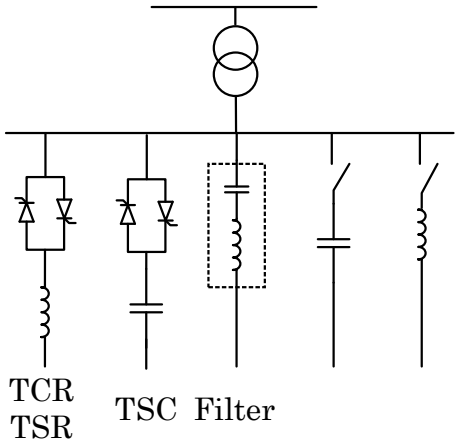


Figure A.12: Symbolic representation of an SVC

SVC is mainly used to control the system voltage and there are hundreds of these devices world-wide. Since decades, it is a well developped technology and the demand on SVC is increasing further [42]. The main FACTS constructors, ABB [93], Siemens [83], Alstom [189], American Semiconductor [190], Hyosung [191], to mention a few, offer well developped SVC catalogues for both industrial and grid applications.

• Static Synchronous compensator (STATCOM)

The STATCOM (Fig.A.13(a)) is one of the most extended FACTS controllers [192]. The AC output voltage of the STATCOM is controlled such that the required reactive power is consumed or injected as depicted in the three cases of Fig.A.13. Two possible operating ways exist for controlling voltage at the STATCOM terminals: (i) the STATCOM is operated at full-wave and the value of the DC voltage is adjusted by regulating the phase-shift between V and V_{sh} and, (ii) the voltage at the DC terminals is kept constant and the output is modulated in magnitude and phase-shift. Ideally V and V_{sh} are in phase but, in a real operation, a little phase-shift exists in order to provide the energy required for losses. When the STATCOM is connected to any energy source that supplies or absorbs power such as a battery, a flywheel, superconducting magnet, large DC storage capacitor or another rectifier/inverter the STATCOM receives the generic name of Static VAR Generator (SVG). The *Battery Enery Storage System* (BESS) and the *Superconducting Magnetic Energy Storage* (SMES), for example, are specific types of SVG.

The main differences between SVC and STATCOM are the speed of response and the size. On the one hand, the attainable response time and frequency bandwidth for closed-loop regulation is much better for STATCOM. The response time itself is not important for transmission systems application, but a higher bandwith yields stable operation over a wider range of line impedance variation. On the other hand, the overall size of the STATCOM is 30%-40% less than that of an SVC, due to the bulky passive components of the later one. In terms of

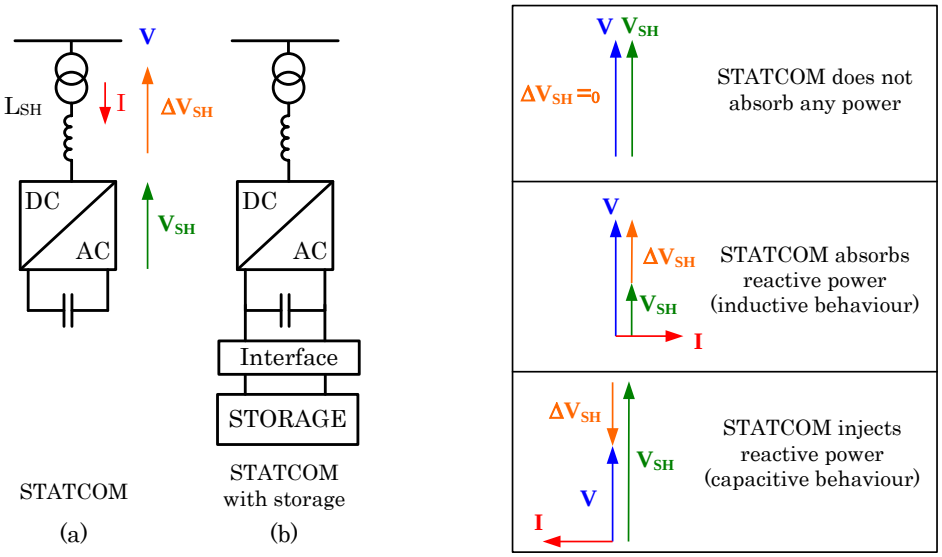


Figure A.13: STATCOM: (a) Without storage, (b) With storage

losses, both loss-reactive power characteristics are comparable: losses are low at zero current (0.1%-0.2%) and increase up to 1% at full rated current [193].

As for SVC, STATCOM is largely available commercially and all major manufacturing companies [93, 83, 189, 190, 191] offer this type of FACTS.

2.3. Universal configuration FACTS

The universal or series-shunt configuration is a combination of FACTS connected in series and in parallel with the line. The series-connected FACTS injects a voltage in series with the line, while the shunt-connected FACTS injects/absorbs a current at the shunt-connection point. Generally, the shunt and the series parts are interconnected by a DC-link that serves for decoupling both sides and as a storage device that provides ride-through capability during transient events. As for other FACTS devices, it is also possible to add a external source or battery to the DC-link. In the cases where the DC-link exists (i.e. UPFC, IPFC), the active power is exchanged via the DC-link. In the cases where a DC-link does not exist (i.e. TCPST, TCPAR, TCVR), the connection is made by thyristor-controlled tap-changers. The most well-known universal configurations are the UPFC/IPFC and the TCPST/TCPAR/TCVR.

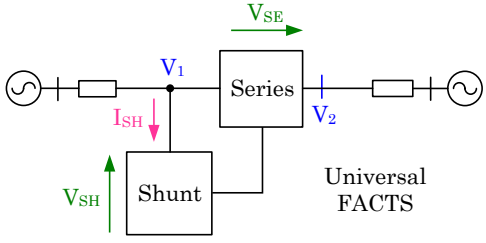


Figure A.14: Schematic drawing of an universal FACTS

• Unified Power Flow Controller (UPFC)

As it is observed in Fig.A.15, an UPFC is a combination of a STATCOM and a SSSC that are coupled by a common DC-link. The DC-link allows bidirectional active power flow betweeen the series and the shunt converter. This DC connection is quite ingenious because it allows the series part injecting not only reactive power, but also active power without the need of a supplementary battery or energy source, as depicted in Fig.A.16. In fact, the series-side is equivalent to a SSSC with an energy storage. The series-side can therefore inject active and reactive power independently. The shunt-side can control two objectives. One, that is compulsory, is to provide/absorb the active power (plus the losses) that the series converter requires. This is often attained by controlling the DC-bus voltage constant. The second objective is optional and it is usually to control the voltage magnitude (or the reactive power) at the shunt-connection point. A more developped description on UPFC can be found in Chapter II.2.

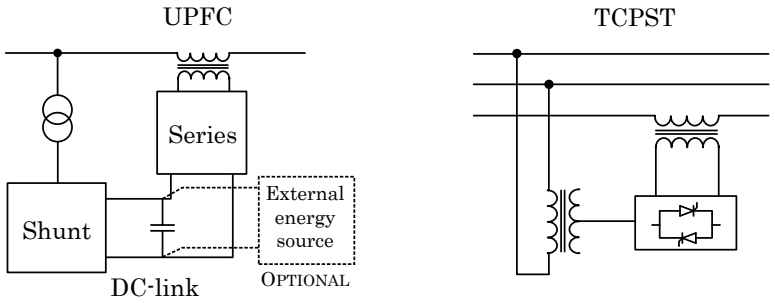


Figure A.15: Single-phase diagram of a UPFC and a TCPST

So far, the author has just found three UPFC installations in operation in the world. In all cases, these installations are reconfigurable and can work either as a single STATCOM, a single SSSC or an UPFC. Two of these UPFC are found in the US: the Inez Project, working at 138 kV and with two ± 160 MV converters [58, 59], and the Marcy Project, working at 345 kV and with two 100 MVA converters [60, 61]. The third convertible UPFC, operating at 154 kV and with two 40 MVA converters, is located in Korea [62, 63, 64].

• Interline Power Flow Controller (IPFC)

The IPFC is a multi-line FACTS composed of various SSSC connected by their DC-link. Each of the SSSC is connected to a different line such that power transfer can be controlled in several lines at a time. With this scheme, any of the interconnected converters can be controlled to supply real power to keep the DC-link constant.

The only IPFC found in the world is the convertible series converter at Marcy, Central New York [60, 61].

• Thyristor-controlled Phase Shifting transformer (TCPST) or Thyristor-controlled Phase Angle Regulator (TCPAR)

The TCPST/TCPAR is basically a phase-shifting transformer which tap-changer is adjusted

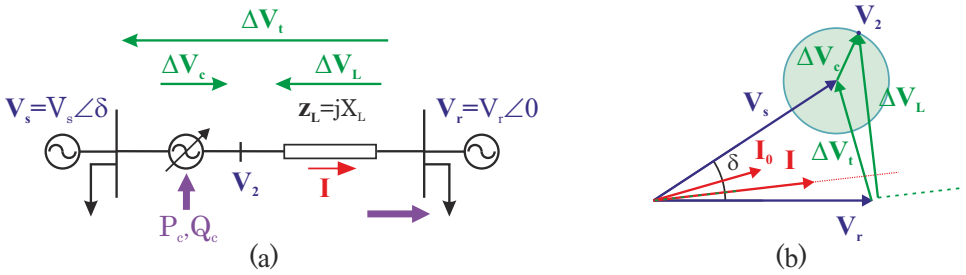


Figure A.16: Representation of a UPFC in a two-bus system and its vector diagram

by thyristor switches to provide a rapidly variable phase-angle (Fig.A.15). In general, phase-shifting is obtained by adding a perpendicular voltage vector in series with the line. The series-injected voltage is derived from the shunt-connected transformer via a thyristor-controlled tap-changer. This FACTS is the static version of mechanical Phase-Angle Regulators (PARs), also known as Phase-Shifting Transformers (PSTs). The advantages of this FACTS in comparison with their mechanical counterparts is their lower maintenance and higher dynamics. The drawback of TCPST/TCPAR in respect of UPFC-like, converter-based universal FACTS is that the real and reactive power needed to accomplish the desired regulation must be supplied externally by the system [40].

Mechanical phase-shifting transformers are not extremely common but they are used in the power systems for steady-state system conditions [42, 194, 195]. Mechanical phase-shifting transformers are commercially available [93, 83]. A review on static phase shifters, including different schemes and functions, is provided in [196]. But, by 1993 no solid-state phase-shifters or voltage regulators were known in service [197] and, so far, the author of this manuscript has not found any.

• **Thyristor-controlled Voltage regulator (TCVR)**

The TCVR is based on the same principle as the TCPAR but the windings of the transformer and the electronic tap-changer are arranged in a way that the injected voltage is in-phase with the terminal voltage. The TCVR acts as a variable turns-ratio transformer.

2.4. HVDC

A HVDC device consists of two converter stations that interconnect two AC connection points as shown in Fig.A.17. The originality of this configuration consists in an intermediate DC stage that enables the interconnection of grids of very different nature. Thanks to this particular AC-DC-AC arrangement the interconnected grids can be asynchronous or have different frequencies. Besides, HVDCs do not contribute to the short-circuit current of the AC system.

When the interconnection distance is negligible, both converter stations are very close and the DC-link is just composed of a capacitor. This configuration is known as *back-to-back (B2B)*. B2B-HVDCs are not usually used for bulk power transmission but rather for interconnecting

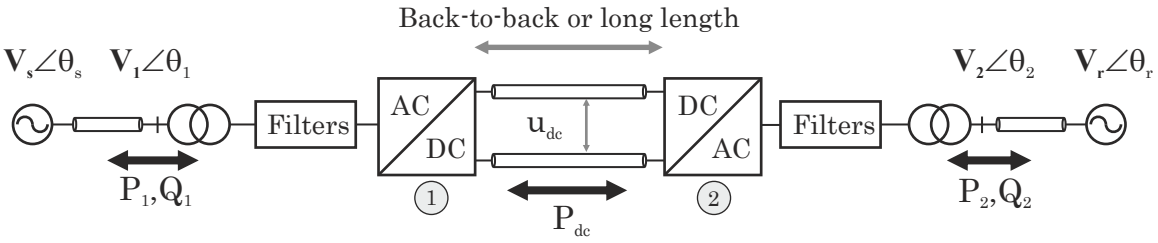


Figure A.17: Schematic view of an HVDC

systems that cannot be interconnected directly in AC. When power has to be transmitted during long distances, the lumped capacitor of B2B-HVDC is replaced by two long DC cables. An extended chapter on HVDC and MVDC (its MV counterpart) can be found in Chapter II.2.

HVDC systems are well established today, with more than 100 installations in operation or planned worldwide [18, 17]. These installations are transmitting over 80 GW

3. Custom power (from [193])

Custom power has been defined as the concept of employing power electronic (static) controllers in 1 kV through 38 kV distribution systems for the purpose of supplying a compatible level of power quality necessary for adequate performance of selected facilities and processes.

A satisfactory operation of the power system depends upon an acceptable level of power quality. But, what is power quality? As it is well introduced in [45], power quality has been given different connotations over the years but, in overal terms, it can be defined as the combination of voltage and current quality. Voltage quality is concerned with the deviations of voltage relative to the ideal voltage waveform, which must be a single-frequency sine wave of constant frequency and constant magnitude. Current quality is a complementary definition to voltage quality: it is the property of the current wave to be ideal. Once more, an ideal current waveform is that with a single-frequency, a constant frequency and a constant magnitude. An additional requirement is that the current waveform must be in phase with the voltage waveform. In a certain way, it is possible to say that voltage quality has to do with the quality of the wave that the utility delivers, and current quality is related to the use that the customer makes of the delivered power.

Power Quality is a relatively new subject that is studied since the late 90's and it therefore essential to establish the characteristics of the power supply system and the requirements of the end-user equipment to ensure the global welfare of the electric power system. The main organizations responsible for power quality standards development in the international community are the *International Electrotechnical Commission* (IEC) and the *Institute of Electrical and Electronics Engineers* (IEEE). Power quality standards must provide guidelines, recommendations, and limits to help assure the compatibility between the end use equipment and

the system where it is applied [198]. However, all standard developers do not share the same points of view towards power quality. The definition of the term *Power Quality*, for example, represents an obvious example of this lack of harmonization. The IEC (as well as CENELEC) does not use the term power quality in its standards [45], the term *Electromagnetic Compatibility* (EMC) is used instead. The difference between the concepts of power quality and EMC is manifest: EMC comprehends a wider domain that power quality. EMC deals with further phenomena other than conducted perturbations through the power system (radiated phenomena, for example), and thus, power quality may be considered as a part of EMC.

Power quality phenomena may be classified according to two criteria: the duration of a perturbation and its origin.

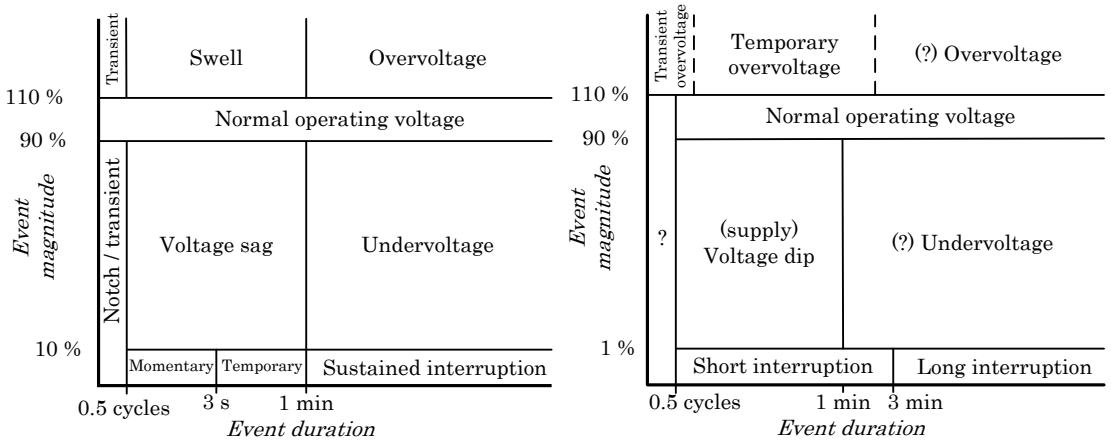


Figure A.18: Some definitions of voltage magnitude events (from [45]). The *question mark* in EN 50160 means that, contrary to IEEE 1192, no specific term has been assigned to that range of values.

Regarding the length of time, power quality phenomena can be divided into two categories: **steady-state (or continuous)** and **disturbances (or events)** (see Fig.A.18). **Steady-state phenomena** are occurrences that happen in a regular basis, such a polluting load that is constantly *consuming* current harmonics. Power quality **disturbances or events** are phenomena that do not occur at a regular basis but can seriously impact the performance of equipment leading to a considerable degradation of the operation and financial losses. For example, tripping of critical equipment can induce the stop of a whole production in an industrial plant. Since events just happen every once in a while, they are best described by the time between events and the characteristics of each event, both expressed in a stochastic way.

According to their origin, power quality deviations can either come from the **supply-side** or from the **load-side**. The most frequent perturbations that come from the utility side are voltage dips and interruptions, frequently caused by faults in the power system. Industrial customers are often harmed by this kind of events because of postponed revenues, negative impact on cash-flow, loss of goodwill from customers, equipment damage, loss of market

share etc. At the load-side, a poor power-quality usually comes from the low current quality absorbed by the load, that often contains undesirable harmonics, it is unbalanced (in low voltage systems different single-phase loads connected to the same three-phase system may produce unbalance) or produces flicker. Sustained harmonics in the grid causes extra-losses, accelerates the ageing of the equipment, reduce the efficiency of rectifiers in sensitive electronics loads and limits the immunity of rotating machines for voltage unbalance.

The most well-known custom-power devices used for mitigating the above-mentioned perturbations are described next.

3.1. Compensation of perturbations due to polluting loads

The great majority of the devices used for compensating or filtering the pollution generated by loads are connected in shunt. These shunt-connected apparatus generate the distorted part of the load current and thus, the overal current consumed by the load plus the compensating device is balanced and distortion free. The most generalized power-quality problems induced by loads are flicker, current harmonics, power factor and unbalances.

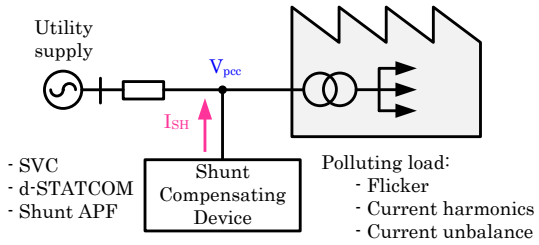


Figure A.19: Illustration of polluting loads and shunt-connected mitigation equipment

Flicker is a low-frequency modulation (around 10 Hz) of the voltage/current generated by a time-changing consumption of power. Flicker can cause harmful effects, such as headaches, on human. For this reason, flicker limits are based on human eye-brain sensitivity to voltage fluctuations (in IEEE Std. 1453-2004 and IEC 61000-4-15). Arc furnace operation has traditionally been the cause of flicker on medium-voltage and high-voltage systems [199] but wind turbines may also cause this phenomenon [200, 201].

Despite the existance of traditional solutions for reducing flicker (i.e. grid reinforcement, dimmers, series capacitors and saturable reactors), the most effective solutions for compensating for flicker are the SVC (Fig.A.12) and the STATCOM (also named distribution-STATCOM or d-STATCOM). The difference between one and the other lays in the dynamics (STATCOM is faster), the volume (SVC is bulkier due to the size of the passive components) and the price (usually STATCOM is more expensive). When a SVC is chosen, the SVC consists of a TCR branch and filters (no TCS is used).

Current harmonics are usually produced by loads interfaced with power electronics equipment that absorb non-sinusoidal currents (e.g. rectifiers). IEEE Standard 519-1992, for exam-

ple, recommends harmonics limits for individual consumers and for utilities. In order to fulfil the specified limits, current filters are installed. These filters can either be passive, active or hybrid, a combination of both.

Passive filters are LC filters with a fixed configuration that offer a zero impedance path for current harmonics at a particular frequency. They are normally combined with high-pass filters that draw the rest of the higher order current harmonics. The drawback of these filters is that, if the frequencies of the harmonics vary, they cannot adapt accordingly. In that sense, active filters are a much more flexible solution, because they can generate the exact current waveform (provided that the physical arrangement and control of the active filter allows it). The topology of a shunt active power filter is exactly the same as a STATCOM, with the only difference that the filter inductance must be carefully chosen so the objective harmonics can be compensated. Hybrid filters are a combination between active filters and passive filters. Passive filters are in charge of eliminating low frequencies and thus the overal dimensioning of the active filter (with the consequent cost) is reduced [202, 85].

Power factor must be kept near unity. Thus, loads that consume too much reactive power (usually of the inductive type) need an external reactive power supply to fit into the standards. The required reactive power can be provided by SVC or STATCOM type power electronics devices.

Current unbalances can be produced when all the three phases do not consume a balanced current. As for flicker and power factor, unbalances can be compensated by SVC or by STATCOM.

3.2. Protection of sensitive equipment

When confronted to very short duration and shallow dips, one solution other than using protection equipment might be to lower the susceptibility level of the equipment, making it insensitive to some types of events. When the severity, recurrence and time-length of the events is higher, then it might be worth to change the configuration of the power system [45] to avoid future events. Finally, when either of the before-mentioned solutions are not possible, some industrial customers may consider the use of protection equipment. The cost of the protection equipment is often high, so a deep analysis must be performed in order to assess the benefits and disadvantages of the installation of a protection equipment. Some possible solutions are briefly explained next.

• Traditional solutions

The most well-known traditional solution, not based on power electronics, is the **motor-generator set**. A motor-generator set is composed of a motor, a flywheel and a generator all connected to the same axis and supplied from the power system (Fig.A.21). The rotational energy stored in the flywheel can be used for steady-state voltage regulation or for voltage support during transients. This system has high-efficiency, low initial costs and enables long-duration ride-through (several seconds), but can only be used in industrial environments, due

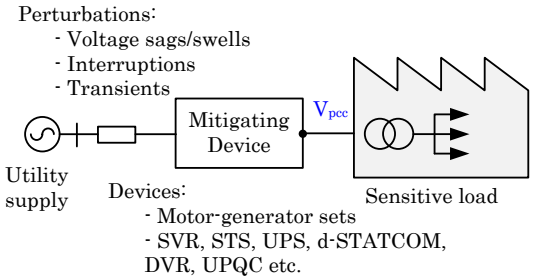


Figure A.20: Illustration of sensitive loads and shunt-connected mitigation equipment

to its size, noise and maintenance requirements.

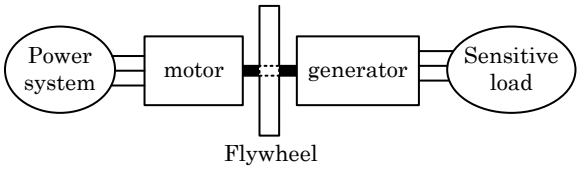


Figure A.21: Traditional solution: motor-generator set

- **Static Voltage Regulator (SVR)**

As shown in Fig.A.22, the SVR is basically a transformer with electronically-switched tap changers. When there is a voltage variation in the supply, the turns-ratio changes and the voltage at the secondary is kept steady. Since the static tap-changer is composed of thyristors a minimum delay of half a cycle is to be expected. In 2003 no existing installations where known [193].

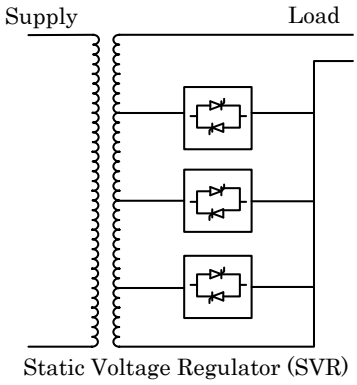


Figure A.22: Illustration of a static voltage regulator (SVR)

- **Static Transfer Switch (STS)**

A STS is a very fast switch that deviates the power coming from a primary source to an alternative supply source. The static switches are composed of two anti-parallel thyristors per phase as depicted in Fig.A.23. The STS is a rather economic solution and it is very interesting for those industrial plants that already have a mechanical transfer switch and want

to upgrade it to its fast counterpart. However, this option presents two major drawbacks: (i) an alternative supply path must be available, and (ii) if the sag affects both supply paths, the STS will not be effective. The STS is a commercially available solution for LV and MV sites [203, 204, 205, 206, 207].

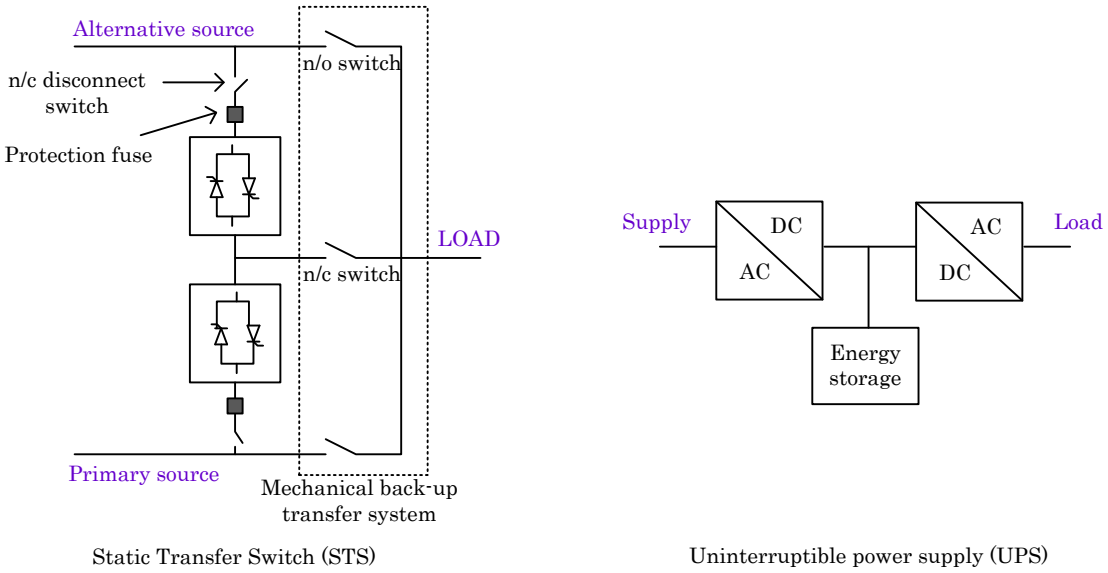


Figure A.23: Illustration of a static transfer switch (STS) and an uninterruptible power supply (UPS)

- **Uninterrumptible Power Supply (UPS)**

The UPS is a back-to-back converter system that has an energy storage system connected to its DC-link. During normal operation, the electric power is converter from AC to DC and from DC to AC, and the energy storage system is charged. When a fault occurs (even a complete interruption), the energy storage system supplies the load. Depending on the load requirements, and the size and nature of the energy storage, the UPS can provide power during minutes or even hours. The main drawback associted to this device is the continuous energy loss associtated to the losses in the converter chain. UPS is a typical solution for low voltage environments, specially computers [203, 208, 205]. It must be noted that, according to the custom-power definition, UPS is not classified as a custom power when it is used below 1 kV voltage levels.

- **STATCOM**

The STATCOM can also be used to compensate for voltage sags. However, for large voltage drops is not considered a cost-effective solution and it is seldom used for these purposes. In [209] the minimum apparent power injection required to correct a given voltage sag is calculated and it its shown that DVR needs less installed power than STATCOM. STATCOM is a largely expanded custom-power and there is a great choice of producing companies.

- **Backup stored energy system (BSES)**

The BSES is basically a STATCOM with an energy source (e.g. battery) connected in its

DC side (Fig.A.24). In this system the efficiency of the conversion system is higher than in a UPS.

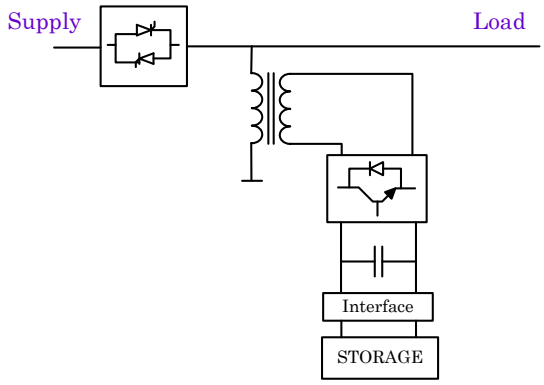


Figure A.24: Illustration of a backup stored energy system (BSES)

• **Dynamic voltage restorer (DVR)**

The DVR has the same topology as a SSSC. The only difference is the purpose and therefore the ratings: the DVR serves for compensating for voltage sags while SSSC is used for power-flow control. Commercially available DVRs use large capacitor banks that allow injecting the required voltage all along the voltage dip without depleting it. Actually, the capacitor size is an important parameter that establishes the compensation capabilities of DVR. In some cases, an external active energy source can be connected to the DC-link.

Although is not extensively used, real-case applications exist [210, 93] and it seems a promising technology for voltage sag compensation. Its major drawbacks are its cost and that it cannot supply power during *long* interruptions.

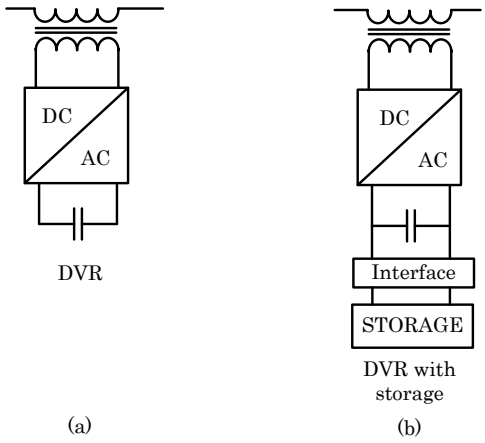


Figure A.25: Illustration of a dynamic voltage restorer (DVR)

• **Unified power quality controller (UPQC)**

A smart alternative to avoid the use of an energy storage device in the DC-side of a DVR is

to connect a parallel converter at the point of common coupling with the load, as an UPFC (see Fig.A.26). This device is known as *Unified Power Quality Conditioner (UPQC)* and it is one of the most flexible custom-power devices. The primary objective of the shunt-connected converter is to supply active power to the DC-bus in order to maintain it to a constant voltage value. Secondarily, the shunt-connected VSC acts as a current compensator that can filter the distorted and unbalanced currents drawn by the load and/or operate as a power-factor corrector. The series-connected VSC works as as a DVR protecting the load from voltage disturbances such as voltage dips (balanced or unbalenced) or voltage harmonics.

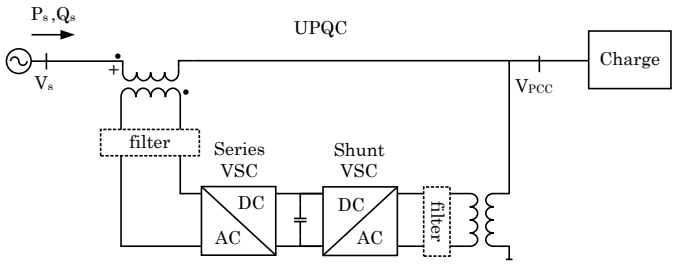


Figure A.26: Illustration of an unified power quality controller (UPQC)

Although shunt APFs are widely developped and installed and DVR seem to have a promising future, this is not yet the case of UPQC in commercial applications. Many research articles and laboratory-scale prototypes [211, 212, 213, 214, 82] have been found in litterature but, on the contrary, not many fabricants and real applications have been found. Hycon, offers UPQC in their catalogue [175] and ABB offers a device called *Active Voltage Conditioner (AVC)* that it is basically a DVR with a possible shunt auxiliar connection, but it cannot be considered as a full-function UPQC.

Because the interest of this device in this PhD, it will be separately developed in Chapter II.2.

Medium voltage direct current (MVDC)

The MVDC is the medium voltage counterpart of the HVDC. The MVDC is not yet widely used as a custom-power device but it is included here because some publications exist and it seems that it can be very interesting for certain applications that require a high flexibility. Alstom and Siemens, for example, propose a MVDC for the marine industry (e.g. in order to connect boats to harbours). The MVDC is more expensive than other devices because it uses full-scale converters, but it ensures an efficient supply of drilling ships and it enables an ecological and reliable supply while ships are docked. In [215], a MVDC is proposed for supplying high-quality electric power to/from an industrial plant.

Table A.1 shows the characteristics and drawbacks of some custom-power devices for mitigation of voltage dips and interruptions. Table A.27 shows a comparison of the most important FACTS and custom-power (also known as d-FACTS), where it can be observed that they share the same topology but their functions are different.

DEVICE	TYPICAL RATINGS	IMPLEMENTED CONTROL FUNCTIONS	DRAWBACKS
STATCOM	Medium voltages up to 100 MVA	• Voltage regulation at the point of connection • Reactive power control • Suppression of flicker and voltage fluctuations • Cancellation of load current harmonics	• High active power demand • Cannot mitigate voltage dips at distribution level • Increases voltage for the whole system
DVR	Medium voltages Power: 0.5-20 MVA (2 MVA modules)	• Mitigation of voltage dips • Suppression of supply voltage harmonics	• Cannot mitigate interruptions
STS	Up to 15 kV/ 600A	• Mitigation of voltage dips and, • Short and long interruptions by fast load transfer	• Cannot mitigate interruptions and dips which originate at higher voltage level • An independent supply must be available
BSES	Up to 2 MVA	• Mitigation of voltage dips and, • Short and long interruptions taking over the total load	• High energy storage requirements
SVR	No existing application found	• Mitigation of voltage dips by static tap changers	• Cannot mitigate interruptions • Slow dynamic response

Table A.1: Custom power devices for mitigation of dips and interruptions ([193])

4. Voltage and current source converters

A possible classification of high-power converters is given in [216] (Fig.A.28). According to this classification, DC-link converters are divided into voltage source converters (VSC) and current source converters (CSC). AC-AC converters, known as cycloconverters are seldom used in high power applications due to their current economical unfeasibility [40]. In the following paragraphs the difference between VSC and CSC is shortly described.

A switching power converter has no internal energy storage, which means that, under ideal conditions (no internal losses), the instantaneous power at the input of the converter is the same to the instantaneous power at the output of the converter. Additionally, the termination of the input and the output terminals is complementary: if the input is ended by a voltage source (a battery or a capacitor, for example), then the output must be terminated by a current source (e.g. a voltage source with an inductance) or vice-versa. In the case of DC-AC converters, the DC side is considered as the input. Accordingly, a VSC has a voltage source at the DC side of the converter and a CSC has a current source instead.

A CSC is characterized by the fact that DC current always flows in one direction and that power-flow reverses with the reversal of the DC voltage. For VSC is the opposite: the power

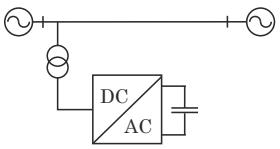
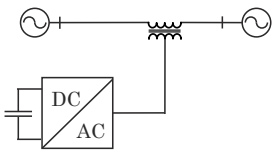
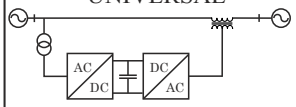
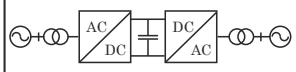
Name		Topology	Preferred Tasks	
Transmission	Distribution		Transmission	Distribution/Power quality
STATCOM	d-STATCOM or Shunt APF	SHUNT 	Voltage control/ reactive power regulation Oscillation damping	Flicker compensation Voltage regulation/ reactive power compensation Current harmonic filter
SSSC	DVR	SERIES 	Power flow (reactive) control Transient stability Oscillation damping	Sag/swell compensation
UPFC	UPQC	UNIVERSAL 	STATCOM+SSSC	Shunt APF + DVR
HVDC	MVDC	AC-DC-AC 	Power flow control Transmission of power over long distances/ interconnection of remote energy sources Interconnection of asynchronous grids Voltage control/ reactive power regulation Transient stability Oscillation damping	Connection of distributed generation and loads Interconnection of distribution grid.

Figure A.27: Comparison table of the fuctions of FACTS and d-FACTS

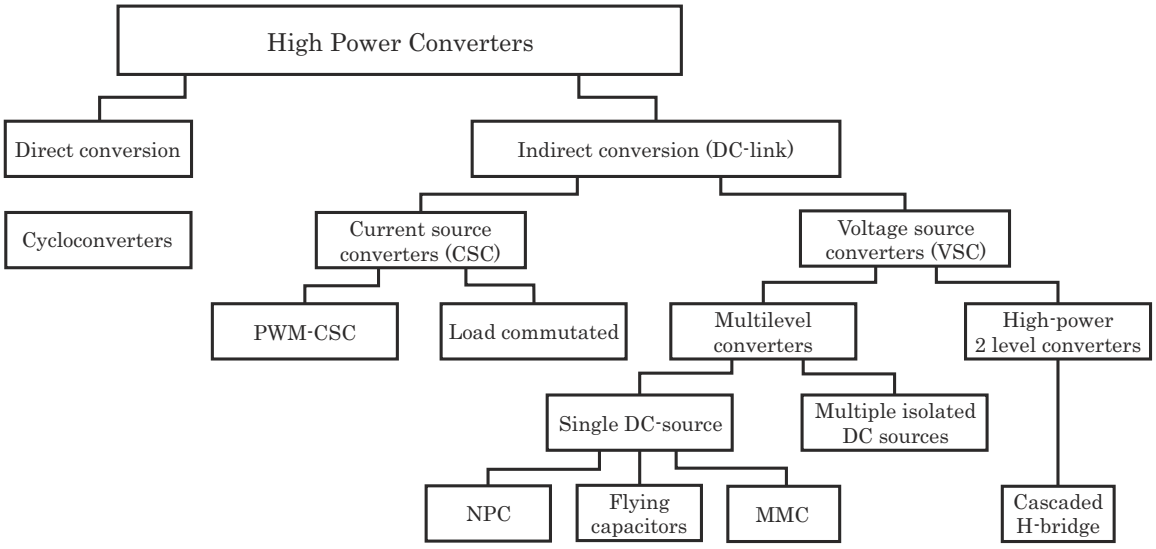


Figure A.28: High power converter classification

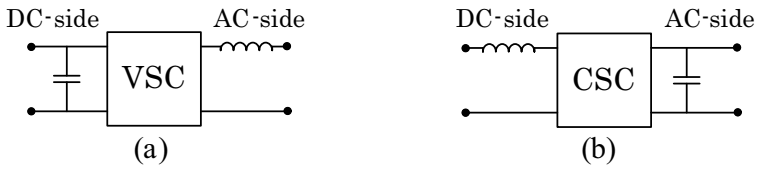


Figure A.29: (a) VSC (b) CSC

flow reversal takes place when the current polarity changes. It is difficult to state which of the configurations offers a better trade-off because both CSC and VSC present advantages and disadvantages [40]:

i) CSCs require power semiconductors with bi-directional voltage blocking capability and, so far, GTOs and IGBTs, power semiconductors with gate turn-off capability, either cannot reverse voltage at all or can do it at expenses of other important parameters such as conduction losses.

ii) CSCs need a voltage source termination at the AC terminals (a capacitive filter, while VSCs have a natural current source represented by the leakage inductance of the coupling transformer. Moreover, the charged current reactor at the DC terminals of a CSC is much lossier than the equivalent capacitor in VSC.

iii) On the one hand, the voltage-source termination (i.e. capacitor) of VSC tends to provide an inherent protection against line voltage transients, while CSC may require additional overvoltage protection. On the other hand, CSC are almost immune to short-circuits at the terminals due to the current limiting capability of inductors.

In general, and compared to CSC, VSC present many practical advantages and it constitutes a relatively new subject of study (two decades). For this reason, in the rest of the manuscript VSC-type converters will be predominantly addressed and the prefix VSC will, in most of the cases, be omitted.

Appendix B

Power system related concepts

All throughout the PhD manuscript multiple concepts, commonly used by power engineers, are evoqued without giving further information. However, the non-specialist readers could find difficulties to follow the thread of the manuscript at certain points. For this reason, the aim of Appendix B is to clarify some basic concepts:

- *The notion of phasor and the different ways of representing three-phase signals: the natural abc frame, the static $\alpha\beta 0$ frame, and arbitrary frequency rotating frames (e.g. dq).*
- *The decomposition of three-phase signals into symmetrical components.*
- *The most well-known power theories (i.e. The Generalized Non-Active Power Theory and The PQ theory).*

1. Three-phase signals: representation and reference frames

Electrical generators connected to the AC power system produce three-phase signals and, for this reason, most of the loads and components connected to the AC power systems need to be three-phase. Since the foundation of the first AC power system, power engineers and researchers have developped different representation tools to deal with three-phase signals.

1.1. Phasor representation in the natural frame

A balanced three-phase signal is an association of three sinusoidal waves that hold the same amplitude and are displaced of 120° electrical degrees from one to the other. In order to ease the mathematical handling, it is often useful to typify these sinusoidal signals by means of phasors. As it is demonstrated in the following lines, sinusoidal signals can be represented by the real part of a complex expression that is known as phasor. The phasor term can either refer to the time-dependent form, $\mathbf{X}(t) = \mathbf{X} \cdot e^{j\omega t}$, or just to the simplified notation, $\mathbf{X} = \hat{X}e^{j\varphi}$, that encodes the amplitude and phase of an underlying sinusoid. The graphical representation of the sinusoidal set and the phasors is presented in Fig.B.1.

$$\begin{aligned} x_a(t) &= \hat{X}_a \cdot \cos(\omega t + \varphi_a) = \Re\left\{\mathbf{X_a}(t)\right\} = \\ &= \Re\left\{\mathbf{X_a} \cdot e^{j\omega t}\right\} = \Re\left\{[\hat{X}_a \cdot e^{j\varphi_a}] \cdot e^{j\omega t}\right\} \end{aligned} \tag{B.1a}$$

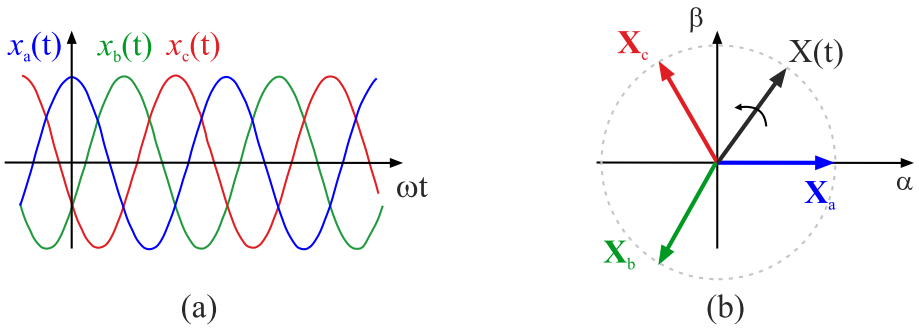


Figure B.1: Graphical representation of three-phase signals (a) time-domain, (b) phasors

$$\begin{aligned} x_b(t) &= \hat{X}_b \cdot \cos(\omega t - \frac{2\pi}{3} + \varphi_b) = \\ &= \Re\{\mathbf{X_b}(t)\} = \Re\left\{\mathbf{X_b} \cdot e^{j\omega t}\right\} = \Re\left\{[\hat{X}_b e^{j\varphi_b} \cdot e^{-2\pi/3}] \cdot e^{j\omega t}\right\} \end{aligned} \tag{B.1b}$$

$$\begin{aligned} x_c(t) &= \hat{X}_c \cdot \cos(\omega t + \frac{2\pi}{3} + \varphi_c) = \\ &= \Re\{\mathbf{X_c}(t)\} = \Re\left\{\mathbf{X_c} \cdot e^{j\omega t}\right\} = \Re\left\{[\hat{X}_c e^{j\varphi_c} \cdot e^{+2\pi/3}] \cdot e^{j\omega t}\right\} \end{aligned} \tag{B.1c}$$

1.2. Static reference frame

The time-dependent form of the phasor, $\mathbf{X}(t)$, is a vector that rotates in the $\alpha\beta$ plane. The real part of this vector is the α component, and the imaginary part corresponds to the β component. Observe that, when an homopolar component exists, a third dimension must be added to the $\alpha\beta$ plane, as depicted in Fig.B.2.

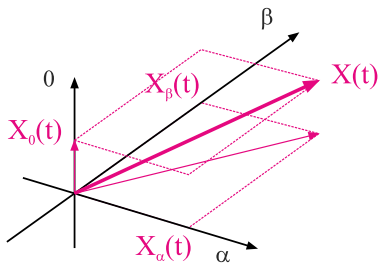


Figure B.2: Phasor in a three-dimensional space ($\alpha\beta 0$)

The time-dependent phasor in the $\alpha\beta$ plane is calculated by the following expression:

$$\mathbf{X}(t) = \mathbf{X}_{\alpha\beta}(t) = \frac{2}{3}k\left[x_a(t) + x_b(t) \cdot e^{+2\pi/3} + x_c(t) \cdot e^{-2\pi/3}\right] \tag{B.2}$$

where k is a factor that represents the type of transform. When $k = 1$, the conversion is amplitude invariant, and it is known as *Clarke Transform*. When $k = \sqrt{3/2}$, the conversion is power invariant, and it is designated as *Concordia Transform*. For the homopolar component the calculation is different for each of the transforms. Here the *Clarke Transform* is expressed

in matrix form,

$$\mathbf{x}_{\alpha\beta 0}(t) = T_{cl} \cdot \mathbf{X}_{\mathbf{abc}}(t) \tag{B.3}$$

$$\begin{bmatrix} x_\alpha(t) \\ x_\beta(t) \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \cdot \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \tag{B.4}$$

1.3. Rotating reference frame

The projections of $\mathbf{X}(t)$ in the $\alpha\beta$ static axes present a sinusoidal shape. However, depending on the selected control method, it is more interesting to use a rotating frame that rotates at the same speed as the phasor, and in the same direction. If the rotating frame has the same angular speed and direction as the phasor, the projections of the phasor on the rotating frame will have a constant value. Fig.B.3 shows the static and the rotating frames in the plane, where the axes of the rotating frame are denominated *dq*.

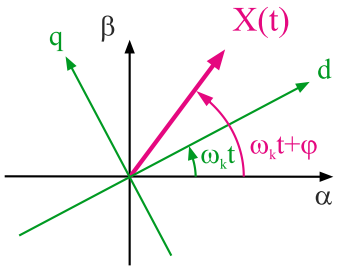


Figure B.3: Static ($\alpha\beta$) and rotating (dq) frames

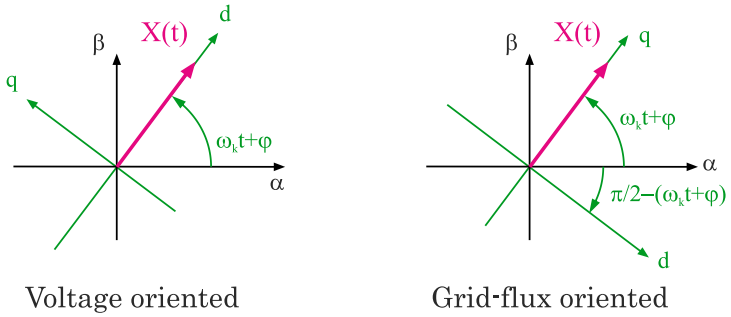
The coordinate conversion from the static to the rotating frame is different depending on two factors: (i) if the rotating frame is voltage- or flux-oriented (Fig.B.4), and (ii) if the rotating frame rotates in the anticlockwise direction (positive sequence) or in the clockwise direction (negative sequence). The rotating frame is voltage-oriented when the phasor is inlined with the *d-axis* and, it is grid flux-oriented when the phasor is inlined with the *q-axis*. The conversion expressions and matrices for the positive sequence case (anticlockwise rotation) are shown in Tables B.1. For the negative-sequence case (clockwise rotation), the conversion expressions are presented in Table B.1.

Finally, it is also possible to directly convert a three-phase signal from the natural *abc* frame to a (positive) rotating frame by combining the Clarke/Concordia transform and the rotating matrices. The resulting transform is known as the *Park Transform*:

$$\mathbf{X}^{dq}(t) = P_{cl}(\omega t) \cdot \mathbf{X}^{abc}(t) \tag{B.5a}$$

Table B.1: Voltage-oriented and flux-oriented conversions for positive frames

Voltage-oriented (anticlockwise rotation)	Flux-oriented (anticlockwise rotation)
$\mathbf{X}^{dq}(t) = \mathbf{X}^{\alpha\beta}(t) \cdot e^{-j\omega t}$	$\mathbf{X}^{dq}(t) = \mathbf{X}^{\alpha\beta}(t) \cdot e^{-j(\pi/2-\omega t)}$
$\mathbf{X}^{dq}(t) = R(\omega t) \cdot \mathbf{X}^{\alpha\beta}(t)$	$\mathbf{X}^{dq}(t) = R(\pi/2 - \omega t) \cdot \mathbf{X}^{\alpha\beta}(t)$
$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & \\ -\sin(\omega t) & \cos(\omega t) & \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}$	$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & \cos(\omega t) & \\ -\cos(\omega t) & \sin(\omega t) & \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}$



Voltage oriented Grid-flux oriented

Figure B.4: Voltage-oriented and flux-oriented rotating frames

Table B.2: Voltage-oriented and flux-oriented conversions for negative frames

Voltage-oriented (clockwise rotation)	Flux-oriented (clockwise rotation)
$\mathbf{X}^{dq}(t) = \mathbf{X}^{\alpha\beta}(t) \cdot e^{+j\omega t}$	$\mathbf{X}^{dq}(t) = \mathbf{X}^{\alpha\beta}(t) \cdot e^{+j(\pi/2-\omega t)}$
$\mathbf{X}^{dq}(t) = R(-\omega t) \cdot \mathbf{X}^{\alpha\beta}(t)$	$\mathbf{X}^{dq}(t) = R(-\pi/2 - \omega t) \cdot \mathbf{X}^{\alpha\beta}(t)$
$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) & \\ \sin(\omega t) & \cos(\omega t) & \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}$	$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \begin{bmatrix} \sin(\omega t) & -\cos(\omega t) & \\ \cos(\omega t) & \sin(\omega t) & \\ 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix}$

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\pi/3) & \cos(\omega t + 2\pi/3) \\ -\sin(\omega t) & -\sin(\omega t - 2\pi/3) & -\sin(\omega t + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{B.5b}$$

1.4. Conversions from static to rotating coordinate systems

Often, model equations are deduced in the natural (abc) frame. However, these equations are seldom useful in the control sythesis and it is better to convert them to (i) the static $\alpha\beta$ frame, or to (ii) rotating frames. In the following paragraphs these conversion procedures are provided.

• **Conversion from the natural** *abc* **frame to the static** $\alpha\beta$ **frame**

Let a generic model in the *abc* frame be,

$$\frac{d[\mathbf{x_{abc}}]}{dt} = A \cdot \mathbf{x_{abc}} + B \cdot \mathbf{u_{abc}} \tag{B.6}$$

Assuming that $\mathbf{x}_{\alpha\beta 0} = T_{cl} \cdot \mathbf{x_{abc}}$, and $\mathbf{u}_{\alpha\beta\mathbf{0}} = T_{cl} \cdot \mathbf{u_{abc}}$,

$$\frac{d[{T_{cl}}^{-1} \cdot \mathbf{x}_{\alpha\beta 0}]}{dt} = A \cdot [{T_{cl}}^{-1}\mathbf{x}_{\alpha\beta\mathbf{0}}] + B \cdot [{T_{cl}}^{-1}\mathbf{u}_{\alpha\beta\mathbf{0}}] \tag{B.7}$$

$$\frac{d[{T_{cl}}^{-1}]}{dt} \cdot \mathbf{x}_{\alpha\beta\mathbf{0}} + {T_{cl}}^{-1} \cdot \frac{d[\mathbf{x}_{\alpha\beta\mathbf{0}}]}{dt} = A \cdot [{T_{cl}}^{-1}\mathbf{x}_{\alpha\beta\mathbf{0}}] + B \cdot [{T_{cl}}^{-1}\mathbf{u}_{\alpha\beta\mathbf{0}}] \tag{B.8}$$

If matrices A and B are diagonal, the products $A \cdot {T_{cl}}^{-1} = {T_{cl}}^{-1} \cdot A$ and $B \cdot {T_{cl}}^{-1} = {T_{cl}}^{-1} \cdot B$ are commutative. Developping the equations, the following expresion in the $\alpha\beta$ frame is obtained:

$$\frac{d[\mathbf{x}_{\alpha\beta\mathbf{0}}]}{dt} = A \cdot \mathbf{x}_{\alpha\beta\mathbf{0}} - \left[T_{cl} \cdot \frac{d[{T_{cl}}^{-1}]}{dt}\right] \cdot \mathbf{x}_{\alpha\beta\mathbf{0}} + B \cdot \mathbf{u}_{\alpha\beta\mathbf{0}} \tag{B.9}$$

Since the derivative of T_{cl} is zero, the preceding equation yields,

$$\frac{d[\mathbf{x}_{\alpha\beta\mathbf{0}}]}{dt} = A \cdot \mathbf{x}_{\alpha\beta\mathbf{0}} + B \cdot \mathbf{u}_{\alpha\beta\mathbf{0}} \tag{B.10}$$

which has exactly the same structure as the equation (B.6) in *abc* coordinates.

• **Conversion from the static** $\alpha\beta$ **frame to the** *dq* **rotating frame**

An analogous procedure is followed for the conversion from $\alpha\beta$ to *dq* coordinates. This time, the rotating matrix $R(\omega t)$ is used instead of the *Clarke Transform*. The only difference with the above developped procedure is that the product $R(\omega t) \cdot d[R(\omega t)^{-1}]/dt$ is not zero and thus, a coupling appears between axes d and q.

$$\frac{d[\mathbf{x_{dq0}}]}{dt} = A \cdot \mathbf{x_{dq0}} - \left[R(\omega t) \cdot \frac{d[R(\omega t)^{-1}]}{dt}\right] \cdot \mathbf{x_{dq0}} + B \cdot \mathbf{u_{dq0}} \tag{B.11}$$

$$\frac{d[\mathbf{x_{dq0}}]}{dt} = A \cdot \mathbf{x_{dq0}} + \omega \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \cdot \mathbf{x_{dq0}} + B \cdot \mathbf{u_{dq0}} \tag{B.12}$$

2. Symmetrical sequence components

Once the representation methods are clear, it is also important to explain the concept of symmetrical components, which are fundamental to understand unbalanced signals. According to Fortescue, any set of three-phase signals can be decomposed in three sets of sequence components: (a) a set of homopolar components, (b) a set of positive-sequence components, and (c) a set of negative sequence components.

Zero-sequence (or homopolar) components, consist of three-phasors with equal magnitudes and zero phase-displacement from one to the other. **Positive-sequence components** consist of three-phasors with equal magnitudes and with a phase-displacement of 120° that rotate in the anticlockwise

direction. **Negative-sequence components** consist of three-phasors with equal magnitudes and with a phase-displacement of 120° that rotate in the clockwise direction. The negative-sequence determines the degree of unbalance of a power grid. For claryfication, Fig.B.5 illustrates the three sets of sequences (homopolar, positive and negative) separated, and summed in each phase.

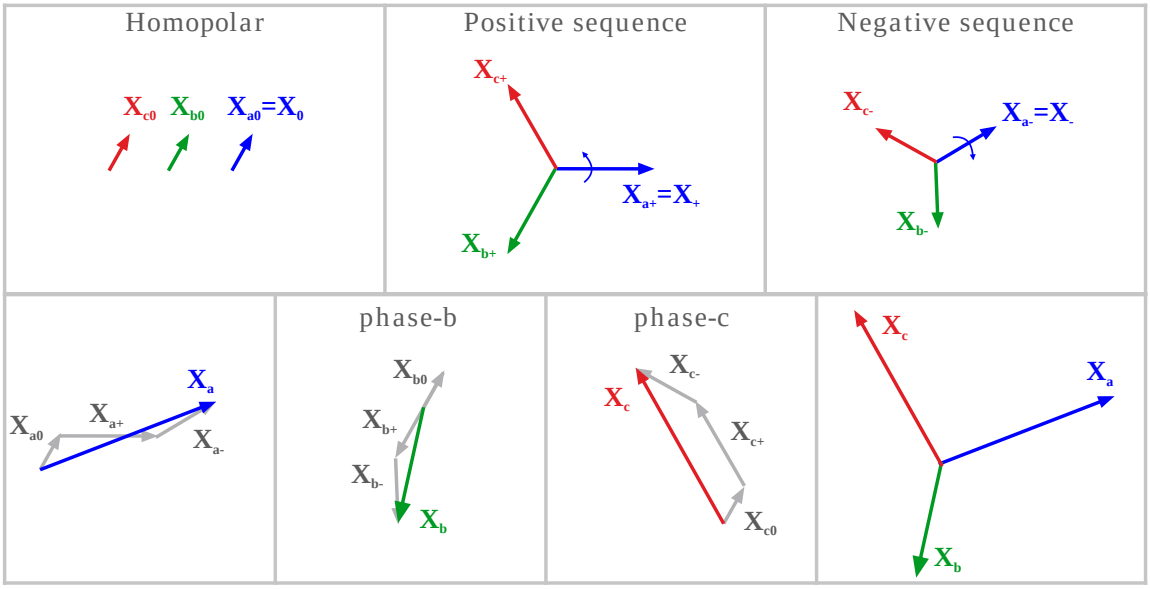


Figure B.5: Symmetrical components

The equation set (B.1) can be rewritten as a sum of a zero-sequence, a positive-sequence, and a negative-sequence. When there are harmonics, it is possible to write these expressions in a generic form:

$$\begin{aligned} x_a(t) &= X_0(t) + X_{a+}(t) + X_{a-} = \\ &= \sum_{h=1}^{\infty} \hat{X}_{h0} \cos(h\omega_1 t + \varphi_{h0}) \\ &+ \sum_{h=1}^{\infty} \hat{X}_{h+} \cos\left[h\omega_1 t + \varphi_{h+}\right] + \sum_{h=1}^{\infty} \hat{X}_{h-} \cos\left[-\left(h\omega_1 t + \varphi_{h-}\right)\right] \end{aligned} \tag{B.13a}$$

$$\begin{aligned} x_b(t) &= X_0(t) + X_{b+}(t) + X_{b-} = \\ &= \sum_{h=1}^{\infty} \hat{X}_{h0} \cos(h\omega_1 t + \varphi_{h0}) \\ &+ \sum_{h=1}^{\infty} \hat{X}_{h+} \cos\left[h\left(\omega_1 t - 2\pi/3\right) + \varphi_{h+}\right] + \sum_{h=1}^{\infty} \hat{X}_{h-} \cos\left[-\left(h\left\{\omega_1 t - 2\pi/3\right\} + \varphi_{h-}\right)\right] \end{aligned} \tag{B.13b}$$

$$\begin{aligned} x_c(t) &= X_0(t) + X_{c+}(t) + X_{c-} = \\ &= \sum_{h=1}^{\infty} \hat{X}_{h0} \cos(h\omega_1 t + \varphi_{h0}) \\ &+ \sum_{h=1}^{\infty} \hat{X}_{h+} \cos\left[h\left(\omega_1 t + 2\pi/3\right) + \varphi_{h+}\right] + \sum_{h=1}^{\infty} \hat{X}_{h-} \cos\left[-\left(h\left\{\omega_1 t + 2\pi/3\right\} + \varphi_{h-}\right)\right] \end{aligned} \tag{B.13c}$$

Or, the equivalent in phasor form (using *Clarke Transform*):

$$\begin{aligned}\mathbf{X}_{\alpha\beta}(t) &= \sum_{h=1}^{\infty}\left(\hat{X}_{h+}\cdot e^{j\varphi_{h+}}\right)\cdot e^{jh\omega_1 t} + \sum_{h=1}^{\infty}\left(\hat{X}_{h-}\cdot e^{-j\varphi_{h-}}\right)\cdot e^{-jh\omega_1 t} \\ &= \sum_{h=1}^{\infty}\mathbf{X_{h+}}\cdot e^{jh\omega_1 t} + \sum_{h=1}^{\infty}\mathbf{X_{h-}}\cdot e^{-jh\omega_1 t}\end{aligned} \tag{B.14a}$$

$$X_0(t) = \sum_{h=1}^{\infty}\hat{X}_{h0}\cos(h\omega_1 t + \varphi_{h0}) \tag{B.14b}$$

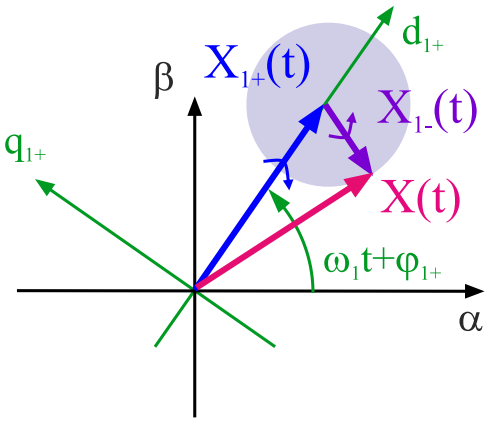


Figure B.6: Example of a rotating frame synchronized to the positive fundamental component

The last set of equations (B.14) is very helpul to understand one of the main problems of vector oriented control: the *other* sequences that project into the chosen rotating frame. If the three-phase signal is balanced and with no harmonic distortion, just the fundamental positive-sequence is present. This means that, if the rotating frame is inlined with the fundamental positive-sequence, the d_{1+} and q_{1+} axes will only yield constant values. However, if the three-phase signal is unbalanced and with harmonic components, the d_{1+} and q_{1+} axes will have external projected components that do not correspond to the positive fundamental sequence.

$$\begin{aligned}\mathbf{X}_{dq(1+)}(t) &= \mathbf{X}_{\alpha\beta}(t)\cdot e^{-j\omega_1 t} = \\ &= \mathbf{X_{1+}} + \sum_{h=2}^{\infty}\mathbf{X_{h+}}\cdot e^{j(h-1)\omega_1 t} + \sum_{h=1}^{\infty}\mathbf{X_{h-}}\cdot e^{-j(h+1)\omega_1 t}\end{aligned} \tag{B.15}$$

For example, if the analyzed signal is composed of a fundamental positive-sequence and a fundamental negative-sequence, and the rotating frame is synchronized with the fundamental positive-sequence, the d_{1+} and q_{1+} axes projections will present a constant value and a sinusoidal component oscillating at double of the fundamental frequency:

$$\mathbf{X}_{dq(1+)}(t) = \mathbf{X}_{\alpha\beta}(t)\cdot e^{-j\omega_1 t} = \mathbf{X_{1+}} + \mathbf{X}_{1-}\cdot e^{-j2\omega_1 t} \tag{B.16}$$

3. Active and reactive power calculation of generic waveforms

The concepts of active, reactive and apparent powers are quite clear for single-phase sinusoidal waveforms. For example, if an ideal (purely sinusoidal) single-phase system is defined by

$$v(t) = \sqrt{2}V \cdot \sin(\omega t) \qquad i(t) = \sqrt{2}I \cdot \sin(\omega t - \phi) \tag{B.17}$$

where V and I are RMS values, the instantaneous (active) power is given by the product of the instantaneous voltage and current:

$$\begin{aligned} p(t) = v(t) \cdot i(t) &= VI\cos\phi[1 - \cos(2\omega t)] - VI\sin\phi[1 - \sin(2\omega t)] \\ &= P[1 - \cos(2\omega t)] - Q[1 - \sin(2\omega t)] \end{aligned} \tag{B.18}$$

The first member of equation (B.18) has an average value of $P = VI\cos\phi$ and an ovelapped oscillating component at double the voltage frequency. This average value is known as active (average) power. This power represents the power consumed, in average, by the load.

The second member of equation (B.18), has a null average value since it is composed of a single term oscillating at double of the voltage frequency. The expression $Q = VI\sin\phi$ is denoted as reactive power. The reactive power has been defined as the power does not realize work, oscillating power, or the power with average value zero. These definitions, specially the later, are valid for sinusoidal single-phase systems.

The apparent power is defined as $S = VI = \sqrt{P^2 + Q^2}$, and it represents the maximum reachable active power at unity power factor.

In electric power systems it is also common to represent P and Q as the real and imaginary parts of a complex apparent power. This complex apparent power is defined as the product of voltage phasor and the conjugate of the current phasor as as,

$$\mathbf{S} = P + jQ = \mathbf{V} \cdot \mathbf{I}^* = [V \cdot e^{j\theta_v}] \cdot [I \cdot e^{j\theta_i}]^* = VI\cos(\theta_v - \theta_i) + jVI\sin(\theta_v - \theta_i) \tag{B.19}$$

where V and I are RMS values, and θ_v and θ_i are the phase-angles of voltage and current, respectively. The module of the complex apparent power is, actually, the value of the apparent power: $\|\mathbf{S}\| = S = VI$.

For polyphase non-sinusoidal systems the definition of active and reactive powers has originated substatial debate in the research community. And, still, a total consensus has not been achieved. The generalization of a power theory is the subject of many specialized papers, where two main trends can be highlighted [217]: (i) the approaches based on active and non-active power and current separation, and (ii) the PQ-theories.

3.1. Approaches based on active and non-active power-component separation.

These research current was initiated by Budeanu, in 1927 [218, 219], and by Frize, in 1932 [220]. The concept proposed by Budeanu was defined in the frequency domain, whereas the concept defined by Fryze was defined in the time-domain. The concept presented by Budeanu did not have much continuation in power-electronics applications because it requires the calculation of the frequency

components, which constraints the real-time operation. The theory presented by Fryze was subsequently completed by different researchers. Depenbrock [221] extended extended Fryze's definition of non-active power and current decomposition method for a single-phase to a polyphase system, and named it FBD-method in honour to Fryze, Buchnolz and Depenbrock. The FBD theory just applies for stationary waveforms. For this reason, a generalization of FBD to non-stationary signals has been recently proposed by [222, 223], where FBD is a particular case of the *generalized non-active power theory*. The principles of these theories are explained next [16, 223]:

3.1.1. Power definitions by Budeanu

The power definitions given by Budeanu are based on single-phase non-sinusoidal systems:

- The **apparent power**, S, is defined as the product between the RMS voltage and current.

$$S = V \cdot I \tag{B.20}$$

  where the RMS values are defined as,

$$V = \sqrt{\frac{1}{T}\int_0^T v(t)^2 dt} \qquad I = \sqrt{\frac{1}{T}\int_0^T i(t)^2 dt} \tag{B.21}$$

  where T is the period of the fundamental wave.

- **Active and reactive powers**, P and Q, is given by

$$P = \sum_{n=1}^{\infty} P_n = \sum_{n=1}^{\infty} V_n I_n \cos\varphi_n \qquad Q = \sum_{n=1}^{\infty} Q_n = \sum_{n=1}^{\infty} V_n I_n \sin\varphi_n \tag{B.22}$$

  where the subscript n denothes the n-th harmonic component, and φ_n the phase displacement between voltage and current harmonic components.

  These definitions of P and Q are somehow incomplete because they do not take into account the cross-products between voltage and current harmonics of different frequencies. They do not correctly characterize the loss of power quality under non-sinusoidal conditions. In order to compensate this deficiency Budeanu proposed another term, called *distortion power*, D, to represent the distortion of the waveforms.

- **Distortion power**, D, is defined as,

$$D^2 = S^2 - P^2 - Q^2 \tag{B.23}$$

  These powers can be represented graphically in a three-dimensional plane.

The reactive and apparent powers defined by Budeanu do not have a clear physical meaning, as is the case of active power, which represents the average ratio of energy transfer between two energy subsystems. According to [16], these mathematical formulations may lead to false interpretations when extended to polyphase systems.

3.1.2. Power definitions by Fryze

The power definitions proposed by Fryze correspond to single-phase systems:

- **Active power**, P_w:

$$P_w = \frac{1}{T}\int_0^T p(t)dt = \frac{1}{T}\int_0^T v(t)i(t)dt = V_w I = V I_w \tag{B.24}$$

  where V and I are the RMS voltage and current values, and V_w and I_w are the active voltages and currents as defined later.

- **Apparent power**, P_s:

$$P_s = VI \tag{B.25}$$

- **Active power factor**, λ:

$$\lambda = \frac{P_w}{P_s} \tag{B.26}$$

- **Active voltages and currents**, V_w and I_w:

$$V_w = \lambda \cdot V \qquad I_w = \lambda \cdot I \tag{B.27}$$

- **Reactive power**, P_q:

$$P_q = \sqrt{{P_s}^2 + {P_w}^2} = V_q I = V I_q \tag{B.28}$$

- **Reactive power factor**, λ_q:

$$\lambda_q = \sqrt{1-\lambda^2} \tag{B.29}$$

- **Reactive voltages and currents**, V_q and I_q:

$$V_q = \lambda_q \cdot V \qquad I_q = \lambda_q \cdot I \tag{B.30}$$

3.1.3. The FBD theory

Depenbrock extended Fryze's definition of non-active power and current decomposition from single-phase systems to polyphase systems with an arbitrary number of m phases, making no special distinctions between phases. The theory of Depenbrock makes uses of the *instantaneous collective values* of voltage, v_Σ, and current, i_Σ, proposed precedingly by Buchholz [224], which are defined as

$$\begin{gathered} v_\Sigma = \sqrt{\sum_{\mu=1}^{m} {v_\mu}^2}, \qquad i_\Sigma = \sqrt{\sum_{\mu=1}^{m} {i_\mu}^2} \\ \|v_\Sigma\|^2 = \overline{v_\Sigma{}^2} = \sum_{\mu=1}^{m} \|v_\mu\|^2 \qquad \|i_\Sigma\|^2 = \overline{i_\Sigma{}^2} = \sum_{\mu=1}^{m} \|i_\mu\|^2 \end{gathered} \tag{B.31}$$

where vectors $\mathbf{v}$ and $\mathbf{i}$ are multidimensional vectors of the form $\mathbf{v} = [v_1\ v_2\ \cdots\ v_m]^t$ and $\mathbf{i} = [i_1\ i_2\ \cdots\ i_m]^t$, and m is the number of phases.

The instantaneous collective power, $p_\Sigma(t)$, and the instantaneous collective power current, $i_{\Sigma p}$, are

defined as,

$$p_\Sigma(t) = \sum_{\mu=1}^{m} p_\mu = \sum_{\mu=1}^{m} v_\mu i_\mu \qquad i_{\Sigma p} = \frac{p_\Sigma(t)}{{v_\Sigma}^2} v_\Sigma \tag{B.32}$$

and the instantaneous collective apparent power,

$$S_\Sigma = \|v_\Sigma\| \cdot \|i_\Sigma\| \tag{B.33}$$

According to Depenbrock, powers and currents can be divided into active and non-active components, where non-active powers are quantities of secondary importance that must be normally derived after the non-active currents, and not viceversa [221]. Depending on the use, non-active components can further be splitted into (i) power and zero components, (ii) active, variation, and zero components, or (iii) active and non-active components:

$$i_\mu = i_{\mu p} + i_{\mu z} = i_{\mu a} + i_{\mu v} + i_{\mu z} = i_{\mu a} + i_{\mu n} \tag{B.34}$$

where

$$\begin{aligned} i_{\mu p} &= \frac{p_\Sigma}{{v_\Sigma}^2} v_\mu \qquad i_{\mu a} = \frac{\overline{p_\Sigma}}{{v_\Sigma}^2} v_\mu \\ i_{\mu z} &= i_\mu - i_{\mu p} \\ i_{\mu v} &= i_{\mu p} - i_{\mu q} \\ i_{\mu n} &= i_\mu - i_{\mu a} = i_{\mu z} + i_{\mu v} \end{aligned} \tag{B.35}$$

Powers are obtained by multiplying these current values with the respective phase voltages.

3.1.4. Generalized instantaneous non-active power theory

The generalized instantaneous non-active power theory is an extension of the FBD theory proposed by Depenbrock. The objective of this theory is to also address non-stationary signals. For this purpose it uses time-varying quantities and moving average values [223]. The current, $\mathbf{i}$, is decomposed into an active current, $\mathbf{i_p}$, and a non-active current, $\mathbf{i_q}$: $\mathbf{i}(t)=\mathbf{i_p}(t)+\mathbf{i_q}(t)$.

The active power is defined as

$$\mathbf{i_p}(t) = \frac{P_L(t)}{{V_p(t)}^2} \mathbf{v_p}(t) \tag{B.36}$$

where

$$V_p(t) = \sqrt{\frac{1}{T_c} \int_{t-T_c}^{t} \mathbf{v_p}(\tau)^T \mathbf{v_p}(\tau) d\tau} \qquad P_L(t) = \frac{1}{T_c} \int_{t-T_c}^{t} \mathbf{v_p}(\tau)^T \mathbf{i_p}(\tau) d\tau \tag{B.37}$$

3.2. PQ-Theories.

PQ theories present a different approach to define instantaneous active and reactive powers. The Instantaneous Reactive Power Theory was first presented by Akagi, Kanazawa and Nabae [225] in 1983. This theory was originally defined for three-phase, three-wire systems, but the authors proposed subsequently a modification in which the homopolar components could be also considered [226].

In their first modification they considered the homopolar variables as an independent single-phase

circuit separated from the other components, and they just defined and active homopolar power. In 1996, Peng and Lai [227] proposed the Generalized Instantaneos Reactive Power Theory, in which the homopolar voltages and currents do not only affect the active homopolar power, but also the reactive homopolar power. Moreover, the advantage of this formulation is that it can be used in the natural *abc* frame without the need of any transformations. However, any other frame can be used provided that the power invariance is preserved (e.g. Concordia Transformation).

In this generalized version of PQ theories, active powers are calculated as dot products of vectors, and reactive powers are calculated by the cross-products of voltages and currents. In [228] Willems provide a very interesting interpretation of the Instantaneous Reactive Power Theory and compares it to Fryze's approach, showing that there is a relationship between both theories.

PQ theories are the most common and expanded power theories used for active filtering. In the following lines the main features of the Generalized Instantaneous Power Theory are summarized. Further explanations on power theories for active filtering can be found in [202].

3.2.1. Coordinate transformation (optional)

The coordinate transformation is optional in the Generalized Instantaneous Power Theory. It can be applied in the *abc* natural frame or in any other frame provided that the transformation matrix ensures the power invariance. This is, the transformation matrix must be orthogonal [202]. In this development, for a demonstration purpose, a natural *abc* frame and a static $\alpha\beta$ frame are selected.

The instantaneous $\alpha\beta$ values are obtained by Concordia transform:

$$\mathbf{v}_{\alpha\beta} = \mathbf{C} \cdot \mathbf{v}_{\mathbf{abc}} \qquad \mathbf{i}_{\alpha\beta} = \mathbf{C} \cdot \mathbf{i}_{\mathbf{abc}} \tag{B.38}$$

where C stands for the Concordia transform (eq.(B.2) with $k = \sqrt{3/2}$), and $\mathbf{v_{abc}} = [v_a \ v_b \ v_c]^t$, $\mathbf{i_{abc}} = [i_a \ i_b \ i_c]^t$, $\mathbf{v}_{\alpha\beta} = [v_\alpha \ v_\beta \ v_0]^t$, $\mathbf{i}_{\alpha\beta} = [i_\alpha \ i_\beta \ i_0]^t$.

3.2.2. Instantaneous active power definition

The instantaneous active power is defined as the dot product between the multidimensional voltage and current vectors,

$$p = \mathbf{v} \bullet \mathbf{i} \tag{B.39}$$

or, in other terms,

$$p = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad p = \begin{bmatrix} v_\alpha & v_\beta & v_0 \end{bmatrix} \cdot \begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} \tag{B.40}$$

which yields,

$$p = v_a \cdot i_a + v_b \cdot i_b + v_c \cdot i_c = v_\alpha \cdot i_\alpha + v_\beta \cdot i_\beta + v_0 \cdot i_0 \tag{B.41}$$

3.2.3. Instantaneous reactive power definition

The instantaneous reactive power is defined as the modulus of the reactive power vector, which is defined as the cross-product between voltage and current vectors,

$$\mathbf{q} = \mathbf{v} \times \mathbf{i} \tag{B.42}$$

The $\mathbf{q}$ vector is composed of three components:

$$\begin{bmatrix} q_\alpha \\ q_\beta \\ q_0 \end{bmatrix} = \begin{bmatrix} \begin{vmatrix} v_\beta & v_0 \\ i_\beta & v_0 \end{vmatrix} \\ \begin{vmatrix} v_0 & v_\alpha \\ i_0 & i_\alpha \end{vmatrix} \\ \begin{vmatrix} v_\alpha & v_\beta \\ i_\alpha & i_\beta \end{vmatrix} \end{bmatrix} \qquad \begin{bmatrix} q_a \\ q_b \\ q_c \end{bmatrix} = \begin{bmatrix} \begin{vmatrix} v_b & v_c \\ i_b & v_c \end{vmatrix} \\ \begin{vmatrix} v_c & v_a \\ i_c & i_a \end{vmatrix} \\ \begin{vmatrix} v_a & v_b \\ i_a & i_b \end{vmatrix} \end{bmatrix} \tag{B.43}$$

Considering that $\|C\| = 1$, $\|\mathbf{q_{abc}}\| = \|\mathbf{q}_{\alpha\beta}\|$. Thus, the instantaneous reactive power is defined as,

$$q_{\{>0 \Rightarrow capacitive\}} = \|\mathbf{q}\| = \|\mathbf{v} \times \mathbf{i}\| \tag{B.44}$$

It must be noted that, the definition presented in equation (B.42) yields a positive value when the current is leading the voltage (capacitive behaviour). In this PhD, the positive value of the instantaneous reactive power is defined for an inductive behaviour; this is, when the current lags the voltage. This reference change can be done by inverting the sign of equation (B.42),

$$\mathbf{q} = -\mathbf{v} \times \mathbf{i} \qquad q_{\{>0 \Rightarrow inductive\}} = \|-\mathbf{q}\| = \|-\mathbf{v} \times \mathbf{i}\| \tag{B.45}$$

For three-phase three-wire systems with no homopolar components, it is possible to define an *instantaneous complex power* similar to that presented in equation (B.19) for single-phase systems [16]. The instantaneous apparent power of voltage and current waveforms is given by the phasor multiplication of voltage and current phasors, using the conjugate form of the current:

$$\mathbf{s} = p + jq_{\{>0 \Rightarrow inductive\}} = \mathbf{v} \cdot \mathbf{i}^* = (v_\alpha + jv\beta) \cdot (i_\alpha + ji\beta)^* = [v_\alpha i_\alpha + v_\beta i_\beta] + j[v_\beta i_\alpha - v_\alpha i_\beta] \tag{B.46}$$

3.3. Active and reactive power calculation in three-phase three-wire systems

Before developping the active and reactive power equations for three-phase three-wire systems, it is important to highlight an important point in relation with Clarke and Concordia transforms.

3.3.1. Power equivalences between Clarke and Concordia

All along this PhD, Clarke Transformation is used to obtain the static $\alpha\beta$ components. However, Clarke transformation is not orthogonal and does not provide power invariance. For this reason, care must be taken when handling power definitions because, when using Clarke, equation (B.46) is not totally true (there is a difference of a coeffient). Power equations must be formulated according to

Concordia (and not Clarke), knowing that

$$\mathbf{S^{co}} = \mathbf{V^{co}} \cdot \mathbf{I^{co*}} = \left(\sqrt{3/2}\ \mathbf{V^{cl}}\right) \cdot \left(\sqrt{3/2}\ \mathbf{I^{cl}}\right)^* = \frac{3}{2}\ \mathbf{S^{cl}} \tag{B.47}$$

where *co* and *cl* subscripts stand for Concordia and Clarke transformations, respectively. This means that, when using voltage and current values that have been transformed using the Clarke matrix (that is the case), power equations must include a 3/2 term for three-phase powers, and a 1/2 term for single-phase powers. Accordingly, the base power values have been formulated respecting the power equivalence.

Using these power and base-power definitions the instantaneous apparent power vector becomes the same in per-unit:

$$\begin{aligned} \mathbf{s} = \frac{\mathbf{S^{co}}}{S_b^{co}} = \frac{\mathbf{V^{co}} \cdot \mathbf{I^{co*}}}{V_b^{co} \cdot I_b^{co}} = \mathbf{v^{co}} \cdot (\mathbf{i^{co}})^* = \\ = \frac{\left(\sqrt{3/2}\ \mathbf{V^{cl}}\right) \cdot \left(\sqrt{3/2}\ \mathbf{I^{cl}}\right)^*}{\sqrt{3/2}\ V_b^{cl} \cdot \sqrt{3/2}\ I_b^{cl}} = \mathbf{v^{cl}} \cdot (\mathbf{i^{cl}})^* \end{aligned} \tag{B.48}$$

Thus,

$$\mathbf{s} = \mathbf{v^{co}} \cdot \mathbf{i^{co*}} = \mathbf{v^{cl}} \cdot \mathbf{i^{cl*}} \tag{B.49}$$

Note that per-unit values are in lower-case letters and that, in this PhD, for per-unit conversion, the single-phase base-power is defined as $S_b = 0.5 V_b I_b$.

3.3.2. Generic power equations for three-phase three-wire systems in phasor form

Equations (B.46) or (B.49) (in per-unit) are very helpful for calculating the generic expressions of active and reactive powers of voltage and current waveforms. Expression (B.49) is therefore used for calculating active and reactive powers in three-phase three-wire systems. For this development only the positive and negative sequences have been considered, the homopolar components have been disregarded. The development is performed in phasor-form.

The calculation begins by developping (B.49):

$$\begin{aligned} \mathbf{s}(t) = \mathbf{v}(t) \cdot \mathbf{i}(t)^* &= \left[\sum_{h=1}^{\infty} \mathbf{v_{(h+)}} \cdot e^{jh\omega_1 t} + \mathbf{v_{(h-)}} \cdot e^{-jh\omega_1 t}\right] \cdot \left[\sum_{k=1}^{\infty} \mathbf{i_{(k+)}} \cdot e^{jk\omega_1 t} + \mathbf{i_{(k-)}} \cdot e^{-jk\omega_1 t}\right]^* \\ &= \left[\sum_{h=1}^{\infty} \mathbf{v_{(h+)}} \cdot e^{jh\omega_1 t} + \mathbf{v_{(h-)}} \cdot e^{-jh\omega_1 t}\right] \cdot \left[\sum_{k=1}^{\infty} \mathbf{i_{(k+)}}^* \cdot e^{-jk\omega_1 t} + \mathbf{i_{(k-)}}^* \cdot e^{jk\omega_1 t}\right] \end{aligned} \tag{B.50}$$

where ω_1 is the fundamental frequency, and $\mathbf{v_{(h+)}}$, $\mathbf{i_{(h+)}}$, $\mathbf{v_{(k-)}}$, $\mathbf{i_{(k-)}}$, are the time-independent harmonic voltage and current phasors refered to the multi-frequency positive and negative rotating frames as,

$$\mathbf{v_{(h+)}} = \hat{v}_{(h+)} \cdot e^{j\varphi_{h+}} = v_{d(h+)} + j v_{d(h+)} \qquad \mathbf{i_{(h+)}} = \hat{i}_{(h+)} \cdot e^{j\gamma_{h+}} = i_{d(h+)} + j i_{d(h+)}$$
$$\mathbf{v_{(k-)}} = \hat{v}_{(k-)} \cdot e^{-j\varphi_{k-}} = v_{d(k-)} + j v_{d(k-)} \qquad \mathbf{i_{(k-)}} = \hat{i}_{(k-)} \cdot e^{-j\gamma_{k-}} = i_{d(k-)} + j i_{d(k-)}$$

Developping (B.50), three types of terms are found: (1) time-independent complex values with constant magnitude, (2) values that oscillate at double the fundamental frequency (in the positive and negative direction), and (3) values that oscillate at other frequencies. The three types of terms are presented separately below:

$$\bar{\mathbf{s}} = \sum_{h=1}^{\infty} \mathbf{v_{(h+)}} \cdot \mathbf{i_{(h+)}}^* + \sum_{h=1}^{\infty} \mathbf{v_{(h-)}} \cdot \mathbf{i_{(h-)}}^* \tag{B.51}$$

$$\tilde{\mathbf{s}}_{\mathbf{2\omega_1}} = \sum_{h=1}^{\infty} \mathbf{v_{(h+)}} \cdot \mathbf{i_{(h-)}}^* \cdot e^{j2h\omega_1 t} + \sum_{h=1}^{\infty} \mathbf{v_{(h-)}} \cdot \mathbf{i_{(h+)}}^* \cdot e^{-j2h\omega_1 t} \tag{B.52}$$

$$\begin{aligned} \tilde{\mathbf{s}}_{other\ terms} = & \sum_{\substack{h=1 \\ h\neq k}}^{\infty} \sum_{k=1}^{\infty} \mathbf{v_{(h+)}} \cdot \mathbf{i_{(k+)}}^* \cdot e^{j(h-k)\omega_1 t} \\ & \sum_{\substack{h=1 \\ h\neq k}}^{\infty} \sum_{k=1}^{\infty} \mathbf{v_{(h+)}} \cdot \mathbf{i_{(k-)}}^* \cdot e^{j(h+k)\omega_1 t} \\ & + \sum_{\substack{h=1 \\ h\neq k}}^{\infty} \sum_{k=1}^{\infty} \mathbf{v_{(h-)}} \cdot \mathbf{i_{(k+)}}^* \cdot e^{-j(h+k)\omega_1 t} \\ & + \sum_{\substack{h=1 \\ h\neq k}}^{\infty} \sum_{k=1}^{\infty} \mathbf{v_{(h-)}} \cdot \mathbf{i_{(k-)}}^* \cdot e^{-j(h-k)\omega_1 t} \end{aligned} \tag{B.53}$$

where $\mathbf{s} = \bar{\mathbf{s}} + \tilde{\mathbf{s}}_{\mathbf{2\omega_1}} + \tilde{\mathbf{s}}_{other\ terms}$. Active and reactive powers for the non-homopolar components are calculated by obtaining the real and imaginary parts of $\mathbf{s}(t)$.

$$p(t) = \Re\{\mathbf{s}(t)\} \qquad q(t) = \Im\{\mathbf{s}(t)\} \tag{B.54}$$

3.3.3. Power equations for three-phase three-wire systems under fundamental positive and negative sequences

These generic expressions are subsequently used to deduce a particular example in which just the fundamental components of the positive and negative sequences exist. This development is interesting to understand some of the concepts (e.g. dual vector control) that are used in this PhD. From equation (B.50), the instantaneous apparent power of a system with only fundamental positive and negative sequences yields,

$$\begin{aligned} \mathbf{s}(t) = \mathbf{v}(t) \cdot \mathbf{i}(t)^* &= \left[\mathbf{v_{(1+)}} \cdot e^{j\omega_1 t} + \mathbf{v_{(1-)}} \cdot e^{-j\omega_1 t}\right] \cdot \left[\mathbf{i_{(1+)}} \cdot e^{j\omega_1 t} + \mathbf{i_{(1-)}} \cdot e^{-j\omega_1 t}\right]^* \\ &= \left[\mathbf{v_{(1+)}} \cdot e^{j\omega_1 t} + \mathbf{v_{(1-)}} \cdot e^{-j\omega_1 t}\right] \cdot \left[\mathbf{i_{(1+)}}^* \cdot e^{-j\omega_1 t} + \mathbf{i_{(1-)}}^* \cdot e^{j\omega_1 t}\right] \end{aligned} \tag{B.55}$$

where $\mathbf{v_{(1+)}} = v_{d(1+)} + jv_{d(1+)}$, $\mathbf{v_{(1-)}} = v_{d(1-)} + jv_{d(1-)}$, $\mathbf{i_{(1+)}} = i_{d(1+)} + ji_{d(1+)}$, and $\mathbf{i_{(1-)}} = i_{d(1-)} + ji_{d(1-)}$.

In this case, since the voltage and the current just have one harmonic component (the fundamental), $\tilde{\mathbf{s}}_{other\ terms} = 0$. After operating equation (B.55), it is possible to observe that the active and reactive power are composed by a constant term and two fluctuating terms oscillating at double the fundamental frequency:

$$\begin{aligned} p(t) &= \bar{p} + \tilde{p}_{2\omega_1} = \bar{p} + p_{c2} \cdot \cos(2\omega_1 t) + p_{s2} \cdot \sin(2\omega_1 t) \\ q(t) &= \bar{q} + \tilde{q}_{2\omega_1} = \bar{q} + q_{c2} \cdot \cos(2\omega_1 t) + q_{s2} \cdot \sin(2\omega_1 t) \end{aligned} \tag{B.56}$$

where the expressions of $\bar{p}$, p_{c2}, p_{s2}, $\bar{q}$, p_{q2}, and p_{q2} are:

$$\begin{bmatrix} \bar{p} \\ p_{c2} \\ p_{s2} \\ \bar{q} \\ q_{c2} \\ q_{s2} \end{bmatrix} = \begin{bmatrix} v_{d(1+)} & +v_{q(1+)} & +v_{d(1-)} & +v_{q(1-)} \\ v_{d(1-)} & +v_{q(1-)} & +v_{d(1+)} & +v_{q(1+)} \\ v_{q(1-)} & -v_{d(1-)} & -v_{q(1+)} & +v_{d(1+)} \\ v_{q(1+)} & -v_{d(1+)} & +v_{q(1-)} & -v_{d(1-)} \\ v_{q(1-)} & -v_{d(1-)} & +v_{q(1+)} & -v_{d(1+)} \\ -v_{d(1-)} & -v_{q(1-)} & +v_{d(1+)} & +v_{q(1+)} \end{bmatrix} \cdot \begin{bmatrix} i_{d(1+)} \\ i_{q(1+)} \\ i_{d(1-)} \\ i_{q(1-)} \end{bmatrix} \tag{B.57}$$

3.3.4. Power equations for three-phase three-wire systems under the fundamental positive sequence

For a system where just the fundamental of the positive sequence exists, oscillating terms do not appear:

$$\begin{aligned} p(t) &= \bar{p} = v_{d(1+)} i_{d(1+)} + v_{q(1+)} i_{q(1+)} \\ q(t) &= \bar{q} = v_{q(1+)} i_{d(1+)} - v_{d(1+)} i_{q(1+)} \end{aligned} \tag{B.58}$$

Appendix C

On some concepts related to synchronization methods

As a complement to Chapter III.6, Appendix C provides some basic concepts of well-known synchronization techniques.

1. DFT-based techniques

DFT-based techniques, specially the recursive version of DFT (RDFT), are very interesting filtering techniques due to their simplicity (they do not need a complicated design stage), their low computational burden, their speed, and their good filtering characteristics. However, it is important to highlight that they are only intended for **single-phase** signals.

The main drawback of DFT-based techniques is that the number of samples per cycle needs to be an integer number. If the DFT sampling is asynchronous to the fundamental frequency of the grid voltage, phase errors occur due to a phenomenon called spectral leakage [229, 230]. This phenomenon is specially noticeable when the fundamental frequency varies. Many different strategies have been reported in literature to face this problem. Among the proposed strategies, the most spread strategies are two:

- The first strategy corrects the number of samples in a period as to perfectly match the fundamental frequency [230].
- The second strategy estimates the phase-error and compensates for it [230, 231, 232].

Simulations and experimental results in [230] have proven that the first approach, the window correction method, achieves the best performance because it ensures that harmonic components are rejected until the aliasing frequency and the sub-harmonics are attenuated 20 dB/decade. The second method, the phase-offset correction method, achieves a sub-optimal filtering characteristics where harmonic distortion is only attenuated 20 dB/decade. In spite of the good properties of the window correction method, it has a potential difficulty that lies on the incapability of many systems in working at variable sampling frequency. These methods are able to cope with frequency changes of up to 40 Hz/s.

1.1. Basic concept of RDFT [230]

Consider a time signal $x(t)$ that is sampled at a rate N/T_ω to produce the time sequence $\{x_n\}$, which contains N data points. The time interval T_ω is the window for the DFT. the DFT producing the

m-th harmonic of $\{x_n\}$ at the frequency m/T_ω at the time step $k-1$ can be written as:

$$\mathbf{X_m(k-1)} = \sum_{n=k-N}^{k-1} x_n \, e^{-\mathbf{j}\frac{2\pi(n-1)m}{N}} \tag{C.1}$$

One time-step later, a new sample $x(t)$ is taken and the DFT at time-step k becomes

$$\mathbf{X_m(k)} = \sum_{n=k-N+1}^{k} x_n \, e^{-\mathbf{j}\frac{2\pi(n-1)m}{N}} \tag{C.2}$$

Substracting (C.1) from (C.2), the recursive expression of the DFT is obtained

$$\mathbf{X_m(k)} = \mathbf{X_m(k-1)} + [x_k - x_{k-1}] \, e^{-\mathbf{j}\frac{2\pi(k-1)m}{N}} \tag{C.3}$$

For power system line filtering, if the time windown T_ω is made equal to the system period, then $m = 1$. In order to extract the phase-angle of the fundamental ($\theta_1(k)$) it is just necessary to:

$$\theta_1(k) = \arctan \frac{\Im\{\mathbf{X_1(k)}\}}{\Re\{\mathbf{X_1(k)}\}} \tag{C.4}$$

2. Space-vector filter (SVF) techniques

The SVF is a low-pass filter modelled in the static $\alpha\beta$ frame. As the other open-loop methods, the SVF needs a complementary module to estimate the grid frequency. The extended SVF (eSVF) proposed in [233], for example, integrates a feedback loop capable of estimating the grid frequency. However the proposed solution is not totally effective since the parallel operation of the frequency regulator and the SVF generates a conflict between frequency tracking and phase-jump identification.

2.1. Basic concept of the Space Vector Filter (SVF) [233]

The Space Vector Filter (SVF) is a low-pass filter for space-vectors. The filter uses a model of the grid voltage vector, $\mathbf{e_{SVF(\alpha\beta)}} = e_{SVF_\alpha} + \mathbf{j}\ e_{SVF_\beta}$ that is updated every time sample. By assuming a constant sampling time and a constant grid-frequency, the grid voltage vector can be estimated for the next sample. The value of the forgetting factor, γ, determines how much influence the grid voltage vector has on the model of the grid-voltage. The filter equations are:

$$\begin{bmatrix} e_{SVF_\alpha}(k+1) \\ e_{SVF_\beta}(k+1) \end{bmatrix} = \gamma \begin{bmatrix} cos(\omega T_s) & -sin(\omega T_s) \\ sin(\omega T_s) & cos(\omega T_s) \end{bmatrix} \begin{bmatrix} e_{SVF_\alpha}(k) \\ e_{SVF_\beta}(k) \end{bmatrix} + \begin{bmatrix} 1-\gamma & 0 \\ 0 & 1-\gamma \end{bmatrix} \begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} \tag{C.5}$$

$$\begin{bmatrix} e_{filt_\alpha}(k) \\ e_{filt\beta}(k) \end{bmatrix} = \gamma \begin{bmatrix} cos(\omega T_s) & -sin(\omega T_s) \\ sin(\omega T_s) & cos(\omega T_s) \end{bmatrix} \begin{bmatrix} e_{SVF_\alpha}(k) \\ e_{SVF_\beta}(k) \end{bmatrix} + \begin{bmatrix} 1-\gamma & 0 \\ 0 & 1-\gamma \end{bmatrix} \begin{bmatrix} e_\alpha(k) \\ e_\beta(k) \end{bmatrix} \tag{C.6}$$

where the grid inputs are $\mathbf{e}_{(\alpha\beta)} = e_\alpha + \mathbf{j}\ e_\beta$, and the filtered values are $\mathbf{e_{filt(\alpha\beta)}} = e_{filt_\alpha} + \mathbf{j}e_{filt_\beta}$. When the forgetting factor is selected to be $\gamma = 1$ the mode has no connection with the grid inputs so the filter outputs are the same as the filter inputs. When $\gamma = 0$ the filter outputs have no relationship

with the inputs, as shown in Fig.C.1.

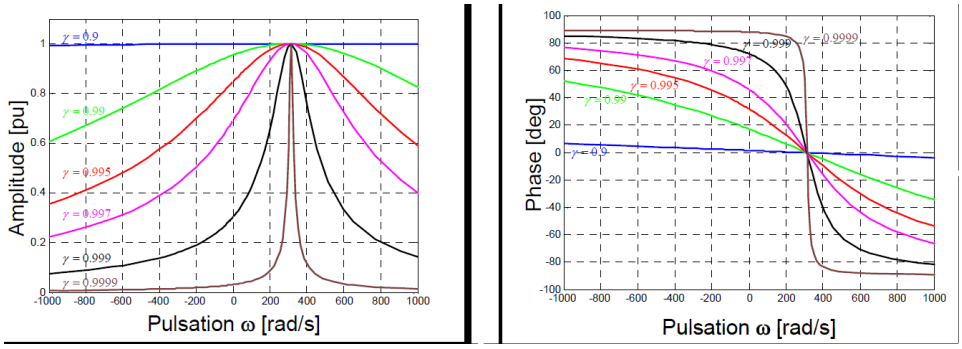


Figure C.1: Behaviour of the SVF according to γ (graph borrowed from [234])

3. Basic concept of the Adaptive Notch Filter (ANF) [235, 163]

The basic ANF structure is characterized by the following set of differential equations:

$$\begin{aligned} \ddot{x} &= -\theta^2 x + 2\zeta e(t) \\ \dot{\theta} &= -\gamma\theta x e(t) \\ e(t) &= u(t) - \dot{x} \end{aligned} \tag{C.7}$$

where $u(t)$ is the single-phase input signal, θ represents the estimated frequency, and ζ and γ are both real and positive parameters (the design parameters). For a single-phase sinusoidal signal $u(t) = A_1\, sing(\omega_0 + \varphi_1)$, the dynamical system of (C.7) has a unique periodic orbit located at

$$\mathcal{O} = \begin{pmatrix} x \\ \dot{x} \\ \theta \end{pmatrix} = \begin{pmatrix} -\frac{A_1}{\omega_0} cos(\omega_0 t + \varphi_1) \\ A_1\, sin(\omega_0 t + \varphi_1) \\ \omega_0 \end{pmatrix} \tag{C.8}$$

Equation (C.8) shows that the second entry of the periodic orbit (i.e. $\dot{x} = A_1\, sin(\omega_0 t + \varphi_1)$), coincides with the input signal $y(t)$ and that $-\theta x = A_1\, cos(\omega_0 t + \varphi_1)$ represents the 90° shifted signal.

In reality, the input signal is composed of several harmonic components and the expression of $y(t)$ becomes

$$y(t) = \sum_{i=1}^{n} A_i\, sin(i\omega_0 t + \varphi_i) = \sum_{i=1}^{n} y_i(t) \tag{C.9}$$

where A_i, φ_i, and ω_0 are real unknown parameters. In the same way, the system of equations of (C.7) can be rewritten as

$$\begin{aligned} \ddot{x} &= -k^2\,\theta^2 x_k + 2\zeta_k\, e(t) \\ \dot{\theta} &= -\gamma\theta x_1 e(t) \\ e(t) &= u(t) - \sum_{i=1}^{N} \dot{x}_i \end{aligned} \tag{C.10}$$

where k corresponds to the harmonic order $k = 1, 2, \ldots, N$, and ζ_k and γ_k are real positive numbers

that determine the behaviour of the k-th filter and the θ update law in terms of (steady-state) accuracy and (transien) convergence speed.

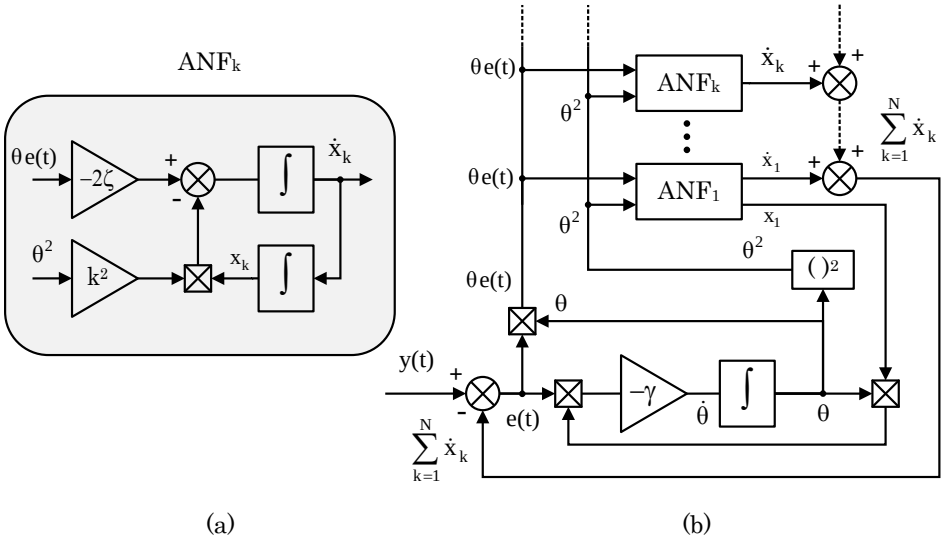


Figure C.2: (a) Structure of a generic, k-th harmonic, ANF (b) Full structure of the filter with k parallel ANFs.

4. The Kalman Filter applied to signal synchronization and sequence extraction

The Kalman filter (KF) is a common filter structure in communication and control applications. In power engineering, the use of Kalman filters is not common but it has already been used for detecting line faults, estimating electric machine parameters, detecting islanding operation of grid-connected converters, calculating the reference current of active power filters, or for monitoring purposes, for example [236].

The Kalman filter is an stochastic linear observer that is well suited for linear systems corrupted by uncertainties and noise. The classical Kalman Filter is usually tuned to a specific grid frequency value. If the grid frequency varies, KF needs an external system to identify the fundamental frequency. Very often these systems are based on measuring the time between two subsequent zero crossings (and averaging it over the time) [231], but some other authors have also used more advanced identification methods based on internal model control [168], for example. As a result, the accuracy and dynamics of KF, depends on the used frequency estimation method.

Alternatively, the Extended Kalman Filter (EKF), a nonlinear version of the Kalman Filter, can include the estimation of the frequency in its model. According to [233], the EKF is able to estimate grid frequency, angle and magnitude successfully but, depending on the type of disturbances, the weighting matrices must be adapted. The main problem of the EKF is finding the optimal weighting matrices and initial states that avoid that the filter diverges [168].

In general, authors prefer KF to EKF. Both KF and EKF can operate in weak grids (provided that the frequency is provided externally to the KF) and are adequate to work in very distorted environments.

An advantage of KF is its simple structure and implementation. When the signal or the measurements are very noisy (high process and measure noise covariance matrices) the bandwidth is reduced. The main drawback of KF and EKF is the high computational burden needed to process the algorithm. In some cases, however, it is possible to compute the Kalman gain offline.

4.1. Basic concept of the KF [229, 168]

Consider a signal with amplitude A_k, angular frequency ω_k, and phase θ_k

$$S_k = A_k \, sin(\omega_k t + \theta_k) \tag{C.11}$$

Let

$$x_{1k} = A_k \, sin(\omega_k t + \theta_k) \tag{C.12}$$

and,

$$x_{2k} = A_k \, cos(\omega_k t + \theta_k) \tag{C.13}$$

Initially, considering that $A_{k+1} \approx A_k$, $\omega_{k+1} \approx \omega_k$, and $\theta_{k+1} \approx \theta_k$. At $t_{k+1} = t_k + T_s$ the signal S_{k+1} may be expressed as

$$\begin{aligned} S_{k+1} =& A_{k+1} \, sin(\omega_k t_k + \omega_k T_s + \theta_{k+1}) = x_{1(k+1)} \\ =& x_{1k} \, cos(\omega_k T_s) + x_{2k} \, sin(\omega_k T_s) \end{aligned} \tag{C.14}$$

where T_s is the sampling period. Analogously,

$$\begin{aligned} x_{2(k+1)} =& A_{k+1} \, cos(\omega_k t_k + \omega_k T_s + \theta_{k+1}) \\ =& - x_{1k} \, sin(\omega_k T_s) + x_{2k} \, cos(\omega_k T_s) \end{aligned} \tag{C.15}$$

Finally, the state-space represenation of the KF when just one frequency is modelled is

$$\begin{aligned} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}_{k+1} &= \begin{bmatrix} cos(\omega_k t_k) & sin(\omega_k t_k) \\ -sin(\omega_k t_k) & cos(\omega_k t_k) \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}_k + \begin{bmatrix} \gamma_1 \\ \gamma_2 \end{bmatrix}_k \\ y_k &= \begin{bmatrix} 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}_k + \nu_k \end{aligned} \tag{C.16}$$

where γ_k and ν_k are uncorrelated Gaussian white noises of the process and measurement, respectively.

If the signal S_k includes harmonics, it becomes

$$S_k = \sum_{i=1}^{n} A_{ik} \, sin(i\omega_k t + \theta_{ik}) \tag{C.17}$$

and the state-variable representation becomes

$$\begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_{2n-1} \\ x_{2n} \end{bmatrix}_{k+1} = \begin{bmatrix} M_1 & \dots & 0 \\ \vdots & \ddots & \vdots \\ 0 & \dots & M_n \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_{2n-1} \\ x_{2n} \end{bmatrix}_k + \begin{bmatrix} \gamma_1 \\ \gamma_2 \\ \vdots \\ \gamma_{2n-1} \\ \gamma_{2n} \end{bmatrix}_k$$

$$y_k = \begin{bmatrix} 1 & 0 & \dots & 1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ \vdots \\ x_{2n-1} \\ x_{2n} \end{bmatrix}_k + \nu_k \tag{C.18}$$

where

$$M_i = \begin{bmatrix} cos(i\omega_k t_k) & sin(i\omega_k t_k) \\ -sin(i\omega_k t_k) & cos(i\omega_k t_k) \end{bmatrix} \tag{C.19}$$

The above described models can be represented by the generic model

$$\begin{cases} x_{k+1} = Fx_k + \gamma_k \\ y_k = Hx_k + \nu_k \end{cases} \tag{C.20}$$

which solution x_k can be found following the two-stepped process (a predicting stage and an updating stage) described in Fig.C.3.

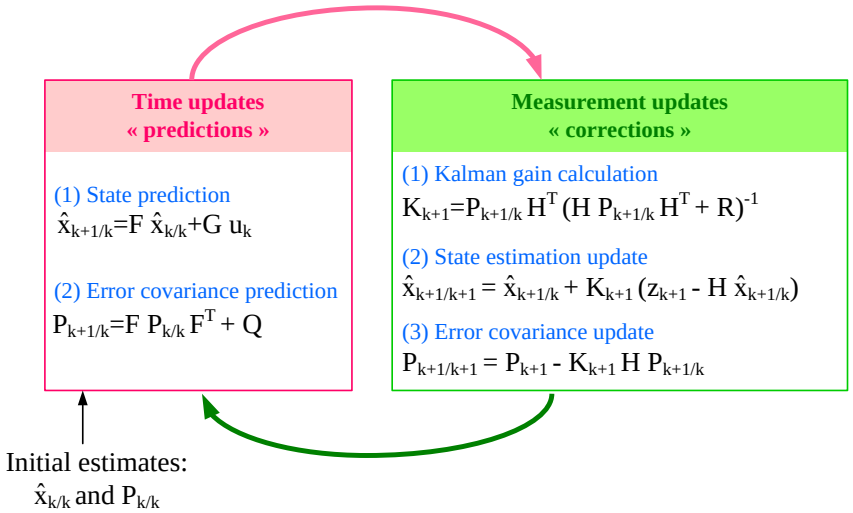


Figure C.3: Detailed description of the two-step process of the Kalman filter.

5. Artificial Neural Networks (ANN)

Artificial Neural Network techniques are based on Adaptive Linear Combiners (Adaline) and, according to [237, 238] yield more accurate and faster estimations than DFT techniques. The weight vector of the Adaline generates the Fourier coefficients of the signal. A similar concept, called Adaptive Linear Optimal Combiner (ALOF) is presented in [153]. The difference between Adaline and ALOF is that, the frequency and phase-angle used in Adaline weight-updating process are assumed to be constant, while in ALOF the frequency and phase angle are recursively updated by a loop filter.

This approach is highly adaptive and is able to follow non-stationary signals. There is not a theoretical restriction in the harmonic components that can be evaluated, except for the complexity of the neural network, that will increase when the number of harmonics increases. The computational loading increases rapidly together with the increment of expected harmonics. This problem also affects DFT, KF and WLSE but, generally, only the fundamental components need to be identified. If harmonic components are to be identified, parallel processing could be used to reduce the computational burden.

5.1. Basic concept of the ANN [237, 238, 160]

Let the discrete version of a single-phase signal be

$$\begin{aligned} y(k) &= \sum_{m=1}^{N} A_m \, sin\,(m\theta_k + \phi_m) + \in (k) \\ &= \sum_{m=1}^{N} [A_{md}\, cos\phi_m]\, sin\,(m\theta_k) + \sum_{m=1}^{N} [A_{mq}\, sin\phi_m]\, cos\,(m\theta_k) + \in (k) \end{aligned} \tag{C.21}$$

where $\theta_k = 2\pi k/N_s$ and $N_s = F_s/F_0$ is the sample rate given by the quotient of the sampling frequency (F_s) and the fundamental frequency (F_0).

The Adaline consists of calculating the weighting vector that will make the error between the real and the estimated signal zero, as shown in Fig.C.4.

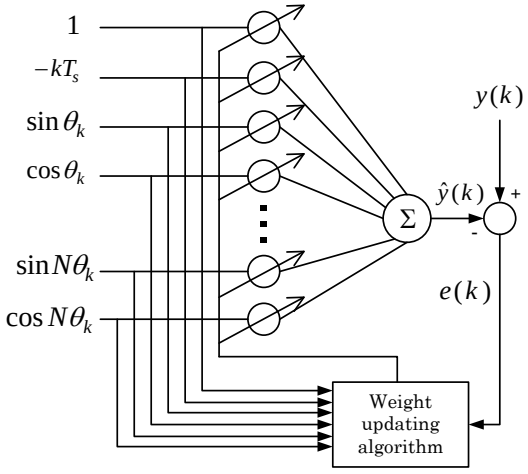


Figure C.4: Block diagram of harmonic estimation using Adaline where $\theta = 2\pi k/N_s$

The input vector $X(k)$ has the following form

$$X(k) = \begin{bmatrix} sin\theta_k & cos\theta_k & sin(2\theta_k) & cos(2\theta_k) & \dots & sin(N\theta_k) & cos(N\theta_k) & 1 & -kT_s \end{bmatrix} \tag{C.22}$$

where the two last elements correspond to the decaying DC component of the signal.

The weight-vector is of the form

$$W(k) = \begin{bmatrix} W_1(k) & W_2(k) & W_3(k) & W_4(k) & W_3(2N-1) & W_4(2N) \end{bmatrix} \tag{C.23}$$

The objective is to obtain the values of the coefficients of the $W(k)$ vector. This is done by means of an updating rule. There are different updating rules; one example is provided by the Widrow-Hoff delta rule [237]:

$$W(k+1) = W(k) + \frac{\alpha\, e(k) X(k)}{X(k)^T X(k)} \tag{C.24}$$

where k is the index of iteration and α is the learning parameter.

When the tracking error converges to zero ($e(t) = 0$), the weight-vector yields the Fourier coefficients

$$W_0 = \begin{bmatrix} A_1\, cos\phi_1 & A_1\, sin\phi_1 & \dots & A_N\, cos\phi_N & A_N\, sin\phi_N & A_{dc} \end{bmatrix} \tag{C.25}$$

Appart from the Widrow-Hoff delta rule, there are also other adaptation algorithms that produce a fast convergence [237].

6. Basic concept of a single-phase PLL [133, 136]

A PLL is composed of a phase-detector (PD), a loop filter (LF) and a voltage controlled oscillator (VCO), as it is illustrated in the block diagram of Fig.C.5.

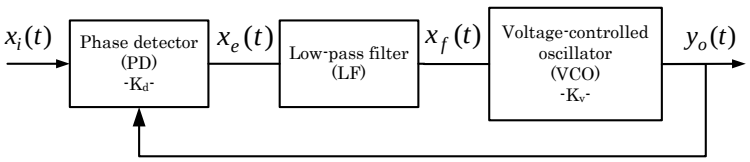


Figure C.5: Block diagram of a PLL.

In order to understand the working principle of the PLL, the input and output signals are defined

$$x_i(t) = A\, cos(\omega_i + \theta_i) \tag{C.26}$$

$$y_o(t) = B\, cos(\omega_o t + \varphi_o) \tag{C.27}$$

where ω_i and ω_o are the angular frequencies of the input and output signal, and θ_i and ϕ_o the initial phase constants. The initial time constants depend on the selected time origin.

In the beginning, the PLL is unlocked, which means that $\omega_i \neq \omega_o$ and the signals are out of synchronism. The PD, which is a signal multiplier, yields

$$x_e(t) = K_d\, \{cos[(\omega_i - \omega_o)t + \theta_i - \varphi_o] + cos[(\omega_i + \omega_o)t + \theta_i - \varphi_o]\} \tag{C.28}$$

From (C.28) it can be observed that the output of the PD contains a lower frequency and a higher frequency term. The LF, which is often a PI, is in charge of filtering the higher-order terms $(\omega_i + \omega_o)$. The filtering stage supplies the following expression to the VCO

$$x_f(t) = K_d \, cos[(\omega_i - \omega_o)t + \theta_i - \phi_o] \tag{C.29}$$

After a long transient time, the output becomes synchronous to the input. This means that the frequencies are the same $(\omega_i = \omega_o)$, but the phase angle can be different $(\varphi_o \neq \phi_o)$.

$$y_o(t) = B \, cos(\omega_i t + \phi_o) \tag{C.30}$$

Comparing (C.27) with (C.30)

$$\varphi_o(t) = (\omega_i - \omega_o)t + \phi_o \tag{C.31}$$

and the LF output becomes a constant signal

$$x_f(t) = K_d \, cos(\theta_i - \phi_o) \tag{C.32}$$

The VCO is a frequency modulated oscillator, whose instantaneous angular frequency (w_{inst}) is a linear function of the controlled signal $(x_f(t))$, around the central angular frequency (w_o)

$$\omega_{inst} = \frac{d}{dt}(\omega_o t + \varphi_o) = \omega_o + K_v \, x_f(t) \tag{C.33}$$

where K_v is the VCO sensitivity. From (C.31) and (C.32) the following relationship is obtained

$$\omega_i - \omega_o = K_d K_v \, cos(\theta_i - \phi_o) \tag{C.34}$$

giving

$$\phi_o = \theta_i - \arccos\left(\frac{\omega_i - \omega_o}{K_d K_v}\right) \tag{C.35}$$

Then, substituting (C.35) into (C.32)

$$x_f = \frac{\omega_i - \omega_o}{K_v} \tag{C.36}$$

The above equation clearly shows that it is the DC signal x_f that changes the VCO frequency

$$\omega_{inst} = \omega_o + K_v x_f = \omega_i \tag{C.37}$$

If $\omega_i - \omega_o << K_d K_v$ and the PLL is locked, then , from (C.35), it is possible to say that

$$\theta_o = \phi_o + \frac{\pi}{2} \tag{C.38}$$

And thus,

$$x_f = K_d \, sin(\theta_i - \theta_o) \tag{C.39}$$

The difference $\theta_i - \theta_o$ is the phase error between the two signals, which is null when the initial frequency

offset is zero. When the difference $\theta_i - \theta_o$ is sufficiently small, the following approximation is used

$$x_f \approx= K_d\,(\theta_i - \theta_o) \tag{C.40}$$

The product $K = K_d K_v$ is called loop gain.

7. Enhanced-PLL [239, 164, 240]

The output of the PD of a conventional PLL, where the input signal is defined as $u(t) = V_i\,sin\phi_i$ and the output signal is $y(t) = V_o\,cos\phi_o$, is given by the expression:

$$u(t)y(t) = \frac{1}{2}V_i V_o\,sin(\phi_i - \phi) + \frac{1}{2}V_i V_o\,sin(\phi_i + \phi_o) \tag{C.41}$$

Equation (C.41) shows that:

- The PD output contains a low-frequency and a high-frequency term.
- The low-frequency term is a nonlinear function of the difference of the input and the output phases.
- The magnitude of the PD output depends on the magnitude of the input signal.

The LF term in Fig.C.5 mitigates the high-frequency term but it does not always totally eliminate it. The EPLL, proposed by [239, 164, 240] proposes a new PD scheme that is able to remove the double frequency-ripple and to provide an error-free estimate of the phase-angle and the frequency when the signal is not highly distorted.

Assuming that the input signal is $u(t) = V_i\,sin\phi_i$ and the output signal is $y(t) = V_o\,cos\phi_o$, [239, 164] propose a detection method such that

$$e(t)\,cos\phi = \frac{1}{2}V_i\,sin(\phi_i - \phi) + \frac{1}{2}\left[V_i\,sin(\phi_i + \phi) - V\,sin(2\phi)\right] \tag{C.42}$$

When the output phase becomes equal to the input phase ($\phi = \phi_i$) and the output voltage magnitude becomes equal to the input voltage magnitude ($V = V_i$), the high-frequency term disappears completely and just the low-frequency term remains. The block diagram of the EPLL structure is presented in Fig.C.6(a).

When the input signal is highly distorted, it is possible to employ several EPLL units in parallel. Each of the units takes care of one harmonic. If all the harmonics present in the input signal are modelled, the proposed parallel EPLL supplies an absolutely error-free estimate.

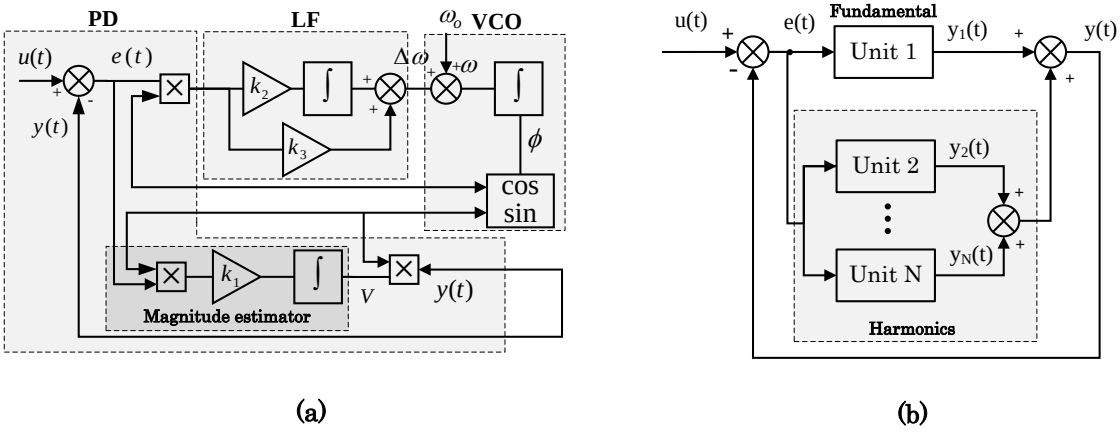


Figure C.6: (a) Block diagram of a unit EPLL, and (b) Several EPLL units in parallel

Appendix D

MV benchmark

In order to test and study the UPLC in a representative distribution network, distribution network benchmarks have been searched in the litterature. However, only one benchmark, proposed by CIGRE Study Committee C6 (CIGRE Task Force C6.04.02), has been found. Appendix D provides information and data on this benchmark and describes the changes that have been applied to this benchmark in this PhD in order to reduce the number of nodes. This appendix also presents some screenshots taken in the power-system simulation software POWERWORLD in different situations described in Chapter 3..

1. MV distribution network benchmark proposed by CIGRE Study Commitee C6 [88]

Within CIGRE Study Committee C6, CIGRE Task Force C6.04.02 proposes three benchmark networks to study the integration of DG following a standardized methodology: a low-voltage urban distribution, a medium-voltage rural distribution, and a high-voltage transmission network.

Some of the simulations performed in this PhD manuscript are based on the MV rural distribution network proposed by CIGRE. As depicted in Fig.D.1, the proposed MV network is divided into two subnetworks but, depending on the case study, the second network can be omitted. A MVDC coupler is also suggested between nodes 8 and 14 in the case that an interconnection is desired. The *T-shaped* symbols stand for normally opened switches that enable either radial or looped operations. The original network is a rural german 20 kV network.

Except for lines 1-2 and 12-13, that are overhead lines, the interconnections are made by cables and, the total length of the lines is around 15 km. In the next lines the furnished data is provided.

2. Modified MV distribution network benchmark

In the simulations presented in this PhD manuscript a modified version of the benchmark proposed by CIGRE is used. The only difference is that the number of nodes has been reduced because so many buses were not needed. On the other hand, since the number of buses is reduced, loads have also been grouped (summing them up) accordingly . It is considered that the location of the distribution-grid coupling may change as well (Fig.D.3).

3. Some simulation cases

The following figures represent some of the simulation cases discussed in section II.3.3.. These simulations have been performed in the PowerWorld simulation sofware.

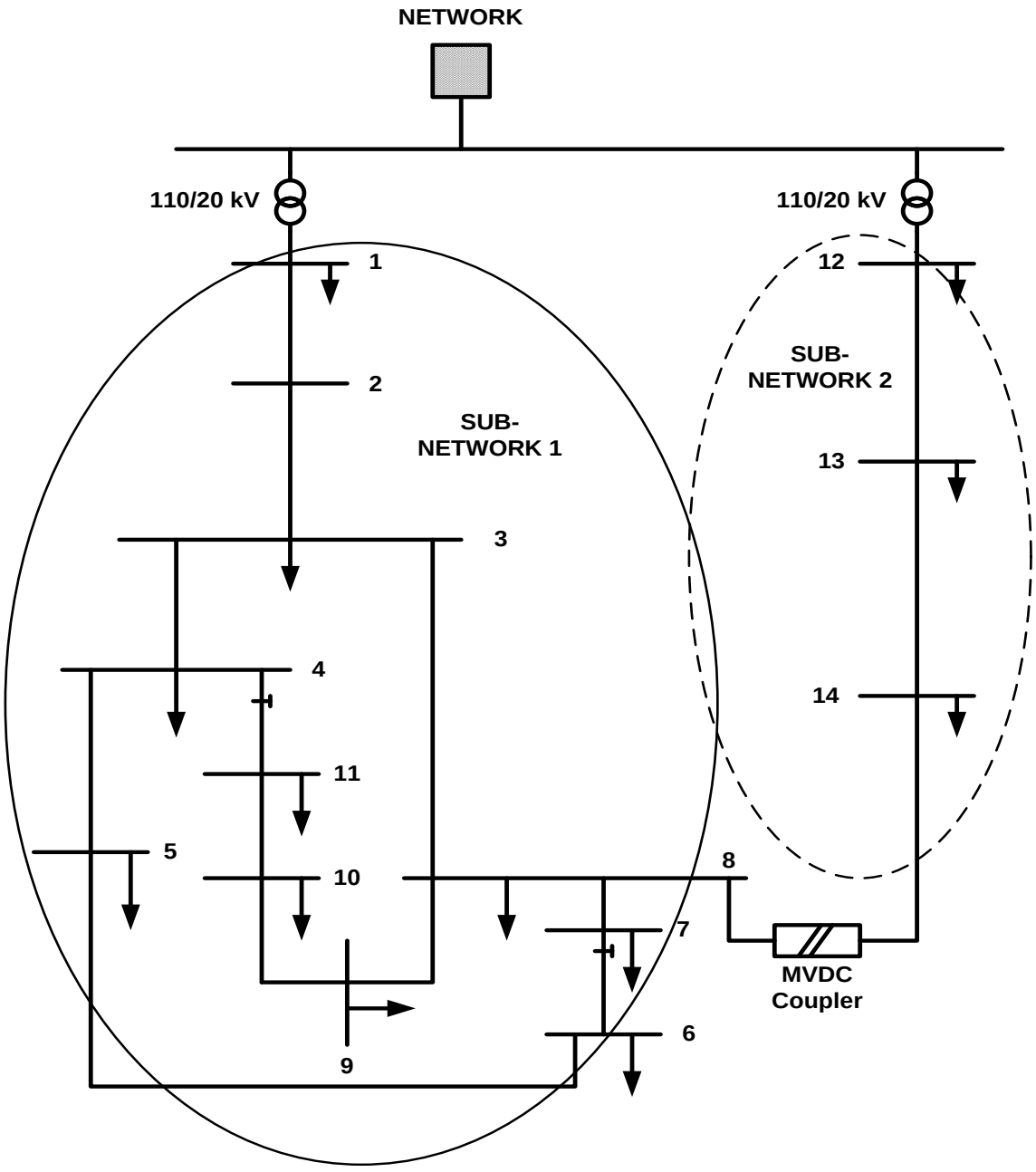


Figure D.1: MV distribution network benchmark proposed by [88]

Node 1	Node 2	Ohmic resistance	Inductive resistance	Parallel capacitance	Line length
---	---	[Ohm/km]	[Ohm/km]	[nF/km]	[km]
1	2	0.579	0.367	9.93	2.82
2	3	0.164	0.113	413	4.42
3	4	0.262	0.121	405	0.606
4	5	0.354	0.129	285	0.56
5	6	0.336	0.126	343	1.54
7	8	0.294	0.123	350	1.667
8	9	0.339	0.13	273	0.320
9	10	0.399	0.133	302	0.77
10	11	0.367	0.133	285	0.328
3	8	0.172	0.115	411	1.3
12	13	0.337	0.358	10.18	4.89
13	14	0.202	0.122	299	2.995
6	*7*	*0.256*	*0.13*	*235*	*0.236*
11	*4*	*0.423*	*0.134*	*310*	*0.487*

(a) Line and cable values

Node No.	Load Type	P_{max}	Q_{max}
		[p.u.]	[p.u.]
1	Household	0.15000	0.03100
1	Industry	0.05000	0.01000
3	Household	0.00276	0.00069
3	Industry	0.00224	0.00139
4	Household	0.00432	0.00108
5	Household	0.00725	0.00182
6	Household	0.00550	0.00138
7	Industry	0.00077	0.00048
8	Household	0.00588	0.00147
9	Industry	0.00574	0.00356
10	Industry	0.00068	0.00042
10	Household	0.00477	0.00120
11	Household	0.00331	0.00083
12	Household	0.15000	0.03000
12	Industry	0.05000	0.01700
13	Industry	0.00032	0.00020
14	Industry	0.00330	0.00205
14	Household	0.00207	0.00052

(b) Load types and pu values

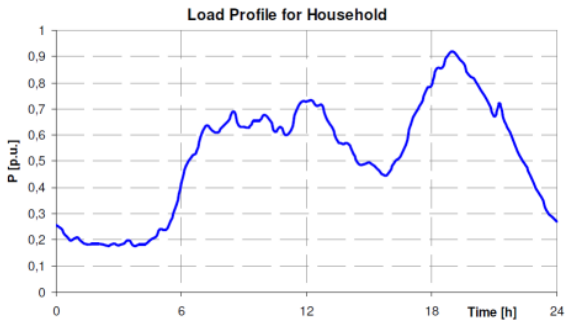
Node 1	Node 2	Max. thermal current
---	---	[A]
1	2	140
2	3	140
3	4	120
4	5	50
5	6	50
7	8	50
8	9	50
9	10	50
10	11	50
3	8	120
6	7	50
11	4	50

(c) Thermal ratings of lines

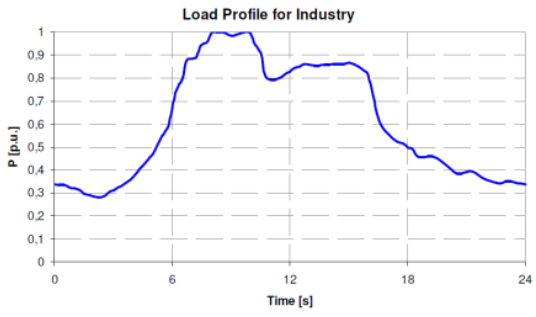
Continent	No. of Phases	S_{base}	U_{base}	I_{base}	Z_{base}	l_{base}
		[MVA]	[kV]	[kA]	[Ohm]	[km]
EUROPE	3	100	20	2.89	4	1

S_{base} – base apparent power,
U_{base} – base voltage,
I_{base} – base current,
Z_{base} – base impedance,
l_{base} – base line length

(d) Base values

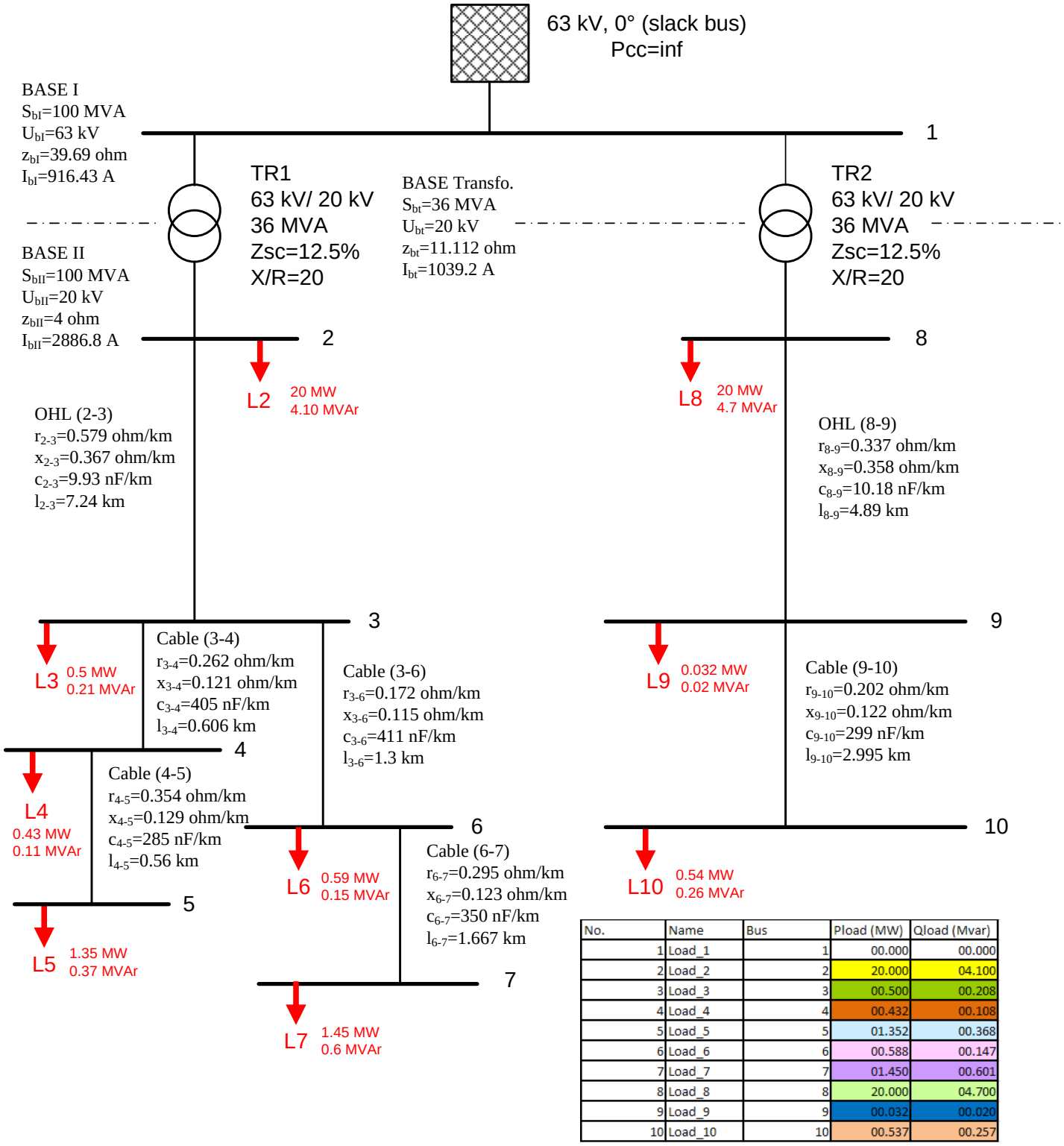


(e) Household load profile



(f) Industry load profile

Figure D.2: MV distribution network benchmark data [88, 89]



No.	Name	Bus	Pload (MW)	Qload (Mvar)
1	Load_1	1	00.000	00.000
2	Load_2	2	20.000	04.100
3	Load_3	3	00.500	00.208
4	Load_4	4	00.432	00.108
5	Load_5	5	01.352	00.368
6	Load_6	6	00.588	00.147
7	Load_7	7	01.450	00.601
8	Load_8	8	20.000	04.700
9	Load_9	9	00.032	00.020
10	Load_10	10	00.537	00.257

Figure D.3: Modified benchmark used in the simulations

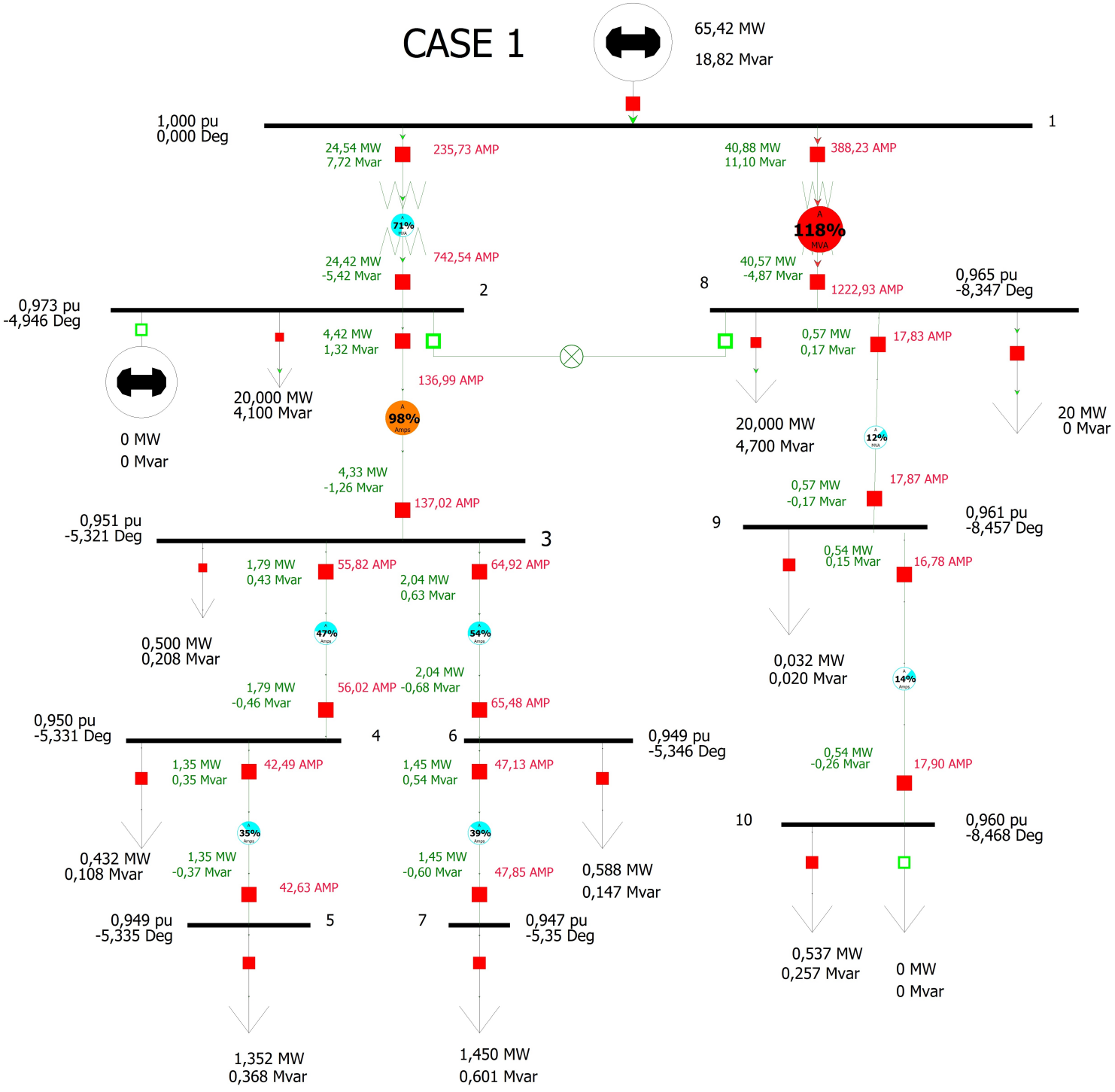


Figure D.4: Benchmark example: case 1 (the red-filled squares denote *closed* circuit-breakers while green-empty squares denote *opened* circuit-breakers)

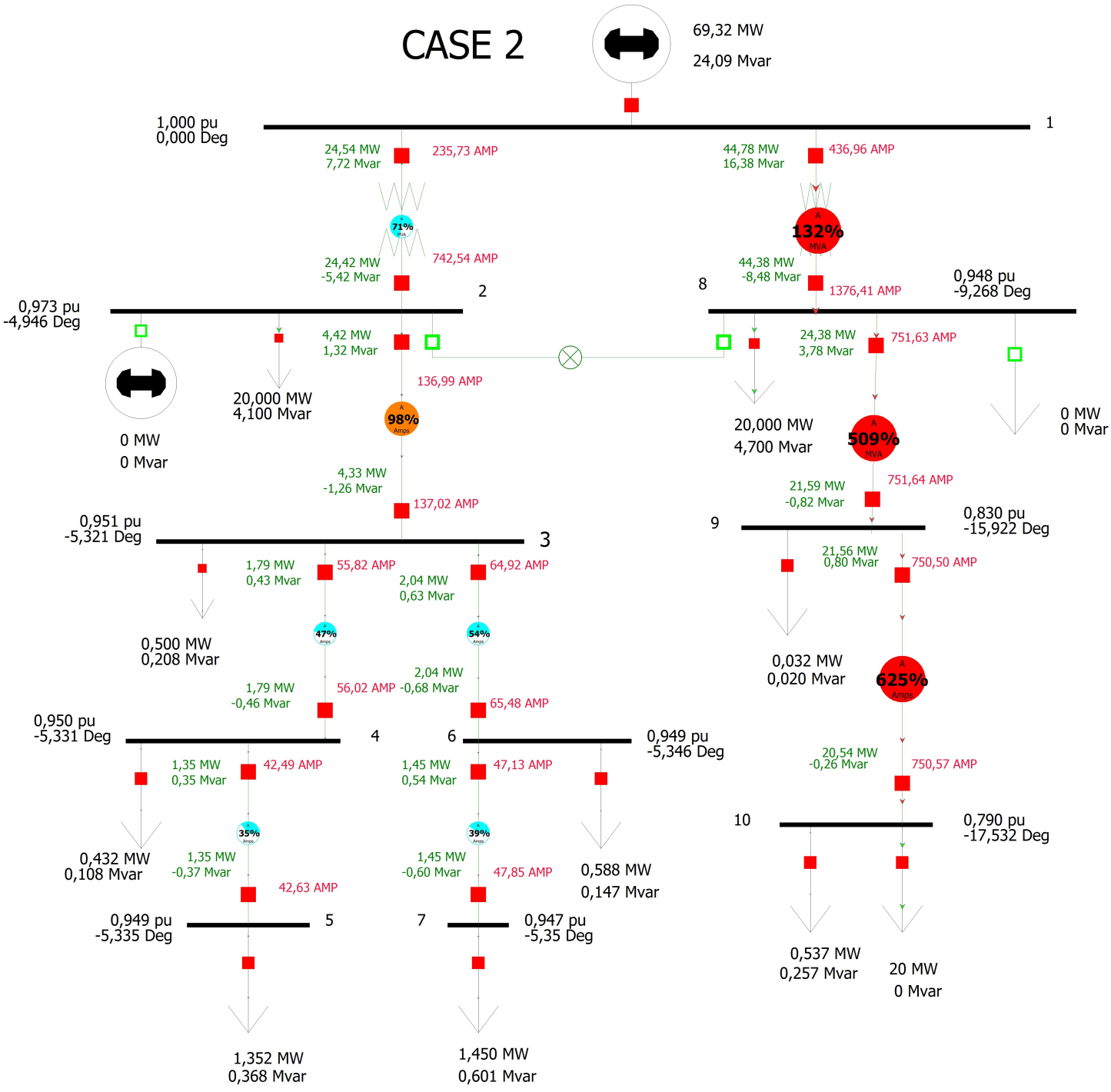


Figure D.5: Benchmark example: case 2 (the red-filled squares denote *closed* circuit-breakers while green-empty squares denote *opened* circuit-breakers)

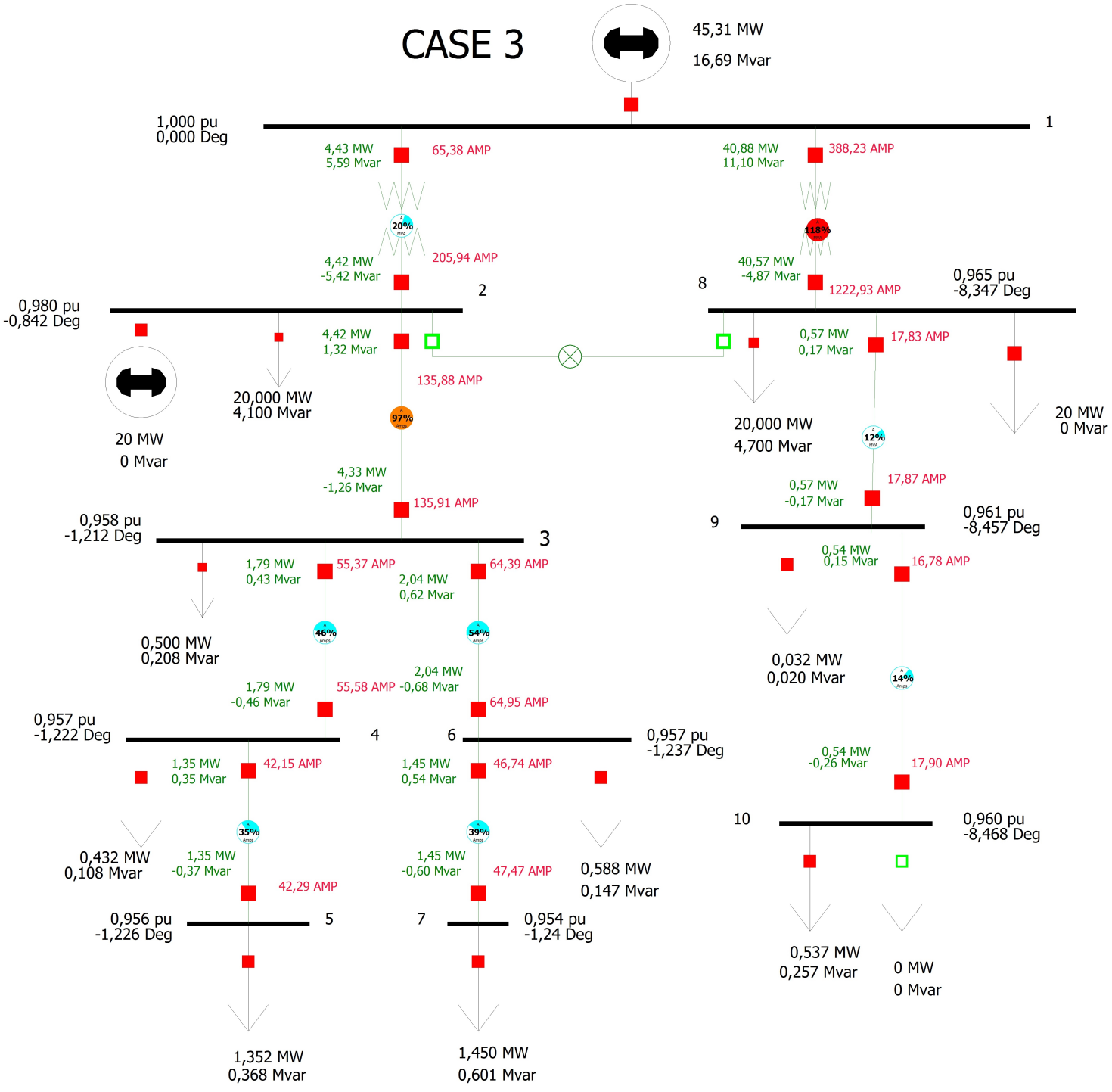


Figure D.6: Benchmark example: case 3 (the red-filled squares denote *closed* circuit-breakers while green-empty squares denote *opened* circuit-breakers)

Appendix E

Modelling and design specifications

Appendix E describes different procedures that have been followed during the modeling and design stages of the UPLC and provides diverse values obtained from these calculations.

1. Per-unit conversion

Due to the existence of several transformers and a DC-link, it is advisable to convert the full values into per-unit values. As illustrated in Fig.E.1 the system can be divided into four zones: ZONE I (MV side), ZONE II (shunt-side), ZONE III (series-side), and ZONE DC (DC-side). Fig.E.1 shows a figure delimiting the zones and giving the corresponding base-values for each zone. In the analyzed case, zones I and III are the same because the turns-ratio of the series transformer is one. Observe that selected voltage base-values are peak values (that is why a term (1/2) appears in the apparent power expression), and that base power is chosen to be the power per phase.

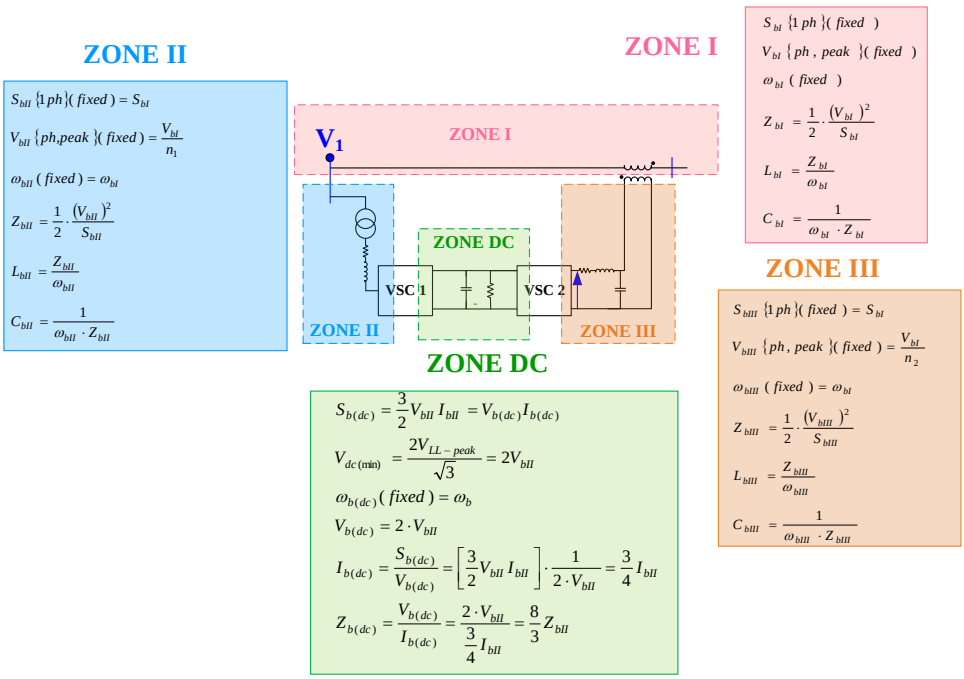


Figure E.1: Per-unit conversion bases

Per-unit values are obtained dividing each full-value by its base-value,

$$i = \frac{I}{I_b} \qquad v = \frac{V}{V_b} \qquad r = \frac{R}{Z_b} \qquad l = \frac{L}{L_b} \qquad c = \frac{C}{C_b} \tag{E.1}$$

where values in upper-case are full-values and values in lower-case are per-unit values.

An example on how to translate the full values to per-unit values is given next. In this example, bold symbols stand for vectors described as $\mathbf{X}^{(dq)} = X_d + jX_q$. The example is based on two arbitrary expressions in full-values and in dq coordinates:

$$\mathbf{V_1}^{(dq)} - \mathbf{E_1}^{(dq)} = R_1\mathbf{I_1}^{(dq)} + L_1\frac{d\mathbf{I_1}^{(dq)}}{dt} + jL_1\omega\ \mathbf{I_1}^{(dq)} \tag{E.2}$$

$$\mathbf{I_L}^{(dq)} = C_L\frac{d\mathbf{V_r}^{(dq)}}{dt} + j\omega\ C_L\mathbf{V_r}^{(dq)} + \mathbf{I_r}^{(dq)} \tag{E.3}$$

All the terms are divided by the voltage base considering that

$$Z_b = \omega_b L_b = \frac{1}{\omega_b C_b} \qquad V_b = Z_b I_b = \omega_b L_b I_b \qquad I_b = \frac{V_b}{Z_b} = \omega_b C_b V_b \tag{E.4}$$

$$\frac{\mathbf{V_1}^{(dq)}}{V_b} - \frac{\mathbf{E_1}^{(dq)}}{V_b} = \frac{R_1}{Z_b}\frac{\mathbf{I_1}^{(dq)}}{I_b} + \frac{1}{\omega_b}\frac{L_1}{L_b I_b}\frac{d\mathbf{I_1}^{(dq)}}{dt} + j\frac{L_1}{L_b}\frac{\omega}{\omega_b}\ \frac{\mathbf{I_1}^{(dq)}}{I_b} \tag{E.5}$$

$$\frac{\mathbf{I_L}^{(dq)}}{I_b} = \frac{1}{\omega_b}\frac{C_L}{C_b V_b}\frac{d\mathbf{V_r}^{(dq)}}{dt} + j\frac{\omega}{\omega_b}\ \frac{C_L}{C_b}\frac{\mathbf{V_r}^{(dq)}}{V_b} + \frac{\mathbf{I_r}^{(dq)}}{I_b} \tag{E.6}$$

After these divisions, per-unit equivalent expressions are deduced,

$$\mathbf{v_1}^{(dq)} - \mathbf{e_1}^{(dq)} = r_1\mathbf{i_1}^{(dq)} + \frac{l_1}{\omega_b}\frac{d\mathbf{i_r}^{(dq)}}{dt} + j\frac{l_1}{\omega_b}\omega\ \mathbf{i_1}^{(dq)} \tag{E.7}$$

$$\mathbf{i_L}^{(dq)} = \frac{1}{\omega_b}c_L\frac{d\mathbf{v_r}^{(dq)}}{dt} + j\frac{c_L}{\omega_b}\omega\mathbf{v_r}^{(dq)} + \mathbf{i_r}^{(dq)} \tag{E.8}$$

However, in (E.7) and (E.8) it is observed that l and c appear divided by ω_b. In order to "mask" this term so the resulting expression looks similar to the original expression, it is possible to define two new variables, l' and c' as,

$$l' = \frac{l}{\omega_b} \qquad c' = \frac{c}{\omega_b} \tag{E.9}$$

Finally, two expressions that are very similar to the original expressions (E.2) and (E.3) are obtained:

$$\mathbf{v_1}^{(dq)} - \mathbf{e_1}^{(dq)} = r_1\mathbf{i_1}^{(dq)} + l'_1\frac{d\mathbf{i_r}^{(dq)}}{dt} + jl'_1\omega\ \mathbf{i_1}^{(dq)} \tag{E.10}$$

$$\mathbf{i_L}^{(dq)} = c'_L\frac{d\mathbf{v_r}^{(dq)}}{dt} + j\omega\ c'_L\mathbf{v_r}^{(dq)} + \mathbf{i_r}^{(dq)} \tag{E.11}$$

In this expressions the term ω_b is implicit and the full-value of ω is available. Instead of defining l' and c' it is also possible to use the per-unit value of time (where the time base value is $t_b = 1/w_b$), which obviates the term w_b from the expression [241].

2. Base-values of the test-case

The base-values used in the simulations are defined in Tables E.1 and E.2.

BASE I=BASE III	BASE II
• $S_{bI}[1\ ph] = 12MVA$	• $S_{bII}[1\ ph] = S_{bI}[1\ ph] = 12\ MVA$
• $V_{bI}[ph-gnd,\ peak] = 16.33\ kV$	• $V_{bII}[ph-gnd,\ peak] = \frac{V_{bI}}{33} = 494.85\ V$
• $Z_{bI} = \frac{1}{2} \cdot \frac{V_{bI}^2}{S_{bI}} = 11.\hat{1}\ \Omega$	• $Z_{bII} = \frac{1}{2} \cdot \frac{V_{bII}^2}{S_{bII}} = 0.01020\ \Omega$
• $\omega_b = 2\pi f_b = 2\pi 50 = 314.1593\ rad/s$	
• $I_{bI} = \frac{2 \cdot S_{bI}}{V_{bI}} = 1469.7\ A$	• $I_{bII} = \frac{V_{bII}}{Z_{bIII}} = 48.5\ kA$
• $L_{bI} = \frac{Z_{bI}}{\omega_b} = 0.03537\ H$	• $L_{bII} = \frac{Z_{bII}}{\omega_b} = 32.47 \cdot 10^{-6}\ H$
• $C_{bI} = \frac{1}{\omega_b Z_{bI}} = 2.8647 \cdot 10^{-4}\ F$	• $C_{bII} = \frac{1}{\omega_b Z_{bII}} = 0.3120\ F$

Table E.1: Base I, II and III values

BASE DC
• $S_{b-dc} = \frac{3}{2} V_{bII} I_{bII}[3\ ph] = 3 \cdot S_{bI} = V_{b-dc} I_{b-dc} = 36\ MVA$
• $U_{b-dc} = 2000\ V$
• $I_{b-dc} = \frac{S_{b-dc}}{U_{b-dc}} = 18\ kA$
• $Z_{b-dc} = \frac{U_{b-dc}}{I_{b-dc}} = 0.\hat{1}\ \Omega$
• $L_{b-dc} = \frac{Z_{bII}}{\omega_b} = 3.5367 \cdot 10^{-4}\ H$
• $C_{b-dc} = \frac{1}{\omega_b Z_{b-dc}} = 28.64 \cdot 10^{-3}\ F$

Table E.2: Base DC values

3. Matrix Definitions

$$\text{Concordia Transform} \qquad C_o = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & \text{-0.5} & \text{-0.5} \\ 0 & \text{-}\sqrt{3}/2 & \sqrt{3}/2 \\ 1/\sqrt{2} & 1/\sqrt{2} & 1/\sqrt{2} \end{bmatrix} \tag{E.12}$$

$$\text{Clarke Transform} \qquad C_L = \frac{2}{3} \begin{bmatrix} 1 & \text{-0.5} & \text{-0.5} \\ 0 & \text{-}\sqrt{3}/2 & \sqrt{3}/2 \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{E.13}$$

$$\mathbf{A_{RL(\alpha\beta)}} = \left[(r_{se}/l'_{se}) \quad +0\ ;0 \quad (r_{se}/l'_{se})\right]$$

$$\mathbf{A_{RL}(dq+)} = \left[(r_{se}/l'_{se}) \quad +\omega\ ;-\omega \quad (r_{se}/l'_{se})\right] \qquad \mathbf{A_{RL}(dq-)} = \left[(r_{se}/l'_{se}) \quad -\omega\ ;+\omega \quad (r_{se}/l'_{se})\right]$$

$$\mathbf{A_{L}(dq+)} = \left[(r_{L}/l'_{L}) \quad +\omega\ ;-\omega \quad (r_{L}/l'_{L})\right] \qquad \mathbf{A_{L}(dq-)} = \left[(r_{L}/l'_{L}) \quad -\omega\ ;+\omega \quad (r_{L}/l'_{L})\right]$$

$$\mathbf{A_{t2}(dq+)} = \left[(r_{t2}/l'_{t2}) \quad +\omega\ ;-\omega \quad (r_{t2}/l'_{t2})\right] \qquad \mathbf{A_{t2}(dq-)} = \left[(r_{t2}/l'_{t2}) \quad -\omega\ ;+\omega \quad (r_{t2}/l'_{t2})\right]$$

$$\mathbf{A_{f2}(dq+)} = \left[(r_{f2}/l'_{f2}) \quad +\omega\ ;-\omega \quad (r_{f2}/l'_{f2})\right] \qquad \mathbf{A_{f2}(dq-)} = \left[(r_{f2}/l'_{f2}) \quad -\omega\ ;+\omega \quad (r_{f2}/l'_{f2})\right]$$

$$\mathbf{A_{1}(dq+)} = \left[(r_{1}/l'_{1}) \quad +\omega\ ;-\omega \quad (r_{1}/l'_{1})\right] \qquad \mathbf{A_{1}(dq-)} = \left[(r_{1}/l'_{1}) \quad -\omega\ ;+\omega \quad (r_{1}/l'_{1})\right]$$

$$\mathbf{Y_m(dq+)} = \left[0 \quad +\omega c'_m\ ;-\omega c'_m \quad 0\right] \qquad \mathbf{Y_m(dq-)} = \left[0 \quad -\omega c'_m\ ;+\omega c'_m \quad 0\right]$$

$$\mathbf{A_\omega(dq+)} = [0 \quad +\omega\ ;-\omega \quad 0] \qquad \mathbf{A_\omega(dq-)} = [0 \quad -\omega\ ;+\omega \quad 0]$$

$$\mathbf{B_{RL}} = \left[(1/l'_{se}) \quad 0\ ;0 \quad (1/l'_{se})\right] \qquad \mathbf{B_{L}} = \left[(1/l'_{L}) \quad 0\ ;0 \quad (1/l'_{L})\right]$$

$$\mathbf{B_{f2}} = [(1/l'_{f2}) \quad 0\ ;0 \quad (1/l'_{f2})] \qquad \mathbf{B_{t2}} = [(1/l'_{t2}) \quad 0\ ;0 \quad (1/l'_{t2})]$$

$$\mathbf{D_{L}} = \left[(1/c'_{L}) \quad 0\ ;0 \quad (1/c'_{L})\right] \qquad \mathbf{D_{m}} = \left[(1/c'_{m}) \quad 0\ ;0 \quad (1/c'_{m})\right]$$

$$\mathbf{D_{f2}} = \left[(1/c'_{f2}) \quad 0\ ;0 \quad (1/c'_{f2})\right] \qquad \mathbf{B_{1}} = \left[(1/l'_{1}) \quad 0\ ;0 \quad (1/l'_{1})\right]$$

where $r_{se} = r_{t2} + r_L$, $l'_{se} = l'_{t2} + l'_L$, and $c'_m = c'_L/2$.

4. Calculation procedure of series transformer impedances.

Once the nominal apparent power of the series transformer is known (i.e. $S_{base-tr2}\ (1ph) = 171.6\ kVA$), the impedances of the transformer are calculated. For these calculations it is assumed that the leakage impedance of the transformer is 0.1 pu of the transformer base impedance. Thus, the first step is to calculate the transformer base impedance:

$$S_{base-tr2}\ (1ph) = 171.6\ kVA \text{ , and} \qquad \hat{V}_{base-tr2}\ (1ph) = 1000\ V$$

$$Z_{base-tr2} = \frac{\hat{V}^2_{base-tr2}}{2 \cdot S_{base-tr2}} = 2.914\ \Omega \tag{E.14}$$

where the apparent power is a per-phase value and the voltage at the primary is the peak voltage. And, once the transformer base-impedance is known, the full transformer leakage impedance value is calculated:

$$Z_{tr2} = 0.1 \cdot Z_{base-tr2} = 0.2914\ \Omega \tag{E.15}$$

Then, assuming that $x/r = 20$:

$$R_{tr2} = \frac{1}{\sqrt{1+(x/r)^2}} \cdot Z_{tr2} = 0.0146\ \Omega \tag{E.16}$$

$$X_{tr2} = (x/r) \cdot R_{tr2} = 0.2910\ \Omega \tag{E.17}$$

where these values are the total (primary+secondary) transformer impedance values refered to the primary, as illustrated in Fig.III.1.12:

$$R_{tr2} = R_{tr2(p)} + R'_{tr2(s)} = R_{tr2(p)} + {n_{t2}}^2 \cdot R_{tr2(s)} \tag{E.18}$$

$$X_{tr2} = X_{tr2(p)} + X'_{tr2(s)} = R_{tr2(p)} + {n_{t2}}^2 \cdot X_{tr2(s)} \tag{E.19}$$

and where, $R_{tr2(p)} = R'_{tr2(s)}$ and $X_{tr2(p)} = X'_{tr2(s)}$.

The magnetizing reactance is 100-1000 times the leakage reactance [242]. In this case, the highest magnetizing reactance value is chosen in order to minimize the magnetizing current. For the core losses, the same value is selected.

$$X_m = 1000 \cdot X_{tr2} = 1000 \cdot 0.2910 = 291\ \Omega \tag{E.20}$$

$$R_c = X_m = 291\ \Omega \tag{E.21}$$

5. Series LC filter calculation procedure

The following steps have been followed to calculate the values of the seris filter:

1. **To choose an exchanged reactive power limit.**

   10% of the inverter nominal power is reasonable exchanged power. If a better filtering performance is wanted, this value can be highered, but a the cost of a higher capacitor and inverter. From a preceding simulations it is known that the series compensator (and hence, the series VSC) has a nominal power of $S_c = S_{se-inv} = 171.6\ kVA$. According to these values the exchanged reactive power is assumed to be $Q_{exchanged} = 17.16 kVA$.

2. **To choose the filter cutting-frequency.**

   A cutting frequency of a tenth of the inverter switching frequency is a typical value: $f_c = 495\ Hz$.

3. **To calculate k as the ratio between ω_1 (the fundamental frequency) and and the cutting frequency ω_c.**

   In this case $k = 0.1010$.

4. **To estimate the fundamental voltage at the inverter terminals.**

   Neglecting the voltage drop at the transformer and the filter, it is possible to approximate the value of the voltage at the inverter output terminals: $\hat{E}(\omega_1) \approx 1000\ V$.

5. **From equation** (III.1.8)**, to calculate** C_{max}**.**

   According to equation (III.1.8), $C = 108\ \mu F$.

6. **From equation** (III.1.6) **to calculate** L**.**

   Then, from equation (III.1.6), $L = 956\ \mu H$.

The filter calculation has been performed assuming that no resistive elements exist. However, the inductance of the filter always presents an inherent resistance. As it can be observed in the bode plots of the series filter (Fig.E.2), a higher resistance damps the reasonance peak of the filter, but it has a negative influence on the immunity of this filter to perturbations, specially around the resonance frequency. The bode plots show the relationships between the input voltage of the filter $E(s)$ and the line current $I_{2(sec)}(s)$ on the output voltage of the filter $V_f(s)$:

$$\begin{aligned} V_f(s) &= G_1(s) \cdot E(s) - G_2(s) \cdot I_{2(sec)}(s) = \\ &= \frac{1}{LCs^2 + RCs + 1} \cdot E(s) - \frac{Ls + R}{LCs^2 + RCs + 1} \cdot I_{2(sec)}(s) \end{aligned} \tag{E.22}$$

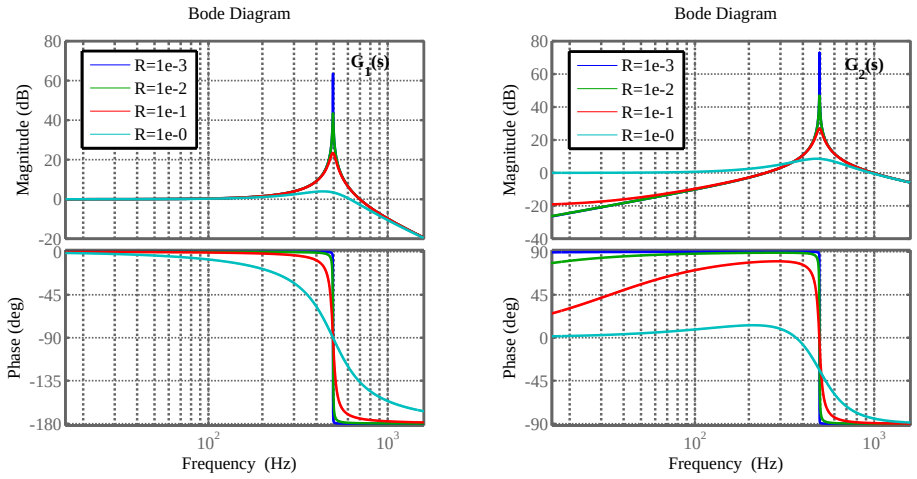


Figure E.2: Series filter bode plots (a) $G_1(s)$, and (b) $G_2(s)$

In this case, the resistance of the inductance is assumed to be $R_f = 0.001\ \Omega$. This low value has been selected because, if the resistance is lower, the voltage drop in the inductance is lower, at the cost of a sharper resonance peak. As it will be observed in the next section, the chosen value will have an influence on harmonics $h9$, $h11$ and $h13$ when a very low modulation index is used.

In any case,the resistance is not a design value because it is given by the constructive characteristics of the inductance. However, it is possible to modify the equivalent value of the resistance artificially by adding a resistor in series or parallel with the filter.

6. Shunt transformer and filter impedance calculation procedure.

When the the total magnitude of the impedance is known (i.e. $Z_1 = 1.5\ \Omega$), the only thing left to do is to decide how much of this impedance corresponds to the transformer, and how much corresponds to the filter. The procedure is as follows

6.1. To define the transformer impedance.

The transformer impedance is calculated as 10% of the transformer base impedance. And, the transformer base impedance is calculated based on the maximum apparent power at the shunt connection point (Fig.E.3):

$$S_{base-tr1}\ (1ph) = 250\ kVA\ \text{, and} \quad \hat{V}_{base-tr1}\ (1ph) = 500\ V$$
$$Z_{base-tr1} = \frac{(\hat{V}_{base-tr1})^2}{2 \cdot S_{base-tr1}} = 0.4897\ \Omega \tag{E.23}$$

where the apparent power is a per-phase value and the voltage at the primary is the peak voltage. When the transformer base-impedance is known, the full transformer leakage impedance value is calculated:

$$Z_{tr1} = 0.1 \cdot Z_{base-tr1} = 0.0489\ \Omega \tag{E.24}$$

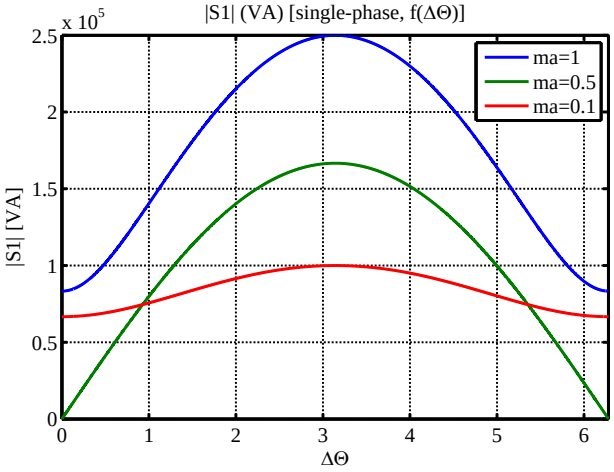


Figure E.3: Apparent powers at the connection point of the shunt-branch.

Odd Harmonics				Harmonic Pairs	
Not multiples of 3		Multiples of 3			
Order h	Relative Voltage (U_n)	Order h	Relative Voltage (U_n)	Order h	Relative Voltage (U_n)
5	6.0%	3	5.0%[a]	2	2.0%
7	5.0%	9	1.5%	4	1.0%
11	3.5%	15	0.5%	6...24	0.5%
13	3.0%	21	0.5%		
17	2.0%				
19	1.5%				
23	1.5%				
25	1.5%				

Table E.3: Voltage harmonic values at the point of supply given in percents of the voltage fundamental U_1 according to standard EN 50160.

Then, assuming that $x/r = 20$:

$$R_{tr1} = \frac{1}{\sqrt{1 + (x/r)^2}} \cdot Z_{tr1} = 2.4454 \cdot 10^{-3}\ \Omega \tag{E.25}$$

$$X_{tr1} = (x/r) \cdot R_{tr1} = 48.90 \cdot 10^{-3}\ \Omega \tag{E.26}$$

6.2. To define the filter impedance.

The filter impedance is the substration of the total impedance and the transformer impedance. As for the transformer, a ratio of $x/r = 20$ has been assumed for the filter reactance and the resistance:

$$Z_{f1} = Z_1 - Z_{tr1} = 1.4340\ \Omega \tag{E.27}$$

$$R_{f1} = \frac{1}{\sqrt{1 + (x/r)^2}} \cdot Z_{f1} = 71.6 \cdot 10^{-3}\ \Omega \tag{E.28}$$

$$X_{f1} = (x/r) \cdot R_{f1} = 1.4322\ \Omega \tag{E.29}$$

7. Standard limits used for filter validation

This section presents the harmonic limits defined by standards EN 50160 (for voltage harmonics) and IEEE 519-1992 (for current harmonics).

Maximum Harmonic Current distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
$\mathbf{I_{SC}/I_L}$	$\mathbf{< 11}$	$\mathbf{11 \leq h < 17}$	$\mathbf{17 \leq h < 23}$	$\mathbf{23 \leq h < 35}$	$\mathbf{35 \leq h}$	**TDD**
$< 20^*$	4.0	2.0	1.5	0.6	0.3	5.0
$20 < 50$	7.0	3.5	2.5	1.0	0.5	8.0
$50 < 100$	10.0	4.5	4.0	1.5	0.7	12.0
$100 < 1000$	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above						
Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed						
*All pozer generation equipment is limited to those values of current distortion, regardless of actual I_{SC}/I_L						
where, I_{SC} = maximum short-circuit current at PCC I_{SC} = maximum demand load current (fundamental frequency component) at PCC						

Table E.4: Current Distortion Limits for General Distribution Systems (120 V through 69 000 V): IEEE 519-1992