

Power quality improvements in 25 kV 50 Hz railways substation based on chopper controlled impedances

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Université de Toulouse

THÈSE

En vue de l'obtention du

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Giuliano RAIMONDO

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Titre :

POWER QUALITY IMPROVEMENTS IN 25kV 50Hz RAILWAY SUBSTATIONS BASED ON CHOPPER CONTROLLED IMPEDANCES

Ecole doctorale :
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M. Andrea DEL PIZZO
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M. Luigi ACCARDO
M. Philippe LADOUX
M. Pompeo MARINO

Thèse

en co-tutelle

Tesi

in co-tutela

En vue de l'obtention du

DOCTORAT DE L'UNIVERSITÉ DE TOULOUSE

Délivré par:
Institut National Polytechnique de Toulouse (INP Toulouse)
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Ai fini del conseguimento del

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Rilasciato da:
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Giuliano Raimondo

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POWER QUALITY IMPROVEMENTS IN 25kV 50Hz RAILWAY SUBSTATIONS BASED ON CHOPPER CONTROLLED IMPEDANCES

Jury/ Commissione

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SUMMARY

This work is the result of collaboration between the LAPLACE laboratory, the "Seconda Università degli Studi di Napoli" (SUN) and the French national railways operator SNCF. The research topic treated herein concerns the use of power electronic devices in 25kV/50Hz railways substations to achieve power quality improvements.

In railway transportation, single-phase 25kV-50Hz electrification system is widely diffused especially for high-speed railway applications. Although electrified DC systems are still widely applied, the adoption of AC single-phase system offers economical advantages for the infrastructures of about 30% in terms of investment, exploitation and maintenance.

In early ages, due to its very simple diagram, there was no necessity to integrate power electronics in substations. However, for the last decade, the interest in power electronic equipments raised since they can provide the solution for network optimization when traffic increases or when a difficulty is foreseen for a substation implementation. Two types of devices are implemented today on the French Railway Network: Reactive Power compensators and Voltage Unbalance compensators.

This thesis presents an investigation into new topologies based on the concept of *"Chopper Controlled Impedances"(CCI)*. Compared to existing solutions, the new topologies show interesting features in terms of semi-conductor losses reduction and volume of reactive components.

The manuscript is developed through three main parts:

Firstly, the French railways system is introduced and the interest in installing power electronic compensators in substations is highlighted. After a brief description of currently used solutions, the CCI concept is presented: the use of Pulse Width Modulated AC Choppers allows achieving structures which behave as variable impedances.

In the second part, the use of CCI structures in reactive power compensation is investigated. The SNCF substation of Revest is under study. It is equipped by a 60MVA single phase transformer with the primary side connected to a 225kV transmission line. Based on the step-down or step-up functioning mode of CCIs, two topologies of reactive power compensator are presented. The converter design is developed on the base of a measurement campaign carried out at the substation. Numerical simulations using real current and voltage waveforms are presented. Finally, experimental results carried out at the SNCF test platform on a 1.2MVAR prototype are shown.

In the last part, the problem of voltage unbalance is treated. Using the concept of CCI, the feasibility of an active Steinmetz circuit based on AC choppers is explored. As a case study, the substation of Evron is considered. It is a 32MVA substation connected to a 90kV transmission line. Measurements carried out on

the substation site allow the compensator design and the possibility to consider real waveforms for current and voltage in numerical simulations. A comparison with classical solution based on two levels VSI and three levels NPC-VSI highlights the advantages of the proposed solution. Calculation and simulation results show that the stored energy in reactive elements is reduced by a factor six whereas the semiconductor losses are 40% lower. Experimental results obtained on a scaled demonstrator (≈ 1.5 kVA) validate the principle of the active Steinmetz circuit.

RÉSUMÉ

Ce travail est le résultat d'une collaboration entre le laboratoire LAPLACE, la "Seconda Università degli Studi di Napoli" (SUN) et la Société National des Chemins de fer Français SNCF. Le sujet de recherche concerne l'utilisation de dispositifs électroniques de puissance dans les sous stations ferroviaires 25kV/50Hz afin d'améliorer la qualité de l'énergie électrique.

Dans le transport ferroviaire, le système d'électrification monophasé 25kV/50Hz est largement diffusé en particulier pour les lignes ferroviaires à grande vitesse. Bien qu'aujourd'hui les systèmes d'alimentation en courant continu soient encore largement utilisés, l'adoption du courant alternatif monophasé offre des avantages économiques pour les infrastructures d'environ 30% en termes d'investissement, d'exploitation et d'entretien.

Initialement, compte tenu de la simplicité du circuit, il n'y avait aucune nécessité d'intégrer de l'électronique de puissance dans les sous stations. Toutefois, au cours de la décennie passée, l'intérêt pour ces équipements est apparu car ils peuvent apporter une solution d'optimisation du réseau lorsque le trafic augmente ou lorsqu'une nouvelle sous station est envisagée. Deux principaux types de dispositifs sont installés aujourd'hui sur le réseau ferré français : les compensateurs de puissance réactive et les compensateurs de déséquilibre de tension.

Cette thèse présente de nouvelles topologies de compensateurs basées sur le concept d'impédances contrôlées par gradateur MLI. Comparées aux solutions existantes, ces topologies ont des caractéristiques particulièrement intéressantes en termes de pertes dans les semi-conducteurs et de volume des composants réactifs.

Le manuscrit contient trois parties principales:

La première partie présente le principe de l'électrification en 25kV/50Hz et souligne l'intérêt d'installer des moyens de compensation statique dans les sous stations. Après une description des solutions actuellement utilisées, le concept d'impédance contrôlée par gradateur MLI (CCI : Chopper Controlled Impedance) est ensuite présenté.

La deuxième partie du travail concerne l'utilisation du concept de CCI pour la compensation de puissance réactive. La sous-station SNCF de Revest est considérée comme cas d'étude. Celle-ci est équipée d'un transformateur monophasé de 60MVA dont le primaire est connecté à une ligne de transport 225kV. Deux topologies de compensateur de puissance réactive, basées sur des montages abaisseur ou élévateur de tension sont présentées. Le dimensionnement des gradateurs est effectué sur la base d'une campagne de mesures réalisée à la sous station. Des simulations numériques utilisant des formes d'ondes réelles de courant et de tension sont présentées. Des résultats expérimentaux effectués à la plateforme de test de la SNCF sur un prototype de 1,2MVAR permettent de valider le concept de CCI.

La dernière partie du travail concerne le problème du déséquilibre de tension en amont de la sous station. Un circuit de Steinmetz « actif », toujours basée sur des gradateurs MLI, est présenté et étudié. La sous station SNCF d'Evron est alors considérée comme cas étude. Celle-ci comporte un transformateur de 32MVA et est connectée à une ligne de transmission 90kV. Les mesures effectuées sur le site permettent le dimensionnement du compensateur ainsi que l'utilisation des formes d'onde réelles de courant et de tension dans les simulations numériques. Une comparaison avec des solutions classiques basées sur des onduleurs 2 niveaux et 3 niveaux souligne les avantages de la solution proposée. Ainsi, les résultats des calculs et des simulations montrent que l'énergie stockée dans les éléments réactifs est réduite d'un facteur six et que les pertes dans les semi-conducteurs sont réduites de 40%.

Des résultats expérimentaux obtenus sur une maquette de 1.5 kVA permettent de valider le principe du circuit de Steinmetz actif.

RIASSUNTO

Il presente lavoro è il risultato di una collaborazione tra il laboratorio LAPLACE, la Seconda Università degli Studi di Napoli (SUN) e l'operatore nazionale delle ferrovie francesi SNCF. La tematica di ricerca concerne l'impiego dei dispositivi di elettronica di potenza nelle sottostazioni ferroviarie 25kV/50Hz al fine di migliorare la qualità dell'energia elettrica.

Il sistema di alimentazione in oggetto è ampiamente diffuso, specialmente per linee ad alta velocità e ad elevata capacità di traffico. I vantaggi economici dell'alimentazione in AC rispetto all'alimentazione in continua in termini di investimento, gestione e manutenzione sono stimati in circa il 30%.

Al debutto delle reti ferroviarie in alternata, data la semplicità del sistema, non si poneva la necessità di integrare dispositivi di elettronica di potenza nelle sottostazioni. Tuttavia, negli ultimi decenni l'interesse nei convertitori è cresciuto notevolmente in quanto questi rappresentano una soluzione a problemi legati al funzionamento della sottostazione dovuti all'incremento del traffico o addirittura possono rappresentare una alternativa alla realizzazione di nuove sottostazioni.

La tesi presenta un investigazione nella possibilità di impiegare nuove topologie di convertitori basate sul concetto di "Chopper Controlled Impedances". Confrontate con le soluzioni classiche, queste nuove topologie mostrano caratteristiche interessanti in termini di riduzione delle perdite nei semiconduttori e riduzione del volume degli elementi reattivi.

Il lavoro è sviluppato secondo tre parti principali:

In primis, si introduce il sistema ferroviario francese della SNCF, evidenziando i motivi che suscitano l'interesse nell'installazione di convertitori elettronici di potenza nelle sottostazioni. Dopo una breve descrizione delle soluzioni attualmente impiegate, viene presentato il concetto di "Chopper Controlled Impedance": l'impiego di convertitori PWM AC Chopper consente di realizzare strutture di conversione che si comportano come impedenze variabili.

Nella seconda parte, si studia la possibilità di impiegare sistemi CCI nella compensazione della potenza reattiva. La sottostazione della SNCF di Revest viene considerata come caso studio. Quest'ultima alimenta la catenaria mediante un trasformatore monofase da 60MVA connesso al primario ad una linea di trasmissione a 225kV. Per il caso studio vengono proposte due soluzioni per la compensazione della potenza reattiva, basate sul funzionamento dei convertitori CCIs in modalità step-down o step-up. Il progetto dei sistemi di compensazione è sviluppato sulla base di informazioni ottenute da una campagna di misure effettuate nella sottostazione. Vengono inoltre presentate simulazioni numeriche effettuate impiegando forme d'onda reali di tensioni e correnti registrate durante le misurazioni. Infine, vengono riportati i risultati sperimentali ottenuti al centro prove della SNCF su un prototipo da 1.2MVAR

Nell'ultima parte viene trattata la compensazione degli squilibri di tensione. Ancora impiegando il concetto di CCI viene studiata la fattibilità di un circuito di Steinmetz attivo basato su convertitori AC choppers.

Anche in questo caso di considera una sottostazione della SNCF, la sottostazione di Evron, come sito di riferimento per lo studio. Si tratta di una sottostazione da 32MVA connessa ad una rete di trasmissione a 90kV. Le misure effettuate sul sito consentono di dedurre le informazioni utili al dimensionamento del compensatore e inoltre consentono di utilizzare forme d'onda reali per tensioni e correnti nelle simulazioni numeriche. In seguito, si riporta uno studio comparativo con soluzioni classiche basate su VSI 2 livelli o 3 livelli NPC, evidenziando i vantaggi della soluzione proposta. Risultati analitici e simulazioni mostrano che l'energia immagazzinata negli elementi reattivi è ridotta di un fattore di circa 6 e le perdite nei semiconduttori sono ridotte del 60%. Infine, vengono presentati dei risultati sperimentali ottenuti su un prototipo in scala (≈1.5 kVA) che consentono di validare il principio di funzionamento del circuito di Steinmetz attivo.

RESUME DE LA THESE EN LANGUE FRANÇAISE

Chapitre I : Introduction

Ce chapitre présente brièvement le système ferroviaire de la SNCF et en particulier le réseau 25kV/50Hz.

L'intérêt pour l'installation de dispositifs électroniques de puissance dans les sous stations a considérablement augmenté ces dernières années. En fait, les convertisseurs statiques permettent de répondre aux exigences de qualité imposées par le fournisseur d'énergie électrique et aussi d'assurer le bon fonctionnement de la sous station.

Actuellement deux types de compensateurs sont installés dans les sous-stations de la SNCF (Fig. 3):

- Les Compensateurs de puissance réactive permettent d'éviter les pénalités imposées par le fournisseur d'électricité lorsque le facteur de déplacement est en dessous d'une valeur minimale (0,93). De plus, en cas de trafic élevé, ils peuvent maintenir la tension de caténaire au dessus de la limite basse normative (19kV) et réduire les pertes en ligne. Ils sont généralement installés au secondaire du transformateur de la sous-station.

- Les Compensateurs de déséquilibre de tension réduisent la composante inverse du courant consommé par la sous-station et diminuent ainsi le taux de déséquilibre de tension au point de raccordement. Ils sont habituellement connectés directement au réseau de transport d'énergie électrique.

Les solutions actuellement utilisées par la SNCF dans le cas de la compensation de puissance réactive sont des convertisseurs à thyristors ou des batteries de condensateurs fixes. Dans le cas de la compensation du déséquilibre, la solution utilisée est basée sur des onduleurs de tension.

Ces solutions présentent des inconvénients importants.

La compensation avec batteries fixes est économique mais ne permet pas une compensation réglable en fonction de la charge.

Les solutions réglables à base de gradateurs à thyristors sont caractérisées par une émission d'harmonique du courant à basse fréquence qui nécessite l'installation de filtres volumineux.

Enfin, les topologies basées sur des onduleurs de tension commandés en modulation de largeur d'impulsion ont l'inconvénient d'avoir des pertes élevées dans les semi-conducteurs qui nécessitent l'installation de systèmes de refroidissement, augmentant les coûts de gestion et de fonctionnement de la sous-station. De plus, que ce soit pour la compensation de déséquilibre ou de réactif, ces convertisseurs nécessitent des condensateurs de forte capacité sur le bus continu afin de réduire l'ondulation de tension provoquée par la puissance fluctuante.

Chapitre II : Le Concept d'Impédance Contrôlée par gradateur MLI

Ce chapitre présente le Concept d'Impédance Contrôlée par gradateur MLI (CCI – Chopper Controlled Impedance). Des convertisseurs directs alternatif-alternatif sont utilisés pour réaliser des impédances contrôlées (inductives ou capacitives) à la fréquence fondamentale.

La structure du convertisseur (Fig. 29) se compose de deux cellules de commutation commandées en fonction du signe de la tension d'entrée (Fig. 31).

Deux modes de fonctionnement possibles sont présentées, le mode abaisseur de tension (fig. 33) ou le mode élévateur de tension (fig. 34). Ces modes vont déterminer deux lois différentes de variation du module de l'impédance contrôlée (Table I).

Pour les applications de forte puissance, l'association des convertisseurs en parallèle (fig. 40) ou en série (fig. 42) est possible, afin d'obtenir les niveaux de courant et de tension nécessaires. Dans ce cas, si les modulateurs sont entrelacés, il y a une amélioration de la qualité du courant ou de la tension car la fréquence apparente de commutation est plus élevée.

Les topologies de compensateur introduites dans ce chapitre représentent une solution alternative à ceux qui sont actuellement utilisées par la SNCF. En fait, comparativement à la solution à gradateurs à thyristors, les gradateurs MLI ne génèrent pas d'harmoniques en basse fréquence. D'autre part, par rapport aux solutions basées sur des onduleurs de tension, les pertes dans les semi-conducteurs et les énergies stockées dans les éléments réactifs sont réduites significativement.

Chapitre III : Compensation de Puissance Réactive à base d'Impédances Contrôlées par Gradateur MLI.

Ce chapitre présente l'utilisation des impédances contrôlées par gradateur MLI pour la compensation de puissance réactive dans les sous stations 25kV/50Hz.

La sous-station de la SNCF de Revest (Région Parisienne) est considérée comme cas d'étude. Il s'agit d'une sous station de 60MVA connectée à une ligne à haute tension 225kV (fig. 44). Ce chapitre constitue une étude de faisabilité relative à l'installation dans la sous-station d'un compensateur de puissance réactive basé sur des impédances contrôlées.

La première partie présente des mesures effectuées sur plusieurs mois sur le site de Revest. Celles-ci permettent d'obtenir des informations utiles pour le dimensionnement du compensateur. En fait, l'analyse harmonique du courant absorbé par la sous-station permet de placer les fréquences de résonance introduites par les filtres des gradateurs MLI. Par ailleurs, une analyse statistique sur la réduction des pénalités imposées sur le facteur de déplacement permet de déterminer le niveau de puissance du compensateur (fig. 50).

Deux solutions sont présentées sur la base des modes de fonctionnement abaisseur (fig. 51) ou élévateur (fig. 58).

La topologie à base de gradateurs élévateurs de tension est plus intéressante, puisque elle peut être 'installée en sous station sans transformateur de raccordement. Pour cette configuration, les résultats des simulations tiennent compte des formes d'ondes réelles de tension et de courant mesurées dans la sous-station. Enfin, la dernière partie de ce chapitre présente les résultats expérimentaux obtenus sur un prototype de 1.2MVAR (fig. 67) à la plateforme d'essais de la SNCF à Vitry.

Chapitre IV : Compensation de déséquilibre de tension basée sur un circuit de Steinmetz à Impédances Contrôlées par gradateur MLI.

Dans ce chapitre, le concept d'impédance contrôlée par gradateur MLI est appliqué à la compensation des déséquilibres de tension dans les sous-stations.

Le circuit de Steinmetz (fig. 80) est classiquement utilisé pour connecter des charges monophasées à un réseau triphasé. Il se compose d'une bobine et d'un condensateur dimensionnés en fonction de la charge monophasée pour rééquilibrer les courants de ligne. Cette technique de compensation, en utilisant de simples éléments réactifs n'est efficace que si la charge est fixe. Dans le cas d'une sous-station où la consommation de puissance dépend de la circulation ferroviaire, cette solution est clairement inadaptée.

En utilisant les impédances contrôlées, il est possible de réaliser un compensateur de Steinmetz actif (fig. 83). Selon la puissance absorbée par la sous-station, les impédances sont contrôlées pour compenser le déséquilibre généré par la sous station.

Cette solution présente toutefois l'inconvénient de compenser la composante inverse de courant que dans une zone limitée du plan complexe (fig. 86). Ainsi, afin de ne pas dégrader le facteur de puissance sur le réseau triphasé, seulement la partie réelle de la composante inverse est compensée (fig. 87). Cela rend le dispositif inadéquat pour des applications où une compensation totale et instantanée des déséquilibres est nécessaire, ce qui n'est pas requis par le fournisseur d'énergie électrique dans le cas d'une sous station ferroviaire.

Une compensation moyenne est suffisante car les limites sont imposées sur mesures moyennées sur 10 minutes. De plus, les anciennes locomotives à thyristors sont progressivement remplacées par des engins à absorption sinusoïdale avec facteur de puissance unitaire. Par conséquent, le fait de compenser seulement la partie réelle de la composante inverse du courant se justifie pleinement.

Malgré un domaine de compensation limité, cette solution présente des avantages significatifs en termes de coûts par rapport aux solutions traditionnelles qui sont détaillés dans le chapitre VI.

Chapitre V : Analyse de la qualité de l'énergie électrique d'une sous-station

La sous-station d'Evron (Pays de la Loire) (fig. 88) est considérée comme cas d'étude pour la compensation des déséquilibres de tension. Ce chapitre présente une analyse des mesures effectuées sur le site de la SNCF afin d'obtenir des informations utiles pour le dimensionnement du compensateur.

La première partie présente les mesures de puissance active, réactive (Fig. 89) et apparente (Fig. 90) effectués pendant environ 6 ans et moyennées sur 10 minutes. A partir de ces mesures, une analyse statistique (Fig. 91 et 92) montre qu'une charge de 10MVA peut être considérée comme référence pour dimensionner le compensateur de déséquilibre.

Une analyse harmonique des formes d'ondes des tensions et des courants mesurées au point de raccordement de la sous station sur le réseau haute tension 90 kV permet d'obtenir des informations utiles pour le dimensionnement du compensateur ainsi que sur le placement des fréquences de résonance des filtres associés aux gradateurs MLI.

Chapitre VI : Compensation des déséquilibres de tension dans la sous-station d'Evron

Ce chapitre présente une étude comparative de la solution à impédances contrôlées et de la solution à onduleurs de tension Le dimensionnement des convertisseurs est basé sur les résultats de l'analyse présentée dans le chapitre précédent. La comparaison est basée sur l'utilisation d'un même module IGBT (3,3kV/1,5kA).

En premier lieu, ce chapitre décrit le dimensionnement du compensateur sur la base d'onduleurs de tension 2 niveaux puis 3 niveaux (NPC). Le compensateur est dimensionné pour garantir un taux de déséquilibre de 1.5% lorsque la sous-station alimente une charge de 10MVA à facteur de puissance unitaire dans le cas où la puissance de court-circuit du réseau d'alimentation est de 295MVA (1^{er} mode dégradé).

Afin d'obtenir le niveau de puissance nécessaire, les onduleurs de tension sont connectés en parallèle.

Ce chapitre présente le calcul des pertes dans les IGBT pour les deux solutions. Les résultats des calculs analytiques sont validés grâce à l'utilisation du logiciel PSIM et du module thermique.

Le compensateur de déséquilibre basé sur des onduleurs 2 niveaux présente environ 128kW de pertes tandis que la solution à onduleurs NPC présente des pertes totales d'environ 80kW.

La deuxième partie de ce chapitre concerne l'utilisation du circuit de Steinmetz actif à la sous-station d'Evron. La puissance du compensateur est choisie comme dans le cas précédent en fonction de la limite d'un taux de déséquilibre de tension de 1,5% dans un cas de réseau en mode dégradé.

La solution proposée garantit seulement la compensation de la partie réelle de la composante inverse de courant. Afin de montrer que cette limitation n'affecte pas l'efficacité du dispositif, un algorithme numérique (Fig. 127) est utilisé pour simuler la présence du compensateur dans la sous-station pendant 2 heures, en utilisant les mesures effectuées sur le site. Enfin, une analyse statistique réalisée sur six ans d'enregistrements, indique que l'utilisation de la solution proposée garantit une réduction de pénalités dans 98% (fig. 152) des cas.

Les critères de dimensionnement du compensateur de Steinmetz actif tiennent compte du contenu harmonique du courant mesuré à la sous-station. Le schéma final du compensateur pour la sous-station d'Evron est présenté à la figure 156.

Le calcul analytique des pertes dans les semi-conducteurs est également validé avec le module thermique de PSIM. Elles sont évalués pour cette topologie à environ 61kW.

La synthèse comparative (fig. 167) des pertes totales des trois topologies étudiées montre que pour le compensateur actif de Steinmetz, celles-ci sont fortement réduites. Les trois topologies sont également comparées en termes d'énergie stockée dans les éléments réactifs (fig. 168). Même dans ce cas la solution à impédance contrôlée par gradateur MLI (Steinmetz Actif) présente des avantages significatifs en termes de volume des éléments réactifs.

Enfin, ce chapitre présente des résultats de simulation de ce nouveau type de compensateur. Ceux-ci démontrent le bon fonctionnement de la structure même lorsque les formes d'ondes des tensions et des courants sont distordues et conformes à celles relevées sur le site d'Evron.

Chapitre VII : Compensateur à circuit de Steinmetz actif – Résultats Expérimentaux.

Ce dernier chapitre présente les résultats expérimentaux obtenus sur un prototype de compensateur de Steinmetz actif de puissance réduite (≈ 1.5kVA), réalisé au laboratoire LAPLACE à Toulouse.

La figure 175 montre un schéma du dispositif expérimental. Un autotransformateur est utilisé pour obtenir une source triphasée. Deux gradateurs MLI (inductifs et capacitifs) sont réalisés avec des IGBT sur circuit imprimé et une résistance de 2.2 kW est utilisée comme charge monophasée. Les essais ont été effectués sous une tension de 300V. Une carte dSPACE est utilisée pour contrôler les gradateurs (fig. 180). Celle-ci assure un contrôle en boucle fermée de la valeur efficace du courant dans les impédances contrôlées.

Le chapitre montre les grandeurs fondamentales avant et après la compensation. La charge monophasée provoque un déséquilibre des tensions d'environ 2,1% (fig. 181). Lorsque le compensateur est activé, le taux de déséquilibre est ramené à 0,55% (fig. 184). Ce qui valide le bon fonctionnement du compensateur.

Conclusion & Perspectives

Suite à l'augmentation du trafic ferroviaire, les sous-stations SNCF 25kV/50Hz sont de plus en plus concernées par les problèmes de qualité de l'énergie électrique. Dans la plupart des cas, afin de respecter les limites imposées par le fournisseur d'énergie ou de garantir le bon fonctionnement du réseau ferroviaire lui-même, l'opérateur des chemins de fer est obligé d'installer des dispositifs électroniques de puissance dans la sous-station.

Deux principaux types de dispositifs sont installés aujourd'hui sur le réseau ferré Français: les compensateurs de puissance réactive et les compensateurs de déséquilibre de tension

Les premiers permettent d'éviter des pénalités imposées par le fournisseur d'énergie et liées à la dégradation du facteur de puissance. En plus, ils peuvent réguler la tension de caténaire lorsque le trafic augmente. Cela permet d'éviter que la tension de la caténaire ne descende en dessous du minimum imposé par les normes internationales (19kV).

Les compensateurs de déséquilibre de tension permettent d'augmenter la capacité de la sous-station sans dépasser la limite du taux de déséquilibre fixé par le fournisseur d'énergie.

L'opérateur des chemins de fer peut choisir entre plusieurs topologies de compensateurs disponibles. Néanmoins, chaque topologie détermine une augmentation du coût de fonctionnement de la sous-station, notamment en raison des pertes dans les convertisseurs.

Dans le cadre de ce travail de thèse, nous avons proposé l'utilisation de nouvelles topologies de compensateurs pour les sous-stations 25kV/50Hz. Les impédances contrôlées par gradateur MLI sont des structures caractérisées par de faibles pertes dans les semi-conducteurs et nécessitent des éléments réactifs de volume réduits par rapport aux solutions classiques.

La nouvelle solution proposée est analysée pour la compensation de puissance réactive et la compensation de déséquilibre. Les critères de dimensionnement sont présentés en utilisant les informations obtenues par

des mesures dans deux sous-stations de la SNCF considérés comme cas typiques. Les résultats des simulations et les résultats expérimentaux valident le principe de fonctionnement de ces compensateurs.

Pour la compensation de déséquilibre, le compensateur de Steinmetz actif parait donc très attractif pour les opérateurs ferroviaires. Les faibles pertes permettent une réduction importante des coûts de fonctionnement et d'entretien de la sous-station alors que le volume réduit des éléments réactifs détermine un coût d'achat plus bas.

Une étude comparative entre la nouvelle topologie et la solution classique à onduleurs montre que les pertes sont réduites d'environ 60% et l'énergie stockée dans les éléments réactifs est réduite d'un facteur six.

Depuis dix ans, les solutions à thyristors et onduleurs de tension ont été utilisées et évaluées sur le Réseau Ferré National Français. Logiquement, dans un avenir proche, un compensateur de déséquilibre basé sur les impédances contrôlées par gradateur MLI pourrait donc être construit et installé dans une sous-station.

RIASSUNTO DELLA TESI IN LINGUA ITALIANA

Capitolo I: Introduzione

Il primo capitolo introduce brevemente il sistema ferroviario della SNCF e in particolare la rete alimentata da sottostazioni a 25kV/50Hz.

L'interesse nell'installazione di dispositivi di elettronica di potenza nelle sottostazioni in corrente alternata è aumentato notevolmente negli ultimi anni. I convertitori infatti consentono di rispettare i requisiti sulla qualità dell'energia imposti dal fornitore dell'energia elettrica ed inoltre di garantire il buon funzionamento della sottostazione stessa.

Attualmente 2 tipi di compensatori sono installati nelle sottostazioni della SNCF (Fig. 3):

- Compensatori di potenza reattiva:

  Consentono di evitare le penali imposte dal fornitore dell'energia elettrica quando si scende al di sotto del valore minino del fattore di potenza. Inoltre, in caso di elevato traffico, consentono di aumentare la tensione di catenaria quando questa diminuisce a causa delle perdite sulla linea, evitando che possa scendere al di sotto del limite imposto (19kV). Sono in genere installati al secondario del trasformatore di sottostazione.

- Compensatori di squilibri di tensione

  Hanno lo scopo di ridurre la sequenza inversa di corrente assorbita dalla sottostazione al fine di ridurre il fattore di squilibrio al punto di connessione del primario del trasformatore di sottostazione. Sono in genere connessi direttamente alla rete di trasmissione in alta tensione.

Le soluzioni attualmente impiegate dalla SNCF nel caso della potenza reattiva fanno uso di convertitori basati su tiristori oppure di batterie di compensazione capacitive fisse. Nel caso della compensazione degli squilibri la soluzione adottata è basata su Voltage Source Inverter (VSI).

Queste soluzioni soffrono di notevoli svantaggi.

La compensazione con batterie fisse, è economica ma non consente una compensazione variabile in funzione del carico.

Le soluzioni a tiristori sono caratterizzate da una notevole distorsione armonica a bassa frequenza della corrente che rende necessaria l'installazione di filtri voluminosi.

Infine, la topologia VSI ha il forte inconveniente di avere elevate perdite nei semiconduttori che rendono necessaria l'installazione di grossi sistemi di raffreddamento, aumentando i costi di gestione e funzionamento della sottostazione. Inoltre, nella compensazione degli squilibri, questi convertitori richiedono condensatori di capacità elevata sul bus DC. Questo per ridurre l'elevata ondulazione di tensione dovuta dalla potenza fluttuante legata alla sequenza inversa di corrente che si inietta.

Capitolo II: Il concetto di Impedenza Controllata mediante PWM AC Chopper

Il capitolo introduce il concetto di *Impedenza Controllata mediante AC Chopper (CCI - Chopper Controlled Impedance)*. Convertitori AC/AC di tipo PWM AC Chopper vengono impiegati per realizzare impedenze controllate (induttive o capacitive) alla frequenza fondamentale.

La struttura del convertitore (Fig. 29) prevede 2 celle switching comandate in PWM in funzione del segno della tensione di ingresso (Fig. 31).

Vengono presentate due possibili modalità di funzionamento, step-down (Fig. 33) o step-up (Fig. 34) che consentono di ottenere due differenti leggi di variazione del modulo dell'impedenza controllata (Table I).

In applicazioni di elevata potenza, l'associazione dei convertitori in parallelo (Fig. 40) o in serie (Fig. 42) è possibile, consentendo di ottenere i livelli di potenza richiesti e di superare i problemi di elevate tensioni. Inoltre interallacciando le PWM dei moduli si ha un miglioramento della qualità della corrente o tensione, avendo una frequenza di switching apparente più elevata.

La topologia di convertitori introdotta nel capitolo, può rappresentare una soluzione interessante come alterativa a quelle attualmente impiegate. Infatti, rispetto alle soluzione a tiristori, gli AC Chopper non generano armoniche di corrente a bassa frequenza. Inoltre, confrontate con soluzioni basate su VSI, le perdite nei semiconduttori sono notevolmente ridotte negli AC-Chopper, e anche gli elementi reattivi impiegati sono di minor volume.

Capitolo III: Compensazione della potenza reattiva mediante l'impiego di Impedenze Controllate

Il capitolo propone l'impiego delle impedenze controllate mediante chopper nella compensazione della potenza reattiva nelle sottostazioni.

La sottostazione della SNCF di Revest è considerata come caso studio. Si tratta di una sottostazione di 60MVA connessa ad una linea alta tensione a 225kV (Fig. 44). Nel capitolo viene sviluppato uno studio di fattibilità di installazione nella sottostazione in oggetto di un compensatore di potenza reattiva basato su CCI.

Nella prima parte, vengono presentate le misure effettuate duranti diversi mesi sul sito della SNCF. Queste consentono di ricavare informazioni utili al dimensionamento del compensatore. Infatti, l'analisi armonica della corrente assorbita dalla sottostazione consente di posizionare le risonanze introdotte in intervalli di frequenze ammissibili. Inoltre, da una analisi statistica sulla riduzione delle penalità imposte sul fattore di potenza, viene determinata la taglia del compensatore variabile da installare (Fig. 50).

Vengono presentate due possibili soluzioni basate sulla modalità di funzionamento step down (Fig. 51) e step-up (Fig. 58) e i relativi criteri di progetto.

La soluzione basata sul modo di funzionamento step-up risulta più interessante, consentendo una installazione transformeless nella sottostazione. Per questa configurazione, si riporta il risultato di alcune simulazioni effettuate considerando forme d'onda reali per correnti e tensione misurate nella sottostazione. Infine, si presentano i risultati sperimentali ottenuti su un prototipo da 1.2MVAR (Fig. 67) nel centro di prove della SNCF a Vitry.

Capitolo IV: Compensazione degli squilibri di tensione impiegando il circuito di Steinmetz attivo a impedenze controllate.

In questo capitolo, il concetto di impedenza controllata da chopper viene applicato nella compensazione degli squilibri di tensione.

Il circuito di Steinmetz (Fig. 80) viene utilizzato per connettere carichi monofase ad una rete trifase. Consiste in un induttore ed un condensatore opportunamente dimensionati e connessi al carico monofase al fine di renderlo equilibrato nei confronti della rete trifase. Questa tecnica di compensazione, facendo uso di semplici elementi reattivi risulta efficace solo se il carico è fisso. Nel caso di una sottostazione in cui l'assorbimento di potenza dipende dal traffico ferroviario, questa soluzione risulta chiaramente poco adatta.

Impiegando le impedenze controllate da chopper, viene proposto nel capitolo un circuito di Steinmetz attivo (Fig. 83). In funzione della potenza assorbita dalla sottostazione, le impedenze controllate assumono i valori necessari alla compensazione dello squilibrio generato.

Questa soluzione, ha però lo svantaggio di compensare sequenze inverse solo in una regione limitata del piano complesso (Fig. 86). Inoltre, se non si vuole degradare il fattore di potenza trifase, allora solo la parte reale della componente simmetrica inversa deve essere compensata (Fig. 87). Questo quindi, rende il dispositivo poco adatto nelle applicazioni dove una compensazione degli squilibri istantanea è richiesta.

Nel caso delle sottostazioni ferroviarie, una compensazione media è sufficiente a rispettare i limiti, imposti su medie di 10 minuti. Inoltre, le vecchie locomotive in funzione saranno sempre meno col passare del tempo, in quanto sostituite da nuovi modelli equipaggiati da convertitori di trazione a fattore di potenza unitario. Di conseguenza, è necessario compensare solo la parte reale della componente simmetrica inversa di corrente assorbita.

Tuttavia, a fronte dello svantaggio legato al dominio di compensazione limitato, questa soluzione presenta dei notevoli vantaggi economici rispetto alle soluzioni classiche. Questo aspetto verrà dettagliato nel capitolo VI.

Capitolo V: Analisi della qualità dell'energia elettrica in una sottostazione

La sottostazione della SNCF di Evron (schema in figura 88) viene considerata come caso di studio per la compensazione degli squilibri di tensione. In tal senso, il capitolo presenta una analisi su misure effettuate sul sito della SNCF al fine di ricavare informazioni utili al dimensionamento del compensatore.

Nella prima parte vengono riportate le misure di potenza attiva,reattiva(Fig. 89) e apparente (Fig. 90) effettuate durante circa 6 anni, su medie di 10 minuti. Da queste si ricava mediante un'analisi statistica che un carico da 10MVA può essere considerato come riferimento nella scelta della taglia del compensatore.

In seguito viene presentata un'analisi armonica delle tensioni e correnti misurate al punto di connessione in alta tensione della sottostazione durante 2 ore. Questo al fine ottenere informazioni utili a progettare il sistema in modo che le eventuali risonanze introdotte siano in intervalli di frequenza consentiti.

Infine, viene riportato il risultato del calcolo della componente simmetrica inversa della corrente assorbita.

Capitolo VI: Compensazione degli squilibri di tensione nella sottostazione di Evron

Il capitolo VI presenta uno studio comparativo tra la soluzione basata su circuito di Steinmetz attivo e le soluzioni classiche basate su VSI. Il dimensionamento dei convertitori è basato sui dati provenienti dalle analisi riportate nel capitolo precedente. Il confronto è basato sull'impiego nelle tre soluzioni dello stesso dispositivo IGBT.

In primis, si descrive il dimensionamento del compensatore basato su VSI 2 livelli e NPC 3 livelli. Il compensatore è dimensionato per garantire un fattore di squilibrio dell'1.5% quando la sottostazione è interessata da un carico da 10MVA a fase nulla, quando la potenza di corto circuito del sistema elettrico è quella minima ipotizzata a 295MVA. Una struttura di moduli VSI associati in parallelo è necessaria per ottenere la potenza di dimensionamento richiesta.

A valle del dimensionamento, viene riportato il calcolo delle perdite negli IGBT per le due soluzioni e se ne validano i risultati mediante l'impiego del simulatore circuitale PSIM e il tool Thermal Module. In totale, il compensatore di squilibri basato su VSI 2 livelli risulta avere perdite per 128kW. Mentre per la soluzione a VSI 3 livelli NPC, le perdite totali ammontano a circa 80kW.

Nella seconda parte si analizza l'impiego del circuito di Steinmetz attivo ad Evron. La taglia del convertitore è scelta come nel caso precedente sulla base del limite del fattore di squilibrio delle tensioni al 1.5% con una potenza di corto circuito minima di 295MVA.

La soluzione proposta, garantisce una compensazione media, in quanto solo la parte reale della componente simmetrica inversa viene ridotta. Al fine di mostrare che questo limite non ne influenzi l'efficacia, un algoritmo numerico (Fig. 127) viene usato per simulare la presenza del compensatore nella sottostazione durante 2 ore, usando le misure effettuate sul sito.

Infine, un'analisi statistica effettuata su sei anni di registrazioni, indica che impiegando la soluzione proposta si ha una riduzione delle penalità del 98% circa (Fig. 152).

In seguito vengono mostrati i criteri di dimensionamento che tengono conto della conoscenza del contenuto armonico della corrente della sottostazione. Lo schema finale del compensatore si Steinmetz attivo per la sottostazione di Evron è presentato in figura 156.

Il calcolo delle perdite, validato anche in questo caso mediante il Thermal Module di Psim, si valutano per questa topologia a circa 61kW.

Una sintesi comparativa (Fig. 167) tra le perdite delle tre topologie di compensatore analizzate mostrano come, per il circuito di Steinmetz attivo, queste siano notevolmente ridotte. Le tre topologie, vengono anche confrontate in termini di energia immagazzinata negli elementi reattivi (Fig. 168). Anche in questo caso la soluzione proposta mostra notevoli vantaggi in termini di dimensione degli elementi reattivi.

Infine, il capitolo riporta il risultato di alcune simulazioni del compensatore proposto. Queste, dimostrano il corretto funzionamento della soluzione basata sulle impedenze controllate anche quando vengono considerate come forme d'onda di tensioni e corrente quelle misurate sul sito della SNCF.

Capitolo VII: Circuito di Steinmetz attivo – Prove sperimentali

L'ultimo capitolo presenta i risultati sperimentali ottenuti su un prototipo di compensatore di Steinmetz attivo di potenza ridotta (≈1.5kVA) realizzato al LAPLACE di Toulouse.

Figura 175 mostra uno schema dell'apparato sperimentale. Un autotrasformatore è impiegato per ottenere una alimentazione trifase, due AC Chopper (induttivo e capacitivo) sono realizzati mediante IGBT e un carico resistivo da 2.2kW è impiegato come carico monofase. I test sono stati effettuati a 300V. Un dSPACE è utilizzato per il controllo del convertitore (Fig. 180). In particolare viene eseguito un controllo a ciclo chiuso del valore rms delle correnti delle due impedenze controllate.

Vengono riportate le registrazioni delle grandezze fondamentali prima e dopo la compensazione dello squilibrio. Il carico monofase determina uno squilibrio delle tensioni pari a circa il 2.1% (Fig. 181). Quando il compensatore è attivato il fattore di squilibrio scende a circa 0.55% (Fig. 184).

In conclusione, il corretto funzionamento del compensatore di Steinmetz attivo è validato.

Conclusioni e Prospettive

In seguito all'aumento del traffico ferroviario, le sottostazioni della SNCF 25kV/50Hz si trovano sempre più ad affrontare problemi di power quality. In molti casi, al fine di rispettare i vincoli imposti dal fornitore dell'energia elettrica o di garantire il buon funzionamento del sistema ferroviario stesso, l'operatore è obbligato a installare dei convertitori di elettronica di potenza nella sottostazione.

I dispositivi installati oggi nelle sottostazioni del sistema francese, sono essenzialmente due: i compensatori di potenza reattiva e i compensatori di squilibri di tensione.

I primi permettono di evitare le penalità imposte dal fornitore dell'energia elettrica legate alla riduzione del fattore di potenza. Inoltre, possono regolare la tensione di catenaria quando a seguito di una aumento del traffico ferroviario. Questa operazione permette di evitare che la tensione di catenaria possa scendere al di sotto del minimo imposto dalle norme internazionali (19kV).

I compensatori di squilibri di tensione permettono di aumentare la capacità della sottostazione evitando di oltrepassare il limite sul fattore di squilibrio fissato dal fornitore dell'energia elettrica.

Le topologie di compensatori che l'operatore ferroviario può impiegare nelle sottostazioni sono molteplici. Tuttavia, ogni topologia determina un aumento dei costi di funzionamento della sottostazione a causa delle perdite nei convertitori.

In questo lavoro di tesi, viene proposto l'utilizzo di nuove topologie di compensatori per le sottostazioni 25kV/50Hz. Le impedenze controllate mediante PWM AC Chopper sono strutture di conversione caratterizzate da basse perdite nei semiconduttori e necessitano di elementi reattivi di volume ridotto rispetto alle soluzioni classiche.

La nuova soluzione proposta è analizzata per la compensazione della potenza reattiva e degli squilibri di tensione. I criteri di dimensionamento presentati sono basati su informazioni ottenute da misure effettuate in

due sottostazioni della SNCF considerate come caso studio. I risultati delle simulazioni e i risultati sperimentali validano il principio di funzionamento di questi compensatori.

Per la compensazione degli squilibri, il compensatore di Steinmetz attivo è di grande interesse per gli operatori ferroviari. Le basse perdite permettono una riduzione importante dei costi di funzionamento e manutenzione della sottostazione. Inoltre, il volume ridotto degli elementi reattivi determina un costo d'acquisto inferiore.

Uno studio comparativo tra la nuova topologia e la soluzione classica basata sull'uso di Voltage Source Inverter, mostra che le perdite sono ridotte di circa il 60% e l'energia immagazzinata negli elementi reattivi è ridotta di circa un fattore sei.

Negli ultimi dieci anni, le soluzioni a tiristori e a voltage source inverter sono state impiegate e valutate nel sistema ferroviario francese. Dunque, a breve un compensatore di squilibri basato su impedenze controllate mediante PWM AC Chopper potrebbe essere realizzato e installato in una sottostazione.

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Chapter I. **Introduction**

In this chapter, the application of power electronic devices in the SNCF 25kV/50Hz railways is discussed. The traffic increasing makes hard for railways operator to handle power quality issues and the respect of the functioning range of electrical parameters requested from european standards.

The installation of power converters can avoid expensive infrastructure modifications, as installation of extras substations or building new power transmission line.

The subject is investigated in this chapter in three parts. Firstly, an introduction of the SNCF AC 25kV/50Hz network is pointed out. Following, in the last two parts, a discussion about the advantages leads by reactive power and voltage unbalance compensation is developed.

I.1 THE RAILWAY SUPPLY SYSTEM 25kV/50Hz

I.1.1 The SNCF electric railways systems

The SNCF railway network is basically supplied by 1500V DC voltage and 25kV/50Hz single phase voltage [1].

The railways electrification in France started at the beginning of the 20th century with the 1.5kV DC. The overhead lines are supplied by means of transformer/rectifier groups connected to the three-phase HV network 63kV or 90kV (figure 1). The distance between substations in is in the range 8-25 km, according to the nominal power. The power draws by substations is up to 15MW.

Regarding the AC 25kV/50Hz system, it debuts in 1954 with the line Valenciennes – Thionville. Overhead lines are supplied using substations equipped by single phase transformers whose the primary is connected to the HV transmission network 63kV to 400kV (figure 2). These substations are placed at distance of about 35km to 90km according to the installation power. Generally, substations nominal power can reach 70MVA.

Compared to 1.5kV DC, the 25kV/50Hz single phase railways system allows economical advantages for the infrastructures of about 30% in terms of investment, exploitation and maintenance.

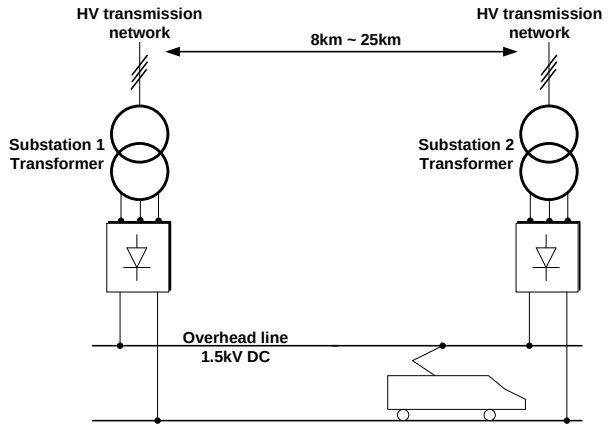


Fig. 1 - 1.5kV railways electrification system

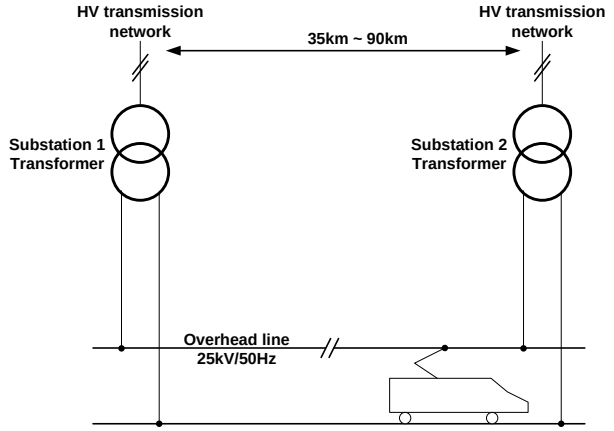


Fig. 2 - 25kV/50Hz AC railways electrification system

I.1.2 Power Electronics in the SNCF 25kV/50Hz railways system

While in DC system, power electronics has been used for more than 50 years through AC/DC rectifiers, in AC system, due to its very simple diagram, there was until now no necessity to integrate power electronics in substations.

However, for the next decades, due to difficulties in funding and also in environmental integration, power electronics can provide the solution for network optimisation when traffic increases or when a difficulty appears for a substation implementation.

Nowadays, in AC electrification, two main types of devices are implemented:

- Reactive Power compensators/High Voltage Boosters
- Three phase line Balancers.

Basically the first device satisfies two objectives. Firstly, it compensates losses in the rail network by injecting reactive energy in order to keep the overhead line voltage in the admissible range [19kV – 29kV] for locomotives. Moreover, as several old locomotives work with a low power factor, reactive power compensation in substations is achieved in order to reduce penalties from the energy provider. In order to avoid this problem, new generation of SNCF locomotives are equipped by unity power factor rectifiers based on Voltage Source Inverters.

The second device allows, in case of weak three-phase public network to enhance the substation power load without exceeding the unbalance limit imposed by the energy provider. In fact, a strong drawback of the AC system is that the substations are phase to phase connected to transmission lines which generates voltage unbalance in high load conditions.

The two compensation systems introduced previously are commonly installed on the railway network as reported in figure 3. These aspects are discussed in detail in the next sections.

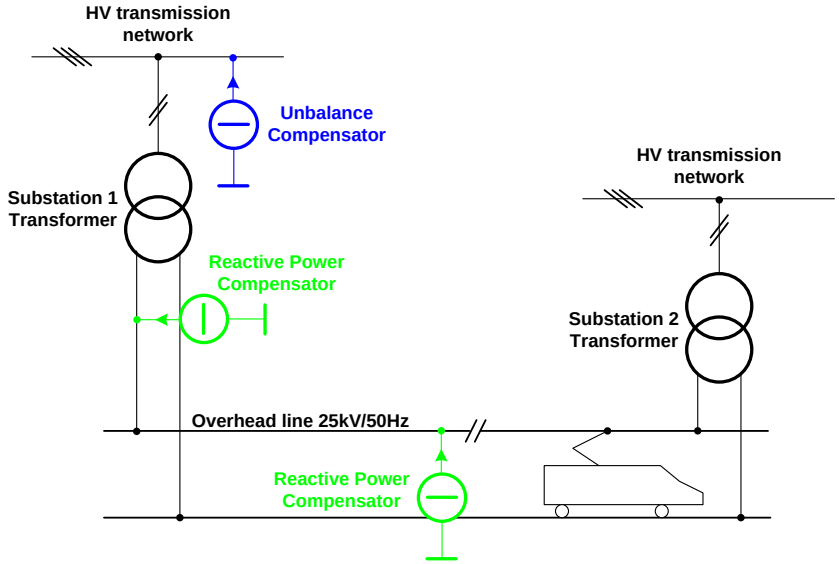


Fig. 3 – Power Electronics devices in 25kV/50Hz railways

I.2 Reactive Power compensation

With the aim of understanding the necessity of reactive power compensators in the SNCF railways network, the influence of locomotives in the traction system is discussed.

A simple scheme of a supply circuit of a traction system is reported in figure 4. The equivalent circuit at grid frequency is shown in figure 5.

With:

u_{HV}: line to line voltage of the three-phase transmission network at the substation coupling point.

R_{HV}, X_{HV}: respectively line resistance and line reactance of the three-phase transmission network

m_{ss}: substation transformer ratio

R_{ss}, X_{ss}: leakage transformer resistance and reactance view at the secondary side

v_{cat}: voltage between overhead line and rail

i_{ss}: current drawn at the secondary of the substation transformer

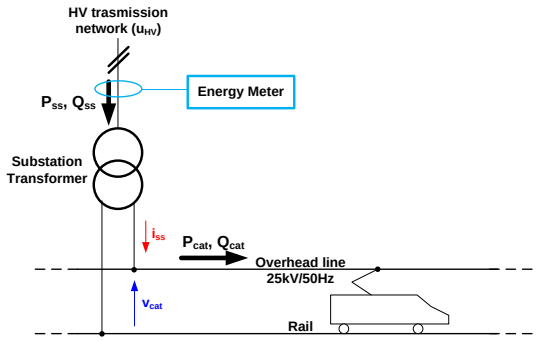


Fig. 4 - a supply circuit of a traction system

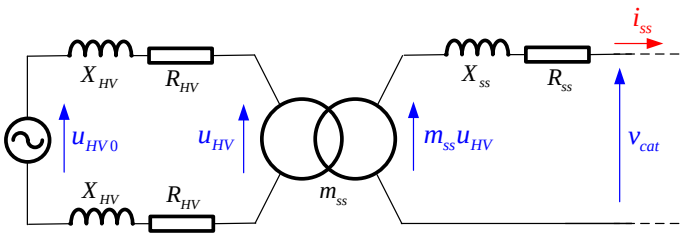


Fig. 5 - equivalent circuit at grid frequency

On this base, the equivalent Thevenin circuit can be pointed out in figure 6.

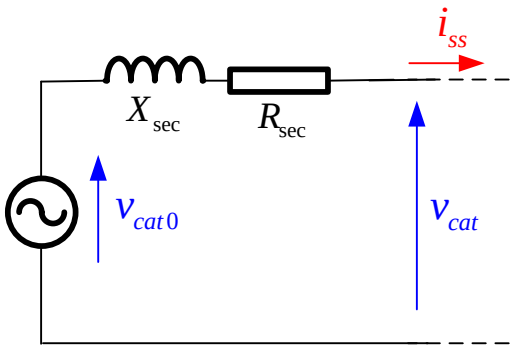


Fig. 6 - Equivalent Thevenin circuit of the substation

The expressions for equivalent reactance X_{sec} and equivalent resistance R_{sec} are the following:

$$X_{\text{sec}} = 2m_{ss}^2 X_{HV} + X_{ss} \quad (1)$$

$$R_{\text{sec}} = 2m_{ss}^2 R_{HV} + R_{ss} \quad (2)$$

The rms value of voltage v_{cat0} is the rms value of the voltage at secondary side of the transformer in open-circuit condition:

$$V_{cat0} = m_{ss} U_{HV0} \quad (3)$$

The Fresnel diagram of the traction circuit is reported in figure 7. Considering the projection on real and imaginary axis, the following equations are obtained:

$$m_{ss}U_{HV0}\cos\theta = X_{\sec}I_{ss}\sin\varphi + R_{\sec}I_{ss}\cos\varphi + V_{cat} \quad (4)$$

$$m_{ss}U_{HV0}\sin\theta = X_{\sec}I_{ss}\cos\varphi - R_{\sec}I_{ss}\sin\varphi \quad (5)$$

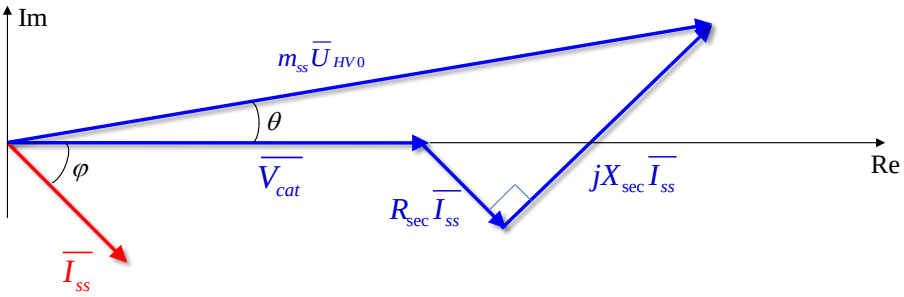


Fig. 7 - Fresnel Diagram

On the assumption that the voltage drop ΔV is low regarding the nominal voltage, the angle θ is small. On this base, a good approximation for the voltage drop is:

$$\Delta V = m_{ss}U_{HV0} - V_{cat} = X_{\sec}I_{ss}\sin\varphi + R_{\sec}I_{ss}\cos\varphi \quad (6)$$

This can be rearranged as following:

$$\Delta V = m_{ss}U_{HV0} - V_{cat} = X_{\sec}\frac{Q_{cat}}{V_{cat}} + R_{\sec}\frac{P_{cat}}{V_{cat}} \quad (7)$$

Where Q_{cat} and P_{cat} are respectively reactive and active power drawn by the trains.

Let's note from the previous equations, where voltage U_{HV0} is assumed as constant, that in case of high power drawn by the trains, the overhead line voltage drop down and can decrease under the minimum value of 19kV imposed by the european standard EN50163 [2]. Thus, in substations supplying high traffic lines, in order to guarantee the locomotives operation, it is mandatory to install reactive power compensator acting as voltage booster devices.

Moreover, to limit losses and voltage drop on transmission lines, the electric energy provider imposes a minimum value for the substation displacement factor. Penalties are applied on reactive energy when this limit is passed. Thus, penalties are avoided or reduced by installing a reactive power compensator device.

I.2.1 Reactive power compensator devices installed in SNCF substations

Currently, two types of reactive power compensation are installed in the SNCF 25kV/50Hz network. The first is a fixed compensation based on capacitive shunt filters. The second is a variable compensation based on a thyristor controlled reactance (TCR). At the moment, the synchronous static compensator (called STATCOM) based on Voltage Source Inverter is not used by the SNCF.

I.2.1.1 Fixed Compensation

In most cases, reactive power compensation in railways is achieved by connecting shunt capacitive filters to the substation. These filters, as reported in figure 8, consist of an inductor L_{fix} and a capacitor C_{fix} connected in series. They are placed at the secondary side of the substation transformer between the overhead line and the rail.

The reactive power provided by the fixed compensation device is:

$$Q_{comp} = \frac{V_{cat}{}^2 C_{fix} \omega_{net}}{1 - L_{fix} C_{fix} \omega_{net}{}^2} \tag{8}$$

Where ω_{net} is the grid angular frequency.

This solution is very straightforward and economical but unsuitable for large reactive power fluctuations. In fact, when the substation is lightly charged, the reactive power is overcompensated and the overhead line voltage exceeds the limit imposed (29kV) by the EN 50_163 standard.

In this case, a variable reactive power compensation system is needed, in order to adapt the level of compensation to the substation load.

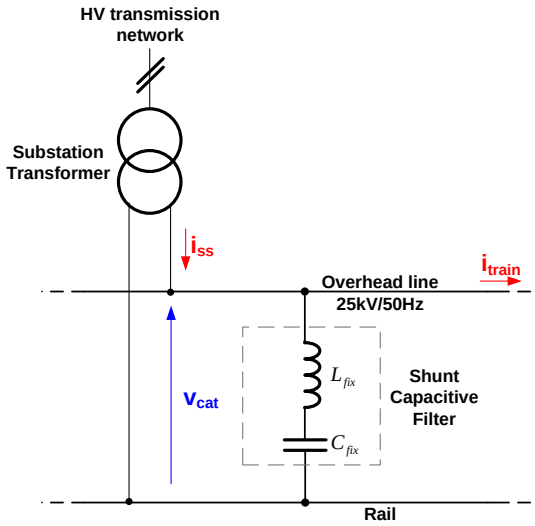


Fig. 8 - Scheme of a substation equipped by fixed reactive power compensation device

I.2.1.2 Variable compensation

Currently, the SNCF used three variable reactive power compensators based on TCRs. The first one was built in the frame of the European project HVB (High Voltage Booster) started in 1998 [3]. The aim of this project was to provide a device able to instantaneously compensate the overhead line voltage drop in function of the train traffic. This compensator was commissioned in 2002 [4]. A scheme of a substation using this solution is presented in figure 9. Basically, the converter topology is composed by a fixed capacitive filter, a single phase TCR that acts as a variable inductor at the grid frequency and a bulky LC filter tuned on

the third harmonic (150 Hz). Pictures of the reactive elements of the compensators are presented in figures 10 and 11.

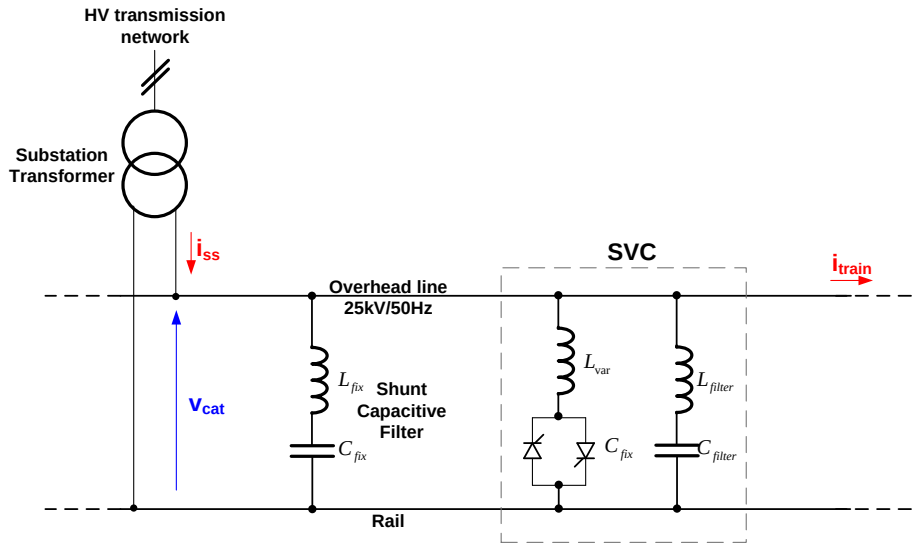


Fig. 9 – Substation equipped by variable reactive power compensator based on thyristors SVC

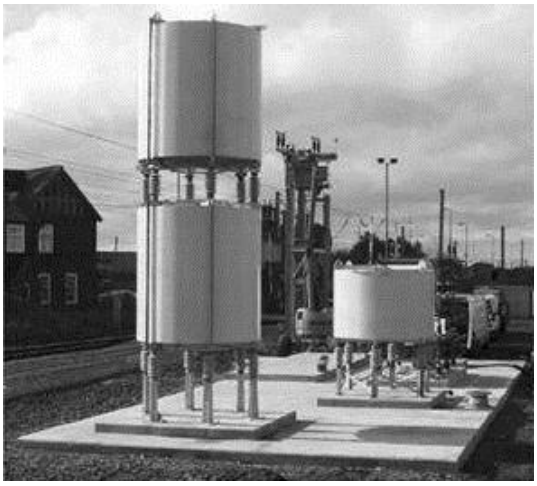


Fig. 10 – Inductor L_{var}



Fig. 11 – Shunt Filter C_{fix} - L_{fix}

This TCR allows the variation of the fundamental lagging current by phase-control, counterbalancing large leading currents from associated fixed capacitors and allowing a continuous compensation of the lagging reactive power. However this solution generates a high level of low rank harmonics and requires onerous LC filters. Moreover, it should be notice that, due to the functioning principle of this compensator, the power losses in semiconductor devices are highest when no compensation is required [5].

I.3 Voltage Unbalance Compensation

In 25 kV/50 Hz railways, the substations are phase to phase connected to transmission lines. They behave as nonlinear and time-varying loads and represent one of the most important sources of voltage unbalance regarding the electricity transmission network

In case of weak networks, railways operators are required to install compensation systems in substations in order to satisfy limits and to avoid penalty. The limits are established by the energy provider with a view to guarantee a sufficient voltage quality to other customers.

Unbalance compensation systems are necessary when the railways operator is interested in increasing traffic on a line and the electric transmission network is not enough "strong" to support a larger load. It is evident that if the voltage unbalance compensation is achieved, the construction of a new transmission line can be avoided, resulting in considerable economical advantages.

In order to understand the phenomenon, some concepts of voltage unbalance theory are pointed out in the following discussions.

I.3.1 Introduction to unbalance

A three-phase AC power system is *balanced* when the three voltages and currents have equal magnitudes and 120° phase-displacements, otherwise it is *unbalanced.*

Unbalanced voltages can produce adverse effects on equipment and on the power system. A small unbalance in the phase voltages can cause an extremely large unbalance in the phase currents and the power system will incur more losses and heating effects. The effect of voltage unbalance can also be severe on equipment such as induction motors, power electronic converters and adjustable speed drives (ASDs) [6].

At the medium and high voltage levels the AC loads phase to phase connected are rare [7]. Some typical loads in this category are as follows:

– traction supplies,
– arc furnaces,
– resistance melting furnaces,
– heavy-current test systems.

AC railway substations, especially for high-speed railway, represent large single-phase loads which draw considerable unbalanced currents from the power-supply system, leading to voltage unbalance.

Figure 12 shows a three phase power systems feeding a single phase substation. Due to the voltage drop on line impedances, PCC voltages $\begin{bmatrix} e_a^{pcc} & e_b^{pcc} & e_c^{pcc} \end{bmatrix}$ are unbalanced.

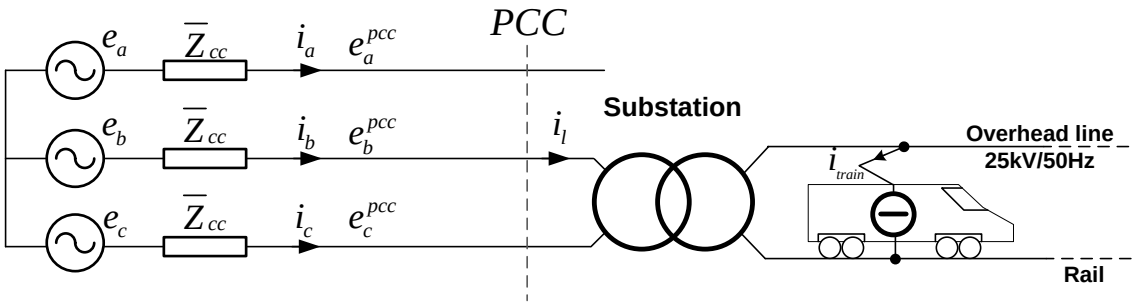


Fig. 12 - Simple traction connection scheme

I.3.2 Characterization of the unbalance

The definition of the voltage unbalance is based on the representation of the three-phase system in the form of symmetrical components. According to Fortescue theory, unbalanced three-phase phasors $\left[\overline{E}_1 \quad \overline{E}_2 \quad \overline{E}_3\right]$ can be decomposed into three symmetrical phasors named *positive*, *negative* and *zero*-sequence components $\left[\overline{E}_+ \quad \overline{E}_- \quad \overline{E}_0\right]$.

Thus, the unbalanced system can be split up into 3 balanced systems:

- a balanced system having the same phase sequence as the unbalanced system:

$$\begin{aligned}\overline{E}_{1+} &= \overline{E}_+ \\ \overline{E}_{2+} &= \alpha^2 \overline{E}_+ \\ \overline{E}_{3+} &= \alpha \overline{E}_+\end{aligned} \tag{9}$$

- a balanced system having the opposite phases sequence to the unbalanced system (rotation of phasors is always anticlockwise, it is the order of the phases that changes, and not the direction of rotation):

$$\begin{aligned}\overline{E}_{1-} &= \overline{E}_- \\ \overline{E}_{2-} &= \alpha \overline{E}_- \\ \overline{E}_{3-} &= \alpha^2 \overline{E}_-\end{aligned} \tag{10}$$

- a balanced system of in-phase quantities:

$$\begin{aligned}\overline{E}_{10} &= \overline{E}_0 \\ \overline{E}_{20} &= \overline{E}_0 \\ \overline{E}_{30} &= \overline{E}_0\end{aligned} \tag{11}$$

where α is the rotational operator $\alpha = e^{j\frac{2\pi}{3}}$.

The unbalanced three phase system can be composed as in (12). An example of symmetrical decomposition of phase voltages is reported in figure 13.

$$\begin{aligned}\overline{E}_1 &= \overline{E}_{1+} + \overline{E}_{1-} + \overline{E}_{10} \\ \overline{E}_2 &= \overline{E}_{2+} + \overline{E}_{2-} + \overline{E}_{20} = \alpha^2 \overline{E}_+ + \alpha \overline{E}_- + \overline{E}_0 \\ \overline{E}_3 &= \overline{E}_{3+} + \overline{E}_{3-} + \overline{E}_{30} = \alpha \overline{E}_+ + \alpha^2 \overline{E}_- + \overline{E}_0\end{aligned} \tag{12}$$

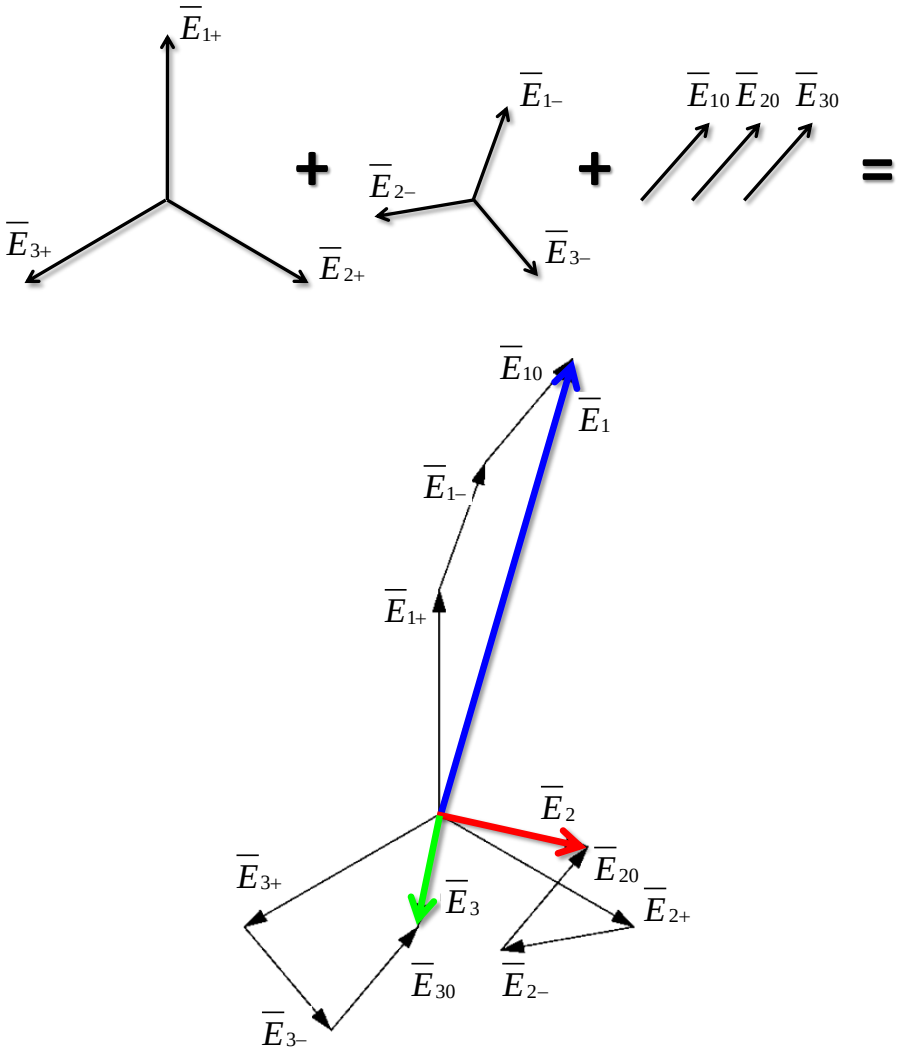


Fig. 13 - Unsymmetrical vector system and its symmetrical components

Simple algebraic manipulation on previous equations would yield the relationship (13) that is known as the Fortescue transformation.

$$\begin{bmatrix} \overline{E}_0 \\ \overline{E}_+ \\ \overline{E}_- \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \alpha & \alpha^2 \\ 1 & \alpha^2 & \alpha \end{bmatrix}\begin{bmatrix} \overline{E}_1 \\ \overline{E}_2 \\ \overline{E}_3 \end{bmatrix} \tag{13}$$

The index used in european standards to indicate the degree of unbalance is the *unbalance factor* (UF) [6] which is the ratio of the negative sequence module to the positive sequence module represented as (14).

$$UF\% = \frac{E_-}{E_+} \cdot 100 \tag{14}$$

I.3.3 Current Unbalance

In this section, an analysis of unbalance produced by a single phase railway substation is carried out. The aim is to find analytical expression describing the phenomenon.

Assomptions are:

- Sinusoidal steady-state
- Perfectly balanced three phase voltage supply
- No consideration on zero sequence is pointed out due to neutral wire absence.
- The substation is considered as current generator.
- Voltage drop on line impedances are neglected.

Referring to figure 12, line currents are reported in phasors domain (15). Substation current is $\overline{I_L} = I_L \angle \varphi_L$ with φ_L given respect to $\overline{V_{BC}}$. The decomposition in symmetrical components of currents drawn by the substation is performed by applying Fortescue transformation (16). The superscript "s" is used for "*substation*".

On this base, a single-phase substation connection draws currents with positive and negative components in opposition (Fig. 14). Let's point out that the positive component has a phase φ_L and the negative component has a phase $\pi - \varphi_L$.

$$\overline{I_A} = 0 \quad \overline{I_B} = \overline{I_L} \quad \overline{I_C} = -\overline{I_L} \tag{15}$$

$$\overline{I_+^s} = \frac{1}{3}(\overline{I_A} + \alpha \overline{I_B} + \alpha^2 \overline{I_C}) = \frac{1}{3}(\alpha - \alpha^2)\overline{I_L} = j\frac{\sqrt{3}}{3}\overline{I_L}$$

$$\overline{I_-^s} = \frac{1}{3}(\overline{I_A} + \alpha^2 \overline{I_B} + \alpha \overline{I_C}) = \frac{1}{3}(\alpha^2 - \alpha)\overline{I_L} = -j\frac{\sqrt{3}}{3}\overline{I_L} \tag{16}$$

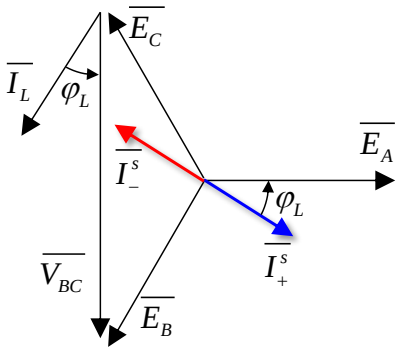


Fig. 14 - Symmetrical components of substation currents

I.3.4 Voltage Unbalance

To calculate the voltage unbalance produced at the PCC by the substation currents, we consider the equivalent circuits presented in figure 15. The positive component of the PCC voltages is considered as phase reference, as it is the only voltage available for measurements. The line impedance is noticed $\overline{Z_{CC}} = Z_{CC} \angle \varphi_{cc}$.

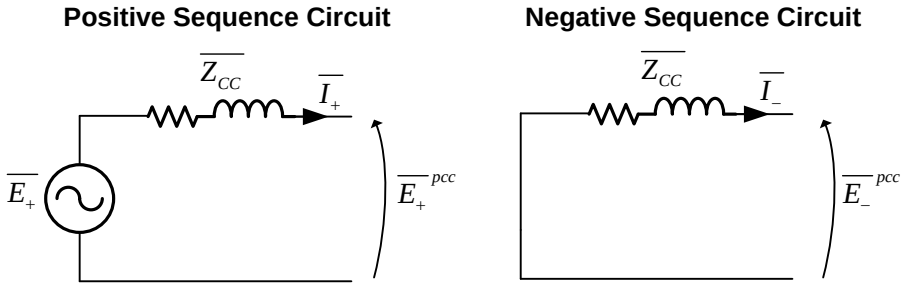


Fig. 15 - Equivalent Sequence Circuits

In order to evaluate UF resulting of the substation connection, magnitudes for positive and negative component of PCC voltages are needed. While the latter is directly expressed in (17), the calculation of the positive component requires some approximations. With reference to figure 16, reporting the vector diagram of the positive sequence circuit, $\overline{\Delta V}$ is approximated with its projection on real axis. Thus, the voltage positive component is given by relation (18), and the voltage unbalance at the PCC is expressed by (19).

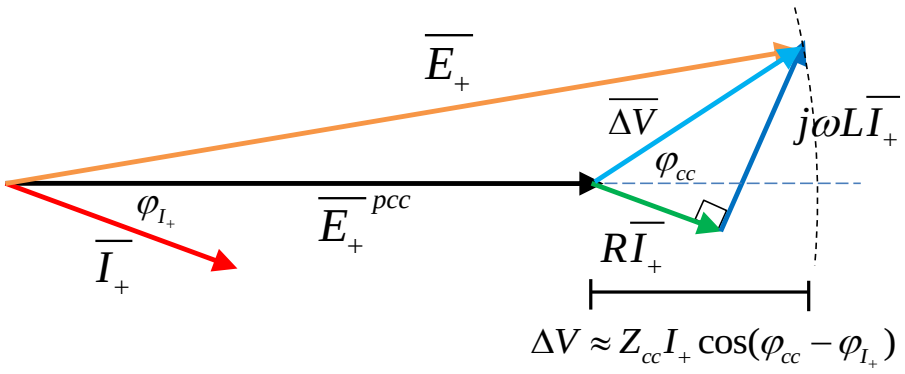


Fig. 16 - Positive Component vector diagram

$$E_-^{pcc} = Z_{CC} I_- = Z_{CC} \frac{\sqrt{3}}{3} I_L \tag{17}$$

$$E_+^{pcc} = \left|\overline{E_+} - \overline{\Delta V}\right| \approx E_+ - Z_{cc} I_+ \cos(\varphi_{cc} - \varphi_{I_+}) = E_+ - Z_{cc} \frac{\sqrt{3}}{3} I_L \cos(\varphi_{cc} - \varphi_{I_+}) \tag{18}$$

$$UF\% = \frac{E_-^{pcc}}{E_+^{pcc}} \cdot 100 = \frac{Z_{cc} I_-}{E_+ - Z_{cc} I_+ \cos(\varphi_{cc} - \varphi_{I_+})} \cdot 100 = \frac{Z_{cc} I_L}{\sqrt{3} E_+ - Z_{cc} I_L \cos(\varphi_{cc} - \varphi_L)} \cdot 100 \tag{19}$$

The qualitative approximation for the voltage unbalance given in (20), uses information on grid short-circuit power S_{cc} and load apparent power S_L, is always used.

$$UF\% = \frac{\frac{S_L}{S_{cc}}}{1 - \frac{S_L}{S_{cc}} \cos(\varphi_{cc} - \varphi_L)} \cdot 100 \approx \frac{S_L}{S_{cc}} \cdot 100 \tag{20}$$

I.3.5 Unbalance Compensators

In order to reduce the voltage unbalance, the unbalance compensator is connected as reported in figure 17. It reduces the negative component of line currents.

Actually two solution are commonly adopted. The first one is based on thyristors SVC while the second one is a VSI STATCOM based solution.

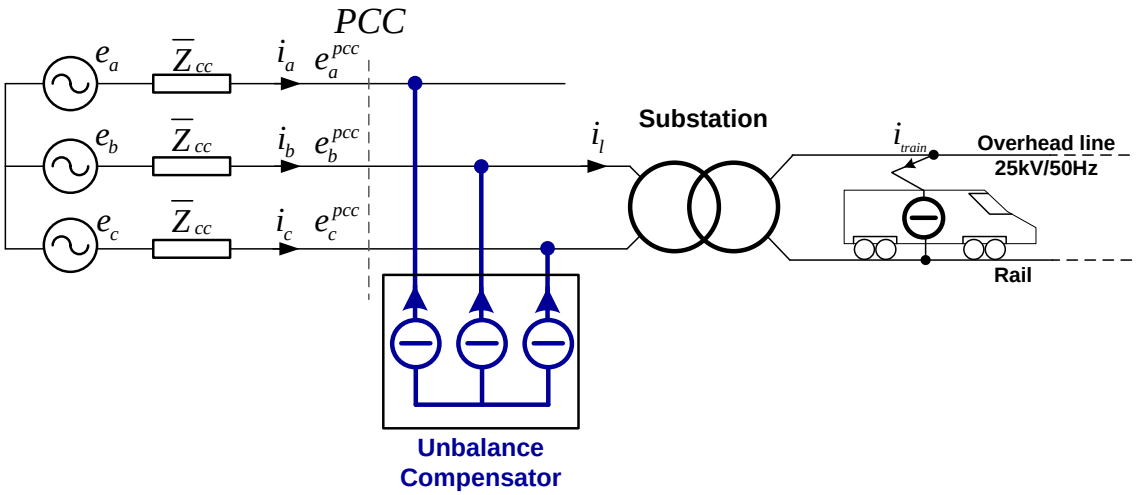


Fig. 17 - General Scheme for an unbalance compensator installation

I.3.5.1 Unbalance Compensation based on SVC

A load balancing using conventional SVC is obtained by control of reactive elements

[8]. In its simplest form the load balancer can be achieved with TCRs and fixed capacitor banks phase to phase connected as it is shown in figure 18.

The generation of low frequency current harmonics make this solution not really suitable for high power quality requirements. Thus, in order to suppress these harmonics, bulky additional filters have to be introduced.

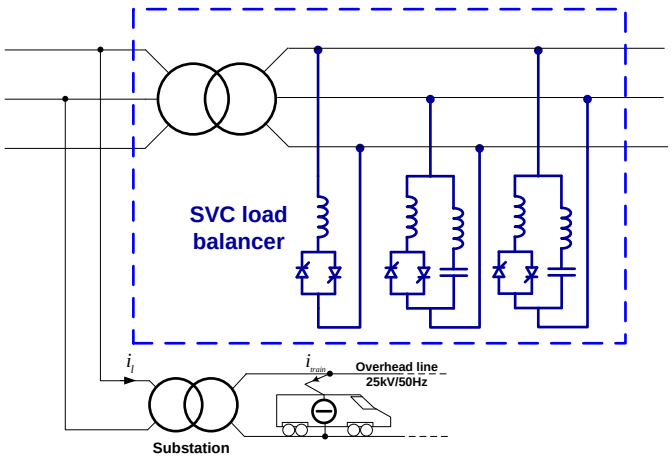


Fig. 18 – SVC Load balancer installation

I.3.5.2 Unbalance Compensation based on VSI STATCOM

In recent years, with increasing operating area of controllable semiconductors, shunt unbalance compensators, based on a VSI, are used in MVA range.

In such an application, the VSI operates as a current source injecting a negative component 180° phase-shifted respect to one generated by the single-phase load (Fig. 19).

This type of compensator is currently installed in the SNCF substation of Evron. Some pictures of this installation are reported in figure 20.

In the following study, a sinusoidal PWM is considered. With the aim of totally compensate the unbalance induced by the substation, the compensator is controlled in order to inject three currents [i_{fa} i_{fb} i_{fc}] forming a negative sequence $\overline{I_-^c}$ as (21). The superscript "*c*" refers to the "*compensator*".

$$\overline{I_-^c} = -\overline{I_-^s} = j\frac{\sqrt{3}}{3}\overline{I_L} \tag{21}$$

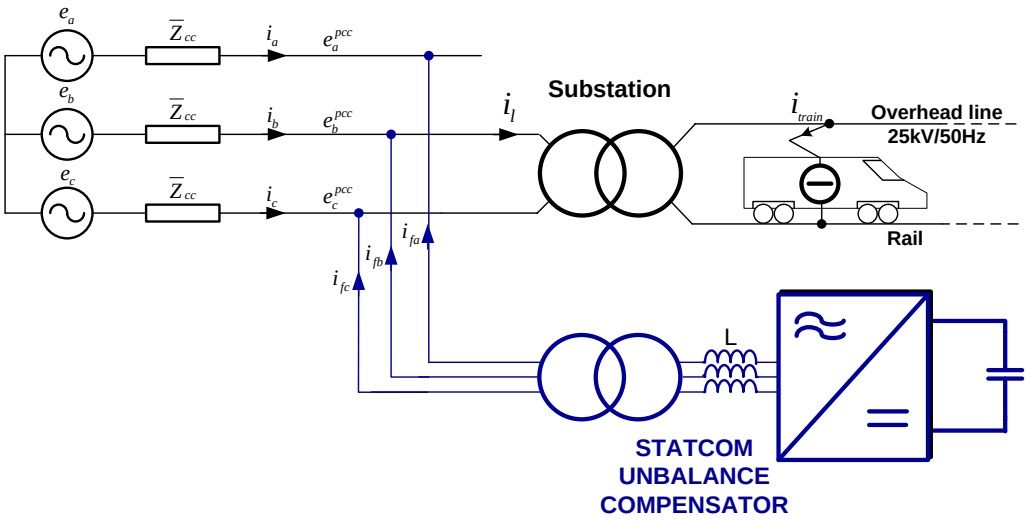


Fig. 19 - Unbalance Compensator based on VSI converter

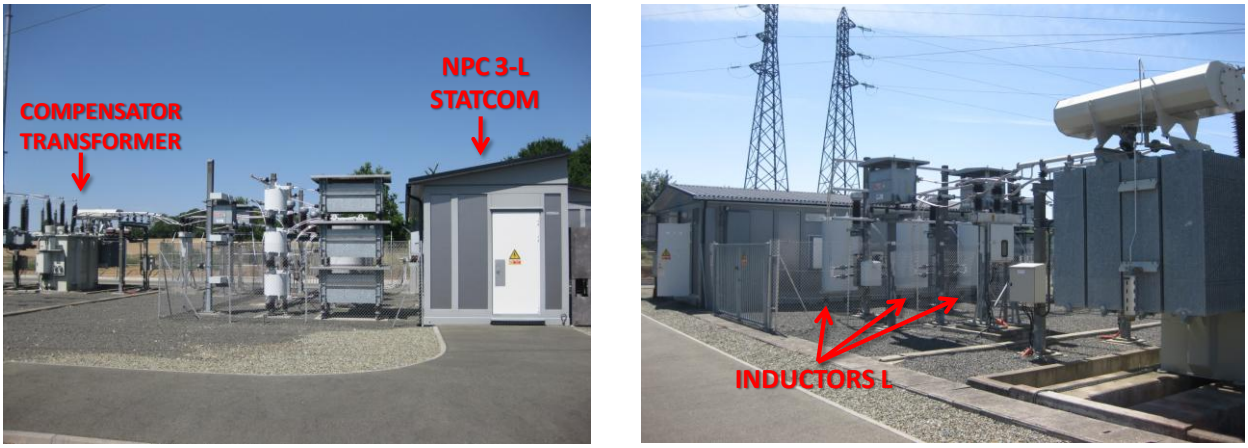


Fig. 20 - Evron Substation - STATCOM exterior photos.

I.3.5.2.1 Compensator Behaviour

In this section the functioning of a balancer based on a VSI converter is studied. The considered topologies are 2-Level and Neutral Point Clamped (NPC) 3-Level (Fig. 21).

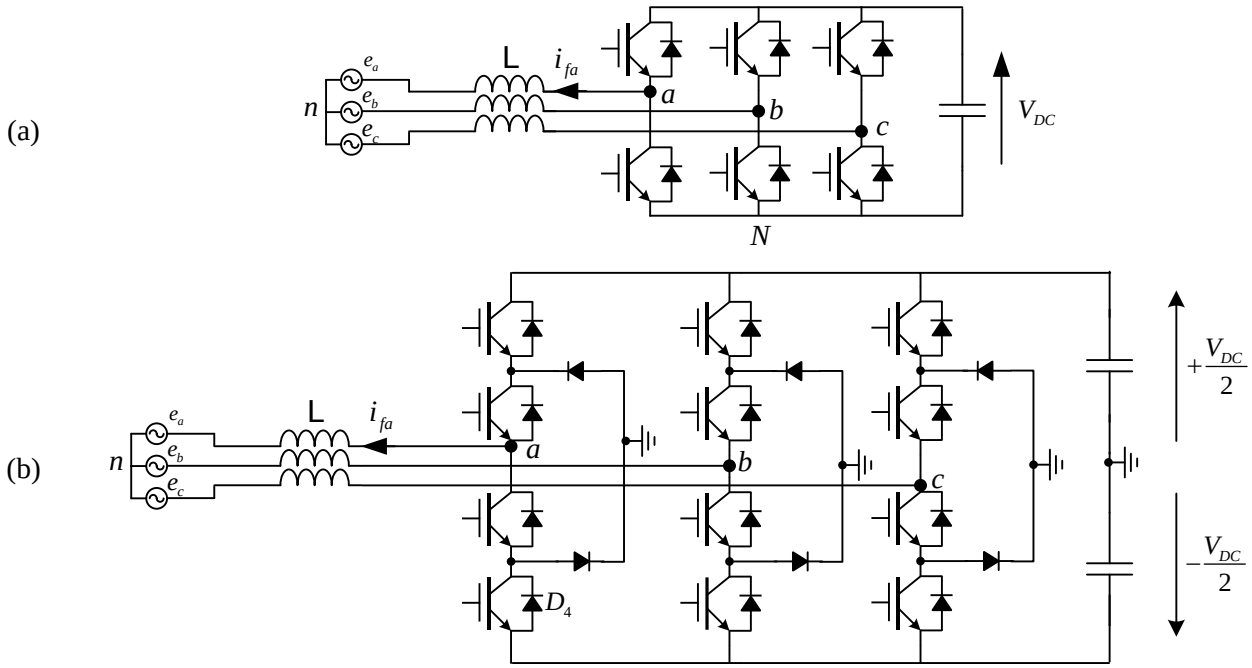


Fig. 21 – 3-phase 3-wire (a) 2-L converter, (b) NPC 3-L converter

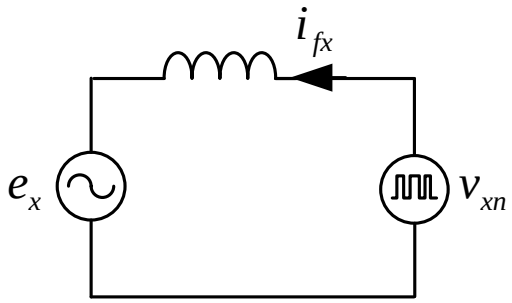


Fig. 22 - VSI single phase equivalent circuit

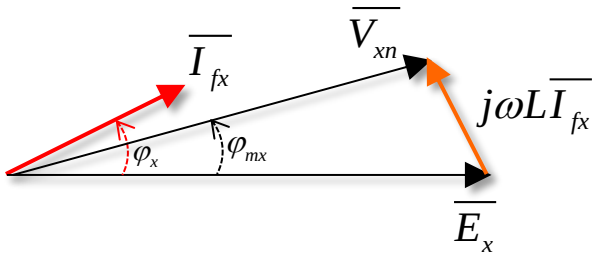


Fig. 23 - vector diagram for single phase equivalent circuit

An equivalent circuit for the generic phase *x* is reported in figure 22. Considering only fundamental values, the voltage imposed by the VSI converter is given by relation (22) where m is the modulation ratio varying sinusoidally (23).

$$v_{xn} = m_x \frac{V_{DC}}{2\sqrt{2}} \tag{22}$$

$$m_x = M_x \sin(\omega t + \varphi_{mx}) \tag{23}$$

On this hypothesis, if the phase reference is the line voltage, the injected line current is given by expression (24) derived from the vector diagram of figure 23.

$$\overline{I_{fx}} = \frac{\overline{M_x} V_{DC} / 2\sqrt{2} - E_x}{j\omega L} \tag{24}$$

I.3.5.2.2 Compensator design

Some consideration on the design criteria of inductor L and voltage V_{DC} are discussed below. Expression (25) is used for the maximum current ripple calculation. By choosing a maximum current ripple equal to 15% of the fundamental component, inductor value L is calculated according to relation (26)

$$\Delta i = \frac{V_{DC}}{8 \cdot L \cdot f_{sw}} \tag{25}$$

$$L \geq \frac{V_{DC}}{8 \cdot 0.15\sqrt{2}\, \mathrm{I}_{\max} \cdot f_{sw}} \tag{26}$$

In all cases, DC link voltage V_{DC} must be chosen higher than the input phase to phase voltage in order to guarantee the current controllability. As the compensator should be able to control a negative sequence with any phase, the design of the DC voltage is made referring to the worst case of 90° lagging current. The vector diagram in this condition is reported in figure 24.

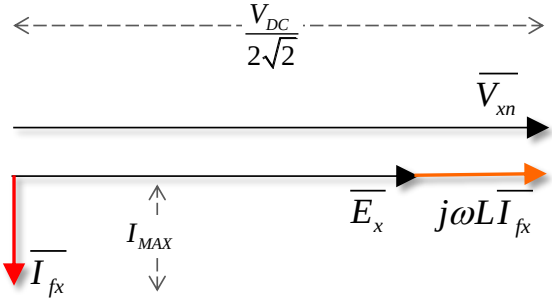


Fig. 24 – Vector diagram in case of 90° lagging current

If I_{max} is the maximum value of the fundamental current delivered by the converter, voltage V_{DC} must respect the constraint expressed in (27).

$$V_{DC} \geq 2\sqrt{2}(\omega L I_{\max} + E_x) \tag{27}$$

I.3.5.2.3 Current Unbalance compensation

If the compensator has to deliver a current with a negative component of magnitude I_- and phase φ_-, each leg produces an output voltage which is determined according to the vector diagram of figure 23. Assuming that the supply voltage is a purely a positive sequence of magnitude E_+, the following modulation index are needed :

$$\begin{aligned} m_a &= M_a \sin\left(\omega t + \arg\left(\overline{M_a}\right)\right) \\ m_b &= M_b \sin\left(\omega t + \arg\left(\overline{M_b}\right)\right) \\ m_c &= M_c \sin\left(\omega t + \arg\left(\overline{M_c}\right)\right) \end{aligned} \tag{28}$$

The magnitudes and phase displacements are then calculated from (29).

$$\begin{aligned} \overline{M_a} &= \left(j\omega L I_- e^{j\varphi_-} + E_+ \right) \frac{2\sqrt{2}}{V_{DC}} \\ \overline{M_b} &= \left(j\omega L I_- e^{j\left(\varphi_- + \frac{2\pi}{3}\right)} + E_+ e^{j\left(-\frac{2\pi}{3}\right)} \right) \frac{2\sqrt{2}}{V_{DC}} \\ \overline{M_c} &= \left(j\omega L I_- e^{j\left(\varphi_- - \frac{2\pi}{3}\right)} + E_+ e^{j\left(+\frac{2\pi}{3}\right)} \right) \frac{2\sqrt{2}}{V_{DC}} \end{aligned} \tag{29}$$

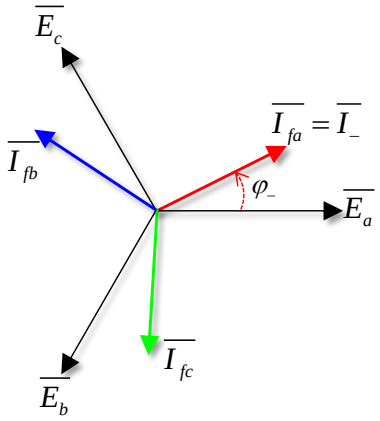


Fig. 25 - Three-phase current negative sequence

I.3.5.2.4 - Compensator Power Rating

The converter is sized in order to totally compensate the current unbalance produced by the substation. The following notations are used:

- S_L is the apparent power load considered as reference for sizing.
- S_c is the apparent power of the PWM converter.

Thus, relation (30) is obtained by multiplying equation (21) with $\sqrt{3}V$ on both sides. Then, it is evident that in order to compensate the current unbalance, the power size of the compensator must be the same of the substation.

$$S_c = S_L \tag{30}$$

The unbalance compensator based on a VSI allows a good current controllability as well as good power quality performance regarding injected currents. Nevertheless, this solution suffers of several drawbacks. In the next chapters it will be shown that bulky capacitors are needed on the DC-link in order to limit the voltage ripple due to power fluctuation derived from negative current sequence. Moreover, it will be shown that the high power losses in semiconductor devices, makes this solution very costly in terms of operation and maintenance.

I.4 Conclusions

Employing power converters in 25kV/50Hz substations allow the railways operator to avoid onerous modifications to the railways infrastructure.

Installation of variable reactive power compensators allows guaranteeing an appropriate overhead line voltage level for locomotives operation (voltage booster) and the penalties imposed by the energy providers in case of low power factor can be avoided.

Unbalance compensators allow to enhance the substation traffic without exceeding the limit imposed on the unbalance factor, thus avoiding the building of new transmission lines to increase the short-circuit power.

This chapter described classical solutions currently used by the French Railway Company. In the next chapters, new topologies are proposed and a special attention is paid to reduce the size of reactive elements and the semiconductor losses. Especially the last one has to be taken into consideration by the railways operator, as it determines a significant growth of costs both in terms of active energy and cooling system maintenance.

Chapter II. **Chopper Controlled Impedance (CCI) concept**

The purpose of this chapter is the introduction of the concept of *Chopper Controlled Impedance (CCI)*. Single phase PWM AC Choppers are used to achieve controlled impedances (capacitive or inductive) at the fundamental frequency. This concept is applied in medium or high power applications and multi-converter structures based on step down or step up AC choppers are proposed.

II.1 Direct AC/AC Conversion with PWM AC Choppers

II.1.1 Introduction

Various converter topologies can be applied to provide AC/AC conversion. Based on the number of conversion stages, they can be classified as either *Direct* or *Indirect* AC/AC converters [9].

Indirect converters use (at least) two conversion stages and an intermediate DC (or much more rarely, AC) link consisting of reactive elements.

On the other hand, Direct converters provide a direct link between the source and the load without additional storage elements but the input and output frequencies are closely related. Nevertheless, passive filters are always required to filter out the high-frequency harmonics introduced at the input and output sides by the converter switching operation.

Among the AC/AC direct converters, Cycloconverters and Matrix converters [10][11] are distinguished by their ability to adjust the output frequency and voltage of a specific AC input voltage source. They also provide bi-directional power transfer capabilities, allowing the use of active loads (e.g. motors in regenerative mode).

On the other hand, the AC Chopper topology, which is quite similar to the well known DC chopper, provides direct AC/AC conversion between two AC sources at the same fundamental frequency (Fig. 26). The AC Chopper may be considered as an autotransformer whose turns-ratio can be electronically controlled. Nevertheless, although it can provide instantaneous bi-directional power transfer, it allows power flow in one direction only according to the type of load. AC Choppers are normally designed to transfer power between a fixed AC voltage source (e.g. the utility grid) and a passive AC load. The load voltage (i.e.

its RMS value) can be adjusted via the duty cycle, α, to control the power flow but the power exchange (either active or reactive) is determined purely by the load type (resistive, capacitive or inductive).

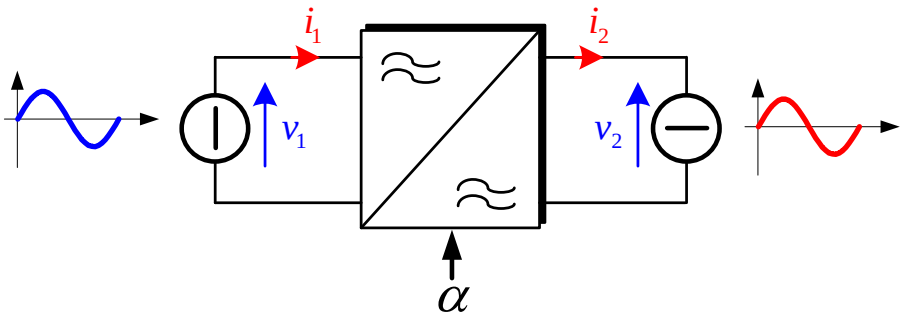


Fig. 26 - Principle of direct AC/AC conversion

II.1.2 Overview of single-phase PWM AC Choppers Topologies

The direct AC/AC conversion concept is not new. Line commutated thyristor-based AC/AC Converters are widely used in AC power control applications such as industrial heating, lighting control, soft starting and speed controllers for induction motors, power conditioning etc. In these applications, the load voltage is controlled by the thyristors firing angle, producing a lagging power factor and significant current harmonics on the supply and corresponding current and voltage harmonics at the output.

The use of PWM (pattern generation) was considered to be a solution for improving the input power factor and eliminating specific current harmonics of thyristor-based AC/AC Converters, leading to the introduction of step-down PWM AC Choppers (Fig. 27) [12][13]. This topology is derived from the classical step-down PWM DC chopper, where the two-quadrant semiconductors (unidirectional voltage and current) are replaced by-four quadrant turn-off semiconductors (bidirectional voltage and current).

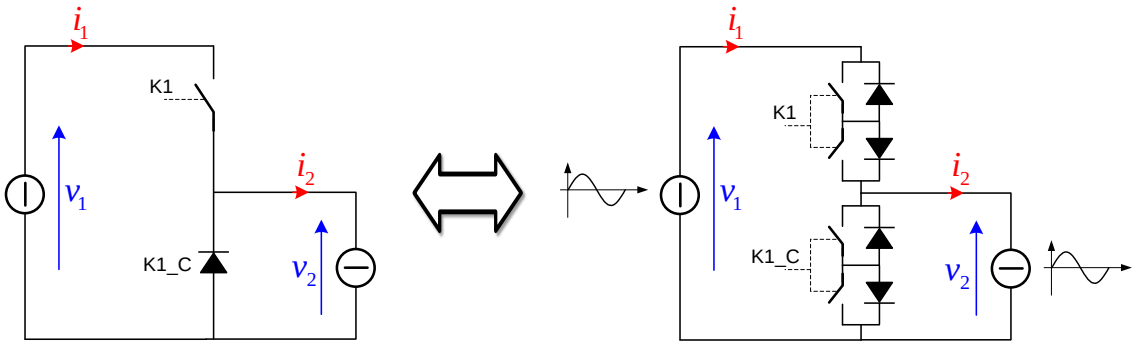


Fig. 27 - Single-phase step-down PWM AC Chopper (right) derived from the step-down DC-chopper (left)

In figure 28, the output voltage v_2 is simply adjusted by alternating the two semiconductors' states: during the active phase, the input voltage is applied to the load, and during the freewheeling phase a short-circuit path is provided for the load current. However, the practical application of this solution is limited by certain technical drawbacks. The most significant problems are due to the need for bulky snubber circuits to provide safe switching conditions for the four-quadrant semiconductors.

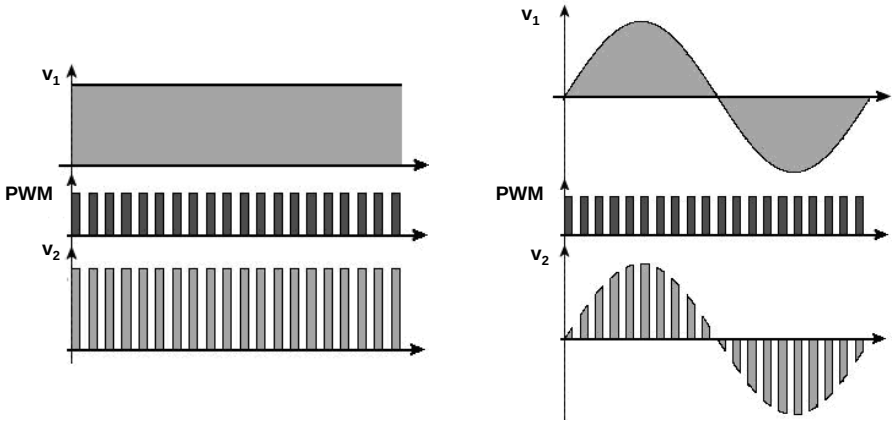


Fig. 28 - DC Chopper output voltage waveforms (left) and single-phase PWM AC Chopper output voltage waveforms (right) at constant duty cycle

A novel PWM AC Chopper topology, using three-quadrant classical switches (bidirectional current - unidirectional voltage, as used in voltage source inverters), has been introduced [14]. The main originality of this conversion structure (Fig. 29) lies in the differential connection of the voltage source v_1 between the two commutation cells.

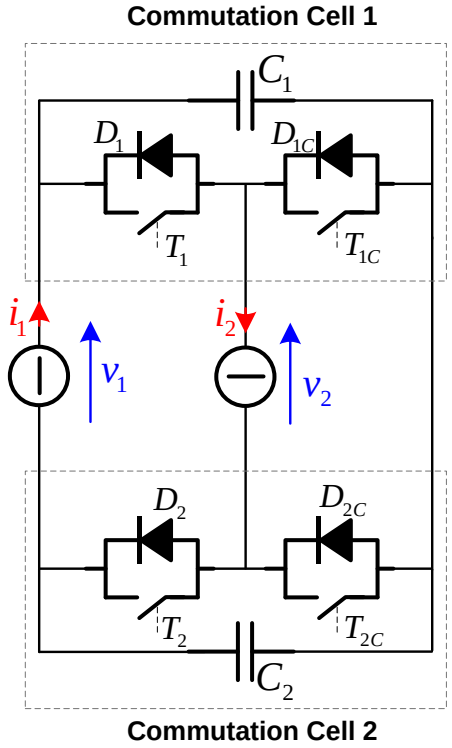
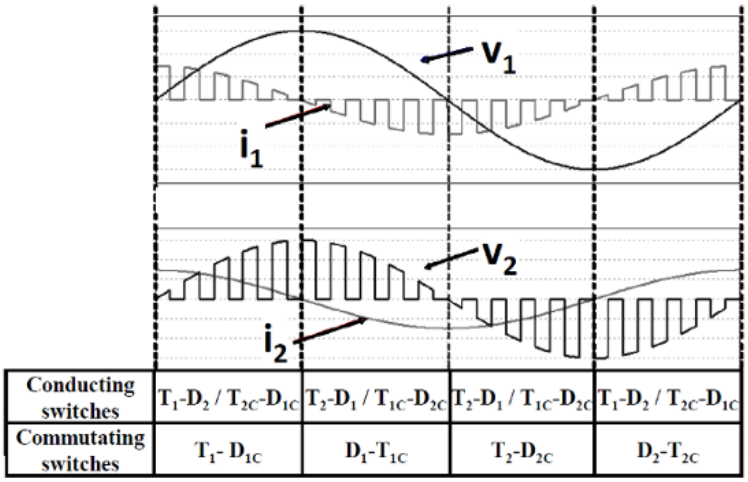


Fig. 29 -AC Chopper topology based on the differential association of two commutation cells

Assuming the ideal waveforms presented in figure 30 (sinusoidal input voltage and sinusoidal output current), the operation of the circuit is as follows:

- When input voltage v_1 is positive, Commutation Cell 1 is switched and T_2 and T_{2C} are always ON
- When input voltage v_1 is negative, Commutation Cell 2 is switched and T_1 and T_{1C} are always ON.



Conducting switches	T_1-D_2 / T_{2C}-D_{1C}	T_2-D_1 / T_{1C}-D_{2C}	T_2-D_1 / T_{1C}-D_{2C}	T_1-D_2 / T_{2C}-D_{1C}
Commutating switches	T_1- D_{1C}	D_1-T_{1C}	T_2-D_{2C}	D_2-T_{2C}

Fig. 30 - AC Chopper based on association of two commutation cells, current and voltage waveforms for duty cycle α = 0.5.

In the example of figure 30, the waveforms are given for the case of a 90° leading current and the corresponding conduction sequences of each device are listed below the waveforms as determined by the polarity of i_2. The switching commutation cell is selected as a function of the polarity of input voltage v_1. The principle of the PWM modulator is illustrated in figure 31.

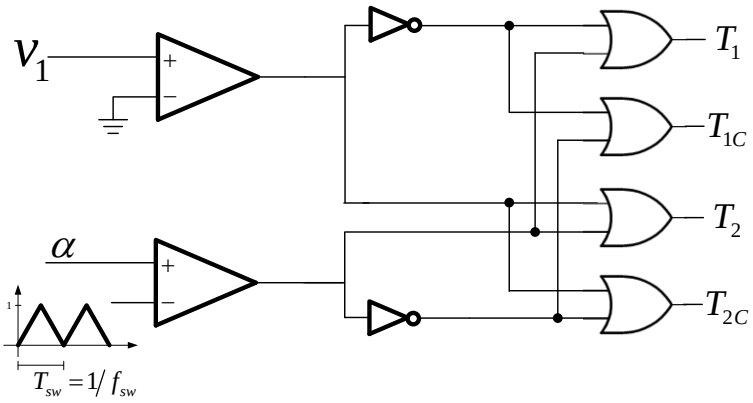


Fig. 31 - AC Chopper PWM modulator

It can be seen from the table of states below the waveforms that each semiconductor conducts during half of the network period and switches during a quarter of the network period. It can be easily demonstrated that the RMS value of the output voltage fundamental V_2 depends on input voltage RMS value V_1 and can be adjusted with the duty cycle α:

$$V_2 = \alpha V_1 \qquad (31)$$

Likewise, the relationship between current RMS values is given by:

$$I_1 = \alpha I_2 \qquad (32)$$

Since all the controlled semiconductors can be off either when the input voltage is close to zero and/or during the switching cell dead-times, the output current is conducted through the freewheeling diodes and the capacitors.

In some applications, for safety reasons, the neutral point of the load must be permanently connected to the input neutral point. To this effect, a non-differential PWM AC Chopper structure, using two imbricated cells was proposed in 1999 [15]. This topology, presented in figure 32, offers the same general behavior as the differential structure (Fig. 29) but requires only one decoupling capacitor: voltage source v_1 being considered as perfect.

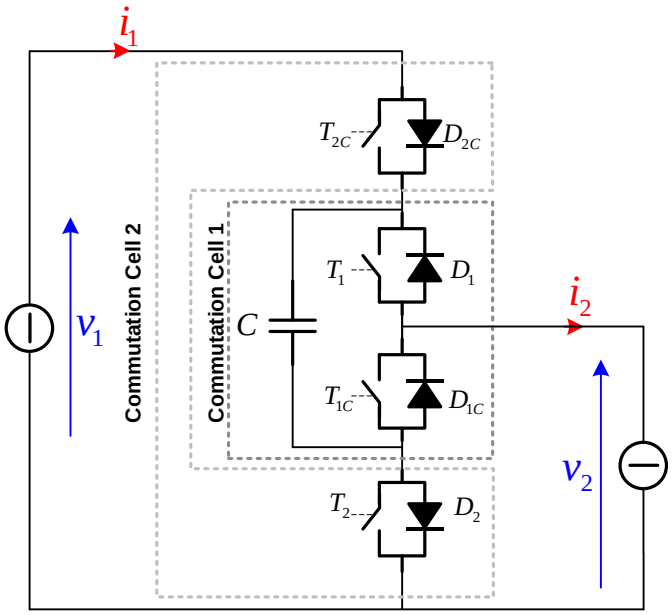


Fig. 32 - AC Chopper topology based on two imbricated commutation cells.

II.2 Practical applications of single-phase AC Choppers

II.2.1 Step-down or step-up AC Chopper

By considering the ideal waveforms presented in figure 30, it is clear that the AC chopper topology requires input and output filtering elements. Anyway, capacitor C_F and inductor L_F will be designed to filter out the switching frequency from i_1 and v_2. Thus, as shown in figures 33 and 34, the AC Chopper can be used as a step-down or as a step-up converter depending on the connection of the network and the load.

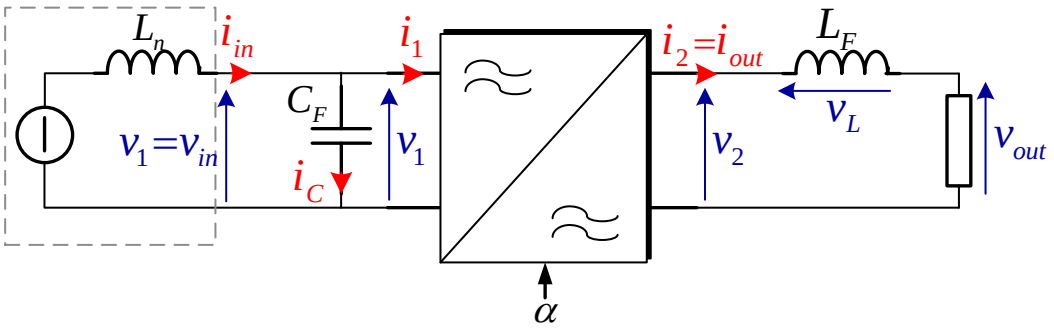


Fig. 33 - AC/AC step-down converter

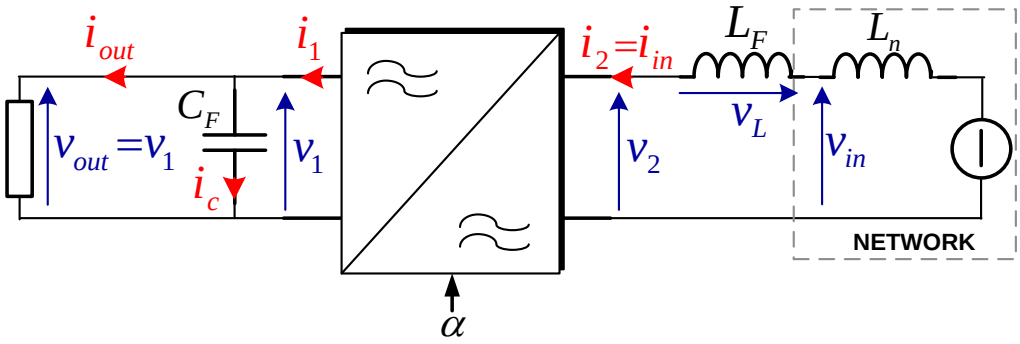


Fig. 34 - AC/AC step up converter

II.2.2 Concept of controlled impedance

Assuming a sufficiently high switching frequency f_{sw}, the filtering elements L_F and C_F can be chosen to have a negligible influence at the network frequency f_n. Then, in terms of fundamental RMS values and relationships of input and output (33),(34) the structures behave as variable impedances controlled by the duty cycle α (Table I).

	AC/AC step down converter	AC/AC step up converter
Input impedance (at f_n)	$Z_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{Z_{out}}{\alpha^2}$ (33)	$Z_{in} \approx \frac{V_{in}}{I_{in}} \approx Z_{out}\alpha^2$ (34)

Table I - AC/AC conversion – Input impedance at fundamental frequency f_n

II.2.3 Active voltage divider

Logically, an impedance can be series-connected to the AC/AC Chopper with the view of forming a voltage divider dependent on α [16]. On the basis of Table I, the averaged models using RMS complex values are given in figures 35ù and 36. They represent the circuit behavior at fundamental frequency when filtering elements are neglected ($V_L \approx 0$; $I_C \approx 0$).

The impedance connected in series with the AC Chopper has the same characteristics at fundamental frequency as the output impedance times a factor q ($\overline{Z} = q \cdot \overline{Z_{out}}$).

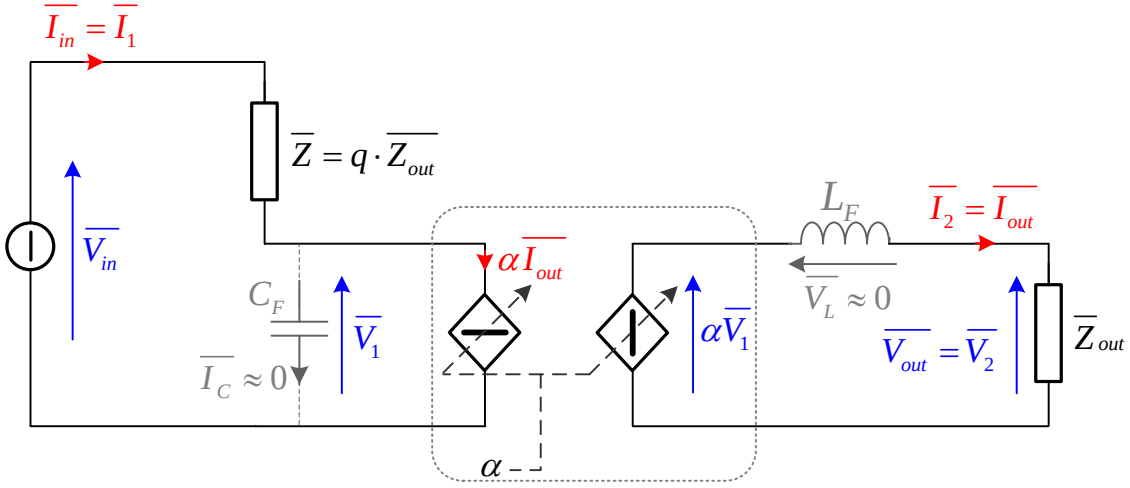


Fig. 35 - Averaged Model for AC/AC conversion with voltage divider and step-down chopper

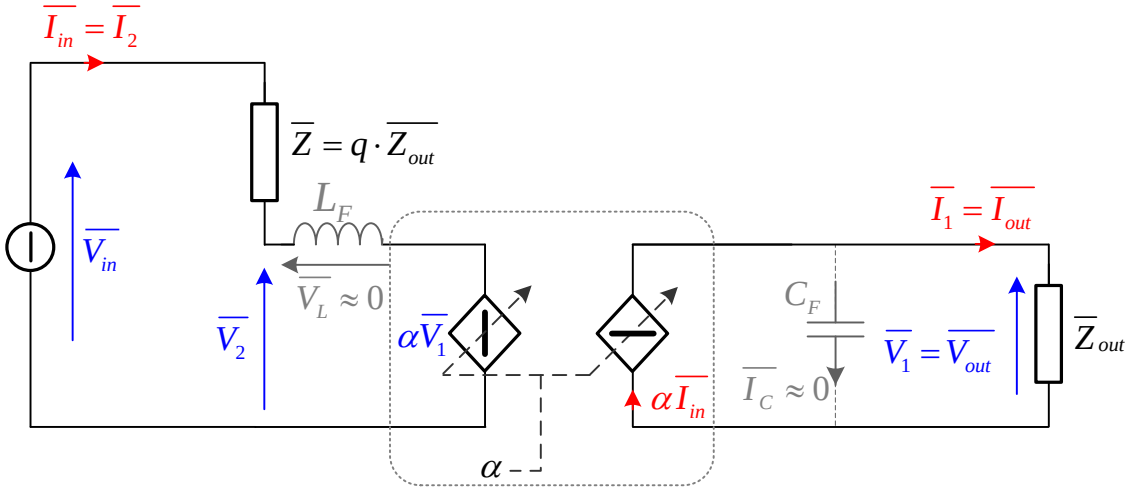


Fig. 36 - Averaged Model for AC/AC conversion with voltage divider and step-up chopper

Compared to the single impedance configurations of figures 33 and 34 the voltage divider has the additional advantage of reduce switching stress on the semiconductors. In effect, voltage v_1 and current i_2 cannot be simultaneously at their maxima and thus switching losses are reduced. We can define an *Apparent Design Power* for the AC Chopper which accounts for this, in equation (35):

$$S_{conv} = V_1 I_2 \tag{35}$$

The main relationships are given in Table II and figures 37 to 39 illustrate the advantage of the active voltage divider in terms of the apparent power rating of the converter.

	Step down Converter	**Step up Converter**
Input Impedance	$\overline{Z_{in}} = \overline{Z_{out}}\left(\frac{1+q\alpha^2}{\alpha^2}\right)$ (36)	$\overline{Z_{in}} = \overline{Z_{out}}\left(\alpha^2+q\right)$ (37)
Maximum Input Apparent Power	$S_{\max} = \frac{V_{in}^{\ 2}}{Z_{out}}\frac{1}{1+q}$ (38)	$S_{\max} = \frac{V_{in}^{\ 2}}{Z_{out}}\frac{1}{q}$ (39)
Minimum Input Apparent Power	$S_{\min} = 0$ (40)	$S_{\min} = \frac{V_{in}^{\ 2}}{Z_{out}}\frac{1}{1+q}$ (41)
Voltage V_1	$\overline{V_1} = \overline{V_{in}}\frac{1}{1+q\alpha^2}$ (42)	$\overline{V_1} = \overline{V_{in}}\frac{\alpha}{\alpha^2+q}$ (43)
Current I_2	$\overline{I_2} = \frac{\overline{V_{in}}}{\overline{Z_{out}}}\frac{\alpha}{1+q\alpha^2}$ (44)	$\overline{I_2} = \frac{\overline{V_{in}}}{\overline{Z_{out}}\left(\alpha^2+q\right)}$ (45)
Dimensioning Apparent Power	$S_{conv} = \frac{V_{in}^{\ 2}}{Z_{out}}\frac{\alpha}{\left(1+q\alpha^2\right)^2}$ (46)	$S_{conv} = \frac{V_{in}^{\ 2}}{Z_{out}}\frac{\alpha}{\left(\alpha^2+q\right)^2}$ (47)

Table II - AC/AC conversion with Active Voltage Divider - Relationships at fundamental frequency f_n

For the step-down structure, it can be demonstrated that ratio S_{conv}/S_{max} is at a minimum when q = 1 (this ratio is equal to 0.65 for α = 0.57). In figure 38 (q >1), it should be noticed that the RMS value of output current I_2 can be greater than the maximum RMS value of input current I_{in} which adversely affects semiconductor conduction and switching losses.

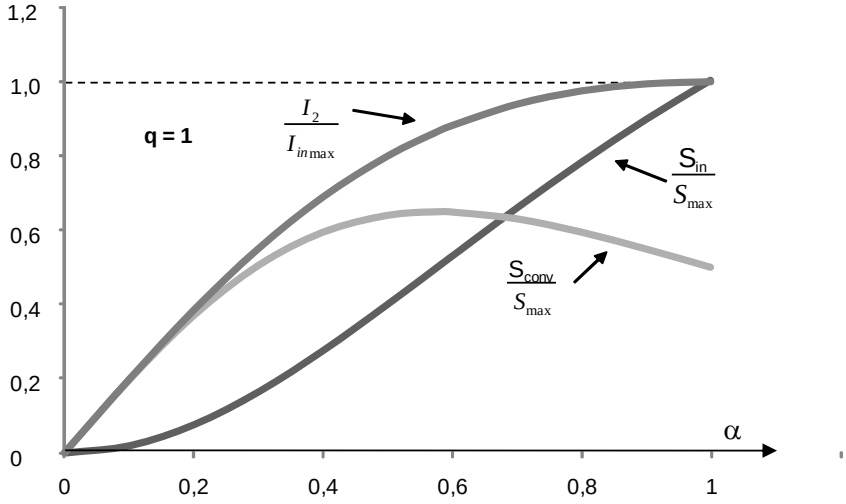


Fig. 37 - Active voltage divider with step-down AC Chopper (q = 1)

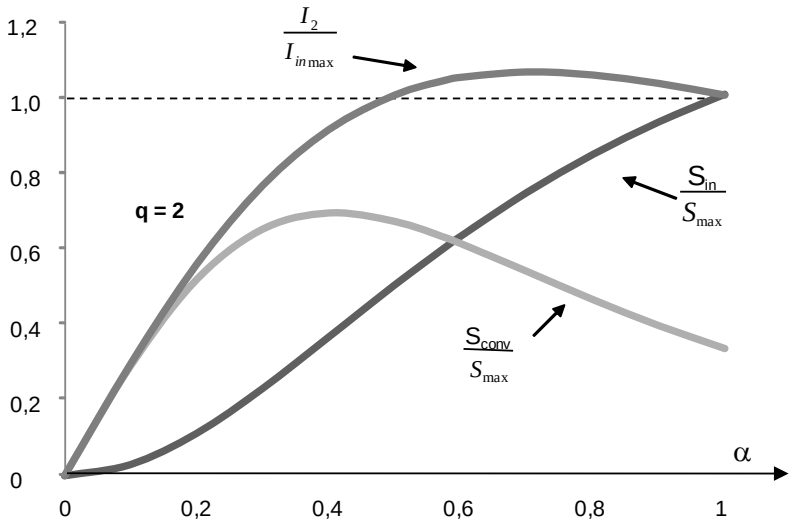


Fig. 38 - Active voltage divider with step-down AC Chopper (q = 2)

For the structure based on the step-up AC chopper, the apparent power is controlled between a minimum and a maximum value. In practice, the value of q will be chosen as a function of the application and the range of controllable apparent power.

In the case of q < 3, it can be demonstrated that ratio S_{conv}/S_{max} shows a maximum value for α < 1:

$$\alpha = \sqrt{\frac{q}{3}} \tag{48}$$

$$\frac{S_{conv_\max}}{S_{\max}} = \frac{3\sqrt{3}}{16\sqrt{q}} \tag{49}$$

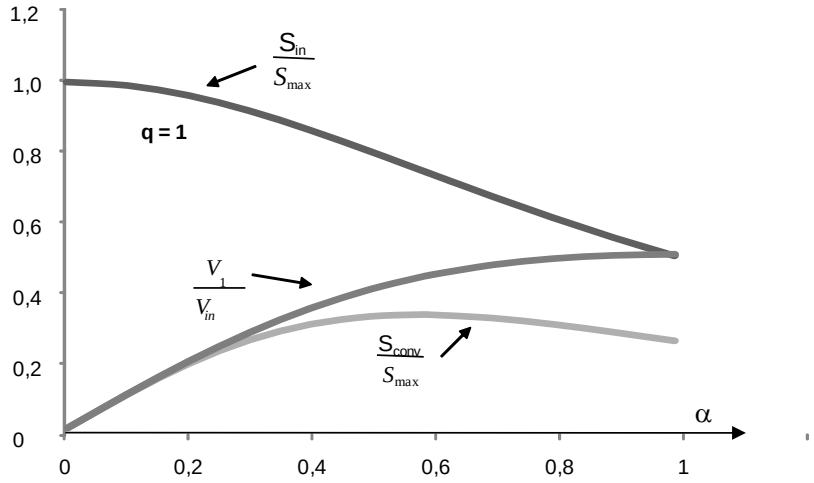


Fig. 39 - Active voltage divider with step-up AC Chopper (q = 1)

If q > 3, the Design Apparent Power of the step-up AC chopper is maximal for $\alpha = 1$ and given by Equation (50).

$$\frac{S_{conv_\max}}{S_{\max}} = \frac{q}{(1+q)^2} \tag{50}$$

II.3 Application of the controlled impedance concept

The concept of controlled impedance can be applied in reactive power control and voltage unbalance compensation. In fact, as described in the first chapter, in both applications it is possible to use TCR structures to regulate the reactive power and for load balancing. The CCI is based on the same principle of the TCR. In both, a controlled reactive element is achieved by means of switching devices.

However, compared to a TCR solution, the AC chopper does not generate any low-order harmonics thanks to its PWM operation. Nevertheless, to avoid over-voltages, it is necessary to choose the filtering elements with regard to pre-existing harmonics in the network.

II.3.1 Choice of the structure

As previously shown, the input impedance of the proposed structure can be controlled by the duty cycle of the AC Chopper. Nevertheless, at fundamental frequency, the behavior of the input impedance is defined by the choice of Z_{out}. If leading reactive power is required, Z_{out} should be a capacitive load at network frequency and in the case of a lagging reactive power, Z_{out} should be an inductive load at network frequency.

For medium and high power applications, multi-converter structures are required to share voltage or current between elementary AC Choppers. For example, figures 40 and 42 show possible arrangements for

leading and lagging reactive power compensation. In both cases, the PWM patterns of the AC choppers are interleaved, thus reducing the size of filtering elements (L_F or C_F).

In the circuit presented in figure 40, input current i_{in} is drawn with a multilevel waveform and apparent switching frequency f_a equal to $N.f_{sw}$. (An example of such a waveform is given in figure 41 for N = 3). The value of capacitor C_F will be calculated to filter the apparent switching frequency and to obtain a quasi sinusoidal waveform for v_1.

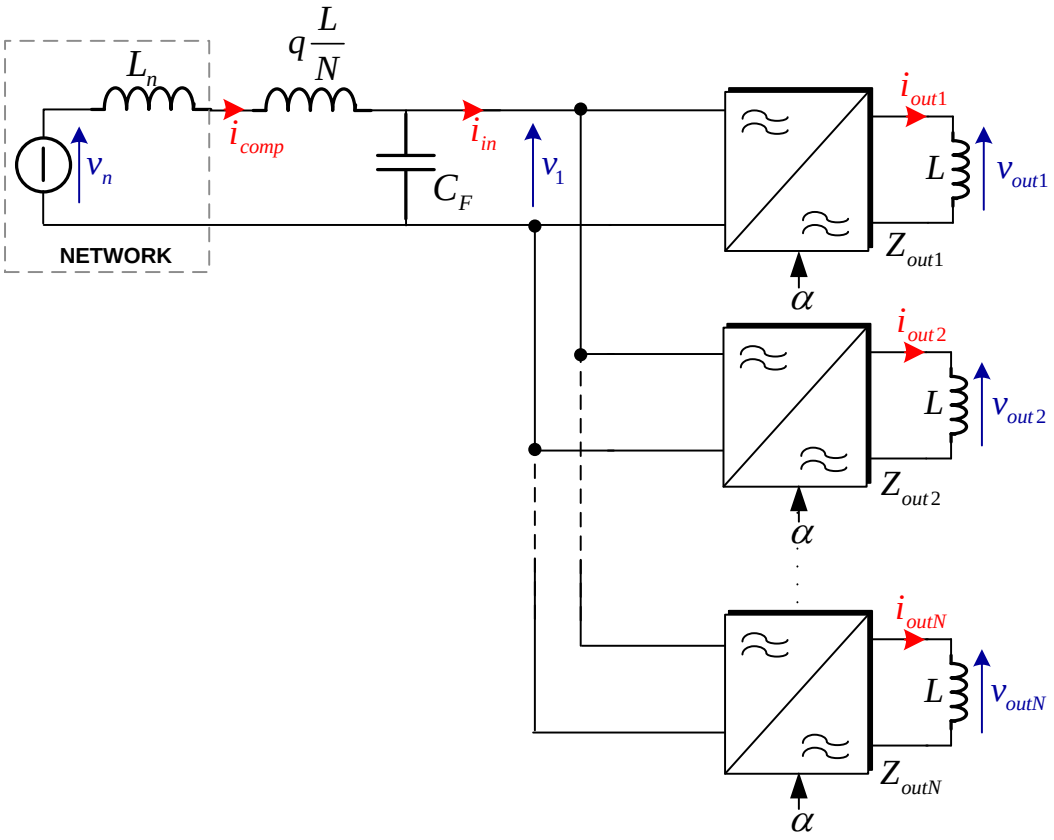


Fig. 40 - Active impedance with step-down AC choppers for lagging reactive power control

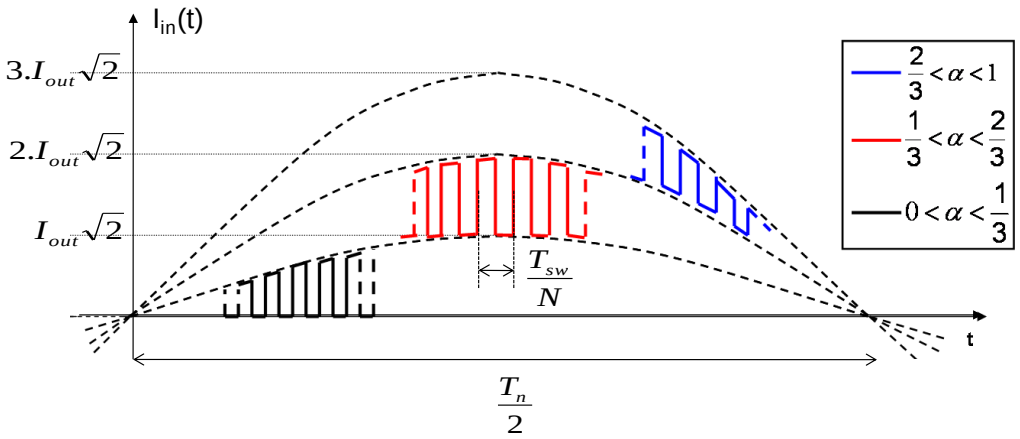


Fig. 41 - Interleaved step-down AC choppers - Input current multilevel waveform for N = 3

Similarly, for the structure presented in figure 42, voltage v will also show a multilevel waveform (Fig. 43) with apparent switching frequency f_a equal to $N.f_{sw}$. The value of inductor L_F will be calculated to filter the apparent switching frequency and obtain a quasi sinusoidal waveform for i_{in}. Moreover, the serial association of converters allows transformerless connection to a medium voltage network.

Special attention must be paid to potential resonance of the filtering elements (L_F or C_F). It is therefore mandatory to know the existing low frequency harmonics on the power network and to adjust the filter elements in order to avoid such resonances leading to over-current or over-voltage in the circuit.

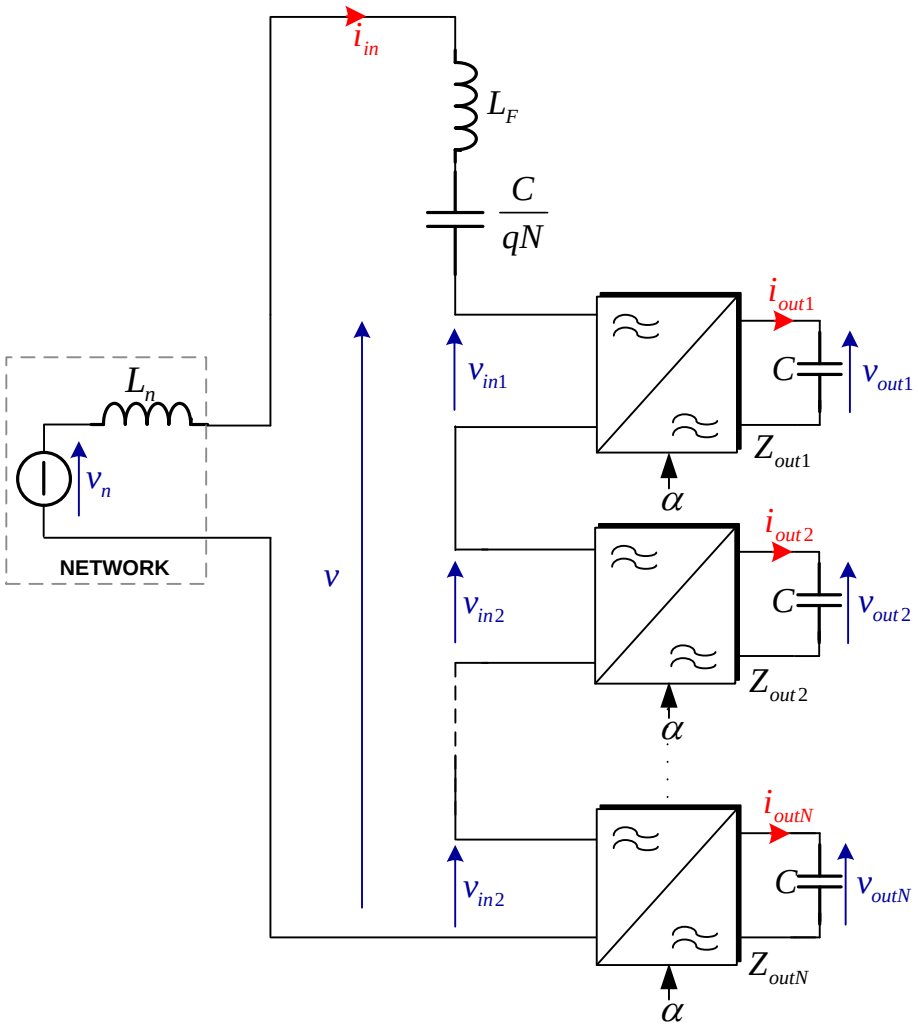


Fig. 42 - Controlled impedance with step-up AC Choppers for leading reactive power control

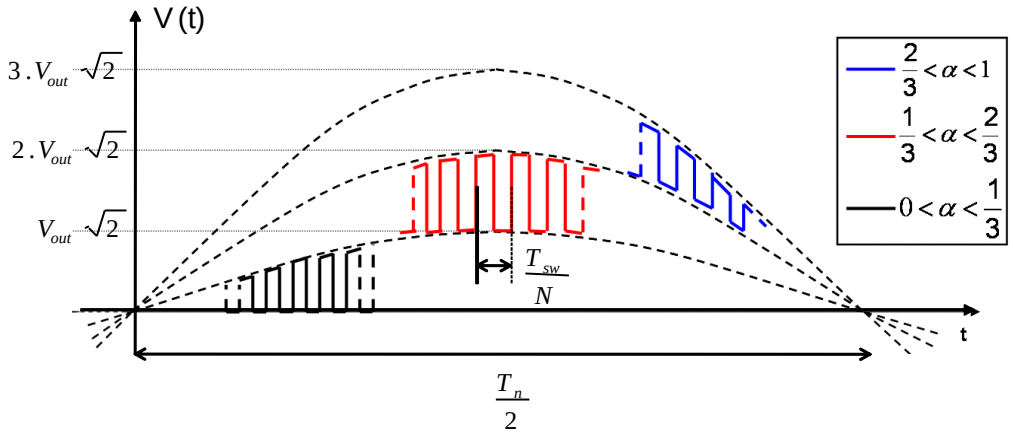


Fig. 43 - - Interleaved step-up AC choppers - voltage multilevel waveform for N = 3

II.4 Conclusions

The concept of Chopper Controlled Impedance was proposed. Variable capacitive and inductive impedances at the fundamental frequency are achieved employing AC-Chopper converter.

Compared to a TCR solution, the AC chopper does not generate any low-order harmonics thanks to its PWM operation. Nevertheless, to avoid over-voltages, it is necessary to choose the filtering elements with regard to pre-existing harmonics in the network.

In the next chapters, the concept is applied in Reactive Power compensation and Voltage Unbalance mitigation. The proposed solution is characterized by low power losses in semiconductor devices and low reactive elements size if compared with classical solutions.

Chapter III. **Reactive power compensation based on CCI**

In most cases, reactive power compensation in railways is realised by connecting shunt capacitive filters to the substation. This solution is very straightforward and economical but is unsuitable for large reactive power fluctuations, a fact which has led the French National Railways (SNCF) to investigate active solutions.

Various works [17][18][19] have demonstrated that CCI conversion structures have lower losses than VSIs in reactive power compensation. Moreover, single-phase VSIs require bulky capacitors on the DC bus, which is not the case with AC chopper-based solutions, a fact which makes them very attractive in high-power single-phase systems such as railway networks.

This chapter presents the design of a new topology based on the new chopper controlled impedance (CCI) and investigate its impact on a substation, focusing on harmonic interactions with locomotives. Two different converter topologies and equivalent models are presented. Current measurements carried out in an SNCF substation and their harmonic analyses are reported, and the frequency response of a substation incorporating the proposed compensator is studied. Additionally, simulations using the real current waveforms from the measurements are performed to replicate the CCI's performance in the substation and confirm its theory of operation. Finally, experimental results, achieved on a 1.2-MVAR prototype, are presented.

III.1 Introduction

In chapter II, variable impedances were achieved by means of a CCI structure, employing PWM AC-chopper converters.

The input impedance expressions for step-down and step-up configurations are given by (33) and (34), respectively. If impedance Z_{out} is capacitive at the grid frequency, the converters act as variable capacitors. Thus, a reactive power compensator can be implemented using the controlled impedance concept. The supplied reactive power can be expressed as shown in (51) for the step-down mode and (52) for the step-up mode.

$$Q = \frac{V_{in}^{\ 2}}{Z_{out}}\alpha^2 \tag{51}$$

$$Q = \frac{V_{in}^{\ 2}}{\alpha^2 Z_{out}} \tag{52}$$

It should be noted that, in the first case, increasing the duty cycle increases the provided reactive power. On the other hand, in the case of a step-up configuration, increasing the duty cycle decreases the reactive power provided by the converter.

III.2 Case study–Revest substation

The considered case study is that of a substation located at *Revest* in the north of Paris close to the largest railway station in Europe, *Gare du Nord*.

Current and voltage measurements were carried out there, and the data were used in the compensator design.

The electrical circuit of the *Revest* substation is shown in figure 44. This substation is equipped with a 60-MVA single-phase transformer, the primary side of which is line-to-line connected to the 225 kV/50 Hz grid. It includes two fixed compensation banks (5.5 MVAR and 7.5 MVAR) tuned to 120 Hz and connected between the overhead line and rail.

III.2.1 Current and voltage measurements

Substation output current and overhead-line voltage measurements were carried out during 18 hours from 04:00 p.m. to 10:00 a.m. with a 5-kHz sampling frequency (figure 45). During the recording, the 5.5-MVAR compensation bank was disconnected.

Two phases could be distinguished:

- *Phase 1*: measurement without fixed compensation banks from 04:00 p.m. to 08:00 p.m.

- *Phase 2*: measurement with the 7.5-MVAR fixed compensation bank connected from 08:00 p.m. to 10:00 a.m.

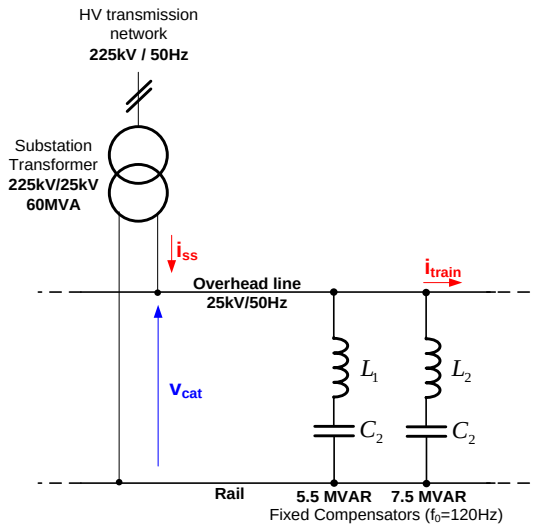


Fig. 44 - *Revest* substation equivalent circuit.

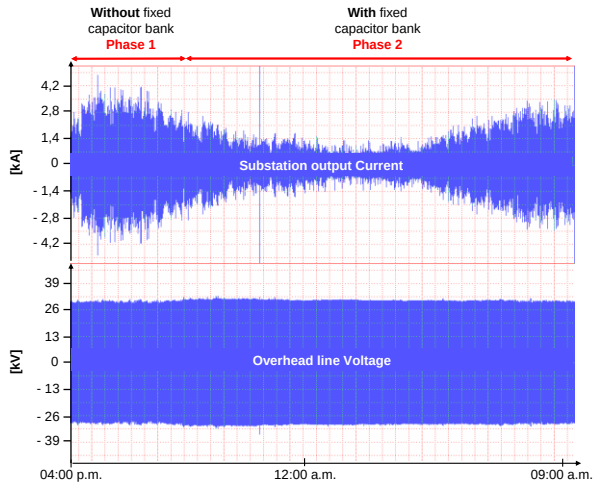


Fig. 45 – Substation output current and overhead line voltage measurements.

III.2.2 Current analysis

A spectral analysis of the output substation current was performed. The development in a Fourier series is

given by:

$$i_{sub}(t) = \sum_{n=1}^{\infty} \left[a_i(n) \cos(2\pi n \omega_{net} t) + b_i(n) \sin(2\pi n \omega_{net} t) \right] \quad \textbf{(53)}$$

with a_i, b_i: Fourier coefficients

n: the rank of the current harmonic.

A discrete Fourier transform algorithm is used to calculate coefficients a_i and b_i at each network period. Thus, the amplitude of the current harmonics can be determined.

$$\hat{I}_{sub}(n) = \sqrt{a_i(n)^2 + b_i(n)^2} \quad (54)$$

The amplitudes of the harmonics (rank 1 to rank 11) calculated during 18 hours are shown in figure 46.

It can be seen that the amplitudes are the highest during rush hours, i.e. in the afternoon and morning. The calculations also show that the substation is always loaded and the current harmonics are quite high during low traffic times.

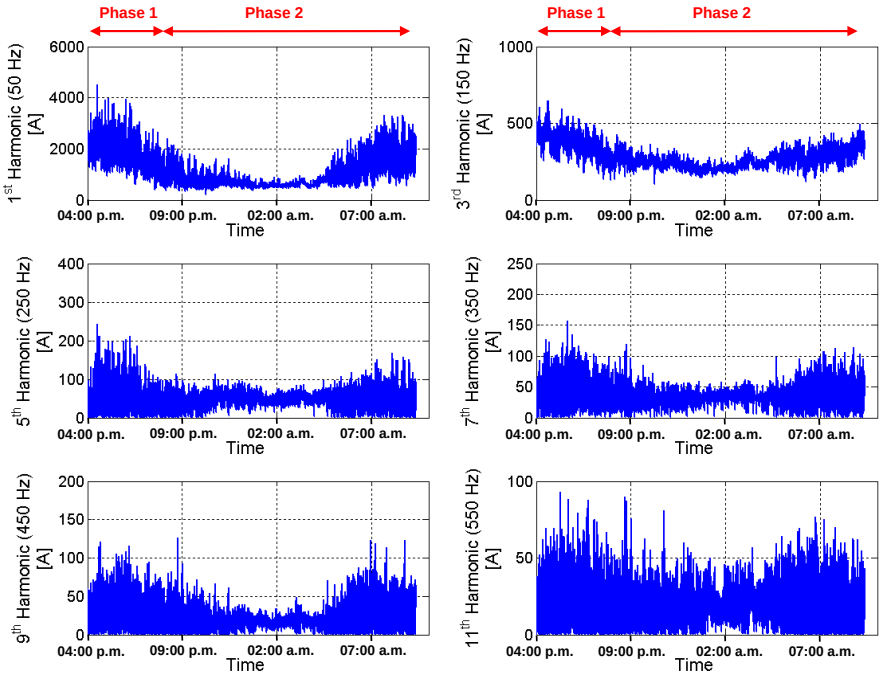


Fig. 46 – Amplitude of current harmonics versus time

The maximal values of the low frequency current harmonics are listed in Table III. They were recorded during Phase 1.

Figure 47 shows that the substation current waveform is greatly distorted, with high amplitudes for low frequency components. In fact, this is a typical current waveform for locomotives using thyristor rectifiers **[20]**.

Table III - Maximum current harmonic amplitudes.

1st Harmonic (50 Hz)	4522 A
3rd Harmonic (150 Hz)	649 A
5th Harmonic (250 Hz)	243 A
7th Harmonic (350 Hz)	157 A
9th Harmonic (450 Hz)	127 A
11th Harmonic (550 Hz)	92 A

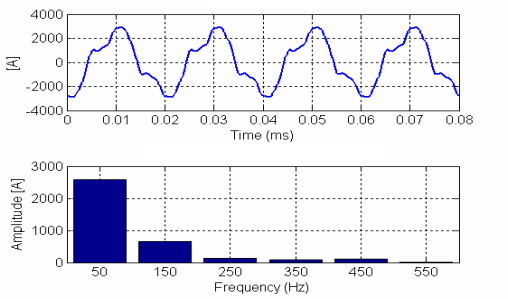


Fig. 47 – Substation output current waveform and spectrum (Phase 1).

The total harmonic distortion of the current (*THD*) can be calculated at each network period using the following relationship:

$$THD = \frac{\sqrt{\sum_{n=2}^{11} \hat{I}_{sub}(n)^2}}{\hat{I}_{sub}(1)} \tag{55}$$

Figure 48 shows that the current THD can reach a value of 65%, and the lowest level of THD is observed during rush hours because of the high level of fundamental current at these times.

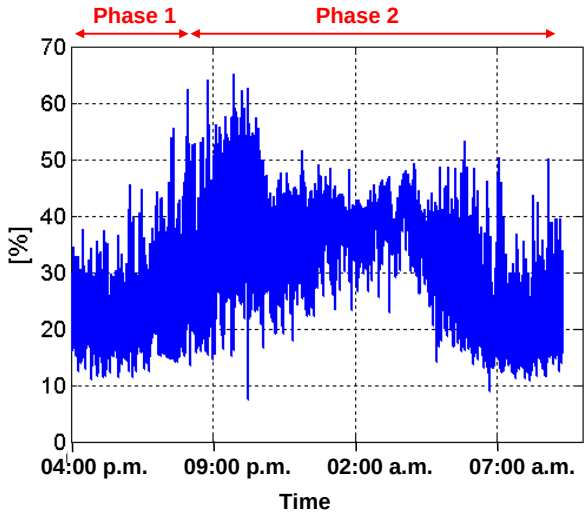


Fig. 48 – Substation output current THD.

III.2.3 Power analysis

The active and reactive powers are calculated for the fundamental frequency as follows:

$$P_{sub} = V_{cat}(1).I_{sub}(1).\cos\left(\phi_{v_{cat}/i_{sub}}\right) \tag{56}$$

$$Q_{sub} = V_{cat}(1).I_{sub}(1).\sin\left(\phi_{v_{cat}/i_{sub}}\right) \tag{57}$$

with $V_{cat}(1)$: the RMS value of the fundamental component of the overhead line voltage

$\phi_{v_{cat}/i_{sub}}$: the phase angle between the fundamental components of the overhead line voltage and the output substation current.

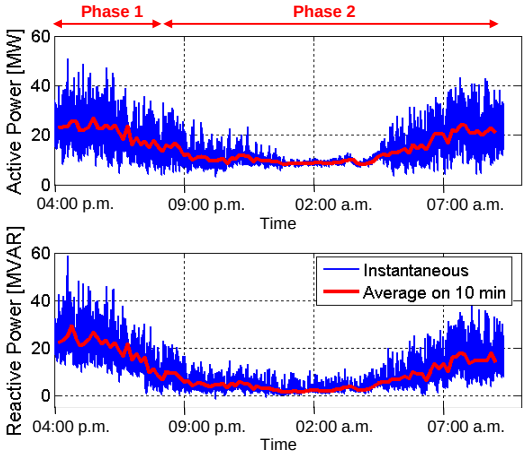


Fig. 49 – Substation active and reactive power.

The results of the power calculations (Fig. 49) show that periods of high power consumption are observed at the end of the afternoon and in the morning, and the influence of the fixed 7.5-MVAR compensation bank can be seen. Indeed, the average reactive power in the morning is lower than that observed in the afternoon

III.2.4 Reactive power compensator

At present, the reactive power compensation in the substation is performed using fixed capacitive LC shunt filters.

Between rush hours, these filters can lead to overcompensation when the train traffic is low. Therefore, it is not possible to increase the fixed compensation level.

Thus, it is interesting to investigate the use of the chopper controlled impedance concept to adjust the level of reactive power compensation.

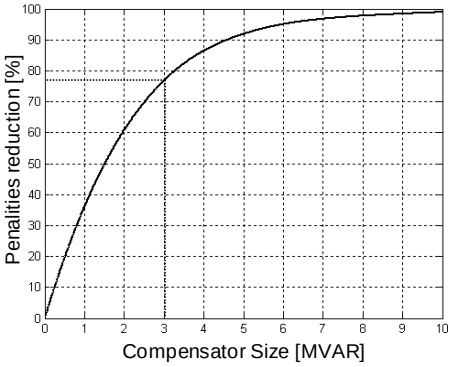


Fig. 50 – Penalty reduction vs. variable compensation level.

In the initial situation, LC filters provide 13 MVAR at 27.5 kV and, to avoid penalties when the load current is high, the compensation range has to be increased by ΔQ. For the *Revest* substation, the value of ΔQ was chosen by performing an analysis of the reactive energy recorded during several months. Figure 50

shows the percentage reduction in penalties as a function of compensation level ΔQ.

For a satisfactory cost/benefit trade-off, ΔQ was set to 3 MVAR.

Two compensators based on the active impedance concept are presented and analyzed in the following sections.

III.2.4.1 - 3-MVAR CCI based on step-down AC chopper

The topology of a 3-MVAR CCI based on a step-down AC chopper, introduced in **[21]**, is shown in figure 51. It is based on 4 interleaved AC choppers using 3.3 kV/1.5 kA IGBTs. The maximal input voltage is fixed at 1.8 kV, and the maximal commutated current at 880 A. The compensator is added to the substation, and the existing 5.5-MVAR compensation bank is removed and replaced by the input filter of the CCI.

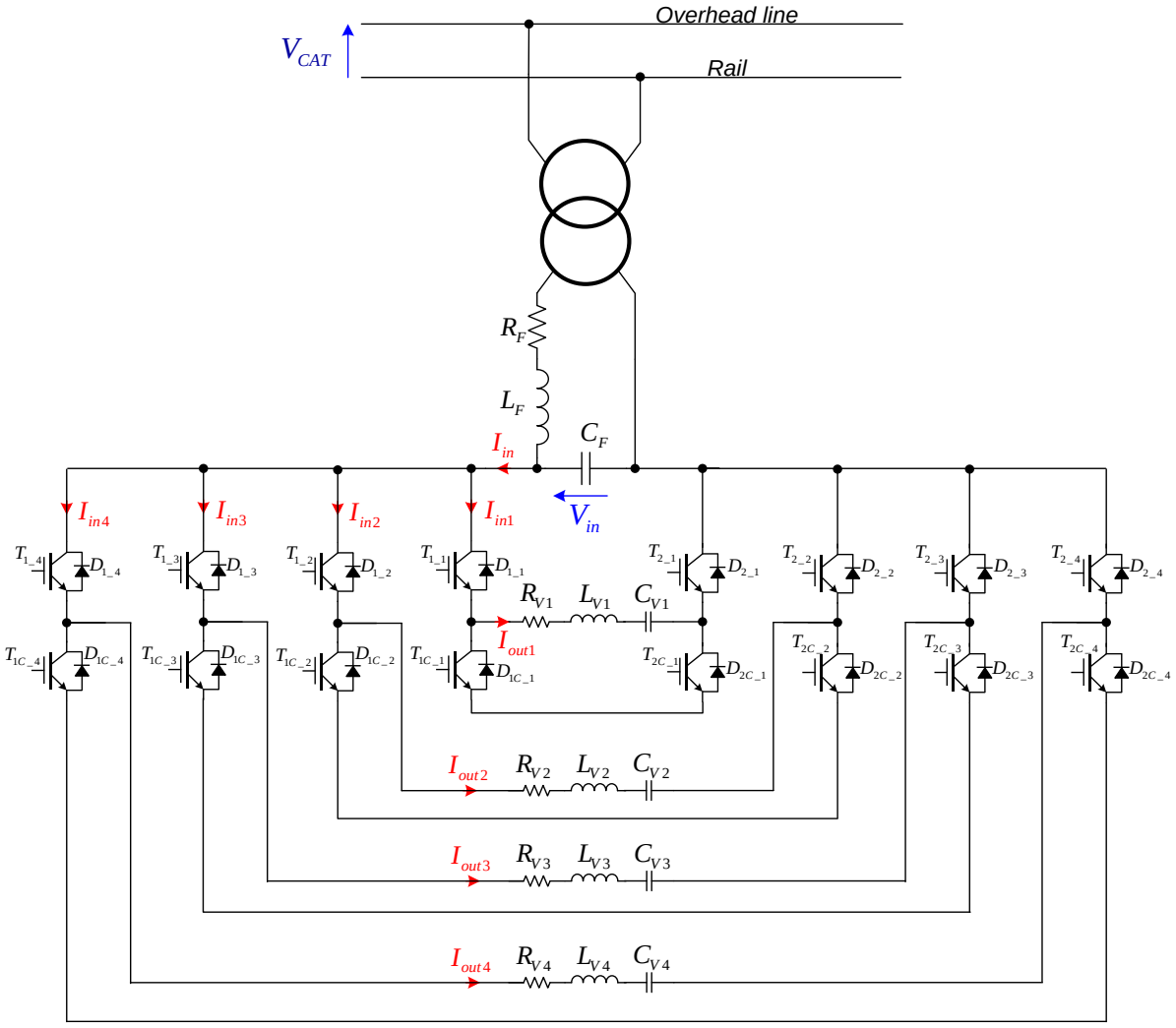


Fig. 51 – 3-MVAR CCI based on step-down AC chopper.

a) 3-MVAR CCI modelling

The 3-MVAR CCI averaged model used for the study is shown in figure 52. Because the compensator behaves as variable impedance **[17]**, this model is used to analyze its influence on the electrical network.

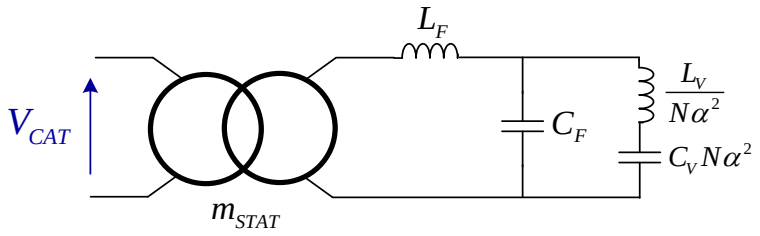


Fig. 52 – 3-MVAR variable CCI based on step-down PWM AC chopper equivalent circuit (α: duty cycle of AC choppers; N = 4).

The output impedance of an AC chopper is given by:

$$Z_{out}(s) = L_V s + \frac{1}{C_V s} \tag{58}$$

The equivalent impedance expression for *N* AC choppers in parallel is:

$$Z_{eq}(s) = \frac{Z_{out}(s)}{N.\alpha^2} \tag{59}$$

On this basis, the total impedance of the compensator is:

$$Z_{STAT}(s) = \frac{1}{m^2}\left[L_F.s + \frac{Z_{eq}(s)}{1 + Z_{eq}(s).C_F.s}\right] \tag{60}$$

b) Design criteria

The following criteria are considered for the design.

- To avoid interaction with low frequency harmonics, the input filter resonant frequency is fixed at 120 Hz.

$$f_{rF} = \frac{1}{2.\pi\sqrt{L_F.C_F}} = 120\,Hz \tag{61}$$

- The reactive power variation provided by the compensator at V_{CAT} = 22 kV is 3 MVAR.

$$\Delta Q_{STAT} = V_{cat}^{\,2}\left(\frac{1}{Z_{STAT}(\alpha_{\max})} - \frac{1}{Z_{STAT}(\alpha_{\min})}\right) = 3MVAR \tag{62}$$

- The maximum crest input working voltage is 1800 V when V_{CAT} = 27,5 kV and α = 0.05.

$$Q_{TOT}(\alpha_{\min}) = V_{cat}^{\,2}\left(\frac{1}{Z_{STAT}(\alpha_{\min})} + \frac{C_2.\omega_{net}}{1 - L_2.C_2.\omega_{net}^{\,2}}\right) = 13MVAR \tag{63}$$

- The output resonant circuit, $L_V - C_V$, behaves as capacitive impedance at the network frequency. Inductor L_v limits the current ripple at the switching frequency.

The parameter values for the compensator are listed in Table IV.

Figure 53 shows the supplied reactive power as a function of the duty cycle at overhead voltage V_{cat} = 22 kV.

Table IV - CCI parameters.

	Parameters	Value
m_{STAT}	Transformer ratio	0.0382
f_{rF}	Filter cut-off frequency (Hz)	120
L_F	Filter inductance (μH)	134
C_F	Filter capacitor (mF)	13.1
N	Number of AC chopper	4
f_{sw}	Switching frequency (kHz)	1
L_V	AC chopper output inductance (mH)	5
C_V	AC chopper output capacitor (μF)	1.1

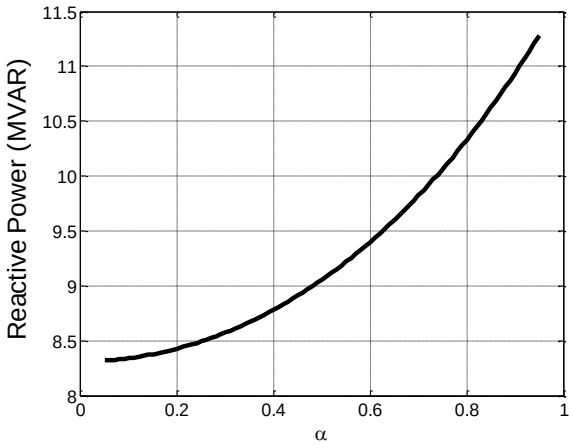


Fig. 53 – Reactive power provided versus duty cycle at V_{CAT} = 22 kV.

c) Frequency analysis

The frequency analysis is based on the averaged model of the AC chopper and takes into account the substation's equivalent circuit (Fig. 54) [22]. The load is assumed to be a current source. The equivalent circuit for the high voltage network and substation transformer is a voltage source, v_{cat0}, with series impedance L_{sec}.

The transfer functions, V_{cat}/I_{train} and V_{in}/I_{train}, are studied for the frequency analysis, and their analytical expressions, neglecting the different resistances, are given by:

$$\frac{V_{cat}}{I_{train}}(s)=\left[\frac{1}{Z_{STAT}(s)}+\frac{1}{Z_2(s)}+\frac{1}{Z_{\sec}(s)}\right]^{-1} \tag{64}$$

$$\frac{V_{in}}{I_{train}}(s)=\left\{\left[\frac{1}{Z_{STAT}(s)}+\frac{1}{Z_2(s)}+\frac{1}{Z_{sec}(s)}\right].\left[L_F.s.\frac{\left(Z_{eq}(s).C_F.s+1\right)}{Z_{eq}(s)}+1\right]\right\}^{-1} \quad (65)$$

where Z_{sec} is the network impedance and Z_2 is the impedance of the 7.5-MVAR compensation banks:

$$Z_2(s)=\frac{1+L_2C_2s^2}{C_2s} \quad (66)$$

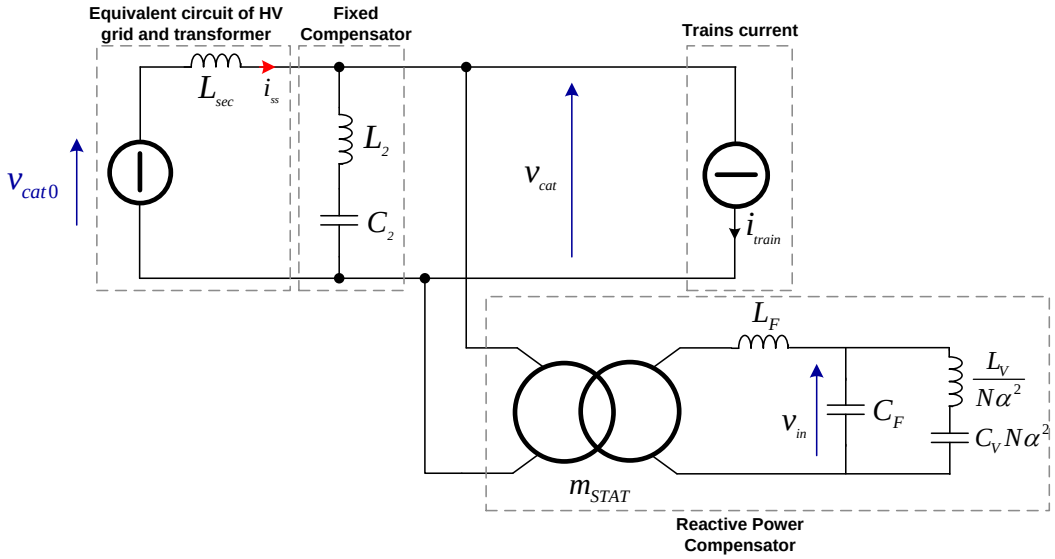


Fig. 54 – *Revest* substation with CCI electrical equivalent circuit (α: duty cycle of AC choppers; N = 4).

The Bode magnitude plots of V_{cat}/I_{train} and V_{in}/I_{train} for frequencies between 50 Hz and 1 kHz are shown in figures 55 and 56, respectively. It can be seen that, with regard to the current harmonics generated by the trains, the CCI has no effect on the substation's behaviour. As can be seen in figures 18 and 19, resonance frequencies are restricted to the 100–150 Hz range and are close to 70 Hz.

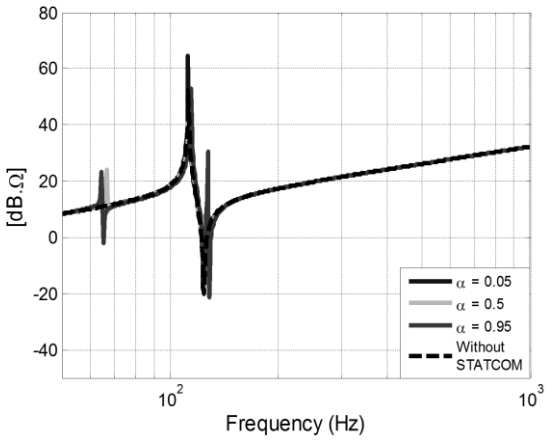


Fig. 55 – V_{cat}/I_{train} gain.

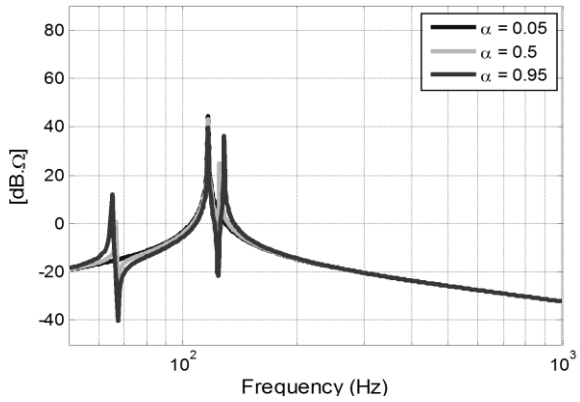


Fig. 56 – V_{in}/I_{train} gain

d) Simulations

In order to validate the results of the frequency analysis, simulations were performed using the substation output current and overhead line voltage measurements.

The simulations concerned the operating point where the load current during Phase 1 had the maximal amplitude of the 7th harmonic.

The AC choppers operate with an open-loop control at the maximal duty cycle.

Current source i_{train} corresponds to the real current waveform. Electromotive force v_{cat0} was reconstituted by using the current and overhead line voltage measurements.

The simulation results reported in figure 57 show that there is no overvoltage across C_F , and the correct operation of the CCI in the substation is confirmed.

Despite the fact that the proposed solution works properly, because of the large input filter (5.5 MVA), it requires an 8.5 MVA step-down transformer. This is a serious drawback and is the reason for choosing a 'transformerless' solution based on the AC chopper in the step-up mode, as shown in the next section.

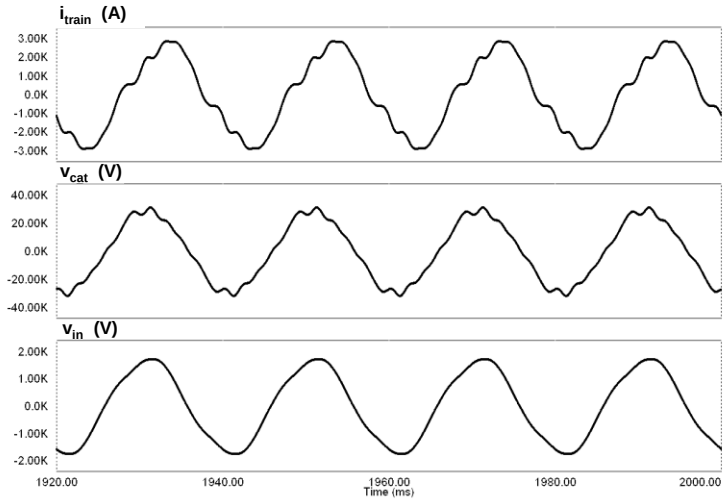


Fig. 57 – Train current, overhead line voltage and CCI input filter capacitor voltage waveforms at α max.

III.2.4.2 3-MVAR CCI based on step-up AC chopper

The proposed structure is shown in figure 58 and was first presented in 2010 **[23]**. Basically, the compensator consists of two series-connected, controlled, capacitive impedances and one fixed impedance. The series-connection of the variable capacitances requires the addition of a fixed shunt filter, L_{fix}-C_{fix}, to obtain a total of 16 MVAR.

Each controlled impedance is composed of one of the already existing LC compensation banks, an inductor L_V and N AC choppers. Inductor L_V represents an additional degree of freedom in the compensator design to adjust the resonance frequency.

In this configuration, the AC choppers operate in step-up mode and an increase in the duty cycle reduces the total reactive power.

Because of the series association of the AC choppers, the voltage is split across N converters. This allows direct operation at high voltage without a step-down transformer. In this case, an interleaved modulation in

the switching pattern generation has to be used. The chosen semiconductor devices are 6.5 kV/600 A IGBT modules switching at 1 kHz.

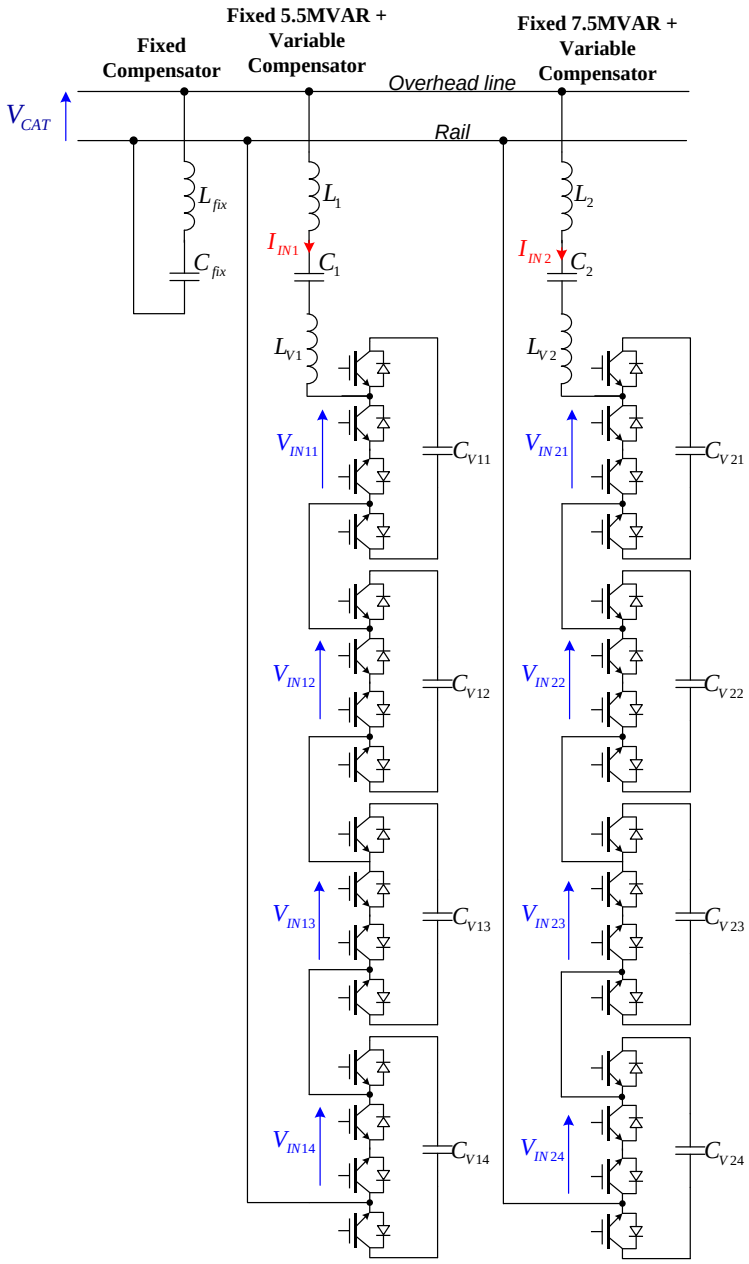


Fig. 58 – 3-MVAR CCI based on step-up AC chopper.

a) 3-MVAR CCI model

The average model of the variable parts is reported in figure 59. At the fundamental frequency, this structure behaves as a fixed capacitive impedance connected in series with a variable capacitive impedance.

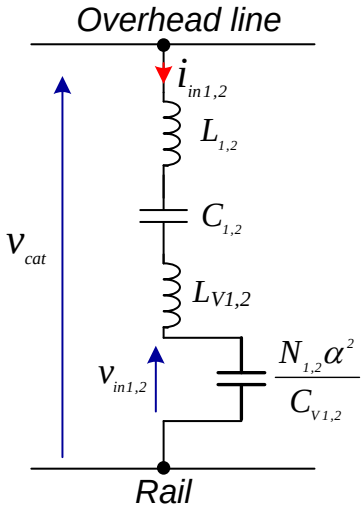


Fig. 59 – Average model for variable part of CCI.

The resulting system is a variable impedance controlled by duty cycle α (67), where the impedance increases with α, while the supplied reactive power decreases.

The supplied reactive power and resonance frequency for each variable part are expressed by relations (68) and (69):

$$Z_{STAT1,2}(s) = \left(L_{1,2} + L_{V1,2}\right)s - \frac{1}{C_{1,2}s} - \frac{N_{1,2}.\alpha^2}{C_{V1,2}s} \tag{67}$$

$$Q_{1,2}(\alpha) = \frac{V_{cat}^{\ 2}}{\left(L_{1,2} + L_{V1,2}\right).\omega - \frac{1}{C_{1,2}.\omega} - \frac{N_{1,2}.\alpha^2}{C_{V1,2}.\omega}} \tag{68}$$

$$f_{r1,2}(\alpha) = \frac{1}{2.\pi.\sqrt{\left(L_{1,2} + L_{V1,2}\right).\frac{C_{1,2}.C_{V1,2}}{C_{V1,2} + C_{1,2}.N_{1,2}.\alpha^2}}} \tag{69}$$

b) Design criteria

The aim is to determine the values for reactive elements $L_{V1,2}$, $C_{V1,2}$, L_{fix}, C_{fix} and the number of AC choppers in series.

The following criteria are considered for the design.

- The resonant frequency for each variable part is fixed at 138 Hz.

$$f_{r1,2}(\alpha_{\max}) = 138Hz \tag{70}$$

- The reactive power variation $\Delta Q_{STAT}=\Delta Q_{STAT1} + \Delta Q_{STAT2}$ provided by the compensator at V_{CAT} = 22 kV is 3 MVAR.

$$\Delta Q_{STAT1,2} = V_{cat}^{\ 2}\left(\frac{1}{Z_{STAT1,2}(\alpha_{\min})} - \frac{1}{Z_{STAT1,2}(\alpha_{\max})}\right) = 3MVAR \tag{71}$$

The values of ΔQ_{STAT1} and ΔQ_{STAT2} are set to be proportional to the compensation level of the fixed bank used in the initial configuration of the substation. Thus, $\Delta Q_{STAT1}=1.17MVAR$ and $\Delta Q_{STAT1}=1.73MVAR$.

- The number of AC choppers in series, N_1 or N_2, is determined by the fact that the maximum voltage at the AC chopper output must be less than the maximal allowable operating voltage on the IGBTs (3600 V) at the maximal overhead line voltage (29 kV) and the maximal duty cycle.

$$V_{out1,2}\sqrt{2} = -\frac{\alpha_{\max}.V_{cat}\sqrt{2}}{L_{1,2}.C_{V1,2}.\omega_{net}^2 - \frac{C_{V1,2}}{C_{1,2}} - N_{1,2}.\alpha_{\max}^2} \tag{72}$$

- The fixed part, L_{fix} - C_{fix}, is designed to produce 13 MVAR of compensation at the maximal overhead line voltage (29 kV) for α_{MAX}, as in the initial configuration. Moreover, a resonant frequency of 138 Hz is considered.

$$Q_{TOT}(\alpha_{\max}) = V_{cat}{}^2\left(\frac{1}{Z_{STAT1}(\alpha_{\max})} + \frac{1}{Z_{STAT2}(\alpha_{\max})} + \frac{1}{Z_{fix}}\right) = 13\,MVAR \tag{73}$$

$$f_{r1,2}(\alpha_{\max}) = 138Hz \tag{74}$$

The calculation results are listed in Table V.

Figure 60 shows the reactive power supplied as a function of the duty cycle at overhead voltage V_{cat} = 22 kV, for both variable parts.

Table V - CCI parameters.

		Variable Part 1	**Variable Part 2**
N	Number of AC-choppers	4	4
L_v	AC chopper output inductance (mH)	14	12
C_v	AC chopper output capacitor (μF)	152	210
		Fixed Part	
L_{fix}	Fixed part inductance (mH)	82	
C_{fix}	Fixed part capacitor (μF)	16	

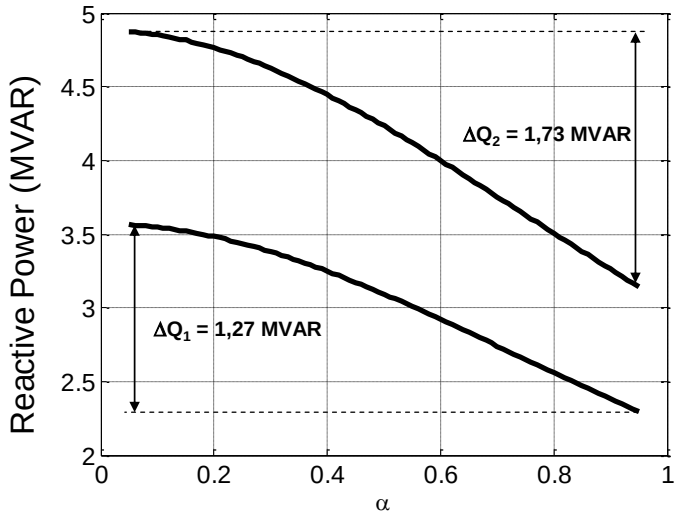


Fig. 60 – Reactive power supplied versus duty cycle at Vcat = 22 kV.

c) *Frequency analysis*

The averaged model for the controlled impedances and substation is shown in figure 61.

The transfer functions, V_{cat}/I_{train} and $I_{in1,2}/I_{train}$, are given by the following expressions:

$$\frac{V_{cat}}{I_{train}}(s)=\left[\frac{1}{Z_{STAT1}(s)}+\frac{1}{Z_{STAT2}(s)}+\frac{1}{Z_{fix}(s)}+\frac{1}{Z_{sec}(s)}\right]^{-1} \tag{75}$$

$$\frac{I_{in1,2}}{I_{train}}(s)=\frac{1}{Z_{STAT1,2}(s)}\left[\frac{1}{Z_{STAT1}(s)}+\frac{1}{Z_{STAT2}(s)}+\frac{1}{Z_{fix}(s)}+\frac{1}{Z_{sec}(s)}\right]^{-1} \tag{76}$$

where Z_{fix} is the impedance of the fixed compensator:

$$Z_{fix}(s)=\frac{1+L_{fix}C_{fix}s^2}{C_{fix}s} \tag{77}$$

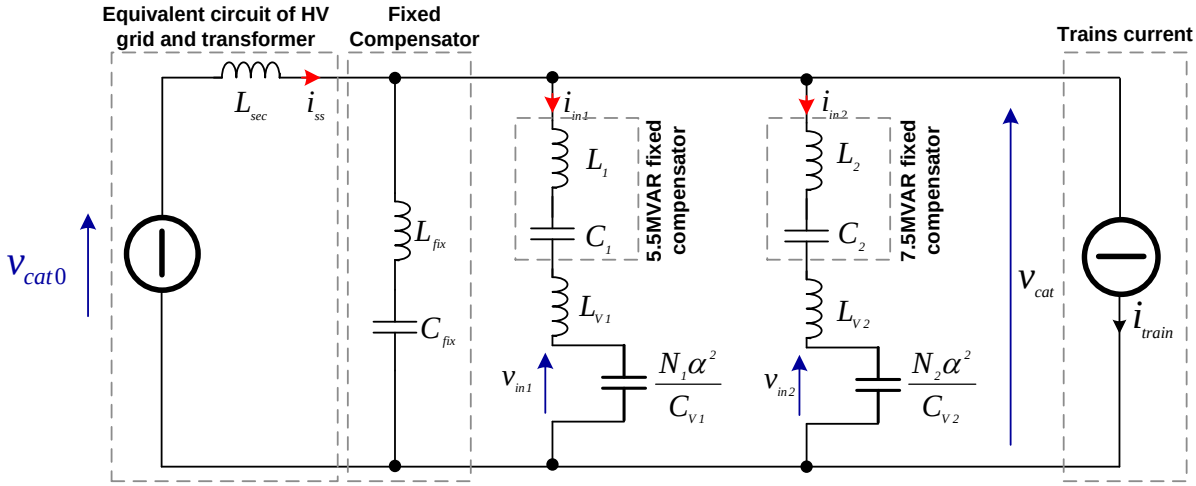


Fig. 61 – *Revest* substation with CCI electrical equivalent circuit.

The Bode magnitude diagram for transfer function V_{cat}/I_{train} is plotted in figure 62 for different values of duty cycle α, and the initial substation total impedance is superimposed.

The frequency responses for I_{in1}/I_{train} and I_{in2}/I_{train} are shown in figures 63 and 64.

The frequency analysis shows that the resonant frequency variations are in the range of 100 to 150 Hz. Thus, the correct performance of the proposed compensator is confirmed.

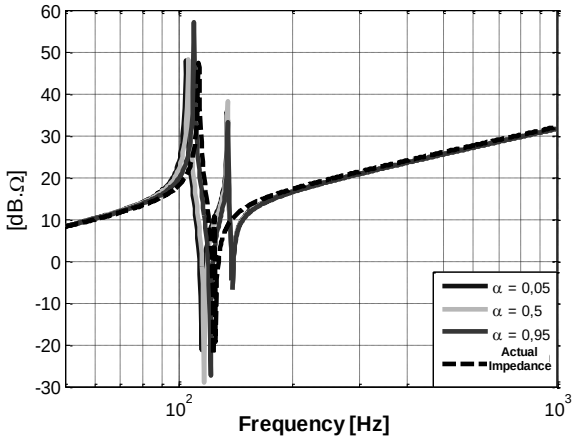


Fig. 62 – Vcat/Itrain frequency response.

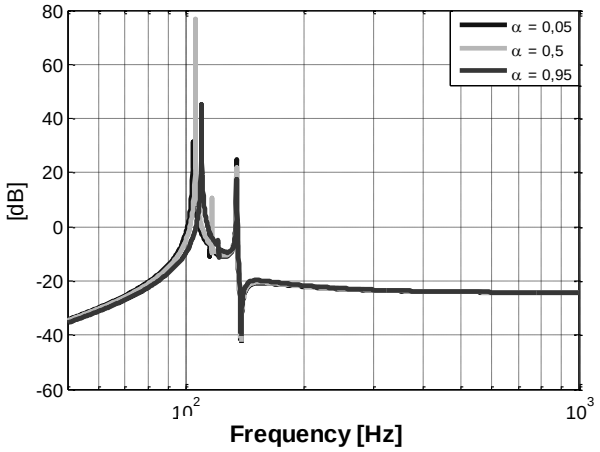


Fig. 63 – I_{in1}/I_{train} frequency response.

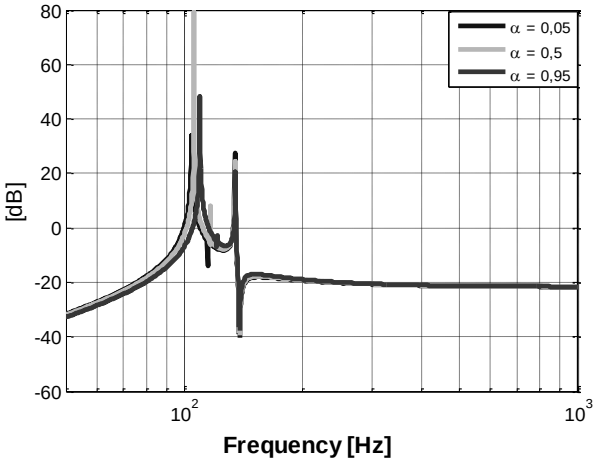


Fig. 64 – I_{in2}/I_{train} frequency response.

d) Simulation results

As in the previous case, the system is modelled and simulated using Psim software.

The simulation results reported in figure 65 refer to the case of the maximal measured third harmonic current in the catenary (649 A) and a maximal duty cycle of 0.95.

It can be seen that simulated currents I_{in1} and I_{in2} drawn by the variable compensators are highly distorted and present a non-negligible third harmonic. Nevertheless, the current in the fixed compensator has the same shape as currents I_{in1} and I_{in2}, and the crest working voltage at the input of the AC chopper is 3100 V, i.e. lower than the maximal allowed for the IGBTs.

Thus, the simulation results confirm the correct operation of the reactive power compensator in this substation.

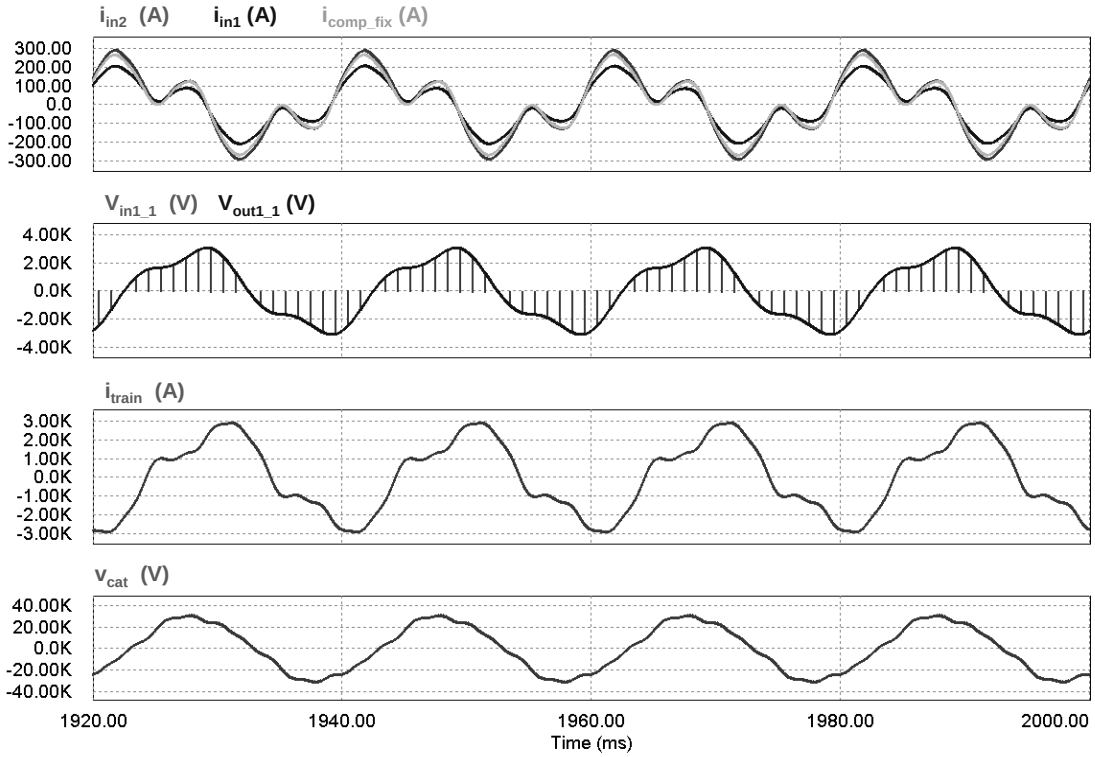


Fig. 65 – AC chopper input current, fixed compensator current, input voltage for AC chopper converters, train current and overhead line voltage (case of maximal third harmonic: 649 A, α = 0.95).

III.2.4.3 Experimental results

To validate the Chopper Controlled Impedance concept, a 1.2 MVAR prototype was built in the LAPLACE laboratory in Toulouse and tested at the SNCF test platform in Vitry (Paris). The test bench, shown in figures 66 and 67, was based on the series connection of an AC chopper and LC filter.

The component values for the compensator are as follows:

L_f =3.7 *mH*, C_{f1}=526.5 *μF*, C_{f2}=1.6 *mF*.

The RMS value of the AC voltage used during the test was 2450 *V*. The semiconductor devices used in the AC chopper were ABB 3.3 kV/1500 A IGBTs (type 5SNA 1500G330300) operating at a switching frequency of 1 kHz.

The control and PWM switching pattern were realised using a mixed environment DSP and FPGA.

The theoretical electrical parameter variations for the prototype are presented in figure 68. The maximal reactive power provided was about 1.2 MVAR and the reactive power variation, ΔQ, was 320 kVAR.

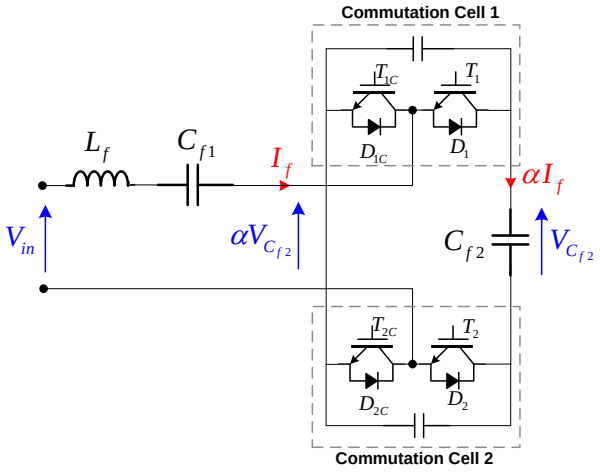


Fig. 66 – Equivalent circuit of prototype under test.

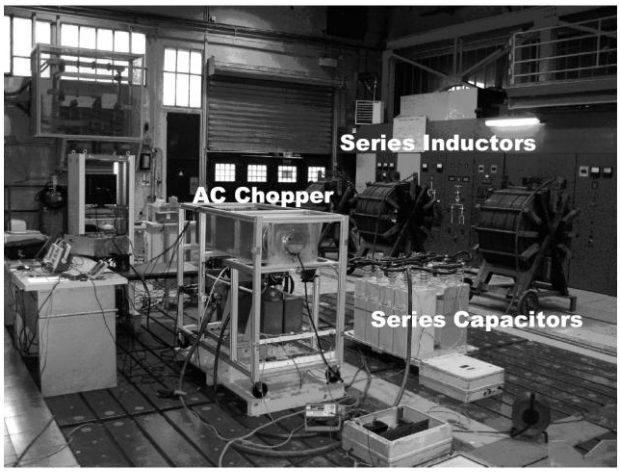


Fig. 67 – Test bench.

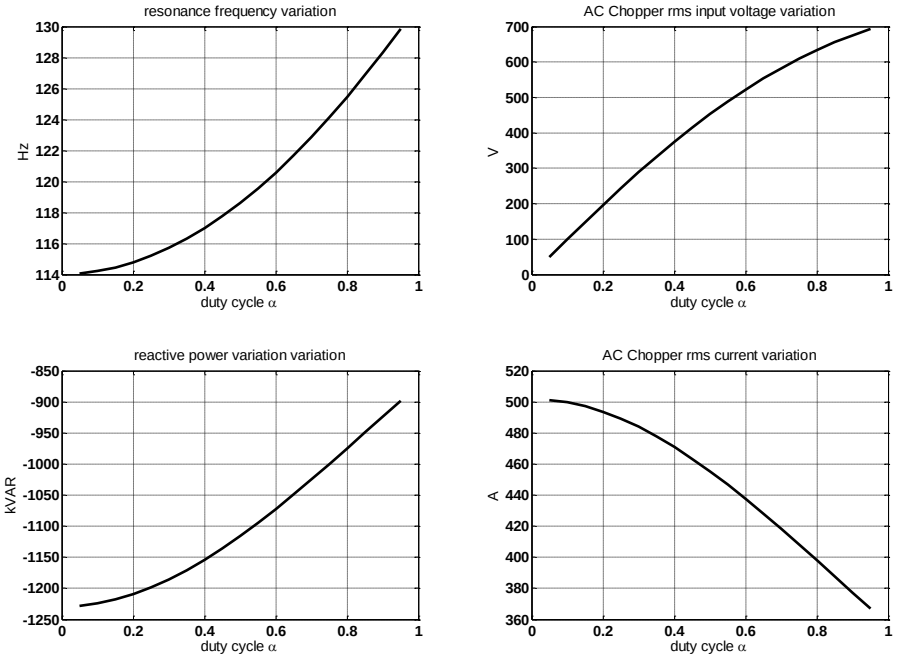


Fig. 68 – Variation expected for V = 2450 V.

Figure 69 shows the AC chopper input voltage waveforms for different duty cycles, and figure 70 shows the current waveforms.

The reactive power variation, Q (α), is plotted in figure 71. All of the experimental measurements match well to the previously calculated values.

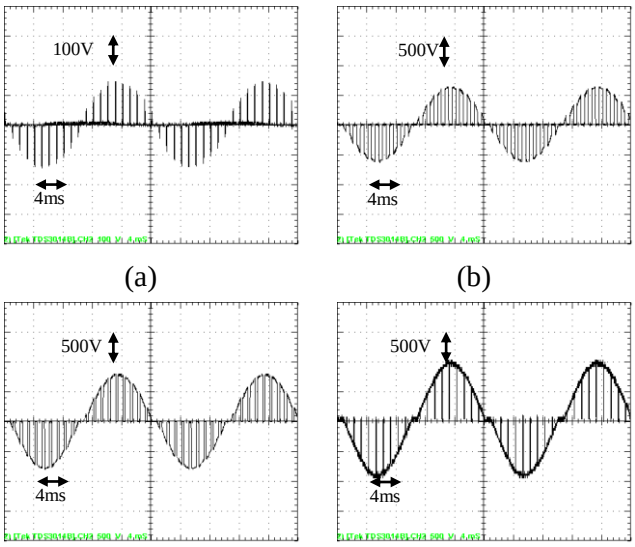


Fig. 69 – AC chopper input voltage for duty cycles:
a) 0.1, b) 0.5, c) 0.7, d) 0.95.

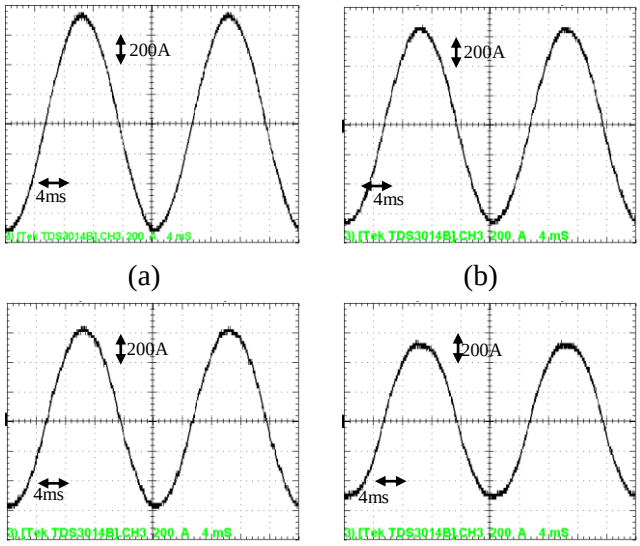


Fig. 70 – Compensator currents for duty cycles:
a) 0.1, b) 0.5, c) 0.7, d) 0.95.

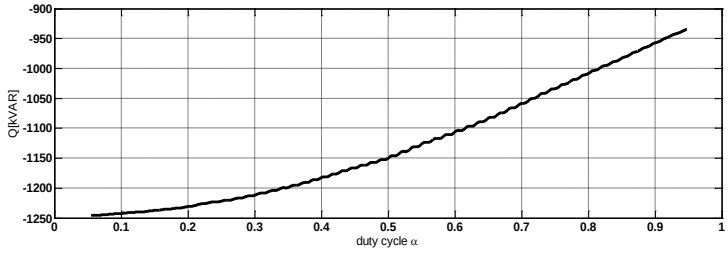


Fig. 71 – Provided reactive power versus duty cycle.

A spectral analysis was performed for all of the measurements. This was necessary to analyze the interaction of the compensator with the pre-existing harmonics on the grid. An FFT for the input voltage

source is presented in figures 72 and 73. These figures show the voltage magnitude before and after the compensator insertion for duty cycles of 5%, 50% and 95%.

The same thing was carried out for the compensation current and figures 74 and 75 show the spectral analyses of the measured currents, again for duty cycles of 5%, 50% and 95%. As expected, by increasing the duty cycle, the compensator resonance frequency increased and came close to the 3rd harmonic frequency, which is why the 150-Hz component was seen to increase with the duty cycle.

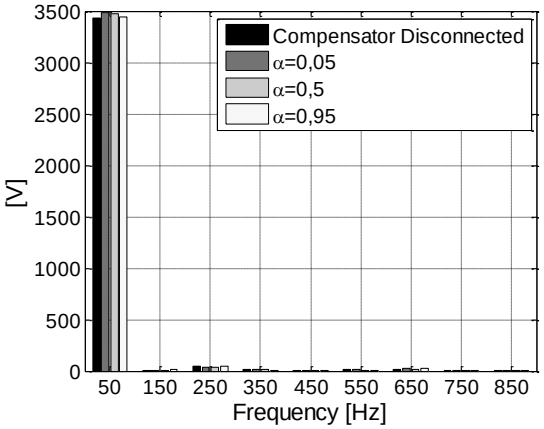


Fig. 72 – Supply voltage FFT.

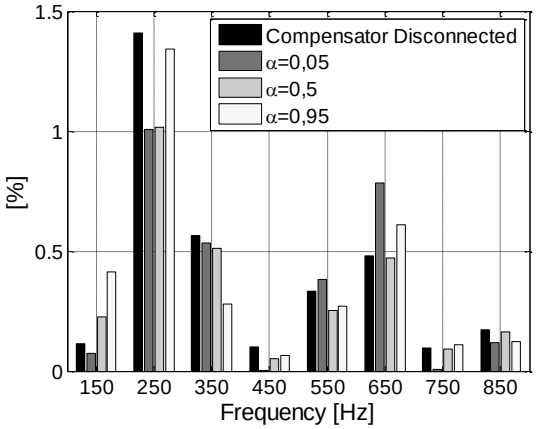


Fig. 73 – Supply voltage FFT in percentage.

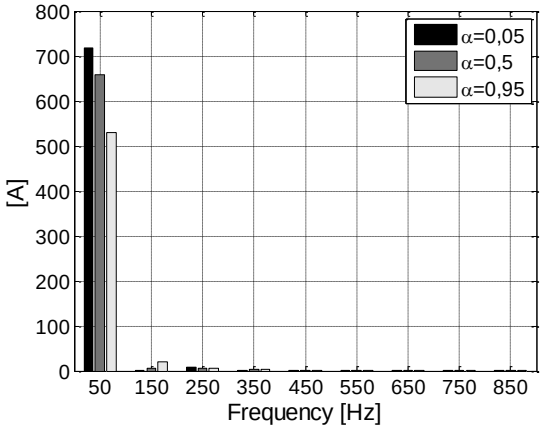


Fig. 74 – Compensator current FFT.

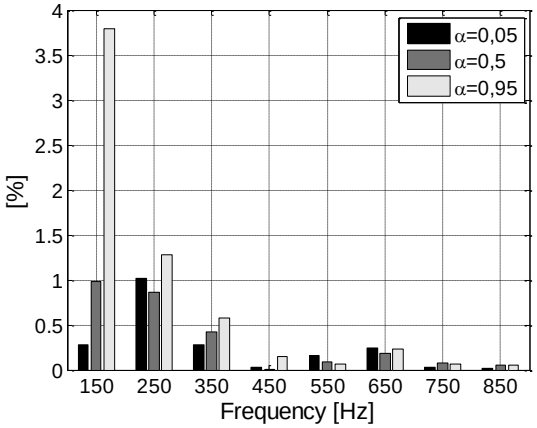


Fig. 75 – Compensator current FFT in percentage of fundamental.

III.3 Conclusion

In this chapter, a new reactive power compensator based on the controlled impedance concept was proposed, and two topologies were presented. The first one requires an input transformer, while the second is a transformerless solution.

A real substation was used as a case study, and the compensator design was based on an analysis of the measurements carried out in this substation.

Additionally, simulations were carried out that confirmed the anticipated performance of the novel topology even when real (measured) waveforms were used in the simulations.

Furthermore, a 1.2-MVAR prototype of the compensator was built and tested on an SNCF test platform. The experimental results confirmed the analytical study and the excellent performance of the system.

Chapter IV. **Voltage unbalance compensation based on CCI: active Steinmetz compensator**

This chapter deals with a new voltage unbalance compensation technique for single-phase railway substations based on CCI.

A common solution to rebalance industrial high-power single-phase loads is the Steinmetz circuit. This technique consists of an inductor and capacitor suitably connected to the three-phase network to rebalance the single-phase load.

Using the chopper controlled impedance concept, the feasibility of an active Steinmetz circuit based on AC choppers is studied.

The proposed compensator topology is introduced, and the advantages and drawbacks in terms of its compensation capability are highlighted.

IV.1 Unbalance compensation based on active Steinmetz circuit

IV.1.1 Steinmetz balancer circuit

The *Steinmetz circuit* [24] represents a common solution to balance industrial high-power single-phase loads. This technique consists of connecting an inductive impedance and capacitive impedance to the single-phase load in order to reduce the unbalance in the electric power system.

In order to understand the functional principle, let us consider the simple schematic of figure 76, where a generic single-phase load is connected between phases ‘b’ and ‘c’ of a three-phase transmission line. The resulting line currents are unbalanced, as described in the phasor diagram of figure 77.

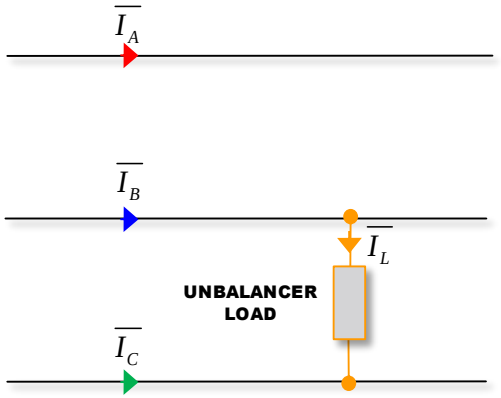


Fig. 76 – Single-phase load connection.

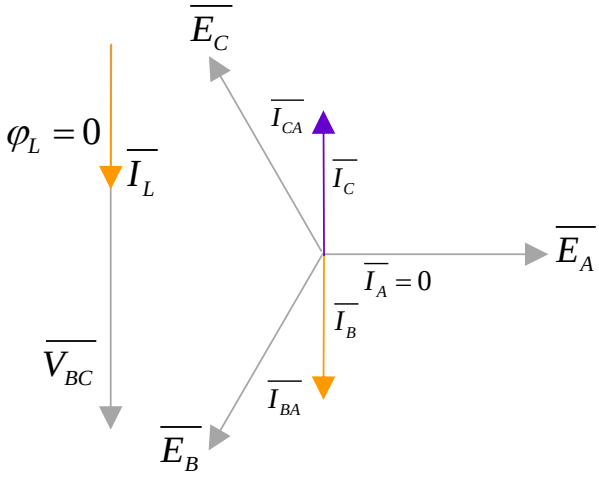


Fig. 77 – Phasor diagram of line currents with single-phase load connection.

For simplicity, a unitary power factor load is considered. On this basis, a balanced condition can be achieved if currents i_{CA} and i_{AB} are injected into the system as shown in the phasor diagram of figure 78. This can ideally be done by considering two current generators in the circuit, as described in figure 79. Let us point out that the generator currents lag and lead the respective line-to-line voltages, v_{AB} and v_{CA}, by 90°. Thus, the requested current can be obtained by connecting an inductor between phases 'a' and 'b' and a capacitor between phases 'a' and 'c'. The circuit composed of these two reactors, as shown in figure 80, is known as a 'Steinmetz circuit'.

It can be demonstrated that in the case of unitary power factor load R, currents can be balanced using inductive and capacitive reactors with the following values [25]:

$$X_C = X_L = \sqrt{3}R \tag{78}$$

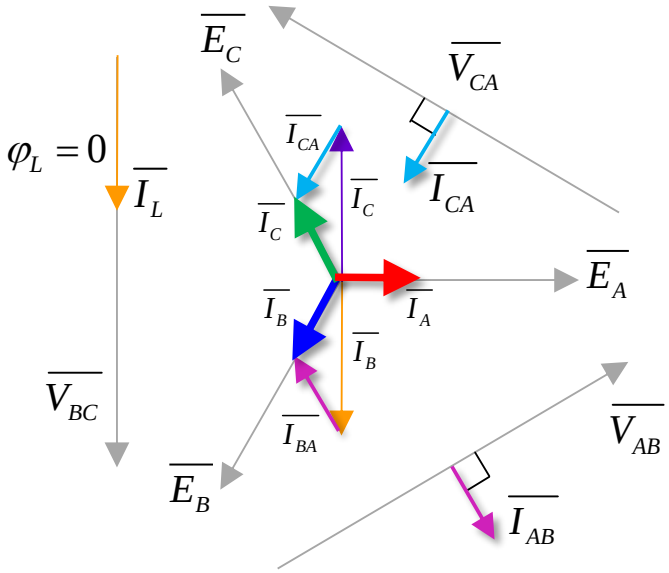


Fig. 78 – Phasor diagram of line currents with single-phase load connection and Steinmetz circuit insertion.

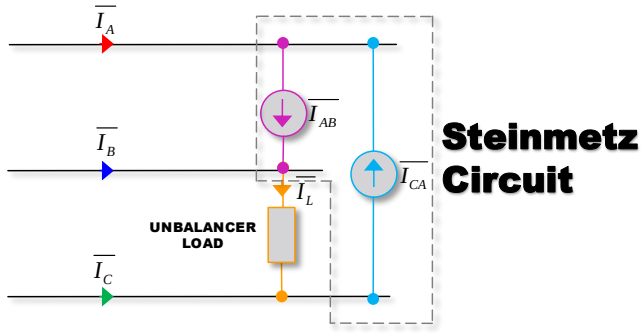


Fig. 79 – Ideal Steinmetz circuit insertion.

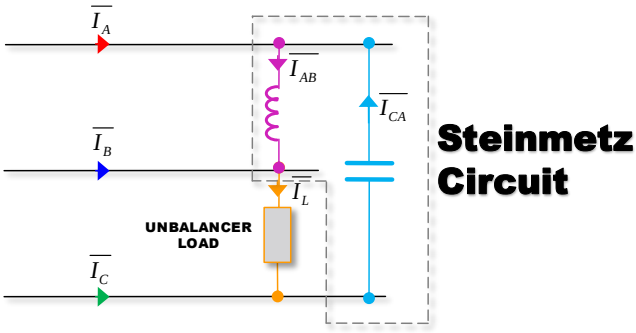


Fig. 80 - Steinmetz circuit insertion.

Otherwise, in the case of non-unitary factor loads, reactances can be chosen according to:

$$\frac{1}{Z} = \frac{e^{j\frac{\pi}{6}}}{|X_C|} + \frac{e^{-j\frac{\pi}{6}}}{|X_L|} \tag{79}$$

where Z is the impedance of the single-phase load.

IV.2 Active Steinmetz compensator

The Steinmetz circuit is a simple solution to rebalance fixed single-phase loads. If the single phase impedance does not vary significantly with respect to the value considered in the design of the inductor and capacitor, acceptable balance is achieved. Nevertheless, in the case of a strongly varying load, as in the railway substation situation, the Steinmetz circuit is not effective.

A possible solution for this limitation consists of using variable reactive elements. In [25][26], a variable Steinmetz circuit is proposed that employs thyristor-controlled reactive (TCR) elements.

The thyristor-controlled reactive elements are presented in figure 81. Two topologies are shown, a thyristor-switched inductor (TSI) and a thyristor-switched capacitor (TSC).

A TSI module consists of an inductor series connected to two inverse parallel thyristors. The TSC module contains a capacitor connected in parallel to a TSI. Both of them appear as a variable impedance that depends on the thyristor's firing angle.

The control system should give firing orders to the thyristors according to the magnitudes desired for the impedances.

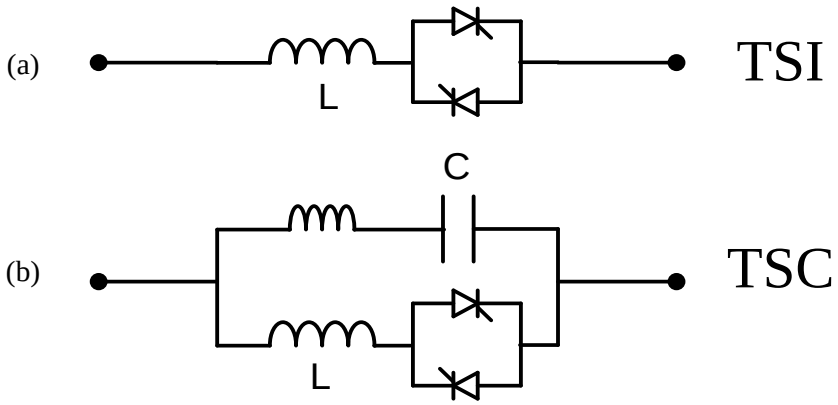


Fig. 81 - Structure of thyristor-controlled reactive elements: a) TSI, b) TSC.

Such a solution suffers from several drawbacks. Foremost among these is the poor performance in terms of power quality. Bulky filters have to be installed in order to reduce the low frequency harmonic currents generated.

An alternative way to realize variable reactive elements is by means of the chopper controlled impedance concept introduced in this manuscript. It is evident that using CCIs enhances the current spectrum compared to the TCR-based solution because of the PWM switching modulation.

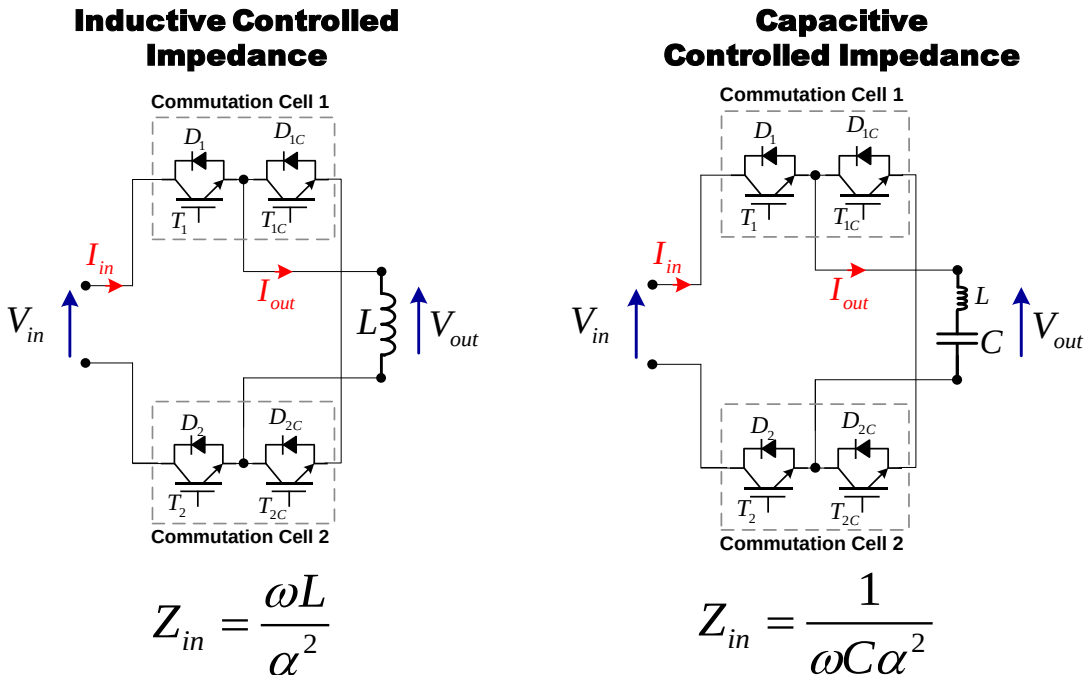
According to the theory presented in chapter II, it is possible to realize a variable capacitive and variable inductive impedance, as reported in figure 82. The step-down mode for the AC chopper converter is considered.

On this basis, if α is the PWM duty cycle for the AC chopper, the magnitude of the two obtained variable impedances is expressed as :

$$Z_L = \frac{\omega L}{\alpha^2} \tag{80}$$

$$Z_C = \frac{1}{\omega C \alpha^2} \tag{81}$$

The Steinmetz circuit realized with the CCIs, presented in **[27]**, will be called an *Active Steinmetz Circuit* later in this manuscript. Figure 83 show the insertion of the complete active Steinmetz compensator at the substation. A parallel association of AC choppers is considered. This could be necessary when it is not possible to reach the requested power rate with one converter, according to the semiconductor device chosen. A step-down transformer is considered for each CCI. The presence of the transformer is necessary to adapt the voltage level to the power electronic components used, as the compensator is connected directly at the HV power transmission line. Finally, a capacitive LC input filter is introduced to reduce the current harmonics caused by PWM modulation.



$$Z_{in} = \frac{\omega L}{\alpha^2} \qquad Z_{in} = \frac{1}{\omega C \alpha^2}$$

Fig. 82 – Inductive and capacitive variable impedances realized by CCI.

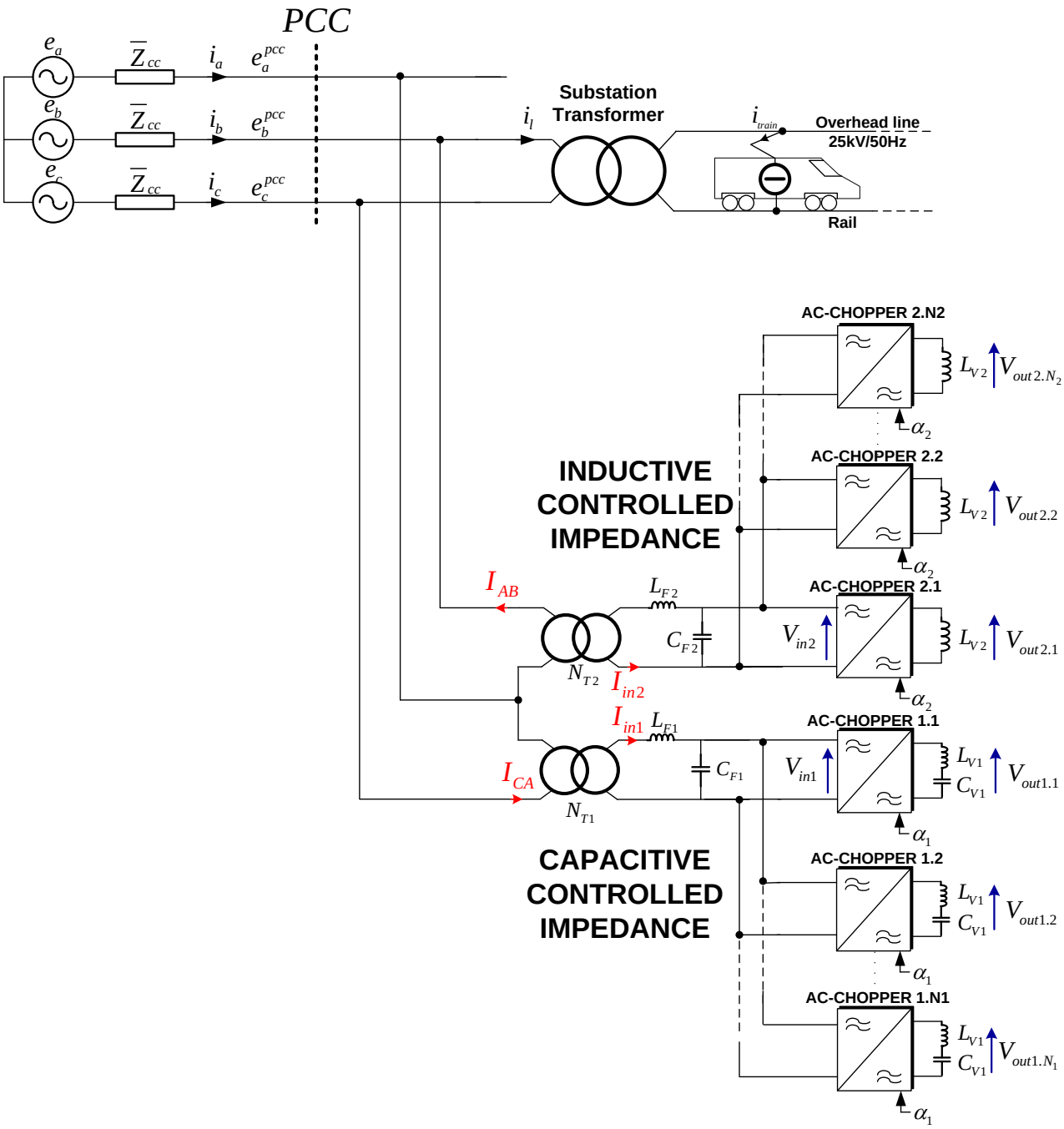


Fig. 83 - Active Steinmetz circuit insertion.

IV.2.1 Symmetrical component decomposition of active Steinmetz compensator

The role of the Steinmetz circuit is to draw currents containing a negative sequence in phase opposition to the one generated by the substation. In this way, the voltage unbalance at the PCC is reduced or totally compensated.

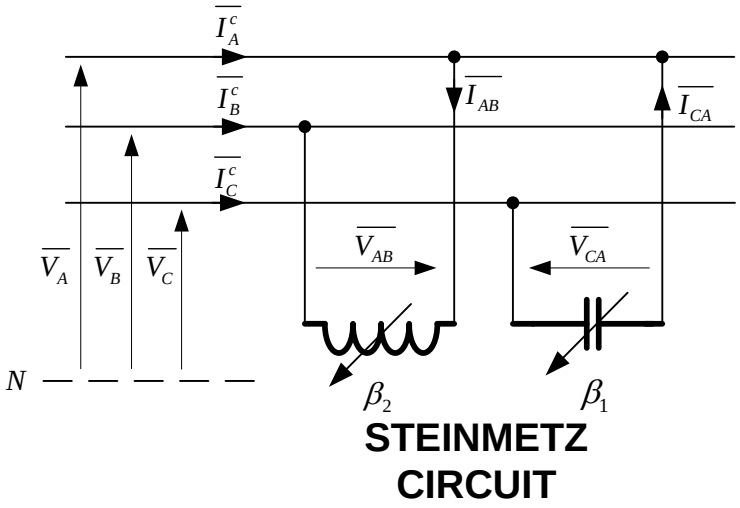


Fig. 84 - Active Steinmetz compensator.

In order to analyze the compensation capability of the active Steinmetz circuit, the simple schematic of figure 84 is considered. This figure shows the active Steinmetz circuit realized with an ideal variable inductor and capacitor.

The following hypotheses are assumed:

- Sinusoidal steady-state
- PWM AC-chopper converters are considered to be sinusoidal current generators at a grid frequency of 50 Hz, providing inductive and capacitive currents.
- The line voltage positive sequence is considered as the zero phase reference.
- The voltage drops on the line impedances are neglected.
- S_{CCI} and I are respectively the power rate and maximum current of the controlled impedances.

On this basis, the injected current magnitudes are:

$$I_{CA} = \beta_1 \frac{S_{CCI}}{V_{CA}} = \beta_1 I \tag{82}$$

$$I_{AB} = \beta_2 \frac{S_{CCI}}{V_{AB}} = \beta_2 I \tag{83}$$

with $0 \leq \beta_{1,2} \leq 1$.

These simplifications make it possible to carry out a symmetrical component analysis of the compensator circuit. Expressions (84) and (85) describe the injected currents in the complex domain.

$$\overline{I_{AB}} = \beta_1 I e^{j\left(\varphi_{V_{AB}} - \frac{\pi}{2}\right)} = \beta_1 I e^{-j\frac{\pi}{3}} \qquad 0 \leq \beta_1 \leq 1 \tag{84}$$

$$\overline{I_{CA}} = \beta_2 I e^{j\left(\varphi_{V_{CA}} + \frac{\pi}{2}\right)} = \beta_2 I e^{j\frac{4\pi}{3}} \qquad 0 \leq \beta_2 \leq 1 \tag{85}$$

In (86), the set of three-phase currents drawn by the compensator is represented (using superscript '*c*' to indicate compensator currents).

$$\begin{cases} \overline{I_A^c} = \overline{I_{AB}} - \overline{I_{CA}} = \beta_1 I e^{-j\frac{\pi}{3}} - \beta_2 I e^{j\frac{4\pi}{3}} = -\alpha\beta_1 I - \alpha^2\beta_2 I \\ \overline{I_B^c} = -\overline{I_{AB}} = -\beta_1 I e^{-j\frac{\pi}{3}} = \alpha\beta_1 I \\ \overline{I_C^c} = \overline{I_{CA}} = \beta_2 I e^{j\frac{4\pi}{3}} = \alpha^2\beta_2 I \end{cases} \qquad (86)$$

$$0 \le \beta_{1,2} \le 1$$

Applying transformation (13) to the set of compensation currents $\left[\overline{I_A^c} \quad \overline{I_B^c} \quad \overline{I_C^c}\right]$, the symmetrical components are obtained in (87) and (88). These represent the positive and negative sequences injected by the active Steinmetz compensator. A graphical representation of such symmetrical components is given in figure 85.

$$\overline{I_+^c} = \frac{1}{3}\left(\overline{I_A^c} + \alpha\overline{I_B^c} + \alpha^2\overline{I_C^c}\right) = \frac{1}{3}\left(-\alpha\beta_1 I - \alpha^2\beta_2 I + \alpha^2\beta_1 I + \alpha\beta_2 I\right) = \frac{1}{3}\left(I(\beta_1 - \beta_2)(\alpha^2 - \alpha)\right)$$
$$= j\frac{\sqrt{3}}{3} I(\beta_1 - \beta_2) \qquad (87)$$

$$\overline{I_-^c} = \frac{1}{3}\left(\overline{I_A^c} + \alpha^2\overline{I_B^c} + \alpha\overline{I_C^c}\right) = \frac{1}{3}\left(-\alpha\beta_1 I - \alpha^2\beta_2 I + \beta_1 I + \beta_2 I\right) = \frac{1}{3}\left(I\beta_1(1-\alpha) + I\beta_2(1-\alpha^2)\right)$$
$$= \frac{\sqrt{3}}{3} I\left(\beta_1 e^{-j\frac{\pi}{6}} + \beta_2 e^{j\frac{\pi}{6}}\right) \qquad (88)$$

Let us note that the active Steinmetz circuit draws a purely reactive positive sequence. Moreover, it is evident that it is not possible to independently control the positive and negative sequence components.

The last two characteristics represent the biggest drawback of the Steinmetz compensator. A more detailed discussion of this restriction is presented in the next sections.

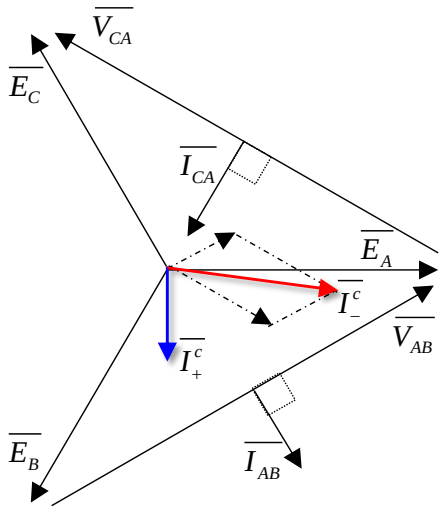


Fig. 85 - Symmetrical components of compensator currents.

IV.2.2 Current unbalance compensation

In this section, the current unbalance compensation capability of the proposed topology is analyzed. From this investigation, possible control laws for AC chopper converters are derived.

Focusing on equations (87) and (88), let us point out that the possible positions of the negative component vector in the complex plane are limited. Evaluating expression (88) for all of the admitted values for β_1 and β_2, the variation area of $\overline{I_-^c}$ is drawn in the complex plane of figure 86. It is evident that the phasor of the negative component is confined to the marked area. Consequently, the magnitude and phase variations are constrained. Particularly, the admissible values for the negative component phase are in the range $-\pi/6 \le \left(\angle \overline{I_-^c}\right) \le \pi/6$.

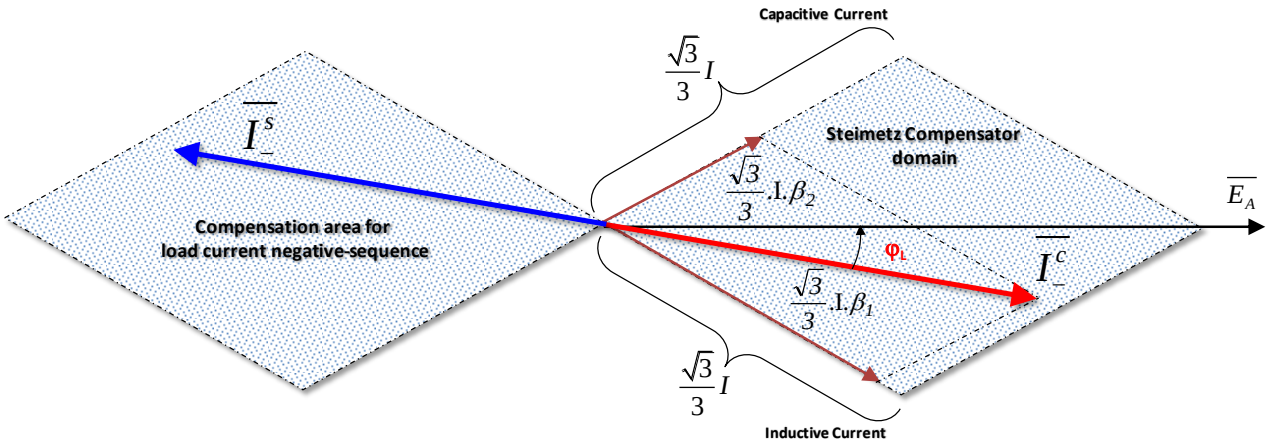


Fig. 86 - Negative component domain of compensator.

On this basis, the active Steinmetz compensator is able to compensate for the current unbalance caused by substation currents only in a limited region of the complex plane. Particularly, in order to have the completely instantaneous compensation defined by (89), the substation current must have a phase $-\pi/6 \le \varphi_L \le \pi/6$ and an admissible magnitude in the marked area of figure 86. The resultant negative component after compensation is shown in (90).

$$\overline{I_-^c} = -\overline{I_-^s} \tag{89}$$

$$\overline{I_-} = \frac{\sqrt{3}}{3} I \left(\beta_1 e^{-j\frac{\pi}{6}} + \beta_2 e^{j\frac{\pi}{6}} \right) - j\frac{\sqrt{3}}{3}\overline{I_L} \tag{90}$$

Equation (90) allows finding the values β_1 and β_2 that guarantee the current unbalance compensation. Solutions are given in (91) as a function of the substation current magnitude and phase. Alternative expressions for the β_1 and β_2 solutions are reported in (92), where P_L and Q_L are respectively the active and

reactive power of the substation. It should be noted that these equations are valid only for $\overline{I_{-}^{c}}$ in the marked area of figure 86.

$$\beta_1 = \frac{1}{I}\left(\frac{I_L\cos(\varphi_L)}{\sqrt{3}} + I_L\sin(\varphi_L)\right)$$
$$\beta_2 = \frac{1}{I}\left(\frac{I_L\cos(\varphi_L)}{\sqrt{3}} - I_L\sin(\varphi_L)\right) \qquad 0 \le \beta_{1,2} \le 1 \tag{91}$$

$$\beta_1 = \frac{1}{S_{CCI}}\left(\frac{P_L}{\sqrt{3}} + Q_L\right)$$
$$\beta_2 = \frac{1}{S_{CCI}}\left(\frac{P_L}{\sqrt{3}} - Q_L\right) \qquad 0 \le \beta_{1,2} \le 1 \tag{92}$$

IV.2.3 Voltage unbalance compensation

The Steinmetz circuit acts as negative sequence current compensator with the aim of reducing the negative sequence voltage of the power system at the PCC. The effect of the current unbalance on the voltage unbalance is clearly related to the 'strength' of the power transmission network, and so to its short-circuit power. The compensator task is easier in a grid with high short-circuit power than in the case of low short-circuit power.

In order to evaluate the voltage UF% after the Steinmetz circuit insertion, expression (19) is used. Particularly, the magnitude of the negative current component is found by (93). The magnitude of the positive current component is found by (94) and its phase by (95). The values of Z_{cc} and φ_{cc} depend on the short-circuit power.

$$I_{-} = \left|\overline{I_{-}^{c}} + \overline{I_{-}^{s}}\right| \tag{93}$$

$$I_{+} = \left|\overline{I_{+}^{c}} + \overline{I_{+}^{s}}\right| \tag{94}$$

$$\varphi_{I_+} = \angle\left(\overline{I_{+}^{c}} + \overline{I_{+}^{s}}\right) \tag{95}$$

IV.2.4 Three-phase power factor reduction

In addition to the needed negative sequence, the active Steinmetz circuit adds a purely reactive positive sequence, as described in (87).

If $\beta_1 = \beta_2$, the given positive sequence is zero. However, when $\beta_1 \neq \beta_2$, this component adds up with a 90° phase to the already existing positive sequence. Consequently, the compensator draws the reactive power described in (96), and the three-phase power factor is reduced. After the negative component compensation, the resulting $\tan(\varphi_{I_+})$ is as shown in (97).

$$Q_c = S_{CCI}(\beta_1 - \beta_2) \tag{96}$$

$$\tan(\varphi_{I_+}) = \frac{Q_c + Q_L}{P_L} \tag{97}$$

Condition $\beta_1 = \beta_2$ is verified only when the system is compensating for a substation current with a unitary power factor ($\varphi_L = 0$).

IV.2.5 Alternative control to avoid power factor degradation

The energy provider imposes penalties on the SNCF when ratio $Q_L/P_L = \tan(\varphi_L)$ is greater than 0.4. Therefore, the biggest drawback of the active Steinmetz compensator is that it makes it necessary to install a additional reactive power compensator to avoid penalties.

An alternative solution can be adopted. On the condition that the negative sequence current compensation ability is reduced, it is possible to control the active Steinmetz compensator so that the two active impedances draw the same current value. This makes it possible to guarantee condition $\beta_1 = \beta_2 = \beta$, and thus the three-phase power factor is not degraded. On this basis, the compensator is able to reduce just the real part of the negative current sequence. Thus, the compensation domain results are restricted to the real axis (figure 87).

The equations for duty cycles β_1 and β_2 in this control strategy are as follows (98).

$$\beta_1 = \beta_2 = \frac{1}{I}\frac{I_L\cos(\varphi_L)}{\sqrt{3}} = \frac{P_L}{S_{CCI}\sqrt{3}} \qquad 0 \le \beta_{1,2} \le 1 \tag{98}$$

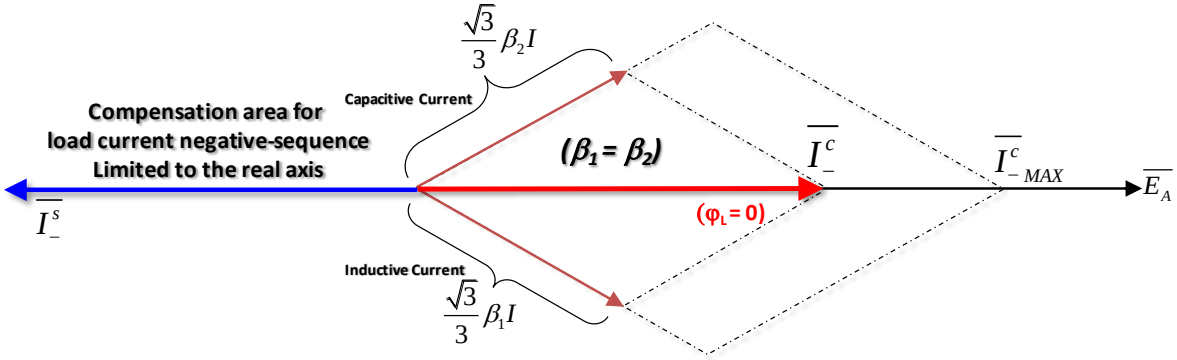


Fig. 87 - Compensation at PF = 1.

IV.2.6 Compensator Rating

The converter's rating depends on the requested compensation region. In particular, two design criteria are possible, according to the two control strategies previously introduced.

1) The compensator is sized to be able to compensate for loads with $0.8660 \le PF \le 1$.
2) The compensator is sized in order to reduce only the real part of the current negative component (load with PF = 1).

It is evident that in the second case, the compensator power rate results in a lower value than in the first case, but the compensation capabilities are reduced.

The following assumptions are made:

- S_L and φ_L are respectively the apparent power and phase of the reference load.
- S_{CCI} is the apparent power of each CCI.

IV.2.6.1 Rating at 0.8660 ≤ LOAD PF ≤ 1

Based on the sizing criteria, S_{CCI} is chosen to have an active Steinmetz compensator capable of compensating for the entire admitted region marked in figure 86. The compensator is rated in order to instantaneously compensate for a current unbalance caused by a load of S_L and a power factor greater than 0.8660. On this basis, each active impedance must be rated at the same power as load $S_{CCI} = S_L$.Thus, the Steinmetz compensator has twice the considered load power $(S_c = 2S_L)$.

IV.2.6.2 Rating at PF = 1

The sizing criteria include choosing S_{CCI} to have an active Steinmetz compensator that is able to compensate for the real part of the negative current sequence for a substation of power S_L. In any case, the compensator is able to partially reduce the negative current sequence for a load with PF ≠ 1.

From equation (98) for $\beta = 1$, it is possible to derive the CCI size*:*

$$S_{CCI} = \frac{\sqrt{3}}{3} S_L \approx 58\% S_L \tag{99}$$

The rate of each CCI is almost 58% of the load power. The complete Steinmetz compensator has 116% of the considered load power.

In conclusion, Table VI summarizes the two rating strategy results.

Table VI

Rating Strategy 1		Rating Strategy 2	
Total compensation for: Load Power S_L*;* Load Phase φ_L*=0*		Total compensation for: Load Power S_L*;* Load Phase -30°≤φ_L≤*30°*	
INDUCTIVE CCI	$\frac{\sqrt{3}}{3} S_L$	*INDUCTIVE CCI*	S_L
CAPACITIVE CCI	$\frac{\sqrt{3}}{3} S_L$	*CAPACITIVE CCI*	S_L
TOTAL ACTIVE STEINMETZ COMPENSATOR	$2\frac{\sqrt{3}}{3} S_L$	*TOTAL ACTIVE STEINMETZ COMPENSATOR*	$2S_L$

IV.3 Conclusions

This chapter presented a new topology for a voltage unbalance compensator based on CCI. The structure of the proposed balancer is an active Steinmetz circuit realized by means of PWM AC-choppers.

Despite the limited compensation domain of the presented topology with respect to a VSI-based compensator, it represents an interesting solution for railway applications, where an average compensation is enough to satisfy power quality requirements.

It will be shown that the most interesting features of this compensator structure involve its economic benefits. The AC-chopper converter presents low losses in semiconductor devices, making this solution

attractive in terms of cost. Moreover, this solution is characterized by a reduced size for the reactive elements compared to a VSI-based topology.

These aspects are treated in the next chapter, where comparative studies between the proposed topology and VSI unbalance compensator are carried out for a real case study.

Chapter V. **Evron substation Power Quality analysis**

The application of the active Steinmetz balancer is investigated in a case study. A substation of French Railways is considered. A measurement campaign obtained useful information regarding the unbalance compensator rating.

V.1 Evron substation

The case study involves a French substation located in Evron (Pays de la Loire). The scheme for the substation is presented in figure 88. For redundancy reason, two 16 MVA single-phase transformers are wired in parallel. The primaries are phase-to-phase connected to a 90 kV/50 Hz transmission line, and a 2.7 MVAR reactive power compensation bank is connected on the 25 kV side.

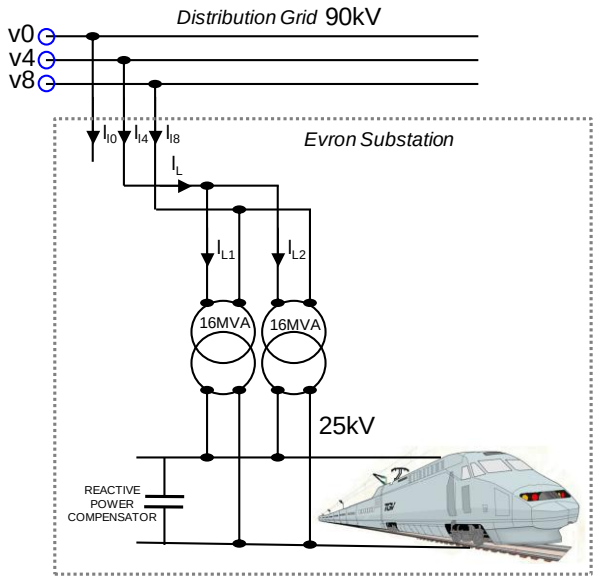


Fig. 88 - Evron substation.

For the voltage unbalance at the PCC, the following limits are considered:
- for Scc ≥ 575 MVA [*usual conditions*]: UF% ≤ **1%** on a 10 min average
- for 295 MVA ≤ Scc < 575 MVA [*degraded mode*]: UF% ≤ 1.**5**% on a 10 min average

A nominal short-circuit power of 700 MVA is assumed. Moreover, a short-circuit impedance phase of 80° is considered in the study.

V.2 Measurements

Two analyses were performed on the basis of electrical measurements at the primary side of the substation. First, active and reactive power measurements carried out over 6 years gave information about the load variation, which is useful for the unbalance compensator rating.

Afterward, current and voltage instantaneous waveforms were recorded during 2 h. The goal was to get information on the working conditions of the unbalance compensator to evaluate harmonic interactions.

V.2.1 SNCF power records for several years

Power measurements at the Evron substation over several years are available from SNCF. Figure 89 shows the active and reactive power averaged for 10-min periods from 01/01/2005 to 22/11/2010. The apparent power, S_L, is calculated and plotted in figure 90.

In order to choose the compensator size, it is interesting to make some statistical considerations on the trend of the variation in S_L. On this basis, figure 91 displays a plot of the empirical cumulative distribution function (cdf) for the data in vector X, where X represents S_L values. The empirical cdf is defined as the probability that random variable X takes on a value less than or equal to x as expressed in (100). Moreover, figure 92 reports a histogram showing the distribution of stored S_L values.

$$x \to F(x) = \mathrm{P}(X \le x) \tag{100}$$

A statistical analysis shows that 99.7% of the recorded values are under 10 MVA. Thus, S_L = 10MVA was considered as the reference load for unbalance compensator rating.

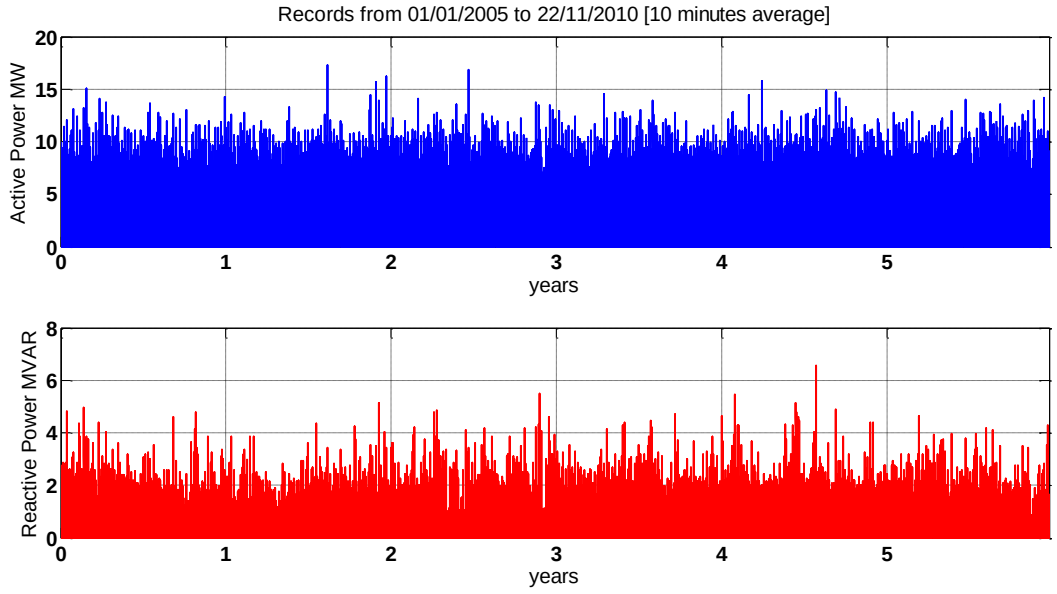


Fig. 89 –10-min averaged active and reactive power values of Evron substation over several years.

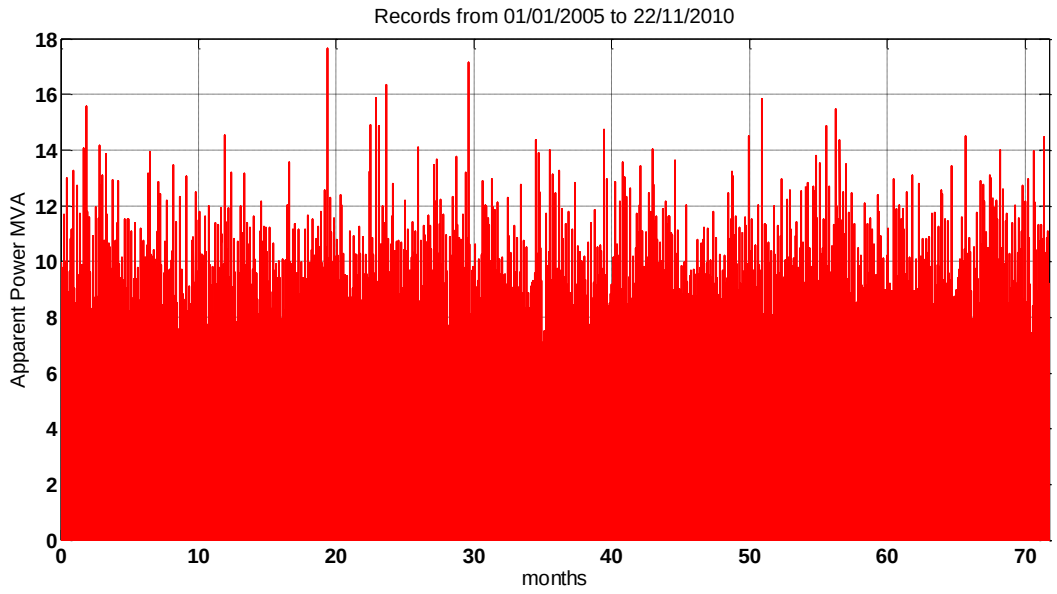


Fig. 90 – 10-min averaged apparent power of Evron substation over several years.

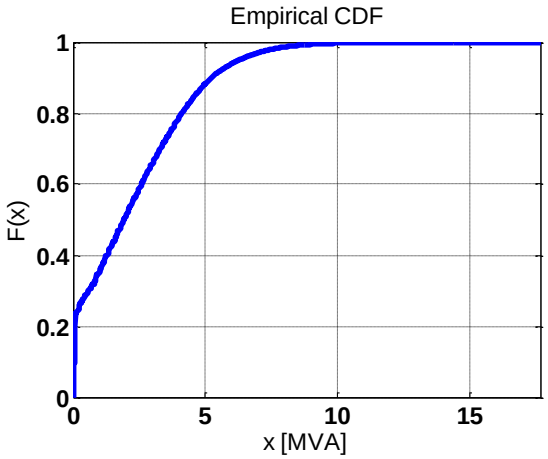


Fig. 91 - Cumulative distribution function of S_L samples.

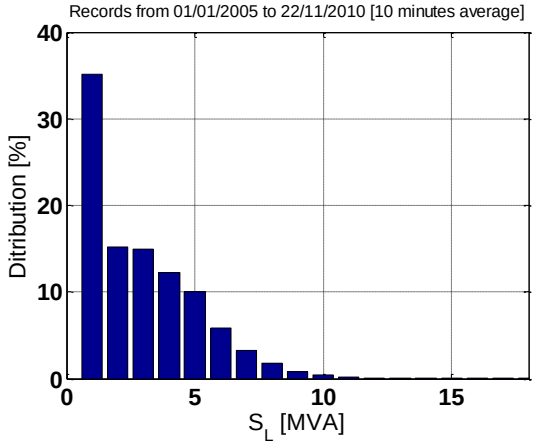


Fig. 92 - Statistical distribution of S_L samples.

V.2.2 Measurements

In order to perform an analysis of the symmetrical components, voltage and current measurements were made at the substation PCC. Current i_l and voltages v_0, v_4, and v_8 were recorded.

Measurements were carried out in two 1-h periods using a data acquisition system with a sampling frequency of 5 kHz per channel:

Case A) 8 July 2010 / 14:55:46 – 15:55:47 / Measure with reactive power compensator connected

Case B) 8 July 2010 / 16:14:59 – 17:15:00 / Measure with reactive power compensator disconnected

The following figures show the measurement results:

- figure 93: line voltages in case A,
- figure 94: substation current i_L in case A,

- figure 95: line voltages in case B,
- figure 96: substation current i_L in case B.

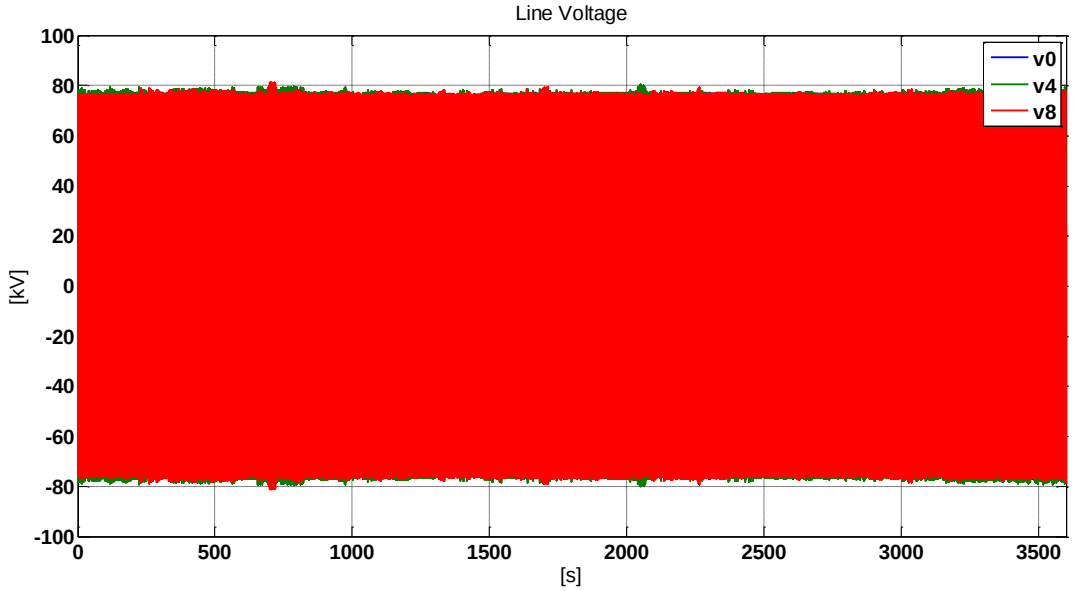


Fig. 93- Line voltages in case A.

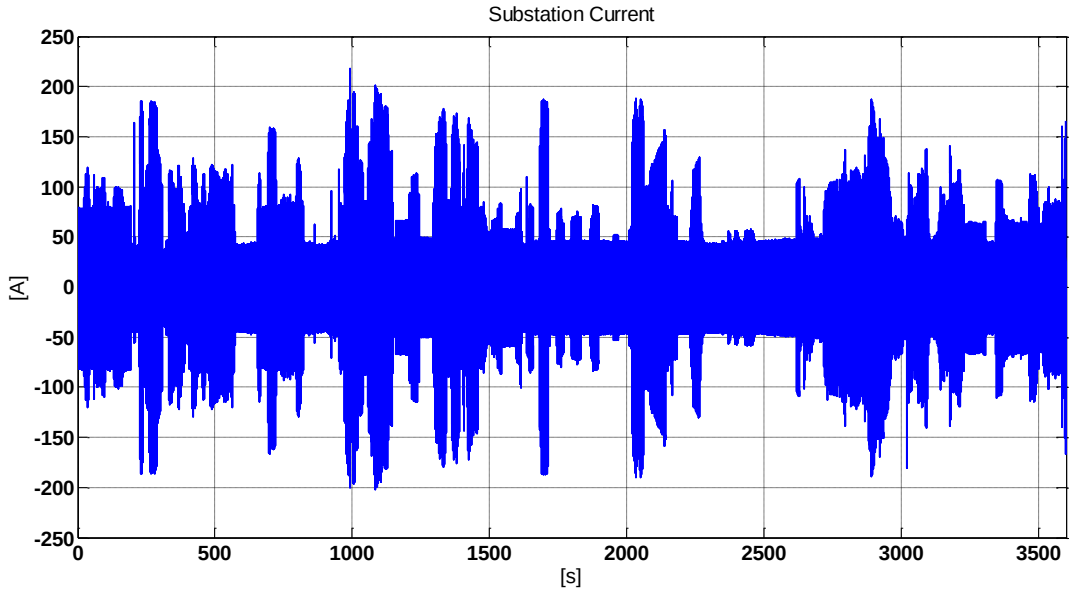


Fig. 94 - Substation current in case A.

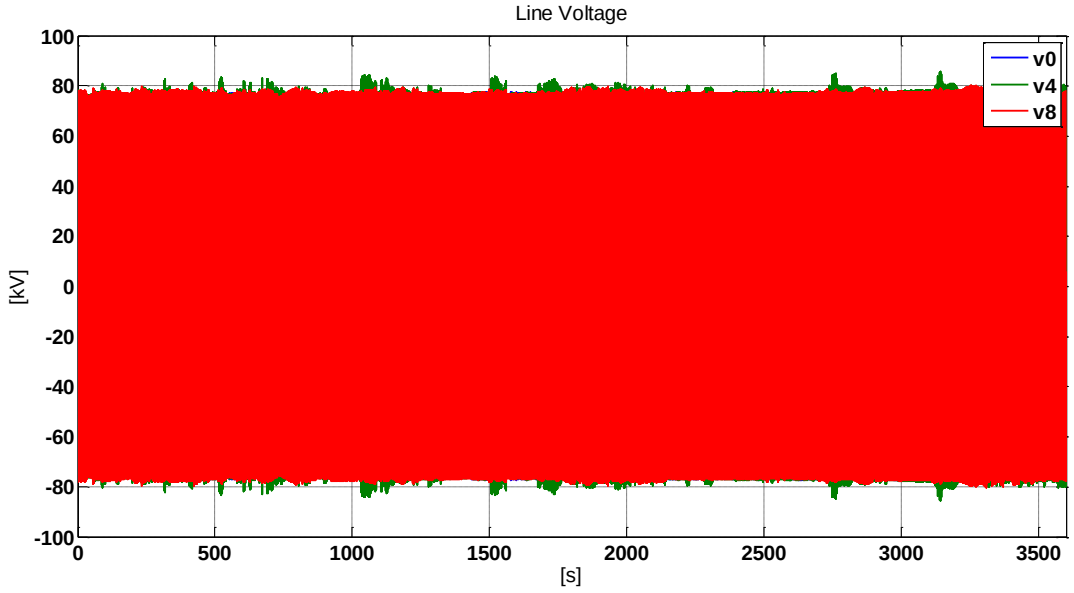


Fig. 95 - Line voltages in case B.

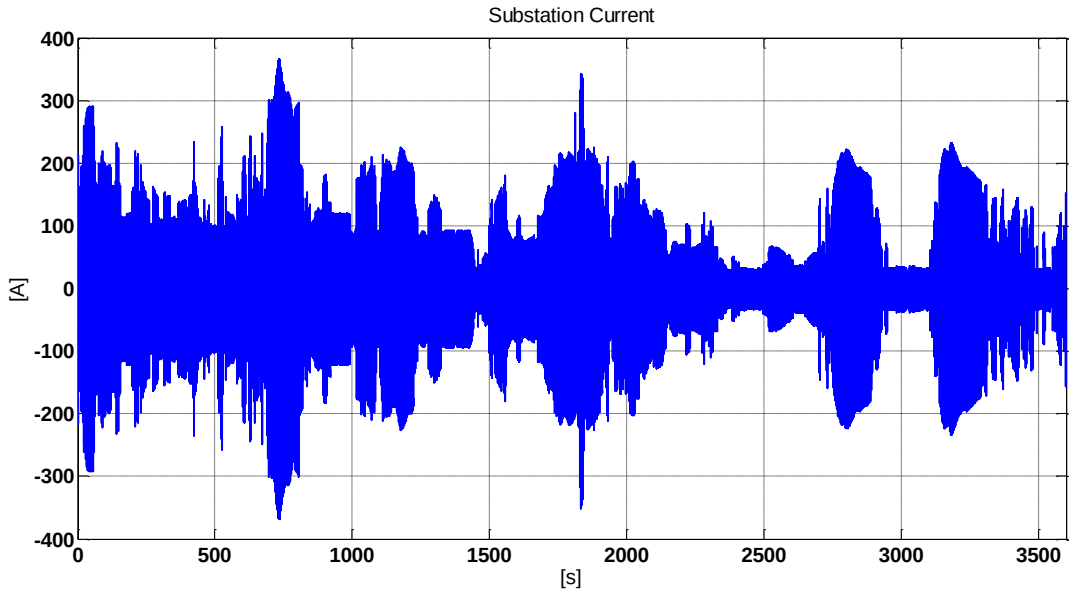


Fig. 96 - Substation current in case B.

V.2.3 Spectral Analysis

A spectral analysis of substation current i_L is carried out by performing a Fourier series decomposition. The following expression is considered:

$$i_L(t) = \sum_{n=1}^{\infty} \left[a_i(n) \cdot \cos\left(2\pi n f_0 t\right) + b_i(n) \cdot \sin\left(2\pi n f_0 t\right) \right] \tag{101}$$

where a_i and b_i are the Fourier coefficients, n is the harmonic rank and f_0 is the grid frequency.

A discrete algorithm is used to evaluate coefficients a_i and b_i for each grid period 1/ f_0. On this basis, the amplitudes of the substation current harmonics are expressed as (102).

$$\hat{I}_L(n) = \sqrt{a_i(n)^2 + b_i(n)^2} \tag{102}$$

The odd rank harmonic magnitudes for measurements A and B are reported, respectively, in figures 97 and 98. The maximum current amplitudes are calculated and reported in figures 99 and 100. The last figures highlight that the third harmonic of the substation current can reach 50 A. This must be considered when a converter has to be installed in a substation.

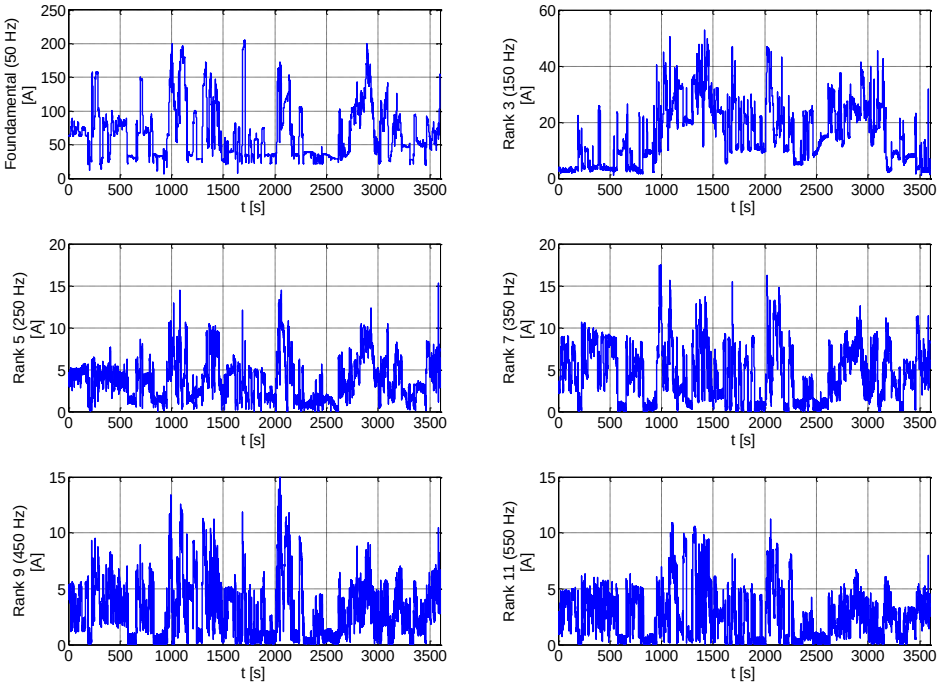


Fig. 97 – Odd rank harmonics in substation current - Case A.

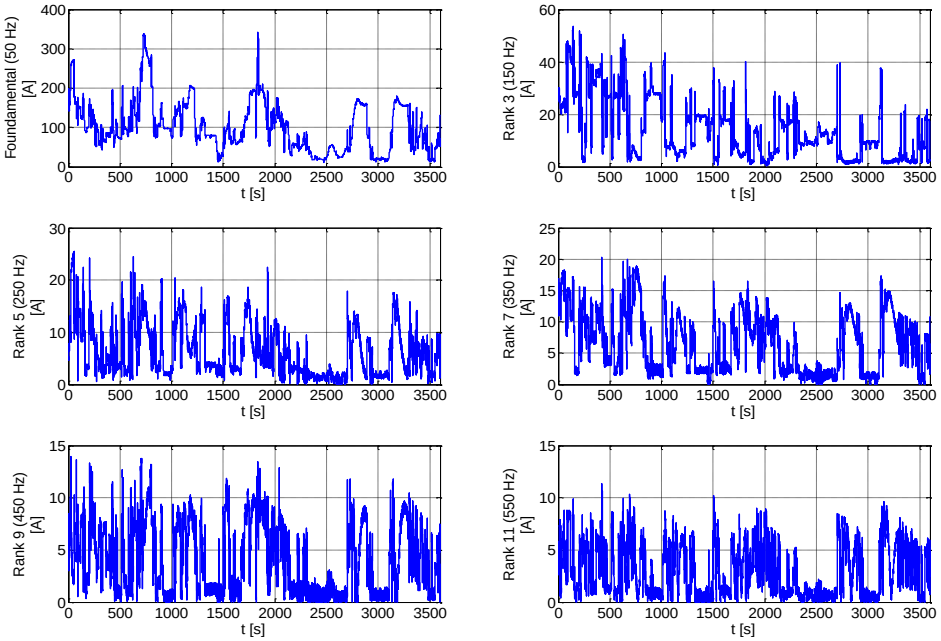


Fig. 98 - Odd rank harmonics in substation current - Case B.

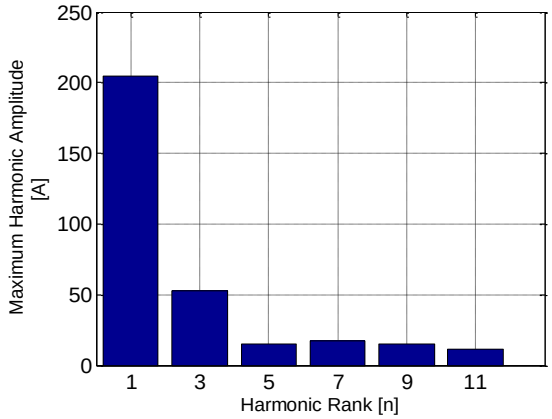


Fig. 99 – Maximum Harmonic amplitude for case A.

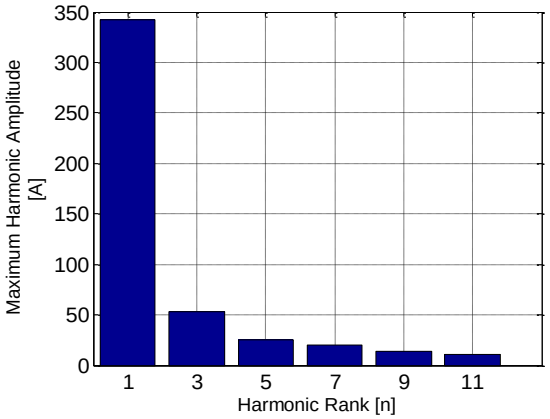


Fig. 100 - Maximum Harmonic amplitude for case B..

A Fourier analysis was also carried out for the records of line voltages v_{04}, v_{48} and v_{80}. The results are shown in figure 101 for case A and figure 102 for case B.

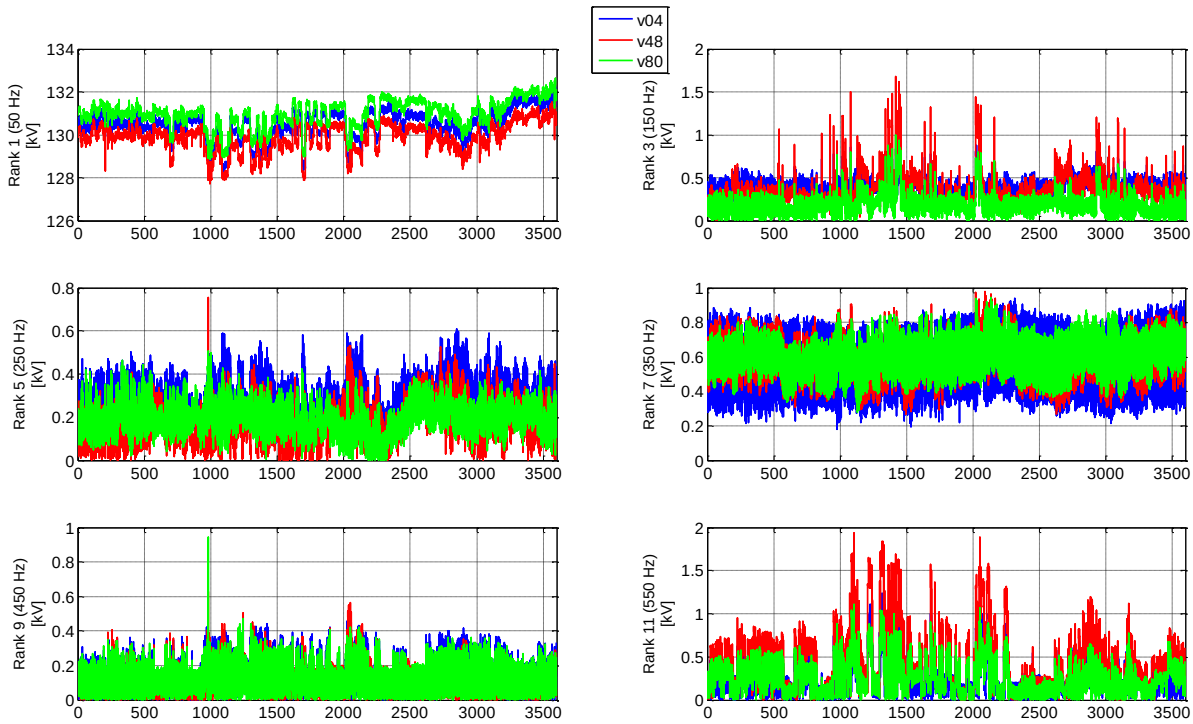


Fig. 101 - Odd rank harmonics in line voltages (Case A).

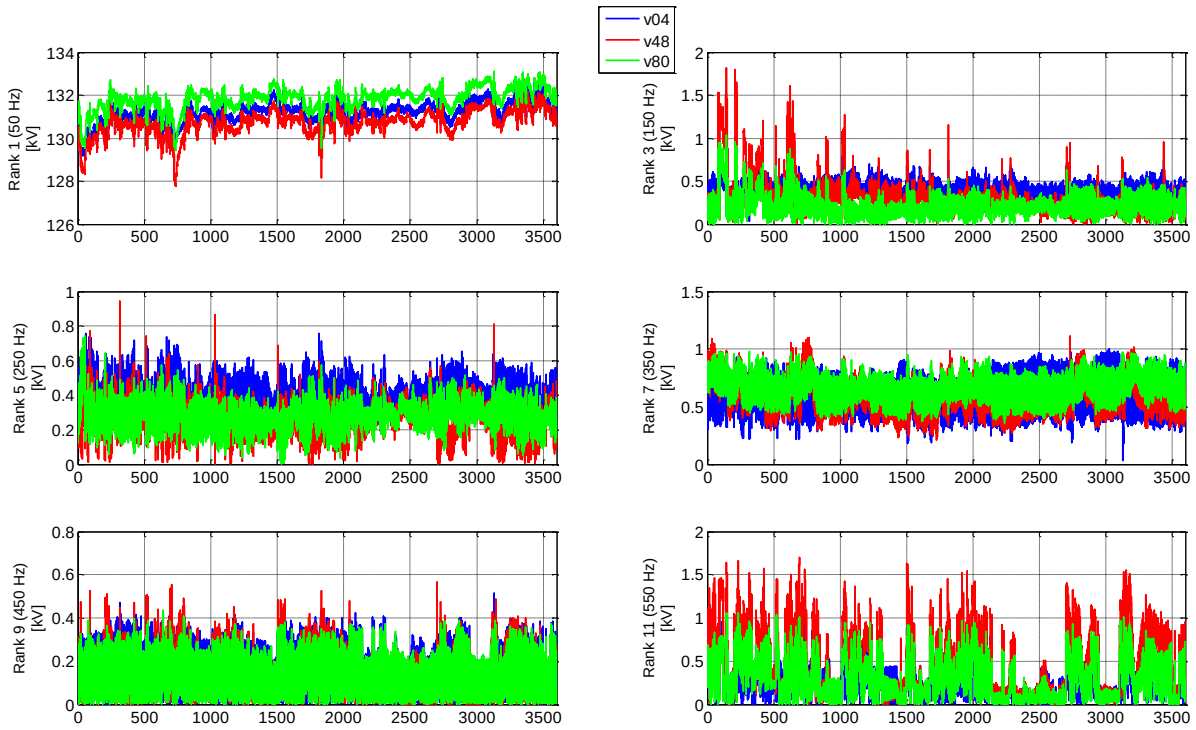


Fig. 102 - Odd rank harmonics in line voltages (Case B).

From the fundamental component of voltage v_{48} and current i_L, it is possible to evaluate the active and reactive power drawn by the substation.

Considering the fundamental voltage:

$$v_{48}(t) = a_v(1)\cdot\cos(2\pi f_0 t) + b_v(1)\cdot\sin(2\pi f_0 t) \tag{103}$$

The rms value is expressed as:

$$V_{48}(1) = \sqrt{\frac{a_v(1)^2 + b_v(1)^2}{2}} \tag{104}$$

The rms value of the substation current is:

$$I_L(1) = \sqrt{\frac{a_i(1)^2 + b_i(1)^2}{2}} \tag{105}$$

The phase displacement between the fundamental voltage and current:

$$\varphi_1 = \arctan\left(\frac{b_v(1)}{a_v(1)}\right) - \arctan\left(\frac{b_i(1)}{a_i(1)}\right) \tag{106}$$

Then, the active and reactive power are:

$$P_L = V_{48}(1)\cdot I_L(1)\cdot\cos(\varphi_1) \tag{107}$$

$$Q_L = V_{48}(1)\cdot I_L(1)\cdot\sin(\varphi_1) \tag{108}$$

The following figures show evaluations of the active and reactive power:

- figure 103: active and reactive power of substation in case A,
- figure 104: active and reactive power of substation in case B.

A active power peak of about 20 MW was recorded during the measurements for B.

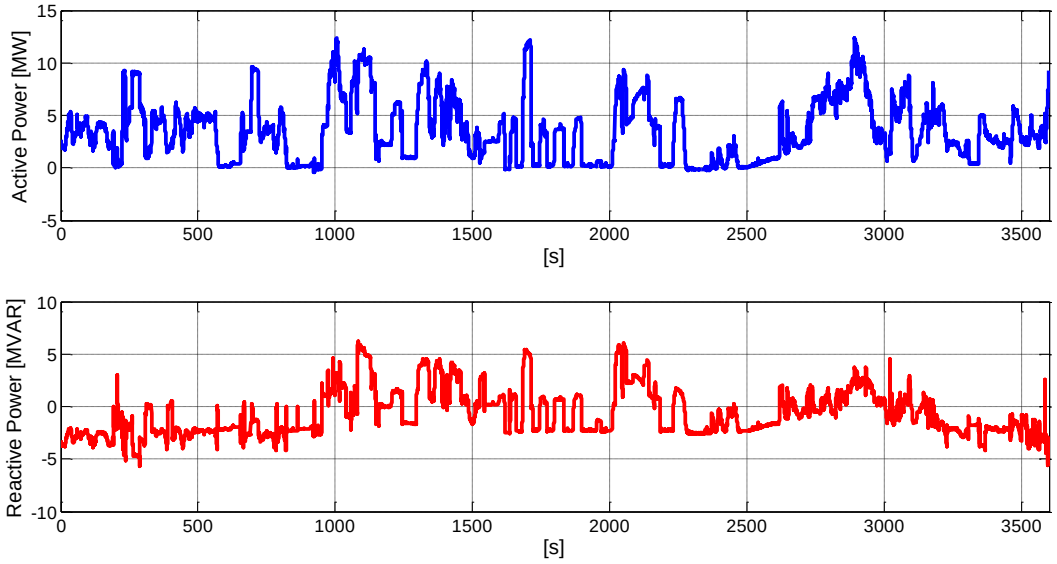


Fig. 103 - Active and reactive power of substation in case A.

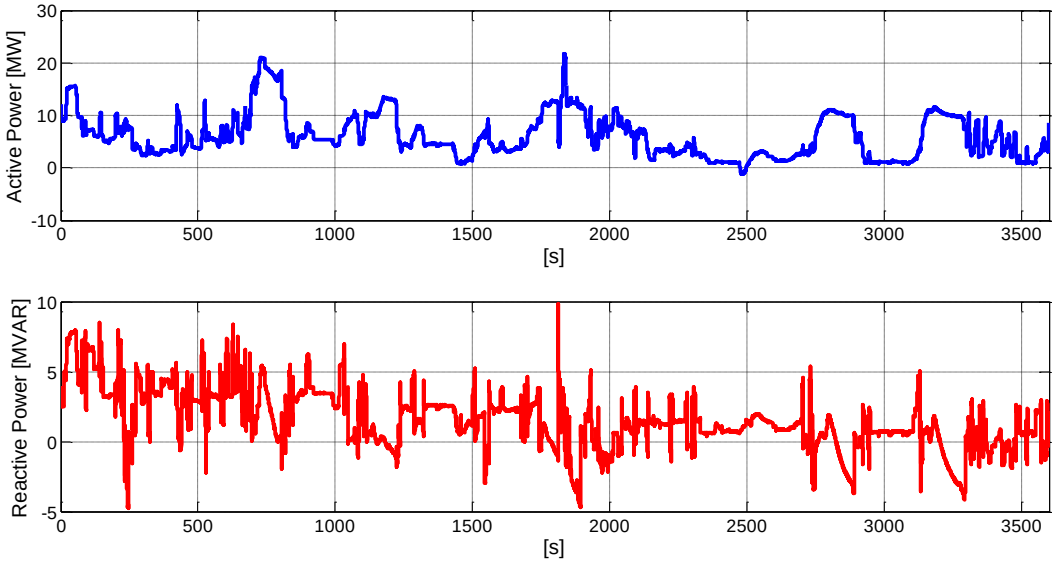


Fig. 104 - Active and reactive power of substation in case B.

V.2.4 Symmetrical components analysis

After processing the voltage and current records, an analysis of the Fortescue symmetrical components was performed. The algorithm used to extract the positive and negative current sequences was implemented in Simulink. The simple scheme of the algorithm is shown in figure 105.

Let us consider fundamental line voltages composed of a positive sequence and negative sequence, as in (109). The zero-sequence has been neglected due to the absence of a neutral wire.

$$\begin{cases} v_0 = V_P \sin(\theta_P) + V_N \sin(\theta_N) \\ v_4 = V_P \sin\left(\theta_P - \frac{2\pi}{3}\right) + V_N \sin\left(\theta_N + \frac{2\pi}{3}\right) \\ v_8 = V_P \sin\left(\theta_P + \frac{2\pi}{3}\right) + V_N \sin\left(\theta_N - \frac{2\pi}{3}\right) \end{cases} \tag{109}$$

$$\theta_P = \omega t + \varphi_P \quad \theta_N = \omega t + \varphi_N$$

The positive sequence angle, θ_P, is detected using a three-phase PLL system. Particularly, the Matlab Simulink PLL is used.

Applying the Park transformation (110) to (109) using the PLL output phase, the result is reported in (111).

It is clear from (111) that the DC components of v_d and v_q are respectively the real and imaginary parts of the positive sequence component. Thus, the last one can be extracted by applying a low-pass filter.

If the park transform is applied using angle $\theta_{PLL} = -\theta_P$, the results are as reported in (112). Thus, the *d* and *q* DC components represent the real part (opposite) and imaginary part of the negative sequence component.

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} \frac{2}{3}\cos(\theta_{PLL}) & \frac{2}{3}\cos\left(\theta_{PLL} - \frac{2\pi}{3}\right) & \frac{2}{3}\cos\left(\theta_{PLL} + \frac{2\pi}{3}\right) \\ \frac{2}{3}\sin(\theta_{PLL}) & \frac{2}{3}\sin\left(\theta_{PLL} - \frac{2\pi}{3}\right) & \frac{2}{3}\sin\left(\theta_{PLL} + \frac{2\pi}{3}\right) \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \begin{bmatrix} v_0 \\ v_4 \\ v_8 \end{bmatrix} \tag{110}$$

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} V_P \cos(\varphi_P) - V_N \cos(2\omega t + \varphi_N) \\ V_P \sin(\varphi_P) + V_N \cos(2\omega t + \varphi_N) \\ 0 \end{bmatrix} \tag{111}$$

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \begin{bmatrix} -V_N \cos(\varphi_N) + V_P \cos(2\omega t + \varphi_P) \\ V_N \sin(\varphi_N) + V_P \cos(2\omega t + \varphi_P) \\ 0 \end{bmatrix} \tag{112}$$

The results obtained from the presented Simulink model are shown in the following figures:

- Figure 106: magnitude of substation negative-sequence current in case A,
- Figure 107: position of negative component in complex plane in case A,
- Figure 108: magnitude of substation negative-sequence current in case B,

- Figure 109: position of negative component in complex plane in case B.

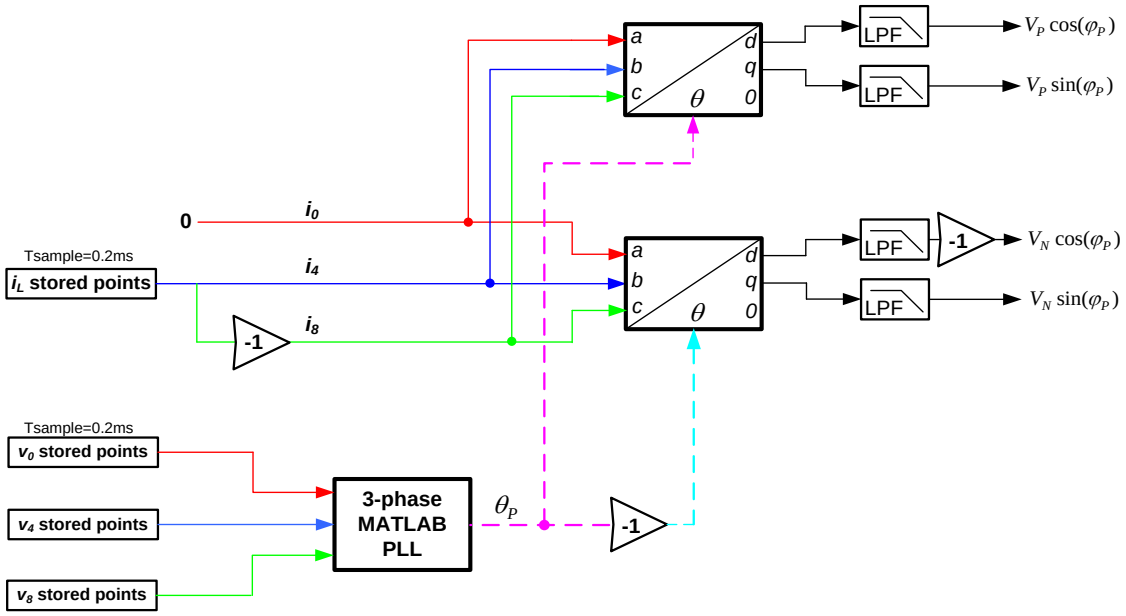


Fig. 105 - Simulink model for symmetrical component calculation.

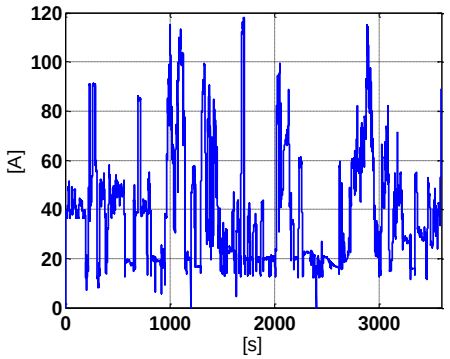


Fig. 106 – Substation negative current sequence magnitude (Case A).

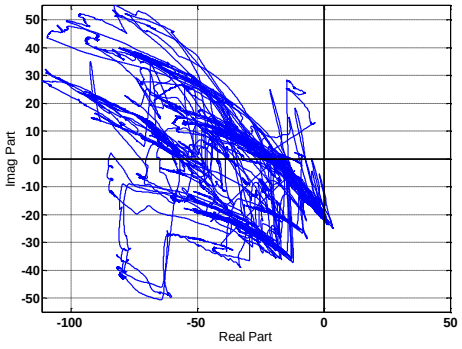


Fig. 107 - Substation negative current sequence in complex plane (Case A).

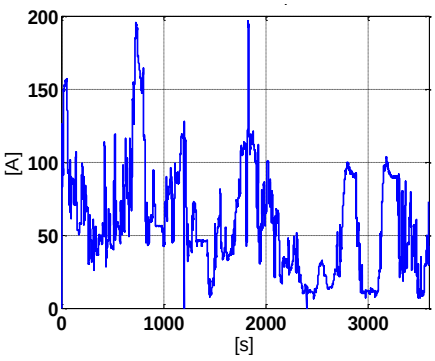


Fig. 108 - Substation negative current sequence magnitude (Case B).

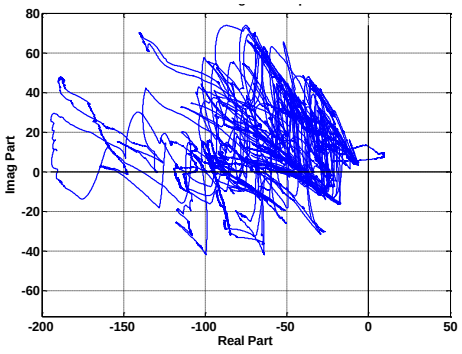


Fig. 109 - Substation negative current sequence in complex plane (Case B).

The maximum peak for the negative current component is about 180 A, which corresponds to the maximum recorded active power (20 MW).

V.3 Conclusions

The chapter presented results from a campaign of measures carried out at the substation of Evron.

Power measurements permit to perform statistical consideration useful in choosing the compensator rate. In that particular case, the compensator rating will be performed on the base of a substation load of 10MVA. Moreover, power quality analysis on measures allow to get information regarding the compensator design in terms of frequential behaviour.

Chapter VI.

Voltage Unbalance compensation in Evron substation

The chapter presents a comparative analysis between the active Steinmetz balancer and a more diffused solution based on a VSI converter in terms of the power losses and energy stored in the reactive elements. On this basis, the advantages and drawbacks of the balancer based on CCI are highlighted. The Evron substation is used as a case study.

The design methodology for the active Steinmetz compensator is illustrated. Finally, simulation results using measured waveforms are presented.

VI.1 Voltage Unbalance compensation in Evron substation based on Voltage Source Inverter

In this section, the use of a voltage balancer based on a VSI topology is considered. First, the sizing criteria are presented. After this, the power losses are evaluated for the two-level and three-level NPC topologies.

VI.1.1 Compensator rating

The aim is to determine the size, S_c, of the VSI compensator. A reference load of S_{Lref} = 10 MVA is considered in the sizing criteria.

The compensator must be able to provide a VUF% under limits when the substation is feeding a load of S_{Lref} or, similarly, a 10-min average load of S_{Lref}.

Figure 110 shows the voltage unbalance factor at the PCC versus the compensator size, S_c, for different short-circuit power values of the transmission line (295 MVA, 575 MVA and 700MVA). A unity power factor load is considered.

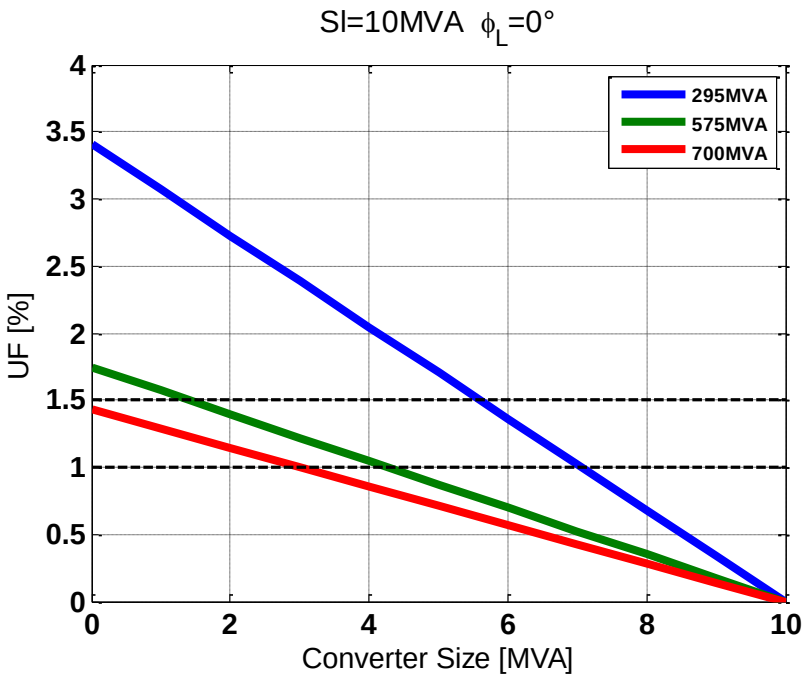


Fig. 110 – Voltage unbalance factor vs. compensator size.

In the rating criteria, the worst case of a weak grid (short-circuit power of 295 MVA) is taken into account. Two strategies are possible. The compensator is sized in order to guarantee a voltage unbalance factor of 1.5% for a substation load of 10 MVA, $\varphi_L = 0°$ (average compensation). In this case, the converter size is S_c = 5.7 MVA

The alternative is to rate the compensator with a view toward guaranteeing a voltage unbalance factor of 0% for a substation load of 10 MVA, $\varphi_L = 0°$ (total compensation). The converter size for this case is S_c = 10 MVA.

VI.1.2 Compensator design and power losses

In this section, the compensator design stage is introduced, and the power losses in the semiconductor devices are calculated. Moreover, simulations using the PSIM software are presented as a means to validate the analytical results.

Only the average compensation case is considered because it represents a more interesting solution in terms of minimizing the costs.

Figure 111 presents the structure of the compensator based on VSI converters.

The IGBT taken under consideration is the commercial ABB single module, model 5SNA 1500E330300. The thermal specifications for this component (see appendix AI) show that the maximum negative current at the thermal limit of the converter is 508 A in the case of VSI 2-L and 485A in the case of VSI NPC 3-L.

The following assumptions are made:

- The converter is supposed to work at its thermal limit (100C° heatsink–125°C junction).
- The DC voltage for the converters is chosen as the maximum allowed value based on the IGBTs used (1800 V).

- The transformer ratio is chosen in order to give the maximum voltage allowed at the secondary side with a view toward current controllability.
- The inductor is chosen in order to guarantee a maximum current ripple of 15%.
- The DC link capacitor is chosen to limit the voltage ripple to 5% (see appendix AII).

Equations for the converter design and loss evaluation are presented in the appendix AI.

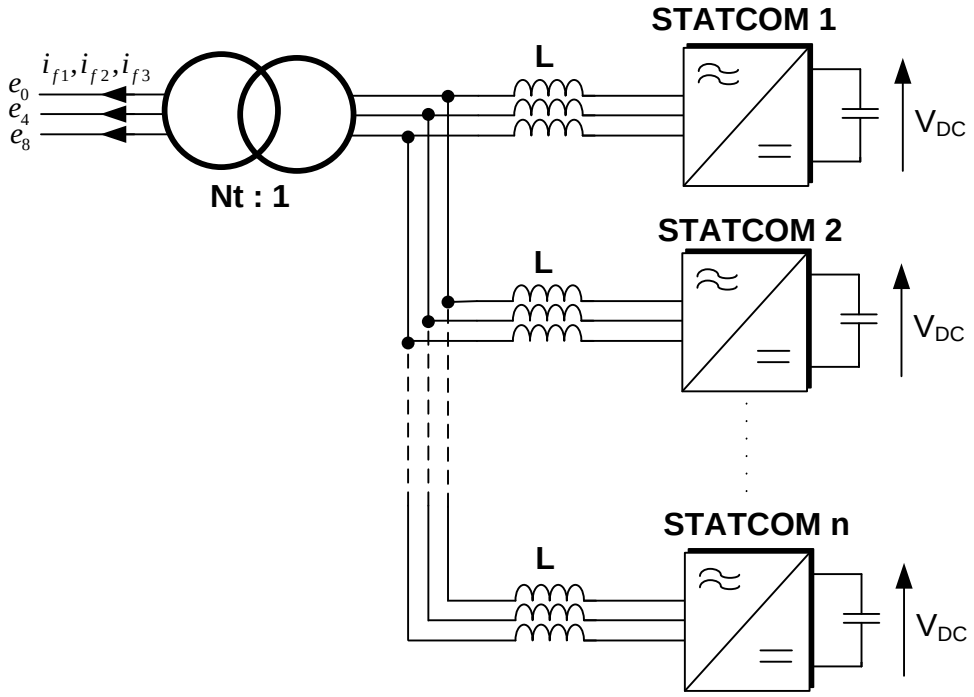


Fig. 111 – Unbalance compensator based on VSI topology parallelization.

VI.1.2.1 2-level VSI topology

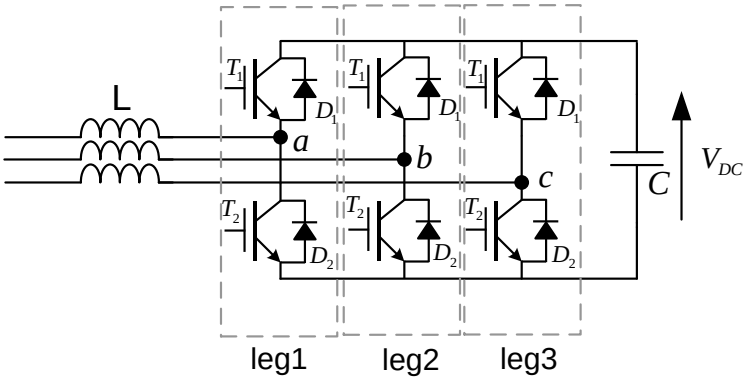


Fig. 112 – 2-level VSI module.

Figure 112 shows the single module for the VSI 2-L topology. The parameters for the compensator are summarized in Table VII. The loss calculations are reported in Table VIII. The considered cases refer to the worst case of a negative current at 60°.

Transformer ratio N_t	172
Primary phase-to-ground voltage	90e3/sqrt(3)V
Secondary phase-to-ground voltage	303 V
DC Voltage	1800 V
Maximum current for each STATCOM at thermal limits	508 A
Inductor L	2.1 mH
DC capacitor C	8.6 mF
Compensator size	5.7 MVA
Transformer secondary current	6289 A
Number of STATCOM modules in parallel	13
Current in each STATCOM	484 A

Table VII - Compensator design parameters for 2-level VSI topology.

3-phase 2-level VSI 484 A phi = 60°	Conduction Power losses [W]	Switching Power losses [W]	Junction Temperature [°C]
IGBT leg1	254	808	118.6
Diode leg1	137	454	120.7
IGBT leg2	254	808	118.6
Diode leg2	137	454	120.7
IGBT leg3	131	808	116.4
Diode leg3	233	454	124
Total Leg1	3306 W		
Total Leg2	3306 W		
Total Leg3	3252 W		
Total Losses	9864 W		

Table VIII - VSI 2-L Power Losses

VI.1.2.1.1 PSIM Simulation

In order to validate the analytical calculations carried out in the previous section, a single module of a three-phase STATCOM based on VSI 2-L is simulated in PSIM. Using the thermal module tool of the simulation software, it is possible to simulate the thermal behaviour of the IGBT's devices.

Figure 113 shows the drawn currents, negative current magnitude and phase. Figure 114 reports the power losses for the three inverter legs evaluated by means of the thermal module. Because of the symmetry, only one IGBT per leg is considered. Finally, figure 115 shows the total power losses for each inverter leg.

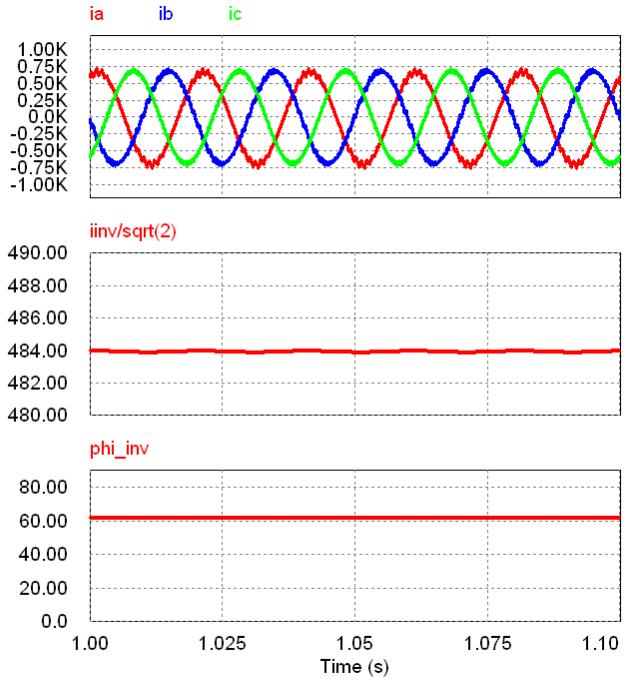


Fig. 113 – Injected currents, negative component module and phase in case of VSI 2-L .

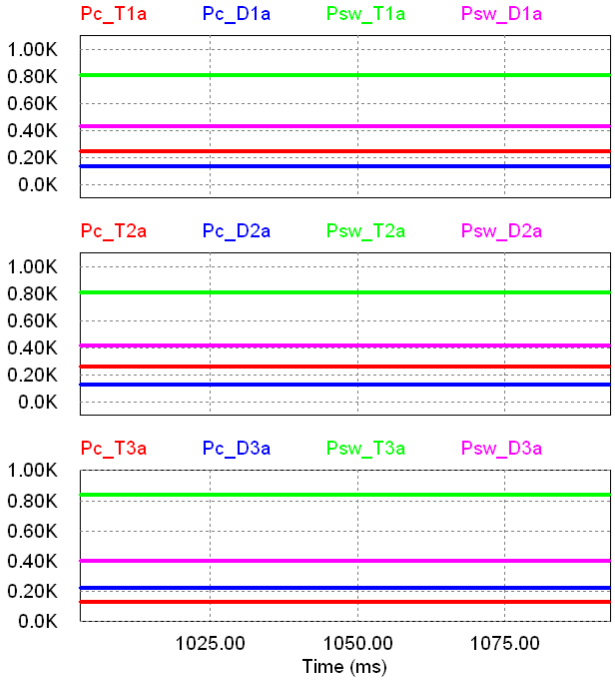


Fig. 114 – Devices power losses in case of VSI 2-L.

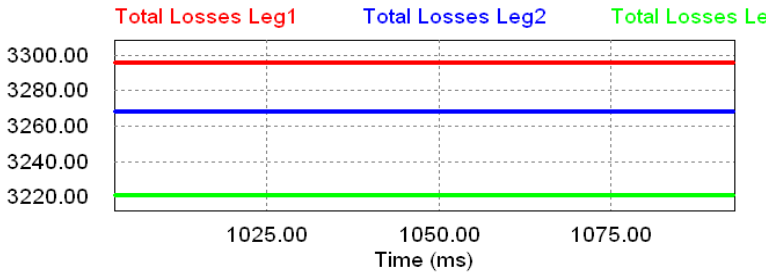


Fig. 115 –Total power losses in case of VSI 2-L strategy A.

VI.1.2.2 3-level NPC VSI topology

The compensator parameters for the case of the VSI NPC 3-L topology are summarized in Table IX. The scheme of the considered converter module is shown in figure 116.

The loss calculations are reported in Table X. The case considered refers to the worst case of a negative current at 80° (see appendix).

Transformer Ratio	86
Primary phase-to-ground voltage	90e3/sqrt(3)V
Secondary phase-to-ground voltage	606 V
DC voltage	3600 V
Maximum current for each STATCOM at thermal limits	485 A
Inductor L	4.4 mH
DC capacitor C	15 mF
Compensator size	5.7 MVA
Transformer secondary current	3144 A
Number of STATCOM modules in parallel	7
Current in each STATCOM	449 A

Table IX - Compensator design parameters for 3-level NPC VSI topology.

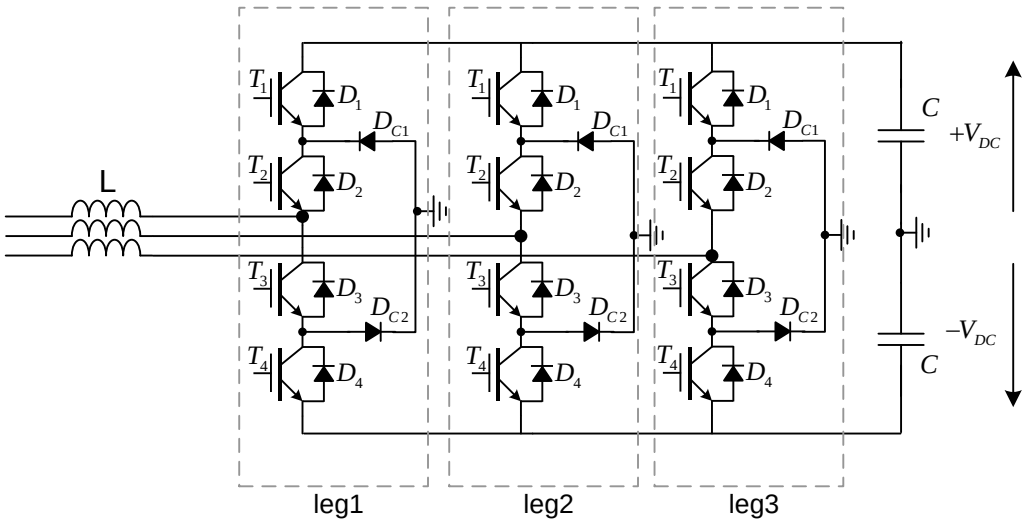


Fig. 116 – 3-level NPC VSI module.

3-phase VSI NPC 3-level 449A phi = 80°		Conduction Power losses [W]	Switching Power losses [W]	Junction Temperature [°C]
Leg 1	IGBT1	26	750	113.6
	Diode1	0	13	100.4
	IGBT2	384	24	107.1
	Diode2	0	0	100
	Clamp Diode	288	423	124.9
Leg 2	IGBT1	145	525	111.7
	Diode1	27	150	106.2
	IGBT2	352	250	110.5
	Diode2	27	0	100.9
	Clamp Diode	165	296	116.1
Leg 3	IGBT1	17	200	103.8
	Diode1	125	362	117
	IGBT2	227	578	114
	Diode2	125	0	104.4
	Clamp Diode	168	111	109.8
Total Leg1		3816W		
Total Leg2		3875W		
Total Leg3		3826W		
Total Losses		11517W		

Table X - VSI NPC 3-L power losses.

VI.1.2.2.1 PSIM simulation

In addition, in the case of 3-L NPC converters, in order to validate the analytical evaluation of the power losses, a single module of the three-phase STATCOM is simulated in PSIM. A STATCOM injecting a negative current sequence of 449 A and phase 80° is simulated. Figure 117 shows the drawn currents, negative current magnitude and its phase. Figures 118, 119 and 120 report the power losses for the three inverter legs simulated by means of the thermal module. Because of the symmetry, only one switching cell per leg is considered. Finally, figure 121 shows the total power losses for each inverter leg. The simulation results and analytical results match quite well.

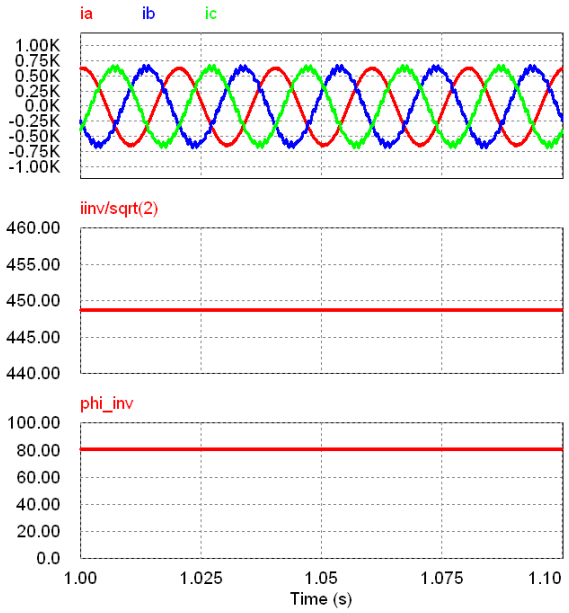


Fig. 117 - Injected currents, negative component module and phase in case of NPC 3-L VSI.

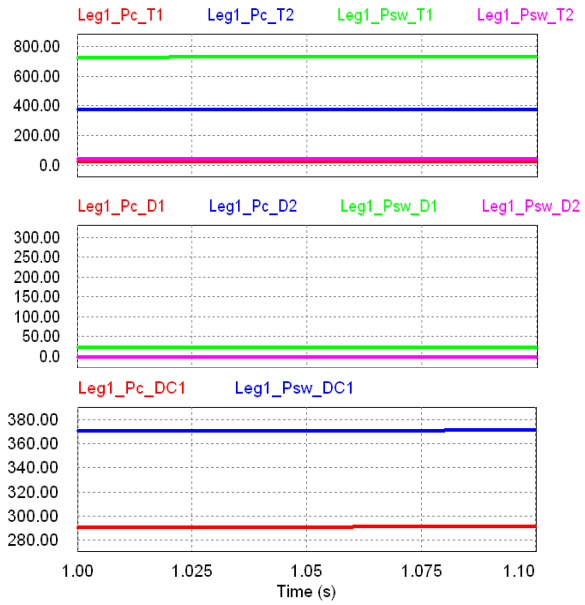


Fig. 118 - Devices power losses in leg 1.

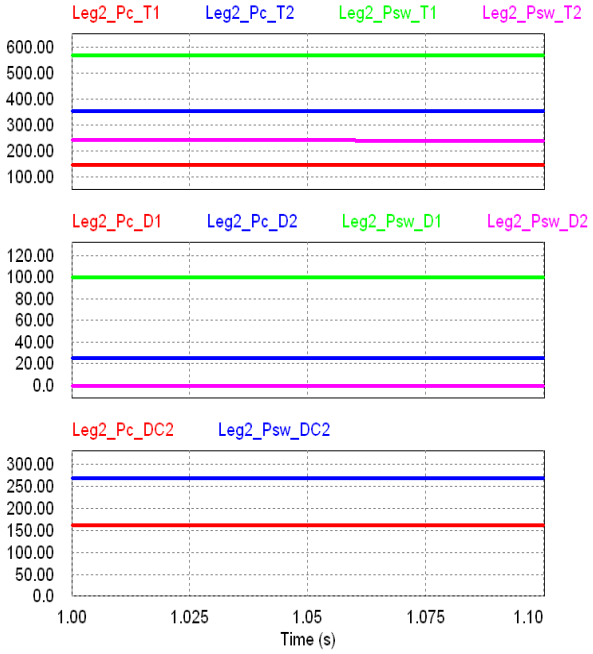


Fig. 119 - Devices power losses in leg 2.

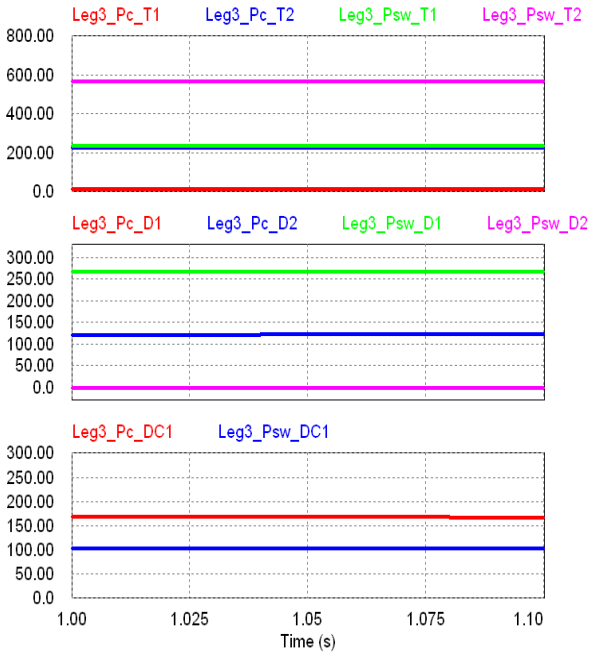


Fig. 120 - Devices power losses in leg 3.

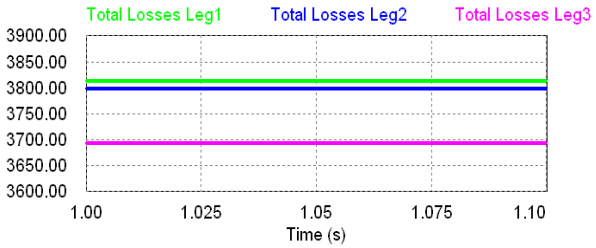


Fig. 121 - Total power losses in case of NPC VSI 3-L.

VI.1.3 Comparison between 3-L NPC VSI and 2-L VSI

In conclusion, Table XI summarizes the total compensator power losses in the case of STATCOMs based on 2-L VSI and NPC 3-L VSI.

The table also shows the power losses in the case of a converter designed for total compensation, even though this case was not considered in the previous paragraph.

UNBALANCE COMPENSATOR		Numbers Of VSI 2-L Modules	Total Power Losses [kW]	Numbers Of VSI 3-L Modules	Total Power Losses [kW]
Average Compensation	5.7 MVA	13	128.2	7	80.6
Total Compensation	10 MVA	22	223	12	141

Table XI - Power losses in STATCOM unbalance compensator.

VI.2 Unbalance compensation in Evron substation using CCI

In this section, the design of a voltage unbalance compensator based on the active Steinmetz structure is investigated for the substation at Evron. As in the case of VSI compensators, first, the compensator design is treated, after which the power losses in the semiconductor devices are evaluated.

VI.2.1 Compensator rating

The aim is to determine the sizes for the inductive and capacitive CCIs composing the active Steinmetz compensator. The power size is chosen in order to guarantee the voltage unbalance factor limits.

An average load of S_{Lref} = 10 MVA is considered as a reference for unbalance compensator sizing. The compensator must be able to provide a UF% under limits when the substation is feeding a load of S_{Lref} or, similarly, a 10-min average load of S_{Lref}.

Regarding the design of the compensator, only strategy 1 (Table VI) is considered. Only the real part of the current negative component is reduced. The two CCIs are controlled to draw the same current ($\beta_1 = \beta_2$).

The compensation case for the whole region is not treated due to its strong drawback of degrading the power factor.

Figure 122 shows the voltage unbalance factor at the PCC versus CCI size, S_{CCI}, for different load phases. Particularly, load phase variations from 0° to 60° are considered. The case of a negative phase is not reported because of the symmetry.

Three short-circuit power values for the transmission line are considered (295 MVA, 575 MVA and 700 MVA).

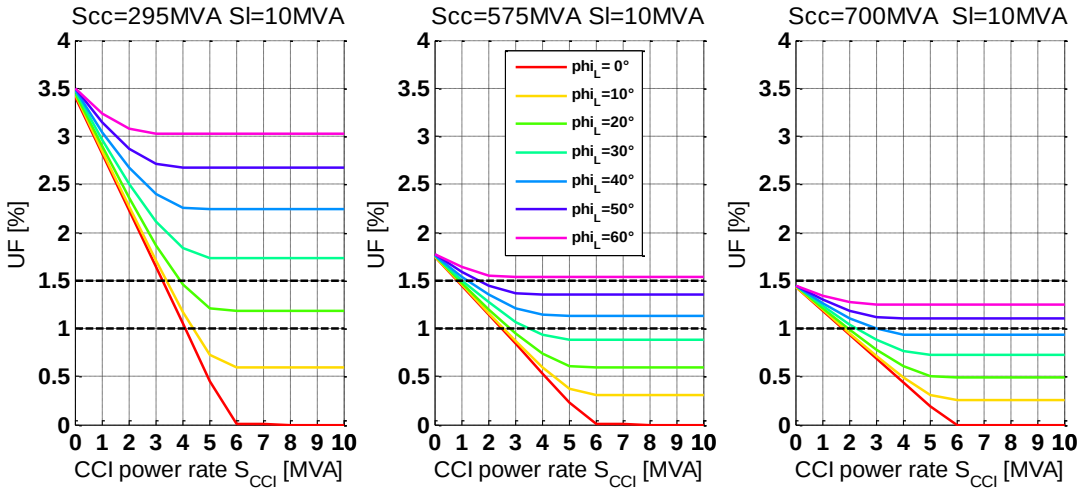


Fig. 122- UF vs. active Steinmetz size, S_{CCI}, for different load phase values.

For the design criteria, the worst case of a weak grid (short-circuit power of 295 MVA) is considered. Two design strategies are possible, as in the case of VSI compensators:

a) The CCIs are sized in order to guarantee a voltage unbalance factor of 1.5% for a substation load of 10 MVA with $\varphi_L = 0°$ (average compensation).

b) The CCIs are sized in order to guarantee a voltage unbalance factor of 0% for a substation load of 10 MVA with $\varphi_L = 0°$ (total compensation).

VI.2.1.1 Average compensation

The CCI power rate is set to $S_{CCI} = 3.3$ MVA. The total active Steinmetz rate, S_c, is clearly twice the CCI size.

As only the real part of the negative component is reduced, for a load at a non-unitary power factor, the compensation capability is lower.

The operation of the compensator in the case of different phases for the load is analyzed under rating condition $S_{CCI} = 3.3$ MVA. Figure 123 shows the percentage of the negative current component (magnitude) as a function of the load phase. As expected, the compensation capability decreases while the phase load increases.

In order to evaluate the compensator efficacy for voltage unbalance reduction, figure 124 shows the UF% versus phase load variation for three different values of S_{cc}. The power quality limits are guaranteed according to the following relations:

- 295MVA≤ S_{cc} <575MVA → *UF%*<1.5% for $|\varphi_L|$ close to 0°
- S_{cc}≥575MVA → *UF%*<1% for $|\varphi_L|$<30°

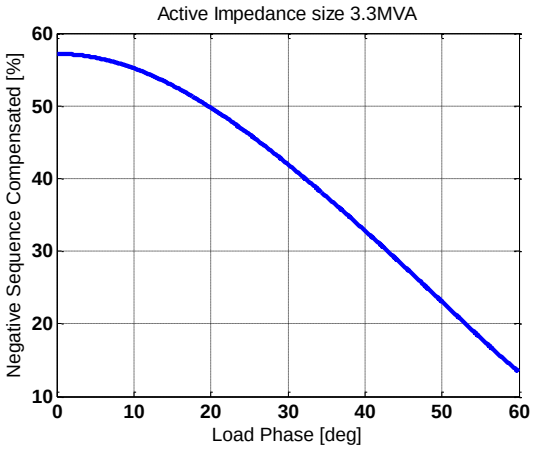


Fig. 123 – Negative sequence current compensation percentage vs. load phase variation.

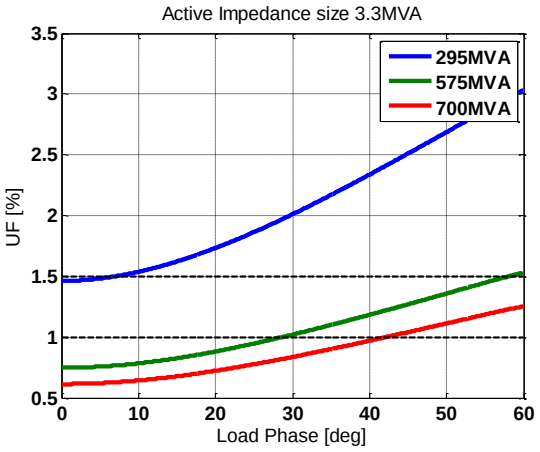


Fig. 124 – Voltage unbalance factor vs. load phase variation for different S_{cc}.

VI.2.1.2 Total compensation

With this approach, the active impedance size is S_{CCI} = 6 MVA. In this rating condition, the compensator is able to guarantee VUF% = 0% when the substation is feeding a load of 10 MVA with φ_L = 0° in the case of a weak power system. As in the previous case, the operation of the compensator in the case of different phases of the load is analyzed in figures 125 and 126. The following results are obtained:

- 295MVA≤ S_{cc} <575MVA → *VUF%*<1.5% for $|\varphi_L|$ <26°
- S_{cc}≥575MVA → *VUF%*<1% for $|\varphi_L|$<35°

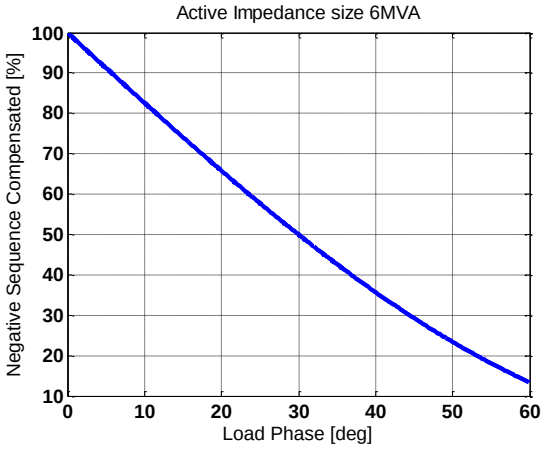


Fig. 125 - Negative current compensation percentage vs. load phase variation.

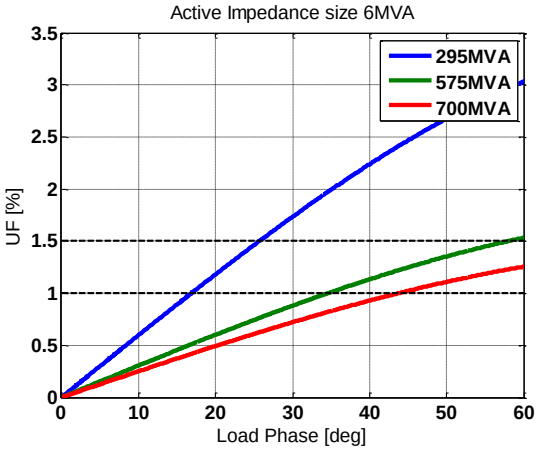


Fig. 126 - Voltage unbalance factor vs. load phase variation for different S_{cc}.

Table XII summarizes the information on compensator sizing.

Average Compensation		Total Compensation	
VUF% = 1.5% when the substation is feeding a load of 10 MVA with $\varphi_L = 0°$ in case of weak power system		VUF% =0% when the substation is feeding a load of 10 MVA with $\varphi_L = 0°$ in case of weak power system	
Theoretical performance: 295 MVA $\leq S_{cc} <$ 575 MVA *VUF%* < 1.5% for $\lvert\varphi_L\rvert$ close to 0° $S_{cc} \geq$ 575 MVA *VUF%* < 1% for $\lvert\varphi_L\rvert <$ 30°		*Theoretical performance:* 295 MVA $\leq S_{cc} <$ 575 MVA *VUF%* < 1.5% for $\lvert\varphi_L\rvert <$ 26° $S_{cc} \geq$ 575 MVA *VUF%* < 1% for $\lvert\varphi_L\rvert <$ 35°	
INDUCTIVE CCI	3.3 MVA	*INDUCTIVE CCI*	6 MVA
CAPACITIVE CCI	3.3 MVA	*CAPACITIVE CCI*	6 MVA
TOTAL ACTIVE STEINMETZ COMPENSATOR S_c	6.6 MVA	*TOTAL ACTIVE STEINMETZ COMPENSATOR S_c*	12 MVA

Table XII – Active Steinmetz rating.

VI.2.2 Numerical Simulation

In order to verify that the requirements are satisfied even if an average compensation is performed, numerical simulations are carried out using measurements from the substation. Moreover, this is a way to validate the design criteria of the active Steinmetz compensator.

The average model at the fundamental frequency of the system is considered. The numerical algorithm evaluates the equations describing symmetrical current and voltage components as functions of the load, compensator size and power transmission line parameters.

The active and reactive power values measured at the Evron substation (figures 103 and 104) are used in the algorithm to set the value of the load.

VI.2.2.1 Algorithm description

A simple diagram of the numerical algorithm is shown in figure 127. The following inputs are needed:

- array of load active power P_L values,
- array of load reactive power Q_L values,
- positive sequence line voltage E,
- short-circuit power of the transmission line, S_{cc}, and line impedance phase, $\varphi_{cc,}$
- power rate, S_{CCI}, of the CCI composing the Steinmetz compensator.

The algorithm can be summarized in the following steps:

- Calculation of negative and positive sequence currents of the load,
- Determination of converter duty cycles $\beta_1(k)$ and $\beta_2(k)$,
- Calculation of negative sequence injected by the compensator,
- Calculation of voltage unbalance factor with ($COMP$ = 1) or without ($COMP$ = 0) the active Steinmetz compensator.

k is the sequence index execution step. It assumes values from k = 1 to k equal to the length of the stored power array.

As the power arrays are discretized at T_{sample} = 20 ms, the calculated algorithm output is discretized at the same value.

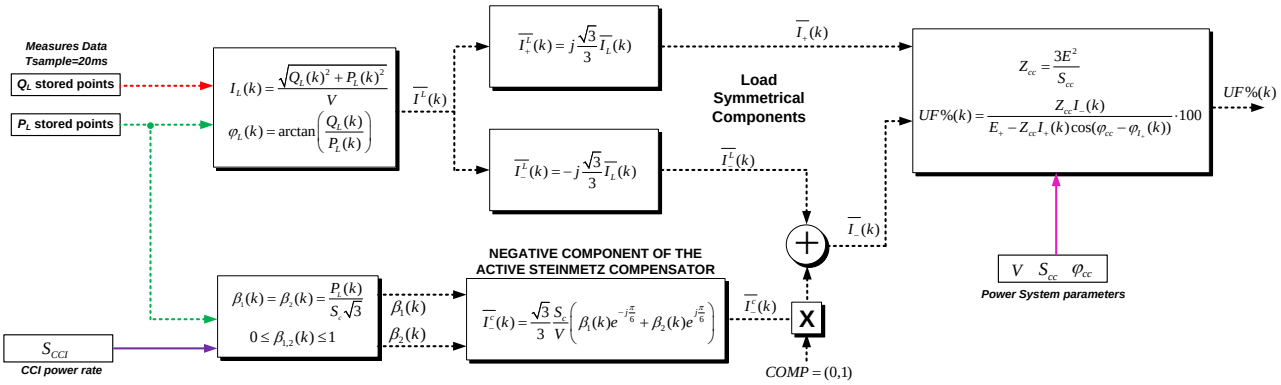


Fig. 127 - Matlab algorithm for symmetrical component evaluation.

VI.2.2.2 Numerical results

The algorithm has been executed for different conditions, as summarized in Table XIII. Load measurements of ‘case a’ and ‘case b’ are used as the load power input, and two short circuit power values are considered (295 MVA and 575 MVA). The line impedance angle, φ_{cc}, has been set to 80°. This is a realistic value for this kind of power system. The results are reported in the figures listed in Table XIV.

	Load Power	*Power System*	*CCI Size*
Analysis 1	P_L and Q_L of measure 'case a'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 295MVA $\varphi_{cc} = 80°$	S_{CCI} = 3.3 MVA
Analysis 2	P_L and Q_L of measure 'case a'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 575MVA $\varphi_{cc} = 80°$	S_{CCI} = 3.3 MVA
Analysis 3	P_L and Q_L of measure 'case a'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 295 MVA $\varphi_{cc} = 80°$	S_{CCI} = 6 MVA
Analysis 4	P_L and Q_L of measure 'case a'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 575 MVA $\varphi_{cc} = 80°$	S_c = 6 MVA
Analysis 5	P_L and Q_L of measure 'case b'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 295 MVA $\varphi_{cc} = 80°$	S_{CCI} = 3.3 MVA
Analysis 6	P_L and Q_L of measure 'case b'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 575 MVA $\varphi_{cc} = 80°$	S_{CCI} = 3.3 MVA
Analysis 7	P_L and Q_L of measure 'case b'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 295 MVA $\varphi_{cc} = 80°$	S_{CCI} = 6 MVA
Analysis 8	P_L and Q_L of measure 'case b'	$E = 90/\sqrt{3}\,kV$ S_{cc} = 575 MVA $\varphi_{cc} = 80°$	S_{CCI} = 6 MVA

Table XIII - Numerical analysis parameters.

Analysis 1	**Analysis 2**	**Analysis 3**	**Analysis 4**	**Analysis 5**	**Analysis 6**	**Analysis 7**	**Analysis 8**	***Description***
Fig. 128	Fig. 131	Fig. 134	Fig. 137	Fig. 140	Fig. 143	Fig. 146	Fig. 149	Voltage unbalance factor before and after compensator insertion
Fig. 129	Fig. 132	Fig. 135	Fig. 138	Fig. 141	Fig. 144	Fig. 147	Fig. 150	Magnitude of current negative sequence before and after compensator insertion
Fig. 130	Fig. 133	Fig. 136	Fig. 139	Fig. 142	Fig. 145	Fig. 148	Fig. 151	Active impedances duty cycles β_1 and β_2

Table XIV - Table of figures for numerical results.

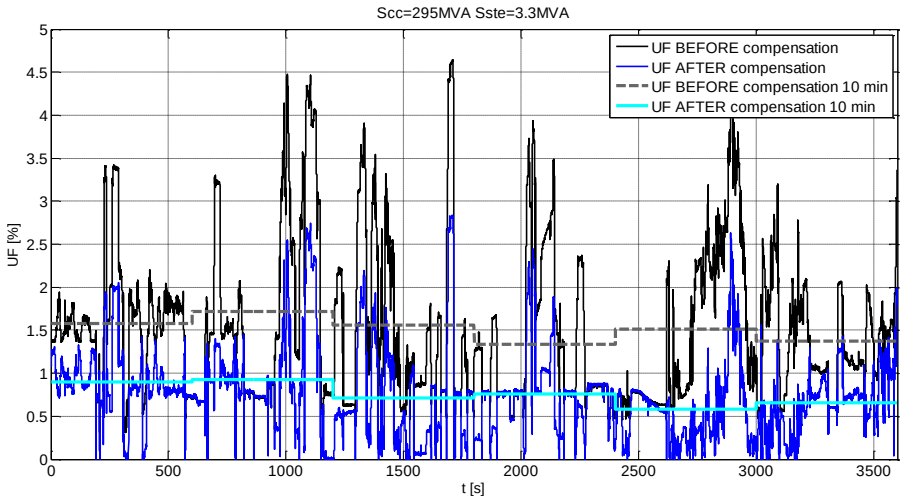


Fig. 128 - Analysis 1 - Voltage unbalance factor.

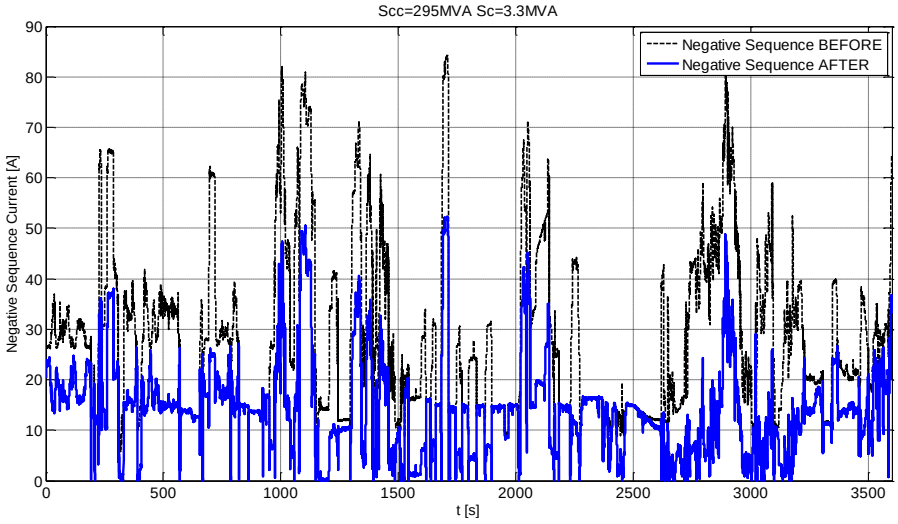


Fig. 129 - Analysis 1 - magnitude of negative current sequence.

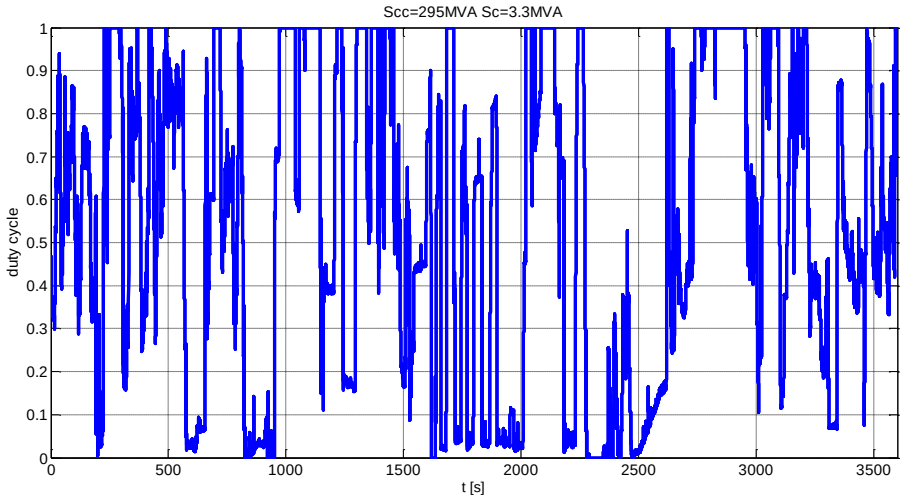


Fig. 130 - Analysis 1 - Inductive AC-chopper duty cycle Beta1 and capacitive AC-chopper duty cycle Beta2.

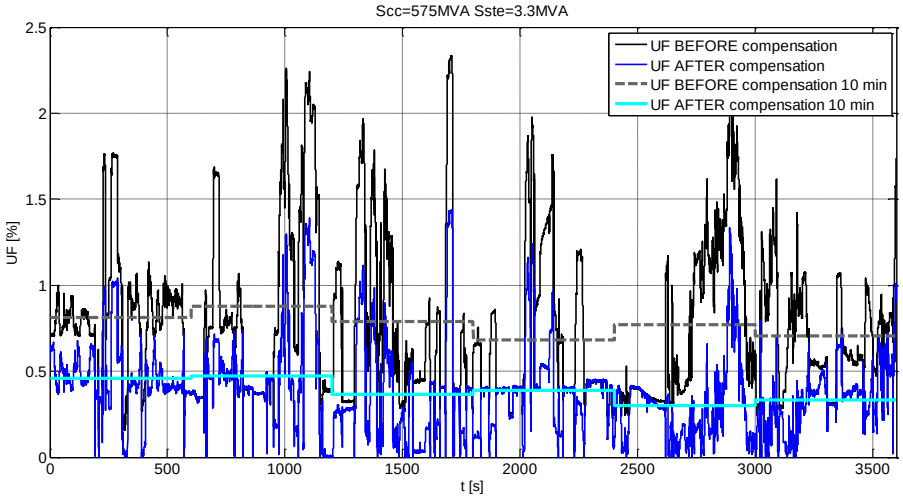


Fig. 131 - Analysis 2 - voltage unbalance factor.

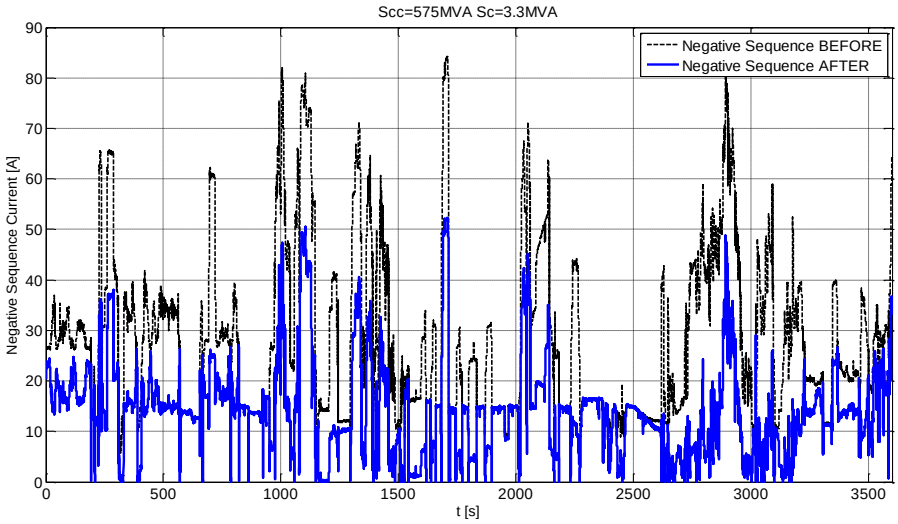


Fig. 132 - Analysis 2 - magnitude of negative current sequence.

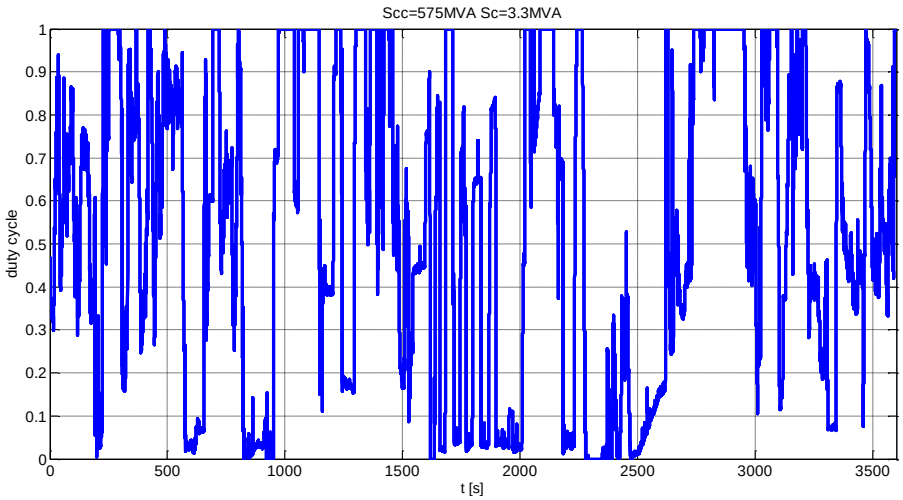


Fig. 133 - Analysis 2 - inductive AC-chopper duty cycle β_1 and capacitive AC-chopper duty cycle β_2.

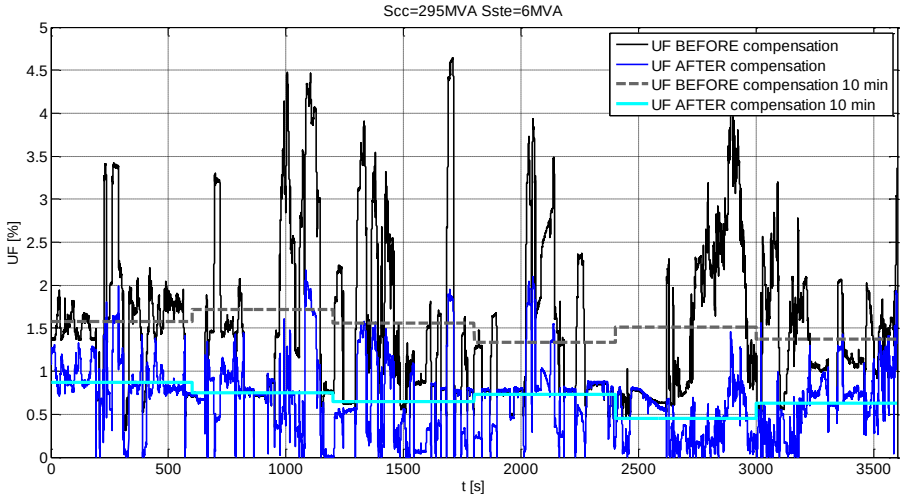


Fig. 134 - Analysis 3 - voltage unbalance factor.

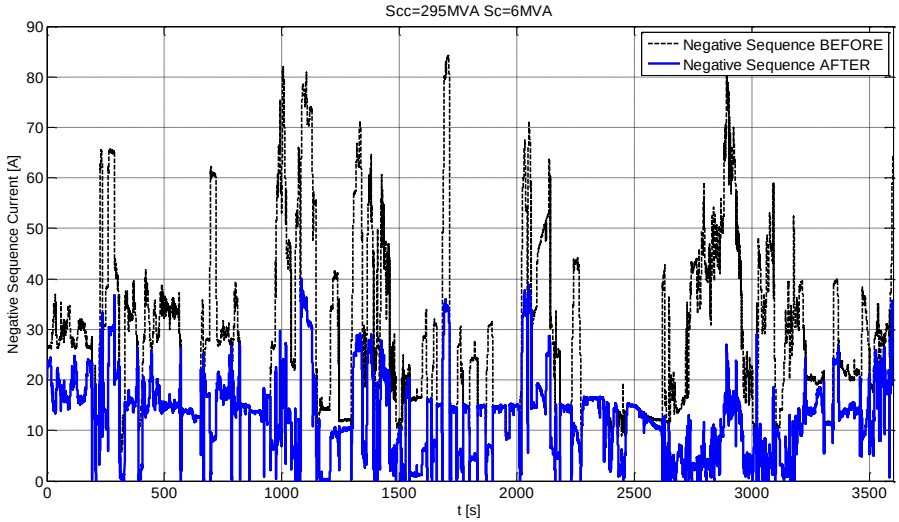


Fig. 135 - Analysis 3 - magnitude of negative current sequence.

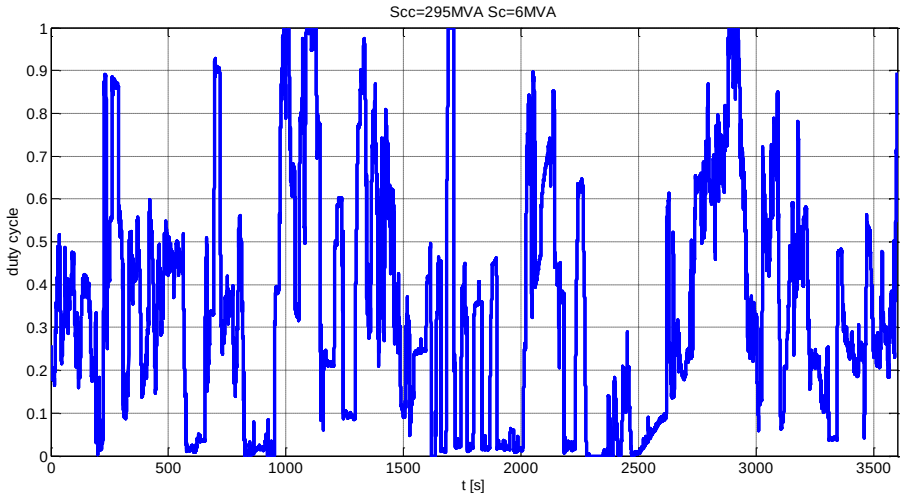


Fig. 136 - Analysis 3 - inductive AC-chopper duty cycle β1 and capacitive AC-chopper duty cycle β2.

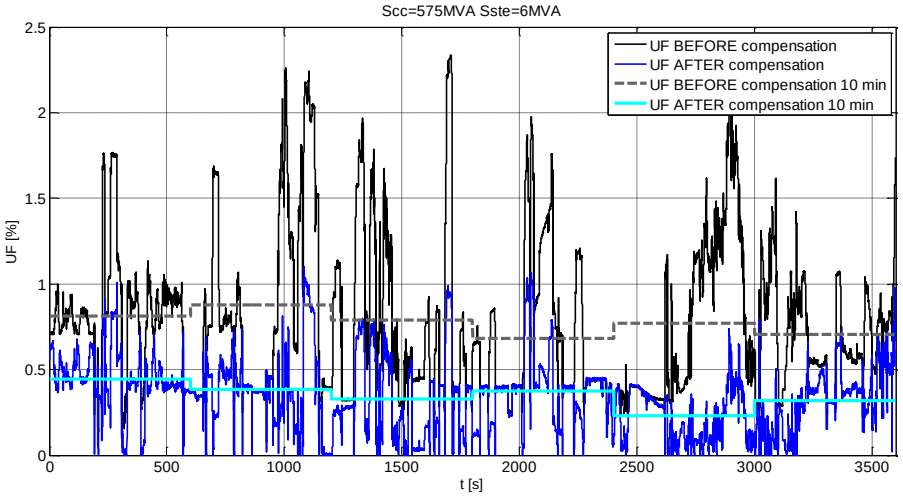


Fig. 137 - Analysis 4 - voltage unbalance factor.

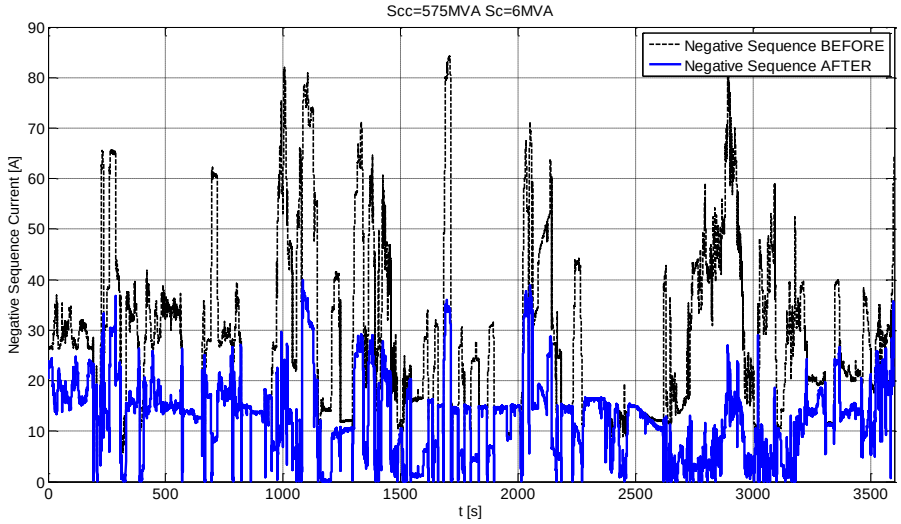


Fig. 138 - Analysis 4 - magnitude of negative current sequence.

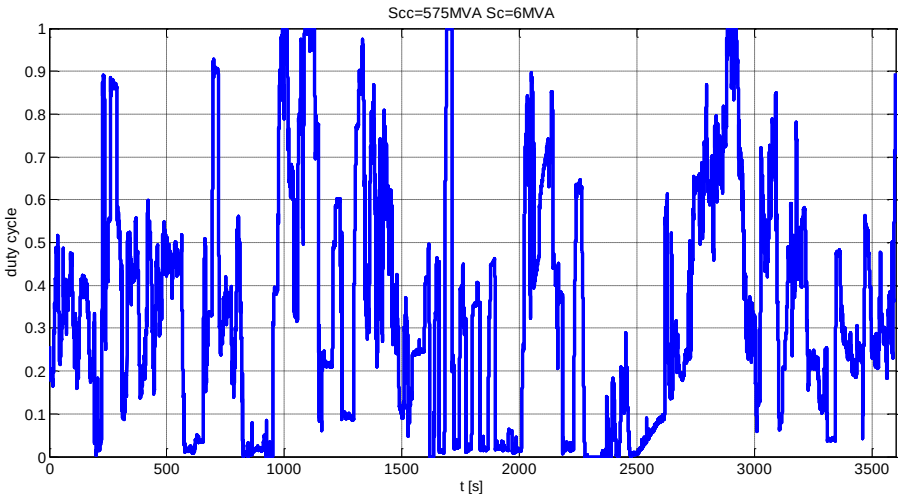


Fig. 139 - Analysis 4 - inductive AC-chopper duty cycle β1 and capacitive AC-chopper duty cycle β2.

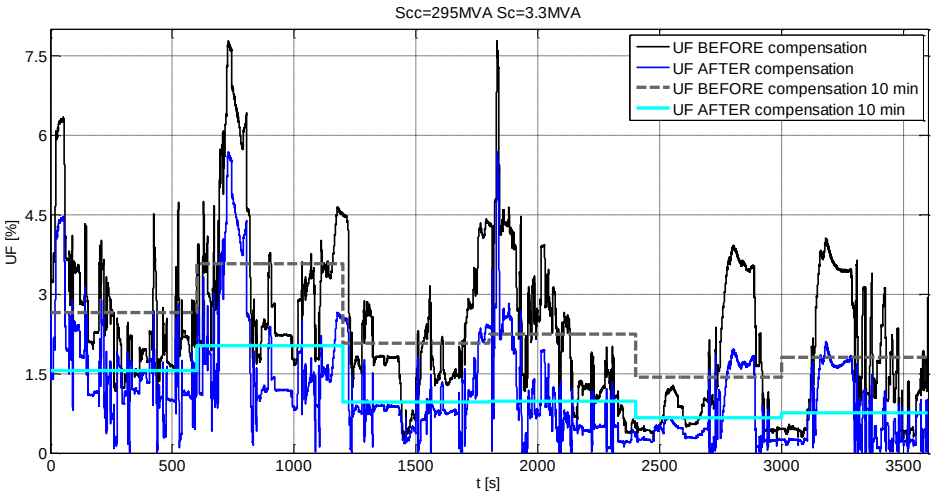


Fig. 140 - Analysis 5 - voltage unbalance factor.

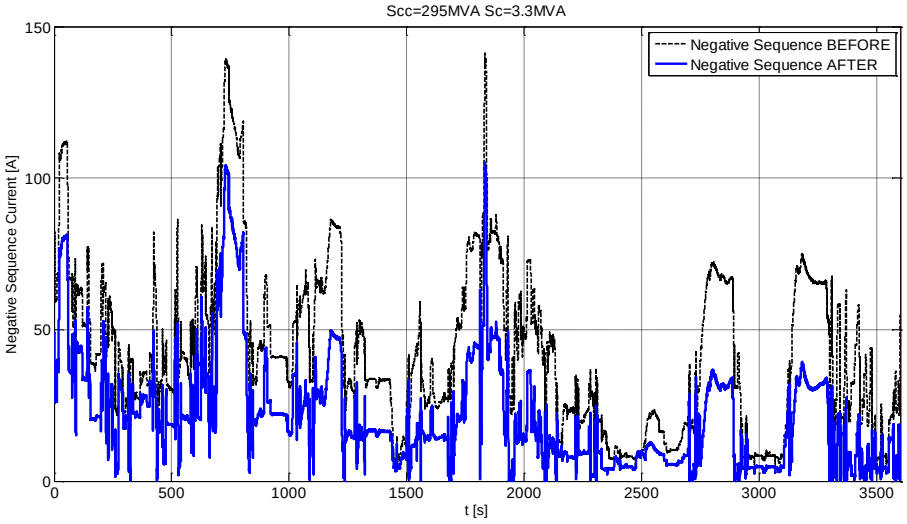


Fig. 141 – Analysis 5 - magnitude of negative current sequence.

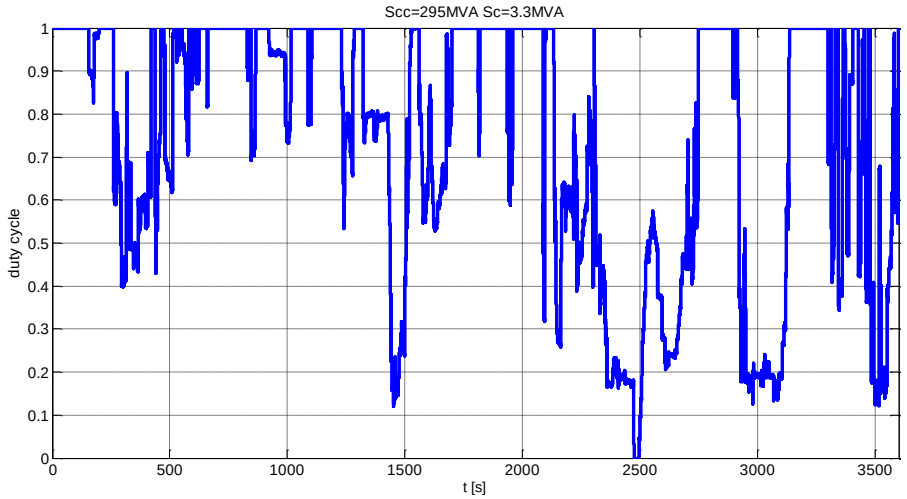


Fig. 142 - Analysis 5 - inductive AC-chopper duty cycle β1 and capacitive AC-chopper duty cycle β2.

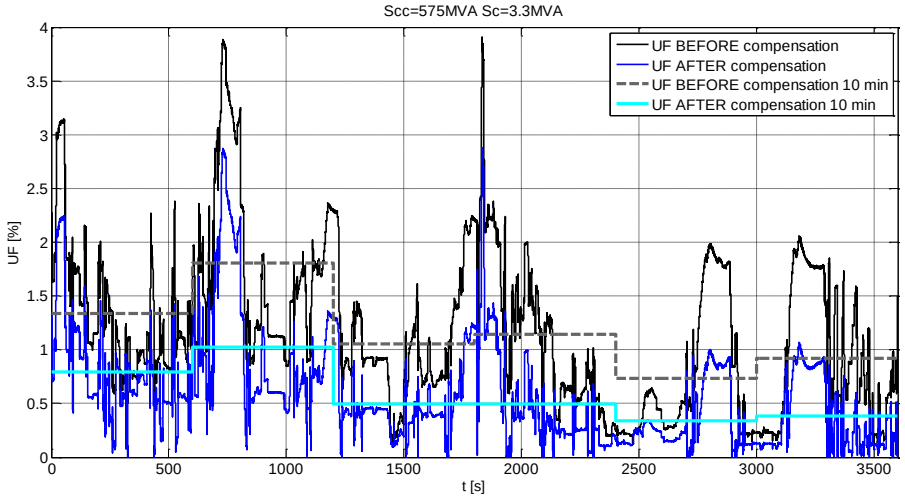


Fig. 143- Analysis 6 - voltage unbalance factor.

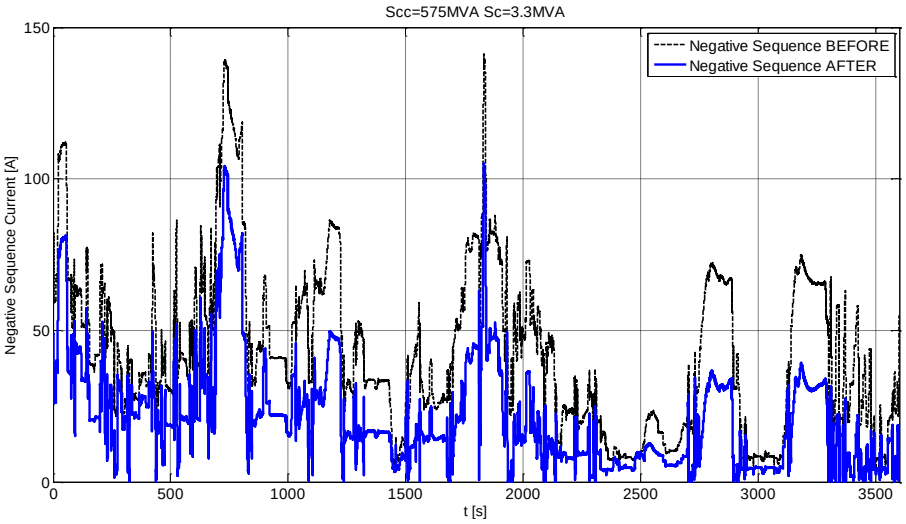


Fig. 144 - Analysis 6 - magnitude of negative current sequence.

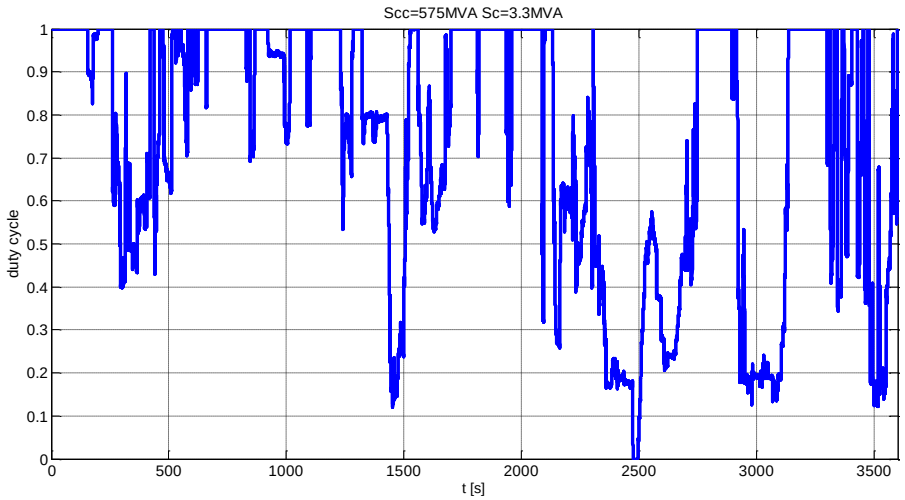


Fig. 145 - Analysis 6 - inductive AC-chopper duty cycle β1 and capacitive AC-chopper duty cycle β2.

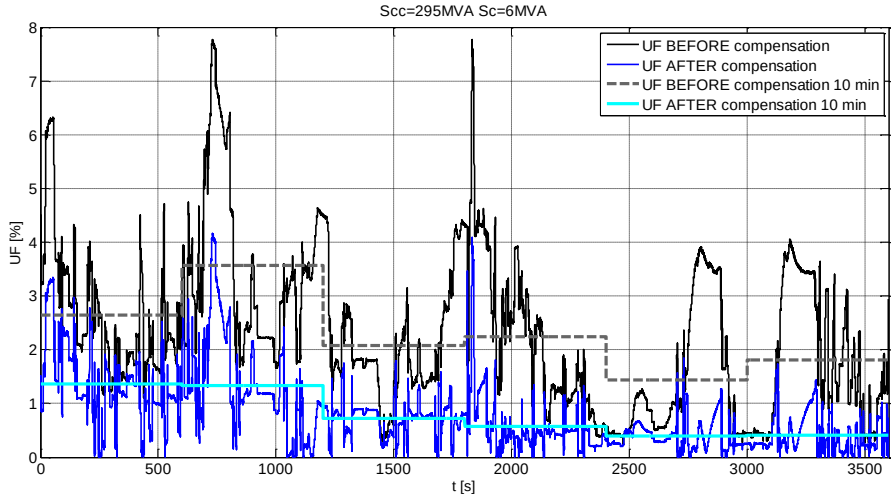


Fig. 146 - Analysis 7 - voltage unbalance factor.

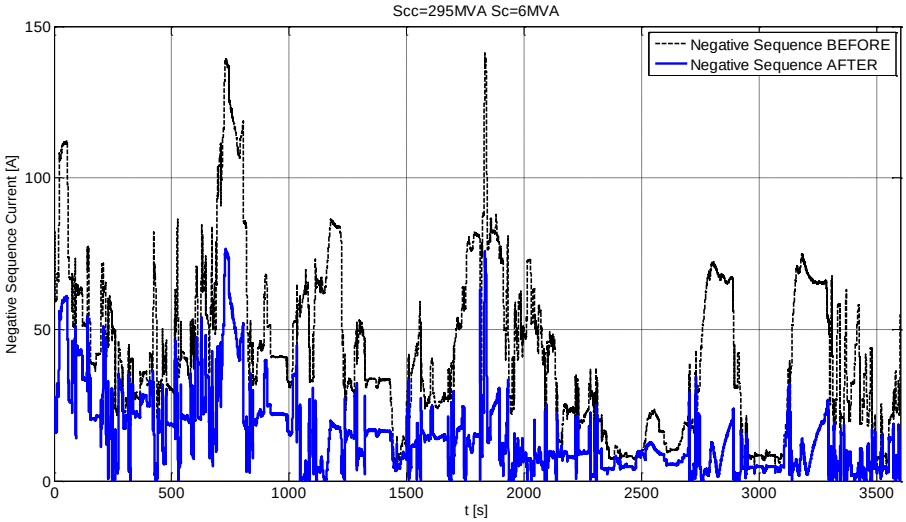


Fig. 147 - Analysis 7 - magnitude of current negative sequence.

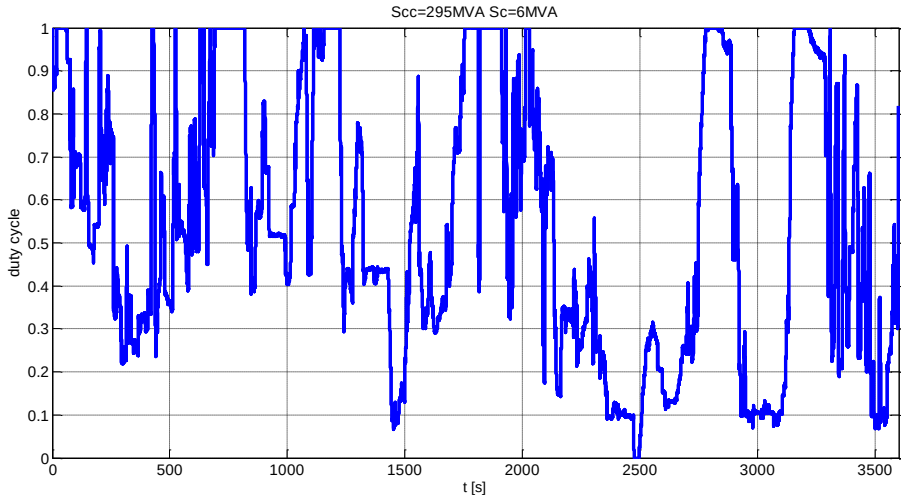


Fig. 148 - Analysis 7 - inductive AC-chopper duty cycle β1 and capacitive AC-chopper duty cycle β2.

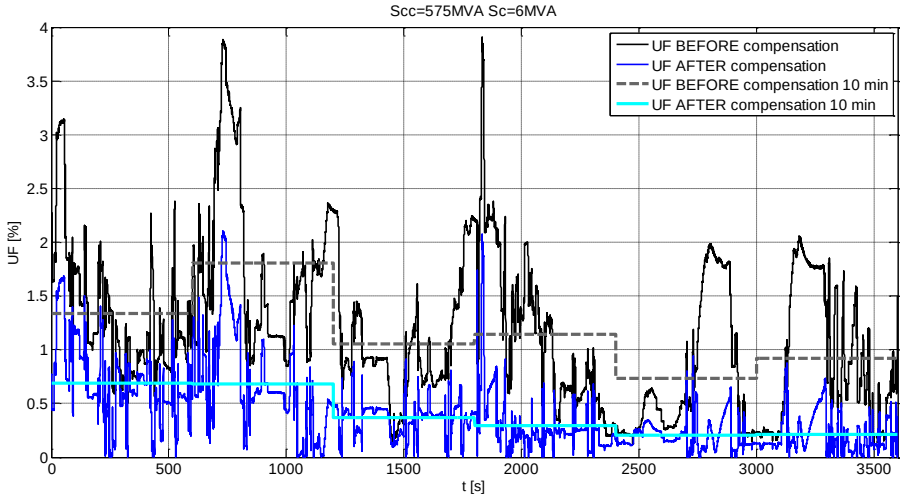


Fig. 149 - Analysis 8 - voltage unbalance factor.

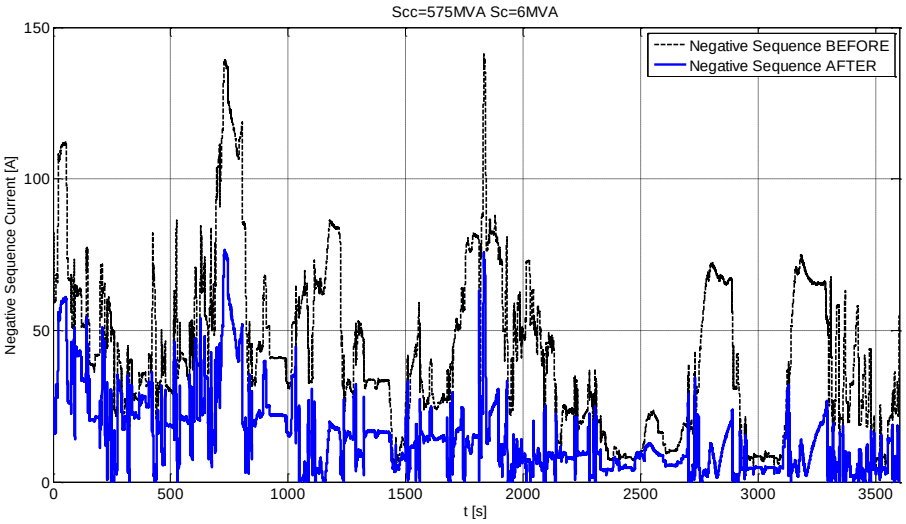


Fig. 150 - Analysis 8 - magnitude of current negative sequence.

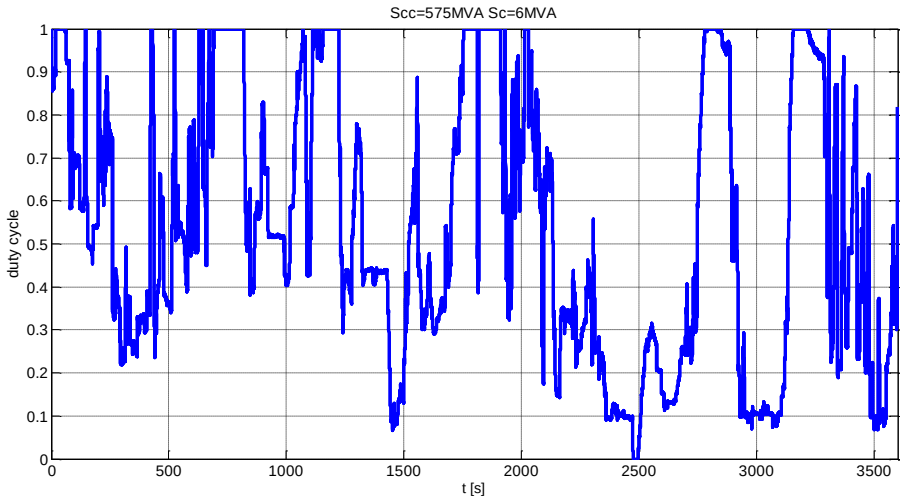


Fig. 151 - Analysis 8 - inductive AC-chopper duty cycle β1 and capacitive AC-chopper duty cycle β2.

VI.2.2.3 Penalties reduction

Let us call a penalty point every measurement point on the 10-min average where the voltage unbalance factor exceeds the limit imposed.

On the basis of the numerical results, the following considerations are made:

- In the case of load measurement '**a**', the voltage unbalance limits are respected for all power system conditions and for both CCI power rate cases (3.3 MVA and 6 MVA)
- In case of load measurement '**b**', looking at figure 140, there is a penalty point. This is the case where a 3.3-MVA CCI is used, and the minimum short-circuit power for the transmission power system is considered. Moreover, in the considered time interval, the substation is feeding a load of 20 MW.

As expected, the proposed compensator is able to achieve an average compensation. The railways operator is not interested in oversizing the power electronic equipment to totally compensate for sporadic peaks of unbalance. This makes possible savings in power losses and volume, and thus has economic advantages.

A statistical analysis is carried out on 6 years of records to evaluate the penalty point reduction as a function of the size of the installed compensator. The results are reported in figure 152. It should be noted that, with an active Steinmetz compensator of a 2 × 3.3-MVA CCI, a reduction of about 98% is achieved. Moreover, figure 153 shows the unbalance factor during the 6 years without and with the compensator (3.3 MVA). There are 52400 penalty points without the compensator, and after the compensation, the number decreases to 985.

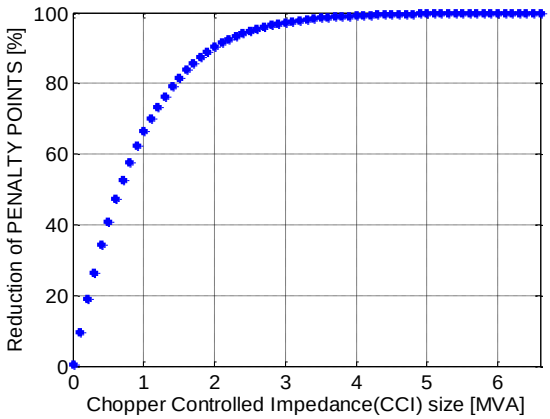


Fig. 152 - Penalty point reduction as function of size of installed compensator.

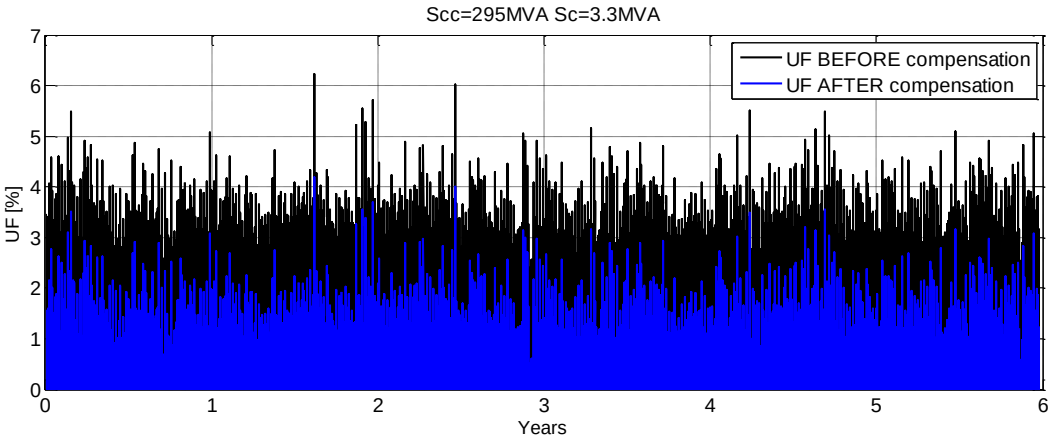


Fig. 153 – Unbalance factor before and after compensation with active Steinmetz.

VI.2.3 Compensator design

The converter design is carried out considering standard 3.3 kV/1.5 kA IGBT modules, as in the VSI STATCOM case. Only the case of the average compensation is treated. The size of each CCI is S_{CCI} = 3.3 MVA. The averaged models for the capacitive and inductive controlled impedances, presented in figures 154 and 155, are used.

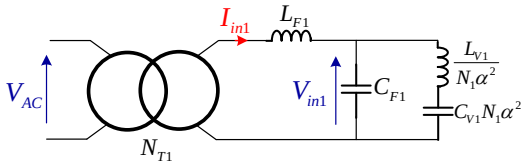


Fig. 154 - Averaged model for capacitive controlled impedance.

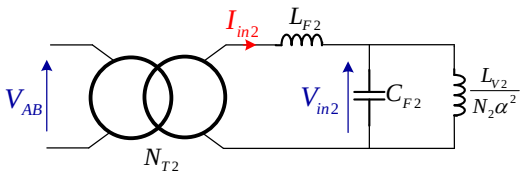


Fig. 155 - Averaged model for inductive controlled impedance.

The following specifications are considered in the design criteria:

- *Transformer ratio*

N_{T1} and N_{T2} are chosen in order to guarantee the limit voltage of 1800 V for semiconductors devices.

- *Input filter*

With the aim of balancing the substation, even when it is not loaded, the 2.7 MVAR reactive power compensator that already exists is replaced with one of 900 kVAR, and the capacitor input filter of the CCI is chosen in order to provide a reactive power Q_F = 900 kVAR. In this way, when no trains are supplied by the substations, the circuit is balanced for the three-phase network.

Moreover, $L_{F1,2}$ is considered as a common leakage inductance for a 3.3-MVA transformer, evaluated as:

$$L_{F1,2} = 10\% \frac{\left(VN_{T1,2}\right)^2}{S_{C1,2}\omega_{net}} \tag{113}$$

- *Maximum AC-chopper output current*

The number of modules in parallel (N_1 or N_2) is chosen according to the thermal limits of the IGBTs with a maximum RMS current I_{max}= 735 A (see appendix AI).

Two different sizing criteria are possible for the variable part of the controlled impedances. The first considers each CCI of power S_{CCI} including the capacitive input filters. In the second case, each CCI is rated at S_{CCI} not including the capacitive input filter. The two strategies are presented following.

- ***Case a***

Output impedance parameters are chosen in order to get the desired power at the maximum duty cycle, including the input filter:

$$S_{CCI1} = \left(V_{AC} N_{T1}\right)^2 \left[L_{F1}\omega_{net} + \frac{L_{V1}\omega_{net} - \frac{1}{C_{V1}\omega_{net}}}{\frac{C_{F1}}{C_{V1}} + N_1 \alpha_{\max}{}^2 - C_{F1} L_{V1} \omega_{net}{}^2} \right]^{-1} = 3.3MVA \tag{114}$$

$$S_{CCI2} = \left(V_{AB} N_{T2}\right)^2 \left[\frac{L_{V2}}{\frac{N_2 \alpha_{\max}{}^2}{\omega_{net}} - C_{F2} L_{V2}\, \omega_{net}} + L_{F2}\omega_{net} \right]^{-1} = 3.3MVA \tag{115}$$

Moreover, regarding the output impedance of the capacitive AC-choppers, a 10% maximum current ripple at the switching frequency is chosen:

$$\Delta I_{out} = \frac{V_{AC} N_{T1}}{4(1 - \omega_{net}{}^2 L_{V1} C_{V1}) L_{V1} f_{sw}} = 0.1 \cdot \mathrm{I}_{\max} \tag{116}$$

The last one is calculated under the hypothesis that the voltage drop on the inductor L_{F1} is neglected.

The design results are summarized in Table XV.

N_{T1}=0.0129	N_{T2}= 0.0137
N_1= **3**	N_2= **5**
L_{F1}= 128µH	L_{F2}= 146µH
C_{F1}= 2.1mF	C_{F2}= 1.82mF
L_{V1}= 6.4mH	L_{V2}= 4.8mH
C_{V1}= 858µF	

Table XV - Theoretical converter parameters.

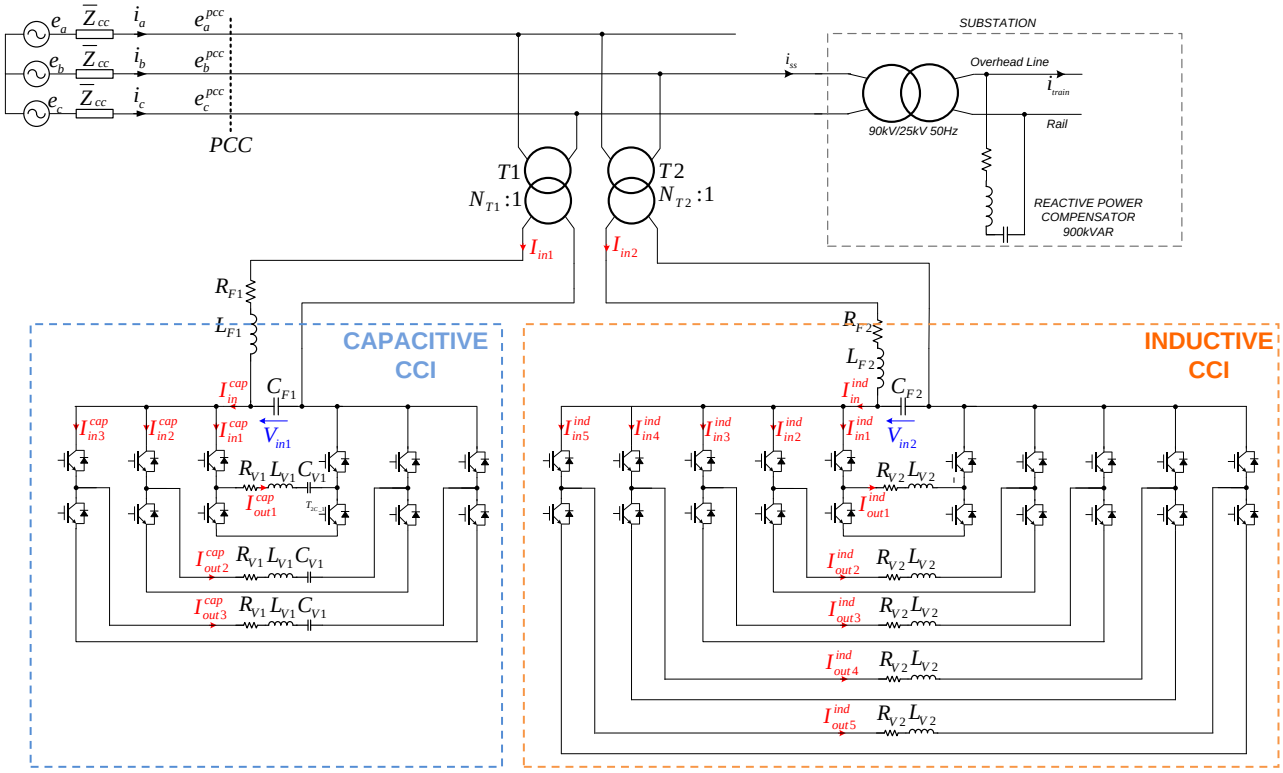


Fig. 156 – Active Steinmetz compensator at Evron substation (design strategy a).

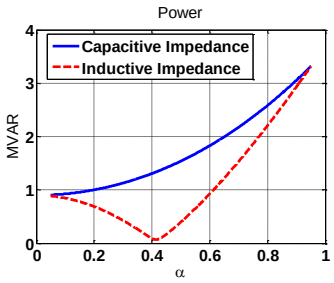


Fig. 157 – Reactive power vs. duty cycle $\alpha_{1,2}$.

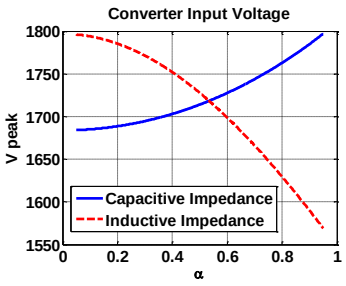


Fig. 158 – Input AC-choppers peak voltage vs. duty cycle $\alpha_{1,2}$.

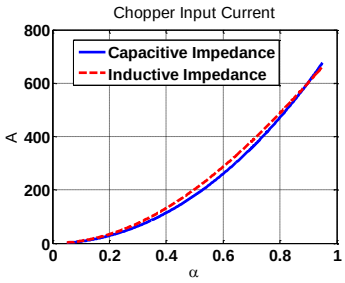


Fig. 159 – Chopper converter input current.

The compensator connection scheme for the substation is reported in figure 156.

Figures 157 , 158 and 159 report the calculations for the reactive power provided by the CCIs, input voltages V_{in1} and V_{in2} and input current variations versus duty cycles α_1 and α_2.

Different control laws are possible for the compensator. The one considered in this manuscript is described in figure 160, which show how the CCIs power are regulated in function of the substation load.

The following aspects can be highlighted:

- The number of AC-choppers in parallel for the inductive CCI is greater than for the capacitive CCI. This is because of the presence of the capacitive input filter, L_{F2}-C_{F2}, which makes it necessary to oversize the converter to show the desired inductive reactive power at the input.

- As expected, the input voltage increases with the duty cycle for the capacitive CCI. On the other hand, the input voltage decreases in the case of the inductive CCI.

- At the minimum duty cycle (0.05), both the CCIs are capacitive because of the input filters. This permits a balanced condition when the substation is unloaded.

- The capacitive CCIs have a lower limit for the provided reactive power due to the input filter. Thus, it is possible to compensate only for substation load $P_L \geq P_{Lmin}$, the minimum reactive power provided (at minimum duty cycle 0.05).

- The input currents at the maximum duty cycle are 677 A for the capacitive CCI and 662 A for the inductive CCI.

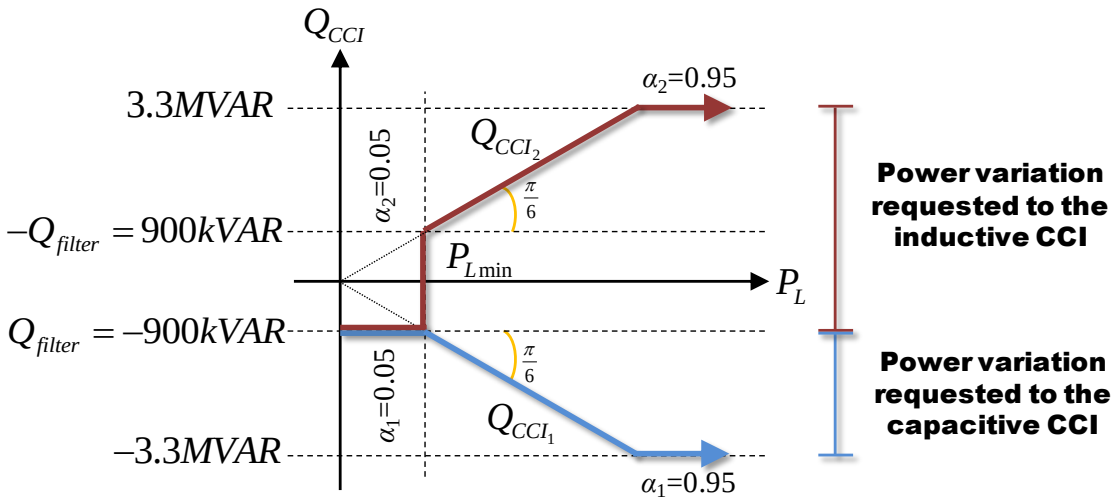


Fig. 160 - CCIs power vs Load power (design strategy a).

The average circuit for the whole system is used to analyze the influence of the substation current harmonics on the compensator operation. A frequential study has been carried out. Figure 161 shows the gain frequency response plots for V_{in1}/I_{ss}, V_{in2}/I_{ss}, I_{CA}/I_{ss} and I_{AB}/I_{ss}. Three resonant frequencies can be highlighted. The one found at a low frequency (68 Hz) is caused by the output impedance, L_{V1}-$C_{V1.}$ The other two resonant frequencies at around 300 Hz are due to interactions between the input filter, $L_{F1,2}$ - $C_{F1,2}$, and the line impedances.

Let us remark that the resonant frequencies are found in a frequency range where no currents should exist under normal conditions, as verified by measurements.

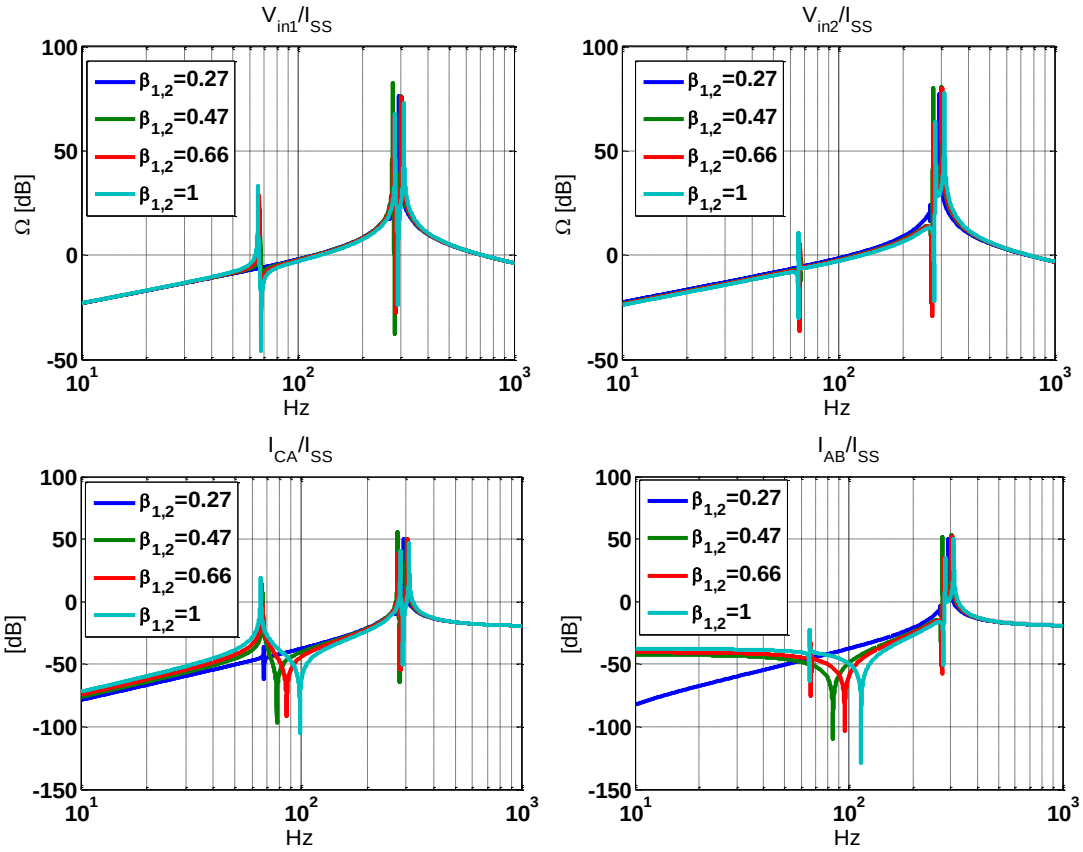


Fig. 161 - Frequency analysis.

- ***Case b***

Output impedance parameters are chosen in order to get the desired power at the maximum duty cycle, without including the input filter:

$$S_{CCI1}=\left(V_{AC}N_{T1}\right)^2\left[\frac{C_{V1}N_1{\alpha_{\max}}^2\omega_{net}\left(C_{V1}L_{V1}\omega_{net}-1\right)}{\left(C_{F1}L_{F1}{\omega_{net}}^2+C_{V1}L_{V1}{\omega_{net}}^2-C_{F1}C_{V1}L_{F1}L_{V1}{\omega_{net}}^4+C_{V1}L_{F1}N_1{\alpha_{\max}}^2{\omega_{net}}^2-1\right)^2}\right]=3.3MVA \quad (117)$$

$$S_{CCI2}=\left(V_{AB}N_{T2}\right)^2\left[\frac{C_{F2}N_2{\alpha_{\max}}^2\omega_{net}}{L_{V2}}\left(L_{F2}\omega_{net}+\frac{L_{V2}}{C_{F2}N_2{\alpha_{\max}}^2\left(\frac{1}{C_{F2}\omega_{net}}-\frac{L_{V2}\omega_{net}}{N_2{\alpha_{\max}}^2}\right)}\right)^2\left(\frac{1}{C_{F2}\omega_{net}}-\frac{L_{V2}\omega_{net}}{N_2{\alpha_{\max}}^2}\right)^2\right]^{-1}=3.3MVA \quad (118)$$

For the calculation of the output impedance of the capacitive AC-choppers a maximum allowed ripple expressed as (116) is considered.

N_{T1}=0.0129	N_{T2}= 0.0137
N_1= **4**	N_2= **4**
L_{F1}= 128μH	L_{F2}= 146μH
C_{F1}= 2.1mF	C_{F2}= 1.82mF
L_{V1}= 7.9mH	L_{V2}= 4.4mH
C_{V1}= 735μF	

Table XVI - Theoretical converter parameters.

The compensator connection scheme for the substation in this design condition is reported in figure 162.

Figures 163, 164 and 165 report the calculations for the reactive power provided by the CCIs, input voltages V_{in1} and V_{in2} and converters input current variations versus duty cycles α_1 and α_2.

The power control law is described in figure 166. Let us note that the power variation required is the same for both the CCIs. As a consequence, in this rating condition the number of choppers converter in parallel is equal for the two controlled impedances (N_1=N_2).

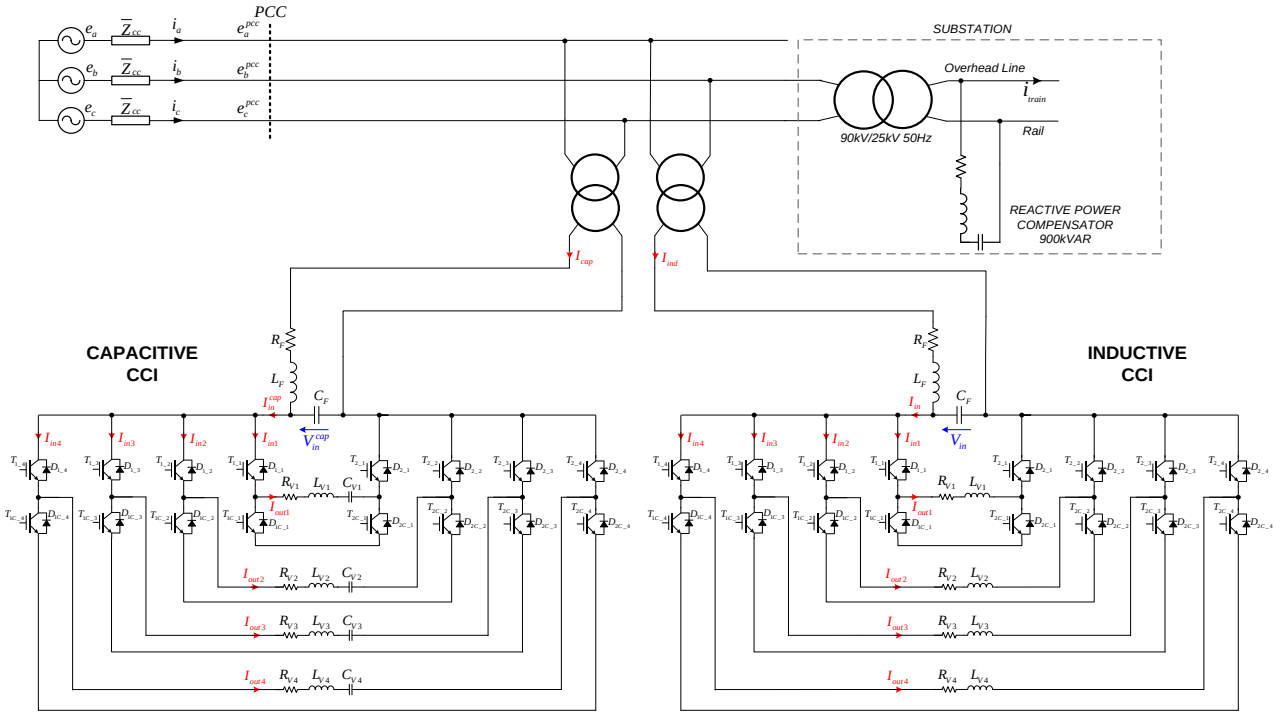


Fig. 162 - Active Steinmetz compensator at Evron substation (design strategy b).

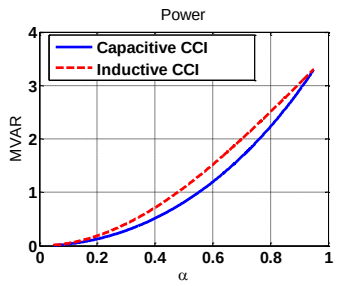


Fig. 163 – Reactive power vs. duty cycle $\alpha_{1,2.}$

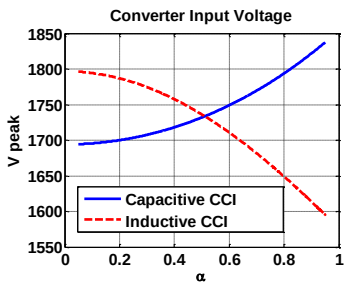


Fig. 164 – Input AC-choppers peak voltage vs. duty cycle $\alpha_{1,2.}$

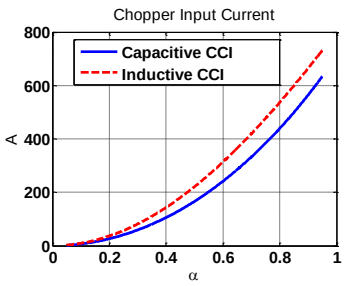


Fig. 165 – Chopper converter input current.

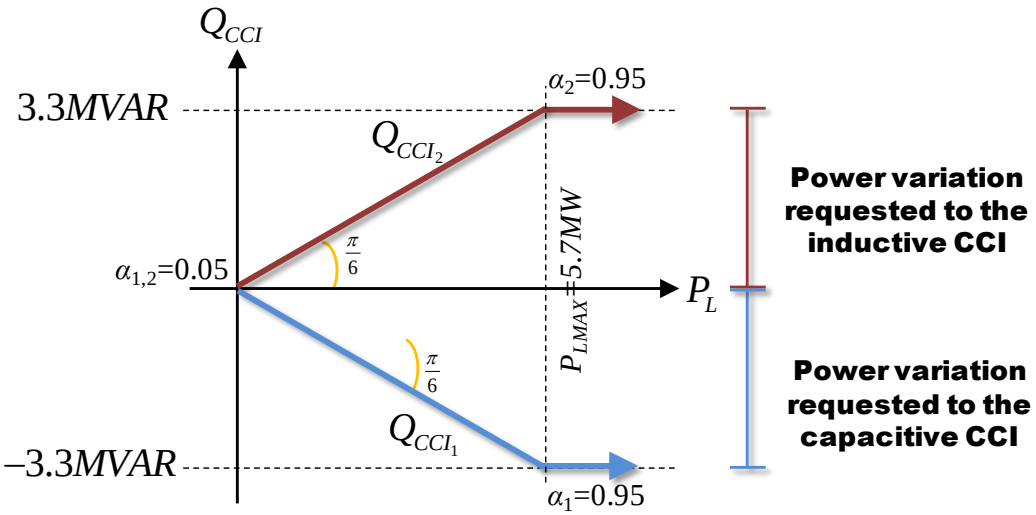


Fig. 166 - CCIs power vs Load power (design strategy b).

VI.2.4 Power losses

The power losses are evaluated using the equations described in the appendix AI. Only the case of design strategy "a" is presented, as for the second case, the results are quite similar.

A single module of each CCI is under study. The reference scheme for the single CCI module is shown in figure 167. Table XVII and Table XVIII report the calculation results for the losses at the maximum duty cycle for modules of the capacitive and inductive CCIs. Due to the symmetry, only the losses for one switching cell are described.

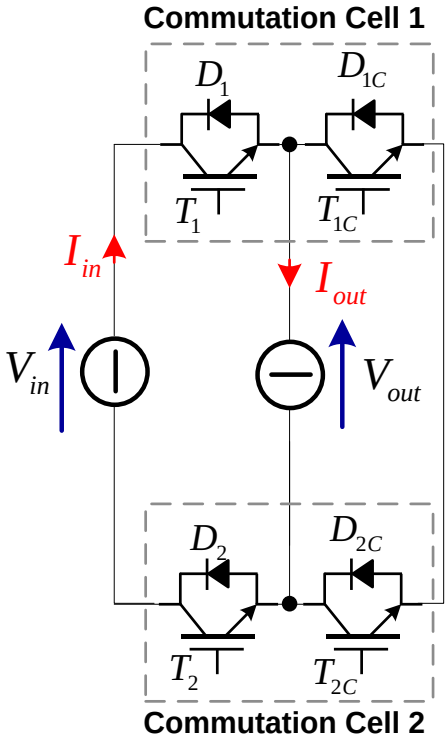


Fig. 167 – CCI single AC-chopper module.

AC-chopper module V_{in} =1800/sqrt(2)V I_{in} = 677 A	**Conduction Power losses [W]**	**Switching Power losses [W]**	**Junction Temperature [°C]**
IGBT1	703	302	117
IGBT1C	37	302	106
D1	522	156	124
D1C	27	156	106
Total Leg	1289	916	
Total AC-chopper	**4410 W**		

Table XVII - Power losses for a single AC-chopper module of the capacitive CCI.

AC-chopper Module V_{in}=1570/sqrt(2)V I_{in}=662A	**Conduction Power losses [W]**	**Switching Power losses [W]**	**Junction Temperature [°C]**
IGBT1	680	259	116
IGBT1C	36	259	105
D1	507	134	122
D1C	27	134	106
Total Cell	1240	786	
Total AC-chopper	**4072 W**		

Table XVIII - Power losses for single AC-chopper module of inductive CCI.

From the calculation, the total losses for the compensator can be evaluated by considering the number of modules in parallel for each CCI. On this basis, the total losses for the active Steinmetz are about 33.6 kW.

For the case of total compensation, the calculations are not reported. The total power losses in this rating condition are about 61.3 kW.

VI.2.4.1 Simulations

Simulation in PSIM using the thermal module tool are used to verify the calculation results.

Figure 168 shows simulation results for a capacitive CCI, and figure 169 reports the thermal module outputs. The same simulations are carried out for the case of an inductive CCI, and the results are shown in figures 170 and 171.

It should be noted that the simulation results and calculations match closely. On this basis, the analytical study of power losses is validated.

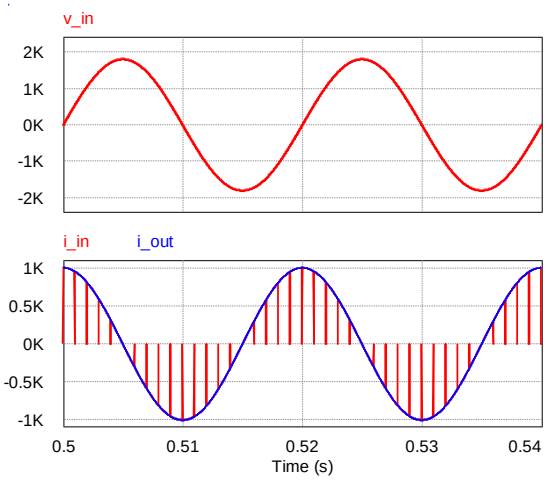


Fig. 168 - Simulation results for capacitive CCI.

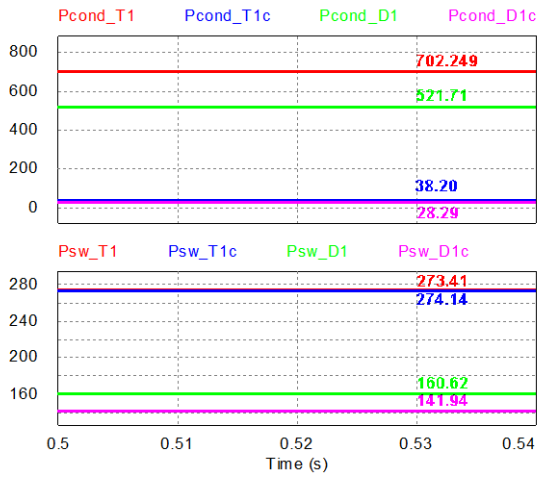


Fig. 169 – Thermal module results for capacitive CCI.

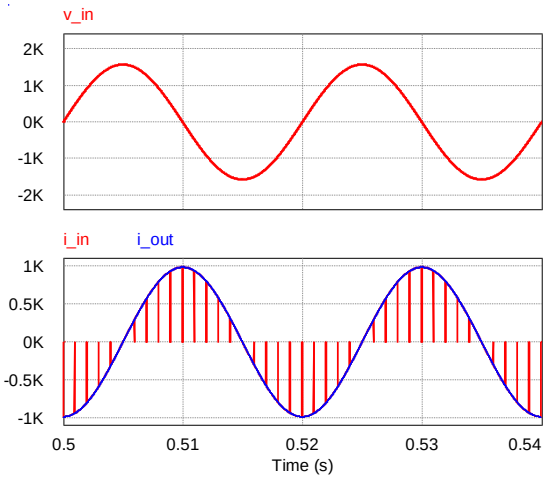


Fig. 170 - Simulation results for inductive CCI.

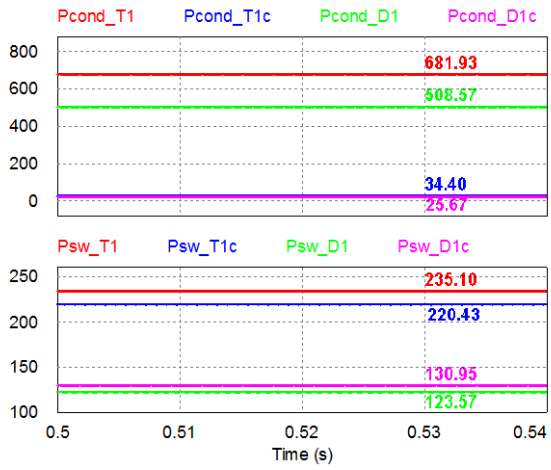


Fig. 171 - Thermal module results for inductive CCI.

VI.3 Comparison of VSI vs. active Steinmetz

On the basis of the results obtained in the previous sections, figure 172 summarizes the power losses for the different voltage balancer topologies under consideration. Losses are referred to a working condition for the compensators when the load phase is $\varphi_L = 0°$.

Comparing the two solutions based on VSI converters, the 3-level NPC solution is characterized by lower losses. In addition, if the active Steinmetz compensator is compared with the 3-L NPC topology, a reduction in the power losses of about 60% is achieved.

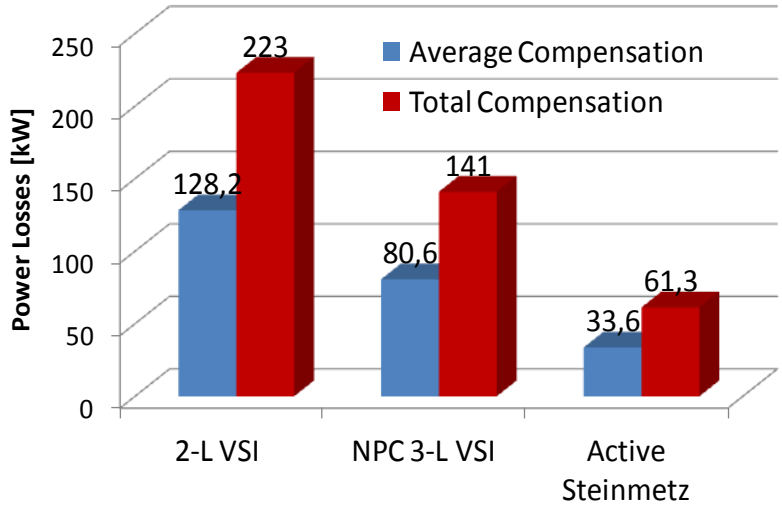


Fig. 172 – Comparison between voltage balancer topologies in terms of power losses.

The energy stored in the reactive elements is used as a qualitative index of the components space volume. Peak values for current $\hat{I}$ and voltage $\hat{V}$ in the inductors and capacitors of the three studied topologies are evaluated and used in the expressions:

$$E_{cap} = \frac{1}{2} C\hat{V}^2 \qquad E_{ind} = \frac{1}{2} L\hat{I}^2 \tag{119}$$

Table XIX shows the calculation results. Figure 173 shows a histogram of the total energies for the three compared solutions.

	Current [A] / Value	Voltage[V]	Energy	Quantity	Total Energy
VSI-2L					
DC-link capacitor [mF]	8.6	1800	13932	13	181116
Link inductor [mH]	2.1	684.5	492	39	19186
VSI NPC-3L					
DC-link capacitor [mF]	15	1800	24300	14	340200
Link inductor [mH]	4.4	635	887	21	18628
ACTIVE STEINMETZ					
Input filter inductor L_{F1} [mH]	0.128	3666.7	860	1	860
Input filter inductor L_{F2} [mH]	0.146	3666.7	981	1	981
Input filter capacitor C_{F1} [mF]	2.1	1800	3402	1	3402
Input filter capacitor C_{F2} [mF]	1.82	1800	2948	1	2948
Output inductor L_{V1} [mH]	6.4	957.4	2933	3	8800
Output inductor L_{V2} [mH]	4.8	936.2	2104	5	10518
Output capacitor C_{V1} [mF]	0.848	1800	1374	3	4121

Table XIX - Calculations for energy stored in reactive elements.

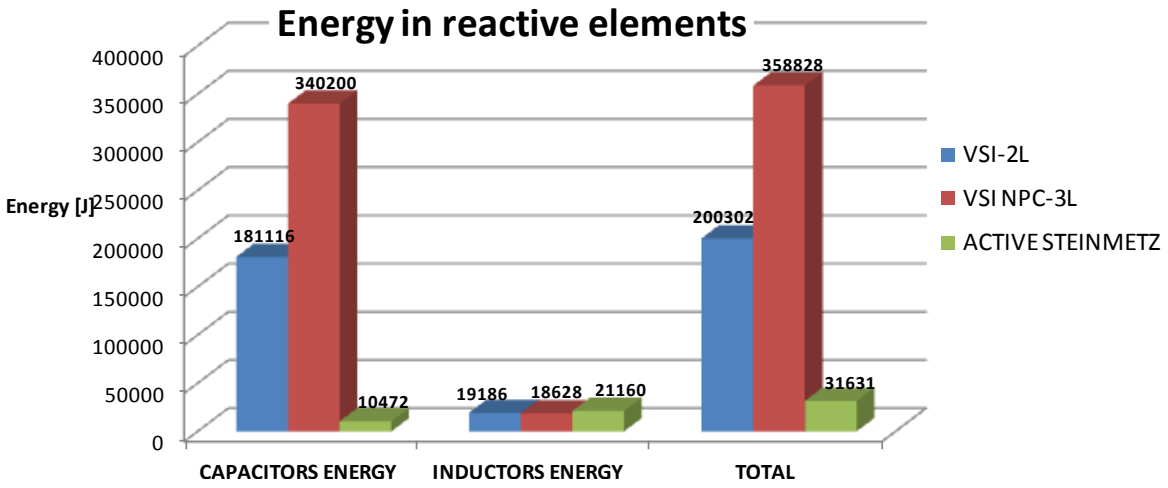


Fig. 173 – Comparison in terms of energy stored in reactive elements.

Comparing the energy stored in the reactive elements for the three topologies under study, a huge difference exists between the proposed compensator and the classical solutions based on VSI converters. Particularly for the size of the DC-link capacitors, the capacitive stored energy in these conversion structures is significant. In fact, as the converter is injecting a purely negative sequence 3-phase current, the fluctuating power makes it necessary to install large capacitors to limit the voltage ripple at the DC side.

VI.4 Simulations

The circuit simulator PSIM is used to validate the principle functioning of the compensator. The transmission power system, the substation at Evron and the balancer are modelled and simulated in PSIM using, first, the ideal waveforms for a train's current and line voltages. Following this, the measured currents and voltages are used as sources in the simulation to evaluate the functioning of the unbalance compensator in a real environment.

The lower short-circuit power, Scc = 295 MVA, is considered.

The compensator control scheme is reported in figure 174. The substation active power is measured and the power reference for the CCIs is calculated. Two control loops ensure that the power values for the two CCI follow the reference.

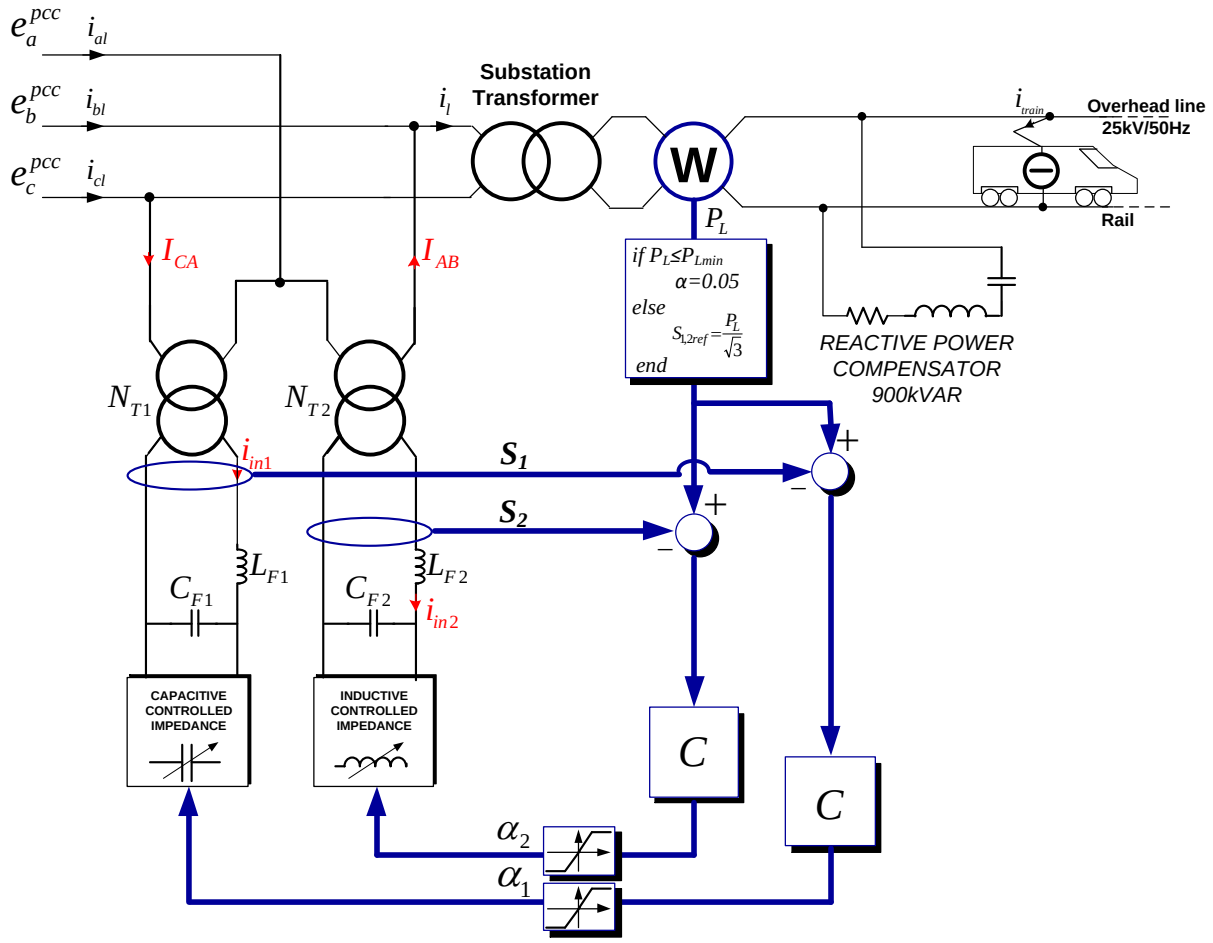


Fig. 174 - Control implemented in Psim.

Figure 175 shows the simulation results in the case of sinusoidal waveforms. The figure reports the substation power, the three-phase current drawn by the substation and at the bottom the voltage UF%.

A purely unitary power factor load is considered. First, the substation is unloaded and the circuit is balanced (UF% = 0). In the second stage, a load of 5 MW is put on the substation and the UF% is 0.5%. Finally a load of 10 MW is put on the substation and the UF% is kept under the limit of 1.5%.

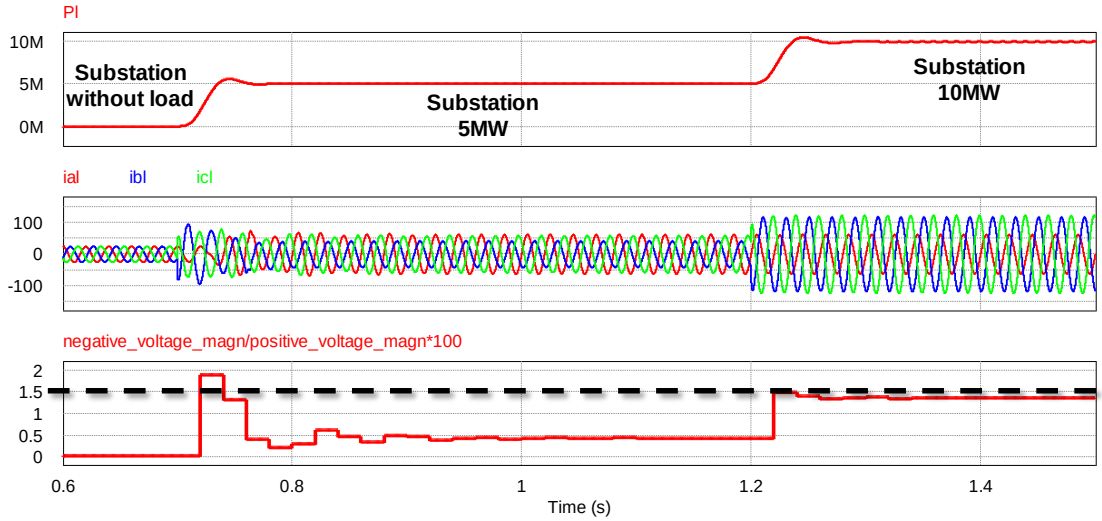


Fig. 175 - Simulation results in case of ideal waveforms.

Following this, the results of simulations carried out using the currents and voltages measured on site at Evron are presented. Controlled generators are used in the PSIM to impose line voltages and the train's current is measured.

The substation current is described in figures 176 and 177. The first figure shows the current, along with the active and reactive power of the load. The second figure presents the FFT of the current. This is the case of a 6-MW load with fairly high harmonic distortion. A 3rd harmonic of about 20 A is measured. The reactive power in this case has a low value. The resulting line currents and *UF*% are presented in figure 178.

Three working periods can be distinguished:

First, the substation is not loaded and appears as a balanced load to the power network.

Next, the substation is loaded and the *UF* reaches 2%.

Finally, the active Steinmetz compensator is turned on, and the UF is close to zero, varying widely under the limit of 1.5%.

In conclusion, figure 179 shows the details of the three-phase line currents and the currents drawn by the compensator.

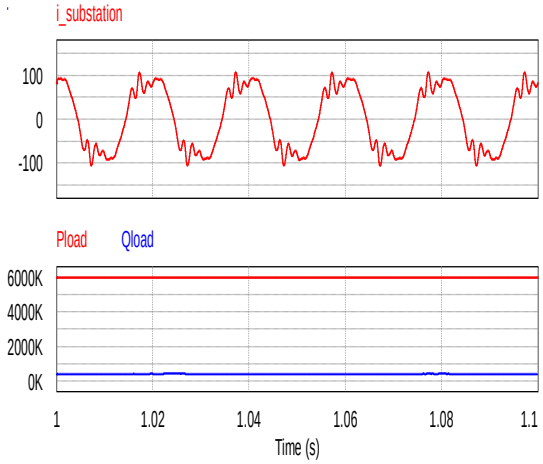


Fig. 176 - Substation current waveforms, active and reactive power.

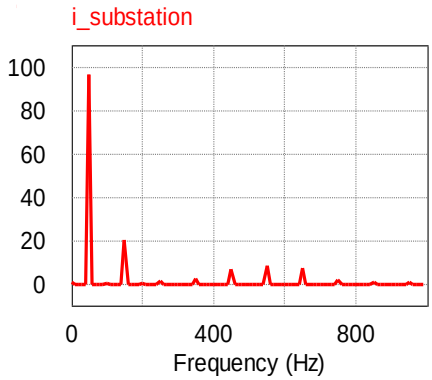


Fig. 177 - Substation current FFT.

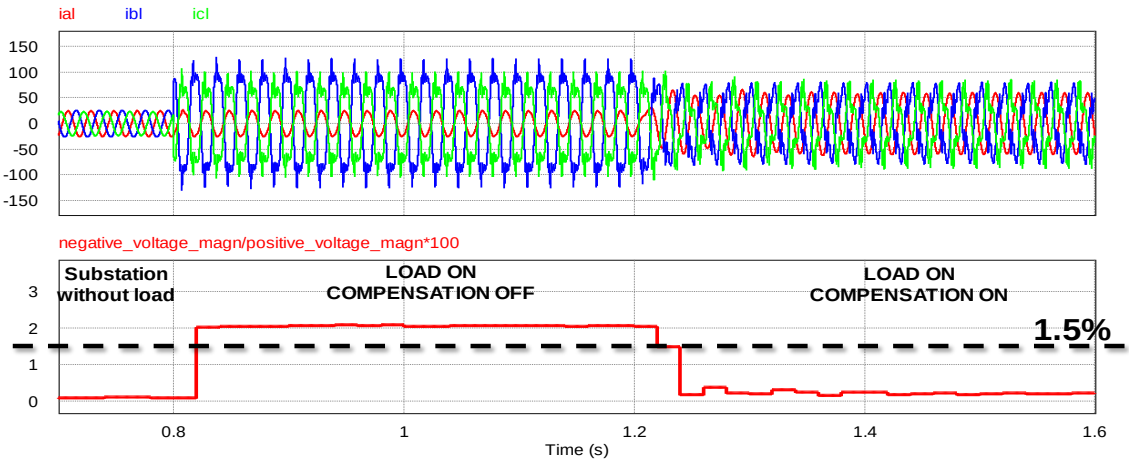


Fig. 178 – Line currents and VUF%.

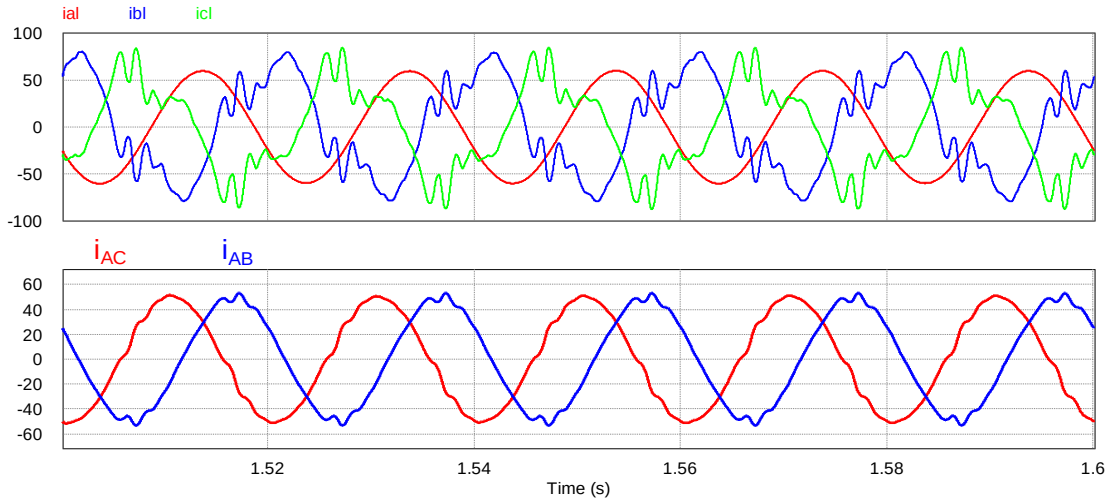


Fig. 179 – Line currents and injected currents i_{AB} and i_{CA}.

VI.5 Conclusions

This chapter explored the feasibility of using an active Steinmetz circuit based on CCI converters. A case study concerning a French substation has been considered. Measurements carried out at the substation allowed a compensator design and the possibility to consider real waveforms for the current and voltage in numerical simulations.

Despite the limited compensation domain of the presented topology, the study highlighted its feasibility in railway substations. In fact, in this kind of application, only an average compensation is enough to respect energy provider constraints. Therefore, the achieved reduction in power losses with respect to the widely used VSI topology makes the proposed solution very attractive for railway operators. Calculation and simulation results showed that the stored energy in the reactive elements was reduced by a factor of six, whereas the semiconductor losses were 40% lower.

The simulation results validated the correct operation of the novel topology even when real waveforms were considered.

The next chapter presents experimental results using a scaled prototype of the compensator.

Chapter VII. Active Steinmetz compensator-experimental results

With the view to validate the principle of the active Steinmetz circuit, a low power prototype was constructed at the LAPLACE laboratory. Two CCIs were built using IGBT devices. A single phase resistive load of about 2.2 kW was used to generate the unbalance.

The following sections describe this prototype and show some waveforms representative of the operation of the compensator.

VII.1 Prototype introduction

The diagram of the test bench is shown in figure 180. An autotransformer, connected to the 400 V/50 Hz power network of the laboratory, is used to get a variable three-phase voltage. Particularly, the tests reported in this section refer to a case where the secondary voltage was set to 300 V.

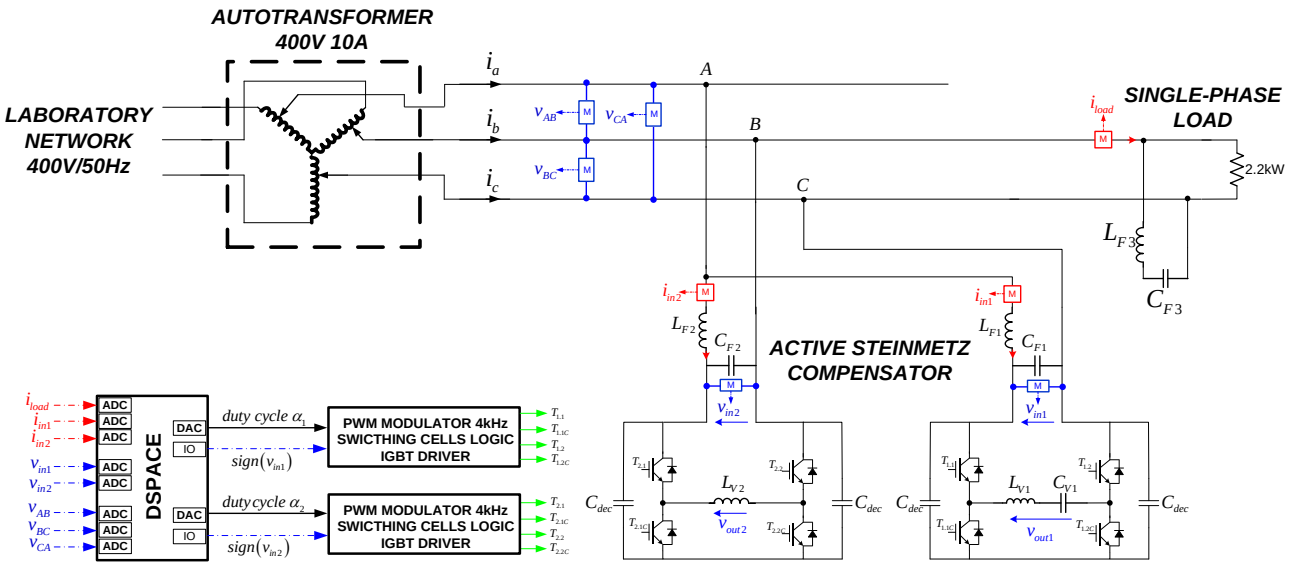


Fig. 180 - Test bench for experiments.

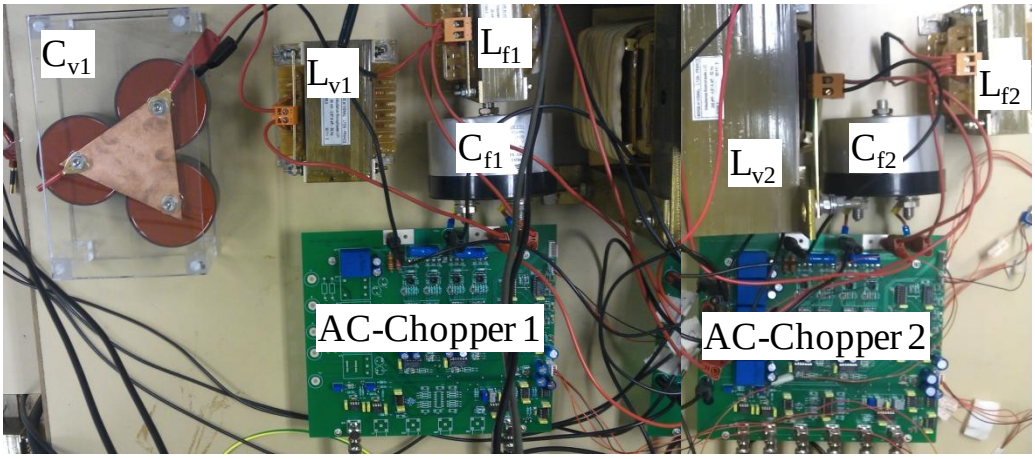


Fig. 181 - Picture of compensator prototype

The active Steinmetz compensator, shown in figure 181, is composed of two AC-Choppers using IGBTs (IRG4PH50KDPbF) from International Rectifiers. The main features of the used semiconductor devices are as follows:

- V_{CES} = 1200 V
- I_C (T_{case} = 100°C) = 24 A

The two AC chopper converters are realized on PCB, with each one containing:

- 4 IGBTs in a TO-247 package mounted on an aluminium heatsink,
- the IGBT drivers,
- the logic for switching cell selection according to the sign of the input voltage,
- the PWM modulator with a carrier set to f_{sw} = 4 kHz,
- a decoupling capacitor, C_{dec}, of 200 nF is connected in parallel to each switching cell in order to guarantee a path for the current during the dead time period (2 μs).

Regarding current and voltage measurements, LEM transducers (LA-25 and LV-25) are used.

At its input, each converter has a filter, L_F-C_F, to reduce the harmonic content of the current due to the PWM. At the output, the capacitive CCI is connected to inductor L_{V1} series associated to capacitor C_{V1}, while the inductive CCI supplies only an inductor, L_{V2}.

The values of the reactive elements used are listed in the following table:

Capacitive CCI	*Input Filter*	L_{F1}=20mH C_{F1}=5.6μF
	Output	L_{V1}=80mH C_{V1}=18μF
Inductive CCI	*Input Filter*	L_{F2}=20mH C_{F2}=5.6μF
	Output	L_{V1}=240mH

A resistor load is connected between phases B and C to cause the unbalance. It represents, at 300 V, a load of 2.2 kW. A capacitive impedance, L_{F3}-C_{F3}, with the same value as the converter input filter is installed in parallel. This emulates the reactive power compensator normally installed in substations and allows a balanced condition when no load is connected. The short circuit power at the autotransformer output is estimated at 110 kVA.

VII.2 Calculation

Using the equations of the CCI averaged model, the reactive power variation for each converter is shown in figure 182 as a function of the duty cycle. A 1.5kVA compensator is then achieved.

For each converter, the input voltage RMS value is reported in figure 183. As expected, due to the voltage drop on the input filter inductor, the input voltage of the capacitive CCI increases with the provided reactive power while for the inductive CCI, the voltage decreases with the reactive power level.

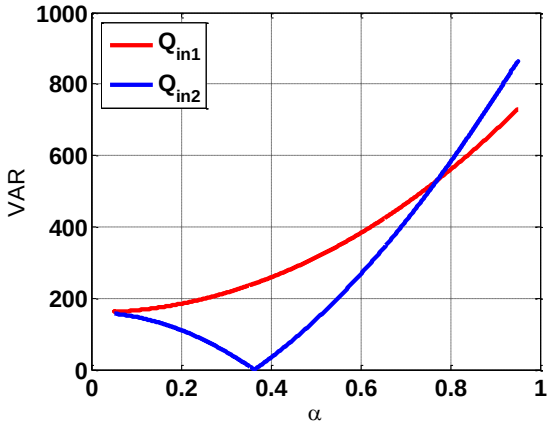


Fig. 182 - CCI power vs. duty cycle.

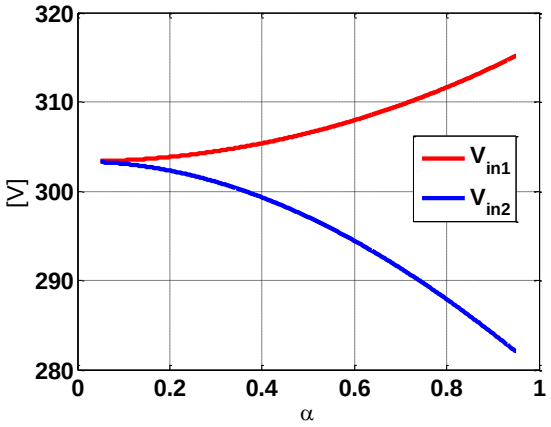


Fig. 183 – AC chopper input voltage vs. duty cycle.

Figure 184 reports the input currents, $I_{in1}(\alpha)$ and $I_{in2}(\alpha)$. These curves make it possible to point out some considerations on the compensator control. Let us note that they are different functions. Nevertheless, I_{in1} and I_{in2} must be equal in order to avoid power factor degradation. On this basis, $I_{in1}(\alpha)$ determines the maximum (I_{max}) and minimum (I_{min}) values for the input current reference. Moreover, as I_{in2} is capacitive up to α_{contr} , the closed loop control is validated only for $\alpha \geq \alpha_{contr.}$

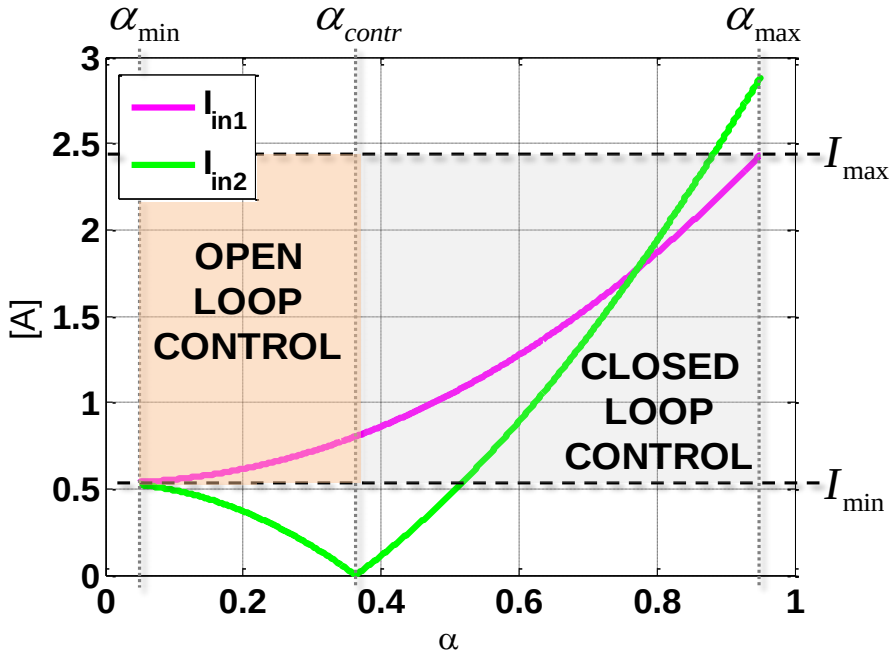


Fig. 184 - CCI input current vs. duty cycle.

VII.3 Control

A dSPACE prototyping system is used to control the input currents of the active Steinmetz compensator. A diagram is presented in figure 185. The algorithm calculates the reference current, I_{ref}, according to the load power level and generates the duty cycles α_1 and α_2. Moreover, it gives, to the pulse width modulators, two logic signals related to the signs of v_{in1} and v_{in2}.

VII.4 Experimental results

Experimental results obtained at 300 V are presented in this section. Measurements from current and voltage transducers were acquired and processed in dSPACE. Figure 186 shows the load current, along with the active power (2.2 kW) and reactive power (-160 VAR).

For the condition of a turned-off compensator, voltages v_{ab}, v_{bc} and v_{ca}, and the measured unbalance factor (2.1%) are reported in figure 187. Moreover, figure 188 shows input voltages $v_{in1,2}$, currents $i_{in1,2}$.

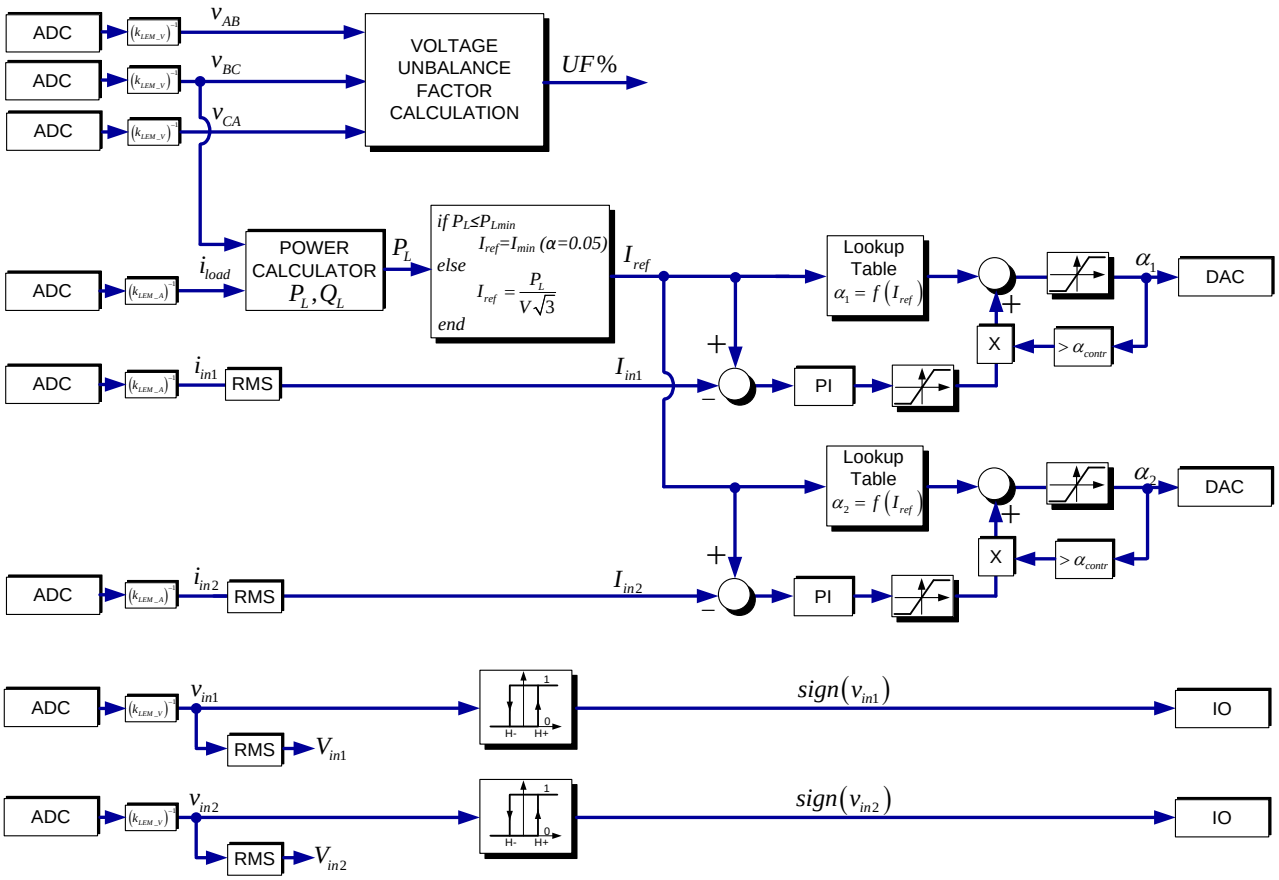


Fig. 185 - dSPACE bloc diagram.

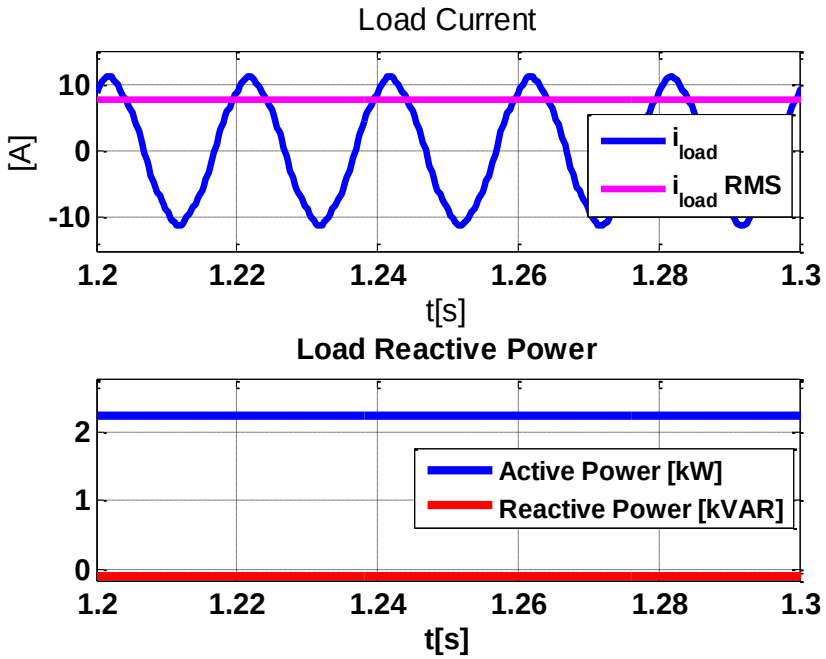


Fig. 186 - Load current and power.

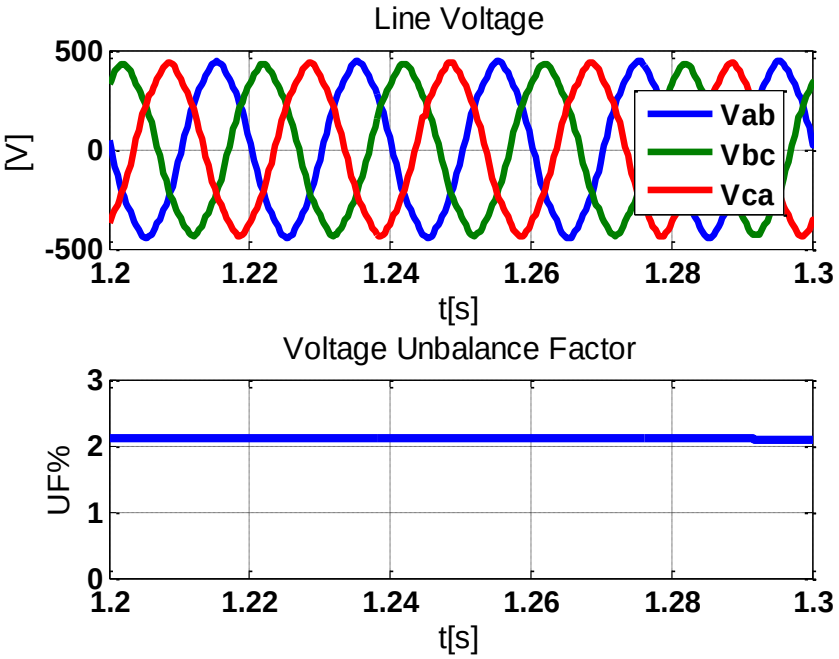


Fig. 187 - Line voltages BEFORE compensation.

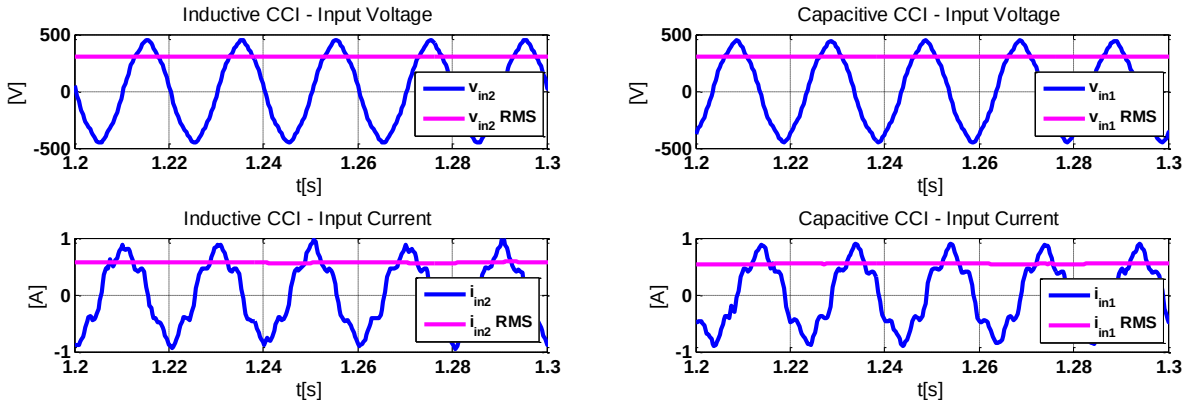


Fig. 188 - CCI input voltages v_{in1} and v_{in2} and currents i_{in1} and i_{in2} BEFORE compensation.

After the compensation, the voltage unbalance factor decreases to 0.55%, as reported in figure 189. Let us note that the unbalance factor is not reduced to zero as the compensator is not sized to totally compensate the unbalance.

Figure 190 shows input voltages $v_{in1,2}$, currents $i_{in1,2}$ and duty cycles $\alpha_{1,2}$ when the compensator is working in steady state. The value for RMS current $I_{in1,2}$ is 2.4 A. This is the maximum current, I_{max}, for the CCIs; in fact, in this case, I_{ref} is saturated because the requested current is about 4.5 A

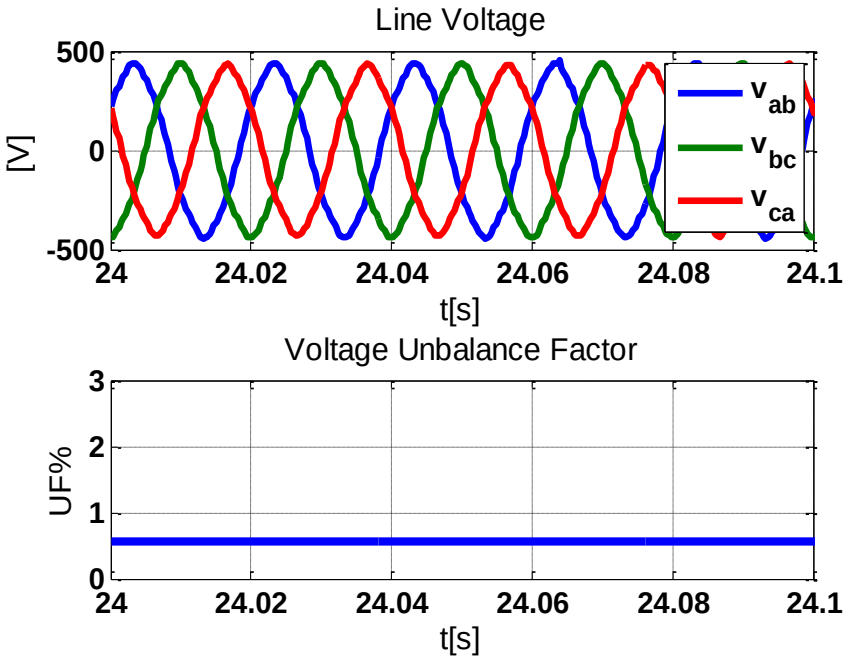


Fig. 189 - Line voltages AFTER compensation.

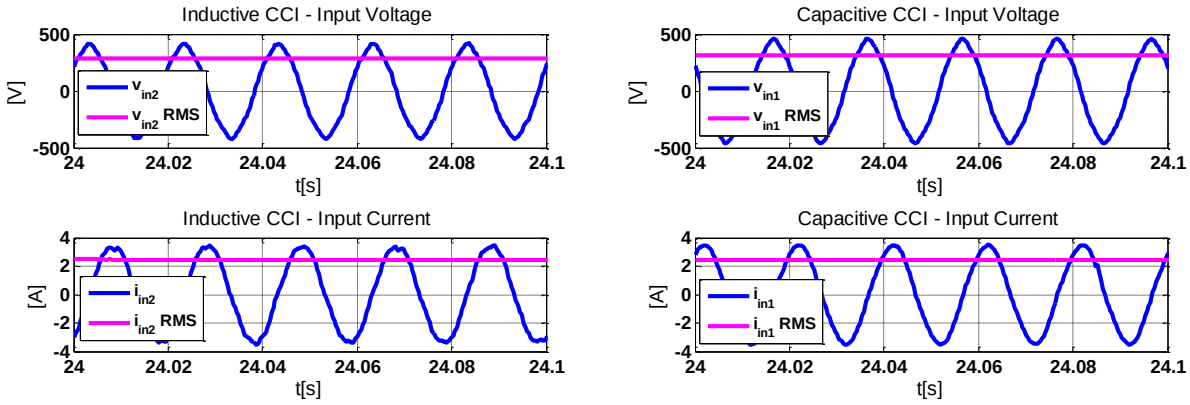


Fig. 190 - CCI input voltages v_{in1} and v_{in2} and currents i_{in1} and i_{in2} AFTER compensation.

Figure 191 reports the variation of currents $I_{in1,2}$, voltages $V_{in1,2}$ and the UF% during the compensation transient time fixed to 20 s. Current i_{in2} is capacitive for the first 9 s. After t = 20 s, both currents have the same rms value, $I_{in1,2}$ = 2.4 A.

Regarding the input voltages, as expected, V_{in1} increases for the capacitive CCI; otherwise, V_{in2} decreases for the inductive CCI.

Line currents measured with an oscilloscope are reported in figure 192 (before the compensation) and in figure 193 (after the compensation). The second figure shows how the current unbalance is reduced.

Finally, figure 194 shows voltages v_{out1} and v_{out2} and currents i_{in1} and i_{in2} in a steady state.

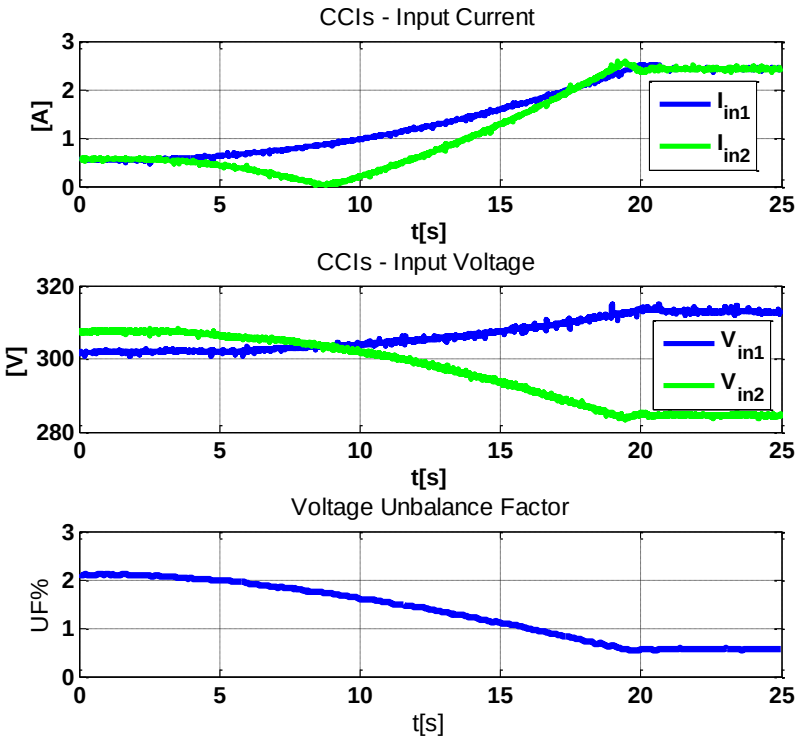


Fig. 191 - Compensation transient.

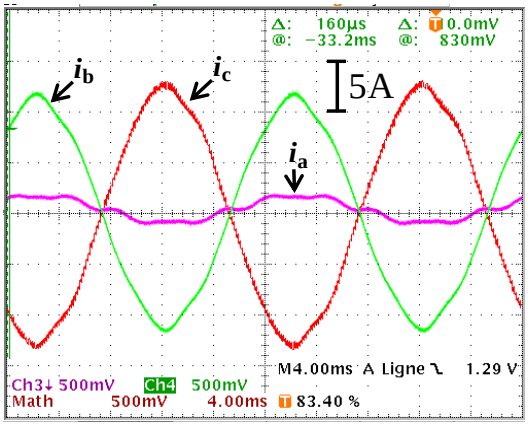


Fig. 192 – Line currents BEFORE compensation.

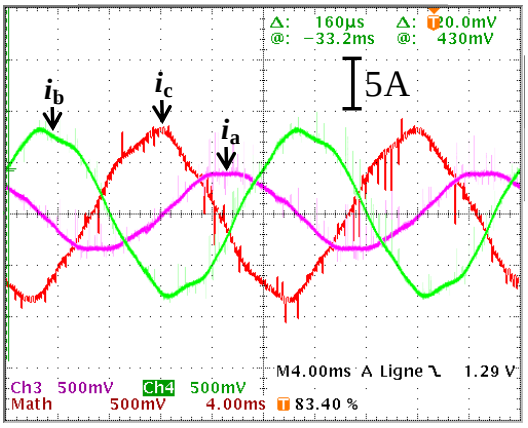


Fig. 193 - Line currents AFTER compensation.

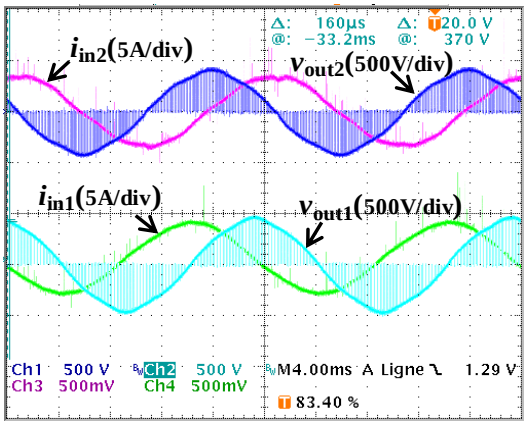


Fig. 194 - Voltages v_{out1} and v_{out2} and currents i_{in1} and i_{in2} AFTER compensation.

VII.5 Conclusions

This chapter presented experimental results carried out on a scaled demonstrator of Active Steinmetz compensator. The tests were carried out at the laboratory LAPLACE. Two AC Chopper converters were built and a DSpace system was used to implement the control. A resistive load was used to produce a voltage unbalance.

The results validate the principle functioning and demonstrate that the compensator is able to reduce the voltage unbalance factor.

Conclusion & Future Prospects

The 25kV/50Hz SNCF substations are more and more facing with power quality issues due to the traffic increasing. In most cases, in order to respect limits imposed by the energy provider or to guarantee the correct functioning of the railway network itself, the railways operator is obliged to install power electronics compensator at the substation.

Nowadays especially reactive power compensator and voltage unbalance compensator are needed in substations.

The first one allows avoiding penalties imposed by the energy provider related to the power factor degradation. Moreover it can boost the overhead line voltage when the traffic increases. This permits to avoid that the line voltage comes down to the minimum imposed by international standards (19kV).

On the other hand, the voltage unbalance compensator allows increasing the substation capability without exceeding the limit in unbalance factor fixed by the energy provider.

The railways operator, in selecting the compensators to install, can choose between several topologies available. Nevertheless, each type of compensator determines an increasing of functioning cost of the substation, especially due to the converter power losses.

The contributions of this dissertation concern the use of new topologies of power electronic compensators for 25kV/50Hz railways substations. Chopper Controlled Impedances are presented as conversion structures characterized by low losses in semiconductor devices and reduced volumes of reactive elements compared to classical solutions.

The proposed concept is analyzed for reactive power compensation and voltage unbalance compensation. Design criteria are presented using information obtained from measurements in two SNCF substations considered as case studies. Simulation results and experimental results validated the functioning principle of the compensators.

In unbalance compensation, the active Steinmetz topology is really attractive for railways operator. The low power losses allow significant cost reduction in substation functioning and maintenance costs while the reduced volume for reactive devices is conducive to a lower purchase cost.

A comparative study carried out between the proposed topology and the widely used Voltage Source Inverter compensators shows that power losses are about 60% lower and energy stored in reactive elements are reduced by a factor six.

For ten years, VSI and TCR solutions were tested by the French Railways. Logically, in the near future, a full scale unbalance compensator based on CCI could be build up and installed in a substation of the French network.

Appendix I Semiconductor power losses and thermal limits

This appendix presents the mathematical details followed to determine power losses of semiconductor devices and thermal limits for the different topologies of unbalance compensators. Thermal limit is defined as the working condition at which the junction temperature of a transistor or a diode of a semiconductor device composing the converter reaches the maximum allowed value. On this base the maximum converter power is pointed out.

The semiconductor device considered in the analytical calculation is an IGBT. The application considered is the unbalance compensation and the converter topologies analyzed are the PWM AC chopper, the 2 level VSI and the 3 level NPC VSI.

AI.1. Analytical expressions for power losses in semiconductor devices

The IGBT (Fig. 195) is a bidirectional current switching device. It is composed by an Insulated-Gate-Bipolar-Transistor and an anti-parallel diode that allows the current bidirectionality. The IGBT combines the advantages of a bipolar transistor (high voltage, high current) and of a MOSFET (fast commutations, low energy level command).

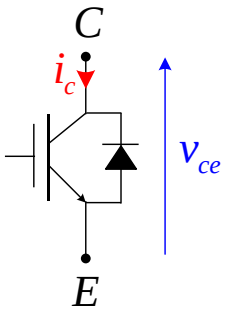


Fig. 195 - IGBT symbol

Condution Losses

The equivalent model of an IGBT during conduction is reported in figure 196. On this base the expression for voltage between collector and emitter when the transistor is conducting is:

$$v_{ce} = V_{T0} + r_T i \tag{120}$$

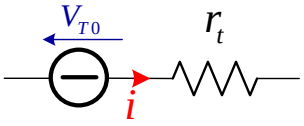


Fig. 196 – equivalent model of an IGBT during conduction

Parameters r_T and V_{T0} can be found from the $I_c=f(V_{ce})$ curve at 125°C on semiconductor datasheet .

Considering the i-th switching period for the device, if i_i is the current during the period $T_{ONi}=\alpha_i T_{sw}$ then the conduction energy lost is:

$$E_{cond_i} = T_{ONi}\left(V_{T0} i_i + r_T i_i^{\,2}\right) \tag{121}$$

On one period T_{net} of the fundamental, power losses can be evaluated as:

$$P_{cond} = \frac{1}{T_{net}} \sum_{i=1}^{n_{cond}} T_{ONi}\left(V_{T0} i_i + r_T i_i^{\,2}\right) \tag{122}$$

Where n_{cond} is the number of conduction period on one fundamental period.
Multiplying and dividing for T_{sw} lets introduce the duty cycle α in the formula:

$$P_{cond} = \frac{1}{T_{net}} \sum_{i=1}^{n_{cond}} \frac{T_{ONi}}{T_{sw}}\left(V_{T0} i_i + r_T i_i^{\,2}\right) T_{sw} = \frac{1}{T_{net}} \sum_{i=1}^{n_{cond}} \alpha_i \left(V_{T0} i_i + r_T i_i^{\,2}\right) T_{sw} \tag{123}$$

Considering the approximation of the summation in integral form $\sum_{i=1} f(x_i).\Delta x \approx \int f(x).dx$:

$$P_{cond} = \frac{1}{T_{net}} \sum_{i=1}^{n_{cond}} \alpha_i \left(V_{T0} i_i + r_T i_i^{\,2}\right) T_{sw} \approx \frac{1}{T_{net}} \int_{t_{cond1}}^{t_{cond2}} \alpha(t)\left(V_{T0} i(t) + r_T i(t)^2\right) dt \tag{124}$$

The analytical expression for conduction losses can be expressed also in an alternative form in case of the transistor conduction:

$$P_{cond_T} = V_{T0} I_T^{avg} + r_T \left(I_T^{rms}\right)^2 \tag{125}$$

Where I_T^{avg} and I_T^{rms} are the average and the rms values of the transistor current and depends on the considered converter topology.

An equivalent expression for the case of diode conduction losses is:

$$P_{cond_D} = V_{D0} I_D^{avg} + r_D \left(I_D^{rms}\right)^2 \tag{126}$$

In this case parameters r_D and V_{D0} are taken from the $I_F=f(V_F)$ curve of the diode at 125°C on semiconductor datasheet

Switching Losses

For the calculation of the switching loss, the constructor provide the characteristic at 125°C of the switching energy lost at the turn-on (E_{on}) and turn-off (E_{off}) of the transistor and due to reverse recovery charge current of the diode (E_{rec}).For switching energy losses, a square dependence on the switched current is assumed:

$$E_{on} = \left(a_{on} I_C^2 + b_{on} I_C + c_{on}\right)\frac{V_i}{V_{ref}} \tag{127}$$

$$E_{off} = \left(a_{off} I_C^2 + b_{off} I_C + c_{off}\right)\frac{V_i}{V_{ref}} \tag{128}$$

$$E_{rec} = \left(a_{rec} I_D^2 + b_{rec} I_D + c_{rec}\right)\frac{V_i}{V_{ref}} \tag{129}$$

All the relations are given for reference commutation voltage V_{ref} and real commuted voltage V_i.

The average switching losses on one fundamental period is found by summing the power lost each switching cycle and dividing by the number of cycle in one period. On this base, a continuous form solution may be found for systems where the carrier is much higher than the fundamental frequency. Thus switching losses for a device on period [t_{com1}, t_{com2}] can be evaluated as:

$$P_{sw} = \frac{1}{T_{net}}\frac{\sum_{i=1}^{n_{com}} E_i}{T_{sw}} T_{sw} \approx \frac{f_{sw}}{T_{net}} \int_{t_{com1}}^{t_{com2}} \left(ai(t)^2 + bi(t) + c\right)\frac{V_{DC}}{V_{ref}} dt \tag{130}$$

Where $E_i = E_{on} + E_{off} = \left(aI^2 + b\ I\ + c\right)\frac{V_i}{V_{ref}}$,

Considered IGBT

The considered switching device is an ABB single module IGBT, model 5SNA 1500E330300. Characteristics of this component taken in the constructor datasheet have been reported in the following table:

	IGBT 3,3 kV / 1,5 kA
Maximum continuous voltage (V)	1800
Switching Frequency (Hz)	1000
Switching Losses Parameters	a_{on}=3,29e-7 b_{on}=6,04e-4 c_{on}=0,35 a_{off}=7,14e-8 b_{off}=1,5e-3 c_{off}=0,35 a_{rec}=-2,2e-7 b_{rec}=1,4e-3 c_{rec}=0,35
Conduction Losses Parameters	V_{T0}=1,2 V r_T=1,4 m□ V_{D0}=1,2 V r_D=0,65 m□
Thermal Resistance (K/W)	$R_{TH\ j\text{-}c\ T}$=0,0085 $R_{TH\ c\text{-}s\ T}$=0,009 $R_{TH\ j\text{-}c\ D}$=0,017 $R_{TH\ c\text{-}s\ D}$=0,018

where

$R_{TH\ j\text{-}c\ T}$: IGBT thermal resistance junction to case

$R_{TH\ c\text{-}s\ T}$: IGBT thermal resistance case to heatsink

$R_{TH\ j\text{-}c\ D}$: Diode thermal resistance junction to case

$R_{TH\ c\text{-}s\ D}$: Diode thermal resistance case to heatsink

The thermal model considered for the IGBT module is presented in figure 197.

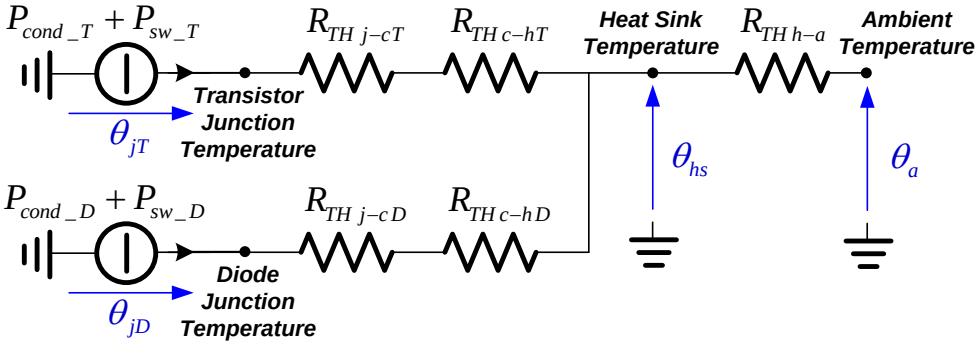


Fig. 197 - IGBT Thermal Model

Where:

θ_{jT} is the transistor junction temperature

θ_{jD} is the diode junction temperature

θ_{hs} is the heat sink temperature

On this base, the junction temperature for transistor and diode are expressed as (131) and (132).

$$\theta_{jT} = \left(R_{TH\ j-cT} + R_{TH\ j-sT}\right)\left(P_{cond_T} + P_{sw_T}\right) + \theta_{hs} \tag{131}$$

$$\theta_{jD} = \left(R_{TH\ j-cD} + R_{TH\ j-sD}\right)\left(P_{cond_D} + P_{sw_D}\right) + \theta_{hs} \tag{132}$$

The following hypothesis are made in the thermal analysis:

- The maximum junction temperature is 125°C
- The cooling system keeps the heat sink temperature at the fixed value of θ_{hs}=100°C.

AI.2. AC-Chopper converters

Power losses calculation in semiconductor devices is detailed for an AC-Chopper converter.

As the thermal limit of semiconductor functioning is searched, the maximum switched current that leads to the maximum junction temperature is pointed out.

Figure 198 shows a simple scheme for an AC Chopper converter. In the Active Steinmetz compensator, the converter draws a capacitive (Fig. 199) or an inductive current (Fig. 200). As the symmetry of the converter,

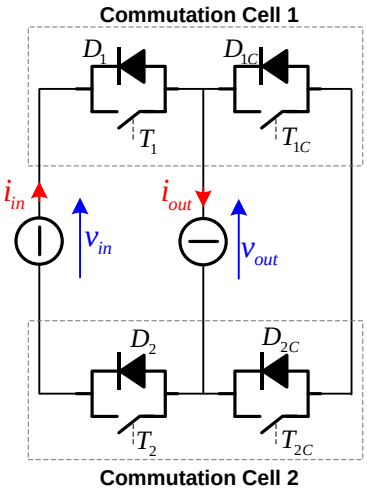


Fig. 198 – AC Chopper converter

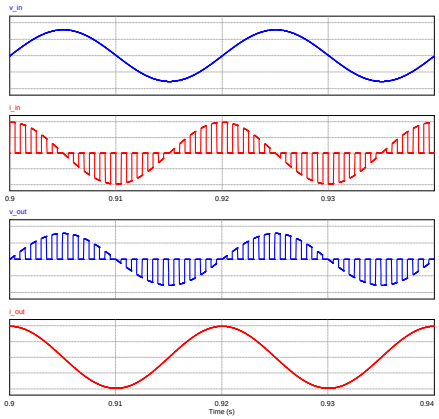


Fig. 199 – Waveforms for capacitive current

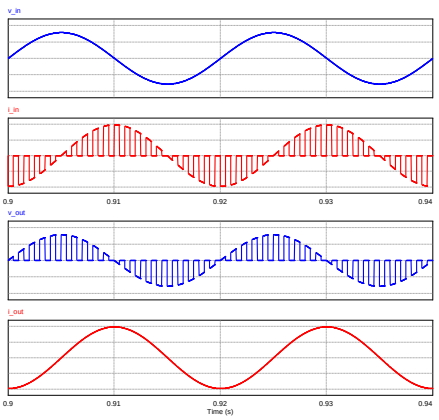


Fig. 200 - Waveforms for inductive current

both functioning mode present the same losses. On this hypothesis only the capacitive case is studied. The expressions for input voltage and the output current are the following:

$$v_{in} = V_{in}\sqrt{2}\sin(\omega t) \tag{133}$$

$$i_{out} = I_{out}\sqrt{2}\sin\left(\omega t + \frac{\pi}{2}\right) \tag{134}$$

An ideal current generator i_{out} is considered at the output.

a) Conduction losses

Let's consider the switching cell 1. Currents in transistors and diodes on one fundamental period are reported in figure 201. The conduction periods for devices in terms of angle are:

T1: [0, π/2] and [3π/2, 2π] with duty cycle α

D1: [π/2, 3/2π] with duty cycle α

T1c:[π/2, 3/2π] with duty cycle 1-α

D1c:[0, π/2] and [3π/2, 2π] with duty cycle 1-α

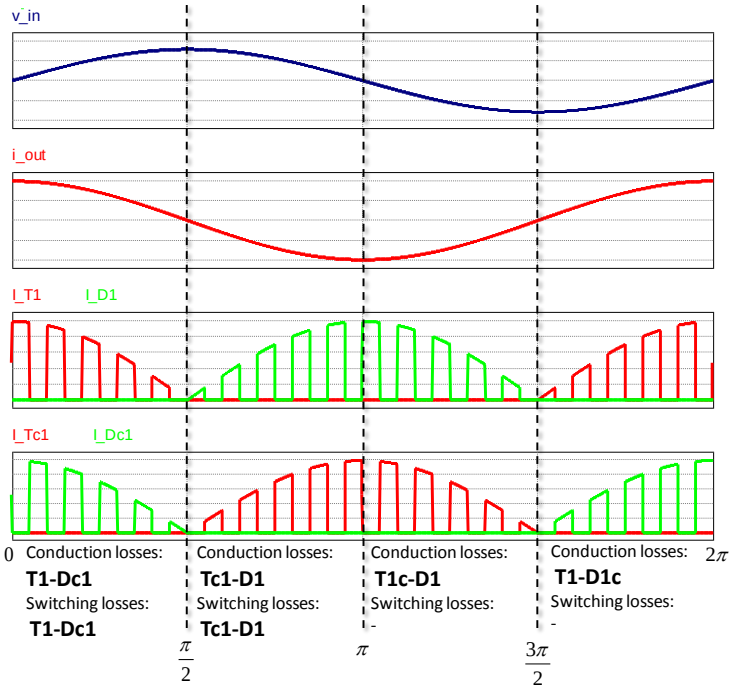


Fig. 201 - Waveform for switching cell 1 devices

Expressions used for losses calculation, are the following:

$$P_{cond_T1} = V_{T0} \cdot 2 \cdot \frac{1}{2\pi} \int_0^{\frac{\pi}{2}} \alpha \cdot i_{out}(\omega t) d\omega t + r_T \cdot 2 \cdot \frac{1}{2\pi} \int_0^{\frac{\pi}{2}} \alpha \cdot i_{out}(\omega t)^2 d\omega t = \\ = V_{T0} \alpha \frac{I_{out}\sqrt{2}}{\pi} + r_T \frac{\left(I_{out}\sqrt{2}\right)^2}{4} \alpha \tag{135}$$

$$P_{cond_T1C} = V_{T0} \frac{1}{2\pi} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} (1-\alpha) \cdot -i_{out}(\omega t) d\omega t + r_T \frac{1}{2\pi} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} (1-\alpha) \cdot i_{out}(\omega t)^2 d\omega t = \\ = V_{T0} (1-\alpha) \frac{I_{out}\sqrt{2}}{\pi} + r_T \frac{\left(I_{out}\sqrt{2}\right)^2}{4} (1-\alpha) \tag{136}$$

$$P_{cond_D1} = V_{D0} \frac{1}{2\pi} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \alpha \cdot -i_{out}(\omega t) d\omega t + r_D \frac{1}{2\pi} \int_{\frac{\pi}{2}}^{\frac{3\pi}{2}} \alpha \cdot i_{out}(\omega t)^2 d\omega t = \\ = V_{D0} \alpha \frac{I_{out}\sqrt{2}}{\pi} + r_D \frac{\left(I_{out}\sqrt{2}\right)^2}{4} \alpha \tag{137}$$

$$P_{cond_D1C} = V_{D0} \cdot 2 \cdot \frac{1}{2\pi} \int_0^{\frac{\pi}{2}} (1-\alpha) \cdot i_{out}(\omega t) d\omega t + r_D \cdot 2 \cdot \frac{1}{2\pi} \int_0^{\frac{\pi}{2}} (1-\alpha) \cdot i_{out}(\omega t)^2 d\omega t =$$
$$= V_{D0}(1-\alpha) \frac{I_{out}\sqrt{2}}{\pi} + r_D \frac{\left(I_{out}\sqrt{2}\right)^2}{4}(1-\alpha) \quad (138)$$

The converter duty cycle α is considered constant in the period of the fundamental voltage of the power system.

Due to the symmetrical functioning of the switching cell, expressions for T_2, D_{2C}, T_{2C} and D_2 are respectively equal to the ones obtained for T_1, D_{1C}, T_{1C} and D_1.

b) Switching losses

Each device switches only for ¼ of the fundamental period. This is one of the advantages of the AC Chopper converter. As a consequence of the symmetry in the switching pattern, the two IGBTs of the cell have the same switching losses. Power losses expressions are evaluated as following:

$$P_{sw_T1} = P_{sw_T1C} = \frac{f_{dec}}{2\pi} \int_0^{\frac{\pi}{2}} \frac{v_{in}(t)}{V_{ref}} \left[(a_{on} + a_{off}) i_{out}(t)^2 + (b_{on} + b_{off}) i_{out}(t) + (c_{on} + c_{off}) \right] d\omega t =$$
$$= \frac{f_{dec}}{2\pi} . \frac{V_{in}\sqrt{2}}{V_{ref}} . \left[\frac{(I_{out}\sqrt{2})^2}{3} . (a_{on} + a_{off}) + \frac{I_{out}\sqrt{2}}{2} . (b_{on} + b_{off}) + (c_{on} + c_{off}) \right] \quad (139)$$

$$P_{sw_D1} = P_{sw_D1C} = \frac{f_{dec}}{2\pi} \int_{\frac{\pi}{2}}^{\pi} \frac{v_{in}(t)}{V_{ref}} \left[a_{rec} i_{out}(t)^2 + b_{rec} i_{out}(t) + c_{rec} \right] d\omega t =$$
$$= \frac{f_{sw}}{2\pi} \frac{V_{in}\sqrt{2}}{V_{ref}} \left[\frac{\left(I_{out}\sqrt{2}\right)^2}{3} a_{rec} + \frac{I_{out}\sqrt{2}}{2} b_{rec} + c_{rec} \right] \quad (140)$$

Due to the symmetrical functioning of the switching cell, losses expressions for T_2, D_{2C}, T_{2C} and D_2 are respectively equal to the ones obtained for T_1, D_{1C}, T_{1C} and D_1.

Remark: All equations reported are related to an AC-Chopper working in buck mode. For converter working in boost mode, equations al obtained swapping i_{out} with i_{in} and v_{in} with v_{out} in the expressions present above.

c) Thermal Limits

Using the presented expressions for losses and temperature calculation, the thermal limit for AC Chopper converter conducing a capacitive or inductive current is calculated.

The heat sink temperature is considered fixed at θ_{hs}=100°C and the duty cycle is fixed to its maximum value $\alpha=0.95$.

The variation of junctions temperatures for transistors and diodes of a switching cell are plotted in figure 202 in function of the peck value of the output current. The maximum current allowed is 735A (1040A peak value) that determines a junction temperature of 125°C.

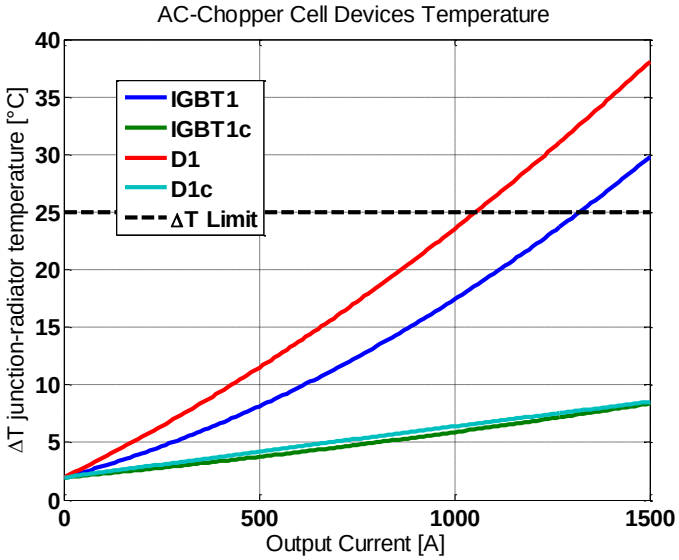


Fig. 202 – Junction temperature variation vs switched current

AI.3. 3-phase VSI 2-level converter

Thermal limits for VSI 2-L is studied when the converters draw a negative current sequence. The aim is to find the maximum current of negative sequence that gives the maximum junction temperature for diodes or transistors.

Losses expressions are pointed out for a single leg of the converter. Figure 203 reports the considered switching cell.

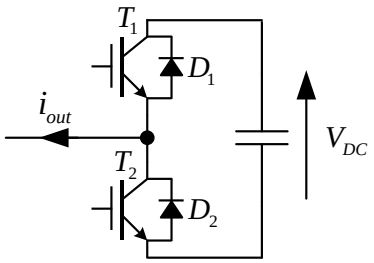


Fig. 203 – 2-L VSI Switching cell

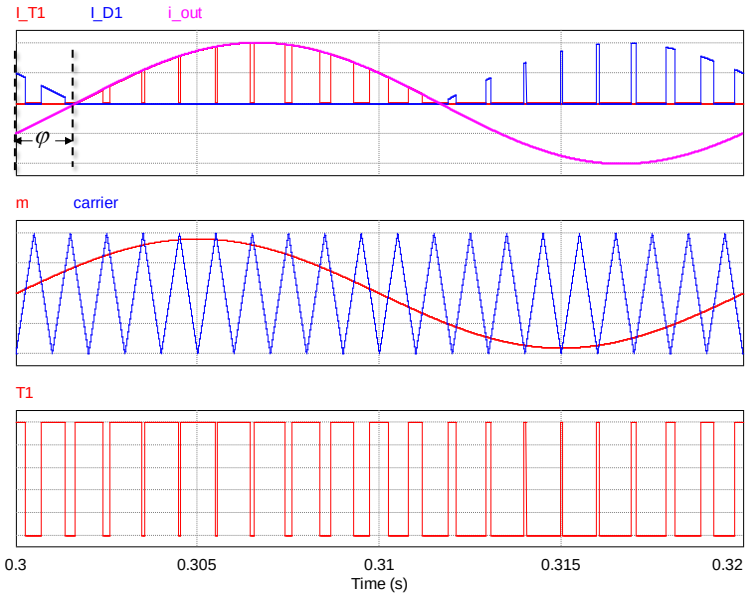


Fig. 204 - IGBT1 waveforms

IGBT1 and IGBT2 switch in complementary way and they present the same losses as the switching cell symmetry. Typical waveforms for IGBT1 are reported in figure 204. The modulation index and the output current expressions are:

$$m(t) = m_a \sin(\omega t) \tag{141}$$

$$i_{out} = I_{out}\sqrt{2}\sin(\omega t - \varphi) \tag{142}$$

Transistor T1 conducts in period [φ, $\varphi+\pi$]. Diode Di conducts in interval [$\varphi+\pi$, $\varphi+2\pi$]. In this interval, the duty cycle for transistor T1 and diode D1 is:

$$\alpha_1 = \frac{1}{2}\left(1 + m_a \sin(\omega t)\right) \qquad 0 < m_a < 1 \tag{143}$$

a) Conduction losses

The average and rms values for currents in transistor T1 and diode D1 are calculated:

$$I_{T1}^{avg} = I_{T2}^{avg} = \frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} i_{out}(t)\alpha_1(t)d\omega t = \frac{I_{out}\sqrt{2}}{4\pi}\left(2 + \frac{m_a}{2}\pi\cos(\varphi)\right) \tag{144}$$

$$I_{D1}^{avg} = I_{D2}^{avg} = \frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} -i_{out}(t)\alpha_1(t)d\omega t = \frac{I_{out}\sqrt{2}}{4\pi}\left(2 - \frac{m_a}{2}\pi\cos(\varphi)\right) \tag{145}$$

$$I_{T1}^{rms} = I_{T2}^{rms} = \sqrt{\frac{1}{2\pi}\int_{\varphi}^{\varphi+\pi} i_{out}(t)^2\alpha_1(t)d\omega t} = I_{out}\sqrt{\frac{m_a}{12\pi}\left(\frac{3\pi}{m_a} + 8\cos(\varphi)\right)} \tag{146}$$

$$I_{D1}^{rms} = I_{D2}^{rms} = \sqrt{\frac{1}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi} i_{out}(t)^2 \alpha_1(t) d\omega t} = I_{out}\sqrt{\frac{m_a}{12\pi}\left(\frac{3\pi}{m_a} - 8\cos(\varphi)\right)} \tag{147}$$

Using the last results, expressions (125) and (126) can be evaluated to calculate conduction losses

b) Switching losses

Switching losses can be evaluated solving integrals:

$$\begin{aligned} P_{sw_T1} = P_{sw_T2} &= \frac{f_{sw}}{2\pi}\int_{\varphi}^{\varphi+\pi}\left(\left(a_{on}+a_{off}\right)i_{out}(t)^2 + \left(b_{on}+b_{off}\right)i_{out}(t) + \left(c_{on}+c_{off}\right)\right)\frac{V_{DC}}{V_{ref}} d\omega t \\ &= f_{sw}\frac{V_{DC}}{V_{ref}}\left[\frac{I_{out}{}^2}{2}(a_{on}+a_{off}) + \frac{I_{out}\sqrt{2}}{\pi}(b_{on}+b_{off}) + \frac{1}{2}(c_{on}+c_{off})\right] \end{aligned} \tag{148}$$

$$\begin{aligned} P_{sw_D1} = P_{sw_D2} &= \frac{f_{sw}}{2\pi}\int_{\varphi+\pi}^{\varphi+2\pi}\left(\left(a_{on}+a_{off}\right)i_{out}(t)^2 - \left(b_{on}+b_{off}\right)i_{out}(t) + \left(c_{on}+c_{off}\right)\right)\frac{V_{DC}}{V_{ref}} d\omega t = \\ &= f_{sw}\frac{V_{in}}{V_{ref}}\left[\frac{I_{out}{}^2}{2}a_{rec} + \frac{I_{out}\sqrt{2}}{\pi}b_{rec} + \frac{1}{2}c_{rec}\right] \end{aligned} \tag{149}$$

c) Thermal Limits

The aim is to determine the maximum negative component that the converter can compensate at the thermal limit.

An iterative numerical algorithm is used to calculate the junctions temperature varying negative current magnitude and phase. As result, the maximum negative sequence is I_{-MAX}=508A.

Junction temperature for variation of negative component phase are plotted in figure 205 for the top igbts of the three legs (a,b,c). Let's note that the limits is given by the diodes.

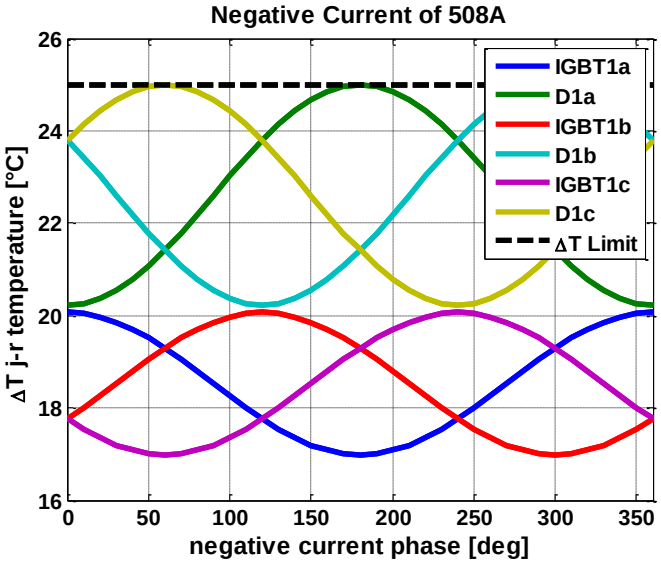


Fig. 205 - Junctions temperature variation vs negative current phase for 508A

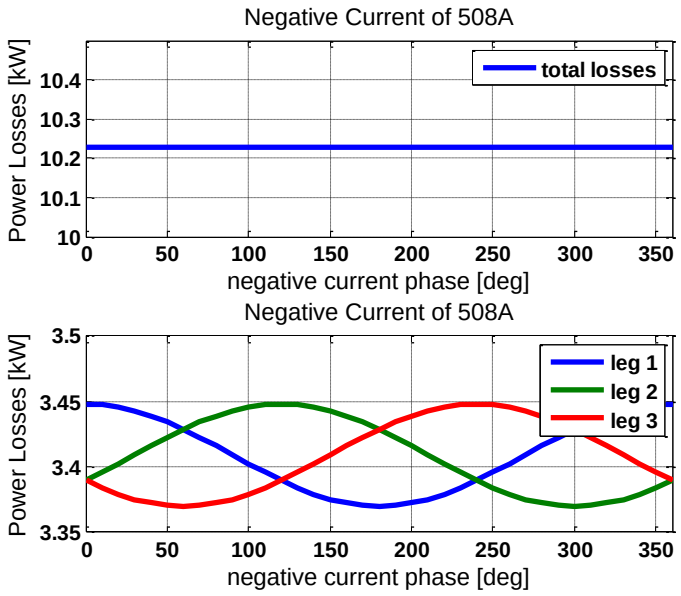


Fig. 206 – Power losses vs negative current phase for 508A

AI.4. 3-phase NPC-3level converter

Thermal limits for VSI 3-L NPC is studied when the converters draw a negative current sequence. Expression for losses are evaluated for one converter leg (Fig. 207). It is made of two cells and two clamp diodes. By using a sinusoidal PWM strategy it is observed that 3L-NPC topology has only three commutation states: P, O and N (Fig. 208). The zero state (state O) is obtained when the inner switches S2(T2-D2) and S3(T3-D3) are turned on. In this case, the load current passes through two different paths, depending on its direction. Table XX shows the possible current paths with the corresponding devices, according to the output current sign.

Figure 209 reports a simple scheme of PWM modulator for NPC three-level inverter. The modulation signal is sinusoidal and there are two triangular carriers, one for each couple of IGBTs. For couple S1-S3 the triangular carrier goes from 0 to 1 with frequency f_{sw}. Instead, for couple S2-S4 the carrier goes from 0 do -1 and it is 180° shifted respect to the first one.

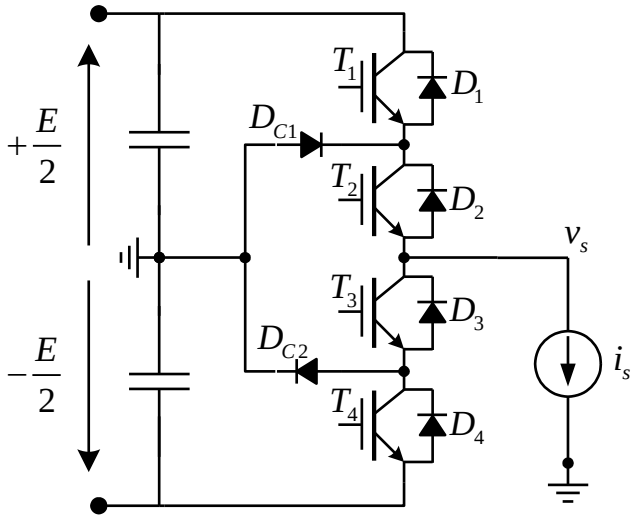


Fig. 207 - 3Level NPC Inverter legs

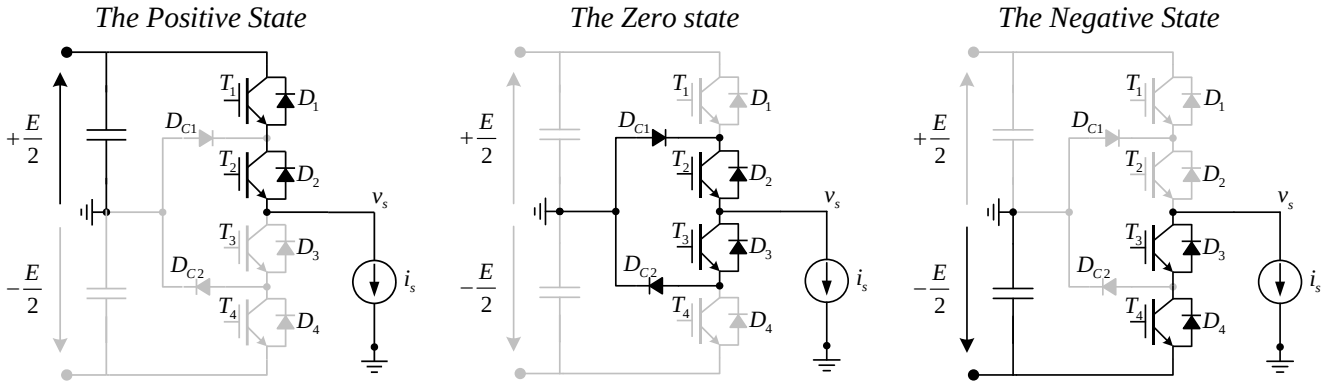


Fig. 208 - Possible NPC Configurations

Current Sign	Devices	Output Voltage [V]
$i_s>0$	T_1,T_2	+E/2
	D_{C1},T_2	0
	D_4, D_3	-E/2
$i_s<0$	T_3,T_4	-E/2
	T_3,D_{C2}	0
	D_1, D_2	+E/2

Table XX – Possible Current Paths in NPC 3-Level Inverter

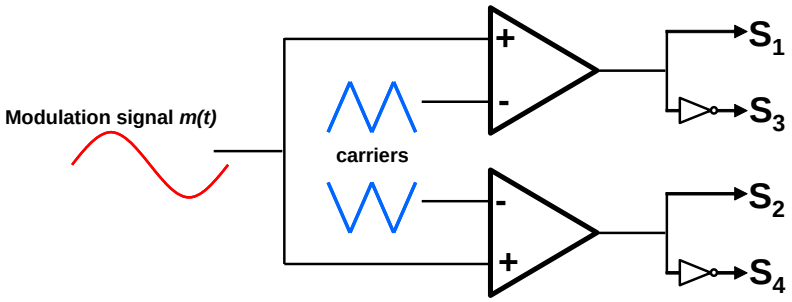


Fig. 209 - Switching Modulator

In order to perform the analysis, a generic load current has been considered:

$$i_s(t) = I\sqrt{2}\,sin(\omega t - \theta) \qquad (150)$$

Figure 210 the switched voltage v_s and the output current i_s has been reported.

The fundamental period, as it is remarked in the figure, can be divided into 4 intervals. In each interval it is possible to define which the active devices are.

Figure 211 reports carrier, modulation signals and the corresponding switching pattern. A resume has been carried out in Table XXI, where conducting devices are reported according to the converter state and the interval.

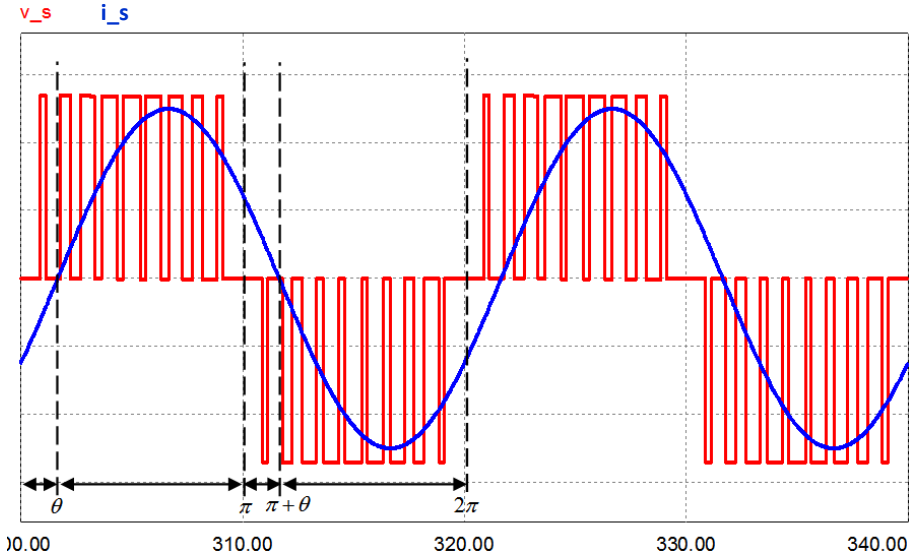


Fig. 210 - Three level NPC - Converter output voltage and current waveforms

Conduction interval	Current Sign	Device Positive State v_s=E/2	Device Zero State v_s=0	Device Negative State v_s=-E/2
$[0,\theta]$	i_s<0	D_1,D_2	T_3,D_{C2}	-
$[\theta,\pi]$	i_s>0	T_1,T_2	T_2,D_{C1}	-
$[\pi,\pi+\theta]$	i_s>0	-	T_2,D_{C1}	D_3,D_4
$[\pi+\theta,2\pi]$	i_s<0	-	T_3,D_{C2}	T_3,T_4

Table XXI – Conducting Devices

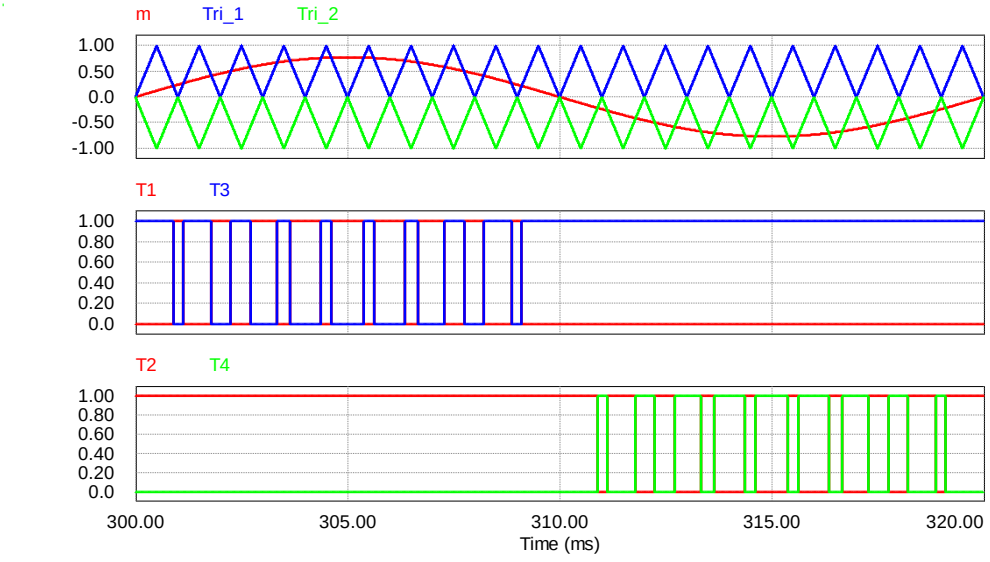


Fig. 211 - Three level NPC – PWM switching pattern

a. Average and rms current values in the semiconductor devices

Switching signal for devices T_1 and T_3 are complementary. The same is for the couple T_2 and T_4. Moreover, each couple works for half period of modulation signal *:*

$$m(t) = M\sin(\omega t) \tag{151}$$

When positive voltage v_s is desired, T_1 and T_3 are activated alternatively, T_2 is hold on, and T_4 is off. The value for output voltage v_s depends only on the state of couple T_1-T_3. If T_1 is on, T_3.is off and the switched voltage is E/2. In the opposite case, the output voltage is zero. The current flows in the transistor or in the diode according to the its sign.

The same considerations are valid in case of negative output voltage, T_2 and T_4 switch alternatively, T_3 is always on, and T_1 is off.

In order to evaluate the correct expressions for currents, the variation of duty cycle during switching intervals has to be taken in account. Thus, three modulation functions describing the duty cycle variation are used, as described in Table XXII, and plotted in 212.

	T_1	**D_1**	**T_2**		**D_2**	**D_{C1}**	
Interval	[θ,π]	[0,θ]	[θ,π]	[π,π+θ]	[0,θ]	[θ,π]	[π,π+θ]
$f_m(t)$	$f_{m1}(t)$ $M\sin(\omega t)$	$f_{m1}(t)$ $M\sin(\omega t)$	1	$f_{m2}(t)$ $1+M\sin(\omega t)$	$f_{m1}(t)$ $M\sin(\omega t)$	$f_{m3}(t)$ $1-M\sin(\omega t)$	$f_{m2}(t)$ $1+M\sin(\omega t)$

Table XXII- Modulation Functions

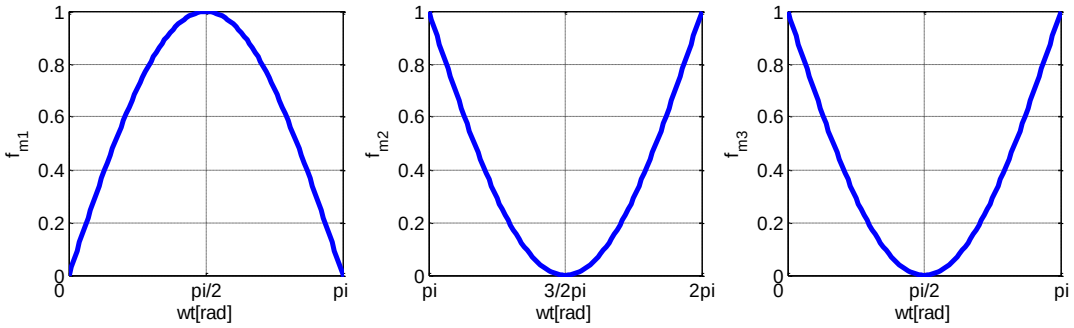


Fig. 212 – NPC duty cycles

Following, for all the semiconductor devices, expressions for drawn currents have been find out. Actually, due to the symmetry behaviour of the converter, it is enough to study the currents in S_1, S_2 and D_{C1}.

IGBT S_1

- *Transistor* T_1

Switching pattern for T_1 is in the range [0,π]. Moreover, due to the current sign, conduction for T_1 is only in [θ,π]. In this range the duty cycle variation is sinusoidal. Its initial value is 0, its maximum is for θ=π/2 and it is 0 at θ=π/2. Thus, modulation function used for current calculation is:

$$f_{m1}(t) = M\sin(\omega t) \quad \omega t \in [0,\pi] \tag{152}$$

The expressions for average and rms currents for T_1 are found:

$$I_{T_1}^{avg} = \frac{1}{2\pi}\int_{\theta}^{\pi} I\sqrt{2}\sin(\omega t-\theta)\cdot f_{m1}(t)\cdot d\omega t = \frac{I\sqrt{2}M}{4\pi}\left[(\pi-\theta)\cos(\theta)+\sin(\theta)\right] \tag{153}$$

$$I_{T_1}^{rms} = \sqrt{\frac{1}{2\pi}\int_{\theta}^{\pi}\left(I\sqrt{2}\sin(\omega t-\theta)\right)^2\cdot f_{m1}(t)\cdot d\omega t} = I\sqrt{\frac{M}{2\pi}\left[1+\frac{4}{3}\cos(\theta)+\frac{1}{3}\cos(2\theta)\right]} \tag{154}$$

- *Diode D_1*

Diode D_1 conducts in $[0,\theta]$ when the current is negative. The modulation function is the same for the previous case. Average and rms values for currents are:

$$I_{D_1}^{avg} = \frac{1}{2\pi}\int_{0}^{\theta} -I\sqrt{2}\sin(\omega t-\theta)\cdot f_{m1}(t)\cdot d\omega t = \frac{I\sqrt{2}M}{4\pi}\left[\sin(\theta)-\theta\cos(\theta)\right] \tag{155}$$

$$I_{D_1}^{rms} = \sqrt{\frac{1}{2\pi}\int_{0}^{\theta}\left(-I\sqrt{2}\sin(\omega t-\theta)\right)^2\cdot f_{m1}(t)\cdot d\omega t} = I\sqrt{\frac{M}{2\pi}\left[1-\frac{4}{3}\cos(\theta)+\frac{1}{3}\cos(2\theta)\right]} \tag{156}$$

IGBT S_2

- *Transistor* T_2

Transistor T_2 is switched on during al the semi-period for positive output voltage. Moreover it conducts only in $[\theta,\pi]$ when the current is positive.

Besides, it commutes in $[\pi,\pi+\theta]$. Considering the duty cycle variation for T_2, for $\theta=\pi/2$ it is maximum, for $\theta=3\pi/2$ it is 0 , and it is again maximum at $\theta=2\pi$. Thus, modulation function used for current calculation is

$$f_{m2}(t) = 1+M\sin(\omega t) \quad \omega t \in [\pi,2\pi] \tag{157}$$

The expressions for average and rms currents for T_2 are calculated:

$$I_{T_2}^{avg} = \frac{1}{2\pi}\int_{\theta}^{\pi} I\sqrt{2}\sin(\omega t-\theta)\cdot d\omega t + \frac{1}{2\pi}\int_{\pi}^{\pi+\theta} I\sqrt{2}\sin(\omega t-\theta)\cdot f_{m2}(t)\cdot d\omega t = \\ = \frac{I\sqrt{2}M}{4\pi}\left[\frac{4}{M}+\theta\cos(\theta)-\sin(\theta)\right] \tag{158}$$

$$I_{T_2}^{rms} = \sqrt{\frac{1}{2\pi}\int_{\theta}^{\pi}\left(I\sqrt{2}\sin(\omega t-\theta)\right)^2\cdot d\omega t + \frac{1}{2\pi}\int_{\pi}^{\pi+\theta}\left(I\sqrt{2}\sin(\omega t-\theta)\right)^2\cdot f_m(t)\cdot d\omega t} = \\ = \sqrt{\frac{1}{2}+\frac{M}{2\pi}\left(-1+\frac{4}{3}\cos(\theta)-\frac{\cos(2\theta)}{3}\right)} \tag{159}$$

- *Diode D_2*

Diode D_2 has the same behaviour of D_1. The two diodes always conduct together. Thus, the same expression for average and rms currents are considered.

Diode D_{C1}

Diode D_{C1} conducts and commutes when the current is positive. During interval $[\theta,\pi]$ it switches with a duty cycle inverse respect to T_1. So the modulation function considered is:

$$f_{m3}(t)=1-M\sin(\omega t)\quad \omega t\in[0,\pi] \tag{160}$$

On the other hand, during $[\pi,\pi+\theta]$ the duty cycle is the same of T_2.

$$I_{D_{C1}}^{avg}=\frac{1}{2\pi}\int_{\theta}^{\pi} I\sqrt{2}\sin(\omega t-\theta)\cdot f_{m3}(t)d\omega t+\frac{1}{2\pi}\int_{\pi}^{\pi+\theta} I\sqrt{2}\sin(\omega t-\theta)\cdot f_{m2}(t)\cdot d\omega t=$$
$$=\frac{I\sqrt{2}M}{4\pi}\left[\frac{4}{M}-(\pi-2\theta)\cos(\theta)-2\sin(\theta)\right] \tag{161}$$

$$I_{D_{C1}}^{rms}=\sqrt{\frac{1}{2\pi}\int_{\theta}^{\pi}\left(I\sqrt{2}\sin(\omega t-\theta)\right)^2\cdot f_{m3}(t)d\omega t+\frac{1}{2\pi}\int_{\pi}^{\pi+\theta}\left(I\sqrt{2}\sin(\omega t-\theta)\right)^2\cdot f_{m2}(t)\cdot d\omega t}=$$
$$=I\sqrt{\frac{1}{2}+\frac{M}{2\pi}\left(-1+\frac{4}{3}\cos(\theta)-\frac{1}{3}\cos(2\theta)\right)} \tag{162}$$

Expressions for currents in the other devices S_3, S_4 and D_{C2}., can be found for symmetry as reported in the following:

$$I_{T_3}^{avg}=I_{T_2}^{avg}=\frac{I\sqrt{2}M}{4\pi}\left[\frac{4}{M}+\theta\cos(\theta)-\sin(\theta)\right] \tag{163}$$

$$I_{T_3}^{rms}=I_{T_2}^{rms}=I\sqrt{\frac{1}{2}+\frac{M}{2\pi}\left[-1+\frac{4}{3}\cos(\theta)-\frac{1}{3}\cos(2\theta)\right]} \tag{164}$$

$$I_{T_4}^{avg}=I_{T_1}^{avg}=\frac{I\sqrt{2}M}{4\pi}\left[(\pi-\theta)\cos(\theta)+\sin(\theta)\right] \tag{165}$$

$$I_{T_4}^{rms}=I_{T_1}^{rms}=I\sqrt{\frac{M}{2\pi}\left[1+\frac{4}{3}\cos(\theta)+\frac{1}{3}\cos(2\theta)\right]} \tag{166}$$

$$I_{D_1}^{avg}=I_{D_2}^{avg}=I_{D_3}^{avg}=I_{D_4}^{avg}=\frac{I\sqrt{2}M}{4\pi}\left[\sin(\theta)-\theta\cos(\theta)\right] \tag{167}$$

$$I_{D_1}^{rms}=I_{D_2}^{rms}=I_{D_3}^{rms}=I_{D_4}^{rms}=I\sqrt{\frac{M}{2\pi}\left[1-\frac{4}{3}\cos(\theta)+\frac{1}{3}\cos(2\theta)\right]} \tag{168}$$

$$I_{D_{C2}}^{avg}=I_{D_{C1}}^{avg}=\frac{I\sqrt{2}M}{4\pi}\left[\frac{4}{M}-(\pi-2\theta)\cos(\theta)-2\sin(\theta)\right] \tag{169}$$

$$I_{D_{C2}}^{rms}=I_{D_{C1}}^{rms}=\sqrt{\frac{1}{2}-\frac{M}{\pi}\left(1+\frac{\cos(2\theta)}{3}\right)} \tag{170}$$

b. Power losses expressions

In this section, expression useful to calculate power losses are presented. Nevertheless the results are not reported due to the mathematical complexity.

Conduction Losses:

$$P_{T_1}^{cond} = P_{T_4}^{cond} = V_{t0} I_{T_1}^{avg} + r_T \left(I_{T_1}^{rms} \right)^2 \quad (171)$$

$$P_{T_2}^{cond} = P_{T_3}^{cond} = V_{t0} I_{T_2}^{avg} + r_T \left(I_{T_2}^{rms} \right)^2 \quad (172)$$

$$P_{D_1}^{cond} = P_{D_2}^{cond} = P_{D_3}^{cond} = P_{D_4}^{cond} = V_{D0} I_{D_1}^{avg} + r_D \left(I_{D_1}^{rms} \right)^2 \quad (173)$$

$$P_{D_{C1}}^{cond} = P_{D_{C2}}^{cond} = V_{D0} I_{DC1}^{avg} + r_D \left(I_{DC1}^{rms} \right)^2 \quad (174)$$

Switching Losses:

$$P_{T_1}^{sw} = P_{T_4}^{sw} = \frac{f_{sw}}{2\pi} \frac{V_{sw}}{V_{ref}} \int_{\theta}^{\pi} \left(a_{sw} i_s(t)^2 + b_{sw} i_s(t) + c_{sw} \right) d\omega t \quad (175)$$

$$P_{T_2}^{sw} = P_{T_3}^{sw} = \frac{f_{sw}}{2\pi} \frac{V_{sw}}{V_{ref}} \int_{\pi}^{\pi+\theta} \left(a_{sw} i_s(t)^2 + b_{sw} i_s(t) + c_{sw} \right) d\omega t \quad (176)$$

$$P_{D_1}^{sw} = P_{D_4}^{sw} = \frac{f_{sw}}{2\pi} \frac{V_{sw}}{V_{ref}} \int_{0}^{\theta} \left(a_{rec} i_s(t)^2 + b_{rec} i_s(t) + c_{rec} \right) d\omega t \quad (177)$$

$$P_{D_2}^{sw} = P_{D3}^{sw} = 0 \quad (178)$$

$$P_{D_{C1}}^{sw} = P_{D_{C2}}^{sw} = \frac{f_{sw}}{2\pi} \frac{V_{sw}}{V_{ref}} \int_{\theta}^{\pi} \left(a_{rec} i_s(t)^2 + b_{rec} i_s(t) + c_{rec} \right) d\omega t \quad (179)$$

c. Thermal Limits

An iterative numerical algorithm is used to calculate the junctions temperature varying negative current magnitude and phase. Expressions presented in the previous sections are used.

As result, the maximum negative sequence is I_{-MAX}=485A for a phase of 80°C. For this converter, the component in the worst thermal condition are the clamping diodes. Figure 213 shows junction temperatures variations respect to the ambient temperature (100°C). For each value of negative sequence current magnitude, temperatures are calculated for phases in [0, 2π] and the maximum values are plotted.

Finally, figure 214 shows power losses for the three legs at 485A for different phases of the negative component.

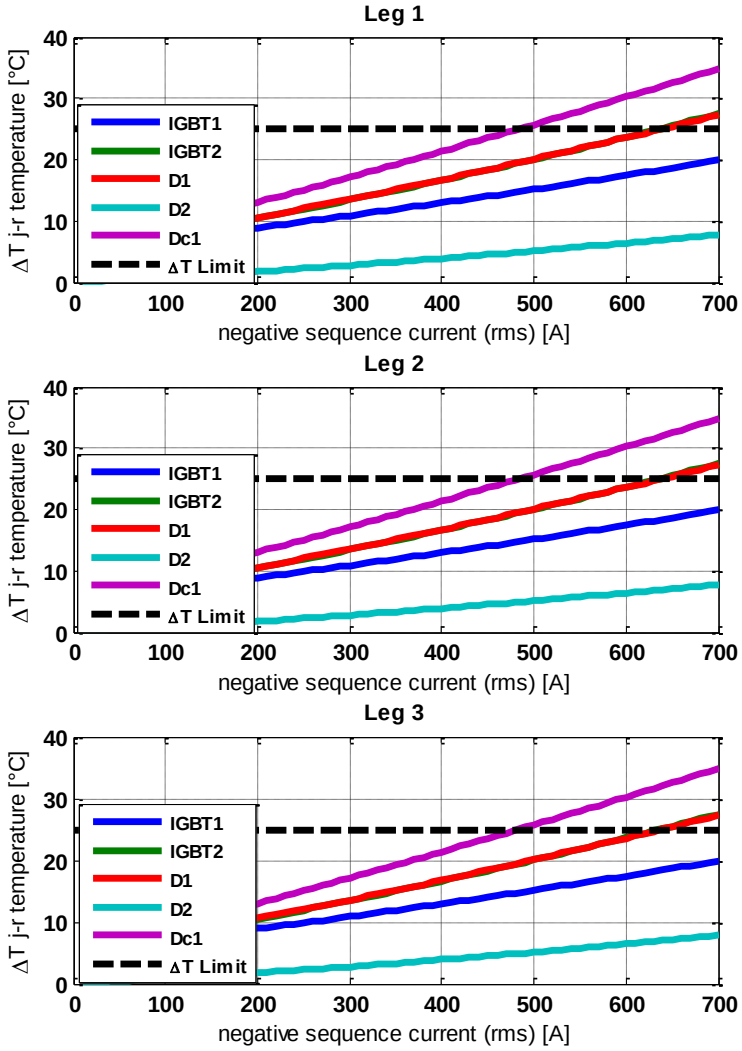


Fig. 213 - Junctions temperature variation vs negative sequence current magnitude

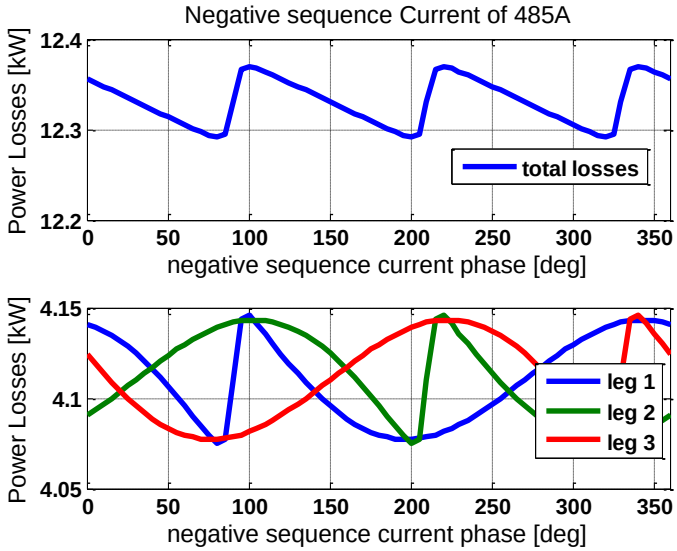


Fig. 214 - Power losses vs negative sequence current phase for 485A

Appendix II DC-Link Capacitor selection in voltage unbalance compensator based on VSI

This appendix presents the approach followed to calculate the DC-link capacitor for unbalance compensator based on Voltage Source Inverter converters. The aim is to determine the value of the capacitor that guarantees specifications for voltage ripple at the dc side.

The study is shown for the two-level and three-level NPC inverters.

For the two-level inverter, the functioning mode permits to face out the study with closed-form expressions. On the other hand, in the case of the three-level NPC topology, a numerical approach is used due to the complexity of expressions.

AII.I Two-Level Inverter

The scheme of a two level VSI converter connected to a supply system ob balanced three phase voltages through 3 link inductors L.

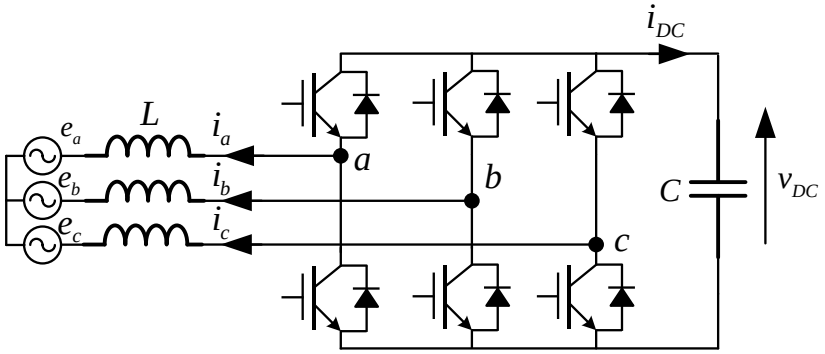


Fig. 215 – 2L VSI converter

As the converter in considered for unbalance compensation, the output currents i_a, i_b and i_c represents a purely negative symmetrical sequence:

$$\begin{aligned} i_a(t) &= I_- \sin(\omega t + \varphi_-) \\ i_b(t) &= I_- \sin\left(\omega t + \frac{2\pi}{3} + \varphi_-\right) \\ i_c(t) &= I_- \sin\left(\omega t - \frac{2\pi}{3} + \varphi_-\right) \end{aligned} \tag{180}$$

Where I_- and φ_- are respectively the magnitude and the phase of the negative current component generated.

From the power balance between the AC and DC side:

$$i_{DC}(t)v_{DC}(t) = i_A(t)e_A(t) + i_B(t)e_B(t) + i_C(t)e_C(t) \tag{181}$$

On the hypothesis that voltages are a positive sequence of magnitude E, power at the DC side is:

$$i_{DC}(t)v_{DC}(t) = -\frac{3}{2}EI_- \cos(2\omega t + \varphi_-) = -P\cos(2\omega t + \varphi_-) \tag{182}$$

Where P is the power transferred to the supply system.

On a first stage, let us neglecting the voltage ripple and considering constant the voltage on the capacitor v_{DC}=V_{DC}. The current in the DC link capacitor is:

$$i_{DC}(t) = -\frac{P}{V_{DC}}\cos(2\omega t + \varphi_-) \tag{183}$$

Thus, the voltage v_{DC} can be expressed as:

$$v_{DC}(t) = \frac{1}{C}\int i_{DC}(t)dt = -\frac{P}{V_{DC}C2\omega}\sin(2\omega t + \varphi_-) + v_{DC0} \tag{184}$$

The peak to peak voltage across the capacitor is:

$$v_{DC_{PP}}(t) = \frac{P}{V_{DC}C\omega} = \tag{185}$$

If a maximum voltage ripple of x% is requested on the DC bus, thus the needed capacitor is:

$$C_{x\%} = \frac{P}{x\%V_{DC}{}^2\omega} \tag{186}$$

For example, for the case study (5.7MVA on 13 modules) reported in this manuscript, a maximum voltage ripple of 5% is fixed:

$$C_{5\%} = \frac{5.7MVA/13}{0.05\cdot 1800^2\cdot 2\pi 50} = 8.6mF \tag{187}$$

AII.II Three-Level NPC Inverter

Let us consider the scheme of the converter in figure 216. The first task is to evaluate the DC link current harmonic content. Thus, harmonic components of i_{DC1} and i_{DC2} are evaluated. Due to symmetry, consideration carried out for i_{DC1} are valid as well for $i_{DC2.}$

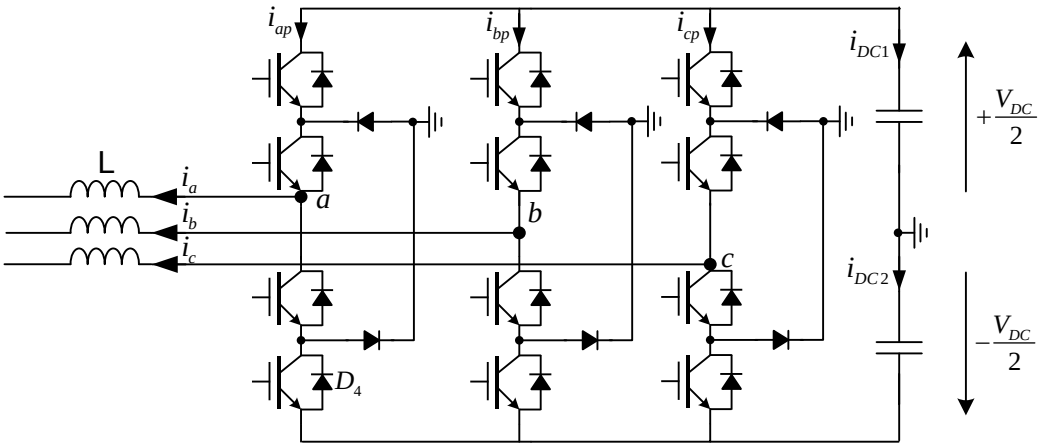


Fig. 216 - 3 level NPC converter

The modulation functions for the three legs (a,b,c) can be expressed as:

$$m_x(t) = M_x \sin(\omega t - \varphi_x) \quad \text{with } x=a,b,c \tag{188}$$

Currents in the legs, i_{ap}, i_{bp} and i_{cp}, are different from zero only when the corresponding modulation index is positive.

On this base, the generic leg current $i_{xp}(t)$ can be expressed as:

$$i_{xp}(t) = i_x(t) \cdot \beta_{px}(t) \tag{189}$$

Where

$$\beta_{px}(t) = m_x(t) sign(m_x(t)) \tag{190}$$

The output current is:

$$i_x(t) = I_x \sin(\omega t - \phi_x) \tag{191}$$

Figure 217, 218 and 219 reports typical waveforms for the legs current.

Finally, current i_{DC1} can be calculated as:

$$i_{DC1}(t) = \sum_{x=a,b,c} i_{xp}(t) = \sum_{x=a,b,c} i_x(t) \cdot \beta_{px}(t) \tag{192}$$

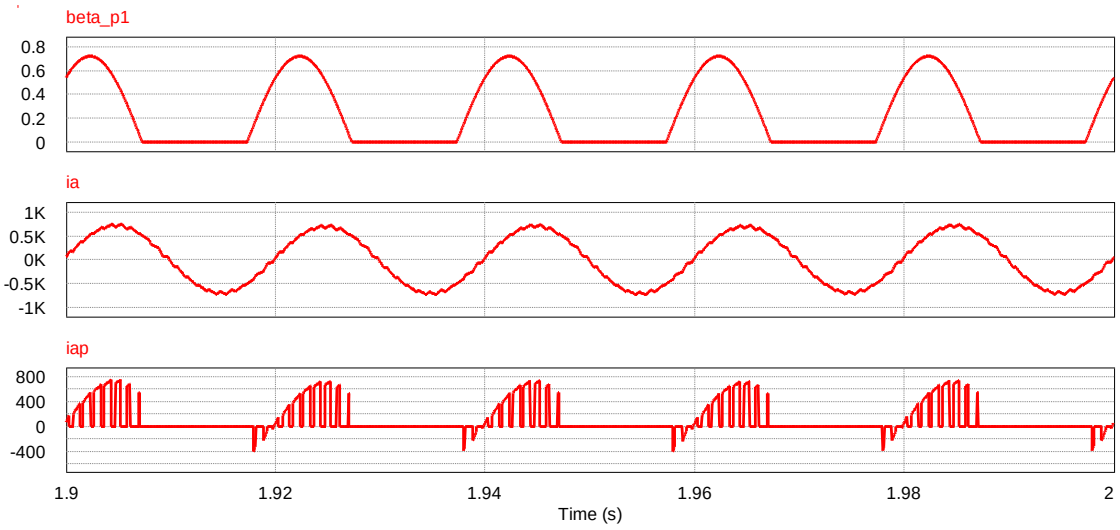


Fig. 217 - Current for leg a

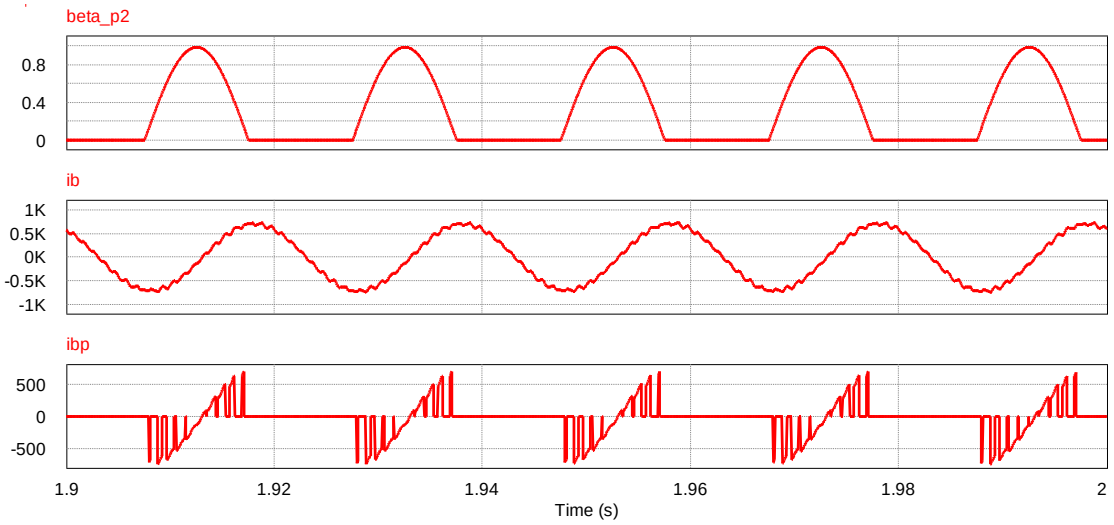


Fig. 218 - Current for leg b

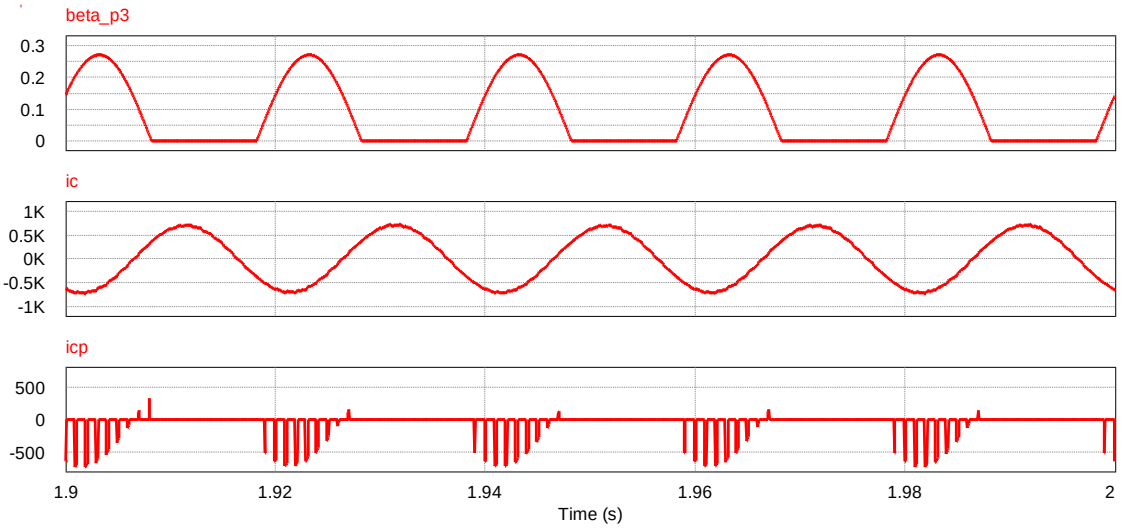


Fig. 219 - Current for leg c

a) Term $\beta_{px}(t)$ evaluation

The term $\beta_{px}(t) = m_x(t) sign(m_x(t))$ is decomposed in Fourier Series:

$$\beta_{px}(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} \left(a_n \cos(n\omega t) + b_n \sin(n\omega t) \right) \tag{193}$$

Values for n up to n=4 are considered. The Fourier coefficients are reported in the following table:

$a_0 = 2\frac{M_x}{\pi}$	$a_1 = -\frac{M_x}{2}\sin(\varphi_x)$	$a_2 = -\frac{2}{3\pi} M_x \cos(2\varphi_x)$	$a_3 = 0$	$a_4 = -\frac{2}{15\pi} M_x \cos(4\varphi_x)$
	$b_1 = \frac{M_x}{2}\cos(\varphi_x)$	$b_2 = -\frac{2}{3\pi} M_x \sin(2\varphi_x)$	$b_3 = 0$	$b_4 = -\frac{2}{15\pi} M_x \sin(4\varphi_x)$

After simple mathematical manipulation, $\beta_{px}(t)$ is expressed as:

$$\beta_{px}(t) = \frac{M_x}{\pi} + \frac{M_x}{2}\sin(\omega t - \varphi_x) - \frac{2}{3\pi} M_x \cos(2\omega t - 2\varphi_x) - \frac{2}{15\pi} M_x \cos(4\omega t - 4\varphi_x) \tag{194}$$

b) Term $i_{xp}(t)$ evaluation

The term $i_{xp}(t)$ can be calculated as:

$$i_{xp}(t) = i_x(t) \cdot \beta_{px}(t) =$$
$$= I_x \sin\left(\omega t - \phi_x\right) \cdot \left[\frac{M_x}{\pi} + \frac{M_x}{2}\sin(\omega t - \varphi_x) - \frac{2}{3\pi} M_x \cos(2\omega t - 2\varphi_x) - \frac{2}{15\pi} M_x \cos(4\omega t - 4\varphi_x) \right] \tag{195}$$

After simplifications, the following harmonic terms are obtained:

rank	**name**	**expression**
DC	i_{xp_DC}	$\frac{M_x}{4} I_x \cos\left(\phi_x - \varphi_x\right)$
h=1	i_{xp_1}	$I_x \frac{M_x}{\pi}\sin(\omega t - \phi_x) + \frac{1}{3\pi} M_x I_x \sin\left(\omega t + \phi_x - 2\varphi_x\right)$
h=2	i_{xp_2}	$-\frac{M_x}{4} I_m \cos\left(2\omega t - \phi_x - \varphi_x\right)$
h=3	i_{xp_3}	$-\frac{1}{3\pi} M I_x \sin(3\omega t - \phi_x - 2\varphi_x) + \frac{I_x}{15\pi} M_x \sin(3\omega t + \phi_x - 4\varphi_x)$
h=4	i_{xp_4}	0
h=5	i_{xp_5}	$-\frac{I_x}{15\pi} M \sin(5\omega t - \phi_x - 4\varphi_x)$

Table XXIII

c) $i_{DC1}(t)$ expression evaluation capacitor design

The term $i_{DC1}(t)$ is evaluated in two cases. The first case, refers to positive sequence currents [$i_a(t)$, $i_b(t)$,$i_c(t)$]. On the other hand, the second case refers to a case of purely negative sequence for currents.

Case positive sequence

Considering a positive sequence currents $i_a(t)$, $i_b(t)$ and $i_c(t)$, with phase ϕ:

$$I_x = I_+ \qquad \phi_a = \phi \quad \phi_b = \phi + \frac{2\pi}{3} \quad \phi_a = \phi - \frac{2\pi}{3}$$

The modulation functions form a symmetrical positive sequence:

$$M_x = M_+ \qquad \varphi_a = \varphi \quad \varphi_b = \varphi + \frac{2\pi}{3} \quad \varphi_a = \varphi - \frac{2\pi}{3}$$

On this base, the current in the DC-Link capacitor is calculated according to the terms in Table XXIII:

$$i_{DC1}(t) = \frac{3M}{4} I_+ \cos(\phi - \varphi) + \frac{M}{5\pi} I_+ \sin(3\omega t + \phi - 4\varphi) - \frac{M}{\pi} I_+ \sin(3\omega t - \phi - 2\varphi) \tag{196}$$

Thus, in case of positive symmetrical currents, a third harmonic is present in the current capacitor. The capacitor has to be chosen in order to guarantee the maximum allowed ripple of vdc according to the following expression:

$$\begin{aligned} v_{DC} &= \frac{1}{C}\int\left[\frac{M}{5\pi} I_+ \sin(3\omega t + \phi - 4\varphi) - \frac{M}{\pi} I_+ \sin(3\omega t - \phi - 2\varphi)\right]dt = \\ &= \frac{1}{C}\left[-\frac{M}{5\pi 3\omega} I_+ \cos(3\omega t + \phi - 4\varphi) + \frac{M}{\pi 3\omega} I_+ \cos(3\omega t - \phi - 2\varphi)\right] \end{aligned} \tag{197}$$

Case negative sequence

In this condition, the three output currents form a purely negative sequence, and the modulation function are unbalanced.

$$I_x = I_- \qquad \phi_a = \phi \quad \phi_b = \phi - \frac{2\pi}{3} \quad \phi_a = \phi + \frac{2\pi}{3}$$

M_a, M_b, M_c and $\varphi_a, \varphi_b, \varphi_c$ are calculated according to expressions (29).

In this case, the current in the DC-Link capacitor is composed of all the harmonic terms reported in Table XXIII. Thus, in case of negative symmetrical currents, the ripple in the DC capacitor is due to several harmonics terms. A numerical approach is needed in order to determine the value of C.

d) Capacitor selection criteria in voltage unbalance compensator based on NPC 3-L VSI

The parameters of the voltage unbalance compensator based on NPC 3-L are listed in the following table:

Transformer Ratio	86
Primary phase-to-ground Voltage	90e3/sqrt(3)V
Secondary phase-to-ground Voltage	606V
DC Voltage (Vdc1+Vdc2)	3600V
Maximum current for each STATCOM at thermal limits	485A
Inductor L	4.4mH
Compensator Size	5.7MVA
Transformer Secondary Current	3144A
Number of STATCOM modules in parallel	7
Current in each STATCOM	449A

The following values for modulation index are calculated for the single VSI module:

$$I_x = I_{_} = 449\sqrt{2}A \qquad M_a = 0.68 \quad M_b = 0.93 \quad M_c = 0.25$$
$$\varphi_a = 45.5° \quad \varphi_b = -135° \quad \varphi_c = 43°$$

Simulation in PSIM are carried out for the single module. In figure 220, the output currents for the single module are reported. Figure 221 shows the modulation functions.

Figure 222 shows the current spectrums of DC link currents i_{DC1} and i_{DC2}.

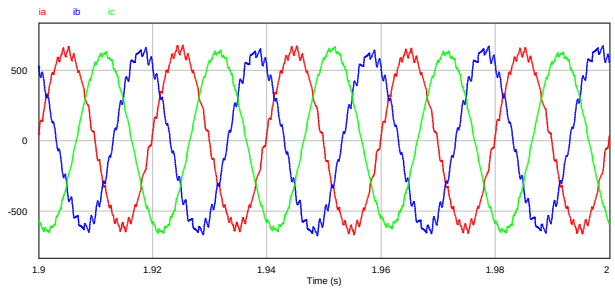


Fig. 220 – 3L-NPC Output Currents

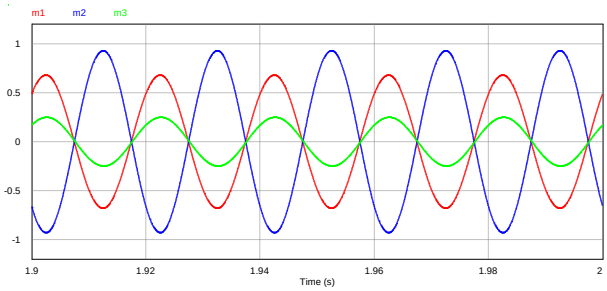


Fig. 221 - Modulation functions

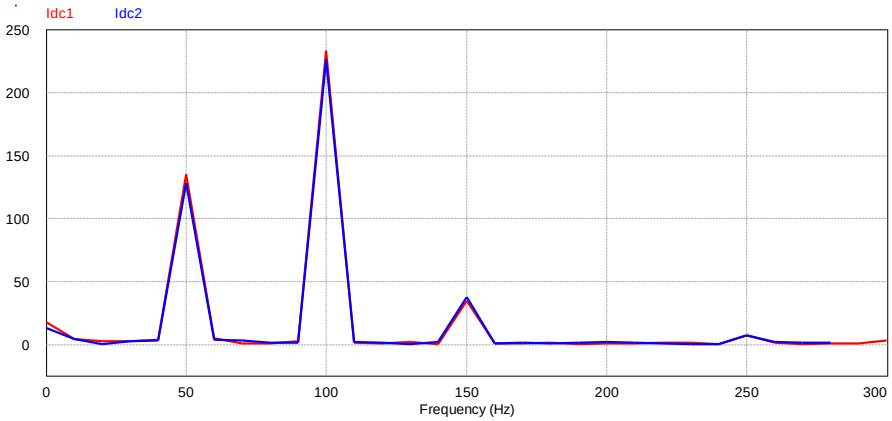


Fig. 222 - DC current FFT - PSIM simulation

The results of the simulation are used to validate the expressions introduced previously, According to expression in Table XXIII, each harmonic terms in the DC link currents is evaluated analytically as following:

$$i_{DC1}\big|_h = i_{ap_h} + i_{bp_h} + i_{cp_h} \rightarrow \overline{I_{DC_h}} = I_{DC_h} e^{j\varphi_{DC_h}} \tag{198}$$

Where h is the harmonic rank.

Calculated harmonics amplitudes are reported in figure 223. Let's remark that analytical results match quite well simulation results.

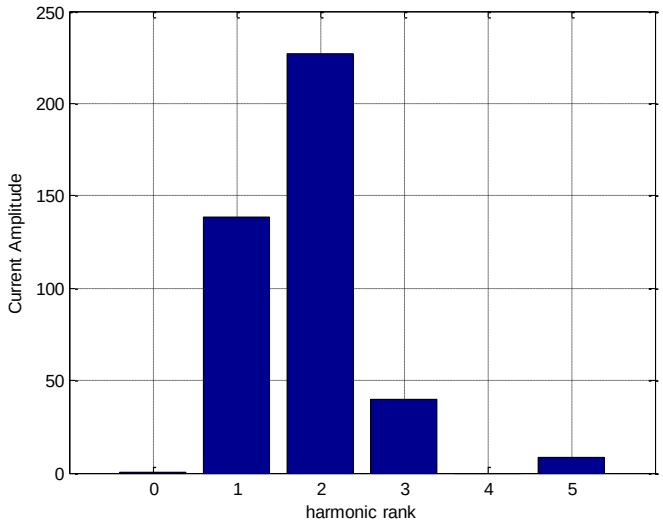


Fig. 223 - analytical evaluation of DC current

As the expressions for the harmonic component in the DC-Link are validated, it is possible to determine with a numerical algorithm, the capacitor C that assures the maximum allowed voltage ripple.

The following equations describe the voltage across the DC-Link capacitor:

$$v_{DC1} = \frac{1}{C}\int \sum I_{DC_h} \sin(h\omega t + \varphi_{DC_h})dt = -\frac{1}{C}\sum \frac{I_{DC_h}}{h\omega}\cos(h\omega t + \varphi_{DC_h}) \tag{199}$$

The executed algorithm is described following:

1) Calculation of harmonic components $\overline{I_{DC_h}} = I_{DC_h} e^{j\varphi_{DC_h}}$
2) Calculation of terms $\sum \frac{I_{DC_h}}{h\omega} \cos(h\omega t + \varphi_{DC_h})$ in t=0:1s, for h=1,2,3,4,5
3) Calculation of $v_{pp} = \max\left(\sum \frac{I_{DC_h}}{h\omega} \cos(h\omega t + \varphi_{DC_h})\right) - \min\left(\sum \frac{I_{DC_h}}{h\omega} \cos(h\omega t + \varphi_{DC_h})\right)$
4) For several values of C, the ripple in percentage of the DC voltage is evaluated:

$$v_{pp}\% = \frac{1}{C\,1800V} \frac{v_{pp}}{} \cdot 100$$

5) $v_{pp}\%$ versus capacitors values is plotted in figure 224.

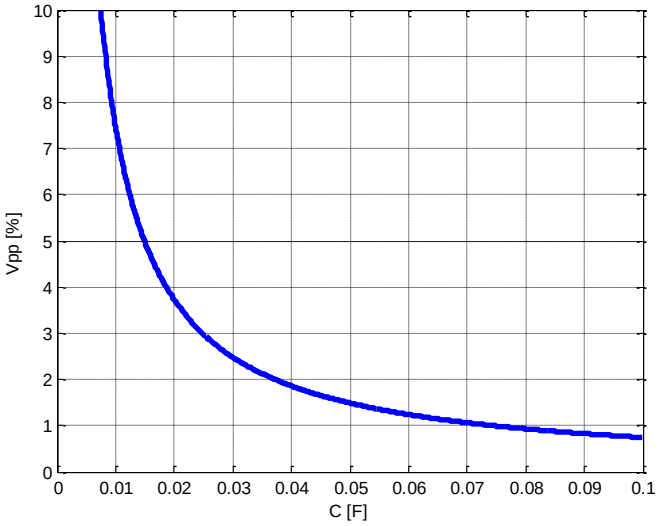


Fig. 224 - v_{DC1} voltage ripple in function of capacitor C

In the figure a dashed line indicates the maximum voltage ripple of 5%. On this base, a capacitor of C≥15mF is needed.

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