Wireless Approach for SIP and SOC Testing

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This work has been carried out within the framework of the IsyTest (Institute for System Testing), joint institute between NXP Semiconductors and LIRMM laboratory. This work has been started at PHILIPS semicoductors (Caen), which became NXP Semiconductors. It has been conducted under the supervision of M. Philippe Cauvet (NXP), and of three researchers at LIRMM: Mme Marie-Lise Flottes, M. David Andreu, and M. Serge Bernard.

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Introduction

The great technology advance in the microelectronic industry has permitted to jointly integrate digital, analog, RF and even MEMS components. Therefore, complex systems can now be designed and integrated as chips. Such design concept reduces the global size of the system and increases its performance as well. These two major features explain the great success of System-on-Chip (SOC), and the growing up of the System-in-Package (SIP) market, despite the increasing complexity in design and test tasks.

Testing is required to guarantee fault-free products because of unavoidable manufacturing imperfections. In fact, the test activity plays a key role in the production process of integrated circuits by its ability to differentiate good devices from faulty ones before delivery to end-users, as well as to improve the manufacturing yield, by giving quasi real-time feedback. Basically, testing consists of two processes: the test generation and the test application. The test generation designates the process of providing appropriate test stimuli, whereas the test application refers to the process of applying these test stimuli to the circuit inputs and analyzing its responses. Traditionally, the first test application is performed at wafer level using contact-based probing technologies.

However, as the integration density of the SIP/SOC continues to increase, test generation and test application becomes more and more complex tasks. Particularly, the current test application solutions based on probing technologies suffer from many drawbacks such as limited parallelism and test cost, among others. Moreover, SIP testing leads to new challenges. Conversely to SOC, where cores and interconnects are tested after manufacturing of the whole system, SIP may require intermediate testing. Indeed, early binning during manufacturing prevents the assembly of good dies on faulty systems. However iterative testing requires multiple touchdowns on the test pads and induces scrubbing. For that, new probing technologies have been developed to push the mechanical limits forward. However, even with the advancing probing solutions, the contact-based probing techniques will not be able to catch up with the SIP/SOC test evolution.

In this context, we propose an original test method based on wireless transmission. It consists in adding a unique Wireless Test Control Block (WTCB) in every Device under Test (DUT) to provide wireless communications between the tester and the DUTs on a wafer and to apply the test. This original wireless solution is not based on any previous work, and is brand new with respect to the “related” methods based on wireless/non-contact transmission.

In this document, Chapter 1 describes the trends in the design and test of SIP and SOC systems, and gives an overview of the main testing issues encountered at every manufacturing step. A state-of-the-art of “related” work is also given in this chapter.

Taking advantage of the wireless transmission, test data can be broadcasted, in packets, from the tester to all DUTs on the wafer providing full test parallelism. The WTCB, integrated in the DUT, is in charge of extracting test signals from received packets, controlling the test at DUT level and sending back the DUT test responses to the tester. The WTCB communicates with the internal circuits of the DUT through

JTAG interface. Its architecture includes a wireless communication module to handle the wireless transmission, and a Test Control Block (TCB) to handle the test application. Chapter 2 is dedicated to the definition of this new wireless test approach, and the proposed WTCB architecture. The structure of the exchanged packets is also given in this chapter.

Chapter 3 reports validation experiments. For that, we elaborated a dedicated wireless test platform, based on the use of FPGA cards. This experimental platform emulates a tester and a WTCB embedded in a DUT. Several experiments have been conducted with this platform, among them a wireless test of a real circuit (ASIC) was successfully performed. In this chapter, the conducted experiments are described and their results are discussed.

Finally, the proposed method is extended in Chapter 4 to a larger application field, namely in-situ testing. The main issue is the remote access to the targeted. In most cases, such as medical implants, or automotive applications for instance, it is practically impossible to have a direct access to the targeted device. A possible solution for such cases consists in embedding an appropriate test interface in the system. In Chapter4, we describe how the proposed WTCB, initially developed for wafer testing, can be also adapted to such context.

Chapter 1

Context and state-of-the-art

I SIP and SOC testing

I.1 Introduction

Electronic systems are going to higher complexity, integrating ever more complex and numerous functions under ever more pressure for cost reduction. With advances in semiconductor manufacturing technology, the *system on chip* (SOC) technology represents a viable solution to reduce device cost through higher levels of integration, while keeping the hardware design effort in reasonable limits, in particular thanks to the so-called reuse strategy. In parallel, the push towards more functionality in a single small "box" requires the integration of heterogeneous devices that cannot be intrinsically achieved in single-technology SOC. In this context, *system in package* (SIP) clearly appears as the best alternative to integrate more functions in an equal or smaller volume.

A good illustration of this global trend is given by cellular handset. Today, a cellular design must support multi-band and multi-mode in addition to Bluetooth networking, *global positioning system* (GPS), *wireless local area network* (WLAN), without mentioning user applications such as games, audio, and video. This miniaturized application pushes the need for both SOC and SIP solutions to solve the problems related to the integration of highly complex design in an economical way.

I.1.A SOC and SIP differences

The SOC refers to integrating the different components of a system into a single IC. These components can be logic, memory or analog cores. Being a single die, an SOC is consequently fabricated using a single process technology. In addition, it has a single level of interconnections from the die to the package pads or to the interposer. The interconnection technologies used are wire bonding or flip chipping. Figure 1-1 presents an example of a SOC.

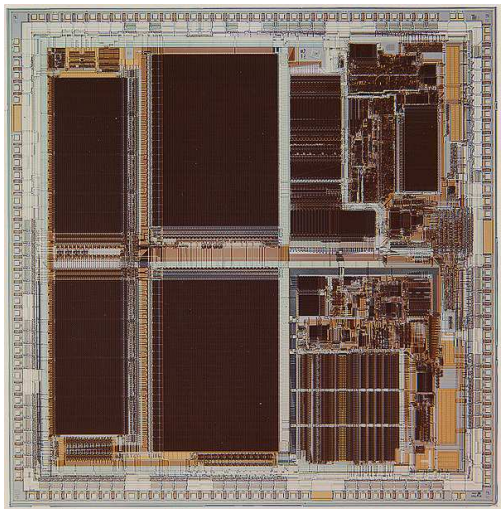


Figure 1-1: SOC example

An attractive alternative for system integration is the SIP technology. The SIP concept started with the development of *multi-chip module* (MCM) in the 1990s. At that time, a typical MCM contained memories and a processor. Since then, the capacity of integrating several dies into a single package has continued to increase over time. Nowadays, a SIP may include analog and RF dies in addition to logic and memory ones, and even *micro-electromechanical system* (MEMS) components. These various dies/components can be

fabricated with different process technologies, such as CMOS, BiCMOS, or GaAs. In addition, they are interconnected with multiple levels of interconnections: from die/component to die/component, or from die/component to the package pads or to the interposer. Several interconnection technologies can be used for this purpose, such as wire-bond, flip-chip, stacked-die technology, or any combination of the above.

An appropriate definition of a SIP is given in the International Technology Roadmap for Semiconductors published by Semiconductor Industry Association, where a SIP is defined as *any combination of semiconductors, passives, and interconnects integrated into a single package* [SIA 2005]. This definition covers all the SIP technologies, which differ in their type of carrier or interposer intended for holding the bare dies (or components) and the type of interconnections between components. The carrier or interposer can be a leadframe, an organic laminate, or silicon-based. Another possibility is to stack components on top of each other [Cauvet 2007]. Figure 1-2 shows an example of a silicon-based SIP fabricated by "NXP Semiconductors", and characterized by:

- A passive die serving as platform for the active ones,
- High level integration of passive components in the passive die.

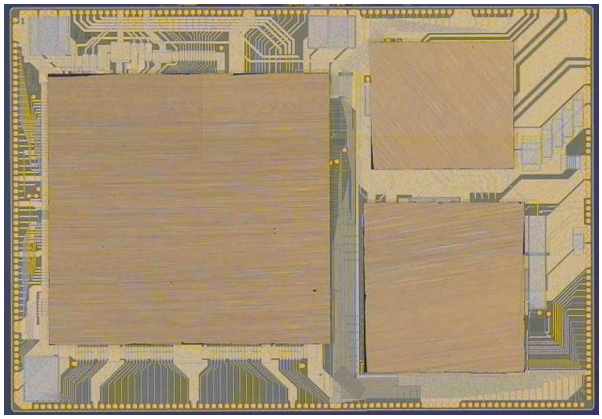


Figure 1-2: SIP example

I.1.B SOC versus SIP

The continuous advance in CMOS technology has led recently to a successful migration of RF and analog circuits from BiCMOS technology to a full CMOS solution. This important transition in the IC fabrication has permitted to a system with logic, mixed and analog functions to be designed as a single IC, namely as a SOC. As consequence, an interesting debate is launched: which is the better technology for a given system, to be designed as a SIP or as a SOC? Clearly, the better technology is dictated by the specifications and the constraints of the intended system. In the following we give a brief description of the main characteristics of both technologies, which are carefully considered by the system designers when they choose the SIP or SOC technology for their design.

With the SIP technology, the system can be designed in shorter time than a SOC. Each die can be separately designed in his most suited technology. Moreover, the SIP technology enables the plug-and-play approach. For example, considering an RF application system made of RF analogue mixed signal and digital dies, different RF designs can be done for different applications, without changing the baseband chip [Wilson 2005]. However, a system fabricated as a SIP is often more expensive than a SOC. fact, a SIP contains multiple pre-tested dies and passive components. They are

assembled together by a complex assembly process, where many different interconnect techniques may be used for wire bonding and flip-chip connections. In addition, the SIP technology uses some complex assembly processes that could reduce the system reliability, which is not the case of a SOC.

As result, the SIP technology seems to be more suitable for systems that have short production cycles, or for systems with short time-to-market. For example, in mobile phone applications, the system integrators came to the conclusion that integrating existing and available *integrated circuits* (ICs) into an SIP is often much easier and faster than creating new SOC designs [L-T. Wang 2008]. On the other hand, the SOC seems to be more suitable for high production volume, or for applications intended for a long run.

Anyway, both SIP and SOC manufacturers have to master the technology. This is one of the essential points to provide a reliable product, with the desired performances. However, this is not sufficient to provide a high quality product. In fact, due to the unavoidable flaws in the materials and masks used in the IC or SOC fabrication, a physical imperfection may be generated, leading to a defect in the fabricated IC or SOC. Similarly, during SIP fabrication several defects may be generated by the assembly process. Thus, any fabricated IC, SOC or SIP is considered to be defect prone. In consequence, all fabricated circuits and systems must be tested in order to filter the good from the defected ones. The following subsection presents an overview of the test principle and basics, focusing on digital IC testing.

I.2 Test principle and basics

In the microelectronic industry, a manufacturer is always interested to deliver a high quality product to its clients. For that, the fabricated circuits must be sufficiently tested before delivery. That is a must to maintain a good reputation, and to minimize the customer compliant as well. The good circuits are delivered, while the faulty ones can possibly undergo a *failure mode analysis* (FMA), which is typically used to improve the production yield, by giving a feedback to the product engineers in charge of the processes and products monitoring and improvement. The yield of a manufacturing process is defined as the percentage of acceptable parts among all manufactured parts:

$$\text{yield} = \frac{\text{Number of acceptable parts}}{\text{Total number of parts fabricated}}$$

In the following, we give an overview of digital IC testing, where we describe the processes of test data generation and the equipments for test application. Next, we present the main features that are added to the IC design in order to improve its testability, before ending this subsection by detailing the JTAG boundary scan technique.

I.2.A ICs Test principle

Testing typically consists of transmitting test stimuli to the inputs of the *device under test* (DUT), while analyzing the output responses, as illustrated in Figure 1-3. The DUT term designates an IC, a SOC or a SIP undergoing a test. DUTs that produce the correct output responses for all input stimuli pass the test and are considered to be fault-free. Devices that fail to produce a correct response at any point during the test sequence are assumed to be faulty.

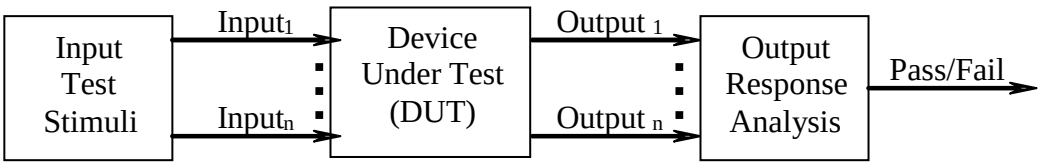


Figure 1-3: Basic test principle [L-T. Wang 2006]

In digital IC testing, the test stimuli consist of a set of input patterns applied to the DUT. Each input pattern is a combination of logic 1's and 0's, called a *test vector*. Thus, in order to test a circuit with *n* inputs and *m* outputs, a set of test vectors is applied to the DUT, and its responses are compared to the known good responses of a fault-free circuit. Two processes are required for this purpose: the *test generation* and the *test application*. The test generation is the process of producing test vectors for efficient testing, whereas the test application is the process of applying those test vectors to the DUT and analyzing the output responses.

I.2.A.a. Test generation

Three approaches can be used in test generation: exhaustive, structural and (peudo)-random approaches. The exhaustive approach consists in applying all possible input combinations to the inputs (2^n input patterns for an n-input logic circuit). This approach detects 100% of static defects that may exist in a combinational circuit; and the generation process is very simple. However, this strategy is not efficient for sequential circuits that require an ordered set of test vectors for every defect, which are necessary to reach required internal states. Thus, the 2^n input patterns are not sufficient for sequential circuit testing. In addition, the test application process is too time-consuming in case of large value of n.

A more practical method, called structural testing is usually used for test generation. Based on circuit structural information, this approach uses a set of fault models to generate specific test patterns dedicated to the detection of these faults.

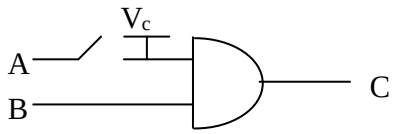
A fault model is an engineering model describing the possible physical defects that can occur in the fabricated device at a higher level of abstraction. By using fault models, the test vectors can be automatically generated by dedicated softwares. Common types of fault models are:

1. single and multiple stuck-at faults affecting the state of signals on the logic circuit lines,
2. delay faults that cause excessive delay along a path,
3. Transistor faults (stuck-open, stuck-short) that results in memory or non-logic behavior on gate outputs, open and short affecting the circuit wires.

A description of a single stuck-at fault is detailed as an example (see Figure 1-4). In this model, only one line in the circuit is faulty at a time. The fault is permanent, and its effect is as if the faulty node is tied to either V_{cc} (stuck-at-1 or s-a-1), or Gnd (stuck-at-0 or s-a-0). This model supposes that the function of the gates in the circuit is unaffected by the fault, this leads to a reasonable number of faults equal to 2*k, where k is the number of signal lines in the gate-level netlist of the circuit.

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

(a)



(b)

A	B	C
0	0	0
0	1	**1**
1	0	0
1	1	1

(c)

Figure 1-4: (a) True table of the fault-free AND gate, (b) fault model: s-a-1 on input A, (c) True table of the faulty AND gate

Using a fault model, the test generation begins by generating the faulty list, which contains all the potential faults. Then, a fault is selected for test generation, where an *automatic test pattern generator* (ATPG) is used to generate a test vector for this selected fault. Once generated, a *fault simulation* is performed to determine all faults that are detected by this test vector. Those detected faults are marked off of the list (fault-dropping). Then, another fault is selected from the remaining undetected faults in the faulty list, and the previous test generation steps are performed for this fault. This process is repeated until all the faults in the list are marked off, or the ATPG is unable to provide a test vector for the remaining faults. This is illustrated in Figure 1-5.

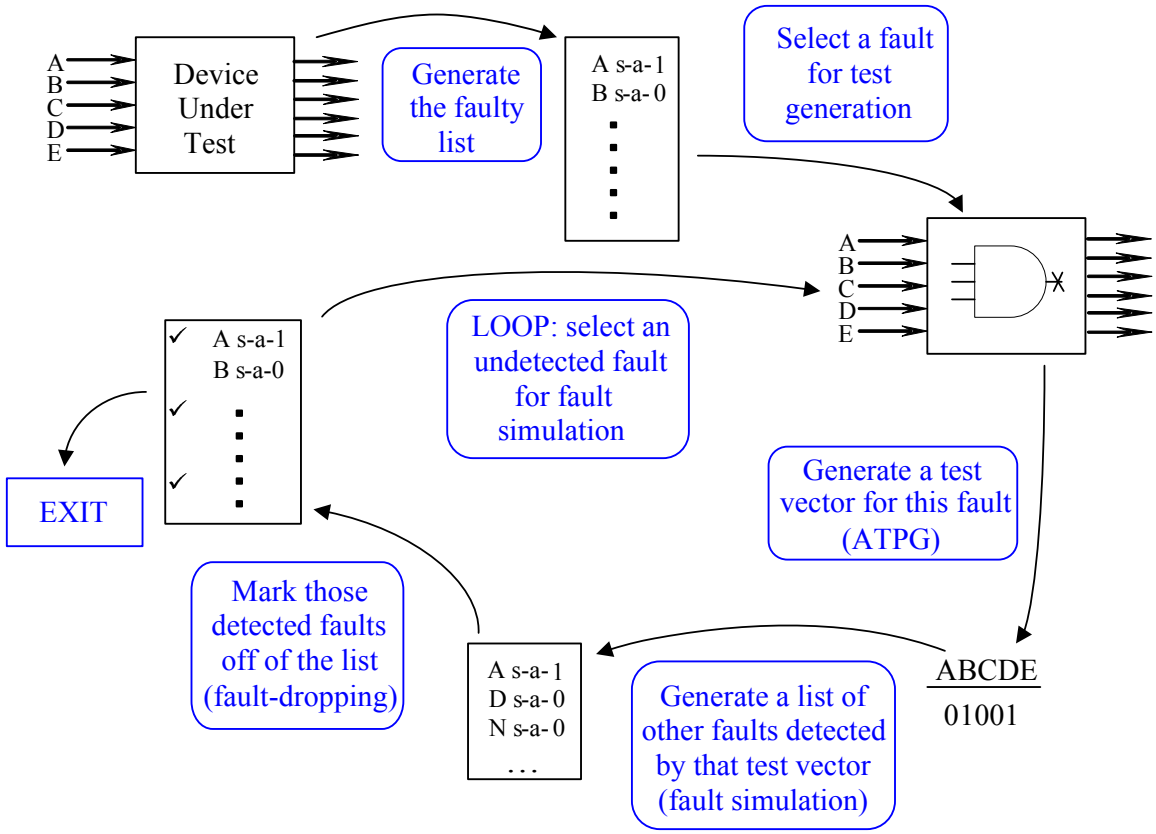


Figure 1-5: test generation process

Structural testing provides high quality test sequences, particularly for combinational circuits, but may require large CPU time. The process can be shortened using the (pseudo)-random approach as preliminary step. Random test vectors are first generated in order to remove the “easy to detect” faults from the faulty list. Easy-to-detect faults are those that can be detected by a large number of test vectors. In consequence, a vector generated randomly is likely to detect some of these easy-to-detect faults. A new pseudo-random test vector is generated until several successive generations fail to provide a test

vector detecting new fault in the list. At this point, the process switches to the deterministic and structural approach in order to generate test vectors for the remaining "hard-to-detect" faults.

Not that test vectors are generated for detection of faults and not defects. In other words, a test sequence including all the necessary vectors for detection of faults in a model, stuck-at faults for instance, cannot guarantee the detection of all possible manufacturing defects.

I.2.A.b. Test application

As already mentioned, the test application designates the process of applying test vectors to the DUT and analyzing output responses. This process is performed by *automatic test equipment* (ATE), which contains typically the following main components:

1) A powerful computer: it represents the interface between the user and the tester, stores the test program, including test data and responses, timing and level information.
2) A main frame and/or a test head: it include(s) all the electronics that are necessary to perform the test (level and timing generators, power supply, vector memory, all necessary pin electronic for driving and reading values on the tester channels). Under the control of the test program, the tester electronics translate test patterns into corresponding electrical waveforms with the desired shape and timing, compare (or measure) DUT output responses to expected values, and return pass/fail information to the computer.
3) DUT board and probe card: they are used as an interface between the electronics of the tester and the DUT IOs. Their goal is to provide electrical paths for power supply and test signals transfer between the tester electronics and the pads of an IC on a wafer or the pins of a packaged chip during testing. The contact elements of the probe card are called probe tips.

The ATE may contain other resources such as *digital signal processors* (DSP), used for analog testing. Regarding the various components of an ATE, this later can be very expensive. The pin electronics and the correspondent probe card are typically the most expensive part of the ATE.

To summarize, the digital IC testing consists in generating logic values of the test vectors (ATPG program), based on fault models. An ATE is used to apply those test vectors to the DUT and to analyze the output responses. Depending on the complexity of the DUT, the test generation process may take a long time to generate a set of test vectors detecting all faults; in some cases, some faults remain undetectable, which reduces the test quality.

In order to decrease test generation and test application times and to enhance test quality, testability-related design rules are used during the circuit design. This will be explained in the following subsection.

I.2.B Design for testability

Integration of design and test consists in considering testing early in the design flow. This task is referred as *design for testability* (DFT). Related techniques are usually

classified into three categories: Ad-hoc DFT techniques, Scan design, and *built-in self-test* (BIST).

I.2.B.a. Ad-hoc DFT techniques and Scan design

The goal of such techniques is to enhance the capabilities of controlling and observing the poorly testable nodes in a circuit. Doing so, the test generation is easier, the quality of test is improved, and the test, debug and diagnose tasks are simplified.

Ad-hoc methods target the difficult-to-test protions of the circuit and consist in adding dedicated circuitry (test points) for controllability and observability improvement. The test points allow to access circuit internal nodes directly.

Scan design is the most common DFT technique used for sequential circuits. All or a part of the storage elements (latches or flip-flops) in the IC design are made externally controllable and observable. An extra circuit signal called *scan enable* is added to the design. When asserted, the storage elements, called scan cells, are stitched together to form one or several shift register(s), called scan chain(s). Each scan chain is connected to one primary input and one primary output. Thus, an arbitrary pattern can be serially entered into the chain of flips flops, and the state of every flip flop can be read out. Therefore, the problem of sequential testing becomes one of combinational logic testing only, leading to an easier test generation process, and better test quality. An example of full scan design circuit is shown in Figure 1-6.

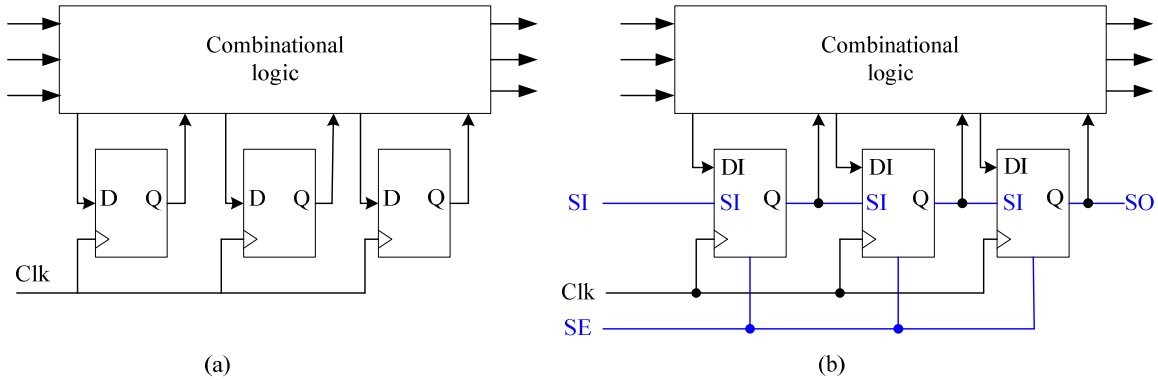


Figure 1-6: sequential circuit (a) designed as full scan circuit (b).

Another important technique based on test data serialization is the JTAG boundary scan test introduced for board testing. Since our work, presented in chapters 2 and 3 of this document, is heavily based on this technique, this later will be described in details in section I.2.C.

I.2.B.b. BIST techniques

The BIST is a design technique consisting in integrating in the DUT a *test pattern generator* (TPG) and an *output response analyzer* (ORA) in order to perform testing internal inside the IC. The TPG generates the test vectors applied to the DUT inputs, while the ORA automatically compacts the output responses of the DUT into a signature. The operations of the TPG, the DUT and the ORA are controlled by a logic BIST controller. This later provides all the necessary timing control signals to ensure a correct testing operation. Once the BIST operation is complete, the BIST controller provides a pass/fail indication after comparison of the final signature with a *golden signature*. Figure 1-7 shows an example of DUT with logic BIST structures.

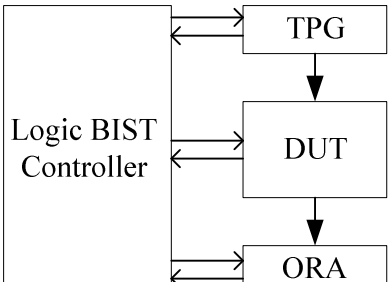


Figure 1-7: typical logic BIST structure

Clearly, the BIST technique generates an important area overhead, since it implies the integration of the TPG, ORA and logic controller in the DUT. However, BIST techniques offer many advantages that can favorite their use:

- In fact, the test time is reduced with BIST. In consequence, the test cost is reduced on its turn, which alleviates the cost of the area overhead.
- BIST techniques permit to avoid the use of high expensive ATE, as most of the tester functions reside on-chip itself.
- BIST techniques offer the possibility to perform a reliable test of internal circuit components, in case of limited external access via the primary inputs.
- BIST can be used from wafer to in-situ testing.

I.2.C JTAG boundary scan

The *joint test action group* (JTAG) TAG was an industry group formed in 1985, which has developed a specification for boundary-scan testing that was standardized in 1990 [IEEE 1149.1 Std]. In 1994, a supplement containing a description of the *boundary-scan description language* (BSDL) was added to the standard. Since that time, JTAG has been adopted by major electronics companies all over the world. Applications are found in high volume, high-end consumer products, telecommunication products, defense systems, computers, peripherals, and avionics.

The boundary-scan test architecture provides a means to test interconnects between integrated circuits on a board without using physical test probes. Its basic idea consists in adding scan registers to the inputs and outputs of ICs, as shown in Figure 1-8.

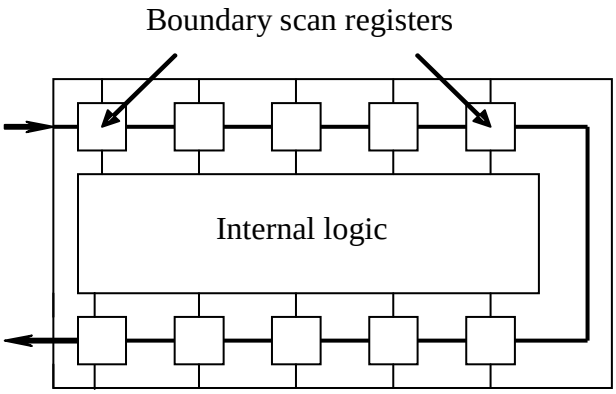


Figure 1-8: basic idea of boundary scan

The boundary scan cells of ICs on the same board are interconnected into a single boundary-scan chain (see Figure 1-9). Through this chain, the I/Os of each IC are

controllable and observable via serial scan and Capture/Update operations. Thus, a pattern can be applied to the circuit inputs, and the response can be read out via the boundary scan chain. This can be used to test the soldered ICs on a board, as well as the interconnections between them.

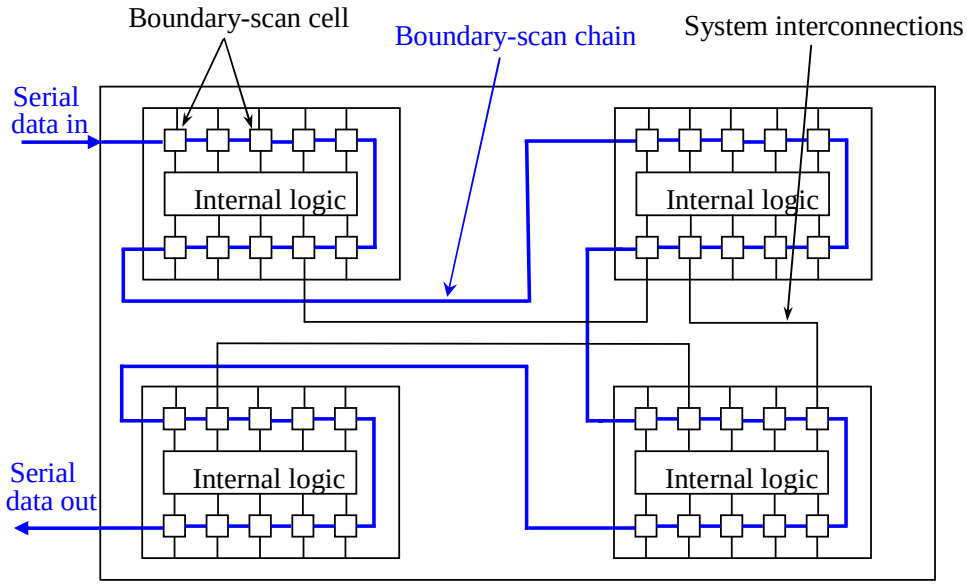


Figure 1-9: a board containing four ICs complying with boundary scan

I.2.C.a. Test architecture and procedure

In addition to the boundary-scan register, extra control circuitry is implemented. The boundary-scan circuitry can be divided into four main hardware components:

- A *Test Access Port* (TAP), which represents the circuit test interface.
- A *TAP controller* (TAPC), which is a 16-states finite-state machine that controls each step of the boundary-scan operations.
- An *instruction register* (IR), and its associated *decoder*.
- Several test data registers, including mandatory register like a *Bypass* register, and some optional registers like *device-ID* register.

Figure 1-10 shows the architecture of a boundary scan compliant circuit. Each of the four main components is detailed in the following sub-sections.

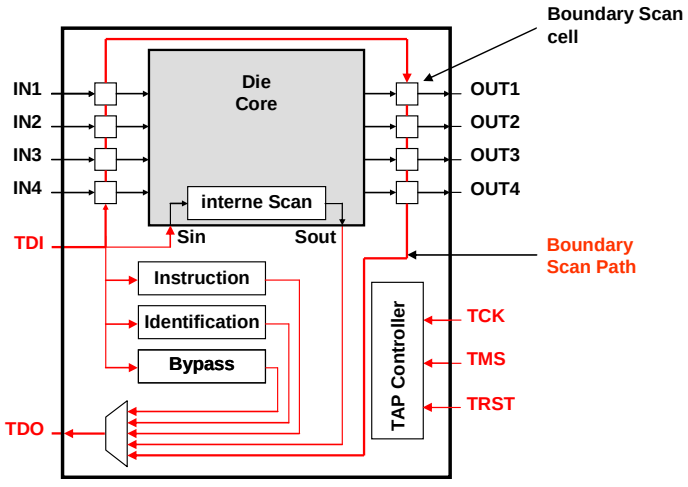


Figure 1-10: Compliant digital die with IEEE 1149.1

In addition to extra hardware components, the IEEE 1149.1 std. also defines a set of test instructions, including four mandatory ones (BYPASS, SAMPLE, PRELOAD, and EXTEST), and several optional ones.

An outline of test procedure using boundary scan is as follows:

1. A boundary-scan test instruction is shifted into the IR through the TDI.
2. The instruction is decoded by the decoder associated with the IR to generate the required control signals so as to properly configure the test logic.
3. A test pattern is shifted into the selected data register through the TDI and then applied to the logic to be tested.
4. The test response is captured into some data register.
5. The captured response is shifted out through the TDO for observation and, at the same time, a new test pattern can be scanned in through the TDI.
6. Steps 3 to 5 are repeated until all test patterns are shifted in and applied, and all test responses are shifted out.

I.2.C.b. Test access port

The TAP of 1149.1 contains four mandatory pins and one optional pin, as described below:

- *Test Clock Input* (TCK): is a clock input to synchronize the test operations between the various parts of a chip or between different chips on a PCB. This input must be independent of system clocks, so the shifting and capturing of test data can be executed concurrently with normal system operation.
- *Test Data Input* (TDI) is an input to allow test instructions and test data to be serially loaded respectively into the instruction register and the various test data registers.
- *Test Data Output* (TDO) is an output to allow carious test data to be driven out. Changes in the state of the signal driven through TDO should occur only on the falling edge of TCK.
- *Test Mode Select* (TMS) is the sole test control input to the TAP controller. All boundary-scan test operations such as shifting, capturing, and updating of test data are controlled by the test sequence applied to this input.
- *Test Reset* (TRST) is an optional pin used to reset the TAP controller.

I.2.C.c. Data registers and boundary-scan cells

Standard 1149.1 specifies several test data registers, as shown in Figure 1-10. Two mandatory test data registers: the *boundary scan register* and the *bypass register*, must be included in any boundary scan architecture.

a) Boundary-scan registers (BSR)

BSR is the collection of the *boundary- scan-cells* (BSCs) inserted at the I/O pins of the original circuit, as shown in Figure 1-10. A typical BSC is shown inFigure 1-11.

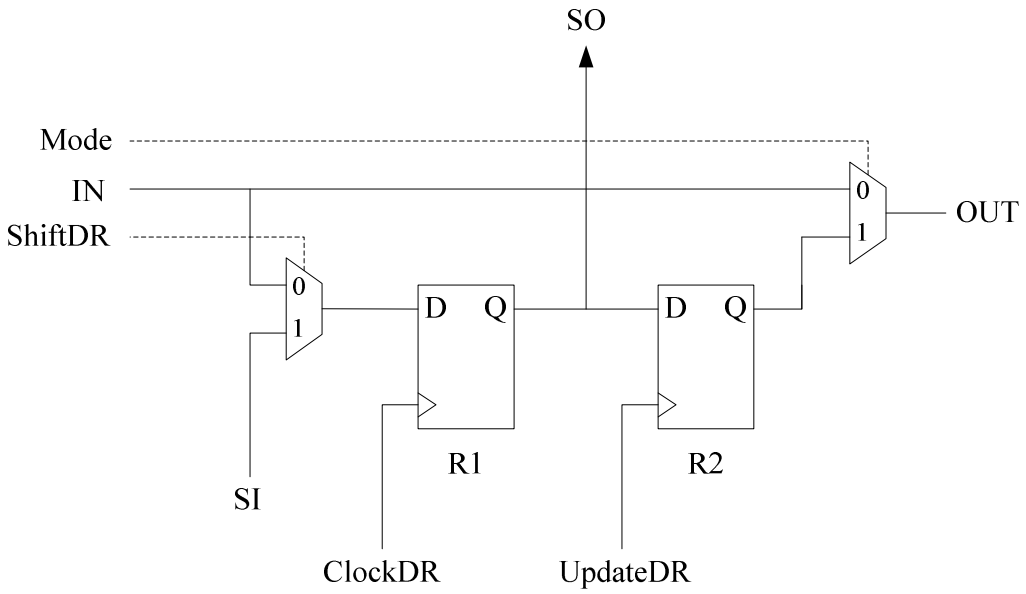


Figure 1-11: a typical boundary scan cell

This cell can be used as either an input or output cell. As an input cell, the IN signal line corresponds to a chip input pad, and the OUT signal line is tied to an input of the internal logic. As an output cell, IN corresponds to the output of the internal logic, and OUT is tied to an output pad.

The test operations of a BSC are controlled by three output signals of the TAP controller: ClockDR, ShiftDR, and UpdateDR. There are four major modes for the boundary-scan cell:

- *Normal mode*: simply passes inputs to outputs. (Mode = '0').
- *Scan mode* or *shift mode* passes data from SI to R_1 and from R_1 to SO. (ShiftDR = '1', ClockDR = clock pulse).
- *Capture mode* loads the value on the input IN to R_1. (ShiftDR = '0', ClockDR = clock pulse).
- Finally, *update mode* loads values from R_1 to the output. (Mode = '1', UpdateDR = 1 clock pulse).

To shift in data, the scan mode must be selected for a number of clock cycles. This number is dictated by the number of scan cells in the scan chain. Once the shift operation is complete, the update mode is selected for only one clock cycle to apply the data. To capture data and scan it out, one cycle of capture mode must be selected followed by the required number of scan cycles.

b) Bypass register

Bypass register is a single-bit register that is used to bypass a chip when it is not involved in the current test operation. This can significantly reduce test time required to shift in/out test data through the long TDI-TDO system path.

I.2.C.d. TAP Controller (TAPC)

The TAPC is a 16-states finite state machine, which operates according to this state diagram.

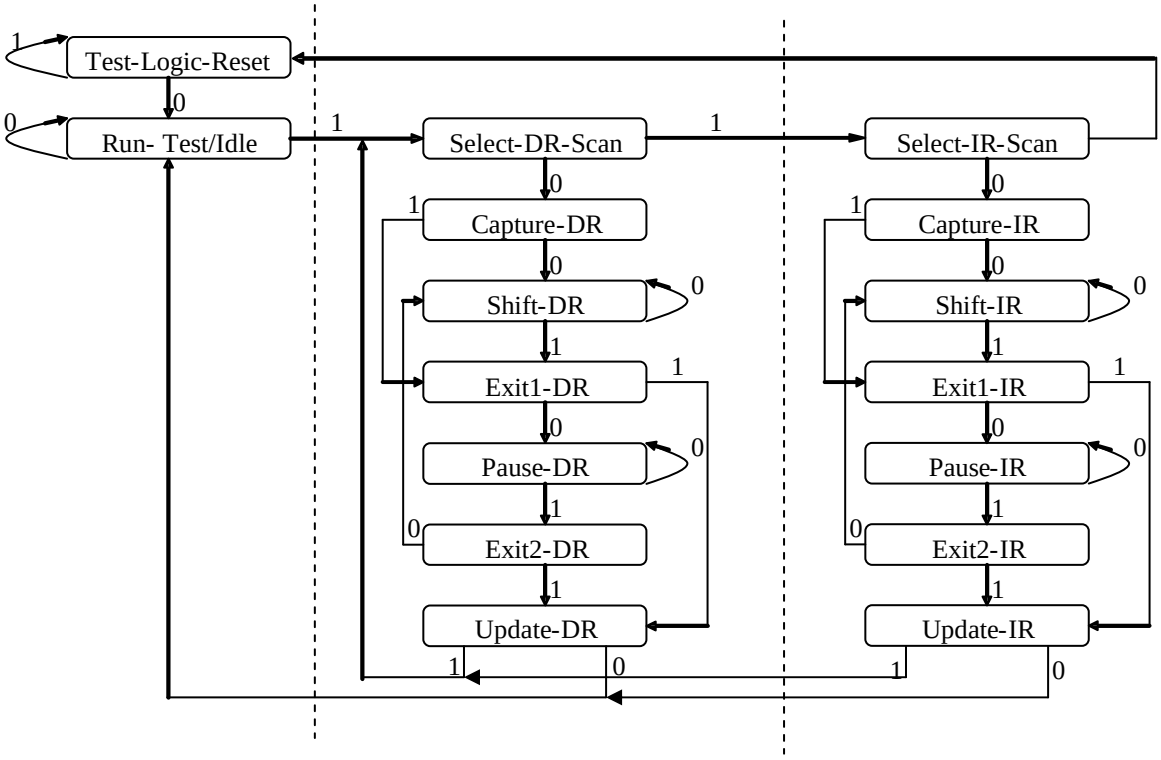


Figure 1-12: state diagram of TAP Controller

According to the state diagram shown in Figure 1-12, we give the data scan timing diagram as an example of test logic operation, shown in Figure 1-13.

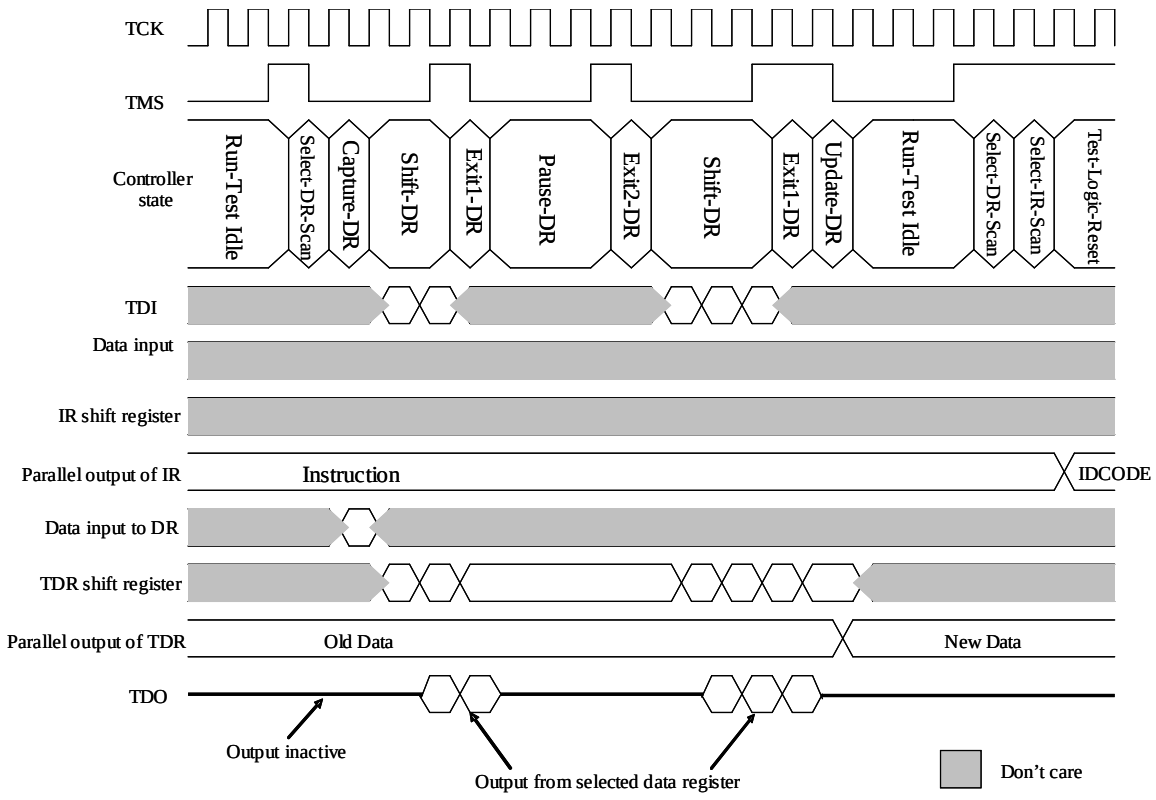


Figure 1-13: timing diagrams in scan operation [IEEE 1149.1 Std]

I.2.C.e. Instruction register and instruction set

The *instruction register* (IR) is used to store the instruction to be executed. The decoder associated with the IR decodes the instruction to generate the required control signals. Four mandatory boundary-scan test instructions (SAMPLE, PRELOAD, BYPASS, and EXTEST) are defined in 1149.1. In addition, the INTEST instruction is recommended. There are other useful instructions such as USRCODE, IDCODE, CLAMP… but they are not described here.

BYPASS: this instruction is used to "bypass" the boundary-scan registers on unused chips so as to prevent long shift operations.

SAMPLE: the sample operation can be completed when the Capture operation is executing, such that the required test data can be loaded in parallel to the selected data registers. This means that a snapshot of the normal operation of the chip can be taken and examined.

PRELOAD: this instruction allows test data to be shifted into or out of the selected data register during the Shift-DR operation, without causing interference to the normal operation of the internal logic (see Figure 1-14). This allows an initial data pattern to be placed at the latched parallel outputs of boundary-scan test operation.

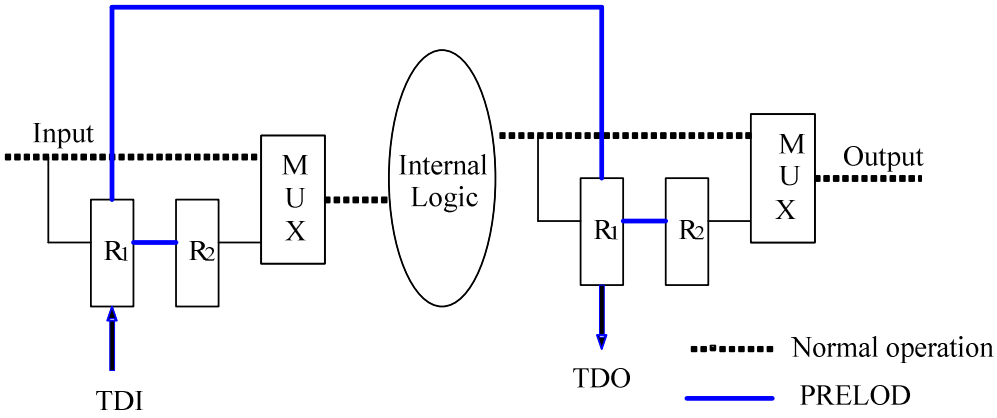


Figure 1-14: execution of PRELOAD instruction

EXTEST: this instruction is used to test the circuitry external to the chips, typically the interconnections between chips and between boards.

There are other versions for the standard IEEE 1149, such as 1149.4 [IEEE 1149.4] which is created to standardize the boundary scan for analog test, and 1149.6 [IEEE 1149.6], which is intended for advanced digital networks that include analog components and high speed I/O ports.

I.3 Testing at various manufacturing stages: test application issues

The microelectronic circuits go through several fabrication steps, prior to their exploitation by the end user. Taking account of the possible defaults which could be generated by the fabrication process, the circuits are tested at the end of each fabrication step. Only the fault-free circuits move to the next step, where the defected circuits are discarded in general.

The lifecycle of a circuit begins when the designers provide the circuit design masks. These latter are used to fabricate the circuits on a silicon wafer. Once the fabrication is complete, the circuits first undergo the "wafer test" (Figure 1-15), where the faulty ones

are marked to be discarded after wafer dicing. The next manufacturing step is packaging (for simple IC or SOC) or assembly with other circuits (in case of bare dies to be included in an SIP before packaging of the complete system. Once packaged, the chips undergo another test before delivery, named “final test”. The packaged circuits or systems that pass the final test are delivered to the board or product manufacturer. Delivered IC and systems are then assembled onto a *printed circuit board* (PCB). The PCB is tested before and after assembly of the components in order to check the interconnections and the assembly process. Later, this PCB is integrated in the final product, which is tested before sale. At this point, the fabrication flow of the IC is finished, where it is now ready to be exploited by the end user.

Some applications require test and diagnosis during the chip lifetime, which means to perform an in-situ test.

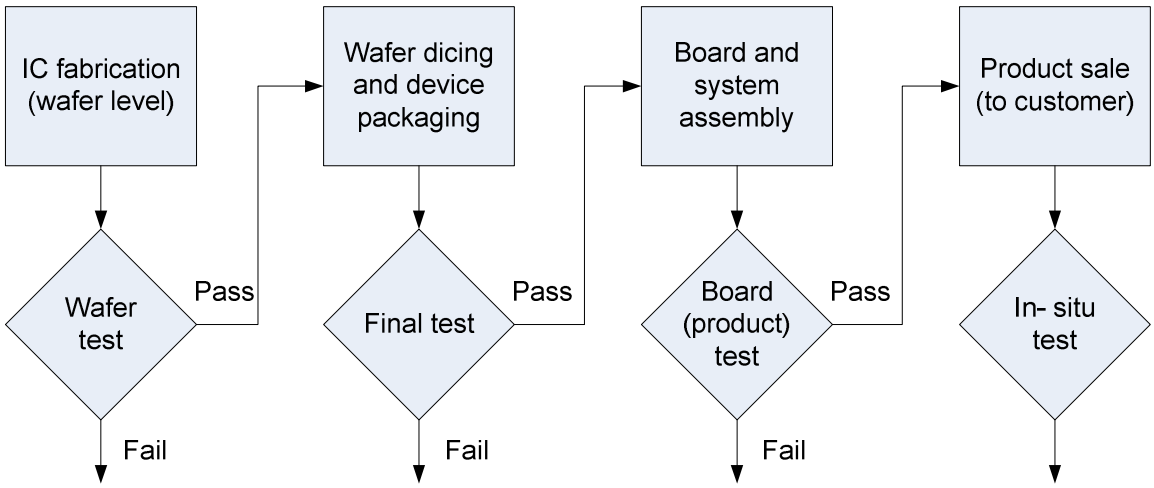


Figure 1-15: IC manufacturing and test steps

A short state-of-the-art of the wafer test technologies is presented in section I.3.A to exhibit the major technological problems. Once the circuits are packaged, the compound needs to be tested again: in section I.3.B, we will see what the most critical issues are. Some considerations will be additionally addressed in sections I.3.C and I.3.D, dealing with the board and the in-situ test issues.

I.3.A Wafer testing issues

Manufacturers try to catch the defects at the earliest stages of the circuit life for both cost savings and quality improvement. Indeed, every late detected defect represents a significant loss, and it is even more costly if it is detected by the customer after delivery. The preferred strategy therefore consists in reaching the highest possible coverage during the wafer test, to minimize the yield losses at final test. A test applied to a bare die is usually called ‘wafer test’ while a test applied to a packaged IC is called ‘final test’.

Clearly, an ATE must be connected to the primary I/Os of the DUT when test is applied. During wafer test, this connection is done with the IC pads through a dedicated *probe card*. The physical contact between the DUT pads and the probe tips is called a touchdown.

This contact-based technology suffers from several limitations and problems. For example, after testing a number of DUTs on a wafer, debris can accumulate on the tips of the probe needles due to repetitive touchdowns. This can affect the probe card efficiency and reduce the test quality in consequence. Thus, the probe tips must be periodically

cleaned. In the following, we address the major technological problems of current probing techniques. Next subsection presents different probing technologies and general related issues. The following section is dedicated to issues related to SIP testing.

I.3.A.a. Probing technologies and limitations

Probe cards are classified according to their probe tips type. The traditional technology is based on tungsten needles shaped in a cantilever profile. The shaft of each needle is held in place by an epoxy ring (seeFigure 1-16.) This technology remains one of the most widely used technologies in the probe card market today [Mann 2004].

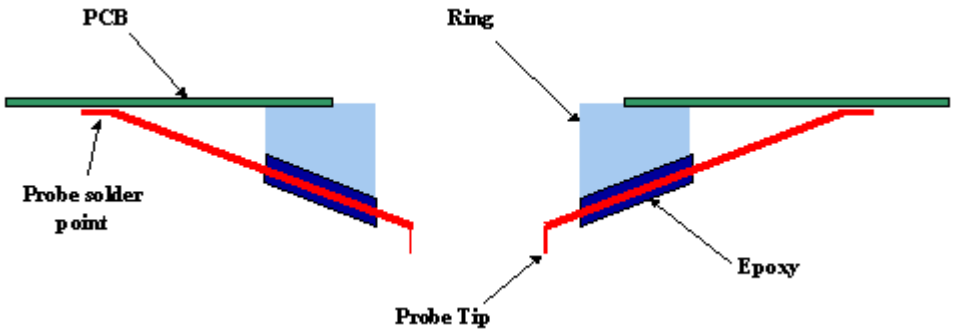


Figure 1-16: Principle of cantilever probe card [L-T. Wang 2008]

This technology suffers from pads scratching. In addition, the number of DUTs that can be concurrently tested (parallel test) with cantilevers probe card is very limited. In fact, two limiting factors are caused by the volume and the shape of the cantilevers: the alignment of probe tips and the important space required by the probe needles -dedicated to one DUT- above the wafer. Typically, the number of DUT concurrently tested with this type of probe card is limited to two.

The vertical probe is an alternative probing technology appeared in 1977. Basically, this technology was developed to fulfill the requirements for array configurations. An array configuration designates an IC design where the I/O pads are placed over the entire IC surface rather than being restricted to the perimeter. Recently, with the increasing demand for concurrent test, the vertical probe technology has known a growing use. Its principle is depicted in Figure 1-17.

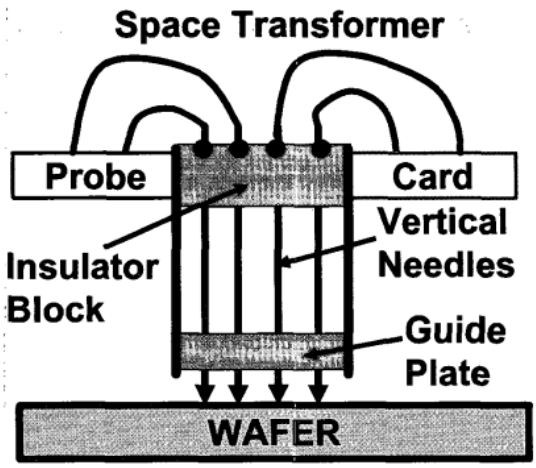
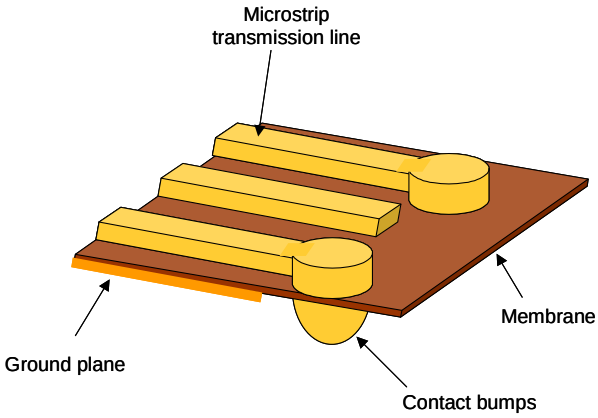


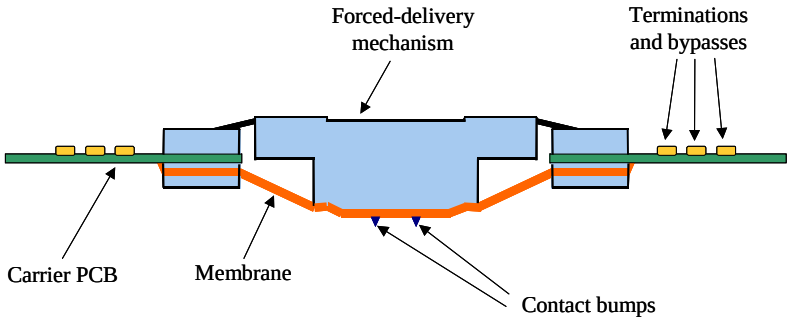
Figure 1-17: principle of vertical probe card [Mann 2004]

The “membrane” technology is a particular type of vertical probe cards, basically developed for RF IC testing. By reducing the distance between the pads and the test head

components, the membrane technology permits a better transfer of analogue and RF signals from the ATE to the DUT. Thus, the problems of signal attenuation and noise interference, encountered with classical probing techniques, are resolved. The membrane technology is illustrated in Figure 1-18. The signals transfer from the ATE electronics to the DUT is done through a set of micro-strip transmission lines, which are designed on a flexible dielectric material. The DUT is contacted by an array of micro-tips formed at the end of the transmission lines through "via holes" in the membrane (Figure 1-18.a) [Leslie 1989], [Leung 1995], [Wartenberg 2006]. The membrane is mounted on a PCB carrier that interfaces with the test board (Figure 1-18.b).



(a) Membrane technology



(b) Structure of the probe card

Figure 1-18: Membrane probe card [Leslie 1989]

In general, the vertical probe technology permits to test several DUTs in parallel, as much as the tester resources can support. However, this concurrent test is limited by the co-planarity factor. In fact, when test is applied, all vertical probes must contact the dedicated pads on the DUTs. A pressured touchdown may cause damaging to the DUTs, whereas a relaxed touchdown may leave some pads without contact. Therefore, it is preferred to test a limited number of DUTs with correct probing, rather than testing a higher number of DUTs with risked probing.

The vertical probe implies that the pad size and pitch (minimum distance between two pads) must be large enough to perform a correct contact with the vertical probe needles. However, pad size and pitch have regularly decreased, requiring more and smaller probe needles, and forcing probe cards therefore towards novel technologies. In addition, the growth of chip-scale and wafer-level packages put further demands on probes, which must contact now solder bumps instead of planar pads [L-T. Wang 2008].

An emerging technology, based on MEMS implementation of probe needles, is recently developed to push the mechanical limits forward. With this technology, the volume of probe needles is significantly reduced. Thus, pitches of 35µm can be achieved with minimal scratching risk, and a higher number of DUT can be tested in parallel. MEMS based probe cards are now starting to replace the traditional ones, where industrial products and research demonstrations show a growing interest in the MEMS-based technologies [Cooke 2005]. However, this novel technology -currently under development- is very expensive. In addition, like other technologies, it suffers from the debris problem. In fact, due to the probe needle reduced size, debris can rapidly accumulate on the MEMS cantilevers. Moreover, it needs more time to become sufficiently reliable. For that, this technology is not used today for high production testing.

Table 1-1 summarizes the main advantages and problems of probing technologies.

	Advantages	**Drawbacks**
Cantilever	simple and cheap	- pads scratching - limited parallel test - debris problem
Vertical	- large parallel test - testing of array configuration - reliable RF test (membrane technology)	- size and pitch of pads are limited - planarity problem - debris problem
MEMS	- bond pads probing - enhanced parallel test - reduced pitch size - no serious scratching problem	- very expensive - not a mature technology (still under development) - debris problem

Table 1-1: advantages and drawbacks of various probing technologies

To summarize, various probing technologies have been developed for IC testing. Each technology presents some advantages but suffers from several limitations at the same time. The reduction of the size and the pitch of the pads, the development of very complex devices, beside the increasing demand for multi-site (parallel) testing, have pushed the fabrication of probe cards towards the limits of the technology. However, even with the most advanced probing techniques, the wafer test stills suffer from contact problems, and it is expected to not be able to catch-up with the increasing requirements for high speed and high frequencies test needed for the complex circuits [Wu 2006].

In this section, we have discussed the major technological problems concerning the wafer test for any type of circuit. Additional limitations that are related to SIP testing are discussed in the next section.

I.3.A.b. SIP testing and related issues

A SIP is a sophisticated system, including multiple pre-tested dies and passive components. They are assembled together by a complex assembly process, where many

different interconnect techniques may be used for wire bonding and flip-chip connections. Thus, the resulting SIP is an expensive product. Knowing that a defective SIP cannot be repaired, we come therefore to the following observation [L-T. Wang 2008]:

"The SIP process is economically viable only if the associated yield Y_{SIP} of the packaged SIP is high enough".

Considering an SIP assembly process including n different dies, the overall yield Y_{SIP} can be ascertained by the Equation 1-1 [L-T; Wang 2008]:

$$Y_{SIP} = 100\,[P_1 \times P_2 \times \ldots \times P_n] \times P_s \times P_{int}^{Q} \times P_w\,. \quad (1\text{-}1)$$

Where P_i is the probability that die #*i* is defect-free, *Ps* is the probability of manufacturing a defect-free substrate (possibly including passive components), P_{int} is the probability of die interconnect being defect-free, *Q* is the quantity of die interconnects, and P_w is the probability of placement and mounting being defect-free.

The previous equation shows that the overall yield of a SIP manufacturing process depends on the quality of assembled components, as well as on the quality of the assembly process. In fact, complex process may create new failures, because:

- More stress is applied during assembly, which may cause die cracks, or broken bonding.
- Placement of active dies on passive die is a potential source of misalignment, i.e. shift and rotation (see Figure 1-19)

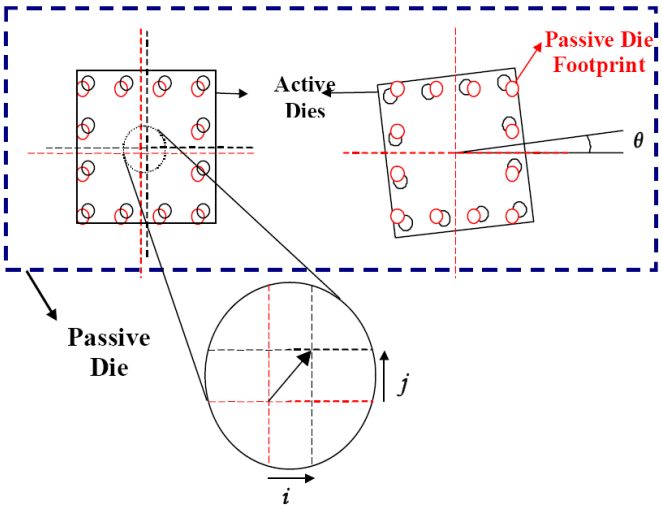


Figure 1-19: possible misplacement during assembly process: shift (left), and rotation (right).

Thus, dies must be of a high quality and the assembly process must be under control in order to achieve a viable yield. For that, a special strategy can be followed during SIP manufacturing process. It consists of:

1. Use of *known good dies* (KGD) in SIP fabrication. A KGD is a bare die with the same, or better, quality after wafer test than its packaged and "final tested" equivalent [Cauvet 2007].
2. An assembly process beginning by the cheaper die and finishing with the most expansive one, and

3. A recursive test after the assembly of each die, in order to avoid the loss of expensive dies not yet assembled, if any default is detected at current assembly phase.

However, recursive test requires several touchdowns on SIP pads. Even with the advanced probing techniques, performing several touchdowns may lead to substrate pad scrubbing (see), which may affect the quality of wire bonding.

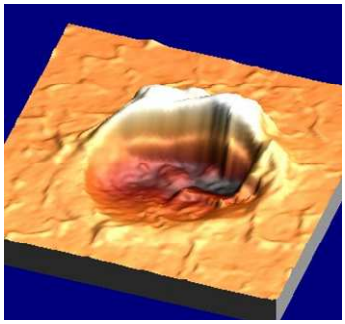


Figure 1-20: pad scrubbing due to several touchdowns (source :NXP semiconductors)

For this reason, the number of touchdowns is typically limited to three. In consequence, the number of assembled active dies is limited to two, since a preliminary test of the substrate is usually performed before to start the assembly process. Regarding the previous limitations of contact-based probing techniques, alternative solutions must be investigated for the particular case of SIP testing during manufacturing.

I.3.B Final testing

After wafer dicing, the expected fault-free devices (IC, SOC or SIP) are packaged. A package consists typically of a "*lead frame*" intended to hold up the bare device, and a kind of box intended to cover this device. The packaging process consists in putting the bare device on the lead frame, interconnecting the die pads to the lead frame pins, and finally fixing the box on the leadframe, creating therefore the final package. Once packaged, the circuits are tested before their delivery. This test is called final test.

In general, the final test tries to detect the possible defects caused by wafer dicing or packaging process, as well as to cover the misses of wafer test. Even when manufacturers try to guarantee the quality of the bare dies by an efficient wafer test, this objective is not easy to reach because of many limitation factors, such as limited contact and probe speed. Fortunately, these limitations do not exist in final test, where the contact is performed with the package pins instead of circuit pads. Moreover, high speed and high frequencies can be handled more easily than at wafer level [Mann 2004].

The final test consists in a combination of *functional* and *parametric* test. The functional test consists in applying a set of test vectors at the input of the DUT and verifying if the output responses are equal to the expected ones. The parametric test consists in verifying the limit values of circuit parameters. Two types of parametric test:

1- *DC parametric test*: it consists in measuring a DC current or a DC voltage during test application. According to the measured value, a "pass/fail" decision is done at the end of test.

2- *AC parametric test*: it permits to measure the dynamic parameters of a circuit: width of the clock pulse, propagation time, set-up time, hold time, fall time, etc…

After final test, the packaged circuits are delivered to the customer. Each delivery is characterized by a *defect level* (DL). A DL, called *reject rate* also, is the ratio of delivered faulty parts to the total number of delivered parts:

$$\text{Reject rate} = \frac{\text{Number of delivered faulty parts}}{\text{Total number of delivered parts}}$$

A reject rate of 300 *parts per million* (PPM) chips or less may be considered to be acceptable for mobile phones, while 100 PPM or lower represents good quality for home consumer devices. A reject rate of 10 PPM or less is needed for automotive applications.

I.3.C Board and product testing

Traditionally, the circuits on board have long been tested using a "Bed of Nails", usually combined with functional testing of every chip. However, this approach has several drawbacks. In fact, a Bed of Nails, basically used to create test access, requires the addition of "test-lands" to the PCB, which generates a significant board area overhead. In addition, fast functional tests are used to test the chips. These tests can target chip damages due to the assembly process but do not provide high fault coverage like a structural test for instance. To overcome these drawbacks, the current test strategy consists in using only "fault-free" chips and the JTAG boundary scan standard [van Geest 2001], [Schuttert 2004]. Following this strategy, the assembled circuits are considered fault-free components (high quality testing must thus be performed on every component before system assembly). Consequently, the board testing can be limited on faults possibly introduced during the PCB assembly process. That leads to focus the test on the interconnections between the circuits, in addition to a partial test of the circuits themselves to ensure that they are not damaged during the assembly process.

Following this strategy, the JTAG boundary scan technique is strongly adopted for interconnections test. Thanks to the analogue extension of the boundary scan standard (IEEE 1149.4), digital and analogue interconnections can be easily tested at board level. Concerning the test of the chips soldered on the board, the JTAG boundary scan infrastructure allows accessing extra test resources introduced by the DFT activity on every chip.

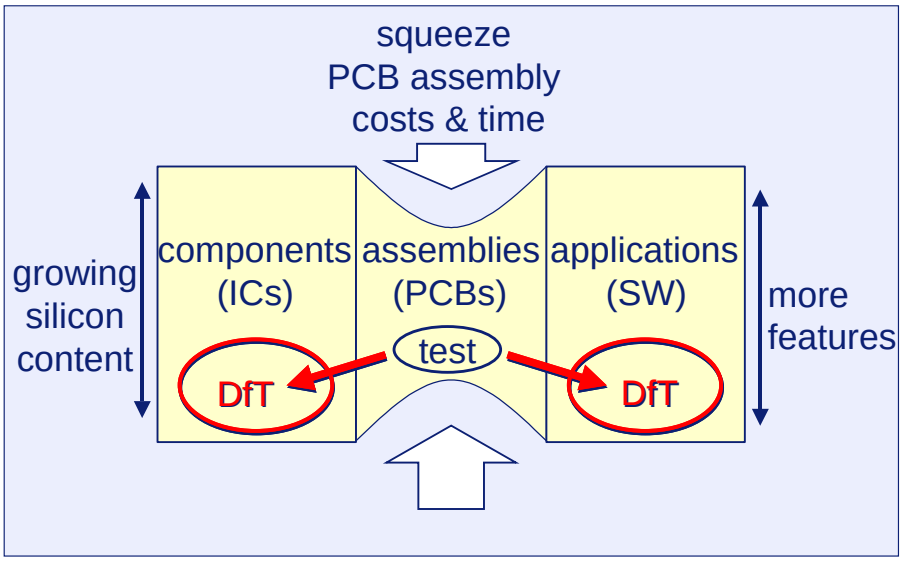


Figure 1-21: novel strategy of PCB assembly test [van Geest 2001]

To summarize, a novel strategy for board testing has been suggested. It consists in building or re-using on-chip test solutions (DFT), beside JTAG boundary scan for convenient test access. With this trend, the area overhead, costs and development time of board testing can be significantly reduced (see Figure 1-21).

As for components at lower level of integration, parallel and concurrent testing of several boards leads to save test application time. However, physical and contact-based accesses to several boards at a time require the development of a dedicated test infrastructure, where the test data could be broadcasted to a large number of boards.

I.3.D In-situ test

As discussed earlier, testing an integrated circuit or system at manufacturing time is a must to guarantee a high quality product, and After delivery, the device undergoes another test when it is assembled to the dedicated system (e.g. PCB). This last test aims to detect the possible defaults generated by the assembly process.

Once the system is successfully assembled, it becomes ready for use, and therefore, to begin its application lifetime. However, some applications need to test and diagnosis the devices on board or system during their active lifetime, which is the case for critical application (e.g. automotive, medical implants …). However, in order to perform an in-situ test, we need to satisfy two conditions:

- First, we need to provide an external access to the device embedded within the system.
- Secondly, this access must be reliable and non-intrusive as well.

In several cases, a wired contact with the DUT is not possible. This can be the case of circuits embedded in a satellite or a vehicle for example, or the case of medical implants in a human body. Thus, an attractive solution for such cases consists in using the wireless communications, where it provides a non-intrusive access to the DUT for in-situ test purpose.

I.4 Conclusion

Because defects created during the chip manufacturing process are unavoidable, the test activity plays a key role in this process by its ability to differentiate good devices from faulty ones before delivery to end-users, and to improve the manufacturing yield, where it permits to analyze and correct the causes of defects when encountered. Basically, testing consists of two processes: the test generation and the test application. Test generation designates the process of providing test vectors, whereas the test application refers to the process of applying those generated vectors to the DUT inputs and analyzing the responses.

As the microelectronic devices continue to shrink in size and increase in density, testing these devices has become increasingly difficult. In fact, while the number of primary I/O is stable, the integration of different cores in the same chip (SOC) or in the same package (SIP) continues to grow up. In consequence, the number of tests that must be applied to a manufactured circuit has increased, while the test access from primary inputs remains relatively limited. Thus, test generation becomes more complicated, implying a higher cost and a longer development time. To solve the previous issues, DFT techniques are increasingly adopted for circuits testing. The test application consists in applying the test stimuli from an ATE to the DUT and in collecting test responses from the DUT through a dedicated interface. As previously mentioned, the test application

suffers from several drawbacks and limitations according to the DUT (IC, SOC, or SIP) and the considered manufacturing or integration step.

At wafer test time, the ATE is connected to the DUT pads through a probe card. Various technologies of probe card have been elaborated for IC wafer testing, but every one has its limitations. The traditional probing technology, based on tungsten needles shaped in a cantilever profile presents a limited parallelism (number of dies on a given wafer that can be tested at a time) [L-T. Wang 2008]. In addition, it suffers from pad scratching and debris problems. These later ones are common also to the vertical probing technology [Mann 2004]. Moreover, it is expected that the vertical technology will not be able to catch up with the continuous decrease of pad size and pitch. Recent probing technology based on MEMS cantilever is currently under development, pushing the mechanical limits forward. However, this technology is very expensive and suffers also from debris problem.

Parallel testing of numerous devices (from bare dies to boards) is always a challenge due to the difficulty to contact numerous devices at a time. Additionally, in-situ testing encounters the problem of missing a reliable external access to IOs of the DUT embedded in the system. Finally, the particular case of SIP testing, which requires several touchdowns during the assembly process, increases the problems related to test application based on physical contacts between probe cards and DUT.

In result of all these contact-based test technology related issues (test costs, limited parallelism, pad scrubbing, in-situ testing) a test technology based on wireless transmissions appears as a possible alternative. For that, we propose a new wireless test solution, which can be used at various levels of manufacturing process. Before describing this solution, we give an overview of the wireless test methods currently under development in the next section.

II State of the art of wireless test methods

Several wireless or contactless test methods were recently proposed to solve the probing-related or contact-related issues. In this section, we first address the main challenges related to test strategies based on wireless communication, and we give a detailed description of several related methods proposed so-far for wafer or in-situ test. In the following, “wireless test” stands for test application strategies using wireless or contactless communications for transmission of test data between the test equipment and the DUT.

II.1 Wireless test challenges

The wireless test is proposed to solve the problems of contact-based test. Its purpose consists in transferring the test signals from the ATE to the DUT through a wireless link, to get rid of the probe needles and their limitations. Clearly, a wireless test interface must be added to the ATE and to the DUTs for this purpose. In consequence, some modifications must be done at design time in order to provide a wireless interface to the DUT, and classical test procedure must be adapted as well. These modifications generate new critical issues that must be addressed in any proposed wireless test approach, mainly the following ones:

- Power supply: In classical probing techniques, the ATE delivers the power and clock signals to the DUTs through the probe needles. However, no contact is

envisaged with the DUT in wireless test; and therefore, an alternative solution must be provided to deliver power and clock signals.

- Area overhead: clearly, an antenna and a RF transceiver and possible extra logic must be integrated in the DUT. The resulting area overhead is a critical issue that must be carefully considered.
- Transmission reliability: the reliability of the wireless communication is crucial. The *bit error rate* (BER) of the transmission must be very low. The possible errors of the RF transmission must not generate any error in the test application.
- MAC protocol: in order to establish a good communication between the ATE and the DUT(s), an efficient *medium access protocol* (MAC) must be used.
- Transparent solution: it is highly preferable that a proposed wireless solution do not imply any modification on the test generation process. Thus, the test programs and software remain unchangeable with wireless test.
- Test data management: once generated, the test data are transported from the tester to the DUT in wireless manner. Generally, the data are transmitted in *packets*. Thus, the DUT must be able to extract the test data from the received packets, and generates a packet to transmit its response, as well.
- Types of test: an interesting method is who permits to perform the large types of test, such as JTAG boundary scan, or BIST application that is not accessible through JTAG interface, etc…
- Security: the access to the internal circuit structures through the embedded wireless interface must be denied for anyone, except the person in charge of performing the test.
- Multi-usage: a powerful method is that which can be used at several stages of manufacturing (e.g. wafer test and in-situ test).

II.2 Scanimetrics approach

An emerging solution for wafer test was recently developed by “Scanimetrics”, a Canadian company. It consists of replacing the traditional probe card by a non-contact interface [Moore 2008], [Moore 2007], [Sellathamby 2005]. Following this approach, each probe needle is replaced by a couple of antennas and transceivers. A first “antenna & transceiver” is connected to the DUT pad, and a second “antenna & transceiver” is integrated in the probe card. Thus, a probe card with *n* probe needles is replaced by a probe card with *n* micro antennas and transceivers. On the other side, the DUT integrates equally *n* micro antennas and transceivers connected to *n* pads, and operating at the same carrier frequency. The communication between the probe card and the DUT is performed pad to pad; where *near field communication* (NFC) is used to transfer data at tens of megabit per second rates. The distance between the probe card and the DUTs is up to 100 µm, depending on the antenna size. The principle is depicted in Figure 1-22 and Figure 1-23.

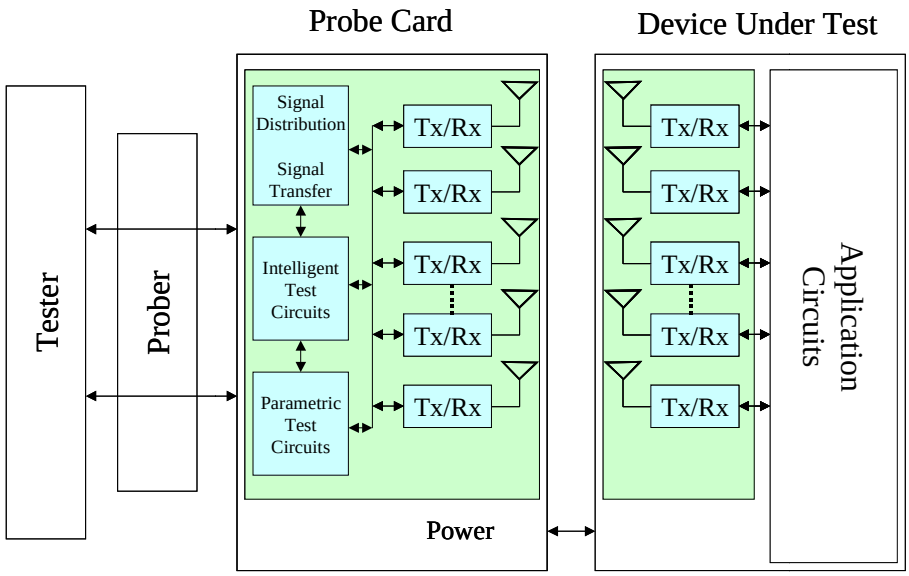


Figure 1-22: Scanimetrics principle of non-contact testing

(Courtesy of Scanimetrics)

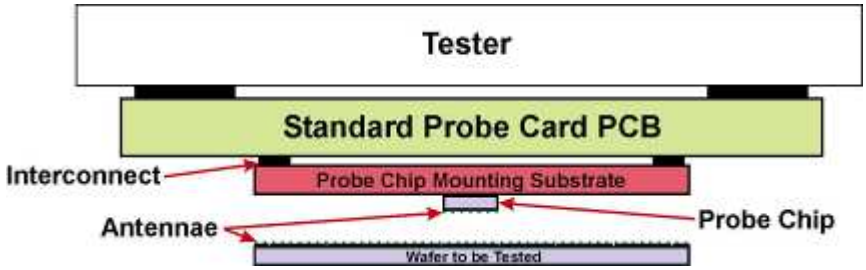


Figure 1-23: Cross-sectional view of the non-contact test solution

(Courtesy of Scanimetrics)

This novel technology offers many advantages including:

- High reliability of wireless communication due to the short-range communication.
- Since the communication is performed from pad to pad (without packets), so there is no need neither for MAC protocol, neither for data processing.
- Low complexity of the added DfT in the DUT (antennas and transceivers),
- The additional area overhead is negligible. In fact the antenna and transceiver can be implemented in a small area varying from 7200 μm^2 to 62500 μm^2 [Slupsky 2006], [Sellathamby 2005], according to antenna size and transceiver power, which increase when the distance between the wireless probe card and the wafer DUT increases. Note that, this overhead area is added to each pad, which must be multiplied by the number of wireless pads to calculate the global area overhead (e.g. 62500 μm^2 x 5, in case of JTAG test because of 5 JTAG signals requiring 5 wireless pads)
- The proposed solution is completely transparent for the actual test software,
- Various types of test such as scan chain, JTAG, etc… can be performed with this solution,

- No need for test data processing on the ATE side, and
- Significant reduction of test time because it enables a parallel test (up to 6 DUT tested in parallel) with high data rate.

However, this non-contact test approach requires the design of a specific chip to be placed on the probe card with “mirror” antennas and transceivers. Hence, for every new device (IC, SOC or SiP) design, a specific probe card must be designed. The alignment remains a key parameter, although the orders of magnitude can be significantly relaxed (up to 100 µm in z direction, and to 30 µm in X or Y direction).

The DUTs must be powered during test. In [Sellathamby 2005], the authors investigate the power delivery from the probe card to the DUT by non-contact means. For that, in addition to the micro antenna and the transceiver, a *power rectifier* (PR) is connected to each power pad in the DUT. The probe card delivers the power to the DUT power pads in form of AC electromagnetic signals. The PR circuits extract the power from the received AC signal and deliver it in form of DC current. The authors show that the amount of delivered power depends on the number of power pads on the DUT, which determines the number of *power rectifier* (PR) circuits (see Figure 1-24). The investigation result shows that the non-contact power transfer method could be used only for low and medium power devices.

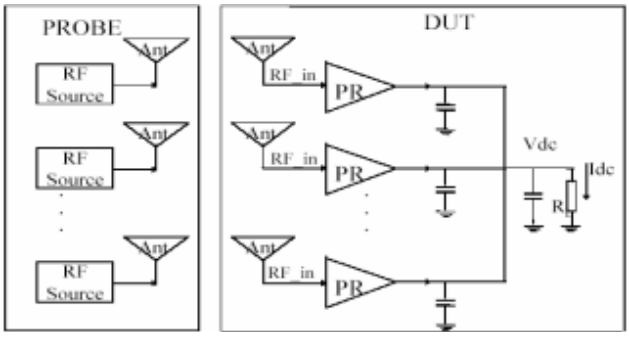


Figure 1-24: block diagram of power transfer system whithout contact [Sellathamby 2005]

For high power dissipations, the authors propose a hybrid solution: some power pads are directly contacted, while the remaining ones receive the power by non-contact means. Thus, a hybrid probe card must be used. It contains micro antennas and transceivers (for test data transmission, and partial power delivery) and some cantilevers (for power delivery). This hybrid solution is possible because the distance between the probe card and the DUT does not exceed the 100 µm, which permits the non-contact communication beside the physical touchdowns. However, the main restricting factor of this hybrid solution is the number of power and ground pads in the DUT. For a low number of power pads, the power is completely delivered by contact. In this case, only the power and ground pads are directly contacted, while the remaining pads (data) perform a contactless communication with the probe card.

This very promising wafer test solution cannot, however, be used for final or in-situ test. In fact, once the DUT is packaged, the near-field communication with the embedded micro antennas and transceivers becomes practically impossible. Thus, the utility of this method is restricted to the wafer test only.

II.3 HOY system

The HOY system proposed by the National Tsing Hua University (Taiwan) is a new wireless test approach, currently under development [Wu 2006], [Chen 2006], [Liou 2007]. This system is based on RF transmission to perform a wireless test of the integrated circuits, and targets wafer test, test after packaging and test during active application of the DUT (in-situ). However, the published papers show that the work was only conducted on wafer test. The general concept of the HOY system is illustrated in Figure 1-25.

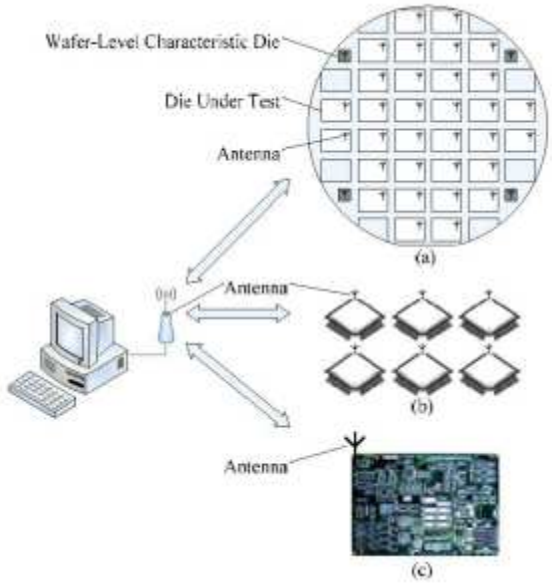


Figure 1-25: HOY applications: (a) wafer test, (b) chip test, and (c) field diagnosis [Wu 2006]

One of the primary goals of HOY system consists in reducing the test cost and discarding the expensive investment in the *automatic test equipment* (ATE) [Wu 2006], [Chen 2006]. Thus, the simplification of the tester is a key factor in the concept of the HOY system. For that, the implementation of advanced DFT techniques in the DUTs is necessary, in order to transfer the complexity from the tester to the DUTs. More particularly, the integration of BIST circuits and even *built in self repair* (BISR) in the DUT is heavily adopted by the HOY system [Wu 2006], [Ko 2007]. Based on that, the tester becomes a simple test controller. Its role is limited to initiate and control the BIST circuitry, and collect the response from the DUT at the end of test. Doing that, the tester can be drastically simplified to a *personal computer* (PC), as it is shown in Figure 1-25.

According to the HOY system, every DUT contains a “Test Module” and a “Communications Module” (see Figure 1-26). The “Test Module” contains the BIST and/or BISR circuitry and a standard interface called HOY Test Wrapper. The “Communications Module” contains the RF, baseband, and *medium access control* (MAC) circuits for communicating test commands and response data between the “HOY Tester” and the DUTs.

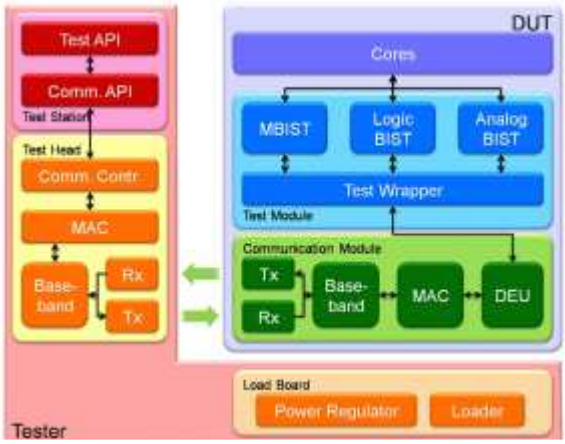


Figure 1-26: HOY architecture for wireless test [Liou 2007]

Every DUT on the wafer contains at least one wireless transceiver to communicate independently with the tester [Wu 2006]; however, this DUT transceiver is not directly described in anyone of the published papers.

In [Liou 2007], the authors describe the wireless transceiver that must be added to the ATE. It has the following main characteristics:

a) ATE transmitter:

- Output frequency: 902 ~ 928 MHz
- Modulation : *on-off keying* (OOK)
- Data rate: 250 Kb/s

b) ATE receiver:

- Input frequency: 2.4 ~ 2.5 GHz
- Modulation: *frequency shift keying* (FSK)
- Data rate: 250 Kb/s

Therefore, we can deduce from the previous ATE transceiver characteristics that the DUT transceiver has a constant bit rate equal to 250 Kb/s. it operates with two frequencies: 900 MHz and 2.45 GHz.

Unfortunately, there is no public information on the expected DUT antenna, and it is not clear if the DUT will have two separated antennae, one for the transmitter (Tx) and one for the receiver (Rx), or if it will integrate only one antenna adapted to work with both frequencies. Anyway, due to the size of the expected antenna(e) for the proposed frequencies (900 MHz and 2.5 GHz), this (these) antenna(e) seems too large to be integrated in the DUT; this remark leads us to suppose that the antenna will be build out the DUT, on the scribe lines of the wafer for instance.

The used MAC protocol allows the tester to establish the connection with the DUTs, broadcast the data to the DUT, and finally collect the responses from the DUT by individual “polling” [Ko 2007]. Thus, the tester must send a polling message to a DUT requesting its transmission. A DUT cannot transmit its response without being polled by the tester.

The *data exchange unit* (DEU) is the last layer in the communication module. Its role consists in storing the received data (from tester) in two buffers: Instruction and Data,

and storing the DUT response in a third buffer: Response. The data stored in Instruction and Data registers are used to control the function of HOY Test Wrapper (see Figure 1-27). Once DEU enable Wrapper, this later begins to fetch instructions and decodes them for initializing, controlling the BIST and sending out test results from BIST [Liou 2007]. Note that the Wrapper is designed according to the BIST controller description. The DEU and the Test Wrapper are illustrated in Figure 1-27.

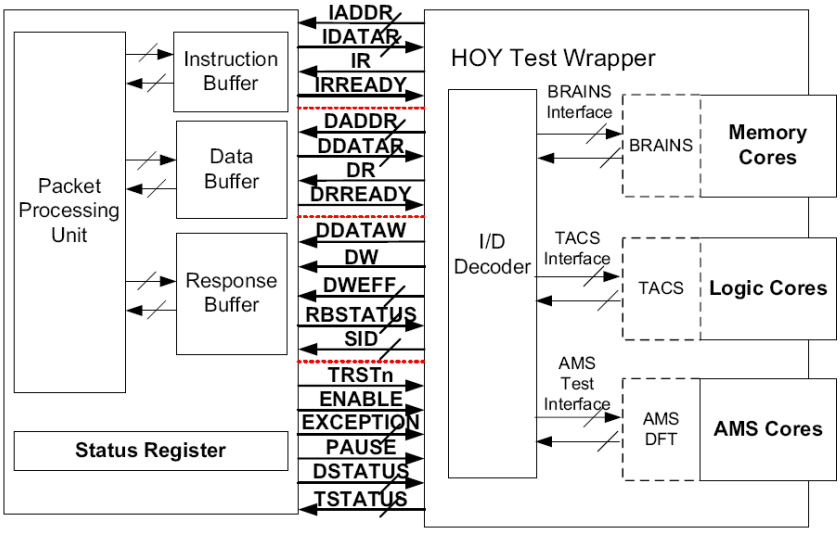


Figure 1-27: DEU and Test Wrapper of HOY system [Liou 2007]

For power supply, the designers of HOY system suggest to power the DUTs in wireless manner, and to generate the clock signal from the received signal (see Figure 1-28). Therefore, in addition to the "Test Module" and "Communications Module", the DUT must contain a "Power Module". This later consists of a power regulator and a clock modulator.

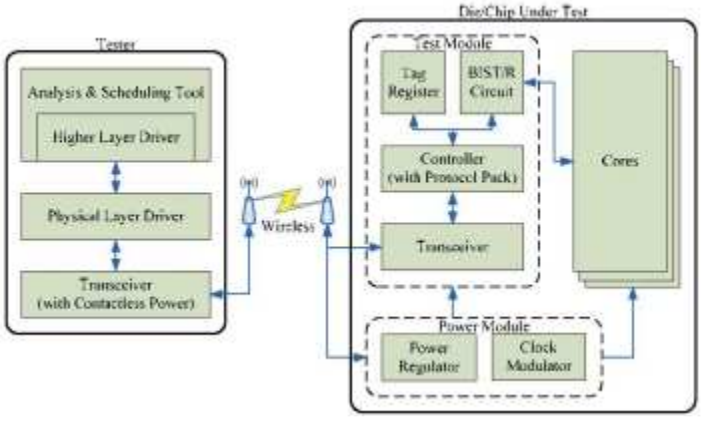


Figure 1-28: The HOY test system with contactless power supply [Wu 2006].

The power regulator extracts the average power of the received carrier through an AC-to-DC conversion, and provides the regulated power to drive the whole chip. The clock modulator generates the clock signal, in synchronisation with the tester [Wu 2006]. However, this method for power supply and clock generation implies a continuous signal transmission from the ATE and a continuous signal reception by the DUT. Thus, when there are no data to be transmitted (e.g. BIST is launched in the DUT), the ATE continues to transmit a signal without data (carrier only) to ensure the proper function of power regulator and clock modulator.

However, if the DUT has only one antenna for transmission and reception as it is shown in Figure 1-28, then the DUT transceiver cannot perform a simultaneous transmission and reception even if the Tx and Rx operate at different frequencies; otherwise the high power signal generated by the Tx is injected in the Rx, damaging its components. In consequence, the antenna cannot be connected to the Tx and to the Rx at the same time. Following that, when the DUT sends back its response to the tester, the DUT Rx and "Power Module" cannot receive any signal from the antenna. Therefore, both components of the "Power Module" cannot operate as expected, and the clock signal cannot be generated properly. Moreover, if the antenna is integrated in the DUT (as inFigure 1-25.a), then it will be a very small antenna. Hence, the amount of signal power captured by this antenna is insufficient to power the DUT during test.

In case of DUT equipped with two antennae, it is possible that the "Power Module" receives a continuous signal, allowing it to work properly. Anyway, the wireless powering method does not guarantee a high power quality for the DUT, which implies the use of a special mechanism to stabilize and monitor the power. Taking account of these difficulties, the HOY system designers proposes the contactless power supply as an option necessitating a further investigation, and not as final solution [Wu 2006]. From the previous remarks, we come to the following conclusions:

- The HOY system is limited to BIST test only. JTAG interconnection testing, scan tests and other types of test are not supported by the HOY system, restricting the usage to systems including IP cores equipped with their own BIST circuitry and cores developed by the system integrator where fault simulation is conceivable.
- The generation of "Test module" depends on the BIST controller description; i.e. the "Test module" is specific to each circuit.
- According to the proposed frequencies, the expected antenna is too large to be integrated in the DUT.
- Wireless power supply for wafer testing is not yet fully explored.

In summary, the HOY system – currently under development – needs further development before proper evaluation. Its usage is restricted to systems including IP cores equipped with their own BIST circuitry.

II.4 "JTAG Technologies" solution

An interesting method for remote wired or wireless communication to board and system level boundary-scan architectures (in compliance with the 1149.1 standard) has been proposed by JTAG Technologies [Collins 2005], [Reis 2006], [Sparks 2006]. According to this method, an in-situ boundary-scan testing is possible, by utilizing the existing wired or wireless communication protocol.

One of the basic ideas of this patented solution [WO2004/046741] is to use existing JTAG controllers according to the IEEE 1149.1 standard and the software thereof, which have the following characteristics:

- They have the five JTAG signals as I/Os.
- The connection of the test controller with the DUT is synchronous.
- The TCK clock driven from the test controller is free running and cannot be switched off.

- Once the first bit of TDI is shifted out on the rising edge of TCK, a first bit read out from the DUT is expected on the JTAG controller TDO input on the next rising clock edge. Since the TDO is updated at the falling edge of TCK in the DUT, this means that the amount of time available for TDO to travel from the DUT to the test controller is half the TCK period.

The architecture of the proposed solution consists of a transceiver pair, one (named TapSpacer Uplink) connected to the boundary scan controller and the other (named TapSpacer Downlink) connected to the board or system under test. The Uplink and the Downlink transceivers use the existing communication interface for connection, which is an asynchronous interface in the most of communication techniques. The general concept of this solution is illustrated in Figure 1-29.

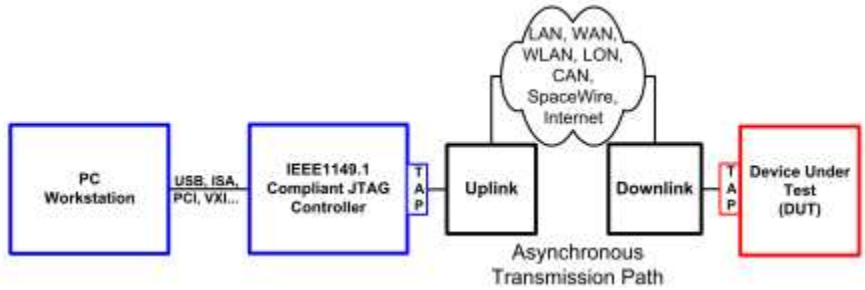


Figure 1-29: proposed architecture of remote boundary-scan [Collins 2005]

The proposed solution is designed to be transparent for the JTAG test controller. Therefore, the characteristics of the test controller mentioned above must be respected, especially the last one. However, the signal is always delayed on an asynchronous transmission path. Supposing that the round trip transmission delay is calculated to be 100 ms for example, in this case the maximum achievable TCK frequency is 5 Hz, leading to very long test time.

In order to have a reasonable TCK frequency, authors in [Collins 2005] propose to add a component at the end of the boundary scan-chain in the DUT. This component is a "virtual" boundary-scan register made of boundary-scan cells not connected to any IO of the DUT (see "virtual" boundary scan cells v1 to v20 in Figure 1-30). That means that a component comprising of *n* boundary scan cells (*n* = 20 in Figure 1-30) is added to the test architecture description of the targeted boundary scan DUT. In this sense, the proposed solution is not completely transparent for the system developer.

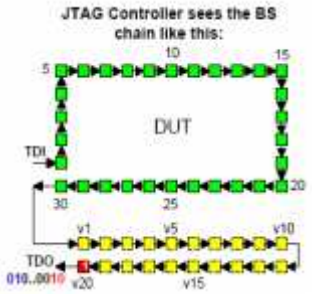


Figure 1-30: principle of virtual component as seen by a test controller

The number of virtual added cells depends on the round trip propagation delay, the communication link speed, the delay created in the encoding and decoding required by the data transmission protocols, and the latency. Regarding that, the worst case delay

must be defined and the corresponding number of virtual cells is added to the end of boundary scan register.

The Uplink gets the TDI, TMS, TCK and TRST from the test controller, and sends only the TDI and TMS bits to the Downlink by packets, which are transported over the existing communication channel of the targeted board/system. Once the Downlink receives a packet, it extracts the TDI and TMS signals, generates the TCK locally and applied them to the DUT. The TDO generated by the DUT is packed and sent back to the Uplink. Once received, this later will store the TDO in a temporary buffer and prior to entering the shift state, the virtual-cell counter will be preset for the prescribed number of virtual cells (see Figure 1-31). Hence, for every TCK cycle within the shift sequence, the virtual-cell counter will decrement until it reaches zero. At this point the uplink will start transferring the real TDO data to the test controller for comparison against the expected TDO data. Doing that, the test control expects the TDO to arrive after predefined delay, which allows variations in the data transmission and latency. Therefore, all the characteristics of the test controller are respected.

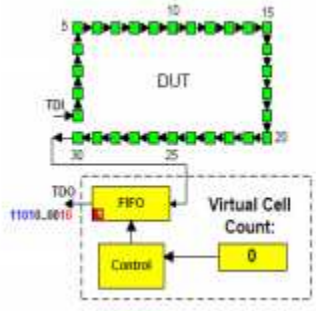


Figure 1-31: hardware implementation in the Uplink of the virtual cells

Public information on this work is not available, particularly with regards to the following points:

- How the Uplink and Downlink TapSpacers are implemented? And how they communicate with the existing system interface.
- How the TDI and TMS are packed into packets: Do these packets have a packet header? Do they have a constant size, or a field in the packet header for showing the packet length?
- How transmission errors are managed?

In summary, the proposed method implies the addition of one virtual component to the description of the DUT at the cost of additional test time. It suggests that each packet sent by one node of the transceiver pair is correctly received by the other one in the predefined delay. Cases of transmission errors are not discussed. Not that, there is no problem concerning the power supply and the clock signals, since they are delivered to the DUT from its embedding system.

II.5 "Sun Microsystems" wireless approach

A wireless test concept for systems on board was developed in "Sun Microsystems" laboratories [Eberle 2004], [Eberle 2002] based on a wireless version of the JTAG standard. This wireless test approach aims to replace the wired scan paths on the board by wireless ones. Thus, the indirections appearing in architectures using daisy-chained or hierarchical wiring are replaced by direct connection between the system controller and

the monitored device on the board. An antenna and a RF transceiver are added to each monitored device for this purpose. This is illustrated in Figure 1-32.

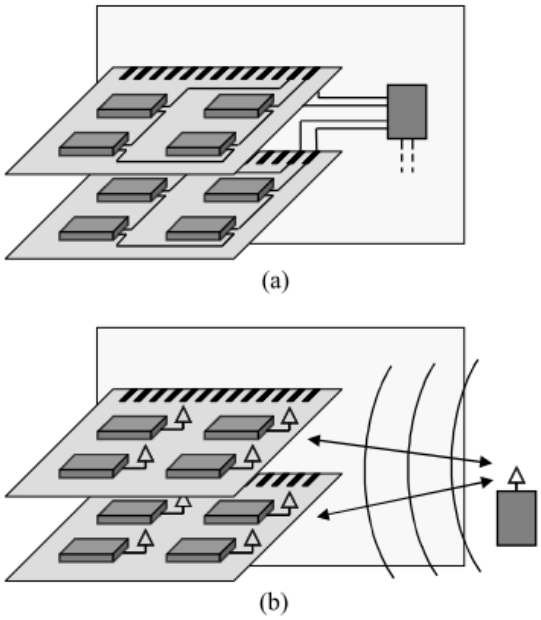


Figure 1-32: wired scan path (a) vs. wireless scan path (b) [Eberle 2004]

This solution offers the opportunity for systems on board to be non-intrusively tested. It permits also to the *electrically erasable programmable read-only memories* (EEPROM) or *field-programmable gate array*s (FPGA) to be wirelessly reprogrammed, without having to physically connect a programmer to the device. Finally, the proposed solution provides direct and more reliable connection to every DUT on the board compared to physical interconnects technologies.

Clearly, there is no problem concerning the power supply and the clock signals in this context, since they are delivered to the DUTs from the board resources. On the other hand, equipment with wireless resources is less critical for system on board for systems on chip. Taking into account this particular context and focusing on the present work (wireless testing of integrated systems from the manufacturing phase down to in-situ testing), here we are interested to the packet format (data processing), the MAC protocol, and the test types supported by this solution.

a) Data processing

According to this solution, the packet used for the wireless exchange has a maximal length of 24 bytes. Among them, there are 8 bytes containing the necessary information for communication, which allow the receiver device to have a reliable connection with the transmitter device. The remaining 16 bytes (at maximum) are reserved for data.

b) MAC protocol

The proposed solution uses a MAC protocol to manage the transmissions between the tester and the DUTs. Communication is based on a master/slave protocol whereby the system controller implements the master and the DUTs on the cards implement the slaves. Message exchanges use a simple request/acknowledge protocol: The master sends a command in a request packet and the slave returns a reply in an acknowledgment packet. That is, a single master initiates all packet transfers and slaves can only send packets after they were instructed to do so by the master (polling).

c) Test types

Eberle et al. describe a possible use of wireless transmission for other applications than boundary scan test. The concept of systems wireless monitoring is given in [Eberle 2004]. In fact, the monitored systems integrate normally an EEPROM, which is permanently updated following the system state. Eberle et al. describe in their paper the idea of EEPROM wireless reading, via an RF interface added to the monitored systems.

In summary, Eberle et al. propose a wireless approach for wireless test and monitoring of the systems on board. The proposed solution is not envisaged to be used for wafer test. It is suitable for big systems only, where the form factor is not really critical.

II.6 Wireless test methods for intra-chip test

A wireless communication for transmission of data between different cores inside the DUT was proposed [Chang 2001], [Zhao 2008], [Zhao 2006], [Y. Wang 2006]. None of these solutions addresses the question related to the transmission of data between the tester and the DUTs. In [Chang 2001], the authors investigate the implementation of RF transceivers coupled to the RF nodes in the DUT. The communication control between multiple RF nodes inside the DUT is addressed in [Zhao 2006], [Zhao 2008] as a network topic. Finally, in [Y. Wang 2006], the authors investigate the new wrapper architecture of each core in the DUT to be compliant with the RF communication, without giving any technical details. While related to wireless transmission of test data, the target application (wireless transmission between cores inside a system) shows specific issues (e.g. integration of many antennae, one per core) that do not apply for the problem addressed by the present work.

II.7 Conclusion

Several wireless/non-contact methods have been proposed so-far, either for wafer test or for in-situ test. Only the HOY system targets both applications. However, the HOY system is limited to BIST solutions where the data volume to exchange between the tester and the DUTs is very limited. Other types of test such as scan test or interconnect testing are not supported. Moreover, the proposed solution raises the very difficult issue related to the wireless transfer of power and clock signals during wafer test.

“Scanimetrics” company has elaborated an interesting non-contact test method for wafer test. Test signals are transferred from the ATE to the DUT test structures through near-field, pad to pad communications. This approach supports all test types (scan test, JTAG, BIST…), and does not imply the integration of additional circuits rather than the antennas and transceivers that are added to every I/O pad. The near field communication with the integrated antennae and transceivers becomes practically impossible after system packaging. Thus the proposed solution cannot be extended to in-situ application.

A wireless test method for in-situ test was elaborated by “Sun Microsystems” for systems on board. Aiming to avoid physical interconnections in the system test infrastructure, the physical paths between circuits on the board are replaced by a direct wireless communications between the ATE and every chip on the board; a wireless test interface is added to each chip for this purpose. This solution cannot be transported to wafer test where the goal is to test simultaneously a large number of identical DUT and where antennae and transceivers must be integrated to every DUT at manufacturing step.

The method proposed for remote testing by JTAG Technologies supposes that the system embedding the targeted DUT has a communication interface (WiFi, Bluetooth,

Internet, etc…). The method consists in using this system interface to perform a remote JTAG boundary scan test. Clearly, it cannot be used for wafer test. A summary of the main characteristics of the previous methods is given in Table 1-2.

		HOY System	**Scanimetrics**	**Sun Microsystems**	**Reis**
Usage	Wafer	Yes	Yes	No	No
	In-situ	Yes	No	Yes	Yes
Test types	JTAG	No	Yes	Yes	Yes
	BIST	Yes		?	No
	others	No		?	No
Transparent solution		No	Yes	?	Yes
Parallel test		Yes	Yes, but limited	Yes (up to 15)	No
Area overhead		Large	Negligible	Large	?
Communication		Far field (900 MHz, 2.4 GHz)	Near-field, pad to pad	Far field (916 MHz)	Any communication interface
MAC protocol		Yes	No	Yes	That of the system interface
Data rate		250 kbit/s	Tens of Mbit/s	19.2 Kb/s	Up to 10 Mbit/s
Security issue		To be addressed	No problem	To be addressed	N/A

Table 1-2: summary table of wireless test methods

Our goal is to develop a wireless test method that can be used at several levels while it covers several types of test at the same time. Indeed, our study targets wafer test, board test, and in-situ test. In addition, it aims to provide a solution for several types of test such as Boundary scan test, BIST applications (without JTAG interface) etc… Finally, massive parallel testing of several DUTs on a wafer is also in order to reduce wafer test time.

Chapter 2

Wireless Test Solution: Principle and Architecture

Chapter 3

Implementation and Experimental Validation of Wireless Test Control Block

Chapter 4

Perspectives: Extension to System and In-situ Tests

Discussion and conclusion

As the microelectronic devices continue to shrink in size and increase in density, testing these devices becomes increasingly difficult. At wafer level, the test is usually performed using probing technologies. However, the contact-based probing techniques will may not be able to catch up with the increasing requirements in terms of parallelism, increasing number of I/Os and decreasing form factors. New test methods based on non-contact or wireless transmission were proposed. However, these solutions were limited to wireless activation of BIST structures (HOY system), wafer testing (Scanimetrics approach), or board level testing (Sun Microsystems's solution).

In order to cope with all related challenges, we elaborated a novel wireless test approach based on the integration of a Wireless Test Control Block (WTCB) in every DUT. This solution allows broadcasting the test data to all the DUT on a wafer allowing a massive parallel test, and thus improved test times, particularly when the test response evaluation is performed on chip. The WTCB interface has been designed as a modular architecture allowing smooth integration in different contexts. It consists of a Wireless communication module for wireless transmission of test data and a TCB for test application and test response collection to/from the system components. The TCB was designed to handle the DUT response in two ways according to the need of precise of global feedbacks.

The communication module embeds a protocol stack of three layers: application, MAC and PHY layers. The application layer is the interface of the communication protocol stack with the TCB. It analyzes the application header of the test stimuli packets sent by the tester (DL packets) in order to generate the necessary information to the TCB, and encodes the application header for test responses packets sent back to the tester (UL packets). The MAC protocol is based on the master/slave model, and relies on allocating a temporal window for a group. It ensures a deterministic medium allocation, where each DUT can by itself send its test result without individual polling. This is a key factor in our solution because it permits to save test time by avoiding individual polling as proposed in the HOY system. The PHY layer is a key factor in the design of WTCB, but it was not the main objective of this work, for that it was only briefly described.

In order to validate our original solution, we conducted several experiments. First ones targeted the power supply issue when addressing iterative wireless testing of SIPs during the manufacturing process. Our proposal of power supplying all the devices from dedicated pads implemented on the wafer border was experimented on real wafers. These experiments showed the feasibility of opening windows in the DUT seal ring for supplying the power from lines embedded in the wafer scribe lines. Complementary works are needed for ascertaining that systems connected to the same power line are sufficiently supplied.

Secondly, we elaborated a dedicated experimental platform that emulates a tester and a WTCB. The tester prototype is implemented using a personal computer (PC) and a first FPGA, and the WTCB is implemented using a second FPGA. This platform was successfully used to perform a wireless test of two distinct circuits. The first one, developed for the targeted experimental validation, was implemented on a FPGA. The second one was an ASIC provided by the industrial partner of this project. Both were successfully tested through the proposed platform. Conducted experiments permitted to validate the following points:

- The operation of the tester-DUT link in both ways: uplink and downlink.
- The efficiency of the proposed protocol stack, especially the application layer and the MAC layer.
- The good interaction between the protocol stack and the TCB.
- The efficient design of TCB, and the good functioning of its components: the JTAG test controller, the packet disassembler and the comparator.
- The two comparison modes, i.e. the centralized mode (comparison in the tester) and the distributed mode (local comparison in the WTCB)

Note that, a demonstration with multi-site test is currently under development. It aims at proving the capacity of our solution to perform parallel testing of multiple devices.

Complementary works must be conducted on the WTCB PHY layer, concerning the integration of an antenna and a transceiver. These works will allow the proposition of complete WTCB IP. Finally, an important work should be conducted on the tester side in order to integrate the required wireless interface.

As the microelectronic industry becomes more and more essential in several domains, such as automotive, health care, nuclear, environment and civil application, in-situ testing solutions get an increasing interest for many applications. In this context, our solution can be extended to be used for remote in-situ testing. In fact, thanks to its modular design, the proposed WTCB could be developed as an independent IP and connected with the functional interface of a system, providing therefore a reliable access between a remote tester and an embedded test infrastructure.

Because wireless communication technology is used in increasing number of fields, radio-communication means are native resources in an increasing number of devices. On the other hand, a PC equipped with an appropriate wireless interface is sufficient for many remote testing applications. Taking into account the previous observations, our solution could preferably be developed for in-situ testing. For that, we are currently writing a patent proposal for defining the WTCB IP in the context of in-situ testing [Noun 2].

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List of acronyms

A

ADC: analogue to digital converter
AM: amplitude modulation
ATE: automatic test equipment
ATPG: automatic test pattern generation

B

BGA: ball grid array
BER: bit-error rate
BIST: built-in-self-test
BISR: built-in-self-repair
BS: base station

C

CRC: cyclic redundancy check

D

DAC: digital to analogue converter
DC: direct current
DfT: design for test
DSP: digital signal processor
DUT: device under test

E

EEPROM: electrically erasable programmable read-only memory

F

FM: frequency modulation
FPGA: field-programmable gate array
FSK: frequency shift keying

G

GPS: global positioning system
GSM: global system for mobile communications

H

HDL: hardware description language

I

IC: integrated circuit

IP: intellectual property

K

KGD: known good die

L

LF: low frequency
LGA: land grid array

M

MCM: multi-chip module
MEMS: micro-electromechanical systems

O

OFDM: orthogonal frequency division multiplexing
OOK: on-off keying
ORA: output response analyzer

P

PAN: personal area network
PC: personal computer
PCB: printed circuit board
PR: power rectifier

Q

QPSK: quadrature phase-shift keying

R

RF: radio frequency
Rx: receiver

S

SIP: system in package
SNR: signal to noise ratio
SOC: system on chip

T

TAM: test access mechanism
TAP: test access port
TPG: test pattern generator
Tx: transmitter

U

UHF: ultra high frequency
UMTS: ultra mobile telecommunication system

V

VHF: very high frequency
VLSI: very large scale integration

W

WLAN: wireless local area network
WPAN: wireless personal area network

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Table 3-2: centralized comparison mode: experimental UL packet (test responses) sent back from the DUT to the tester..... **Error! Bookmark not defined.**
Table 3-3: distributed comparison mode: experimented DL packet (test data) sent from the tester to the DUT..... **Error! Bookmark not defined.**
Table 3-4: distributed comparison mode: experimental UL packet (test responses) sent back from the DUT to the tester ..... **Error! Bookmark not defined.**