"Analogue Network of Converters": a DfT Technique to Test a Complete Set of ADCs and DACs Embedded in a Complex SiP or SoC

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UNIVERSITÉ MONTPELLIER II
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THÈSE

Pour obtenir le grade de

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Discipline : Systèmes Automatiques et Microélectroniques
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La science est toujours utile,
On ne perd pas le temps employé à l'acquérir
[proverbe chinois]

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Introduction

The conventional approach to test analogue/RF systems is to test each component separately. The methods developed to test these components are matured and effective considering that the system is made of physically independent elements, because we need to access the primary inputs and outputs of the components. Another required condition is the use of analogue instruments with better performances than the component under test ones. For instance, it is commonly admitted that to test a N-bit ADC, there is a need of at least a N+2-bit analogue waveform generator.

The trends for system design make difficult to match all these required conditions. Indeed due to an increasing integration rate it becomes difficult to access primary inputs and outputs of components under test. In addition it becomes difficult to find effective analogue test instruments. Chap.1 describes precisely these trends for system design and gives the resulting test issues. A new trend in test development consists in addressing the test at a system-level and not anymore at a core-level. A state-of-the-art of the test methods dealing with these test constraints is also given.

Considering all these promising test approaches at a system-level, it usually appears that integrated Digital-to-Analogue Converters (DAC) and Analogue-to-Digital Converters (ADC) are respectively used as stimuli generators and test response digitizers. In order to enable the use of integrated converters for a test purpose, they should be firstly tested to insure their quality and effectiveness. The second chapter is dedicated to a new test method that we have developed. This method is called ANC-based method and has been developed to test a set of Analogue-to-Digital Converters (ADC) and Digital-to-Analogue Converters (DAC) embedded in a complex system such as a SiP or a SoC. The ANC-based method has been developed considering previously given test issues relative to system design trends.

The purpose of the third chapter is to validate the theoretical developments previously described by evaluating the efficiency of the ANC-based test method. The efficiency will be considered in terms of accuracy for the estimation of some dynamic parameters according to converter resolutions and performances. The validation is conducted in two steps: simulation and hardware measurement.

The test method is suited to test a set of converters embedded in a complex system. It has been developed for a general case considering the converter architectures and resolutions and the number of converters under test. As a consequence the domain of application of the method has been extended to the test of stand-alone ADCs and DACs and to the calibration of analogue instruments. Finally, the proposed method is extended in the fourth chapter to a larger application field including stand-alone ADCs and DACs, as well as the calibrationof analogue instruments.

Chapter 1

Context and state-of-the-art

I Context

I.1 Introduction

Nowadays microsystems find applications in many domains. Indeed microsystems are used in consumer applications but also non-exhaustively in automotive, space, and healthcare applications. These different domains tend to drive microsystems development in many directions, considering different purposes, and consequently inducing a lot of challenges. This first part of the chapter presents an overview of the development trends for systems, and the related test issues.

I.2 Systems development trends

I.2.A Increasing system complexity

A complex system is usually made of heterogeneous components, in other words components made in various technologies and consequently working in different domains, such as RF, mixed-signal or digital ones. A high-level complexity is reached when the system works in the three domains. We find such complex systems in mass production applications like cell phones, WLAN transceivers, digital TV receivers, near-field communication devices, automotive electronic products, but also in specific application fields such as instrumentation, industrial, and aerospace. In wireless applications, the system architecture is traditionally divided into an RF front-end transceiver and a base-band section. They are interfaced with analogue-to-digital converters (ADC) and digital-to-analogue converters (DAC).

Increasing system complexity is driven by the trend in offering more and more services with one product. The best example of this service integration trend is the cell phone. Indeed a current cell phone offers a huge number of services. These services can be classified in two categories: hardware and software services. Following tables give a non-exhaustive list of current and future services.

Hardware services	Software services
Digital TV reception	Voice/Image recording
Wireless Bluetooth communication for headset	SMS
Wi-Fi communication for internet connection	Games
Compass	Mp3 player
Sensors for camera and video camera	Polyphonic rings
	Organizer

Table 1-1: Current cell phone services

Hardware services	Software services
Health monitoring	Distant learning/ home office
Defibrillator	More secured services
GPS	e-education
Context awareness	e-commerce
	Location based services (news, maps…)

Table 1-2: Future cell phone services

According to the example of cell phones, it is obvious that the multiple services available with actual complex systems push towards the developments of RF, mixed-signal and digital components.

Higher bandwidth is obviously a dominant driver to more RF applications development. It is pushed by the combined development of increasing internet use, the growing size of transferred files and increased bandwidth of wired connections. Indeed nowadays communication standards are USB2, Firewire or gigabit Ethernet connections, that offer bit rates over 200Mb/s. Figure 1-1 gives a chronological description of the evolution of frequencies used for RF application.

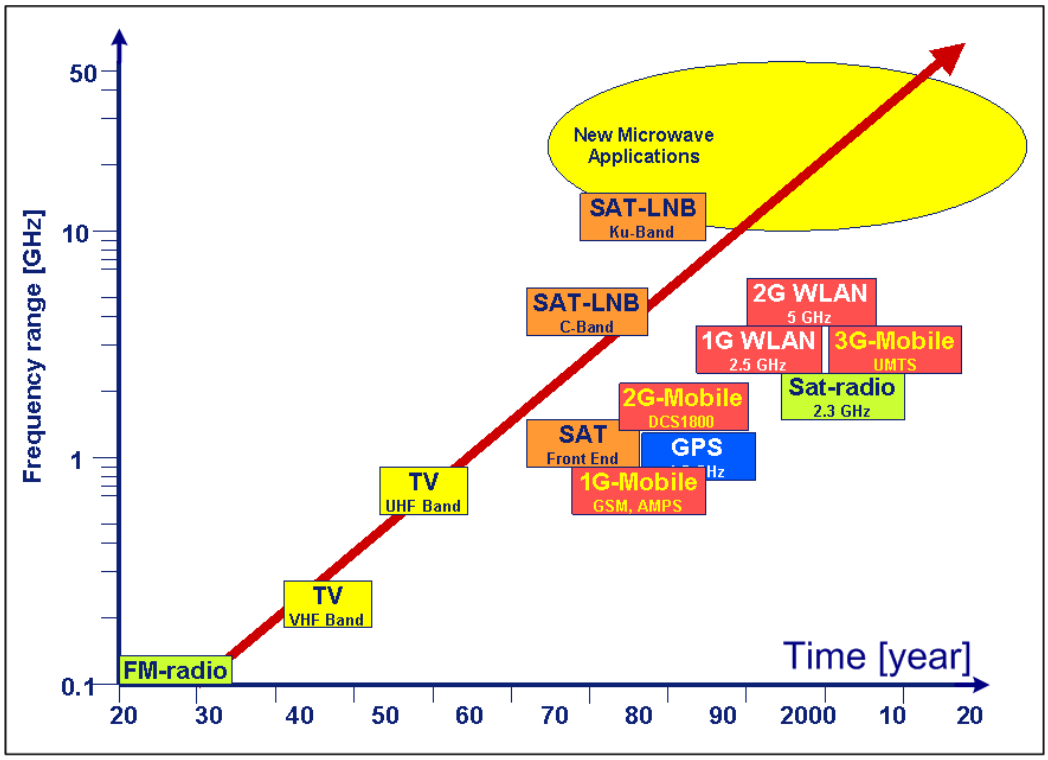

Figure 1-1: Chronological evolution of RF application frequencies [hooi03]

Chronologically, the first RF application was AM radio. It is also the first RF broadcasting application. Following RF broadcasting applications were Frequency Modulation (FM) radio (87.5-108.5MHz), developed by Edwin H. Armstrong in 1933, TV very high frequency or VHF (174-230MHz), TV ultra high frequency or UHF (470-860MHz). Once analogue modulation limits has been reached, thanks to digital modulation and satellite communication, a next step has been overcame. Indeed nowadays standards use gigahertz frequencies. Future RF broadcasting would be done at 20 or 30 GHz.

The second application of RF transmission is mobile telephone. On contrary to broadcasting applications, mobile phone applications had a very fast development. In only 10 years from 1990 and 2000, it has reached a high-level integration rate and has flooded the market. The first generation was using 900MHz band. Currently, the mobile phones of the third generation (Ultra mobile communication system UMTS) use the 2GHz band. Future generations would work at 40GHz.

The third RF application, Wireless Local Area Network (LAN) and Personal Area Network (PAN) have emerged from the success of mobile phone, internet and need of wireless broadband internet access. This is the third application to RF communications, nowadays using the 2.4-2.5GHz bands, and over 10GHz in the future.

Because of increasing frequencies, some parasitic elements become dominant. Layout elements that could be ignored become non-negligible and influence circuit performances [hooi03]. Some of these new contributive elements are interconnections such as bond pads, bumps. Consequently, the test of these components becomes a real challenge.

Complex systems tend also to integrate more mixed-signal components such as analogue-to-digital and digital-to-analogue converters, with increasing resolution and frequencies. The resolution is depending on the quality requirements of the signals coming from or sourced to the RF section [mirf07]. In addition to the improvement of their performances, the number of data converters is growing in integrated systems. The following figure gives an example of a complex system embedding several data converters. The product is the NXP pnx8327 type, a digital television decoder system. Apart from RF and digital components, it embeds 2 ADCs and 6 DACs.

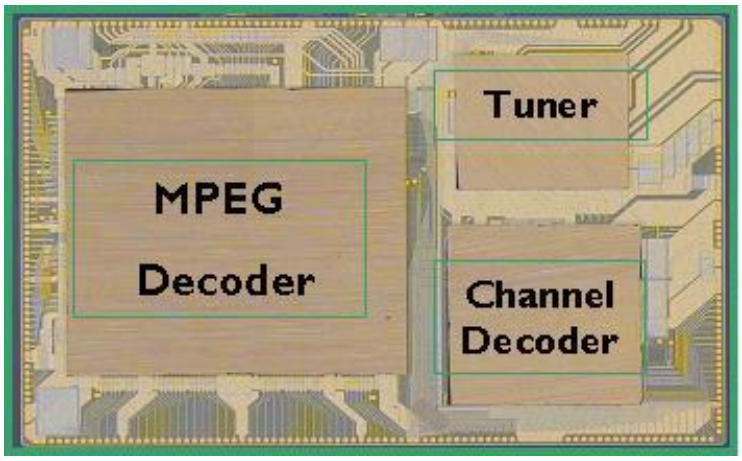

Figure 1-2: NXP pnx8327, digital TV receiver for set-top box application

The functional frequency race is not only the spearhead of personal computer processor manufacturers. Indeed, as previously mentioned, complex systems propose an increasing number of services in one product. Those services are not only hardware-based new functionalities. But they are in majority software services proposing image or sound processing, or multi-media applications. This demand drives the development of the digital functions in the systems, with key factors such as the clock rate, and the computational and storage capabilities. An example of such a complex system embedding a lot of digital elements is the Intel PXA800f, it is a cellular processor for wireless-internet-on-a-chip. Figure 1-3 gives an overview of the block diagram of the product. The digital part embeds four types of memory:

- ✓ SDRAM stacked
- ✓ Intel Flash stacked
- ✓ Intel Flash
- ✓ SRAM frame buffers

Additionally, this SoC includes a lot of computation units.

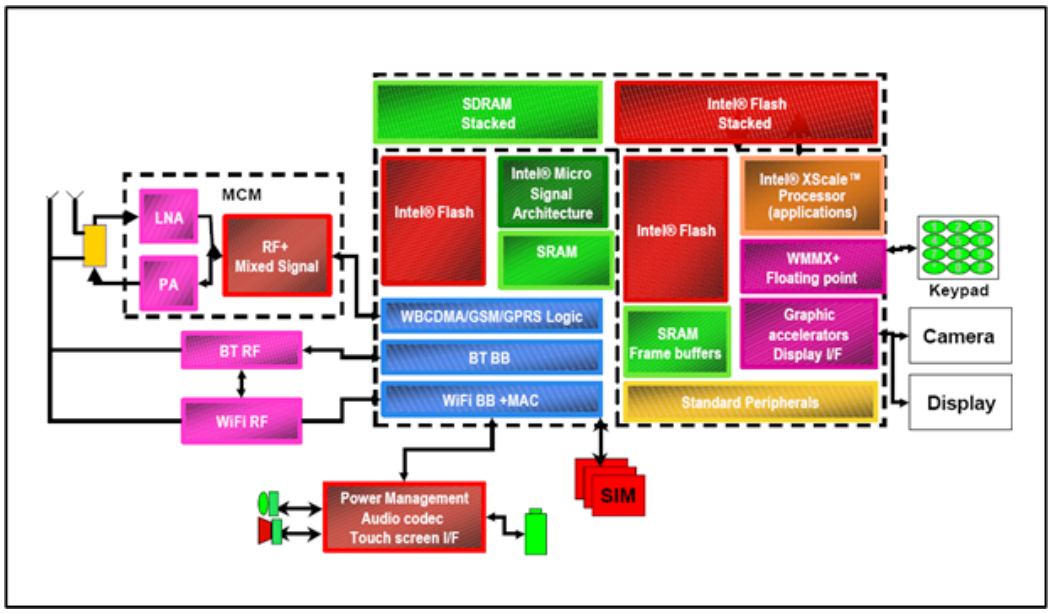

Figure 1-3: Intel pxa800f

I.2.B Increasing hardware integration rate

Because of the high-volume nature of consumer products, cost reduction has always been a key factor of success for chips suppliers. As a consequence, the integration density is also increasing in parallel with the improvement of the system performances. Additionally, the reduction of the form factor represents a key advantage in portable applications [farl04], thanks to a decreasing number and to a size reduction of the components. Figure 1-4 illustrates the reduction of the number of components in a mobile. We can see that, as the cellular phone was flooding the market, the number of IC's in the system decreased by a factor of 10, from 300 to 30.

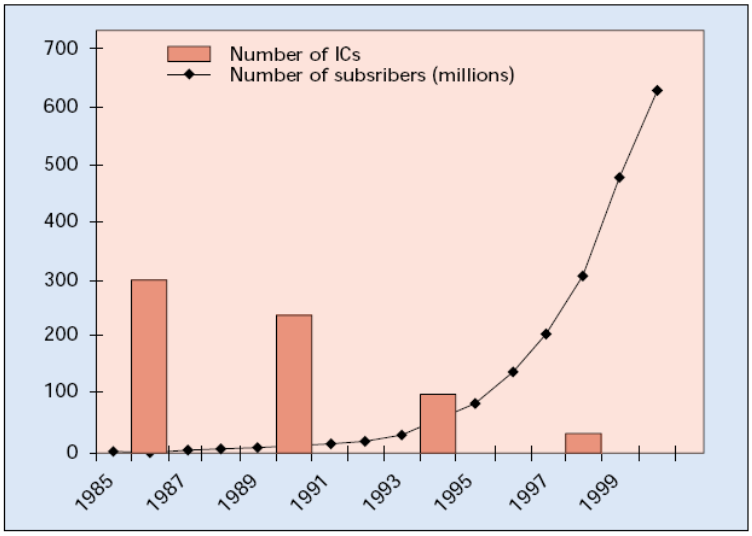

Figure 1-4: Chronological description of number of ICs in a cell phone / number of subscribers [bi01]

The desire for low off-chip component count in RF applications has led to the introduction of even more integrated RF front-ends, using architectures like zero-IF or near zero IF. Following Figure 1-5 gives an example of a typical block diagram of a direct conversion or zero-IF transceiver architecture. This architecture uses the now well-known IQ modulation. It is a hardware implementation of a rectangular to polar coordinate conversion. The transmitted signal will be of the form

$$s(t) = I(t)\cos(2\pi f_0 t) + Q(t)\sin(2\pi f_0 t) \qquad \textbf{eq. 1-1}$$

where I(t) and Q(t) are the signals to transmit, digitally modulated. And f_0 is the carrier frequency. This IQ modulation gives a higher signal quality.

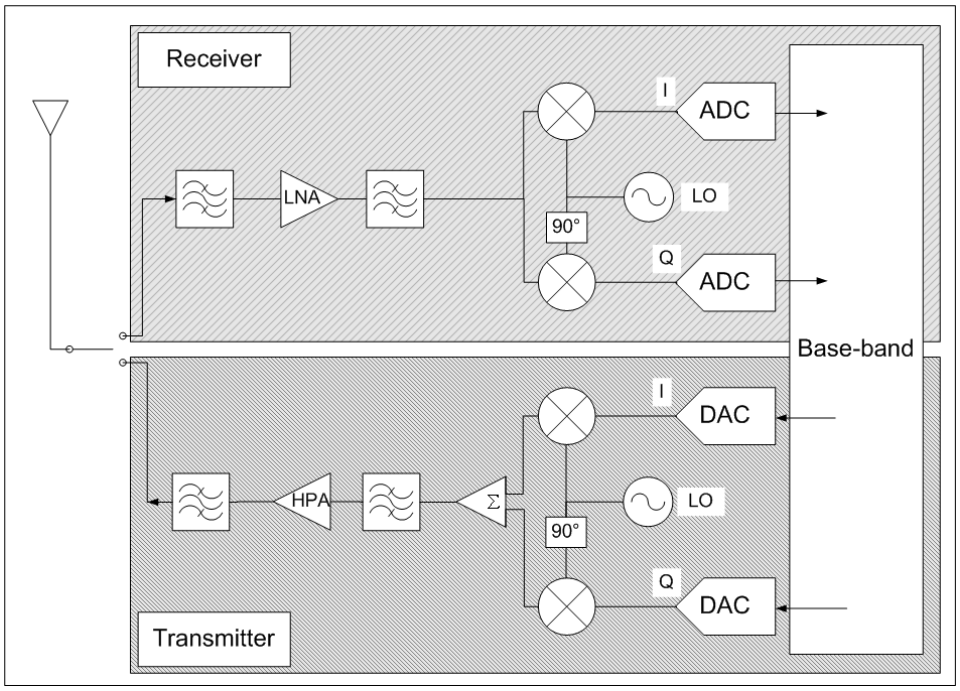

Figure 1-5: Zero-IF architecture

Figure 1-6 presents a superheterodyne architecture with an IQ modulation. The superheterodyne architecture is based on several frequency shifting. Each frequency shifting requires a mixer and a local oscillator. As a consequence the more you shift your frequency, the more you increase the number of required components.

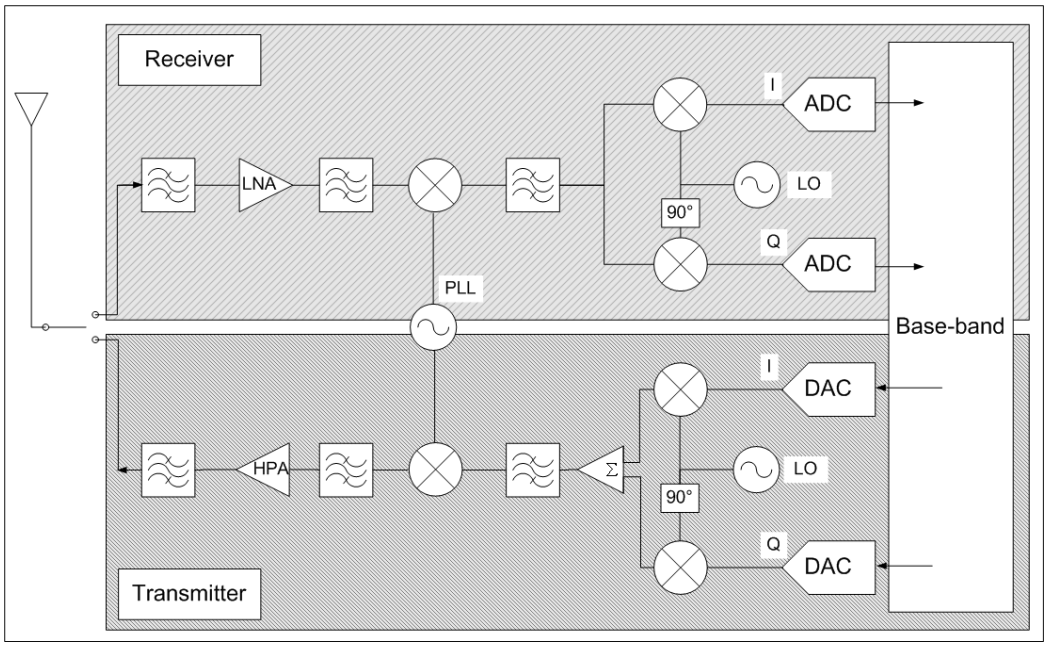

Figure 1-6: Superheterodyne architecture

These two types of RF transceivers illustrate the trend towards a reduction of the number of analogue components, in other words to a digitization of the transceivers.

Indeed, pushed by the steady development of successive generations of CMOS technology, processing capabilities have become so high that complex functions like demodulation are now performed in the digital domain. Over the years the analogue-to-digital converter (ADC) in receivers has thus moved slowly towards the antenna. The whole digitization of analogue functions is actually limited by the power consumption of ADCs [hooi03].

The digitization for signal processing in RF applications and the increasing frequencies in the end-systems (cell phone, WLAN, Bluetooth…) have led to the introduction of a new concept, the software-defined radio (SDR). A SDR system is a radio communication system, which can tune to any frequency band and receive any modulation. In order to enable the adaptability of the system to several frequencies and modulations, significant amount of signal processing is transferred from analogue/RF to digital domain. As a consequence a new run for a new form of radio protocol consists in running new software.

Figure 1-7 gives some hardware implementations of potential SDR.

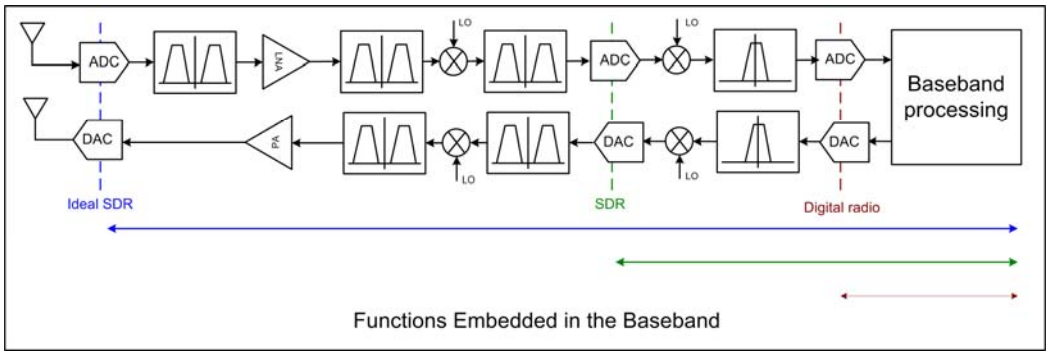

Figure 1-7: SDR architecture

The ideal SDR is made only of one antenna, some ADCs and DACs and a big computation unit. However, it cannot be really implemented yet, because of the limited bandwidth of the data converters.

The ultimate reduction of off-chip components is reached once we have only one package for the whole system. This final step can nowadays be reached using new technologies: SiP or SoC. As previously mentioned a complete system is made of digital, mixed-signal, analogue and RF components. Each component requires a particular technology. Thanks to recent technology developments, some solutions have been developed to embed all these components in only one package.

The SoC technology is created from a single chip, as a consequence a SoC is made using only one process technology. In addition it uses only one type of interconnections from the die to the package. The interconnection technologies used are wire bonding or flip chipping.

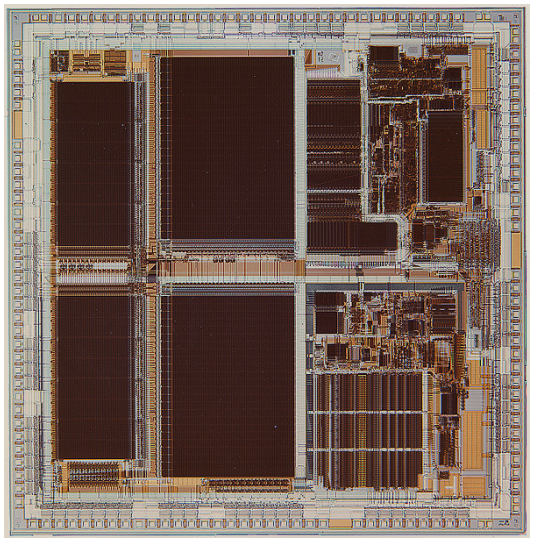

Figure 1-8: Example of SoC embedding, CFPA chip developed by CVAX.

The second technology able to increase the density is the System-in-Package or SiP. Actually the SiP technology is not based on one solution, but various configurations are now available, using the stacked-die or the planar assembly, or both. A very attractive technology, named silicon-based SiP, has been developed for some years by NXP, based on two principles.

- ✓ Stacking active dies on a passive one
- ✓ High level integration of passive components in the passive die

Several different process technologies are used to fabricate the different dies (CMOS BiCMOS GaAs). In addition several interconnection levels are used between different dies, using several interconnect technologies (wire bond, flip chip, soldering, gluing).

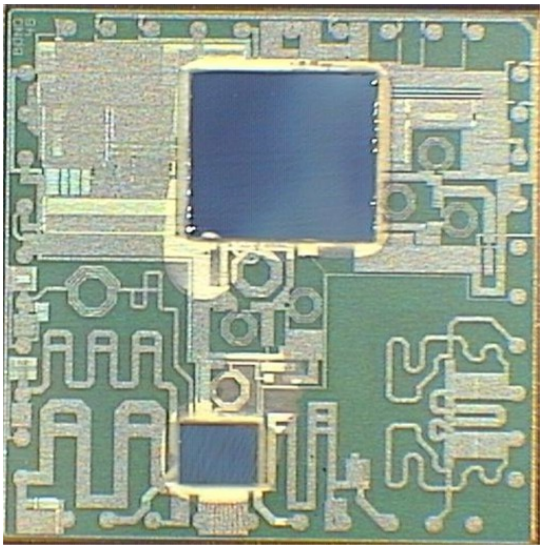

Figure 1-9: Example of SiP made of two active dies stacked on a passive one

Both SoC and SiP have advantages and drawbacks [wils05] [paill05] [cauv07]. Table 1-3 gives the pro's and con's for both technologies.

	For	Against
SiP	Each functional die can be fabricated in his most suited technology	SiP technology uses some complex assembly processes that could reduce reliability
	Possible plug-and-play approach, for example considering an RF application system made of RF analogue mixed signal and digital dies, different RF designs can be done for different applications, without changing the baseband chip	
	SiP can be more compact thanks to high-q passive components and antenna integration.	
	SiP design is shorter	
SoC	Reliability not influenced by several complex assembly processes.	A SOC that contains 10 RF interfaces would be very sensitive to crosstalk between inputs and to noise from digital baseband
	SoC fabrication is less expensive	It's going to be very difficult to embed in one chip all the future applications that would required in future systems, like future cell phones.
	Suitable for mass production	Increased design and test time.
	RF design are migrating from BiCMOS to CMOS as digital, it's going to be possible to propose a single chip solution	

Table 1-3: For and against SiP and SoC

To summarize, the relatively short time to develop SiP devices makes the technology more appealing for consumer electronics that have short production cycles, and SiP is also growing fast in markets for WLAN, WiMAX, Bluetooth and Wi-Fi modules. Basically, SoC approach forces the supplier to a fixed solution for a long run, or for big volumes. An effective solution considering practical performances and cost could be to associate SiP and SoC, embedding SoC and other chips (saw filters, MEMS, power amplifiers, passive components) in a SiP [paill05] [cauv07].

System integration is challenging the edge of integrated systems and consequently affects the test. Indeed over last few years, test cost has been on the rise and nowadays constitutes a significant portion (up to 40%) of the total manufacturing cost for wireless products [bhat05]. As already seen, the trend is to integrate more and more applications and particularly RF applications. In parallel, the size and the price of these systems decrease. As a consequence test is driven by a constant trade-off between product test cost and test effectiveness. Increasing device complexity in terms of transistors count, frequencies, power consumption, and integration of diverse circuit types will pose significant challenges to the test community in the future.

I.3 **Test issues**

I.3.A Analogue test strategy issue

As digital components were growing up, the digital test strategy has been adapted. The first step was to define fault models such as stuck-at fault, in order to move test from a functional to a structural methodology. It consists of testing the structure of the digital component without taking into account the function emulated by the component. This structural test methodology permits to test a whole digital component embedding several functions using one test strategy. In addition to this translation from functional to structural methodology, the test development process benefits from automation. Indeed digital test synthesis and design for testability (DfT) tools have been developed to simplify the test development and optimize the test coverage. The digital test methodology follows the systems development trends.

In comparison to digital, mixed-signal and analogue test strategy is totally different [ozev04]. Actually, there is no efficient and simple fault model and no possible structural strategy. Consequently, the test methodology is not unique, and each core is tested independently using the results of a set of parametric measurements [DYNA00][Maho87][IEEE1241]. This strategy may be considered as a legacy, because, until recently, all the cores of a system were used as stand-alone components. This strategy is no longer efficient, because of the restricted access to embedded cores. Even if there were enough access points, the test of the whole system would be very expensive. Indeed it would require a long test time because each core should be tested independently.

I.3.B Test platform issues

Equipment cost, for a long time, dominates product test cost [ITRT03]. The trend towards more system functionality on a single die (SoC) or in a single package (SiP) brings closer digital, analogue, RF/microwave and mixed-signal devices. Ideally, a single platform solution that can test any application should be used. In real life, the number of instruments in a given test system is limited to the maximum capabilities of the tester, and most importantly by the cost of ownership of such a sophisticated equipment. In addition instrument designs for ATE are chasing ever-increasing test requirements, especially for arbitrary waveform generators (AWG) and digitizers. AWG and digitizers are commonly used to test analogue and mixed-signal components. They require higher linearity and speed than the device under test (DUT) in order to ensure the test quality. As a consequence integrated circuits (IC) suppliers work to produce the best components in term of linearity and speed, and the test platform supplier should have better performances on their analogue instruments, close to one generation in advance. The needs for multiplying the instruments, for improving their performances are expected to continue if no breakthrough is achieved, leading to a contradiction with the permanent pressure on test costs. Examples are usually reported where the test of the analogue cores in the system may represent up to 90% of the whole test effort while these analogue cores only represent 10% of the whole chip area [kerz06]. Three key factors actually affect the costs of the analogue cores testing:

1. The time for development: because the tests cannot be simulated in advance, the time for debug is much longer than for digital cores

2. The cost of ownership of the analogue instruments: it includes the price itself, but also the cost of the calibration, and of the maintenance
3. The test time: in general, it is function of the target accuracy, and of the settling of the device

In addition to high cost of analogue options, there are some technology limiters to analogue tests. The bandwidth, the sampling rates of AWGs, the dynamic range for RF applications, the noise floor, and the ability to integrate some digital and analogue instruments.

Multi-site parallel test as well as concurrent test of all analogue functions could be a solution to reduce test time [ITRT03]. It requires multiple instruments with fast parallel execution of DSP test algorithms (FFTs etc). Parallel test has been used for many years to test memory and high volume digital devices but not to test mixed-signal devices, because additional analogue instruments would increase tester cost and reduce the benefits of parallel testing.

I.4 Summary and objectives

Integration is the global trend in system development whatever the purpose. By integration we mean service and hardware integration. Concerning service integration, systems' developments tend to integrate more and more services in one system. The most significant example is the cell phone, which nowadays proposes, not only to be able to make a phone call, but also to take a picture, listen to music, play games, watch the television, access the world wide web and future services that would address healthcare, e-commerce, or positioning (GPS). Concerning hardware integration, complex systems embed several technologies from RF to digital. From an architectural point of view, complex systems' hardware is more and more digitized. Digitization consists mainly in transferring signal processing from RF to digital domain. Driven by the digitisation of the electronic functions, the software-defined radio facilitates the introduction of multiple RF transceivers into the systems. From hardware integration point-of-view, systems' developments tend to integrate in one package the whole system. The trend is indorsed by SiP and SoC technologies. Figure 1-10 shows a simplified block diagram of a potential complex system. It is made of two main digital cores that embed several sub-blocks, and several analogue cores. The converters interface digital with analogue cores or internal cores with I/O pins.

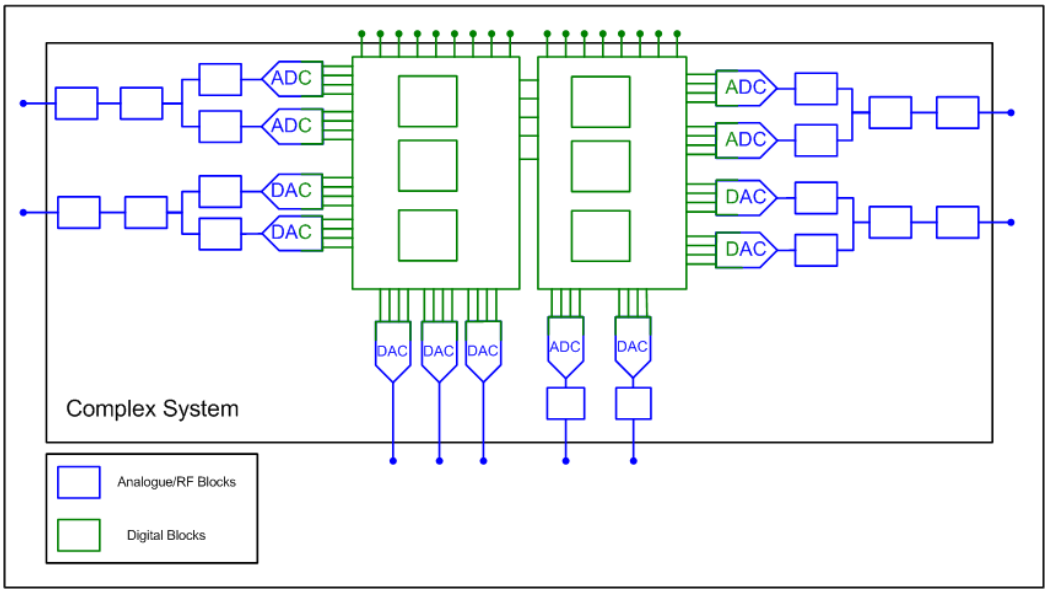

Figure 1-10: Block diagram of a potential system.

These development trends induce some test issues more or less addressed by recent test evolutions. Concerning digital, Figure 1-11 presents the test implementation of digital cores from the previous potential system (Figure 1-10).

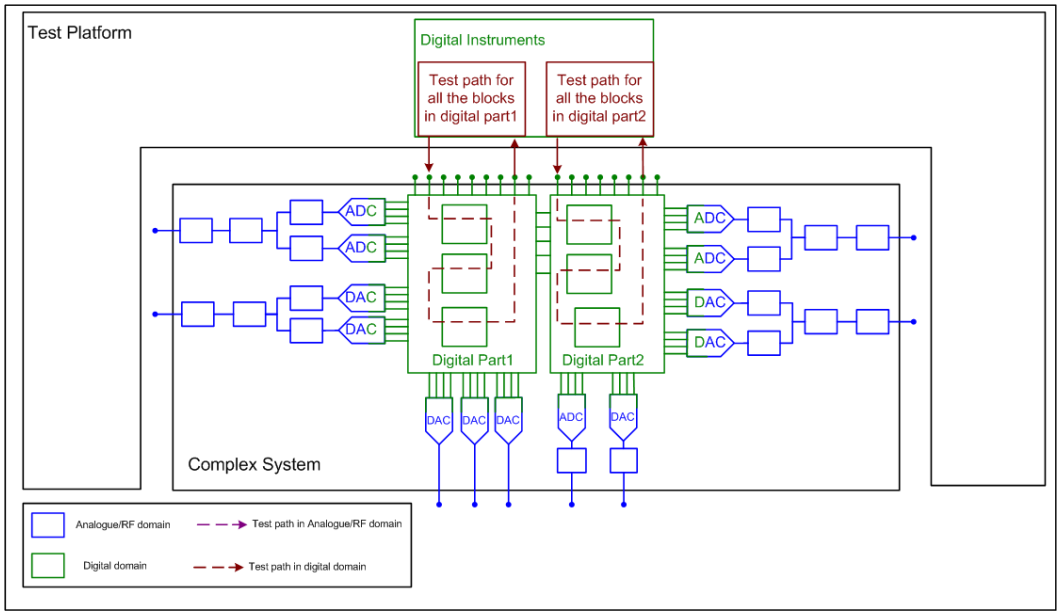

Figure 1-11: Test of digital cores from potential system

Test concepts addressed a global test. Structural test and digital BIST avoid issues like the reduced number of access points and the increasing complexity of digital portions embedded in complex systems.

Concerning RF, analogue and mixed-signal cores of systems, Figure 1-12 gives a non-exhaustive representation of configurations and paths required to test the analogue cores of such a complex system (Figure 1-10)

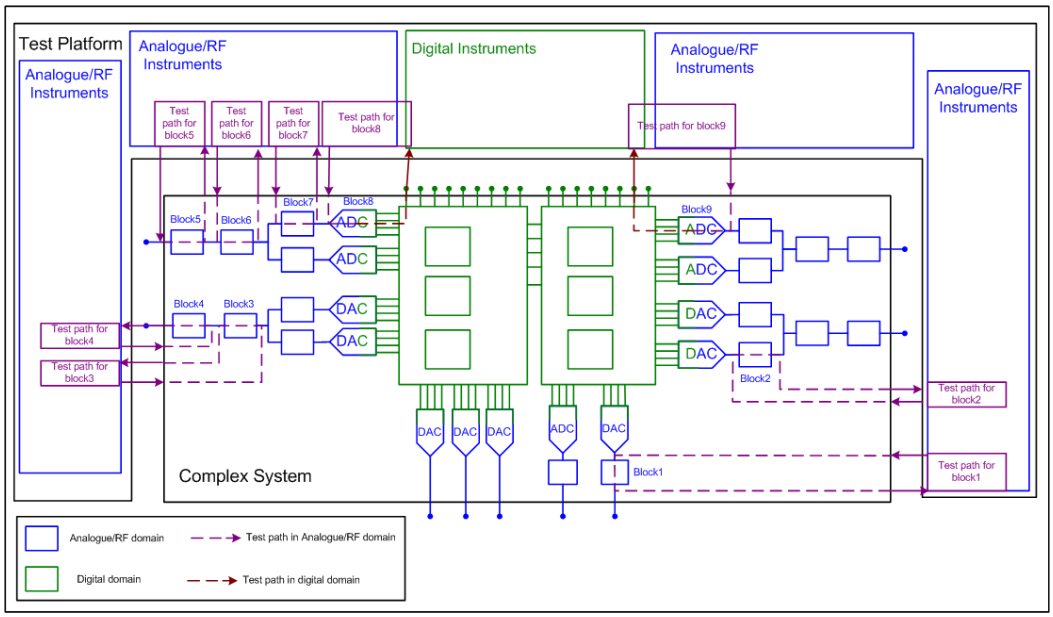

Figure 1-12: Test of analogue cores of a potential system

Test methodologies are not well suited to the issues induced by development trends. Indeed in majority analogue cores are tested independently, requiring the access to primary inputs and outputs. It goes against development trends that consist of more functions on less area and consequently with less access points. And finally it induces a long-test time and as a result high test cost. In addition conventional test methodologies require dedicated analogue test instruments. These instruments are cost-effective by their own, and consequently the ATE, required to test a SoC or a SiP, is expensive because it requires a complex configuration to test all the cores, from RF to digital.

Alternate methods are needed for analogue/RF. Main issues stand in huge numbers of tests, access points and instruments due to the traditional core-level test strategy. A solution could be, like for digital cores, to change the strategy from core to system level. Therefore, two main objectives must be targeted:

1. System-level testing, for reduction of the number of tests and of the access points
2. Low-cost ATE using, in other words, digital-only testers, to get rid of the expensive analogue instruments

The two targets are described in the next section. Figure 1-13 gives an example of test paths for analogue and digital cores, which enable a fully digital test strategy

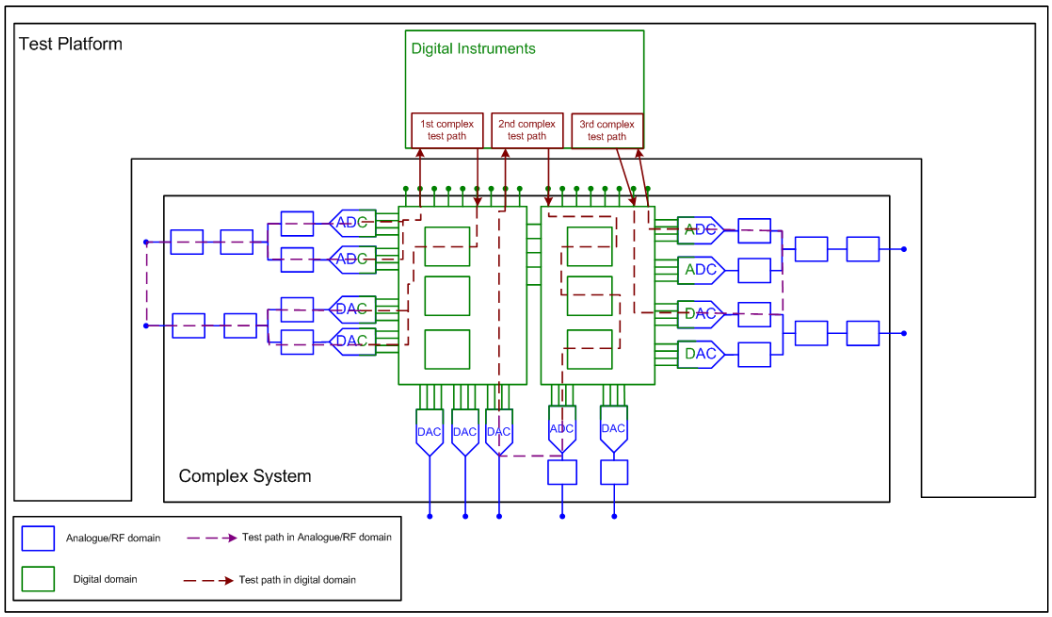

Figure 1-13: Fully digital tests

II State-of-the-art of system-level testing

II.1 Introduction

Testing heterogeneous integrated systems requires test platforms with high-performances (i.e. high cost) instruments, usually dedicated to test each kind of technologies embedded in the system under test. The cost of test operation, directly dependant on the test time, is also significant. Indeed the traditional test approach for analogue/RF systems is based on a per-core strategy. Because of the increasing hardware complexity, the total test time could lead to a prohibitive test cost. Additionally, with the new integration technologies like SiP or SoC the number of test points becomes insufficient.

Considering all these issues, an obvious solution is to develop the test strategy at a system-level and not anymore at core-level. By system-level test, we mean that the device-under-test is not anymore a core but a multi-core system. In this second section, a first system-level test strategy (developed by Ozev et al) is introduced. The third sub-section presents some other test methodologies for system-level testing. Finally, the last sub-section addresses the hardware implementation of system-level test strategy also called path-based testing and loopback. This sub-section also gives some description of alternate methods.

II.2 Signal path in systems to transfer from core-level to system-level testing

A first approach of system-level testing was developed by Ozev et al [ozev01][ozev04]. Their methodology aims at solving some problems induced by systems' developments, namely:

- ✓ The lack of test automation concerning the analogue cores
- ✓ The "per-core" strategy
- ✓ The limited number of test points in complex systems

To address all these crucial issues Ozev et al propose to transfer core-level tests to system-level using existing functional signal paths, in several steps. At first, they propose to define the test stimulus characteristics (amplitude, frequency, phase, DC level, noise floor, accuracy) relatively to the test path. The second step consists of classifying core-level tests at the system level. The transfer of the test from core to system level induces a new test path. As a consequence the tests are classified in three categories relatively to the characteristics of the new test path:

- ✓ Untranslatable due to amplitude and frequency range deficiency
- ✓ Untranslatable due to noise or inadequate accuracy
- ✓ Directly translatable tests

The classification is achieved according to the availability of a test stimulus from one core to be driven through the other cores. Using this transfer scheme allows to improve the automation of test development for analogue cores and for system.

The first experimental validation has been achieved on a quite basic system, only made of analogue cores: a typical two-channel up-conversion path shown in Figure 1-14.

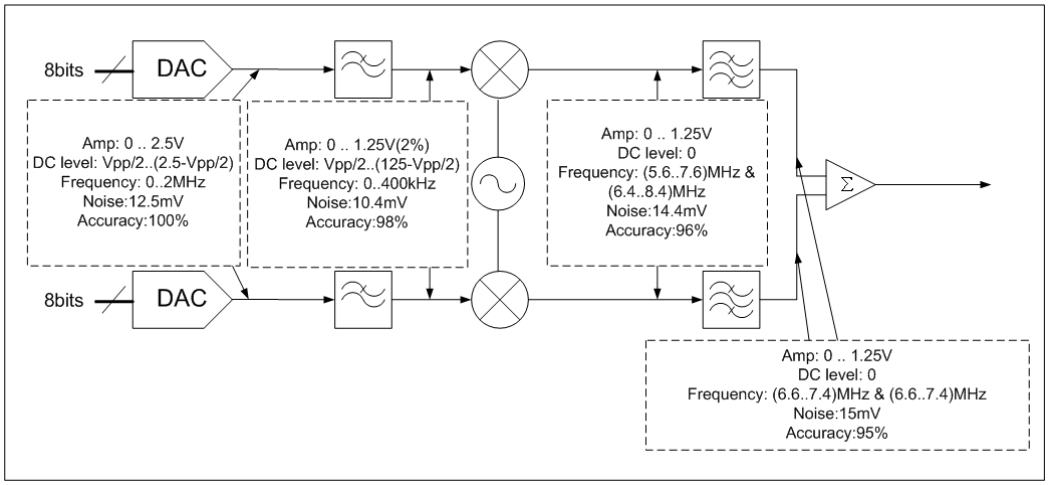

Figure 1-14: Mixed-signal up-conversion path

Fifteen over twenty-two tests have been transferred from core-level to system-level. In addition good fault coverage has been obtained.

The first experimental validation address only analogue cores. As already mentioned, complex systems embed not only analogue and RF cores, but also digital elements. To go further in their approach, Ozev et al [ozev04] present a seamless test of digital components in mixed-signal paths. This approach goes further in the path-based test developments. Indeed they include a digital filter in the path under test, usually made of analogue cores. Digital elements are tested targeting stuck-at fault default. It obviates the need of test point for internal cores. It also permits at-speed test. A two-tone sine wave is used to test the digital filter. The tones of the two-tone sine wave are chosen close together. Indeed as presented in Figure 1-15, the closer are the tones, the greater variety of patterns you have.

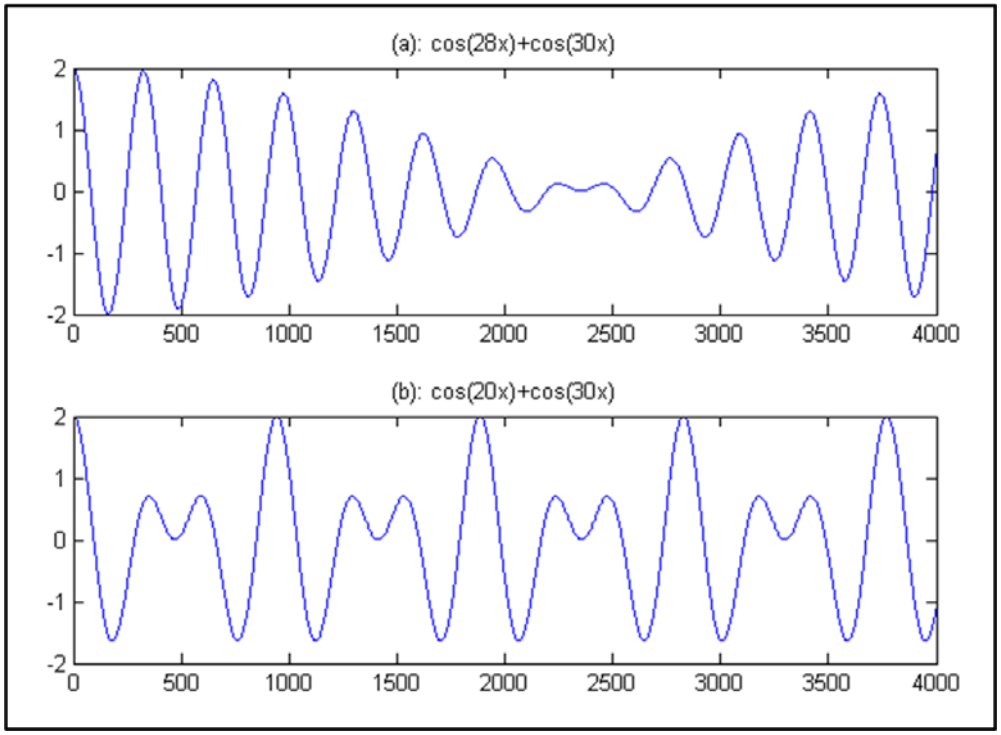

Figure 1-15: Two examples of two-tone sine waves

Ozev et al [ozev01] [ozev04] propose an interesting methodology to move from core-level to system-level testing, in order to carry out a path-based test. This methodology is very interesting because it requires no test access point. As a consequence the test is applied at the primary inputs and captured at the primary outputs. The limited observability and controllability have some drawbacks. At first some key tests, like DNL of DAC in the example of [ozev01] cannot be performed and logged because of frequency or amplitude deficiency. Moreover, the test coverage is actually linked to the noise level of the whole path. In [ozev04], the authors show how the noise level can affect the test coverage in an example. To go further the path-based test methodology also developed by Ozev et al suffer from test masking, but this subject will be addresses in another section. Another drawback, with respect to our initial objectives, is linked to the required test configuration. Indeed, their methods require using at least one RF signal generator (for Rx testing) and one signal analyser (for Tx testing). But obviously the association of analogue and digital cores in the test path appears to be a promising approach that would surely be developed in future works.

II.3 Configurations for system-level testing

II.3.A Introduction

As previously mentioned, systems are becoming more and more complex (cf. Figure 1-8, Figure 1-9, Figure 1-10), with a significant impact on test. A strategy, which could solve all these test issues, would address the whole system in its complexity (digital, analogue and RF cores). Ideally, the resulting configuration would get rid of the RF/analogue options of the tester, in other words would make use of a digital-only ATE.

Ozev et al (cf.I.2.B) have proposed a configuration to address the whole complexity of a system. However, their solution suffers from several drawbacks. For the time being, no methodology exists for testing complex systems with digital, analogue and RF cores all together, although we can find some methodologies in the literature where analogue systems made of several cores are tested as a path. The second sub-section focuses on system-level testing of RF transceivers, as described in the literature. The third section deals with the implementation of such methodologies and some alternate methods using diverse configurations.

II.3.B An example: system-level testing for transceivers

II.3.B.a. System-level testing of transceivers: error-vector-magnitude

IQ modulation (cf. 1.B.b) can be used as RF parametric data. These data are usually displayed on a complex plane. Figure 1-16 gives an example of an IQ complex plan representation and an error vector for a symbol. This vector represents the difference in amplitude and phase between the real and the ideal (reference) vector.

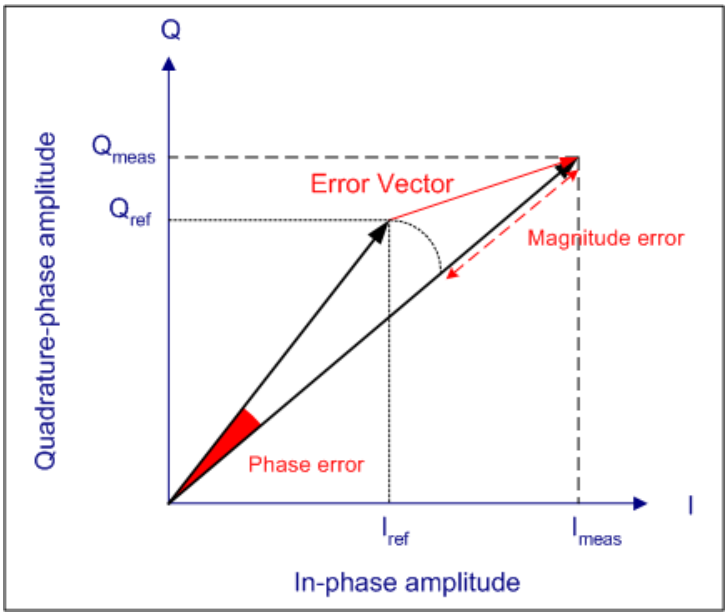

Figure 1-16: Error vector between reference vector and measured vector

Following figures are complex plane representation of IQ sampled data. This representation enables the detection of faults affecting the modulated signal. Indeed for a known signal as a sine wave, the modulated signal captured at the output of the DUT should follow an expected representation, and a particular variation in the constellation can characterize a particular default. Following figures present some measured constellations for faulty and fault-free signals and for several digital modulations.

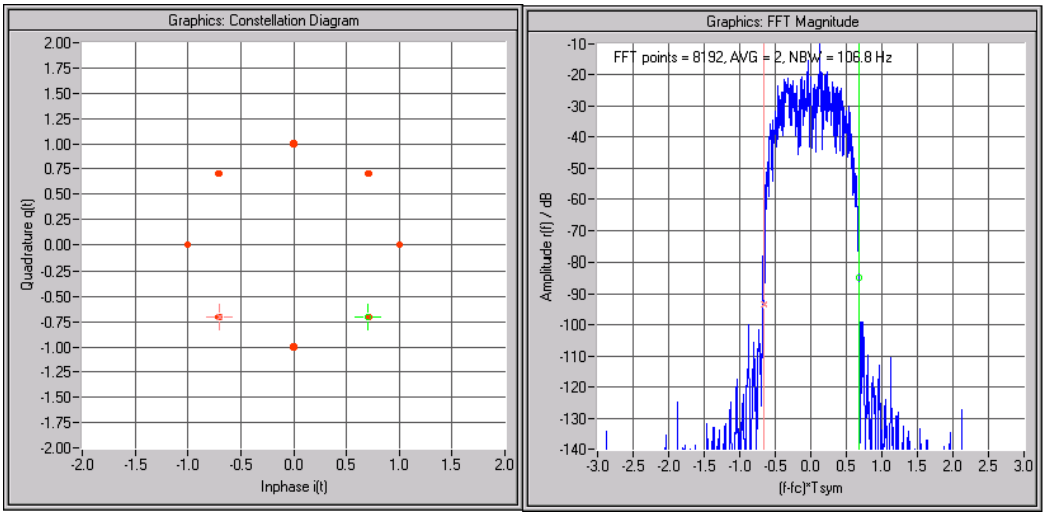

Figure 1-17: Constellation and spectrum of a ⍉/4DQPSK modulated sine wave at 21kHz, no distortion

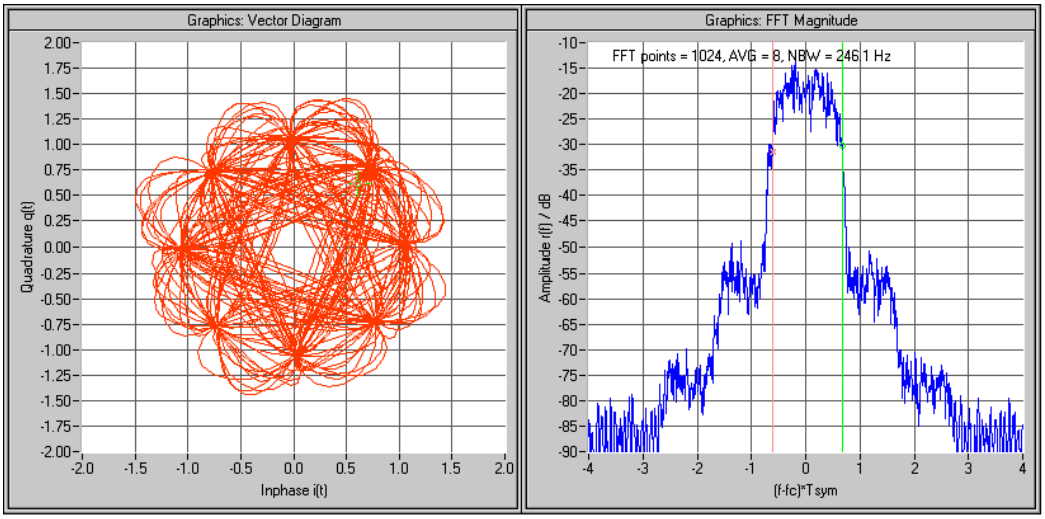

Figure 1-18: Constellation and spectrum of a ⍉/4DQPSK modulated sine wave at 21kHz, with distortion

Figure 1-17 and Figure 1-18 are the IQ plane representation of a sine wave (21kHz) modulated by a ⍉/4DQPSK. For Figure 1-17 the signal is not deteriorated as for Figure 1-18 the signal is deteriorated by some distortions. The difference is visually notable and permits to discriminate a good from a defective device. Figure 1-19 and Figure 1-20 are similar figures but for a different modulation and at a different frequency. Note that the shape of constellation is linked to the type of modulation.

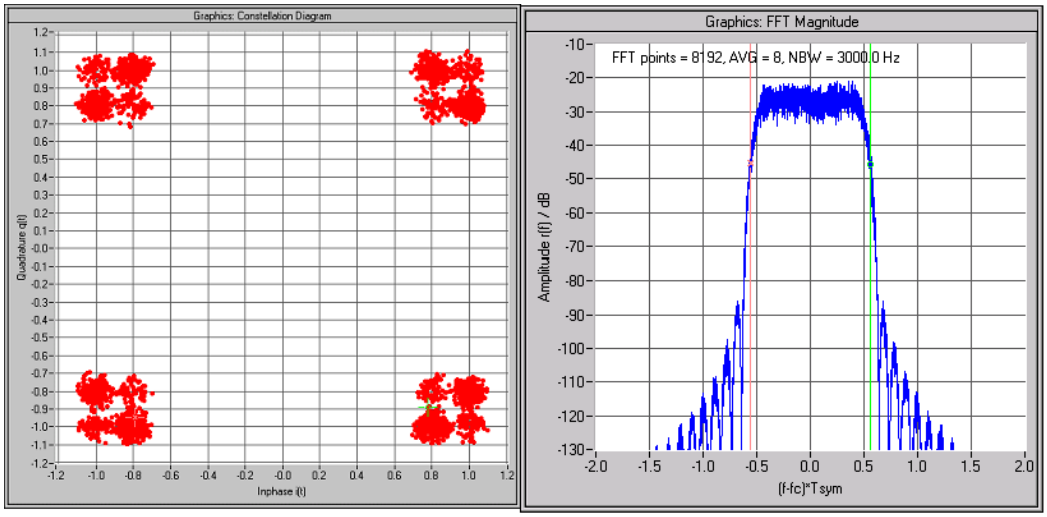

Figure 1-19: Constellation and spectrum of a QPSK modulated sine wave at 4.096MHz, no distortion

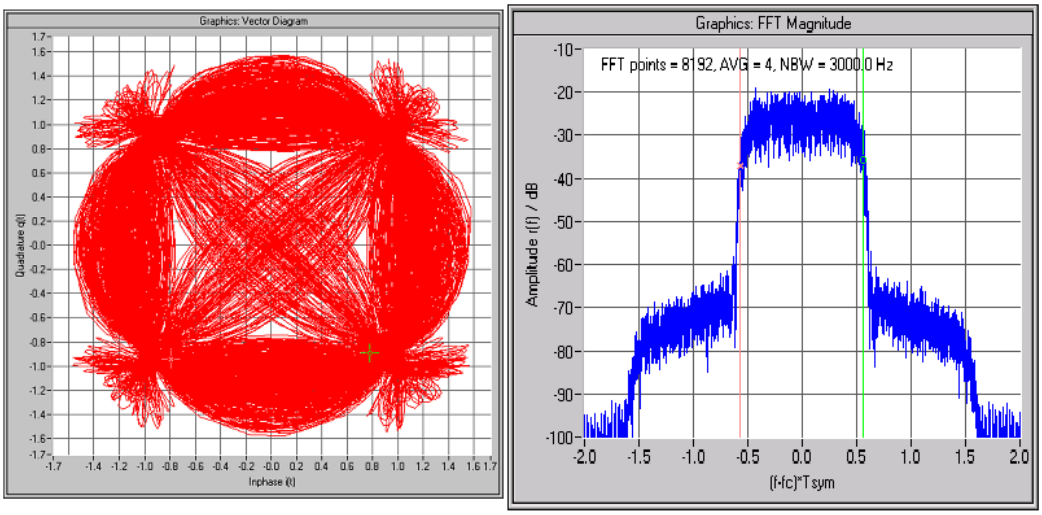

Figure 1-20: Constellation and spectrum of a QPSK modulated sine wave at 4.096MHz, with distortion

The most common parametric test parameter resulting from IQ sampled data is the error-vector-magnitude. The EVM is a specification that determines the performance of the wireless system in terms of transmitted and received symbols corresponding to a digital modulation. The EVM measurement, according to literature, is commonly used for receiver [acar06] [hald05_3] [dabr04] and transmitter testing [acar06] [hald06] [dabr04].

Practically, the EVM calculation is given by eq. 1-2 [hald05_3].

$$EVM = \sqrt{\frac{\frac{1}{N}\sum_{1}^{N}\|R-S\|^2}{\|S_{max}\|^2}} \quad \textbf{eq. 1-2}$$

R= received symbol in vector form (I+jQ),

S= reference symbol in vector form (I+jQ),

S_{max}= outermost symbol in the constellation diagram,

N=number of symbol used for EVM computation.

Dabrowski [dabr04] uses the EVM metric for testing a CDMA transceiver. The efficiency of EVM test is discussed considering the detection of spot defaults that degrade gain and/or NF of the RF cores. In order to improve fault coverage and to address some fault that are not susceptible to EVM, Dabrowski proposes to complete the test set by an IP3 test.

In [acar06] it is demonstrated that EVM testing alone cannot provide sufficiently high fault coverage. Taking this issue into account, the authors propose an input stimulus and a test limit optimisation, based on the detection capability, the set-up complexity and the test time of each test. They finally recommend combining EVM and a set of system level specifications to ensure product quality. With respect to the stimuli, they propose to reduce the number of symbols from 320, the IEEE standard recommendation, to 20. The method is based on a learning technique. The 320 symbols are applied to a set of DUTs, and then the redundant symbols are removed, leading to a significantly shortened test time (in their example, from 1.3ms to 80µs). The test results are also improved using complementary tests, such as Z_{in} and Z_{out}, instead of IIP3 or noise figure that are considered to be too costly and time-consuming tests.

Another optimized EVM test is presented in [hald05_3]. Halder et al focus on test implementation cost. For a path-based test of an RF receiver, the ATE must embed an RF transmitter with the appropriate digital modulation capability and higher performance and accuracy than the receiver under test. To get rid of such an expensive configuration, Halder et al propose to use a low cost RF generator and to set the EVM test using a multi-tone sine wave as test signal. To improve the efficiency of a test using a low performance set-up, a learning process is necessary. This learning process consists in applying the "full" test and the simplified test on a set of DUTs and to calculate a non-linear regression between the two set of results. In production, the regression functions are used to predict the performances of the DUT using the results of the simplified test. A similar methodology has been proposed [hald06] to test RF transmitter.

II.3.B.b. System-level testing of transceivers: Bit-error-rate

At system level, the quality of the modulation of a receiver or a transmitter can also be estimated using the bit-error-rate (BER) parameter [bhat05] [dabr04] [nowa01]. BER is a system specification that measures the erroneous bits received for a fixed number of bits transmitted. Next equation gives the expression of the BER calculation.

$$BER = \frac{N_e}{N_{Tx}} \qquad \textbf{eq. 1-3}$$

where N_e is the number of error bits and N_{tx} the number of bits transmitted.

This parameter is sensitive to jitter and distortion. It quantifies the ability of the system to receive error-free data, and reflects the quality of the communication medium.

A major drawback of BER test is often the huge number of samples to be acquired to get the target accuracy. Bhattacharya et al [bhat05] propose a method to reduce the number of symbol required to achieve a BER test. The algorithm selectively rotates the transmitted symbols to increase the BER. Using some simulation models of the transceiver, and some non-linear regression functions, the true BER can be estimated thanks to the alternate BER test, in a short test time.

Dabrowski [dabr05] focuses on fault masking risks resulting from BER technique. As a consequence some physical defects can be more difficult to detect. To overcome this issue Dabrowski proposes to increase the sensitivity of the signal path under BER test, by controlling the SNR at the input or by using a baseband interferer.

II.3.B.c. Hardware implementation of system-level testing of transceivers: path-based

The two previous sub-sections introduce various methodologies that can be used to develop a test strategy at system-level. These different tests are based on two types of hardware implementation: the path-based and the loopback-based ones.

The path-based implementation deals with the whole chain of the receiver or the transmitter under test. It uses the primary inputs to feed the stimulus and the primary outputs to capture the response. This test implementation is shown in a number of publications [acar06][hald05_2][hald05_03][hald06][ozev01][ozev04]. As a key advantage, this approach does require neither internal access nor specific DfT (Design-for-Test). However, RF instruments are necessary, such as signal generators for receivers, and down-converters coupled to digitizers for transmitters.

II.3.B.d. Hardware implementation of system-level testing for transceivers: Loopback-based implementation

Loopback-based implementation is the extension of the path-based strategy for transceivers. As shown in Figure 1-21, the receiver is connected to the transmitter; creating the loop in the transceiver. This hardware implementation of the system-level testing is depicted in many publications [bhat04] [bhat05] [bhat06] [dabr03] [dabr04] [dabr05] [hald05] [heut99] [jarw95] [lupe03] [negr02] [negr06].

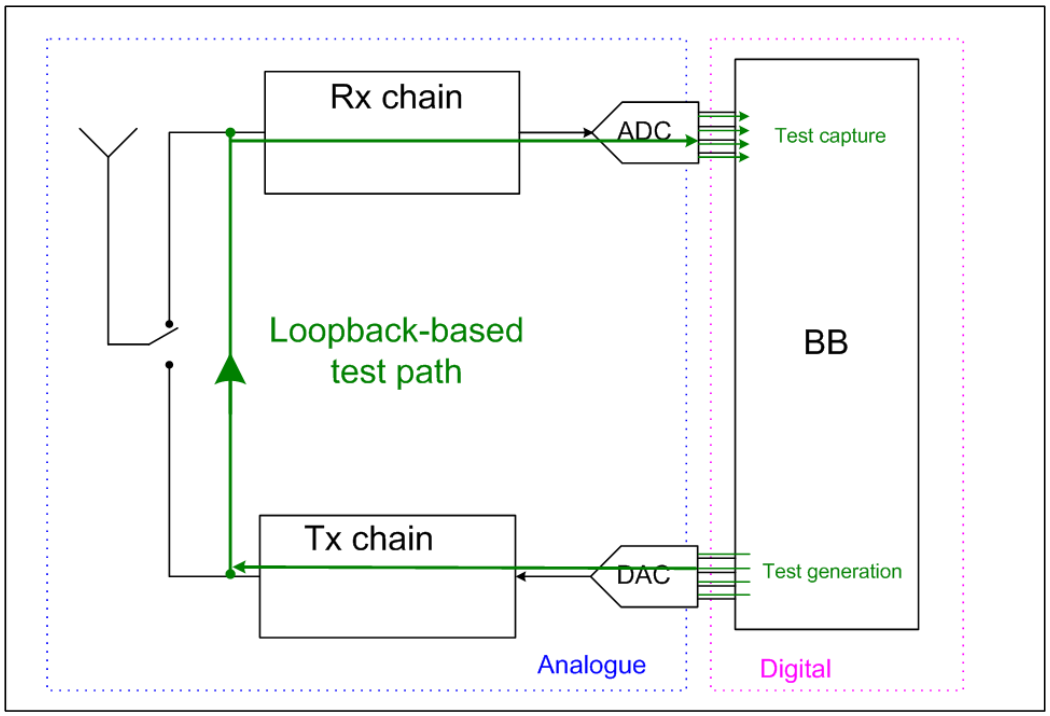

Figure 1-21: Basic principle of loopback-based test implementation

The biggest advantage of using such a test path is the reduction of the test instrumentation. Only digital channels are required because the test signal is generated on-chip or on-board, then converted by the embedded DAC(s). The response signal is converted by the embedded ADC(s) and is either internally or externally processed. Therefore, no high-end RF instruments are required, in other terms, a low-cost tester may be used for even complex transceivers.

Several authors have covered the loopback topic from a hardware perspective. Connecting the Tx to the Rx close to the antenna is not straightforward. Indeed, signals generated by the Tx and entering in a Rx have different frequencies and amplitudes in the application context.

Yoon and Eisenstadt have designed a loopback for 5-GHz WLAN transceiver [yoon05]. The proposed approach explores the on-chip implementation of the loopback. The following figure gives the core diagram the configuration.

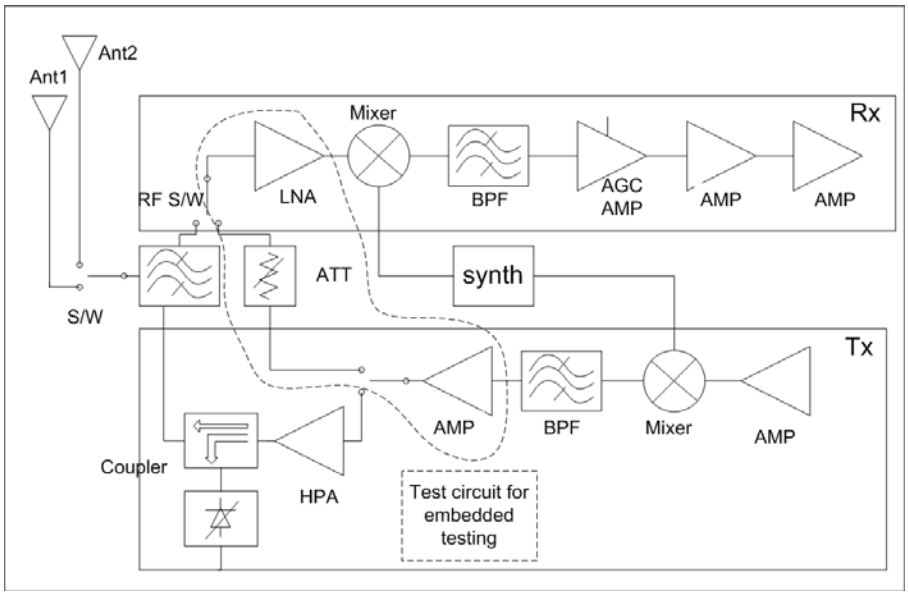

Figure 1-22: Core diagram of a loopback implementation for WLAN transceiver [yoon05]

Due to on-chip implementation of the loopback, the band-pass filter, close to the antenna, and the high power amplifier in the transmission path are removed for testing. In this application, there is no need for frequency shifting. Therefore, the loopback subcircuits are high-frequency attenuators, which reduce the transmitted signal to sufficiently low signal amplitudes, and RF switches that select the test path operation or normal operation signal path.

The purpose of [yoon05] is to design and evaluate a loopback, taking some performance and surface constraints into consideration. Several types of attenuator and RF switches are counted.

Attenuator types	RF switch types
MOS-active	CMOS
PIN-diode	GaAs
Ferrimagnetic	MEMS
Thick-film	PIN-diode
Coaxial-line	ferrite
Resistor-based	

Table 1-4: Available technologies for attenuators and switches

The resistor-based attenuator was chosen, because it is the most suitable for embedding a loopback in a radio frequency integrated circuit. It has wideband circuit operation and a compact implementation. Two types of resistor-based attenuators were considered: T-type and ⦸-type (Figure 1-23).

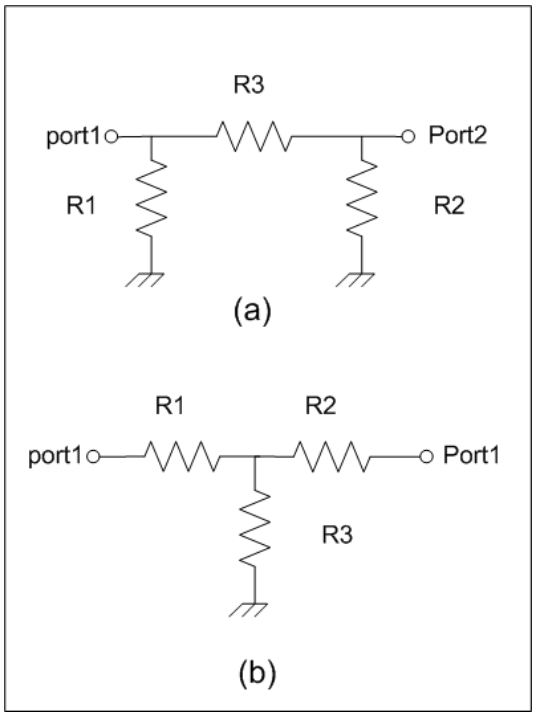

Figure 1-23: Implementation of a resistor-based attenuator [yoon05] a) Ω-attenuator b) T-attenuator

In this paper, RF switches were designed in BiCMOS RF switches. This solution, associating RF switches and attenuators, gives an attenuation of 30dB at 5 GHz. More attenuation is expected using two attenuators in series. But proper isolation during loopback test is a relevant challenge that is mentioned in this paper and should be addressed to permit efficient tests. A significant advantage of such a solution is the small overhead required, only 300*300µm, being cost and yield effective.

Similar loopback methodologies are proposed by Dabrowsky and Bayon, of the university of Linköping, Sweden [dabr03] [dabr04] [dabr05]. The transceiver presented in [dabr03] (cf. Figure 1-24) integrates a test amplifier powered on in test mode. As for Yoon loopback, it removes a power amplifier and the RF circuitry near antenna from the test path. The local oscillator in test mode supports Tx to operate at the carrier frequency of Rx.

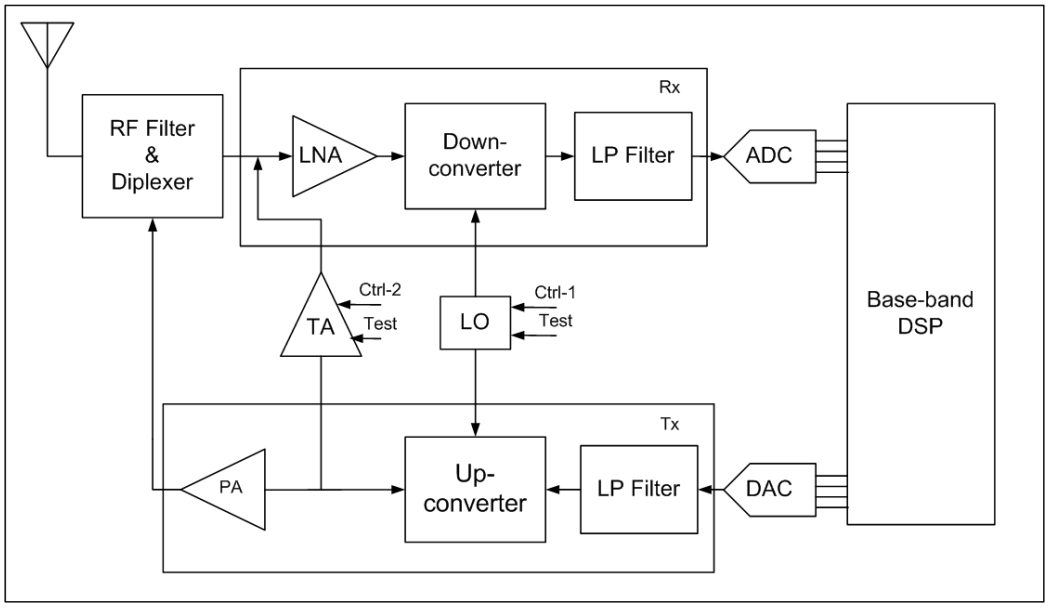

Figure 1-24: Loopback principle with different frequencies for Tx and Rx [dabr03]

Another transceiver architecture is presented in [dabr04] [dabr05] Figure 1-25. In these publications they consider a transceiver architecture for which Rx and Tx operate at the same carrier frequency, like CDMA systems.

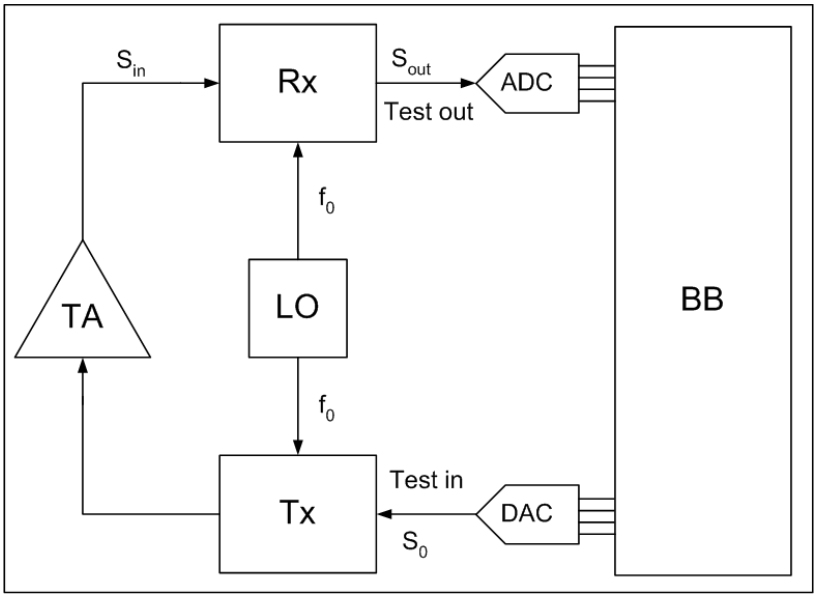

Figure 1-25: Loopback principle with Tx and Rx operating at the same carrier frequency [dabr04]

For that reason, there is no need anymore to adapt the local oscillator to a test mode. The loopback is presented as a test attenuator, as in Yoon's solution, and some design considerations are presented.

When Rx and Tx are working at different frequencies, two solutions can be considered.

The first has been previously described, and corresponds to [dabr03] solution. This first solution consists in designing a local oscillator that could make Tx working at the same frequency as Rx.

In [dabr05] another solution is proposed, also described in [srin06] [hald05] [heut99] [jarw95]. All the signal adaptations are included in the loopback, both signal amplitude and signal frequency. Rx and Tx paths do not need to be modified in test mode; therefore, they can be tested at their functional carrier frequencies.

This solution was introduced by [jarw95]. The implementation is also described in publications of Chatterjee et al. The loopbacks presented in [srin06] (Figure 1-26) [hald05] (Figure 1-27) are designed to attenuate the signal from Tx to Rx, and in addition to shift the frequency. The frequency shift is operated using a mixer and an oscillator. This oscillator is also introduced in [lupe03]. The significant number of additional cores necessary to implement this loopback requires some silicon overhead. As a consequence the loopback presented by Chatterjee et al should be implemented off-chip, on test board.

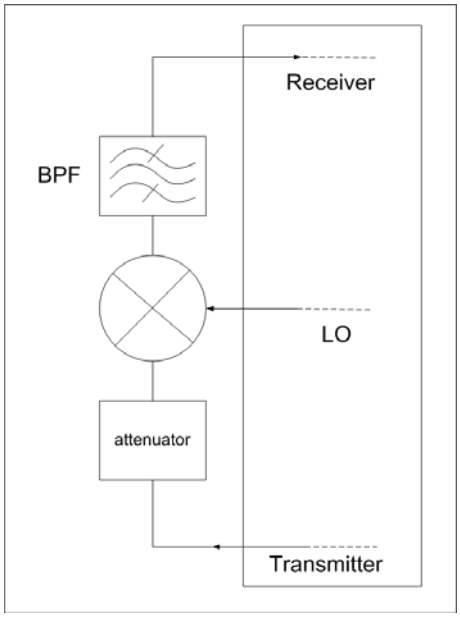

Figure 1-26: Loopback circuitry, as proposed by [srin06]

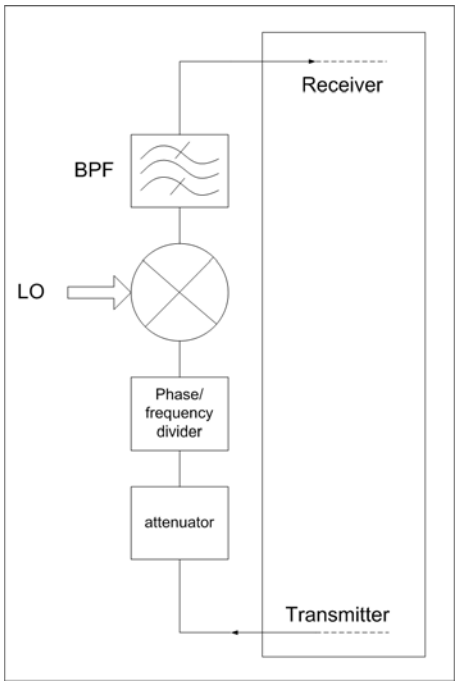

Figure 1-27: Loopback circuitry, as proposed by [hald05]

To summarize, the transceiver architecture must be investigated prior to the implementation of the loopback. In an application such as WLAN, the Rx and Tx work at the same carrier frequency. As a consequence the loopback can be implemented using only an attenuator. This case is covered by [dabr03], where the attenuator is used to adapt the signal coming from Tx to Rx.

But such architecture, with Tx and Rx working at the same carrier frequency is not a common architecture. Indeed many types of architecture use different carrier frequencies for Tx and Rx, to limit interferences between Rx and Tx paths. In such cases, a simple loopback using only an attenuator cannot be used. The first solution consists in modifying the LO to run at the same carrier frequency for both paths in test mode. However, in this solution, Tx is tested at a different frequency from its functional one. In addition the design of Tx is suited to work at its frequency and not to Rx frequency. And a big effort must be made to adapt the design of the local oscillator. The second solution adapts the signal sourced by Tx before it goes into Rx. The signal adaptation consists of amplitude attenuation and frequency shift in the loop. The loopback implementation is preferably made on board, to avoid too much silicon overhead. Although this solution is very attractive, some precautions must be taken, especially to guarantee a high reliability and a high signals integrity.

II.3.B.e. Alternate methods

As previously described path-based and loopback-based test methodologies are possible solutions to overcome some common issues affecting system testing, in particular the lack of observability and controllability of tested cores. Given that the strategy moves from a per-core to a system approach, the tested parameters are mainly describing system specifications and not anymore core specifications.

Despite of this new strategy, there are still some observability and controllability issues, or more precisely there are some problems to stimulate or observe some errors. Indeed due to complex test paths some errors can be masked or compensated by the

system. This masked fault issue is a common study topic considered in literature publications dealing with path-based and loopback-based test methodology [dabr04] [ozev04] [lupe03] [negr06].

For instance, the path-based methodology proposed in [ozev04] to test a receiver suffers from error masking. The noise level of the DUT affects indeed the fault coverage. For a SNR of 74dB their test methodology reaches a very good 93% fault coverage. But for a 60dB SNR the test coverage is reduced to 80%.

[dabr04] addresses the masked-faults issue. The mathematical expression given by eq. 1-4 must be verified in order to avoid fault masking

$$\left|\mu_f - \mu_0\right| \geq 3\left(\sigma_0 + \sigma_f\right) \qquad \textbf{eq. 1-4}$$

where σ_f is the variance of a faulty circuit, and σ_0 is the variance of a fault-free circuit. . If the difference μ_f-μ_0 (test results average of faulty and fault-free circuits) is not large enough, the likelihood of getting test escapes and yield losses will be high, as illustrated in Figure 1-28.

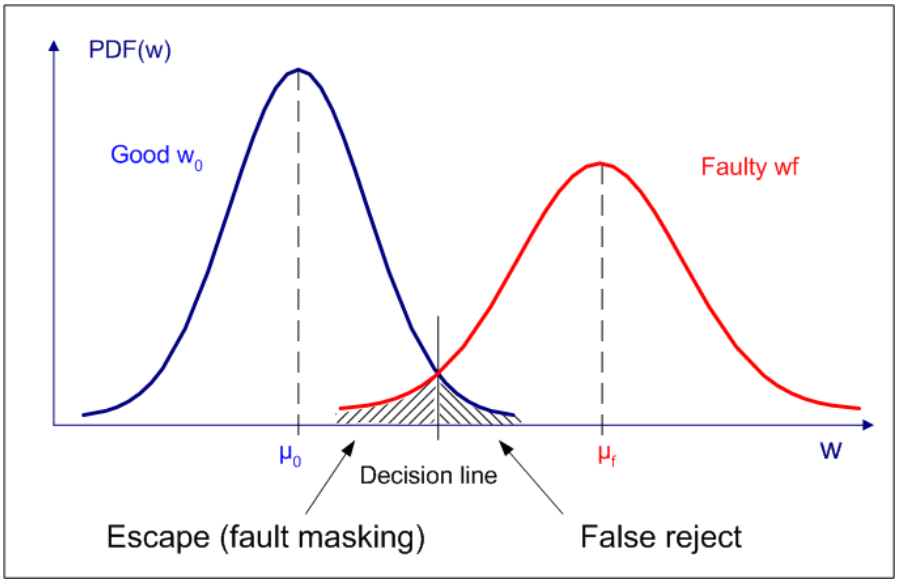

Figure 1-28: Test response PDF [dabr04]

Dabrowski proposes to predict the risk of fault masking. This prediction method is based on a behavioural BIST model and discusses the problem in terms of statistical parameters supported by sensitivity analysis.

The masking phenomenon that affects fault detection is mainly due to complex test path and the reduced observability and controllability of RF cores. An alternative to strictly loopback-based test has been published [negr06] [bhat04]. The new approach uses additional DfT resources such as sensors [bhat04] [bhat06] or statistical samplers [negr06] [negr02] to realize some measurements at several points in the RF chain.

Bhattacharya et al technique includes some sensors in the RF chain to increase test coverage. For the sensors, they propose to use detectors that generate DC signals, proportional to specific characteristics of the captured signal. As shown in Figure 1-29, the sensor is made of a bias network, a matching network, and a detection diode.

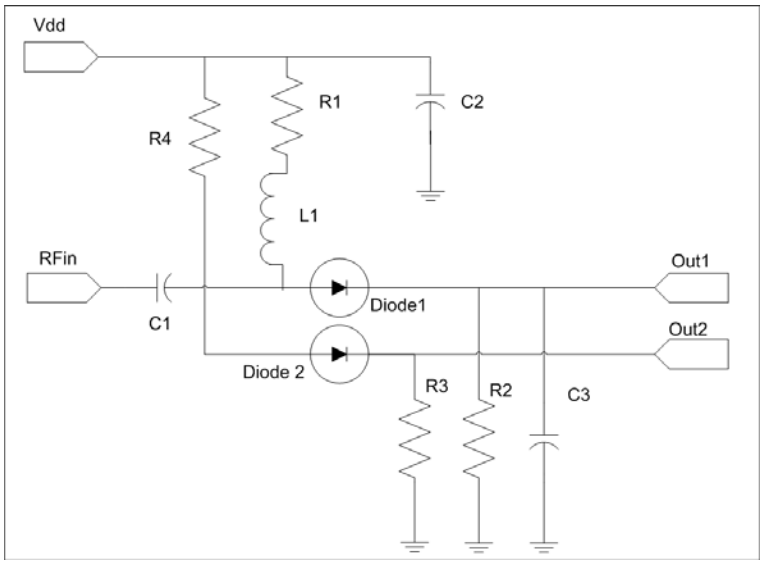

Figure 1-29: Sensors design [bhat06]

The test method, used by Chatterjee et al aims at predicting the specifications using simple measurements. This prediction is available using non-linear regression functions. A number of DUTs are primarily tested under the nominal conditions, i.e. at functional frequencies, and the measurement results are stored for reference. The same devices are tested under low frequency or DC measurements, using the embedded sensors, and a correlation processed to define the test limits. The method was validated on a GSM receiver.

Unfortunately, the sensor measurements are still in the analogue domain. To capture the sensors measurements there is a need to output them to a test platform, or to convert them in the digital domain to transfer the data to the baseband and propose a BIST solution. However, transferring the data to an external test platform requires additional I/O, whereas the initial goal was to reduce them (cf. I). Converting to the digital domain and transferring the data to the baseband for processing might be a costly solution also, because additional DfT resources are necessary to transfer the data from the A/D

Negreiros et al propose a less restrictive solution. As for Bhattacharya solution, they implement a new DfT solution to access critical points in the RF path. The additional DfT is made of a sampler or 1-bit digitizer, as presented by Figure 1-30.

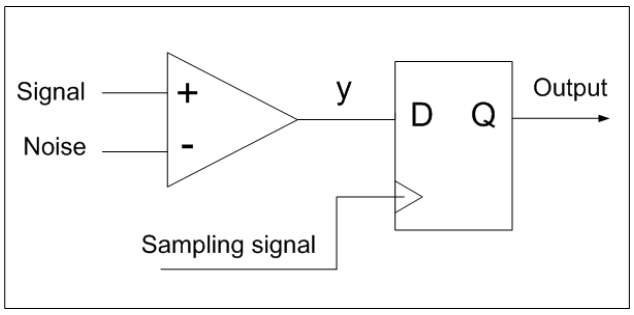

Figure 1-30: 1-bit embedded digitizer

The presented digitizer is made of a comparator connected to the test signal and a noise source. The digitizer permits to monitor spectral characteristics of the tested signal [negr02].

Such a digitizer permits to access critical points in a RF path as shown in Figure 1-31.

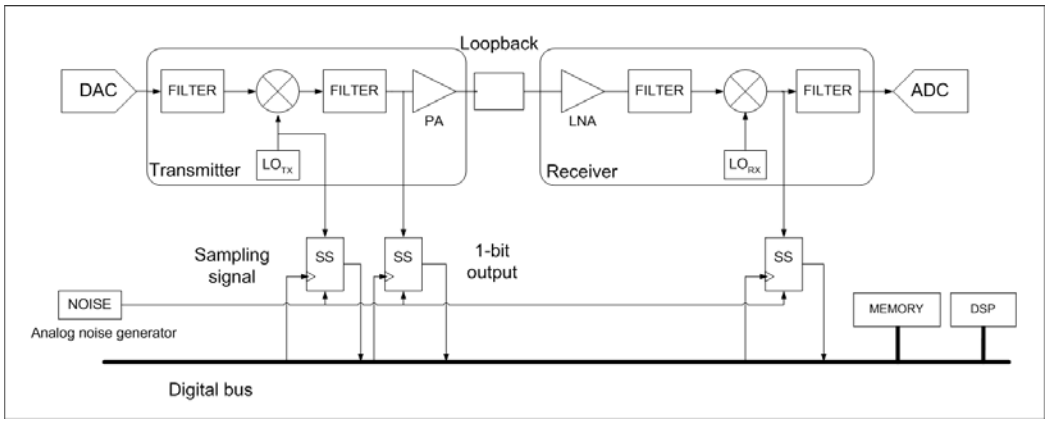

Figure 1-31: Improved loopback structure

Obviously, the digitizers outputs are digital, therefore they can be connected to a data bus. This solution is less restrictive than Bhattacharya's one.

Both teams that propose these similar solutions suggest that their sampler or sensors are permanently connected, and consequently the RF circuit load is constant, and it can be adequately accounted for during the design of the RF stage. This assumption is valid when the frequency remains in a low bandwidth. However, as already mentioned, the frequency range of the applications are constantly increasing with time, it becomes difficult to protect the RF chain from external perturbations. So far, the addition of such DfT resources in multi-gigahertz represents a big challenge.

Another method has been developed to overcome the difficulty of including the sensors in the RF circuitry [ello06]. The basic concept of this method is to predict RF parameters of a transceiver through DC-LF measurements. LF measurements are obtained through a loopback configuration. DC measurements are obtained using conventional measurements (e.g. current consumption) and advanced measurements using simple DC sensors.

This alternate method is based on signature analysis, requiring a learning phase to correlate some RF parameters with DC-LF measurements. The non-linear regression between RF parameters and DC-LF measurements is computed using nonlinear Artificial Neural Networks (ANN).

The method was validated on a 2.4GHz WLAN transceiver. Four RF parameters were estimated: Noise Figure (NF), IIP3, Gain and TXOutput. The parameters prediction seems to be effective in a production configuration, from an accuracy point of view without test time consideration.

Thanks to this method there is no need of expensive RF probing for industrial testing, and no risky DfT implementations, like sensors or samplers. As previously observed with alternate methods [negr06] [bhat06] there is a need of a learning process on a lot of devices to map alternate measurements with test parameters, in order to implement some efficient at-frequency measurements of classical RF

parameters (IIP3, Gain…). This method requires RF instruments more efficient than the DUT, and cannot avoid the need of expensive instruments.

II.4 **Conclusion**

According to literature, the new millennium has bred a new way to hold the test of systems. The test of analogue and RF systems was considered at a core-level, because the systems were made of stand-alone cores that can be quite easily accessed for test. Nowadays the design trend for system is to integrate the whole system (RF + analogue + digital) in one package using SiP or SoC technologies, making the cores less individually observable and controllable. Additionally, the test of very complex systems is increasingly costly, in terms of instrumentation and time consumption. To cope with all these issues, the trend towards a system-level strategy - and not anymore a core-level one-, combined with the high power of the digital techniques, will find many applications in the test of the integrated systems of the future.

Considering these new trends in test development that consists in addressing the test at a system-level, there is only one solution developed to deal with the whole system complexity: digital to RF cores. Ozev et al proposition [ozev01] [ozev06] moves the tests from core-level to system-level. The methodology is interesting because they propose a seamless test with a path that contains analogue and digital cores. But this solution has several drawbacks. As a consequence there is no efficient solution that addresses the test of the whole system complexity. On contrary a lot of work can be found in the literature proposing system-level test solutions for RF transceivers, and these solutions are described in the three previous sub-sections. These methodologies rely on path-based or on loopback-based tests. The first solution address a test path made of a full receiver or transmitter, as the second solution address simultaneously the receiver and transmitter path of a transceiver by connecting them through a loopback near the antenna.

Several university researchers propose various solutions for RF transceiver testing. EVM and BER parameters are able to give an estimation of the quality of the modulation of an RF chain, but need to be completed by some other tests to achieve a sufficient coverage. Dabrowski [dabr04] proposes to complete the test set by an IP3 measurement, or to monitor the SNR. Acar et al propose the Z_{in} and Z_{out} parameters to EVM, and Halder et al use a multi-tone sine wave as test stimuli. Bhattarcharya et al propose to optimize the BER test by selectively rotating the transmitted symbols. All these methods suffer mainly from fault masking due to the complex test path. Dabrowski [dabr04] propose to predict the risk of fault masking. Considering the risk of fault masking Negreiros [negr06] and Bhattacharya [bhat06] insert some samplers or sensors in the RF circuitry. These solutions increase the observability on cores, and the stimulation is still a path-based or loopback-based, but may introduce some disturbances in the RF signal, increasingly with the frequency. Ellouz et al [ello06] propose a solution based on loopback, complemented by some DC-LF measurements in the test path to lower the risk of disturbances. However, the method needs a learning process, which requires high performance instruments, in contradiction with our initial objective.

Published examples of system-level methods address the test of RF transceivers. These tests are dedicated to test analogue cores, and the converters are usually considered as good. For instance Dabrowski [dabr04] assumes that the converters have been tested previously to perform the test of the transceiver. Moreover, there is

no published solution dealing with the whole complexity of the systems. The key elements of the new complex systems are converters, because they interface analogue and digital cores, and their number is growing. Eventually, in a fully digital test of the whole system using signal path like for Ozev solutions or loopback-based methods, the DACs should be used as signal generators and the ADCs as digitizers for the test of the analogue cores, or paths. As a consequence before testing analogue sections using for instance loopback-based methods, or before developing a test solution at system-level, the ADCs and DACs of the system should be tested, and, most likely, calibrated.

Considering the need to test DACs and ADCs in a complex system, the next chapter deals with the test of converters and especially converters embedded in a complex system.

Chapter 2

Fully digital method to test a set of DACs and ADCs embedded in a complex system

I Introduction

As mentioned in chapter 1, ADCs and DACs are key elements of systems because of their growing number and their role of interfacing digital domain with analogue cores and I/O pins. Their errors, their test parameters and their test methods are well known and well defined. They are presented in the second section of this chapter. Usually the test of converters embedded in a system requires a long test time because they are tested independently. In addition, they require high performance (expensive) mixed-signal test instruments, namely one or several arbitrary waveform generators and digitizers. As a consequence, the test cost of converters added to other cores test costs has become a crucial bottleneck for an efficient test. The main cost for converters testing comes from the test platform. Testing in a fully digital way some converters embedded in a system is consequently an attractive solution because it requires a low-cost test platform, but it represents nevertheless a big challenge. The third section presents some alternative methods that do not require analogue test instruments. The fourth section deals with the best approach for a fully digital test of converters embedded in a complex system: re-use of embedded components as test instruments. Finally a novel strategy is proposed in the fifth section, and its associated method is also described.

II Basics of converter testing

II.1 Introduction

Converters are mixed-signal components; indeed, they interface digital and analogue domains. Analogue-to-digital converter or ADC is an electronic circuit, which converts an analogue signal into digital codes within three operations: sampling, quantization and encoding. Figure 2-1 gives a representation of the analogue-to-digital interface.

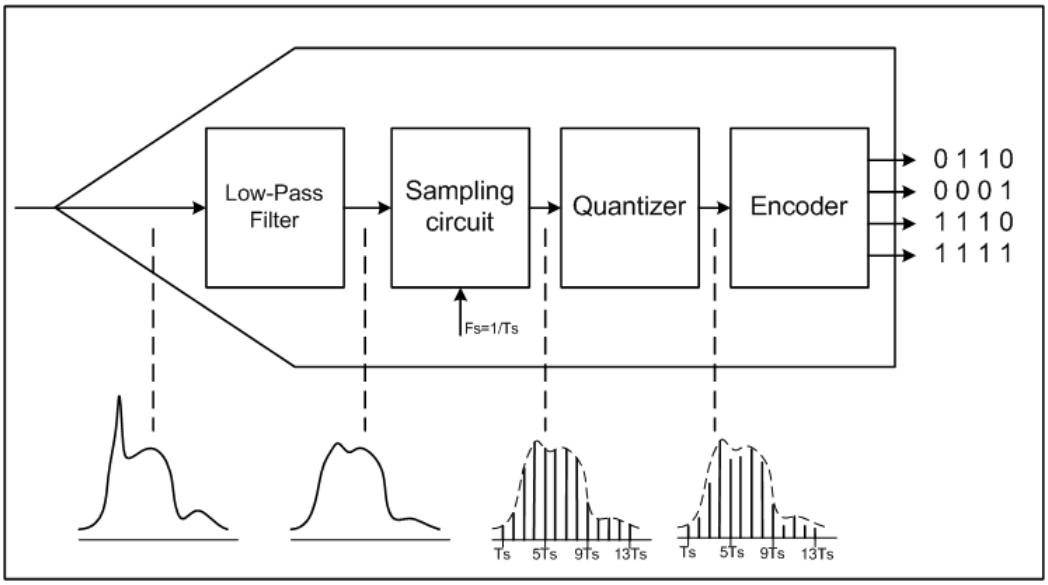

Figure 2-1: Analogue-to-digital conversion

The analogue-to-digital interface converts a continuous-amplitude, continuous-time analogue input signal into a discrete-amplitude, discrete-time digital code. A low-pass

filter limits the input signal bandwidth so that subsequent sampling does not alias any unwanted noise or signal component into the actual signal band. Next, the filter output is sampled so as to produce a discrete-time signal. The amplitude of each sample of this waveform is then "quantized", i.e. approximated to a level from a set of fixed references, thus generating a discrete-amplitude signal. Finally a digital representation of that level is established at the output.

If the digital output is a R-bit binary number, then the digital output corresponding to a sample of the input signal with amplitude V_{in} is given by

$$D = \left[\left(2^R - 1\right) \frac{V_{in}}{V_{ref}} \right] \qquad \textbf{eq. 2-1}$$

where [] denotes the integer part of the argument and V_{ref} is the input signal full-scale voltage.

A digital-to-analogue converter (DAC) must convert a discrete-amplitude, discrete-time signal to a continuous-amplitude, continuous-time output. Figure 2-2 details the interface.

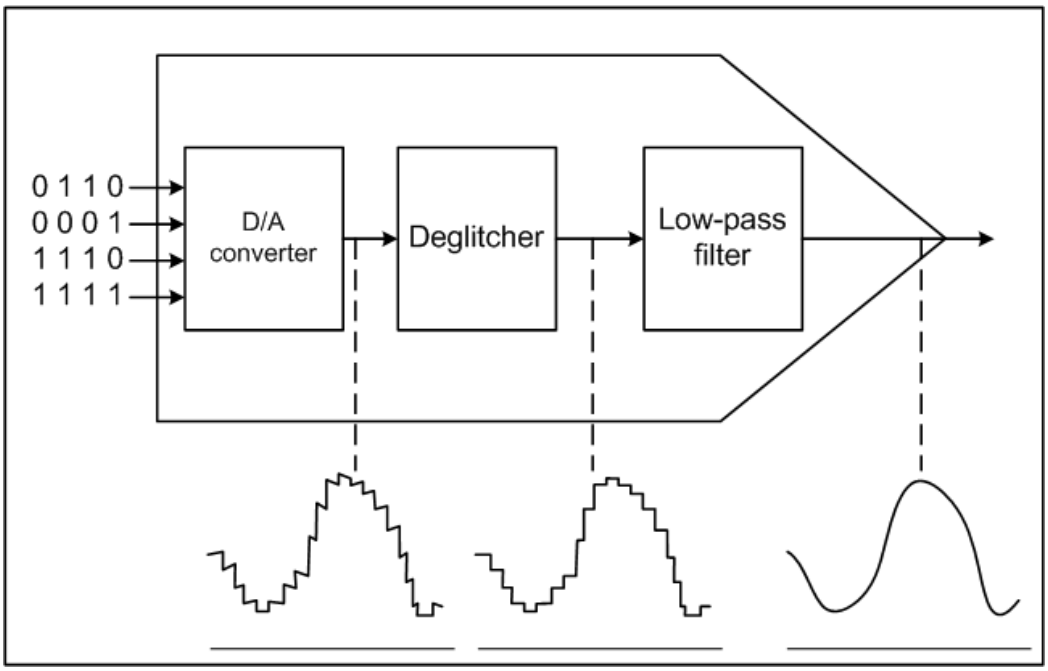

Figure 2-2: Digital-to-analogue conversion

To begin with, a D/A converter produces an analogue level from a set of fixed references according to the digital input code. If the DAC generates large glitches while switching from one level to another, then a deglitching circuit is used to mask the glitches. Finally, since the reconstruction function performed by the DAC introduces sharp edges in the waveform as well as cardinal sine envelope in the frequency domain, a low-pass filter is required to smooth out the signal and suppress these effects.

An ADC and a DAC are both defined by a transfer function. Figure 2-4 presents the transfer functions of both circuits.

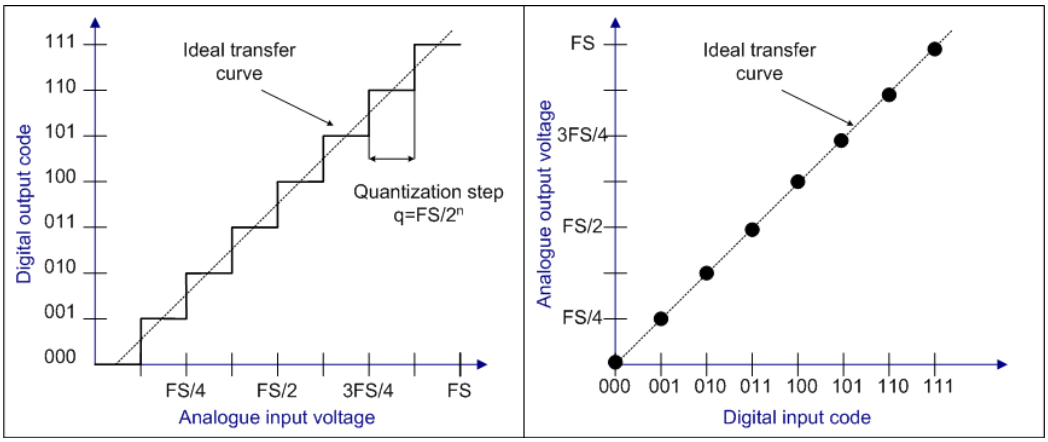

Figure 2-3: Transfer functions of a 3-bit ADC (left) and of a 3-bit DAC (right)

ADCs and DACs are different systems with several potential types of architecture. The architecture is usually chosen according to expected performances and consequently to the type of application. Figure 2-4 gives details about performances for different ADC architectures.

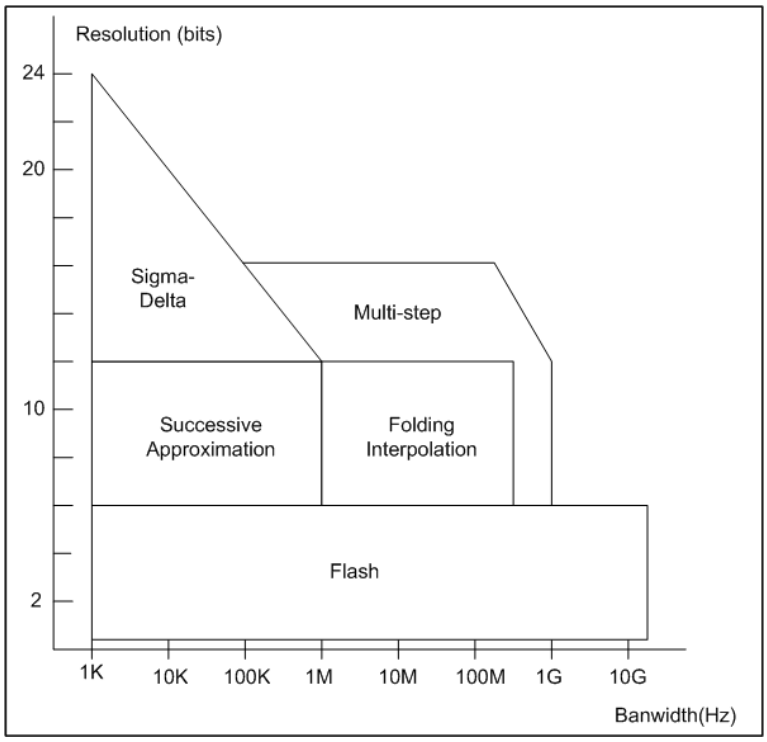

Figure 2-4: Performances of ADC architectures

DACs and ADCs have not only different principles but also different types of architectures. As a consequence, there are different sources of errors for all these types of converters. But from a transfer function point of view, all the converters, DACs and ADCs, are affected by the same kind of errors described in the following section.

II.2 Errors affecting converters

The conversions from analogue to digital of an ADC and from digital to analogue of a DAC are affected by errors. With respect to their transfer functions, we consider that the same types of errors affect ADCs and DACs. As a consequence, only the errors affecting the ADC transfer function will be detailed in this manuscript. These errors are usually split in two categories: deterministic errors and stochastic errors.

II.2.A Deterministic errors

A converter is defined by its transfer function. This mathematical representation gives a relationship between the input and the output of the converter. Figure 2-4 presents the transfer functions of a 3-bit ADC and a 3-bit DAC.

Intrinsically, a DAC and an ADC introduce a deterministic error in the signal because of the quantization operation. This quantization error is the difference between the continuous and the quantized signal. Despite its deterministic nature, this error is improperly called “quantization noise”. Figure 2-5 gives an example of the quantization noise of a sampled sine wave.

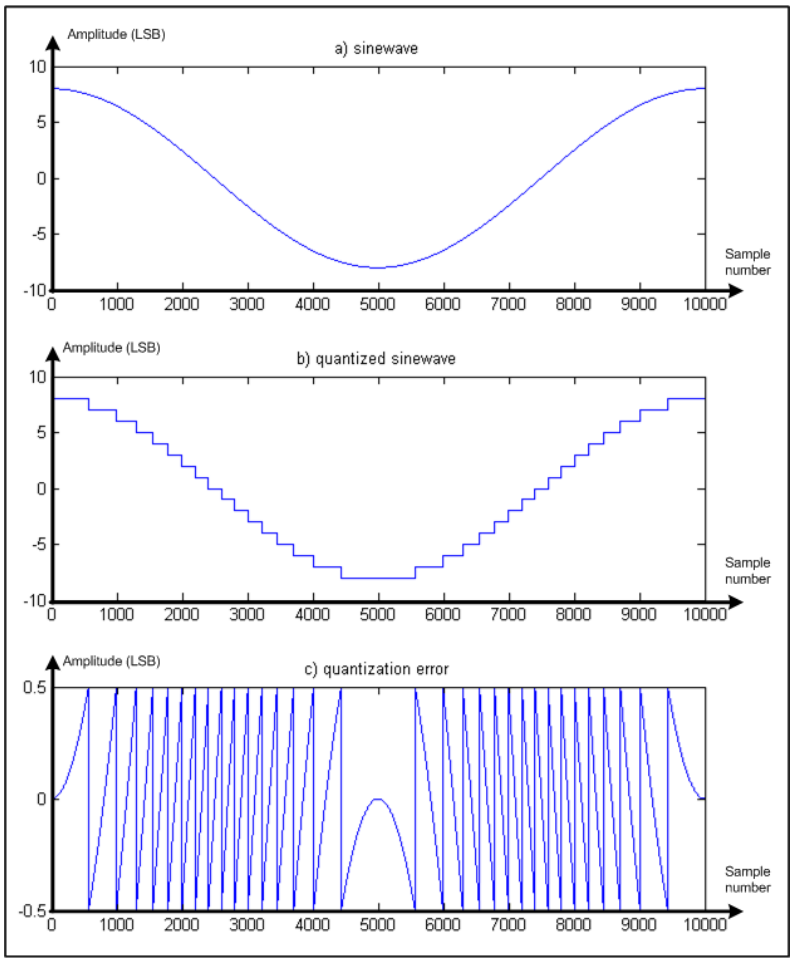

Figure 2-5: Deterministic “quantization noise”: a) continuous sine wave, b) sine wave quantized for conversion, c) quantization error (difference between continuous and quantized sine waves)

The quantization noise can actually be predicted because it is related to the shape of the input signal and the resolution of the converter. The quantization error by its spectral characteristics is close to a white noise. A white noise is characterized by bins of equal amplitudes in the spectral domain. The quantization can be considered as a random variable uniformly distributed in the interval $\left[-\frac{q}{2},\frac{q}{2}\right]$, where q is the quantization step. Its probability density is constant on this interval.

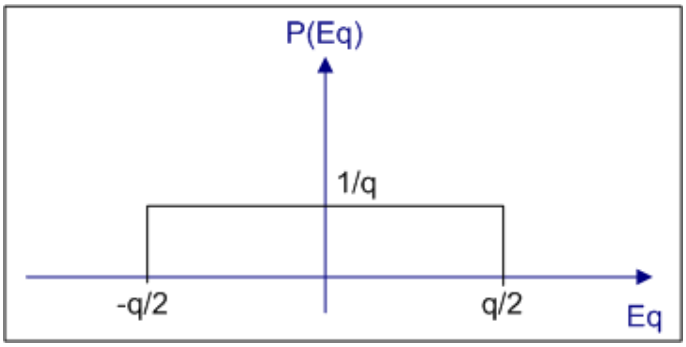

Figure 2-6: Probability density of quantization error

The power of the quantization noise is given by the following equations

$$B_q^2 = \lim_{T_e \to \infty} \frac{1}{T_e} \int_0^{T_e} E_q(t)^2 \, dt = \int_{-\infty}^{+\infty} E_q^2 \, p(E_q) dE_q \qquad \textbf{eq. 2-2}$$

$$B_q^2 = \int_{-\infty}^{+\infty} E_q^2 \, p(E_q) dE_q = \int_{-q/2}^{q/2} x^2 \frac{1}{q} dx = \frac{1}{q}\frac{q^3}{12} \qquad \textbf{eq. 2-3}$$

$$\textbf{then } B_q = \frac{q}{\sqrt{12}} \qquad \textbf{eq. 2-4}$$

The power of the quantization noise is $q^2/12$, with q the quantization step.

The transfer function of a real converter is usually affected by deterministic errors. Figure 2-7 presents the offset error that affects the transfer function. The offset error shifts the ideal transfer function.

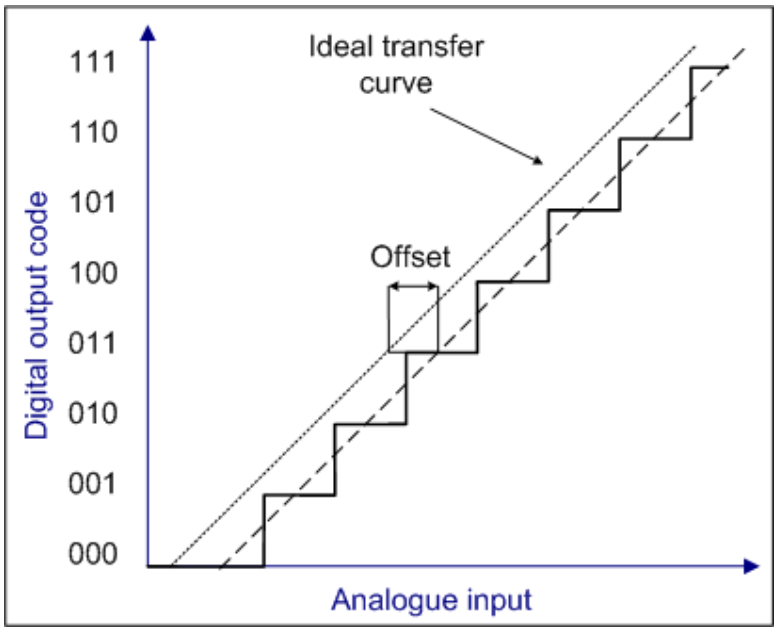

Figure 2-7: Offset error on an ADC transfer function

Gain error is the next deterministic error, presented by Figure 2-8, the gain error of an ADC or DAC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function.

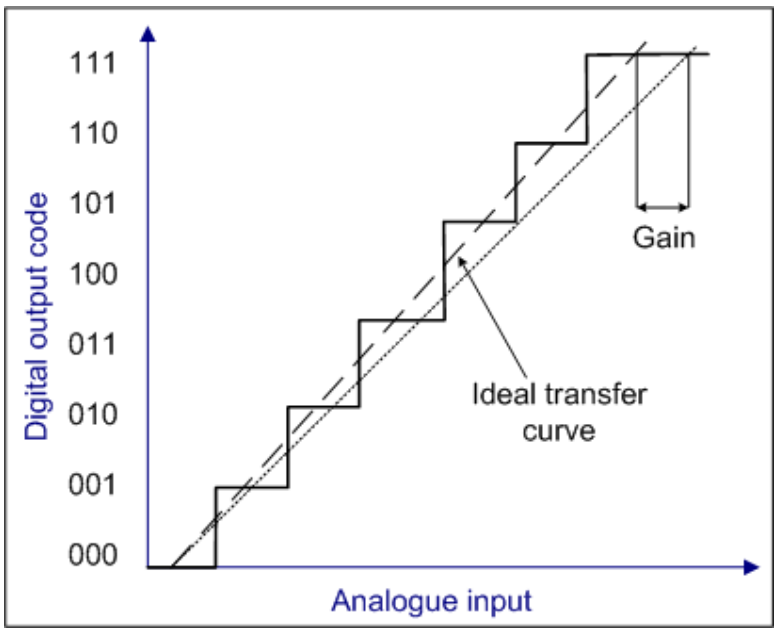

Figure 2-8: Gain error on an ADC transfer function

Another type of deterministic error affecting the transfer function of a converter is the non-linearity. Figure 2-9 gives an example of transfer function affected by non-linearity. Non-linearity errors correspond to the deviation of the actual transfer function from the ideal one. After nullifying offset and gain errors, the ideal transfer function is either a best-fit straight line or a line drawn between the end points of the transfer function.

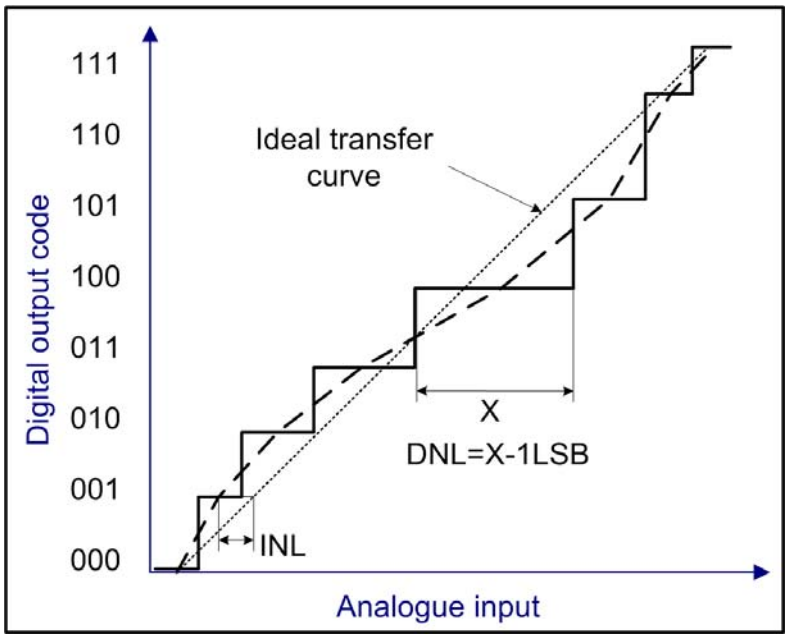

Figure 2-9: Non-linearity error on an ADC transfer function

II.2.B Stochastic errors

The second category of errors is the stochastic one. A stochastic process in opposition with a deterministic one is defined by the fact that a state does not fully determine its next state. This is also characterized by conjecture and randomness.
A first significant stochastic error that affects the conversions is the thermal noise. The thermal noise is due to the temperature variation of the converter supplies. The temperature variation induces some noise on the supplies that is brought out on the converted signal.

Thermal noise is usually modelled as an independent random variable, timely invariant. This model is obviously an idealisation. But this assumption is essential to simplify the model of noise affecting the conversion. As a consequence, for further developments thermal noise would be modelled as a random variable defined by a standard deviation and centred on zero.

The second stochastic error affecting conversions is the jitter. The jitter is an unwanted variation of one or more signal characteristics. This is a phenomenon that affects signal integrity in many conditions. For instance, in voice over IP, jitter is the variation in time between packets arrival. Concerning converters, jitter affects the sampling moment and consequently is called sampling jitter. The sampling jitter is the consequence of timing uncertainties or timing jitter affecting the sampling signal or clock. Jitter is usually modelled as a white noise and as a consequence can be defined by its standard deviation.

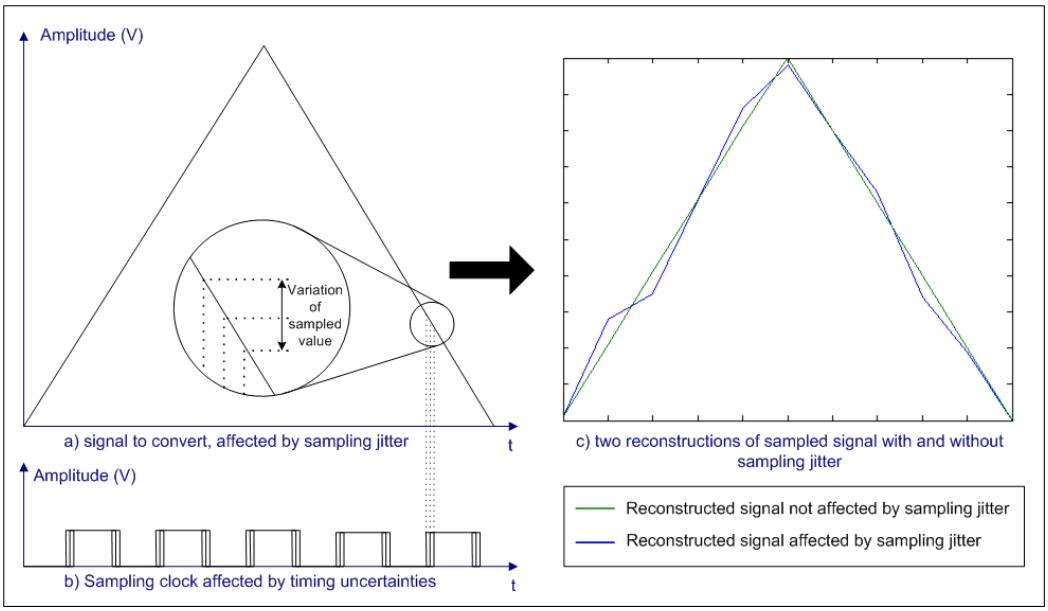

Figure 2-10: Effect of sampling jitter a) signal to convert b) sampling clock affected by some jitter c) signal reconstructed after sampling with and without jitter

II.3 Converter test parameters

Signal conversions are usually affected by several types of errors. The previous section has presented these different errors. Several test parameters are used in order to estimate the quality of the conversion. These parameters are mainly classified in two categories: static and dynamic parameters.

II.3.A Static parameters

Static parameters are the measurements of the errors that affect the transfer function:

- ✓ Offset: the offset parameter is the direct measurement of the offset error.
- ✓ Gain: the gain parameter is the direct measurement of the gain error (i.e. 2.A):

$$Gain = 100\frac{G_{real} - G_{ideal}}{G_{ideal}} \quad [\%] \qquad \textbf{eq. 2-5}$$

where G_{real} is the real gain from the transfer function and G_{ideal} the expected gain

- ✓ Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are two static parameters dedicated to non-linearity measurements (see Figure 2-9). These are the only test parameters for which the expression is different between DAC and ADC, even if their curve representations are similar. Hence, we give hereafter the expressions of both parameters for DAC and ADC.

  ADC DNL: is the individual deviation of each code width from the ideal value.

$$DNL(i) = \frac{V_{in}(i+1) - V_{in}(i)}{S} - 1,\ i = 0..2^n - 2 \qquad \textbf{eq. 2-6}$$

  where V_{in} is the input amplitude, S is the slope of the ideal transfer curve or the value of the Least Significant Bit or LSB in volt, and i the code value.

  ADC INL is defined as the deviation of the transfer function from the ideal transfer curve, which is indeed a straight line. The INL at end points is, by

definition, equal to zero. For intermediate points, INL is given by the following equation.

$$INL(i) = \frac{V_{in}(i) - V_{in}(ideal)}{S} - 1, \; i = 0..2^n - 1 \qquad \textbf{eq. 2-7}$$

DAC DNL: This is the difference between a code width and the average code width (LSB).
Thus:

$$DNL(i) = \frac{(V_{i+1} - V_i) - S}{S}, \; i = 0..2^n - 2 \qquad \textbf{eq. 2-8}$$

where V_i is the output voltage for the code i
DAC INL: This is, for each code, the difference between output quantity and the best-fit line, again expressed in LSB. Hence, the definition is:

$$INL(i) = \frac{V_i - (F - iS)}{S}, \; i = 0..2^n - 2 \qquad \textbf{eq. 2-9}$$

For DAC and ADC, the tested INL and DNL are defined as the maximum absolute value of DNL(i) and INL(i).

$$INL = max(|INL(i)|) \quad \forall i = 0..2^n - 2 \qquad \textbf{eq. 2-10}$$

$$DNL = max(|DNL(i)|) \quad \forall i = 0..2^n - 2 \qquad \textbf{eq. 2-11}$$

II.3.B Dynamic parameters

This section gives the definition of the dynamic parameters for DAC and ADC. Figure 2-11 shows the spectrum of a sine wave at frequency f_{in}, coherently sampled. A coherent sampling respects the following equation:

$$Nf_{in} = Mf_s \qquad \textbf{eq. 2-12}$$

where N is the number of samples, M the number of cycles (i.e. signal period), f_s the sampling frequency and f_{in} the input signal frequency. M and N are integer and relatively prime. Coherent sampling keeps the periodicity of the test signals. By processing the Fast Fourier Transform (FFT) of a coherently sampled signal, it is assumed that for a single tone signal all the power of the signal is contained in one FFT bin, as shown in Figure 2-11a). The spectrum of a non-coherently sampled signal suffers from frequency leakage as shown (Figure 2-11b)). Due to frequency leakage, there is a loss of information that would lead to measurement errors for the converter dynamic test parameters. Therefore the coherence condition must be carefully respected.

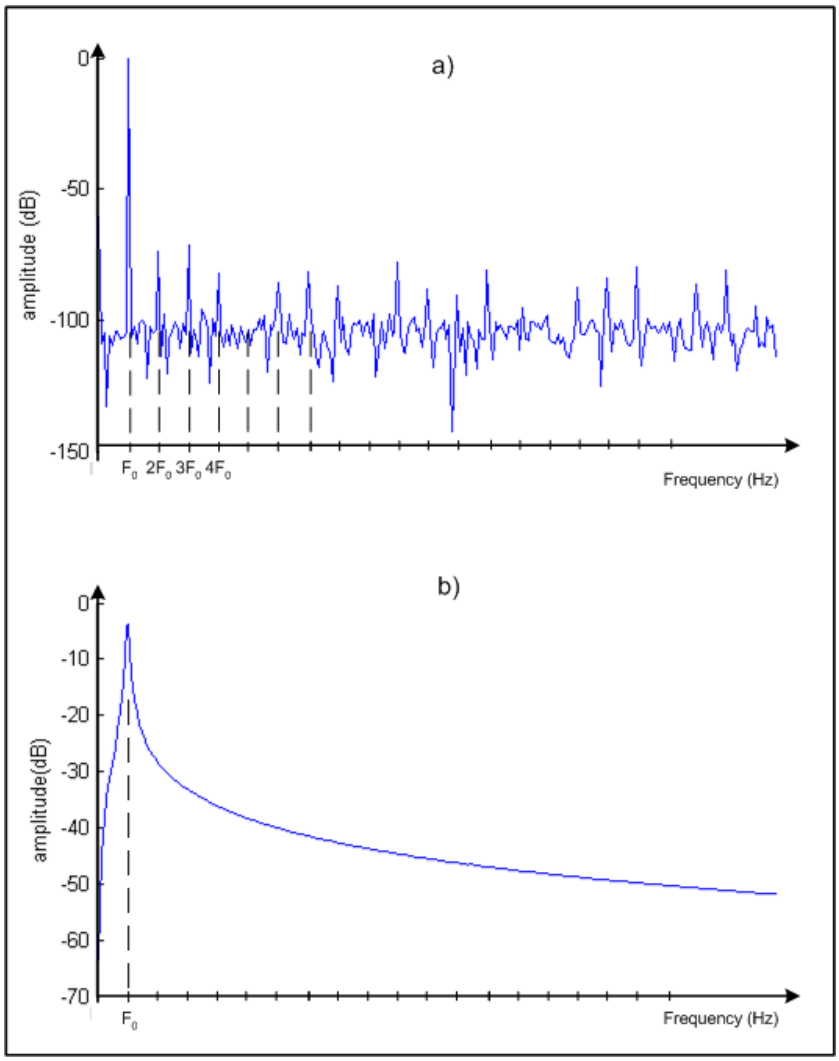

Figure 2-11: Spectrum a of sine wave a) coherently sampled b) non-coherently sampled

According to Figure 2-11a), a coherent sampling permits to extract useful data from the spectrum representation. Indeed we can see the fundamental bin at f_0, which corresponds to the input sine wave frequency, and the errors induced by the converter:

- ✓ 10 first harmonics H2 to H11 at frequencies $2f_0$ to $11f_0$
- ✓ Noise spread in all bins, it is the main part of all the bins other than harmonics and fundamental.

Once extracted, these values enter in the computation of the dynamic parameters.

The dynamic parameters are listed and defined hereafter.

Total Harmonic Distortion (THD)

This is defined as the ratio of the power contained in the harmonic spectral components and the power of the fundamental component. The power of the harmonics is the sum of a defined number of products, starting from the second order to the k^{th} one, as shown in the equation below:.

$$THD = \left(\frac{P_{harmonics}}{P_{signal}} \right)^{1/2} = \left(\frac{a_2^2 + a_3^2 ... + a_k^2}{a_1^2} \right)^{1/2}, \left[linear \right] \quad \textbf{eq. 2-13}$$

where a_1 is the *rms* amplitude of the signal, and a_2, …, a_k are the *rms* amplitudes the first *k-1* harmonics.

On a logarithmic scale:

$$THD = 10 \log \left(\frac{P_{harmonics}}{P_{signal}} \right), \left[dB \right] \quad \textbf{eq. 2-14}$$

Spurious Free Dynamic Range (SFDR)

SFDR specifies the distance between the fundamental and the maximum spurious component in the bandwidth.

$$SFDR = 20 \log \left(\frac{a_1}{max(s)} \right), \left[dB \right] \quad \textbf{eq. 2-15}$$

where s is the *rms* amplitude of the bins other than the fundamental.

Signal to Noise Ratio (SNR)

This parameter gives the ratio between the fundamental power and the noise power:

$$SNR = 10 \log \left(\frac{P_{signal}}{P_{noise}} \right), \left[dB \right] \quad \textbf{eq. 2-16}$$

The noise power computation sums all the components of the spectrum, excluding the *DC* component, the signal, and the first *k-1* harmonics.

The SNR parameter is partly dependant on the resolution, directly correlated to the quantization error (or noise). A maximum value for this SNR is thus achievable, as demonstrated in eq. 2-21. For a full-scale input sine wave of amplitude V_{fs}, the power of the fundamental is given by:

$$P_{signal} = \frac{1}{2} \left(\frac{V_{fs}}{2} \right)^2 \quad \textbf{eq. 2-17}$$

$$P_{signal} = \frac{1}{2} \left(2^{R-1} \right)^2 q^2 = 2^{2R-3} q^2 \quad \textbf{eq. 2-18}$$

where R is the resolution of the converter.

According to eq.2-4, the power of the quantization noise is $q^2/12$. As a consequence, the maximum SNR which is the one of an ideal converter can be calculated and predicted from its resolution by:

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{2^{2R-3} q^2}{\frac{q^2}{12}} = \frac{3}{2} 2^{2R} \quad \textbf{eq. 2-19}$$

$$SNR_{dB} = 20 \log (SNR) = 20R \log (2) + 10 \log \left(\frac{3}{2} \right) \quad \textbf{eq. 2-20}$$

$$SNR_{dB} \approx 6.02R + 1.76 \qquad \textbf{eq. 2-21}$$

SIgnal-to-Noise And Distortion ratio (SINAD)

This number gives the ratio between the power of the signal, and the sum of the power of the harmonics and the noise in the considered bandwidth, given by:

$$SINAD = 10\log\left(\frac{P_{signal}}{P_{harmonics} + P_{noise}}\right), [dB] \qquad \textbf{eq. 2-22}$$

Effective Number Of Bits

This parameter is derived from the SINAD. It specifies how many bits an ideal converter would require in order to obtain the same SINAD as that measured on the real converter. Comparing this number to the designed number of bits indicates how well the converter approaches the ideal case.

$$ENOB = \frac{SINAD_{dB} - 1.76}{6.02} \qquad \textbf{eq. 2-23}$$

II.4 **Converters testing**

II.4.A Usual test set-up

DSP-based set-up is nowadays the usual test set-up for analogue and mixed-signal devices [bern03][bella96][majh97][maho87][DYNA00]. It is even standardised for ADC test [IEEE1241]. In this configuration, the test signal is driven through the DUT primary inputs and the response is captured at the DUT primary outputs. Pre- and post-processing are computed in the digital domain. Figure 2-12 and Figure 2-13 give the commonly used test set-up for ADC and DAC.

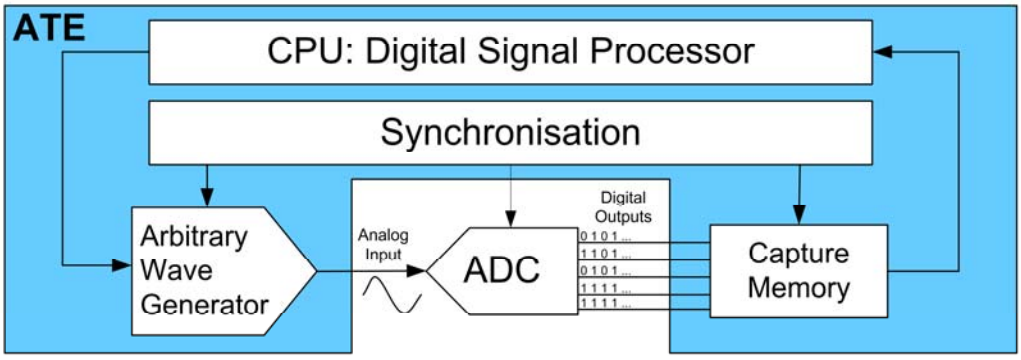

Figure 2-12: DSP-based test set-up of an ADC

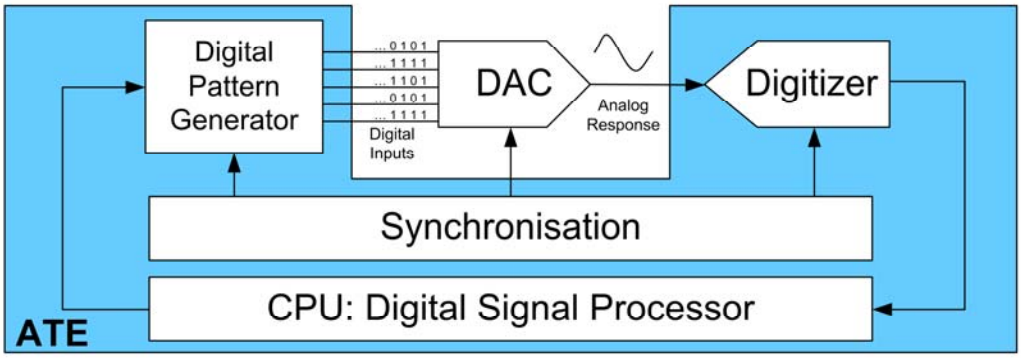

Figure 2-13: DSP-based test set-up of a DAC

Pre- and post-processing being performed in the digital domain, they put some related requirements on ADC and DAC test setups. For ADC testing, an arbitrary waveform generator is required in order to convert the test signal from digital to analogue domain and to drive it to the analogue input of the converter. The output samples are captured and stored in a memory before being processed. For the DAC, the memory is used to store the test signal and to send it to the digital inputs of the DAC. To enable digital post-processing, a digitizer converts the analogue output signal into digital codes.

In addition to this test hardware configuration, the test frequencies must be chosen such that the coherent condition is fulfilled (eq. 2-12).

II.4.B Test methods

II.4.B.a. Static testing

For DACs and ADCs the principle of static testing is to apply an input ramp to the converter – analogue ramp for the ADC and digital ramp for the DAC – in order to stimulate every code. Once the input ramp is applied to the converter and output codes (or digitized signal) are stored into the memory, a histogram is computed giving the number of occurrences of every code. This histogram is then compared to the reference histogram corresponding to an ideal converter of the same resolution to extract the static parameters.

II.4.B.b. Dynamic testing

For DACs and ADCs, as previously mentioned, the same dynamic parameters are defined. These parameters are measured using dynamic testing. A sine wave is generated at the input of the converter and the response of the converter is captured. Once the output signal or sample set is captured, the spectrum is computed using the Fast Fourier Transform. Subsequently, the dynamic parameters are drawn from the FFT (SNR, THD, and so on). It is to mention that test signals usually try to match the full-scale of the converter in order to stimulate all the codes.

II.5 **Summary**

Converter test parameters have been defined and standardised [IEEE1241] [DYNA00] for a long time. They truly describe static and dynamic behaviours of the converters under test. in addition, test methods for stand-alone converters are mature. Converters embedded in systems are usually tested using conventional test methods as

for stand-alone components testing. Consequently, the ATE has to be equipped with multiple high-performance mixed-signal test instruments. These methods do not enable a fully digital test of a set of embedded converters. The next section deals with this targeted fully digital test of converters.

III State-of-the-art of fully digital test methods for converters

III.1 Introduction

Fully digital test of data converters means that the test methods require only the digital resources of the test platform. Focusing on this purpose, two different approaches have been published since the early 90's. Chronologically, the first approach is to transfer the analogue test instruments from the test platform to the circuit itself. This approach is the so-called Built-In-Self-Test or BIST. The second approach aims at using some functional elements of the device under test (DUT) as test instruments. These two approaches are described in the following sections.

III.2 Built-In-Self-Test (BIST)

Equipment limitations have forced to embed test resources on-chip Because of this test development trend the built-in-self-test or BIST have emerged, with solutions for embedding test signal generators and response analysers in order to reduce the resources of the test platform, or to overcome their poor performances. BIST solutions have first revolutionized digital testing, and later it appeared also in the analogue and mixed-signal areas. The key advantage of this approach regarding analogue testing is the reduction of the resources of the test platform. Several BIST solutions have been developed and commercialised for converter testing [geor02], which can be found in the literature.

III.2.A Histogram-based BIST

The first BIST solution for converters, HABIST [fris97], is a straightforward BIST implementation of the histogram test. A test signal is sourced to the DUT, and then the output sample set is stored in a memory before the histogram computation. The histogram of the DUT is compared to an ideal reference. Thanks to this processing, the noise, the gain, the offset and the distortions of the DUT are tested. This solution is the only commercialised histogram-based BIST. A drawback is the significant area overhead required to store the captured data. In addition, the test generation must be very accurate, and this subject is not addressed in the publications. A similar solution, suffering from similar drawbacks, has been developed in [racz95] [racz96] [racz96_2].

Considering the drawbacks affecting direct implementation of statistical verification of converter activity, Renovell et al [reno00] [azai01_2] [azai01_3] have published an approach that reduces area overhead. The solution is based on a time decomposition of parameter computations. All the parameters are calculated step-by-step. The time decomposition approach removes the need of a dedicated memory to store response data. The hardware implementation for post-processing is limited to a comparator, a counter, a register, an adder/subtractor and a small control unit. The majority of published solutions do not address the linearity issue of the test signal. The use of a DAC and a filter is a solution generally proposed but which is not really efficient.

Indeed, it induces both area overhead and reliability issues. This issue is also addressed by Renovell et al publications [bern01] [bern02]: an accurate ramp generator is presented, based on the load of a capacitor with a constant current. Another signal generator is proposed in [chen99] [huan00] [huan00_2]. The stimulus generator is made of a pattern memory and a simple 1-bit DAC. It is to notice that the solution proposed in Figure 2-14 is the only one developed to test the linearity of a DAC and ADC, both embedded in the same system.

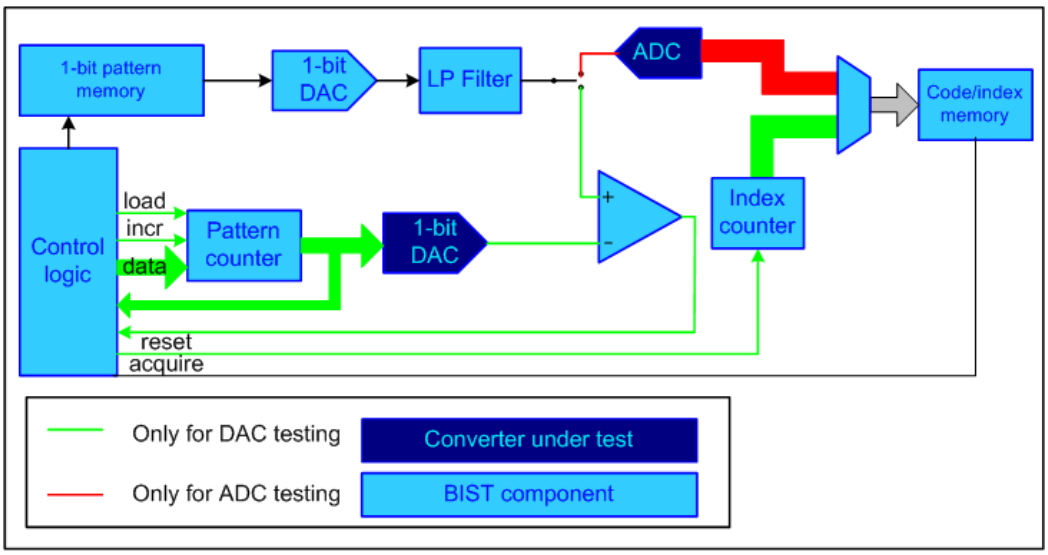

Figure 2-14: BIST architecture for DAC and ADC [chen99]

The stimulus generation is based on delta-sigma modulation technique. The stimulus is at first generated by a software delta-sigma modulator. The delta-sigma modulator converts the signal into a high-speed but low-resolution (typically single-bit) digital signal. The bit stream is stored on-chip in a pattern memory. Then a 1-bit DAC and a low-pass filter are required on-chip to convert the digital pattern into an analogue stimulus. The proposed stimulus generator requires an additional analysis in order to evaluate if it is accurate enough for high-resolution converters.

It is to notice that the histogram-based BIST solutions enable to test the transfer function parameters, i.e. gain, offset error, and non-linearities.

III.2.B Oscillation-based BIST

The principle of the oscillation-based BIST is to convert the DUT into a circuit that oscillates. Additional circuitry enables a partitioning of the DUT into building cores. The building cores oscillation frequency is linked to performance parameters and can be used as a fault detection criterion.

Concerning converters, an ADC can be tested into an oscillation mode thanks to a feedback path, as proposed by Arabi [arab97] (see Figure 2-15).

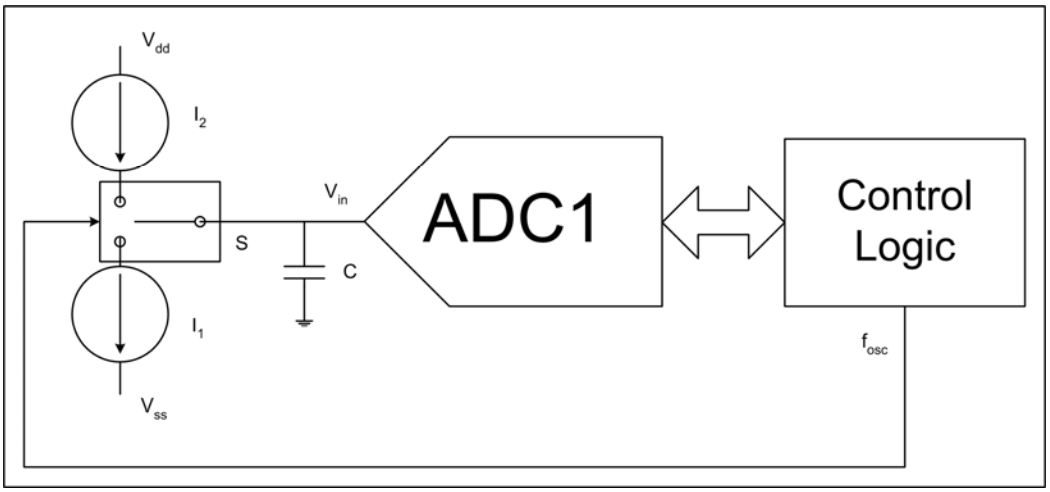

Figure 2-15: Oscillation-based BIST architecture proposed in [arab97]

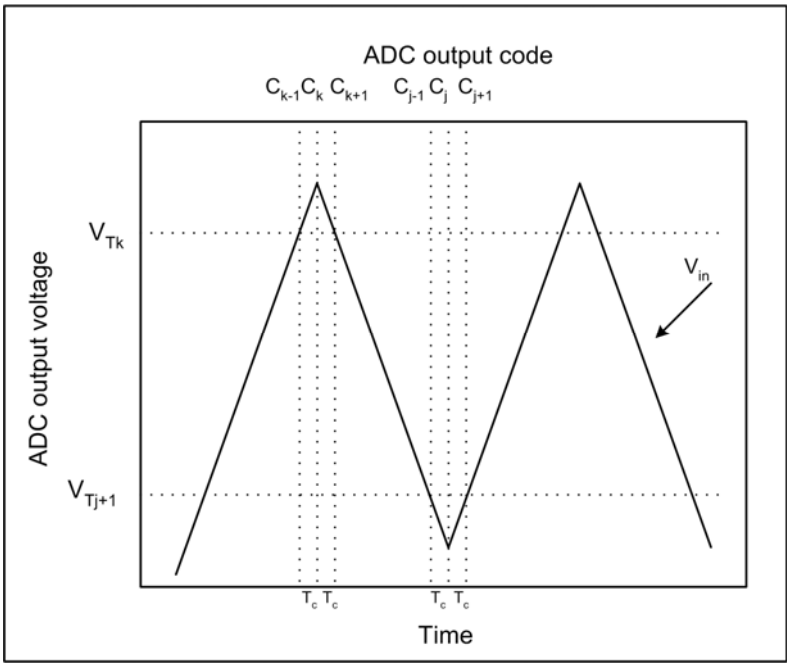

Figure 2-16: ADC input voltage oscillation between V_{Tk} and V_{Tj+1} transition thresholds

Figure 2-16 illustrates the oscillation around two predetermined codes, C_j and C_k. All operations are directed by the control logic. When the ADC output reaches the code C_j the integrator input current is switched to I_2 (Figure 2-15) and the input voltage of the ADC under test V_{IN} increases until the control logic detects Cj, whereupon the switch is changed ramping down the ADC input voltage. The switch S passes the current I_1 until the ADC reproduces code Cj, and the procedure is repeated. The oscillation frequency is link to the capacitor C, the conversion time, V_{Tk} and V_{Tj+1}.

In order to measure DNL at a specified code C_k, using the test configuration in Figure 2-15, the ADC output must be forced to oscillate between Ck and Ck-2. The other tests are defect oriented. Indeed they propose to test the time of conversion or the oscillation frequency.

Advantageously, the test response is digital and no analogue high-precision stimulus is required. However, this test solution is mainly defect oriented and is potentially suffering from test escapes or decrease in yield. In addition the oscillation around one code to measure INL and DNL is sensitive to noise.

III.2.C FFT-based BIST

Above referenced BIST solutions test static parameters using two approaches:

- ✓ Direct implementation of conventional static test: the histogram-based test;
- ✓ Alternate solution: oscillation-based approach.

Concerning dynamic parameters of converters, the dedicated approach consists in implementing conventional dynamic test: FFT-based test. The most mature BIST approach based on FFT analysis is the MADBIST. This solution has been proposed by Toner and Roberts. First publications [tone93] [tone95] deal with SNR measurement using a single-tone test signal. Later [tone96], the method was extended to dynamic measurements, harmonic and inter-modulation distortion measurements using a multi-tone test signal. Considering our objective of system-level testing, this method is interesting. Indeed, the circuit under test in these papers is a complex system made of a DAC, an ADC and a DSP core. In addition, the fully digital test of both converters is introduced. The plan would be to test the ADC and afterwards to use it to test the DAC [ton95]. Unfortunately, this subject is not really addressed and relative performances are not discussed. Regarding our objective, the MADBIST solution does not fulfil our initial objective, because it is dedicated to test sigma-delta converters. We are looking for test solutions that are not dedicated to a particular architecture.

Most of the referenced BIST solutions are suited for static parameters estimation of ADCs. In addition some solutions are dedicated to sigma-delta ADCs. The only BIST solution related to dynamic parameters estimation is the MADBIST of Toner and Roberts. The advantage of such a method is its application to both DACs and ADCs testing of dynamic parameters. But this solution is difficult to adapt to our conditions. Indeed, this solution is dedicated to the sigma-delta architecture, and generates a significant area overhead.

In summary, BIST is a solution to reduce test resources on the test platform for stand-alone converters. However, the proposed solutions do not fulfil all the requirements of industrial testing, in terms of reliability, cost, or flexibility. The re-use of the embedded converters for test could be an attractive solution, minimizing the area overhead and being able to run the test at-speed. . The next section focuses on this subject.

III.3 **Functional elements as test instruments**

Considering a set of several ADCs and DACs embedded in a system, the main drawback of BIST is the fact it would require significant area overhead or very long test time. Additionally, BIST is sensitive to faults in the circuitry, as well as to process variations. As a consequence, they are not suited to our test conditions. An interesting solution is to connect a DAC output to an ADC input in order to test simultaneously or consecutively these converters using only digital test resources like for the BIST, but with a negligible area overhead in order to reduce the design for testability. Indeed, with such a configuration, the DAC generates the test signal for the ADC and

the ADC digitizes the test signal outing from the DAC. Some solutions based on this idea can be found in the literature.

III.3.A Re-use of embedded functional DAC to test ADC

The first study that proposes to re-use functional elements to test the embedded converters was published by Ehsanian et al [ehsa96][ehsa98]. They propose a histogram-based BIST approach, targeting the INL, the DNL, the gain error and the offset error. They propose to re-use a DAC in the system to generate the test signal for the ADC. The main drawback of this approach is the fact that they re-use a functional element without testing it. As a consequence, the accuracy of the test can be deteriorated by the DAC. In addition, the DAC performances should be higher than the DUT performances in order to implement an efficient test. The conclusion of this first proposition to connect DAC and ADC is the need to test both of them in order to validate the efficiency of the test.

III.3.B DAC/ADC chain, test of both elements simultaneously

Teraoka et al [tera94] have developed a test solution for a DAC and an ADC embedded in a system. This system is a voice codec (coder-decoder) and is comprised of a 13-bit DAC, a 13-bit ADC and a digital section made of a memory and a DSP. This is the first solution that introduces the test of embedded DAC and ADC using no expensive external test instrument and no area overhead dedicated to test. The test solution uses an analogue interconnection of the two converters and re-uses embedded DSP core. The test signal is generated on chip, stored in a RAM. The test signal is sent by the DAC to the ADC, and then stored in a RAM. Afterwards an FFT-based analysis of the captured signal is performed. The experimental validation is successful. Indeed, there is no test escape or yield loss due to BIST implementation. But the drawback of this method is linked to the estimated test parameters. Indeed, for experimental validation, they do not measure conventional dynamic parameters of each converter. The test method gives an estimation of two non-conventional dynamic parameters called attenuation/frequency distortion and variation of gain with input level. According to experimentations, these two dynamic parameters give some good results to converters testing. But they are suited for this application and maybe not for several different ones. In addition these two test parameters are given for the chain DAC/ADC. Consequently, it is a go/no-go test and no discrimination of defective element is possible. Moreover, a compensation of the errors could occur, leading to test escapes. In addition, these alternative test parameters are suited for the presented application but cannot be used as a generic test method. The conclusions that should be drawn from this second approach of DAC/ADC chain testing are:

- ✓ Use conventional test parameters for the universality of the method like conventional tests
- ✓ Discriminate error sources in order to truly test the DAC and the ADC.

III.3.C DAC/ADC chain, discrimination of test parameters of both elements

Abraham et al from the university of Texas at Austin have published several papers [chun04] [yu03] [yu03_2] [shin06] [shin06_2] from 2000 to 2006, dealing with the DAC/ADC chain testing. Their test developments are interesting because on contrary to Teraoka et al's method, they plan to test each converter and to discriminate their parameters.

[yu03] [yu03_2] are two complementary publications addressing DAC/ADC chain testing. These two publications are complementary because they address the test of different parameters. [yu03] deals with the estimation of static parameters: DNL and INL. The method is based on pseudo-DNL (PDNL) and pseudo-INL (PINL) measurements. These PDNL and PINL are the INL and DNL of the chain of converters. Using these primary measurements and an additional post-processing, they plan to estimate the DNL and INL from each converter. There is no experimental validation. In the second publication, the SNR is tested. This second method is dedicated to sigma-delta converters. Indeed, it requires the observation of an additional internal point. As for the previous method, there is no experimental validation. The main drawbacks of these methods are: no experimental validation and they are suited for sigma-delta architecture converters. Nevertheless, they demonstrate the growing interest in testing embedded converters using fully digital test and a loopback configuration between DACs and ADCs.

2004 publication from Abraham et al [chun04] addresses again the linearity testing of the DAC and the ADC. The test path is modified. Indeed, as shown in Figure 2-17, an adder is introduced in the loopback between the DAC and the ADC, in order to add some noise to the test signal.

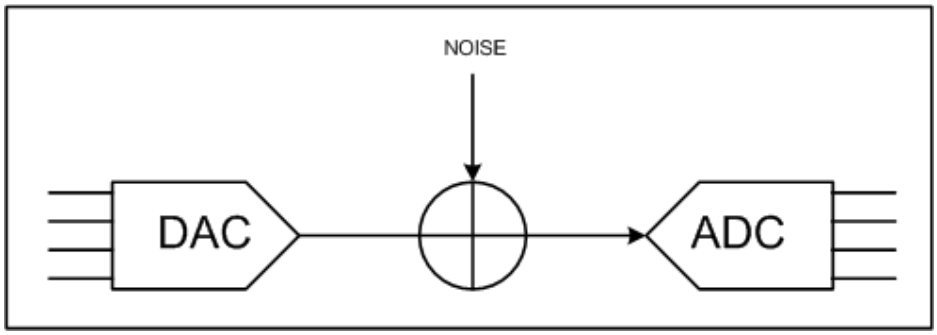

Figure 2-17: [chun04] test configuration

The test method is based on dithering technique [gray93] [wann03]. Thanks to the addition of noise, the linearity of the test signal is artificially increased. As a consequence, the signal at the output of the ADC is distorted by the non-linearities from the ADC and not from the DAC. The ADC is firstly fully characterized in term of INL and DNL, and then the DAC is characterized using the extracted non-linearities of the ADC. This method was validated by simulation, but it could be limited because it relies on the "quality" of the noise.

[shin06] is the first publication from Abraham et al that addresses the discrimination of harmonic contributions in the DAC/ADC chain. The method is based on a particular loopback between the DAC and the ADC. Figure 2-18 presents this particular hardware implementation.

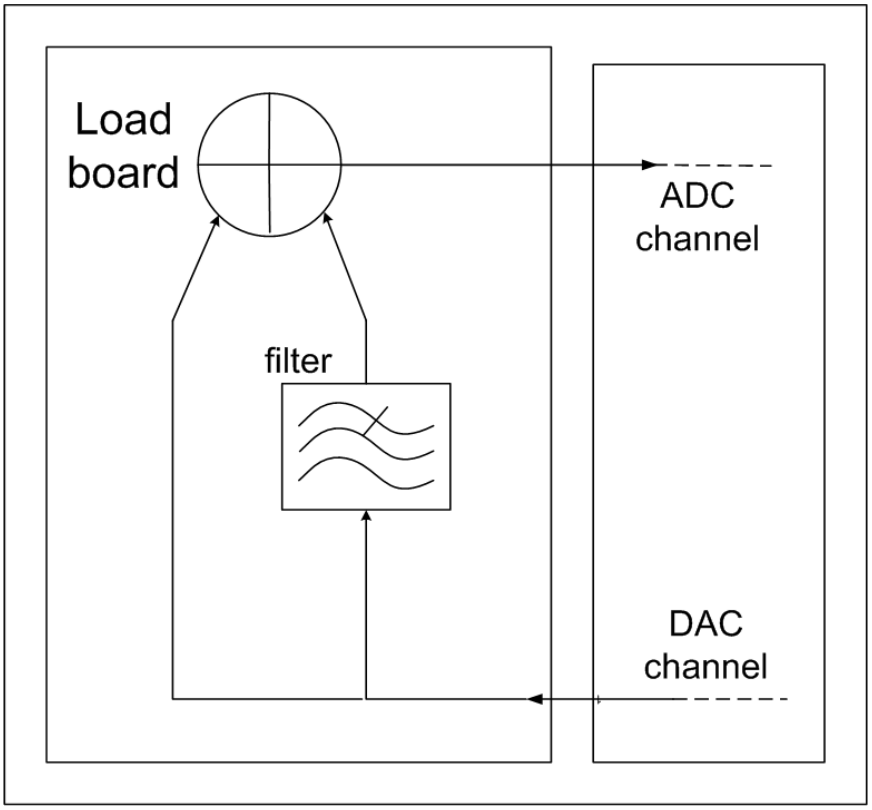

Figure 2-18: Loopback implementation from Abraham et al solution [shin06]

The loopback is implemented on the test board. It requires a filter and an adder. The output of the DAC channel goes through a filter. This filtered signal is summed with the DAC channel output. Afterwards the signal is sent to the ADC channel. The filter specifications, group delay, noise contribution and attenuation/frequency, should be characterized before implementation. The test signal is a two-tone sine wave. In the mathematical development, the signal and the harmonic contributions of each element are modelled using a Taylor expansion equation. The equation that describes the signal at the output of the ADC can be decomposed in a system of equations. The number of equations in the system is equal to twice the number of harmonics that you want to estimate. Solving the system allows one to estimate the harmonic contribution of the DAC on one side and the ADC on the other side. However, the equations are linearly independent and consequently simply solvable only when you consider the first three harmonics. Therefore, the dynamic parameters cannot be estimated with a sufficient accuracy. As a consequence, the method should be completed by a non-linear regression algorithm. The non-linear regression starts with a learning phase where a conventional measurement is made on many devices, before applying the alternative method. Because this learning phase is necessary, a conventional test should be implemented and this is exactly what we want to avoid because of the reduced number of access points to converters embedded in a complex system. This publication also proposes to discriminate the noise from both converters. The method is shortly explained and based on an approximation concerning the noise. The experimental results show some significant variations in SNR estimations. This method is of interest with respect to our objective because this is the only publication addressing the issue of dynamic parameters discrimination in a DAC/ADC chain. Unfortunately, the implementation of such a method is not possible in a complex

system. Indeed, the hardware implementation is based on a filter. This filter should be on the test board in order to be fully characterized before it is used for test. The integration of such a design-for-testability is not possible because it could not be fully characterized due to the reduced access points in such systems. In addition, the test method requires a learning phase, using conventional test instruments, and this is what we want to avoid, because of instruments cost.

Finally, [shin06_2] is a publication of Abraham et al addressing DAC/ADC direct chain testing. The purpose of this publication is to discriminate the INL/DNL of each converter. The test set-up is a simple loopback between a DAC and an ADC, as presented by Figure 2-19.

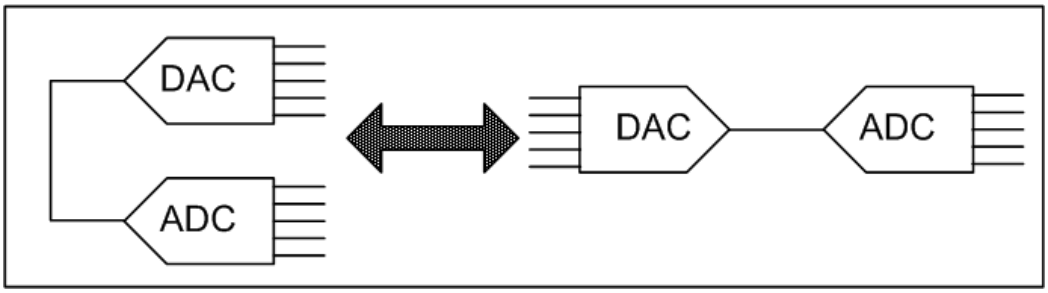

Figure 2-19: Loopback DAC/ADC

This work is the continuation of [shin06], using an estimation of the ADC harmonics combined with a Chebychev polynomial algorithm in order to compute the INL of the ADC. The INL of the DAC is compensated using a statistical digital equalizer. Once the INL values of the DAC are compensated, the ADC INL is measured. This approach is contradictory. Indeed, it is composed of two steps. The first step gives the harmonics estimation of a DAC and an ADC from a DAC/ADC chain. Then the INL curve of the DAC is estimated using its estimated harmonics and a Chebychev polynomial based algorithm. This computed INL is used to compensate nonlinearities of the DAC, in order to measure the INL from the ADC. Why do they use a Chebychev polynomial based algorithm to measure the INL of the DAC and not of the ADC? In addition, experimental validations give not so good results. Indeed, when the DAC INL is quite big (over 2.5LSB), there is a significant estimation error of 0.5 to 1LSB for the ADC INL.

III.4 **Summary and opening**

Fully digital test of converters has been studied since the early 90's. The first approach developed is the Built-In-Self-Test or BIST, which consists in embedding the signal generation and capture directly into the DUT. The test is consequently fully digital as far as it requires only digital resources on the test platform. The second approach consists in using functional elements already available in the device to test the embedded converters. The majority of the published studies focus on the static parameters estimation. In addition, we can find in the literature a lot of studies that link static and dynamic parameters. Indeed, INL strongly influences the dynamic performances through harmonic generation. The information given by the spectral analysis performed for dynamic parameters could thus be used to extract INL values with a shorter testing time. Indeed, this method requires much fewer samples than the histogram-based one, thus the time for processing, so the test time, can be significantly shortened. Two very different approaches can be used to evaluate the relationship between static and dynamic specifications: i) a statistical approach

proposed in [bern03] consists in detecting devices for which one of the functional parameters overruns specifications, but this kind of statistical method is not viable in a BIST context; ii) an analytical approach that consists in identifying the Fourier coefficients, obtained from the FFT computation, with the coefficients that describe the INL curve. Most of the proposed techniques are based on polynomial interpolation of the INL curve [sunt97] [xu99] [adam02] [csiz99]. A more recent one [kerz06_2] [jani06] is based on the Fourier series expansion of the INL. As a consequence, our further studies will focus only on dynamic parameters estimation.

It is to notice that there is no efficient fully digital method for converter dynamic parameters estimation. But if we consider a set of converters (DACs and ADCs) embedded in a system, the best approach is obviously to re-use some functional elements to test the converters. In this method, the DAC output is connected to the ADC input, building a chain where the DAC is used to generate the test signal of the ADC, and the ADC is used to capture the test signal at the output of the DAC. This approach has been introduced by Abraham et al, but it does not give some convincing results. The main consequence of this approach is the need to test all the converters of the chain, and discriminate their dynamic parameters. The next section deals with DAC/ADC chain testing.

IV Serialization of DACs and ADCs in complex systems in order to test them

IV.1 **Introduction**

Let us consider a complex system embedding several converters as shown in Figure 2-20. It contains a set of converters: DACs and ADCs. We aim to test them fully digitally.

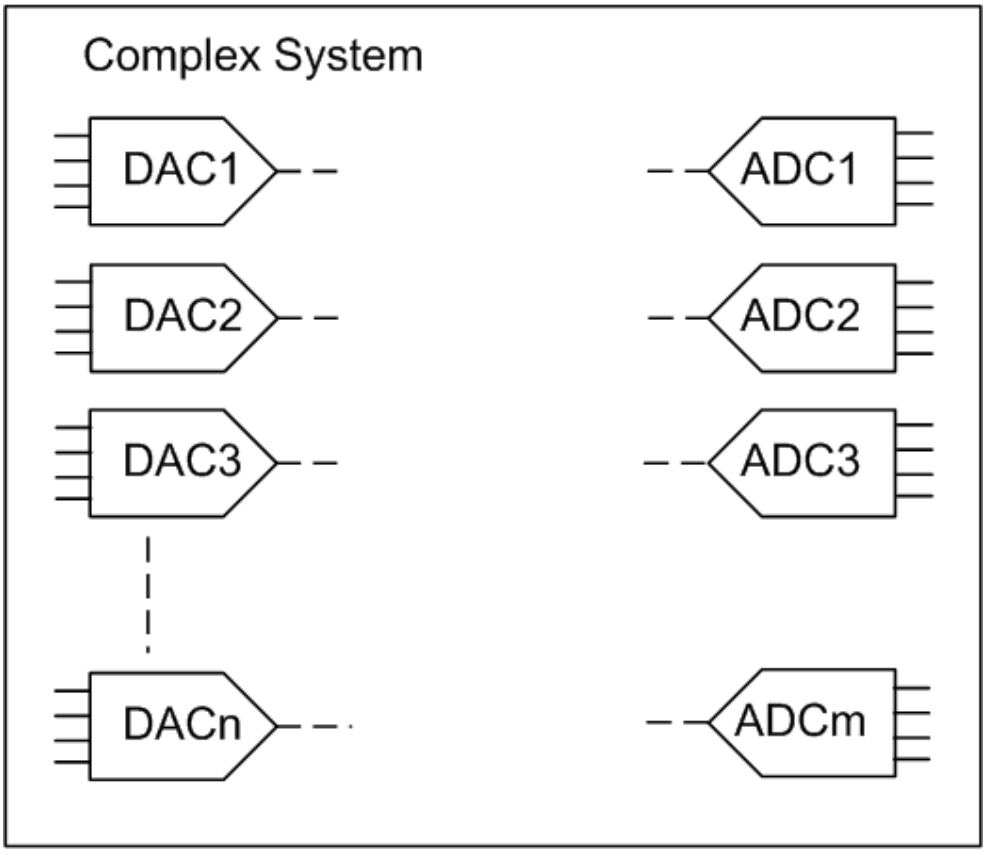

Figure 2-20: Complex system embedding several converters

As previously explained, we are going to focus on dynamic parameters estimation. Dynamic parameters are computed using two types of data: noise and harmonic distortions. Concerning noise, a mature and efficient method exists [cauv00] that is suited to our test conditions. Figure 2-21 depicts the test configuration.

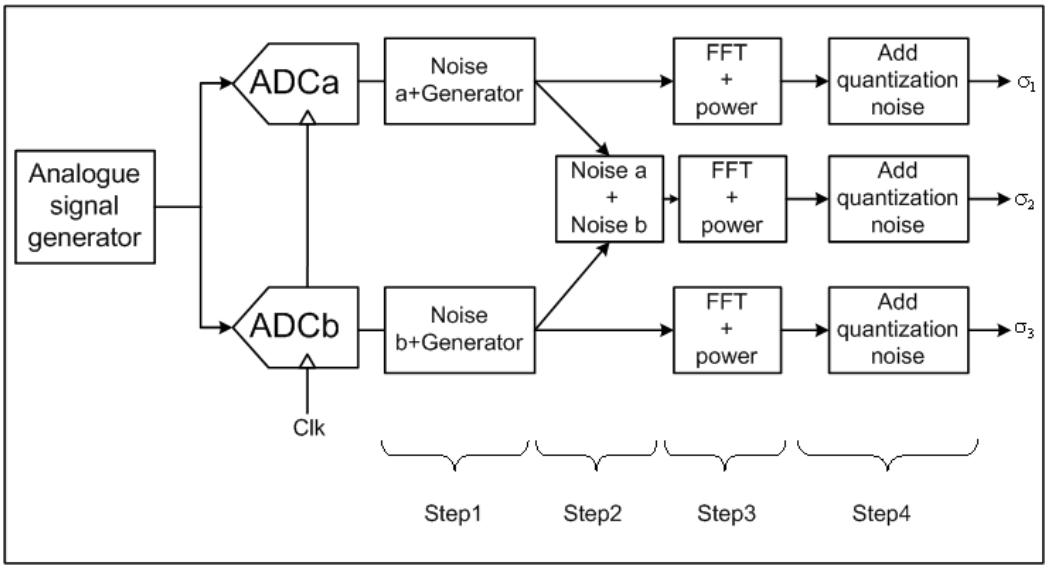

Figure 2-21: 2-ADC method for noise discrimination

This method is based on one of the properties of random variables. Two ADCs receive simultaneously the same input and clock signals. The variances of the noise of each individual converter and of the differential signal between A and B are computed, giving the following system of equations:

$$\begin{cases} \sigma_1^2 = \sigma_a^2 + \sigma_g^2 \\ \sigma_2^2 = \sigma_a^2 + \sigma_b^2 \\ \sigma_3^2 = \sigma_b^2 + \sigma_g^2 \end{cases} \quad \textbf{eq. 2-24}$$

where σ_g represents the noise induced by the generator(s), and $\sigma_{a,b}$ the noise of the converters a and b.

Once the calculations have been performed, the noise of the generator is removed, giving the variance for each ADC:

$$\begin{cases} \sigma_a^2 = \dfrac{\sigma_1^2 - \sigma_3^2 + \sigma_2^2}{2} \\ \sigma_b^2 = \sigma_2^2 - \sigma_a^2 \end{cases} \quad \textbf{eq. 2-25}$$

The method is derived from a method developed by Langard [lang94]. In [cauv00], the method has been suited to ADC test by discriminating the noise of each ADC from the noise induced by the analogue signal generator. This method can be used in our test conditions. Indeed, the analogue signal generator can be replaced by a DAC. As a result, by using this approach we could be able to discriminate the noise of the two ADCs from the DAC one.

Harmonic distortions, the second type of data used to compute dynamic parameters, are key data in the evaluation of the conversion quality. Considering our test conditions, a promising test configuration, presented by Figure 2-22, is to connect DAC output to ADC input. As a consequence we will be able to implement a fully digital test, driving test signal through DAC to ADC.

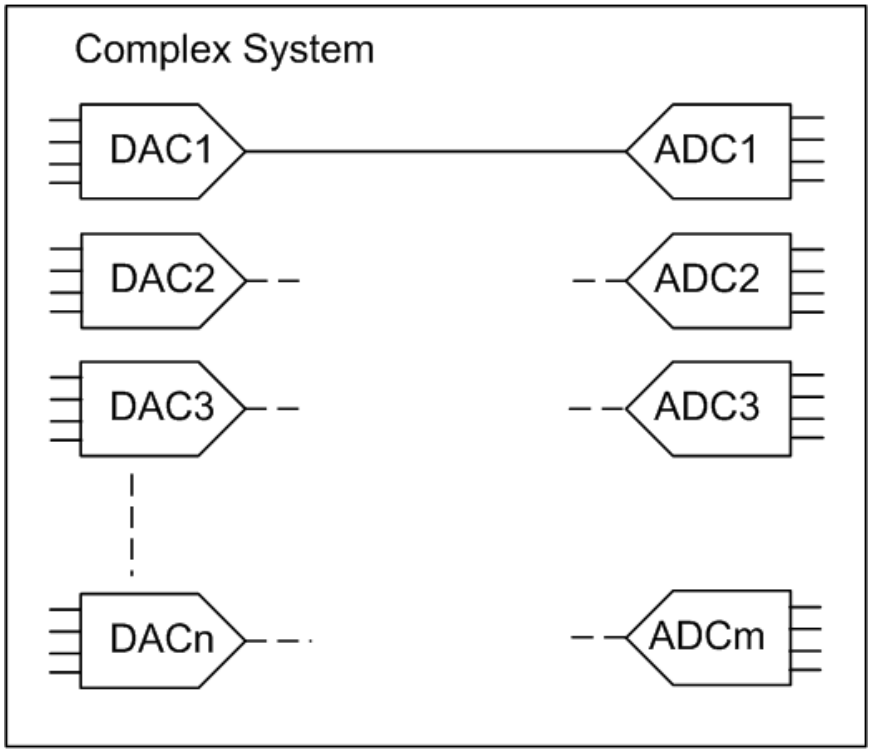

Figure 2-22: A fully digital test implemented by connecting a DAC and an ADC in the analogue domain

The following section deals with the test difficulties induced by implementing such a test configuration.

IV.2 **DAC/ADC chain test difficulties**

IV.2.A One converter model

Testing several cores using a complex test path made of these tested cores induces some difficulties. For instance, a path-based or loopback-based test for a transceiver suffers from reduced observability and controllability of tested cores. These reduced observability and controllability induce some risks of fault masking whatever the test parameters. The path-based test implementation of Ozev et al [ozev04] suffers from reduced test coverage due to noise level. Dabrowski [dabr04] addresses the risk of fault masking and proposes to predict it. Considering a complex test path made of one DAC and one ADC, the risk of fault masking is also obviously present.

Let us consider a single-tone test signal applied to an ADC.

$$x(t) = V_{in}\cos(2\pi f_{in}t + \theta_i) + V_{DC} \qquad \textbf{eq. 2-26}$$

where V_{in} is the amplitude, f_{in} the frequency, θ_i the initial phase and V_{DC} the offset of the sine wave. This sine wave is distorted during the conversion by several sources of errors. The signal is sampled N times, at frequency f_s. In order to have a coherent sampling the following equation where M is the number of cycles should be verified

$$Nf_{in} = Mf_s \qquad \textit{eq. 2-12}$$

The first kind of error is the quantization noise. It is due to the quantization of the sampled signal. Once sampled, the signal at the output of the ADC, affected by quantization noise, could be written like this:

$$s(n) = x(n) + q(n) \quad \textbf{eq. 2-27}$$

where $$x(n) = 2^R \frac{V_{in}}{V_{FS}} cos(\theta_n + \theta_i) + 2^R \frac{V_{DC}}{V_{FS}} \quad \textbf{eq. 2-28}$$

$$\theta_n = 2\pi\left(\frac{M}{N}\right)n \quad \textbf{eq. 2-29}$$

and q(n) is the quantization noise.

The converted sine wave is also affected by other errors. The conversion is affected by timing uncertainties from the clock. It induces some sampling jitter. As a consequence [jani01]:

$$x(n) = 2^R \frac{V_{in}}{V_{FS}} cos(\theta_n + \theta_i + Ji(n)) + 2^R \frac{V_{DC}}{V_{FS}} \quad \textbf{eq. 2-30}$$

where $Ji(n) = 2\pi f_{in}\delta_j(n)$, $\delta_j(n)$ is the timing uncertainty usually modelled by a white noise. As $Ji(n) << 1$, thanks to a first order Taylor series expansion:

$$x(n) = 2^R \frac{V_{in}}{V_{FS}} cos(\theta_n + \theta_i) - 2^R \frac{V_{in}}{V_{FS}} sin(\theta_n + \theta_i) Ji(n) + 2^R \frac{V_{DC}}{V_{FS}} \quad \textbf{eq. 2-31}$$

As a consequence:

$$s(n) = x(n) + q(n) - 2^R \frac{V_{in}}{V_{FS}} sin(\theta_n + \theta_i) Ji(n) \quad \textbf{eq. 2-32}$$

In addition, another stochastic error is the thermal noise. As a consequence

$$s(n) = x(n) + q(n) - 2^R \frac{V_{in}}{V_{FS}} sin(\theta_n + \theta_i) Ji(n) + N_{th}(n) \quad \textbf{eq. 2-33}$$

where $N_{th}(n)$ is the thermal noise.
This equation can be written like this:

$$s(n) = x(n) + \varepsilon(n) \quad \textbf{eq. 2-34}$$

where $\varepsilon(n)$ is the sum of the quantization noise, the jitter and the thermal noise.

The converted signal is also affected by deterministic errors, also called nonlinearities. Nonlinearities are defined by a curve. Figure 2-23 presents an example of an INL curve from a 12-bit ADC.

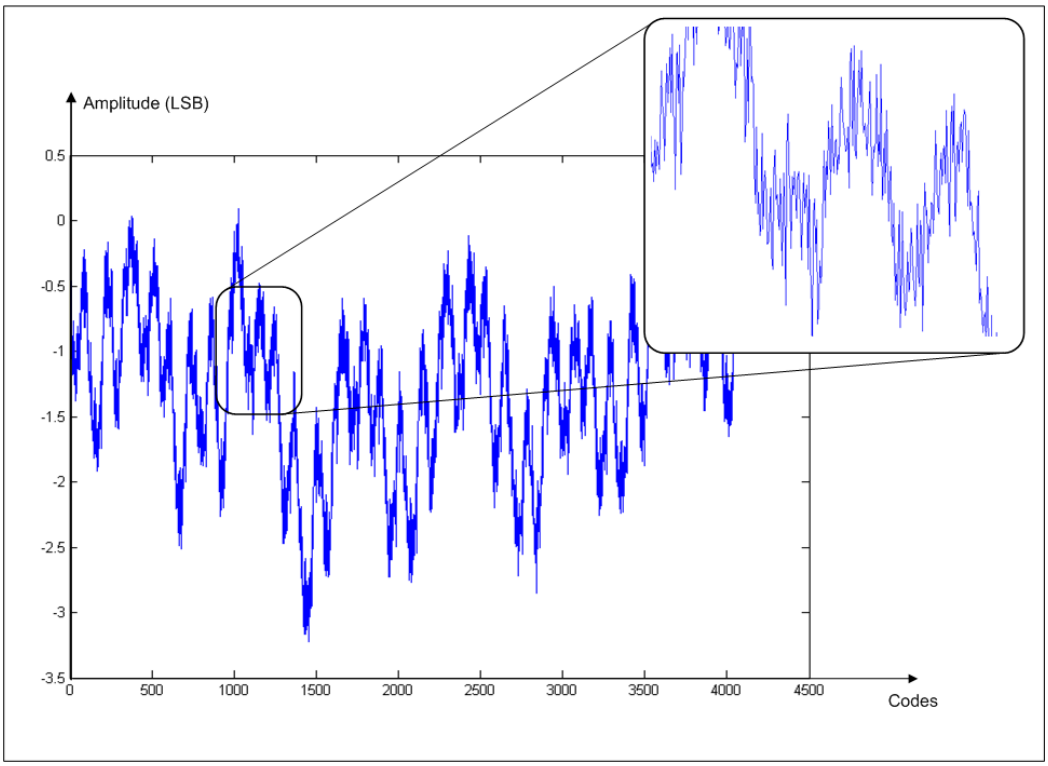

Figure 2-23: INL curve of a real-life 12-bit ADC

These INL curves are usually modelled by polynomial expressions. But as presented by Figure 2-23, an INL curve is usually made of a huge number of sharp transitions. Thus the polynomial model is limited because its number of transitions is set by its order, and this order is limited. As a consequence, considering sharp transitions, an interesting model would be a Fourier series expansion [jani06] [kerz06_2]. The only constraint relative to this series expansion is the need of periodicity of the expanded signal. In order to address this requirement, let us consider a periodic expansion of the INL function:

$$\begin{cases} INL(x),\ 0 \le x \le 2^R - 1 \\ INL(x + p.2^R) = INL(x),\ p \in Z \end{cases} \quad \textbf{eq. 2-35}$$

where x=0…2^R-1 is the digital code of the converter. The Fourier series expansion of the INL can be expressed by

$$INL(x) \approx \frac{a_0}{2} + \sum_{m=1}^{2^R-1} \left\{ a_m \cos\left(2\pi \frac{l}{2^R} x\right) + b_m \sin\left(2\pi \frac{l}{2^R} x\right) \right\} \quad \textbf{eq. 2-36}$$

where the discrete Fourier series coefficients a_m and b_m are

$$\begin{cases} a_m = \frac{1}{2^R} \sum_{x=0}^{2^R-1} INL(x) \cos\left(2\pi \frac{m}{2^{Res}} x\right) & m \in \{0,1,\ldots,2^{Res}-1\} \\ b_m = \frac{1}{2^R} \sum_{x=0}^{2^R-1} INL(x) \sin\left(2\pi \frac{m}{2^{Res}} x\right) & m \in \{1,\ldots,2^{Res}-1\} \end{cases} \quad \textbf{eq. 2-37}$$

As a consequence, the signal that is disturbed by the conversion can be modelled by:

$$s(n) = x(n) + INL(x(n)) + \varepsilon(n) \qquad \textbf{eq. 2-38}$$

$$s(n) = x(n) + \frac{a_0}{2} + \sum_{m=1}^{2^R-1} a_m \cos\left[2\pi m\left(\frac{V_{in}}{V_{FS}}\right)\cos(\theta_n) + 2\pi m\left(\frac{V_{DC}}{V_{FS}}\right)\right] + \sum_{m=1}^{2^R-1} b_m \sin\left[2\pi m\left(\frac{V_{in}}{V_{FS}}\right)\cos(\theta_n) + 2\pi m\left(\frac{V_{DC}}{V_{FS}}\right)\right] + \varepsilon(n) \qquad \textbf{eq. 2-39}$$

s(n) is the expression of a signal disturbed by distortion and noise. It can be modified using the following expressions:

$$\begin{cases} \cos[\alpha\cos(p)] = J_0(\alpha) + 2\sum_{h=1}^{\infty} J_{2h}(\alpha)(-1)^h \cos(2hp) \\ \sin[\alpha\cos(p)] = 2\sum_{h=0}^{\infty} J_{2h+1}(\alpha)(-1)^h \cos[(2h+1)p] \end{cases} \qquad \textbf{eq. 2-40}$$

where $J_h(x)$ is the h order Bessel function

$$J_h(x) = \sum_{n=0}^{\infty} \frac{(-1)^n x^{h+2n}}{n!(n+h)!2^{h+2n}} \qquad \textbf{eq. 2-41}$$

As a consequence s(n) can be expressed by

$$s(n) = x(n) + \sum_{k\geq 0} Hconv_k^{amp} \cos(k(\theta_n + \theta_i)) + \varepsilon(n) \qquad \textbf{eq. 2-42}$$

where $Hconv_k^{amp}$ represents the harmonic distortion number k for input signal of an amplitude equal to amp. The analytical expression of $Hconv_k^{amp}$ is given by:

$$\begin{cases} Hconv_{2k'}^{amp} = \underset{k'\geq 1}{2(-1)^{k'}} \sum_{k=1}^{2^R-1} [a_m \cos(m\alpha_2) + b_m \sin(m\alpha_2)] J_{2k'}(m\alpha_1) \\ Hconv_{2k'+1}^{amp} = \underset{k'\geq 0}{2(-1)^{k'}} \sum_{k=1}^{2^R-1} [b_m \cos(t\alpha_2) - a_m \sin(t\alpha_2)] J_{2k+1'}(m\alpha_1) \end{cases} \qquad \textbf{eq. 2-43}$$

where

$$\alpha 1 = 2\pi \frac{V_{in}}{V_{FS}}, \alpha_2 = 2\pi \frac{V_{DC}}{V_{FS}} \qquad \textbf{eq. 2-44}$$

Eq. 2-43 gives the expression of a sine wave deteriorated by several types of errors and particularly nonlinearities. This mathematical development is based on the assumption of a static behaviour of nonlinearities. These nonlinearities induce some harmonics characterized by amplitude and phase.

Theoretical developments have demonstrated that the phase of the harmonics products can be directly linked to the phase of the input signal. Indeed the phase of the k-order harmonic is equal to the phase of the input signal, θ_i, multiplied by the order of the harmonics. Experiments have shown that this characteristic of harmonics is not always verified. As a consequence in order to complete our converter model and to consider the worst case, we add a parameter that is an additional phase, $\theta_{conv,k}^{amp}$,

relative to each harmonic and each converter. As a consequence, s(n), the model of a sine wave disturbed by a converter, can be expressed by:

$$s(n) = x(n) + \sum_{k \geq 0} Hconv_k^{amp} \cos\left(k\left(\theta_n + \theta_i\right) + \theta_{conv,k}^{amp}\right) + \varepsilon(n) \qquad \textbf{eq. 2-45}$$

Now considering a general case of a periodic signal s(t) with pulsation ω, its Fourier decomposition is given by:

$$s(t) = a_0 + \sum_{k=1}^{\infty}\left[a_k \cos(k\omega t) + b_k \sin(k\omega t)\right] \qquad \textbf{eq. 2-46}$$

This equation can be rewritten by

$$s(t) = S_0 + \sum_{k=1}^{\infty} S_k \cos(k\omega t + \varphi_k) \qquad \textbf{eq. 2-47}$$

with

$$S_0 = a_0,\ a_k = S_k \cos(\varphi_k),\ b_k = -S_k \sin(\varphi_k) \qquad \textbf{eq. 2-48}$$

Eq.2-47 is the Fourier decomposition of a time-domain signal s(t).
The sampling is coherent and consequently respects the following expression

$$Nf_{in} = Mf_s \qquad \textbf{eq. 2-49}$$

with N number of samples, M number of periods, f_{in} the frequency of the sampled signal and f_s the sampling frequency. According to eq.2-49:

$$\omega t = 2\pi f_{in} t = 2\pi \frac{M}{N} f_s t = 2\pi \frac{M}{N} n \qquad \textbf{eq. 2-50}$$

As a consequence, the discrete Fourier decomposition of a discrete signal s(n) is given by:

$$s(n) = S_0 + \sum_{k=1}^{\infty} S_k \cos\left(k2\pi \frac{M}{N} n + \varphi_k\right) \qquad \textbf{eq. 2-51}$$

which may be rewritten as

$$s(n) = S_0 + \sum_{k=1}^{\infty} S_k \cos(k\varphi_n + \varphi_k) \qquad \textbf{eq. 2-52}$$

with

$$\varphi_n = 2\pi \frac{M}{N} n \qquad \textbf{eq. 2-53}$$

In a real case the FFT computation of a discrete signal gives the estimations $\hat{S}_k$ and $\hat{\varphi}_k$, that are the measures of the harmonic modules and phases disturbed by the noise of the signal.

$$\hat{s}(n) = \hat{S}_0 + \sum_{k=1}^{\infty} \hat{S}_k \cos\left(k\varphi_n + \hat{\varphi}_k\right) \qquad \textbf{eq. 2-54}$$

The FFT measurement expression (eq. 2-55) and the model of a signal deteriorated by a conversion (eq. 2-50) are linked. The following table gives the relations between the parameters of these two expressions.

FFT measurement results		Converter output model
φ_n		θ_n
$\hat{\varphi}_k$	⟺	$k\theta_i + \theta_{conv,k}^{Amp}$
$\hat{S}_0$	⟺	$2^R \frac{V_{DC}}{V_{FS}} + Hconv_0^{Amp} + \varepsilon_0$
$\hat{S}_1$	⟺	$2^R \frac{V_{IN}}{V_{FS}} + Hconv_1^{Amp} + \varepsilon_1$
$\hat{S}_k \quad \forall k \geq 2$	⟺	$Hconv_k^{Amp} + \varepsilon_k \quad \forall k \geq 2$

Table 2-1: Comparison between FFT measurement results and the parameters of the converter output model

Where $\varepsilon_0, \varepsilon_1$ and ε_k are the noise contributions.

According to Table 2-1, as we focus on harmonics estimation, the significant parameters from the model of sine wave disturbed by conversion (eq. 45) are $Hconv_k^{Amp} + \varepsilon_k$ and $k\theta_i + \theta_{conv,k}^{amp}$. As the influence of noise on harmonic amplitude is reduced for harmonics significantly over the noise level, we can limit the model to the following expression:

$$s(n) = x(n) + \sum_{k \geq 0} Hconv_k^{amp} \cos\left(k\theta_n + \theta_{conv,k}^{amp}\right) \qquad \textbf{eq. 2-55}$$

Eq. 2-55 is the mathematical expression that we are going to use to define the signal at the output of a converter. We can use this model for an ADC and for a DAC.

IV.2.B DAC/ADC chain model

Let us consider a DAC/ADC chain, and a sine wave as test signal. In order to stimulate all the codes of the converters, the test signal amplitude should match the full-scale of both converters. As a result, considering eq. 2-55, the output signal of the converter can be expressed by eq. 2-56, where the *conv* index is equal to *dac* because this is the output of a DAC and the index amp is equal to FS because the amplitude of the test signal reaches the full-scale of the converter.

$$s(n) = x(n) + \sum_{k \geq 0} Hdac_k^{FS} \cos\left(k\theta_n + \theta_{dac,k}^{FS}\right) \qquad \textbf{eq. 2-56}$$

It is to notice that the DAC output is a time-continuous signal and the expression used to describe this signal is discrete. We assume for any DAC test configuration, the DUT output signal should be digitized before being analysed. As a consequence the proposed mathematical expression for the DAC output becomes correct.

We state two hypotheses concerning the ADC:

1. . The full-scale input voltage of the ADC is equal to the full-scale output voltage of the DAC; as a consequence, the same test signal can be used for the DAC and the ADC.

2. The input signal of the ADC is composed of a sine wave and some errors (harmonic distortions and noise). Except when the DAC exhibits some catastrophic errors, the ADC is sourced with a sine wave with a sufficiently wide dynamic range. In other words, the noise and the harmonic contribution of the DAC do not disturb the ADC behaviour. As a consequence, the output signal of the ADC can be modelled by:

$$s(n) = x(n) + \sum_{k\geq 0} Hdac_k^{FS} \cos\left(k\left(\theta_n + \theta_i\right) + \theta_{dac,k}^{FS}\right) + \sum_{k\geq 0} Hadc_k^{FS} \cos\left(k\left(\theta_n + \theta_i\right) + \theta_{adc,k}^{FS}\right) \quad \textbf{eq. 2-57}$$

By expanding eq. 2-57, we obtain:

$$s(n) = x(n) + \sum_{k\geq 0} \begin{Bmatrix} \left[Hdac_k^{FS} \cos\left(k\theta_i + \theta_{dac,k}^{FS}\right) + Hadc_k^{FS} \cos\left(k\theta_i + \theta_{adc,k}^{FS}\right)\right]\cos\left(k\theta_n\right) \\ -\left[Hdac_k^{FS} \sin\left(k\theta_i + \theta_{dac,k}^{FS}\right) + Hadc_k^{FS} \sin\left(k\theta_i + \theta_{adc,k}^{FS}\right)\right]\sin\left(k\theta_n\right) \end{Bmatrix} \quad \textbf{eq. 2-58}$$

with

$$\begin{aligned} Re\left(H_k^m\right) &= Hdac_k^{FS} \cos\left(k\theta_i + \theta_{dac,k}^{FS}\right) + Hadc_k^{FS} \cos\left(k\theta_i + \theta_{adc,k}^{FS}\right) \\ Im\left(H_k^m\right) &= -Hdac_k^{FS} \sin\left(k\theta_i + \theta_{dac,k}^{FS}\right) - Hadc_k^{FS} \sin\left(k\theta_i + \theta_{adc,k}^{FS}\right) \end{aligned} \quad \textbf{eq. 2-59}$$

where H_k^m is the harmonic number k, measured at the output of the ADC.

The real part of the measured harmonic k results from the combination of

- ✓ The real part of harmonic contribution from DAC, $Hdac_k^{FS} \cos\left(k\theta_i + \theta_{dac,k}^{FS}\right)$
- ✓ The real part of harmonic contribution from ADC, $Hadc_k^{FS} \cos\left(k\theta_i + \theta_{adc,k}^{FS}\right)$

The imaginary part of the measured harmonic k results from the combination of

- ✓ The imaginary part of harmonic contribution from DAC, $-Hdac_k^{FS} \sin\left(k\theta_i + \theta_{dac,k}^{FS}\right)$
- ✓ The imaginary part of harmonic contribution from ADC, $-Hadc_k^{FS} \sin\left(k\theta_i + \theta_{adc,k}^{FS}\right)$

As a consequence, as presented by Figure 2-24, there is a potential fault masking.

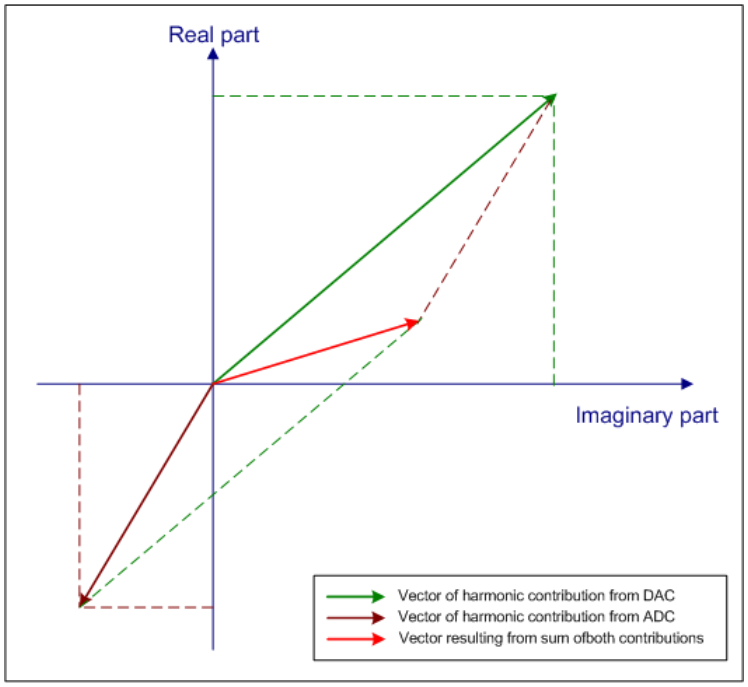

Figure 2-24: Sum of two harmonic contributions

As the harmonics are complex values, Figure 2-24 gives a vector description of these harmonics. We can see that the sum of two harmonic contributions can give a resulting harmonic smaller than each contribution.

In addition, according to eq. 2-59, the measure of harmonics at the output of the converter gives two results (real and imaginary part) and 4 unknown variables (real and imaginary parts of DAC and ADC) by harmonic. In other words, we have a 2-equation system with four unknowns. As a consequence, the system cannot be solved and the harmonic contributions from both converters cannot be discriminated.

IV.3 Conclusion and opening

Using embedded components of a system to test the converters of this system, and precisely connecting DACs and ADCs in series in order to test their dynamic parameters simultaneously is an interesting solution. Concerning noise, we have found in the literature an interesting method that could be used in a complex system test environment [cauv00]. Dealing with harmonics, we have introduced a model of test signal deteriorated by both converters of a DAC/ADC chain. Eq. 2-59 gives the model of harmonics measured at the output of a DAC/ADC chain. The mathematical expression for one harmonic is made of two equations and four unknown variables. The two equations are the real and imaginary parts of the harmonic. The unknown variables are the real and imaginary parts of the harmonic contributions of both converters. As a result, it is obviously impossible to solve this equation system and discriminate the harmonic contributions of both converters.

Despite of this problem, connecting DACs and ADCs in a complex system in order to test their dynamic parameters is a very interesting solution. Let's keep modelling by an equation system the harmonics measured at the output of DAC/ADC chains. As we have two equations and four unknown variables, we just need two additional equations with the same unknown variables in order to obtain a solvable equation

system. New equations mean new tests using the same converters. It is to notice that the harmonic contribution of a converter is linked to the test signal characteristics and especially its amplitude. As a result, the test signal should reach the full-scale of the converter. In addition, if we want the same unknown variables in our new equations, we should use the same test signals.

Thus we want new equations, so new tests, but we need to use the same converters and the same test signals. As a consequence, the only solution to have new equations would be to vary the test path or configuration. But there is no other possible test path than connecting in series the DAC and the ADC. As a result, it is not possible to obtain a solvable equation system using only one DAC and one ADC. The solution is to use not only one DAC and one ADC but also all the potential test paths using all the converters to test in the complex system. The next section deals with this method to test a set of converters interconnected in a complex system.

V Method to discriminate harmonic contributions of interconnected converters

V.1 Introduction to Analogue Network of Converters

Let us consider a complex system embedding several DACs and ADCs. In order to implement a fully digital test of these converters, there are a significant number of potential test paths. Indeed the output of any DAC can be connected to the input of any ADC. But this is not the only possible fully digital test path. Two DAC outputs can be combined and connected to an ADC input. All the potential test paths are conceptualized by the Analogue Network of Converters or ANC presented by Figure 2-25.

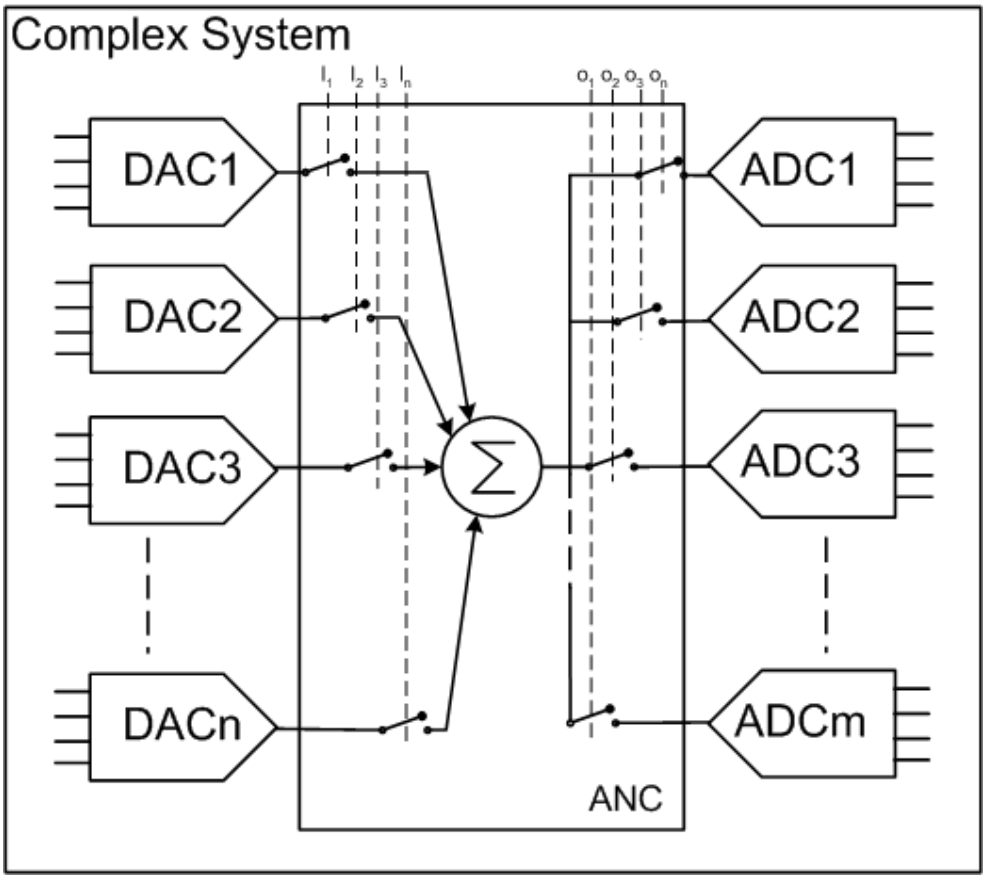

Figure 2-25: Analogue Network of Converters in a complex system

According to the ANC representation (see Figure 2-25), a lot of test paths can be implemented. When n DACs are connected with m ADCs, this is called a configuration C(n,m). The simplest configuration is C(1,1). According to eq. 2-59, using only a C(1,1) configuration in order to test its DAC and ADC is ineffective, due to the limited number of potential test paths and consequently tests. As a consequence, we are going to focus not only on one DAC and one ADC but on the test of two DACs and one ADC, as presented by Figure 2-26.

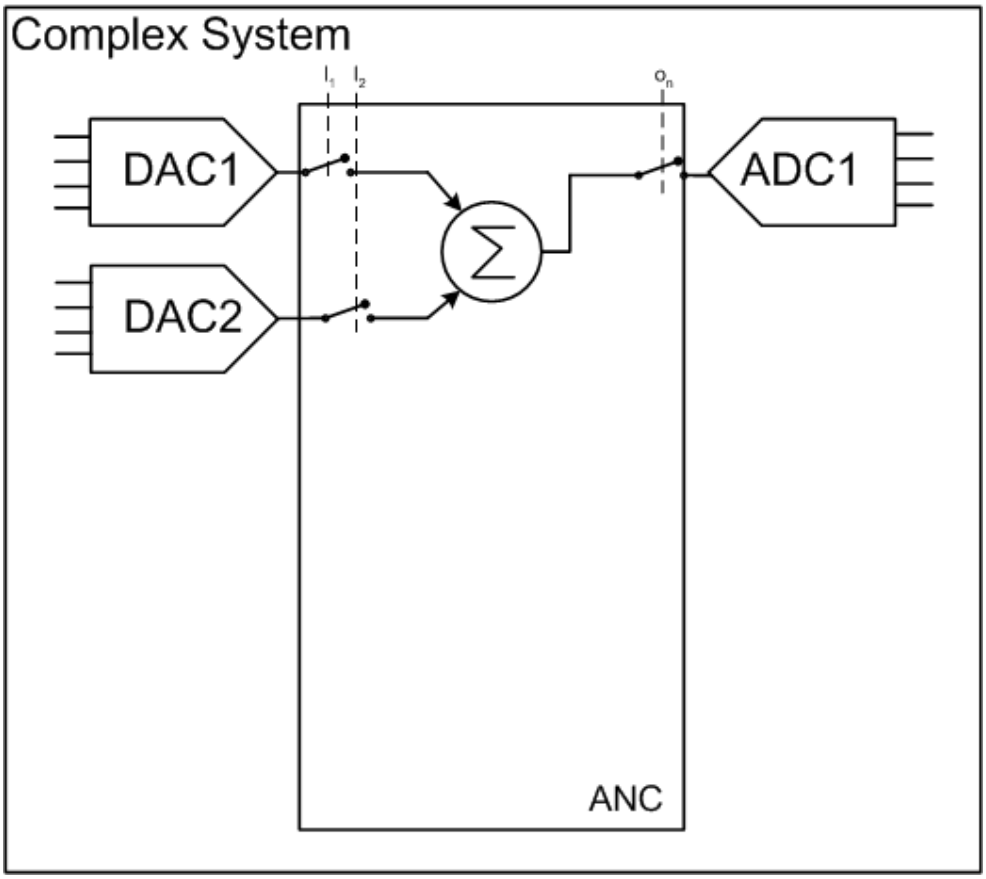

Figure 2-26: Two DACs and one ADC interconnection using ANC

The first step would consist in testing these three converters. The second step of the global method would be to generalize this approach to the test of the whole set of potential converters embedded in a complex system.

V.2 Two DACs and one ADC

The ANC principle uses different hardware configurations in terms of converter interconnections. Then, the idea is to find adequate test setup – i.e. test paths and test signals – to discriminate the influence of each converter on the final response. In practice, the only test setup parameters we can easily control are the phase and the amplitude of the digital stimulus. In this section, two configurations, using DAC1, DAC2 and ADC1, are studied in order to discriminate their harmonic contributions.

V.2.A Configuration C(1,1) at full-scale

The first configuration considered is made up of a single DAC and a single ADC (Figure 2-27).
According to the harmonic contribution model of eq. 2-57 and considering a null initial phase θ_i, the influence of the two data converters on the sampled signal can be expressed by:

$$s(n) = x(n) + \sum_{k\geq 0} \begin{Bmatrix} \left[Hdac1_k^{FS} \cos\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS} \cos\left(\theta_{adc1,k}^{FS}\right) \right] \cos(\theta_n) \\ -\left[Hdac1_k^{FS} \sin\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS} \sin\left(\theta_{adc1,k}^{FS}\right) \right] \sin(\theta_n) \end{Bmatrix} \quad \textbf{eq. 2-60}$$

where $Hdac1_k^{FS}\cos\left(\theta_{dac,k}^{FS}\right)$ and $-Hdac1_k^{FS}\sin\left(\theta_{dac,k}^{FS}\right)$ are respectively the real and imaginary parts of the k[th] harmonic contribution of DAC1 for an input signal reaching the converter full-scale. These are the variables we want to know in order to estimate the harmonic contribution of DAC1. In addition, $Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right)$ and $-Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right)$ are respectively the real and imaginary parts of the k[th] harmonic contribution of ADC1 for an input signal reaching the converter full-scale, with an initial phase equal to zero. These are the variables we want to know in order to estimate the harmonic contribution of ADC1. It is to notice that, in this study, we consider that all the converters have the same dynamic range.

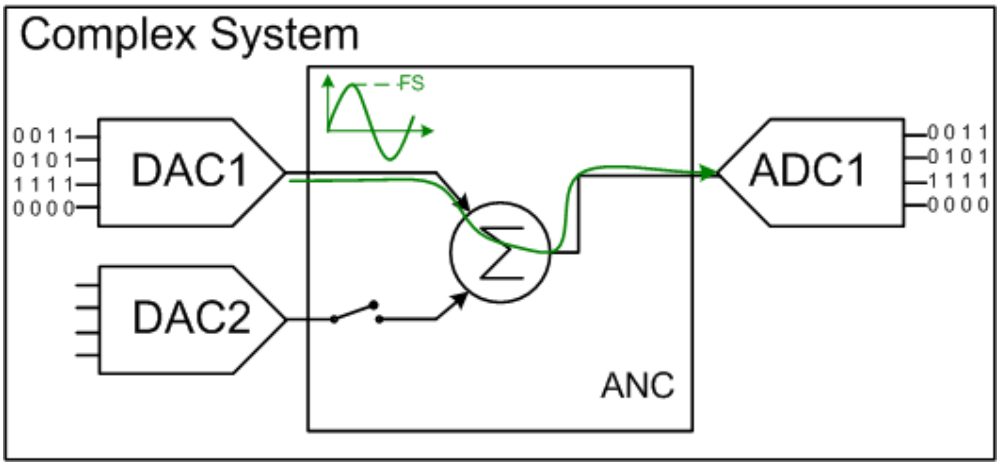

Figure 2-27: C(1,1) test configuration

If we consider DAC1, DAC2 and ADC1, C(1,1) configuration at full-scale can be applied twice:

- ✓ Through DAC1, ADC1
- ✓ Through DAC2, ADC1

For the first case, let us consider $H_k^{m,a}$, the k[th] harmonic measured on the ADC output. The real and imaginary parts of this measure can be modelled by:

$$\begin{aligned} Re\left(H_k^{m,a}\right) &= Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\ Im\left(H_k^{m,a}\right) &= -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \end{aligned} \qquad \textbf{eq. 2-61}$$

In the second step, the test path goes through DAC2 and ADC1. The amplitude of the test signal still reaches the full-scale of the converters. Therefore, we obtain a second set of two equations given by eq. 2-62, where $H_k^{m,b}$ is the amplitude of the k[th] harmonic measured on ADC output.

$$\begin{aligned} Re\left(H_k^{m,b}\right) &= Hdac2_k^{FS}\cos\left(\theta_{dac2,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\ Im\left(H_k^{m,b}\right) &= -Hdac2_k^{FS}\sin\left(\theta_{dac2,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \end{aligned} \qquad \textbf{eq. 2-62}$$

At this point, we have six unknown parameters (real and imaginary parts of harmonic contributions from DAC1, DAC2 and ADC1) and only four equations (eq. 2-61 and eq. 2-62).

One could think of playing with the amplitude and phase of the input signal to establish new equations. Unfortunately, variations of these test setup parameters give no additional independent information to discriminate the influence of each converter on the final response. Indeed, the input signal phase has no influence on the converter harmonic contribution and even if the input signal amplitude A_{in} modifies the converter harmonic contribution ($Hdac1_k^{A_{in}} \neq Hdac1_k^{FS}$ if $A_{in} \neq FS$), each new acquisition would give a new equation but also two new unknown parameters ($Hdac1_k^{A_{in}}, Hadc1_k^{A_{in}}$).

To avoid this problem, the two DAC outputs can be added to establish a new configuration. This new configuration is called C(2,1) and is described in the next section.

V.2.B Configuration C(2,1) at full-scale

The second hardware configuration is made up of two DACs and one ADC. The input of the ADC is the sum of the two DAC outputs.

Unfortunately, considering three converters with the same resolutions, the sum of two full-scale signals from DAC1 and DAC2 with no relative phase shift is twice the converter full-scale and would saturate the ADC.

The solution to overcome this problem is to introduce a relative phase shift of $2\pi/3$ between the two input signals (Figure 2-28).

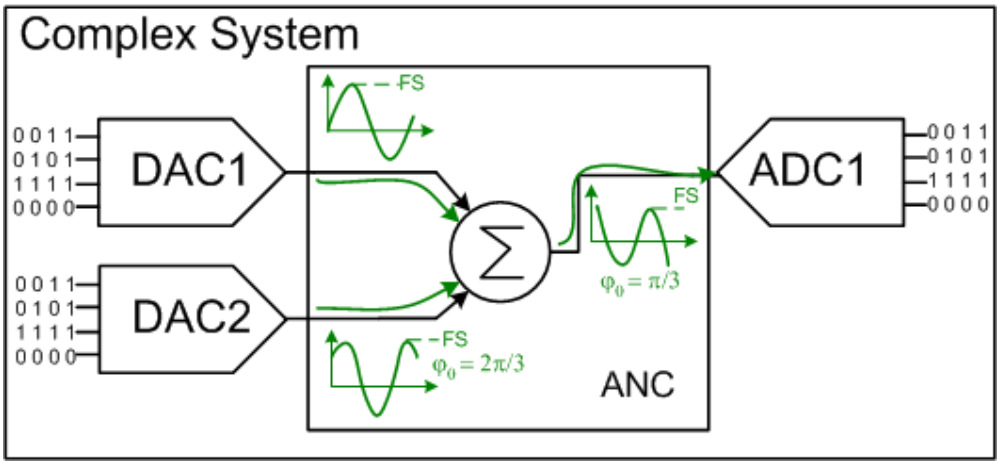

Figure 2-28: Third test setup

The sum of the two DAC outputs is a full-scale signal; this property is mathematically explained by eq. 2-63.

$$\cos\left(x+\frac{2\pi}{3}\right)+\cos(x)=2\cos\left(x+\frac{\pi}{3}\right)\cos\left(\frac{\pi}{3}\right)=\cos\left(x+\frac{\pi}{3}\right) \qquad \textbf{eq. 2-63}$$

We obtain eq. 2-64 that gives the third set of two equations: eq. 2-65.

$$s(n)=x(n)+\sum_{k=0}^{\infty} Re\left(H_k^{m,c}\right)\cos(k\theta_n)+Im\left(H_k^{m,c}\right)\sin(k\theta_n) \qquad \textbf{eq. 2-64}$$

and

$$Re\left(H_k^{m,c}\right)=\left[\begin{array}{l} Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+ \\ Hdac2_k^{FS}\left[\cos\left(k\frac{2\pi}{3}\right)\cos\left(\theta_{dac2,k}^{FS}\right)-\sin\left(k\frac{2\pi}{3}\right)\sin\left(\theta_{dac2,k}^{FS}\right)\right]+ \\ Hadc1_k^{FS}\left[\cos\left(k\frac{\pi}{3}\right)\cos\left(\theta_{adc1,k}^{FS}\right)-\sin\left(k\frac{\pi}{3}\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{array}\right] \quad \textbf{eq. 2-65}$$

$$Im\left(H_k^{m,c}\right)=-\left[\begin{array}{l} Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)+ \\ Hdac2_k^{FS}\left[\sin\left(k\frac{2\pi}{3}\right)\cos\left(\theta_{dac2,k}^{FS}\right)+\cos\left(k\frac{2\pi}{3}\right)\sin\left(\theta_{dac2,k}^{FS}\right)\right]+ \\ Hadc1_k^{FS}\left[\sin\left(k\frac{\pi}{3}\right)\cos\left(\theta_{adc1,k}^{FS}\right)+\cos\left(k\frac{\pi}{3}\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{array}\right]$$

where $H_k^{m,c}$ is the amplitude of the k[th] harmonic measured on the ADC output. Finally, considering the three sets of two equations (eq. 2-61, eq. 2-62 and eq. 2-65), we obtain a 6-equation system for each k[th] harmonic contribution:

$$\left\{\begin{array}{l} Re\left(H_k^{m,a}\right)=Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\ Im\left(H_k^{m,a}\right)=-Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)-Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \\ Re\left(H_k^{m,b}\right)=Hdac2_k^{FS}\cos\left(\theta_{dac2,k}^{FS}\right)+Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\ Im\left(H_k^{m,b}\right)=-Hdac2_k^{FS}\sin\left(\theta_{dac2,k}^{FS}\right)-Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \\ Re\left(H_k^{m,c}\right)=\left[\begin{array}{l} Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+ \\ Hdac2_k^{FS}\left[\cos\left(k\frac{2\pi}{3}\right)\cos\left(\theta_{dac2,k}^{FS}\right)-\sin\left(k\frac{2\pi}{3}\right)\sin\left(\theta_{dac2,k}^{FS}\right)\right]+ \\ Hadc1_k^{FS}\left[\cos\left(k\frac{\pi}{3}\right)\cos\left(\theta_{adc1,k}^{FS}\right)-\sin\left(k\frac{\pi}{3}\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{array}\right] \\ Im\left(H_k^{m,c}\right)=-\left[\begin{array}{l} Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)+ \\ Hdac2_k^{FS}\left[\sin\left(k\frac{2\pi}{3}\right)\cos\left(\theta_{dac2,k}^{FS}\right)+\cos\left(k\frac{2\pi}{3}\right)\sin\left(\theta_{dac2,k}^{FS}\right)\right]+ \\ Hadc1_k^{FS}\left[\sin\left(k\frac{\pi}{3}\right)\cos\left(\theta_{adc1,k}^{FS}\right)+\cos\left(k\frac{\pi}{3}\right)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{array}\right] \end{array}\right. \quad \textbf{eq. 2-66}$$

This system would enable the discrimination of the harmonic contribution of every converter if the three equations were independent. This condition is not verified for harmonic components that are of a prime order and greater than three, i.e. 5, 7, 9, 11,

13… Indeed for these harmonics, the third equation is a linear combination of the two other equations.

We have observed a similar limitation whatever the relative phase shift introduced between the two input signals. So, this 3-equation system permits to discriminate the 3 first harmonics, but is not sufficient to calculate the THD or the SFDR. To go further and discriminate more harmonics, it is necessary to vary the input signal amplitude, as described in following sections.

V.2.C Configuration C(1,1) and C(2,1) at half -scale

The second parameter we can control is the input signal amplitude. As previously explained, the use of different amplitudes induces additional unknown parameters. Nevertheless, it also introduces new test setup possibilities that can be exploited to get additional independent useful information.

Practically, we have looked for a system of equations that allows the discrimination of the three converter harmonic contributions, $Hdac1_k^{FS}, Hdac2_k^{FS}, Hadc1_k^{FS}$ using test stimuli with amplitude at full-scale and amplitude at half -scale, as presented by Figure 2-29.

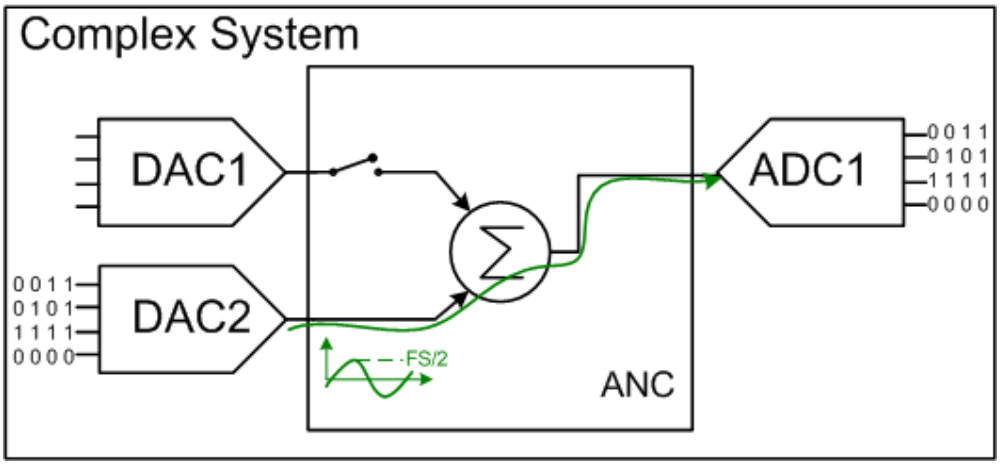

Figure 2-29: New third test setup

The new third set of two equations is the result of a test at half-scale through DAC2 and ADC1 (eq. 2-67). The measured harmonics are the sum of DAC2 and ADC1 harmonic contributions for an input signal at half -scale.

$$\begin{aligned} Re\left(H_k^{m,c}\right) &= Hdac2_k^{FS/2}\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right) \\ Im\left(H_k^{m,c}\right) &= -Hdac2_k^{FS/2}\sin\left(\theta_{dac2,k}^{FS/2}\right) - Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right) \end{aligned} \qquad \textbf{eq. 2-67}$$

Due to this test, we have 10 unknown variables and only 6 equations. To solve the system we need to have the same number of unknowns and equations. As a consequence, C(2,1) configuration with both amplitude and phase variations is used to establish the two last equations. The fourth test setup involves a full-scale input signal on DAC1 and a half -scale input signal on DAC2 with a ⦸ phase shift (Figure 2-30). The resulting signal at the ADC input is a sine wave at half -scale as described by eq. 2-68:

$$\cos(x)+\frac{\cos(x+\pi)}{2}=\cos(x)-\frac{\cos(x)}{2}=\frac{\cos(x)}{2} \qquad \textbf{eq. 2-68}$$

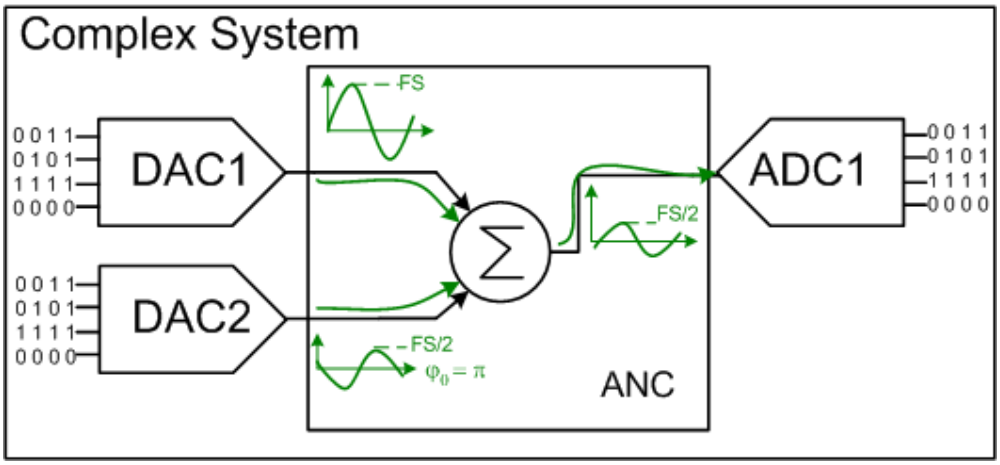

Figure 2-30: Fourth test setup

The resulting equation is the sum of the harmonic contribution at full-scale of DAC1, the harmonic contribution at half-scale of DAC2 balanced by the phase shift and the harmonic contribution at half-scale of ADC1.

$$s(n)=x(n)+\sum_{k=0}^{\infty}\left[Re\left(H_k^{m,d}\right)\cos(k\theta_n)+Im\left(H_k^{m,d}\right)\sin(k\theta_n)\right] \qquad \textbf{eq. 2-69}$$

where

$$\begin{aligned} Re\left(H_k^{m,d}\right)&=Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right)+Hdac2_k^{FS/2}\cos(k\pi)\cos\left(\theta_{dac2,k}^{FS/2}\right)+Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right)\\ Im\left(H_k^{m,d}\right)&=-Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right)-Hdac2_k^{FS/2}\cos(k\pi)\sin\left(\theta_{dac2,k}^{FS/2}\right)-Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right)\end{aligned} \qquad \textbf{eq. 2-70}$$

The fifth and last required test is very similar to the previous one. The input amplitudes are the same but they are relatively phase shifted of φ_1. The resulting signal at the ADC input is now a sine wave at full-scale with a phase shift of φ_2, as presented by eq. 2-71 and eq. 2-72.

$$\cos(x)+\frac{\cos(x+\varphi_1)}{2}=\cos(x+\varphi_2) \qquad \textbf{eq. 2-71}$$

$$\textbf{with } \varphi_1=\pi-ar\cos\left(\frac{1}{4}\right),\varphi_2=\pi-2ar\cos\left(\frac{1}{4}\right) \qquad \textbf{eq. 2-72}$$

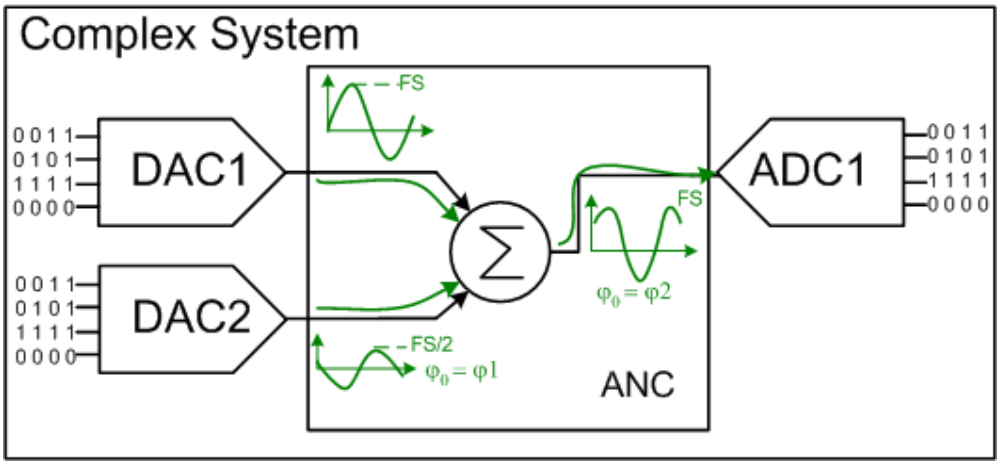

Figure 2-31: Fifth test setup

The fifth equation then corresponds to the sum of the harmonic contributions balanced by their phase shift:

$$s(n) = x(n) + \sum_{k=0}^{\infty}\left[Re\left(H_k^{m,e}\right)cos(k\theta_n) + Im\left(H_k^{m,e}\right)sin(k\theta_n)\right] \qquad \textbf{eq. 2-73}$$

with

$$Re\left(H_k^{m,e}\right) = \begin{bmatrix} Hdac1_k^{FS}\, cos(\theta_{dac1,k}^{FS}) + \\ Hdac2_k^{FS/2}\left[cos(k\phi_1)cos\left(\theta_{dac2,k}^{FS/2}\right) - sin(k\phi_1)sin\left(\theta_{dac2,k}^{FS/2}\right)\right] + \\ Hadc1_k^{FS}\left[cos(k\phi_2)cos\left(\theta_{adc1,k}^{FS}\right) - sin(k\phi_2)sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{bmatrix}$$

$$Im\left(H_k^{m,e}\right) = -\begin{bmatrix} Hdac1_k^{FS}\, sin\left(\theta_{dac1,k}^{FS}\right) + \\ Hdac2_k^{FS/2}\left[sin(k\phi_1)cos\left(\theta_{dac2,k}^{FS/2}\right) + cos(k\phi_1)sin\left(\theta_{dac2,k}^{FS/2}\right)\right] + \\ Hadc1_k^{FS}\left[sin(k\phi_2)cos\left(\theta_{adc1,k}^{FS}\right) + cos(k\phi_2)sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{bmatrix} \qquad \textbf{eq. 2-74}$$

In summary, the proposed test strategy is composed of five successive tests. Each test consists in an acquisition and a spectral analysis (with Fast Fourier Transform) to evaluate harmonic bins. For each test we measure the real and imaginary parts of each harmonic. For each part we have an equation for which the unknown variables are the harmonic contributions of each converter from the concerned test configuration, i.e. test setup and test signals. For five tests we obtain a 10-equation system for each harmonic bin:

$$
\begin{cases}
Re\left(H_k^{m,a}\right) = Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\
Im\left(H_k^{m,a}\right) = -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \\
Re\left(H_k^{m,b}\right) = Hdac2_k^{FS}\cos\left(\theta_{dac2,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\
Im\left(H_k^{m,b}\right) = -Hdac2_k^{FS}\sin\left(\theta_{dac2,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \\
Re\left(H_k^{m,c}\right) = Hdac2_k^{FS/2}\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right) \\
Im\left(H_k^{m,c}\right) = -Hdac2_k^{FS/2}\sin\left(\theta_{dac2,k}^{FS/2}\right) - Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right) \\
Re\left(H_k^{m,d}\right) = Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hdac2_k^{FS/2}\cos(k\pi)\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right) \\
Im\left(H_k^{m,d}\right) = -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hdac2_k^{FS/2}\cos(k\pi)\sin\left(\theta_{dac2,k}^{FS/2}\right) - Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right) \\
Re\left(H_k^{m,e}\right) = \begin{bmatrix} Hdac1_k^{FS}\cos(\theta_{dac1,k}^{FS}) + \\ Hdac2_k^{FS/2}\left[\cos(k\phi_1)\cos\left(\theta_{dac2,k}^{FS/2}\right) - \sin(k\phi_1)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right] + \\ Hadc1_k^{FS}\left[\cos(k\phi_2)\cos\left(\theta_{adc1,k}^{FS}\right) - \sin(k\phi_2)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{bmatrix} \\
Im\left(H_k^{m,e}\right) = -\begin{bmatrix} Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) + \\ Hdac2_k^{FS/2}\left[\sin(k\phi_1)\cos\left(\theta_{dac2,k}^{FS/2}\right) + \cos(k\phi_1)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right] + \\ Hadc1_k^{FS}\left[\sin(k\phi_2)\cos\left(\theta_{adc1,k}^{FS}\right) + \cos(k\phi_2)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{bmatrix}
\end{cases}
\qquad \textbf{eq. 2-75}
$$

This system of independent equations is sufficient to calculate the real and imaginary parts of harmonic contribution at full-scale of the three converters. Once real and imaginary parts are known, the modules of the three contributions, $Hdac1_k^{FS}, Hdac2_k^{FS}, Hadc1_k^{FS}$, can be computed, in order to calculate THD and SFDR for the three converters. It allows thus a fully independent characterization of the three converters of the C(2,1) configuration in terms of harmonic contributions.

V.3 **Generalization**

V.3.A Basic principle

The first step consists in using C(2,1) and C(1,1) configurations to characterize the three first converters (DAC1, DAC2 and ADC1). Five consecutive tests are necessary in order to characterize these three converters.

The generalization of the method is based on two ideas.

At first, by using an already characterized converter, we can characterize an additional one with only one test. For instance, DAC1 can be used to characterize the harmonic contribution of an uncharacterized ADCi using one digital stimulus at full-scale. This test gives the following equation system:

$$
\begin{aligned}
Re\left(H_k^{m,j}\right) &= Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hadci_k^{FS}\cos\left(\theta_{adci,k}^{FS}\right) \\
Im\left(H_k^{m,j}\right) &= -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hadci_k^{FS}\sin\left(\theta_{adci,k}^{FS}\right)
\end{aligned}
\qquad \textbf{eq. 2-76}
$$

We have a 2-equation system, with only two unknown variables:

✓ The real part of harmonic contributions from ADCi, $Hadci_k^{FS}\cos\left(\theta_{adci,k}^{FS}\right)$

✓ The imaginary part of harmonic contributions from ADCi, $-Hadci_k^{FS}\sin\left(\theta_{adci,k}^{FS}\right)$

The other parameters of the system are the real and imaginary parts of the total harmonic terms and the real and imaginary parts of DAC1 harmonic contributions, which have been characterized previously. As a consequence by solving this simple 2-equation system, we are able to estimate the harmonic contribution from ADCi.

The first step requires five consecutive tests in order to test two DACs and one ADC. These tests don't involve consistently all the three converters. In addition the test approach requires only some digital resources of the ATE and these digital options are usually numerous in the ATE. As consequence it possible to do some additional tests in parallel of the five tests required for the first step. Let's consider the first basic idea from the generalization and the potential parallel tests. Thus the second fundamental idea from the generalization is to perform some parallel tests during the five tests required for the first step, in order to test additional converters as described by the first idea of the generalization.

V.3.B Generalization example

For instance, let us consider the ANC presented by Figure 2-32. This is a set of 5 DACs and 5 ADCs interconnected. The network of interconnections would be defined according to the tests that should be done.

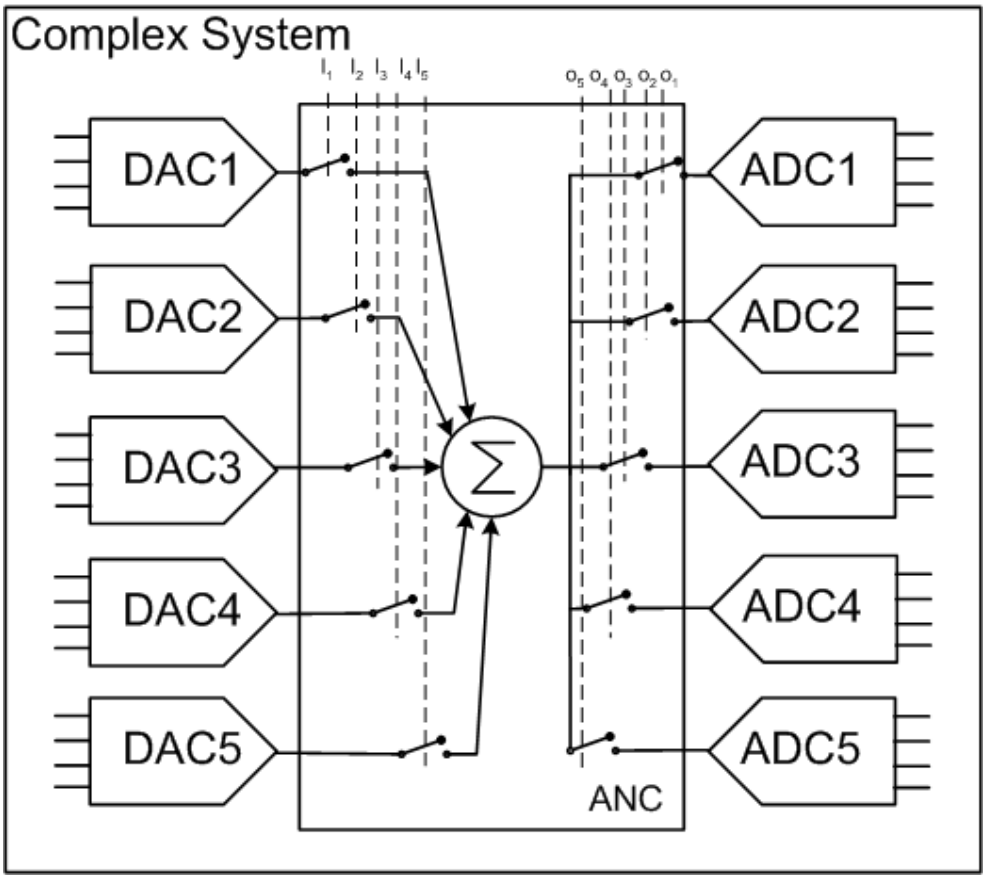

Figure 2-32: ANC made of 5 DACs and 5 ADCs

Figure 2-33 gives a temporal description of the test configurations that would be used in order to test this set of 10 converters. There are two kinds of tests:

- ✓ Test configurations for the first step of the method, used to characterize DAC1, DAC2 and ADC1 thanks to eq. 2-76.
- ✓ Additional test configurations for the generalization of the method in order to test the seven other converters. Only one test per converter is required to additionally test DAC3 to DAC5 and ADC2 to ADC5, and parallel testing can be used.

The time unit is one test. One test is equal to the time required to test one converter with a classical approach. We assume that this time is equivalent to the time for a C(1,1) or C(2,1) test. Indeed, the same number of samples has to be captured and processed in both cases, and the additional processing required to solve the equation systems is negligible compared to the acquisition and FFT time.

In the first time slot, two tests are performed simultaneously. The test configurations are DAC1/ADC1 and DAC2/ADC2. The results of the DAC1/ADC1 are exploited in the estimation of DAC1, DAC2, and ADC1 parameters (i.e. test first step), while the results of DAC2/ADC2 will help characterize ADC2, when DAC2 parameters are known.

In the second time slot, three tests are achieved using DAC2/ADC1, DAC1/ADC3 and DAC3/ADC2 configurations. The first test is part of the process for estimating DAC1, DAC2, and ADC1, and the two additional tests permit to characterize ADC3 and DAC3.

The remaining tests necessary to compute all the converter parameters are similarly performed in the subsequent time slots.

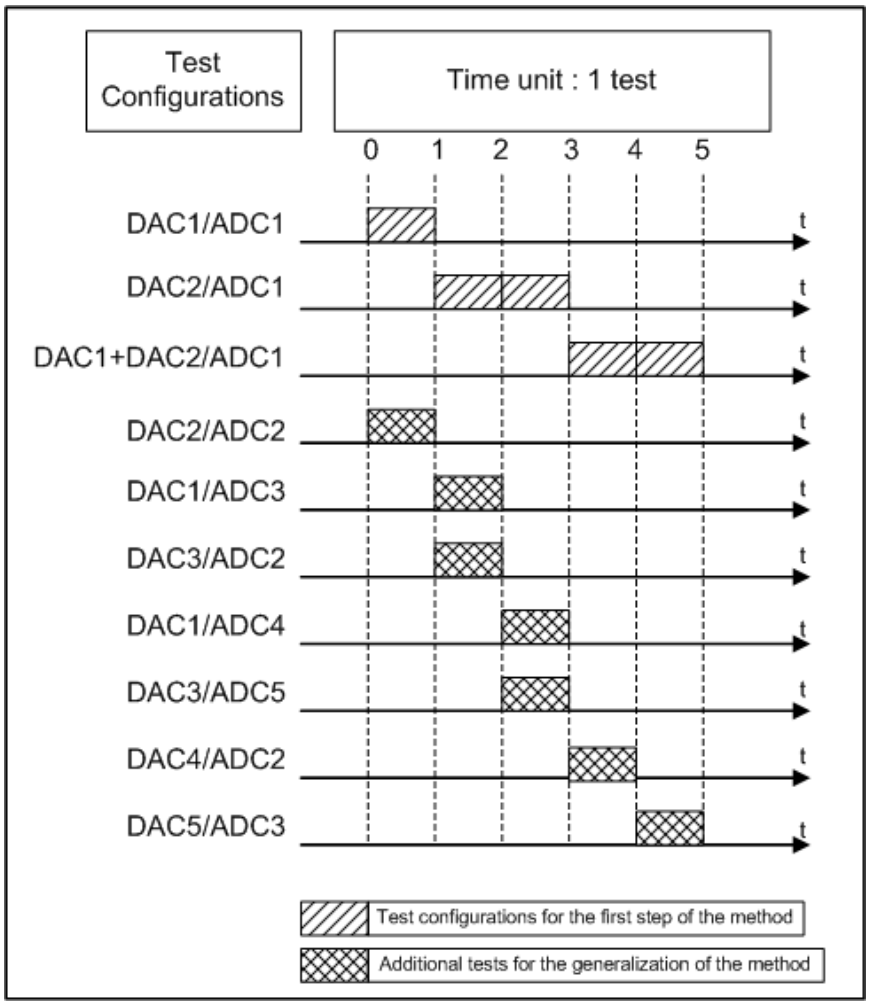

Figure 2-33: Temporal description of the test configurations for the generalization of the method

At the end of the process, for a total test time of five elementary tests, the distortion of ten converters can be computed. This test time is incompressible because five tests are required for the first step of the method, which cannot be done in parallel as far as the same converter ADC1 is involved in the five tests. In comparison, a conventional test approach that requires high performance ATE and performs each converter test independently and consecutively would last ten elementary tests. As a conclusion, besides requiring only digital test instruments, the proposed test approach reduces the test time to approximately half the conventional test time.
Obviously this generalization example shows a possible process that can be elaborated in order to reduce the test time. The generalization depends on the number of converters to test, their specifications and the number of digital pins available on the tester. As a consequence, a generalization should be elaborated for each practical case. But it appears clearly that using this test method helps reducing the test time of a set of converters embedded in a SiP or SoC.

VI Conclusion

The study on test methods presented in this chapter proves that the fully digital test of a set of converters in a complex system is possible. Concerning static parameters several solutions can be considered. At first a lot of methods, also called Built-In-Self-

Test solutions, have been developed over the past few years. Another solution could be to take advantage of the link between static and dynamic parameters. Indeed several studies have been published concerning this subject. According to these publications the INL curve could be estimated using the results of harmonic distortion measurements. Considering all these potential solutions for static parameter estimation, we focused on dynamic parameters. Dynamic parameters are computed using measurements of noise and harmonic distortions induced by the DUT. There exists a published method that could suit to our test conditions. This method allows the discrimination of the noise contributions from one DAC and two ADCs in a fully digital test configuration [cauv00]. Considering this effective solution to measure the noise, the resulting bottleneck towards a fully digital test of converters in a complex system is to estimate their harmonic distortions. As a result, we have proposed a test method in order to achieve a fully digital estimation of harmonic distortions from embedded converters. This method avoids several issues from conventional test methods. At first, as mentioned previously, it avoids the need of analogue instruments. Indeed, only digital instruments are required on the test platform because the test method re-uses some embedded components in order to do the interface between analogue and digital domains. In addition, this method also addresses the issue of test time. Indeed, the conventional test of all the converters embedded in a system requires a long test time because they are tested consecutively. The generalization of our method proves that the test time can be reduced, for instance for a set of 5 DACs and 5 ADCs we can reduce to half the global test time.
Next chapter addresses the validation of this novel method.

Chapter 3

Validation of the ANC-based method

I Introduction

The theoretical developments described in the second chapter deal with a fully digital test of converters embedded in a complex system. The approach is based on an "Analogue Network of Converters" also called an ANC. The principle of the ANC consists in interconnecting DACs and ADCs in the analogue domain in order to apply fully digital tests to these converters. By using the ANC, we could be able to sum any DAC outputs and drive the signal to any ADC. A test method, based on this ANC, has been developed. The purpose of this method is to measure the harmonic distortion contributions from all the converters embedded in the system.

The purpose of this third chapter is to validate the theoretical developments by evaluating the efficiency of this new test method. The efficiency will be considered in terms of accuracy for the estimation of some dynamic parameters according to converter resolutions and performances. The validation is conducted in two steps: simulation results are presented in the second section and hardware measurement results in the third section.

II Simulation results

A large number of experiments based on simulation have been performed to validate the proposed approach. In this section, the converter model used for simulation is first introduced, then the simulation setup is defined, and finally experimental results are presented. The performance of the proposed test strategy is discussed in terms of estimation error on dynamic parameters.

II.1 **Converter model**

In order to simulate the proposed test method, we need to establish a converter model that takes into account possible non-idealities. In line with the converter errors described in the second section of chapter 2, four main sources of errors will be considered:

- ✓ Sampling jitter of the converter
- ✓ Thermal noise
- ✓ Non-linearity of the transfer function
- ✓ Quantization noise.

Firstly, let us consider a sine wave $v_i(t)$ used as stimulus for the test of ADCs described by the following mathematical expression:

$$v_i(t) = V_0 \cos(2\pi f_0 t + \Phi) \qquad \textbf{eq. 3-1}$$

where V_0, f_0, Φ are respectively the amplitude, the frequency and the phase of the sine wave.

In order to achieve coherent sampling, N samples are collected on M cycles of the signal with a sampling frequency f_s following the equation:

$$f_s = (N/M) f_0 \qquad \textbf{eq. 3-2}$$

It is important to notice that M and N should be integer and prime with each other.

II.1.A Sampling jitter

The signal affected by sampling jitter can be described by the following expression:

$$v(n) = V_0 \cos(\theta_n + J_n) \quad \forall n \in I \qquad \textbf{eq. 3-3}$$

considering

$$\theta_n = 2\pi \frac{M}{N} n + \Phi \qquad \textbf{3-4}$$

where J_n is the noise phase affecting the sampling signal.

$$J_n = 2\pi f_0 \delta_{tn} \qquad \textbf{eq. 3-5}$$

δ_{tn} is the random variable associated to the sampling event n. We can consider that δ_{tn} follows a white noise distribution defined by its standard deviation σ_j.
By realizing a first order Taylor series expansion of the sampled expression, we obtain:

$$v(n) = V_0 \cos(\theta_n) + \varepsilon_n \quad \forall n \in I \qquad \textbf{eq. 3-6}$$

$$\text{with } \varepsilon_n = -\varphi_n J_n \quad \forall n \in I \qquad \textbf{eq. 3-7}$$

$$\varphi_n = V_0 \sin(\theta_n) \quad \forall n \in I \qquad \textbf{eq. 3-8}$$

As the standard deviation, σ_j, of the phase noise is modulated by the sinus, the power of the noise induced is σj^2. Figure 3-1 depicts a 1kHz sine wave sampled at f_s=16.384MHz and deteriorated by a jitter with a standard deviation of 5ps, and the difference between this deteriorated sine wave and a pure one. In other words, it is the jitter noise affecting the sine wave.

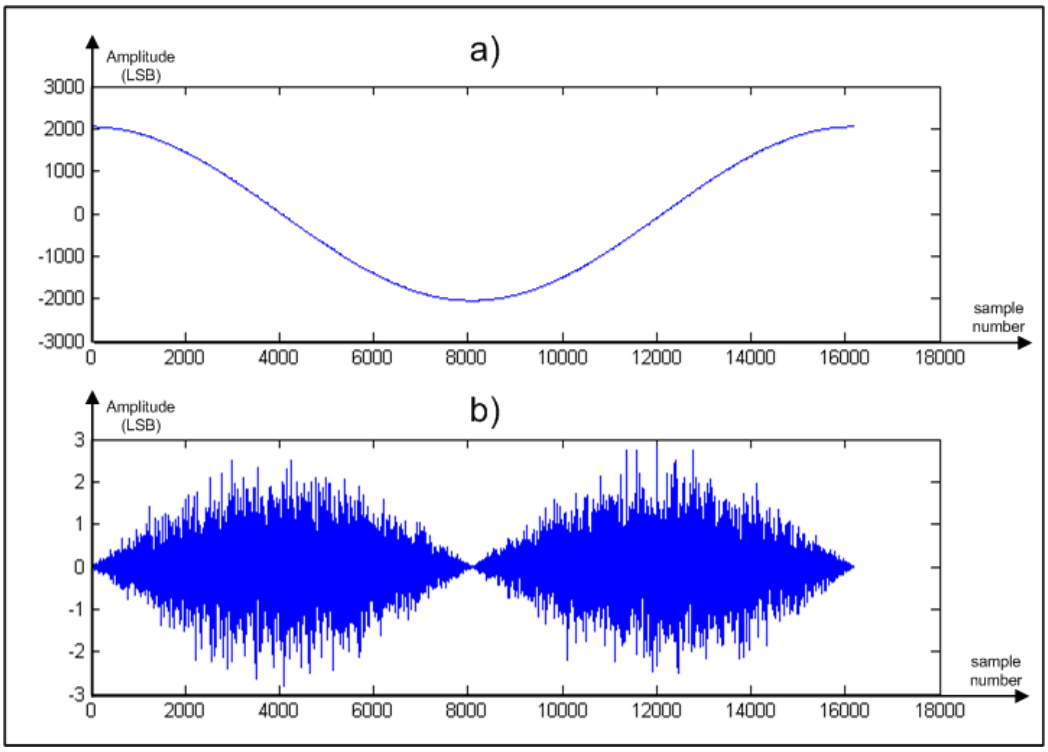

Figure 3-1: a) 1kHz sine wave sampled at f_s=163.84MHz and deteriorated by a sampling jitter with standard deviation of 5ps
b) difference between the deteriorated sine wave from a) and a pure sine wave

We observe that, while the input signal affected by jitter is a cosine, the jitter noise is modulated by a sinus function. This observation goes in favour of the model of jitter noise given by eq. 3-8.

II.1.B Thermal noise

The second stochastic error is the thermal noise. The model of the thermal noise is a white noise following a centred Gaussian distribution, defined by a standard deviation. The mathematical expression of the test signal deteriorated by errors can be updated as given by eq. 3-9 and 3-10:

$$v(n) = V_0 \cos(\theta_n) + \varepsilon_n \quad \forall n \in I \qquad \textbf{eq. 3-9}$$

$$\text{with } \varepsilon_n = -\varphi_n J_n + N_{Th} \quad \forall n \in I \qquad \textbf{eq. 3-10}$$

where N_{th} is the thermal noise.

II.1.C Non-linearity

Non-linearities are described by a curve, the so-called INL curve. In order to include the non-linearity perturbations into the model of the converted signal, the description of the INL curve has to be simple. This INL curve is usually described by a polynomial expression or a Fourier series expansion [xu99] [jani06] [kerz06_2]. Figure 3-2 presents examples of INL curve fitting based on these two different techniques. To allow the comparison of the two techniques, the same numbers of parameters is used. The first fitting technique is based on a 80th order polynomial, and

the Fourier series expansion is realized with 40 odd and 40 even Fourier coefficients. This number of parameters seems acceptable keeping model integration in mind.

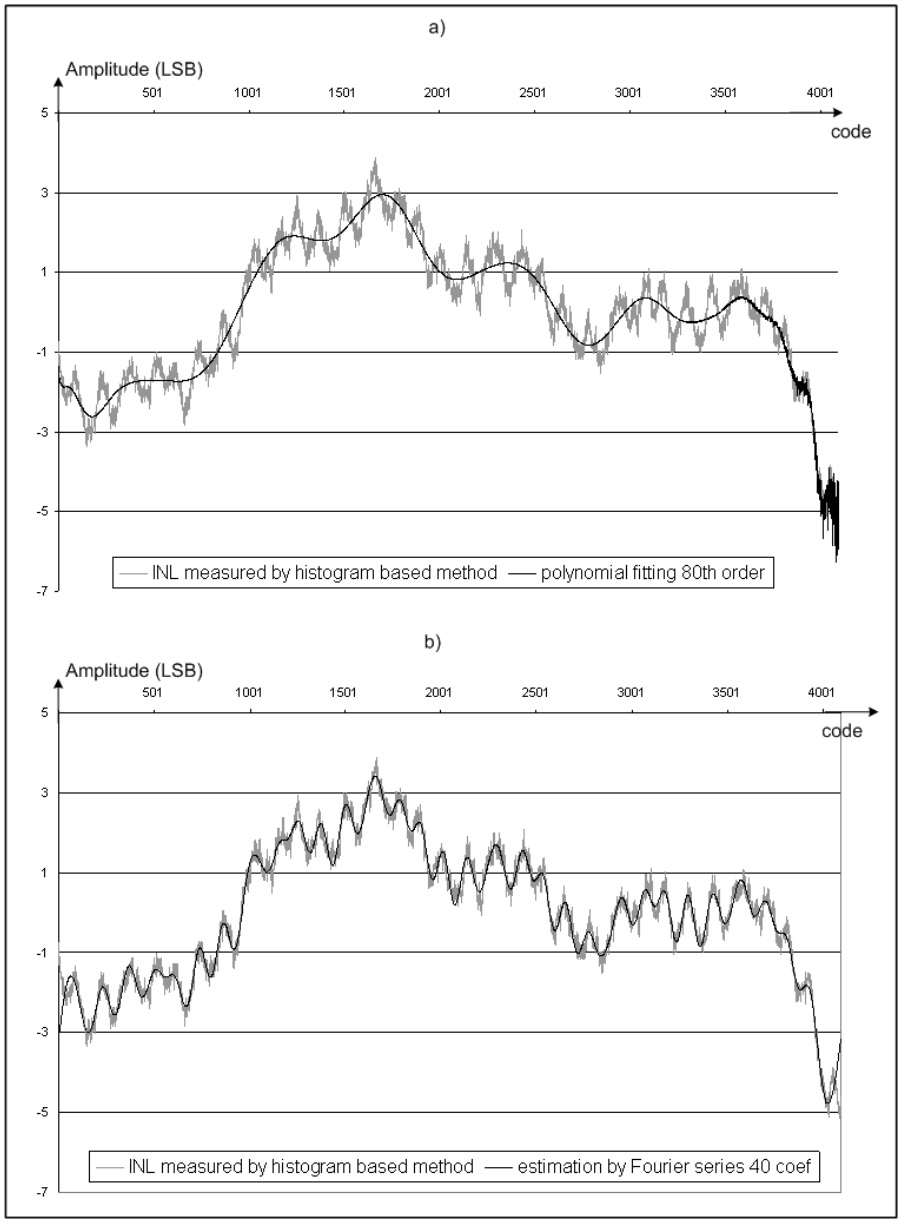

Figure 3-2: INL curve model a) comparison between an INL curve and its 80th order polynomial fitting b) comparison between an INL curve and its Fourier series expansion, the series development is made with 40 odd and 40 even Fourier coefficients

According to Figure 3-2, the problem of a model based on polynomial is the poor description of the sharp transitions [kerz06_2]. Indeed, the number of transitions described cannot exceed the order of the polynomial. As illustrated in Figure 3-2, for the same number of parameters, the Fourier series expansion gives a more accurate description of the curve. However, it seems difficult to give a very accurate description of an INL curve and its sharp transitions using a model. In order to

overcome this limitation, we have decided to use "true" INL curve measured on converters using a conventional histogram method.

II.1.D Final model

Consequently, let us consider v(n) given by eq. 3-10 as the signal deteriorated by the two first types of errors: sampling jitter and thermal noise. Eq. 3-12 gives the expression of the signal deteriorated by the whole set of considered errors.

$$s(n) = [v(n) + INL([v(n)])] \qquad \textbf{eq. 3-11}$$

where INL(x) is a non-linearity curve measured through histogram testing of a real converter. This non-linearity curve is indexed by [v(n)], the rounded expression of v(n). The complete equation is rounded to model the last non-ideality: the quantization effect. Consequently eq. 3-11 gives s(n), the mathematical expression of a sine wave deteriorated during the conversion by four types of errors: sampling jitter, thermal noise, non-linearities of the converter transfer function and quantization noise. This mathematical expression is the foundation expression used to validate the test method by simulation.

II.2 Simulation setup and strategy

The ANC-based test approach for a set of ADCs and DACs in a complex system is made of two steps. The first step is the C(2,1) configuration depicted in Figure 3-3. It involves two DACs and one ADC. The DAC outputs are summed; the resulting sum is driven to the ADC input. The second step consists in using previously tested converters to a direct test of the remaining untested converters, using a simple one DAC / one ADC test set-up. Because the set-up is simpler and the proposed test method is less sensitive to this second step, we have decided to focus on the validation of the first step.

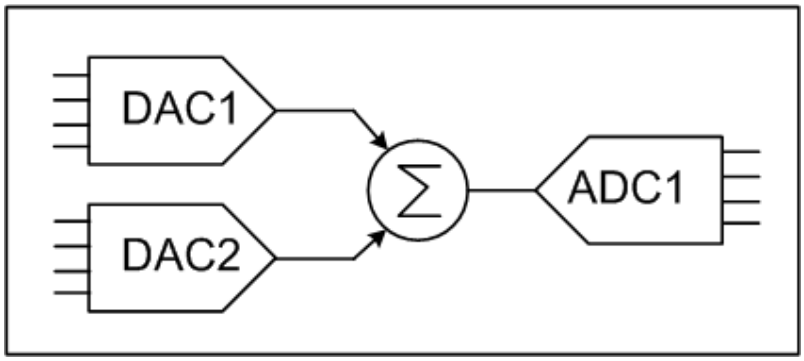

Figure 3-3: C(2,1) configuration

Several sets of simulation have been carried out. They are based on the converter model previously described. We assume that the three converters have the same full-scale and that the additional circuitry required for the test has no influence on harmonic measurements. These assumptions will be discussed in the section of experimental validations.

The purpose of the first step of the ANC-based method is to discriminate the harmonic contributions from the three converters. The method requires five captures using five different sets of input test signals.

The test signals are sine waves with the same frequency (the frequency given by the datasheet for the test of dynamic parameters) and different amplitudes. When two input signals are driven simultaneously through DAC1 and DAC2, their relative phase shift is also a varying parameter. The characteristics of the test signals required for the five captures of the first step are summarized in Table 3-1.

Capture number	DAC1 input signal amplitude	DAC2 input signal amplitude	Relative phase shift between DAC1 and DAC2 input signals (rad)
1	*Full-scale*	-	-
2	-	*Full-scale*	-
3	-	*Half -scale*	-
4	*Full-scale*	*Half -scale*	$\varnothing$
5	*Full-scale*	*Half -scale*	*1.8235*

Table 3-1: Characteristics of the test signals required for the five captures of the first step.

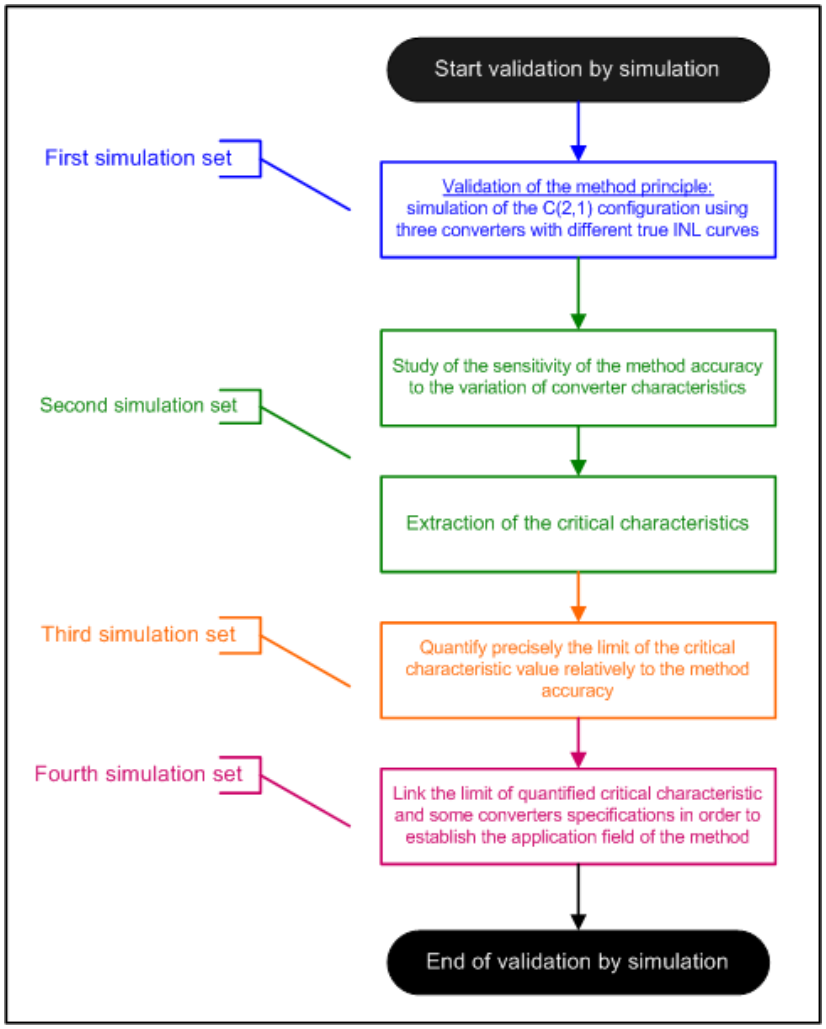

Figure 3-4: Simulation strategy in order to validate the test approach

Based on the C(2,1) configuration, the idea is to vary performances of ADC and DACs to assess the application field of our method. As described in chapter 2, converters are characterized by a set of parameters (static and dynamic). For our method, only dynamic parameters (SINAD, THD, ENOB, SFDR, SNR) are taken into account. Considering only dynamic parameters could obstruct the validation to address an exhaustive range of converter characteristics. Fortunately according to [jani06], static and dynamic parameters are linked. As a consequence, the solution we propose to cover the maximum of possible cases consists in playing with SNR and THD of converters. THD gives information about harmonic power and SNR informs about the noise power except harmonic power.

The method efficiency is evaluated in terms of accuracy of THD and SFDR measurement. In order to evaluate the measurement accuracy, a reference measurement has been simulated. This reference measurement is obtained by simulating high performance analogue instruments such as a digitizer for DAC testing and an AWG for ADC testing.

II.3 **Test method efficiency**

II.3.A Validation on several samples of converters

Harmonics are mainly induced by non-linearities, which are described in the converter model by an INL curve. The first validation consists in evaluating the test method efficiency using converters with different INL curves. For this, we consider the C(2,1) configuration with 12-bit converters. The complete procedure to extract the three converters' characteristics was simulated four times, using different INL curves for the three different converters at each time. Simulation results are summarized in Table 3-2 and Table 3-3 in terms of THD and SFDR of the three converters under test respectively. For each tested converter, the table gives the reference measurement (Ref), the parameter estimation using the proposed method (Est) and the difference between both (*Diff*).

Test #	DAC1			DAC2			ADC		
	Ref	Est	*Diff*	Ref	Est	*Diff*	Ref	Est	*Diff*
1	-57.70	-57.72	*0.02*	-85.41	-86.29	*0.88*	-72,31	-72,29	*-0,02*
2	-65.81	-65.66	*-0.15*	-75.18	-75.47	*0.29*	-71.62	-71.36	*-0.26*
3	-76.66	-76.58	*-0.08*	-72.69	-72.74	*0.05*	-69.17	-69.12	*-0.04*
4	-73.98	-74.00	*0.02*	-71.14	-71.08	*-0.06*	-77.44	-76.81	*-0.62*

Table 3-2: THD parameter measurement for the fifteen tested converters

Test #	DAC1			DAC2			ADC		
	Ref	Est	*Diff*	Ref	Est	*Diff*	Ref	Est	*Diff*
1	81.63	81.49	*0.15*	58.83	58.90	*-0.07*	72.22	72.46	*-0.25*
2	78.27	78.19	*0.08*	68.43	68.20	*0.23*	73.41	73.57	*-0.15*
3	72.86	72.70	*0.16*	77.99	78.35	*-0.36*	71.71	71.77	*-0.06*
4	71.70	71.11	*0.59*	74.38	74.59	*-0.21*	74.71	74.52	*0.19*

Table 3-3: SFDR parameter measurement for the fifteen tested converters

The results show that there is a maximum estimation error of 0.88dB for the THD and 0.59dB for the SFDR. This error is satisfactory in comparison with the repeatability of the traditional measurements, which is usually in an order of magnitude of 1.5dB for real-life components.

It is important to notice that a wide range of converters was simulated. Indeed SFDR goes from 58.83dB to 81.63dB, and THD from -57.7dB to -85.41dB. Specifications from commercial products are often close to 70dB for THD and -71dB for SFDR [AD9676][AD9866][TDA9910]. Therefore we can conclude, according to these simulation results, that the method is efficient to discriminate the good from the bad devices.

II.3.B Study of the test method sensitivity

The first simulation set has allowed us to conclude that the method is theoretically well developed and gives good results in terms of SFDR and THD measurement. The purpose of this second set of simulations is to vary the converter parameters to evaluate the most critical parameters for the accuracy of the proposed test method.

In this section, in order to reduce the number of test parameters to monitor, we focus on one converter over the three tested ones: the ADC. Indeed we assume that the estimation of DACs parameters will be affected in a similar manner than the estimation of the ADC parameters. This assumption will be discussed in the last section.
Experiments are performed with 14-bit converters in a C(2,1) configuration. Two different ADCs are considered, which differ by their THD and SFDR and consequently by their ENOB:

- ADC1: ENOB=12.6, SNR=82.5dB, THD=-83dB
- ADC2: ENOB=13.3, SNR=82.5dB, THD=-93dB

In order to find the most critical parameters for the accuracy of ADC parameter estimation, each ADC was tested using DACs with various values of SNR and THD. Moreover, to estimate and discriminate the influence of the THD and SNR of the DACs, we considered two cases of ENOB variations:

- DACs with THD variations: ENOB=13.3 to 4.6, SNR=82.5dB, **THD=-93 to -33dB**
- DACs with SNR variations: ENOB=12.4 to 9, **SNR=79 to 55.7dB**, THD=-83dB

Consequently, we have four sets of simulations corresponding to the two cases of variations applied during the test of the two different ADCs. Results are summarized in Figure 3-5 a) and b), which give the estimation error on THD and SFDR vs. the ENOB of DACs respectively.

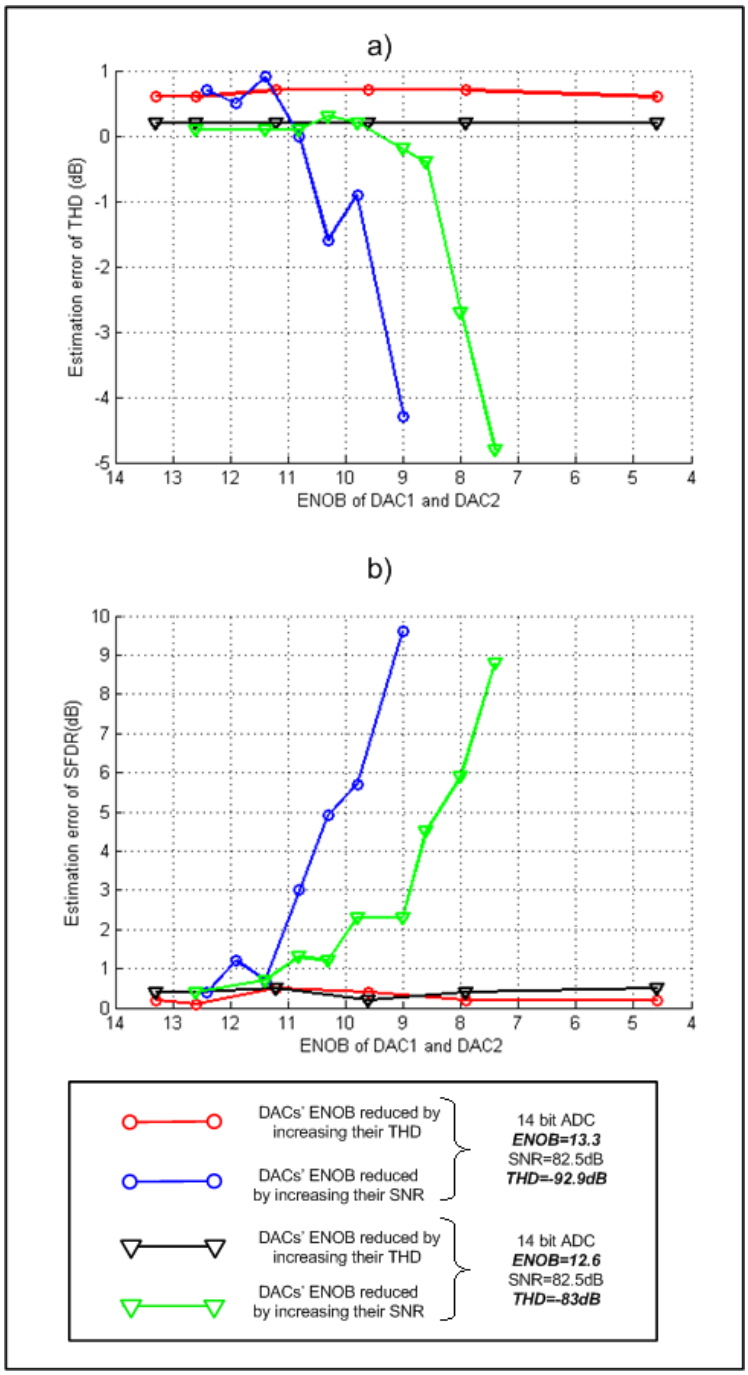

Figure 3-5: a) THD estimation error vs. ENOB of DACs b) SFDR estimation error vs. ENOB of DACs

Analyzing these results, it appears that two cases should be distinguished, i.e. i) the use of DACs with a reduced ENOB due to an increased THD and, ii) the use of DACs with a reduced ENOB due to an increased SNR.

In the first case (red and black curves), the estimation error on the ADC parameters remains almost constant and below 1dB whatever the THD of the tested ADC is. Consequently, we can conclude that the test accuracy is not influenced by the THD of the DACs used in the C(2,1) configuration. In other words, it means that even in

presence of DACs with a poor THD, we can accurately estimate the parameters ADC under test, whereas, for the existing methods described in the first and second chapters, the faults of a component in the test path can be masked by the faults from another one. Using the ANC-based method allows us to discriminate the errors of the components from the test path without fault masking.

In contrast in the second case (green and blue curves), the estimation error on the ADC parameters increases as the ENOB of DACs decrease. For these cases, the variations of the test results are caused by a decreasing SNR of the DACs. In order to go further, Figure 3-6 a) and b) give a different representation of the same results as Figure 3-5. Figure 3-6 a) and b) respectively present the estimation error of THD and SFDR versus the SNR of the DACs.

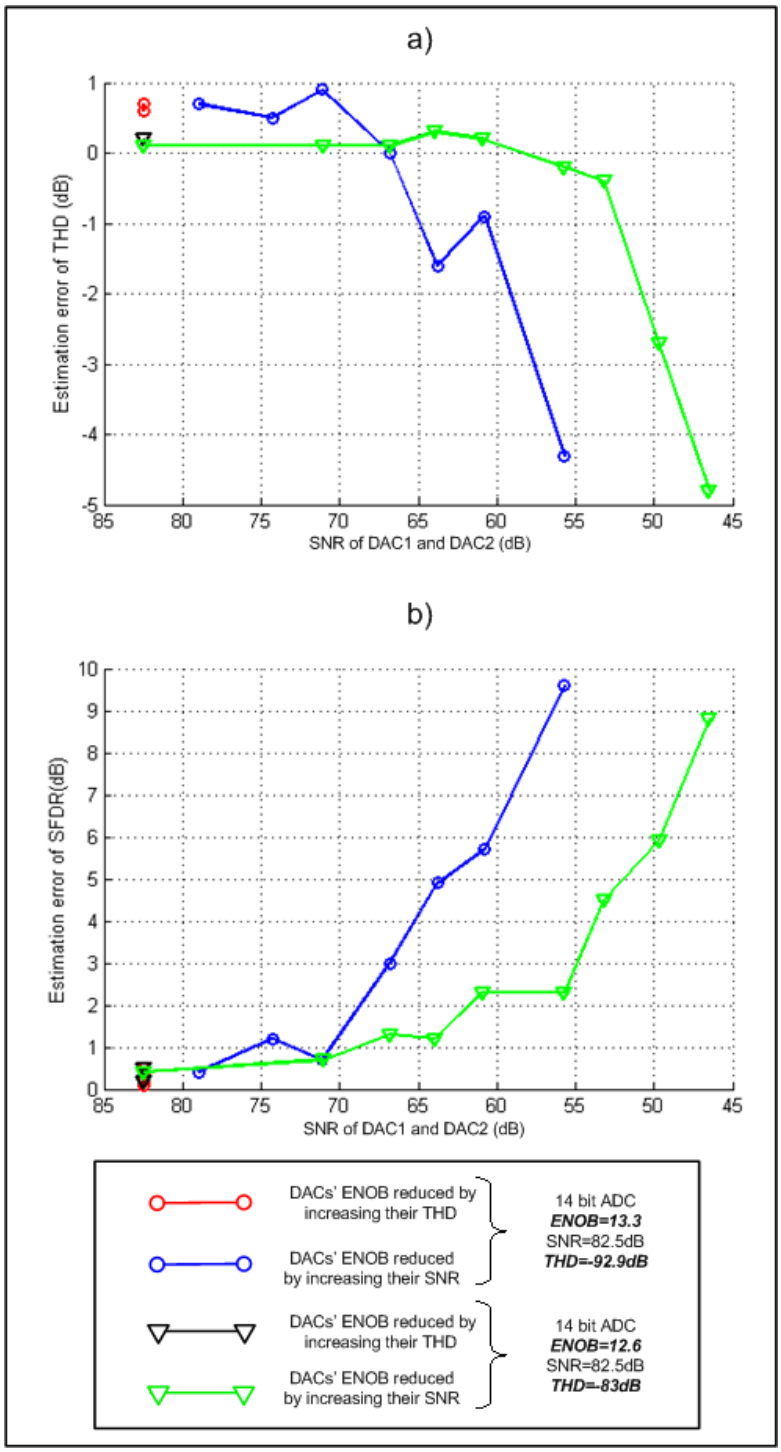

Figure 3-6: a) THD estimation error vs. SNR of DACs b) SFDR estimation error vs. SNR of DACs

To begin with, we still observe (on red and black curves) that for a constant SNR the results of the estimation of the ADC parameters are also constant, whatever the value of the THD of the DACs is. Considering the blue and green curves, it is confirmed that the noise level influences the test accuracy. Indeed, the higher the noise levels of the DACs, the higher the estimation error for both THD and SFDR of the ADC under

test. This observation can be explained by looking at the spectral representation (Figure 3-7) of a capture.

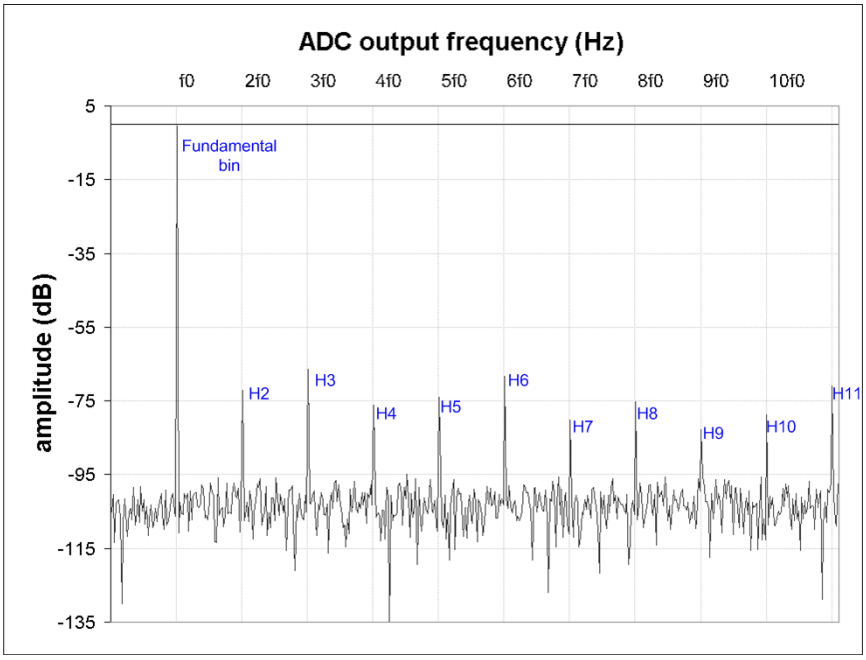

Figure 3-7: Spectrum of a signal captured at the output of a C(2,1) configuration

Let's consider Figure 3-7, the spectral representation of a signal captured at the output of a converter. As previously explained, the signal is affected by several errors. The harmonic distortions located in bins at multiple of input frequency f0 represent the first type of errors. The signal is also affected by noise. The noise contribution is spread over all bins of the spectrum, even harmonic bins. The degradation of the SNR of the DACs induces an increase of the noise level in the spectrum. Then it is easy to understand that the degradation of the SNR is reflected by a noise contribution to the amplitude of harmonic bins.

As the noise is a random phenomenon, its contribution to harmonic bins is also random and varies at every capture. When the noise floor is low enough in comparison with the harmonic amplitude, its contribution can be neglected. When the noise floor comes close to the harmonic level, its contribution becomes significant. In addition it may introduce some errors in the computation.

Now let us consider the simulation results given in Figure 3-6. The black and red lines have a constant estimation error despite of the increase of the harmonic amplitudes. Indeed in these cases, the noise contribution is negligible and there is no significant estimation error. Considering the blue and green lines, we observe different behaviours. In both cases the degradation of the SNR of the DACs induces an increase of the estimation error. However, the two cases exhibit a difference: the estimation error increases more rapidly on the blue line than on the green one. This difference can be explained by the value of the THD to be estimated. In the blue case, the ADC THD is equal to -92.9dB and in the green one, the ADC THD is equal to -83dB therefore the harmonics are more distant from the noise floor. Consequently by considering an acceptable error of 2dB in the THD estimation, the maximum

acceptable SNR for DACs is between 70 and 65dB for the blue case and between 65 and 60dB for the green one.

To conclude, it appears that the method efficiency is linked to the noise level of the captured signals. To go deeply in the analysis of this criterion, additional simulations have been realised. They are described in the next section.

II.3.C Quantitative estimation of acceptable amount of noise

The results of the previous set of simulations have shown that the converter parameter that significantly influences the accuracy of the estimation is the SNR. The purpose of this third simulation campaign is to quantify the acceptable amount of noise with respect to the result accuracy in order to define the application field of the method.
In order to quantify the noise influence on the result accuracy, two different 14-bit ADCs were considered which differ by their THD value. A good and a bad converter in terms of THD were simulated with the following characteristics:

- ✓ ADC1: ENOB=12.8, SNR=79dB, THD=-88dB
- ✓ ADC2: ENOB=12.1, SNR=79dB, THD=-78dB

Two types of DACs were used to evaluate the parameters of each ADC:

- ✓ First type of DACs: 12-bit DAC with ENOB=11 to 8, SNR=-67.5 to -50dB, THD=-93dB
- ✓ Second type of DACs: 10-bit DAC with ENOB=9.7 to 7.7, SNR=-60 to -48dB, THD=-87.8dB

The critical parameter, i.e. the DAC SNR, was varied to evaluate the accuracy of our estimation method.
Figure 3-8 a) and b) give the estimation error of the THD and the SFDR of the ADC versus the DACs SNR.

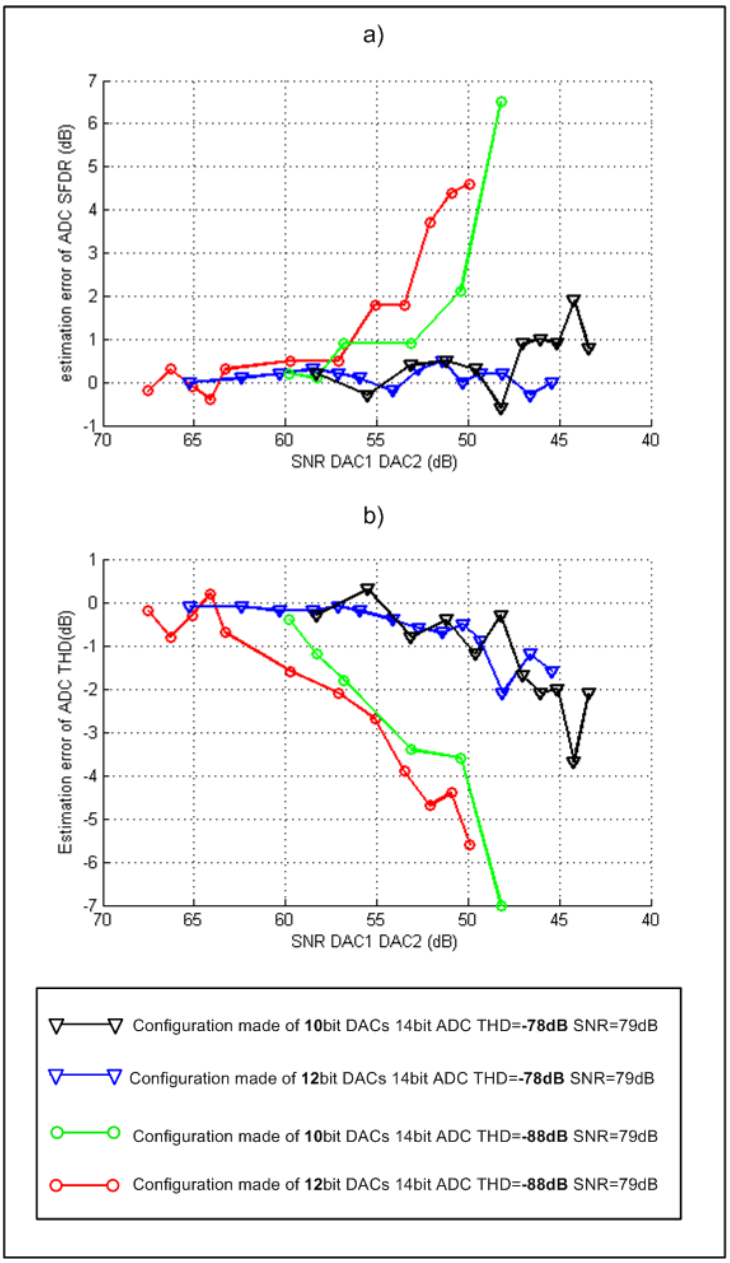

Figure 3-8: a) THD estimation error vs. SNR of DACs b) SFDR estimation error vs. SNR of DACs

As previously observed, the lower the DACs SNR, the higher the estimation error. Moreover, the higher the harmonics to be estimated, the lower limit of acceptability for the SNR.

In order to draw quantitative conclusions concerning the acceptable noise level, we have evaluated the noise present in the system for each value of the DACs SNR. The noise level is evaluated from the spectrum of the signal captured at the output of the C(2,1) configuration. It is computed with respect to experimental observations and to the properties of white noise. The power spectral density of white noise is flat. All the noise contributions are not white but experimental observations have shown that noise power is fairly spread over all the frequency bins. Therefore, noise level (nl) is

computed by dividing the noise power from SNR by the number of bins as presented by eq. 3-12.

$$nl = \frac{P_{noise}}{N/2} \qquad \text{eq. 3-12}$$

where N is number of samples used for the FFT and as a consequence, N/2 is equal to the number of bins in the spectrum computed by FFT.

$$nl_{dB} = 10\log_{10}\left(\frac{nl}{P_{signal}}\right) \qquad \text{eq. 3-13}$$

This approximation is verified for all kind of converter architecture, except for the sigma-delta one. For the sigma-delta architecture, the noise spectral density is reshaped to push the majority of the noise power at high frequencies. Because of this specificity, the sigma-delta architecture is not considered in this study. Consequently the noise floor computation is effective for all the architectures addressed by our method. The Figure 3-9 presents a spectrum measured at the output of a simulated converter with a real INL curve and the computed noise floor.

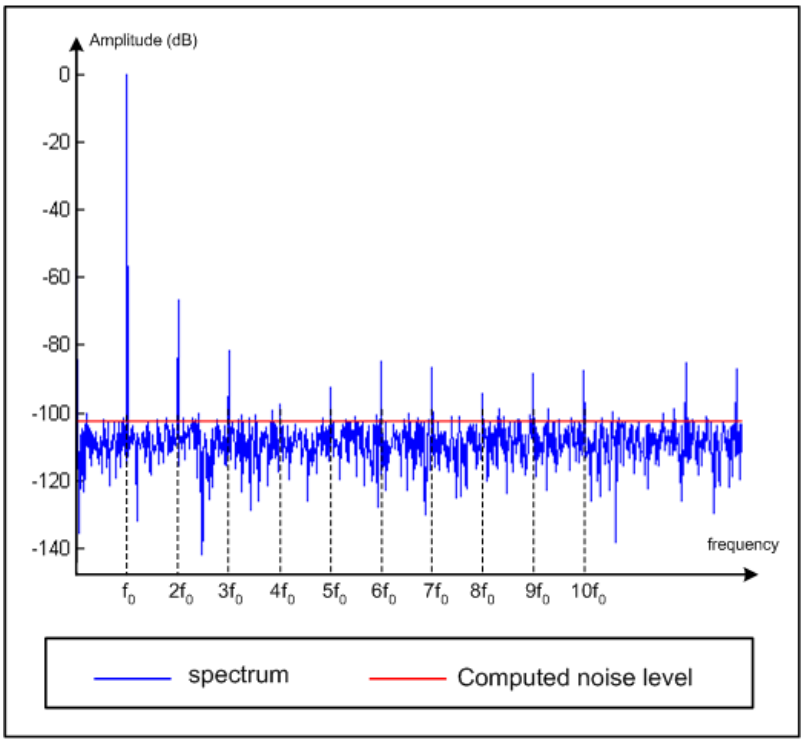

Figure 3-9: Computed noise level for a given spectrum

As previously mentioned, the higher the harmonics to be estimated, the higher the noise level can be without a significant degradation of the estimation error. To illustrate this point, a second representation of the results is presented in Figure 3-10. As for Figure 3-8, it gives the estimation error for the THD and SFDR of the ADC under test, but with respect to a new parameter that corresponds to the difference between the highest harmonic to be estimated and the noise level present in the system. This new parameter permits to normalize the results whatever the THD of the converter under test is.

Note that the highest harmonic to be estimated has been considered, because it reflects the value of the SFDR, and gives the maximum contribution to the THD. As a consequence, this harmonic that must be significantly over the noise level in order to limit the noise contribution to the value of its magnitude.

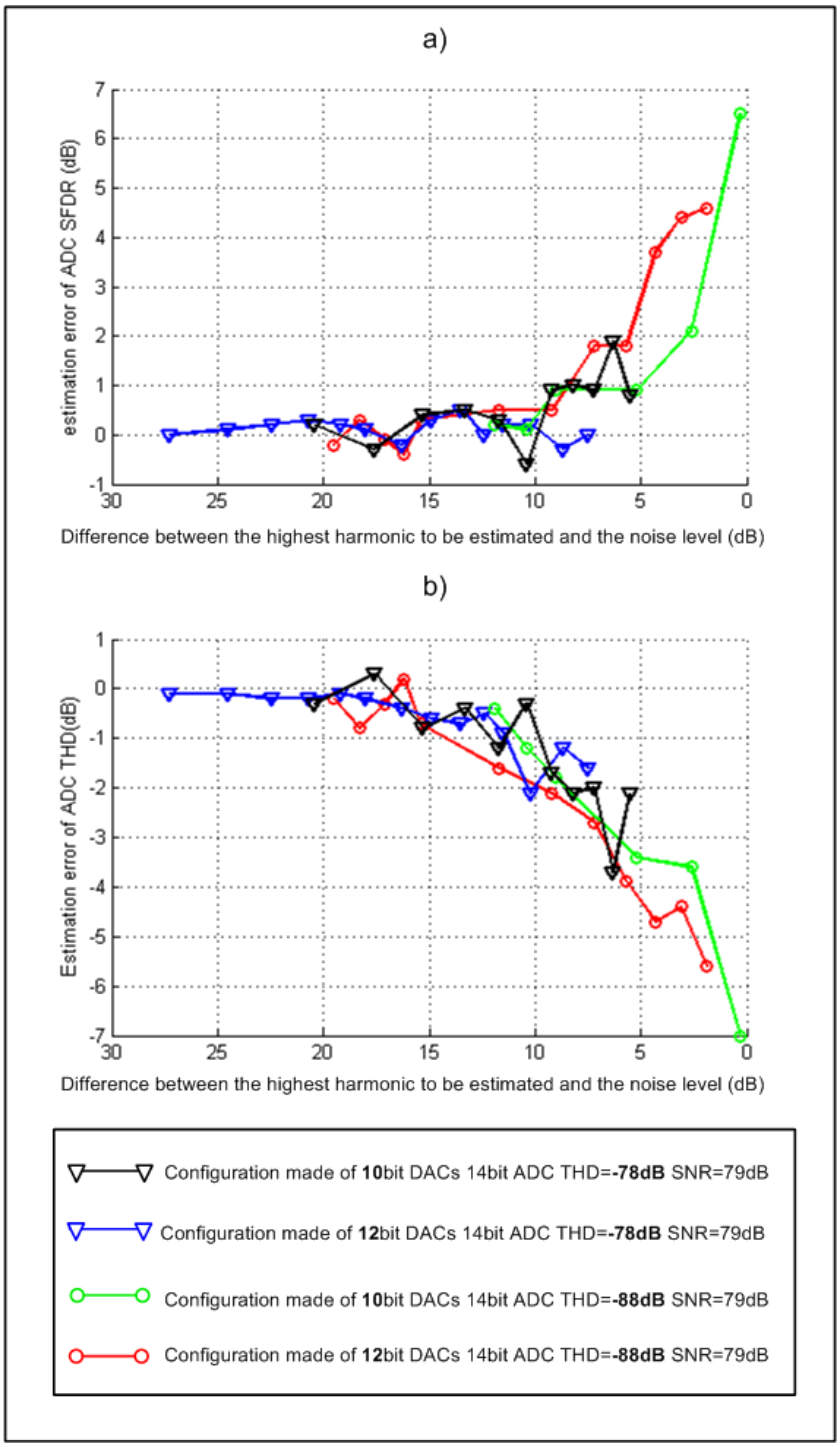

Figure 3-10: a) THD estimation error vs. difference between the highest harmonic to be estimated and the noise level
b) SFDR estimation error vs. difference between the highest harmonic to be estimated and the noise level

Results of Figure 3-10 quantify the necessary gap between the highest harmonic and the noise level in order to achieve an acceptable accuracy. We can assume that an acceptable estimation error is 1.5dB. Indeed this value is close to usual measurement variations observed in ATE during production test. We can see that whatever the resolution is, considering the SFDR and the THD estimation, the necessary condition for an effective measurement with the ANC-based technique is a difference of at least 10dB between the highest harmonic and the noise level. This necessary condition could be a limitation for our method. It is therefore the objective of the next section to further evaluate the implications of this condition.

II.4 **Application field of the proposed method**

The necessary condition for an accurate estimation of the converter parameters using our new method is a minimum gap of 10dB between the highest harmonic to estimate and the noise level. There are two different situations in which this condition may not be satisfied.

The first one is an excess of noise due to a defective component. In this case the test accuracy can be affected, but the defective converter should be rejected by another test addressing noise measurement. As a consequence, the test coverage should be preserved.

The second one is an excess of noise due to a large difference between the converter resolutions. In presence of a large difference between their resolutions, the normal noise level (mainly due to the quantization) of one converter may exceed the harmonic amplitude of another converter. In this case, it could be a real limitation of the method. It is therefore required to link the necessary condition to converter specifications in order to generalize it and to establish the application field of the proposed method.

This necessary condition addresses the noise level and harmonic amplitude of the converters. These characteristics are linked to the resolution of a converter. As a consequence, the necessary condition can be linked to the resolution of the converter.

The purpose of the next set of simulations is to establish the application field of the method relatively to the converter resolutions. A new set of simulations was carried out considering converters of different resolutions in a C(2,1) configuration. The DACs and ADC resolutions were varying from 6 to 12 bits by increment of 2 bits. Figure 3-11 shows the estimation error on the THD and SFDR of the ADC in function of the DACs resolution. Figure 3-12 gives the results for the estimation error on the THD and SFDR of DAC1 in function of the ADC resolution. The objective of this set of simulations is to estimate the range of resolutions suitable for the converters in a C(2,1) configuration. Note that all the simulated converters are good converters in terms of SNR.

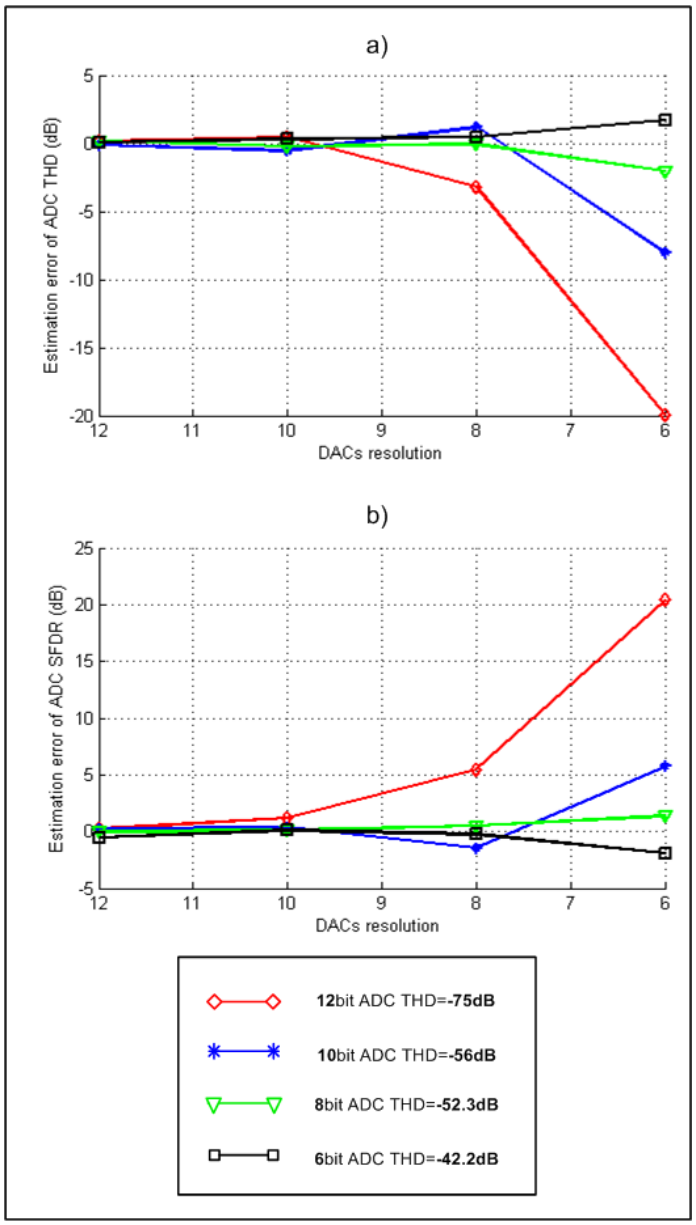

Figure 3-11: a) estimation error of ADC's THD Vs DACs resolution
b) estimation error of ADC's SFDR Vs DACs resolution

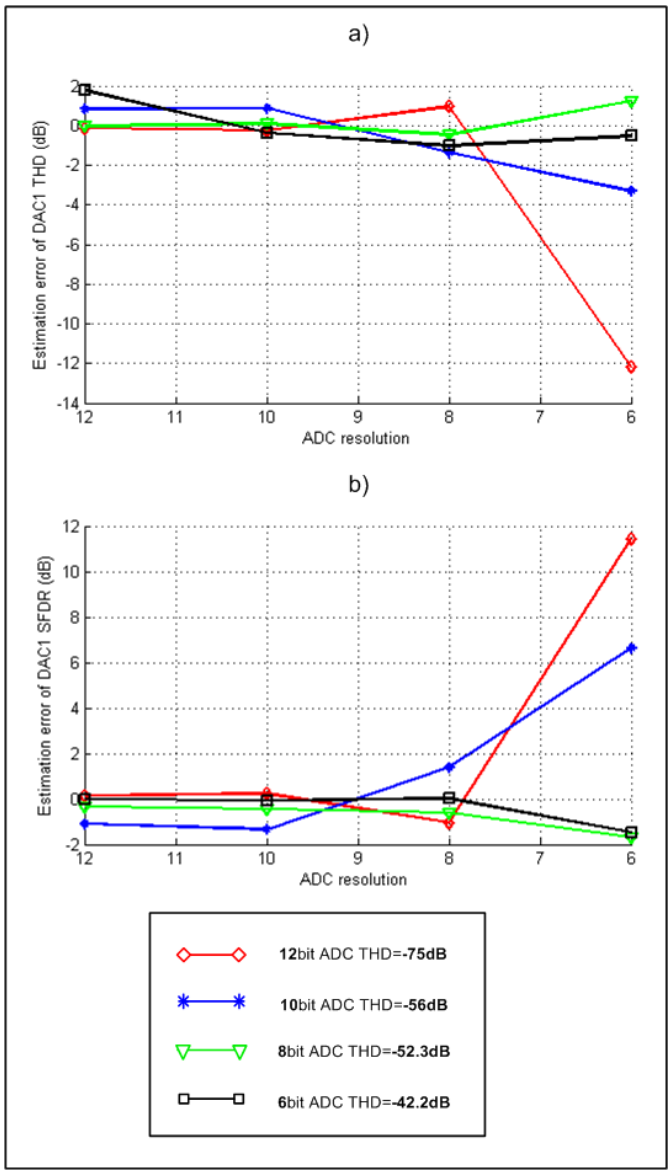

Figure 3-12: a) estimation error of DAC1's THD vs. ADC resolution
b) estimation error of DAC1's SFDR vs. DACs resolution

Let us first consider the ADC test results presented in Figure 3-11. As expected, we observe globally for THD and SFDR estimations that the estimation error increases when the DACs resolution decreases. Indeed when the DACs resolution decreases, the quantization noise increases and consequently the noise level. To go deeper in the analysis, let us consider an acceptable limit of estimation error between 1.5 and 2dB. This limit is close to the measurement repeatability usually observed on production test. According to this limit of acceptance, the harmonic estimation of 6-bit and 8-bit ADCs, is accurate enough in a 6 to 12-bit range for the DACs resolution. The 10-bit ADC test gives some accurate results using DACs from 12 to 8-bit resolution. The test of the 10-bit ADC gives an inaccurate result using 6-bit DACs. To summarize, we observe that

The distortion of an R-bit ADC can be accurately tested using DACs with a resolution of at least (R-2)-bits

This validation result brings a significant improvement in the domain of converter testing. Indeed as previously explained, the usual test approach for converter testing requires analogue instruments with a resolution at least 2 or 3 bits higher than the resolution of the converter under test.

Now let us consider the DAC1 test results presented in Figure 3-12. In previous simulations, we assumed that the estimation of DAC parameters would be affected in a similar manner than the estimation of the ADC parameters. In other words, we assumed that the critical parameter (noise level) from the test set-up influences in the same way the estimation of the DACs parameters and the estimation of the ADC parameters. Considering the DAC1 test results, the assumption is verified. Indeed the estimation of DAC1 parameters also suffers from noise influence. The higher the difference between the resolutions of converters, the higher the estimation error. This estimation error is due to the noise level. However a slight difference could be observed in comparison with ADC test results. Indeed the estimation error increases more slowly for the DAC1 test than for the ADC test. This can be explained by the fact that the DAC2 resolution is the always same as DAC1 and only the ADC resolution is decreased. As a consequence when the ADC1 resolution is 12 bits and the two DACs resolution is 6 bits, the noise level (mainly due to quantization noise) is higher than when the DAC1 (and DAC2) resolution is equal to 12 bits and the ADC resolution is equal to 6 bits. As the noise level is lower, the estimation error is also lower.

II.5 **Summary**

Thanks to these sets of simulations we can draw several conclusions. The first important conclusion is relative to the first set of simulations. This first set of simulations proves that theoretical developments were properly done and that the method is effective when we use a C(2,1) configuration to test 2 DACs and 1 ADC with the same resolution. Additional sets of simulations allowed a deep study of the accuracy of the method. To begin with, a necessary condition for the method was defined: the highest harmonic of the tested converter must be at least 10dB over the noise floor. This condition comes from the random contribution of noise to harmonics. If the harmonic amplitude is too close to the noise level, the noise contribution becomes significant enough to induce some errors. It is important to notice that despite of this necessary condition there is no risk of test coverage loss. Indeed a malfunctioning converter would cause an unexpected noise level and this defective component would be detected by a noise test. Another source of unexpected noise would be a large difference between converters resolutions. Indeed in this situation, the harmonics of the tested converter could be disturbed by the quantization noise from the other converters. According to this risk, a last set of simulations has been driven. Thanks to this set of simulations, it has been proven that a converter can be tested using a C(2,1) configuration with two other converters with resolutions 2 bits lower. This observation is a true improvement for the domain of converter testing. Indeed conventional test approaches require an analogue instrument with a resolution at least 2bits higher than the resolution of the tested converter.

III Hardware measurement results

Thanks to simulations it has been proven that the method is efficient Moreover the application field of the method has been swept. A major conclusion is that the harmonic distortion of a converter can be tested using two converters the resolution of which is lower of 2bits.

The next important step for validation is the set-up of the method in order to implement the method using stand-alone converters. This type of validation is close to the final purpose, the test of converters embedded in a system. Thanks to the use of stand-alone converters, we can prevent from any DfT issue, because the analogue interconnections can be easily managed.
The second section presents the test set-ups implemented to validate the method. And the third section gives the experimental results and their explanations.

III.1 Validation setup

The experimental validation of the ANC method requires several set-ups. At first before implementing the method we decided to estimate the influence of the splitter/combiner on harmonics amplitude. The corresponding set-ups are given by Figure 3-13 and Figure 3-14. The first set-up connects the AWG output to the spectrum analyser. The AWG is a source of analogue signal, delivering a sine wave affected by some harmonics. These characteristics are measured precisely by the spectrum analyser.

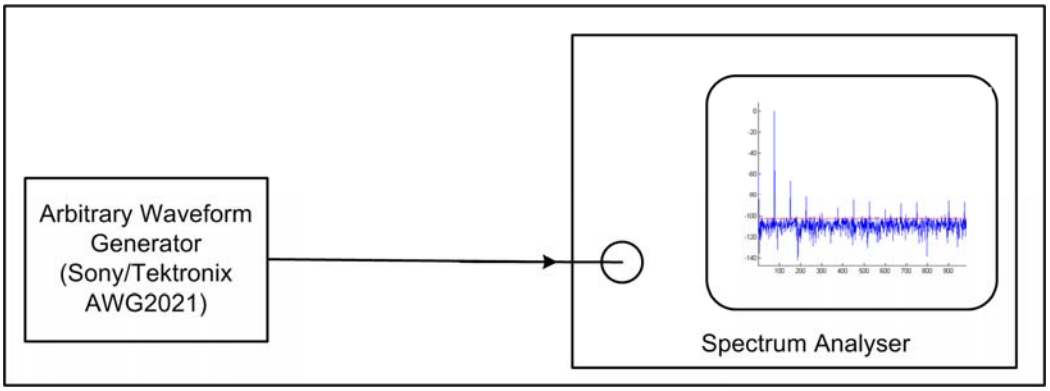

Figure 3-13: Splitter influence on harmonics, first set-up

For the second set-up the sine wave produced by the AWG goes through the splitter then the spectrum analyser. Both set-ups results allow estimating the influence of the splitter on harmonics levels.

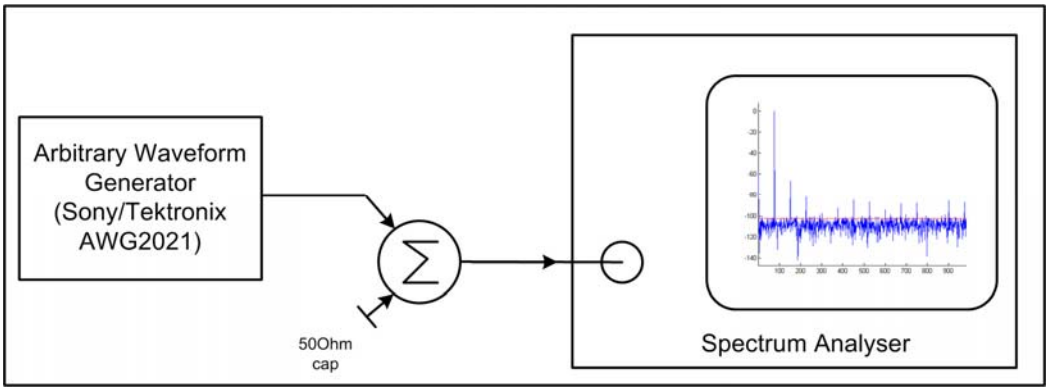

Figure 3-14: Splitter influence on harmonics, second set-up

Then the ANC-based test should be set up using stand-alone converters. The measurements of dynamic parameters given by the ANC method should be correlated with conventional test set-ups. As a consequence two additional tests should be set up:

- ✓ Conventional test set-up for the DACs

- ✓ Conventional test set-up for the ADC.

Figure 3-15 gives a block diagram description of the implementation of the ANC-based test.

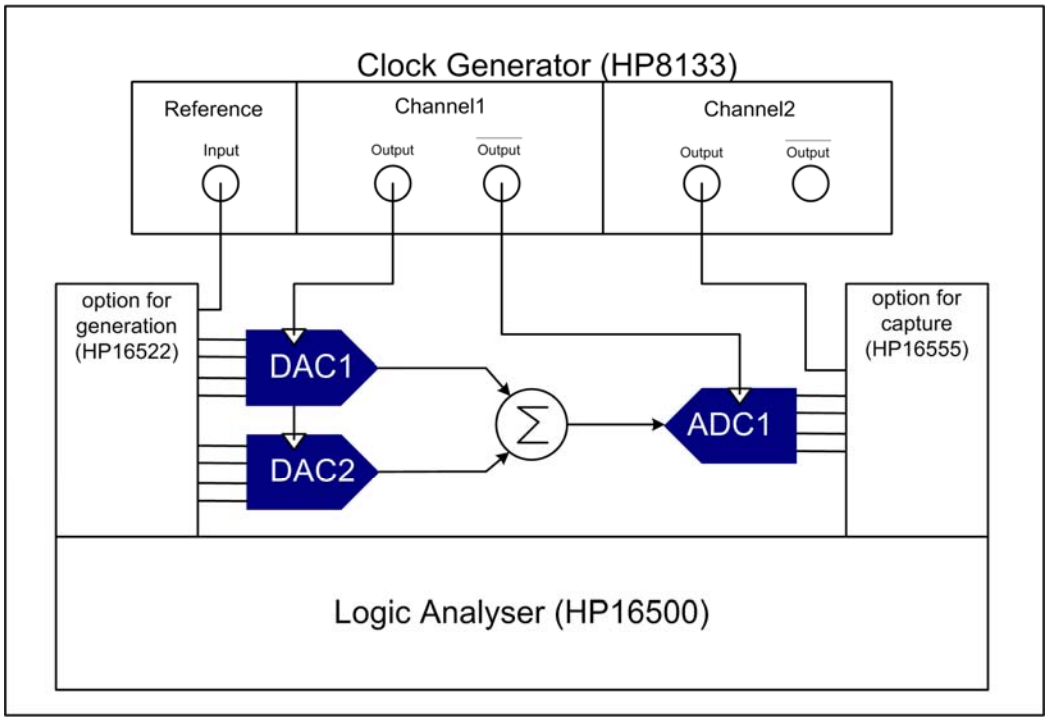

Figure 3-15: Set-up for the ANC-based test

This set-up is made of three converters under test: two 10-bit DACs and one 8-bit ADC. The sum of DACs outputs is achieved using a splitter/combiner, Mini-Circuit ZFSC-2-5. This component being fully resistive, it should have no effect on the phase or amplitude of the harmonics. This characteristic was checked and is presented in the next section. The only potential influence of the combiner is an additional thermal noise. The set-up is also made of a logic analyser HP16500. This instrument is used to generate the test pattern driven to the DACs inputs and it is also used to capture the data at the output of the ADC. These functions are respectively realised by the options HP16522 and HP16555. The second important instrument is the clock generator, HP8133. The instrument enables a good synchronisation between the pattern generations, the conversions and the captures. The clock reference is given by the pattern generator. As for a usual test set-up, the synchronisation is a crucial element of the test implementation. A HP6626A model provides the power supplies to the converters under test. And all these instruments are controlled through a GPIB bus by a computer using a HP-Vee program. The computer and the voltage supply are not presented in the Figure 3-15.

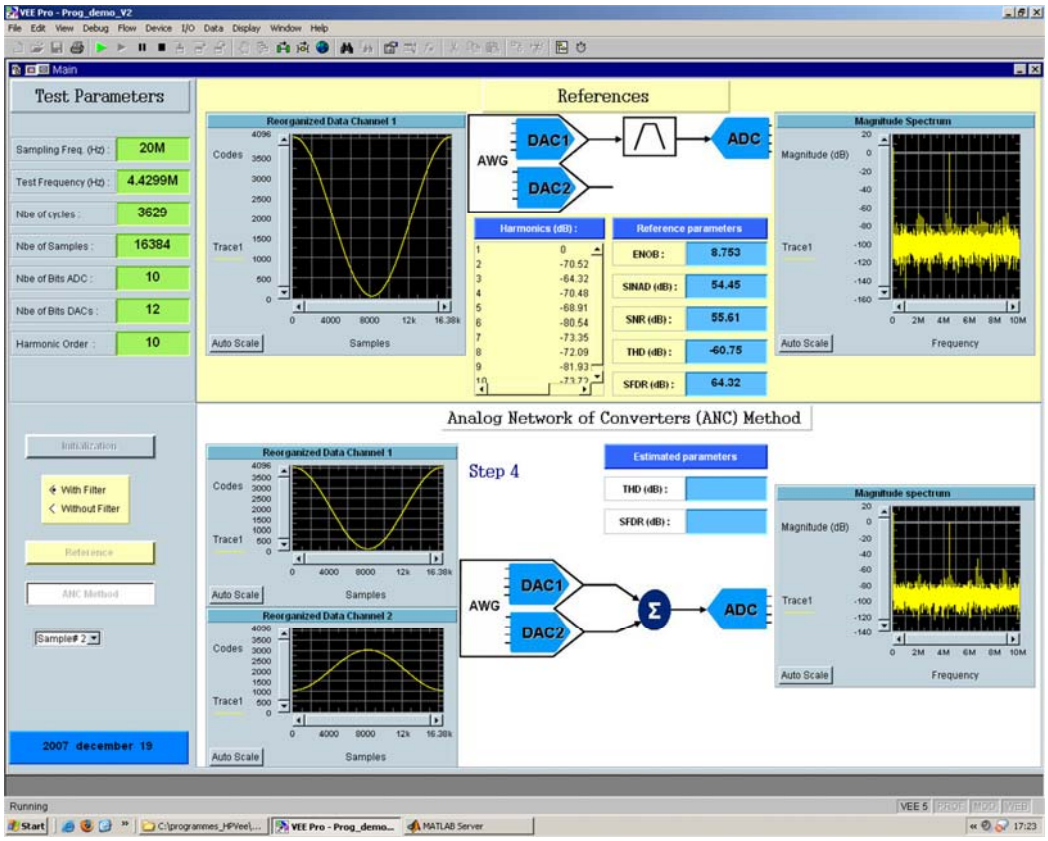

Figure 3-16: HP-Vee interface to control the instruments and the implementation of the method

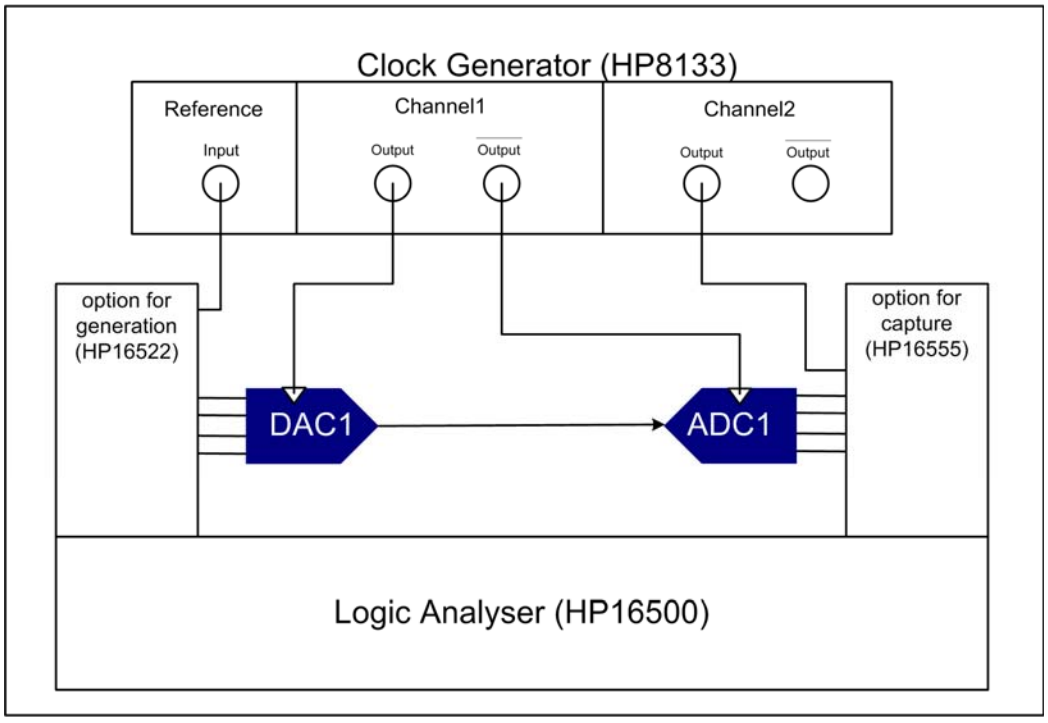

Figure 3-17: Second experimental set-up for ANC-based method validation

The set-up presented by Figure 3-15 is used for the full ANC method. A second set-up was implemented for the validation of the ANC approach. It is made of a chain of a DAC and an ADC. The use of these set-ups is more precisely described in the next section.

Figure 3-18 presents the conventional set-up for ADC testing. The test signal is generated by an arbitrary waveform generator, Sony/Tektronix AWG2021. In order to increase the linearity of the test signal and to overcome the low performance of the AWG, the test signal goes through a band-pass filter centred on the test signal frequency. The synchronisation is managed by the clock generator, HP8133. The ADC output signal is captured by the logic analyser. This set-up is used in order to have some reference measurements for the ADC parameters.

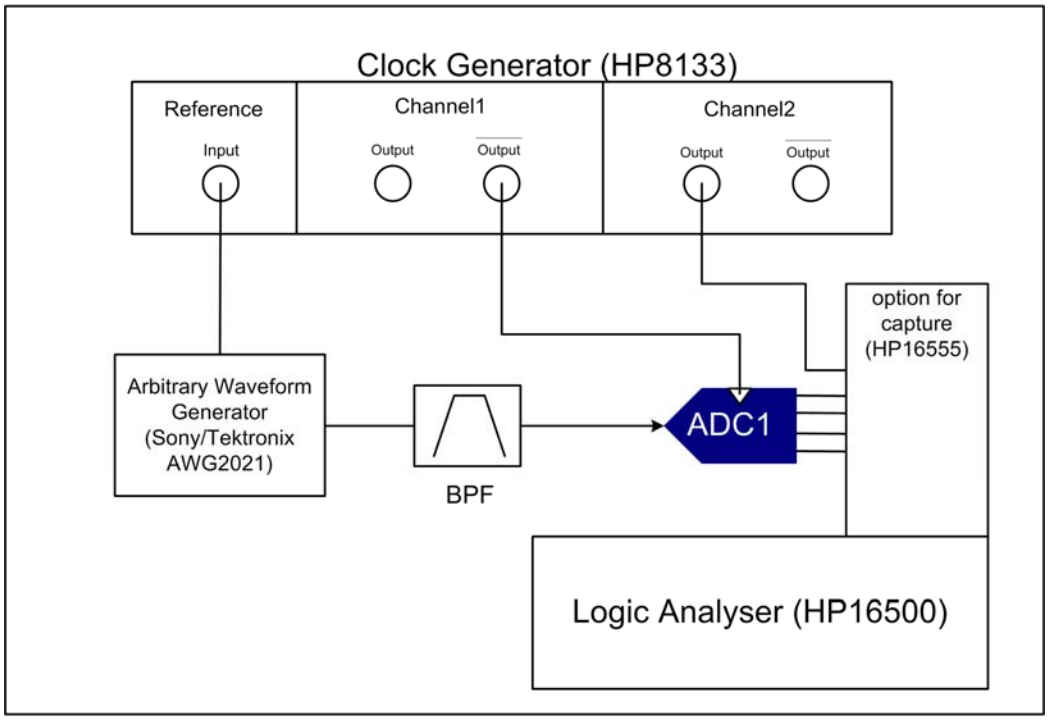

Figure 3-18: Conventional set-up for ADC test

Figure 3-19 presents the test set-up for a conventional DAC test. As previously the clock generation is made with the HP8133. The test pattern generator is the HP16522 option from the logic analyser, HP16500. The DAC harmonics are measured by a spectrum analyser, Agilent N9020A.

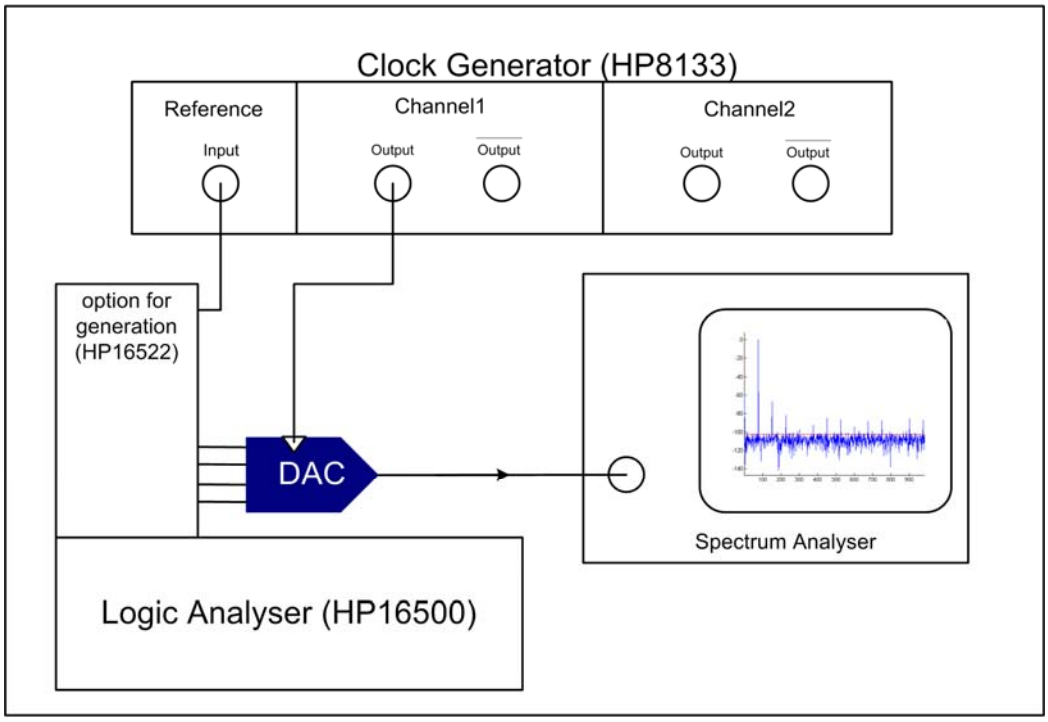

Figure 3-19: Conventional set-up for DAC test

This set-up is used in order to have some reference measurements for the DACs parameters.

III.2 **Results and discussion**

III.2.A Splitter influence characterization

The estimation of splitter influence on harmonics level requires two test set-ups. The first test consists in generating a sine wave using an AWG. This sine wave is affected by harmonics induced by the generator. These harmonics are then precisely measured using a spectral analyser. In a second test, the same sine wave is generated by the AWG, but subsequently goes through the combiner and then to the spectrum analyser. For both tests the amplitude of the fundamental and harmonic bins are measured. The comparison of both results would permit to estimate the influence of the combiner on harmonics amplitude.

The results are presented in the Table 3-4, where H1 is the fundamental bin and H2 to H6 the harmonics. Harmonics levels (dBc) are given relatively to the signal level.

	H1 (dBm)	H2 (dBc)	H3 (dBc)	H4 (dBc)	H5 (dBc)	H6 (dBc)
Configuration #1 without splitter	-2,3	-65,0	-64,1	-78,1	-74,7	-85,5
Configuration #2 with splitter	-5,5	-65,2	-64,4	-78,1	-74,7	-83,9

Table 3-4: Splitter influence characterization results

According to Table 3-4, the first splitter influence is the attenuation of the fundamental bin. This consequence is due to resistor scale architecture of the splitter and is figured in the datasheet. Concerning harmonics the maximum influence of the

splitter is an attenuation of 0.3dBc of H3. This attenuation is very small and can be neglected. As a consequence we can conclude that the combiner has no influence on harmonics levels. The phase of harmonics is the second important information. No experimental validation has been driven to prove that the splitter has no influence on harmonics phase. Actually, we made this assumption because the splitter is only composed of resistors, which intrinsically do not introduce any changes in the signal phase.

III.2.B ANC method experimental validation

III.2.B.a. Test of three converters using ANC method

The purpose of this first experiment is to validate the full ANC method. The set-up presented in Figure 3-15 is used to implement the ANC method. It is made of two DACs and one ADC. The full method, comprising 5 tests, is applied ten times to the three converters, in order to estimate the measurement variations. The results of the method are compared to the results of the conventional tests represented in Figure 3-18 and Figure 3-19. This protocol was executed two times, in order to prove that the method can be effective on two lots of three converters. The THD and SFDR measurements are respectively presented by Table 3-5 and Table 3-6. The tables show the reference measurement, the maximum, the minimum and the average estimation errors for the 10 iterations of the ANC method. It is important to notice that for each test the size of the sample set is the same as for a conventional test $4*2^R$ samples, where R is the resolution of the DAC

	Reference measurement (dB)	Minimum estimation error (dB)	Average estimation error (dB)	Maximum estimation error (dB)
DAC1	-55.6	0.1	0.3	0.7
DAC2	-55.6	0.1	0.6	0.9
ADC1	-43.5	0.1	0.2	0.2
DAC3	-55.5	0.1	0.8	1.2
DAC4	-55.8	0.1	0.3	1.1
ADC2	-52.5	0.1	0.7	1.1

Table 3-5: THD measurements for the first ANC method validation

	Reference measurement (dB)	Minimum estimation error (dB)	Average estimation error (dB)	Maximum estimation error (dB)
DAC1	56	0.4	0.9	1.2
DAC2	56.1	0.1	0.3	0.9
ADC1	46.7	0.7	0.8	1
DAC3	55.9	0.2	0.9	1.3
DAC4	56.2	0.1	0.2	1.1
ADC2	55.4	0.1	0.6	1

Table 3-6:SFDR measurements for the first ANC method validation

The first obvious observation addresses the maximum estimation error. Indeed whatever the type converter is (DAC or ADC), the maximum estimation error is 1.2dB for THD and 1.3dB for SFDR. In addition we can see that the maximum average error for the six converters is below 1dB. The method is effective for two sets

of converters. Moreover it is effective with a good and a bad ADC in terms of THD and SFDR: in this example, their THD values differ by 9dB.

III.2.B.b. Learning and test production steps validation

According to the first experimental validation, the full ANC method has shown some good results. The purpose of this second experiment is to go further in the validation of the ANC approach. The learning and test production steps will be validated. The test set-ups are the same has the ones used for the previous validation. But the alternate test approach is now partitioned in two steps. For the first step, the learning phase, two DACs and one ADC is set-up (Figure 3-15) in order to estimate the harmonics induced by the ADC. The THD and SFDR results of the learning phase are given in the following tables.

	Reference measurement (dB)	Minimum estimation error (dB)	Average estimation error (dB)	Maximum estimation error (dB)
DAC1	-54.1	0.1	0.2	0.8
DAC2	-55.8	0.2	0.4	1.0
ADC1	-43.6	0.1	0.1	0.3

Table 3-7: THD learning phase

	Reference measurement (dB)	Minimum estimation error (dB)	Average estimation error (dB)	Maximum estimation error (dB)
DAC1	54.4	0	0.5	1.3
DAC2	56.9	0.3	0.4	0.9
ADC1	46.7	0.1	0.5	0.9

Table 3-8: SFDR learning phase

The results are similar to the ones given by the first experiments. Indeed we observe a maximum error of 1.3dB for the SFDR and 1dB for the THD. The ADC harmonics values used for the dynamic parameters computations are kept for the second step: the production test step.

For the second step, the test set-up implemented is presented by Figure 3-17. It requires a DAC and an ADC. As described in (cf. Chapter 2V.3) this is called test production step because it requires a simple test set-up and a test time equal to the time of a conventional test. Indeed one single test using one single test signal and one single capture are required to test one additional DAC as for a conventional test. For this step we kept the ADC previously characterized during the learning step. This 8-bit ADC was used to test six additional 10-bit DACs. The results are given in Table 3-9 and Table 3-10. Each DAC was tested ten times, and the tables present the minimum, maximum and average estimation errors.

	Reference measurement (dB)	Minimum estimation error (dB)	Average estimation error (dB)	Maximum estimation error (dB)
DAC3	-56,0	0,0	0,0	0,3
DAC4	-55,7	0,0	0,3	0,7
DAC5	-55,9	0,6	0,8	1,0
DAC6	-55,1	0,0	0,2	0,5
DAC7	-55,9	0,2	0,8	1,5
DAC8	-55,7	0,6	1,1	1,9

Table 3-9:THD production test

	Reference measurement (dB)	Minimum estimation error (dB)	Average estimation error (dB)	Maximum estimation error (dB)
DAC3	56,4	0,9	1,3	1,6
DAC4	56,7	0,0	0,1	0,6
DAC5	56,4	0,1	0,3	0,5
DAC6	56,4	0,0	0,4	0,6
DAC7	56,4	0,0	0,2	0,4
DAC8	56,9	0,6	0,5	1,0

Table 3-10:SFDR production test

The results presented are very positive. Indeed for the six tested DACs, we observed a maximum estimation error of 1.9dB for THD and 1.6dB for SFDR. In addition the maximum average of estimation error is 1.3dB. These variations are close to the variations observed on tester measurements. These experiments validate the conclusion extracted from simulation validations. Indeed using an 8-bit ADC, we are able to test 10-bit DACs. In addition the test time is the same as for a conventional test and requires only digital instruments to generate and capture the test signals.

IV Conclusion

The theory of a method using digital signals has been developed to test a set of DACs and ADCs embedded in a same system. This method has been validated through simulations and hardware experiments.

With the simulation, we have been able to validate the method and to estimate its application field. The method accuracy is sensitive to the noise level of the C (2,1) configuration (ref. Figure 3-3), but we have demonstrated that a converter can be tested using such a configuration even when the resolution of the converters used as instruments have 2 bit less of resolution. This observation represents a real breakthrough in the field of converter testing. Indeed conventional test approaches require analogue instruments with resolution at least 2bits higher than the resolution of the converter under test.

The method was experimentally validated on stand-alone converters. The implemented C (2,1) configuration was made of two 10-bit DACs and one 8-bit ADC. These three converters were successfully tested using the ANC method. Their SFDR and THD parameters were measured several times with a maximum estimation error of 1.3dB, which is close to classical industrial measurement uncertainties. In addition to the full ANC method, the generalization of the method was also validated on a lot of seven DACs using only one capture per DAC. These first experimental results have

validated the theory of the ANC method and also demonstrated that it can be extended to configurations embedding multiple converters. We also have confirmed by hardware experiments that a converter can be tested even when the resolution of the instruments is 2-bit lower.

Chapter 4

Extension of the application field of the ANC method

I Introduction

The basic principle of the ANC-based test method is to interconnect DACs and ADCs in the analogue domain in order to only drive in and out digital test signals. The test method purpose is to discriminate the harmonic contribution of the converters contained in the test path. This methodology targeted the test of converters embedded in a complex system, but clearly this original method can be extended to other applications.

A first possible application is described in the second section. It consists in using ANC approach to be able to use only low resolution Arbitrary Waveform Generator (AWG) for the production test of ADCs. This second section gives a state-of-the-art of test methods that use low performance AWG for ADC testing. Then, a new technique based on the ANC method is described. And finally, the test setup and the results of experimental validations are given. The third section presents the second extended application. This is a method that relaxes the constraints on digitizer performances for the test of DACs. The last section presents the last extended application. This is the use of the ANC method as part of an ATE calibration.

II ADC testing with low resolution Arbitrary Waveform Generators

II.1 Introduction

The conventional way to test ADCs in production is the DSP-based method [maho87]. This test approach required an Analogue Waveform Generator (AWG) and a capture memory combined with a processing unit in the tester. The quality of such a test depends on the test instrument performances. One of the most critical instruments is the AWG. As a rule of thumb, considering harmonic testing, the harmonics of the signal delivered by the generator must be at least 15dB better than the specification limits of the ADC under test, to ensure acceptable test conditions. Translated in terms of number of bits, the generator resolution should be at least 2-bits higher than the tested ADC resolution. The second section figures precisely the influence of AWG on tests accuracy, and estimates the required performances for AWG relatively to the ADC under test performances. This requirement concerning AWG performances is an increasing critical issue for ADC test. Indeed AWG performances development should follow the same growth than ADCs performances. In addition AWG performances development should ahead ADCs developments in order to guaranty AWG performances to be higher than ADC ones. This is a relevant challenge. Even if it were achieved, the resulting instrument exhibiting such high performances would be very expensive and so would be the test process.

In this context, it clearly appears that there is a great interest in developing new test solutions allowing the relaxation of the constraints on the test instrument performances.

Digital-to-Analogue Converters (DACs) are the main components of AWGs. In [saee04] [buge00] [cong03] [groe89], solutions for the compensation of DACs non-linearity are proposed. These solutions are based on hardware modifications. Unfortunately, in our context, the DACs are already embedded in test instruments. In [tail04], a digital processing technique is proposed to compensate DAC nonlinearity without any hardware modification. This technique could be suitable for the

compensation of AWGs, but the technique needs high performance instruments to implement the calibration routine. Obviously, if high performance instruments are required for calibration, the interest in using a low performance AWG is reduced.

The third section presents two publications that address another approach [jin07] [cauv00]. This approach consists in relaxing constraints on AWG performances by discriminating the sources of errors in the test path or by virtually improving the performances of the test instrument. The first technique; the SEIR [jin07], is a histogram-based technique dedicated to the test of ADC linearity using low-linearity stimuli. The second one is the 2-ADC method [cauv00] that permits to estimate noise parameters from ADCs under test. Both methods overcome the performance issue of the stimuli by discriminating the errors of the DUT from the errors of the set-up. However these methods are dedicated to the measurement of linearity or noise of an ADC under test. None of them address the measurement of harmonics in order to compute some dynamic parameters.

As a consequence the fourth section presents an alternative solution to estimate harmonics distortions of an ADC using a low resolution AWG. This method relies on an initial learning phase, in which the AWG characteristics are estimated. These AWG characteristics are subsequently used to discriminate the harmonic distortions induced by the ADC under test from the ones induced by the AWG. In addition to theoretical description of the alternate method, the fourth section gives also some experimental validation results.

II.2 **Influence of AWG on the Test quality**

For ADC testing, an analogue instrument is required to generate the test signal. This analogue instrument is an arbitrary waveform generator. High-efficient test of converters is usually a challenging issue because of stringent constraints on the linearity of analogue instruments. For instance, according to [jin05_2], for testing static parameters of ADCs with 16bit or higher resolution by using the conventional histogram method, more than 20bit linear signals are needed. The constraint is also relative to the estimation of dynamic parameters. In order to achieve a correct evaluation of the ADC dynamic parameters, there are some constraints concerning the generator or AWG. Indeed, an ideal test signal is a pure sine wave, but a realistic signal applied to the converter input is obviously deteriorated by the noise and the harmonics induced by the AWG. Clearly, the noise and the harmonic levels of the test signal should be low enough to be negligible compared to the noise and harmonics induced by the converter under test. AWG influence on test accuracy is also figured in this section.

II.2.A Noise level

As previously explained, the main critical part of AWG is the embedded DAC that defines AWG performances. The noise level induced by a converter is mainly because of the quantization noise linked to the ADC resolution. Eq. 4-1 gives the ideal SNR of a converter according to the resolution, where R is the converter resolution:

$$SNR_{ideal} = 20R\log(2) + 10\log\left(\frac{3}{2}\right) \qquad \textbf{eq. 4-1}$$

The following table gives the ideal SNR of a converter versus its resolution.

Converter Resolution	*Ideal SNR (dB)*
12	74
11	68
10	62
9	56
8	50

Table 4-1: Ideal SNR vs. converter resolution

Let us consider the ideal case, i.e. a sine wave without any distortion generated by an AWG and converted by an ideal ADC. The digital signal at the output of the ADC is deteriorated by two noise sources: the quantization noise induced by the AWG and the quantization noise induced by the ADC. Therefore, the SNR measured on the output of the ADC corresponds to the quadratic sum of the noise from the AWG and the noise from the ADC. The following table gives the ideal SNR of the 8bit ADC and the SNR measured on the output of the ADC versus the DAC resolution of the AWG.

Test configuration	*True SNR of ideal ADC (dB)*	*Measured SNR (dB)*
8-bit ADC tested using 8-bit DAC	50.0	47.0
8-bit ADC tested using 9-bit DAC	50.0	49
8-bit ADC tested using 10-bit DAC	50.0	49.9
8-bit ADC tested using 11-bit DAC	50.0	49.9
8-bit ADC tested using 12-bit DAC	50.0	50.0

Table 4-2: SNR measurement, ideal ADC vs. ideal DAC/ADC set-up

This table clearly illustrates that the correct estimation of the ADC SNR is only achieved if the noise induced by the AWG is negligible compared to the noise induced by the ADC. It is obvious that if the AWG has the same resolution than the tested ADC, the measured SNR is not representative of the actual ADC SNR. A resolution at least 2 bit higher is required to have a correct estimation of the ADC noise contribution. Considering a real case, the test signal is not only deteriorated by the quantization noise of the generator but also by additional noise sources. As a consequence, it clearly appears that the resolution constraints would be higher than 2 bits.

II.2.B Harmonic distortions

The other important elements used to compute the test parameter are the harmonics. To illustrate the influence of the AWG on harmonics measurements, we only consider the second order harmonic, H2, but similar behaviour could be obtained with other harmonic orders. Table 4-3 gives an idea of H2 amplitude that could be induced by converters according to practical experiments and datasheets. The second harmonic values given in table 4-3 correspond to good converters.

Converter Resolution	*Common H2 (dB)*
12	-88
10	-73
8	-55

Table 4-3: Common H2 amplitude vs. converter resolution

As previously explained, AWG consists of a DAC with harmonic distortions. Consequently if we consider a sine wave generated by an AWG and converted by an ADC, the digital signal at the output of the ADC is deteriorated by both components. In the worst case, the H2 amplitude induced by both sources can be summed. Table 4 gives the true H2 amplitude of the tested 8bit ADC, and the measured H2 amplitude considering the influence of the AWG.

Test configuration	*True H2 (dB)*	*Measured H2 (dB)*
8-bit ADC tested using 8-bit DAC	-55.0	-49.0
8-bit ADC tested using 10-bit DAC	-55.0	-54.0
8-bit ADC tested using 12-bit DAC	-55.0	-54.8

Table 4-4: H2 measurement, ADC vs. DAC/ADC set-up

We observe in Table 4-3 that an acceptable measurement is obtained with a 10-bit DAC, i.e. when the harmonic of the generators is 15dB lower than the harmonic of the ADC. We can deduce the following condition. Indeed the harmonic induced by the generator should be at least 15dB lower than the tested harmonic of the DAC. In term of resolution, the correct estimation of the ADC harmonics requires the use of an AWG with a resolution at least 2 bits higher than the resolution of the ADC under test.

II.2.C Conclusion

We can conclude that for any kind of converter and for any kind of test, there is a significant constraint relative to analogue instruments. Indeed the analogue instrument should have an effective resolution 2 bits higher than the resolution of the converter under test. It is important to notice that considering the harmonics, the 2 bits higher constraint is a necessary condition but not sufficient. In addition the harmonics induced by the generator should be 15dB lower than the tested harmonics. This additional condition is generally, but not always, verified when the 2 bits higher constraint is verified.

Considering these crucial constraints, the use of low-resolution AWG to test ADCs seems to be difficult to set up. A potential solution to overcome these constraints is to develop some methods that allow to discriminate the sources of errors or to virtually improve the performances of the test instruments. The next section gives the state-of-the-art of such test methods.

II.3 State-of-the-art of ADC test methods using low performance analogue signal generators

II.3.A SEIR method

Jin et al from the electrical and computer engineering department of the Iowa State University, propose a method to test ADC linearity using low-linearity signals [part02] [jin03] [jin05] [jin05_2] [jin07]. The method is called “Stimulus Error Identification and Removal” or SEIR method. Figure 4-1 presents the basic principle of this method.

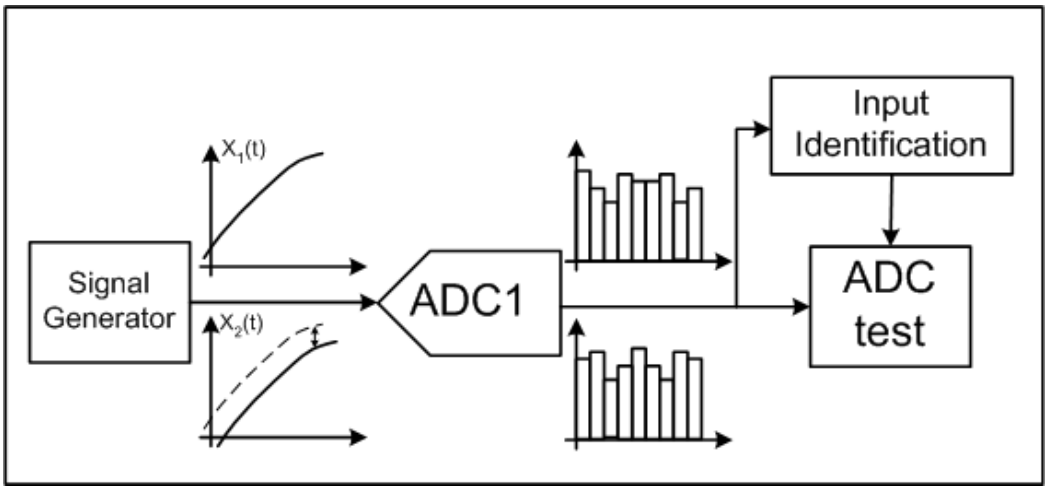

Figure 4-1: Basic principle of the SEIR approach [jin05_2]

The method is based on the conventional histogram-based test method. The accuracy of this method is affected by non-linear components from the test signal. The conventional solution to this issue is the use of a high linearity signal generator. Jin et al propose another approach. They propose to take into account the non-linear component from the test signal in order to discriminate it. The following equation presents the model of the normalized test signal.

$$x(t) = t + F(t) \qquad \textbf{eq. 4-2}$$

where F(t) is the non-linear component. This non-linear component is expanded over a set of M basis function $F_j(t)$'s with unknown coefficient a_j's as

$$F(t) = \sum_{j=1}^{M} a_j F_j(t) \qquad \textbf{eq. 4-3}$$

The SEIR algorithm uses two ramp signals with a constant α to test an ADC

$$x_1(t) = t + F(t) \qquad \textbf{eq. 4-4}$$

$$x_2(t) = x_1(t) - \alpha \qquad \textbf{eq. 4-5}$$

By feeding the two ramps into an ADC under test, two sets of histogram data can be collected. Using a least square method the M a_j unknowns are estimated. Once the nonlinearity a_j's are known their effects on histogram data can be removed for an accurate identification of true INL from the ADC.

This is the basic principle of the SEIR method. It has been extended to non-constant α case. And experimental validation has demonstrated the effectiveness of this method to test a 16-bit ADC using a 7-bit DAC.

II.3.B 2-ADC method

Another method has been developed to discriminate the source of errors in a test path. This is the 2-ADC method [cauv00]. This method is suited for the measurement of ADC noise parameters. The principle of this method has already been presented in Chapter 2IV.1.

II.3.C Summary

According to previously published approaches, two methods give some results that allow using low-resolution test instruments. These methods are the SEIR and the 2-ADC method. These two techniques deal directly with low performance stimuli for converter testing. The first technique aims at testing the ADC linearity using low-linearity stimuli. The second method dealing directly with low-performance stimuli is the 2-ADC method. This method has been developed to estimate noise parameters from ADCs under test. Both methods overcome the performance issue of the stimuli by discriminating the errors of the DUT from the errors of the set-up.
None of these techniques is dedicated to harmonics measurements. So considering these domains of applications, a test set-up based on the ANC can be an alternative to test the harmonics of an ADC using a low-resolution AWG. This alternate solution is presented in the next section.

II.4 **A new solution to test ADC dynamic parameters using low-resolution AWG**

A conventional solution to reduce the AWG non-linearities is to use a filter centred on the test frequency. However this solution is quite expensive as a new filter is required for each test frequency, involving a complex test board with costly calibration phase. Instead, an ANC-based method for stand-alone ADC testing using a low performance AWG can be an effective alternate solution. This concept is developed in this section.

Following sub-sections gives an explanation of the implementation of the ANC method for industrial testing of ADCs. An experimental validation of this extended application has also been driven in order to prove its viability and effectiveness. The experimental protocol and the results are also presented in the following section.

II.4.A ANC-based alternative method for production test of ADC

This section presents a test method that allows mass production testing of ADC harmonic distortions using low-cost testers. By low cost testers, we mean testers that contain standard-performance AWGs that would be not efficient enough to apply a conventional DSP-based test. At first the theoretical fundamentals of the ANC-based approach for ADC testing are presented. The two steps of the method are then precisely described. The first step, called learning process consists in estimating the AWG harmonic contribution. The second step, called production test step, consists in testing ADCs using a post-processing calibration of the AWG.

II.4.A.a. Theoretical fundamentals

Let us consider a sine wave applied to an ADC. Using a Fourier series expansion, the output signal can be expressed by eq. 4-6. In this equation we distinguish the sampled sine wave x(n) that would be obtained from the ideal ADC and the sum of all the harmonic values introduced by static and dynamic non-linearity of the converter [jani07][kerz06_2].

$$s(n) = x(n) + \sum_{k \geq 0} Hconv_k^{Amp} \cos\left(k\left(\theta_n + \theta_0\right) + \theta_{conv,k}^{Amp}\right) \qquad \textbf{eq. 4-6}$$

n is the sample index, θ_0 the initial phase shift, $\theta_{conv,k}^{Amp}$ the phase shift induced by dynamic non-linearity, $Hconv_k^{Amp}$ the amplitude of the k^{th} harmonic, and θ_n is the instantaneous sampling phase given by:

$$\theta_n = 2\pi\left(\frac{P}{M}\right)n \qquad \textbf{eq. 4-7}$$

where P is the number of cycles and M the number of samples in the test record.

Eq. 4-6 may also apply to a DAC and can thus be used to express the signal generated by an AWG.

II.4.A.b. Learning AWG harmonic contribution for post-processing calibration

According to theoretical developments described in the Chapter 2V and considering a system of two DACs and one ADC connected by a set of switches and a combiner as illustrated in Figure 4-2, it is possible to discriminate the harmonic contribution of each individual converter.

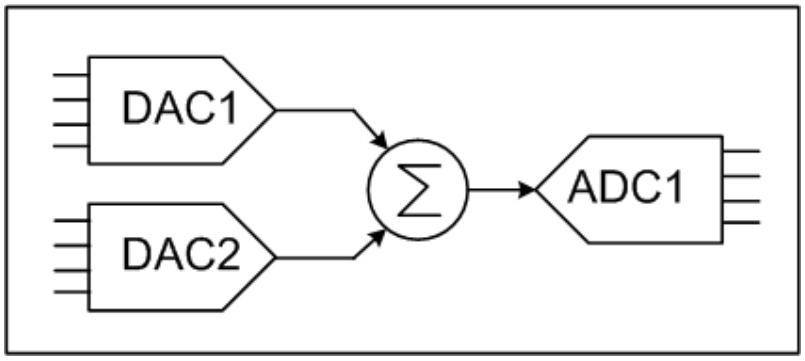

Figure 4-2: C(2,1) configuration

Let us consider a test configuration in which the output of DAC1 is directly connected to the ADC1 input. According to eq.4-6 the signal captures at the output of the ADC can be described by the following equation:

$$s(n) = x(n) + \sum_{k\geq 0}\begin{Bmatrix}\left[Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right)\right]\cos(\theta_n) \\ -\left[Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right)\right]\sin(\theta_n)\end{Bmatrix} \qquad \textbf{eq. 4-8}$$

The spectrum of the output signal can be computed and we can extract the values of the harmonics H_k. Obviously, the output signal is impacted by errors of both converters. In other words, the measured spectrum includes the harmonic contribution of DAC1 as well as the harmonic contribution of ADC1, and the measured harmonics can be described by the following equation

$$\begin{aligned} Re\left(H_k\right) &= Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\ Im\left(H_k\right) &= -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right)\end{aligned} \qquad \textbf{eq. 4-9}$$

In this equation, we assume that amplitudes of harmonics created by the DAC are negligible with respect to the fundamental amplitude of the signal. In this way, we can consider that the ADC is driven by a single tone signal and the harmonics induced by the ADC are similar to the ones induced by a good test signal.

Eq.4-9 establishes a relation between the harmonic contributions of the two converters involved in the test configuration. In this equation, the left member is known and corresponds to the real and imaginary parts of the k^{th} spectral bin measured at the output of the ADC, while the right member represents the unknowns.

This small example demonstrates the relationship between one configuration and its resulting equation, which leads to the fundamental idea of the new test method. As described in Chapter 2V, by using different configurations - DAC1/ADC1 or DAC2/ADC1 or DAC1+DAC2/ADC1 - we are able to obtain a set of different equations. So, with an adequate set of configurations (i.e. system of ten independent equations eq.2-75), we are able to discriminate the harmonic contribution of each converter.

$$
\begin{cases}
Re\left(H_k^{m,a}\right) = Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\
Im\left(H_k^{m,a}\right) = -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \\
Re\left(H_k^{m,b}\right) = Hdac2_k^{FS}\cos\left(\theta_{dac2,k}^{FS}\right) + Hadc1_k^{FS}\cos\left(\theta_{adc1,k}^{FS}\right) \\
Im\left(H_k^{m,b}\right) = -Hdac2_k^{FS}\sin\left(\theta_{dac2,k}^{FS}\right) - Hadc1_k^{FS}\sin\left(\theta_{adc1,k}^{FS}\right) \\
Re\left(H_k^{m,c}\right) = Hdac2_k^{FS/2}\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right) \\
Im\left(H_k^{m,c}\right) = -Hdac2_k^{FS/2}\sin\left(\theta_{dac2,k}^{FS/2}\right) - Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right) \\
Re\left(H_k^{m,d}\right) = Hdac1_k^{FS}\cos\left(\theta_{dac1,k}^{FS}\right) + Hdac2_k^{FS/2}\cos(k\pi)\cos\left(\theta_{dac2,k}^{FS/2}\right) + Hadc1_k^{FS/2}\cos\left(\theta_{adc1,k}^{FS/2}\right) \\
Im\left(H_k^{m,d}\right) = -Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) - Hdac2_k^{FS/2}\cos(k\pi)\sin\left(\theta_{dac2,k}^{FS/2}\right) - Hadc1_k^{FS/2}\sin\left(\theta_{adc1,k}^{FS/2}\right) \\
Re\left(H_k^{m,e}\right) = \begin{bmatrix} Hdac1_k^{FS}\cos(\theta_{dac1,k}^{FS}) + \\ Hdac2_k^{FS/2}\left[\cos(k\phi_1)\cos\left(\theta_{dac2,k}^{FS/2}\right) - \sin(k\phi_1)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right] + \\ Hadc1_k^{FS}\left[\cos(k\phi_2)\cos\left(\theta_{adc1,k}^{FS}\right) - \sin(k\phi_2)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{bmatrix} \\
Im\left(H_k^{m,e}\right) = -\begin{bmatrix} Hdac1_k^{FS}\sin\left(\theta_{dac1,k}^{FS}\right) + \\ Hdac2_k^{FS/2}\left[\sin(k\phi_1)\cos\left(\theta_{dac2,k}^{FS/2}\right) + \cos(k\phi_1)\sin\left(\theta_{dac2,k}^{FS/2}\right)\right] + \\ Hadc1_k^{FS}\left[\sin(k\phi_2)\cos\left(\theta_{adc1,k}^{FS}\right) + \cos(k\phi_2)\sin\left(\theta_{adc1,k}^{FS}\right)\right] \end{bmatrix}
\end{cases}
\qquad \textbf{eq. 4-10}
$$

with $\varphi_1 = \pi - ar\cos\left(\frac{1}{4}\right)$, $\varphi_2 = \pi - 2ar\cos\left(\frac{1}{4}\right)$.

To develop this method, the combiner influence is neglected. This assumption has been established considering that we use a fully resistive combiner. Note that this assumption has been practically validated (cf. Chapter 3III.2.A) A system of a two-channel AWG has two DACs. If we connect this system to an ADC by set of switches and a combiner we obtain the set-up required for our method as presented in Figure 4-3.

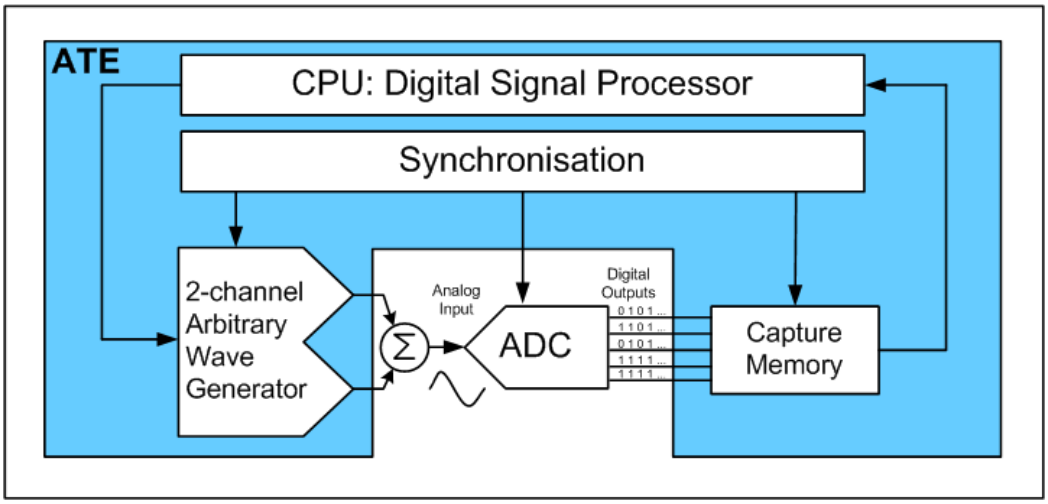

Figure 4-3: Required set-up to estimate the harmonic contributions of the AWG

Therefore, it is possible to apply this method to estimate the harmonic contribution of the AWG in the objective to perform a post processing calibration of this AWG to test ADCs.

II.4.A.c. Mass production test using post-processing calibration

The method described in the previous section aims at estimating the harmonic contributions of the AWG and the tested ADC. Five test configurations are required to perform this estimation.

After one application of the whole method, if we change the ADC and repeat the complete procedure, we will obtain a new test result for the ADC under test but still the same AWG contribution. In fact, once the AWG has been characterized, there are only two unknown variables in the 2-equation system, eq. 4-9. Solving this 2-equation system, it is therefore possible to determine the harmonic contribution of every new ADC using only one test.

In summary, considering mass production test, we need to apply the five required test configurations in order to estimate the AWG harmonic contribution (learning process). Then we only need one additional test per ADC to be tested and the ADC harmonic contribution is estimated by performing a post-processing calibration of the AWG contribution. This single test is captured using a conventional test set-up given by Figure 4-4. It is really important to mention that the single capture is done in a conventional test set-up but there are no more strict requirements relative to the AWG resolution.

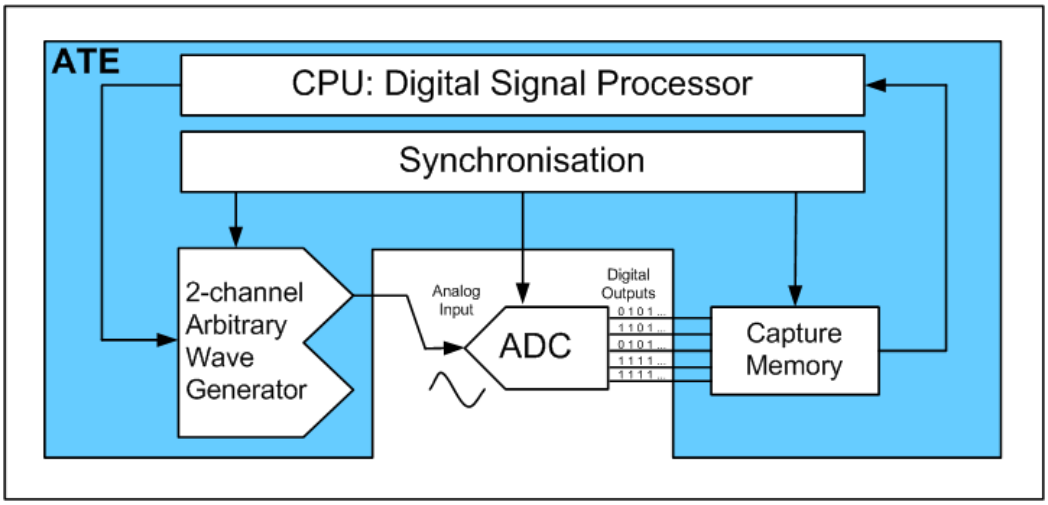

Figure 4-4: Conventional test set-up using a low-resolution AWG for the new approach of industrial ADC test

As a consequence for mass production test, the test time required to know the AWG contribution with the five test configurations is negligible compared to total test time. In other words, the test time required to apply our method is absolutely comparable to the test time required to apply a conventional ADC test but by using this new approach, there is no need for high-performance AWG.

II.4.B Hardware experimental validation

Large sets of hardware measurements were performed to validate the proposed approach. The purpose of the experimentation is to evaluate the efficiency of our method to accurately test an ADC using an AWG of the same resolution. The experimental set-up is first introduced, then the protocol is described, and finally results are presented. The performance of the proposed test strategy is evaluated by comparing the THD and SFDR (cf. eq. 2-4 and eq. 2-15) results with reference measurements. Harmonics from the 2^{nd} to the 10^{th} order were considered for these computations.

II.4.B.a. Experimental set-up

In order to experiment the test strategy, we use a two-channel AWG Sony/Tektronix AWG2021 containing two 12-bit DACs, a resistive splitter/combiner and a 10-bit ADC, as presented in Figure 4-5.

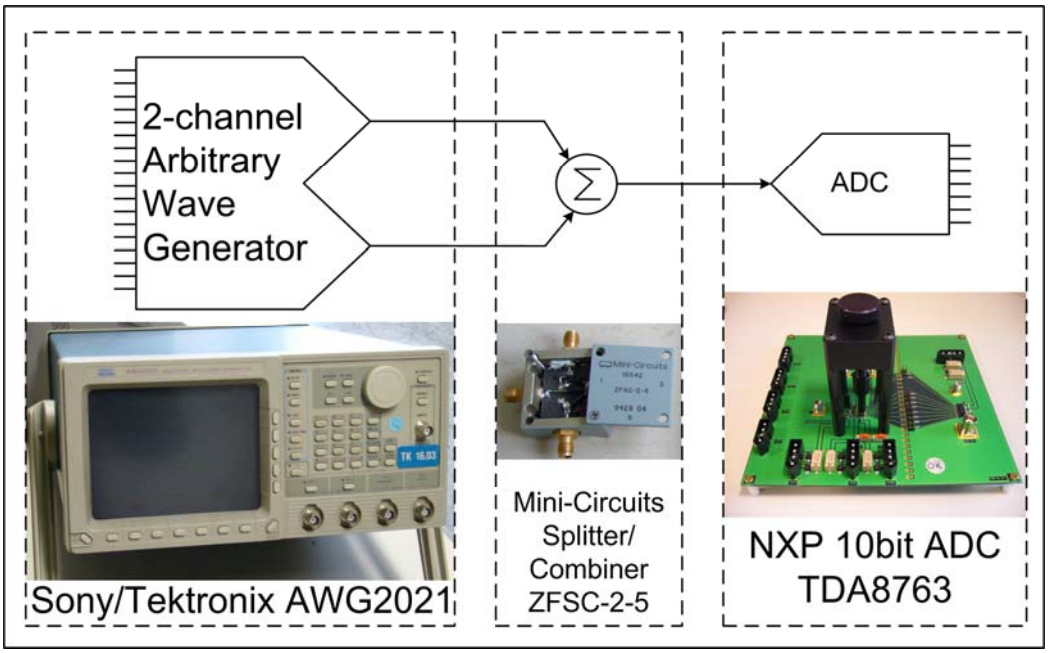

Figure 4-5: Hardware set-up

Moreover, to compare the results of our method to a conventional ADC test, some reference measurements were performed using a usual test set-up with high performance analogue generator.

Finally, to demonstrate that the AWG is not efficient enough to accurately characterize the ADC dynamic performances without the proposed method, the conventional DSP-based method was implemented by directly connecting one output of the AWG to the input of the ADC. Table 4-5 presents the results of this test in comparison with the reference measurements regarding THD and SFDR test parameters.

	THD (dB)	*SFDR (dB)*
Test with AWG2021	-51.6	52.5
Reference test	-68.4	63.5

Table 4-5: Test results for the standard test using low resolution AWG vs. reference test set-up

An error of more than 16dB is observed on the estimation of the THD, and 11dB on the estimation of the SFDR. We observe that even with a 2bits higher resolution, it is not enough for this set-up. As explained in II.2.C, despite the AWG has a resolution of 12 bits, it is not efficient enough to test a 10-bit ADC, because it exhibits worse performances than common 12-bit converters in terms of THD. As a consequence the harmonics measured at the output of the ADC are mainly influenced by the ADC and the AWG.

II.4.B.b. Experimental protocol

In order to validate the method, four ADC samples of the same batch have been tested. These four samples were chosen in order to represent a significant population of converters considering the SDFR and THD variations. Indeed, these samples have THD varying from -60.5dB to -68.3dB and SFDR varying from 63.3dB to 70.3dB.

Each of these four ADCs has been tested with a conventional ADC test procedure to obtain reference measurements. The test has been performed ten times to estimate the repeatability of the technique. The evaluated dynamic parameters are the THD and the SFDR

Then, the proposed method has been applied considering both the 5-test procedure used in the preliminary learning phase and the 1-test procedure used during production test. As for the conventional ADC test, the THD and the SFDR parameters are computed from the estimated values of the harmonic components. Again, the test has been performed ten times on each ADC.

II.4.B.c. Experimental results of the full test procedure

II.4.B.c.1 Learning process validation

In order to validate the learning process that permits to characterize the AWG, the 5-test procedure described in section III.B has been applied to the four sampled ADCs. Results are presented in Table 4-6. This table gives the estimated values of the harmonic components induced by the AWG for 2^{nd} to the 10^{th} harmonics. The right column gives the standard deviation for each harmonic considering the four estimations using the 5-test procedure with four different ADCs.

	ADC #1	*ADC #2*	*ADC #3*	*ADC #4*	σ
H2 (dB)	-59.5	-60.1	-58.7	-58.1	0.9
H3 (dB)	-52.0	-52.1	-52.2	-52.3	0.1
H4 (dB)	-79.7	-77.1	-86.4	-90.6	6.2
H5 (dB)	-84.1	-87.5	-90.7	-94.0	4.2
H6 (dB)	-88.7	-82.9	-84.4	-83.6	2.6
H7 (dB)	-94.5	-108.8	-107.6	-120.9	10.8
H8 (dB)	-93.5	-97.2	-87.9	-85.0	5.5
H9 (dB)	-94.9	-84.3	-91.3	-88.3	4.5
H10 (dB)	-93.7	-105.3	-87.3	-82.7	9.8

Table 4-6: Estimated values of the AWG harmonic components using the 5-test procedure

Looking at the results, it appears that the level of the most significant harmonic components is well estimated when taking into account the different converters used during the 5-test procedure. More precisely in this experiment, the major contributors to the AWG harmonic distortion are H2 and H3. Similar values are obtained for the amplitude of these components whatever the converter used during the procedure (around -59dB for the H2 harmonic and -52dB for the H3 harmonic, with a standard deviation of less than 1dB). For harmonic components with lower amplitude, results show a more important spread depending on the converter used during the procedure. In fact, these harmonics are nearby or below the noise floor and they are not relevant. As a consequence, even a rough estimation of these harmonics will not strongly impact the test procedure efficiency.

In summary, these results demonstrate that the 5-test procedure allows the extraction of the amplitude of the most significant harmonic components induced by the AWG with a good accuracy, whatever the converter used during the procedure.

II.4.B.c.2 Production test validation

Using the AWG harmonic distortion estimated during the learning 5-test procedure, we defined a post-processing on the response of the ADC under test. The objective of this section is to validate the effectiveness of this post-processing calibration of AWG in order to accurately test subsequent ADCs with only a 1-test procedure per ADC.

To this aim, we consider the amplitude of the AWG harmonic components extracted with the 5-test procedure using ADC#1. Then, the 4 samples of ADCs are tested ten times using the 1-test procedure described in section III.C, and post-processing calibration on the response of the DUT is performed to take into account the AWG contribution. Results are presented hereafter in comparison with the reference measurements obtained using a conventional ADC test set-up and a high performance AWG.

Table 4-7 gives the average THD measurements for the four ADC samples tested ten times, using either a conventional ADC test (2nd column) or the 1-test procedure with post-processing calibration (3rd column). Each result is the average of ten measurements. The last column gives the difference between the two measurements.

	THD reference (dB)	*THD estimation (dB)*	*Measurement difference (dB)*
ADC#1	-66.6	-67.3	0.7
ADC#2	-68.1	-66.7	-1.4
ADC#3	-62.6	-62.4	-0.2
ADC#4	-60.5	-60.6	0.1

Table 4-7: Average THD measurements reference test vs. 1-test procedure

Table 4-7 shows that the maximal difference between the proposed method and a conventional ADC test is less than 1.5dB. This result is very interesting especially when we consider the repeatability of the measurement for the same product on ATE that is around 1dB.

Results for the SFDR estimation are given in Table 4-8. As for the THD measurements, we obtain good estimations. The estimation uncertainty (1.2dB) is in the same range of the test production scattering (1.3dB) on the SFDR measurement for the same ADC.

	SFDR reference (dB)	*SFDR estimation (dB)*	*Measurement difference (dB)*
ADC#1	68.7	67.9	0.8
ADC#2	70.1	70.0	0.1
ADC#3	67.0	66.7	0.3
ADC#4	63.3	62.1	1.2

Table 4-8: Average SFDR measurements reference test vs. 1-test procedure

All these results demonstrate that once the harmonic contribution of the AWG has been extracted in the initial learning process, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and post-processing calibration.

II.4.C Estimation of the production test efficiency vs. AWG resolution

The two first experimental validations have brought two conclusions. At first, the 5-test procedure, also called learning phase, gives a stable estimation of the amplitudes of the most significant harmonic components induced by the AWG whatever the ADC used. This conclusion leads to the second experimentation. Indeed the second experimentation allows us to conclude that once the harmonic contribution of the AWG has been extracted in the initial learning phase, it is possible to accurately test the ADC dynamic parameters (SFDR and THD) using the 1-test procedure and a very simple software post-processing calibration. These two first experiments were performed with a 12-bit AWG. It has been demonstrated (cf. II.4.B.a.) that this AWG is not efficient enough to accurately characterize the ADC dynamic performances using the standard DSP-based method. To go further, a third experiment has been carried out in order to estimate the lowest resolution acceptable for the AWG relatively to the accuracy of the new production test results. The purpose of this last experiment is to reach the limit of the application domain of the method.

II.4.C.a. Experimental protocol

The established test set-up is similar to the previous one. It is made of a Sony/Tektronix AWG2021, a resistive combiner, and a 10-bit ADC. The AWG resolution was lowered by increasing its quantization noise.

Two ADCs were tested. Each converter was tested four times, each test being performed with a different AWG resolution (from 12 bits to 6 bits, by steps of 2 bits).

II.4.C.b. Experimental results

Table 4-9 presents the results of THD measurements for the two ADCs. Three different results are given:

- ✓ Reference measurement made with a high performance AWG in a conventional test set-up
- ✓ Estimation with our method
- ✓ Estimation error

Table 4-10 gives the same kind of results as Table 4-9, but for a different dynamic parameter: SFDR

	AWG resolution	*THD reference (dB)*	*THD estimation (dB)*	*Measurement difference (dB)*
ADC#1	12	-61.8	-61.7	-0.1
	10	-61.8	-62.0	0.2
	8	-61.8	-62.4	0.6
	6	-61.8	-61.7	-0.1
ADC#2	12	-59.8	-59.1	-0.7
	10	-59.8	-58.8	-1.0
	8	-59.8	-58.9	-0.9
	6	-59.8	-59.1	-0.8

Table 4-9: THD estimation accuracy vs. AWG resolution

	AWG resolution	*SFDR reference (dB)*	*SFDR estimation (dB)*	*Measurement difference (dB)*
ADC#1	12	63,9	65,1	-1,2
	10	63,9	64,7	-0,8
	8	63,9	65,4	-1,5
	6	63,9	66,0	-2,1
ADC#2	12	63,0	62,8	0,2
	10	63,0	62,6	0,4
	8	63,0	61,8	1,2
	6	63,0	62,1	0,9

Table 4-10: SFDR estimation accuracy vs. AWG resolution

Production test repeatability usually shows variations of dynamic parameters estimation around 1.5dB. Considering this limit of acceptance for dynamic parameter estimations, Table 4-9 and Table 4-10 give some interesting results. Indeed, considering THD estimation for both ADCs, whatever the AWG resolution between 12 bits and 6 bits, there is no estimation error over 1dB. Considering SFDR parameter estimation, there is only one estimation error over this limit; this is for the ADC#1 tested with a 6-bit AWG.

The fact that the limit was not exceeded for the test of ADC#2 can be explained by the difference between the two ADCs reference measurements. Indeed the SFDR reference from ADC#1 is better than the one from ADC#2. In other words, it means that for ADC#1 the highest spurious harmonic is closer to the noise than for ADC#2. As a consequence, the noise contribution to this spurious harmonic is higher. As the noise contribution is random, it induces some measurement variations and errors higher for ADC#1 than for ADC#2.

Anyway, given these experimental results, we can draw some very interesting conclusions. Indeed, let us consider a 10-bit ADC. In order to set up a conventional test, the AWG resolution should be at least of 12 or 13 bits. Using the proposed new approach, the constraints on AWG resolution can be considerably relaxed. ADCs can be tested using 8-bit or less AWG.

II.5 **Conclusion**

We propose an ADC test solution based on the estimation of ADC harmonics and a post-processing calibration on the test response. The method relies on a preliminary learning process in which the AWG harmonic contribution is estimated. The AWG characteristics are then used during production test with a post-processing calibration of the test data in order to take into account the AWG contribution.

Thanks to the proposed method, it is possible to accurately measure ADC harmonics using an ATE with standard-performance AWG, whereas a conventional DSP-based test requires an AWG with a resolution at least 2 bits higher than the ADC under test resolution. This method can be associated to the 2-ADC method [cauv00], that is suited to noise measurements in a test set-up similar to the one required to apply the novel method. Indeed, using these two methods we can test all the ADC dynamic test parameters. As a consequence, one of the main benefits of the method is that it allows the test of a wide range of converters with conventional test equipment, and without the need of customising the test board for every new product. Moreover, after the

learning process, there is no additional test time compared with a conventional ADC test procedure. To go further, it has been proven that using this new approach the constraints on AWG resolution can be considerably relaxed.

The theoretical developments were made under the assumptions that the combiner has no distortion influence and that the ADC is not influenced by dynamic non-linearity. The combiner influence was verified during practical experimentations. The ADC used for practical experimentations was not influenced by dynamic non-linearity. Further theoretical developments would be done in order to take into account ADC architectures that do not prevent dynamic non-linearity.

III Alternate DAC test, relaxing constraints on digitizer performances.

III.1 Introduction

As for the extended application presented in the second part of this section, this extension of the ANC method is dedicated to the test of a stand-alone converter using low performance analogue instrument. For this case, the tested converter is no longer an ADC but a DAC, and the low performance instrument is no longer an AWG but a digitizer.

The ANC test method is based on the discrimination of harmonic contributions from the two DACs and one ADC of a C(2,1) configuration (Figure 4-2). A mass production methodology for DAC testing can be developed based on the ANC approach. This approach is also based on a preliminary learning process, followed by the production test. The learning process, as shown in the second section, consists in learning the harmonics contribution of the digitizer. The second step described in the third section is the mass test production. It consists in testing some DACs using a simple test signal and a post-processing compensation of the digitizer harmonics.

III.2 Learning process

The first step is based on the test set-up presented in Figure 4-6. The set-up is similar to the one used for the conventional ANC test method (Figure 2-26). Instead of using two DACs and one ADC embedded in a system, we now set up two stand-alone DACs and the ADC is replaced by the digitizer of the ATE.

The purpose of this first step is to learn the harmonic contribution of the digitizer. The theoretical approach is the one developed for the ANC method (cf. Chapter 2V). It consists in applying five different test signals and to do five captures. The harmonics computed with these five captured are used to solve a 10-equation system. The results of the solved equation system give the digitizer contribution. Once this harmonic contribution is estimated the second step can be launched.

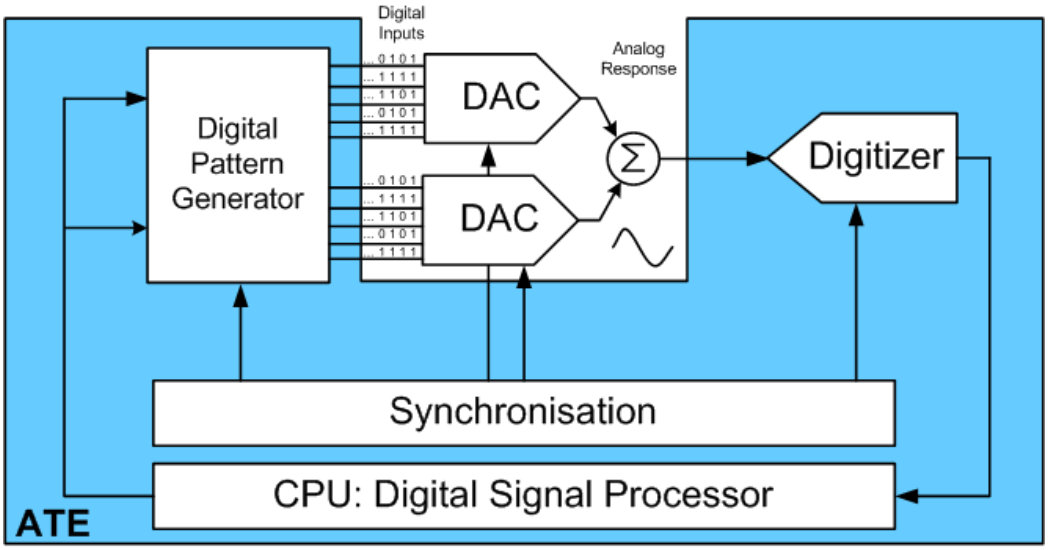

Figure 4-6: Learning step set-up

III.3 Mass test production

The second step is called mass production test step. It is based on the test set-up presented by Figure 4-7. This is a conventional DSP-based test set-up for DAC, but without any constraint on the digitizer performances. Once the harmonic contribution of the low-resolution digitizer is known, using a post-processing calibration of the digitizer, the DAC can be tested using only one test. A mass production test can be based on this approach because it requires a conventional test set-up and a low-resolution digitizer, getting rid of any additional high-performance instrument, while keeping the test time unchanged.

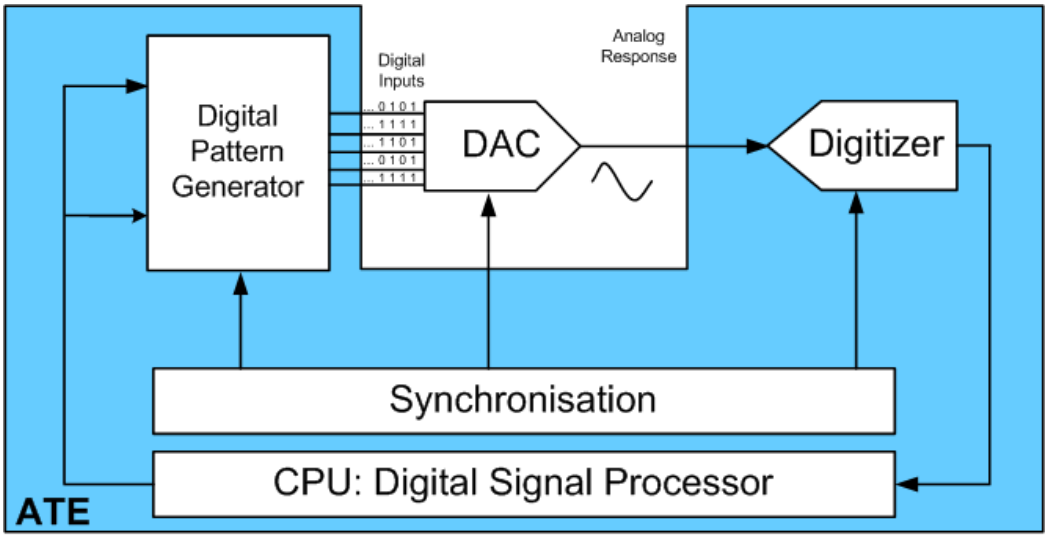

Figure 4-7: Mass production test set-up

IV Self calibration of ATE

This last section goes even deeper in the method extension to additional applications. Let's consider a conventional ATE. It embeds some arbitrary waveform

generators and some digitizers. These analogue instruments usually suffer of low performances and especially low linearity compare to the device under test performances.

The errors induced by the converters embedded in these instruments could be compensated using some calibration routines. For instance [shin06] proposes a digital equalizer to compensate non-linearity of a DAC. In addition Hummels et al from university of Maine develop for years [larr97] [rile98] [iron91] some routines to compensate non-linearity of DAC and ADC using look-up tables. These approaches require a learning process of nonlinearity measurement using a high-performance analogue instrument. This is an issue to the application of such methods to the calibration of ATE instruments. Indeed ATE don't embed the required instruments; as a consequence these calibration routines cannot be easily applied.

Such calibration routines can be automated on ATE using ANC-based method. Indeed let's consider the set-up presented in Figure 4-8.

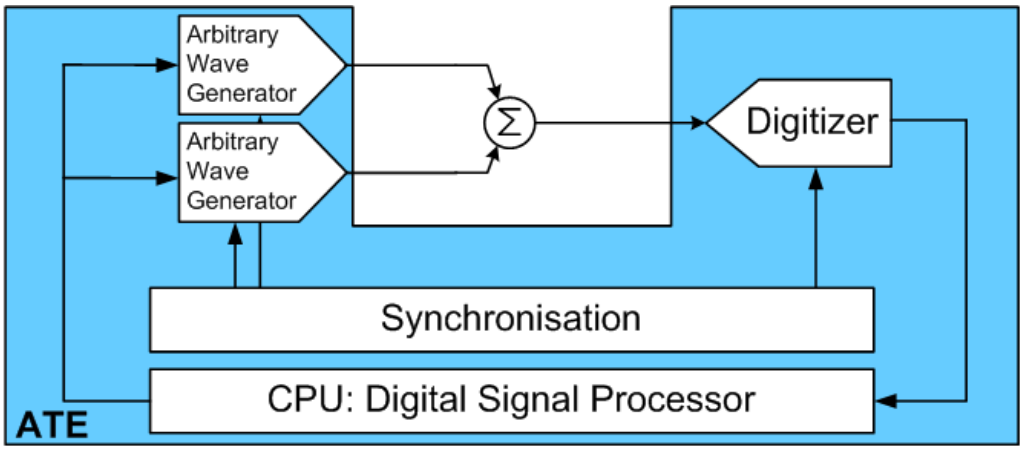

Figure 4-8: Set-up for the calibration of analogue instruments from ATE

This set-up is made of two AWGs and one digitizer. It is similar to the set-up required to implement the ANC method. The AWGs and the digitizer are used instead of the DACs and the ADC. Using the theoretical approach developed for the ANC method (cf. Chapter 2V), we are able to estimate the harmonics induced by the three instruments despite they have similar performances. As a consequence there is no need of high performance analogue instruments. Then it has been demonstrated [jani07] [xu99] that non-linearity and harmonics of converters are linked. As a consequence once harmonics induced by the analogue instruments are known, it is possible to estimate their non-linearity. Once their non-linearity errors are known, some routines could be implemented to compensate the instruments errors.

This additional extension of the ANC method offers a new interesting application. Indeed using the ANC approach in combination with some fully digital compensation routines, it is possible to implement a calibration scheme of ATE analogue instruments without any additional high-performance analogue instrument.

V Conclusion

Initially intended for converters embedded in a mixed-signal integrated system, the ANC method has found other application fields, such as:

- ✓ Industrial test of ADC using a low-resolution AWG
- ✓ Industrial test of DAC using a low-resolution digitizer

- ✓ Calibration / enhancement of ATE instruments

Getting rid of high-resolution analogue instruments for converters testing represents the major benefit of the method, especially for high-end circuits where the performances of the instrumentation are recurrently far behind the DUT requirements.

The first derivative application was validated through initial experiments, and the two other applications will be considered in further studies.

Discussion and conclusion

Test issues are increasingly linked to design trends. Using SiP or SoC technologies, or both, a full system made of RF, analogue and digital cores is commonly embedded in one single package, posing new and complex test challenges. The conventional test approach for RF and analogue is core-based, which becomes unsuitable as far as the number of functions is endlessly increasing while the number of access points is decreasing. Moreover, testing each core independently requires long test times, leading to prohibitive production costs. The main of these issues relative to the system architecture, is the limitation of available test instrumentations. Indeed, in order to test an analogue, RF or mixed-signal component, high-performance instruments are required to generate and/or capture the test signals. As demonstrated in Chap4.II.2, these analogue instruments should have better performances than the device under test to satisfy the accuracy needs. With the combination of the number and the level of performances of the embedded cores, it becomes almost impossible to find an ATE configuration that fulfils the technical requirements together with keeping the costs at a reasonable level.

As a solution to solve this problem, the test is moving from a core-level to a system-level strategy. Several system-level test approaches are already published. They propose to use path-based testing [ozev04] [hald05_2], or loopback-based tests [dabr03] [hald05].

Considering a transceiver, the loopback-based approach could be a very interesting solution. The test signals are generated by a DAC, driven through the transmitter, then through the receiver thanks to a loopback connection, and finally digitized by an ADC. Consequently, a fully digital approach can be used to test the whole transceiver. Re-using the embedded converters as test instruments to generate and capture the test signals looks straightforward and relevant, because, as they are embedded in the system, they should adequately meet most of the test requirements, e.g. clock rate, analogue bandwidth, etc. However, in many cases, the linearity of the embedded converters is not high enough to ensure an accurate test of the path. Therefore, as proposed in [dabr03], they should be at first tested and eventually calibrated.

Focusing on the final purpose: the use of converters as embedded test instruments, we have developed a test method for a set of converters embedded in a system.

Connecting the DACs to the ADCs of the system in the analogue domain represents an attractive solution. Indeed, without any need of analogue instrumentation, only low cost digital equipments are required. We made the assumption that digital access points are easier to manage than analogue ones. To enable this set-up, connecting DACs and ADCs, the concept of Analogue Network of Converters (ANC) was established (see Figure 2-25). Thanks to the ANC, we could be able to sum any DAC outputs and to drive them to any ADC input.

Test parameters of converters are classified in two categories: static and dynamic parameters. According to literature [sunt97] [xu99] [adam02] [csiz99] [kerz06_2] [jani06] [bern03], it is possible to link static parameters to dynamic ones. That is why we have only focused on one kind of parameters, the dynamic ones. Dynamic parameters are computed using two types of data: noise and harmonic distortions (cf. Chap2.II.3.B). By serializing DACs and ADCs, it becomes necessary to discriminate the contribution of each converter on these data to avoid fault masking. Concerning noise, a mature and efficient method exists [cauv00] that is suited with our test conditions (cf. Figure 2-21). Moreover, we have developed a test method to discriminate and estimate the harmonic contributions of the converters of the network.

The new test method has been developed under two realistic assumptions, which were verified afterwards by the experimental validations. The principle is based on a mathematical expression (cf. eq. 2-45) that describes the signal disturbed by a converter. The method has been developed to test the three converters of a C(2,1) configuration. A C(2,1) configuration is a basic version of the ANC, which is made of two DACs and one ADC. In summary, five different test conditions are applied to the network, and five sample sets are captured. The level of the harmonics is computed in order to establish a ten-equation system, with ten unknowns, using the real and imaginary parts of the harmonics. Solving this linear equation system gives the estimation of the harmonics of the three converters of the C(2,1) configuration. Moreover, using the converters of the C(2,1) configuration previously tested , the method can be generalized in using a simple configuration (one DAC one ADC chain). As one of these two converters has been already tested, only one additional capture is required to test one additional converter.

The method was simulated and validated by hardware experiments on real devices. The experiment protocol consisted in varying characteristics of the set-up to be able to estimate the application domain of the method. It was appeared that the critical characteristic is the noise level of the hardware set-up. Nevertheless, Thanks to our new method, we have showed that is possible to discriminate the harmonics of a converter in a C(2,1) configuration using the two other converters with a resolution two bits lower than the resolution of the converter under test. The results were confirmed on several samples of stand-alone converters. Moreover, the generalization of the method was validated by hardware experiments, which also confirmed that the test time is the same as with a traditional test method.

Three additional applications was proposed, addressing the test of stand-alone ADCs and DACs and the calibration of ATE with no need of high-resolution analogue instruments. The test of ADCs using low-resolution AWG was successfully investigated even if some additional experiments would be welcome. In parallel, the method applied to DAC testing and ATE calibration seems to be very promising.

Finally, this study also allows us to anticipate many possible perspectives in the analogue testing area, by exploiting the phase information from signals.

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List of acronyms

ADC: analogue to digital converter
ANC: analogue network of converters
ANN: artificial neural network
AM: amplitude modulation
ATE: automatic test equipment
AWG: arbitrary waveform generator
BER: bit-error rate
BIST: built-in-self-test
DAC: digital to analogue converter
DC: direct current
DfT: design for test
DUT: device under test
ENOB: effective number of bits
EVM: error vector magnitude
FFT: fast fourier transform
FM: frequency modulation
IC: integrated circuit
LF: low frequency
PAN: personal area network
QPSK: quadrature phase-shift keying
RF: radio frequency
Rx: receiver
SEIR: stimulus error identification and removal
SDR: software defined radio
SFDR: spurious free dynamic range
SINAD: signal to noise and distortions ratio
SiP: system in package
SNR: signal to noise ratio
SoC: system on chip
THD: total harmonic distortion to signal ratio
Tx: transmitter
UHF: ultra high frequency
UMTS: ultra mobile telecommunication system
VHF: very high frequency
WLAN: wireless local area network

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RESUME en français

Une nouvelle méthode de test pour les convertisseurs ADC et DAC embarqués dans un système complexe a été développée en prenant en compte les nouvelles contraintes affectant le test. Ces contraintes, dues aux tendances de design de systèmes, sont un nombre réduit de point d'accès aux entrées/sorties des blocs analogiques du système et une augmentation galopante du nombre et des performances des convertisseurs intégrés. La méthode proposée consiste à connecter les convertisseurs DAC et ADC dans le domaine analogique pour n'avoir besoin que d'instruments de test numériques pour générer et capturer les signaux de test. Un algorithme de traitement du signal a été développé pour discriminer les erreurs des DACs et ADCs. Cet algorithme a été validé par simulation et par expérimentation sur des produits commercialisés par NXP. La dernière partie de la thèse a consisté à développer de nouvelles applications pour l'algorithme.

TITRE en anglais

“Analogue Network of Converters”: a DfT Technique to Test a Complete Set of ADCs and DACs Embedded in a Complex SiP or SoC

RESUME en anglais

A new method has been developed to test a pool of ADCs and DACs embedded in a complex SiP or SoC. This method has been developed concidering current test constraints. Indeed due to system design trends, theses constraints are: a few number of access points to the primary inputs of the converters and the increase of the nnumber and the performances of the converters under test. In order to test these converters, we propose to connect them in the analog domain. As a consequence we need only digital test instruments to generate the test stimuli and capture the test responses. A signal processing routine has been developed in order to discriminate the errors from DACs and ADCs. The approac has been validated through simulations and experimentations. Finally I have extend the application domain of the method to the test of stand-alone ADCs and DACs.

DISCIPLINE

Microélectronique (electrical engineering)

MOTS-CLES

Test, analog to digital converter (ADC), digital to analog converter (DAC), system-in-package (SiP), analog network of converters (ANC), dynamic parameters, total harmonic distortion (THD), spurious free dynamic range (SFDR)

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