Enhancement technique for dynamic CMOS current mirror : Application to high-performance current sources in biomedical devices.

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Solutions pour l'amélioration des performances des miroirs de courant dynamiques CMOS : Application à la conception de source de courant pour des dispositifs biomédicaux

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Doctoral Thesis

Enhancement Techniques for Dynamic CMOS current mirror: Application to high performance current sources in biomedical devices

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Nomenclature

ADC	Analog-to-Digital Converter
BIA	Bio-Impedance Analysis
CCII	Current Conveyor of second generation
CM	Current Mirror
CMOS	Complementary Metal Oxide Semi-conductor
COA	Current Operational Amplifier
DAC	Digital-to-Analog Converter
DCO	Diode-connected
IRRC	Input-Referred Regulated Cascode configuration
LDO	LowDrop-Out regulator
NL-CCII	Non-linear Current Conveyor of second generation
OPAMP	Operational Amplifier
OTA	Operational Transconductance Amplifier
PM	Phase Margin
SFDR	Spurious-Free Dynamic Range
SSPA	Switching-Sequence Post Adjustment
THD	Total Harmonic Distortion
V_{EFF}	MOS device drive voltage ($V_{GS} - V_{TH}$)
VCCS	Voltage-Controlled Current Source
WSCASC	Wide-Swing Cascode configuration

French abstract

Solutions pour l'amélioration des performances des miroirs de courant dynamiques CMOS :
Application à la conception de source de courant pour des dispositifs biomédicaux.

Contexte Scientifique

Les sources de courant statiques, mais aussi dynamiques, sont présentes dans la quasi-totalité des circuits intégrés. Elles sont généralement implémentées en tant que sous-circuits pour la construction de fonctions plus complexes. Pour certaines applications, telles que les convertisseurs de tension DC/DC, les circuits analogiques de traitement du signal, la mesure de bio-impédance ou encore la stimulation électrique de tissus vivants, l'implémentation des sources de courant est soumise à de fortes contraintes et domine le budget et les ressources alloués pour la conception du système complet. Dans le but d'améliorer les performances des dispositifs analogiques ou mixtes, il est courant d'agir au niveau "système". Ainsi, lorsqu'on dispose de ressources digitales, la calibration ou l'intégration de mécanismes d'auto-correction, permettent de compenser les erreurs dues aux défauts des sous-circuits. Il est cependant possible de s'attaquer aux défauts directement par la recherche de topologies de sous-circuits à hautes performances. Les travaux présentés ici, portent sur l'analyse, les méthodes de conception et la recherche de nouvelles structures de sources de courant, en se focalisant principalement sur les miroirs de courant (CM). Depuis la naissance des circuits intégrés jusqu'à aujourd'hui, des groupes de recherche s'intéressent à ces problématiques. Comme on peut le constater sur la figure 1, le miroir de courant CMOS en lui-même est un sujet continuellement étudié malgré les différentes évolutions des méthodes de conception ou des technologies que la micro-électronique a connues.

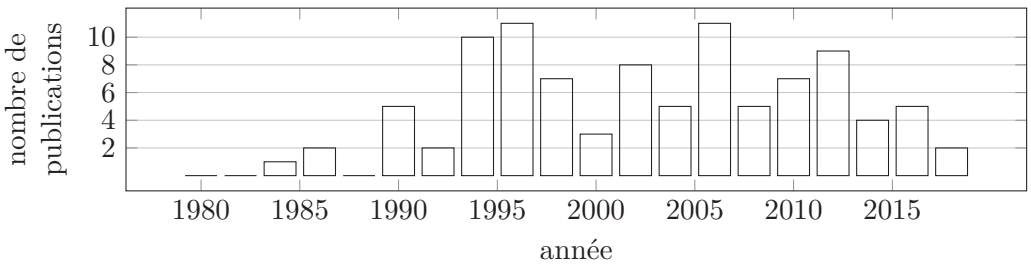
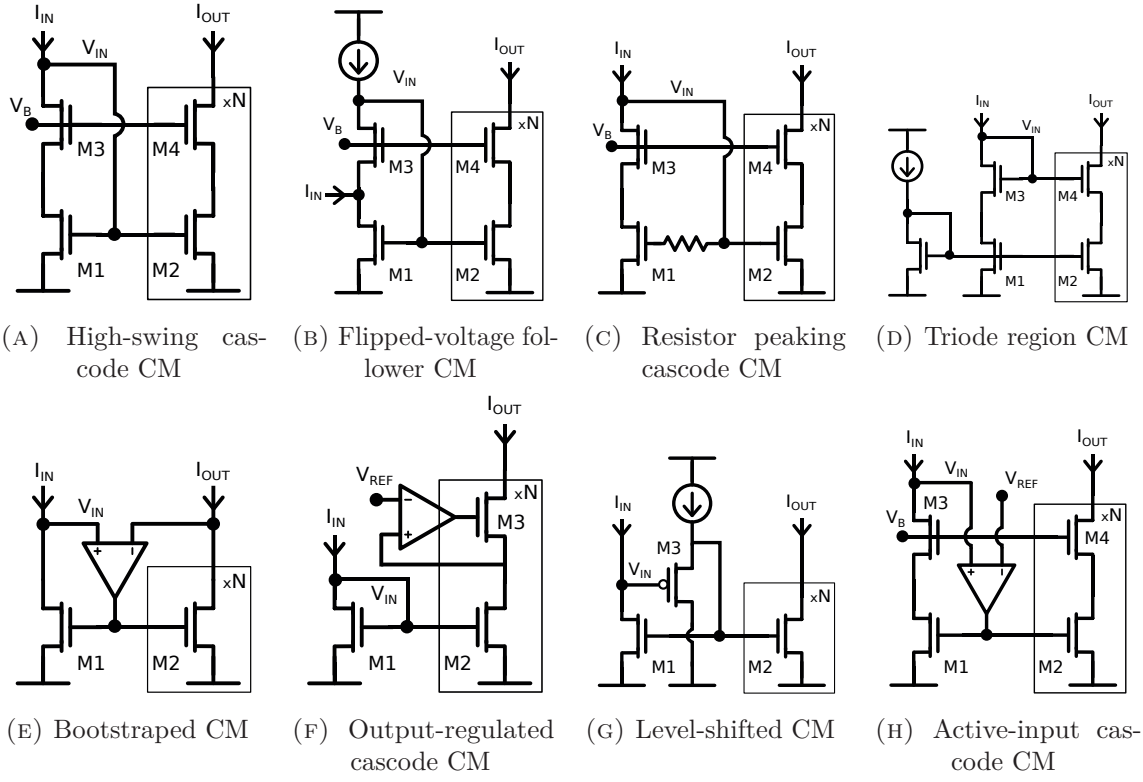


Figure 1 – Chronologie des publications concernant les miroirs de courant CMOS dans les journaux ou conférences internationales de la communauté IEEE

Les caractéristiques principales des miroirs de courant statiques sont la consommation en puissance (ou le rendement énergétique), les plages de tension acceptables pour l'entrée et la sortie ainsi que la précision de la recopie. Dans le cas d'une utilisation dynamique des miroirs de courant, la vitesse et la linéarité deviennent des performances complémentaires à prendre en compte. On peut noter que c'est généralement le budget en puissance qui fixe le compromis entre les performances statiques et le comportement dynamique. Il existe une grande variété de topologies de miroir de courant, offrant aux concepteurs différentes solutions pour optimiser les caractéristiques de leurs architectures. La figure 2 présente un ensemble de topologies populaires ayant permis la conception de systèmes à haut niveau de performances.



(A) High-swing cascode CM (B) Flipped-voltage follower CM (C) Resistor peaking cascode CM (D) Triode region CM

(E) Bootstraped CM (F) Output-regulated cascode CM (G) Level-shifted CM (H) Active-input cascode CM

FIGURE 2 – Différentes structures de miroirs de courant utilisées en conception CMOS

Le premier chapitre de ce manuscrit débute par la mise en exergue des origines des contraintes limitant les performances des miroirs de courant CMOS. Vient ensuite, une revue des différentes solutions proposées par le passé pour pallier ces contraintes. Des solutions intervenant aussi bien au niveau système qu'au niveau des sous-circuits sont envisagées. Cependant, de l'étude de l'état de l'art vient un premier constat : la littérature scientifique recense peu de solutions visant à optimiser spécifiquement le compromis vitesse-précision-consommation d'un miroir de courant. Compromis pourtant fréquemment étudié et inévitablement rencontré dans les nœuds technologiques avancés pour la conception de sources dynamiques. Le dépassement des limites actuelles lors de l'optimisation du compromis vitesse-précision-consommation est l'objectif majeur des travaux présentés.

Modélisation et optimisation de miroirs de courant classiques

Dans le but de comprendre et d'agir sur les limites discutées précédemment, la mise en place d'outils analytiques est nécessaire. La mise en équation du compromis vitesse-précision-consommation, à partir de modèles approchés du comportement des transistors, est une étape qui permet de cibler les paramètres principaux influant sur les liens entre ces trois performances. Ainsi dans le chapitre 2 nous mettons en place un formalisme, basé sur les modèles classiques des transistors CMOS, dédié à l'optimisation des miroirs de courant. De cette première étude théorique découle une proposition de stratégie de conception ainsi qu'un ensemble de métriques qui vont nous permettre d'explorer différentes solutions pour la réalisation de miroirs rapides et précis à haut rendement énergétique. La figure 3 est une illustration de la stratégie adoptée pour le développement des topologies de miroirs de courant proposées dans ce manuscrit. Cette approche préconise de choisir les dimensions, le gain en courant et la polarisation des transistors effectuant la copie en courant en fonction des performances statiques visées (précision, plage de fonctionnement et efficacité énergétique). Le comportement dynamique, et plus spécifiquement la vitesse, est traité dans un second temps via l'ajout de bloc actifs supplémentaires.

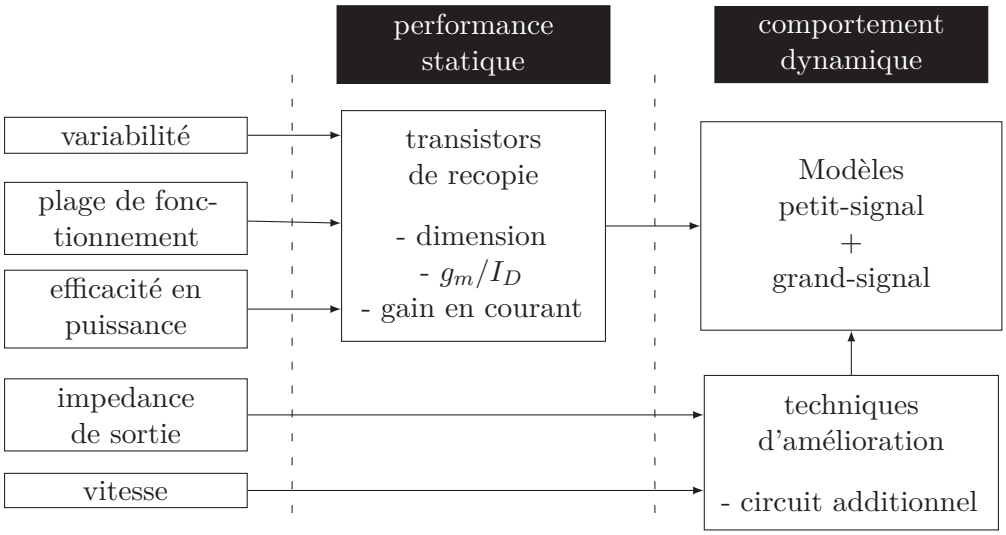


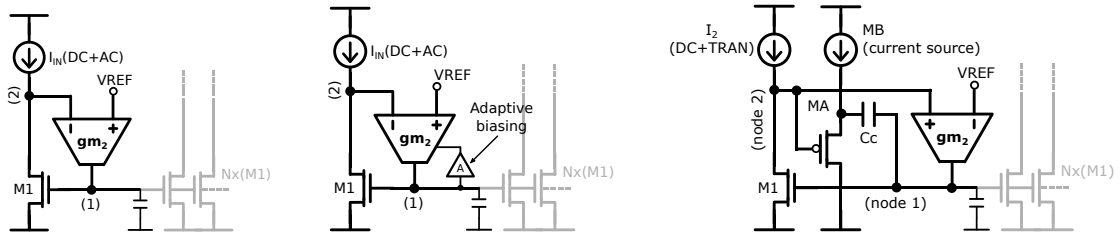
FIGURE 3 – Synthèse de l'approche de conception développée pour des miroirs de courant à haute performance

Dans le chapitre 2, l'analyse porte sur les structures de miroir de courant classiques et plus précisément sur les miroirs pour lesquels la branche d'entrée est montée en diode (figures 2a, 2b, 2d, 2f). Il est montré que pour de tels miroirs, indépendamment de la performance optimisée, le lien entre vitesse, précision et consommation est fixé, et donc limité, par des constantes technologiques dépendant seulement de la nature et de la qualité du procédé de fabrication. Reste alors la piste des miroirs à entrée active dans lesquels la tension de grille est régulée au travers d'un bloc de rétroaction actif (figures 2e, 2g, 2h)

Étude des structures de miroir à entrée active

Une des premières contributions de nos travaux de recherche a été de proposer un formalisme dédié à l'analyse et au dimensionnement de la structure classique de miroir à entrée active

sous la forme montrée figure 4a. Les outils analytiques mis en place dans le chapitre 3 servent à identifier les possibilités et limites offertes par ce type de topologie pour améliorer la vitesse d'un miroir de courant avec un budget en puissance minimal. La précision et la consommation, considérées comme performances statiques, sont initialement fixées par les choix de conception appliqués aux transistors effectuant la copie en courant. Les résultats cette étude montrent qu'il est effectivement possible de réduire le temps de réponse d'un miroir de courant au moyen d'une rétroaction linéaire basée sur un amplificateur de transconductance (OTA). Ainsi, sous certaines conditions la structure classique de miroir à entrée active permet de relâcher le compromis vitesse-précision-consommation. Cependant on observe plusieurs limitations, indépendantes du budget en puissance accordé, restreignant la vitesse et l'allure de la réponse réalisables.



(A) Miroir à entrée active classique (B) Proposition de miroir à entrée active avec polarisation adaptative (C) Proposition de miroir à entrée active stabilisé

FIGURE 4 – Miroirs de courant à entrée active basés sur des rétroactions linéaires

La première limitation intervient lorsqu'on cherche à faire fonctionner le miroir de courant sur un grande plage de courant. En effet, une variation du courant d'entrée du miroir entraine une variation du point de fonctionnement des transistors effectuant la copie en courant et par conséquent une modification de leurs caractéristiques intrinsèques (i.e g_m ou r_{out}). Le gain de la rétroaction (ou transconductance de l'OTA) étant fixe, le déplacement du point de fonctionnement du miroir a pour effet de désaccorder la boucle de régulation, avec pour conséquence soit une dégradation de la vitesse finale soit l'apparition d'un dépassement et/ou de pseudo-oscillations dans la réponse temporelle. Pour remédier à ce problème, nous proposons une amélioration de la rétroaction, rendant le gain de boucle dépendant du point de fonctionnement. La polarisation de l'OTA est rendue proportionnelle à la tension de grille du miroir comme illustré figure 4b. Cette solution permet d'assurer le gain en vitesse offert par la structure classique de miroir à entrée active sur une plus large gamme de courant.

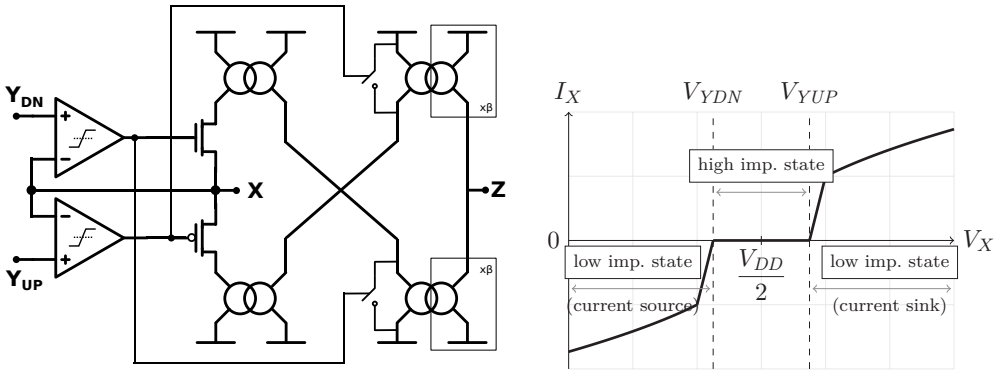
La principale limitation concerne les conditions de stabilité de la structure qui contraignent sévèrement la plage des vitesses accessibles. De plus, la condition de stabilité dépend de caractéristiques intrinsèques des transistors de recopie, telles que leurs impédances de sortie (r_{out}) ou leurs facteurs de transconductance (g_m), réduisant le degré de liberté de réglage dont on dispose. La topologie montrée figure 4c, est proposée pour élargir le domaine de stabilité à moindre coût et donc élargir la plage de vitesse accessible. La solution repose sur l'introduction d'un circuit de compensation de l'OTA, réalisé à partir d'un suiveur de tension et d'une capacité stabilisant la réponse du miroir. Un formalisme ainsi qu'une méthode de conception dédiés à l'optimisation de cette structure améliorée accompagnent

l'implémentation CMOS présentée figure 4c. La méthode est construite selon la technique classique de compensation de pôle dominant. Les conclusions de cette étude montrent qu'il est possible d'atteindre des vitesses supérieures à celles obtenues avec la structure classique pour un miroir donné. Enfin, nous montrons également qu'avec cette solution, au 1^{er} ordre le domaine de stabilité n'est plus défini par les caractéristiques intrinsèques des transistors de recopie mais est directement lié à la consommation dédiée au circuit de rétroaction.

Cependant, bien que ces topologies de miroir à entrée active présentent des avantages pour la construction de sources de courant précises, rapides et faible consommation, la nature des limites mises en évidence nous a poussé à poursuivre la recherche de nouvelles formes de régulation.

Nouvelle approche de régulation basée sur une rétroaction non-linéaire en mode courant

Le développement d'une approche de conception utilisant un principe de rétroaction non-linéaire en mode courant est l'objet du quatrième chapitre et constitue la contribution majeure de cette thèse. La rétroaction est réalisée grâce à un convoyeur de courant de seconde génération (CCII) très faible consommation ayant un comportement volontairement non-linéaire. L'allure de la caractéristique d'entrée ainsi qu'une vue simplifiée de la structure du convoyeur de courant développé sont présentées figure 5. La caractéristique non-linéaire de la régulation permet de dissocier les contraintes liées aux spécifications statiques et les contraintes liées au fonctionnement dynamique. Le remplacement du circuit de contre-réaction en mode tension (OTA), présent dans les topologies de miroir à entrée active précédentes, au profit d'une régulation en mode courant (CCII), permet d'élargir significativement le domaine de stabilité du système bouclé tout en offrant un degré de liberté supplémentaire pour le réglage de la réponse temporelle. La proposition d'implémentation CMOS s'accompagne ici aussi d'un formalisme théorique pour l'optimisation de ce nouveau type de miroir à entrée active. Les conclusions de l'analyse montrent qu'il est possible d'obtenir des vitesses largement supérieures à celles obtenues avec les structures classiques tout en assurant un impact minimal sur la précision ou le rendement énergétique du miroir à accélérer.



(A) Schéma simplifié (B) Allure de la caractéristique I-V de l'entrée

FIGURE 5 – Convoyeur de courant non-linéaire proposé pour la régulation de miroir de courant

Les meilleurs résultats ont été obtenus avec la structure présentée figure 6 qui combine, la régulation non-linéaire en mode courant de la vitesse avec une rétroaction sur la branche de sortie de type cascode régulé, pour une copie en courant précise. Cette dernière topologie constitue une source de courant élémentaire compétitive pour la réalisation de systèmes à haut niveau de performances statique et dynamique, capable de générer des courants sur une large gamme allant de quelques dizaines de µA à plusieurs mA.

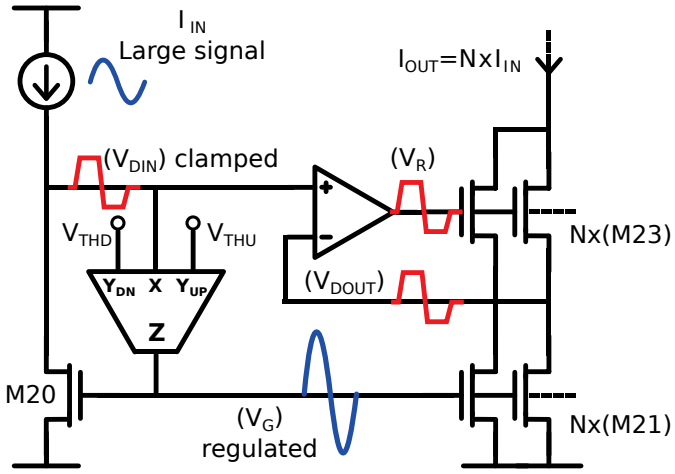


FIGURE 6 – Schéma de la topologie combinant, cascode régulé sur l'entrée et rétroaction à base de convoyeur de courant non-linéaire, illustrée pour un comportement en grand-signal

Application à la conception de dispositifs biomédicaux

Dans le dernier chapitre, l'approche de conception discutée chapitre 4 est mise en œuvre puis validée par la réalisation, en technologie CMOS 0.18 µm (AMS puis TSMC), de deux étages de génération de courant de sortie d'un implant dédiée à de la stimulation neurale. La stimulation neurale consiste en l'excitation par un courant électrique de cellules nerveuses présentes chez un sujet vivant, dans le but de provoquer artificiellement une réaction physiologique en exploitant l'amplification naturelle du système neuro-musculaire. La stimulation électrique est une technique d'ingénierie biomédicale très plus populaire. On la retrouve dans les pacemakers, les implants cochléaires ou les implants rétiniens et plus généralement dans la majorité des neuro-prothèses.

L'objectif du premier circuit, fabriqué en technologie AMS, est de vérifier la faisabilité d'une implémentation sur silicium de la régulation non-linéaire en mode courant. Un autre résultat attendu était la validation de la stratégie de conception proposée. A savoir, l'application de techniques d'amélioration de vitesse faible consommation, à des miroirs de grande dimension à faible variabilité et haute précision. Cependant, en raison des reports multiples de la fabrication des puces par AMS, seul les résultats de simulation sont disponibles. L'opportunité de tester les circuits dans un futur proche reste très incertaine.

On retrouve en figure 7 un diagramme simplifié de l'architecture de l'étage de sortie fabriqué en technologie TSMC. Cette seconde version, est un exemple de réalisation d'un étage de génération de courant d'une puce de stimulation neurale bi-polaire (deux sorties dans le

plan anodique et deux sorties dans le plan cathodique). Le circuit s'interface avec un micro-contrôleur et offre plusieurs niveaux de configurabilité. D'une part, il est possible d'ajuster les temps de réponse de chacune des quatre sorties indépendamment pour un contrôle plus fin des timings. D'autre part le système propose deux modes de fonctionnement : un mode *miroir* dans lequel chaque sortie conduit le même signal (polarité inversée entre anodes et cathodes) et un mode *electrode* dans lequel anodes et cathodes sont court-circuitées pour générer des formes d'onde centrées à valeur moyenne nulle. Dans ce dernier mode le système peut aussi être utilisé en tant que source de courant pour de la mesure de bio-impédance. Le circuit délivre un courant allant de 100 µA à 2.3 mA sur chaque sortie avec un temps de réponse variant de 150 ns à 1 µs en fonction de l'amplitude du signal. L'efficacité en puissance moyenne est supérieure à 90 % et l'erreur relative maximale de la copie en courant mesurée (1σ) est inférieure à 0.4 %

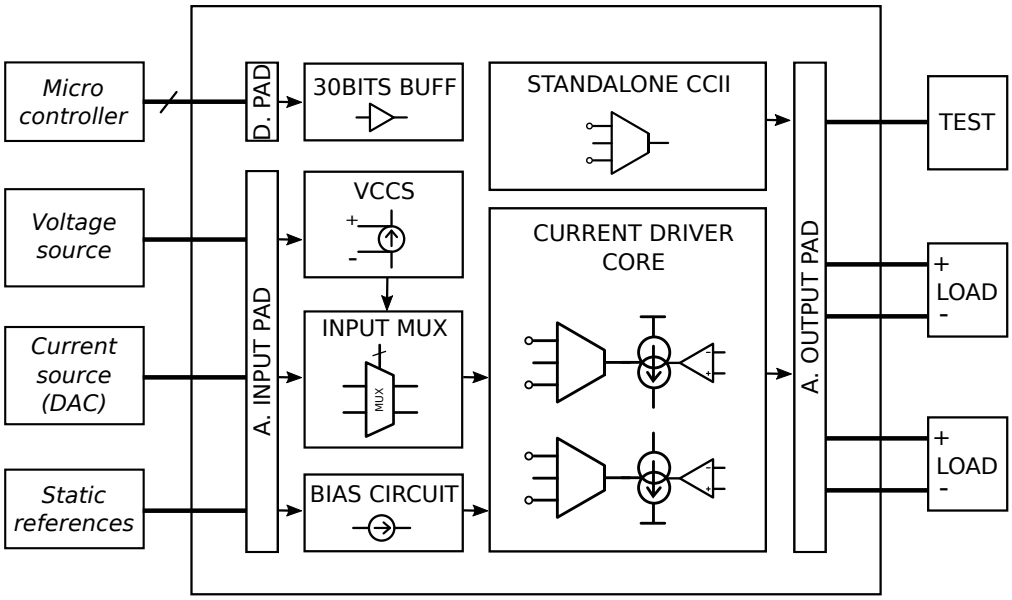


FIGURE 7 – Architecture de l'étage de sortie programmable réalisé en technologie CMOS 0.18 µm TSMC

Afin de confirmer la pertinence scientifique des circuits fabriqués, nous avons comparé les performances avec des travaux précédemment publiés dans la littérature, selon trois champs d'application : les stimulateurs neuraux implantés, les drivers de courant pour de l'analyse de bio-impédance, et différentes architectures avancées de sous-circuit tels que les convoyeurs de courant, les amplificateurs en courant, et les miroirs de courant améliorés.

L'ensemble des résultats obtenus dans les chapitres 4 et 5 démontre qu'il est possible de dépasser les limites actuelles du compromis vitesse-précision-consommation en se basant sur la stratégie de conception et les nouvelles topologies de miroir à entrée active proposées.

Preamble

The work presented in this manuscript has been carried out at the LIRMM laboratory in Montpellier, France. The author was part of the smartIES team. Their major interests are oriented towards biomedical applications and implantable devices. This study was initiated by the will of the team to develop analog functional blocks in CMOS technology for future chips. And more precisely at this time, to develop custom current source architectures for the next neural stimulation chip. However, it should be mentioned that the approaches discussed later in this document have been made generic and not driven by any specific application. Fields covered should not be restricted to those related to biomedical circuit design.

The work involves analysis, design methods and search for improved structures of current mirrors, the most elementary current source and basic building block of analog circuits. Over the past, the literature has offered a large variety of enhanced current mirror topologies. However, the first ascertainment we have made is that only few published topologies directly address the speed-power-accuracy trade-off, even though this trade-off is frequently studied and unavoidable during the design of current sources. This observation, was the starting point of the work presented in this manuscript and has fixed its primary objective:

Outperforming the present limitations in terms of speed, power and accuracy that exists in CMOS current mirror design.

The reader will find in Chapter 1 more elements about the scientific context, the origins of the challenges in CMOS current source design, the potential application fields and a literature review of design techniques dedicated to current sources and current mirrors improvements. The Chapter 2 is dedicated to the analysis and modelling of classical current mirrors with main focus on effects of static and/or dynamic optimisations. In Chapter 3, capabilities of standard active-input current mirror to relax the trade-off between speed, power and accuracy are investigated. Follow then, two solutions proposed to enhance the standard active-input structure at low costs. Major contributions are introduced and detailed in Chapter 4. We present, analyse and illustrate a novel design approach that relies on a power-efficient speed boosting technique based on current-mode non-linear control loops. The CMOS implementation comes with a theoretical design-oriented analysis of the structure, along with results on a practical realisation in TSMC 180nm technology. Introduction of last discussed structures to the design of biomedical current generators is presented in Chapter 5. Two circuits have been sent to manufacturing. Comparison between post-layout simulation results and previous published work are examined. The last chapter is devoted to discuss and conclude about assertions and outcomes of the study.

Chapter 1

Scientific Context

1.1 Context and challenges

The reader will find in this section, several examples of applications where current sources are among the most constrained sub-circuits in their architectures. Then, will follow a set of design techniques used in recent publications to counteract undesirable effects. But before, we will move to the origin and nature of the constraints encountered in current sources or current-mode[1]designs. We will see that advanced technological nodes enable very large scale integration but require new strategies with more design efforts to ensure good performances and yields. In his book, *CMOS current-mode circuits for data communications* (Yuan, 2007), F. Yuan dedicates a complete chapter on design techniques for current-mode circuits and starts with the following assertion, which concisely outlines the major challenges:

"Rapid down-scale of the feature size of MOS devices, the aggressive reduction in the supply voltage, and the moderate reduction in the threshold voltage of modern CMOS technologies have greatly affected the performance of CMOS current-mode circuits, reflected by a small dynamic range, a reduced effective gate-source voltage, a low device output impedance, and an increased level of device mismatches."

1.1.1 Current source design trade-off

Processing, amplifying or conveying current signals typically requires both static and dynamic current sources. Several performances are shared by both type, but as further discussed, dynamic operation brings additional difficulties. Optimizing static and dynamic performances at once leads to conflicting decisions.

[1] *Current-mode* circuits commonly refers to systems where information is conveyed using currents. They are often opposed as *voltage-mode* circuits. The term has been employed in many publications but should be used with care as it is ambiguous and no clear divide between the *current-mode* and *voltage-mode* approach can be stated (Schmid, 2003) (Gilbert, 2004)

Variability: the source of issues

Many analog and mixed signal circuits are based on the availability of supposed *identical components*. Differential pairs, comparators, current mirrors work under this assumption, but also A/D and D/A converters, bandgap references or PLLs. However, with devices approaching the nanometre sizes, atomistic and statistical effects become more and more dominant and manufacturing sufficiently *identical components* is merely impossible.

Among phenomenons inducing differences between two supposed identical devices, we need to distinguish effects that are deterministic from effects that are purely random. For instance, influence of power supply variations or temperature, can be predicted and kept under control. These are deterministic differences. But influence of phenomenons such as dopant fluctuation, edge roughness, noise or trapped oxide charges, often more related to the intrinsic matter composing the device, can not be anticipated. They are random processes and should be studied using probabilistic tools.

In CMOS processes, random differences arise at different scales. We measure wafer to wafer variations, die to die variations but also variations within a single die. Fluctuations observed between two supposed *identical components* inside a selected circuit is referred as *device mismatch* as depicted in Fig. 1.1.

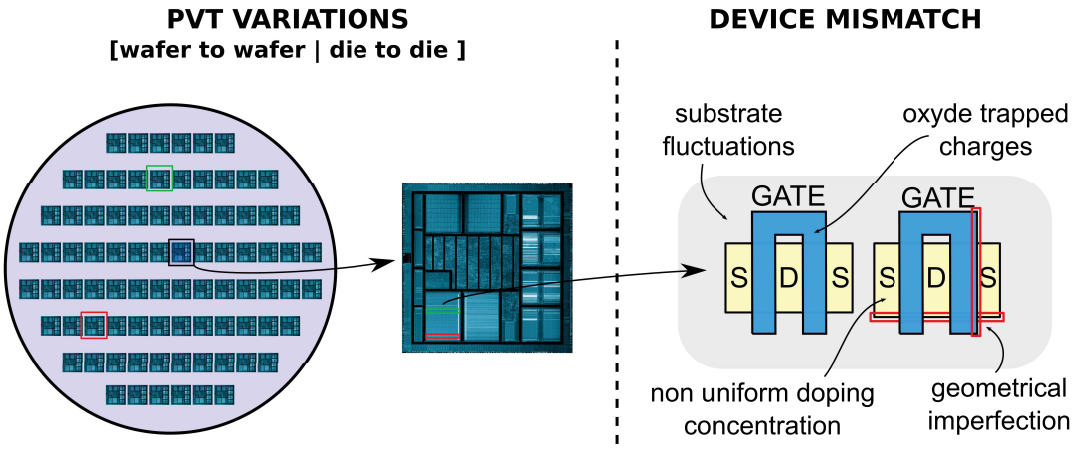


FIGURE 1.1 – Process-Voltage-Temperature variations and device mismatch in CMOS process

Mismatch in devices characteristics is commonly treated using random variables (x_i) for parameters subject to variations in equations ($y = f(x_i)$) modelling the device behaviours. Distributions of variables x_i are typically Gaussian due to the numerous random sources that contribute at atomic scale. Parameters are characterized by a typical (or average) value $\mu(x_i)$ and a standard deviation $\sigma(x_i)$. $\sigma(x_i)$ quantifies the parameter dispersion around the average value, such that for $\approx 68\,\%$ of the circuits fabricated, the measured parameter value will fall in the interval $\mu(x_i) \pm \sigma(x_i)$.

With y a differentiable function of random variables x_i reflecting the device behaviour and x_i modelling independent parameters, the resulting standard deviation of y is calculated with the formula (1.1). We note that the expression is similar to a RMS (Root Mean

Square) calculation, meaning that the largest random sources will determine the outcome.

$$\sigma(y) = \sqrt{\sum \left(\frac{\delta y}{\delta x_i} \sigma(x_i) \right)^2} \tag{1.1}$$

In the well-known MOSFET quadratic current law (1.2) dominant random sources are represented as fluctuation over threshold voltage V_{TH} and β parameter (Pelgrom, Duinmaijer, and Welbers, 1989). Mismatch amount (or fluctuations amplitude) is characterized by the value of $\sigma(V_{TH})$ in mV and $\frac{\sigma(\beta)}{\beta}$ in % and are typically modelled as in (1.3) and (1.4). These fluctuations occur during the manufacturing process and depend on both physical and layout properties. Values of A_{VTH} and A_β are experimental ones and supplied by the foundry according to the process used.

$$I_D = \frac{\mu C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 = \frac{\beta}{2} (V_{GS} - V_{TH})^2 \tag{1.2}$$

$$\sigma^2(V_{TH}) = \frac{A_{VTH}^2}{WL} \tag{1.3}$$

$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{\sigma^2(W)}{W^2} + \frac{\sigma^2(L)}{L^2} + \frac{\sigma^2(\mu)}{\mu^2} + \frac{\sigma^2(C_{OX})}{C_{OX}^2} = \frac{A_\beta^2}{WL} \tag{1.4}$$

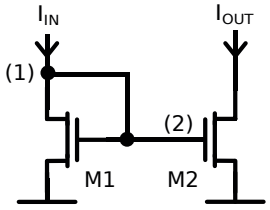


FIGURE 1.2 – Basic diode-connected current mirror

Accuracy of the current copy or amplification using currents mirrors is essentially determined by the ability to match their transistors. For the elementary current mirror shown in Fig. 1.2, the relative mismatch error on the output current can be formulated as in (1.5).

$$\frac{\sigma(I_{OUT})}{I_{OUT}} = \sqrt{\frac{\sigma^2(\beta)}{\beta^2} + \kappa \sigma^2(V_{TH})} \tag{1.5}$$

The term κ in the equation above depends the device operating point. Table. 1.1 shows the approximate expressions for the weak and strong of inversion regimes. It is the second degree of freedom with device area, that designers have to size transistors with care for accuracy.

This representation of variability is necessarily an approximation of all random phenomenons that occur in reality in CMOS technology. However it offers a good compromise between model complexity and accurate results (Yeh et al., 2001). In addition, we have seen before that due to the RMS summation in standard deviation, only dominant random sources will eventually count. Hence, equations (1.3), (1.4) and (1.5) demonstrate that to

general expression	$\kappa = \frac{gm^2}{I_{IN}^2}$
strong inversion	$\kappa = \frac{4}{(V_{GS} - V_{TH})^2}$
weak inversion	$\kappa = \frac{1}{(\eta \frac{kT}{q})^2} \qquad \eta \approx 1.25$

TABLE 1.1 – Scaling factor for V_{TH} variations versus polarization

minimize random source effects it is recommended to use large gate areas ($W \times L$) and large gate-source voltages (V_{GS}) for matched devices. We will see in the next sub-section, that those two general recommendations become inconsistent if we search to optimize dynamic operation. Mismatch in current mirrors is further investigated in Chapter 2.

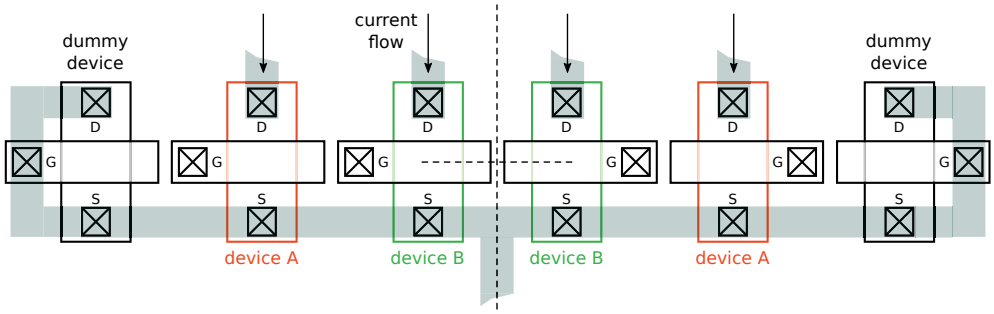


FIGURE 1.3 – Illustration of common-centroid technique for mismatch reduction in current mirror

From the transistor layout point of view, several techniques and good practices are essential to get the most of the features offered by the process. Popular recommendations are illustrated Fig. 1.3. Common centroids or inter-digitized structures average spatially distributed errors and reduce mismatch due to gradient effect during process. But because devices have constrained locations and orientations, the interconnect headroom tends to increase. We can add that, large shapes or patterns are less sensitive to lithography imperfections. In addition, dummy devices should be added around matched structure to ensure that each device, especially devices located on borders, share similar environment. Matching devices in layout costs die area. Another important rule in layout concerns the relative orientations. To preserve symmetry between matched devices, currents have to flow in the same direction, source and drain of each transistors have to be oriented accordingly. Indeed, tilted ion implantation used for proper n/p diffusions results in asymmetric parasitics capacitances for sources and drain areas. This effect may introduce significant differences if the rule of orientation is neglected (Pelgrom, Duinmaijer, and Welbers, 1989).

Finally within computer-aided design software, it is always possible to prototype with exactly *identical devices* but the manufacturing process introduce random errors. These effects have been studied for many years and have become more and more critical with the latest technological nodes. As argued before minimizing random errors at transistor level leads to large dimensions in many aspect of the design. Transistor sizes are kept far from minimal dimensions. Matched layout structures typically need more room and bigger interconnects. But in many cases, for static current sources it is an appropriate solution.

When working with dynamic current sources, choices made to counteract random effects will be paid by a limited dynamic operation or a significant increase of power consumption.

The technology constraints the speed-power-accuracy trade-off

Each application has a specific type of time-variant signals which need to be handled by dynamic current source. That being said, there are still typical performances that are commonly used to characterize sub-circuits amplifying or conveying current signals. They can be divided into the following categories:

- **Accuracy:** So far, only random sources of error have been discussed, but they always add on top of systematic and predictable errors. They come from well-known transistor characteristics, such as *vds*-modulation or bulk-modulation, and are included in behavioural models provided by modern design kits. At transistor level this concerns design parameters like output-impedance (r_{DS}) and bulk bias voltage (V_{BS}). At system level, predictable errors generally impact the linearity, reduce the load compliance and constraint the dynamic range of signals carrying the information.
- **Speed:** According to the type of signals (broadband, pulse, sine ...) we found specifications formulated as bandwidth, settling times or slew-rate, but they all refer to the general speed performance of the current source. Many times for a system, with speed enhancement solutions come stability issues. Hence, studying speed involves studying the stability condition. Also, amplitudes and dynamic ranges may significantly differ, for example between internal signals and signals going off-chip, so speed and stability should be studied for both small and large signal behaviours.
- **Power consumption:** From physical perspective, deterministic and random phenomenons that affect the information conveyed by the system can be seen as a loss of energy, eventually dissipated as heat, that will not be transmitted to the next stage. To actively compensate those effects, some energy has to be externally supplied to the system. An efficient use of the total power dedicated to a current-mode circuit is necessary to achieve high-speed and high-accuracy operation.

The compromise introduced above, commonly referred as the *speed-power-accuracy trade-off*, has been extensively investigated in classical current mirror structures. We could cite the work of Prof. W. Sansen or Dr. M. Pelgrom, that have conducted and released several studies (Pelgrom, Duinmaijer, and Welbers, 1989) (Pelgrom, Tuinhout, and Vertregt, 1998) (Bastos et al., 1997) (Bosch, Steyaert, and Sansen, 2001) that quantify the implication of process quality during the design of elementary circuit components based on matched structures.

In 2015, P. Kinget, who has collaborated in the past with W. Sansen, publish in the *IEEE Journal of Solid-State Circuits* his research on the origins of the *speed-power-accuracy trade-off* (Kinget, 2005). His main argued conclusion is:

“Speed, accuracy and power consumption of a circuit have a fixed relationship and the minimal power consumption of a circuit is determined by technological constants only

which express the matching quality of the technology. The limit imposed by mismatch on the minimal power consumption for a given speed and accuracy or dynamic range is shown to be several orders of magnitude higher than the limit imposed by noise for modern MOS processes."

To reveal the role played by the technology in the design of dynamic current mirror, P. Kinget proposes a figure-of-merits (1.6) as benchmark. It combines the bandwidth BW, the power consumption PW and the relative accuracy A_{cc} of the current mirror. The result has the dimension of energy and is evaluated for the simple current mirror shown Fig. 1.2. For more details the reader might reffer to the articles (Kinget, 2005) and (Kinget and Steyaert, 1996).

$$FOM_1 = \frac{Power}{Bandwidth \times Accuracy^2} \propto C_{OX} A_{VTH}^2 V_{DD} \left(\frac{g_m}{I_{IN}}\right) \tag{1.6}$$

An optimized current source will score low value for the FOM_1, regardless of which one of the three performances have been prioritized. C_{OX}, A_{VTH} and V_{DD} are technological constants and specific to the process. The only left parameter that can be tuned by designers to optimize the circuit is the (g_m/I_D) ratio of transistors. (g_m/I_D) is minimized by choosing bias point with high V_{GS} (Silveira, Flandre, and Jespers, 1996) (Jespers and Murmann, 2015). But high gate voltages are hardly compatible with low-voltage/low-power operation, V_{GS} for a current mirror will in practice be limited to $V_{DD}/2$, we found again the limitation from the power supply.

Finally, it is in this sense that the technology is claimed to be the dominant factor in the *speed-power-accuracy trade-off*. This is also the reason why achieving high-performances with advanced technological nodes demands more efforts and new design strategies. We will expect from elected strategies the possibility to improve one or more performances with minimal impact on the others.

This approach, with slightly different definitions for the *power*, the *bandwidth* and the *accuracy*, will be reused in Chapter 2 to search for optimum transistor dimensions and in Chapters 3-5 to compare topologies. The reader will find in the next section (1.2) a literature review of recent design techniques for current stages that have successfully addressed the *speed-power-accuracy trade-off*. To contextualize the scientific relevance of the study before going deeper in circuit analysis, the last part of this section is an insight into the applicative background

1.1.2 Potential application fields

▷ Where high-performances current sources are requisite?

Above all, it should be said that the evaluation of a system performance is necessarily linked to its application context. Hence, the notion of *high-performance* may not be consistent and can not be covered in an absolute sense. However, most of analog circuits shares

the same concerns and general characteristics. Today's designs have to exhibit low power consumption, robustness, safety and versatility with minimal silicon area to be competitive.

When dealing with current source architectures, robustness and safety are addressed by controlling systematic and random errors of the generated current. Versatility involves sufficient compliance to be connected to a large range of loads. In dynamic operations, sources often have to exhibit fast but controlled responses to handle complex current waves. Eventually, low power consumption and small silicon area requirements tend to limit the complexity we can add to obtain an effective current source. Then, will be considered as high-performances, structures which offer efficient solutions to overcome those constraints and enhance the performances with minimal negative impact on the overall behaviour.

Listed categories below are not exhaustive, but should illustrate the diversity of applications where current sources are among the most constrained sub-circuits in the architecture.

Low drop-out regulators

A low-dropout or LDO regulator is a DC linear voltage regulator that can regulate the output voltage even when the supply voltage is very close to the output voltage. The advantages of a low dropout voltage regulator over other DC to DC regulators include the absence of switching noise, smaller area as neither large inductors nor transformers are needed, and greater design simplicity, Fig. 1.4.

The disadvantage is that linear DC regulators must dissipate power, and thus heat, across the regulation device in order to regulate the output voltage. On top, LDO regulators in VLSI circuits have to face high peak of power demands, typically followed by sleep phases with minimized power consumption. Fast transient responses and large output currents with minimal quiescent power are typical requirements for the design of Low Drop-Out (LDO) regulators.

For portable applications, authors in (Lam and Ki, 2008) have developed a LDO regulator based on a Transient-Enhanced Super Current Mirror. This solution, thanks to the use of low bias currents and large current copy-ratio, achieves a current efficiency of more than 99% for an output current ranging from 1 mA to 50 mA. The fast response is obtained using a current boosting technique, making the speed from 4 to 20 times higher than the equivalent conventional current mirror.

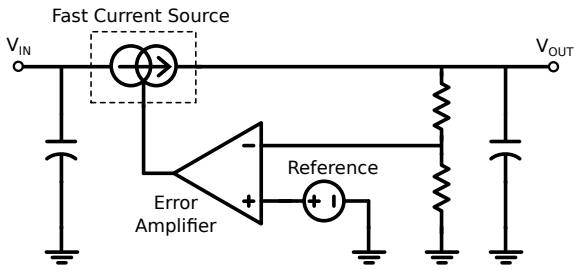


Figure 1.4 – Typical structure for LDO regulators

Other references: (Or and Leung, 2010) (Maity and Patra, 2016)

Signal processing

Analog signal processing is a field which particularly requires extreme speed and accuracy. *Current-mode* techniques have given way to a number of important signal processing circuits found inactive filters, oscillators, current comparators or rectifiers (Biolek et al., 2008).

An other example can be the use of active-input current mirror for greater performances in terms of power speed and compliance in high speed analog-to-digital decoder (ADC) design (Nairn and Salama, 1990) (Moazzeni and Cowan, 2009).

Many recent current-mode signal processing blocks come from modified versions of the standard current conveyor (CC) or current operational amplifier (COA). These two types of components are further discussed in section 1.2

Bio-impedance spectroscopy

The principle of the impedance spectroscopy is to put in relation, chemical or physiological characteristics of the object under study, with its electrical properties and more specifically to its equivalent impedance. A current signal is injected and the voltage developed across the subject is measured to extract the amplitude and phase of the complex impedance.

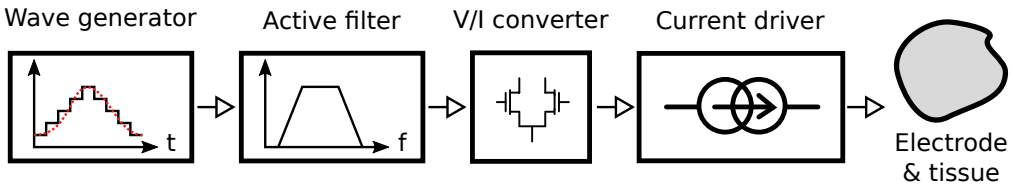


FIGURE 1.5 – Typical current generation scheme for bioimpedance measurements

Typical current generation scheme for bioimpedance measurements, as shown in Fig. 1.5, begins with several blocks of signal conditioning to ends with a current driver capable to handle signals, up to several MHz with amplitude in the order of 100 µA.

Best results reported in the literature have been achieved using high-performances Operational Transconductance Amplifier (OTA) based on matched common mode feedback and enhanced current mirror structures (Constantinou, Bayford, and Demosthenous, 2015). In (Lamlih et al., 2018), the authors propose an enhanced version of the structure in (Constantinou, Bayford, and Demosthenous, 2015). It uses improved current mirror topologies for high-output impedance and a trimmed independent reference voltage to compensate process variations for the output common mode. The current driver is built around a linearized OTA and has a 67 MHz bandwidth with maximum output current of 600 µA peak to peak with a Total Harmonic Distortion (THD) below 0.3% at low frequencies. But the class A operation of their circuits leads unavoidably to poor power efficiency (<50 %).

Biomedical stimulation

Biomedical stimulation techniques induce artificial excitation of muscles and nerves through the use of electrical signals. It is the technology implemented in pacemaker, cochlear implants. The current excitation has shown better results and safety, and today's neural chips use multi-polar electrodes to generate spatially and temporally distributed current waves, with an amplitude of several mA, across target nerves (more details in Chapter 5).

Accuracy and power consumption are the major constraints in neural stimulator design. Precise current signals are mandatory for selective and efficient nerve stimulation with no tissue degeneration for the living subject. High power efficiency are part of the challenge as implantable chip cannot not dissipate much heat and should ensure long-life operation.

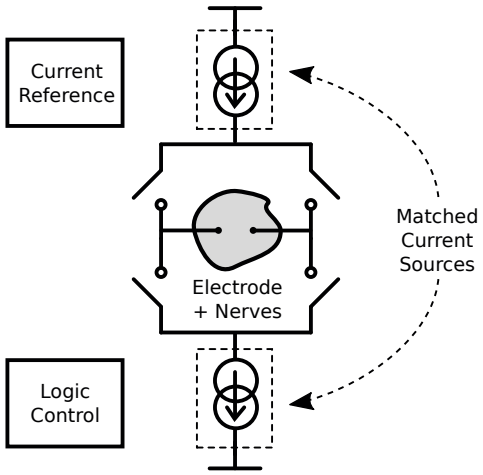


FIGURE 1.6 – Typical structure of output stages in neural stimulation chips

A simplified schematic of typical structure for output stages in neural stimulation chips is depicted in Fig. 1.6. In several designs of electrical stimulators, authors have investigated non-linear or discrete solutions for the implementation of output current sources to optimize *speed-power-accuracy trade-off* while offering high current drive capabilities. In (Greenwald et al., 2017) and (Liu et al., 2014), a current DAC with calibration is deployed to achieve precise balanced stimulation current (≈0.3% of relative error) in a multi-polar application. An other sample-and-hold method based on a closed loop OTA is presented in (Sit and Sarpeshkar, 2007), this solution offers a low quiescent power of 47 µW and a matching error of 0.4% but at the price of a settling time greater than 16 µs.

In the next section we focus on techniques that have been employed in output stage design. Several have been used in the circuits presented above. Advantages and limits of each approach are examined.

1.2 Conventional and recent approaches in current source design

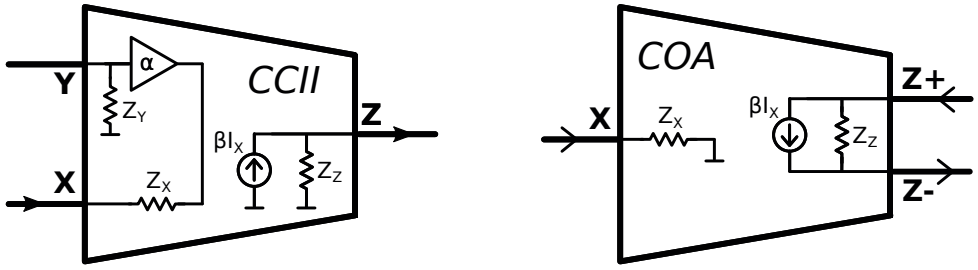
1.2.1 Solutions for fast and accurate output stages in current generation

Output stages generally deal with bigger capacitive or inductive loads and involve higher current density than internal nodes. In some applications, loads (in a general meaning) can also be sensitive to charge errors or bad frequency content of the generated current wave. Hence, consumption, accuracy and linearity are relatively challenging in current output stage. Consequently, as discussed in the previous section (1.1.1) the speed will also be constrained. This section presents a classified set of recent published solutions, with high-driving capabilities, that have achieved good results in relation with the *speed-power-accuracy trade-off*.

Current conveyors and amplifiers

Current conveyor (CCII) and current amplifier (COA), shown respectively in Fig. 1.7a and Fig. 1.7b, are the most popular *current mode* components. They are characterized by a very low input impedance Z_X, a high output impedance Z_Z and an easily adjustable current gain. The standard CCII has the advantage of a regulated input voltage suitable for large current dynamic. The standard COA has a differential output improving its sensitivity to common mode errors (correlated noise, power supply variations, ...).

CCII and COA with high driving capabilities typically offer large gain-bandwidth products at reasonable static power consumption when compared to their equivalent circuits in *voltage-mode*. Even if they may be electrically configurable or programmable this type of component are based on full analog solutions. Most of the time, speed, accuracy and power are optimized at transistor level using classical design techniques such as matched structures, active feedback loop or class AB operation.



(A) CCII (B) COA

FIGURE 1.7 – Equivalent circuits of CCII and COA

A 1.5V CMOS class AB current conveyor (CCII+) with high input/output ranges is presented in (Mita, Palumbo, and Pennisi, 2003). The solution offers a quasi rail-to-rail input and output ranges, as well as a high-drive current capability obtained together with a good power conversion efficiency. The circuit also exploits a negative feedback loop in the

input section, which improves both the voltage transfer accuracy and linearity, reducing the input resistance without excessively sacrificing bandwidth.

G. Palmisano et al. (Palmisano, Palumbo, and Pennisi, 2000) present two types of current amplifiers dedicated to high-drive output stages which exhibit settling times of 260 ns and 165 ns along with good linearity. An improved and programmable solution operating in class A-B is proposed in (Esparza-Alfaro, Pennisi, et al., 2014). Authors have used a feedback realized with transistors as resistors to isolate gain control from bandwidth performances. It shows more versatility and a lower quiescent power of 280.5 µW than structure in (Palmisano, Palumbo, and Pennisi, 2000).

Current DAC and calibration techniques

Current digital-to-analog converters (DAC) are built using weighted current cell array and digitally controlled switches to generate complex current waves. Timing and amplitude are set by controlling the switching period and the digital code applied. However, variations between each current cell characteristics will introduce current errors on the output current that degrade the conversion. Calibration techniques combines error measurement and correction mechanisms. Calibration methods ensure the static linearity and accuracy by adjusting the current values of current sources. With calibration, the sizes needed for the current sources can be greatly reduced, so this technique has the advantage of a smaller area and potentially better dynamic performances.

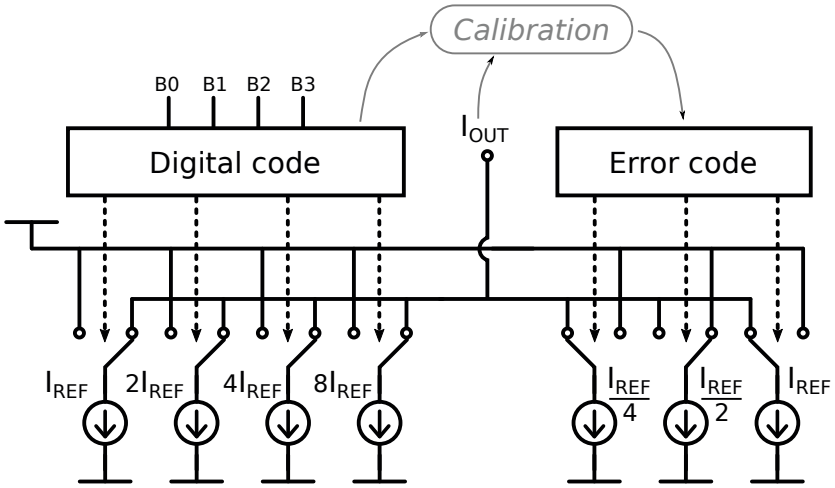


FIGURE 1.8 – current DAC with an amplitude error correction after calibration

An example on a simple current DAC with amplitude error correction is shown Fig. 1.8. In this example a calibration circuit (not represented) senses the error on the output I_{OUT} and compares it to the reference I_{REF} to determine the error code to apply to finally subtract the difference. Various solutions with different level of complexity exist to quantify the error. It ranges from the use of simple current comparators to more advanced circuits involving, for instance, I/Q demodulation and high-resolution ADC. Recent sensing techniques allows sensitivity up to 10 nA (McDonnell et al., 2017).

Once the amount of error is known, there exist also several techniques to compensate the mismatch error. Instead of acting on the total output current by injecting or removing additional current, some work have proposed solution that dynamically adjust the switching sequence of current cells after fabrication (T. Chen and Gielen, 2007) (Zeng and D. Chen, 2010). Called *SSPA* (Switching-Sequence Post-Adjustment), it basically consists in rearrangement of the elementary current cells activated, in order to average their dispersion in characteristics. This technique is often privileged in very low-power application as it is claimed to reduce analog and digital resources needed for calibration.

The DAC architecture proposed in (T. Chen and Gielen, 2007) achieves same order of linearity than the equivalent DAC realized with large device but with only 10% of the area required by the last one. Their DAC generates currents up to 16 mA with a maximum frequency of 2 MHz and the power consumed under 1.8 V is 210 mW. A current comparator is needed to implement the SSPA-based calibration. Expected accuracy of the current comparator generally requires an additional offset cancellation circuit.

Eventually, besides full analog solution like class AB operation or active feedback, digital calibration and compensation techniques well succeed in cancellation of variability effect and offer a new degree of freedom to optmize the *speed-power-accuracy trade-off*. It make this solution attractive for high-precision application. However compensation techniques require additional digital resources. A calibration phases is necessary during which the normal system operation is interrupted and the offsets of the building blocks are sampled and dynamically stored in an analog memory circuit. We can that add the more the number of switched elements, the more the system is sensitive to charge injection errors. In (Kinget and Steyaert, 1996), the author discuss these techniques and formulate the following ascertainment:

"Maximum time between calibration phases is determined by the quality of the analog memory circuits and limits the maximal duration of a continuous operation phase. In sampled data systems, the calibration can be done in one of the clock phases but clocked circuits intrinsically have a much lower operation speed as continuous time circuits."

This observation, even though it is general, suggests that there may be an advantage to study solutions, not based on digital resources, that are capable to deals with large but precisely-matched devices with low variability.

1.2.2 Solutions for enhanced current mirror

As discussed Section 1.1.1, variability at transistor-level is the origin of limitations encountered during the design of high-performances current source. Previously in this chapter, we have seen that dealing with accuracy errors at system level, to relax constraints on speed and power consumption, may not be the only alternative.

Thus, here, we continue to decrease the scale to take a closer look at the CMOS current mirror itself, basic building block and common part of all previously mentioned system. Benefits of design techniques that improve the performance of low-voltage CMOS current mirrors, will at the end be granted to the overall performances of the full circuit.

The basic current mirror, which consists in a simple alignment of transistors sharing the same gate-source connection, is known for almost the beginning of integrated systems. From this time until nowadays, there have been research groups investigating on this elementary building block with the intention to improve their designs by tackling issues at the bottom. From the IEEE database we gathered a hundred of papers specifically dedicated to the CMOS current mirror over the past 40 years. We observe in Fig. 1.9 that this topic has been continuously studied despite the changes in design trends or the advances in CMOS technology.

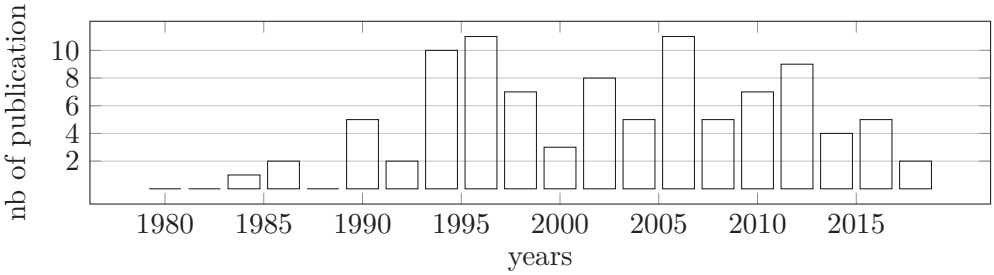


FIGURE 1.9 – Publications on CMOS current mirrors in IEEE international conferences or journals across the years.

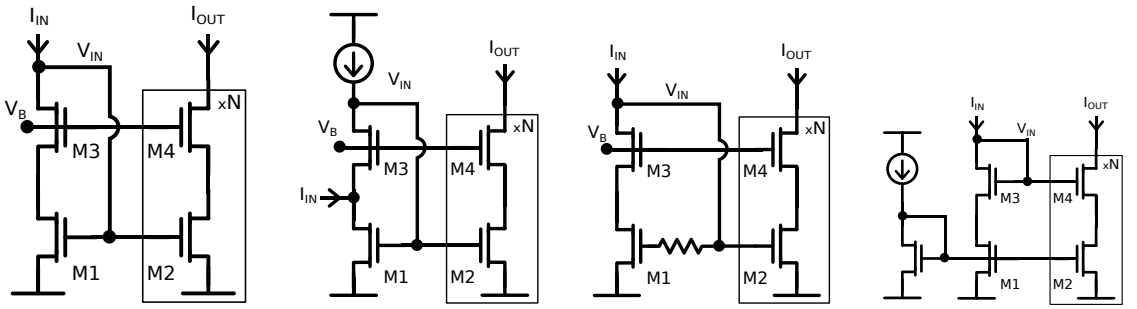
Important factors influencing the performance of a current mirror are: (i) Accuracy, defined as the precision of the current copy from input to output nodes. (ii) Bandwidth or settling time, accounting for the overall speed. (iii) Power efficiency, defined as the ratio between current actually delivered to the load and current consumption. (iv) Input/output compliance voltage, given as minimum voltage required at input/output node for proper operation. (v) Input resistance. (vi) Output resistance. For the next circuit analysis we will focus on structures that improve the three first performances mentioned (i, ii, iii) and that offer the possibility to multiply output branches for amplification factors higher than one.

In 2016, B. Aggarwal *et al.* have released an extensive review (Aggarwal, M. Gupta, and A. K. Gupta, 2016) that compares and classifies existing enhanced current mirror topologies. Results of their comparative study have been validated on a CMOS 0.18 µm technology. This technology is similar to the available technologies we had for the fabrication of our circuits (Chapters 2-5). Therefore, advantages and drawbacks of enhanced current mirrors detailed below will be partly drawn from conclusions stated by B. Aggarwal *et al.*. A qualitative comparison of structures shown in Fig. 1.10 is given in Table. 1.2 and 1.3 (pages 26,27).

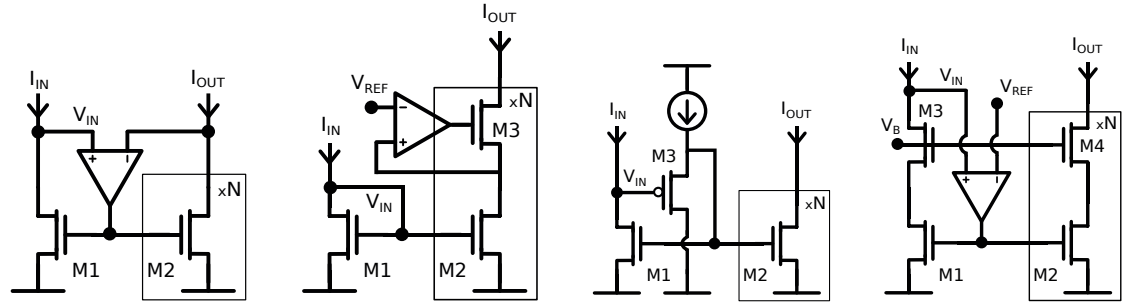
High-swing cascode CM (Fig. 1.10a)

The cascode technique is used to increase the output impedance of a current mirror. With high output impedance, the output current value is less affected by output voltage variation caused by the load. But cascoding devices on the signals path increases the voltage headroom required to ensure their operation in saturation region.

The low-voltage high-swing cascode (Swanson, 1986) offers the same output impedance as the simple cascode ($g_m r_{o2} r_{o4}$) but reduces its voltage compliance by V_{TH}. With M1=M2



(A) High-swing cascode CM (B) Flipped-voltage follower CM (C) Resistor peaking cascode CM (D) Triode region CM



(E) Bootstraped CM (F) Output-regulated cascode CM (G) Level-shifted CM (H) Active-input cascode CM

FIGURE 1.10 – High-performance current mirrors in literature

and M2=M4 this structure ensure a precise current current copy as $V_{DS1} = V_{DS2}$. Speed is identical to the speed of the simple current mirror. This is the privileged implementation for simple mirrors in low-voltage applications.

Flipped-voltage follower CM (Fig. 1.10b)

The Flipped-voltage follower (Carvajal et al., 2005) (Koliopoulos and Psychalinos, 2007) has the same output performance as the high-swing cascode, but it offers low input resistance, hence lower input voltage requirements (V_{EFF}), due to negative feedback provided by M3. The gate voltage of M1 is regulated to ensure that the input voltage (V_{DS1}) remains constant.

Resistor peaking cascode CM (Fig. 1.10c)

To increase the bandwidth of simple and high-swing current mirror, authors in (Voo and Toumazou, 1995) have presented a resistance compensation technique. With a resistor R connected between input gates of the copying pair, a controllable zero is introduced in the current transfer function (1.7).

$$\frac{i_{OUT}}{i_{IN}}(s) = \frac{g_{m2}(1 + Rg_{m2}C_{GS1}s)}{g_{m1} + (C_{GS1} + C_{GS2})s + RC_{GS1}C_{GS2}s^2} \tag{1.7}$$

They have shown that with the right value of R this zero can compensate the dominant pole and consequently increases the speed of the current mirror. However, speed can not be increased by a factor greater than two, beyond the zero induces peaking in the frequency response, traduced in the time domain by oscillations and overshoot for the output current.

Triode region CM (Fig. 1.10d)

A triode-region current mirror is proposed in (Mulder et al., 1996). The circuit resembles a simple current mirror, comprising M3 and M4, transistors M1 and M2 act as active resistors, biased at a constant gate voltage for source degeneration. The degeneration resistors increase the output resistance of the current mirror. Thanks to the use of transistors operating in the triode regime in weak or moderate inversion, the input and output compliance is improved compared to the classical cascode configuration.

Bootstraped CM (Fig. 1.10e)

In the boostrapped configuration(You et al., 1997), M2 mirrors the current injected in M1 and an error amplifier regulates drain voltages of both devices by tuning the gate voltage. This configuration forces a similar change at input node that occurs at output node with the help of one positive and one negative feedback loops. This helps reducing errors due to modulation channel and increases the output impedance. However, variations of the output are also reported to input through the amplifier. An other limit is that the same gain is applied for positive and negative feedback which may lead to unstable behaviour under certain conditions. This circuit has the advantage of very low-voltage operation.

Output-regulated cascode CM (Fig. 1.10f)

The output regulated cascode techniques (Sackinger and Guggenbuhl, 1990) has a very high output impedance and the advantage of a regulated drain voltage for the output transistors (M2) mirroring the current. The amplifier imposes the drain voltage using active feedback through the cascode device (M3). Same techniques can be applied on the input device (M1) to match V_{DS} and ensure good copy accuracy. The positive input of the amplifier can also be connected to the input drain for better equality between V_{DS} of M1 and M2. But at the price of large capacitance on the input node and thus potential significant speed reduction.

Level-shifted CM (Fig. 1.10g)

The level-shifted current mirror (Ramirez-Angulo, 1994), which can also be combined with output cascode techniques, uses an active elements to reduce input impedance and enhance the input voltage requirement. The added transistor M3 acts as a source follower (gain close to 1) between input drain and gates. It allows, in dynamic operation to propagate input voltage changes on gate voltage as in the simple diode-connected current mirror, but

	High-swing casc.	Flipped-voltage follower	Resistor peaking casc.	Triode region
V_{IN}	$V_{EFF} + V_{th}$	V_{EFF}	$V_{EFF} + V_{th}$	$V_{eff\text{casc}} + V_{th}$
V_{OUT} min.	$2V_{EFF}$	$2V_{EFF}$	$2V_{EFF}$	V_{EFF}
Input res.	$\frac{1}{g_m}$	$\frac{1}{g_{m\text{casc}}}$	$\frac{1}{g_{m\text{casc}}}$	$< \frac{1}{g_{m\text{casc}}}$
Output res.	$\frac{g_{m\text{casc}} r_o^2}{N}$	$\frac{g_{m\text{casc}} r_o^2}{N}$	$\frac{g_{m\text{casc}} r_o^2}{N}$	$\frac{g_{m\text{casc}} r_{o\text{triode}}}{N}$
Current dynamic	$++++$	$+$	$++++$	$++$ (till I_{DC})
Bandwidth	$\frac{g_m}{(N+1)C_{gs}}$	$< \frac{g_m}{(N+1)C_{gs}}$	$< \frac{2g_m}{(N+1)C_{gs}}$	$\frac{g_{m\text{casc}}}{(N+1)C_{gs}}$
Copy accuracy	$++++$	$+++$	$++++$	$+++$ (till I_{DC})
Power efficiency	$\frac{N}{N+1}$	$\frac{N}{N+1}$	$\frac{N}{N+1}$	$\frac{N}{N+1+\frac{I_{DC}}{I_{IN}}}$

Power efficiency(%)$= 100 \times \frac{\text{Power delivered to the load}}{\text{Total power dissipated}}$.

TABLE 1.2 – Comparison of enhanced current mirror in literature

in static operation the minimum drain voltage to ensure operation in saturation region is reduced by V_{TH}.

This level shifting technique can reduce the input and output compliance voltages of simple and cascode mirrors but may degrades the bandwidth and increases the power consumption. Gate to source capacitance of the copying pair loads the source follower, hence the overall speed depends on how fast this elements can charge the C_{GS} which strongly depends on bias current of M3.

Active-input cascode CM (Fig. 1.10h)

The active-input current mirror (Serrano and Linares-Barranco, 1994) maintains a constant voltage equal to V_{REF} at the input terminal independently of the input current, with the help of an amplifier. This leads to significant reduction in input resistance and minimizes the loading effect of previous stage.

Values of V_{REF} depends on the target current dynamic and should be sufficiently high to ensure that transistors mirroring the current are saturated. Gain and DC bias of the amplifier also impact the speed at small (bandwidth) and large signal (slew-rate) operation. The mirror accuracy is not affected by the active element on input terminal. In addition to the improvement of input behaviour, this solution offers potential speed enhancement and good output characteristics when combined with cascode techniques.

Among the solutions discussed before, this is the only one that permits to tune speed of the copying pair with minimal impact on accuracy. Active-input techniques has been the starting point for our work on enhanced current mirror topologies and will be further discussed in Chapters 3 and 4.

	Boot-straped	Output-regulated casc.	Level-shifted	Active-input casc.
V_{IN}	V_{EFF}	$V_{EFF} + V_{th}$	V_{EFF}	$\approx V_{REF}$
V_{OUT} min.	V_{EFF}	$\approx V_{REF}$	V_{EFF}	$2V_{EFF}$
Input res.	$\frac{1}{Ag_m}$	$\frac{1}{g_m}$	$\frac{1}{A_{\text{follower}}g_m}$	$\frac{1}{Ag_m}$
Output res.	$\frac{1}{NAg_m}$	$A\frac{g_{m\text{casc}}r_o^2}{N}$	$\frac{r_o}{N}$	$\frac{g_{m\text{casc}}r_o^2}{N}$
Current dynamic	+++++	+++++	+++++	+++
Band-width	$> \frac{g_m}{(N+1)C_{gs}}$	$\frac{g_m}{(N+1)C_{gs}}$	$< \frac{g_m}{(N+1)C_{gs}}$	$> \frac{g_m}{(N+1)C_{gs}}$
Copy accuracy	+++++ (till triode)	+++++	++	++++
Power efficiency	$\frac{N}{N+1+\frac{I_{OPAMP}}{I_{IN}}}$	$\frac{N}{N+1+\frac{I_{OPAMP}}{I_{IN}}}$	$\frac{N}{N+1+\frac{I_{DC}}{I_{IN}}}$	$\frac{N}{N+1+\frac{I_{OPAMP}}{I_{IN}}}$

Table 1.3 – Comparison of enhanced current mirror in literature (continued)

Combined techniques for higher performances

Various architectures proposed in literature have combined several of the techniques discussed to obtain very high performance for low voltage current mirrors. Tables B.1 and B.2 in appendix B compares performances of circuits presented below.

In (Esparza-Alfaro, Lopez-Martin, et al., 2012) (Pennisi, 2002) low-power CMOS class AB current mirrors are presented. Their circuits combines very high linearity, very low input and high output resistance, high current handling capability at low standby power consumption thank to the biasing in class AB.

In (Serrano, Linares-Barranco, and Andreou, 1999), authors have proposed an enhanced version of the active-input topology by controlling the source voltage instead of the gate voltage of the copying pair. They achieve higher current dynamic and better stability than with the conventional structure.

In (Ramirez-Angulo, Carvajal, and Torralba, 2004), they reuse the principle of the level-shifted current mirror but with an unbalanced differential pair in place of the simple level-shifter for better current dynamic. They have conjointly implemented an output regulated cascode for better output resistance and compliance.

Resistor based current mirrors have not been presented so far but in (Safari and Minaei, 2016) they show that this type combined with cascode techniques can offer wide input and output swing along with good linearity. The main advantage of this solution is its simplicity but it suffers from poor accuracy and die area, required to match resistors, can significantly increase.

Authors in (Aggarwal, M. Gupta, and A. K. Gupta, 2013) propose a variation of the conventional high-swing cascode topology with bulk-driven transistors instead of the traditional gate-driven implementation. They show that controlling devices operation by adjusting the bulk voltage leads to lower voltage requirement and higher bandwidth than the equivalent gate-driven high-swing cascode. However acting on bulk voltage requires isolated (floating) well for the copying pair which adds complexity in layout, increases the silicon area and may introduce coupling through the substrate.

A sub-threshold current mirror, whose performance shows low sensitivity to PVT variations is presented in (Amaya, Espinosa, and Villamizar, 2014). The robustness of the performance was achieved by the use of multiple negative feedback loops implemented with simple structures as one-transistor error amplifier to minimize the impact of process variation. Their solution has the advantage of high output compliance combined with high output impedance.

A low-voltage version of the well-known Wilson current mirrors is proposed in (Minch, 2007). The structure features a cascode-type output impedance and a wide output-voltage swing while it benefits of the good accuracy of the Wilson current mirror.

Dedicated to bias differential pairs, authors in (Ramirez-Angulo, Carvajal, and Lopez-Martin, 2007) have developed a compact implementation of a high-impedance single transistor tail current source. It is based on replica bias feedback arranged in way similar to the boostrapped mirror presented before.

A modified regulated cascode structure operating below 1 V supply that incorporate a push-pull inverting amplifier and having a low output compliance voltage is proposed in(Vajpayee et al., 2010). On the input they have used the level-shifted mirror techniques with adaptive biasing for very low input compliance. Because of drain asymmetry of the copying pair this structure does not offer accurate current copy. However size of devices can be reduced and thus dynamic behaviour improved as systematic errors will dominate random errors.

In (Torralba et al., 2003) authors propose a simple output stage for high-performance current mirrors. The stage is a modified version of the high-swing regulated cascode circuit, which achieves a very high output impedance and accurate current copy when combined with the flipped-voltage follower technique on the input. The principle relies on the use of a transconductance amplifier which senses output node variations and provides the corresponding current on the output branch to compensate v_{DS} modulation effect. The speed is similar to the speed of the flipped voltage follower current mirror with identical devices.

The current mirror proposed in (Zeki and Kuntman, 2000) makes use of the self-cascode structure and partial positive-feedback to reduce the input and output voltage restrictions. All devices are aimed to be kept in saturation to achieve a high output impedance. Advantages of this structures are the self-biasing solution that require minimum additional device and the drain equality for accurate copy ensured by an simple error amplifier.

1.2.3 Synthesized literature review

This section is intended to summarize performances of circuits discussed before. To our knowledge, these interesting and competitive architectures have achieved the best specifications in their respective application field. Thus, the limit in performances they have fixed constitutes the target specification to outperform for future proposed architectures.

In appendix A, tables A.1, A.2 and A.3 compare specifications of circuits and systems presented in section 1.1.2 and 1.2.1 only. Additional references are given in Chapter 5 for a more exhaustive comparison with our proposed architectures.

In appendix B, tables B.1 and B.2 compares specification of current mirror topologies presented in section 1.2.2. Current mirror performances will be more largely discussed in Chapters 2 to 4.

To ease the comparison between published and later proposed work, we recommend the use of the figure-of-merits defined in Table. 1.4. Those metrics are inspired by the figure-of-merit introduced in (Kinget, 2005) and presented section 1.1.1. We used a set of 10 metrics because applications can differ and each formulates their needs with different specifications.

$\text{FOM A} = \dfrac{\text{power eff}}{\text{resp. time} \times \text{dc error}}$	$\text{FOM D} = \dfrac{\text{power eff}}{\text{resp. time} \times \text{dc error}^2}$
$\text{FOM B} = \dfrac{\text{power eff} \times \text{bandwidth}}{\text{dc error}}$	$\text{FOM E} = \dfrac{\text{power eff} \times \text{bandwidth}}{\text{dc error}^2}$
$\text{FOM C} = \dfrac{\text{power eff} \times \text{bandwidth}}{\text{thd}}$	$\text{FOM F} = \dfrac{\text{power eff} \times \text{bandwidth}}{\text{thd}^2}$
$\text{FOM G} = \dfrac{\text{power eff}}{\text{resp. time}}$	$\text{FOM H} = \text{power eff} \times \text{bandwidth}$
$\text{FOM I} = \text{resp. time} \times \text{dc error}$	$\text{FOM J} = \dfrac{\text{bandwidth}}{\text{dc error}}$

Table 1.4 – Definition of various figure-of-merits used for circuits comparison

For the three first metrics, FOM A, B and C, a high score indicates that the topology offers high-performances and has implemented interesting design techniques to relax the *speed-power-accuracy trade-off*. In other terms, high scores demonstrate an efficient use of the total power dedicated to a block, or a circuit, to achieve precise and/or fast current generation. Metrics FOM D, E and F are similar to the three first, but the terms related to the accuracy (static error or THD) is squared. For the simple current mirror their values are fixed by technological constants and relate to the process quality. The last metrics put in relation the speed with power efficiency (FOM G, H) or accuracy (FOM I, J). This information is less relevant than the information given by the 6 first metrics but it allows to identify which performance has been privileged.

Table 1.5 gives the results of the 10 metrics introduced for each advanced current mirrors reported in Tables B.1 and B.2 in Appendix B. Values have been normalized. A score of 100 represents the best performance. Absence of a value means that one of the specifications involved in the calculation has not been reported.

1.3 Conclusion

We know that both static and dynamic current mirrors are found in the large majority of analog and mixed signal chips. They generally serve as basic building blocks to realize more advanced functions. In several applications, such as DC/DC voltage regulators, signal processing circuits or biomedical chips, we have seen that the design of current sources is subject to strong constraints and often dominates budgets and resources allocated to the whole system. This first chapter has started with an introduction to the origins of the constraints encountered in current source design.

Then, we have shown in section 1.2.1, several interesting approaches that rely on digital resources and calibration/auto-correction mechanisms to achieve high-performance current sources. But the additional circuitry they require, which often involves clocks, flip-flops, integrated memories and large interconnect, consumes power, die area and increases the system complexity. And this may become a limiting factor for certain applications. In section 1.2.2, we have seen that an other approach consists in tackling the issues at the bottom, by looking for enhanced topologies of the elementary current source, namely the current mirror. Most popular enhanced current mirror structures have been presented and recent publications of more advanced current mirrors have been examined and compared.

However, from the literature review comes a first ascertainment: Solutions that specifically address the *speed-power-accuracy trade-off* of a current mirror is a slightly treated topic. And this, despite the fact that this trade-off has been frequently studied and is unavoidably encountered in dynamic CMOS current mirror design. Outperforming the existing limits during the speed, power and accuracy optimisation in CMOS current mirror is the major objective of the work presented in the following chapters.

In order to apprehend and then act on these limits, the development of theoretical tools is necessary. The derivation of an analytic expression for the *speed-power-accuracy trade-off* is a first step allowing to target the main parameters which influence the relation between the speed, the accuracy and the power efficiency. This topic is treated in the next chapter.

Metric	Weight	Koliopoulos 2007 a	Esparza 2012 b	Pennisi 2002 c	Ramirez 2004 d	Safari 2016 e	Aggarwal 2016 f	Amaya 2014 g	Vajpayee 2010 h	Torralba 2003 i	Zeki 2000 j
FOM A	+++			100					30.8		
FOM B	+++	29.4		100		58.4	78.6		25		27.1
FOM C	+++	10.8	100	7.7		3.4				67.6	
FOM D	++			100					2.5		
FOM E	++	4.9		100		77.9	39.3		2		21.7
FOM F	++	1.1	100	1		0.4				67.6	
FOM G	+			22.6	17.3			0.5	86.8	100	
FOM H	+	56.3	52.2	32	25	14	50.3		100	35.3	10.8
FOM I	+			100					28		
FOM J	+	22		100		76.2	47.1		22.7		16.6

TABLE 1.5 – Score of published enhanced current mirror topologies for the 10 metrics used. Values in table are normalized and mapped between 0 and 100.

Chapter 2

Classical current mirror modelling and design

In this Chapter the reader will find more details on approaches, analytical tools and theoretical assumptions we have used to model and optimize our current mirror designs.

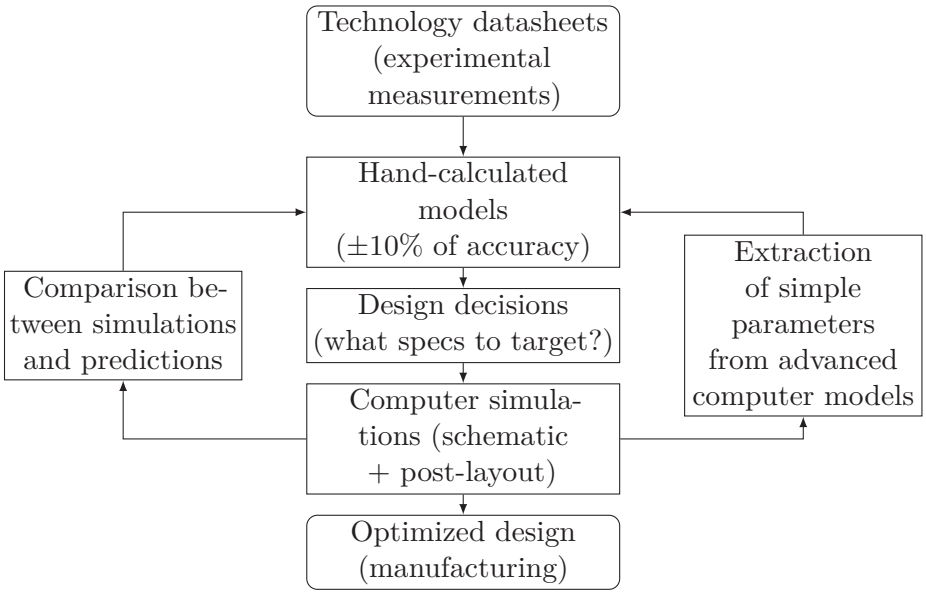


FIGURE 2.1 – Typical analog design flow.

There exist standardized models with various levels of complexity to emulate transistor behaviour. For instance, EKV and BSIM4 models are implemented in electrical simulators such as SPICE or Spectre®. Benefits of these models are precise estimations of output impedance, short channel effect, carrier velocity saturation ... But they can not be manipulated for hand calculation. Much simpler models are used to analyse and interpret circuits behavior before moving within the computer-aided design software for accurate simulations. A typical analog design flow is outlined in Fig. 2.1.

2.1 General assumptions on MOS device models

This short section details the considered large and small signal transistor representations used to build the analytical models.

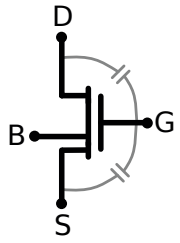


FIGURE 2.2 – Terminal names and transistor schematic

2.1.1 Large-signal modelling

In published advanced current mirror designs, MOS devices have been implemented in various regimes, ranging from weak to strong inversion but also from triode to saturated region. The following equations recall the large-signal MOS current laws in each operating region. We define the drive voltage $V_{EFF} = V_{GS} - V_{TH}$, and physical parameters $K = \mu C_{OX}$ and $\beta = K(W/L)$.

Saturated device in strong inversion ($V_{GS} > V_{TH}$ and $V_{DS} > V_{EFF}$):

$$I_D = \frac{K}{2}\frac{W}{L}(V_{EFF})^2(1 + \lambda V_{DS}) \tag{2.1}$$

Triode region device in strong inversion ($V_{GS} > V_{TH}$ and $V_{DS} < V_{EFF}$):

$$I_D = K\frac{W}{L}(V_{EFF} - \frac{V_{DS}}{2})V_{DS} \tag{2.2}$$

Saturated device in weak inversion ($V_{GS} < V_{TH}$):

$$I_D = K\frac{W}{L}(\eta - 1)\left(\frac{kT}{q}\right)^2 \exp\left(\frac{V_{GS}}{\eta kT/q}\right)\left(1 - \exp\left(\frac{-V_{DS}}{kT/q}\right)\right) \qquad \eta \approx 1.25 \tag{2.3}$$

2.1.2 Small-signal modelling

In small-signal, the drain current is approximated by $i_{ds} \approx g_m v_{GS} + g_{mb} v_{BS} + g_{ds} v_{DS}$, with parameters derived from large signal equations as in (2.4). Expressions of these main small signal parameters in each regime of operation are summarized in Table. 2.1. A typical small-signal schematic of a MOS device used for analytical study is given Fig. 2.3. This small-signal model is valid only for low-frequency or mid-frequency applicative contexts.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \qquad g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} \qquad g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} \qquad c_{GS} = \frac{\partial Q_G}{\partial V_{GS}} \tag{2.4}$$

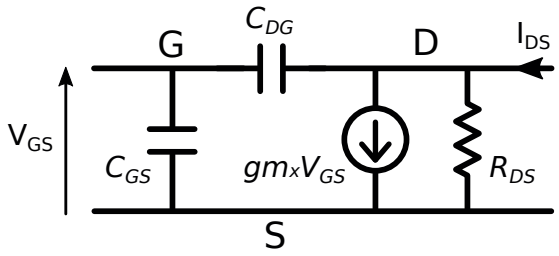


FIGURE 2.3 – Typical small signal representation

	saturated device in strong inversion	triode region device in strong inversion	saturated device in weak inversion
g_m	$\frac{2I_D}{V_{EFF}} \approx K\frac{W}{L}(V_{EFF})$	$K\frac{W}{L}V_{DS}$	$\frac{I_D}{\eta\frac{kT}{q}}$
g_{ds}	λI_D	$K\frac{W}{L}(V_{EFF}-V_{DS})$	$\frac{\eta g_m}{\exp\left(\frac{V_{DS}}{kT/q}\right)-1}$
C_{GS}	$\frac{2}{3}C_{OX}WL+C_{OV}$	$\frac{1}{2}C_{OX}WL+C_{OV}$	-
C_{GD}	C_{OV}	$\frac{1}{2}C_{OX}WL+C_{OV}$	-

TABLE 2.1 – small-signal parameters in hand-calculation MOSFET model

2.2 Generic model with admittance matrix

2.2.1 Definitions

For elementary structures, when building analytical models it is fair to represent a system as a generic two-port circuit. The system is treated as a *black box* and its behaviour is expressed with linear relations between currents and voltages at each port. This type of representation is used to describe the electrical behaviour of linear circuits. They are also used to describe the small-signal linearized response of a non-linear system. The admittance matrix (Y-matrix) representation, among others, is a method to formulate the relations between input and output ports. The Y-matrix reflects how the circuit will allow a current to flow.

Relations between currents and voltages at each ports are in the form of $I = Y.V$. The term V represents the voltage at each port, the term Y is the admittance matrix that emulates the circuit behaviour. Equation (2.5) gives the expressions for a two-port circuits. The small-signal circuit that corresponds to the matrix representation is given in Fig. 2.4.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} . \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} y_{11}V_1 + y_{12}V_2 \\ y_{21}V_1 + y_{22}V_2 \end{bmatrix} \tag{2.5}$$

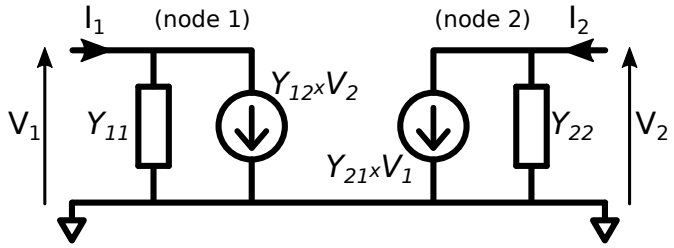


FIGURE 2.4 – Admittance parameters in the small signal schematic

We assume that admittance parameters y_{ij} are complex parameters. The term g_{ij} represents the real part as a conductance, the imaginary part is represented by $C_{ij}s$ traducing capacitive effects. Reason for this assumption comes from our focus on CMOS analog design, where MOS devices are considered as active capacitive devices in many applications. For the next theoretical analysis based on Y-matrix representation we will take the definition in (2.6) for the admittance parameters. The term s is the Laplace complex variable. Minus signs found in the equations of y_{12} and y_{21} are here to manipulate positive capacitance value for parameters C_{ij} with respect to the convention on current and voltage directions imposed in Fig. 2.4.

$$Y = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} + C_{11}s & g_{12} - C_{12}s \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} \tag{2.6}$$

This general representation will be used to model transistor and current mirror behaviours during the exploration of active-feedback solutions treated in the next chapters. Depending on the elementary circuit we want to model, or more specifically on the aimed accuracy of the model, different assumptions can be made on the values of admittance parameters y_{ij}. Assumptions will be given and justified case-by-case for the next theoretical analysis found in this manuscript.

2.2.2 Correspondence with classical small-signal model of MOS devices

The following part proposes an illustration on how admittance parameters corresponds to more classical/specific parameters of a circuit. This example is presented for the single MOS device, with the hypothesis introduced section 2.1. Correspondences below are based on general knowledge and identification with the typical small signal representation in Fig. 2.3. Gate terminal of the device is defined as the node 1, drain terminal of the device is the node 2, the source terminal is taken as the common reference for other nodes (AC ground). This naming convention will be adopted for the rest of the manuscript. In these conditions, admittance parameters have the following meaning:

- y_{11} defines the amount of current that flows into the node 1 (gate) due to voltage variation at this same node. For a single MOS transistor, this parameters is purely capacitive and represents the gate-to-source capacitance. It is assumed that there is no resistive path going from gate to source terminal. Hence, we have $y_{11} = g_{11} + C_{11}s$ with $g_{11} = 0$ and $C_{11} = C_{GS}$.

- y_{12} defines the amount of current that flows into the node 1 (gate) due to voltage variation of node 2 (drain). Again, that parameter is purely capacitive. In MOS devices, there exists no active or resistive path going from drain to gate. We have $y_{12} = g_{12} - C_{12}s$ where $g_{12} = 0$ and C_{12} represents the contribution of the drain-to-gate capacitance C_{GD} when the drain voltage is varying and the gate voltage stays constant.
- y_{21} defines the amount of current that flows into the node 2 (drain) due to voltage variation of node 1 (gate). For MOS devices, g_{21} represents the transconductance factor. The frequency dependant term $C_{21}s$ model the capacitive path that exist from gate to drain terminal. Hence, we have $y_{21} = g_{21} - C_{21}s$ with $g_{21} = g_m$ and C_{21} represents the contribution of the drain-to-gate capacitance C_{GD} when the gate voltage is varying at a constant drain voltage.
- y_{22} defines the amount of current that flows into the node 2 (drain) due to voltage variation at this same node. The conductance part g_{22} represents the resistive path that exists between drain and source terminals. Drain-to-source capacitances have been neglected. We have $y_{22} = g_{22} + C_{22}s$ with $g_{22} = g_{ds}$ and $C_{22} = 0$

Finally, the admittance matrix for a single MOS device expresses as:

$$Y_{MOS} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} C_{GS}s & -C_{DG}s \\ g_m - C_{GD}s & g_{ds} \end{bmatrix} \tag{2.7}$$

These last statements concerns a single MOS devices. When modelling current mirrors, the node 1 will still correspond to the gate terminal, common to all devices, the node 2 will generally represent the mirror input terminal which can be a more complex combination of components than the drain of a single transistor.

2.2.3 Motivations

When building analytical model for solution exploration, such representation has multiple advantages. First it brings some homogeneity in the formulation of mathematical expressions that describe the behaviour of the different tested solutions, and thus eases the result interpretations and comparisons.

The other advantage is that admittance parameters can be directly extracted from simulation to improve the accuracy of model predictions. For example, during a preliminary design phase where only some part of the circuits are already defined, measuring admittance parameters by simulation helps to start taking into account side effects that are not modelled by typical hand-calculation parameters. The measure of Y-parameters also offers the possibility to establish their large-signal dependencies and finally study the system for different operating points with the same equations.

An other benefit of using generic representations is that small changes in the system structure, for instance switching from simple to cascode configuration for a current mirror or changing the process, do not negate the validity of the model build. Only admittance parameters will change, their relations can stay identical.

A last advantage that worth citing is that, formulating the system behaviour with its admittance representation enables the direct integration in the Y-matrix of parasitics or alternative signal paths brought by the load, the reference source or any additional circuitry . Again the idea behind is to have a model that is valid for many configuration and which can be tuned according to either, the desired prediction accuracy, the knowledge of the system environment or the various assumptions that can be made for the topology under study.

The last section of this chapter introduces the design approach adopted for optimized current mirrors with special care for speed power and accuracy. The Y-matrix representation will be used to analyse the dynamic behaviour. Assumptions on MOS devices discussed section 2.1 will be used to move from system model to design choices.

2.3 Current mirror design approach

From conclusions drawn in Chapter 1, we choose to adopt the approach depicted in Fig. 2.5 to design high-performance (fast, precise and low-power) current mirrors. The strategy is to first address *static* performances such as mismatch, voltage compliance or power consumption with optimized size and bias for the current mirroring devices. Then we apply enhancement techniques, some are described in section 1.2.2, for *dynamic* performances improvement, such as input/output impedance or general speed.

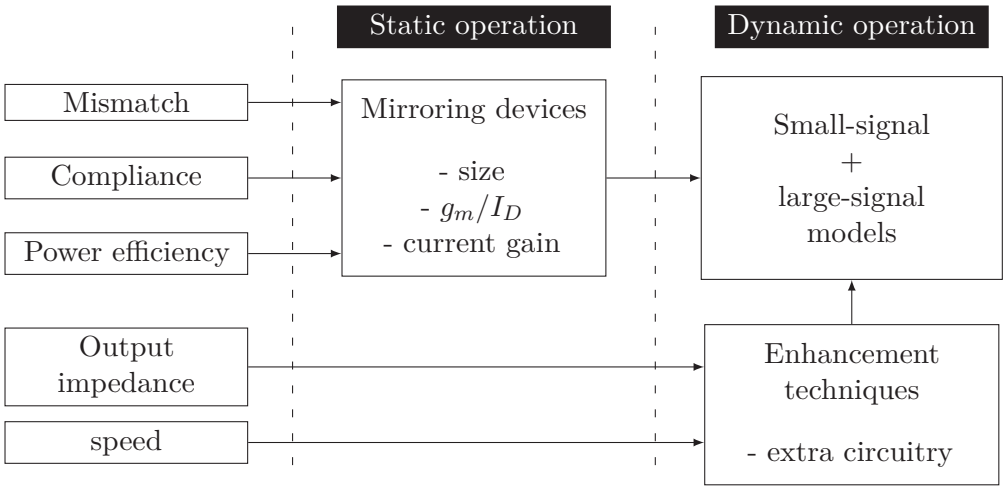
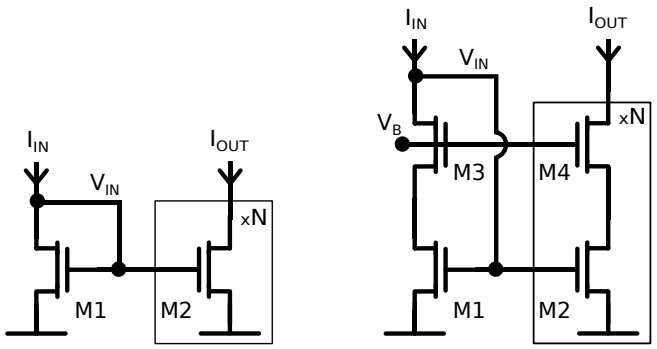


FIGURE 2.5 – Synthesized design approach for high-performance current mirrors.

In this section, we will discuss how to optimize size and bias of mirroring devices according to power, accuracy and current level requirements. For the sake of clarity, the modelling approach is illustrated on the simple diode-connected current mirror or its equivalent high-swing cascode configuration shown Fig. 2.6.



(A) Diode-connected CM (B) High-swing cascode CM

FIGURE 2.6 – Simple diode-connected and high-swing cascode

2.3.1 Power and accuracy optimization

With power-efficiency defined as the ratio between the amount of current delivered to the load over the amount of current consumed (input branch, output branches, auxiliary devices), we note that the only way to save power is to increase the mirror current gain (N), also called the copy-ratio and expressed as $1 : N$. For current mirrors with copy ratio of $1 : 1$, the power efficiency can not be greater than 1 and this figure automatically decreases when additional circuits are added. For higher current gain, the power efficiency can be expressed as in (2.8). I_{extra} represents current bias possibly required by additional circuitry. For current mirrors show in Fig. 2.6 this current is null[1].

$$PW_{EFF} = \frac{N}{1 + I_{\text{extra}}/I_{IN}} \tag{2.8}$$

Concerning the accuracy, the main factor is assumed to be the error on the output current due to device variability. Error induced by v_{ds} modulation will be eliminated using output impedance boosting techniques and topologies that ensure drain voltage equality for the mirroring devices. For instance, the high-swing cascode (Fig. 2.6b) offers high output impedance $r_{OUT} = g_{m4} r_{DS4} r_{DS2}$ and ensure that $V_{DS1} = V_{DS2}$ as long as M3 and M4 are matched and kept saturated. It is known that mismatch of cascoded transistor has low influence and drain current mismatch is the same for both saturation and linear regions.

In Chapter 1 (page 13), we have seen the equation for the relative mismatch error of the simple current mirror. For mirrors with current gain (N) larger than one, the relative mismatch error is given by equation (2.9). The mathematical derivation of this equation from MOS device models is given in Appendix C. Process quality is represented by constants A_β and A_{VTH} (random fluctuation amounts of V_{TH} and β), experimentally measured and provided by the technology manufacturer. From (2.9) we note again that output mismatch errors are inversely proportional to the square root of gate areas ($W \times L$). Large transistors

[1]Generation of the bias voltage V_B is not counted in the power budget. There exists too many ways to implement it, we have the possibility to share the voltage reference with other sub-parts and above all it does not significantly influence the other design choices

are the only way to minimize the influence of fluctuations over the physicals parameters μ, C_{OX}, W and L. Long channel length also tends to increase the device output impedance.

$$\frac{\sigma(I_{OUT})}{I_{OUT}} = \frac{1}{\sqrt{WL}}\sqrt{\left(\frac{1}{2N}\right)A_\beta^2 + \left(\frac{2N-1}{N}\right)\left(\frac{g_m}{I_{IN}}\right)^2 A_{VTH}^2} \tag{2.9}$$

The impact of threshold voltage mismatch is reduced by minimizing the g_m/I_{IN} ratio. With the representation of g_m/I_{IN} versus the normalized current $I_{IN}/(W/L)$ in Fig. 2.7, we observe that for good matching, the strong inversion operation is recommended. In this regime:

$$\frac{g_m}{I_{IN}} = \frac{2}{V_{EFF}} \qquad \text{(in strong inversion)} \tag{2.10}$$

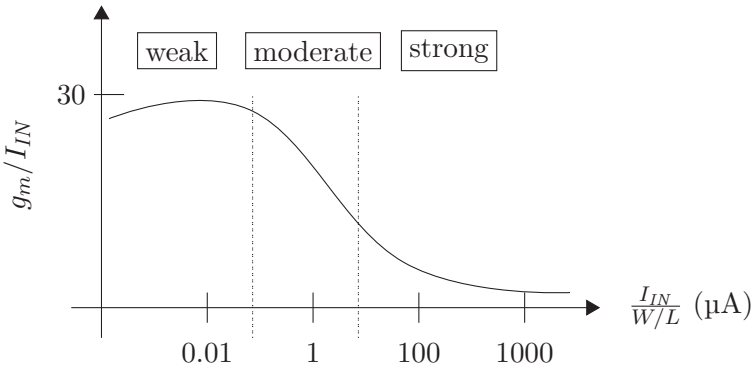


FIGURE 2.7 – g_m/I_{IN} ratio versus normalized drain current from weak to strong inversion

We also note that the higher the aspect ratio W/L, the more we need current to maintain the transistor in strong inversion. The last remark is that for fixed width W and length L, the highest mismatch error will occur at the lowest current level of the specified current range.

The maximum value of drive voltage V_{EFF} is dependent on input voltage requirement, or more broadly bounded by the maximum gate voltage admissible before saturating the system. The minimal value V_{EFFmin} is fixed by the technology. In classic CMOS processes the transition from moderate to strong inversion occurs at approximately 200 mV. Typically minimum input and output current are determined by the application and come, for instance, from previous stages specifications or signal-to-noise requirements. Hence, with I_{INmin} fixed, the aspect ratio is also fixed and expresses as in (2.11).

$$\left(\frac{W}{L}\right)_{1,2} = \frac{2I_{INmin}}{KV_{EFFmin}^2} = \frac{2I_{OUTmin}}{NKV_{EFFmin}^2} \tag{2.11}$$

By injecting equations (2.10) and (2.11) in (2.9), we obtain an expression for the worst-case mismatch error (2.12) only dependent on devices length L. Minimum drive voltage V_{EFFmin} and constants K, A_β, A_{VTH} are set by the technology. I_{INmin} or I_{OUTmin} are specified by the application.

$$ERR_{rel} = \frac{\sigma(I_{OUT})}{I_{OUT}} = \frac{1}{L}\sqrt{\left(\frac{K}{2I_{OUTmin}}\right)\left(\frac{V_{EFFmin}^2}{2}A_\beta^2 + 4(2N-1)A_{VTH}^2\right)} \tag{2.12}$$

This equation is valid for devices in strong inversion. What we see is that optimizing the accuracy ($1/ERR_{rel}$) with both sizes and bias as design parameters does not necessary lead to high drive voltage V_{EFF} (or high V_{GS}). Equation (2.12) shows that at low current levels it is better to have devices operating close to the transition from moderate to strong inversion. Long channel length and large bias current help to reduce mismatch errors.

The factor N scaling the contribution of threshold voltage mismatch in (2.12) also appears in the equation of power efficiency in (2.8). It represents the first part of the *speed-power-accuracy trade-off*. A potential metric appears, the power-accuracy ratio:

$$\frac{PW_{EFF}}{ERR_{rel}} = \frac{\dfrac{NL}{1 + I_{\text{extra}}/I_{IN}}}{\sqrt{\left(\dfrac{K}{2I_{OUTmin}}\right)\left(\dfrac{V_{EFFmin}^2}{2}A_\beta^2 + 4(2N-1)A_{VTH}^2\right)}} \tag{2.13}$$

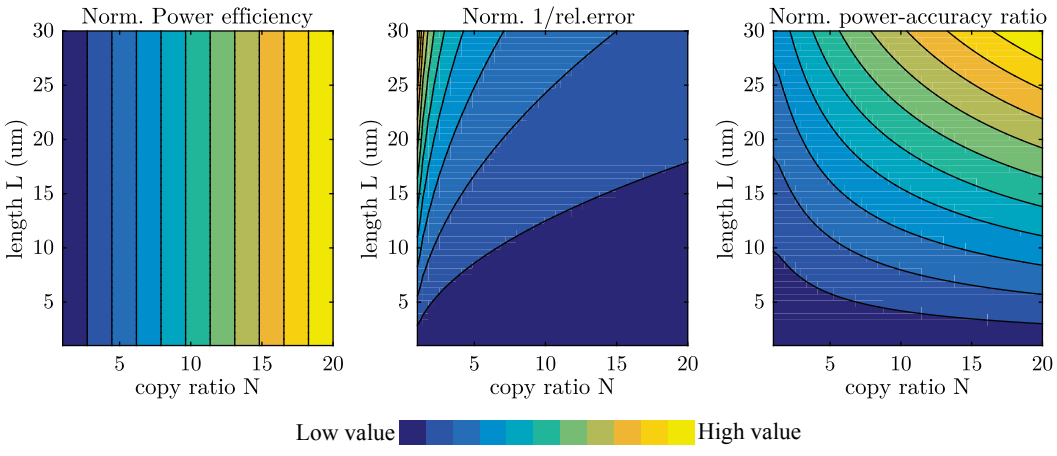
Numerical Application:

Technology: Standard CMOS 0.18 µm process at 1.8 V supply

K	A_β	A_{VTH}	V_{EFFmin}
250 µA V^{-2}	1.08 nm	1.65 nV m	200 mV

Application: Expected output current range I_{OUT}= 50 µA to 500 µA

Estimation: Calculation of power efficiency PW_{EFF}, inverse function of mismatch error $1/ERR_{rel}$ and the power-accuracy ratio defined in (2.13), with copy-ratio N varying from 1 to 20 and channel length L varying from 1 µm to 30 µm. Curves below are trend graphs that show the evolution of the metrics according to values of copy-ratio N and channel length L



Example 1: High precision current mirror

Theoretical calculation

N	L	W/L	PW_{EFF}	P_{load}/P_{tot}	ERR_{rel}	power-accuracy ratio
2	15 µm	5	2	66 %	0.061 %	33.2

Montecarlo simulation

K		V_{TH}		ERR_{rel}	
mean	std	mean	std	mean	std
256 µA V^{-1}	0.093 µA V^{-1}	443 mV	0.13 mV	0.003 %	0.1 %

Example 2: High power-efficiency current mirror

Theoretical calculation

N	L	W/L	PW_{EFF}	P_{load}/P_{tot}	ERR_{rel}	power-accuracy ratio
20	5.5 µm	0.5	20	95 %	0.59 %	33.7

Montecarlo simulation

K		V_{TH}		ERR_{rel}	
mean	std	mean	std	mean	std
246 µA V^{-1}	0.25 µA V^{-1}	453 mV	0.11 mV	0.091 %	0.57 %

We observe that both examples of high speed and high power efficiency current mirrors score the same value at the power-accuracy ratio. Meaning that they have been both optimized but different performances have been privileged. We will see in the next section how the conclusions drawn from this type of static optimization impact the speed performances and what analytic model can be used to optimize power consumption, accuracy and dynamic behaviour at the same time.

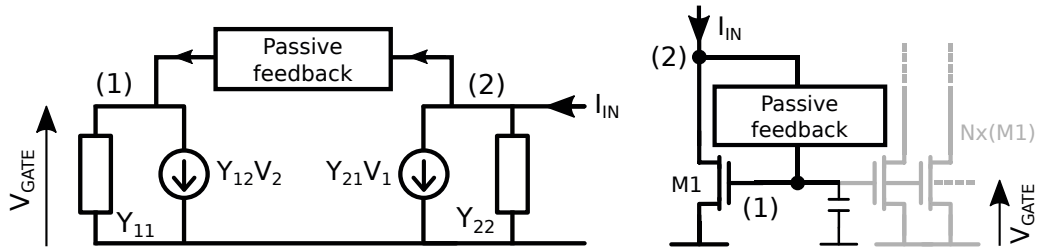
2.3.2 Consequences on dynamic behavior

Authors of (Alves and Aguiar, 2002) presents a study of frequency behaviour of classical current mirrors. They have shown that two major ratios dominate all the time constants in the frequency response:

$$\frac{1}{\tau_1} = \frac{g_m}{C_{GS}} \approx \frac{3\sqrt{2}}{2}\sqrt{\frac{\mu I_{IN}}{WL^3 C_{OX}}} \qquad \frac{1}{\tau_2} = \frac{g_{DS}}{C_{GS}} \propto \frac{I_{IN}}{WL^2 C_{OX}} \tag{2.14}$$

We note that at first order, bandwidth of the current transfer function only depends on the maximum achievable speed to vary the gate-to-source voltage of mirroring devices ($1/\tau_1$). Thus for speed consideration, we will focus on the study of the trans-impedance transfer function V_{GATE}/I_{IN}, as illustrated Fig. 2.8. We only need to study and model the current mirror input branch to estimate the dynamic behaviour. Influence of the output branch, and more specifically influence of output impedance frequency response will superimpose to the 1st order behaviour dictated by the gate voltage response. The evaluation of dynamic

operation is based on the admittance matrix representation of the current mirror. Links between bias levels, physical properties and small-signal parameters have been discussed in section 2.1.



(A) Small signal model expressed with admittance parameters

(B) Schematic

FIGURE 2.8 – Simple current mirror with generic gate-to-drain feedback

The input branch of the current mirror is modelled using the Y-matrix defined in (2.15). In these expressions, no feedback block is considered. We note that the admittance parameters are similar to the ones found for a single MOS device, the exception resides in the parameter y_{11}. Indeed now we are looking at a current mirror, the overall capacitance between gate (node 1) and source (ground) is multiplied by the number of devices in parallel (N) that compose the output branch.

$$Y_{CM} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} + C_{11}s & g_{12} - C_{12}s \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} = \begin{bmatrix} (N+1)C_{GS}s & -C_{DG}s \\ g_m - C_{GD}s & g_{DS} \end{bmatrix} \tag{2.15}$$

For the basic or high-swing cascode diode-connected current mirror the "passive feedback" block in Fig. 2.8a is simply replaced by a wire connecting the input drain (node 2) with the gates (node 1). From this small-signal model, we derive the transimpedance transfer function which expresses as:

$$\begin{aligned} \frac{V_1}{I_2} = \frac{V_{GATE}}{I_{IN}} &= \frac{1}{y_{11} + y_{12} + y_{21} + y_{22}} \\ &= \left(\frac{1}{g_m + g_{DS}}\right) \frac{1}{1 + \dfrac{(N+1)C_{GS} - C_{GD} - C_{DG}}{g_m + g_{DS}} s} \\ &\approx \left(\frac{1}{g_m}\right) \frac{1}{1 + \dfrac{(N+1)C_{GS}}{g_m} s} \end{aligned} \tag{2.16}$$

Continuing with design choices made for optimized *static performances*, namely, devices on the edge of the strong inversion at minimum input current, we have $g_m = \sqrt{2\mu C_{OX}(W/L)I_{INmin}}$ and $C_{GS} = (2/3)\mu C_{OX}$. Finally, the bandwidth of the current transfer function, expressed with large signal parameters, is equal to (2.17). We retrieve the first ratio mentioned in (Alves and Aguiar, 2002).

$$BW = \frac{3\mu V_{EFFmin}}{2(N+1)L^2} \tag{2.17}$$

From there, we observe that to increase the speed of a diode-connected current mirror, bias current I_{INmin} ($\approx K(W/L)V_{EFFmin}^2$) should be increased and copy-ratio N decreased, but this will degrade the power consumption and power efficiency. The other option is the reduction of device width W and length L but with the consequence of an altered accuracy. To evaluate both static and dynamic performances at the same time we can derive a metric similar to the figure-of-merits presented in Chapter 1. For instance, let's define:

$$\frac{PW_{EFF} \times BW}{ERR_{rel}} = \frac{\dfrac{3\mu V_{EFFmin} N}{2(1+I_{\text{extra}}/I_{IN})(N+1)L}}{\sqrt{\left(\dfrac{K}{2I_{OUTmin}}\right)\left(\dfrac{V_{EFFmin}^2}{2}A_\beta^2 + 4(2N-1)A_{VTH}^2\right)}} \tag{2.18}$$

Evolution of the metric (2.18) according to variations of length L and copy-ratio N shows that best scores are achieve with small length and copy-ratio close to one, which again conflicts with design choices for high accuracy and high power efficiency. The more important remark is that to maintain equivalent score, an increase of devices length is traduced by a reduction of copy-ratio. In other words, we have found once more the *speed-power-accuracy trade-off* and the limits imposed by the technology.

2.4 Conclusion

In this chapter, we have introduced the basis of a generic formalism (sections 2.1 and 2.2), based on classical CMOS device models and dedicated to the optimization of current mirrors in relation with the *speed-power-accuracy trade-off*. From this first theoretical study, arise a proposition of a design strategy and a set of metrics that will enable the solution exploration for the realization of high-performance current mirrors. The proposed strategy, which will be adopted for the next presented topologies, relies on power-efficient speed boosting techniques applied to very large but precise current mirrors to relax the trade-off on speed, power and accuracy previously highlighted. Dimensions and biases of mirroring devices, as well as the mirror copy ratio, are set according to static performances. The dynamic behaviour is treated in a second step, with the help of additional active blocks and control loops.

In section 2.3, from assumptions and models previously defined, several expressions for the *speed-power-accuracy trade-off* in classical current mirrors are derived and illustrated. This general study concerns the diode-connected types of current mirror. It has been shown that for such mirrors, independently of the privileged performance, the relation between speed, power and accuracy is fixed and limited by technological constants related to the nature and quality of the process used. Finally, among the enhanced current mirror structures discussed in Chapter 1, if we eliminate the ones with diode-connected mirroring devices, we are left with solutions that use active devices on the input branch to control gate and

drain evolutions. Capabilities and limits of active-input current mirror topologies to relax the *speed-power-accuracy trade-off* is the subject of the next chapter.

Chapter 3

Design of fast precise and accurate current mirror with linear feedback circuits

In the previous chapter, we have studied the effect of static performance optimisation on the dynamic behaviour for diode-connected types of current mirror. At the end, we have concluded that only solutions that use active devices on the input branch to control gate and drain evolutions, will allow us to go beyond the limit fixed by the technology. This Chapter starts with a theoretical study that proves the relevance of active feedback to improve speed of current mirrors. Then, the reader will find a dedicated formalism intended to theorize and systematize the design of the existing standard active-input topology. Then will follow two propositions that improve the behaviour of such current mirrors at minimal cost. The first solution is made for larger dynamic ranges, the second for faster responses.

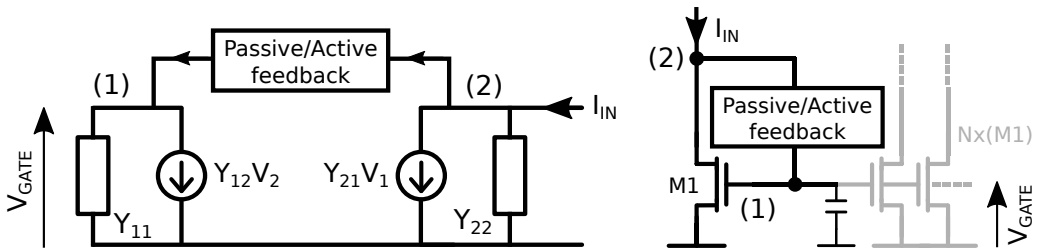
3.1 Active feedback for better dynamic performances

In Chapter 2, we used our formalism to derive an expression for the *speed-power-accuracy trade-off* in classical diode-connected current mirrors. We have seen that in this case the optimization of both static and dynamic performances is unavoidably limited by technological constants. Now we will see, if instead of a simple drain to gate connection, we use an active circuit on the current mirror input branch to control the gate voltage.

For instance, a transconductance stage (g_{mA}) replaces the wire in the "passive/active feedback" block Fig. 3.1a. This active sub-circuit would sense input voltage variations (node 2) and provides a current that adjusts the gate voltage (node 1) according to input current change.

We have already defined the admittance matrix of the input branch Y_{CM}. Equation (3.1) is a recall from (2.15) page 43. With the simplistic assumption that the transconductance stage is ideal, meaning infinite input impedance and ideal current generator on the output, the admittance matrix of the system Y_{SYST} expresses now as (3.2).

$$Y_{CM} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} + C_{11}s & g_{12} - C_{12}s \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} \tag{3.1}$$



(A) Small signal model expressed with admittance parameters

(B) Schematic

FIGURE 3.1 – Simple current mirror with generic gate-to-drain feedback

$$Y_{SYST} = \begin{bmatrix} y'_{11} & y'_{12} \\ y'_{21} & y'_{22} \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} - g_{mA} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} + C_{11}s & g_{12} - C_{12}s - g_{mA} \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} \tag{3.2}$$

By solving the system $I = Y_{SYST}.V$ with initial condition $I_1 = 0$, we can derive the transimpedance transfer function including the active feedback (3.3). Here we have assumed that gate-to-drain an drain-to-gate capacitances (C_{GD},C_{DG}) are negligible.

$$\frac{V_{GATE}}{I_{IN}} = \frac{g_{mA} - y_{12}}{y_{11}y_{22} + y_{21}(g_{mA} - y_{12})} \approx \left(\frac{1}{g_m}\right) \frac{1}{1 + \dfrac{g_{DS}}{g_{mA}} \dfrac{(N+1)C_{GS}}{g_m} s} \tag{3.3}$$

With active feedback on the input, the bandwidth has been multiplied by a factor g_{mA}/g_{DS}. This factor can be linked to physical parameters. $g_{DS} = \lambda I_{IN}$ and with the assumption that the the transconductance stage is realized with a differential pair biased to operate at the limit of moderate to strong inversion, $g_{mA} = I_{\text{extra}}/V_{EFFA}$ and $V_{EFFA} = V_{EFFmin}$. Hence, the new bandwidth can be formulated as in (3.4).

$$BW_{ai} = \left(\frac{3\mu V_{EFFmin}}{2(N+1)L^2}\right)\left(\frac{NI_{\text{extra}}}{\lambda I_{OUTmin} V_{EFFA}}\right) \tag{3.4}$$

Recalculating the speed-power-accuracy ratio gives:

$$\frac{PW_{EFF} \times BW_{ai}}{ERR_{rel}} = \frac{\dfrac{3\mu V_{EFFmin} N^2 I_{\text{extra}}}{2L(N+1)\lambda V_{EFFA}(I_{OUTmin} + NI_{\text{extra}})}}{\sqrt{\left(\dfrac{K}{2I_{OUTmin}}\right)\left(\dfrac{V_{EFFmin}^2}{2} A_\beta^2 + 4(2N-1)A_{VTH}^2\right)}} \tag{3.5}$$

The first remark is the fact that active gate control offers a new degree of freedom to optimize current mirror in terms of speed, power and accuracy. Indeed, the parameters $Iextra$ and V_{EFFA} are almost independent of other current mirror characteristics. Moreover, with moderate amount of additional bias current, it is now possible to increase device length for better matching and copy-ratio for better power efficiency, while ensuring equivalent overall performances. This is reflected by a constant scores at the speed-power-accuracy ratio. The following numerical application illustrates these assertions.

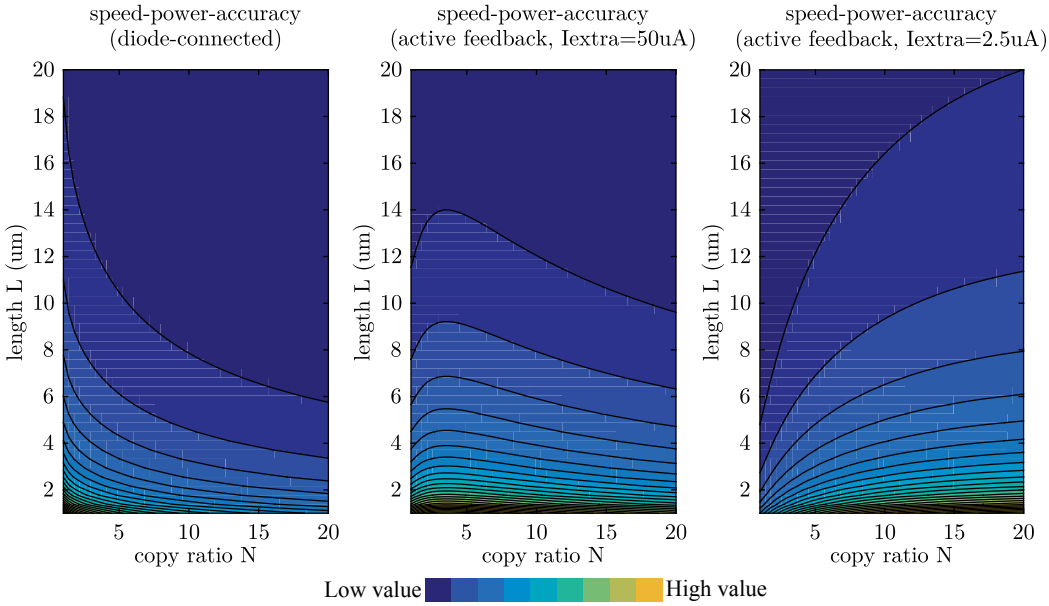
Numerical Application:

Technology: Standard CMOS 0.18 µm process at 1.8 V supply

μ	C_{OX}	A_β	A_{VTH}	V_{EFFmin}	λ
35 µA V^{-2}	7.1 µF µm^{-2}	1.08 nm	1.65 nV m	200 mV	0.09 V^{-1}

Application: Expected output current I_{OUT}= 100 µA

Comparison: Calculation of speed-power-accuracy ratio (SPA ratio) for the diode-connected current mirror (2.18) and for active current mirror with transconductance stage (3.5). Current gain N varies from 1 to 20 and channel length L varies from 1 µm to 20 µm.



Example 1: High-speed CM

Theoretical calculation

				diode-connected			active feedback		
N	L	W	ERR_{rel}	BW	$\frac{P_{load}}{P_{tot}}$	SPA ratio	BW	$\frac{P_{load}}{P_{tot}}$	SPA ratio
-	µm	µm	%	MHz	%	-	MHz	%	-
2	5.5	55	0.12	115	67	1990	320	65	5270

Example 2: High power-efficiency CM

Theoretical calculation

				diode-connected			active feedback		
N	L	W	ERR_{rel}	BW	$\frac{P_{load}}{P_{tot}}$	SPA ratio	BW	$\frac{P_{load}}{P_{tot}}$	SPA ratio
-	µm	µm	%	MHz	%	-	MHz	%	-
20	15	15	0.15	2.2	95	289	62	93	5350

We observe in the numerical application above that with diode-connected topologies, saving power degrades the overall performances. Indeed, both examples show similar error amount but their scores at the speed-power-accuracy ratio are drastically different. The high speed current mirror obtains a score of 1990 while the high power efficiency current mirror obtains a score of only 289, despite the fact that its power efficiency has raised up to 95 %. However with active feedback ($I_{extra} = 2.5\,\mu A$) the two examples obtain an equivalent score of about 5300 thanks to the speed improvement offered by the active block. This generic study, even if it is not sufficient to assert any conclusion, gives an insight to the relevance of active feedback current mirrors to obtain fast and precise response with optimized power consumption.

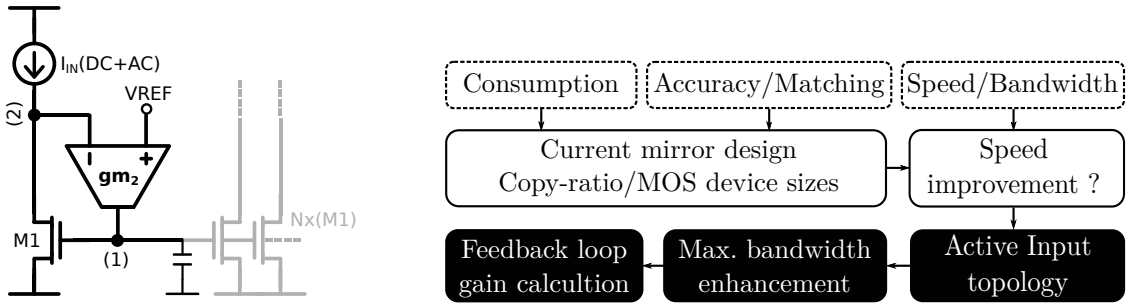
Current mirror with active feedback realized with a transconductance stage is a structure found in the literature as the active-input topology. The next section is a more detailed study of possibilities and limits offered by this specific topology. We will see how to select the optimal feedback gain and what type of response we can achieve.

3.2 The basic active-input current mirror

The active-input current mirror (Fig. 3.2a), first introduced by Serrano *et al.* (Serrano and Linares-Barranco, 1994), has been proposed to enhance input compliance and speed-power ratio of dynamic current mirrors in various applications as in (Moazzeni and Cowan, 2009) or (Nairn and Salama, 1990). The structure is based on a shunt-shunt feedback configuration using an OTA around the current mirror. It has the advantages of a voltage regulated input and a controlled speed. To preserve its use as fundamental building block for current sources, an active current mirror should exhibits a response shape similar to diode-connected mirrors, especially in terms of resonance, oscillation amount and overshoot. Although the active-input current mirror has been used in different practical implementations, as far we know, none of previous related work have proposed analytical tools to study and optimize the speed-power ratio improvement alleged.

To design an optimized structure, we will adopt the approach depicted in Fig. 3.2b, which is based on the general strategy discussed in Chapter 2. Number of parallel devices, sizes and bias of copying transistors are set according to static requirements. Then, we study the ability of the feedback loop to speed up the mirror response, whereas the overall system exhibits a dynamic response similar to diode-connected current-mirror. The proposed approach starts with the estimation of the maximum bandwidth reachable and then uses the calculation flow presented section 3.2.1 to compute the OTA gain value from the desired frequency behaviour.

In the next sections, performances of the active-input mirror under design is compared to its equivalent diode-connected configuration. A linear small-signal representation is used to study the system, where the current mirror is represented by its admittance matrix according to the method presented Chapter 2. An ideal operational transconductance amplifier (OTA) model the linear feedback circuits. Actual OTA input and output impedances can possibly be studied separately as covered in appendix D.



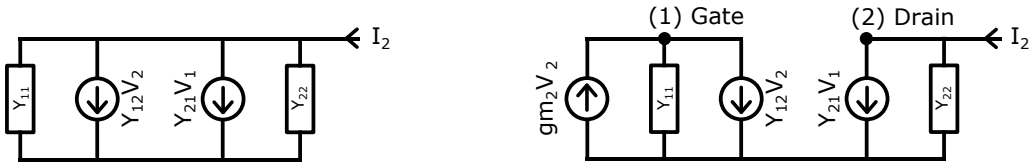
(A) Schematic (B) Generic design approach

FIGURE 3.2 – Basic active-input current mirror

3.2.1 Transimpedance transfer functions and stability study

Modelling current mirror with its admittance matrix (Y_{CM}) allows to get design parameters for the feedback loop independently to the current mirror topology. The admittance parameters can be directly extracted from simulation with respect to process corners and for several levels of input current. This gives designers the opportunity to study system behaviour against process variations and evolution of intrinsic MOS parameters over large input current ranges. For a given operating point, the admittance matrix expresses as in (3.6) and has been used for the small signal models shown Fig. 3.3. Compared to the previous definition, we start with the assumptions that parameters y_{11} and y_{12} are pure capacitive components.

$$Y_{CM} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} C_{11}s & -C_{12}s \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} \tag{3.6}$$



(A) Diode-connected CM (B) Active-input CM

FIGURE 3.3 – Mid-frequency 2nd-order models

Thereafter, the indices $_{\text{dco}}$ will refer to the diode-connected current mirror, while the indices $_{\text{ai}}$ will refer to the active-input one. From small-signal models introduced figure Fig. 3.3, trans-impedance transfer functions of both mirrors are derived in Table. 3.1.

Diode-connected CM	
$\left(\frac{V_{gs}}{I_{IN}}\right)_{\text{dco}} = G\frac{1}{1+\frac{s}{\omega_{\text{dco}}}}$	$\omega_{\text{dco}} = \frac{g_{21}}{C_{11}+C_{22}-C_{21}-C_{12}}$ $G = \frac{1}{g_{21}}$
OTA-based active-input CM	
$\left(\frac{V_{gs}}{I_{IN}}\right)_{\text{ai}} = G\frac{1+\frac{s}{\omega_1}}{1+2m\frac{s}{\omega_{\text{ai}}}+\frac{s^2}{\omega_{\text{ai}}^2}}$	$\omega_1 = \frac{g_{m2}}{C_{12}}$ $\omega_{\text{ai}}^2 = \frac{g_{21}g_{m2}}{C_{11}C_{22}-C_{21}C_{12}}$ $\frac{2m}{\omega_{\text{ai}}} = \frac{g_{22}C_{11}+g_{21}C_{12}-g_{m2}C_{21}}{g_{21}g_{m2}}$ $G = \frac{1}{g_{21}}$

Table 3.1 – Transimpedance transfer function for diode-connected and active-input CM.

Introducing active feedback has increased the system order, the structure is now subject to potential stability issues. The next step is to derive conditions over the feedback gain $gm2$ to keep the system in a stable state. Basically, for a system to remains stable, the real parts of all poles in its transfer functions have to be negative. Poles of the active-input mirror are roots of the second order polynomial:

$$1+\left(\frac{g_{22}C_{11}+g_{21}C_{12}-g_{m2}C_{21}}{g_{21}g_{m2}}\right)s+\left(\frac{C_{11}C_{22}-C_{21}C_{12}}{g_{21}g_{m2}}\right)s^2 \tag{3.7}$$

Finally, the stability condition expresses as:

$$g_{m2}>0 \quad \text{and} \quad g_{m2}<\frac{g_{22}C_{11}+g_{21}C_{12}}{C_{21}} = g_{m2\text{MAX}} \tag{3.8}$$

3.2.2 Bandwidth enhancement capabilities

The interest in using active-input topologies resides in an increase of the mirror speed while it shows a dynamic response similar to the classic current mirror response. Specially in term of oscillation and overshoot. To compare bandwidth of the active-input mirror and the basic diode-connected mirror used as reference, we define a bandwidth enhancement factor K as follows:

$$K = \frac{\omega_{\text{ai}}}{\omega_{\text{dco}}} \tag{3.9}$$

Corner frequencies ω_{dco} and ω_{ai} for both system are found Table. 3.1. Given an target objective for the speed, we can combine expressions of ω_{dco} and ω_{ai} with the definition in

(3.9), to derive the upper limit for K as a function of g_{m2}.

$$K^2 < \frac{g_{m2}}{g_{21}} \frac{(C_{11} + C_{22} - C_{21} - C_{12})^2}{C_{11}C_{22} - C_{21}C_{12}} \tag{3.10}$$

At this point, the damping factor m has not been investigated. It needs to be evaluated because its value influences the poles locations around the corner frequency and consequently modifies the mirror response. By identification in the transimpedance transfer function, the damping factor is expressed as:

$$m = \frac{1}{2} \frac{g_{22}C_{11} + g_{21}C_{12} - g_{m2}C_{21}}{\sqrt{g_{m2}g_{21}\left(C_{11}C_{22} - C_{12}C_{21}\right)}} \tag{3.11}$$

The feedback gain g_{m2} is the only degree of freedom available to control the frequency behaviour. Others parameters C_{ij} and g_{ij} are determined by design choice made during static optimization. As a consequence, we cannot control the damping factor m and the corner frequency location independently. It must be noticed that higher the feedback gain value (g_{m2}), the more the system exhibits oscillatory response. To get the expected $gm2$ value with a fixed m factor, the following equation must be solved:

$$Ag_{m2}^2 + Bg_{m2} + C = 0 \tag{3.12}$$

with:

$$A = (C_{21})^2 \tag{3.13}$$

$$B = 2\left(g_{21}C_{12}C_{21} + g_{22}C_{21}C_{11}\right) + 4m^2 g_{21}\left(C_{11}C_{22} - C_{12}C_{21}\right) \tag{3.14}$$

$$C = -(g_{22}C_{11})^2 - (g_{21}C_{12})^2 - 2g_{22}C_{11}g_{21}C_{12} \tag{3.15}$$

An interesting result is the expression of g_{m2} , shown in (3.16), and the corresponding K factor, shown in (3.17), when the damping factor is fixed at the particular value of $m = 1$. At this particular damping amount, both poles are real and equals, the system is moving from an under-damped to an over-damped one. With a typical value $m = 1$, we ensure that no overshoot or pseudo-oscillation occur and still have a margin to accept device variations before the system start to show oscillatory behaviour.

$$g_{m2@m=1} = \frac{(g_{22}C_{11})^2 + (g_{21}C_{12})^2 + 2g_{21}g_{22}C_{11}C_{12}}{2g_{22}C_{11}C_{21} + g_{21}(4C_{11}C_{22} - 2C_{12}C_{21})} \tag{3.16}$$

$$K_{@m=1} = \sqrt{\frac{g_{m2@m}\left(C_{11} + C_{22} - C_{12} - C_{21}\right)^2}{g_{21}\left(C_{11}C_{22} - C_{12}C_{21}\right)}} \tag{3.17}$$

$$\omega_{\mathrm{ai@m=1}} \approx \sqrt{\frac{g_{21}}{2C_{11}^2}} \frac{g_{22}C_{11} + g_{21}C_{12}}{\sqrt{g_{22}C_{21}C_{22} + 2g_{21}C_{22}^2}} \tag{3.18}$$

Finally, through the use of a properly estimated Y-matrix we are able to predict the benefits of the active-input solution in terms of response speed. With regards to a desired

damping value, the K factor range indicates the ability to extend the initial bandwidth. Using this results to calculate the feedback loop gain will ensure the highest bandwidth from the desired frequency behaviour.

3.2.3 Illustration through a case study

This section exemplifies theoretical analysis and assertions presented before through an arbitrary case example. We compare the active-input and the diode-connected topology with identical MOS devices. Results are shown for the system tuned to achieve a critically damped response with various external capacitance loading the input drain. Circuits have been simulated using the AMS 0.18μm CMOS design kit, under a 1.8V supply voltage.

Transistors M1 and M2 have a W/L ratio of 0.7, with $L = 10\mu$m. The input DC current for biasing is for both cases 10μA, leading to a $V_{\mathrm{EFF}} = 350$mV. This operating point gives, for the diode-connected mirror, a standard deviation for the mismatch-induced copy error of 0.21% (obtained with 200 runs in monte-carlo simulation). The OTA in Fig. 3.2a, is implemented using a ideal current controlled source with a transconductance gain of g_{m2} and an input capacitance referred as C_{OTA}, acting as a drain load. These current mirrors will be considered with 20 output branches, giving an DC output current of 200μA. The table 3.2 gives the result of the admittance matrix extraction under the condition mentioned above.

g_{21} ($\mu A/V$)	C_{11} (pF)	C_{12} (fF)	C_{21} (pF)	C_{22} (fF)	g_{22} (nA/V)
54.2	4.3	2.6	0.14	7.8 / 17.8 / 42.8	429.7

Table 3.2 – Y-parameters of the A-I current mirror

Except for the calculation below, intended to determine the maximum drain load tolerated, the OTA input capacitance C_{OTA} is directly included in the C_{22} parameter and taken as 0fF, 10fF and 35fF

At the stability limit, calculated value of $g_{m2\mathrm{MAX}}$ is close to $25\,\mu\mathrm{A\,V^{-1}}$ for each load capacitance. A feedback loop gain beyond this value will cause the system response to diverge and no steady-state could be reached.

Table 3.3 shows numerical results of, the diode-connected CM corner frequency (F_{dco}), the bandwidth enhancement factor value (K) when the system is critically damped ($m = 1$), the related feedback gain g_{m2} and finally the resulting value of the active-input CM corner frequency F_{ai}. Simulated bandwidths are given fig. 3.4. Numerical and simulation results correlate as expected, calculated corner frequencies $F_{\mathrm{ai}}@m = 1$ correspond to the measured -3dB bandwidth observed during simulations.

3.2.4 Discussion and conclusion

First, from equations in section 3.2.2, we note that if the number of parallel output branches is large enough, then the resulting bandwidth ($F_{\mathrm{ai}}@m = 1$) become independent to the global gate capacitance (C_{11}). At a certain point, adding branches will only affect the OTA

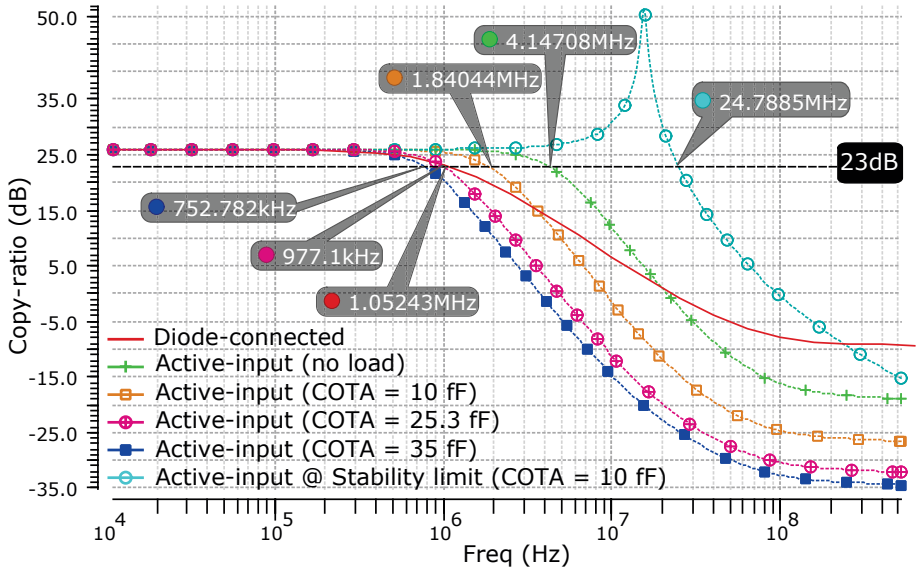


FIGURE 3.4 – Copy-ratio vs. Magnitude @ $m = 1$

	C_{OTA}		
	0fF	10fF	35fF
F_{dco} (MHz)	1.0	1.0	1.0
$K@m = 1$	4.3	1.9	0.8
$g_{m2}@m = 1$ (μA/V)	0.90	0.41	0.17
$F_{\text{ai}}@m = 1$ (MHz)	4.3	1.9	0.8

TABLE 3.3 – Numerical results for the critically damped system

gain but not the bandwidth, unlike in the diode-connected structure. Based on this fact, we can say that the active-input topology better suits current mirrors with large copy-ratio or large number of parallel outputs, which is also the adequate solution to reduce power waste.

On the other hand, the proposed formalism can be used to estimate the speed improvement capability of the active input technique and shows that improvement are feasible. Nonetheless, this demonstrated ability to extend the bandwidth is derived from a linear 2nd-order system model. When wide dynamics for currents or voltages are targeted, intrinsic MOS characteristics vary significantly. Model parameters and feedback loop gain (OTA gain) have to be re-evaluated. For instance, the transconductance factor g_m increases proportionally to $\sqrt{I_{IN}}$, while output impedance r_{DS} decreases linearly with I_{IN}. The study of dominant parameter variation for large-signals is needed for a proper estimation of the system behaviour across the dynamic range. In the next section (3.3) we propose a modified version of the basic active-input structure which includes an OTA with adaptive biasing to overcome limitations found on the dynamic range.

The last observation concerns the sensitivity of this structure to MOS output conductance (g_{22}) and input capacitance (C_{22}) which represents the second dominant pole of the system. Those two parameters are difficult to keep under control when designing with advanced nodes. Moreover, from equations (3.16) to (3.18) we note that with a decrease of output conductance (g_{22}) the system tends to be more unstable. This conflicts with the use of

large devices and cascode techniques required for high accuracy. Later, in section 3.4, we detail a stabilized version of the active-input structure, proposed to enlarge the stability domain, which solves the strong dependency of the active input topology to intrinsic device characteristics.

3.3 Adaptive-biasing technique for active-input current mirror

As said before, when targeting large input current range, because intrinsic current mirror characteristics will vary but the feedback loop gain will stay constant, we likely face a detuned feedback which will cause the system behaviour to shift from prediction. In this section, a new feedback structure for the active-input current mirror is proposed, where the feedback loop gain is made dependent on the DC input current level, ensuring the speed performances of the classical active-input topology over a wider input dynamic.

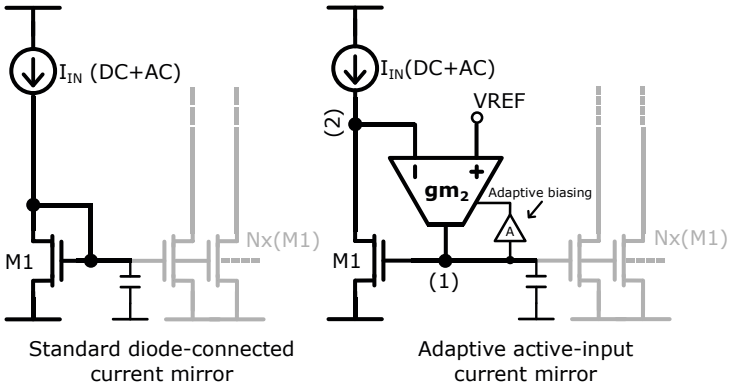


FIGURE 3.5 – Principle of the adaptive biasing for active-input CM

3.3.1 Calculation of the initial feedback loop gain

From the generic modelling presented section 3.2, we recall in (3.19) the OTA gain $g_{m2@m=1}$ leading to a critically damped response and in (3.20) the related system bandwidth $BW_{\text{ai@m=1}}$. Components C_{11}, C_{22}, g_{22}, g_{21} model respectively the total gate-to-ground capacitance, the overall drain-to-ground capacitance, the overall output conductance of the input branch and the input MOS transconductance. The gate-drain capacitance is represented by C_{21} when the gate voltage is varying and by C_{12} when the input drain voltage is changing.

$$g_{m2@m=1} = \frac{(g_{22}C_{11})^2 + (g_{21}C_{12})^2 + 2g_{21}g_{22}C_{11}C_{12}}{2g_{22}C_{11}C_{21} + g_{21}(4C_{11}C_{22} - 2C_{12}C_{21})} \tag{3.19}$$

$$BW_{\text{ai@m=1}} = \sqrt{\left(\sqrt{2}-1\right)\frac{g_{21}(g_{m2@m=1})}{C_{11}C_{22} - C_{21}C_{12}}} \tag{3.20}$$

For a given operating point we extract values of current mirror components C_{ij} and g_{ij} and then deduce the optimum OTA gain g_{m2}. If the operating point varies, there are two cases:

- The feedback gain becomes lower than expected, the system is getting slower, and for large differences, the active-input current mirror may show poorer speed-power ratio than the equivalent diode-connected current mirror.
- The feedback gain is higher than expected, the system becomes under-damped and the amount of overshoot and oscillation directly relate to the difference between the actual OTA transconductance and the expected one.

3.3.2 Adaptive biasing operation

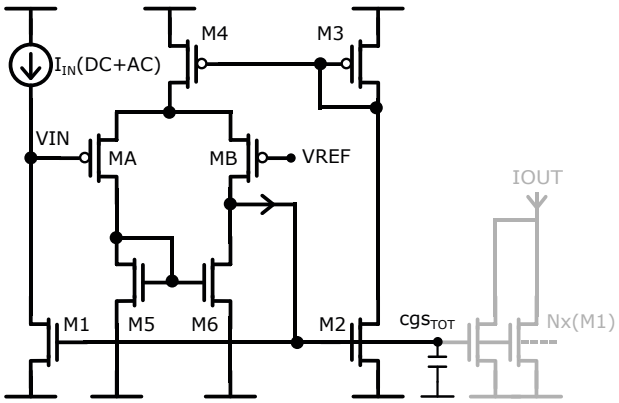


FIGURE 3.6 – Active-input current mirror with adaptive biasing

To ensure speed performances of the basic active-input topology over a larger input dynamic, we implement an adaptive biasing of the OTA to link its transconductance to the DC input current level. When MOS characteristics are changing, the adaptive bias tune the OTA transconductance to reduce the difference with its expected value. A simple implementation of the active-input structure with adaptive biasing is shown Fig. 3.6.

As a first approximation, it is known that the output conductance of M1 (g_{22} here) varies proportionally to the input current I_{IN} and the transconductance of M1 (g_{21} here) varies proportionally to the square root of the input current I_{IN}. Thus, using (3.19) and the previous assumptions, we can prove that the OTA gain should increase to maintain the desired speed when the input current increases. If we define the coefficient α as $I_{IN} = \alpha I_{INmin}$ and assume as an approximation that only g_{22} and g_{21} of the current mirror are varying, then the bandwidth of the active input with adaptive biasing (indices $_{\text{aai}}$) and the basic active input (indices $_{\text{bai}}$) can be expressed according to input current variation.

$$BW_{\text{aai}} = \omega_{\text{ai}min}\sqrt{\alpha\left(\sqrt{(2\alpha-1)^2+1}-(2\alpha-1)\right)} \tag{3.21}$$

$$\text{with} \quad g_{m2aai} = \sqrt{\alpha}\, g_{m2min} \tag{3.22}$$

$$BW_{\text{bai}} = \omega_{\text{ai}min}\sqrt{\sqrt{\alpha}\left(\sqrt{(2\alpha\sqrt{\alpha}-1)^2+1}-(2\alpha\sqrt{\alpha}-1)\right)} \tag{3.23}$$

Finally, we prove the theoretical efficiency of our proposed enhancement by comparing the evolution of bandwidths in (3.22) and (3.23) when α increases. Fig. 3.7 shows the evolution of the scaling factor ($\sqrt{...}$) multiplying the corner frequency ($\omega_{\text{ai}min}$) in bandwidth equations. We note that when $\alpha = 1$ (meaning $I_{IN} = I_{INmin}$) we have $BW_{\text{aai}} = BW_{\text{bai}}$ as expected, the same speed is achieved. But for instance, whis $\alpha = 5$ then $BW_{\text{aai}} = 2.3BW_{\text{bai}}$, the adaptive active-input shows better speed performance.

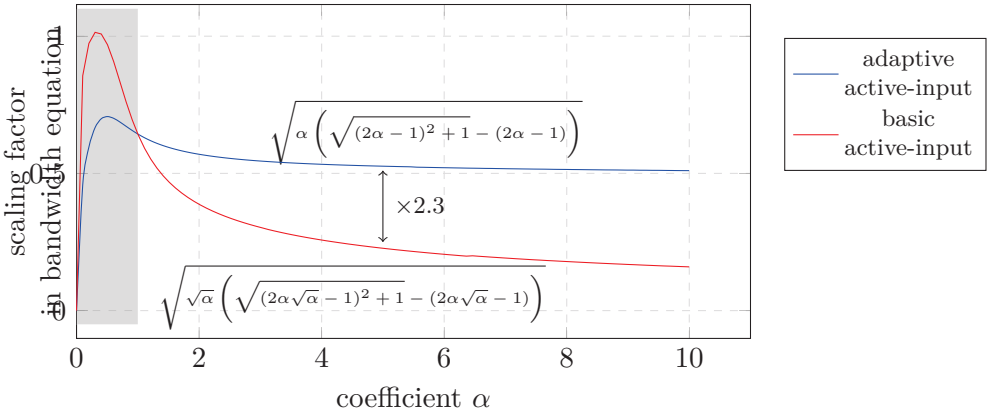


FIGURE 3.7 – Evolution of the scaling factor in bandwidth equations against evolution of input current level

We can notice that the relative speed improvement over the input current range, between a basic active-input and an adaptive active-input solution, is independent of the mirror characteristics and by extension, independent of the devices sizes or the mirror structure (cascode, drain regulation, ...). Ratio between (3.23) and (3.22) only depends at the end on the parameter α reflecting the current dynamic range.

3.3.3 Design considerations and noise analysis

In Fig. 3.6, the adaptive bias circuit (M2, M3) is a common-source amplifier placed between the mirror gates and the gate of the transistor biasing the differential pair of the OTA. The input capacitance of this common-source amplifier has to be negligible compared with the total gate-to-ground capacitance, or taken into account in the parameter C_{11} when calculating the optimum OTA gain value with (3.19) and (3.20). Moreover, for large signal variation, we must ensure that the common-source amplifier bandwidth is equal or larger than the overall system bandwidth, needed to guarantee that the OTA gain tuning is fast enough to follow system variations. Relative aspect ratio for transistors M2, M3 and M4 can be derived from the OTA bias current I_{D4} required to perform a transconductance gain of g_{m2min} at I_{INmin}, and from the common-source amplifier bandwidth which needs to be greater than $BW_{\text{ai@m=1}}$. With α defined as $I_{IN} = \alpha I_{INmin}$, V_{EFF} of M4, MA and MB are seen proportional to $\sqrt{\alpha}$. High level DC input current might saturate the OTA gain. To maximize the speed benefits of this structure, these transistors should be designed with large W/L ratio for low V_{EFF} at minimum input current I_{INmin}.

In the next analysis, we are interested in the output current noise, when considering both thermal and flicker noise sources. Input referred noise due to the OTA bias transistor M4 has not been included as it is assumed to be negligible thanks to the symmetry of the

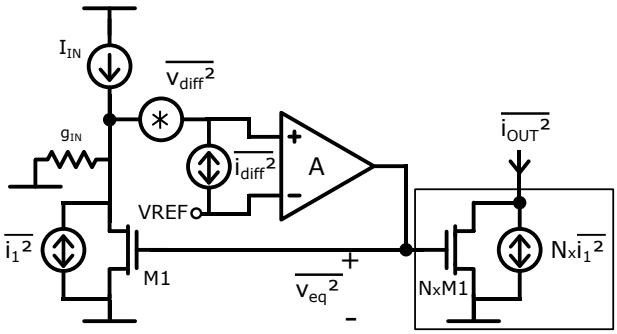


FIGURE 3.8 – Noise model of the active-input structure

structure, which is not the case for the differential pair noise. Fig 3.8 shows the model considered to estimate output noise contributions. Inside the system bandwidth, the output noise power spectral density $\overline{i_{out}^2}$ can be expressed in relation with the intrinsic noise of the current mirror elementary transistor $\overline{i_1^2}$ and with the noise generated by the differential pair $\overline{v_{diff}^2}$ as:

$$\overline{i_{out}^2} \approx (N^2+N)\overline{i_1^2} + N^2\overline{i_{in}^2} + (g_{in}N)^2\overline{v_{diff}^2} \tag{3.24}$$

with:

$$\overline{i_1^2} = 4KT\gamma g_{m1} + \frac{K_f g_{m1}^2}{W_1 L_1 C_{ox} f} \tag{3.25}$$

$$\overline{v_{diff}^2} = 8KT\gamma\left(\frac{g_{mA}+g_{m5}}{g_{mA}^2}\right) + \frac{2K_f}{C_{ox}f}\left(\frac{1}{W_A L_A} + \frac{g_{m5}^2}{g_{mA}^2 W_5 L_5}\right) \tag{3.26}$$

From (3.24), we denote that the noise of the current mirror itself is not affected by the feedback loop, as it can prove to be equal to $(N^2+N)\overline{i_1^2} + N^2\overline{i_{in}^2}$. Also, the feedback circuit contribution to the output current noise has become mainly dependent on the overall input conductance g_{in}. Which brings a trade-off between speed and output noise, as it can be proven using (3.19), (3.20) that when the input impedance increases the maximum speed reachable for a given damping factor decreases.

3.3.4 Illustration through a case study

In the context of high output current application, we have compared the diode-connected, the basic active-input and the adaptive active-input topologies with identical MOS devices. Current mirrors described in this section have been simulated using AMS 0.18 µm CMOS models, under a 1.8 V supply voltage. Transistors of the current mirror have a W/L ratio of 0.7, with $L = 10\,\mu m$. All current mirrors have a copy-ratio of $N = 40$, where the output branch is composed of N transistor equivalent to M1 connected in parallel. The input current ranges from 15 µA to 55 µA, Leading to an output current dynamic of 600 µA to 2.2 mA

For the theoretical calculations displayed in Fig.3.9 (dotted lines), admittance parameters such as C_{11}, g_{21} or g_{22} have been evaluated by simulation with the system biased at minimal

input current, and then extrapolated along the input range. Table 3.4 shows Y-parameters measured at $I_{IN} = 15\,\mu A$ for the proposed adaptive active-input current mirror. Numerical results give for the initial OTA gain a value of $g_{m2min} = 0.9\,\mu A\,V^{-1}$. Which has been achieved with an OTA bias current of 0.3 µA and a common-source amplifier bias current of 1 µA.

TABLE 3.4 – Simulated admittance parameters at $I_{IN} = 15\,\mu A$.

g_{21} (µA V^{-1})	C_{11} (pF)	C_{12} (fF)	C_{21} (pF)	C_{22} (fF)	g_{22} (nA V^{-1})
67.1	16.5	16.4	0.15	9.7	445.1

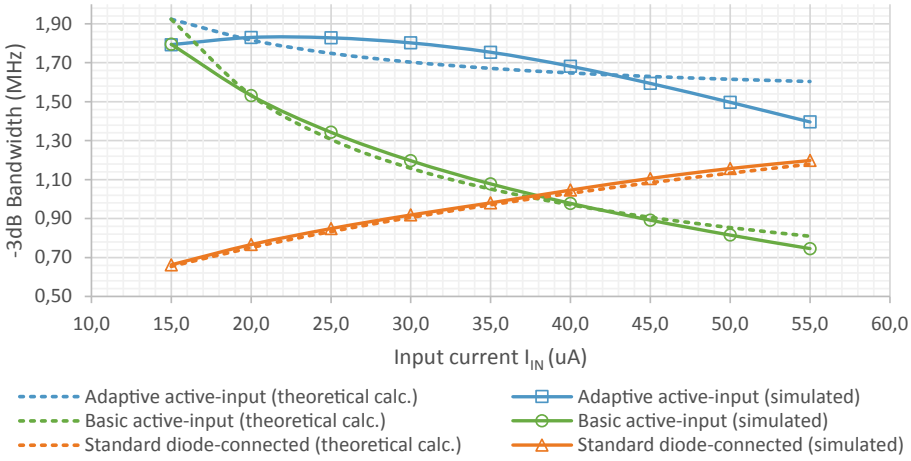


FIGURE 3.9 – Cut-off frequencies versus input currents for the three compared types of current mirror

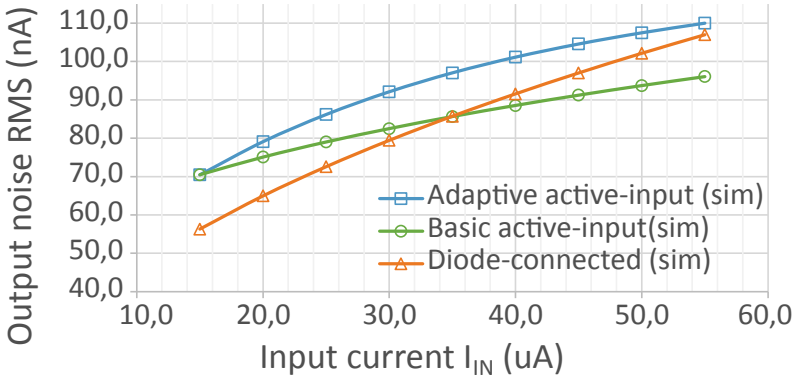


FIGURE 3.10 – RMS value of output noise versus input currents. PSD integrated from 1 Hz to 20 MHz

Simulated −3 dB bandwidth and total RMS output noise for the three compared types of current mirror, shown in Fig 3.9 and 3.10, correlates with the theoretical predictions. In our case study example, whereas the basic active-input exhibits a poorer speed than the equivalent diode-connected within the upper half input current range (35 µA to 55 µA), speed of the proposed adaptive active-input is kept higher all over the input range at solely the price of two additional MOS devices and an extra bias current. In addition, the proposed solution has negligible impact on noise and differences observed in Fig. 3.10 essentially relate to differences in system bandwidth values.

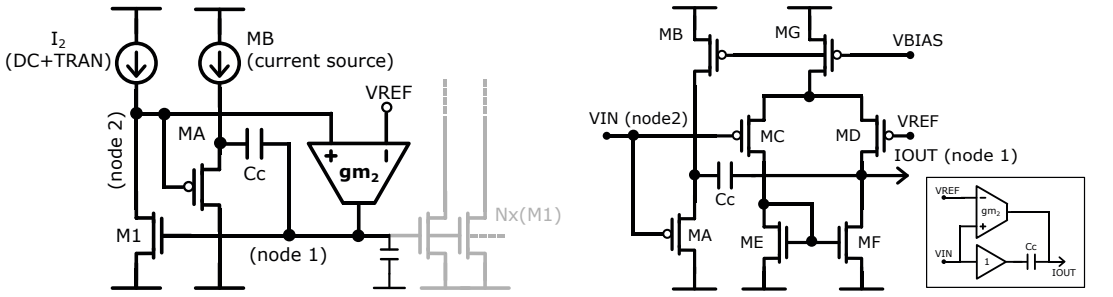
Here, we have seen that adaptive biasing is a low-cost solution that improve the dynamic current range of active-input current mirrors. However, the proposed structure do not address the stability issue and its sensitivity to device output conductance which is found to be the major limitation. This is the topic of the following section.

3.4 The stabilized active-input structure

In this section we present, a stabilized version of the active-input topology (Fig. 3.11a) which solves the previously found constricting stability issue and offers larger bandwidth for few additional MOS devices and dedicated bias current. Introduction to the structure comes with a dedicated formalism intended to achieve the best speed-power performance when designing stabilized active-input current mirror. Like the standard active-input topology, its stabilized version can also be combined with simple or improved cascode techniques.

In its basic form, the stabilized feedback loop (Fig. 3.11b) comprises, a standard 5-devices OTA increasing the apparent input gm, a compensation capacitance acting as a derivative control for more stability margin and a source follower placed between the mirror drain and the capacitance. The source follower is here to de-symmetrize the current path, allowing to control the zero of the closed loop system induced by the compensation capacitance (Razavi, 2001), while avoiding an excessive load of the mirror input, which would have neutralized the OTA effect.

Relying on a dominant pole compensation method, this stabilized feedback loop is used to further extend the bandwidth with speed limitations no longer related to the MOS device first order characteristics (C_{gs}, g_m), but dominated by the DC power possibly dedicated to meet our target speed.



(A) Simpified schematic (B) Proposed feedback loop implementation

FIGURE 3.11 – Stabilized active-input current mirror

3.4.1 System modelling and stability study

The current mirror input branch is again modelled by its admittance matrix:

$$Y_{CM} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} = \begin{bmatrix} g_{11} + C_{11}s & g_{12} - C_{12}s \\ g_{21} - C_{21}s & g_{22} + C_{22}s \end{bmatrix} \tag{3.27}$$

Components C_{11}, C_{22}, g_{22}, g_{21} model respectively the total gate-to-ground capacitance, the overall drain-to-ground capacitance, the overall output conductance of the input branch and the input MOS transconductance. The gate-drain capacitance is represented by C_{21} for gate voltage variations and by C_{12} for drain voltage variations.

In the following sections, the indices $_{\text{ai}}$ (active-input) will refer to the system shown in Fig. 3.11a. Concerning the feedback circuit, g_{m2} and C_C represent respectively the OTA gain and the compensation capacitance value. These are the design parameters we want to evaluate. From the corresponding small-signal model introduced Fig. 3.12, we can derive the transimpedance function of the stabilized active-input mirror:

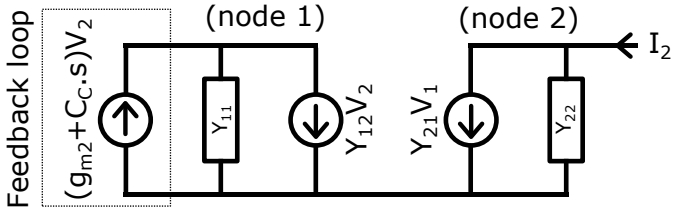


FIGURE 3.12 – Small signal model of the stabilized active-input current mirror

$$\left(\frac{V_1}{I_2}\right)_{\text{ai}} = G\frac{1+\frac{s}{\omega_1}}{1+2m\frac{s}{\omega_{\text{ai}}}+\frac{s^2}{\omega_{\text{ai}}^2}} \tag{3.28}$$

$$\omega_1 = \frac{g_{m2}-g_{12}}{C_C+C_{12}} \qquad \omega_{\text{ai}}^2 = \frac{g_{11}g_{22}+g_{21}(g_{m2}-g_{12})}{C_{11}C_{22}-C_{21}(C_C+C_{12})} \tag{3.29}$$

$$\frac{2m}{\omega_{\text{ai}}} = \frac{g_{22}C_{11}+g_{11}C_{22}+g_{21}(C_C+C_{12})-C_{21}(g_{m2}-g_{12})}{g_{11}g_{22}+g_{21}(g_{m2}-g_{12})} \tag{3.30}$$

For a system to remain stable, the real parts of all poles in its transfer functions have to be negative. Thus, from the transimpedance transfer function, stability conditions are derived and express as:

$$g_{m2} > \frac{g_{21}g_{12}-g_{22}g_{11}}{g_{21}} \qquad C_C+C_{12} < \frac{C_{11}C_{22}}{C_{21}} \tag{3.31}$$

$$g_{m2} < \frac{g_{22}C_{11}+g_{11}C_{22}+g_{21}(C_C+C_{12})+g_{12}C_{21}}{C_{21}} \tag{3.32}$$

Ensuring g_{m2} and C_C values respect the conditions above will keep the system in its stability domain. We observe that larger C_C values increase the possible upper value for g_{m2} and consequently increase the potential maximum speed .

Here we are interested in determining the OTA gain (g_{m2}) and the compensation capacitance value (C_C) to achieve the desired frequency behaviour. Y-parameters such as C_{11}, g_{21} or g_{22}, directly related to MOS device sizes and bias, have been initially determined from static performances optimization. Thus, to simplify calculation steps and result interpretations, we chose to reduce the problem in a two-dimensional space. Let us use the previous stability conditions in (3.31) and (3.32), to define two new variables, x and y, respectively linked to C_C and g_{m2} as:

$$x = \frac{(C_C + C_{12})C_{21}}{C_{11}C_{22}} \tag{3.33}$$

$$y = \frac{C_{21}}{g_{21}}\left(\frac{(g_{m2} - g_{12})C_{21}}{C_{11}C_{22}} - \frac{g_{11}}{C_{11}} - \frac{g_{22}}{C_{22}}\right) \tag{3.34}$$

The stability domain boundaries become:

$$x < 1 \quad \text{and} \quad y < x \quad \text{and} \quad y > y_{min} \tag{3.35}$$

Fig. 3.13 shows its graphical representation of this new domain. As the system has been normalised through x and y, this abacus is valid for many considered current mirror with topology coupled with the stabilized active-input. Let us define four more parameters, representing the inherent pole pulsations for each current path:

$$\omega_R = \frac{g_{21}}{C_{21}} \quad \omega_{IN} = \frac{g_{22}}{C_{22}} \quad \omega_{OUT} = \frac{g_{11}}{C_{11}} \tag{3.36}$$

$$\omega_P = \omega_R(\omega_{IN} + \omega_{OUT}) + \omega_{IN}\omega_{OUT} \tag{3.37}$$

We obtain a new expression of the system transimpedance function (eq. 3.28):

$$\left(\frac{V_1}{I_2}\right)_{\text{ai}} = G\frac{1 + \frac{s}{\omega_1}}{1 + 2m\frac{s}{\omega_{\text{ai}}} + \frac{s^2}{\omega_{\text{ai}}^2}} \tag{3.38}$$

$$\omega_1 = \frac{y\,\omega_R + \omega_{IN} + \omega_{OUT}}{x} \tag{3.39}$$

$$\omega_{\text{ai}}^2 = \frac{y\,\omega_R^2 + \omega_P}{1 - x} \qquad \frac{2m}{\omega_{\text{ai}}} = \frac{(x - y)\,\omega_R}{y\,\omega_R^2 + \omega_P} \tag{3.40}$$

Eventually, the final bandwidth and step-response characteristics, such as the overshoot or the amount of pseudo-oscillation, are defined by the absolute values of x and y, but also to their relative positions on the (x, y) plane. Again, we want the system behaving like the basic diode-connected current mirror, to preserve its use as fundamental analog element. So, no overshoot neither oscillations are tolerated in the final response.

We decide to address the case of an over-damped system ($m > 1$) where the dominant pole is compensated by the zero in the transimpedance function (eq. 3.28). In this case, the current mirror is expected to act as a low–pass 1st order system. Thus, we need to find a relation between x and y such that $z_1 = p_1$, where p_1 is expressed as $p_1 = \omega_{ai}(-m + \sqrt{m^2 - 1})$ and $z_1 = -\omega_1$. Using equations (3.39) and (3.40), we obtain the relation:

$$x\,\omega_{IN} - y\,\omega_R = \omega_{IN} + \omega_{OUT} \tag{3.41}$$

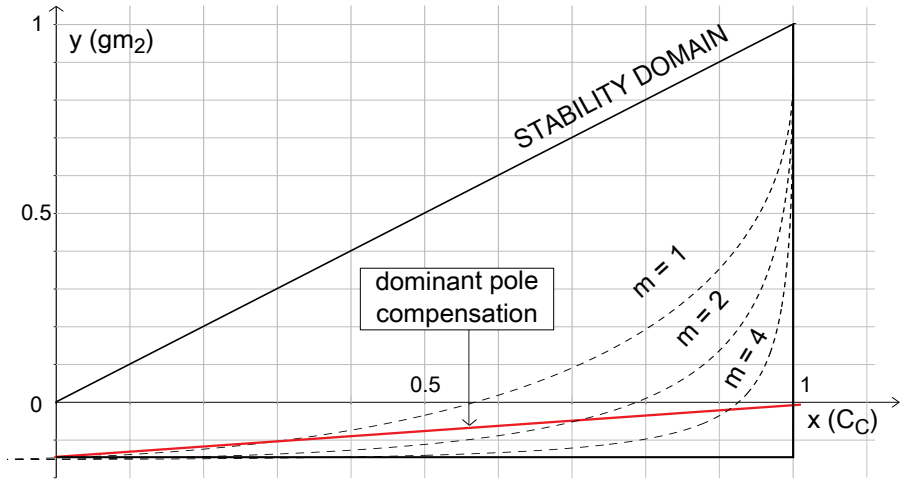


FIGURE 3.13 – Graphical representation of system operation

Every $\{x, y\}$ couple verifying relation (3.41), will ensure the dominant-pole compensation ($z_1 = p_1$). Hence, the resulting bandwidth is fixed by their absolute values and expresses as:

$$BW_{\text{ai}} = \frac{\omega_{\text{ai}}(m + \sqrt{m^2 - 1})}{2\pi} \tag{3.42}$$

Where corner frequency and damping factor can be defined as functions of x only:

$$\omega_{\text{ai}} = \sqrt{\frac{x\,\omega_R\omega_{IN} + \omega_{IN}\omega_{OUT}}{1 - x}} \tag{3.43}$$

$$m = \frac{1}{2}\frac{x\,(\omega_R - \omega_{IN}) + \omega_{IN} + \omega_{OUT}}{\sqrt{(1 - x)\,(x\,\omega_R\omega_{IN} + \omega_{IN}\omega_{OUT})}} \tag{3.44}$$

The more x is moving towards 1, the more the system is going faster, but at the price of larger values for the OTA gain and compensation capacitance. Within the stability domain, there will always be a $\{x, y\}$ pair, or more precisely, a $\{C_C, g_{m2}\}$ pair which verifies the relation 3.41, for any pulsation ω_{ai} (or any m factor). Thus for the linear model defined in figure 3.12, the final system bandwidth can be extended with no upper limit.

3.4.2 Next limitations with more realistic feedback circuits

As demonstrated in the previous section, the way we model and tune our system gives an unlimited bandwidth enhancement. In practice, the challenge remains in the feedback loop design. To meet our speed goal, we have to ensure sufficient transconductance and bandwidth for the OTA and the source follower, which strongly depends on the dedicated bias currents. In other words, the higher the speed is, the more it costs in extra power consumption. In this section, a numerical solution is proposed to determine optimal values for the compensation capacitance (C_C) and the OTA gain (g_{m2}), according to power and/or speed objectives.

The following equations are used to compute, at any given x value (which relates to C_C), the final bandwidth BW_{ai} and an estimation of the extra bias current $I_{FB} = I_{\text{OTA}} + I_{\text{FOL}}$

required by the feedback circuit to ensure it. If we know x, we can deduce C_C and then g_{m2}, to finally link them with feedback bias current and final bandwidth.

The feedback circuit considered is shown in Fig. 3.11b. We assume all MOS devices are on the edge of the strong inversion, giving a V_{eff} of 200 mV and a maximum g_m/I_D ratio of 10 (for a differential pair $g_m/I_{bias} = 5$). Then OTA bias current source follower bandwidth can be estimated by:

$$I_{\mathrm{OTA}}(x) \approx 0.2 g_{m2}(x) \qquad BW_{\mathrm{FOL}} \approx \frac{g_{mFOL}}{2\pi(C_{gsFOL} + C_C)} \approx \frac{5 I_{\mathrm{FOL}}}{\pi(C_{gsFOL} + C_C)} \tag{3.45}$$

With $C_{gsFOL} \ll C_C$, since MOS devices are taken with minimal length to avoid excessive capacitive load of the current mirror input.

When the loop is closed the main pole of the source follower introduces a zero in the system transimpedance function which may leads to undesired overshoot. With $BW_{\mathrm{FOL}} = 10 BW_{\mathrm{ai}}$ the zero has no significant influence on the system response. With $BW_{\mathrm{FOL}} = 5 BW_{\mathrm{ai}}$, we are ensuring that no overshoot occurs with a zero still close enough to slow down the gain cut-off. Then in this last case, bias current for the source follower is estimated as:

$$I_{\mathrm{FOL}}(x) = \pi BW_{\mathrm{ai}}(x) C_C(x) \tag{3.46}$$

To finally compute or plot bandwidths and bias currents versus x, we now need to derive $C_C(x)$ from (3.33), $g_{m2}(x)$ from (3.34) and (3.41) and $BW_{\mathrm{ai}}(x)$ from (3.42), (3.43) and (3.44). An example based on a graphical resolution is presented in section 3.4.3.

Noise introduced by the OTA differential pair, the source follower, the current mirror devices and the input source are denoted respectively $\overline{v_{diff}^2}$, $\overline{v_{fol}^2}$, $\overline{i_1^2}(\omega)$ and $\overline{i_{in}^2}$. When considering both thermal and flicker noise sources, the total output noise current is approximated by:

$$\overline{i_{out}^2} \approx (N^2 + N)\overline{i_1^2} + N^2 \overline{i_{in}^2} + \frac{(g_{22} N)^2}{g_{m2}^2 + C_C^2 \omega^2} \left(g_{m2}^2 \overline{v_{diff}^2} + C_C^2 \omega^2 \overline{v_{fol}^2} \right) \tag{3.47}$$

From equation above, we note that the noise of the current mirror itself is not affected by the feedback loop, as it can be proven to be equal to $(N^2 + N)\overline{i_1^2} + N^2 \overline{i_{in}^2}$. With N being the number of output branches in parallel. Moreover, the noise introduced by the feedback, at low frequency, is dominated by the noise generated by the OTA differential pair. Thus, the solution proposed to stabilise the active-input topology has little effect on output noise level when compared to the standard active-input.

3.4.3 Illustration through a case study

In this section, numerical results and simulated frequency responses illustrate the validity and advantages of the calculation flow. In the context of high output current application, we have compared the stabilized active-input and the diode-connected topology with identical MOS devices.

Current mirrors described in this section have been simulated using the AMS 0.18 µm CMOS models, under a 1.8 V supply voltage. Transistors of the current mirror have a W/L ratio of 0.7, with $L = 10\,\mu m$. The input DC current for biasing is for both cases 10 µA, leading to a $V_{eff} = 350\,mV$. This operating point gives, for the diode-connected mirror, a standard deviation for the mismatch-induced copy error of 0.21 % (obtained with 200 runs in monte-carlo simulation). These current mirrors will be considered with 20 output branches, giving a DC output current of 200 µA.

Using the equations introduced in section 3.4.2, the graph in Fig. 3.14 compares possible target bandwidths with related minimal bias currents required for the feedback circuit. Finally, with a bias current $I_{FB} \approx 13\,\mu A$ (5 % of the output DC current), we can achieve a bandwidth of about 20 MHz, which corresponds to an x value of 0.25. Then with a correct Y-matrix extraction, feedback circuit parameters g_{m2} and C_C are derived using (3.34), (3.41) and (3.33). Starting with $V_{eff} = 200\,mV$ and minimal lengths for MOS devices in the source follower, we have all the elements to design the feedback circuit.

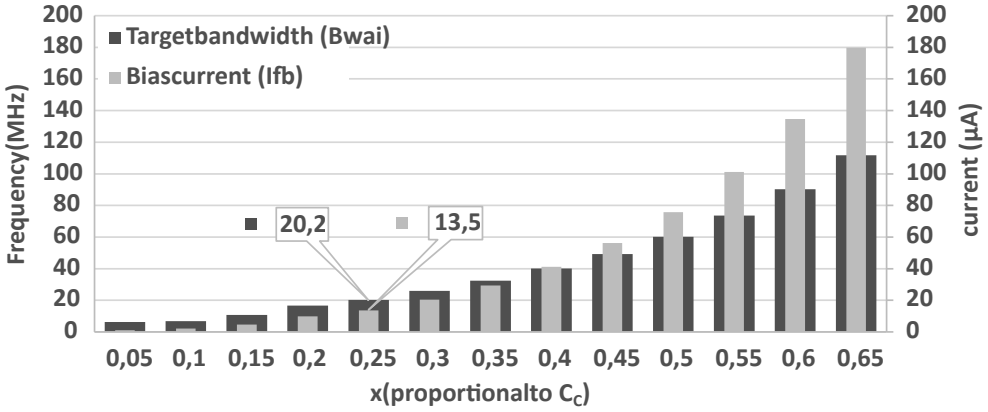


FIGURE 3.14 – Target bandwidth and feedback bias current versus x ($\propto C_C$)

Fig. 3.15 shows simulated frequency response of the current mirror gain (copy-ratio) for the diode-connected current mirror and for the stabilized active-input current mirror. Initially, the diode-connected current mirror had a bandwidth of 1 MHz. The stabilized active-input current mirror, simulated with ideal feedback, shows a bandwidth of 22 MHz which is close to the predicted values of 20 MHz, given Table 3.5. As we notice in Fig. 3.15, the stabilized active-input current mirror shows higher bandwidth (37 MHz) when the feedback circuit is actually implemented with real components. The reason resides in the influence of the zero introduced by the source follower. We placed this zero close enough to the system cut-off to slow down a bit the phase rotation, winning several MHz on the overall bandwidth while saving bias current for the source-follower.

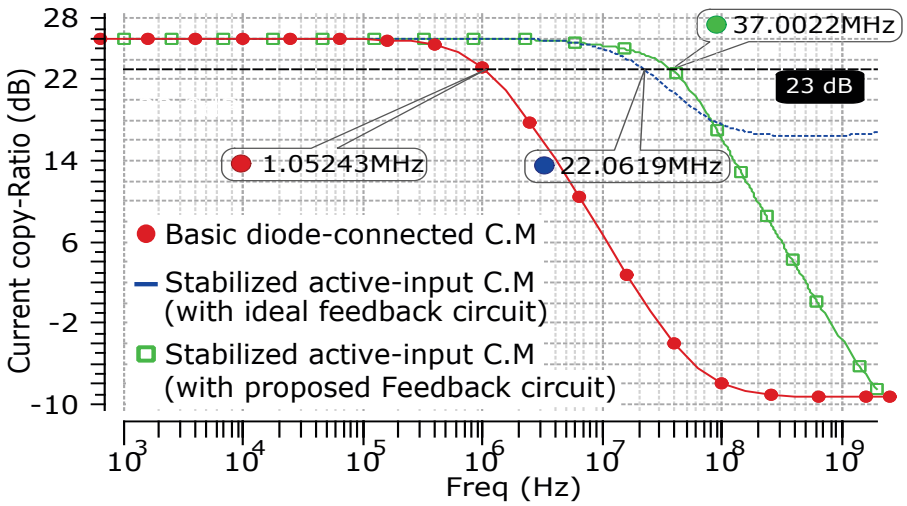


FIGURE 3.15 – Simulated bandwidth for the diode-connected and the stabilized active-input current mirrors

TABLE 3.5 – Theoretical calculation results

x	C_C	C_{gsFOL}	y	g_{m2}	I_{OTA}	I_{FOL}	BW_{ai}
0.25	160	0.5	−0.082	6.3	1.4	12.3	20.2
–	fF	fF	–	µA/V	µA	µA	MHz

From noise simulation, we measure for the stabilized active-input structure, output noise current values of 836 pA/$\sqrt{\text{Hz}}$ and 18 pA/$\sqrt{\text{Hz}}$ at respectively 10 Hz and 1 MHz, whereas the diode-connected current mirror shows values of 185 pA/$\sqrt{\text{Hz}}$ and 3 pA/$\sqrt{\text{Hz}}$ at the same frequencies.

3.5 Conclusion

One of the first contribution of our research work is a dedicated formalism for the design of standard active-input current mirrors. Although the active-input topology has been used in different practical implementations, as far we know, none of previous related work have proposed analytical tools to study and optimize the speed-power ratio in the standard active-input topology . Analytical expressions and calculation flow developed in 3.2 have been used to characterize and quantify the potential speed improvement offered by such structures. The results of this study show that, it is indeed possible to increase the speed of a current with minimum impact on the power consumption, by using linear OTA-based feedback on the input branch. Thus, under certain conditions, the standard active-input topology can effectively relax the *speed-power-accuracy trade-off*. However we have observed several limitations, not related to the power budget, which restrain the speed range and the type of response we can achieve.

The first limitation appears when we require the current mirror to operate on a large input current range. Large input current variation causes a significant variation of the mirroring device operating point and consequently implies a modification of their intrinsic characteristics (i.e g_m or r_{ds}). In the standard active-input topology, the feedback loop gain

is fixed, a shift in the operating point results in a detuned feedback. The consequences are either a degraded speed or the occurrence of pseudo-oscillations or overshoot. In section 3.3, we have proposed a modification of the feedback circuit, that makes the feedback gain dependent on the operating point thanks to an adaptive biasing scheme for the OTA. This solution ensure the speed improvement of the standard active-input solution over a wider input current range.

The main limitation concerns the stability condition of such structure that strongly constraints the maximum speed we can achieve. In addition, we have seen that this stability condition mainly depends on intrinsic device characteristics, such as r_{ds}, that reduce the degree of freedom we have to tune the system. In section 3.3, we have proposed a stabilized version of the active-input topology that enlarges the stability domain at minimal cost and thus enlarges the range of possible speeds. The CMOS implementation is supported by a dedicated formalism and a design method for optimal system tuning according to speed, power and accuracy objectives. Conclusions of the study show that significant speed improvement with minimal impact on power consumption can be achieve thanks to the stabilized version. In addition we have shown that with this solution, at first order, the stability domain is no longer related to device characteristics but to the bias current level dedicated to the feedback circuit.

Even though, we have demonstrated the benefits of the discussed active-input topologies to the design of fast, precise and power-efficient current sources, the constricting nature of the limits highlighted was a sufficient motivation to further investigate new form of control loops. The development of a new design approach for active current mirror, based on non-linear feedback and current-mode components is the topic of the next chapter.

Chapter 4

Design of fast precise and accurate current mirror using non-linear current-mode feedback circuits

In Chapter 3 we have presented active topologies based on voltage-input current-output linear feedback circuit. But the physical quantity which serves as setpoint for input regulated current mirrors is a current. Thus, for voltage-input feedback circuits (i.e OTA or OPAMP) to sense variation of this reference current, it has to be converted to a voltage variation. The conversion is done across the mirror input impedance. The closed-loop behaviour become mainly dependant on its value and this constitutes the main limitation of the active-input techniques presented so far.

In this chapter the reader will be introduced to a novel approach to design active current mirrors. Dedicated types of feedback circuits are investigated with main focus on speed enhancement, power consumption reduction and accuracy improvement. The study comes through with a proposition of a high performance current mirror architecture based on a non-linear current-mode feedback which will be used as a new competitive architecture for current source and current driver design.

4.1 From voltage-mode to current-mode feedback

In this first section, we will see what are the effective advantages of a current-mode feedback compared to a voltage-mode feedbacks, and what solutions we have for its CMOS implementation.

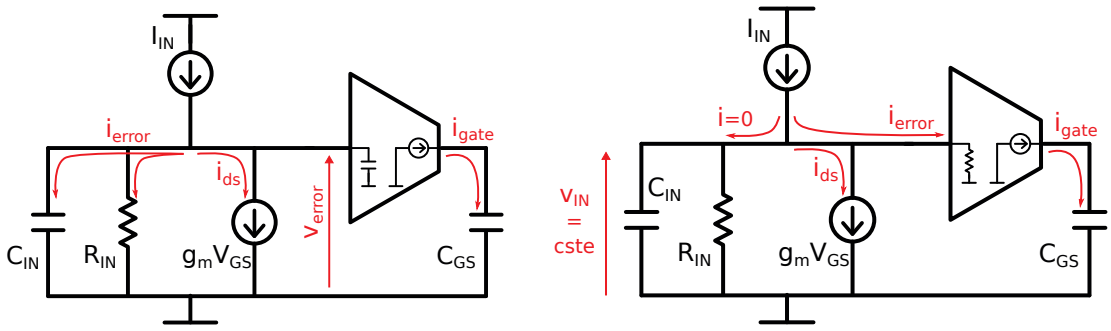
4.1.1 Advantages of current-input current-output feedback

Firstly, in previous structures the mirror input impedance is defined by the output impedance of devices composing the current mirror, which have been already fixed by sizes and polarizations applied to meet target static performances. Input impedance of OTAs or OPAMPs are purely capacitive and thus considered as infinite at low frequencies. In addition, large device output impedance helps to reduce current errors due to v_{DS}-modulation effect. But as previously discussed, this also reduce the bandwidth improvement

capabilities of such active-input topology. Indeed, proper operation is ensured when the pole on the current mirror gates is largely dominant. An increase of the current mirror input impedance brings the pole on the input towards lower frequencies. Unfortunately, two close low frequency (or high-impedance) poles in a closed loop system lead to oscillatory response.

Unlike transconductance or voltage amplifiers, current-mode circuits (i.e. current amplifiers/conveyor) are components with low-input impedance capable to absorb current with minimal variation of their input voltage. The Fig. 4.1 illustrates how the use of current-mode circuits changes the feedback nature and more specifically the nature of the error quantity the closed-loop system attempts to cancel. In this illustration, for both cases, the system reaches his steady state when the input current I_{IN} is equals to the current i_{ds} absorbed by the current mirror. The feedback tends to nullify the difference between the two. To measure this difference, a current-mode feedback absorbs the error current and provides an amplified image, whereas a voltage-mode feedback requires a conversion of this error from current to voltage domain before acting.

Eventually, the use of current-mode components in place of the OTA should improve the current mirror input compliance and push the input pole towards higher frequencies for wider stability domain and better speed. This presumption will be confirmed in section 4.2.



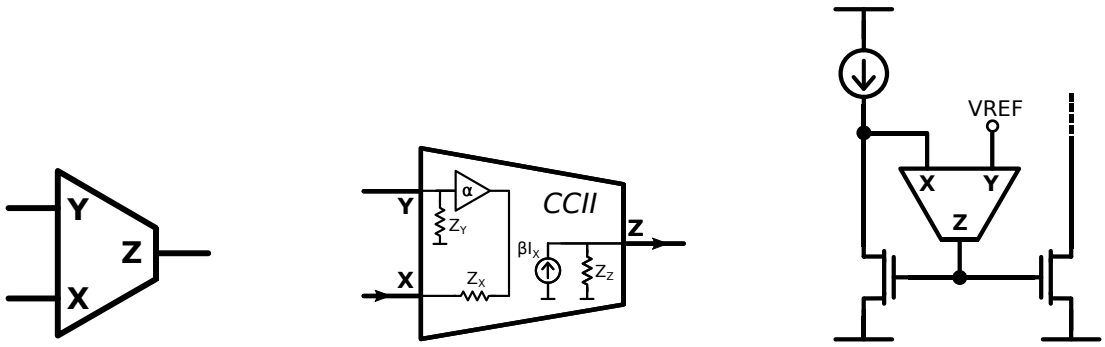
(A) With transconductance amplifier (B) With current amplifier

FIGURE 4.1 – Simplified view of differences between voltage-mode and current-mode feedback

4.1.2 Feedback implementation using standard CCII

One of the most popular current-mode component is the second-generation current conveyor (CCII) which was first published by A. Sedra in 1970 (Sedra and Smith, 1970). Basically, a CCII is a low input impedance current amplifier with input voltage regulated. Its symbol and equivalent circuit are given Fig. 4.2.

Input current is applied on node X, the amplified current copy flows through output node Z. Voltage applied on terminal Y fixes the voltage level of node X. The parameter α represents the voltage gain between nodes Y and X. α is typically close to 1. The current amplification is characterized by the value of β, so that $I_Z = \beta I_X$. Parameters Z_X, Z_Y and Z_Z represent the impedance seen at each nodes. Ideally we have:



(A) Symbol (B) Equivalent circuit (C) Use for active CM

FIGURE 4.2 – Standard CCII with current mirror

Terminal	Impedance	Type
X	$Z_X \approx 0$	mainly resistive
Y	$Z_Y \approx \infty$	mainly capacitive
Z	$Z_Z \approx \infty$	mainly resistive

In the same way as what have been done to study dynamic behaviour of previous current mirrors, we can represent the CCII by the small-signal admittance matrix defined in (4.1). For the expression of the transimpedance transfer function of the simple CCII-based active current mirror shown Fig. 4.2c, the CCII admittance matrix is seen in parallel with the admittance matrix of the current mirror itself (4.2). Here, for the sake of simplicity we have made the approximation that gate-to-drain capacitance in the current mirror are neglected. According to previous definition of the current mirror admittance matrix (see 2.2), that means that parameters $y_{12} = 0$ and y_{21} only represents the transconductance factor. The parameter y_{11} accounts for the overall gate-to-source capacitance Its value depends on the number of devices in parallel. In the current conveyor admittance matrix Y_{CCII}, parameters g_X and g_Z model respectively the input and output conductance at terminals X and Z. Node 1 of the current mirror is connected with node Z, node 2 is connected with node X.

$$Y_{CCII} = \begin{bmatrix} g_Z & \beta g_X \\ 0 & g_X \end{bmatrix} \qquad (4.1) \qquad\qquad Y_{CM} = \begin{bmatrix} C_{GS}s & 0 \\ g_m & g_{DS} + C_{DS}s \end{bmatrix} \qquad (4.2)$$

With the convention:

$$\begin{bmatrix} I_Z \\ I_X \end{bmatrix} = Y_{CCII} \begin{bmatrix} V_Z \\ V_X \end{bmatrix} \qquad (4.3) \qquad\qquad \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = Y_{CM} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \qquad (4.4)$$

According to these assumptions, Table 4.1 gives the transfer function V_{GATE}/I_{IN} of the standard active-input discussed in Chapter 2 (g_{m2} is the OTA gain) and the transfer function of the CCII-based active current mirror shown in Fig. 4.2c. These expressions

are largely approximated and are used here for primary interpretation and comparison. A more accurate model for the CCII-based solution will be presented later in section 4.2.

OTA-based active-input CM	
$\left(\frac{V_{gs}}{I_{IN}}\right)_{\text{ota}} = G_{\text{ota}} \frac{1}{1 + 2m_{\text{ota}}\frac{s}{\omega_{\text{ota}}} + \frac{s^2}{\omega_{\text{ota}}^2}}$	$\omega_{\text{ota}}^2 = \frac{g_m g_{m2}}{C_{GS} C_{DS}}$ $m_{\text{ota}} = \frac{1}{2}\sqrt{\frac{C_{GS}}{g_m C_{DS}}}\sqrt{\frac{g_{DS}^2}{g_{m2}}}$ $G_{\text{ota}} \approx \frac{1}{g_m}$
CCII-based active-input CM	
$\left(\frac{V_{gs}}{I_{IN}}\right)_{\text{cc}} = G_{\text{cc}} \frac{1}{1 + 2m_{\text{cc}}\frac{s}{\omega_{\text{cc}}} + \frac{s^2}{\omega_{\text{cc}}^2}}$	$\omega_{\text{cc}}^2 = \frac{\beta g_X g_m}{C_{GS} C_{DS}}$ $m_{\text{cc}} = \frac{1}{2}\sqrt{\frac{C_{GS}}{g_m C_{DS}}}\sqrt{\frac{g_X}{\beta}}$ $G_{\text{cc}} = \frac{\beta}{\beta g_m + g_Z} \approx \frac{1}{g_m}$
Approximations:	
$\beta > 1$, $g_X \approx g_m \gg g_Z \approx g_{ds}$ and $C_{GS} \gg C_D$	

TABLE 4.1 – Transimpedance transfer function for OTA-based and CCII-based active-input CM.

Looking at the transfer functions for both systems, the first observation is that for CCII-based solution, there is now two parameters, β and g_X, independent of the current mirror itself, that can be adjusted to set the corner frequency and damping ratio. In OTA-based solution only the OTA gain g_{m2} could be tuned. In addition, whereas the corner frequency ω_{CC} is fixed by the product $\beta \times g_X$, the damping amount is set by the ratio of these two quantities. Derivation of the bandwidth BW_{cc} for the critically damped system ($m_{\text{cc}} = 1$) in equation (4.5) shows that, at first order, speed of CCII-based solution is strictly proportional to the CCII current gain and to the speed of the equivalent diode connected current mirror (BW_{DCO}).

$$BW_{\text{CC}} = \sqrt{\sqrt{2}-1}\frac{\omega_{\text{cc}}}{2\pi} = \frac{2\sqrt{\sqrt{2}-1}}{2\pi}\frac{\beta g_m}{C_{GS}} \approx 1.3\beta BW_{\text{DCO}} \tag{4.5}$$

When the input current changes, difference with the current driven by the MOS is absorbed by the CCII, amplified and injected to the gates of the current mirror. The input drain voltage directly relates to the product of the current absorbed (I_{error} in Fig. 4.1) with the CCII input impedance ($1/g_X$), which can be made very low using class-A topologies similar to Fig 4.3. Current gain β is fixed by the copy-ratio of output current mirrors inside the CCII. Due to the closed loop behaviour, accuracy of the CCII have a low influence on the overall current copy quality. Indeed, as long as we ensure $\beta \times g_m << g_Z$, the transimpedance gain G_{cc} is equal to g_m as expected. Hence the CCII can be build with simple mirrors structures and device lengths close to minimal dimension.

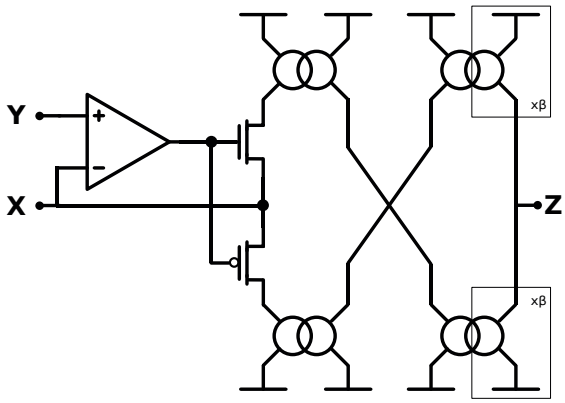


FIGURE 4.3 – Schematic view of a standard class A CCII

4.1.3 Limitations

In their book *Low voltage low power CMOS current conveyors* (Ferri and Guerrini, 2003), G. Ferri *et al.* investigate several implementations of various CCII and propose different design techniques for enhanced input compliance, accuracy or power efficiency. Based on their analysis we designed dedicated current conveyors to validate by simulation the relevance of CCII-based feedback in active current mirror. The conclusions were:

- The speed actually increases linearly with the CCII current gain and gain errors have negligible influence on the current mirror copy accuracy.
- High-speed current mirror requires high-gain CCII but, increasing the gain typically leads to a reduction of the CCII speed. If both speeds are too close to each other, the system may generate undesired overshoot and oscillations.
- The CCII finite output impedance at node Z dissipates current and consequently induces a systematic offset current on the input node X. This current is not driven by the mirroring devices and adds to the overall current copy error.
- This effect can be minimized by using output impedance boosting technique on the CCII output stage, but at the price of higher power consumption.
- For class A and AB current conveyors, an increase of input conductance, speed or current gain necessarily results in a significant increase of static power dissipated

Finally, regarding the *speed-power-accuracy trade-off* the CCII-based feedback offers interesting speed improvement capabilities but input DC offset and static bias current required limit its overall performance. As a result, speed enhancement might cancel the efforts made on the current mirror design itself to minimize consumption and optimize precision.

4.2 Solution for speed-power improvement using a non-linear feedback approach

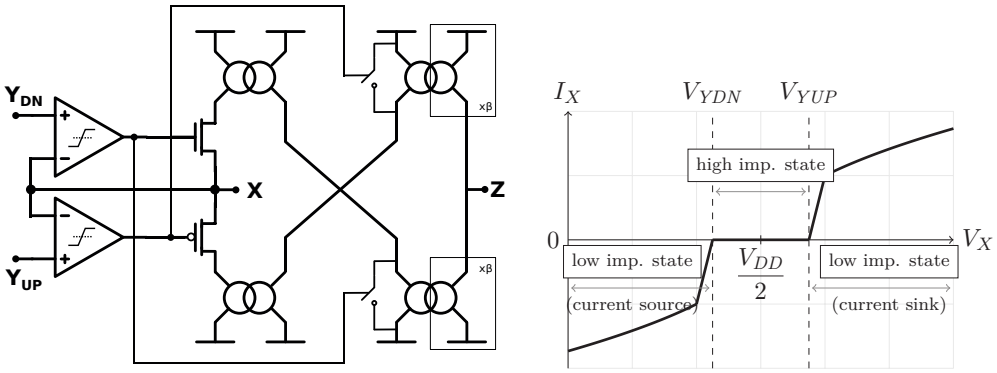
In this section, a design solution for dedicated CCII is proposed to unbind static requirements and dynamic performance of active current mirrors. Higher speed can be achieve

with better power efficiency and minimal impact on current mirror copy accuracy.

Improvement of static performances

As mentioned before, having a low input impedance for the CCII is required to achieve large speed and to keep the system in a stable state during transient response. Previously published work have proposed several techniques to achieve very low-input impedance. The dedicated CCII topology presented below adds the possibility to have a relatively high input impedance once the system reaches its steady state, meaning that a very low current is consumed on the input by the CCII, the DC offset is minimized and so the overall copy error.

To do so, instead of using an opamp-based linear control of the input voltage (Fig 4.3), a bang-bang control is deployed (Fig 4.4a) to switch between low and high input impedance depending on the system state. The switching, based on two comparators, is triggered by the input voltage reaching one of two thresholds located around the expected operating point. Fig 4.4b gives the general shape of the CCII input characteristic to illustrate the operation of the switched input mechanism.



(A) Schematic view (B) Input I-V characteristic

FIGURE 4.4 – Proposed topology for non-linear CCII

Also, the CCII is built with no static bias current. Current mirrors inside, are biased using the current derived on the input during a transient state. This leads to very high output impedance and no static power consumption during steady state.

To summarize, the dynamic behavior comprises two states and the system alternates between the two until it reach its final value. In high impedance state, the input voltage is located in the dead-zone, no current flow through the CCII, the output current does not vary and the input voltage variations depends on the difference between the input current and the actual current driven by the current mirror. In low impedance state, the input voltage is clamped to one of the fixed threshold values, the CCII is now active and the output current evolves towards its final value.

The next section details the proposed CMOS implementation of the non linear CCII-based feedback solution.

4.2.1 Circuit description

Current mirror and current copy

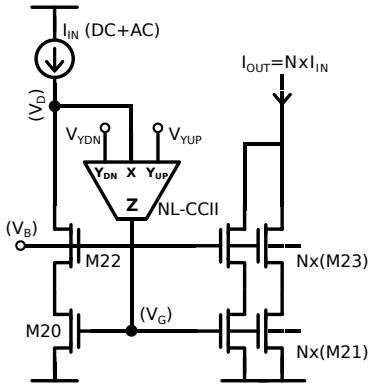


FIGURE 4.5 – High-swing cascode current mirror with non-linear CCII

In Fig. 4.5, transistors M20-M23 compose the cascode current mirror in charge of the input current copy to the output. The W/L ratio is set according to the specified input current and voltage dynamics. In the structure, the input voltage V_D is clamped and varies around a fixed voltage reference. Threshold width and voltage references constrain the drain voltages of M20 and M22. Thus, the current input range relates to: (i) the maximum gate voltage needed to keep M20 saturated according to constraints on drain voltage and (ii) the minimum gate voltage to operate in the strong inversion at minimum input current.

Area of M20 and M21 are defined according to target static precision. Indeed in steady state or DC operation the output error directly relates to matching and noise performance of the current mirror M20-M23. Large area for MOS devices improves the current copy accuracy and the output resistance. In this study, sizes have been defined using a maximum dynamic approach and dedicated matching models given by the manufacturer.

TABLE 4.2 – Transistors sizing in the current mirror

Transistor	W/L (µm)	Transistor	W/L (µm)
M20	29/33	M21	$32 \times (29/33)$
M22	29/0.36	M23	$32 \times (29/0.36)$

CCII non-linear input stage

The input stage (shaded area in Fig. 4.6) is a symmetric structure composed of two complementary single-stage opamps MC-MF and MG-MJ, two MOS switches MA, MB and two diode-connected devices M1, M2. The single stage opamps are designed with large open loop gain and sufficient biasing for sharp edges and fast switching. A large output dynamic for the opamps ensure strong ON and OFF states for MA and MB. Also the way the opamps are connected and the use of complementary switches avoid the simultaneous operation of MA and MB (idem for M1 and M2).The CCII input impedance value depends on the operating regions of MA, MB, M1 and M2, which relate to the input voltage V_D

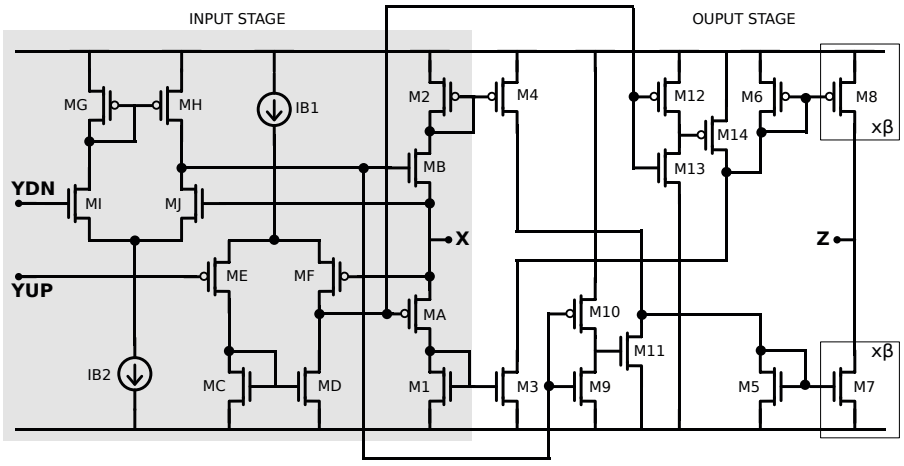


FIGURE 4.6 – Schematic of the proposed non-linear CCII

through the comparators. In the high-impedance state, MA and MB are OFF and the CCII input impedance can be approximated by:

$$\begin{aligned} &g_{Xhz} \approx g_{OFFMA} + r_{OFFMB} \\ &\text{for } V_{YDN} < V_D < V_{YUP} \end{aligned} \tag{4.6}$$

In the low-impedance state, either MA or MB are ON, the input impedance expresses as:

$$\begin{aligned} g_{Xlz} &\approx \frac{1}{r_{ONMA} + 1/g_{mM1}} \quad \text{for } V_D > V_{YUP} \\ g_{Xlz} &\approx \frac{1}{r_{ONMB} + 1/g_{mM2}} \quad \text{for } V_D < V_{YDN} \end{aligned} \tag{4.7}$$

To achieve better stability margin and better speed we search to maximize the value of g_X during the low impedance state. This is done using large channel width for the switches MA, MB and large W/L ratio for M1 and M2. Transistors M1 and M2 can be sized to be in weak inversion for low levels of CCII input current to maximise their transconductance and the CCII input current dynamic.

Because there is no static biasing for these current mirror, the CCII might show significant gain distortion across the full current dynamic, which can lead to detuned feedback. To limit these effects in the proposed implementation characterized section 4.2.3, a high impedance Wilson current mirrors have been used in place of simple current mirrors M1-M3 and M2-M4.

CCII current gain and output stage

The output stage realizes the current inversion and amplification. Ratio of current mirrors M5-M7 and M6-M8 fixes the CCII current gain and, due to the gates connected in parallel, it is assumed to be the slowest internal node of the CCII. Thus transistors M5 to M8

should be taken with length close to minimal dimension to reach large bandwidth when large CCII current gain is needed.

In section 4.2.2, we will demonstrate that the overall dynamic behavior of the system strongly depends on current gain and bandwidth of the CCII. But current flowing through the CCII output stage, is either sinked by an NMOS current mirror (M5-M7) or sourced by a PMOS current mirror (M6-M8), which have different performances. Hence, to obtain a symmetrical structure and have a similar behavior for rising and falling edge, we need to size these current mirrors accordingly. As the gain is mainly fixed by the number of devices in parallel, relation between NMOS and PMOS is such that they have the same speed, ensuring the symmetry of the output stage. In other words, we need $g_{m5} = g_{m6}$ and $C_{gs5} = C_{gs6}$, giving:

$$W_6 = \sqrt{\frac{\mu_N}{\mu_P}} W_5 \qquad L_6 = \sqrt{\frac{\mu_P}{\mu_N}} L_5 \tag{4.8}$$

Eventually, to enforce the switching mechanism, the output node is also quickly turned into high impedance using switches controlled by the same signal used for the input. It ensures that the current stops flowing out the CCII at the same time the input stage goes from low to high impedance state. The duration for the output stage to switch between high and low impedance state mainly depends on the delay of the inverters M9-M10 and M12-M13 and on current capabilities of the shorting devices M11 and M14.

TABLE 4.3 – Transistors sizing in the CCII

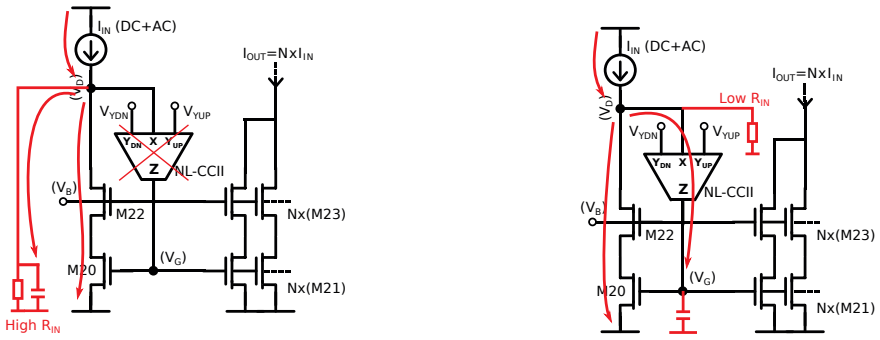
Transistor	W/L (µm)	Transistor	W/L (µm)
M1	0.7/0.18	M2	3.5/0.18
M3	0.7/0.18	M4	3.5/0.18
MA	3/0.18	MB	1/0.18
M5	0.7/0.18	M6	3.5/0.18
M7	0.7/0.18	M8	3.5/0.18
M11	4/0.8	M14	20/0.8

Characterisation results of a non-linear CCII with slight differences are given in Appendix F. The CCII characterized corresponds to the one presented later in section 4.3.3, but it is mentioned here as an illustration of the actual behaviour of such component.

4.2.2 Analysis and design method

This section describes the analysis and a calculation flow dedicated to the implementation of this CCII-based feedback solution according to a behaviour specified by the application. The method is built to reach the maximum speed while respecting the target phase margin all across the input dynamic.

As specified before, this non-linear system comprises two state. An *OFF* state (Fig. 4.7a) where the CCII is in high-impedance and the current mirror gate voltage does not vary. A *ON* state (Fig. 4.7b) where the CCII is active and corrects the gate voltage to follow variations of the input current. In the *OFF* state, the error current I_ϵ, representing the difference between the input current I_{IN} and the saturation current of the mirroring



(A) *OFF state* with CCII in high impedance

(B) *ON state* with CCII in low impedance

FIGURE 4.7 – Schematic view of the current paths in both states

transistor $(K/2)(W/L)V_{EFF}^2$, is low-pass filtered and create the voltage V_D on the input node. By knowing the initial conditions for gate and drain voltages (V_{G0} and V_{D0}) we determine the final value $V_{D\infty}$ with equation (4.9) or either equation (4.10) with large signal parameters.

$$V_{D\infty} = V_{D0} + \frac{I_\epsilon}{g_{ds}} \qquad (4.9) \qquad\qquad V_{D\infty} = \frac{1}{\lambda}\left(\frac{2I_{IN}}{K(W/L)V_{EFF}^2} - 1\right) \qquad (4.10)$$

Here, for an initial value V_{G0} and a given variation of I_{IN} it is possible to determine if the system will leave the *OFF* state. The condition being that $V_{D\infty}$ is located above the upper threshold V_{YUP} or below the lower threshold V_{YDN}. Convergence of V_D towards its final value $V_{D\infty}$ follows a first-order response with a time constant $\tau_D = C_D/g_{ds}$. If the initial conditions are known we can estimate the amount time the system will take to leave the *OFF* state and starts acting on the mirror gate voltage.

However, as mentioned in the previous section, switching from low to high input impedance for the CCII is done for static performances improvement. But here we are principally interested in the dynamic performances and during transient phases The CCII is expected to be predominantly active. Hence in a first place the system dynamic will be treated without considering the high input impedance state. The non-linear input resistance of the CCII $g_X = f(V_D)$ is considered constant and equals to its low value. Performance predictions are done using a linearised model of the system. Impact of the non-linearity is then estimated and timing results refined. As illustrated later in section 4.2.3, this model results in a wrong prediction of the input node voltage evolution. The hypothesis g_X =cste is not realistic. However it offers a an accurate prediction of the gate voltage variation and consequently an accurate prediction of the general dynamic behaviour of the system.

System model

The block diagram Fig. 4.8 is derived from a small signal representation of the system shown in Fig. 4.5. I_ϵ corresponds to the difference between the reference current I_{IN} and the current absorbed by the transistor I_{MOS} at a given moment. A certain amount of I_ϵ is driven by the CCII, the rest charges/discharges the parasitic capacitance on the input node

under the voltage V_D developed across the overall input conductance g_{IN}. Parameters β, g_Z and g_X are respectively the gain, the output conductance and the input conductance of the CCII. $\tau_X = C_D/g_X$, $\tau_Z = C_G/g_Z$ and τ_{CC} represent respectively the time constant on the input drain, the time constant on the current mirror gates and the intrinsic time constant of the CCII ($\tau = C/g_m$). Parameter g_{m20} represents the main current mirror transconductance factor.

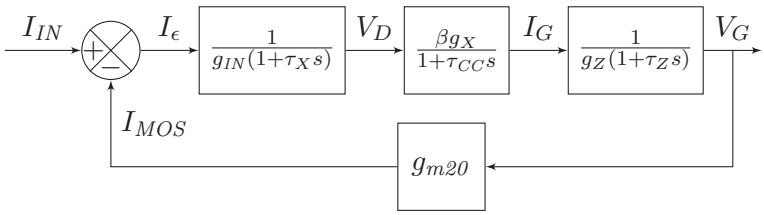


FIGURE 4.8 – Block diagram modelling the CCII-based feedback solution

Using this system model, the open-loop transfer function is derived and expresses as:

$$H_{OL} = \frac{G_{OL}}{(1+\tau_X s)(1+\tau_{CC} s)(1+\tau_Z s)} \tag{4.11}$$

$$G_{OL} = \frac{\beta g_X g_{m20}}{g_{IN} g_Z} \tag{4.12}$$

When the CCII is in the active state, the output conductance of transistor M20 becomes negligible compared to the CCII input conductance and $g_{IN} \approx g_X$

General behaviour set using a linearised system

We distinguish in the open-loop transfer function H_{OL}, three first-order low-pass systems. In most cases, we have concurrently, gate capacitances of the main current mirror much larger than input parasitic capacitances and input conductance g_{IN} much higher than the conductance g_Z found in parallel with the gate capacitances. Then we can assume that $\tau_X \ll \tau_Z$. System response is mainly affected by locations of the dominant pole on the gates (τ_Z) and of the pole representing the finite bandwidth of the CCII (τ_{CC}).

To increase the system speed, we need to increase the open-loop gain G_{OL}, which can be done by increasing the CCII gain β. However, structurally the CCII gain and its time constant are linked and found to be roughly proportional. Hence, to have the desired dynamic behaviour, we need a relation between the CCII gain β, its time constant τ_{CC} and the current mirror parameters. As the time constant τ_{CC} is technology dependant, we will focus on the gain calculation, which can be fully fixed by the designer, for a range of τ_{CC} values.

A phase margin calculation approach is used to compute β according to the expected damping amount. Choosing a specific phase margin PM for the system, implies a fixed relation between gain and time constant for the CCII. Equations (4.13) and (4.14) give the detailed operation used to derive the relation $\beta = f(\tau_{CC})$. This first relation is obtained by calculating the expression of ω_{PM} from (4.13) and injecting the result into (4.14).

$$PM = \pi - \operatorname{atan}(\tau_X \omega_{PM}) - \operatorname{atan}(\tau_Z \omega_{PM}) - \operatorname{atan}(\tau_{CC} \omega_{PM}) \tag{4.13}$$

$$\beta = \frac{g_Z}{g_{m20}} \sqrt{(1 + \tau_X^2 \omega_{PM}^2)(1 + \tau_{CC}^2 \omega_{PM}^2)(1 + \tau_Z^2 \omega_{PM}^2)} \tag{4.14}$$

At this point, for a desired behaviour (damping factor) the maximum CCII gain applicable can be tuned, according to the maximum intrinsic bandwidth of the CCII, feasible with the CMOS technologies used. The next step consists in the derivation of an approximated relation between the gain β and the intrinsic bandwidth ($\omega_{CC} = 1/\tau_{CC}$) for the CCII structure shown in Fig 4.6.

Due to the number of transistors put in parallel to obtain the required current gain, here it is assumed that CCII dominant poles are on the gates of the current mirrors composing the output stage (gate of M5 or M6) . Derivation is given for the case where the CCII is sinking current on the output, the active current mirror is a NMOS type (M5-M7), but the reasoning is identical when current is sourced on the output.

From this assumption, we can write:

$$\omega_{CC} = \frac{g_{m5}}{(1+\beta) C_{gs5}} = \frac{\sqrt{2 K_n \frac{W_5}{L_5} I_X}}{(1+\beta) \frac{2}{3} W_5 L_5 C_{OX}} \tag{4.15}$$

Leading to the second relation $\beta = f(\tau_{CC})$:

$$\beta = \frac{3 \tau_{CC}}{2 C_{OX}} \sqrt{\frac{2 K_n I_X}{W_5 L_5^3}} - 1 \tag{4.16}$$

Eventually the optimum current gain value is derived by calculating the intersection between the curve $\beta = f(\tau_{CC})$ given by the phase margin approach, in eq. (4.13) and (4.14), and the second curve $\beta = f(\tau_{CC})$ derived from design and technology considerations, in eq. (4.16).

In cases where $\tau_X \ll \tau_{CC} < \tau_Z$, the system can be reduced to a second order system and the optimum current gain value can be approximated by (4.17). In this equation τ_{CM} represents the natural time constant (C_{GS}/g_{m20}) of the current mirror with a diode-connected input branch.

$$\beta_{optim}^2 \approx \frac{3 \tau_{CM}}{2 C_{OX} L_5} \sqrt{\frac{2 K_n I_X}{W_5 L_5^3}} \frac{\sqrt{\tan^2(PM) + 1}}{\tan^2(PM)} \tag{4.17}$$

This equation supposes that the CCII is evaluated for a fixed input DC current, whereas in practical application this current will vary from the applied current step magnitude to zero. The CCII worst speed performances are obtained for low level of input current I_X. Then evaluating the device at the minimum step amplitude specified by the application seems to be a reasonable choice to ensure that the system has a phase margin always equals or greater than the one predicted.

Settling time estimation

At this point, characteristics of the current mirror are known and from the method previously introduced we are capable of evaluating characteristics of the CCII, such as its gain, its bandwidth and input conductance, to meet application requirements. The method is built to find the optimal couple of feedback gain and bandwidth to ensure that the system respects the tolerated oscillation amount which is fixed by the desired phase margin. Thus the maximum speed achievable is defined as a consequence of this configuration. One interesting result would be the estimation of speed performances before the final implementation, to easily approve or discard this solution depending on target specifications.

Assuming again that the input time constant is negligible compared to the time constant on the gates of current mirror M20-M23, in short $\tau_X << \tau_Z$, an approximated expression for the closed loop transfer function is derived in (4.18).

$$H_{CL} = \frac{\beta}{g_Z + \beta g_{m20}} \frac{1}{1 + \dfrac{g_Z \tau_Z \tau_{CC}}{g_Z + \beta g_{m20}} s + \dfrac{g_Z (\tau_Z \tau_{CC})}{g_Z + \beta g_{m20}} s^2} \tag{4.18}$$

with the natural pulsation:

$$\omega_n = \sqrt{\frac{g_Z + \beta g_{m20}}{g_Z \tau_Z \tau_{CC}}} \approx \sqrt{\beta \omega_{CC} \omega_{CM}} \tag{4.19}$$

System parameters have been chosen to respect the specified phase margin, which directly relates to the damping factor m. Then, characteristics of the step response can be estimated using classical relation between frequency domain and time domain behaviors. For instance, for a under-damped second order system in the form of (4.18), overshoot O_V and settling time $t_{r\alpha\%}$ are approximated with the following expression:

$$t_{r\alpha\%} = \frac{1}{m\omega_n} \ln\left(\frac{100}{\alpha}\right) \qquad O_{V\%} = 100 \exp \frac{-\pi m}{\sqrt{1 - m^2}} \tag{4.20}$$

Influence of the non-linearity on stop condition and settling time

For a more realistic approximation of the final response we need to consider the influence of the low to high impedance switching of the CCII. Indeed, when the CCII is in high impedance state no current is flowing through and no charges are injected on the gate, the output current does not vary and every cross of the high impedance section will add delay on the settling time.

Also, while the gate voltage come closer to its expected final value, the input drain voltage tends to move forward to the fixed input voltage reference, located between the two activation thresholds. Eventually the input node might enter for the last time in the high impedance section (CCII inactive) and no more charge will be injected in the gate. The system will only stop if residual current error can be absorbed by the MOS device under the influence of its v_{DS}-induced current modulation and the residual input voltage

variation. This implies that v_{DS}-induced errors for the current mirror in the range between the two thresholds have to be lower than the minimum acceptable overall error fixed by the application specifications.

With a CCII designed according to the method above, with a target phase margin greater than 70°, the system is assumed to reach more than 95 % of its expected final value before the first overshoot occurs and more than 99 % after the second. Thus, in first approximation it is reasonable to consider that only the two first crossing of the high impedance state will add significant delay to the 1 % response time. Maximum delay due to the first crossing can be calculated knowing the room between the two thresholds ($V_{YUP} - V_{YDN}$), the input current step amplitude (I_{IN}), the input impedance and pole value while the CCII is in high impedance state (g_{INhz},τ_{Xhz}).

$$D_{CC} = -\tau_{Xhz} \ln\left(\frac{g_{INhz}}{I_{IN}}(V_{YUP} - V_{YDN}) - 1\right) \tag{4.21}$$

4.2.3 Validation and simulation results

In this section, numerical results and simulations illustrate the validity and advantages of the non-linear CCII based feedback and its dedicated calculation flow. Circuits have been simulated using the Cadence Design Environment, and the AMS 0.18 µm CMOS models, under a 1.8 V supply voltage.

The following use case example is designed according to the method presented above. The calculation flow has been scripted and automated using MATLAB. Speed, power and accuracy performances of the proposed current mirror, referred with the subscript $_{cccm}$, are compared to the performances of the classical diode-connected cascode current mirror, referred with the subscript $_{dco}$, with identical MOS devices. We are searching for the maximum speed improvement with target system specifications reported in Table 4.4.

Table 4.4 – target specifications

Minimum input current	5 µA
Target output current range	160 µA to 2500 µA
Target relative output error	0.1 %
Target phase margin	65°

In the following results, transistors of the current mirror M20-M23 have a W/L=0.9, with $L = 33$ µm. These current mirrors will be considered with a copy ratio $N = 32$, resulting in a total gate capacitance of 156.8 pF for the 33 devices in parallel.

According to theoretical calculation flow, the CCII current gain β is set to 11, which is expected to be the maximum gain to respect the 65° phase margin requirement across the input range. NMOS and PMOS comparators of the CCII input stage are both biased with a DC current of 7 µA. The activation thresholds of the non-linear CCII are V_{YDN}=0.7 V and V_{YUP}=1.3 V.

Static precision

Accuracy is evaluated by measuring mean and standard deviation of the relative copy error E_{RR} defined as:

$$E_{RR} = 100 \left| \frac{I_{OUTmeas} - N \times I_{IN}}{N \times I_{IN}} \right| \tag{4.22}$$

System output is loaded by a voltage source set to $V_{DD}/2$ and tested at different input current level. We measure error induced by the mismatch in the current mirror and error due to the feedback circuit also subject to mismatch variation. Influence of v_{DS}-induced modulation on the overall copy error is negligible in this test condition. Indeed, in steady state the CCII is inactive, the input voltage (V_D) has converged to a value located in the range between the two CCII thresholds. The exact value depends on initial conditions but we know that the maximum variation ΔV_D is fixed and $\Delta V_D = (V_{YUP} - V_{YDN})/2 = 0.3\,\mathrm{V}$. On the other hand, thanks to the cascode structure, we measure a DC input impedance $(1/g_{INhz}) > 77\,\mathrm{M\Omega}$ (measured at 1 kHz for $I_{IN} = 60\,\mu\mathrm{A}$). Eventually, we can compute the worst case v_{DS}-induced current error with $\Delta V_D g_{INhz} \approx 4\,\mathrm{nA}$. Compared to the input current it represents a relative current copy error $< 0.04\,\%$. In practice, we observe that for static operating point simulation the input node tends to converge to values close to the CCII upper threshold.

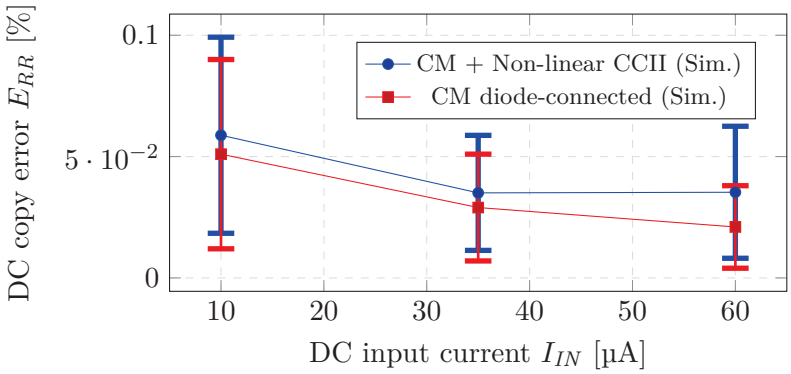


FIGURE 4.9 – Copy error of the proposed circuit and of the diode connected current mirror. Error bars represent the standard deviation (σ) obtained after a 200 runs monte-carlo simulation.

Fig. 4.9 shows copy errors of proposed and equivalent diode-connected current mirrors after a 200 montecarlo runs. The non-linear CCII-based feedback circuit shows limited impact on the DC copy error when compared to the precision of the current mirror itself. This confirms the efficiency of the low to high impedance switching mechanism to reduce the CCII DC offset current.

Settling time

Speed is evaluated by considering the output current settling time at 1 % and 0.4 %. Average values and standard deviations of the settling times are obtained after 200 montecarlo run.

Tables 4.5 and 4.6 show simulated response time for two different step amplitudes: $\pm 1\,\mu\mathrm{A}$ and $\pm 30\,\mu\mathrm{A}$, the last one corresponding to the full input current dynamic. The DC

operating point is fixed in the middle of the input dynamic (I_{INdc} =35 µA), giving a DC output current of 1120 µA and a V_{eff} = 550 mV.

		mean $tr_{1\%}$	std $tr_{1\%}$	mean $tr_{0.4\%}$	std $tr_{0.4\%}$
Rising edge	step ±1 µA	0.216 µs	0.066 µs	0.279 µs	0.097 µs
	step ±30 µA	0.625 µs	0.152 µs	0.727 µs	0.193µs
Falling edge	step ±1 µA	0.238 µs	0.071 µs	0.320 µs	0.115 µs
	step ±30 µA	2.01 µs	0.821 µs	2.35 µs	0.994µs

TABLE 4.5 – Response time of the proposed current mirror

		mean $tr_{1\%}$	std $tr_{1\%}$	mean $tr_{0.4\%}$	std $tr_{0.4\%}$
Rising edge	step ±1 µA	2.71 µs	0.85 µs	4.17 µs	1.30 µs
	step ±30 µA	7.18 µs	1.21 µs	8.62 µs	2.07 µs
Falling edge	step ±1 µA	2.82 µs	0.81 µs	4.28 µs	1.32 µs
	step ±30 µA	27.2 µs	5.98 µs	32.7 µs	6.86 µs

TABLE 4.6 – Response time of the diode-connected cascode current mirror

We observe that the settling time dispersion is affected by mismatch and process variation, in the same proportion for the proposed implementation and for the diode-connected current mirror. Although transistors in the CCII are sized with small area and length close to minimal dimension, dispersion of the feedback circuit seems to have a negligible contribution to the overall speed dispersion. Regarding average values of the settling time, we denote that our structure shows better speed improvement when looking at the time response at 0.4 % than 1 %. This is explained by the non-linear behaviour of the feedback.

Transient responses when both current mirrors are stimulated with a full range step are given in Fig. 4.10. The graph shows both output current and input voltage evolution in response to positive change of the input current (rising edge). The dotted line represents theoretical results derived from the linearised model introduced section 4.2.2 where small signal parameter values have been extracted by simulation at mid-range operation point. Straight lines are results from full Spectre® simulations.

Speed improvement versus power consumption

Figures defined in (4.23) and (4.24) are used to put in relation the speed improvement offered by the proposed feedback circuit with the fraction of extra power it requires to operate.

Static power loss PW_{loss} is defined as the total DC amount of current consumed but not delivered to the load, multiplied by the supply voltage (1.8 V). It comprises the input current I_{IN} and all additional biasing sources. We propose the ratio in (4.23) to evaluate the amount of additional power required by the CCII-based solution to operate.

$$\text{Power Increase} = \frac{PW_{cccm}}{PW_{dco}} = \frac{I_{IN} + I_{B1} + I_{B2}}{I_{IN}} \tag{4.23}$$

Speed improvement is characterized by the ratio of settling times at 0.4 % of the proposed solution over the one of the classical diode-connected cascode current mirror. For instance,

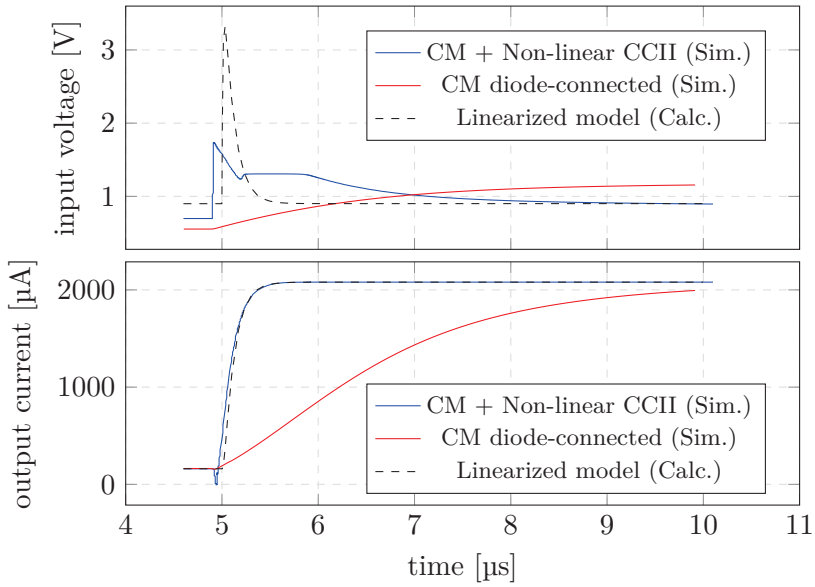


FIGURE 4.10 – Transient Step responses. Dashed lines are results of numerical computation using MATLAB and the linearized system model. Full lines are Spectre® simulation results.

a speed improvement of 10 means that the system has reached its final value in a time interval 10 times lower than the classical current mirror.

$$\text{Speed Improvement} = \frac{tr_{0.4\%,cccm}}{tr_{0.4\%,dco}} \tag{4.24}$$

The bar diagram in Fig. 4.11 compares measured power increase and speed improvement, with the classical cascode current mirror as a reference. Measurement has been done for various DC input current values and various step magnitudes. Correspondences between case names, DC currents and step magnitudes are given table 4.7.

TABLE 4.7 – Measurement case summary

Name	DC input current (µA)	step magnitude (µA)
LowBias-LowStep	5	±1
MidBias-LowStep	35	±1
HighBias-LowStep	65	±1
Fullrange	35	±30

The static power loss ranges from 34 µW at minimum input current (5 µA under 1.8 V) to 142 µW at maximum input current (65 µA under 1.8 V). Regarding the speed improvement against power, using a non-linear CCII based feedback, allows the current mirror to operate faster with a minimal extra power consumption. This solution is specifically efficient for large signal operation. Indeed, while for a step of ±1 µA we measure a speed 12 times higher than the diode-connected current mirror, for a full range step the current mirror operates at a speed 33 times higher with a static power loss increased by a factor of 1.4 only. This amount of static power loss represents 1.3 % of the total DC power consumption

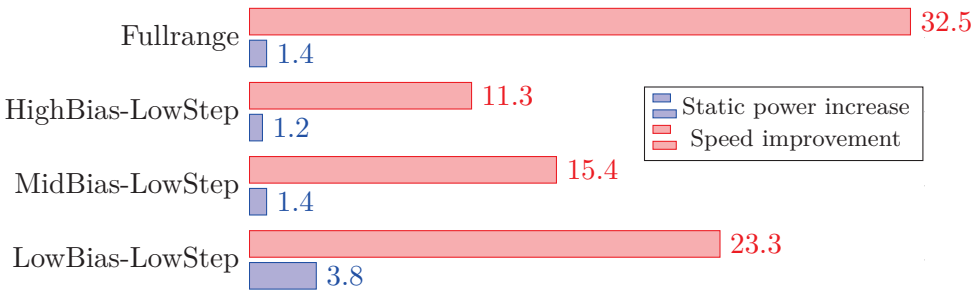


FIGURE 4.11 – Speed improvement compared with static power increase for various input signal (Cf. Table 4.7)

State-of-the-art comparison

Performance comparison with prior work is done in Table 4.8. However, only simulation results are available for the proposed solution whereas most of the work cited presents silicon measurements. Also, as far as we know the topic of high-speed, precise and low-power current sources capable of delivering high output current is slightly treated on its own in the literature, despite the fact that interest for current mode architectures has grown over the past few years.

Hence, strict comparison here is inappropriate and conclusions are subject to silicon validation. Therefore, we can assess that advantage of our solution compared to (Greenwald et al., 2017), (Luo and Ker, 2016), (Sit and Sarpeshkar, 2007) is that, the same order of accuracy and output current level are achieved, but with no need of additional clocked digital circuits. On the other hand, compared to class AB current amplifier and current conveyor presented in (Esparza-Alfaro, Pennisi, et al., 2014) and (Mita, Palumbo, and Pennisi, 2003), our solution achieve similar performances in terms of speed and output level but with better accuracy and lower static power consumption thanks to the low to high impedance switching mechanism of the CCII.

4.2.4 Discussion

The non linear CCII-based feedback and its proposed implementation are optimized for current sources delivering multi-level current pulses. For continuous multi-tonal signals: (i) the distortion (THD) introduced by the non-linear input should be considered. (ii) The dynamic power consumption of the CCII, dependent to the input signal magnitude, should also be considered in the performances evaluation as the CCII will be active most of the time.

When constraints on precision, consumption or output current level are relaxed, the proposed non-linear CCII feedback might become less efficient. Indeed, size of transistors in the current mirror can be reduced, increasing its intrinsic speed. Which can possibly reach a point where the proposed non-linear CCII cannot be made faster due to technological limitation. However, biasing internal nodes of the CCII to operate in class AB can extend its bandwidth and overcome this limitation, but at the price of accuracy and power efficiency reduction.

TABLE 4.8 – State of the art comparison

	This work	(Esparza-Alfaro, Pennisi, et al., 2014)	(Mita, Palumbo, and Pennisi, 2003)	(Palmisano, Palumbo, and Pennisi, 2000)	(Greenwald et al., 2017)	(Luo and Ker, 2016)	(Sit and Sarpeshkar, 2007)	(Lam and Ki, 2008)
Year	2018	2014	2003	2000	2017	2016	2007	2008
Techno.	0.18 µm	0.5 µm	0.35 µm	1.2 µm	0.18 µm	0.18 µm	0.7 µm	0.35 µm
Supply	1.8 V	3.3 V	1.5 V	5 V	3.3 V	12 V	15 V	1.05 V
Maximum output current	2 mA	±0.5 mA	±0.9 mA	±7 mA	0.25 mA	3 mA	1 mA	50 mA
DC current error	0.1 %	-	0.45 %	4.5 µA	0.3 %	0.25 %	0.4 %	-
Settling time	296 ns	138 ns	660 ns	165 ns	-	-	16 µs	< 2 µs
Power consumption	34 µW to 142 µW	280 µW	260 µW	5.5 mW	-	150 µW	47 µW	4 µW to 172 µW
FOM1	85	85	16	80	-	-	20	152
FOM2	850	-	35	-	-	-	52	-
	FOM1 = (Power load / Power Consumption) / (Settling time) [μs^{-1}]							
	FOM2 = (Power load / Power Consumption) / (Settling time × DC error) [μs^{-1}]							

The CCII current gain β can easily be made programmable. It requires the addition of parallel MOS devices on the CCII output stage and small digital control circuit to connect/disconnect them. Programmable gain offers the possibility to, adapt the system to various application requirements, compensate some process variations or tune the cut-off for signal filtering. Programmable gain can be combined with programmable current mirror copy ratio for more versatility.

The last remark concerns phenomenons that may occur in the dead-zone during which the current mirror is in open loop and the gate voltage memorized until the next CCII activation. In steady state, the CCII is built to be in high-impedance state meaning that the current driven by the mirroring device is expected to be equal to the input reference current. However in practical implementation, parasitic capacitances discharges, temperature drift, leakage or charge injection due to switching behaviour of the CCII can cause a shift of one of these current. The error current $I_{IN\text{error}}$, even if small, will induce a voltage variation across current mirror input impedance which can be sufficient to reach one of the threshold value and activate the CCII. This current can be defined as:

$$I_{IN\text{error}} = \frac{V_{YUP} - V_{YDN}}{r_{X\text{hz}} \,//\, r_{IN\text{cm}}} \approx \frac{V_{YUP} - V_{YDN}}{r_{IN\text{cm}}} \tag{4.25}$$

In the dead-zone, the input impedance can be relatively large and thus the error current relatively low. For the system shown in Fig. 4.7a, input impedance value is close to the output impedance of a cascode current mirror. But too small currents can not be properly conveyed through the CCII and in this case the control loop may start to introduce static errors. A solution is to reduce the intrinsic current mirror input impedance $r_{IN\text{cm}}$, so that the $I_{IN\text{error}}$ quantity is larger or equal to the minimum input current requirement of the CCII. But this reduction of the current mirror input impedance $r_{IN\text{cm}}$ necessarily affect the copy accuracy. In the next section we propose a continuously regulated topology which recover this precision with the help of a second control loop.

4.3 The current-mode non-linear approach combined for very high-performances

The topology discussed in this section constitutes our major contribution to the state-of-the-art of high-performances current mirrors. In Chapter 5 we will present a versatile and high-drive current output stage based on this topology that achieves fast and accurate responses with minimal static power consumption.

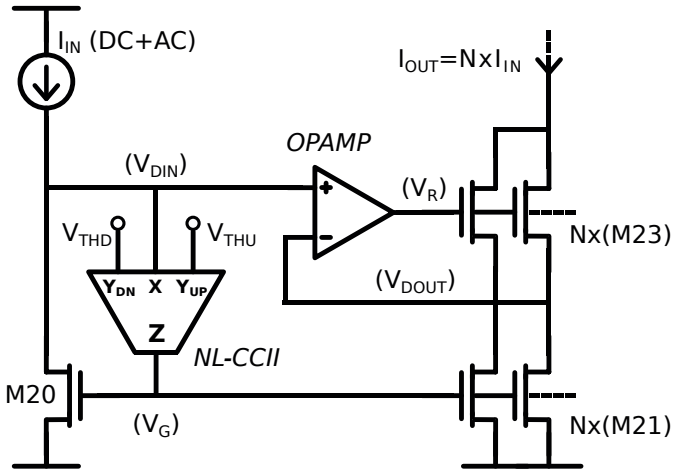


FIGURE 4.12 – Proposed input referred regulated cascode current mirror (IRRC) with non-linear CCII-based feedback

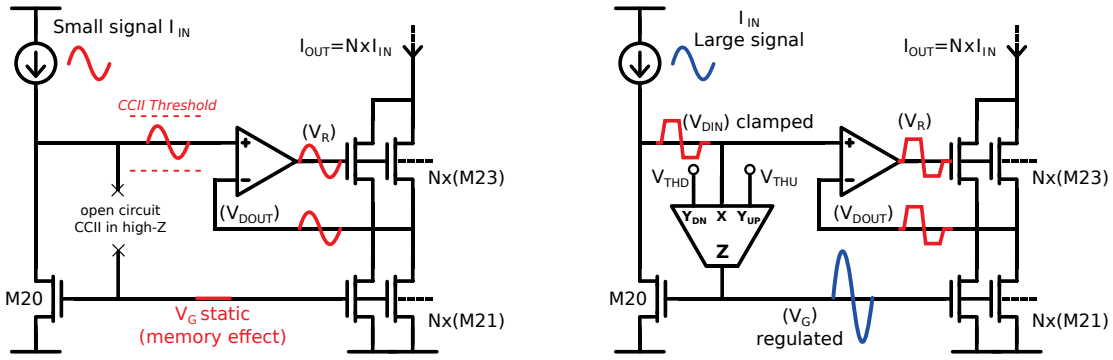
4.3.1 Principle of operation

Illustrated in Fig. 4.12, this enhanced current mirror relies on the non-linear control presented in the previous section (4.2) with a similar structure for the CCII (see Fig. 4.6). The major change consists in the replacement of the high-swing cascode configuration by an input-referred output-regulated cascode one (IRRC), with reference voltage terminal connected to the input node. This way, we force the V_{DS} equality of mirroring devices, we boost the output impedance by the OPAMP gain and we decrease the intrinsic input branch impedance (releasing low current constraints on the CCII). The structure has two feedback loops operating simultaneously, regulating both gate voltage for speed improvement and drain voltages for precise current copy.

The accuracy of the current mirror is ensured conjointly by: (i) large areas for the mirroring devices to minimize mismatch errors (ii) the drain regulation to reduce systematic errors due to asymmetrical v_{ds} modulation in the mirroring pair (iii) the very high output impedance offered by the output regulated cascode configuration (iv) the impedance switching mechanism in the CCII that avoids the speed control loop to introduce static error on the output current.

The low power consumption is achieved thanks to: (i) The use of low-power topologies for the OPAMP (ii) Channel length of cascode devices sized close to minimal dimension which reduces the capacitive load the OPAMP has to drive, reducing consequently the bias current it requires (iii) Large current gain or copy-ratio for the current mirror to minimize

current losses (iv) The unbiased non-linear CCII structure that consumes zero power in steady state.



(A) During small signal operation (B) During large signal operation

FIGURE 4.13 – Schematized behaviour of the IRRC current mirror with non-linear CCII-based feedback

To analyse the behaviour of these devices, let us set the following definitions:

- V_{DIN} nominal (V_{DN}) is defined as

$$V_{DN} = \frac{V_{THD} + V_{THU}}{2} \tag{4.26}$$

- I_{DS20} nominal (I_{DN}) is defined as the current flowing through $M20$ when $V_{DIN} = V_{DN}$. Of course, I_{DN} is a function of V_G.
- input error current I_ϵ is defined as $I_\epsilon = I_{IN} - I_{DN}$.

The dynamic behaviour depends on the amplitude of the currents involved and differentiates in two cases: (i) for sufficiently small input error current (I_ϵ), only the OPAMP is active (Fig. 4.13a). Induced variation of the input voltage occurs within the range fixed by the two CCII thresholds. Equality between input current and output current is achieved by modulation of the drain voltage of $M21$. The CCII stays in high-impedance state and the gate voltage is constant. The speed is mainly determined by pole on the OPAMP output. (ii) large input current variations will cause the input voltage to reach one of the threshold values. The CCII is activated, its low input impedance force the input voltage to be clamped close to the threshold. Gate regulation is activated and the output current follows the input variations according to gate voltage changes. The OPAMP is still active but in this case the mirror speed is mainly dictated by the speed of the CCII-based control loop. Fig. 4.13 summarizes the two cases of the dynamic operation.

This structure also offers the possibility for the mirroring devices to operate in triode region for very high input current range. From the MOS current law in this regime (4.27) we note that with control of both drain and gate voltages, we are still capable to ensure an accurate current copy.

$$I_D = K\frac{W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \tag{4.27}$$

Highest values for the input current are principally determined by residual DC offset (V_{OFF}) and output common mode ranges ($OCMR$) of the OPAMP. Technically, with the proposed CCII structure and with mirroring devices operating in triode region at high current level, the gate voltage can go up to values close to the power supply. However, high output current means large V_{GS} for the cascode device as well and it may saturate the OPAMP output node. This is another reason to take cascode devices with minimal length and maximum W/L for low drive voltage V_{EFF}. On the other hand, with input current increasing and mirroring devices going deeper in the triode region, we can observe a drastic reduction of their output impedance. For drain current modulation due to loads, this output impedance reduction is compensated by the high gain of the output regulated cascode technique as long as the cascoded device stay saturated. But for v_{ds} modulation of mirroring devices, the small voltage difference introduced by the OPAMP offset can now induce significant variations of the output current and this, independently of the load connected.

4.3.2 Analysis and design method

The following part presents theoretical analysis and recommended design choices that lead to an optimized structure in terms of dynamic range, speed, accuracy and power-efficiency. Numerical applications and simulation results are given along the text to illustrate the method, but more extensive simulations and comparisons with previously discussed topologies are presented later in section 4.3.3.

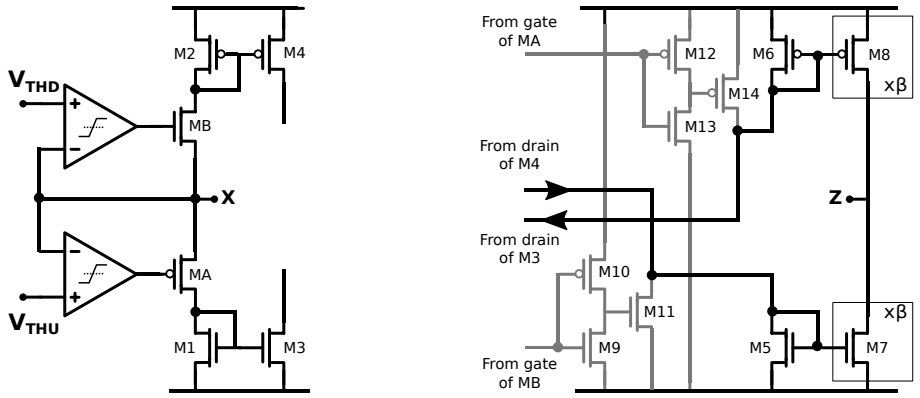
Current mirror sizing for maximal current dynamic range

The current mirror itself is composed by transistors M20 to M23. N identical devices in parallel form the transistors M21 and M23. Each unity device of M21 has the same W and L as the input device M20 and are ideally matched. Each unity device of cascode transistor M23 has the same W as M21. Mirroring devices M20 and M21 are operating in strong inversion for the whole current range because of the high-precision targeted. M23 need to stay in the saturation region to achieve high output impedance. However, for better output compliance, M23 can be sized to be in weak inversion for low current levels as noise and mismatch introduced by a cascode device have a meaningless influence on the overall copy error.

According to the method presented in Chapter 2 (mainly page 40), W/L ratio of M20 and M21 are calculated (4.28) from the minimal input current I_{INmin} specified by the application and the minimum drive voltage V_{EFFmin} to be in strong inversion. The channel length is calculated from target mismatch error at minimum input current (4.29).

$$\left(\frac{W}{L}\right)_{20,21} = \frac{2I_{INmin}}{KV_{EFFmin}^2} = \frac{2I_{OUTmin}}{NKV_{EFFmin}^2} \tag{4.28}$$

$$L_{20,21} = \frac{1}{ERR_{rel}}\sqrt{\left(\frac{K}{2I_{OUTmin}}\right)\left(\frac{V_{EFFmin}^2}{2}A_\beta^2 + 4(2N-1)A_{VTH}^2\right)} \tag{4.29}$$



(A) Input stage (B) Output stage

FIGURE 4.14 – Schematics of NL-CCII stages

Thanks to the non-linear characteristic of the CCII input stage (Fig. 4.14a), the drain of M20 is restrained to a voltage comprised between the two CCII thresholds V_{THD} and V_{THU}. Where V_{THD} is supposed to be higher than V_{EFFmin}. For the sizing procedure below, the input drain voltage V_{DIN} will be considered equal to V_{DIN} nominal (V_{DN}) defined section 4.3.1 page 88.

The maximum drive voltage V_{EFFmax} is defined by the CCII output compliance. Indeed, too high gate voltage for the current mirror can saturate the CCII output stage, diminishing its gain and consequently reducing the speed of the closed loop system. For the proposed output stage shown Fig. 4.14b, to avoid this saturation we need to respect:

$$V_{EFFmax} < V_{DD} - V_{EFFccii,M8} - V_{THn} \tag{4.30}$$

But the CCII is built to be unbiased, the value of its saturation voltage ($V_{DD} - V_{EFFccii,M8}$) fully depends on magnitude of the transient current conveyed. Fortunately the output compliance increases when amplitude of the currents conveyed decreases, the last one depending on the input step amplitude applied. Everything is going in the right direction, the mirror drive voltage is close to V_{EFFmax} when I_{IN} is high, but at these level only small step amplitude are possible as we are working close to the upper limit of the input range. Hence we choose to reduce the dynamic parameter $V_{EFFccii,M8}$ to an arbitrary margin voltage V_{MARG} that should ensure that the CCII output stage stay unsaturated. We observed that in most cases $150\,\text{mV} < V_{MARG} < 250\,\text{mV}$ is sufficient.

Let us define the current dynamic α as:

$$\alpha = \frac{I_{INmax}}{I_{INmin}} \tag{4.31}$$

where I_{INmax} is the maximum input current for which the current mirror gate voltage saturate the CCII output. The following equations give the expressions of the current dynamic, where the mirroring devices continuously operate in saturation region (4.32) and for mirrors where the mirroring devices operate in triode region (at high current level) (4.33).

$$\alpha = \frac{I_{INmax}}{I_{INmin}} = \left(\frac{V_{DD} - V_{THn} - V_{MARG}}{V_{EFFmin}}\right)^2 \tag{4.32}$$

$$\alpha = \frac{I_{INmax}}{I_{INmin}} = 2\frac{(V_{DD} - V_{THn} - V_{MARG} - \frac{V_{DIN}}{2})V_{DIN}}{V_{EFFmin}^2} \tag{4.33}$$

The input drain voltage V_{DIN} is fixed by the CCII thresholds. Value of the lower threshold V_{THD} has to be compatible with minimum input compliances of the OPAMPs found in the CCII and in the regulated cascode. Typically, we have:

$$V_{THD} > 2V_{EFFmin} + V_{THn} \approx 700\,\text{mV in standard 180 nm CMOS} \tag{4.34}$$

This voltage limit can be decreased by the use of rail-to-tail techniques for the OPAMPs. Value of the upper threshold V_{THU} determines the input/output compliances of the current mirror and tends to be as low as possible. However, the gap between the two threshold ΔV_T defines the minimum current variation I_{TRIG} that activates the CCII.

$$I_{TRIG} = g_{DS20}(V_{THU} - V_{THD}) = g_{DS20}\Delta V_T \tag{4.35}$$

We have seen that undesired CCII activation penalizes the dynamic behaviour, hence ΔV_T can not be too small. In simulation, with this topology we observed that a threshold gap set around 200 mV is sufficient to ensure a proper operation of the circuit when g_{DS20} is sufficiently high.

Numerical Application:

Technology:

AMS Standard CMOS 0.18 µm process at 1.8 V supply

V_{THn} V	V_{THp} V	K_n uA/V^2	K_p uA/V^2	V_{EFFmin} V	λ V^{-1}	C_{OX} fF/µm^2
0.35	0.45	280	60	0.2	0.03	7.75

Application requirements:

Minimum input current $I_{min} = 5\,\mu\text{A}$.
8bit resolution for the full range scale.

Calculation of maximum current dynamic:

Transistors operate in triode region at high current level.
CCII saturation margin $V_{MARG} = 100mV$.
CCII threshold voltages V_{THD}=700 mV, V_{VTHU}=900 mV.

Current dynamic α	$= 38$	calculated from (4.33)
Maximum input current I_{max}	$= 190\,\mu A$	calculated from (4.31)
Full range step ΔI	$= 185\,\mu A$	$\Delta I = I_{max} - I_{min}$
Quantum value q	$= 720\,nA$	$q = (\alpha - 1)I_{min}/2^8$

Transistor sizing:

Equation (4.29) is used to compute device channel lengths to target a matching errors less than 0.2%. The condition *M20 always in strong inversion* is used to determine (W/L) ratios.

Mirroring device		Cascode device	
Ratio $(W/L)_{20}$	$= 0.9$	Ratio $(W/L)_{23}$	$= 145$
Channel length L_{20}	$= 33\,\mu m$	Channel length L_{23}	$= 0.2\,\mu m$
Channel width W_{20}	$= 29\,\mu m$	Channel width W_{23}	$= 29\,\mu m$

Dynamic range and matching summary:

For simulation results below, the current mirror output node is fixed to 0.8 V. That value correspond to a voltage located halfway between the two CCII thresholds.

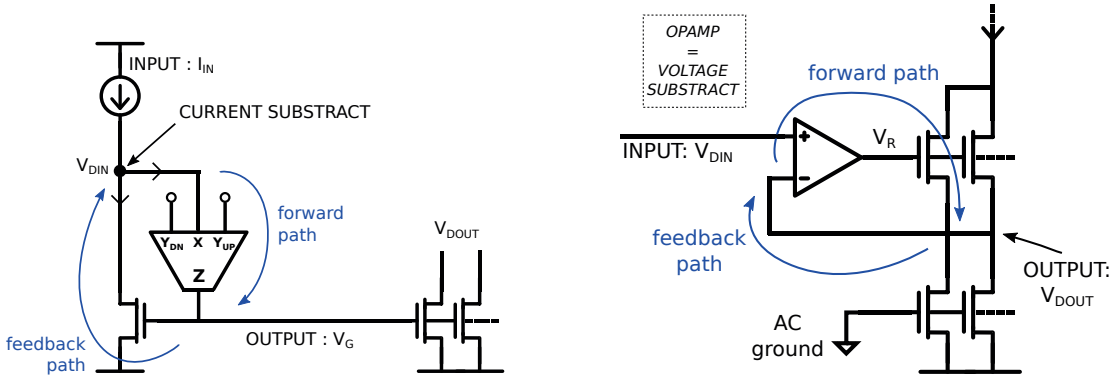
				Mirroring device			Cascode device	
	I_{IN} max µA	α	Err match. %	V_{EFF} min V	V_{EFF} max V	I_{IN} triode µA	V_{GS} min V	V_{GS} max V
calc.	190	38	0.2	0.2	1.35	80.64	x	x
sim.	140	28	0.13	0.22	1.1	95	555	702

The output impedance of this mirror in a simple cascode configuration is calculated with: $r_{OUTCM} \approx g_{m23} \times r_{OUT23} \times r_{OUT21}$
It is equal to 100 MΩ at the minimum input current (5 µA) and 160 kΩ at the maximum input current (140 µA and device in triode region).
These values will be multiplied by the OPAMP DC gain in the input-referred regulated-output cascode configuration.

The previous calculation flow has been used to design the current mirror M20-M23 to meet accuracy requirements while maximizing the dynamic range. Extracted small-signal parameters will be reused in the next analysis to determine optimum values of first order parameters, such as gain, bandwidth or input/output impedance of the CCII and the OPAMP.

System model

The dynamic behaviour is determined by two feedback loops as depicted in Fig. 4.15. Because they affect weakly dependent quantities and address two different characteristics of the current mirror, they will be treated separately.



(A) For V_{GS} control (B) For V_{DS} control

FIGURE 4.15 – Concurrent closed loop systems considered

The first feedback loop, based on the proposed non-linear CCII and dedicated to speed control of the current mirror (Fig. 4.15a) has been already presented and analysed in section 4.2.2 (page 77). The block diagram modelling its behaviour during a transient state is recalled in Fig. 4.16a. The second feedback loop is made for high accuracy and high output impedance. It can bee seen as a low output impedance voltage amplifier, with unity gain feedback, loaded by a resistance (r_{DS} of M21). Here, we consider that the dominant capacitance is the gate capacitance of M23 and thus the dominant pole is on the OPAMP output. Drain-to-source capacitance of M21 and input capacitance of the OPAMP are neglected. The amplifier DC offset is included as a voltage source in series with the non-inverting OPAMP input. The block diagram used for the analysis is shown in Fig. 4.16b. The parameter A_0 is the open-loop gain of the OPAMP, the parameter GBW is its gain-bandwidth product. The equivalent conductance g_{DSeq} is defined as $g_{DSeq} = g_{DS21} // g_{DS23}$.

The voltage transfer function V_{DOUT}/V_{DIN} for drain regulation of the mirroring devices is given in Table. 4.9. We observe that the speed of this loop is dominated by the intrinsic speed of the cascode device M23, which support the decision to size cascode devices with minimal channel length for small gate capacitance and high transconductance gain.

$\frac{V_{DOUT}}{V_{DIN}} = G_{CL}\frac{1+\tau_2 s}{1+\tau_1 s}$	$G_{CL} = \frac{A_0}{1+\frac{A_0}{2\pi GBW}s}$ $\tau_2 = \frac{C_{GS23}}{g_{m23}}$ $\tau_1 = \frac{C_{GS23}}{g_{m23}+g_{DSeq}}$

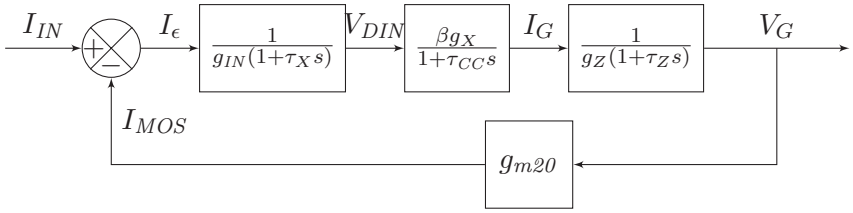
TABLE 4.9 – Transfer function of the drain voltage control loop

The expression of the total output impedance seen by the load is displayed in (4.36). The higher the OPAMP open-loop gain A_0, the higher the output impedance and the more the voltage transfer gain is close to the unity gain.

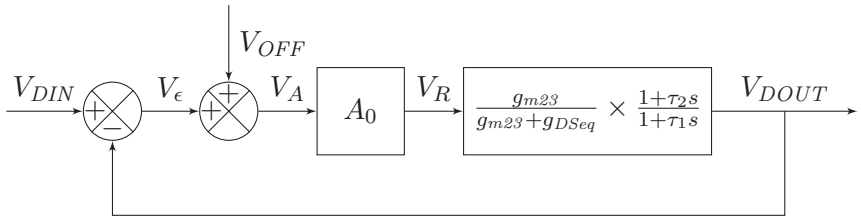
$$r_{OUTCM} = r_{DS21} + r_{DS23} + A_0 \times g_{m23} \times r_{DS21} \times r_{DS23} \tag{4.36}$$

However, the frequency behaviour affect in the same proportion the input voltage V_{DIN} and the OPAMP offset voltage V_{OFF}. Hence, the totality of static voltage errors in the OPAMP is reported to the drain voltage of M23 and generate an output current error I_{OFF} as expressed in (4.37). However with an offset in the order of 10 mV and an output impedance value for the mirror device of about 1 MΩ, this error current is found to be in the order of the dozen of nA. In triode region, the output impedance can go down to several kΩ, significantly increasing the error current but it occurs at large output currents. The relative difference has to be examined to see if the error due to the OPAMP offset starts to dominate the overall error.

$$I_{OFF} = g_{DS21} \times V_{OFF} \tag{4.37}$$



(A) For V_{GS} control



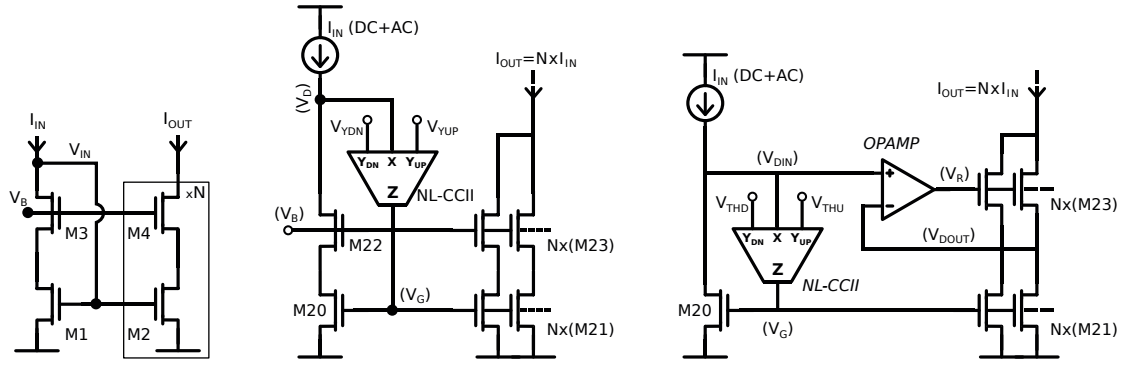
(B) For V_{DS} control

FIGURE 4.16 – Block diagram

4.3.3 Physical implementation and simulation results

This last part presents the implementation and simulation results of the input referred output-regulated cascode current mirror with non-linear CCII-based feedback (NL-CCII IRRC CM in Fig. 4.17c). For comparison purposes we also have implemented the equivalent high-swing cascode current mirrors with both diode-connection (Fig. 4.17a) and non-linear CCII-based feedback (Fig. 4.17b). The full set of simulation results is given in Appendix G.

The circuits have been designed using the TSMC 0.18 µm standard CMOS process. This technology offers better transconductance factor and higher device output impedance than the AMS 0.18 µm process we have used so far for the circuits implementations. Another advantage of the TSMC design kit was the possibility to implemented both standard-V_T and low-V_T devices. Layouts of the proposed feedback circuits in TSMC technology are given in Appendix E.



(A) DCO WSCASC CM (B) NL-CCII WSCASC CM (C) NL-CCII IRRC CM

FIGURE 4.17 – The three current mirror structures evaluated: (A) diode-connected wide-swing cascode DCO WSCASC (B) non-linear CCII-based wide-swing cascode NL-CCII WSCASC (C) non-linear CCII-based input-referred regulated cascode NL-CCII IRRC

Design considerations for the NL-CCII and the OPAMP

Schematic of the CCII is presented in Fig. 4.18. Main differences with the previous non linear current conveyor of section 4.2 are: (i) the self biased cascode devices (M3B and M4B) to improve gain linearity by reducing the v_{ds}-modulation error of the input mirrors. (ii) the output configurable current mirrors, that allow to trim or digitally tune (B[0:3]) the absolute gain value for a more precise control of the system dynamic behaviour. Devices sizes are summarized in Table. 4.10. Simulation results of this non-linear CCII are given in Appendix F.

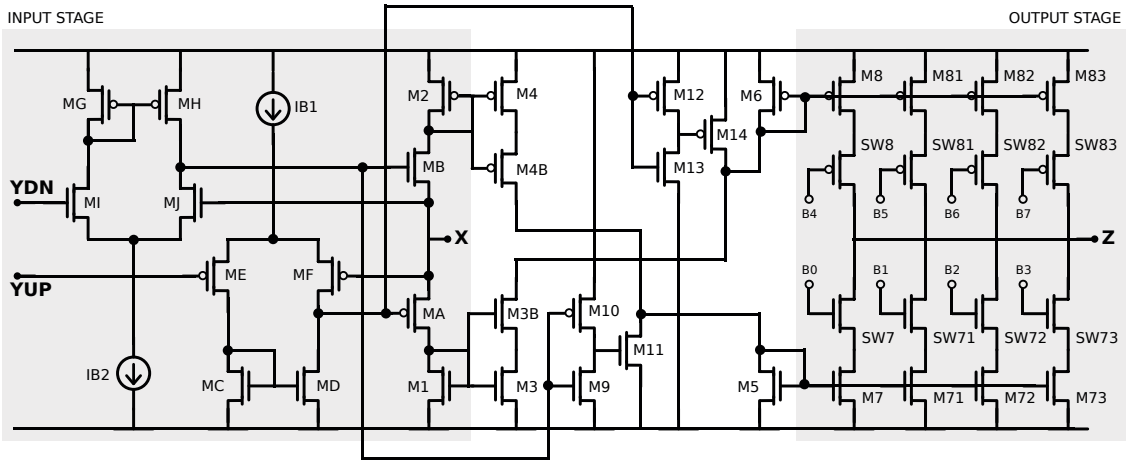


FIGURE 4.18 – Programmable implementation of the non-linear CCII

The OPAMP used for the V_{DS} control loop is identical to the OPAMP controlling the transistor MB in the CCII input stage. Differential pairs are biased in moderate inversion under a tail current of 5 µA (IB1 and IB2) and are realized with low V_{TH} devices (mos mvt). To restrict to a minimum the static consumption, while ensuring sufficient output compliance, we opted for a single stage amplifier with no cascode configuration. More advanced OPAMP topology can replace the single stage OPAMP in both drain and gate

feedback but with a certain increase of the power budget, not always justifiable. Techniques that reduce the OPAMP DC offset will also reduce copy error at high current level. Techniques that increase its gain-bandwidth product will lead to higher output impedance when used for drain regulation and sharper transition between the two NL-CCII states when used for gate regulation.

	W/L µm		W/L µm		W/L µm		W/L µm
M1	3.5/0.25	M2	5/0.25	M5	0.45/0.25	M6	1.5/0.25
M3	3.5/0.25	M4	5/0.25	M7	$2 \times 0.45/0.25$	M8	$2 \times 1.5/0.25$
M3B	12/0.25	M4B	20/0.18	M71	$4 \times 0.45/0.25$	M81	$4 \times 1.5/0.25$
MA	7/0.18	MB	2/0.18	M72	$8 \times 0.45/0.25$	M82	$8 \times 1.5/0.25$
MC	1/1.5	MG	0.5/1.5	M73	$12 \times 0.45/0.25$	M83	$12 \times 1.5/0.25$
MD	1/1.5	MH	0.5/1.5	M9	0.5/4.5	M12	0.5/4.5
ME	2.5/0.5	MI	2/0.5	M10	2.5/4.5	M13	2.5/4.5
MF	2.5/0.5	MJ	2/0.5	M11	0.5/4.5	M14	2.5/4.5

Transistors ME,MF,MI and MJ are low-threshold devices

TABLE 4.10 – Transistors sizing for the NL-CCII

Tests presentation

In the whole following tests, mirroring devices of the three current mirrors presented Fig. 4.17 are sized with $W/L = 1.2$ in order to operate on the edge of the strong inversion at minimum input current I_{IN} =5 µA. The mirror current gain (the copy ratio) is fixed at $N = 20$, leading to a minimum output current of 100 µA.

Tests include: (i) Measure of the influence of the channel length on accuracy and bandwidth for the diode-connected current mirror. We look at the speed versus the variability for small dimension as well as for the maximum dimension authorized by the process rules. (ii) Measure of static performances such as input/output compliances, systematic current transfer errors (no mismatch) and output impedances. (iii) Illustration of the typical dynamic behaviour with measurement of the step response and the harmonic response for a full-range input signal. (iv) Statistical measurements to evaluate both static and dynamic performance dispersions.

CM sizing and speed-accuracy trade-off

In this first test we compare accuracy and bandwidth of a diode-connected high-swing cascode current mirror (Fig. 4.17a) for a channel length (L_{CM}) ranging from 4 µm to 18 µm (the maximum length allowed by the DRC rules). The operating point is fixed at $I_{IN} = 30$ µA (current source), $V_{out} = V_{DD}/2 = 0.9$ V (voltage source) and $V_B = 1.3$ V (voltage source). The (W/L) ratio of mirroring devices is kept constant and chosen such that $V_{IN} \simeq 0.9$ V for the considered operating point ($W_{CM}/L_{CM} = 1.2$). Channel width of cascode devices W_{CASC} are kept equal to the width of mirroring devices W_{CM}. Lengths L_{CASC} are taken at the fixed value of 0.25 µm. Fig. 4.19 shows the DC output error distribution for different channel length, taking into account systematic errors, process

variations and mismatch errors. Fig. 4.20 is an AC measurement of the current mirror bandwidth as a function of the channel length L_{CM}.

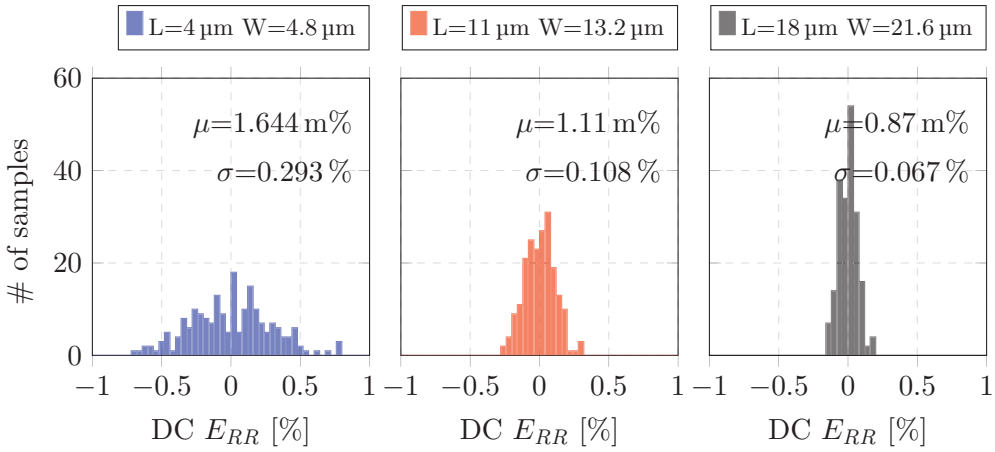


FIGURE 4.19 – Static output error the diode connected wide-swing cascode current mirror (DCO WSCASC CM) at various lengths.

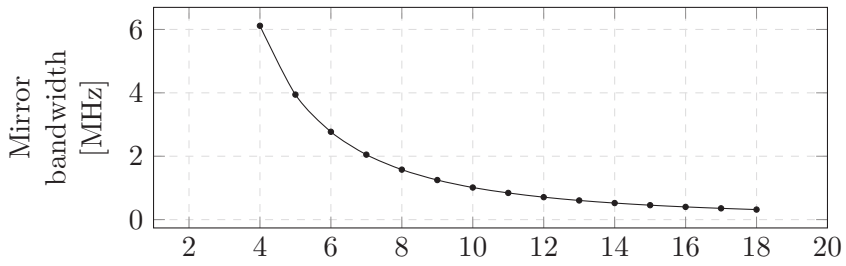


FIGURE 4.20 – Simulated bandwidth for the diode connected wide-swing cascode current mirror (DCO WSCASC CM) at various lengths of the mirroring devices. Without surprise the bandwidth is decreasing proportionally to $1/L^2$.

As expected, output error and bandwidth decrease when the channel length increase, but using the metric $FOM1$ of (Kinget, 2005) introduced Chapter 1 which is defined by:

$$FOM1 = \frac{\text{bandwidth}}{\text{power} \times \text{error}} \tag{4.38}$$

We observe again that independently of the channel length we obtain the same score. This means that by taking the mirror devices with the maximum length (18 µA) we have spent all the speed-accuracy budget to minimize the output error. This will be our choice for the next tests. The NL-CCII in the gate voltage control in charge of speeding up the mirror with minimal impact on error and power

Static measurements

With the measurement of static behaviours we compare input/output compliances, systematic current transfer errors (no mismatch) and output impedances. Mirroring devices are sized with $W_{CM}/L_{CM} = 21.5\,\mu m/18\,\mu m$ and cascode devices with $W_{CM}/L_{CM} =$

21.5 µm/0.25 µm. As in the previous test, $V_{OUT} = V_{DD}/2 = 0.9\,\text{V}$, $V_B = 1.3\,\text{V}$ and CCII thresholds are fixed at 0.6 V and 0.8 V in the IRRC CM. The input current I_{IN} is imposed by an ideal current source and varies from 5 µA to 160 µA. Input voltage and systematic copy error as a function of the input current[1] are shown Fig. 4.21. These are DC simulations. Fig. 4.22 gives the output current/voltage characteristic and the evolution of the output impedance as a function of the expected output current.

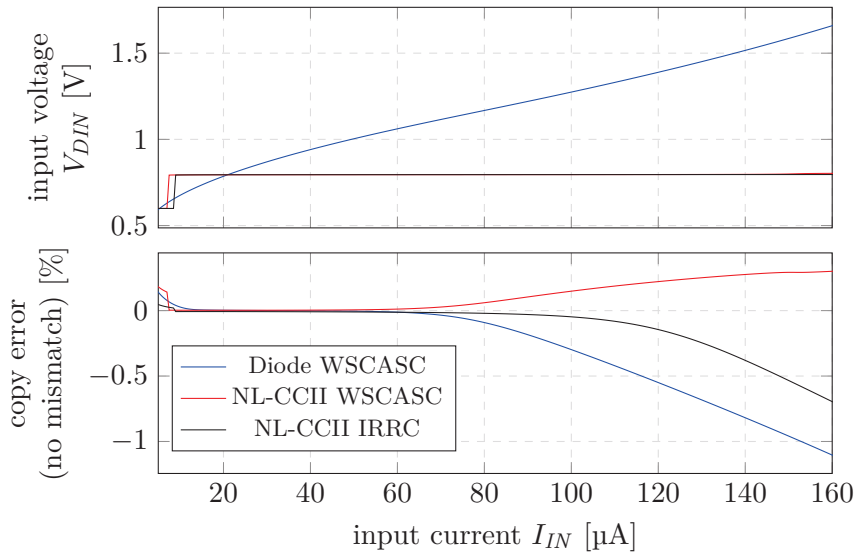


FIGURE 4.21 – Static characteristics of input voltage and current transfer error versus input current

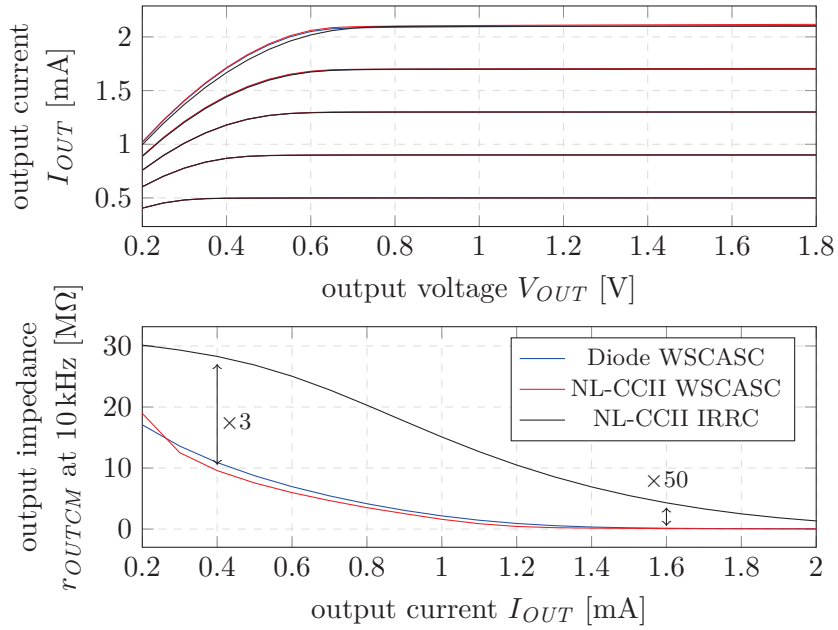


FIGURE 4.22 – Static characteristics of output I/V curve and output impedance versus output current. $V_B = 1.3\,\text{V}$, $I_{IN} = 5\,\mu\text{A}$ to $100\,\mu\text{A}$. CCII thresholds = 0.6 V and 0.8 V.

[1] In practice, we note that during operating point computation (.dc analysis), the input voltage V_{DIN} has systematically converged to a value close to one of the CCII thresholds.

We observe that while all the circuits require approximately the same minimum output voltage for a proper operation in the saturated region ($V_{OUT} > 0.7\,\mathrm{V}$ for I_{OUT} up to 2 mA), the minimum input requirement is drastically different between diode-connected configuration and with NL-CCII-based feedback. Thanks to the input switching mechanism of the CCII, the input voltage is constrained and the minimum admissible value is actually equals to the upper threshold value (0.8 V). Diode-connected high-swing cascode mirror show lower input requirement as long as the input current is under 20 µA. But the minimum admissible value increases with the input current at a rate of $\approx \sqrt{I_{IN}}$, which significantly reduces the room for the input source to operate at high current level.

Regarding the accuracy, the diode-connected mirror has the lower dynamic range before systematic error occurs. At high level, the NL-CCII IRRC CM shows higher current error than the NL-CCII WSCASC CM. This is due to the saturation of the OPAMP controlling the cascode device. Indeed, when moving toward high current levels, the gate voltage of cascode devices increases until it reaches the maximum output voltage of the OPAMP. Beyond this limit, if we keep increasing the input current, the OPAMP can not ensure a proper regulation and starts to degrade the drain equality of mirroring devices and so the copy accuracy. But the reduction in the dynamic range is compensated by an increase of the output impedance (ranging from ×3 to ×50).

Based on the error plot we will consider for the next dynamic response measurements, an input current ranging from 5 µA to 110 µA, common for the three circuits. All mirrors showing a typical systematic error $< 0.4\,\%$ across this dynamic range.

Dynamic behaviours

The typical dynamic behaviour is illustrated by a transient simulation of the three circuit with a full-range signal applied on the input. A more extensive coverage of the behaviour for different operating points and step sizes is made in sub-section *Statistical measurements*. For time domain evaluation, the input stimuli is a 3 µs current pulse from 5 µA to 100 µA which leads to an output current pulse of 100 µA to 2 mA. For distortion measurements, we looked at the output current spectrum when the input stimuli is a pure sine wave of 50 µA ± 20 µA at 100 kHz. All devices have the same size as in the previous test. The load is an ideal voltage source at $V_{DD}/2$ =0.9 V. The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V. CCII threshold are fixed at 0.6 V and 0.8 V and CCII gains are set to 24 ('0111') for both NLCCII WSCASC and NLCCII IRRC current mirrors.

Fig. 4.23 shows the evolutions of input current, output current and transient relative output current error, for one period of the input signal (6 µs). Measured response times at 0.4 % demonstrate the efficiency of the NL-CCII-based feedback to speed up the current mirror. Table. 4.11 compares the response times and the power efficiencies of the three structure for rising edge transitions. *Total Harmonic Distortion* (THD) and *Spurious Free Dynamic Range* (SFDR) measurements results are given in Table. 4.12. More details on the distortion measurement are given in Appendix G.

	$tr_{0.4\%}$	PW_{EFF} at $I_{OUT} = 100\,\mu A$	PW_{EFF} at $I_{OUT} = 2\,mA$
DCO WSCASC CM	1.69 µs	95.2 %	95.2 %
NL-CCII WSCASC CM	244 ns	90.9 %	94.5 %
NL-CCII IRRC CM	71.4 ns	88.9 %	94.1 %

TABLE 4.11 – response time and static power efficiency measurements for a full range input signal

	THD (dB)	SFDR (dB)
DCO WSCASC CM	-27.8	30.2
NL-CCII WSCASC CM	-35.4	37.24
NL-CCII IRRC CM	-43.7	46.32

TABLE 4.12 – THD and SFDR measurements for a sine wave of 50 µA±20 µA at 100 kHz

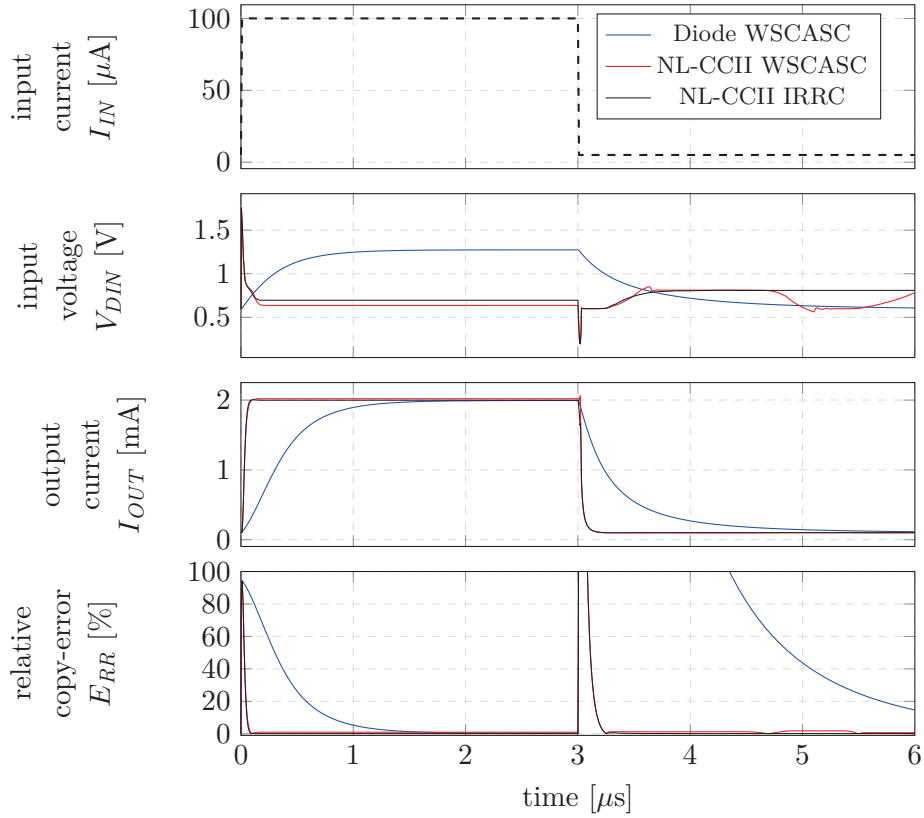


FIGURE 4.23 – Transient response to a full range step

In Fig. 4.23 we can see that the input nodes voltages of the two NL-CCII-CM actually vary within the fixed CCII thresholds. However for the NL-CCII WSCASC current mirror after the falling edge, we observe a slow residual oscillation on the input. This is due to the issue discussed in section 4.2. It relates to the high input impedance we obtain with cascode devices on input branch, which induces unwanted activations of the current conveyor. For the next statistical measurement, the current conveyor gain in the NL-CCII WSCASC CM will be limited to a lower value (from 24 to 8) to try to eliminate the residual oscillation

by reducing the amplification of errors due unwanted activations of the current.

Regarding the distortion measurements, the NL-CCII IRRC shows better THD and SFDR for the step considered thanks to the drain regulation and the high output impedance offered by the topology. However, when the step amplitude decreases, the effects of noise and distortion generated by the CCII switching mechanism become more important and degrade the THD. The diode connected configuration generally shows more linear response. Fig. 4.24 shows the results of the long-time transient simulation for which we have calculated the spectrum and measured the THD and SFDR.

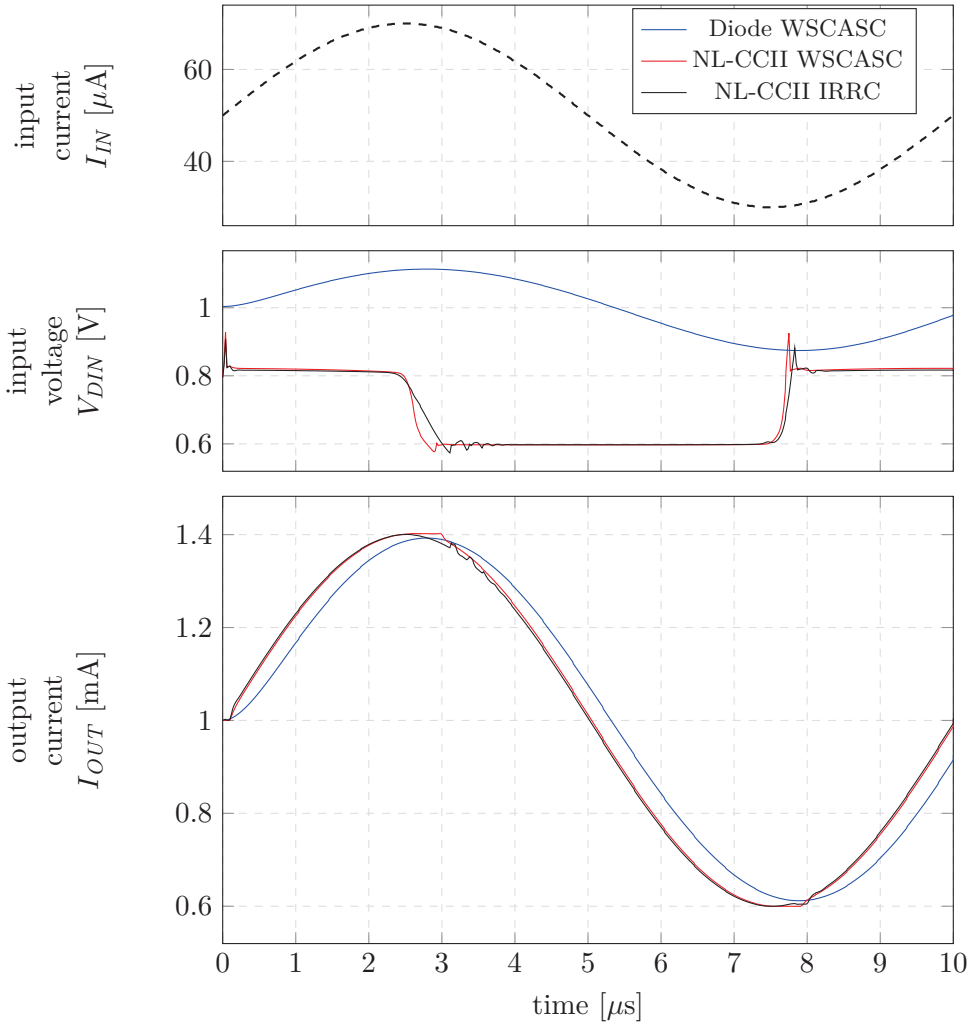


FIGURE 4.24 – 1 period of long time simulation with harmonic signal. Input current wave has a DC component of 50 µA and a magnitude of 20 µA.

Statistical measurements

Monte-carlo simulations are performed for statistical evaluations of the overall copy error, the drain mismatch of mirroring devices (absolute difference between drain voltage), the settling time and the output impedance. The three circuits are stimulated with several steps of various amplitudes, ranging from ±500 nA to ±50 µA while biased at different levels across the input current range, starting from 5 µA up to 110 µA. Stimuli cases are

summarized in Table. 4.13. Static output error and drain mismatch versus the input current range are reported in Fig. 4.25. The curve represents the average values and error bars show the corresponding standard deviation ($\pm\sigma$). Fig. 4.26 puts in relation the measured response time and its standard deviation with the static power efficiency for each of the 17 stimuli cases.

#	name	bias	step	#	name	bias	step
1	bias1-pulse1	10 µA	±0.5 µA	9	bias4-pulse1	70 µA	±0.5 µA
2	bias1-pulse2	10 µA	±2 µA	10	bias4-pulse2	70 µA	±2 µA
3	bias2-pulse1	30 µA	±0.5 µA	11	bias4-pulse3	70 µA	±20 µA
4	bias2-pulse2	30 µA	±2 µA	12	bias5-pulse1	90 µA	±0.5 µA
5	bias2-pulse3	30 µA	±20 µA	13	bias5-pulse2	90 µA	±2 µA
6	bias3-pulse1	50 µA	±0.5 µA	14	bias5-pulse3	90 µA	±20 µA
7	bias3-pulse2	50 µA	±2 µA	15	bias6-pulse1	110 µA	±0.5 µA
8	bias3-pulse3	50 µA	±20 µA	16	bias6-pulse2	110 µA	±2 µA
				17	fullrange-pulse	60 µA	±55 µA

TABLE 4.13 – Stimuli summary

.

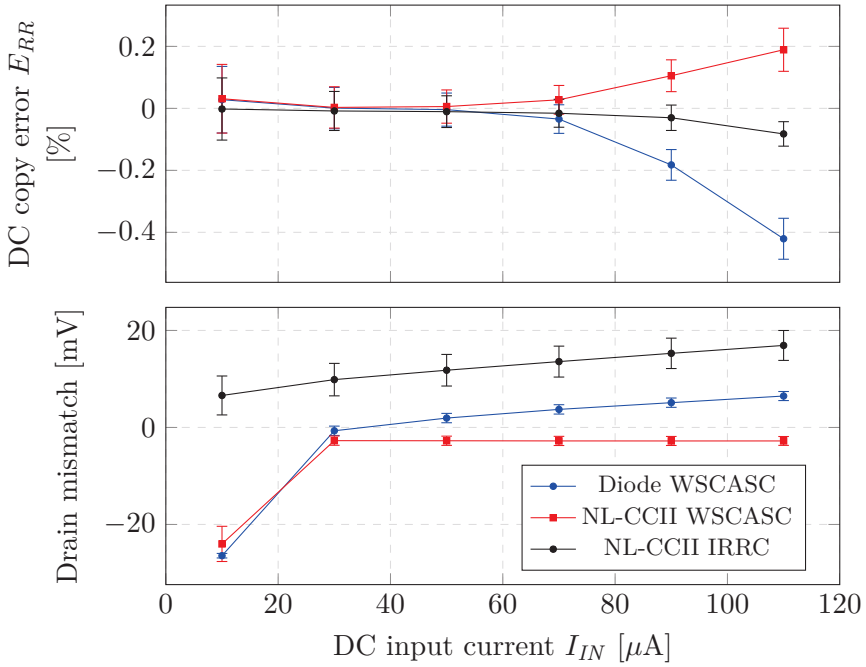


FIGURE 4.25 – DC current copy error and drain mismatch of mirroring device. Error bars represent the standard deviation (σ) obtained after a 200 runs monte-carlo simulation.

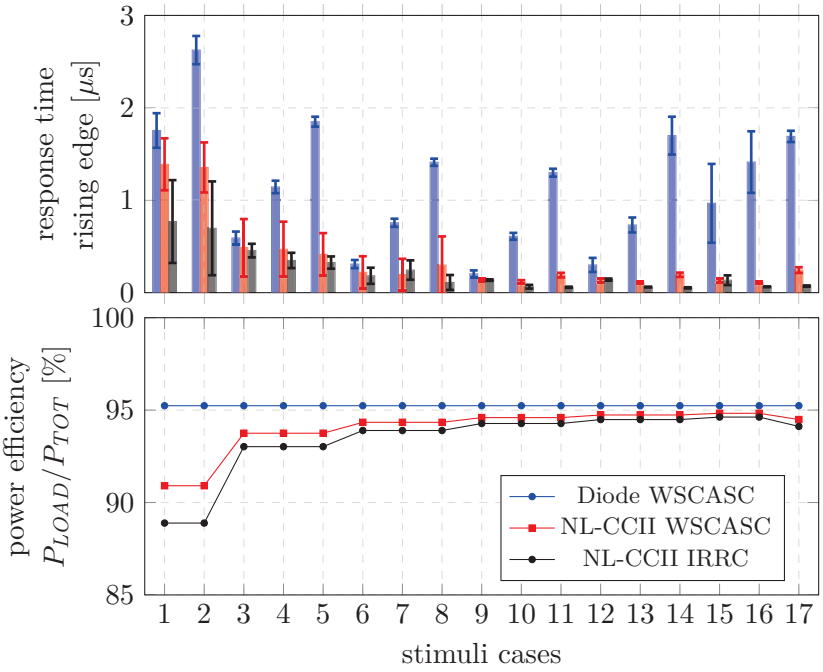


FIGURE 4.26 – Response time at 0.4 % and power efficiency for each stimuli reported in Table. 4.13. Error bars represent the standard deviation (σ) obtained after a 200 runs monte-carlo simulation.

As expected, the NL-CCII IRRC CM exhibits a drain voltage difference (10-20 mV) slightly greater than the WSCASC configurations (5-10 mV), but looking at the copy error plot we observe that the NL-CCII IRRC CM still offers the highest accuracy, the error at 1σ is always lower than 0.2 % for the full input range.

Regarding the mirror speeds (Fig. 4.26), we observe larger relative standard deviations ($\sigma_t r/\mu_t r$) for the both topologies based on the current conveyor. This is explained by the device dimensions constituting the CCII. Transistors are all close to minimal dimensions to reduce silicon area and achieve high speed feedback operation but at the price of large variability. However, as the speed has drastically increased, the absolute amount of response time dispersion stays in the order of ≈ 100 ns. The higher response time of the NL-CCII WSCASC compared to the NL-CCII IRRC is due to the reduction of its current conveyor gains. Indeed to avoid unwanted pseudo-oscillations of the input node we reduced the CCII gain to 8. What we observe is the direct relation between CCII gains and overall system speeds.

Evaluation with speed-power-accuracy metrics

To ease the comparison, we re-use the figure-of-merits that have been presented in Chapter 1. Definitions of the metrics are recalled in Table. 4.14. Results are given for each stimuli case mentioned in the previous section (Table. 4.13).

The response time $t_{r0.4\%}$ is measured on the transient response. The static output error E_{RR} is defined here as the simple sum of systematic and random errors that occurs:

$$\text{DC copy error} = |\mu(E_{RR})| + |\sigma(E_{RR})| \tag{4.39}$$

Power efficiency is defined as the ratio of the power delivered to the load ($I_{OUT} \times V_{DD}$) over the total power dissipated, which includes input reference currents and dedicated bias for the feedback circuits.

$$\text{power efficiency} = \frac{P_{LOAD}}{P_{TOT}} = \frac{I_{OUT}}{I_{OUT} + I_{IN} + I_{BIAS}} \tag{4.40}$$

The bandwidth is estimated as:

$$\text{estim. bandwidth} = \frac{1}{2\pi \times \tau} \approx \frac{1}{2\pi \times \frac{t_{r0.4\%}}{5}} \tag{4.41}$$

For the metrics FOM A, B and C, a high score demonstrates an efficient use of the total power dedicated to the circuit to achieve precise and/or fast current generation. In metric FOM C, measure of the static precision is replaced by a measure of the linearity (THD). The last metrics put in relation the speed with power efficiency (FOM G) or with accuracy (FOM I). The Fig. 4.27 gives the score at the four mentioned metrics for each stimuli cases in Table. 4.13.

$\text{FOM A} = \frac{\text{power eff}}{\text{resp. time} \times \text{dc error}}$	$\text{FOM B} = \frac{\text{power eff} \times \text{bandwidth}}{\text{dc error}}$
$\text{FOM C} = \frac{\text{power eff} \times \text{bandwidth}}{\text{thd}}$	
$\text{FOM G} = \frac{\text{power eff}}{\text{resp. time}}$	$\text{FOM I} = \frac{1}{\text{resp. time} \times \text{dc error}}$

TABLE 4.14 – Definition of various figure-of-merits used for circuits comparison

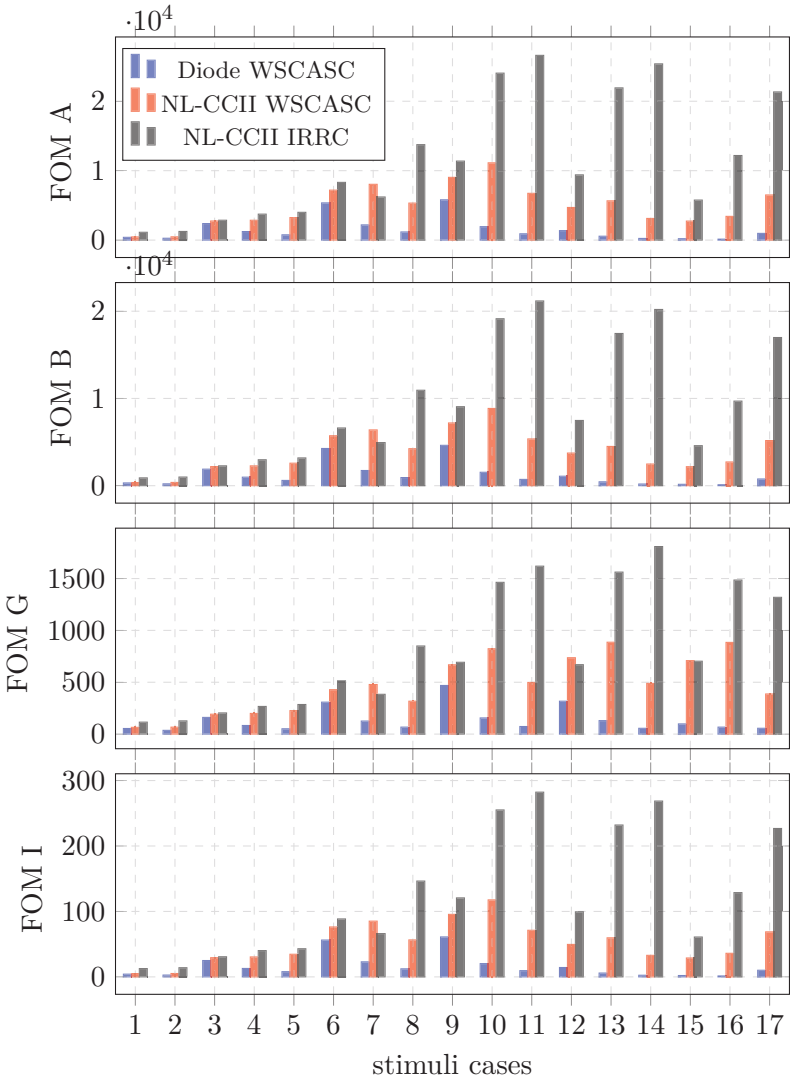


FIGURE 4.27 – Time domain evaluation with metrics of the speed-power-accuracy trade-off

To compare the NL-CCII IRRC CM with other topologies of advanced current mirror available in the literature, we use the performances measured for the full-range stimuli case. Published work cited here have already been detailed in section 1.2.2 of Chapter 1. Performances summary and scores to the FOMs are presented in Table. 4.15.

Finally, according to the scores achieved by the different circuits, the proposed NL-CCII IRRC CM is found to be the most efficient structure to achieve fast and precise response at minimal power while offering high dynamic and high drive capabilities. This topology exhibits the best score for each stimuli case simulated when compared to the equivalent DCO WSCASC and NL-CCII WSCASC current mirrors. It also obtains for the two first metric (FOM A,B) the best score when compared to previous published work. We see the limitation of the non-linear control loop by looking at the last metric (FOM C), putting in relation speed and power efficiency with THD, for which the proposed topology is not as much competitive.

perf	This work	Koliopoulos 2007	Esparza 2012	Pennisi 2002	Ramirez 2004	Safari 2016	Aggarwal 2016	Vajpayee 2010	Torralba 2003	Zeki 2000
Min output current (µA)	100		10	10	4.2	0	0	0	0	-220
Max output current (µA)	2000		200	100	8	60	280	300	20	570
Output error (%)	0.06	2.4		0.4		0.3	0.8	5		0.5
Resp. time at 1% (µs)	0.07			0.07	0.25			0.02	0.02	
THD (%)	0.65	1	0.1	0.8		0.8			0.1	
Bandwidth (MHz)	11.15		98	140	40	80	132	398	122	29
Power efficiency (%)	94.12	40	70	30	82		50	33	38	49
FOM A	22.7			1.07				0.33		
FOM B	16.99	3.08		10.5			8.25	2.63		2.84
FOM C	1.61452	7.4	68.6	5.25					46.36	

TABLE 4.15 – Performances summary and comparison with previous published work

4.4 Conclusion

In this chapter, we have introduced, analysed and illustrated a novel design approach relying on a power-efficient speed boosting technique based on current-mode non-linear control loop. The control loop has been implemented using a dedicated low-power current conveyor of second generation, for which the behaviour have been made intentionally non-linear. This solution constitutes the major contribution of the work presented in this manuscript.

As demonstrated in section 4.1, the replacement of the voltage-mode feedback (OTA) that exists in standard active-input current mirror by a current-mode circuit (CCII), significantly enlarges the stability domain and increases the maximum speed we can achieve, while offering a supplementary degree of freedom for the tuning of the system response. In addition, in section 4.2, the forced non-linear characteristic of the current conveyor has been proposed to unbind static specifications from constraints related to the dynamic behaviour and overcome the *speed-power-accuracy trade-off* found in classical current mirror design. The proposed CMOS implementation is supported again by a theoretical analysis dedicated to the optimisation of this new type of active-input current mirror. Conclusions of the study show that with this solution higher speed than the previous active-input structures can be reached, with minimal impact on the overall accuracy and the static power consumption.

Best performances have been achieved with the topology discussed in section 4.3, which combines the non-linear current-mode feedback solution for fast and energy-efficient operation with an input-referred regulated-cascode configuration for precise current mirroring. This last topology constitutes a competitive elementary current source for the design of high-performances circuits, capable to provide wide range of currents (from several dozen of µA to several mA) with high-precision. In the context of biomedical devices, the next chapter presents practical applications of the new design approach developed so far.

Chapter 5

Application to high-performance current sources dedicated to biomedical devices

This last chapter presents the application of the active current mirrors proposed in Chapter 4 to the design of output stages in biomedical devices. Two circuits were designed and sent to manufacturing. Comparison between typical results and post-layout simulation results are examined. Finally the proposed approach will be compared with a set of recent published circuits that share the similar challenges and constraints.

5.1 Introduction to biomedical applications

Electrical stimulation

The first medical application where the proposed current sources are of main interest is the functional electrical stimulation. Electrical stimulation is a widely spread procedure in biomedical engineering. It consists in activating parts of the nervous systems, skeletal muscles or organs. An example of recent advances in the field of neuroengineering is the publication of significant results in brain–spine interface alleviating gait deficits after spinal cord injury (Capogrosso et al., 2016). Design of miniaturized, fully implantable implants with advanced technological nodes have considerably facilitated *in-vivo* experiments.

Today's common practice of electrical stimulation makes the use of current waves ranging from several dozens of µA to few mA. They convey electrical charges through the electrode/tissue interface to target specific muscles, nerves or cells (Stuart F. Cogan, 2008). Equilibrating charges with inverted current is the key for safe and reliable experimentations on living organisms. However, extra left charges, due to device or electrode imperfections may induce irreversible chemical reactions. Drawbacks are the implant rejection and/or tissues degeneration (Merrill, Bikson, and Jefferys, 2005) (Stuart F Cogan et al., 2016). With full control of the injected electrical charge, we can limit the risk to compromise the experiment or harm the subject. Applied external electric fields disturb the equilibrium membrane potential and trigger a cell reaction.

Inward (positive) currents move the membrane potential to more negative values (hyperpolarization) and outward currents (negative) change it to less negative values (depolarization). Beyond a threshold level, membrane depolarization can trigger an action potential (Bhadra, 2015).

Action potential is the elementary unit of information manipulated by the majority of neurons and muscle fibres. The goal of functional electrical stimulation is the artificial generation or suppression of action potential in targeted excitable cells.

An electrode forms the interface between implanted hardware and living tissue. Electrode choices have to consider bio-compatibility, geometric constraints of location, mechanical requirements, and electrical parameters for charge transfer. This interface is usually represented by a parallel resistance (Faradaic effect) and capacitance, in series with a solution resistance. The applied stimulation regime has to avoid irreversible reactions at the electrode, to minimize chemical products that can harm tissues or electrodes. In practical systems, the primary electrode for stimulation is connected to a controlled current source and an electrical return path is provided to ground. Multi-polar applications use multiple electrodes or electrodes arrays to deliver temporally and spatially distributed coherent signals to the target components. Spatial patterns of stimulation, such as bipolar and tripolar, have been studied for many year (Sweeney, Ksienski, and Mortimer, 1990) and has shown conclusive results to target groups of cells or nerves that are topographically segregated (Polasek et al., 2009). But efficiency of the selective process resides in a precise control of current amplitudes and phases between each poles.

The main criteria for choice of stimulus parameters are specific functional objectives and capability of target tissue, which can significantly varies depending on the application. For instance, retinal cell stimulation for vision recovery (Grumet, Wyatt, and Rizzo, 2000) has very different specifications from vagus nerve stimulation used to modulate essential autonomic (heart pace) or somatic (motion) functions (Guiraud et al., 2016).

Unit pulses of applied current are characterized by amplitude, duration, and shape. Stimulation frequencies range from continuous signal to intermittent pulses in the order of several kHz (Greenbaum and Zhou, 2009). In Fig. 5.1, are represented the most popular types of stimulation signal encountered in the literature.

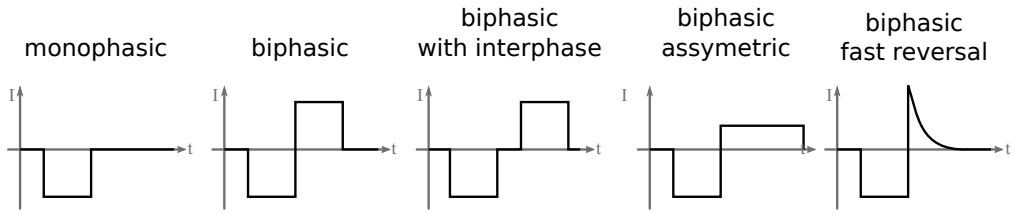


Figure 5.1 – Most common types of neural stimulation signals

Although single-phase pulses may be adequate for neural effects, biphasic pulses are used to ensure the electrochemical stability of the electrode/tissue interface. In this case, the second phase may alters the neural effects of the first phase. Thus, it can be delayed in time (interphase gap), has different shape (asymmetric) or both. Most experiments has been using rectangular stimulation pulses, but other pulse shapes (exponential, gaussian, linear...) have been proposed to provide more energy-efficient stimulation (Sahin and

Tie, 2007). Some works also have demonstrated the efficiency of repeated burst of short pulse (several µs) with increasing amplitude in hearing implants (Killian, Wallenberg, and Smoorenburg, 2008). Others recommend the use of sinusoidal current waves to enforce the strength of muscle contraction and subject comfort. They are shown to require less charge density to elicit the same fibre activation (Bennie et al., 2002).

What we note is the generalized need for implanted devices with very precise charge-balanced generation and capable to handle a large range of time-variant signals. Such devices would open new areas of scientific exploration for functional electrical stimulation.

Bio-impedance analysis

Another important domain of bioengineering is the extraction of chemical or physiological properties of a tissue through the measurement of its electrical impedance. This technique is called bio-impedance analysis.

Biological tissues can be modelled as parallel resistor/capacitor combinations and characterized by a complex valued admittance (Y) for its ability to transmit current. When current is injected through cell membrane, the transient voltage response depends on the cell time constant determined by the resistor/capacitor combination.

An artificial source injects a current into the tissue while a measurement channel evaluates the impedance by analyzing the voltage developed across electrode/tissue interfaces. Contrary to the electrical stimulation, charges flowing into the subject should not induce any physiological response. Undesired cell or nerve activations during the impedance measurement may lead to wrong result interpretations. They may also reveal inconvenient or harmful to the subject when studying living organisms. The charge-balanced stimuli requirement is still present for bio-impedance measurements as any change in the electrode or tissue composition would bias the experiment. However, stimuli amplitude can not be too small because we need to cause a potential variation that can be properly acquired by the measurement channel. Hence, linearity (THD) and good signal-to-noise ratio (SNR) for the current generation channel are the main challenges for bio-impedance device.

Different types of current wave are employed in bio-impedance analysis. Measurements have been performed using sine waves with frequency sweep, binary waves or multi-tone/broadband signals (Sanchez et al., 2012). Typical amplitudes range from few µA to several hundreds of µA and frequencies from few kHz to few MHz depending on the chemical or physiological properties we want to characterize. Impedance measurement was traditionally done at a single frequency, but for some applications, bio-engineers are more interested in the full complex spectrum of the impedance.

In-vivo and implanted bio-impedance measurement devices is a recent topic. To our knowledge, among the integrated designs, best results reported in the literature have been achieved using high performances OTAs as voltage-controlled output current drivers (see section 1.1.2).

Even if in many aspect, bio-impedance analysis is related to electrical stimulation, this topic was slightly out of the scope of the work carried out during this thesis. However, we

will see that the proposed current output stage in section 5.3 can be easily configured to operate as a current driver for bio-impedance measurements. The implementation has not been optimized for this application, but the results show positive perspective about the uses of design solutions presented in Chapters 3 and 5 to the conception of implantable device dedicated to bio-impedance analysis.

In summary

What we note is the generalized need for implanted devices with very precise charge-balanced generation capable to handle a large range of time-variant signal, to open the scientific exploration of the electrical stimulation capabilities. In summary, designing implantable biomedical devices and more specifically electrode current generation stages require specific care for:

1. random and systematic errors during current amplification and distribution between each poles
2. stability and speed of transient response for both small and large signal operation
3. power efficiency as the heat dissipated by implanted circuits have to be kept low and autonomy of portable devices kept high.

5.2 A versatile architecture for monopolar output stage (AMS Chip)

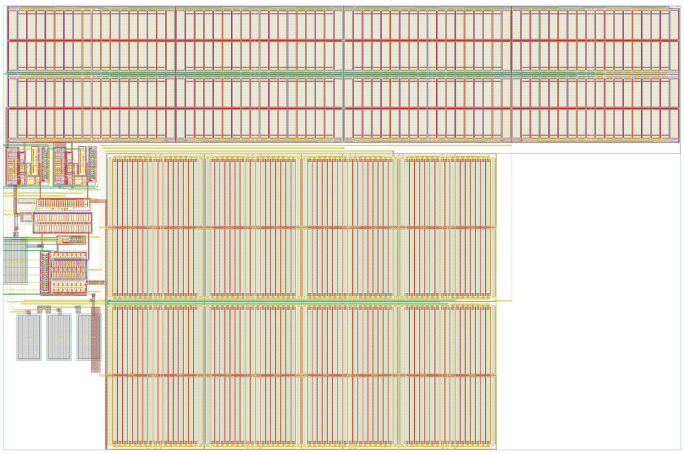


FIGURE 5.2 – Layout of the proposed current output stage

5.2.1 Overview and general specifications

The current driver presented in this section has been designed as a proof-of-concept for the non linear CCII-based control. It has been realized in the AMS standard CMOS 0.18 µm process. The objective was to test if the solution could be used in a practical implementation of a current output stage dedicated to mono-polar neural stimulation.

Another expected outcome was the validation of the adopted design strategy. Indeed, as discussed so far, to achieve high-performances we rely on power-efficient speed boosting techniques applied to very large but precise current mirrors. However, layout decisions and phenomenons that occur on large die area, not necessary modelled, can only be evaluated on silicon. Unfortunately, due to the premature end of life of the technology, the manufacturer decided to postpone the fabrication of our chip to an undetermined date. As a consequence, only post-layout measurements are available.

This output stage has been designed to provide an output current of $\pm 1\,\mathrm{mA}$, with a maximum response time less than $1\,\mu\mathrm{s}$, a maximum relative output error less than $0.4\,\%$ (corresponds to a resolution of 8 bits = 1/256) with a static power efficiency greater than $80\,\%$. The output polarity is digitally controlled and an external DAC provides the input current. A schematic view of the circuit architecture is shown Fig. 5.3. The circuit comprises, a 12 bits digital buffer to allow the configuration through a micro-controller, a bias circuit providing static currents to polarized devices, a current multiplexer to select between two analog inputs for the DAC current and finally the current driver core provides the output current to the external load.

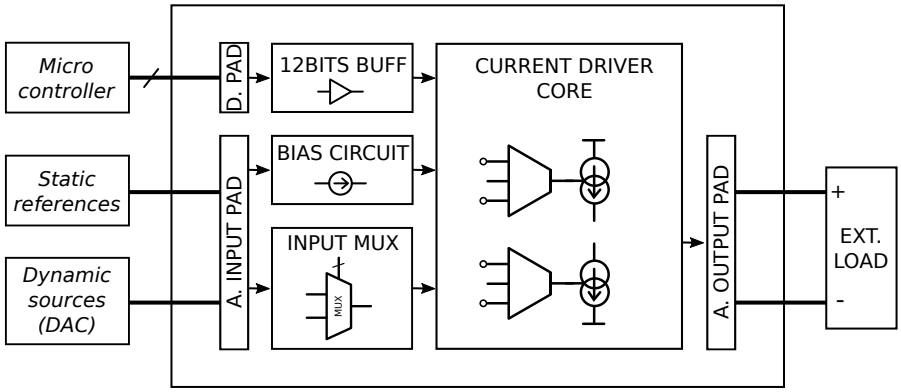


FIGURE 5.3 – System architecture diagram

5.2.2 Detailed description

I/O summary

Table. 5.1 gives the summary of external input and output signals required by the circuit to operate. The *Type* column tells if it is an analog (A) or digital (D) pin and the direction either it is an input signal (I) or an output signal (O).

To connect the I/Os with the package we used the pads given in the design kit. All pads come with a low-level model and therefore can be added in test benches for a more accurate simulation of the complete circuit. For the critical inputs, namely I0_IDAC_0 and I0_IDAC_1 we used analog pads with reduced ESD protection to limit parasitic capacitances brought to the current driver input node.

Name	Type	Function	Name	Type	Function
I0_IDAC_0	A.I	current input	CCBA[0:2]	D.I	CCII gain control
I0_IDAC_1	A.I	voltage input	CCBB[0:2]	D.I	CCII gain control
IN_REF_1UA	A.I	current ref.	INSEL[0:1]	D.I	select input
VREF_UP	A.I	voltage ref.	BREF	D.I	output short to ground
VREF_DN	A.I	voltage ref.	BSNK and $\overline{\text{BSNK}}$	D.I	output polarity control
H_LOADP	A.O	current output	BSRC and $\overline{\text{BSRC}}$	D.I	output polarity control
H_LOADN	A.O	current output			

TABLE 5.1 – I/O summary of the current driver

Bias circuit

The bias structure works with a static input reference current of 1 µA which is then amplified and spread in both N and P domain to provide four 5 µA static currents required by the NL-CCII in the driver core. The bias circuit also provides two voltages of 0.5 V and 1.3 V to polarize the cascode devices of the output current mirrors.

It is implemented using simple diode-connected current mirrors with unity NMOS transistor taken as 0.54/6 µm and PMOS transistor taken as 1.4/6 µm

Input multiplexer

The analog multiplexer on the input is here to select which pin is used to provide the DAC current. The input I0_IDAC_1 has only a low-resistance switch on the current path to activate/deactivate this pin. The other input I0_IDAC_0 includes a 8 kΩ resistor in series with the low-resistance switch. The resistor is placed to possibly drive this pin with a dynamic voltage source in order to generate the input current. With this configuration it is not possible to fully control and measure the current provided to the circuit but it allows to limits the effect of parasitic capacitance brought by the pad during transient characterization.

Current amplification

In the core (Fig. 5.4), the current amplification and distribution in both anodic and cathodic domains is built with complementary current mirrors implemented with the solution presented in section 4.2 of Chapter 4.

The same non-linear CCII is used for both NMOS and PMOS current mirrors. The two NL-CCIIs share the same threshold voltages, fixed at 0.7 V and 1.1 V, centred around $V_{DD}/2$. However each NL-CCII can have its gain independently tuned using the digital buses CCBA[0:2] and CCBB[0:2].

The NMOS current mirror provides the current to the PMOS mirror. Both type are sized to achieve similar drive voltage, and same level of accuracy. It gives equivalent unity

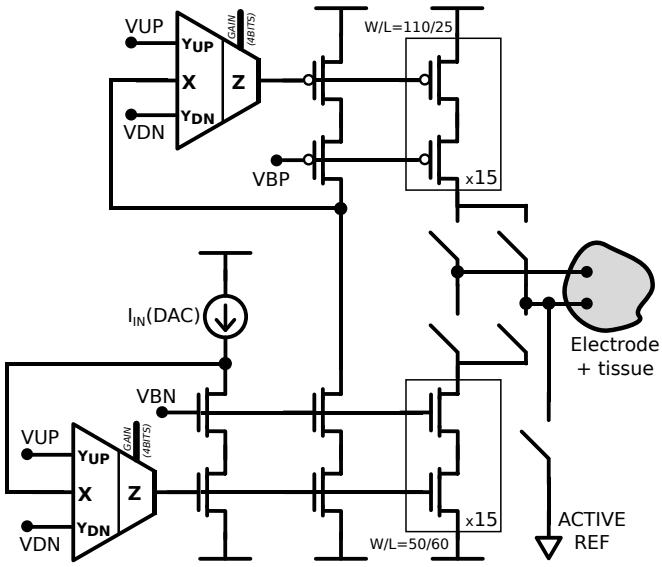


FIGURE 5.4 – Proposed architecture for the current driver core

transistors of 50/60µm for NMOS type and 110/25µm for PMOS type. The copy-ratio is equal to 15, leading to an ideal power efficiency $> 90\,\%$

The outputs of NMOS and PMOS current mirrors in the core are connected in a H-bridge configuration. In addition to the dynamic properties of the structure, built to drive various type of current wave, the H-bridge adds features that makes it suitable for typical neural stimulation patterns. It consists in a set of five switches to control the direction of the current flowing through the load. Several configurations can be applied according to the desired stimulation current shape.

For charge-balanced stimulation using the H-bridge feature, a precise timing for switch control is necessary. A design with care for charge injection errors is also required as the high level of output current involves large switches and thus a potentially significant amount of undesired charges can be stored in parasitic capacitances.

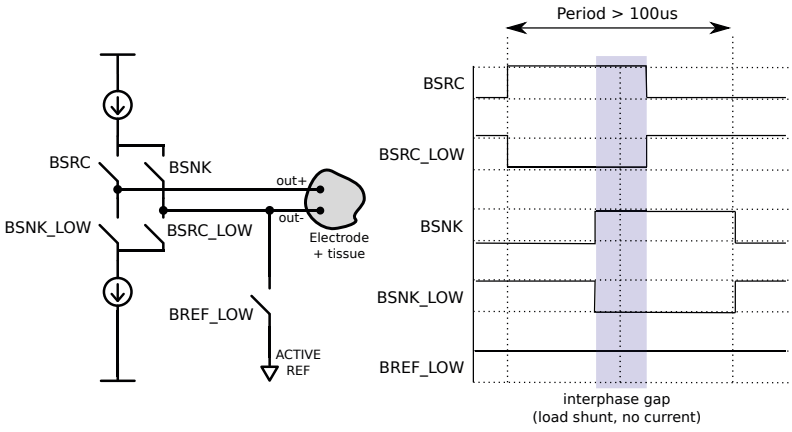


FIGURE 5.5 – Example of switching control of H-bridge to generate symmetric biphasic pulses with inter-phase delay

Fig. 5.5 shows an example of the switching sequence used to generate symmetric biphasic

pulse with inter-phase delay. The H-bridge also offers the possibility to characterise separately the NMOS and PMOS current mirrors to validate the proposed implementation.

5.2.3 Test and performance measurement

This section is dedicated to the evaluation of the current driver performances. All simulation results come from post-layout simulations with a full chip parasitics extraction. Off-chip signals are provided with ideal current or voltage sources. First simulations are run to characterize the speed, power and accuracy performances of each outputs. Then a use case example is given to illustrate the H-bridge functionality to generate a train of biphasic pulses with increasing magnitudes.

NMOS and PMOS current mirror characterizations

Table. 5.2 and Table. 5.3 summarize the speed, power and accuracy performances of the main current mirrors. Response time are given for both rising and falling edges and represent worst case values when simulating the system using classical corner models[1]. The power efficiency is calculated by taking the average ratio over one period of the power delivered to the load over the total power dissipated. Copy error measurements have been obtained using statistical models for devices and Monte Carlo simulations.

		NMOS CM		PMOS CM		average
bias	step	rising	falling	rising	falling	power efficiency
10 µA	±2 µA	728 ns	957 ns	927 ns	1198 ns	72.1 %
20 µA	±10 µA	688 ns	1108 ns	855 ns	1324 ns	77.3 %
30 µA	±20 µA	702 ns	1243 ns	843 ns	1459 ns	78.4 %
40 µA	±30 µA	747 ns	1328 ns	904 ns	1544 ns	78.9 %

TABLE 5.2 – Response time of both current mirrors for various bias levels and step magnitudes

		NMOS CM		PMOS CM	
bias	step	avg error	std	avg error	std
10 µA	±2 µA	0.201 %	0.047 %	0.212 %	0.042 %
20 µA	±10 µA	0.186 %	0.043 %	0.195 %	0.040 %
30 µA	±20 µA	0.183 %	0.041 %	0.156 %	0.033 %
40 µA	±30 µA	0.191 %	0.046 %	0.195 %	0.041 %

TABLE 5.3 – Measured systematic plus random copy error of both current mirror for various bias levels and step magnitudes

The main observation is that after the layout phase, the circuit shows performances that does not completely meet the target specification in terms of power efficiency ($> 80\,\%$) and

[1]Five corners with the classic definition are considered: typical corner (TYP), worst case speed (SS), worst case power (FF), worst case zero (SF) and worst case one (FS)

speed (response time $< 1\,\mu s$). Regarding the static errors, statistical simulation including post layout parasitics seems to predict that the current driver will meet the requirement over accuracy. Indeed measured copy error falls under the targeted 0.4 % limit and tends to support the decision to work with large but precise current mirrors coupled with power efficient speed boosting techniques. However this last assumption still needs to be further confirmed by silicon measurement on a sample of dies picked up at distant location on the wafer.

Biphasic pulse generation using the H-bridge

In this test we use a specific control sequence for the H-bridge to generate biphasic pulses with interphase gap. Pulse durations as well as interphase delays are set to 20 µs. The input current starts at 30 µA and increases by 15 µA each 80 µs to stops at 60 µA. To create the inter-phase gaps, anodic and cathodic outputs are periodically shorted using the H-bridge. This way we keep the outputs biased and avoid the output device to switch between open-circuit and driving conditions. The drawback is that during the interphase gap a residual offset current exists whereas we ideally expected no current flowing through the load. However the good matching properties of the structure ensure a minimal residual current level. Voltage and current waves are shown in Fig. 5.6.

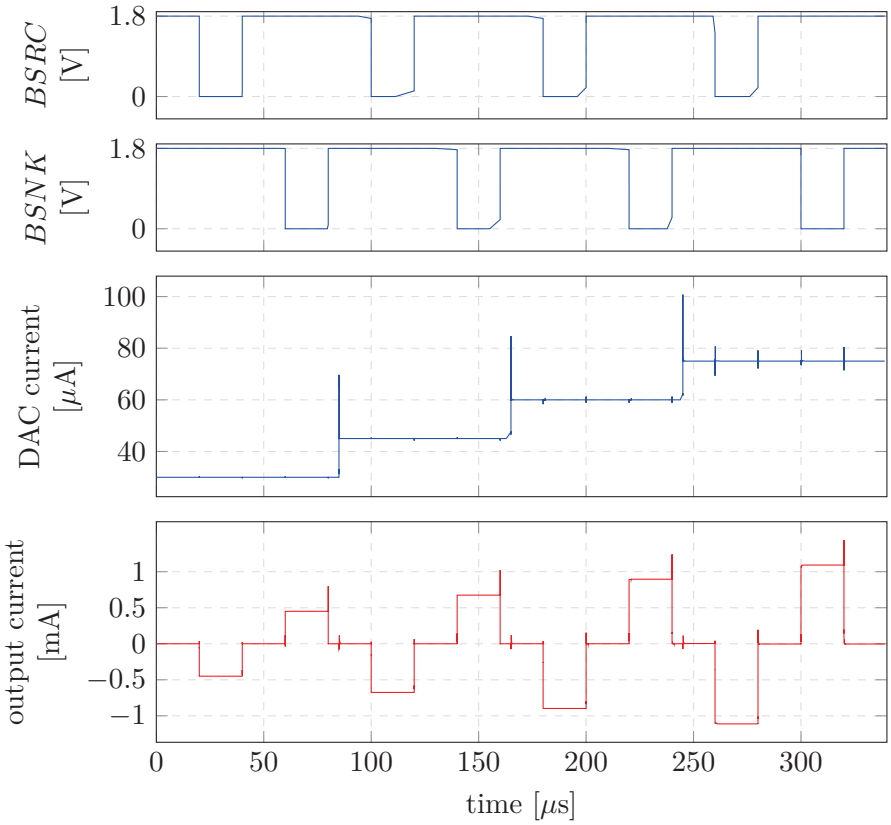


FIGURE 5.6 – DAC current, control signals of the H-bridge and output current for the generation of a pulse train with increased amplitude

To evaluate the safety of such pattern for electrical stimulation we measure the charge error introduced by the device imperfections. Charges injected and charges not recovered

are calculated by integrating the current over the total duration of the pulse train (340 µs). Charge measurement results are given Table. 5.4.

Average charge injected	Average charge not recovered	Relative charge error
125.2 nC	413.2 pC	0.330 %

Table 5.4 – Charge error measurement for the stimulation pattern shown Fig. 5.6

5.3 A configurable multipolar output stage architecture (TSMC Chip)

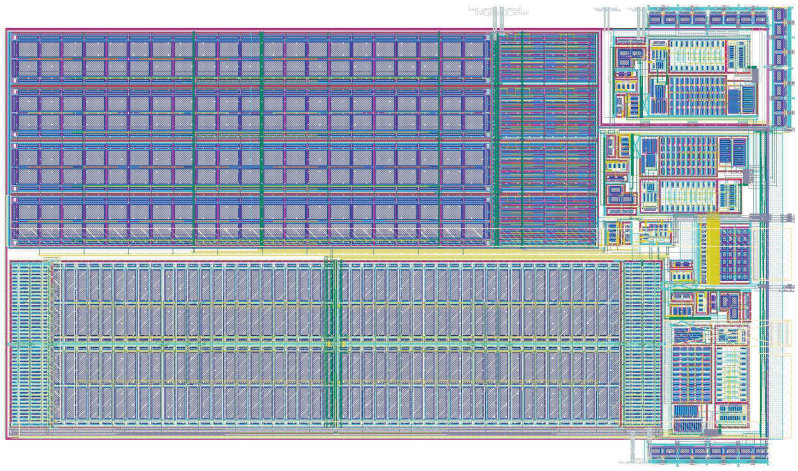


Figure 5.7 – Layout of the proposed implementation

5.3.1 Overview and general specifications

The circuit presented in this section has been designed using the TSMC standard CMOS 0.18 µm process. It includes the improved version of the current mirror with NL-CCII-based feedback presented in section 4.3 of Chapter 4. Beside the technology used, the main differences with the previous current driver are the bipolar configuration (2 anodic and 2 cathodic outputs), the possibility to configure the system to work as a bio-impedance driver and the use of smaller devices for the main current mirrors. The circuit has been sent to fabrication in June (2018) and should be delivered shortly by the manufacturer. Silicon measurements are not yet available to be integrated in this manuscript but we hope that they will be part of the results presented during the Ph.D. defence. Circuits testing is programmed for October (2018).

This output stage has been designed to provide an output current ranging from 100 µA to 2.3 mA at each pole in bipolar configuration or a current ranging from 200 µA to 5.6 mA in the monopolar configuration (2 poles shorted). When configured in bio-impedance driver the system can generate currents up to ±1 mA. Depending on the stimuli applied, the average response time ranges from 150 ns to 1 µs at a static power efficiency greater than

90 % and with maximum relative output error less than 0.4 % (corresponds to a resolution of 8 bits).

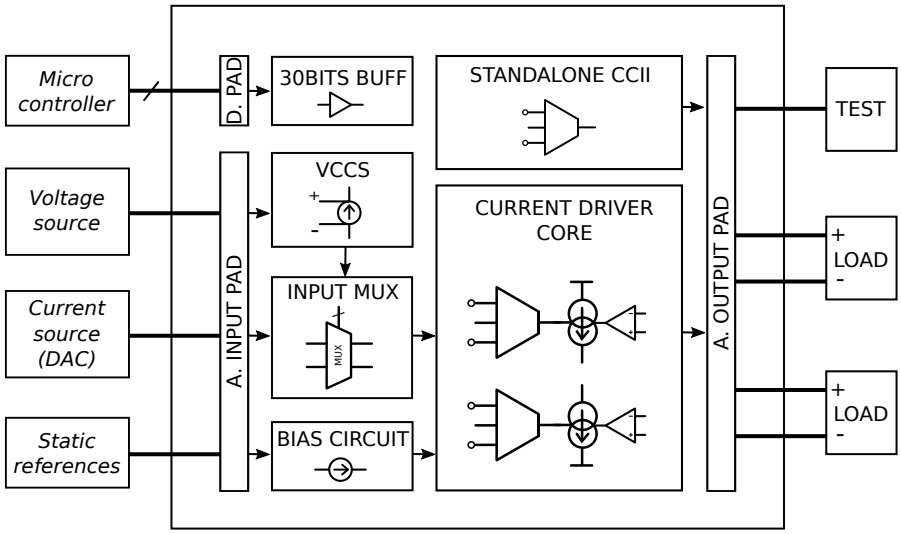


FIGURE 5.8 – System architecture diagram

A schematic view of the circuit architecture is shown Fig. 5.8. It comprises, digital buffers to be programmed by a micro-controller, a bias circuit to distribute static currents to components that need to be polarized, an integrated voltage controlled current source (VCCS) to generate the input current inside the chip, an analog current multiplexer to select between internal (from the VCCS) or external (DAC) input current but also to switch between *mirror* or *electrode configuration* (more details below), a stand-alone NL-CCII for charaterization and finally the current driver core providing the output currents.

5.3.2 Detailed description

I/O summary

The Table. 5.5 gives the summary of the 24 external input and output signals required by the circuit to operate. Three more 8 bits buses (24 inputs), not represented in this table are required to set the current conveyors gains. The *Type* column tells if it is an analog (A) or digital (D) pin and the direction either it is an input signal (I) or an output signal (O).

Pads available in the design kit were provided as black-boxes with no model. Hence for post-layout simulation we used a simple representation of the pad, consisting in an inductance of 1 nH for bonding wire in serial with a π-arrangement of one 1 mΩ resistor and two grounded capacitors of 100 fF.

Bias circuit

The bias structure works with a static input reference current of 5 µA and provides 8 output currents of 5 µA. It comprises 4 sinks and 4 sources at ±5 % to bias the NL-CCIIs and the OPAMPs in the driver core as well as the standalone NL-CCII used for test purposes.

Name	Type	Function
en_i_nmos_vccs	D.I	enable VCCS current to NMOS mirror
en_i_pmos_vccs	D.I	enable VCCS current to PMOS mirror
en_i_meas_vccs	D.I	enable VCCS current to pin for measurement
shift_dyn_vccs	D.I	change the VCCS output current range
vin_vccs	A.I	dynamic voltage input of the VCCS
vb_1v2_vccs	A.I	voltage reference for the VCCS
iout_meas_vccs	A.O	output current of the VCCS for measurement
vydn_test	A.I	upper threshold of the stand-alone CCII
vyup_test	A.I	lower threshold of the stand-alone CCII
inx_test	A.I	input current of the stand-alone CCII
outz_test	A.I	output current of the stand-alone CCII
iin_snk_5u	A.I	reference current for the bias circuit
en_indir	D.I	enable input current from external DAC
sel_indir	D.I	select between stimulation or bio-impedance mode
iin_stat	A.I	external static input current
iin_dac	A.I	external dynamic input current from DAC
vydnn	A.I	upper threshold of CCII for NMOS current mirror
vyupn	A.I	lower threshold of CCII for NMOS current mirror
vydnp	A.I	upper threshold of CCII for PMOS current mirror
vyupp	A.I	lower threshold of CCII for PMOS current mirror
iout_nmos_1	A.O	sunk output current of the first pole
iout_pmos_1	A.O	sourced output current of the first pole
iout_nmos_2	A.O	sunk output current of the second pole
iout_pmos_2	A.O	sourced output current of the second pole

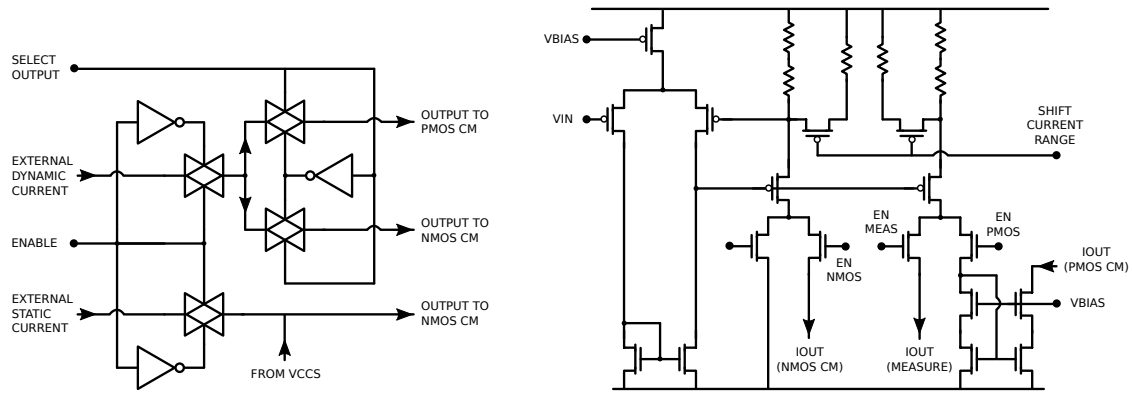
TABLE 5.5 – I/O summary of the current driver

(W/L) of NMOS and PMOS transistors are respectively sets to 1/2µm and 2.5/2µm. All output devices are used as single transistor tail current source to bias a differential pair. Target voltage compliance did not allow the use of cascode configuration for the bias structure.

Voltage controlled current source and input multiplexing

On the input current path, between the I/O pad and the core structure we integrated the analog current multiplexer shown in Fig. 5.9a. It has two roles: (i) enable/disable the inputs providing the static and dynamic off-chip currents, to isolate the circuit from the outside when using the VCCS. (ii) Redirect the provided off-chip dynamic current towards either the NMOS or PMOS current mirror in the driver core. The multiplexer is built with 4 identical pass-gates designed to be slow but with a low ON-resistance.

The voltage controlled current source (VCCS) shown in Fig. 5.9b has been implemented as a test resource for the dynamic evaluation of the current driver. It allows to generate the input current inside the chip to avoid the large parasitic capacitances brought by the I/O pads to the core inputs, which can penalize the system speed. The VCCS is built to be driven by an external voltage ranging from 1.2 V to 1.6 V to generate currents from 20 µA to 110 µA. Three outputs are available, two of them are connected to the NMOS and PMOS



(A) (B)

FIGURE 5.9 – Schematic of the analog current multiplexer (A) and of the voltage controlled current sources (B)

current mirrors in the core, the last one is connected to an output pad to measure amplitude of the current generated outside the chip. Each output can be digitally enabled/disabled. An other switch is used to shift and reduce the current range (from 7 µA to 45 µA) to generate currents with smaller amplitude but with better precision. It is implemented using a single stage OTA regulating a common-source amplifier. The current is generated by forcing the voltage across the resistors to be equal to the input voltage externally provided. The structure allows to supply a current to the driver core while measuring at the same time a copy of this current on the pin dedicated to the measure. At minimum current, the VCCS shows relative error between the NMOS and measure outputs of $0.94 \pm 0.71\,\%$. At maximum current, the error goes down to $0.21 \pm 0.16\,\%$. The response time to an input step in found to be in the order of several dozen of ns.

Core of the current driver

The proposed core for this output stage is shown Fig. 5.10. It comprises two complementary current mirrors with two separated outputs for each. The copy ratios are fixed to 20 for both anodic and cathodic outputs. The topology selected for the main current mirrors is the NL-CCII IRRC CM presented in section 4.3 of Chapter 4.

Identical NL-CCII are used for the NMOS and PMOS current mirrors. The structure has been presented in Fig. 4.18. To maximize the input and output compliances we choose to apply different thresholds to the two current conveyors. Typical values are fixed at 0.6 V and 0.8 V for the NMOS current mirror and 1 V and 1.2 V for the PMOS type. Voltages are applied from outside the chip. There is also separated digital buses for a more precise gain tuning. For each NL-CCII, a different current gain can be set for the cases where the conveyor absorbs or injects current on the mirror gates. This allows to compensate differences observed in the response time at large-signal between falling and rising edges.

Sizes of unity transistors composing the main current mirrors are given in Table. 5.6. The layout strategy adopted to draw the large current mirrors was to divide them in four smaller matched structures with intermediate dummy devices, and then to arrange these structures according to common centroid layout rules. With this solution, depicted in

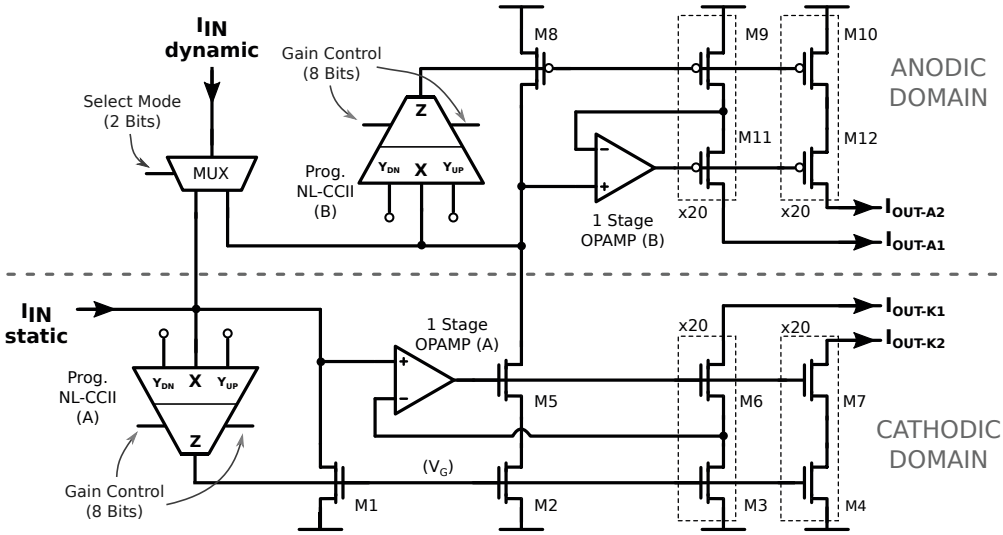


FIGURE 5.10 – Proposed output stage architecture

Fig. 5.11, we expected to average both local mismatch errors and errors that occur at die scale.

	NMOS (M1-M7)	PMOS (M8-12)
mirroring devices (µm)	3.75 / 13.5	8.45 / 6.70
cascode devices (µm)	3.75 / 0.18	8.45 / 0.18

TABLE 5.6 – Sizes of unity transistors in the main current mirrors

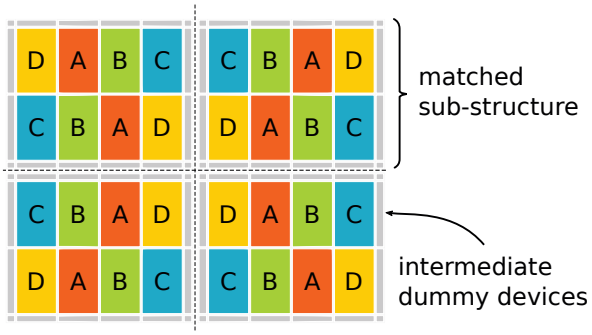


FIGURE 5.11 – Layout strategy for the main current mirrors

System configuration

As mentioned before, this current driver comes with various levels of configurability. First, we have the NL-CCII gain that can be digitally set to balance the speed during rising/falling edges or to optimize the dynamic power dissipated according to the speed required by the application. The possible gain values range from 2 to 20. Configuring the conveyor gain requires 8 bits (B[0:7]) shared into 2 buses. The current amplification follows the equations below, I_Z is the output current and I_X represents the input current.

$$I_Z = I_X\,(2 \times B0 + 4 \times B1 + 8 \times B2 + 12 \times B3) \qquad \text{for positive } I_X$$
$$I_Z = I_X\,(2 \times B4 + 4 \times B5 + 8 \times B6 + 12 \times B7) \qquad \text{for negative } I_X$$

Through the current multiplexer, the system can be configured in two different modes: the *mirror* configuration or the *electrode* configuration. Fig. 5.12 gives a simplified view of the

current paths in both configuration, only one pole is represented but the other one shows similar behaviour.

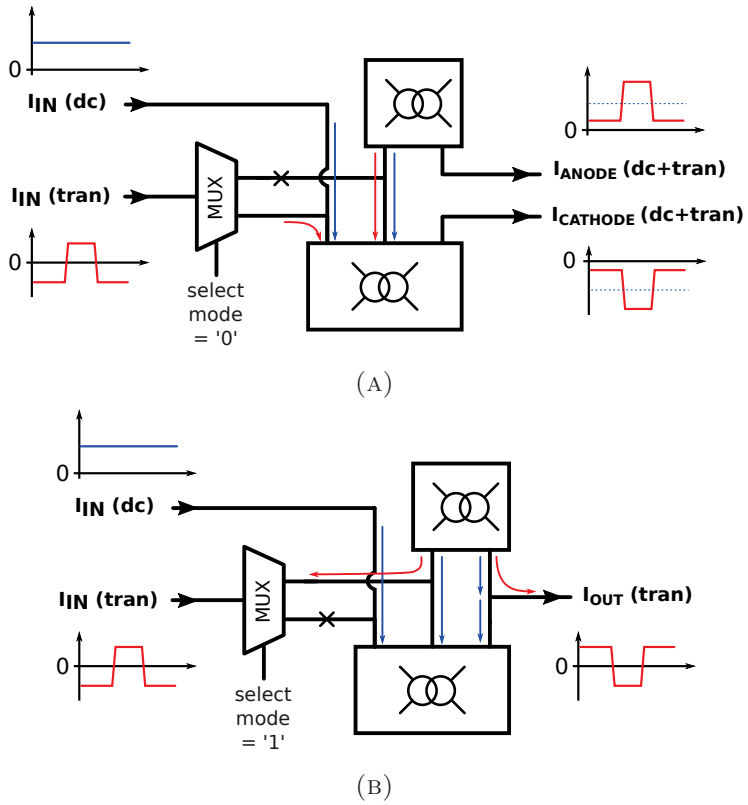


FIGURE 5.12 – Current paths and resulting signals in both *mirror* configuration (A) and *electrode* configurations (B)

In the *mirror* mode, static and dynamic input currents are supplied to the main NMOS current mirror, anodic and cathodic outputs drive the same current but with inverse polarity. In this mode the circuit can be seen as a current buffer/amplifier. When coupled with an H-bridge similar to the one presented in the previous section (5.2) we retrieve the possibility to generate classical charge-balanced biphasic pulses found in neural stimulation.

The system is put into the *electrode* configuration by shorting the anodic with the cathodic outputs and by redirecting the dynamic current to the main PMOS current mirrors. The NMOS mirrors keep driving the static current and supplying a copy to the PMOS one. This way we subtract the static current at the output node and only the dynamic component is provided to the load. Resulting in charge-balanced current wave centred around 0. Residual DC current depends on the matching between the NMOS and PMOS structure, errors on the amplitudes of the dynamic components depends solely of the characteristics of the PMOS mirrors.

5.3.3 Test and performance measurement

This section is dedicated to the evaluation of the current driver performances. First, the circuit is placed in its *mirror* configuration to evaluate the speed and accuracy of each output separately. We will examine in details the relative errors found between anodic and

cathodic currents but also between the two outputs of a same domain. Then, the circuit is configured in the *electrode* mode, where we will examine the residual DC current, the charge error and the linearity with practical current waves found in neural stimulation or in bio-impedance analysis.

All simulation results come from post-layout simulations with a full chip parasitics extraction. Off-chip signals are provided with ideal current or voltage sources. For all current analog input and output of the system we placed a pad model between the ideal source and the actual nodes.

System in the mirror configuration

The integrated voltage controlled current source is here disabled and inputs are provided off the chip. Thresholds for the non-linear current conveyors are fixed at 0.6 V-0.8 V for the NMOS current mirror and fixed at 1 V-1.2 V for the PMOS type. By default, same symmetrical current gain of 8 is set for both current conveyors.

The circuit is stimulated with several steps of various amplitudes, ranging from ±500 nA to ±50 µA while biased at different level across the input current range, starting from 5 µA up to 110 µA. Stimuli cases are summarized in Table. 5.7.

#	name	bias	step	#	name	bias	step
1	bias1-pulse1	10 µA	±0.5 µA	9	bias4-pulse1	70 µA	±0.5 µA
2	bias1-pulse2	10 µA	±5 µA	10	bias4-pulse2	70 µA	±2 µA
3	bias2-pulse1	30 µA	±0.5 µA	11	bias4-pulse3	70 µA	±20 µA
4	bias2-pulse2	30 µA	±2 µA	12	bias5-pulse1	90 µA	±0.5 µA
5	bias2-pulse3	30 µA	±20 µA	13	bias5-pulse2	90 µA	±2 µA
6	bias3-pulse1	50 µA	±0.5 µA	14	bias5-pulse3	90 µA	±20 µA
7	bias3-pulse2	50 µA	±2 µA	15	bias6-pulse1	110 µA	±0.5 µA
8	bias3-pulse3	50 µA	±20 µA	16	bias6-pulse2	110 µA	±2 µA
				17	fullrange-pulse	60 µA	±55 µA

TABLE 5.7 – Stimuli summary

► *Comparison between post-layout and typical simulation results.*

The first result is the measurement of performances reduction due to the layout decisions. In Fig. 5.13, we compare the response time at 0.4 % and the relative static current error (no mismatch) obtained by simulation of the typical circuit and by simulation of the circuit after post-layout parasitics extraction including pads. This evaluation does not take into account random fluctuations or process gradients. Measurement results are given for only one output of the main NMOS current mirror.

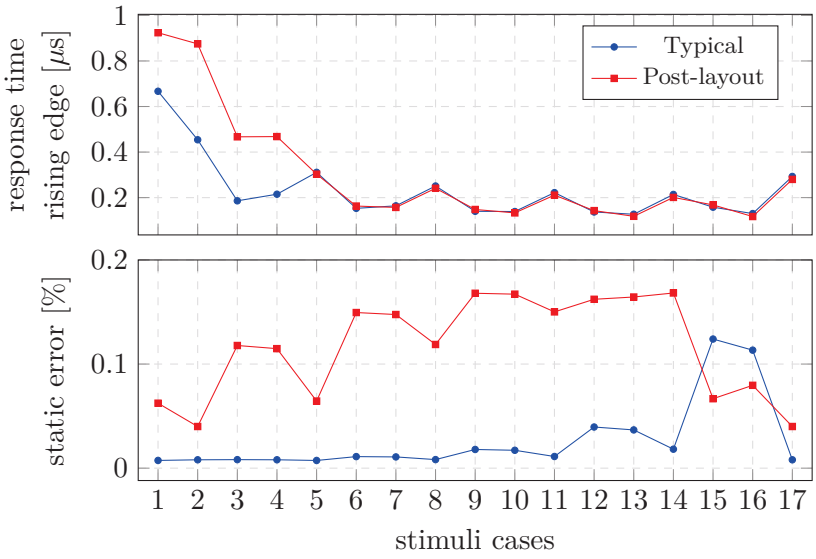


FIGURE 5.13 – Comparison of typical and post-layout simulation

Regarding the speed, we note that post-layout simulation shows higher response time at low bias levels (stimuli 1 to 4). We discussed in Chapter 4 the effect of undesired conveyor activation under slow residual oscillations of the input node. The switching mechanism in the CCII introduces small current spikes at its output when the current to convey is too small to be properly amplified. These spikes introduce short transient errors that can be greater than our target of 0.4 % error and consequently delay the last time for the system to settle within the tolerance range (±0.4 %) of the final value. The reason for these residual oscillation and thus for the associated spikes to happen is the shift of the input pole toward lower frequency under the pad and interconnect parasitic capacitance. The solution is to decrease the CCII gain or to use the integrated VCCS for system speed characterisation at low bias level.

As expected the static output error is almost null for the typical circuit when considering no mismatch between devices. But as we can see on the error plot for post-layout simulation, estimation of the layout impact on performances shows that a small but not negligible amount of systematic error ($< 0.2\,\%$) is due to the interconnect..

▶ *Measurement of systematic and random errors*

We used the post-layout extracted netlist and statistical models for devices to evaluate the overall current driver static errors. We measure, the relative errors between actual measured current and the expected nominal value for the 2 outputs of the first pole and the relative difference current between anodic and cathodic outputs.

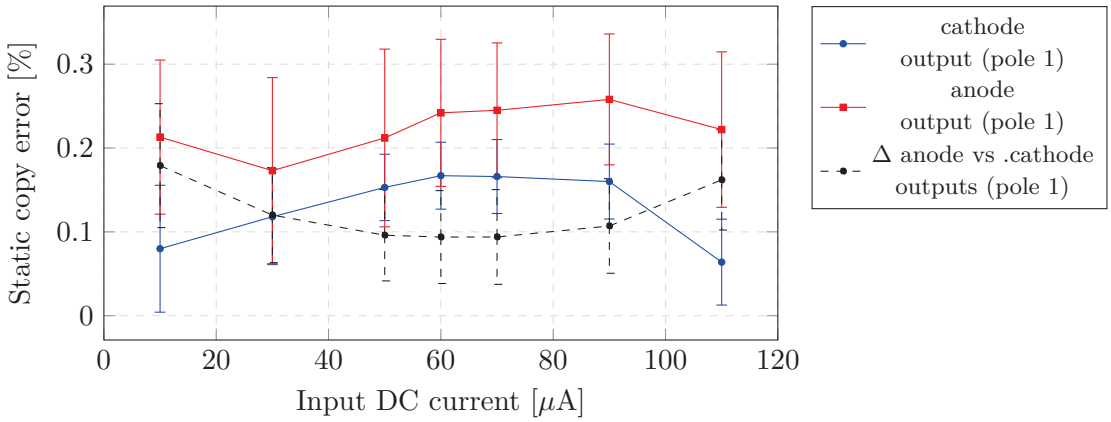


FIGURE 5.14 – Relative current copy error of both anodic and cathodic current mirrors, and relative difference between the anodic and cathodic output currents. Error bars represent the standard deviation (σ) obtained after a 200 runs monte-carlo simulation.

► *Measurement of speed performance*

Fig. 5.15 shows measurement results of the response time at 0.4 % and the power efficiency of the circuit when current conveyor gains are set to the default value of 8. Inside the NL-CCIIs, the same gain is applied for positive and negative currents. The power efficiency is defined as the average ratio between power delivered to the load and total power consumed during one period of the input pulse.

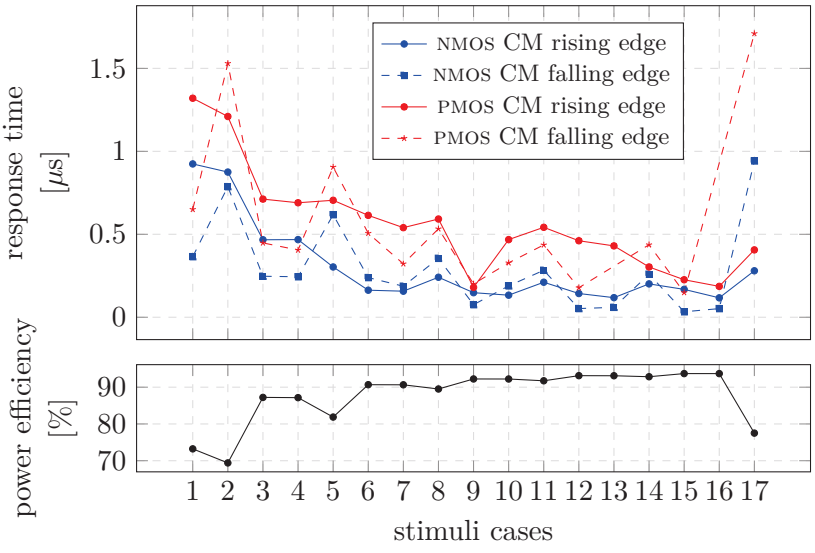


FIGURE 5.15 – Response time at 0.4 % for both NMOS and PMOS current mirror with default current conveyor gain of 8 and power efficiency for the 17 stimuli cases

Most of measured response times fall under the 1 µs target and goes down to ≈ 100 ns for best cases reported. Exceptions are located at low bias level (stimuli 1, 2) and during falling edge of the full-range input signal (stimuli 17). These cases are partly explained by the intrinsic non-linear characteristics of MOS devices,which are naturally slower at low

bias level. The current mirrors have a reduced initial bandwidth and NL-CCIIs regulating the speed show less reactivity. Best reported cases of response time also coincide with best power efficiency, which is found greater than 90 % for stimuli 6 to 16.

For several stimuli, we observe a significant gap between rising and falling edge, which results in asymmetric output pulses. In addition, we also note speed differences between anodic and cathodic outputs, which can introduce error of charge-balance during electrical stimulation. By configuring different gain for positive and negative currents inside a NL-CCII we can compensate differences observed between rising and falling edges. By configuring different gain between current conveyors controlling the main NMOS or PMOS current mirrors, we can compensate speed deviation that exists between anodic and cathodic outputs.

Table. 5.8 shows the gain tuning applied to re-symmetrize the current driver for a pulse of ±20 µA when biased at 30 µA (stimuli case 5). The expected output currents are four identical square waves with amplitude ranging from 200 µA to 1 mA. Fig. 5.16 gives the measured deviations in response time before and after gain correction. Comparisons are made between rising a falling edge for a same output and between anodic (A) and cathodic (K) outputs.

	NL-CCII A (NMOS CM)	NL-CCII B (PMOS CM)
Positive current gain	8 → 6	8 → 12
Negative current gain	8 → 12	8 → 18

TABLE 5.8 – NL-CCII gain tuning for speed balance

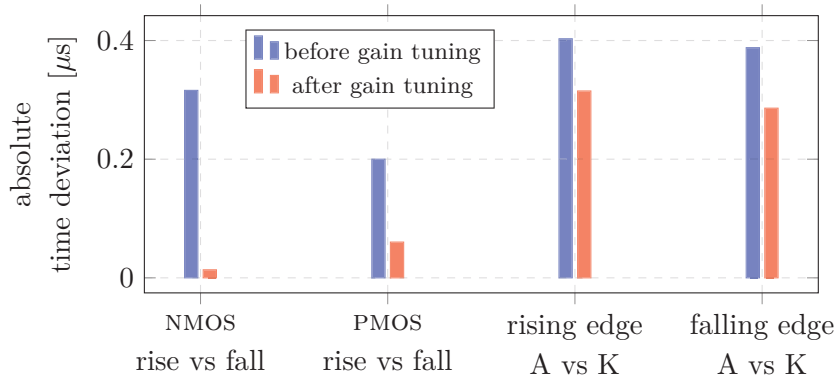


FIGURE 5.16 – Time deviation between rising a falling edge for a same output and between anodic (A) and cathodic (K) outputs, before and after gain tuning

In the previous example of gain tuning, time differences between rising and falling edge have been reduced by a factor 10, from several 100 ns to several 10 ns. Gain tuning has lower effect on anodic/cathodic time differences. As in the *mirror* mode, the NMOS mirror provides the current to the PMOS type, response time of anodic outputs are the sum of the delays introduced by both NMOS and PMOS current mirrors. This is one limitation of

the architecture when configured in this mode. This issue does not concern the *electrode* configuration.

System in the electrode configuration

For each pole, anodic and cathodic outputs are shorted. The external DAC current is redirected to the PMOS current mirror by the analog multiplexer. Both NMOS and PMOS types drive the static current also provided off-chip. The integrated voltage controlled current source is still disabled. Thresholds for the non-linear current conveyors have not changed and gains are set to the value applied after system tuning (see Table. 5.8).

▶ *Characterisation of accuracy, speed and power efficiency*

The circuit is driven with several step of various amplitudes, but different from the ones used in the *mirror* configuration. To achieve a power efficient neural stimulation, bias levels are adapted to signal amplitudes. Stimuli cases for the following tests are summarized in Table. 5.9.

#	name	bias	step	#	name	bias	step
1	bias1-pulse1	10 µA	±2 µA	6	bias3-pulse2	50 µA	±20 µA
2	bias1-pulse2	10 µA	±5 µA	7	bias3-pulse3	50 µA	±40 µA
3	bias2-pulse1	30 µA	±10 µA	8	bias4-pulse1	70 µA	±20 µA
4	bias2-pulse2	30 µA	±20 µA	9	bias4-pulse2	70 µA	±40 µA
5	bias3-pulse1	50 µA	±10 µA	10	fullrange-pulse	60 µA	±55 µA

TABLE 5.9 – Stimuli summary

In this mode, with static but no dynamic current supplied, currents at the outputs are expected to be null. However because of small systematic and random differences that exist between NMOS and PMOS mirrors we observe a residual static current. Fig. 5.17 presents the measure of this residual DC current across the bias current range and for different values of output voltage.

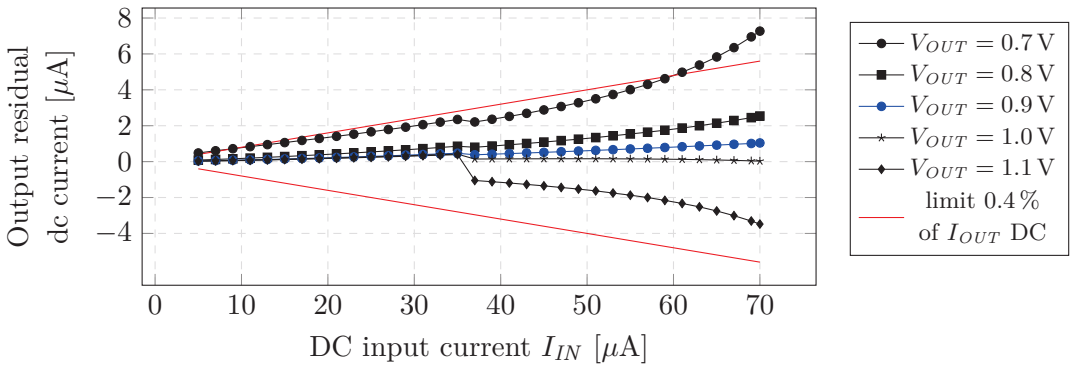


FIGURE 5.17 – Residual static current at different output voltage values

As expected, the residual current increases when the bias level increases. However, we note that this residual error falls under the limit of 0.4 % when compared to the static current biasing the outputs. This is coherent with previous accuracy measurement results. This

limit defines the output compliance of the current driver in *electrode* mode. Minimum and maximum voltage requirements are specified at 0.7 V and 1.1 V.

Fig. 5.18 shows the measurement of response times, power efficiencies, time deviations between rising/falling edges and relative pulse magnitude errors for the ten stimuli cases presented in Table. 5.9. We note that, the higher the bias level the higher the speed and best average power efficiencies are achieved when the step amplitude is maximised according to the bias level. In the next part we will see how these characteristics affect the specification of the output stage in practical contexts of a neural stimulation or a bio-impedance analysis.

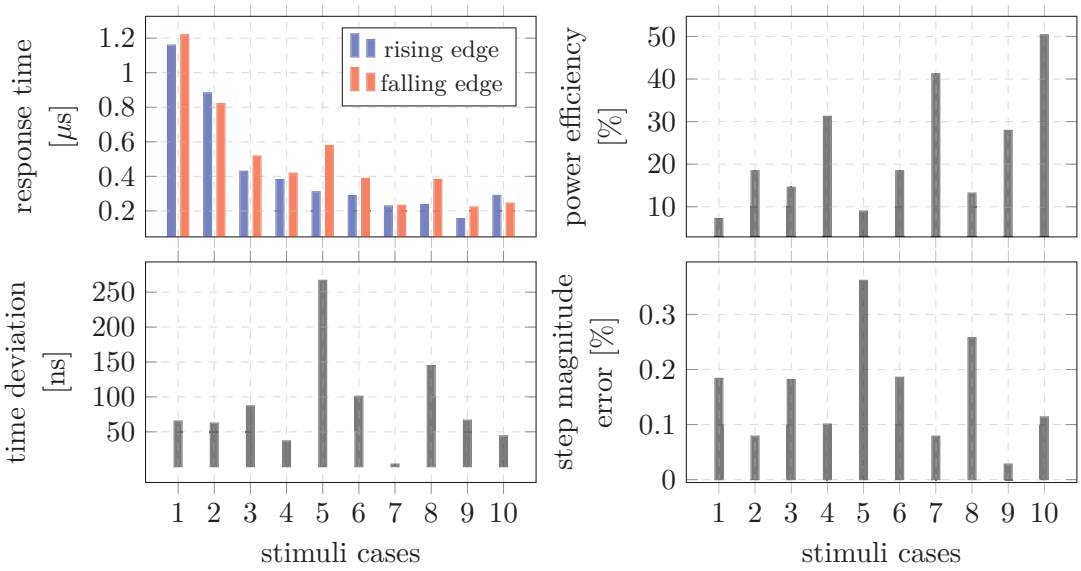


FIGURE 5.18 – Response time, time deviation between rising/falling edges, power efficiency and relative step magnitude error in electrode configuration

► *Measure with practical biomedical signals*

The stimulation signal parameters used here as an example of practical application come from a study published in Nature (Deprez et al., 2018). In their work authors investigate different types of pulse for brain stimulation to initiate leg movements on rat subject. The stimuli we decide to reproduce consists of a biphasic pulse with, a duration of 50 µs for each phase, an amplitude of 500 µA for both positive and negative current and an inter-phase gap of 50 µs between anodic and cathodic currents. The signals used as an example of bio-impedance measurement is a single tone sine wave of 300 µA magnitude at 50 kHz and 300 kHz. Many physiological models use electrical impedance measurements at the particular frequency 50 kHz to predict human body composition. Authors in (Pietrobelli et al., 1998) have shown that going up to 300 kHz adds information for more accurate predictions.

In the following test we will focus on charge error evaluation, which reflect the amount of charge left in the electrode tissue interface. For the sine stimuli we will also evaluate the linearity of the driver by measuring the THD and SFDR from the output current spectrum.

Fig. 5.19 shows one unity biphasic pulse of the input DAC current applied for neural stimulation and the resulting output current supplied to the load. In Table. 5.10, are reported charge measurement[2]over one period (250 µs). The first column gives the total amount of charges injected during the first phase, which are then ideally recovered during the second phase with inverse polarity. We also measure the amount of charge left (or not recovered) due to current driver imperfections, which are in this case less than 0.4 % of the total amount of charges injected. These quantities are found to be proportional to the stimulation time and number of biphasic pulses used.

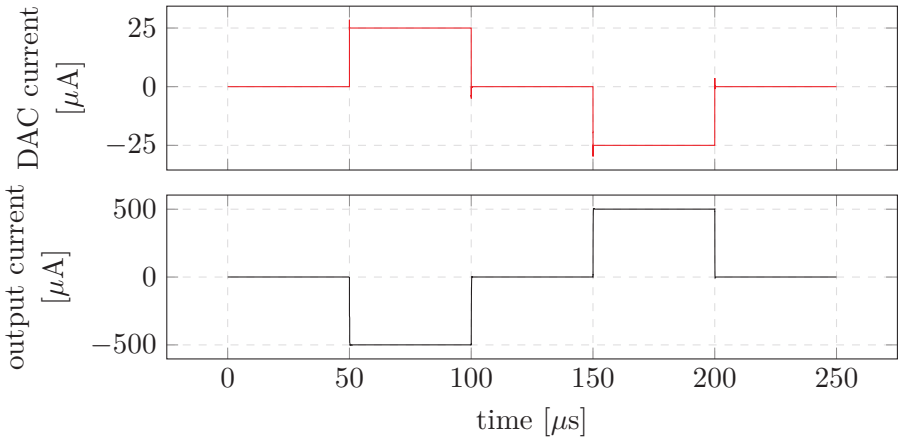


FIGURE 5.19 – External DAC current and output current of the first pole when driven with practical neural stimulation signal

Charge injected		Charge left		Relative charge error	
min	max	min	max	min	max
25.03 nC	25.05 nC	72.5 pC	91.4 pC	0.289 %	0.365 %

TABLE 5.10 – Total amount of charge injected (and then recovered), amount of charge left in the electrode/tissue interface and its relative value, measured over 1 period of the stimulation pattern shown in Fig. 5.19.

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In Fig. 5.20 we see the spectrum of DAC and output currents when the system is driven with the sine waves for bio-impedance analysis. We observe that the non-linear behaviour of the speed control loop introduces some harmonic components, resulting in a THD of −37 dB for the 50 kHz signal which reduces to −32 dB for the 300 kHz signal as reported in Table. 5.11. Another observation is that the relative charge error is less than 0.4 % at 50 kHz but goes up to 4 % for the 300 kHz wave. This is due to the fact that the amount of charge injected during one period decreases when the input frequency increases but the amount of charge not recovered stay constant.

[2]Results are minimum and maximum values of CMOS corners simulation

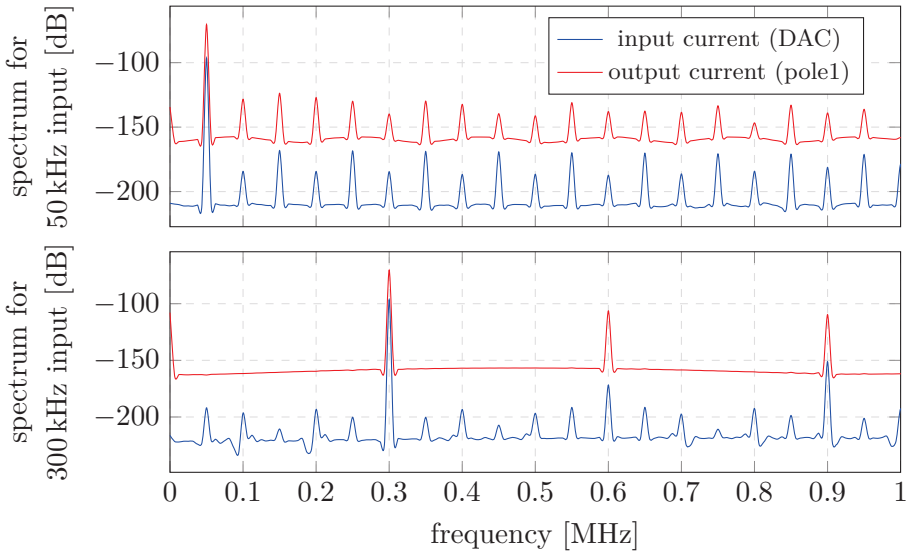

FIGURE 5.20 – Spectrum of external DAC current and output current of the first pole when driven with practical bio-impedance analysis signal

	THD (dB)		SFDR (dB)		Charge injected (nC)		Charge left (pC)		Charge error (%)	
	min	max	min	max	min	max	min	max	min	max
50 kHz	-37.6	-37.2	58.1	53.4	1.91	1.92	3.6	7.1	0.191	0.370
300 kHz	-32.2	-31.8	36.4	35.8	0.319	0.321	11.7	13.7	3.4	3.9

TABLE 5.11 – THD, SFDR, total amount of charge injected (and then recovered), amount of charge left in the electrode/tissue interface and its relative value, measured over 1 period of the BIA patterns.

5.4 Literature comparison and discussion

This last section is dedicated to the performances evaluation of the current drivers presented in this chapter against previous published work. The circuit introduced in section 5.2 is referred as the AMS circuit, the last one introduced section 5.3, is referred as the TSMC circuit. For a clearer comparison we have separated published work in three categories, namely the neural stimulator output stages, the bio-impedance analysis drivers and the low-level current sources. The last category includes elementary components such as current conveyors, current amplifiers or enhanced current mirrors.

5.4.1 Comparison with neural stimulators

In Table. 5.12 we compare the two proposed current drivers with performances of previous published output stages of neural stimulation chips.

What we note is that solutions with digital calibration ((Greenwald et al., 2017), (Liu et al., 2014), (Luo and Ker, 2016)) show the minimal charge error during a stimulation

cycle despite the fact that they have higher static current errors. For the proposed current drivers, we adopted a different strategy which consists in minimizing errors structurally instead of using additional digital resources and calibration phases. It enables to achieve lower power consumption and lower die area. This is particularly true for the TSMC chip, the AMS circuits may have been over-sized and thus still have large area. However compared to the size of the other full-analog solution in (Giagka et al., 2015), the die area of the core is still lower.

5.4.2 Comparison with bio-impedance analysis drivers

In Table. 5.13 we compare the two proposed current drivers with performances of previous published current drivers dedicated to bio-impedance measurements.

Bio-impedance analysis is not the main target for the proposed output stages and we see that due to the non-linear characteristic the THD is not as good as with the full-differential OTA solutions presented in (Constantinou, Bayford, and Demosthenous, 2015) and (Lamlih et al., 2018). However, measured bandwidth and power efficiency show that our solutions can drive signals in similar frequency ranges with less power, which makes it a potential candidate for implanted bio-impedance measurement devices. An other remark is that authors in (Constantinou, Bayford, and Demosthenous, 2015) and (Lamlih et al., 2018) do not address static current errors neither charge errors during a measurement cycle, whereas our solutions are specially designed to minimize these errors.

5.4.3 Comparison with low-level current sources

In Table. 5.14 we compare the performances of the main current mirrors in the proposed current driver with performances of previous published topologies of enhanced current mirrors, current conveyors or current amplifiers. Because each structure has a different application, we use the following figure-of-merits to ease the comparison.

$$\text{FOM 1} = \frac{\text{power efficiency}}{\text{static errors} \times \text{response time}} \qquad \text{FOM 2} = \frac{\text{power efficiency} \times \text{bandwidth}}{\text{static errors}}$$

$$\text{FOM 3} = \frac{\text{power efficiency}}{\text{response time}} \qquad \text{FOM 4} = \text{power efficiency} \times \text{bandwidth}$$

Structures that obtain a high score to FOM 1 and FOM 2 are structures that propose the best optimization of speed and accuracy with an efficient use of the power dedicated. FOM 3 and FOM 4 traduce the relation between speed and power only.

The proposed current driver realized with the TSMC technology shows the best scores to metrics FOM 1 and FOM 2 when compared to previous published work. This means that we achieve our objective to propose a current source architecture that breaks the limit of the classical *speed-power-accuracy trade-off*.

5.5 Conclusion

In this last chapter, the design solutions discussed in Chapter 4 are deployed and validated with the realisation of two circuits in 0.18 µm CMOS technology (AMS and TSMC). Cores of the circuits are two examples of output stages dedicated to neural stimulation chips. The neural stimulation is a popular bioengineering technique found in the majority of advanced prosthesis (i.e. pacemaker, cochlear implants, retinal implants ...) which imposes very strong constraints on the sub-parts in charge of the stimulation current generation. Thus, it constitutes a good candidate to evaluate our solutions in a practical context.

The main objective of the first circuit (section 5.2), fabricated in the AMS technology, was to verify the feasibility on silicon of the non-linear current-mode feedback operation. Another expected outcome was the validation of the design strategy adopted which relies on low-power speed improvement techniques applied to very large current mirrors with low variability and precise current copy. However, because at the end we did not have the chips, we have only tested the circuit in simulation

The second circuit (section 5.3), fabricated in TSMC technology, is an example of an output current generation stage of a bipolar (2 anodic and 2 cathodic outputs) neural stimulation chip. The circuit interfaces with a micro-controller and offers different levels of configurability. It enables the possibility to adjust independently the response time of each of the 4 outputs for a fine tuning of timings. On the other hand, the system proposes two modes of operation: the *mirror mode* in which each outputs drives the same signal (with inverse polarity between anodes and cathodes) and the *electrode mode* where anodic and cathodic outputs are shorted to generate symmetrical current waves with no static components. In this last mode, we have seen that the circuit can also be used as a current driver for bio-impedance analysis, which is another important domain in bioengineering. Simulated performances show that the circuit is able to provide a current ranging from 100 µA to 2.3 mA simultaneously at each output, with a response time ranging from 150 ns up to 1 µs depending on the signal amplitude. The average power efficiency is found to be greater than 90 % for a maximum relative current error less than 0.4 %.

To confirm the scientific relevance of the fabricated circuits, we have compared their performances to previously published work that fall in the three following categories: the neural stimulators, the bioimpedance analysis current drivers and the advanced current-mode sub-circuit architectures, such as current conveyors, current amplifiers and enhanced current mirrors. Comparison results demonstrate that it is actually possible to outperform the present limit of the *speed-power-accuracy trade-off* with the design strategy and the new active-input current mirror topologies we have proposed.

	This work (AMS)	This work (TSMC)	(Greenwald et al., 2017)	(Liu et al., 2014)	(Sit and Sarpeshkar, 2007)	(Luo and Ker, 2016)	(Giagka et al., 2015)
year	2017	2018	2017	2014	2007	2016	2015
techno	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm	0.18 µm
type	NL-CCII based	NL-CCII based	DAC + calib	DAC + calib	OTA + switched cap	current mem. + calib	cascode CM
output range	up to 0.9 mA	up tp 5.6 mA	up to 250 µA	up to 2 mA	up to 1 mA	up to 3 mA	up to 1 mA
static error	0.2 %	<0.4 %	-	0.7 %	0.7 %	0.25 %	0.94 %
charge error	0.33 %	0.34 %	0.3 %	0.05 %	0.4 %	0.25 %	2.75 %
power consumption	45 µW to 126 µW	63 µW to 252 µW	-	136 µW	750 µW	150 µW	114 µW
die area	0.192 mm^2	0.062 mm^2	0.072 mm^2	0.069 mm^2	1.45 mm^2	≈0.63 mm^2	0.36 mm^2

Table 5.12 – state-of-the-art for neural stimulator and proposed current driver performances

	This work (AMS)	This work (TSMC)	(Constantinou, Bayford, and Demosthenous, 2015)	(Lamlih et al., 2018)
year	2017	2018	2015	2018
techno	0.18 µm	0.18 µm	0.35 µm	0.18 µm
type	NL-CCII based	NL-CCII based	full-diff OTA	wideband full-diff OTA
output range	±525 mA	±1 mA	±1 mA	±600 µA
output impedance			>1 MΩ	>79 MΩ
bandwidth	<5 MHz	<15 MHz	1 MHz	10 MHz
THD	-	−37 dB	−60 dB	−50.4 dB
power efficiency	78 %	91 %	<50 %	<50 %

Table 5.13 – State-of-the-art for BIA current driver and proposed current driver performances

	This work (AMS)	This work (TSMC)s	(Mita, Palumbo, and Pennisi, 2003)	(Palmisano, Palumbo, and Pennisi, 2000)	(Esparza-Alfaro, Pennisi, et al., 2014)	(T. Chen and Gielen, 2007)	(Esparza-Alfaro, Lopez-Martin, et al., 2012)	(Vajpayee et al., 2010)	(Torralba et al., 2003)	(Zeki and Kuntman, 2000)
year	2017	2018	2003	2000	2014	2007	2012	2010	2003	2000
techno	0.18 µm	0.18 µm	0.35 µm	1.2 µm	0.5 µm	0.18 µm	0.5 µm	0.25 µm	0.35 µm	0.51 µm
type	NL-CCII based	NL-CCII based	class AB CCII	class AB COA	class AB VF-COA	DAC + SSPA calib	class AB regulated casc.	improved regulated casc.	improved high-swing casc.	class AB self casc.
output range	up to 0.9 mA	up to 5.6 mA	±1 mA	±7 mA	±0.5 mA	16 mA	200 µA	300 µA	20 µA	570 µA
static error	0.2 %	<0.4 %	0.5 %	2.2 %	-	?0.31 %	-	5 %		0.5 %
response time	747 ns	363 ns	-	-	138 ns	-	-	200 ns	<100 ns	-
bandwidth	<5 MHz	<15 MHz	1.2 MHz	1.2 MHz	0.6 MHz	2 MHz	98 MHz	398 MHz	122 MHz	29 MHz
power consumption	70 µA	140 µA	173 µA	200 µA	84 µA	116 mA	80 µA	199 µA	12 µA	20.5 µA
power efficiency	78 %	91 %	91 %	92 %	59 %	14 %	70 %	33 %	38 %	49 %
FOM 1	522	626	-	-	-	-	33	-	-	-
FOM 2	1950	3412	218	51	-	90	-	2626	-	2842
FOM 3	104	251	-	-	427	-	-	165	380	-
FOM 4	390	1365	109	110	35	28	6860	13134	4636	1421

TABLE 5.14 – State-of-the-art for low-level current sources and current mirror performances in proposed current drivers

General conclusion and discussion

In the first chapter we have investigated the origin and nature of the constraints encountered in current sources designs. We found that for classical CMOS current mirrors, basic building blocks in analog design, there exists a fixed relation between the speed, the accuracy and the power consumption that limits the overall performance of a system. In the past, several studies have proved that this relation is mainly determined by the nature and the quality of the process used to fabricate the devices. More recent studies have shown that it still concerns today's designs, and worsens with more advanced technological nodes. This technologically fixed relation is known as the *speed-power-accuracy trade-off*. However, among the solutions proposed in the literature very few specifically address the *speed-power-accuracy trade-off* of a current mirror, despite the fact, that this trade-off have been frequently studied and is unavoidably encountered in dynamic CMOS current mirror design. This observation, was the starting point of the work presented in this manuscript and, have fixed its primary objective: outperforming the present limitations in terms of speed, power and accuracy that exists in CMOS current mirror design.

In Chapter 2 we have presented analytical tools, used in a first place to derive an expression for the *speed-power-accuracy trade-off* and then to search for optimized sizes and biases of classical diode-connected current mirror. This step allowed us to target the main parameters that influence the relation between the speed, the accuracy and the power efficiency. This study have been conducted for diode-connected mirrors, for which we studied the effect of static performance optimisation on the dynamic behaviour. At the end, we arrived to the conclusion that only solutions that use active devices on the input branch to control gate and drain evolutions, will allow us to go beyond the limit fixed by the technology.

Hence, in Chapter 3, we have investigated on capabilities of standard active-input current mirror to achieve fast and precise response with minimal power consumption. In the first part, we reuse the analytical tools previously introduced to go deeper in the analysis of the active-input current mirror behaviour and to identify what are the limitations of such structures. Indeed we have demonstrated the potential speed improvement offered by the active-input topology. But we have also highlighted several constricting drawbacks that limit the relevance of this type of current mirror for some applications. The last sections were dedicated to present two possible enhancements of the standard topology that address the limitations previously discussed. The first solution has been proposed to ensure speed improvement offered by active-input technique over a wider current range. The second solution has been proposed to address the stability issue of such structure. Enlarging the stability domain at minimal cost enables higher speed and better speed-power-accuracy

ratio. However, despite the demonstrated advantages of such topologies based on voltage-mode linear feedback (OTA), the nature of the limitations has pushed us towards the search of new forms of active feedback.

Major contributions are detailed in Chapter 4. We have introduced, analysed and illustrated a novel design approach relying on a power-efficient speed boosting technique based on current-mode non-linear control loops. We have demonstrated that the replacement of the voltage-mode feedback (OTA) that exists in standard active-input current mirror by a current-mode circuit (CCII), significantly enlarges the stability domain and increases the maximum speed we can achieve while offering a supplementary degree of freedom to tune the system response. In addition, we have shown that, by forcing the feedback to have a non-linear behaviour, static specifications can be unbidden from dynamic behaviour. And this constitutes the key of the proposed approach to overcome the *speed-power-accuracy trade-off* found in classical current mirror design. The proposed CMOS implementation is supported again by a theoretical analysis dedicated to the optimisation of this new type of active-input current mirror. Conclusions of the study show that with this solution higher speed than the previous active-input structures can be reached with minimal impact on the overall accuracy and the static power consumption.

In the last chapter, we have presented the application of this new type of active current mirrors to the design of two circuits dedicated to neural stimulation. Comparison between typical results and post-layout simulation results are examined. For the first circuit realized in AMS technology, due to the manufacturer decision to not deliver the chips, we did not have the opportunity to validate the design with silicon measurements. The second circuit fabricated in TSMC technology is expected to arrive soon. We hope that silicon measurements would be available for the Ph.D defence. The proposed approach has been compared with a set of recent published circuits that share similar challenges and constraints. Finally, the state-of-the-art comparison results have demonstrated that, thanks to the design strategy and the new active-input current mirror topologies proposed, it is actually possible to outperform the present limit of the *speed-power-accuracy trade-off*.

There is a certain number of topics, not treated in this manuscript, that may worth citing to open the discussion on the outcomes:

- The proposed non-linear current conveyor architecture is surely not the only alternative to implement the current-mode non-linear feedback control. For instance, very low-voltage or low-power applications may require a much simpler implementation with limited number of devices. On the other hand, for applications with higher power budget, we might opt for modified versions of high-drive or high-speed current conveyors/amplifiers, that reuse the principle of the input impedance switching mechanism.
- The theoretical analysis of the current-mode non-linear feedback solution should include a formal stability proof, that considers a non-linear large-signal model of the full system. Work on this topic has given no results. To prove the stability of such control, we have used the decomposition of the dynamic behaviour into two separated phases and assumed the continuity between the two. Only numerical

resolutions on large-signal models using Matlab® and extensive exploration with Spectre® simulations support this assertion.

- To deploy this approach for current source architectures dealing with harmonic signals (sine waves, multi-tonal waves, ...), the work should be completed by a study that focuses more on the linearity optimisation than the optimisation of the static precision. Requirements over the CCII specifications would slightly differ.
- The input impedance switching mechanism of the CCII, and the way it is used, presents some similarities with the work done in the past on current memory cells. A comment would be that some answers to the points raised above may be found with a deeper investigation on this domain.
- Eventually, regarding the application of the proposed approach to biomedical devices, future work must involve the adaptation of the current drivers presented in the last chapter, to high-voltage architectures with multiple supply domains. High-voltage tolerant outputs are mandatory for electrical stimulation chips. Without this feature circuits can not be tested in actual biological or clinical experiments.

Appendix A

Literature review: summary of system-level architectures

This appendix summarizes the performances of circuits discussed Chapter 1, in sections 1.1.2 (page 16) and 1.2.1 (page 20).

	Lam and Ki, 2008	Or and Leung, 2010	Maity and Patra, 2016
Year	2008	2010	2016
Techno	0.35 µm	0.35 µm	0.18 µm
Type	LDO + boosted CM	LDO + boosted CM	LDO + boosted CM
Output compliance	-	-	-
Output impedance	-	-	-
Output dynamic range	up to 50 mA	up to 99 mA	up to 50 mA
Static current error	-	-	-
THD	-	-	-
Response time	0.132 µs	0.2 µs	0.4 µs
Max bandwidth	-	-	-
Power consumption	164 µA	70 µA	50 µA
Power efficiency	>99 %	>99 %	>99 %
Area	0.053 mm^2	0.032 mm^2	0.039 mm^2

Table A.1 – Performance summary of system-level architectures

	Constantinou, Bayford, and Demosthenous, 2015	Lamlih et al., 2018	Greenwald et al., 2017	Liu et al., 2014	Sit and Sarpeshkar, 2007
Year	2015	2018	2017	2014	2007
Techno	0.35 µm	0.18 µm	0.18 µm	0.18 µm	0.7 µm
Type	Improved full-diff OTA	Wideband full-diff OTA	Multipolar stim. + DAC calib.	Multipolar stim. + DAC calib.	OTA + switched cap. comp.
Output compliance	±2 V	0.95 V	-	±3.3 V	
DC Output impedance	>1 MΩ	>79 MΩ	-	-	-
Output dynamic range	±1 mA	±600 µA	up to 250 µA	<2 mA	<1 mA
Static current error	±1.45 %	-	-	0.7 %	0.7 %
THD	<0.1 %	0.3 %	-	-	-
Settling time	-	-	- calib. ≈200 ms	-	16 µs
Max bandwidth	1 MHz	10 MHz	-	-	-
Power consumption	-	-	-	136 µW	51 µA (0.75 mW)
Power efficiency	<50 %	<50 %	-	81 %	94 %
Area	0.4 mm^2	0.26 mm^2	0.072 mm^2	0.069 mm^2	1.45 mm^2

Table A.2 – Performance summary of system-level architectures (continued)

	Mita, Palumbo, and Pennisi, 2003	Palmisano, Palumbo, and Pennisi, 2000	Esparza-Alfaro, Pennisi, et al., 2014	T. Chen and Gielen, 2007
Year	2003	2000	2014	2007
Techno	0.35 µm	1.2 µm	0.5 µm	0.18 µm
Type	High-drive class AB CCII	High-drive class AB COA	High-drive class AB VFCOA	Current DAC + SSPA calib.
Output compliance	1 V	-	-	-
Output impedance	300 kΩ	-	-	-
Output dynamic range	±1 mA	±7 mA	±500 µA	16 mA
Static current error	0.5 %	2.2 %	-	- INL 0.76 LSB
THD	0.3 %	0.2 %	≈1 %	- SFDR 0.013 %
Settling time	-	-	138 µs	-
Max bandwidth	1.2 MHz	≈1.2 MHz at 20 dB	≈0.6 MHz at 20 dB	<2 MHz
Power consumption	173 µA	200 µA	84 µA	116 mA
Power efficiency	91 %	92 %	58.8 %	14 %
Area	0.026 mm^2	0.26 mm^2	0.127 mm^2	3 mm^2

TABLE A.3 – Performance summary of system-level architectures (continued)

Appendix B

Literature review: summary of enhanced current mirror architectures

This appendix summarizes the performances of current mirrors presented Chapter 1, in section 1.2.2 (page 22).

	Koliopoulos and Psychalinos, 2007	Esparza-Alfaro, Lopez-Martin, et al., 2012	Pennisi, 2002	Ramirez-Angulo, Carvajal, and Torralba, 2004	Safari and Minaei, 2016
Year	2007	2012	2002	2004	2016
Techno	0.18 µm	0.5 µm	0.5 µm	2 µm	0.18 µm
Type	FVF regulated casc.	Class AB regulated casc.	Class AB resistor based	Level shifted regulated casc.	Resistor based
Output compliance	-	-	-	145 mV	100 mV
Output impedance	-	650 MΩ	3.6 MΩ	200 MΩ	1.45 MΩ
Output dynamic range	56.9 dB	10 µA to 200 µA	±10 µA to ±100 µA	4.2 µA to 8 µA	±60 µA
Static current error	2.4 %	-	0.4 % (no montecarlo)	-	0.3 %
THD	1 % at 50 µA	0.1 % at 200 µA	0.8 % at 100 µA	-	0.8 % at 60 µA
Response time	-	-	70 ns at 20 µA (1 %)	250 ns (1 %)	-
Max bandwidth	185 MHz	98 MHz	140 MHz	40 MHz	80 MHz
Power consumption	121 µA	80 µA	250 µA	1.75 µA	200 µA
Power efficiency	40 %	70 %	30 %	82 %	23 %
Area	mm^2	mm^2	mm^2	mm^2	mm^2

♦ calculated values

TABLE B.1 – Summary performances of enhanced current mirror architecture

	Aggarwal, M. Gupta, and A. K. Gupta, 2013	Amaya, Espinosa, and Villamizar, 2014	Vajpayee et al., 2010	Torralba et al., 2003	Zeki and Kuntman, 2000
Year	2013	2014	2010	2003	2000
Techno	0.25 µm	0.18 µm	0.25 µm	0.35 µm	0.8 µm
Type	Bulk-driven high-swing casc.	Active feedback sub-threshold	Improved regulated casc.	Improved high-swing casc.	Class AB self casc.
Output compliance	-	60 mV	500 mV	220 mV	220 mV
Output impedance	0.6 MΩ	800 MΩ	3010 MΩ	>GΩ	5130 MΩ
Output dynamic range	0 µA to 280 µA	20 nA to 50 nA	0 µA to 300 µA	0 µA to 20 µA	-220 µA to 570 µA
Static current error	<0.8 %	-	<5 %	-	<0.5 %
THD	-	-	-	0.05 % at 100 kHz	-
Response time	-	5 µs	0.2 µs at 0.1 %	20 ns at 1 %	-
Max bandwidth	132 MHz	-	398 MHz	122 MHz	29 MHz
Power consumption	280 µA	60 nA	199 µA at I=100 µA	12 µA at I=0 µA	20.5 µA at I=0 µA
Power efficiency	50 %	45 %	33 %	38 %	49 %
Area	mm^2	mm^2	mm^2	mm^2	mm^2

TABLE B.2 – Summary performances of enhanced current mirror architecture (continued)

Appendix C

Relative mismatch error in current mirrors with current amplification

Expression of the relative mismatch error in current mirrors with current amplification. The copy ratio is equal to $1:N$ $(N>1)$ and corresponds to the number of output device in parallel.

Demonstration:

Index 1,2 ... N represents devices of the output branch. Single device on the input branch is referred with the index 0.

Total output current:

$$I_{OUT} = I_{OUT,1} + I_{OUT,2} + ... + I_{OUT,N}$$

Random fluctuation for device i:

$$\delta I_{OUT,i} = g_m(\delta V_{TH,0} \pm \delta V_{TH,i}) + I_{OUT,i}\frac{\delta\beta_i}{\beta}$$

Variance of output current for each output devices i:

$$\sigma^2(I_{OUT,i}) = g_m^2(\sigma^2(V_{TH,0}) + \sigma^2(V_{TH,i})) + I_{OUT,i}^2\frac{\sigma^2(\beta_i)}{\beta^2}$$

$$\text{as:} \quad cov(V_{TH,0}, V_{TH,i}) = 0$$

With random dispersion expressed for two matched device as defined in Chapter 1 $(\sigma/\sqrt{2})$:

$$\sigma^2(I_{OUT,i}) = g_m^2\sigma^2(V_{TH}) + I_{OUT,i}^2\frac{\sigma^2(\beta)}{2\beta^2}$$

$$cov(I_{OUT,i}, I_{OUT,j}) = g_m^2\sigma^2(V_{TH})$$

Variance of the total output current I_{OUT}:

$$\begin{aligned}\sigma^2(I_{OUT}) &= \sum_{i=1}^{N}\sigma^2(I_{OUT,i}) + 2\sum_{1<i,j<N} cov(I_{OUT,i}, I_{OUT,j}) \\ &= N\sigma^2(I_{OUT,i}) + 2N(N-1)cov(I_{OUT,i}, I_{OUT,j})\end{aligned}$$

Retrieve the form in (2.9) by replacing variance and covariance for each devices:

$$\sigma^2(I_{OUT}) = \left(\frac{1}{2N}\right)\frac{\sigma^2(\beta)}{\beta^2} + \left(\frac{2N-1}{N}\right)\left(\frac{g_m}{I_{IN}}\right)^2\sigma^2(V_{TH})$$

with:

$$\sigma^2(V_{TH}) = \frac{A_{VTH}^2}{WL} \qquad \frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^2}{WL}$$

Appendix D

Sensitivity analysis for load influence on bandwidth in standard active input current mirror

This appendix is in the continuity of the theoretical analysis of standard active input current mirror treated in Chapter 3 section 3.2 (starting page 50). It is recommended to go through the sections 3.2.2 and 3.2.3 for better reading of this appendix.

Equations for load or parasitics influence on mirror speed

The components connected to the current mirror influence the bandwidth enhancement capability of the active-input structure. For instance, the feedback circuit or the source biasing the current mirror will load the input drain and consequently will modify the input pole location, causing a shift in system behaviour.

These external impedances can be included in the Y-Matrix as variations of the initial admittance parameters. If the maximum bandwidth (at fixed damping factor) offered by the active-input current mirror is higher than the bandwidth required to meet the target speed, then the impact on margins has to be quantified and the critical parameters identified.

Once margins have been estimated, we exploit the sensitivity analysis described below, to compute the rate of change of the corner frequency F_{ai} for several parameters variations. Thus we are able to predict the minimum or maximum admissible values for these external impedance to preserve the desired bandwidth. This approach is synthesized in the diagram presented in figure D.1.

In the following calculation, only one admittance parameter p is varying at the time, the others are kept identical. p_{LOAD} and p_{INIT} refer to the parameter value with and without the load. A coefficient A is introduced to quantify variations of the parameter value under the influence of an external load.

$$p_{\mathrm{LOAD}} = A p_{\mathrm{INIT}} \tag{D.1}$$

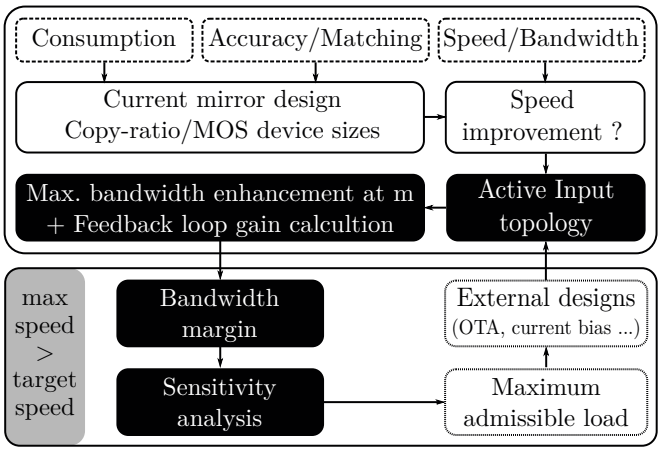

FIGURE D.1 – The load influence calculation approach

Rate of change for the corner frequency F_{ai}, referred as Q, is defined as the ratio of the loaded mirror corner frequency to the initial corner frequency with no loading effect considered. Equations (D.2) to (D.4) show expressions of the function $Q = f(A)$ for the main parameters subject to variations.

$$A_{C11} = \frac{C_{11\text{LOAD}}}{C_{11}} \qquad A_{C22} = \frac{C_{22\text{LOAD}}}{C_{22}} \; A_{g22} = \frac{g_{22\text{LOAD}}}{g_{22}}$$

Leading to:

$$Q_{C11} = \frac{a + \dfrac{b}{A_{C11}}}{a + b} \tag{D.2}$$

$$Q_{C22} = \frac{1}{A_{C22}} \sqrt{\frac{c + d}{\dfrac{c}{A_{C22}} + d}} \tag{D.3}$$

$$Q_{g22} = \frac{A_{g22}a + b}{a + b} \sqrt{\frac{c + d}{A_{g22}c + d}} \tag{D.4}$$

$$a = C_{11}g_{22}$$
$$b = C_{12}g_{21}$$
$$c = C_{21}C_{22}g_{22}$$
$$d = 2g_{21}C_{22}^2$$

We observe that when C_{11} increases, the bandwidth ($= F_{\text{ai}}$) tends toward a constant value. Also, When C_{22} increases, the maximum bandwidth reachable decreases and tends to zero for relatively large C_{22} value. On the contrary, an increase of g_{22} leads to higher bandwidth. Eventually, by analysing the function $Q = f(A)$ we are able to link the bandwidth improvement offered by the active-input structure to changes brought by external loads on the mirror characteristics.

Example:

use of the function $Q = f(A)$ to predict maximum admissible loads according to target bandwidth.

There is no bandwidth margin left, when the maximum bandwidth reachable for

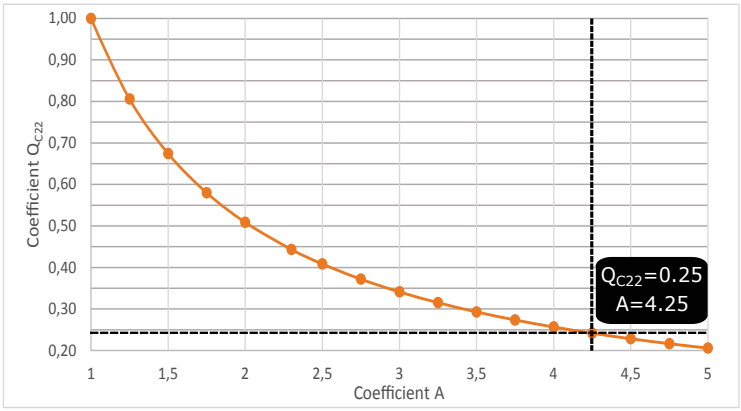

FIGURE D.2 – Evolution of $F_{\text{ai}}@m = 1$ against C_{22} variations

the active-input mirror (at fixed damping factor) is equal to the diode-connected mirror bandwidth. This specific case is obtained when the ratio Q is equals to the previously-calculated value $1/K$.

With the help to graphical or analytical resolution of $Q = f(A)$, we can derive the A value corresponding to $Q = 1/K$ and then extract the maximum admissible impedance Z_{MAX} as:

$$Z_{\text{MAX}} = (A_{MAX} - 1).p_{\text{INIT}} \tag{D.5}$$

A load greater than Z_{MAX} for the concerned node leads to a bandwidth enhancement factor K below 1. It means that the active-input solution is no longer capable of improving speed of the loaded current-mirror.

Illustration on case study

Fig. D.2 is given to illustrate a calculation example of the maximum admissible capacitance load on the input drain. Which is defined as the maximum load bringing the corner frequency $F_{\text{ai}}@m = 1$ back as it is now equal to the diode-connected corner frequency F_{dco}. We know without any load, the $F_{\text{ai}}@m = 1$ is equal to 4.3 MHz and the F_{dco} is equal to 1 MHz, so the ratio between the two is:

$$\frac{1}{K_{@m=1}} = \frac{1}{4.3} = 0.23$$

Using the graphical resolution shown fig. D.2, we determine that $A_{C22} = 4.25$ when $Q_{C22} = 0.23$. Then the maximum admissible capacitance load on the input drain is calculated as:

$$C_{\text{MAXload}} = (A_{C22} - 1)C_{22} = 25.3 \text{ fF}.$$

If we considers the optimal system response as critically damped, these results show that there is no bandwidth enhancement possible when the input drain is loaded by a capacitance greater than the value calculated above, $F_{\mathrm{ai}}@m = 1$ is lower than F_{dco}. It can be observed in Fig. 3.4, looking at the frequency response for the current mirror with a 35fF load.

Appendix E

Layout of proposed feedback circuits in Chapter 4

Layout of the programmable non-linear current conveyor in Fig. E.1 has the following dimension: 62 µm×35 µm. Layouts of both nmos and pmos OPAMP in Fig. E.2 have the following dimension: 10 µm×10 µm. Pictures below are not displayed at the same scale.

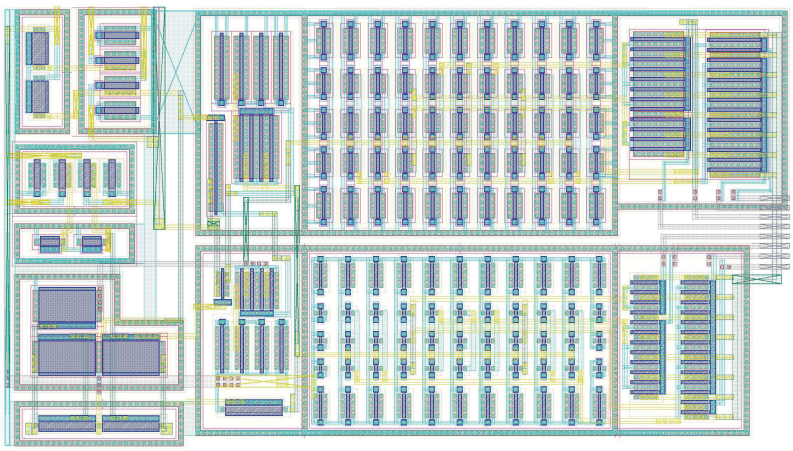

FIGURE E.1 – Layout of the programmable non-linear CCII

(A) NMOS differential pair

(B) PMOS differential pair

FIGURE E.2 – Layout of the input stage OPAMPS

Appendix F

Characterization of the non-linear CCII

This appendix presents the characterization of the non-linear current conveyor presented in section 4.3.3 of Chapter 4. Results displayed here are Spectre® simulation results.

Technology: TSMC Standard CMOS 0.18 µm

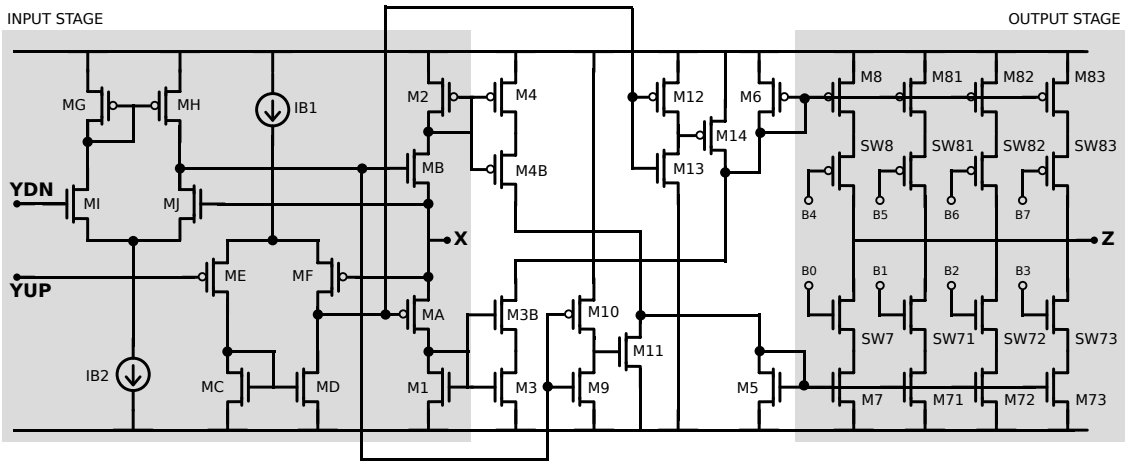

FIGURE F.1 – Programmable implementation of the non-liner CCII

	W/L µm		W/L µm		W/L µm		W/L µm
M1	3.5/0.25	M2	5/0.25	M5	0.45/0.25	M6	1.5/0.25
M3	3.5/0.25	M4	5/0.25	M7	$2 \times 0.45/0.25$	M8	$2 \times 1.5/0.25$
M3B	12/0.25	M4B	20/0.18	M71	$4 \times 0.45/0.25$	M81	$4 \times 1.5/0.25$
MA	7/0.18	MB	2/0.18	M72	$8 \times 0.45/0.25$	M82	$8 \times 1.5/0.25$
MC	1/1.5	MG	0.5/1.5	M73	$12 \times 0.45/0.25$	M83	$12 \times 1.5/0.25$
MD	1/1.5	MH	0.5/1.5	M9	0.5/4.5	M12	0.5/4.5
ME	2.5/0.5	MI	2/0.5	M10	2.5/4.5	M13	2.5/4.5
MF	2.5/0.5	MJ	2/0.5	M11	0.5/4.5	M14	2.5/4.5

TABLE F.1 – Transistors sizing for the NL-CCII

F.0.1 Static measurement

Testbench setup for Fig. F.2: CCII threshold are set to 0.6 V (V_{YUP}) and 0.8 V (V_{YUP}) or 1.0 V (V_{YUP}) and 1.2 V (V_{YUP}). The input node X is driven by an ideal voltage source varying from 0.5 V to 1.3 V. The output node Z is loaded by an ideal voltage source at $V_{DD}/2$. The CCII gain β is programmed to 10 for both current directions. In this test condition we measure:

	thresholds at 0.6V-0.8V		thresholds at 1V-1.2V	
for $I_X =$	r_X	β	r_X	β
−100 µA	5.9 kΩ	8.4	8.1 kΩ	8.4
−1 µA	767 kΩ	10.1	971 kΩ	10.1
1 µA	826 kΩ	9.5	1306 kΩ	9.5
100 µA	9.9 kΩ	8.2	12.1 kΩ	8.2

TABLE F.2 – Measure of input impedance r_X and current gain β for small and maximal values of the input current I_X

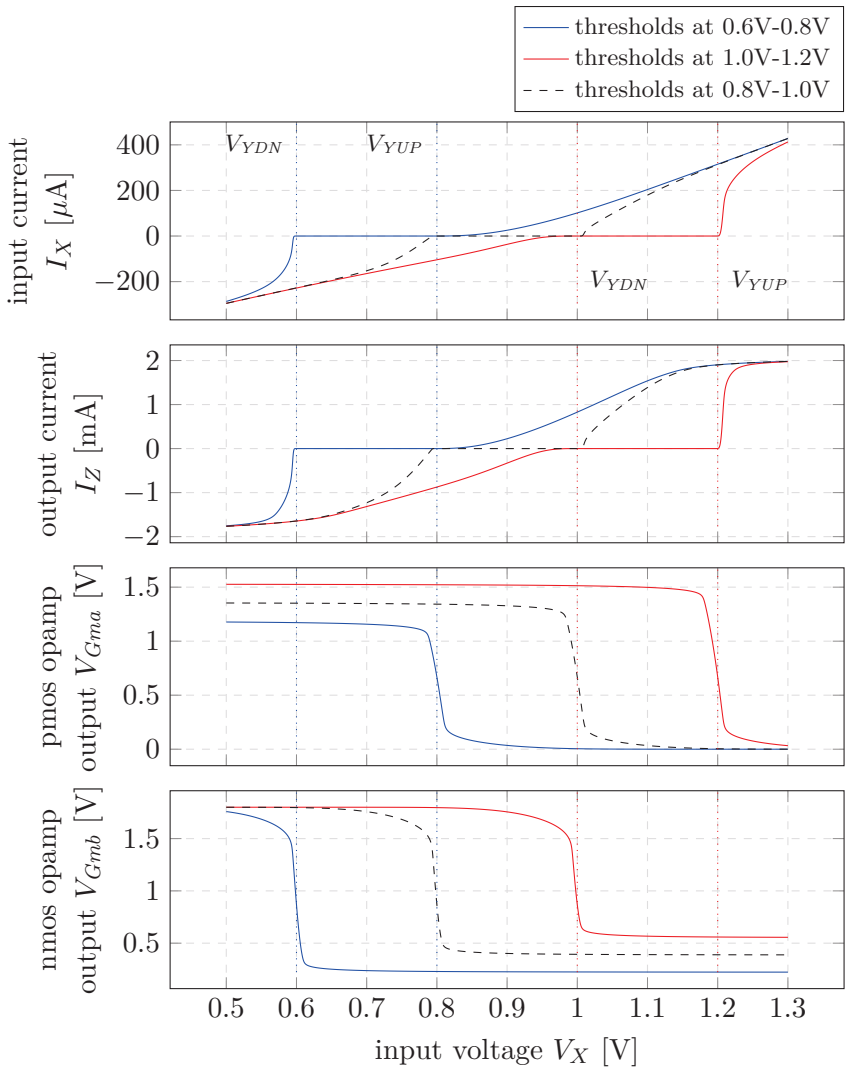

FIGURE F.2 – Static characteristics versus input voltage

F.0.2 Dynamic measurement

Testbench setup for Fig. F.3 and Fig. F.4: CCII threshold are set to 0.6 V (V_{YUP}) and 0.8 V (V_{YUP}). The input node X is loaded by an ideal resistor of 100 MΩ and driven by an ideal current with both small step (±1 µA) and a full-range step (±100 µA). The output node Z is loaded by an ideal voltage source at $V_{DD}/2$. The CCII gain β is programmed to 10 for both current directions.

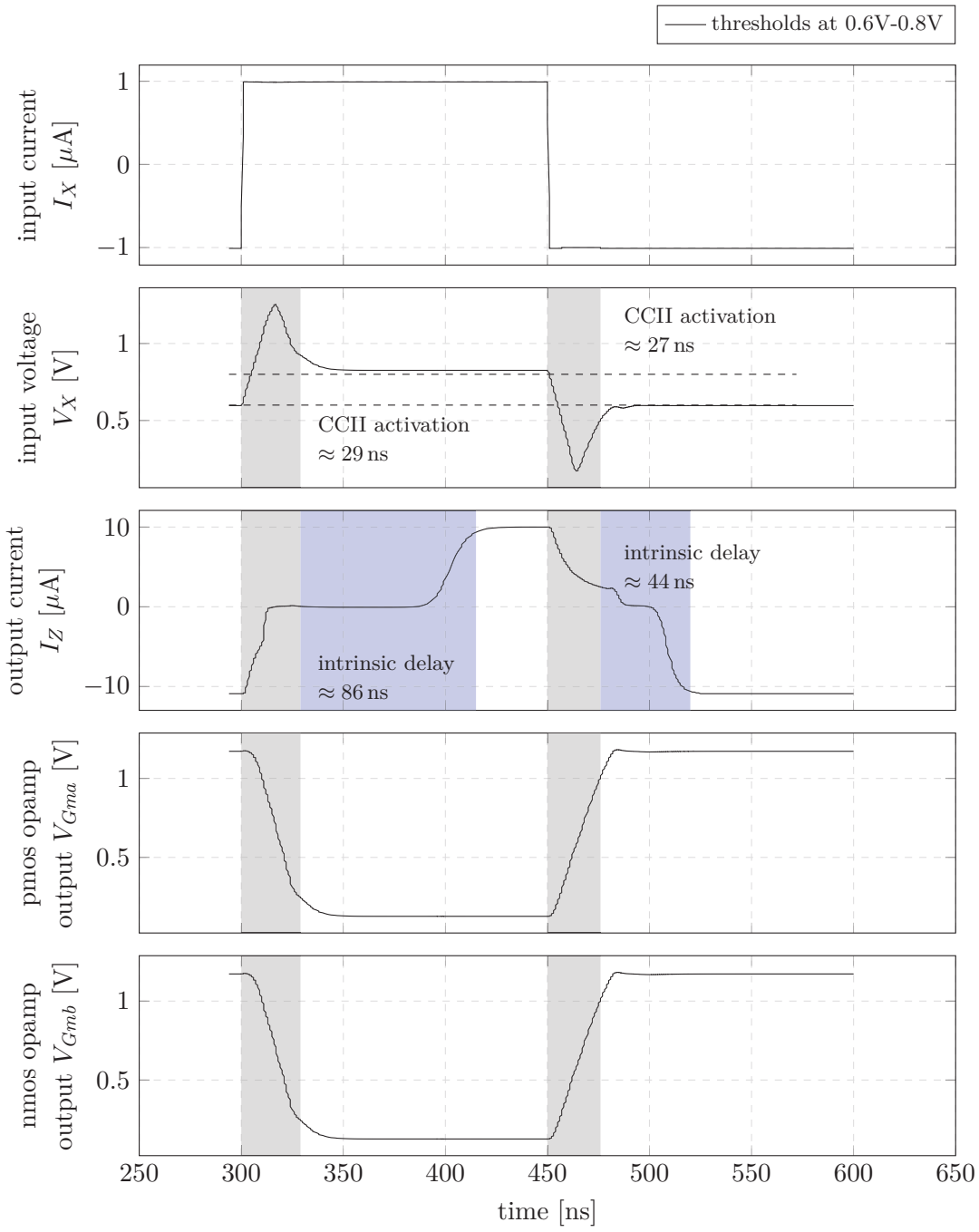

FIGURE F.3 – Transient response to a small step ($I_X = \pm 1\,\mu A$)

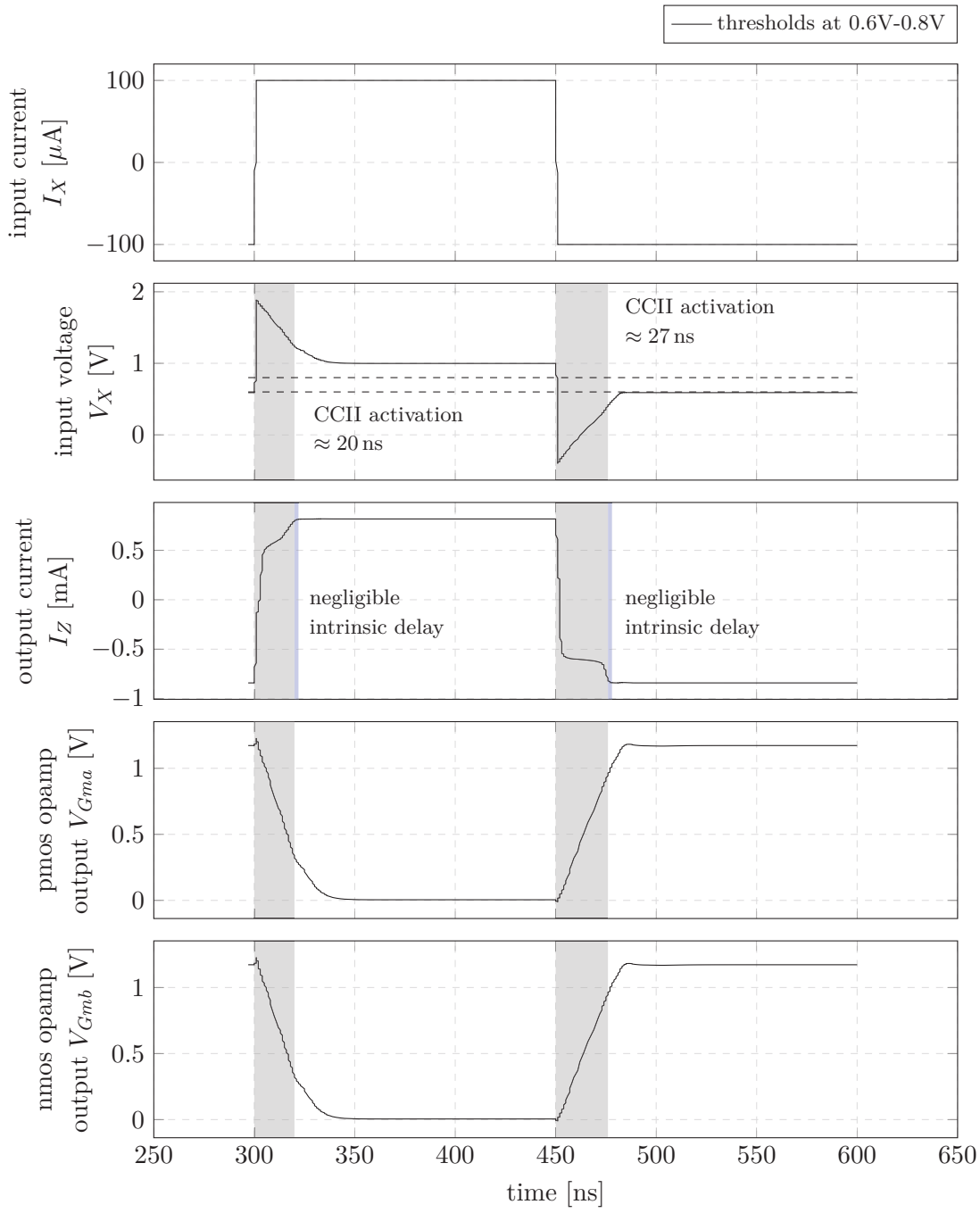

FIGURE F.4 – Transient response to a full range step ($I_X = \pm 100\,\mu A$)

Appendix G

Complete simulation results for section 4.3.3 of chapter 4

G.1 CM sizing and speed-accuracy trade-off

Testbench setup for Fig. G.1 and Fig. G.2: DC and AC meas. for three values of L.

The static input current is taken as 30 µA, giving an output current of 600 µA.
L_{CM}=4 µm or 11 µm or 18 µm, $(W/L)_{CM}$=1.2 µm, $W_{CASC} = W_{CASC}$, L_{CASC}=0.25 µm and N=20.
The load is an ideal voltage source at $V_{DD}/2$ =0.9 V.
The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V

G.2 Static measurements

Testbench setup for Fig. G.3: DC meas. with sweep over I_{IN}.

W_{CM}=21.5 µm, L_{CM}=18 µm, W_{CASC}=21.5 µm, L_{CASC}=0.25 µm and N=20.
The load is an ideal voltage source at $V_{DD}/2$ =0.9 V.
The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V
CCII threshold are fixed at 0.6 V and 0.8 V.

Testbench setup for Fig. G.4: DC meas. with sweep over V_{OUT}.

W_{CM}=21.5 µm, L_{CM}=18 µm, W_{CASC}=21.5 µm, L_{CASC}=0.25 µm and N=20.
The input current is taken at 3 values, I_{INmin}, $I_{INmidrange}$ and I_{INmax}.
The load is an ideal voltage source at V_{OUT}.
The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V
CCII threshold are fixed at 0.6 V and 0.8 V.

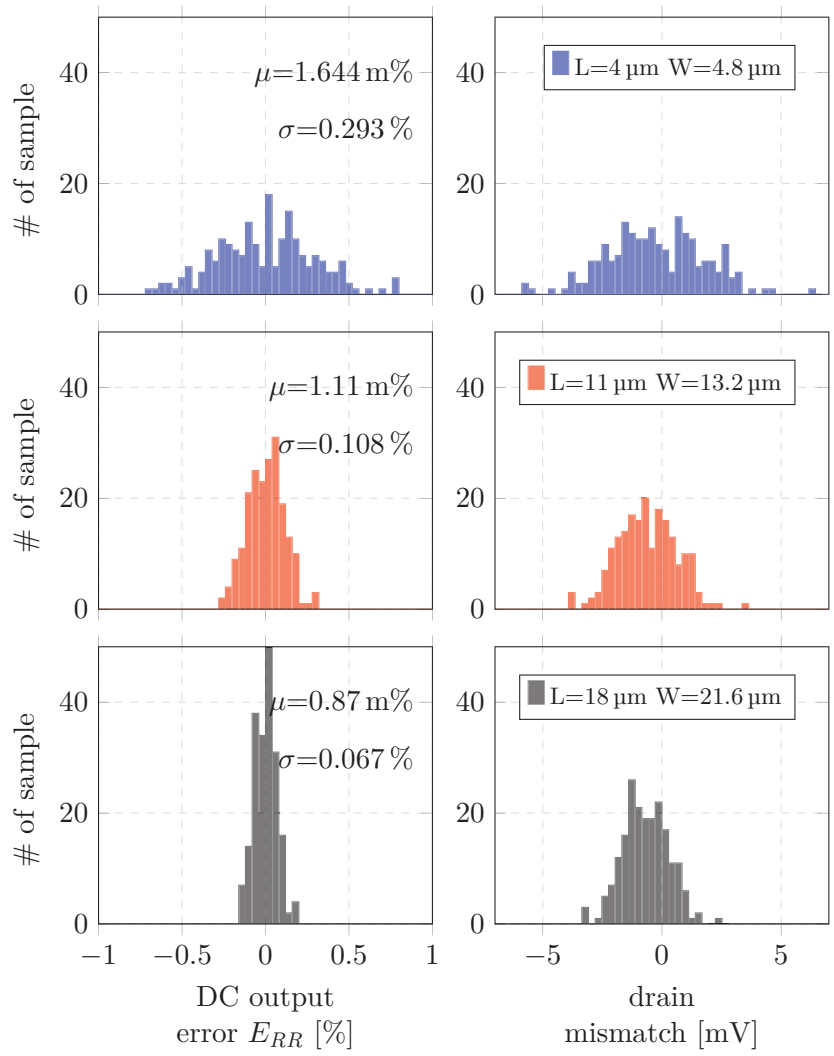

FIGURE G.1 – Output error and drain mismatch for the diode-connected WSCASC current mirror at various lengths.

G.3 Dynamic behaviour

G.3.1 Typical step response

Testbench setup for Fig. G.5: TRAN meas. with full range step.

W_{CM}=21.5 µm, L_{CM}=18 µm, W_{CASC}=21.5 µm, L_{CASC}=0.25 µm and N=20.
The load is an ideal voltage source at $V_{DD}/2$ =0.9 V.
The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V
CCII threshold are fixed at 0.6 V and 0.8 V. The input stimuli is a current step from 5 µA to 100 µA leading to an expected current step of 100 µA to 2 mA.
The CCII gain is set to 24 ('0111') both NLCCII WSCASC and NLCCII IRRC.

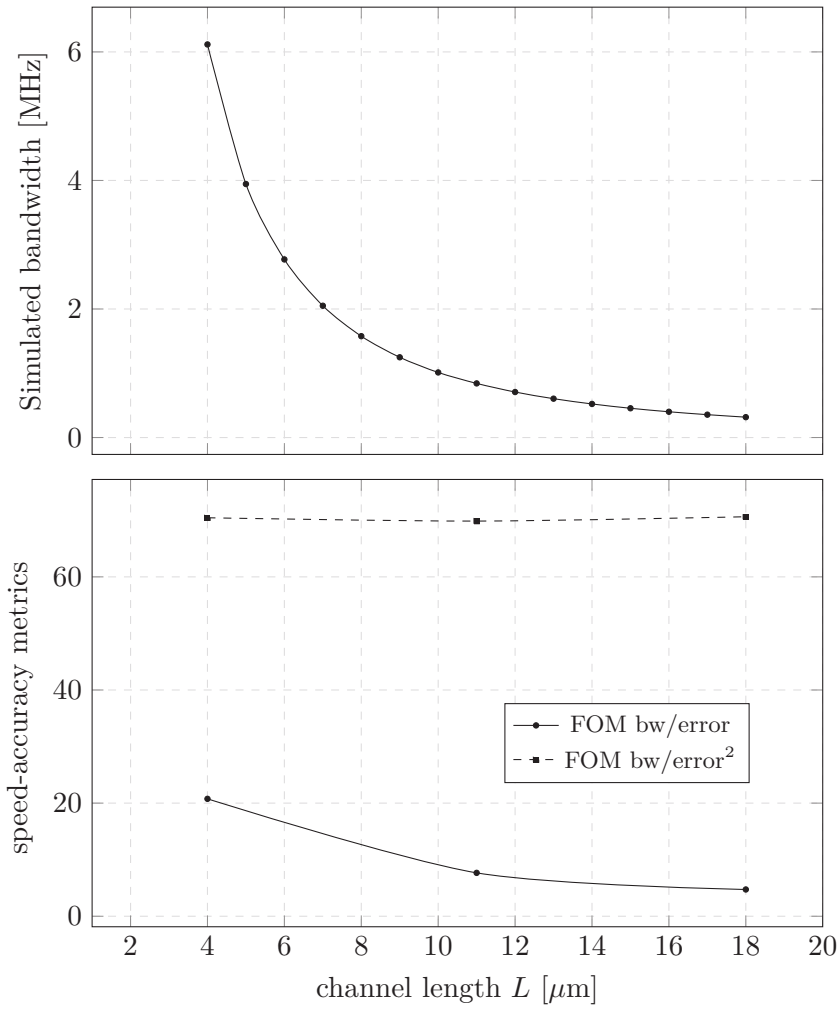

FIGURE G.2 – Bandwidth for the diode-connected WSCASC current mirror at various lengths.

G.3.2 Distortion measurements

Frequency analysis is done using transient simulation results and the dft (discrete fourir transform) functions in virtuoso..
The time window (i.e. the transient stop time) fixes the bandwidth resolution of the DFT: $t_{win} = 1/res_{bw}$.
The transient step time fixes the maximum frequency of the dft: $F_{max}/2 = 1/t_{step}$ and should be forced to to a constant via the transient analysis form.
The number of sample set in the calculator dft form should corresponds to
sample $= t_{win}/t_{step}$=$2F_{max}/res_{bw}$.
The input frequency should be a power of two of the sampling frequency, in other words: $t_{in} = 2^x t_{step}$ or $F_{in} = 2^x F_{max}$.

Testbench setup for Fig. G.6 and Fig. G.7: TRAN meas. long time simulation.

W_{CM}=21.5 µm, L_{CM}=18 µm, W_{CASC}=21.5 µm, L_{CASC}=0.25 µm and N=20.
The load is an ideal voltage source at $V_{DD}/2$ =0.9 V.

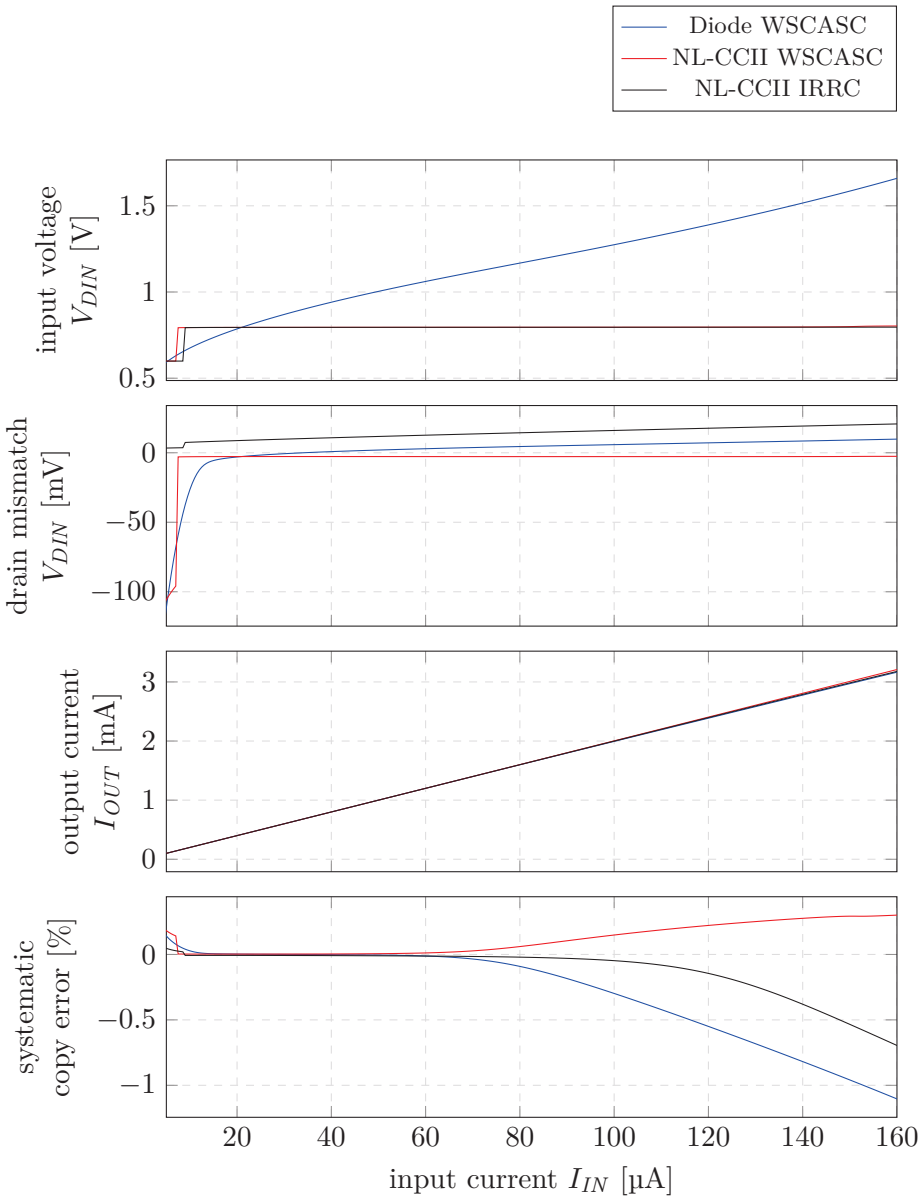

FIGURE G.3 – Static characteristics versus input current

The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V
CCII threshold are fixed at 0.6 V and 0.8 V. The input stimuli is a current step from 5 µA to 100 µA leading to an expected current step of 100 µA to 2 mA.
The CCII gain is set to 08 ('0010') for the NLCCII WSCASC.
The CCII gain is set to 24 ('0111') for the NLCCII IRRC.

The input current source is an sine wave current generator.
The total transient simulation time equals 1280 µs.
The total number of sample is $2^{16} = 65536$.
The simulation time step is set to $1280/2^{16}$ =19.5 ns giving a sample frequency of 50.8 MHz.
The input signal period is equals to 1280/128 =10 µs giving a fundamental frequency of 100 kHz and a total of 128 period simulated.

G.4 Statistical measurements

G.4.1 Mismatch influence

Monte-carlo simulation are performed for statistical evaluations of the overall copy error, the drain mismatch of mirroring devices, the settling time and the output impedance. The 3 circuits are stimulated with several step of various amplitudes while biased at different level across the input current range. Stimuli cases are summarized in Table. G.1.

#	name	bias	step	#	name	bias	step
1	bias1-pulse1	10 µA	±0.5 µA	9	bias4-pulse1	70 µA	±0.5 µA
2	bias1-pulse2	10 µA	±2 µA	10	bias4-pulse2	70 µA	±2 µA
3	bias2-pulse1	30 µA	±0.5 µA	11	bias4-pulse3	70 µA	±20 µA
4	bias2-pulse2	30 µA	±2 µA	12	bias5-pulse1	90 µA	±0.5 µA
5	bias2-pulse3	30 µA	±20 µA	13	bias5-pulse2	90 µA	±2 µA
6	bias3-pulse1	50 µA	±0.5 µA	14	bias5-pulse3	90 µA	±20 µA
7	bias3-pulse2	50 µA	±2 µA	15	bias6-pulse1	110 µA	±0.5 µA
8	bias3-pulse3	50 µA	±20 µA	16	bias6-pulse2	110 µA	±2 µA
				17	fullrange-pulse	60 µA	±55 µA

Table G.1 – Stimuli summary

Testbench setup for Fig. G.8 and Fig. G.9: Montecarlo simulation (200 runs)

W_{CM}=21.5 µm, L_{CM}=18 µm, W_{CASC}=21.5 µm, L_{CASC}=0.25 µm and N=20.
The load is an ideal voltage source at $V_{DD}/2$ =0.9 V.
The gate voltage for cascode devices in WSCASC CM is fixed at 1.3 V
CCII threshold are fixed at 0.6 V and 0.8 V. The input stimuli is a current step from 5 µA to 100 µA leading to an expected current step of 100 µA to 2 mA.
The CCII gain is set to 08 ('0010') for the NLCCII WSCASC.
The CCII gain is set to 24 ('0111') for the NLCCII IRRC.

G.5 Comparison with figure-of-merits

To ease the comparison, we use the figure-of-merits that have been presented in Chapter 1.

G.5.1 Pulse stimuli (time domain evaluation)

Definitions of the metrics used are shown in Table. G.2.
Results are given for each stimuli case mentioned in the previous section (Table. G.1).

The response time $t_{r0.4\%}$ is measured on transient simulation.
The static output error E_{RR} is measured.
Power efficiency and accuracy are expressed in % and defined as follow:

$$\text{power efficiency} = \frac{P_{LOAD}}{P_{TOT}} = \frac{I_{OUT}}{I_{OUT} + I_{IN} + I_{BIAS}} \tag{G.1}$$

$$\text{DC copy error} = |\mu(E_{RR})| + |\sigma(E_{RR})| \tag{G.2}$$

The bandwidth is estimated as:

$$\text{estim. bandwidth} = \frac{1}{2\pi \times \tau} \approx \frac{1}{2\pi \times \frac{t_{r0.4\%}}{5}} \tag{G.3}$$

For the metric FOM A a high score demonstrate an efficient use a the total power dedicated to a block or a circuit to achieve precise and/or fast current generation. Metric FOM D is similar but the terms related to the accuracy is squared. For the simple current mirror their values are fixed by technological constants and relate to the process quality. The last metrics put in relation the speed with power efficiency (FOM G) or with accuracy (FOM I).

$\text{FOM A} = \frac{\text{power eff}}{\text{resp. time} \times \text{dc error}}$	$\text{FOM D} = \frac{\text{power eff}}{\text{resp. time} \times \text{dc error}^2}$
$\text{FOM G} = \frac{\text{power eff}}{\text{resp. time}}$	$\text{FOM I} = \frac{1}{\text{resp. time} \times \text{dc error}}$

TABLE G.2 – Definition of various figure-of-merits used for circuits comparison

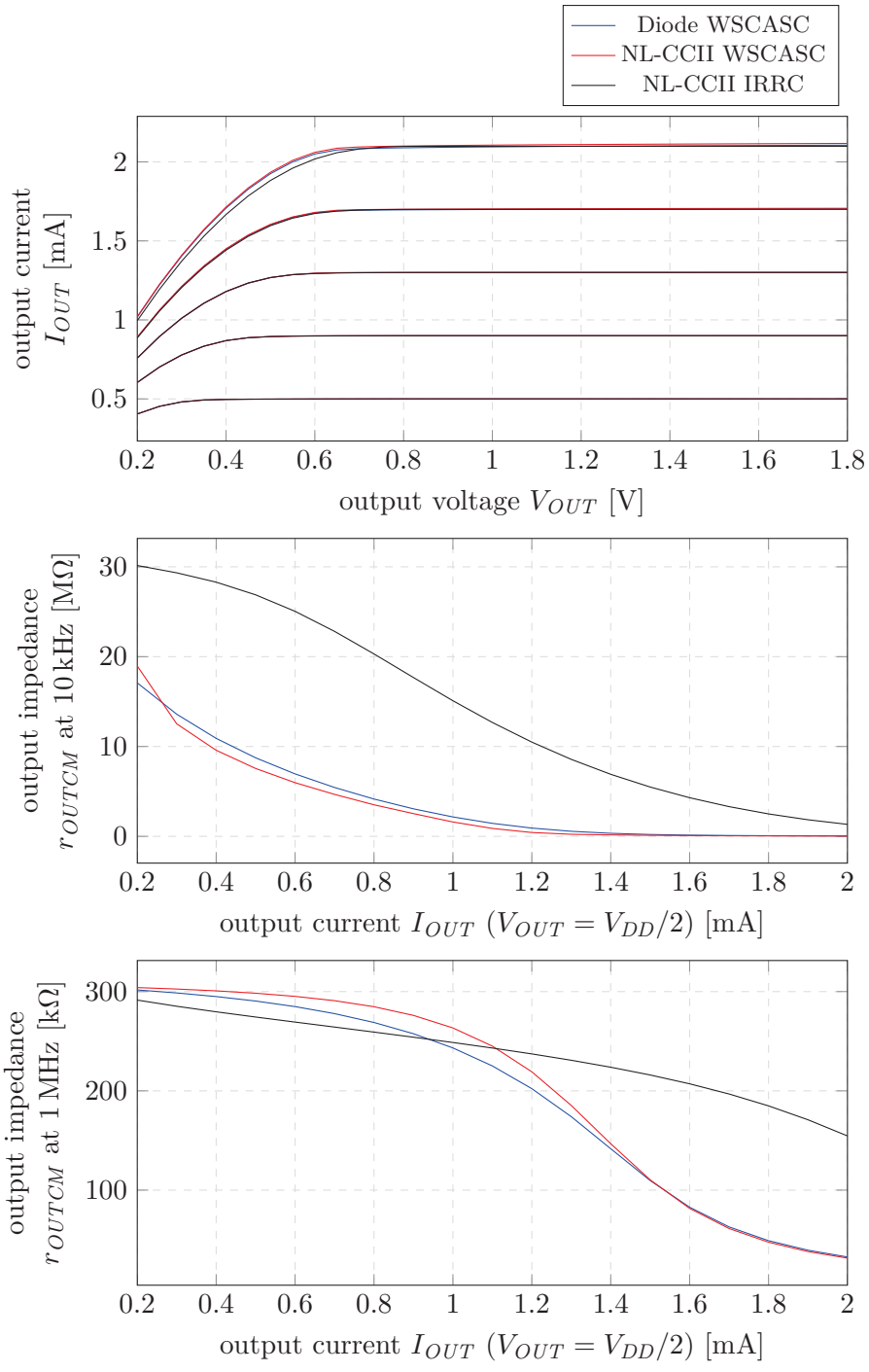

FIGURE G.4 – Output characteristics

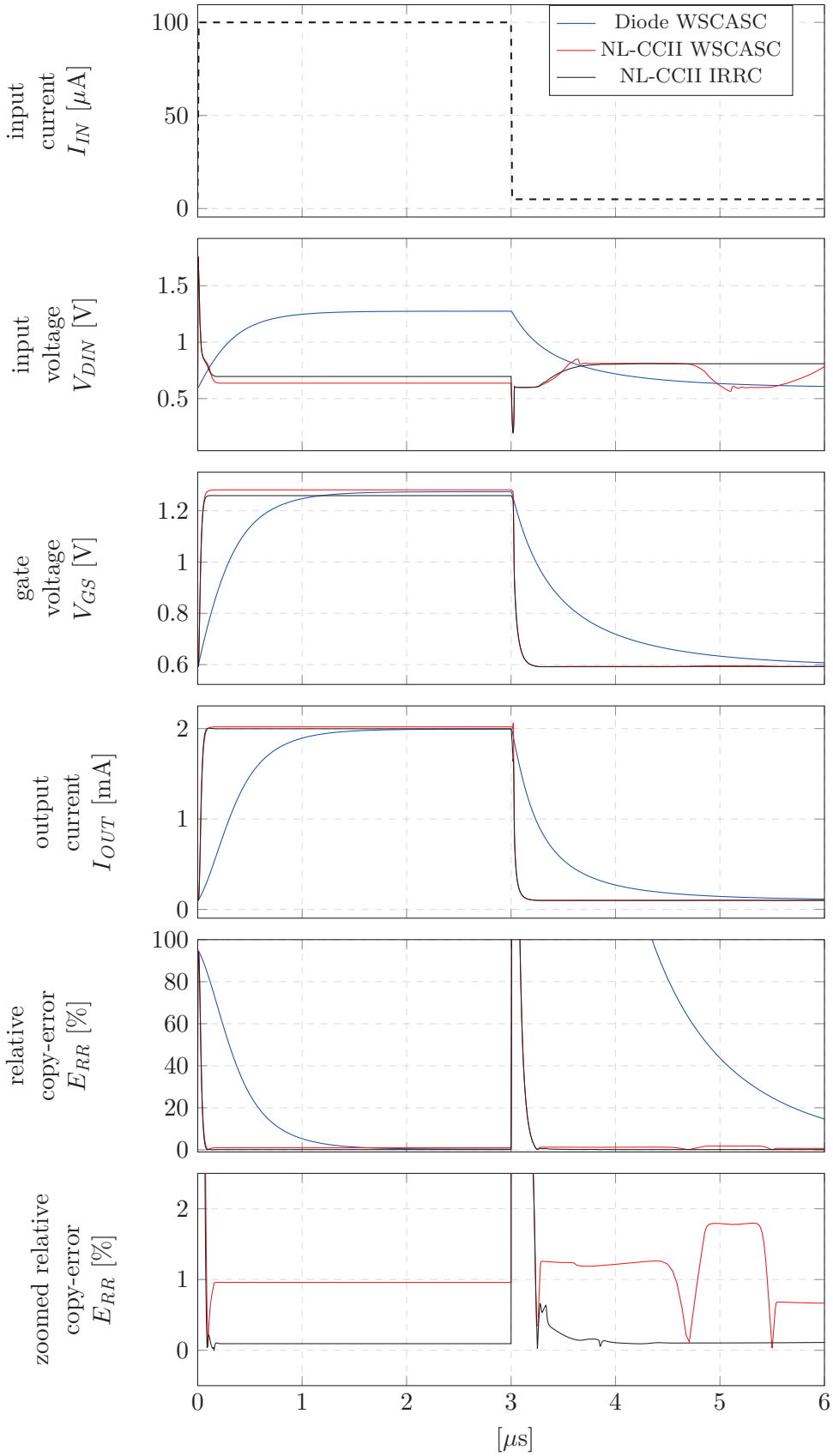

FIGURE G.5 – Transient response to a full range step

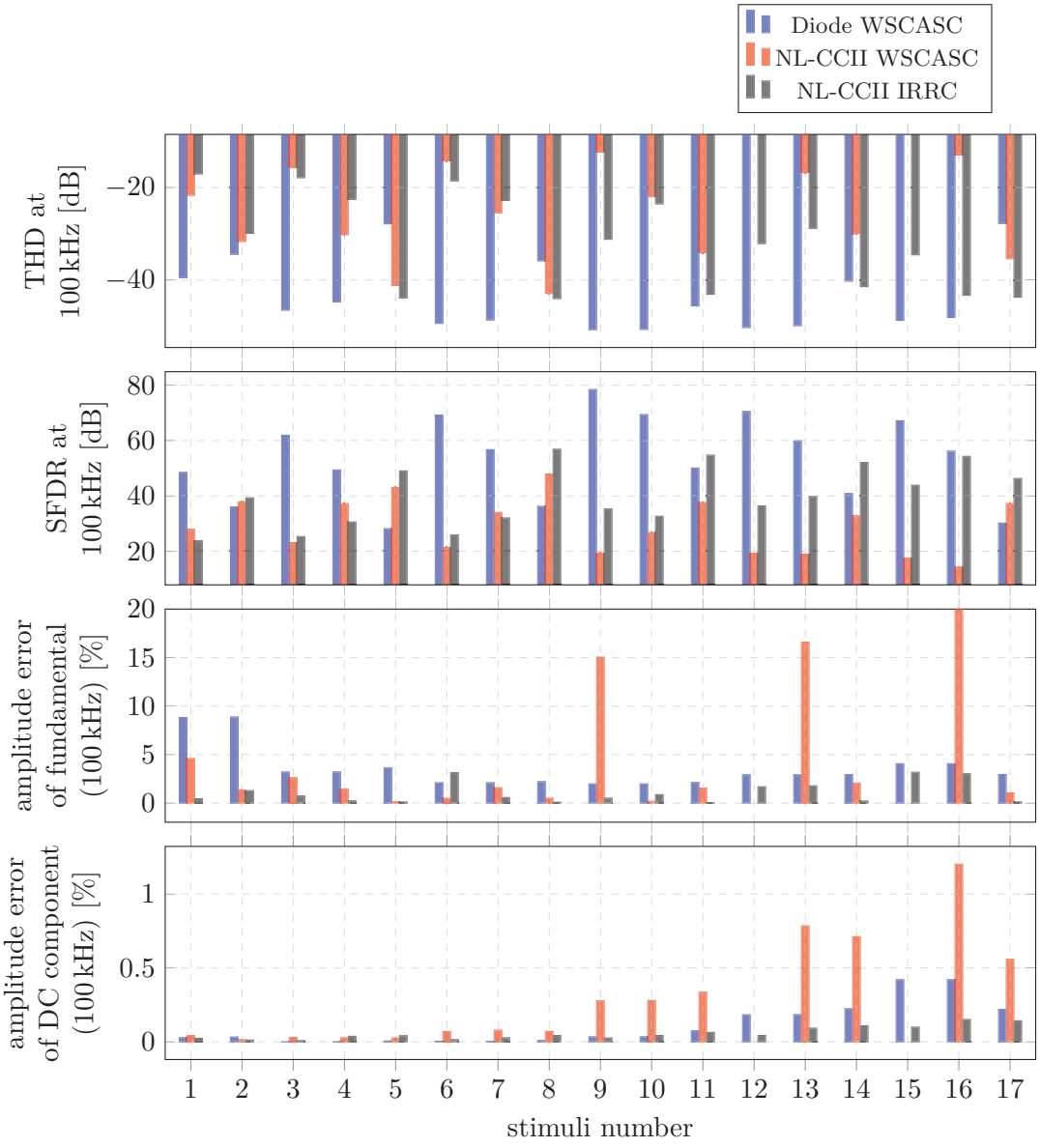

FIGURE G.6 – THD, SFDR and amplitude errors of the fundamental and DC frequency for distortion evaluation

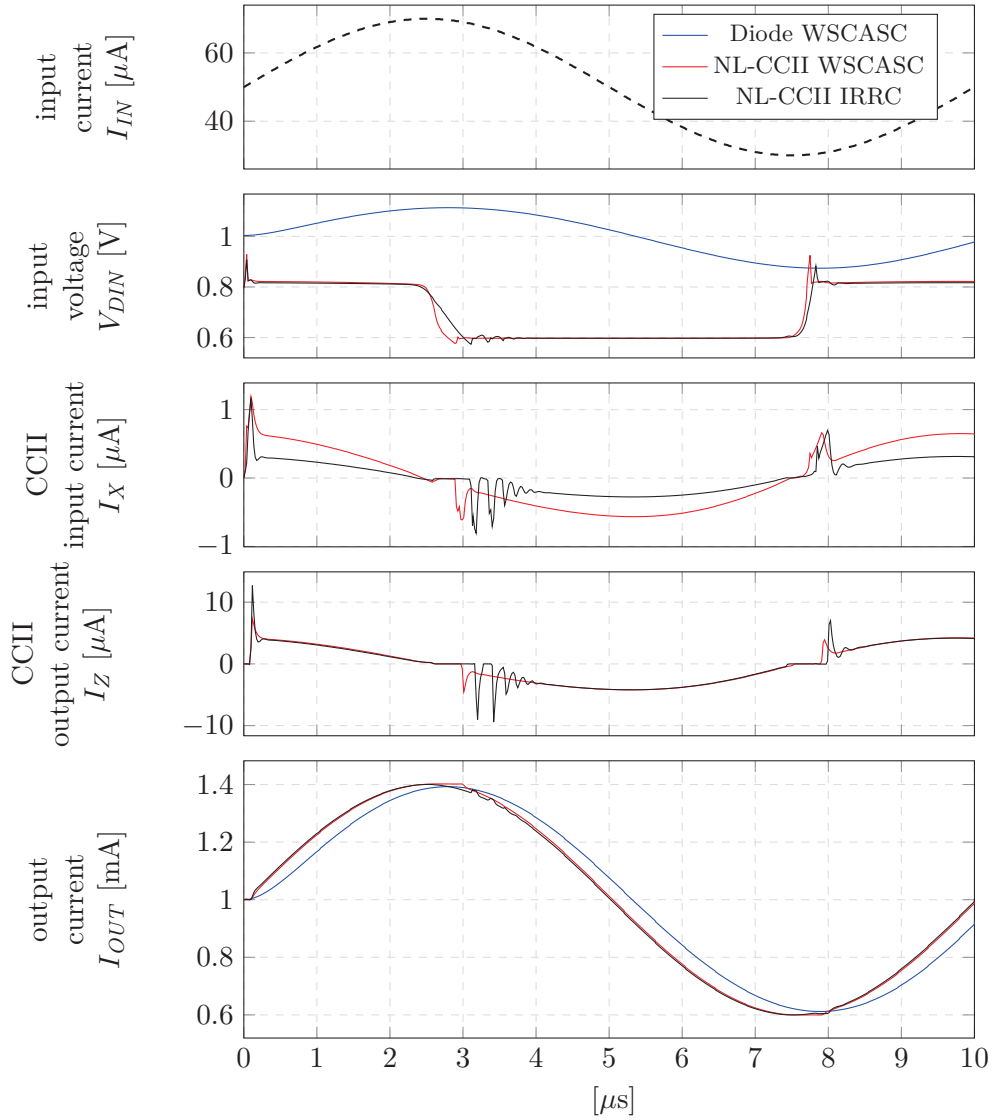

FIGURE G.7 – One period of long time simulation with sinusoidal signals response. Input current wave has a DC component of 50 µA and a magnitude of 20 µA.

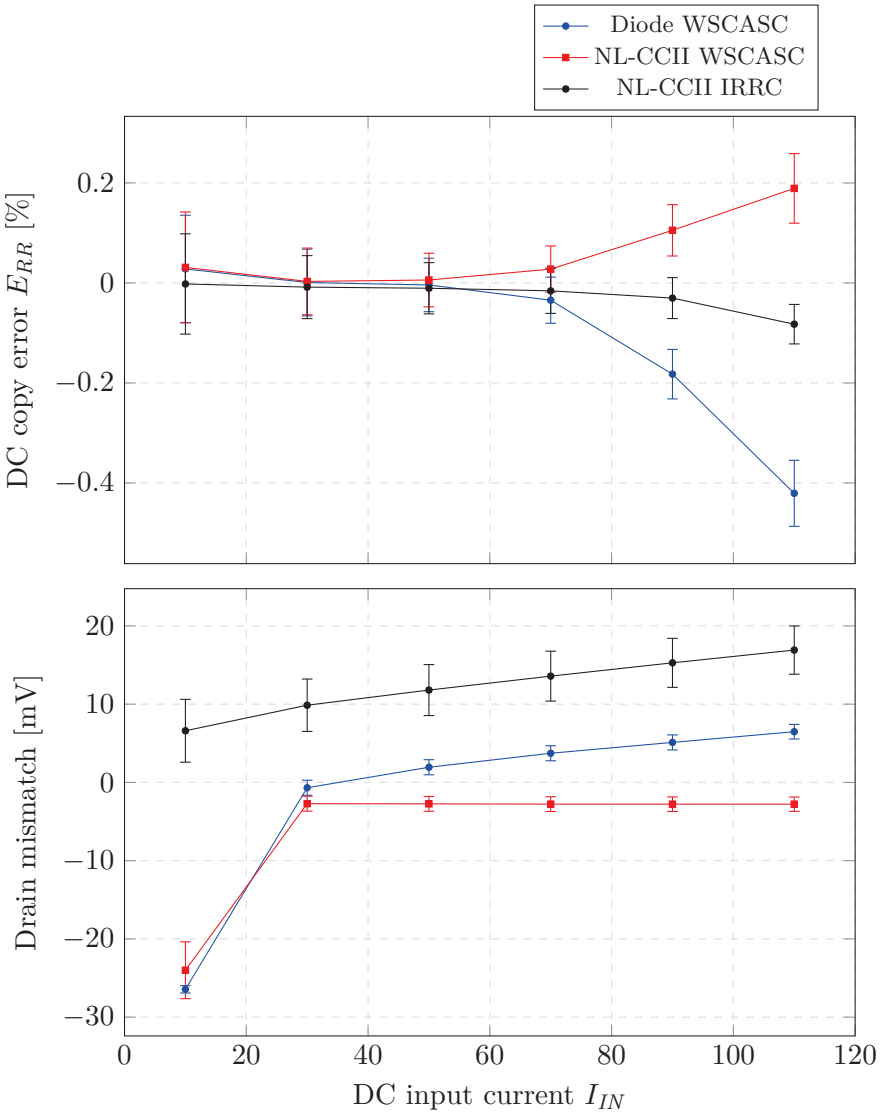

FIGURE G.8 – DC current copy error and drain mismatch. Error bars represent the standard deviation (σ) obtained after a 200 runs monte-carlo simulation.

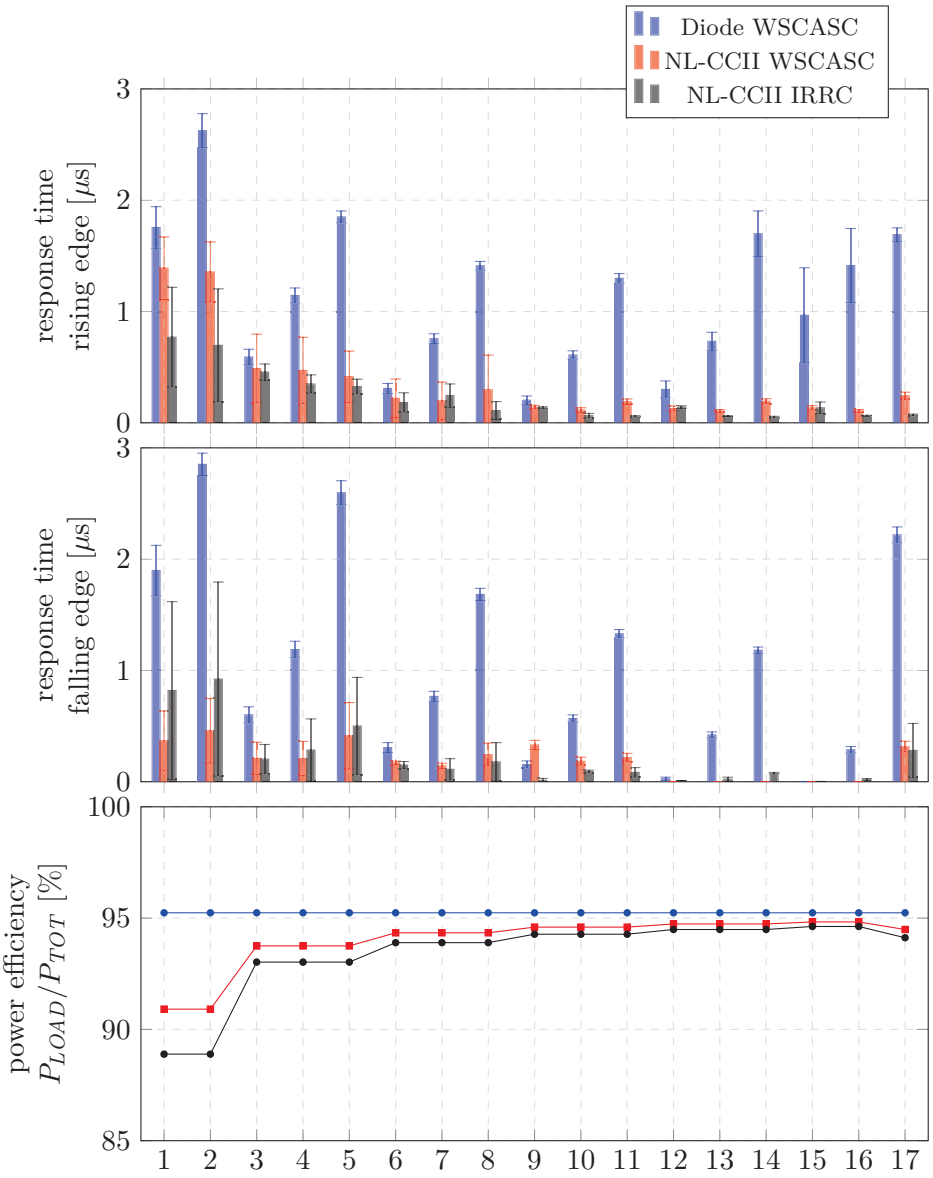

FIGURE G.9 – Response time at 0.4 % and power efficienct for each stimuli reported in Table. G.1. Error bars represent the standard deviation (σ) obtained after a 200 runs monte-carlo simulation.

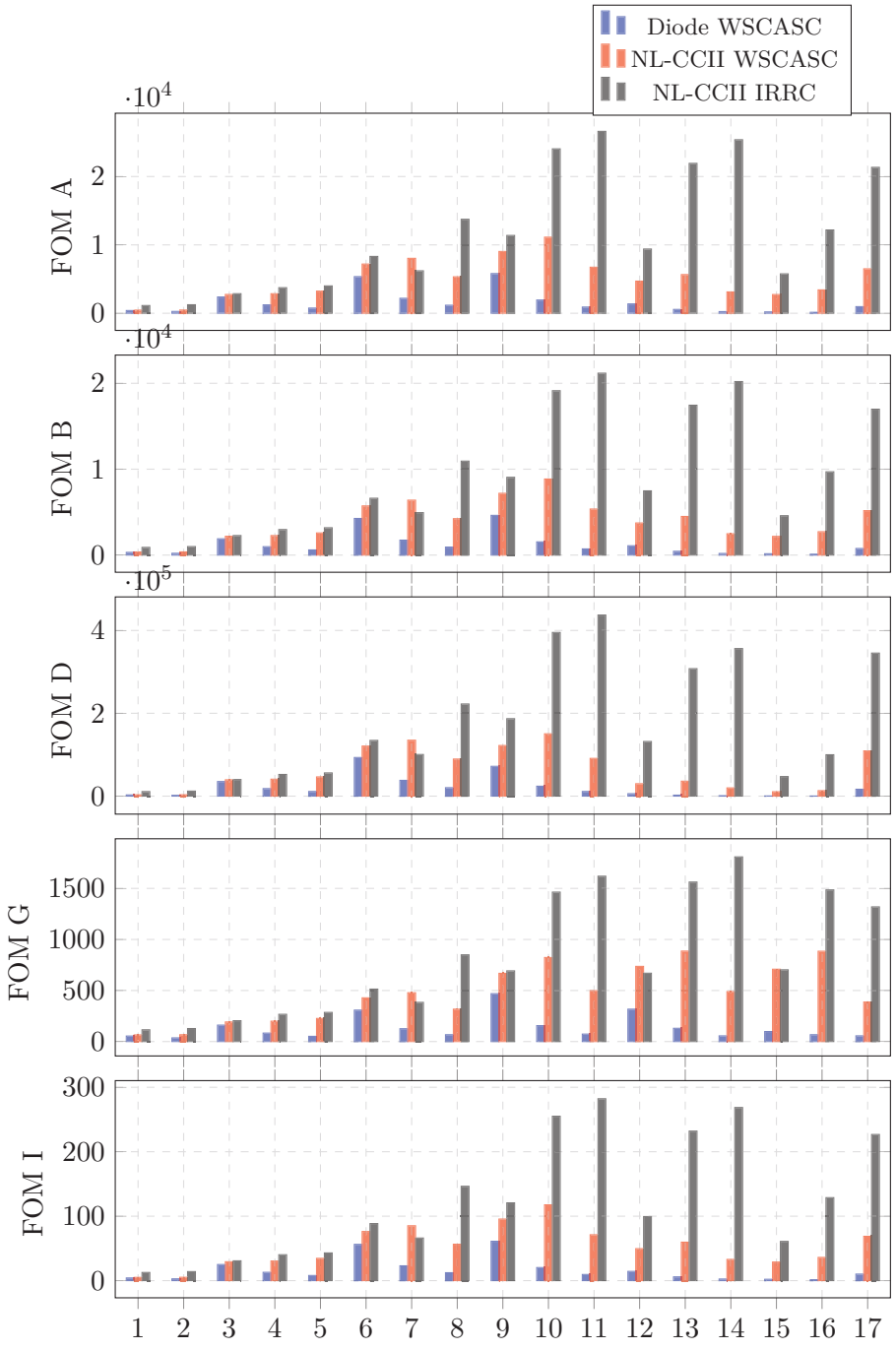

FIGURE G.10 – Time domain evaluation with metrics of the speed-power-accuracy trade-off

Bibliography

Aggarwal Bhawna, Maneesha Gupta, and Anil Kumar Gupta (2013). "A low voltage wide swing level shifted FVF based current mirror". In: *2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI)*. IEEE. doi: 10.1109/icacci.2013.6637292 (cit. on pp. 28, 146).

— (2016). "A comparative study of various current mirror configurations: Topologies and characteristics". In: *Microelectronics Journal* 53, pp. 134–155. doi: 10.1016/j.mejo.2016.04.015 (cit. on p. 23).

Alves Luis Nero and Rui Luis Aguiar (2002). "Frequency behavior of classical current mirrors [CMOS]". In: *9th International Conference on Electronics, Circuits and Systems*. IEEE. doi: 10.1109/icecs.2002.1045365 (cit. on pp. 42, 43).

Amaya Andres, Guillermo Espinosa, and Rodolfo Villamizar (2014). "A robust to PVT variations low-voltage low-power current mirror". In: *2014 IEEE 5th Latin American Symposium on Circuits and Systems*. IEEE. doi: 10.1109/lascas.2014.6820256 (cit. on pp. 28, 146).

Bastos Jose et al. (1997). "Mismatch Characterization of Submicron MOS Transistors". In: *Analog Integrated Circuits and Signal Processing* 12.2, pp. 95–106. doi: 10.1023/a:1008256724276 (cit. on p. 15).

Bennie Scott et al. (2002). "Toward the optimal waveform for electrical stimulation of human muscle". In: *European Journal of Applied Physiology* 88.1-2, pp. 13–19. doi: 10.1007/s00421-002-0711-4 (cit. on p. 111).

Bhadra Narendra (2015). *Physiological principles of electrical stimulation*. Elsevier, pp. 13–43. doi: 10.1016/b978-1-78242-101-6.00002-1 (cit. on p. 110).

Biolek Dalibor et al. (2008). "Active elements for analog signal processing: classification, review, and new proposals". In: *Radioengineering* 17.4, pp. 15–32 (cit. on p. 18).

Bosch Anne van den, Michiel Steyaert, and Willy Sansen (2001). In: *Analog Integrated Circuits and Signal Processing* 29.3, pp. 173–180. doi: 10.1023/a:1011261330190 (cit. on p. 15).

Capogrosso Marco et al. (2016). "A brain-spine interface alleviating gait deficits after spinal cord injury in primates". In: *Nature* 539.7628, pp. 284–288. doi: 10.1038/nature20118 (cit. on p. 109).

Carvajal Ramon Gonzalez et al. (2005). "The flipped voltage follower: a useful cell for low-voltage low-power circuit design". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 52.7, pp. 1276–1291. doi: 10.1109/tcsi.2005.851387 (cit. on p. 24).

Chen Tao and Georges G. E. Gielen (2007). "A 14-bit 200-MHz Current-Steering DAC With Switching-Sequence Post-Adjustment Calibration". In: *IEEE Journal of Solid-State Circuits* 42.11, pp. 2386–2394. doi: 10.1109/jssc.2007.906200 (cit. on pp. 22, 136, 143).

Cogan Stuart F. (2008). "Neural Stimulation and Recording Electrodes". In: *Annual Review of Biomedical Engineering* 10.1, pp. 275–309. doi: 10.1146/annurev.bioeng.10.061807.160518 (cit. on p. 109).

Cogan Stuart F et al. (2016). "Tissue damage thresholds during therapeutic electrical stimulation". In: *Journal of Neural Engineering* 13.2, p. 021001. doi: 10.1088/1741-2560/13/2/021001 (cit. on p. 109).

Constantinou Loucas, Richard Bayford, and Andreas Demosthenous (2015). "A Wideband Low-Distortion CMOS Current Driver for Tissue Impedance Analysis". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 62.2, pp. 154–158. doi: 10.1109/tcsii.2014.2387632 (cit. on pp. 18, 132, 135, 142).

Deprez Marjolijn et al. (2018). "An evaluation of the effect of pulse-shape on grey and white matter stimulation in the rat brain". In: *Scientific Reports* 8.1. doi: 10.1038/s41598-017-19023-0 (cit. on p. 129).

Esparza-Alfaro Fermin, Antonio J. Lopez-Martin, et al. (2012). "High-performance micropower class AB current mirror". In: *Electronics Letters* 48.14, p. 823. doi: 10.1049/el.2011.3863 (cit. on pp. 27, 136, 145).

Esparza-Alfaro Fermin, Salvatore Pennisi, et al. (2014). "Low-Power Class-AB CMOS Voltage Feedback Current Operational Amplifier With Tunable Gain and Bandwidth". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 61.8, pp. 574–578. doi: 10.1109/tcsii.2014.2327390 (cit. on pp. 21, 86, 87, 136, 143).

Ferri Giuseppe and Nicola C Guerrini (2003). *Low-voltage low-power CMOS current conveyors*. Springer Science and Business Media (cit. on p. 73).

Giagka Vasiliki et al. (2015). "An Implantable Versatile Electrode-Driving ASIC for Chronic Epidural Stimulation in Rats". In: *IEEE Transactions on Biomedical Circuits and Systems* 9.3, pp. 387–400. doi: 10.1109/tbcas.2014.2330859 (cit. on pp. 132, 134).

Gilbert Barrie (2004). "Current Mode, Voltage Mode, or Free Mode? A Few Sage Suggestions". In: *Analog Integrated Circuits and Signal Processing* 38.2/3, pp. 83–101. doi: 10.1023/b:alog.0000011161.44537.da (cit. on p. 11).

Greenbaum Elias and David Zhou (2009). "Implantable Neural Prostheses 1". In: doi: 10.1007/978-0-387-77261-5 (cit. on p. 110).

Greenwald Elliot et al. (2017). "A CMOS Current Steering Neurostimulation Array With Integrated DAC Calibration and Charge Balancing". In: *IEEE Transactions on Biomedical*

Circuits and Systems 11.2, pp. 324–335. DOI: 10.1109/tbcas.2016.2609854 (cit. on pp. 19, 86, 87, 131, 134, 142).

GRUMET Andrew E, John L WYATT, and Joseph F RIZZO (2000). "Multi-electrode stimulation and recording in the isolated retina". In: *Journal of Neuroscience Methods* 101.1, pp. 31–42. DOI: 10.1016/s0165-0270(00)00246-6 (cit. on p. 110).

GUIRAUD David et al. (2016). "Vagus nerve stimulation: state of the art of stimulation and recording strategies to address autonomic function neuromodulation". In: *Journal of Neural Engineering* 13.4, p. 041002. DOI: 10.1088/1741-2560/13/4/041002 (cit. on p. 110).

JESPERS Paul G. A. and Boris MURMANN (2015). "Calculation of MOSFET distortion using the transconductance-to-current ratio". In: *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. DOI: 10.1109/iscas.2015.7168687 (cit. on p. 16).

JULIEN Mohan et al. (2017a). "Formal analysis of bandwidth enhancement for high-performance active-input current mirror". In: *2017 12th International Conference on Design Technology of Integrated Systems In Nanoscale Era (DTIS)*. DOI: 10.1109/DTIS.2017.7930162.

— (2017b). "Formal analysis of high-performance stabilized active-input current mirror". In: *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. DOI: 10.1109/ISCAS.2017.8051012.

— (2018). "Improvement of Active-Input Current Mirrors Using Adaptive Biasing Technique". In: *2018 33nd Conference on Design of Circuits and Integrated Systems (DCIS)*.

— (2019). "Breaking the speed-power-accuracy trade-off in current mirror with non-linear CCII feedback". In: *Microelectronics Journal* 83. ISSN: 0026-2692. DOI: https://doi.org/10.1016/j.mejo.2018.11.016.

KILLIAN Matthijs, Ernst von WALLENBERG, and Guido SMOORENBURG (2008). *Pulse burst electrical stimulation of nerve or tissue fibers*. US Patent 7,333,858 (cit. on p. 111).

KINGET Peter R. (2005). "Device mismatch and tradeoffs in the design of analog circuits". In: *IEEE Journal of Solid-State Circuits* 40.6, pp. 1212–1224. DOI: 10.1109/jssc.2005.848021 (cit. on pp. 15, 16, 29, 98).

KINGET Peter R. and Michiel STEYAERT (1996). "Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits". In: *Proceedings of Custom Integrated Circuits Conference*. IEEE. DOI: 10.1109/cicc.1996.510569 (cit. on pp. 16, 22).

KOLIOPOULOS Costas and Costas PSYCHALINOS (2007). "A Comparative Study of the Performance of the Flipped Voltage Follower Based Low-Voltage Current Mirrors". In: *2007 International Symposium on Signals, Circuits and Systems*. IEEE. DOI: 10.1109/isscs.2007.4292650 (cit. on pp. 24, 145).

Lam Yat-Hei and Wing-Hung Ki (2008). "A 0.9V 0.35um Adaptively Biased CMOS LDO Regulator with Fast Transient Response". In: *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers*. IEEE. DOI: 10.1109/isscc.2008.4523247 (cit. on pp. 17, 87, 141).

Lamlih Achraf et al. (2018). "Wideband Fully Differential Current Driver with Optimized Output Impedance for Bioimpedance Measurements". In: *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. DOI: 10.1109/iscas.2018.8351464 (cit. on pp. 18, 132, 135, 142).

Liu Xilin et al. (2014). "Design of a net-zero charge neural stimulator with feedback control". In: DOI: 10.1109/biocas.2014.6981770 (cit. on pp. 19, 131, 134, 142).

Luo Zhicong and Ming-Dou Ker (2016). "A High-Voltage-Tolerant and Precise Charge-Balanced Neuro-Stimulator in Low Voltage CMOS Process". In: *IEEE Transactions on Biomedical Circuits and Systems* 10.6, pp. 1087–1099. DOI: 10.1109/tbcas.2015.2512443 (cit. on pp. 86, 87, 131, 134).

Maity Ashis and Amit Patra (2016). "Design and Analysis of an Adaptively Biased Low-Dropout Regulator Using Enhanced Current Mirror Buffer". In: *IEEE Transactions on Power Electronics* 31.3, pp. 2324–2336. DOI: 10.1109/tpel.2015.2432913 (cit. on pp. 17, 141).

McDonnell Samantha M. et al. (2017). "Compensation and Calibration Techniques for Current-Steering DACs". In: *IEEE Circuits and Systems Magazine* 17.2, pp. 4–26. DOI: 10.1109/mcas.2017.2689518 (cit. on p. 21).

Merrill Daniel R., Marom Bikson, and John G.R. Jefferys (2005). "Electrical stimulation of excitable tissue: design of efficacious and safe protocols". In: *Journal of Neuroscience Methods* 141.2, pp. 171–198. DOI: 10.1016/j.jneumeth.2004.10.020 (cit. on p. 109).

Minch Bradley A. (2007). "Low-Voltage Wilson Current Mirrors in CMOS". In: *2007 IEEE International Symposium on Circuits and Systems*. IEEE. DOI: 10.1109/iscas.2007.378723 (cit. on p. 28).

Mita Rosario, Gaetano Palumbo, and Salvatore Pennisi (2003). "1.5-V CMOS CCII+ with high current-driving capability". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 50.4, pp. 187–190. DOI: 10.1109/tcsii.2003.809715 (cit. on pp. 20, 86, 87, 136, 143).

Moazzeni Shahaboddin and Glenn E. R. Cowan (2009). "Application of active current mirrors to improve the speed of analog decoder circuits". In: *2009 52nd IEEE International Midwest Symposium on Circuits and Systems*. IEEE. DOI: 10.1109/mwscas.2009.5236145 (cit. on pp. 18, 50).

Mulder Jan et al. (1996). "High-swing cascode MOS current mirror". In: *Electronics Letters* 32.14, p. 1251. DOI: 10.1049/el:19960857 (cit. on p. 25).

Nairn David G. and C. Andre T. Salama (1990). "Current-mode algorithmic analog-to-digital converters". In: *IEEE Journal of Solid-State Circuits* 25.4, pp. 997–1004. DOI: 10.1109/4.58292 (cit. on pp. 18, 50).

Or Pui Ying and Ka Nang Leung (2010). "A Fast-Transient Low-Dropout Regulator With Load-Tracking Impedance Adjustment and Loop-Gain Boosting Technique". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 57.10, pp. 757–761. DOI: 10.1109/tcsii.2010.2058590 (cit. on pp. 17, 141).

Palmisano Giuseppe, Gaetano Palumbo, and Salvatore Pennisi (2000). "Solutions for CMOS current amplifiers with high-drive output stages". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 47.10, pp. 988–998. DOI: 10.1109/82.877141 (cit. on pp. 21, 87, 136, 143).

Pelgrom Marcel J. M., Aad C. J. Duinmaijer, and Anton P. G. Welbers (1989). "Matching properties of MOS transistors". In: *IEEE Journal of Solid-State Circuits* 24.5, pp. 1433–1439. DOI: 10.1109/jssc.1989.572629 (cit. on pp. 13–15).

Pelgrom Marcel J. M., Hans P. Tuinhout, and Maarten Vertregt (1998). "Transistor matching in analog CMOS applications". In: *International Electron Devices Meeting 1998. Technical Digest*. IEEE. DOI: 10.1109/iedm.1998.746503 (cit. on p. 15).

Pennisi Salvatore (2002). "A low-voltage design approach for class AB current-mode circuits". In: *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing* 49.4, pp. 273–279. DOI: 10.1109/tcsii.2002.801463 (cit. on pp. 27, 145).

Pietrobelli A et al. (1998). "Appendicular skeletal muscle mass: prediction from multiple frequency segmental bioimpedance analysis". In: *European Journal of Clinical Nutrition* 52.7, pp. 507–511. DOI: 10.1038/sj.ejcn.1600592 (cit. on p. 129).

Polasek Katharine H. et al. (2009). "Stimulation Stability and Selectivity of Chronically Implanted Multicontact Nerve Cuff Electrodes in the Human Upper Extremity". In: *IEEE Transactions on Neural Systems and Rehabilitation Engineering* 17.5, pp. 428–437. DOI: 10.1109/tnsre.2009.2032603 (cit. on p. 110).

Ramirez-Angulo Jaime (1994). "Current mirrors with low input and low output voltage requirements". In: *Proceedings of 1994 37th Midwest Symposium on Circuits and Systems*. IEEE. DOI: 10.1109/mwscas.1994.519201 (cit. on p. 25).

Ramirez-Angulo Jaime, Ramon Gonzalez Carvajal, and Antonio J. Lopez-Martin (2007). "Single Transistor High-Impedance Tail Current Source With Extended Common-Mode Input Range and Reduced Supply Requirements". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 54.7, pp. 581–585. DOI: 10.1109/tcsii.2007.896817 (cit. on p. 28).

Ramirez-Angulo Jaime, Ramon Gonzalez Carvajal, and Antonio Torralba (2004). "Low Supply Voltage High-Performance CMOS Current Mirror With Low Input and Output Voltage Requirements". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 51.3, pp. 124–129. DOI: 10.1109/tcsii.2003.822429 (cit. on pp. 27, 145).

Razavi Behzad (2001). *Design of Analog CMOS Integrated Circuits*. 1st ed. New York, NY, USA: McGraw-Hill, Inc., pp. 369–370. isbn: 0072380322, 9780072380323 (cit. on p. 61).

Sackinger Eduard and Walter Guggenbuhl (1990). "A high-swing, high-impedance MOS cascode circuit". In: *IEEE Journal of Solid-State Circuits* 25.1, pp. 289–298. doi: 10.1109/4.50316 (cit. on p. 25).

Safari Leila and Shahram Minaei (2016). "A simple low voltage, high output impedance resistor based current mirror with extremely low input and output voltage requirements". In: *2016 39th International Conference on Telecommunications and Signal Processing (TSP)*. IEEE. doi: 10.1109/tsp.2016.7760872 (cit. on pp. 27, 145).

Sahin Mesut and Yanmei Tie (2007). "Non-rectangular waveforms for neural stimulation with practical electrodes". In: *Journal of Neural Engineering* 4.3, p. 227 (cit. on p. 110).

Sanchez Benjamin et al. (2012). "Basics of broadband impedance spectroscopy measurements using periodic excitations". In: *Measurement Science and Technology* 23.10, p. 105501. doi: 10.1088/0957-0233/23/10/105501 (cit. on p. 111).

Schmid Hanspeter (2003). In: *Analog Integrated Circuits and Signal Processing* 35.1, pp. 79–90. doi: 10.1023/a:1023477605076 (cit. on p. 11).

Sedra Adel and Kenneth Smith (1970). "A second-generation current conveyor and its applications". In: *IEEE Transactions on Circuit Theory* 17.1, pp. 132–134. doi: 10.1109/tct.1970.1083067 (cit. on p. 70).

Serrano Teresa and Bernabe Linares-Barranco (1994). "The active-input regulated-cascode current mirror". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 41.6, pp. 464–467. doi: 10.1109/81.295247 (cit. on pp. 26, 50).

Serrano Teresa, Bernabe Linares-Barranco, and A.G. Andreou (1999). "Very wide range tunable CMOS bipolar current mirrors with voltage clamped input". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 46.11, pp. 1398–1407. doi: 10.1109/81.802845 (cit. on p. 27).

Silveira Fernando, Denis Flandre, and Paul G. A. Jespers (1996). "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower (OTA)". In: *IEEE Journal of Solid-State Circuits* 31.9, pp. 1314–1319. doi: 10.1109/4.535416 (cit. on p. 16).

Sit Ji-Jon and Rahul Sarpeshkar (2007). "A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6nA DC error for 1-mA full-scale stimulation". In: *IEEE Transactions on Biomedical Circuits and Systems* 1.3, pp. 172–183. doi: 10.1109/tbcas.2007.911631 (cit. on pp. 19, 86, 87, 134, 142).

Swanson Eric J (1986). *Mixed threshold current mirror*. US Patent 4,618,815 (cit. on p. 23).

Sweeney J.D., D.A. Ksienski, and J.T. Mortimer (1990). "A nerve cuff technique for selective excitation of peripheral nerve trunk regions". In: *IEEE Transactions on Biomedical Engineering* 37.7, pp. 706–715. DOI: 10.1109/10.55681 (cit. on p. 110).

Torralba Antonio et al. (2003). "New output stage for low supply voltage, high-performance CMOS current mirrors". In: *Proceedings of the 2003 International Symposium on Circuits and Systems, 2003. ISCAS.* IEEE. DOI: 10.1109/iscas.2003.1205552 (cit. on pp. 28, 136, 146).

Vajpayee Prateek et al. (2010). "Low voltage regulated cascode current mirrors suitable for sub-1V operation". In: *2010 IEEE Asia Pacific Conference on Circuits and Systems.* IEEE. DOI: 10.1109/apccas.2010.5774891 (cit. on pp. 28, 136, 146).

Voo Thart Fah and Chris Toumazou (1995). "High-speed current mirror resistive compensation technique". In: *Electronics Letters* 31.4, pp. 248–250. DOI: 10.1049/el:19950207 (cit. on p. 24).

Yeh Ta-Hsun et al. (2001). "Mismatch characterization of 1.8 V and 3.3 V devices in 0.18 um mixed signal CMOS technology". In: *ICMTS 2001. Proceedings of the 2001 International Conference on Microelectronic Test Structures.* IEEE. DOI: 10.1109/icmts.2001.928641 (cit. on p. 13).

You F. et al. (1997). "Am improved tail current source for low voltage applications". In: *IEEE Journal of Solid-State Circuits* 32.8, pp. 1173–1180. DOI: 10.1109/4.604073 (cit. on p. 25).

Yuan Fei (2007). "Design Techniques for Current-Mode Circuits". In: *CMOS Current-Mode Circuits for Data Communications.* Springer US, pp. 13–48. ISBN: 978-0-387-47691-9. DOI: 10.1007/978-0-387-47691-9_2 (cit. on p. 11).

Zeki Ali and H. Kuntman (2000). "High-linearity low-voltage self-cascode class AB CMOS current output stage". In: *2000 IEEE International Symposium on Circuits and Systems. Emerging Technologies for the 21st Century. Proceedings (IEEE Cat No.00CH36353).* Presses Polytech. Univ. Romandes. DOI: 10.1109/iscas.2000.858737 (cit. on pp. 28, 136, 146).

Zeng Tao and Degang Chen (2010). "New calibration technique for current-steering DACs". In: *Proceedings of 2010 IEEE International Symposium on Circuits and Systems.* IEEE. DOI: 10.1109/iscas.2010.5537534 (cit. on p. 22).

List of Publication

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— (2017b). "Formal analysis of high-performance stabilized active-input current mirror". In: *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. DOI: 10.1109/ISCAS.2017.8051012.

— (2018). "Improvement of Active-Input Current Mirrors Using Adaptive Biasing Technique". In: *2018 33nd Conference on Design of Circuits and Integrated Systems (DCIS)*.

— (2019). "Breaking the speed-power-accuracy trade-off in current mirror with non-linear CCII feedback". In: *Microelectronics Journal* 83. ISSN: 0026-2692. DOI: https://doi.org/10.1016/j.mejo.2018.11.016.

RÉSUMÉ

Ce manuscrit porte sur l'analyse, les méthodes de conception et la recherche de nouvelles structures de sources de courant, en se focalisant principalement sur les miroirs de courant, source la plus élémentaire. Le dépassement des limites actuelles pour l'optimisation du compromis vitesse-précision-consommation est l'objectif majeur des travaux présentés. La première partie est consacrée à l'étude de l'origine de ces limites et dresse l'état de l'art des structures de miroir de courant CMOS. Sont ensuite étudiées plus en détails, les possibilités offertes par les miroirs à entrée active. Une des premières contributions de nos travaux de recherche a été de proposer un formalisme dédié à l'étude et à l'implémentation de ce type de miroir, suivi de propositions d'amélioration à coût minimum de la topologie classique. Le développement d'une nouvelle approche de conception utilisant un principe de rétroaction non-linéaire en mode courant constitue la contribution majeure de cette thèse. La rétroaction implémentée grâce à un convoyeur de courant de seconde génération dédié, très faible consommation et conçu pour avoir un comportement volontairement non-linéaire. Couplée avec des techniques classiques de régulation cascode pour une copie en courant de haute-précision, cette topologie constitue une source de courant élémentaire compétitive pour la réalisation de systèmes à haut niveau de performance. L'approche est mise en œuvre puis validée par la conception, en technologie CMOS 180nm, de deux circuits dédiés à la génération des courants dans les puces de stimulation neurale. L'ensemble des résultats obtenus dans ces dernières études démontre, qu'il est possible de dépasser les limites actuelles du compromis vitesse-précision-consommation, en se basant sur la stratégie de conception et les nouvelles topologies de miroirs à entrée active proposées.

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The work presented in this manuscript involves analysis, design methods and search for improved structures of current sources, with main focus on the current mirrors, the most elementary current source. The main objective of our research was to outperform the present limitations in terms of speed, power and accuracy that exists in CMOS current mirror design. In the first part of the manuscript, we investigate on the origin of these limitations and present a literature review of popular and recent advanced current mirror structures. Then follow, a deeper analysis of active-input current mirror capabilities. The first scientific contributions were, the development of analytical tools dedicated to the implementation of the standard active-input topology, supported by two solutions for dynamic range and stability improvements at minimal costs. The proposition of a novel design approach, relying on a power-efficient speed boosting technique based on current-mode non-linear control loops, constitutes the major contribution of the work presented in this manuscript. The feedback circuit is implemented using a custom low-power current conveyor (CCII), built to be intentionally non-linear. Coupled with classical regulated cascode structures required for high-precision current copy, this enhanced active-input current mirror topology forms a new competitive elementary current source to the design of high-performance systems. The approach is validated and illustrated with the realization of two circuits in 180 nm CMOS technology. Cores of the circuits are two examples of output stages dedicated to neural stimulation chips. Finally, Results of the last studies have demonstrated that, thanks to the design strategy and the new active-input current mirror topologies proposed, it is actually possible to outperform the present limit of the speed-power-accuracy trade-off.

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