Distributed clock generator for synchronous SoC using ADPLL network

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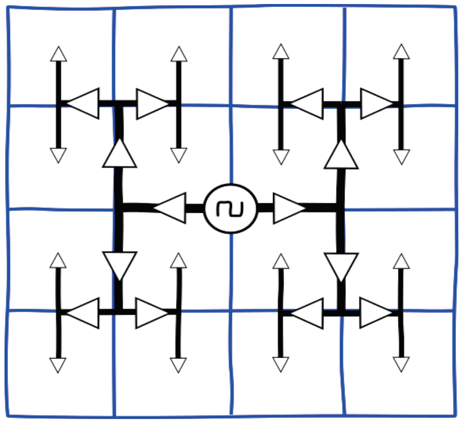
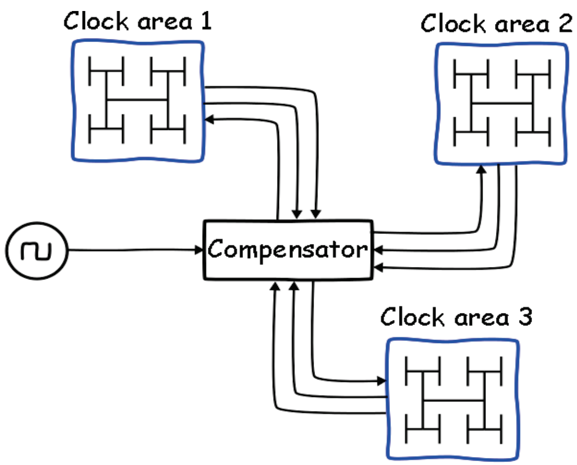
Outline

- Introduction
- Design of the ADPLL clocking network
- Experimental results
- Conclusion

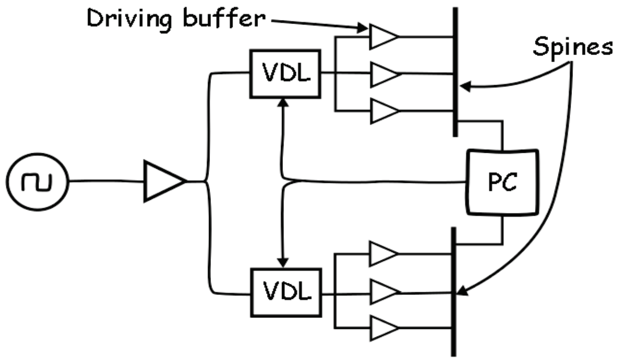
Introduction: conventional clock distribution



Balanced H-tree



Centralized skew compensation [HSIEH98]



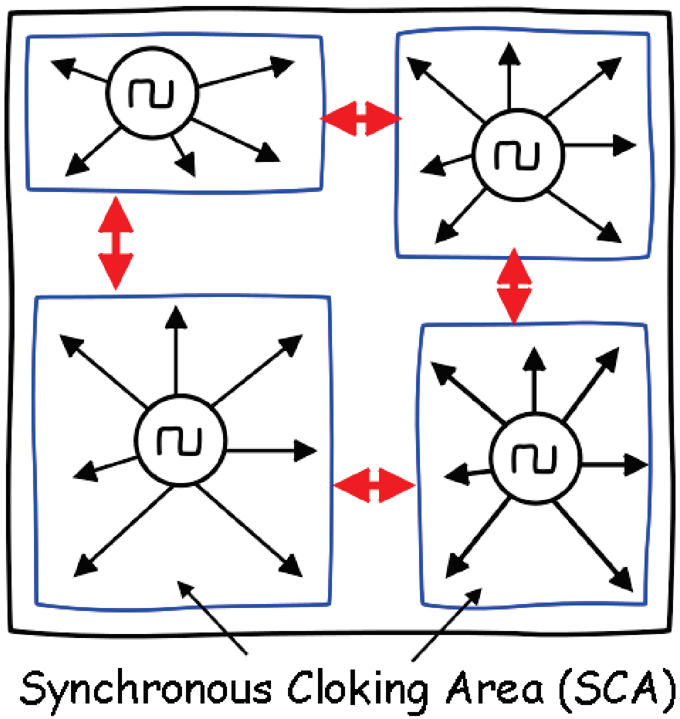
Decentralized skew compensation [SENTH99]

Limitations in advanced technologies:

- Environment perturbations and process variations
- Complex impedance due to parasitic components
- Propagation delay is comparable to clock period
- Power consumption

[HSIEH98] *Hsieh, H. Y., Liu, W., Clements, M., & Franzon, P. Self-calibrating clock distribution with scheduled skews. , ISCAS 98*
[SENTH99] *Senthinathan, R., Fischer, S., Rangchi, H., & Yazdanmehr, H. A 600 MHz IA-32 microprocessor with enhanced data streaming for graphics and video. , ISSCC 99*

Introduction: Globally Asynchronous Locally Synchronous (GALS)



Drawbacks:

- Asynchronous interfaces are generally have lower bandwidth
- Verification and debug are challenging tasks
- Reliability is lower than fully synchronous circuits
- Undeterministic behaviour

Introduction: Globally Synchronous Locally Synchronous (GSLS) via distributed clocking

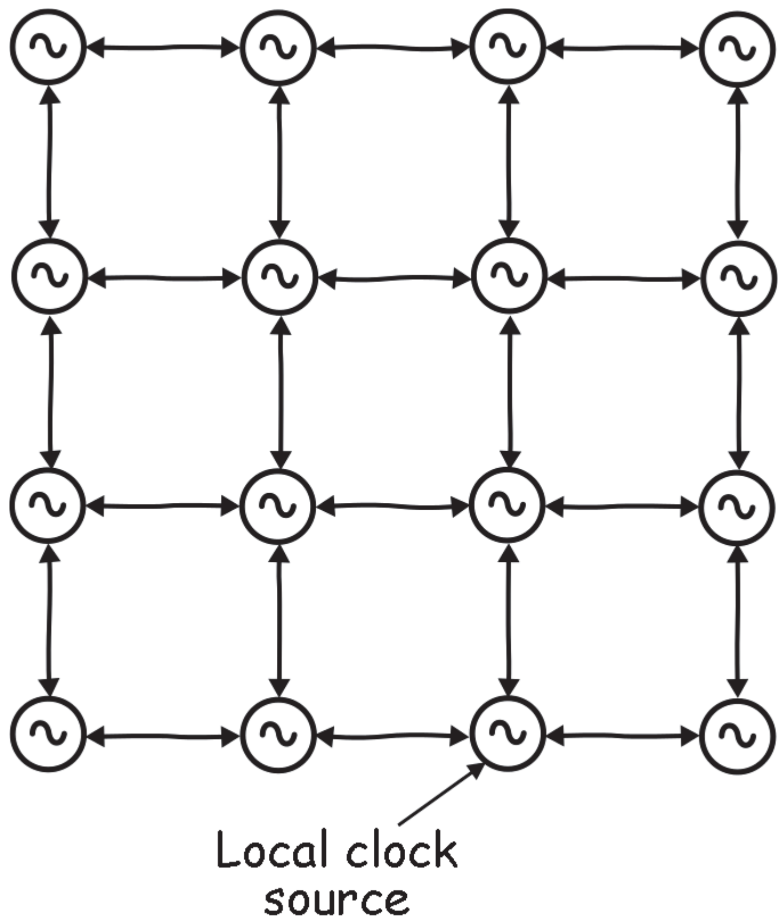
- One synchronous clocking area = one clock source
- Clock sources are synchronized in frequency and phase by local links

Advantages:

- No global clock distribution links
- Regular structure
- No accumulative error
- Good extensibility

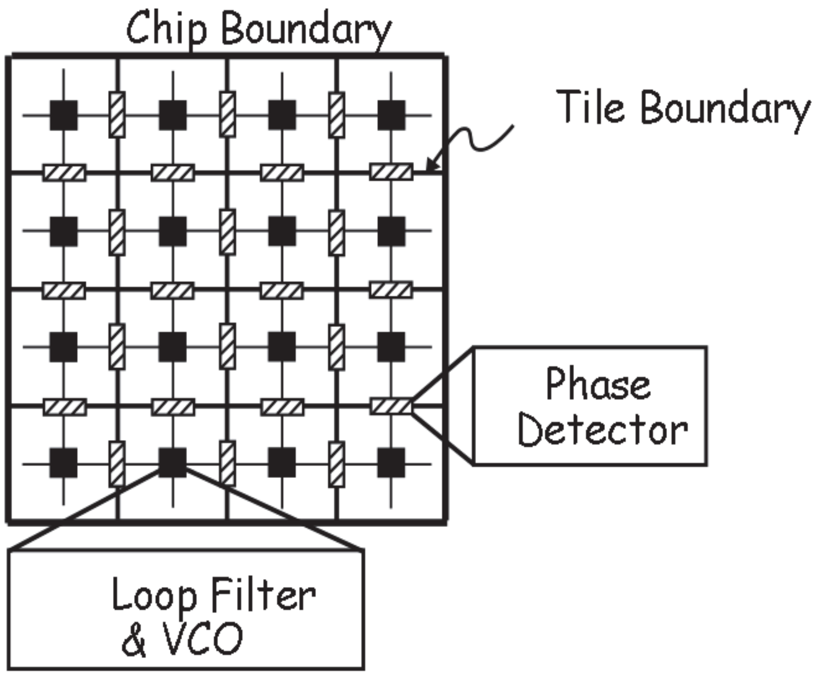
Drawbacks:

- Understudied approach
- Not industrially proven
- Synchronous communication limited to the neighboring zones



State of the art: phase coupling by Phase-Locked Loops

- Gill Pratt and John Nguyen [Pratt95]:
  - Theoretical basement is established
- V. Gutnik and A. Chandrakasan [Gutnik2000]:
  - First silicon prototype introduced
  - Analog phase-locked loops (PLLs) as local clock generators

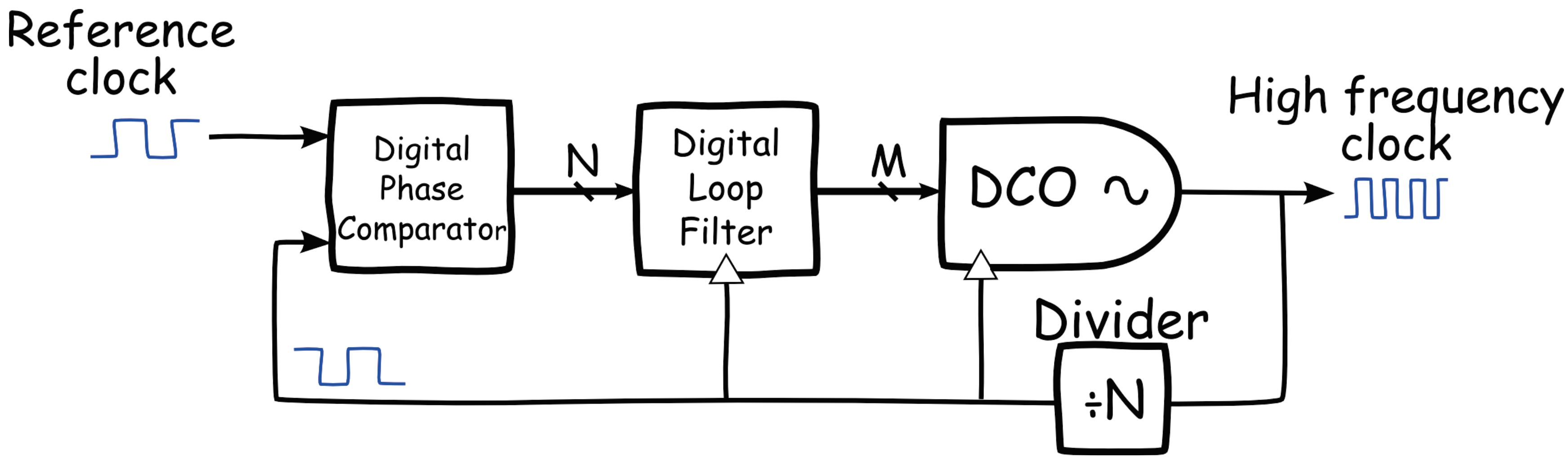


Disadvantages:

- Performance of PLLs is sensitive to the PVT variation and noise of digital circuits
- The design flow of analog circuits is incompatible with the design flow of digital circuits

[PRATT1995] Pratt, G.A., Nguyen J., “ Distributed synchronous clocking ”, February 1995
[GUTNIK2000] V. Gutnik and A. Chandrakasan “Active GHz clock network using distributed PLLs”, ISSCC 2000

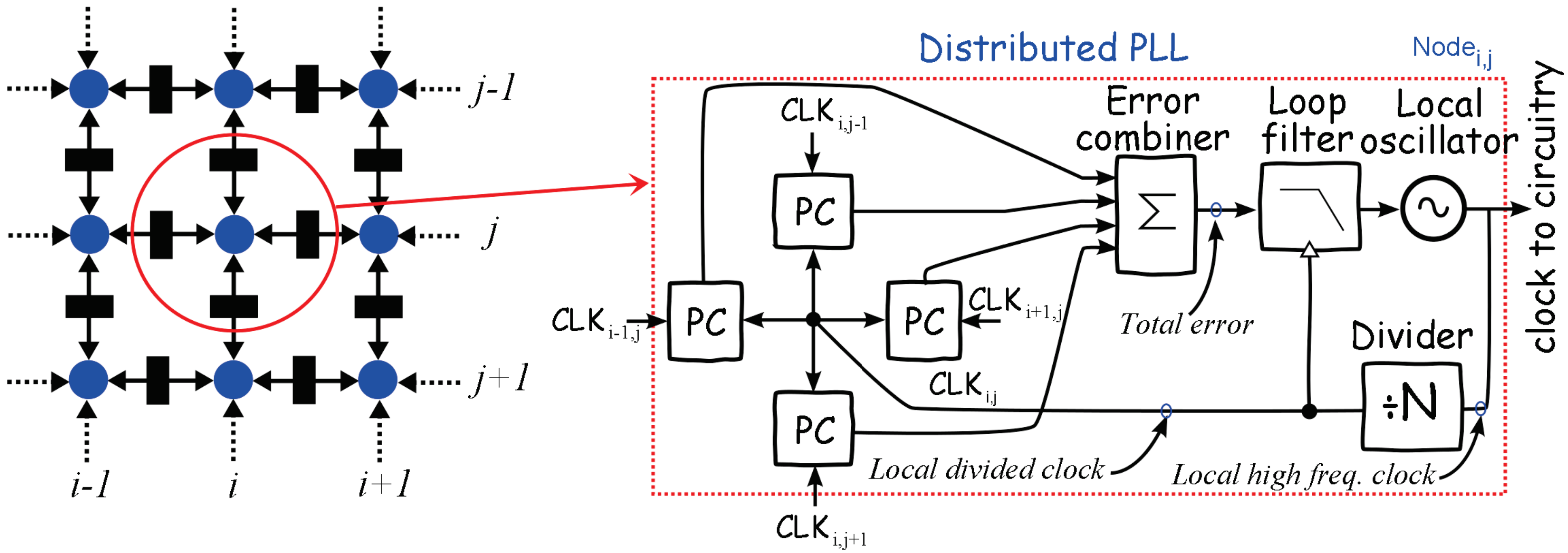
Proposed solution: PLL => ADPLL



All Digital Phase Locked Loop (ADPLL) – digital replacement of analog PLL

- Distributed oscillators coupled in phase by ADPLLs
- Phase Comparator (DPC) and Oscillators (DCO) are digital
- Signal processing in the digital domain by the Loop Filter (DLF)

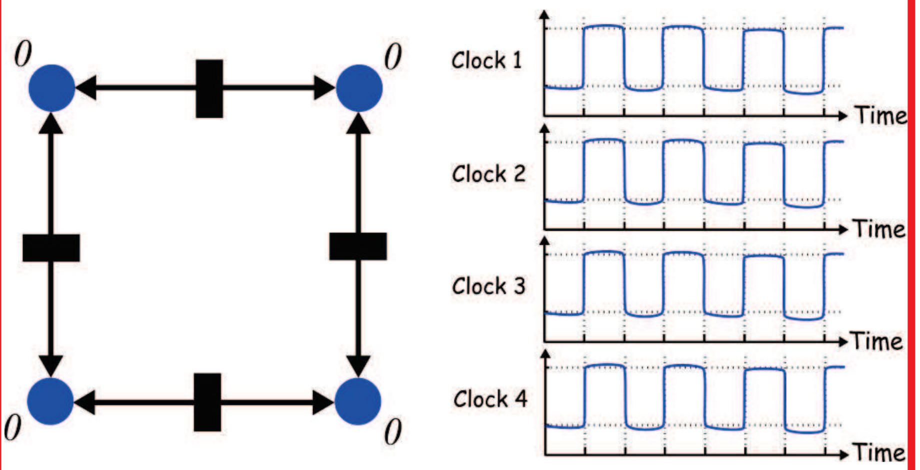
Distributed ADPLL: network configuration & node



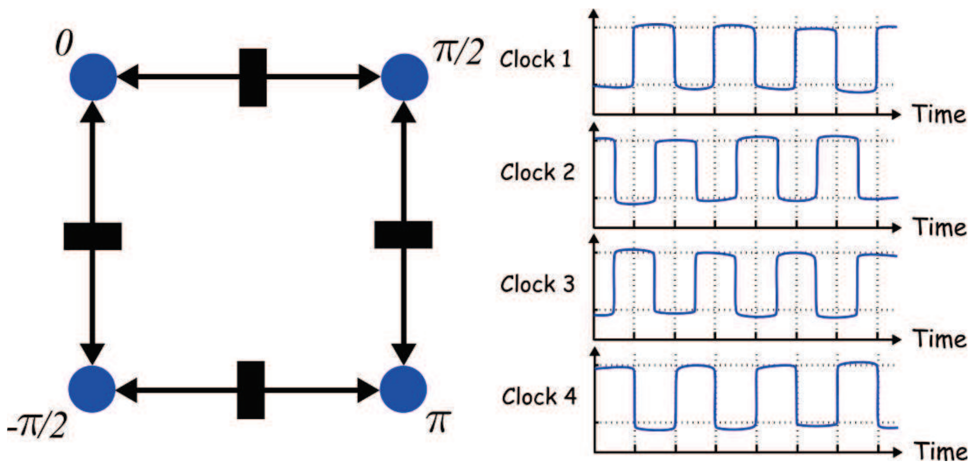
- Network consists of clock sources coupled by phase comparators and controlled by the local control circuitry of ADPLL
- Phase comparators are located between neighbor nodes and shared by them
- Each node processes the error signals from up to four comparators
- The errors are summarized and normalized before processing

Problem: multiple synchronization modes

- Single PLL: if synchronized, than the phase error is always close to zero
- PLL network: can synchronize with zero or nonzero errors
- Actual synchronization mode depends on initial conditions: not controllable

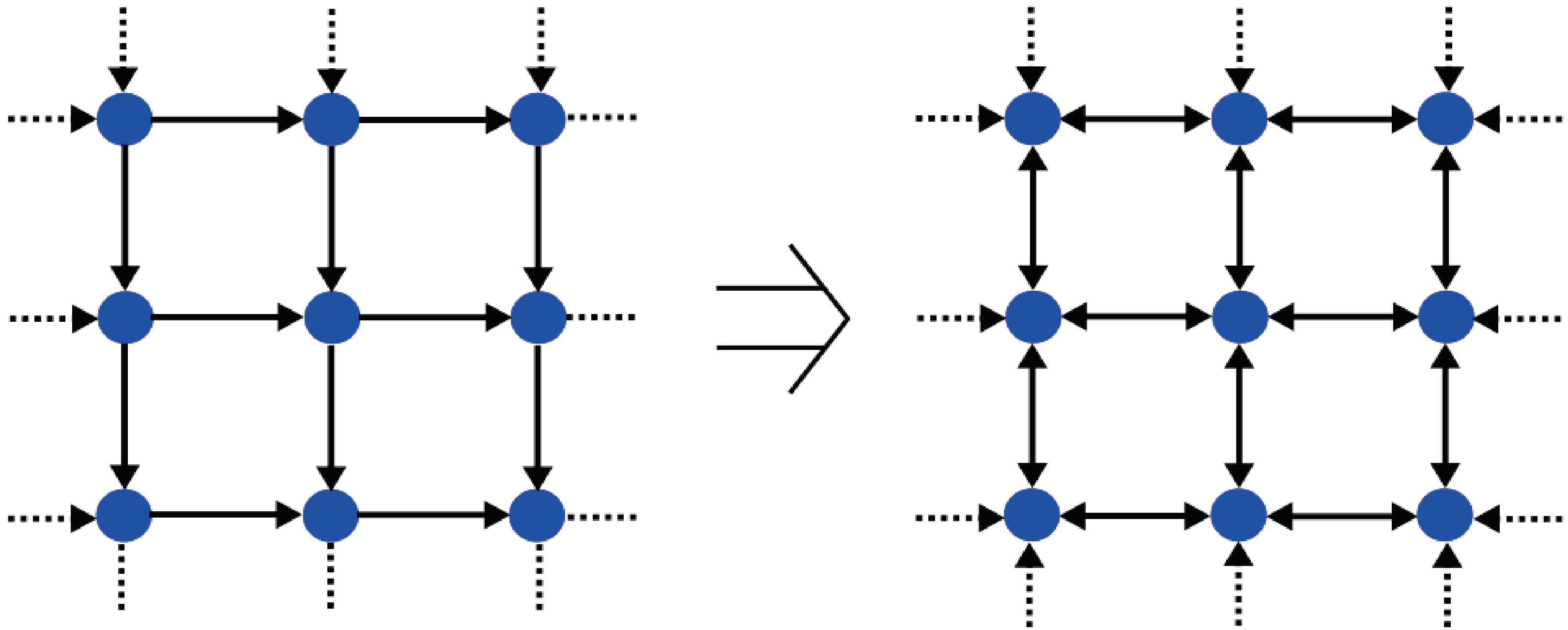


Synchronous mode with zero phase errors (desirable mode)



Synchronous mode with nonzero phase errors (undesirable mode)

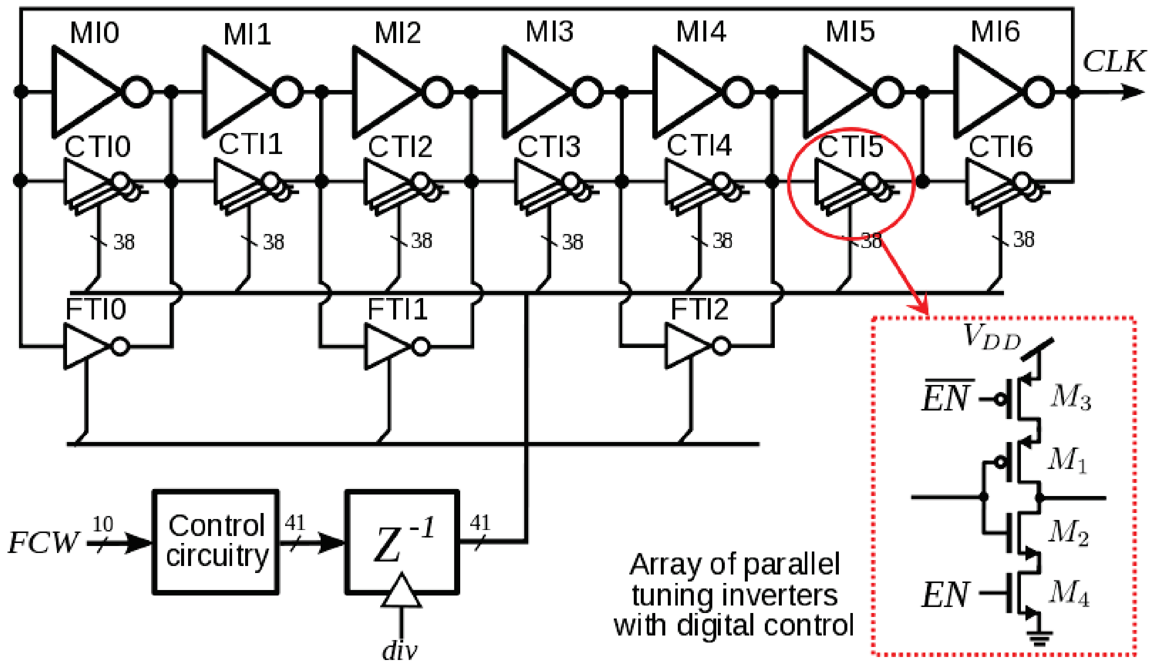
Proposed solution: dynamic synchronization mode selection



Reconfigurable clocking network:

- Network starts in unidirectional configuration and converges with phase errors close to zero
- Network switched to bidirectional configuration and compensate remaining errors

Digitally Controlled Oscillator design



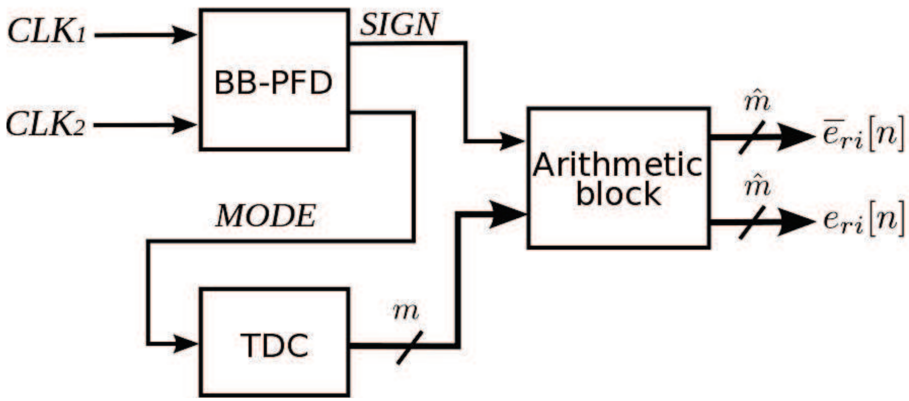
Main parameters:

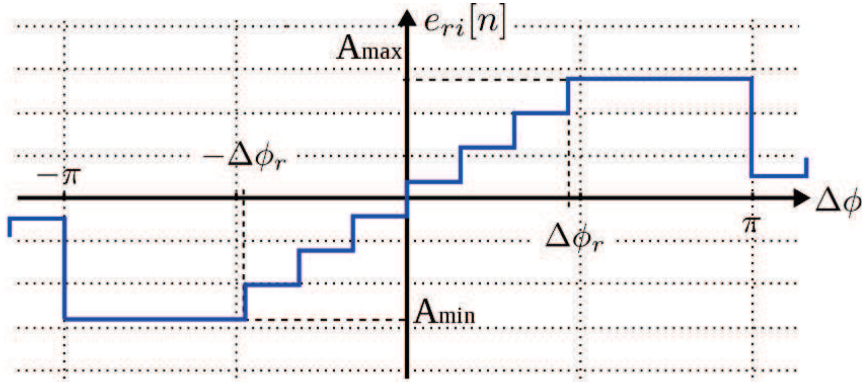
- 1 MHz tuning step
- ±40 % tuning range
- 10 bit resolution
- 1GHz nominal frequency
- Monotonic *F/FCW* characteristic

Architecture features:

- 7 stage main ring
- 256 coarse tuning inverters
- 3 fine tuning inverters
- Binary-thermometer control

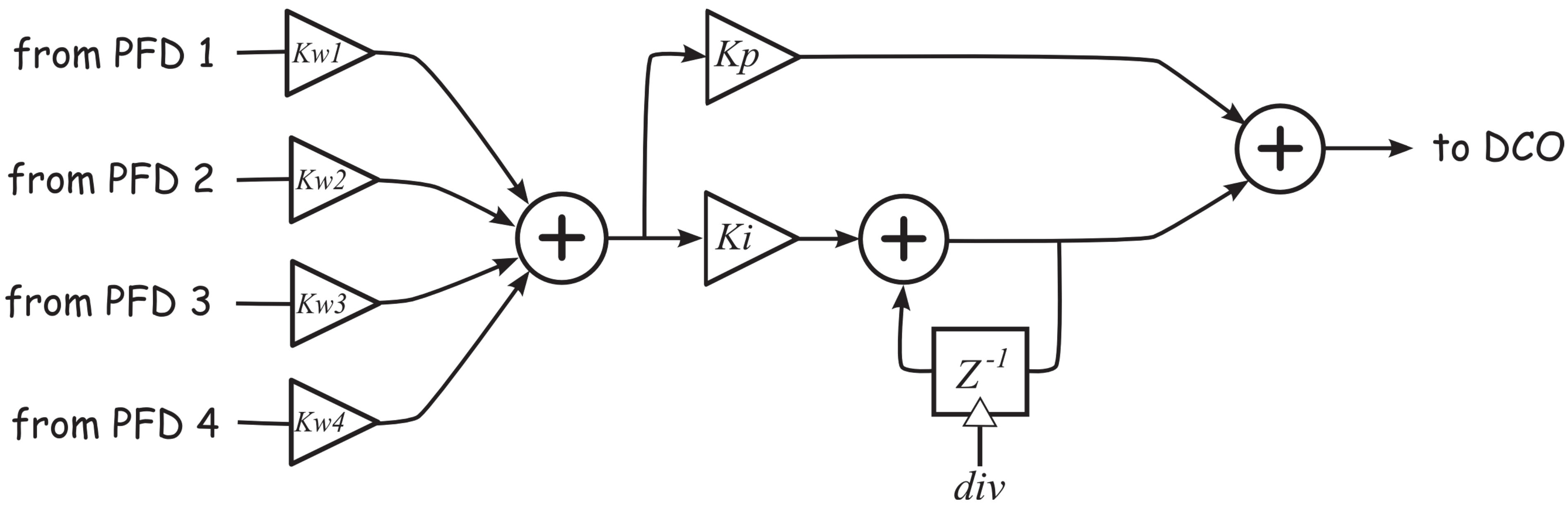
Proposed digital phase/frequency detector





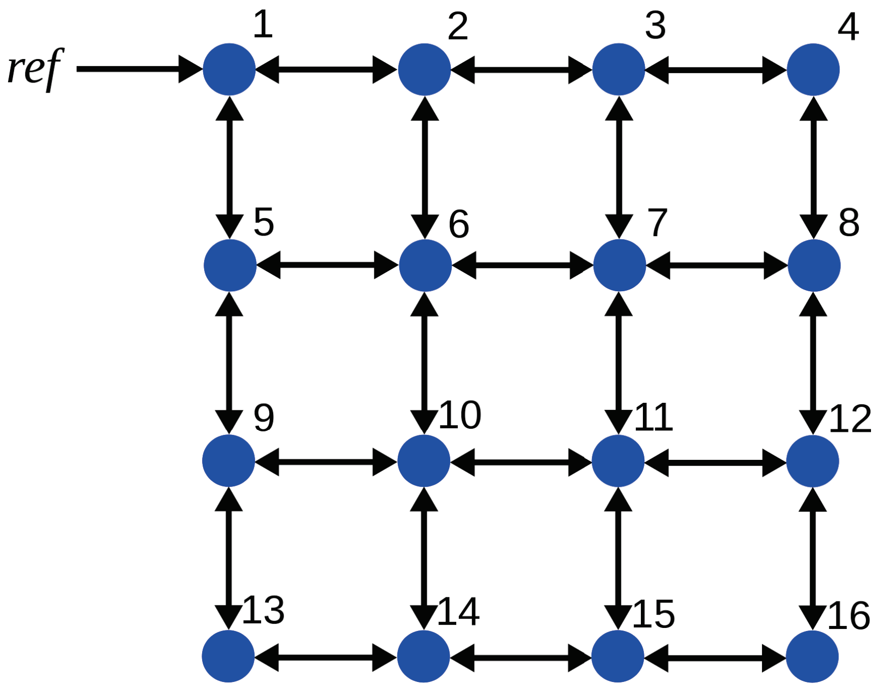
- Bang-bang detector (BB-PFD) detects the sign of the phase/frequency error
- Time-to-digital converter (TDC) quantifies the absolute phase error between input signals
- Arithmetic block combines digital signals and generates signed binary code
- Linear region of transfer function is limited by $\pm\Delta\varphi_r$

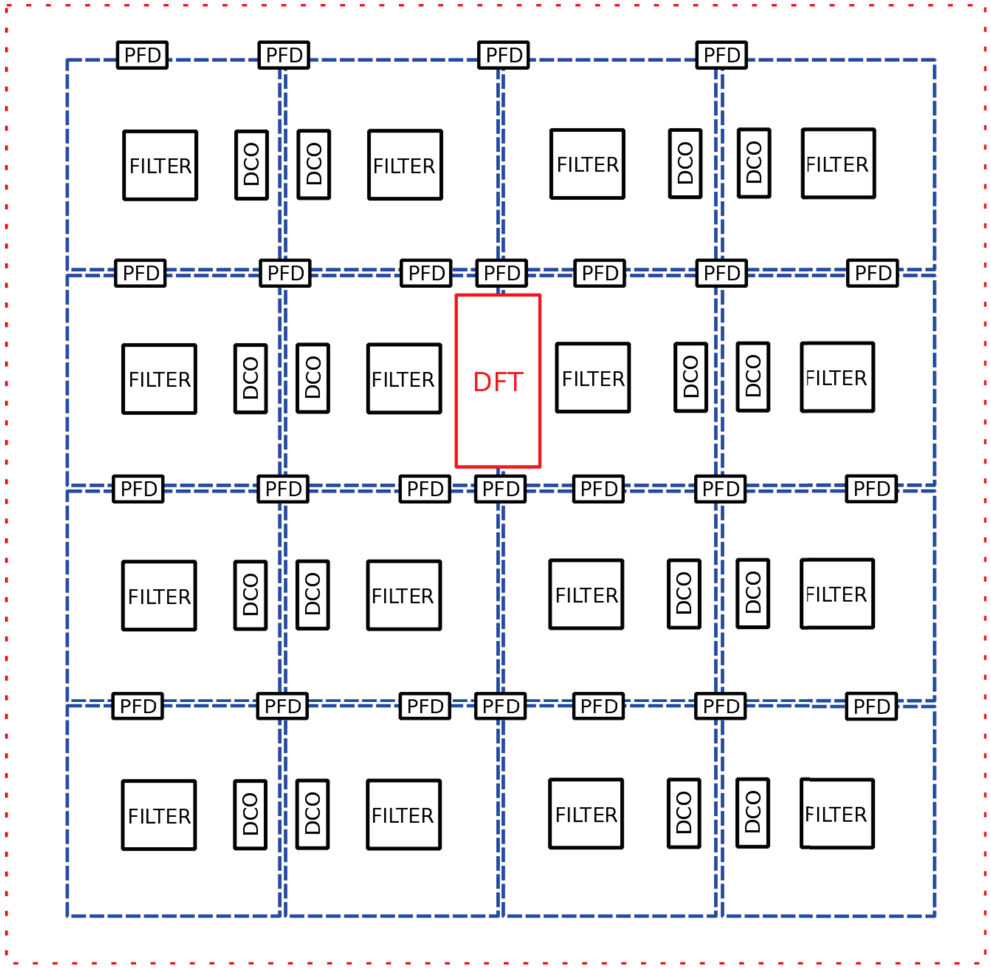
Digital loop control of ADPLL network node



- Switching between two configuration modes during initialization and running
- Sum and normalize the errors with the neighbors
- Proportional-integral filtering (theory says it is a sufficient solution)
- All blocks implemented together in common digital design flow

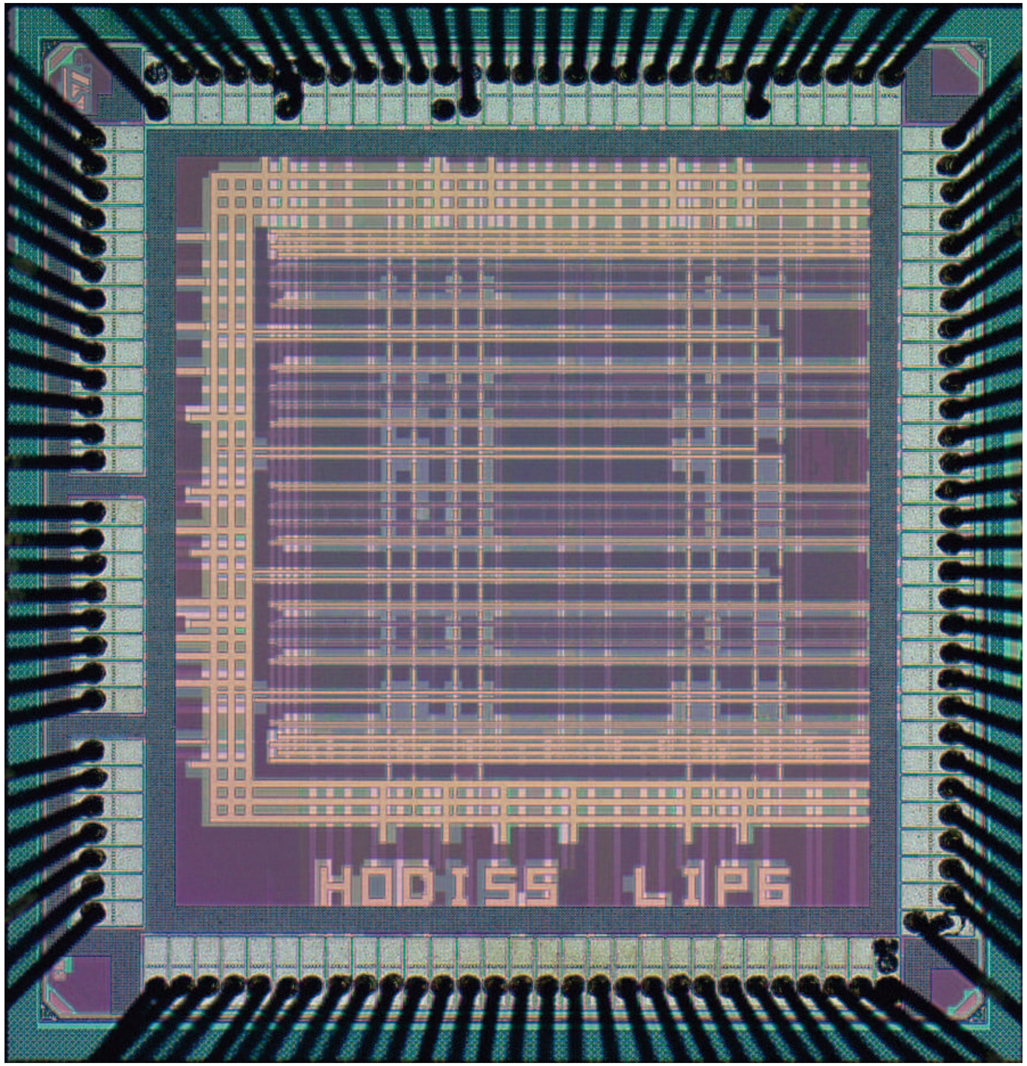
Implementation: floorplan of the test chip





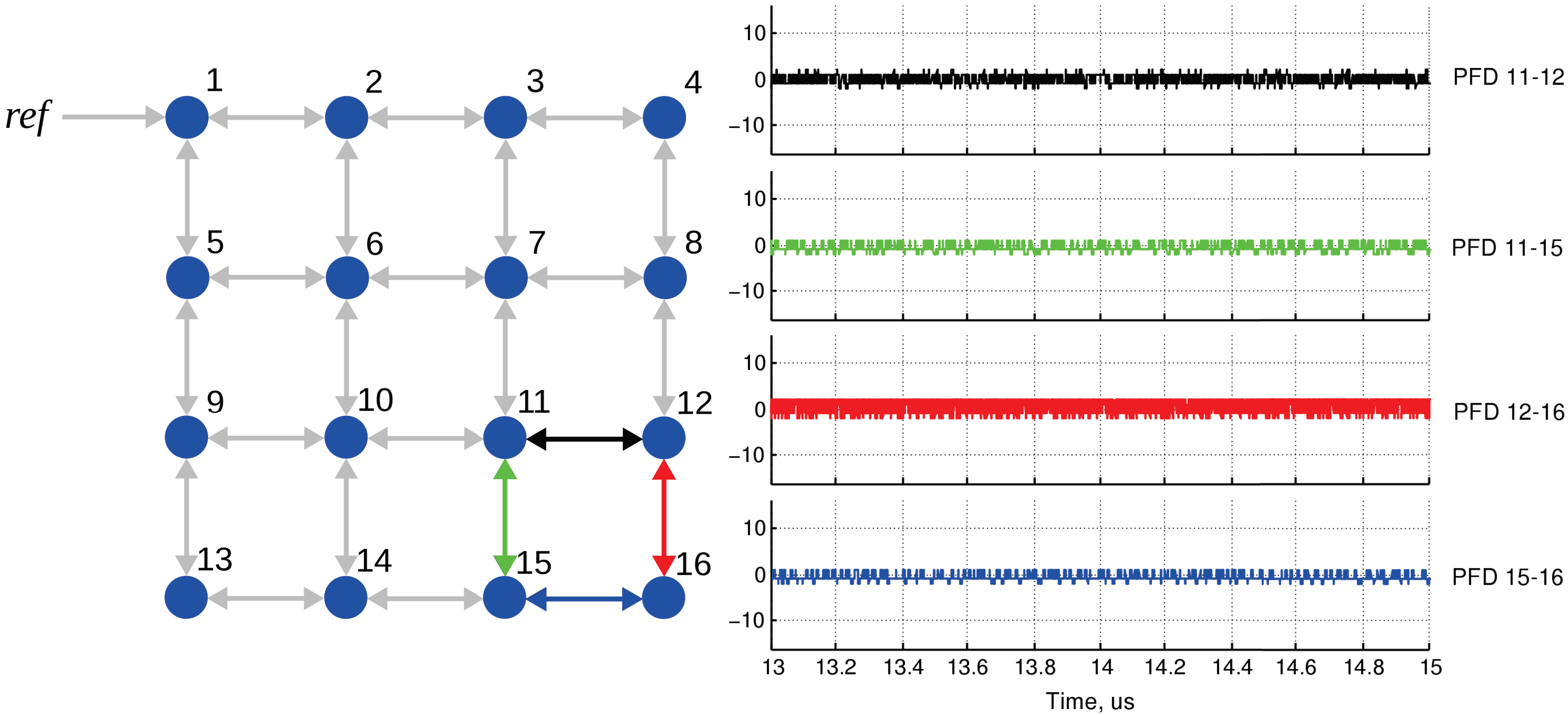
- Blocks are placed within their own clocking areas
- PFDs are located on the borders of clocking areas
- Design-for-Test circuitry is placed at the middle to guarantee the shortest connections

Implementation: microphotograph of the fabricated chip



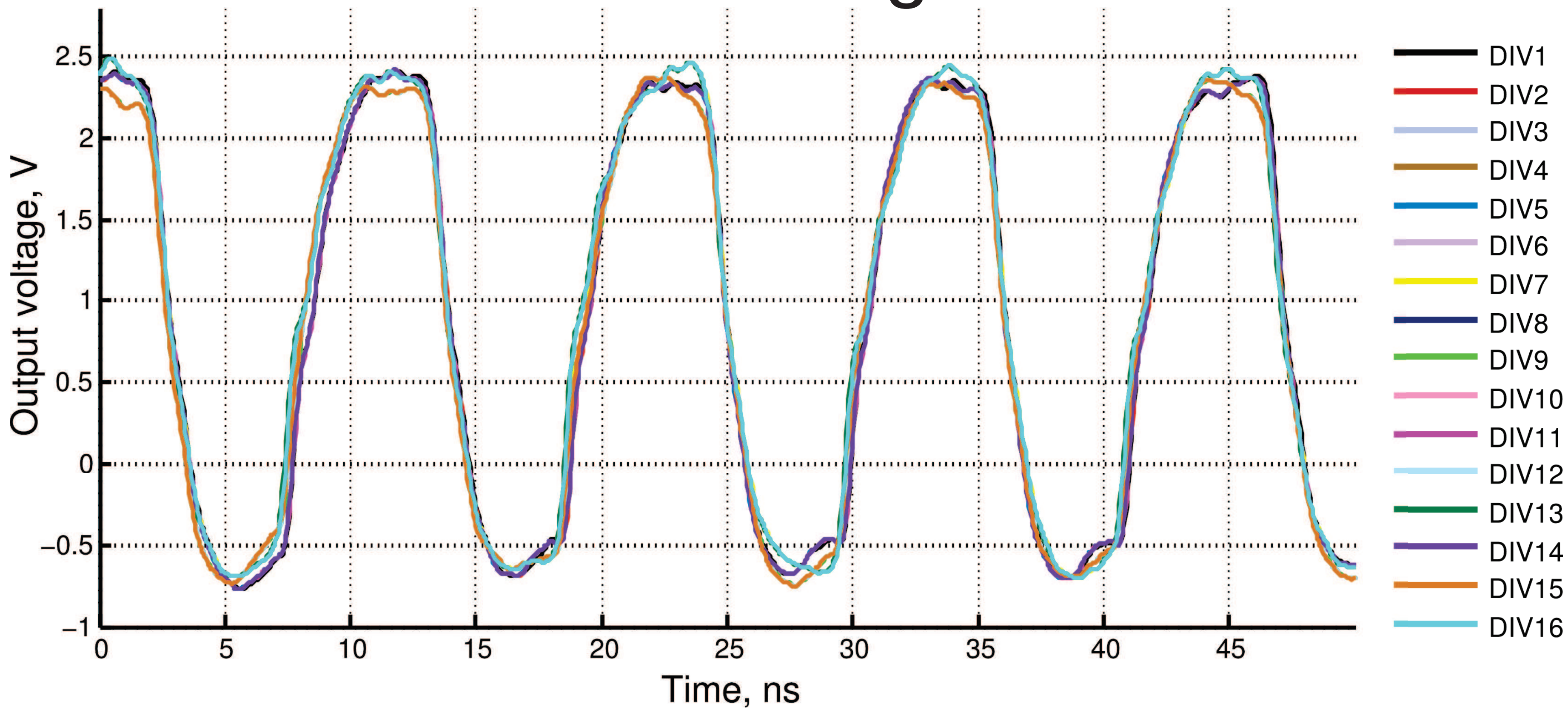
- Dimensions: 1470x1390 µm
- Clocking core: 900x800 µm
- ~ 290 000 transistors
- Operational
- Tested and characterized

On-chip measurement: timing error between neighbors



- Captured outputs of PFDs
- Maximum error is ±2 steps of the PFD resolution, i.e. 30 ps < err < 60 ps

Off-chip measurement: timing error between neighbors

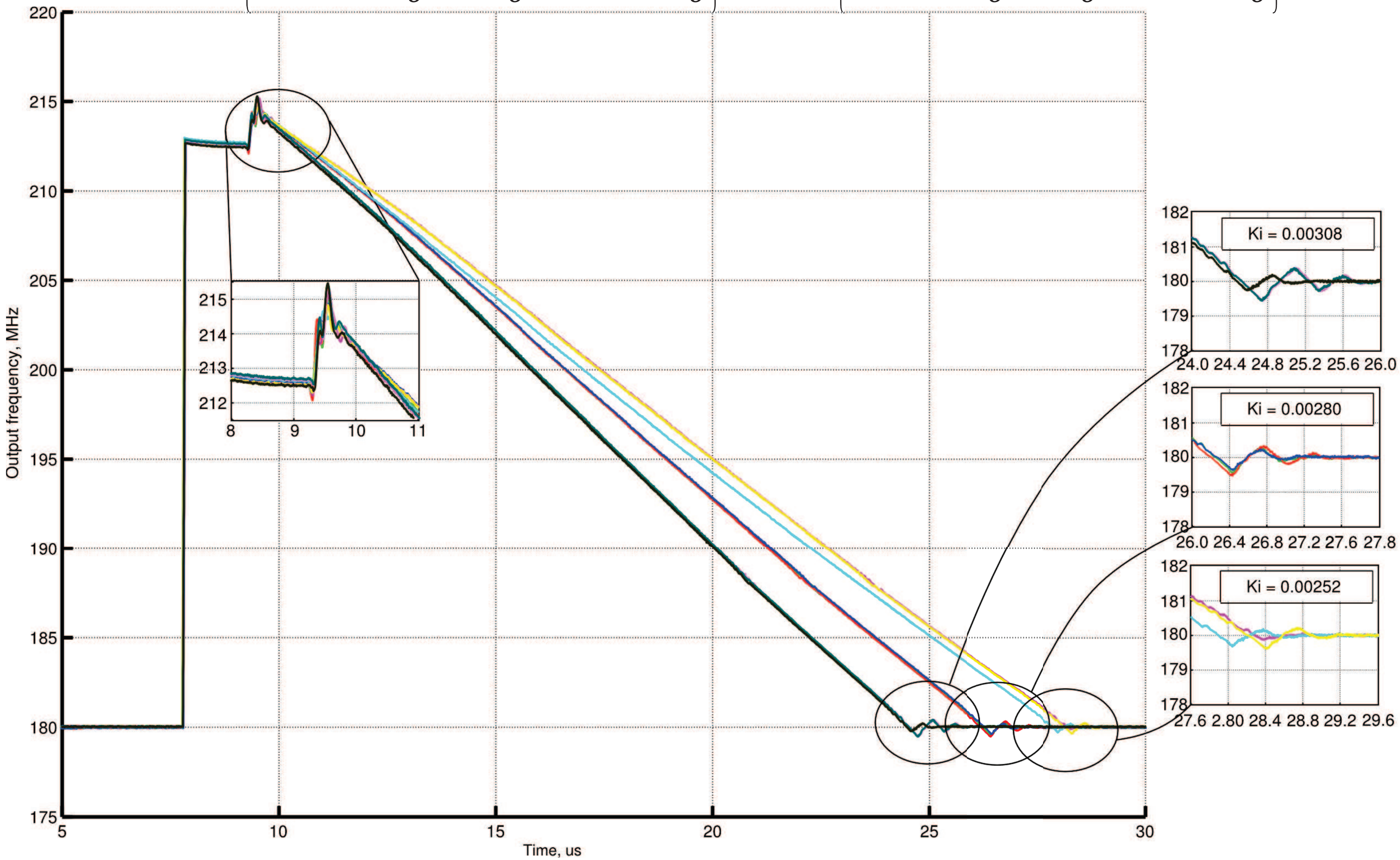


- Captured clocks for all 16 nodes of the network
- Bidirectional configuration of the network
- Reference frequency 180 MHz
- Clock error measured off-chip:
  - for neighboring nodes is 140 < err < 220 ps
  - Between any two nodes is < 300 ps

Transient response and locking process

9 experiments with different couples (K_p, K_i)

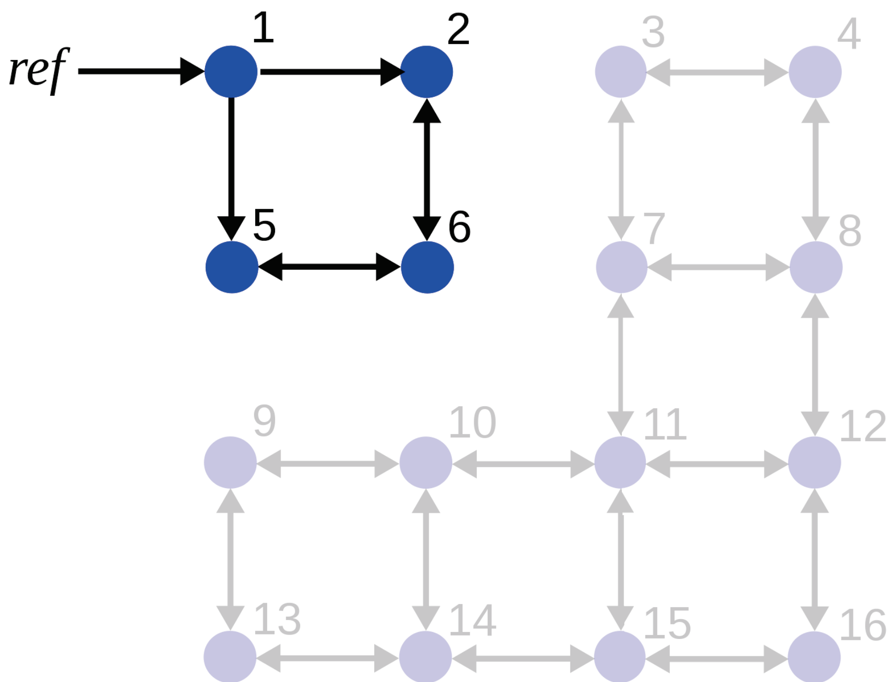
$$Kp \in \{0.9\,Kp_0, Kp_0, 1.1\,Kp_0\}, Ki \in \{0.9\,Ki_0, Ki_0, 1.1\,Ki_0\}$$



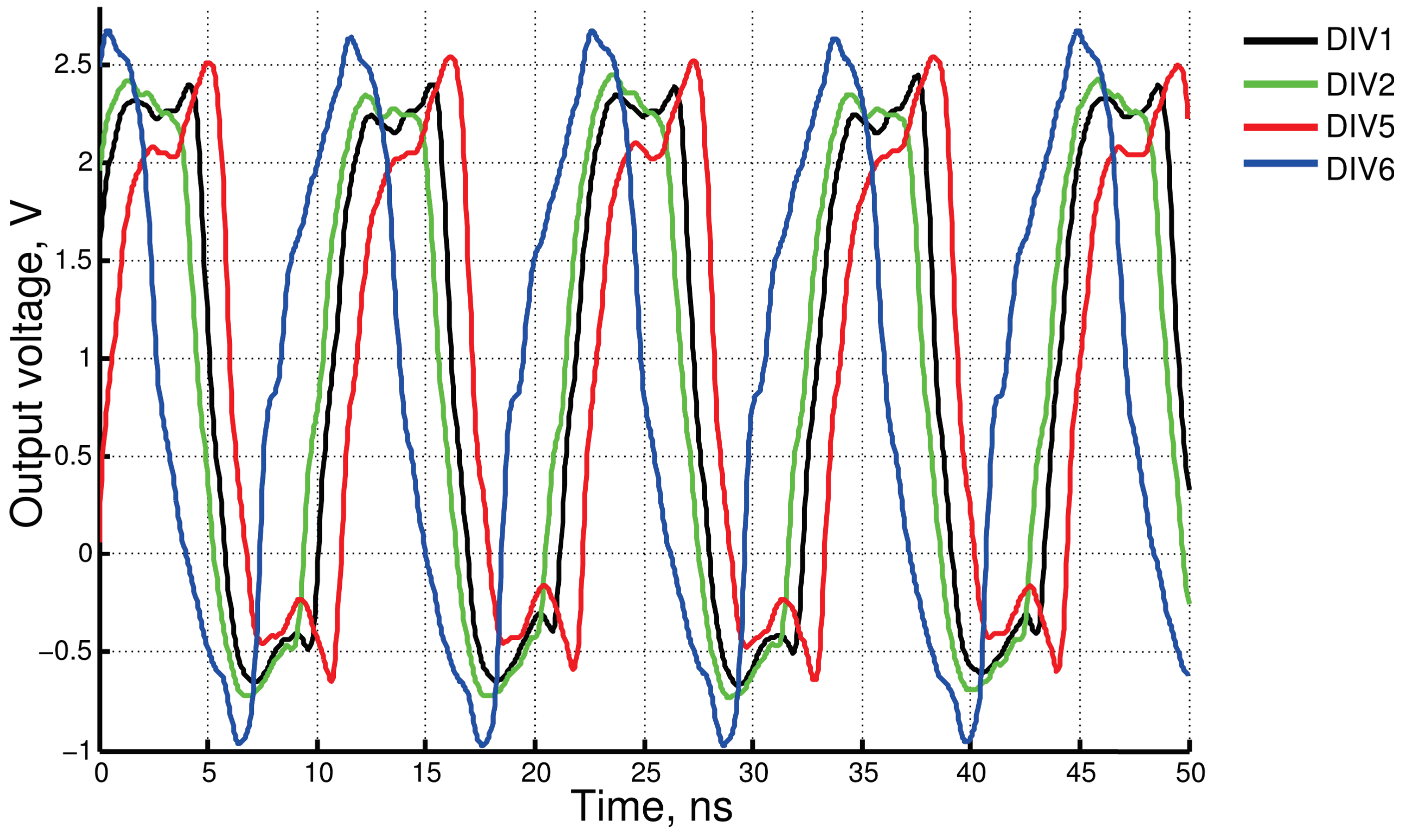
Weak impact on the transient reponse → robustness

Experimental results: mode-lock study

- For 500 start-ups of the network in a full 4x4 configuration we have not observed mode-locks
- We have studied mode-locks in a reduced configuration 2x2, where mode-lock can appear with a high probability
- This experiment was possible thanks to the reconfiguration features of the developed network



Experimental results: synchronization in undesired mode



- Reference frequency 180 MHz
- Mode-lock exists and it is stable

Chip prototype summary and comparison

Parameter	[Gutnik2000]	This work
Central frequency of SCA	1200 MHz	870 MHz
Frequency range	1100~1300 MHz	550~1190 MHz
Timing error	30 ps	60 ps
Convergence rate	≈ 10 MHz/μs	≈ 5 MHz/μs
Power consumption	390 mW @ F_{clk} = 1200 MHz	186.2 mW @ F_{clk} = 800 MHz
Chip area	~ $9mm^2$	~ $2.04mm^2$
Nature	analog	digital
Technology	350 nm	65 nm

Advantage of our work: reconfigurability and compatibility with digital environment

[GUTNIK2000] V. Gutnik and A. Chandrakasan "Active GHz clock network using distributed PLLs", ISSCC 2000

Conclusion

- First successful realization in silicon of ADPLL network for synchronous clocking

- Multioscillator system is reliable

- The designed system has been modeled at several levels of abstraction

- The test prototype of the distributed clocking network has been fabricated, successfully tested and characterized

- Maximum timing error between neighboring clock areas was measured to be less than 60 ps