Millimeter-wave UWB architecture for wireless sensor networks

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Ohana means family.
Family means nobody gets left behind, or forgotten.

— Lilo & Stitch

Dedicated to my Mother, Anna Maria.

A Special thanks to my only true big Love

and future wife Rosa.

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ABSTRACT

Exploiting wireless communications has had an unstoppable growth in the last years. In this attracting scenario, the Ultra Wide Band (UWB) market represents one of the main interesting targets for semiconductor industry. The availability of newer and larger bandwidth in the frequency spectrum (60 GHz and 77 GHz) opens to the possibility of higher bitrates communications.

The technology cost reduction is made possible by the use of silicon as semiconductor substrate in the place of classical heterojunction materials. The rapid reduction of the technological node (seen as the thinning of the gate channel) in the new generation of CMOS transistors allows obtaining faster transistors that become usable on V band applications. Therefore, the digital origin of the technology yields two additional advantages. First of all, the facilities for the circuits' production already exist as well as the recipe to create the devices on the substrate. The only additive cost remains the characterization of the technology at mm-wave frequencies. The second fundamental advantage is the possibility to have a complete integration of the system in the same dies with a substantial reduction of packaging and interconnection costs.

The objectives of this thesis is the design and the modeling of a complete 60 GHz UWB transceiver starting from the characterization and the optimization of the single subcomponents.

The main feature that constitutes the principal constraint of the entire work of this thesis is the high efficiency required for the transceiver front – end. The energy safe capability, in fact, represents the strength point of this project, being the system conceived for wireless sensors network applications.

Passive components as inductors and RF lines, have been the first elements that have been designed and characterized. Then the structure of CMOS transistor have been analyzed and characterized in order to obtain performances as higher as possible, in particular for wide transistors.

The knowledge acquired during this first part has allowed the developed of high quality factor inductors and high performance transistors (used in the design of upconversion mixer). In addition, the optimum correspondence between simulations and measurements combined with the gained experience on the RF electromagnetic simulations have been exploited to create a series of innovative (when possible) passive structures as baluns, power splitters and power couplers.

The second significant part of this work has been consecrated to the modeling of a series of high performance active circuits in the transmitter and the receiver blocks (upconversion mixer, voltage controlled oscillator ad a series of differential and single-ended buffers). The behavior of these structures has been accurately in-

vestigated and optimized in order to be later efficiently integrated in the complete transceiver system.

The systems are finally integrated in two different dies, transmitter and receiver blocks, and the 60 GHz link has been yield by a demostrator set-up.

PUBLICATIONS

During the course of the PhD, some publications have been produced which are based on the works presented in this thesis. They are listed here for reference:

[1] M. Ercoli, M. Kraemer, D. Dragomirescu, and R. Plana. "A passive mixer for 60 GHz applications in cmos 65nm technology". Proceedings of German Microwave Conference, pages 20 -23, march 2010.
[2] M. Kraemer, M. Ercoli, D. Dragomirescu, and R. Plana. "A wideband single-balanced down-mixer for the 60 GHz band in 65 nm cmos." Proceedings of Asia Pacific Microwave Conference (APMC), pages 1849 -1852, dec. 2010.
[3]M. Ercoli, M. Kraemer, D. Dragomirescu, and R. Plana. "A high performance integrated balun for 60 GHz application in 65nm cmos technology". Proceedings of Asia Pacific Microwave Conference (APMC), pages 1845 -1848, dec. 2010.
[4]M. Ercoli, M. Kraemer, D. Dragomirescu, and R. Plana. "An ultra small passive balun for 60 GHz applications in cmos 65nm technology." Proceedings of 8th IEEE International NEWCAS Conference (NEWCAS), 2010, pages 329 -332, june 2010.
[5]M. Ercoli, D. Dragomirescu, and R. Plana. "Small size high isolation wilkinson power splitter for 60 GHz wireless sensor network applications." Proceedings of 11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF), pages 85 -88, jan. 2011.
[6] M. Ercoli, D. Dragomirescu, and R. Plana. "Low size high efficiency local oscillator signal driver system for 60 GHz applications in 65nm cmos technology." Proceedings of German Microwave Conference, 2012, pages 20 -23, march 2012.
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[11] M. M. Jatlaoui, D. Dragomirescu, M. Ercoli, M. Kraemer, S. Charlot, P. Pons, H. Aubert, and R. Plana. "Wireless communicating nodes at 60 GHz integrated

on flexible substrate for short-distance instrumentation in aeronautics and space." International Journal of Microwave and Wireless Technologies vol 4(1), pages 109–117, 2012.

CONTENTS

ACRONYMS

IL	Insertion Loss
RL	Return Loss
IF	Intermediate Frequency
RF	Radio Frequency
LO	Local Oscillator
BB	Base Band
CG	Conversion Gain
gm	Transconductance
DC	Direct Current
AC	Alternate Current
CMOS	Complementary Metal Oxide Semiconductor
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
nMOS	n-Well Metal Oxide Semiconductor
pMOS	p-Well Metal Oxide Semiconductor
SSB	Single Side Band
DSB	Double Side Band
L	Attenuation
IP_3	Third order Intercept Point
DK	Design Kit
WLAN	Wireless Local Area Network
AM	Amplitude Modulation

FM Frequency Modulation

SHMS Structure Health Monitoring System

LOS Line Of Sight

NLOS Not Line Of Sight

NRP Normalized Received Power

SNR Signal to Noise Ratio

MAC Medium Access Control

PHY physical

IR-UWB Impulse Radio UltraWide Band

UWB UltraWide Band

MMIC Monolithic Microwave Integrated Circuit

ADC Analog-to-Digital Converter

DAC Digital-to-Analog Converter

LNA Low Noise Amplifier

VCO Voltage Controlled Oscillator

VGA Variable Gain Amplifier

RFIC Radio Frequency Integrated Circuit

SRF Self Resonance Frequency

DRC Design Rules Check

PSP Periodic S-Parameters

FTR Frequency Tuning Ratio

CMRR Common Mode Rejection Ratio

OCP Output Compression Point

OFDM Orthogonal Frequency Division Multiplexing

INTRODUCTION

1 INTRODUCTION

Starting by the first wireless transatlantic radio wave transmission accomplished by Guglielmo Marconi in 1901, the wireless communications have undergone tremendous growth. They were first used mainly by military (during the I and II world war) and later quickly expanded into commercial use such as commercial broadcasting services (shortwave Amplitude Modulation (AM) and Frequency Modulation (FM) radio, terrestrial TV), cellular telephony, global positioning service (GPS), wireless local area network (WLAN), and wireless personal area network (WPAN) technologies. Today, these wireless communications systems have become an integral part of daily life and continue to evolve in providing better quality and user experience. One of the recent emerging wireless technologies is millimeter-wave (mm-wave) technology. It is important to note that mm-wave technology has been known for many decades, but has mainly been deployed for military applications. Over the past 5–6 years, advances in process technologies and low cost integration solutions have made mm-wave a technology to watch and begun to attract a great deal of interest from academia, industry and standardization bodies. In very broad terms, mm-wave technology is concerned with that part of the electromagnetic spectrum between 30 and 300 GHz, corresponding to wavelengths from 10mm to 1mm. In this thesis, the work it will focus specifically on unlicensed 60 GHz band which enables many new applications that are difficult if not impossible to offer by wireless systems at lower frequencies.

1.1 APPLICATIONS

For dense local communications, the 60 GHz band is of special interest because of the specific attenuation characteristic due to atmospheric oxygen of 10–15 dB/km. Figure 1 shows the spectrum in whole of 60 GHz band at different atmospheric altitude. The 10–15 dB/km regime near the ground makes the 60 GHz band unsuitable for long-range (> 2 km) communications, so it can be dedicated entirely to the short range (< 1 km) communications. For the small distances to be bridged in an indoor environment (<50 m) the 10–15 dB/km attenuation has no significant impact. This makes the 60 GHz band of utmost interest for all kinds of short-range wireless communications. With an allocated bandwidth up to 7 GHz in most countries (as Figure 7 shows), the 60 GHz radio has become the technology enabler for many gigabit transmission applications that are technically constrained at lower frequencies (2.4 - 5.8 GHz).

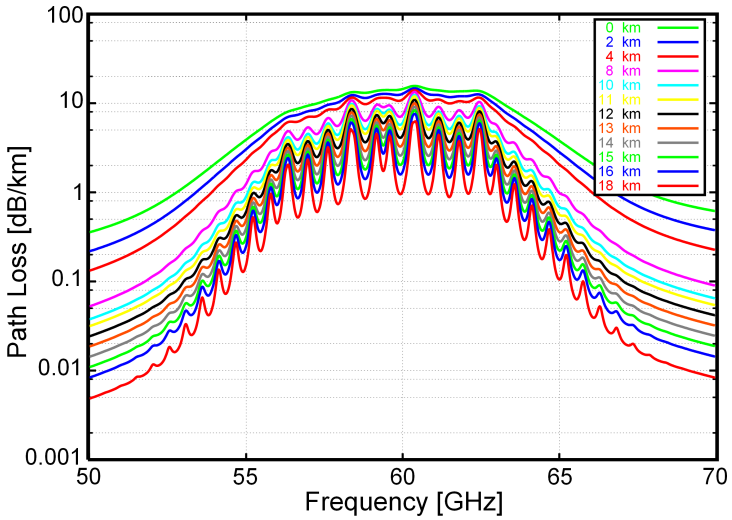

Figure 1: Insertion loss for 60 GHz band [12]

The large variety of possible applications have to assure that the wireless infrastructures should support real-time traffic with largely varying delay constraints as well as non-real-time traffic with different reliability requirements.

Flexible network solutions are required to accommodate the large number of communicating devices. In particular, the flexibility requirement is prominent in ad hoc network architectures that have multi-hop capabilities with many different operators in the same areas. Furthermore, in many applications, information integrity plays a vital part and thus should be well secured. The significance of all this is that next to the network capacity required to accommodate the actual application, there is much additional transfer capacity needed for quality of service provisioning and key features such as dynamic resource allocation and routing and security protocols for data integrity and protection against unauthorized access. Finally upon to these constraints the price of the system requires low-cost technology in order to assure the mass production of these new devices.

In the following 2 sub-paragraphs a distinction between two groups of potential application in 60 GHz band it will be performed. In the first, large retailer market applications will be discussed. Instead in the second one the niche industrial applications will be analyzed.

1.1.1 *Large retailers market applications*

Among the different products proposed for this slice of market it is possible to find different categories of products. Most of them do not need a very ultra wide band to work but thank to the others features of 60 GHz systems (such as extremely high dimension scaling, short distance communication, and high

integration capability) they find wide applicability in systems based on the 60 GHz band.

A large number of indoor applications are envisioned, such as:

- Cable replacement for uncompressed high definition (HD) video streaming that enables users to wirelessly display content to a remote screen with wired equivalent quality/experience;
- "Synch and go" file transfer that enables gigabytes of file transfer in a few seconds;
- Wireless docking stations that allow multiple peripherals (including an external monitor) to be connected without the need for frequent plugging and unplugging;
- Wireless gigabit Ethernet that permits bidirectional multi-gigabit Ethernet traffic;
- Wireless gaming that ensures high-quality performance and low latency for exceptional user experience;
- Domotic application like remote control (TV, ligting,door/windows lock), wireless burglar alarm (wireless windows/doors sensors), wireless connection between domestics appliances and internet (remote control of oven, washing machine, home heating systems or also the check of freezer content) etc. . . ;
- Wireless ad hoc communications i.e. notebook to notebook, notebook to printer, notebook to camera, camera to printer, notebook to TV, tablet to camera, camera to TV etc. . . ;
- Wireless surveillance cameras (baby videophones or home security video surveillance);
- Wireless digital entertainment on board of Aircrafts, cars, trains and allo other type of vehicles.

The previous list is principally oriented to the digital entertainment and the domestic purposes. Figure 2 proposes a possible scenario for future 60 GHz application in domestic environments.

On the other hands 60 GHz can supply also to professional and services environment, such as:

- Wireless LAN bridges to interconnect GigaEternet LANs between adjacent buildings;
- Wireless High quality videoconference, and interactive design;
- Wireless internet download of lengthy files;

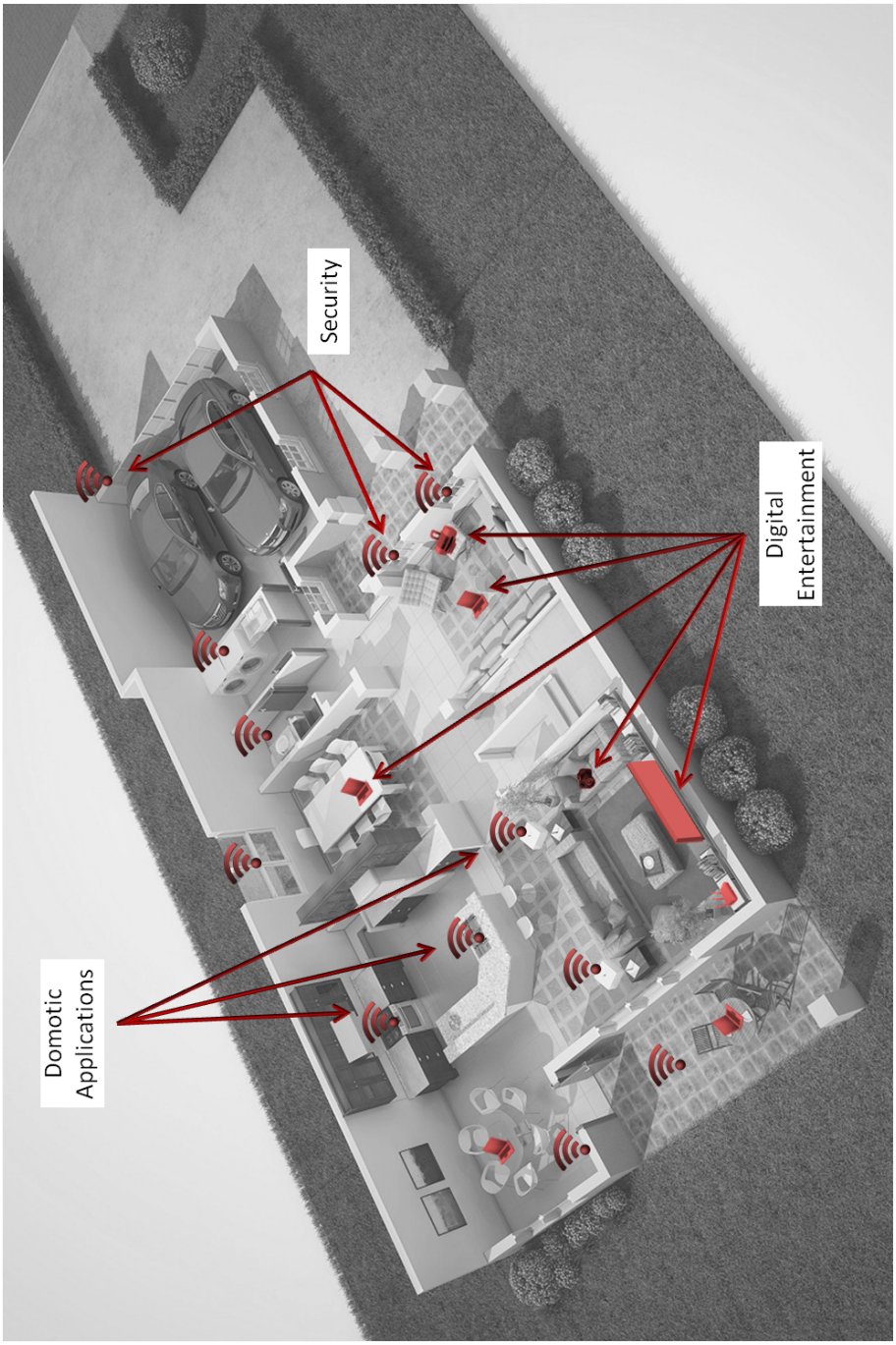

Figure 2: Different types of 60 GHz applications in a domestic enviroment.

- Wireless billing (highways, petrol station) from car to station.
- Wireless embedded systems (sensors in a cars);
- Hospital applications:
  - Patient status;
  - Patient position inside the structure;
  - Rapid access to collected data (such as, X ray, or others exams results');
  - Real time data, such as blood pressure ECG brain's activities, etc...

As example of the advantage given by the 60 band, the uncompressed video streaming is one of the most attractive applications. Related products, based on the WirelessHD specification, are already available on the market from companies such as Panasonic, LG Electronics and Toshiba . Depending on the progressive scan resolution and number of pixels per line, the data rate required varies from several hundred Mbps to a few Gbps. The latest commercially available high-definition television (HDTV) resolution is 1920 × 1080, with a refresh rate of 60 Hz. Considering RGB video formats with 8 bits per channel per pixel. The required data rate turns out to be approximately 3 Gbps, which is currently supported by the HDMI 1.1 specification. In the future, higher numbers of bits per channel (10 and 12 bits per color) as well as higher refresh rates (90 Hz, 120 Hz) are expected to improve the quality of next-generation HDTV. This easily scales the data rate to well beyond 5Gbps.

1.1.2 *Niche market: high technologies industrial applications*

Interesting applications in industrial contest are the dense wireless sensor networks: hundreds or thousands of different sensors could be placed in a restricted environment, acquire different parameters and transmit them with a highest data rate.

The exploitation of the 60 GHz band for these applications is it is advantageous to the reliability of the system. As know 60 GHz band it offers a very wide unlicensed frequency bandwidth and a relatively high power level per MHz compared to the other UltraWide Band (UWB) standards in the 2.4-5.8 GHz bands. Moreover, thanks to the strong electromagnetic field absorption done by the oxygen, different areas relatively close can use the same band with negligible interferences.

The wireless sensor network applications were the starting point for the development of this thesis work. Company as Airbus, TAS (Thales-Alenia Space) and EADS were strongly interested to the feasibility of this **WSN!** (WSN!) system based on 60 GHz band. In fact, in the industrial market the 60 GHz systems can contribute in different way to the development of a product.

Focusing the interest into the aeronautic-space field WSNs could supports several phases of product creation.

During the design phase, wireless sensors could be inserted into the scale model to evaluate the behavior of the wind around the wings or along the fuselage. Classical approaches are to cover the wings and fuselage of reduced scale models with mini-tufts or even with clay to highlight the pattern characteristic of the air flow. Figure 3 shows images to the Airbus A380 plane in the National Centre for Aeropsace Research (ONERA) [13] and the technique used in the Kirsten Wind Tunnel http://www.uwal.org/uwalinfo/techguide.htm (University of Washington Aeronautical Laboratory) to study the air flows around the plane. In the future, thanks to the high scale reduction of the 60 GHz transceiver it will be possible to replace these methods with specific sensors attached along the fuselage. The data acquisition, therefore, it will be possible by a radio base station placed out of the wind tunnel using the UWB 60 GHz protocol. This new method of data acquirement helps to increase the reliability of data assuring real time evaluation of the phenomena around the model as well as the total time dedicated to accomplish this phase of the design.

The 60 GHz wireless sensor networks will also be an integral part of the testing phase of the aircraft prototype. In the actual design procedure, several test flight are scheduled during the final phase of aircraft design. Figure 4 shows the equipments used to acquire all of possible data coming from wired sensor into the plane. Enormous quantities of cables are required to interconnect these sensors. Unfortunately this set-up poses several problems because it influences the real condition of flight. The weight of the cables inside of the wings, for instance, changes their balancing and consequently they add some incertitude on the acquired measurements. On the other hand, using wireless sensors networks the weight of the monitoring structure is strongly reduced and the number of possible sensors could be strongly increased. As a consequence the quality of measurement will be improved as well as the reliability of the aircraft.

At the conclusion of prototype test, 60 GHz WSNs are still of use because they can be exploited during the normal monitoring of the health status of the aircraft. The structure health monitoring systems (SHMSs), in fact, have in the last years assumed a primary role in the maintenance of the aircrafts. The automatic controls of the health status of the primary structures reduce the times of maintenance services and in several circumstances it can also delay the maintenance time scheduling. In case of “hard landing” events, instead, the Structure Health Monitoring System (SHMS) will advise the pilots and the ground crew of possible damages to the aircraft structure and then anticipate the technical inspections if necessary. Therefore the insertion of WSNs based on 60 GHz band could firstly reduce the time design of the aircraft and in the follow it could drastically reduce the number of human interventions during the lifetime of the airplane. In terms of costs this new strategy will safe million of Euro and improve at the same time the reliability of the new era of aircraft. Figure 5 shows

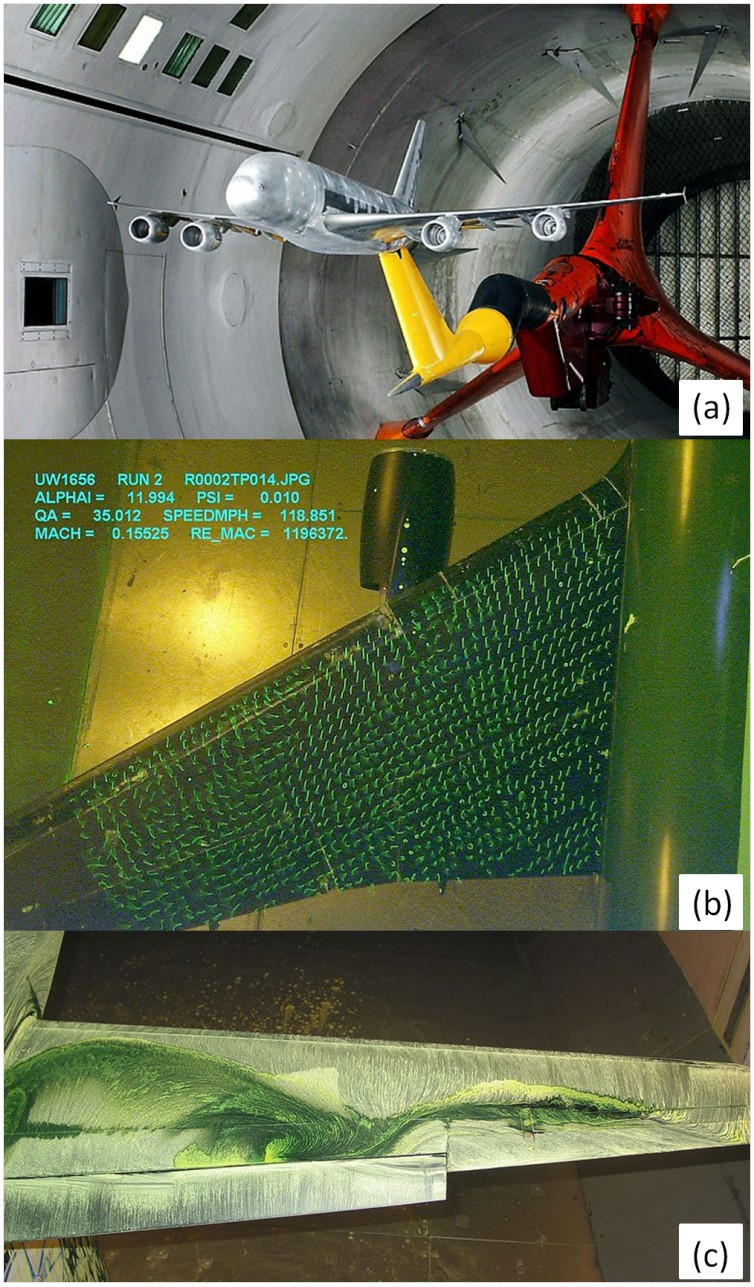

Figure 3: Classic methods to study fluid-dynamics of wind. (a) Wind tunnel of Onera [13] (b) mini-tufts technique, and (c) China clay technique **(author?)** [14] .

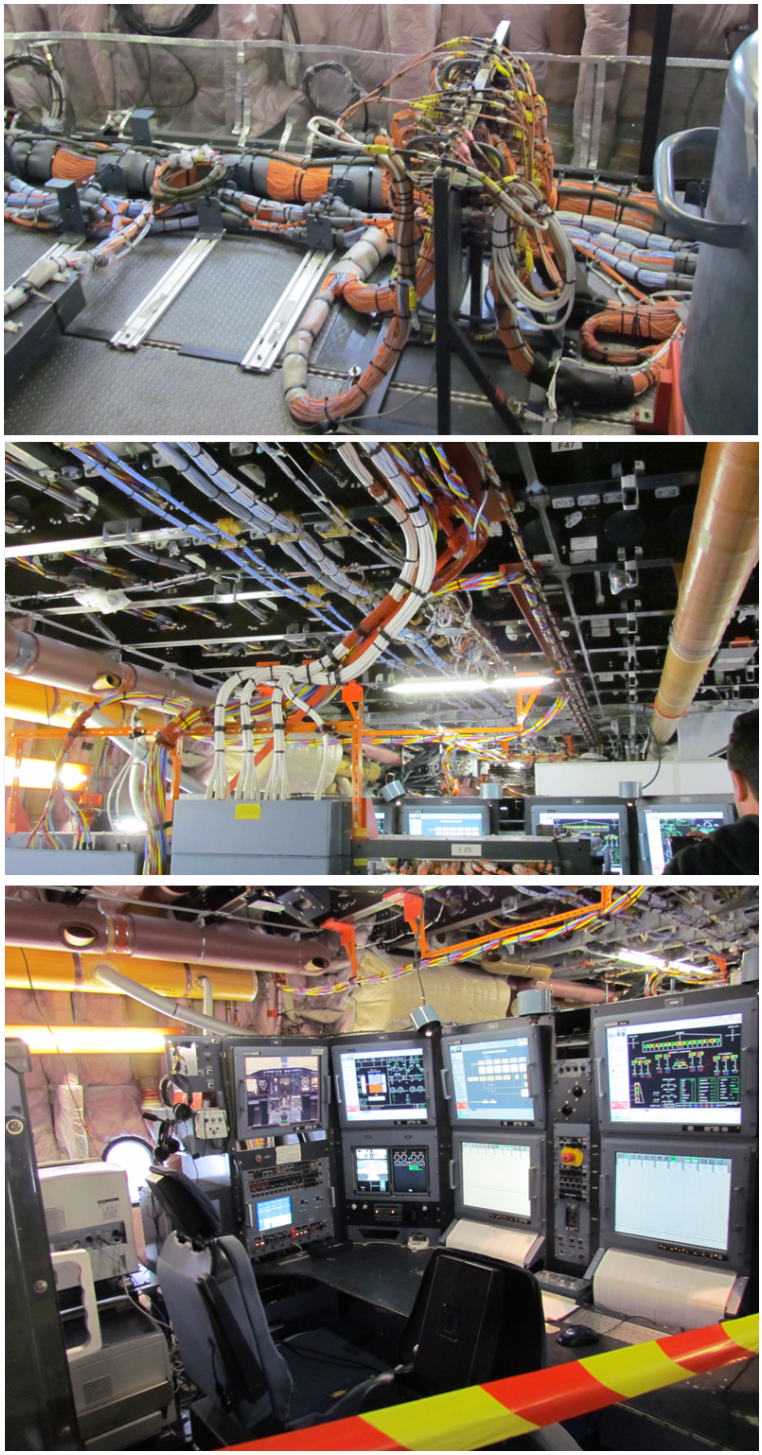

Figure 4: Equipments used to monitoring the Airbus A380 aircraft during test flights.
http://www.flickr.com/photos/spacemike/6173378635/in/photostream/

quantitatively the possible placement of the WSNs on the new A350 of Airbus Industries.

1.2 60 GHz link performances

At 60 GHz there is much more free space loss than at classical wireless link (2.4 or 5 GHz) since free space loss increases quadratically with frequency. In principle this higher free space loss can be compensated for by the use of antennas with more pattern directivity while maintaining small antenna dimensions. When such antennas are used, however, antenna obstruction (e.g., by a human body) and issue of antenna pointing may easily cause a substantial drop of received power, which may nullify the gain provided by the antennas. This effect is typical for millimeter waves because the diffraction of millimeter waves (i.e., the ability to bend around edges of obstacles) is weaker. Regarding blocking effects, omnidirectional antennas have an advantage in a reflective (e.g., indoor) environment since there they have the ability to still collect contributions of reflected power in the event of line of sight (LOS) obstruction. Walls, however, may considerably attenuate millimeter waves. The electromagnetc wave transmission strongly depends on material properties and thickness. At 60 GHz, the feature of glass transmissivity may range from 3 to 7 dB, whereas transmission through a 15 cm thick concrete wall can be as high as 36 dB [15]. With these attenuation values, therefore it is expected that concrete floors between stocks of a building to act as reliable cell boundaries. This could be represents an advantage for the 60 GHz transmission because it helps to create small indoor cells for hot spot communications. However, a typical/moderate inner wall consisting of multiple partitions of different materials: wood (for doors and windows) concrete, bricks, thermal and sound insulating materials and in particular circumstances it may be considered neither a reliable cell boundary nor a transparent medium. Therefore, due to the possible significant attenuation of inner walls, it will generally be necessary to have at least one access point per indoor environment (room, hall, corridor, etc.) to create a reliable shared medium. From a coverage point of view the best place for the access point antenna would be somewhere nears the center of the room at a high position near the ceiling. Another attractive option would be the possibility to place a small access point in each room, with its small antenna(s) mounted on a wall where it can readily be connected to the existing LAN cabling already installed or also, for very high speed data transfer (several Gb/s) an opportune optic network that relies all rooms/office of the building. In order to allow flexible terminal use, the low position of the access point (antenna) necessitates measures to cope with the drop in received power due to Line Of Sight (LOS) obstruction by a person or object. One measure is to apply macro diversity by switching to another access point as soon as the received signal drops below a certain threshold. A more attractive solution may be found in another direction, namely that of applying particular antenna patterns that may be adaptive to some extent (e.g., by applying

Figure 5: WSNs for SHMSs and digital entertainment on the future Airbus A350

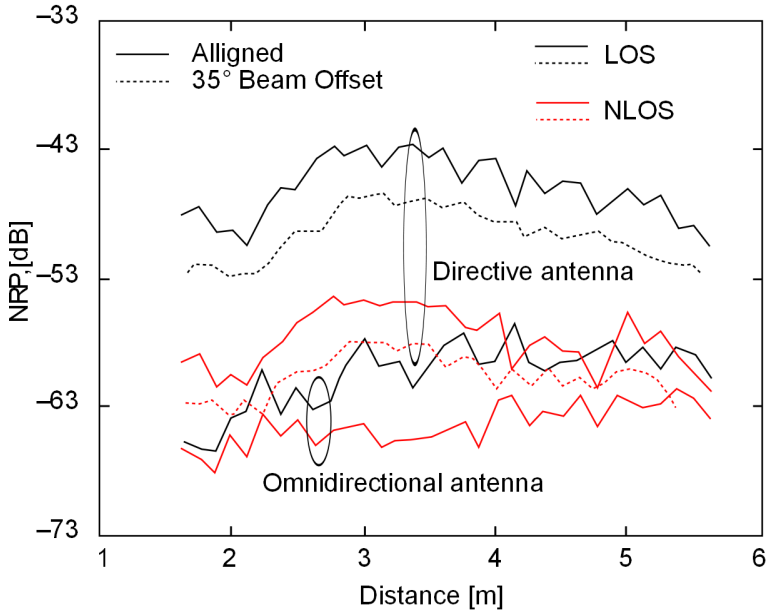

Figure 6: Normalized received power (NRP) for 60 GHz indoor transmission [16].

beam switching). Low or medium gain antennas may be preferred to high gain antennas in order to avoid stringent antenna pointing and tracking requirements. Experimental work on 60 GHz antenna pattern optimization has been carried out in [16]. Measurements have been conducted in many indoor environments. Figure 6 shows the normalized received power (NRP) in dB measured in the 58–59 GHz band as function of the separation distance between transmitter and receiver [16].

The employed antenna has an antenna gain of 16.5 dBi and produces a fan beam that is wide in azimuth and narrow in elevation. The same type of antenna was applied at the receiving station, which was positioned at various places in the room. The upper solid curve in Figure 6 shows the NRP when the beam of the receiving antenna is pointing exactly toward the transmitting antenna. The dotted curve, instead, represents the situation in which the fan beam at the receiver has an azimuth pointing deviation of 35°. The lower solid curve represents the situation in which the fan beam antenna at the receiver is replaced by an antenna that has an antenna gain of 6.5 dBi and radiates omnidirectionally in the horizontal plane.

The curvature of both solid Normalized Received Power (NRP) curves is typical of indoor situations in which antenna patterns are not well pointed toward each other at short distances. In that area, the NRP increases with distance. This is because the increased free space loss is more than compensated for by antenna gain since the antennas are better directed toward each other. If the separation distance is increased further, these curves tend to become higher than the free-space curves because the reflections from walls and so on contribute effectively to the received power. The dotted curve remains lower because of the fixed

35° antenna mispointing at all distances. In case of Not Line Of Sight (NLOS) condition on applying the fan beam antenna the average drop of NRP due to LOS path obstruction is about 11 dB for 0° as well as 35° pointing deviation. With the omnidirectional antenna instead, this drop is reduced to only 4 dB. The lower losses in the case of omnidirectional receiver antenna is attributable to the capability of the antenna to combine reflected power coming from different direction to the principal source of power covered by the undesired obstacle.

The results in Figure 6 are representative for other indoor environments in the sense that the free-space law can be considered a reliable lower bound of NRP at relatively large distances. Hence, we can estimate the feasible link performance on the basis of the free space loss. If considering for instance the described antenna setup in a larger room. The transmitted power is 7 dBm (5 mW), which is well feasible with today's 60 GHz CMOS amplifiers [17] operating in their linear region. According to the Friis formula:

$$P_r = P_t + G_t + G_r + 20\log\left(\frac{\lambda}{2\pi R}\right), \tag{1.1}$$

the received power is –58 dBm with a distance R of 2.5 meters.

If only thermal noise is encountered, the noise power at the receiver is:

$$P_N = 10\log(kTBF) \tag{1.2}$$

with k is Boltzmann's constant ($1.38e^{-23}$ J/K), T is equivalent noise temperature of the receiver and the room temperature is 290° K. B is noise bandwidth, and F is receiver noise figure. With a receiver noise figure of 10 dB and a noise bandwidth of 1 GHz the received noise power amounts to −74 dBm. This yields a signal-to-noise ratio (SNR) of 16 dB. For sufficient performance in terms of bit error ratio ($< 10^{-6}$) an Signal to Noise Ratio (SNR) of about 10 dB is required. This implies that 6 dB of margin is left to cope with shadowing and performance degrading factors occurring in the transceiver such as phase noise and frequency shift.

For the issue in the phase noise, it depends on the performance of the integrated oscillator exploited in the transceiver system. This value can be established and weighted in the link budget estimation on the base of the particular oscillator implementations. Sources of frequency shift, instead, are not correlated with the transceiver architecture but they depend on the environment where the system is exploited. Movements of the portable station as well as movements of objects in the environment cause Doppler effects as frequency shift and spectrum broadening of the received signal. These Doppler effects are relatively severe at 60 GHz because they are proportional with frequency. If persons move at a speed of 1.5 m/s (walking speed), the Doppler spread that results at 60 GHz is 1200 Hz [15].

A rigorous link budget calculus (taking into account all possible contributes)) for 60 GHz transmissions is proposed in [18].The same estimation procedure is exploited in the last chapter of this thesis to estimate the transmission capability for the circuits realized and discussed in the two next chapters of this thesis.

1.3 STANDARDS AND REGULATION FOR 60 GHZ COMMUNICATIONS

The field of application described in the previous paragraphs is potentially enormous but, with a market oriented to the profits the cost reduction to an acceptable level is of primary concern for a successful take-up of 60 GHz wireless products. An essential prerequisite for low fabrication cost is that the required technology be produced in high volumes and with high yields and short turnaround times, short time to market, and quick return on investments. Consequently, there should be clear incentives for the semiconductor industry to invest in the new generation of ICs required. The clear incentive would be the promise of a mass market on top of an interesting niche. Therefore, a set of protocols should be developed and standardized, supporting not only typical WLAN configurations but a whole family, including ad hoc networking, remote access/wireless local loop (WLL), point-to-point, consumer business standards, and all kinds of low-cost, short-range communication between all kinds of appliances as discussed before. Thus, an extended family of configurations should be addressed covering the broadest possible range from low-speed, low-bandwidth, low-cost products to high-speed, high-bandwidth products that can be produced at reasonable cost. This section discusses the current status of worldwide regulation and standardization efforts for the 60 GHz band. The regulatory bodies in the United States, Japan, Canada and Australia have already set frequency bands and regulations for 60 GHz operation, while in Korea and Europe intense efforts are currently under way. Whatever, the bandwidth allowed for each area is already established and Figure 7 shows their spectral occupation. The narrower bandwidth is delivered in Australia with

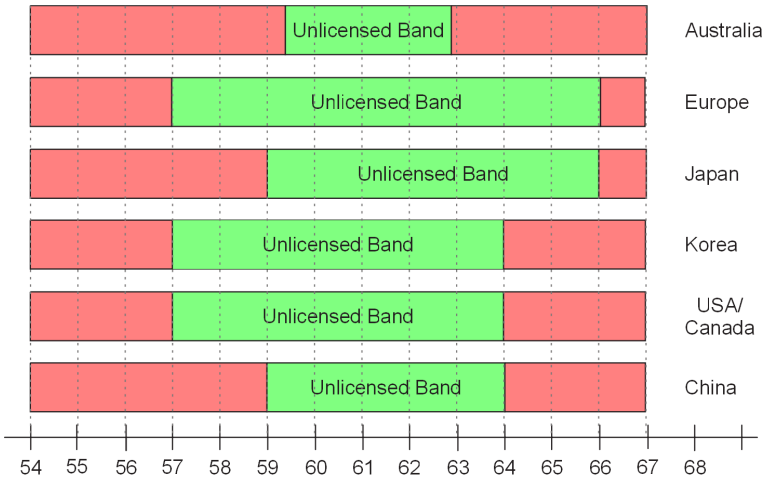

Figure 7: Worldwide frequency allocation for 60 GHz band

only 3.5 GHz of spectrum (59.4-62.9 GHz). On the other hand Europe has the wider spectrum with 9 GHz (57-66 GHz). In this band, 4 UWB channel can be placed, following the trasmit spectral mask proposed in [19]. Concerning the limits on transmit power, EIRP and antenna gain, Table 1 summarizes all of these

parameters. The transmit spectral mask for standard 60 GHz Channel is instead

Region	Unlicensed Bandwidth [GHz]	Transmit Power [mW]	EIRP [dBm]	Maximum antenna gain [dBi]
USA/Canada	57-64	500 max	40	33
Japan	59-66	10 max	58	47
Korea	57-64	10 max	27	17
Australia	59.4-62.9	10 max	51.7	41.8
Europe	57-66	20 max	57	30

Table 1: Frequency band plan, limits on transmit power, EIRP and maximum antenna gain.

represented in Figure 8.

Overview on the global standardization efforts

The first international industry standard that covers the 60 GHz band is the IEEE 802.16 standard for local and metropolitan area networks [20]. However, this is a licensed band and is used for line-of-sight (LOS) outdoor communications for last mile connectivity. In Japan, two standards related to the 60 GHz band were issued by Association of Radio Industries and Business (ARIB): the ARIB-STD T69 [21] and ARIB-STD T74 [22]. The former is the standard for mm-wave video transmission equipment for specified low-power radio stations (point-to-point systems), while the latter is the standard for mm-wave ultra high-speed WLANs for specified low power radio stations (point-to-multipoint systems). Both standards cover the 59–66 GHz band defined in Japan. Interest in 60 GHz radio continued to grow with the formation of multiple international mm-wave standards groups and industry alliances. In March 2005, the IEEE 802.15.3c Task Group was formed to develop a mm-wave based alternative physical layer (PHY) for the existing IEEE 802.15.3 WPAN standard [19]. In August 2006, ECMA TC-48 began an effort to standardize medium access control (Medium Access Control (MAC)) and **PHI!** (**PHI!**) layers for high-speed, short-range communications using the 60 GHz unlicensed frequency band for bulk data applications and for multimedia streaming applications [23]. In 2006, the formation of the WirelessHD consortium was announced with a number of key consumer electronics companies to deliver a specification for high-speed, high-quality uncompressed audio/video (A/V) streaming using 60 GHz technology `http://www.wirelesshd.org/`. In the latest development, the Wireless Gigabit Alliance (WiGig) was formed in May 2009 to establish a unified specification for 60 GHz wireless technology in order

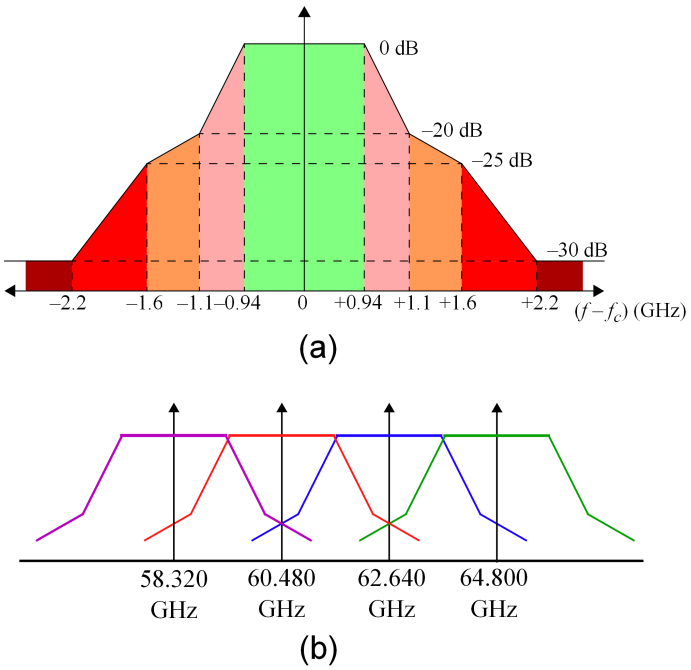

Figure 8: Transmit spectral mask (a) and band allocation in 60 GHz European bandwidth (b).

to create a truly global ecosystem of interoperable products for a diverse range of applications http://wirelessgigabitalliance.org .

1.4 TECHNOLOGIES USED FOR 60 GHZ CIRCUITS

Considering the scenario discussed above, the 60 GHz band represents for the high-tech industries a market with an enormous potential. In order to maximize the profits, however, the wireless system on which will be based communication protocol must be as cheaper as possible. Until few years ago, only the III-V technologies (such as GaAs, AlGaAs, GaN, InP or SiC) allowed the necessary cut off frequency (fT) to work upon the 60 GHz band. These technologies mainly based on Monolithic Microwave Integrated Circuit (MMIC) circuits suffer of two main weak points;

- The power consumption of these circuits can reach considerable values;
- III-V materials are quite expensive.

Concerning the first point, the power hungry feature shown by most of these circuits could represent a problem for several low power applications previously proposed (battery driven applications). In addition, the total price of the product could be considerable increased by the cost of the MMIC component, in particular for application in which great volume of Radio Frequency (RF) transceiver are

employed (such as dense WSN applications for SHMSs). Considering this type of scenario many of the previously proposed applications would not even be considered by the industries due to excessive development costs and limited profit margins. Fortunately, in aid of the low cost applications, comes the most economic silicon based technology. In fact, the improvement on the silicon base circuits, during in the past years, place the CMOS technologies among the best candidates to fill the shortage of III-V materials. The reduction of channel length (180/130 µm in 1995 - 65/42 µm in 2012), as Figure 9 shows, has pushed up the fT of several GHz allowing the use of CMOS transistors for 60 GHz applications.

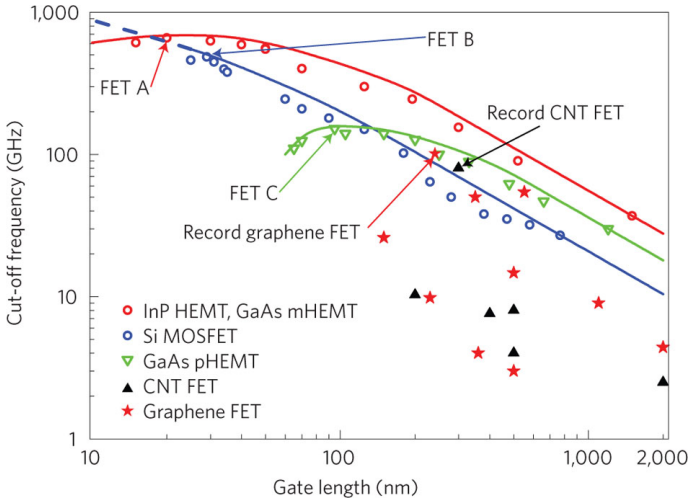

Figure 9: Channel lenght reduction for CMOS family in the last 30 years and previsions until 2020. [24]

The exploitation of CMOS in analog 60 GHz transmissions reduces the technology production costs for two reasons:

- CMOS substrates is cheaper compared to III-V families of devices;
- Analog CMOS process is directly derivate from the digital CMOS one with clear advantages in the development costs.

A crucial feature of the CMOS technology derives directly by the second reason, i.e. the silicon based circuits can integrate the analog and digital part in the same chip. This feature constitutes an enormous advantage for the 60 GHz wireless system. The integration of the two blocks within the same substrate reduces the delay of communication between the chips, increases the compactness of the total system and so avoids any type of external support to interconnect the analog and digital part (no PCB cards or other substrate are needed).

Concerning the power consumption, the CMOS technology offers incomparable performances if it is compared to the other family of devices. The relatively low electron mobility (µ) in p-doped silicon, compared to the 2D electron gas mobility of heterojunction (2-DEG) imposes several geometric countermeasures on the

layout of CMOS transistor. Among that, channel length and oxide thickness in the gate contact are the most sensible one. The higher mobility in III-V materials allows yielding transistors with longer channels (L) and thicker oxide in correspondence of the gate pin. Quantum phenomena as the tunnel effect or breakdowns of the gate oxide are then less probable in concomitance of high drain-source voltages. In short channels transistors, instead, the maximum drain-source voltage must be strongly reduced in order to avoid malfunction or worse breaking of the devices. For these reasons CMOS transistors with channel lengths lower than 100 nm are biased with voltages of 1.2 V or lower (1 V for 65 nm tech.).

The "energy safe" nature of the sub-micrometer transistors can be seen as great advantage for all of purposes that require very low power consumption or a considerable lifetime (such as the WSN applications). However the very low power supply of the short channel CMOS could represents an issue when power RF stages have to be designed. As said, for 65 nm and other high scaled technologies the power supply drops lower than 1 Volt. Therefore, to generate RF power, in order to assure the reliability of the wireless link, the power stages of the RF transceiver must drive high quantity of currents and several issues arise.

The work described in this manuscript exploits the energy safe features of the ST Microelectronics 65 nm CMOS bulk technology under all possible points of view and, in the final part of the manuscript the problem of the RF power generation is discussed and a possible solution (not completely implemented due to time and costs limitation) is proposed.

1.5 HIGH – LEVEL ARCHITECTURE OF THE TRANSCEIVER

The final version of the 60 GHz transceiver it would have been made by a single silicon chip which includes both the analogue and digital parts. The black box representation of this chip is described in Figure 10.

The coexistence of analog and digital part allows obtaining a decisive improvement of the size reduction of the chip. The schematic block shown in Figure 10 considers a general purpose system capable to interact with at least 2 interfaces: the first interface with the sensor, to acquire data and, the second one with an elaboration unit such as: CPU, DSP or ASIC. In terms of functionality, in the considered scheme there are 4 functional areas:

- Digital MAC and PHY layers part;
- Analog to Digital (Analog-to-Digital Converter (ADC)) and Digital to Analog Digital-to-Analog Converter (DAC) conversion part;
- Transmitter and Receiver part;
- Phase shift a beam-forming network part.

In the framework of this thesis the third point is treated; receiver and transmitter chain are designed realized and characterized in two stand alone dies. The first

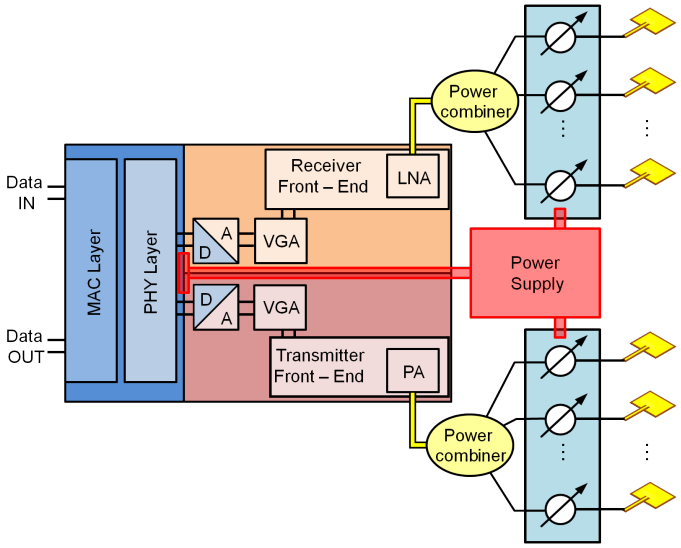

Figure 10: 60 GHz proposed system

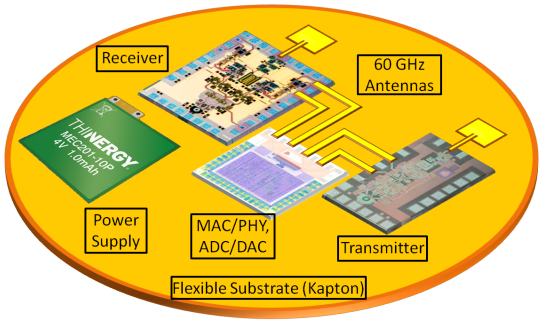

Figure 11: Single dies of 60 GHz system integrated in a flexible substrate

and the second point are developed by others members of our team [25, 26]. In this context also the coexistence of digital and analog part in the same silicon die is demonstrated by the integration of MAC and PHY layer with the ADC / DAC circuits. The three blocks are, therefore, ready for integration. At the moment of manuscript redaction a new project is ready to start and one of the objectives is the integration of the three dies on flexible substrate (kapton) [11]. Figure 11 shows the idea proposed in this new project.

Concerning the fourth and last point, time and limited resources have stopped the research on this field. At the end of the thesis, however, a simulation for the first part of beam-forming network will be shown and discussed.

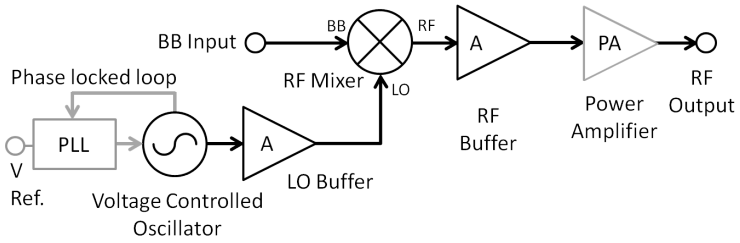

Figure 12: Transmitter chain

1.6 TRANSMITTER AND RECEIVER CHAIN

The heart of analog part, composed by the transmission and reception chain, has been developed using the direct conversion approach to translate the information in and from the 60 GHz band. The choice to use a single stage to yield the frequency translation is corroborated by the reduction of the power consumption required for the energy save systems as the WSNs. The homodyne approach therefore, reduces the complexity of the RF chain by the suppression of the intermediate frequency (Intermediate Frequency (IF)) filter and of all of other circuit required to generate the IF carrier. On the other hands, the homodyne circuits compared to the super-heterodyne systems suffer of some limitations. The direct up/down conversion of the signals requires 60 GHz signals to drive the mixer and the local oscillators that work upon this frequency band show some weakness points.

As example, the high phase noise of the generated carrier or also their reduced output power can represent a big issue comparing to the higher performances shown in 20/30 GHz oscillators employed in the double step frequency conversion transceivers. It important to underline, however, that these and the other possible issues as the 1/f noise generated in the downconversion process depend on the particular circuit topology. Therefore a redesign of the critical stages of the up/down conversion chain is required to overcome them. In following parts of this manuscript the several issue encountered during the circuit design will be handled and, innovative solutions (where possible) will be proposed and demonstrated.

1.6.1 *Transmitter front - end*

The transceiver chain, as Figure 12 shows, is composed by a direct up conversion mixer, a voltage controlled oscillator and buffers appropriately placed to increase the local oscillator power (in the VCO arm) and to partially recover the conversion loss of the mixer in concomitance of the RF output chain.

The design flow employed to conceive the transmitter of Figure 12 is based on the evaluation of the power levels of the signals flowing inside the blocks. The choice of the mixer topology together with the definition of the local oscillator

power level and the architecture and placement of the necessary buffers have been done to assure the higher as possible performances maintaining at the same time the lower as possible energy consumption.

The complete description of the design flows and all of realization details will be discussed on chapter 3 in the transmitter integration section.

1.6.2 *Receiver front - end*

A first receiver chain was already integrated, measured and, characterized during the Ph.D thesis Michael Kraemer [18]. The version of receiver proposed in these pages can be considered as the evolution of that circuit. The majority of the constitutive sub-blocks have been modified or completely redesigned in order to improve the RF matching properties or to increase their system integrability.

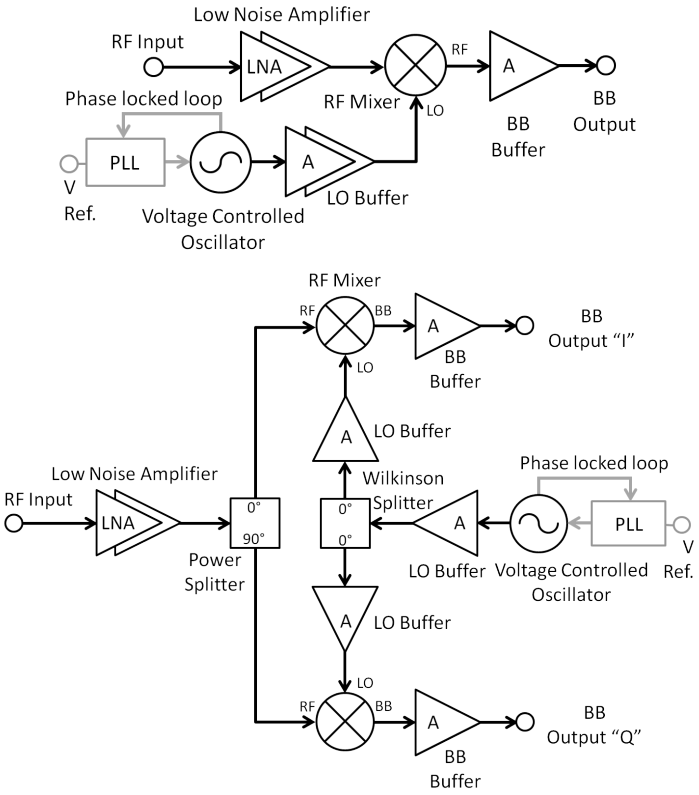

Figure 13: Single branch receiver chain [27] and I/Q receiver conceived in this thesis

Figure 13 describes the two versions of 60 GHz receivers in order to highlight what differences exist between the two receiver architectures. In the new receiver chain in – phase and quadrature (I/Q) demodulation is exploited. This has involved among the other things the complete redesign of the local oscillator source and the insertion of a 90° power splitter to recognize the I/Q signals at the output baseband.

1.7 ORGANIZATION OF THE MANUSCRIPT

In the following pages the research work accomplished during the three years of Ph.D will be discussed.

Chapter 2 talks about the synthesis, design and characterization of passive structures: the work on the lines and inductors, already introduced in [18] is expanded with the analysis of octagonal inductors and slow-wave lines. The chapter proceeds with the discussion of the passive structure as baluns, power splitters, and couplers developed by using the design methodologies acquired during the first part of the work.

Chapter 3 deal with active structures: mixers blocks, and buffers based on differential pairs. These are the main structures developed over the thesis lapse. Others structure as Low Noise Amplifier (LNA), power amplifier and Voltage Controlled Oscillator (VCO) are already developed during [18] and in this thesis they are modified, optimized or when necessary redesigned (as example the VCO) in order to comply with the required features.

Chapter 4 concerns the design of base band circuitry as variable gain amplifier (VGA). The main difference with the others circuits developed in this thesis is the exclusive use of resistors at the place of inductors in the amplifiers chains. The chapter talks about the strategy employed to extend the allowable band starting from Direct Current (DC) and rise up to 2.5 GHz. Two main categories of Variable Gain Amplifier (VGA) are treated: active and passive architecture for the control of the gain regulation.

Chapter 5 describes the integration process followed to obtain complete transmitter and receiver chain and it highlights the obtained performances.

Finally, on Chapter 6 are discussed the performances of the obtained 60 GHz radio connection. A demonstrator, using the designed circuits is presented in order to verify the reliability of the V band link. Three different case of study, based on three different chains set up are proposed with an estimation of the respective link budget. The performance of the system energy consumption is also discussed considering two different links (10 kbps and 100Mbps). The manuscript finishes with general conclusions on the accomplished work and on the obtained results and perspective works.

PASSIVE COMPONENT DESIGN

2

PASSIVE COMPONENT

INTRODUCTION

In complete millimeter-wave systems a fundamental role is attributed to passive components as baluns, power dividers, and different type of couplers. The impact that these components have on the complete system response is comparable with the function yielded by the active ones. The main aspects that characterize the passive structures are the occupied area, the insertion loss, and the bandwidth. The dimensions of a passive component (such as power splitters or hybrid couplers) depend on the wavelength of the involved signal. In Radio Frequency Integrated Circuit (RFIC), it is well known how the use of a branchline coupler or a Wilkinson power splitter requires many space. In a 65 nm CMOS bulk technology the effective electrical permittivity is around 3.89 and the wavelength (λ) of a 60 GHz signal corresponds to 2.44 mm. Consequently, the dimensions of a passive $\lambda/4$ component become huge compared to whichever active block. Furthermore, the CMOS bulk technology is characterized by a low resistivity substrate, and as a consequence the losses at high frequency become very high. In literature, there are many different solutions proposed and implemented for millimeter-wave passive components, and they show appreciable performances.

In the following of the chapter, classic components like different type of balun, hybrid coupler, and power splitter will be discussed and their critical aspects highlighted.

The chapter, however, starts with the characterization of lumped inductor components. This research has been started during the thesis of M. Kraemer [18] and here completed. In effect, the work on lumped inductors has permitted to establish with high precision the characteristics of the CMOS substrate and all type of interactions between the RF structures and the remaining part of the circuit. Thanks to this information it has been possible to expand the design of passive elements to high performances lines, balun, power splitter and couplers.

2.1 INDUCTORS

The design of inductive elements can be accomplished in two different approaches: lumped component structures, using spiral topologies, or distributed component, using lines and stubs. In 60 GHz circuits design both of the strategies are employed. In the power amplifiers field, for instance, a large number of teams prefer the employment of lines and stubs [28, 29] in the place of lumped component elements.

In the RFIC circuits the use of distributed structures is an extension of the common design strategy adopted in the MMIC technologies.

In MMIC the size of the circuits is normally comparable or even bigger than the wavelength of the treated signal. In the case of RFIC, instead, the circuits are many times smaller and the distributed elements could represent a waste of the silicon surface of the chips. Another design technique in RFIC circuits is to employ the slow wave methods to realize shorter inductive lines and thus reducing the total circuit area [30, 31].

The principle of functioning of the slow wave lines is very intresting and is based on a separation between the two electromagnetic component of the field: the electric field lines do not penetrate the semiconductor substrate, whereas the magnetic field fully penetrate it. This particular combination of ecffects allows obtaining high capacitance and high inductance lines, thus increasing the ε_r and hence the line delay [32]. As a final result, the total length of the line is reduced and the quality factor increased. This approach is then suitable to improve the compactness of the analog circuitry, but it does not overcome the problem of the too wide occupation area.

On the other hand, the spiral inductors are often considered unsuitable for the design of power amplifier (PA) because they cannot carry the same quantity of DC power compared to the wide lines used in the PA applications. This statement could be considered true in all the technologies in which the thicker metals of back end of lines are thinner than 2 μm. This is the case of 65 nm CMOS technology used in this thesis. The reduced thickness of the metal (1.2 μm in Alucap layer) does not allow the design of spiral inductors with small line width. Electro-migration phenomena due to the high DC currents could burn the spiral inductors and, then, destroy the circuit. For different technologies (IBM or TSMC) the thickest metals could allow the use of spiral inductors also for the power amplifier applications.

An example that well describes the difference between the two design philosophies is shown in Figure 14. The image represents the first version of the transmitter designed in the framework of Nanocomm project `http://www.nanocomm.fr/` in collaboration with the IMS laboratory of Bordeaux. Unfortunately, due to a problem on the design of the matching network of the mixer, the chip does not work and it will not be discussed in this thesis. However, the microphotography shows the enormous difference in terms of occupied area by comparing the up-conversion chain, realized with lumped elements, and the power amplifier stage, designed using distributed lines.

In the domain of small signal applications, instead, the use of spiral inductors is much more suitable: a very small-size passive devices are feasible due to the extremely small metal widths and distances that can be realized in the available multi-layer metal back-end. Thanks to the very tight fabrication tolerances an excellent repeatability of the performance is achieved. The small sizes, therefore, help to enhance the performance of the device. Due to the loops, the magnetic field

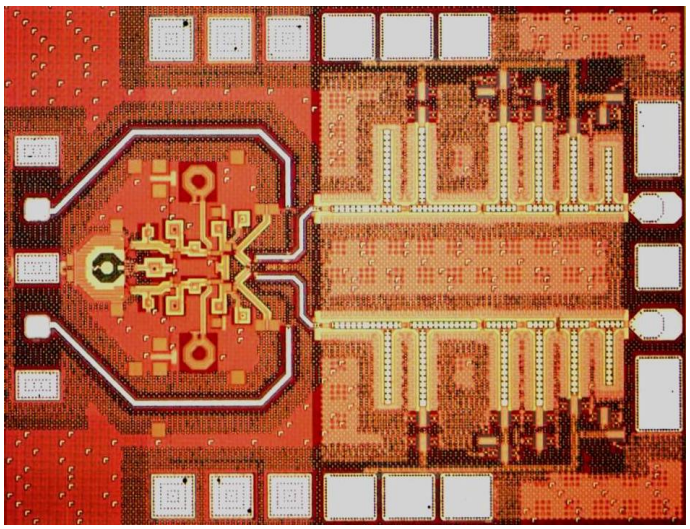

Figure 14: Example of lumped element and distributed element circuit: 60 GHz transmitter

is concentrated and the area over the lossy substrate is minimized. Furthermore, die area is minimized when using lumped elements, which is mandatory for low-cost applications.

ST 65nm metallization process

In order to understand the following part of dissertation is important to introduce the metal stack proposed in the 65 nm technology. The fabrication process offers several metallization choices, were mM-xX-yY-zZ refers to a process with a total of m metal layers out of which x are fine pitch, y are intermediate pitch, and z are thick. Depending on the metallization choice the rules and process characteristics applied to the different metals and via levels are different. In this work a 7M-4X-0Y-2Z process is employed. Figure 15 gives a scheme of principle of the metallization stack. No more details on the composition of the stack will be furnished due to the non-disclosure agreement signed by the author with the foundry.

2.1.1 *Spiral inductors design*

The description of the design and characterization procedure of the small size inductors have already been treated by M. Kraemer in his thesis [18] and summarized in two different publications [33, 34]. For this reason, during the following part of the paragraph, all references (where needed) relating to the thesis of M. Kraemer will be strictly quoted in order to differentiate the contribution done by the two authors.

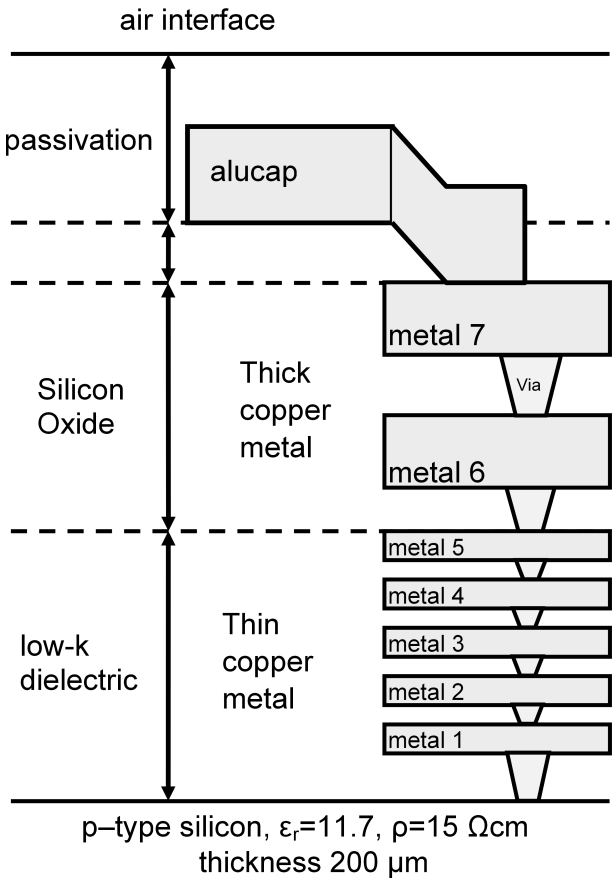

Figure 15: Simplified metal back-end of the 65nm CMOS technology

In the 65 nm CMOS design kit the spiral inductors working in the band of 60 GHz are not available. However, this circumstance does not necessarily represents an issue. On the contrary, it gives to the designer, the possibility to create its own library of elements customizing every single part of the component. Thanks to the possibility to design full custom device it is possible to yield conformal spiral inductors that contribute to the shrinking of the total surface of the circuit. Examples of this statement will be found in every circuit proposed in this thesis.

The fundamental research executed during the Ph.D of M. Kraemer [18] has allowed obtaining the complete characterization of the phenomena around the spiral inductors and the guidelines on the maximization of the component performances[33]. However, some figures of merit and design techniques of these components were not still totally characterized and the target of the following pages is to complete the analysis.

In particular, the study is focused on three fields:

- High value inductors, which require a higher occupied surface;
- Circuits with high concentrations of inductive components;

- Interaction between close inductors.

High value inductors

In [18] a sort of differentiation has been introduced between the small size inductors, which the nominal value is assumed lower than 150 pH, and the larger one. In particular, the author suggests the employment of the only 7th metal layer for the small inductive components and a stacked inductor version using the combination of 6th and 7th metal for the larger version. The motivation adduced to this design approach is the reduction of the occupied area and the concentration of the electromagnetic field in a reduced volume. The approach can be considerate correct but more accurate simulations show that also other parameters are influenced by this metal stacking and not always in a positive way. This is the case of the self resonance frequency (SRF) and the Q-factor (Q) of the coils. The Self Resonance Frequency (SRF) determines the point at which the inductor lost its functionality showing a negative reactance, whereas the Q is a figure of merit that describes the efficiency of the component.

Following the general concept of the chip size reduction, the stacked inductors are preferred to the planar ones. In particular circuit configuration, however, the performances of the component are critical and more accurate structure must be evaluated. In the circuit of the buffer, discussed in Section 3.3 the performances of the load inductors determine the maximum gain of the stage. Figure 17 shows the response of two inductors of 150pH designed following the procedure described in [33] for the square inductors. The simulated structures, on which the discussion of the following pages will be based, are shown in Figure 16.

As the Figure 17 shows, the quality factor of the octagonal version is about 50% better than the one shown by the square inductor (14.288 in the place of 9.488 at 60 GHz). As for the maximum Q, the gap in terms of performance between the two versions increases further: around 93 GHz the estimated Q is 16.1 for the octagonal version and only 10.4 for the stacked version.

The growth of the quality factor is probably due to the high number of 90 degrees curves present in the stacked inductor. The sharp curves increase the charge density on the angles of the winding increasing the resistivity of the structure. In the octagonal shape, instead, the 45 degree curves act like mirrors for the electromagnetic field and they aid the propagation through the component.

The other remarkable difference between the two structures in terms of is the inductor self resonance frequency value.

As shown in Figure 18, the SRF values of the two inductors versions represented in Figure 16 differs only in few GHz (190 GHz for the octagonal version and 178 for the squared one). This difference is further emphasized in case of higher inductance values, where the SRF decreases more rapidly for the stacked version than in the octagonal one. The causes are attributed to the boundary condition of the inductor.

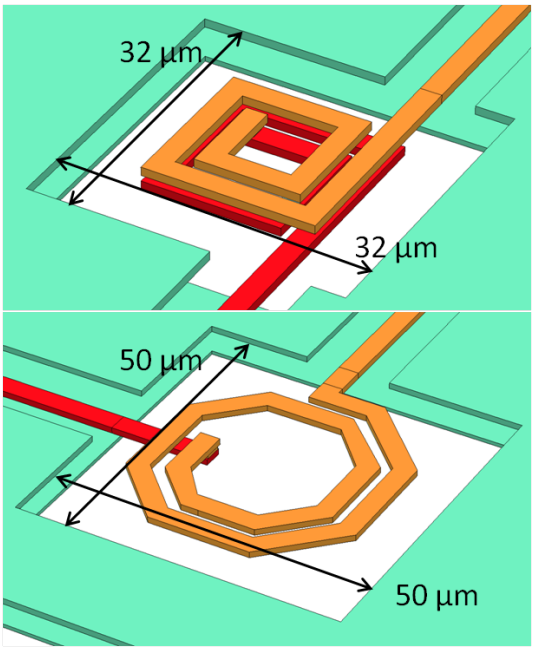

Figure 16: Simulated inductors

In the design flow proposed in [33]the ground reference is placed at the lower metals (metal 1 and metal 2) as the Figures in [33] shows. On the contrary, in the real condition, a metal stack around the coils is necessary in order to contain the EM field of the inductor and avoid the crosstalk among different coils (as shown in Figure 16). The presence of multi-layered ground around the spiral inductor increases the parasitic capacitance to the ground, and in the stacked version of the inductor the doubling of the metal layers increases the fringing capacitance with the ground wall. For high value inductors this effect is more destructive than the capacitive coupling between the coils and the bulk as described in [33]. For this reason planar octagonal inductors must be preferred to stacked one when the circuit requires high inductive contributes.

The only drawback of the planar approach consists in the increase of the occupied area (dimensions shown in Figure 16). Despite the larger area, however, the spiral inductor remains several times smaller than its distributed version and it exhibits higher performances in every aspects.

Circuits with high concentrations of inductive components

The design of circuits with a large number of inductive components introduces a certain number of issue during the design rules check (DRC) procedure. As said before, the inductors used in this work are full custom structures not existing in the libraries of the design kit (DK). As a consequence, it could occur that these elements do not fulfill some of the rules imposed by the foundry.

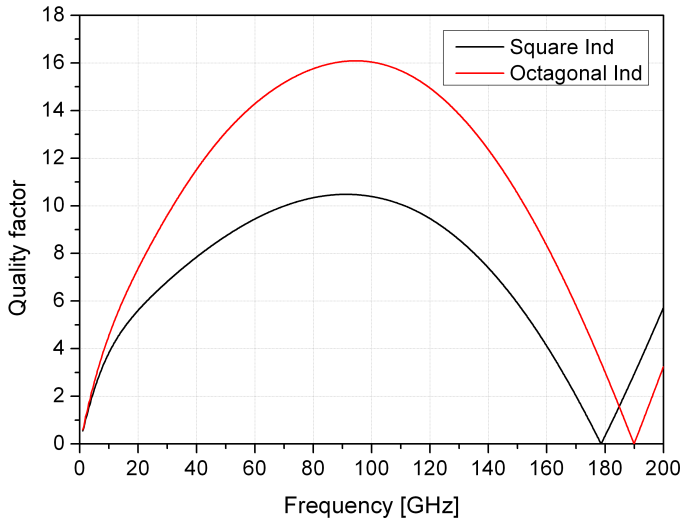

Figure 17: Inductors quality factor

During the inductor synthesis all the basic rules imposed by the design rule manual have been verified: metal width, spacing, number of via, etc. However, the critical aspect concerns the density rules check. For every technology the foundries establish a minimum value of metal density for in each layer in order to assure an equilibrium in the tensile stress inside the chip and to guarantee a flatter surface during the superposition of the different layers in to the back end of line (BEOL) stack. Therefore, several different rules could be systematically violated during the DRC procedure when full custom structures are employed. Among the different rules, the most important are the minimum /maximum metal density per square and the maximum ratio between full-empty metalized areas.

The evaluation method used by the software (Calibre) to verify the metal density is based (squares of 50 µm size). The software scans the entire circuit with step of 1 µm and verifies each time the compliance of the rule inside the square. When one of the described rules is not attained, the software highlights the interested area. Normally, in circuits where a large number of inductors are put into a closed surface the violations of these rules are certain. In effect, although a large part of the designed inductors are smaller than the square footprint used for the verification, the metals employed to separate them are not sufficient to satisfy the filling percentage required by the design rules. Figure 19 shows an example of Design Rules Check (DRC) error on the buffer structure discussed in Section 3.3. The area enclosed in the yellow path does not satisfy the minimum metal density required. In the first series of circuits realized in [18], a series of derogations upon these rules has been requested to overcome this type of errors. This procedure, however, is unconventional and it does not assure the industrialization of the circuits. For this reason, it has been necessary to insert “dummy metal” bricks

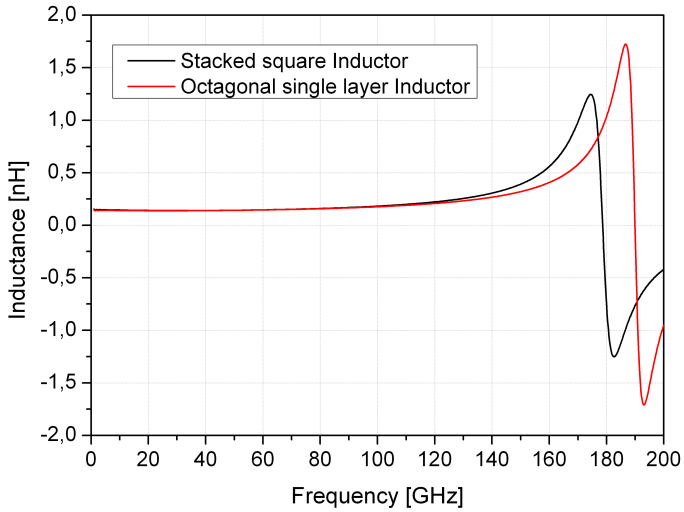

Figure 18: Inductors self resonance frequency

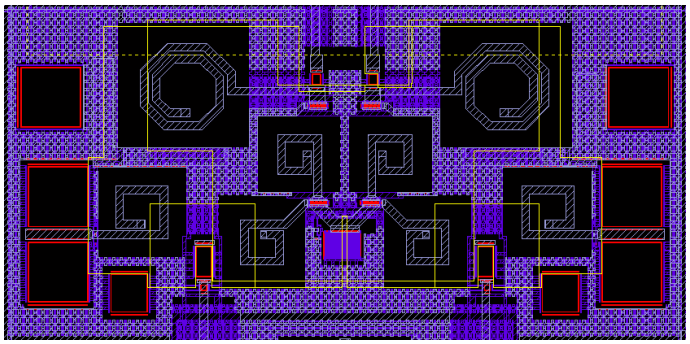

Figure 19: DRC errors in buffer layout

around the full custom spiral inductors. The insertion of these small metallic elements causes, in the first instance, a variation of the inductance value, and moreover, also the others figures of merit of the inductor are influenced. A simulation of the effects induced by the presence of dummy metals around the coils is proposed in [8] and reported in Figure 20. The efficiency of the inductor is reduced with resulting effects on the quality factor and, most of all, in the nominal value of the inductor is changed. Considering the role of the component inside an impedance matching network, the undesired change in the inductor value moves away the desired point of matching with dangerous consequence on the circuit response. Figure 14 shows the most representative example of this type of problem. As will be explained during the mixer characterization section 3.1.1, an underestimated interaction between matching networks and others structures (among which dummy metals) can determine the failure of an entire project. By starting from these considerations, once the circuit is placed into the layout environment, it is opportune to proceed to a post-layout simulation in order to resize, when it is necessary, the inductors containing dummy metals. Normally, a

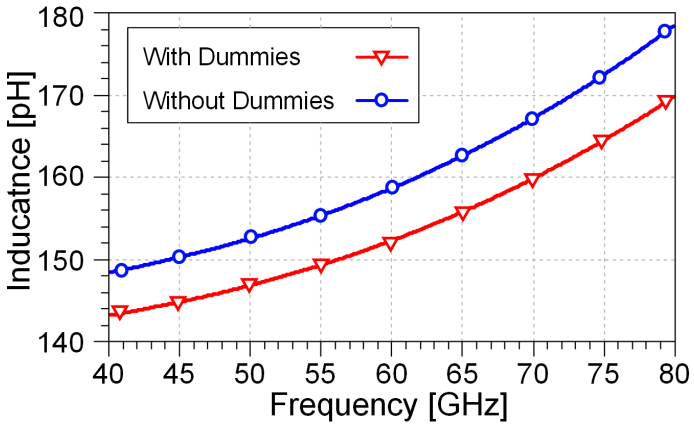

Figure 20: Inductance variation due to dummy metals effect

slight growth of the spiral diameters is required to regain the desired value of inductance. Among the different layers of dummy metals, the stronger effect on the inductor performance is produced by metal 6 dummies. There are two main reasons behind this behavior: metal 6 is near to metal 7, and the required metal density for this layer is higher than for the other layers. Therefore, the metallic bricks are surrounded by a stronger EM field and, on the other hand, they cause a stronger variation of the field around the coil. As a consequence, it is important to manually place the bricks by using shapes that minimize the induced currents on the dummy metals. In this manner, it is possible to satisfy the requirement of minimum metal density and, at the same time, to reduce the interaction between the two systems as much as possible.

Interaction between adjacent inductors

The crosstalk between neighboring inductors is a problem with the same level of criticality of dummy metals. As for the presence of floating metals, the interaction between adjacent inductors has to be carefully analyzed. In the impedance matching networks the mutual inductive coupling could be source of undesired paths for the electromagnetic field. A representative example of the possible problems deriving from undesired signal paths could be once again the buffer block of Section 3.3. This block is widely employed during this thesis work in both transmission and reception chains. For this reason the design of this stage has been optimized under different aspects, such as the reduction of occupied area. By observing the buffer block it is possible to see how the different spiral inductors are placed in order to occupy all of the available space. In the previous subsection this approach has required a special treatment to satisfy the metal density rules. Here, instead, the crosstalk issue is treated and solved (where it was possible). A very useful paper [35] shows how it is possible to increase the isolation of neighboring inductors using metal walls working as shields. In [35]

the simulations exhibit an improvement of 19 dB in the coupling factor of the two structures. However, the proposed test bench can be considered as an ideal configuration. Actually the placement of inductors in the buffer circuit is many times more complex and a complete Faraday cage, as assumed in [35], is not achievable. Consequently, the technique here employed in the design of the buffer can be considered an evolution of the one proposed in [35]. The objective of the electromagnetic cage is to block the currents induced by the inductor and to avoid theirs propagation into the other structures. A very representative image describing the arising effect is proposed in [18] and here reported in Figure 21(a) , while the current simulation, in Figure 21(b), confirms the presence of high

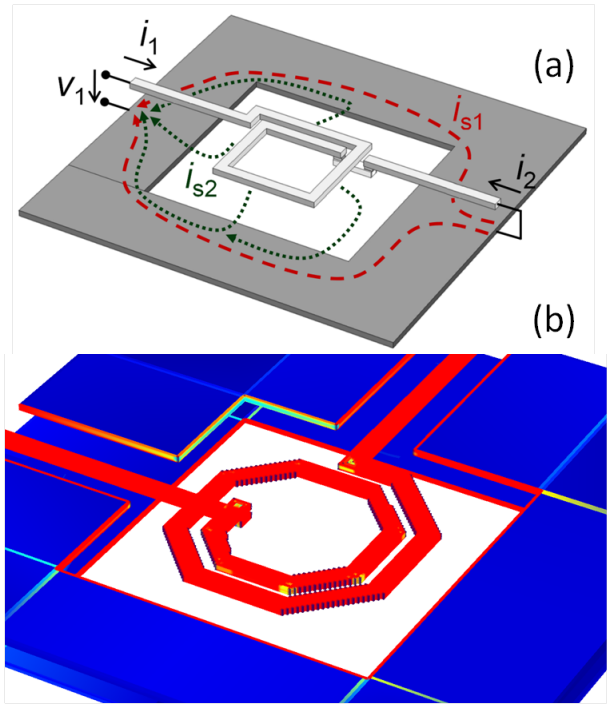

Figure 21: Induced currents around the spiral inductors (a) [18], (b) Sonnet simulation

currents in the ground edge. Therefore, the technique employed in the buffer design consists in a stack of the seven metal layers (interconnected by arrays of via) which surround the entire structure and in conjunction with the points of interconnection between the different coils. To overcome the coils interaction issue the proposed solution is to use microstrip lines transitions. By using this design strategy the fields generated in the cavity where the inductor is placed is closed by these transitions and the currents loops generated by the inductors are closed in the microstrip lines. In this way, by means of the induced current dispersion on the adjacent spiral inductor, the possibility of RF coupling is avoided and the performances obtained in [35] can be maintained also for more complex inductors placements.

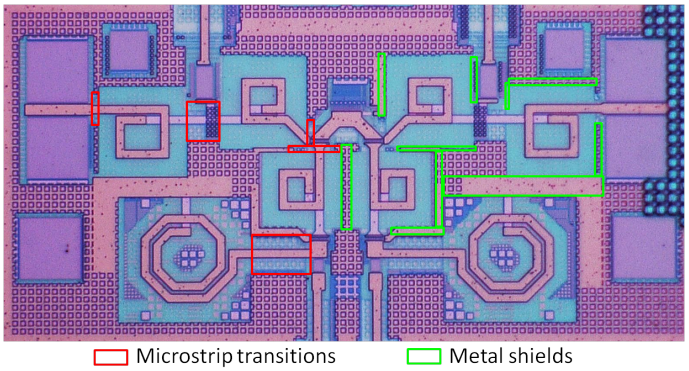

Figure 22: Shielded inductors in the buffer block

Figure 22 represents the buffer block, the points where this technique is employed are highlighted. In order to simplify the observation of the figure, being the circuit symmetric, the transitions and the metal walls are shown only on the left side and on the right side, respectively. This architectural solution has allowed obtaining extremely compact circuit with a highest number of spiral inductors concentrated in a smallest area. The non-interactions between the spirals are proved directly on the standalone buffer in single-ended configuration (discussed in section 3.3 and deduced, for the differential version, in the measurement of the local oscillator driver system shown in section 5.2.1).

2.1.2 *Conclusions*

The investigation realized on the lumped inductors structure has allowed obtaining an improvement of the inductors design under different points of view. First of all, the analysis of the high size inductors has defined a new guideline to design big inductances with reasonable quality factor and higher self resonance frequency. The characterization of the dummy metals interaction has also permitted to define the influences that these small floating metals have on the RF performance of the lumped components. Finally, the design of high performance isolating structures surrounding the spiral inductors has drastically improved the compactness of the circuits maintaining high isolation values among the several inductors present in the discussed circuits.

2.2 HIGH PERFORMANCES LINES

The same procedure developed for the inductor design has been exploited in order to design high performance 60 GHz lines. These structures are required to interconnect the different blocks when a direct contact between the input/output blocks is not possible. This circumstance occurs in particular on the design of I/Q receiver discussed in Section 5.2.2. There are only two possibilities to realize low

loss lines on silicon substrate: microstrip and coplanar lines. Both types of lines have the advantage to shield the lossy silicon substrate: the microstrip by means of its ground plane whereas the coplanar line by focusing the field between the signal line and the two ground planes situated on either side. The two typologies of lines exhibit strength and weakness points. As for the microstrip lines, the main issue is the coupling with the others lines. Despite the small distance between ground and signal line, in very dense circuits the possibility of crosstalk between nearby lines is considerable. On the other hand, concerning the coplanar lines, there is the possibility to have part of the EM field penetrating the low resistance substrate (generating resistive losses). Another important issue, in particular in the high concentrated circuits, is the ground contact among the different parts of the circuit. In order to cancel all possible weakness and exploit the benefit of both structures, the here proposed solution is to employ the Grounded Coplanar Waveguides (G-CPW). The sections of the three structures with their respective electric fields are described in Figure 23. The distribution of the field demonstrates

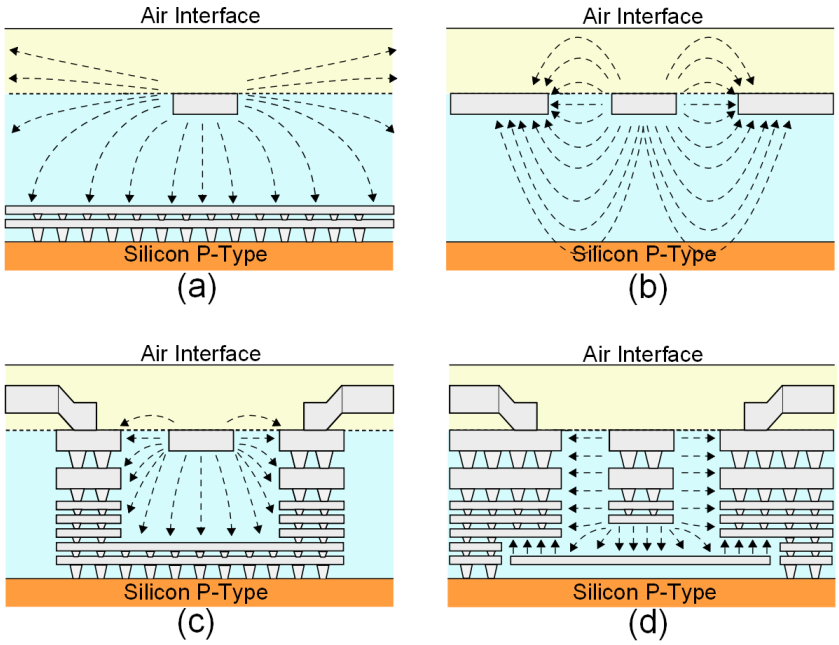

Figure 23: Structures of integrated lines: (a) Microstrip line; (b) Coplanar line; (c) Grounded coplanar line; (d) Slow-wave line

the improvement that the G-CPW yields comparing to the other two. This type of lines are therefore largely employed in the design of LO driver system; as for instance to connect the four LO signal coming out from the Wilkinson dividers pair (Figure 107) Thanks to the reduced transversal section of the lines id derives a very low coupling factor in the crossing lines as described in the section of LO power driver system.

To conclude, Figure 23(d) describes the section of a slow-wave guide architecture. This particular approach to design the slow-wave lines is proposed by P.

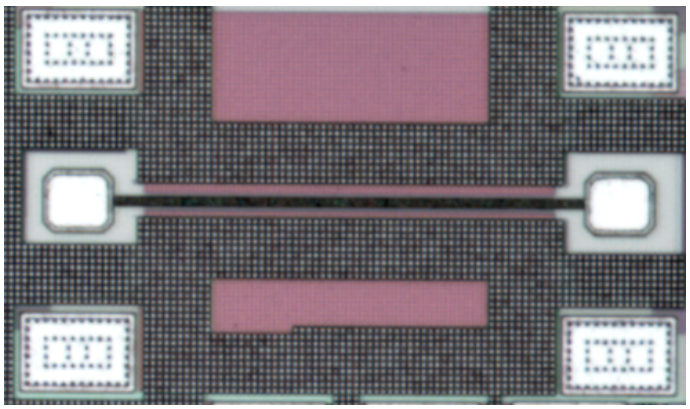

Figure 24: Slow wave Line test bench

Ferrari in [31]. There are also other approaches to obtain a slow-wave behavior but, in according with the designer of [31] this architecture is considered by the author the most interesting version. In effect, among the different subject treated during the thesis's work, the realization of CMOS phase shifter has been marginally explored. A test bench structure has been then developed in order to evaluate the benefits of this technology. It is important to underline, however, that due to the proximity with a production run the design of the lines has not been deeply investigated. Simulations executed with sonnet are not performed for this type of structure and the final result is quite far for the simulated one. Despite the time problems, the structure represented in 24 with its corresponding version realized in G-CPW shows very interesting performance in particular for the increased propagation time.

The two lines have a total length of 315 µm. In Figure 25 is described the

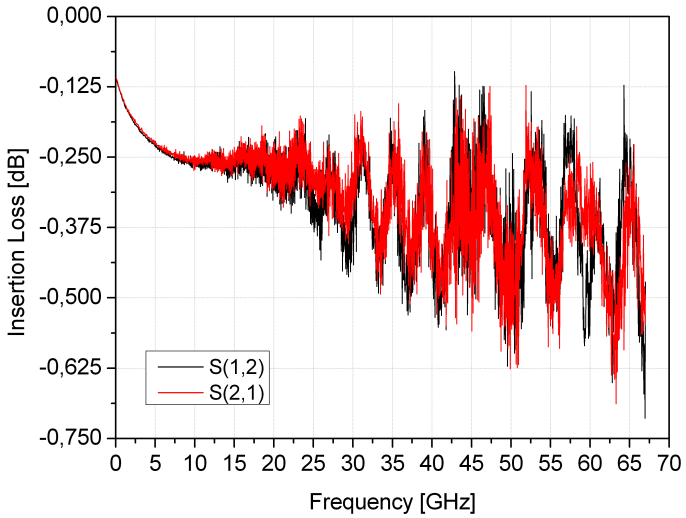

Figure 25: Insertion Loss of G-CPW line

insertion loss shown by the G-CPW version whereas in Figure 26 is traced the IL of the slow-wave one. The results of the G-CPW are in line with expectations

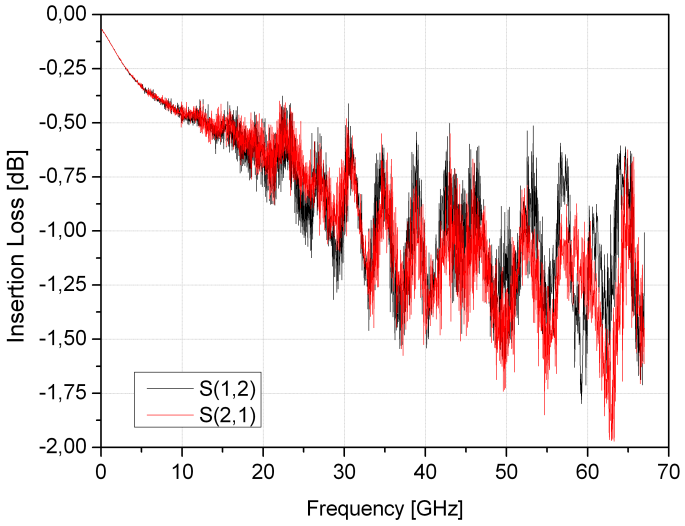

Figure 26: Insertion Loss of slow-wave line

while the slow-wave line shows a higher IL. This difference however is also probably due to the mismatch between the line impedance and the probes one. A de-embedded measurement shows characteristic impedance for the slow-wave line close to 20 Ω instead of 50 Ω. A redesign of the geometrical dimension of the structure is then required in order to obtain the desired impedance value. Concerning the previously discussed performances of the slow wave line in terms of increased propagation time, Figure 27 reports the phase of the $S_{(2,1)}$ parameters for both the lines. As it is possible to see the phase of slow wave lines is doubled compared to the G-CPW one. Therefore, this result confirms the rise of the ε_r value inside the substrate due to the increased capacitive coupling of the lines.

2.3 BALUNS

Among the complex passive structure the first discussed component is the balun. The differential architecture, chosen for the implementation of the transceivers system, has been influenced by the balun performances for the first characterization of the stand alone blocks as shown in Figure 71 in the mixer characterization section 5.2.4 and also in the complete transmitter chain as shown by Figure 99 in section 5.1.1

There are many different approaches to build a balun and, in function of the adopted conception method, it could assume various sizes. The classical design for this structure was proposed by Nathan Marchand in 1944 [36]. The Marchand balun is based on the use of open circuit $\lambda/4$ coupled lines. Other types of balun can be derived by rat-race hybrid coupler and by transformers.

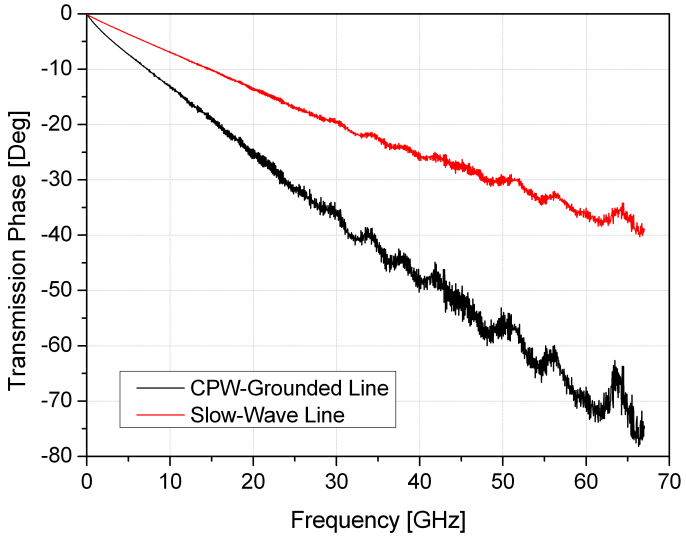

Figure 27: Transmission delay of the two types of lines

2.3.1 *Transformer Balun*

The size of cited baluns, with the exception of the transformer version, depends on the wavelength and, therefore, its dimension into the chip could be excessive compared to the remaining part of the circuit. The size of the transformer balun, instead, is independent on the wavelength, hence its dimension can be significantly reduced. The balun presented in the next pages is based on the transformer configuration in order to obtain the minimal occupied surface on the silicon. The purpose of the project is to yield a signal conversion from single ended to differential mode, but, thanks to the nature of the transformer, an impedance transformation could be also taken into account if necessary.

Analytical study of the Balun Design

In [37] Dickson describes the performances that an integrated transformer can reach in a CMOS technology. Dickson shows two classes of transformer layout: planar and staked transformer. The first one has the two coils into the same metal layer, and the undercrosses to avoid the short circuit are obtained using the inferior metal layers. This technique of design requires the respect of the minimum intra-line distance (d) set by technology rules and imposes two other constraints: a geometric constraint (determining the minimum occupied area), and a electromagnetic constraint (imposing the coupling factor k). The area used for the outer diameter of coils and the value of k for the two coils are of 45 µm and of 0.5, respectively [37] . The stacked version of transformer, instead, shows a higher value of coupling factor ($k = 0.75$) with a reduction of the coils diameter (30 µm). This behavior is due to the proximity effect between the coils. In this configuration the distance between the primary and the secondary coil is set by

the technology: in this case, for a transformer built in contiguous layers (metal 6 and 7), the gap between the metals is 600 nm. The proximity effect creates a strong capacitive coupling that, in addition to the magnetic field, increases the value of k. The main design parameters for both the before-mentioned transformers are the footprint and the coils shape.

The most important causes of losses, in fact, in the integrated transformers are: the resistive loss of the metal lines and the losses of electromagnetic field into low resistive silicon substrates. The reduction of coils diameters and the rise of lines width are the most efficacy countermeasure to minimize these effects. The shrink of the coil diameter reduces the magnetic field around the windings and, consequently, causes a drop of the k value. The growth of lines' width, instead, shows different behaviour in function of the nature of the transformer. For the planar version, the enlargement of lines width increases the total occupied area and raises the bulk parasitic capacitances. This latter effect is still more undesired because it is responsible of the reduction of the self resonances frequency of the structure. Differently to the planar transformer, in the stacked version the occupied area remains practically unchanged, but, the mutual capacitance between the coils increases and this produces a growth of k. These considerations conduct to the choice of stacked solution in the place of planar transformer: in particular, the reduced dimension and the greater value of k could be exploited to design a high integrated and low losses balun.

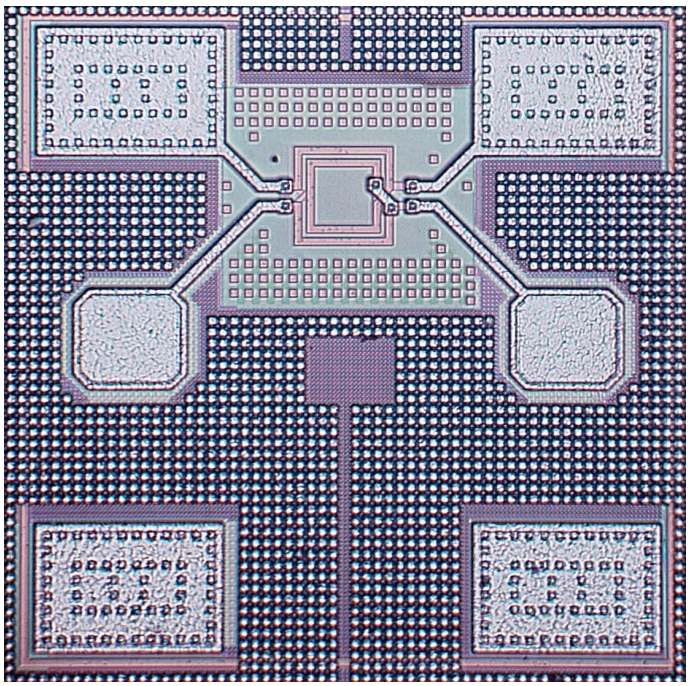

Figure 28: Die of the transformer used to validate the simulations.

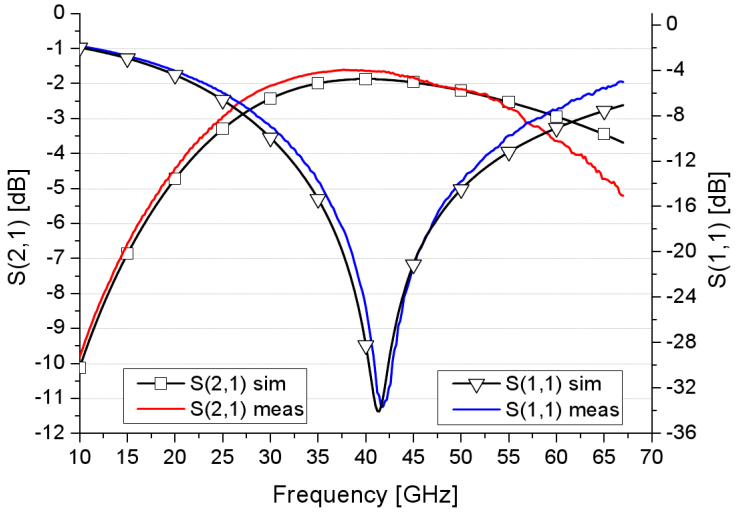

Figure 29: Measurement and simulation of the transformer block

If the discussed component is in the transformer configuration, it consists of 2 ports, the single ended input and the single ended output, whereas the other termination of the coils are shorted to ground. In the balun configuration, instead, the secondary coil is floating and both the terminations are used as outputs. In these conditions a virtual ground is placed at the middle of the floating spiral. Assuming that this theoretical behavior of the coil was satisfied, the balun synthesis would be reduced to the dimensioning of the coil diameter (in order to specify the central frequency) and to the optimization of the metal width (in order to minimize the insertion loss). The transformer configuration of the structure is realized and measured in a stand alone block. Figure 28 shows the photo of the transformer die and Figure 29 compares the simulations, performed using Sonnet software v12.52, with the measurements. The high reliability of the simulations is confirmed by the good fitting of the presented curves. Starting from these results the transformer structure was re-adapted to work as a balun. The ground contact of the secondary coil was removed and connected as a differential signal port. On the contrary of what is expected, however, the simulations of the proposed balun set-up show a response very far from its theoretical behavior. In fact, the transmission parameters S_{12} and S_{13} have completely different trend: instead of staying close for the whole frequency range, they remain quite close only at lower frequencies, while they diverge quickly with increasing frequency. Concerning the phase difference between the differential ports, the simulations show a phase shift extremely far from the 180 degree asked by the balun specification. Figure 30 shows the simulation results of this component. The curves confirm a behavior completely distorted for the balun. By means of a study of the structure and the evaluation of the current, developed using CST Microwave Studio and Sonnet, respectively, a theoretical explication of this behavior is proposed. In particular, the analysis of the electromagnetic field in

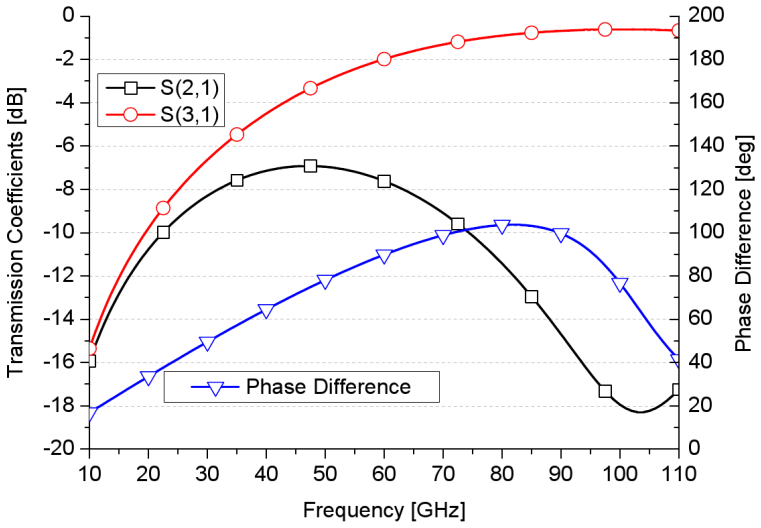

Figure 30: Amplitude and phase measurement of standard transformer in balun configuration

the structure highlights a very strong capacitive effect between the single-ended and the differential coils. These phenomena can be explained by the geometrical structure of the transformer balun. The component shape, as discussed in the previous section, is built on two superimposed metal layers (metal 6 and metal 7) With a gap between them of only 600 nm of thickness filled by silicon oxide ε_r of 4. At 60 GHz and with the described geometric conditions the superimposed lines work as a semi-distributed capacitors. The conducted full wave simulation confirm a very stronger capacitive effect compared to the magnetic field around the coils. In these EM conditions, the transformer does not work with the required balance between electric and magnetic contribute of the field, and therefore, the proposed shape for the balun does not respect the classical expected behavior. More specifically the variation of the EM fields in the balun changes the current density along the spirals and, as a consequence, the hypothesis of virtual ground placed in the middle of the secondary coil is violated.

To force the potential to be zero in the middle of the secondary coil, a short circuit was imposed by the connection of the spiral to the ground. Figure 31 shows the simulated structure. However, despite the ground connection, the response of the structure remains extremely different from the required one. Simulations performed on this architecture and reported in Figure 32 shows that the structure remains imbalanced and, consequently, it cannot be used as a balun. In the following section a new balun architecture is proposed to overcome this limitations.

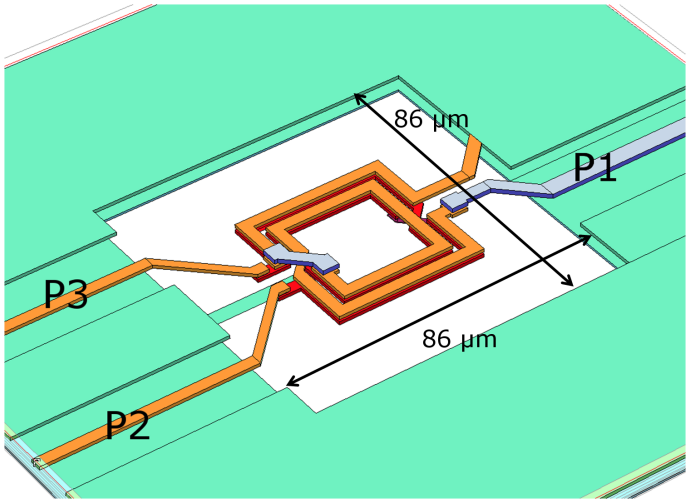

Figure 31: Grounded transformer balun

Transformer to Balun Transition

The results obtained through the analysis executed in the previous section provide a new base for developing a new structure of balun. In effect the high coupling and the reduced size shown by the transformer remains a really interesting feature. In order to exploit these qualities, the shape of the transformer must be changed as well as the electromagnetic interpretation of the component. Concerning the first point a total redraw of the shape has been executed. Instead of employing a single coil for the balun, two separate and consecutive coils are used. Furthermore, for the single ended part, two identical coils are used, whereas, for the differential part two distinct windings are placed in correspondence of the single ended coils. Figure 33 represents the proposed shape of the new balun. In a first analysis, this component can be seen as two different single ended transformers generating a differential signal at theirs outputs when a signal is sent at the single ended input port. As long as the response of the integrated transformer is far from the classical low frequency response, the interpretation of the balun behavior cannot be completely exact. Therefore, the modeling of the interaction between the pairs of coils has to be treated differently.

Mathematical model for the proposed balun

To model the new transformer balun, instead of representing the interaction using the equivalent circuit, an evolution of the coupled lines model is employed [37]. However, due to the particular boundary condition of the lines that compose the balun, the coupled line model used here is different from the one proposed in [38], especially in regards to the influence of the ground upon the lines. The electromagnetic field around the coupled lines is different compared to the standard representation, therefore, also the classical formulas used to determine the lines'

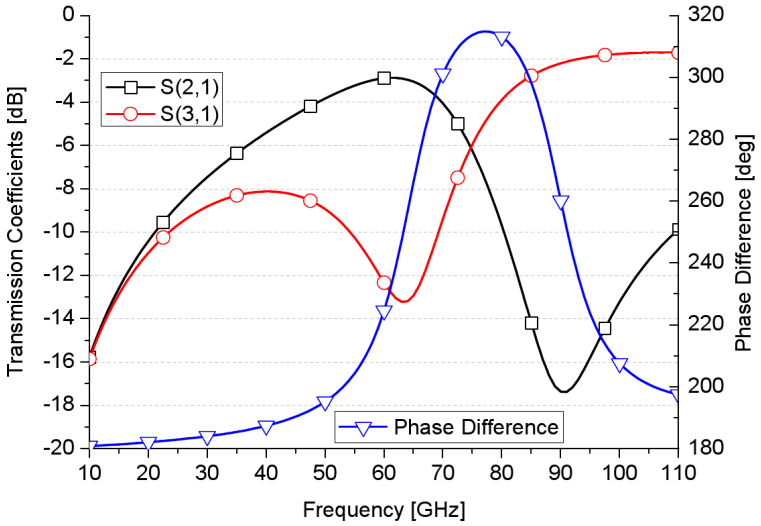

Figure 32: Measurement and simulation of the grounded transformer balun component

impedance must be changed. To explain how the power flow through the passive component, a pseudo-empiric approach is adopted. The next considerations have been extrapolated evaluating the electromagnetic field, the current density, and how the power flow evolves in phase of simulations. The size of the coils, their position, and the position of the ground contact are taken into account to verify the variation of phase difference and power flows at the output of differential ports. The equivalent circuit used to explain the power flows and to propose a behavioral model of the Balun is based on the scheme shown by Figure 34. There are two different contributions to be taken into account: the coupled power (C) and the transmitted power (T). To build the model, the single ended port and the differential ports have been assumed as input and as outputs, respectively. C represents the signal captured by the coupled line, while T is the power that remains on the first line. In our case, a direct correspondence is assumed when the interaction is described: the first line is the first coil of the primary part of the balun, whereas their coupled lines represents the secondary coil (output port 2). The same concept is extended at the second part of balun for the port 2. The relation between T and C is described in [38] and here reported for brevity:

$$T = \sqrt{1 - C^2} \tag{2.1}$$

For a classical coupled line coupler with $\lambda/4$ lines the value of C can be evaluated by:

$$C_{dB} = 10\log\frac{P_3}{P_1} = S_{3,1} \tag{2.2}$$

The coupled lines model proposed to represent the coils has two main differences if compared with the classical model: the lines lengths are much smaller than $\lambda/4$, and the coupled port (P_3 in Figure 34) is shorted to ground. The difference in

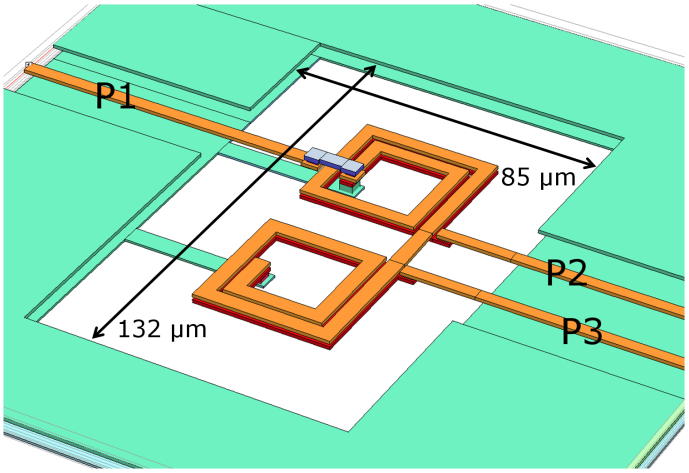

Figure 33: Sonnet 3D layout representation of the novel shape for the proposed balun.

terms of line length influences the maximal value of coupled power; while, the short circuit in the coupled port changes completely the response of coupled lines. To understand what happen with this coupler set-up, the following equations of $S_{2,1}$ and $S_{3,1}$ will be discussed:

$$S_{2,1} = C' \sqrt{1 - C'^2} e^{j\theta} \Gamma_{cc} + \sqrt{1 - C'^2}(1 - C'^2) C' e^{j\theta} \Gamma_{cc} \tag{2.3}$$

$$S_{3,1} = C' \sqrt{1 - C'^2} e^{j\theta} + \sqrt{1 - C'^2}(1 - C'^2) C' e^{j\theta} \tag{2.4}$$

In these equations, C' represents the coupling factor in the coils, while Γ_{cc} is the reflection coefficient in short circuit termination. In the $S_{2,1}$ formula there are two main contributions of the power delivered by the pair of coils. The first part represents the power captured by the coil number 1. The power coupled into the second line and sent into coupled port is $C' e^{j\theta}$. The coupled port is closed in short circuit causing a complete reflection of the coming signal. At this time step the concept of coupled line is mirrored: coupled port becomes the input port and vice versa. Now, the old isolated port (P_4 in Figure 34) becomes the transmitted port for the mirrored coupler and the power that flows in direction of this port is $\sqrt{1 - C'^2}$. As for the second contribution in 2.3, the behavior is quite similar. Transmitted signal in first coils ($\sqrt{1 - C'^2}$) became the input power for the second line coupler. It will be in part coupled and sent directly to the output generating the first term of equation 2.4 (P_7 in Figure 34), while, the transmitted portion is reflected on short circuit in P_6 and re-transmitted back to P_5. This power bounce generates the $(1 - C'^2)\Gamma_{cc}$ coefficient and the power returns into the first coil where it is directly coupled to the output P_4 with $C' e^{j\theta}$ coefficient (second term of equation 2.3). The last contribution that remains to explain is the second term of 2.4. This term is characterized by a first coefficient of $\sqrt{1 - C'^2}$ that models the power coming to the first coil. Afterward, a part of power is directly coupled, as said before, and another part is transmitted. The transmitted power is

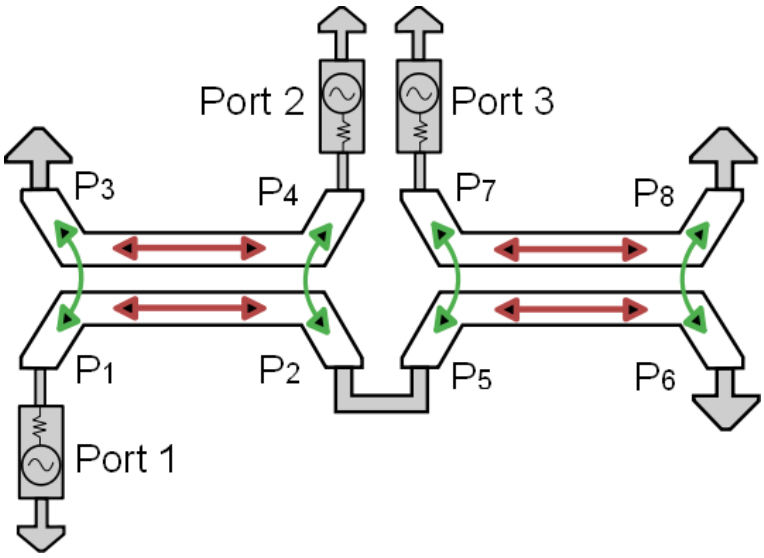

Figure 34: Power flow model fort the new Balun.

reflected Γ_{cc} on the short circuit, coupled on the secondary lines by $C'e^{j\theta}$. The short circuit in port P_8 reflects another time the signal and erases the 180° phase shift. After the double reflection the signal is finally sent at port P_7 by $(1 - C'^2)$ coefficient. Following this procedure of analysis, it is possible to generate a 3×3 scatter matrix including the principal contribution of power flowing among the three ports (matrix 2.5).

$$\begin{bmatrix} 0 & C'T'e^{j\theta}\Gamma_{cc} + T'T'^2C'e^{j\theta}\Gamma_{cc} & C'T'e^{j\theta} + T'T'^2C'e^{j\theta} \\ S_{21} = S_{12} & 0 & C'e^{j2\theta} + T'C'e^{j2\theta} \\ S_{31} = S_{13} & S_{32} = S_{23} & 0 \end{bmatrix} \tag{2.5}$$

In 2.5 the T' coefficient represents the power transmitted on the lines. In the matrix it is possible to remark that there is the expression $T'T'^2$, this representation method is adopted by the author to underline the possible difference on the transmission value between the power couplings into the coils. This consideration is also valid for C', being directly dependent on T'2.1. In the matrix any difference is imposed to distinguish the two coils contributions; this strategy has been adopted in order to avoid a hard and unnecessary rigorous representation of the factors. However it is good to know that these variations exist even if their values are smaller. The effects of different values of coupling will be treated in the optimization structure sections.

Lumped component model

In order to facilitate the use of different simulator engines in Cadence, an equivalent lumped model has been developed for the proposed balun. The considerations exposed about the behavior of the balun's structure suggest the use of the

coupled line coupler model to give a first raw representation of the component. However the model must cover a band as wide as possible to yield a reliable response for all of the possible harmonics eventually present inside the spectre and therefore, to assure convergence of the simulations. In order to satisfy this constraint, the classical coupled line coupler model is extended with the help of the wide band inductance model shown in [37]. The fusion between these two equivalent circuit representations has been done to extract the lumped model for the proposed balun. Figure 35 shows the detailed scheme. Each one of the four lines are represented by a Π circuit, a series of capacitors are placed in the model to represent the capacitive coupling between the coils, and six mutual inductance components are employed to consider the magnetic coupling among the four coils. The not ideal short circuit to ground for the three lines is modeled by series resistances and, on the input and output ports, inductors are placed to represent the inductance of the connection lines. Figure 36 shows the comparison between simulated 3D structure and circuital model. The response of equivalent circuit is extremely close to the real behavior of the structure.

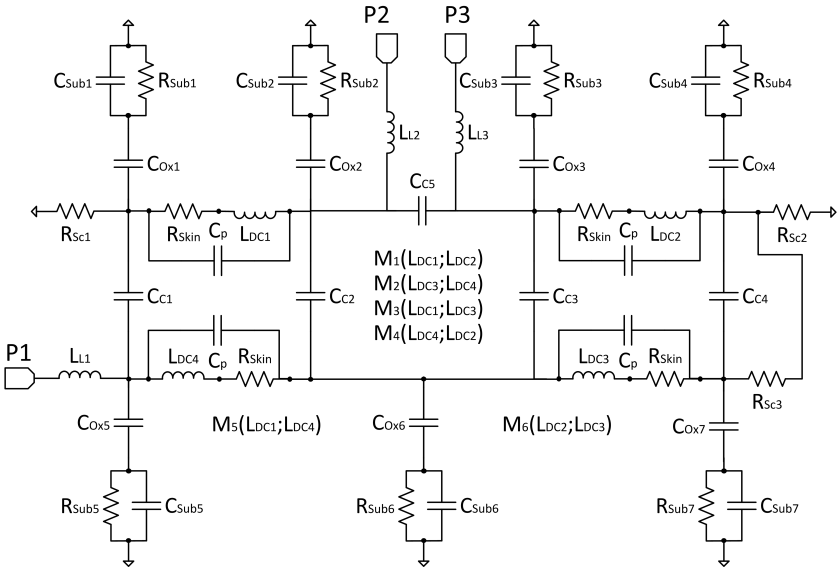

Figure 35: Equivalent lumped circuit for the transformer balun

Electromagnetic Simulation and Measurement

The simulations and the optimization of the structure have been done using Sonnet. The conception of the balun has been based on previous experience in inductors and lines design [33, 8] has facilitated the conception of the balun. Line losses have been taken into account employing a thick metal model for the conductors and a multi-sheet representation for the inner metal meshing. This strategy permits to evaluate, with a good level of accuracy, the skin effect on the metal that at 60 GHz causes remarkable difference between EM simulations

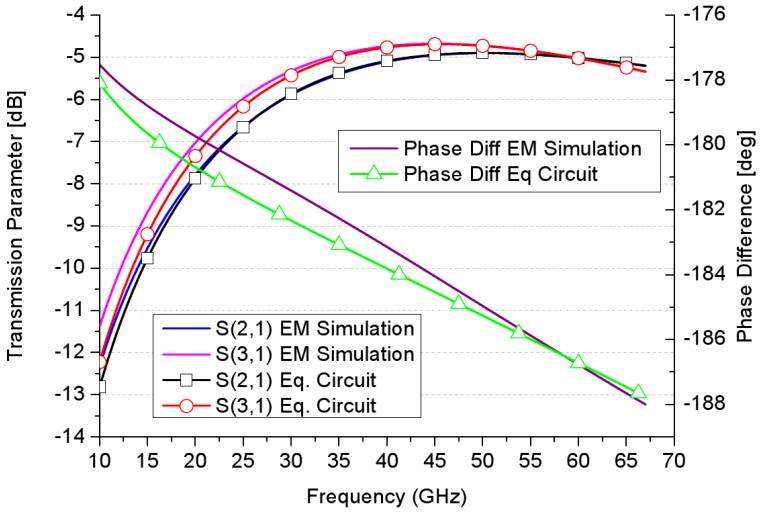

Figure 36: Curves fitting between electromagnetic and circuit simulations

and measurements. The only drawback of this method is a raise of requested memory and duration time of simulations. In particular, by using a Z800 HP workstation with 8 core and 16 GB of RAM, a complete simulation of the structure requires from 1 to 15 hours in function of the number of mesh sheets for each metal layer. To proceed to the first tuning of the balun, simulations have been done with a limited number of sheets (in this case 2). The target of the first step was the maximization of the transmitted power in the whole frequency band of interest. In these circumstances, the work was principally focused on the sizing of diameter coils and on the definition of the free space around the balun. This procedure is quite easy to accomplish and a reduced number of simulations cycles are needed to do it. To reach the optimal power and phase balancing at the differential outputs, instead, a second optimization flow is required. Due to the weak electromagnetic interaction between pairs of coupled lines, the optimal balancing at the differential ports is not attained. To compensate these effects, the size of the second coupled line has been changed during the optimization. The variation has interested the diameter and the metal width of the coils. At the end of this process the total length is 174.5 µm for the first coupled line, while; is 184 µm for the second one. As for the metal width, the optimization has suggested an increase of 0.5 µm for the second coupled line. In Figure 37 a test bench layout of designed balun is shown. With regard to measurements, a de-embedding procedure described in [34] is used to eliminate the lines and pads interaction.

The measured balun responses are shown in Figures 38, 39 and 40. Figure 38 shows the transmission parameters $S_{2,1}$ and $S_{3,1}$. The balun furnishes a bandwidth much wider than required. Considering the whole measured band (10 GHz - 67 GHz) the component shows a maximum value of transmission coefficients of -4.9 dB at 44 GHz, and, the -3 dB point corresponds to 21 GHz. The amplitude

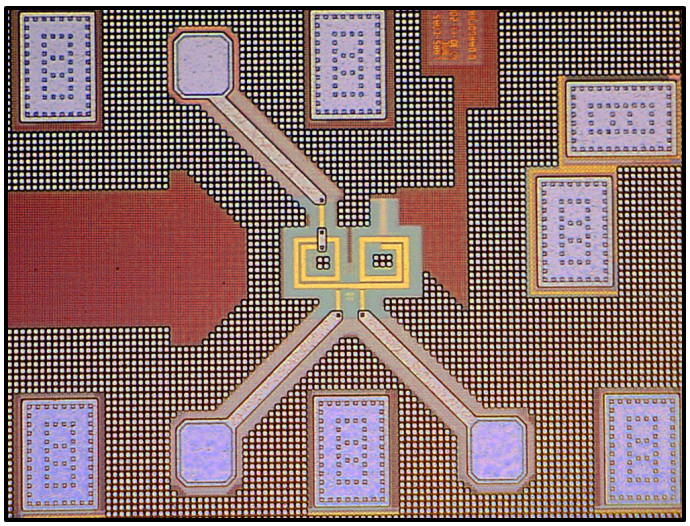

Figure 37: The test bench used to characterize the balun.

difference, reported in the right axis of Figure 38 is limited to 0.2 dB for the desired band of our applications (57 to 63 GHz). For the 3 dB band (44 to 67 GHz), the amplitude difference rises up to 0.5dB. The phase imbalance, shown in Figure 39, remains limited to 8 deg (in the band of 60 GHz applications. The curve exhibits small oscillations, in particular at high frequency; these are probably due to the measurement setup but the reproducibility of the trends, obtained by measuring different chips, confirms the quality of the component. To conclude this section about measurements, Figure 40 shows the reflection coefficient of the balun. As it can be noticed, the structure is not matched to 50 Ω at 60 GHz. In particular, differential ports show an inductive degeneration due to the short circuited lines in the balun. Differently, for the single ended port, the response at 60 GHz is capacitive; this is due to the high capacitive coupling among the primary and secondary lines. Seeing the response in magnitude, the matching at the three ports is lower than -6 dB and an appropriate matching network is required.

Despite the lower matching at the input and output ports, the balun shows very high performances. Considering the size and the losses, the proposed component achieves performances that overcome the state of the art for the balun architectures. As it has been anticipated, an opportune matching network is needed to allow a good exchange of power with the others connected blocks. The design of matching network could be exploited to execute further improvement of the balun response as well. The difference in length and width on the second coupled lines changes the line impedance and, consequently, the reflection coefficient. In order to obtain the same reflection coefficient at the differential ports an asymmetrical matching network is requested. Furthermore, being the device completely passive, the variations on the output ports changes the single ended impedance as well. Consequently, the design of single ended and of a differential

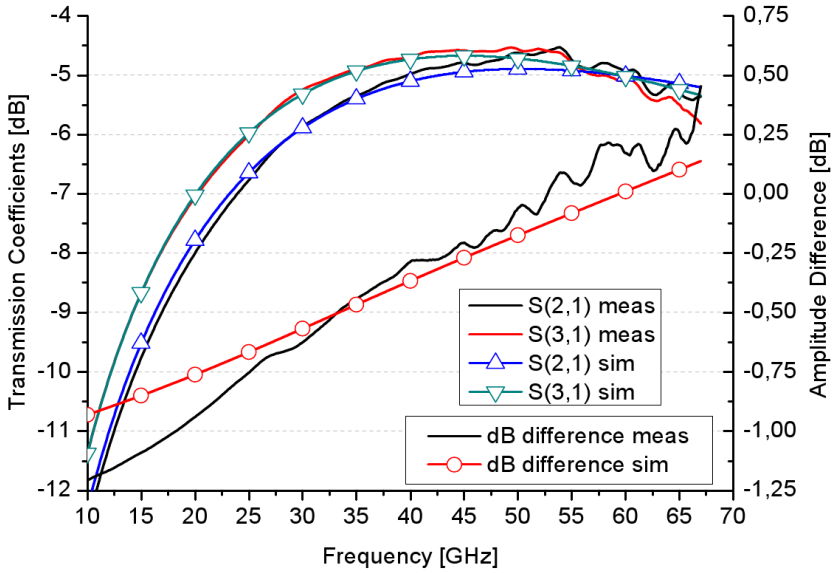

Figure 38: Transmission coefficients and Amplitude difference between the differential outputs

matching network must be done at the same time. As said before, the differential ports have an inductive part that can be compensated with a simple capacitive matching network. Instead, for the single ended port, a series inductor is requested to erase the capacitive behavior. On the other hand, the insertion of inductor accomplishes the matching at the input port but increases the mismatch and the phase imbalance at the differential output ports. To mitigate this effect, the countermeasure is very simple: the differential outputs require a series capacitance followed by a shunt capacitor. The series capacitor has a double effect: the first one is to push the reflection coefficient in direction of real impedance axis, and the second one is to reduce the phase imbalance between the two ports. In fact, the value of the two series capacitors is different and the difference is around 10%. The value difference for the capacitor is of 10 fF (94.5 fF - 104.5 fF).

2.3.2 *Marchand Balun*

The work performed during the design of the transformer balun has highlighted how the line, designed to work as spiral inductors, have shown a strong coupled line coupler behavior. Starting from this assumption and considering the nature of the Marchand balun topology a compact version of this balun is proposed and demonstrated in the following pages.

Theoretic analysis of the component

The issue of the size reduction for the Marchand topology is already treated in many different studies. Interesting solutions are investigated by Robertson with a

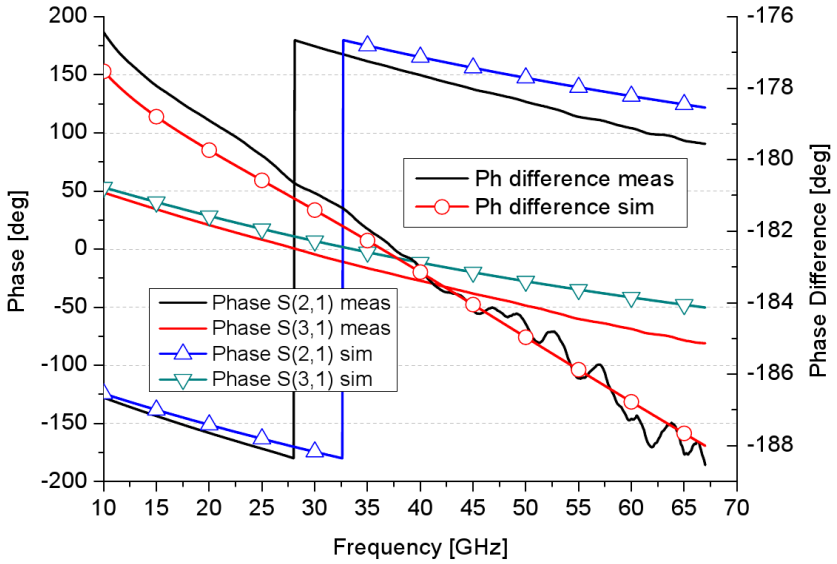

Figure 39: Phase of transmission coefficients and total phase difference among the differential outputs

spiral approach [39] and also by Liu [40] who employs meandered placement for the couplers. The use of these solutions aim at the reduction of the total occupied area and they will be taken into account during the design of the proposed balun. The Robertson structure will be adopted as component shape. The main difference between the proposed structure and [39] is the use of coupled line couplers having lines much shorter than classical $\lambda/4$ length. The line shortening has two main consequences: first, the desired size reduction is achieved; second, a variation of the coupled line coupler behavior is remarked. As a consequence of the latter effect the first step on the analytical part of the work is to find a simple and scalable behavioral model for the short coupled line coupler and use it to redesign the compacted Marchand balun.

The formulas to describe the transmitted T and the coupled C power in a coupled line coupler are know and described in [38]:

$$S_{12} = \frac{\sqrt{1 - C_{Co}^2}}{\sqrt{1 - C_{Co}^2}\cos\theta + j\sin\theta} = T \tag{2.6}$$

and

$$S_{13} = \frac{jC_{Co}\sin\theta}{\sqrt{1 - C_{Co}^2}\cos\theta + j\sin\theta} = C \tag{2.7}$$

Here C_{Co} represent the coupling coefficient between the lines in the coupler and θ is the electrical length of the lines.

$$C_{Co} = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{2.8}$$

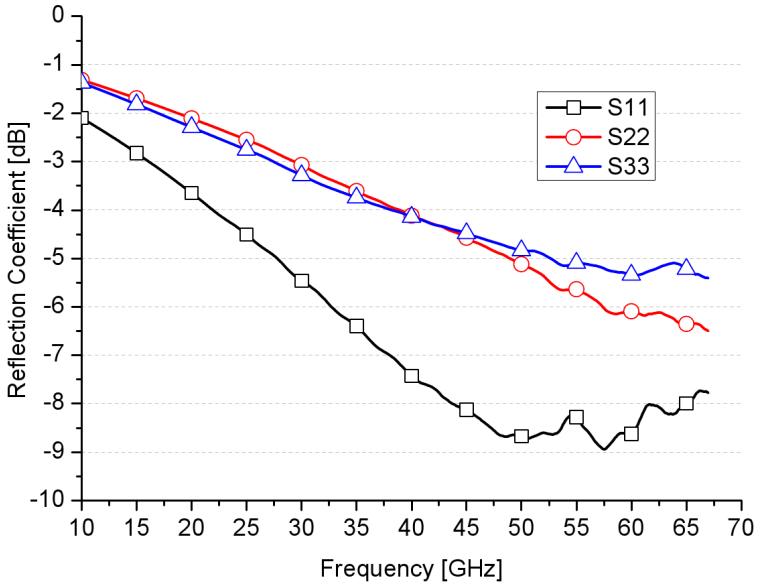

Figure 40: Balun return loss

This equation introduces the fundamental modes inside the coupler: the even and odd modes. The coupling value as shown by Equation 2.8 depends on the suitable values of even and odd impedances. In CMOS technology, a range of possible impedance values has been determined [41]. In particular, for the even mode, these values are limited by the parasitic capacitances existing between the lines and ground. A possible range of values is around 100 - 150 Ω. Due to these limits on the even mode impedance, to obtain the desired C_{Co} values for the coupler, it is necessary to optimize other parameters: the mutual capacitance C_{cm} and the mutual inductance M between the coupled lines. Following this strategy it is possible to have better control over the odd mode impedance without substantially changing the even mode impedance. $Z_{0e,e}$and $Z_{0e,o}$ can be expressed by the lumped component element model commonly used to represent a small coupled line coupler section [38]:

$$\begin{aligned} Z_{0e} &= \sqrt{\frac{L+M}{C_c}} \\ Z_{0o} &= \sqrt{\frac{L-M}{C_c+2C_{cm}}} \end{aligned} \tag{2.9}$$

Here, C_c, C_{cm}, L, and M are ground coupling capacitance, mutual coupling capacitance, inductance and mutual inductance respectively. Once that the coupled lines coupler parameters are identified and the θ length is established, it is possible to address the problem of the power splitting over the entire balun struc-

ture. Robertson [39] describes with closed formulas, based on the transmission coefficient, the power re-bounce inside the couple pair:

$$\begin{aligned} S_{21,bal} &= -TC + \frac{T^3C}{1+C^2} \\ S_{31,bal} &= TC - \frac{T^3C}{1+C^2} = -S_{21} \end{aligned} \tag{2.10}$$

T and C represent the transmitted and the coupled power into the balun (bal). To understand the function of the balun it is necessary to know the distribution and the magnitude of the principal power flow inside the structure. Considering the equation used to describe the power flow into the coupler and given the possibility to manipulate their magnitude values, it is possible to use Equation 2.6 and 2.7 in Equation 2.10. By replacing the coupling coefficient (C) with equation 2.7 and the transmission coefficient (T) with equation 2.6, it is possible to obtain this new set of equations:

$$\begin{aligned} S_{21,bal} &= -\frac{jC1\sin\theta}{T1^2\cos\theta + j\sin\theta}\frac{T1}{T1\cos\theta + j\sin\theta} + \dots \\ S_{13,bal} &= \frac{T1}{T1\cos\theta + j\sin\theta}\frac{jC1\sin\theta}{T2\cos\theta + j\sin\theta} - \dots \end{aligned} \tag{2.11}$$

where$T = \sqrt{1-C^2}$. Each coefficient of Formula 2.11 depend on the geometrical shape of the couplers on the balun. The extended formula was truncated at the first step of the approximation to give an idea of the complexity of the calculus. Therefore, the electrical length of the two couplers is different and as a result there will be two different values of θ. In the next section the sizing procedure to reach maximum power balancing with minimum losses and small component size will be explained. The optimization of the power balancing involves a trade off between other parameters such as the input return loss and the phase balancing at the differential outputs. More detail on this subject will be addressed in the measurement section.

Layout Rescaling Procedure

The synthesis of the balun starts by utilizing λ/12 for the lines' electrical length (3 time smaller than the classical configuration). Considering equations2.6 and 2.7, the lines shortening is expressed using two coefficients: 0.86 for the cos (λ/12) and 0.5 for thesin (λ/12) where the values of transmitted and coupled coefficients, therefore, are scaled by the described two factors. Figure 41 represents the proposed version of the Marchand balun. The shape is inspired by the design of [39], with the main difference being that the coupled lines length reduced to λ/12 to maximize the size reduction. The multilayer feature of the technology allows staking of the balun lines in two contiguous metal layers. The layers chosen to place the lines are metal 7 for the input line and metal 6 for the coupled lines. The reduced distance between the layers (only 600 nm) improves the mutual capacitance between the superposed lines and as a consequence the value of the coupling coefficient of equations 2.6 and 2.7. To verify the theoretical hypothesis

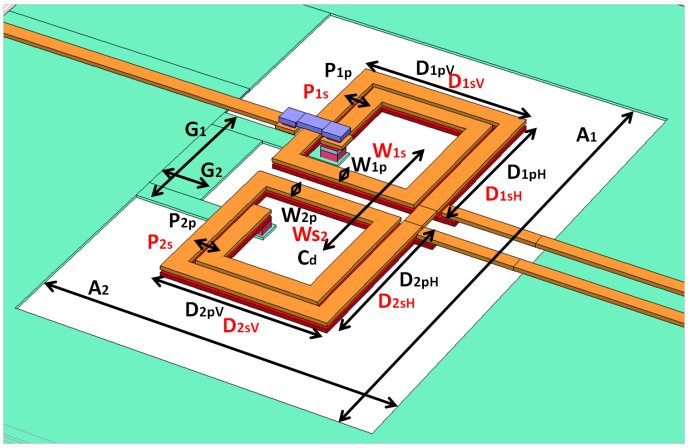

Figure 41: Layout of Balun before optimization with design variable employed

explained in the previous section of the paper the structure shown in Figure 41 is used as proof of concept design. The Marchand balun topology can be seen as two sections of coupled lines placed in series. The line length of each pair of coupled lines is $\lambda/4$ [36].

In the balun of Figure 41, the coupled lines are folded and stacked to shrink the total occupied area. The upper metal (on level 7) constitutes the primary lines for both couplers and is connected in just one continuous line. Both the secondary lines of the two couplers are placed below the primary lines. The simulation tool exploited for the structure analysis is Sonnet V12.52. The first simulation of the balun shows an output power imbalance of 1.5 dB and around 6 degree of phase shift between the differential ports. This result far from those Marchand balun is not unforeseen. In the classical configuration, the use of two identical couplers to build the structure of the Marchand balun is sufficient to assure an equal power distribution upon the differential outputs; at the contrary in this work the shortening of the lines causes a variation in the value of the coupled coefficient C in Equation 2.7. The $\sin(\lambda/12) = 0.5 = 0.5$ in the numerator of equation results in a 2 fold reduction of the coupling factor. In contrast to the reduction of the coupling coefficient caused by the shortening of the lines, the growth of the mutual capacitance between the lines due to the stacking of the conductors causes a partial rebalancing of the coupled power C.

The equations in 2.11 describe with more efficacy the different contributions yielded by each power flow inside the coupler. A change of the geometry of the coupled lines in both of couplers is needed in order to balance with high precision the power level at the output of the differential port. This strategy represents the only way to allow the use of shorter lines in place of $\lambda/4$ couplers into the balun to assure equal power output values. This constitutes the principal novelty proposed in this paper. As previously explained, each coupled line coupler is modeled by electrical modes that depend on the electric parameters summarized in Equation 2.9. The variation of the size in terms of line width and line length

changes the impedance of even and odd modes and consequently the coupled and transmitted power is adjusted at the output ports. The rolled up structure imposes a series of other parameter constraints in the tuning of balun lines. The line length (L_l) of each coupler block can be changed by the diameter of the coils represented by $D_{I,V}$ and $D_{j,H}$. Furthermore, the windings like the classic inductor are described by a set of parameters: the line pitch $P_{i,i}$ or the distance between the lines and ground. Displayed in Figure 41 are the sets of exploitable variables which allow the tuning of the entire balun. They can be classified in terms of line width, line length, coil emplacement and structure distance to the ground. Table 2 describes each parameter and the value obtained at the end of the optimization run whereas Figure 42 shows the final result of the optimization procedure.

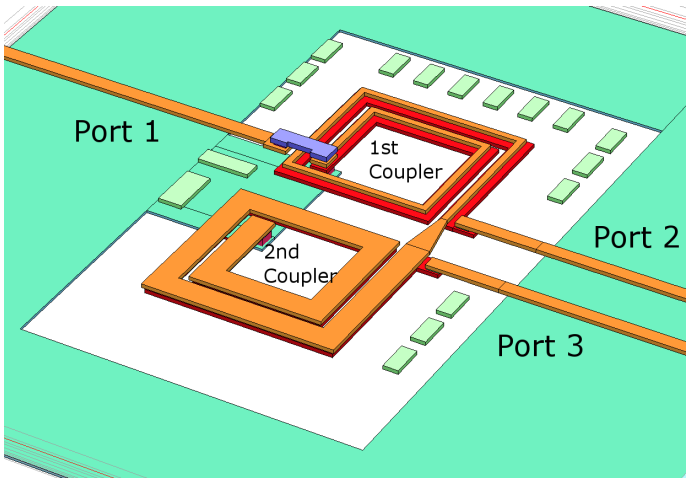

Figure 42: Final shape of Balun after the optimization run.

The free ground area around the balun and the ground plane are described by the A and G parameters respectively. The shape of the ground plane around the coupler has a great influence on the component response. The confinement of the magnetic field around the component is a very critical point of study. The eddy currents generated by the proximity effect between the lines and the ground cage reduce the total magnetic field around the windings. In addition, the capacitive coupling effect with the ground changes the mode impedance for the even and odd mode across the C_c parameter of Equation 2.9. In the other hand a too wide spacing between the ground and the balun increase the losses within the low resistivity substrate and causes an inductive degeneration effect inside the ground contact for the secondary lines of the coupler. The sizing of the ground contact, in fact, is a tradeoff between the parasitic capacitive coupling with the lines and the parasitic inductance generated by the metal line. This inductive effect on the ground contact, that shows an estimated value of 10-15 pH, has strong effect on the balun. The undesired inductance together with the line resistance on the ground contact changes the ideal behavior of the coupler. To reduce the parasitic effects, the ground contact placed on metals 1 and 2 must be enlarged. In this

Variable	Name	Value [μm]
D_{1pV}	Vertical diameter 1^{st}, coupler 1	39.5
D_{1sV}	Vertical diameter 2^{nd}, coupler 1	42.5
D_{1pH}	Horizontal diameter 1^{st}, coupler 1	33
D_{1sH}	Horizontal diameter 2^{nd}, coupler 1	36
D_{2pV}	Vertical diameter 1^{st}, coupler 2	39
D_{2sV}	Vertical diameter 2^{nd}, coupler 2	38
D_{2pH}	Horizontal diameter 1^{st}, coupler 2	45
D_{2sH}	Horizontal diameter 2^{nd}, coupler 2	44
P_{1p}	Coil pitch 1^{st}, coupler 1	5.5
P_{1s}	Coil pitch 2^{nd}, coupler 1	5.5
P_{2p}	Coil pitch primary, coupler 2	7
P_{2s}	Coil pitch 2^{nd}, coupler 2	7
W_{1p}	Line width primary, coupler 1	1
W_{1s}	Line width 2^{nd}, coupler 1	4
W_{2p}	Line width primary, coupler 2	5.5
W_{2s}	Line width 2^{nd}, coupler 2	4
C_d	Pitch between coils	48.5
G_1	Ground width	33
G_2	Ground Length	29
A_1	Free Area 1	128
A_2	Free Area 2	79.5

Table 2: Variables employed during optimization run. $1^{st}$is for primary coil and $2^{nd}$for the secondary one.

case the inductance effect is attenuated reducing the imbalance at the output and thus the input matching as well. In order to assure a small difference in the impedance value between the balanced ports, simulation suggests that the width of the secondary coupled lines must be the same therefore the lines size W_{1s} and W_{2s} must be identical. Concerning the remaining parameters the size limitation is dictated by the global shape of the structure and the compliance with the design rules. Another fundamental aspect considered during the simulation process is the presence of the dummy metal brick around the structure. Dummy metals, in particular for metal 7 (M7) and M6 are mandatory to meet the minimum metal density requirements imposed by design rules. Simulations demonstrate the influence of the dummy metal on the EM field around the balun. As a consequence careful consideration must be taken during the optimization process. The bricks represented around the balun in Figure 42 are dummy metals placed on the realized component.

Simulation and Measurements

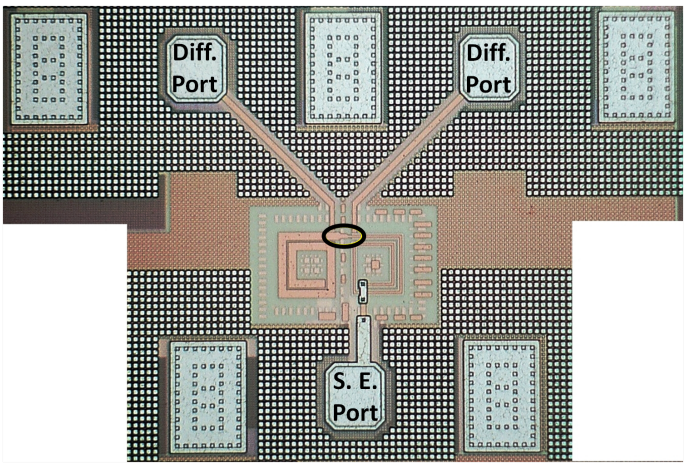

Figure 43: Test chip for the Marchand balun

The measurement campaign of balun was done using an Agilent N5247A PNA-X with 4 ports. Figure 43 shows the test bench die realized for the measurement campaign. Figure 44 shows the transmission parameters S_{21} and S_{31} compared to simulations. The maximum insertion loss for the balun is 1.5dB at 67 GHz with the port matched by on 50 Ω loads.

Measurements confirm the reliability of the simulator software and as a consequence the good behavior of the balun. The main differences among simulations and measurements are the 0.4 dB of imbalance between the differential ports and a small drop in the total transmitted power in the 60-67 GHz band as reported in Figure 44.

These differences between simulations and measurements have been investigated. The amplitude difference has been attributed to an underestimated

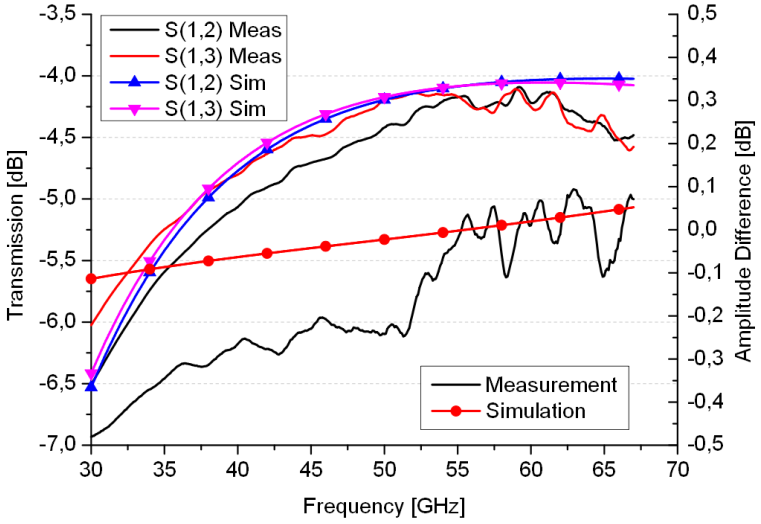

Figure 44: Transmission parameters for the balun

coupling factor among the balun with the M1 - M5 dummies. The increase of losses at 60 GHz can be attributed to the skin effect on the lines. To simulate with accuracy this effect an internal metal meshing is adopted. In Sonnet it is possible to describe each metal line with a thick metal model. The thick metal model is defined with a minimum of two levels (top and bottom of the thick metal layer) or even with a number of intermediate cutting planes. The number of these planes depends on the memory and matrix solving time available. The rise of the planes number increase rapidly the requested memory and the elaboration time. In the presented balun six level of internal mesh for each metal layer have been used.

With this simulations set up the mismatch remains limited by fractions of a dB and the performance of the components shows to be highly promising. The power difference in the balanced ports, does not exceed 0.1 dB in the entire band of interest. This result exhibit the state of the art performance in terms of amplitude balance. Figure 45, shows the phase difference between the differential ports. The phase shift is due to two factors: the first one is the tradeoff to reach a minimum amplitude difference between the ports. Optimization processes show that the amplitude and phase imbalance are correlated as explained before. In this case it has been chosen to push the design towards perfect amplitude balance; however, part of phase shift can be compensated by sacrificing power balancing. The second tradeoff concerns the connection between the coupler pairs (highlighted in Figure 43). The length of the line depends on the pitch of the coupler described in Figure 41. The spacing between the coupler determines the quality of impedance matching on the single ended port. A minimum distance between the coupler pairs must be guaranteed to avoid interferences among the lines. After the optimization process, a line of 11 µm length is used to connect the couplers. The phase difference between the differential ports changes linearly

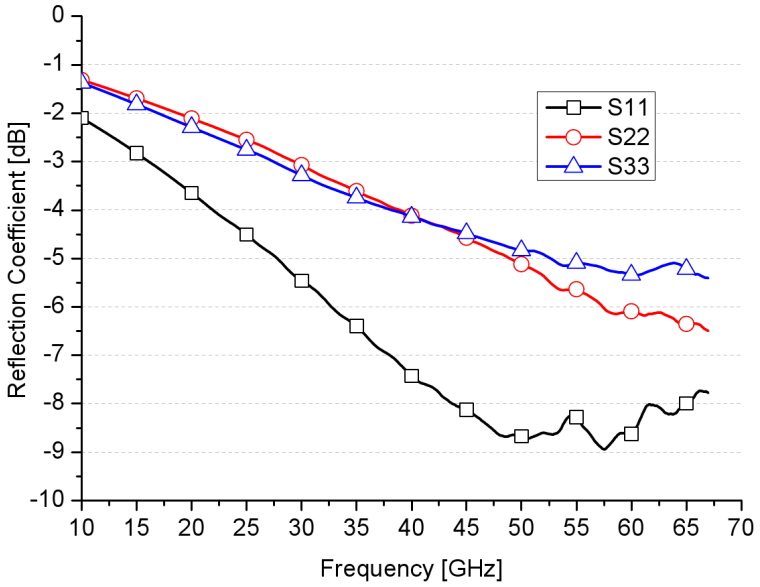

Figure 45: Phase difference at balanced ports

with frequency. This is a typical behavior of "true delay lines" (TDL) and, as a consequence, the phase delay could be recovered using a TDL at the output of Port 3. Simulation show how, with a 45 µm of TDL, the phase shift is reduced to zero. This line require space but it can be employed also to separate the output port which is extremely close.

Figure 46 shows the reflection coefficient of the balun where for the single ended port, the 50 Ω matching is better than 12.5 dB in the whole band of interest. Regarding the peak of the reflection coefficient, the best matching point is not centred at 60 GHz. This is caused by the tradeoff needed to minimize the power imbalance. The reflection coefficients for the differential ports are instead far from the 50 Ω matching. The response at the output port highlight an inductive effect. This is due to the short circuit at the end of the coupled lines. The shortening of the coupler that constitute the balun changes the impedance seen at the output port showing a strong inductive part. The 50 Ω matching could be implemented by a 57 fF series capacitor at the output of the differential port. With the proposed matching network, however, the impedance of secondary lines of both coupled line couplers is changed and the response of the balun is highly distorted. The solution proposed to overcome the balun output mismatch problem is the design of an active block (a buffer for instance) that it maintains the 50 Ω as input impedance but at the same time does not suffer from inductive effect shown by the differential ports of the balun. Using this strategy, the performance of the balun remains unchanged and the system does not suffer from mismatch of the ports.

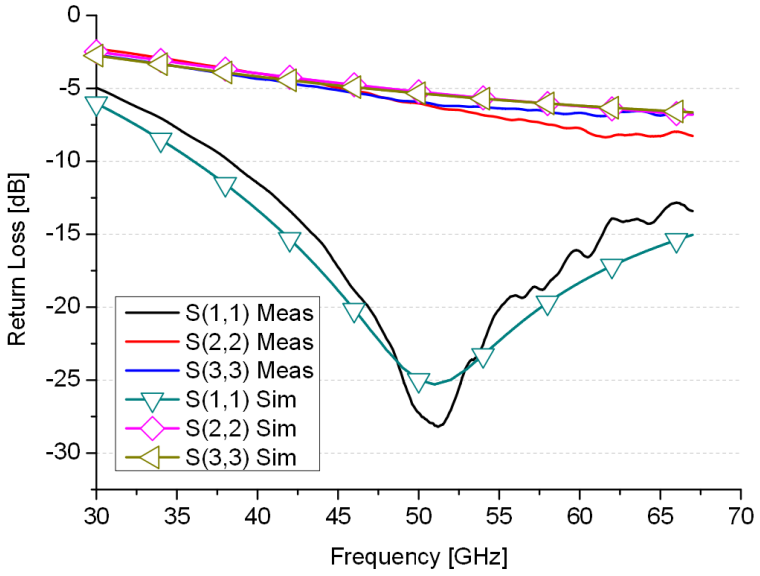

Figure 46: Reflection coefficient of Marchand balun

2.3.3 *Conclusion*

The research on the reduced size balun has lead to the synthesis of two new shapes of baluns. The mathematical models developed to describe the interaction between the superposed spirals had allowed obtaining a higher control on the power flows inside the structure. As a consequence, a faster optimization procedure is possible with final results that overcome the state of the art under different points. Table 3 summarizes the most representing baluns proposed in the state of the art. Concerning the occupied area the discussed baluns represent the reference on the literature, in addition, the last developed version of transformer balun, not characterized in a stand-alone chip but exploited in the transmitter chain 5.1.1, exhibits 0.0071 mm^2 of occupied area (99×72 µm instead of the 132×85 µm of the characterized one). The measurement campaign confirms the high quality of design flow and the developed model as well. The low insertion loss (only 2 dB for the transformer version and 1.5 for the Marchand version), and the very good amplitude balance (better than 0.1 / 0.2 dB in the whole of interest band) confirm the very high performances of these structures.

Table 3: State of the art for millimeter-wave Baluns

Ref.	Tech.	Band [GHz]	IL [dB]	RL [dB]	A.I.* [dB]	P.I.* [Deg]	Area [mm^2]
Trans. Balun [9]	65nm	**57-63**	**2**	**8**	**0.2**	**6**	**0.01**
March. Balun [10]	65nm	**57-63**	**1.5**	**12**	**0.1**	**8**	**0.01**
[40]	180nm	25-65	3.4	10	1.5	±10	0.55
[42]		57-63	4	7	N.A.	N.A.	0.01
[43]	GaAs	14-28	1.5	15	1	±10	0.26
[44]	90 nm	20-26	2	N.A.	0.5	5	0.05
[45]	130nm	50-65	3	N.A.	3	5	0.05
[46]	180nm	20-70	1	N.A.	1	5	0.06
[47]	InGaP GaAs	15-45	1.5	13	1	5.5	0.40
[41]	180nm	18-32	0.8	12	1	5	0.07
[48]	180nm	27-54	1.1	15	1	5	0.06

2.4 LANGE COUPLER

The different 90° hybrid couplers the Lange's version is the best compromise between high radio frequency (RF) performances and small component dimension. The coupler was proposed for the first time in 1969 by J. Lange [49]. It is composed by 4 interdigitated lines of $\lambda/4$ of length, which are respectively interconnected by pairs with bond wires or bridges. The Lange's architecture is preferred to other topologies, like rat-race [50] or branch line coupler [51, 52], for different reasons, and, in particular, for the available bandwidth and for the phase difference stability between the transmitted and the coupled signal, that are the most important required electromagnetic features. The shape of the device, also, is a great advantage over the other technological solutions. In fact all the different couplers cited before base their functioning on their lines dimensions ($\lambda/4$). Due to their particular construction, the branch-line and the rat-race architectures have a shape factor (W/L) approximately equals to 1, whereas the Lange coupler shows a $W/L \ll 1$. This property is a great advantage for the Lange because their geometric linearity permits the use of meandering techniques to shrinks the total

area of the component [53]. Another benefit arriving from the meandered solution is the placement of the output connections. In all of the coupler structures the outputs are placed in the opposite points of the component, this meaning that for highly symmetrical circuits, as I/Q receiver or transmitter, the distance between the outputs can represent an issue. On the other hand, the meandering structure refolds the coupler's line and approaches their ports resulting in more compact solution. The principal improvements shown by the component proposed in this paper are the enhancement of the input/output impedance matching, the reduction of the insertion loss, and the raise of the isolation value for the 4th port of the coupler. The technique employed to design the component minimizing the silicon surface area is inspired by [53]and use meandering technique. Although the two coupler topologies seem very similar, they share just the meandering property of the lines and they differ in two essential design features (see Figure 47) for a representation of proposed coupler design. The first remarkable difference is that the proposed structure allows the use of the short circuit in the middle of the lines, thus permitting the port 2 to be located diagonally opposed to port 1 (as in the classical design of the Lange coupler). This is a great advantage for the placement of the remaining part of the circuitry around the coupler because the distance from port 2 and 3 are exactly the same (Figure 47). Furthermore, simulations have shown an improvement in the coupling factor and in the bandwidth if the lines of port 3-4 are also shunted. The second difference is in the lines width and in the lines spacing of the Lange coupler. The state of the art performances of the hybrid ring are $-15 \div -18.6$ dB for the return loss, while from -12 up to -21 dB for the S_{41} isolation. For the component proposed in this paper the tuning of the lines thickness and their interspacing has allowed a significant increasing in the quality of the circuit response. The different impedance in the coupler lines yields a perfect tradeoff between the coupling factor and the impedance of the lines. Both the presence of the junction in the middle of the coupler and the tuning of the lines thickness allow obtaining a good value of isolation at port 4.

Design procedure of Lange coupler

The procedure to design a 90° power splitter is very simple and can be described in five steps.

- Size: the nominal value of the central frequency and the properties of the substrate determine the value of the wavelength and then the dimensions of the device.
- Number of lines: classical Lange coupler is constitued by 4 parallel lines of which three entire an one segmented in 2 parts. The other Lange couplers proposed in literature use more lines to improve the coupling but the geometric complexity increases.

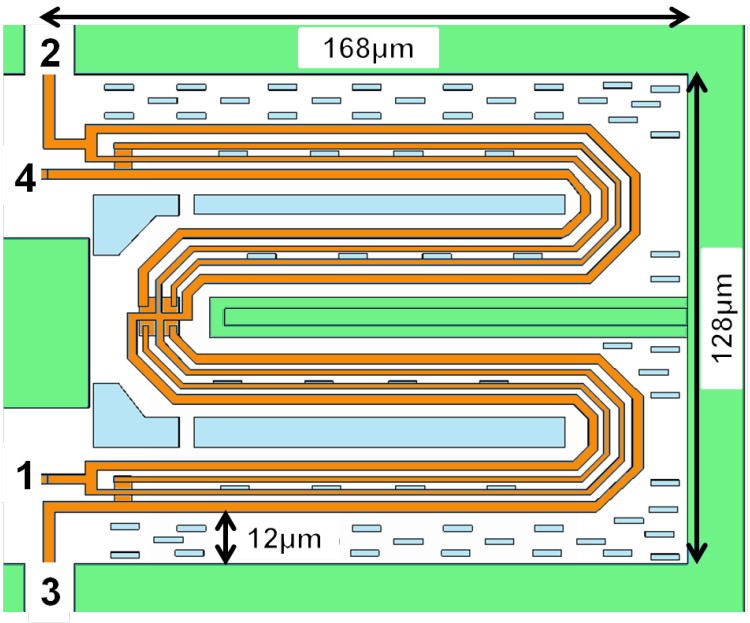

Figure 47: Figure 1. Structure of the proposed coupler

- Shape: meandering procedure is optional. It is normally used when the requirement of the occupied area reduction is a strict constraint or when the placement of the I/O ports must satisfy a particular shapes.
- Interconnections: a short circuit at the middle of the lines improves the EM response. This can be easily done by means of the CMOS multilayer structure that, at the contrary of the other tecnologies, offers the opportunity to yield simple and effective bridges using arrays of via holes and lower or upper metal layers.
- Ground: the coupler must be counturned by a cage of ground to reduce the dispersion of the electromagnetic field and to minimize the interactions with the other possibles inductors or lines placed in the neighbor of the coupler. If the coupler use meanders to reduce its sizes it is prefereable the placing of ground wall among the meanders to reduce the possible cross-talk of the lines.

The work presented in these pages has a central frequency of 60 GHz and it is placed on silicon CMOS bulk substrate. To compact the shape of the coupler a "W" form is used as suggested in [53]. To reduce the curve sharpness smoothing the folding of the lines 45° line segments are used in this work. This procedure reduces the concentration of the currents at the corners and improves the propagation of the signals. The short circuit in the middle of the coupler is very easy to be achieved. For the primary line (transmitted signal: connection between port 1 and port 2) a metal strip is added perpendicularly to the sense of propagation

of the signal. For the secondary lines, (coupled signal: connection between port 3 and port 4), four arrays of vias connect the lines with a square placed at the lower level. The lines width to start the simulation stage is fixed at 2.5μm. The distance between external lines of the coupler and the ground cage is established to be 12μm. This value has been chosen in reason of previous experiences into passive component simulation in 60 GHz devices [8]. The same distance is used to separate the coupler's meanders before and after the central junction. Instead, a thin ground wall is placed in the middle of the central meander to reduce the interactions among the different groups of lines.

The first step in the Lange coupler optimization is the tuning of the central frequency in order to satisfy design requirements. The characteristic response of the Lange permits to identify the minimum distance between the transmitted and the coupled powers even if the two coefficients are not still correctly tuned. Employing a length of 610μm (λ/4) for the lines, the response of the component is shifted at lower frequency. This effect is attributed to a lightly interaction among the lines of different sections of the coupler. In order to avoid the insertion of other ground walls, the length of the four groups of line in Figure 47 has been reduced.

The tuning of line width, instead, is the second and last design steps. The correct coupling/transmitting values and the port impedances as well depend on the lines width. The equations shown in [53]for the even and odd modes provide an estimation of the size of the lines. The pair of lines that constitutes each one of the two branches of the coupler yields a total width of 5μm.

The simulation result of the previous explained set up for the structure show two important data. First, the input impedances at the 4 ports are lower than 50 Ω. Second, the coupling (C) is too high compared to the transmission value (T). The solution proposed to solve both these problems is a change in the geometry of the coupled lines. Concerning the impedance issue the reduction of the lines section will fix it, while, for the equilibration of the output power flows, the solution requires further investigations.

A simulation including the currents estimation is performed in order to understand how the charges flow through the structure. To evaluate the phenomenon a full wave simulation using CST Microwave Studio has been executed. The simulation results highlight a higher concentration of the currents in the internal lines of the coupler, as theoretically expected. As a consequence also the electromagnetic fields are more intense in the core of the lines.

The solution found to solve at the same time the impedance compensation and the power flow distribution consists in the resizing of the two internal lines of the Lange coupler. The section of the four lines, previously fixed at 2.5μm, is reduced during the optimization process until 1.5μm. The thinning of the lines increases the characteristic impedance of the component improving the 50 Ω matching at the I/O ports. The effect of this impedance growth imposes on the electromagnetic field a redistribution of the current into the external lines, which

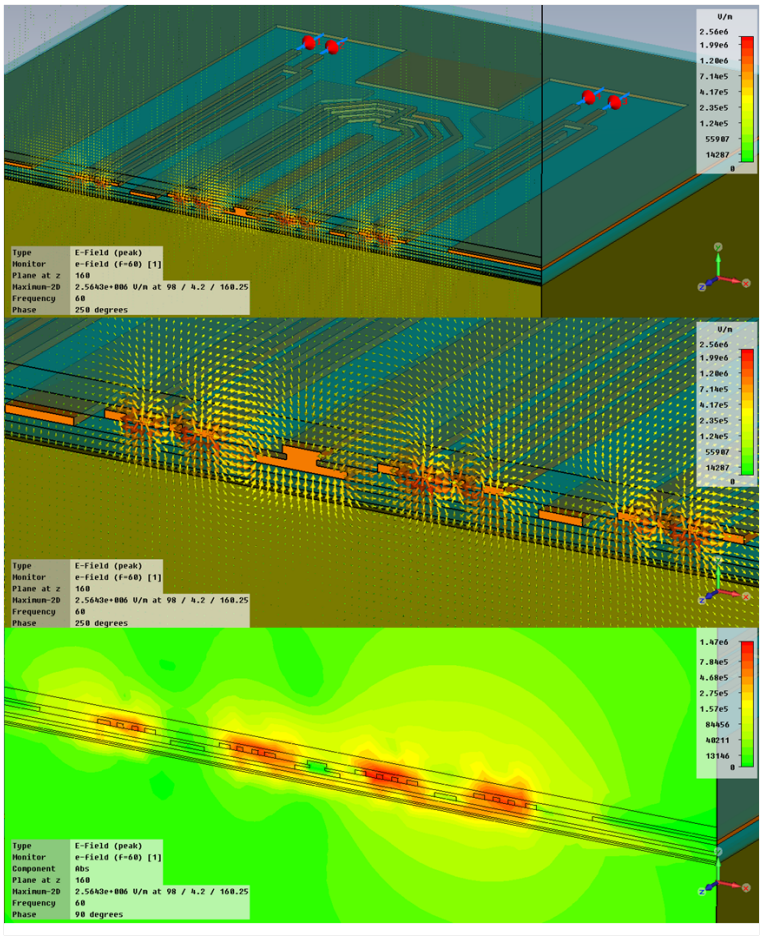

Figure 48: Figure 2. Electromagnetic field among the lines simulated by CST

are at lower impedance. The reallocation of the charges decreases the EM field and the coupling effect as well. The final result is a rebalancing of the power flows between C and T coefficients. Figure 48 shows the final distribution of the field in the optimized structure.

The final shape of Lange coupler occupies a surface of $128 \times 168\,\mu m^2$ including the empty area around the lines. To satisfy the strict rules on the metals concentration; dummy metals are inserted and their effect is considerate during the simulation runs. Figure 49 shows the eddy currents on the floating metal brick placed around the coupler. The presence of dummy metal changes the response of the structure, and the principal effects remarked during the simulation and confirmed by measurements are the reduction of the total magnetic field and the rising of losses. To solve the first issue a tuning of the distance among the lines is sufficient to compensate the floating metal brick presence. Concerning the losses, instead, a smart placement of the elements around the structure reduces the interaction with the EM field of the coupler.

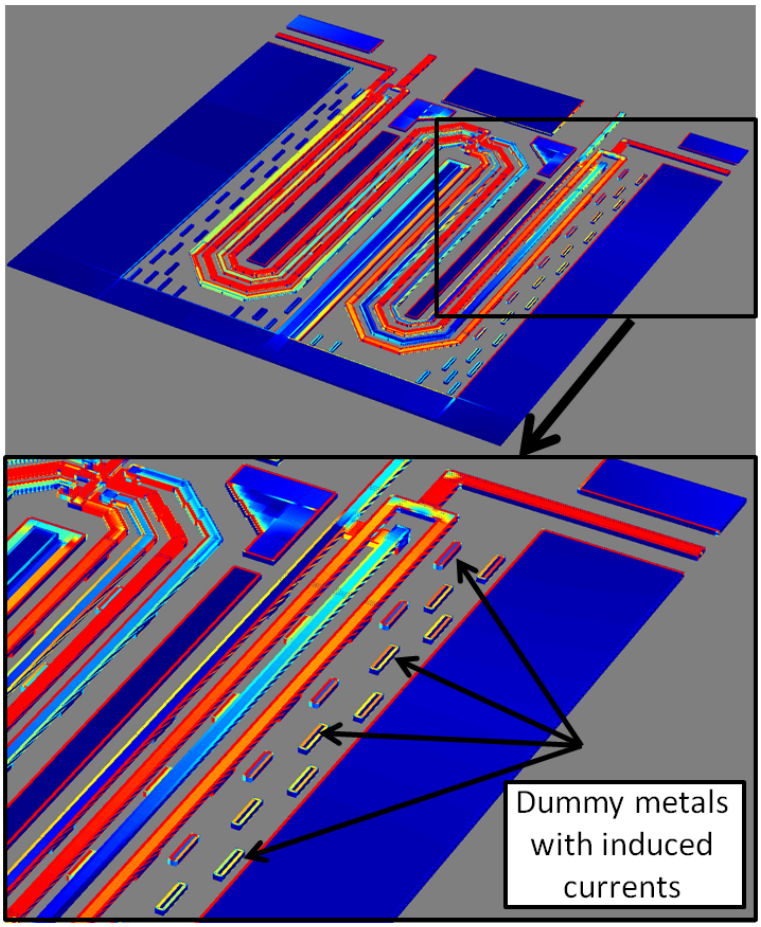

Figure 49: Current concentration on the lines and eddy current on the dummy metals

Simulation and measurements

The Lange coupler is realized in a standalone block Figure 50 to measure and verify the hypothesis shown in the previous section. The measurement setup is able to cover the band of 40 MHz – 67 GHz with a N5247A PNA-X 4 port VNA by Agilent. Due to the number of ports needed for the measure, the setup has been simplified by the employment of G-S-G-S-G 50 Ω probes in the place of classical G-S-G probes. Concerning the layout, these probes impose a rigid placement of the pads. To assure the minimum phase shift among the different ports, interconnection lines with identical electric length must be designed. Grounded coplanar wave guides (CPWG) are expressly developed for this task. The simulations of the lines assure identic phase shift for all of the ports.

The measurement campaign shows good fitting between simulations and real behavior.

Figure 51 and represents simulated values until 120 GHz in order to show the complete response of the Lange coupler, while the de-embedded measurements

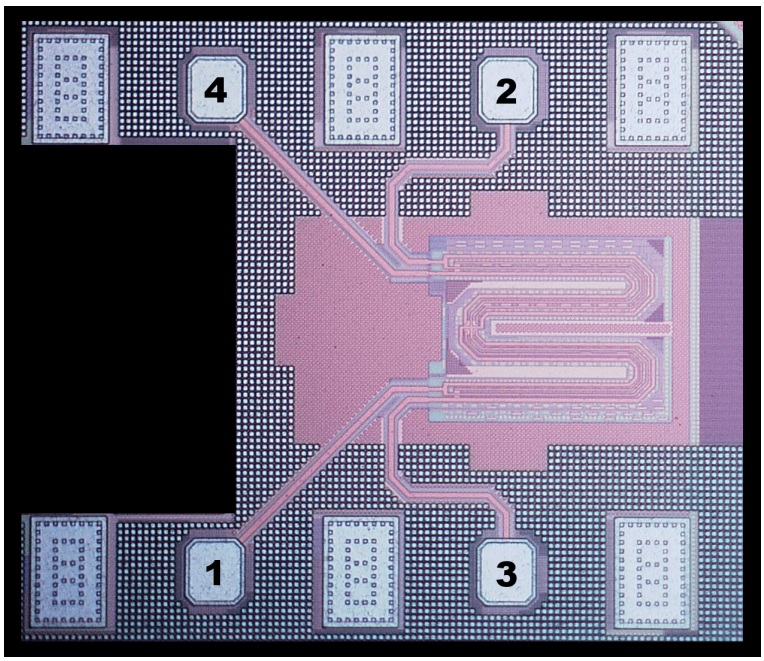

Figure 50: Realized Lange Component

are stopped at 67 GHz. Comparing the simulation with the real response of component, a small difference at the coupled port is remarkable as shown in Figure 52. This is probably due to the overestimation of the coupling factor simulated by the software. A redesign of the structure that considers this effect is sufficient to re-equilibrate the transmitted and coupled values into the component.

In Figure 53 the phase shift between the output ports is showed. The curve highlight a difference of 7÷10° compared to the desired behavior. A valid explication to justify the mismatch is not still found, however a countermeasure to recover the phase delay is proposed. In order to reach the quadrature of the signal a capacitance is placed in the transmitted output of the coupler. Figure 53 shows the behavior of the phase difference at the output ports obtained with the presence of a 160 fF capacitor placed in series to the port 2. Concerning the reflection coefficient, reported in Figure and the isolation between port 1 and 4, measurements show an improvement of the performances compared to the simulated results. This is probably due to the underestimated losses of the structure caused by metal roughness. This hypothesis is also confirmed by the increased value of the insertion loss. The difference between simulated results and measurements reaches the values of 0.5dB in the worst case. The proposed Lange coupler covers about 20 GHz around the central frequency of 60 GHz. The maximum insertion loss in this band is 1.2 dB, the return loss at the four ports remain lower than 23 dB in the whole band of interest. The isolation at port 4 is better than 22 dB. These results place the designed component in the state of the

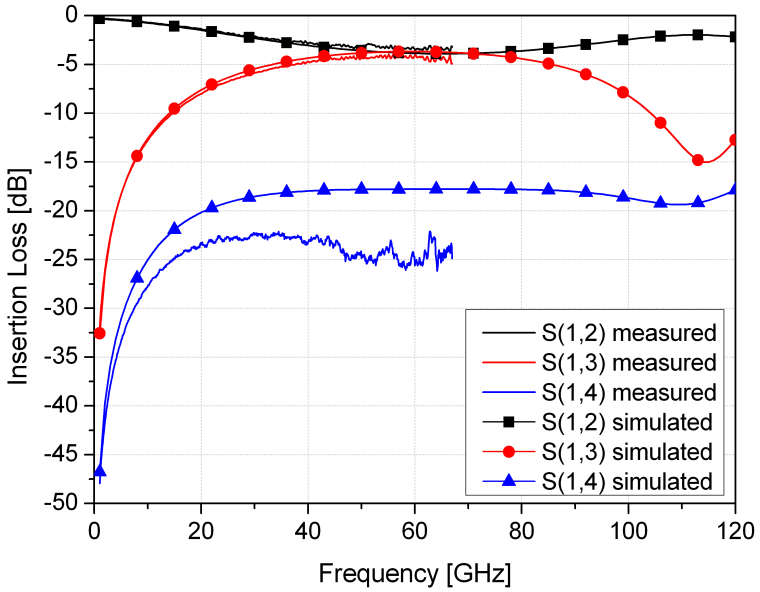

Figure 51: Transmission Coefficient

art compared to the other architecture of hybrid coupler/splitter. It yields better return loss, insertion loss, and isolation maintaining reduced dimensions.

2.4.1 *Conclusion*

In the previous pages novel method to optimize a Lange coupler is presented. The procedure is based on the tuning of coupled line thickness. The change in the impedance line permits to equilibrate with higher efficacy the power flow at the output ports and the impedance value of the structure as well. Full wave simulations done to verify the intensity of EM field and to investigate the current density into the coupler lines have contributed to understand the field propagation allowing a more effective synthesis of the final component. The measurement campaign, finally, confirms the reliability of the design procedure. The coupler shows low losses with a very high isolation coefficient between port 1 and 4. The return loss values are also very good with values that remaining lower than -20 dB in the whole of measurement band. The total size of component is very attractive with only 128×168 µm of total occupied area including grounded walls to confine the EM fiend.

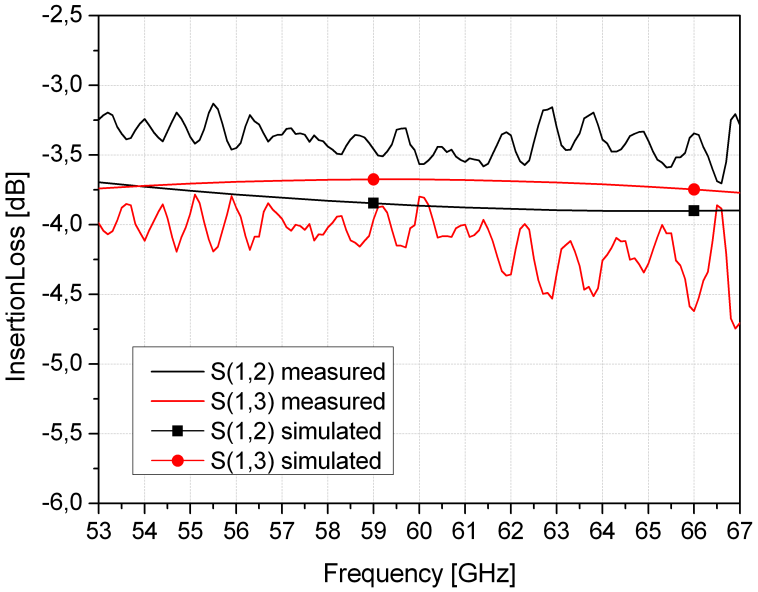

Figure 52: Transmission Coefficients in 60 GHz band

2.5 WILKINSON POWER SPLITTER

Introduction

The Wilkinson power splitter/combiner is a passive circuit constituted by very simple architecture. It is composed by three ports: two of them are interconnected by a 100 Ω resistor and they allow obtaining the split of the signal injected at the third port or even the sum of theirs input signal to send at the third port as well. The phase and the amplitude equilibrium between the two output ports are assured by the symmetry of the structure. The most attractive feature shown by the Wilkinson splitter/combiner is the reciprocal high isolation between the ports interconnected by the resistor. This characteristic represents the greater advantage of the Wilkinson splitter compared on the other typologies of dividers (combiners). Assuming that an undesired variation on the traveling signal occurs at one of the ports' pairs a part of the signal could be reflected. This phenomenon takes place when the devices connected show different impedance values (as instance unexpected different load for elements into an antenna array). The reflected wave returns back inside the Wilkinson device and it tries to propagate it through the other two ports. At this moment the resistance placed between the two ports executes its task killing the parasitic signal by resistive power dissipation. This response is made possible by the geometric length of the two output ports of the splitter combiner. At the central frequency, the two branches assume an electrical length of $\lambda/4$. The undesired signal, reflected by one of these two ports, comes back and travels the other line with a total distance of $\lambda/2$. At this point the two

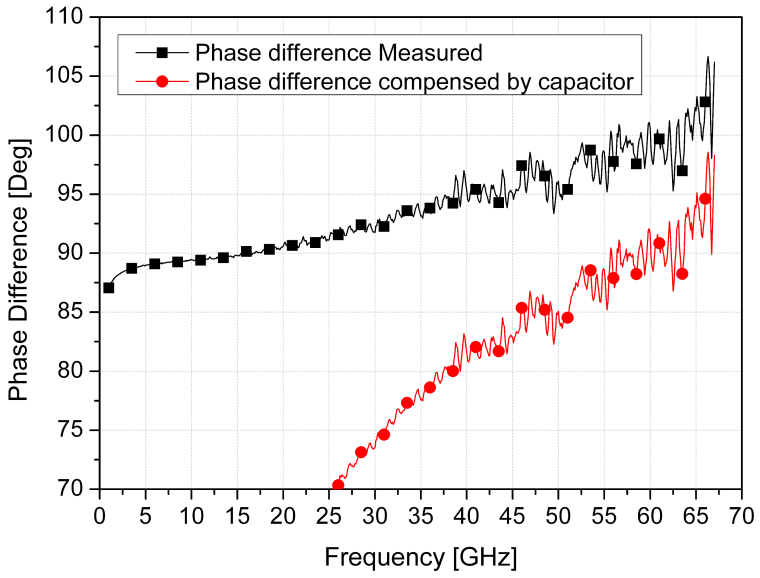

Figure 53: Phase difference for quadrature ports

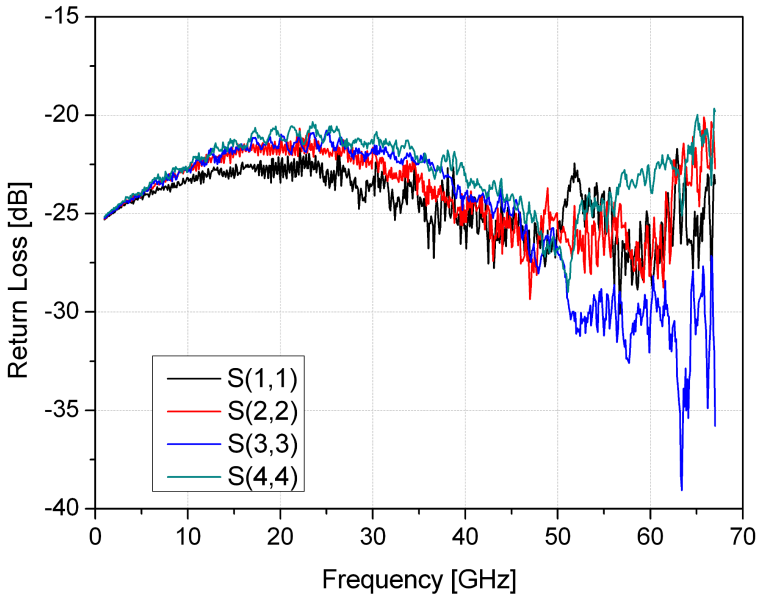

Figure 54: Return loss of Lange Coupler

signals are in counter phase at the middle of the resistor R. The resistivity of the component dissipates the undesired wave blocking hence the propagation.

Size considerations

The passive components, like power combiners/dividers, hybrid couplers, transformers and baluns are responsible of cumbersome chip area occupation. In [54] is presented a power amplifier in 90 nm CMOS technology for 60 GHz applications. The area dedicated to the Wilkinson power splitters is $536 \times 150\,\mu m^2$ for the dividers and $305 \times 294\,\mu m^2$ for the combiners. In [55] a 60 GHz receiver is presented and the power splitter occupies $430 \times 360\,\mu m^2$ (estimated values) which is 11% of the total circuit area. In [56], 60 GHz splitter and 90 coupler are reported. The two passive components occupy almost 50% of the total I/Q demodulator area. These examples are a clear evidence of the impact that passive components have on the overall chip size at different working frequencies (λ). Hence the motivations behind this work where a dramatic size reduction of a power divider has been achieved with a dedicated design optimization procedure and validated with experimental data. Owing to its high port isolation, Wilkinson architecture has been chosen as the reference design while size reduction and improved RF performances were at stake [54].

In the Wilkinson power splitter the length of the lines determines the working frequency. The simpler configuration of the divider is represented by 2 lines of $\lambda/4$ length with characteristic impedance of $Z = \sqrt{2} \times Z_0$. Z_0 is the input and output 50 Ω impedance. As described above in CMOS technology $\lambda/4$ corresponds at 650 μm. The use of devices with these dimensions in radio frequency integrated circuit could be prohibitive or even incompatible with the rest of the integrated circuit. Meandered solutions are exploited in [56] to reduce the total area however phenomena of parasitic coupling and substrate losses degrade the component behavior in terms of insertion loss and input matching. A lumped component solution is proposed to overcome the problem. The key to reduce the dimension is to transform the $\lambda/4$ lines in equivalent a Π-type circuit made of inductors and capacitors. This transformation yields a strong reduction of the dimension as will be demonstrated in the following.

Lumped component representation

Previous similar works have proposed the design of 4 way splitter using lumped elements [57]. The present work has extended this approach to ultra wide band applications by maintaining superior RF performances. Π or L-type lumped element circuits can reproduce any arbitrary line behavior independently from their impedance or length. In this work, Π-type configuration is used to represent

$\lambda/4$ lines of the splitter. The matrix admittance of a line with electrical length of θ is:

$$Y_{Line} = \frac{-jY_0}{\sin\theta}\begin{bmatrix} \cos\theta & -1 \\ -1 & \cos\theta \end{bmatrix} \tag{2.12}$$

Using ABCD matrix and considering a central frequency $f_0 = 60$ GHz and a line impedance of Z, the admittance matrix results:

$$Y_{Line} = \frac{1}{-j\omega L}\begin{bmatrix} 1-\omega^2 LC & -1 \\ -1 & 1-\omega^2 LC \end{bmatrix} \tag{2.13}$$

In the matrix 2.13 it is possible to find L and C that correspond respectively at series inductance and shunt capacitance for the lumped component representation. ω represents the 60 GHz central frequency in rad/s. The extraction of the lumped component value from this matrix is simple. The equations to extract values are reported here with the calculated values for $Z = 50\sqrt{2} = 70.71\Omega$ and $f_0 = 60$ GHz:

$$L_{\sqrt{2}Z_0} = \frac{Z}{2\pi f_0} = 187.5pH \tag{2.14}$$

and

$$C_{\sqrt{2}Z_0} = \frac{1}{Z2\pi f_0} = 37.5fF \tag{2.15}$$

It is important to highlight that the obtained values are extracted considering each component as ideal and independent. In the reality this is not true and a refining of the L and C values must be done by means of full-wave electromagnetic modeling. In the next paragraphs a discussion on the performances of each lumped component will be discussed. The purpose is to understand the interaction mechanisms and compensate them.

2.5.1 *Synthesis of the splitter*

To proceed on the splitter design the first components to be developed are the inductors. Using the value obtained from Equation 2.14 a 187 pH inductor is designed and simulated. In order to extract the electrical behavior of the structure a circuital representation has been simulated with Agilent ADS. Being the capacitors well characterized in the design kit they are reproduced with ideal components characterized by small series resistances. The inductors are represented through the full-wave simulated scattering parameters as top immage in Figure 55 shows . At this point of the synthesis the model does not yet account for important factor such as the coupling mechanisms due to surrounding elements as for instance the dummies metal, between the two inductor coils. Starting

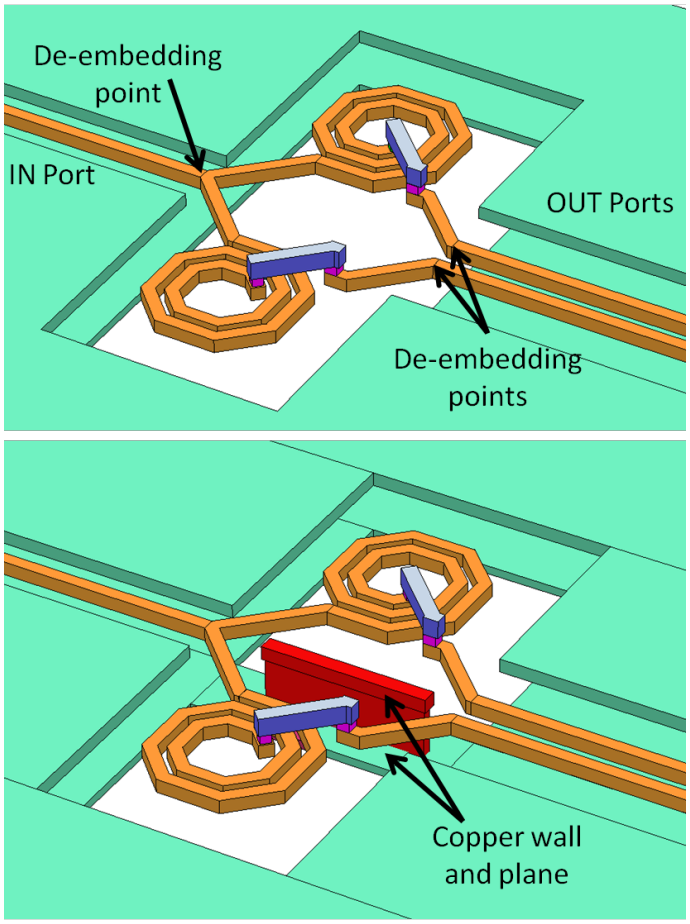

Figure 55: Spiral Inductors: Simulation of grounded separation wall

from these considerations a first improvement is carried out by introducing a copper wall between the coils to mitigate the mutual inductance and secondly to maintain the control on the undesired interaction (as shown at bottom of Figure 55). Based on this topology a global optimization based on a single full wave simulation of the three ports network is done to account for the actual structure adjustment and include all coupling mechanisms. As result of this simulation the values of the inductors are reduced and the final values are fixed at 155 pH. Concerning the shunt capacitance of 37.5 fF of Equation 2.15 their need to be reduced being compensated by the parasitic shunt capacitances of the inductors. For the output ports the effects of the inductor parasitic capacitances is too strong to reproduce the designed value and are therefore omitted. On the contrary at the input the parasitic effect reduces the capacitor value to 38.2 fF, instead of the originally designed 75 fF (i.e. 37.5×2). The optimization procedure has yielded a power splitter with excellent matching and low losses performances. However the peculiarity that distinguishes the Wilkinson divider from the other power splitter is the high isolation value between the output ports. To reach this objective in a

classical configuration a 100 Ω shunt resistor is placed at the end of λ/4 lines. In the proposed lumped element representation the only resistor is not sufficient to guarantee high level of isolation. The reason again has to be ascribed to the inductors. In fact the copper wall, placed at the middle of circuit, is not sufficient to avoid the coupling and to cancel the mutual inductance between the coils. In order to alleviate and cancel this effect a capacitor C_s is used on the resistive branch. The role of the capacitor is to resonate with the mutual inductance while the resistance is reduced in size and split in a R-C-R series to enforce design symmetry. Owing to this capacitor the $S_{2,3}$ parameter is strongly improved. The value of the capacitor and resistors are optimized by a tuning procedure and finally reach the value of 50 fF and 27.1 Ω respectively.

The final shape of synthesized splitter is represented in 3D image in Figure 56. Here, capacitors, resistors and dummy metals are added in order to show

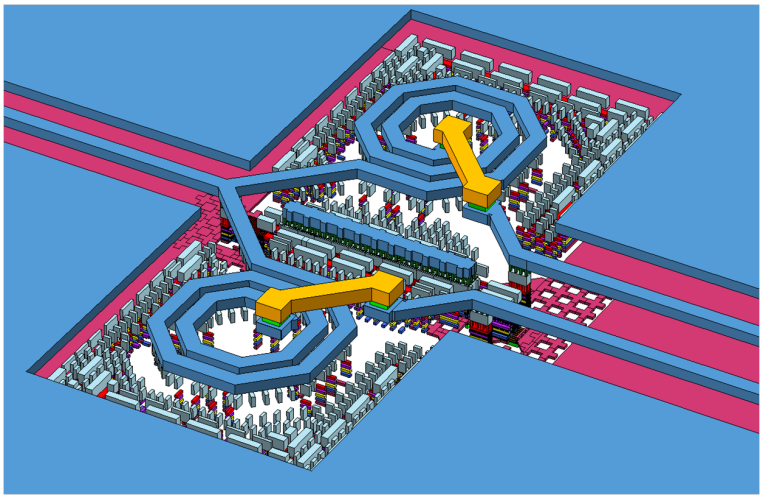

Figure 56: Final shape of wilkinson power splitter

the complexity of the final structure. For the final step of inductor simulation, however, only the top level of dummy metals (metal 6) has been take in to account to maintain the simulation under 20 GB of virtual memory.

Simulations and measurements

The component is measured with N5247A PNA-X 4 port VNA by Agilent. Figure 57 shows the test bench circuit realized to characterize the circuit. A de-embedding procedure is used to eliminate the interactions of access pads and lines. Figure 58 and 59 show simulations and measurements results for the insertion loss (IL) and return loss (RL) of the splitter. The data show a very good agreement within each other and confirm the validity of the presented approach.

The combination of electro-magnetic and circuital simulators has allowed overcoming the well known intrinsic limitations of the two separate approaches. Full wave simulations are limited by the virtual memory needed to consider

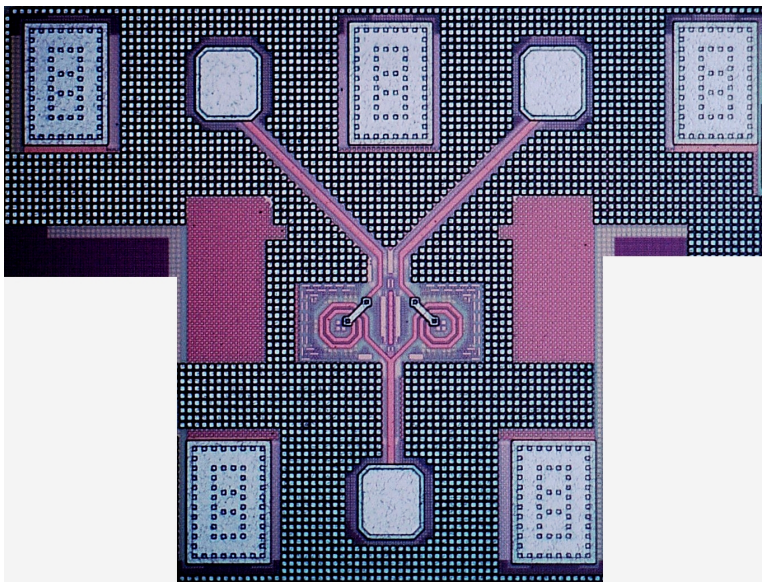

Figure 57: Test bench ciruit

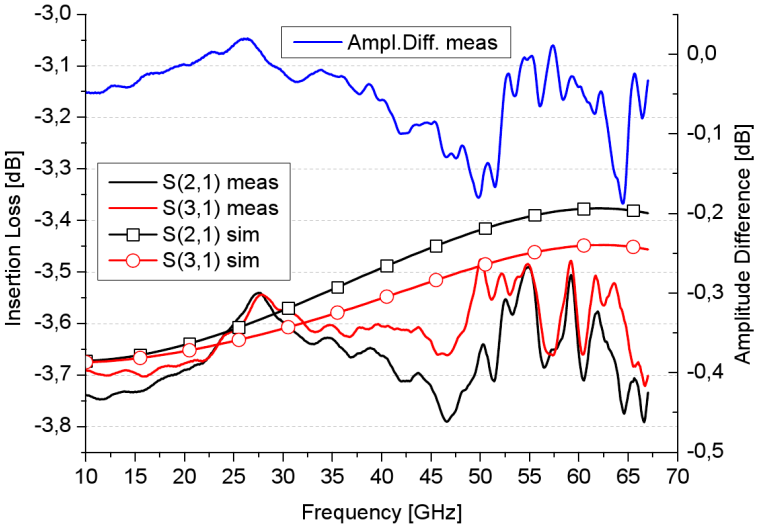

Figure 58: Insertion loss of Wilkinson power splitter

Ref.	Band [GHz]	IL [dB]	RL [dB]	Is. [dB]	Size W×L [µm]
This Work [8]	**10-60**	**0.8**	**-25**	**25**	**114×49**
[54]	60	0.52	-24	22	536×150
[55]	60	0.5	-17.5	22	400×300

Table 4: State of the art for reduced size wilkins power splitter

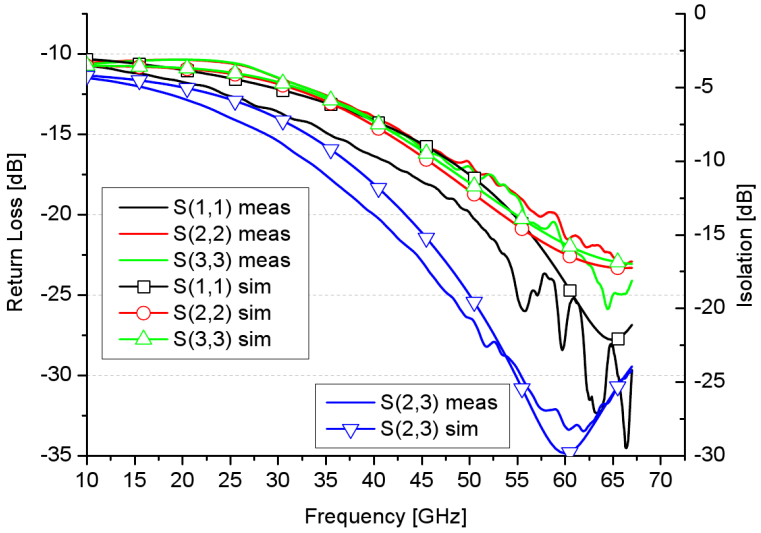

Figure 59: Return loss of Wilkinson power splitter

all the possible interactions among the different components inside the splitter. Schematic simulators are not able to consider all the possible interactions among the different components inside the splitter. Thanks to this approach the time simulation of the EM part is strongly reduced and even the optimization of the remaining parts becomes simpler. The small differences on the IL are probably due to some residual coupling mechanisms not yet considered in the model. The principal suspects of the degradation on the transmission value are the dummy metal posts around the coils. Although their presence has been considered in the full-wave simulation of the entire structure, computing memory considerations have restricted the options to a perfect metal conductor modeling of the same. In reality the measurement results highlight the role of the losses which dependent from the frequency due to the skin effect. Return loss and isolation remain close to the simulation confirming once again the high quality of the design flows and the dissipative effect being the only reason to transmitted power losses.

Conclusion

In the previous pages the design of a miniaturized Wilkinson power splitter in CMOS 65 nm technology is discussed. The proposed procedure is based on a two steps synthesis approach. First the main structure parameters are extracted from simple analytical design rules. Second, an efficient modeling flow combining the use of full wave modeling with a schematic circuit simulation is applied to carry out the final splitter optimization. The proposed method translates in a time-effective prototyping procedure very useful in the 60 GHz RFIC design. A result of it the splitter presented here presents state of the art RF performances and unrivaled size reduction with only $114 \times 49\ \mu m^2$. The IL remains below 0.8

dB while the input and output RL are better than -10 dB over the entire 10 to 67 GHz band. The output port isolation is better than 10 dB from 35 to 67 GHz. Noteworthy is that the isolation response can be tuned by varying the shunt capacitance value, here optimized for the 60 GHz band. The most representative power splitters found in literature are collected in Table 4.

ACTIVE BLOCKS

3.1 MIXER

The mixer is a high non linear circuit usually represented by a block with three I/O ports: the intermediate frequency port (IF, also called Base Band (BB)), the radio frequency port (RF), and Local Oscillator port (Local Oscillator (LO)). For the upconverter version of the mixer IF and RF are respectively the input and output ports, whereas the third port (LO) is the driver of the mixer. The driving action, sometimes also called switching or modulation is highly nonlinear and causes the change of the device conductance (or transconductance) between two states: high and low conductance (transconductance).

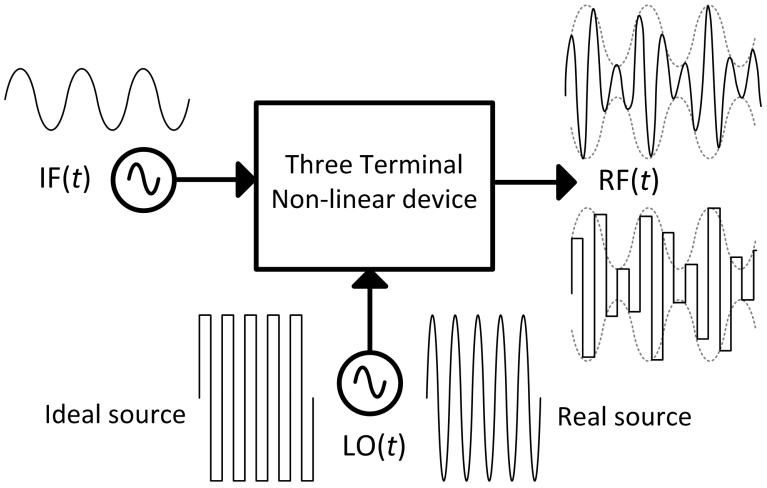

Figure 60: Generalized mixer mode

In a passive mixer architecture the parameter to be modulated is the device conductance, whereas in active architectures it is the transconductance.

The frequency translation is then obtained by a time variation of this parameter. The switching between the two states occurs at the local oscillator frequency f_{LO}, thus the conductance contains the fundamental component, and all possible higher harmonics as well. With a LO signal strong enough to make the mixer's operation non linear it is possible to represent the non linearity with the following formula:

$$\begin{aligned} g(t) &= g_0 + g_1 \cos(\omega_{LO} t) + \\ &+ g_2 \cos(2\omega_{LO} t) + g_3 \cos(3\omega_{LO} t) + \ldots \end{aligned} \tag{3.1}$$

Where $\omega_{LO} = 2\pi f_{LO}$. Assuming that the shape of the LO signal is a perfect square, the non linear mixer conductance $g(t)$ becomes:

$$\begin{aligned} g(t) = \tfrac{g_{ON}}{2} + \tfrac{2g_{ON}}{\pi}\cos(\omega_{LO}t) - \\ + \tfrac{2g_{ON}}{3\pi}\cos(3\omega_{LO}t) + \tfrac{2g_{ON}}{5\pi}\cos(5\omega_{LO}t) - ... \end{aligned} \tag{3.2}$$

If a signal v_{IF} with a certain frequency ω_{IF} is sent to the IF port (maintaining the hypothesis of upconversion mixer) the RF port output corresponds to:

$$\begin{aligned} i(t) = g(t)v_{IF}(t) = g_0 v_{IF}\cos(\omega_{IF}t) + \\ + \tfrac{g_1}{2}v_{IF}\left[\cos(\omega_{LO} - \omega_{IF})t + \cos(\omega_{LO} + \omega_{IF})t\right] + \\ + \tfrac{g_2}{2}v_{IF}\left[\cos(2\omega_{LO} - \omega_{IF})t + \cos(2\omega_{LO} + \omega_{IF})t\right] + \\ + \tfrac{g_3}{2}v_{IF}\left[\cos(3\omega_{LO} - \omega_{IF})t + \cos(3\omega_{LO} + \omega_{IF})t\right] + ... \end{aligned} \tag{3.3}$$

The IF signal, translated in frequency by the LO carrier, preserves its phase and amplitude values in the Fourier components at the output waveform. For the upconverter mixer, the RF component at frequency $\omega_{LO} \pm \omega_{IF}$ is the one of interest. Consequently, the desired RF output is the first harmonic component at the frequency $\omega_{LO} + \omega_{IF}$, which amplitude is $(g_1/2)\, v_{IF}$ thus meaning that the IF signal strength linearly drives the amplitude of the desired RF signal.

The conductance g is defined as $\delta I/\delta V$, for the simplest case of a square-law device. The current flow inside the device corresponds to:

$$I = I_0 + G_1 V(t) + G_2 V^2(t) \tag{3.4}$$

and consequently the conductance is:

$$g(t) = G_1 + 2G_2 V(t) \tag{3.5}$$

The LO signal $V(t) = V_{LO}\cos(\omega_{LO}t)$ represents the control voltage and the coefficients of eq. 3.5 are the g_i of eq. 3.1: $g_0 = G_1$ and $g_1 = 2G_2 V_{LO}$. By this consideration it results that the RF component $(g_1/2)v_{IF}$ depends on the second order non linearity and it is linearly related to the input signal v_{IF}. In the n-order devices the differentiation of equation 3.4 produces some terms $(n+1)G_{n+1}V(t)^n$, thus increasing the numbers of harmonics components. The value of g_0, g_1 changes and further dependencies on the LO signal level are added.

The most common figure of merit used to characterize a mixer is the conversion gain C_G, which relates the input and the output signal powers. For the upconverter the C_G is:

$$C_G = 10\log\left(\frac{\text{RF Signal Level}}{\text{IF Signal Level}}\right) \tag{3.6}$$

Assuming a square wave for the LO signal, it is possible to estimate the conversion gain of a mixer using equations 3.2 and 3.1. The IF frequency current is $g_0 v_{IF} =$

$g_{ON}v_{IF}/2$ while the RF is $g_1 v_{IF}/2 = g_{ON}v_{IF}/\pi$, where $g_{ON}$is the conductance in ON state. Then, the of RF to IF signal level ratio is $2/\pi$ which gives, normalized to a resistance value of 50 Ω Ohm, the following value of C_G:

$$C_G = 10\log(2/\pi)^2 = 10\log(0.4055) = -3.92\,\text{dB}. \tag{3.7}$$

This value represents the theoretical upper bound of the conversion gain for mixers since it is calculated considering an ideal square wave for the LO signal. Now, considering the passive mixer architecture,−3.92 dB represents the maximum theoretical C_G, whereas, for the active mixer architecture, it is the minimum value of gain required for the active part of the circuit to obtain a C_G of 0 dB. However, in real conditions, the C_G is lower than −3.92dB. The LO signal is a sinusoidal wave that requires a small but finite time to switch the devices state (ON /OFF) inside the mixer while the previous estimation considers an input square wave with zero switching time. Therefore the RF value decreases from $g_{ON}v_{IF}/2$ to $g_{ON}v_{IF}/4$ and the C_G becames 0.25, i.e. −6 dB. As the LO becomes even weaker and is unable to drive the conductance between an off-state and a fully saturated on-state, the peak value of the IF current becomes correspondingly smaller and the conversion loss becomes worse.

It is important to point out that the previous considerations are based on Single Side Band (SSB) modulations widely used to preserve occupied spectrum. For the 60 GHz application and, more specifically, for the direct up/down-conversion the Double Side Band (DSB) technique is adopted. This choice is due to the absence of high selectivity filters able to cut the single side band of the signal without damaging the quality of the other sideband. As shown in 2.1.1 at 60 GHz is not possible to yield passive components with highest quality factor values and, as a consequence, the quality factor of a filter does not allow a reasonable ratio between the Insertion Loss (IL) in the pass-band and the Attenuation (L) in the stop-band. Therefore, the double side band is the only possible choice. The doubling of occupied band shows at least two positive features: the C_G, derived in Equation 3.7, is reduced to -0.92 dB due to the contribution of both the sidebands, and the noise figure of the circuit decreases of the same value. In conclusion, considering a DSB mixer with ideal devices driven by a sinusoidal wave, it shows a maximum conversion gain of −3 dB in place of −6 dB for the SSB, and a minimum noise figure of 3 dB.

The linearity of a mixer is another very important feature. As explained before, the mixer shows a highly nonlinear response to yield a frequency conversion. Despite that, the relationship between the IF and RF signal must be kept linear over a specified range. In order to meet this requirement, the linear gain (or conversion loss), the −1dB compression point, and the intercept point can be defined in the same way as in the (linear/nonlinear) amplifier theory. The LO power level at which the measurements are made is usually fixed and needs to be sufficiently high to achieve the desired conductance waveform. The harmonic components

of the mixer are the "m, n" distortion products that occur at frequencies of $m\omega_{RF} \pm n\omega_{LO}$ with $n, m = 1, 2, 3, ...$

On the other hand the Third order Intercept Point (IP_3) of a mixer is defined by the extrapolated intersection of the primary RF response with the product of the two tone third-order intermodulation RF tones that is obtained when two IF signals are applied to the input port of the mixer.

As for an amplifier, it is common to model the output IP_3 point as 10 dB above the compression point ($CP_{-1\,dB}$).

This result, which was given for a general third-order nonlinearity, can be applied also here because the intermodulation distortion still results from mixing within the cubic term in the conductance nonlinearity. As with amplifiers, it is only a rule of thumb, wereas in real devices higher intercept points can be achieved if the higher-order terms in the nonlinearity shift the third-order term.

3.1.1 *Upconversion Mixer*

The requirements for the designed up-conversion mixer circuit were: low-power consumption, good linearity, and low conversion loss. The IF bandwidth has to exceed the channel bandwidth defined by the 60 GHz standards (i.e. from DC to around 1.5 GHz, because the IF bandwidth is doubled due to direct up-conversion). The RF bandwidth should cover the whole unlicensed band from 57 GHz to 66 GHz. Furthermore, LO and RF rejection is an important issue. A very common solution to meet these requirements is a fully balanced up-converter topology like the Gilbert cell [58]. It requires differential IF and LO signals to generate a differential RF output, from which both of input signals are deleted, achieving a good isolation. The dual gate mixer is another way to realize an active up-converter circuit [59]. It can be seen as a derivation of Gilbert cell circuit as discussed in [18]. Both circuits work with transconductance (g_m) stages to amplify the IF frequency and switches controlled by LO signal to yield the frequency shift. The main limitation of these architectures is constituted by the stack of transistors needed to amplify and mix the signals. The problem is even more marked in the case of low voltage supply technology (such as the 1-1.2 V in 65 nm Complementary Metal Oxide Semiconductor (CMOS)). In the Gilbert cell the circuit shows a transistor stack composed by three nMOS in addition to the passive load (Figure 61a). The non ideal behavior of the current mirror and LO switches reduce the value of Transconductance (gm)in the transconductance stage by the introduction of parasitic voltage drops. For the dual gate version of the mixer the problem is the same: the non ideality of the switches reduce the C_G and the linearity of the mixer.

A completely different family of mixers is represented by the passive architectures [60]. The simplest implementation of passive mixers is the single transistor resistive mixer. In this architecture the LO, injected in the gate of n-Well Metal Oxide Semiconductor (nMOS), opens and closes the channel of the diode, thus

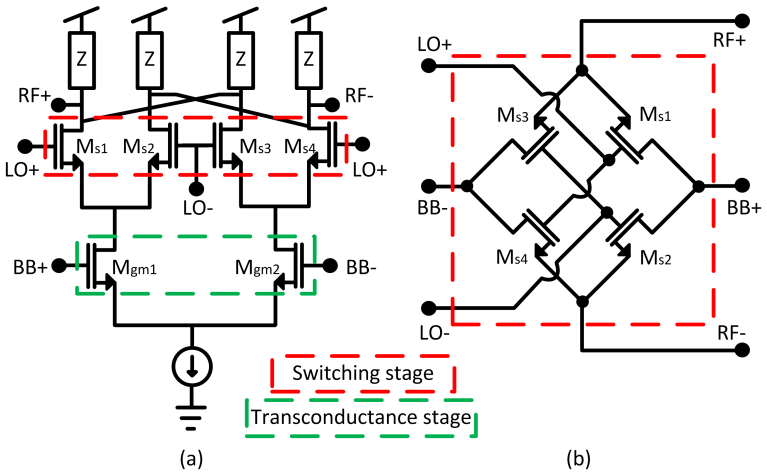

Figure 61: Mixer detail

acting it as a switch. The IF signal is connected to the drain whereas the source is connected to the ground. The RF signal is already connected to the drain and it is extracted by an opportune decoupling network. To improve the performance of the passive version of the mixer in terms of port isolation and linearity, a full balanced architecture can be employed placing the transistors in a ring configuration as shown in Figure 61b. It is worth to note that the main advantage of a passive mixer is the zero DC power consumption. On the other hand, literature shows as the passive mixers require higher value of LO signal power in order to reduce their conversion loss. Table5, in the next pages, summarizes the state of the art of the 60 GHz up-conversion mixers. The better examples of the three discussed families of mixer are proposed in order to evaluate their respective performances. In literature it was found that great part of the mixers for 60 GHz applications are based on the active configurations; among those, the Gilbert cell is the most employed. Analyzing the structure in Figure 61a is possible to redraw the Gilbert cell in order to highlight the passive mixer hidden in this architecture. Figure 62 shows the redrawn circuit. The Gilbert mixer can then be viewed as a passive mixer to where an active block has been added to amplify the baseband input signal. The considerations concerning the limits on C_G and IP_{-1dB} for the Gilbert cells with low voltage supply technology are even more evident in Figure 62.

The melting of the passive and the active stage in Gilbert cell mixer could represent an issue, especially for low power technologies. The performances of the active block are deteriorated by the presence of a switching network that afflicts the transconductance stage in different ways. The first issue is related to the DC bias of the active block. In particular, the channel of the CMOS shows an intrinsic resistance (R_{ch}) that causes the fall of the absolute value of the bias supply reducing the dynamic of the voltage headroom in the amplifier stage. For this reason also the loads Z must show very low losses if composed by reactive components (inductors) or, however, they should assume a small resistive value if

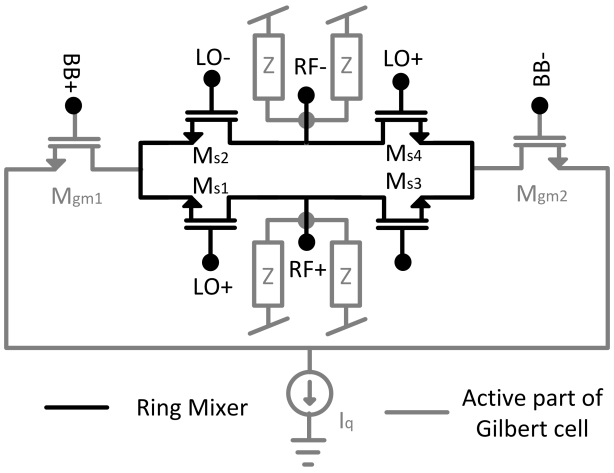

Figure 62: Gilbert cell redrawn in order to highlight the hidden ring mixer

resistors are employed. As a result of the above considerations, the total gain of the active parts is reduced. On the other hand, also the active stage has negative effects on the switching capability in the passive block: the DC current, required for the correct bias of the active stage, flows into the drain of the switching transistors hindering the locking up of theirs channels. If the system requires a high value of linearity the problem gets worse.

In order to carry higher value of power the transconductance stage should work with wider transistors. To maintain the correct value of quiescent current per micron in the active block and to limit the resistive losses into the channel of the switching transistors the size of these latter should be rised. The increased DC current together with the augmented size of the transistors make worse the switching capability of the resistive block. The bad performances of the switches reduce the nonlinear behavior of the passive block and, as a consequence, the conversion loss value rises. In conclusion, the lowered capability of amplification in the transconductance stage, caused by the smaller voltage headroom togheter and by the increase of conversion loss in the resistive part make the Gilbert cell a bad candidate for frequency conversion in which the linearity is one of the main features to satisfy.

A remedy to the above issues is the use of the current bleeding technique [61], which is also known under the name of charge injection [62]. The insertion of a current source in parallel to the switching pairs allows to by-pass one part of the bias current of the transconductance block from the upper transistors and the load Z. Thus, independent transistor biasing is possible. This countermeasure yields higher transconductance in the active block, and faster switching and lower conversion loss in the resistive mixer part. The drawback of this solution, especially for very high frequency conversion, is the non ideality of the current sources in the current bleeding branches. The current sources, being realized through current mirror more or less complex, are subject to a parasitic effect

that reduces the high output impedance normally showed at low frequency. In order to isolate the current generator from the Gilbert cell, inductors or $\lambda/4$ high impedance lines are employed [63]. The proposed technique improves the performance of the complete structure in terms of linearity and conversion loss but the problem is not still completely solved. The not ideality of the inductor working as high RF impedance path shows DC resistance that can rise until $5-7\,\Omega$ producing undesired power dissipation in the DC path. Moreover the total power consumption of the circuit (not considered until now in the design feature) can arise relevant problems in particular on the low power and ultra low power architectures. Starting from the above-mentioned consideration and given the intrinsic nature of passive mixer in the full balanced Gilbert cell, in the work presented in this thesis it has been chosen to separate the two parts of the Gilbert mixer and to optimize separately the resistive ring mixer and the amplifier. In this way, the mixer is designed to obtain performancesas better as possible both in linearity and conversion loss. The absence of supply voltage (instead required for the Gilbert cell) allows zero power dissipation and does not hinder the locking up of transistor channels. On the other hand, the stand alone differential amplifier can be optimized without the interference of the switches or the constraint of the current bleeding path.

3.1.2 *Resistive Mixer: Core Design*

As previously demonstrated, the maximum C_G suitable for a DSB passive mixer driven by a sinusoidal wave is -3 dB. In the real conditions the performance are worse because the devices are conditioned by the well known parasitic effects present on the CMOS transistors.

The model of switches used in the calculus in eq. 3.7 performs infinite resistance (open circuit) when they assume the OFF-state and a zero impedance value (short circuit) when they are in the ON-state configuration. The performances of the real CMOS device working as switch are quite far from these features. Both of the functioning states are affected by parasitic phenomena that move away from the concept of ideal switch. Figure 63 highlights the parasitic effects existing in a self-aligned CMOS transistors [64].

The problem of the different behavior between an ideal switching device and a real Metal Oxide Semiconductor (MOS) switch is analytically discussed in [65]. In the paper it is shown how the C_G of a mixer is strictly connected to the minimum allowed R_{ON} resistance and the maximum allowed Z_{OFF} impedance, as reported in the following formula:

$$G_C = 20\log\left[\frac{2}{\pi}\left(\frac{Z_L}{Z_L+R_{ON}\|Z_{OFF}}\right)-\frac{2}{\pi}\left(\frac{Z_L}{Z_L+Z_{OFF}}\right)\right] \tag{3.8}$$

As for the parasitic resistance in the ON-state, the total R_{ON} is:

$$R_{ON} = \frac{L_G}{\mu_n C_{OX} W_T\left((V_G - g_c v_{RF}) - V_{th} - V_{DS}\right) Z_L} \tag{3.9}$$

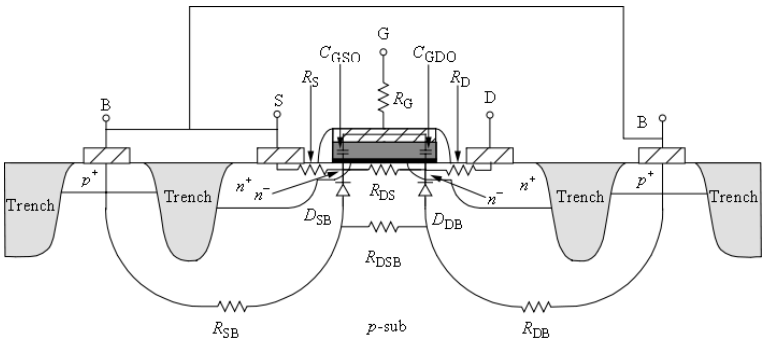

Figure 63: CMOS Parasitic effects

Where L_G is the channel length (65 nm for the adopted technology), μ_n is the electron mobility, C_{OX} is the oxide capacitance, V_G is the DC applied voltage on the gate, g_c is the conductance of the device, v_{IF} is the input applied signal. V_{th} is the threshold voltage of transistor, and V_{DS} is the DC voltage difference between drain and source (assumed zero for the passive mixer).

As for the OFF-state, the maximum allowable Z_{OFF} impedance is:

$$Z_{OFF} = \frac{1}{j\omega_{RF}(C^0_{GS} \| C^0_{GD})W_T} + \frac{1}{j\omega_{RF}(C^{M0}_{DS})W_T} \parallel R_{ch(OFF)} \tag{3.10}$$

In this equation C^0_{GS} and C^0_{GD}represent the normalized capacitances between the three contacts of the CMOS, as shown in Figure 63 whereas C^{M0}_{DS} represents the parasitic capacitance of the metallic contact between drain and source normalized to the unit length.

An important variable present in both of the previous equations is the geometrical parameter W_T representing the total width of the transistor. The equations 3.9,3.10 highlight a response inversely proportional to the W_T. So, for low R_{ON} values the W_T parameter has to be very high, while to reduce the capacitive effects that degrade the high OFF-impedance the W_T must be as smaller as possible.

For this reason, the design of the ring mixer starts with the analysis of the single transistor block in order to understand how minimize the occurrence of these unwanted phenomena. The first point to solve is the reduction of the shunt capacitance between drain and source (C^{MO}_{DS}).This parasitic capacitance, differently from the others C^0_{GS} and C^0_{GD} that depend on the realization of the active zone of the transistor, hinges on the shape of copper metal of the drain and of the source contacts. C^{MO}_{DS} capacitor reduces the value of the transistor impedance when the MOS is in OFF-state and it is directly proportional to the transistor size W_T. In order to reduce the losses, the passive elements like the inductors or, more simply, the connection lines are implemented on metal 7. In this case, it is necessary to connect the active region of the transistors with the passive device at layer 7. A stack of via-holes and metal levels were then used to fill the gap between the contacts of the Source and Drain and the metal of layer 7. As shown in Figure 15 the stack of seven copper metals has a total

height of 5.1µm (from the doped area up to top of metal 7) and the maximum available gap between the drain and source contacts correspond to 160 nm. Under these conditions it is of fundamental importance to evaluate the capacitive effects that occur between the two walls of contacts. The metal connections (between metal 1 and metal 7) are composed by rows of via-holes and copper lines and do not constitute exactly a filled wall of metal because there are many apertures in correspondence of the via-holes rows. On the other hand, considering the electromagnetic characterization, the overall metal connection can be modeled with good approximation as a full copper wall (the fringing effects around the cavities is able to balance the absence of the real metal). Assuming this hypothesis it is possible to model the two consecutive contact walls as a parallel plate capacitor. The C_{DS}^{MO} parasitic capacitance can then easily estimated by an equivalent capacitor with a rectangular shape size of 5.1µm of width and W_T of length. To evaluate the parasitic capacitance between the two metal contacts a simulation campaign using CST microwave studio was performed. The main simulations analisys are substantially two: the capacitive effect between the walls and the current density flowing into the contact. The first analysis is important to estimate the total effect of the parasitic capacitor, while the second one shows the distribution of the current into the metal. By knowing the current density inside the metal layer and the via-holes it is possible to design the best shape able to reduce the parasitic effect of the coupling capacitance (C_{DS}^{MO} in this case) while maintaining other parameters, such as the total equivalent contact resistance and the maximal current density, in reasonable ranges. Figure 64 represents the

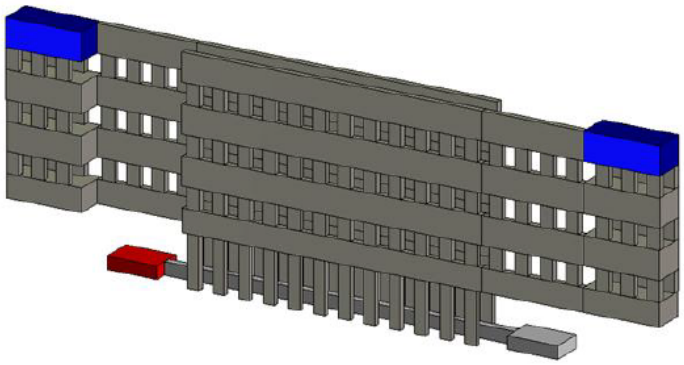

Figure 64: Metal connection in a standard CMOS transistor

copper connection for a drain-source contact realized up tu metal 4 layer. As described above, the two walls constitute a vertical parallel plate capacitor that generates high value of parasitic capacitance. On the other hand, the current density simulation for the single metal wall highlights a non homogeneous distribution of the current. In effect the charges flowing into the structures are injected from the top of the blue brick in figure 64 and they are sunk by a perfect

electric sheet (emulating the doped n^+ silicon) placed on the first row of via in the bottom of the structure. The metal used in the model is the copper with a conductivity of $4.13E^7$ S/m as described in the Design Kit (DK). The simulation shows a gradient of the current density with a maximal value in direction of the arrow head. This behavior can be easily justified by the principle of minimum available path. The homogeneous conductivity of the copper induces the charges to minimize the distance between the IN/OUT ports. Therefore, the side of the metal wall far from the two contacts shows a minimum density of charges. The change of the structure's geometry with the insertion of the second wall of contacts affects the distribution of the currents into the walls. In this configuration the potentials are placed into the two anti-symmetrical points, and the via-holes into the bottom are connected with a perfect metal sheet.

Differently from the previous simulation setup, in this case the density of currents increases in the corner where previously the currents were less dense. The rise of the charges is attributable to the presence of the second contact in the other side of the structure. In order to reduce the capacitive effect generated by the high proximity of the two metals a reshape of the metal is required. Simulations performed on a single metal wall have shown that the use of a square shape is not the most suitable in terms of current flow in the active region of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). For this reason, the metal is redesigned using a triangular shape to conduct the currents from the high layer to the doped region.

Thanks to this approach, the superposition area of the interleaved contact has been highly reduced. The maximum allowed current density in the via-holes and in the metal lines has been checked by current simulation using CST. In the particular case of a cold device, (and this is the case for the passive mixer), the absence of DC currents flowing into the device reduces the problem of electro-migration phenomena due to the too high currents in the interconnection lines of the transistor. In fact, the technology DK rules allow the alternate currents (Alternate Current (AC)) to have absolute values many times bigger than the DC currents ones. In order to maintain high values of reliability, the current densities on the metal contacts are bounded to satisfy the DC current rules. Figure 65 shows the new shape of the transistor contacts. Thanks to this approach, the total parasitic capacitance between drain and source is strongly reduced and the Z_{OFF} impedance improves its total value. Then the total W_T can rise maintaining a reasonable value of parasitic capacitive contributes. The discussed tradeoff between high OFF-state impedance and very low ON-state resistance, however, is not still solved because the shape of transistor is not still completely fixed. The performances of the switch are also influenced by the total amount of RF power that the transistor must carry out. For high values of power the total W_T must be large and the shape of transistor, in term of number of fingers and fingers length, is decisive for the good response of the device. After a campaign of simulations the transistor chosen as RF switch is composed by 20 finger of 2.5 µm for a total

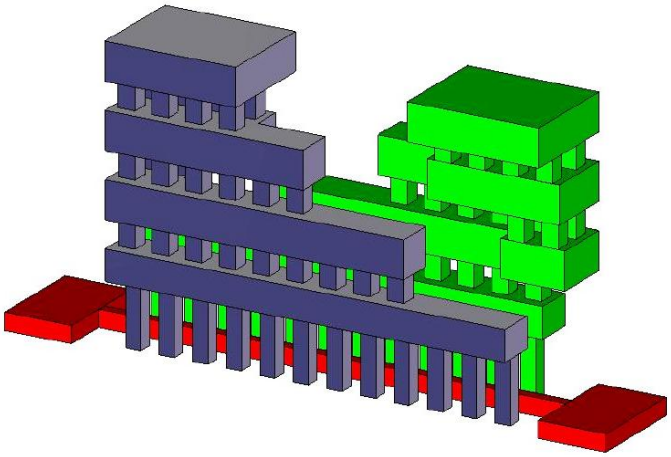

Figure 65: Redesign of the contact metals

width of 50 µm. The gate resistance (R_g), directly proportional to the finger width, is slightly sacrificed (in literature the better width of RF transistor is 1 µm) in order to maximize the reduction of capacitive effect by means of the metal triangular shape of the contact. Therefore, this sizing of transistor allows obtaining more compact transistors that simplify the placement of the entire mixer block.

The fully balanced ring mixer, as other differential frequency converters, shows high isolation values between the three ports. Under the condition of high symmetry on the interconnection structures, the mixer allows obtaining very good performances. The counter-phase signals in the symmetric branches assure the suppression of parasitic propagation into the other ports. In order to exploit this property maximizing the performances of the circuit, the design of the interconnections has to be very accurate. The main issue in the mixer design is represented by the circular shape of the switching block. As shown in Figure 61b a certain number of interconnections crossings are mandatory. Among these there are two cases where the intersections are critical. The first is inside the core of the mixer, between the LO+ and LO- paths, and the second one is between the ±LO paths and RF or IF lines (depending on the designer's choice). Concerning the intersection between the LO paths inside the mixer core, a simulation of the structure has been carried out in order to evaluate the entity of the coupling effect and the phase delay at each port.

Figure 66 shows the simulation setup of the paths intersection, whereas Figure 67 shows the transmission parameters. The S_{ij} values are referred to the port numbers assigned in Figure 66. As shown in the Figure 67, the power coupling among the differential branches remains limited to −30 dB at 60 GHz. The −30 dB, in effect, constitutes the worst performance in the parasitic coupling of ports $1 \div 3$ and $2 \div 6$. In these two circumstances, in fact, an upper value of LO coupling is due to the superposition of the two differential main paths, coming from ports 1 and 2, with the split paths of port 3 and 6. By closing the two metals,

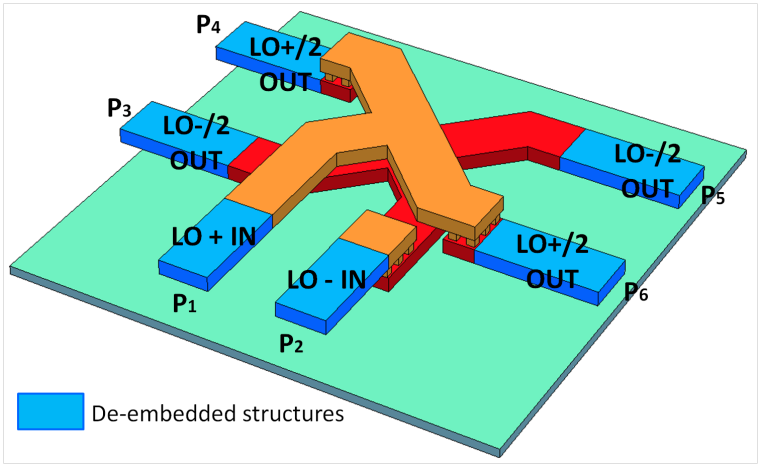

Figure 66: Simulation Setup for the LO crossing paths

the capacitive coupling between the balanced signals can be increased by a factor of four (+6 dB). The reduced size of the metal lines (the total size of the signal splitting network is only 10×15 µm) is also favoured by the compact transistors working as switches.

Concerning the problem of the crosstalk between the LO and RF /IF lines, a risk analysis is required. There are two possible scenarios: the superposition between LO and RF, and the superposition between LO and IF. Considering that the band of IF signals starts from 10 kHz up to 1.5-2 GHz, the modulated RF signal is quite close to the LO carrier one. The presence of parasitic coupling paths between RF and LO can create an undesired feedback loop and the RF signal could became a second carrier generating spurious tones as part of the exploited frequency band. On the other hand, the coupling among LO and IF generates similar effects on the mixer, but, considering the enormous difference between the frequencies of the two tones, the effects on the frequency conversion are less dangerous. In effects, considering the possible feedthrough of the LO signal in the IF paths, the modulation sends half power of the parasitic signal to one frequency two times higher than LO and the other half part to DC. On the contrary, for the feedthrough of the IF into LO paths the probability of the occurrence is approximately zero for one main reason: the wavelength of the highest frequency in the base band is at least 30 times wider than the LO carrier one (2 GHz versus 60 GHz of LO carrier). For relatively low frequencies (under 3 GHz) the coupling factor decreases rapidly. Therefore, the only possible influence on the crosstalk phenomena between LO and IF signals is referred to the feedthrough of LO carrier into IF paths. Starting from these considerations, the choice to intersect LO and IF paths is preferable compared to the RF and LO one. Figure 68 shows the 3D representation of the mixer core with the placement of the three differential ports. The gate of the four 50 µm transistors are connected by the high symmetrical structure (discussed above) to the differential LO signal (LO±). Input and output signals (BB± and

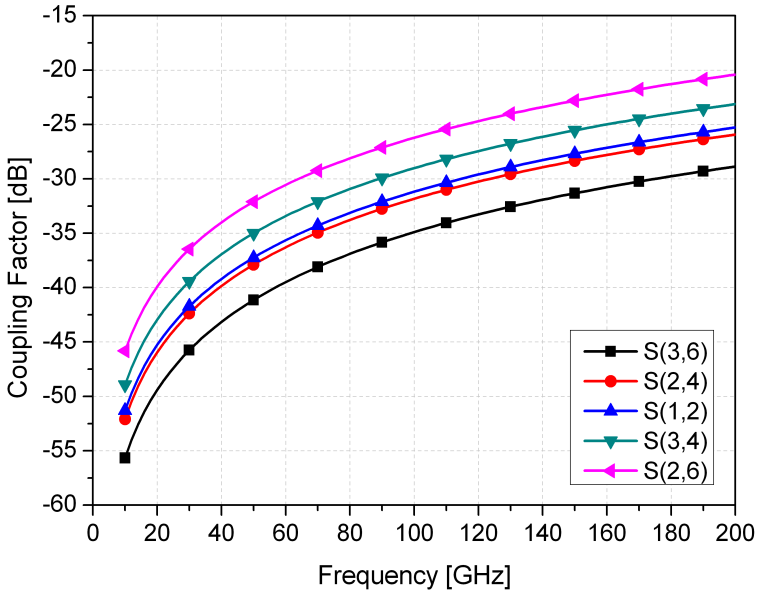

Figure 67: Coupling factor in the mixer crossing path

LO± respectively) are, instead, directly relied to the source and the drain of the MOS transistors. Furthermore, to reduce the effect of LO feedthrough into IF+ port, a stub is opportunely placed at the end of IF+ contact in order to catch the same quantity of LO power absorbed in the superposition of IF+ and LO +. This solution has been studied in order to erase the effect of the parasitic LO signal at the input of the IF+ port. Concerning the possible effects of the stub in the IF+ signal, it is opportune to underline that the length of the stub is only 21 µm that results imperceptible for the IF frequency carried by the metal. Moreover, the presence of the stub forces the field around LO- line to have the same discontinuity encountered by LO+ lines and, then, the phase balance at the input terminal is maintained.

3.1.3 *Matching Networks*

The design of the matching network for the three differential ports represents the last required step. Large signal simulations are performed in order to understand the behavior of the structure under the effect of strong signals. In this phase of analysis it was discovered a strong dependence between the LO signal level and the return loss (RL) of IF and RF. In particular, transient simulations highlighted a strong influence of the V component of the LO signal on the variation of Return Loss (RL) at the IF and RF ports. For this reason the design of the matching networks has to start from the LO port. The four big transistors constituting the ring show a high mismatching compared to the required 50 Ω. The S-parameter simulation shows a value of $0.95 - 21.08j\ \Omega$ that corresponds

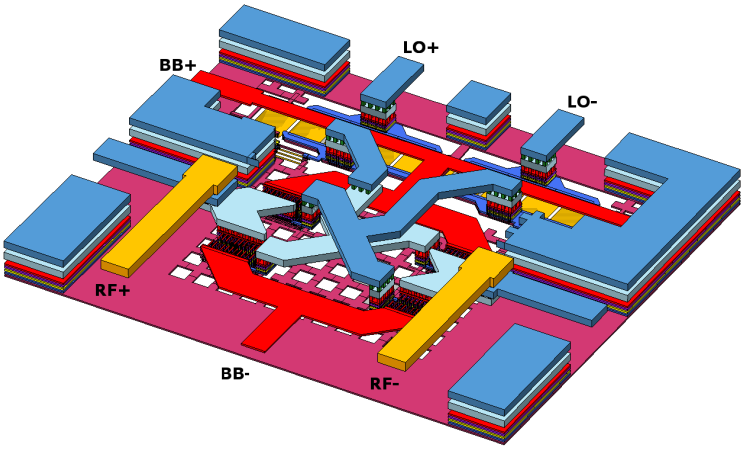

Figure 68: Sonnet 3D model of complete mixer core

to 128 fF of capacitance and 0.92 Ω of resistance. The impedance, represented on the Smith chart, is extremely close to the external border of the chart. This means that the matching network is very hard to synthesize. The simpler version of the matching network consists of two small inductances: a shunt inductor of 18.5 pH followed by a series inductor of 37.4 pH. The small inductive values of the two components impose the use of distributed inductances in the place of the spiral inductors. Moreover, the shunt inductor is dynamically connected to the ground through two capacitor of 2 pF in order to maintain 200 mV of DC bias for the LO switches. This configuration was employed in the first design of the passive mixer. In that case the architecture was conceived for a downconversion block. The results obtained during the measurement campaign were disastrous. The mixer show around -40 dB in conversion gain at +5 dBm of LO signal. After a series of retro-simulations the problem was discovered: the LO matching network was miscalculated. The coupling effects with the others parts of the circuit and the underestimation of the parasitic effects caused by the contacts (in particular the connections between the shunt inductor and the capacitors) led to an unwanted change in the values of the matching network components and, as a consequence, the RL increased rapidly. Anyway, the experience acquired by the down converter mixer design has been exploited during the development of the frequency upconverter. In this case, to avoid the danger of variations on the intrinsic values of the matching network component, another strategy has been employed: on the place of the two distributed components, a network of R – L lumped elements has been used in order to reduce the variability of the RL in the LO ports. This approach, however, shows strength and weak points. The only weakness shown by this circuital solution is the reduction of the voltage peak value. Although his reduced resistivity (4.65 Ω of polysilicon resistor plus 1.5 Ω added by the IN/OUT vias), the resistor causes a voltage reduction of around 50 mV in the LO signal. On the other hand, there are several points of strength introduced by this type of

matching network. The first and more important is the drastic reduction of the possible variation of the RL value due to the not perfect design of the component in the matching network. A Monte Carlo analysis has been performed in order to verify the behavior of the R – L matching network, and the obtained results have been compared to the response of the L - L network described above. Figure 69 shows the behavior of the two networks. The analysis has been performed by

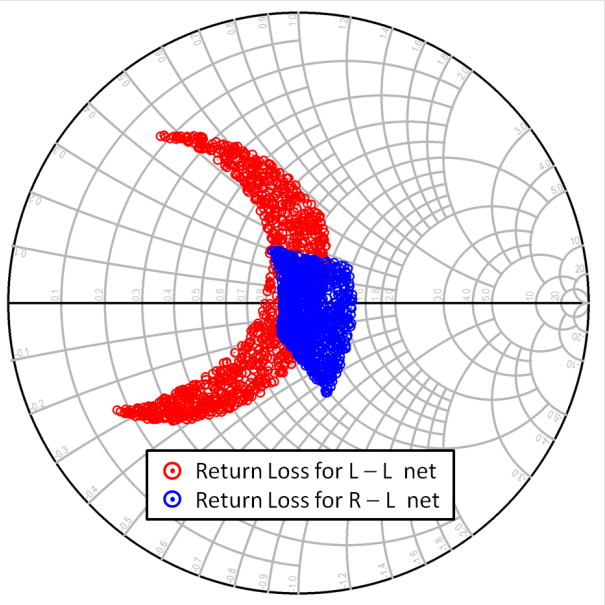

Figure 69: Monte carlo analysis for the LO matching networks at 60 GHz

using an uniform probability distribution function for the component values. A delta of 10% around the nominal value is chosen for the lumped inductor and for the lines, whereas, for the resistance the delta is 33% (as described in DK manual). Despite the three time bigger variance of the polysilicon resistor, the effect in the RL of the full inductive network results many times bigger. Another positive consequence deriving by the reduction of the possible variance of the RL in the LO port is the increase of the reliability of the performance of LO source. This problem, in fact, is particularly critical during the integration of the different blocks as results in 5.1.1. If the mixer shows a bad value for the input impedance, also the LO source suffers from a worsening of performance due to the bad load impedance. In the case of this new version of matching network, the possibility of impedance variation remains constant but the possible range of impedance values is strongly reduced as shown in the Monte Carlo analysis (Figure 69). In the case of R – L network, however, it is mandatory to underline the different value of matching impedance. The use of resistor moves the LO input impedance along the curve with 23 i of constant reactance. The 6.15 Ω are sufficient to move the matching point near the circle of constant admittance 0.013 S (75 Ω). In order to increase the voltage swing at the gate of the switching transistor and get back

part of the voltage swing loss into resistance, the LO port impedance was fixed at 75 Ω instead of 50 Ω. To achieve the required 75 Ω of real impedance, two inductors of 67 pH are placed in parallel at the LO differential input ports. One time fixed the input impedance and the available LO power for the mixer it is possible to start the build of the RF and IF matching networks. As for the LO power, as shown during the design of the VCOs (3.2.2), the carrier generator can deliver up to +2.5 dBm as maximum differential LO power. Despite this value of the LO signal, a more reasonable value of 0 dBm was chosen for the RF matching network. This choice has been done in order to have a mean value of power in the whole band of interested band. As shown in 3.2.2, the delivered power rises from -4.5 dBm at 57.5 GHz up to +2.2 dBm at 60.25 GHz. With a large signal analysis (Periodic S-Parameters: PSP in Cadence) it is possible to evaluate the behavior of the RL for the IF and RF ports. In Figure 70 the behavior of the differential ports with different values of injected LO signal is reported. As shown in Figure 70, the influence of the LO power is extremely strong and the control of the injected signal into the switches is mandatory. As established above, a 0 dBm of LO power is chosen as reference for the design of the matching networks.

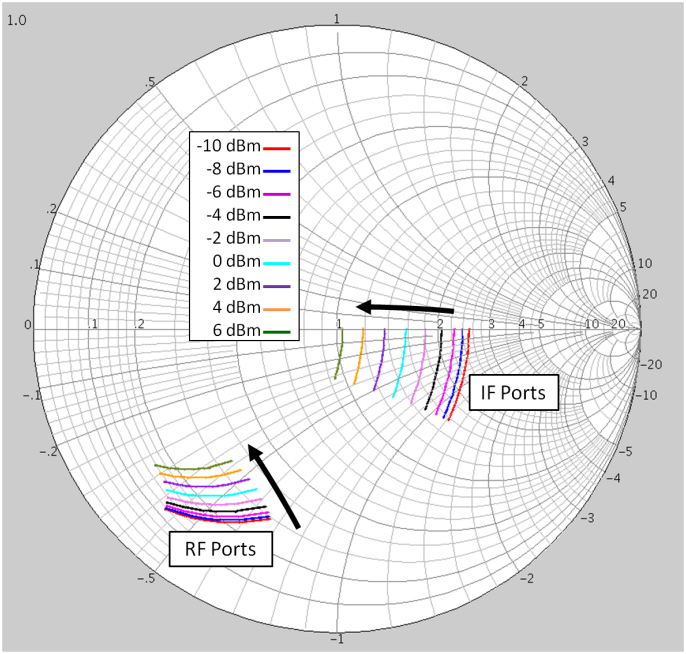

Figure 70: Influence of LO power in IF and RF matching network ports.

The Periodic S-Parameters (PSP) simulation of the mixer shows an impedance of $11 - 21j\ \Omega$ for the RF ports at 60 GHz and, as a consequence, the 50 Ω matching can be obtained by placing a shunt inductor of 62 pH at the output of the RF matching network. Concerning the impedance of the IF port, for a LO signal of 0 dBm the impedance is not too far from 50 Ω (75 Ω), therefore, being the frequency

too low and the bandwidth too large for a simple lumped component matching, it has been chosen to left the IF port without the impedance matching circuit.

3.1.4 *Measurements*

The measurement campaign for the mixer starts with the test of the RF and IF return loss. In order to verify the performance of the mixer a standalone circuit is realized (in Figure 71). To transform the single-ended LO signal in the

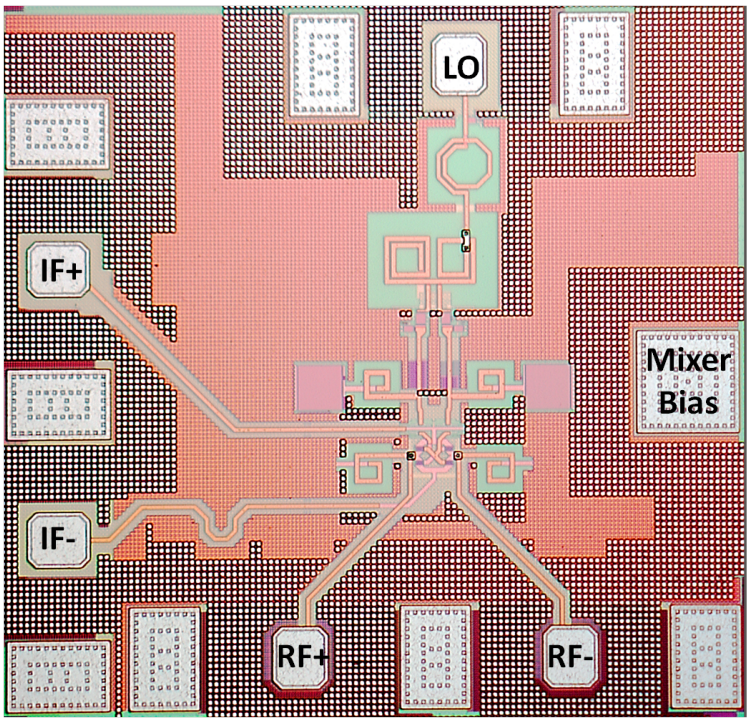

Figure 71: Chip of the mixer

differential one, the balun shown in Section 2.3.1is employed. The measurements of the differential ports are performed using a 4 port PNA-X by Agilent. Figure 72 shows the obtained results. The RL of both the differential ports have been acquired at different LO power value in order to verify the behavior of the mixer. In this direction the measurement confirm the hypothesis obtained by simulation. On the other hand, the absolute value of the impedance achieved during the measurement is different from the expected value. By the help of retro-simulations it has been possible to discover a different value of impedance at the RF port. By removing the effect of pads, interconnections line, and inductance, the real impedance on the RF moves from 11-j*21 Ω (obtained by PSP simulation) to 5-j*28.7 Ω. This inconvenient on the matching network design can be addressed to the particular state of the MOS constituting the mixer. In this case, the 4 switches are unbiased in terms of drain source voltage and, in this circumstance, the MOS

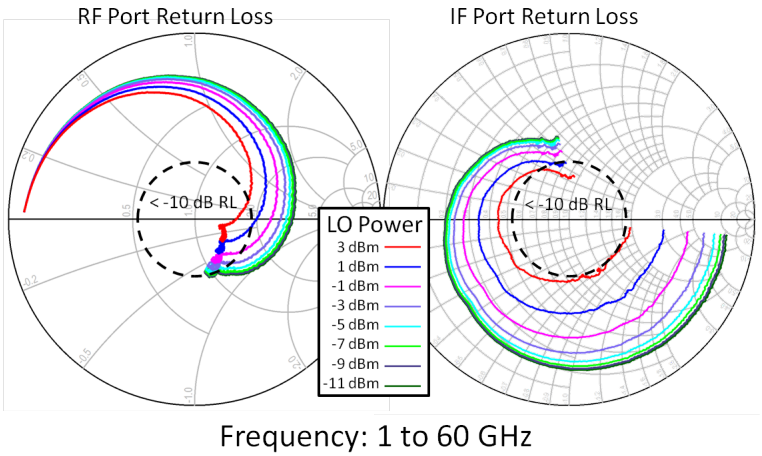

Figure 72: Return loss for IF and RF ports

work with their bias point placed in the origin of the I/V characteristic. For this reason it is possible that the BSIM model of transistor has some problems to represent the transistor response with high precision. As happened for the RF port, also the IF port shows discordance in impedance value. In this case, the real part of impedance diverts to higher value. Despite the impedance variation, the measurements show good value of impedance matching, in particular for the RF differential port. For 0 dB of LO power the RF ports shows a RL better than -10 dB from 53 GHz up to 67 GHz. On the other hand, the IF ports show a degradation of the performances with a RL higher than -5 dB.

Concerning the frequency conversion performances, the best conversion loss achieved by the mixer is -9 dB. The measurements presented in the first plot of Figure 73 represent the C_G for the required LO power (0 dBm) with an IF frequency sweep starting from 100 KHz up to 6 GHz. In the second plot, instead, the C_G is measured for different IF frequencies at different LO carriers. The effect of LO power on the mixer performance can be summarized by Figure 74. The result shown in this picture underlines one more time, the importance of the control of the LO signal value. The conversion gain rises with a gradient of more than 20 dB/ dec in the range of -13 to 0 dBm for the LO signal magnitude. The rise of power on the carrier improves the switching capability, assuring better condition of ON/OFF states and, at the same time, the IF / RF return loss must be controlled by an adequate matching network. Finally, for the large signal behavior, thanks to the wider switching transistors, the mixer shows a higher compression point compared to the other device on the state of the art. Figure 75 shows the trend of the output power of the mixer obtained with a 0 dBm of LO and 58 GHz of LO carrier and 500 MHz of IF signal. Following the previously described design procedure,, the performances of the passive mixer are strongly improved. By comparing the proposed mixer to the state of the art architectures, the difference is huge: the output compression point (OP_{-1} dB), obtained as the

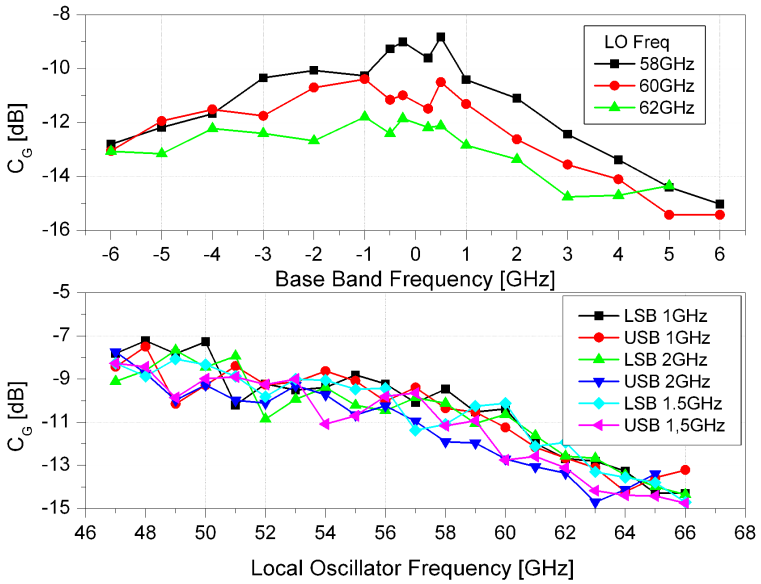

Figure 73: Mixer Conversion Gain

sum of C_G and $IP_{-1}dB$ in [66] is -19 dBm while for the proposed one it rises until -9 dBm. Therefore, the proposed circuit passes the existing state of the art with a difference of 10 dBm in terms of output compression point. For the same reason also for the active device as the Gilbert cell, the performances becomes comparable. In [67] the $OP_{-1}dB$ is 5.5 dB better than our proposed mixer but at the price of 24 mW of power DC consumption. To resume and compare the performances of the presented mixer with the other circuits in the state of the art, Table 5 summarizes the different topologies of 60 GHz homodyne mixers in CMOS technology.

3.1.5 *Conclusion*

The power performance of the upconversion mixer is the most important feature shown by the presented structure. The capability to transfer at mm-wave frequency high value of base band power allows reducing the number of power stages after the up conversion block. In this way it is possible to use smaller power block, thus reducing the power dissipation attributed to the low efficiency of the power amplifier in the 60 GHz frequency band. The output compression point of the mixer assumes relevant importance in order to reduce the waste of energy in the power hungry front-end amplifiers. The mixers resumed in table 5 represent the state of the art of V-band architecture. The most important parameters described in this table compare the OP-1dB to other parameters like the power dissipation of the block and the LO power level required to work. This latter parameter can assume a relevant importance because, if the mixer needs high value of LO power, the problem of energy efficiency in the LO driver buffer could represents

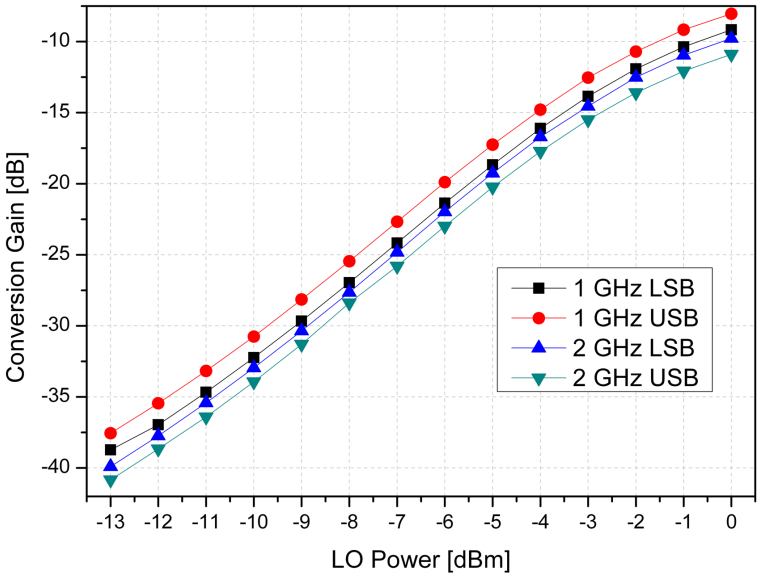

Figure 74: Conversion Gain versus LO signal power

a criticism into the system design. An overview on the Table 5 shows that the highest OP-1dB value the work of F. Zhang [71] with only -3.5 dBm. However, this mixer, based on the Gilbert architecture, consumes 24 mW of DC power compared to the 0 mW of the passive topology. In this field the work of J.H.Chen represents the state of the art of the passive mixer with an OP-1dB of -10.5 dBm and 0 mW of power consumption. The only but very big drawback of this structure, however, is the LO power needed to drive the switching ring. The 10 dBm of LO power constitute a consistent dissipation of energy in the LO chain. Referring to Table 2 , at the end of the voltage controlled oscillator (VCO) section, this power level is about one decade higher than the state of the art of 60 GHz VCO. Thus, to yield the required 10 dBm, a real power amplifier is needed between the VCO and the passive mixer and the total energy efficiency is drastically reduced. Otherwise, the optimization process, explained in these pages, has allowed the proposed passive mixer to be characterized by a good OP-1dB, a very good C_G (if compared with the family of passive mixers), a reasonable LO driver signal, and a zero power dissipation.

3.2 VOLTAGE CONTROLLED OSCILLATOR

The voltage controller oscillator discussed in this section represents the evolution of the first prototype developed by M. Kraemer during his Ph.D [18]. The VCO is based on the Colpitts architecture and exhibits very good performance in terms of power consumption and efficiency. The VCO version exposed in the next pages has been inspired by the guidelines left from M. Kraemer in his Ph.D manuscript thesis and from the increased power required to drive the passive up conversion

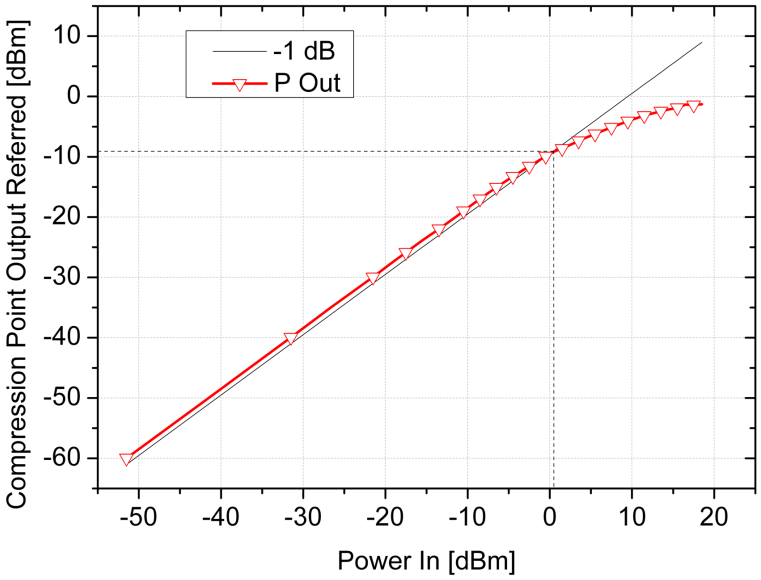

Figure 75: Mixer -1dB output compression point

mixer shown in the previous section. The new version of VCO maintains the original architecture as the matter of its resonating cell. The circuit redesigns has mainly interested the output stage of the oscillator with a considerable improvement of the delivered power preserving a reduced power consumption. Table 6, at the end of this section, summarizes the state of the art of the most representative VCOs in the 60 GHz band.

3.2.1 *First Version of the VCO*

The core of the voltage controlled oscillator (VCO) employed in the framework of this thesis has been developed as first instance in [18]. In the next pages a brief summary of the VCO designed in [18] will be discussed in order to contextualize the modifications added by the redesign of the circuit presented in this thesis and reported inthe final part of the section. The circuits developed in this thesis work have to meet reduced power consumption requirements. However, for the design of oscillators with reduced power consumption the output power is equally important, because mixer performance increases with local oscillator power. In order to minimize transceiver power consumption, the VCO's efficiency has to improve. CMOS VCOs operating around 60 GHz regularly exhibit quite low output power. The most powerful designs in bulk CMOS arrive to show P_{out} of -4 dBm in [75] or, even worse, P_{out} of -6.6 dBm in [76]. Thanks to the use of a differential common-source Colpitts architecture [77], which was not yet used for CMOS oscillators operating in the 60GHz band, a record efficiency of up to 4.9% and a record output power of up to -0.9 dBm is achieved. A large majority of the 60GHz CMOS VCOs uses the differential cross-coupled

Reference	Topol.	IF [GHz]	RF [GHz]	C_G [dB]	P_{LO} [dBm]	OP-$_{1dB}$ [dBm]	P_{DC} [mW]
[68]	Gilbert	1-5	60	-4	N.A.	N.A.	70
[69]	Resist.	1-5	60	-13.5	8.7	-19	0
[66]	Gilbert	11	51	-11	0	-10	13.2
[70]	Sub-harm.	0	60	-6	7	-19	75.9
[71]	Gilbert	1	63	4	0	-3.5	24
[72]	Sub-harm.	2.5-5.5	63	5	5	-5	92.2
[73]	Gilbert	10	60	-6.5	5	-18	29
[74]	Gilbert	0-3.5	60	-5.6	N.A.	-19.6	8.6
[67]	Resist.	0-5	50	-14.5	10	-10.5	0
[59]	Dual-gate	0-3	64	-2.4	6	-15.5	23
This work	**Resist.**	**0-10**	**60**	**-9**	**3**	**-9**	**0**

Table 5: State of the art for up-conversion mixers

architecture. To allow frequency tuning, a part of the tank capacitance is made of MOS-based varactors. The proposed VCO, instead, makes use of an alternative architecture based on a differential common-source Colpitts VCO [77]. To the best of the author's knowledge it was not yet employed in the 60 GHz band. The simplified schematic of the circuit is given in Figure 76 . The chosen architecture can be considered as the extension of a cross-coupled oscillator by capacitive voltage dividers. The transistors are used in a common source configuration which inverts the signal. Hence, the output signal is fed back from the other half of the differential circuit, where the drain voltage is available at inverted polarity due to odd-mode operation. The key differences between the proposed Colpitts VCO and a cross-coupled VCO are illustrated in Figures 77: 77a shows that the cross-coupled VCO's gate voltage is just an inverted version of its drain voltage, implying that gate bias voltage and supply voltage are identical. In the case of a large voltage swing, the gate voltage deviates considerably from its initial (already non-ideal) bias point. As a consequence, the transistor is providing less transconductance than at the bias point, eventually even entering the triode region. This limits the drain voltage swing at which a cross-coupled VCO can provide sufficient negative resistance to further increase the oscillation amplitude. In the case of the proposed Colpitts VCO, the capacitive connection between gate

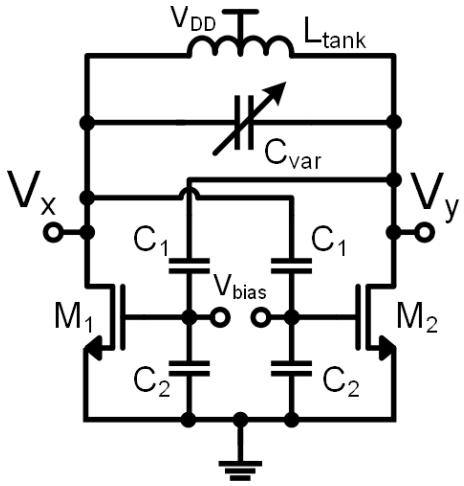

Figure 76: Voltage Controlled Oscillator core

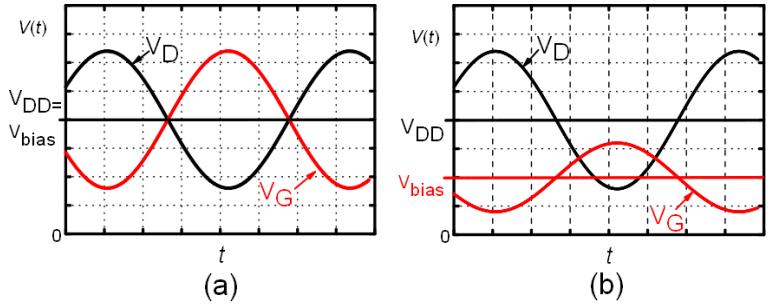

Figure 77: Gate and drain voltage in (a) cross-coupled and (b) proposed oscillator.

and drain allows to independently choose the gate bias voltage as illustrated in Figure 77b. Hence, the drain current density of the transistors can be chosen arbitrarily, and the optimum bias points can be selected. Because efficiency is the main issue here, a current density of around 0.3 mA/µm, which maximizes the transistor's linearity, is set. Alternatively, to minimize the noise contribution of the transistors, the minimum noise current density of around 0.15 mA/µm may be selected. The gate voltage swing observed in Figure 77b is C1/(C1 + C2) times the drain voltage swing (in the illustration is ≈0.5). Thus, the transistor's gate voltage stays close to the initial bias point. But, compared to the cross-coupled case, a Colpitts VCO requires wider transistors: this is because the capacitive voltage division also reduces the negative resistance that is added to the tank per micron of transistor width. The transistors used in the proposed VCO are general purpose (GP) devices composed of 14 fingers with 1 µm width. However, as the drain current density of the transistors is much lower than in the cross coupled case, power consumption does not increase. The higher linearity provided by these larger transistors can be exploited to achieve a higher output power, and thus increase efficiency. In order to further maximize voltage headroom and minimize phase noise, the usual tail current source is replaced by a tail inductor L_{tail}. Its

size is chosen to resonate with the transistor's parasitic source-bulk capacitances in order to filter the second harmonic of the oscillation frequency. Finally, the proposed common-source VCO has the advantage of a potentially higher tank voltage swing and thus linearity. This is due to the fact that it connects the tank to the transistor's drain rather than to its gate and source. The disadvantage of the proposed solution however is that the oscillator's output and the tank share the same terminals: the attached load has thus an influence on the tank impedance. To minimize this loading of the VCO core and to allow the driving of a differential 100 Ω output, common drain buffers are used. The buffer transistors are 65 nm GP devices with 14×1 µm channel width. Figure 78 shows the complete

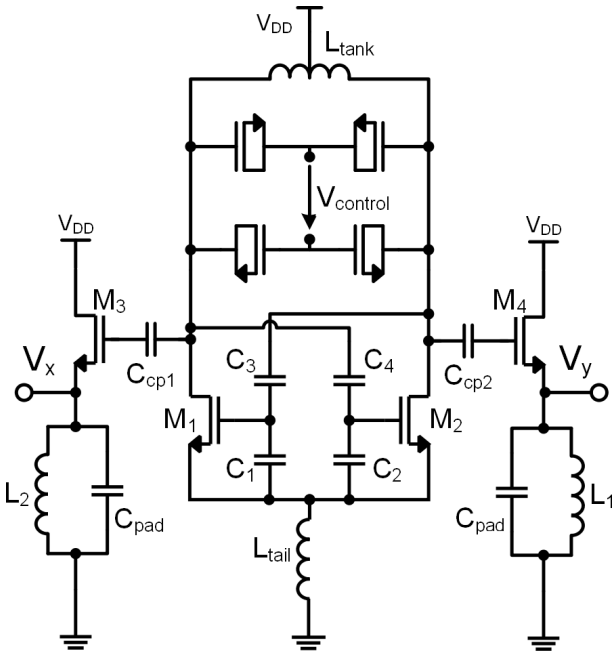

Figure 78: Voltage Controlled Oscillator plus buffers.

scheme of VCO block. Once the architecture and bias point of the VCO are fixed the component values (L_{tank}, C_{var}, C_1, C_2) and transistor widths ($W_1 = W_2$) have to be found. L_{tank} represents the tank inductor and C_{var} the varactors. C_1 and C_2 are the capacitance of the capacitive voltage divider constituted of MOM capacitors. The remaining parasitic capacitance (originating from inductor, transistors and buffer amplifiers) will be incorporated in C_{par}. The loss associated to each of these elements is represented by parallel admittances gm. Concerning the tank inductor, L_{tank} is connected with both ends to the resonator therefore, its differential performance is more important than its single ended behavior. This has consequences on the optimization of the spiral dimensions in order to obtain a high Q-factor at the specified resonance frequency 60 GHz: a slightly larger metal width than in the case of single ended excitation, as well as shunting of the two topmost thick metal layers is advantageous in this case. Figure 79a shows

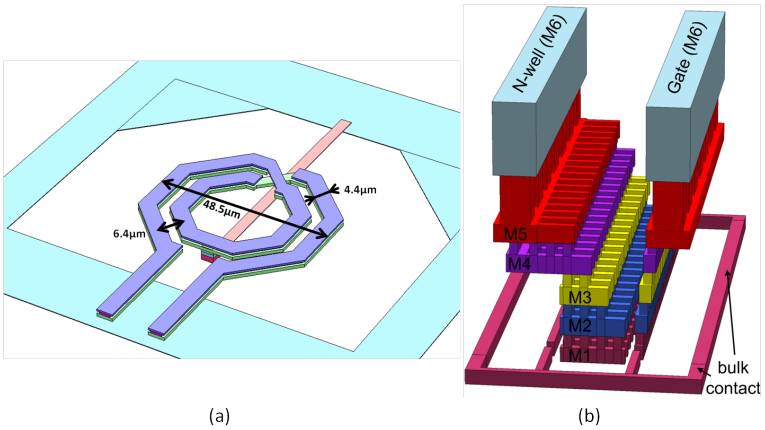

Figure 79: (a) Tank inductor; (b) metallization contact of varactors.

the synthesized inductor in the 3D model in Sonnet Simulator. To limit power consumption, L_{tank} is chosen to be 155 pH. This value is considerably larger than the minimum value possible (which would minimize phase noise). The tank inductor's differential Q-factor is 19.1 at 60 GHz, while the single-ended peaks at that frequency with a value of 14.5. To complete the resonating cell 4 accumulation MOS (AMOS) varactors are used to change oscillation frequency. Each of them has a capacitance ranging from 8.4 to 12.7 fF. They are differentially tuned in order to reduce phase noise. The full-custom AMOS varactors are realized by placing an n-channel MOSFET into an n-well. A multi-finger layout is used (Figure 79b). The finger width is 0.78 µm, while relying on GP devices with minimum channel length. Figure 79b shows the 3D model of varactor with the metal contacts.

The first version fabricated VCO it was characterized on-wafer, using a R&S 67 GHz spectrum analyzer for frequency, power and phase noise measurements. The measurement was done in a single ended configuration while the other one output was terminated by a 50 load. Corrections for cable loss are applied. The VCO is tuned by a differential voltage $V_{control}$, The oscillation frequency reaches from 57.58 to 60.80 GHz, which corresponds to a frequency tuning ratio (FTR) of 5.4%. The VCO's phase noise is decreasing when increasing the frequency of oscillation. The phase noise at 60.77 GHz, achieves the minimum of 90.3 dBc/Hz at 1 MHz offset. Phase noise lies around -86 dBc/Hz @1 MHz over the Frequency Tuning Ratio (FTR), with a maximum of -83 dBc/Hz @1 MHz at 57.6 GHz. The main feature shown by this VCO is its highest output power the maximum achieved value is -0.9 dBm at 60 GHz.

3.2.2 *VCO Redesign*

The second version of the VCO, proposed in the following pages, improves some weaknesses of the previously discussed VCO. In the circuit proposed in Figure 78 a pair of source follower amplifiers is employed as buffer. The principal issues

detected in this configuration are the unitary gain and the reduced feedback isolation ($S_{1,2}$). In effect the source follower stage plays the role of impedance matching block between the VCO core and any other 50 Ω possible blocks (probes during the characterization step or mixers in the transmission/reception chains). Concerning these disadvantages, the zero gain of the amplifier concurs in the reduction of the total energy efficiency of the block and the lowest feedback isolation influence the load value seen by the VCO core with consequences on the nominal value of frequency oscillation. As a result of these considerations, the topology of the output amplifier has to be revisited. In order to improve the feedback isolation and, at the same, time increase the power efficiency of the block, a Cascode amplifier is exploited as buffer at the output of the VCO core. The scheme of the buffer and the optimization technique here used is the same employed to design the Buffer block described in Section 3.3.

The scheme of the new VCO is represented in Figure 80 whereas the micropho-

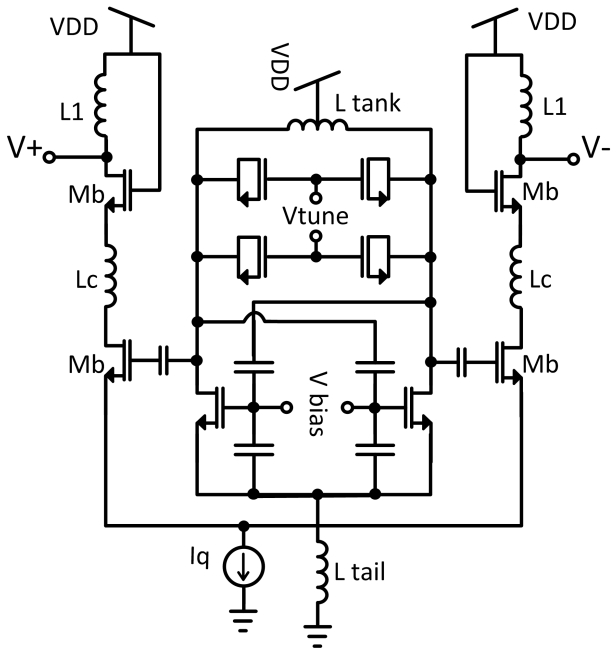

Figure 80: Schematic of the redesigned VCO

tography of the realized circuit is reported in Figure 81.

3.2.3 *Measurements*

The VCO has been characterized on-wafer using: an Agilent PNA-X vector network analyzer to measure the output return loss, a R&S 67GHz spectrum analyzer for frequency and phase noise characterization, and a Agilent E4416AZ power meter for the output power measurements.. The bias, supply and tuning voltages are connected using an eye-pass probe of 100 µm pitch placed upper the 6

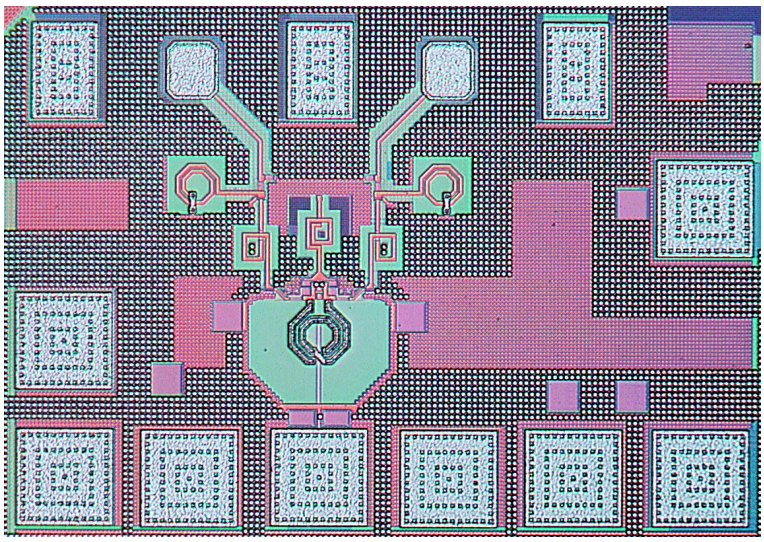

Figure 81: Microphotograpy of the second version of VCO

pads in the bottom of figure 81. Each tip is equipped with a 10 µF decoupling capacitor connected to ground in order to kill parasitic RF components. The VCO is tuned by a differential voltage $V_{control}$, applied by two voltage sources with $VDD \pm V_{control}/2$. With the exception of the VNA that it is connected at both of differential pads, the spectrum analyzer and the power meter are connected to one of the VCO's outputs, while the other output is terminated by a 50 Ω precision load. Corrections for cable loss and single-ended measurement (in total around 9 dB to 11 dB, depending on the cables used) are applied.

S-Parameters measurements

The small signal measurements to verify the output impedance of the VCO shows an improving in the whole band of interest (57-63 GHz). Figure 82 compares the measured curves with those of the previous version. The new version of VCO exhibits an improvement of 5 dB in the RL coefficient upon the upper side of its band. Observing the trend of the curves, the different nature of the output buffers and their matching networks are remarkable. The old version offers a wider 50 Ω band but in the 60 GHz region the response is degraded. This behavior is probably due to the underestimation of parasitic capacitance of the pads. In the old version of VCO the pads capacitance resonate with a grounded inductor, as shown in Figure 78. In the new version of VCO the problem of the capacitive effect of the pad is less dangerous. The output matching network of the Cascode buffer, in fact requires, a ground capacitance to match the 50 Ω, and simulations confirms that the small parasitic capacitance (estimated to be less than 30 fF) does not cause high variation in the functioning of the circuit. To completely remove the effect of the pads and of the 50 Ω coplanar wave guide the same de-embedding method proposed in [34] is used. Finally, it is worth to note that the unwanted

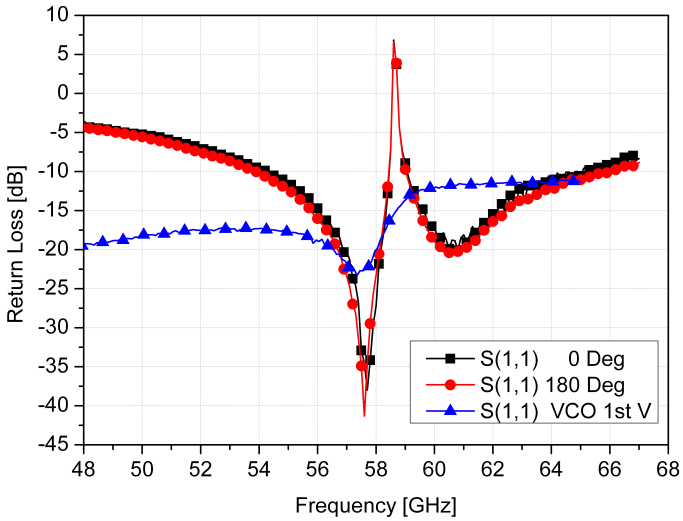

Figure 82: S Parameters measurement of the VCO differential ports

spike centered at 58.60 GHz is basically due to the carrier of the VCO running during the measurements session.

VCO Frequency sweep and output power

The measurements to characterize the VCO in terms of maximum output power and frequency sweep have been obtained in the same measurement session. Exploiting the differential outputs of the VCO, the power meter is connected at the first output, whereas the R&S spectrum analyzer occupies the second output port. In this manner, is possible to measure at the same time the nominal value of the carrier frequency and its intrinsic power by calibrating the sensor of the power meter at the right frequency. Figure 83 represents the spectrum of the carrier at its maximal oscillation frequency. The values are de-embedded from cable, dc block and probes losses. The VCO frequency tuning ratio remains unchanged compared to the previous VCO version because the core of the circuit has not been modified. The different value of coupling capacitance used to connect the new architecture of the output buffer reduces the capacitive influence of the buffer and, then, the 5.4% of FTR is maintained and still improved by means of several tens of MHz added at the lower and upper oscillation frequencies. The power delivered in the whole band of interest is described in Figure 84. The Cascode output amplifier, with its intrinsic gain, improve the performance of the VCO maintaining very low power consumption. In Figure 84 the comparison between the two versions of VCO is widely in favor of the newer version. The new configuration guarantees a larger -3 dB band with 2.8 GHz (58 to 60.8 GHz) versus 2 GHz of the older one. In particular, the new version seems to contrast the power drop caused by the turn off of the VCO in the lower part of the frequency band.

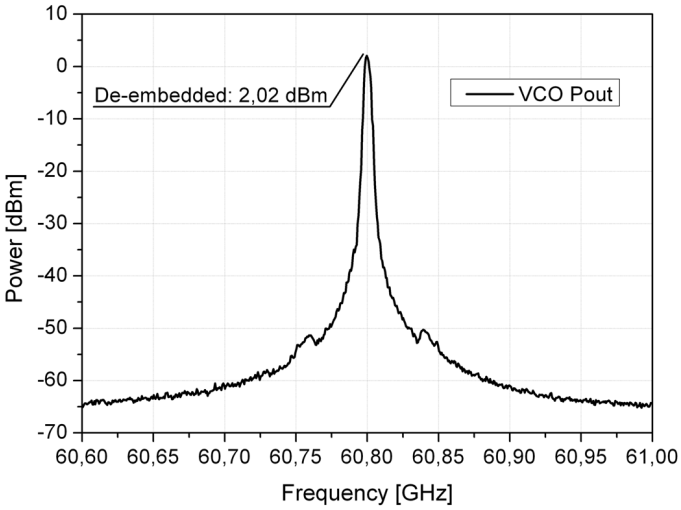

Figure 83: VCO carrier spectrum

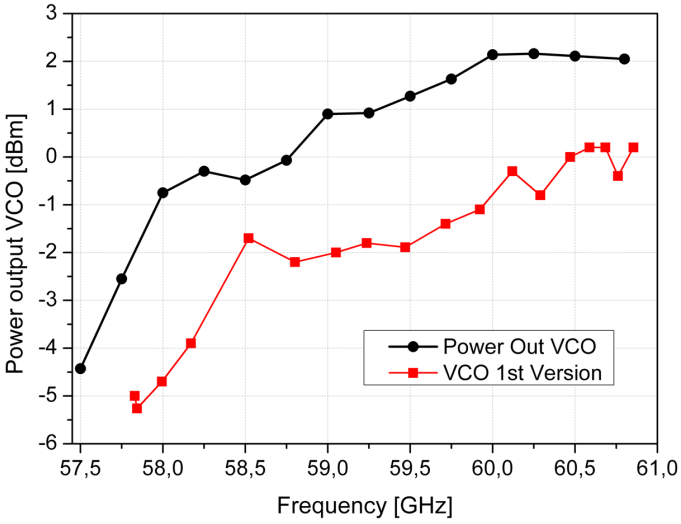

Figure 84: VCO output power

Phase noise measurements

As occurs for the previous VCO version, the phase noise does not constitute the key feature of the developed oscillator, however, it is important to achieve a sufficient spectral purity of its output signal. After measurements made with a R&S spectrum analyzer the obtained value are not so far from the [78] version. Figure 85 shows the measured phase noise of the VCO over its band of operation

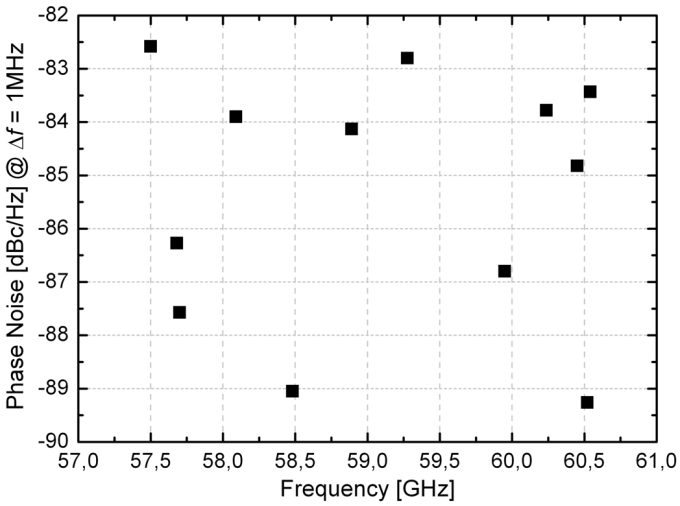

Figure 85: VCO Phase noise measurements

at 1MHz offset from the carrier. The range of values varies from -82.5 dBc/Hz to -89.5 dBc/Hz in the whole band of interest. The best phase noise measurement is obtained at 57.5 GHz that accidentally match with the minimum delivered power of the VCO. The phase noise at 10 MHz offset lies around -110 dBc/Hz at the same frequency.

3.2.4 *Conclusion*

Table 6 summarizes the performance of the implemented VCO in comparison to the literature circuits operating at 60GHz. The most energy saver designs are proposed by D. Huang, [80] and R. Genesi, [84] but they don't give any information about the power yielded at the output; this probably means that the carriers show very low amplitudes. However, the main feature for a VCO circuit is their efficiency, i.e., the capability to convert DC power into RF single tone. In Table 6 the efficiency is calculated as PRF/PDC. As the VCO [78], it shows a very high output power: 2.5 dBm as maximum RF value with only 22 mW of power consumption. In this condition, the efficiency of the block is almost doubled with 8.04% of power efficiency. As for the frequency tuning range the best performance is achieved in [81]; thanks to the use of optimized AMOS varactors, largest frequency tuning range is obtained. Finally, for the best phase-noise performance

Reference	Tech.	f_0 [GHz]	Ph. Noise	FTR [%]	P_{DC} [mW]	P_{out} [dBm]	Eff. η[%]
[79]	90 nm	77	-100.3	8.1	38	-13.8	0.11
[80]	90 nm	60	100.2	0.2	2	N.A.	N.A.
[81]	130 nm	56.5	-89	17.8	10	-10	1.02
[82]	65 nm	70.2	-106.1 @ 10 MHz	9.55	10	-35	0.003
[83]	65 nm	54	-118 @ 10 MHz	11.5	7	N.A.	N.A.
[84]	90 nm	53	-116.5 @ 10 MHz	3.77	2	N.A.	N.A.
[85]	90 nm	52	-95	6	20	N.A.	N.A.
[86]	65 nm	63.3	-85	10.5	80	-13	0.06
[87]	90 nm	64	-95	8.75	3	-11	2.51
[88]	65 nm	56	-99.4	17	25	-9.3	0.47
[78]	65 nm	59	-90.3	5.4	16.5	-0.9	4.93
This Work	**65 nm**	**59**	**-89.5**	**5.4**	**22**	**2.5**	**8.1**

Table 6: State of the art for 60 GHz VCO

the work described in [79] shows -100.3 dBc/Hz at 1MHz offset. Despite that, this oscillator works at a slightly higher frequency (77 GHz) than the others.

3.3 MID POWER BUFFERS

The design of the complete transceiver requires the use of buffers in order to maintain the amplitude of the signals within the predetermined levels of power. In order to attain to the strict constraint of very low power consumption, the buffers are optimized with the maximization of theirs power efficiency.

Buffer block design

To design the buffer, the Cascode architecture has been chosen in order to obtain good values of gain and, at the same time, to increase the feedback isolation of the block by exploiting the high isolation feature exhibited by this amplifier topology. In this manner, the buffers not only increase the power level of the RF chain but also they act as isolator stage to avoid undesired load/source influence between VCO and mixers. Another important feature required for the buffers design is a

relatively high level of linearity. In fact, the amplitude of the signals managed by these blocks cannot be considered as a small signal at 60 GHz and, therefore, the evaluation of the compression point of the block assumes the same relevance that the small signal gain expressed by itself.

The Cascode buffers are developed in two different configurations: single-ended and differential. The single-ended version is also characterized in a standalone block in order to verify its performances. The same buffer is also exploited at the end of the transmitter chain as small mid-power amplifier to restore the losses added by the balun or also to play the role of driver amplifier in presence of a true power amplifier at the end of the transmitter chain. The differential version of the buffers, instead, is designed to increase the power of balanced signals generated by the VCO or, as occurs in the transmitter chain in section 5.1.1, to restore the level of the RF signals at the output of up converter mixer.

In the differential configuration, a current mirror (as represented in Figure 86) imposes 11 mA of quiescent current (I_q) and works as high impedance stage in case of common mode parasitic signal into the buffer block. The common mode rejection ratio (CMRR) of the block is then increased as well as the performances of the entire transmitting chain.

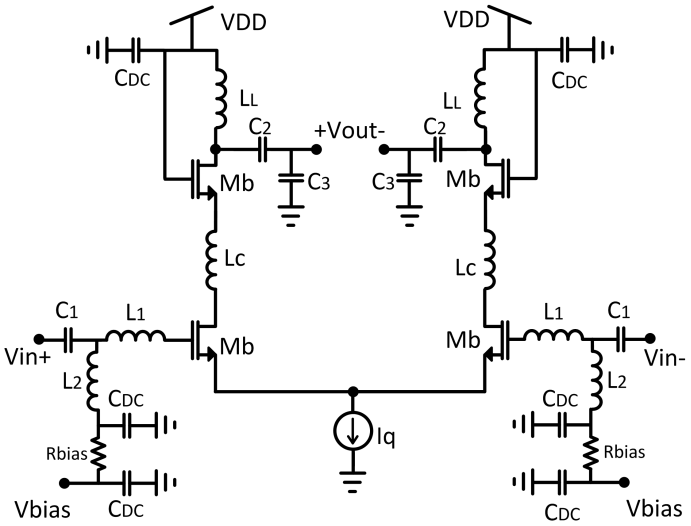

Figure 86: Schematic of the differential cascode buffer

Concerning the characteristics of the buffers, the Cascode configuration employs pairs of transistor with 22 µm of gate width. The devices are biased with 250 µA/µm to yield the maximum transconductance. As for the loads (L_L), high quality factor inductors have been exploited in order to reduce the resistive losses. The 153 pH inductor with octagonal shape shows a single ended Q of 16 in the whole band at 60 GHz. The L_C inductor is introduced, instead, between the two transistors of each chain to resonate with the parasitic capacitance inside the drain and the source of the M_b transistor. The resulting resonance improves the

maximal cut-off frequency (f_T) of the transistor and then increases the nominal gain of the buffer block.

The design of the input / output matching network has been performed following the double band matching network strategy. This approach is widely known in literature and allows obtaining a wider bandwidth through the sacrifice of a small part of the maximal achievable gain of the stage. In the proposed amplifier, the matching networks have been designed to resonate at 55 and 65 GHz respectively. By using this approach it is possible to reshape the curve of the maximal $S_{2,1}$ coefficient to expand the -3 dB band of the device. The matching networks are developed to match the 50 Ω in the standalone circuit represented in Figure 87 and, when necessary (as for the mixer IN/OUT ports), the impedance of the differential ports is 150 Ω (75 Ω in single-ended). The lumped component circuit employed to constitute the matching network are designed to minimize the total occupied area and, at the same time, minimize the losses by the reduction of R_L (intrinsic resistance of the inductors).

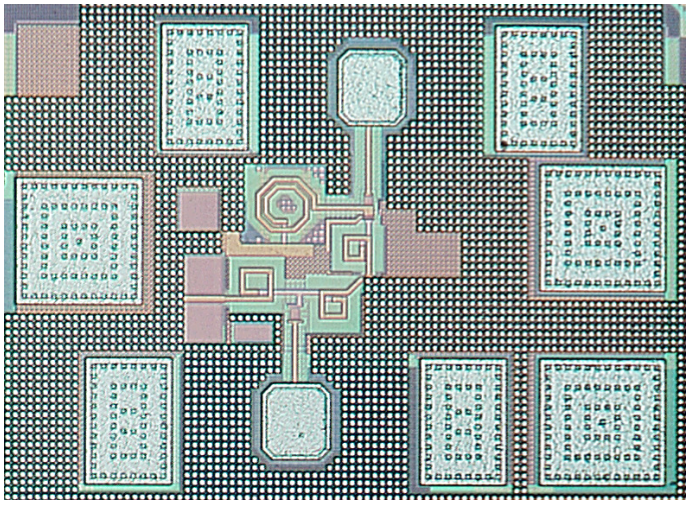

Figure 87: Standalone single-ended buffer

Measurements

The buffer has been characterized by Agilent PNA-X network analyzer. The results shown in Figure 88 highlight a slight shift of the matching network peak stowards lower frequencies. This response is probably due to small (unconsidered) interaction among the lumped elements of the buffer circuit; however, the expected performances of the circuit are maintained. The buffer exhibits a -3 dB band at least from 51 GHz to 67 GHz (the measurement setup does not allow higher frequency). The input matching network displays reflection coefficients lower than -10 dB in the band of 51-58 GHz and remains close to -9 dB in the upper frequency. At the output port, in the first part of the exploitable band, the behavior is slightly worse: $S_{2,2}$ coefficient growths up to -5 dB at 51 GHz, but it is higher than -10

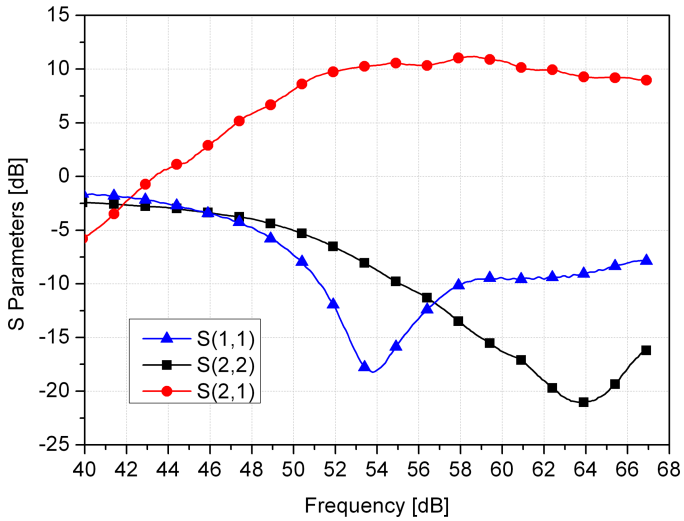

Figure 88: Measurements of standalone buffer

dB in the band from 55 GHz to the maximal measurable frequency (67GHz). The maximum transconductance gain of the amplifier exceeds the 11 dB at 58 GHz, whereas the measured input compression point is -11 dB at the same frequency allowing obtaining 0 dBm at the output of the amplifier.

The differential version of the buffer seems to confirm the performance discussed above. The presence of a current mirror at the bottom of the structure, however, reduces the maximum gain of the block of 2 dB (9 dB instead of 11). The input compression point is does not suffer from the presence of the current mirror and, consequently, it increases of 2 dBm. Therefore, the differential buffer block allows obtaining the +3 dBm as output power compression point.

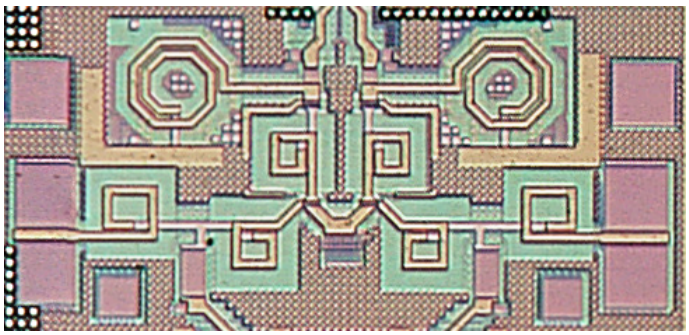

Figure 89: Differential Buffer

Figure 89 represents a portion of the differential buffer realized for the 60 GHz transmitter block.

BASE BAND ACTIVE STRUCTURES

4

VARIABLE GAIN AMPLIFIER

INTRODUCTION

Two versions of wide band variable gain amplifiers are presented and illustrated in this chapters. The main innovation proposed for the circuits is a new technique to increase the allowable pass band. Classical Cherry-Hopper topology is modified with a capacitive degeneration network to boost at higher frequencies the cutoff value in the transfer function of the single sub-block. Exploiting this design methodology, the variable gain amplifiers proposed yield a -3 dB band up to 2.5 – 2.7GHz. This value of cutoff band represents the state of the art performance for this type of components. Among the novel communication systems the ultra low-power Impulse Radio UltraWide Band (IR-UWB) (impulse-radio ultra-wideband) and UWB-Orthogonal Frequency Division Multiplexing (OFDM) (orthogonal frequency division multiplexing) are the most attractive solutions to create high data rate links. When using the UWB radio for the wireless streaming of audio between, for example, a smartphone and an HI-FI system, the battery lifetime of the first will increase by over 3 times compared to a conventional Bluetooth-based solution. In contrast to the Bluetooth communication, the UWB radio will not suffer from interference due to other wireless technologies that operate in the same location and in the same frequency band. IR-UWB systems are especially suited for short-range (< 20m) communication. The large bandwidth improves the resilience against fades, resulting in superior communication reliability. This is particularly true if compared to narrowband solutions, which tend to lose signals in surroundings with reflective surfaces and multi-path propagation. Also, spreading information over a wide bandwidth decreases the power spectral density, thus reducing the interference with other systems and lowering the probability of interception. UWB is also suitable for positioning sensors: the reflection of the wide-band signal allows for centimeter-ranging positioning accuracy. Both the reduction of the pulse duration and the increment of the carriers' number increase the capacity of the channel; on the other hand, also the occupied frequency band that have to be managed by the base-band (BB) circuitry increases. To moderate the enlargement of the frequency band caused by request of more and more higher bitrate different techniques have been investigated. For example in the IR-UWB standard different pulse shaping methods are proposed in literature. The improvements on the signal generation have increased the bitrate maintaining reduced range of occupied band. The VGA presented in this paper, instead, is designed for applications that need a total bandwidth higher than the classical frequency range. The requirements for this amplifier are 2.5 GHz of band starting

from DC. The main challenge in this design is to obtain a very flatness response for the VGA upon multi octave frequency band. Contrary to the high frequency blocks where usually the engaged fractional band is much times lower than the unity in the VGAs stages the UWB design is a serious issue to solve. Classical VGA structures are characterized by reduced passband, especially when they are composed of multiple stages [89]. The circuits proposed in these pages show up to 2.7 GHz band and 50-56 dB of dynamic range. In the following section the problem of the broadband VGA design is treated.

4.1 BROADBAND VGA DESIGN

Typical VGA architectures are characterized by a very wide dynamic range (50 to 75 dB) [5-8]. These performances can be reached only by using cascades of more amplifiers stages. The use of a large number of stages, however, entails a reduction of the entire system passband. To estimate the allowable bandwidth of each sub-block the transfer function $H(s)$ of the amplifier must be evaluated.

$$H_i(s) = \left(\frac{A_0}{1 + \frac{s}{f_{T_0}}} \right) \tag{4.1}$$

$f_{T_0} = (R_{out} C_L)^{-1}$ is the -3dB cut off frequency of the i^{th} stage. R_{out} is the output resistance of amplifier and C_L is the load capacitance. The total gain for a chain of N amplifiers is the product of their $|H_i(s)|$. The available bandwidth f_T is calculated using the formula proposed by [90]:

$$f_T = f_{T_0} \sqrt[N]{\sqrt{2} - 1} \tag{4.2}$$

The VGAs proposed in this paper must yield a f_T of 2.5 GHz, with a maximum gain of 50 dB which results with a cascade of 4-5 identical amplifiers. Reversing the Equation 4.2, the band demanded at each stage inside the chain exceeds a value of 2.6 times the value of $f_T 0$ i.e. 6.5-7 GHz.

Broadband Techniques

To satisfy the request of 7 GHz of bandwidth, classical configuration of resistive differential pairs are not adequate. The (R_{out}) and (C_L) parameters establish the maximal value of f_{T_0} as shown in Equation 4.1. The output resistance R_{out} derives from the design of the amplifier and it cannot be reduced without changing the entire system response. On the other hand C_L is a capacitive parasitic contribution coming principally from load (normally constituted by the gate of another transistor) but also from the drain-bulk capacitance of the MOS that constitute the amplifier itself. The capacitor is useless and harmful for the response, therefore, it is recommended to minimize its effect.

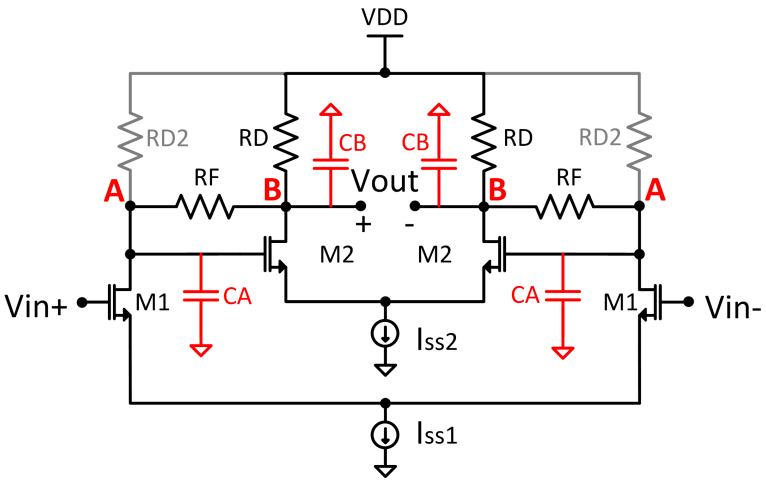

Figure 90: Cherry-Hooper amplifier Topology

Several methods to increase f_T are present in literature, including: the inductive peaking [90], the capacitive degeneration [90], and the use of the Cherry-Hooper amplifier in the VGA design [89, 91, 90]. The inductive peaking suppresses C_L making it resonate with an inductor. The pole-zero cancellation caused by resonance increases the f_T value of the amplifier. Unfortunately this method has two drawbacks. The high value inductor (order of nH) in RFIC technology occupies wide silicon surface and the voltage headroom due to their intrinsic resistivity precludes its use for CMOS technology with voltage supplies under 2.5÷3V. An active load can be used in the place of an inductor; however, its applicability for circuits with supply voltages of 1 - 1.2V, as the 65 nm CMOS technology, remains problematic. The voltage drop is caused by the stack of 3 transistors (active load, active transistor and current mirror stage). As a consequence the MOS trans-conductance (g_m) is greatly reduced and the amplifier gain as well.

The capacitive degeneration method, instead, is based on the use of $R_d - C_d$ circuit placed in the middle of the differential pair [90]. As result of this insertion the Bode diagram of g_m changes; moreover, when the product of $R_d C_d$ is equal to $R_{out} C_L$ a pole zero cancellation on the $H_i(s)$ increases the total available band. A sensible reduction of the total gain of the amplifier stage is the only drawback brought up employing this strategy.

The third and last solution is constituted by the Cherry-Hooper topology for the VGA design. Here the amplifier incorporates a feedback loop in its drain network. The aim of the counteractions is an improvement of the amplifier speed that increases the total f_T. The key advantage shown by the configuration proposed in Figure 90 is the reduced resistance at the transistors' drain (A and B points). The f_{T_0} of the single stage is increased by the reduction of the output resistance and the total gain of the stage is approximately $g_{m1} R_F 1$. In Cherry-Hooper's classical amplifier configuration the voltage headroom in M_1 transistor is unacceptable for low voltage technology. The sum $R_D + R_F$, with R_F particularly high, causes a drop

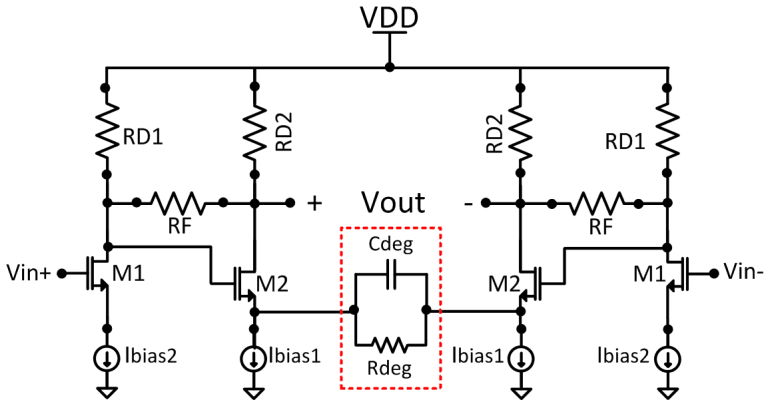

Figure 91: Figure 3. Modified Cherry Hooper amplifier

on the drain voltage that neutralizes the gain of the first stage. To overcome this issue a secondary path for the current bias can be placed among the supply voltage (VDD) and the drain of M_1 (R_{D2}). This version of customized Cherry-Hooper amplifier is widely used in broadband amplifier applications. The broadband response of this structure is an advantageous feature for the design of an UWB component. The calculations performed in previous section highlight the need to have a bandwidth of at least 7 GHz for each sub-block in order to satisfy the total available band of 2.5 GHz. In order to verify the performances of the circuit shown in Figure 90 a series of simulation have been carried out. The circuit show a good response compared to the classical common source configuration but, the 7 GHz requested in the analytical estimation are not reached.

4.1.1 *Active VGA Architecture*

The proposed design for the VGA is an evolution of the solution adopted by [89] and [91].The main innovation proposed in this paper is the combination of the Cherry-Hooper amplifier with the source capacitive degeneration. As previously described, the amplifier architecture reduces their R_{out} while the C_d contribute cancels out the zero imposed by the load capacitance C_L. Figure 91 describes in detail the modification made at the structure of Figure 90 to improve the bandwidth. In the dashed box are represented the $R_d - C_d$ circuit adopted as capacitive degeneration.

Simulation results show that with the new configuration the f_T in the single stage increase up to 8 GHz satisfying the bandwidth value asked by equation 4.2.

The main difference between the circuits in Figures 90 and 91 is the construction of the current mirrors. To place the $R_d - C_d$ cell it was necessary to split the current mirror of the differential pairs in 2 identical blocks in order to avoid the short circuit of the degeneration cell. The main drawback that arises from the change of the schematic is the decrease of the common mode rejection ratio (CMRR) of the

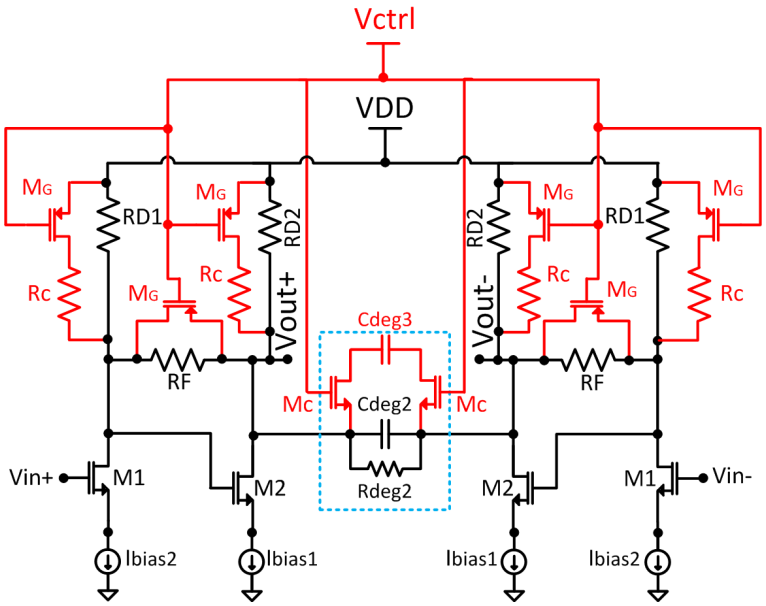

Figure 92: Final version of modified Cherry Hooper Amplifier

differential pair. Despite this, the benefits gained from the bandwidth increase are more valuable than the decrease of the Common Mode Rejection Ratio (CMRR) value.

In order to control the gain of each sub-amplifier component, a gain control sub-circuitry must be added to the circuit in Figure 91, which will be soon explained. From literature, the classical technique adopted to change the gain value in the Cherry-Hooper amplifiers is to modify the size of the resistance network R_{D1}, R_{D2} and R_F. The reduction of the nominal resistances values decreases or increase the total gain of the circuit. In the discussed architecture the principal parameter that influences the amplifier gain is the resistor R_F [90].

The strategy to change the component value and consequently to reduce the amplifier gain is attained by placing a second low impedance path (constituted by pMOS transistors M_G) in parallel to the R_F resistors. To improve the effect on the circuit response also the drain resistances R_{D1} and R_{D2} are shunted with a low resistance path constituted by the series of transistors M_G and smaller resistances R_C

Figure 92 shows the overall circuit of one sub-amplifier that constitutes the VGA. The components in red in this schematic represent the control gain network. The insertion of this secondary network on the amplifier circuit affects the response of the broadband circuit. The f_T of the circuit in Figure 92 drops of 1 GHz compared to the previous configuration in Figure91. The degradation on the response can be ascribed to the capacitive parasitic to ground of the pMOS transistors.

To contrast this effect a new capacitor C_{deg3} is placed in parallel to the existing component C_{deg2}. It is important to underline that the capacitive compensation

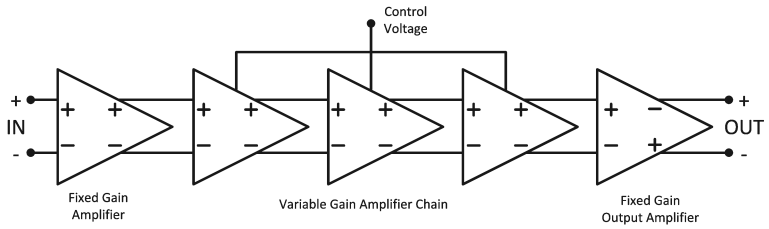

Figure 93: Active VGA configuration

is necessary only when the amplifiers work at the maximal gain. For this reason a nMOS pair is used to switch off the C_{deg3} path. If the capacitor remains active (without the nMOS), for small gain configuration the amplifier loses the flatness of its response increasing the gain in the 1-3 GHz frequency range. The high impedance path presented by the nMOS pair at low control voltages isolates the capacitor from the remaining part of the circuit. When a high gain is requested the control voltage V_{ctrl} rises up to 1.2 V, the pMOS are interdict and the nMOS are completely open. The effect of the capacitance C_{deg3} increase the response flatness and the parallel with C_{deg1} improves the frequency bandwidth.

The stand alone amplifier, represented in Figure 92 shows a max of 12 dB in high gain setup while it attenuates the signal until -5 dB in low gain configuration. The power dissipation for the single block is only 1.2 mA at 1.2 V of drain bias.

The proposed VGA system consists of 5 amplifiers stages, 3 of which with variable gain and 2, the first and the last of the chain, with fixed gain. The first and last stages are designed following the same scheme of Figure 92; in addition, the values of the devices inside the circuits were chosen to match with the impedance network of the RF front-end and the ADC/DAC circuitry. In particular, for the receiver chain, the first amplification block undertakes the impedance matching and in the same time fixes the value of bias point for the others stages of the VGA. The proposed VGA in fact, is DC coupled with the remaining part of the receiver chain. This choice has been done to avoid the presence of big decupling capacitors. The typical high pass behavior of AC coupled circuits is undesired for the aim of this RF front end. In particular for the OFDM-UWB technique the high pass response of the BB circuitry must be kept lower than 10 KHz with respect to the minimal frequency to preserve the carriers' integrity. The capacitors' value to satisfy this request is too big (occupied area) in the domain of fully integrated CMOS system. The VGA output stage instead is characterized by a slightly higher output power in order to drive the analog to digital converter or the up-converter mixer more effectively. The first and in particular the last stage, as previously said, must comply with the further purpose of impedance matching. As a consequence, their power consumption is higher. The first stage consumes 1.4 mA at 1.2 V whereas the last stage 7 mA being the VGA power stage.

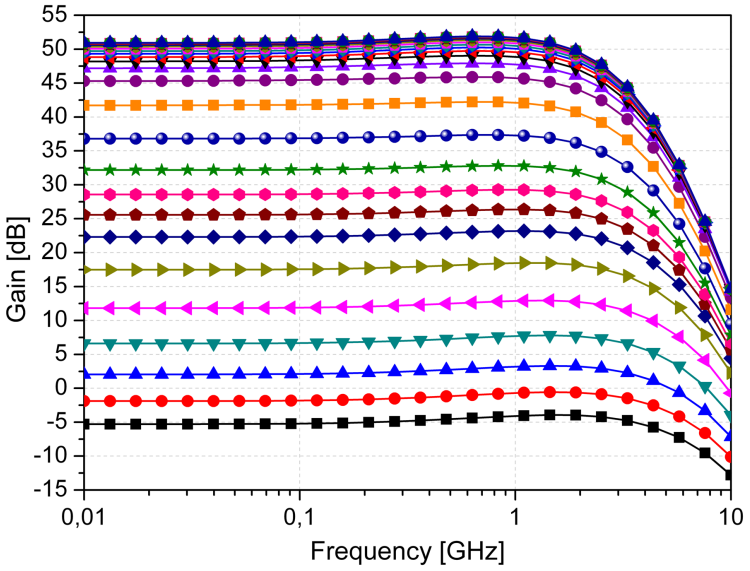

Figure 94: Simulated VGA frequency response for different fixed gains

The maximum allowable gain shown by the VGA is 52.7 dB with 2.52 GHz of f_T, whereas the minimum gain is instead -4.2 dB. Figure 94 shows the different curves of gain for 25 points of bias for the pMOS in the whole of 0-1.2 V.

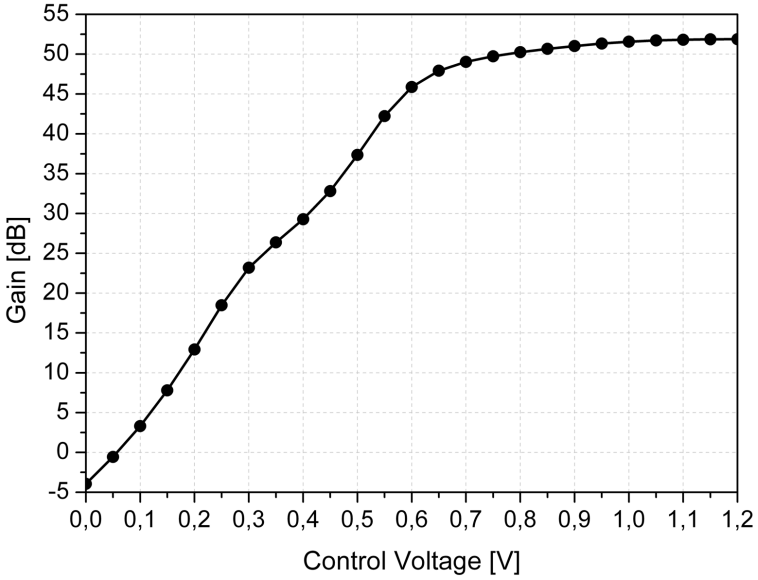

Figure 95: Figure 6. Gain variation for voltage gate sweep from 0 to 1.2 V

Figure 95 shows the VGA gain variation in function of the bias voltage imposed at the pMOS gate. As a consequence of the non linearity of the MOS response, the dynamic of the gain sweep is limited at the range of 0 to 0.8 V. Over this value the channel can be considered open due to the threshold voltage of pMOS

(≈0.73V). The maximal gain of 52.7 dB is however reached at 1.2 V of bias when the p-transistors gate is completely open and the positive value of the gate bias rejects the holes in the channel increasing the MOSFET OFF-resistivity and the switches isolation too.

4.1.2 *Passive VGA Architecture*

Attenuator

The passive version of VGA is inspired by the variable gain amplifier used in the audio systems. A passive block constituted by switching transistors and resistors are exploited to generate the attenuation on the coming signal when required. The passive attenuator circuit is an evolution of the work presented in [92]. The main difference inside of the proposed architecture is the differential nature of the signals. The attenuator proposed in [92] is composed by a single ended resistive block constituted by Π and T networks. In the low attenuation state, the nMOS transistors used as switches are completely open and they offer a reduced attenuation of the signals. In high attenuation state, the switches are open and the signal is forced to flow towards the resistance networks and it is strongly attenuated. Part of the signal is dissipated on the matching resistor and the remaining part is short-circuited to ground.

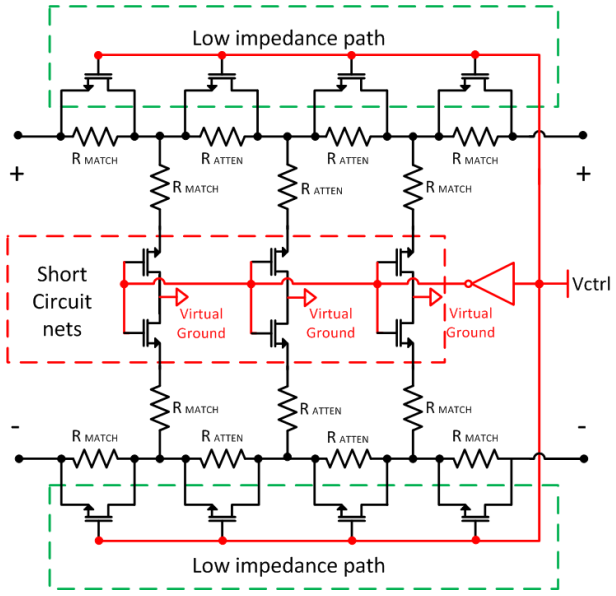

Figure 96: Balanced CMOS attenuator

The proposed version of differential attenuator, instead exploit the nature of the differential signals coming out from the downconverter mixer to improve the performances of the attenuator network. Figure 96 shows the circuit of the proposed attenuator. It is constituted by four switching steps. The switches are

made with 50 μm nMOS transistors. The transistors shape is identical them used in the upconverter mixer. The objective as it was for the mixer is to obtain high impedance in the off state and as lower as possible channel resistance when they are activated. In the shunt path, the short circuit networks constitute by pairs of transistors and resistors, erase the signals that flows in the resistor network when the low impedance transistors are open. The controlling signal in the short circuit network is, then, opposed in logic value to the main Vctrl signal (as the inverter block highlights in Figure 96). Therefore with the switches open in the principal path and the transistors on the short circuit network closed, in the shunt lines the counter phase signals are erased by thermal dissipation by the resistors. The principle at the base of this architecture is inspired to the shunt 100 Ω resistance placed at the output of Wilkinson power splitter devices. The total attenuation, consequently is strongly, improved as well as the final behavior of the VGA.

The doubling of short circuit transistors has been required for symmetry reasons. Despite the high symmetry achieved by the shape of transistors, with a single switch transistor in the short circuit path, the final response of the variable attenuator results unbalanced. Doubling the transistors (placed in Drain-Source-Source-Drain configuration) the signal at the output of the attenuator maintains the required symmetry.

The final configuration for the passive version of variable gain amplified is realized as Figure 97 shows. The active part of VGA is made with the modified Cherry-Hooper amplifiers shown in Figure 91. Exploiting this approach all bias variation along the amplifier chain is avoided (problem that occurs in the gain control of active amplifiers). In this way the gain of the total chain is controlled on the passive part of the circuit and the circuit robustness is enhanced.

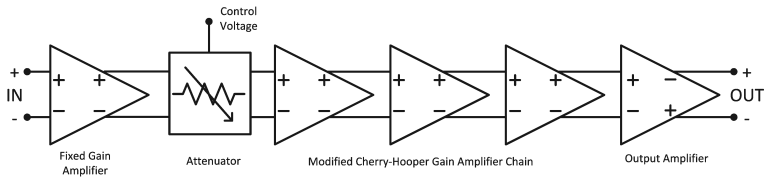

Figure 97: Passive version of VGA

4.1.3 *VGAs realization*

The two version of VGA and a prototype of attenuator have been realized in standalone chips. Figure 98 show the microphotography of the circuits.

4.1.4 *Measurement campaign*

The measurements of the VGAs, unfortunately, have highlighted an enormous weakness of the conceived circuits. The modified Cherry-Hooper amplifiers, as

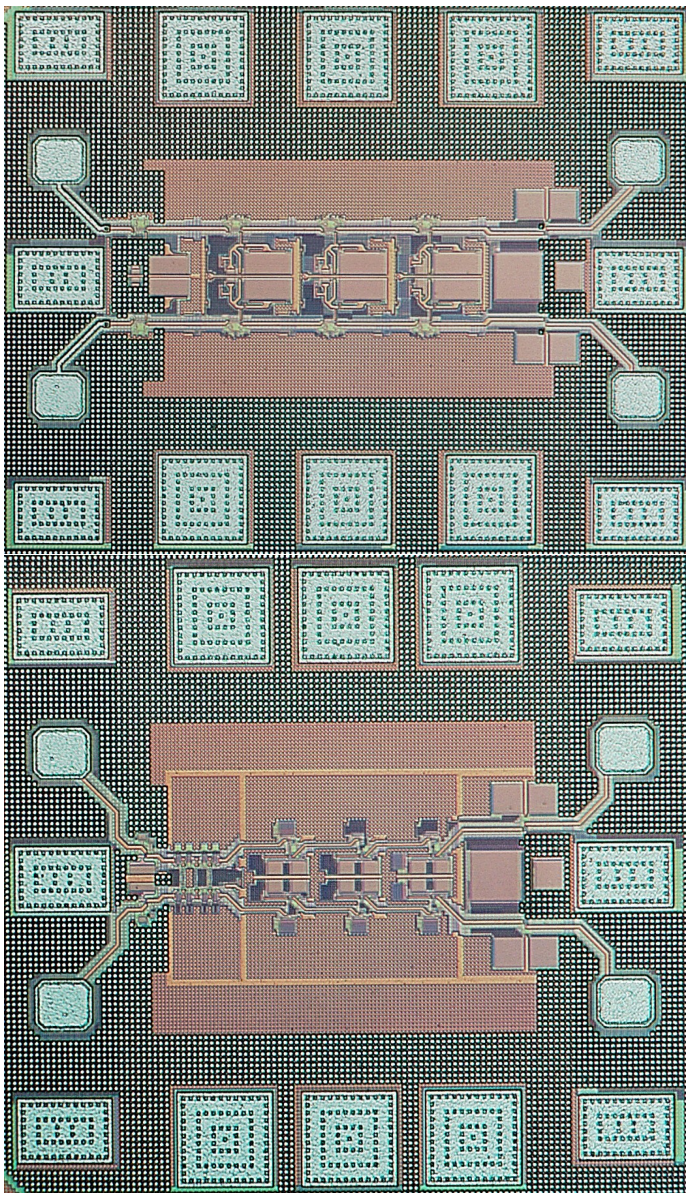

Figure 98: Variable Gain Amplifier dies.

shown in the previous Figures are principally based on architectures that exploit resistors as loads. These resistors are subject a quite large variability, due to the nature of the process and at the same time, the value of the bias resistors play a fundamental role along the amplifiers chain. The gain of each single stage (12 dB as anticipated in 4.1.1) amplifies the undesired offset on the quiescent point towards the amplifiers chain. The absence of AC couplings (no capacitors are used along the chain to avoid the high pass filter response at lowest frequencies) has allowed the propagation and amplification of the offset error and as a consequence

the output of the amplifiers is completely saturated for all difference levels of gain.

This occurrence has not been considerate during the VGAs design and the consequences on the final circuit have been disastrous. For this reason the measurement are not proposed in this thesis due to the scientific uselessness of the acquired data.

TRANSCEIVER INTEGRATION

5 TRANSMITTER INTEGRATION

Today the reliability of transceivers based on CMOS devices are widely demonstrated [93] and, now, the attention is focused on their performances improving. Gain, output power, bandwidth, and power efficiency are the performances at stake. In this work of thesis is tackled the energy efficiency characteristics together with the minimization of the total occupied area.

Author	Gain [dB]	CP [dBm]	Vdd [V]	Area [mm^2]	Psat [dBm]	Power [mW]	Tech. [nm]
[94]	n.d.	n.d.	1.2	n.d.	11	170	90
[95]	n.d.	-8.6**	1.5	0.2**	-7.2**	78**	90
[96]	8.9	n.d.	1	1	-0.7	131	65
[42]	8.6	1.5	1.2	2.1	5.7	76	90
[42]	12.4	4.1	1.2	1.95	8.6	112	90
[97]	7.4	-5	3	0.6	2	90	130
[98]	17	5.1	1	n.d.	8.4	156	90
[99]	18.3	9.5	1.2	n.d.	n.d.	186	65
[100]	17	5.1	1.8	2.62	8.4	113	90
[101]	19	5.2	1	1.5	6	133	90
[7]	5	-3.5**	1.2	0.6**	0.2**	53	65
[7]+[17]	19	10	1.2	1.2	12	118	65

Table 7: State of the art for 60 GHz Transmitters

5.1 60 GHZ TRANSMITTER

5.1.1 *Transmitter integration*

Concerning the transmission chain a comparative overview upon the state of the art is given in Table 7.

The circuits shown in Table 7 allow highlighting the high performances achieved by the present work. As anticipate in the previous chapters, the power efficiency of the transmitter is obtained through the optimization of each single sub-block.

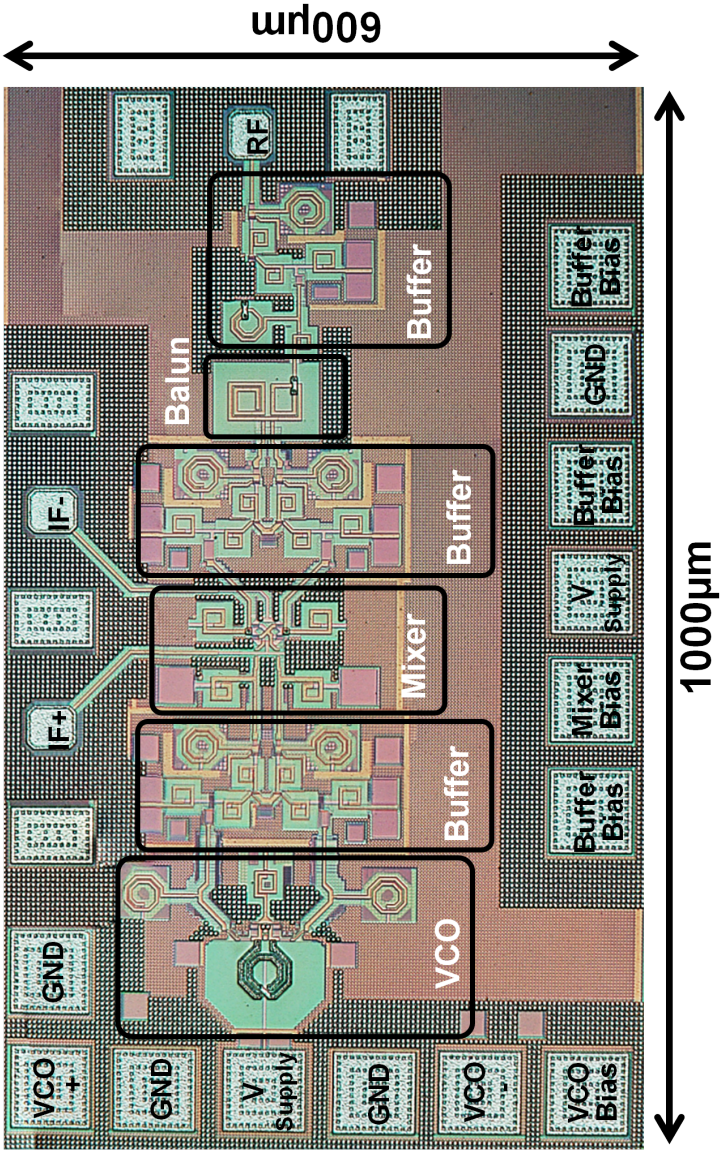

Figure 99: Transmitter die

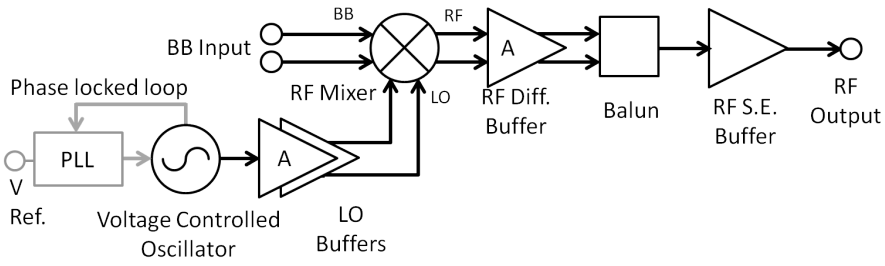

Figure 100: 60 GHz integrated transmitter: detailed scheme blocks

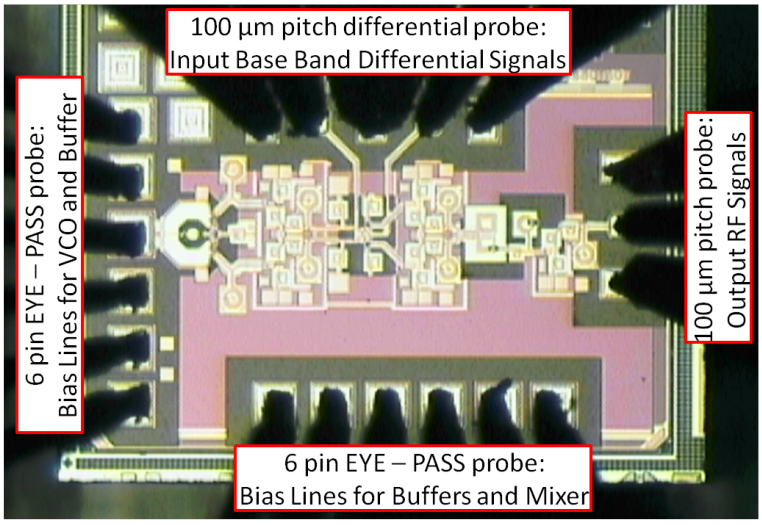

Figure 101: Measurement setup for the transmitter circuit

Voltage controlled oscillator (VCO), mixer, buffers and the passive elements (as the balun) have been chosen among the large selection existing in literature. Each class of circuits has been evaluated considering two sets of criteria. First, the standalone performances have been classified in order to find the best architectural solutions. Second, system compatibility among the blocks has been investigated. The principal feature, considered with particular care during the second steps step, is the estimation of the energy levels inside the transmitter. The power generated by the local oscillator and, the total RF power delivered to the antenna represent critical factors in the design of the transmitter. The magnitude of the LO signal determines the quality and the effectiveness of single stage upconverter mixer whereas the output RF power influences the maximum range of operability for the transceiver system. Following the considerations discussed during the mixer design, this latter component has been choose as reference block in the creation of emission chain. The required level of LO power is then fixed by the passive mixer discussed in section 3.1.2 and it correspond to 0 dBm. In these conditions the mixer is able to achieve around -9 dB of conversion loss with 0 dBm as BB input power. As a consequence, the RF output of the passive mixer will be around

-9dBm. In order to reach the required output values a couple of buffer chain is required. Figure 100 describes with more details the black blocks proposed in Figure 12 of 1.6.1. In this representation of the transmitter the handling of the differential nature of the system is highlighted as well as the importance of the balun presence.

The final transmitter chip, realized by ST Microelectronics, is shows at the end of this section in Figure 99. Its total dimension with pads is of 600 times 1000 µm.

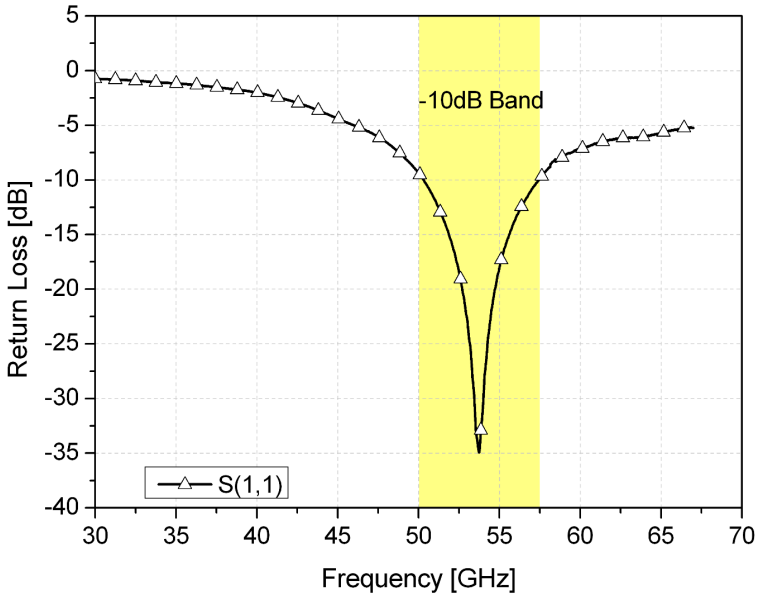

Figure 102: 60 GHz output reflection coefficient

5.1.2 *Measurements*

The realized transmitter has been measured on wafer up to 67 GHz. Probe station equipped by single ended and differential 100 µm pitch points are exploited to carry out the measurement campaign. Completely biased, (Figure 101 shows microphotography of the measurement setup), the transmitter absorbs 44 mA of DC currents with 1.2V of bias voltage involving 53 mW of total power dissipation.

5.1.3 *Transmitter output reflection coefficient*

The 50 Ω matching for the 60 GHz port has been measured by the N5247A PNA-X microwave network analyzer by Agilent. Measurement shows a 7.5 GHz of -10 dB of band around 53.5 GHz, Figure 102. The frequency scrolling of the best matching point toward lower frequencies is due to the capacitive effect of the RF pad. The retro-simulation confirms this hypothesis. The redesign of RF pad or an

improving of the output matching network of the driver buffer could solve this issue.

5.1.4 *RF Transmitter performaces*

The conversion gain and the frequency sweep measurements of the transmitter have been effectuated by using the Agilent E8257D as base band source and connecting the 67GHz spectrum analyzer by Rohde & Schwarz to the RF ports as shown in the inset of figure Figure 103. In order to obtain an input base-band differential signal a 180° hybrid coupler is used as balun. All losses originating from cables and probes are considerate and de-embedded in the results. Figure 103 shows the measurement results obtained from the transmitter for a sinusoidal base band signal spanning from 250 kHz up to 10 GHz. The central frequency of the VCO is 58.22 GHz. The measurement result shows very flat response for the upper side band of the transmitter (67 GHz represents the upper limit of the spectrum analyzer resolution). The response in the lower side band, instead, shows a raise of losses. This behavior probably is due to two independent factors, the first is the reduced gain of the RF buffer and driver amplifier and, the second issue arise from the phase shift produced by the balun during the differential to single ended signal recombination.

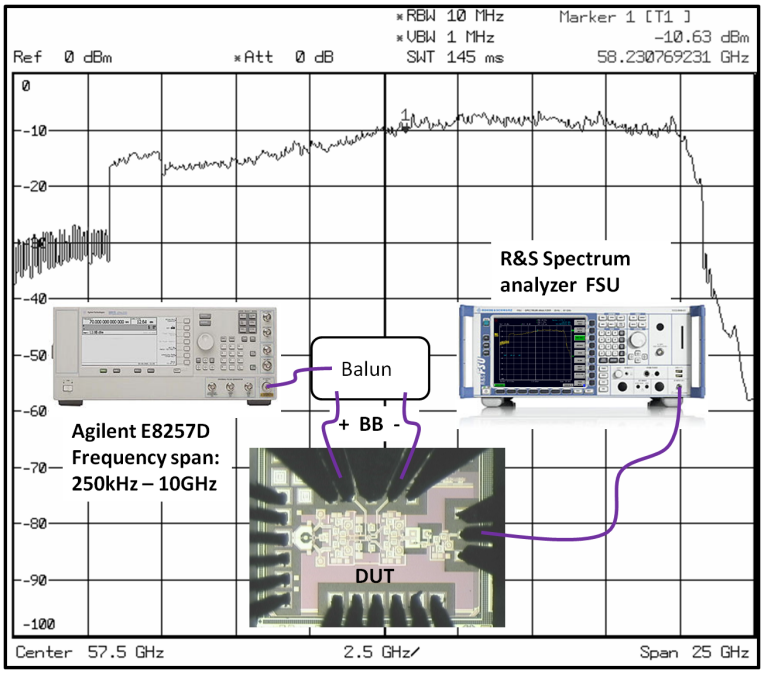

Figure 103: Transmitter Conversion Gain

5.1.5 *Transmitter power measurement*

The power measurement shows -3.5 dBm OCP that constitutes an extremely good result for a transmitter without PA. The power compression point is obtained adding 3 dB at the peak value measured at 59.7 GHz, to take into account the power of the two side bands. The saturated power is reached at 0.2 dBm with 0dB of BB input power. Figure 104 shows the curve of output compression point of the transmitter.

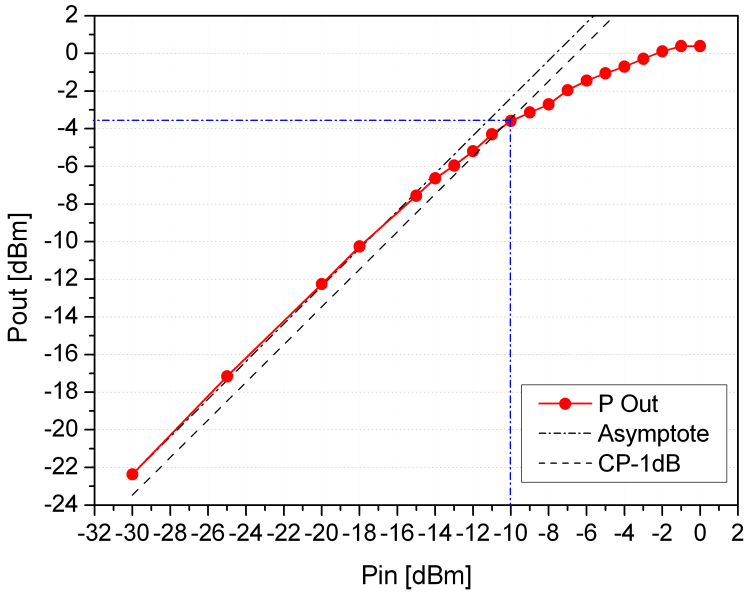

Figure 104: Transmitter Output compression point

5.1.6 *OFDM modulation in 60 GHz band*

Figure 105 shows the spectral response of UWB-OFDM signal around the 58 GHz carrier. The BB signal is composed by 128 different carriers with 120 MHz of band. The response is obtained replacing the Agilent synthesizer with a Virtex™-5 FPGA embedded in the Red Rapids® card. The figure represents not de-embedded values.

5.1.7 *Conclusion*

The design of a low power transmitter based on passive mixer architecture is presented. The highest value od $CP_{\_1dB}$ of the mixer combined with its zero power dissipation yields an extremely efficient transmitter. The experimental characterization shows a very wide operative bandwidth for the transmitter with really high performances in terms of linearity and gain. The output referred

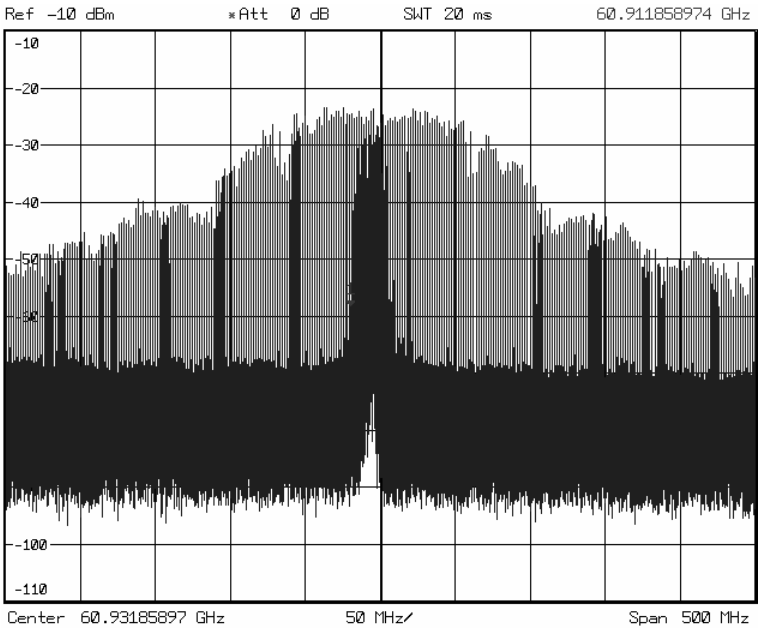

Figure 105: Spectrum of OFDM modulation into 60 GHz band

compression point of the transmitter reaches the -3.5 dBm without PA stages. The saturated power is 0.2 dBm with odBm input power. UWB-OFDM modulation is employed to demonstrate the quality of the channel. The total transmitter power dissipation results in 53 mW with 1.2 V of bias voltage. Thanks to this high performance combined with very low power consumption, the proposed architecture finds an ideal application field in the battery driven wireless sensor network. Some studies to increase the transmission range for the transmitter are already started, and the uses of smart antennas with active arrays are in phase of evaluation. The employment of a very compact and reduced losses device together with the proposed low power mid amplifier could increase rapidly the range of functioning of the whole proposed transmitter maintaining a reduced dissipation power for the entire system as well.

5.2 60 GHz I/Q receiver

The design of I/Q receiver require higher efforts due to the increased complexity of the in-phase / quadrature demodulation architecture. As anticipated in 1.6.2 the proposed receiver is the evolution of the circuit realized in [27]. The studies performed during this thesis work aim to improve its performances increasing the demodulation capabilities. Among the component added in the I/Q version of the receiver, the Lange coupler described in 2.4 and the variable gain amplifiers are the most important ones. The Lange coupler splits the received signal, coming from the low noise amplifier in two identical portions with a reciprocal phase shift of 90°. The variable gain amplifiers instead are exploited to increase the

dynamic range of the receiver. Another important redesign in the receiver has been accomplished in the LO generation line. In order to understand the increased complexity a more detailed block scheme of the downconversion chain is proposed in Figure 106.

The design of receiver is then divided into two consecutive steps. In the first run the LO driver system is developed (the circuit in the dashed red square on Figure 106) whereas the final run contains the entire integrated receiver.

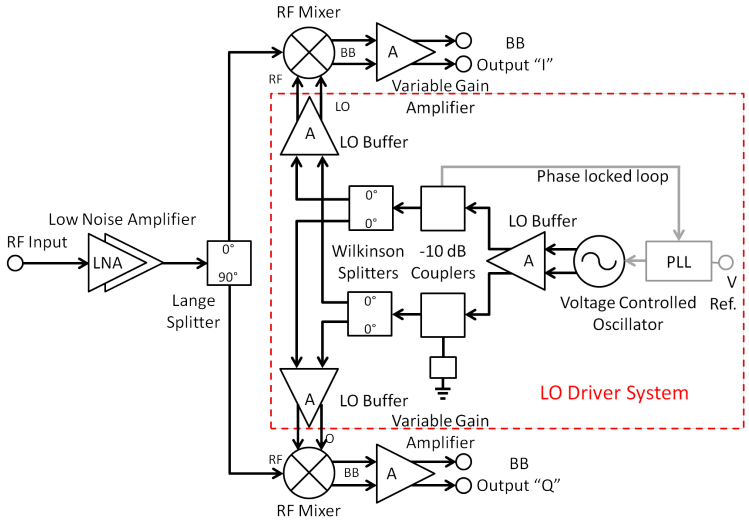

Figure 106: Detaile block scheme of 60 GHZ receiver

5.2.1 *LO driver system*

In the homodyne architectures only one carrier signal is necessary to yield the frequency conversion. A 60 GHz oscillator provides to the required carrier. As discussed in the previous chapters, the control of the power level on the local oscillator signal is crucial for a good response of the up/down converter mixers, then, it is extremely important to characterize each single part of the LO signal path.

Concerning the realization of the I/Q receiver, the differential VCO proposed by [78], have to be enhanced (the redesign of the VCO proposed in section 80 were not still completed). Following the description of Figure 106 the differential LO is in a first instance acquired by a coupled branch in order to drive the frequency divider of the phase locked loop circuit (PLL, not implemented in this thesis). The transmitter part of the signal, at the output of the coupler, is then split by two Wilkinson power splitters 2.5.1. The insertion losses added by the power splitter and by the -10dB coupler together with the half power division require the use of differential buffers in order to recover the power levels necessary to drive the downconverter mixer. The buffers employed here are designed with the design

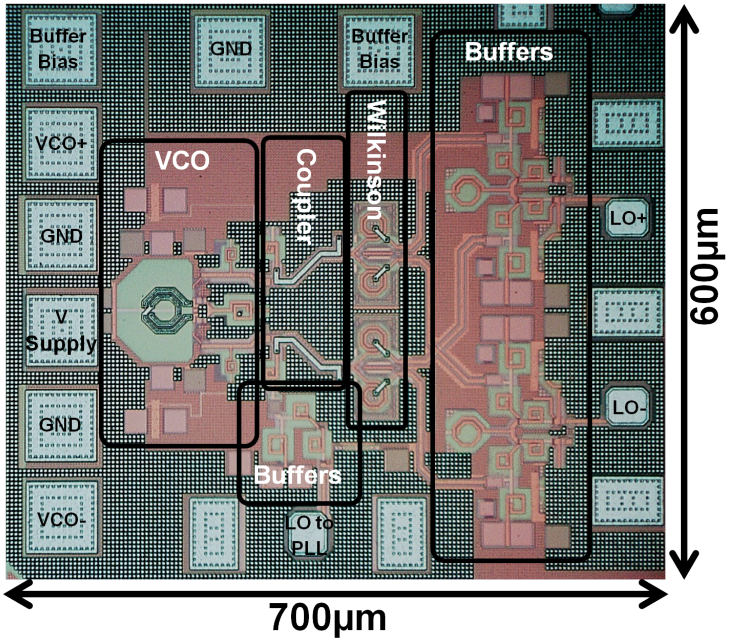

Figure 107: LO driver system chip

flow procedure discussed in 3.3. It's important to underline that, at 60 GHz, the realization of such complex structure implies a series of issues to solve. The losses and parasitic couplings minimization, the control of the LO phase shift towards the four branches constitute the set of constraints to satisfy in order to avoid undesired response of the system.

The realized sub-system is shown in Figure 107 it occupies 0.7×0.6 mm² including RF and DC pads. For this version of power driver no current mirror are employed to control bias currents into the buffer.

The total power dissipation for the entire structure is 49 mA at 1.2 V. This value includes the 16 mA of the VCO and the current needed for the 5 buffers (two differentials and one single ended) . The power dissipation is relatively small compared to the values of the LO power output delivered from the respective 5 outputs. The power values together with the other feature of the system will be shown in the next section.

LO drive measurements

The system has been measured using an Agilent N5247A PNA-X with 4 port VNA to estimate the return loss at the ports. A 20 kHz - 67 GHz Rhode & Schwartz spectrum analyzer is employed to estimate the minimum and maximum frequency swing of the system. Finally a power meter Agilent N1913PM is used to estimate the total power delivered from each port. The system in the work conditions

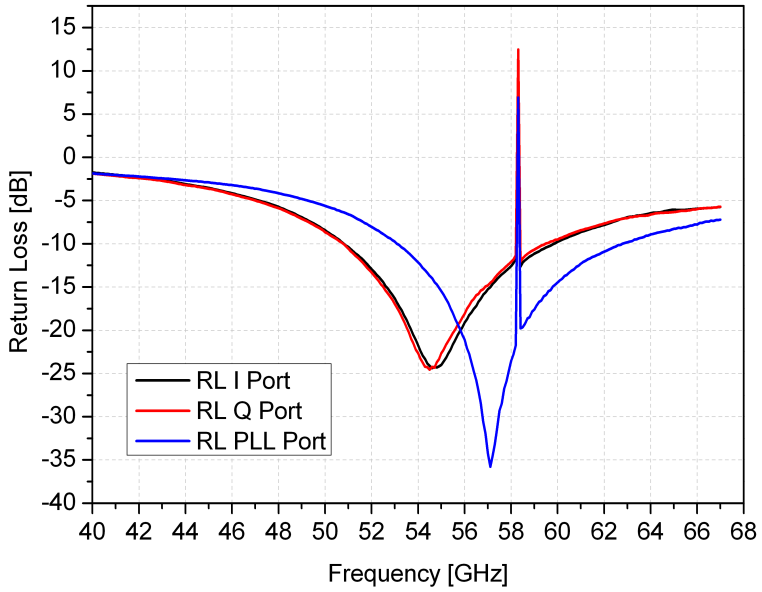

Figure 108: Return loss of LO driver system

shows two pairs differential output channels to drive two differential mixers and one single ended output to drive the PLL frequency divider. To minimize the silicon surface for the prototype and to simplify the measurement campaign, two outputs have been closed on 50 Ω loads directly within the circuit. The two loads are accurately simulated and the parasitic are extracted to guarantee as much as possible the real desired value of load. The others two outputs, instead, have been connected to the pads to be measured. However, in these conditions the effective load on the measured ports is different from the load on the on-chip matched ports. The parasitic capacitances added from the pad are estimated. Therefore, to obtain the same behaviors a 24 fF shunt capacitor is placed at the output of the on-chip ports.

Return loss

The output port impedance measurements confirm the quality of the design. The output matching network of these buffers has been centered at 55 GHz and the measurements shown in Figure 108 confirm the simulations results. The -10 dB band for the IQ output is 50.7-60 GHz instead, for the PLL output is 53-63 GHz. Port I and Q show an identical behavior due to the high symmetry of the circuits. For the PLL output the difference on the output matching is due to the small variation on the topology of buffer. The peak at 58.37 GHz is the VCO carrier that runs during the measurements.

VCO Frequency Tuning

The VCO [78] shows a frequency tuning range (FTR) from 57.58 to 60.80GHz. Being the VCO common source buffer not perfectly isolated, a charging effect influences the VCO central frequency. As a consequence, the central frequency shifts at lower frequencies. In particular for the measured system for a voltage sweep from -4.84 to +2 V the FTR is from 56.5 to 60 GHz. The FTR remains the same as the [78] but the capacitive effect on the coupler component and other blocks determines a sensible change on the buffer impedance that causes a shift on the L-C central frequency resonation.

Output Power

In [78] the output power delivered from the VCO depends on the frequency. It rises from -5 dBm at 57.58 GHz to -0.9 dBm at 60.52 GHz. This dependence between LO power and frequency influences the mixer behavior's in particular if the mixer is passive. This is partly compensated in the design phase through a buffer with an opposite behavior. The remaining part of the compensation is achieved exploiting the buffer compression point. The saturation of the buffer does not represent a problem because the mixer does not require high linearity signal at LO input port. The buffer is designed to have an output compression point of +1 dBm. For the high value of input power at 60 GHz a saturation effect is detectable. For lower frequencies instead, this phenomenon is not present. As a consequence, the variation of the total power, shown in Figure 109, is reduced to 1.25 dB, as opposed to the initial 4.1 dB of difference in [78]. The increased flatness of the response improves the control on the mixer. The high power level delivered allows driving easily different type of mixers [102, 2, 103]. The small difference between I and Q outputs could be attributed to measurement errors. The difference is limited at only 0.2 dB so the performances of the entire I/Q receiver are not penalized. In Figure 109 the right axis shows power delivered from the buffer at PLL block. The measurements show a lower than expected value of power. This is probably due to a lower coupling value furnished by the coupled-line coupler. However this drop of power is not considered as a problem, because the minimum power level is still in the range of power accepted for the frequency divider. The power difference in this case is more accentuated. In effect, in this case the low power at the input of buffer does not causes the saturation as on the I/Q output, so the linearity of the characteristic on the buffer does not help to maintain flat the power level at the PLL out. However, as for the absolute power level, the power raise does not affect the good performance of the frequency divider.

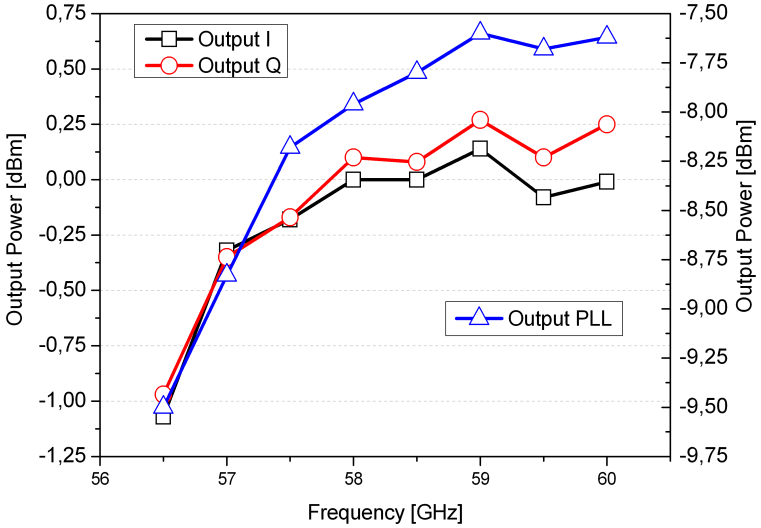

Figure 109: Output power for LO driver systems

5.2.2 *Receiver complete*

The integration of the remaining part of receiver has been done using the low noise amplifier and the single balanced mixer developed by M. Kraemer during his PhD thesis [18]. A brief introduction about these components is proposed in the next two paragraphs.

Low noise amplifier

The LNA [18, 104] employs two single-ended Cascode stages. The Cascode topology allows good stability and excellent reverse isolation, which is especially important in direct conversion architectures. The first stage is optimized for very low noise. Therefore, the transistors are biased around minimum NF current density at 0.15 mA/µm [105]. The widths of the transistors are chosen to be 22×1 µm in order to yield a real part of the optimum noise impedance that equals 50Ω to facilitate matching. All transistors used in the design have a minimum drawn gate length of 60 nm. The transistors in the second Cascode stage have a width of 26×1 µm and thus are slightly larger than the first one to improve the linearity of the output LNA stage. To increase the linearity of the stages without risking damage for the transistors, a remedy is used during LNA design. In effect, one consequence of the use of GP transistors is the lower breakdown voltage (1 V). The solution proposed for this LNA design is to embed the Cascode transistors into a deep n-well. The transistors are then isolated from the grounded substrate and the drain and the gate voltages in excess of 1V become feasible. The fabricated LNA (in a standalone chip) occupies 0.4×0.4 mm die area. It can be biased using two different supply voltages: When using 1.5V, a peak gain of 22.4 dB and an output referred 1 dB compression point of -3.4 dBm is measured while drawing

11.2 mA supply current. The noise figure is 5.1 dB. When using a supply voltage of 1.0 V, a peak gain of 18.7 dB and an output-referred 1 dB compression point of -6.5 dBm is measured while drawing 8.5 mA supply current. The noise figure is 5.4 dB. Figure 110 shows the fundamental features of LNA and Figure 111 the stand alone chip.

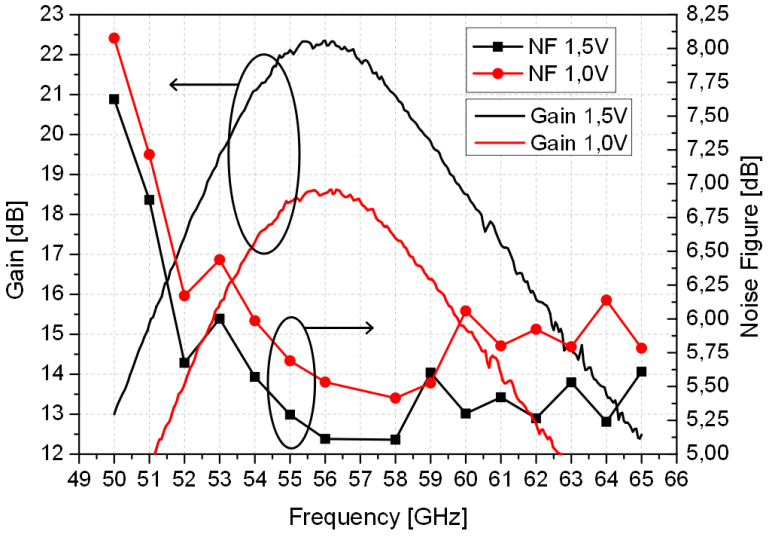

Figure 110: LNA gain and noise figure performances for 1V and 1.5 V of bias

Half balanced mixer

Single balanced mixer The circuital scheme of the designed mixer is shown in Figure 112.

The RF input port is single-ended, because the preceding is the single-ended low noise amplifier described before [104] (in the first version of 60 GHz receiver, in the I/Q version is the single ended output of Lange coupler). The differential base band frequency of the mixer is connected to a buffer amplifier based on a differential pair. The BB buffer has been designed to drive a differential load (100 Ω) and, its power consumption is around 14 mW. In the I/Q receiver redesign the BB buffer it has been replaced by a differential variable gain amplifier (VGA). Concerning the mixer core design, a current bleeding technique [61] is employed to permit ideal biasing of both transconductance and switching transistors. The current which by-passes the switching pair is determined by the resistor R_B. It passes by the inductance L_B, which at the same time resonates the parasitic capacitances present at the drain of M_1 [63]. The transistor M_1 is biased at the minimum noise current density of 0.15 mA/µm. Its width is 14×1 µm. M_1 is degenerated by the inductor L_D. This improves linearity and allows a simultaneous noise and power match. Inductors L_2, L_3 and L_4 realize this match over a wide bandwidth. Transistors M_2 and M_3, which are 35×1 µm wide, are biased at very low current densities to allow fast switching. The resistive loads R_1

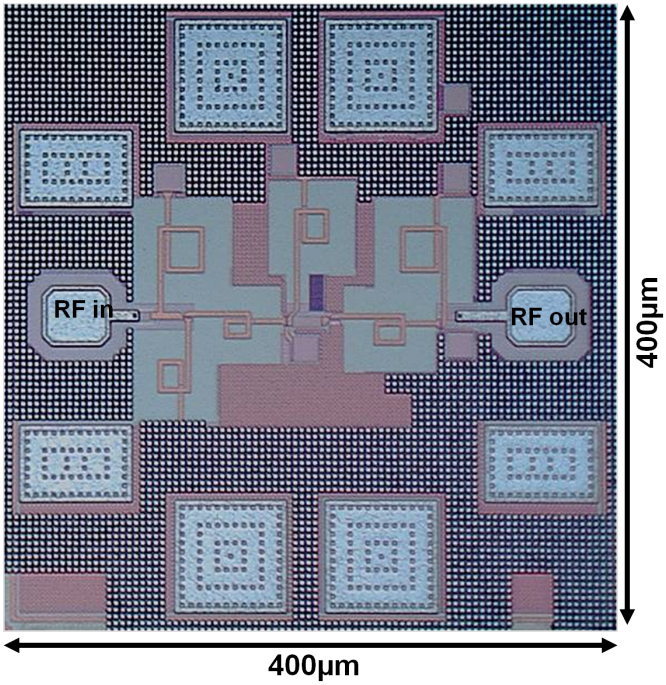

Figure 111: LNA standalone chip

are short-circuited by C_1 for RF and LO frequencies to increase conversion gain GC and improve isolation. A very small, pad limited die size of only 0.49×0.52 mm²is obtained, which is further reduced when integrating the mixer into the receiver. The mixer circuit of is measured on-wafer up to 65 GHz. The return loss is determined using an Anritsu ME7808A vector network analyzer (VNA). The LO signal is generated by an Agilent E8257D source that provides up to 14 dBm output power at 60 GHz. Power conversion gain and power sweep measurements are done using the VNA as RF signal source and connecting a Rohde&Schwarz FSU 67 GHz spectrum analyzer to one of the IF ports, while terminating the other one. All loss originating from cables and probes are subtracted from the obtained results, and 3 dB are added to the IF output power to account for the differential signal. While measuring, the mixer is biased at the current densities fixed during design. The bias of the switching pair depends on the LO power and is set to 0.7V for the LO power sweep. For the other measurements, the power of LO is equals -1 dBm and the switching pair is biased at 0.56V. The circuit including buffers is drawing 16.8 mA from a 1 V supply, from which only 2.8 mA are attributed to the mixer core. An excellent broadband match is assured, contributing to a very flat, wideband response of the mixer. The measured IF return loss stays below -15 dB up to 5 GHz and at RF, instead, the return loss remains close to -20 dB starting from 55 GHz up to 65 GHz. Figure 113 plots the conversion gain in the lower (LSB) and upper sideband (USB). A very flat, wideband response can be observed for BB frequencies of 1 GHz and 2 GHz, while both sidebands are very

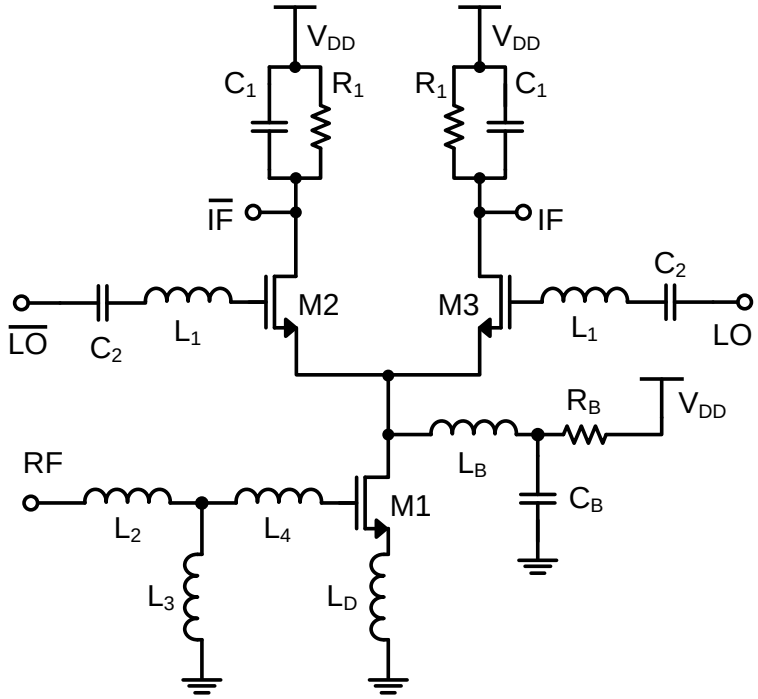

Figure 112: Circuital scheme of half balanced down convertsion mixer designed by M. Kraemer

symmetric. The conversion gain is around 6 dB at 1 GHz from the carrier over the whole band. The measurement frequency range was bounded to below 65GHZ due to the used equipment. An output referred 1 dB compression point of -5 dBm is obtained for LO power of −1 dBm.

5.2.3 *Receiver Integration*

The system integration started around the already characterized LO power driver system. The principal efforts, on this last phase of the design were focused on the placement of the remaining parts of circuits (LNA, hybrid 90° coupler Mixer and VGA). In this phase of design the layout of the half balanced downconverter mixer has been completely redesigned. The 50 Ω output buffer was removed to left space at the VGA and the placement of the input and output lines together with the inductors positioning have been retouched to improve integrability of the mixer. At the end of this layout reconfiguration the shape of the mixer was quite different from the original one. Concerning the LNA, only small changes on the output network were done in order to improve the matching with the Lange coupler. Finally for the Lange coupler the isolated port (port 4) has been closed on a 50 Ω resistor. To connect together all the different blocks, high-Q grounded coplanar wave guides are exploited to reduce the losses. The final

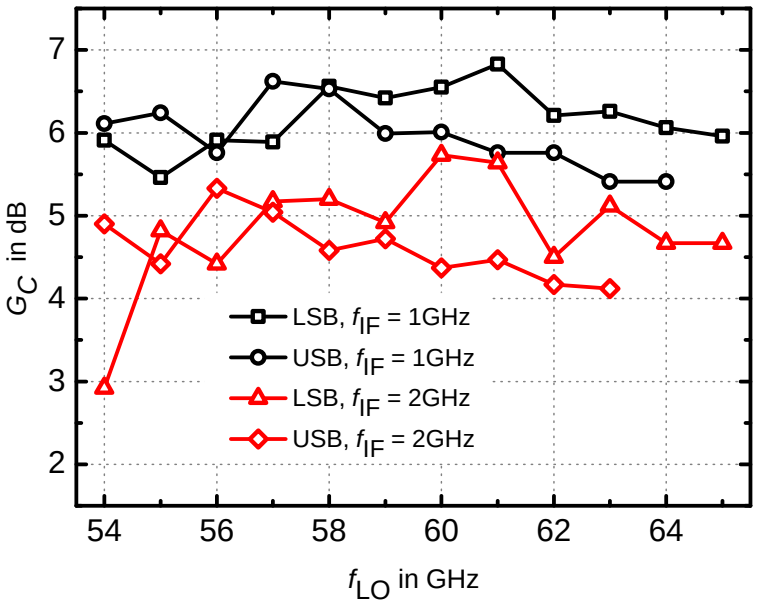

Figure 113: Conversion Gain of down converter mixer

chip for the 60 GHz receiver is shown in Figure 114. The circuit occupies a total surface of 1×1.2 mm^2. As the figure shows, due to the complexity of the system a very high number of DC pads are needed. A wide number of these pads are dedicated to the DC voltage supply. In fact, due to the large area occupied by the circuit it is important to guarantee a constant level of VDD all around the die. For this reason, VDD and Ground pads are multiplied all around the die (were possible). In addition, inside the Faraday cage thick copper connection on metal 7 are used to improve the VDD bias in the high dense circuit areas (as for instance, around the buffer of LO driver systems). The other DC pads instead (in particular along the top and bottom side of the die) are dedicated to the voltage bias of the different blocks (VGAs, mixers, buffers) the bias pads of mixers and VGAs are replicated two times in order to assure the correct bias of the circuits. The DC pads in the left are dedicated to the biasing of the VCO with exception of the first and last one (dedicated to the VDD). On the right, instead, only VDD and GND pad are inserted to maximize the current flows in the mixers and in the LNA. The total number of pad in the presented die is 20 for the DC contacts and 16 for the RF one. However, to allow the operation of the circuit only 16 DC pads and 12 RF pads have to be really connect.

5.2.4 *Measurements*

Measurement setup

The characterization of the I/Q receiver with this large number of pads require a test structure based on PCB substrate. The test fixture was designed to facilitate

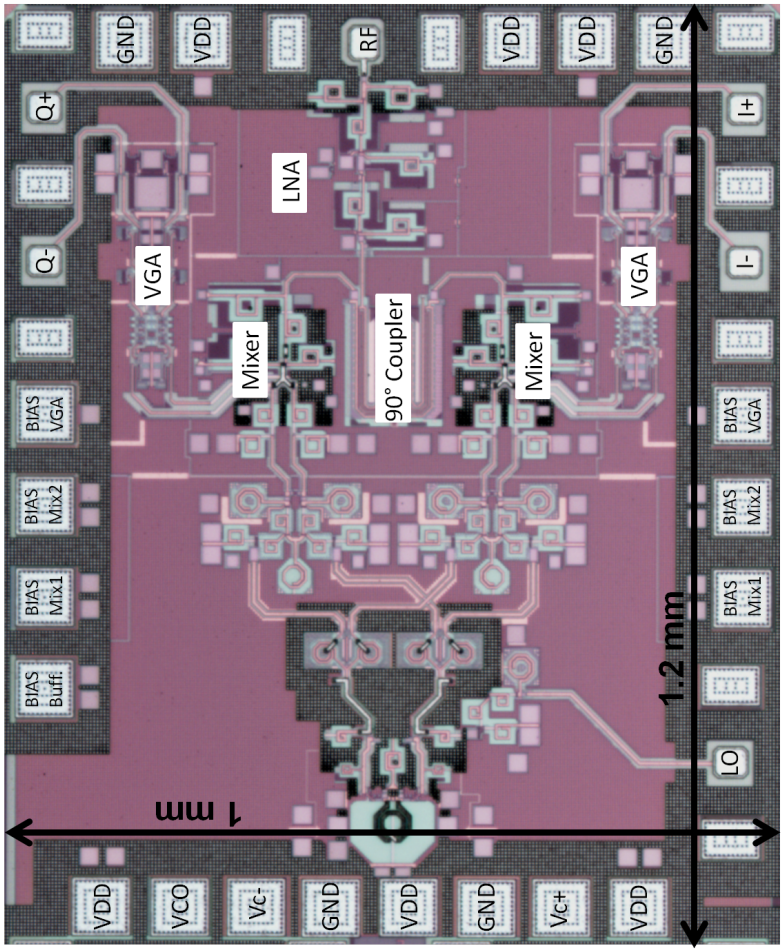

Figure 114: Receiver Complete

the measurement campaign and to improve the performance of the measurements. The main difference, in fact, between probe station measurement and the characterization upon a test fixture support concerns the strengthening of the external interference rejection. With a series of filtering networks (R-C circuits) placed in concomitance of the voltage bias pads the undesired harmonic signal will be shorted to ground. In the case of probe station measurements, the voltage biases are imposed by the use of DC probes. The probes don't are equipped by a filtering network and all of parasitic signal captured by the floating cables are sent in the DC pads of the receiver. This phenomenon causes undesired (and unconsidered as well) behaviors of the circuit and an overall degradation of system performances. The test fixture developed for the 60 GHz receiver is shown in Figure 115. In the detailed portion of the figure a microphotography shows the wire-bonding connection between the PCB and the die. In the microphotography it is possible to remark that only the 60 GHz pads are left without bond-wire. This is due to the

too high operative frequency. In the final design, the interconnection between the 60 GHz pad and the antenna will be obtained with flip-chip technique. During the measurement campaign the 60 GHz signal, will be injected in the input port of LNA with RF probes. The PLL output, instead, will be exploited (with an RF probe as well) to control the values of the VCO signal: the central frequency and, most important, the good work of VCO itself. BB output of the receiver allows a downconversion starting from DC up to 2.7 GHz. The output differential impedance of the VGA is 400 Ω according to the input impedance of ADCs. To match this impedance with the 50 Ω of measurement equipment a 1:3 balun is exploited. It is clear that the not perfect impedance transformation between VGA output and measurement instrumentations cause partial reflection of the signals but this non ideality has been evaluated during the design process.

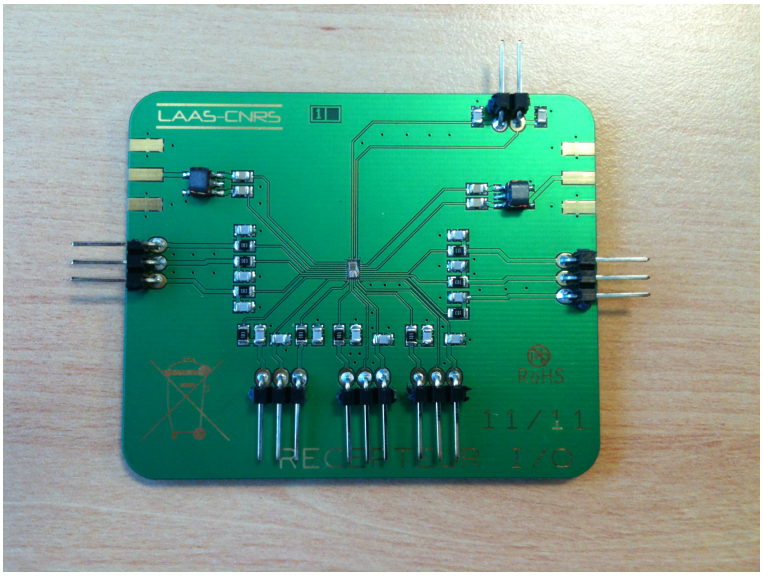

Figure 115: Test fixture PCB

Measurement results

The advantages offers by the test fixture setup are paid with delays on the measurement scheduling. The realization of the PCBs and the most critical wire-bonding connections has to be programmed with considerable advance. This criticism involves also the risk of chip breaking during the measurement campaign. To minimize this probability a first on-wafer measurement campaign has been executed. As previously discussed, the I/Q receiver can work with a reduced number of bias contacts and this number can be still reduced if only half demodulation chain works. The on-wafer measurement have been started with the use of one 8 pin EYE-PASS DC probes, one differential 100 µm pitch probe (for the BB output) one single ended µm µm pitch probe (for the 60 GHz input) and 6 single point

DC probes to Bias the remaining necessary plots on the circuit. Figure 116 shows the probe station with all of probes placed.

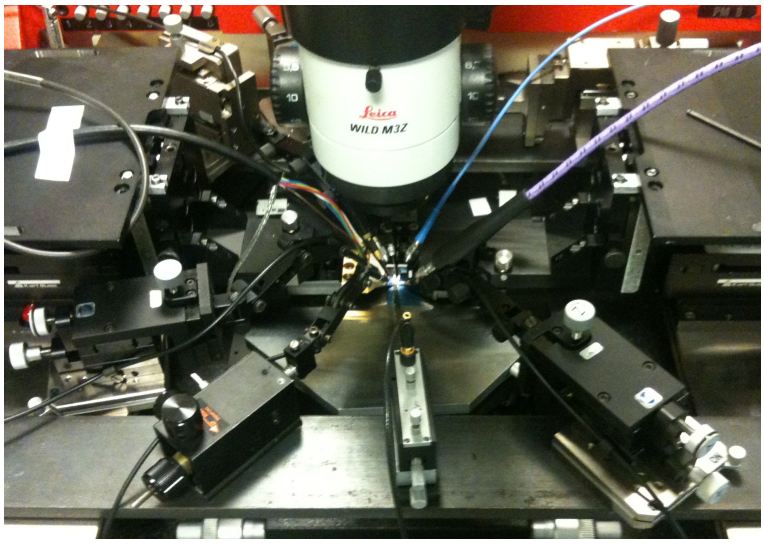

Figure 116: On-wafer measurement for the 60 GHz receiver: probe station setup.

The Receiver, using a supply voltage of 1.2 V, draws 63.5 mA of current therefore the power consumption is 76.2 mW. This power consumption is aligned to the prevision and in concordance with the very low power consumption shown by the first version of receiver was proposed by M. Kraemer [27, 18]. The main difference on the power consumption comes from the LO driver system with the pair of differential buffers and from the VGA blocks. The measurement campaign starts with the evaluation of the LNA performances. The input impedance has been measured with the Agilent N5247A PNA-X up to 67 GHz, the results are represented in Figure 117.

Before starting the downconversion measurement, the integrated VCO has been tested in order to verify the allowable frequency tuning ratio and the oscillator center frequency. R&S spectrum analyzer is therefore connected by a single ended probe on the pad dedicated to the PLL. The resulting oscillation frequency with the oscillator varactor connected to ground is 58.1 GHz, as Figure 118 shows.

The power level represented in Figure 118 are not de-embedded from cables and probe losses. The minimum and maximum allowable frequencies are respectively 56.28 and 59.89 GHz, as a consequence, the FTR for this receiver is 6.21%. . The Agilent E8257D signal generator has been chosen as RF source, in the base band output, instead, the differential signals are respectively sent to the power meter (Agilent N1913PM) and to the R&S spectrum analyzer.

The downconversion and noise figure measurement, however, have not been accomplished because, as shows in Figure 106 the base band output of the receiver is controlled with VGAs. Unfortunately, due to the superposition between the receiver design and the characterization of the standalone VGAs, the design

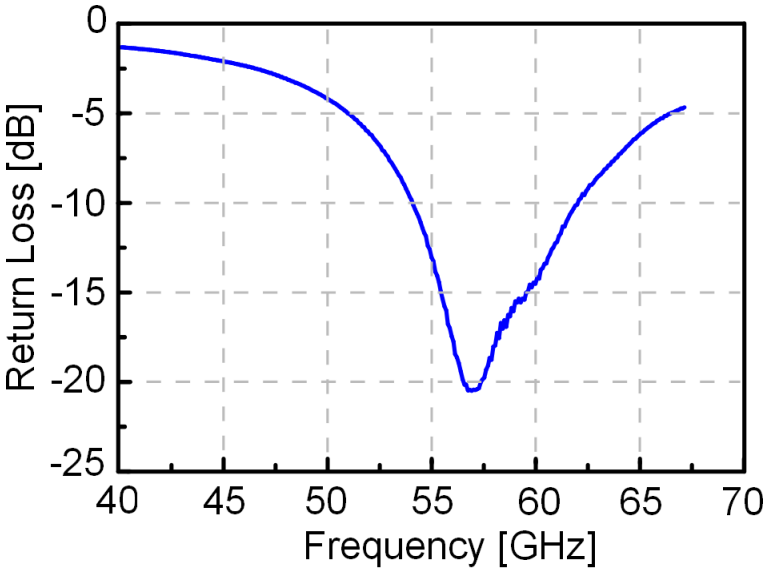

Figure 117: LNA input return loss

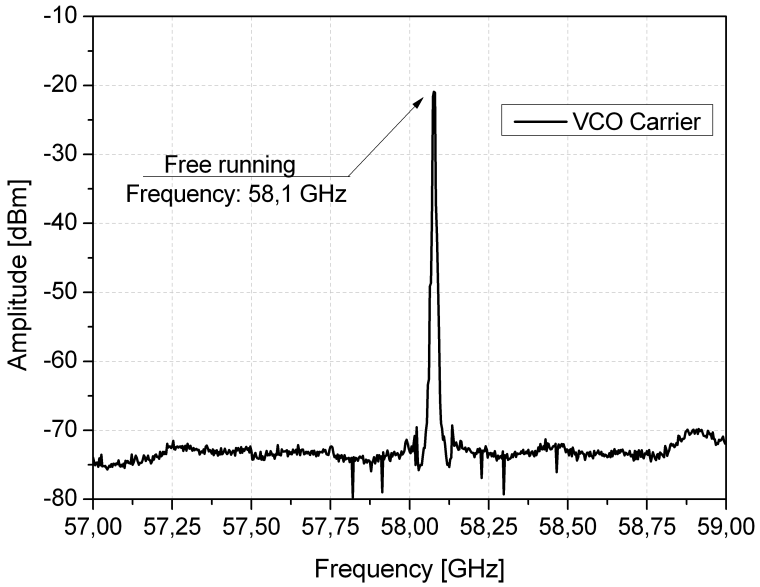

Figure 118: Free running oscillator frequency for the integrated receiver VCO

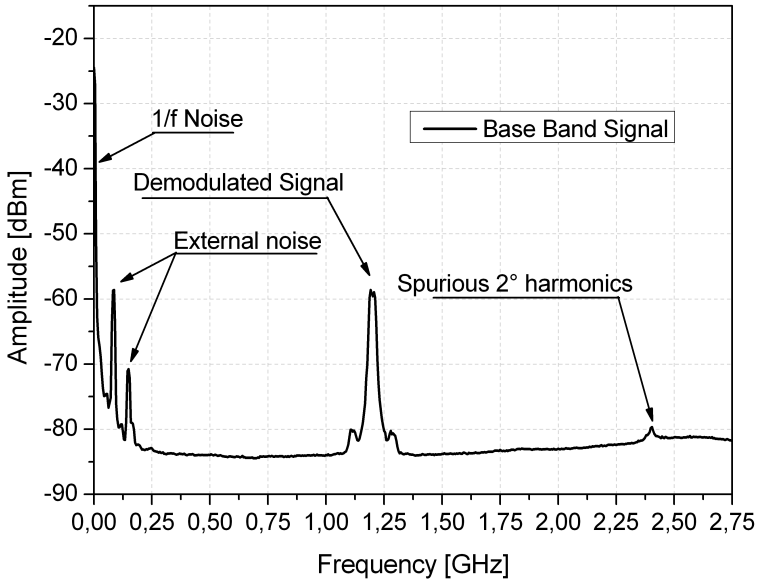

Figure 119: Dovnconverted signal

issue observed in the amplifiers chains has been discovered after the sending to production of the I/Q receiver. As expected during the measurement campaign, the design errors on the architecture of VGA have completely destroyed the very good performance expected form the circuit. The downconversion chain however has been tested. In fact, despite the malfunctioning of the VGAs block a very small leakage signal flows towards the chain and the RSU spectrum analyzer reach to recognize it. Figure 119 shows the downconverter signal. As anticipated in [paragrafo test_fixture], without the test-fixture setup several parasitic signals are captured by the bias setup. The spike highlighted in Figure 119 are composed by very pure tone at 86.5 MHz and 150 MHz. They probably come from other instruments in the neighborhood of the probe station.

The state of the art for the 60 GHz receivers are summarized in Table 8 [18]. Concerning the proposed I/Q receiver the simulated RF performance will be considered.

Reference	Tech. [nm]	RF [GHz]	IF [GHz]	NF [dB]	C_G	IP_{-1dB}	P_{DC}
[63]	130	57-64	0	12.5	28	-22.5	9
[106]	90	51-56	3-5	6	21.5	-21	60
[107]	130	57-63	2	10.4	11.8	-15.8	76.8
[108]	90	59-61	0	9.5	23	/	54
[109]	65	58-63	0	5.6	14.7	-22	151
[110]	90	58-62	0.2.2	6.1	18	-26	24
[111]	130	60-65	20	10	30	-27	44
[101]	90	60-64	0	8.3	/	/	206
[112]	90	61-63	0.1	8.4	22.5	/	144
[113]	90	61-63	1	5.6	25	-16	132
[114]	45	56-67	0-1	6	26	-21.5	21
[115]	65	51	0.5-2	9.2	14.5	-24.4	174
[116]	90	60	10	7	25	-26	103
[117]	65	62-67	20	9	28	-26	80
[55]	130	50-60	0.1	9	18	-20.8	50.2
[118]	65	55-68	20	5.6	35.5	-39	75
[27]	65	56-61	0-1.5	9.2	30	-36	43
This work	**65**	**56-61**	**0-2.5**	**/**	**26-60**	**-32**	**73**

Table 8: State of the art of 60 GHz receivers.

SYSTEM INTEGRATION

6

SYSTEM INTEGRATION

6.1 LINK BUDGET COMPLETE ESTIMATION

A first raw example of link budget for 60 GHz link is proposed in section **??**. However in order to understand how are the realistic possibilities for the proposed transceiver chain, a more accurate estimation is proposed o the next pages. Three different configurations for the system are considered and depending of these architectures the allowable distance between the communicating point changes enormously. The intention is to give an overview of the possible issues, without focusing on a specific environment or implementation. Specific link budgets can be found for example in [119] or [120]. As exposed in section **??** a reliable link require at least a margin of 10 dB into signal to noise ratio (SNR). Considering only the main contributes, the SNR formula can be written as follow:

$$SNR = P_t + G_t - PL(d) + G_r - PN - IL - FM \tag{6.1}$$

In which: P_t is the transmitted power, G_t and G_r are the antenna gains, $PL(d)$ is the path loss at a distance d, PN the noise power, IL the implementation loss and FM the fading margin. The expression is considered in dB.

The proposed value for the variable in equation 6.1 are given in Table 9 for three 60GHz examples and will be explained in the following pages.

The considered bandwidth is 1.88 GHz bandwidth, as shown in figure 8, when simple single carrier or impulse modulations are employed.

The noise term PN in equation 6.1 is given by

$$PN - 10\log(kBT) + NF \tag{6.2}$$

The first part corresponds to the thermal noise power over the channel bandwidth $B = 1.88$ GHz. Due to this ultra wide bandwidth, a quite large value of -81.09 dBm at room temperature T = 300K is obtained. The second part of 6.2 is the receiver noise figure NF, which is added to the thermal noise level due to noise added by the receiver front-end. The receiver designed in [27] shows a noise figure of around 7 dB. The term IL originated from the non-idealities of the transceiver degrades the signal, like nonlinearity in the front-end and phase noise of the local oscillator. An implementation loss of $IL = 6$ dB is assumed. Finally FM represents the fading margin. The fading decreases with channel bandwidth, as a consequence FM remains as low as 3 dB for a channel bandwidth of 1.880 GHz. The path loss PL as a function of distance d is given by

$$PL(d) = PL_{d0} + 10n\log\left(\frac{d}{d_0}\right) + \chi_\sigma \tag{6.3}$$

Parameters		Case 1	Case 2	Case 3
Bandwidth	B	1.88 GHz	1.88 GHz	1.88GHz
Transmit power	Pt	8 dBm	8 dBm	- 4
Receiver antenna Gain	Gr	15 dBi	3 dBi	3 dBi
Transmit Antenna Gain	Gt	15 dBi	3 dBi	3 dBi
Noise Power	PN	-74 dBm	-74 dBm	-74 dBm
SNR	SNR	10	10	10
Implementation Loss	IL	6 dB	6 dB	6 dB
Fading	FM	3 dB	3 dB	3 dB
Path loss at 1m d_0		68 dB	68 dB	68 dB
Resulting Path Loss d_{max}	PL	88 dB	88 dB	88 dB
Temperature	T	300 K	300 K	300 K
Power Consumption	W	$\lessapprox$0.220	$\lessapprox$0.220	0.130
LOS (n=2)		10 m	1 m	0.30 m
NLOS (n=4)		3.16 m		//

Table 9: Link budget parameters

where n is the path loss exponent and χ_σ is the shadowing parameter. The reference path loss at a close reference distance do corresponds to the free space path loss given by

$$PL_{d0} = 20n \log\left(\frac{\lambda}{4\pi d_0}\right) \tag{6.4}$$

The path loss exponent n, which equals 2 in the case of ideal free space propagation, depends on the environment due to constructive and destructive multipaths and additional attenuation. The channel modeling furnished with the IEEE 802.15.3c standard [119] shows that for LOS indoor channels, the path loss component n varies from 1.2 to 2.0. For NLOS environments, n sweeps between 1.97 and 10. For the following considerations, one LOS indoor/outdoor channel with n = 2 and one indoor NLOS channel with n = 4 are taken as example. Similar values for n are likely to appear in typical 60GHz environments. Due to the variation in the surrounding environments, the received power will be

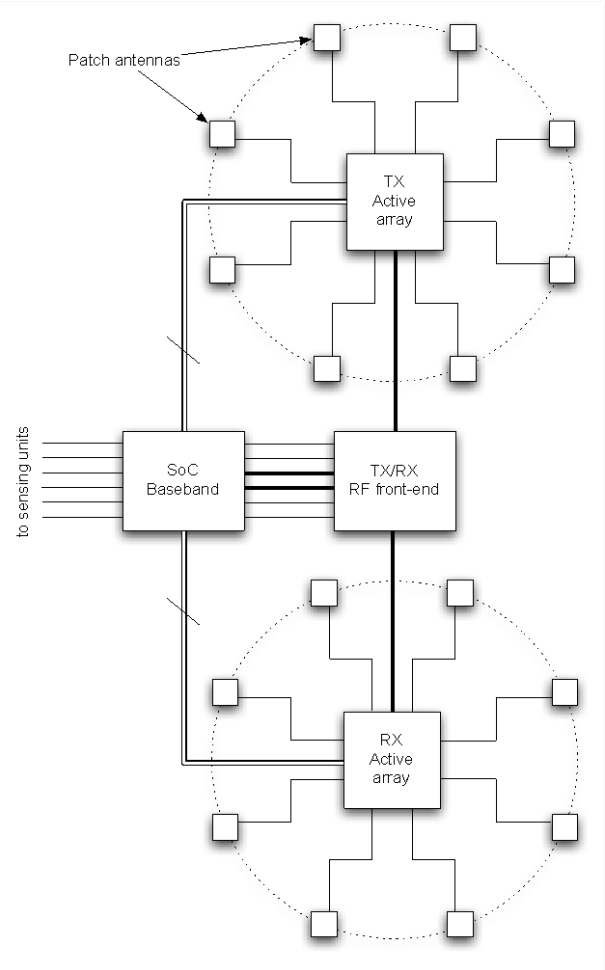

Figure 120: Active antenna array configuration

different from the mean value by the shadowing parameter. In the following, will be neglected and only the mean value is taken into account. However, depending on the environment, several dB of shadowing margin could become necessary for a more pessimistic estimation.

6.1.1 *Link budget configuration setup*

Three different configurations for the system have been evaluated. Table 9 summarizes the different distances achieved.

Case 1

The first considered configuration involves active array antenna to allow the communications. A design block of active antennas with the T/R part is proposed in Figure 120.

In this case an array of 8 patch placed following a circular shape yield around 15 dBi of total gain for the antenna. A proof of concept of power splitting network is proposed in Figure 121.

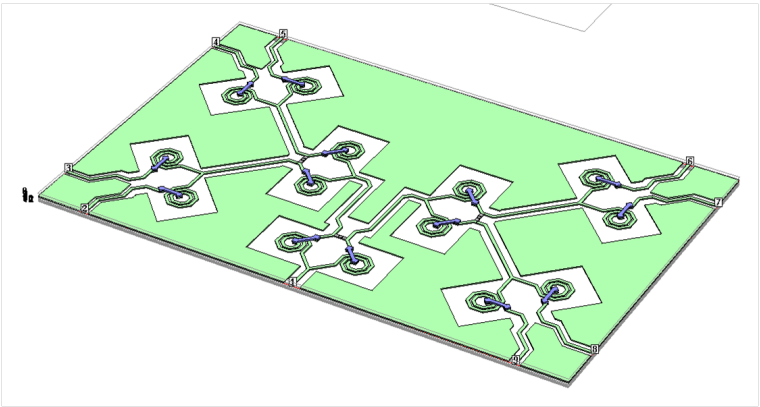

Figure 121: Proof of concept of power splitting network

Here, Wilkinson power splitters, discussed in section 2.5.1 are employed in a 1-IN-8-OUT network to connect the patch antennas. A simulation of insertion loss of the network is represented in Figure 122.

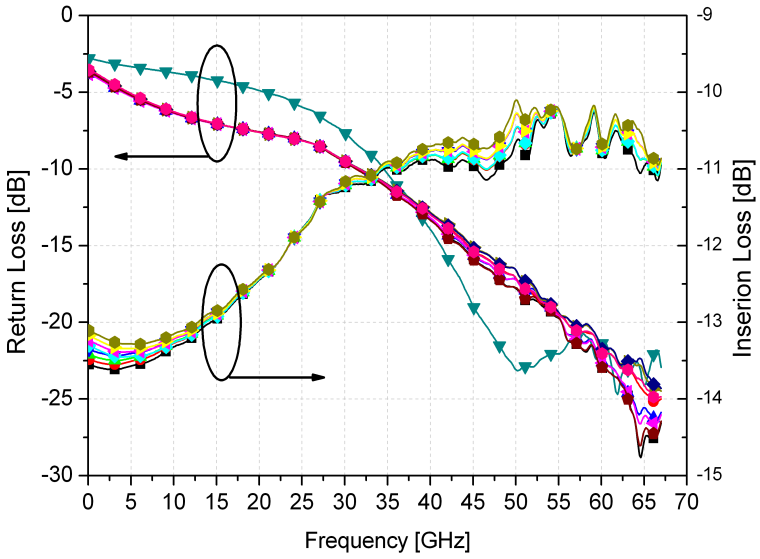

Figure 122: Response of Wilkinson power splitter network

The 1.5 dB of insertion loss can be recovered by the medium power amplifier proposed in section 3.3. As a consequence, placing a mid power buffer on each terminal of the splitting network the allowable power at coming into each patch antenna is approximately -1 dBm. Therefore, the total power sent in the array of antennas is +8 dBm as described in Table 9 "Case 1". Considering the power dissipation of the entire transmitter, the placement of medium power amplifiers

in the active array, increases the power dissipation of the total system. On the other hands, the exploit of distributed medium power amplifier at the place of the single power amplifier reduces the problem of power dissipation inside the power splitting network with great advantage in terms of temperature growth and total power dissipation.

As concern the receiver part, an active array can be exploited using the same strategy of the transmitter side. However being the power consumption of the LNA blocks higher than the medium power amplifiers one, the combining chain could be separate in two different stages and the LNA could be placed after the first stage of power combining. In this circumstances only 4 LNAs are required and the NF of the total receiver chain is not strongly influenced from the very reduced losses of the single stage power combiner 58.

Case 2

For the second case a single patch is considered antenna. This transceiver set up allows using the power amplifier produced by the IMS laboratory in the framework of the NanoComm project [17]. The performances in terms of power consumption are the same as represented in table 8 and table 7. However due to the low performance of the single patch antennas the reliability of the 60 GHz link is strongly reduced (the line of sight trasmission is lower than 1 meter). On the other hand this configuration is less influenced by dynamic obstacles (as a human body that can introduce loss as high as 36 dB [121] and[122]). The non high directive beam could than exploit the multipath to reconstitute part of the signals blocked in the LOS path.

Case 3

The third and last case considers the very low power configuration for the 60 GHz links. In this case as occurs for the case 2, only one patch antenna is exploited at the T/R blocks. In addition for the transmitter chain the power amplifier designed in [28] has been removed. The very short wireless link however is not necessary a problem because it will be exploited in all the application where the proximity constitutes an advantage. As described in the introduction chapter. Application as wireless billing requires very short distances in order to ensure the security of the payment or the transfer of sensible information. In this case thanks to the extremely low power consumption, the 60 GHz system could be supported by the new energy harvest solutions to assure the power supply.

6.2 LINK DEMONSTRATION

The demonstration of the 60 GHz link constitutes the final step for this thesis work. Despite the problem discussed during the characterization of the 60 GHz

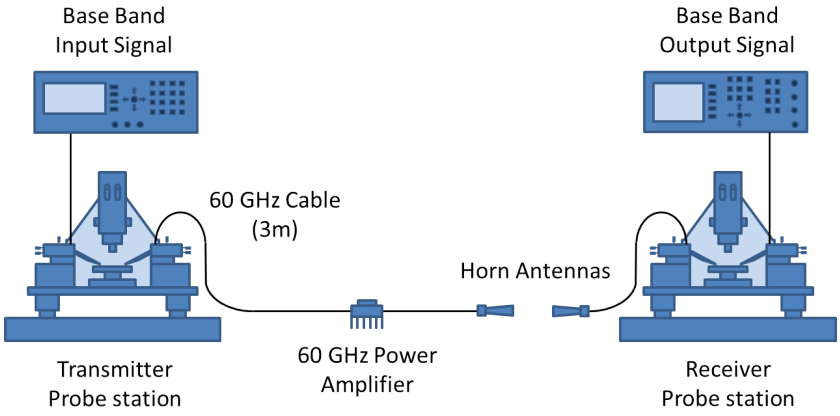

Figure 123: 60 GHz link set-up

receiver a demonstrator system has been organized to verify the possibility to yield a 60 wireless communication.

The measurement has been accomplished by using probe stations to exploit nude chip for transmitter and receiver part. As a consequence several logistic issues have to overcome after to start the test. The first and most important issue was the placement of the two probe stations. The distance between the two instrumentations cannot be changed and consequently 60 GHz cables are required to approach the transmitting and receiving point.

The setup proposed for the demonstration is represented in Figure 123 and Figure 124 represents the photo of the LAAS characterization room were the demonstration has been done.

In order to assure linearity to the signals and knowing the power levels delivered by the transmitter block 4 meters of 60 GHz coaxial cable is employed to approach the probe stations. The considerable losses added from the RF probe in the probe station and to the cables reduce enormously the already feeble signal emitted by the transmitter 5.1.5. To restore the power levels an MMIC low noise amplifier has been placed at the end of the first 3 meters of V cable (as shown in Figure 123). The output of the LNA is therefore connected to another 50 cm of V cable to the emitting horn antenna. On the other side (reception block) the horn antenna is connected to the RF input probe by 50 cm of V cable. The LNA amplifier is an MMIC component, it yields a gain of 31.7 dB at 60 GHz. The sum of losses added by the cables and probe station is 27 dB therefore the LNA amplifier add 4.7 dB at the power emitted by the transmitter.

The result of the test is shown in Figure 125 where a single side of the differential base band signal is is acquired by the Rohde & Schwarz spectrum analyzer. The power level of the down-converted signal is extremely low due to the bad functioning of the receiver. However, if the single branch receiver version [27] is employed the reliability of the system will be assured.

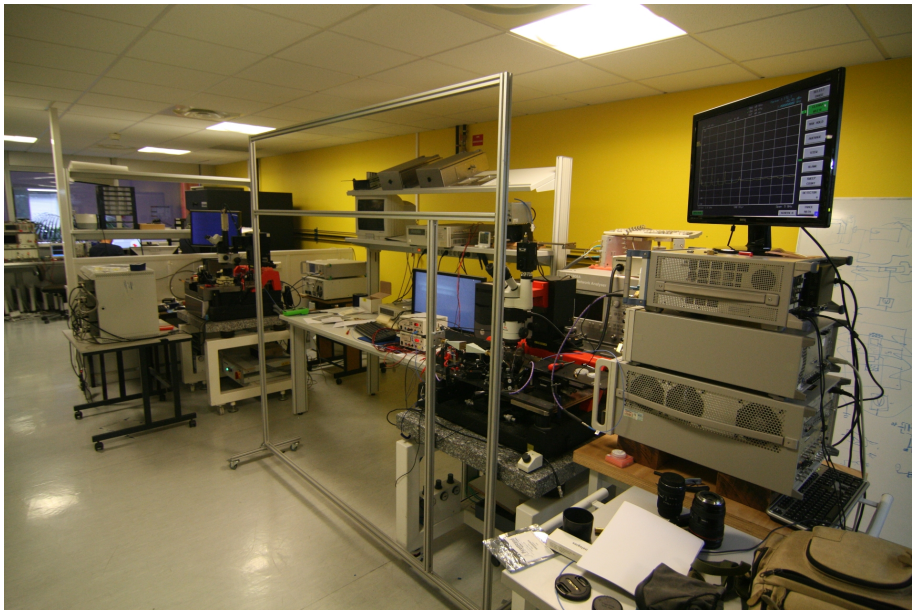

Figure 124: LAAS characterization room

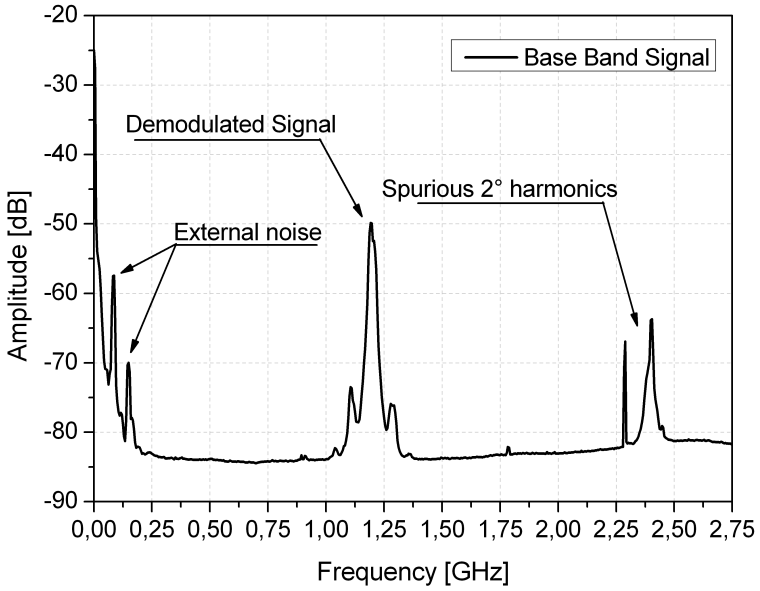

Figure 125: Results of the 60 GHz demostration link

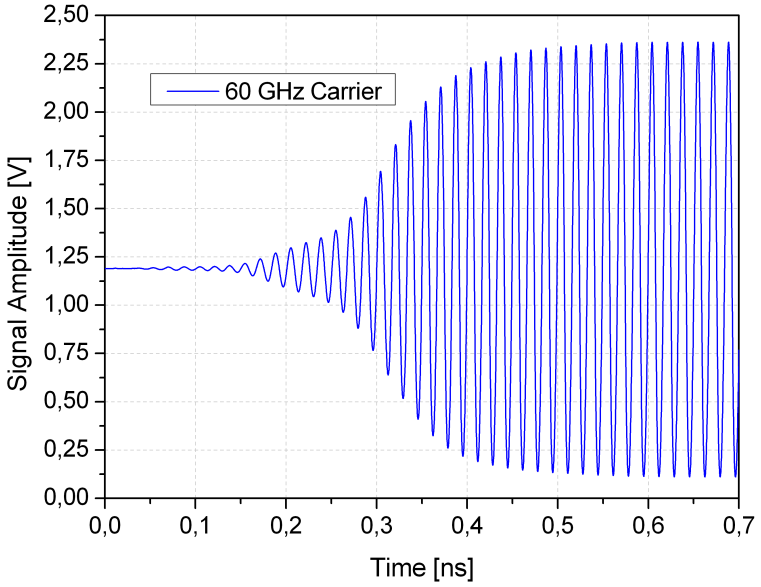

Figure 126: Switch on of the voltage controlled oscillator

6.3 ENERGY SAVE MODE

The proposed transceiver system, shows in the configuration proposed in "Case 3" of link budget Table 9 works with a total instant power of 130 mW, whereas in configuration with PA or Active array it requires the 220 mW. In these conditions the transceiver is capable to work with a considerable reliability for long time periods. In very high data rate link, the transceiver work continuously without interrupts. On the other hand in all of communication links where the bitrate is lower than hundred of kbps energy save approach could be implemented.

Figure 126 shows the run up time required for the VCO to generate a stationary RF carrier. Considering results of Figure 126 it is possible to affirm that the VCO requires less than 1 ns to give out a stable carrier to up-converts the signal coming from the BB circuitry. With a base band link of 10 Kbps it could be possible to turn off the transceiver part during the non-working time. With the rapidity exibiths by the VCO the analog part of the system offers the possibility to strongly reduce the energy consumption. PHY layer in [25] generates BB pulse with a maximum time duration of 2 ns. By including a security margin of 2 ns to start-up and turn off the system, the total time in which the analog part of the transceiver systems work for each bit correspond to 4 ns. In each second of data transmission there are 10 Kbps as a conequence the total working time of the transceiver is $4 \times 10^{-9}[\text{s}] \times 10^{5}[\sharp\text{bits}] = 40\ \mu\text{s}$. Considering the best case described in Table 9 the total energy consumption per second, then, correspond to: $4 \times 10^{-4}\ [\text{s}] \times 0.13\ [W] = 52\ \mu\text{J}$ for each second. In terms of power per bit, instead, it results: $4 \times 10^{-9}\ [\text{s}] \times 0.13\ [W] = 520\ \text{pJ}$

In the others two configuration the energy consumption corresponds respectively to 88 μJ per second and 880 pJ per bit.

In the case of 100 Mbps link, the bits would be transmitted every 10 ns. Thanks to the VCO run-up speed, the transceiver ON-OFF configuration will be maintained and, the transceiver system could be maintained switched off for at least the 60% of time. As a consequence there will be considerable advantages for the lifetime extansion of the battery supply.

CONCLUSIONS AND PERSPECTIVES

7

GENERAL CONCLUSION AND PERSPECTIVE

The objective of this thesis work was the design and characterization of a transceiver front-end for 60 GHz UWB application. The principal features required for the system are a low power consumption, small size and an output power that allows obtaining reliable communications links up to 10 m.

The work started with the synthesis of a robust design flows to create passives blocks as inductors and wave guide lines (microstrips, coplanar wave guides and slow-wave prototypes) in order to complete the ST Microelectronics design kit. The research upon the inductors has given a reliable methodology of design that in a second step has supported the design of more complex structures as balun, hybrid coupler and power splitters.

The need to maintain small dimensions for the entire system has pushed the research towards new architectures. The developed baluns, together with the conceived Wilkinson power splitter, constitute the actual state of the art with regard to the occupied area on the chip surface. In addition, the reduced size of the component improves the insertion loss by decreasing the field dispersion on the low resistivity CMOS substrate.

Concerning the circuits, seen as stand-alone block, the up conversion mixer has assumed the principal role in the design of transmitter chain. In the proposed homodyne architecture the mixer constitutes the main issue to overcome. The strategy followed in this thesis has been based on the evaluation of the RF power level inside the chain and over the principle that RF power generated in the base band is more efficient than the generation of high level of RF power at 60 GHz. For this reason a passive mixer topology has been chosen. The ring mixer offers higher compression point by using wider transistors and, at the same time, zero power dissipation. The principal problem, tackled and solved during this thesis is the reduction of the high conversion loss that characterizes this family of mixers. Starting from the analysis of the single switching transistor up to the design of the mixer core and the relative input and output matching network the conversion loss are reduced up to -9 dB with relatively low local oscillator driving signal. The proposed mixer constitutes the state of the art of passive mixer in 60 GHz band with its -9 dB of conversion gain and its 0 dBm of input power 1 dB compression point. The realization of the others block with partial reuse of already designed topology has been done following this strategy. A wide research over the state of the art with the evaluation of the most energy saver topologies has been done and when possible innovative solution or improvement of the existing architecture has been accomplished.

The last step of the thesis has focused on the integration in the two different chips of the transmitter and receiver chains. Both realized dies have been characterized and excellent result has been reached with the transceiver part. The highest ICP value of the mixer combined with its zero power dissipation yields an extremely efficient transmitter. The experimental characterization shows a very wide operative bandwidth for the transmitter with really high performances in terms of linearity and gain. Thanks to this high performance combined with very low power consumption, the proposed architecture finds an ideal application field in the battery driven wireless sensor network. With only 53 mW of DC power dissipation it yields up to 0 dBm of output power (considering the CP_{-1dB}) and it occupies only 0.6 mm^2 of silicon surface. Some studies to increase the transmission range for the transmitter are already started, and the uses of smart antennas with active arrays are in phase of evaluation. The employment of a very compact and reduced losses device together with the proposed low power mid amplifier could increase rapidly the range of functioning of the whole proposed transmitter maintaining a reduced dissipation power for the entire system as well.

On the other hand receiver chain suffers from a bug on the design of base band variable gain amplifiers. As a consequence its characterization has not been terminated.

Despite this inconvenience, a proof of concept of the 60 GHz link has been carried out by using the leakage signal flowing through the base band variable gain amplifier. By using the simpler version of the receiver distances between 10 cm and 10 m can be reached.

In perspective, works has to be done to improve the design of VGA and therefore a new version of receiver is expected.

Studies on the flexible substrate integration of the whole system, as anticipated in the Introduction are scheduled in the framework of future projects. The minimization of the total power consumption to increase the energy efficiency of the system continues to be the main prerequisite.

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