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UNIVERSITÉ DE GRENOBLE

THÈSE

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dans **l'École Doctorale EEATS**
et de **Nano Device Laboratory Korea University**

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Electrical properties and modeling of Advanced MOS devices: FD-SOI Tri-gate device, Junctionless Transistor, and Amorphous-Oxide-Semiconductor Thin Film Transistor

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ABSTRACT

Novel advanced metal-oxide semiconductor (MOS) devices such as fully-depleted-silicon-on-insulator (FD-SOI) Tri-gate transistor, junctionless transistor, and amorphous-oxide-semiconductor thin film transistor were developed for continuing down-scaling trend and extending the functionality of CMOS technology, for example, the transparency and the flexibility. In this dissertation, the electrical characteristics and modeling of these advanced MOS devices are presented and they are analyzed.

For the theoretical basis, at first, the scaling effect in MOS devices was briefly covered. With down-scaling trends, CMOS devices technology has scaling effects such as short channel effects and narrow channel effects. While the device scale is shrunk, the general scaling rule can be applied to keep the device performance. And mobility, the important parameter to characterize the device can be defined as conductivity mobility and the mobility in metal-oxide semiconductor field effect transistor (MOSFET). The effective mobility in MOSFET is affected by several scattering mechanisms, which mainly consist of lattice scattering, ionized impurity scattering, and surface roughness scattering. Accordingly, the effect of dominant scattering effects is shown as device operation influenced by temperature and the effective field. Besides, the performance of the device is varied by the series resistance and the substrate bias. At last, the conduction in amorphous oxide semiconductor thin film transistor incorporating the band-tail states was introduced.

For the measurement of the electrical characteristics of MOSFET, the proper measurement equipment should be utilized. It is worth to note that several kinds of voltmeter have different measurement limit each other. The practical tips for precise measurements such as the guarding technique are also important to avoid possible measurement errors. The electrical parameters can be extracted by the characterization methods such as Y-function and C-V measurement technique. In addition, there are extraction methods for electrical parameter, for example, the threshold voltage, the series resistance and trap density. 2-dimensional (2-D) numerical simulation is also indispensable tool for the proper physical interpretation of electrical characteristics in MOSFET.

The sidewall mobility trends with temperature in multi-channel tri-gate MOSFET showed that the sidewall conduction is dominantly governed by surface roughness scattering. The degree of surface roughness scattering was evaluated with modified mobility degradation factor. With these extracted parameters, it was noted that the effect of surface roughness scattering can be higher in inversion-mode nanowire-like transistor than that of FinFET. The series resistance of multi-channel tri-gate MOSFET was also compared to planar device having same channel length and channel width of multi-channel device. The higher series resistance was observed in multi-channel tri-gate MOSFET. It was identified, through low temperature measurement and 2-D numerical simulation, that it could be attributed to the variation of doping concentration in the source/drain extension region in the device.

ABSTRACT

The impact of channel width on back biasing effect in n-type tri-gate MOSFET on SOI material was also investigated. The suppressed back bias effects was shown in narrow device (W_{top_eff} = 20 nm) due to higher control of front gate on overall channel, compared to the planar device (W_{top_eff} = 170 nm). The variation of effective mobility in both devices was analyzed with different channel interface of the front channel and the back channel. In addition, 2-D numerical simulation of the the gate-to-channel capacitance and the effective mobility successfully reconstructed the experimental observation. The model for the effective mobility was inherited from two kinds of mobility degradations, i.e. different mobility attenuation along lateral and vertical directions of channel and additional mobility degradation in narrow device due to the effect of sidewall mobility.

With comparison to inversion-mode (IM) transistors, the back bias effect on tri-gate junctionless transistors (JLTs) also has been investigated using experimental results and 2-D numerical simulations.

Owing to the different conduction mechanisms, the planar JLT shows more sensitive variation on the performance by back biasing than that of planar IM transistors. However, the back biasing effect is significantly suppressed in nanowire-like JLTs, like in extremely narrow IM transistors, due to the small portion of bulk neutral channel and strong sidewall gate controls.

Finally, the characterization method was comprehensively applied to a-InHfZnO (IHZO) thin film transistor (TFT). The series resistance and the variation of channel length were extracted from the transfer curve. And mobility values extracted with different methods such as split C-V method and modified Y-function were compared. The static characteristic evaluated as a function of temperature shows the degenerate behavior of a-IHZO TFT inversion layer. Using subthreshold slope and noise characteristics, the trap information in a-IHZO TFT was also obtained. Based on experimental results, a numerical model for a-IHZO TFT was proposed, including band-tail states conduction and interface traps. The simulated electrical characteristics were well-consistent to the experimental observations.

For the practical applications of novel devices, the electrical characterization and proper modeling are essential. These attempts shown in the dissertation will provides physical understanding for conduction of these novel devices.

Keywords: advanced MOS transistors, multi-channel tri-gate MOSFET, junctionless transistor, sidewall mobility, surface roughness scattering, series resistance, electrostatic coupling, channel width variation, back bias effect, 2-D numerical simulation, a-InHfZnO, thin film transistor (TFT), DC characteristics, electrical parameter extraction, low frequency noise (LFN), numerical simulation.

INTRODUCTION

The most important trend of CMOS technology is to decrease the minimum feature size and cost-per-function. According to the ITRS roadmap, the minimum feature size of MOSFET in 2026 is predicted as 6 nm [1]. The CMOS scaling consists of two approaches, geometrical scaling and equivalent scaling. Geometrical scaling reduces the physical feature size according to Moore's law, inspiring semiconductor industry. The equivalent scaling improves the performance of the devices and is increasingly important from nowadays and new design/processing or software solutions are needed for the scaling. As the size of device is shrunk extensively, more efforts to maintain the performance of devices is dedicated against short channel effects, dopant-induced fluctuation in threshold voltage, etc [2-4]. For example, high-k gate dielectric has been used to scale down the equivalent oxide thickness (EOT) with keeping tolerable gate leakage current. Metal gate electrodes are employed in the CMOS device of recent generation for efficient gate control to channel since even degenerately doped polysilicon gate reduces metal-oxide-semiconductor capacitance with its depletion layer [5]. Higher-k dielectric and appropriate metal gates are required for further scaling as shown in Fig. 1. In addition, metal gate provides low gate resistance and efficient heat sink which is for power aspect. To improve the channel carrier low-field mobility, strained silicon is also used as a channel material [6, 7] and higher mobility materials, for example, SiGe, Ge, and III-V compound semiconductor will be used. (Fig. 1) Instead of thick body partially-depleted-silicon-on-insulator (PD-SOI) or bulk MOSFET, ultra-thin body fully-

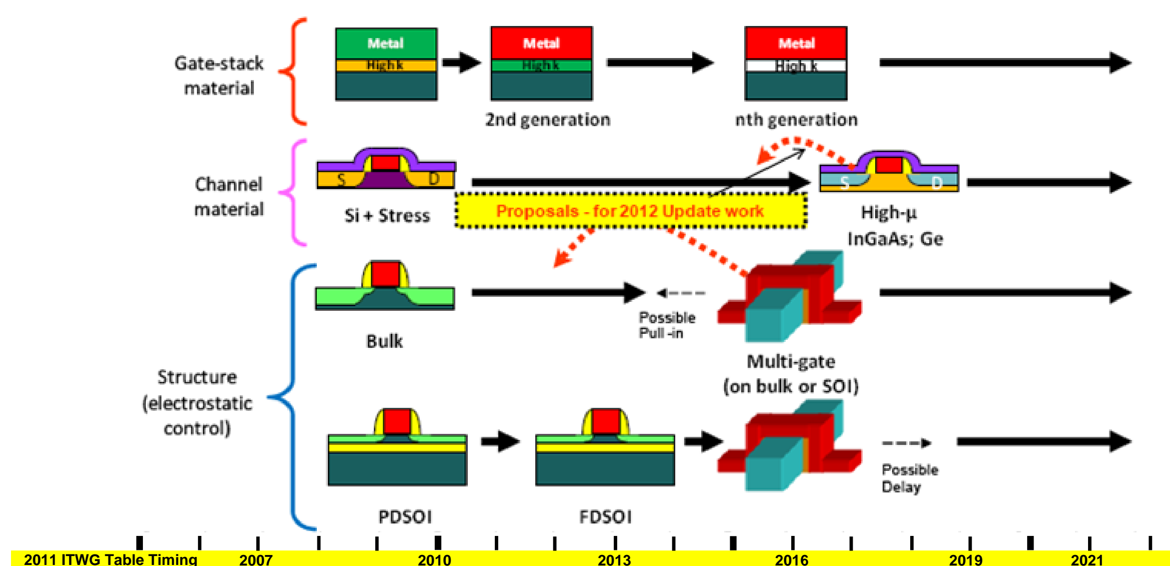

Figure 1 2011 ITRS "Equivalent Scaling" Process Technologies Timing [1]

depleted-silicon-on-insulator (FD-SOI) and multiple-gate MOSFET are expected as potential device to eliminate the variation threshold voltage corresponding to increased doping concentration.

On the other hand, various channel material, device architecture and technologies are required to meet the need of ultra-low power consumption and new functionality. For example, thin film transistor (TFT) is a promising device for flexible and transparent electronic circuit. The active channel material is deposited at low temperature (< 600 ^{o}C), thus glass substrate and flexible substrate can be used and the channel material is amorphous. TFT can be widely used for large-area transparent and flexible display [8, 9] which are challenging with conventional semiconductor processing. For these applications, TFT is feasible device type since the required device performance such as response speed and the driving current is not quite critical while it is not used for integrated circuits owing to its low channel mobility.

For the realization of these advanced devices, it is required to investigate their electrical properties compared to classical transistor and to optimize their performance. To perform this task, physical parameters of these new devices should be evaluated based on analysis method of classical silicon devices which has been enormously investigated during previous decades. The development of their device model and the investigation of special mechanisms governing their electrostatics accompanying with special electrical properties and non-conventional effects should be carried

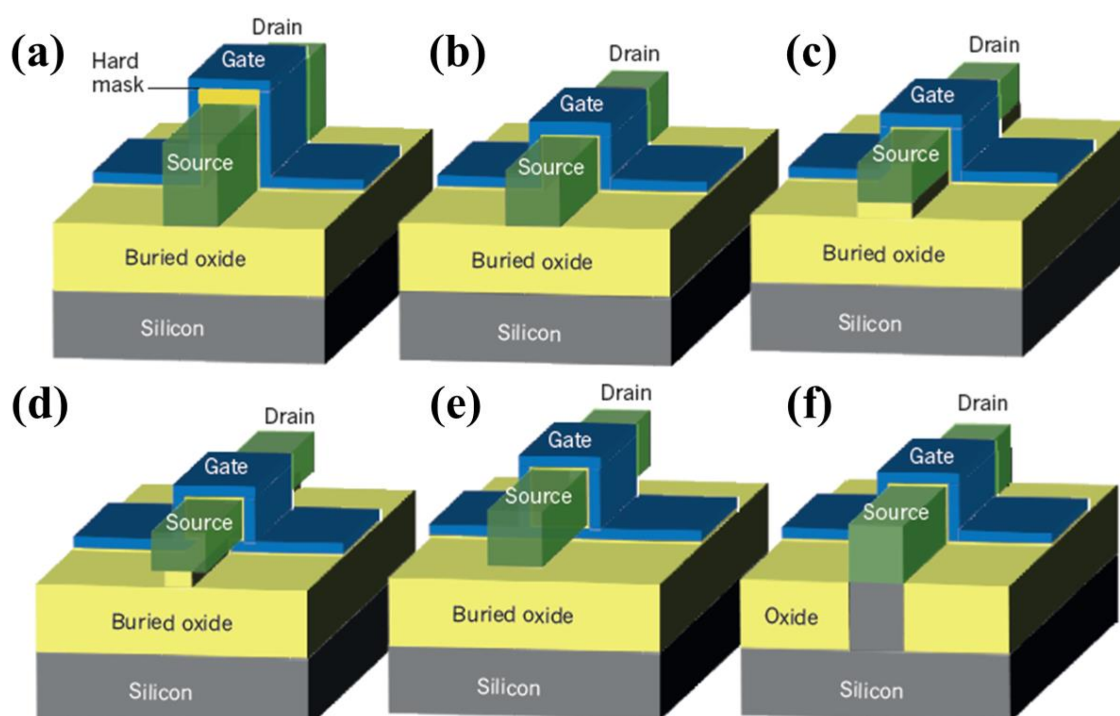

Figure 2 Multigate MOSFETs (a) SOI FinFET (b) SOI triple-gate MOSFET (c) SOI Π-gate MOSFET (d) SOI Ω-gate MOSFET (e) SOI gate-all-around MOSFET (f) A bulk tri-gate MOSFET [10]

out.

Fully-depleted silicon-on-insulator (FD-SOI) Trigate device is one of the new potential structures for continuing scaling down CMOS technology [10]. Indeed, FD-SOI structure eliminates punch-though effect with the shallow source/drain region and it can be free from the high channel doping problem [11]. It is very difficult to control the concentration of channel doping in extremely small device and spatial random dopant fluctuation seriously degrades the device reliability. Low channel doping concentration of FD-SOI device also enables to achieve enhanced channel mobility. Furthermore, the parasitic capacitance between interconnect metal lines and substrate is reduced owing to the buried oxide and the switching speed is enhanced. The reduction of parasitic devices, called as latch-up phenomenon in CMOS ICs is another benefit of using FD-SOI structure. With FD-SOI structure, the implementation of multi-gate structure can also be interesting to enhance device performance. Multi-gate MOSFET shows the best subthreshold swing and significant reduction of off-state current [12, 13]. It shows better control of short channel effects [14] since the influence by drain field on the channel is reduced [15]. As shown in Fig. 2, the multi gate MOSFET includes FinFET, tri-gate MOSFET, Π-gate MOSFET, Ω-gate MOSFET, gate-all-around MOSFET, and a bulk tri-gate MOSFET. In recent device simulation studies, it was shown that the gate-all-around device with gate length of 3 nm could work well without significant short channel effects [16]. In addition, multi-gate device, having large channel width, can be used to drive higher current than single gate device. For double gate SOI device, threshold voltage is low, compared to the bulk single gate SOI device and DIBL effect is reduced [17]. FinFET also shows many advantages such as increased drive current, reduced short channel effect and shorter access time for memory applications [18].

In 2011, among multigate structure, Trigate MOSFET was introduced to the mass industrial production by announcement, Intel will use tri-gate structure for 22-nm technology. Trigate means that a single gate electrode folded to cover three sides of transistor [19]. The gate is a common gate, thus, three gates are electrically connected and apply the same gate bias. A Trigate MOSFET shows improved gate electrostatic control to the channel and this effectively reduces short channel effects [20, 21]. It provides strong gate control over not only at the top surface channel but also on two sidewall channels (lateral channels) [22, 23]. Due to their gate control property, they have less stringent requirements for the silicon channel dimensions and larger driving current per unit area of the silicon wafer can be achieved [21, 24]. Especially, the introduction of metal gate on the trigate structure enhances the on-current and eliminates the leakage current as well as inverter delay. In narrow trigate transistors, it was shown that the device has the immunity against substrate effects caused by drain-induced virtual substrate biasing and hot carrier-induced charge build-up in the buried oxide [25]

On the other hand, the formation of ultra-shallow junctions with abrupt high channel doping concentration gradients is still very difficult as the device size becomes extremely small. The junctionless

transistor (JLT) can be free from this difficulty since it doesn't have junctions or doping concentration gradient corresponding to junction (Fig. 3). In addition, JLTs using silicon nanowires are compatible with CMOS process.

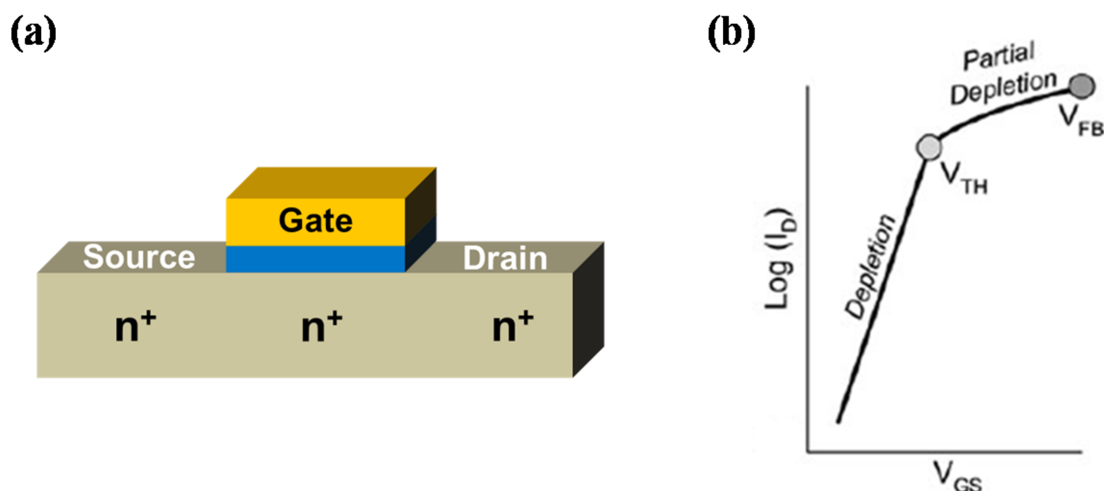

Figure 3 (a) Longitudinal cross-section schematic of a junctionless transistor, showing the doping profiles and (b) Drain current (log scale) versus gate voltage in a heavily-doped junctionless transistor [18]

The junctionless transistor is a "normally on" device, however, the difference of the work function between the gate electrode and the channel silicon make the flatband voltage V_{FB} and the threshold voltage V_{TH} shifted. Below threshold, JLT is fully depleted and the carrier concentration of a part of channel of JLT reaches initial doping concentration N_D at its threshold voltage. As increasing the gate voltage the region where carrier concentration is same with N_D becomes larger in cross-section of the channel. Finally when the channel cross section is full with region of carrier concentration $n=N_D$, the gate bias corresponds to the flat band voltage. The conduction mechanism in JLT was presented in Fig. 3(b).

The fabrication of JLTs is very simple since only one doping concentration is needed from source region to drain region. The subthreshold slope of JLTs are excellent, exhibiting 64 mV/decade at room temperature and very close value to the ideal value of subthreshold slope in the temperature range of 225-475 K [26]. Different from the general concerning, the mobility is not seriously degraded by high doping concentration in JLTs since the electric field in the channel is almost zero, allowing bulk mobility values [27]. The carrier mobility of JLT is lower than that of IM device at room temperature owing to the mobility dominantly governed by ionized impurity scattering. However, the decrease of mobility in JLT is less than 7 % when the temperature is increased up to 200 ^oC while it was about 36 % with IM device [28]. Furthermore, high I_{on}/I_{off} ratio, lower DIBL and reduced short-channel ef-

fects were reported in nanowire-like JLTs [29,30]. It can be expected that the variation of the threshold voltages of JLTs is below 35 mV with recent technology controlling channel thickness below 0.2 nm since the variation of threshold voltage is not severe when the channel thickness of JLT is small enough [31]. The variation of L_{eff} caused by gradient of doping concentration at junction boundary is not observed in JLT.

However, JLTs are more sensitive than undoped IM devices to doping fluctuation due to its high doping concentration [32]. Moreover, Rios et al reported that JLT devices show degraded gate control and short-channel behaviours and increased off current while they exhibit better mobility at moderate doping concentration [33]. There is also a theoretical approach showing significant variation of threshold voltage in JLTs due to the dopant fluctuation when L_g = 20 nm [34].

Another candidate for advanced MOS device technology, transparent amorphous oxide semiconductor (AOS) based TFTs have gotten great interest for the applications in flexible displays, flat-panel displays, optical sensor, solar cells, transparent and/or flexible electronic devices since they can be fabricated on plastic substrates at relatively low temperature [9, 35]. They also can be used for the highly uniform and large-area displays with low cost [36]. Among the AOS TFT, a-InGaZnO (a-IGZO) TFT has been intensively studied because it exhibits high mobility, a good on/off ratio and sufficient electrical stability [37]. It is mostly used for the application of switching/driving devices in active-matrix liquid crystal display (AMLCD) and active-matrix organic light emitting diode display (AMOLED) back planes due to its excellent electrical properties, compared to a-Si TFT [9].

The scaling effects on electrical properties of a-IGZO TFTs were investigated by Cho et al [38]. They examined the threshold voltage shift, subthreshold swing degradation and the field-effect mobility in scaled-down devices owing to short-channel effect and contact resistance. Stability issue in AOS TFTs

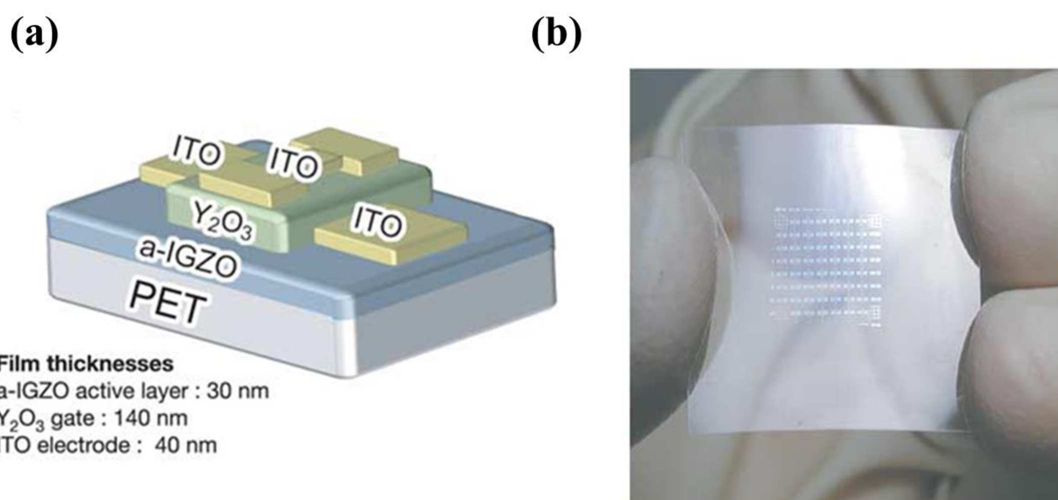

Figure 4 (a) Schematic of of a-IGZO TFT fabricated on a plastic sheet, PET. (c) A photograph of transparent a-IGZO TFT on flexible sheet [36].

has also been intensively studied by researchers. In many research results, the variation of threshold voltage in AOS TFT after electrical stress comes from charge trapping/detrapping at, or close to, channel/insulator interface [39-41]. It takes times, from few minutes to few hours, to recover the original properties of AOS TFT [42, 43] and, in some cases, heating treatment is required for the recovery. It is reported that using passivation layer improves the stability of AOS TFT [44, 45]. For what concerns the dielectric layer, high-k material increases the gate capacitance, leading to low subthreshold swing though high trap density. But most of high-k dielectric has issues of high leakage current, low breakdown voltage and rough surface [46, 47]. Park et al reported that the introduction of Hf to channel materials enables to fabricate highly stable and high performance TFT devices. Concerning the reliability of AOS TFT, the investigation of interface states is also important. Low frequency noise measurements in AOS TFTs have provided meaningful trap information in AOS TFTs [48-50]

The objective of this thesis lies on the development of the advanced semiconductor device models and the characterization of the conduction mechanisms in these devices. This thesis covers three kinds of devices: inversion-mode trigate FD-SOI MOSFET, Junctionless transistor and AOS TFT. In chapter 1, the trend of device technology and effects corresponding to scaling are briefly introduced with theoretical background of the thesis. And some measurement precautions and electrical characterization methods, needed to study the electrical conduction in devices are followed in chapter 2.
In Chapter 3, the sidewall mobility and the series resistance in multi-channel tri-gate MOSFET are discussed via low temperature characteristics and examined by 2-D numerical simulation.
The impact of channel width on back biasing effect in multi-channel tri-gate MOSFET and the analysis of mobility behavior corresponding to interface quality are presented in chapter 4.
The back bias effect on tri-gate junctionless transistors (JLTs) using experimental results and 2-D numerical simulations are described in chapter 5.
In chapter 6, electrical characterization of amorphous InHfZnO (a-IHZO) TFTs through static characteristic, low frequency noise characteristic and 2-D numerical simulation are summarized.

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CHAPTER 1

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THEORETICAL BACKGROUND

In this chapter, the general scaling rule in MOSFET to maintain the performance of the device is introduced. However, practically, the effect of scaling on the operation of the device such as short channel effect or narrow channel effect is common in I-V characteristics of MOSFET. Carrier mobility, an important parameter to evaluate the device performance can be determined from several concepts. The effective mobility in MOSFET is influenced by the scattering mechanisms which mainly consist of lattice scattering, ionized impurity scattering, and surface roughness scattering. The device operation is also affected by temperature, series resistance, and substrate bias. At last, the conduction mechanism in amorphous oxide semiconductor thin film transistor is described.

1 DOWN SCALING OF MOSFET

1.1 General down-scaling rules of MOSFET

As the channel length of MOSFET is decreased, proper adjustment of other device parameters is needed to maintain the device performance. When the channel length is reduced, depletion widths of source and drain region meet each other and electrons are pulled by drain field from the source, which is called as punch-through effect. To prevent this effect, higher channel doping is required. For P-type substrate ($N_D \ll N_A$), the depletion layer width at source/drain is given as [1];

$$w_d \approx w_p \approx \sqrt{\frac{2\varepsilon_s(V_{bi}+V_R)}{qN_A}} \qquad (1.1)$$

where w_p is the depletion layer (m) of p-type silicon, ε_s is the dielectric permittivity (F/m) of the semiconductor, V_{bi} is the built-in potential, V_R is a reverse-biased voltage. However, introducing more dopants to the channel increases the threshold voltage V_T because of higher body factor γ ($V^{1/2}$),

$$V_T = V_{FB} + 2\phi_F + \gamma\sqrt{2\phi_F + V_{SB}} \qquad (1.2a)$$

$$\gamma = \frac{\sqrt{2\varepsilon_s q N_D}}{C_{ox}} \qquad (1.2b)$$

V_{FB} is the flat-band voltage, ϕ_F is the Fermi potential, V_{SB} is source-to-bulk voltage and C_{ox}

Channel length L	L/S
Channel width W	W/S
Gate-oxide thickness t_{ox}	t_{ox}/S
Substrate doping $N_{A,D}$	$N_{A,D} \times S^2$
Drain current $I_D \propto W/(Lt_{ox})$	$I_D \times S$
Input capacitance $C_{in} \propto WL/t_{ox}$	C_{in}/S
Maximum switching frequency $f \propto I_D/C_{in}$	$f \times S^2$
Cell area $A \propto WL$	A/S^2

Table 1 Down scaling rules of MOSFET when the gate length is reduced by S times.

is the gate-oxide capacitance (F/m^2). In order to keep reasonable threshold voltage value, the thickness of the gate oxide should be reduced. Accordingly, the input capacitance is increased and it is fixed by reduced channel width. The down scaling rules when the gate length is reduced by S times are summarized in Table 1.

1.2 Scaling effects on device performance

For a given current density, the channel mobility of short channel device is related to the drift velocity for given electric fields E as;

$v_d = -\mu_n E$ (for electrons) (1.3a)

$v_d = \mu_p E$ (for holes) (1.3b)

At low electric fields, the drift velocity has linear relation with the electric field as shown in Eq. (1.3a) and Eq. (1.3b). However, when the electric field is high, the drift velocity trend saturated to a constant value, deviating from the linear relation. It occurs before the pinch-off condition. In extremely short devices, the saturated velocity severely limits the drain current.

Drain induced barrier lowering (DIBL), the one of the short channel effects, is the origin of punch-through effect. As shown in Fig 2, it causes the barrier at source end to reduce by high drain bias and

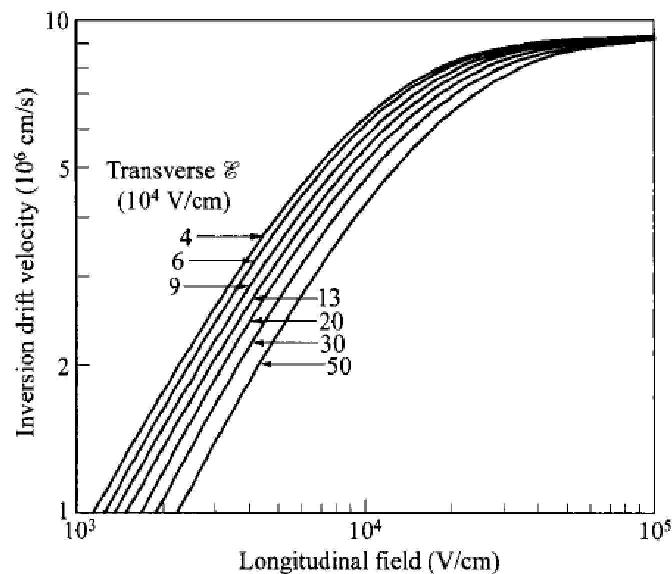

Figure 1 Inversion drift velocity versus longitudinal field for various transverse fields. [2]

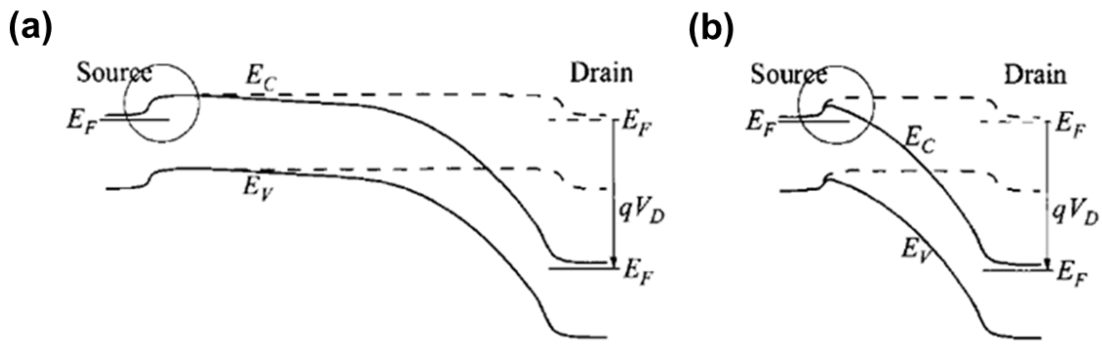

Figure 2 The energy-band diagram from source to drain at V_D > 0 V for (a) long channel and (b) short channel in transistor. Dashed line for V_D = 0 V [3].

the substantial increase of the drain current [3]. With punch-through effect, DIBL is presented by the reduction of threshold voltage and the increase of off-state current with drain voltage. For short channel devices, the subthreshold drain current increases with drain voltage while subthreshold swing is increased as a result of threshold voltage shift. On the other hand, the subthreshold drain current is not changed with drain voltage in long channel device [4]. For extreme case of DIBL, the device doesn't turn-off.

The narrow width effect (NWE) is another scaling related effect. It corresponds to an increase of the threshold voltage when the channel width is below 1μm in device using LOCal Oxidation of Silicon isolation. When the channel width is comparable to the edge effect region, the wider depletion region

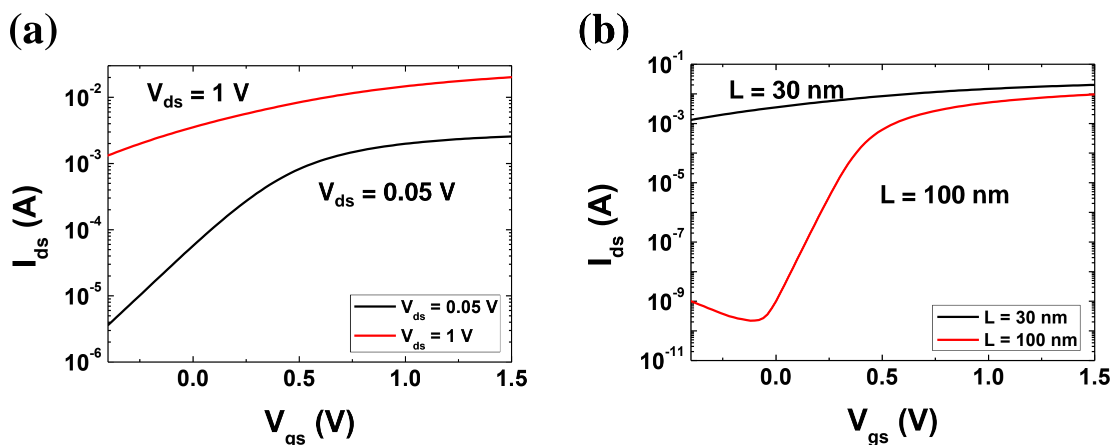

Figure 3 Drain characteristics of MOSFETs showing DIBL effects. (a) Transfer curves with L = 30 nm at V_{ds} = 0.05 V and V_{ds} = 1 V. (b) Transfer curves with L = 30 nm and L = 100 nm at V_{ds} = 1 V.

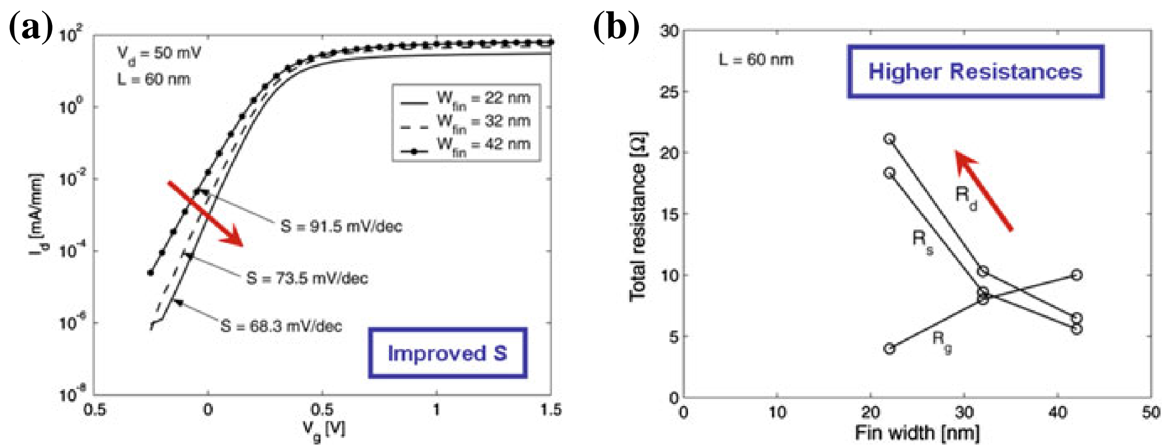

Figure 4 (a) transfer characteristic (b) extracted access resistances of 60 nm-gate length Fin-FET for different fin widths (W_{fin}) [5]

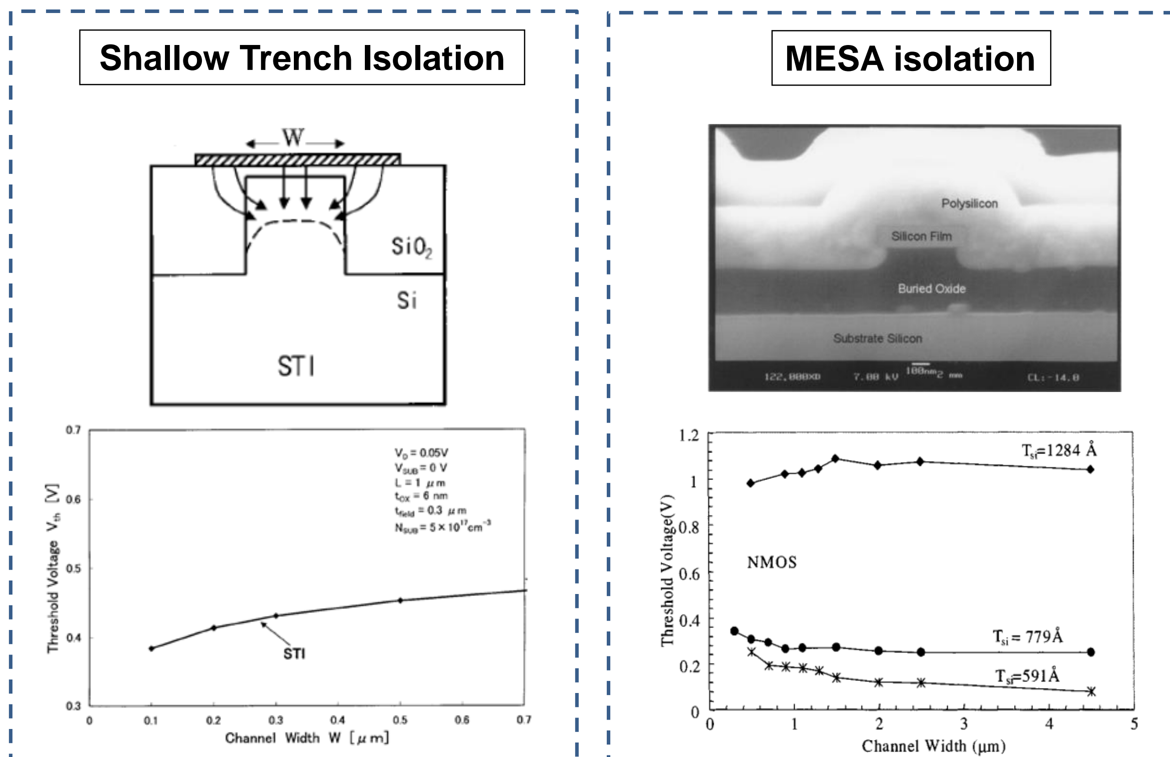

Figure 5 Variation of the threshold voltage with various channel widths for shallow trench isolation and MESA isolation. [6, 7]

by the gate voltage is observed. As a result, the depletion charge by gate voltage is increased and the threshold voltage is increased in very narrow devices. According to the isolation method, the variation of threshold voltage with channel widths exhibits different trend. As shown in Fig. 5, with shallow

trench isolation, the threshold voltage decreases with narrow channel width due to the gate fringing field [6]. In contrast, the thin channel device using MESA isolation shows increased threshold voltage with narrow channel configuration which eliminates effects of positive oxide fixed charge in BOX [7]. In SOI device, the narrow channel width is useful for better controllability for short channel effect. FinFET with narrow channel width exhibits limited DIBL and improved transport properties with small variation of threshold voltage [5, 8]. For gate-all-around nanowire devices, the subthreshold swing was reduced with using very narrow nanowire [9]. However, as the channel width is reduced, series resistance increases, which causes the decrease of drain current [10]. In multi-gate FETs, the device with heavily doped channel may present corner effect. As gate voltage is increased, the top corner of channel reaches inversion before top and sidewall surface channel is formed due to the overlap of electric field from top gate and sidewall gate. Figure 6 shows the derivative of transconductance curves for multi-gate FET with various channel doping concentrations from 10^{18} to 5×10^{19} cm^{-3}. The corner effect is illustrated by the derivative of transconductance curve having two humps when channel doping is high, corresponding to channel formation at top corner and surface. However, the corner effect is eliminated in a device with low channel doping concentration [11].

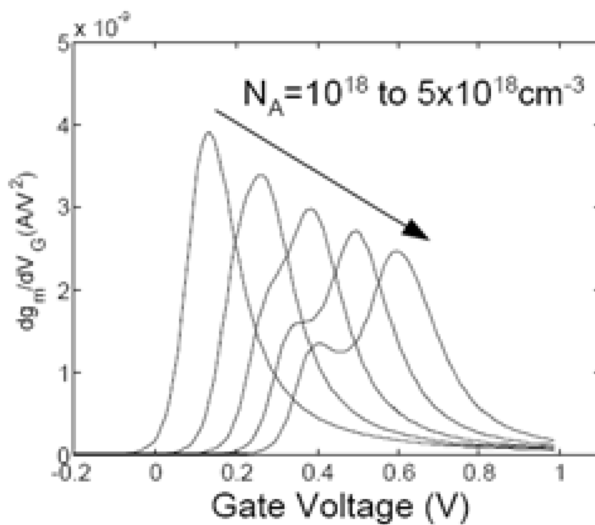

Figure 6 The derivative of transconductance in Ω-FET with various channel doping concentrations from 10^{18} to 5×10^{19} cm^{-3} [11].

2 MOBILITY

Carrier mobility is a macroscopic transport property characterizing semiconductor materials as well as device performance. Mobility can be affected by microscopic properties such as the effective mass and the degree of carrier scattering. For multiple scattering mechanisms, the net mobility μ is derived from the various mobilities, by Mathiessens's rule;

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \dots \qquad (1.4)$$

There are several kinds of mobility according to the definition method such as the conductivity mobility, Hall mobility, and effective mobility in MOSFET.

2.1 Conductivity mobility

The conductivity mobility is determined by measuring carrier concentration and the conductivity. For n-type semiconductor, the relationship between the conductivity σ (S/cm) and the conductivity mobility μ_n (cm^2/Vs) given by:[12]

$$\sigma = qn\mu_n \qquad (1.5)$$

where, q is the electron charge, n is the electron concentration ($/cm^3$).

The conductivity mobility comes from the drift of group of carriers by external electric field E. For example, when the external field in x-direction E_x is applied to a group of carriers, the group of carriers is forced by $-qE_x$ to move in x-direction. The average velocity of the group of carrier is called average particle drift velocity $< v_x >$.

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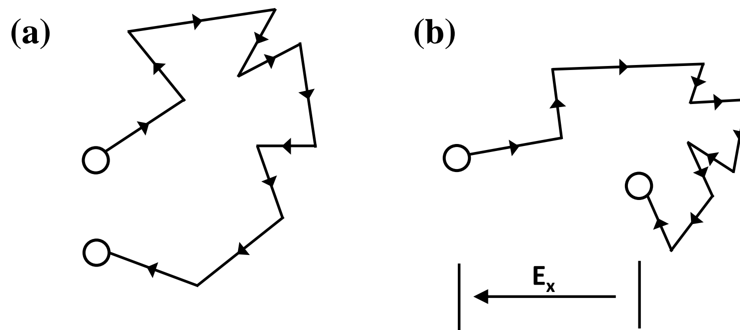

Figure 7 Drift of an electron as a result of thermal motion. (a) When there is no electric field, the electron randomly moves but ends up with no net displacement; (b) when an electric field is applied, the electron drifts opposite to the direction of the field and has a net displacement (and therefore a drift velocity).

The conductivity mobility μ_n is defined as the proportionality constant of the drift velocity to the electric field E_x. The net motion of the group of carriers is accelerated by the external field, however, there are many scattering sites such as crystal defects, vacancies, dislocations, impurities in a solid. Thus, the velocity of electrons is saturated with a constant electric field E_x.

$$< v_x > = \frac{< p_x >}{m_n^*} = -\frac{qt}{m_n^*} E_x = -\mu_n E_x \qquad (1.6)$$

where, $< p_x >$ is the average momentum per electron, t is the mean free time, and m_n^* is the effective mass of electron.

From the drift, the current density J_x is defined by:

$J_x = -qn < v_x >$ (1.7)

where $-q$ is the charge of electron and $n < v_x >$ is the number of electrons crossing a unit area per unit time [13].

And the current density is expected to be proportional to the applied electric field with Ohm's law as;

$J_x = \sigma E_x$ (1.8)

Applying Eq (1.6) and (1.7) to Eq. (1.8), the relation between the conductivity mobility and the conductivity shown in Eq. (1.5) is established.

2.2 Effective mobility

When the carrier flow is limited in the inversion layer the mobility is low, compared to the bulk mobility due to the interface effect and thin thickness of the inversion layer.

The effective mobility μ_{eff} is obtained at low drain voltage as:

$$\mu_{eff} = \frac{I_d L}{W Q_n V_d} \quad (1.9)$$

where I_d is the drain current and Q_n is the channel charge density (C/m^2), and V_d is the drain voltage.

There are two ways to obtain the channel charge density Q_n. The channel charge density Q_n can be approximated by just multiplying the effective oxide capacitance per unit area C_{ox} (F/m^2) with overdrive gate voltage at strong inversion $V_{gt}(= V_{gs} - V_{th})$ as:

$Q_n = C_{ox} V_{gt}$ (1.10)

It is simple but there are difficulties to obtain the exact value of C_{ox} and the threshold voltage V_{th}. Another way is to obtain Q_n directly from the measurement of gate-to-channel capacitance.

$$Q_n = \int_{-\infty}^{V_{gs}} C_{gs} dV_{gs} \quad (1.11)$$

where C_{gs} is the gate-to-channel capacitance per unit area. Usually, it provides better results, compared to the previous one [12].

As described in (Eq 1.6), the mobility is proportionality constant of velocity to electric field. When the field is low, the velocity is linearly increased with electric field and the mobility is constant. How-

ever, at high field, the velocity is saturated to constant value. When the electric field is between these two regimes, the effective mobility is given as;

$$\mu_{eff} = \frac{\mu_0}{[1+(E/E_C)^n]^{1/n}} \qquad (1.12)$$

where μ_0 is the low field mobility and E_C is the critical field. n is 2 for electrons and 1 for holes in silicon [3, 14]. The effective mobility is higher with lower channel doping concentration owing to reduced normal field and low threshold voltage.

The effective mobility μ_{eff} includes mobility degradation by the several scattering mechanisms such as phonon scattering, ionized impurity scattering and surface roughness scattering. The scattering effect is varied by the transverse field by gate bias and it can be presented in MOSFET by empirical relation as [15];

$$\mu_{eff} = \frac{\mu_0}{1+\theta_1(V_{GS}-V_T)+\theta_2(V_{GS}-V_T)^2} \qquad (1.13)$$

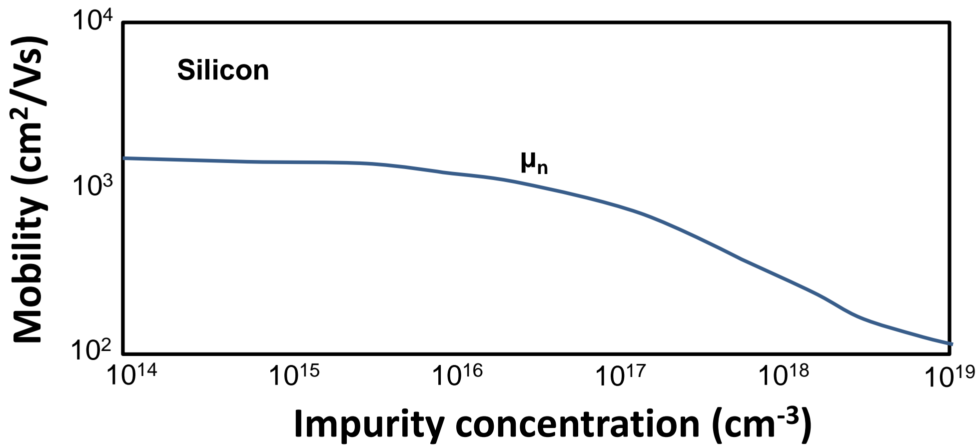

Figure 8 Electron mobility in silicon as a function of impurity concentration

θ_1, θ_2 are mobility degradation factors which are affected by gate oxide thickness and doping concentration. While classical effective channel mobility is presented by only first-order mobility degradation factor θ_1, recent MOSFETs have been scaled down and the second-order mobility θ_2 degradation factor is required since the drain current is significantly degraded at high field. It is known that this degradation is due to surface roughness scattering [16].

3 DOMINANT SCATTERING EFFECTS IN MOSFET

There are several scattering mechanisms which influence the mobility of MOSFET. They are phonon scattering (lattice scattering), Coulomb scattering (Ionized impurity scattering), and surface roughness scattering. Depending on the temperature and the effective electric field or the carrier concentration, different scattering mechanism governs the mobility behavior of MOSFET. The universal mobility

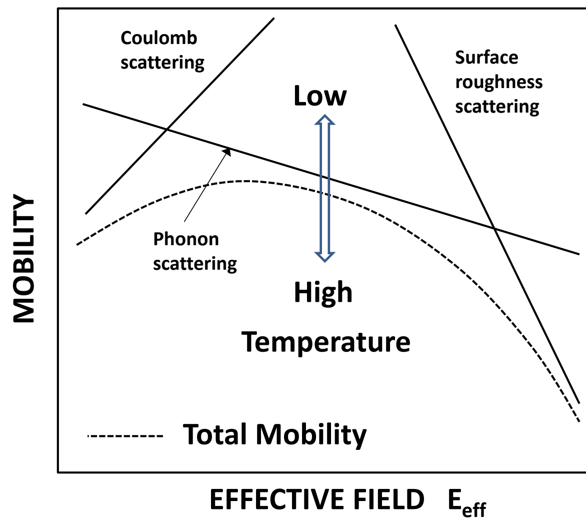

Figure 9 Schematic diagram of effective mobility as a function of the effective field E_{eff} with three scattering mechanisms, Phonon scattering, Coulomb scattering, and Surface roughness scattering

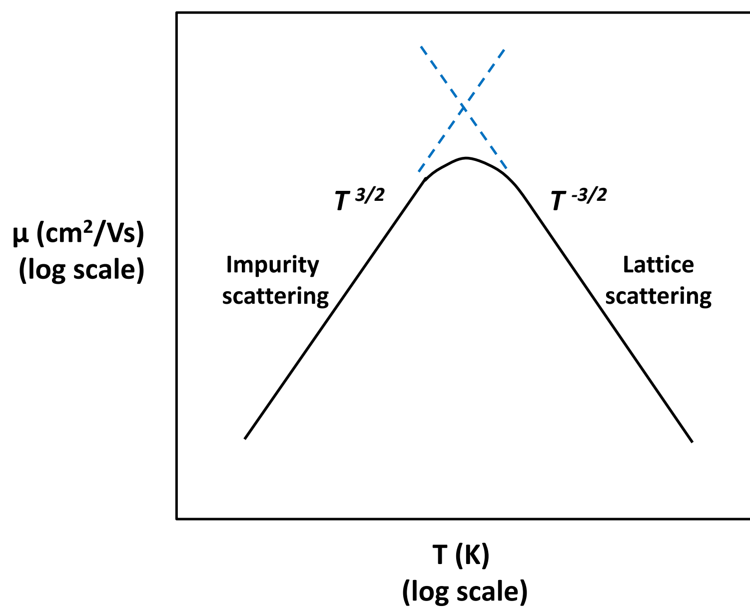

Figure 10 Approximate temperature dependence of mobility with both lattice and impurity scattering

behavior according to these scattering mechanisms depends on the effective field as shown in Fig. 9 [17].

At given temperature, crystalline lattice is vibrating with thermal energy. These vibrations are represented by particle called as "phonon". When a carrier moves in vibrating crystal lattice, this carrier is scattered by this vibration. As temperature increases, more vibration occurred and the mobility is reduced since the scattering rate increases. The mobility limited by phonon scattering is decreased with temperature ($\mu \sim T^{-3/2}$ in silicon) [3].

One of important scattering mechanisms for carrier transport is ionized impurity scattering. When temperature is low, lattice scattering is less important due to reduced lattice vibration, thus, ionized impurity scattering becomes the dominant scattering mechanism. In contrast with the effect of lattice scattering, the mobility increases with temperature (Fig. 10) since a carrier which moves fast with higher thermal energy less interacts with a charged ion than one moving slowly. The mobility approximately depends on the temperature as $T^{3/2}$ in silicon, owing to ionized impurity scattering. When the concentration of ionized impurities is high, the mobility limited by impurity scattering is shown at higher temperatures.

Phonon scattering always involves the mobility behavior and, especially, it dominantly affects the effective mobility at room temperature. When the carrier concentration is not high, Coulomb scattering is important for the determination of the effective mobility while the surface roughness scattering become important with high carrier concentration. Surface roughness scattering strongly affects the mobility behavior when the transistor is in strong inversion regime.

Surface roughness in the MOS structure is related to the random fluctuation of surface, which is represented by atomic step, between oxide insulator and channel silicon. The fluctuation creates the dipoles at the interface, inducing electrical potentials. It is expected the surface roughness always exists at the interface between insulator and channel due to the misfit of the lattice spacing and the existence of interfacial stress due to the difference in thermal expansion coefficient.

4 THE EFFECT OF TEMPERATURE ON ELECTRICAL CHARACTERISTICS IN MOSFET

4.1 Variation of threshold voltage with temperature

The threshold voltage in MOSFET is defined as the sum of the flat band voltage, the surface potential of $2\psi_B$, and the voltage drop across the oxide (Fig. 11(a));

$$V_{th} = V_{fb} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_{ox}} \qquad (1.14)$$

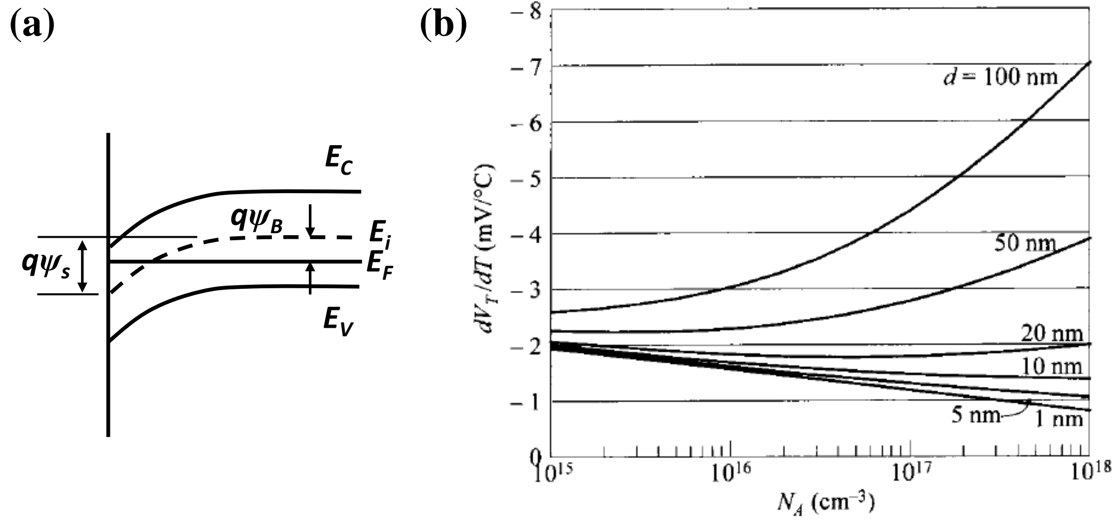

Figure 11 (a) Energy-band diagram and (b) the derivative of the threshold voltage with temperature as a function of the oxide thickness d with various doping concentration [3].

$$= \phi_{ms} - \frac{Q_f}{C_{ox}} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B)}}{C_{ox}}$$

where V_{fb} is the flat-band voltage, ψ_B the Fermi potential, ε_s is the dielectric permittivity of the semiconductor, N_A is the substrate doping level (/m^3), C_{ox} is the gate oxide capacitance (F/m^2), Q_f is the fixed oxide charges (C/m^2), and ϕ_{ms} is the work function difference between the gate material and the semiconductor. Because ϕ_{ms}, Q_f and C_{ox} are independent of temperature, the derivative of threshold voltage with temperature is given as;

$$\frac{dV_{th}}{dT} = \frac{d\psi_B}{dT}\left(2 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_s q N_A}{\psi_B}}\right) \qquad (1.15)$$

And ψ_B is given as;

$$\psi_B = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \qquad (1.16)$$

Since, $n_i (= \sqrt{N_C N_V}\exp(-E_g / 2kT))$ is also is a function of temperature.

$$\frac{d\psi_B}{dT} \approx \frac{1}{T}\left(\psi_B - \frac{E_{g0}}{2q}\right) \qquad (1.17)$$

Adopting above equation to the equation of derivative of threshold voltage,

$$\frac{dV_{th}}{dT} \approx \left(\frac{1}{T}\left(\psi_B - \frac{E_{g0}}{2q}\right)\right)\left(2 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_s q N_A}{\psi_B}}\right) \qquad (1.18)$$

The derivation of threshold voltage with temperature change is shown with various doping concentration as a function of the oxide thickness d (Fig. 11(b)). It is worthwhile to note that the derivation of threshold voltage is influenced by oxide thickness as well as doping concentration in MOSFET.

4.2 Variation of subthreshold slope with temperature

The subthreshold swing of MOSFET, SS shows the explicit temperature dependence as shown in Fig. 12. The subthreshold slop is expressed by

$$SS = (\ln 10)\left(\frac{kT}{q}\right)\left(\frac{C_{ox} + C_D}{C_{ox}}\right) \qquad \text{[V/decade]} \qquad (1.19)$$

where C_D is the depletion-layer capacitance.

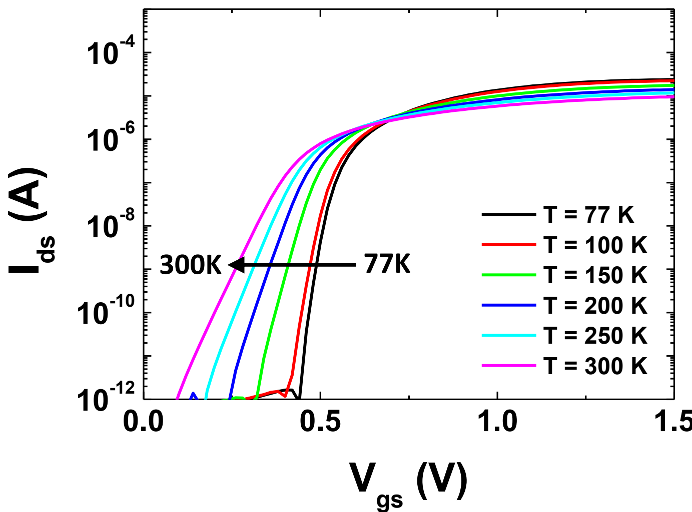

Figure 12 Subthreshold characteristics with various temperature for FD-SOI MOSFET of L = 10 μm and W = 10μm.

4.3 Variation of carrier concentration with temperature

Figure 13 shows the temperature dependence of the carrier concentration. When the temperature is very low (large 1/T), most dopants are frozen out and can't donate electron or holes to conduction band or valence band. As temperature increases, dopants are fully ionized and carrier concentration in the medium temperature range is remained constant, determined by carriers which are provided by

dopants. Beyond this temperature range, the intrinsic carrier concentration become dominant in the determination of carrier concentration, thus it is increased with temperature [13].

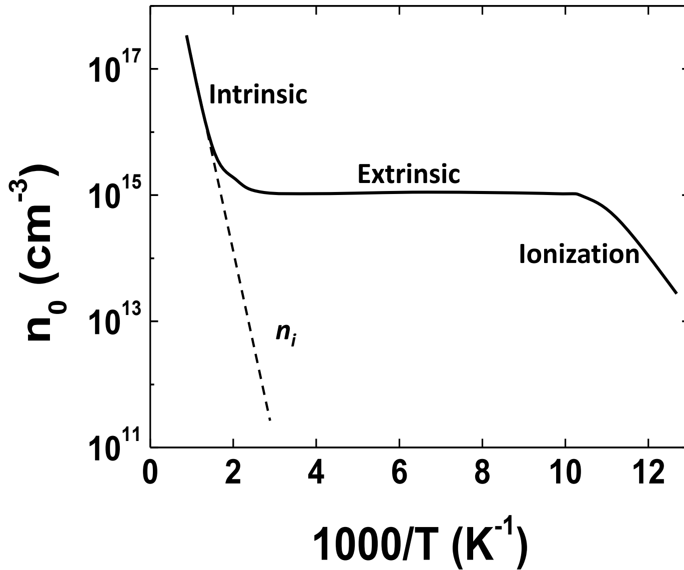

Figure 13 Temperature dependence of the carrier concentration

5 THE SERIES RESISTANCE AND THE VARIATION OF CHANNEL LENGTH IN MOSFET

The series resistance is the sum of the source resistance and the drain resistance, including the contact resistance in source/drain R_{co}, the sheet resistance of source/drain R_{sh}, the spreading resistance between source/drain and channel R_{sp} and accumulation-layer resistance R_{ac} [3, 18].

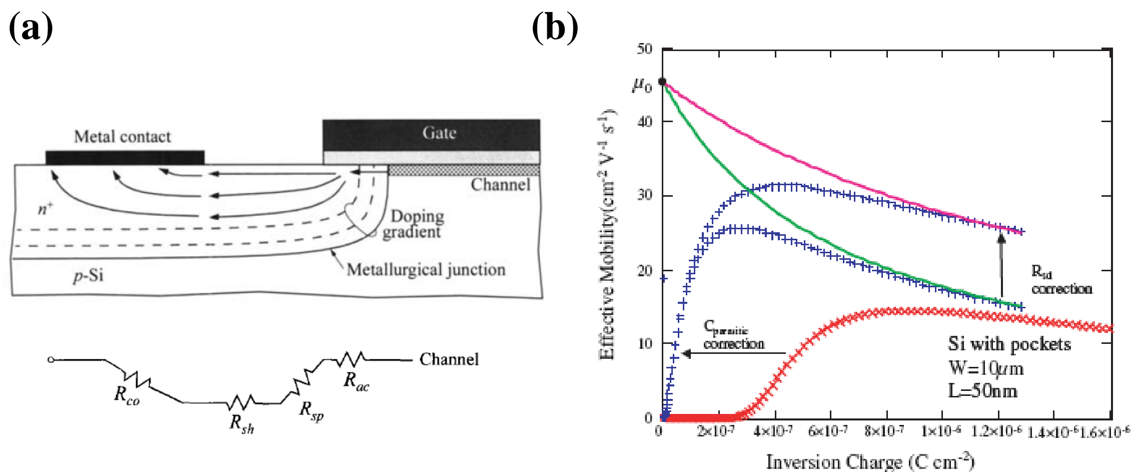

Figure 14 (a) Series resistance in MOSFET [3], (b) the correction of the effective mobility with the series resistance correction [19]

The effect of series resistance on electrical property of MOSFET is important in the performance of device. At first, the series resistance causes the reduced drain current due to the voltage drop in series resistance. It leads to the degradation of the speed of the device. The effective mobility is also degraded by the series resistance and it can be corrected by the extraction of the series resistance as shown in Fig. 14 [19].

The channel length might deviate from mask-defined channel length owing to the imperfection of the fabrication process, such as over-or underexposed photoresist/polysilicon/metal. Besides, the channel length can be different from the distance between the ends of source and drain electrodes since source/drain junctions are spread during high temperature annealing process and the channel length is extended to the LDD region with high gate voltage [12, 13].

In amorphous oxide semiconductor transistors, the increase of channel length is often observed (Fig. 15). Some portion of carriers in AOS TFT is collected/injected at some distance apart from the edge of source/drain electrodes because an insulating layer is formed at electrode edge during the fabrication process [20, 21].

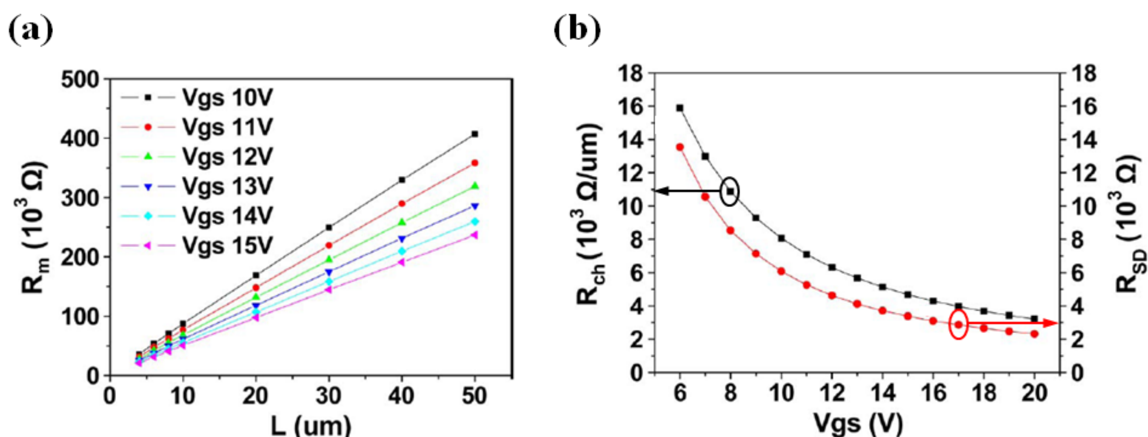

Figure 15 (a) Total resistance R_m as a function of channel length L for TFTs (W = 50 μm, L = 4, 6, 8, 10, 20, 30, 40, 50 μm). (b) Channel resistance R_{ch} and series resistance R_{SD} at source/drain contacts with various gate voltage Vgs. [20]

6 THE SUBSTRATE BIAS EFFECT ON ELECTRICAL CHARACTERISTICS IN MOSFET

In FD-SOI MOSFET, the substrate biasing effects on transport properties and gate tunnelling currents have received a lot of interest since it has a possibility to change the carrier concentration distribution and electric field distribution in the silicon film. In addition, the bias applied to the substrate

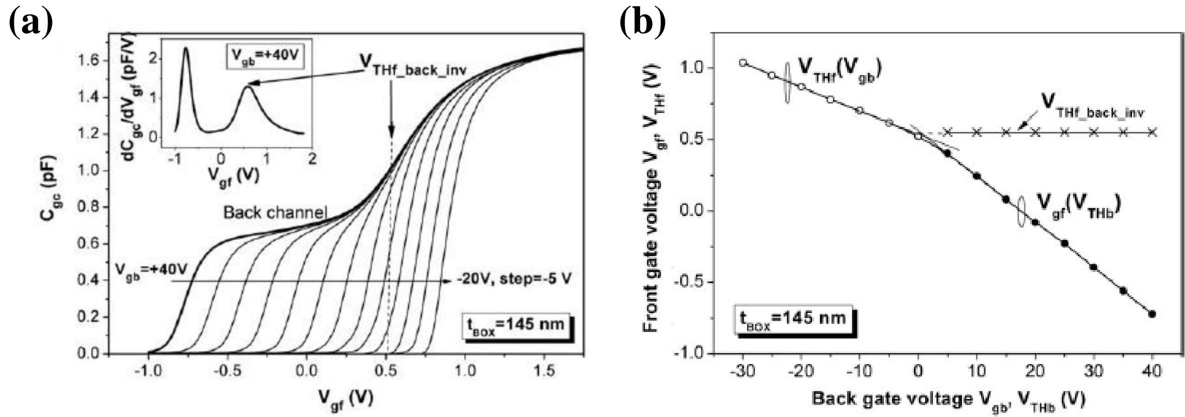

Figure 16 (a) Gate-to-channel capacitance C_{gc} as a function of the front-gate voltage V_{gf} at different back-bias voltages V_{gb} from 40 V to -20 V with step -5 V, (b) front-channel threshold voltage and back-channel threshold voltage versus back gate bias [22]

modulates the intrinsic gate-to-channel capacitance and the front gate threshold voltage due to the interface coupling as shown in Fig. 16 [22]. Ritzenthaler et al., also reported that the short channel effect such as DIBL could be variable with substrate bias [23]. The substrate biasing effect which is presented as the polarization of the substrate is important in the operation of the transistor and it should be concerned in the practical use of SOI devices.

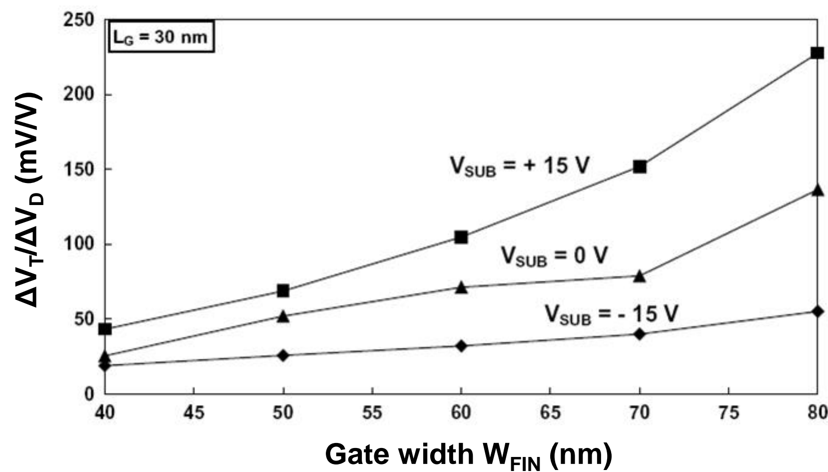

Figure 17 Threshold voltage lowering $\Delta V_T/\Delta V_D$ in ΩFET with gate length L_G = 30 nm by DIBL as a function of gate width W_{FIN} for various substrate bias (V_{SUB} = -15, 0, and +15 V) [23].

7 CONDUCTION IN AMORPHOUS OXIDE SEMICONDUCTOR THIN FILM TRANSISTOR (AOS TFT)

Generally, the density of states (DOS) in a-Si:H is adopted for explaining the conduction mechanism of AOS TFT. Different from the silicon, there are states in the band gap of AOS and these states consist of band-tail states and deep-gap states [24]. Similar to a-Si, some portion of carrier is localized in band-tail states and localized carriers in band-tail states decrease at higher gate voltage. Delocalized carriers can contribute to the drain current and increase the effective mobility in AOS TFT [25, 26]
The band-tail states are given as a function of energy E (Fig. 18):

$$g_{CBa} = g_{ta} \exp[(E - E_C)/E_a] \qquad (1.20a)$$

$$g_{VBd} = g_{td} \exp[(E_V - E)/E_d] \qquad (1.20b)$$

Where g_{ta} the densities of acceptor-like tail states at $E = E_C$, and g_{td} the densities of donor-like tail states at $E = E_V$.

AOS TFT shows gate voltage dependent mobility as;

$$\mu_{eff} = K(V_{gs} - V_{th})^{\alpha} \qquad (1.21)$$

where K is the constant which is related to the material and α is the exponent which shows the degree of dependence on the gate voltage [24].

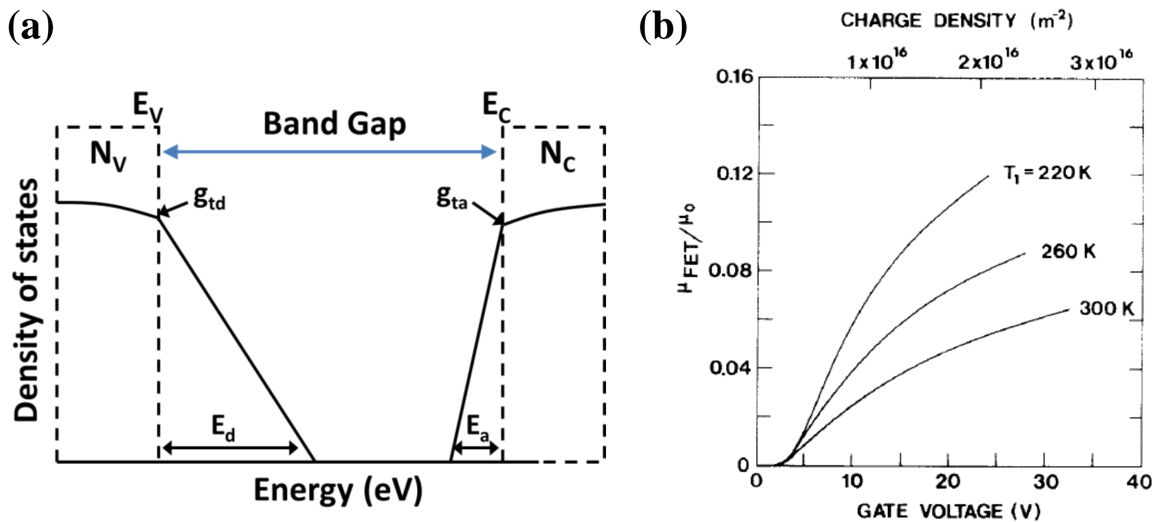

Figure 18 (a) The density of states model of AOS TFT and (b) gate-dependent mobility of AOS TFT, ratio of field-effect to band mobility versus the gate voltage for varying temperature T [26].

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CHAPTER 2

1 MEASUREMENT TECHNIQUE TO AVOID ERRORS
1.1 The limit of voltmeter
1.2 The guarding technique
2 ELECTRICAL CHARACTERIZATION AND ANLYSIS
2.1 Y-function
2.2 The Split C-V measurements
2.3 Defining threshold voltage
2.4 Defining the series resistance and the effective channel length
2.5 Defining the trap density
2.6 2-D numerical simulations

EXPERIMENTAL BACKGROUND

To observe previous theoretical phenomena, experimental precautions and experimental methods are worth to note. In this chapter, the consideration in the measurement tips such as the limit of voltmeter and guarding technique to avoid possible experimental error and the experimental parameter characterization method such as Y-function and C-V measurement technique will be covered. The extraction method of electrical parameters such as threshold voltage, the series resistance and trap density is also discussed. For the analysis of electrical characteristics of the MOSFETs with proper model, 2-dimensional (2-D) numerical simulation is also important tool to investigate the conduction in MOSFET.

1 MEASUREMENT TECHNIQUE TO AVOID ERRORS

1.1 The limit of voltmeter

When DC voltage measurement is performed, the measurement accuracy is limited by the noise voltage which is created by the resistances in circuit and the source resistance. For Digital multimeter (DMM), the measurement of 1 μV with source resistance 1 Ω is possible, however, the measurement of 1μV with source resistance of 1kΩ is not practical since this measurement condition is below the theoretical limit of DMM. In this case, nanovoltmeter (nVM) can be used. The voltmeter can't measure the source resistance which is much larger than its input resistance because it induces input loading errors [1].

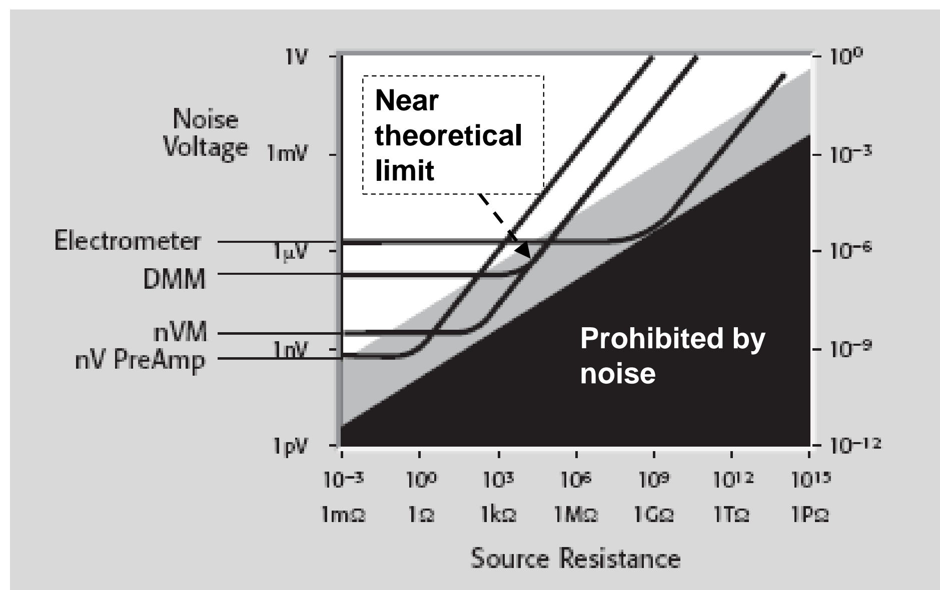

Figure 1 Limit of measurement equipment; Digital Multimeter(DMM), Nanovoltmeter (nVM), Nanovolt Preamplifier (nV PreAmp), and Electrometer [1]

1.2 The guarding technique

With guarded configuration, the cable leakage current can be reduced. As cable shield is connected to the output of guard buffer instead of low terminal of voltmeter, the voltage difference between high terminal voltmeter and cable shield become very small (Fig. 2(a)). Hence, the current flowing through

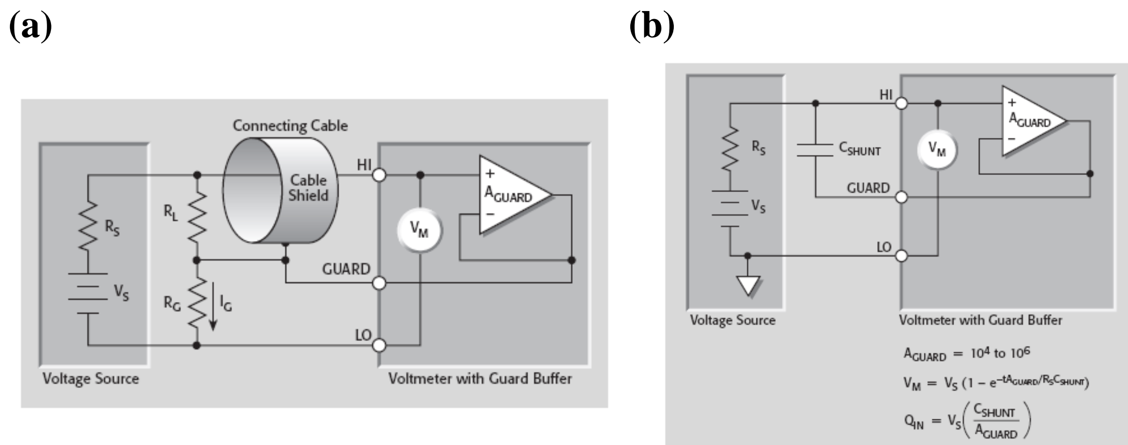

Figure 2 (a) Guarding leakage resistance and (b) Shunt Capacitance [1]

the cable leakage resistance is negligible. Another important advantage of guarding is reducing the effect of shunt capacitance (Fig. 2(b)). As open-loop gain of guard buffer A_{GUARD} is 10^4 to 10^6, the charging time of shunt capacitance is significantly reduced.

When the coaxial cable is used, the leakage current through the cable leakage resistance can be created due to the voltage difference between Force/Output HI terminal and Force/Output LO terminal. The leakage current can be a serious problem in the low current measurement. In contrast, the usage of triaxial cables (Fig. 3) eliminates the leakage current because voltage difference between

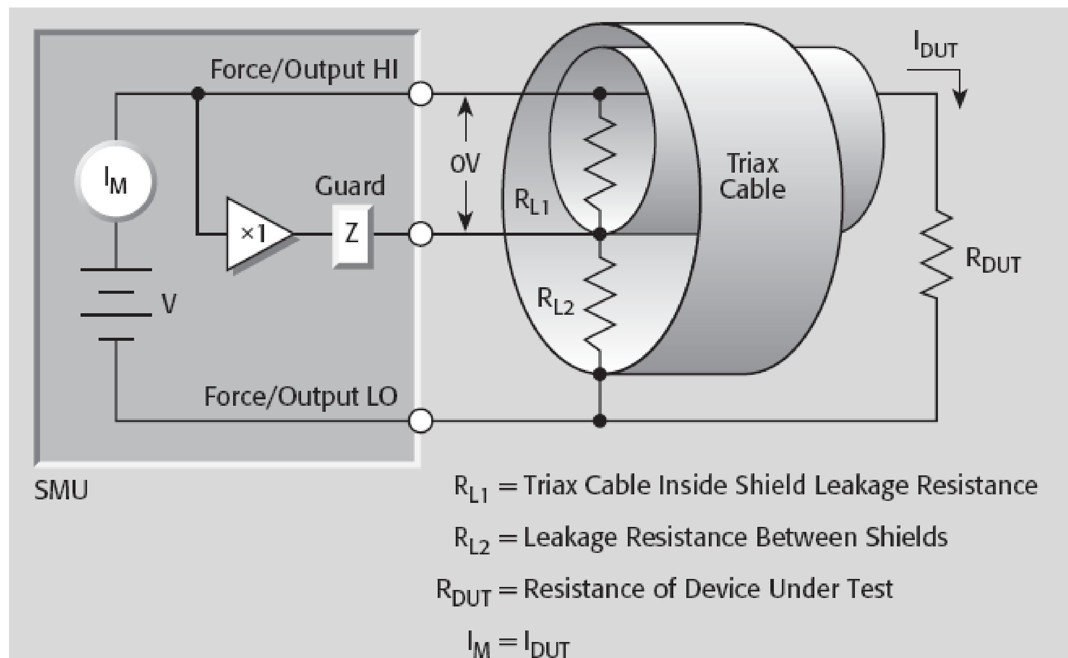

Figure 3 Current measurement with guarding the leakage resistance with the triaxial cable [1]

Force/Output HI and inside shield of the triaxial cable, connected to the guard terminal of SMU, becomes almost zero.

2 ELECTRICAL CHARACTERIZATION AND ANALYSIS

2.1 Y-function

Y function method is developed to avoid the effect of series resistance and mobility degradation on the threshold voltage and the low-field mobility [2]. Y function is defined as;

$$Y = \left(\frac{I_d{}^2}{g_m} \right)^{\frac{1}{n}} \quad [(\mathrm{A\,V})^{1/n}] \qquad (2.1)$$

n is 2 for 200 - 300 K and is 3 for 4.2 - 40 K for silicon MOSFET [3]. The drain current I_d in a strong inversion regime of MOSFET is presented as;

$$I_d = \frac{WC_{ox}}{L} \frac{\mu_0}{[1+\theta(V_g - V_{th})]} (V_g - V_{th}) V_d \qquad (2.2)$$

where θ is the mobility degradation factor.

Then, the transconductance g_m is defined as;

$$g_m = \frac{WC_{ox}}{L} \frac{\mu_0}{[1+\theta(V_g - V_{th})]^2} V_d \qquad (2.3)$$

With applying equations to Y function at room temperature, Y function is again presented as;

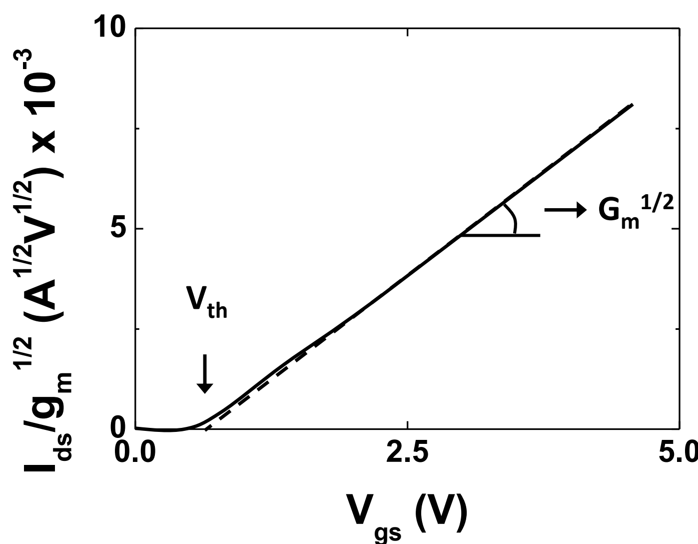

Figure 4 Y function of MOSFET characteristic

$$Y = \left(\frac{W}{L} C_{ox} \mu_0 V_d \right)^{1/2} (V_g - V_{th}) = G_m{}^{1/2} (V_g - V_{th}) \qquad (2.4)$$

where G_m is the transconductance parameter $(= \frac{W}{L} C_{ox} \mu_0 V_d)$.

As shown Eq. (2.4), the effect of the degradation factor is excluded from the Y function and Y function is linear with the gate voltage.

The low field mobility can be extracted from the slope of Y function to the gate voltage and the threshold voltage is obtained from the x-axis intercept as shown in Fig. 4.

The mobility degradation factor θ can be calculated with the extracted threshold voltage value;

$$\theta = \frac{I_d}{[g_m (V_g - V_{th}) - 1]} \frac{1}{(V_g - V_{th})} \qquad (2.5)$$

Using the relation between θ and channel length L, the series resistance R_{sd} also can be extracted by plotting θ versus G_m;

$$\theta = \theta_0 + R_{sd} C_{ox} \mu_0 W / L = \theta_0 + R_{sd} G_m \qquad (2.6)$$

2.2 The split C-V method

As shown in the previous section of effective mobility, capacitance-voltage characteristics are also important for the investigation of MOSFETs. Especially, to measure the gate-to-channel capacitance of MOSFET, split C-V method is useful [4, 5]. For the measurement of gate-to-channel capacitances, high terminal of LCR meter is connected to gate electrode while the source and drain are connected together with low terminal of LCR meter when substrate is grounded (Fig. 5). With measured gate-to-channel capacitance, the inversion charge can be obtained and the effective mobility can be extracted [6]. The effective mobility extracted by split C-V method tends to go to zero in subthreshold regime.

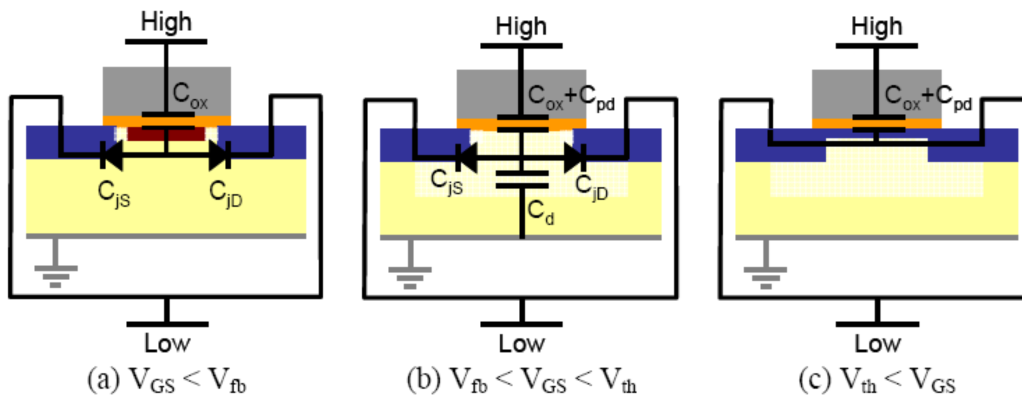

Figure 5 The equivalent circuit of the gate-to-channel capacitance measurement for (a) accumulation, (b) depletion, and (c) inversion regimes [6].

It cannot be applied below threshold as well as the Y function because of inappropriateness.

2.3 Defining the threshold voltage

Besides Y-function which is described previously, there are several methods to define the threshold voltage such as constant current technique, maximum derivative of transconductance, and linear extrapolation of transfer characteristics [7].

At first, constant current method determines the threshold voltage V_{th_cc} at a certain value of the drain current, for example, e.g. $I_{ds} = 1 \times L/W$ (nA).

Secondly, the threshold voltage is determined at the maximum position of transconductance derivative (V_{th_dgm}). The threshold voltage extracted by this method is not affected by series resistance and mobility degradation.

The threshold voltage is also obtained from the extrapolation point of transfer curve to $I_{ds} = 0$ at low drain voltage (V_{th_ex}). The linear line deviates from original transfer curve below the threshold voltage due to the subthreshold current and above the threshold voltage due to series resistance as well as mobility degradation.

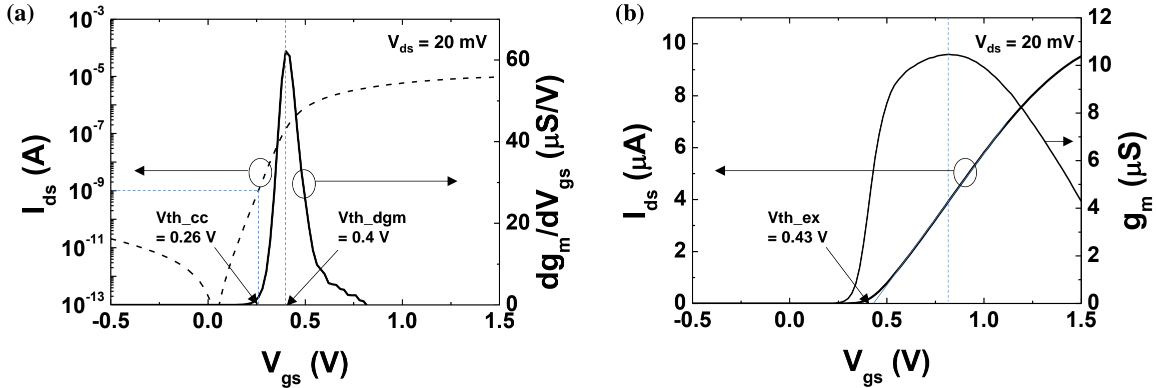

Figure 6 Threshold voltage determined by (a) constant current technique, V_{th_cc}, maximum derivative of transconductance, V_{th_dgm} and (b) linear extrapolation of transfer characteristics, V_{th_ex}.

2.4 Defining the series resistance and the effective channel length

2.4.1 TLM method

The transfer length method is used to extract the series resistance and the effective channel length. Total measured resistance $R_m (=V_{ds} / I_{ds})$ is the sum of channel resistance R_{ch} and the series resistance R_{sd}. The series resistance can be obtained by extrapolation of R_m versus mask channel length L_m in the gate bias range above threshold voltage;

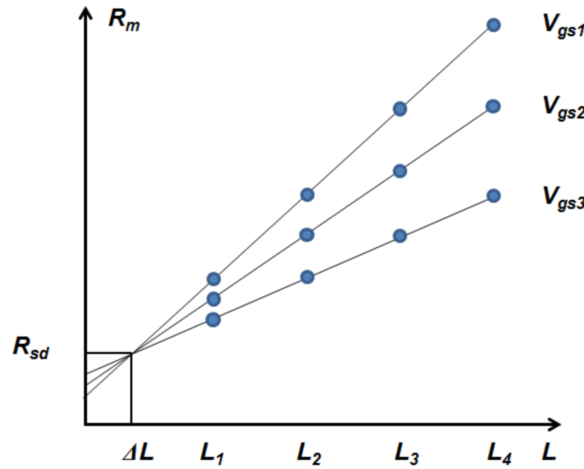

Figure 7 Measured resistance R_m versus mask channel length L (L_1, L_2, L_3, L_4) as a function of different gate bias (V_{gs1}, V_{gs2}, V_{gs3})

$$R_m = R_{ch} + R_{sd} = \frac{L_m - \Delta L}{W_{eff}\,\mu_{eff}\,C_{ox}(V_{gs} - V_{th})} + R_{sd} \quad (2.7)$$

Where ΔL is the discrepancy of channel length.

2.4.2 Four-probe method

The measured resistance R_m of DUT includes the contact resistance R_C when the 2-probe method is used for the measurement [7].

$$R_m = V/I = 2R_W + 2R_C + R_{DUT} \quad (2.8)$$

where R_W is the wire or probe resistance and R_{DUT} is the resistance of the device under test (DUT). However, the intrinsic resistance of DUT can be measured with 4-probe method since the

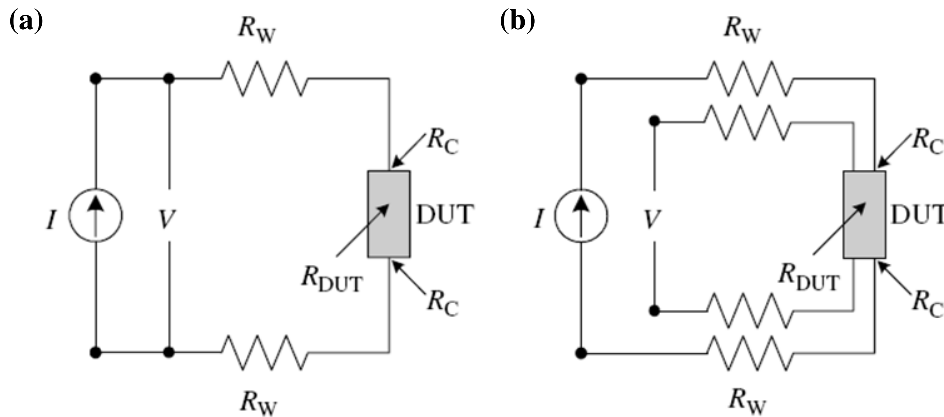

Figure 8 (a) Two-probe measurement and (b) four-probe measurement [7]

current flowing through R_C is very low due to the high input resistance of the voltmeter, thus, the voltage drop by R_C becomes negligibly small.

2.5 Defining the trap density

2.5.1 Trap density from subthreshold swing

With significant interface trap density N_{it}, the equation of subthreshold swing SS is presented as [8];

$$SS = (\ln(10))\left(\frac{kT}{q}\right)\left(\frac{C_{ox} + C_D + C_{it}}{C_{ox}}\right) \quad \text{[V/decade]} \quad (2.9)$$

where C_{it} is the interface trap capacitance and C_D is the depletion-layer capacitance.

The interface trap density can be determined from the subthreshold swing SS when Cox and C_D are known. In the case where C_D is negligible one has;

$$N_{it} = \frac{C_{it}}{q} = \left(\frac{SS}{\ln(10)kT} - 1\right)\frac{C_{ox}}{q} \quad \text{[/cm}^2\text{eV]} \quad (2.10)$$

2.5.2 Trap density from 1/f noise

Low frequency noise characteristic also can be used for the investigation of interface trap density in device. There are two kinds of mechanisms explaining the origin of noise characteristics. One is mobility fluctuation model and the normalized drain current noise depends on $1/I_D$ [9].

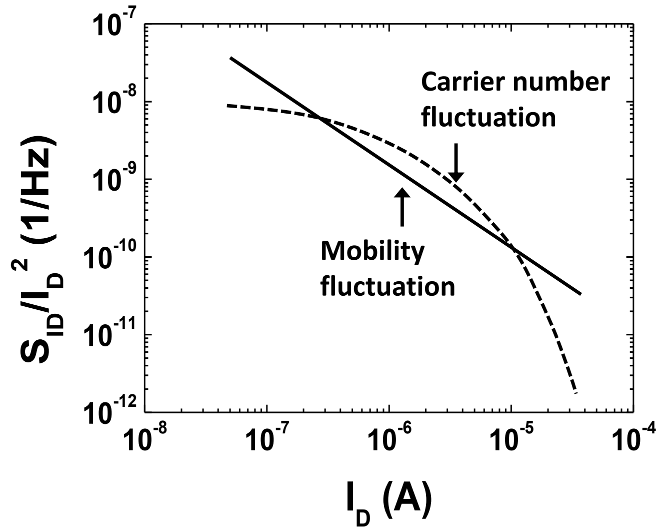

Figure 9 Normalized drain current noise characteristics obey mobility fluctuation and carrier number fluctuation

$$\frac{S_{I_D}}{{I_D}^2} = \frac{q\alpha_H}{WLQ_i f} = \frac{q\alpha_H \mu_{eff} V_{DS}}{L^2 f I_D} \quad \text{[1/Hz]} \quad (2.11)$$

where α_H is the Hooge parameter, Q_i is the inversion charge (C/cm^2), and f is the frequency. In contrast, the normalized drain current noise following only the carrier number fluctuation model with correlated mobility fluctuation depends on $(g_m / I_D)^2$ as [10].

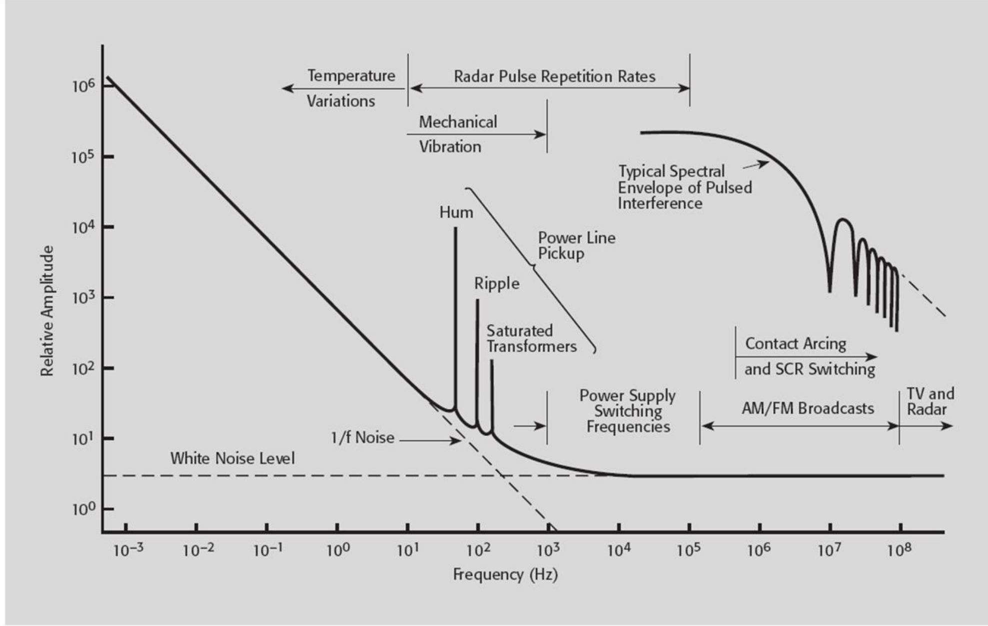

Figure 10 The voltage noise frequency spectrum [1]

$$\frac{S_{I_D}}{{I_D}^2} = S_{V_{FB}} \left(1 + \frac{\alpha \mu_{eff} C_{ox} I_D}{g_m}\right)^2 \frac{{g_m}^2}{{I_D}^2} \quad (2.12a)$$

$$S_{V_{FB}} = \frac{q^2 kT\lambda N_{it}}{fWL{C_{ox}}^2} \quad (2.12b)$$

where N_t is the slow trap volume density (cm^{-3}eV^{-1}), α is the Coulomb scattering coefficient (Vs/C), λ is the tunneling attenuation length in gate oxide, which is about 1 Å for Si/SiO_2 interface. When the carrier number fluctuation model acts a major role in noise property, the trap density can be characterized from noise characteristics depending on the frequency and bias.

$$N_{it} = \frac{fWL{C_{ox}}^2 S_{V_G}}{q^2 kT\lambda(1 + \alpha\mu_{eff} C_{ox} I_D / g_m)^2} \quad (2.13)$$

where, $S_{V_G} = S_{I_D} / {g_m}^2$ is the equivalent input gate voltage noise.

In noise measurements, various sources of voltage noise should be concerned for the accuracy of the measurements. Figure 10 shows the possible sources of voltage noise depending on the frequency [1].

2.6 2-D numerical simulations

With numerical simulation, we can calculate the solution of mathematical models on a computer and simulate the physical phenomena [11]. The mathematical model is established by partial differential equations with several variables such as voltage, and time. For the numerical simulation, the solution is not exactly calculated but is approximated at given points. The given point is the node which is the cross point of grid lines. Generating grid lines should be fine enough to obtain the property of interest while generating too fine grid significantly increase the simulation time. After having a solution in initial conditions, the grid density adjusted again, for example, the region is zoomed in where the property changes rapidly to resolve the change.

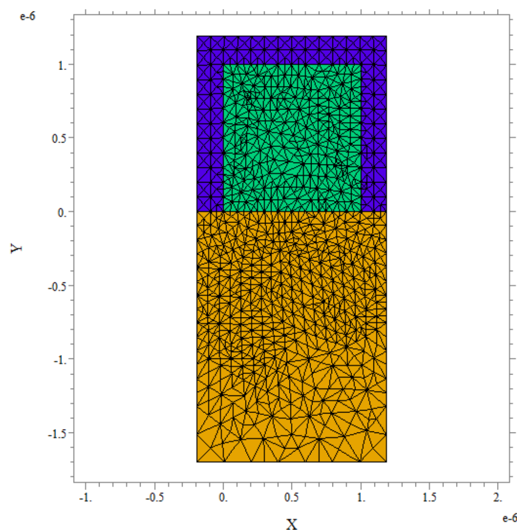

Figure 11 Generation of grid in 2-D numerical simulation of Tri-gate device with Flex-PDE program.

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CHAPTER 3

1 INTRODUCTION
2 EXPERIMENTAL DETAILS
3 RESULTS AND DISCUSSIONS
3.1 Sidewall mobility in multi-channel tri-gate MOSFET
3.2 Series Resistance in multi-channel tri-gate MOSFET
4 CONCLUSIONS

SIDEWALL MOBILITY AND SERIES RESISTANCE IN MULTI-CHANNEL TRI-GATE MOSFET

The sidewall mobility and the series resistance in multi-channel tri-gate MOSFET were investigated with low temperature measurement and 2-D numerical simulation. With sidewall mobility separated from total transfer characteristics, it was shown that the sidewall conduction is mainly affected by the surface roughness scattering. The effect of surface roughness scattering in sidewall mobility was evaluated with the mobility degradation factor normalized by the low field mobility, which exhibited almost 6 times higher value than that of top surface mobility. The series resistance of multi-channel tri-gate MOSFET was studied by comparing with that of planar MOSFET. Through 2-D numerical simulation, it was revealed that relatively high series resistance of multi-channel tri-gate MOSFET is attributed to the variation of doping concentration in the source/drain extension region in the device.

1 INTRODUCTION

According to the ITRS roadmap, the minimum feature size of MOSFET in 2015 is predicted as 10 nm [1]. As the size of device is shrunk extensively, more efforts were done to keep the performance of devices against short channel effects, dopant-induced fluctuation in threshold voltage, etc [2-4]. The multiple-gate MOSFETs, showing better immunity to scaling concerns, such as FinFET, Double-Gate-FET and multiple-gate planar MOSFET have been focused as candidates for the next CMOS device generation [5-7]. Among these devices, multi-channel tri-gate MOSFET is attractive structure to obtain not only tight gate control but also stable and high current level [8, 9] However, some optimization are still required in multiple-gate MOSFET such as complicate fabrication process in FinFET, the degradation of the performance related to the variation of geometrical parameters [10], series resistance variation with the channel width [11]. It was reported that the effect of surface roughness on sidewall, resulting from the etching process for the formation of fin structure in FinFET, is an important issue for the device performance [12]. Although tri-gate transistor has similar geometry with FinFET, the effect of surface roughness in tri-gate MOSFET is not properly evaluated yet. It is worthwhile to compare the effect of surface roughness on FinFET and tri-gate MOSFET. In addition, the physical interpretation of sidewall mobility behavior, such as scattering mechanism, complements previous reports showing temperature dependence in performance of tri-gate MOSFET [13].

In this chapter, the effect of surface roughness on the sidewall mobility of multi-channel tri-gate MOSFET was analyzed with varying temperatures ranging from 77 K to 350 K. The effect of surface roughness was quantified using the second order mobility degradation factor. Series resistance characteristics in multi-channel tri-gate MOSFET were also investigated by comparing with those in planar MOSFETs. In addition, the origin of series resistance was studied with 2-D numerical simulation.

2 EXPERIMETAL DETAILS

The sidewall mobility behavior was investigated with multi-channel MOSFETs. N-type inversion mode MOSFETs were fabricated at CEA-LETI and provided by Sylvain Barraud. Details of fabrication process are described elsewhere [14]. As shown in Fig. 1(a) and (b), multi-channel device used in this paper has tri-gate MOSFET structure on (100) SOI wafer with a 145 nm-thick BOX oxide. 50 identical channel structures were established as a form of 50 fingers from 10 nm-thick undoped channel silicon layer (Fig. 2). The channel of transistor is patterned by optical (deep ultra violet) lithography and resist trimming. The gate stack is composed of HfSiON/ TiN/ Polysilicon with equivalent oxide thickness of 1.2 nm. The mask channel length L_M was fixed as 10 μm and the mask channel width W_M was varied from 100 nm to 1 μm. The wide planar devices ($L_M = W_M = 10$ μm) were used

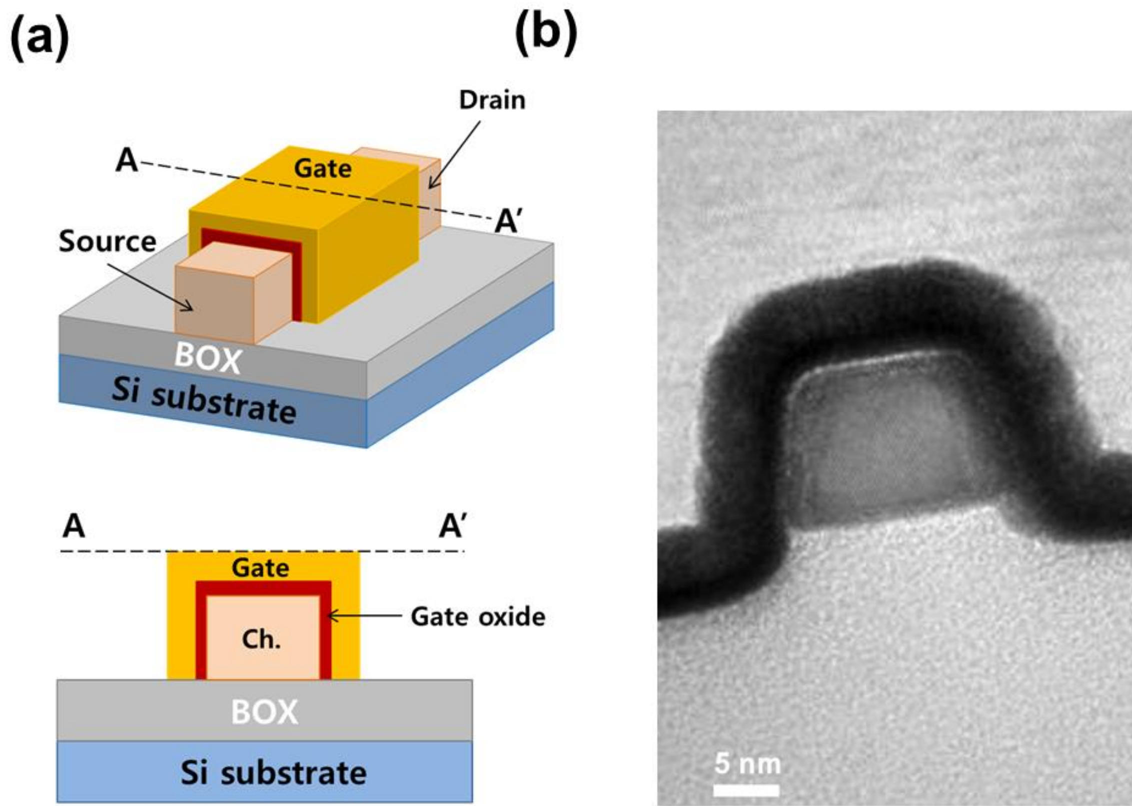

Figure 1 (a) Schematic of the tri-gate MOSFET structure and the corresponding cross-section of the device along the line A-A´(b) cross-section TEM image

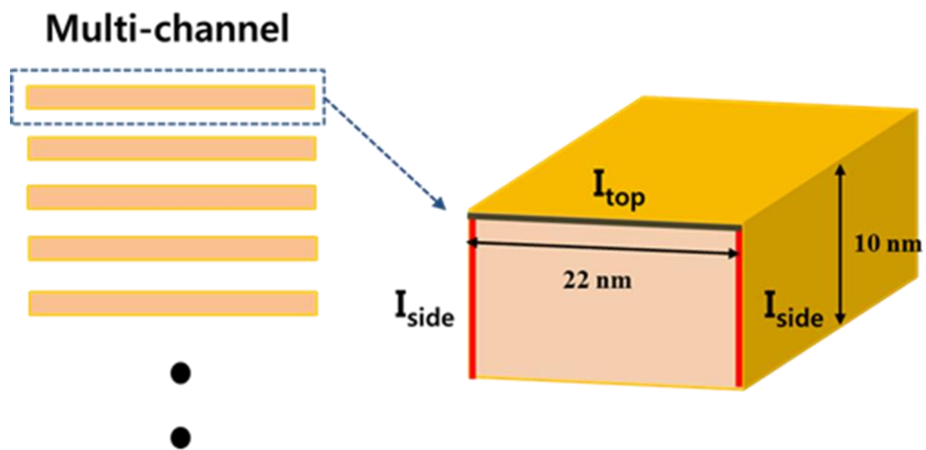

Figure 2 Illustration of multi-channel and one singel channel

to compare their series resistances with those of the multi-channel device. Multi-channel devices used for the series resistance extraction have 50 channels with W_M = 250 nm and L_M = 10 μm. 2-D numerical transport simulation was carried out with Flex PDE 5.0 software based on the finite element method to simulate the series resistance. The effective channel width discrepancy (ΔW) of around 58 nm was obtained using transfer length method (TLM) with the measurement of gate-to-channel capacitance of devices with different channel width [15].

Transfer characteristics of MOSFETs were measured at V_{DS} = 20 mV with Agilent 4155A measurement unit. Low temperature transfer characteristics were measured in the temperature ranging from 77 K to 350 K using SussMicroTec LT probe station. The gate-to-channel capacitance was recorded using a precision HP4294A with the split capacitance–voltage (C-V) method.

3 RESULTS AND DISCUSSION

3.1 Sidewall mobility in multi-channel tri-gate MOSFET

The n-channel drain current of the tri-gate MOSFET with 50 channels was measured at room temperature as a function of effective channel width (W_{eff} = W_M – ΔW) in order to study the effect of sidewall on total conduction. Multi-channel structure device was used for the better accuracy and easier capacitance measurements. Then, the drain current and the gate-to-channel capacitance were

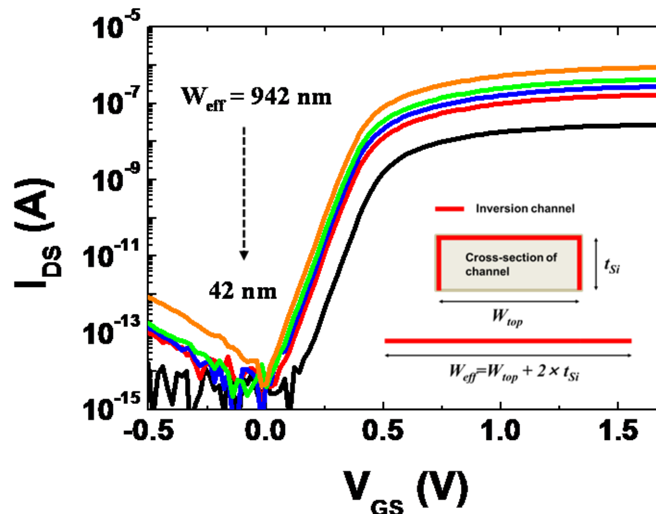

Figure 3 Transfer curves at V_{DS} = 20 mV for tri-gate MOSFET with different channel widths (W_{eff} = 42, 192, 292, 442, 942 nm) and fixed channel length (L_M = 10 μm). The drain current was divided by 50 from the transfer curve of multi-channel MOSFET. Inset illustrates the definition of W_{eff} and W_{top}.

divided by 50 from the measured data of multi-channel device for normalization purpose. As shown in Fig. 3, for a narrower channel, smaller currents are observed in tri-gate MOSFET. Different from wide channel MOSFET, nanowire-like narrow MOSFET possesses transfer characteristics which are more sensitive to sidewall conduction since it features a larger portion of sidewall area to total channel area.

Sidewall currents were separated from transfer characteristics of tri-gate MOSFETs with different channel width. As shown in Fig. 4 and Fig. 5(a), sidewall current was obtained from extrapolated drain current values when the top width, W_{top} becomes zero with different gate bias at strong inversion region. The gate bias voltage was replaced by gate overdrive voltage V_{GT} ($V_{GT} = V_{GS} - V_{th}$) for extraction of sidewall electrical characteristics in order to compensate the difference of threshold voltages V_{th} in devices of different width. V_{th} was determined from the peak position of the transconductance derivative with gate voltage. The assumption of the surface conduction along the surface of the device is valid only for the gate bias region over threshold voltage [8]. For the mobility calculation, $C_{GC\ side}$ is also obtained with same extrapolation method from gate-to-channel capacitance (Fig. 5(b)). In Fig. 5(c), total effective mobility was obtained from the transfer characteristics and the gate-to-capacitance

$$\mu_{eff} = \frac{I_{DS} L_{eff}}{W_{eff} Q_i V_{DS}} \qquad (3.1)$$

$$Q_i(V_{GT}) = \int_0^{V_{GT}} \frac{C_{GC}(V_{GT})}{W_{eff} L_{eff}} dV_{GT} \qquad (3.2)$$

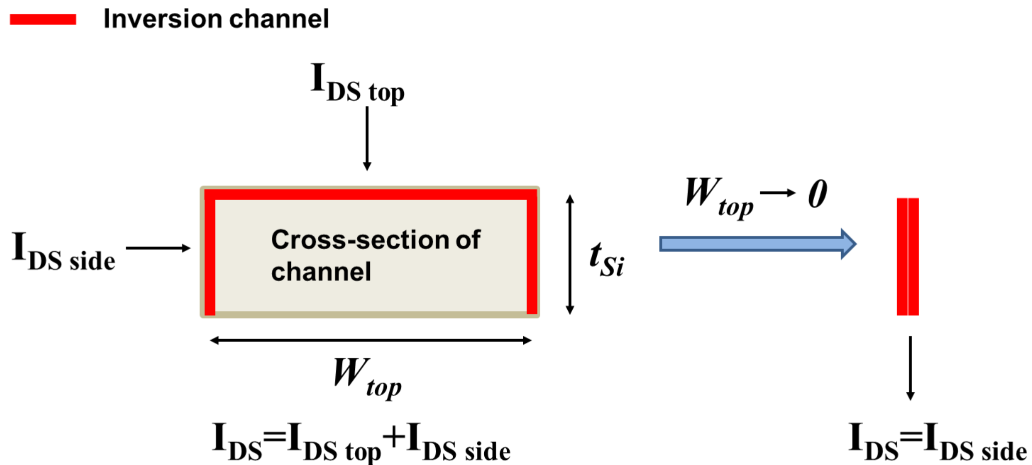

Figure 4 Illustration explaining the extraction of sidewall current

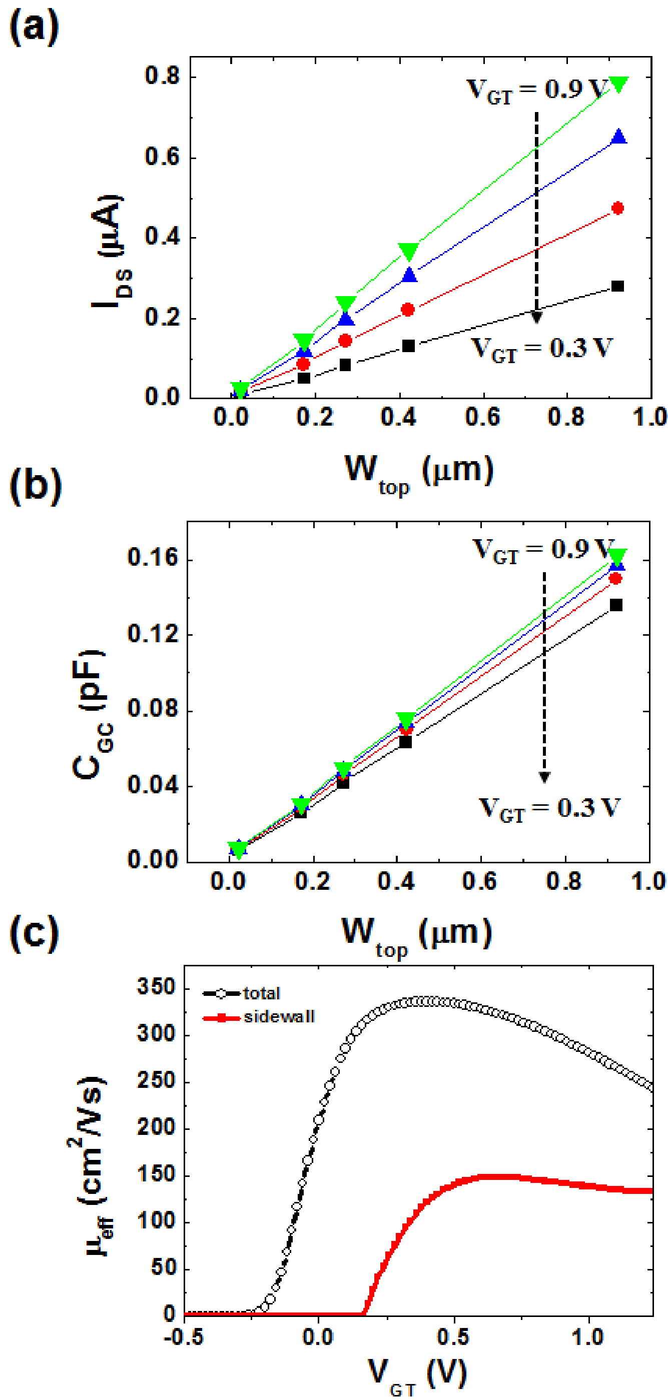

Figure 5 (a) Sidewall current is obtained from extrapolated drain current values I_{DS} and (b) sidewall capacitance is obtained from extrapolated gate-to-channel capacitance C_{GC} when the top width, W_{top} becomes zero with different gate overdrive voltage V_{GT} ($V_{GS} - V_{th}$). (c) Effective mobility in total and the sidewall. The sidewall effective mobility shows more degraded values (≈ 60 %) compared to the total effective mobility.

where L_{eff} is an effective channel length, W_{eff} is an effective channel width, Q_i is the inversion charge per unit area and C_{GC} is the gate-to-channel capacitance. Sidewall effective mobility could be obtained by substituting $2 \cdot t_{Si}$ and $C_{GC\ side}$ for W_{eff} and C_{GC}, respectively, in Eq. (3.1) and Eq. (3.2).

As shown in Fig. 5(c), both the total effective mobility and the sidewall effective mobility are decreased under high gate overdrive voltage condition. And the sidewall effective mobility shows lower values (≈ 40 %) compared to the total effective mobility.

For further analysis, drain current was measured at various temperatures from 77 K to 350 K (Fig. 6) and sidewall current was separated. The drain current at low temperature is increased because the phonon scattering is reduced with temperature lowering. Transconductance (g_m) shown in inset of Fig. 6 indicates that the mobility degradation at high vertical field is more severe at low temperature as compared to room temperature. As the temperature is decreased, surface roughness scattering is predominant in the transfer characteristics since phonon scattering contribution is diminished.

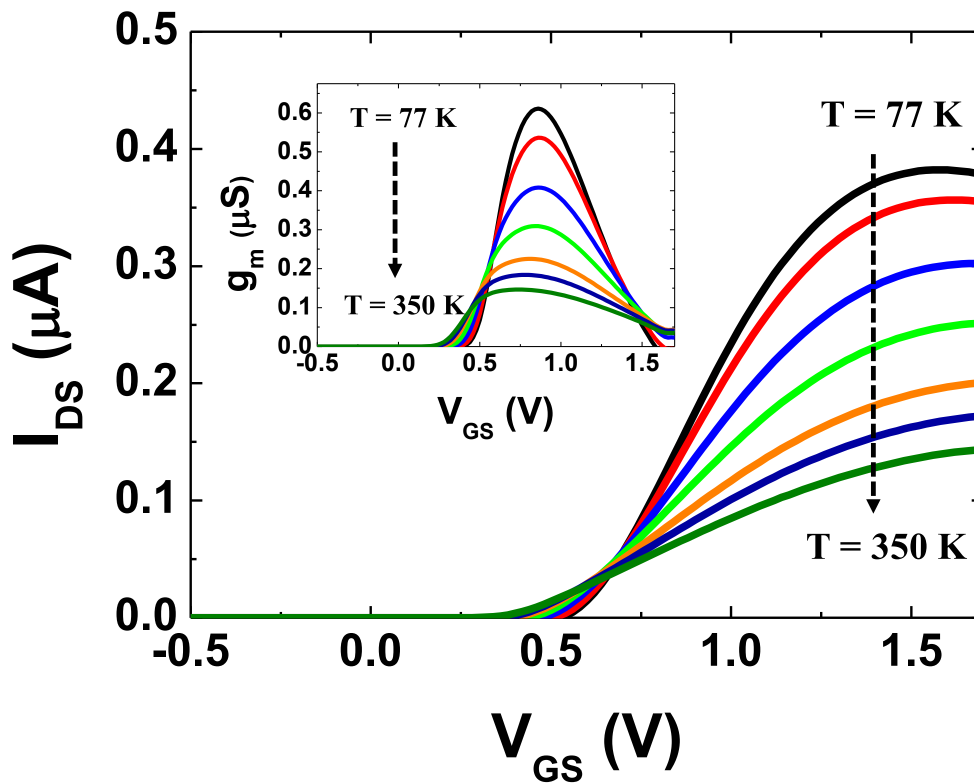

Figure 6 Drain current with various temperatures from 77 K to 350 K. The drain current at low temperature is increased due to diminished phonon scattering. Inset: the corresponding transconductance versus gate voltage.

From the low temperature measurement data, the sidewall mobility and the top mobility were extracted separately. The sidewall mobility was obtained from transfer curves of different devices with varied channel width, like previous extraction procedure at room temperature. The transfer characteristic of the device with W_M = 1 μm was used for the extraction of the top mobility. It was confirmed that the top mobility in the device of W_M = 100 nm has almost same behavior with that in the device of W_M = 1 μm, showing temperature dependence on mobility at any carrier density. The top surface cur-

rent was derived from the subtraction of the sidewall current from the total current, i.e. $I_{DS\ top} = I_{DS} - I_{DS\ side}$. As shown in Fig. 7(a) and (b), the sidewall mobility at low temperature is dramatically decreased with the increase of inversion carrier concentration while the top mobility is slightly decreased in same condition.

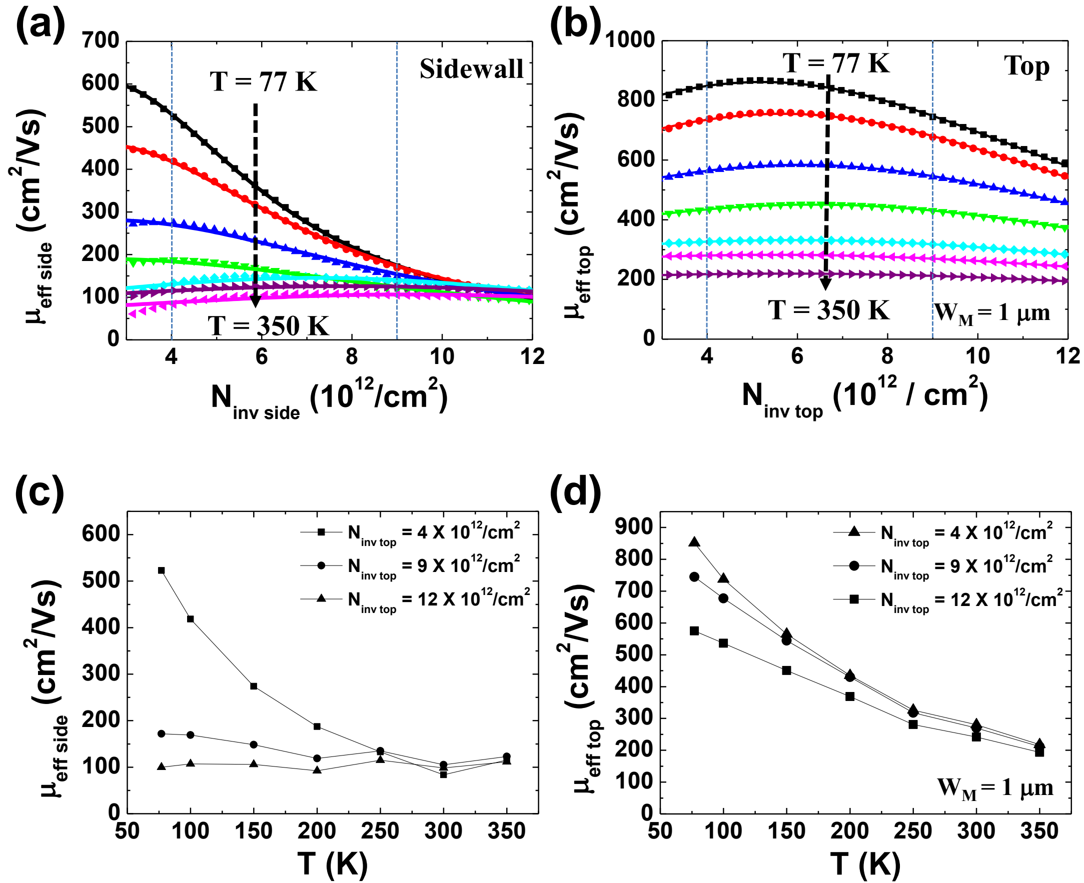

Figure 7 Effective mobility versus the inversion carrier concentration with different temperatures in (a) sidewall and (b) top surface. The solid lines are the best fit with the equation of effective mobility. Sidewall mobility is rapidly decreased with the inversion carrier concentration. These behaviors were checked once more with effective mobility versus temperature extracted at different inversion carrier concentrations in (c) sidewall and (d) top surface.

In addition, the sidewall mobility shows temperature independence when the inversion carrier concentration is high, whereas the top mobility depends on temperature in the whole inversion carrier concentration range. It is noted that the sidewall mobility is seriously affected by surface roughness scattering mechanism compared to the top mobility in tri-gate MOSFET [16]. The mobility behavior of tri-gate MOSFET could be identified more clearly in Fig. 7(c) and (d). In Fig. 7(c) and (d), the sidewall mobility and the top mobility were plotted as a function of temperature with various inversion carrier concentrations. The sidewall mobility has a monotonic behavior with high inversion carrier

concentration, indicating that surface roughness scattering plays an important role in the sidewall mobility, while the top mobility shows temperature dependence regardless of the inversion carrier concentration. It was also checked that the series resistance effect can't reproduce the temperature independent mobility behavior of sidewall mobility in high inversion carrier concentration while it makes the mobility degraded (Fig. 8).

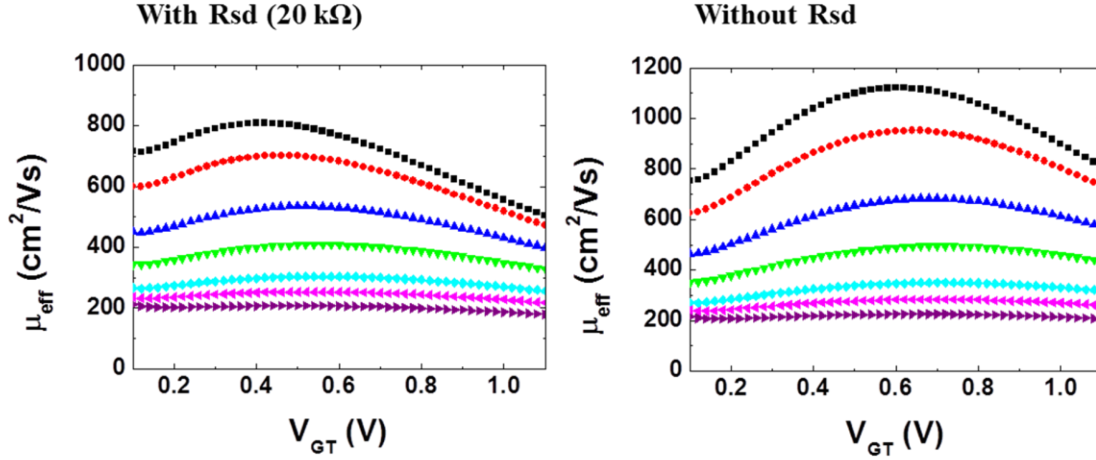

Figure 8 Effective top mobility with and without the series resistance R_{sd} (20 kΩ).

To evaluate the effect of surface roughness scattering in the mobility, mobility degradation factors were extracted using the equation of the effective mobility [17];

$$\mu_{eff}(V_{GT}) = \frac{\mu_0}{1+\theta_1 V_{GT} + \theta_2 V_{GT}{}^2} \qquad (3.3)$$

where μ_0 is the low field mobility, θ_1 and θ_2 are the mobility degradation parameters. Phonon scattering due to the enhanced confinement is represented by θ_1 and the scattering by surface roughness at high transverse field is represented by θ_2 [18]. Sidewall mobility and top mobility were fitted using the above equation and the effective mobility parameters μ_0, θ_1 and θ_2 were extracted.

In Fig. 9(a), the value of θ_1 of sidewall mobility was extracted as –2.3 V^{-1} and –0.81 V^{-1} at T = 77 K and 350 K, respectively, which is comparable to the result of FinFET [12] and negative θ_1 indicates

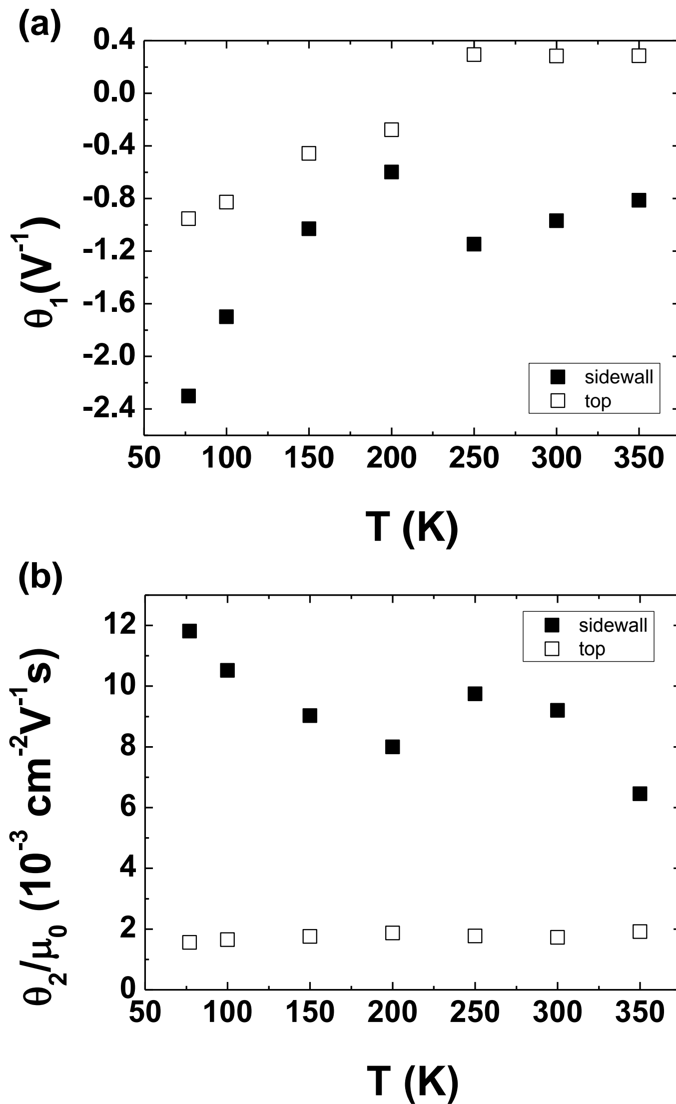

Figure 9 (a) Extracted mobility degradation factor, θ_1 and (b) modified mobility degradation factor, θ_2 normalized by low field mobility (μ_0) from sidewall and top surface

that conduction is seriously affected by Coulomb scattering [19]. Therefore, θ_1 in Fig. 9(a) indicates strong Coulomb scattering contribution is associated with both sidewall mobility and top mobility, although, it seems that sidewall mobility includes more significant Coulomb scattering effect on the whole temperature range. On the other hand, θ_2 of sidewall mobility varies from 5.43 V^{-1} to 0.58 V^{-1} when temperature decreases from 77 K to 350 K. However, low field mobility depends on the temperature and θ_2 depends on phonon limited term as well as surface roughness scattering [12, 20]. Hence, modified mobility degradation factor, θ_2 normalized by low field mobility (μ_0), is proper parameter to reflect surface roughness scattering mechanism to global effective mobility, excluding the effect of the phonon limited term from θ_2 . As shown in Fig. 9(b), the effect of surface roughness scattering could be evaluated appropriately with the normalized mobility degradation factor, θ_2 / μ_0 .

θ_2 / μ_0 from sidewall mobility is more than 5 times higher than that of top surface mobility and it is about 1.25 times higher compared to the previous reports on FinFET [12]. It could be originated from the creation of rough surface in sidewall through the pattering process while the top surface is protected during the etching process [21, 22]. Although it is hard to clearly separate the sidewall current in tri-gate MOSFET owing to the smaller height of active channel, it is shown that the sidewall mobility degradation could be more serious in tri-gate MOSFET than in FinFET.

3.2 Series Resistance in multi-channel tri-gate MOSFET

With the sidewall conduction, the comparison of the series resistance between planar device and multi-channel tri-gate device was investigated. For the comparison, the transfer characteristics were measured at 77 K on planar MOSFET and multi-channel MOSFET. The channel configuration of planar device and multi-channel device is shown in Fig. 10(a). The total surface area of channel region has the difference below 5 % between planar device (total W_{eff} = 9.942 μm) and multi-channel device (total W_{eff} = 9.6 μm) concerning W_{eff}. However, transfer characteristics in Fig. 10(b) show huge difference in drain current between planar device and multi-channel device. In Fig. 10(c), the modified Y-function is obtained as [23, 24]:

$$Y(V_{GS}) = \left(\frac{I_{DS}^{2}}{g_m} \right)^{\frac{1}{n}} \qquad (3.4)$$

n varied with temperature is 2 for 200 - 300 K and is 3 for 4.2 - 40 K. For T = 77 K, n of 2.7 is used for linear shape of Y-function. Y-function shows nonlinearity at high gate bias since the second order mobility degradation factor, θ_2 is not negligible under huge gate bias condition. Interestingly, the electrical geometry in these two devices doesn't have difference since Y-functions of both devices are perfectly matched (Fig. 10(c)). It is known that the effect of series resistance could be excluded from the transfer characteristics with Y-function. Hence, the decrease of drain current in multi-channel device shown in Fig. 10(b) arises from the difference of series resistance.

In order to verify the behavior of series resistance, the total resistance of planar device and multi-channel device were obtained from transfer characteristics with different temperature. The difference of total resistance in two devices (ΔR_{total}) approaches the difference of series resistance (ΔR_{SD}) under high gate bias because the channel resistance can be neglected compared to the series resistance in strong inversion region (Fig. 11(a)):

$$\Delta R_{total} \approx \Delta R_{SD} \qquad (3.5)$$

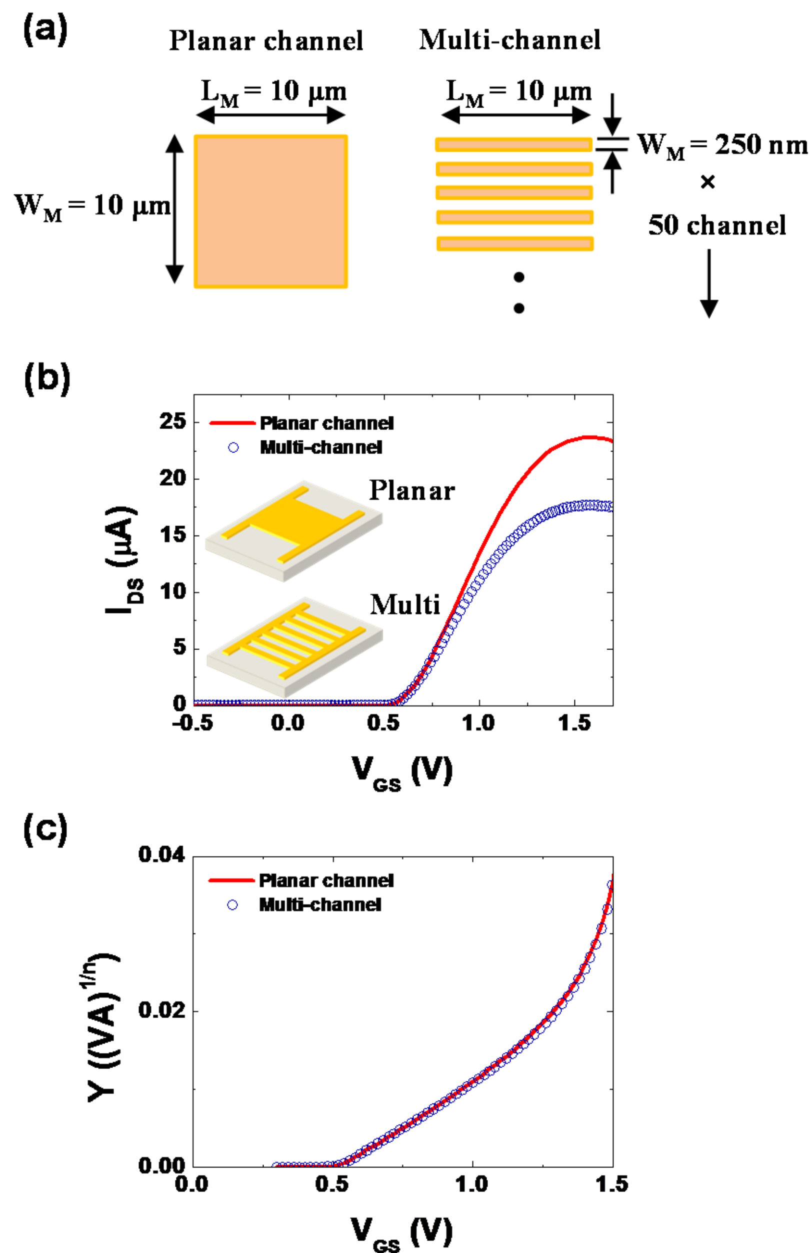

Figure 10 (a) Channel configuration of planar device and multi-channel device. (b) The transfer characteristics measured at 77 K on planar MOSFET and multi-channel MOSFET. Both of W_M and L_M are 10 μm in planar device (total W_{eff} = 10 μm – 0.058 μm = 9.942 μm) and multi-channel device of 50 channels with W_M = 250 nm and L_M = 10 μm (total W_{eff} = (0.25 μm – 0.058 μm) × 50 channel = 9.6 μm). (c) Y-function of planar MOSFET and multi-channel MOSFET are well matched.

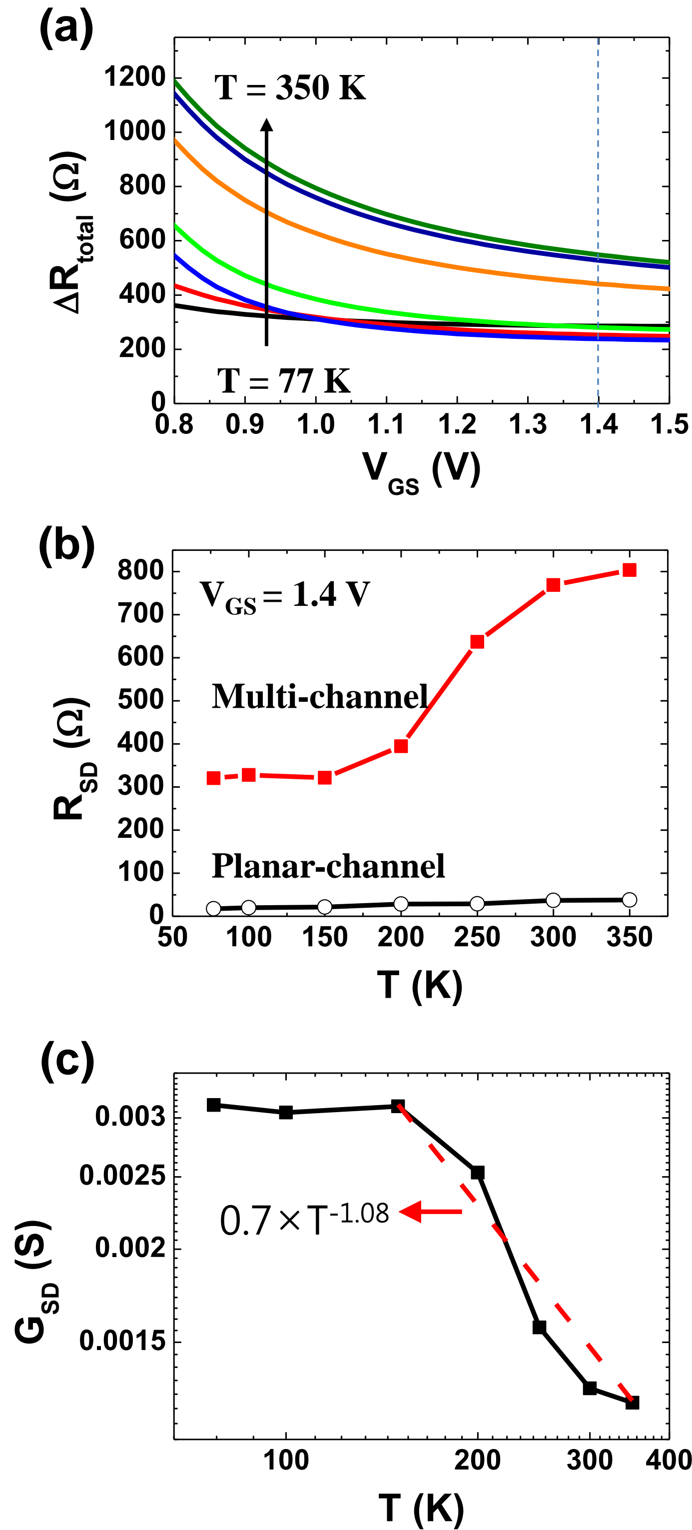

Figure 11 (a) Difference of total resistance in planar MOSFET and multi-channel MOSFET, (b) Series resistance on multi-channel device and planar device as a function of temperature, (c) log-log plot of the series conductance versus temperature in multi-channel device.

Finally, the series resistance of multi-channel MOSFET, R_{SDM} was roughly calculated from the difference of series resistance, ΔR_{SD} and the series resistance of planar device, R_{SDP} extracted using TLM method with devices of different channel length:

$$R_{SDM} = \Delta R_{SD} + R_{SDP} \quad (3.6)$$

In Fig. 11(b), the series resistance of multi-channel device is 20 times higher than the series resistance of planar device (200 Ω·μm - 400 Ω·μm). The variation of parasitic series resistance with channel width was reported previously [11] but it couldn't account for this huge difference series resistance in our results. The temperature dependence of the series resistance in multi-channel device is shown again with the relation between the series conductance and the temperature. (Fig. 11(c)) In Fig. 11(c), the series conductance of multi-channel device (G_{SD}) is inversely proportional to the temperature between 150 K and 350 K. Conductivity ($\sigma = ne\mu$) is dependent only on mobility (μ) in this temperature range since carrier density (n) is not significantly changed due to full impurity ionization [25]. Therefore, it is noted that the mobility is inversely proportional to temperature from G_{SD} behavior. This observation indicates that the origin of high series resistance of multi-channel device electrically behaves like a semiconductor which is not heavily doped [26]. The constant value in temperature range from 77 K to 150 K is attributed to dopant freeze-out and Coulomb scattering [25].

The 2-D numerical simulation was also used to clarify the origin of huge series resistance of multi-channel device. The schematic of n-channel MOSFET and the distribution of potential in the simulated part of device are shown in Fig. 12(a). The dissipation power in unit width P is calculated in contact region with surface integral as:

$$P = \int_S E \cdot JdS \qquad (3.7)$$

where E is the magnitude of electric field , J is the magnitude of current density.

The series resistance multiplied by width R_{SD} is obtained from above dissipation power with drain current in unit width I_d $(= P/V_{DS})$ as:

$$R_{SD} = 2 \cdot \frac{P}{I_d^{\,2}} \qquad (3.8)$$

For the simulation, 4 parameters, resistivity of heavily doped S/D region (ρ_{hdd}), resistivity of extension region (ρ_{ext}), resistivity of silicide (ρ_{sil}), the length of extension from the silicide to the real channel region (L_{ext}), were controlled. The electrical parameters of active channel such as channel width and mobility were excluded for the selection of simulation parameters because Y-function of planar channel device and multi-channel device are matched. The series resistance was calculated through the simulation with these parameters varied with 10 times value and 100 times value from initial

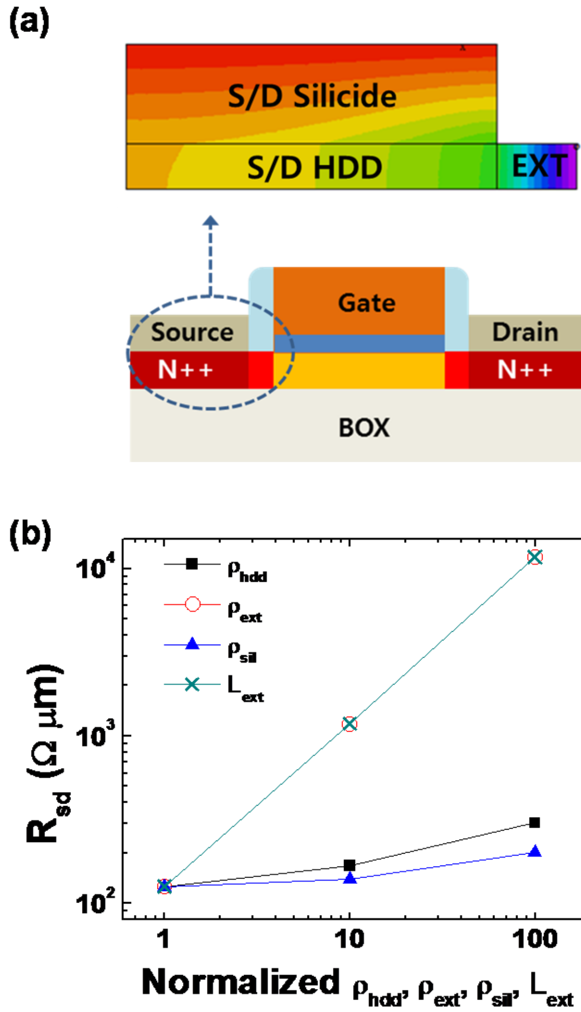

Figure 12 (a) 2-D contour plot of potential distribution in the device simulation and schematic of n-channel MOSFET. (b) Series resistance values were simulated with 4 simulation parameters: resistivity of heavily doped S/D region (ρ_{hdd}), resistivity of extension region (ρ_{ext}), resistivity of silicide (ρ_{sil}), the length of extension from the silicide to the real channel region (L_{ext}) were varied with 10 times value and 100 times value from initial values, 6.3 × 10^{-4} Ω·cm, 3.1 × 10^{-3} Ω·cm, 1.0 × 10^{-4} Ω·cm and 15 nm, respectively and presented with normalized value by their initial values in graph.

values, 6.3 × 10^{-4} Ω·cm, 3.1 × 10^{-3} Ω·cm, 1.0 × 10^{-4} Ω·cm and 15 nm for ρ_{hdd}, ρ_{ext}, ρ_{sil}, L_{ext}, respectively. As shown in Fig. 12(b), the series resistance value can be increased linearly with normalized ρ_{ext} and normalized L_{ext} by their initial value. However, 20 times longer extension length of multi-channel device than that of planar device is not practicable. On the other hand, the resistivity of extension region can be easily modulated by the different doping environment during the implantation in heavily doped S/D region. In particular, the extension region in multi-channel device could have different dopant diffusion condition from that of planar device because multi-channel device has the smaller interface area between S/D HDD region and extension region as shown in Fig. 13 compared to that of planar device. Therefore, the origin of high series resistance in multi-channel device could be attributed to high resistivity of extension region due to the variation of doping concentration. The method to minimize the series resistance and analytical model for series resistance in multi-channel device should be investigated as further research.

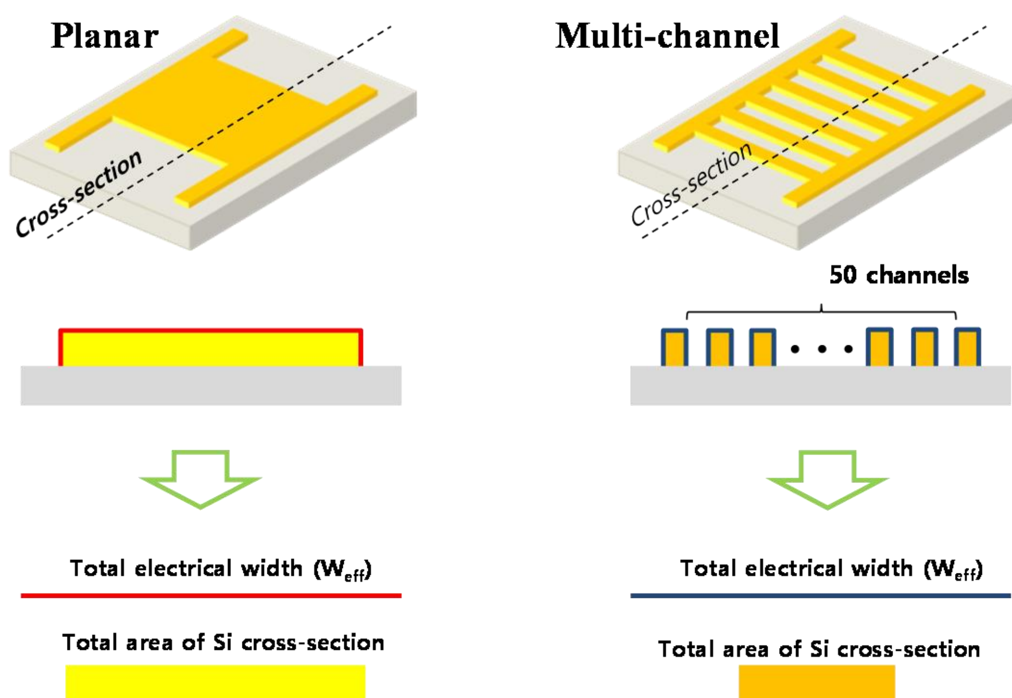

Figure 13 The illustration showing the difference of total area of silicon cross-section in the extension region

4 CONCLUSION

The effect of surface roughness in sidewall mobility was investigated in the multi-channel tri-gate MOSFET structures. From mobility extraction with gate voltage at low temperature, it was shown that the degradation of sidewall mobility is mainly affected by surface roughness scattering. The parameter related to the scattering mechanism was extracted with the fitting of measurement data. The quantification of the effect of surface roughness scattering in the device was carried out with the second order mobility degradation factor normalized by low field mobility. The effect of surface roughness scattering was about 6 times higher in the sidewall of tri-gate MOSFET compared to the top surface of the device. Therefore, the surface roughness scattering can affect mainly the degradation of mobility when the width of channel in tri-gate MOSFET is extremely small.

In addition, the series resistance of multi-channel tri-gate MOSFET shows huge increase compared to the planar type device. With 2-D numerical simulation, the origin of the difference in series resistance is possibly attributed to the reduction of doping concentration in the extension region.

Based on these results, it is outlined that the optimization of fabrication process should be carried out in further research in order to enhance the performance of multi-channel tri-gate MOSFET.

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CHAPTER 4

1 INTRODUCTION
2 EXPERIMENTAL DETAILS
3 RESULTS AND DISCUSSION
3.1 Back biasing effect on I-V characteristics and gate-to-channel capacitance
3.2 2-D numerical simulation of the back biasing effect in tri-gate MOSFET
4 CONCLUSIONS

IMPACT OF CHANNEL WIDTH ON BACK BIASING EFFECT IN TRI-GATE MOSFET

The impact of channel width on back biasing effect in n-type tri-gate metal-oxide semiconductor field effect transistor (MOSFET) on silicon-on-insulator (SOI) material was investigated. In narrow device (W_{top_eff} = 20 nm), the relatively high control of front gate on overall channel leads to the reduced electrostatic coupling between back and front channels as well as the suppression of back bias effects on both channel threshold voltage and the effective mobility, compared to the planar device (W_{top_eff} = 170 nm). The lower effective mobility with back bias in narrow device was attributed to poorer front channel interface, and, to significant effect of sidewall mobility. The back biasing effect in tri-gate MOSFET was successfully modeled with 2-D numerical simulation. Through the simulation, the mobility results were interpreted as the consequence of two kinds of mobility degradations, i.e. different mobility attenuation along lateral and vertical directions of channel and additional mobility degradation in narrow device due to the effect of sidewall mobility. The potential profile extracted from numerical simulation provides strong evidence showing different degree of electrostatic coupling in narrow device and planar device due to a relative influence of front gate bias control over channels.

1 INTRODUCTION

The Tri-gate fully-depleted-silicon-on-insulator (FD-SOI) MOSFET with undoped channel is considered as very attractive candidate for further scaling CMOS technologies due to its high immunity to short channel effect (SCE), good mobility and low threshold voltage variability [1-3]. Therefore, tri-gate FD-SOI MOSFETs have huge potential as a device not only for digital but also for analog circuit applications since they offer high on current and transconductance performances [1, 4-6].

However, there are still some issues concerning the tri-gate FD-SOI MOSFET, which are to be investigated in details. For example, the electrostatic coupling between the front and back channels is an important topic since the back biasing effect can be used to further tune the MOSFET performance by threshold voltage adjustment. Daugé et al. reported that the influence of back bias on FinFET with varying channel width and the suppressed variation on transport properties (transconductance, threshold voltage) of narrow fin device was analyzed as the result of strong lateral gate control [7]. In addition, there are reports which have shown the variation of the effective mobility with channel width for FinFET [8, 9]. The back bias effect with multi-gate transistor of various shapes (Tri-gate, Pi-gate, Omega-gate) was also previously evaluated [10]. However, the back biasing effect with different channel widths on the effective mobility and gate-to-channel capacitance in Tri-gate MOSFET is still worthwhile to be studied in details.

In this chapter, the influence of back biasing on the electrical characteristics of tri-gate MOSFET is investigated with different channel top effective width down to 20 nm. The effective mobility with back bias as a function of channel width is studied and it enables to understand the relative strength of front gate control and the different channel interface quality between front channel and back channel. 2-D numerical simulations are performed to physically interpret the variation of electrical characteristics such as threshold voltage, gate-to-channel capacitance and effective mobility with channel width.

2 EXPERIMETAL DETAILS

N-type inversion mode MOSFETs were fabricated at CEA-LETI and provided by Sylvain Barraud. Silicon channel of channel top effective width (W_{top_eff}) of 20 nm and 170 nm with channel effective length (L_{eff}) of 10 μm were patterned on (100) SOI wafers as shown in Fig. 1. All devices have been fabricated with a thickness of the buried oxide t_{BOX} = 145 nm and a thickness of undoped top-silicon t_{Si} = 10 nm as described in details elsewhere [11]. The MOSFET channel is defined by optical (deep ultra violet) lithography and resist trimming. HfSiON was deposited by chemical-vapor-deposition (CVD) with an equivalent gate oxide thickness of 1.2 nm. For the midgap metal gate stack, TiN of 5 nm was deposited by atomic layer deposition and capped with polysilicon layer of 50 nm.

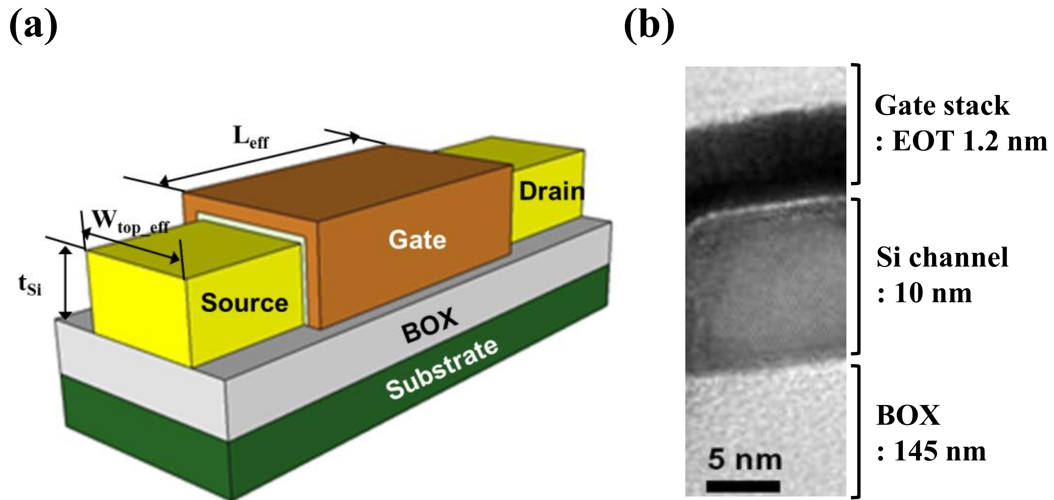

Figure 1. (a) Schematic of the tri-gate MOSFET structure and (b) cross-section TEM image

For clarity, a channel top effective width is defined as:

$W_{top_eff} = W_{eff} - (2 \times t_{Si})$ (1)

W_{eff} was obtained by transfer length method (TLM) using linear relationship between gate-to-channel capacitance and mask channel width W_M (Fig. 2) [12]. The effective channel length L_{eff} ($=L_M - \Delta L$) is also extracted with the effective channel length discrepancy ΔL of around 15 nm obtained using TLM with the I-V characteristic from devices of various channel length [13, 14].

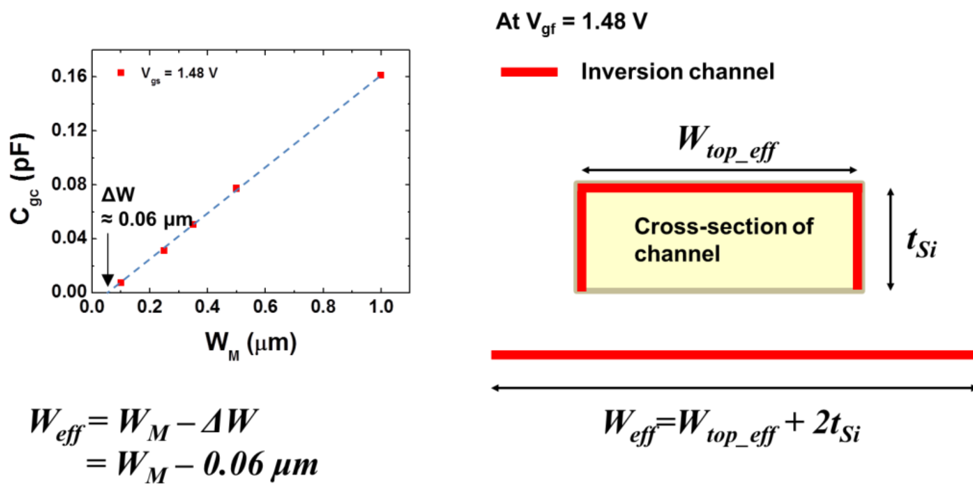

Figure 2 W_{eff} extracted from the TLM method and illustration explaining the relation between W_{eff} and W_{top_eff}

Static I-V characterization was performed using Agilent 4155A measurement unit. Back biasing using grounded source as a reference was applied to the back side of SOI substrate. The gate-to-channel capacitance was measured using a precision HP4294A with the split capacitance-voltage (C-V) method. For better measurement precision, I-V characteristic and gate-to-channel capacitance were
measured with 50 identical channels having a form of 50 fingers and then normalized after the measurements for further analysis. 2-D numerical charge simulation was carried out using Flex PDE 5.0 software based on the finite element method to simulate the gate-to-channel capacitance and the effective mobility.

3 RESULTS AND DISCUSSION

3.1 Back biasing effect on I-V characteristics and gate-to-channel capacitance

Figure 3 (a) and (b) show the n-channel drain current I_{ds} at V_{ds} = 50 mV by varying front gate voltage (V_{gf}) of the tri-gate MOSFET with channel top effective widths (W_{top_eff}) of 20 nm and 170 nm. V_{gf} was applied from −0.5 V to 1.5 V at different back bias V_{gb} from −30 V to 30 V. Relatively huge back bias was applied, compared to front gate bias, considering much thicker BOX thickness (145 nm) than that of front gate insulator (EOT = 1.2 nm). I_{ds} - V_{gf} curves of narrow tri-gate MOSFET (W_{top_eff} = 20 nm) are only slightly affected by back bias V_{gb} while those of planar tri-gate MOSFET (W_{top_eff} = 170 nm) exhibit significant voltage shift. The influence of back bias according to the channel width is more clearly observed with the derivative of transconductance dg_m/dV_{gf} in Fig. 3 (c) and (d). dg_m/dV_{gf} versus V_{gf} in narrow device exhibits single peak regardless of V_{gb} variation and it indicates that only front gate bias dominantly controls the inversion channel, which is consistent to the previous report [7]. In contrast, dg_m/dV_{gf} characteristic of planar device shows two separated peaks when V_{gb} > 0 V. The two peaks are composed of the first peak (the left-side peak) shifted with back bias and the second peak (the right-side peak) which keeps its position nevertheless V_{gb} is varied. The first peak positioned in the region of V_{gf} < 0 V shows that an inversion channel is activated at the back interface by the back biasing since the peak of dg_m/dV_{gf} depicts a threshold voltage [15]. On the other hand, the second peak corresponds to the inversion mainly governed by front gate bias.
Similar to drain currents trend, gate-to-channel capacitance C_{gc} behavior shows the different back bias effect on planar device and narrow device as plotted in Fig. 5 (a) and (b). The gate-to-channel capacitance curve in planar device is noticeably changed by the variation of back bias compared to that in narrow device which is slightly affected by varying the back bias. Moreover, the additional shoulder

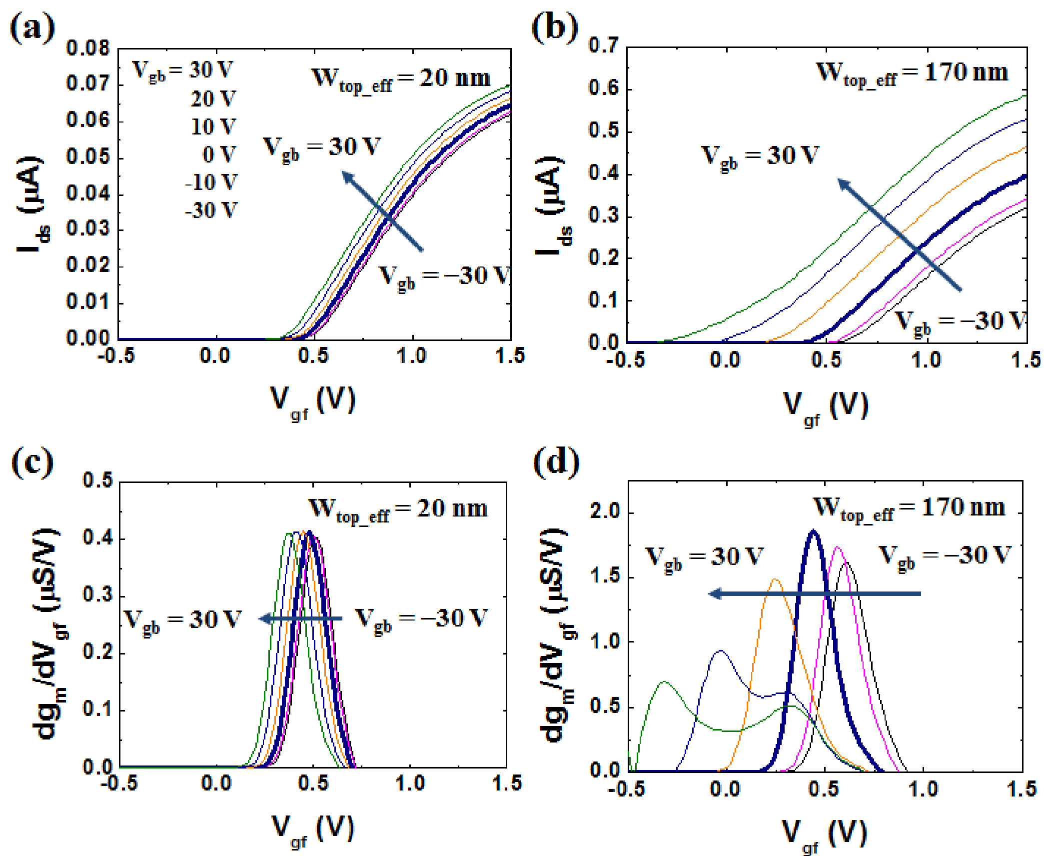

Figure 3 N-channel drain current of the tri-gate MOSFET measured at V_{ds} = 50 mV with channel top effective widths (W_{top_eff}) of (a) 20 nm and (b) 170 nm when back bias V_{gb} is varied from –30 V to 30 V. The corresponding dg_m/dV_{gf} curves for the tri-gate MOSFET of (c) W_{top_eff} = 20 nm and (d) W_{top_eff} = 170 nm. Drain currents and dg_m/dV_{gf} at V_{gb} = 0 V are plotted with bold line.

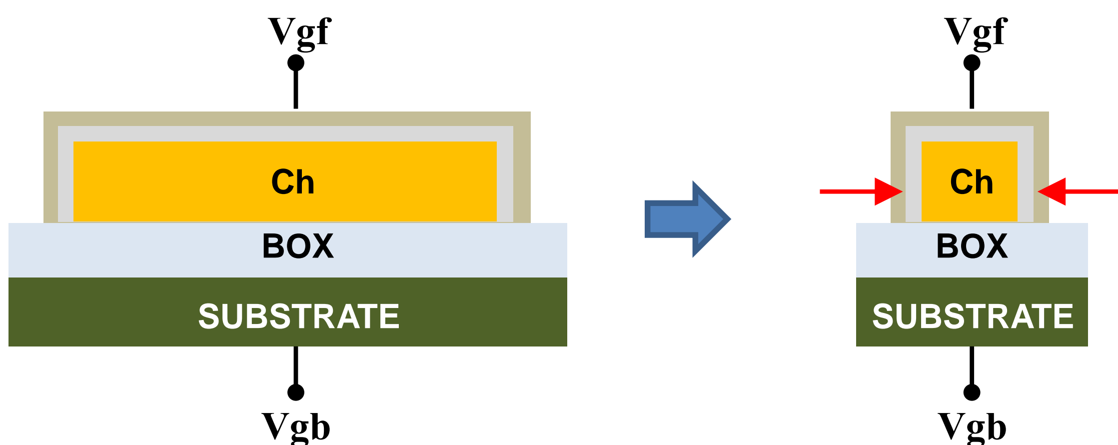

Figure 4 Illustration of sidewall gate effects when the width is extremely small.

is shown in gate-to-channel capacitance curve of planar device (Fig. 5 (b)) with positive back bias, indicating that the additional channel is created at the back interface by back bias. The first peak (the left-side peak) according to the additional shoulder is clearly shown in dC_{gc}/dV_{gf} versus V_{gf} plot of planar device as shown in Fig. 3 (d), which is consistent to the previous dg_m/dV_{gf} results (Fig. 3 (d)). It should be noted that the channel of narrow tri-gate MOSFET is significantly affected by sidewall gates, which is the reason why the narrow device possesses only single peak (Fig. 5(c)) denoting less effects from back bias. Planar device also shows single peak in dC_{gc}/dV_{gf} when $V_{gb} \leq 0$ V since the back bias does not create a back inversion channel.

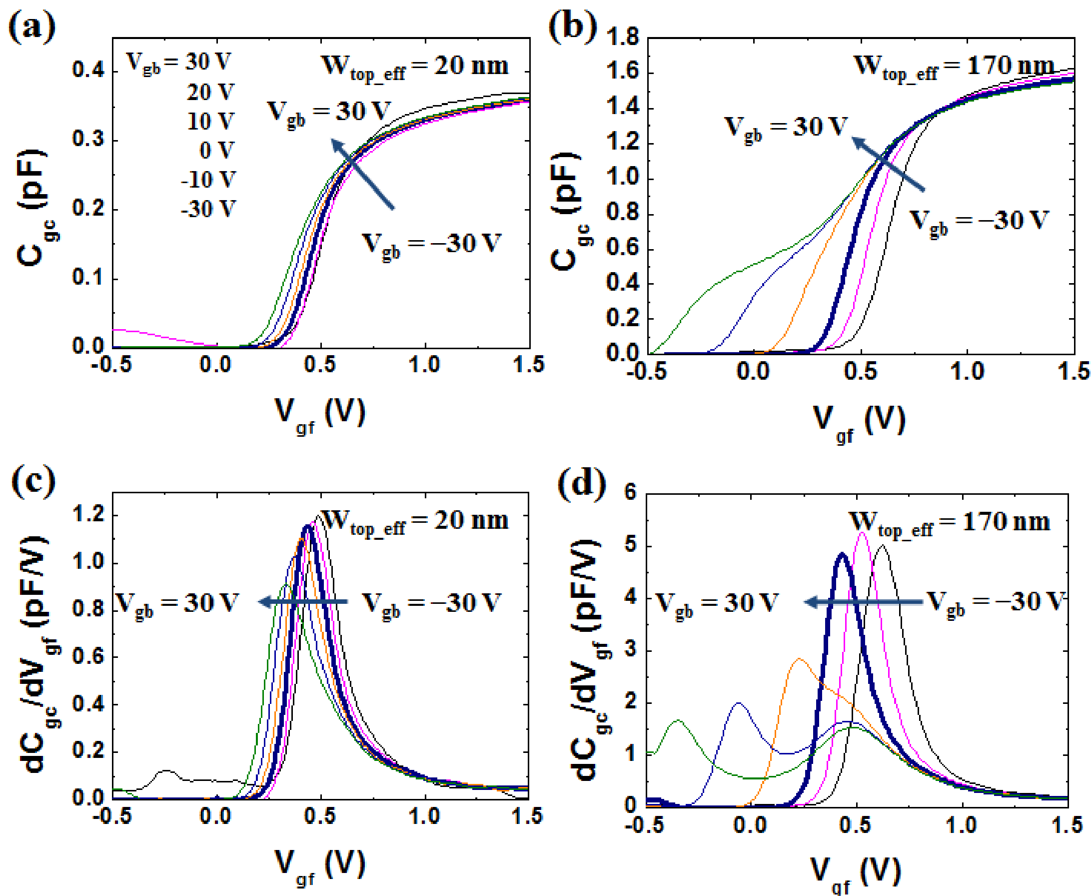

Figure 5 Gate-to-channel capacitance C_{gc} behavior shows the difference between (a) narrow device (W_{top_eff} = 20 nm) and (b) planar device (W_{top_eff} = 170 nm) when back bias is applied from –30 V to 30 V. The corresponding dC_{gc}/dV_{gf} curves for the tri-gate MOSFET of (c) W_{top_eff} = 20 nm and (d) W_{top_eff} = 170 nm. C_{gc} and dC_{gc}/dV_{gf} at V_{gb} = 0 V are plotted with bold line.

The conduction threshold voltages obtained from peaks in dC_{gc}/dV_{gf} curve, to eliminate the effect of series resistance [16], are plotted in Fig. 6. The threshold voltage defined by the position of single peak in dC_{gc}/dV_{gf} -V_{gf} is presented as V_{th} for both narrow and planar devices. For $V_{gb} > 0$ V, V_{thb} and V_{thf} are obtained from the first peak and the second peak, respectively, in dC_{gc}/dV_{gf} of the planar device. In Fig. 6 (a), V_{th} of narrow device is decreased as V_{gb} is increased. In planar device, V_{th} is decreased with V_{gb} like in narrow device when $V_{gb} < 10$V and it is separated into V_{thb} and V_{thf} when $V_{gb} \geq 10$ V (Fig. 6 (b)). It is interesting to notice that V_{thf} is almost constant with V_{gb}, although, V_{thb} is reduced as V_{gb} is increased. The V_{thf} trend is likely stemming from dominant front gate control on the inversion channel in Tri-gate structure.

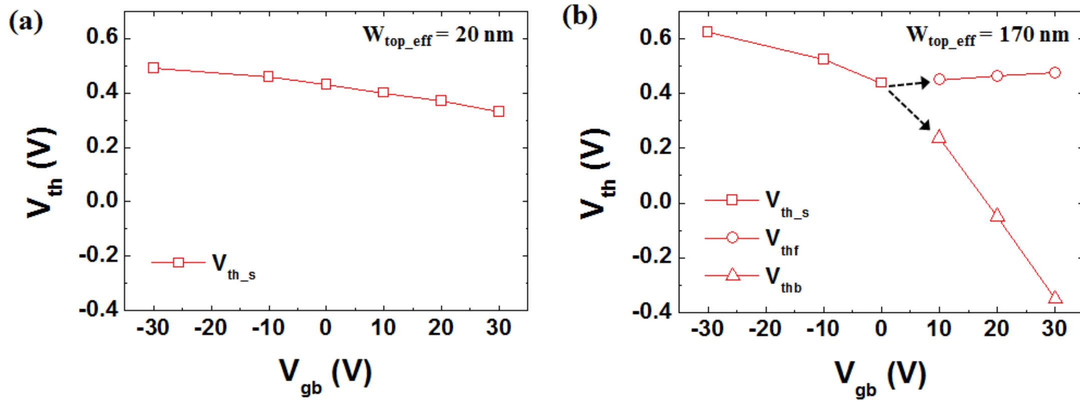

Figure 6 . Threshold voltages V_{th} obtained from the peak position in dC_{gc}-V_{gf} curve for tri-gate MOSFET of (a) $W_{top_eff} = 20$ nm and (b) $W_{top_eff} = 170$ nm. The threshold voltage defined by the position of single peak in dC_{gc}/dV_{gf} -V_{gf} plot is presented as V_{th} for both of narrow device and planar device. For $V_{gb} > 0$ V, the threshold voltages of planar device related to the first peak in dC_{gc}/dV_{gf} is named as V_{thb} and the threshold voltage depicted by the position of the second peak in dC_{gc}/dV_{gf} is named as V_{thf}.

The effective mobility was also extracted from transfer characteristics and gate-to-channel capacitance for narrow and planar channels as:

$$\mu_{eff}(V_{gs}) = \frac{L_{eff} I_{ds}}{W_{eff} Q_i(V_{gs}) V_{ds}} \qquad (4.2)$$

$$Q_i(V_{gs}) = \int_{-\infty}^{V_{gs}} \frac{C_{gc}(V_{gs})}{W_{eff} L_{eff}} dV_{gs} \qquad (4.3)$$

where Q_i is the inversion charge per unit area (C/cm^2). As shown in Fig. 7, the effective mobility of planar device is significantly shifted as the back bias varies from −30 V to 30 V, while the effective mobility in narrow device shows very small shift with the variation of back bias. The effective mobility behavior illustrates that the back bias effect is more pronounced in planar channel compared to

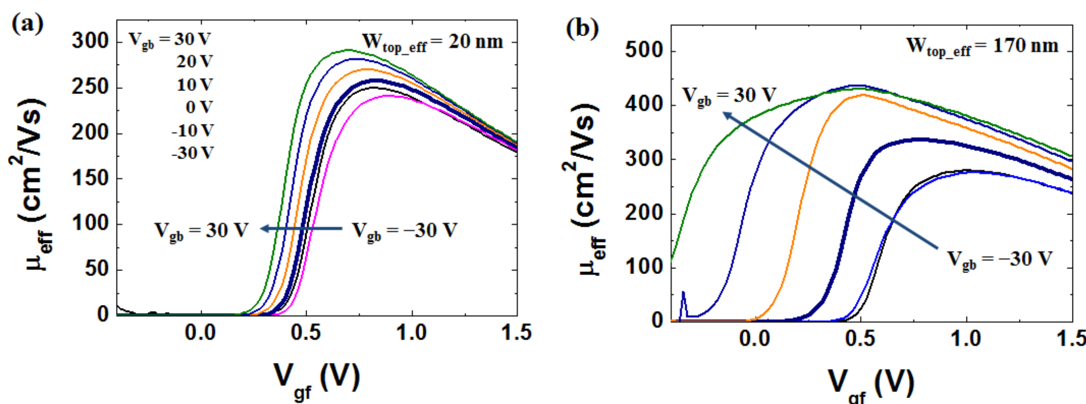

Figure 7 The effective mobility for tri-gate MOSFET of (a) W_{top_eff} = 20 nm and (b) W_{top_eff} = 170 nm when back bias V_{gb} is varied from –30 V to 30 V. The shift of effective mobility in narrow device, corresponding to varying the back bias from –30 V to 30 V, is significantly suppressed. The effective mobility at V_{gb} = 0 V is plotted with bold line.

narrow ones. It is worth noting that the maximum effective mobility is smaller in narrow device as compared to that in planar device. This is attributed to the lower mobility at the sidewall and top oxide interfaces of the channel. Indeed, the high-κ material has a poorer interface property as compared to pure thermal oxide, where there is fewer defects and, by turn, lower remote Coulomb scattering [17]. Therefore, the mobility at the bottom interface on SiO_2 is higher compared to that in top and sidewall interfaces with HfSiON gate dielectric. In narrow device, the contribution of back channel is small and the effective mobility, mainly controlled by top and sidewall interfaces, shows relatively low value. Even for planar device, the mobility is significantly reduced when the front gate field effect is dominating the mobility behavior i.e., in the range of V_{gb} < 0V, where the back inversion channel doesn't exist. In addition, the mobility degradation corresponding to sidewall conduction,

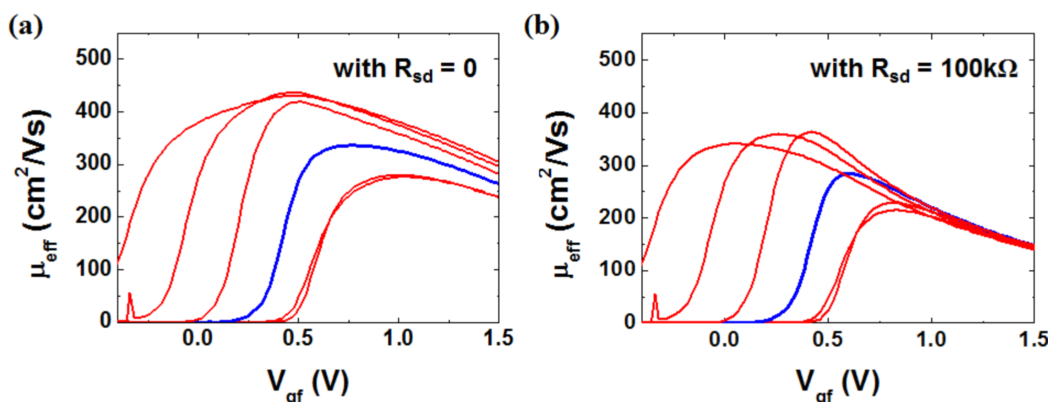

Figure 8 The effective mobility of planar device (a) with R_{sd} = 0 and (b) with R_{sd} = 100 kΩ.

which could be associated to etching process induced defects and/or different crystal orientation, becomes remarkable in narrow channel since the portion of sidewall contribution is substantial in total channel transport when channel width is extremely small [7, 18-20]. It is worth noticing that the effect of series resistance was examined and it can't reproduce the trend experimentally observed for narrow device with back bias (Fig. 8).

3.2 2-D numerical simulation of the back biasing effect in tri-gate MOSFET

The influence of back biasing on electrical characteristic of tri-gate MOSFET can be studied by 2-D numerical simulation of Poisson's equation. In simulation, gate-to-channel capacitance was calculated as:

$$C_{gc}(V_{gs}) = \frac{1}{(W_{top} + 2t_{Si})} \frac{dQ_n}{dV_{gs}} \qquad (4.4)$$

$$Q_n = q\int_S ndS \qquad (4.5)$$

where n is the volume carrier concentration (/cm^3), Q_n is the total integrated charge over the silicon

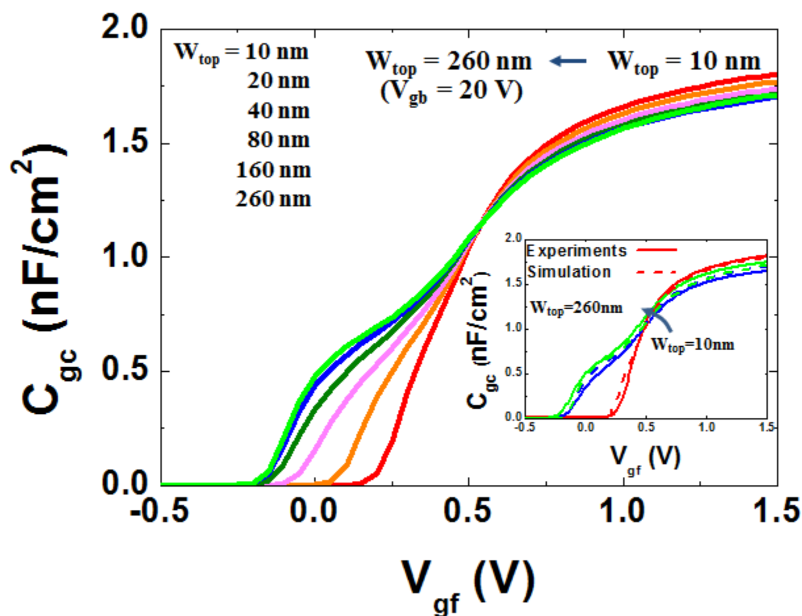

Figure 9 Gate-to-channel capacitance was simulated with the device of channel top width W_{top} varied from 10 nm to 260 nm at V_{gb} = 20 V. Inset: Simulated gate-to-channel capacitance is compared to the experimental results.

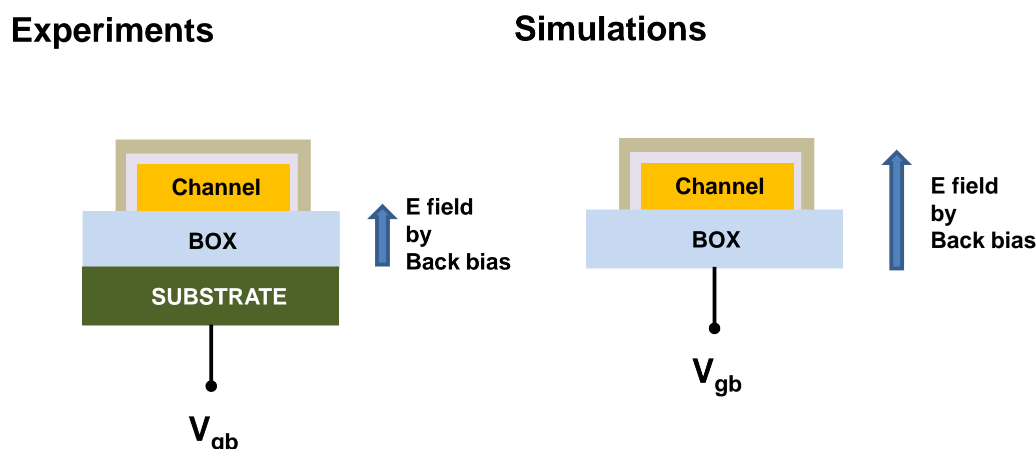

Figure 10 Illustration showing that the difference of electric field strength between experiments and simulations

channel (C/cm) and S is the cross section area of silicon channel.

As shown in Fig. 9, gate-to-channel capacitance was simulated at V_{gb} = 20 V with tri-gate MOSFET structure of top width W_{top} from 10 nm to 260 nm. The top width W_{top} is distinguished with experimental channel top effective width W_{top_eff} because the condition of simulation is inherently different from that of the experiment. For example, the back bias is applied at bottom side of BOX in simulation while back bias was actually applied at bottom of substrate in experiments. (Fig. 10) Thus, it can be expected that the field induced by back bias could be stronger in simulation than that in the experimental result where depletion could occur in the substrate. However, it should be noted that the simulation results well reproduced the experimental data as shown in the inset of Fig. 9. Similarly to experiment, simulated gate-to-channel capacitance characteristics exhibit a shoulder with back bias in planar device while this is not observed in narrow device. The transition of gate-to-channel capacitance shape with varying W_{top} is clearly shown in the simulation results. As the W_{top} is decreased, front gate bias plays an increasing role and the contribution of back biasing on channel formation is diminished. Accordingly, the shoulder shape on gate-to-channel capacitance curve is gradually changed as W_{top} is reduced and is finally disappeared when W_{top} = 10 nm. For planar devices, the back inversion channel controlled by the back bias, featured by the shoulder shape in gate-to-channel capacitance curve, is almost saturated when W_{top} reaches 160 nm.

The simulation of the effective mobility was also performed in tri-gate transistor for further study of modification of electrical properties with back bias. The effective mobility is described by a universal relationship between the effective mobility and transverse electric field as [21]:

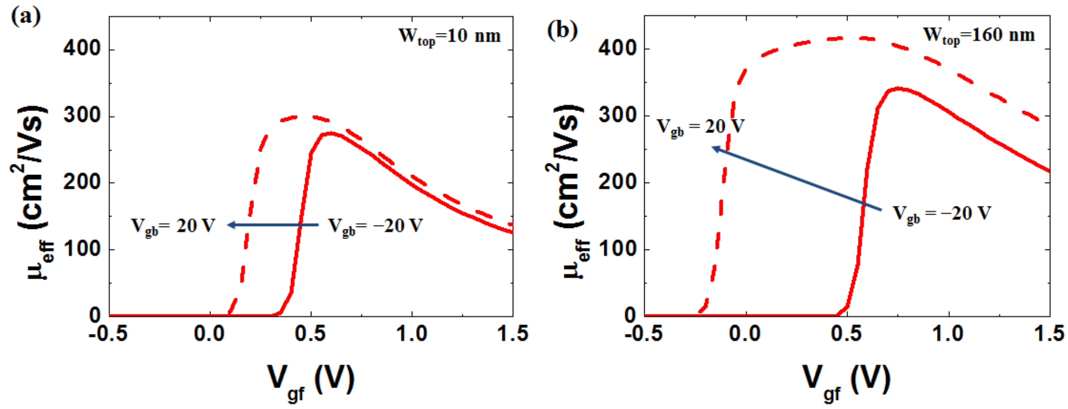

Figure 11 Simulated effective mobility with the device structure of (a) W_{top} = 10 nm and (b) W_{top} = 160 nm at V_{gb} = 20 V and V_{gb} = –20 V.

$$\mu_{eff} = \frac{\mu_0}{\left(1+\left(\frac{E_x}{E_{cx}}\right)^{\alpha_x}+\left(\frac{E_y}{E_{cy}}\right)^{\alpha_y}\right)} \qquad (6)$$

where μ_0 is low field mobility, E_x, E_y are the local electric fields along x-axis (along the channel width) and y-axis directions (along the channel height), respectively, E_{cx} is the critical field in x-axis, E_{cy} is the critical field in y-axis , α_x and α_y are the exponents representing the degree of mobility degradation to the local electric field.

Due to the different interface quality and orientation from top/sidewall to bottom, the low field mobility is considered to vary along the height of silicon channel as:

$$\mu_0 = \mu_{0back} + (\mu_{0top} - \mu_{0back}) \times \frac{y}{t_{Si}} \qquad (7)$$

where, μ_{0back}, μ_{0top} are the low field mobility of back surface and top surface, respectively. y is the coordinate along the channel height.

The mobility simulation results at V_{gb} = –20 V and 20 V are shown in Fig. 11 with $E_{cx} = 5 \times 10^5$ V/cm, $E_{cy} = 10^6$ V/cm, $\alpha_x = \alpha_y = 2$. For W_{top} = 10 nm, μ_{0back} = 330 cm^2/Vs, μ_{0top} = 280 cm^2/Vs were used to fit the experimental data with consideration of sidewall mobility degradation in narrow channel while μ_{0back} = 450 cm^2/Vs, μ_{0top} = 400 cm^2/Vs were used when W_{top} = 160 nm. The effective mobility of narrow device has smaller change with back bias due to weaker electrostatic coupling between back and front interfaces than that of planar device. The simulation results for the

effective mobility, showing suppressed voltage shift and degraded mobility in narrow device, is in qualitatively good agreement with the experimental results.

The potential distribution in silicon channel was extracted from the simulation in order to analyze the electrostatic coupling between front and back interfaces. The extracted potential distribution with V_{gf} = 0.1 V was compared for V_{gb} = 0 V and V_{gb} = 20 V (Fig. 12) to emphasize the variation of back bias effect with channel width. As shown in Fig. 6, both narrow and planar device are below

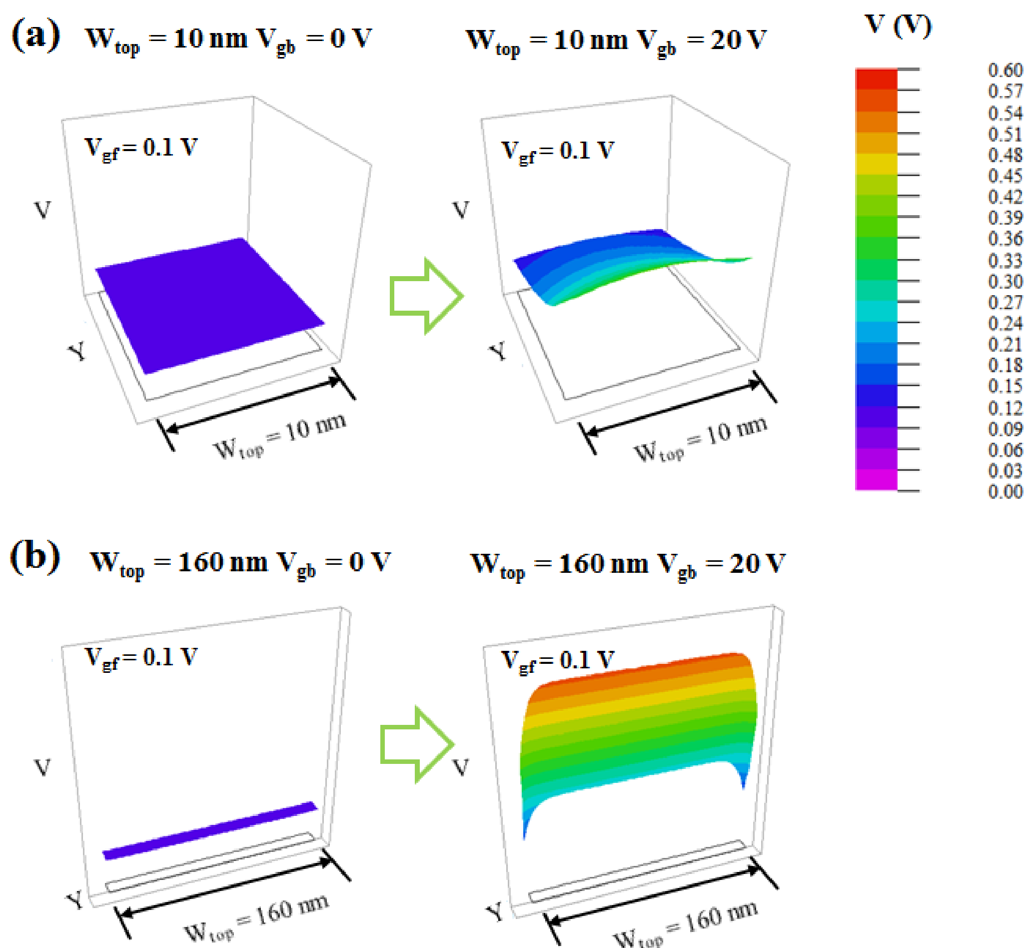

Figure 12 Extracted potential distribution in silicon channel from simulation for (a) narrow device (W_{top} = 10 nm) and (b) planar device (W_{top} = 160 nm). The potentials with V_{gf} of 0.1 V were compared for V_{gb} = 0 V and V_{gb} = 20 V.

threshold at V_{gb} = 0 V. When W_{top} = 10 nm, the potential distribution for V_{gb} = 20 V is relatively less deviated from that for V_{gb} = 0 V, showing that the potential distribution along the depth of the channel is less modulated by the back bias compared to that of planar device. It also means that the narrow channel is mainly controlled by front gate bias from top to bottom with weak electrostatic coupling between back bias and front gate bias, which is associated to the strong influence of sidewall gates.

Whereas, for W_{top} = 160 nm the potential values in silicon channel is significantly increased up to 0.56 V by applying V_{gb} = 20 V, indicating that the electrostatic coupling between front gate bias and back bias is quite strong. This explains why V_{thb} has low value in Fig. 6 (b) since it shows that potential distribution at bottom surface of planar channel is enhanced noticeably by the back biasing.

4 CONCLUSION

The variation of the electrical properties of tri-gate MOSFETs with the back biasing V_{gb} was investigated. The transfer curve and gate-to-channel capacitance C_{gc} characteristic are strongly influenced by the back biasing V_{gb} in planar devices, whereas the back biasing effect is suppressed in narrow devices. The effective mobility characteristic also consistently showed a different behavior with back biasing in narrow and planar device. The front gate control becomes dominant in the electrical characteristic of the Tri-gate MOSFET when the channel width is narrow, i.e. typically below 15-20 nm, and the device showed lower mobility due to the poorer channel-insulator interface quality with high-κ material than that with SiO_2 dielectric at the bottom interface, and, to the mobility degradation on the sidewall.

In addition, the back biasing effect on electrical characteristic of Tri-gate MOSFET with the variation of channel width was well reproduced by 2-D numerical simulation considering sidewall mobility attenuation for narrow channel as well as mobility degradation along channel width and channel height directions. Using the potential profile extracted from the simulation, the impact of back biasing over the channel is weaker in narrow devices since the electrostatic coupling between front and back interface is smaller in narrow device with strong front gate bias control. In contrast, the back bias significantly modulates the potential of the whole channel in planar devices, justifying the strong influence of back bias on electrical characteristics. Our results provide better understanding of the relation between back bias effects and channel width, and, it can be applied for further optimization of device performance and for the design of new multiple-gate MOSFET architecture.

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CHAPTER 5

1 INTRODUCTION
2 EXPERIMENTAL DETAILS
3 RESULTS AND DISCUSSION
3.1 The back bias effect on JLTs
3.2 The back bias effect on narrow JLTs
3.3 2-D numerical simulation results of the back bias effect
4 CONCLUSIONS

BACK BIASING EFFECTS IN TRI-GATE JUNCTIONLESS TRANSISTORS

The back bias effect on tri-gate junctionless transistors (JLTs) has been investigated using experimental results and 2-D numerical simulations, compared to inversion-mode (IM) transistors. Results show that JLT devices are more sensitive to back biasing due to the bulk conduction. It is also shown that the effective mobility of JLT is significantly enhanced below flat band voltage by back bias. However, in extremely narrow JLTs, the back bias effect is suppressed by reduced portion of bulk conduction and strong sidewall gate controls. 2-D numerical charge simulation well supports experimental results by reconstructing the trend of back bias effects

1 INTRODUCTION

Junctionless transistor (JLT) is a new potential candidate for further device scaling. Due to its specific structure, not having junctions, JLT can be free from doping concentration gradient or implant activation annealing. In addition, processing for device fabrication is simple since the same doping concentration is applied from source to drain region.

Due to above advantages, JLT have gotten huge interests in literatures and electrical properties of JLT were highlighted [1-4]. Superior electrical characteristics such as high I_{on}/I_{off} ratio, good subthreshold slope, lower DIBL were observed in nanowire-like JLTs with suppressed short-channel effects [5-7].

However, JLTs possibly have significant back bias effect since they operate in the channel volume and not at the channel surface when gate voltage remains below the flat band voltage [8]. While considerable studies on back bias effect were carried out for inversion-mode (IM) transistors, showing the deviation of device performance such as threshold voltage and transconductance [9-11], the back bias effect on JLTs is not reported so far [12].

In our study, the back bias effect on the electrical behavior of tri-gate JLTs was investigated, compared to that of IM transistors. It is also evaluated on nanowire-like JLTs having very small width. For further analysis, 2-D numerical simulation using Poisson equation was performed for the effective mobility and carrier density extraction in the middle of channel.

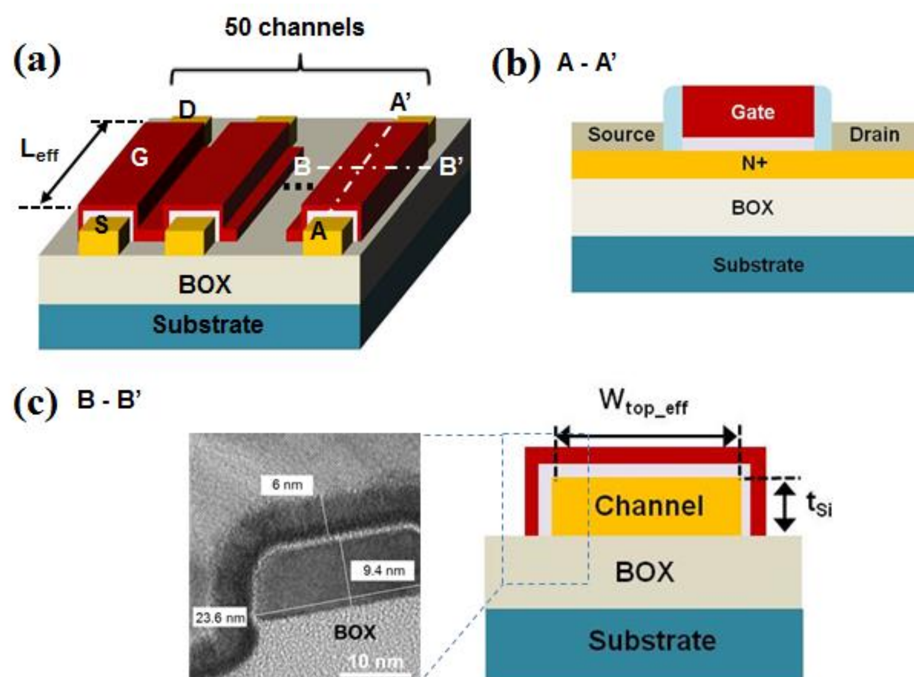

Figure 1 (a) The schematic of the tri-gate MOSFET structure, (b) cross-section along the line A-A’ , (c) cross-section along the line B-B’ and corresponding TEM image.

2 EXPERIMETAL DETAILS

N-type tri-gate JLT devices were fabricated on a (100) SOI wafers with 145 nm thick buried oxide (BOX) at CEA-LETI (provided by Sylvain Barraud), similar to the one described in elsewhere [4, 13]. The Si body was thinned down to ≈ 9.4 nm and ion implantation was carried out with a phosphorus doping, which is resulted as 5×10^{18} cm^{-3} [4]. The channel of transistor is defined by optical (deep ultra violet) lithography and resist trimming. The gate stack is formed by HfSiON/ TiN/ Polysilicon (1.2 nm equivalent oxide thickness). Tri-gate JLT devices featuring channel effective length L_{eff} = 10 μm and channel top effective width W_{top_eff} = 20 nm/ 170 nm in arrays of 50 channels were selected for more accurate gate-to-channel capacitance measurement. The reference IM device was fabricated with the same structure of JLT devices, except that the channel was remained undoped. The schematic architecture of the tri-gate JLT devices is shown in Fig. 1(a). For clarity, in Fig. 1(b) and (c), schematic cross-section along the lines A-A' and B-B' are displayed, respectively. The cross-section TEM image clearly shows gate stack and thinned silicon channel on BOX.

The current-voltage I-V characteristics were measured at V_{ds} = 50 mV, applying back bias on the substrate, with Agilent 4155A measurement unit. The gate-to-channel capacitance was recorded at 500 kHz using an HP 4294A with the split capacitance-voltage (C-V) method. 2-D Poisson equation numerical simulations were carried out using Flex PDE 5.0 software based on the finite element method.

3 RESULTS AND DISCUSSION

3.1 The back bias effect on JLTs

Figure 2 (a) shows the variation of transconductance (g_m) as a function of front gate voltage V_{gf} for different back bias conditions in n-channel JLT (W_{top_eff} = 170 nm, L_{eff} = 10 μm). The lateral shift of the drain current normalized by total channel effective width W_{eff} (= (W_{top_eff} + 2 × t_{si}) × 50) is occurred by changing the back bias V_{gb} from –20 V to 20 V, as shown in insets. In an n-channel JLT, above the threshold voltage, a part of channel becomes neutral with bulk carriers and the gate bias which reaches the flat band voltage V_{fb} makes whole channel neutral [8]. Transconductance behavior in JLTs is different from the trend of IM transistor as shown in Fig. 2(b), which has the same geometry with JLT, due to the existence of the bulk conduction in JLT [14]. It is more clearly shown in derivative of transconductance, dg_m/dV_{gf}, curves (Fig. 2(c) and (d)). The additional peak in JLTs, reflecting the threshold voltage of neutral bulk channel starts to appear when V_{gb} = 0 V, different from IM transistors, and, it is significantly shifted by back bias. However, IM transistor only shows the additional peak in dg_m/dV_{gf} curve at high back bias (V_{gb} = 20 V) due to the formation of back inversion channel for positive back bias [11]. Calculated dV_{th}/dV_{gb} are 26.7 mV/V and 24 mV/V for JLTs and IM device, respectively. It means that bulk neutral channel is more easily influenced by back bias,

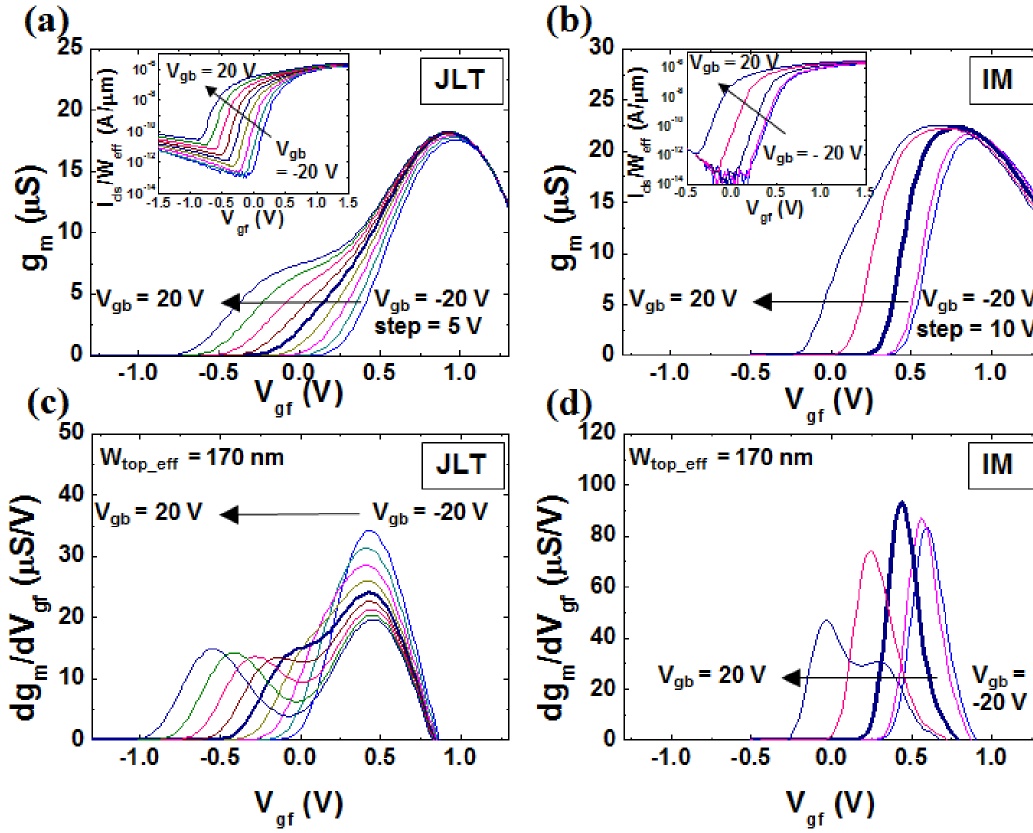

Figure 2 The transconductance measured at V_{ds} = 50 mV with channel top effective width (W_{top_eff}) of 170 nm for (a) JLT and (b) IM transistor when back bias V_{gb} is varied from –20 V to 20 V (Inset: normalized drain current by total channel effective width W_{eff} (= (W_{top_eff} + 2 × t_{si}) × 50) for JLT device and IM device). The corresponding dg_m/dV_{gf} curves for (c) JLT and (d) IM transistor, respectively. Bold line denotes the plots with V_{gb} = 0 V.

compared to IM device. As bulk neutral channel is located in the center of channel, the effective gate capacitance between the channel and the front gate is decreased [15]. Accordingly, the front gate control weakens, which could lead to relatively higher controllability of back bias in JLTs.

Figure 3(a) and (b) shows effective channel mobility behaviors obtained with transfer characteristics and gate-to-channel capacitance C_{gc} by varying back bias for JLT and IM transistor, respectively. The effective mobility was extracted as;

$$\mu_{eff} = \frac{I_{ds} L_{eff}}{W_{eff} Q_i V_{ds}} \qquad (5.1)$$

$$Q_i(V_{gf}) = \int_{-\infty}^{V_{gf}} \frac{C_{gc}(V_{gf})}{W_{eff} L_{eff}} dV_{gf} \qquad (5.2)$$

where Q_i is the inversion charge per unit area.

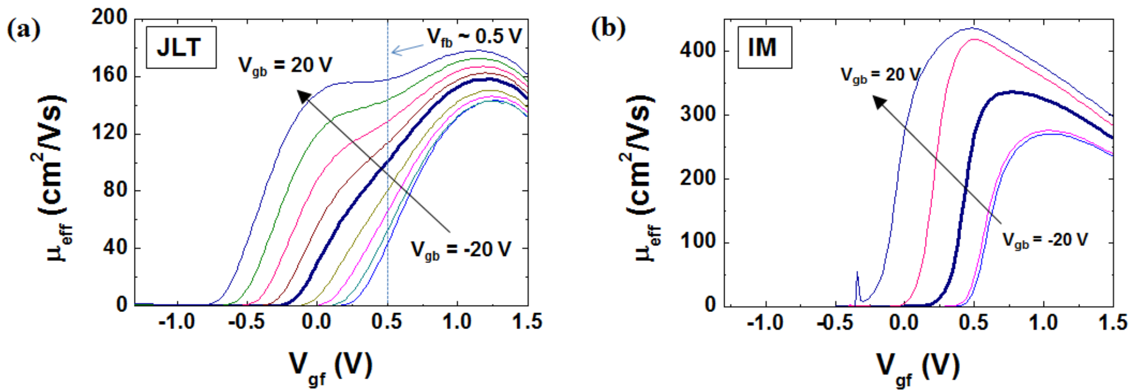

Figure 3 The effective mobility for (a) JLT and (b) IM transistor when back bias is applied from –20 V to 20 V. Bold line denotes the plots with V_{gb} = 0 V.

The effective mobility in JLT exhibits remarkable mobility enhancement with back bias, before V_{fb} (≈ 0.5 V), related to bulk neutral channel conduction. On the other hand, the mobility in JLT is decreased by negative back bias when the back surface of channel is significantly depleted. It should be noted that the V_{fb} of the IM transistor is almost 0 V, attributed to the midgap metal gate and undoped Si channel [16]. The electron bulk mobility in JLTs which have carriers located in the middle of neutral bulk region [8] is strongly degraded by impurity scattering due to high channel doping concentration [17], which is confirmed by low effective mobility value of JLTs in Fig. 3(a). It should be noted that the mobility degradation under high front gate bias is less significant, compared to IM transistor, since the electric field which is perpendicular to the current flow is low in JLTs [18].

3.2 The back bias effect on narrow JLTs

The back bias effect on bulk channel is seriously suppressed in narrow multi-channel JLT (W_{top_eff} = 20 nm, L_{eff} = 10 μm) as shown in Fig. 4. Strongly suppressed transconductance shoulder and lateral shift in Fig. 4(a) show that the portion of bulk conduction is reduced for JLTs of very small width. It was previously found that, as channel width is decreased, the single peak in dg_m/dV_{gf} is observed and the threshold voltage is increased as a result of strong sidewall gate effect and smaller portion of bulk neutral channel in tri-gate JLTs [19]. In Fig. 4(b), single peak is found in dg_m/dV_{gf} curve when V_{gb} = 0 V and the threshold voltage which is depicted by the peak position of dg_m/dV_{gf} is increased in narrow JLT, compared to that of planar like JLT (Fig. 2(c)). However, the peak in dg_m/dV_{gf} is gradually broaden by increasing back bias and, finally, separated into two peaks when V_{gb} = 20 V. Separated peaks are related to the prevailing influence of back bias on the conduction. The effective mobility behavior in narrow JLT also shows limited back bias effects as shown in Fig. 4(c). The enhancement of mobility, found in planar device in Fig. 3(a), was not observed but there is a slight overall increase

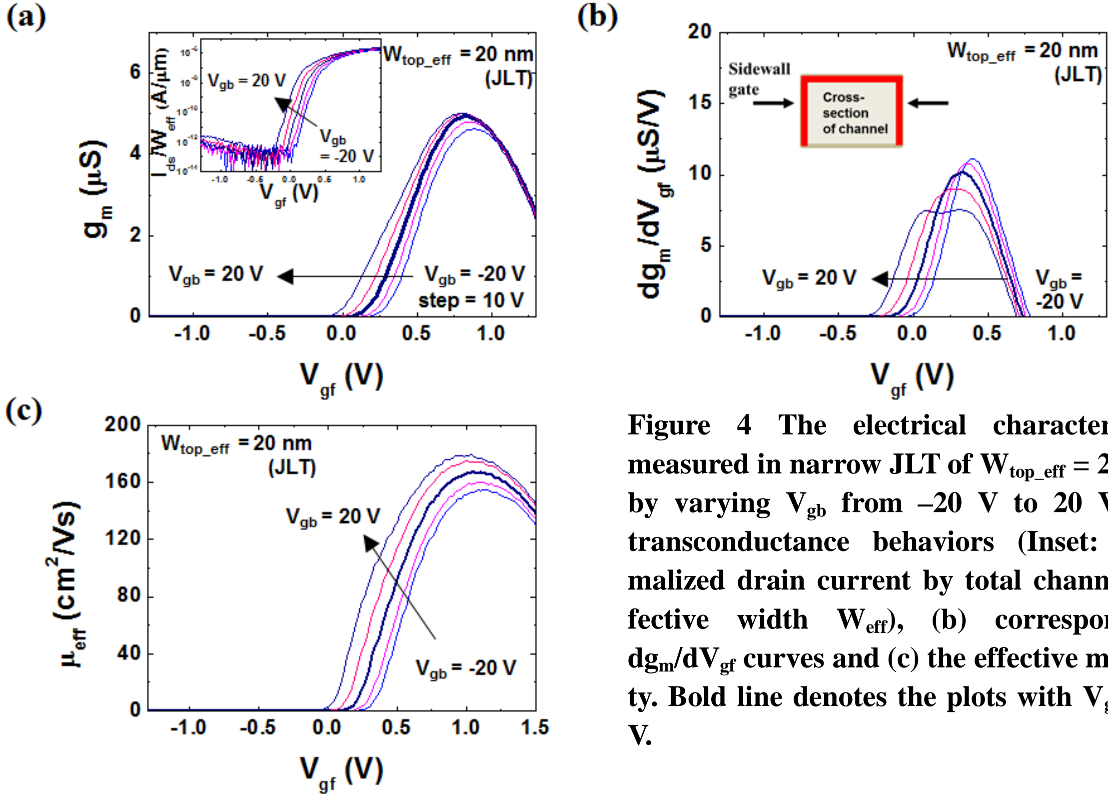

Figure 4 The electrical characteristics measured in narrow JLT of W_{top_eff} = 20 nm by varying V_{gb} from –20 V to 20 V; (a) transconductance behaviors (Inset: normalized drain current by total channel effective width W_{eff}), (b) corresponding dg_m/dV_{gf} curves and (c) the effective mobility. Bold line denotes the plots with V_{gb} = 0 V.

in mobility with back bias. The suppression of back bias effects on extremely narrow device is consistent with reports on IM transistors [9, 10].

3.3 2-D numerical simulation results of the back bias effect

The simple 2-D numerical simulation, using Flex PDE finite element software, was carried out to investigate the back bias effects on JLTs by varying channel doping concentrations and channel widths. For the simulation, the effective channel mobility is described using a universal relationship between the effective mobility and transverse electric field as [20]:

$$\mu_{eff} = \frac{\mu_0}{\left(1 + \left(\frac{E_x}{E_{cx}}\right)^{\alpha_x} + \left(\frac{E_y}{E_{cy}}\right)^{\alpha_y}\right)} \tag{5.3}$$

where μ_0 is low field mobility, E_x, E_y are the local electric fields along x-axis (along the channel width) and y-axis directions (along the channel height), respectively, E_{cx} is the critical field in x-axis, E_{cy} is the critical field in y-axis, α_x and α_y are the exponents representing the degree of mobility degradation to the local electric field. These parameters are fixed as $E_{cx} = 5 \times 10^5$ V/cm, $E_{cy} = 1 \times 10^6$ V/cm, $\alpha_x = \alpha_y = 2$. E_{cx} and E_{cy} were set differently to take into account the effect of

surface roughness scattering on sidewall conduction [21, 22]. μ_0 is given by ;

$$\mu_0 = \mu_{back0} + (\mu_{top0} - \mu_{back0}) \cdot \frac{y}{t_{Si}} \tag{5.4}$$

where μ_{back0} and μ_{top0} are low field mobility at back interface and front interface in Si channel, respectively. The mobility deterioration is observed in JLTs due to the impurity scattering. Hence, μ_{back0} = 150 cm^2/Vs and μ_{top0} = 120 cm^2/Vs were used for $N_D = 5 \times 10^{18}$ /cm^3, while μ_{back0} = 450 cm^2/Vs and μ_{top0} = 400 cm^2/Vs for other doping concentrations. Low field mobility at back interface is considered to be higher than that of top interface since top insulator is high-k material which has poor interface quality while back surface of channel is on pure thermal oxide insulator [23].

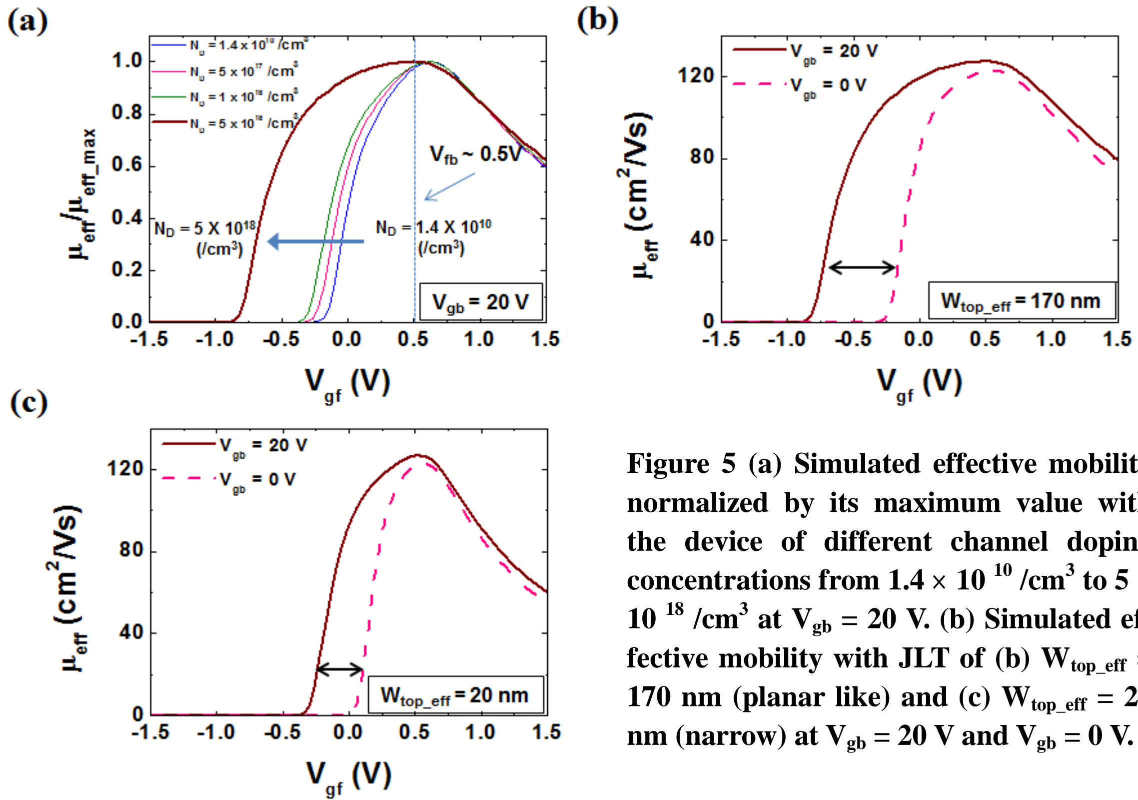

Figure 5 (a) Simulated effective mobility normalized by its maximum value with the device of different channel doping concentrations from 1.4 × 10 ^{10} /cm^3 to 5 × 10 ^{18} /cm^3 at V_{gb} = 20 V. (b) Simulated effective mobility with JLT of (b) W_{top_eff} = 170 nm (planar like) and (c) W_{top_eff} = 20 nm (narrow) at V_{gb} = 20 V and V_{gb} = 0 V.

Figure 5 (a) shows the simulated effective mobility normalized by their maximum values at V_{gb} = 20 V with various doping concentrations from $N_D = 1.4 \times 10^{10}$ /cm^3 to $N_D = 5 \times 10^{18}$ /cm^3. As the channel doping concentration is increased, the device displays lateral shift of the effective mobility and the enhancement of the effective mobility when $N_D = 5 \times 10^{18}$ /cm^3 is noticeable, which is previously shown in the experimental result in Fig. 3(a). Figure 5(b) and (c) show simulated effective mobility behaviors of planar like JLT (W_{top_eff} = 170 nm) and narrow JLT (W_{top_eff} = 20 nm), respectively, as a

function of V_{gf} at V_{gb} = 20 V and V_{gb} = 0 V. In the case of the narrow JLT, it is clearly observed that the effective mobility trend is less affected by back bias.

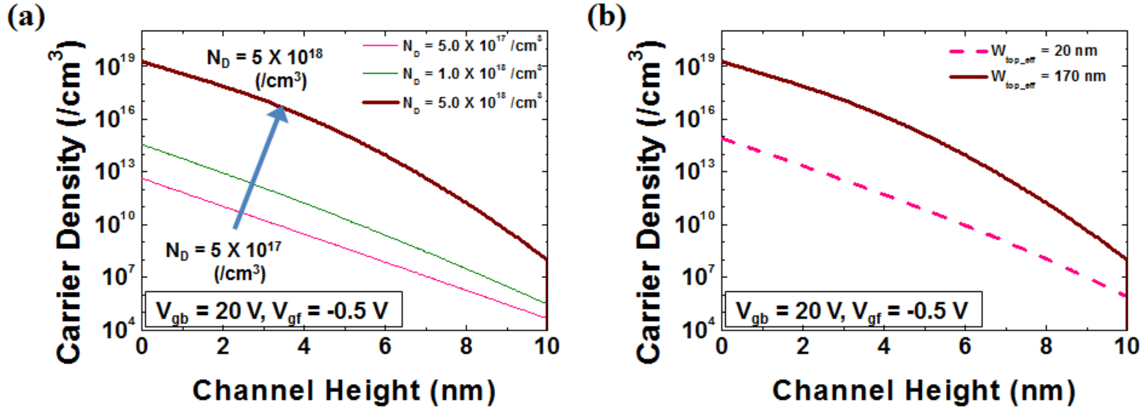

Figure 6 The extracted carrier density along the channel height in the middle of channel silicon at V_{gb} = 20 V for (a) different channel doping concentrations from 5 × 10 ^{17} /cm^3 to 5 × 10 ^{18} /cm^3 and (b) different channel top effective width W_{top_eff} = 20 nm and W_{top_eff} = 170 nm.

The simulated carrier density along the height of Si body in the middle of the channel is shown to elucidate the back bias effect in JLTs. Figure 6(a) presents the influence of doping concentration on the extracted carrier density at V_{gb} = 20 V and V_{gf} = –0.5 V. For N_D = 5 × 10 ^{18} /cm^3, the channel at the Si-BOX interface (channel height = 0 nm) is slightly accumulated whereas it is still depleted for other doping concentrations. This result roughly explains much lower threshold voltage of JLTs with back biasing, shown in Fig. 2, than that of IM transistor.

The back bias effect according to the channel width, when doping concentration is fixed N_D = 5 × 10 ^{18} /cm^3, is also addressed in Fig. 6(b) for W_{top_eff} of 20 nm and 170 nm at V_{gb} = 20V and V_{gf} = –0.5V. It is seen that, for very narrow devices, the carrier density is not recovered to its original doping level even at Si-BOX interface, indicating that the channel is rather insensitive to back bias. These results could support the fact that the electrical behavior of narrow JLTs is more immune to back biasing, compared to IM transistors.

4 CONCLUSION

The back bias effect on JLTs has been experimentally investigated with comparison to that of IM transistor. The transfer characteristic of JLT shows greater V_{th} shifts, associated to the lateral shift of drain current, with back bias than that of IM transistors. In addition, the effective mobility was noticeably enhanced in bulk conduction region with back bias, while overall mobility is degraded by

high doping concentration in JLTs. In narrow device, it was shown that the back bias effect was suppressed by reduced portion of bulk conduction and strong sidewall gates control.
2-D numerical simulations on JLTs have been performed for further analysis of back bias effects and simulation results well support experimental observations.
Consequently, JLT is a very attractive candidate for further scaling, however, the optimization of device performance will be needed to meet specifications for the practical applications.

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CHAPTER 6

1 INTRODUCTION
2 EXPERIMENTAL DETAILS
3 RESULTS AND DISCUSSION
3.1 Static characteristics at room and low temperatures
3.2 LF Noise characteristics
3.2 Numerical simulation
4 CONCLUSIONS

STATIC ELECTRICAL CHARACTERIZATION AND LOW FREQUENCY NOISE OF a-InHfZnO THIN FILM TRANSISTORS

The static characteristics and low frequency noise of a-InHfZnO (IHZO) thin film transistor (TFT) were comprehensively investigated. The effective mobility extracted from the transfer curve and gate-to-channel capacitance-voltage (C_{gc}-V) characteristic is compared with that obtained by Y-function adopted for the first time on AOS TFT. The static characteristics at low temperature show nearly independent electrical property of a-IHZO TFT, illustrating the degenerate behavior of a-IHZO TFT inversion layer. Noise measurement was performed on a-IHZO TFT and indicates that fluctuations stem from carrier trapping-detrapping at the interface between the oxide and channel layer and/or in bulk traps. Based on the analysis with static characteristics and low frequency noise of a-IHZO TFT, a numerical model was proposed and the model including band-tail states conduction and interface traps provides a good agreement with the experimental results.

1 INTRODUCTION

Amorphous oxide semiconductor (AOS) based thin film transistor (TFT) have attracted a great deal of attention to replace amorphous (a-Si:H)/polycrystalline silicon (poly-Si) TFTs as the driver device for active matrix organic light emitting diodes (AMOLED) [1-3] and active matrix liquid crystal displays (AMLCD) [4] since it has key advantages such as excellent electronic transport characteristics including uniformity on carrier mobility and threshold voltage, large carrier mobility (1 − 35.8 cm^2/Vs), and low subthreshold gate swing (~ 0.2 V/decade) [5-8]. AOS TFTs are also a promising candidate for large area flexible displays because they can be fabricated uniformly at low temperature (< 400 ^oC) on large substrate [7]. Furthermore, AOS having high optical transparency allows the fabrication of transparent thin film transistor [9].

To have a better physical understanding on AOS TFTs, Park et al. [10] reported the effects of series resistance in amorphous indium-gallium-zinc-oxide (a-IGZO) TFTs and Theodorou et al. [11] reported that a trap density of 2.3×10^{12} $cm^{-2}eV^{-1}$ extracted from the low frequency noise (LFN) measurement in a-IGZO TFT with SiO_2 gate dielectrics while few publications were dedicated to the LFN of AOS TFT. Several modeling approaches were demonstrated to study the electrical properties of a-IGZO TFT [12, 13].

Among the different AOS TFTs, amorphous indium-hafnium-zinc-oxide (a-IHZO) TFTs has been reported to have better stability, good film uniformity and enhanced performance such as low subthreshold swing, due to the presence of Hf ions which possess high oxygen bonding ability and lower trap density in active channel material [2, 6, 14]. However, there are only few reports on the electrical characterization of a-IHZO TFTs [2, 6].

In this chapter, we present a detailed electrical characterization of a-IHZO TFTs with different channel length. The device electrical parameters are extracted through static characteristics at room and low temperatures and the LFN is also analyzed. A numerical simulation based on a model including the exponential band-tail structure and the interface trap condition is finally presented to better understand static characteristics of a-IHZO TFTs.

2 EXPERIMETAL DETAILS

A schematic of the device structure and a cross section-view transmission electron microscope (TEM) image of the a-IHZO TFT after the deposition of passivation layer are shown in Fig. 1. a-IHZO TFTs were fabricated at Samsung Advanced Institute Technology with staggered bottom-gate configuration on a glass substrate. The gate and source/drain (S/D) electrodes sputtered with Molibdenum were patterned using dry etching. Plasma- enhanced chemical vapor deposition (PECVD) at 370 ^oC was

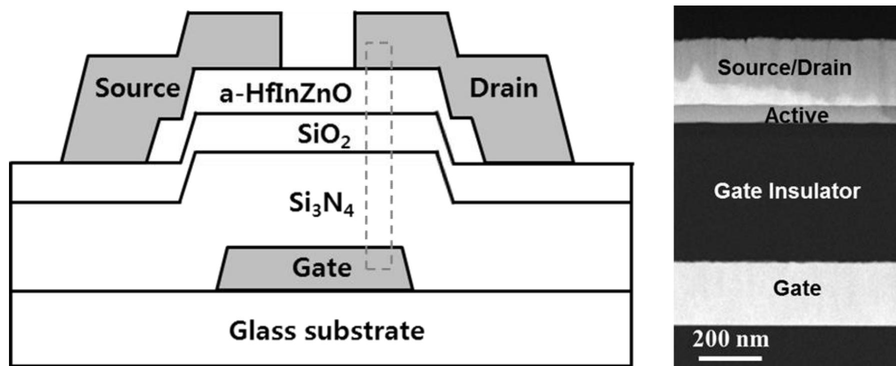

Figure 1 The schematic of the device structure and the corresponding cross-section TEM image of the device which show the uniformity of layers (dotted region in the schematic)

used to form a 350-nm-thick Si_3N_4/50-nm-thick SiO_x bilayer as the gate insulator. Subsequently, 50-nm-thick a-IHZO active thin-film layer was deposited at room temperature via radio frequency sputtering in a mixed atmosphere of Ar and O_2. The sputtering was carried out using IHZO targets, which were prepared through mixing HfO_2, In_2O_3, and ZnO powders, with the composition of HfO_2:In_2O_3:ZnO=0.1:1:1 mol %. Depostion of 100-nm-thick SiO_x etch stopper using PECVD was followed to protect the channel layer from dry etching damage during source/drain patterning. Finally, 200-nm-thick SiO_x was deposited on the TFTs using PECVD as the passivation layer. The completed devices were annealed at 200 °C for 1 hour in ambient air. TFTs with a fixed width W = 100 μm but various mask channel lengths L_M (from 3 μm to 100 μm) were used for the electrical characterizations. The TEM image shows a uniform thickness and a low surface/interface roughness of gate, insulator, channel, and source/drain layers in the resulting devices. The current–voltage characteristics were recorded using an Agilent 4155A measurement unit. The gate-to-channel capacitance was measured with the split capacitance–voltage (C-V) method [15] using a precision HP4284 LCR Meter. Current-voltage measurements at low temperature were performed in probe station equipped as a liquid helium cryostat. The LFN characteristics were measured in the frequency range from 10 Hz to 10 kHz at drain voltage V_{ds} = 0.5V.

3 RESULTS AND DISCUSSION

3.1 Static characteristics at room and low temperatures

As shown in Fig. 2, the drain current I_d was decreased with channel length L_M. This is due to the increase of channel resistance. The $I_d - V_{gs}$ characteristics measured at V_{ds} = 0.5V, which is in linear regime, gives typical effective mobility μ_{eff} of 2 – 4 cm^2/Vs, a threshold voltage V_{th}, which

is obtained from the maximum position of the derivative of transconductance g_m, in the range of 3 – 3.5V, a subthreshold swing S, of 0.2 – 0.5 V/dec and an I_{on}/I_{off} ratio of $10^7 - 10^8$. It was reported that the low mobility was obtained in a-IHZO TFT with high Hf content because of suppressed generation of carriers by Hf ions [6]. The transconductance g_m, presented in the inset of Fig. 2, shows that it is not degraded even under high gate bias, suggesting the absence of mobility degradation and little impact of access series resistance.

To extract the value of the series resistance and the effective channel length, the transfer length method (TLM) was applied. The drain current I_d in the linear regime is defined by:

$$I_d = \frac{W}{L_{eff}} \mu_{eff} C_{ox} (V_{gs} - V_{th}) V_{ds} \qquad (6.1)$$

where, W is a channel width, L_{eff} is a channel effective length, μ_{eff} is a mobility and C_{ox} is a gate-insulator capacitance per unit area.

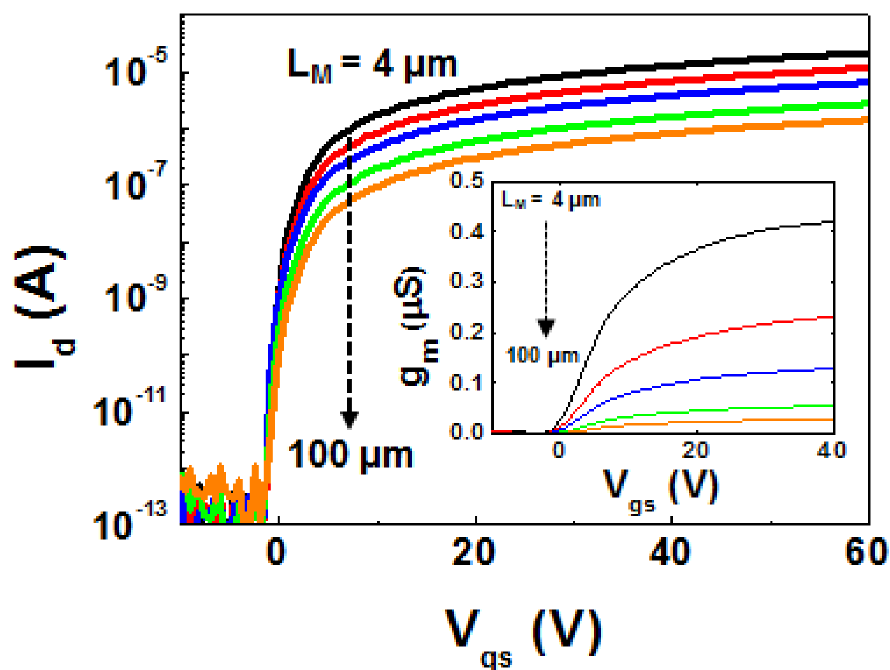

Figure 2 Transfer curves at V_{ds} = 0.5V for a-InHfZnO TFTs with different channel lengths (L_M = 4, 10, 20, 50, 100 μm) and fixed channel width (W = 100 μm). Inset: the corresponding transconductance g_m versus gate voltage V_{gs}.

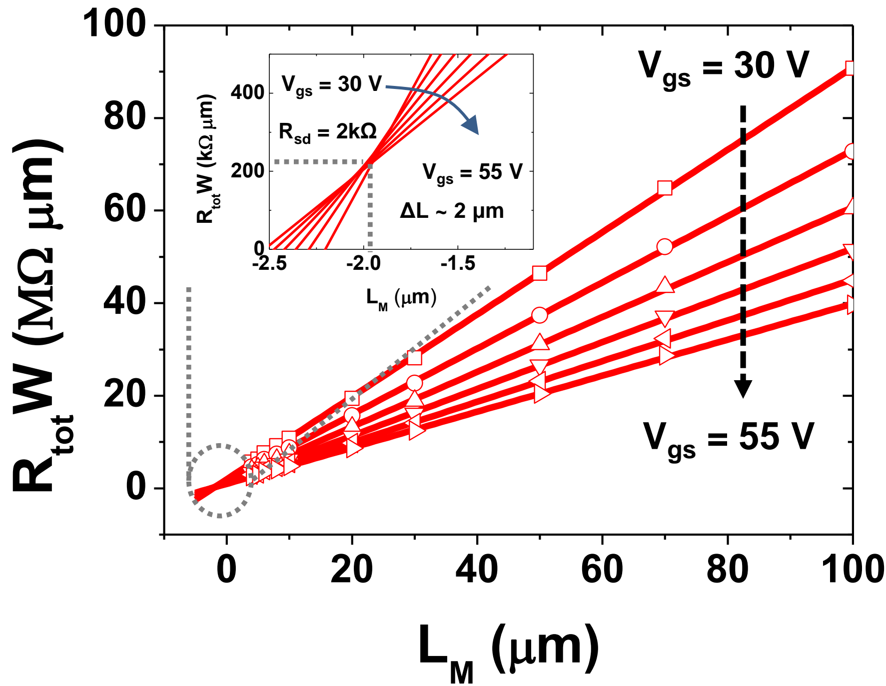

Figure 3 Plot of $R_{tot}W$ ($= R_{tot} \times W$) as a function of channel length at different V_{gs} from 30V to 55V. Inset: Series resistance (2kΩ), and the channel length variation (−2 μm).

The total resistance is defined as $R_{tot} = V_{ds} / I_d$ and it can be written as:

$$R_{tot} = R_{ch}(L_M - \Delta L) + R_{sd} \qquad (6.2)$$

with $R_{ch} = 1/(\mu_{eff} C_{ox} W(V_{gs} - V_{th}))$, where R_{ch} is the intrinsic channel resistance per unit channel length and R_{sd} is a series resistance at the source/drain contacts, ΔL is the difference between mask length L_M and L_{eff}. The width normalized total resistance $R_{tot}W$ is plotted as the function of the channel length for various gate voltages from 30V to 55V in Fig. 3. R_{sd} and ΔL were extracted as 2 kΩ and −2 μm, respectively, from the cross point of linear fits through the $R_{tot}W$ versus L for different gate voltages. The extracted value of R_{sd} is comparable to those obtained from

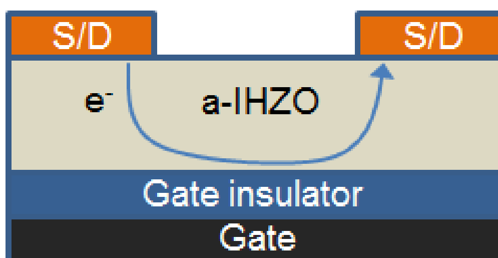

Figure 4 The illustration explaining the extension of the effective channel length

other reports on AOS TFT [16] and ΔL of negative value meaning that the increase of channel length value is also frequently observed in a-TFT since electron would rather tend to be injected at some distance from edge of S/D electrode because of imperfect edge condition of contacts (Fig. 4) [16-19].

Gate-to-channel capacitance C_{gc} versus gate-over-drive V_{gt} ($= V_{gs} - V_{th}$) characteristics of a-IHZO TFT was measured in the range of gate bias V_{gs} from 0 V to 40 V using split C-V method at the frequency of 10 kHz (Fig. 5(a)). From C_{gc}-V_{gt} results, the plot of gate-to-channel capacitance versus mask channel length for a-IHZO TFT is shown in Fig. 5(b). The measured gate-to-channel capacitance C_{gc} in strong inversion can be approximated as:

$$C_{gc} = C_{ox} W (L_M - \Delta L) \qquad (6.3)$$

where C_{ox} is the gate oxide capacitance per unit area. Hence, value of C_{ox} and ΔL, 15 nF/cm^2 and −2 μm were obtained from the slope of C_{gc} as a function of L_M and the intercept of the straight line through C_{gc} at the x-axis in the plot. The extracted ΔL value confirms the value of ΔL obtained from TLM method using the total resistance. The value of C_{ox} is in good agreement with the simple parallel plate capacitor model regarding the configuration of the device (14 nF/cm^2).

The effective mobility was also evaluated from the transfer curve and the gate-to-channel capacitance, C_{gc} (Fig. 6(a)). The effective mobility is obtained as:

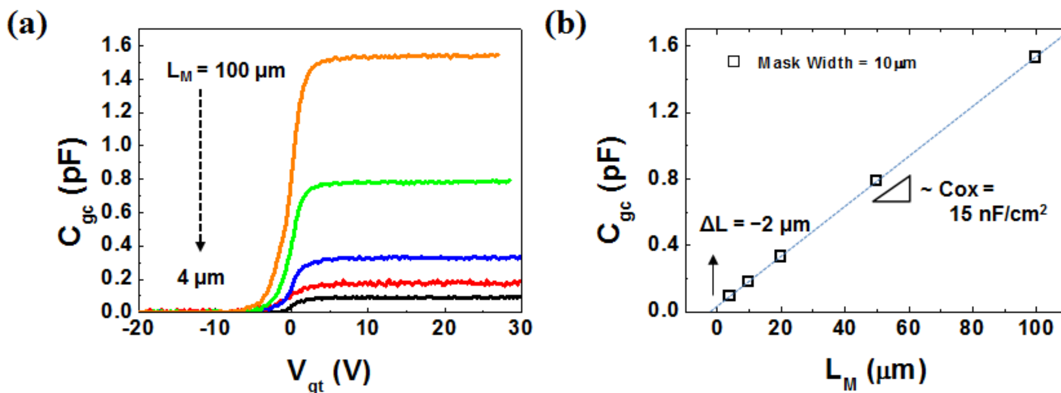

Figure 5 (a) Gate-to-channel capacitance, C_{gc} versus gate-over-drive voltage V_{gt} ($=V_{gs} - V_{th}$) measured using split C-V method for a set of a-InHfZnO TFT with different length (L_M = 4, 10, 20, 50, 100 μm, W = 100 μm), (b) TLM plot for capacitance with the gate oxide capacitance of 15 nF/cm^2 and the channel length variation of −2 μm.

$$\mu_{eff} = \frac{I_d L_{eff}}{W Q_i V_{ds}} \qquad (6.4)$$

The inversion charge Q_i per unit area is given by

$$Q_i(V_g) = \frac{1}{L_{eff} W} \int_{V_{th}}^{V_{gs}} C_{gc}(V_{gs}) dV_{gs} \qquad (6.5)$$

and approximated as

$$Q_i(V_{gs}) \approx C_{ox}(V_{gs} - V_{th}) \qquad (6.6)$$

in strong inversion. Then, the mobility extractions are either obtained using Eq. (6.4) and Eq. (6.5) or from the transfer curve using Eq. (6.1) and Eq. (6.6).

It is worth noting that the effective mobility has an increasing behavior with gate voltage as shown in Fig. 6(b). The gate bias dependence of the mobility observed in the nonlinear current-voltage behavior of amorphous semiconducting TFTs can be described with a power law: [12, 20]

$$\mu_{eff} = K(V_{gs} - V_{th})^{\alpha} \qquad (6.7)$$

In the above equation, K is a constant related to the material and α is the exponent for voltage dependence. It is believed that for a-TFT, induced charges in the channel fill the band-tail states in the energy gap. As higher gate bias is applied, the number of induced trapped charges in the band-tail states is increased and it leads to an increment of free charge carriers in conduction band as the Fermi-level approaches to the conduction band. The increase of the free carrier concentration in the conduction band is at the origin of the gate dependency of the mobility [12, 20, 21]. Based on the gate

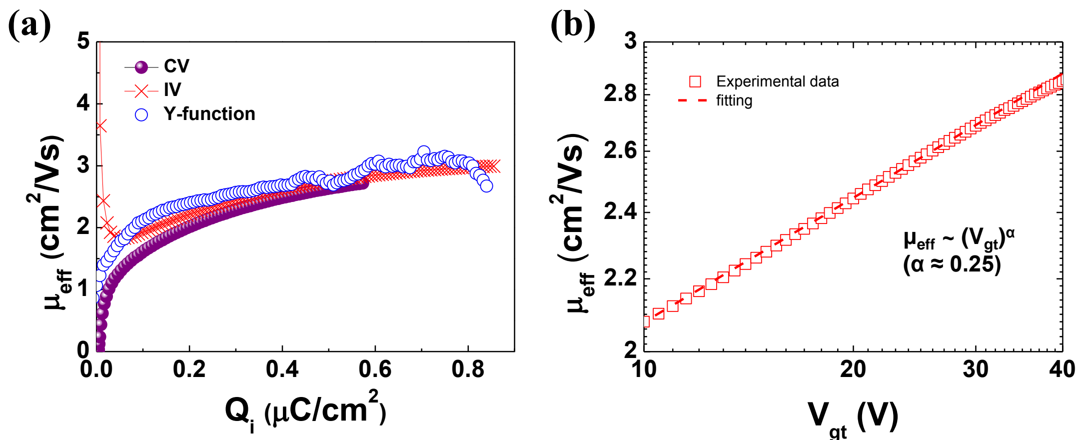

Figure 6 (a) Comparison between the effective mobility μ_{eff} directly extracted from the transfer curve (cross) and the gate-to-channel capacitance C_{gc} (solid circle), respectively, and that was obtained from the Y-function (empty circle). (b) Log-log plot of μ_{eff} vs. V_{gt} showing power law dependence of μ_{eff} .

voltage dependent mobility, Y-function was applied to a-IHZO TFT to obtain the low field effective mobility. Y-function, widely used method to extract the electrical parameter from the linear regime of crystalline Si MOSFETs, could be written as:

$$Y = (I_d^2 / g_m)^{1/n} \qquad (6.8)$$

which is linear with gate voltage above the threshold voltage and is not affected by the series resistance [22]. Usually, n has the value of 2 in Silicon MOSFET at room temperature. Substituting the Eq. (6.7) to the Eq. (6.8), n has the value of $2+\alpha$ to obtain linear Y-function with gate voltages. The effective mobility could be reconstructed from [23]:

$$\mu_{eff} = \mu_g \frac{X^{n+2}}{1+X^{n+1}} \qquad (6.9)$$

where $X = \theta(V_g - V_{th})$ is a reduced gate voltage, θ is a mobility attenuation factor and μ_g is a generalized mobility parameter related to the maximum effective mobility. As shown in Fig. 6(a), the effective mobility μ_{eff} directly extracted from the transfer curve and the gate-to-channel capacitance C_{gc}, respectively, and that obtained from Y-function give consistent values, showing that Y-function with gate voltage dependent mobility is valid for the extraction of the electrical parameters in the AOS TFTs. The divergence of mobility extracted from the transfer curve and the mobility reducing to zero using the gate-to-channel capacitance at low field are due to the inapplicability of both techniques at low inversion charge.

For a better understanding of the electronic transport in a-IHZO TFT, static characteristics of a-IHZO TFT were measured at low temperature. In Fig. 7(a), the transfer curves measured in the temperature range from 10 K to 300 K shows that the current level is not changed significantly according to the change of temperature, indicating that the conductivity of the transistor was rarely affected by temperature. The effective mobility extracted from these transfer curves also exhibited small increase with temperature (Fig. 7(b)). The mobility from the device with long channel showed larger increase than that of short channel device, which was significantly influenced by contacts. The result is far from the dramatic increase of mobility with temperature in the thermally activated hopping conduction model [24]. This observed conduction behavior is similar with the degenerate conduction in the a-IGZO TFT [25, 26] with carrier concentration over 10^{19} cm^{-3} (Fig. 8). In AOS TFT, it is well known that amorphous semiconducting channel has band-tail states in the electronic band gap due to its disordered nature [27]. Even though the Fermi level of amorphous semiconductor is located below the edge of the conduction band, if it is in the band-tail states, the semiconductor could behave like degenerated semiconductor [28]. As shown in Fig. 7(c), the threshold voltage, which is determined by the density of carriers, showed a decrease with temperature since the mobile carrier density increases with temperature.

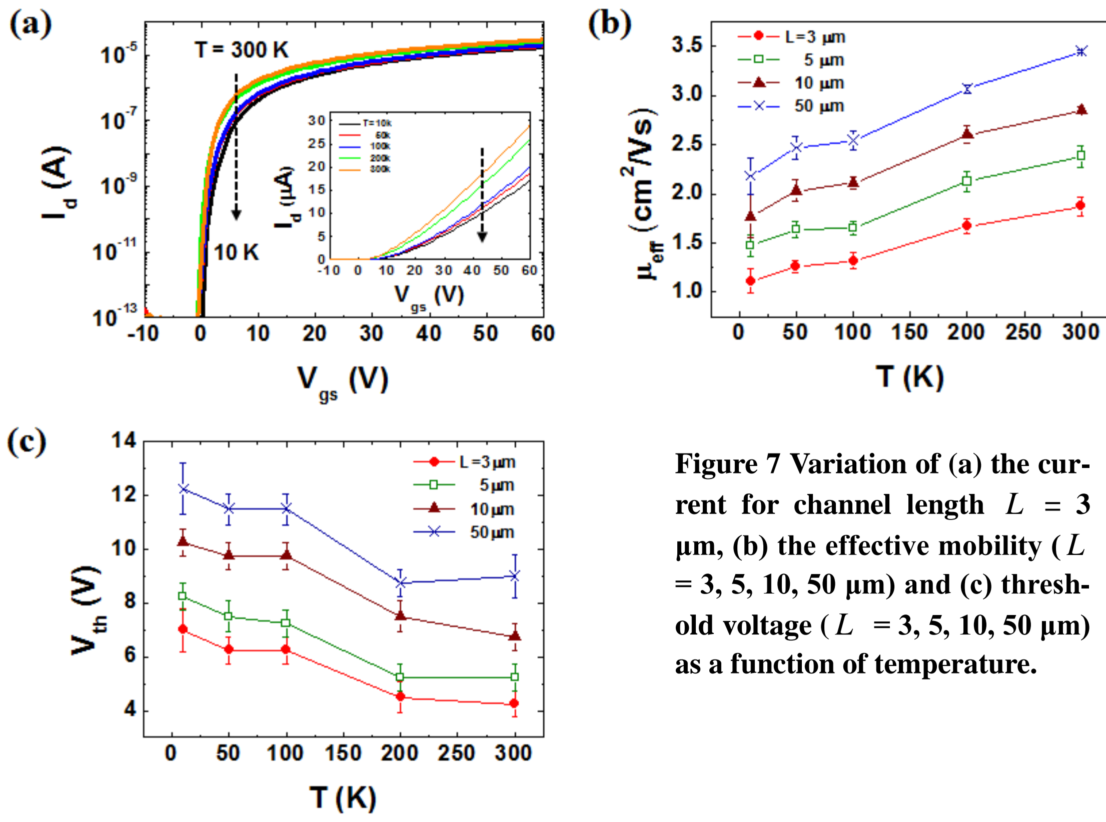

Figure 7 Variation of (a) the current for channel length L = 3 μm, (b) the effective mobility (L = 3, 5, 10, 50 μm) and (c) threshold voltage (L = 3, 5, 10, 50 μm) as a function of temperature.

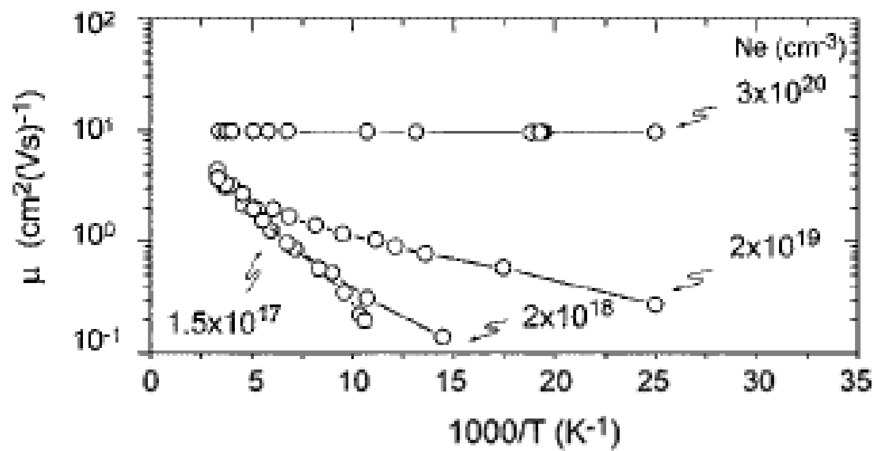

Figure 8 Temperature dependencies of Hall mobility for poly-crystalline-IGZO films with carrier concentrations range from 10^{17} to 10^{19} cm^{-3} [25].

3.2 LF Noise characteristics

The low frequency noise (LFN) was investigated in the frequency range from 10 Hz to 10 kHz at room temperature. The drain current noise power spectral density, S_{Id} with different gate voltage from 0V to 5V and drain voltage of 0.5V in the device with channel length of 3 μm are presented in Fig. 9(a). The LFN obeys $1/f^{\gamma}$ noise behavior with $\gamma = 0.7$ over the threshold voltage. There are two physical major models for 1/f noise, namely the carrier number fluctuation (CNF) model and the Hooge mobility fluctuation model. In the CNF model, the 1/f spectrum is assumed as the addition of generation-recombination (g-r) noise from traps, likely due to the presence of large number of traps in the interface between the insulator layer and the channel layer [29]. If the mobility fluctuation

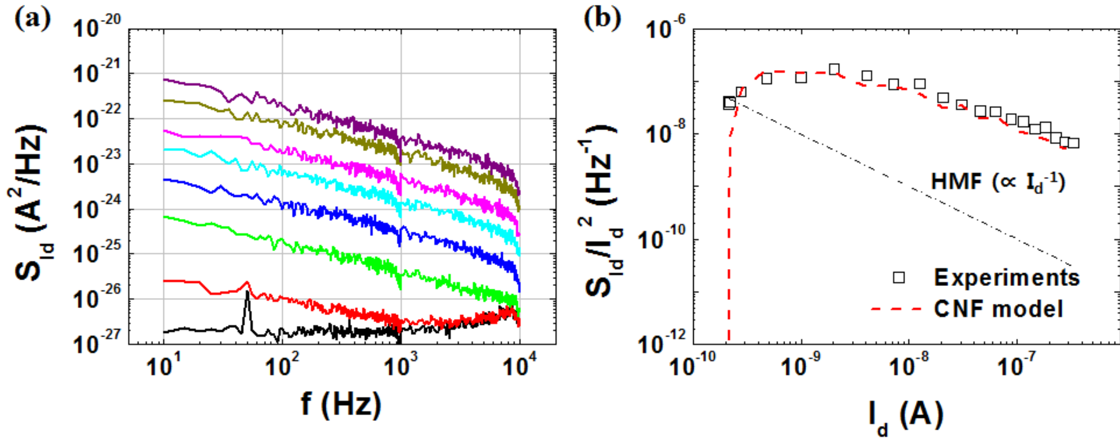

Figure 9 (a) Drain current noise power spectrum as a function of the frequency for V_{gs} ranging from 0V to 5V and V_{ds} of 0.5V in a-IHZO TFT with channel length of 3 μm and (b) noise power spectrum normalized by the drain current and carrier number fluctuation model (CNF)

is negligible, the normalized drain current noise from CNF model can be expressed by [30]

$$\frac{S_{Id}}{{I_d}^2} = S_{Vfb}\left(\frac{g_m}{I_d}\right)^2 \qquad (6.10)$$

$$S_{Vfb} = \frac{q^2 kTN_{it}}{fWLC_{ox}{}^2} \qquad (6.11)$$

where S_{Vfb} is the flat-band voltage power spectral density, g_m the transconductance, q the electronic charge, k the Boltzmann constant, T the temperature, N_t the surface oxide trap density, and W the channel width.

On the other hand, if the LF noise can be described by Hooge mobility fluctuation (HMF) due to fluc-

tuation in the individual carrier mobility contributed by phonon scattering [31], the drain current noise reads:

$$\frac{S_{Id}}{I_d^2} = \frac{q\alpha_H}{WLQ_i f} \quad (6.12)$$

where α_H is referred to as the Hooge parameter.

From Eq. (6.10) and Eq. (6.12), it is shown that the normalized drain current noise S_{Id} / I_d^2 is dependent on $(g_m / I_d)^2$ and $1/I_d$ for CNF model and HMF model, respectively. The normalized current noise is plotted as a function of the drain current I_d in log scale for the diagnosis of the dominant noise source in Fig. 9(b). The plot shows that the noise characteristics of a-IHZO TFT is well fitted by the CNF model of Eq. (6.10). Therefore, the LFN in a-IHZO TFT is stemming from the carrier trapping-detrapping at the gate oxide interface and/or in bulk traps. The trap density could be yielded with the value of 4×10^{11} cm^{-2}eV^{-1} at f = 20Hz. The extracted trap density was compared with the trap density which was extracted using the subthreshold slope at T = 300 K as:

$$S = \frac{qN_t}{C_{ox}+1} \ln(10)k \cdot 300 \quad (6.13)$$

The trap density extracted by subthreshold slope of a-IHZO TFT was in the range of 2×10^{11} – 5×10^{11} cm^{-2}eV^{-1}, which is in very good agreement with the results from our noise analysis.

3.3 Numerical simulation

Numerical simulation was carried out in order to investigate the electronic structure in a-IHZO TFT with our proposed model. For the device modeling, we consider two contributions for the charge participating to the transport: the conduction occurring in the band-tail states and the conduction in the free states above the mobility edge. The band-tail density of states (DOS) was treated with the acceptor-like exponential function which is described by,

$$g(E) = N_{TA} \exp\left[-\frac{(E_g/2 - E)}{E_{TA}} \right] \quad (6.14)$$

where N_{TA} is the maximum density of interface states, E_g the bandgap energy and E_{TA} the characteristic slope of conduction band-tail states. For simplicity, the deep-gap states of a-IHZO were not considered in this study since DOS model with a very low deep-gap state concentration showed nice fitting to the measured data for a-IGZO TFT, previously [12].

The carrier density n in the conduction band can be obtained as a function of energy E as:

$$n(E) = \sqrt{N_c N_v}\, \exp\left[-\frac{(E_g/2 - E)}{kT} \right] \qquad (6.15)$$

where N_C, N_V are the effective density of states in the valence band and the conduction band, respectively.

From the carrier density, the total charge Q_{total} as sum of the free carrier charge in the conduction band Q_i and the charge in the band-tail states Q_{TA} were evaluated and the channel capacitance C_{gc}, the transfer curve and the effective mobility were obtained subsequently. In the boundary condition, the interface-trap charge density $Q_{ss} = qN_{it}E_F$, where N_{it} is the interface trap density and E_F the Fermi level (referred to mid gap), was considered between the insulator layer and the a-IHZO semiconductor layer. The conduction in the AOS is supposed to occur in the band-tail states as

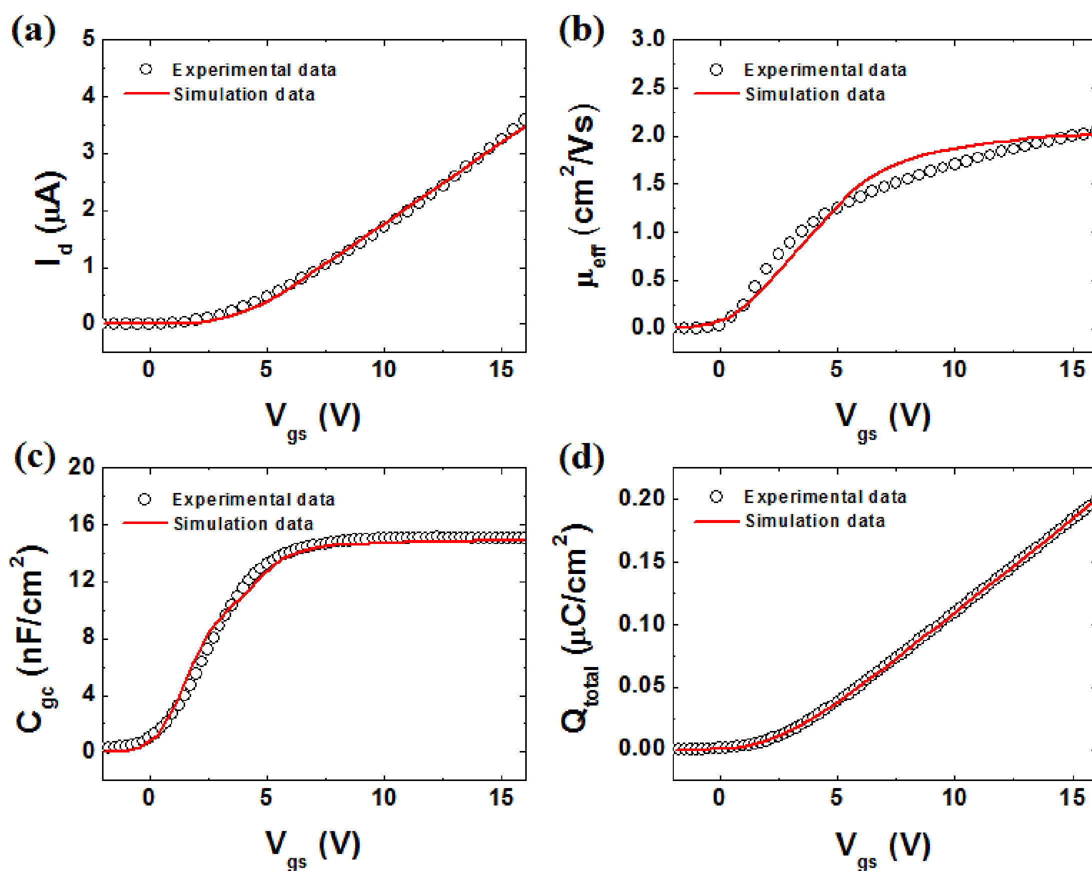

Figure 10 Measured (a) transfer characteristics, (b) effective mobility, (c) gate-to-channel capacitance and (d) inversion charge of a-IHZO TFT with the best fit using the model including the exponential band-tail structure and the interface trap states.

Table 1 Optimized parameters for the numerical simulation

Parameter	Value	Parameter	Value	Parameter	Value
N_C	10^{19} cm^{-3}	N_{it}	7×10^{10} cm^{-2}eV^{-1}	μ_{TA}	1.5 cm^2/Vs
N_V	10^{19} cm^{-3}	E_{TA}	0.3 eV	Q_{TA}	5x10^{-8} C
N_{TA}	10^{17} cm^{-3}	μ_n	2.2 cm^2/Vs	α	0.6

well as in the free states conduction band. The mobility is lower in band-tail state because the carrier conduction is limited by the potential barrier disorder [28]. Therefore, the effective mobility was modeled by the parallel transport of carriers in the conduction band and in the band-tail states, where effective mobility in band-tail states was assumed to depend on the filling degree in the band-tail states, such that:

$$\mu_{eff} = \frac{Q_i\mu_n + Q_{TA}\mu_{TA}}{Q_i + Q_{TA}} \qquad (6.16)$$

$$\mu_{TA} = \mu_{TA0}\left(\frac{Q_{TA}}{Q_{TA0}}\right)^{\alpha} \qquad (6.17)$$

where μ_n is the intrinsic mobility of free carriers in the conduction band , μ_{TA} the mobility in the band-tail states, μ_{TA0} the maximum band-tail states mobility, Q_{TA0} the maximum band-tail charge, α the constant related to the dependence of band-tail mobility on the filling ratio of band-tail states. In Fig. 10, the experimental data for a-IHZO TFTs consisting of transfer curve, mobility, the gate-to-channel capacitance, total charge are compared with the model, obtained from the simulation, including the band-tail states and interface trap density. As can be seen, the simulation results provide a good fitting of the overall experimental data and well reproduce the electrical property of a-IHZO TFT. The optimized fitting parameters are summarized in Table 1. High carrier concentration (10^{19} cm^{-3}) supports the degenerate conduction of a-IHZO TFT and the chosen trap density of 7×10^{10} cm^{-2}eV^{-1} is also comparable with the trap density extracted from LFN. For further research, scattering mechanism and electronic structure in amorphous semiconductor should be investigated and concerned in simulation model to explain low-temperature behavior of amorphous semiconductor TFT.

4 CONCLUSION

In this paper, we have investigated the electrical properties of a-InHfZnO thin film transistors using static and LFN measurements. The electrical device parameters such as the threshold voltage, the series resistance, the gate oxide capacitance and the effective mobility were extracted from the gate-to-channel capacitance $C_{gc}(V_{gs})$ as well as transfer I_d-V_{gs} characteristics. They showed reasonable value referred to previous results in AOS TFTs. The effective mobility, which shows the gate bias dependence, was compared with the effective mobility obtained from modified Y-function and the validity of Y-function on the AOS TFT was confirmed for the first time. The static characterization at low temperature showed the degenerate conduction of a-IHZO TFT with the mobility which is almost independent of temperature.

The LFN behavior of a-IHZO TFT provided strong evidences that the source of noise in a-IHZO TFT stems from the carrier number fluctuation (CNF), originated by traps in the gate oxide interface and/or in bulk traps. The trap density was also evaluated to be around $10^{11}cm^{-2}eV^{-1}$with LFN. The static characteristics of a-IHZO, including the gate bias dependent mobility, were successfully simulated with a model containing exponential band-tail states and interface traps between the insulator layer and the channel layer.

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CONCLUSIONS & PERSPECTIVE

As the minimum feature size of MOSFET is shrunk, many issues to maintain the best performance of device were highlighted while the innovation of channel material and the device architecture are investigated. With this trend of CMOS technology, the diverse need for ultra-low power consumption and new functionality shows another direction of improvement of device technology.

With these trends of CMOS technology, the dissertation covered the electrical characterization and analysis on advanced MOS devices to fulfill the need of this era such FD-SOI devices, Junctionless transistors, and amorphous-oxide-semiconductor thin film transistors (AOS TFT).

In chapter 1, the theoretical basis was focused for the understanding several concepts which is appeared following experiments. The general scaling rule and scaling effects are described in chapter 1.1 and the definition of mobility and scattering mechanisms are followed. The variation of electrical characteristic of MOSFET by several factors such as temperature, series resistance, and back bias was also summarized in this chapter. Finally, researches on conduction in AOS TFT were introduced. To observe these phenomena introduced in chapter 1, it is necessary to perform an experiment for obtaining characteristic of the device. Experimental precautions and characterization method are introduced to obtain proper characteristic of the device in chapter 2.

FD-SOI device is one of most promising candidates for future electronic device. The sidewall mobility and the series resistance were investigated in multi-channel tri-gate MOSFET. The sidewall mobility behavior with various temperature shows that the surface roughness scattering significantly influences on the sidewall conduction. The effect of surface roughness scattering was quantitatively analyzed with modified mobility degradation factor, θ_2/μ_0. θ_2/μ_0 exhibited more than 5 times and 1.25 times higher value compared with top surface mobility in tri-gate MOSFET and sidewall mobility in FinFET, respectively. It was noted that the surface roughness scattering effects is serious in sidewall mobility and it can degrades the total electrical property of extremely narrow tri-gate MOSFET. The series resistance in multi-channel tri-gate MOSFET was studied with low temperature measurement and 2-D numerical simulation. It was shown that relatively high series resistance of multi-channel tri-gate MOSFET is due to the variation of doping concentration in the source/drain extension region in the device.

In addition, it was investigated that the impact of channel width on back biasing effect in n-type MOSFET on SOI material. The variation of electrical properties, composed of transfer characteristics, gate-to-channel capacitance and effective mobility, showed suppressed back biasing effect in narrow device (W_{top_eff} = 20 nm) whereas strong influence of the back biasing V_{gb} exists in wide device (W_{top_eff} = 170 nm). The lower mobility of narrow device is attributed to the poorer channel-insulator interface quality with high-k material than that with SiO_2 dielectric at the bottom interface, and, to the

mobility degradation on the sidewall for narrow channel. The back biasing effect on electrical characteristics of tri-gate MOSFET was also successfully modeled with 2-D numerical simulation in order to physically interpret. The potential profile extracted from the simulation provides strong evidence showing that the impact of back biasing over the channel is weaker in narrow devices since the electrostatic coupling between front and back interface is smaller in narrow device with strong front gate bias control. On the other hand, the back bias significantly modulates the potential of the whole channel in wide devices.

It was followed by the investigation of the back bias effect on tri-gate junctionless transistors (JLTs) using experimental results and 2-D numerical simulations. The transfer characteristic of JLT shows more sensitive variation with back bias, presented by threshold voltage shifts. The effective mobility of JLT is significantly enhanced below flat band voltage by back bias. In extremely narrow JLTs, it was shown that the back bias effect was suppressed by reduced portion of bulk conduction and strong sidewall gates control. 2-D numerical simulation results on JLTs successfully reconstruct the trend of back bias effects and enable to analyze the back bias effect with carrier density profiles.

Finally, electrical characterization methods based on silicon devices were applied to amorphous In-HfZnO (a-IHZO) TFTs with static characteristic, low frequency noise characteristic and 2-D numerical simulation. The extraction of mobility with Y-function is adopted on a-IHZO TFT for the first time and it was confirmed by the comparison with the conventional mobility extraction method. The degenerate behavior of the conduction was shown with low temperature measurement. And from low frequency noise characteristic, carrier number fluctuation influenced by interface traps between the oxide and channel layer and/or bulk traps in a-IHZO TFT was exhibited. Based on these results, a numerical model including band-tail states conduction and interface traps was proposed and it provides a good agreement with the experimental results.

It is believed that our study provides fundamental information for the improved performance of innovative advanced MOS device including multiple-gate MOSFETs, JLTs, and AOS TFTs through the optimization of fabrication process. It also can be applied for further optimization of the device performance and for the new design of advanced MOSFET architecture.

APPENDICES

- APPENDIX 1: IMPEDANCE STUDY WITH BACTERIOPHAGE SOLUTION
- APPENDIX 2: PREAMP FOR SIMPLE MEASUREMENT
- APPENDIX 3: ZnO NANOROD GAS SENSORS
- APPENDIX 4: EXAMPLE OF FLEX-PDE SIMULATION CODE
- PUBLICATION LIST

APPENDIX 1:

Impedance study with bacteriophage solution

The filamentous bacteriophage is very interesting material due to its simple structure, easy amplification, functionality with modification, and possibility for building 1-D or 2-D nanostructures.
Electrochemical impedance spectroscopy for the conductiometric method uses a modulating AC voltage with small amplitude by sweeping the excitation frequency. Biological materials exhibit their own impedance response according to their electronic structures. Impedance spectroscopy is beneficial for investigating the electrical response of biological materials, because typical biological materials have a large electrical resistance and they are in aqueous solution with rich mobile ions.
Silicon wafers were thermally oxidized to grow 300-nm-thick field oxide for the substrate preparation. Fifty pairs of Au interdigitated electrodes (IDE) with 3-µm-width/spacing, 120 µm in length, were designed for using impedance spectroscopy to study fd phage solutions. The IDE pattern was defined

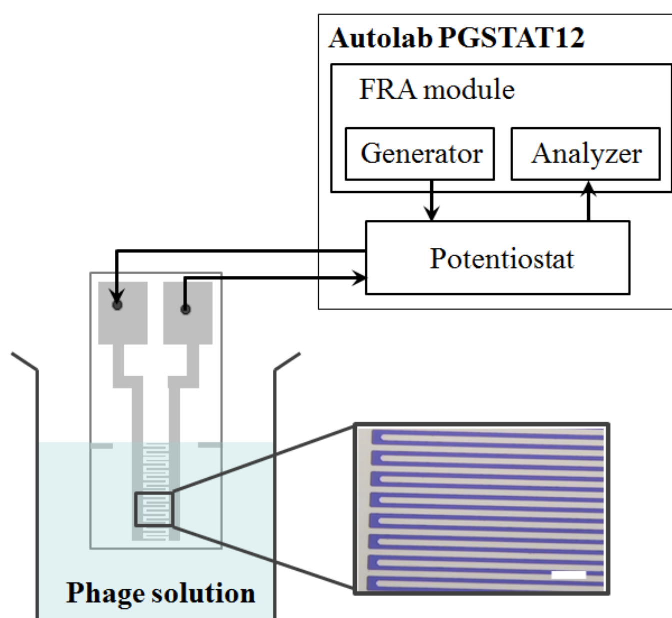

Figure 1 Experimental set-up for impedance spectroscopy, including the substrate, fd phage solution, and potentiostat with FRA modules. The electrode spacing was 3 µm and the length was 120 µm. The white scale bar in the optical microscopy image of the electrode electrode represents 10 µm. The substrate (3.5 × 7 mm) was immersed in the solution carried by a 1.5-ml tube. Impedance spectra were obtained by sweeping the frequency from 100 Hz to 1 MHz.

by standard photolithography and subsequent e-beam evaporation of a 65-nm Au layer on top of a 5-nm Cr adhesion layer on the substrate. The substrate was cut into smaller sizes of 3.5 × 7 mm because the substrate was to be immersed in a solution held in a 1.5-ml tube.

In order to prepare filamentous fd phage solution, the fd-tet phage vector and *E. coli* strain K91BluKan (K91BK) were used. The titer of the fd phage, measured with tetracycline- (20 µg/ml) and kanamycin- (100 µg/ml) resistant colony forming units (cfu), was estimated to be 1.0×10^{13} cfu/ml. Dilutions (10^{10} and 10^{12} cfu/ml) of the fd phage solution were prepared in PBS solution. As shown in Fig. 1, the electrodes patterned on the substrate were carefully positioned in a solution of 500 µl to ensure reproducible geometry. In order to observe the AC characteristics of the fd phage solution by impedance spectroscopy, an AC voltage with 10-mV amplitude was applied to the electrode while sweeping the frequency from 1 Hz to 1 MHz. The electrochemical impedance of the fd phage solution was measured by the Metrohm, AUTOLAB 12 potentiostat frequency response analysis (FRA) module and recorded using FRA software (FRA for Windows, v.4.9).

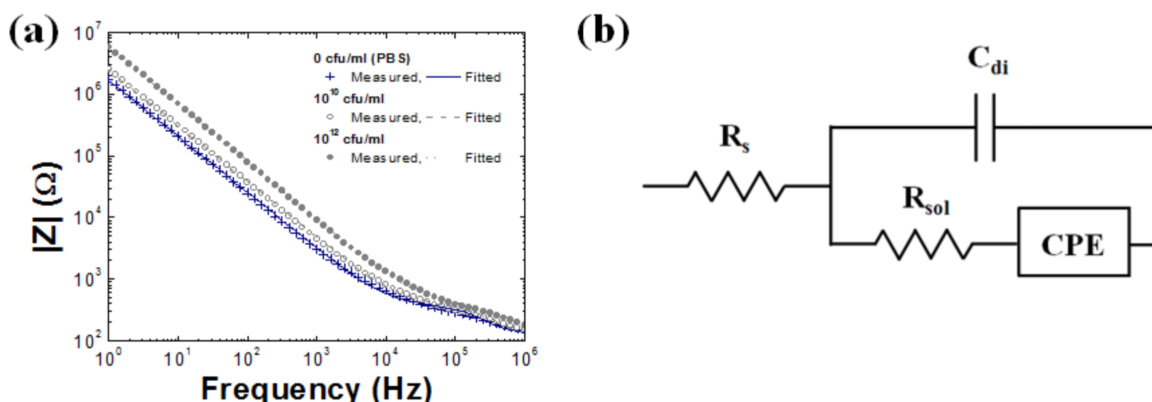

Figure 2 (a) The impedance amplitude characteristics of fd phage solution measured at room temperature and fitting measurement data to the equivalent circuit model, (b) the equivalent circuit of phage solution.

The amplitude of the impedance of the fd phage solutions are shown in Fig. 2(a). The measurement setup could be represented with an equivalent circuit (Fig. 2(b)). The equivalent circuit consisted of the series resistance, R_s, the constant phase element (CPE), the resistance of the solution, R_{sol}, and the capacitance of the solution, C_{di}. The constant phase element was associated with the double-layer capacitance including the compact inner layer (Stern layer) and outer layer (Gouy–Chapman layer) formed on the electrode surfaces with uneven microstructure of the electrodes [1, 2]. The constant phase element was expressed by the following equation:

$$Z_{CPE} = 1/(j\omega)^n B \qquad (1)$$

where ω is the angular frequency, B is the value of capacitive element, and n is a parameter related to the surface roughness of the electrodes, which ranges between 0 and 1; n values between 0.5 and 1 indicate a micron-scale rough surface on the capacitor, whereas a value of 1 reflects an ideal capacitance [1]. C_{di} represents the dielectric property of the solution; it has been reported that this mainly affects the trend of impedance responses of the solution over 100 kHz [3, 4]. Prior to the measurement, the capacitance of IDE patterns on the substrate was measured under ambient conditions with a capacitance meter (Hewlett Packard 4278A) at 1 kHz. The measured capacitance value was 169 pF and it was considered in the extraction of the equivalent circuit parameters.

For a quantitative analysis of the impedance data, the measurements were fitted to the equivalent circuit model (Fig. 2) and the equivalent circuit parameters were obtained. With the equivalent circuit, the total impedance of fd phage solution is given by

$$Z = \left(\frac{B}{R_{sol}B + 2(j\omega)^{-n}} + j\omega C_{di}\right)^{-1} \qquad (2)$$

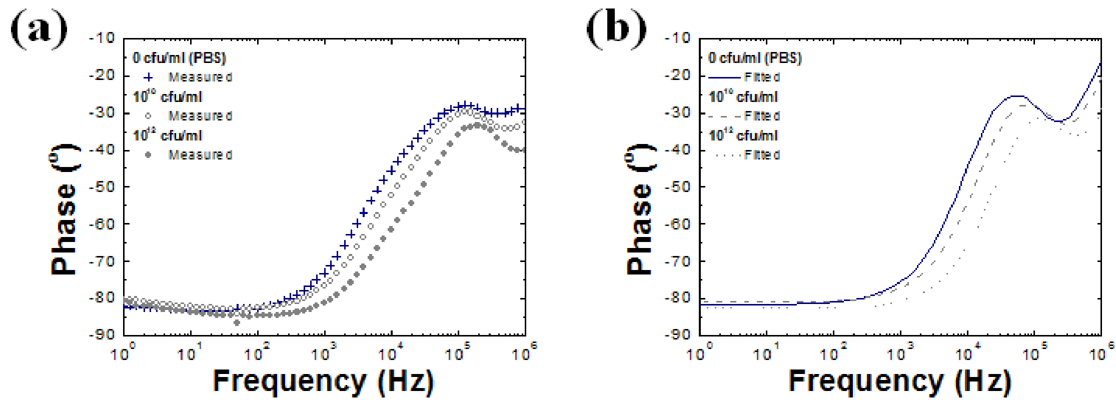

Figure 3 phases of the impedance for PBS (cross), fd phage solution of low concentration (10^{10} cfu/ml, empty circle), fd phage solution of high concentration (10^{12} cfu/ml, solid circle) in the frequency range from 100 Hz to 1 MHz.

For a more precise interpretation, the phase data were also fitted. The phase of the impedance can be readily obtained from Eq. (2):

$$\theta = \tan^{-1}\left(\frac{Z_{im}}{Z_{re}}\right) \quad (3)$$

As shown in Fig. 3, the trend of fitting results is well consistent to the measurement data. Among obtained parameters, n had a value around 0.9(0.9 – 0.91) for all samples.

Depending on the concentration of the fd phage solutions, R_{sol} and B values were extracted from the impedance data (Fig. 4). The resistance components were higher for the fd phage solution than the PBS solution. The increase of resistance in fd phage solution could be attributed to the reduced number of mobile cations in the solution due to the attraction between fd phages and cations, as

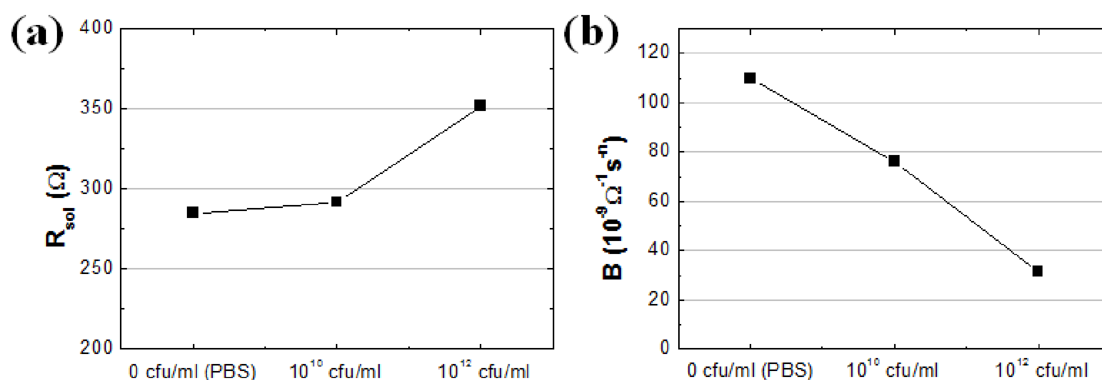

Figure 4 Extracted values of (a) R_{sol} and (b) B obtained by the best fit of the equivalent circuit.

negative charges at the surface of fd phage will capture the mobile cations.

The adsorption of ions on the fd phage body, resulting in the change of ion concentration in the electrolyte, also influences the capacitance between the electrode and fd phage solution. It is interesting to note that the increase of fd phages induces a decrease of double-layer capacitance, as shown in Fig. 4(b). The Debye length in an electrolyte is closely correlated with the ion concentration [2]:

$$L_D \propto \left(\frac{1}{c_i^{\,0}}\right)^{\frac{1}{2}} \qquad (4)$$

where L_D is the Debye length and c_i^0 is the initial local concentration of species. The Debye length of PBS with an ionic strength of 0.172 M is reported to be 0.73 nm [5, 6]. Based on this calculation, we can assume that the Debye length of the fd phage solution in this study was 2.2 nm for the higher concentration and 0.9 nm for the lower concentration. The lower value of capacitance due to the presence of fd phages is basically related to the lower ion concentration.

It was characterized that impedance for a fd phage solution depends on the concentration of phage solution. The amplitude of the impedance increased with the concentration of the fd phages. Circuit parameters were fitted to an equivalent circuit model with the values of R_s, R_{sol}, C_{di} and CPEs. The increase of R_{sol} and the decrease of the CPE value were directly related to the reduction in the number of carrier ions in fd phage solutions. The attractive interaction between positive carrier ions and the negatively charged surface of fd phage led to a reduced number of mobile ions. The current results are applicable to the detection of harmful biological materials that have a different charge amount with the proper interpretation of biological phenomena. However, a more careful approach should be developed and confirmed for sensitive decisions based on the electrochemical responses from biological materials in solution.

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APPENDIX 2:

Preamp for simple measurement

For the measurement of electrical response of phage solution, the simple measurement equipment, the program controlling the measurement was needed. The DAQ equipment (National instrument) was used to apply the DC voltage to the device and the pre-amp circuit was made for the conversion of current coming from the phage solution to voltage. The pre-amp circuit was made of differential amplifier and buffers. Low power FET-Input electrometer op-amp was used for the differential amplifier. For the control of the measurement, Labview program was built as shown in Fig. 8. In order to find proper feedback resistor in differential amplifier, PSPICE simulation was carried out. Based on this result, several feedback resistors were selected to measure various range of sample resistance. A dial switch was equipped to select measurement range on the metal box of preamp.

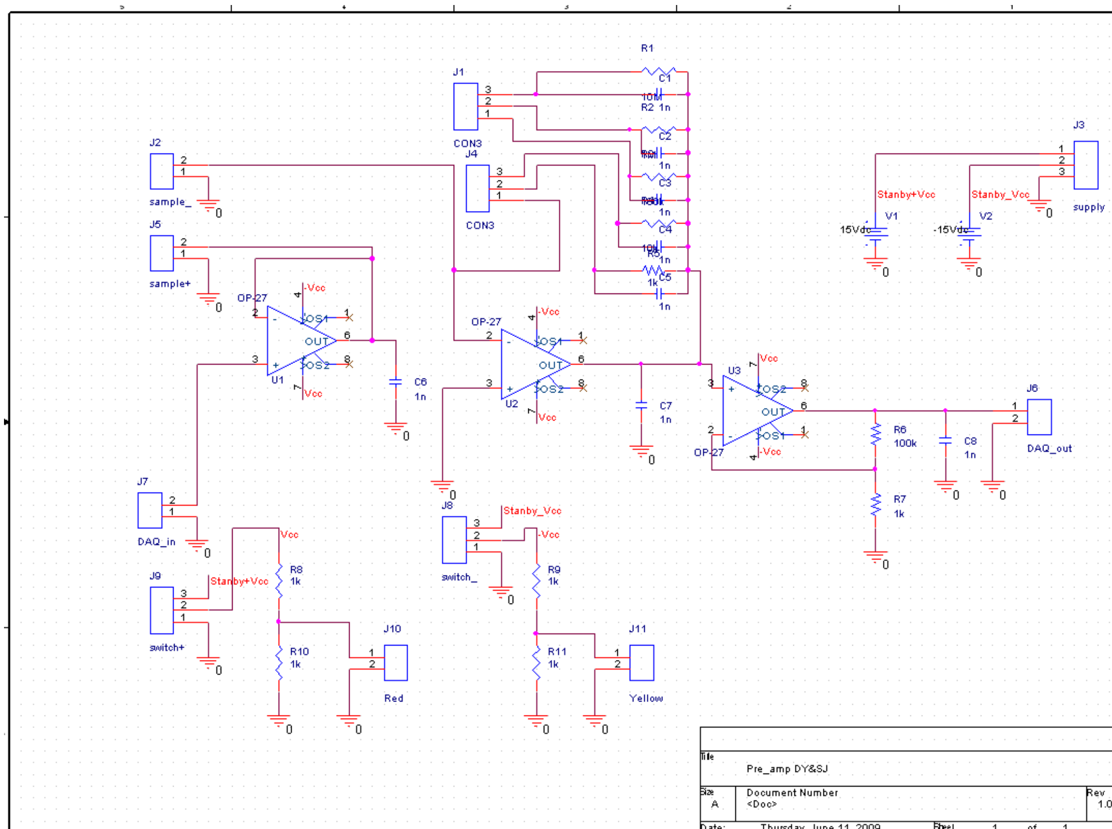


Figure 5 The PSPICE schematic of pre-amp

This composition of preamp successfully measured the resistance over 100 MΩ and it was available to measure the current with Labview program while the sweeping voltage is applied.

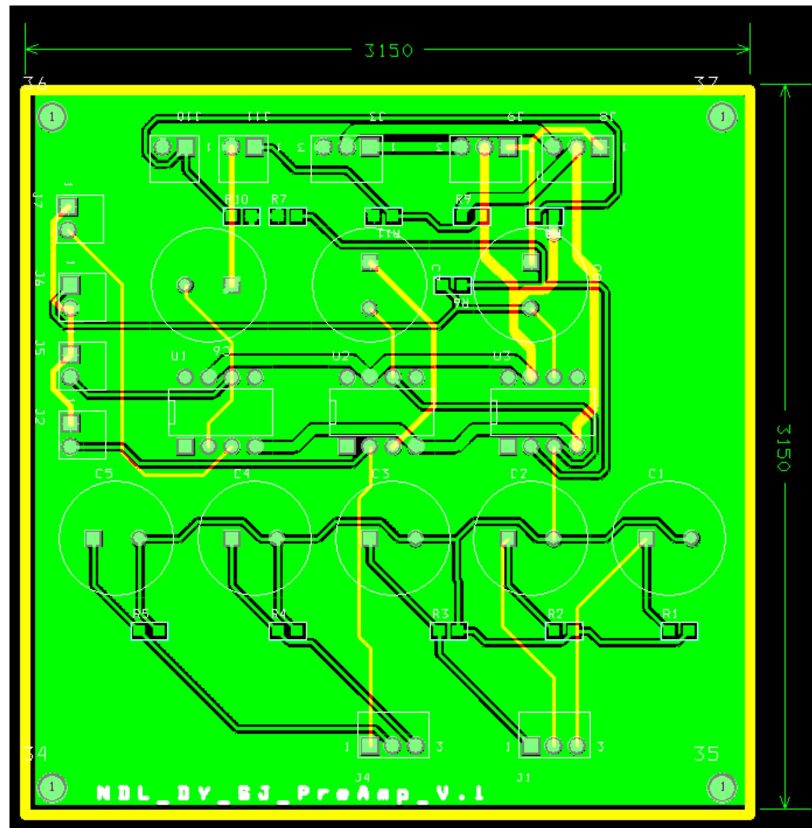


Figure 6 PCB Layout of pre-amp

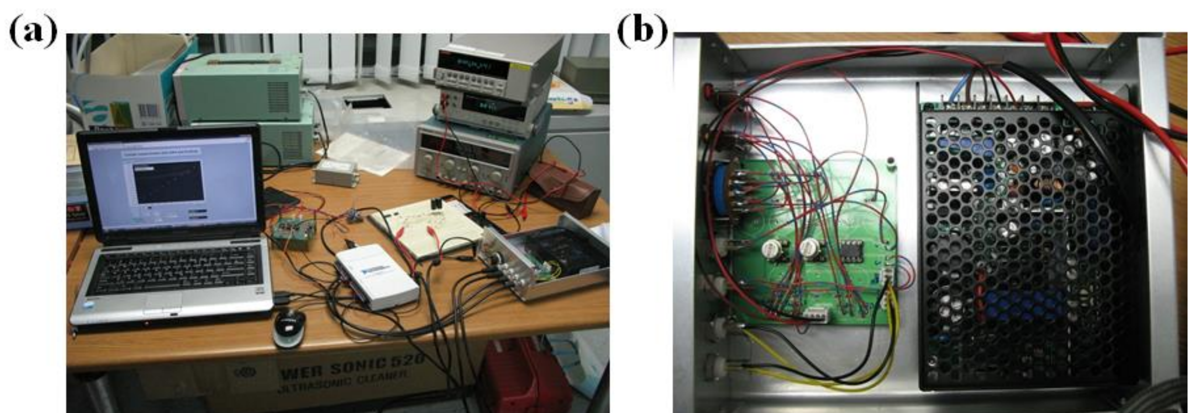


Figure 7 (a) The photograph of testing the pre-amp and (b) the composition of pre-amp metal box

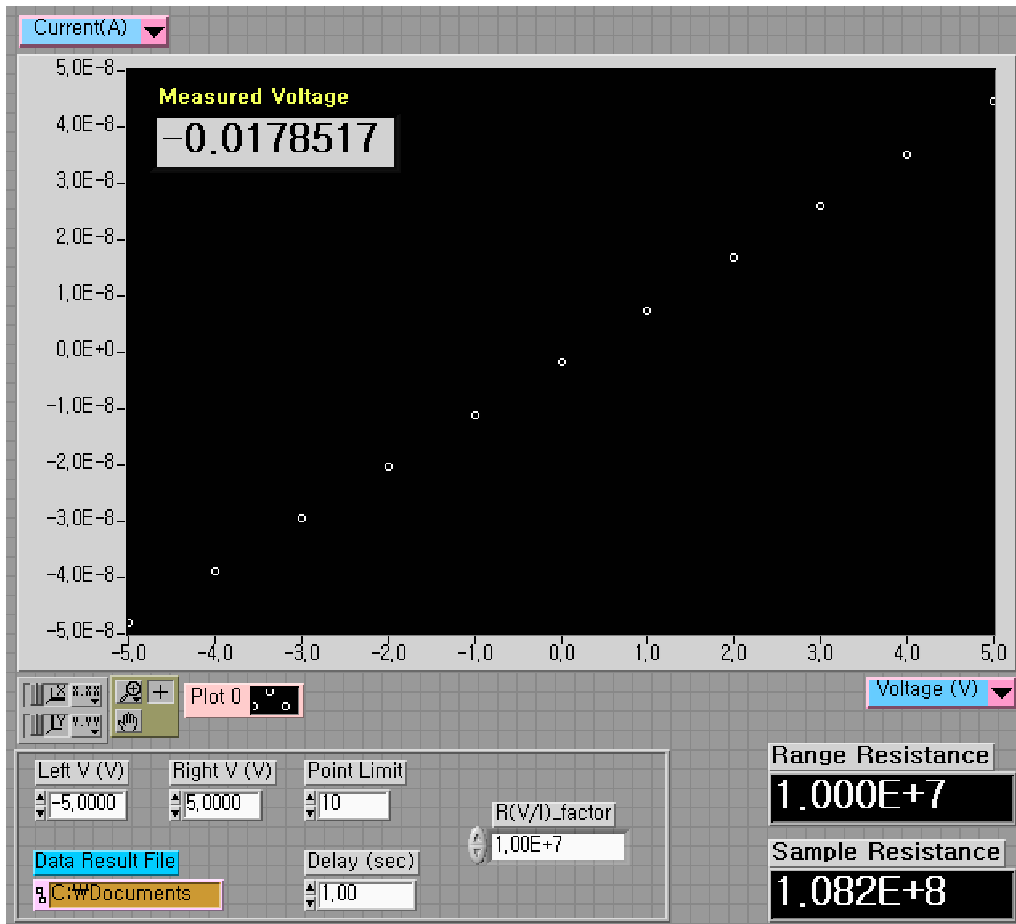


Figure 8 The Labview program for measurement; the test with test resistance of 100MΩ

APPENDIX 3:

ZnO nanorod gas sensors

Nano-structured materials have recently received great interests because of their distinct characteristics from those of bulk materials. Especially, in the field of the chemical sensor, nano-structured materials have huge potential since they show high sensitivity, good response time.
In this work, novel gas sensor using multiple ZnO nanorods was easily fabricated at the low temperature and its sensing characteristic was measured. And it was also observed that the change of the sensing properties of the gas sensor according to their ambient surroundings.
The sensing material, ZnO nanorods were synthesized by the sol–gel growth method based on aqueous solutions (Fig. 9). To obtain ZnO nanorods, 0.02 M of aqueous solution (milliQ, 18.2 MΩ) of zinc nitrate hexahydrate ($Zn(NO_3)_2 \cdot 6H_2O$) and the same concentration of aqueous solution of methenamine (HMTA, $C_6H_{12}N_4$) were prepared. These equimolar solutions were mixed and kept in the laboratory oven with immersed Si_3N_4/Si substrate at 95 ^oC for 4 hours. After the growth, the sample was rinsed immediately by deionized (D.I.) water in order to remove the residues of salts and was dried with the N_2 gas.

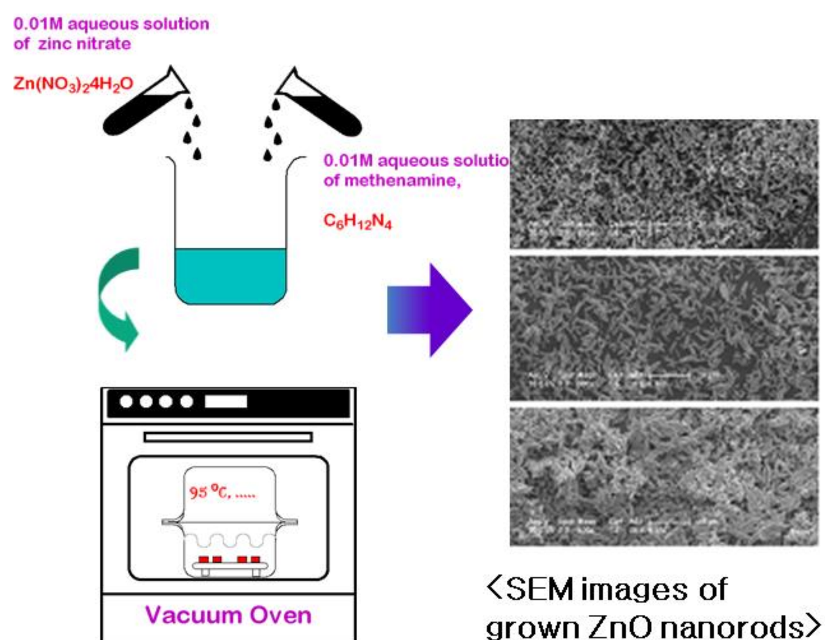


Figure 9 Sol-gel process for the growth of ZnO nanorod

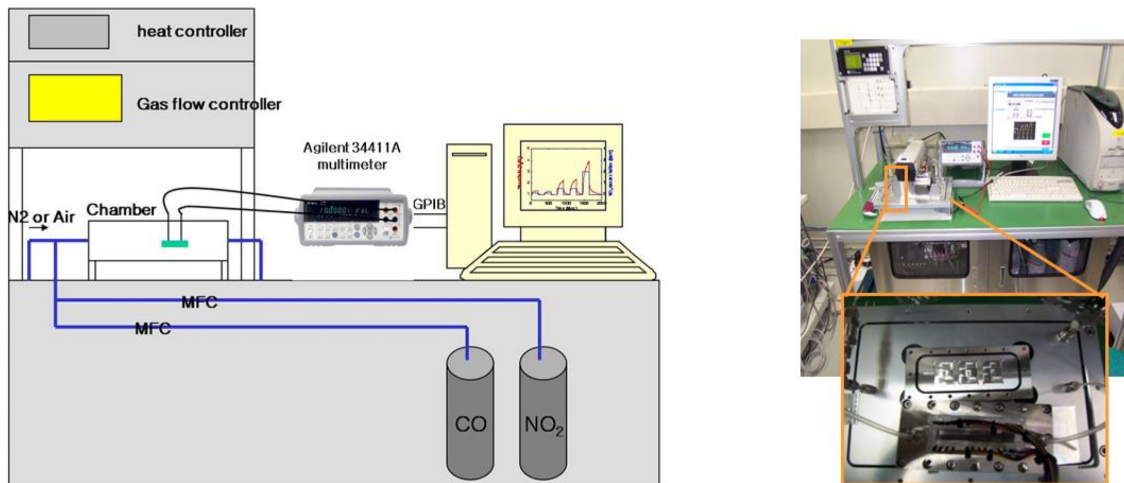


Figure 10 Gas sensing characterization system

The NO_2 gas sensing characteristic was recorded by our home-made gas reaction characterization system with samples showing the uniform resistance of several hundred MΩ. The sensor device was placed in the gas reaction chamber and was connected to the measuring equipment. The NO_2 gas was balanced with N_2 gas which has relative humidity under 4% and the concentration of target gas was controlled by the adjustment of the flow ratio between NO_2 gas and N_2 gas with mass flow controller (MFC). To supply the power to the heater the source meter (Keithley 2400) was used and the multimeter (Agilent 34411A) was employed for the measurement of the resistance of the ZnO nanorods network device (Fig. 10).

In Fig. 11 (a), the sensitivity (= $\Delta R/R_0 = (R_g - R_0)/R_0$; R_g and R_0 are values of the resistance of the sensor device when it was exposed to NO_2 gas balanced with ambient gas and to only ambient gas

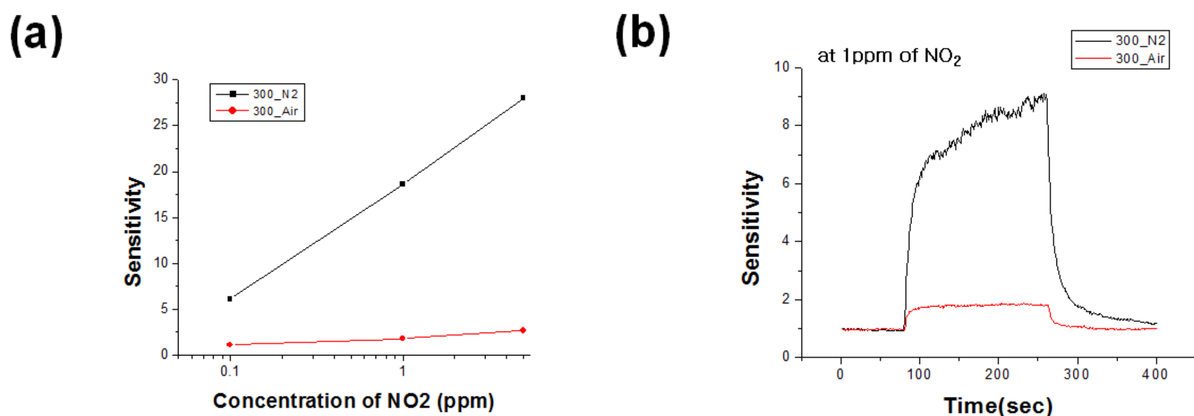


Figure 11 (a) Values of sensitivity to NO_2 gas with varying 0.1 - 5 ppm and (b) measured NO_2 gas response of the ZnO nanorods device at 300 °C

respectively.) of the device presented with varying the concentration of NO_2 gas from 0.1 ppm to 5 ppm. In the result, the resistance of the device was decreased when NO_2 gas was introduced into the gas reaction chamber. It is known that the exposure of NO_2 gas makes the resistance of ZnO decreased since NO_2 gas supplies oxygen molecules to metal oxides surface. Attached oxygen molecules on the surface of ZnO could capture free electrons existing in the ZnO .

Values of sensitivity were observed as 1.8 and 9 for air ambient and N_2 gas ambient, respectively, when NO_2 gas of 1 ppm was injected. (Fig. 11(b)) However, response time and recovery time is faster with air ambient.

APPENDIX 4:

Example of Flex-PDE simulation script

Flex-PDE program (PDE Solutions Inc.) is a finite element model builder and numerical solver with script-base. It shows data or plots as a result as Flex-PDE program solve the partial differential equation written by users with finite element system at given points (nodes). The program can solve partial differential equations in 1/2/3-dimensional Cartesian geometry and 2 dimensional cylinder geometry, sphere geometry. A number of regions can be set with different material properties according to the usage of different material in model.

(Sample script of Flex-PDE)

```
Title
        'Plate capacitor'

Variables
        u

Definitions
        Lx=1        Ly=1    delx=0.5      d=0.2          ddy=0.2*d
        Ex=-dx(u)    Ey=-dy(u)
        Eabs=sqrt(Ex**2+Ey**2)
        eps0=8.854e-12
        eps
        DEx=eps*Ex             DEy=eps*Ey
        Dabs=sqrt(DEx**2+DEy**2)
        zero=1.e-15

Equations
    div(-eps*grad(u)) = 0

Boundaries
        Region 1
                eps=eps0
                start(-Lx,-Ly)   Load(u)=0
                line to (Lx,-Ly) to (Lx,Ly) to (-LX,Ly) to close
                start(-delx/2,-d/2)            value(u)=0
                line to (delx/2,-d/2) to (delx/2,-d/2-ddy) to(-delx/2,-d/2-ddy)
        to close

                start(-delx/2,d/2+ddy)            value(u)=1
                line to (delx/2,d/2+ddy) to (delx/2,d/2) to(-delx/2,d/2)
        to close

        Region 2
                eps = 7.0*eps0
                start(-delx/2,-d/2)
                line to (delx/2,-d/2) to (delx/2,d/2) to(-delx/2,d/2)
        to close

monitors
        contour(u)

plots
        contour(u)
        surface(u)

end
```

(Commands of the script)

(1) Variables

- In this section, the definition of all the primary dependent variables is performed in a problem.

(2) Definitions:

- Definition is used to assign names and default values to the material parameters.

(3) Equations

- Equation section is used to list the partial differential equations defined with dependent variables defined in Variable section in the problem.

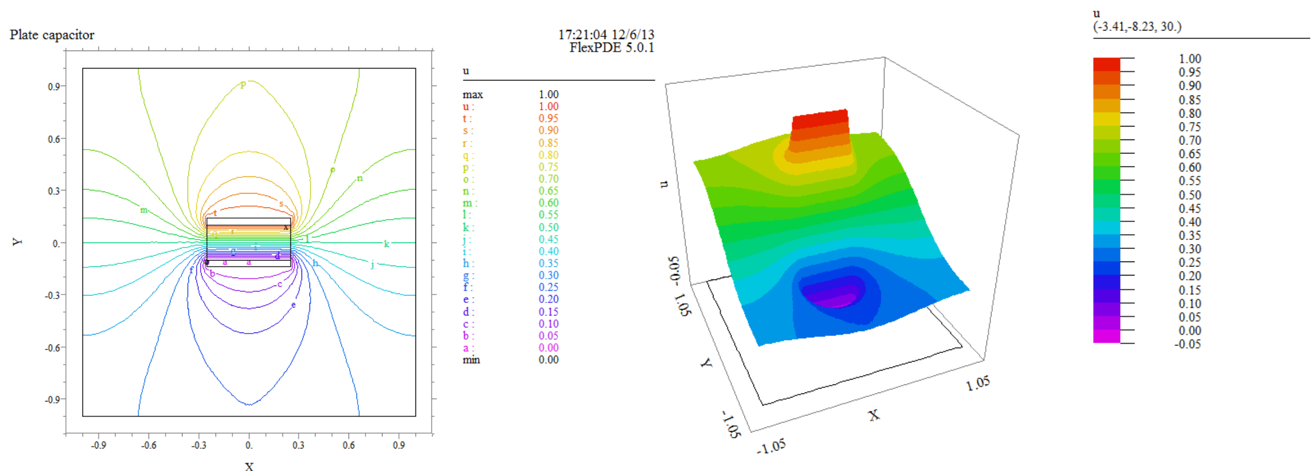
(4) Boundaries

- in this section, the boundary condition which will be used for the solving problem.

(5) Monitors and Plots

- Monitors and Plots are used for the presentation of resulting values. With Monitors, the result was shown with graphic displays at each step during solving problem. On the other hand, Plots show the results at the end of simulation.

(Results of the script)



Reference

[1] Flex-PDE 6 User Guide

Publication list

A. Journal Papers

1. **S. J. Park,** D.-Y. Jeon, Y.-J. Kim, G.-T. Kim, K. H. Hwang and C.-H. Nam, ″Sensitive detection of filamentous bacteriophage by impedance analysis″ Applied Physics Letters, submitted.

2. Dae-Young Jeon, **So Jeong Park**, Yongha Kim, Min-Ju Shin, Pil Soo Kang and Gyu-Tae Kim, ″Impedance characterization of nanogap interdigitated electrode arrays fabricated by tilted angle evaporation for electrochemical biosensor applications″ Journal of Vacuum Science and Technology B, submitted.

3. **S. J. Park,** D. Jeon, L. Montès, S. Barraud, G. Kim and G. Ghibaudo, ″Static electrical characterization and low frequency noise of a-InHfZnO thin film transistors″ Thin Solid Films, submitted.

4. **S. J. Park,** D. Jeon, L. Montès, S. Barraud, G. Kim and G. Ghibaudo, ″Impact of channel width on back biasing effect in tri-gate MOSFET″ Microelectronics Engineering, submitted.

5. D.-Y. Jeon, **S. J. Park**, M. Mouis, M. Berthomé, S. Barraud, G.-T. Kim and G. Ghibaudo , ″New method for the extraction of bulk channel mobility and flat-band voltage in junctionless transistors″ Solid-State Electronics, submitted.

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11. M.-K. Joo, J. Huh, M. Mouis, **S. J. Park**, D.-Y. Jeon, D. Jang, J.-H. Lee, G.-T. Kim and G. Ghibaudo, ″Channel access resistance effects on charge carrier mobility and low-frequency noise in a

polymethyl methacrylate passivated SnO2 nanowire field-effect transistors″, Ap-plied Physics Letters 102 (5), 053114-053114-053115 (2013).

12. D.-Y. Jeon, **S. J. Park**, M. Mouis, S. Barraud, G.-T. Kim and G. Ghibaudo, ″A new method for the extraction of flat-band voltage and doping concentration in Tri-gate Junctionless Tran-sistors″, Solid-State Electronics 81, 113-118 (2013).

13. D.-Y. Jeon, **S. J. Park**, M. Mouis, S. Barraud, G.-T. Kim and G. Ghibaudo, ″Low-frequency noise behavior of junctionless transistors compared to inversion-mode transistors″, Solid-State Electronics 81, 101-104 (2013).

14. D.-Y. Jeon, **S. J. Park**, M. Mouis, S. Barraud, G.-T. Kim and G. Ghibaudo, ″Low-temperature electrical characterization of junctionless transistors″, Solid-State Electronics 80, 135-141 (2013).

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국문초록

새로운 CMOS 기술을 위한 새로운 소자의 전기적인 특성을 측정하였다. FD-SOI 트리-게이트 인버전 소자와 정션리스 소자에서 채널의 두께가 얇아짐에 따른 측벽 전도와 시리즈 저항, 기판 바이어스 효과에 의한 전기적 특성 변화에 대한 연구를 수행하였다. 이와 함께 실리콘 소자에서 개발된 측정/분석법을 비정질 산화 금속 반도체 소자에 적용해 볼 수 있었다. 모빌리티, 문턱전압, 트랩 정보와 같은 전기적인 파라미터들을 성공적으로 얻을 수 있었고 이를 통해 비정질 산화 금속 반도체 소자에서의 전기 전도에 대한 이해를 얻을 수 있었다

먼저, 트리 게이트 인버전 모드 소자에서의 측벽 이동도와 시리즈 저항을 저온 측정과 차원 전산모사를 이용하여 연구하였다. 소자의 트랜스퍼 커브에서 얻어진 측벽 이동도로부터 측벽 이동도가 표면 거칠기 산란에 영향을 주요하게 받는 것을 알 수 있었다. 측벽 이동도에서 표면 거칠기 산란 효과를 정량적으로 평가하기 위해 수정된 이동도 저하 상수를 추출하였고 그 결과 상부 이동도보다 5 배 이상 높은 표면 거칠기 산란 효과를 확인할 수 있었다. 이와 함께 다채널 트리-게이트 소자의 시리즈 저항을 planar 소자의 경우와 비교하여 연구하였다. 2 차원 전산모사 결과를 통하여 상대적으로 높은 다채널 소자에서의 시리즈 저항이 소스/드레인 확장 영역으로부터 상대적으로 낮은 도판트 확산 정도로 인해 얻어짐을 알 수 있었다.

트리-게이트 소자에서의 기판 바이어스 효과도 채널 두께에 따라 연구하였다. 얇은 채널의 소자에서 상대적으로 높은 게이트 제어 효과로 하부채널과 상부 채널의 커플링 효과가 약해져서 문턱 전압과 이동도에 대한 기판 바이어스 효과가 작아짐을 알 수 있었다. 채널 두께가 얇은 소자에서 얻어지는 낮은 이동도는 하부 채널과 비교했을 때 상대적으로 낮은 상부 채널의 이동도와 앞에서 확인한 측벽 이동도 저하에 의한 것이다. 측벽 이동도 저하와 상부/하부 절연체 특성 차이에 의한 상부 채널의 낮은 이동도를 고려하여 차원 전산모사를 수행하였고 그 결과 채널 두께의 변화에 따른 기판 바이어스 효과 차이에 대한 주요한 근거를 얻었다.

이와 함께 정션리스 소자에서의 기판 바이어스 효과를 트리-게이트 인버전 모드 소자와 비교하여 연구하였다. 기판 바이어스를 이용한 실험 결과 정션리스 소자가 인버전 모드

소자에 비해 기판 바이어스 효과에 민감함을 알 수 있었고 플랫밴드 이하에서 정션리스 소자의 이동도가 기판 바이어스를 인가함에 따라 향상됨을 확인하였다. 이와 함께 채널 두께가 작은 정션리스 소자에서 억제된 기판 바이어스 효과를 보았다. 이러한 특성 경향들은 수치 전산모사를 통해 재현할 수 있었다.

차세대 실리콘 소자와 더불어 비정질 금속 산화물 박막 트랜지스터의 전기적인 특성 분석을 진행하면서 실리콘 소자의 분석법을 적용해 보고자 하였다. 비정질 금속 산화물은 상대적으로 저온에서도 채널 형성이 가능하므로 유연성이나 투명성을 가지는 기판에 적용될 수 있다는 장점을 가지고 있다. 하지만 비정질 금속 산화물 소자에 대한 전기적인 모델이 따로 존재하지 않아 비정질 금속 산화물 박막 트랜지스터에서의 정특성과 저주파 잡음 특성을 실리콘 소자 분석 방법을 도입하여 종합적으로 연구하였다. 이를 통해 비정질 금속 산화물 박막 트랜지스터에서 시리즈 저항, 유효 채널 길이, 모빌리티, 트랩 농도 등의 전기적인 파라미터 값들을 얻을 수 있었다. 또한 저온에서의 전도 특성 측정으로 비정질 금속 산화물 박막 트랜지스터가 도핑이 많이 된 반도체 특성을 보임을 알 수 있었고 저주파 잡음 특성 결과로부터 소자의 잡음이 전자가 소자 내 트랩에 트래핑/디트래핑 현상으로 인해 기인함을 알 수 있었다. 마지막으로 실험 측정 결과를 바탕으로 비정질 금속 산화물 박막 트랜지스터를 위한 수치 모델을 제안하였고 이 모델을 이용한 전산 모사 결과가 앞서 확인한 실험 결과와 잘 맞는 것을 확인하였다.

다수 게이트 소자에서 채널의 폭이 나노 미터 사이즈에 접근함으로써 일어날 수 있는 문제에 대해 우선 잘 알려진 실리콘 기반으로 제조된 나노 소자의 특성 연구 및 분석을 통해 논의함과 함께 실리콘 소자에서의 측정과 분석법을 실리콘 소재와 공정을 기반으로 하지 않은 새로운 소재를 이용한 소자에 이러한 분석법을 적용해 볼 수 있었다. 이러한 연구 결과는 실리콘 재료를 사용한 차세대 소자뿐 만 아니라 신소재를 이용한 소자에서의 전기적인 분석을 수행하는데 뒷받침 될 만한 정보를 준다. 또한 앞으로 차세대 소자의 성능과 집적도를 함께 높이기 위한 소자의 디자인에도 도움을 줄 것으로 예상한다.

주요어: 측벽 이동도, 다수 채널 트리-게이트 트랜지스터, 표면 거칠기 산란, 시리즈 저항, SOI (silicon on insulator), 정전기적 커플링, 기판 바이어스 효과, 채널 폭 변화, 정션리스 소자, 2차원 수치 전산모사, 비정질 금속 산화물, 박막 트랜지스터, 정특성,

전기적 파라미터 추출, 저주파 잡음.

Résumé Français

1 INTRODUCTION

Selon la feuille de route des industriels de la microélectronique (ITRS), la dimension critique minimum des MOSFET en 2026 ne devrait être que de 6 nm [1]. La miniaturisation du CMOS repose essentiellement sur deux approches, à savoir la réduction des dimensions géométriques physiques et des dimensions équivalentes. La réduction géométrique des dimensions conduit à la diminution des dimensions critiques selon la « loi » de Moore, qui définit les tendances de l'industrie des semiconducteurs. Comme la taille des dispositifs est réduite de façon importante, davantage d'efforts sont consentis pour maintenir les performances des composants en dépit des effets de canaux courts, des fluctuations induites par le nombre de dopants…. [2-4]. D'autre part, la réduction des dimensions équivalentes devient de plus en plus importante de nos jours et de nouvelles solutions pour la miniaturisation reposant sur la conception et les procédés technologiques sont nécessaires. Pour cela, des solutions nouvelles sont nécessaires, en termes de matériaux, d'architectures de composants et de technologies, afin d'atteindre les critères requis pour la faible consommation et les nouvelles fonctionnalités pour les composants futurs ("More than Moore" et "Beyond CMOS"). A titre d'exemple, les transistors à film mince (TFT) sont des dispositifs prometteurs pour les circuits électroniques flexibles et transparents.

Pour la réalisation de ces composants avancés, il est nécessaire d'investiguer leurs propriétés électriques par rapport à celles des transistors classiques afin de les optimiser. A cet effet, les paramètres physiques de ces composants doivent être évalués au moyen de méthodes d'analyse des dispositifs silicium classiques qui ont été énormément étudiés durant les décennies précédentes. De plus, le développement de modèle pour ces composants avancés et l'étude de mécanismes spécifiques gouvernant leurs propriétés doivent être menés à bien car ils sont caractérisés par des phénomènes non conventionnels et particuliers.

En 2011, parmi les dispositifs multi grilles, le MOSFET Trigate a été introduit en production de masse industrielle par INTEL, qui l'utilisera pour la technologie CMOS 22 nm. Un transistor MOS Trigate montre un excellent contrôle électrostatique du canal par la grille, ce qui réduit fortement les effets de canal courts [5,6]. Il procure un très bon contrôle pas seulement en surface du canal mais aussi sur les flancs du canal [7,8]. En raison de leur très bon contrôle de grille, ils ont moins de contrainte de dimensionnement du canal que les transistors bulk et présentent de plus grand courant de drain par unité de surface sur la plaquette de silicium [6,9].

Le transistor sans jonction (JLT) présente l'avantage de ne pas nécessiter la formation de jonctions fines pour les électrodes de source et de drain avec un profil de dopage abrupt comme le transistor à inversion. De plus, les JLT sous forme de nanofils sont compatibles avec les procédés des technologies CMOS et leur fabrication est plus simple car un seul niveau de dopage est nécessaire pour le canal et les régions de source et drain. La pente sous le seuil des JLT est excellente, à savoir 65 mV/dec à 300 K et reste proche de la valeur idéale entre 225 et 475 K [10]. La mobilité des porteurs des JLT est plus faible que celle des transistors à inversion (IM) à 300 K en raison des collisions sur les impuretés dues au dopage. Néanmoins, la diminution de mobilité dans les JLT est moins de 7 % quand la température est portée à 200 ℃, alors que pour les transistors IM celle-ci est réduite de 36 % [11]. De plus, de bons ratios Ion/Ioff, des faibles DIBL et des effets de canal court réduits ont été reportés dans la littérature pour des nanofils JLT [12,13].

Cependant, les JLT sont plus sensibles aux fluctuations de dopage que les transistors IM en raison de leur forte concentration d'impuretés dans le canal [14] comme cela est également confirmé par des simulations TCAD pour une longueur de canal de 20 nm [15]. De plus, Rios et al ont reporté que les JLT montrait davantage de dégradation de contrôle de grille et d'effet canal court ainsi que des courants Ioff supérieurs pour des dopages trop faibles de canal [16].

Un autre candidat pour les technologies MOS avancées est le transistor TFT à base d'oxyde amorphe de semiconducteur (AOS), qui présente un grand intérêt pour les applications pour afficheurs flexibles ou plats, les capteurs optiques, les cellules solaires, les composants pour l'électroniques flexible ou transparente car il peut être fabriqué sur des substrats plastiques à basses températures [17,18]. Il peut être aussi utilisé pour les afficheurs de grande surface et à bas coût [19].

Néanmoins des problèmes de stabilité et de fiabilité des TFT/AOS ont été largement étudiés dans la littérarture avec notamment le role des états d'interface. C'est pourquoi les mesures de bruit basse fréquence dans les TFT/AOS peuvent fournir une information très utile pour la caractérisation des pièges dans ces dispositifs [20-22].

2 Mobilité de flanc et résistance série dans les MOSFET Trigate

Le comportement de la mobilité de flanc a été étudié dans les MOSFET multi grille. Des MOSFET de type n à inversion ont été fabriqués au LETI-CEA. Les détails des procédés de fabrication sont donnés ailleurs [23]. Les dispositifs multi grille étudiés sont des MOSFET Trigate réalisé sur des plaquettes de SOI d'orientation (100) avec 145 nm de BOX. Des structures parallèles avec 50 doigts ont été réalisées sur des plaques SOI avec 10nm de silicium non dopé (cf Fig. 1). Le canal du transistor est gravé par lithographie optique (DUV) et amincissement de résine. L'empilement de grille est composé de HfSiON/TiN/polysilicium avec une épaisseur équivalente d'oxyde de 1.2 nm. La longueur de canal a été fixée à 10μm et la largeur du canal a été variée entre 100 nm et 1 μm. Un transistor planaire de

grande largeur (10 µm) a été utilisé pour la comparaison des résistances série avec celle extraite des transistors étroits à 50 doigts (W = 250 nm et L = 10 µm). Des simulations TCAD à 2D ont été effectuées avec FLEXPDE 5.0 par la méthode des éléments finis pour modéliser la résistance série.

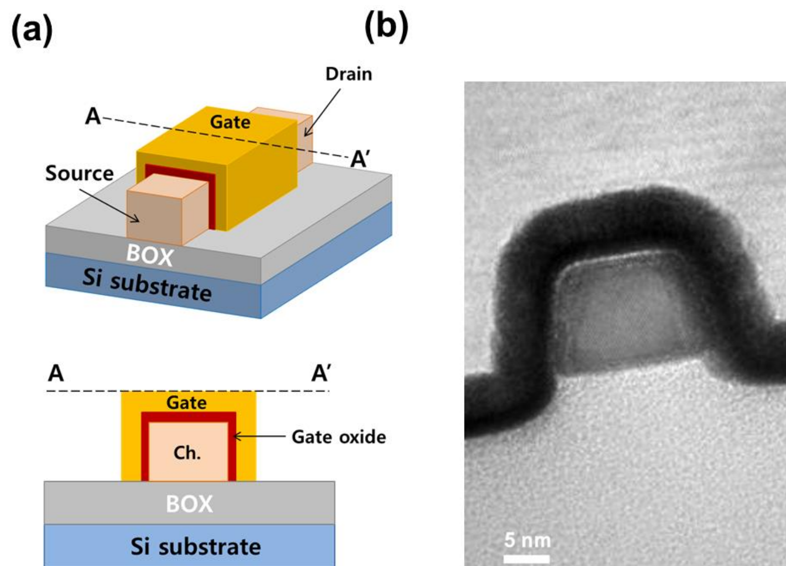

Figure 1 (a) Schéma d'un MOSFET Trigate et coupe selon l'axe AA', (b) coupe TEM d'un MOSFET Trigate.

La réduction de largeur effective de canal (ΔW) d'environ 58nm a été extraite à partir de la méthode TLM avec des mesures de capacité grille-canal de dispositifs avec différentes largeur de canal [24]. Les caractéristiques de transfert des MOSFET ont été mesurées à Vds=20mV avec un Agilent 4155A. Des mesures de caractéristiques de transfert ont également été effectuées en fonction de la température entre 77 K et 350 K avec une station cryogénique sous pointe SussMicroTec LT. La capacité grille-canal a été mesurée avec un capacimètre HP 4294A.

A partir des données obtenues à basse température, la mobilité de flanc et la mobilité de surf ace ont été extraites séparément. La mobilité de flanc a été obtenue à partir des caractéristiqu es de transfert des MOSFET Trigate avec différentes largeurs de canal. Le courant de flanc a été obtenu par extrapolation du courant drain total pour une valeur nulle de la largeur de su rface et cela pour différentes tensions de grille en forte inversion. La caractéristique de transf ert pour le dispositif avec une largeur de 1µm a été utilisée pour l'extraction de la mobilité de surface. Le courant de surface a été déduit par soustraction du courant de flanc au couran t drain total. Comme montré en Fig. 2(a) et (b), la mobilité de flanc à basse température est considérablement réduite avec l'accroissement de la charge d'inversion alors que la mobilité

de surface n'est que faiblement réduite en forte inversion. De plus, la mobilité de flanc est p lutôt indépendante de la température à très forte inversion. On peut noter que la mobilité de flanc est donc fortement affectée par les collisions sur la rugosité de surface par comparaison à la mobilité de surface dans les MOSFET Trigate [25].

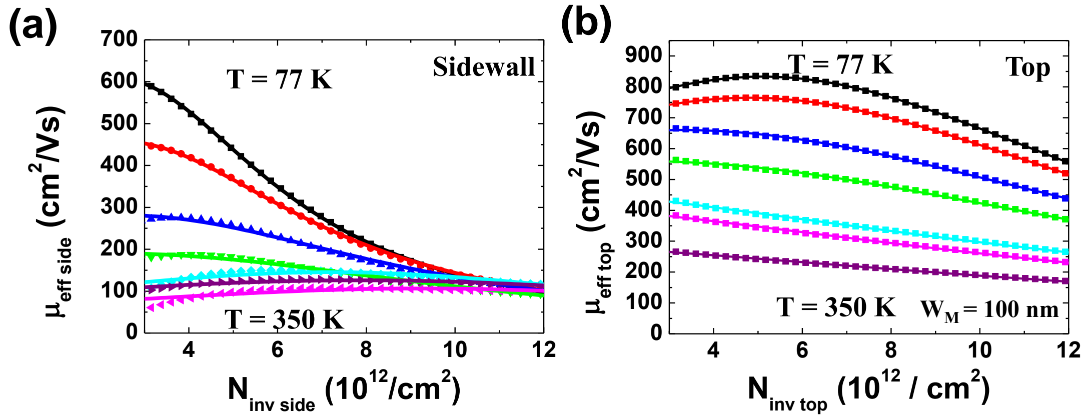

Figure 2 Variation de la mobilité effective avec la charge d'inversion pour différentes températures sur les flancs (a) et en surface (b). Les traits continus sont les meilleurs ajustements obtenus par l'équation de mobilité effective.

Afin d'évaluer l'effet des collisions sur la rugosité de surface dans la mobilité, les facteurs de dégradation de mobilité ont été extraits en utilisant l'équation de la mobilité effective [26] ;

$$\mu_{eff}(V_{GT}) = \frac{\mu_0}{1+\theta_1 V_{GT} + \theta_2 V_{GT}^2} \qquad (2.1)$$

où µ0 est la mobilité à faible champ et θ_1 and θ_2 sont les facteurs de dégradations de mobilité. Les collisions sur les phonons sont associées au facteur θ_1 et les collisions sur la rugosité de surface sont associées au facteur θ_2 [27]. La mobilité de flanc et la mobilité de surface ont été ajustées par l'équation 2.1 et les paramètres μ_0, θ_2 ont été extraits. θ_2 pour la mobilité de flanc varie entre 5.43 V^{-1} to 0.58 V^{-1} quand la température croit de 77 K jusqu'à 300 K.

Cependant, la mobilité à faible champ dépend de la température et θ_2 dépend aussi du terme de diffusion sur les phonons ainsi que ce celui sur la rugosité de surface [28,29]. C'est pourquoi c'est le facteur de dégradation normalisé à la mobilité, θ_2/μ_0, qui doit être analysé pour évaluer le rôle des collisions sur la rugosité se surface en excluant les effets de phonons. Comme indiqué sur la Fig. 3,

θ_2/μ_0 pour la mobilité de flanc est 5 fois plus grand que celui pour la mobilité de surface et est 25 % plus élevé que celui reporté pour les FinFETs [28]. Cela pourrait être dû à la formation d'une surface très rugueuse sur les flancs lors du procédé de gravure alors que la surface planaire est protégée par un masque dur lors de l'opération [30,31]. Bien qu'il soit difficile de séparer les contributions des flancs dans les MOSFET Trigate à cause de la faible hauteur du canal, il est montré que la dégradation de la mobilité de flanc pourrait être plus critique que dans le FinFETs.

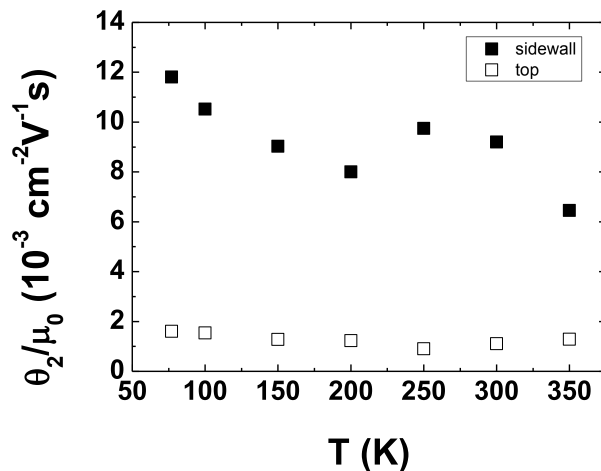

Figure 3. Variation du facteur de dégradation de mobilité normalisé θ_2/μ_0 avec la température pour le s mobilités de flanc et de surface.

Avec la conduction sur les flancs, la comparaison des résistances série entre les dispositifs planaires et multi grille Trigate a été investiguée. A cet effet, les caractéristiques de transfert ont été mesurées à 77 K sur les MOSFETs planaires et les MOSFET multi grille. La surface totale du canal ne diffère que de 5 % entre les planaires (W = 9.942 µm) et les multi grilles (W = 9.6 µm). En revanche, pour les deux dispositifs, la fonction Y(Vg) est parfaitement confondue, alors que les caractéristiques de transfert sont très différentes en termes de courant de drain.

Il est bien connu que l'effet des résistances série est éliminé sur la caractéristique de la fonction Y(Vg). C'est pourquoi on peut en déduire que la décroissance du courant drain dans les dispositifs multi grilles provient des résistances série. Afin de vérifier le comportement des résistances série, la résistance totale des dispositifs planaires et multi grille a été mesurée à différentes températures. La différence de la résistance totale entre les deux dispositifs (ΔR_{total}) correspond à la différence des résistances série entre ces deux dispositifs (ΔR_{SD}) notamment en très forte inversion.

Finalement, la résistance série des dispositifs multi grille, R_{SDM} a été estimée à partir de la différence de résistance ΔR_{SD} et de la résistance série du dispositif planaire RSDP extraite par la méthode TLM avec des transistors de différentes longueurs de canal :

$$R_{SDM} = \Delta R_{SD} + R_{SD1} \quad (2.2)$$

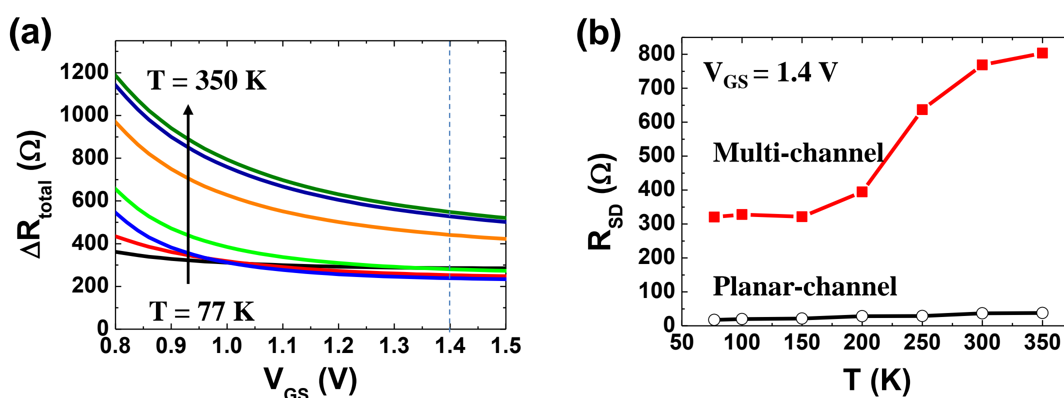

Figure 4 (a) The difference of total resistance in planar MOSFET and multi-channel MOSFET, (b) the series resistance on multi-channel device and planar device as a function of temperature.

Sur la Fig. 4(b), on voit que la résistance série des transistors multi grilles est 20 fois plus grande que celle dans les dispositifs planaires (200 Ω·µm - 400 Ω·µm). Cette variation de résistance série a déjà été reportée précédemment [32] mais cela ne peut pas expliquer la très grande différence observée ici. Des simulations TCAD 2D ont donc été entreprises pour clarifier l'origine des grandes valeurs de résistances série observées sur les transistors multi grilles. Pour la simulation, 4 paramètres ont été analysés à savoir la résistivité des régions fortement dopées de source et drain (ρ_{hdd}), la résistivité des régions d'extension (ρ_{ext}), la résistivité des siliciures (ρ_{sil}) et la longueur de l'extension entre le siliciure et le canal (L_{ext}). La résistance série a été calculée par simulation avec ces paramètres dont les valeurs ont été variées entre 10 et 100 fois leurs valeurs nominales i.e. 6.3×10^{-4} Ω·cm, 3.1×10^{-3} Ω·cm, 1.0×10^{-4} Ω·cm et 15 nm pour ρ_{hdd}, ρ_{ext}, ρ_{sil}, L_{ext}, respectivement.

Comme montré en Fig. 5(b), la valeur de la résistance série croit linéairement avec ρ_{ext} normalisé et L_{ext} normalisé par rapport à leur valeurs initiales. Cependant, des valeurs de longueur d'extension 20 fois plus grande ne sont pas praticables pour les dispositifs multi grille par rapport aux planaires. D'autre part, la résistivité des régions d'extension peut être facilement modulée par des variations de niveau de dopage lors des implantations de régions fortement dopées de source et drain. En particulier, les régions d'extension dans les dispositifs multi grille pourraient avoir des conditions de diffusion des dopants différentes dans les transistors multi grille par rapport aux planaires à cause de la plus section entre la région S/D HDD et la région de canal. C'est pourquoi l'origine de la plus grande valeur des résistances série dans les dispositifs multi grilles pourrait provenir d'une plus grande résistivité dans les régions d'extension due à une variation de la concentration de dopants. Les

méthodes pour minimiser les résistances série et leur modélisation dans les dispositifs multi grilles pourraient faire l'objet de recherche supplémentaires dans le futur.

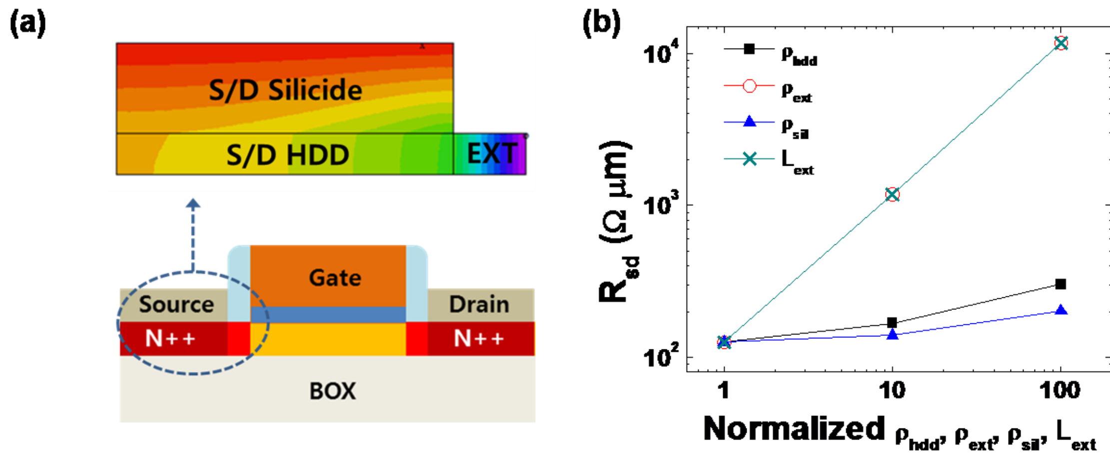

Figure 5 (a) Cartographie 2D du potentiel et schéma en coupe du transistor MOS simulé. (b) Variation de la résistance série en fonction des 4 paramètres variables.

.

3 Impact de la largeur du canal sur l'effet de polarisation arrière dans les MOSFET Trigate

L'impact de la largeur du canal sur l'effet de polarisation arrière dans les n MOSFET Trigate (Fig. 6) sur substrat isolant a été étudié.

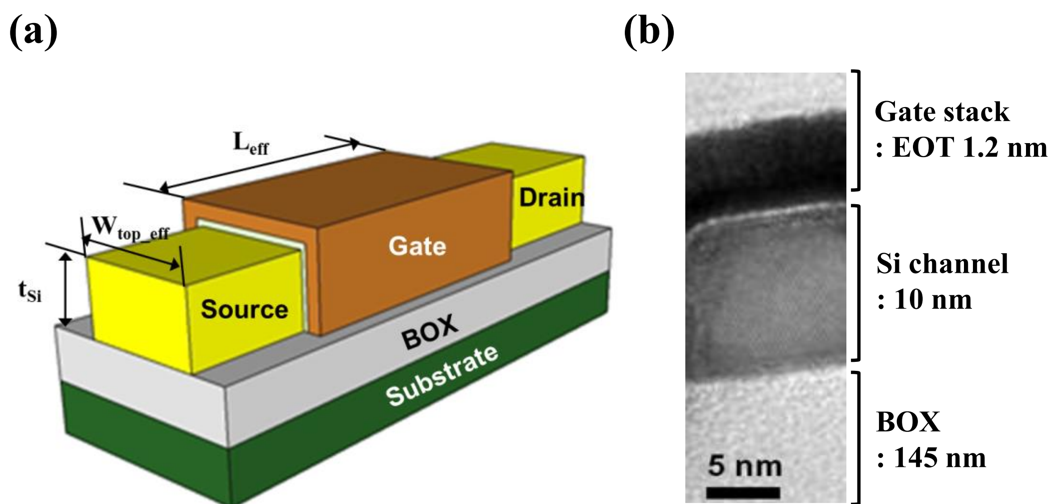

Figure 6 (a) image Schéma d'un MOSFET Trigate et (b) coupe TEM associée.

La mobilité effective a été aussi extraite à partir des caractéristiques de transfert et des capacités grille-canal sur des dispositifs à canal étroit (W = 20 nm) et à canal large (W = 170 nm) selon :

$$\mu_{eff}(V_{gs}) = \frac{L_{eff} I_{ds}}{W_{eff} Q_i(V_{gs}) V_{ds}} \qquad (3.1a)$$

$$Q_i(V_{gs}) = \int_{-\infty}^{V_{gs}} \frac{C_{gc}(V_{gs})}{W_{eff} L_{eff}} dV_{gs} \qquad (3.1b)$$

Où Qi est la charge d'inversion (C/cm2). Comme indiqué en Fig. 7, la mobilité effective pour un dispositif planaire est significativement décalée par la polarisation arrière variant entre –30 V et 30 V, alors que celle pour un dispositif étroit ne montre qu'un faible décalage ace la polarisation arrière.
Le comportement de la mobilité effective montre que l'effet de polarisation arrière est plus prononcé dans les dispositifs larges que dans les dispositifs étroits. De plus, il est bon de noter que la mobilité effective maximum est plus petite pour les dispositifs étroits. Cela peut être attribué à la plus forte contribution de la mobilité de flanc dans les dispositifs étroits.

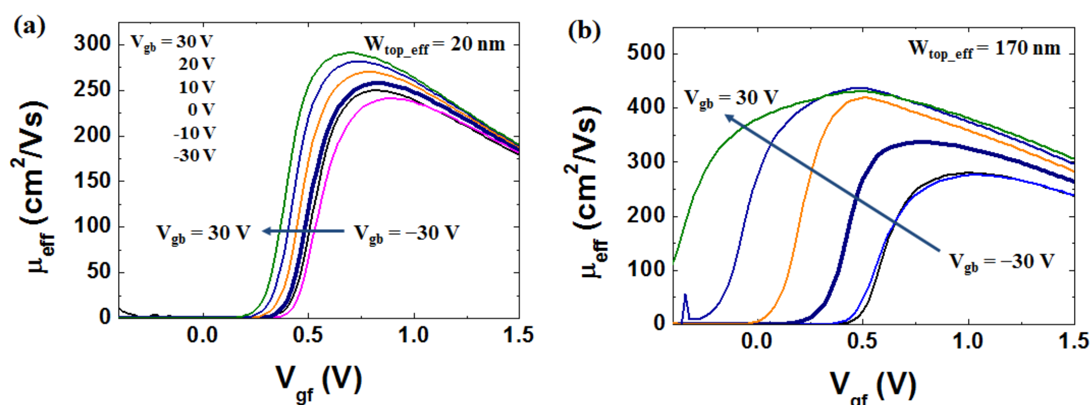

Figure 7 Variation avec Vgf de la mobilité effective pour un transistor Trigate de largeur (a) W=20nm et (b) W=170nm pour différentes polarisations arrières variant entre –30 V to 30 V. Le décalage avec la polarisation arrière de la mobilité effective pour les dispositifs étroits est significativement supprimé. La mobilité effective à Vgb=0V est tracée en trait gras

En fait, il est à noter que le diélectrique de grille high-k a une interface de moins bonne qualité que l'oxyde thermique du BOX et donc présente moins de défauts chargés, ce qui diminue les collisions coulombiennes à longue portée [33].

C'est pourquoi la mobilité à l'interface arrière est meilleure que celle aux interfaces avant et de flancs qui ont un diélectrique de grille HfSiON. Dans les dispositifs étroits, la contribution du canal arrière est plus petite et ainsi la mobilité est principalement contrôlée par les interfaces avant et de flancs, la rendant plus faible. Même pour les dispositifs larges, la mobilité est fortement diminuée lorsque le

champ à l'interface avant est fortement polarisée, c'est-à-dire pour les Vgb << 0V. De plus, la dégradation de la mobilité, liée à la conduction sur les flancs et qui pourrait être associée aux défauts induits par les procédées de gravure et/ou à une différence d'orientation cristalline, devient plus importante dans les canaux étroits car la contribution des flancs s'accroit pour des largeurs de canal très petites [28,30,34,35].

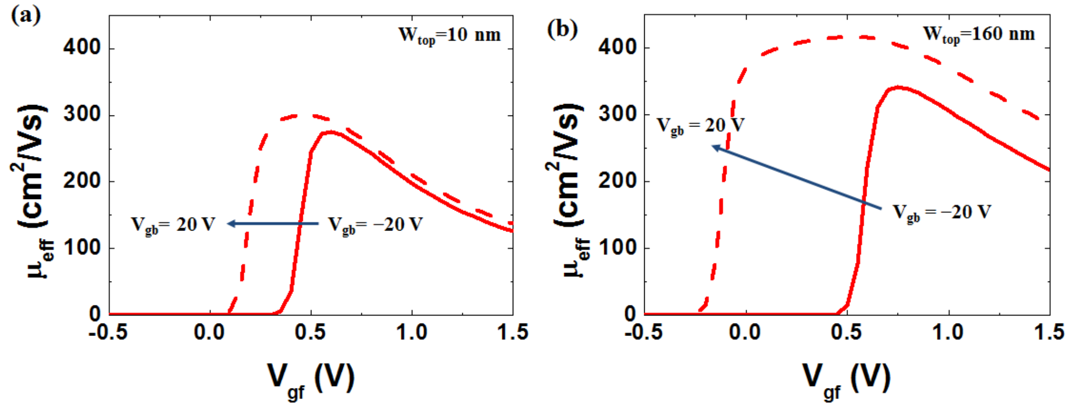

Figure 8 Variation avec Vgf de la mobilité effective simulée pour des dispositifs de largeur (a) W = 10 nm et (b) W = 160 nm pour différentes polarisation arrière V_{gb} = 20 V and V_{gb} = – 20 V.

L'influence de la polarisation arrière sur la mobilité effective des MOSFET trigate a été étudiée par simulation TCAD 2D. La mobilité effective est obtenue à partir de la mobilité locale des porteurs en fonction du champ électrique selon [36]:

$$\mu_{eff} = \frac{\mu_0}{\left(1+\left(\frac{E_x}{E_{cx}}\right)^{\alpha_x}+\left(\frac{E_y}{E_{cy}}\right)^{\alpha_y}\right)} \qquad (3.2)$$

Ou μ_0 est la mobilité à faible champ, E_x, E_y sont les champs électriques locaux selon les axes x (largeur du canal) et y (hauteur du canal), E_{cx} et E_{cy} sont les champs critiques selon les axes x et y, et α_x and α_y sont les exposants des lois de dégradation de mobilité locale avec le champ.

En raison de la différence de qualité et d'orientation entre la surface, les flancs et l'interface arrière, la mobilité à faible champ est considérée comme variable selon la hauteur dans le canal comme :

$$\mu_0 = \mu_{0back} + (\mu_{0top} - \mu_{0back}) \times \frac{y}{t_{Si}} \qquad (3.3)$$

Où μ_{0back}, μ_{0top} sont les mobilités à faible champ aux interface avant et arrière, y la coordonnée selon la hauteur.

Les résultats de simulation de la mobilité à V_{gb} = –20 V and 20 V sont donnés en Fig. 8 avec pour paramètres $E_{cx} = 5 \times 10^5$ V/cm, $E_{cy} = 10^6$ V/cm, $\alpha_x = \alpha_y = 2$. Pour W_{top} = 10 nm, μ_{0back} = 330 cm^2/Vs, μ_{0top} = 280 cm^2/Vs ont été utilisés afin de fitter les données expérimentales en considérant la dégradation de la mobilité dans les canaux étroits, alors que pour les canaux larges (W=160m), les valeurs μ_{0back} = 450 cm^2/Vs et μ_{0top} = 400 cm^2/Vs ont été utilisées. La mobilité effective pour les canaux étroits varie faiblement avec la polarisation arrière en raison du couplage électrostatique plus faible entre les interfaces avant et arrière par rapport aux dispositifs larges. Les résultats de simulation pour la mobilité effective, montrant une suppression du décalage en tension et une dégradation de mobilité dans les canaux étroits, sont en bon accord avec les résultats expérimentaux.

4 Effets de polarisation arrière dans les transistors trigate sans jonction

L'effet de polarisation arrière sur les transistors trigate sans jonction a été investigué grâce à des mesures expérimentales et des simulations TCAD 2D pour comparaison à des transistors à inversion. Des transistors trigate JLT de type n ont été fabriqués au LETI-CEA sur des plaquettes SOI (100) avec un BOX de 145nm d'épaisseur, comme celles décrites ailleurs [37,38]. Le film de silicium a une épaisseur de 9.4nm et le canal a été dopé par implantation ionique avec du phosphore en concentration de 5×10^{18} cm^{-3} [37]. Le canal du transistor est défini par lithographie optique (DUV) et amincissement de résine. L'empilement de grille est formé par du HfSiON/ TiN/ Polysilicium (EOT=1.2nm). Les transistors JLT trigate ont une longueur de canal de 10µm et des largeurs variables entre 20nm et 170nm avec des structures multi doigts (50) afin de mesurer plus précisément la capacité des canaux. Des transistors à inversion de référence ont été également fabriqués avec les mêmes structures mais n'ayant pas de dopage canal.

Les caractéristiques I-V ont été mesurées a Vd=50mV et avec une polarisation de substrat en utilisant un analyseur de paramètres électriques de type Agilent HP 4155A. Les capacités grille-canal ont été mesurées à 500kHz avec un HP 4294A selon la méthode split. Des simulations TCAD 2D ont été réalisées en éléments finis avec le logiciel FLEXPDE v5.0.

La Figure 9 (a) montre la variation de la transconductance (g_m) en fonction de la tension de grille avant V_{gf} pour différentes conditions de polarisation arrière pour les JLT à canal n (W_{top_eff} = 170 nm, L_{eff} = 10 µm). Le décalage du courant de train normalisé par la largeur effective du canal W_{eff} (=

(W_{top_eff} + 2 × t_{si}) × 50) intervient lorsque la polarisation arrière V_{gb} passe de –20 V à 20 V, comme on peut le constater dans les inserts.

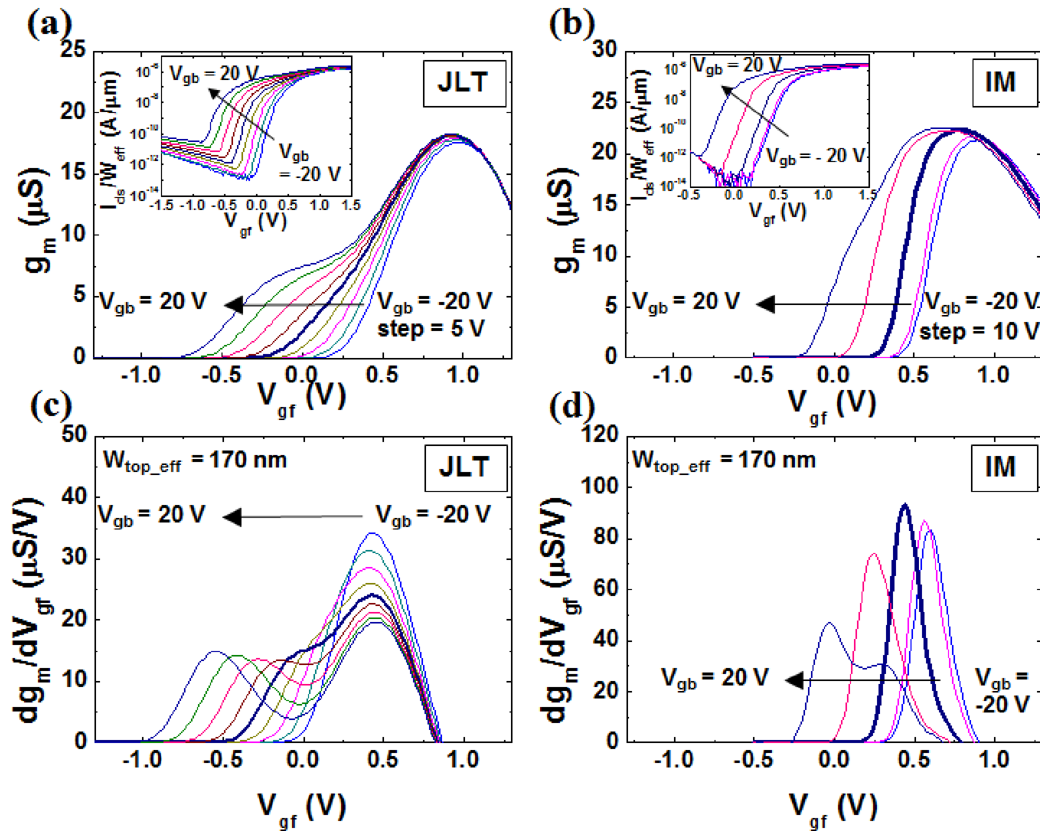

Figure 9 Courbes de transconductance mesurées pour V_{ds} = 50 mV avec des largeurs de canal supérieur effectif (W_{top_eff}) de 170 nm pour les transistors (a) JLT et (b) IM lorsque la polarisation arrière V_{gb} varie de –20 V à 20 V. Insert : courant de drain normalisé par la largeur totale effective du canal W_{eff} (= (W_{top_eff} + 2 × t_{si}) × 50). Courbes dg_m/dV_{gf} pour les transistors (c) JLT et (d) IM. La courbe en traits gras est donnée pour V_{gb} = 0 V.

Pour les JLT à canal n, au dessus de la tension seuil, une partie du canal devient neutre avec des charges de volume, et la polarisation de grille qui atteint le tension de bandes plates V_{fb} rend le canal entièrement neutre [39]. Le comportement de la transconductance dans les JLTs est différent de la tendance observée dans les transistors IM comme montré sur la Fig. 9(b), où l'on a la même géométrie que pour un JLT, du fait de l'existence de conduction de volume dans les JLT [40]. Ceci est encore plus clair sur les courbes représentant la dérivée de la transconductance, dg_m/dV_{gf} (Fig. 9(c) et (d)). Le pic additionnel pour les JLTs, qui reflète la tension seuil pour le canal neutre commence à apparaître lorsque V_{gb} = 0 V, et est décalé de manière significative par la polarisation arrière. Toutefois, les transistors IM montrent un pic additionnel dans la courbe dg_m/dV_{gf} pour les fortes polarisations arrières (V_{gb} = 20 V) du fait de la formation d'un canal d'inversion à l'arrière pour les polarisation positives [41]. On peut extraire dV_{th}/dV_{gb} pour les JLTs et les IM de 26.7 mV/V et 24 mV/V respectivement. Ceci signifie que le canal neutre volumique est plus facilement influencé par la

polarisation arrière, comparé au dispositif IM. Comme le canal volumique neutre est situé au centre du canal, la capacité effective de grille entre le canal et la grille avant est diminuée [35]. Ainsi, le contrôle par la grille est affaibli, ce qui pourrait amener à un meilleur contrôle par la polarisation arrière dans le cas des JLTs.

La mobilité effective peut être extraite :

$$\mu_{eff} = \frac{I_{ds} L_{eff}}{W_{eff} Q_i V_{ds}} \qquad (4.1a)$$

$$Q_i(V_{gf}) = \int_{-\infty}^{V_{gf}} \frac{C_{gc}(V_{gf})}{W_{eff} L_{eff}} dV_{gf} \qquad (4.1b)$$

où Q_i est la charge d'inversion par unité de surface.

La mobilité effective dans les JLT montre un accroissement remarquable de la mobilité avec la polarisation arrière, avant V_{fb} (≈ 0.5 V), due au canal neutre de volume. D'un autre côté, la mobilité des JLTs est diminuée par une polarisation arrière négative, lorsque la surface arrière du canal est désertée de manière significative.

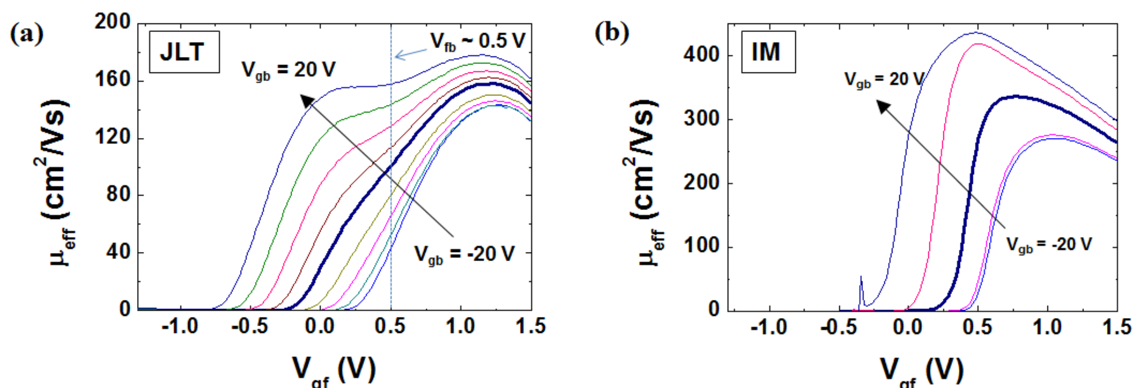

Figure 10 Courbe de mobilité effective pour des transistors (a) JLT et (b) IM avec des polarisations arrière de –20 V à 20 V. La courbe en traits gras est donnée pour V_{gb} = 0 V.

Il faut noter que la tension de bandes plates V_{fb} des transistors IM transistor est quasi-nulle, ce qui peut être attribué à la grille métallique mid-gap, et au canal Si non dopé [42]. La mobilité des électrons dans ls JLTs qui ont des charges localisée au centre de la région volumique neutre [39] est fortement dégradée par la diffusion sur les impuretés du fait du dopage important du canal [41], ce qui est confirmé par la faible valeur de la mobilité effective pour les JLTs comme montré sur la Fig. 10(a). Il est important de remarquer que la dégradation de la mobilité pour des tensions de grille avant importantes est plus restreinte, comparé aux transistors IM, ce qui s'explique par le fait que le champ électrique, qui est perpendiculaire au courant électronique, est faible dans les JLTs [43].

L'effet de la polarisation arrière sur le canal volumique est nettement diminué pour les JLT multi-canaux étroits (W_{top_eff} = 20 nm, L_{eff} = 10 μm) comme représenté sur la Fig. 11. On note aussi une

forte suppression du décalage de la transconductance sur la Fig. 11(a), ce qui montre que la portion de conduction volumique est réduite pour les JLTs de très petite dimension. Il a été montré précédemment que, lorsque la largeur du canal est réduite, un pic unique de dg_m/dV_{gf} est observé et la tension de seuil décroit du fait d'un effet plus marqué de la grille latérale et d'une plus faible portion de canal volumique neutre dans les JLTs tri-gate [44]. Sur la Fig. 11(b), un seul pic is observé dans la courbe dg_m/dV_{gf} lorsque V_{gb} = 0 V et la tension seuil qui est représentée par la position du pic dans dg_m/dV_{gf} est réduite pour les JLT étroits, par rapport aux planaires comme les JLT (Fig. 9(c)). Toutefois, le pic dans dg_m/dV_{gf} s'élargit peu à peu, en accroissant la polarisation arrière, et finalement se sépare en deux pics lorsque V_{gb} = 20 V. Ces pics séparés sont liés à l'influence de la grille arrière qui devient dominante sur la conduction. La mobilité effective dans les JLT étroits montre également des effets de polarisation arrière limités comme illustré sur la Fig. 11(c). L'accroissement de la mobilité, que l'on observe pour les dispositifs planaire Fig. 10(a), n'est pas observé mais il y a un léger accroissement global de la mobilité avec la polarisation arrière. La suppression des effets de polarisation arrière sur les dispositifs très étroits est consistante avec ce qui a été observé sur les transistors IM [7,34].

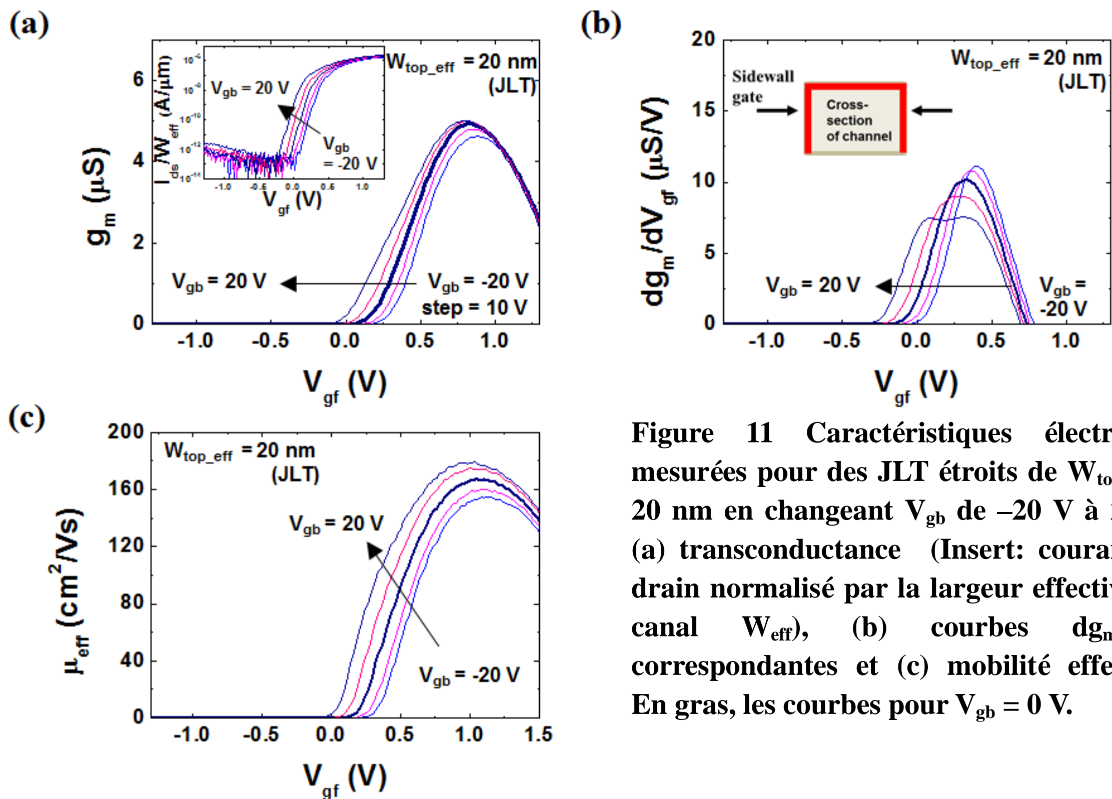

Figure 11 Caractéristiques électriques mesurées pour des JLT étroits de W_{top_eff} = 20 nm en changeant V_{gb} de –20 V à 20 V; (a) transconductance (Insert: courant de drain normalisé par la largeur effective du canal W_{eff}), (b) courbes dg_m/dV_{gf} correspondantes et (c) mobilité effective. En gras, les courbes pour V_{gb} = 0 V.

Une modélisation numérique simple, utilisant un logiciel de résolution par éléments finis (Flex PDE) a été entreprise pour étudier les effets de polarisation arrière sur les JLTs en variant le dopage du

canal et sa largeur. Pour la simulation, la mobilité effective du canal est décrite en utilisant la relation universelle entre la mobilité effective et le champ électrique transverse [36]:

$$\mu_{eff} = \frac{\mu_0}{\left(1+\left(\frac{E_x}{E_{cx}}\right)^{\alpha_x}+\left(\frac{E_y}{E_{cy}}\right)^{\alpha_y}\right)} \quad (4.2)$$

où μ_0 est le mobilité à faible champ, E_x et E_y sont les champs électriques locaux le long des axes x (direction suivant la largeur du canal) et y (direction suivant la hauteur du canal) respectivement, E_{cx} et E_{cy} sont les champ électriques critiques en x et y respectivement, α_x et α_y sont les exposants représentant la dégradation de la mobilité. Ces paramètres sont fixés à $E_{cx} = 5 \times 10^5$ V/cm, $E_{cy} = 1 \times 10^6$ V/cm, $\alpha_x = \alpha_y = 2$. E_{cx} et E_{cy} ont été pris avec différentes valeurs pour prendre en compte les effets de dispersion par la rugosité de surface sur la conduction [28, 30]. μ_0 est donné par :

$$\mu_0 = \mu_{back0} + (\mu_{top0} - \mu_{back0}) \cdot \frac{y}{t_{Si}} \quad (4.3)$$

où μ_{back0} et μ_{top0} sont les mobilité à faible champ pour l'interface arrière et l'interface avant dans le canal Si, respectivement. La dégradation de mobilité observée dans les JLTs est due aux dispersions par les impuretés.

$\mu_{back0} = 150$ cm^2/Vs et $\mu_{top0} = 120$ cm^2/Vs ont été utilisée pour $N_D = 5 \times 10^{18}$ /cm^3, tandis que pour les autres concentrations, on a pris : $\mu_{back0} = 450$ cm^2/Vs and $\mu_{top0} = 400$ cm^2/Vs. La mobilité à faible champ au niveau de l'interface arrière est considérée plus importante que celle de l'interface avant du fait de l'utilisation d'un isolant de forte constant diélectrique (de type high-k) qui ont une très mauvaise qualité d'interface, comparée à la surface arrière du canal qui est celle d'un oxyde thermique, donc de très bonne qualité [33].

La Figure 12 (a) montre la mobilité effective simulée, normalisée par leur valeur maximale à $V_{gb} = 20$ V pour plusieurs niveaux de dopage, de $N_D = 1.4 \times 10^{10}$ /cm^3 à $N_D = 5 \times 10^{18}$ /cm^3. Lorsque la concentration du canal est réduite, le dispositif montre un décalage latéral de la mobilité effective et un accroissement de la mobilité effective lorsque le dopage $N_D = 5 \times 10^{18}$ /cm^3 est à noter, ce qui avait été montré précédemment sur les caractéristiques expérimentales de la Fig. 10(a). Les Figures 12(b) et (c) montrent la mobilité effective simulée pour des dispositifs planaires comme le JLT ($W_{top_eff} = 170$ nm) et le JLT étroit ($W_{top_eff} = 20$ nm), respectivement, en fonction de V_{gf} pour $V_{gb} = 20$ V et $V_{gb} = 0$ V. Dans le cas des JLT étroits, on observe de manière très nette que la mobilité effective est moins affectée par la polarisation arrière.

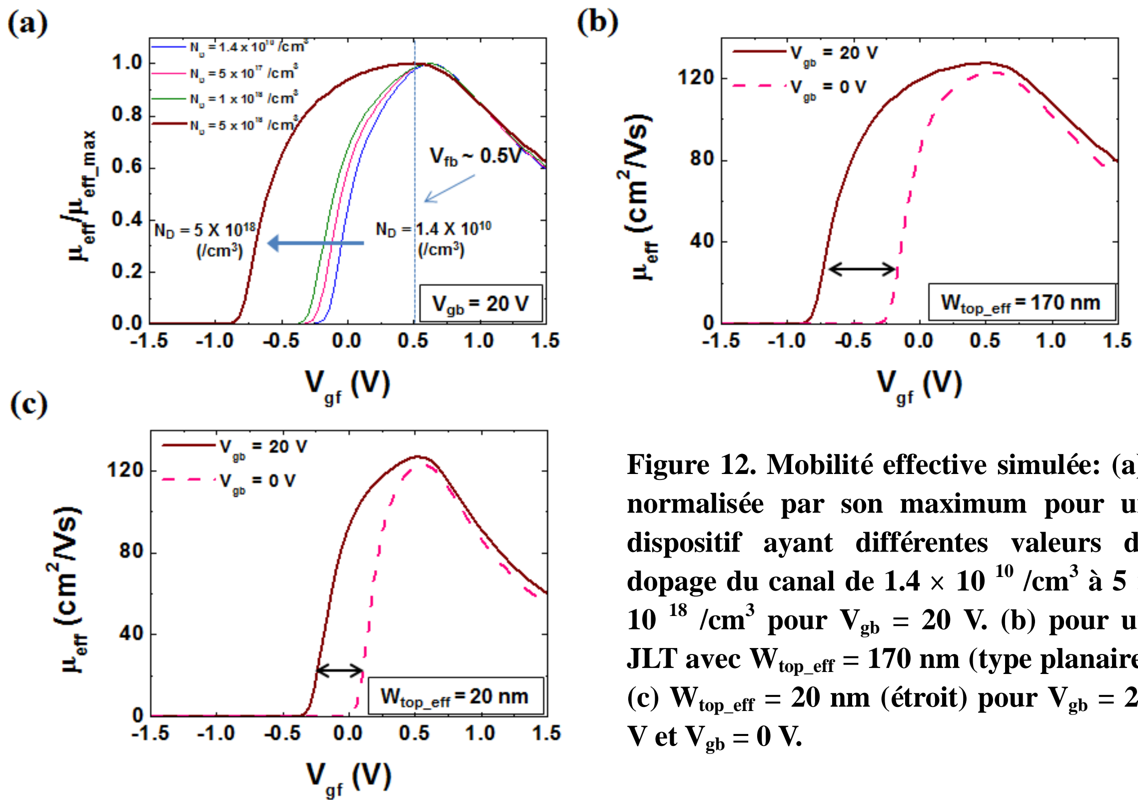

Figure 12. Mobilité effective simulée: (a), normalisée par son maximum pour un dispositif ayant différentes valeurs de dopage du canal de 1.4 × 10 ^{10} /cm^3 à 5 × 10 ^{18} /cm^3 pour V_{gb} = 20 V. (b) pour un JLT avec W_{top_eff} = 170 nm (type planaire) (c) W_{top_eff} = 20 nm (étroit) pour V_{gb} = 20 V et V_{gb} = 0 V.

5 CARACTERISATION ELECTRIQUE ET BASSE FREQUENCE DE TRANSISTOR A COUCHE MINCE en a-InHfZnO

Cette partie présente une étude complète des caractéristiques statiques et de bruit basse fréquence de transistor à film mince (TFT – Thin Film Transistor) en a-InHfZnO (IHZO) fournis par Samsung Advanced Institute of Technology (SAIT).

La Fig. 13 donne une représentation schématique de la structure du dispositif ainsi qu'une vue en coupe au microscope électronique à transmission (TEM) de ces a-IHZO TFT après le dépôt d'une couche de passivation. Ces transistors sont fabriqués avec une grille arrière étagée sur un substat de verre. Les électrodes de source/drain (S/D) et de grille sont déposées par pulvérisation avec du Molibdène puis les motifs sont crées par gravure sèche. Un dépôt chimique phase vapeur plasma (PE-CVD, Plasma- Enhanced Chemical Vapor Deposition) est réalisé à 370 °C pour créer un bicouche 350-nm Si_3N_4/50-nm SiO_x qui servira de diélectrique de grille. Ensuite, une couche servant de film mince (50-nm) actif de a-IHZO est déposé à température ambiante par une pulvérisation RF dans une atmosphère mixte Ar et O_2.

La pulvérisation est réalisée en utilisant des cibles de IHZO, obtenues à partir d'un mélange de poudres de HfO_2, In_2O_3 et ZnO, avec des compositions HfO_2:In_2O_3:ZnO = 0.1:1:1 mol %. Afin d'assurer la protection du canal des dommages engendrés par la création des contacts source/drain, un

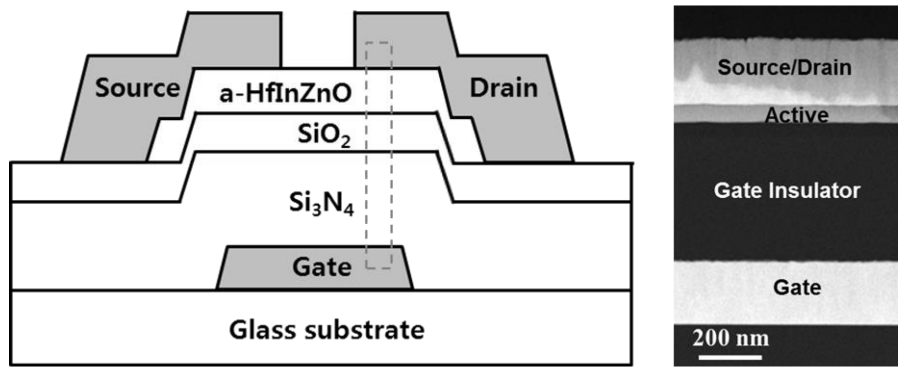

Figure 13 Vue schématique en coupe de la structure du dispositive et image TEM correspondante. On peut remarquer en particulier la bonne uniformité des couches.

dépôt PECVD d'une couche de 100 nm en SiO_x est réalisée en tant que couche d'arrêt (etch stop). In fine, une couche de passivation de 200 nm en SiO_x est déposée par PECVD. Les dispositifs sont ensuite recuits à 200 °C pendant 1 heure à l'air ambiant. Concernant leur conception, les TFTs ont une largeur fixe W = 100 µm mais plusieurs longueur de canal L_{eff} ont été dessinées sur les masques de lithographie (de 5 µm à 102 µm). L'image TEM montre une bonne homogénéité des épaisseurs et une faible rugosité des interfaces grille, isolant, canal, source/drain. Les caractéristiques courant-tension ont été obtenue à l'aide d'un analyseur Agilent 4155A. La capacité grille-canal a été extraite à partir de mesures de type 'split-CV' [45] en utilisant un impédancemètre de précision HP4284 LCR. Les mesures à basse température ont été obtenues en utilisant une station sous pointes équipée d'un cryostat à l'hélium liquide. Les caractéristiques de bruit basse fréquence (LFN) ont été réalisées dans des gammes de fréquence de 10 Hz à 10 kHz pour des tensions de drain de V_{ds} = 0.5 V.

La mobilité effective a aussi été évaluée à partir des courbes de transfert et de la capacité grille-canal, C_{gc} (Fig. 14(a)) évaluée à partir de l'équation :

$$\mu_{eff} = \frac{I_d L_{eff}}{W Q_i V_{ds}} \quad (5.1)$$

La charge d'inversion par unité de surface Q_i est donnée par :

$$Q_i(V_g) = \frac{1}{L_{eff} W} \int_{V_{th}}^{V_{gs}} C_{gc}(V_{gs}) dV_{gs} \quad (5.2)$$

et peut être appoximée en forte inversion par :

$$Q_i(V_{gs}) \approx C_{ox}(V_{gs} - V_{th}) \quad (5.3)$$

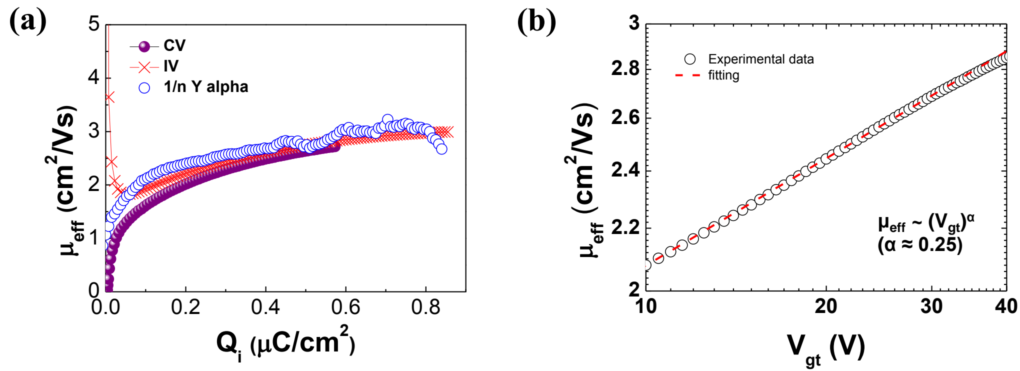

Figure 14 (a) Comparaison entre la mobilité effective μ_{eff} extradite directement à partir des caractéristiques de transfert (croix) et à partir de la capacité grille-canal C_{gc} (cercles pleins), et les extractions obtenue à partir de la function Y (cercles vides). (b) Courbe log-log de μ_{eff} vs. V_{gt} montrant la dependence en puissance de μ_{eff} .

Les extractions de mobilité sont obtenues à partir des Eq. (5.1) et Eq. (5.2), mais aussi en utilisant les caractéristiques de transfert en utilisant les Eq. (5.1) et Eq. (5.3).

Il est intéressant de noter que la mobilité effective a un rôle plus important lorsqu'on augmente la tension de grille comme illustré sur la Fig. 14(b). La dépendance de la mobilité en fonction de la tension de grille observée dans la zone nonlinéaire de la caractéristique courant-tension pour les transistors TFT avec des semiconducteurs amorphes peut être décrite par une loi en puissance de type [46, 47] :

$$\mu_{eff} = K(V_{gs} - V_{th})^{\alpha} \qquad (5.4)$$

où K est une constante qui dépend du matériau et α traduit le dépendance en tension.

Il est courant de considérer que pour les transistors de type a-TFT, les charges crées dans le canal remplissent les niveaux de queue (band-tail states) dans la bande interdite. Lorsque des tensions de grille plus importante sont appliquées, le nombre de charges piégées dans la queue de bande décroit, ce qui a pour conséquence d'accroître les porteurs libres dans la bande de conduction tandis que le niveau de Fermi se rapproche de la bande de conduction. L'augmentation des porteurs libres dans la bande de conduction est à l'origine de la dépendance en tension de grille de la mobilité [46-48]. A partir de cette dépendance, nous avons appliqué la technique d'analyse de la fonction Y sur les dispositifs a-IHZO TFT afin d'extraire la mobilité à faible champ. Cette technique est couramment utilisée pour extraire les paramètres électriques en régime linéaire dans les transistors MOSFET Si cristallins :

$$Y = (I_d^{\,2} / g_m)^{1/n} \qquad (5.5)$$

De cette façon, on a une relation linéaire avec la tension de grille au-dessus de la tension seuil, sans être affecté par les résistances séries [49]. En général, n vaut 2 pour des transistors MOSFET en silicium monocristallin, à température ambiante. En utilisant l'Eq. (6.7) dans l'Eq. (6.8), n a une valeur de $2+\alpha$ pour obtenir une relation linéaire de la fonction Y avec la tension de grille. La mobilité effective peut être retrouvée à partir de [50]:

$$\mu_{eff} = \mu_g \frac{X^{n+2}}{1+X^{n+1}} \qquad (5.6)$$

où $X = \theta(V_g - V_{th})$ est la tension de grille réduite, θ est le facteur d'atténuation de la mobilité et μ_g est le paramètre de mobilité généralisé relié aux effets de mobilité effective maximale. Comme illustré sur la Fig. 14(a), la mobilité effective μ_{eff} directement extraite de la courbe de transfert et de la capacité grille-canal C_{gc}, et celle obtenue à partir de la fonction Y donnent des valeurs similaires, ce qui démontre que la fonction Y est une méthode valide pour extraire la dépendance en tension de la mobilité pour l'extraction des paramètres électriques de transistors de type AOS TFTs.

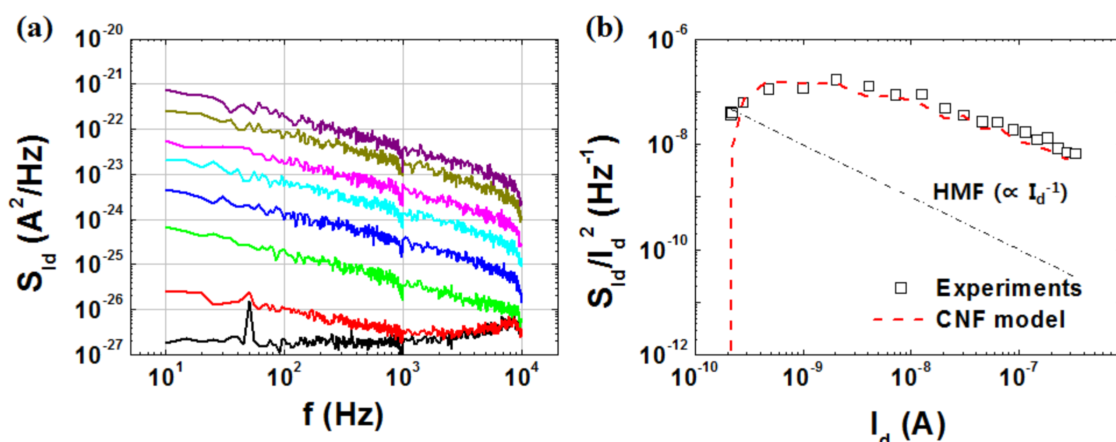

Figure 15 (a) Spectre de densité de puissance du courant de drain en function de la fréquence pour V_{gs} allant de 0V à 5V et V_{ds} = 0.5V pour des transistors a-IHZO TFT avec une longueur de canal effective de 5 µm (b) Spectre de puissance de bruit normalize en function du courant de drain et modèle de fluctuation du nombre de porteurs (CNF)

Une étude de bruit basse fréquence (LFN) a été menée à température ambiante pour des gammes de fréquence comprises entre 10 Hz et 10 kHz. La densité spectrale de bruit du courant de drain, S_{Id}, pour différentes tensions de grille de 0 à 5 V et une tension de drain de 0.5 V pour des dispositifs de longueur de canal de 5 µm sont présentés sur la Fig. 15(a). Le bruit LFN suit une loi en $1/f^{\gamma}$ avec γ = 0.7 au-delà de la tension seuil. Le bruit du courant de drain normalisé, S_{Id} / I_d^2, dépend de

$(g_m / I_d)^2$ pour le modèle de fluctuation de porteurs (CNF) et de $1/I_d$ pour le modèle de fluctuation de la mobilité, dit modèle de Hooge [51, 52]. Le bruit en courant normalisé est représenté Fig. 15(b) en fonction du courant de drain I_d en échelle logarithmique de façon à diagnostique le modèle dominant de source de bruit. Le tracé montre que les caractéristiques de bruit des transistors a-IHZO TFT peuvent être correctement ajustées par le modèle de fluctuation de porteurs (CNF). Ainsi le bruit basse fréquence dans les transistors a-IHZO TFT proviendrait du piégeage-dépiegeage des porteur à l'interface de l'oxyde de grille et/ou de pièges volumiques. La densité de ce pièges peut être estimées à des valeurs de l'ordre de 4×10^{11} cm^{-2}eV^{-1} pour une fréquence de $f = 20$Hz.

Une simulation numérique a été entreprise afin d'étudier la structure électronique des transistors en a-IHZO TFT. Pour cette modélisation du dispositif, nous avons considéré deux contributions pour les charges qui participent au transport : la conduction qui a lieu dans la queue de bande et la conduction dans les états libre au-dessus de limite de mobilité. La densité d'états (DOS) de la queue de bande a été décrite par une fonction exponentielle de type accepteur décrite par :

$$g(E) = N_{TA} \exp\left[-\frac{(E_g/2-E)}{E_{TA}}\right] \qquad (5.7)$$

où N_{TA} est la densité maximale d'états d'interface, E_g est la bande interdite, et E_{TA} est la pente caractéristique des états de queue de bande.

La densité de porteurs n dans la bande de conduction peut être obtenue en fonction de l'énergie E :

$$n(E) = \sqrt{N_c N_v}\, \exp\left[-\frac{(E_g/2-E)}{kT}\right] \qquad (5.8)$$

où N_c, N_v sont les densités d'état effectives dans la bande de valence et dans la bande de conduction respectivement.

La mobilité est plus faible dans la queue de bande car la conduction des porteurs est limitée par la barrière de potentiel du désordre [53]. Ainsi, la mobilité effective est modélisée par un transport parallèle des porteurs dans la bande de conduction et dans la queue de bande, en considérant que la mobilité effective dans la queue de bande dépend de son niveau de remplissage, de sorte que :

$$\mu_{eff} = \frac{Q_i \mu_n + Q_{TA}\mu_{TA}}{Q_i + Q_{TA}} \qquad (5.9a)$$

$$\mu_{TA} = \mu_{TA0}\left(\frac{Q_{TA}}{Q_{TA0}}\right)^{\alpha} \qquad (5.9b)$$

où μ_n est la mobilité intrinsèque des porteurs libres la dans la bande de conduction et μ_{TA} la mobilité dans la queue de bande, μ_{TA0} étant le maximum de mobilité dans la queue de bande et

Q_{TA0} le maximum de charge dans la queue de bande, α est une constante reliée à la dépendance de la mobilité dans la queue de bande au facteur de remplissage de cette queue de bande.

Sur la Fig. 16, les données expérimentales pour des transistors a-IHZO TFTs sont données, notamment la caractéristique de transfert, la mobilité, la capacité grille-canal, la charge totale, et comparés à notre modèle. Comme on peut le remarquer, les résultats de simulation donnent un bon ajustement des propriétés électrique des transistors a-IHZO TFT. Les fortes concentrations de porteurs (10^{19} cm^{-3}) supportent l'idée d'une conduction dégénérée pour les dispositifs de type a-IHZO TFT et les densités de pièges choisies pour l'ajustement qui sont de 7×10^{10} $cm^{-2}eV^{-1}$ sont aussi comparables aux densités de pièges extraites des mesures de bruit LFN. En perspective, il serait intéressant d'étudier les mécanismes de diffusion et la structure électronique du semiconducteur amorphe.

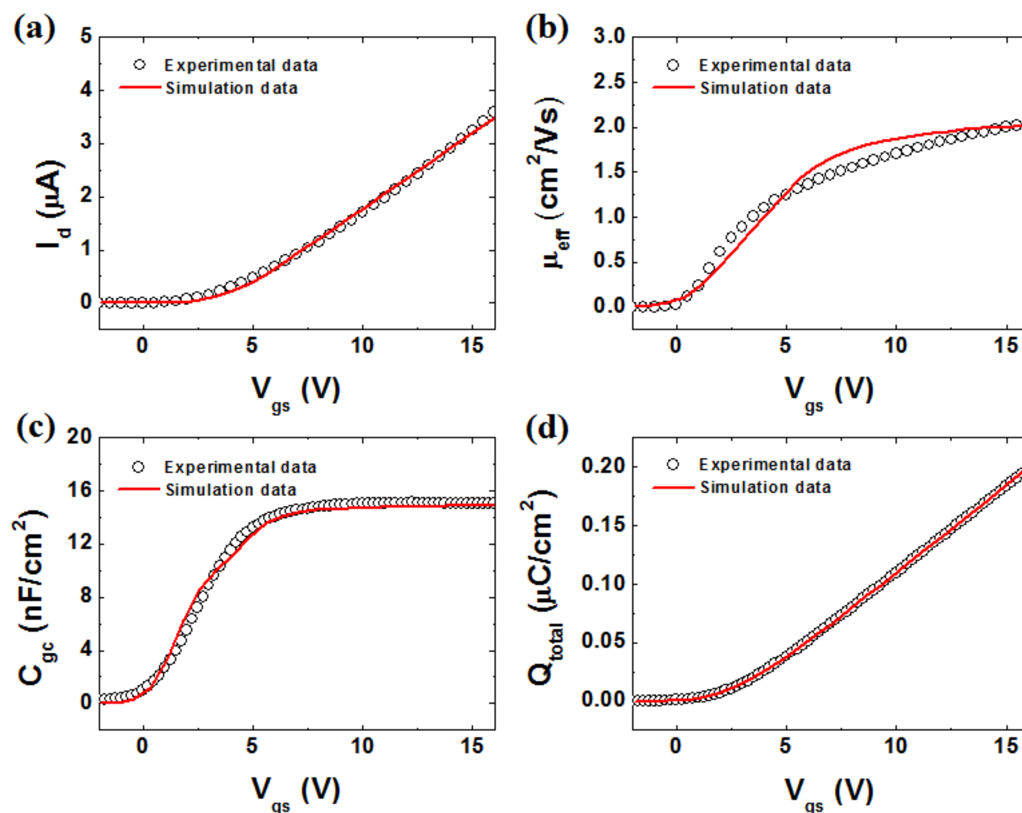

Figure 16 Mesures expérimentales de (a) la caractéristique de transfert, (b) la mobilité effective, (c) la capacité grille-canal et (d) la charge d'inversion pour les transistors a-IHZO TFT avec un ajustement du modèle incluant la structure de queue de bande des états et les pièges d'interface.

6 Conclusion et Perspectives

En réduisant les dimensions caractéristiques des MOSFET, plusieurs problèmes sont mis en évidence si l'on veut maintenir les performances des dispositifs à leur meilleur niveau de performance, tandis

que des innovations sur les matériaux du canal de conduction et sur de nouvelles architectures sont étudiés. Avec ces tendances en technologies COMS, des besoins variés en ultra-basse consommation et de nouvelles fonctionnalité, on peut entrevoir de nouvelles directions d'amélioration pour les technologies des dispositifs.

La thèse couvre la caractérisation électrique et l'analyse de dispositifs MOS avancés qui permettent de répondre au besoin de cette nouvelle ère de dispositifs, comme des transistors FD-SOI Tri-gate MOSFET, des transistors sans jonction (Junctionless, JLT), et des transistors avec un film mince d'oxyde semiconducteur amorphe (AOS TFT).

Les FD-SOI Tri-gate MOSFET figurent parmi les meilleurs candidats pour l'électronique du futur. La mobilité sur les flancs, et les résistances séries ont été étudiées. Le comportement de la mobilité avec la température montre que les effets de diffusion par la rugosité de surface influence de manière significative le conduction sur les flancs. Les effets de la diffusion par la rugosité de surface a été analysé quantitativement à partir du facteur modifié de dégradation de mobilité, θ_2/μ_0. Ce facteur θ_2/μ_0 est plus plus grand que la plus grande valeur obtenue dans le cas des mobilité de surface supérieure dans les trigate MOSFET et la mobilité des flancs dans les FinFET. Les résistances séries ont été étudiées dans le cas des tri-gate MOSFET multi-canaux, pour des basses températures, et par une simulation numérique 2D. Nous avons montré que les résistances séries relativement élevées pour ces transistors sont dues à la variation du dopage dans les zones d'extension source/drain du dispositif.

De plus, nous avons étudié l'impact de la largeur du canal sur les effets de polarisation arrière pour les MOSFET de type n sur matériau SOI. La variation de la mobilité effective montre une suppression de l'effet de polarisation arrière pour les dispositifs étroits (W_{top_eff} = 20 nm).

La faible mobilité est attribuée à la qualité médiocre de l'interface canal-isolant à forte permittivité plutôt qu'à l'interface arrière avec la silice, mais aussi à la dégradation de mobilité sur les flancs pour les canaux étroits.

L'effet de la polarisation arrière sur les caractéristiques électriques des MOSFET triple grilles ont aussi été modélisation avec succès à partir d'une modélisation numérique 2D afin de donner une interprétation physique. Une étude de l'effet de polarisation arrière des transistors JLT a aussi été menée à partir de résultats expérimentaux et de simulations numériques 2D. Les caractéristiques de transfert des JLTs montrent une sensibilité de variation plus prononcée comparé aux transistors à inversion, illustrés par des décalages de tension de seuil. La mobilité effective des JLTs est largement accrue par la polarisation arrière, en dessous de la tension de bandes plates. Pour les JLTs extrêmement étroits, nous avons montré que l'effet de polarisation arrière est supprimé du fait de la réduction de la portion de conduction volumique et du contrôle renforcé des grilles latérales. Les résultats des simulations numériques 2D sur les JLTs ont permis de rendre compte de l'influence des effets de polarisation arrière.

Enfin, des méthodes de caractérisation électrique basées sur des dispositifs en silicium ont été utilisées

avec succès pour la première fois sur des dispositifs de type transistor à film mince amorphe a-InHfZnO (a-IHZO) TFTs pour lesquels nous avons aussi étudié les caractéristiquees statiques, le bruit basse fréquence et réalisé des simulations numériques 2D. Nous avons en particulier montré la validité de la méthode d'extraction de la mobilité par la fonction Y sur des transistors a-TFT pour la première fois, en comparant notamment avec des méthodes plus conventionnelles d'extraction de la mobilité. Concernant le bruit basse-fréquence pour ces dispositifs a-TFT, nous avons montré qu'il rend compte d'une fluctuation de porteurs influencée par les pièges d'interface entre l'oxyde et le canal et/ou le volume. A partir de ces résultats expérimentaux, nous avons bâti un modèle numérique qui prend en compte la contribution des états de queue de bande et les pièges d'interface. Ce modèle rend bien compte des effets expérimentaux observés.

Cette étude a donc permis de mettre en avant des informations fondamentales pour l'amélioration des performances de transistors très innovants, incluant les MOSFETs multi-grilles, les transistors sans jonction (JLTs) et même les transistors à film mince amorphe (AOS TFTs). Cette étude peut aussi s'étendre à l'optimisation d'autres types de dispositifs, tels que des transistors multi-grilles et multi-canaux et la conception de nouvelles architectures MOSFET avancées.

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