Study and improvement of radiation hard monolithic active pixel sensors of charged particle tracking

Xiaomin Wei

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par

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Study and Improvement of Radiation Hard Monolithic Active Pixel Sensors for Charged Particle Tracking

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Résumé

Les capteurs monolithiques actifs à pixels (Monolithic Active Pixel Sensors, MAPS) sont de bons candidats pour être utilisés dans des expériences en Physique des Hautes Énergies (PHE) pour la détection des particules chargées, car ils offrent un compromis avantageux entre leur résolution spatiale, leur budget de matière, leur tolérance aux rayonnements et leur vitesse de lecture. Les MAPS sont directement exposés aux particules produites dans les expériences de PHE, y compris aux hadrons, aux leptons et à des noyaux légers. Le taux des réactions de particules traversant les MAPS se situe entre 10^6 $cm^{-2}·s^{-1}$ et 10^8 $cm^{-2}·s^{-1}$. La dose intégrée du rayonnement ionisant et la fluence du rayonnement non-ionisant peuvent varier, respectivement, de quelques dizaines de kRads à plusieurs MRads par an et de 10^{10} n_{eq}/cm^2 à 10^{15} n_{eq}/cm^2. Les MAPS, soumis à une irradiation intense dans leur l'environnement, doivent conserver leurs performances à la reconstruction de la trajectoire des particules chargées. Dans cette thèse, nous avons étudié et amélioré la tolérance des MAPS aux radiations. Les principales étapes du travail sont résumés comme suit :

1. Les effets des rayonnements sur les MAPS sont étudiés non seulement en fonction du type de rayonnement (non-ionisant et ionisant), mais prennent aussi en compte la composition des matériaux (semi-conducteur, conducteur et diélectrique) ainsi que les fonctionnalités et le câblage intégrés dans le capteur. Le rayonnement non-ionisant induit principalement des déplacements d'atomes. La dose du rayonnement dans la majorité des expériences en PHE engendre seulement des déplacements mineurs dans les conducteurs et les diélectriques, mais réduit la durée de vie des porteurs minoritaires dans les semi-conducteurs. Le rayonnement ionisant génère des paires électrons-trous dans les matériaux. Les principaux effets ionisants sont des effets d'une particule isolée (Single Event Effects, SEE) et des effets de dose ionisante intégrée (Total Ionizing Dose, TID) dus aux paires électron-trou déposées respectivement dans les semi-conducteurs et les diélectriques. Les circuits CMOS (Complementary Metal Oxide Semiconductor) dans les MAPS sont vulnérables tant aux effets SEE qu'aux effets TID. De plus, les diodes qui détectent la charge sont sensibles à la réduction de la durée de vie des porteurs minoritaires ainsi qu'aux courants de fuite générés par irradiation.

2. Le progrès dans la conception des MAPS radiorésistants est étudié. Au cours des dernières années, les effets des rayonnements non-ionisants et les effets TID ont été évalués à l'aide d'irradiations soigneusement sélectionnées utilisant des protons, des neutrons et des rayons X mous. En outre, les performances en termes d'efficacité de détection et de rapport signal sur bruit (Signal to Noise Ratio, SNR) ont été mesurées dans des expériences réelles avec faisceau de particules. Les résultats de ces tests démontrent que les effets non-ionisants conduisent principalement à la diminution de l'efficacité de collection de charge tandis que les effets ionisants induisent surtout une augmentation du bruit électronique. Des baisses de SNR et d'efficacité de détection des particules ont été observées avec les deux types de

rayonnement pour ces raisons. En sélectionnant une épaisseur de la couche épitaxiée adéquate et en optimisant la densité des diodes, les MAPS ont atteint une efficacité de détection de 99,5% après une dose de rayonnement non-ionisant allant jusqu'à 2×10^{12} n_{eq}/cm^2 (resp.10^{13} n_{eq}/cm^2) pour une température de fonctionnement de 30ºC (resp. 0ºC). Les effets TID dans les MAPS ont été atténués par des techniques de conception spécifiques de durcissement au rayonnement et un design auto-biaisé de pixel. En outre, certains résultats de tests indiquent que la tolérance TID peut être améliorée en réduisant le temps d'intégration des MAPS, temps qui est égal au temps de lecture dans la plupart des designs des MAPS. La tolérance TID pourrait atteindre 1 MRad avec un temps d'intégration de 200 µs et près de 10 MRad avec un temps d'intégration de 10 µs. Par conséquent, l'amélioration de la tolérance TID de MAPS, passe par l'implémentation d'une lecture rapide.

3. Avec les exigences d'une vitesse de lecture élevée et d'une haute tolérance TID, des MAPS de lecture rapide ont été conçus en intégrant un bloc de compression de données et deux cœurs SRAM (Static Random Access Memory) IP (Intellectual Property). Toutefois, la tolérance au rayonnement de ces deux cœurs n'est pas aussi élevée que pour les autres parties dans les MAPS et limite sensiblement la tolérance au rayonnement de la puce MAPS entière. Notamment, la SRAM est sensible aux effets SEE, y compris aux effets d'événement latchup (Single Event Latchup, SEL) et de perturbation par particule isolée (Single Event Upset, SEU). Par conséquent, trois mémoires résistantes au rayonnement sont conçues pour les puces MAPS présentes et futures.

En analysant les stratégies existantes de durcissement aux rayonnements, une SRAM radiorésistante est conçue pour remplacer les cœurs SRAM IP incorporés dans les MAPS. Dans ce but, la cellule SRAM standard à six transistors est choisie et durcie par augmentation de la marge au bruit statique (Static Noise Margin, SNM) de la cellule et par ajout d'anneaux de garde de type P+ dans le schéma d'implantation. Dans la conception du câblage périphérique de la mémoire SRAM est incorporée une bibliothèque de logiciels de conception radiotolérante par accroissement de la distance entre transistors NMOS et PMOS donnée par une bibliothèque de logique standard. La commande de synchronisation interne de la SRAM est durcie par un design de synchronisation auto-adaptatif. Enfin, la SRAM radiorésistante est implémentée et testée dans un procédé standard CMOS - 0,35 µm. La SRAM est adaptée pour fonctionner avec des fréquences allant jusqu'à 80 MHz, des tensions d'alimentation de 2,9 V à 3,3 V et des températures de 0 à 60 ^{o}C. La tolérance aux rayonnements de la SRAM est évaluée et comparée à des résultats de test d'irradiation antérieurs. La tolérance aux effets SEU et TID est comparable et même meilleure que la tolérance des autres circuits sur les MAPS. La tolérance à l'effet SEL est supérieur à 56 $MeV\cdot cm^2/mg$, à comparer à 5,2 $MeV\cdot cm^2/mg$ avant l'amélioration. La SRAM a été développée pour être intégrée dans le capteur ULTIMATE qui équipera bientôt l'expérience STAR (Solenoidal Tracker At RHIC (Relativistic Heavy Ion Collider)).

Récemment, des procédés avec taille réduite des grilles des transistors (comme des procédés de 0,18 µm et 0,13 µm) ont aussi été utilisés pour la conception de MAPS. Les effets TID et les effets SEL sont atténués grâce à l'épaisseur réduite à de

l'oxyde de la grille et la baisse de la tension d'alimentation. Toutefois, les effets SEU s'aggravent beaucoup en raison de la charge critique SEU réduite, qui diminue avec la tension d'alimentation. Outre les techniques de durcissement aux rayonnement déjà utilisées dans la SRAM avec un procédé de 0,35 μm, un algorithme de détection et correction d'erreurs (Error Detection And Correction, EDAC) est implémenté dans la SRAM conçue avec un procédé de 0,18 μm afin d'améliorer encore la tolérance au SEU. Avec l'adoption de l'approche EDAC, une perturbation d'une bit peut être corrigée automatiquement et des perturbations de deux bits peuvent être détectées et signalées. Bien que la surface de la SRAM soit augmentée d'environ 60% par l'algorithme EDAC, la densité de bits de cette nouvelle SRAM est plus élevée que celle de la SRAM réalisée en technologie 0,35 μm en raison de la gravure plus fine – et donc plus dense – du procédé 0,18 μm. Le temps d'accès de la SRAM inférieur à 10 ns, est augmentée d'environ 3 ns à cause de la procédure EDAC. Par conséquent, la SRAM convient pour des MAPS équipant des expériences en PHE.

A l'avenir, quand les MAPS seront développés pour une plus grande précision et une plus grande zone de détection, plus de données devront être traitées par des mémoires. Dans ce cas, une mémoire radiorésistante plus petite sera préférable, en particulier en cas de procédé de 0,35 μm. Dans cette thèse, une mémoire à double accès avec cellule-2T originale est conçue et évaluée pour les puces MAPS futures. La cellule-2T proposée est constituée de seulement deux transistors PMOS. La surface de la cellule est de $4{,}55 \times 5{,}45\ \mu m^2$, qui ne représente que 67% de la surface de la cellule SRAM du procédé 0,35 μm conçue dans cette thèse. En outre, la cellule-2T est exempte d'effet SEL et a une immunité élevée contre les effets TID. La tolérance SEU est améliorée en optimisant le compromis entre la charge critique et la vitesse de lecture. Une mémoire à double accès basée sur la cellule-2T a été conçue selon les exigences des MAPS. Le temps d'accès en lecture est de 100 ns et celui en écriture est de 10 ns. Par conséquent, la mémoire à double accès basée sur la cellule-2T est un choix potentiel pour le développement futur des MAPS.

4. La tolérance aux rayonnements des MAPS avec des nouveaux procédés disponibles est étudiée. (a) Des procédés de couche épitaxiée de haute résistivité sont privilégiés. La haute résistivité de la couche permet sa déplétion presque complète, conduisant à une efficacité de collection de charge élevée. En raison du champ de dérivation associé à la déplétion, l'effet des pièges dus aux dommages non-ionisants s'atténue entraînant une amélioration de la tolérance aux rayonnements. Dans le test d'irradiation, la tolérance aux rayonnements non-ionisants a atteint plus de 3×10^{13} n_{eq}/cm^2 à 30ºC pour les MAPS basées sur une résistivité de la couche épitaxiée excédant 1 kΩ·cm. (b) Un procédé de 0,18 μm avec un puits P profond et une couche épitaxiée de haute résistivité est utilisé. La tolérance aux effets TID et SEL est améliorée grâce à un oxyde de grille plus mince et une tension d'alimentation plus basse. Les effets SEU peuvent être atténués par la SRAM radiorésistante équipée d'algorithme EDAC. (c) Actuellement, des technologies intégrées en trois dimensions (3D), qui intègrent deux ou plusieurs couches (feuilles) de dispositifs semi-conducteurs dans une même puce par amincissement, collage et interconnexion, offrent plus de possibilités de conception des circuits et d'optimisation des procédés

de MAPS. Les MAPS utilisant la technologie 3D intégrée (3D Integrated Technology, 3DIT) sont susceptibles d'atteindre une haute résolution spatiale, une vitesse de lecture accrue, une tolérance aux rayonnements élevée et une - peut-être - consommation d'énergie faible. Dans les puces 3D, la tolérance aux rayonnements peut bénéficier à la fois de l'optimisation du procédé et de la vitesse de lecture élevée.

5. Une conclusion de cette thèse et les perspectives des travaux futurs sont exposées. La tolérance aux rayonnements de MAPS aux effets non-ionisants et aux effets TID a atteint plus de 10^{13} n_{eq}/cm^2 and 1 MRad, respectivement. La tolérance aux effets TID devrait être encore améliorée grâce aux nouveaux procédés disponibles. La tolérance SEE sera améliorée par les mémoires radiorésistantes conçues dans cette thèse. À l'avenir, des designs d'architecture plus évolués incorporant les nouveaux procédés disponibles peuvent être conçus pour une tolérance plus élevée aux rayonnements. En outre, les SEE dans les procédés de couche épitaxiée de haute résistivité doivent encore être étudiés et les puces MAPS intégrées avec les mémoires présentées dans cette thèse doivent être expérimentées davantage.

Abstract

This thesis was proposed by the CMOS image sensor group in IPHC for charged particle tracking in high energy physics experiments. Monolithic active pixel sensors (MAPS) are attractive candidates for this application since their good trade-off between spatial resolution, material budget, radiation tolerance, and readout speed. Under the harsh environmental radiations of the high energy physics experiments, radiation tolerance of MAPS based on the commercial CMOS processes still need to be improved. This thesis focuses on the study and improvement of the MAPS radiation hardness.

Both non-ionizing radiation effects and ionizing radiation effects should be considered for MAPS, especially for charge sensing diodes and the MOS transistors. In the past, the MAPS radiation tolerance has been improved by selecting a proper epitaxial layer thickness, optimizing the diode density on epitaxy thickness, using radiation-hardening layout techniques and reducing the charge integration time.

With the requirements of higher radiation tolerance and higher readout speed, fast readout MAPS are conceived. However, the radiation tolerance of the SRAM IP cores built in fast readout MAPS chips is not as high as the tolerance of the other circuits and mitigates the radiation tolerance of the whole MAPS chip. Therefore, three radiation hard memories are designed in this thesis for the present and future MAPS chips. Firstly, a radiation hard SRAM prototype is realized by a full-custom designed radiation hard 6T SRAM cell, an SEL (Single Event Latchup) hardened logic library and a TID (Total Ionizing Dose) hardened timing. The tolerance to the SEU (Single Event Upset) effects and TID effects of the prototype chips is better than that of the other circuits in the MAPS. The tolerance to the SEL effect is estimated above 56 MeV·cm^2/mg as compared with 5.2 MeV·cm^2/mg before the improvement. Secondly, a prototype of radiation hard SRAM with enhanced SEU tolerance is implemented with an EDAC algorithm and a bit-interleaving storage since the SEU effects become worrying when the fabrication process is migrated to smaller feature size. Thirdly, a dual-port memory with an original 2T-cell is proposed and evaluated for higher bit density and higher radiation tolerance.

Recently, some new processes are available for MAPS chips. The tolerance of MAPS chips to non-ionizing radiation effects and TID effects can be further improved. In the future, advanced architecture designs with the new available processes can be conceived for higher radiation tolerance. Moreover, the single event effects in high resistivity epitaxy processes are still need to be studied and the MAPS integrated with the developed memories should be further experimented.

Key Words: High Energy Physics Experiments, Monolithic Active Pixel Sensors (MAPS), Radiation Effects, Radiation Hardening, Static Random Access Memory (SRAM)

1 Introduction

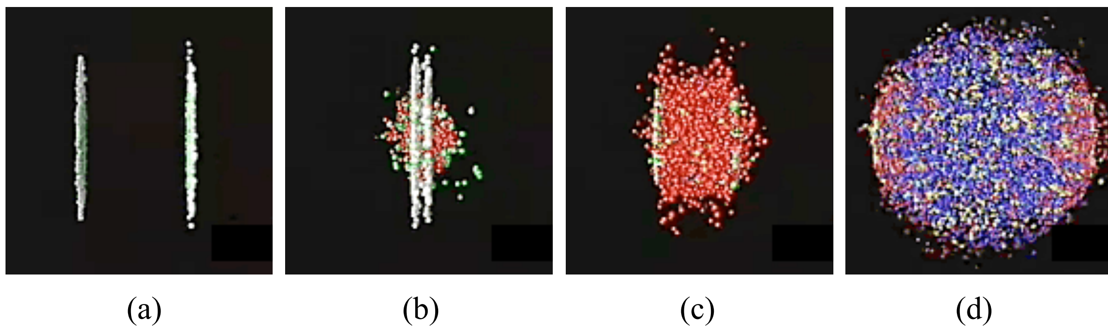
Human beings sense the world by the faculties of hearing, sight, smell, touch, taste, and equilibrium directly. Sensors help human to recognize the world as these faculties but in an extended range. The charged particles in high energy physics (HEP) experiments are not visible for human eyes. Kinds of sensors are employed to detect the particle information. Monolithic active pixel sensors (MAPS) are the silicon detectors developed for charged particle tracking in HEP experiments. In this chapter, charged particle tracking and detector technologies are introduced firstly. Then, the applications of MAPS in HEP are presented. Finally, the doctoral work is proposed in brief and the layout of the thesis is given.

1.1 Charged Particle Tracking in HEP

1.1.1 High Energy Physics

Human beings were exploring the universe for understanding its formation and nature ever since. The Big Bang model proposed by Georges Lemaitre is a prevailing theory of the early development of the universe in modern physics. It explains that the universe originated from singular point with an extremely hot and dense. With the expanding and cooling of the system evolution, new particles and matter were produced until to our current universe. [1]

Particle collision at high energy allows us to reconstruct the phenomenon after the Big Bang universe in laboratory, so as to enhance our vision on the original of our universe and the fundamental matter. Two biggest on going accelerators RHIC (Relativistic Heavy Ion Collider) and LHC (Large Hadron Collider) and near future ILC (International Linear Collider) aim to this target, as well as to find something new beyond.



(a) (b) (c) (d)

Fig. 1-1. Heavy Ion Collisions at RHIC. (a) Ions about to collide, (b) Ion collision, (c) Quarks, gluons freed, (d) Plasma created. [2]

Here we take the RHIC as an example to explain the particle collision as shown in Fig.1-1. In RHIC, ions of gold, one of the heaviest common elements, were primarily used. Two beams of gold ions from opposite direction are collided when they're traveling at nearly the speed of light, called relativistic speed. When the ions collide at such high speeds, interesting things happen. The collision "melts" the protons and neutrons and liberates their constituent quarks and gluons. Just after the collision, thousands of particles form as the collision zone cools off. Each of the particles provides a clue as to what occurred inside the collision zone. Physicists sift through those clues for interesting information.[2]

1.1.2 **Particle Detection**

The fundamental particles are shown in Fig. 1-2. The particles are classified into fermions and bosons according the spins of the particles. Fermions are with half-integer spin and obey Fermic-Dirac statistic. The Standard Model recognizes two types of elementary fermions: quarks and leptons. In all, the model distinguishes 24 different fermions: 6 quarks (up u, down d, strange s, charm c, bottom b and top t) and 6 leptons (electron e, muon μ, tau τ, electron neutrino ν_e, muon neutron ν_μ and tau neutrino ν_τ), each with a corresponding anti-particle. Bosons are with integer spin and obey Bose-Einstein statistics. The bosons are the carriers of weak, strong, gravity and electromagnetic forces. The fundamental bosons are photon (γ), gluon (g), and weak force (W^+, W^- and Z^0).

Fig. 1-2. Elementary particles in the Standard Model

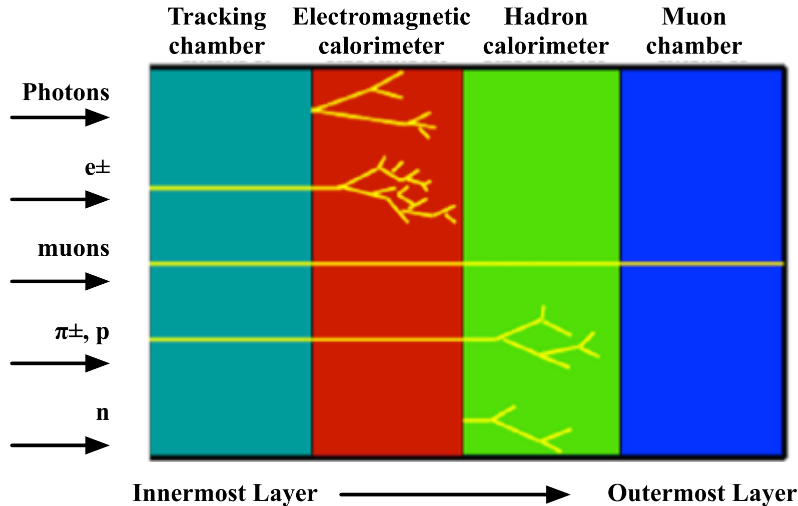


Fig. 1-3. Schematic view of particles going through a particle detector consisting four sub-detectors including tracking chamber, electromagnetic calorimeter, hadron calorimeter and muon chamber from inside to outside. [3]

The particles can be detected only through their interaction with matter [4]. In the HEP experiments, a particle detector generally consists of several types of detectors in order for detecting certain types of particles or characterizing their motion. Fig.1-3 presents a typical schematic view of particles going through a particle detector. The particle detector consists of four sub-detectors including tracking chamber, electromagnetic calorimeter, hadron calorimeter and muon chamber from inside to outside. The tracking of charged particles (such as e±, π±, p, and μ) can be detected by ionization in tracking chamber. The electromagnetic calorimeter can be used for the energy measurement of charged particles and photons. Hadron calorimeter measures the energy of hadrons. Additionally, hadron calorimeter provides an indirect measurement of the presence of non-interacting, uncharged particles such as neutrinos. Muon chamber is used to identify muons by detecting them outside of the iron of the hadron calorimeter due to the long penetration length of muons. The detectors work together for an advanced data acquisition including particle trajectories, particle velocity, energy, and so on. Subsequent physics analysis allows final statements to be made about the collision.

1.1.3 Charged Particle Tracking

During the particle tracking, the information we get from detector is almost the final-state particles, as shown in Fig. 1-4. Some short-lived particles cannot be detected directly. We infer what actually happened in the initial collision based on working backwards in time. Hence the more precisely the final-state particles are measured, the more accurately we can determine the parameters of the initial state.

Generally, the innermost detector should provide most precise measurements including particle production positions, particle momentum and particle trajectories to the outer detectors. The particle production positions reveal the presence of long-lived particles and the final-state of short-lived particles. The particle momenta are complimentary to calorimeter at low energy. The association of particle trajectories with calorimeter energy deposits and muon hits allows global pattern recognition of physics objects.

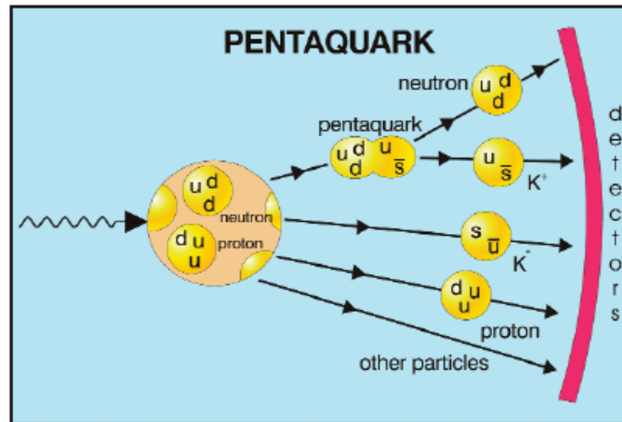


Fig. 1-4. Detection of a pentquark

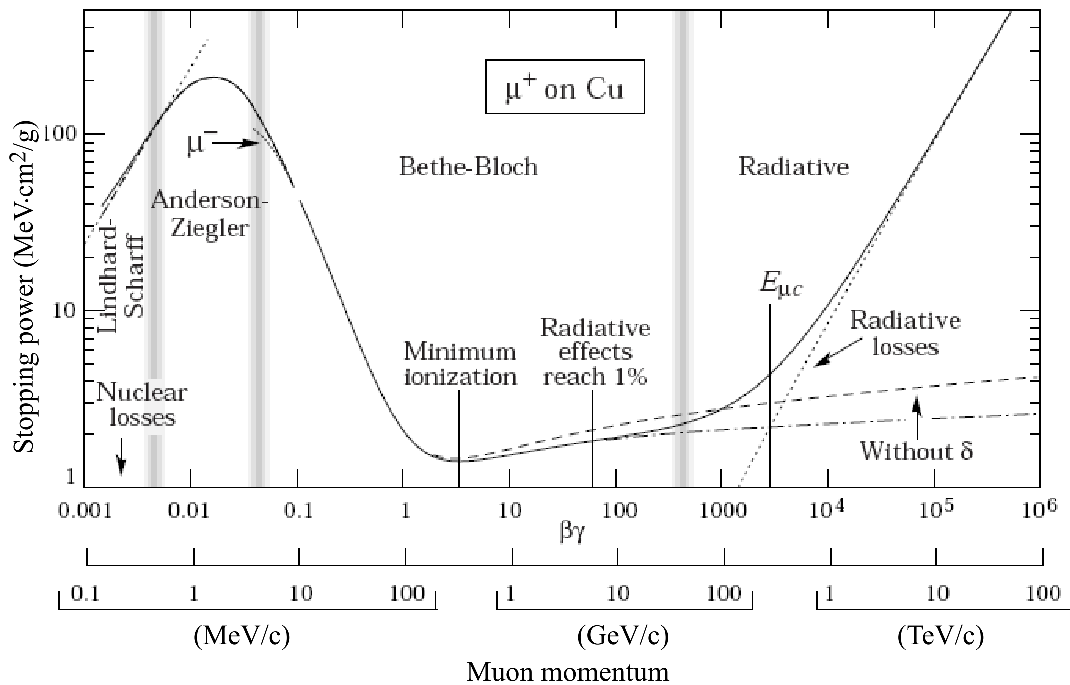


Fig. 1-5. Stopping power for positive muons in copper as function of βγ [5].

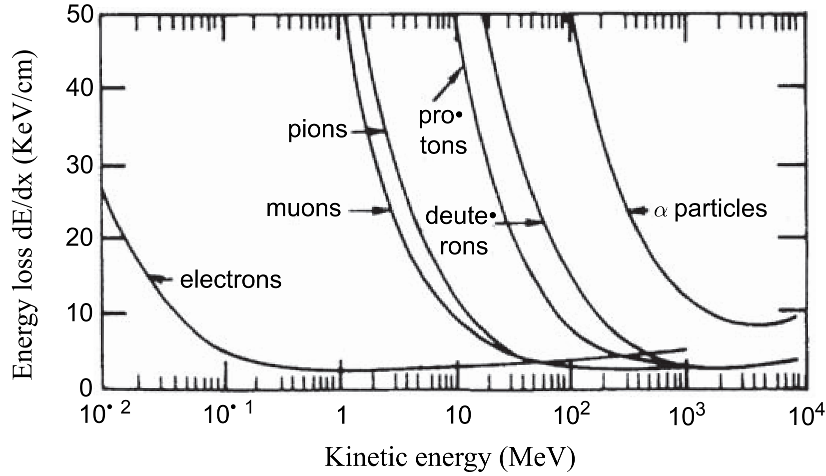


Fig. 1-6. Energy loss for electrons, muons, pions, protons, deuterons and alpha particle in air [4].

The detection of a charged particle is based on the energy loss of the charged particle, which is described by stopping power dE/dx. The stopping power is related with the category of impinging particle and properties of the absorber. Fig. 1-5 shows stopping power for positive muons in copper as function of the relativistic factor βγ. Fig 1-6 shows the ionization energy loss for electrons, muons, pions, protons, deuterons and alpha particles in air. The average energy loss of charged particles by ionization and excitation is given by Bethe-Bloch equation. For the most concerned particle in the tracking detection - minimal ionizing particles (MIP, a particle with an energy corresponding to the minimum of the energy loss rate), the stopping power can be expressed as,

$$-\frac{dE}{dx} = Kz^2 \frac{Z}{A} \frac{1}{\beta^2} \left[\frac{1}{2} \ln \frac{2m_e c^2 \beta^2 \gamma^2 T_{\max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2} \right], \quad [6]$$

where

dE/dx has units of MeV·cm²/g;

x is ρs, where ρ is the material density, s is the path length;

z is the charge of the incident particle in terms of electron charge;

A and Z are the atomic number and mass of the absorber;

$K/A = 4\pi N_A r_e^2 m_e c^2 / A = 0.307\, MeV \cdot g^{-1} \cdot cm^2$ for A = 1g mol⁻¹;

$m_e c^2$ = 0.510 MeV, electron mass times squared speed of light;

$r_e = \frac{e^2}{4\pi m_e c^2} = 2.817 \times 10^{-13}$ cm is the classical electron radius;

$N_A = 6.022 \times 10^{23}\ mol^{-1}$ is Avogadro's number;

I is the mean excitation energy in units of eV;

β = v/c is the velocity of the particle in units of speed of light;

$\gamma = 1/\sqrt{1-\beta^2}$ is the Lorentz factor;

δ(βγ) is the density effect correction to ionization energy loss;

$T_{\max} = \dfrac{2m_e c^2 \beta^2 \gamma^2}{1 + 2\gamma m_e/M + (m_e/M)^2}$ is the maximum energy loss in a single collision, where M is the mass of the incident particle.

The loss energy triggers an electronic signal in a sensor. Then the electronic signals can be processed in advance to give the position and energy information, which helps to provide the gravity of the impinging particles. The particle production positions and particle trajectories are reconstructed by combining the detected position and physics analysis. The particle momentum needs to be calculated according to the tracking information. Generally, the tracker is placed in a magnetic field to distinguish the charged particles and neutral particles. The charged particles follow a curved trajectory in the magnetic field. Thus the particle momentum can be obtained by

$$p_T = 0.3BR,$$

where p_T is transverse momentum in Gev/c. B is the axial magnetic field in T. R is the radius of curvature in m. [4] The only required parameter radius R can be known by several points along particle trajectory.

Actually, the particle tracking is much complicated due to many effects such as other energy losses, multiple Coulomb scattering and so on.

The Bethe-Bloch equation gives only the average energy loss of charged particles by ionization and excitation. Strong fluctuations around the average energy loss exist. This behavior follows Landau distribution for thin absorber and tends toward Gaussian distribution for thick absorber.

In addition, a charged particle may divert from straight path due to multiple Coulomb scattering effects. It is caused by collisions with atomic electrons. The distribution of scattering angles is described by Moliere's theory.

The root mean square of the projected scattering-angles distribution is given by

$$\theta_{rms}^{proj} = \sqrt{\theta^2} = \frac{13.6MeV}{\beta cp} z \sqrt{\frac{x}{X_0}} \left[1 + 0.038\ln(x/X_0)\right] [4],$$

where p is the momentum in MeV/c, βc is the velocity, and z is the charge of the scattered particle. x/X_0 is the thickness of the scattering medium, measured in units of the radiation length.

$$X_0 = \frac{A}{4\alpha N_A Z^2 r_e^2 \ln(183 Z^{-1/3})} [4],$$

where Z and A are the atomic number and the atomic weight of the absorber respectively. Therefore, thin and low mass detector is preferred in precision particle tracking.

1.2 Detector Technologies for Charged Particle Tracking

For charged particle tracking, there are many detector technologies such as multiwire proportional chambers, planar drift chambers, cylindrical wire chambers, micropattern gaseous detectors, scintillating fibre trackers, and semiconductor track detectors. For the innermost vertex detector, semiconductor detectors are good choices due to their dramatic merit on spatial resolution and the smallness of the ionization energy.

Silicon detector is the most popular semiconductor detector in high energy physics experiments due to the cost, resolution, and detection efficiency. Silicon is a material wildly existing in the nature and wildly used in very large scale integrated circuit (VLSI) design and the fabrication technologies are mature. As a result, the cost is low. With the decreasing of feature size of modern VLSI technologies, the spatial resolution will be improved. The energy for one electron-hole pair generation is about 3.6 eV for silicon, which is relative small in the semiconductor materials. The small ionization energy is helpful for a high energy resolution. In addition, the electron/hole lifetime in intrinsic silicon is in order of microsecond, which is a proper readout period.

The principle of silicon detector is based on ionizing interaction of the impinging particles. The detection procedure includes four steps. First of all, the charged particles interact with the detector active medium and transfer part of energy to the detector. Secondly, the medium absorbs the energy and then charge carriers are created. The number of generated charges depends on the absorbed energy and the energy required for generating one electro-hole pair. The later is related with the band gap of a marital. Thirdly, the charge carries are transported across the detector volume and collected by an electrode. Not all the created charge can be collected. Hence the charge collection efficiency should be evaluated. The charge collection efficiency is related with the charge diffusion path, charge collection speed, the electron/hole lifetime and so on. To get high efficient, the charges should be collected before their combination. Finally, the collected charge should be amplified and processed by electronic circuits. The readout circuits are the interface between the detectors and the data acquisition system. The actual particle position is obtained after data processing such as calculation of the gravity center of the charge collection.

The silicon detectors have undergone a great development in HEP experiments. Silicon pad detector, microstrip detector, silicon drift detector are ever very popular technologies for vertex detection. The requirements of HEP experiments are still pushing the silicon detectors for high granularity, low material budget, high radiation tolerance, and high readout speed. New detector techniques such as hybrid pixel sensors, charged coupled device (CCD), DEPleted Field Effect Transistor (DEPFET), MAPS are developed. In addition, sensors using SOI technology and 3D integrated technology are being developed. [7-9] Some detector technologies are introduced as follow.

1.2.1 Microstrip Detector

Microstrip detectors were proposed in early 1980's and have been used as position sensitive devices in many particle physics experiments requiring high precision tracking such as DELPHI (DEtector with Lepton, Photon and Hadron Identification) experiment vertex detector, ATLAS (A Toroidal LHC Apparatus) semiconductor tracker, and PHENIX vertex detector.

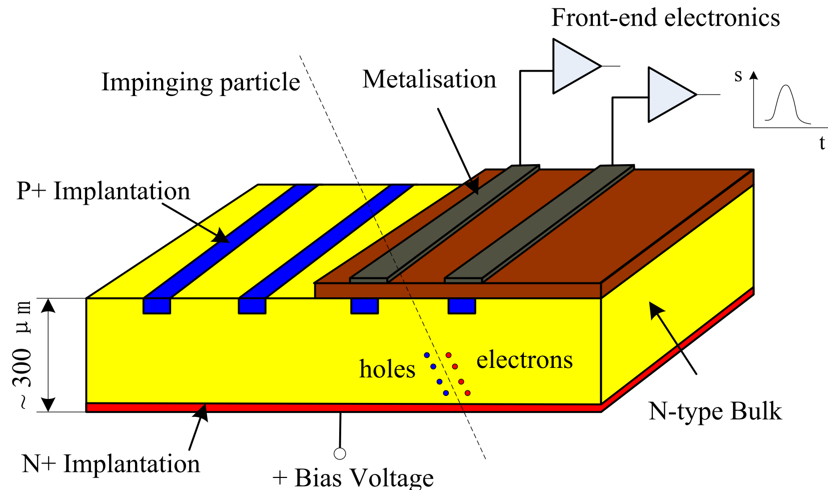


Fig. 1-7. View of a silicon microstrip detector

Microstrip detector can be seen as strip diodes on a plane. Fig. 1-7 shows the structure. The detector is formed from a high resistance n-type silicon bulk with p+ strip implementations as collection electrons and n+ implantation for bias. The typical thickness of the silicon bulk is about 300 μm. A bias voltage is required to deplete bulk region for charge collection. This voltage is about 10 to 35 V in the PHENIX multiplicity vertex detector [10]. The created electric field guides the generated charge to the cathodes, namely the p+ strips. Each strip is connected to a channel of front-end readout electronics by micro-bonding. In some detectors, some of the trips are just left floating, which transfer the charge information by coupling, to get high spatial resolution without increasing readout channel. The microstrip detectors usually are segmented in width of 10 μm to 50 μm and length of several centimeters. The readout chips can be bounded on one side or on both sides of a detector.

The microstrip detectors can provide very good spatial resolution as few microns in one dimension. In order to achieve two-dimension position information, one solution is to mount two planes of microstrip detectors back to back by placing the strips in two directions. Obviously, this solution will increase the material budgets. The other solution is the double-side silicon microstrip detector [11]. N-type diffusion strips are implanted onto the backside of a detector, which should have some angle with respect to the p-type strips on topside. In addition, the n-type strips on n-type

bulk should be separated by p-type channel stoppers. In both case, only single track can be unambiguously reconstructed. Multiple tracks will produce ghost tracks. To conquer this disadvantage, several microstrip planes should be combined. Moreover, track-finding algorithms are required to distinguish the ambiguities partially or fully.

In short, microstrip detectors can achieve good spatial resolution [12] but make hit reconstruction ambiguous. In addition, the microstrip detectors require high voltage in order to deplete the sensitive region. That results in high power consumption. In some extent, additional cooling facilities, namely additional material, are required.

1.2.2 Hybrid Pixel Sensors

Due to the good time resolution and high hadron radiation tolerance, the hybrid pixel sensors are widely considered in high energy physics experiment. Especially, the hybrid pixel sensors are advanced a lot by the requirements of the LHC experiments.

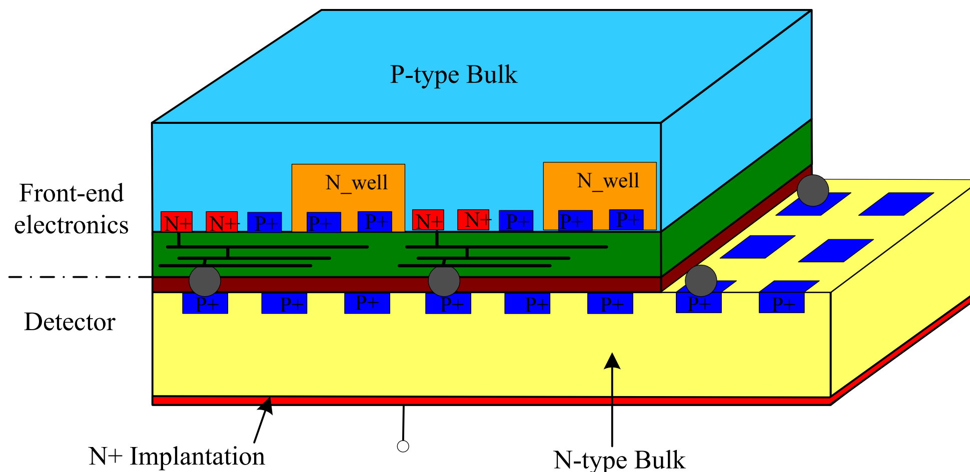


Fig. 1-8. View of a hybrid pixel sensor

Hybrid pixel sensors integrate the detector and readout circuits together by flip-chip bonding technique. The detector part can be seen as subdividing the strips in microstrip detector into many pieces. The readout channels are bonded vertically on the detector. Primarily, one active region corresponds to one readout channel. The active region and the corresponding readout channel consists one pixel. In such case, the spatial resolution is usually determined by the size of the readout circuits. To get higher spatial resolution, an idea is to implant several active regions in one pixel. Only one of the regions is connected to the readout circuits, the others work as the floating strips in microstrip detectors. Fig.1-8 shows a view of a hybrid pixel sensor.

As pixel detectors, the hybrid pixel sensors produce unambiguous position information. Since each pixel has its own readout circuits, the fully parallel readout is realized. Moreover, the small pixel area leads to low detector capacitance and low leakage current, which means large signal to noise ratio. However, the millions of bonding connections are quite complex, and the large number of readout channels lead to large power consumption of electronics.

1.2.3 **Charge-Coupled Device**

The charge-coupled device (CCD) was invented in 1969 at Bell Labs by Willard Boyle and George E. Smith. Using the CCD, the first solid-state video camera was built in 1970. In the following decades, the performances of CCDs such as quantity efficiency, fill factor, resolution, noise, readout speed and so on get a great development. CCD cameras are developed and widely used in industry and scientific discovery. In HEP experiments, CCD has been successfully used in vertex detector of the SLD experiment at the SLAC's Linear Collider. The detector consists of more than 300 million pixels with pitch size of 20 um. The frame readout time is about 200 ms.

The basic structure of CCDs is shown in Fig. 1-9. The pixels are formed by the structures like MOS capacitors. The electrons generated by impinging particles will be attracted towards the most positive potential in the device where the 'charge-packets' are created. The charge-packets can be moved out with the most positive potential moving by controlling the voltage potential of the gates. Fig. 1-10 shows the process of charge transportation and the phases of the controlling gates [13]. The operation principles are to transfer the charges in order and then to measure the charges in a special cell used for readout. Finally, the measured signal is amplified by the special cell.

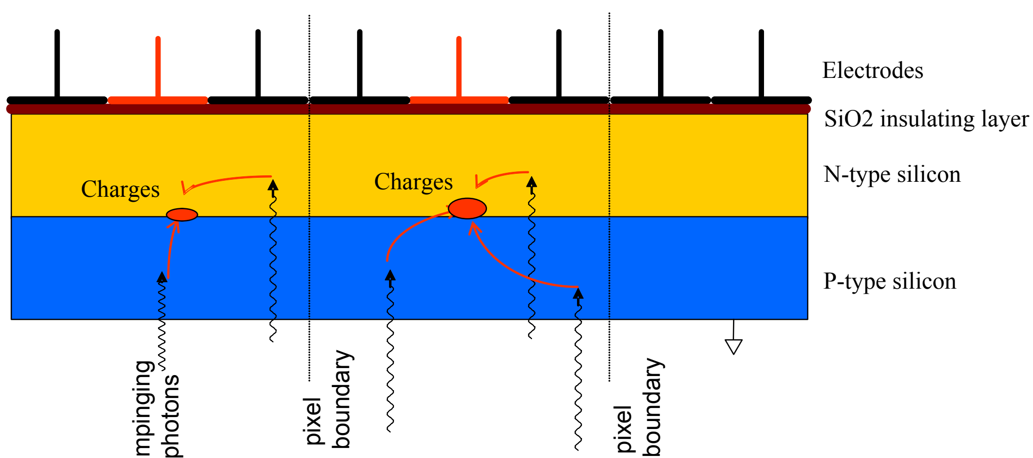


Fig. 1-9. Cross section view of charge coupled device

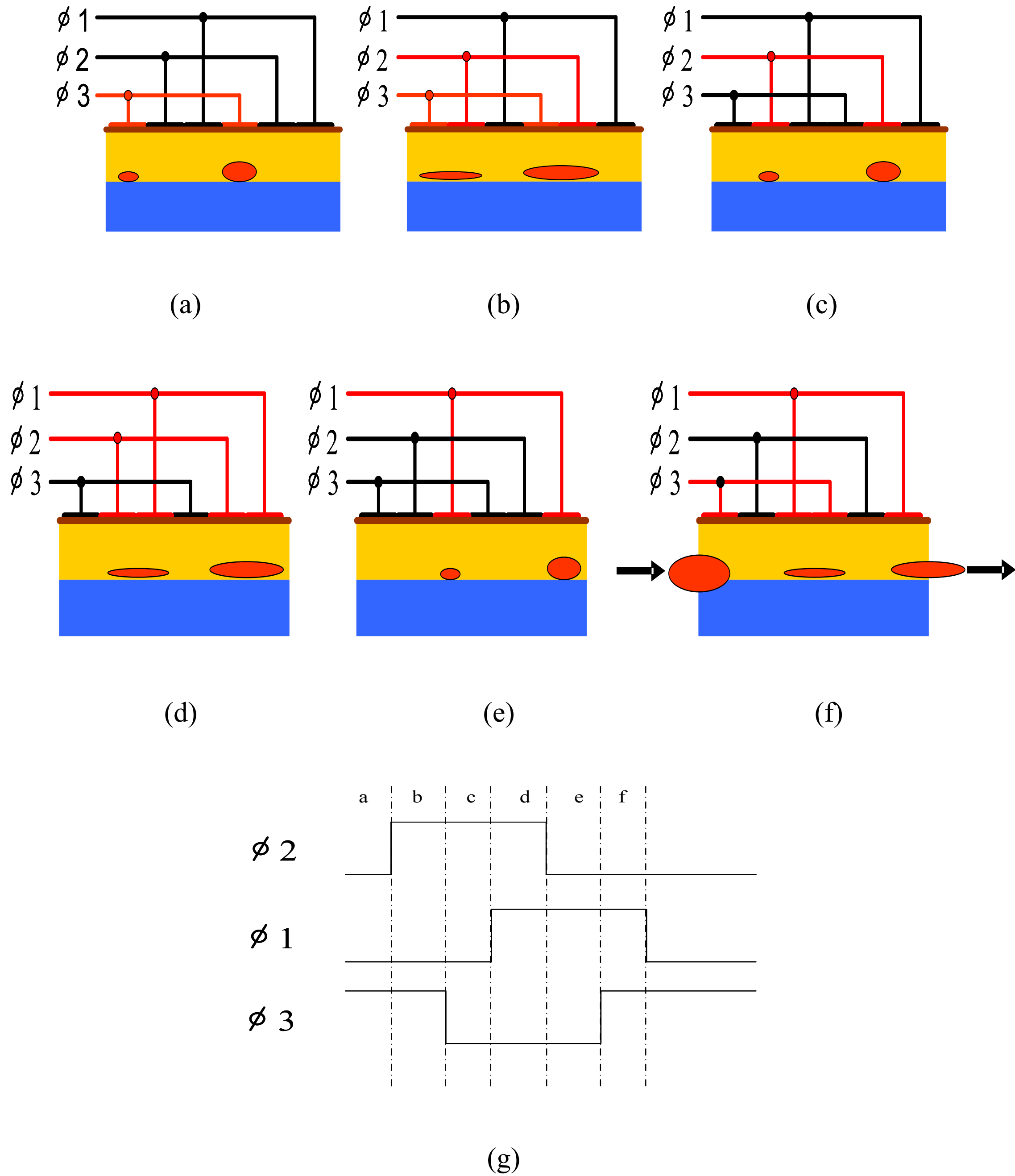


Fig. 1-10. Transport of charge packets in CCD. The charge packets are transported as processes (a)-(f) under the timing of the phase control (g).

The CCD sensors can provide good quality imaging with high readout speed. The resolution is also high enough for the HEP experiments. However, the CCD process is complex and not easy to integrate with more functions, such as analog to digital conversion and digital single processing. Moreover, since the input charge in HEP experiments is much less than visible light imaging, the CCD sensors can not provide low enough noise at room temperature. Thus, some facilities to cool down the chips are required. Furthermore, the CCD process has lower hadron irradiation tolerance than CMOS process.

1.2.4 DEPleted Field Effect Transistors

DEPleted Field Effect Transistor (DEPFET) is a new type of active pixel particle detectors. DEPFET technology has been used in an inner detector in Belle II experiment, and it is one of candidates for ILC experiments [14-16].

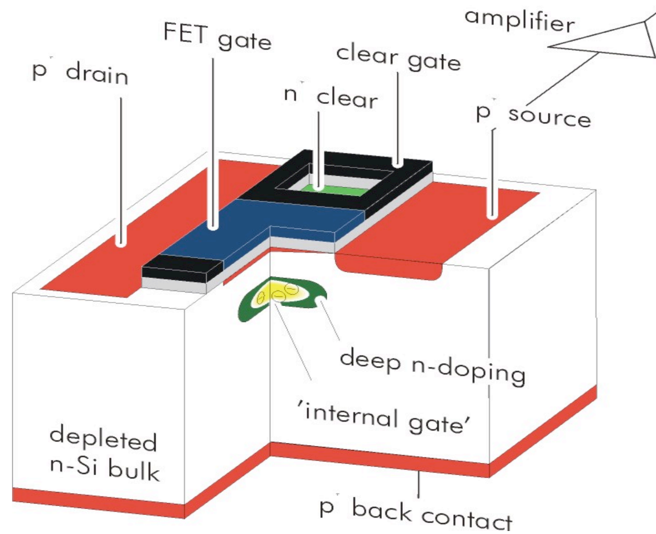


Fig. 1-11. Structure of DEPFET pixel [17]

DEPFET pixel structure is shown in Fig. 1-11. The main element is a MOSFET with a deep n-doping underneath the transistor channel, which is regarded as an internal gate. The bulk is fully depleted during the work of the detector. The electron-hole pairs are created in the bulk when a charged particle is traversing. While the holes drift to the p back contact, the electrons are moved to the internal n+ gate. The internal gate collects and stores the charges. As a result, the potential of the internal gate is changed. Consequently, a variation of channel current of the MOSFET is induced due to the potential change. Thus, the signal is read out by the MOSFET, which is also the first amplification stage of the readout electronics. During the process, the signal charge is not destructed. Hence, multiple and selective readout operations are allowed. The signal must be reset by a positive voltage at the “clear” terminal, which is n+ diffusion on the surface of bulk. The readout can be performed either in a voltage or in current mode.

DEPFET detector is full sensitivity over the whole bulk. Moreover, low noise can be achieved due to the small capacitance of the internal gate, and there is no reset noise because of the complete clearing of signal charge. Therefore, a high signal to noise ratio can be obtained. In addition, DEPFET detector can be thinned down to 50 μm for achieving low material budgets. A 64 × 128 DEPFET pixel prototype shows noise values of 225 e- and frame readout time of 18 ms [14].

1.2.5 Monolithic Active Pixel Sensors

Since 1990s, CMOS active pixel sensors (APS) have been intensely developed and widely used in digital cameras [18]. In 1997, a near 100% fill factor CMOS active pixel sensor was proposed for charged particle tracking [19]. The epitaxial layer is used as sensing volume. In 1999, monolithic active pixel sensors (MAPS) were implemented by IPHC-Strasbourg group for MIP detection. The MAPS are intended to be used in STAR experiments and are being improved for future HEP experiments including CBM, ILC and so on.

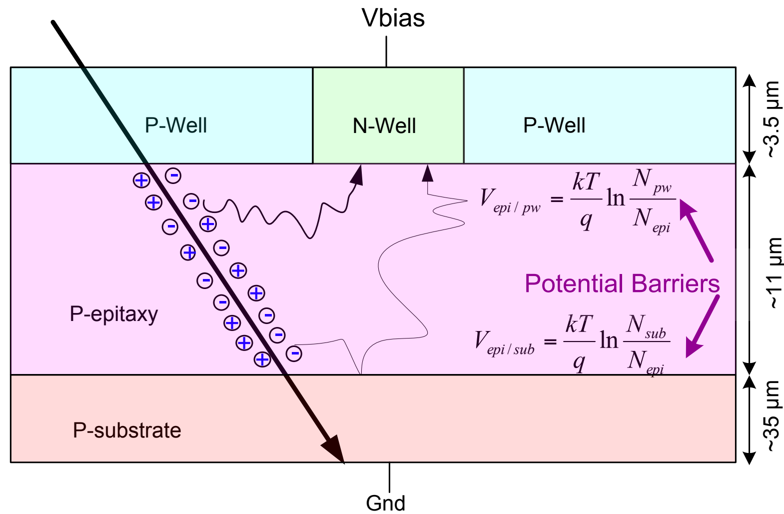


Fig. 1-12. Schematic of charge sensing element in MAPS. [9]

MAPS are based on standard CMOS processes with twin tubs on a 10-20 μm thick epitaxial layer. The sensing elements of MAPS are N-well/P-epitaxy diodes. Fig.1-12 shows the cross section of a pixel. When a charged particle traverses through the sensing element, electron-hole pairs are generated along the track by ionizing interaction. The generated electrons thermally diffused in epitaxial layer owning to the two potential barriers formed by lightly doped P-epitaxy, highly doped P-well and highly doped P-substrate. When the electrons enter into the depletion region of the sensing diode, the electrons move towards N-well quickly due to the presence of the electric field. The collected charges are integrated on the junction capacitor of the sensing diode, and then read out by the circuits on the same substrate. The fill factor can achieve 100% if there is no additional N-well in pixel. In addition, the chip generally can be thinned down to about 50 um ~ 100 μm to satisfy the material budgets in the HEP experiments. As a result, the material budget is in order of $0.1X_{0}$.

The detection performances of MAPS have been demonstrated by a series of MIMOSA (**M**inimum **I**onizing particle **MOS** **A**ctive pixel sensor) chips [20-22]. The spatial resolution can achieve 1~2 μm; the readout speed can achieve 35 μs per frame; the equivalent input noise is about 20 e^- to 30 e^-.

1.3 Applications of MAPS in HEP

1.3.1 Why MAPS?

In the high energy physics experiments, the detectors are developed for high spatial resolution, high readout speed, high radiation tolerance, and low material budgets. To detect the short-lived particles, the detectors are placed quite close to the interaction point (primary vertex). Thereby, the impinging particle density is quite high. Thus, enormous number of particle collisions should be observed and high accuracy is preferred. In order to get high accuracy, high spatial resolution (high granularity) is desired. The high granularity will lead to abundant data to be processed. (Generally, the actual granularity should be compromised with the whole sensing area.) Considering the enormous number of particle collisions, high readout speed is essential. In addition, the scattering when a particle traverses through the sensor layers may influence the particle's trajectory. Hence, the mass of the material, namely material budgets, should be low enough to achieve the required accuracy. Moreover, the detector should be survived under the irradiation of the particles.

Table 1-1 Compare of the attractive detectors

Topics	Hybrid	CCD	MAPS (2012)	Requirements of Future PIXEL Detector		
				STAR	CMB	ILC
Material budget	~1% X0	~0.1% X0	~0.1% X0	~0.3% X0	Few 0.1% X0	-
Spatial resolution	~30 μm	~1-2 μm	~1-2 μm	~1-2 μm	~5 μm	~2-3 μm
Time resolution	~ 25 ns	~ 50 μs	~ 35 μs	~ 200 μs	~ 100 ns	~ 25 μs、~ 100 μs
Radiation hardness	$\sim 10^{15}$ n_{eq}/cm^2	$\sim 10^{10}$ n_{eq}/cm^2	$\sim 10^{12}$ - 10^{13} n_{eq}/cm^2	$\sim 10^{13}$ n_{eq}/cm^2	$\sim 10^{15}$ n_{eq}/cm^2	$\sim 10^{12}$ n_{eq}/cm^2

In the prevailing detector technologies, hybrid pixel sensor, CCD, DEPFET and MAPS are the potential ones for future high energy physics experiments. The DEPFET requires a very special process and MPI is the only producer of this device although it has very good performances. The rests are compared in Table 1-1. The hybrid technology has the disadvantages on material budgets and spatial resolution. Due to the two layers for sensors and readout circuits and the connections between them, hybrid pixel sensors are much thicker than that can be done in a CCD or MAPS

technology. In addition, the readout channels make the pixel size of hybrid sensor much greater than that in the other technologies. The CCD sensors are much susceptive to hadron irradiation. Since the charge is transferred from one pixel to another in CCD sensor, the charge in the end row of a CCD chip may be transferred through more than 1000 pixels for a 1000×1000 array. Sum of the loss in charge transfer produces large signal losses and signal sharing. In addition, CCD requires a low temperature operation environment, which means mass budgets due to cooling facilities. MAPS can achieve trade-off between spatial resolution, material budget, radiation tolerance, and readout speed. Thereby, MAPS are very attractive in future high energy physics experiment for particle tracking, such as STAR, CBM and ILC.

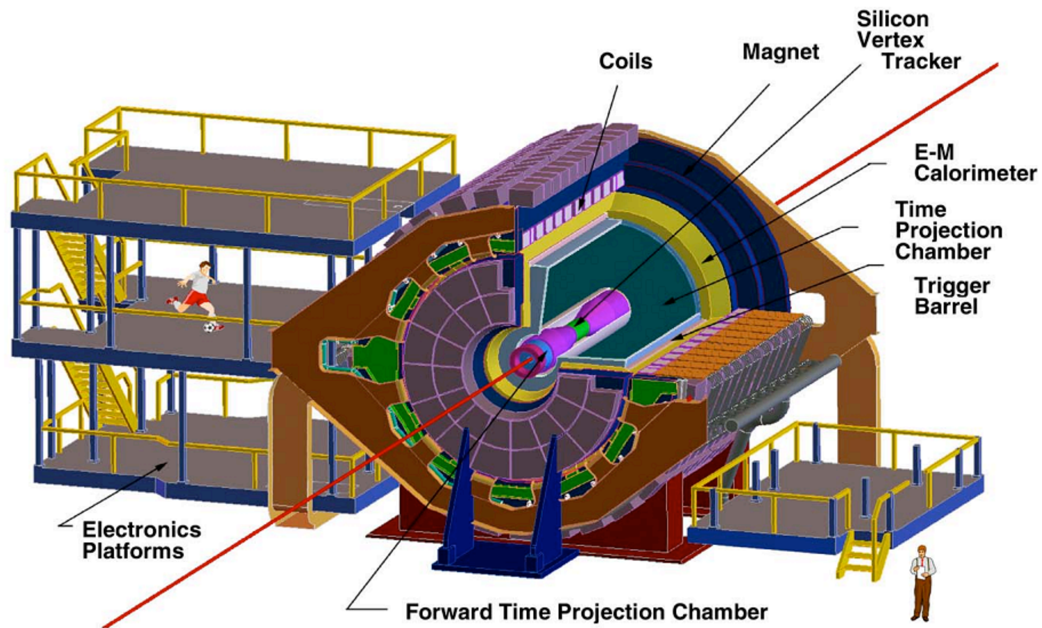
1.3.2 Example of HEP experiments – STAR experiment

STAR experiment is significantly introduced in this thesis since MAPS are intended to be used in the upgrade of STAR experiment in the near future and the research in this thesis is mostly concerned in the STAR experiment.

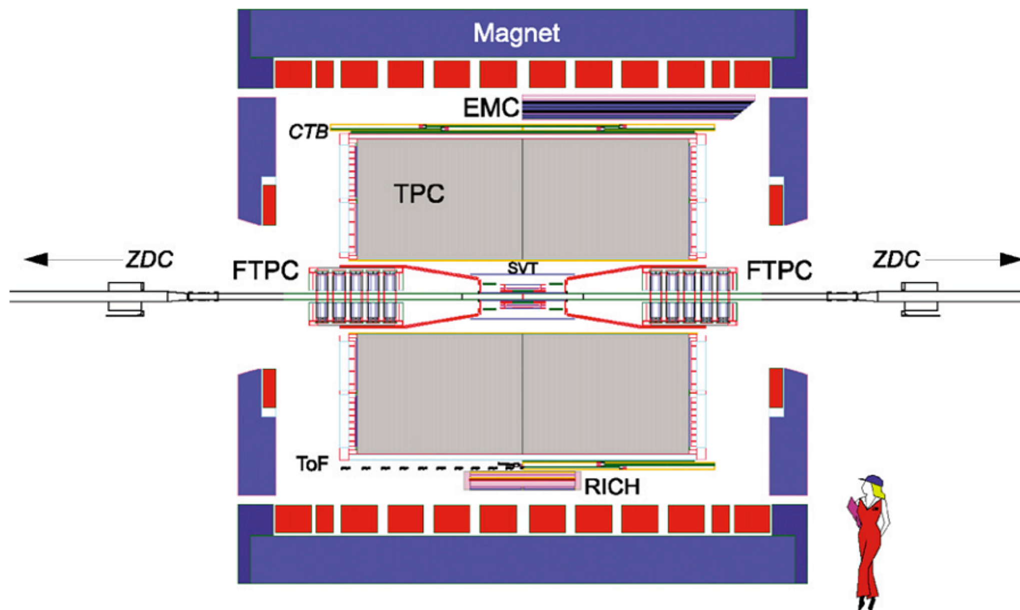
STAR, short for solenoidal tracker at RHIC, is one of the four experiments constructed at RHIC. The primary physics task of STAR is to study the formation and characteristics of the quark-gluon plasma (QGP), which is a hot and dense state as the matter in the moments after Big Bang. In this state, mesons and baryons are no longer existed as hadrons but as plasma of quarks and gluons. It is believed that this state has been existed for a few microseconds when matter started to be formed. In STAR experiment, Au particles or protons are accelerated to near relativistic speeds from opposite directions and are collided in the center of STAR detector. The matter produced in the collision can be investigated by studying the dynamics of the produced particles and the interaction of the medium with penetrating probes. The STAR experiment features detector systems for high precision tracking, momentum analysis, and particle identification [23].

Fig.1-13 shows the STAR detector. The heart of the STAR detector includes the silicon vertex tracker (SVT) and time projection chamber (TPC) for detection of trajectory and stopping power, respectively. The SVT consists of three cylindrical layers of silicon drift detectors at the radius of approximately 7, 11, and 15 cm. For three layers, the total average radiation length is below 6%. The SVT is used for accuracy position detection. The particle momentum will be provided by the track curvature in the magnetic field. The TPC is a gaseous detector. It is used for three-dimensional imaging of the ionization trail left along the path of charged particles. It helps distinguish particles with different masses or charges. It was improved by a silicon strip detector (SSD) at radius of 23 cm. The SSD is built in double-side silicon strip technology. It can achieve resolution of 20 μm in the transverse plane. The total radiation length of SSD is bout 1%. For the particle energy measurement, the electromagnetic calorimeter is outside of the TPC. To extend the tracking to the forward region, a radial-drift TPC is installed for complete azimuthal coverage and symmetry. To get the particle momenta, all above are installed in a large solenoid magnet, where the operating field is about 0.5T. The presented STAR

detector allows for the primary vertex with a precision of approximately 100 μm and secondary decay vertices with precision of about 500 μm.



(a)



(b)

Fig. 1-13. STAR detector. (a) perspective view, (b) Cross section view as configured in 2001. [23]

In order to improve the capability of the detector, the STAR detector is upgraded by adding a heavy flavor tracker (HFT). By using a much precision detector, physicists will be able to measure the displaced vertices which are 100 μm or less from the primary vertex. Thereby identify neutral and charged particles with very short lifetimes can be distinguished from the primary particles originated at the collision vertex. In addition, the HFT will extend STAR detector's capabilities further by providing particle identification for hadrons containing charm and beauty and electrons decaying from charm and beauty hadrons. As a result, the HFT enables the STAR experiment for making direct charm and beauty measurements.[24]

At the time of HFT installation, a time of flight (TOF) for time identification surrounds the TPC. Generally, TOF provides particles identification in a high momentum range than TPC. Integration of TPC and TOF can extended the detection range to 0~10 GeV/c for pion, 0.2~3GeV/c for kaon and more than 0.2 GeV/c for proton.[25] Also, when the HFT is installed, the original SVT was decommissioned and replaced by an intermediate silicon tracker (IST), which has higher resolution and higher data acquisition rates.

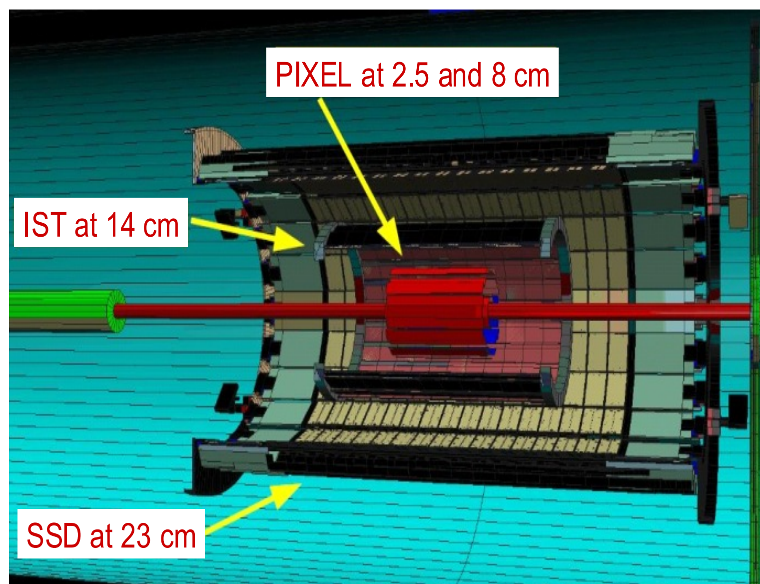


Fig. 1-14. STAR Heavy Flavor Tracker

To measure very short-lived particles, the single track point accuracy is in order of 1-2 μm and the radiation length is in order of 0.1%. PIXEL detector in MAPS technology is added closet to the interaction point. The SSD, IST and PIXEL detector are consisted of the HFT detector as shown in Fig. 1-14. The IST and SSD employing silicon drift detector are fixed at radius of 14 cm and 23 cm. The PIXEL consists of two layers of MAPS, which are fixed at 2.5 cm and 8 cm respectively. Each layer consists of many ladders, which are 10 ladders for inner layer and 30 ladders for outer layer. Each ladder consists of ten MAPS chips and a PCB board with readout buffers and drivers. Main features and specifications of PIXEL detector are summarized in Table 1-2.

Table 1-2 Main Features and Specifications of PIXEL detector

Items	Value
Layers	Layer 1 at 2.5 cm radius Layer 2 at 8 cm radius
Pitch size	18.4 μm
Hit resolution	8 μm rms
Radiation length	~ 0.3X0
Total ionizing dose	~ 300 krad/year
Non-ionizing dose	~ 10^{13} n_{eq}/cm^2
Readout speed	200 μs/frame

1.4 Work Proposal and Thesis Layout

The MAPS are placed quite close to the interaction point (primary vertex) in the high energy physics experiments. Harsh irradiation backgrounds are induced by the generated particles. MAPS are directly exposed to the particles generated in high energy physics experiments, both the sensing elements of a MAPS chip and the readout circuitry on the same substrate are irradiated. For the innermost layer of vertex detectors, the reaction rate can achieve in order of 10^6 $cm^{-2}s^{-1}$ (STAR) to 10^8 $cm^{-2}s^{-1}$ (LHC) [26]. The integrated radiation doses may vary from few tens of krad and 10^{10} neutrons/cm^2 (TESLA Linear Collider) up to many Mrad and close to 10^{15} neutrons/cm^2 (LHC). The MAPS undergo a harsh environmental radiation and mitigate their performances for charged particle tracking.

In high energy physics experiments, the particle collision yields kinds of particles including protons, electrons, neutrons, muons, neutrinos, photons and small amount of alpha particles. The charged particles yield electron-hole pairs in the sensor volume by ionizing interaction with the atoms in sensor material. The electron-hole pairs may influence the work of circuitry. The neutral particles cannot ionize a material directly, but they may transfer part of their kinetic energy to an atom by collision. If one atom receives sufficient energy, it will be removed from its position in the lattice and leave a vacancy or defect. The removed atom may be recombined with another vacancy or be lodged in an interstitial position in the lattice. Bulk damage is induced in the sensor materials. In addition, although high energy neutrons cannot ionize a material directly, the neutrons may lead to ionizing radiation by reacting with the material and releasing protons, which can ionize the material. Both the non-ionizing radiation and ionizing radiation should be considered in the high energy physics experiments.

The main effects for CMOS devices include non-ionizing effects and ionizing effects. Both of them will influence the MAPS performance.

The non-ionizing radiation induced atom displacements may reduce the lifetime of minority carriers in semiconductors. The decrease of minority carrier’s lifetime

may influence the charge collection efficiency.

The electron-hole pairs, yielded by ionizing radiation, will not lead to any obvious problem for the conductor. However, the holes may be accumulated in dielectric in presence of electric field while the electrons are swept from conductor (or semiconductor). That is long term effect well known as the total ionizing dose (TID) effects. Generally, the dielectric on the surface of devices or the gate oxide of MOS transistors is vulnerable to the TID effects. The leakage paths are induced between the sensing diode and the adjacent P-wells, thus the integrated charge on the sensing diode is reduced. The positive charge accumulated in gate oxide influences the threshold voltage and the I-V curve of CMOS transistors. In submicron processes, the effects in MOS transistors are alleviated due to thin gate oxide. However, much attention should be paid to the leakage path at the edge of the NMOS transistor, where thick field oxide still exists.

In addition, abundance of electron-hole pairs deposited by a single high energy particle may induce large transient current. The phenomenon is well known as single event effect (SEE). The SEE is categorized into many types according to the types of the sensitive circuits and devices. For instance, single event latchup (SEL) effects happen in parasitic thyristor structures, single event upset (SEU) effects in storage circuits, single event transient (SET) effects in logic circuits, while single event gate rupture (SEGR) effects and single event burnout (SEB) effects in power MOSFETs.

In high energy physics experiments, the non-ionizing radiation dose and total ionizing radiation dose are quite high for MAPS based on commercial CMOS process. The radiation effects will lead a great degradation of MAPS performances including detection efficiency, reliability, power consumption and so on. In this thesis, the radiation tolerance of MAPS is studied and improved.

In Chapter 2, the radiation effects on MAPS are not only studied in terms of radiation types (non-ionizing radiation and ionizing radiation) but also accounted for the compositions (semiconductor, conductor and dielectric) and operation/function of device/circuitry.

The radiation hard study on basic MAPS architecture is presented in Chapter 3. The principle and characteristics of MAPS are introduced firstly, and then the radiation effects and improvement are illustrated on non-ionizing radiation and ionizing radiation, respectively. The radiation tolerance of basic MAPS architecture has been improved a lot by selecting a proper epitaxial layer thickness, optimizing the diode density, using radiation hard layout techniques and designing a self-biased pixel architecture. In addition, some test results indicate that the TID tolerance can be improved by reducing the integration time of the MAPS, which equals to the readout time in most designs of MAPS.

With the requirements of high readout speed and high TID tolerance, fast readout MAPS are conceived by integrating a data compression block and two SRAM (Static Random Access Memory) IP (Intellectual Property) cores. However, the radiation tolerance of the two SRAM IP cores is not as high as for the other parts in MAPS and mitigates the radiation tolerance of the whole MAPS chip. Especially, the SRAM is sensitive to the SEE effects, especially SEL and SEU effects. Therefore, three

radiation hard memories are proposed and designed for the present and future MAPS chips in Chapter 4.

Under the new trends of manufacture process, the MAPS are designed with some new available processes including high resistivity process, 3D integration process and a small feature size process. The radiation tolerance of MAPS with these new available processes is studied in Chapter 5.

Finally, Chapter 6 gives the conclusion and the perspectives.

2 Main Radiation Effects on MAPS

In high energy physics experiment, numerous high energy particles will be generated in the collisions. The particles may interact with the detector materials by ionizing, scattering, strong interaction, electromagnetic interaction, photocurrent interaction, photonuclear interaction, and so on. The characteristics of semiconductor material and consequently the performance of the devices made from the material are influenced. The resulted radiation effects depend on the type of the radiation, its mode and rate of interaction with the material, the type of material and its particular contribution to the device characters and the physical principles of the devices. This chapter will introduce the HEP radiation environment and the type of radiation in such environment firstly. Then, the main radiation effects on MAPS will be illustrated according to the main devices and its physical principles.

2.1 HEP Radiation Environment

In HEP experiments, kinds of high energy particles will be generated after the collision. MAPS using for the innermost detectors receive the largest fluence. The radiation rate and radiation dose for several HEP experiments at the innermost pixel layer is listed in Table 2-1.

Table 2-1 Particle rate and fluence for several experiments at the position of the inner most pixel layer. [26]

Experiment	Luminosity ($cm^{-2}S^{-1}$)	Bruch crossing time (ns)	Rate (Hz/cm^2)	Fluence (n_{eq}/cm^2)	Ionizing Dose (rad/year)
LHC	10^{34}	25	10^8	10^{15}	10 M
superLHC	10^{36}	25	10^9	10^{16}	70 M
superBelle	10^{35}	2	4×10^6	3×10^{12}	1 M
ILC	10^{24}	350	2.5×10^7	10^{12}	40 k
STAR @RHIC	8×10^{27}	110	3.8×10^5	5×10^{13}	300 k

In HEP experiment, the yield particles hitting the detector mainly include proton, electron, neutron, muon, neutrino and photon. During the heavy ion collision, there are small amount of alpha particles and the other ions may rarely exist. These particles interact with the material and affect the work of electronic devices.

2.2 Introduction to Radiation

2.2.1 Type of Radiation

The radiation can be differentiated in two types: ionizing radiation and non-ionizing radiation. Fig. 2-1 shows a summary of the main consequences and the interaction particles for the ionizing and non-ionizing radiation.

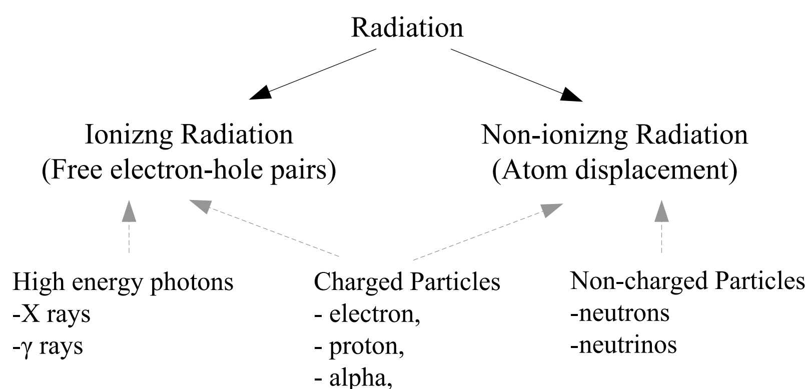


Fig. 2-1. Type of radiation

During the ionizing radiation, the particles deposit energy in the material when they pass through the material. The bound electrons that get enough energy are removed from atom. Then the electron hole pairs and ions are yielded in the material. The semiconductor even an insular may conduct for a time at a level higher than normal condition. Devices made from these materials may be mal functional even destroyed. The main ionizing processes are ionizing and electromagnetic. The high energy charged particles (such as electrons, protons, alpha) participate the ionizing interaction. While part of high energy photons (gamma-ray, X-ray) and low energy photons lead ionizing by electromagnetic interaction. High energy neutrons can not ionize with the materials directly, but may lead ionizing radiation by reacting with materials and releasing protons, which can ionize the material.

The non-ionizing radiation moves or vibrates atoms but not create ions. High energy particles passing through detector materials, part of kinetic energy may be deposited during the collision with atoms in the materials. If one atom receives sufficient energy, it will be removed from its position in the lattice and leave a vacancy or defect. The removed atom may be recombined with another vacancy or be lodged in an interstitial position in the lattice. The vacancies will be mobile and then may either combine with impurity atoms or cluster with other vacancies. The resulting vacancy complexes are usually electronically active in semiconductors, but the interstitial atoms are less active. The consequences of the displacement are complex and conventionally termed as “bulk damage”. Most high energy particles including

neutrons can lead atomic displacement.

Ionizing radiation is much more frequent than non-ionizing radiation in integrated circuits. On one hand, the ionizing has much larger radius for charged particles during interaction. On the other hand, the energy causing ionization is quite small. To create one electron hole pair only needs 3.5 eV in silicon. However, the estimate for the formation of a vacancy-interstitial point defect is 25 eV in silicon[27].

2.2.2 Radiation Quantities

（1） Total Ionizing Dose

For ionizing radiation, the number of electron hole pairs generated is proportional to the amount of energy absorbed, termed total ionizing dose. The total dose received by a device is measured in unites of rads or Grays. One rad is equivalent to the deposition of 100 ergs in one gram of matter. Gray (SI unit) is equivalent to the deposition of one joule in one kilogram. Therefore, one Gray equal to 100 rad. Unit rad (or Gray) is used to measure the accumulative ionizing dose.

（2） Linear Energy Transfer

Linear energy transfer (LET) of a particle passing through matter is the energy deposited per unit length, which equals to the energy loss per unit, namely stopping power, which has been formula and illustrated in Chapter 1.1.3. The unit is $MeV \cdot cm^2/mg$.

（3） Non-Ionizing Energy Loss

A quantity to describe the non-ionizing radiation dose is termed “non-ionizing energy loss (NIEL)” in $MeV \cdot m^{-2} \cdot s^{-1}$. The product of NIEL and the particle fluence (time integrated flux) gives the energy deposition per unit mass of material due to the non-ionizing radiation. NIEL is widely used for particles induced displacement damage in semiconductor and optical devices. In many studies, the degradations of semiconductor devices or optical sensors under irradiation are linearly correlated to the NIEL in the semiconductor devices or optical sensors [28, 29]. Although some discrepancies were observed in the application of NIEL in GaAs semiconductor devices, NIEL is quite useful in the study of Si devices [30-32].

Although the irradiation caused damage is not identical for all particles at all energies, it is possible to express the effect on silicon of all particles in terms of the damage equivalent fluence of a 1 MeV electron. This concept has been described by Brown, Gabbe and Rosenzweig in 1963 [28]. Comparing with an electron, a proton of the same kinetic energy will displace over a thousand times more because the proton

has far greater momentum and it is more rapidly stopped. Generally, the damage equivalents for protons and neutrons are also induced in the study of displacement damage. In high energy physics experiment, the NIEL value is usually scaled by referring to the equivalent fluence of 1 MeV neutrons producing the same damage as an examined beam of the fluence with a given spectral energy distribution.

2.3 Radiation Effects on MAPS

The non-ionizing and ionizing radiation result in non-ionizing radiation effects and ionizing radiation effects, respectively. To study these radiation effects, the radiation types (non-ionizing radiation and ionizing radiation) should be considered firstly. In addition, the materials of devices in the integrated circuits include conductors, semiconductors, and dielectrics. They have different responses to the radiation. Moreover, the physical principles of devices such as capacitor, resistor, MOS transistor, bipolar transistor, and diode included in CMOS circuits are various. They are sensitive to different radiation effects. Whether the effects are long-lived or transient is also quite important. The radiation effects on MAPS are studied in terms of radiation types and accounting for the compositions and operation/function of device/circuitry.

2.3.1 Radiation Effects in Different Materials

（1） Non-Ionizing Radiation Effects in Conductor

The main consequence of non-ionizing radiation is atomic displacement. Atomic displacement effects are generally long-lived. For conductor, the atomic displacement effect can be ignored in most case. In some circumstances, the atomic displacement may cause changes in conductivity such as in carefully balanced resistive elements. At extra high particle fluence, greater than 10^{20} neutrons/cm^2, atomic displacement may lead serious changes in mechanical strength.

（2） Non-Ionizing Radiation Effects in Dielectric

Dielectric materials do not require crystalline perfection in order to be good dielectrics. Consequently, the displacement generally has no significant effect on the dielectric properties of a dielectric material. The chief contribution of atom displacement to radiation effects is through the ionization accompanying the displacement, which generated by interactions between the electric field of the displaced nucleus with the electrons of other nuclei as it passes by on its way to its resting place. Such ionization contributes to charge trapping.

(3) Non-Ionizing Radiation Effects in Semiconductor

The main non-ionizing effects for devices are in semiconductor. The electrical properties of a semiconductor device are affected by the concentration of point defects. The defects result in a reduction of carrier mobility and result in a removal of carriers by trapping. The carrier lifetime will be reduced due to the new energy levels in the band gap introduced by the defects. The relation between the carrier lifetime (τ_{def}) and the concentration of defects (N_{def}) follows

$$\tau_{def} = \frac{1}{V_{th}\sigma_{def}N_{def}},$$

where V_{th} is the thermal velocity of charge carriers, and σ_{def} is the charge carrier capture of the point defect. The produce rate of the defects in irradiated material is related with the interaction and the intensity of the incident radiation.

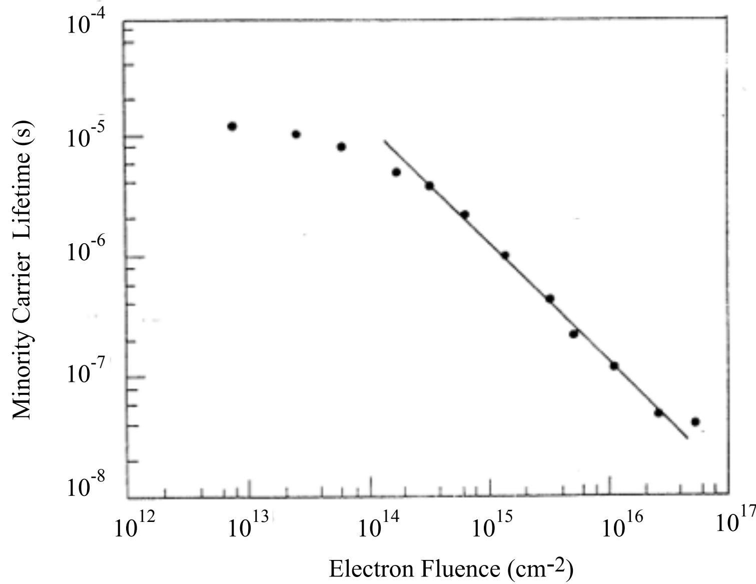


Fig. 2-2. Minority carrier lifetime of holes in N-type silicon caused by 1 MeV electron irradiation. [33]

The lifetime decrease caused by 1 MeV electron irradiation is shown in Fig. 2-2. It can be seen that, over a wide range of electron fluence (Φ), lifetime varies with fluence as follows:

$$1/\tau - 1/\tau_0 = 1/\tau_{def} = K_\tau \Phi,$$

where τ_0 and τ are the values of lifetime before and after irradiation respectively. K_τ is the minority carrier lifetime damage constant. It expresses the "damage" (charge in lifetime) per unit electron fluence [33]. The value of K_τ for 1 MeV electrons is taken as the standard with which the effect of all other particles is compared.

（4） Ionizing Radiation Effects in Conductor

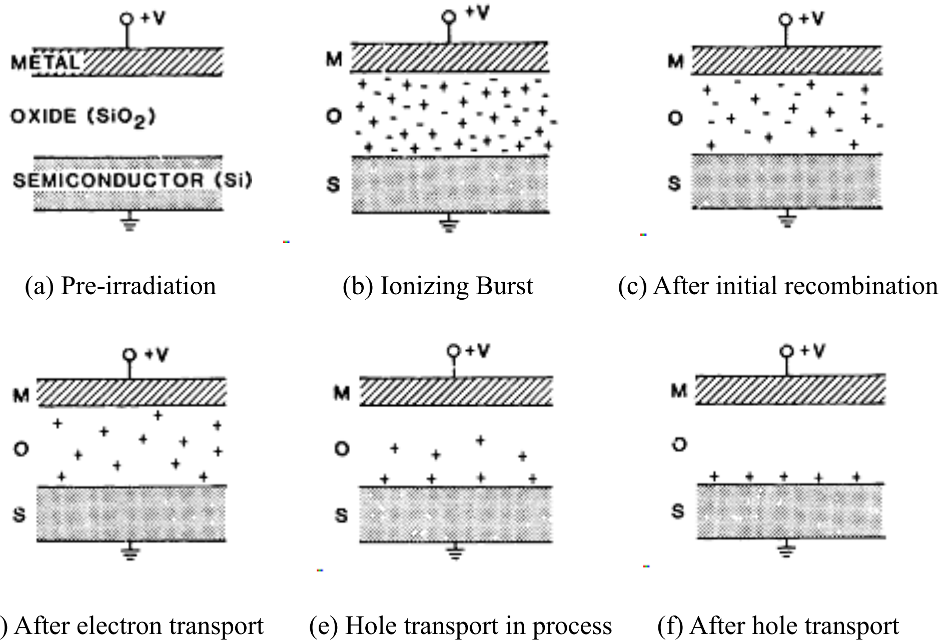
The consequence of ionizing radiation is mainly the generation of electron hole pairs. The ionization will not lead obvious problems for conductors.

（5） Ionizing Radiation Effects in Semiconductor

In semiconductor, the ionization may induce transient peak current. The magnitude of this effect is dependent on the radiation dose rate and the LET of the radiation rather than total dose. Thus, the effects may be caused by a single high-energy particle when it strikes the sensitive nodes in electronic devices, and thus referred as single event effects (SEE).

（6） Ionizing Radiation Effects in Dielectric

The ionizing effects of radiation in dielectric sub-element are particularly significant. Since dielectric should be non-conducting, electron hole pairs produced by ionizing in dielectric may change the conductivity of materials. Under an electric field, the charge traps will be built up in dielectric. As a result, additional voltage should be supplied on the devices to compensate this change. In addition, leakage path may be formed due to the charge trapping.



(a) Pre-irradiation (b) Ionizing Burst (c) After initial recombination

(d) After electron transport (e) Hole transport in process (f) After hole transport

Fig. 2-3. Illustration of initial recombination, hole transport and long-term trapping near SiO^2/Si interface.[34]

Fig. 2-3 shows the processes of ionizing induced degradation of dielectric in an MOS structure. In fact, the same process may happen on the other device, such as passivation layers of bipolar transistor. In an MOS structure, electron hole pairs are created as the radiation passes through the dielectric oxide layers. In the first few picoseconds, some electrons and holes recombine. The fraction of the recombination depends on the applied electric field and the energy and type of incident particles. The initial e-h pairs creation and instant recombination determine the actual charge yield in the oxide, and thus the initial voltage shifts. After the instant recombination, the electrons and holes will be free to diffuse and drift away from their points of generation. The electrons, which are more mobile than holes, are swept out of the oxide to be collected by the positive electrode. Some of the holes that escape from initial recombination stay near their points of generation, acting as "charge traps", causing a positive charge. Other holes undergo a slow, stochastic "trap-hopping" process through the oxide. Under the positive bias, part of the holes are captured in long-term trapping sites called "interface traps" when they reach the Si/SiO_2 interface. These interface traps can cause lightly negative voltage shifts. The effects may persist in time for few hours to several years. In addition to e-h pair generation, ionizing radiation can rupture chemical bonds in the SiO_2 structure. Some of these broken bonds may reform, whereas others can give rise to electrically active defects that can serve as trap sites for carriers or as interface traps. [34]

The ionizing effects of radiation on dielectric generally are long-lived and could be accumulated. Since the energy absorbed increases with the total dose and the number of electron hold pairs generated is proportional to the amount of energy absorbed, the ionizing effects are depends on the ionizing dose. Generally, these effects can be categorized into total ionizing dose (TID) effects.

2.3.2 Main Radiation Effects on MAPS

In MAPS based on CMOS technology, various devices mainly include resistor, capacitor, MOS transistor, bipolar transistor, general diode and the charge sensing diode for particle detection. The radiation effects in these devices are dependent on their constituted materials and the physical principle of the devices.

（1） Resistor

The resistor as a conductor is rarely influenced in HEP radiation environment.

（2） Capacitor

Capacitors consist of large areas of conductor separated by a thin insulator. It is mainly affected by ionizing radiation. Under long-term irradiation, some charge becomes trapped and may be released slowly. Thus, a small and long-term leakage

current is produced. The leakage current becomes severe in a dose of above 10^7 rads. In addition, a photovoltaic type of leakage, quite small, may be induced with high dose rate radiation. To yield significant radiation-induced conductivity (RIC) [33] in capacitors' dielectrics requires a very high dose rate.

（3） Bipolar transistor

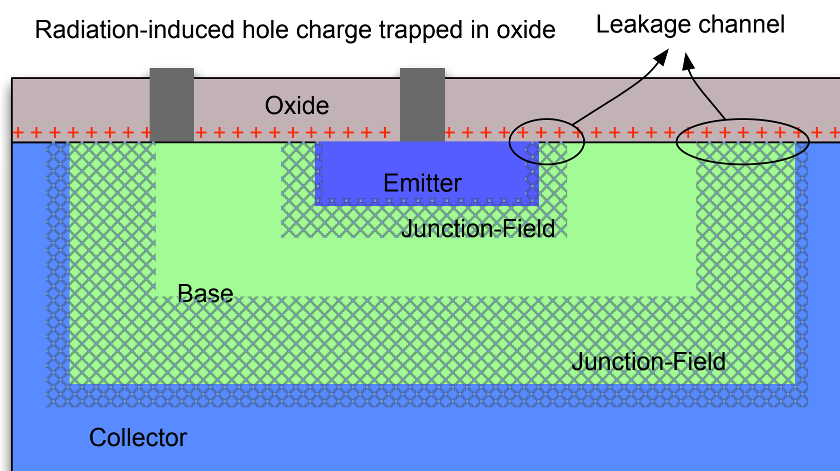


Fig. 2-4. Schematic of radiation induced charge traps and leakage channel in a bipolar transistor

Bipolar transistors consist of a pair of p-n junctions back to back, as shown in Fig. 2-4. The order can be NPN or PNP. The most common radiation effects on bipolar transistors are the degradation of gain and the increase of leakage current. One cause of gain degradation is atomic displacement in the bulk, which reduces minority carrier lifetime. The other main cause of gain degradation is ionization in the oxide passivation layer. By a process similar to that happened in MOS devices (as presented in Chapter 2.3.1), the charge trapping and the generation of new interface states are induced by the irradiation. The trapped surface charge and interface states cause an increase in minority carrier surface recombination velocity and reducing of gain. The ionization in the surface oxide, particularly the region over the collector-base junction, will also lead increase in the junction leakage currents. The radiation may also induce some other radiation effects such as increase in the collector-emitter saturation voltage and transient effects in bipolar transistors. However, in CMOS technology, only PNP connected as diode is provided. The bipolar transistors are mainly used in bandgap reference generator. The degradations on gain and leakage current are not the main concerned characteristics.

（4） MOS transistor

MOS transistors are the main active devices in CMOS technology. As mentioned above, MOS devices are not sensitive to non-ionizing radiation since MOS devices employ voltage signals rather than currents signals and the functions are dependent on the majorities. However, due to the complex composition, the MOS devices unfortunately are sensitive to the unpredictable and long-lived effects response to total ionizing dose radiation, and the short-lived upsets and the damaged latchup effects response to high rate radiation. These effects are generally considered for all CMOS circuits working under radiation environment.

Total Ionizing Dose Effects

Main total ionizing dose effects on a CMOS transistor are the shifts of threshold voltage, I-V curve and C-V curve of gate capacitor. In addition, the leakage paths between n-type active regions are induced.

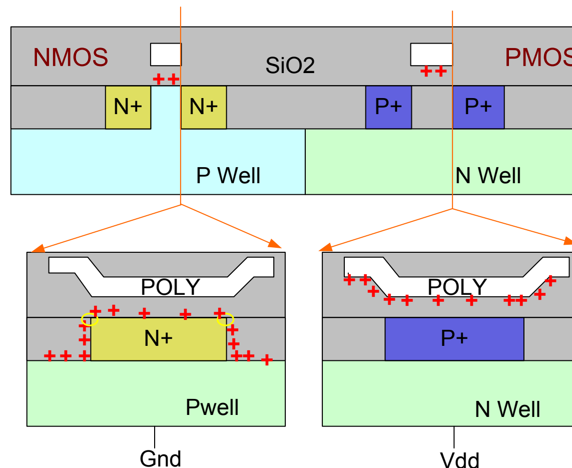
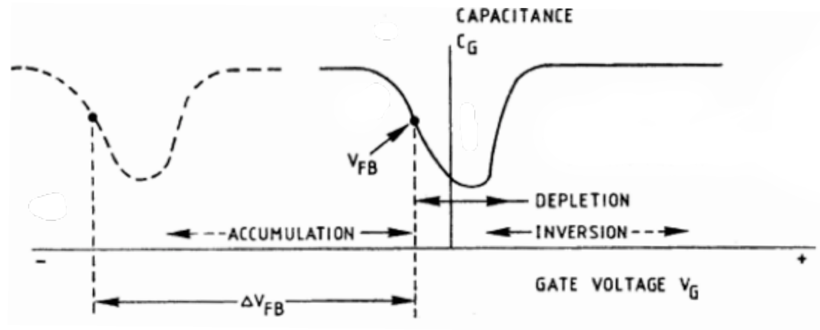
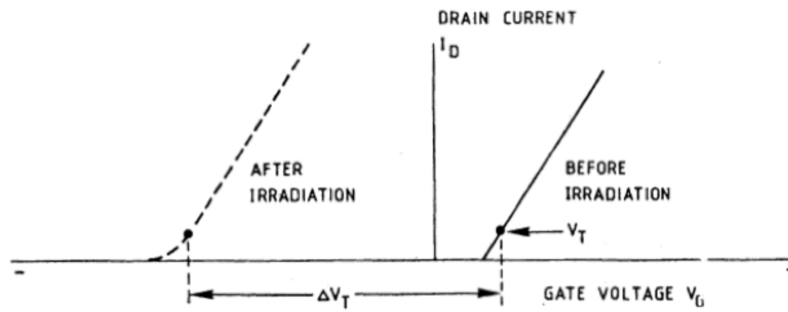


Fig. 2-5. Schematic of TID-induced positive charge in NMOS and PMOS transistors. The lower ones are the cross sections of the upper ones in the lined place.

Fig. 2-5 shows the radiation-induced positive charge on the oxide region viewed from two cross-sections of a PMOS transistor and an NMOS transistor. The charge generates an additional space charge field at the poly surface for PMOS, and an additional space charge filed at the Si surface for NMOS due to the opposite gate biases. Taking the NMOS as an example, the additional charge adds a positive potential on gate of the transistor. Fig.2-6 shows the resulting characteristics of C-V and I-V curves. The minimum in the C-V curve reflects the transition from depletion to inversion conditions. The flatband and threshold voltages shift negatively.



(a)



(b)

Fig. 2-6. Typical variation of capacitance (a) and drain current (b) with gate voltage showing the shifts in flatband and in threshold voltage due to rapped charge (no interface states) [33]

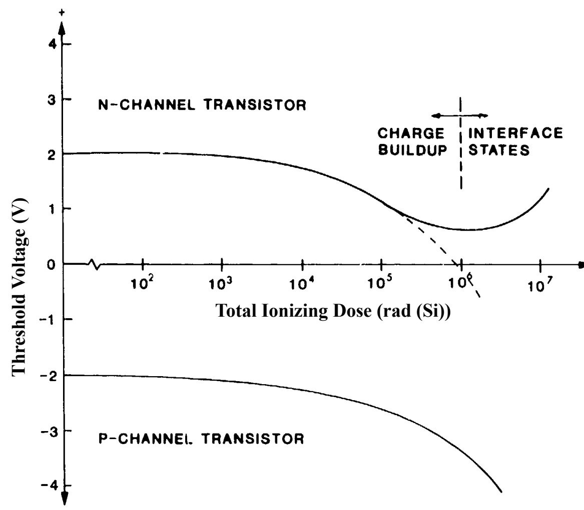


Fig. 2-7. The effects of ionizing radiation (gamma) on the threshold voltage of MOS transistors [34]

For sufficiently large amounts of trapped positive charge, the NMOS may be turned on even for zero applied gate bias and the PMOS maybe could not be turned on. The effects of ionizing radiation on the threshold of MOS transistors are shown in Fig. 2-7.

The total ionizing dose radiation is an accumulative process. As the increasing of irradiation doses, the radiation-induced charges increase. As the change of threshold voltage, I-V characteristic of the devices are also shifted. Fig. 2-8 shows a series of curves of drain current (I_D) versus gate voltage (V_G) for an NMOS device subjected to the increasing radiation dose. Each of the curves corresponds to particular malfunction in the CMOS devices. The curve 0 corresponds to the function before irradiation and the threshold voltage is V_T. As the radiation dose increase to level 1, corresponding curve 1, the threshold voltage is less than original V_T but larger than zero. The main degradations are the minor noise immunity reduction (NIR) and possibly minor loss in switching speed. The curve 2, radiation dose level 2, shows the I-V characteristic when the threshold voltage crosses zero, termed V_T of N-channel crossing zero (VTNZ). Under radiation dose of this level, quiescent current sharply increases due to VTNZ. With curve 3, radiation dose level 3, the threshold voltage get negative and switching speed reduction (SSR) is induced. When the radiation induced threshold shift to $-V_T$, change of logic state is impossible, termed logic failure (LF).

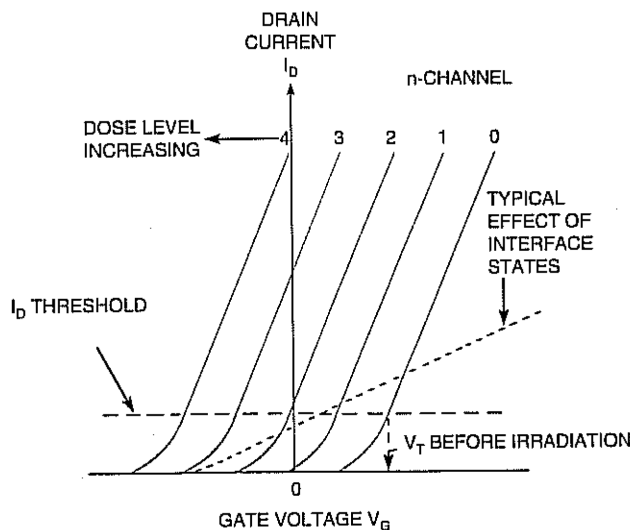


Fig. 2-8. Typical drain current (I_D) versus gate voltage (V_G) for an NMOS device subjected to the increasing radiation dose.[33]

Some researches show that the influence of the oxide traps get less effective as the gate oxide get thinner, since less charge can be generated in a thinner volume. Hughes and Powell show experimental evidence of that radiation-induced threshold shifts vary as the square of the oxide thickness [35]. Some other researches show that the threshold shift is not obvious anymore when the gate oxide is shirked to 5 nm. With the development of modern CMOS technology, the gate oxide gets thinner and thinner. The effect of threshold shift is lightly active in 0.35 um technology. However,

on the edgy of the transistors, amount of charges can be generated in the field oxide. Thus, current leakage path still exists for NMOS transistor. In addition, the leakage current exits in the parasitic structures that are similar with NMOS structure. Fig. 2-8 shows the possible leakage between n-well and n-diffusion which are covered by a positive conductor. This structure is quite common in adjacent PMOS and NMOS transistors.

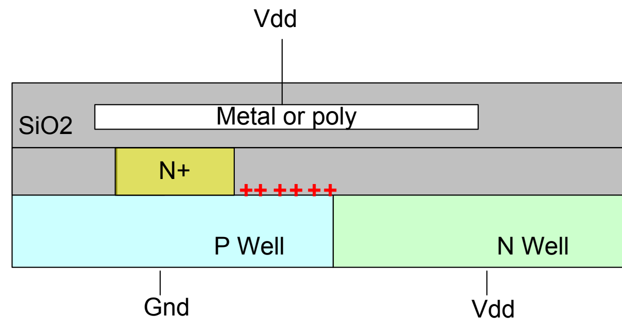


Fig. 2-9. Radiation-induced leakage path between n-diffusion and n-well in CMOS technology.

In one word, total ionizing radiation damage leads changes in circuit parameters including the standby power supply currents, input and output voltage level thresholds, leakage currents, critical path delays, and timing specification degradations. Increasing radiation dose causes progressive loss of function and eventual failure of a MOS device.

During the design of circuits, radiation tolerance to the effects is desired to be defined. Generally, the failure cannot be defined at the level of a single device element, but is rather the point at which a particular network of devices no longer tolerates the radiation effects. In space application, a radiation dose limit or maximum acceptable dose is defined for any CMOS circuits based on the dose at which the significant failure mechanism appears for those circuits. Among the degradation effects descried with the radiation dose increasing, VTNZ is an important point for most digital circuits since it leads to large increases of quiescent current. However, for some current sensitive circuits, the acceptable levels of current increase may be very low.

Single Event Effects

Single event effects induced by the charged particles passing through the CMOS circuits are significantly concerned in HEP experiment environments. The single event effects are caused by the ionizing effect due to a single high energy particle as it hits the sensitive nodes of the electric circuits. Due to different sensitive circuits or devices, there are many types of SEE including single event latchup (SEL) in parasitic

thyristor structures, single event upset (SEU) in storage circuits, single event transient (SET) in logic circuits and single event gate rupture (SEGR) and Single event burnout (SEB) generally happened in power MOSFET, and so on. In MAPS, the main SEE effects are SEU, SET and SEL.

Single Event Upset

Single event upset is the ionizing radiation-induced logic change in storage cells, such as registers, latches, flip-flops, RAM cells, and so on. This is generally a soft error and the logic reversal can be recovered in the following operations of circuits. In very sensitive devices, a single particle can cause multiple-bit upsets (MBU) in several adjacent storage cells. Although the SEU do not cause lasting damage to the device, it may cause lasting problems to a system, which cannot recover from such an error state. For instance，SEU becomes single-event functional interrupts (SEFI) when it upsets control circuits, such as state machines, placing the device into an undefined state, a test mode, or a halt, which would then need a reset or a power cycle to recover.

An important consideration to evaluate SEU susceptibility is the critical charge, which is defined as the minimum charge that must be deposited in a device to cause single event effects. For the SEU in a storage cell, the critical charge

$$Qcrit = Cs \times \Delta Vcrit$$

Where Cs is the capacitance of the sensitive node, and $\Delta Vcrit$ is the maximal voltage variation that could be accepted at the sensitive node. In general, the critical charge decreases with reduction of feature size of the technology due to the decrease of supply voltage.

Single Event Transition

Single event transition effects are due to the same reason with SEU. Since the charge collect node is not a storage cell, it can be recovered quickly from input of the circuits. As a result, only a transition pulse is induced on the transition line. If the deposited energy is high enough, the upset can be transferred to the following logic. The final affects are related with the operation details of circuit. If synchronous clock is adopted in the circuit design, the radiation-induced pulse may not be sampled and can be omitted. However, if the transition pulse is induced in the clock, the results become much serious.

Single Event Latchup

Single event latchup happens on a special parasitic device in CMOS process. Fig. 2-10 shows the cross section of an inverter based on twin-tub CMOS technology with p-epitaxial layer. Some bipolar transistors are formed on the substrate. The most

critical transistor induced latchup is shown in the figure. A NPN bipolar transistor T1 is formed n+ source diffusion of an NMOS, n well and p well and a PNP bipolar transistor is consisted of p+ source diffusion of PMOS, n well and p well. Combining with the voltage connection of an inverter, the parasitic thyristor (or parasitic silicon rectifier, SCR) is also shown in Fig. 2-10.

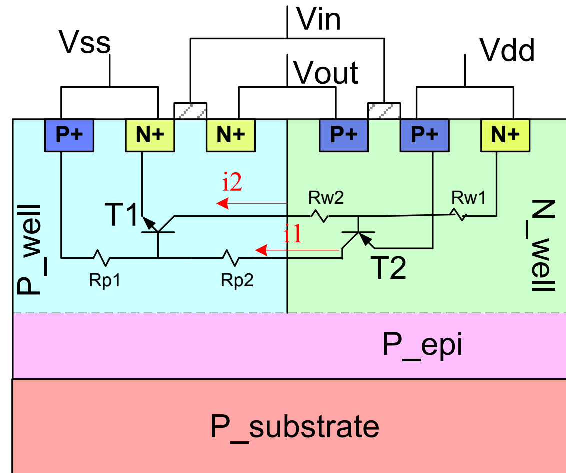


Fig. 2-10. Parasitic SCR in an CMOS inverter

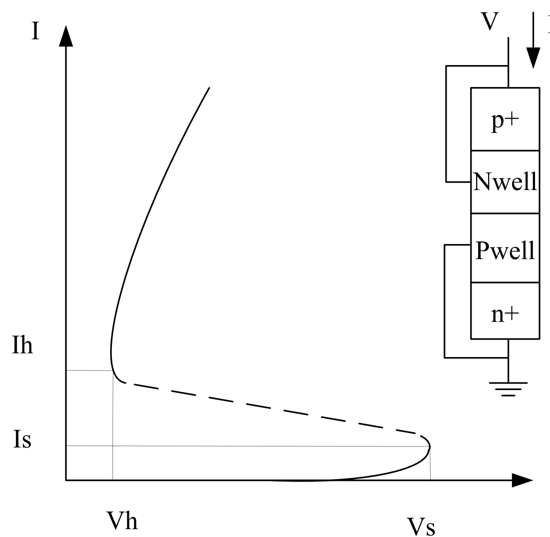


Fig. 2-11. I-V characteristic of a silicon rectifier

Fig. 2-11 shows the I-V characteristic of a SCR. Is is the minimal current which are able to switch the SCR from high impedance region to the negative differential resistance region. Ih is the minimal current to keep the SCR in the negative differential resistance region. Is and Vs are typically referred to the switch current and voltage, respectively. Ih and Vh are referred to the holding current and voltage, respectively.

Without external trigger, the SCR is closed. As the charged particle penetrates the devices, transient current may be induced in n well or p well. If the current large enough, T1 or T2 may be turned on due to the voltage increase on the parasitic p well resistor Rs1 or the voltage drop on the parasitic n well resistor Rw1. Thus,

$$i1(t) = \beta_{T1} \cdot \beta_{T2} \cdot i2(t-1)$$

$$i2(t) = \beta_{T1} \cdot \beta_{T2} \cdot i1(t-1)$$

Where β_{T1}, β_{T2} are the gains of bipolar transistors T1 and T2. $i1(t)$, $i2(t)$ are the base currents of T1 and T2.

If the gain product of bipolar transistors T1 and T2 is larger than unit (which is true in most conditions), the current from power supply to ground will increase quickly and reach the switch current Is. Thus, the SCR is switched to low impendence state, the latchup happens. In standard CMOS process, Vh is much lower than Vdd. Hence, the low impedance state can be maintained even the transient triggering is removed. Obviously, the current will continuously increase until the chip is destroyed or the power is cutoff. The SEL is a destructive effect.

（5） Diode

The most common diode is formed from a diffused p-n junction. The diodes can perform a large variety of electronic function such as rectification or blocking, switching, photocurrent generation, light emission and Zener breakdown at an electronic barrier. In MAPS, there are mainly two kinds of diodes in function: blocking and charge sensing. The charge sensing diode will be discussed specially in the following section. The blocking action is not affected seriously by radiation since the non-ionizing radiation induced atomic displacements are not enough to make sense on the blocking function and the ionizing induced transient current will be discharged.

（6） Charge Sensing Diode

The charge sensing diodes are formed from n-well and p-epitaxy. The function of the diode is for charge collection. The collected charge is the integration of the radiation-induced current during the integrated time, which depends on the system design.

Not all the charge deposited in the sensing element can be collected because some of the deposited charge may be collected by the adjacent sensing diodes, and some may be recombined. The most important characteristic of the charge sensing diode is the charge collection efficiency, the ratio of collected charge to deposited charge. Total amount of the collected charge is quite small (most probable value of 400 electrons) for MIP. The performance of charge sensing diode is easily affected by

the radiation.

Firstly, the non-ionizing radiation induced semiconductor defects will combine the electron-hold pairs generated by the incident particle.

Secondly, the ionizing radiation induced positive charge may lead additional recombination of electrons in sensing diode.

Thirdly, random telegraph signal (RTS) due to radiation induced bulk damage has been detected in CMOS image sensors under proton and neuron irradiation [36-38]. It is necessary to study the RTS in MAPS.

2.4 Conclusion

This chapter gives the physical mechanism and consequence of the radiation firstly. Consequently, the radiation effects in different materials and the main radiation effects on MAPS are analyzed. The main radiation effects for MAPS chips can be concluded as follow:

(1) Non-ionizing radiation effects. They result in degradations on charge collection efficiency and noise performance.

(2) Total ionizing dose effects. They may lead to an increase of leakage current between adjacent n-type diffusions. The power consumption will be increased and the reliability will be reduced. Especially, the noise in charge sensing diode is increased.

(3) Single event upset and single event transition effects. They cause functional error.

(4) Single event latchup effect. It may induce very large current from power supply to ground and then may destroy the chip.

The strategies to resist the radiation effects and the experimental studies will be discussed in next chapter.

3 Radiation Hardness Study on MAPS

In HEP experiments, the MAPS chip will be exposed to harsh environmental radiation without shielding of any packages for the application of particle detection. The radiation effects lead degradations on the performances and reliability of the MAPS chips. This chapter introduces the principle and main characteristics of MAPS firstly and then discusses the radiation tolerance and the improvement strategies for non-ionizing radiation and ionizing radiation, respectively.

3.1 Principle of MAPS

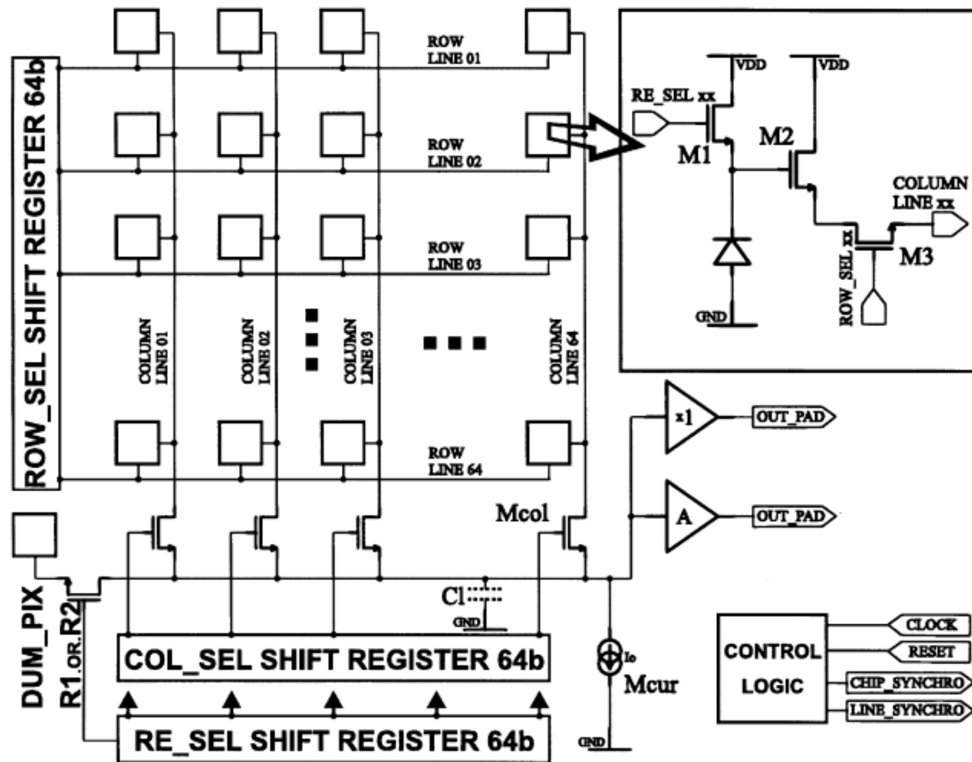


Fig. 3-1. Simplified block diagram of primary MAPS.[27]

The original idea of MAPS is to integrate the detector and readout circuits on the same substrate like optical CMOS image sensors. Thus, the primary organization of the MAPS is quite similar with optical CMOS image sensors. Fig 3-1 shows a simplified block diagram of primary MAPS (named MIMOSA I), which is designed for demonstrating the feasibility of the new detection technique. It consists of a pixel array, row and column control registers, read control registers, column select switches,

column bias circuits, output amplifier and control logic. On the top right of Fig 3-1, a three-transistor (3T) pixel is shown. The transistor M1 resets the sensing diode to reverse bias. The transistor M2 is a source follower, which is biased by the column current source Mcur. The transistor M3 is used for row selection. The main differences between the MAPS and optical CMOS image sensor are the sensing element and the charge collection principle. The CMOS image sensors use a photodiode, which convert the light to electric signal by photocurrent effective. While the MAPS require to detector an extended range of particles, the sensing element of MAPS is an n-well/p-sub diode. The electric signal is generated by ionizing interaction between the particles and silicon materials. In addition, the photocurrent in CMOS image sensor is generally much larger than the particle induced current in MAPS chip. Therefore, the charge collection efficiency and noise are very strict for MAPS design.

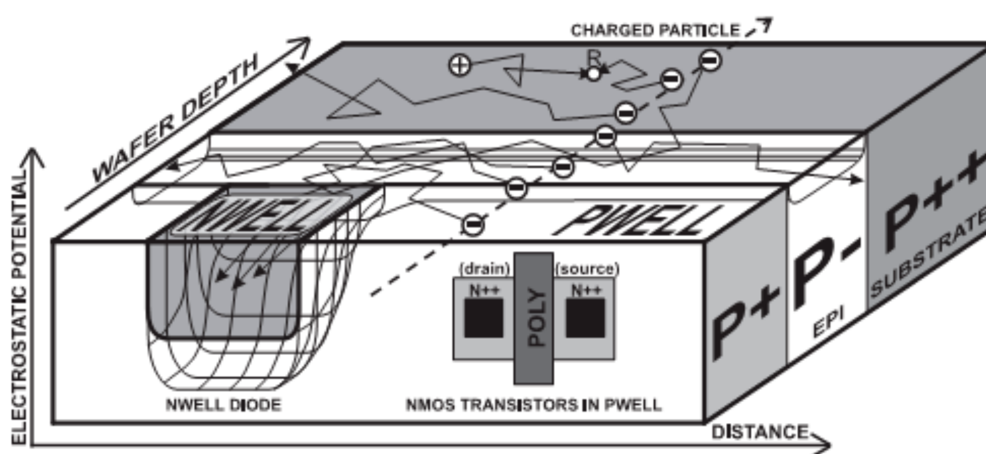


Fig. 3-2. Sketch of the structure of MAPS for charged particle tracking. The charge-collecting element is an n-well/ p-epitaxy diode. Because of the difference in doping levels (about three orders of magnitude), the p-well and the p++ substrate act as reflective barriers. The generated electrons are collected by the n-well. [27]

Fig. 3-2 shows the physical structure of MAPS. A twin-well process with p epitaxial layer is selected. As we have discussed in the first chapter, the amount of electron hole pairs created by a particle is proportional to the path length of the impinging particle. In modern submicron CMOS process, the well is shallow for charge generation. The well depth is about 3 microns or less, and the depth is prone to be diverse during the production. The epitaxial layer, whose thickness of 4 μm to 20 μm, is used for charge generation in the MAPS and the n-well is used for charge collection electrode. A much important reason of using epitaxial layer is that the structure provides the possibility of 100% fill factor. Obviously, to get a 100% fill factor, any other n-wells should be avoided. Namely, PMOS transistors cannot be used in pixel. In addition, the graded doping process of p-well, p-epi and p-sub is

selected to form barriers for electrons moving to p-well and p-substrate. The potential barriers formed between p-well, p-epi and p-sub can be formulated as

$$V_{epi/sub} = \frac{kT}{q}\ln\frac{N_{sub}}{N_{epi}}$$

and $V_{epi/pw} = \frac{kT}{q}\ln\frac{N_{pw}}{N_{epi}}$,

where k is the Boltzmann constant. q is the electron charge. T is the absolute temperature. N_{sub}, N_{epi} and N_{pw} are the doping of substrate, of epitaxy and of p-well, respectively. In MAPS, the epitaxy is lightly doped. The doping concentration of epitaxy is about 3 orders lower than the doping of the substrate and well. Thus, most generated electrons move towards the n-well.

The collected charge is integrated on the capacitance of the sensing diode and droved by the source follower. The procedure includes three phases: reset, charge integration, and readout. During the reset period, the floating diffusion of the sensing diode and the floating gate of the source follower are adequately initialed. The floating node must to be reset periodically for removing the collected charge and compensating the diode leakage current. After reset, the charge starts to be integrated on the capacitor of the input node until next reset operation. This period is defined as integration time τ_{int}. In this case, it equals to the readout time of one frame. Then, the integrated signal can be readout by turning on the corresponding row and column select transistors. In the primary chip, the signal is readout and amplified simply. Advanced data processes are performed by software during offline to extract the expected signals.

Offline data processes mainly include correlated double sample (CDS), pedestals subtraction, and common mode shift calculation.

The operation of CDS is to calculate the difference between two consecutive frames taken after the reset. The pixel works as a charge-integrating device. The integration time equals to the readout time of one frame. By addressing a certain column and row, the pixel information can be read out one by one. In primary MAPS chips, the output is with an analogue signal. An external 12-bit ADC (analogue to digital converter) is used offline to digitize the raw analog signal. Fig. 3-3 illustrate the CDS processing, subtracting the raw data of two successive frames. We can find that the fixed pattern dispersion is much larger than the typical signal amplitude.

The signal remaining after the CDS processing is still a combination of signals including the incident particle interactions considered as the signal to be detected, the constant in time pedestals resulting from the integration of leakage currents, the noise contributions from thermally generated leakage current, and the signal fluctuation in the readout electronics. G. Deptuch categorized the signals into the expected signal due to interaction, the random signal variation, the pedestal, and the common mode

shifts [27]. The pedestals (shown in Fig. 3-4 (a)) can be calculated by averaging measured signals over many events without physical signals. Then, the pedestals are subtracted from the remaining signal after CDS. Fig. 3-4 (b) shows the results after pedestal subtraction. The new pedestal signals are nearly uniform. In general, the data for interferences are of unknown origin, but exhibiting correlation for all pixels in an array. The subtraction of common mode shift allowed correcting the data for interferences. Fig. 3-4 (d) shows the data after the pedestal correction and common mode correction. These data include expected signal and the residual random noise.

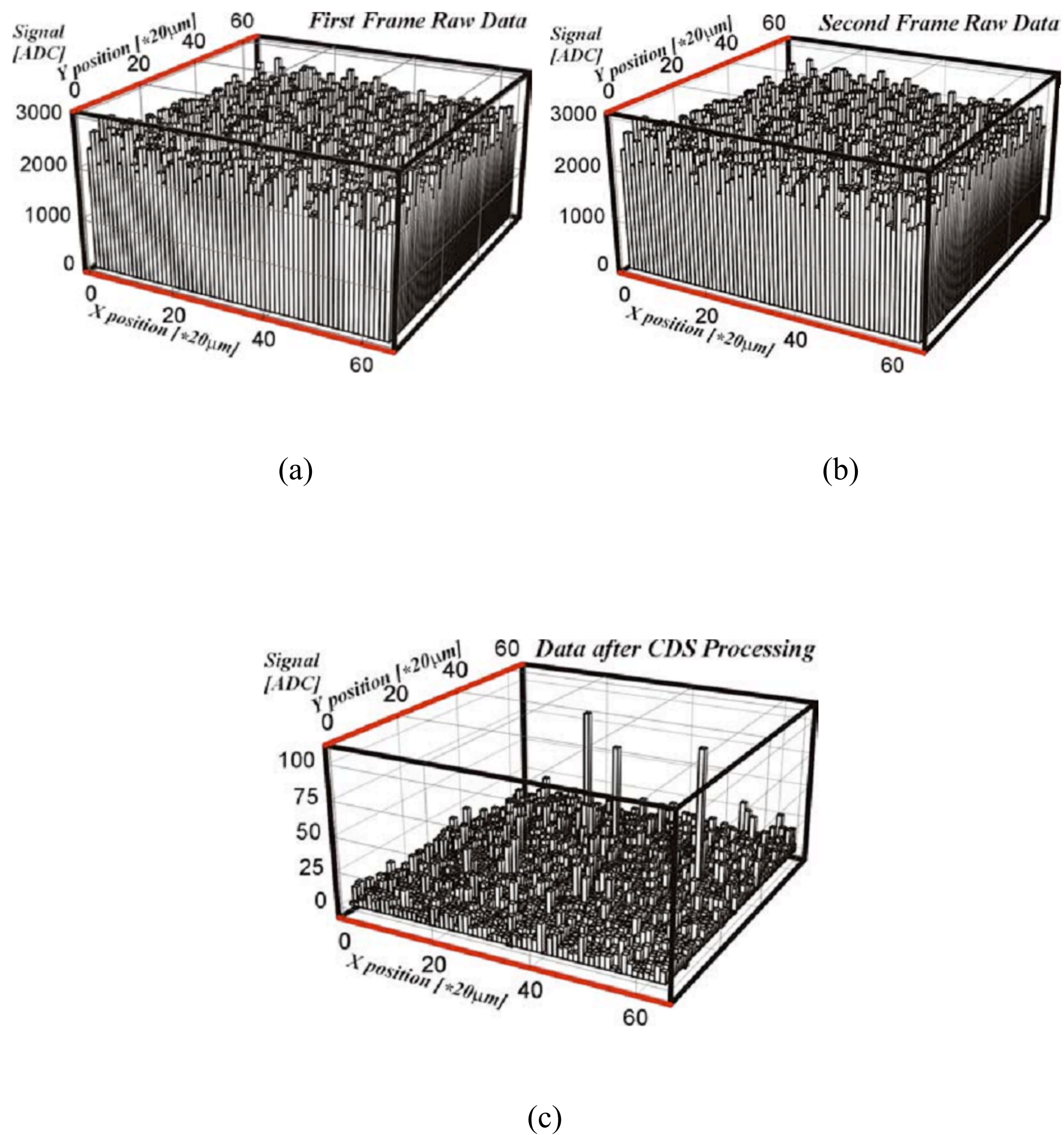


Fig. 3-3. Correlated double sampling. (a) the first frame raw data, (b) the second frame raw date, (c) the data after CDS processing [27]

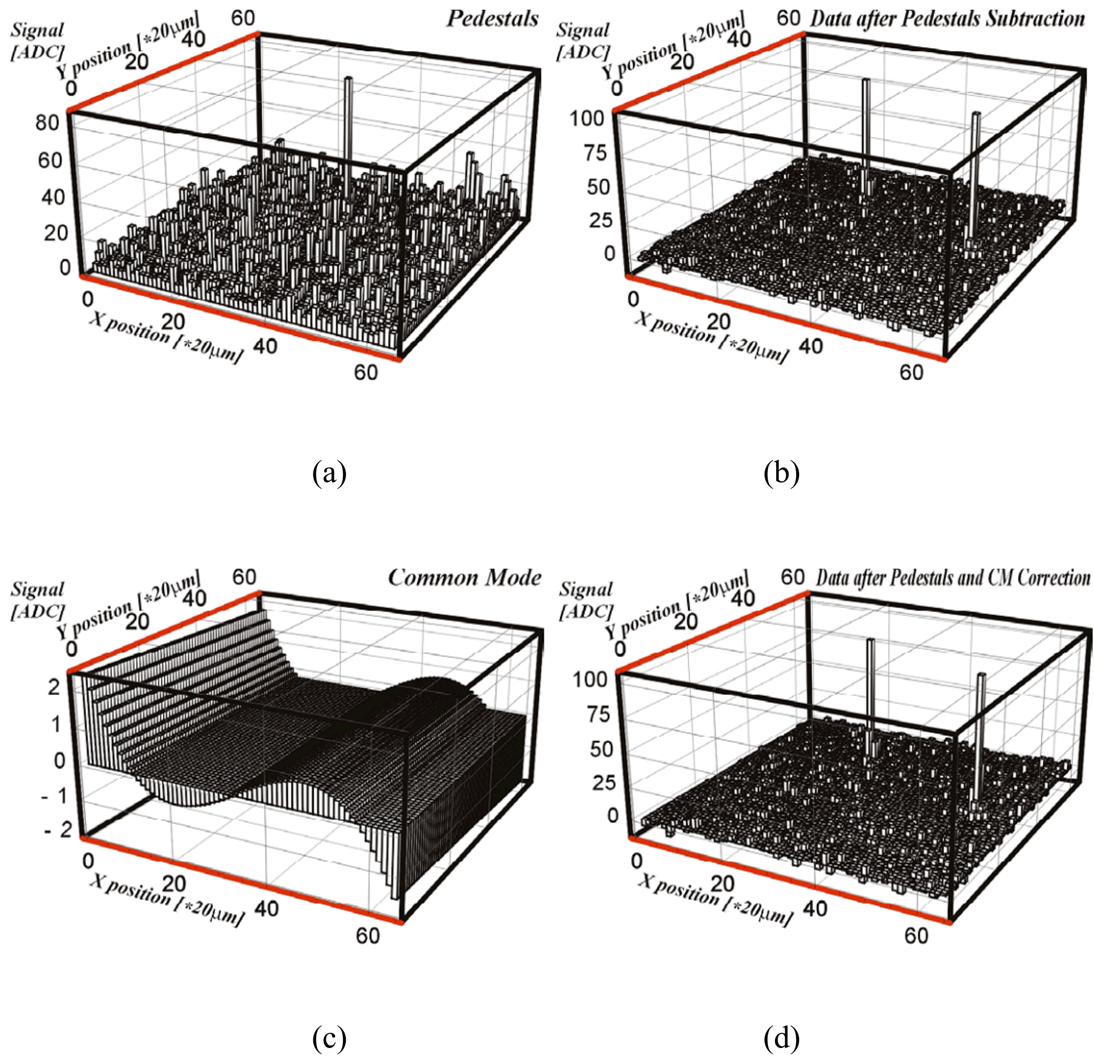


Fig. 3-4. Data processing after CDS. (a) Pedestals, (b) Data after pedestals subtraction (c) Common mode shift calculated for the analyzed event, (d) Data after pedestals and common mode shift subtraction.[27]

The noise distribution also exhibits a high degree of uniformity. The average noise level is measured as a mean value of the distribution. Proper single to noise ratio (SNR) is used to extract the expected signal. The high level of temporal signal fluctuations may fake real signal, since they could be survived after the CDS processing, pedestal subtraction, common mode correction and even SNR filtration. However, this signal is possible to be recognized in the cluster recognition pattern. Since a particle hit may fire the surround pixels, the SNRs in the cluster following a recognition pattern can be picked up. The noise signals that really lead a same pattern may be taken as a real signal and result in fake detection.

3.2 Characteristics of MAPS

3.2.1 Charge Collection Efficiency

The typical value of charge generation for MIPs is 80 electron-hole pairs per micron in silicon. In the epitaxy thickness of 14 - 15 μm (used in most MAPS chips), about 1000 e- are generated. However, not all the electrons can arrive at the n-well and can be collected to electric signal. Part of the electrons may be recombined quickly, and some may be dispersed to the adjacent electrodes. Charge collection efficiency η is defined as

$$\eta = \frac{Q_c}{Q_{tot}},$$

where Q_c is the collected charge and Q_{tot} is the total charge deposited in sensitive volume.

The total charge for MIPs can be estimated by the production of the charge of 80 electrons and the depth of the crossing path of the particle. Thus, the total charge for a certain fabrication process mainly depends on the angle between the sensors and the particle.

The collected charge is the integration of the particle-induced current on integration time, namely,

$$Q_c = \int_{\tau_{\mathrm{int}}} i_p(t)dt.$$

It should be noted that i_p is the particle induced current on the concerned pixel. In fact, part of charge may be collected by the adjacent pixels in an array and are not included in i_p. In addition, this formula indicates that some charge will be lost due to the infinite integration time.

In order to reduce the loss of the charge, a bias voltage is already used to extend the depleted region of the sensing diode for reducing the recombination possibility and the graded doping process is selected to form barriers for electrons moving to p-well and p-substrate. In addition, multiple sensing diodes in one pixel are also experimented for reducing the amount of charges recombined due to the diffusion path of the charge. However, the capacitance of the input node is also multiplied. It results a degradation of the charge to voltage conversion gain and single to noise ratio, which will be illustrated in the following sections.

3.2.2 Charge to Voltage Conversion Gain

In the pixel, the input signal is the collected charge and the output signal is a

voltage. The gain of the circuits is defined as charge to voltage conversion gain,

$$G_{q\to v} = \frac{\partial V_o}{\partial N_e},$$

where V_o is the output voltage, and N_e is the number of collected charge carries. The charge to voltage conversion gain defines the voltage various at output due to an electron. The unit is V/e^-.

For the 3T pixel, shown in Fig. 3-1, the collected charge is converted to voltage signal on the capacitance of input node C_{in} and then readout by the source follower T2. Suppose V_{in} is the voltage induced by the incident particle and q is the charge of an electron, then

$$\partial V_{in} = \frac{\partial N_e \cdot q}{C_{in}},$$

$$G_{q\to v} = \frac{\partial V_o}{\partial N_e} = \frac{\partial V_o}{\partial V_{in}} \frac{q}{C_{in}} = \frac{g_{m2}}{g_{m2} + g_{mb2}} \cdot \frac{q}{C_{in}}.$$

The charge to voltage conversion gain is proportional to the voltage gain of the amplifier and source follower in the described pixel, and is inversely proportional to the capacitance of input node. The input capacitance includes sensing diode capacitance, gate to source and source to substrate capacitances of transistor M1, equivalent input capacitance of the source follower, and other parasitic capacitance of input line. The sensing diode capacitance (C_d) is the domain capacitance. It is varied according to the collected charge and can be calculated from

$$C_d = WL \frac{C_j}{\left(1 + \frac{V_d}{V_{bi}}\right)^{MJ}} + 2(W + L) \frac{C_{jsw}}{\left(1 + \frac{V_d}{V_{bi}}\right)^{MJSW}},$$

and

$$V_{bi} = \frac{kT}{q} \ln \frac{N_{e,nw} N_{p,pw}}{n_i^2},$$

where C_j is the junction capacitance per unit bottom area, C_{jsw} is the junction capacitance per unit perimeter of layout, MJ and MJSW are the area and sidewall junction grading coefficients, respectively, and W and L are the dimensions of the rectangular diode implantation area. V_d is the bias voltage of the diode. It may change a little due to the incident particle and can be ignore. However, V_{bi} is the internal junction potential of the sensing diode. It may instantaneously increase nearly ten times when the particle path through. Hence, C_d varies nonlinearly with the input signal. As a result, the charge to voltage conversion gain is a nonlinear quantity.

3.2.3 **Noise**

During the whole design of MAPS, noise is one of the most important parameters to be considered. There are many sources of noise, such as environmental noise, quantization noise, electric noise, and so on. The environmental interferences such as temperature variation, electromagnetic fields, and so on can cause the fluctuation in the sensor output. When the output analogue signal is digitized, quantization noise is induced. The intrinsic electronic noise in the devices (thermal noise, shot noise and flicker noise) can be transferred to the output. In addition, power supply fluctuation and substrate coupling may lead noise on the output node. Generally, the noise can be reduced by proper layout, good circuit design, and signal processing. For example, the substrate and power supply couple noise can be suppressed by implementing appropriate guard rings and layout distribution. The intrinsic electronic noise is significantly considered in circuit design of MAPS. By applying CDS operation, the noise deriving from non-uniformity in the pixel array can be removed. In addition, the CDS operation reduces the influence of the flicker noise. Therefore, the flicker noise can be neglected in the analysis of overall noise.

The noise analysis is complicated due to the non-linearity charge to voltage conversion in MAPS. Here, the noise is separately analyzed for the three phases of operation, the reset, the integration, and the readout [21].

During the reset, the dominant noise source is the kTC noise of the switch-capacitor circuits composed by the transistor of M1 and the sensing diode. The average reset noise power can be expressed as

$$\overline{V_{n,rst}^2} = \frac{kT}{C_{in}},$$

where C_{in} is the capacitance of input node, k is the Boltzmann constant. Since in real systems the steady state of the diode bias voltage is usually not obtained due to the insufficient duration of the reset time, the average reset noise power is given by

$$\overline{V_{n,rst}^2} = \frac{1}{2}\frac{kT}{C_{in}}.$$

During the integration phase, the dominant noise is the shot noise due to the diode leakage current (i_{leak}). The mean square value of the noise sampled at the end of integration is given by

$$\overline{V_{n,\text{int}}^2} = \frac{q i_{leak}}{C_{in}^2}\tau_{\text{int}}.$$

During the readout, the source follower, composed of M2, M3, Mcol, and current source Mcur, is the main noise source. Suppose the capacitance of column line is C_1, the noise induced by each transistor can be calculated as,

$$\overline{V_{n,read,M2}^2} = \frac{2}{3}\frac{kT}{C_1}\frac{1}{1+\frac{g_{m,M2}(g_{ds,Mcol}+g_{ds,M3})}{g_{ds,M3}g_{ds,Mcol}}},$$

$$\overline{V_{n,read,M3}^2} = \frac{kT}{C_1}\frac{1}{g_{ds,M3}(1/g_{ds,M3}+1/g_{ds,Mcol}+1/g_{m,M2})},$$

$$\overline{V_{n,read,Mcol}^2} = \frac{kT}{C_1}\frac{1}{g_{ds,Mcol}(1/g_{ds,Mcol}+1/g_{ds,M3}+1/g_{m,M2})},$$

$$\overline{V_{n,read,Mcur}^2} = \frac{2}{3}\frac{kT}{C_1}g_{m,Mcur}(1/g_{ds,Mcol}+1/g_{ds,M3}+1/g_{m,M2}),$$

where $g_{ds,Mx}$ and $g_{m,Mx}$ are the output conductance and the transconductance of transistor Mx (x=2, 3, col, cur), respectively.

The total noise power at the output stage of the pixel is the sum of the previous noise components:

$$\overline{V_{on}^2} = \overline{V_{n,rst}^2} + \overline{V_{n,\mathrm{int}}^2} + \overline{V_{n,read,M2}^2} + \overline{V_{n,read,M3}^2} + \overline{V_{n,read,M\mathrm{col}}^2} + \overline{V_{n,read,M\mathrm{cur}}^2}.$$

In fact, the kTC noise during reset period $\overline{V_{n,rst}^2}$ can be removed by applying CDS signal processing technique. In addition, at room temperature, the mean value of the leak current i_{leak} is in order of several femtoampers. As the development of MAPS, the integration time reduces. This part of noise $\overline{V_{n,\mathrm{int}}^2}$ is not significant for an integration time of a few milliseconds. The main noise source is during the readout.

The equivalent input noise and the signal to noise ration define the minimal signal that are able to detect by MAPS. Equivalent noise charge (ENC) is used to evaluate the equivalent input noise. It is defined as

$$ENC = \frac{\sqrt{\overline{V_{on}^2}}}{G_{q\to v}}.$$

The unit of ENC is e^-. Consequently, the signal to noise ratio (SNR) can be calculated as,

$$SNR = \frac{Q_c}{ENC} = \frac{Q_c \cdot G_{q\to v}}{\sqrt{\overline{V_{on}^2}}}.$$

SNR can be increased by reducing the readout noise and increasing the charge to voltage conversion gain.

In the test with soft X-ray source (^{55}Fe) and minimum ionizing particles (15 GeV/c pions), the individual pixel ENC of MIMOSA I is below 20 electrons and the SNR for both 5.9 keV X-rays and MIP is in order of 30.

3.2.4 **Spatial Resolution**

One of beneficiations from MAPS technology is the small spatial resolution. The spatial resolution is a function of the pixel pitch in MAPS. The actual resolution is generally much smaller than the pixel pitch. The reason is that more than one pixel will be fired due to one event, and the gravity center of hitting can be calculated from a cluster of pixels. The actual resolution is related with the quantization and chip design. Fig 3-5 shows the resolution varying with number of ADC bits in MIMOSA I. As the increase of the number of ADC bits, the resolution gets higher. For most of our design, the spatial resolution follows similar dependence on pixel pitch for the same quantization.

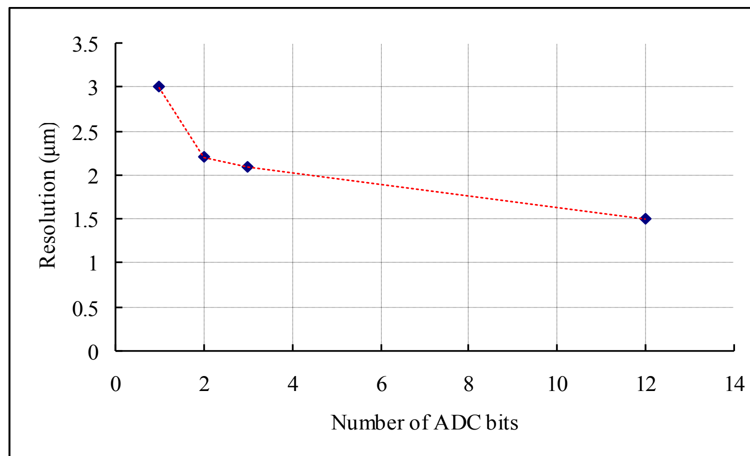


Fig. 3-5. Resolution versus with number of ADC bits (MIMOSA I) [39]

Pixel pitch between 20 μm and 40 μm are usually designed by compromising the spatial resolution, the detection area and the number of channels. The spatial resolution dependent on the pitch size was tested in one of chips (MIMOSA 9). Fig. 3-6 shows the test results from MIMOSA 9. A 12bit ADC is used for readout. The spatial resolution σ can be approximated with

$$\sigma \approx 0.075p,$$

where p is the pixel pitch.

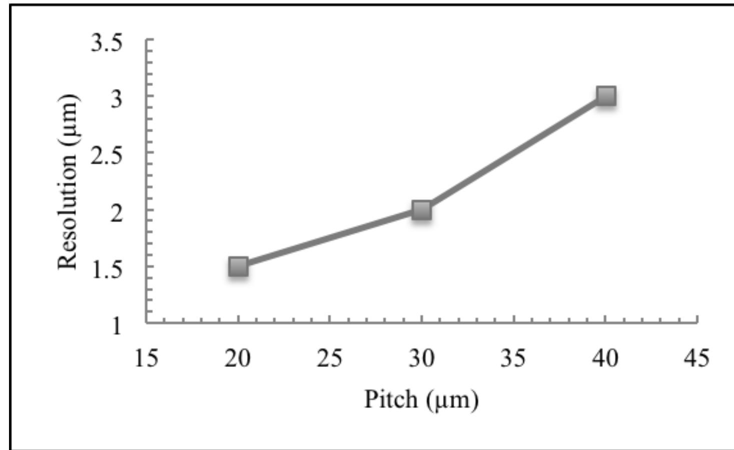


Fig. 3-6. The spatial resolution of MAPS as a function the pixel pitch (MIMOSA 9).[40]

In the fast readout MAPS (presented in Chapter 4), one bit on-chip ADC was realized for high-speed readout. The spatial resolution dependent on pixel pitch is derived from experiments as

$$\sigma = \frac{p}{\sqrt{12}} = 0.289p.$$

For a pixel pitch of 20 μm, the spatial resolution can achieve about 1.5 μm and 5.8 μm with analogue output and digital output respectively.

3.2.5 Time Resolution

Time resolution is the time difference between successive readout frames. It equals to the readout time of one frame in most cases. In MIMOSA I, the time resolution is 200 ms. With the development of MAPS design, the time resolution has achieved 200 μs in fast readout MAPS and about 25 μs in MAPS using 3D integration technology (illustrated in Chapter 5).

3.2.6 Detection Efficiency

In high energy physics experiment, the expected detection efficiency is higher than 99.5%. The detection efficiency is related to the cluster finding algorithm. A cluster generally can be a 3×3 pixel array, where the center pixel is supposed to be hit by a particle. A hit is found if SNRs of the center pixel and the around 8 pixels are higher than respective predefined thresholds for them. Fig. 3-7 shows the detection efficiency as a function of the thresholds (the cuts) applied on the center pixel signal and search window radius, which is the radius of a cluster. As the increase of the

threshold, the detection efficiency decreases. If a low signal threshold is applied, the noise should be small enough so that it could not be treat as a signal.

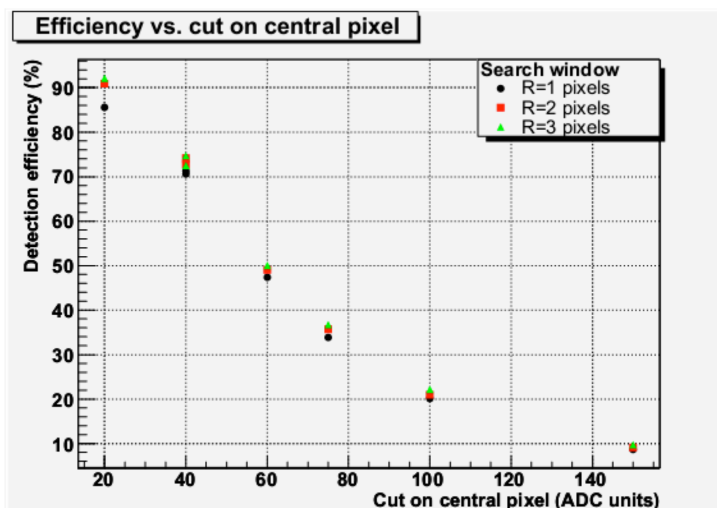


Fig. 3-7. Detection efficiency as a function of the cuts applied on the pixel signal and search window radius.[41]

3.2.7 Radiation Tolerance

In the high energy physics environment, radiation background can not be ignored. MAPS have relatively high radiation tolerance comparing to CCD sensors. However, the radiation effects described in Chapter 2 will degrade the performance of MAPS. By proper design and layout, the degradation can be reduced or removed. The detail study and improved design will be illustrated in the follow sections.

3.3 Radiation Hard Study of MAPS

In MAPS, pixel array takes more than 90% of the total area. The weak input signal makes the pixel diode sensitive to both ionizing and non-ionizing radiation. The readout circuits are not sensitive to non-ionizing radiation. The total ionizing dose effects didn't lead obvious performance degradation of readout circuits when the AMS 0.35 μm process is selected due to the thin gate oxide. Therefore, the pixel design is mainly considered based on the basic MAPS architecture. The influence of epitaxy thickness, sensing diode density, radiation hard layout and advanced circuit topologies are studied.

3.3.1 Introduction to SB pixel

In the study of radiation tolerance of MAPS, pixel especially the charge collecting diode is concerned significantly. A self-biased (SB) pixel proposing specially for particle tracking is also studied except the 3T pixel in Fig 3-1. Fig 3-8 shows the structure of SB pixel. The primary 3T pixel requires reset transistor and reset timing consequence for controlling. The SB pixel utilizes a diode to complement the leakage current continuously. Thus, the SB pixel can simplify the operation of the MAPS and reduces the layout plan of control lines.

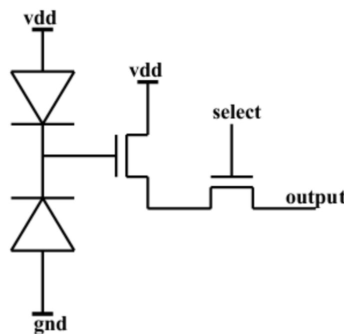


Fig. 3-8. Scheme of a self-biased pixel.

3.3.2 Primary Radiation Hardness Evaluation

3.3.2.1 Radiation Sources

In order to study the different radiation damage effects on MAPS, proton, neutron and soft X-rays irradiation tests were performed for study of total radiation effects, non-ionizing effects and ionizing effects respectively.

Proton irradiations are performed by 30 MeV proton beam from the cyclotron at Karlsruhe Forshungszentrum, Germany. The maximum proton fluence in the series of tests was set to 5×10^{11} p/cm^2. It corresponds to the ionization dose of about 50 krads and the atomic displacement effect equivalent to 10^{12} neutrons/cm^2.

Neutron irradiations are executed by a fast neutron beam with peak of 1 MeV. In order to separate the bulk effects and interface states modification due to ionization, the ionization dose from the background of high energy photons should be keep in a negligible level. The ionizing dose corresponding to a neutron fluence of 6×10^{11} was measured to be below 1 krad.

Soft X-ray irradiations are using a 10 keV X-ray photon source. The displacement effects of such soft X-ray photons could be negligible. The soft X-ray

irradiation tests were aimed to evaluate the signal decrease and leakage current increase due to ionizing effects but not displacement damage.

The study and calibration of the charge collection, leakage current and signal distribution were done using low energy X-ray photons from ^{55}Fe source as an excitation source.

3.3.2.2 Tested Chips

Three prototypes following the presented principle were tested. The first device MIMOSA I was fabricated in a 0.6 um process with an epitaxial layer of about 14 um, and the second device MIMOSA II was fabricated in 0.35 um process with epitaxial layer of less than 5 um. The third one is a test structure in MIMOSA 3, which was fabricated in a 0.25 um process with shallow trench isolation (STI) and twin tubs set in an epitaxial layer of about 2 um.

MIMOSA I has been described in Chapter 3.1 and Chapter 3.2.

The architecture of MIMOSA II is similar with MIMOSA I. The main difference is that two separate readout lines with two current sources are switched alternatively to the output amplifier in MIMOSA II. The two readout lines can work in a pipeline mode. Combined with an optimized design of output amplifier, the readout frequency of MIMOSA II achieved 25 MHz, while the readout frequency is 5 MHz in case of MIMOSA I. Especially for radiation study, radiation tolerant layout rules are applied for all the NMOS transistors in pixel of MIMOSA II. Fig. 3-9 shows the layout. The enclosed gate eliminates the thick field oxide existing at the edges of transistor. Thus, the leakage paths between drain and source induced by radiation are avoided. The leakage path on the gate edge will not cause any problem since the two side of the gate edge is in fact the same potential.

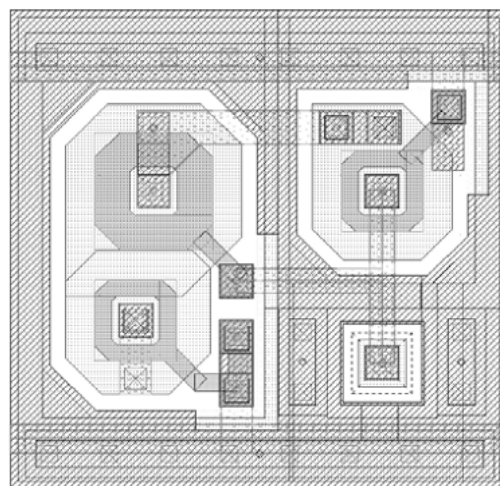


Fig. 3-9. Single pixel layout with enclosed NMOS transistors and n-well/p-epi charge sensing diode

The test structures in MIMOSA 3 consist of only diodes in the pixel. The array of diodes is shorted to one output pad parallel. The layout of the diodes is identical to the layout in a pixel excluding some filling pattern on top for passing design rule check (DRC). Two structures were tested. One is a diode array from the standard pixel as Fig 3-9. The other is a diode array from a pixel with poly-silicon belt around the diode, shown in Fig 3-10.

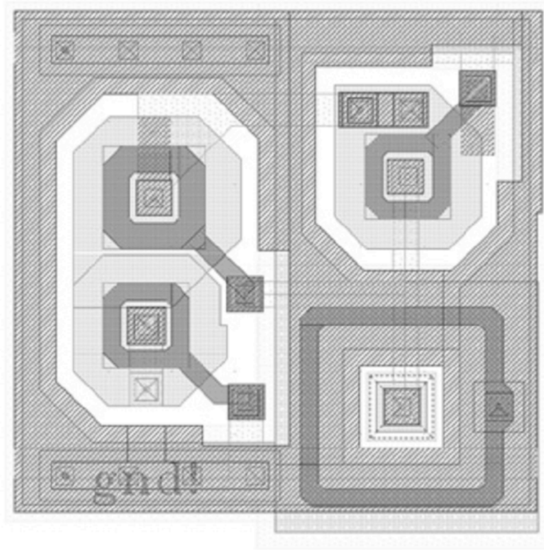


Fig. 3-10. Single pixel layout with enclosed NMOS transistors and n-well/p-epi charge sensing diode designed for radiation hardness test with poly-silicon belt around the diode.

3.3.2.3 Test Results

The major effect anticipated on a pixel consists of non-ionizing effects and ionizing effects. The bulk damage induced by non-ionizing radiation lead a decrease of minority carrier's lifetime. The minority carrier's lifetime is estimated to be about 10 μs for the lightly doped (10^{15} cm^{-3}) p-epi layer of MAPS. The charge collection time through thermal diffusion is in order of 100 ns in the undeleted epitaxial layer of MAPS. Therefore, the decrease of minority carrier's lifetime may influence the charge collection efficiency, and then decrease the signal amplitude. In addition, space charges at the Si/SiO_2 interface resulted by the ionizing effects may induce increasing leakage currents of diode and transistors. Therefore, the charge collection and leakage currents are mainly studied.

(1) Charge collection

The consequences of irradiation were calculated from the signal generated by the

^{55}Fe X-ray source. There are two peaks in the signal distribution (see Fig. 3-13). The first high peak corresponds to the most probable collected charge. The second low peak is thought to be corresponding to charge collection efficiency of 100%. The position of the second low peak was used for the calculation of charge collection efficiency after irradiation. The test results with proton, neutron and soft X-ray sources are shown in Fig. 3-11, Fig. 3-12 and Fig. 3-13, respectively.

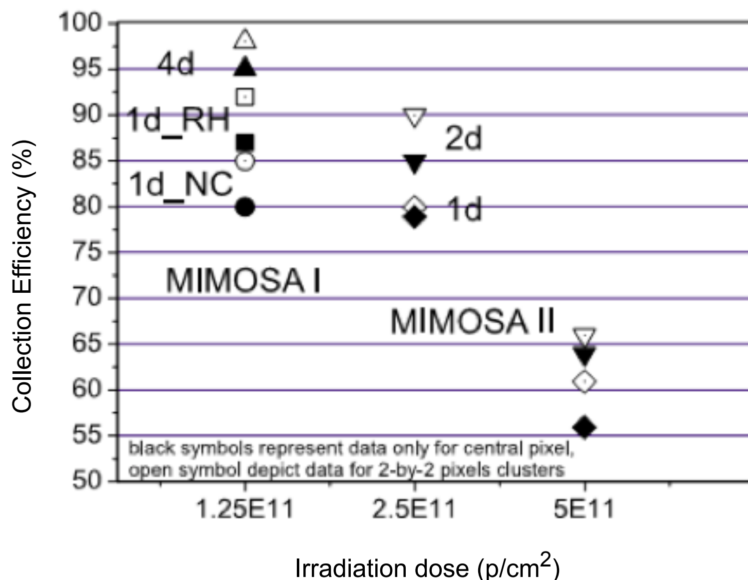


Fig. 3-11. Collected charge (normalized to the initial sample measurements) after irradiation with protons for MIMOSA I and MIMOSA II, for different pixel configuration implemented inside.[42]

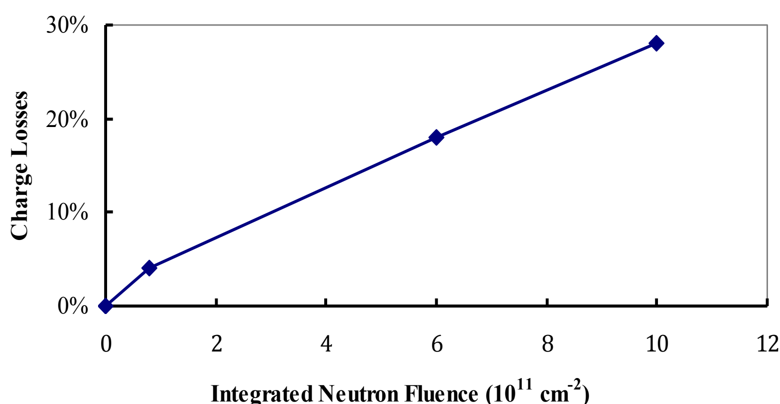


Fig. 3-12. Collected charge losses as a function of neutron fluence[42]. (MIMOSA I)

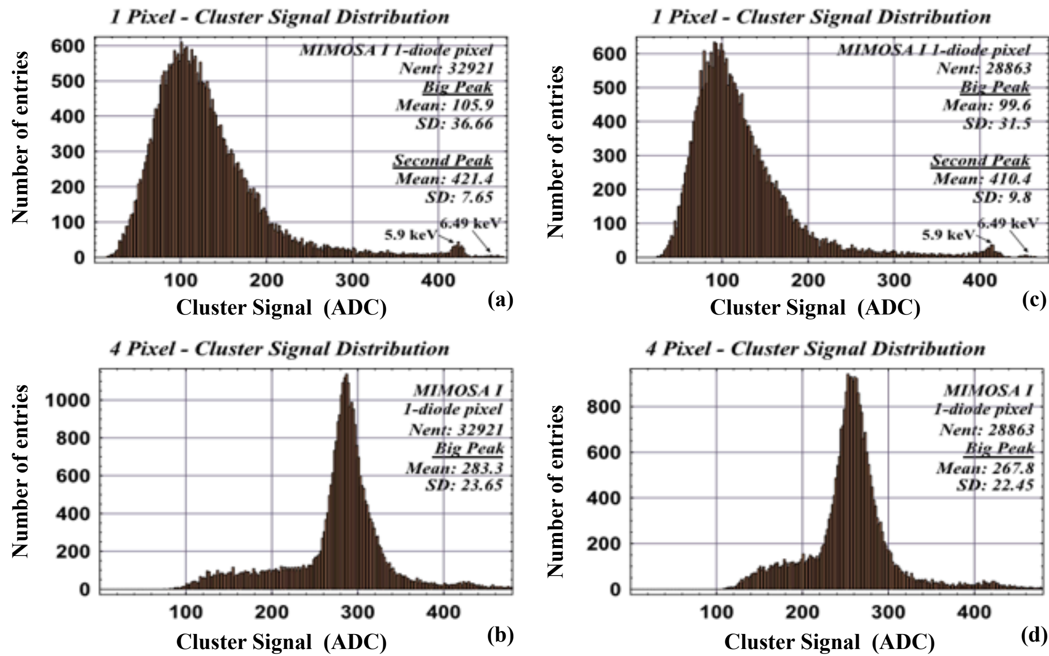


Fig. 3-13. Sensor response to a ^{55}Fe X-ray source. The signal pulse-height distribution is shown before (a,b) and after (c,d) a dose of 100 kRads 10keV photons. Plots (a) and (c) corresponds to the seed pixel. Plots (b) and (d) corresponds to a cluster of 4 pixels including the seed one [42]. (MIMOSA I)

Fig. 3-11 shows the charge collection efficiency after irradiation with 30 MeV protons for MIMOSA I and MIMOSA II, namely the results of both ionizing effects and atomic displacement. The loss of charge is up to 45% after a fluence of 5×10^{11} protons/cm^2, which corresponds to neutron fluence of 10^{12} cm^{-2} and ionizing dose of 50 kRad. In Fig 3-12, the collected charge losses approach 30% after a fluence of 10^{12} neutron/cm^2. In Fig 3-13, the charge losses are about 6% after ionizing radiation dose of 100 kRad.

(2) Leakage current

Radiation induced changes of leakage current are also tested under proton, neutron and soft X-ray irradiation sources. The corresponding results are shown in Fig. 3-14, Fig. 3-15 and Fig. 3-16, respectively.

The radiation induced leakage currents are evaluated in several ways. In Fig. 3-14 and Fig. 3-16, the results are derived from the pixel output by observing the voltage drop. In Fig. 3-15, ENC is calculated since it is one of main results related with the increase of leakage current. However, the voltage drop at pixel output and changes of ENC induced by the leakage currents are response of whole pixel, the results may be affected by the compensation of leakage currents of the diode and the

reset transistor or any other connected leakage paths. Therefore, the test structures were designed to observe the diode leakage currents directly. Fig 3-17 shows the results of the irradiation and the annealing effects.

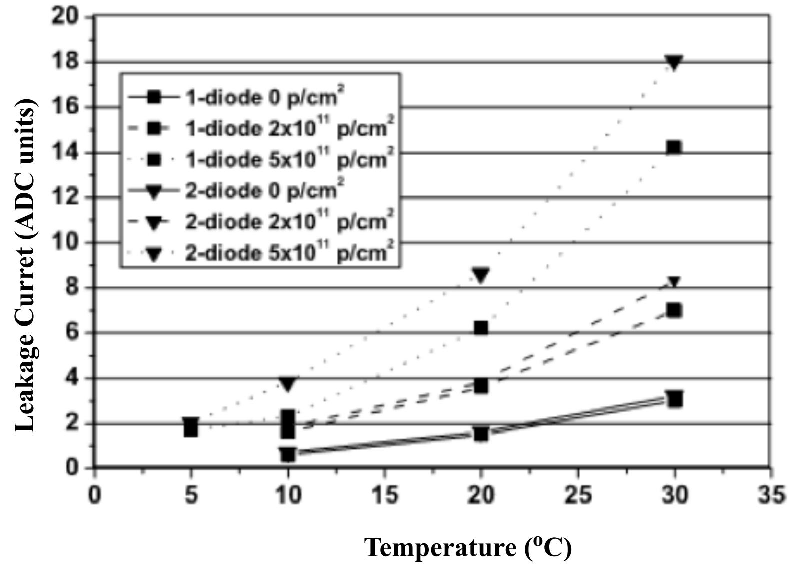


Fig. 3-14. Increase of leakage current after irradiations with 30 MeV/c protons measured as a function of temperature [42]. (MIMOSA II)

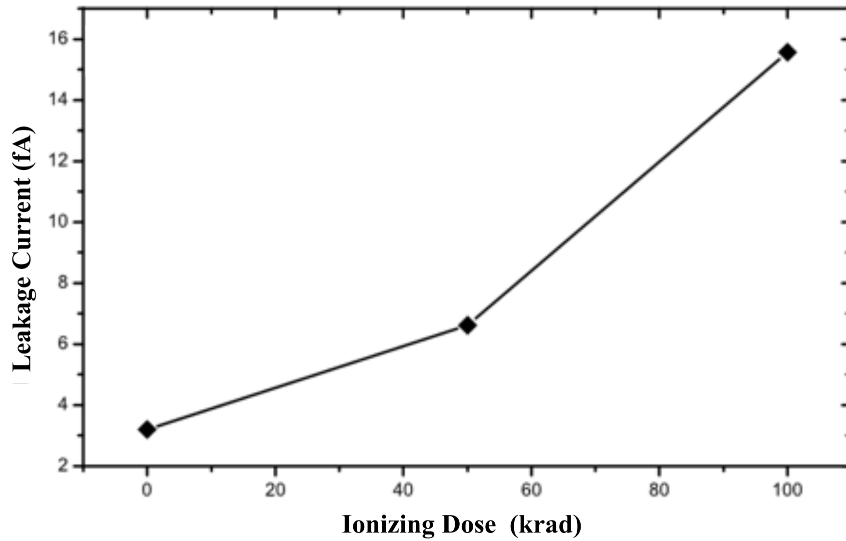


Fig. 3-15. Variation of the leakage current as a function of the irradiation dose with 10 keV photons (MIMOSA I prototype, measured at 0 °C).[42]

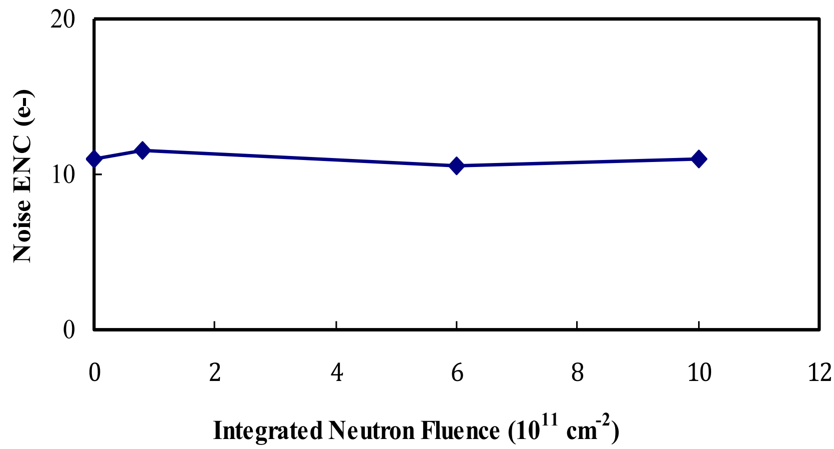


Fig. 3-16. Noise as a function of neutron fluence [42]. (MIMOSA I)

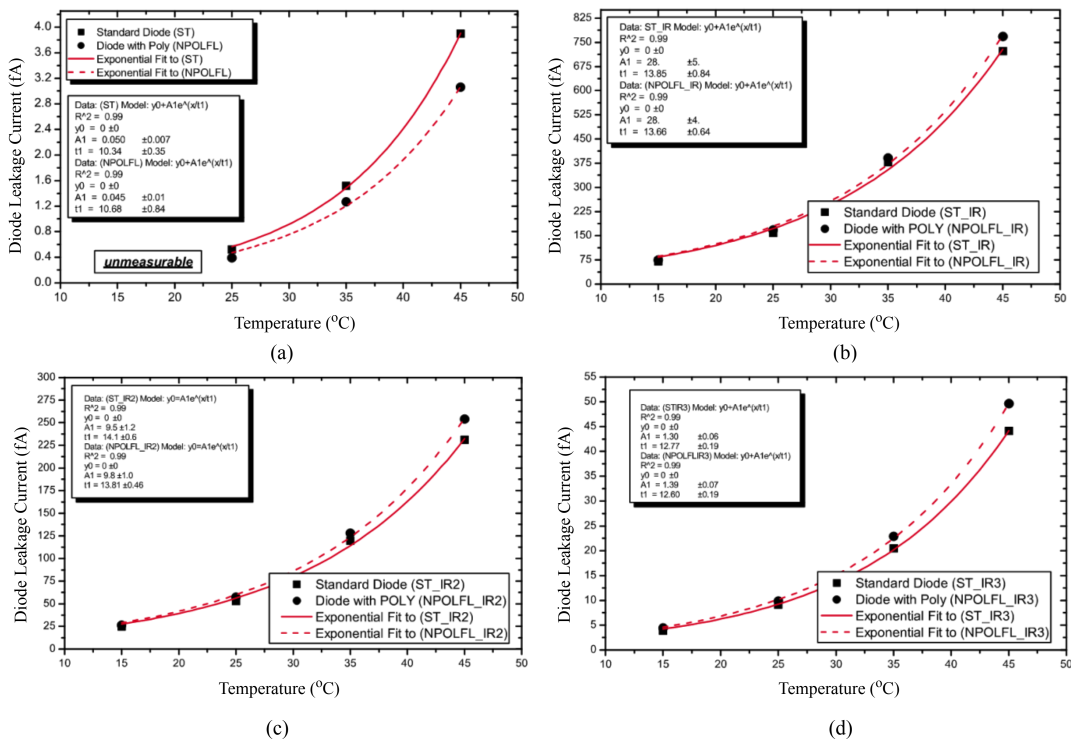


Fig. 3-17. Variation of the leakage current before (a) and after 10 keV photons irradiations as a function of temperature (MIMOSA 3). The post irradiation measurements were done 24 h after irradiation (b), after 3 weeks of room temperature annealing (c) and after another 24 h annealing at 100 ^{o}C (d). [42]

Comparing all the test results, the influences of proton and photon irradiation are obvious, while the neutron irradiation results in almost no change on the ENC of MIMOSA I. If the neutron irradiation effects can be ignore, MIMOSA II shows equivalent tolerance with MIMOSA I by comparing the leakage currents in Fig. 3-14 and Fig. 3-16. With 50 kRad irradiation, the leakage current of MIMOSA I increase more than two times at 0 ^{o}C, while there was almost two to four time increase on the leakage current of MIMOSA II at different temperature for equivalent irradiation dose of 50 kRad, namely 5×10^{11} protons/cm^2. It indicates that the leakage currents are also induced by the diode since enclosed NMOS layout is used in MIMOSA II. It is quite necessary to test the leakage currents of sensing diode. Since leakage current of a single diode is very small, a test structure of a diode array was constructed in MIMOSA 3. The test results of the structure (Fig. 3-17) show about 200 times increase of diode leakage currents with irradiation dose of 800 kRad. In fact, the complete sensor only exhibited an increase factor of 10. Fig. 3-17 also shows a strong annealing effect for irradiation. Although the diode with poly-silicon belt around exhibits smaller leakage current than standard one, it shows larger leakage current than standard one after annealing.

3.3.2.4 Conclusion

During the primary evaluation, we can conclude as follow. Firstly, the atomic displacement is the main reason of charge losses, while the ionizing radiation effects are the domains of leakage current increase. Moreover, the charge losses due to irradiation are quite considerable. Thirdly, the leakage currents of the sensing diode still should be significantly studied.

3.3.3 Non-ionizing Radiation Hard Study

The non-ionizing radiation effects mainly lead to the decrease of charge collection efficiency. The initial charges are mainly dependent on the thickness of epitaxial layer. The charge thermal diffusion and collection are related with the distribution of sensing diode. As the decrease of charge collection efficiency, MAPS generally demonstrate the decreases on signal to noise ratio and detection efficiency. Therefore, the non-ionizing radiation is studied by testing the signal to noise ratio and detection efficiency with the different diode size, pixel pitch, thickness of epitaxial layer under varied neutron irradiation dose in order to select the proper value for radiation hard.

In addition, the random telegraphy noise of CMOS sensor under high dose neutron or proton irradiation has been reported in many articles [36-38]. It was also studied for MAPS in the past.

3.3.3.1 Epitaxial Layer Thickness

Thickness of epitaxial layers provided in standard CMOS processes is quite limited. Several MIMOSA chips are selected for this study. The detail information is listed in Table 3-1. The compared chips are based on 3T pixel if there is no declare of SB pixel. In order to study the dependence on epitaxial layer thickness, the charge collection efficiency, the noise and the signal to noise ratio of these chips are compared.

Table 3-1 List of compared chips

Chip name	Process (μm)	Thickness of epi-layer (μm)	Diode size (μm^2)	Pixel pitch (μm)
MIMOSA I	0.6	14	3.1 × 3.1	20
MIMOSA II	0.35	4	1.7 × 1.7	20
MIMOSA 9	0.35	11	4.3 × 3.4	20
MIMOSA 15	0.35	11	4.3 × 3.4	20

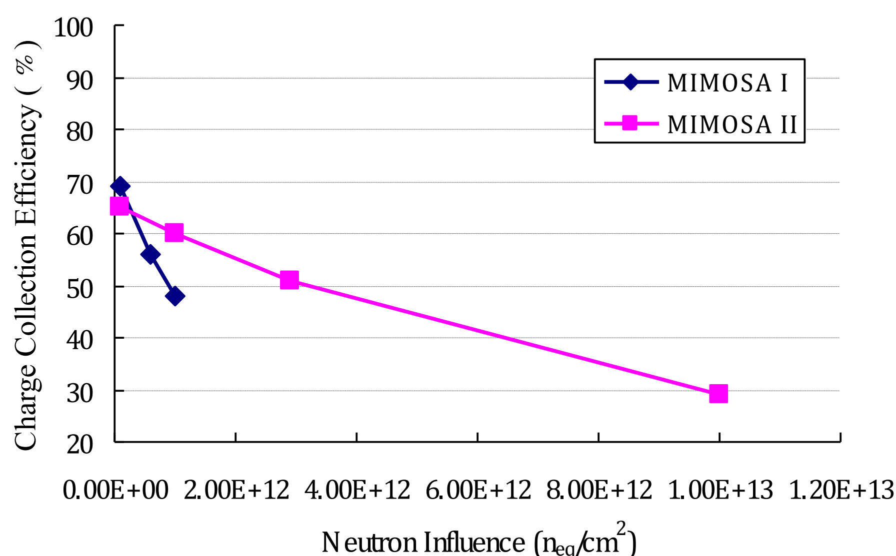


Fig. 3-18. Charge collection efficiency of MIMOSA I and MIMOSA II as a function of the neutron fluence. [40]

The charge collection efficiency of MIMOSA I and MIMOSA II was measured for groups of four pixels detecting the charge generated with the photons of a ^{55}Fe-source. Fig. 3-18 shows the results, which is taken from [40]. The initial charge

collection efficiency of MIMOSA I is higher than MIMOSA II before irradiation. The result is mainly caused by the size of diode. While, the charge collection efficiency of MIMOSA I decreases more sharply than that of MIMOSA II. That can be explained that the lifetime of charges is decreased as the increase of the radiation dose, and the charges are collected much faster in thinner volume, where the diffusion paths are shorter.

The noise of MIMOSA I, MIMOSA II and MIMOSA 15 are compared in Fig. 3-19. In most case, the equivalent noise doesn't change a lot. However, the noise in MIMOSA 15 demonstrates irregular behavior at 20 °C. Same tests were also done for a pixel array based on SB-pixel in MIMOSA 15 at 20 °C. The noise increases lineally as the increase of radiation dose. The noise still cannot be clarified according to these tests.

Fig. 3-20 shows the signal to noise ratio of MIMOSA I, MIMOSA II, MIMOSA 9 and MIMOSA 15 as a function of irradiation dose. The signal to noise ratio of MIMOSA I and MIMOSA II are estimated from the tests with ^{55}Fe source. MIMOSA 9 and MIMOSA 15 were tested on a ~ 5 GeV electron beam at DESY. The minimum SNR required for a reasonable detector is estimated according to the data from MIMOSA II detector tested in a ~120 GeV pion beam of the CERN-STS. The test shows that the detector delivers a sufficient detection efficiency (> 95 %) for MIPs after an irradiation dose of 1.2×10^{12} n_{eq}/cm^2. In Fig. 3-20, the SNR of MIMOSA II decreases most slowly. However, MIMOSA II just maintains available detection efficiency until irradiation dose of 1.2×10^{12} n_{eq}/cm^2 due to the smallest initial SNR. The MIMOSA 9 and MIMOSA 15 chips show the radiation tolerance higher than 2×10^{12} n_{eq}/cm^2.

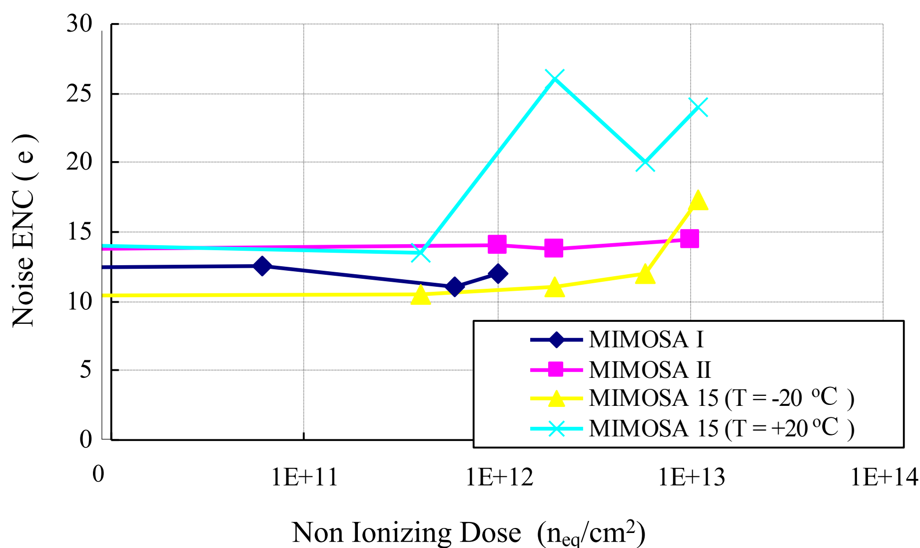


Fig. 3-19. Noise as a function of the irradiation dose.[40]

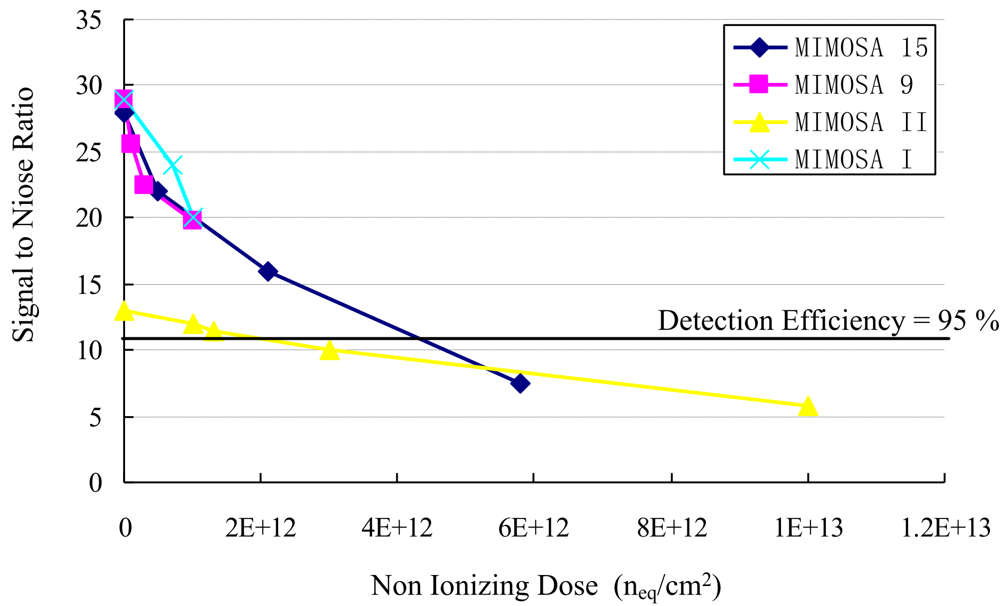


Fig. 3-20. Signal to noise ratio as a function of irradiation dose.[40]

3.3.3.2 Diode Density

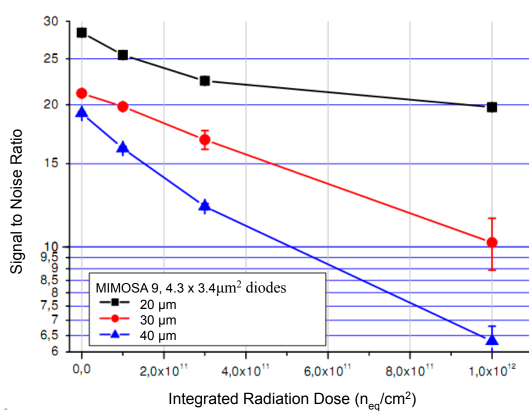
In MIMOSA I and MIMOSA II, the density of the sensing diode is varied by hosting two and four diode in a pixel. However, it also leads to a higher input capacitance and higher pixel noise. Chip MIMOSA 9 was designed with various pixel and diode size. It is interesting for study the variation of signal to noise ratio and detection efficiency as a function of the irradiation dose and the density of sensing diodes.

In the MIMOSA I and MIMOSA II chips, the density of sensing diode is varied by hosting two or four parallel diodes in a pixel. The four-diode pixel retains the best charge collection efficiency after irradiation of 10^{12} N_{eq}/cm^2 [43] due to the shortest diffusion paths. However, the total input capacitance of the diodes is increased and additional noise (such as shot noise of the additional diodes) is induced. Consequently, charge to voltage conversion ratio is reduced and the equivalent input noise charge is increased.

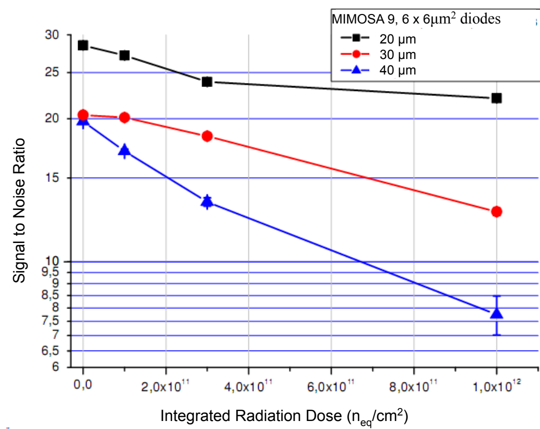
With another approach, various pixel sizes are implemented and tested in the MIMOSA 9. Some of them are selected for analysis of the radiation tolerance dependence on the pixel pitch. The thickness of the epitaxial layer is about 11 µm. The pixel pitches include 20 µm, 30 µm, and 40 µm. For each pixel pitch, a small diode and large diode were implemented separately. The small diode size is 3.4 × 4.3 µm^2. The large diode size is 5 × 5 µm^2 in pixel pitch of 30 µm, and is 6 × 6 µm^2 in pixel pitches of 20 µm and 40 µm. The pixel arrays are based on the SB pixel. Table 3-2 shows the list.

Table 3-2 List of some pixel matrices in MIMOSA 9

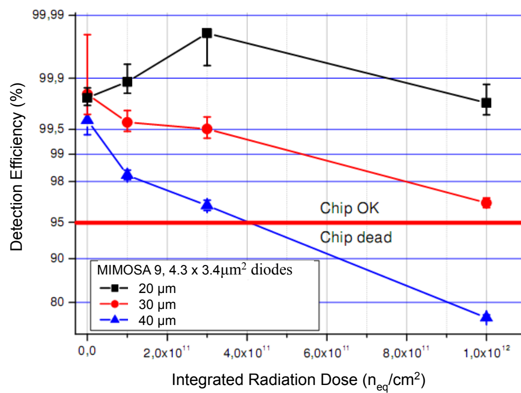
Pixel array	Diode size (μm^2)	Pixel pitch (μm)
64 × 32 SB-Pixels	4.3 × 3.4	20
64 × 32 SB-Pixels	6 × 6	20
32 × 16 SB-Pixels	4.3 × 3.4	30
32 × 16 SB-Pixels	5 × 5	30
32 × 16 SB-Pixels	4.3 × 3.4	40
32 × 16 SB-Pixels	6 × 6	40



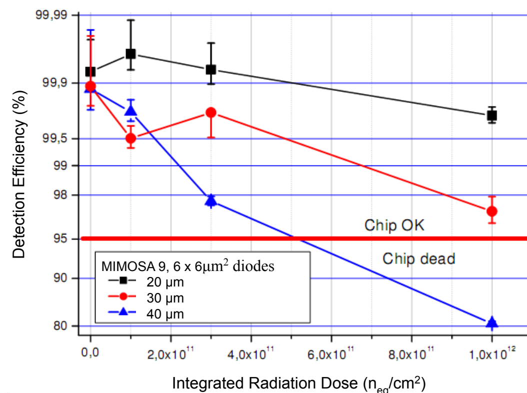
(a)



(b)



(c)



(d)

Fig. 3-21. Signal to noise ratio (a,b) and detection efficiency (c,d) of MIMOSA 9 as a function of the radiation dose, the pixel pitch and the diode size. Note that the big diode size of the pixel with 30 μm pitch is 5 × 5 μm^2. The data was taken at T= -20 °C and f_{clk} = 2.5 MHZ. [40]

Fig. 3-21 shows the signal to noise ratio and detection efficiency as a function of the irradiation dose up to 1×10^{12} n_{eq}/cm^2. The measurements were done with a beam test on a ~ 5 GeV electron beam at DESY (Hamburg). The smallest pixel pitch demonstrates best radiation tolerance. If the detection efficiency is required higher than 95 % with irradiation dose 1×10^{12} n_{eq}/cm^2, the pixel pitch of 20 µm or 30 µm are available. The bigger diodes also show a little positive influence.

The measurements of irradiation dose above 1×10^{12} n_{eq}/cm^2 were done on MIMOSA 15. It is a chip optimized for ionizing radiation with radiation hard pixel. The thickness of epitaxial layer is 11 µm, the pixel pitch of the tested device is 30 µm, and the diode size is 3.4×4.3 µm². Fig. 3-22 shows the signal to noise ration and the detection efficiency as the radiation dose up to 5.8×10^{12} n_{eq}/cm^2. The beam test was done at - 20 °C and an integration time of 0.7 ms in order to reduce the shot noise. The detection efficiency is above 99 % after an irradiation dose of 2.1×10^{12} n_{eq}/cm^2.

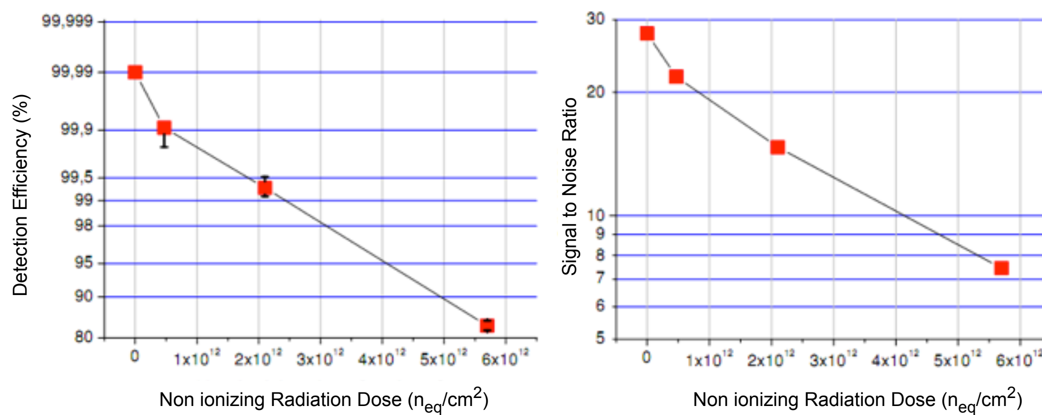


Fig. 3-22. Signal over noise ratio and detection efficiency of MIMOSA 15 as a function of the radiation dose. (T = - 20 °C, τ_{int} = 0.7 ms.)[40]

3.3.3.3 Random Telegraphy Signal Noise

Random telegraphy signal (RTS) is characterized with its amplitudes varied randomly between two or more discrete levels. In 1990s, H. Hopkins and G.R. Hopkinson observed and firstly reported the RTS in CCD sensor due to proton irradiation [44, 45]. The radiation-induced RTS is different with the RTS observed in small geometry MOS transistors. The later is generally attributed to the degradation of flicker noise of the transistors [46]. The radiation-induced RTS in CCD and CMOS sensor presents random leakage current fluctuations in the sensing elements. Some researches reported that this RTS is related with the non-ionizing radiation induced atom displacement in the bulk [37, 38, 47]. An individual crystal defect changes its charge state by electron/hole capture and emission processes. Consequently, it leads to a current modulated by a change of an individual quantum state in the material. There are arguments for the hypothesis that the RTS in MAPS is caused by a

modulation of the leakage current of the collecting diode. Although it remains to be proven, this hypothesis is used in the present analysis.

The RTS was observed on MIMOSA II irradiation with 10^{13} n_{eq}/cm^2. Fig. 3-23 shows the details. The upper of the figure is a representative pixel showing RTS. The output signal of a pixel after CDS over the time is presented. One observes the output signal to jump between three different levels. The corresponding currents of these levels are ~ 25 fA, ~ 45 fA and ~ 60 fA. The noise of the pixel distributes in the levels of 30 e^-, 31 e^- and 33 e^-. The noise is not strongly dependent on the current value.

Although not having a strong impact on the equivalent noise charge, RTS may have serious consequence on the detection of MAPS. In the downer of Fig. 3-23, the amount of hits, indicated within 2×10^4 events, is shown as a function of pixel number. Few tens of hits were expected for each pixel while the number of indications reaches values above 10^4. We can observe that the amplitude of the RTS has exceeded the discrimination threshold. A pixel generating strong RTS becomes a hot pixel. On one hand, the RTS requires additional calculation to be separated. On the other hand, large amount of hot pixels results in fake hits and reduces the detection efficiency of the chip.

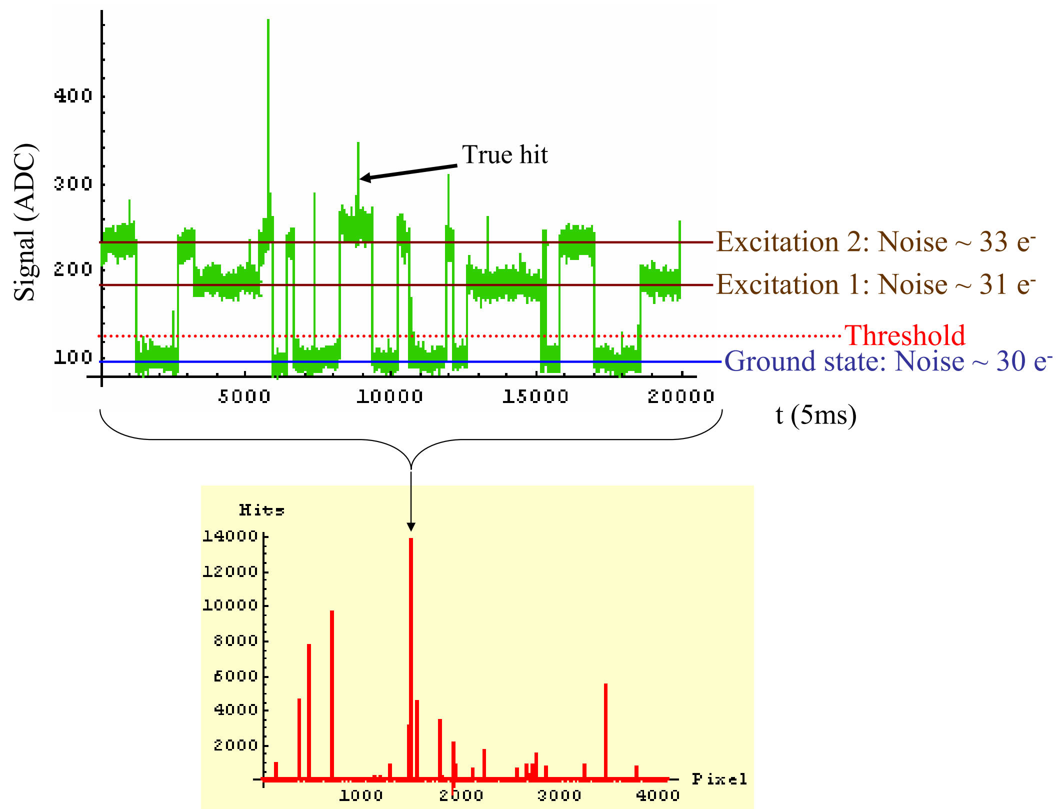


Fig. 3-23. Random Telegraphy Signal (RTS) on MIMOSA II after an irradiation with 10^{13} n_{eq}/cm^2 at a temperature of 40 ˚C and an integration time of 3.3 ms. [40]

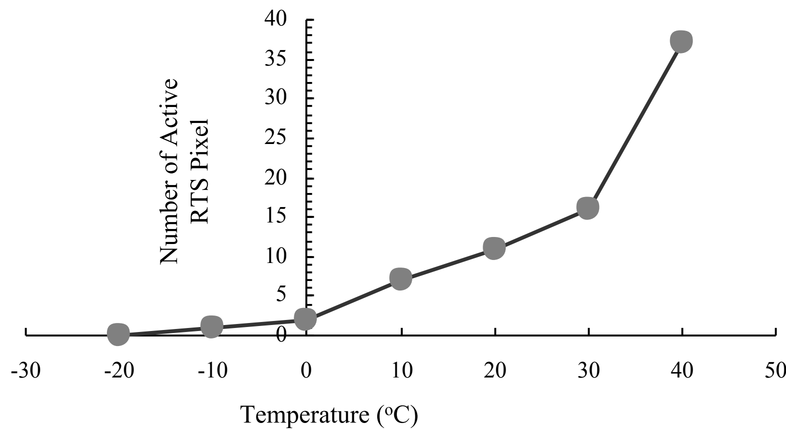


Fig. 3-24. The number of RTS-pixels as a function of temperature.[40]

In most case, the electric circuits perform better at low temperature. The temperature dependence of RTS is shown in Fig. 3-24. The data was taken on MIMOSA II irradiated with 10^{13} n_{eq}/cm^2 with the integration time of 3.3 ms. A RTS pixel is defined as active, if its indicated hit rate is more than five standard deviations above the mean hit rate of all pixels. The results indicate the amount of significant RTS pixels increase strongly with temperature. As the temperature is reduced to – 20 ^oC, the amplitudes of RTS reduced to the order of thermal noise. This forms one option to overcome the unwanted effects of RTS and the hot pixels become operational again.

As the SB pixels adapt themselves efficiently to the leakage current, the use of SB pixels is helpful to overcome the RTS. In fact, RTS hasn't been observed for the SB pixels. But it remains to be worked out if the use of SB pixels alone is sufficient to overcome the RTS problems, namely whether the time that the pixel requires to adapt itself to the new leakage current is on a comparable time scale of RTS fluctuations.

3.3.4 Ionizing Radiation Hard Design

As the previous study, the main result of ionizing radiation is the increase of the leakage currents of sensing diode. Therefore, specified layout designs are discussed for reducing the influences firstly. In addition, considering that the increase leakage current finally results in an increase of integration noise, the affects of the integration time are also studied for ionizing radiation.

3.3.4.1 Radiation Hard Layout

Under long-term irradiation, positive charges may be deposited in SiO_2. When the charges are accumulated to a certain level, the circuit functions and performances may be affected. Fig. 3-25 shows a probable distribution of positive charge deposited

in a 3T pixel. Leakage current path between n-well and n-diffusions of NMOS transistor is formed at the Si/SiO_2 interface. In addition, interface charges may be recombined with the electrons that are expected to be collected by n-well.

The main idea of the radiation hard diode design is to cut-off the leakage paths and to reduce the number of accumulated positive charges at the Si/SiO_2 interface. Firstly, a p-diffusion guard ring can be implemented around the sensing diode for cutting the leakage path between n-well and n-diffusions of NMOS transistor. In addition, the radiation induced positive charge should not stay at the surface of active region of the sensing diode. An easy way is to use a negative poly or metal shielding to keep the radiation induced charge away from the diode active surface. Fig 3-26 shows this solution. However, this method is not very efficient in the irradiation test. The reasons are contributed that the electronic field induced by poly on the top of thick oxide is weak, and a lot of holes are accumulated during irradiation inside thick oxide. Fig. 3-27 shows another strategy, replacing the thick field oxide with thin gate oxide. For a sub-micron process, the positive charges induced by irradiation are quite limited in the thin gate oxide.

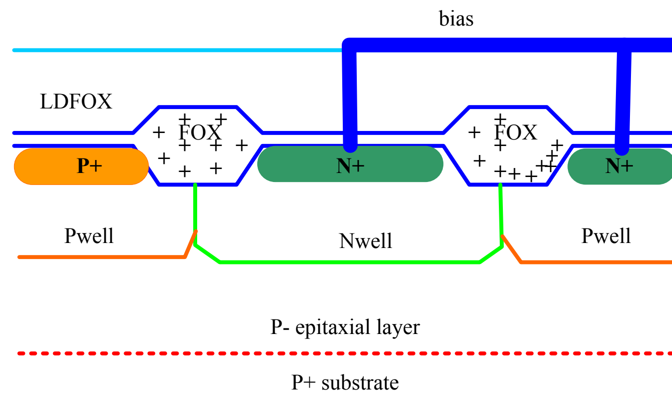


Fig. 3-25. The positive charge built in standard pixel

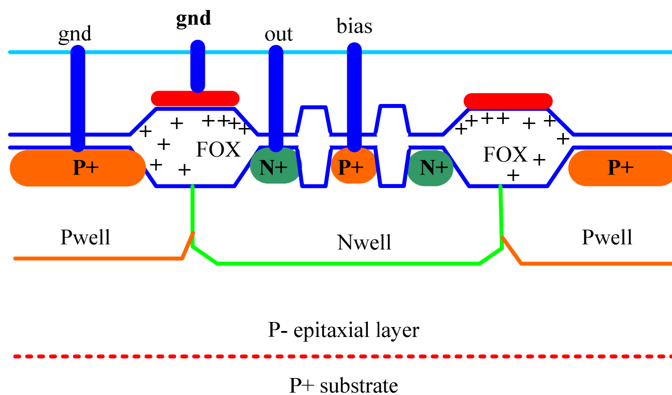


Fig. 3-26. A proposed radiation hard pixel with dummy poly shielding

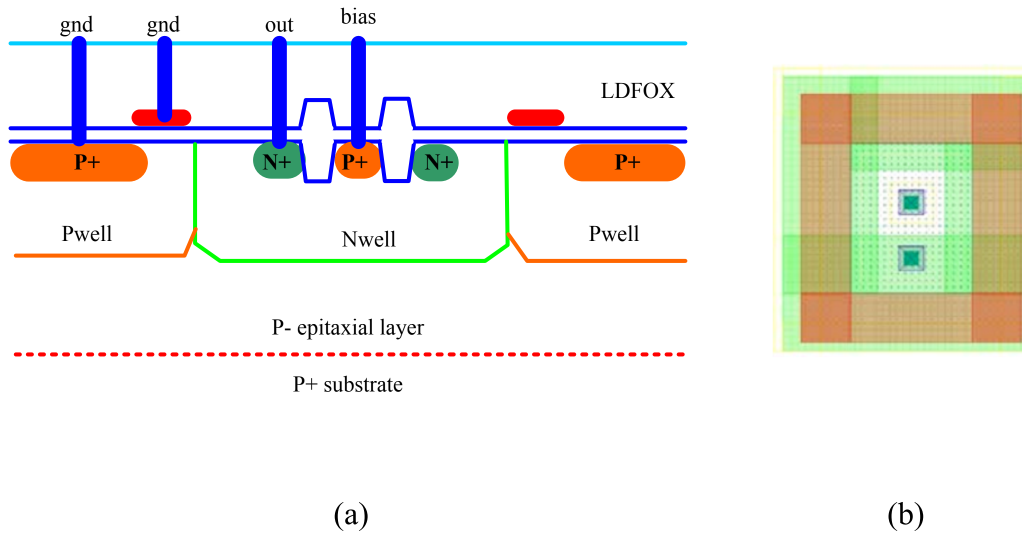


Fig. 3-27. A radiation hard pixel with annular pseudo-poly-gate. (a) Cross section view, (b) Layout view.

The radiation hard diode in Fig. 3-27 has been implemented in several chips and tested. Fig 3-28 shows a comparison result of standard and radiation hard diodes. The radiation hard layout is very efficient. In order to evaluate the radiation tolerance of the design in advance, MIMOSA 15 using the described radiation hard diode was irradiated with an ionizing radiation dose of 1 Mrad of 10 keV X-rays. The chip was run at a temperature of -5 ^{o}C and with integration time of about 0.17 ms. The signal over noise ratio is about 19.4 electrons (most probable value). The detection efficiency is above 99.9%.

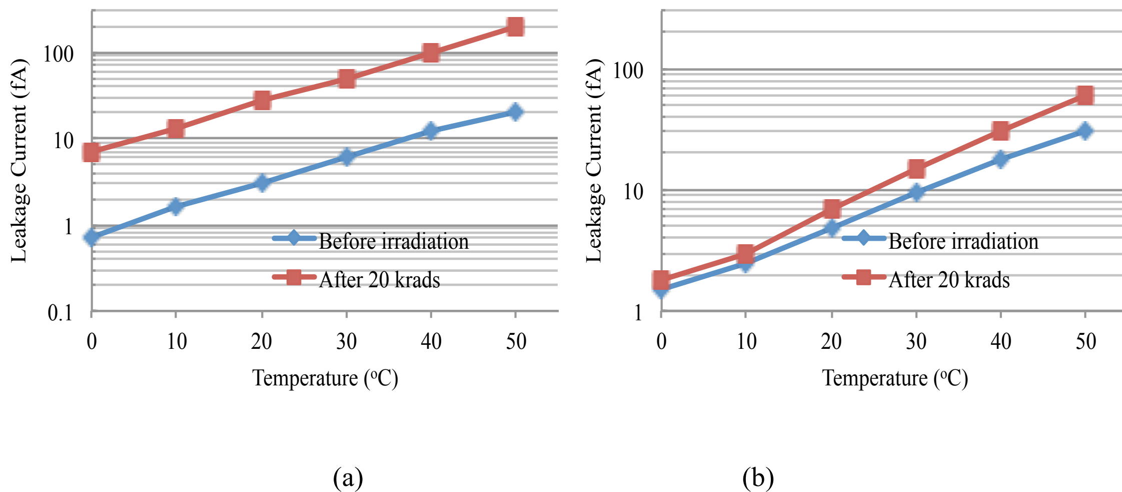


Fig. 3-28. The leakage currents for standard (a) and radiation hard diode (b) as a function of temperature before and after receiving the ionizing radiation dose of 20 kRad. (MIMOSA 11 with 4 ms of integration time)[41]

3.3.4.2 Integration Time

During the study of ionizing radiation, the leakage currents of sensing diode are hugely increased after high dose irradiation. A main result of the leakage current increase is the increase of the shot noise. The mean square value of the shot noise sampled at the end of integration period is given by

$$\overline{V_{n,\text{int}}^2} = \frac{qi_{leak}}{C_{in}^2}\tau_{\text{int}}\ .$$

This contribution to noise can be ignored before irradiation since the mean value of the leakage current i_{leak} is in order of several fA at room temperature without irradiation. However, the leakage currents increase about ten times after irradiation of 20 krads in the non-radiation-hardened layout. Even with the radiation hardened layout, the leakage currents can achieve about 60 fA at a temperature of 50 ^{o}C [41].

In order to limit the noise, the integration time should be decreased. The strategy is consistent with the requirement of fast readout speed since the integration time equals to the duration of one frame in most MAPS chips.

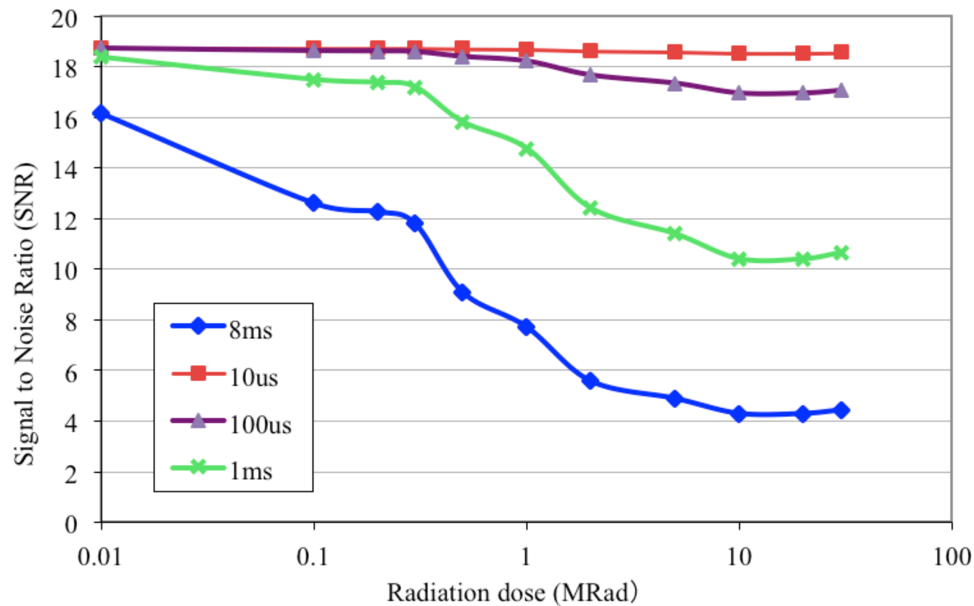


Fig. 3-29. SNR versus irradiation with different integration time.[48]

The leakage currents were tested in the CAP1(Continuous Acquisition Pixel 1) detector, which is a monolithic active pixel sensor based on 3T pixel, in the vertex detector environment of a Super-B Factory with irradiation dose up to 30 Mrad. Gamma irradiation (^{60}Co) of the CAP1 detector is performed with four landmark doses: 200 kRad, 2 MRad, 3 MRad and 20 MRad. A summary of the leakage current

measurements is presented in [49]. The peaks of signal to noise ratio are evaluated according to the measurements. Fig. 3-29 shows the evaluated signal to noise ratio as a function of irradiation doses and integration time, taken from [48]. When the integration time is reduced to 100 μs, the signal to noise ratio is still about 17 with irradiation of 30 Mrad. In the actual X-ray test, the MIMOSA 15 chip with integration time of 170 μs shows TID tolerance of 1 Mrad. The results well fit the evaluation in Fig. 3-29. High readout speed, namely short integration time, is desired for high radiation tolerance MAPS. Recently, fast readout chip is being developed in order to get higher radiation tolerance. The details of fast readout MAPS development and the new problem appearing on radiation tolerance will be illustrated in chapter 4.

3.3.5 Conclusion

The radiation tolerance and the radiation hard technologies of MAPS are studied on non-ionizing radiation and ionizing radiation.

The strategies to alleviate the non-ionizing effects were studied from two aspects: shorting the diffusion paths by increasing the density of diodes and increasing the number of initial signal charge by using thicker epitaxial layer. Reducing the size of pixels from 40 μm to 20 μm leads to an enhanced radiation tolerance of one order of magnitude. The efficiency of the latter is quite limited since the thicker epitaxial layer also lengthens the electron diffusion paths. The best thickness is suggested in the order of 10 - 20 μm. In one word, the charge collection efficiency was dropped after an irradiation of some 10^{11} n_{eq}/cm^2. The leakage current and noise has a little increase after non-ionizing irradiation. The losses in signal to noise ratio caused a drop of detection efficiency for MIP above an irradiation of 2×10^{12} n_{eq}/cm^2. RTS was observed under 10^{13} n_{eq}/cm^2 in 3T pixels. The RTS can be alleviated by cooling the chip. In addition, RTS isn't observed in the use of SB pixels.

The ionizing radiation induced leakage currents influence the detection efficiency of MAPS. By applying radiation hard layout and reducing the integration time, the MAPS can achieve ionizing radiation tolerance above mega rads. To reduce the integration time, fast readout MAPS should be developed. The details of fast readout MAPS development and the new problem appears on radiation tolerance will be illustrated in chapter 4.

4 Improvement of the MAPS Radiation Hardness by Memory Design

Considering that the increase leakage current finally results in an increase of integration noise, which is increased with the leakage current and integration time, another strategy for radiation hardness improvement is to reduce the integration time. The strategy is consistent with the requirement of fast readout speed in some high energy physics experiments such as STAR and ILC. Therefore, fast readout architecture was proposed for MAPS.

In order to increase the readout speed, the pixels are readout row by row with binary outputs, which are realized by on-chip correlated double sampling (CDS) and column level discriminators (one-bit ADCs) [50]. Thus, the readout speed is improved to 640 μs per frame. Fast readout speed of 100 μs per frame is achieved by an integrated data sparsification module named SUZE, which is mainly composed of zero suppression block and memory blocks [51]. In the present design, the radiation tolerances of the memory blocks realized by SRAM IP cores becomes the bottleneck of the whole sensor since SRAM IP core generally aims at high density and are vulnerable to radiation effects. As a result, high radiation hard memories should be designed.

This chapter introduces the architecture and design of the fast readout MAPS firstly and then significantly illustrates the design of high radiation hard memories.

4.1 Fast Readout MAPS

4.1.1 Architecture

In order to increase the readout speed of MAPS, many efforts haven been done. Firstly, the pixels are read out row by row. In addition, memories in pixel were ever proposed. This specific structure is particularly well adapted when the time during the beams' crossing is short in comparison of the time between two beams' crossings. In this case, it is possible to store quickly several frames in pixel's memory cells during beams' interaction. In the second step, the storage data are read slowly during the dead time. The strategy in common use for fast readout is to digitalize the signals and to suppress the data to be read out. Since the hit occupancy is generally quite low in one frame, the amount of readout data will be reduced sharply.

MIMOSA 26 is the first fast readout sensor integrating the zero suppression. Fig. 4-1 shows the schematic of the main data path. Each column of pixels correspond a

discriminator, which is realized by a one-bit ADC. A whole row of pixels is read out and digitized in parallel manner. The digitalized data of each row are compressed to a “16-bit status” and 9 of “16-bit states” in maximal by zero suppression blocks. The compressed data are buffered by two memories. In the present frame, the data are written into one of the memory. In the successive frame, the new data will be written into the other memory, and the date of the first memory will be readout at the same time. Thus, the two memories are written and read alternately. Eventually, the hit information will be serially output by two LVDS transmitters with frequency as high as 80 MHz.

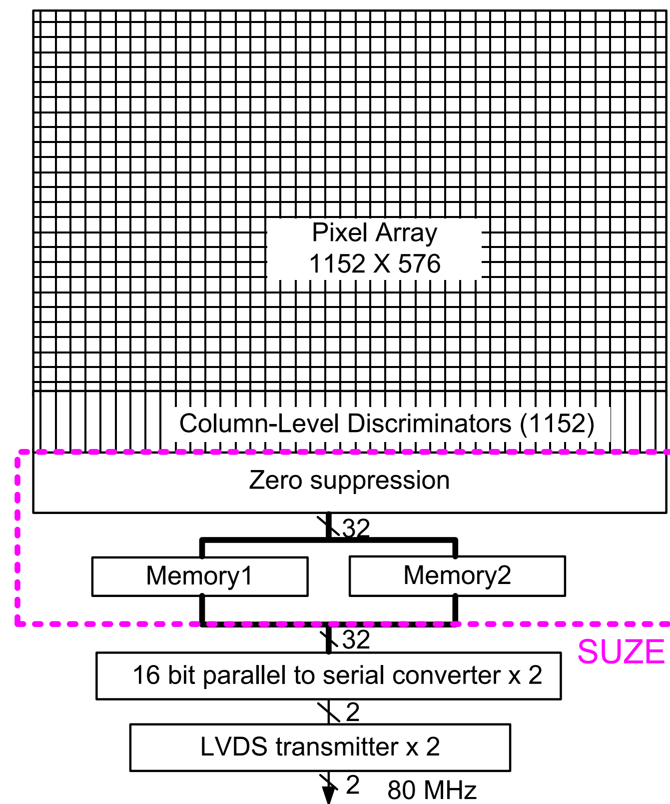


Fig. 4-1. Schematic of a fast readout MAPS (MIMOSA 26).

4.1.2 Pixel and Discriminator

4.1.2.1 Structures and CDS operations

It is worth to note that the on-chip data sparsification requires improving the noise performance, minimize fix pattern noise (FPN) and remove the pedestals on chip. The improved pixel architectures and two time CDS operation are well satisfied the requirements.

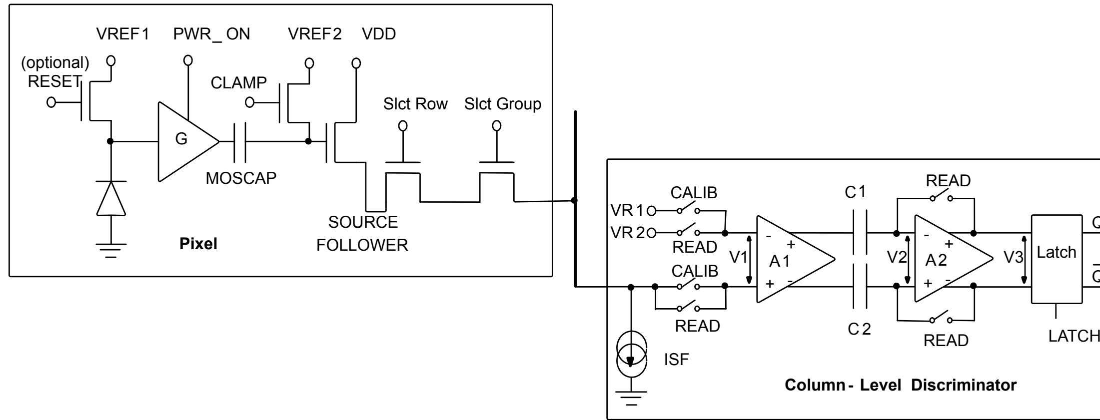


Fig. 4-2. Topology of a pixel and a discriminator.

Fig. 4-2 shows the topology of a pixel and a discriminator. An in-pixel amplifier is implemented at the output of charge sensing element to reduce the noise contribution to the signal after the amplifier. As a result, the signal to noise ratio can be improved. The pixel-level CDS is performed by a capacitor realized by a NMOS transistor (MOSCAP) and a clamping operation. In the case of the self-biased structure, the pixel-level CDS is used to extract useful signals generated by impinging particles. Following the source follower, the two switches are for row and group select respectively. In the MIMOSA 26, there are 1152 pixels in one column. In order to reduce the capacitance on the readout line, pixels in the same column are divided into 72 groups with one group of 16 pixels. The pixels in one column share a discriminator. The discriminator is an offset-compensated comparator, which is based on an auto-zero simplifying stage and a dynamic latch, as shown in Fig. 4-2 [52].

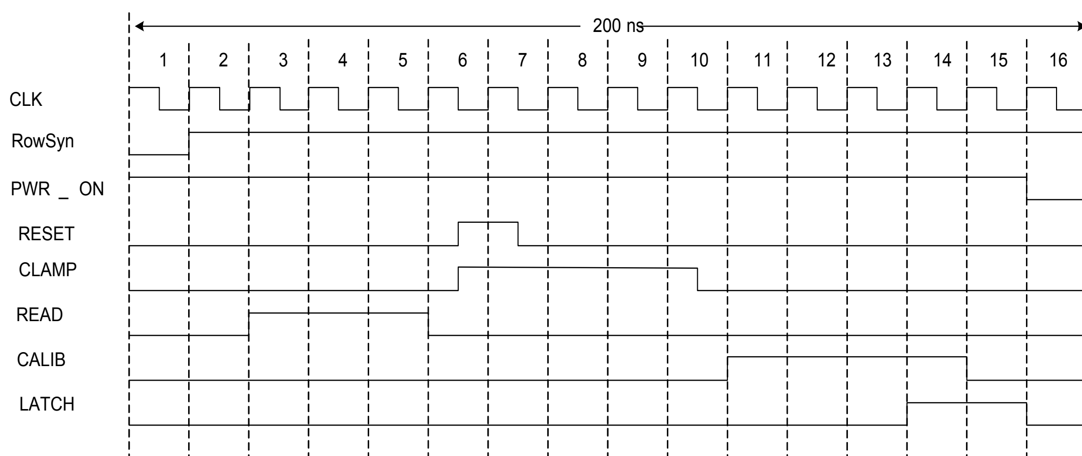


Fig. 4-3. Timing Sequence of Pixel and Discriminator in Fig. 3-33.

Fig. 4-3 shows the operation sequence of the readout and two time CDS operations.

In pixel level, the CDS operation is worked as follow. The charge integrated during last frame is readout at the beginning of the cycle (READ phase). The corresponding integration signal voltage V_{S1} is stored on MOSCAP. Suppose that the output voltage of the preamplifier, namely the input voltage of the source follower, is V_{SFIN}, the voltage across the capacitance is

$V_{CAP} = V_{SFIN1} - V_{S1}$.

After the reset, an initial charge corresponding to the reset voltage V_{S2} is added on the left plate of MOSCAP. The voltage of the other plate, namely the input voltage of the source follower, is clamped to V_{REF2}. The voltage across the capacitance does not change, thus the voltage across the capacitance is

$V_{CAP} = V_{REF2} – V_{S1}$.

Combining the two equations above, the input voltage of the source follower during READ phase is

$V_{SFIN1} = V_{REF2} - V_{S1} + V_{S2}$.

Suppose that the gain of the source follower is G_{SF} and the voltage variation on the two switches is $V_{SW,}$ the outputs of pixel-level circuits during the READ phase V_{PO1} and after reset V_{PO2} can be derived from

$V_{PO1} = G_{SF} \times (V_{REF2} - V_{S1} + V_{S2}) + V_{SW,}$

and

$V_{PO2} = G_{SF} \times V_{REF2} + V_{SW}$, respectively.

In the column level, the discriminator subtracts the voltage in the READ phase from the voltage in the CALIB phase for each pixel and then compares the results with the reference (VR2 – VR1).

During the READ phase, the output from pixel V_{READ} is V_{PO1}. During the CALIB phase, the output V_{CALIB} equals to V_{PO2}. Thus, the signal readout

$$
\begin{aligned}
Vsignal &= V_{READ} - V_{CALIB} \\
&= V_{PO1} - V_{PO2} \\
&= G_{SF} \times (V_{REF2} - V_{S1} + V_{S2}) + V_{SW} - (G_{SF} \times V_{REF2} + V_{SW}) \\
&= G_{SF} \times (V_{S1} - V_{S2}).
\end{aligned}
$$

Combining the two CDS operations, reset noise is removed and the pixel-to-pixel dispersion is reduced.

4.1.2.2 In-pixel Amplifier

In order to reduce the noise contribution after the amplifier like clamping or sampling, a high gain amplifier is desired after the sensing diode. In pixel, PMOS transistors are not allowed since the PMOS hosted n well will decrease the signal. However, adopting PMOS transistor as a load would be the preferred choice to increase the gain of in-pixel amplifier.

Standard common source schematic with NMOS load is shown in Fig. 4-4 (a).

The gain of the amplifier

$$G = V_{out}/V_{in} = \frac{g_{m1}}{g_{m2} + g_{mb2} + g_{ds1} + g_{ds2}}.$$

In order to increase the gain, g_{m2} and g_{mb2} should be reduced and the g_{m1} should be increased. With the decreasing of g_{m2}, DC current will be decreased. As a result, g_{m1} is decreased. Therefore, g_{m2} should be not dependent on the DC current. A biasing circuit was introduced in [53, 54]. The gate of M2 is decoupled from the power supply and biased with one additional NMOS transistor M3, shown in Fig. 4-4 (b). Transistor M3 works in saturated sub-threshold mode, and the gate of M2 has the DC potential close to power supply. Therefore, the DC operation point of the amplifier is almost not changed. The AC voltage at the gate is coupled from the output voltage by parasitic gate to source capacitor. Thus, the g_{m2} for voltage frequencies larger than g_{m3}/C_{gs2} is cancelled. The gain of the improved amplifier is

$$G = V_{out}/V_{in} = \frac{g_{m1}}{g_{mb2} + g_{ds1} + g_{ds2}}.$$

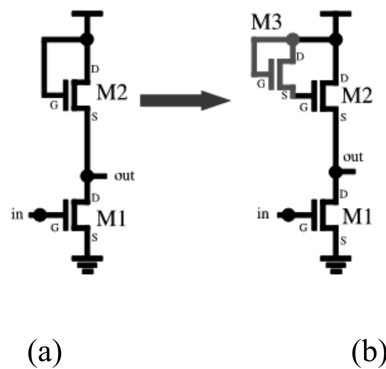


Fig. 4-4. Schematic of in-pixel amplifier. (a) Common source amplifier (b) Improved amplifier.[54]

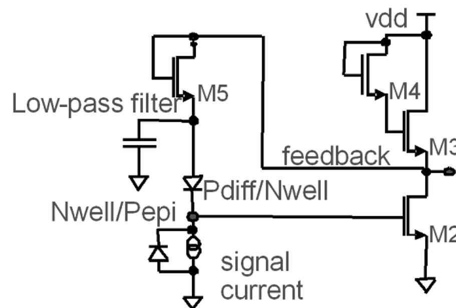


Fig. 4-5. Improved amplifier with a negative feedback and self-biased sensing element.[55]

The AC gain of the improved amplifier increases about a factor of two, but the DC operation point and DC gain are almost not changed, which makes the circuits resistant to CMOS process variation. In addition, negative feedback can be used to stabilize the operation point of the amplifier. Fig. 4-5 shows the improved amplifier with a negative feedback and self-biased sensing element. The feedback is a low pass filter with very large time constant. It also provides biasing via a high resistive Pdiff/Nwell diode for the charge sensing diode.

4.1.3 **Zero Suppression**

In the application of MAPS in some high energy physics experiments, the hit occupancy of the whole pixel array is quite small. For example, it is less than 1% in average in STAR experiment. Large amount of the unfired pixels will be digitized with "0" after the discriminators. The zero suppression circuits suppress this part of data and only memorize the address of hit pixels to reduce the amount of readout data. A proper hit recognition and encoding format and a hit finding algorithm will be introduced firstly, and then the readout chain is explained.

4.1.3.1 Hit Recognition and Encoding Format

When a particle gets through the pixel array, several pixels will be fired. The upper of Fig. 4-6 shows a sketch map. The pixels are readout row by row. The adjacent fired pixel in the same row is defined as a "state". Generally, the radius of one hit is less than 4 pixels. If the number of adjacent hot pixel is larger than 4, a new "state" starts from the fifth pixel. The downer of Fig. 4-6 shows the data of Row i after discriminator. There are two states. State 1 has four-fired pixels and the state 2 has three.

Each state is encoded as a 16-bit data. Fig. 4-7 shows the format of the data. The first two bits are the identification of the hit pattern. Four possible patterns and the corresponding code are also shown in Fig. 4-7. The bits from 2 to 12 are the 11-bit column address of the first pixel in the hit pattern. The rest three bits are not used. Thus, the hit information in a certain row can be recorded.

In order to increase the suppression rate, all the states in the same row share a same field for the row address. This field is termed "status". The format of a status is shown in Fig. 4-8. The binary data of the first four bits is the total number of the states in the present row, the address of which is indicated by the bits from fourth to fourteenth. The last bit 15 OVF is an overflow flag. The OVF is valid when the number of states larger than a certain value M. The M is derived from a statistical study based on the highest occupancy expected in the pixel array. In the actual design, up to M states by row can be processed.

Fig. 4-6. A sketch map of hits in pixel array.

	0–1	2–12	13–15
State	Hit Pattern Flag	Column Address (the first pixel in the hit pattern)	Unused

Hit Pattern	Hit Pattern Flag
1 0 0 0	00
1 1 0 0	01
1 1 1 0	10
1 1 1 1	11

Fig. 4-7. Encoding format of a state.

	0–3	4–14	15
Status	Number of States	Row Address	OVF

Fig. 4-8. Encoding format of a status.

4.1.3.2 Realization of Zero Suppression

The block diagram of the readout chain of MAPS is shown in Fig. 4-9. The pixel array is divided into 18 banks, and a sparse data scan [56] is performed parallel for each bank. The sparse data scan blocks generate 18 × N states in total. Only M states will be retained for one row. After the state multiplexer, one status and M states will be stored in memory successively. The readout chain of zero suppression is based on row by row readout, and is organized in pipeline mode in three steps, which are sparse data scan, state multiplexer, and data storage [51]. The row of matrix is read out during 200 µs and the read out frame frequency is about 10 KHz.

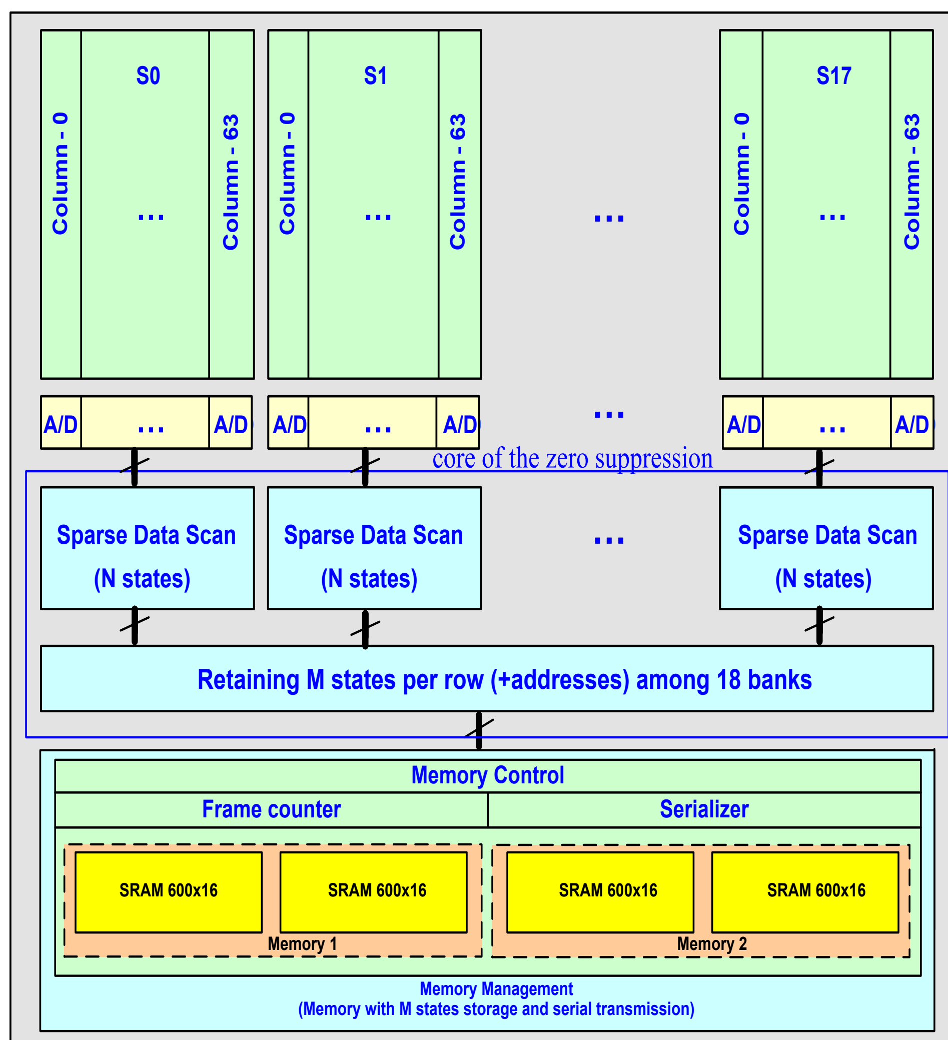


Fig. 4-9. Block diagram of the MAPS readout chain with zero suppression

4.1.4 **Performance**

MIMOSA 26 is the first fast readout MAPS with zero suppression. It actually combines the architecture of two earlier prototypes: MIMOSA 22 and SUZE. MIMOSA 22 is with the pixel array and discriminator, while SUZE is the prototype of zero suppression. The tests of MIMOSA 26 were performed in several steps. [22, 55]

Firstly, the analogue part of the pixel array was tested. The performance was investigated by illuminating the sensors with a ^{55}Fe source. The noise of pixel array is uniformly distributed and that there are no dead pixels. The average equivalent noise charge is less than 14 electrons with a readout frequency of 80 MHz. The charge collect efficiency was derived from the reconstructed clusters generated by the 5.9 and 6.49 keV X-Rays. For the seed pixel, the CCE is about 22%. In the case of cluster size of 3 × 3, the CCE can achieve 73%.

Secondly, the noise performance was estimated for individual discriminator by group of 288 discriminators with and without pixel array respectively. In case of the discriminators isolated from the pixel array, the thermal noise is ~0.4 mV and the fix pattern noise is ~0.2 mV. When the discriminators were connected to the pixel array and the chip response was assessed at 80 MHz, namely 112.5 μs frame read-out time, the noise measurement results for one group are shown in Fig. 4-10. The total thermal noise is about 0.6-0.7 mV, which is basically the value of the pixel thermal noise. The fix pattern noise is about 0.3-0.4V, which is dominated by the fix pattern noise of the column discriminators. These values remain almost constant with the readout clock frequency from 80 MHz to 20 MHz.

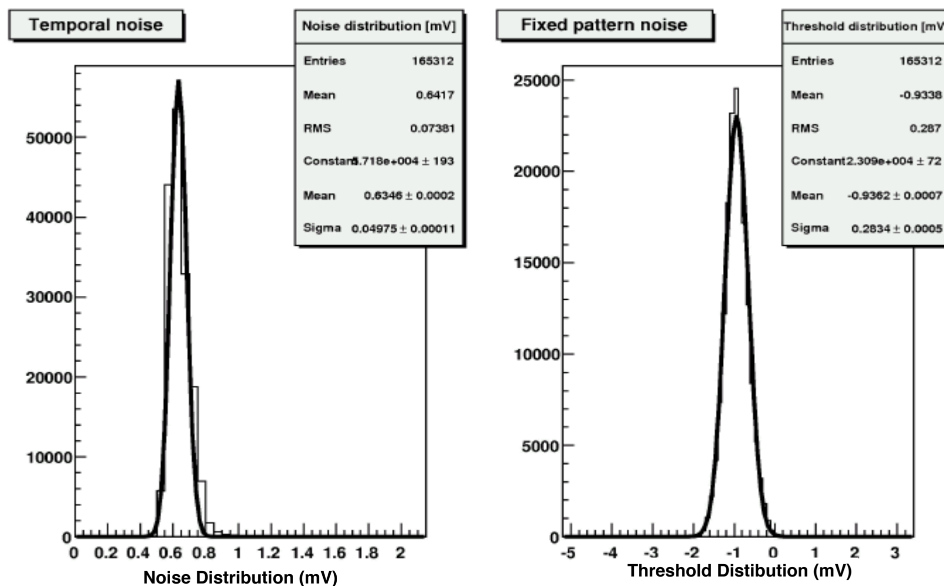


Fig. 4-10. Response of a group of 288 discriminators connected to the pixel array [22, 55].

Thirdly, the zero suppression circuitry was tested separately. The run frequency can achieve 115 MHz.

Finally, the complete signal processing from pixel array to the output of the data transmission was tested. The ratio of fake hits is related with the discriminator threshold. To keep the fake hit rate at a level of 10^{-4} (< 70 pixels per frame), the discriminator threshold values rang is from 5 to 5.5 times of the noise value. This result remains essentially unchanged when varying the operation temperature from 20 ^{o}C to 40 ^{o}C. The power consumption of the sensor is ~ 750 mW for the whole chip. This value corresponds to ~ 250 mW/cm^2 and to ~ 640 µW/column.

The beam test of MIMOSA 26 was operated on particle beams (~ 120 GeV/c pions) at the CERN-SPS. The thermal noise and the fix pattern noise are consistent with the results observed in the laboratory.

Setting the threshold of 6 times of the average noise, the distribution of the number of pixels per frame with noise fluctuations was shown in Fig. 4-11. The average value of fired pixels per frame is about 40. Compared to the total number of pixels (~ 660,000), the corresponding rate is ~ 6 × 10^{-5}.

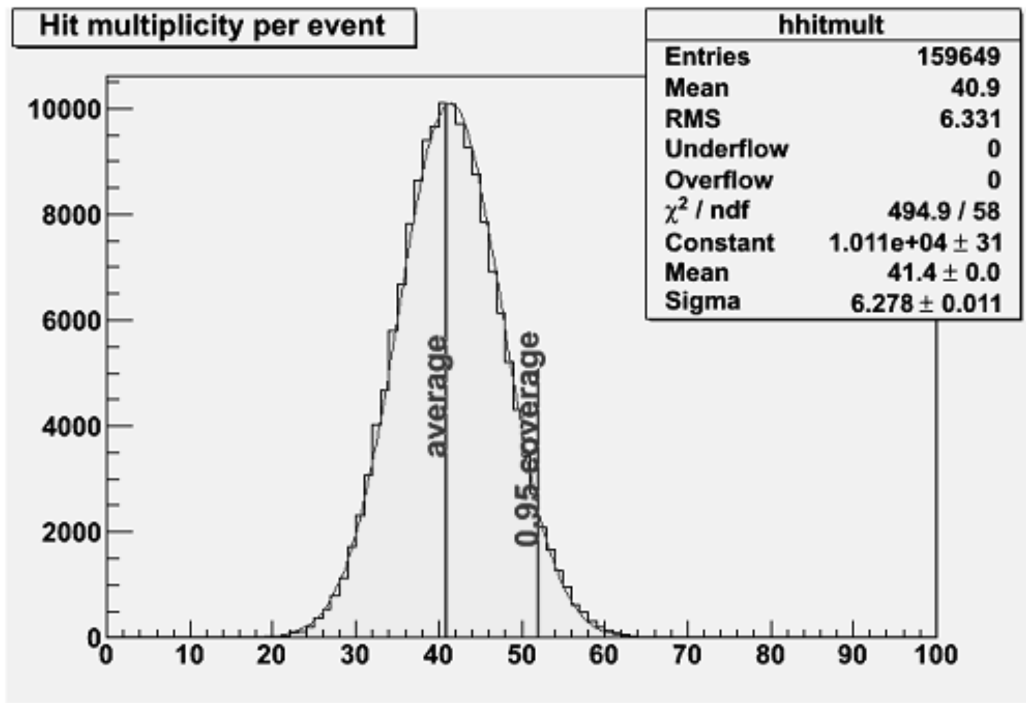


Fig. 4-11. Number of pixels per frame with a noise fluctuation passing a discriminator threshold of 6 times of the average noise.[55]

The detection efficiency was evaluated for different threshold values and on different sensors. Fig. 4-12 shows the results. The detection efficiency is about 99.5% for a fake rate of 10^{-4}. Although the result is slightly below that of MIMOSA 22, the detection efficiency is satisfied well with the STAR experiment.

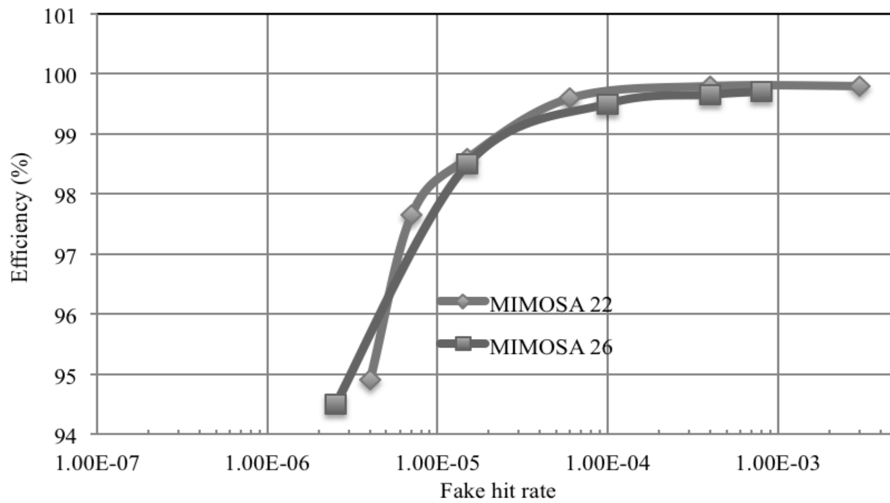


Fig. 4-12. Variation of the detection efficiency with the fake hit rate.[22, 55]

The radiation tolerance of MIMOSA 26 to non-ionizing radiation effects and total ionizing radiation effects will be improved due to the fast readout. However, a predictable weak point is the radiation tolerance of the digital circuits, especially the two memories blocks implemented by SRAM IP cores. Therefore, the radiation tolerance of the two memories is an important issue for evaluating the tolerance of the whole MAPS. This issue will be significantly studied in the rest of this chapter.

4.2 Radiation Tolerance of the Fast Readout MAPS

Under the harsh environment of high energy experiments, the radiation effects, including non-ionizing effects, total ionizing effects, and single event effects, should be considered. In the past years, the radiation tolerance of MAPS has been improved by reducing pixel pitches, selecting proper thicknesses of epitaxial layer, using radiation hard layout techniques and designing a self-biased pixel architecture. Moreover, the influences of the TID-induced leakage currents have been effectively alleviated by reducing the charge integration time of MAPS. The MAPS radiation tolerance to total ionizing radiation and non ionizing radiation can achieve about 1 MRad and 2×10^{12} N_{eq}/cm^2 for 20 µm pitch, respectively. Recently, fast readout MAPS is being developed, while the radiation tolerance of the built-in memories should be evaluated and improved.

An application of MAPS in high energy physics experiments is the upgrade of the PIXEL detector for the STAR experiments (illustrated in Chapter 1.3). The non-ionizing radiation fluence is estimated in the order of 10^{13} N_{eq}/cm^2. The ionizing radiation dose on the PIXEL detector is about 300 krads/year with a radiation rate of

3.8×10^5 Hz/cm^2 [26, 57]. Under these conditions, MAPS are vulnerable to SEE. Thus, the SEE including SEL and SEU should be carefully considered apart from the non-ionizing radiation effects and the TID effects. The sensor prototypes called MimoSTAR2, Phase1 and MIMOSA 22 and a prototype of a data processing block called SUZE were developed and tested for the STAR experiments.

MimoSTAR2 is one of the first generation sensors, featuring analog outputs with a rolling-shutter readout mode. The particle detection efficiency of MAPS has been demonstrated. Phase1 and MIMOSA 22 [58] are the second generation sensors, integrating column level discriminators (one-bit analog to digital converters) and providing a binary readout with charge integration time of 640 µs. However, MIMOSA 22 improves the radiation tolerance as compared to Phase1. The improved pre-amplifier with a negative feedback and self-biased sensing element (like the pixel design in MIMOSA 26 presented in Chapter 4.1.2.2) was introduced in pixel to decrease the operating point variation due to process dispersion in MIMOSA 22. SUZE [51] is a chip to verify the function of data sparsification. It consists of the zero suppression block and two identical SRAM IP cores. The latest generation sensor named ULTIMATE is currently developed. It combines the architectures of MIMOSA 22 and SUZE, providing charge integration time of 200 µs. In fact, ULTIMATE has the same architecture and design with MIMOSA 26 but larger pixel array.

Fig. 4-13 shows the SEL test results of MimoSTAR2, Phase1, MIMOSA 22 and SUZE. It is clear that the digital chip, SUZE, has the lowest value of latchup cross-section. It is about a factor of 5 times more sensitive than the MimoSTAR2 sensor. It is worth to mention that all the latchup effects detected in SUZE occurred on the power supply line of the two SRAM IP cores. Therefore, the SEL tolerance of the two SRAM IP cores will be the bottleneck of the SEL tolerance in the case of ULTIMATE.

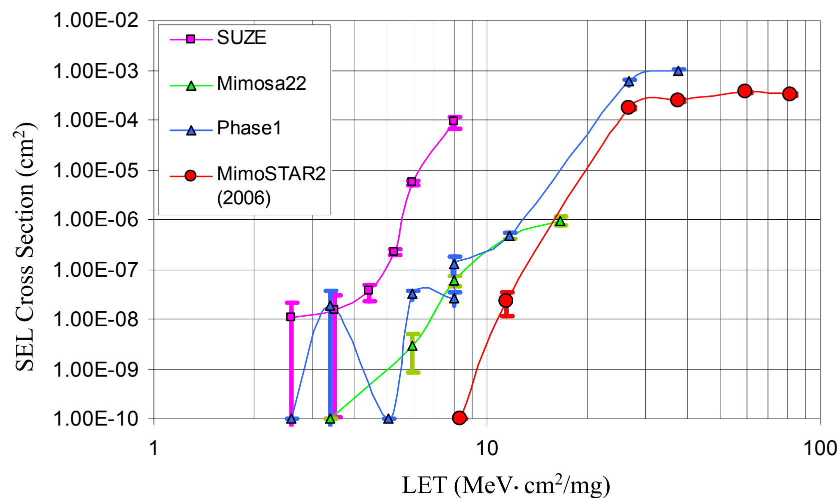


Fig. 4-13. SEL cross-sections of MimoSTAR2, Phase1, MIMOSA 22 and SUZE

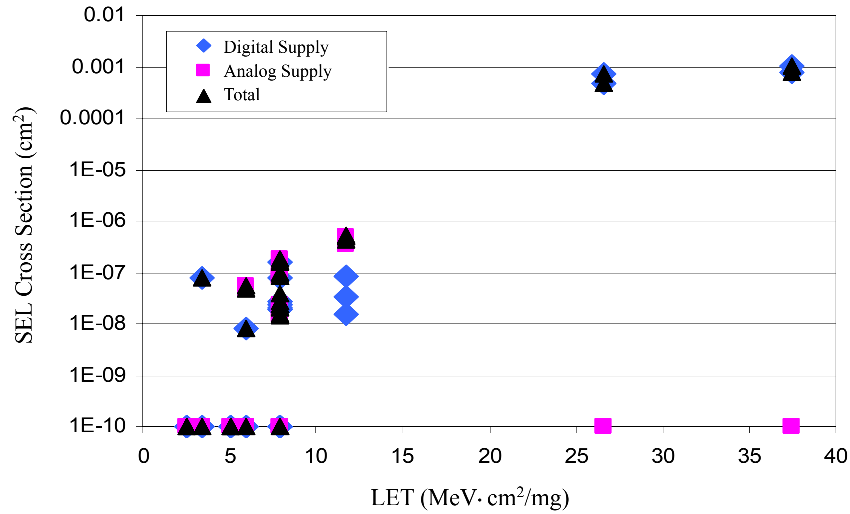


Fig. 4-14. SEL cross-section measured for MIMOSA 22 with distinction between latchup events registered on the analog and digital power supplies.

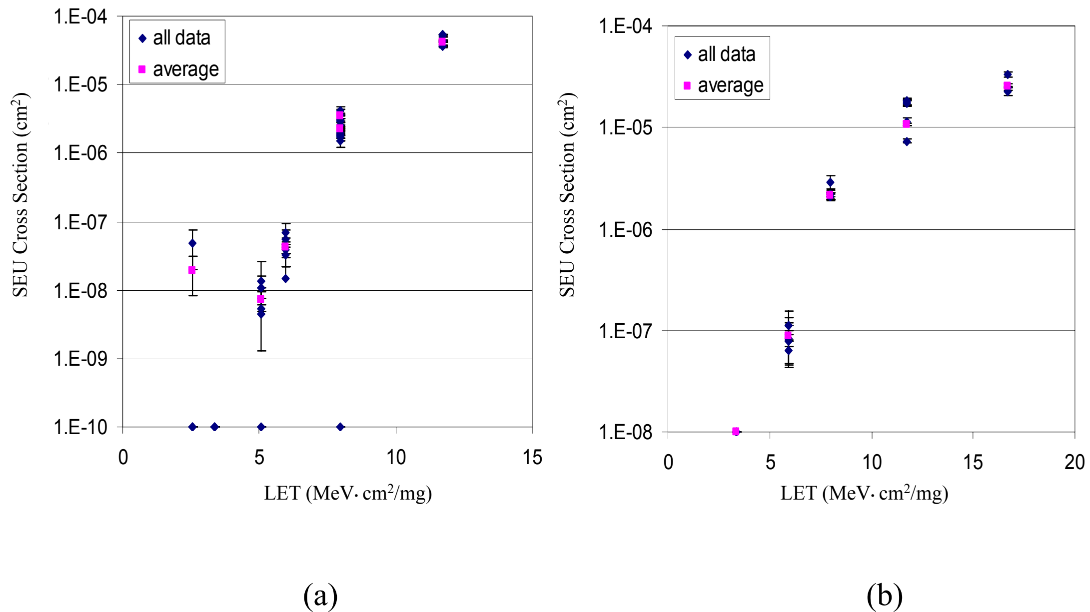


Fig. 4-15. SEU cross-section measured for Phase1 (a) and MIMOSA 22 (b). Points at 1E-10 (Phase1) and 1E-8 (MIMOSA 22) indicate measurements that yielded no errors.

Cross-section of SEL on MIMOSA 22 was also measured with distinction between latchup events registered on the analog and digital power supplies for compare. The results are shown in Fig. 4-14. It appears that it is more likely to have a latchup on an analogue rather than digital power supply. The similar conclusion can be derived from the test of Phase1. This may result from that the area of the analog

circuits is much larger than that of the digital circuits. The results indicate again that the two SRAM IP cores will be the bottleneck of SEL tolerance in the future MAPS.

The cross-section of SEU effects was measured on Phase1 and MIMOSA 22. The test results indicate the saturation cross-sections are less than 10^{-4} cm^{-2} at 12 $MeV \cdot cm^2/mg$ for Phase1 and at 17 $MeV \cdot cm^2/mg$ for MIMOSA 22, as shown in Fig. 4-15. The SEU cross-section of SUZE was not tested. The SEU cross-section of the SRAM IP cores is predicted to be higher since the IP cores include high-density latches (SRAM cells).

The above results demonstrate that the radiation tolerance of the two SRAM IP cores is the main limitation of the whole MAPS radiation tolerance. In order to improve the radiation tolerance of MAPS, the radiation tolerance of the two SRAM IP cores should be improved.

4.3 Design of Radiation Hard SRAM

4.3.1 Introduction to SRAM

4.3.1.1 Architecture

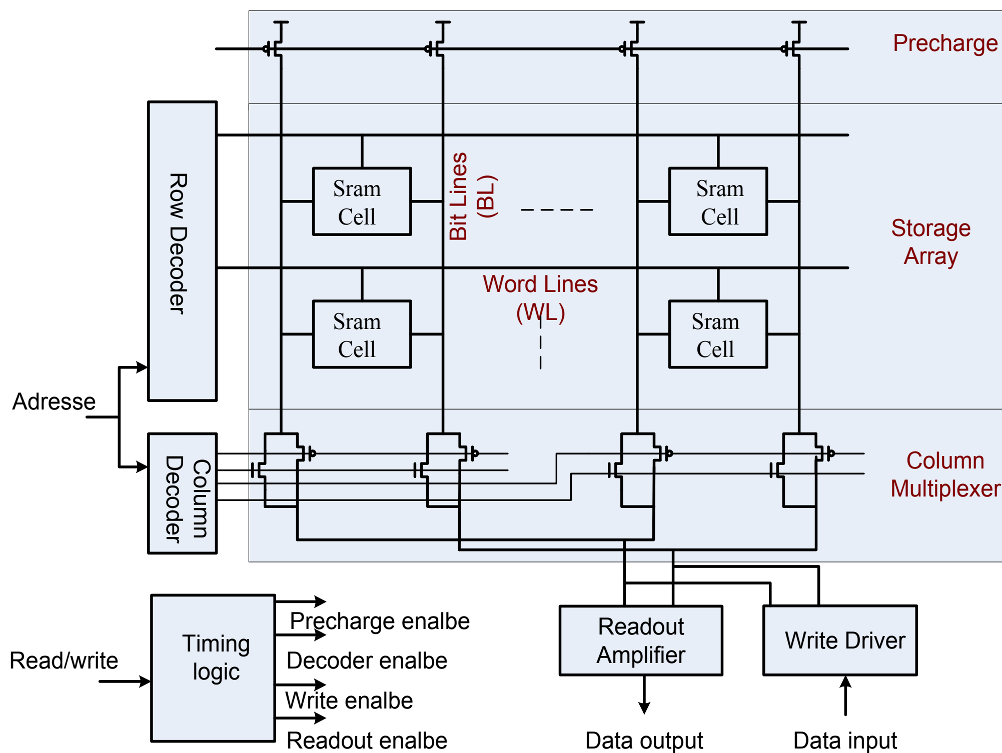


Fig. 4-16. A simplified block diagram of SRAM

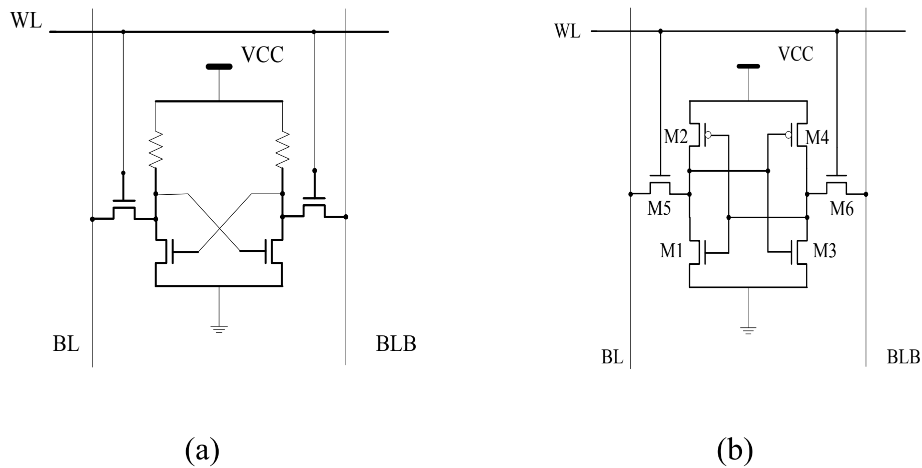


Fig. 4-17. SRAM cell. (a) 4T2R (b) 6T

The structure of an SRAM is similar with that of the MAPS. An SRAM consists of a storage body and its peripheral circuits, as shown in Fig. 4-16.

The storage body consists of duplicate SRAM cells, which are arranged as an array by sharing the word lines (WL) horizontal and sharing the bit lines (BL) vertically.

The access and control of the storage body are realized by peripheral circuits. They include row and column decoders for addressing a certain SRAM cell, column multiplexer for data distribution, pre-charge circuits for recovering the data on bit lines, readout amplifier for fast readout, timing logic for generating the timing control signals and input/output drivers for correctly receiving and sending the data.[59]

SRAM cell is a bi-stable flip-flop consisting of four or six transistor, namely 4T2R cell and 6T cell shown in Fig. 4-17. The two stable states can be defined as logic 1 and logic 0 separately. The flip-flop can be either of the two states under the control of the peripheral circuits. The 4T2R cell has compacted layout, but requires poly resistor with high resistance. In addition, the static current of the 4T2R cell cannot be ignored. Hence, the 6T cell is widely used in low power application and large-scale system on chip. Under the radiation environment, 6T cell is much stable than 4T2R cell. Therefore, the SRAM based on 6T cell is significantly studied in this work.

4.3.1.2 Operation Principle

The read/write operations of the 6T SRAM cell depend on the voltage and timing on bit lines and word lines.

The read operation is illustrated in Fig. 4-18. We suppose the data in the SRAM cell is ‘1’, namely Q is ‘1’ and QB is ‘0’. (In opposite, the storage data is thought as ‘0’ if the SRAM cell is in the other stable state, namely Q is ‘0’ and QB is ‘1’.) The M1 and M4 are cut off. The Q maintains ‘1’ by the pull-up of M2, and the QB maintains ‘0’ by the pull-down of M3. In static mode, the word line is disabled and

the two bit lines are pre-charged to a certain potential (V_{DD} in Fig. 4-18). There are almost no currents from power supply to ground. Therefore, the static power consumption is very low in static mode.

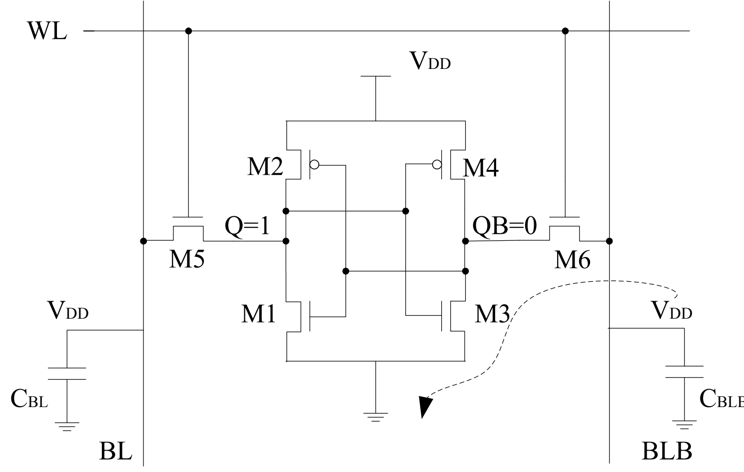


Fig. 4-18. Read operation of a SRAM cell

A read operation is in fact to distinguish which side of the storage node is "0". It can be performed by three steps. Firstly, the two bit lines are released. The voltages of the bit lines are kept at VDD by the parasitic capacitors on the interconnection lines and the connected devices. Secondly, the word line is activated. The transistors M5 and M6 are turned on. The storage node of "0" (QB) and the connected bit line (BLB) are prone to get charge balance. On the other side of the cell, Q and BL are already balance. As a result, the potential of BLB is decreased while the potential of BL is almost no change. Thirdly, the data can be recognized by reading the data on BL or BLB after a discharge period. The lower bit line corresponds "0" at the storage node on its side. Generally, the discharge of bit lines requires a long time to achieve a discrete level in large size memory since the capacitance of the bit line may be in hundreds of femtofarads. In a high speed SRAM, sense amplifier is used to speed up the read procedure.

During the read process, the node QB should not be reversed. Thus, the current strength of M3 must be higher than that of M6. The critical value of the transistor ratio can be derived from the current equation when the voltage variation on the BLB is the largest acceptable value ΔV. Ignoring the body effects of M6, we can get that

$$k_{n,M6}\left[\left(V_{DD}-\Delta V-V_{TN}\right)V_{DSATn}-\frac{V_{DSATn}^2}{2}\right]=k_{n,M3}\left[\left(V_{DD}-V_{TN}\right)\Delta V-\frac{\Delta V^2}{2}\right].$$

Namely,

$$\Delta V=\frac{V_{DSATn}+CR(V_{DD}-V_{Tn})-\sqrt{V_{DSATn}^2\left(1+CR\right)+CR^2\left(V_{DD}-V_{Tn}\right)^2}}{CR},$$

where CR (Cell Ratio) is defined by

$$CR = \frac{W_3/L_3}{W_6/L_6}$$

The analysis above is in the worst case. Actually, the other bit line BL will keep the storage node at the power supply level. It makes the SRAM cell difficult to be upset.

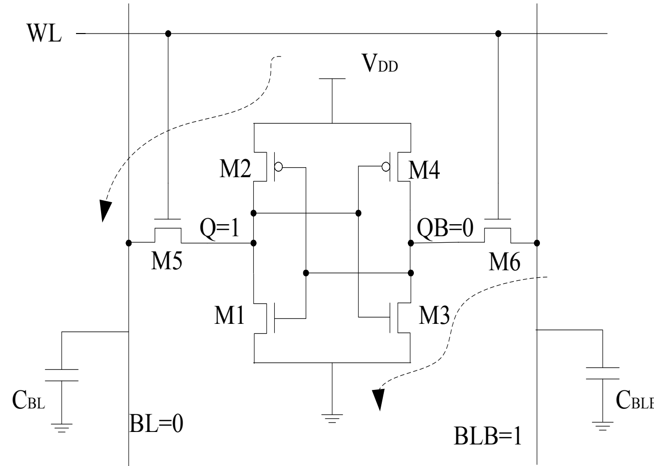


Fig. 4-19. Write operation of a SRAM cell

The write operation of the SRAM cell is illustrated in Fig. 4-19. Suppose the storage data is “1”, and “0” is intended to be written by driving the bit lines BL and BLB to “0” and “1” respectively. To simplify the analysis, the M2 gate is thought at ground level and M3 gate is at power level before the turn-on of M1 and M4. The current flow is shown in the Fig. 4-19. Once M1 and M4 get through, the stable state of the flip-flop is destroyed. The case of QB and BLB is similar with that in a read operation. That means the QB must be promised not to be written into “1”. Therefore, the write operation should be performed by M5.

In order to write “0”, the potential of Q must be low enough. Normally, the data can be written if the voltage of Q is lower than the threshold of the inverter consisting of M3 and M4. However, we generally impose the voltage of Q lower than the threshold of M4 in order to increase the noise margin. Under the case, the current equation when the potential of Q is the desired threshold is

$$k_{n,M5}\left[\left(V_{DD}-V_{TN}\right)V_Q-\frac{V_Q^2}{2}\right]=k_{p,M2}\left[\left(-V_{DD}-V_{TP}\right)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right].$$

Namely,

$$V_Q = V_{DD} - V_{TN} - \sqrt{\left(V_{DD} - V_{TN}\right)^2 - 2\frac{\mu_p}{\mu_n} PR\left[\left(-V_{DD} - V_{TP}\right)V_{DSATp} - \frac{V_{DSATp}^2}{2}\right]}$$

where PR (Pull-up Ratio) is defined as

$$PR = \frac{W_2/L_2}{W_5/L_5}.$$

During the analysis above, M1 and M4 are supposed not to perform the write operation. Actually, once the voltage of Q is lowered, the QB will be raised quickly due to the positive feedback of the cell. In addition, the bit lines generally can be driven to the desired values during the whole write operation. The write operation will be much safe.

4.3.2 **Analysis of Prevailing Radiation Hard Design Method**

For a standard SRAM, the main radiation effects are the ionizing effects including single event latchup effect, single event upset effect, single event transition effect, and total ionizing dose effects. The designer generally enhances the radiation tolerance of the SRAM from process choice, system design, circuit design, and layout design.

4.3.2.1 Process

The radiation tolerance of MOS devices strongly depends on the detail process technologies such as surface contaminants, substrate doping concentration, polysilicon concentration, annealing and so on. In order to improve the radiation tolerance, the designer generally can chose the processes with thin gate oxide, with twin-tub process on thin epitaxial layer, with low well resistance and high concentrations, with SOS/SOI substrates and so on. The SRAM in MAPS is based on the same substrate with the charge sensing elements. Hence, commercial twin-tub CMOS process with epitaxial layer is adopted. The thickness of the epi layer is mainly optimized for the charge collection efficiency. Since the commercial process is not optimized for high radiation tolerance, the improvement is quite limited and not enough for the high energy physics experiments. The hardening techniques on circuits and system design are still required.

4.3.2.2 System

In system level, the main radiation effects (TID, SEU and SEL) can be mitigated. Firstly, a popular strategy for the accumulative TID effects is to place several memory modules and then to use them alternatively. The unused memories can be powered off

for removing or decreasing part of the accumulated charges. Secondly, the SEL effects generally should be prevented before the chip is destroyed. This can be realized by latchup-protected technique (LPT) [60-62]. Thirdly, SEU tolerance can be improved by many techniques. According to the system requirements, hardening by software or hardware can be asserted. A usual approach to protect the circuits from SEU is to add redundancy to the storage information. That can be realized by triple modular redundancy (TMR) [63, 64] or error detection and correction (EDAC) techniques [65-71]. The TMR technique is also popular for resist SET effects. These techniques are simply introduced as follow.

LPT

In the LPT technique, power supply of the protected circuits will be cut off for a certain time when the currents through power supply wires achieve a certain value, thus the chip can be prevented from being destroyed.

The latchup-protected circuits should be free from latchup, while the commercial CMOS process is not immune form latchup. Moreover, the parameters such as the threshold current of power-off, and the power-off duration should be preset. Therefore, the technique is adequate to be implemented off chip in system level.

TMR technique

The mechanism of the TMR technique is shown in Fig. 4-20. The idea is based on the assumption that the upset is a small probability event. In order to enhance the tolerance of a combinatorial logic cell, the signal path is tripled. A majority voter is used to decide the final result in each path. Namely, if the state in one of the paths is upset, the other two will be coincidence and the right result can be output by the majority voter. This method will be failure when states of two or three paths are upset. The hardware expenses for realizing this technique are more than three times of that of the original circuits.

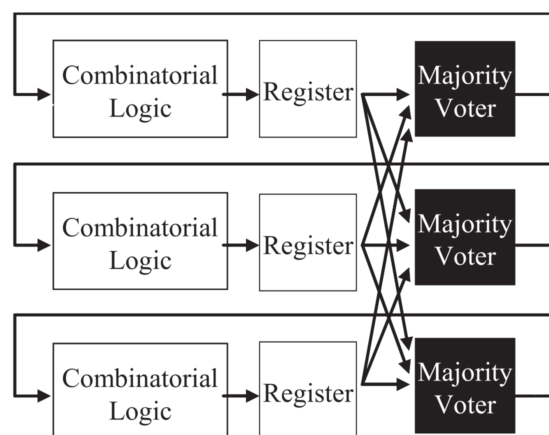


Fig. 4-20. Scheme of the TMR technique

EDAC technique

EDAC technique is implemented by adding a verification code to the original data. The common-used encode algorithms include Parity Code, Hamming Code, Cyclic Redundancy Check (CRC) code and so on [65, 68, 71]. Both the original data and the verification code are written in a memory. Before output, the data read from the memory are decoded. A correction code should be generated to locate the error bit according to the encoding method. The correction code should be able to reflect the errors happened on the original data and itself. Then, the original data can be recovered according to the correction code. In fact, the number of errors that can be detected and corrected depends on the code and decode algorithm. Generally, not all the errors can be found in order to increase the encode efficiency. Therefore, flag bits to show if the output data is available should be given.

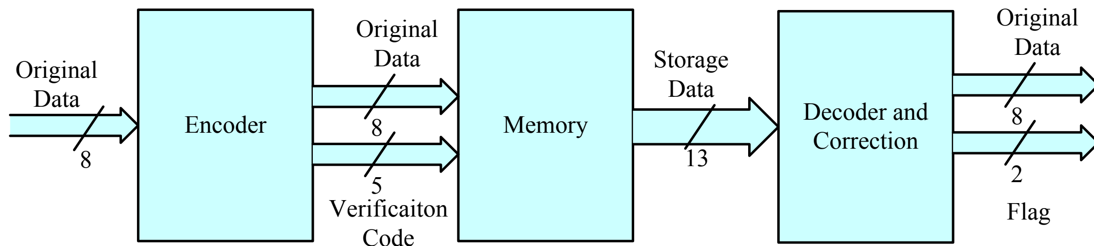


Fig. 4-21. Scheme of the EDAC technique

A scheme of the EDAC technique is shown in Fig. 4-21. For instance, an Hamming Code (13, 8) is used for an 8-bit original data. The 13-bit data will be output from the encoder as format {d7, d6, d5, d4, d3, d2, d1, d0, c4, c3, c2, c1, c0}, include 8 bit original data and 5 bit correction data. Where ‘di’ is the original data and ‘ci’ is the verification code. The c4, c3, c2, c1 and c0 can be obtained according to the following algorithm.

c0= d6^d4^d3^d1^d0;

c1= d6^d5^d3^d2^d0;

c2= d7^d3^d2^d1;

c3= d7^d6^d5^d4;

c4= d7^d6^d5^d4^d3^d2^d1^ d0^c1^c2^c3.

Then, the 13 bit data is stored in the memory. If there is any upsets, the data from memory should be corrected. In the decoder, a correction code matrix {s4, s3, s2, s1, s0} should be generated to locate the error bit. Where,

s4= d7^d6^d5^d4^d3^d2^d1^d0^c1^c2^c3^c4

s3=d7^d6^d5^d4^c3;

s2=d7^d3^d2^d1^c2;

s1=d6^d5^d3^d2^d0^c1;

s0=d6^d4^d3^d1^d0^c0.

The value of s4, s3, s2, s1, s0 and the corresponding error location are listed in Table 4-1. If the value of {s4, s3, s2, s1, s0} is not listed, this algorithm is failed. In

such case, more than one error happens. This example is able to correct one-bit error and detect two-bit errors. The output flag bits give the information of what happened, such as four cases in this example: no errors, one error and correction, two errors and no correction, and more than two errors. Generally, more bits can be detected and corrected if more verification bits are used.

Table 4-1 Error location of a 5-bit Hamming Code

<table>
<tr><th colspan="2">s4 s3 s2 s1 s0</th><th>Error Location</th><th>Flag bits</th><th>Case</th></tr>
<tr><td colspan="2">11100</td><td>d7</td><td rowspan="13">11</td><td rowspan="13">One error detected and corrected</td></tr>
<tr><td colspan="2">11011</td><td>d6</td></tr>
<tr><td colspan="2">11010</td><td>d5</td></tr>
<tr><td colspan="2">11001</td><td>d4</td></tr>
<tr><td colspan="2">10111</td><td>d3</td></tr>
<tr><td colspan="2">10110</td><td>d2</td></tr>
<tr><td colspan="2">10101</td><td>d1</td></tr>
<tr><td colspan="2">10011</td><td>d0</td></tr>
<tr><td colspan="2">11000</td><td>c3</td></tr>
<tr><td colspan="2">10100</td><td>c2</td></tr>
<tr><td colspan="2">10010</td><td>c1</td></tr>
<tr><td colspan="2">10001</td><td>c0</td></tr>
<tr><td colspan="2">10000</td><td>c4</td></tr>
<tr><td colspan="2">00000</td><td>-</td><td>10</td><td>No error</td></tr>
<tr><td rowspan="2">Others</td><td>S4=0</td><td>-</td><td>00</td><td>Failure with two errors</td></tr>
<tr><td>S4=1</td><td>-</td><td>01</td><td>Failure with more than two errors</td></tr>
</table>

4.3.2.3 Circuit and Layout

In the circuit and layout design, the main improvements are focused on the SRAM cell design. Since the SRAM cell array takes over 60 % area of the whole memory, the improvement of the cell is quite efficiency. Some common-used schematics and corresponding layouts are analyzed as follow.

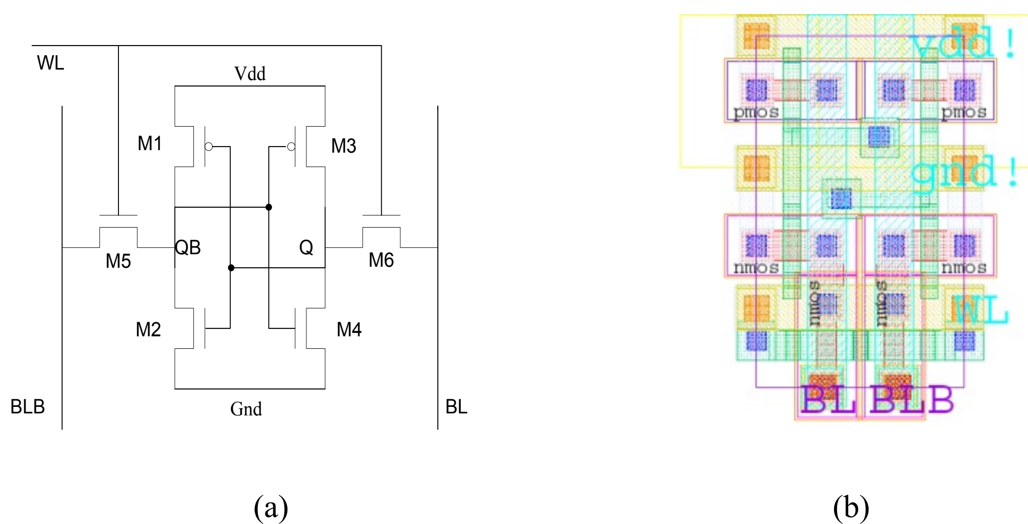
A. Standard 6T-Cell

Basic 6T SRAM cell is preferred for radiation hardness design. Fig. 4-22 shows a schematic and layout of standard 6T SRAM cell. The well and substrate taps of the layout are placed in special tap columns to minimize the area of SRAM array.

Since the well and substrate taps are not close to the sources of transistors as

standard digital cells, latchup effect becomes easier to be triggered due to the transient current pulse on the substrate or the wells. A common strategy to resist latchup effect is to adding guard rings between the complementary transistors. On one hand, the substrate resistance is clamped. On the other hand, the guard rings may appeal part of radiation-induced charges from the sensitive node. Therefore, both SEL and SEU tolerance can be improved with guard rings.

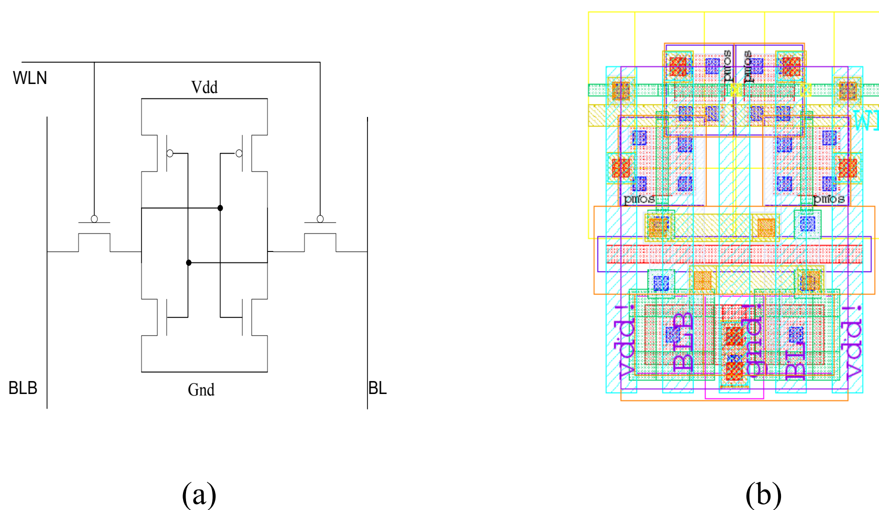
Another popular radiation hard technique is using the enclosed NMOS transistors for the mitigation of TID effects. However, the enclosed NMOS transistor has a very large W/L ratio. Moreover, the W/L ratios of transistors in an SRAM cell should follow certain cell ratio and pull-up ratio. The area of the 6T cell with enclosed NMOS layout is very large. Therefore, it is not proper for high density SRAM design.



(a) (b)

Fig. 4-22. Standard 6T-Cell, (a) Schematic, (b) Layout.

B. 6T-Cell with PMOS Pass Gate Transistor

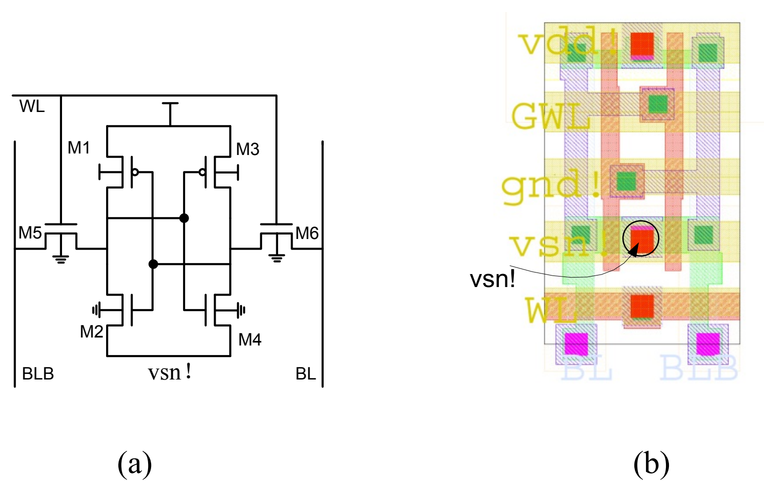


(a) (b)

Fig. 4-23. SRAM cell with PMOS pass gate transistors, (a) schematic, (b) layout.

Since PMOS transistor is TID tolerant in sub-micron process, the SRAM cell using PMOS transistor as pass gate is another choice in radiation hard design [72]. Thus, only the two pull down transistors are NMOS and require to be designed as enclosed transistors. However, the area is still difficult to be controlled. In order to reduce the W/L ratio of the NMOS transistor, the L is increased and only one of four sides the enclosed transistor is used. The rest three sides of the channel are totally covered by poly. Fig. 4-23 shows the schematic and the layout. The total area is 62.56 μm^2 in a 0.35 µm process. The area is almost two times of the area of the standard cell.

C. 6T-Cell with Reverse-Body Bias



(a) (b)

Fig. 4-24. Reverse-Body Bias 6T SRAM cell. (a) Schematic (b) Layout. The sources of two pull-down transistors are connected to a voltage (vsn!), which is higher than ground.

The other convenient strategy is to provide the source of transistors with reverse-body bias (RBB) voltage [73]. The aim is to raise the voltage potential of NMOS source. The threshold voltage of the transistor will be increased due to the well-known body effects. The TID-induced decrease of NMOS threshold will be compensated in some extent. This strategy is originally proposed for TID mitigation.

The tolerance to SEL of this strategy is also required to be discussed for using in high energy physics experiments. In the schema, the sources of NMOS transistors are connected to a voltage potential higher than substrate potential. That raises the emitter voltage potential of parasitic PNP bipolar transistors or reduces the emitter voltage potential of parasitic NPN bipolar transistors. Hence larger amplitudes of base voltage are required to conduct these bipolar transistors than that in a standard SRAM cell. The efficiency of this strategy depends on the source voltage of the pull-down transistors in SRAM cell. The voltage is limited by the static noise margin (SNM) of SRAM cell and power supply voltage. Therefore, the increased emitter-base voltage

on the NPN bipolar transistors cannot be very high. As a result, this strategy may not efficient enough for low power supply voltage. Moreover, the voltage drops due to the parasitic resistance on source power supply lines and currents through them will cause instantaneous voltage decrease on the NMOS sources and then invalidate the strategy.

D. SEU Hard SRAM Cell

One approach to alleviate the SEU effects is to reduce the peak of radiation-induced current/voltage pulse. If the radiation-induced voltage fluctuation is less than the upset threshold, the voltage can be recovered by the two invertors. For certain deposited charge, the voltage peak can be reduced by increasing the capacitance or resistance of the sensitive nodes. Therefore, the schematic as shown in Fig. 4-25 (a) [74] was proposed. However, the compacted large capacitance and resistance generally require to be fabricated in complicate process. Fig. 4-25 (b) shows another schematic, where the transistors P3, P4, N3 and N4 are used as resistors. The penalties of the approach are the increase of area and access time.

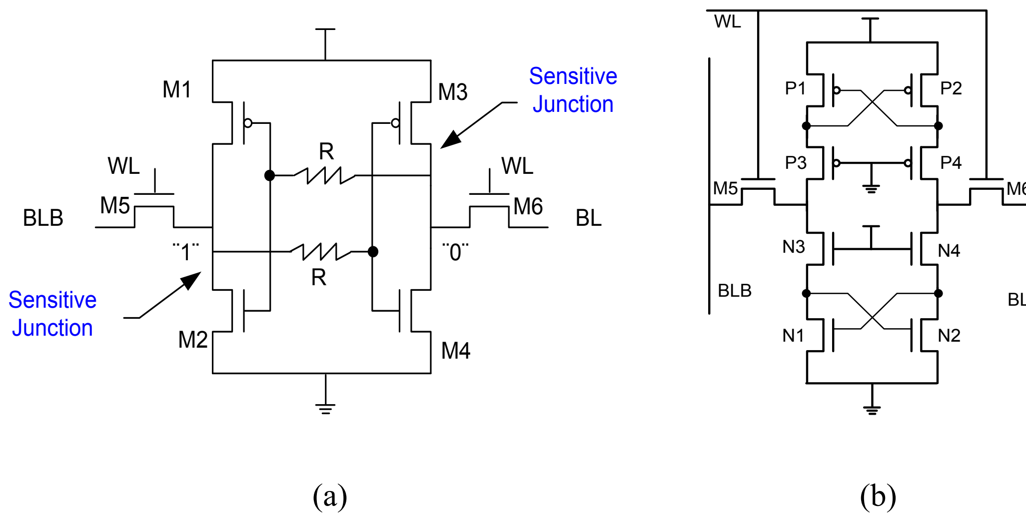


Fig. 4-25. SRAM cell harden by resistor, (a) resistor on gate, (b) 10T cell.

Another approach is to protect the storage node or one of the redundancy storage nodes from upset. The approach uses the knowledge that particle strikes in n+ diffusion can only induce upset from "1" to "0", while the opposite is true for p+ diffusions. For instance, the drains of M2 and M3 in Fig. 4-25 (a) are the sensitive nodes when the storage data is as shown in this figure. This approach is a very popular research subject, therefore a large number of different cells, such as ROCK, WHIT, LIU, HIT, HAD, DICE and so on [75-79], have been proposed. The cells using this approach usually take large area due to the additional redundancy or protect transistor. In addition, some cells have strict requirements at the peripheral circuitry.

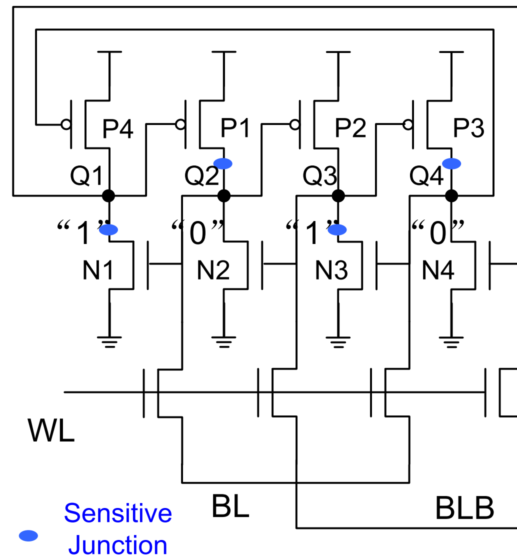


Fig. 4-26. SEU hard SRAM cell DICE.

Among them, DICE, short for dual interlocked storage cell, is a very popular schema due to the compacted layout. The schematic is shown in Fig. 4-26. Each transistor in storage part functions an inverter, hence no strict transistor ratios are required. The storage part consists of four pairs of latches. If upset happens on one of the latch, the adjacent latches are able to isolate the transfer of the upset. For example, the data in the latch consisted of N1 and P1 (Q1 and Q2) is upset, the data in the latch consisted of N3 and P3 (Q3 and Q4) will be preserved. When the particle-induced current disappears, the data of Q1 and Q2 can be recovered by the protected data Q3 and Q4.

4.3.3 **Prototype Design**

4.3.3.1 Design Considerations

In order to replace the SRAM IP core in MAPS, a direct way is to design a radiation hard SRAM with compatible electric characteristics and comparable performances. Among the main characteristics of the SRAM IP core, the bit density is difficult to be achieved for a radiation hard SRAM since the SRAM IP core uses the minimal layout design rules, and even violates them, for sake of high density. The area of an SRAM cell totally following layout design rules is about 20% larger than the area of the SRAM cell in the IP core. Moreover, additional area is required for using radiation hard layout techniques. For the SRAM in ULTIMATE, an acceptable area is two times of that of the SRAM IP core. The main characteristics of the required SRAM are summarized in Table 4-2.

Table 4-2 Main characteristics of the required SRAM

Items	Requirements
Process	0.35 μm standard CMOS twin-well process
Radiation Environment	10^{13} N_{eq}/cm^2 (non-ionizing radiation fluence) 300 krads/year @ 3.8×10^5 Hz/cm^2 (ionizing radiation dose and rate)
Operation frequency	50 MHz
Bit density	80 μm^2/bit
Power consumption	0.75 mW/MHz
Write peak current	100 mA
Read peak current	240 mA @ 0.4 pF load

The non-ionizing radiation-induced bulk damages may reduce the lifetime of the minority carriers in semiconductor. Since their operations depend on the movement of the majority carriers, MOS transistors are not sensitive to the non-ionizing radiation effects. The main ionizing effects including TID, SEL and SEU are thoroughly considered for the SRAM design.

Since a 0.35 μm process is adopted for the SRAM design, TID effects are alleviated due to the thin gate oxide. The function should be not affected. The enclosed NMOS layout technique limiting the leakage currents at the edges of transistors after long-term ionizing irradiation is given up for saving the circuit area. The speed of logic circuits may be varied due to TID-induced transistor parameter shifts [59]. However, the work of an SRAM strongly depends on the timing sequence of internal control signals. Therefore, the SRAM timing design should be tolerant to the speed variation induced by the TID effects.

The destructive SEL effect must be well solved since some particles with large linear energy transfer (LET) value exist in high energy physics experiments. Latchup-protected regulators have been designed in system level of the STAR experiments. The power supply of the sensors can be cut off by the regulators when the current flowing through power supply wires is larger than the threshold current of the latchup event. Thus, the sensors can be prevented from being destroyed. However, it generally takes some time to power down and power up the sensors due to the long-distance signal transmissions between the sensors, the latchup-protected regulators, and the control computers, as shown in Fig.4-27. As a result, additional dead time will be introduced if a latchup event happens. In addition, it is difficult to integrate the protected regulators into a MAPS chip. On one hand, the standard CMOS process is not immune from latchup, while the protected regulators should be free from latchup. On the other hand, some parameters such as the threshold current for powering off, and the duration of power-off should be preset. Therefore, the probability of SEL must be reduced on chip level for retaining the detection performance of MAPS.

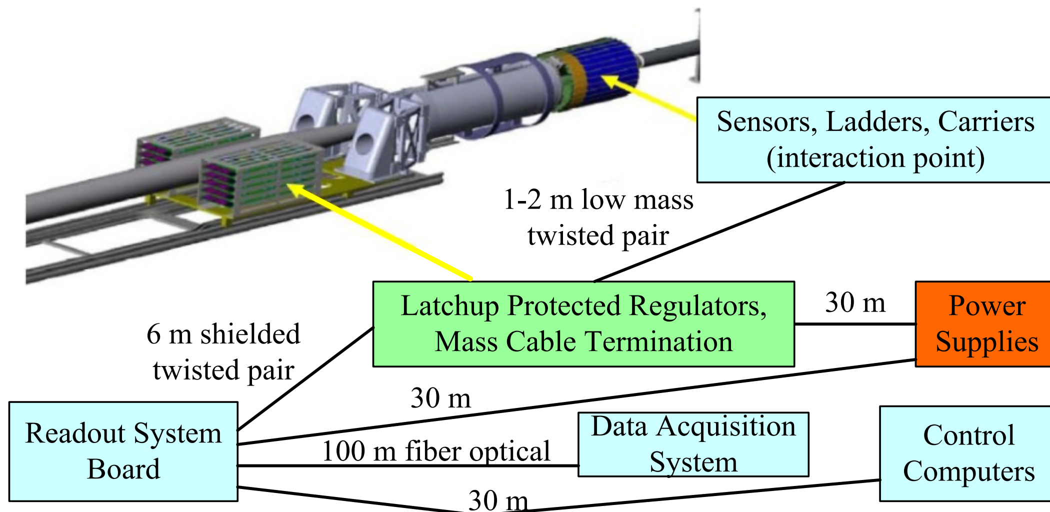


Fig. 4-27. Readout system for the PIXEL detector in STAR experiment. [80]

Most of the particles striking MAPS are minimal ionizing particles (MIPs) in high energy physics experiments. The LET value of an MIP is about 1.157 keV·cm^2/mg for silicon, which is far lower than the process intrinsic tolerance to SEU effects (in order of MeV·cm^2/mg). Since the SEU effects are not destructive, small amount of upsets are acceptable and can be disposed in system level by software design. Therefore, the SEU effects should be mitigated without much cost.

In short, the SRAM should be high immune from SEL firstly, then the timing should be promised under the radiation environment, and finally SEU effect should be improved without much area cost. Therefore, the critical issues are to construct a high latchup immune logic library and to design tolerant timing.

The SRAM cell array takes over 60% of the whole SRAM area. Thus, a critical issue is to design a radiation hard SRAM cell with a small area. In addition, an SEL hard logic library for the peripheral circuitry design and a TID tolerant timing design are required.

4.3.3.2 Radiation Hard SRAM cell

To get a high density SRAM, small area of SRAM cell is quite essential. Any little increase in the area of an SRAM cell will result in obvious increase of the whole area of the SRAM since tens of thousands cells are required.

The 6T SRAM cell, consisting of a flip-flop and a pair of NMOS pass-gate transistors, is preferred for radiation hard designs. The 6T SRAM cell can recover the storage node voltages quickly from an unwanted voltage pulse below the static noise margin (SNM) of the cell. In this design, the SNM is optimized to 600 mV as compared with 400 mV in a non-radiation hard SRAM cell by adjusting the transistor size ratios for a high SEU tolerance.

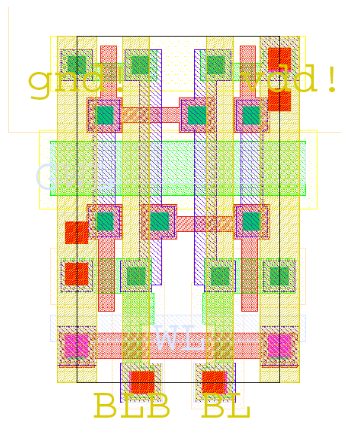


Fig. 4-28. Layout of the radiation hard SRAM cell

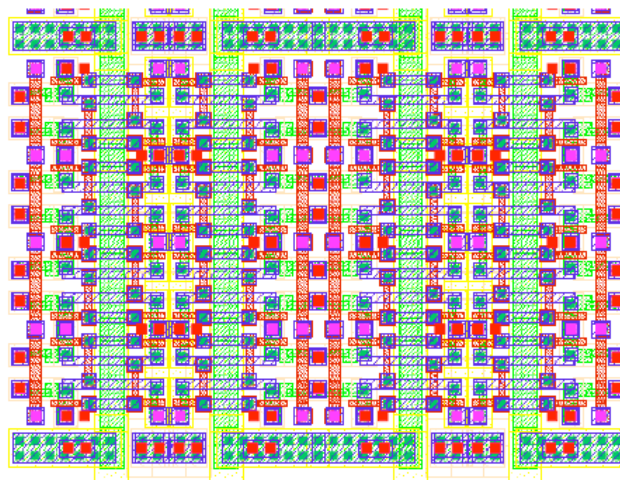


Fig. 4-29. Layout of the SRAM array of 4 × 4 cells

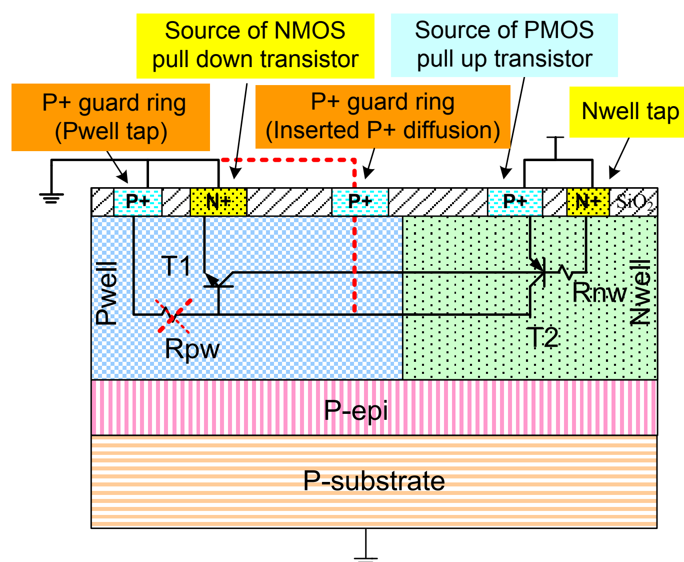


Fig. 4-30. Cross-section of the radiation hard SRAM cell

In the layout of the SRAM cell, P+ diffusion is inserted between NMOS and PMOS transistors, as shown in Fig. 4-28. Thus, P+ guard rings are formed by combining the inserted P+ diffusion and the P-well taps, as shown in Fig. 4-29. Fig. 4-30 shows the cross-section of the SRAM cell with parasitic thyristor and parasitic resistors. The P+ guard ring is connected to the ground level. Thus, the parasitic P-well resistor (Rpw) is shorted, and the radiation-induced transient currents on the P-well are led to ground. The amplitudes of the radiation-induced voltage pulses on the base of the NPN bipolar transistor are reduced. As a result, the parasitic NPNP thyristor is not susceptible to be conducted, and then high SEL immunity is achieved.

The TID effect is also mitigated, since the TID-inducing leakage paths between N wells and N+ diffusions are cut off by the inserted P+ diffusion. The leakage currents from drain to source of NMOS transistors and the leakages between different NMOS transistors still exist. These leakages may slightly increase the power dissipation and influence the speed of the logic, but don’t make function failure. Considering the cost of area, additional guard rings and enclosed-gate layout technique for avoiding the leakage paths are given up.

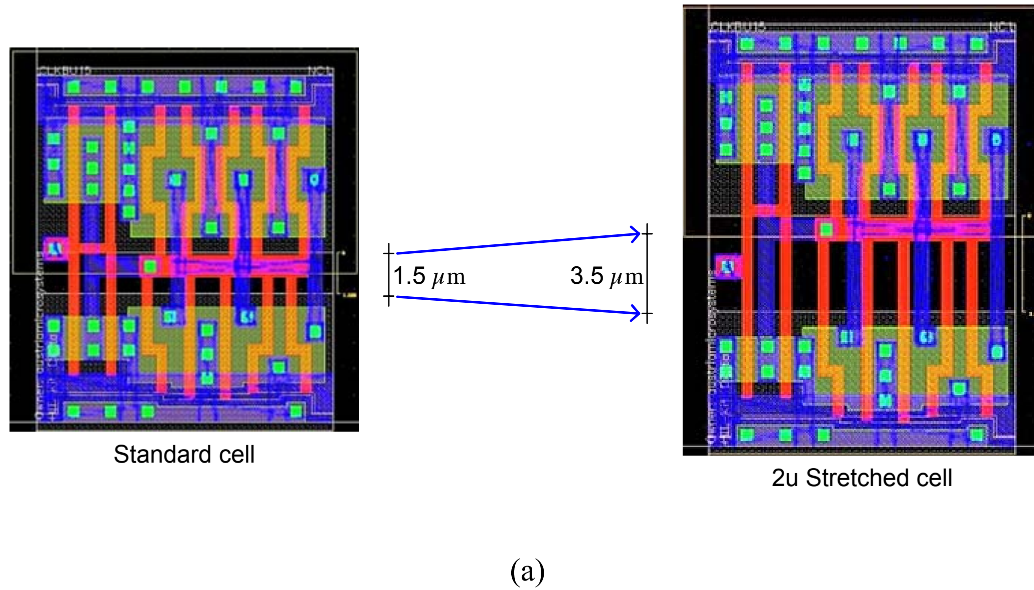
The SEU effects are also alleviated by the layout since the radiation-induced charge on sensitive nodes is distributed by the P+ diffusion. The critical charge is the product of the capacitance of storage node and the threshold of the cross-coupled invertors. The critical charge of this cell is higher than that of a non-radiation hard SRAM cell own to the optimization of SNM. In addition, the radiation-induced charge on the storage node is less than that in a non-radiation hard cell since parts of the charge is absorbed by the P+ diffusions. The redundancy structures for resisting SEU effects are not used for saving the circuit area. Finally, the designed cell area is $4.6 \times 7.975\ \mu m^2$.

4.3.3.3 Latchup Immune Logic Library

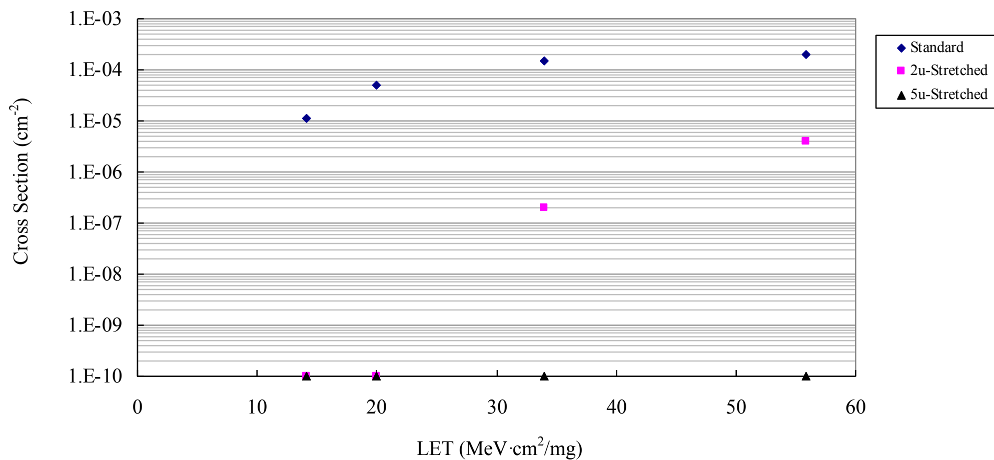
An effective approach to resist SEL effect is to add guard rings between NMOS and PMOS transistors as mentioned in Chapter 4.3.3.2 for the SRAM cell. On one hand, the polysilicon interconnections cannot be routed above guard rings. On the other hand, only three metal layers are available for the built-in SRAM. As a result, it will be difficult to use a logic library with guard rings for routing wires in limited area.

An alternative strategy is to increase the distance between NMOS and PMOS transistors. Fig. 4-31 (a) shows the layouts of a standard cell and the corresponding 2μ-stretched cell. A 2μ-stretched library and a 5μ-stretched library are built by stretching the distance between NMOS and PMOS transistors in an unhardened library provided by the foundry with 2 μm and 5 μm, respectively. Some circuits composed of D flip-flops, buffers, I/O pads were tested in order to evaluate the efficiency of this strategy [81]. The SEL test results of the circuits using the standard library, the 2μ-stretched library and the 5μ-stretched library are shown in Fig. 4-31

(b). The SEL tolerance for the 2μ-stretched library is two orders of magnitude higher than that for the standard library. For the 5μ-stretched library, no latchup events were observed.



(a)



(b)

Fig. 4-31. SEL test results of the standard, 2μ-stretched and 5μ-stretched logic libraries. The cross-section of 10^{-10} cm^{-2} indicates that no latchup events were observed at the points. [81]

The 5μ-stretched library is chosen for the peripheral circuit design of the radiation hard SRAM. Although the area of each logic cell is dramatically increased in this way, the whole area of the memory can be well controlled. Since the increased space will be used for routing the controlling wires in peripheral circuits, which are numerous and require even larger space.

4.3.3.4 Radiation Hard Timing Design

To perform a read/write operation, the timing sequence of internal control signals for bit-line pre-charge circuitry, word-line pre-charge circuitry, bit-line writing drivers, and output latches is critical. Traditionally, the required delays between the control signals are evaluated by calculating parasitic capacitance and resistance according to the given process parameters. The timing sequence is generated by using delay cells and logic circuits. Therefore, the design of precise delay cells and the evaluation of parasitic parameters are very important in the timing design. However, these tasks become much difficult under radiation environment due to the TID-induced baseline shifts of device parameters. If we leave a large margin in the timing sequence design, the power consumption of the SRAM will be increased and the speed of the SRAM will be decreased.

For this design, the radiation hard timing is implemented by a bit-line and word-line tracking technique. The idea is derived from a bit-line tracking technique for low power consumption SRAMs [82, 83] and a timing-control technique for configurable SRAMs [84]. In this thesis, the techniques are applied for radiation hard design in order to get a self-adaptive timing sequence by tracking the status of word lines and bit lines. Fig.4-32 shows the schema of the tracking technique in this design. The signal names in the figure are described in Table 4-3. A tracking column and a tracking row are added in the SRAM cell array. The tracking row is controlled by the global tracking word line (GWL_TRACK) and the local tracking word line (LWL_TRACK) due to the application of the hierarchical word line technique, which is illustrated in Chapter 4.3.3.5. The GWL_TRACK and LWL_TRACK signals are activated when any row in SRAM cell array is accessed. Thus, the timing information on the actual global word lines (GWL) and local word lines (LWL) is tracked for each read/write operation. The tracking of bit lines is implemented by the tracking column. The tracking bit lines (BL_TRACK and BLB_TRACK) are read out automatically when any columns are read out. When the output of the tracking column (DO_TRACK) is logic “0”, the outputs of the addressed columns are also stable to be latched. The timing sequence is ensured by the feedback of the LWL_TRACK and DO_TRACK signals.

Table 4-3 SRAM internal signal name description

Abbreviation	Description
CLK	SRAM system clock
GWL	Global word line
GWL_TRACK	Global tracking word line
LWL	Local word line
LWL_TRACK	Local tracking word line
BL	Bit line, positive

BL_TRACK	Tracking bit line, positive
BLB	Bit line, negative
BLB_TRACK	Tracking bit line, negative
DO_TRACK	Output of the tracking column
GWLPC	Global word line pre-charge, high active
GBLPCN	Global bit line pre-charge, low active
LBLPCN	Local bit line pre-charge, low active
GLATCH	Global output latch control, high active
LLATCH	Local output latch control, high active
GWE	Global write enable, high active
LWE	Local write enable, high active

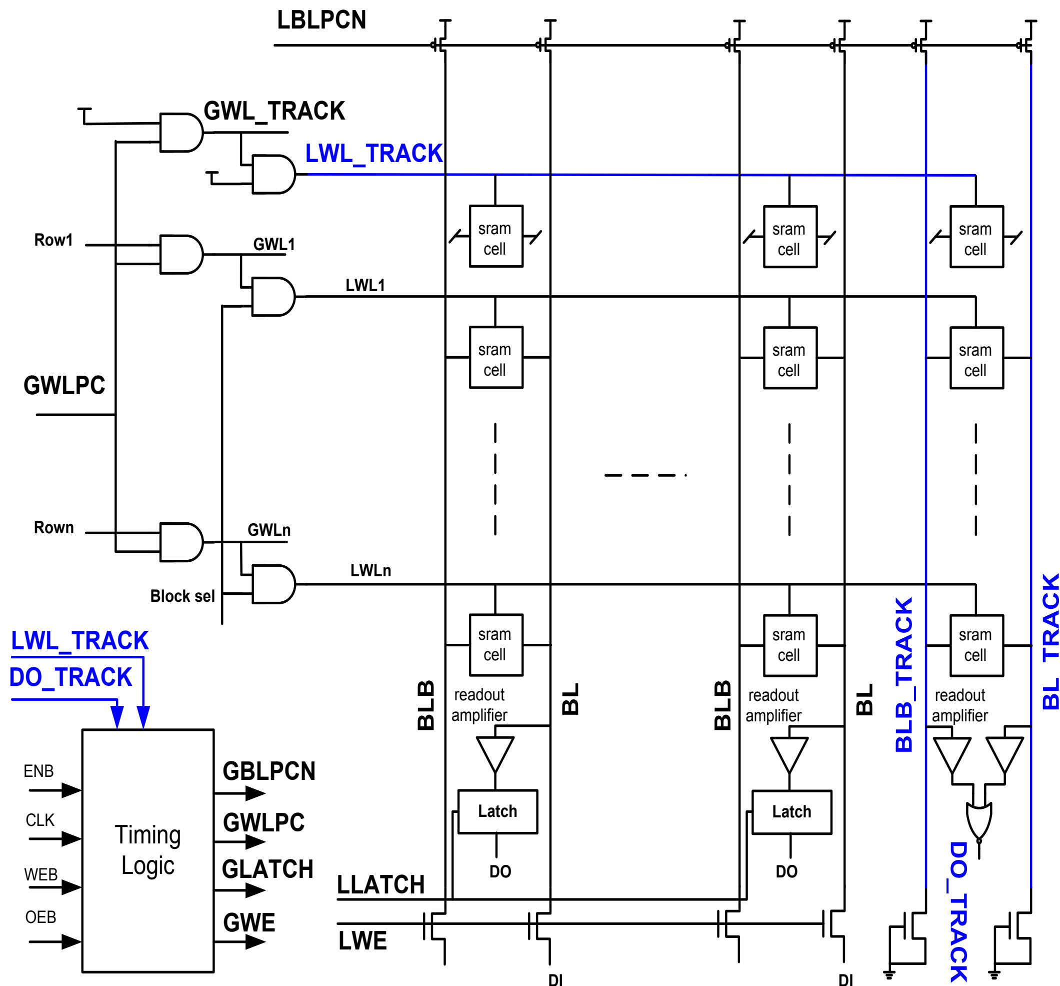
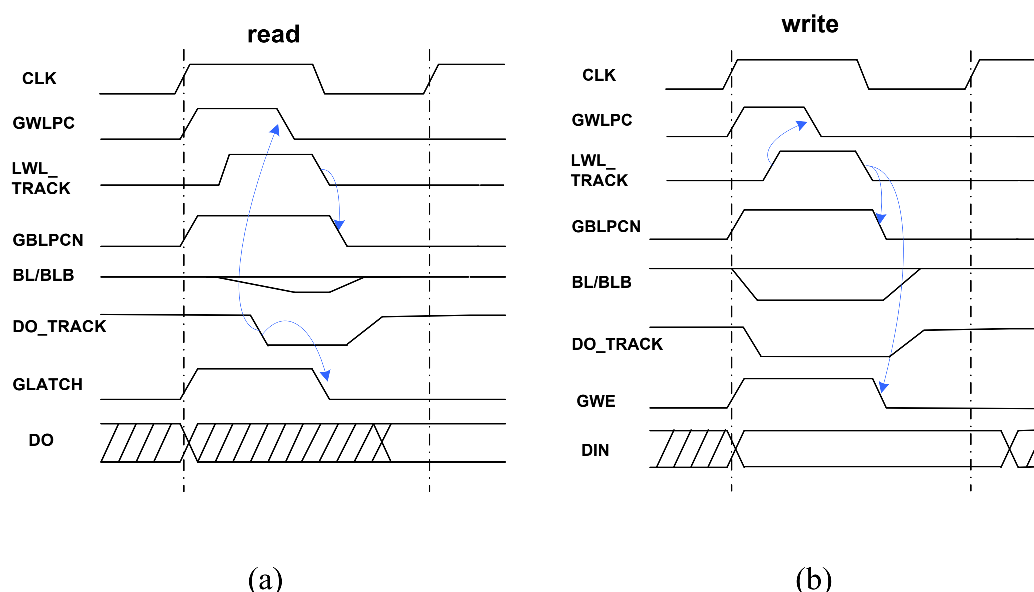


Fig. 4-32. Scheme of the bit-line and word-line tracking technique. The GWL_TRACK and LWL_TRACK signals track the timing information of word lines, and the DO_TRACK signal reflects the timing information of bit lines.



(a) (b)

Fig. 4-33. Timing sequence of the presented SRAM. (a) The timing sequence of a read operation. The negative edge of DO_TRACK is used to disable GWLPC and GLATCH, and the negative edge of LWL_TRACK is used to enable GBLPCN. (b) The timing sequence of a write operation. The positive edge of LWL_TRACK is used to disabled GWLPC, and the negative edge of LWL_TRACK is used to disable GWE and to enable GBLPCN.

Based on the scheme in Fig.4-32, the details of the radiation hard timing sequence are illustrated in Fig.4-33. All the bit lines are supposed to be initialed to power supply voltage during a reset period. For a read operation, the global word line pre-charge control (GWLPC, high active) is enabled and the global bit line pre-charge control (GBLPCN, low active) is disabled at the positive edge of the SRAM clock (CLK). The LWL_TRACK always follows the GWLPC. The delay time between the GWLPC and the LWL_TRACK is just equal to the sum of row decoding time and word-line driven time. The addressed local word line is active at the same time with the LWL_TRACK. The addressed SRAM cells and the tracking cell in the same row start to be read out simultaneously. When the voltage of the BL_TRACK/BLB_TRACK decreases to the threshold voltage of the readout amplifier, the DO_TRACK is turned to logic “0”. At this moment, all the addressed bit lines are ready to be read out. The negative edge of DO_TRACK is used to disable the GWLPC and the global output latch control (GLATCH, high active). The outputs are correctly latched. The LWL_TRACK again follows the GWLPC. The GBLPCN is reset by the negative edge of LWL_TRACK, and the bit lines are finally recovered to power supply voltage. As for a write operation, the start of the signals GWLPC, GBLPCN, and LWL_TRACK is the same as that for the read operation. Moreover, the global write enable signal (GWE, high active) is also activated at the positive edge of CLK for switching the input data to the bit lines of the addressed columns. Once

the input data are written on the bit lines, upsetting an SRAM cell only requires about 200 ps. The delay between the signals GWLPC and LWL_TRACK is enough for writing SRAM cells. Hence, the GWLPC is directly reset by the positive edge of LWL_TRACK. By the negative edge of LWL_TRACK, the GBLPCN and GWE signals are reset. The bit lines are recovered to power supply voltage finally.

The described timing design is adapted to TID-inducing speed variations since the timing sequence is totally asserted by the tracking bit lines and the tracking word line. In addition, the timing sequence can adjust itself according to the SRAM capability and the process dispersion since the tracking lines also reflect the timing information related to logic circuits, the size of SRAM cell array, parasitic devices and process parameters.

4.3.3.5 Architecture Design

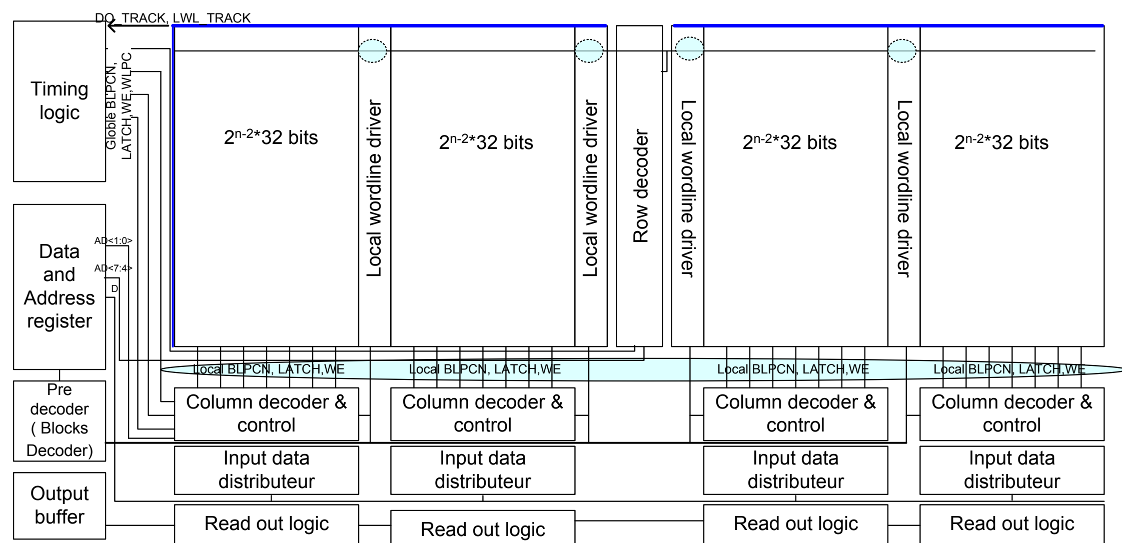


Fig. 4-34. Architecture of the SRAM

Fig. 4-34 shows the architecture of the SRAM. The SRAM is divided into four blocks in order to realize hierarchical word lines [85, 86]. As shown in Fig. 4-32, the local word lines (LWL1, …, LWLn) are derived from AND operations on the corresponding global word lines (GWL1, …, GWLn) and a block select signal. The loads of the global word lines are reduced since parts of the loads (such as pass gate transistors of the memory cells) are distributed into each block. As a result, the response of the word lines is sped up. In addition, the bit lines perform charge balance with the storage cells having an active word line during either a read or a write operation, and all the bit lines need to be recovered before next read/write operation. With the hierarchical word lines, the power consumption can be saved since only the local word line of the selected block is active. The hierarchical control technique is also applied to the other timing control signals GBLPCN, GWEN and GLATCH.

4.3.3.6 Experimental Results

For the ULTIMATE chip, two 1024 × 32 bit SRAMs (four 1024 × 16 bit SRAMs, in fact) are required. Originally, the peripheral circuitry and the hierarchical architectures were designed for the actual bit dimensions. An SRAM prototype configured with capability of 240 × 8 bits was realized in the AMS 0.35 μm standard CMOS process for functionality verification and performance evaluation. Fig. 4-35 shows the layout of the SRAM prototype. The tracking column is placed on the left side of storage array and the tracking row is arranged on the top of storage array in order to efficiently support the radiation hard timing design. The tracking word line and the tracking bit lines are matched with the other word lines and bit lines. The feedback signal LWL_TRACK goes the longest path. If the LWL_TRACK is active, the local word line of the addressed cells will be active. The tracking column represents the most distant cells to be accessed. The data from the exactly addressed cells will be ready to be output when the DO_TRACK is logic "0". In this design, all the bit access circuitries (including SRAM cells, bit-line pre-charge cells, readout amplifiers, readout latches, and bit-line writing drivers) and local word line drivers are designed with P+ guard rings. The 5μ-stretched library is used for the design of the peripheral circuitry (including row decoder, timing logic, data registers, address decoders, readout logic, and so on). The area of the SRAM core is 1000 × 375 μm^2.

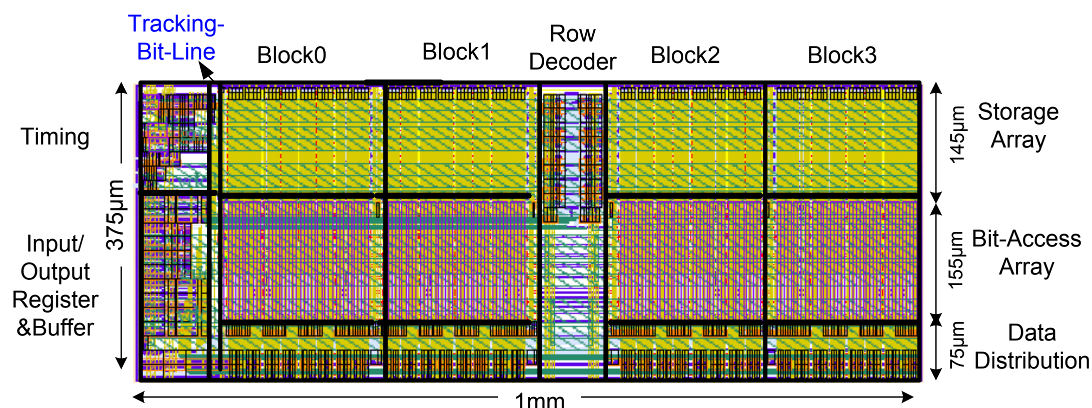


Fig. 4-35. Layout of the SRAM

To reconfigure a radiation hard SRAM with different bit dimensions, only the row decoder needs to be adjusted, while the storage array and the input registers can be reused. When a 1024 × 16 bit SRAM core is configured, the area is 1600 μm × 800 μm, which is suitable for the ULTIMATE chip.

The performances of the prototype are evaluated by post simulation. In typical case (PVT=process typical models, VDD=3.3V, Juction TEMPERATURE=25°C),

the access time of the prototype is about 4.3 ns. The average current is less than 15mA, and peak current is about 70 mA when clock frequency is 100 MHz and both the input address and data are turned over every time. The results indicate that the radiation hard SRAM is comparable with the IP memory on the other main performances.

A prototype chip including two SRAM cores (shown in Fig, 4-36) was implemented and fabricated in AMS 0.35 μm process in order to verify the function of the SRAM. The two cores based on the same schematic. The only difference is the layout of the SRAM cell. The upper SRAM core adopts 6T SRAM cell with P-diffusion isolation. The lower SRAM core adopts the 6T SRAM cell without P-diffusion isolation for compare.

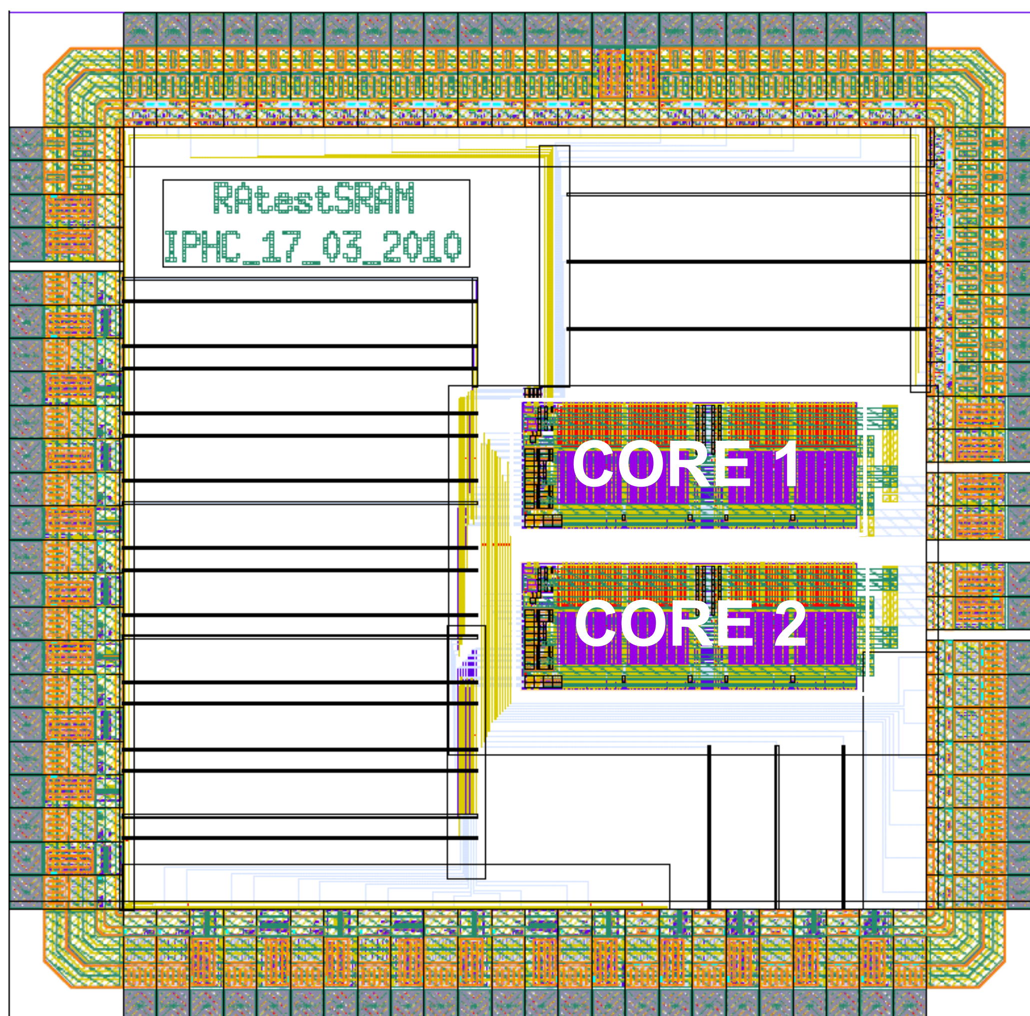
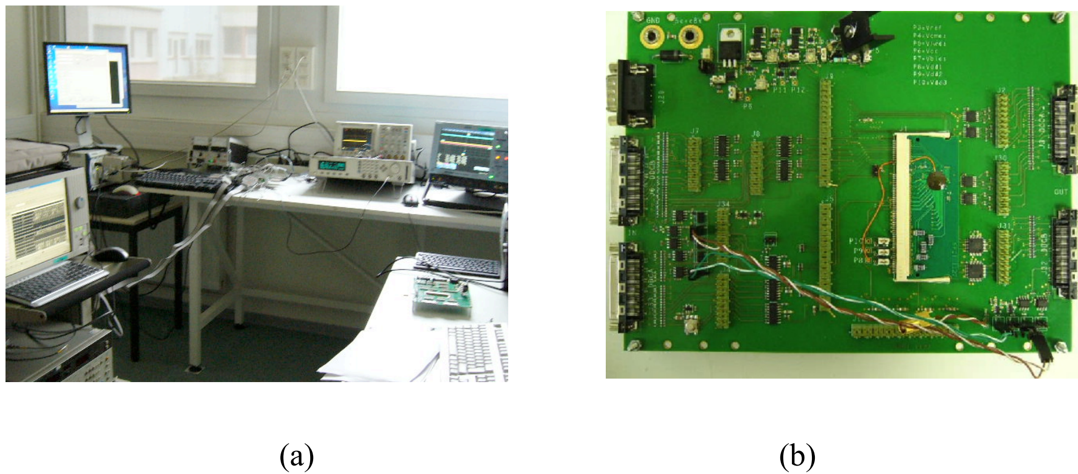


Fig. 4-36. Layout of Prototype Chip



(a) (b)

Fig. 4-37. Test of the prototype chip. (a) Test environment, (b) Test board.

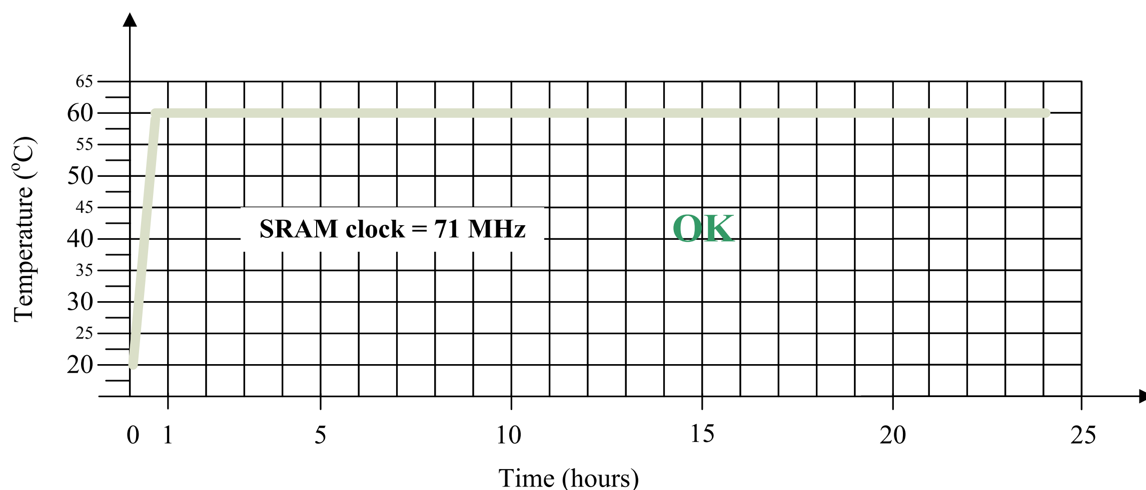


Fig. 4-38. SRAM temperature test results

The prototype chips were tested as shown in Fig. 4-37 with two configurations. One is using the Agilent pattern generator and data analyzer for characterizing and analyzing the data access time. The other is using the National Instrumentation FlexRIO7953r for the reliability test and the power consumption evaluation. The chips were characterized with SRAM clock frequencies from 5 to 80 MHz. Some test patterns covering all the memory addresses and different data types were tested without errors. The data access time and the power consumption were directly observed from an oscilloscope. The access time is about 8 ns (± 0.5 ns) with power supply of 3.3 V at 20 °C. At 60 °C, the access time has no obvious increase. The access time increases about 1 ns with the power supply of 2.9 V as compared with the power supply of 3.3 V. The average current is about 14.6 mA with power supply of 3.3 V and work frequency of 71 MHz. The test results demonstrate that the presented SRAM meets the design requirements. Temperature ageing tests were performed

since there is only an air-cooling system in the STAR experiments. As presented in Fig.4-38, the SRAM works correctly with operation frequency of 71 MHz at 60 ^{o}C for 24 hours. The longer-term tests are still need to be conducted for real application.

The radiation tolerance is evaluated according to the previous test results. As analyzed in Chapter 4.3.3.1, the SEU effects do not seem to be so critical for MAPS in the STAR experiments. Due to the optimization of the static noise margin and the layout of SRAM cell, the SEU tolerance of SRAM is not any more the main limitation in MAPS. The TID effects lead to insignificant leakage currents owing to the using of the deep submicron process. The radiation hard timing design makes the SRAM adaptive to the circuit speed variation resulting from TID effects. According to the Fig. 4-31(b), the SEL tolerance of 2μ-stretched library is close to 56 MeV·cm^2/mg. The SEL tolerance of the SRAM cell array should be higher than this value due to the insertion of P+ guard rings between NMOS and PMOS transistors. The peripheral circuitry designed with the 5μ-stretched library has even higher SEL tolerance. The SEL tolerance of the whole SRAM can achieve 56 MeV·cm^2/mg at least.

4.4 Design of Radiation Hard SRAM with enhanced SEU tolerance

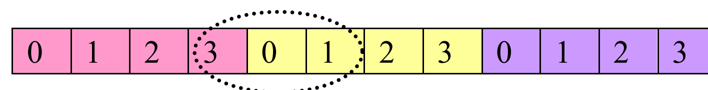
For sake of higher radiation tolerance, smaller feature size processes (such as 0.18 μm and 0.13 μm processes) are also used for the MAPS development. Recently, the MAPS design in 0.35 μm process is migrated in a 0.18 μm process. The detection area and resolution is kept. The main requirements of the SRAM, including the area, haven't been changed except a smaller feature size process. However, the critical issue for the radiation hard SRAM design is changed a lot for the new process. The area is not as strict as that in the design with 0.35 μm process due to the smaller transistor size. Due to the thinner gate-oxide and lower power supply voltage provided by the small feature size processes, the tolerance to TID and SEL would be enhanced. However, the SEU effects get much significant due to the reduction of SEU critical charge, which decreases with the power supply voltage. Therefore, the SEU tolerance must be improved in the design with the 0.18 μm process except considering the tolerance to TID and SEL.

4.4.1 Circuit Design

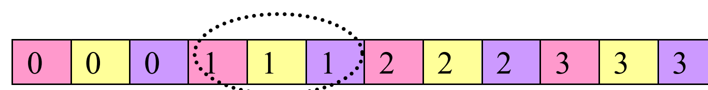
As presented in Chapter 4.3.2, the SEU tolerance can generally be improved by SRAM cell and EDAC technology. At first, the area cost and the radiation tolerance improvement of the two strategies are compared. DICE cell is a popular compacted

design due to the independent transistor ratio. However, the area of DICE cell is above one time larger than that of a standard 6T cell. The area cost of EDAC algorithm is mainly dependent on the bits of verification codes. Generally, the bits of verification code are less than the bits of original data in an efficient algorithm. Hence, the area cost of 6T SRAM with EDAC technique is less than that of a DICE SRAM. In addition, the DICE cell is only effective when the upsets happen on only one in four storage points. The upsets will be stored in DICE cell when the data stored in separated storage points are upset simultaneously. Therefore, the improvement with EDAC algorithm is chose for this design.

In order to minimize the required bits of verification code, the storage of the data should be studied to reduce the upset bits induced by a single particle. Fig. 4-45 shows two storage strategies of three four-bit data. Suppose the marked region is influenced and upset by a single high energy particle, two-bit correction is required for the data in Fig. 4-39 (a), while only one-bit correction is required for the data in Fig. 4-39 (b). If sixteen data in one row is stored by bit interleaving, multiple bit upsets (MBU) can almost be avoided. Under such case, only one-bit error correction and detection is required for solving the SEU. As the first proposal of EDAC algorithm to be used for avoiding SEU, two-error detection is also realized to obtain the probability of two-bit upsets, which will be used to verify the inference that multiple upset are rarely happened in high energy physical experiment. Finally, the Hamming Code (13, 8) presented in Chapter 4.3.2.2 is chose for the radiation hard SRAM design.



(a)



(b)

Fig. 4-39. The distributions of storage data, (a) general, (b) bit interleaving. Three 4-bit data are taken for example.

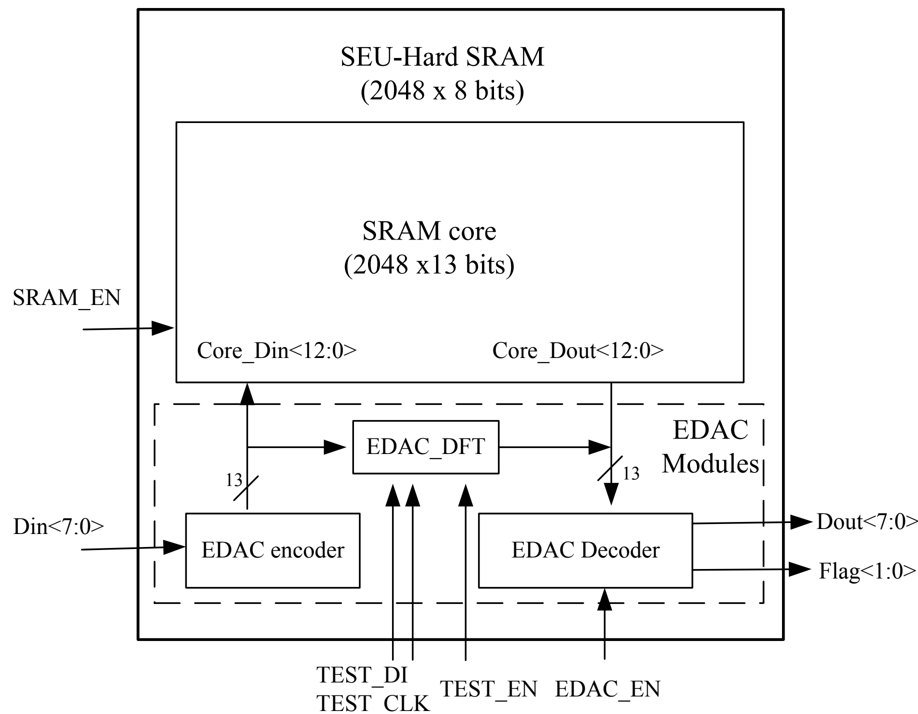


Fig. 4-40. Block Diagram of SEU Hard SRAM.

Fig.4-40 shows the block diagram of the radiation hard SRAM. An SEU hard SRAM with 2048 × 8 bits is realized by a standard SRAM core of 2048 × 13 bits enclosed by an encoder module and a decoder module, where the applied EDAC algorithm is realized. In this design, a module for testing the EDAC algorithm (EDAC_DFT) is designed by bypassing the SRAM core. The EDAC_DFT module provides two paths from EDAC encoder to EDAC decoder. In one path, the data is directly buffered. In the other path, the data from EDAC encoder is reversed and then buffered to EDAC decoder. The bits to be reversed are controlled by a serial input data and a test clock.

Considering the other ionizing effects, the radiation hardening techniques using in the 0.35-µm SRAM presented in Chapter 4.3 is also required. The SRAM cell is hardened by inserting guard rings or by enlarging the distance between NMOS and PMOS transistors. All the other circuits including the EDAC modules are designed with a SEL hard logic library, where the distance between NMOS and PMOS is enlarged 2 µm more than that in the standard library. In addition, the readout speed of the SRAM core is optimized by using a much sensitive readout amplifier. In order to realize the bit-interleaving data, hierarchical word line control is not utilized in this design. Therefore, large size SRAM should be realized by several SRAM cores for saving the power consumption and increasing the readout speed.

4.4.2 Experimental Results

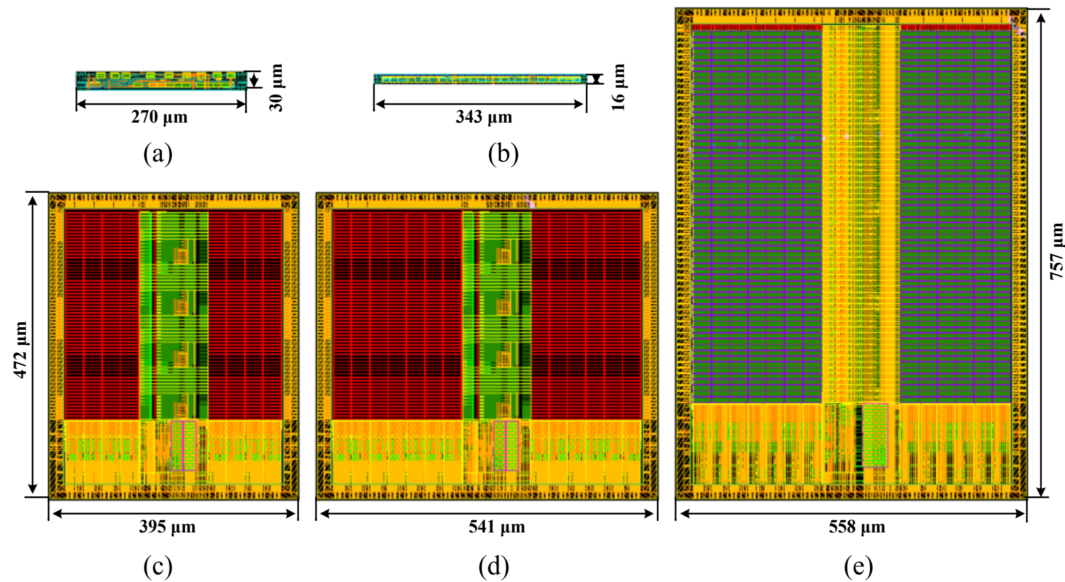


Fig. 4-41. Layouts of the SRAM components. (a) SEL hardened EDAC decoder, (b) SEL hardened EDAC encoder, (c) standard 2048 × 8 bit SRAM, (c) standard 2048 × 13 bit SRAM, (d) SEL hardened 2048 × 13 bit SRAM.

Table 4-3 Area comparison of the modules in SRAM

No.	Module Description	Area (μm^2)	Layout
1	SEL hardened EDAC decoder	270 × 30	Fig. 4-41(a)
2	SEL hardened EDAC encoder	343× 30	Fig. 4-41(b)
3	Standard SRAM core, 2048 × 8 bits	395× 472	Fig. 4-41(c)
4	Standard SRAM core, 2048 × 13 bits	541× 472	Fig. 4-41(d)
5	SEL hardened SRAM core, 2048 × 13 bits	558×757	Fig. 4-41(e)

Due to the integration of EDAC modules and the application of SEL hardened layout design, the radiation tolerance of the SRAM is satisfied, while the influences on the other performances are required to be evaluated.

At first, the area cost is evaluated. Fig. 4-41 shows the layouts of the main module in the proposed SRAM including EDAC modules and SRAM cores. The areas are listed in Table 4-3. The area cost of the two EDAC modules is quite small as compared to the SRAM cores. The main area cost of EDAC algorithm is the increase of the storage array for the verification code. In addition, addition area is required for SEL hardening. The required 2048 × 8 bit SRAM is the composition of the SEL hardened 2048 × 13 bit SRAM core and EDAC modules. The area is about 558 × 800

μm^2, which is 2.6 times of the area of the standard 2048 × 8 bit SRAM. The bit density of the required SRAM is about 27 μm^2/bit, which is quite high for MAPS chips.

The timing of the SRAM with EDAC algorithm should be redefined. The encoding and decoding of the EDAC algorithm lead to increases of the data setup time and the data access time of the SRAM, respectively. The periods required for encoding and decoding of the EDAC algorithm are about 1.2 ns and 2.6 ns, respectively. The main changes of the SRAM timing are listed in Table 4-4. The unlisted timing parameters are not influenced.

Table 4-4 Timing parameter comparison of SRAM with and without EDAC

Parameter	**SRAM with EDAC**	**SRAM without EDAC**
Clock cycle time (ns)	10	5
Data access time (ns)	5.6	3
Data setup time (ns)	2	0.8

The power consumption is almost not influenced. The average current and the peak current are about 13 mA and 218 mA whether with or without EDAC modules in typical case simulation (PVT=process typical models, VDD=1.8 V, Juction TEMPERATURE=25°C), respectively.

Finally, a prototype chip with four 24K × 8 bit SRAMs was realized in a 0.18 μm standard CMOS process, as shown in Fig.4-42, for functionality verification and performance evaluation. Each SRAM is composed of twelve SRAM cores. The capability of SRAM core is 2048 × 13 bits for radiation hard SRAM and is 2048 × 8 bits for non-radiation hard SRAM. The EDAC modules (EDAC_encoder, EDAC_decoder, EDAC_DFT) are placed at the side of the SRAM cores. According to the requirements of the MAPS chip, different capability of SRAM can be realized by reconfiguring the number of the SRAM cores.

The prototype chips were tested with the NI FlexRIO7953r, as shown in Fig.4-43. The read and write operations were performed correctly at 20 MHz. The EDAC algorithm was significantly verified by upsetting the data from the EDAC encoder. The results demonstrate that the algorithm is correctly realized. The data access time was observed from an oscilloscope. The access time is about 8 ns with enabling the EDAC algorithm and is about 6 ns with disabling the EDAC algorithm.

In one word, the required SRAM resisting to SEL and SEU is successfully realized in a 0.18 μm process. The main penalties are the increase of area by 1.26 times and the increase of data access time with about 3 ns.

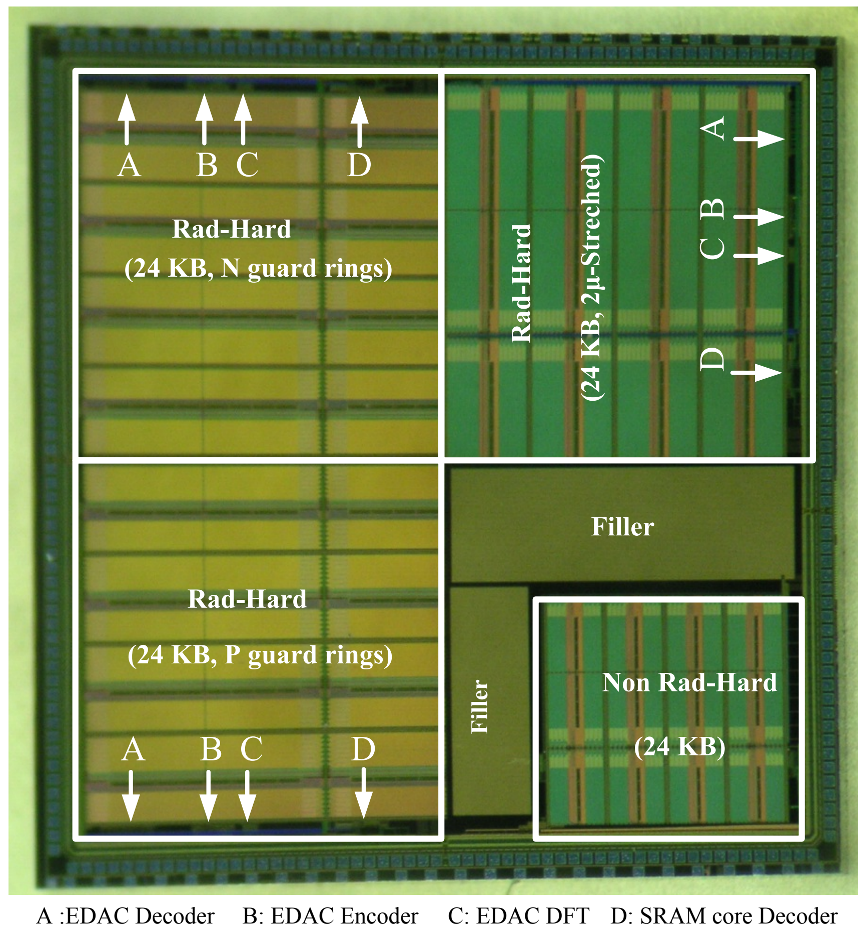
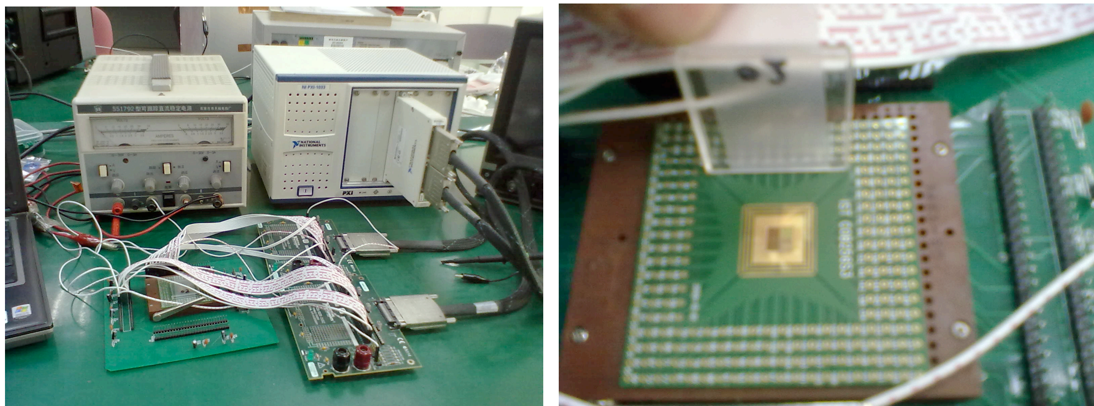


Fig. 4-42. Micrograph of the prototype chip. A non-radiation hard SRAM is realized on the bottom right corner. The other three SRAMs are hardened by the EDAC algorithm, the 2μ-stretched logic library and the radiation hard SRAM cells (with P+ guard ring layout, N+ guard ring layout or 2μ-stretched layout)



(a) (b)

Fig. 4-43. Test of the prototype chip. (a) Test environment, (b) Chip under test.

4.5 Proposal of a Dual-Port Memory Based on a 2T Cell

The capability of the memory is prone to be increased for the future high physical experiment since the MAPS are prone to be higher accuracy and larger detection area. Although the pixel pitch may be decreased by integrating a 4-bit column level ADC [22], the data need to be buffered by memory is increasing. In addition, comparing with STAR experiment, the radiation environment of some other experiments (such as LHC, ILC) is much harsher on total dose and particle rate. The details have been described in Chapter 2.

Under such case, the required capability of the memory will be increased and the requirement of radiation tolerance will be higher in the future. Moreover, it is worth to mention that the larger of the memory capability, the worse of the radiation tolerance. Therefore, the memory area and the required capabilities of the system should be reduced. In this part, an original 2T Cell with small area and a FIFO structure memory are proposed for solving these problems.

4.5.1 Proposal of using DRAM Cell

A memory generally can be implemented by an SRAM or a DRAM. 6T SRAM is widely used in monolithic chip due to power consumption and standard CMOS process compatibility. However, DRAM can generally achieve four-time density of an SRAM. Moreover, a DRAM cell can be free from latchup since the NPNP structure may be avoided. The disadvantages of a DRAM cell are obvious. Firstly, three-dimensional structures such as trenches etched into silicon and stacked layers rising above the surface are required in fabrication process to get large storage capacitance with high density. Secondly, storage data should be refreshed frequently to avoid data loss due to leakage currents. As a result, power consumption is high and access speed is low. Thirdly, the storage node is susceptible to upsets since radiation induced charges can be accumulated on storage capacitors.

In MAPS, the memories are used as buffers. The storages data only need to be maintained for one frame period, which is about 200 μs. A total leakage current in the order of picoampere can be accepted. As a result, the additional data refresh operation is not necessary. Therefore, the storage capacitor does not need to be very large and can be implemented by MOS transistor.

For a single storage cell, the SEU effect is not accumulated because rare successive hits happen on the same cell. The possibility of successive hits on the same pixel is very small in effective sensors. Under the same irradiation environment, the possibility on a certain memory cell is less, since the DRAM cell area is much less than pixel area. Therefore, it is possible to realize a high radiation tolerant memory with a DRAM based cell.

4.5.2 **Design of a 2T Cell**

4.5.2.1 Circuit Design

Fig. 4-44 shows two schematics of 2T memory cells, which is compatible with standard CMOS process. Both of the cells consist of only PMOS transistors to avoid the parasitic thyristor structures. Thus, the cells are totally free from SEL. Fig. 4-44 (a) is a general single port DRAM cell but is implemented with PMOS pass gate and PMOS storage capacitor. Fig. 4-44 (b) is a dual-port memory cell. M1 is a pass gate for writing a data. M2 is used as a storage capacitor and read access transistor. Data on write bit line (WBL) is written by activation of word line (WL), and stored at node Q. Before read operation, read line (RL) and read bit line (RBL) are initialized to ground voltage level. Then, read operation is performed by setting read line (RL) to high voltage and sensing the voltage or current variation on read bit line (RBL). If the voltage potential or current achieves a certain value, the storage data is thought to be ‘0’. Otherwise, the data is ‘1’. Both RL and RBL are recovered with ground potential after read operation.

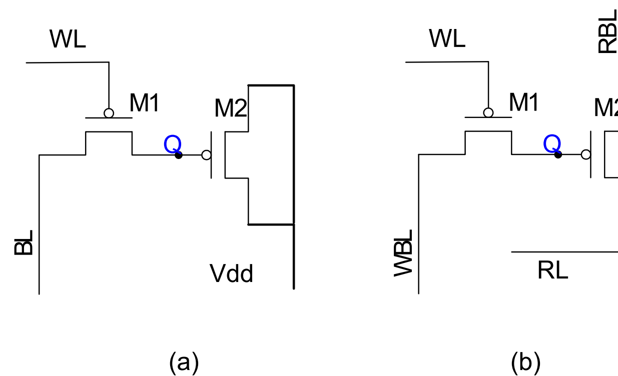


Fig. 4-44. Proposed 2T memory cells. (a) Single port cell (b) Duel port cell.

The dual port cell is quite interested in the applications of MAPS, since it is possible to be used for reducing the required memory capability. The design of the dual port cell is significantely described in the following.

The radiation tolerances of the dual-port DRAM cell are addressed on SEL, TID and SEU effects. Firstly, the cell is immune from SEL due to only one kind of transistors. Secondly, TID effects including leakage currents and parameter shifts are mitigated by applying PMOS and a thin oxide process. Thirdly, SEU effect can be minimized by increasing the critical charge of the cell and reducing the charge

collection efficiency of storage node.

The critical charge in this cell can be defined as the dynamic range of storage charges (Qq) for “1”or “0”. The critical charge depends not only on the storage charges but also on the threshold of the drain current for read operation. The current depends on the size of transistor M2 and determines the readout speed. The critical charge Q_{crt} and readout time T_{read} can be formulated by

$$Q_{crt} = C_{store} \cdot \Delta V_Q$$

$$T_{read} = \frac{C_{RBL} \cdot \Delta V_{RBL}}{I_{read}}$$

where, C_{store} is the capacitance of the storage node. ΔV_Q is the maximal voltage range corresponding logic ‘0’ or ‘1’. C_{RBL} is the load capacitance of read bit line. ΔV_{RBL} is the expected voltage variation during read operation. I_{read} is the drain-source current of M2 when logic ‘0’ is read. It mainly depends on the voltage of node Q.

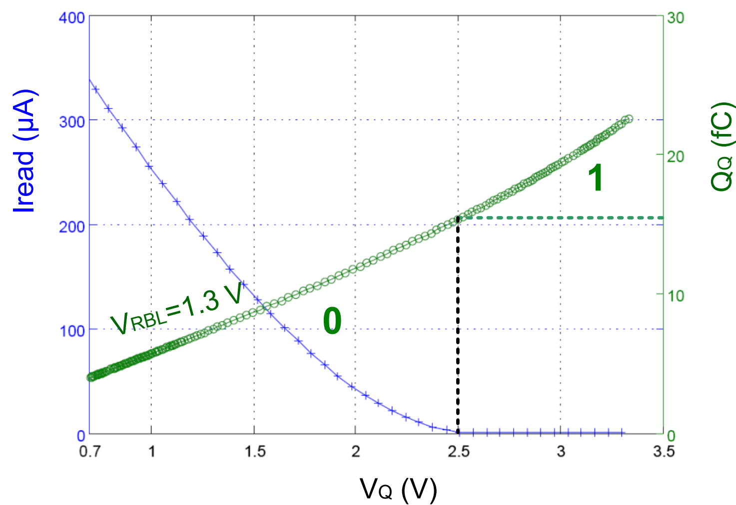


Fig. 4-45. Read operation current and storage charges versus voltage of storage node.

Fig. 4-45 shows the dependence of Q_{crt} and I_{read} on the voltage of storage node (V_Q). The threshold of readout current is selcected as 10 µA, which crresponds to 2.5 V of the storage voltage and 80 ns of an access time for 800 fC of C_{RBL}. The critical charges are about 11.4 fC and 7 fC for ‘0’ and ‘1’ respectively. In this design, the leakage currents of storage node include gate leakge of M2, P-N junction leakage of node Q and the source to drain leakages of M1. The total leakage current is less than 1 pA before irradiation. For a period of one frame, the total charge is 0.2 fC. It is far from 11.4 fC or 7 fC. The radiation induced currents should be also considered. Since a particle hit will lead an increase positive charges on the storage node, the critical

charge for logic ‘0’ will be decreased. Considering the charge feedthrough during a read operation, radiation-induced threshold increasing and the well-known body effects, a possible and safe voltage range for logic ‘0’ will decrease. The corresponding critical charge for SEU effect decreases as well, but it is still larger than 4 fC of SRAM critical charge.

In addition, the SEU effects can be mitigated by reducing the charge collection efficiency of storage node. This is implemeted by a dedicated layout design, shown in Fig. 4-46. In this cell, the sensitive node is the P-diffusion connected with node Q. Since most of the generated holes will be collected by substrates and the p- diffusions around, the hole collection effiency of Q is small.

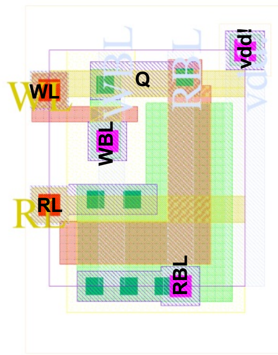


Fig. 4-46. Layout of the proposed dual port DARM cell

4.5.2.2 Performance Evaluation

A 2T memory cell is designed in 0.35 μm AMS process to verify the proposed design. Fig. 4-46 shows the layout. The cell area is $4.55 \times 5.45\ \mu m^2$. It is smaller than a standard 6T SRAM cell and is 26% of the area of described PMOS pass gate SRAM cell.

The designed cell is simulated with capacitive loads of 100 fF, 250 fF, 250 fF and 800 fF on WL, WBL, RL, RBL respectively, which correspond to an array of 64 × 32 bits. The simulation results are interpreted in Fig. 4-47. The read and write operations are functional and the access periods are 1.14 ns and 61.67 ns respectively. In extreme condition, the read access time is 80 ns in worst case.

Radiation tolerance on SEL and TID effects of the proposed cell is obvious due to only PMOS transistors. The SEU rates can be accepted in STAR experiment. MAPS is used to detect minimal ionizing particle (MIP). The deposition energy of MIP produces 80 e-h pairs per micrometer for silicon. The total charges are about 4000 e-h pairs for 50 μm silicon bulk, namely 0.64 fC. If the charge collection efficiency of the sensitive node is less than 5 %, the critical charge is nearly 500 times of the maximal collected charges.

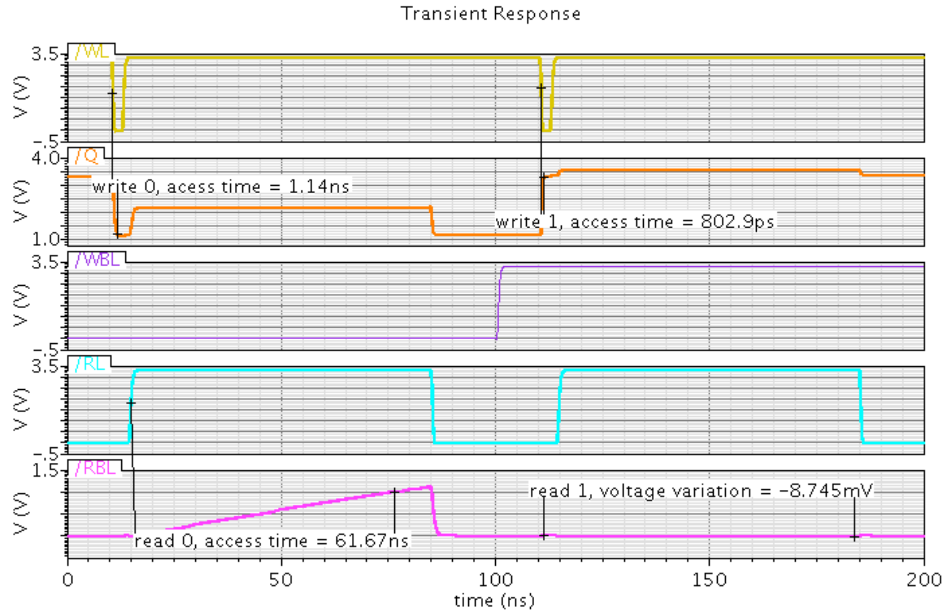


Fig. 4-47. Simulation results of read and write operation

4.5.3 Design of a Memory Based on the 2T Cell

4.5.3.1 Concept Design

The timing sequence of Memory in MAPS is extracted as Fig. 4-48. The system clock frequency is 80 MHz. The pixel-level signals are read out row by row in a frequency of 5 MHz. The write operation frequency of the memories is decided by maximal data for one row. The maximal frequency is 25 MHz. The read frequency is designed to be as low as possible for lowering the frequency of LVDS transmitters. In ULTIMATE Sensor, the maximal read frequency is 5 MHz. The frame frequency may achieve 10 kHz. The frequency is about 5 to 6 kHz in MIMOSA 26 [51, 87].

If a dual-port memory is used, the data can be read during the same frame. The readout contents can be reused, thus the required memory capability can be decreased. The penalty is that a frame head may be required. In the worst case, all the data are written in the last 40 µs of one frame. Namely, all the particles hit the last rows of the sensor. During the 40 µs, more than 40% addresses of the memory are read out and can be reused for writing. Thus, the total required memory capability can be reduced about 1/3. The actual required capability will be much smaller considering the distribution of the incident particles.

Since the memory in MAPS is accessed by continuous addresses, it is configured as a FIFO memory to reduce the load of memory control logic. Moreover, the address lines from the memory controller to memory can be suppressed. By suppressing these

long and high frequency lines, the power consumption is reduced and the reliability of the circuits is increased. In addition, the memory controller will not need to be modifying when extending the capability of FIFO.

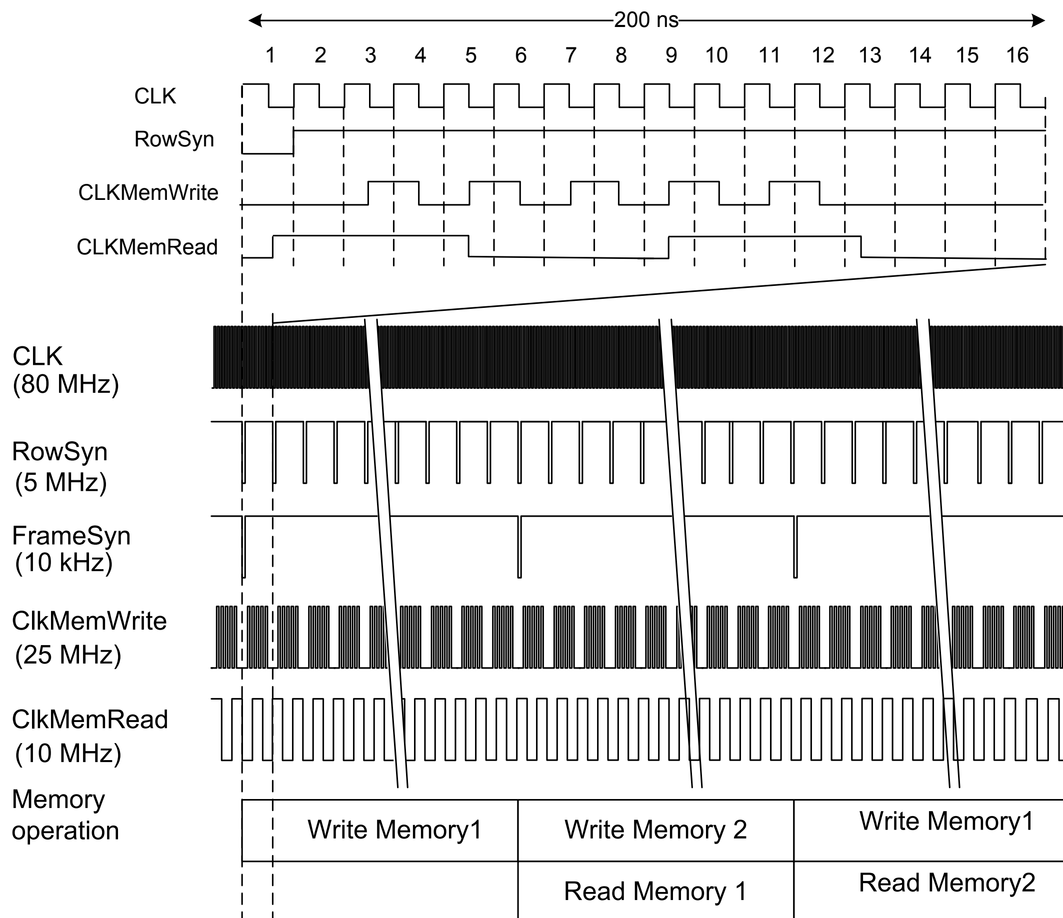


Fig. 4-48. Memory control sequence

4.5.3.2 Circuit Design

The design of the radiation hard FIFO adopts the same techniques with the SRAM. The 5μ-stretched logic library can be used for the peripheral circuit design. The radiation hard timing control technique is also applied. Fig. 4-49 shows the block diagram. The modules of write driver, input data distribution, pre-charge, output latch and output driver are almost same with an SRAM design. Since the two ports should be provided for read and write operations, respectively, two timing logics and two address decoders are required. A tracking column and a tracking row are designed for the radiation hard timing control. The tracking of WL is feed backed to write timing logic and the tracking of RL and DO is feed backed to read timing logic. The hierarchical signal control is also used. Based on the presented memory design techniques, the difficulty associated with the FIFO design is related to generating the

FIFO pointers and finding a reliable way to determine full and empty status on the FIFO.

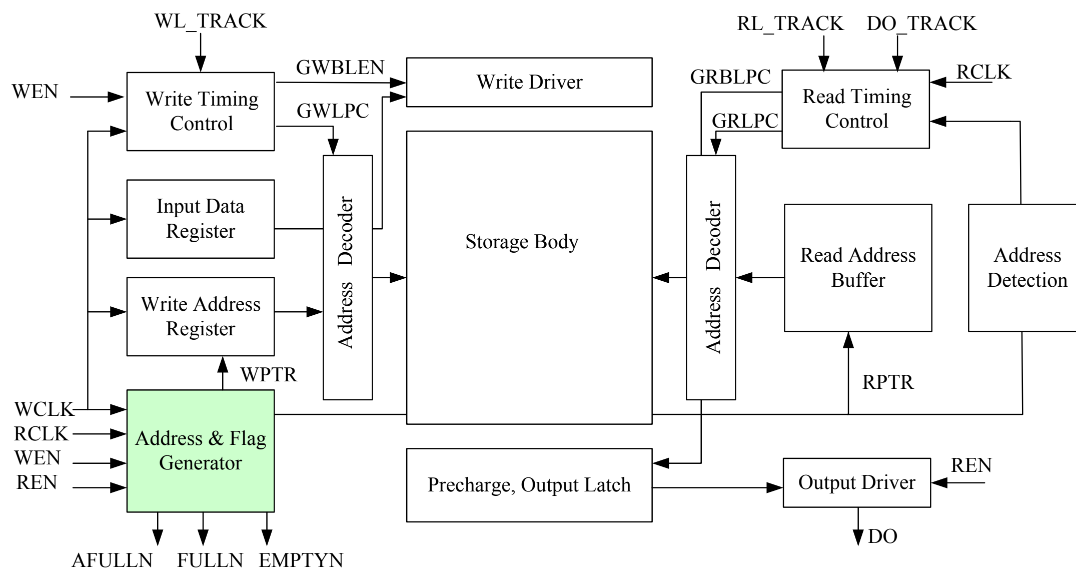


Fig. 4-49. Block diagram of the FIFO

Before the FIFO design, we make some assertions. The write pointer is the next address to be accessed and the read pointer is the present read address. When there is a read or write operation, the corresponding pointer is incremented to the next address. If the FIFO is full or empty, the pointer will be hold. Namely, the last address will be accessed. Therefore, a key issue of FIFO design is to judge whether the memory states is full or empty status.

Generally, the full or empty status can be judged by comparing the write address and read address. One approach is to synchrony the address and then to compared them [88]. Trying to synchronize a binary address from one clock domain to another is not reliable because each bit of the address may be change simultaneously. By using the general synchronizing circuits consisting of two flip-flops, the sub-stable status can be avoided, but the results can be the status either before or after the clock. Therefore, the address is generally converted to Gray Code (where only one bit will be changed between the successive data) before the synchronization. Another interesting approach is to perform asynchronous comparisons between the FIFO write and read pointers and then synchronize the compare results [89]. The asynchronous comparison method uses fewer synchronization flip-flops. Gray code is also used in asynchronous comparison to reduce the unwanted glitches.

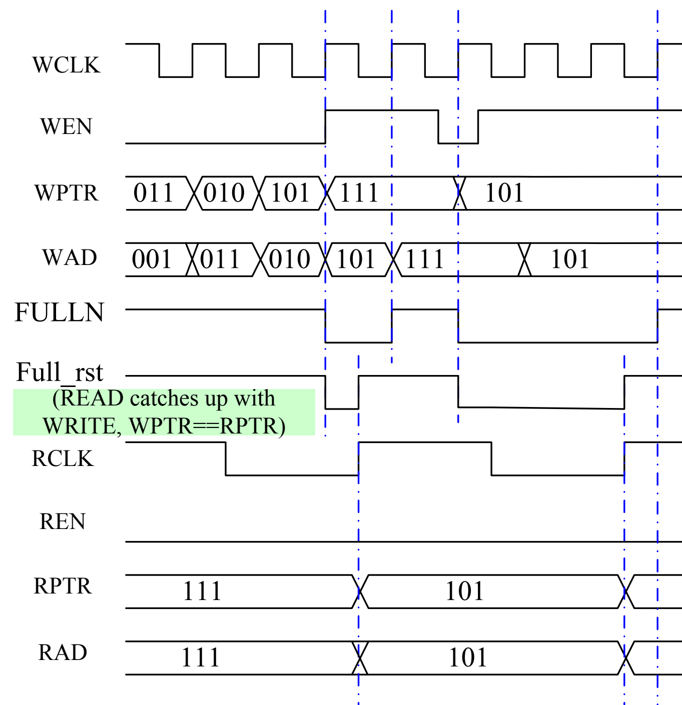


Fig. 4-50. Generation of full signal (FULLN).

In MAPS, the read clock and the write clock are synchronized by the system clock. The timing can be promised during timing analysis. The gray code is still necessary during comparison in order to remove the unwanted glitches. Another important issue is to yield the correct status. In this thesis, the asynchronous comparison method is adopted. According to our assumption of the read or write pointer, the full is asserted when writer pointer catch up read pointer and the empty is asserted when read pointer catch up write pointer. The full status is asserted by write operation and disabled by read operation. Therefore, the disable edge of full signal should be synchronized with write clock for timing analysis tools. Fig. 4-50 shows the generation of full signal (FULLN). It is asserted when the read pointer catches up with the write pointer. Almost full signal (AFULLN) is also given when half of the contents are used for future content evolution. On the contrary, the empty is asserted when write pointer catches up with read pointer. During the reset period, the FIFO is empty and the output data is invalid. After a write operation, an internal read operation is performed and the output data is set to be valid. Thus, reliable read and write operation can be performed without additional clock period.

4.5.3.3 Simulation Results

The final FIFO is configured as 1024 × 16 bit. The read and write access cycles are designed as 100 ns and 10 ns respectively. The whole surface is evaluated as 1600 μm × 600 μm in the AMS 0.35 μm process, which is 75 % of the area of SRAM with

same capability. The actual required capability needs to be evaluated according to the hitting distribution and system design. In STAR experiment the existing infrastructure require full frame events to the data acquisition (DAQ) systems, the FIFO can be used in pipeline mode as the IP memories without redefining the capability.

Owing to the limited research funds, this design didn't fabricated. However, the feasibility and potential benefits of the proposal have been demonstrated in the design and analysis. Overall, the 2T-cell-based FIFO not only saves some surface but also has high radiation tolerance. The FIFO is immune from SEL and TID effects and higher radiation tolerance on SEU than the designed SRAM, as explained in Chapter 4.4.2. In addition, the SEU can be improved in the future with EDAC technique due to the saved area. Therefore, the 2T-cell based FIFO is a potential choice for future MAPS design. The design of the FIFO is still need to be further developed in the future to explore the potential benefits.

4.6 Conclusion

With the requirements of high readout speed and high TID tolerance, fast readout MAPS are conceived by integrating a data compression block and two SRAM IP cores. However, the radiation tolerance of the two SRAM IP cores is not as high as for the other parts in MAPS and mitigates the radiation tolerance of the whole MAPS chip. Especially, the SRAM is sensitive to the SEE effects including SEU effects. Therefore, three radiation hard memories are designed for the present and future MAPS chips. Firstly, a radiation hard SRAM prototype is realized and verified in a 0.35 µm process according to the requirements of STAR experiments. Secondly, a prototype chip of radiation hard SRAM with EDAC algorithm and bit-interleaving storage is designed and tested when the fabrication process is migrated to 0.18 µm process. Finally, a FIFO based on a 2T cell is proposed and evaluated for future high energy physical experiments.

5 MAPS Radiation Hardness with New Available Processes

5.1 MAPS with High Resistivity Epitaxy Process

The sensing elements of MAPS were found to be sensitive to the reduction of carrier lifetime due to the non-ionizing radiation. This phenomenon is related with the charge collected by the relatively slow thermal diffusion. The charge lost in this way can be compensated by an accelerated charge collection. In order to reach this purpose, the pixel pitch has been reduced. With small pixel pitch, a large number of pixels are required for a certain area to be covered. As a result, power consumption and readout time will be increased. An alternative way to accelerate the charge collection is to deplete the sensing volume and then to reduce the carrier recombination [90]. The standard CMOS process with epitaxy resistance of tens Ω·cm cannot full fill the requirements with low voltages in those processes. However, a new industrial trend of CMOS process provides high resistivity epitaxial layer of hundreds of Ω·cm, which is possible to be depleted with low voltage. Table 5-1 shows the simulation results of the depletion depth of p-type resistivity epitaxy with different concentrations and voltages from [91].

Table 5-1 Depletion depth of p-type resistivity epitaxy with different voltages.

P-type resistivity	P-type concentration	Depletion layer @0V	Depletion layer @ 1V	Depletion layer @ 2V	Depletion layer @ 3V
100 Ω·cm	1.2e14/cm^3	2.6 µm	4.8 µm	5.2 µm	6.1 µm
500 Ω·cm	2.6e13/cm^3	5.5 µm	9.0 µm	11.5 µm	13.5 µm
1000 Ω·cm	1.3e13/cm^3	7.7 µm	12.6 µm	16.2 µm	19.0 µm

An available process is the XFAB 0.6 µm process that provides an epitaxial layer with high resistivity of 1K Ω·cm and thickness of 14 µm. The depletion zone is simulated by a TCAD tools as compared with a standard epitaxy. Fig. 5-1 shows the results. The depletion zone depth is comparable to the thickness of the high resistivity P-epi. As a result, fast charge collection of 5 ns can be achieved. MAPS chip MIMOSA 25 [92] was fabricated in this process. The pitch size is 20 µm. The charge collection and charge sharing are shown in Fig. 5-2 as comparing with MIMOSA I and MIMOSA 18 chips, which are with standard epitaxy. The collected charges in seed pixel are almost two times of that with standard epitaxy. In the cluster of 3 × 3 pixels, the charge collection efficiency can achieve more than 90 %. A limitation of

this process is that only three metal layers. Thus, the circuit is restricted to conventional 3T-pixels with analog readout and off-chip discrimination. Nevertheless, MIMOSA 25 demonstrates good performance with non-ionizing radiation dose as high as 3×10^{13} n_{eq}/cm^2 in beam tests with 120 GeV pions. The non-ionizing radiation tolerance is improved more than one order of magnitude with respect to similar designs based on standard resistivity processes.

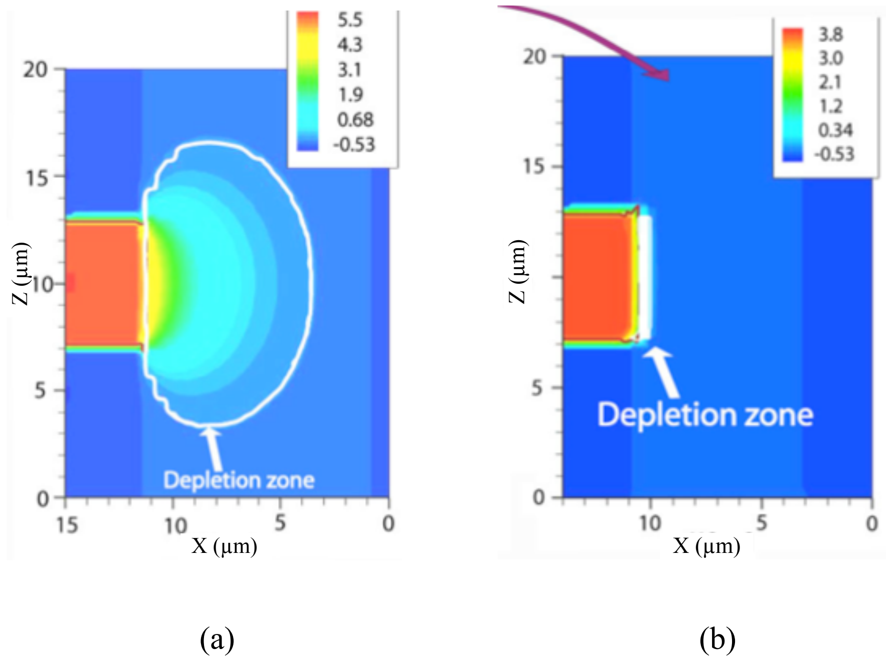


Fig. 5-1. Depletion zone with TCAD simulations. (a) High Resistivity (1K Ωcm) P-epi, (b) Standard resistivity (19Ωcm) P-epi. [91]

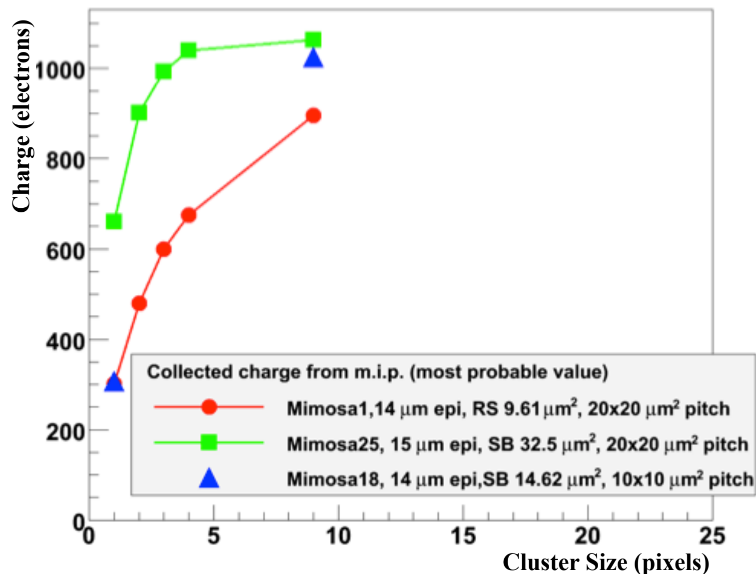
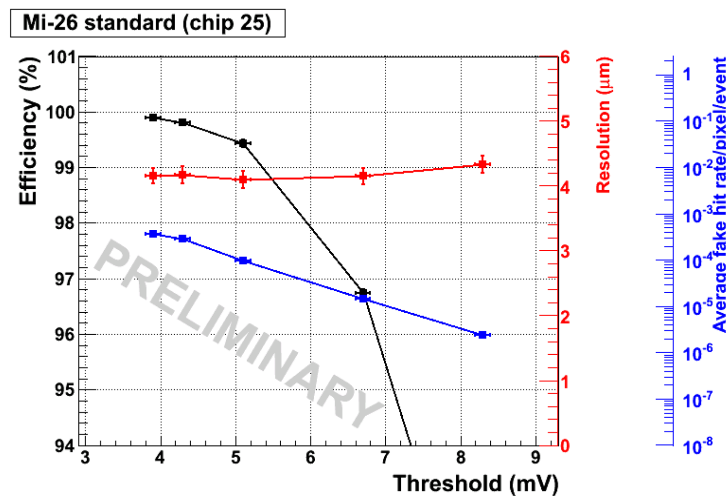


Fig. 5-2. Charge collection from MIP in several chips [91]

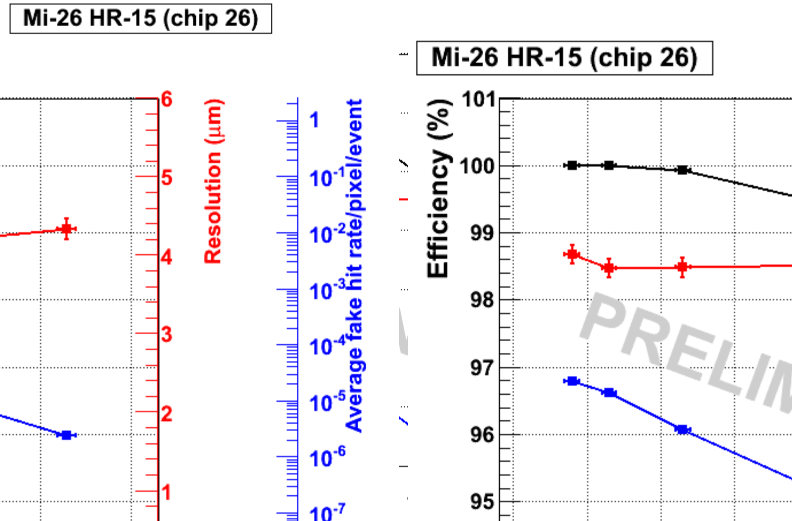
Recently, another available process is AMS 0.35 μm process with an epitaxial layer of 400 Ω·cm. MIMOSA 26 was refabricated in this process with epitaxial layer thickness of 10, 15 and 20 μm respectively. The signal to noise ratio for the seed pixel of clusters are measured by beta particles emitted by a ^{106}Ru source. The results comparing the MIMOSA 26 with a standard epitaxy are shown in Table. 5-2 [91, 93-96]. The high resistivity epitaxy improves the signal to noise ratio for the seed pixel by a factor of two. The HR-15 performs the best signal to noise ratio. The charge collection efficiency shrinks with the increasing thickness of the active volume, since the stretch of the average diffusion paths of the signal electrons increases the probability that charge carriers are lost by recombination. The beam tests are done with 120 GeV/c pion beam of CERN-SPS. The sensors under test were cooled to 15 ^{o}C and 0 ^{o}C for non-irradiated sensors and irradiated sensors respectively in order to reduce the shot noise. All sensors were operated with the digital outputs at their nominal readout time of 115 μs/frame. Fig. 5-3 shows the measured single point resolution, the detection efficiency and the fake hit rate of the sensors. The spatial resolution is about 3.5 to 4 μm for all chips. The standard chip provides a detection efficiency of 99.5% with a fake hit rate of 10^{-4} at a threshold of 5mV. The detection efficiency of HR-15 chip is above 99.9 % with a fake hit rate of 10^{-4} at a threshold of 5.8 mV. The high resistivity chips even keep higher efficiency after an irradiation dose of 1×10^{13} n_{eq}/cm^2 than the low resistivity chips without irradiation.

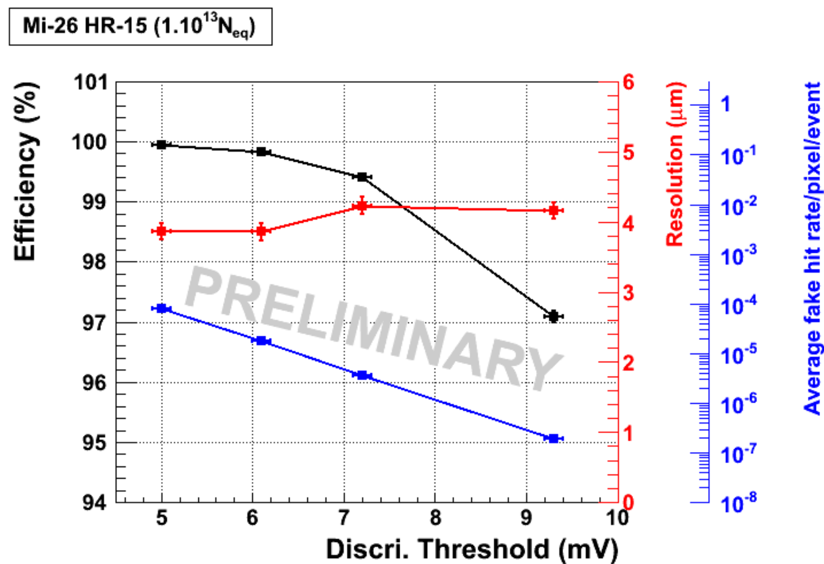
Table 5-2 Signal to noise ratio of MIMOSA 26 with several processes.

Epi type	Epi resistivity/ thickness	SNR
Standard	10 Ω·cm /14 μm	20
HR-15	400 Ω·cm /15 μm	41
HR-10	400 Ω·cm /10 μm	35
HR-20	400 Ω·cm /20 μm	36



(a)





(c)

Fig. 5-3. Beam test results for MIMOSA 26. (a) Standard, (b) HR-15, (c) HR-15 irradiated with 10^{13} n_{eq}/cm^2. [95]

The use of high resistivity epitaxial layers provides potentially high charge collection efficiency due to large depletion region. According to the tests of MIMOSA 26 chips, the sensors with high resistivity epitaxy can achieve a signal to noise ratio of two times of that with low resistivity epitaxy. Thus the high resistivity sensor provides very good performances even after an irradiation of 1×10^{13} n_{eq}/cm^2.

5.2 MAPS using a Small Feature Size Process

Generally, radiation tolerance to TID and SEL can be improved in a smaller feature size process due to a thinner gate oxide and a lower power supply. In addition, low power, high density, and high speed can be achieved due to lower power supply voltage, smaller transistors and more metal layers. For MAPS, proper bias voltage for charge collection should be provided and 0.35 μm process has being mainly adopted in the past. Now, the high resistivity processes provide the possibility to get adequate charge collection efficiency with lower voltage. In IPHC, a fast readout MAPS chip named MIMOSA 32 was designed in a 0.18 μm process. This process provides 14 μm thick epitaxial layer with high resistivity of 1-5 kΩ·cm. In addition, the process provides quadruple wells with deep p-type layer embedding n-well hosting PMOS transistors. Hence, the in-pixel amplifier can be realized by using both PMOS and NMOS transistors. In MIMOSA 32, simple pixel of 20×20 μm^2, deep p-well pixel of 20×20 μm^2, and simple pixel of 20×40 μm^2 were tested. High SNR and high detection efficiency were performed with integration time of 32 μm/frame after ionizing irradiation dose of 1 Mrad and non-ionizing dose of 10^{13} n_{eq}/cm^2. With the validation of the charge collection part and its radiation hardness, in-pixel amplification and in-pixel discrimination will be developed in the future. The complete sensor architecture is expected to be validated in 2016 for ILC vertex detector.

5.3 MAPS with 3D Integrated Technology

5.3.1 Introduction to 3D Integrated Technology (3DIT)

A 3D integrated circuit is generally referred to a chip comprised of two or more layers (tiers) of semiconductor devices that have been thinned, bonded, and interconnected to form a monolithic circuit [97]. Through silicon via (TSV) is one of the key technologies in the manufacture of 3D integrated circuits for the connection of the circuits between different tiers.

The process of 3D integrated technology can be implemented in several different ways due to the order of TSV implementation in the whole process: (1) TSV is made before the CMOS devices, namely “Via First”; (2) TSV is made between CMOS devices and back end of line (BEOL), namely “Via Middle”; (3) TSV is made after BEOL, namely “Via Last”; (4) TSV is made after bonding, namely “Via After Bonding” [98]. Fig. 5-4 illustrates a three-tier chip fabricated by via after bonding. Firstly, individual tiers are fabricated. Secondly, the oxide bonded is used to integrate the two wafers. The oxide bond is a strong bond with two specially prepared smooth silicon oxide surfaces. This bonding technique only provides mechanical bonds, and is used for wafer-to-wafer bonding. For electrical and mechanical connections, copper

thermo compression bonding and copper tin eutectic bonding can be used. Thirdly, 3D TSV is implemented after thinning of wafer 2. TSVs typically have an 8 to 1 aspect ratio. In order to keep the area of via as small as possible, the wafers should be thinned as much as possible. Generally, the wafer can be thinned down to less than 10 µm. In the fourth step, the wafer 3 is bonded with the wafer 1 and 2, and then is thinned and integrated on the wafer 1 and 2 by the TSVs.

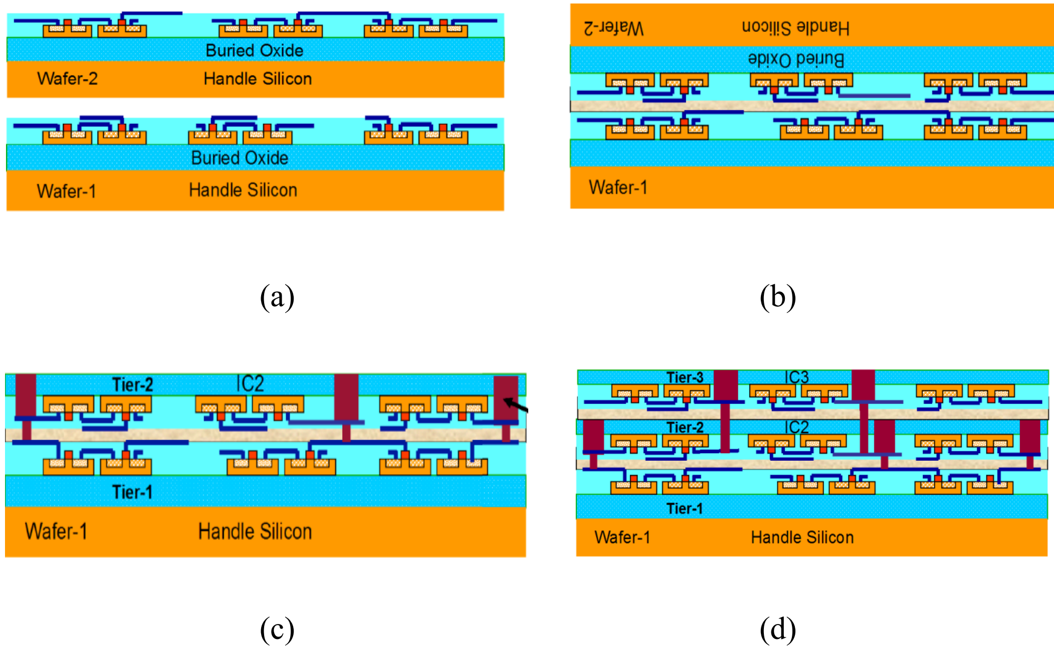


Fig. 5-4. Illustration a three-tier chip fabricated by via after bonding. (a) Fabricate individual tiers, (b) Invert, align, and bond wafer 2 to wafer 1, (c) Remove handle silicon form wafer 2, etch 3D Vias, deposit and CMP tungsten, (d) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D Vias form tier 2 to tier 3. [99]

5.3.2 Advantages of MAPS using 3DIT

Fig. 5-5 shows the architecture of the MAPS using 3DIT (3D MAPS) with 3 tiers as compared to the architecture of 2D MAPS (MAPS with traditional technology). The basic functional modules and the work principles are the same. The particle-induced charge is collected and converted to voltage signal by the sensing element, and then the voltage signal is amplified and shaped, discriminated and processed for output. However, the 3D integrated technology provides new possibilities of circuit and process optimization for MAPS. The 3D MAPS are prone to achieve high spatial resolution, high readout speed, high radiation tolerance and low power consumption.

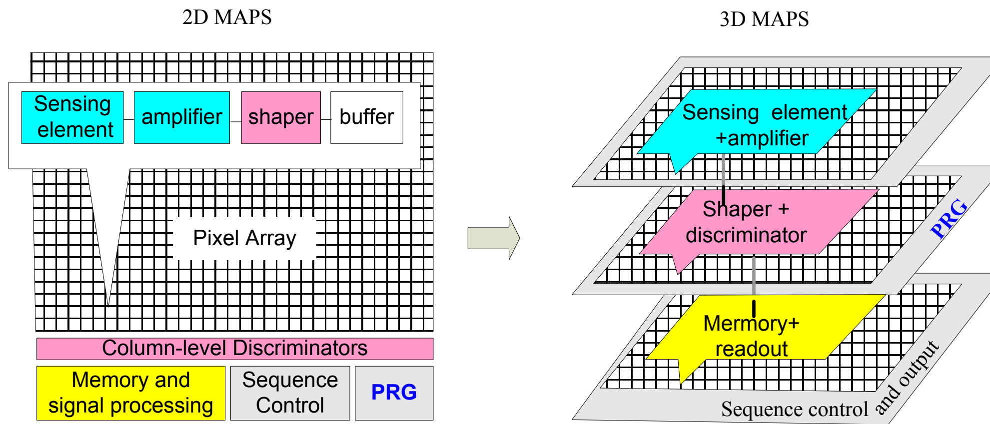


Fig. 5-5. An architecture of 3D MAPS with 3 tiers conversion from an architecture of 2D MAPS

On one hand, the sensing elements, analog processing circuits and digital processing circuits can be realized in several layers with different manufacture processes in 3D MAPS chip. As a result, the charge collection efficiency and the non-ionizing radiation tolerance of the MAPS chip can be improved by using the high resistivity process for the sensing element [100]. This high resistivity process is limited to be used in 2D MAPS since only three metal layers are available. Moreover, the PMOS transistors can be used easily on the tiers not including sensing element, while only NMOS transistors can be used in pixel design in order to achieve 100% fill factor with the N-Well/P-Substrate sensing diode in 2D MAPS [100]. Consequently, the possibilities of circuit topologies and functions are numerous. Thirdly, the small feature size process such as 0.13 µm process is prone to be used in 3D MAPS for the analogue and digital processing since the resolution, speed, power consumption, and radiation tolerance generally benefit from small feature size process. In 2D MAPS, proper bias voltage for charge collection should be provided and 0.35 µm process has being mainly adopted in the past.

On the other hand, owing to the vertical integration, the discriminator and digital processing can be realized in pixel level. Consequently, the readout of pixel array can be parallel processed and the interconnections between the modules are shortened. Fast 3D MAPS with pipelined digital readout have been proposed to improve spatial resolution and time resolution and to minimize power consumption [101, 102].

5.3.3 MAPS using 3DIT

Several MAPS chips with 3D integrated technology (3D MAPS) have been developed and show predicted benefits [103-105]. Fig. 5-6 shows the block diagram of a proposed architecture for 3D MAPS. The readout circuits are divided into three stages implemented in three tiers respectively. The sensing diode and pre-amplifier are the first stage. The second stage is for the charge integration, time invariant

shaping and signal discrimination. In the third stage, the signal is latched and readout. XFAB 0.6 μm PIN process is used for the Tier_0, and the Tier_1 and Tier_2 employ a Chartered 0.13 μm process. During this design, the three tiers are fabricated separately firstly. Then, the Tier_1 and Tier 2 are bonded by Chartered (wafer-to-wafer bonding). Tier_0 is bonded with the bonded Tier_1 and Tier_2 by a third company (Ziptronix) as a post-processing (chip-to-wafer bonding).

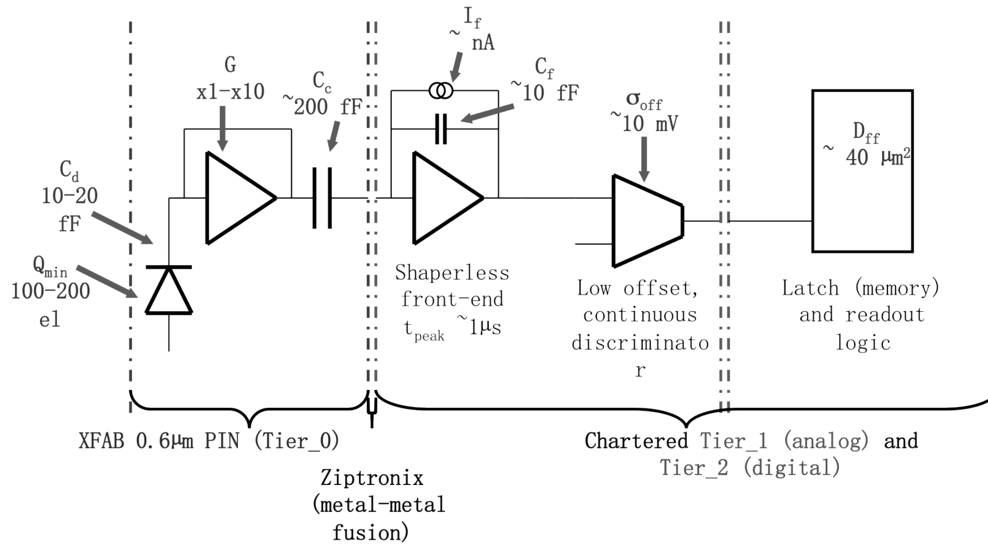


Fig. 5-6. Block diagram of a proposed architecture using 3DIT.[103]

In the first stage, PIN diode is used as sensing element. Pixel pith is 20μm. Due to the high resistivity epitaxy, the sensing volume almost can be depleted. Thus, a fast charge collection can be achieved. The radiation tolerance of as high as 3×10^{13} n_{eq}/cm^2 has been verified in MIMOSA 25. The signal noise ratio defined by the first stage will be rather good since the gain of charge amplification can achieve 100 μV/e, owning to the parasitic capacitor coupling to the second stage (200 fF).

In the second stage, a “shapeless front-end” (SFE) structures [106, 107] and low offset continuous discriminator are chosen. This structure is simple and efficient for the minimum signal charge is of few thousand electrons, which is after the charge amplification. The shaping time is of 1 μs. This time resolution is enough and insensitivity to the irradiation induced leakage current. For the minimum signal at the input of the discriminator of ~ 150 mV, the offset of few mV is acceptable. The expected equivalent noise charge is less than 15 electrons for a pulse peaking time of about 500 ns. The voltage gain at the discriminator input is 150 μV/e, and the total analog power dissipation of ~ 5W/pixel. In the connection with the first stage, signal to noise ratio of more than 40 are obtained for minimum ionizing particles.

In the third stage, digital readout with a fast, data driven, self-triggering data flow is implemented. The idea is to read the X and Y projection of a hit pattern in less than 2 μs, following a trigger signal set by the first hit pixel. [103]

Another structure based on rolling shutter mode with fast digital pipelined

readout is proposed to improve spatial resolution and time resolution and to minimize power consumption. The readout time is expected to be in range of single μs.

In 3D chips, the radiation tolerance can get benefits from both the process optimization and high readout speed. Since the fabrication processes of 3DIT are complex and challengeable, the 3D chips are still being fabricated. In one word, the 3D design may pave a way for the construction of high precision vertex detector, approaching requirements of hadron colliders in term of speed and radiation hardness.

5.4 Conclusion

This chapter introduces several MAPS chips with new available processes including a process of high resistivity epitaxial layer, a process of 0.18 μm feature size and the process of 3D integrated circuits. The MAPS chip with high resistivity process has demonstrated high detection performance and high radiation tolerance of more than 3×10^{13} n_{eq}/cm^2. The MAPS chips based on 3D integrated process and the 0.18μm process are prospected higher performances on radiation tolerance, speed and power consumption.

6 Conclusion and Perspectives

In high energy physics experiments, charged particle tracking helps to give the information of the invisible phenomena during the experiment. Monolithic active pixel sensors is prospected for charged particle detection due to the high spatial resolution, low material budget, potential radiation tolerance, and fast readout speed. A recent application of MAPS is to construct PIXLE detector in the upgrade of STAR vertex detector. Since the MAPS are close to interaction point, a very high spatial resolution (1-2 μm) and high radiation tolerance (total ionizing radiation dose of 300 krad/year and non-ionizing radiation influence of 10^{13} n_{eq}/cm^2) are required. In future high energy experiments such as ILC, CBM and so on, the MAPS must keep high performances under an even harsher radiation environment.

In high energy experiments, the yield particles such as protons, electrons, neutrons, muons, neutrinos, photons and small amount of alpha particles may hit and interact with the sensor material. Both of ionizing radiation and non-ionizing radiation should be considered. The non-ionizing radiation induced atom displacements rarely affect the conductor and dielectric but may reduce the lifetime of minority carrier in semiconductor. The ionizing radiation yields electron hole pairs in materials, thus single event effects and total ionizing effects are induced in semiconductor and dielectric respectively. In MAPS, the MOS transistors are venerable to the single event effects and total ionizing effects; and the charge sensing diode are sensitive to the reduction of minority carrier lifetime and the leakage currents results from the total ionizing effects.

In the past few years, the non-ionizing radiation effects and TID effects have been studied with carefully selected proton, neutron and soft X-ray irradiation. In addition, the performances such as detection efficiency and Signal to Noise Ratio (SNR) were measured in real beam experiments. The test results demonstrate that the non-ionizing effects mainly lead to the decrease of the charge collection efficiency and the ionizing effects result in a noise increase. Both effects reduce the SNR and the particle detection efficiency. By selecting a proper epitaxial layer thickness and optimizing the diode density, the MAPS have achieved a detection efficiency of 99.5% under a non-ionizing radiation dose up to 2×10^{12} n_{eq}/cm^2 (resp.10^{13} n_{eq}/cm^2) at an operating temperature of +30ºC (resp. 0ºC). The TID effects in MAPS have been alleviated by radiation-hardening layout techniques and a self-biased pixel design. In addition, some test results indicate that the TID tolerance can be improved by reducing the integration time of the MAPS, which equals to the readout time in most designs of MAPS. The TID tolerance may nearly reach 1 Mrad with an integration time of 200 μs and 10 Mrad with an integration time of 10 μs. Therefore, fast readout MAPS are required for improving their TID tolerance.

With the requirements of high readout speed and high radiation tolerance, fast readout MAPS are conceived by integrating a data compression block and two SRAM IP cores. However, the radiation tolerance of the two SRAM IP cores is not as high as

for the other parts in MAPS and mitigates the radiation tolerance of the whole MAPS chip. Especially, the SRAM is sensitive to the SEE effects including SEU effects. Therefore, three radiation hard memories are designed for the present and future MAPS chips. Firstly, a radiation hard SRAM prototype is realized and verified in a 0.35 μm process according to the requirements of STAR experiments. The tolerance to the SEU and TID effects is comparable to and even better than the tolerance of the other circuits in the MAPS. The tolerance to the SEL effect is above 56 MeV·cm^2/mg as compared to 5.2 MeV·cm^2/mg before the improvement. Secondly, a prototype of radiation hard SRAM with EDAC algorithm and bit-interleaving storage is proposed and designed for higher SEU mitigation when the fabrication process is migrated to 0.18 μm process. Thirdly, a dual-port memory with an original 2T-cell is proposed and evaluated for future high energy physical experiments. The memory is predicated to be almost free from SEL effect and be very high immune from TID effects.

In the development of the particle detectors, the requirement of high performance sensors has no end. The higher performance, the more clearly we know form the experiments. The possibility of new processes promotes the MAPS designs and performances. Firstly, high-resistivity epitaxial layer processes are preferred for MAPS. The high resistivity of the layer allows for nearly full depletion, resulting in high charge collection efficiency. Because of the drift field associated to the depletion, the effect of the traps due to non-ionizing damage is alleviated resulting in an improved radiation tolerance. In the irradiation test, the non-ionizing radiation tolerance has reached above 3×10^{13} n_{eq}/cm^2 for the MAPS based on an epitaxial layer resistivity exceeding 1 kΩ·cm. Secondly, a 0.18 μm process with deep P-well and high resistivity epitaxial layer is available. The tolerance to TID and SEL effects is improved due to the thinner gate oxide and lower power supply voltage. The SEU effects can be alleviated by the radiation hard SRAM with the EDAC algorithm. Nowadays, three-dimensional (3D) integrated technologies, integrating two or more layers (tiers) of semiconductor devices in a chip by thinning, bonding, and interconnecting, provide more possibilities of circuit design and process optimization for MAPS. The MAPS using the 3D integrated technology (3DIT) are prone to achieve high spatial resolution, high readout speed, high radiation tolerance and low power consumption. In the 3D chips, the radiation tolerance can benefit from both the process optimization and high readout speed.

In the future, some efforts still should be put on the radiation hard MAPS design from the following aspects.

Firstly, the SEE assessment of the SRAM developed in this thesis still refers to a low resistivity epitaxial layer. A similar assessment remains to be done in case of a high resistivity layer. On one hand, some test circuits will be designed and tested under irradiation. On the other hand, device simulations will be constructed for analyzing the physical principle combined with the experimental results.

Secondly, advanced architecture of fast readout MAPS according to the new available processes can be developed for improving the detection efficiency and for minimizing the sensitive components such as memory capabilities, which are probably much efficiency for the improvement of the radiation tolerance in the future.

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Biography

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