# Nanoscale characterization of leakage currents in ultra-thin oxide layers for microelectronics

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THÈSE

# Caractérisation des courants de fuite à l'échelle nanométrique dans les couches ultra-minces d'oxydes pour la microélectronique

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# Résumé

La miniaturisation de la structure de transistor MOS a conduit à l'amincissement de l'oxyde de grille. Ainsi, la dégradation et le claquage sous contrainte électrique est devenu l'un des problèmes de fiabilité les plus importants des couches minces d'oxydes. L'utilisation de techniques de caractérisation permettant de mesurer les courants de fuite avec une résolution spatiale nanométrique a montré que le phénomène de claquage des oxydes est un phénomène très localisé [1]. Le diamètre des «points chauds», des endroits où le courant de fuite est très élevé pour une tension appliquée continue, peut-être de quelques nanomètres uniquement [2]. Ceci illustre pourquoi les méthodes de caractérisation avec une résolution spatiale à l'échelle nanométrique peuvent fournir des informations supplémentaires par rapport à la caractérisation classique macroscopique. Il y a deux instruments, dérivés de la microscopie à force atomique (AFM) qui peuvent être utilisés pour faire ce travail, soit le Tunneling Atomic Force Microscope (TUNA) ou le Conductive Atomic Force Microscope (C-AFM). Figure 1 montre le principe de l'AFM en mode TUNA qui est utilisé dans notre travail et qui est capable de mesurer des courants très faibles variant entre 60 fA et 100 pA. Il s'agit d'un Veeco Dimension 3100 qui utilise l'électronique Nanoscope V.

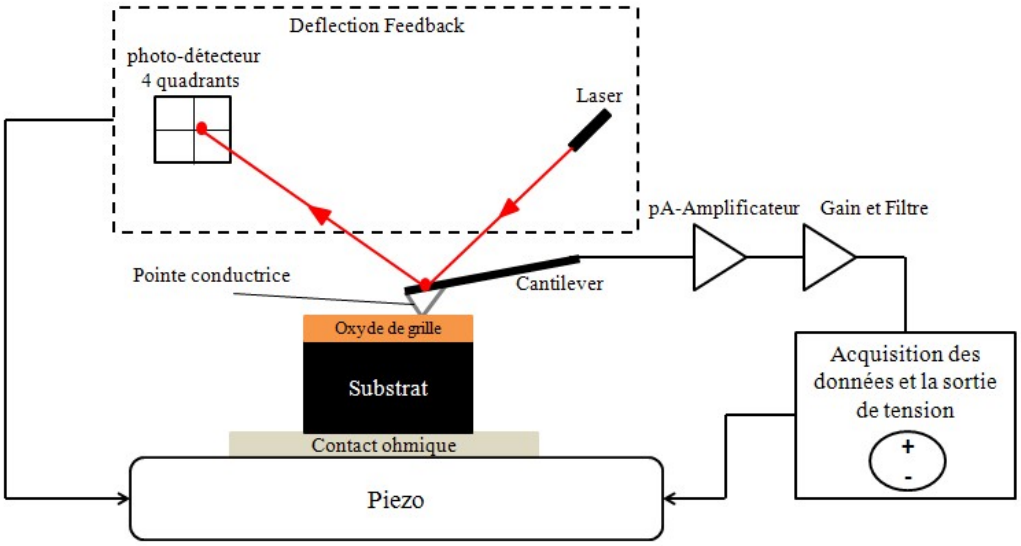


*Figure 1: Le principe de l'AFM en mode TUNA.*

Avant de commencer les mesures électriques à l'échelle nanométrique en utilisant le mode TUNA, il est important de montrer que ces mesures qui sont faites avec des pointes AFM couvertes par une couche conductrice de $PtIr_5$ sont fiables. Afin de le vérifier, des comparaisons ont été faites entre des mesures effectuées à l'échelle macro-métrique (à l'aide

d'Agilent 4156B) et à l'échelle nanométrique (en utilisant Nanoscope V connecté au mode TUNA-Veeco AFM) sur des électrodes de Ti/Au de taille 11 x 11 $\mu m^2$ déposées par lithographie électronique sur 3,5 nm de $SiO_2$ thermique sur un substrat Si de type-p ($10^{15}$ $at.cm^{-3}$).

Figure 2 (à gauche) montre les caractéristiques représentatives I-V obtenues à l'échelle macro et nanométrique. Ces caractéristiques représentent la moyenne de plusieurs mesures effectuées sur des électrodes différentes de la même dimension afin de montrer la reproductibilité des mesures. Des rampes de tension négative ont été appliquées sur le substrat de 0 à -3 V avec une vitesse de 0,5 V/sec. En conséquence, les deux caractéristiques I-V obtenues par les deux méthodes différentes sont ainsi superposées indiquant la bonne fiabilité des mesures électriques du mode TUNA de l'AFM.

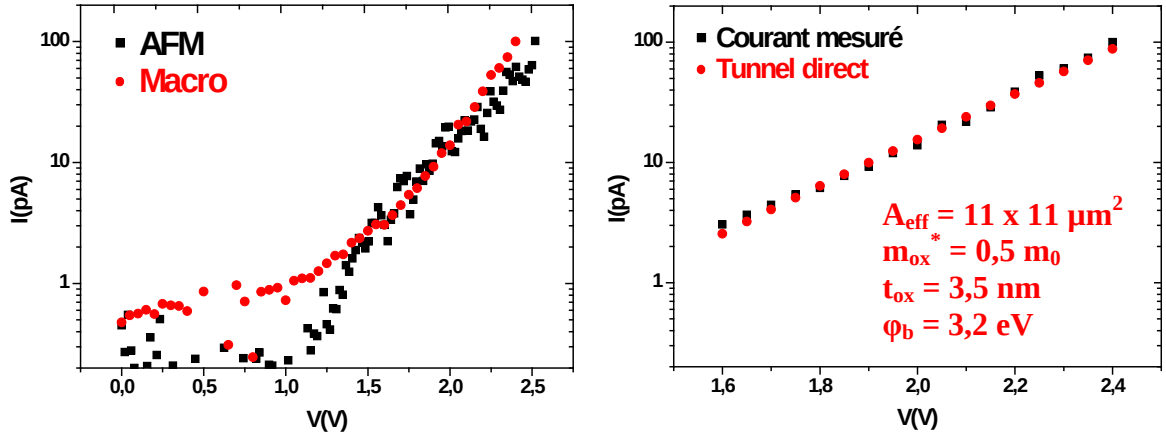


*Figure 2: Caractéristiques I-V à l'échelle macro et nanométrique (à gauche) sur des électrodes de taille 11x11 $\mu m^2$ déposées sur 3,5 nm de $SiO_2$ thermique et la modélisation de ces caractéristiques par un tunnel direct (à droite).*

D'autre part, pour étudier la correspondance de ces caractéristiques du courant tunnel à travers un film d'oxyde mince et pour des tensions inférieures à 3,2 V (correspondant à la hauteur de barrière de $SiO_2$), le tunnel direct a montré un ajustement parfait à ces caractéristiques comme indiqué dans le graphique de la Figure 2 (à droite). Le tunnel direct par les oxydes peut être exprimé par la formule suivante [3]:

$$\mathbf{I_{direct} = A_{eff}\ \frac{q^2}{8\,\pi\,h\,\Phi_b}\ \frac{m_0}{m_{ox}^*}\ \left(\frac{V_{ox}}{t_{ox}}\right)^2\ e^{\left[\frac{-8\,\pi\sqrt{q}}{3\,h}\sqrt{2\,m_{ox}^*}\left(\Phi_b^{\frac{3}{2}}-(\Phi_b-V_{ox})^{\frac{3}{2}}\right)\frac{t_{ox}}{V_{ox}}\right]}} \qquad \mathbf{(1)}$$

où $A_{eff}$ = 11x11 $\mu m^2$ est la surface effective du contact, q est la charge de l'électron, et h est la constante de Planck. Dans une première approximation nous avons considéré $m_{ox}^*/m_0$ = 0,5 est la masse effective de l'électron dans la bande de conduction de $SiO_2$, $t_{ox}$ = 3,5 nm est l'épaisseur physique de l'oxyde, $\Phi_b$ = 3,2 eV est la hauteur de barrière du $SiO_2$ [4] et $V_{ox}$ la différence de potentiel de l'oxyde, qui est donné par:

$$V_{ox} = V_G - \Phi_{MS} - \Psi_S \quad (2)$$

avec $V_G$ la tension de grille, c.à.d. la tension appliquée sur la pointe AFM, $\Phi_{MS} \approx -0{,}15$ eV est la différence du travail de sortie entre la pointe AFM qui est couverte par le métal $PtIr_5$ (travail de sortie ≈ 4,7 eV) et le substrat Si dopé p (≈ $10^{15}$ at.cm$^{-3}$) et $\Psi_S$ est la potentiel de surface du substrat qui est dans notre cas dans son régime d'inversion puisque la tension appliquée $V_G$ est positive sur la pointe et largement supérieure à $\Phi_{MS}$.

Pour presque toutes les mesures du courant à l'échelle nanométrique que nous avons fait, nous avons utilisé les pointes AFM couvertes par $PtIr_5$ en raison de leur stabilité mécanique et électrique élevée [5]. Un des paramètres essentiels inconnus des caractéristiques I-V effectuées à l'échelle nanométrique est la surface effective du contact entre la pointe et l'échantillon. Cette surface du contact dépend de différentes variables telles que la force appliquée par la pointe sur l'échantillon, les conditions de l'atmosphère et l'apex de la pointe. Pour cette raison et afin d'éviter les fluctuations de nos mesures, nous avons utilisé la même valeur de la déflexion de consigne (0,5 V) afin d'avoir approximativement la même surface de contact pour toutes les mesures en utilisant le même type des pointes AFM.

Figure 3 montre la caractéristique I-V pour un échantillon de 3,5 nm $SiO_2$: $I_m$ en pA, et la densité du courant de type tunnel Fowler-Nordheim correspondant: $J_{FN}$ en pA/µm$^2$.

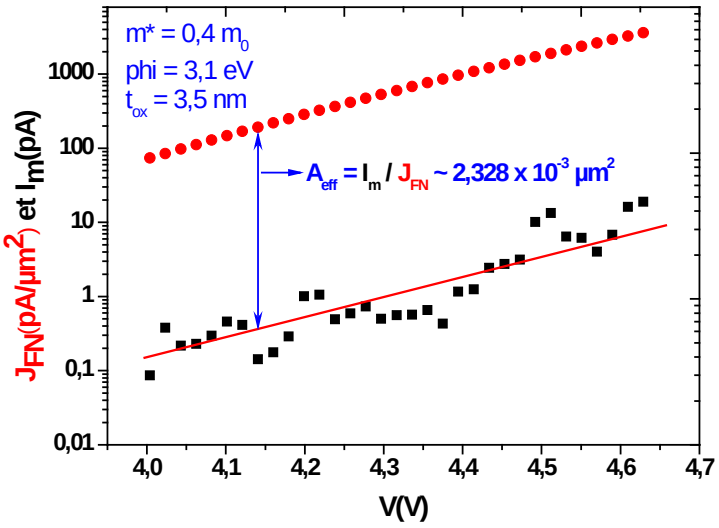


*Figure 3: Caractéristique I-V mesurée et la densité du courant type FN avec les paramètres de l'ajustement pour le 3,5 nm $SiO_2$ en utilisant une pointe AFM couverte par $PtIr_5$.*

La formule du tunnel FN utilisée est:

$$I_{FN} = A_{eff} \frac{q^2}{8\,\pi\,h\,\Phi_b} \frac{m_0}{m_{ox}^*} \left(\frac{V_{ox}}{t_{ox}}\right)^2 e^{\left[\frac{-8\,\pi\sqrt{q}}{3\,h}\sqrt{2\,m_{ox}^*}\,\Phi_b^{\frac{3}{2}}\frac{t_{ox}}{V_{ox}}\right]} = A_{eff}\,J_{FN} \quad (3)$$

Dans une première approximation les valeurs suivantes des paramètres ont été considérées:

$\Phi_b$ = 3,1 eV, $m_{ox}^*/m_0$ = 0,4, et $t_{ox}$ = 3,5 nm. Ainsi, en calculant le rapport du courant mesuré $I_m$ sur la densité de courant de type FN $J_{FN}$, une valeur approximative de la surface du contact peut être déterminé, qui se trouve être dans notre cas ~ 2328 $nm^2$. Si on considère une surface de contact circulaire, nous pouvons déterminer le rayon de la pointe ~ 26 nm. Il est important de rappeler que cette expérience a été faite à l'air. Donc, cette valeur déterminée par nous peut être affectée par l'existence d'un ménisque d'eau entre la pointe et la surface qui conduit à une surface du contact plus grande lorsque les expériences sont faites à l'air.

La silice $SiO_2$ qui est utilisé dans les structures MOS possède les propriétés électriques suivantes: la constante diélectrique $\varepsilon \approx 3.9$, énergie du band gap $E_g \approx 9$ eV. Le $SiO_2$ a atteint ses limites physiques pour des épaisseurs de l'ordre de 1,5 nm, car pour ces épaisseurs, le courant de fuite devenu très élevé et important en provoquant le dysfonctionnement des appareils électroniques. Néanmoins, ces épaisseurs sont essentielles pour obéir aux lois de la miniaturisation et d'avoir des systèmes de haute performance. Un grand nombre d'études ont été réalisées afin de développer des oxydes avec une constante diélectrique forte (appelés oxydes high-k) [6][7]. Ces matériaux possèdent des constantes diélectriques plus élevées que celui du $SiO_2$ et qu'ils sont capables de remplacer l'oxyde de silicium dans les structures MOS [8][9].

Cette thèse abordera la caractérisation électrique à l'échelle nanométrique de deux oxydes high-k: le $LaAlO_3$ (LAO) amorphe et le $Gd_2O_3$ (GdO) amorphe élaborés par MBE (Molecular Beam Epitaxy) à l'INL et qui représentent des bons candidats pour remplacer le $SiO_2$. Donc, des couches minces de LAO et GdO déposées par MBE en utilisant des protocoles différents ont été étudiées à l'échelle nanométrique en utilisant le mode TUNA. Ce mode nous permet de voir les points chauds présents dans ce type d'oxyde en évitant le problème de court-circuit qui peut avoir lieu entre des électrodes macroscopiques et le substrat Si lors de la caractérisation des oxydes ayant une grande densité de points chauds.

L'objectif de cette étude est d'étudier à l'échelle nanométrique l'influence de l'atmosphère pendant le dépôt (oxygène moléculaire ou atomique) sur les propriétés électriques du LAO et du GdO. Nous avons montré que le dépôt de ces oxydes high-k dans une atmosphère d'oxygène atomique améliore leurs propriétés électriques par rapport à l'atmosphère de l'oxygène moléculaire. Ce résultat peut être représenté par deux façons en utilisant le mode TUNA: soit par des images du courant soit par des caractéristiques I-V.

Figure 4 montre les images du courant (1 x 1 $\mu m^2$) de chaque échantillon du LAO ayant la même épaisseur physique de 3,2 ± 0,3 nm (mesurée par X-Ray Reflectometry (XRR)). Pour l'échantillon A le LAO a été déposé dans une atmosphère d'oxygène moléculaire et pour l'échantillon B le LAO a été déposé dans une atmosphère d'oxygène atomique. Nous avons augmenté progressivement la valeur de la tension appliquée continue

jusqu'en zones sombres sont apparues sur les images pour atteindre la valeur de -5,8 V sur l'échantillon A, avec une échelle du courant [-10 pA (foncé), 5 pA (brillant)] et -7,2 V sur B avec une échelle du courant [-9 pA (foncé), 1 pA (lumineux)]. Nous avons appliqué des tensions négatives sur le substrat pour éviter l'oxydation anodique des pointes AFM. Sur les images du courant, des zones plus foncées correspondent à des points chauds où le courant de fuite est élevé.

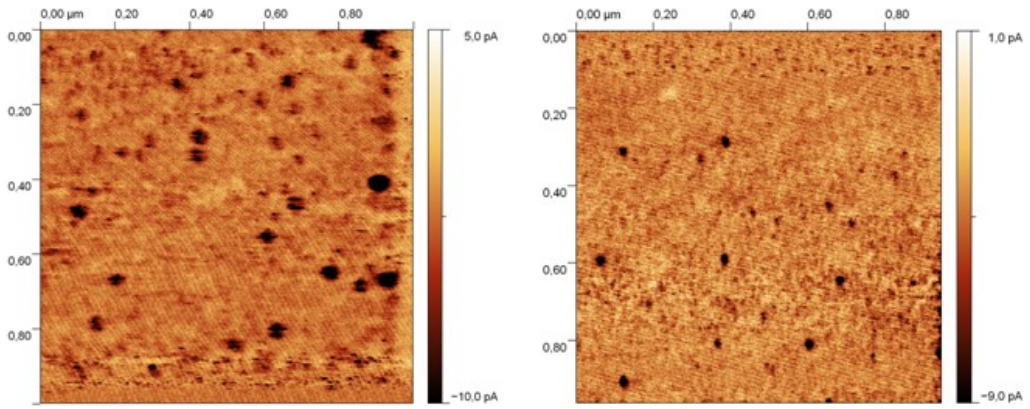


*Figure 4: Les images du courant (1 x 1 µm$^2$) de l'échantillon A (à gauche, $V_{app}$ = -5,8 V) et B (à droite, $V_{app}$ = -7,2 V) du LAO.*

Nous remarquons que l'échantillon A a plus des zones conductrices que B, même pour une tension appliquée plus faible. Considérant plusieurs images du courant différentes, la densité des points chauds peut être estimée: elle est ≈ 20 x $10^8$ par cm$^2$ pour l'échantillon A et ≈ 12 x $10^8$ par cm$^2$ pour l'échantillon B démontrant les meilleures propriétés diélectriques pour le dernier échantillon où le LAO a été déposé dans une atmosphère d'oxygène atomique. Ce résultat est une bonne indication sur l'influence positive de l'oxygène atomique sur le comportement électrique de LAO.

Pour confirmer ce résultat, nous avons fait à l'échelle nanométrique 16 mesures I-V sur 16 zones différentes de chaque échantillon pour calculer la valeur moyenne de la tension de seuil $V_{th}$ correspondante à la tension pour laquelle le courant traversant l'oxyde atteint 1 pA. Les caractéristiques I-V représentatives pour les deux échantillons sont présentées à la Figure 5. Nous avons appliqué sur chacune des 16 zones une rampe de 0 à -10 V avec une vitesse de 0,5 V/s et une limite du courant de -80 pA (pour éviter le claquage de l'oxyde). Toutes les valeurs du courant et de la tension sont présentées en valeur absolue.

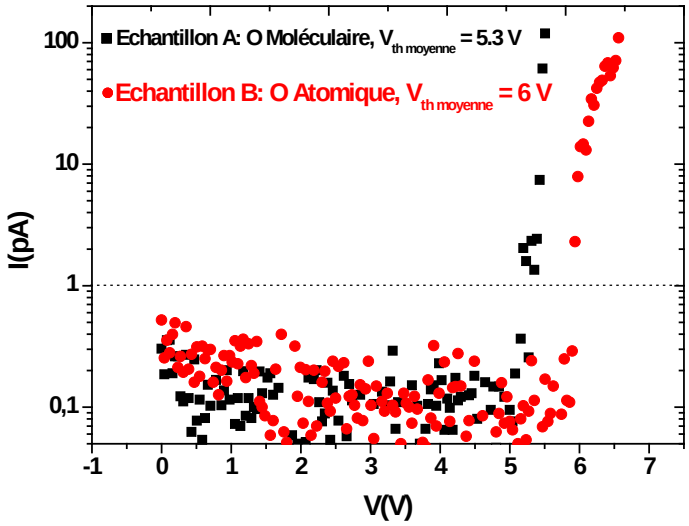


*Figure 5: Les caractéristiques I-V représentatives de l'échantillon A et B.*

Selon les caractéristiques I-V, les valeurs moyennes de $V_{th}$ sont 5,3 V et 6 V pour l'échantillon A et B respectivement, avec une incertitude de 0,3 V. Considérant le fait que l'épaisseur de deux échantillons est presque la même (~ 3,2 nm), nous attribuons cette différence à l'atmosphère du dépôt qui est l'oxygène atomique pour l'échantillon B et l'oxygène moléculaire pour l'échantillon A.

Mêmes résultats ont été déterminés pour le GdO où l'échantillon qui a été déposé dans une atmosphère d'oxygène atomique a montré de meilleures caractéristiques électriques par rapport à celui où GdO a été déposé dans une atmosphère d'oxygène moléculaire.

Nous pouvons rapporter l'existence d'un courant de fuite à travers les films de LAO et de GdO dû aux lacunes d'oxygène dans le volume de ces oxydes [10]. Cependant, la diminution de la densité des points chauds dans les échantillons ayant le LAO et le GdO déposés dans une atmosphère d'oxygène atomique pourrait être expliquée par le remplissage des lacunes d'oxygène présentées dans les deux oxydes par les atomes d'oxygène.

Par ailleurs, l'influence des procédures de préparation du substrat sur les caractéristiques électriques du LAO a été explorée. Les deux procédures utilisées sont: une technique de haute température pour préparer le substrat (High-T) et un nettoyage chimique de la surface du substrat à l'aide de l'acide fluorhydrique (HF-last). Les caractéristiques I-V ont montré de meilleures caractéristiques électriques pour l'échantillon dont la procédure de la préparation du substrat avant le dépôt de LAO était le nettoyage chimique. Ceci peut être expliqué par le fait que l'étape de recuit à 900 °C de la procédure High-T conduit à une réaction entre le substrat de Si et la contamination résiduelle de carbone initialement présent sur le substrat formant des trous et des bosses de SiC sur le substrat. La formation de SiC empêche localement la croissance de LAO, conduisant à une dégradation de la morphologie de LAO pour l'échantillon de High-T comme les images topographiques l'ont montré. D'autre part, pour l'échantillon HF-last, en raison de la procédure à basse température, ni de trous ni

de points de SiC ont été formés dans la couche finale de LAO conduisant à une meilleure performance électrique de l'oxyde.

Concernant le GdO, une étude de l'influence de la température de dépôt sur les caractéristiques électriques de GdO est présentée, où nous avons réalisé des mesures I-V à l'échelle nanométrique sur des films déposés entre 650 et 720 °C. Caractéristiques I-V de quatre échantillons avec des températures de dépôt différentes (650, 680, 700, 720 °C) sont présentées à la Figure 6.

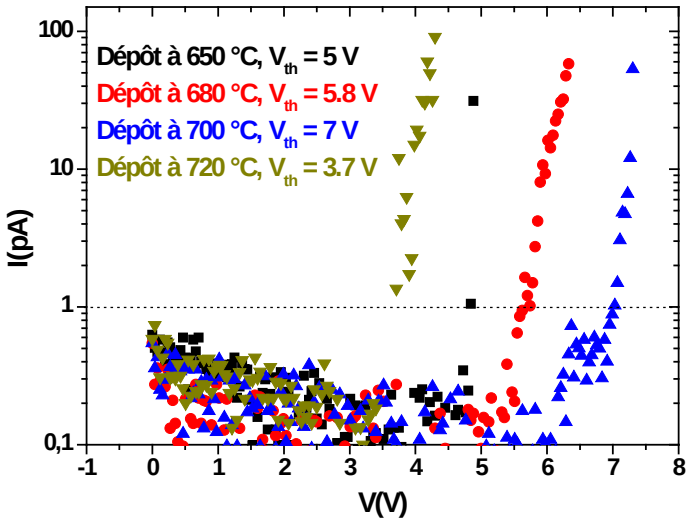


*Figure 6: Les caractéristiques I-V représentatives des films de GdO déposés à des températures différentes.*

Les valeurs moyennes de $V_{th}$ sont 5 V, 5,8 V, 7 V et 3,7 V pour les échantillons élaborés à 650 °C, 680 °C, 700 °C et 720 °C, respectivement avec une incertitude de 0,3 V. Considérant le fait que tous les échantillons ont la même épaisseur (~ 5,5 nm), nous attribuent cette différence à la température de croissance de GdO où nous pouvons remarquer que quand la température du dépôt augmente de 650 °C à 700 °C $V_{th}$ augmente et à 720 °C elle diminue indiquant que le GdO commence à cristalliser à cette température. De plus, comme les mesures qui sont faites à l'échelle macro-métrique, les caractéristiques I-V à l'échelle nanométrique montrent que la température optimale de croissance de GdO est de 700 °C puisque elle montre la tension de seuil le plus élevé de 7 V.

L’application d'une tension positive sur le substrat et négative sur la pointe AFM mène à l'oxydation du silicium à l'interface $Si/SiO_2$ [11][12][13] conduisant à l'inflation normale de la surface de l'oxyde (création d'une bosse). Cette oxydation a lieu à cause de l'existence d'une couche d'eau sur la surface de l'oxyde dans l'air ambiant. L'application d'une tension négative sur la pointe AFM mène à l'injection d'ions $HO^-$ à travers l'oxyde résultant de l'oxydation de Si à l'interface $Si/SiO_2$.

Dans le cas contraire, l'application d'une tension de polarité inversée, c.à.d. négative sur le substrat et positive sur la pointe de l'AFM n’oxyde pas normalement le silicium à l'interface. Toutefois, des bosses anormales (hillocks) ont été observées à la surface de l'oxyde après cette procédure comme illustré à la Figure 7.

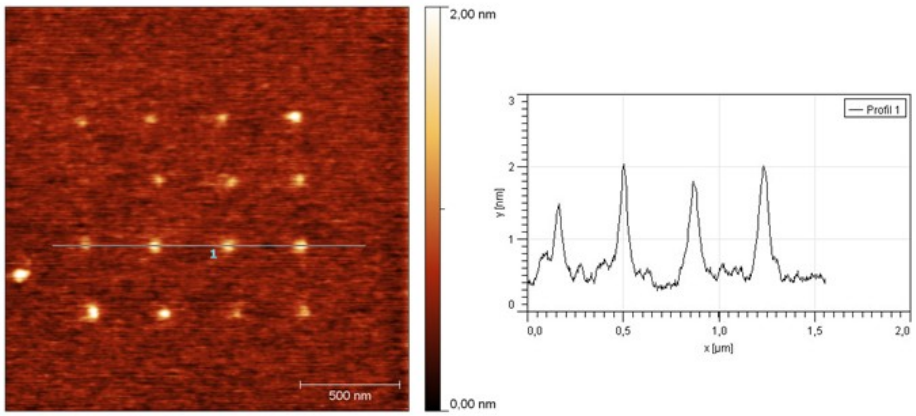


*Figure 7: Topographie affichant 16 bosses anormales créées après l'application d'une tension négative sur le substrat et positive sur la pointe de l'AFM sur 16 endroits différents de l'oxyde. Image de droite montre les profils des bosses créées.*

Nous avons effectué plusieurs études sur ces bosses anormales en utilisant des modes différents de l’AFM (contact et contact intermittent) et en utilisant des différents types de pointes AFM (conductrice et non-conductrice) pour savoir leur nature physique. Nous avons démontré que l'existence de la bosse sur la surface de l'oxyde après l'application d'une tension électrique est une combinaison de deux phénomènes: la modification morphologique réelle de la surface de l'oxyde et la force électrostatique entre les charges piégées à l'intérieur de l'oxyde et la pointe AFM.

Par ailleurs, nous avons étudié l'influence des différents paramètres sur la hauteur de la bosse. A l'air, nous avons montré que la bosse existe toujours avec presque la même hauteur indépendamment du temps de stress et que la quantité de charges augmente lorsque la limite du courant augmente en particulier après la $1^{ère}$ rampe de tension qui forme un chemin de défauts à l'intérieur de l'oxyde aidant le passage des charges. D'autre part, dans l'air sec la bosse n'est pas créée pour un temps de stress court. Ainsi, nous avons proposé deux

phénomènes physiques expliquent la création de la bosse selon le nombre de rampes de tension appliquées et les images du courant obtenues par AFM en mode TUNA: l'effet électrothermique et l'oxydation du silicium à l'interface $Si/SiO_2$.

Nous avons étudié l'influence de l'existence de la couche d'eau sur la surface de l'oxyde $SiO_2$ au cours de l'application d'une tension électrique. Nous avons démontré que le courant est plus élevé sous vide pour la première caractéristique I-V alors qu'il est beaucoup plus élevée à l'air pour la deuxième caractéristique I-V indiquant une dégradation plus importante de la couche d'oxyde à l'air (Figure 8). Cela confirme l'hypothèse de l'effet tunnel assisté par des défauts électriquement actifs liés à l'hydrogène provenant de la dissociation par le champ électrique élevé de la couche d'eau sur la surface de l'oxyde quand les expériences sont menées à l'air ou sous vide sans chauffage.

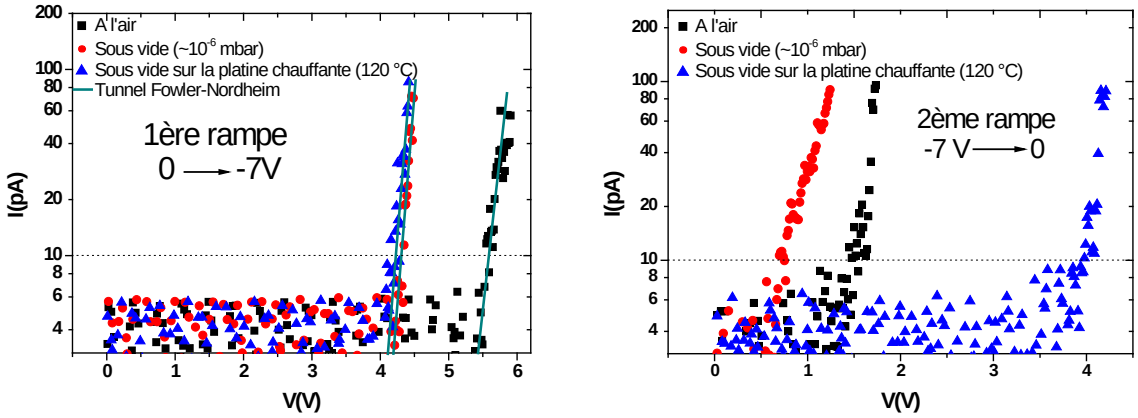


*Figure 8 : Caractéristiques I-V de $SiO_2$ d'épaisseur 3,5 nm effectuées à l'air, sous vide et sous vide sur une platine chauffante.*

Par ailleurs, l'existence d'une bosse sur la surface de l'oxyde, après l'application d'une tension électrique est plus importante à l'air que sous vide, ce qui souligne l'importance du vide dans la réduction de la dégradation électrique et physique de la couche d'oxyde (Figure 9). Ceci est cohérent avec le rôle prédominant de l'effet électrothermique dans la création des bosses pendant la dégradation de la couche d'oxyde à l'air. Le phénomène de conduction a été étudié en utilisant les statistiques de Weibull, où nous avons confirmé que la tension de seuil à l'air est plus élevée que celle sous vide.

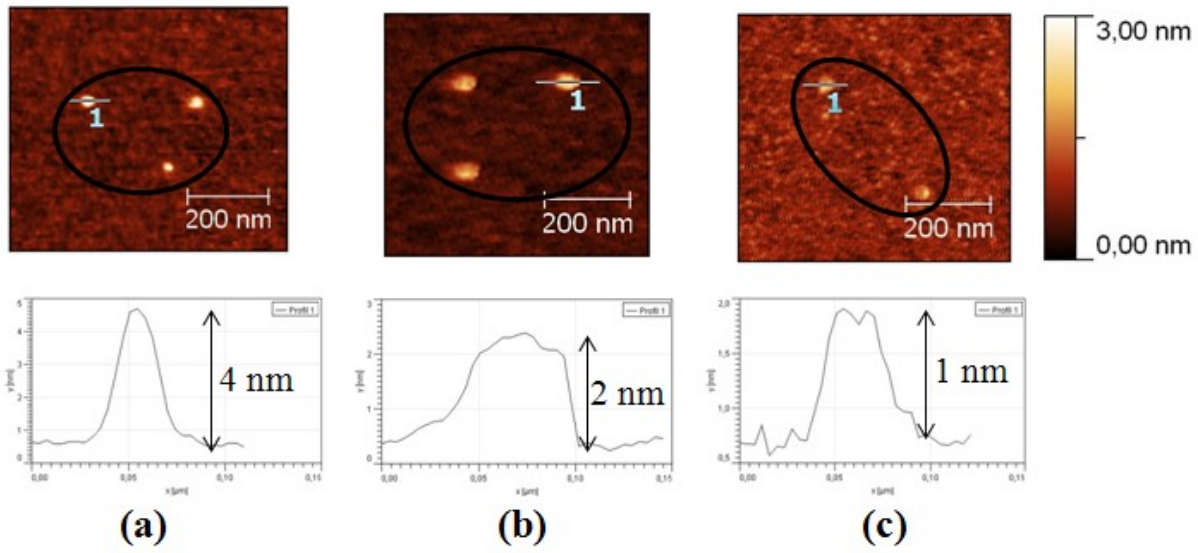


*Figure 9: Topographies après l'application de plusieurs rampes de tension sur des endroits différents et les profils des bosses créées (a) à l'air, (b) sous vide et (c) sous vide sur la platine chauffante.*

En conclusion, nous avons montré qu'afin d'avoir des caractérisations électriques fiables des couches ultra-minces d'oxydes, il est très essentiel d'effectuer ces mesures sous vide avec chauffage. Ceci assure l'élimination complète de la couche d'eau qui joue un rôle très important dans les dégradations physiques et électriques de ces couches.

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# Abstract

Miniaturization of the MOS transistor structure has led to the high thinning of the gate oxide. Hence, degradation and breakdown under electrical stress became one of the important reliability concerns of thin oxide films. The use of characterization techniques allowing to measure leakage currents with a nanometric spatial resolution has shown that breakdown phenomenon of oxides is a highly localized phenomenon. So called “hot spots”, places where the leakage current is very high for a given applied continuous voltage, can be several nanometers wide only. This illustrates why nanometric characterization methods with a nanometer range spatial resolution provide additional information compared to the classical macroscopic characterization. There are two instruments that can be used to do this job, either the Tunneling Atomic Force Microscope (TUNA) or the Conductive Atomic Force Microscope (C-AFM). TUNA which is used in our work is capable to measure very low currents ranging between 60 fA and 100 pA. Our work can be divided into two principle topics:

- Electrical characterization of thin high-k oxides ($LaAlO_3$ and $Gd_2O_3$) at the nano-scale using the Veeco Dimension 3100 where we have shown that the difference in their elaboration techniques largely influence the electrical behavior of these oxides.
- Nano-scale electrical and physical characterization of thin $SiO_2$ thermal oxides in different surrounding ambient, that is in air and under vacuum ($\approx 10^{-6}$ mbar) using the Veeco E-scope microscope. The influence of the experiment surrounding ambient has been well studied where we have shown that the breakdown phenomena of thin oxide films can be highly reduced under vacuum especially in the absence of the water meniscus on the oxide’s surface under study.

Using different AFM modes, it was demonstrated that the existence of the well-known hillock (protrusions) on the oxide’s surface after the application of an electrical stress is a combination of two phenomena: the real morphological modification of the oxide’s surface and the electrostatic force between the trapped charges in the oxide’s volume and the AFM tip. Depending on the current images obtained by TUNA AFM mode, two physical phenomena for the creation of these hillocks have been proposed: the first is the electro-thermal effect and the second is the oxidation of the Si substrate at the Si/oxide interface.

# Content

# General Introduction

The development of the microelectronics industry is related to the continuous enhancement of the performance of the integrated circuits. This constant enhancement strongly depends on the scaling down in size of the dimensions of a key component: the metal oxide semiconductor transistor (MOS). Hence, one of the structures of the MOS transistor that must be scaled down is the thickness of the gate oxide (a few nanometers) whose breakdown leads to the whole structure malfunctioning. So it is important to study the reliability of these oxides at the nano-scale and to improve the techniques of electrical characterization with a nanometric spatial resolution in order to better study the electrical and physical properties of ultra-thin gate oxide films which are used in the fabrication of MOS transistors nowadays.

Actually, our work deals with the study at the nano-scale using the Atomic Force Microscope (AFM) of the electrical and physical reliability of ultra-thin oxide films and aims at enhancing the techniques in use in order to provide better, more reliable and more quantitative results.

In the first chapter we present the context of the thesis, and deal with the continuous miniaturization of the MOS transistor and the difficulties arising due to the scaling down of the transistor's dimensions and how they can be solved. One of the solutions is by replacing the classical $SiO_2$ oxide by high-k ones. Thus we describe $LaAlO_3$ and the $Gd_2O_3$ oxides as good candidates for this replacement. Moreover we underline the importance of nano-scale studies of the degradation phenomenon of gate oxides which is a highly localized phenomenon leading to the transistor malfunctioning and then to the whole system breakdown.

Since this work entirely relies on AFM-based techniques to get the desired information, the second chapter presents the AFM in all its modes (contact, non-contact and intermittent contact modes) focusing on the Tunneling-AFM (TUNA) which is the basic instrument used in this work. Indeed, we evaluate its reliability compared to macro-scale measurements conducted on macroscopic electrodes. In addition, an estimation of the conductive AFM tip's radius used in our work is shown using the Fowler-Nordheim tunneling current model. Then, we present the Electric Force Microscopy (EFM) and the Kelvin Probe Force Microscopy (KPFM) and their utility and finally we present the measurements artifacts and how they can be reduced.

The third chapter presents the nanoscale study by the TUNA on thin high-k oxide films of $LaAlO_3$ and $Gd_2O_3$ deposited by Molecular Beam Epitaxy (MBE) using different

protocols. The aim of this study is to describe at the nanoscale the influence of the ambient gas (molecular or atomic oxygen) used for the growth of the layer on the final electrical properties of $LaAlO_3$ and $Gd_2O_3$. Moreover, the influence of the substrate preparation procedures on the electrical characteristics of $LaAlO_3$ films is explored, namely a high temperature substrate preparation technique leading to an atomically clean surface and a chemical surface cleaning using the Hydrofluoric acid (HF). Finally, a study of the influence of the deposition temperature on the electrical characteristics of $Gd_2O_3$ is presented where I-V measurements have been conducted on films deposited between 650 and 720 °C.

The final chapter focuses on the reliability of the TUNA mode through the study of the physical and electrical properties of thin $SiO_2$ thermal oxide films subjected to electrical stress. It presents the study of the physical nature of abnormal hillocks that appear after the application of a positive voltage on the AFM tip (and negative on the substrate). It is well known that hillocks appear when an inverse polarity voltage is applied on the sample (that is negative on the AFM tip and positive on the substrate) because of the injection of $HO^-$ through the oxide which causes the local oxidation of the Si-oxide interface leading to the inflation of the oxide's surface. But using positive voltages on the tip, such an oxidation should not happen. In order to clarify this point, which is of crucial importance for the reliability of AFM based current measurements, a study of the different parameters governing the creation of hillocks is presented where experiments are conducted in nitrogen ambient, under vacuum and under vacuum with a heating stage in order to better study the influence of the water layer present on the oxide's surface on the occurrence of this phenomenon. Finally, a statistical study of the conduction phenomenon using the Weibull statistics is presented in different surrounding ambient and with different experimental parameters. Conclusions are drawn on the role of the water layer in the breakdown or pre-breakdown of ultra-thin oxides.

# CHAPTER 1 – Context of the thesis

## Content

## 1.1) Miniaturization of the MOS transistor

### *1.1.1) Reasons for MOS scaling and Moore's law*

The Metal Oxide Semiconductor (MOS) structure is one of the most important and simplest components of the microelectronics. It is also essential in the fabrication of the MOSFETs (Metal Oxide Semiconductor Field Effect Transistor) whose number now exceeds the 2 billion in a single microprocessor [1]. Depending on the purpose of the use of a MOS, the desired specifications are either the value of the capacitance C, or the absence of leakage currents through the gate oxide (as shown by the current – voltage (I-V) characteristics), or the linearity of the capacitance (as shown by the C-V characteristics).

Figure 1.1 shows the schematic of the MOS capacitor used in the actual microprocessors, as well as its respective band diagram corresponding to the equilibrium state (gate voltage $V_G = 0$). In the energy band diagram, $E_F$ is the Fermi energy level, $E_C$ and $E_V$ are respectively the conduction band and the valence band energy levels, $\Phi_m$ is the metal work function, and $\chi$ is the electronic affinity of the oxide. $\Phi_{sc}$ and $\Psi_S$ are respectively the semiconductor work function and the surface potential of the substrate and $V_{ox}$ is the oxide's potential difference.

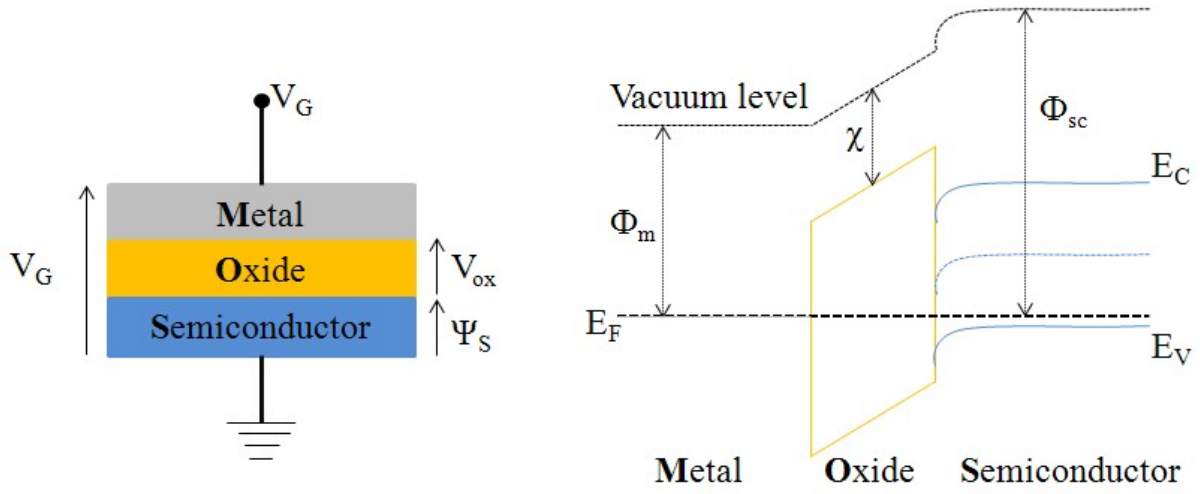


*Figure 1.1: Schematic of the MOS capacitor structure (left) and its corresponding energy band diagram at the equilibrium state (right).*

The work function difference between the metallic gate electrode and the semiconductor induces a band curvature of the conduction and valence bands of the latter. Hence, we can apply a voltage at the metallic gate equal to the flat band potential $V_{FB}$ in order to correct this difference where $V_{FB}$ can be expressed as follows [2]:

$$V_{FB} = \Phi_m - \Phi_{sc} - \frac{Q_{ox}}{C_{ox}} \quad (1.1)$$

where $Q_{ox}$ is the quantity of charges found at the semiconductor/oxide interface and in the oxide's volume, and $C_{ox}$ is the oxide capacitance per unit surface.

Over the past decades, the MOS transistor has continually been scaled down in size. Typical MOS channel lengths were once several micrometers, but modern integrated circuits are incorporating MOS transistors with channel lengths of several tens of nanometers. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Actually, over the past 30 years the number of transistors per chip has been doubled every 2-3 years once a new technology node is introduced. For example the number of MOS transistors in a microprocessor fabricated in a 45 nm technology is twice as large as in a 65 nm chip. This doubling of the transistor count was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law [3][4][5]. Figure 1.2 shows how the number of transistors on a chip is exponentially increasing from 1971 till 2011.

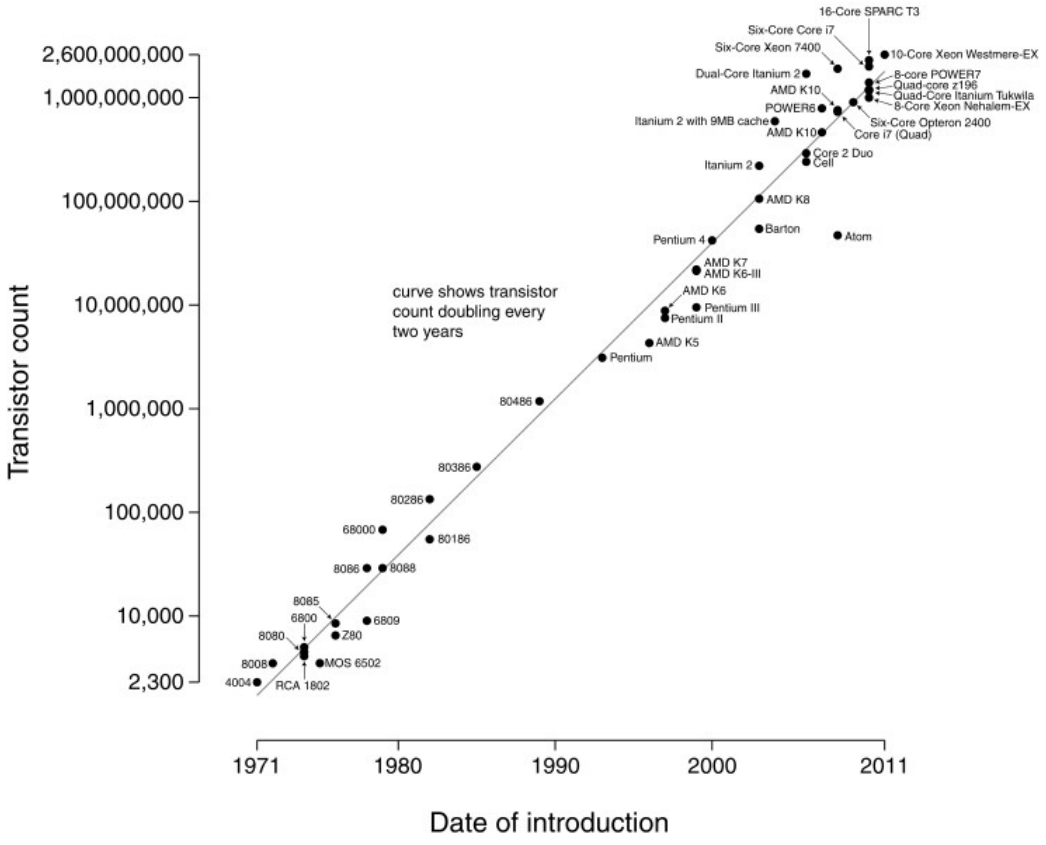


*Figure 1.2: Microprocessor transistor counts 1971-2011 and Moore's law* [6].

Historically, the difficulties with decreasing the size of the MOS transistor have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation.

Indeed, small MOS transistors exhibit higher leakage currents, and lower output resistance, discussed below.

However, it is also expected that smaller transistors switch faster. For example, one approach to size reduction is a scaling down of the MOS transistor that requires all device dimensions to be reduced proportionally by a scaling factor α as proposed in [7] (Figure 1.3). The main device dimensions are the transistor's length, width, and the gate oxide thickness.

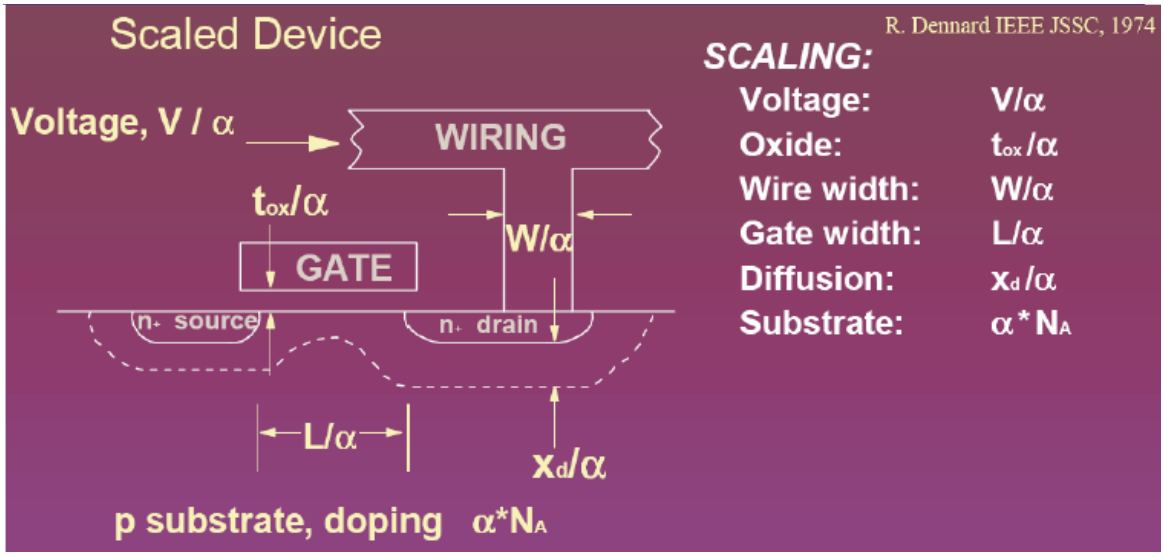


*Figure 1.3: Schematic representation of a scaled MOS transistor by a scaling factor α [7].*

Recently, in May 2011, Intel has announced the invention of the 3-D Tri-Gate transistor manufactured at 22 nm node (Figure 1.4). This great invention is a good evidence of the pursuing of Moore's law and ensuring that the pace of technology advancement consumers expect can continue for years to come. This new transistor uses three gates wrapped around the silicon channel in a 3-D structure enabling a high performance and high energy efficiency.

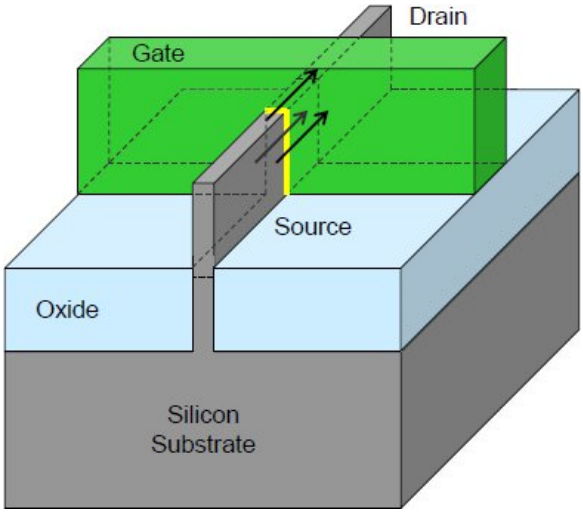


*Figure 1.4: Schematic of the 3-D Tri-Gate transistor manufactured at 22 nm by Intel. Source Intel Corporation.*

### *1.1.2) Difficulties arising due to MOS scaling*

Producing MOS transistors with channel length much smaller than a micrometer is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. In the recent years, the small size of the MOS, below few tens of nanometers, has created operational problems:

- Increased gate – oxide leakage current
- High electric field / Breakdown
- Technological difficulties

Actually, our work deals with the study of the problems related to the increased gate-oxide leakage current and aims at finding solutions to reduce it.

### *1.1.3) Leakage currents: Direct, Fowler-Nordheim, Poole-Frenkel and Trap Assisted Tunneling currents*

When a voltage $V_G$ is applied at the gate of a MOS capacitor, leakage currents through the thin gate oxide appear and they increase as the oxide's thickness decreases [8][9]. These leakage currents are caused by different type of defects related to the oxide itself or to the component structure. These defects assist the passage of charges from one electrode to other through the oxide. Hence, they are responsible of the heating of the electronic devices, of their accelerated degradation and can also induce errors in the functioning and calculations of the microprocessors.

The four different conduction phenomena that can take place and be applied to our studies are the Direct Tunneling, Fowler-Nordheim (FN) tunneling, Poole-Frenkel (PF) emission and the Trap Assisted Tunneling (TAT) which are represented in the energy band diagram of Figure 1.5.

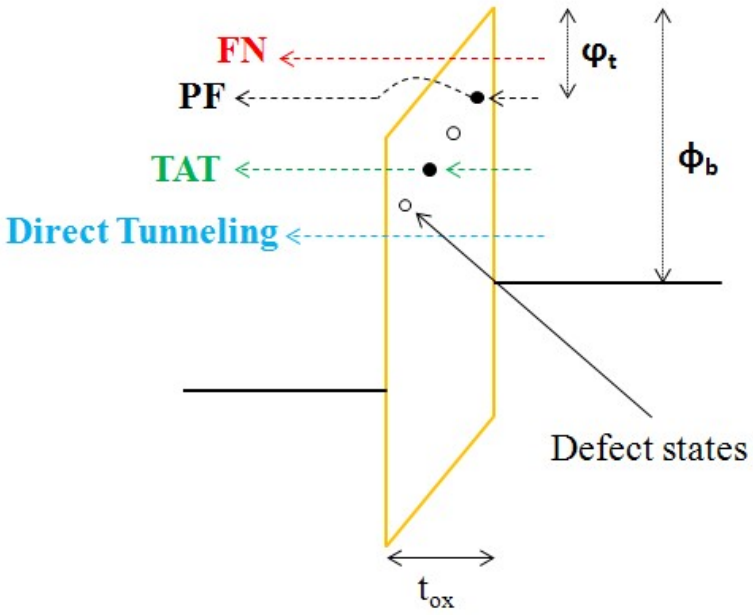


*Figure 1.5: Schematic representation of a MOS's energy band diagram showing the four different conduction mechanisms.*

The four conduction mechanisms can be defined as follows:

- **Direct tunneling current:**

  Tunneling is a quantum-mechanical phenomenon. In classical mechanics, carriers are completely confined by the potential walls. Only those carriers with excess energy higher than the barriers can escape. However, in quantum mechanics, an electron can be represented by its wave-function. The wave-function does not terminate abruptly on a wall of finite potential height and it can penetrate into and through the barrier. The probability of electron tunneling through a barrier of finite height and width is thus not zero [2]. The direct tunneling current can be expressed by the following formula [10]:

$$I_{direct} = A_{eff} \frac{q^2}{8 \pi h \Phi_b} \frac{m_0}{m_{ox}^*} \left(\frac{V_{ox}}{t_{ox}}\right)^2 e^{\left[\frac{-8 \pi \sqrt{q}}{3h} \sqrt{2 m_{ox}^*} \left(\Phi_b^{\frac{3}{2}} - (\Phi_b - V_{ox})^{\frac{3}{2}}\right) \frac{t_{ox}}{V_{ox}}\right]} \quad (1.2)$$

  where $A_{eff}$ is the effective contact area, q is the electron charge, h is Planck's constant, $m_{ox}^*$ is the effective mass of the electron, $m_0$ is the electron rest mass, $\Phi_b$ is the oxide's barrier height, $V_{ox}$ is the oxide's potential difference, $t_{ox}$ is the oxide's physical

thickness. As shown in the formula, the direct tunneling current $I_{direct}$ varies exponentially in function of $1 / V_{ox}$.

- **Fowler-Nordheim tunneling current:**

For thicker gate oxide layers, the tunneling effect is observable only at high values of the applied electric field. This field modifies the potential barrier shape to a triangular one leading to a virtually thinner oxide seen by the charge allowing its tunneling effect through the oxide [11][12][13]. This is the Fowler-Nordheim tunneling which can be expressed as following [10]:

$$I_{FN} = A_{eff} \frac{q^2}{8 \pi h \Phi_b} \frac{m_0}{m_{ox}^*} \left(\frac{V_{ox}}{t_{ox}}\right)^2 e^{\left[\frac{-8 \pi \sqrt{q}}{3 h} \sqrt{2 m_{ox}^*} \Phi_b^{\frac{3}{2}} \frac{t_{ox}}{V_{ox}}\right]} \quad (1.3)$$

Compared to the direct tunneling where the charges traverse all the oxide's thickness, in the FN tunneling the charges traverse a triangular potential barrier of thinner physical oxide's thickness as shown in the band diagram of Figure 1.5.

- **Poole-Frenkel emission current:**

The Poole-Frenkel emission of trapped electrons occurs at moderately high oxide's potential in the case of oxide having many defect states where the trapped electron jumps from the defect to the conduction band by emission effect. The current due to Poole-Frenkel emission is given by [14]:

$$I_{PF} \propto A_{eff} \frac{V_{ox}}{t_{ox}} e^{\left(\frac{-q}{k T} \left(\varphi_t - \left(\frac{q V_{ox}}{\pi \epsilon t_{ox}}\right)^{\frac{1}{2}}\right)\right)} \quad (1.4)$$

where k is Boltzmann's constant, T is the temperature, ε is the dielectric constant and $\varphi_t$ is the trap energy level. Here the current varies exponentially in function of the square root of $V_{ox}$.

- **Trap Assisted Tunneling (TAT):**

It is a two-step tunneling process via traps generated in the dielectric which takes place at low electric fields. The tunneling current is approximately given by [14]:

$$I_{TAT} \propto A_{eff} e^{\left(\frac{-8 \pi \sqrt{2 q m_{ox}^*} t_{ox} \varphi_t^{\frac{3}{2}}}{3 h V_{ox}}\right)} \quad (1.5)$$

In almost all the studies of the reliability of ultra-thin oxide films, a statistical approach is adopted since the dimensions become smaller; it becomes more difficult to measure exact values. In fact, the more dimensions are reduced, the more defects present at

the interfaces or in the volume of the gate oxide become troublesome for the device and its functioning [15].

### *1.1.4) The dielectric electrical breakdown*

The dielectric electrical breakdown is a common phenomenon of gate oxides which takes place when these oxides lose their insulating properties. This is noticed by the strong increase of leakage currents through the oxide when it is subjected to a constant electric field for a given period of time (Time Dependent Dielectric Breakdown TDDB) [16] or when it subjected to a Ramped Voltage Stress (RVS) [17]. Figure 1.6(a) shows a typical plot of the current in function of the stress time of a 5 nm $SiO_2$ subjected to a constant voltage stress (CVS) [17] where the breakdown phenomenon can be evidenced by the strong increase of the current after a given period of time and for a compliance current (C.C.) of 100 nA. Figure 1.6(b) clearly shows the increase of the oxide current for a given applied voltage after nine RVS [17] which can be noticed by the I-V shift towards lower voltage values.

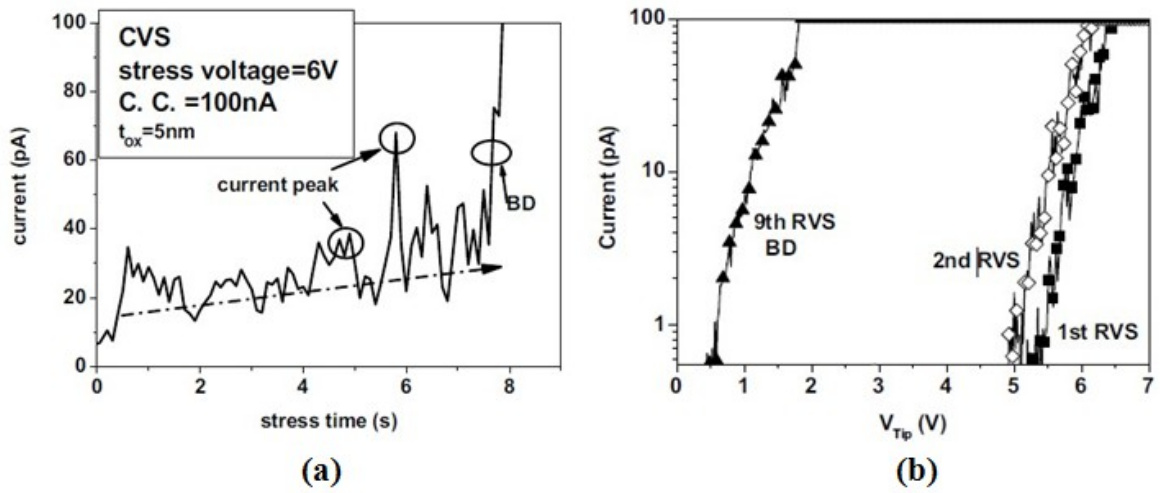


*Figure 1.6: (a) Typical plot of oxide leakage current vs. stress time of a 5 nm $SiO_2$ subjected to CVS. (b) Typical I-V characteristics of 3.4 nm $SiO_2$ [17].*

In general, this phenomenon concerns all the insulators and it constitutes a well opened and complex domain. For solid dielectric oxides used in electronic circuits, the magnitude of the breakdown electric field varies from 1 to 10 $MV.cm^{-1}$ [10].

The main mechanism of the dielectric degradation depends on the generation of electrically active defects (traps) inside the oxide forming at the end a conductive percolation path assisting the charges in passing through the oxide thickness [17-21] (see Figure 1.7). The generation of these defects is caused either by the injection of charge carriers or by the breaking down of chemical bonds. In the first case, the generation of defects is produced

either by the impact ionization that take place at high applied electric field by which the hot injected electrons collide with bound electrons generating a positively charged hole (defect) [22], or by the injection of holes in the oxide coming from the anode electrode [23], or by the release of hydrogen from near the oxide/anode interface [24][25]. In the second case, the thermochemical model [26] allows the calculation of the number of defects per unit of time which is proportional to a reaction constant during a chemical reaction which leads to the breaking down of bonds.

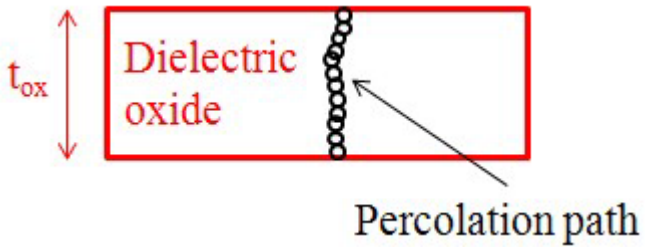


*Figure 1.7: Schematic representation of the formation of a percolation path by the generated defects in an electrically stressed dielectric oxide.*

### *1.1.4.1) Injection of $H^+$ ions*

Here we will discuss in detail the generation of defects by the injection of hydrogen $H^+$ ions into the oxide because it is thought to play an important role in the understanding of the electrical behavior of oxide films when probed with an Atomic Force Microscope (AFM) tip in air.

As mentioned in the reference [25] with larger electric fields Si-Si bond breakage may be induced. However, it is not large enough to induce Si-O bond breakage. In $SiO_2$, stable structure is found in which interstitial Hydrogen attaches to O and stretches the nearby Si-O bonds (Attached-Radical state). The corresponding energy state is approximately 1.0 eV higher than the energy state of the configuration where H resides in the interstitial region. A pair of such attached radical states is stabilized by an additional 1.4 eV when the O attached to the H atoms are both attached to the same Si (Attached-Dimer state) to form a spin single state. The three states are represented in Figure 1.8.

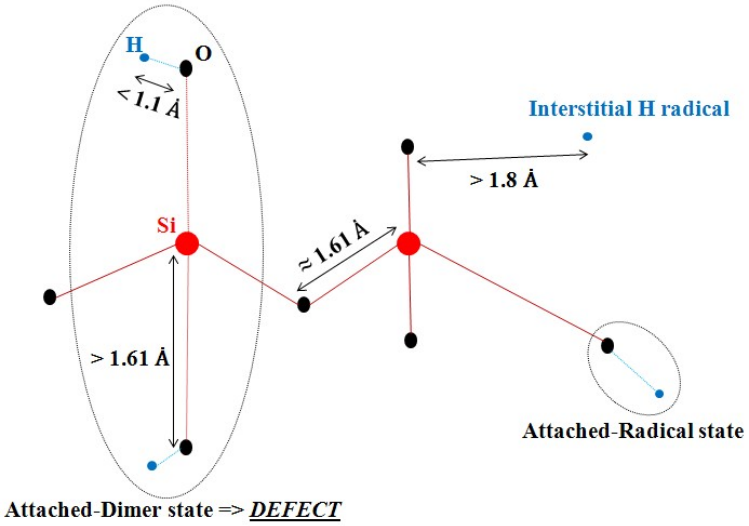


*Figure 1.8: Representative figure showing $SiO_2$ atomic structure with the three states: Interstitial H (O-H distance > 1.8 Å), Attached-Radical state (O-H distance < 1.1 Å) and the Attached-Dimer formed by 2 Attached-Radical states attached to the same Si [25].*

The interstitial H (interstitial state) is known theoretically to be the most stable site for a neutral Hydrogen atom in α-cristobalite and is 1.8 Å from the closest Oxygen (a normal OH bond is 1.0 Å). Moreover, under an applied voltage on the $SiO_2$ structure the local Si-O bonds are stretched of about 0.1 Å (because of the applied voltage), then starting from an O-H distance less than 1.4 Å, the converged geometry always leads to an O-H distance of 1.1 Å with two adjacent stretched Si-O bonds without breakage. The Attached-Radical state would be further stabilized if the initial Si-O bond were elongated leading to a smaller O-H distance as occurs in realistic amorphous $SiO_2$.

It is important to mention that with voltages across the dielectric leading to fields of approximately 5 MV/cm, it is energetically favorable for two Interstitial-Radical hydrogen atoms to form an Attached-Dimer state.

Hence, the formed Attached-Dimer state represents an electrically active defect inside the oxide which plays an important role in the degradation of the oxide layer.

The hot carriers at the anode play an important role in generating H radicals by impact ionization as explained before. It is known that H radicals are unstable in $SiO_2$ and $Si/SiO_2$ interfaces [27][28].

As the electric field across the oxide is increased, the making of the Attached-Dimer states becomes more favorable. These states have diffused “bond” orbitals and lead to states in the $SiO_2$ band-gap. Percolation of H dimers leads to the creation of a pathway for electronic transport through the dielectric and eventual breakdown. In addition, Joule heating from

electron transport due to hopping along a percolating dimer pathway can lead to Si-O bond breaking and hard breakdown.

## 1.2) Interests and properties of high-k oxides

### *1.2.1) The successors of the $SiO_2$*

The usual silicon dioxide $SiO_2$ (silica) which is used in the MOS structures has the following electrical properties: dielectric constant $\varepsilon \approx 3.9$, energy band gap $E_g \approx 9$ eV. $SiO_2$ has reached its physical limits for thicknesses in the order of 1.5 nm because for these thicknesses, leakage tunneling currents become very high and important in causing the malfunctioning of the electronic devices. Nevertheless, these thicknesses are essential for obeying the miniaturization laws of the electronic devices and having high performance systems. A large number of studies have been performed in order to develop oxides with high dielectric constant (called high-k oxides) [30][31]. These materials possess dielectric constants higher than that of the $SiO_2$ and are able to replace silicon oxide in the MOS structures [32][33]. Examples of these materials and their characteristics are given in Table 1.1.

Indeed, if we consider that the surface of the MOS structure is S and the oxide's thickness is $t_{ox}$, then the capacitance can be written as:

$$\mathbf{C = \varepsilon_0\ \varepsilon\ \frac{S}{t_{ox}}} \qquad \textbf{(1.6)}$$

where $\varepsilon_0$ is the vacuum's permittivity and $\varepsilon$ is the oxide's relative permittivity.

So increasing the dielectric constant by using high-k oxides as gate oxides allows the use of a thicker layer while maintaining a high capacitance C (Figure 1.9). Consequently, a higher dielectric thickness reduces the tunneling leakage current through the oxide, hence decreasing the breakdown probability of the whole electronic device.

On the other hand, the notion of the Equivalent Oxide Thickness (EOT) of the gate oxide is introduced for comparing, for the same value of C, the performance of the high-k oxide with respect to the $SiO_2$ oxide. Thus, the EOT of a dielectric of permittivity $\varepsilon$ and thickness $t_{high\text{-}k}$ can be written as:

$$\mathbf{EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon}\ t_{high\text{-}k}} \qquad \textbf{(1.7)}$$

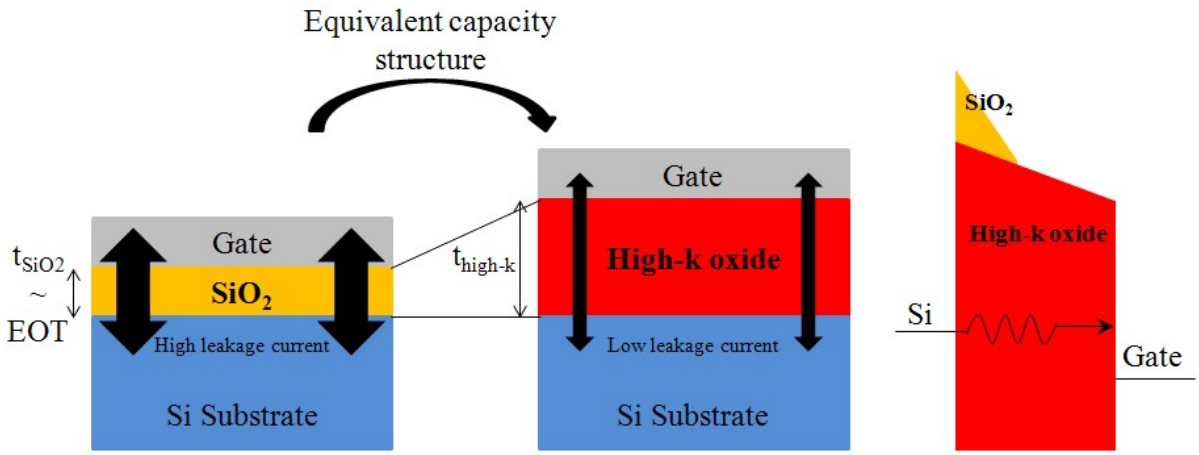


*Figure 1.9: Schematic of the equivalent capacity structure of a MOS with a high-k gate oxide and the corresponding band diagram. Thicker layer of high-k oxide allows limiting the tunneling leakage current through it.*

Actually, the gain in thickness due to the change of the gate material constitutes only a first technological proposition aiming at maintaining of the capacitance. Hence, introducing high-k materials as gate oxides for replacing the usual $SiO_2$ oxide in the electronic applications must respect strict specifications. The specific conditions that the high-k oxide must respect in order to be a good candidate for replacing of the $SiO_2$ oxide are [34]:

- The relative permittivity must be high in order to be able to replace $SiO_2$ for several technological generations.
- In order to ensure an insulating behavior, the band offsets with respect to the substrate must be sufficiently important so that to reduce the injection from the substrate.
- The thermodynamic stability of the oxide in contact with the substrate must be maintained during the whole fabrication process.
- The interface quality is an essential parameter for the carriers' transportation. So a weak interfacial state density is needed, typically less than $10^{11}$ $cm^{-2}.eV^{-1}$ in order to be very close to that of the $SiO_2$/Si interface.
- In addition to minimizing the number of defects in the volume, the integrated material must respond to the specific application needed (power component, memory…).

Table 1.1 shows the characteristics (relative permittivity ε, energy band gap $E_g$, conduction band offset $\Delta E_c$, the electron effective mass $m^*$) of different high-k oxides with their corresponding references.

| Component | ε | $E_g$ (eV) | $\Delta E_c$ (eV) | $m^*$ ($f(m_0)$) | References |
|---|---|---|---|---|---|
| vacuum | 1 | | 4.05 | 1 | |
| $SiO_2$ | 3.9 | 9 | 3.3 – 3.5 | 0.5 | [35] |
| $La_2O_3$ | 25 | 5.5 | 2.3 | 0.26 | [36][37][38] |
| $Al_2O_3$ | 11.6 | 8.8 | 2.8 | 0.35 | [39][40][41][42] |
| $LaAlO_3$ | 24 | 5.6 | 1.8 – 1.9 | 0.3 | [34][43][44][45] |
| $HfO_2$ | 22 | 5.8 | 1.3 – 1.5 | 0.17 | [46][47] |
| $SrTiO_3$ | 277 | 3.3 | -0.1 – 0.3 | | [34][48] |
| $Gd_2O_3$ | 24 | 5.3 | 1.8 | | [49] |

*Table 1.1: Electrical parameters of some high-k oxides with their corresponding references.*

Nevertheless, the different high-k oxides presented in table 1.1 have an energy band gap less than that of the $SiO_2$, which leads to lower barrier heights for electrons and holes. For all the applications, the value of the dielectric constant must be as high as possible. However, the increase of the dielectric constant is correlated to the decrease of the band gap [50]. Consequently, the leakage currents increase as well as the probability of the dielectric breakdown.

Since amorphous $LaAlO_3$ and $Gd_2O_3$ seem to be good candidates in replacing $SiO_2$ in MOS structure, this thesis will address the electrical characterization of these two high-k oxides grown by Molecular Beam Epitaxy (MBE) at INL.

### *1.2.2) Lanthanum Aluminate $LaAlO_3$ oxide (LAO)*

Amorphous LAO oxide appears as an interesting candidate in replacing the $SiO_2$ oxide. From an electrical point of view, it presents a high band gap of 5.6 eV [51], a large conduction band offset of 2 ± 0.1 eV and a large valence band offset of 2.6 ± 0.1 eV [43][52]. The dielectric constant of LAO is from 23.3 to 24.2 [53-55] in its bulk crystalline phase.

One of the interests of this dielectric is that it can be formed of a crystalline lattice compatible with the silicon substrate [34]. Figure 1.10 shows the schematic diagram of the perovskite LAO lattice deposited on a monocrystalline Si [34]. On the other hand, LAO is stable in air and is theoretically thermally stable in contact with Si up to 1000°C [45].

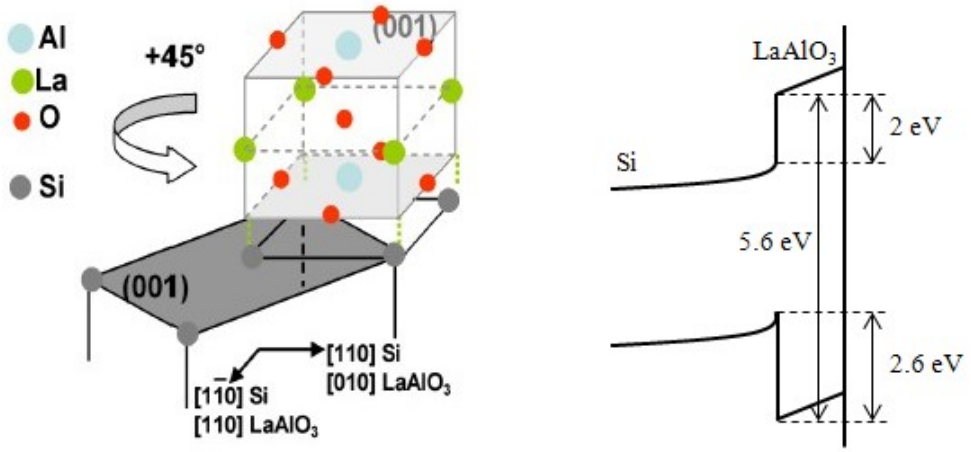


*Figure 1.10: Lattice structure of $LaAlO_3$ and its band alignment with Si* [34].

An advantage of LAO is that it has much lower atomic diffusion rates than $HfO_2$ which is used nowadays in industries. This advantage limits the growth of any subcutaneous $SiO_2$ layer between the Si channel and the oxide which causes a strong decrease of the global dielectric constant of the structure [43][56]. This property of the LAO leads to a higher crystallization temperature and indeed LAO does not crystallize until 850 °C [57]. This important characteristic gives LAO the ability to stay in the amorphous state which is more preferred since it is isotropic and do not contain grain boundaries which act as short circuit diffusion paths.

### *1.2.3) Gadolinium $Gd_2O_3$ oxide (GdO)*

Amorphous GdO belongs to the rare earth oxide family which appears to be also a good candidate in replacing the $SiO_2$ oxide in the future MOS technologies since it covers all the requirements: a wide band gap of 5.3 eV, large conduction and valence band offsets with respect to Si of 1.8 eV and 2.4 eV respectively, and a dielectric constant of 24 [49] (Figure 1.11). Moreover, GdO is thermodynamically stable on Si. As mentioned in [49], GdO films on Si (111) exhibits highly perfect crystalline structure which turns out to be quite appealing for its application to the realization of monolithic integration of functional oxides and semiconductors on the Si substrate.

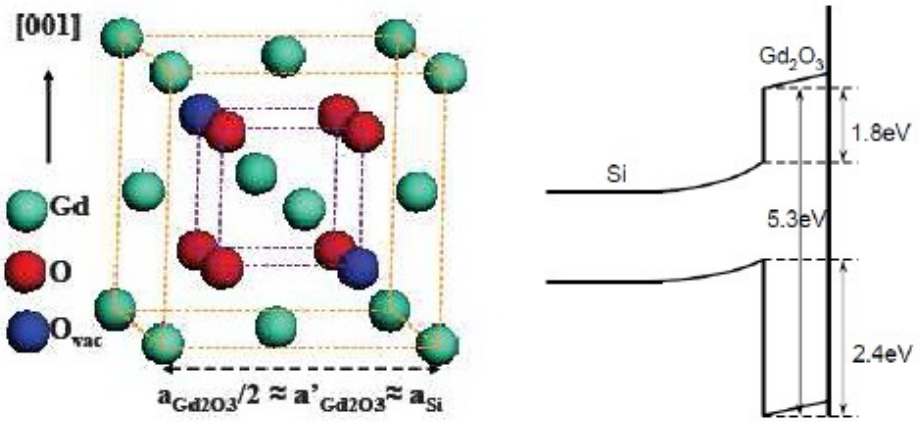


*Figure 1.11: Lattice structure of $Gd_2O_3$ and its band alignment with Si* [49].

Figure 1.12 shows that good EOT results and excellent electric properties (low leakage currents) have been reported for both the LAO and GdO high-k oxides [44].

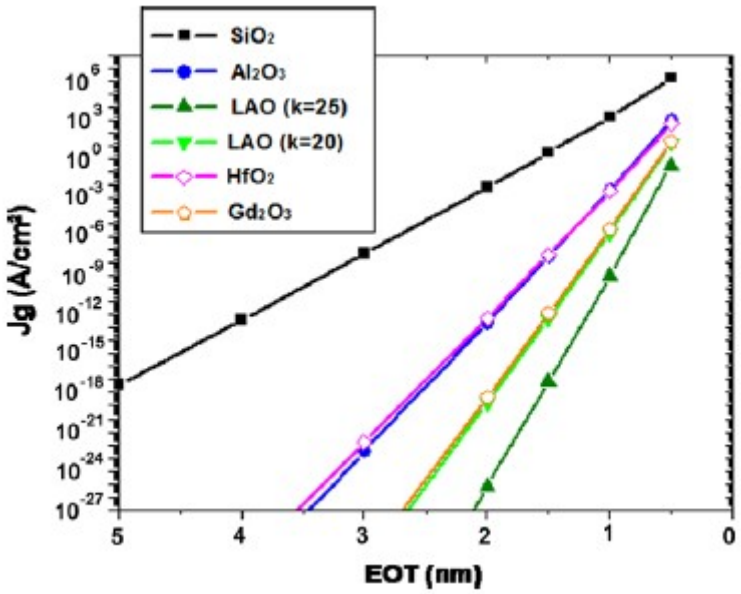


*Figure 1.12: Leakage current densities calculated for a constant gate voltage of 1.5 V as a function of the equivalent oxide thickness EOT for different dielectric oxides* [44] .

Chapter 3 discusses our results about the electrical characterization conducted at the nano-scale on different LAO and GdO samples elaborated at the INL by Sylvain Pelloquin and Gang Niu respectively.

## 1.3) Nano-scale electrical measurements

### *1.3.1) Importance of the nano-scale electrical characterization*

As previously discussed, the continuous miniaturization of MOS structure requires the scaling down of all its components. An essential component is the gate oxide which its degradation leads to the transistor malfunctioning and then to the whole system breakdown. So it is crucial to understand the mechanism of physical and electrical breakdown of the gate oxides. Moreover, the use of characterization techniques allowing to measure leakage currents with a nanometric spatial resolution has shown that breakdown phenomenon of gate oxides is a highly localized phenomenon [21][58][59].

So-called “hot spots”, places where the leakage current is very high for a given applied continuous voltage, can be several nanometers wide only. This illustrates why nanometric characterization methods with a nanometer range spatial resolution provide additional information compared to the classical macroscopic characterization. Indeed, when an electrode of large size is used to record I-V characteristics, the leaky behavior of the hot spots will predominate and the information about the local material electrical properties will be lost. Thus the Atomic Force Microscope (AFM) is used to characterize the electrical properties of the gate oxides since its probe tip area is in the same order of magnitude as the breakdown spot, avoiding the problem of short circuits which can take place between macroscopic electrodes and the Si substrate during the characterization of oxides having many leaky spots. More information on the electrical modes of the AFM is discussed in Chapter 2.

Many works have been done using conductive atomic force microscope (C-AFM). Porti et al have studied the electrical and physical breakdown of thin oxide films using a C-AFM in air [18][19][58][60][61] they have electrically characterized Si nanocrystals based memory MOS devices in order to better investigate their electrical properties at the nano-scale using an AFM [62]. Wu et al also have observed and studied the breakdown characteristics of thin oxide films [17][20][63] and they have studied the nano-scale bias-annealing effect on thin oxide films [64], all these experiments have been conducted by a C-AFM in vacuum to avoid possible contamination and further oxidation on the oxide surface. Zhang et al have visualized the progressive breakdown evolution in thin oxide films [21] and they have studied the breakdown mechanism of ultrathin oxide films [65] using a C-AFM in vacuum for all the experiments. Polspoel et al have studied the physical degradation of thin gate dielectrics using a C-AFM in vacuum also [66]. Sire et al have statistically studied the electrical breakdown of $HfO_2$ and $SiO_2$ thin films using C-AFM in ultra-high vacuum conditions [10][67]. Last and not least, we and Arinero et al have studied the influence of the experimental surrounding on the electrical characterization of thin oxide films in order to find out the best conditions for

more reliable measurements [68]. This last part will be more discussed in section 4.2 of Chapter 4.

In all these references, it has been demonstrated that AFM was able to provide information which are not available at the macroscale. Hence, we propose in this thesis to illustrate this fact.

## 1.4) Conclusion

In summary, this chapter discussed the importance of the continuing miniaturization of MOS transistor following Moore's law and the difficulties that are produced because of this scaling down. One of the problems is the thinning down of the gate oxide which leads to the increasing of the leakage current through it leading to the malfunctioning of the MOS and consequently of the whole device. The four different types of tunneling have been introduced: Direct tunneling, Fowler-Nordheim tunneling, Poole-Frenkel emission and the Trap Assisted Tunneling currents. We have presented the phenomenon of generation of electrically active defects inside the electrically stressed gate oxide and its causes. On the other hand, we have presented high-k oxides as one of the solutions for decreasing the leakage currents by replacing the usual $SiO_2$ oxide in the new technology MOS transistors. We have discussed the properties of $LaAlO_3$ and $Gd_2O_3$ whose nano-scale electrical characterization are presented in Chapter 3. Finally, we have introduced the importance of electrical measurements performed at the nano-scale on thin oxide films.

We now move on to the next chapter talking about the Atomic Force Microscopy.

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# CHAPTER 2 – Atomic Force Microscopy

## Content

## 2.1) Introduction

In 1986, the Atomic Force Microscope (AFM) was invented by Gerd Binnig et al to overcome a limitation of the AFM's predecessor, the Scanning Tunneling Microscope (STM) [1][2]. The STM could only image conductive materials which conduct a tunneling current. STM shows an excellent resolution because of the exponential dependence of the tunneling current on distance such that:

$$I \approx V\, e^{(-2\,K\,d)} \qquad (2.1)$$

where V is the applied voltage, K is the modulus of the wave vector associated to particles at the tunneling barrier and d is the distance between the probe tip and the sample's surface. A representative figure of the STM is shown in Figure 2.1.

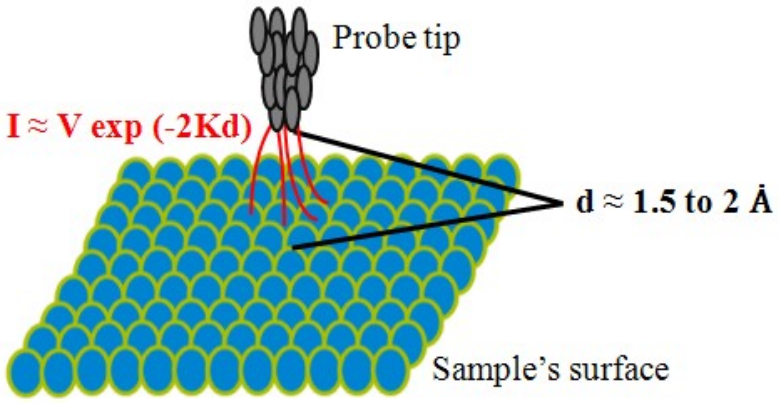


*Figure 2.1: Schematic representation of the STM principle.*

On the other hand, the AFM permitted the imaging of other types of materials, such as polymers and biological samples that do not conduct current. The principle of the AFM is based on the measured forces between an AFM tip and the sample's surface under study. The AFM tip itself is mounted on a flexible cantilever, both made of silicon.

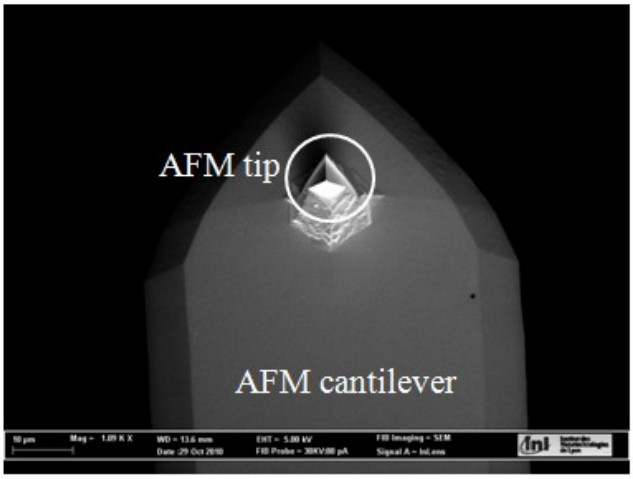


*Figure 2.2: Focused Ion Beam (FIB) image of an AFM cantilever and its tip.*

The interaction forces modify the deflection of the static or the oscillating torsion of the cantilever. These forces largely depend on the tip-surface distance and can be electrostatic, magnetic, Van der Waals or capillary forces. These forces are either attractive or repulsive. Moreover, the interaction potential which is used to represent the interaction between two atoms separated by a distance r is the Lennard-Jones potential ($V_{LJ}$) [3]:

$$V_{LJ} = 4\,\varepsilon \left[ \left(\frac{\sigma}{r}\right)^{12} - \left(\frac{\sigma}{r}\right)^{6} \right] = \frac{A}{r^{12}} - \frac{B}{r^{6}} \qquad (2.2)$$

where ε is the depth of the potential well and σ is the finite distance at which the inter-particle potential is zero. The graph of the Figure 2.3 represents the Lennard-Jones potential between two non-charged atoms.

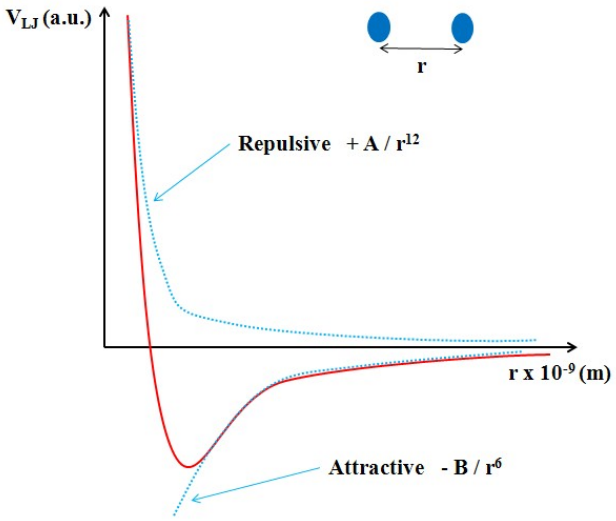


*Figure 2.3: The Lennard-Jones potential between two non-charged atoms [3].*

The AFM is capable to probe the repulsive and the attractive parts of this potential. The force sensor in an AFM is typically constructed from a light lever (Figure 2.2). In the light lever, the output from a laser is focused on the backside of a cantilever and reflected into a 4 quadrants photo-detector. AFM can generally measure the horizontal (X,Y) and vertical (Z) deflections of the cantilever with a picometer resolution (Figure 2.4). The difference between the four photodiode signals indicates the position of the laser spot on the detector and thus the angular deflection of the cantilever. When the tip scans the sample surface, then the deflection of the cantilever can be recorded as an image which represents the three dimensional shape of the sample's surface (contact mode AFM).

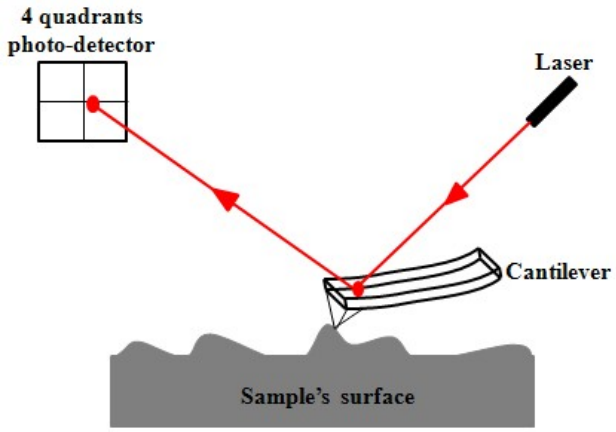


*Figure 2.4: The AFM laser detection system for measuring the cantilever deflection in contact mode.*

## 2.2) Operating principles of the AFM

The AFM can operate in three different modes according to the distance of the tip's cantilever with respect to the sample's surface under study. The three modes are:

- Contact mode
- Non-contact mode
- Intermittent contact mode

These three modes are explained graphically in Figure 2.5 showing the force or the deflection of the cantilever in function of its distance to the sample's surface.

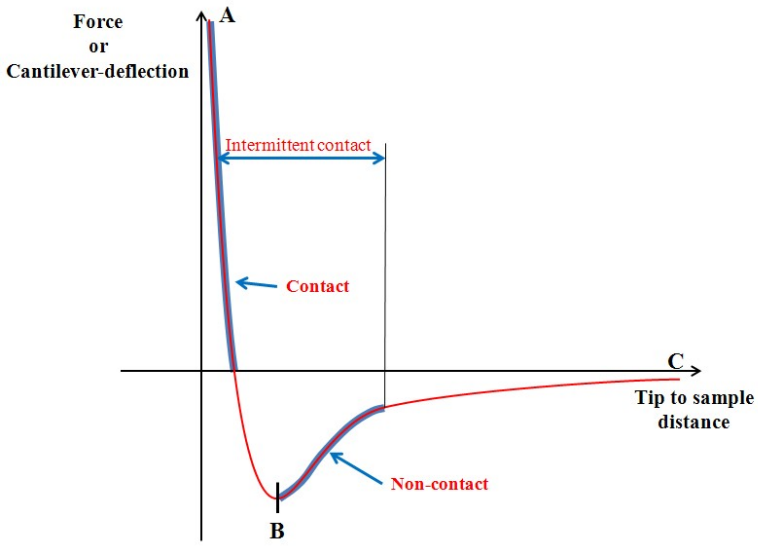


*Figure 2.5: The parts of an approach-retract cycle of the tip.*

### *2.2.1) Contact Mode*

It uses the sum of forces in the region "AB" of Figure 2.5 as the indicator forces for the topography. The tip is attached to the end of a cantilever with a low spring constant (0.02 – 10 N/m). As the scanner gently traces the tip across the sample's surface, the constant force causes the cantilever to bend to accommodate changes in topography (Figure 2.4). The regulation is affected by the measurement of the deviation directions which can be considered as deflections of a spring directly proportional to the force according to Hooke's law:

$$\mathbf{F = k\,\Delta z} \qquad \textbf{(2.3)}$$

where F is the force applied on the cantilever, k is the stiffness of the cantilever and Δz is the distance the cantilever is bent.

The resolution of AFM depends mainly on the sharpness of the tip. Figure 2.6 shows an example of two topography images using a contact mode AFM with two different AFM tips. The left image shows the topography of a 3 nm $LaAlO_3$ high-k oxide film using a $PtIr_5$ coated tip where we can clearly notice the low resolution of the image because of the tip's large apex while the right image shows the atomic resolution topography image of a purple membrane deposited in a buffer solution using an oxide sharpened $Si_3N_4$ tip [4].

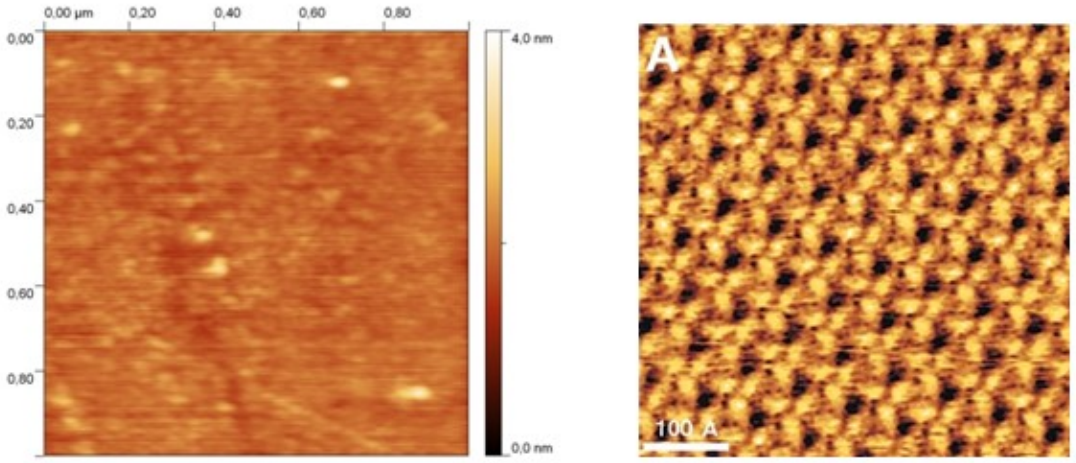


*Figure 2.6: 1 x 1 µm$^2$ topography image in contact mode using Si AFM tip coated by $PtIr_5$ of a 3 nm $LaAlO_3$ high-k oxide (left image) and an atomic resolution topography image of purple membrane surface observed in a buffer solution using an oxide sharpened $Si_3N_4$ AFM tip (right image)* [4].

### *2.2.2) Non-Contact Mode*

This mode was developed in 1987 [5] in order to enhance the techniques of observation of the samples' surfaces. In contrary to the contact mode, the tip does not enter directly in contact with the surface, but it oscillates far from the surface by which it remains sensitive to long range forces. This non-contact mode requires the vibration of the cantilever by means of a piezoelectric bimorph (see Figure 2.7). The cantilever responds to the excitation of the bimorph by oscillating with amplitude $A_0$ depending on the frequency. The system has a resonance frequency of oscillation $f_0$ which depends on its geometry in the absence of any applied external force. When a force $\vec{F}$ is applied on the tip/cantilever system, the resonance angular frequency $\omega_0$ becomes [6]:

$$\omega_0 = \sqrt{\frac{k - \frac{\partial F}{\partial z}}{m}} \qquad (2.4)$$

where m is the mass of the oscillator constituted of the tip/cantilever system, k is the cantilever stiffness and z is the axis covering the distance between the tip and the sample's surface. For values of $\frac{\partial F}{\partial z}$ very small compared to k, the angular frequency shift becomes [6]:

$$\frac{\Delta\omega_0}{\omega_0} = -\frac{1}{2k}\frac{\partial F}{\partial z} \qquad (2.5)$$

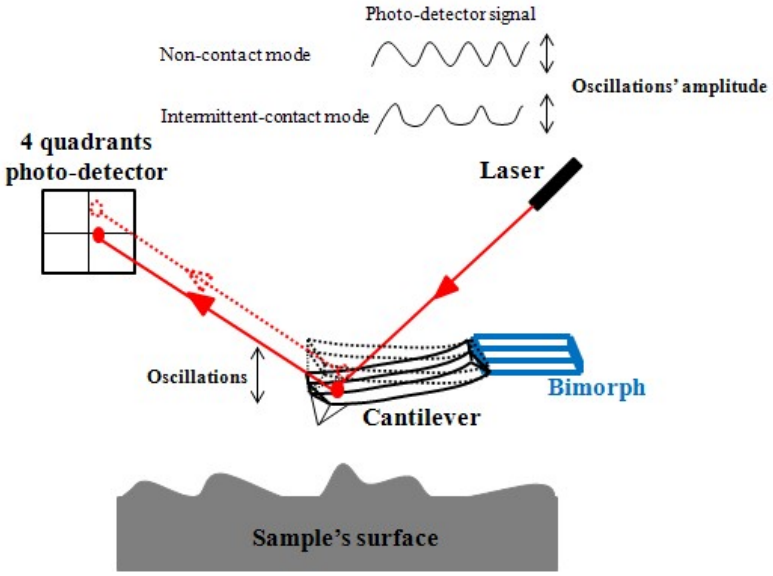


*Figure 2.7: The principle of detection of the cantilever's vibrations' amplitude in non-contact and intermittent modes of the AFM.*

Thus any applied force on the tip causing a non-zero force gradient, will lead to a change in the resonance frequency (attractive force: $\omega_0$ decreases, repulsive force: $\omega_0$ increases). The detection of this force can be operated according to two principles:

- The cantilever is left to oscillate freely at its natural frequency (free oscillations). When interacting with a force from the surface, this frequency will be modified. Then the difference in resonant frequency $\Delta f$ caused by the interaction can be detected. This technique is implemented in ultra-high vacuum systems. Hence, the system is subjected to a constant variation of frequency while the distance between the tip and the sample is modified in order to keep the same $\Delta f$ (constant gradient force mode). Similarly, $\Delta f$ can be registered directly without varying the distance between the tip and the sample's surface (constant height mode).

- The cantilever is excited by a constant frequency (forced oscillation at the drive frequency $f_d$). In this case the difference in the vibrations' amplitude $\Delta A$ can be detected. The system is forced to oscillate at constant amplitude by modifying the distance between the tip and the surface according to the experienced forces. The topography will be then obtained by adopting a tip-sample distance where the van der Waals forces are the dominant ones. The schematic diagram of this procedure is shown in Figure 2.8 where the filled line curve represents the resonance curve of the cantilever in the absence of any applied force while the dotted one represents the resonance curve when an attractive force is applied on the cantilever that leads to the shift of the resonance frequency by $\Delta f$.

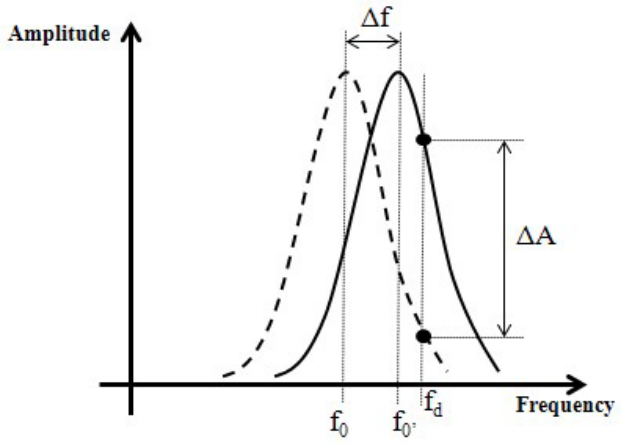


*Figure 2.8: The curve of oscillation of the cantilever in function of the drive frequency of the piezoelectric bimorph.*

The amplitude detection is limited by the characteristic time τ at equilibrium of the oscillator during the variation of the force felt by the cantilever [7]:

$$\tau = \frac{2\,Q}{\omega_0} \qquad (2.6)$$

where Q is the quality factor of the cantilever's resonance. When Q becomes very large, as the case in ultra-high vacuum (UHV), τ also increases unreasonably (it takes about 3τ before reaching the actual equilibrium of the oscillator). So in this case more time is needed in order to obtain a good topography image.

### *2.2.3) Intermittent Contact Mode*

The AFM in air often use a hybrid mode derived from the non-contact mode: the **intermittent contact** or the **tapping**® mode where the cantilever is excited in the same way as in the non-contact mode, but here the tip regularly enters in contact with the surface during its oscillation. This mode uses the amplitude detection principle. Figure 2.9 shows the topography image using the intermittent contact mode of the AFM on a 3.3 nm $LaAlO_3$ high-k oxide.

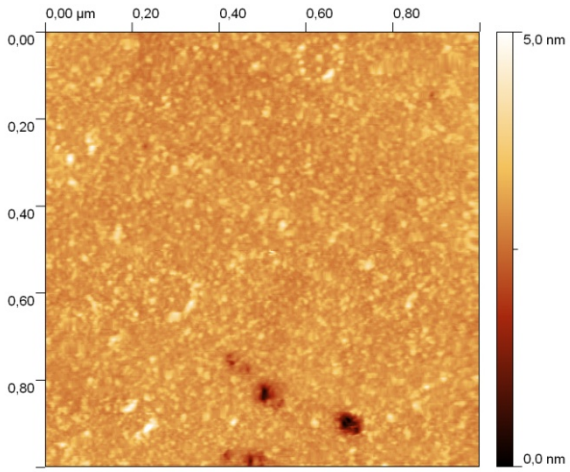


*Figure 2.9: 1 x 1 µm$^2$ topography image in intermittent contact mode using a Si AFM tip of a 3.3 nm $LaAlO_3$ high-k oxide film.*

## 2.3) Tunneling Atomic Force Microscopy (TUNA)

### *2.3.1) Definition and Utility*

TUNA which is the basic instrument used in this work can measure sub-picoampere tip/sample currents through highly resistive samples [8]. Leakage current maps using AFM can be obtained either by the TUNA mode AFM or by the conductive AFM (C-AFM). TUNA is a very sensitive mode by which currents ranging from 80 fA to 120 pA can be measured, while by C-AFM mode, higher currents can be measured ranging from 1 pA to 1 µA (this corresponds to the denomination of the manufacturer of our apparatus-Veeco Instruments – now Bruker) [8]. The principle of the TUNA mode (Figure 2.10) is the same as C-AFM, by which simultaneous topographic imaging and current imaging (constant bias is applied between the tip and the sample) or spectroscopic intensity-voltage (I-V) curves at a local fixed position can be collected. TUNA operates in contact mode by using conductive tip made of silicon coated by $PtIr_5$ for the electrical measurements of the samples. Just like contact mode AFM, the z-feedback loop uses the dc cantilever deflection as a feedback signal to maintain a constant force between the tip and the sample to generate the topography image. In our study, like almost other studies on Si, the tip is grounded and the substrate is negatively biased to minimize possible damages of the tip and to avoid anodic oxidation of the surfaces under study [9][10].

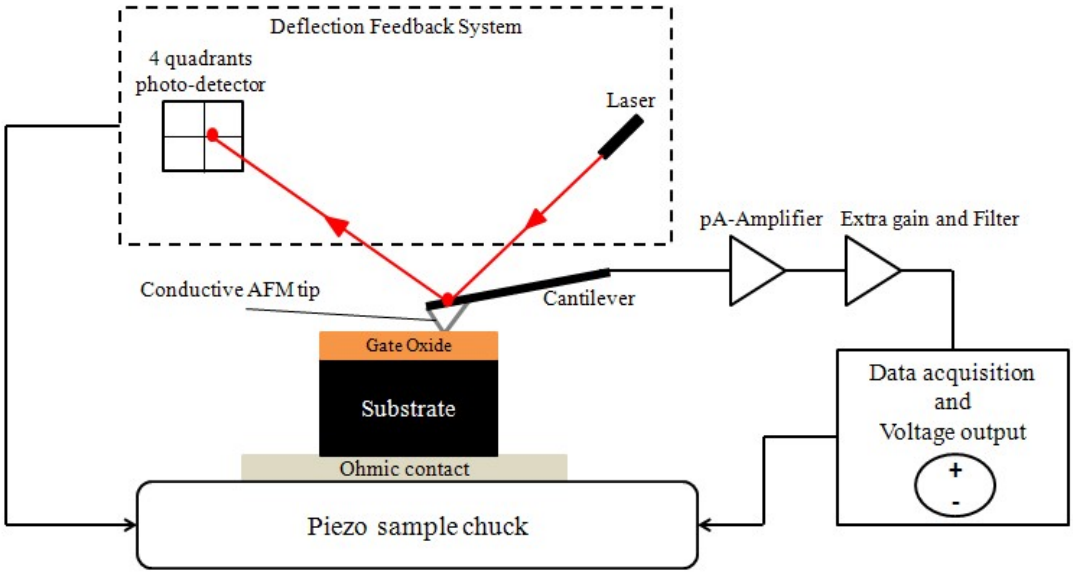


*Figure 2.10: Experimental setup of the TUNA mode AFM.*

TUNA is especially useful for evaluating dielectric films subjected to breakdown, such as silicon dioxide $SiO_2$ oxide films and other transistor gate oxides as the high-k ones. Tip/sample tunneling current depends on film thickness, leakage paths, possibly caused by defects, charge traps and tip geometry. Figure 2.11 shows examples of measurements done by the TUNA mode AFM on a 3.3 nm $LaAlO_3$ high-k oxide film deposited within molecular oxygen $O_2$ ambient. The left image represents the current map conducted by applying a constant voltage of -5.8 V on the Si substrate. The black areas in this current map correspond to the hot spots where the leakage current through the oxide is very high by which it exceeds the saturation current of the apparatus of 120 pA. On the other hand, the right image of Figure 2.11 represents an I-V characteristic of the same oxide where a ramped voltage stress (RVS) was applied from 0 to -10 V with a speed of 0.5 V/s and a current limit of -80 pA to prevent the complete breakdown of the oxide (which means that the ramp is stopped when the current exceeds -80 pA).

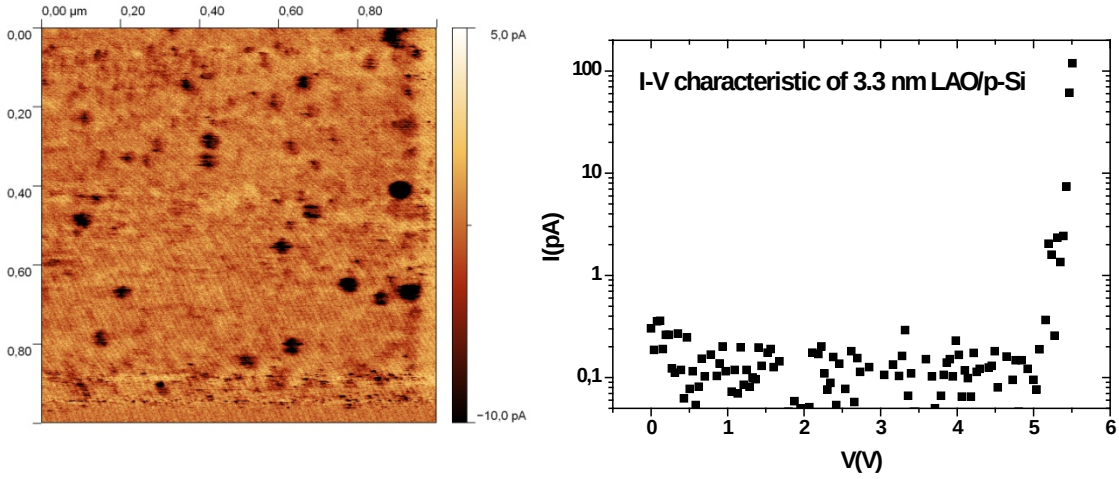


*Figure 2.11: Current map for an applied voltage of -5.8 V (left) and the nano-scale I-V characteristic (right) of the 3.3 nm $LaAlO_3$ high-k oxide deposited within molecular $O_2$ ambient.*

It is essential to note that all the current and the voltage in all the I-V characteristics shown in this work are represented in their ***absolute values*** since the recorded current is negative when the applied voltage is negative on the substrate and positive on the AFM tip. Moreover, all the I-V characteristics shown in this thesis are represented after eliminating the displacement current which can be expressed as:

$$\mathbf{I_{displacement} = C \frac{dV}{dt}} \qquad \mathbf{(2.7)}$$

where C is the capacitance value of the structure AFM tip/oxide/substrate and dV/dt is the speed of the applied RVS. Figure 2.12 shows the same I-V characteristic as in Figure 2.11 adding to it the value of the displacement current $I_{displacement}$ which is approximately 4 pA giving a capacitance value of almost 8 pF when a ramp speed of 0.5 V/sec is used.

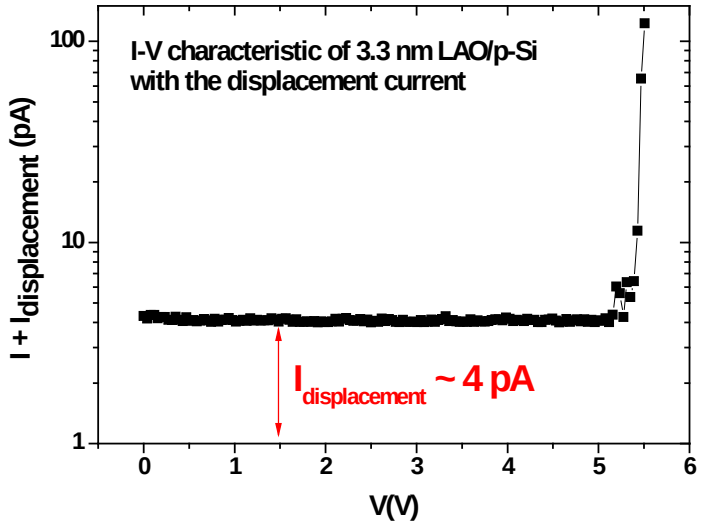


*Figure 2.12: The nano-scale I-V characteristic with the displacement current of the 3.3 nm $LaAlO_3$ high-k oxide deposited within molecular $O_2$ ambient.*

### *2.3.2) Macro vs. Nano electrical characterization*

As previously discussed, electrical characterizations at the nano-scale using the AFM probes are becoming more and more essential in order to study the physical and electrical behavior of gate dielectrics since the breakdown phenomena occur at the nanometric scale. So, it is important to show that electrical measurements using conductive AFM probes ($PtIr_5$ coated tips) are **reliable**. In order to verify that, comparisons have been done between macroscopic electrical characterization (using Agilent 4156B apparatus) and nano-electrical characterization (using Nanoscope V connected to TUNA mode-Veeco AFM) on 11 x 11 $\mu m^2$ Ti/Au electrodes deposited by A. Belarouci of the INL using the e-beam lithography process on 3.5 nm $SiO_2$ thermal oxide on p-type Si substrate ($10^{15}$ at.$cm^{-3}$). Figure 2.13 shows the topography image of the electrode (left) and corresponding line profiles showing the electrode's thickness of ≈ 54 nm.

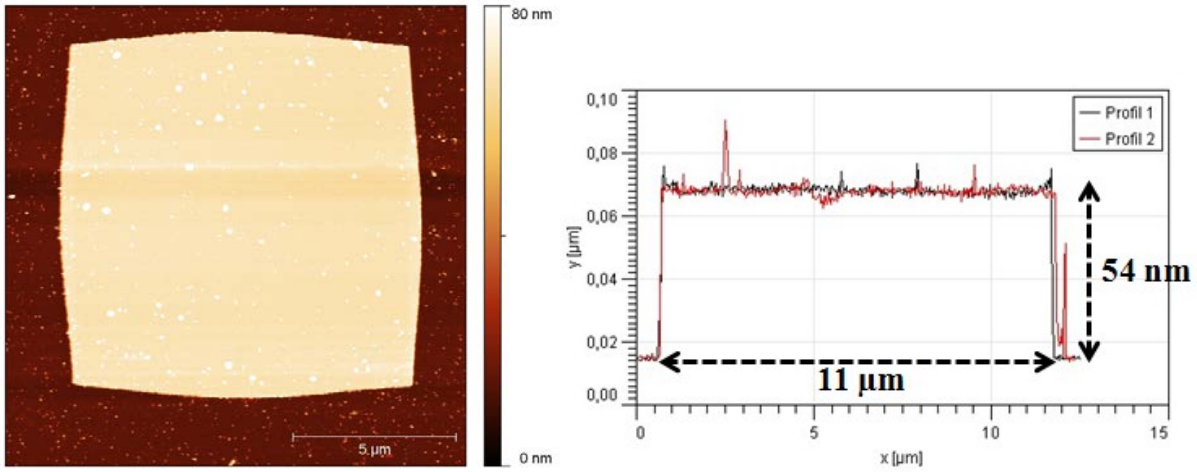


*Figure 2.13: Topography image of the 11 x 11 $\mu m^2$ electrode deposited by e-beam lithography on a 3.5 nm $SiO_2$ oxide film with its transversal and longitudinal profiles (right).*

Figure 2.14 (left) shows representative I-V characteristics obtained at the macro and nano-scale. These characteristics are the average of several tests done on different electrodes of the same dimension in order to show the reproducibility of the measurements. Negative voltage ramps were applied on the substrate from 0 to -3 V with a speed of 0.5 V/sec. As a result, the two I-V characteristics obtained by the two different methods are well superimposed indicating the good reliability of the AFM electrical measurements.

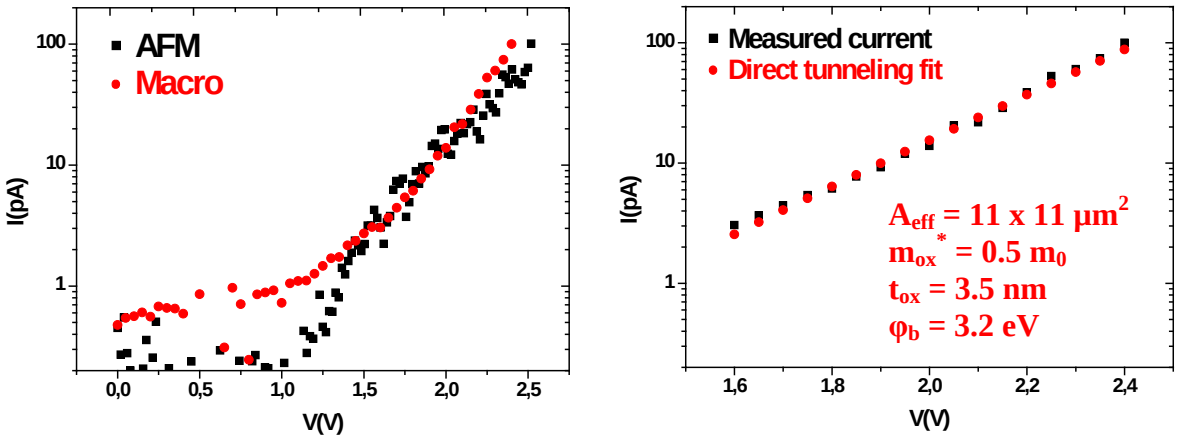


*Figure 2.14: Nano and Macro I-V characteristics (left) and the direct tunneling fit of the macro characteristic (right) on 11 x 11 µm$^2$ electrode deposited on 3.5 nm $SiO_2$ thermal oxide.*

On the other hand, to study the correspondence of these characteristics to the tunneling current through a thin oxide film and for voltages lower than 3.2 V (corresponding to the $SiO_2$ barriers height), direct tunneling has shown a perfect fit to these characteristics as shown in the right graph of Figure 2.14. The direct tunneling through oxides can be expressed as [11]:

$$\mathbf{I_{direct} = A_{eff}\ \frac{q^2}{8\,\pi\,h\,\Phi_b}\ \frac{m_0}{m_{ox}^*}\ \left(\frac{V_{ox}}{t_{ox}}\right)^2\ e^{\left[\frac{-8\,\pi\,\sqrt{q}}{3\,h}\sqrt{2\,m_{ox}^*}\left(\Phi_b^{\frac{3}{2}} - (\Phi_b - V_{ox})^{\frac{3}{2}}\right)\frac{t_{ox}}{V_{ox}}\right]}} \qquad \mathbf{(2.8)}$$

where $A_{eff}$ = 11 x 11µm$^2$ is the effective contact area, q is the electron charge, h is Planck's constant. In a first approximation we considered $m_{ox}^*/m_0$ = 0.5 is the effective mass of the electron in the conduction band of $SiO_2$, $t_{ox}$= 3.5 nm is the oxide's physical thickness, $\Phi_b$=3.2 eV is the $SiO_2$'s barrier height [12] and $V_{ox}$ is the oxide's potential difference which is given by:

$$\mathbf{V_{ox} = V_G - \Phi_{MS} - \Psi_S} \qquad \mathbf{(2)}$$

$V_G$ is the gate voltage, that is the voltage applied on the AFM tip, $\Phi_{MS} \approx$ -0.15 eV is the work function difference between the tip which is coated by $PtIr_5$ metal (work function value ≈ 4.7 eV [13]) and the p-doped Si substrate of doping concentration ≈ $10^{15}$ at.cm$^{-3}$ and $\Psi_S$ is the surface potential of the substrate which in our case is in its inversion regime since the applied voltage $V_G$ is positive on the tip and largely greater than $\Phi_{MS}$.

### *2.3.3) Estimation of the AFM tip's radius*

For almost all the nano-scale current measurements that we have done, we have used the $PtIr_5$ coated tips because of their high mechanical and electrical stability [14][15]. One of the unknown essential parameters of the I-V characteristics carried out at the nano-scale is the effective contact area between the tip and the sample. This contact area depends on different variables such as the force applied by the tip on the sample, the surrounding conditions and the apex of the tip. For this reason and in order to avoid fluctuations in our measurements, we have used the same value of the deflection setpoint (0.5 V) in order to have approximately the same contact area for all our measurements using the same type of conductive tips.

I-V characteristics of 3.5 nm $SiO_2$ thermal oxide film on p-type Si of doping concentration ~$10^{15}$at.cm$^{-3}$ have been conducted in order to extract the effective contact area $A_{eff}$ using the Fowler-Nordheim tunneling fit. RVS was applied from 0 to -10 V with a ramp speed of 0.5 V/sec and a current limit of -20 pA to preserve the tip from Joule effect. Figure 2.15 shows the measured I-V characteristic $I_m$ in pA with the corresponding FN current density $J_{FN}$ in pA/µm$^2$.

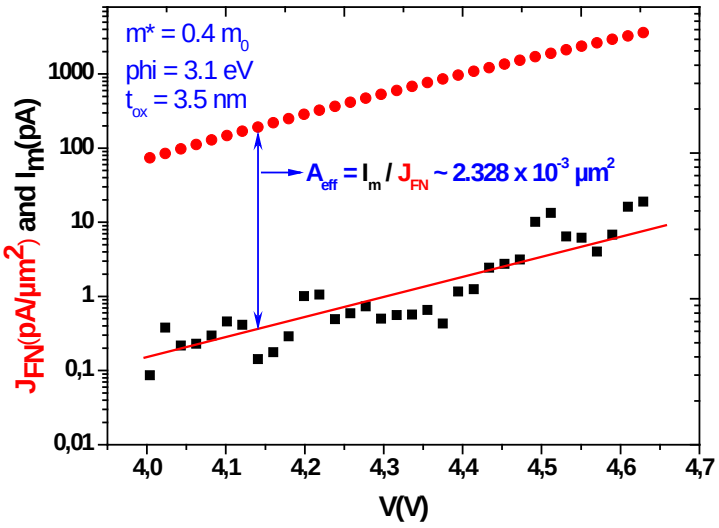


*Figure 2.15: Measured I-V characteristic and the FN current density with the fit parameters of 3.5 nm $SiO_2$ thermal oxide using a $PtIr_5$ coated tip.*

The FN tunneling formula used is:

$$I_{FN} = A_{eff}\ \frac{q^2}{8\,\pi\,h\,\Phi_b}\ \frac{m_0}{m_{ox}^*}\ \left(\frac{V_{ox}}{t_{ox}}\right)^2\ e^{\left[\frac{-8\,\pi\,\sqrt{q}}{3\,h}\sqrt{2\,m_{ox}^*}\ \Phi_b^{\frac{3}{2}}\ \frac{t_{ox}}{V_{ox}}\right]} = A_{eff}\ J_{FN} \qquad (2.9)$$

In a first approximation the values of the parameters are taken as follows:

$\Phi_b$ = 3.1 eV, $m_{ox}^*/m_0$ = 0.4, and $t_{ox}$ = 3.5 nm. Hence, by calculating the ratio of the measured current $I_m$ on the FN current density $J_{FN}$, an approximate value of the contact area can be determined which is found to be in our case ~ 2328 $nm^2$. If we consider a circular contact area we can determine the radius of the tip to be ~ 26 nm. It is important to remind that this experiment was conducted in air ambient. Smaller value of the contact area was used by Sire et al. in [16] where they have used a value of 10 $nm^2$ since they have conducted their measurements in UHV ambient (< $10^{-9}$ torr). However, the higher value determined in our work can be attributed to the existence of a water meniscus between the tip and the surface which leads to a larger contact area when the experiments are conducted in air ambient.

On the other hand, as discussed is section 1.1.5 of Chapter 1, the degradation of the oxides can be remarked from the shift of the I-V characteristics towards lower values of the applied voltage. We used this phenomenon in order to verify the value of the tip's radius where several I-Vs have been carried out on different locations by the displacement of the same tip by distances varying from 20 to 50 nm while for each location the degradation of the oxide has been detected by the high increasing of the oxide's current after the previous RVS. The protocol of the experiment is presented by the tip's displacement scheme of Figure 2.16. The RVS applied on the 3.5 nm $SiO_2$ film were from 0 to -10 V with a ramp speed of 0.5 V/sec and without any current limit in order to breakdown the oxide at the zone where the voltage is applied. Figure 2.17 shows the corresponding I-V characteristics.

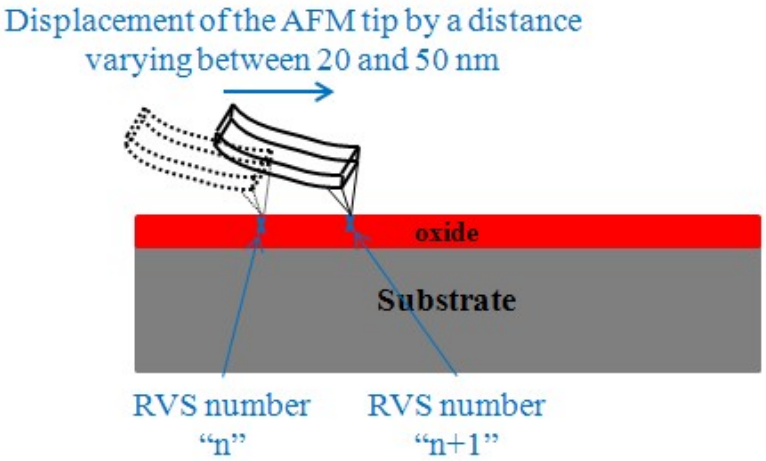


*Figure 2.16: Scheme representing the displacement of the AFM tip. At each location of the tip, RVS are performed.*

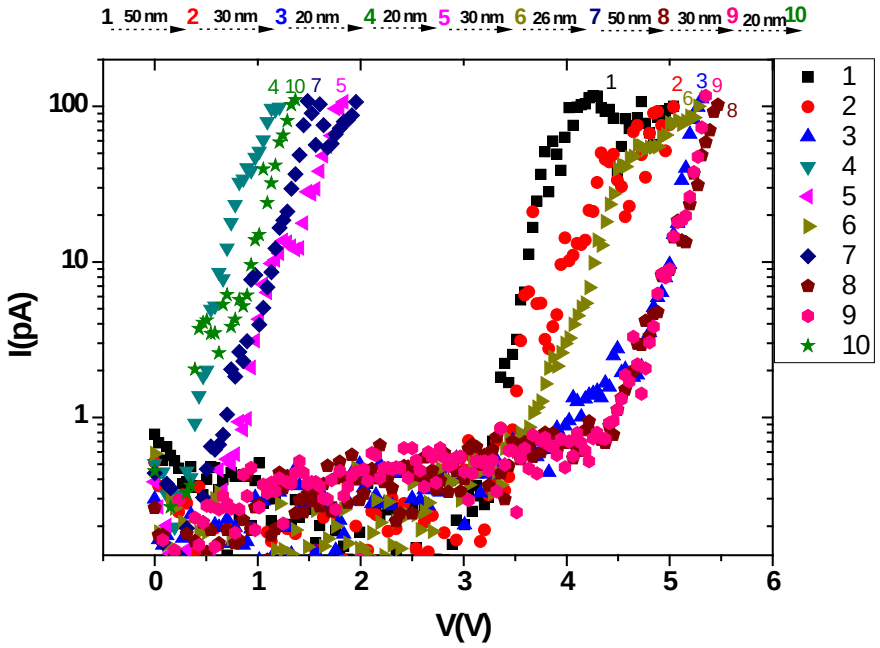


*Figure 2.17: 10 I-V characteristics on 10 different locations separated by distances between 20 and 50 nm carried out on the 3.5 nm $SiO_2$ thermal oxide using the same $PtIr_5$ coated tip.*

It is shown in this Figure that when the distance between two successive locations (i.e. between RVS number n and RVS number n + 1, 1 < n < 9) where the RVS has been applied is 30 nm and above (as between the 1st and 2nd, 2nd and 3rd, 5th and 6th, 7th and 8th, 8th and 9th RVSs) the tip is located on a fresh zone giving a normal I-V characteristic of the 3.5 nm $SiO_2$ oxide film. On the other hand, for a distance of 26 nm (as between the 6th and 7th RVSs) or 20 nm (as between the 3rd and 4th, 4th and 5th, 9th and 10th RVSs) the n+1 RVS shows a highly broken down oxide where the measured current is very high (I-V shifted towards small voltage values).

This means that if we considered that the apex of the tip is circular, the radius of the tip (that is the contact area between the tip and the sample) is approximately 26 nm.

## 2.4) Electric Force Microscopy (EFM)

The Electric Force Microscopy is one of the microscope's modes which operate in the non-contact mode. The long range force that the EFM is capable to detect is the electrostatic Coulomb attraction force. A complete description of the EFM mode can be found in the reference [7].

The EFM is used to further evaluate the role of trapped charges on the measured contrast of topography images in order to study the physical properties of hillocks created on the oxide's surface after the application of an electrical stress (discussed in Chapter 4). EFM is used to map the vertical (Z) and near-vertical gradients of the electric field between the tip and the sample versus the in-plane coordinates X and Y. It operates using the so-called "Lift

Mode" or "Double pass Mode" which necessitates a double scan of the surface as explained in Figure 2.18.

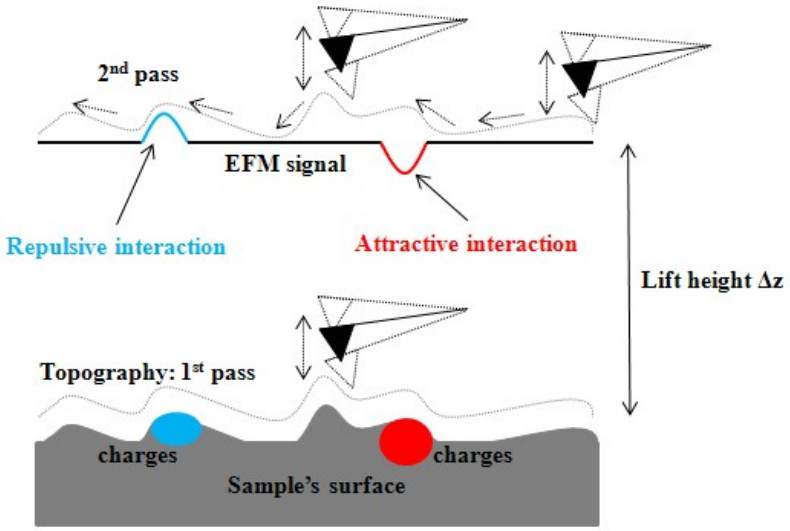


*Figure 2.18: Principle of the Lift Mode EFM.*

The first pass is used to record the topography by using the classical intermittent contact mode AFM. The second pass is operated at a distance of 10 to 50 nm from the sample's surface and the tip-sample distance is kept constant by following the previously recorded topography. Any change of the amplitude vibration of the lever will be due to a long range interaction. For a better sensitivity, the phase signal between the vibration of the cantilever and the excitation of the piezoelectric bimorph is often recorded as shown in Figure 2.19. The EFM data are thus generated during the second pass in a lift mode.

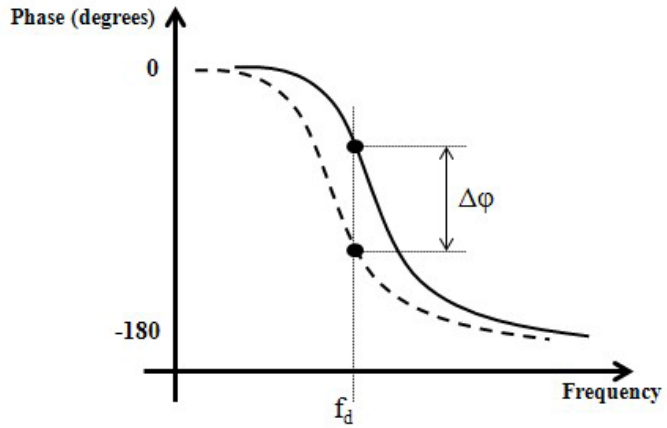


*Figure 2.19: EFM phase signal of the cantilever as a function of the drive frequency of the piezoelectric bimorph used to generate the EFM signal.*

In Figure 2.18, the blue and red-colored regions in the sample symbolize the charged source of contrast in an EFM image. The electric field due to trapped charges (on or beneath

the sample surface) is often sufficiently large to generate contrast in the EFM image in order to distinguish whether the detected charges are negative or positive ones [17]. Otherwise, a field can be induced by applying a voltage between the tip and the sample.

## 2.5) Kelvin Probe Force Microscopy (KPFM)

The Kelvin Probe Force Microscopy, also known as surface potential microscopy, is a noncontact variant of the AFM that was invented in 1991 [18]. With KPFM, the work function of surfaces can be observed at atomic or molecular scales. The work function relates to many surface phenomena, including reconstruction of surfaces, doping and band-bending of semiconductors, charge trapping in dielectrics and corrosion. The map of the work function produced by KPFM is able to provide information about the composition and electronic state of the local structures on the surface of a solid.

KPFM is a scanning probe method where the potential offset between a probe tip and a surface can be measured using the same principle as a macroscopic Kelvin probe [18]. The cantilever in the AFM is a reference electrode that forms a capacitor with the surface, over which it is scanned laterally at a constant separation. The cantilever is not piezoelectrically driven at its mechanical resonance frequency $\omega_0$ as in normal AFM although an alternating current (ac) voltage is applied at this frequency.

When there is a potential difference between the tip and the surface, the combination of the constant (dc) potential difference and the alternating (ac) applied voltage will cause the cantilever to vibrate. The origin of the force can be understood by considering that the energy of the capacitor formed by the cantilever and the surface is:

$$\mathbf{E = \frac{1}{2}C[V_{dc} + V_{ac}\sin(\omega_0 t)]^2 = \frac{1}{2}C[2V_{dc}V_{ac}\sin(\omega_0 t) - \frac{1}{2}V_{ac}^2\cos(2\omega_0 t)]} \quad \mathbf{(2.10)}$$

plus constant terms. Only the cross-term proportional to the $V_{dc}V_{ac}$ product is at the resonance frequency $\omega_0$. A null circuit is used to drive the dc potential of the tip to a value which minimizes the vibration. A map of this nulling dc potential versus the lateral position coordinate therefore produces an image of the work function of the surface.

KPFM is based on an AFM setup and the determination of the work function is based on the measurement of the electrostatic forces between the AFM tip and the sample. The potential called the "contact potential difference" denoted generally with $V_{cpd}$ is the potential which arises from the difference of the Fermi levels of the tip and the sample when they are brought into contact. For the measurement of $V_{cpd}$, a voltage is applied between the tip and the sample, consisting of a dc-bias $V_{dc}$ and an ac-voltage $V_{ac}\sin(\omega_2 t)$ driven at the second resonance frequency $\omega_2$ of the AFM cantilever:

$$\mathbf{V = (V_{dc} - V_{cpd}) + V_{ac}\sin(\omega_2 t)} \quad \mathbf{(2.11)}$$

Tuning the ac-frequency to the second resonance frequency of the cantilever results in an improved sensitivity and allows the independent and simultaneous imaging of the topography and the contact potential. As a result of these biasing conditions, an oscillating electrostatic force appears, inducing as additional oscillation of the cantilever with the characteristic frequency $\omega_2$. The general expression of such electrostatic force not considering coulomb forces due to charges can be written as:

$$\mathbf{F = \frac{1}{2}\frac{dC}{dz}V^2 = F_{dc} + F_{\omega_2} + F_{2\omega_2}} \quad \textbf{(2.12)}$$

The dc component, $F_{dc}$ contributes to the topographical component, the term $F_{\omega 2}$ at the characteristic frequency $\omega_2$ is used to measure the contact potential and the contribution $F_{2\omega 2}$ can be used for capacitance microscopy.

$$\mathbf{F_{dc} = \frac{dC}{dz}\left[\frac{1}{2}\left(V_{dc} - V_{cpd}\right)^2 + \frac{1}{4}V_{ac}^2\right]} \quad \textbf{(2.13)}$$

$$\mathbf{F_{\omega_2} = \frac{dC}{dz}\left(V_{dc} - V_{cpd}\right)V_{ac}\sin(\omega_2 t)} \quad \textbf{(2.14)}$$

$$\mathbf{F_{2\omega_2} = -\frac{1}{4}\frac{dC}{dz}V_{ac}^2\cos(2\omega_2 t)} \quad \textbf{(2.15)}$$

For contact potential measurements a lock-in amplifier is used to detect the cantilever oscillation at $\omega_2$. During the scan, $V_{dc}$ will be adjusted so that the electrostatic forces between the tip and the sample become zero and thus the response at the oscillation frequency $\omega$ becomes zero. Since the electrostatic force at $\omega_2$ depends on $V_{dc} - V_{cpd}$, $V_{dc}$ corresponds to the contact potential. Absolute values of the sample work function can be obtained if the tip is first calibrated using a reference sample of known work function.

### *2.5.1) Estimation of the $PtIr_5$ work function*

We have conducted experiments with the collaboration of Richard Arinero at the South Institute of Electronics (IES), University of Montpellier 2, UMR CNRS 5214, in order to estimate the value of the $PtIr_5$ work function.

We have used KPFM (lift mode - double pass mode) on a sample of gold Au as the reference sample since its work function is known to be ≈ 5 eV [19]. We have used the method of the force gradient of the dc component (grad $F_{dc}$) such that:

$$\mathbf{\text{grad } F_{dc} = \frac{1}{2}\frac{d^2C}{dz^2}\left(V_{dc} - V_{cpd}\right)^2 + \frac{1}{4}\frac{d^2C}{dz^2}V_{ac}^2} \quad \textbf{(2.16)}$$

since the frequency variation $\Delta f$ is directly proportional to the force gradient, we can trace $\Delta f = f(V_{dc})$ and we can search the value of "$V_{dc} - V_{cpd}$", then we can obtain the value of the $PtIr_5$ work function such that:

$$\mathbf{V_{cpd} = q\left(\varphi_{tip} - \varphi_{Au}\right)} \quad \textbf{(2.17)}$$

Figure 2.20 (left) shows the contact potential image of the Au sample scanned by a $PtIr_5$ tip and applying different values of dc voltage in order to trace Δf in function of the $V_{dc}$ as shown in the right image of Figure 2.20.

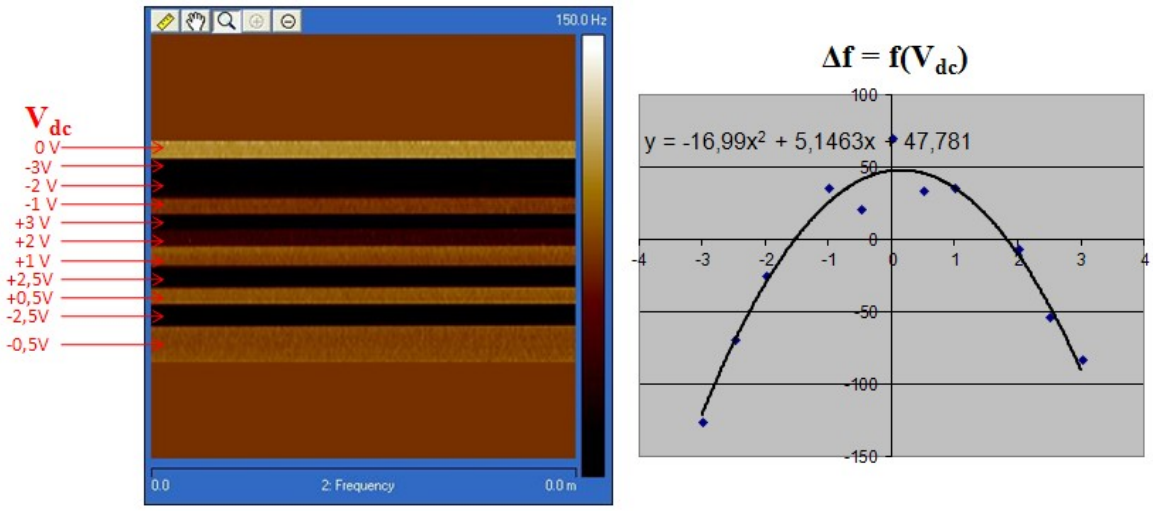


*Figure 2.20: Contact potential image of Au sample scanned by a $PtIr_5$ tip (left) and the corresponding $\Delta f = f(V_{dc})$ curve (right).*

As a result, $V_{cpd}$ was found to be -0.15 V leading to a $PtIr_5$ work function value to be: $\varphi_{Au}$ - 0.15 eV ≈ 4.85 eV which is coherent with the value found in [13].

## 2.6) Measurements' limitations and artifacts

### *2.6.1) Experimental perturbations and their solution*

Topography recording and electrical measurements by AFM are commonly affected by artifact that must be controlled.

Because of the humidity of the atmosphere where the measurements are performed, a water meniscus is present between the AFM tip and the sample. The applied voltage at the tip during imaging or spectroscopy measurements of the current produces electrochemical migration. In some cases, the apex of the tip and the state of the surface under study are modified.

The shape of the tip and the presence of protrusions at its extremity can have an effect on the electric field and increase its value in a non-controllable manner at the apex of the tip [20][21].

The most common measurements' artifacts and their possible solutions can be listed as following:

- Double tip

The double image (Figure 2.21) takes place when the AFM tip interacting with the sample has two apexes. This can be solved by scanning the tip over the surface for a while in order to remove the contamination found at the tip. Otherwise, if the image quality is not improved after few scans, then the AFM tip should be replaced.

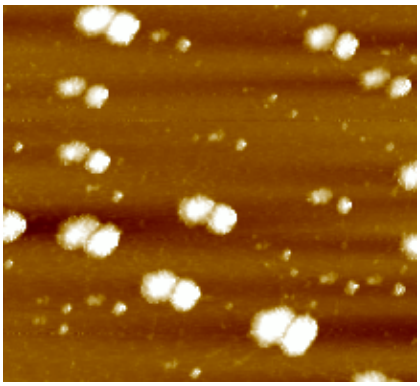

*Figure 2.21: Topography image showing the double tip effect.*

- Oxidation of the tip

  It is caused by the natural dissociation of $HO^-$ ions causing the oxidation of the tip and resulting in a more important apparent thickness of the tip and a work function shift. This problem can be reduced by conducting measurements under vacuum or under nitrogen ambient.

- Erosion of the tip

  It is the cause of friction of rigid and hilly surfaces. Its consequences are that we may lose the lateral resolution of the tip and the current intensity in the case of current measurements. This problem can be reduced by applying less force on the tip or by using cantilevers with small stiffness.

- Effect of the tip length

  It is caused by the rapid scanning which results in jumps in the image and this problem can be solved by changing the scan parameters or changing the type of the tip.

### *2.6.2) Importance of the Faraday cage*

A Faraday cage or Faraday shield is a grounded enclosure formed by conducting material or by a mesh of such material. We have introduced this cage around the AFM system in order to decrease the noise in the current measurements caused by the present electrostatic charges. Figure 2.22 shows the difference between two current images, one conducted in the absence of the Faraday cage while the other is conducted in its presence. The left image of

Figure 2.22 shows an example of a noised current image ($I_{RMS}$ = 0.9 pA) conducted on 2 nm $SiO_2$ oxide film without any applied voltage at the tip and without using the Faraday cage while the right image shows a non-noised current image ($I_{RMS}$ = 0.5 pA) because of the presence of the Faraday cage.


*Figure 2.22: Current images taken the absence of the Faraday cage (left image: $I_{RMS}$ = 0.9 pA) and in its presence (right image: $I_{RMS}$ = 0.5 pA).*

## 2.7) Conclusion

In summary, this chapter covered the essential ideas of the AFM focusing on some of the electrical measurements modes (TUNA, EFM and KPFM) used in this work. The importance of the TUNA mode of the AFM has been shown and its validity has been demonstrated by comparing the macroscopic current measurements to those conducted at the nanoscale. Moreover, the contact area between the AFM tip and the sample's surface was estimated (radius ≈ 26 nm) using the Fowler-Nordheim tunneling model. We have verified the value of the radius by doing successive I-V measurements on different zones by displacing the tip from 20 nm to 50 nm away from where the previous I-V has been carried out. In addition, the necessity of the EFM and KPFM modes has been represented where we have estimated the value of the $PtIr_5$ work function (≈ 4.85 eV). Finally, we have discussed the AFM topographical and electrical measurements' artifacts and how they can be reduced.

## 2.8) References

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# CHAPTER 3 – High-k thin oxide films

## Content

## 3.1) Introduction

In this chapter, thin films of $LaAlO_3$ and $Gd_2O_3$ deposited by Molecular Beam Epitaxy (MBE) using different protocols have been studied at the nanoscale by TUNA. Degradation and breakdown under electrical stress is one of the important reliability concerns of gate oxides and since this phenomenon is highly localized [1][2][3], the microscopic characterization may provide additional information compared to the macroscopic characterization. Therefore TUNA appears as a natural tool to characterize these high-k oxides since its probe tip area is in the same order of magnitude as the breakdown spot, allowing to avoid the problem of short circuits which can take place between macroscopic electrodes and the Si substrate during the characterization of oxides having many leakage spots (the case where the measured leakage current arises from a few leakage spots cannot be distinguished from a uniform leakage current flowing from the whole electrode area).

The aim of this study is to describe at the nanoscale the influence of the ambient gas (molecular or atomic oxygen) on the electrical properties of LAO and GdO proposed as a gate oxide replacing $SiO_2$ in MOS structures (*see section 1.2 of Chapter 1*). Moreover, the influence of the substrate preparation procedures on the electrical characteristics of LAO films has been explored, namely a high temperature substrate preparation technique leading to an atomically clean surface and a chemical surface cleaning using the Hydrofluoric acid (HF).

Finally, a study of the influence of the deposition temperature on the electrical characteristics of GdO is presented where I-V measurements have been conducted on films deposited between 650 and 720 °C.

## 3.2) $LaAlO_3$ thin oxide films

### *3.2.1) Preparation of the samples*

The LAO films were elaborated by Sylvain Pelloquin at INL in the frame of his PhD thesis at the Ecole Centrale de Lyon. The LAO films were deposited at 400°C on p-type (001)-oriented Si substrates ($10^{15}$ at.cm$^{-3}$) by electron beam evaporation of crystalline LAO targets in a RIBER2300 molecular beam epitaxy (MBE) reactor equipped with a system of reflection of high energy electron diffraction (RHEED) system. Prior to the film deposition, two different surface preparations were performed to remove native $SiO_2$ from Si substrates. For all samples, a $SiO_2$ layer was grown by ozonation under UV exposure for 20 min. "HF-last" samples were simply dipped in a diluted Buffer Oxide Etch solution (BOE) before introduction in the reactor. "High-T" samples were cleaned using a four-steps procedure: chemical cleaning with BOE solution, re-ozonation of the surface for 2 min to form a thin

protective $SiO_2$ layer and introduction in the molecular beam deposition (MBD) chamber, annealing at 900°C in ultra-high vacuum and finally electron beam evaporation of Si/Si at 650°C to obtain a perfect 2 × 1 reconstruction (RHEED controlled). LAO was then deposited using a two-step procedure: 1) LAO deposition with no additional O pressure until complete disappearance of the Si RHEED pattern, to avoid or limit interface reactions, and then 2) LAO deposition under a 5 x $10^{-6}$ Torr oxygen partial pressure. For "molecular O" samples, molecular oxygen was used in step 2), while for "atomic O" samples, atomic oxygen (produced using a RF-plasma cell) was used in step 2.

X-Ray Reflectometry (XRR) was used to measure their physical thickness. XRR is a non-destructive analyzing technique which was discovered in 1954 by Lyman G. Parrat [4] and then improved by S.K. Sinha et al. [5] in order to introduce the roughness of layers to the technique. This technique uses the X-ray diffractometer to obtain the thickness, the roughness and the density of a thin layer film as also as a multi-layer film. Its principle is based on the reflection of an X-ray beam on the sample's surface (Figure 3.1(a)). After calibration, the source and the detector move simultaneously with respect to the plane of the sample's surface (2θ between 0 and 15°, θ being the incidence angle) and we measure the intensity of the reflected beam ($I_{reflected}$). The spectrum log($I_{reflected}$) in function of 2θ (Figure 3.1(b)) presents fringes which are interferences due to the thickness of the traversed layer(s). The critical angle $\theta_C$ of the total reflection depends of the density of the traversed material. The slope of the spectrum and the amplitude of the oscillations give information about the roughness at the interfaces and the density contrasts.

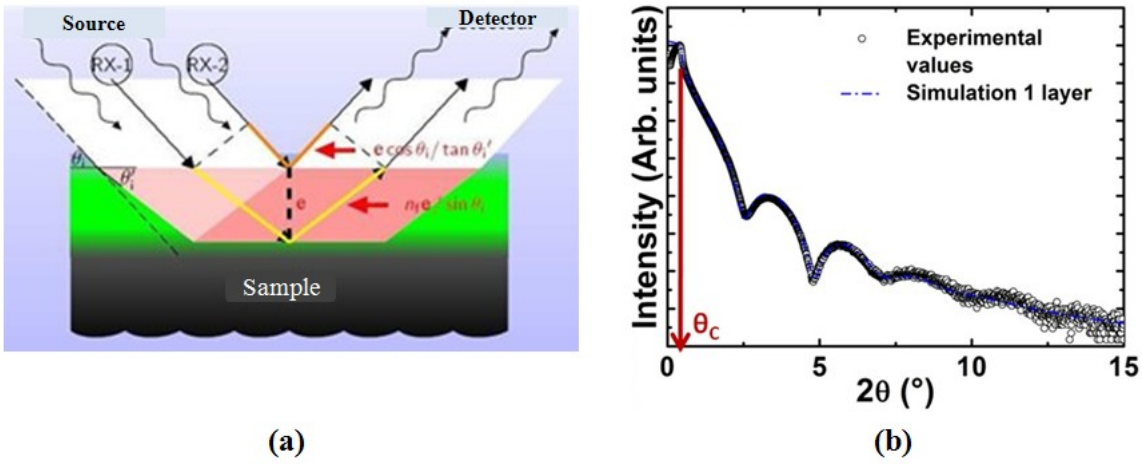


*Figure 3.1: (a) Principle of functioning of X-ray reflectivity. (b) Example of XRR spectrum obtained by Sylvain Pelloquin on a 3.7 nm LAO oxide film with a density of 5.6 g.cm$^{-3}$*

Specifically, the parameters (thickness, density, roughness) are obtained by matching a simulation (software GXRR Rigaku Smartlab) bringing these three parameters with the spectrum obtained. This method is very sensitive to initial parameters of correspondence and

requires a good knowledge of the influence of the latter. The measurements were performed on a Rigaku diffractometer Smartlab.

Returning back to our experiments, we will present two groups of samples where each group contains two different samples. In the **1st group** two samples **A** and **B** are presented, where for sample A, LAO was deposited within molecular O ambient, while for sample B it was deposited within atomic O ambient. For both samples the High-T process was performed before the LAO deposition. Both samples have a thickness between 3.2 and 3.3 nm with uncertainty of 0.3 nm.

The **2nd group** contains two other samples **C** and **D**, where for both samples LAO was deposited within atomic O ambient. However, the difference between the two samples is the applied surface preparation procedure; High-T process for sample C, and HF-last process for sample D. Both samples have a thickness between 3.7 and 3.8 nm with uncertainty of 0.3 nm. Table 3.1 summarizes the essential data of all the samples.

| **LAO** | Samples | | | |
|---|---|---|---|---|
| | 1st Group | | 2nd Group | |
| | **A** | **B** | **C** | **D** |
| Deposition ambient | Molecular O | Atomic O | Atomic O | Atomic O |
| Si surface preparation process | High-T | High-T | High-T | HF-last |
| Thickness ± 0.3 nm | 3.3 | 3.2 | 3.8 | 3.7 |

*Table 3.1: Deposition characteristics and thicknesses of the LAO samples under study.*

### *3.2.2) Topographical study of the samples*

Topographies of the four samples using the intermittent contact mode (Tapping®) of the AFM are shown in Figure 3.2. These 2 x 2 $\mu m^2$ topography images have been taken using a Si tip oscillating near its resonant frequency ranging from 280 to 320 kHz.

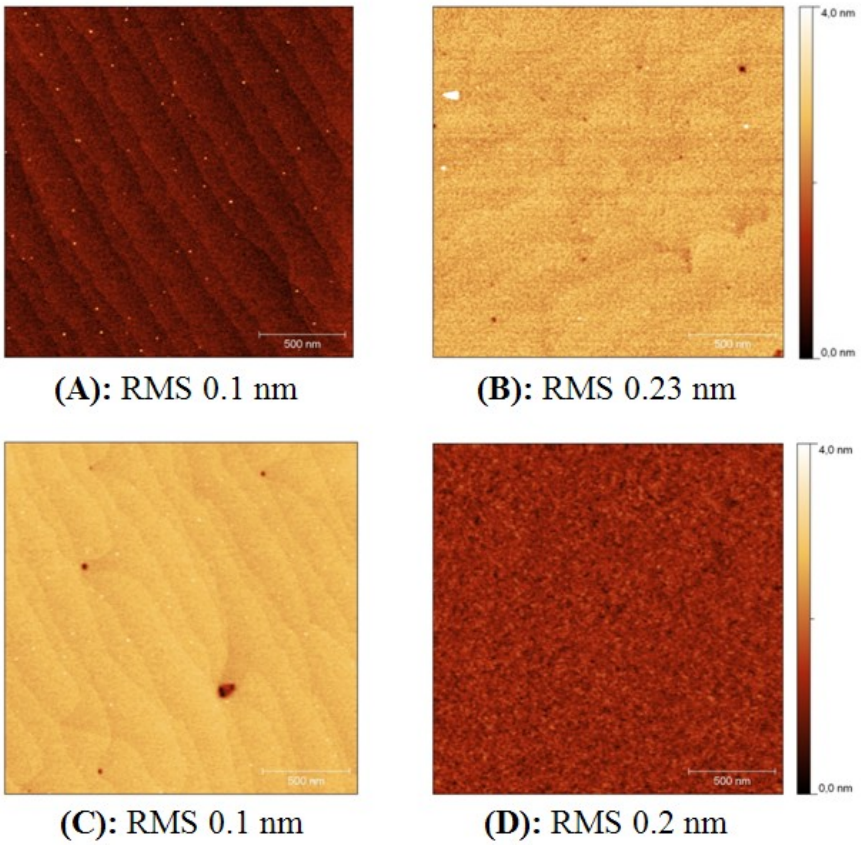


*Figure 3.2: 2 x 2 µm$^2$ topographies of the four LAO samples with their corresponding RMS values.*

The roughness of the surface of the samples expressed by its root mean square value (RMS) varies between 0.10 nm and 0.23 nm for the four different samples as shown in Figure 3.1. So with these small values of RMS we can consider that the four samples have a good quality surface and the current measurements are not disturbed by the topography of the surface.

We notice in the topography images of samples A, B and C (High-T samples) the existence of holes and humps. Although the hypothesis is still under study, this may be explained this way: when it is heated during the deposition of LAO, a reaction takes place on the Si substrate between carbon atoms which exist in the MBE chamber and the Si substrate forming silicon carbide molecules (SiC) which appear sometimes as humps and sometimes as holes when the humps explode. On the other hand, for sample D where the HF-last process is adopted for the surface preparation we can notice that there are neither holes nor humps on the surface revealing that HF-last is better for surface cleaning at the atomic scale.

### *3.2.3) Influence of different parameters on the electrical characteristics of the samples*

Current-Voltage measurements have been conducted on the four samples in order to study the influence of two different parameters on the electrical characteristics of the samples:

- Influence of the deposition ambient: Molecular O vs. Atomic O ambient, comparison between sample **A** and sample **B** is done.
- Influence of the Si surface preparation before the LAO deposition: High-T vs. HF-last procedure, comparison between sample **C** and sample **D**.

#### *3.2.3.1) Influence of the deposition ambient: Molecular O vs. Atomic O ambient*

Figure 3.3 shows the normalized macroscopic I-V characteristics with respect to the electrodes' surfaces on the samples A and B where the voltage was applied on the tip while the substrate was grounded. The measurements have been done on Ni (3 nm) / Au (250 nm) metal electrodes with different surfaces ranging from 100 x 100 $\mu m^2$ to 600 x 600 $\mu m^2$. The good influence of the deposition of LAO within atomic oxygen ambient is also obvious from the clear difference in the density of current through samples A and B (the current density at -2 V is more than one order of magnitude for sample A with respect to sample B). From the comparison with nano-scale characterization, this can now be related to the smaller amount of nanometric leaky spots combined with a higher local threshold voltage for samples elaborated within atomic O ambient.

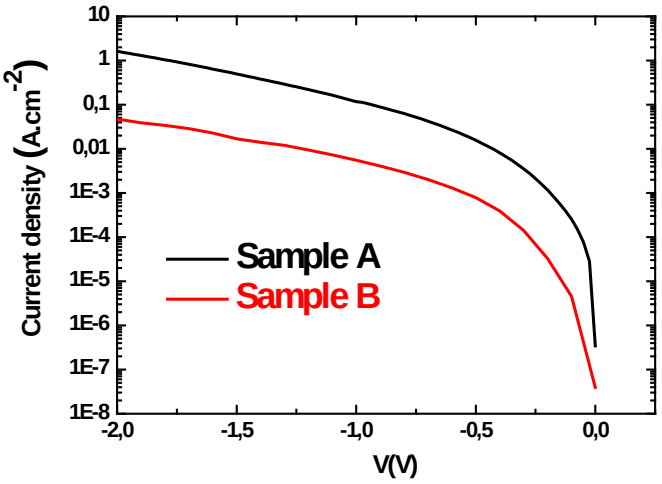


*Figure 3.3: Macroscopic I-V characteristics of sample A (black curve) and of sample B (red curve).*

Now we will present the nano-scale electrical characterization of samples A and B performed by the TUNA. 1 x 1 $\mu m^2$ current images of each sample are shown in Figure 3.4. We have increased gradually the value of the applied voltage until dark areas have appeared on the images reaching the value of -5.8 V on sample A with a current scale [-10 pA (dark), 5 pA (bright)] and -7.2 V on B with a current scale [-9 pA (dark), 1 pA (bright)]. On current images, darker areas correspond to hot spots where the leakage current is higher. These hot spots appeared instantaneously with the passage of the AFM tip on the surface during the first scan and they evolve during the second scan indicating the oxide's degradation after the first one. We notice that the density of leaky spots (black rounded areas) which are the most conductive regions where the current through the oxide exceeds 120 pA, is smaller in sample B than in sample A even with the application of a lower voltage on A. Considering several different AFM images, the density of leaky spots can be estimated: it is about 20 x $10^8$ per $cm^2$ for sample A and 12 x $10^8$ per $cm^2$ for that of sample B demonstrating better dielectric property for the latter sample where LAO was deposited within atomic O ambient.

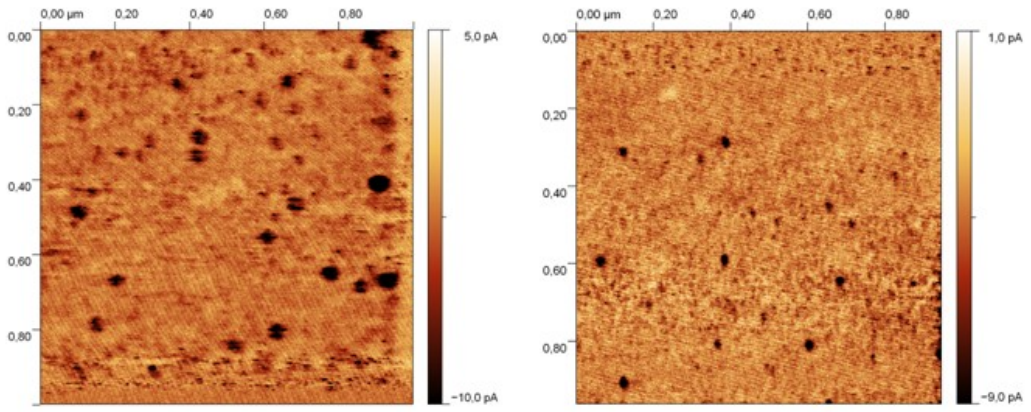


*Figure 3.4: 1 x 1 $\mu m^2$ current images of sample A for an applied voltage of -5.8 V (left) and of sample B for an applied voltage of -7.2V (right).*

From the obtained current images one can notice the importance of the nano-scale electrical characterization compared to the macro-scale using large electrodes. However, if the electrodes were deposited above a region having a high density of hot spots, one cannot determine the real characteristics of the oxide since short circuit may occur between the electrodes and the substrate through the hot spots.

On the other hand, in order to confirm the beneficial influence of atomic O on the electrical behavior of the oxide, nano-scale I-V characteristics of samples A and B are compared. We have determined the I-V characteristics on **16 different regions** of each sample in order to obtain the average value of the threshold voltage $V_{th}$. The applied RVS are from 0 to -10 V (negative polarity on the substrate and positive on the AFM tip) with a speed of 0.5 V/s and a current limit of -80 pA to prevent the complete breakdown of the oxide (which means that the ramp is stopped when the current exceeds -80 pA).

As shown in Figure 3.5, the average value of $V_{th}$ is 5.3 V for sample A and 6 V for sample B with uncertainty of ~ 0.3 V. Considering the fact that the thickness of both samples is almost the same (~ 3.2 nm), we attribute this difference to the deposition ambient which is atomic O for sample B and molecular O for sample A.

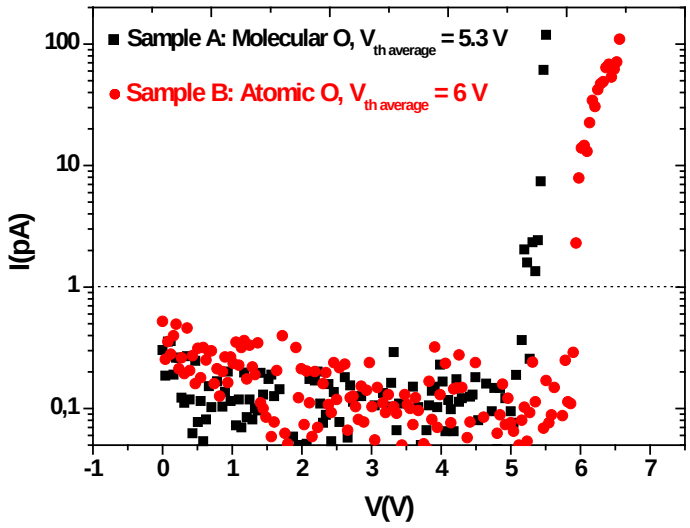


*Figure 3.5: Representative nanoscale I-V characteristics of sample A (black curve) and of sample B (red curve) and the corresponding average values of the threshold voltages (voltage and current are represented in their absolute values).*

Since the $V_{th}$ values for both samples are greater than the LAO barrier height $\Phi_b \approx 2 \pm 0.1$ eV [6], so their I-V characteristics could be fitted to the FN tunneling current represented by the following formula:

$$I_{FN} = A_{eff} \frac{q^2}{8 \pi h \Phi_b} \frac{m_0}{m_{ox}^*} \left(\frac{V_{ox}}{t_{ox}}\right)^2 e^{\left[\frac{-8 \pi \sqrt{q}}{3h} \sqrt{2 m_{ox}^*} \Phi_b^{\frac{3}{2}} \frac{t_{ox}}{V_{ox}}\right]} \quad (3.1)$$

where $A_{eff}$ is considered as the surface of the AFM tip in air, previously determined in section 2.3.3 of Chapter 2 to be ~ 2328 $nm^2$ and $t_{ox} \approx 3.2$ nm. The difficulty was in fitting the values of the barrier height and the effective mass. For sample A, we found a value of $\Phi_b$ of 2.15 eV and that of sample B of 2.47 eV which are considered slightly different from the value found in the literature (2 ± 0.1 eV). The surprising determined parameter was the value of the effective mass which we found to be ≈ 1.5 $m_0$ which is considered completely false. The effective mass of electrons in LAO oxide is found in the literature to be ~ 0.3 $m_0$ [7].

As a result it was very difficult to fit these I-V characteristics with a tunneling model and this may be attributed to the quality of the oxide which is influenced by the presence of a high density of electrically active defects.

We can relate the existence of a leakage current through the LAO oxide films to the oxygen vacancies found in the oxide's volume. Oxygen vacancies are a serious possible problem in high-k oxides. They cause transient trapping and threshold voltage shifts since they can give energy levels near the LAO conduction band and above the Si gap as discussed in [8]. Tse et al. [9] have demonstrated that oxygen vacancies are most consistent with defect levels seen experimentally in high-k oxides by optical, luminescence and charge pumping experiments leading to the conclusion that oxygen vacancies are the main cause of charge trapping. On the other hand, leaky spots may arise from a local thinning of the layer or the pre-existence of defects, like oxygen vacancies, allowing the current to cross the layer more easily [10]. The decrease of the density of leaky spots in the samples having LAO deposited within atomic O ambient might be related to the filling of the oxygen vacancies by the oxygen atoms, hence decreasing their density in the LAO oxide. The current image of sample B in Figure 3.4 confirms this influence, by the decrease of the density of the leaky spots.

#### *3.2.3.2) Influence of the Si surface preparation before the LAO deposition: High-T vs. HF-last procedure*

Figure 3.6 shows the nano-scale I-V characteristics of samples C and D which were subjected to two different Si surface preparations before the LAO deposition within atomic O ambient as discussed in section 3.2.1. Similarly, I-V characteristics have been determined from 16 different zones of each sample in order to calculate the average value $V_{th}$.

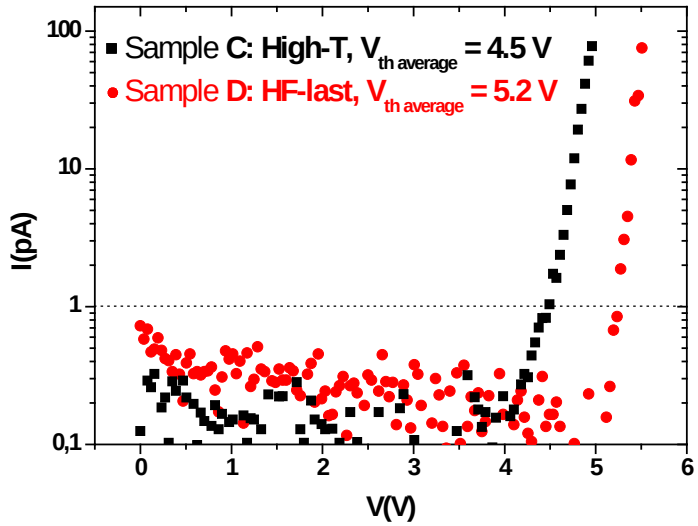


*Figure 3.6: Representative nanoscale I-V characteristics of sample C (black curve) and of sample D (red curve) and the corresponding average values of the threshold voltages (voltage and current are represented in their absolute values).*

As shown in Figure 3.5, the average value of $V_{th}$ is 4.5 V for sample C and 5.2 V for sample D with uncertainty of 0.3 V. Considering the fact that for both samples, the LAO was deposited in the same manner and that their thicknesses are almost the same (~ 3.7 nm), we attribute this difference to the Si surface preparation process before the LAO deposition which is the High-T process for sample C and the HF-last process for sample D. This can be explained by the fact that the annealing step at 900 °C of the High-T process leads to a reaction between the Si substrate and the residual carbon contaminations initially present on the substrate forming holes and SiC dots on the substrate which locally prevents LAO growth hence leading to a degradation of the LAO morphology for High-T sample C as shown in the topographical images of Figure 3.2. On the other hand, for the HF-last sample D, due to the low temperature process, no SiC dots are formed and thus no holes are present in the final LAO layer leading to a better electrical performance of the oxide.

However, modeling of the I-V characteristics of both samples was difficult also as in the case of samples A and B. Fits to FN tunneling current have given abnormal values of $\Phi_b$ (between 2.25 and 2.4 eV) and of $m^*$ (between 0.8 $m_0$ and 1 $m_0$). As discussed before, this may be attributed to the presence of defects in the oxide.

## 3.3) $Gd_2O_3$ thin oxide films

### 3.3.1) *Preparation of the samples*

The GdO films were elaborated by Gang Niu at INL at the Ecole Centrale de Lyon. As mentioned in [11] the GdO films were grown on p-type (111)-oriented Si substrates ($10^{15}$ at.cm$^{-3}$) in a RIBER EVA 32 MBE reactor, with a base pressure ~ 5 x $10^{-10}$ Torr. The samples were prepared using electron beam evaporation of commercial granular GdO target, either under molecular O or under atomic O. The Si substrates were first etched in HF solution, and then oxidized under UV-activated ozone for 2 minutes. This procedure can lead to an atomically flat Si surface protected by 1 nm-thick $SiO_2$. Si substrates were then introduced to MBE chamber and heated up to 800 °C for 20 minutes in order to grow a Si buffer layer whose surface is clean and well-ordered (111) Si. GdO films were then grown at 650 – 720 °C under ultra-high vacuum (~ 5 x $10^{-10}$ Torr) during the first stage to avoid any interface parasitic phase formation. The growth rate is 2 – 3 Å/min. After ~ 1 monolayer growth of GdO, the molecular O pressure was ramped up to 1 x $10^{-6}$ Torr for the "molecular O" samples, while for the "atomic O" samples, GdO was deposited within atomic O ambient produced using a RF-plasma cell. The physical thicknesses of the films were measured by XRR.

We will again present two groups of samples containing a total of six different samples. The **1st group** includes four different samples **A**, **B**, **C** and **D** where for each sample the growth temperature is 650 °C, 680 °C, 700 °C and 720 °C respectively within a molecular O ambient. The four samples have a thickness of approximately 5.5 nm with uncertainty of 0.3 nm.

The **2nd group** contains two other samples **E** and **F**, where for sample E, GdO was deposited within molecular O ambient, while for sample F it was deposited within atomic O ambient. For both samples the growth temperature was 700 °C. Both samples have a thickness of approximately 3 nm with uncertainty of 0.3 nm. Table 3.2 summarizes the essential data of all the samples.

| **GdO** | Samples | | | | | |
|---|---|---|---|---|---|---|
| | 1st Group | | | | 2nd Group | |
| | **A** | **B** | **C** | **D** | **E** | **F** |
| Deposition ambient | Molecular O | Molecular O | Molecular O | Molecular O | Molecular O | Atomic O |
| Growth temperature °C | 650 | 680 | 700 | 720 | 700 | 700 |
| Thickness ± 0.3 nm | 5.5 | 5.5 | 5.5 | 5.5 | 3 | 3 |

*Table 3.2: Deposition characteristics and thicknesses of the GdO samples under study.*

### 3.3.2) *Topographical study of the samples*

Topographies of the six samples using the intermittent contact mode of the AFM are shown in Figure 3.7. These 2 x 2 $\mu m^2$ topography images have been taken using a Si tip oscillating near its resonant frequency ranging from 280 to 320 kHz.

As shown in Figure 3.6, all the GdO samples (A, B, C, E and F) grown at temperatures less than or equal to 700 °C have RMS values between 0.25 nm and 0.38 nm indicating good quality surfaces for current measurements at the nano-scale. However, the surface of sample D where GdO growth temperature was 720 °C represents a relatively rough surface of (RMS roughness of 1.4 nm). As we will present in the next sessions, the samples with a GdO growth temperature of 700 °C and the smoothest surfaces (0.25 nm < RMS < 0.38 nm), represent the best electrical characteristics (lowest leakage currents) with respect to the others, allowing to conclude that 700 °C is the optimal growth temperature of GdO [11].

On the other hand, concerning the humps and holes appearing on the samples' surfaces, they may be explained again by the presence of SiC on the surface as discussed before in section 3.2.2 of the LAO samples.

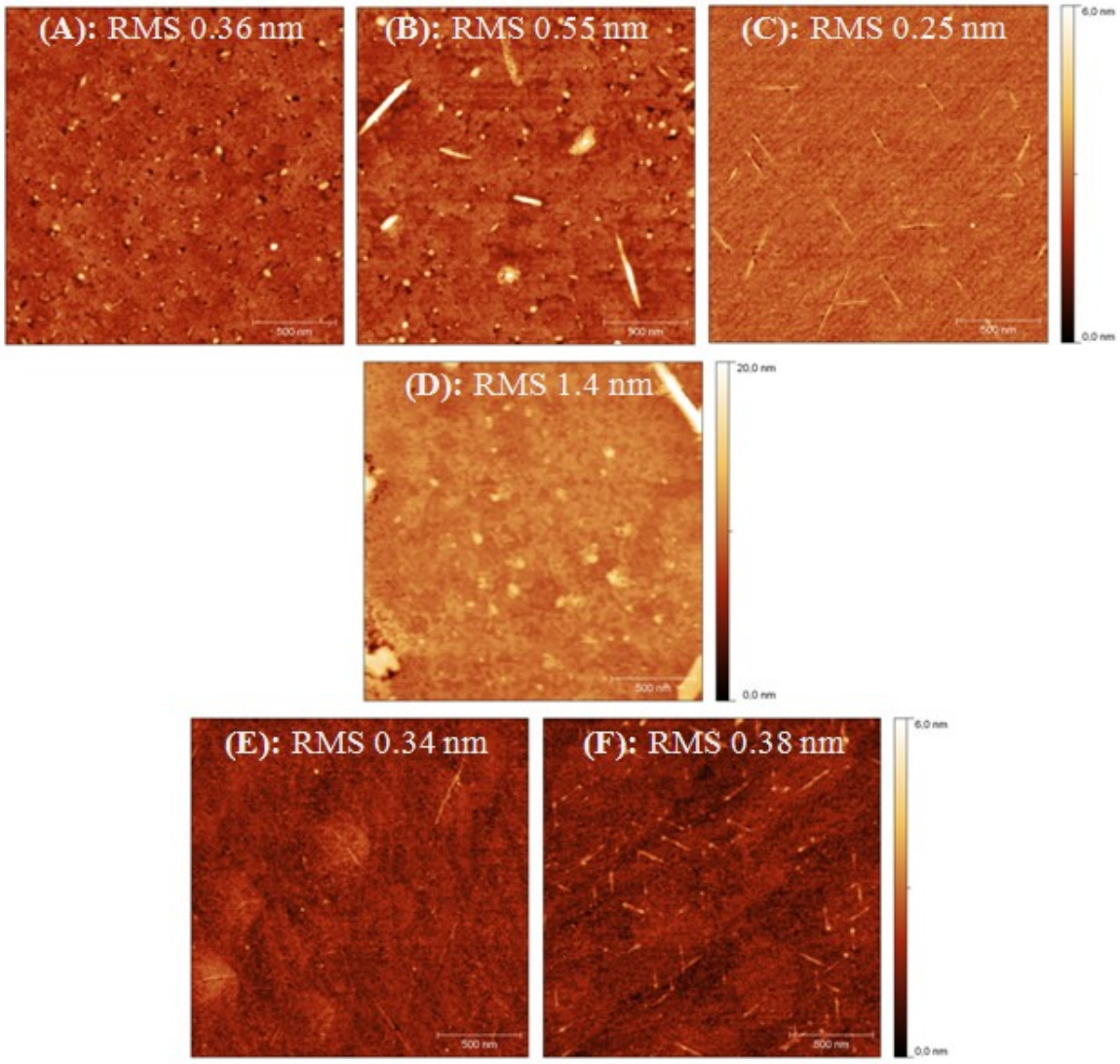


*Figure 3.7: 2 x 2 µm$^2$ topographies of the six GdO samples with their corresponding RMS values. Note that all the images have the same z-scale (6 nm) except that of sample D (20 nm).*

### *3.3.3) Influence of different parameters on the electrical characteristics of the samples*

I-V measurements have been conducted on the six samples in order to study the influence of two different parameters on the electrical characteristics of the samples:

- Influence of the GdO growth temperature: the growth temperatures adopted during the GdO growth varied between 650 and 720 °C, so in order to find the best temperature, I-V characteristics of samples **A**, **B**, **C** and **D** are compared.
- Influence of the deposition ambient: Molecular O vs. Atomic O ambient, comparison between sample **E** and sample **F** is done.

### *3.3.3.1) Influence of the GdO growth temperature*

Macro-scale C-V and J-V characteristics shown in Figure 3.8 were conducted on 100 x 100 µm$^2$ Ni (3 nm) / Au (250 nm) metal electrodes [11]. C-V characteristics indicate low leakage current densities through the samples A, B and C since there is a capacitance in accumulation which is confirmed by the J-V characteristics while for sample D (grown at 720 °C) the leakage current density was too high to measure any C-V characteristics. Moreover, J-V characteristics show good characteristics for sample C (grown at 700 °C) where the measured EOT is 0.7 nm and the leakage current at $|V_g - V_{FB}| = 1V$ is 3.6 x $10^{-2}$ A.cm$^{-2}$ [11]. Hence, the electrical properties of GdO grown at 700 °C are in good agreement with the ITRS recommendations for the 32 nm node ($J < 10^{+2}$A.cm$^{-2}$) [11] where its objective is to ensure cost-effective advancements in the performance of the integrated circuit and the products that employ such devices, thereby continuing the health and success of this industry and removing roadblocks facing the continuation of Moore's law.

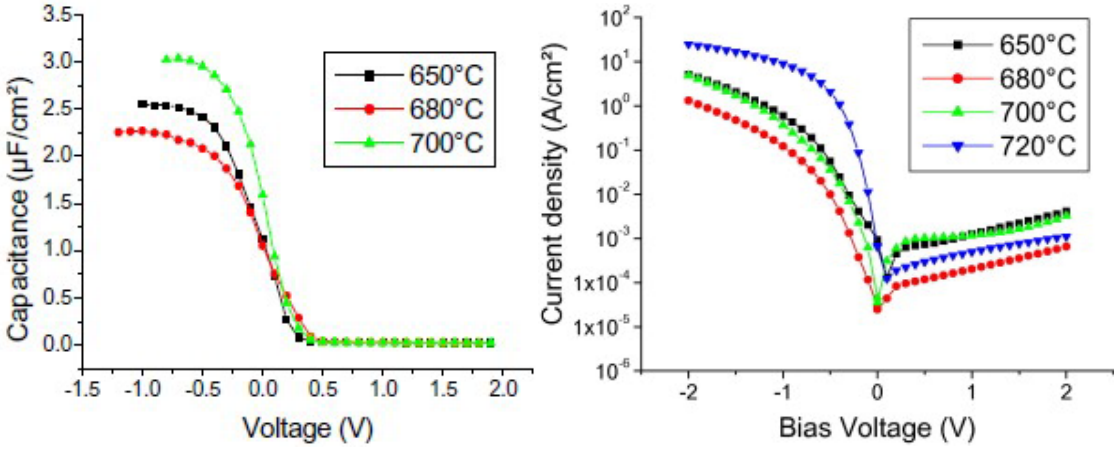


*Figure 3.8: Room temperature C-V measurements at f = 100 kHz (left image) and J-V measurements (right image) for GdO layers grown at different temperatures* [11].

Current images were difficult to obtain for these samples because of the uniform distribution of high leakage currents.

On the other hand and similarly as in the case of LAO, we have determined the nano-scale I-V characteristics on **16 different regions** of each sample in order to obtain the average value of $V_{th}$. The applied RVS are from 0 to -10 V with a speed of 0.5 V/s and a current limit of -80 pA.

I-V characteristics of samples A, B, C and D are compared. As shown in Figure 3.9, the average values of $V_{th}$ are 5 V, 5.8 V, 7 V and 3.7 V for samples A, B, C and D respectively with uncertainty of 0.3 V. Considering the fact that all the samples have the same thickness (~ 5.5 nm), we attribute this difference to the GdO growth temperature.

As the macro-scale measurements, the nano-scale I-V characteristics reveal that the optimal growth temperature of GdO is 700 °C since it shows the highest threshold voltage of 7 V.

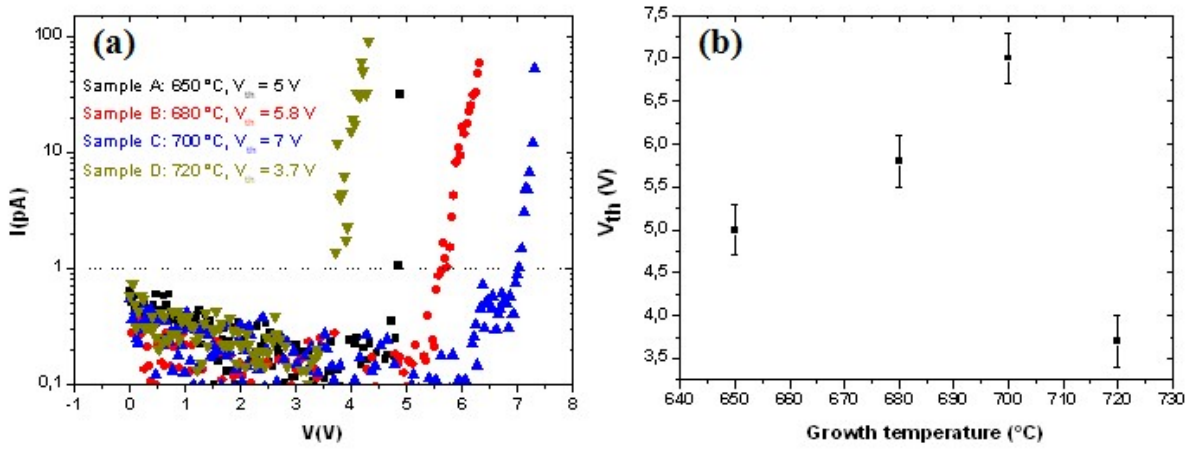


*Figure 3.9: (a) Representative nanoscale I-V characteristics of samples A (black curve), B (red curve), C (blue curve) and D (green curve). (b) The corresponding average values of the threshold voltages (with uncertainty of 0.3 V) in function of the growth temperature.*

### *3.3.3.2) Influence of the deposition ambient: Molecular O vs. Atomic O ambient*

After we have shown by nano-scale and macro-scale electrical characterizations that the optimal growth temperature of GdO is 700 °C, two samples **E** and **F** have been prepared at 700 °C in two different ambient: Molecular O ambient for E and Atomic O ambient for F. 1 x 1 $\mu m^2$ current images of each sample are shown in Figure 3.10. We have increased gradually the value of the applied voltage until dark areas (hot spots) have appeared on the images reaching the value of -7.2 V on sample E with a current scale [-20 pA (dark), 5 pA (bright)] and -6.4 V on F with a current scale [-10 pA (dark), 5 pA (bright)]. These hot spots appeared instantaneously with the passage of the AFM tip on the surface during the first scan and they evolve during the second scan indicating the oxide's degradation after the first one. We can notice that the density of leaky spots (black rounded areas) which are the most conductive regions where the current through the oxide exceeds 120 pA, is smaller in sample F than in sample E demonstrating better dielectric property for sample F where GdO was deposited within atomic O ambient.

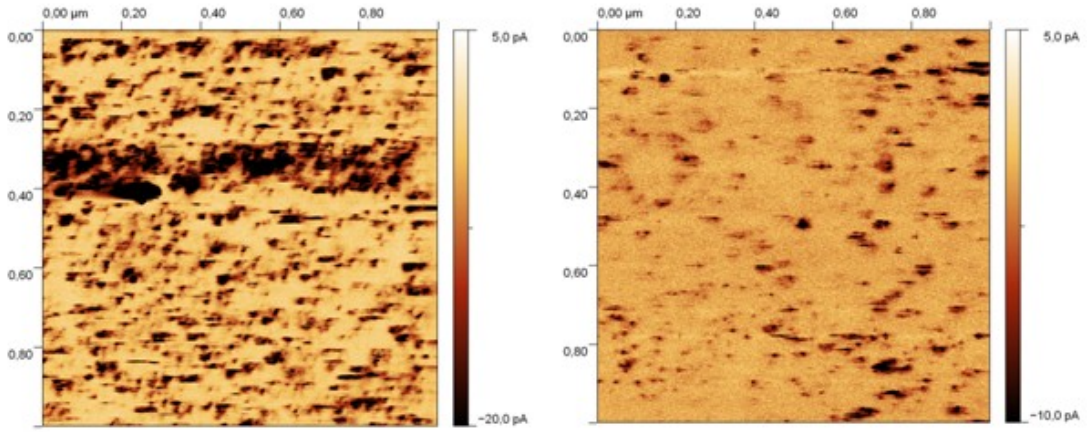


*Figure 3.10: 1 x 1 µm$^2$ current images of sample E for an applied voltage of -7.2 V (left) and of sample F for an applied voltage of -6.4V (right).*

On the other hand, nano-scale I-V characteristics in Figure 3.11 show that the average value of $V_{th}$ is 5 V for sample E and 6 V for sample F. Considering the fact that both samples have approximately the same physical thickness of 3 nm, we attribute this difference to the deposition ambient which is atomic O for sample F and molecular O for sample E.

GdO is one of the high-k oxides whose in their volume oxygen vacancies may exist [9]. Hence, the leakage current through the GdO films can be attributed to these vacancies which play the role of electrically active defects. However, the decrease of the leakage current in the GdO film deposited within atomic O ambient might be related to the filling of the oxygen vacancies by the oxygen atoms, hence decreasing their density in the GdO oxide.

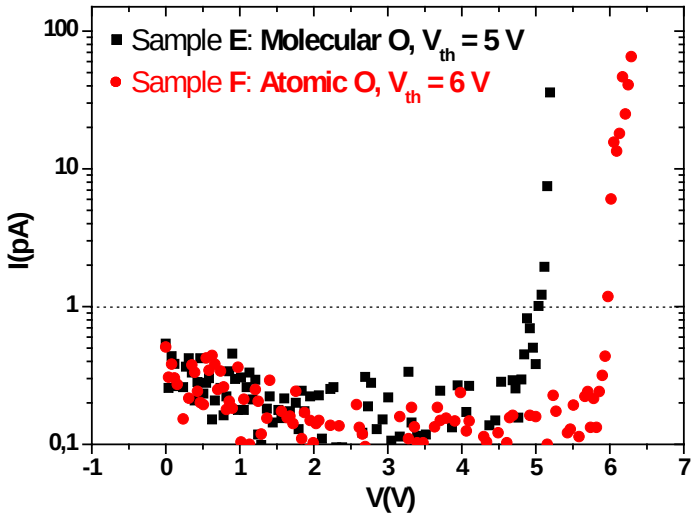


*Figure 3.11: Representative nanoscale I-V characteristics of sample E (black curve) and of sample F (red curve) and the corresponding average values of the threshold voltages (voltage and current are represented in their absolute values).*

Concerning the physical model of the tunneling current through the GdO samples, it was difficult to fit the I-V characteristics with the FN tunneling current as in the case of the LAO samples. The values of the barrier height and the effective mass found to be 2.4 ± 0.3 eV

and 0.9 $m_0$ respectively. These values don't correspond at all to that found in literature where the GdO barrier height is given to be 1.8 eV [12]. This might be also due to the presence of the a high density of electrically active defects in the oxide.

## 3.4) Stress induced surface modification: Appearance of hillocks

After applying the electrical stress by the TUNA on the LAO and GdO samples, the presence of hillocks on the surfaces was observed precisely in the regions where the voltage was applied. Figure 3.12 shows an example of these abnormal hillocks with heights varying from 1 nm to 3 nm on the surface of LAO after conducting the I-V measurements. This is why we have only presented the nano-scale I-V characteristics corresponding to the 1st RVS since the next ones presented very high leakage currents indicating the degradation of the dielectric property of the oxide layers under study.

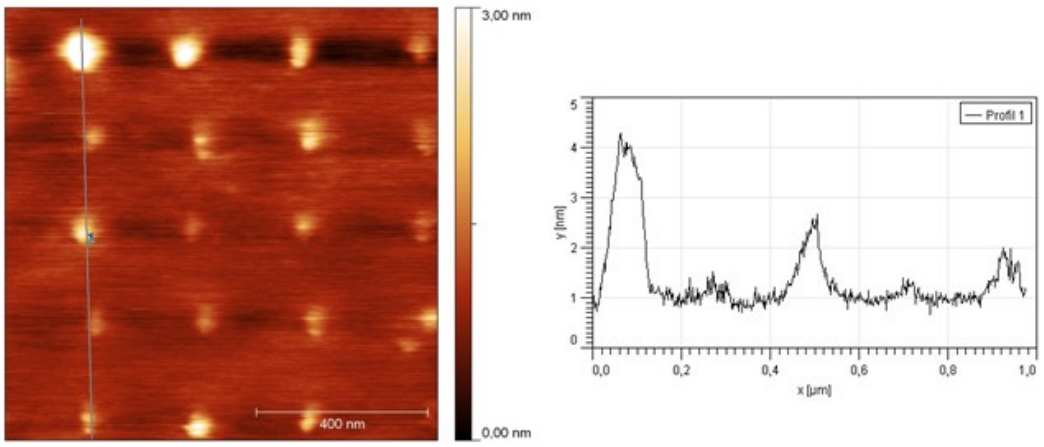


*Figure 3.12: Topography image of the LAO showing the physical modification of the surface after the application of an electrical stress. Right image shows the hillocks' profiles.*

The study of these hillocks has attracted the attention of numerous researchers [13][14][15]. A detailed study of the physical and electrical properties of hillocks will be given in Chapter 4.

## 3.5) Conclusion

In summary, this chapter discussed the electrical characterization at the macro-scale and the nano-scale of thin high-k oxide films of $LaAlO_3$ and $Gd_2O_3$ elaborated at the INL. We have shown the importance of the nano-scale electrical characterization compared to that at the macro-scale. Indeed, current images performed by the TUNA permits observing the hot spots (leaky spots) in the oxide layers which cannot be seen in macro-scale measurements where large electrodes are deposited and short circuits could be formed between them and the substrate through these hot spots. Moreover, different deposition parameters have been studied: Molecular O vs. Atomic O ambient for LAO and GdO, High-T and HF-last Si surface preparation processes before the deposition of LAO, and the growth temperature of GdO. The influence of these parameters on the electrical properties of LAO and GdO oxide films has been studied at the nano-scale using the TUNA mode AFM. In combination with macroscopic measurements, we have shown that the deposition of these high-k oxides within atomic O ambient enhances their electrical properties compared to the molecular O ambient. We have presented a comparison between the HF-last and High-T processes for the Si surface preparation before the LAO deposition and we have shown that the first process has given cleaner and smoother surfaces with no SiC leading to better electrical results. On the other hand, the electrical characteristics of GdO have shown that its optimal growth temperature is at 700 °C as was also demonstrated by the macroscopic electrical measurements. Finally, as in the case of the $SiO_2$ oxide, the hillocks appear on the LAO and GdO surfaces after the application of a voltage stress through the AFM tip; this case will be more physically and electrically studied in Chapter 4.

## 3.6) References

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# CHAPTER 4 - $SiO_2$ thin oxide films

## Content

## 4.1) Study of the physical and electrical reliability of thin oxide films

### *4.1.1) Introduction: abnormal phenomena occurring during ramped voltage stress*

Application of a positive voltage on the substrate and negative on the AFM tip leads to the oxidation of the Si at the $Si/SiO_2$ interface [1][2][3] leading to the normal inflation of the oxide's surface (creation of a hillock). This oxidation takes place because of the existence of a water layer on the oxide's surface in air ambient. The application of a negative voltage on the AFM tip leads to the injection of $HO^-$ ions through the oxide resulting in the oxidation of the Si at the $Si/SiO_2$ interface. A schematic of the oxidation phenomenon is presented in Figure 4.1.

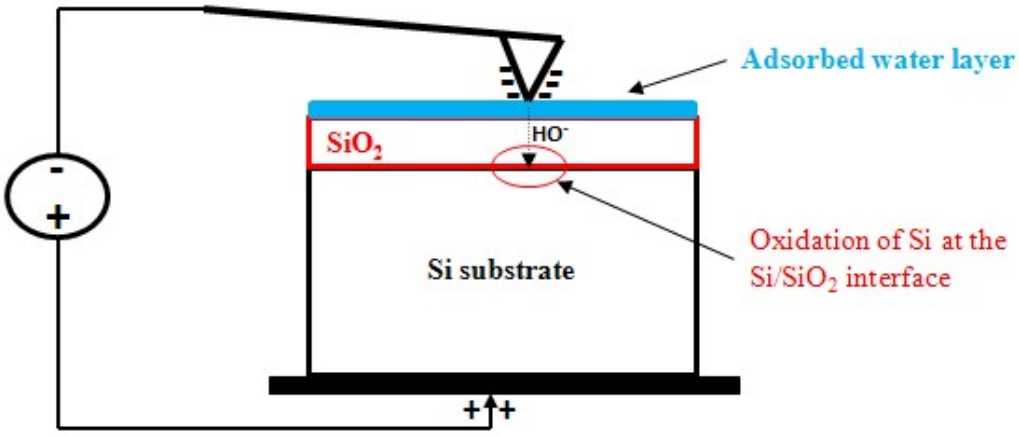


*Figure 4.1: Schematic representation of the injection of $HO^-$ ions through the oxide by applying a negative voltage on the AFM tip.*

In the contrary, the application of an inverse polarity voltage that is negative on the substrate and positive on the AFM tip normally doesn't oxidize the Si at the interface. However, abnormal hillocks were observed on the oxide's surface after this procedure, as illustrated in Figure 4.2 and as we have already seen in the case of high-k oxides in the previous chapter.

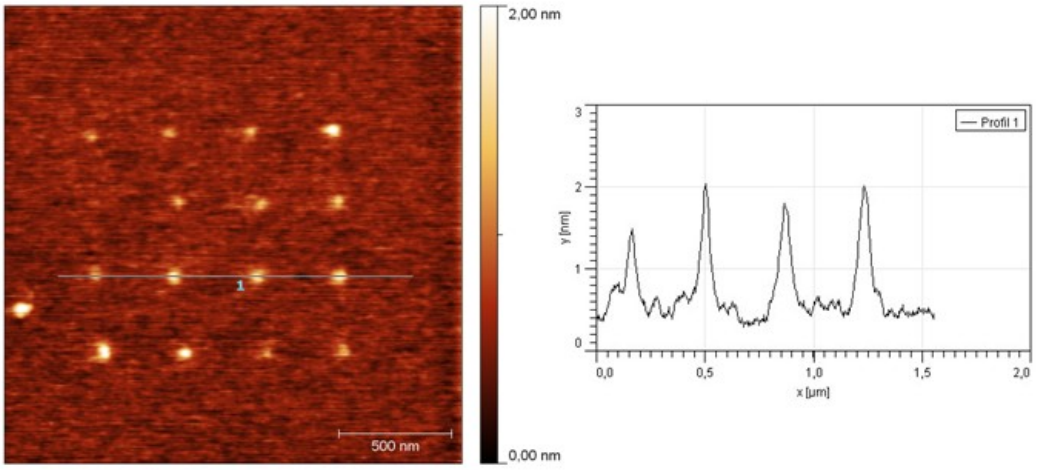


*Figure 4.2: 2 x 2 µm$^2$ topography image showing 16 abnormal hillocks created after applying a negative voltage on the substrate and positive on the AFM tip on 16 different places of the oxide. Right image shows the profiles of the created hillocks.*

Experiments have been conducted on a 2 nm thick thermal $SiO_2$ oxide grown at 1000 °C on an n-type Si substrate ($10^{15}$ at.cm$^{-3}$). RVS have been applied on this sample with the AFM tip as the top electrode in air. A current limit of 100 pA has been used in some cases (mentioned in the text) in order to avoid the complete breakdown of the oxide due to the injection of too important current through the oxide. Corresponding I-V characteristics are presented on Figure 4.3. The stress has been applied from 0 to -10 V with a ramp speed of 0.5 V/sec to reduce the displacement current that is proportional to the ramp speed. The curves are represented with the absolute values of the voltage and the current. Here, we define the threshold voltage $V_{th}$ as the voltage at which the current through the oxide reaches -1 pA, a value that can be precisely measured.

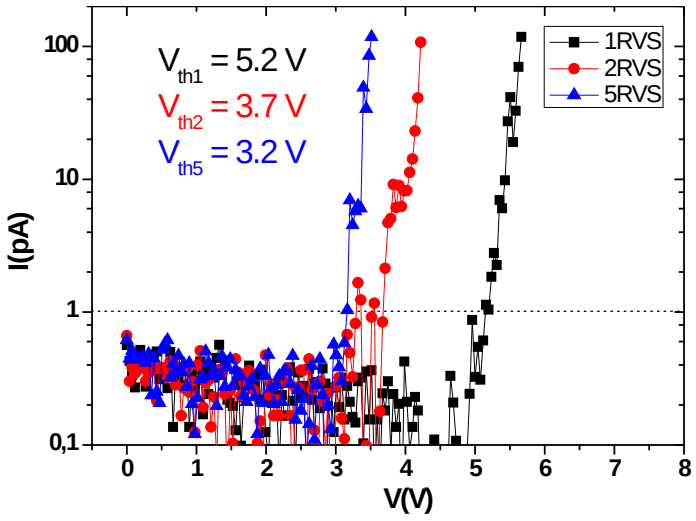


*Figure 4.3: The first five I-V characteristics in air of the 2 nm $SiO_2$ oxide film.*

In the case of our sample, $V_{th}$ is 5.2V at the 1st RVS and then decreases down towards lower voltages to 3.2 V for the 5th RVS. This decrease has been explained in the literature by the activation of defects generated in the oxide that helps the tunneling of charges through the oxide leading to the presence of the TAT (explained in section 1.1.4 of Chapter 1).

After applying the electrical stress, the presence of a hillock in the middle of the topography image was observed with a height of about 4 nm and a diameter of 100 nm (Figure 4.4). The height of the hillock varies depending on different parameters which will be discussed in the following sections.

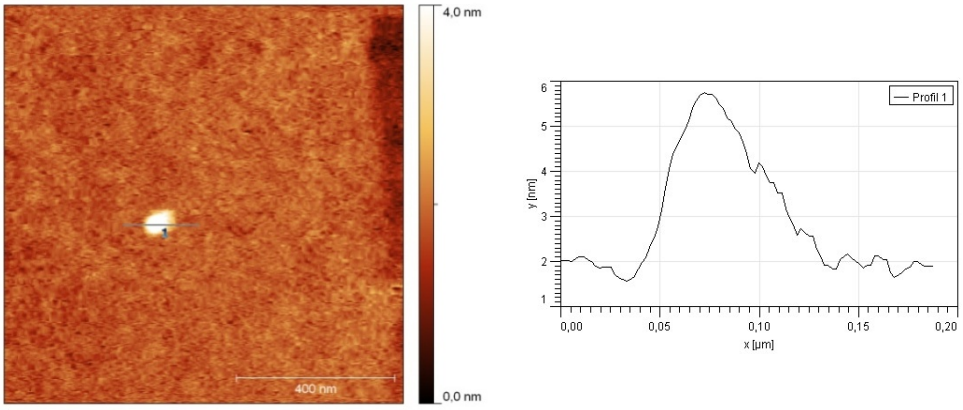


*Figure 4.4: 1x1 µm² topography image of the $SiO_2$ surface after the electrical stress (left) and the profile of the hillock (right) created at the middle of the topography image.*

Studies have shown that at the nanoscale, the degradation of oxides occurs at two different levels:

- The electrical level: a high leakage current flowing through the oxide is detected after the application of an electrical stress [4].
- The physical level: appearance of abnormal hillocks on the oxide's surface is evidenced by topography images using the AFM [4-7].

In this chapter we study this phenomenon on the well-known classical gate oxide, the $SiO_2$ oxide. In other words, we present studies on the physical and electrical degradation of thin $SiO_2$ oxide films subjected to electrical stress on different surrounding ambient in order to find the more reliable conditions for the nano-scale electrical measurements.

### *4.1.2) Study of the physical nature of the hillock by different AFM scanning modes*

The presence of hillocks created at the surface of the oxide after the application of a repetitive RVS can have different origins:

- The local oxidation of the Si-oxide interface leading to a local increase of the thickness of the oxide. Polspoel et al. [2] have shown that the created protrusions and holes due to a negative substrate voltage consist of oxidized Si. Transmission electron microscopy (TEM) image of Figure 4.5(a) shows a local protrusion that was produced during a constant voltage stress ($V_{substrate}$ = -5 V, $t_{stress}$ = 10 s) measurement on a sample with n-type Si substrate covered with a 2.6±0.1 nm $SiO_2$ layer. The protrusion consists of a depression in the Si. This depression is covered with oxidized Si as revealed by the electron energy loss spectroscopy (EELS) O signal of Figure 4.5(b). For this protrusion, the penetration of the oxidized Si into the substrate was 12 nm [2].

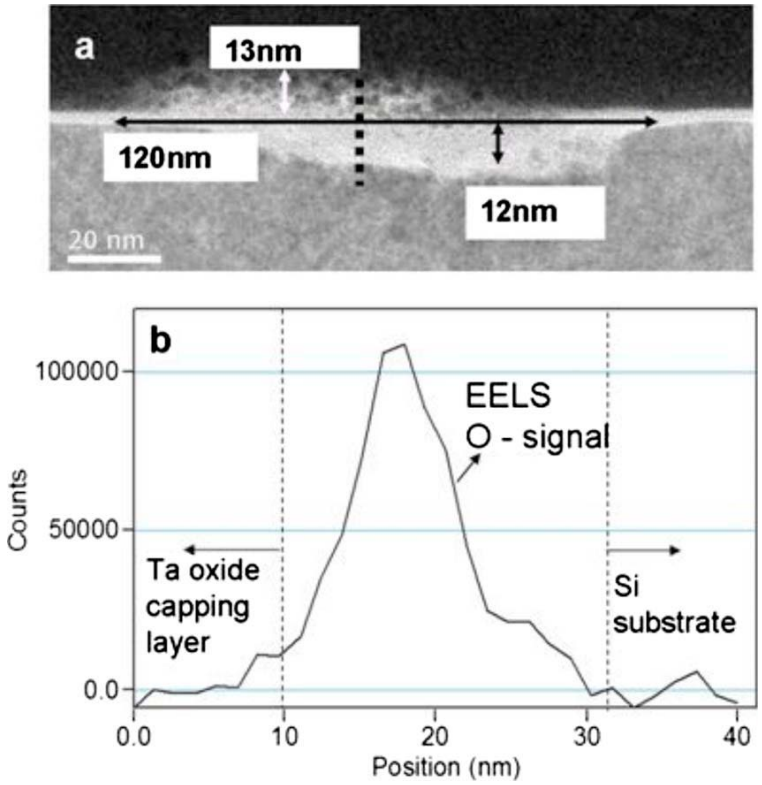


*Figure 4.5: (a) Cross-section TEM image of a protrusion. (b) EELS measurements in the section depicted by the black dotted line in (a). The O signal clearly indicates the formation of oxidized Si inside the protrusion [2].*

- The negatively charged defects introduced by the RVS which help the charges to pass through the oxide causing an electro-thermal effect and playing an important role in

the breakdown triggering as has been shown by Zhang et al. [5]. Figure 4.6 shows this mechanism. Zhang et al. have shown that Si deformation occurs prior to the breakdown transient and hastens it. Hence, the topographical hillock increases in height during the breakdown evolution of 5±0.1 nm $SiO_2$ oxide on an n-type Si substrate which was subjected to a negative voltage stress in a vacuum ambient (< 5 x $10^{-3}$ Pa).

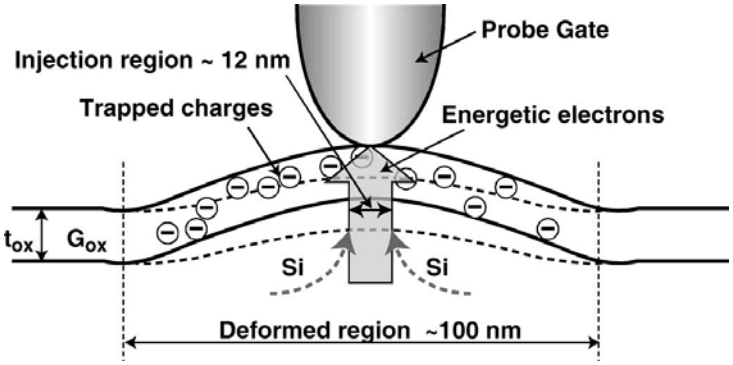


*Figure 4.6: Mechanism diagram of breakdown evolution* [5].

- Porti et al. [8] have claimed that these hillocks do not correspond at all to real modifications of the oxide surface but are the consequence of the electrostatic interactions between the tip and the negative charges induced in the oxide during the breakdown event. They have used the Kelvin probe force microscope (KPFM) which measures, simultaneously with the topography, the contact potential difference (CPD) of the structure by applying to the substrate the required bias to cancel the electrostatic force between the tip and the sample at the measuring location. As a result, they have shown that the height of the hillock depends of the applied voltage, hence influenced by the trapped charges inside the oxide. Figure 4.7 shows the results obtained on a 4.2 nm SiO2 oxide broken down by an electrical stress. Figure 4.7(a) and (b) show the topography (hillock's height ≈ 17.5 nm) and the current image (leakage current ≈ 25 nA) respectively measured with the C-AFM in contact mode. Figure 4.7(c) and (d) show the topography and the CPD image respectively taken with the AFM operated as KPFM. The CPD is 0.4 V smaller at the breakdown location suggesting the presence of negative charges. Figure 4.7 (e) and (f) correspond to the topography of the same spot measured with the AFM in non-contact mode with a bias of 0 and 3.4 V respectively was applied to the sample. Height differences are 37 nm for (e) and 55 nm for (f). In summary, Porti et al. have concluded that the topography features are the consequence of electrostatic interactions between the breakdown induced negative charges and the conductive tip.

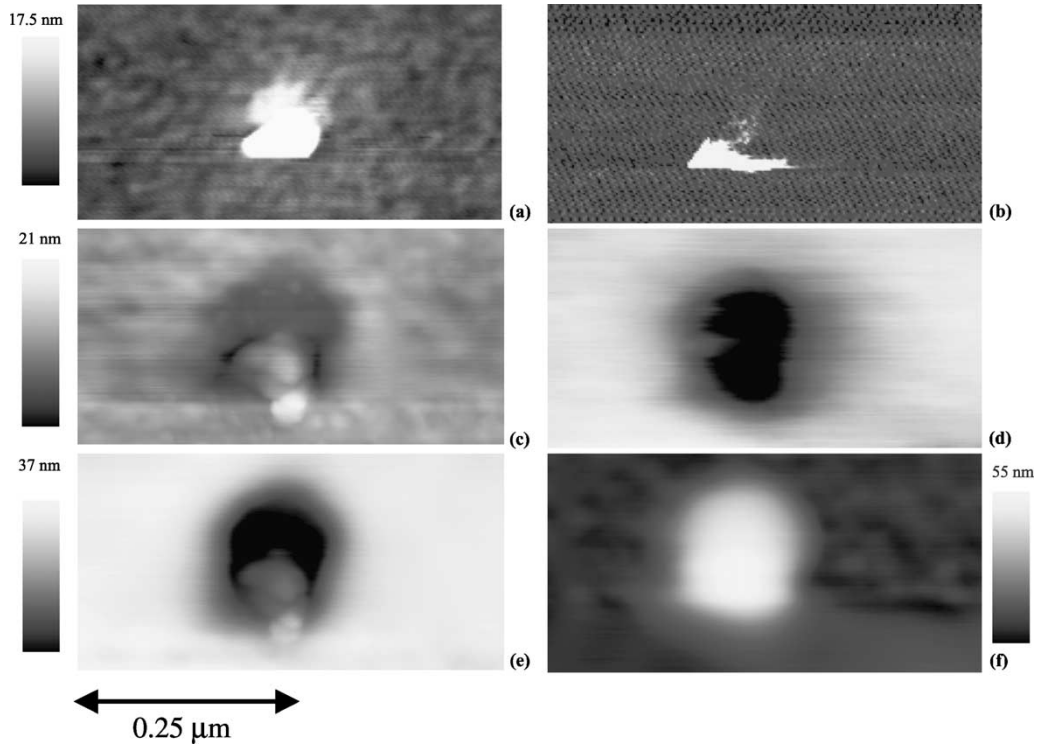


*Figure 4.7: AFM analysis of the breakdown spot induced on 4.2 nm $SiO_2$ oxide [8]. (a) Topography and (b) current images measured with C-AFM. (c) Topography image of the same spot taken with the AFM operated as KPFM. (d) The CPD map. (e) and (f) correspond to the topography of the same spot measured with the AFM operated in non-contact mode, when bias of 0 and 3.4 V, respectively, was applied to the sample.*

The choice between these hypotheses will seriously influence the interpretation of local RVS, in particular if the hillock is entirely an artifact due to the measurements with an AFM. That's why we conducted further experiments which will help to better understand the exact nature of the hillocks.

If the hillock is an artifact due to the AFM operation mode, its physical features (height, width) must be influenced by the mode chosen to obtain the topographical images of the hillocks, and in particular by the choice of a conductive or insulating tip, or by the tip-sample distance since the balance between electrostatic forces and Van der Waals interaction responsible for the topographical contrast in AFM varies strongly with the tip-sample distance [9]. That's why different types of AFM tips have been used (conductive $PtIr_5$ and non-conductive $Si_3N_4$ AFM tips) and 3 different AFM modes have been applied (contact, intermittent-contact and double pass intermittent-contact) to scan the same region where the hillock was previously created. In intermittent-contact (tapping) mode the tip scans the surface area while oscillating near its resonant frequency, ranging from 280 kHz to 320 kHz. In air, the feedback signal is the amplitude of vibration: the higher the value of the feedback, the higher the tip-surface distance. The tips used for this AFM mode were made of silicon.

Before analyzing the experiment, it has to be mentioned that all the results presented here are reproducible and correspond to average values extracted from statistical studies.

First step was to create a mark on the surface of the oxide in order to find the same zone after the change of the scanning mode. This step is done by the application of negative voltage on the AFM tip in order to intentionally grow an additional oxide which delimitates a zone where a hillock will be subsequently created as in the local anodization process [1]. To do so, we have applied RVS from 9 to 10 V with a 0.02 V/sec ramp speed on 12 different zones (6 at the top and 6 at the bottom of the topography image). The topography image representing the oxidized zone is shown in Figure 4.8.

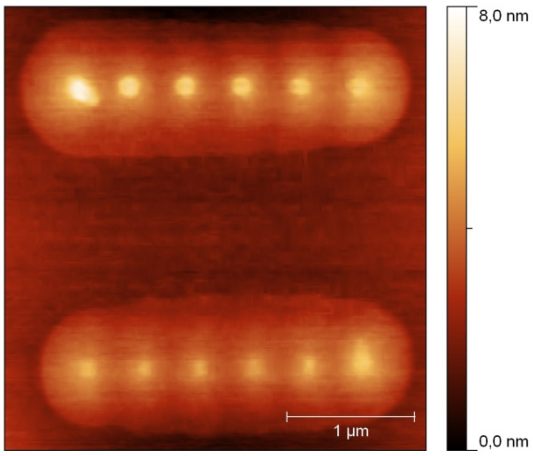


*Figure 4.8: Topography image in contact mode AFM representing the 12 hillocks created on the surface of a 2 nm $SiO_2$ oxide film after a voluntary oxidation.*

The second step was the application of negative voltage on the substrate and positive on the AFM tip. The RVS applied was from 0 to -10 V with ramp speed of 0.5 V/sec. By doing so, there should be no oxidation of the layer and no hillocks should be created. However, a hillock of ≈ **16 nm** in height and of ≈ 150 nm diameter was indeed created at the middle of the topography image taken with AFM in contact mode using a conductive $PtIr_5$ tip as shown in Figure 4.9.

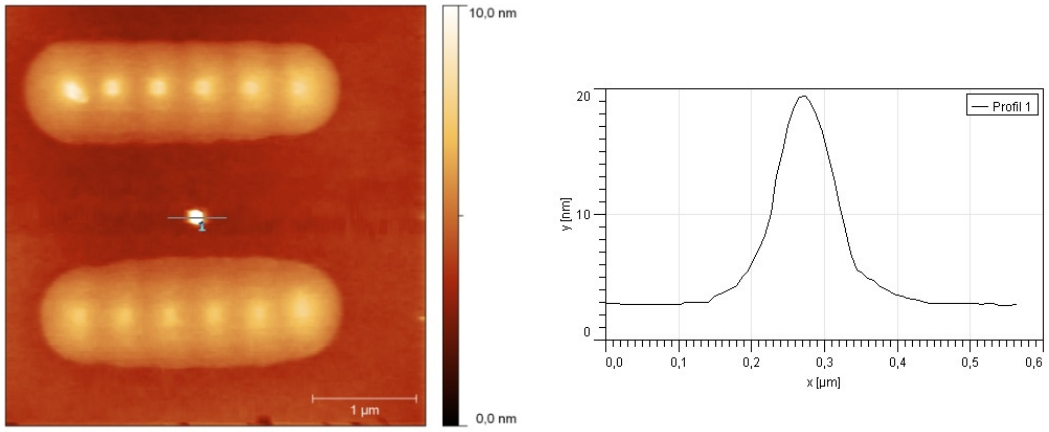


*Figure 4.9: 4x4 µm² topography image in contact mode AFM using a $PtIr_5$ silicon coated AFM tip representing the hillock (left) created on the surface of the 2 nm $SiO_2$ after the application of negative voltage on the substrate and its corresponding profile (right).*

In a second step, the surface was scanned in tapping mode where the influence of the distance between the oxide's surface and the AFM tip on the measured hillock's height can be studied by varying the set-point. Figure 4.10 shows the resulting topography images with the corresponding hillocks' profiles. For the topography (Figure 4.10, left) the AFM tip was oscillating near the surface with a low set-point corresponding to a relatively small tip - sample distance, in order that the electrostatic force arising from trapped charges is less predominant on Van der Waals forces which are responsible for the topographic contrast. In these conditions, the measured hillock's height is ≈ **18 nm** almost the same as that obtained in contact mode using $PtIr_5$ AFM tip. For the right topography image the AFM tip was oscillating further from the oxide's surface where the electrostatic forces should play a more important role. The influence of the electrostatic interaction leads to a measured hillock's height of ≈ **13 nm**, which must be compared to the previously measured 18 nm obtained with a smaller set-point. The difference may be attributed to the electrostatic interaction felt by the AFM tip when the tip - sample distance is increased, which tends to modify the apparent height of the hillock by adding an attractive force on the tip. This behavior is similar to that discussed by Porti et al. [8]. This can be explained as follows: when oscillating near the surface, the tip oscillates with constant amplitude and when it passes above the hillock, the surface-AFM tip distance increases keeping the same oscillation amplitude. On the other hand, during oscillation with a larger surface-AFM tip distance and when passing above the "hillock", the tip is subjected to electrostatic attractive forces causing it to become nearer to the surface in order to find the Van der Waals forces and leading to a less height "hillock". For more details on the intermittent contact mode AFM procedure, see section 2.2 of Chapter 2.

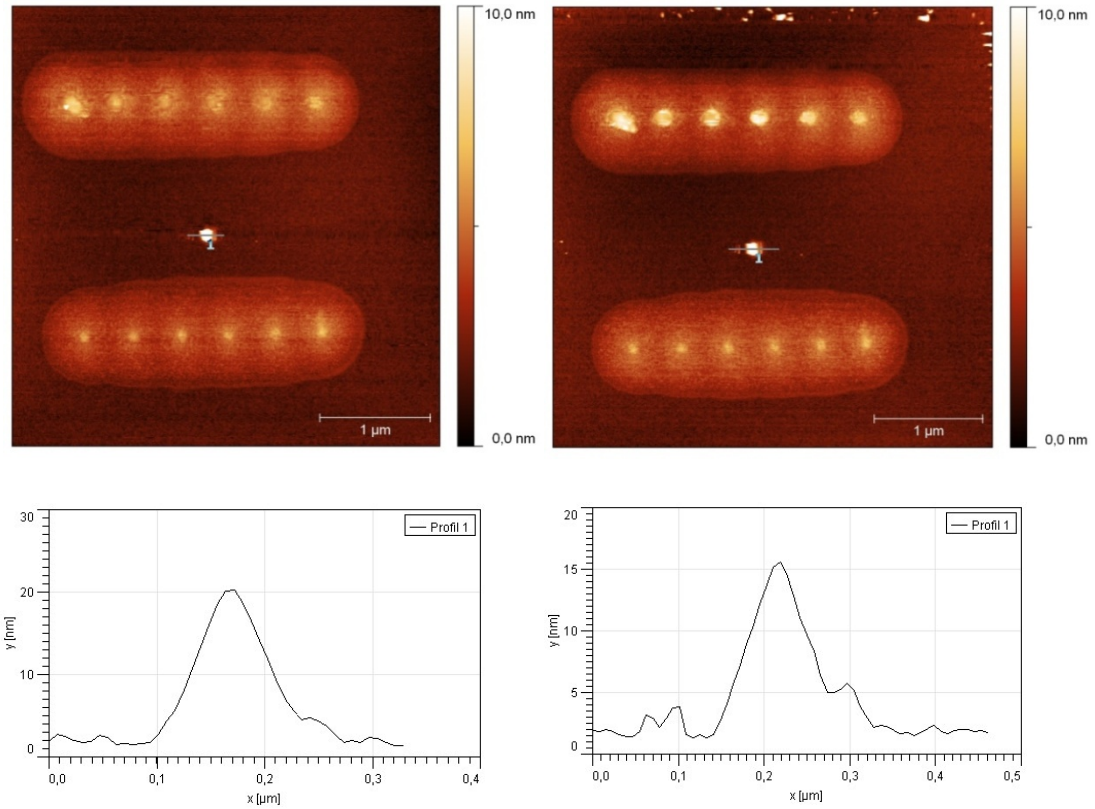


*Figure 4.10: 4x4 µm$^2$ topography images in tapping mode AFM using a silicon tip oscillating near to the surface (left) and far from the surface (right) and the corresponding hillocks' profiles (bottom).*

To study the influence of the long range electrostatic Coulomb forces between the conductive AFM tip and the surface of the sample, a topography image has been recorded in contact mode using a non-conductive $Si_3N_4$ AFM tip. In contact mode the short range Van der Waals forces are predominant compared to Coulomb forces. This means that the contrast on the image should mostly arise from true topographical features. Figure 4.11 shows the topographic image using these conditions, where a hillock of ≈ **24 nm** height is present. This result tends to confirm the hypothesis that the hillock is a real morphological modification of the oxide surface since in this case the height of the hillock does not depend on the conductive nature of the tip.

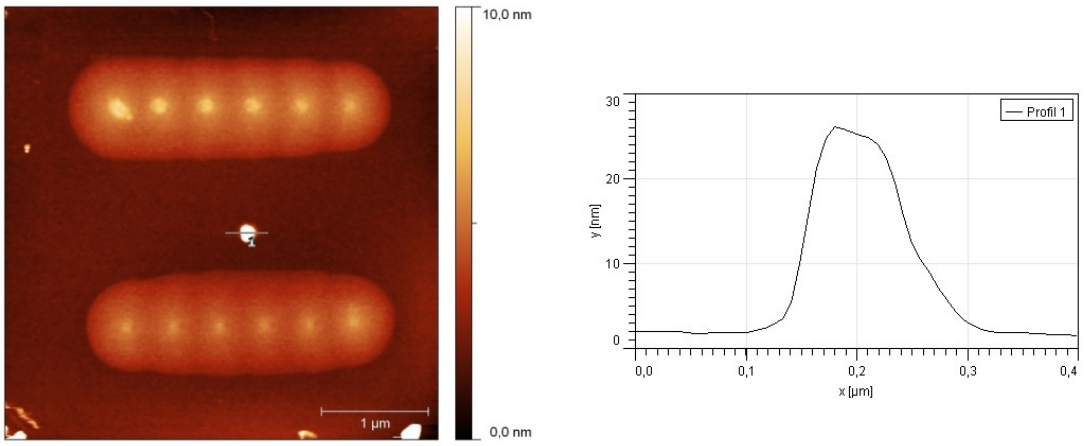


*Figure 4.11: 4x4 µm² topography image in contact mode AFM using a non-conductive $Si_3N_4$ AFM tip (left) created on the surface of the 2 nm $SiO_2$ and the corresponding hillock's profile (right).*

The use of three different operating modes (contact mode with conductive AFM tip, tapping mode, and contact mode with non-conductive AFM tip) results in different measured hillock's height (see Table 4.1). This suggests that the hillock detected by the AFM after the application of an electrical stress is a real morphological modification of the oxide's surface (inflation of the surface) and its different measured heights are due to the influence of the electrostatic forces between the trapped charges in the oxide and the AFM tip.

| Contact mode | | | Intermittent-contact mode | | |
|---|---|---|---|---|---|
| AFM tip type | Conductive $PtIr_5$ | Non-conductive $Si_3N_4$ | Tip-sample distance | small | large |
| Hillock's height (nm) | **16** | **24** | Hillock's height (nm) | **18** | **13** |

*Table 4.1: Hillock's height in function of the AFM scanning mode, AFM tip type and the tip-sample distance.*

To evaluate further the role of trapped charges on the measured contrast, we have used Electric Force Microscope (EFM).

The EFM image shown in Figure 4.12, measured on our $SiO_2$ surface represents the phase detection mode with a tip bias of -2 V, after a RVS from 0 to -10 V with a ramp speed of 0.5 V/sec has been applied. The lift height is 30 nm (slightly greater than the hillock height). The represented EFM image was recorded 24 hours after the application of the electrical stress and the creation of the hillock to ensure that all the charges present on the surface of the sample had time to flow away.

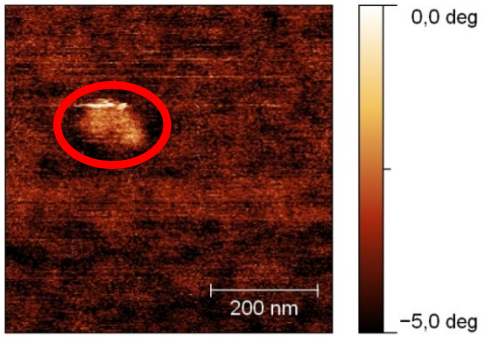


*Figure 4.12: Phase detection EFM lift mode images with a lift height 30 nm and tip bias of -2 V.*

We notice that the contrast over the hillock is different from its surrounding area showing a hump which indicates that there is a repulsive force between the negatively biased tip and the surface, indicating the existence of negative trapped charges inside the hillock. Indeed, injection of charges through the oxides has been largely studied by R. Dianoux [9] who had injected and detected charges in oxides by the AFM.

As a conclusion of all the results obtained using different modes of scan, we postulate that the hillock created after the application of an electrical stress over the surface of $SiO_2$ oxide is caused by two phenomena: **the real morphological modification** of the oxide (demonstrated by the contact mode scan using non-conductive $Si_3N_4$ AFM tip) and **the electrostatic interaction phenomenon** between the trapped charges in the oxide and the AFM tip (demonstrated by the tapping mode and the EFM lift mode scans).

The next section will be dedicated to a further understanding of the origin of this hillock by the study of several experimental conditions that influence its apparition.

#### *4.1.2.1) Study of the influence of different parameters on the height of the hillock*

- *Influence of the time of stress in air of 30 % humidity and in nitrogen ambient of 2.5 % humidity*

In this study, the experiments were performed in air with 30 % humidity and RVS ranging from 0 to -10 V without any current compliance. Figure 4.13 (black squares symbol curve) shows the height of the hillock as a function of the duration of the applied electrical stress in air. The hillocks height decreases from 30 nm to 23 nm for a stress time of 50 sec and 10 sec respectively, and it remains constant at 23 nm for the lower stress durations (5 and 2 sec). In air, the stress time doesn't have a great influence on the hillock's height, where it slightly varies from 23 nm to 30 nm.

The same experiment is performed in a closed nitrogen ambient chamber using NTEGRA AFM platform, with 2.5 % relative humidity inside the AFM chamber. Figure 4.13

(red circles symbol curve) shows the hillock's height as a function of the electrical stress time. At this low humidity level, the water meniscus, created when the tip enters the water layer present on the surface, is reduced and probably not entirely removed. This influences the height of the hillock compared to that obtained in air ambient. Compared to the experiment done in air, for short times of stress there is almost no hillock created on the oxide's surface. In the contrary, for 50 sec of stress, the hillock's height is 30 nm in air and in nitrogen ambient. For this time of stress the 2 nm thick oxide is totally damaged in both surroundings. We proposed the following interpretation of the phenomenon: in air ambient because of the higher presence of the water layer on the oxide's surface, high densities of $HO^-$ pass through the Si substrate causing the oxidation of the Si at the $Si/SiO_2$ interface from the beginning of the stress (2 sec) till the end (50 sec) where the oxidation reaches its maximum. On the other hand, in nitrogen ambient, since the water layer on the surface is highly reduced, lower densities of $HO^-$ are injected at the beginning of the stress reaching the same density as that in air but after 50 sec of the electrical stress.

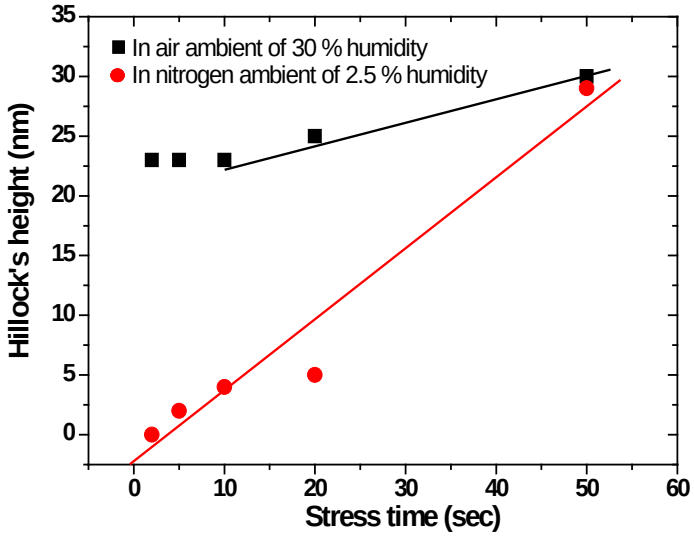


*Figure 4.13: Hillock's height in function of the stress time applied. Studies are performed in air ambient of 30 % humidity (square symbol curve) and in nitrogen ambient of 2.5 % humidity (circle symbol curve).*

Our conclusion is that, in nitrogen ambient the electro-thermal effect is the cause of the surface inflation since almost no water layer at this level of humidity. This mechanism will be explained in detail further.

➢ *Influence of the current limit in air of 30 % humidity*

In order to study the influence of the current limit, RVS were applied from 0 to – 10 V with 0.2 V/sec ramp speed and with different current limits. The current limit aims at preventing the complete degradation of the oxide. Figure 4.14 summarizes the results: the height of the hillocks is far lower with the current limit, leading to the conclusion that the existence of the hillocks depends on the quantity of current flowing through the oxide. Hence, this is the importance of the current limit in decreasing the creation of hillocks and this is why the hillocks height in the preceding experiment done in air ambient varied from 23 nm to 30 nm when no current limit was used.

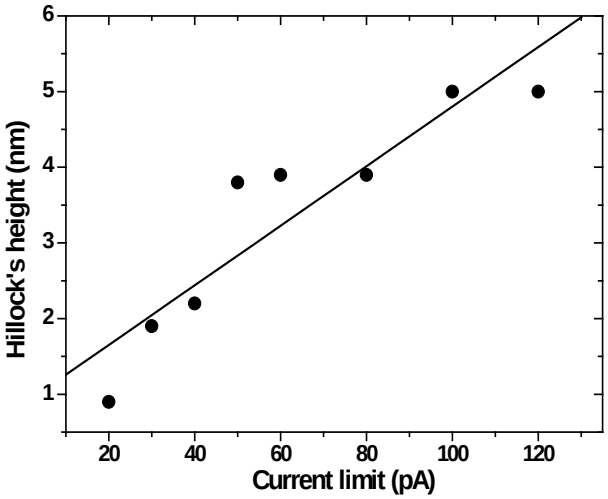


*Figure 4.14: Hillock's height in function of the current limit applied. This study is performed in air of 30 % humidity.*

The quantity of charges Q (in Coulombs) passing through the oxide is calculated from the I-V curves by performing the integration of the current I as a function of the applied voltage V:

$$\mathbf{Q = \frac{1}{v} \int_{V_1}^{V_2} I\, dV} \qquad \mathbf{(4.1)}$$

where v is the ramp speed (0.2 V/sec), $V_1$ and $V_2$ are the voltage boundaries of the I-V curve such that $V_1$ = 0 and $V_2$ = 10 V. Q as a function of the different current limits used is presented the bar graph of Figure 4.15 for both the forward (from 0 to -10 V) and the backward (from -10 V to 0) ramps. This graph shows that the quantity of charges traversing the oxide increases (from $0.6 \times 10^{-11}$ C to $38 \times 10^{-11}$ C) when the current limit is high and after the 1st RVS (the backward I-V) indicating the formation of a path of traps that helps the tunneling of the injected charges through the oxide; this is a characteristic behavior when TAT takes place.

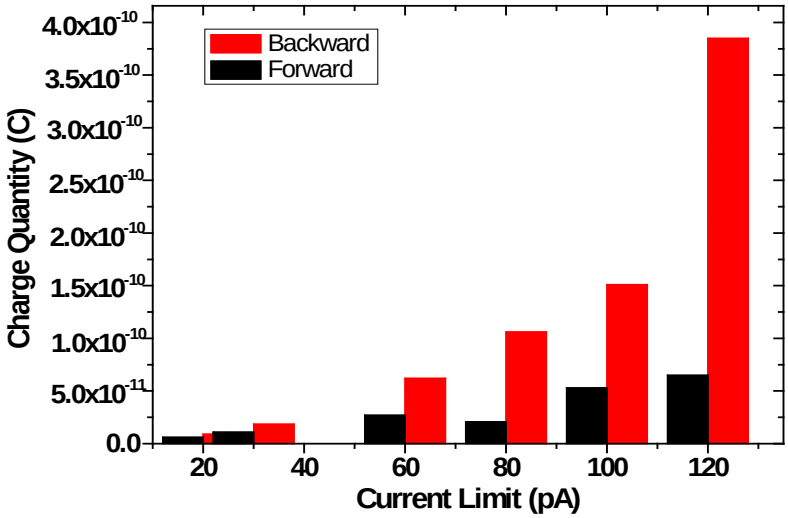


*Figure 4.15: The quantity of charges Q in function of the current limit for both the extended and the retracted RVS.*

#### *4.1.2.2) Study of the conductivity of the hillocks*

I-V characteristics have been studied as a function of the number of RVS. Figure 4.16 (left) shows the corresponding characteristics where RVS were applied from 0 to -10 V with a speed of 0.5 V/sec and a current limit of -100 pA. The oscillation of the threshold voltage $V_{th}$ as a function of the number of RVS is shown in Figure 4.16 (right). $V_{th}$ = 5 V for the 1$^{st}$ RVS and then it decreases down to 0.85 V for the 3$^{rd}$ RVS. This can be explained by the creation of defects inside the $SiO_2$ oxide which help the displacement of charges flowing through it (TAT). At the 7$^{th}$ RVS, the $V_{th}$ value increases again: from 1.3 V (7$^{th}$ RVS) up to 4.5 V (14$^{th}$ RVS). We attribute this behavior to the oxidation of the Si substrate at the $Si/SiO_2$ interface, leading to the increase of the oxide's thickness. As the oxide grows, the number of defects created inside it reaches a maximum (critical) value [10]. That's why from the 8$^{th}$ RVS $V_{th}$ is almost constant at a value of 4.5 V, corresponding to the passage of charges through a thick oxide containing a maximum number of defects.

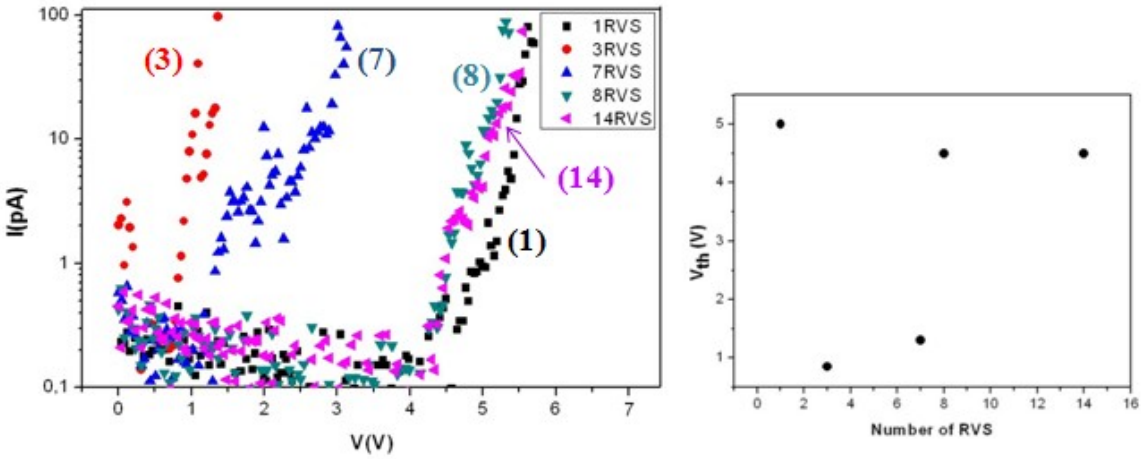


*Figure 4.16: I-V characteristics for several numbers of RVS (left) and the threshold voltage in function of the number of RVS (right).*

In order to confirm these conclusions, Figure 4.17 shows the TUNA images after the creation of a hillock by 6 RVS (Figure 4.17(a)) and 14 RVS (Figure 4.17(b)). A voltage of -6 V is applied on the substrate during the scan. TUNA images recorded after 6 RVS and 14 RVS illustrate that hillocks are leaky when the number of RVS is low, and become non-leaky after a certain number of RVS. Moreover, the two topography images demonstrate the difference in the hillocks' heights which increase from ≈ 5 nm for 6 RVS to ≈ 20 nm for 14 RVS. This result allows considering 2 phenomena to explain the existence of the hillock.

The first phenomenon is the electro-thermal effect by which the oxide is pushed toward the surface by the expansion of the Si bulk while the oxide thickness remains the same [5]. The second phenomenon appears when the stress time is increased, switching from the electro-thermal effect to the oxidation of the Si substrate at the $Si/SiO_2$ interface, increasing the oxide's thickness and preventing the current to pass easily through the oxide. Hence, a layer of oxidized Si ($SiO_x$) may be created as discussed by Polspoel et al. in **[2]**. It must be mentioned that these images allow us to exclude any contribution of the drift of the AFM tip which could have played a role in the results of Figure 4.17 by displacing the tip over a fresh region.

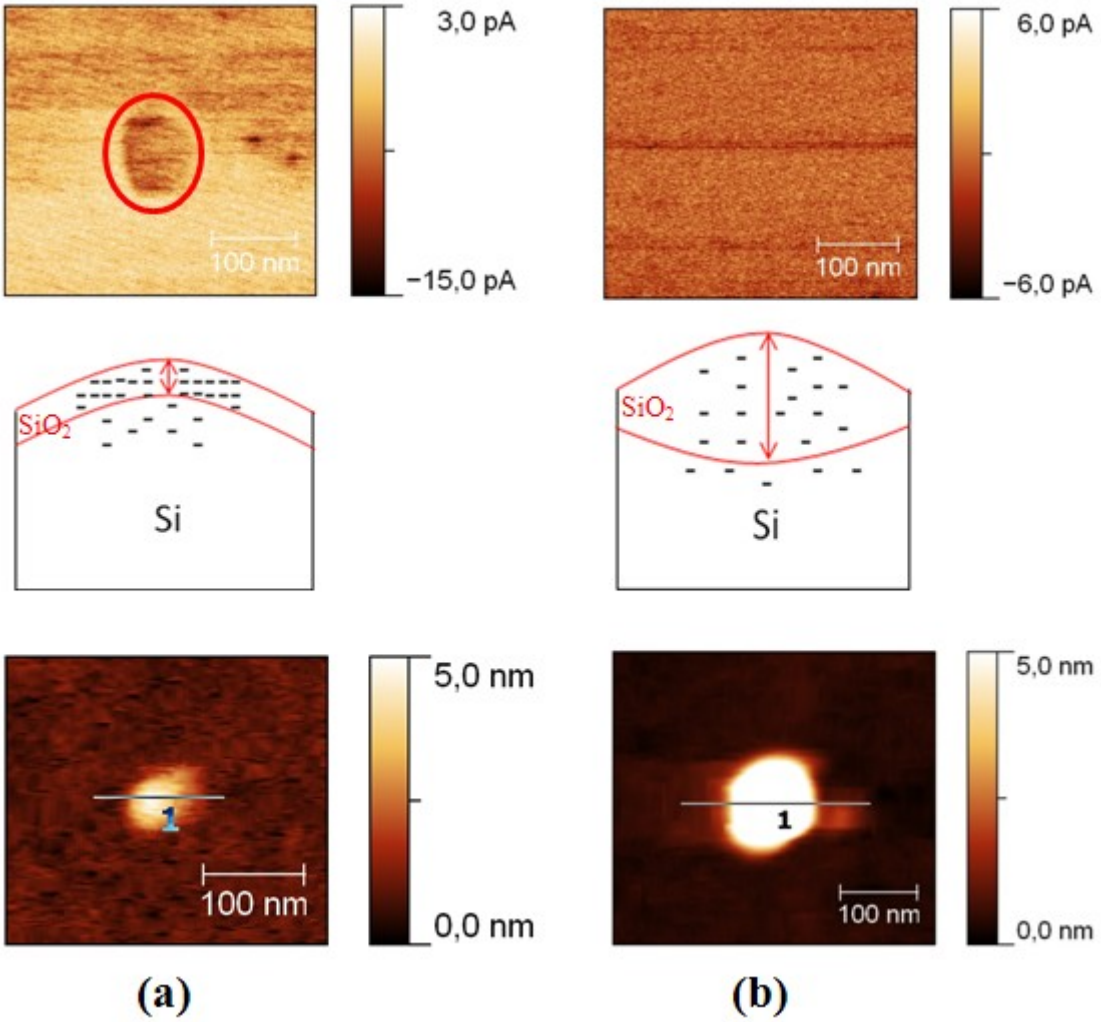


*Figure 4.17: Current images recorded by TUNA mode AFM and by applying a constant voltage of -6 V on the substrate and the corresponding topography images. The centers of the images correspond to the current measured on the hillock (a) Electro-thermal effect phenomenon obtained after 6 RVS. (b) Oxidation of the Si substrate at the Si/$SiO_2$ interface phenomenon after 14 RVS.*

## 4.2) Role of the experimental surrounding ambient

### *4.2.1) Introduction*

Macro-electrical characterizations conducted on macro-size electrodes are almost reproducible because no physical contaminations can take place on the oxide's surface under study. In the contrary, nano-electrical characterizations using the AFM tip as the gate electrode have shown that physical and electrical degradations of the oxide under study may appear as discussed in the previous section (4.1). The main difference between both situations is the protection of the surface of the oxide from the contaminants present in the atmosphere by the metallic electrode in the case of macroscopic characterizations. The aim of this section is to study the influence of the surrounding ambient on the nano-electrical characterization and to find the best conditions in order to have reproducible and non-destructive measurements at the nano-scale.

One of the conditions for improving the quality of the nanoscale electrical measurements is to characterize thin layer oxides in vacuum environment in order to prevent the oxide surface from possible contamination and further oxidation [2][5][11]. In addition, it has been demonstrated that in vacuum environment reproducible results can be obtained without material formation on the surface [12].

In this section, the contribution of the measurement environment, and especially the water layer adsorbed on the oxide's surface, is studied by comparing the electrical and physical properties of thin thermal $SiO_2$ oxide layers using the TUNA mode AFM in air and in secondary vacuum with a heating stage.

### *4.2.2) Experiment*

All the following experiments have been performed by or with the collaboration of Richard Arinero at the South Institute of Electronics (IES), University of Montpellier 2, UMR CNRS 5214.

Experiments have been conducted on a 3.5 nm thick thermal $SiO_2$ oxide grown on a p-type Si substrate ($10^{15}$ at.cm$^{-3}$).

TUNA is used to electrically characterize the 3.5 nm $SiO_2$ films by applying ramped voltage stress (RVS) and measuring the current flowing through the oxide, resulting in localized I-V characteristics. I-V characteristics have been carried out in two different surroundings:

- In air using a Veeco Dimension 3100.
- In vacuum (~ $10^{-6}$ mbar) using a Veeco Enviro-Scope (E-Scope) instrument.
- In vacuum (~ $10^{-6}$ mbar) using a Veeco E-Scope instrument. Additionally, a heating stage (up to ~ 120 °C) monitored by a Lakeshore temperature controller has been used in vacuum during the application of the RVS with the aim to further evaporate the water layer adsorbed on the oxide's surface.

In the two surroundings, the AFM is equipped with a Nanoscope IV controller and a current amplifier (TUNA module). A schematic of the TUNA mode AFM with the vacuum E-Scope chamber is shown in Figure 4.18.

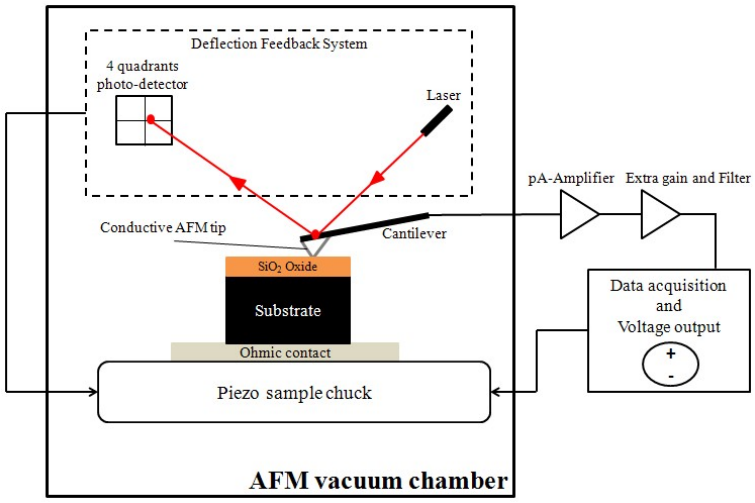


*Figure 4.18: The principle of the TUNA mode AFM.*

### *4.2.2.1) Comparison of threshold voltages*

Representative I-V characteristics corresponding to the very first ramp applied on the fresh oxide in air and in vacuum on a heating stage are presented on the left image of Figure 4.19 (absolute values of the current and the applied voltage are presented). These characteristics are the average result of more than 20 I-V measurements obtained on more than 20 different regions in the three ambient. The stress has been applied on the substrate from 0 to -7 V (forward and backward) which means that the AFM tip was positively biased, with a ramp speed of 0.5 V/sec, although only the forward ramp is presented in the left figure. Here we define the threshold voltage $V_{th}$ as the voltage at which the current through the oxide reaches 10 pA.

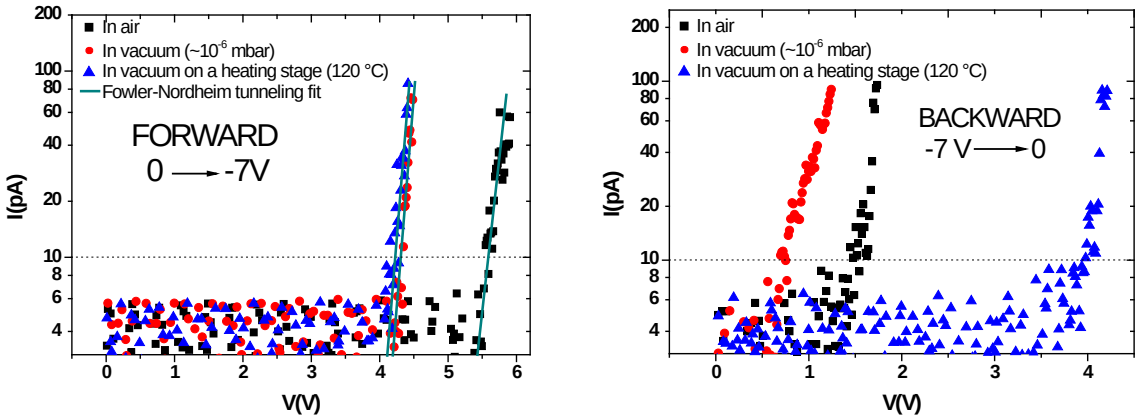


*Figure 4.19: The 1st forward I-V characteristics with their Fowler-Nordheim tunneling fits (left) and the 1st backward I-V characteristics (right) of the 3.5 nm $SiO_2$ oxide film carried out in air, in vacuum and in vacuum on a conductive heating stage respectively.*

An average value of the threshold voltage $V_{th}$ of 5.5 V is measured in air which decreases down to 4.3 V in vacuum and 4.2 V in vacuum on a conducting heating stage. Smaller $V_{th}$ values in vacuum have been demonstrated by Polspoel et al. in [13]. This can be explained by the partial removing of the water layer in vacuum which can be also further removed by the heating stage. This results in a suppression of an access resistance between the tip and the sample. The corresponding electrical model is shown in Figure 4.20.

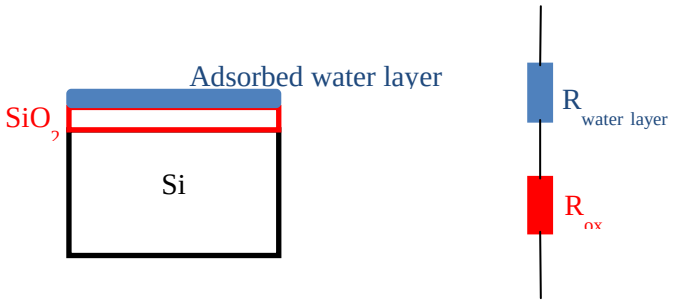


*Figure 4.20: Electrical model of the oxide in air ambient with the adsorbed water layer and its equivalent electrical scheme showing the oxide's resistance in series with water layer resistance corresponding to an access resistance.*

The straight lines in Figure 4.19 (left) are the fits of the Fowler-Nordheim tunneling current that can be expressed by the following equation:

$$I_{FN} = A_{eff} \frac{q^2}{8\pi h \varphi_b} \frac{m_0}{m_{ox}^*} \left(\frac{V_{ox}}{t_{ox}}\right)^2 e^{\left(\frac{-8\pi\sqrt{q}}{3h}\sqrt{2m_{ox}^*}\varphi_b^{\frac{3}{2}}\frac{t_{ox}}{V_{ox}}\right)} \quad (4.1)$$

where $A_{eff} = \pi \times 26^2$ nm$^2$ is the effective contact area between the AFM tip and the surface (the radius is calculated using the FN fit on I-V characteristics of $SiO_2$ oxide film: *shown in Chapter 2 paragraph 2.3.3*), q is the electron charge, h is the Planck's constant, $m_{ox}^*/m_0 = 0.5$ is the effective mass of the electron in the conduction band of $SiO_2$ [14], $t_{ox} = 3.5$ nm is the oxide's physical thickness and $V_{ox}$ is the oxide's potential difference.

In a first approximation, considering the same contact area in air and in vacuum without or with the heating stage since a high electric field is applied on the thin oxide film through the apex of the tip, the $SiO_2$'s effective barrier height $\varphi_b$ can be estimated. By fitting our data we determine the value of $\varphi_b$ to be 3.3 eV in air, 3 eV in vacuum and 2.9 eV in vacuum on a heating stage respectively. The suppression of the access resistance by either the partial or the total removing of the water layer in vacuum without or with a heating stage can be represented by the decrease of the barrier height from 3.3 eV to 2.9 eV.

On the other hand, the representative backward I-V characteristics obtained by ramping from -7 V to 0 V after the first ramp from 0 V to -7 V are presented on Figure 4.19 (right). The strong decrease of the threshold voltage in air and in vacuum is demonstrated, while in vacuum on the heating stage the current remains the same as during the first forward ramp. This can be explained as follows: in the presence of a water layer on the oxide's surface and by applying a positive voltage at the AFM tip greater than that needed for the electrolysis of water (1.23 V) [15], H radicals can be formed and injected through the oxide as interstitial radicals forming attached hydrogen defects in it [16]. These electrically active defects form a path between the tip and the substrate facilitating the passage of charges through the oxide which can be described by the TAT mechanism. However, in vacuum the water layer is partially removed, so by the application of the same voltage applied in air, the oxide is exposed to a higher electric field since the water layer is thinner. On the other hand, in vacuum on the heating stage, the water layer may be removed, so no $H^+$ ions are injected which prevents the oxide layer from any degradation.

As a conclusion, these considerations imply that controlling of Hydrogen existence at the interface is crucial to reduce the degradation of very thin oxide films. This emphasizes the importance of this surrounding atmosphere in the degradation of the oxide layer during the application of an electrical stress: the water layer plays an active role in the degradation process by providing charged species responsible for the degradation of the electrical properties of the film. This means that electrical characterization of oxide films should not be operated in air.

#### *4.2.2.2) Physical degradation of oxide films under vacuum*

In all cases, after applying the electrical stress, the presence of hillocks was observed in the topography image at the places where the tip was positioned. The hillocks' heights are approximately 4 nm in air, 2 nm in vacuum and 1 nm in vacuum on the heating stage (surrounded regions in Figure 4.21). Hence, the hillock's height depend on the experimental ambient as has been discussed in the previous sections.

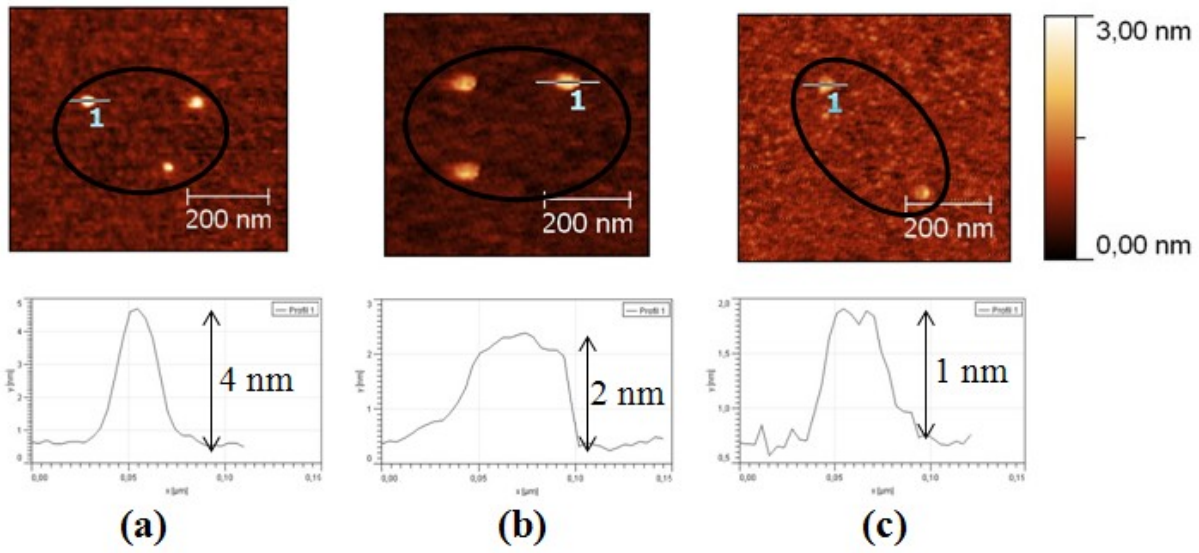


*Figure 4.21: Topography images after the application of several RVS on different zones and the corresponding hillocks' profiles of the surrounded region (a) in air, (b) in vacuum and (c) in vacuum on the heating stage.*

Our results show that by applying a single two ways RVS on the oxide layer, more charges pass through the oxide when it is performed in air. This may increase the Joule heating process within the layer and favor the electro-thermal effect mechanism during the formation of the hillocks.

### *4.2.3) Statistical study of the conduction phenomenon*

A statistical interpretation of the measurements allows to better describe the oxide's reliability [17] in the presence and in the absence of the water layer on the oxide's surface. For this reason, we measure the statistical distribution of the threshold voltage $V_{th}$ extracted from 30 I-V characteristics operated at the nanoscale. The cumulative probability variation P as a function of $V_{th}$ can be expressed using the following Weibull distribution [18]:

$$F = 1 - e^{\left(-\frac{V_{th}}{\alpha}\right)^{\beta}} \qquad (4.2)$$

where F represents the probability that currents higher than 10 pA flows at a particular applied voltage $V_{th}$, α is the voltage at which 63 % of the RVS reach 10 pA, and β is the Weibull modulus indicating the dispersion in the $V_{th}$ values. Voltage ramps were applied from 0 to -7 V with a ramp speed of 0.5 V/sec on 30 different regions in air and in vacuum on a heating stage.

Figure 4.22 (left) shows a comparison of the cumulative breakdown probability versus voltage in air and in vacuum using a heating stage. From this figure, the threshold voltages in air (varying from 5 V to 5.4 V) are higher than those in vacuum (varying from 4.3 V to 4.8 V). As mentioned before, this is coherent with the hypothesis supposing that in vacuum the electrical resistance encountered by the current injected in the oxide is decreased by the suppression of the water layer adsorbed on the oxide's surface. Figure 4.22 (right) shows another Weibull plot representing the linearization of Eq. (4.2) given by:

$$\ln\left[-\ln\left(1-F\right)\right] = \beta \ln\left(V_{th}\right) - \beta \ln\left(\alpha\right) \qquad \textbf{(4.3)}$$

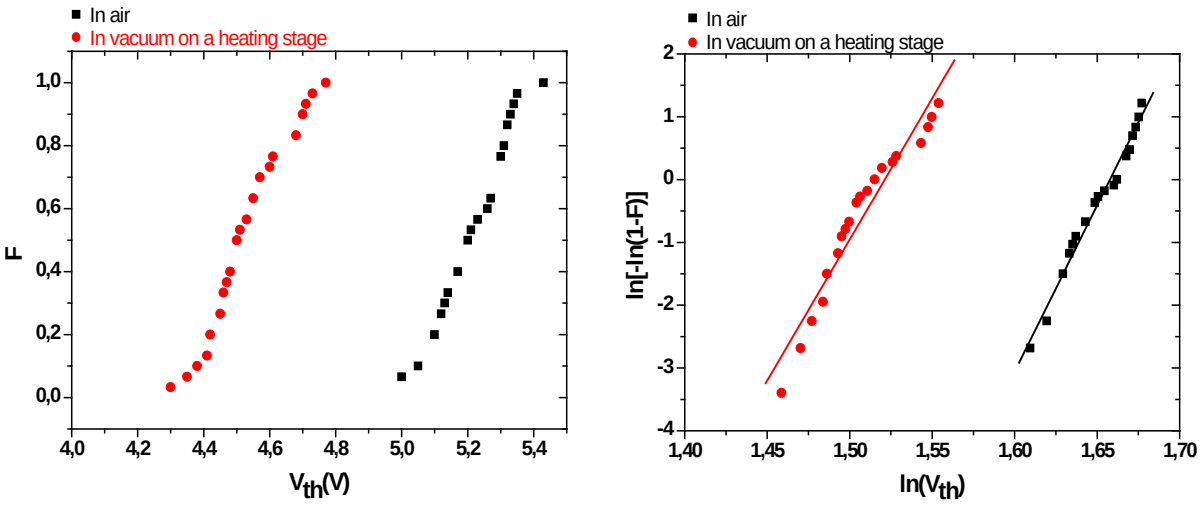


*Figure 4.22: Cumulative probability of breakdown voltages $F = f(V_{th})$ (left curves) and the corresponding Weibull plots of the breakdown voltage distribution $ln[-ln(1-F)] = f(ln(V_{th}))$ (right curves) for the 3.5 nm $SiO_2$ in air and in vacuum using a heating stage. Lines in the right figure are fits to the linearized Weibull plots.*

The Weibull parameters α and β can be easily determined this way by the linear fit of each plot. The corresponding (α, β) values are (5.25 V, 52.88) and (4.58 V, 44.94) in air and in vacuum on a heating stage respectively. The values of α correspond to the values of $V_{th}$ obtained previously. On the other hand, β is lower (higher dispersion in $V_{th}$ values) in vacuum on a heating stage than in air. This can be caused again by the presence of a water layer in air ambient which generates the electrically active defects in the oxide giving rise to a more homogeneous distribution of extrinsic defects which form a path for charges to pass easily through the oxide during the application of an electrical stress [10][16].

### *4.2.4) Study of the influence of the oxide thickness on the electrical degradation of thin oxide films under vacuum*

This study was elaborated with the collaboration of Richard Arinero and it can be found in reference [19].

Arinero et al. have studied the influence of different parameters on the electrical degradation of thin oxide films. They have adopted the Weibull statistics expressed by equation (4.3) for analysing the results where for each analysis, 25 measurements have been performed on 25 different zones. All the experiments have been done in vacuum.

One of the parameters studied by Arinero et al. is the influence of the thickness, where measurements have been conducted on 2 nm, 4 nm and 7 nm $SiO_2$ oxide films deposited on highly-doped $p^+$-Si ($10^{18}$ at.cm$^{-3}$). Weibull plots for the 1$^{st}$ RVS are shown in Figure 4.23. The linear fit of each plot gives the values of β ranging from 28.8 for the 2 nm to 37.9 for the 7 nm indicating the low dispersion of $V_{th}$ values during the 1$^{st}$ RVS, and the values of α which are 4.5 V for the 2 nm, 6.6 V for the 4 nm and 8.7 V for the 7 nm well indicating the logical increase of $V_{th}$ with the increase of the oxide's thickness.

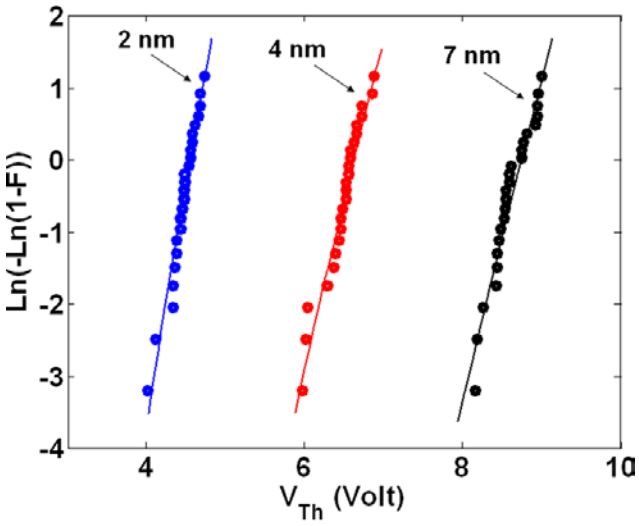


*Figure 4.23: 1$^{st}$ RVS Weibull plots ln[-ln(1-F)] = f($V_{th}$) for different $SiO_2$ oxide film thicknesses of 2 nm (blue points), 4 nm (red points) and 7 nm (black points) on a highly-doped $p^+$-Si [19].*

Concerning the breakdown phenomenon of thin film oxides, Arinero et al. have shown that as the oxide thickness increases, the early breakdown phenomenon disappears. For studying that, two successive RVS (forward and backward) must be applied at the same zone and the 2$^{nd}$ RVS should be taken into account. Figure 4.24 (a), (b) and (c) show the Weibull plots of the 1$^{st}$ and 2$^{nd}$ RVS of the 2 nm, 4 nm and 7 nm respectively.

The red curve of Figure 4.24 (a) presents two groups of points: the 1$^{st}$ group at high $V_{th}$ values which can be linearly fitted by the Weibull plot as for the 1$^{st}$ RVS and the 2$^{nd}$ group

at low $V_{th}$ values which can be considered as early breakdowns. For the first group of values, $\alpha_{2nd\ RVS}$ = 1.96 V and $\beta_{2nd\ RVS}$ = 1.12, which indicate a lower value of $V_{th}$ combined with a high variability. The lower values of $V_{th}$ after the 1st RVS can be explained by the formation of a path of defects leading to the TAT tunneling mechanism of charges during the 2nd RVS.

The red curve of Figure 4.24 (b) represents the Weibull plot of the 2nd RVS of the 4 nm sample. The plot presents one group fitted linearly and no (or few) early breakdowns are evidenced. The values of $\alpha_{2nd\ RVS}$ and $\beta_{2nd\ RVS}$ are respectively 2.6 V and 1.44. The lower value of $V_{th}$ compared to that of the 1st RVS can be explained by the TAT tunneling mechanism of charges.

Whereas for the 7 nm sample, no early breakdowns nor TAT mechanism are noticed as shown in Figure 4.24 (c). In contrast to the previous samples, here the Weibull plot of the 2nd RVS is shifted to the right toward higher $V_{th}$ values indicating the possible trapping of charges in the created defects because of the larger thickness with respect to the other samples.

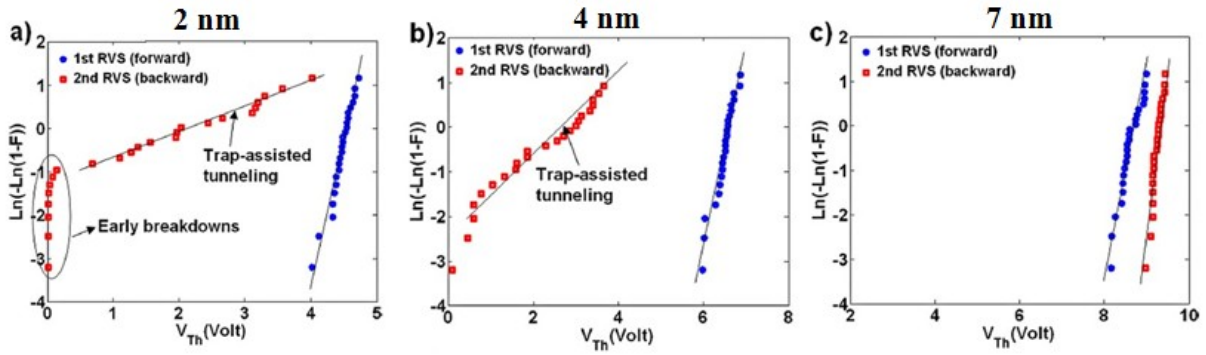


*Figure 4.24: 25 RVS Weibull plots of the 1st (Blue lines) and the 2nd (Red lines) RVS, $V_{th}$ values obtained for: (a) 2 nm, (b) 4 nm and (c) 7 nm thick $SiO_2$ deposited on $p^+$-Si [19].*

### *4.2.5) Study of the influence of the AFM tip composition on the physical degradation of thin oxide films under vacuum*

Similar experiments with PtCr and conductive diamond coated tips have been carried out by Arinero et al. [19] in order to study the influence of each type of AFM conductive tips on the creation of the hillocks. The topography images showing the created hillocks are presented in Figure 4.25. These experiments can be interpreted in two ways: the first is the influence of the thickness and the second is the influence of the type of the AFM tip used. For the first study, Arinero et al. have shown that for both AFM tips used, the hillock's heights increase as the oxide's thickness increase. On the other hand, the diamond coated tip doesn't

produce any morphological modification for the low thicknesses oxides (2 and 4 nm) while hillocks become visible for the thicker one (7 nm).

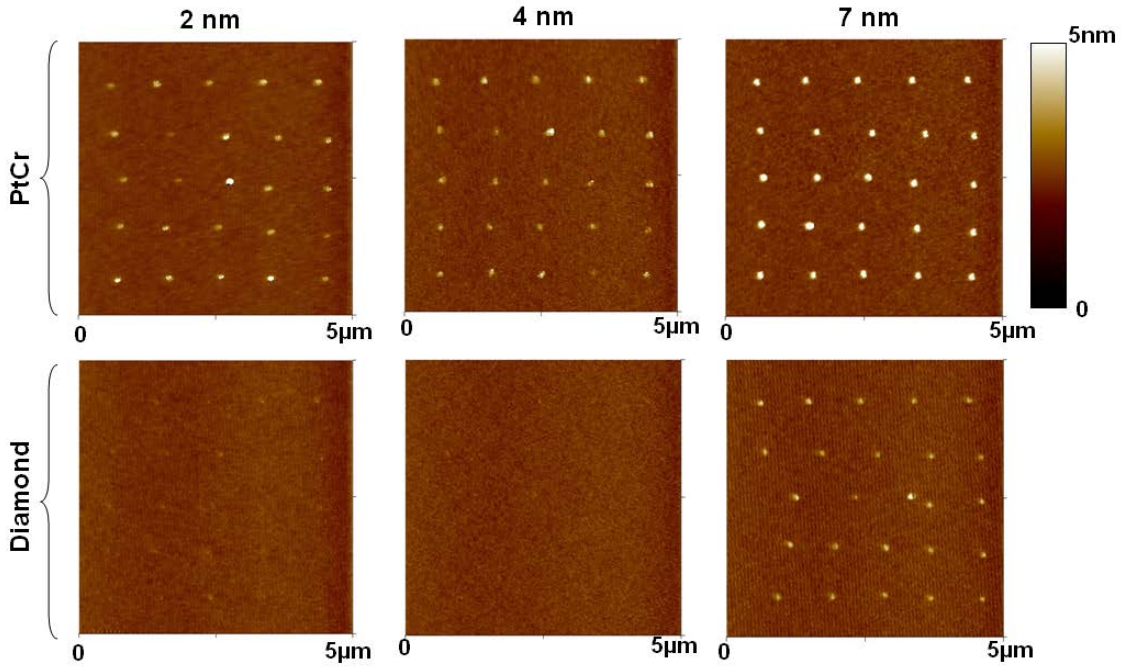


*Figure 4.25: Structural modifications ("Hillocks") observed for different $SiO_2$ thicknesses (2, 4 and 7 nm) deposited on $p^+$-Si and for two types of AFM tip (PtCr coated tips and diamond coated tips) [19].*

Arinero et al. have supposed that these stress-induced physical modifications can be related to the power dissipation by a possible significant Joule heating (as discussed in paragraph 4.2.2.3) and because the tip is separated from the substrate by dielectrics with low thermal conductivity, so heat cannot be removed efficiently. Therefore the temperature rise at the oxide surface can be non-negligible. The phenomenon is illustrated in Figure 4.26.

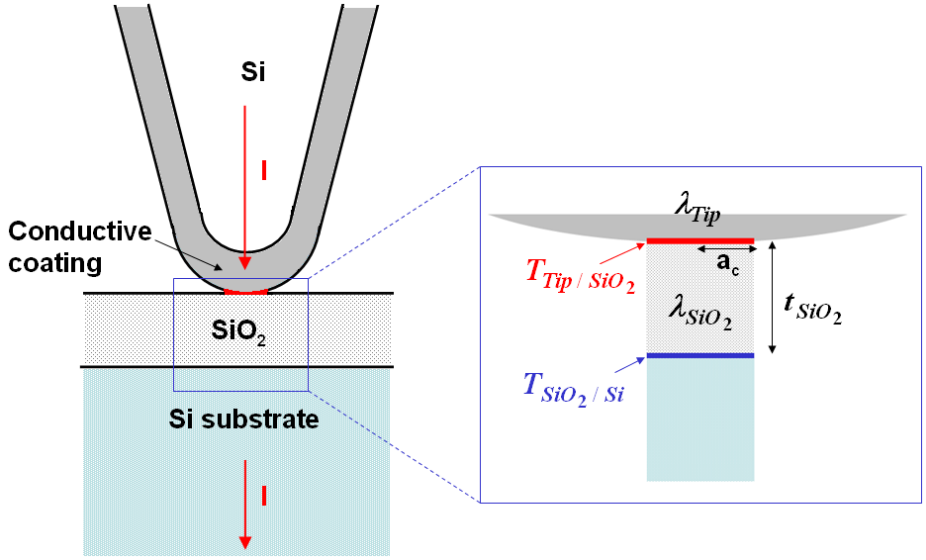


*Figure 4.26: Illustration of tip/oxide power and energy dissipation effects [19].*

Arinero et al. have explained the non-creation of hillocks when diamond tips are used on the small thickness oxide films by the high curvature area of this tips compared to that of the PtCr tips leading to a local temperature approximately five times lower with diamond coated tips. On the other hand, the effect of the increase of the hillocks' heights with the oxide thickness is interpreted by Arinero et al. by the higher energy dissipation $\Delta Q$ in this case, since $\Delta Q$ is directly proportional to the difference between the contact temperature and the $SiO_2$/Si interface initial temperature, that is $T_{Tip/SiO2} - T_{SiO2/Si}$ and to the oxide thickness $t_{SiO2}$ value such that:

$$\Delta Q = \frac{t_{SiO2}}{\lambda_{SiO2}} (T_{Tip,SiO2} - T_{SiO2,Si}) \quad (4.4)$$

where $\lambda_{SiO2}$ is the thermal conductivity of the $SiO_2$ oxide which is about 1.4 $W.K^{-1}.m^{-1}$.

It is clear from relation (4.4) that the energy dissipated into the oxide increases with the sample's thickness. The energy dissipated is always more important in the case of a thicker sample and this can explain why the morphological modifications are more pronounced in this case.

## 4.3) Conclusion

In this chapter different ultra-thin $SiO_2$ thermal oxide films were electrically and physically characterized at the nano-scale in different experimental surrounding ambient with different measurement parameters in order to find the best condition for a reliable nano-scale electrical measurements.

It was demonstrated that the existence of the hillock at the surface of the oxide after the application of an electrical stress is a combination of two phenomena: the real morphological modification of the oxide's surface and the electrostatic force between the trapped charges inside the oxide and the AFM tip. Moreover, a study of the influence of different parameters on the height of the hillock was presented. In air, it was shown that the hillocks always exist with almost the same height independently of the stress time, and that the quantity of charges increases when the current limit increases especially after the 1st RVS after where a path of defects is created inside the oxide which helps the charges flowing through it. On the other hand, in dry air the hillock is not created for short stress time. Hence, two physical phenomena of the creation of the hillock have been proposed according to the number of applied RVS and depending on the current images obtained by TUNA mode AFM, the first is the electro-thermal effect and the second is the oxidation of the Si substrate at the Si/$SiO_2$ interface.

Concerning the influence of the existence of the water layer on the oxide's surface during the application of an electrical stress, it was shown that the current is higher in vacuum for the 1st forward I-V characteristic while it is much higher in air for the 1st backward I-V characteristic indicating the higher degradation of the oxide layer in air. This supports the hypothesis of the tunneling of charges assisted by electrically active defects related to hydrogen coming from the dissociation by the high electric field of the water layer present on the oxide's surface when experiments are conducted in air or in vacuum without heating. Moreover, the existence of a hillock on the oxide's surface after the application of an electrical stress is more important in air than in vacuum emphasizing the importance of the vacuum surrounding in reducing the oxide electrical and physical degradation. This is consistent with the predominant role of electro-thermal effect in the creation of the hillocks during the degradation of the oxide layer in air. Conduction phenomenon was studied using the Weibull statistics, where it has been confirmed that $V_{th}$ in air is higher than in vacuum.

Under vacuum, Weibull distributions of $V_{th}$ allowed to explain that for the thinner samples (2 and 4 nm); TAT occurs starting from the 1st backward RVS. Early breakdowns are even observed for 2 nm samples in which conductive paths are more easily created. Concerning thicker samples (7 nm) second ramp is shifted toward higher $V_{th}$ values indicating the possible trapping of charges in the created defects in the case of higher thicknesses. The formation of hillocks has been studied as a function of the type of tip used and the oxide thickness. The hillocks height was observed to be more notable using PtCr coated tip in comparison with diamond coated tips. This effect may be attributed to higher local temperature rise for a PtCr tip due to smaller contact radius value. Moreover, it has been shown that the energy dissipated is always more important in the case of a thicker sample and this can explain why the morphological modifications are more pronounced in this case.

As a conclusion in the light of these results, in order to have reliable electrical measurements of ultrathin oxide films, it is a major condition to perform these measurements under vacuum in addition to a heating stage in order to ensure a complete removal of the water layer which plays an important role in the electrical and physical degradations of these films.

## 4.4) References

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# General Conclusion

The aim of this work was to demonstrate the capabilities of the atomic force microscope as a valuable tool for providing information about the breakdown mechanisms of ultra-thin oxides with a real nanometric resolution and a maximum of reliability. As the development of innovative devices require the use of characterization techniques able to provide a spatial resolution compatible with the strong decrease of their size, techniques derived from the atomic force microscope can play a major role in gaining knowledge on the nanoscale mechanisms governing their behavior. In order to attain this goal, an effort must be undertaken to enhance the quantitative aspect of measurements provided by the atomic force microscope, impinged by the nature of the AFM itself: mainly the variable size and shape of the tip, the conditions of the tip-sample contact, the sometimes low signal to noise ratio due to the extremely small size of the top electrode (when an AFM tip is used as a top electrode), and the role of the measurement environment when operated in air as it is very often the case which limits the possibility of performing reliable and reproducible nano-scale electrical measurements.

This thesis presented a general study of the current measurements conducted by the AFM on ultra-thin gate oxide films. Taking advantage of the nanometric size of the probe, we could electrically characterize oxide films having many leakage spots as it is the case for high-k gate oxides avoiding the problem of short circuits which may take place between macro electrodes and the substrate in the case of these oxides. Hence, the AFM-based techniques have permitted us to have essential information on the electrical characteristics of ultra-thin oxides that the macro-scale techniques are not capable to detect.

Comparing leakage current measurements conducted by the Agilent 4156B apparatus and by the Nanoscope V connected to TUNA mode-Veeco AFM on 11 x 11 $\mu m^2$ Ti/Au electrodes deposited on 3.5 nm $SiO_2$ thermal oxide film, we have clearly shown that electrical measurements performed by the latter are reliable. We have estimated the circular contact radius to be $\approx$ 26 nm between the $PtIr_5$ conductive tip and the 3.5 nm $SiO_2$'s surface using the Fowler-Nordheim tunneling model on current measurements performed in air ambient and using the measurement technique by which successive I-V characteristics are operated after the AFM tip is displaced 20 nm to 50 nm away from where the previous measurement has been carried out. We have shown that a displacement of more than 26 nm was necessary to obtain the I-V characteristic of a fresh oxide.

The electrical properties of high-k $LaAlO_3$ and $Gd_2O_3$ oxide films have also been studied at the nano-scale using the TUNA mode AFM and in combination with macroscopic

measurements. We have shown that the deposition of these high-k oxides within atomic O ambient enhances their dielectric properties compared to the molecular O ambient. This was explained by that the fact that atomic O may reduce the density of oxygen vacancies which are one of the electrically active defects commonly found in these oxides. This beneficial action of atomic O ambient was demonstrated by the current images which have shown lower densities of leakage spots and by the I-V characteristics showing higher threshold voltages for the high-k oxides deposited within atomic O ambient. Moreover, we have presented a comparison between HF-last and High-T processes for the Si surface preparation before the $LaAlO_3$ deposition and we have shown that the first process has led to cleaner and smoother surfaces with no SiC humps or holes leading to better dielectric properties for the $LaAlO_3$ oxide. On the other hand, the electrical characteristics of $Gd_2O_3$ have demonstrated that its optimal growth temperature is at 700 °C as was also verified by the macroscopic measurements.

After showing that the application of a single electrical stress on the high-k oxides leads to the electrical and physical degradation of these layers which is demonstrated by higher leakage currents during the second stress and the appearance of abnormal hillocks on the oxides surfaces, we have studied more closely the electrical and physical degradation phenomena on the well-known thermal $SiO_2$ oxide. The choice of this classical oxide of very small thickness has been guided by the need to use a reference sample. It was demonstrated that the appearance of the hillock at the oxide's surface after the application of an electrical stress may be the combination of two phenomena: the real morphological modification of the surface and the electrostatic force between the trapped charges inside the oxide and the AFM tip.

Our study of the influence of the experimental ambient on the appearance of the hillock has shown that in air ambient the hillocks are always present with almost the same height independently of the stress time. On the other hand, in dry air the hillocks are not created after a short stress time. As a result, we have proposed two physical phenomena for the creation of the hillocks depending on the number of applied ramped voltage stress and according to the current images obtained by TUNA:

- The electro-thermal effect: the oxide is pushed toward the surface by the expansion of the Si bulk while the oxide thickness remains the same.
- The oxidation of the Si substrate at the $Si/SiO_2$ interface: a layer of oxidized Si ($SiO_x$) may be formed leading to the increase of the oxide's physical thickness.

We have studied the influence of the existence of the water layer on the oxide's surface on the degradation of the stressed oxide layer, and we have shown that the leakage

current is much higher in air for the 2nd RVS compared to experiments conducted under vacuum with a heating stage indicating the higher degradation of the oxide layer in air. We have related this phenomenon to the injection of charges which is assisted by electrically active defects represented by the hydrogen coming from the dissociation by the high electric field of the water layer present on the oxide's surface when experiments are conducted in air. This emphasizes the fact that when probed in air, the electrical behavior of the oxide is strongly influenced by the presence of the water layer and does not behave the same way as what can be measured when an electrode is deposited on the surface. In particular, water favours the breakdown of the oxide layer when water is dissociated by the applied voltage leading to the injection of hydrogen species inside the oxide, which play the role of electrically active defects. So, an important condition to reduce the degradation of the oxide layer during the nano-scale electrical measurements is to remove the water layer on the oxide's surface. This condition can be achieved by performing the experiments under vacuum ($\approx 10^{-6}$ mbar) on a heating stage.

As a conclusion, we have found that in order to have more reliable nano-scale electrical characterization of ultrathin oxide films, the major condition is to perform these measurements under vacuum in addition to a heating stage in order to ensure a complete removal of the water layer.

Considering the results of this work, different perspectives can be considered:

- Studying the evolution of the leakage current through ultra-thin oxide films as a function of time in order to have more information on the kinetics of appearance of hot spots.
- Finding more solutions (other than the Farady cage) to increase the signal to noise ratio in order to increase the dynamic range of current-voltage characteristics, enabling the modeling of these characteristics by well-known conduction types (Fowler-Nordheim, Poole-Frenkel, Trap Assisted Tunneling,…). By doing so, oxide's electrical properties can be estimated with less incertitude.
- A more reliable, more sensitive, more quantitative current measurement operated with an AFM should enable to address more efficiently the study of still badly understood mechanisms like resistive switching effects, with obvious consequences on the enhancement of Resistive Random Access Memories (RRAM).

# Publications/Communications of the author

## Publications

- *Study of the physical and electrical degradation of thin oxide films by atomic force microscope*

  Wael Hourani, Brice Gautier, Liviu Militaru, David Albertini, and Armel Descamps-Mandine

  Journal of Vacuum Science and Technology B, vol. 29, n°. 1, p. 01AA06, 2011; DOI: 10.1116/1.3521474.

- *Influence of the surrounding ambient on the reliability of the electrical characterization of thin oxide layers using an atomic force microscope*

  Wael Hourani, Brice Gautier, Liviu Militaru, David Albertini, Armel Descamps-Mandine, and Richard Arinero

  Microelectronics Reliability; DOI: 10.1016/j.microrel.2011.07.035.

- *Nanoscale study of the influence of atomic oxygen on the electrical properties of $LaAlO_3$ thin high-k oxide films deposited by molecular beam epitaxy*

  Wael Hourani, Liviu Militaru, Brice Gautier, David Albertini, Armel Descamps-Mandine, Sylvain Pelloquin, Carole Plossu, and Guillaume Saint-Girons

  2010 MRS Spring Meeting Symposium I Proceedings, Paper **#:** 1252-I05-09, DOI: 10.1557/PROC-1252-I05-09.

- *Towards a better understanding of the nanoscale degradation mechanisms of ultra-thin $SiO_2$/Si films: Investigation of the best experimental conditions with a Conductive-Atomic Force Microscope*

  R. Arinero, W. Hourani, A.D. Touboul, B. Gautier, M. Ramonda, D. Albertini, L. Militaru, Y.G. Velo, C. Guasch, and F. Saigné

  Journal of Applied Physics 2011, vol. 110, n°. 1, p. 014304-014304-7, 2011; DOI: 10.1063/1.3603037.

- $LaAlO_3$/Si capacitors: Comparison of different molecular beam deposition conditions and their impact on electrical properties

  S. Pelloquin, G. Saint-Girons, N. Baboux, D. Albertini, W. Hourani, J. Penuelas, G. Grenet, C. Plossu, and G. Hollinger

Journal of Applied Physics 2013, 113, p. 034106-1_034106-7 (2013), DOI: 10.1063/1.4769890.

**Oral presentations, participation in conferences**

- European Materials Research Society EMRS, Spring Meeting, Strasbourg, France, June 7-11, 2010.
- Forum des Microscopies à sondes locales, Mittelwihr, France, March 15-19, 2010.

**Poster presentations, participation in conferences**

- Materials Research Society MRS, Spring Meeting, San Francisco, United States of America, April 5-9, 2010.
- Workshop on Dielectrics in Microelectronics WoDiM, Bratislava, Slovakia, June 28-30, 2010.
- International Scanning Probe Microscopy ISPM conference, Munich, Germany, June 19-22, 2011.

# FOLIO ADMINISTRATIF

## THESE SOUTENUE DEVANT L'INSTITUT NATIONAL DES SCIENCES APPLIQUEES DE LYON

NOM : HOURANI DATE de SOUTENANCE : 09/11/2011

Prénoms : Wael

TITRE : Caractérisation des courants de fuite à l'échelle nanométrique dans les couches ultra-minces d'oxydes pour la microélectronique

NATURE : Doctorat Numéro d'ordre : 2011-ISAL-0109

Ecole doctorale : Electronique, Electrotechnique, Automatique (EEA)

Spécialité : Dispositifs de l'Electronique Intégrée (DEI)

RESUME :
La miniaturisation de la structure de transistor MOS a conduit à l'amincissement de l'oxyde de grille. Ainsi, la dégradation et le claquage sous contrainte électrique est devenu l'un des problèmes de fiabilité les plus importants des couches minces d'oxydes. L'utilisation de techniques de caractérisation permettant de mesurer les courants de fuite avec une résolution spatiale nanométrique a montré que le phénomène de claquage des oxydes est un phénomène très localisé. Le diamètre des «points chauds», des endroits où le courant de fuite est très élevé pour une tension appliquée continue, peut-être de quelques nanomètres uniquement. Ceci illustre pourquoi les méthodes de caractérisation avec une résolution spatiale à l'échelle nanométrique peuvent fournir des informations supplémentaires par rapport à la caractérisation classique macroscopique. Il y a deux instruments, dérivés de la microscopie à force atomique (AFM) qui peuvent être utilisés pour faire ce travail, soit le Tunneling Atomic Force Microscope (TUNA) ou le Conductive Atomic Force Microscope (C-AFM). Le mode TUNA qui est utilisé dans notre travail est capable de mesurer des courants très faibles variant entre 60 fA et 100 pA. Notre travail peut être divisé en deux thèmes principaux:

-La caractérisation électrique des couches minces d'oxydes high-k ($LaAlO_3$ et $Gd_2O_3$) à l'échelle nanométrique en utilisant le Dimension Veeco 3100 où nous avons montré que la différence de leurs techniques d'élaboration influe largement sur le comportement électrique de ces oxydes.
-Les caractérisations électriques et physiques à l'échelle nanométrique des couches minces d'oxydes thermiques $SiO_2$ sous différentes atmosphères, c.à.d. dans l'air et sous vide ($\approx 10^{-6}$ mbar) en utilisant le microscope Veeco E-Scope. L'influence de l'atmosphère a été bien étudiée, où nous avons montré que les phénomènes de claquage des couches minces d'oxydes peuvent être fortement réduits sous vide surtout en l'absence du ménisque d'eau sur la surface de l'oxyde pendant les expériences.

En utilisant les plusieurs modes de l'AFM, il a été démontré que l'existence de bosses anormales (hillocks) sur la surface de l'oxyde après l'application d'une tension électrique est une combinaison de deux phénomènes: la modification morphologique réelle de la surface de l'oxyde et la force électrostatique entre les charges piégées dans le volume de l'oxyde et la pointe de l'AFM. Selon les images du courant obtenues par AFM en mode TUNA, deux phénomènes pour la création de ces hillocks ont été proposés: le premier est l'effet électrothermique et la seconde est l'oxydation du substrat Si à l'interface Si/oxyde.

MOTS-CLES :
Échelle nanométrique, microscope à force atomique AFM, Tunneling-AFM TUNA, couches d'oxydes ultra-minces, $SiO_2$, $LaAlO_3$, $Gd_2O_3$, courant de fuite, courant tunnel, tunnel direct, tunnel Fowler-Nordheim, claquage, hillocks.

Laboratoire (s) de recherche : Institut des Nanotechnologies de Lyon (INL)

Directeur de thèse: Brice GAUTIER et Liviu MILITARU

Président de jury : Abdelkader SOUIFI

Composition du jury : Jacques COUSTY, Didier GOGUENHEIM, Martin KOGELSCHATZ, Abdelkader SOUIFI, Brice GAUTIER, Liviu MILITARU, Richard ARINERO.