Etude de la fiabilité de MEMS à fonctionnement électrostatique

Adam Koszewski

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Laboratoire Caratérisation et Fiabilité des Microsystèmes
dans l'École Doctorale:
Électronique, Électrotechnique Automatique et Traitement du Signal

Étude de la fiabilité de MEMS à fonctionnement électrostatique

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Abstract

As MEMS achieve maturity, reliability concerns become of paramount importance. The successful commercialization of MEMS requires preliminary identification and elucidation of possible failure mechanisms, in order to evaluate the probability of the component to perform the required functions over its lifetime. The operating characteristics of electrostatically actuated MEMS (such as RF MEMS switches) are often hampered by dielectric charging effects.

The work which is summarized in this thesis was done entirely in CEA-Leti which has been developing electrostatic RF MEMS switches in collaboration with industrial partners. The objective of this research is to develop reliable ohmic- and capacitive-type RF MEMS switches, which means that the device properties must be well controlled between manufacturing runs and that a minimum operating lifetime under specific conditions is guaranteed.

The main objective of the thesis is to contribute to a better understanding of one of the most important failure modes of this type of devices, that is the dielectric charging mechanism. As a result this thesis tries to elucidate the physical mechanism and the origin of the dielectric charging in RF MEMS switches, to identify the factors accelerating this phenomenon, how it can be characterized and to study the impact of the properties of the dielectric material on the long term behavior of the fabricated switches.

In this thesis two dielectric materials and two switch types are investigated. The investigated dielectric materials are PECVD HF and MF SiN_x and MF SiO_2 dielectrics, which have been used in the present study for the fabrication of capacitive- and ohmic-type RF MEMS switches. At first, the structural properties of the dielectrics are characterized in order to detect any deviation in composition of these materials related to the deposition conditions. Secondly, the dielectric properties of these materials are characterized by measurements on MIM-capacitors. The conduction mechanisms are studied by I-V measurements, while the trapping kinetics is determined using a constant current injection technique. Based on these results, we propose an original model which uses the identified conduction mechanisms and the kinetics of charge trapping in the dielectrics to predict the voltage drifts in the investigated MEMS switches under specific operating conditions and, in particular, under a constant voltage stress. This model is validated by comparing the voltage drifts measured on real RF MEMS switches of capacitive- and ohmic-type, with the results of modeling. It turns out that the model offers a strong potential for a quantitative lifetime prediction. In particular it can be effectively used for screening the potential materials to be used in RF MEMS switches and to investigate the effect of switch design on its long term behavior. Moreover, it may be useful to establish the criteria for the dielectric properties that should be monitored during manufacturing process for early detection of process abnormalities, which could lead to fabricating switches with unacceptable lifetime.

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List of Symbols

$\bar{x}$ Position of charge centroid from injecting electrode

β_s Schottky coefficient

β_{PF} Poole-Frenkel coefficient

ΔC_{max}^{calc} Calculated difference between down-state and up-state capacitance

ΔC_{pi}^{calc} Calculated difference between pull-in and up-state capacitance

ΔC_{max} Difference between down-state and up-state capacitance

ΔC_{pi} Difference between pull-in and up-state capacitance

ΔV_c Shift of ramp-down of I-V curve

ΔV_p Voltage drift due to trapped charge

ΔV_{I-V} Voltage offset between I-V curves

δ_w Radial distance from center of wafer

ϵ_0 Vacuum permittivity

ϵ_r Dielectric constant

ϵ_{r_S} Dielectric constant calculated from Schottky emission model

$\epsilon_{r_{PF}}$ Dielectric constant calculated from Poole-Frenkel model

κ Decay constant

μ Carriers mobility

ν_m Poisson's ratio of material

ν_w Poisson's ratio of wafer material

Ω Range of detection angles

ϕ Barrier height

Φ_0 Electric flux density in air-gap

ϕ_0 Zero-field barrier height

Φ_d Electric flux density in dielectric

ϕ_m Metal work function

ϕ_s Semiconductor work function

$\phi_{M_1M_2}$ Difference of workfunctions between metals

ρ_w Difference of wafer curvature before and after film deposition

σ Electron capture cross-section

σ^* Effective capture cross-section (in logarithmic model)

σ_x^{fit} Fitted value of residual stress

σ_1 Charge concentration at top electrode of switch or capacitor

σ_2 Charge concentration at bottom electrode of switch or capacitor

σ_p Parasitic charge concentration in the dielectric

σ_x Residual stress

σ_{distr} Distribution of trapped charge

σ_{eq} Equivalent surface charge distribution

τ_C^J Charging time constant

τ_D^J Discharging time constant

θ_n Slope in nth built-in end of deflected beam

θ_{RBS} Backscattering angle

Θ_{SC} Ratio of total injected charge to trapped charge

A Richardson constant

A_{el} Surface of electrode

A_{sec} Surface of beam cross-section

C_0 Capacitance of air-capacitor

C_d Capacitance of capacitor with dielectric

C_n nth constant

C_s Capacitance of switch

C_{bulk} Bulk capacitance

C_{distr} Distribution of capacitance

C_{dn} Down-state capacitance

$C_{interface}$ Interface capacitance

C_{MIS} Capacitance of a MIS capacitor

C_{pi} Closed contact capacitance

C_{up} Up-state capacitance

$d\Omega$ Differential capture cross-section in RBS technique

d_n Distance from support to nth concentrated normal force

d_{el} Distance to electrode center from support

E Electric field

e Elementary charge

E_0 Energy of incident particle

E_1 Energy of backscattered particle

E_a Field-dependent activation energy

E_C Conduction band

E_d Electric field in a dielectric

E_F Energy of Fermi level

E_i Intrinsic Fermi level

E_m Young's modulus of material

E_s Electric field in dielectric in switch

E_V Valance band

E_{FM} Fermi level of metal

E_{FS} Fermi level of semiconductor

E_{ln}, E_{ln1} Constant

E_w Young's modulus of wafer material

F_c Contact force

f_f Fringing field correction

F_n nth concentrated normal force

F_r Restoring force

F_z Normal force

F_{el} Electrostatic force

F_{mech} Mechanical force

g_0 Electrode gap height

g_c Contact gap height

h Planck constant

h_d Volume of dielectric inactivated for trapping

I Electric current

I_C Charging current

I_D Discharging current

I_z Moment of inertia of plane figure

IL Insertion loss

$IP3$ Third-order intercept point

J Leakage current density

J_0 Current density prefactor

J_{inj} Injection current density

k_c^{fit} Fitted value of stiffness at beam center

k_{el}^{fit} Fitted value of stiffness at electrode center

k_B Boltzmann constant

k_c Stiffness at beam center for 1 concentrated normal force at beam center

k_s Switch/beam stiffness

$k_{c_{2F}}$ Stiffness at beam center for 2 concentrated normal forces at electrode centers

k_{el} Stiffness at electrode center for 1 concentrated normal force at beam center

k_{F_c} Stiffness at beam center for calculating contact force

k_{RBS} Kinematical factor

$k_{el_{2F}}$ Stiffness at electrode centers for 2 concentrated normal forces at electrode centers

l_i Mean distance between trap sites

l_s Switch length

m Mass of incident particle

M_0 Reaction force moments in built-in ends for symmetrical loads

M_1 Mass of targeted particle

m_e Effective mass of an electron

m_S Slope of $\ln J = f\left(\sqrt{E_d}\right)$ in Schottky model

$M_{A,B}$ Reaction force moments in built-in ends of beam

m_{PF} Slope of $\ln J = f\left(\sqrt{E_d}\right)$ in Poole-Frenkel model

n_0 Constant

N_t Total available trap surface concentration

n_t Filled traps surface concentration

N_t^* Effective concentration of trapped charges (in logarithmic model)

N_{inj} Number of injected charges

n_{t_i} Filled traps surface concentration in i_{th} trap center

P_{in} Input signal power

P_{out} Output signal power

Q_0 Bulk trapped charge

Q_1 Charge at top electrode of switch or capacitor

Q_2 Charge at bottom electrode of switch or capacitor

Q_f Fixed charge

Q_m Mobile (ionic) charge

Q_s Surface charge

Q_t Trapped charge

Q_{inj} Injected charge

Q_{it} Interface charge

Q_{ot} Bulk charge

R_a Arithmetic average roughness

R_q Root mean squared roughness

R_s	Switch resistance
R_{ku}	Kurtosis
R_{max}	Maximum peak height
R_{off}	Off-state (open state) switch resistance
R_{on}	On-state (closed-state) switch resistance
R_{sk}	Skewness
S_{21}	Scattering parameter
T	Absolute temperature
T_a	Axial stretching force due to beam elongation for large deflection
t_d	Thickness of dielectric
t_s	Thickness of switch/beam
t_{down}	Time in down-state (closed-state)
T_r	Axial stretching force to model residual stress
t_{up}	Time in up-state (open-state)
t_w	Thickness of wafer
v	Carriers velocity
$V_{pi_R}^{calc}$	Calculated ohmic pull-in voltage
V_0	Voltage across air-gap
V_d	Total volume of dielectric
v_d	Drift velocity
V_G	Gate voltage
v_t	Trapping rate
V_{act}	Actuation voltage
V_{app}	Applied voltage
V_{FB}	Flat band voltage
V_{max}	Maximum absolute value of voltage applied during test
V_{pi_R}	Ohmic pull-in voltage
V_{pi}	(Capacitive) pull-in voltage

V_{pi}^{calc} Calculated (capacitive) pull-in voltage

V_{po} Pull-out voltage

v_{th} Thermal velocity

W_c Energy stored in capacitor

w_s Switch width

x_s Position along beam length

$x_{N/Si}$ N/Si ration in SiN_x

$x_{O/Si}$ O/Si in SiO_x

Z Atomic number

Z_0 Atomic number of incident particle

Z_1 Atomic number of targeted particle

z_i Vertical distance from the mean line of ith point

z_s Deflection of switch/beam

M_0 Reaction force moments in built-in ends of a beam, for central normal force

Chapter 1

Introduction

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1.1 Overview of RF MEMS switches

MEMS[1] are devices with characteristic length between 1 µm and 1 cm, which combine electrical and mechanical components and are fabricated using IC[2]-compatible batch processing [1].

The RF MEMS switches, in particular, are designed to operate in a broad range of frequencies from 0.1 to 120 GHz. For instance, for communication applications the frequencies vary from less than 1 MHz for AM and 88-108 MHz for FM, up to more than 400 MHz for hand-held military radio transceivers and ∼900 MHz and 2.4 GHz for cellular applications [2]. For automotive applications, such as radars and roof antennas, the standard frequencies are 24, 60 and 77 GHz [3].

The first paper on RF-MEMS switches dates to 1979 [4], however the acceleration of research and development in this domain has been observed since the mid 1990's, especially in the USA. The first RF MEMS switches have been commercialized in 2003 [5] by Magfusion and Teravicta start-ups. The demand for the switches was high and both start-ups failed to respond to it, due to limited fabrication capabilities. In 2006 more than 40 companies, all over the world, have been actively involved in the research and development of RF-MEMS switches, but only a small part of them was close to commercializing their products [5].

[1]MEMS stands for Micro Electro-Mechanical Systems
[2]IC stands for Integrated Circuits

The RF MEMS market is estimated to grow rapidly from US$126 million in 2004 to US$1.1 billion in 2009 [5], which is the main motivation for continuing this research.

1.1.1 Types

An RF MEMS switch uses the mechanical movement of a beam, to modify the impedance of the device. Consequently, the RF MEMS switches can be divided into categories, with respect to the method of actuation of the beam and the type of the contact, which is used to modify the impedance.

1.1.1.1 Actuation methods

The mechanical movement, which is required to switch from the pass-through to blocking state and vice-versa, can be realized in several ways. The choice of the actuation method depends, in general, on the application and performance requirements. Below is a non-exhaustive list of the most common actuation methods used in RF MEMS switches, with a short description of their principles and their main advantages and drawbacks [2, 3, 6, 7]:

- *Piezoelectric*

  In this actuation method, the deformation of a material is achieved by applying a voltage bias, which changes the strain of the piezoelectric material. As a consequence, to sense the position, the change of voltage across the material is measured [7].

  This method requires a moderate actuating voltage (3-20 V) and almost no current flow, which results in nearly-zero power consumption. The switching speed is relatively high, when compared to other actuation methods, and it is in the order of 50-500 µs. The contact forces are relatively low (50-200 µN) [3].

  What presents a problem, is the integration of the piezoelectric material. For instance, the deposition of PZT[3] requires high temperature annealing (at 700°C) to obtain crystalline structure, which makes the whole process CMOS-incompatible[4]. One possible solution, is to replace PZT with AlN, which can be deposited at much lower temperature. The main drawback, however, of using AlN is its low piezoelectric coefficient, which is 15 times lower than that for the PZT. Consequently, to obtain the same deflection, it is necessary to apply to a switch with AlN a voltage 15 times higher, compared to a switch with PZT. Apart from this, both piezoelectric materials are sensitive to the fabrication process and to temperature changes.

- *Electrostatic*

  In the electrostatic actuation method, a voltage bias is applied across a pair of actuation electrodes, one of which is fixed and the other is movable (beam). The applied voltage generates an electrostatic downward force, which pulls-down the beam. Once it is pulled-down, it remains in the down state as long as the voltage is applied. To release the beam, that is to put it back in its initial position, the voltage has to swept back to zero[5]. The

[3]Lead zirconate titanate, a ceramic perovskite material that shows piezoelectric effect
[4]CMOS stands for Complementary Metal Oxide Semiconductor
[5]More detailed discussion of the electrostatic type of actuation is carried out in section 2.3.5.3

beam position is sensed by measuring the capacitance of a capacitor formed between the two actuation electrodes [7].

This actuation method requires a relatively high actuation voltage V_{act} of the order of 10-80V, which is its main drawback. Despite this high voltage, hardly any current is consumed, which leads to very low power dissipation, which ranges from 10 to 100 nJ per switching cycle. The switching speed is the highest among all actuation mechanisms and it ranges from 1 to 200 μs. The contact forces are relatively high (50-1000 μN) [3].

By far, this is the most common method of actuation used in the RF MEMS switches and it has been demonstrated that switches of this type can operate from 100 million to 10 billion cycles.

- *Thermal*

  Similarly to the piezoelectric method, in the thermal actuation method, the deformation of the material is obtained by changing its strain, which is done by controlling the temperature of the material. The main advantage of this method is a lower complexity of the design of the actuator [7].

  The temperature of the actuator is controlled by the current level, which is passing across it. Because the actuation is current controlled (usually 5-100 mA), the actuation voltage can be low (usually 3-5 V). The thermal actuation has the worst performance, in terms of the power consumption (0-200 mW) and the switching speed (300-10000 μs), among all actuation methods. On the other hand, this method provides the highest contact forces, typically ranging from 500 to 4000 μN [3].

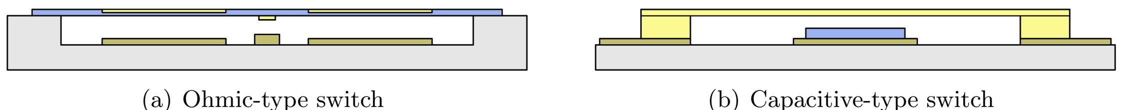
- *Electromagnetic*

  With the electromagnetic actuation method, a magnetic field is used to deflect the beam. The magnetic force is generated by a current flowing in a coil and the actuation is achieved by controlling the level of the current flowing in the circuit. For sensing the displacement, the current induced in the coil is measured. This method is characterized by the highest complexity of switch design, as it requires using the coil and permanent magnets, thus ferroelectric materials. This relatively complex design is the main drawback, preventing from using this method [7].

  Alike the thermal actuation, the electromagnetic actuation is current controlled. It requires the highest current from all the methods (20-150 mA), but the actuation voltage can be as low as 3-5 V. Despite the highest current, this type of switch is slightly less power consuming (0-100 mW), when compared to the thermal actuation. The switching speed is relatively low (300-1000 μs), which is comparable to the thermal actuation. The contact force is also low (50-200 μN) and it is similar to the piezoelectric method [3].

1.1.1.2 Contact types

The RF MEMS switches can be further divided into two categories, with respect to the type of the contact which is used to modify the impedance of the device. Cross-sectional views of these two types of MEMS switches are presented in Figure 1.1(a) for the ohmic-type contact and in Figure 1.1(b) for the capacitive-type.



(a) Ohmic-type switch (b) Capacitive-type switch

Figure 1.1: Cross-section views of ohmic- and capacitive-type RF MEMS switches

- *Ohmic-type contact*

  The ohmic-type contact, which is often used in series configuration, is presented schematically in Figure 1.1(a) [3]. Switches of this type have a metal-to-metal contact. In the blocking state the input and output terminals on the RF-signal transmission line are separated by a gap, thus the signal is blocked. In the pass-through state, the beam is pulled down and a metallic contact, which is attached to the beam, shorts these two terminals and the signal passes. Characteristics of the ohmic contact make it suitable for applications for a broad range of frequencies from a DC up to 40 GHz [8]. The RF-properties, that is the insertion loss and isolation of the switch depends on the quality of the ohmic contact (low resistance). As a consequence, the switch lifetime defined in terms of the minimum acceptable RF-performance, strongly depends on the reliability of the ohmic contact.

- *Capacitive-type contact*

  The capacitive-type contact, which is often used in shunt configuration, is presented schematically in Figure 1.1(b) [3, 9]. Switches of this type use a metal-dielectric contact for blocking and passing the RF signal. This is done by modulating the air gap (the capacitance), between the movable beam and a dielectric layer on top of the RF line. In the initial undeflected position, the switch is in the pass-through state, because the air gap is maximum (the capacitance is the lowest). This low capacitance limits the losses of RF-signal transfer, through the signal line. When the beam is pulled-down, it comes in contact with the dielectric. The air gap virtually disappears and the capacitance abruptly increases, blocking the RF signal. The isolation depends on the C_{dn}/C_{up} ratio, where C_{dn} is the down-state capacitance (when the switch is closed) and C_{up} is the up-state capacitance (when the switch is open). The higher the C_{dn}/C_{up} ratio is, the higher the isolation. Because of the capacitive coupling used for blocking the signal, the capacitive-type switches are not suitable for low-frequency applications, unlike the ohmic-type switches. The typical bandwidth of the capacitive-type switches is from 10 to 120 GHz [8].

1.1.2 Performance

RF MEMS switches are alternative to p-i-n diodes and field-effect transistor (FET) switches [3]. The performances of the state of the art RF MEMS switches in 2007 and their perspectives until 2015 are presented in Table 1.1 and Table 1.2 , for the ohmic- and capacitive-type switches, respectively.

The performance of alternative (to RF MEMS) p-i-n diodes and FET switches is presented in Table 1.3 [8].

This performance is typically characterized by a set of parameters parameters, as listed and explained below.

Table 1.1: Performance of the state of the art (SoA)electrostatically actuated ohmic-type RF MEMS switches and perspectives for improvement (reprinted from [8])

Parameter	SoA switch in 2007	2010	2015
Insertion loss [dB]	0.2-0.5	0.2	-
Isolation [dB]	> 20	> 30	-
Power consumption [µW]	10^{-6}	-	-
Bandwidth [GHz]	0-40	0-80	-
Linearity (IP3) [dBm]	> 65	70	80
Actuation voltage [V]	10-70	5	3
Switching speed [µs]	< 100	< 30	-
Switching cycles [1] [10^9]	< 1	< 10	100
Power handling [W]	10	< 45	-
Level of integration	hybrid	hybrid	hybrid + monolithic
Packaging	Die level sealing and overmolding approaches	Also thin film	-

[1] 100 Hz, 50% duty cycle, unipolar actuation

Table 1.2: Performance of the state of the art (SoA)electrostatically-actuated capacitive-type RF MEMS switches and perspectives for improvement (reprinted from [8])

Parameter	SoA switch in 2007	2010	2015
Insertion loss [dB]	0.2-0.5	0.2	-
Isolation [dB]	> 20	> 30	-
Power consumption [µW]	10^{-8}	-	-
Bandwidth [GHz]	10-120	1-120	-
Linearity (IP3) [dBm]	> 65	70	80
Actuation voltage [V]	40-70	40-70	40-70
Switching speed [µs]	< 100	< 10	1
Switching cycles[1] [10^9]	< 0.01	< 1	10
Power handling [W]	2	5	-
Level of integration	hybrid	hybrid	hybrid + monolithic
Packaging	Die level sealing and overmolding approaches	Also thin film	-

[1] 100 Hz, 50% duty cycle, unipolar actuation

- *Insertion loss*

  Insertion loss IL [dB] of an RF MEMS switch is the RF loss dissipated in the device [2, 10]. It is typically characterized by the S_{21} parameter, between the input and output of the switch in its pass-through state. For the ohmic type switches, the main factors that contribute to the insertion loss, include resistive loss due to the resistance of the signal and contact lines at low to medium frequencies and loss due to skin depth effect at high frequencies. In capacitive switches, it includes dielectric absorption [2, 10]. The insertion loss is calculated as a ratio of the input P_{in} to the output P_{out} signal power [6, 10]:

  $$IL = 10 \log \left(\frac{P_{in}}{P_{out}} \right) \tag{1.1}$$

  Because the output signal is lower than the input, the insertion loss is > 0 dB.

  In RF MEMS switches, the insertion loss ranges from 0.2-0.5 dB, compared to 0.5-2 dB per switching cycle for alternative, standard solid-state switches [6, 8].

- *Isolation*

  Isolation of an RF MEMS switch refers to RF isolation between the input and output, typically characterized by S_{21} parameter of the switch in its blocking state, which is the open state for a series switch. The main factors that contribute to isolation are capacitive coupling and surface leakage [2, 3, 5, 6, 8, 10, 11].

  RF MEMS capacitive switches can be fabricated with large air-gaps, which results in very low up-state capacitance, thus high isolation at 10-120 GHz.

  Typically, the isolation in RF MEMS switches is better than 20 dB [3, 6, 8, 10].

- *Power consumption*

  Electrostatic actuation is the most common actuation method for RF MEMS switches. It requires relatively high voltages (10-80 V) but it hardly consumes any current, leading to a very low power dissipation of the order of 10-100 nJ per switching cycle [2, 3, 6, 8].

- *Bandwidth*

  Bandwidth is the measure of the width of a range of operating frequencies of the switches. For instance, for the ohmic-type RF MEMS switches the cut-off frequency is 40 GHz, which is much higher, compared to 5 GHz, for GaAs p-i-n diode switches and 2.5 GHz for FET switches. For the capacitive-type switches the cut-off frequency is even higher than for the ohmic-type and it is approximately 120 GHz [3, 5, 6, 8].

- *Linearity*

  Linearity of RF component refers to the independence of the device impedance from the input RF signal power, typically characterized by the third-order intercept point, or $IP3$, in a two-tone RF intermodulation measurement [2, 6].

  RF MEMS switches are very linear devices, and therefore, result in very low intermodulation products. In general, their linearity is 30 dB better than for p-i-n or FET switches [6, 8].

- *Actuation voltage*

  Actuation voltage V_{act}, is defined as the minimum DC voltage required to close the switch. The main contributing factors are the stiffness of the beam and the air-gap. By adjusting these two parameters it is possible to optimize the switch behavior, according to specific requirements. A detailed mathematical model to calculate this actuation voltage is presented in section 2.3.5.3.

  Electrostatic MEMS switches require 10 to 80 V for operation. This high voltage presents a problem for portable telecommunication systems, for which a voltage up-converter chip is required. However, this is not a problem for potential satellite applications, where the primary bus is 100 V on modern spacecrafts [3, 5, 6, 8, 11].

- *Switching speed*

  Switching speed is the minimum time between opening and closing of a switch [3, 6]. The main contributing factors are the mass and the stiffness of the beam, the damping coefficient and the ratio between the applied voltage and the minimum actuation voltage.

  Most of the MEMS switches have a relatively low switching speed, which is in the range of 2 to 40 μs, while for alternative p-i-n diodes and FETs the switching time is as short as several ns [3, 6].

- *Power handling*

  Up to date, most of the MEMS switches are not suitable for handling high power signal. The typical maximum signal power is 2-5W, which is much lower than 27-38 W, for the p-i-n diodes and FETs [3, 6, 8].

- *Level of integration*

  The strong potential of the RF MEMS switches lies in common VLSI[6] design and batch processing, which includes fabrication using IC-compatible micromachining techniques [3, 6, 11]. The RF MEMS can be build on a number of substrates, including high resistivity silicon, silicon-on-insulator (SOI), or SiC and GaAs substrates. Moreover, the switch dimension are large compared to IC, thus the fabrication does not require the use of the most recent equipment.

  The RF MEMS switches not only replace existing solutions thanks to superior performance, but also introduce new functionalities (redundancy, electrical reconfigurability). As a consequence it is possible to replace multiple single components by a single device, whose characteristics can be adjusted.

  The use of IC-compatible fabrication techniques allows monolithic integration of MEMS switches with electronics to produce a complete system-on-a-chip that can sense, perform computations and communicate.

  Thanks to monolithic integration with electronics, simplifications of the circuits and reconfigurability it is possible to further reduce the size and weight of the RF systems [3, 6, 8, 11].

[6]VLSI stands for Very-large-scale integration

Table 1.3: Performance of alternative technologies for RF MEMS switches up to 6 GHz (reprinted from [8])

Parameter	p-i-n	FET
Insertion loss [dB]	0.5-1.5	1-2
Isolation [dB]	25-40	20-24
Power consumption [μW]	-	-
Bandwidth [GHz]	0-5	0-2.5
Linearity (IP3) [dBm]	40-50	39
Actuation voltage [V]	2.5-3.0	3
Switching speed [μs]	0.01-0.02	-
Switching cycles[1] [10^9]	-	-
Power handling [W]	30-38	27
Level of integration	-	-

[1] 100 Hz, 50% duty cycle, unipolar actuation

- *Packaging*

  MEMS switches need to be packaged in inert atmospheres (nitrogen, argon, etc.) and in very low humidity for correct operation. This results in hermetic or near-hermetic seals, which are several times more expensive than non-hermetic packaging. Currently, the packaging cost can be as high as 20% to 90% of the unit price of a MEMS switch [3, 6, 8, 11].

To sum up, the silicon FET switches are appropriate for operating at low frequencies, where they can handle a high power signal. At high frequencies, their performances drop dramatically. The GaAs metal-semiconductor FET (MESFET) and p-i-n diodes work well at high frequencies, but can handle only a low power signal. The first of the drawbacks of all solid-state switches, is a large insertion loss of 1-2 dB in the pass-through state above 1GHz. This may require additional gains in the circuit, which complicates the design and increase power consumption. The second drawback is poor electrical insulation, which is of the order of -20 to -25 dB in the blocking state [2, 6] .

The RF MEMS switches are better than their solid-state counterparts, especially in terms of isolation, insertion loss and linearity. Thanks to their performance and reconfigurability the RF MEMS components can replace entire solid-state circuits [2]. Nevertheless the RF MEMS are an emerging technology, which is still facing reliability issues. Further improvements are also required to decrease the switching time.

1.1.3 Reliability issues in RF MEMS

The reliability of MEMS switches was demonstrated to be 0.1-200 billion cycles, which meets the required 20-200 billion cycles, for typical applications. However, the long term reliability (in years) has not been yet addressed and the lifetime characterization is often limited to test under laboratory conditions on a limited number of devices [6].

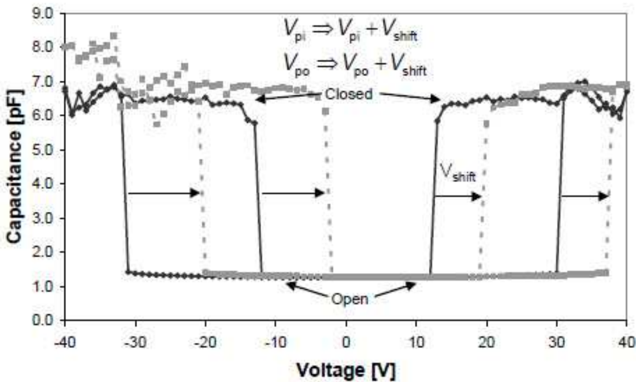


Figure 1.2: C-V characteristics of capacitive-type switch before and after voltage stress [12]

For the RF MEMS switches there are still two failure modes, which contribute to significant reduction of switch lifetime. One is related to the actuation method and the other one to the reliability of the contacts.

1.1.3.1 Failure related to actuation method

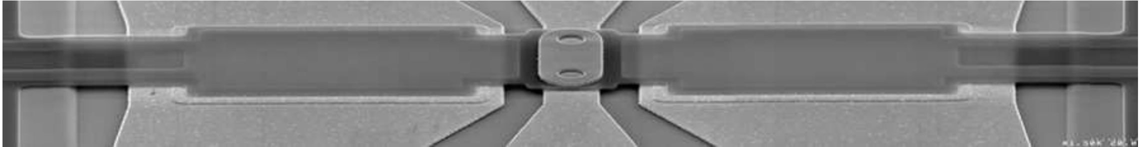
The most common actuation method in RF MEMS switches is electrostatic actuation. The standard actuating voltage in electrostatically RF MEMS is in the range of 10-80 V, the air-gap is lower than several μm and the thickness of the dielectric is typically below 1 μm. These relatively high voltages combined with a small air-gap and a low thickness of the dielectric, create a very high electric field in the dielectric layer, which can be as high as several MV/cm, during normal operation. In these conditions, some parasitic charge may be trapped in the dielectric. The charge generates a permanent electrostatic force even in the absence of an external electric field. Depending on the distribution of the trapped charge in the dielectric layer, it may lead to either drift of the pull-in voltage or narrowing of the window between the negative and positive pull-in voltages. Consequently, if the voltage drift is high enough, the pull-in voltage may exceed the actuating voltage and the switch cannot be closed anymore, or the negative pull-out voltage will shift towards positive voltage values and the switch will remain permanently closed at zero bias [11].

To give an example, Figure 1.2 presents an initial C-V curve for a capacitive-type switch and a shifted C-V curve after an application of a constant voltage stress during a given time [12].

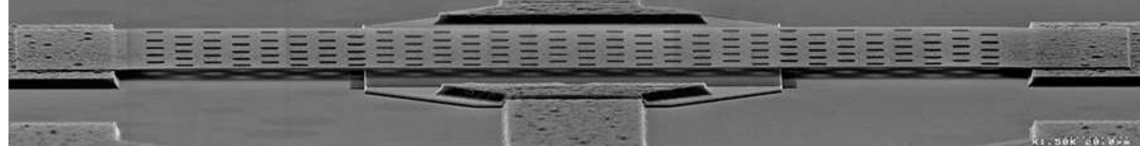
Quantitative analysis of the influence of the trapped charge on the pull-in voltage and the C-V characteristic of the RF MEMS switches will be carried out in detail in Chapter 4.

1.1.3.2 Failure related to contact quality

The ohmic-type switches use a metal-to-metal contact to switch between the blocking and the pass-through state. Any degradation of the contact increases the resistance, thus it increases the



(a) SEM image of ohmic-type switch



(b) SEM image of capacitive-type switch

Figure 1.3: Ohmic- and capacitive-type RF MEMS switch fabricated by CEA-Leti

signal loss. The critical point, is the choice of the contact materials, which has to be optimized in terms of contact resistance, stiction tendencies and expected lifetime.

1.2 Motivations, objectives and organization of thesis

1.2.1 Thesis motivations

The entire thesis has been realized in the CEA-Leti in Grenoble[7], which is an applied research center for microelectronics and information technology, and acts as an interface between industry and academic research.

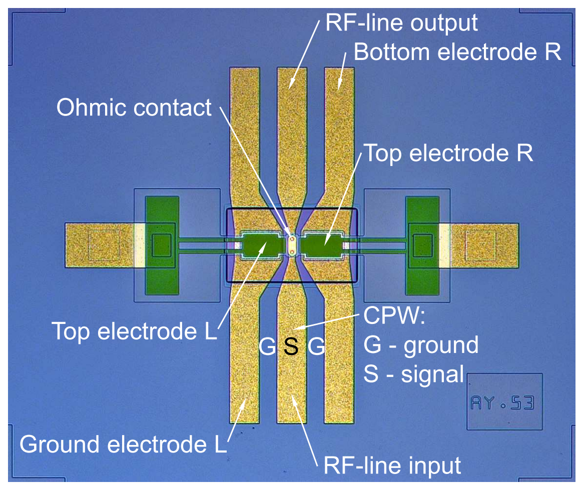
One of the research topics that the CEA-Leti together with industrial partners has been recently working on, is the development of electrostatically-actuated RF-MEMS switches, with the primary interest in the ohmic-type ones. The aim of this joint project is fabrication of reliable RF MEMS switches and their commercialization.

This thesis was launched to investigate the reliability of electrostatically-actuated, ohmic- and capacitive-type RF MEMS switches, which had been designed, fabricated and packaged by the CEA-Leti.

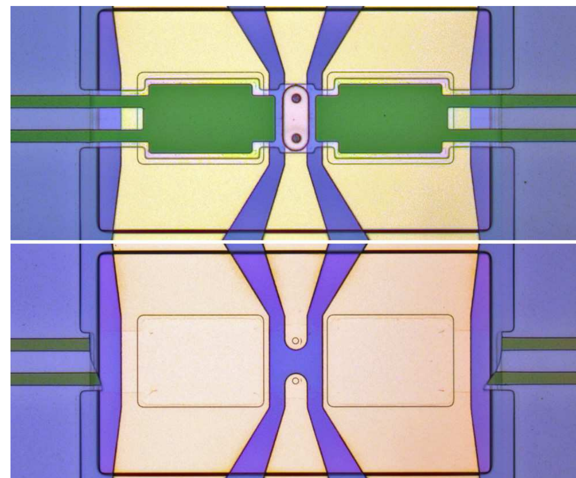
1.2.2 Test samples - RF MEMS switches from CEA-Leti

In the recent years the CEA-Leti has been exploring various MEMS switch technologies, including different actuation mechanisms. The electrostatic actuation turned out to be the most promising one. Currently, the CEA-Leti fabricates electrostatically-actuated MEMS switches of ohmic- (Figure 1.3(a)) and capacitive-type (Figure 1.3(b)), which will be investigated throughout this thesis. The following sections present a detailed description of their working principles, performance, as well as the fabrication process flow.

[7]This thesis has been realized in the Microsystems Characterization and Reliability Laboratory (LCFM)



(a) Top view of ohmic-type switch



(b) Top view of switch with and without beam

Figure 1.4: Ohmic-type RF MEMS switches fabricated by CEA-Leti

1.2.2.1 Ohmic-type switches

The CEA-Leti ohmic-type RF MEMS switch is presented in Figure 1.3(a) and Figure 1.4. It is composed of top (movable) beam with side-electrodes (TiN) and ohmic contact (Au), which are suspended over ground electrodes (Au) and a signal-line (Au). The top electrodes are separated from the ground electrodes by a layer of dielectric (PECVD SiN_x) and an air-gap.

The area of the actuation electrodes is 2 x 6300 μm^2, the thickness of the dielectric below the top TiN electrode, is roughly 400 nm and the typical air gap is 0.4-1 µm. The beam is 340 µm long and 60 µm wide (on average).

This switch uses a coplanar waveguide (CPW) design with a ground-signal-ground parallel metal line configuration [13] that results in a constant characteristic impedance of 50 Ω. Dimensions of the CPW have been optimized using full wave analysis. The gold CPW is 830 µm long, the transition length is 100 µm and the width of the ground / signal / ground lines is: 45/80/45 µm at the ports and 12/20/13 µm under the SiN_x beam.

The working principles of the ohmic-type switches are following. When the switch is in its original undeflected position, there is a gap between the input and the output terminals of the RF line (Figure 1.4(b)), thus the switch is in the blocking state. Suspended over the RF line is a beam with a metallic contact. When a voltage is applied across the top and bottom side electrodes, it creates an electrostatic downward force, which pulls-down the beam. The metallic contact shorts the RF-line, switching to the pass-through state.

These switches are fabricated using surface micromachining techniques. The main process steps are presented in Table 1.4.

The substrate is a high resistive silicon (5 kΩcm and $\epsilon_r = 11.7$), which has been chosen to meet the requirements of RF performance. The bottom electrodes and the ohmic contact (fixed and mobile) are made of gold, because of its good conductivity and compatibility with MMICs[8]

[8]MMIC stands for Monolithic Microwave Integrated Circuit

Table 1.4: Fabrication of ohmic-type RF MEMS switch fabricated by CEA-Leti

Result	List of fabrication steps
	• Preparation of 100/200mm Si HR substrate (5 kΩcm) • Thermal oxidation of Si substrate (3 μm) • Etching of thermal oxide (1.5 μm) - formation of recess • Etching of thermal oxide (0.3 μm) - formation of bosses
	• Deposition of Ti seed layer (100 nm) • Patterning of Ti layer • Deposition of Au (1 μm) • Patterning of Au - formation of coplanar waveguide (CPW) • Deposition and patterning of polymeric sacrificial layer • Annealing at 300° C
	• Deposition of HF PECVD SiN_x (400 nm) • Patterning of HF PECVD SiN_x - formation of membrane
	• Deposition of TiN (150 nm) • Patterning of TiN - formation of top side electrodes
	• Deposition of HF PECVD SiN_x (200 nm) • Deposition of Cr (100 nm) Au (300 nm) resist
	• Etching through Cr / Au layer • Stripping of Cr / Au resist • Etching two through holes in the SiN_x membrane • Etching two blind holes in the polymer resist
	• Deposition of Au (1.2 μm) - formation of mobile contact • Deposition of HF PECVD SiN_x (200 nm) • Patterning of HF PECVD SiN_x • Removal of polymeric sacrificial layer

technology. A HF PECVD[9] SiN_x is used as a structural material for the beam. The use of PECVD allows limiting the process temperature to 300°C, which ensures monolithic integration capability with MMICs [2] and helps avoiding hillocking [14]. Moreover, by using the STS mixed-frequency technique[10] it is possible to control the level of the residual stress in the beam, which defines its stiffness. It is then possible to adjust the level of the pull-in voltage and the contact and restoring forces.

1.2.2.2 Capacitive-type switches

The capacitive-type RF MEMS switch fabricated by the CEA-Leti is presented in Figure 1.3(b) and Figure 1.5. It is composed of top (movable) beam (Al or AlSi), which is suspended over a signal-line (Pt). The top electrode is separated from the signal line by an air-gap and a layer of dielectric (PECVD SiN_x or SiO_2).

The effective area of the actuation electrode is 9000 μm^2, the air gap is 1.5-2 μm and the thickness of the dielectric is comprised between 250 and 330 nm. The beam is 330 μm long and 100 μm wide.

Similarly to the ohmic-type switches, the capacitive-type switches use a coplanar waveguide (CPW) designed with a ground-signal-ground parallel metal line configuration that results in a constant characteristic impedance of 50 or 75 Ω, depending on the switch design.

The working principles of the capacitive-type switches are following. When the switch is in its original undeflected position the switch is in the pass-through state, as the air gap is maximum, hence the switch capacitance is minimum. When a voltage is applied across the top and bottom electrodes, the membrane is pulled-down and it comes to intimate contact with the dielectric on top of the RF-line. The increased capacitance creates a small impedance between the RF-line and the ground, blocking the RF signal from passing to the other side of the line, hence the switch is in the blocking state.

The C_{dn}/C_{up} capacitance ratio defines the isolation and the insertion loss of the switch. This ratio is a compromise between a high C_{dn} required for high isolation and a low C_{up} required for small insertion loss. The high value of C_{dn} requires an intimate contact between the top electrode and the dielectric in the down-state, thus a low roughness and a high flatness of the dielectric and the beam. The low value of C_{up} can be obtained by increasing the air gap between the electrodes, but the trade-off is an increase of the pull-in voltage.

The capacitive-type switches are fabricated using surface micromachining techniques. The main fabrication process steps are presented in Table 1.5.

The substrate is a high resistive silicon (2-10 kΩcm and $\epsilon_r = 11.7$). The bottom electrode is made of platinum (500 nm) deposited on a thin titanium seed layer (20 nm). PECVD SiN_x or SiO_2 are used as dielectric layers. The top membrane is made of a 0.5 μm thick aluminum or aluminum-silicon alloy.

1.2.2.3 Comparison of ohmic- and capacitive-type switches

Both switch types use the same electrostatic actuation method. In each case, the top movable electrode is separated from the bottom electrode (the RF-line) by a layer of a PECVD dielectric. What is different for these two types is the position of the air gap. In case of the ohmic-type

[9] HF PECVD stands for High Frequency (13.56 MHz) Plasma Enhanced Chemical Vapor Deposition
[10] This technique is described in detail in Appendix B

Table 1.5: Fabrication of capacitive-type RF MEMS switch fabricated by CEA-Leti

Result	List of fabrication steps
	• Preparation of 100/200mm Si HR substrate (2-10 kΩcm) • Deposition of poly-Si(1 μm)
	• Thermal oxidation of poly-Si (300 nm)
	• Deposition of Ti (20 nm) • Patterning of Ti - formation of bottom electrode
	• Deposition of Pt (400 nm) • Patterning of Pt - formation of bottom electrode
	• Deposition of PECVD SiN_x or SiO_2 (250-330 nm)
	• Sputtering of Au (2 μm) - formation of CPW
	• Deposition of Al or AlSi (500 nm) • Patterning of Al or AlSi - formation of membrane

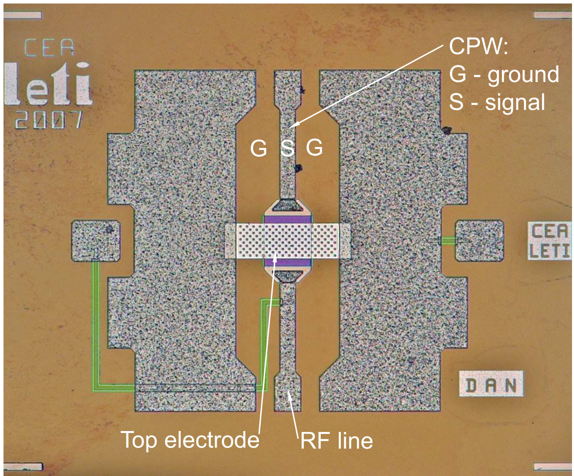


Figure 1.5: Capacitive type RF MEMS switch fabricated by CEA-Leti

switch, the dielectric constitutes the movable electrode, thus the air-gap is formed between the dielectric and the bottom electrode. In case of the capacitive-type, the dielectric is deposited on top of the RF-line, thus the air-gap is located between the dielectric and the top electrode.

Table 1.6 compares the performance and characteristics of the ohmic- and capacitive-type switches fabricated by the CEA-Leti. The ohmic-type switches are designed to operate at lower frequencies from DC to approximately 40 GHz, while the capacitive-type switches can operate in the range of 10 to 120 GHz. The nominal actuation voltage for the ohmic-type switches is 15 to 25 V and it is lower than for the capacitive-type switches, where it is 25 to 40 V. The dimensions of the ohmic-type and capacitive-type switches are comparable.

1.2.3 Review of thesis objectives

In the course of research and development of the RF MEMS switches by the CEA-Leti, it has turned out that their lifetime is seriously affected by the problems of ohmic contact degradation and the dielectric charging. While the ohmic contact degradation is a lifetime limiting factor for the ohmic-type switches only, the dielectric charging failure mode affect both ohmic- and capacitive-type switches.

It has been decided that this thesis will focus on the problem of the dielectric charging in the ohmic-type switches which have been developed and fabricated by the CEA-Leti.

To investigate this failure mode, three intermediate objectives have been set:

- Study of the electromechanical behavior of the ohmic-type RF MEMS switches,
- Characterization of structural and electrical properties of the dielectrics in the RF MEMS switches,
- Modeling of dielectric charging and verification of the model.

1.2.4 Organization of thesis

The intermediate objectives which have been presented in the previous section, are reflected in the organization of this thesis, which is divided into 3 experimental chapters.

Table 1.6: Performance of ohmic- and capacitive-type RF MEMS switches from CEA-Leti

Parameter	Ohmic-type	Capacitive-type
Insertion loss [dB]	0.15 @ 5 GHz 0.3 @ 30 GHz	< 0.5
Isolation [dB]	36 @ 5 GHz 20 @ 30 GHz	20 @ 20 GHz
Bandwidth [GHz]	DC - 40	10-120
Actuation voltage [V]	15-25	25-40
Switching speed [µs]	0.5-2	
Switching cycles [1] [10^9]	250	250
Dielectric material	PECVD SiN_x	PECVD SiN_x or SiO_2
Dielectric thickness [nm]	400	250-300
Air gap [µm]	0.4 - 1	1.5-2
Beam length [µm]	340	300
Beam width [µm]	60	100
Beam thickness [µm]	0.7	0.5

[1] 100 Hz, 50% duty cycle, unipolar actuation

The first experimental chapter (Chapter 2) discusses the electro-mechanical behavior of the ohmic-type RF MEMS switches. This chapter presents an electro-mechanical model, which helps understanding the working principles of the RF MEMS switches and which is used, to investigate the influence of the material properties (*e.g.* residual stress) and the switch geometry on its electro-mechanical behavior. To validate this model a series of nanoindentations tests is carried out on the ohmic-type RF MEMS switches. The test results are then used to calculate the theoretical electrical responses of these switches, which are then compared with the measured responses.

In Chapter 3 the structural and electrical properties of the dielectrics are studied. In this part, the capacitive-type RF MEMS switches are investigated. These switches have been chosen because of two reasons: the first one is a higher number of available test structures, for the capacitive-type switches; the second one is a more simple switch geometry. It is worth pointing out, that in some of the investigated capacitive-type switches the same type of dielectric as in the ohmic-type switches (HF PECVD SiN_x) is used. The Chapter 3 is divided into two parts. The first part presents and discusses the results of structural and compositional analyses of PECVD SiN_x and SiO_2, which are then compared with the state-of-the-art. In the second part, the conduction mechanisms and trapping kinetics are identified thanks to I-V sweeps and constant current injections on MIM-capacitors[11]. Again, these results are discussed in the context of available literature data.

Chapter 4 addresses the problem of dielectric charging in RF MEMS switches. It starts with a concise review of existing approaches of modeling of the dielectric charging in RF MEMS switches. Next, it presents our original model of a parasitic charge build-up in a dielectric for a constant voltage stress. Using the dielectric properties identified in the previous chapter, the kinetics of charge build-up as a function of the voltage stress is calculated for 3 different types of

[11] MIM is an acronym for Metal-Insulator-Metal capacitor

dielectric (capacitive-type switches) and two switch designs (ohmic-type switches). These calculated voltage drift rates are compared with experimental results and after positive verification of the proposed model they are used to investigate the impact of material properties and switch design on kinetics of charge build-up.

The last Chapter 5 concludes this work and indicates the perspectives for a future work.

Chapter 2

Electro-mechanical behavior of MEMS switches

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2.1 Introduction

This chapter aims at explaining the electro-mechanical behavior of RF MEMS switches, with the ohmic-type switches used as a case study.

It starts with a presentation and discussion of two analytical models. The first one is an original mechanical model, which has been devised for a fixed-fixed switch with side electrodes. The second one is a standard electro-mechanical model, that has been adapted for the ohmic-type switches. These two models are used, in particular, to explain the operation of electrostatically actuated switches and to demonstrate the effect of material properties and switch geometry on their behavior.

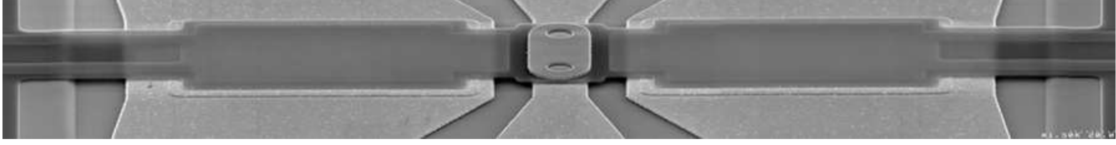
Next sections report the results of failure analysis which has been carried out on 4 characteristic wafers of ohmic-type switches. These analyses include: the measurements of the geometry and the topography (roughness) of the ohmic contacts and the top and the bottom electrodes, the measurements of the mechanical properties of the switches (stiffness) and the measurements of their typical electrical responses.

This chapter ends with a comparison of these experimental results with the theoretical responses calculated thanks to the electro-mechanical model.

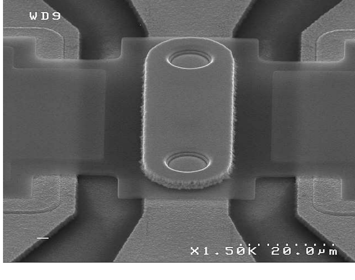
2.2 Test samples - general description

The ohmic-type switches fabricated by CEA-LETI are investigated throughout this chapter. These switches have been already presented in detail in the previous chapter, in section 1.2.2.1. Nevertheless, to remind the design of these switches, the Figure 2.1 presents SEM images of: the entire switch (a) and the mobile (b, c) and the fixed contacts (d).

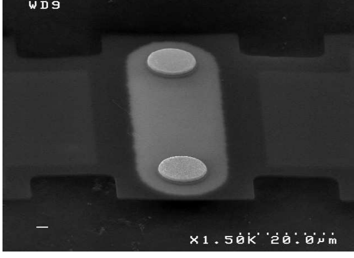
Switches for the tests have been selected from 4 characteristic manufacturing wafers, which are denoted as: ohm.A, ohm.B, ohm.C and ohm.D.



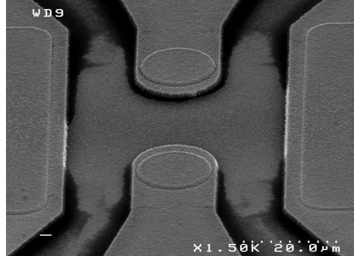
(a) Ohmic-type switch - general view



(b) Mobile contact - top view



(c) Mobile contact - bottom view



(d) Fixed contact

Figure 2.1: SEM images of the ohmic-type RF MEMS switch from CEA-LETI (ohm.D wafer)

Table 2.1: Summary of the main differences between wafers of ohmic-type switches

Parameter	Ohm.A	Ohm.B	Ohm.C	Ohm.D
Residual stress	Low	High	Medium	Low
g_c/g_0 ratio	High	Low	Medium	Medium
Mobile contact fabrications	Standard	Optimized	Optimized	Optimized

Table 2.1 presents a concise summary of the main differences between the investigated wafers:

- *Level of the residual stress σ_x in SiN_x*

  The residual stress is measured at the fabrication stage, for a given set of deposition parameters, by depositing a full-sheet layer of SiN_x on a wafer. By measuring the curvature of the wafer before and after the deposition, the value of the stress can be obtained from the following equation [15]:

$$\sigma_x = \frac{E_w t_w^2}{3\,(1-\nu_w)\,t_d} \frac{\delta_w}{\rho_w^2} \tag{2.1}$$

  where E_w is the Young's modulus of the wafer material, t_w is the thickness of the wafer, ν_w is the Poisson's ratio of the wafer material, t_d is the thickness of the dielectric, δ_w is the radial distance from the center of the wafer and ρ_w is the curvature difference before and after the deposition.

  The average value of the residual stress for our ohmic-type switches, measured at fabrication stage, is ∼300 MPa. This stress can be controlled by the deposition conditions. In our study, the lowest stress has been induced in the ohm.A wafer and the highest in the ohm.B wafer.

- *Contact (g_c) and electrode (g_0) gap heights*

  The contact and electrode gap heights are schematically presented in Figure 2.2. By optimizing these gap heights, it is possible to tune the electrical behavior of the switches. Requested gap heights are managed by controlling the etching depths.

  In the present case, the electrode gaps g_0 should all be below 1 µm and should be similar for all wafers. What differentiates the samples is the contact gap. The ohm.B wafer has the lowest contact gap, while the ohm.A wafer has the highest contact gap.

- *Fabrication process flow to realize the mobile contact*

  The quality of the ohmic contact is a limiting factor for the RF performance of the ohmic-type switches. In order to optimize the contact quality two fabrication processes have been used to fabricate the ohmic contacts of the investigated switches. These two processes are denoted here as a *standard* and an *optimized* process flow and are presented in detail in Table 2.2.

  The main difference concerns the method of etching the through hole in the SiN_x beam and the method of stripping of the resist (steps 3.1 and 3.2). For the standard process flow, a through hole is etched in the beam in one step. In the following step the resist is stripped off. However, while removing the resist the polymeric sacrificial layer (underneath SiN_x

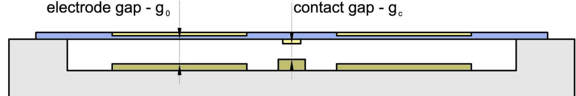


Figure 2.2: Contact and electrode gap heights in the ohmic-type switch

beam) is not protected and it deteriorates, which may result in an increased roughness of the mobile contact, sputtered on this sacrificial layer.

To avoid the deterioration of this polymeric sacrificial layer during removal of the resist, the process flow has been optimized in the following manner. First, instead of the through hole, a blind hole is etched in the beam, so that there remains a thin residual layer of SiN_x, which protects the sacrificial layer during stripping of the resist. After the stripping, the SiN_x is etched, to open the blind hole. By realizing the contact hole in two steps, it is then possible to protect the sacrificial layer, and to better control the roughness of the mobile contact.

In this study, the standard process flow is only used to realize the mobile contact of the ohm.A wafer. The optimized process flow is used for the remaining ohm.B, ohm.C and ohm.D wafers.

The mobile contacts, for all 4 wafers, are fabricated from sputtered gold.

The nominal geometrical dimensions and material properties of the ohmic-types switches are presented in Table 2.3.

2.3 Electro-mechanical model of a MEMS switch

2.3.1 Introduction

Analytical modeling of MEMS devices is a non-trivial task, as it often requires making many assumptions and simplifications, concerning the material properties and the geometry of the devices. These are inevitable sources of errors which have to be minimized. The task of modeling is further complicated by the fact that the material properties of MEMS are different from those of their bulk counterparts due to lower scale and different fabrication techniques.

For instance, a good example of a parameter which strongly influences the functioning of MEMS devices, and which is strongly dependent on the fabrication process is the residual stress. The residual stress is induced during deposition process but it can be further modified in subsequent fabrication steps including the post-deposition annealing. It has been reported [16, 17] that this parameter alone may have a significant influence on the electro-mechanical behavior of MEMS. Compressive stresses, for example, may be a source of initial deformations of mechanical parts, without any external load, which may lead to buckling, when the compressive stress exceeds Euler stress limit. On the other hand, tensile stresses cause beam stiffening. In some cases, for multilayered stacks, the difference of residual stresses in adjacent layers may result in cracking or delamination [18].

In this section we devise an original mechanical model, for a fixed-fixed switch with side electrodes. This model is then combined with a standard electrostatic model to describe the

Table 2.2: Standard and optimized process flows for fabrication of mobile contact

Step	Standard process	Optimized process
1	Deposition of mask, etching of contact impressions	
2	Etching of SiN_x and sacrificial layer	Etching of SiN_x
3.1	Stripping of mask	
3.2		Etching of SiN_x and sacrificial layer
4	Deposition of Au + etching (fabrication of mobile contact)	
5	Removing of sacrificial layer	

Table 2.3: Nominal parameters of the ohmic-type RF MEMS switch

Parameter	Symbol	Value
Switch length	l_s	340
Switch width	w_s	50 µm
Dielectric thickness - mechanical model[1]	t_d	600 nm
Dielectric thickness - electrostatic model[2]	t_d	400 nm
Surface of electrodes	A_{el}	6300 µm^2 $\times 2$
Distance to electrode center from support	d_{el}	95 µm
Nominal residual stress	σ_x	Tensile, 300 MPa
Young's modulus	E_m	200 GPa
Poisson's ratio	ν_m	0.3
Dielectric constant	ϵ_r	7.2 (for SiN_x)

[1] - the total thickness of the dielectric
[2] - the thickness of the dielectric below the top electrode

electro-mechanical behavior of the switch. Based on these two models we discuss the influence of the residual stress and the switch geometry on the theoretical electro-mechanical behavior.

2.3.2 Mechanical model

2.3.2.1 Literature review

A mechanical model of a microbeam describes the beam deflection as a function of an applied load.

The mechanical models can be split into two general categories: analytical and finite-element models (FEM) [19]. The main advantage of using analytical models is shorter computation time, while their main drawback is poor accuracy, as a result of simplifications of the geometry and material properties. On the other hand, there are FEM models, which require less simplifications and consequently produce more accurate results. Nevertheless, they may require significantly longer computation time. In this work, only the analytical model is presented.

The analytical models presented in the literature are calculated using either the Castiliagno's displacement theorem or Timoshenko method [20]. Depending on the ratio between the length, width and thickness of a microbeam, this may be considered as a one-dimensional beam (when $l_s \gg w_s$, t_s) or a two-dimensional plate (when $l_s \approx w_s \gg t_s$).

The models are available for single- and multilayer fixed-free or fixed-fixed beams of uniform width and thickness. The typical loading conditions are one concentrated normal load applied at the beam center or symmetrical distributed load. To simplify the calculations, some models ignore the residual stress and assume small deflections ($z_s < t_s$).

On the other hand, for more accurate solutions, some authors add the effect of the residual stress, which significantly complicates the analytical solution. In case the beam deflection exceeds its thickness, the most accurate models include also the contribution of the axial stretching force, which arises due to elongation of the deflected beam.

The Table 2.4 gives a non-exhaustive list of the types and main characteristics of the mechanical models of microbeams, available in the literature.

Table 2.4: Mechanical models available in the literature.

		Analytical	FEM
Beam type	fixed-free	[19]	[21, 22]
	fixed-fixed	[18, 19, 23–26]	[16, 21, 27–29]
Load type	concentrated	[18, 19, 23–25]	[21]
	distributed	[26]	[16, 22, 27–29]
Parameters	residual stress	[18, 23, 25, 26]	[16, 27–29]
	axial stretching	[19, 23, 24, 26]	

In our case, to study the behavior of the ohmic-type switches, one needs a model of a fixed-fixed beam with tensile residual stress under one or multiple normal concentrated loads, applied at any position along the beam length x_s. As such a model is not available in the literature, it will be derived in the following section.

2.3.2.2 Derivation of a mechanical model

Introduction
In this section, we devise an original analytical formula for calculating the deflection curve of a beam with build-in ends, under normal and axial forces. This mechanical model includes the main characteristics of the ohmic-type RF MEMS switches fabricated by CEA-LETI, which are: two normal forces corresponding to electrostatic actuation forces applied to side electrodes and axial stretching forces representing the effect of residual stress.

Deflection curve - one concentrated normal load
The mechanical model includes the following assumptions and simplifications:

- This model is based on the elastic beam theory, which is valid when the beam length is much larger than its width and thickness (*i.e.* the Euler-Bernoulli limit is satisfied) and no plastic deformation is assumed.
- The switch is approximated by a fixed-fixed, single-layer beam with a rectangular cross-section, uniform width and thickness. The switch is initially planar and parallel to the bottom electrode.
- The tensile residual stress, which is represented by the axial stretching forces T_r applied at both ends, is calculated as $T_r = \sigma_x A_{sec}$, where A_{sec} is the surface of the cross-section of the beam. The residual stress is uniaxial along the beam length x_s and is completely released along the beam width and thickness directions.
- Stretching axial forces due to beam deflection are neglected as the maximum deflections are comparable to the beam thickness.
- The electrostatic forces can be reduced to concentrated normal forces applied in the geometrical centers of the electrodes, that is at the distances d_1 and d_2 from a support.
- The positive direction of z-axis is downward.

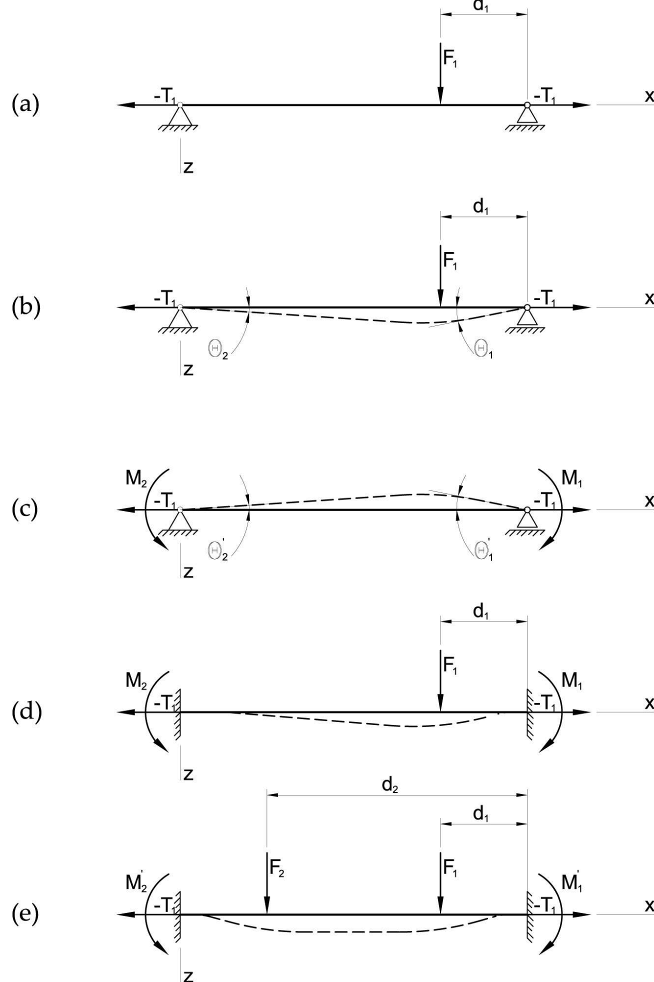


Figure 2.3: Mechanical model: schematic representation of the ohmic-type RF MEMS switch with two side electrodes; (a)-(d) simplified loading conditions to calculate partial solutions , (e) complete loading conditions to calculate final model

A beam with build-in ends is an example of an overrigid beam, which is statically indeterminate. It means that it is not possible to determine all the reactions in the supports from the equations of statics only. To solve this problem additional equations have to be found from consideration of the beam bending. To solve the stated problem of calculating the deflection z_s of the overrigid beam, it is necessary to find the partial solutions for a simplified loading and support conditions and then the final generic solution is found as a superposition of these partial solutions [20].

The method of superposition used hereafter is based on the fact that the deflection of a beam at a point is defined by the bending moment at this point only. It is known from the definition of the bending moment that the bending moment produced at a given point by several simultaneously acting loads is equal to the sum of the moments produced at this point by the individual loads acting separately. Hence, the deflection at a point produced by a system of simultaneously acting loads can be obtained by summing up the deflection at this point produced

by each load acting alone [20].

In the present case, where bending of a beam is combined with axial tension, this method is limited to the normal loads, assuming that the axial forces remain constant. Thus, the deflection in our case, for two normal loads, will be found as a sum of deflections caused by each normal load separately. The first partial solution, for a simply-supported beam with one normal load F_n applied at a distance d_n (see Figure 2.3(a)) is presented below.

As it has been already mentioned, the curvature of the deflection curve at any point depends only of the magnitude of the bending moment at that point. Hence, the differential equation of the deflection curve for the left and right parts of the beam are:

$$E_m I_z \frac{d^2 z_s}{dx^2} = T_r z_s - \frac{F_n d_n}{l_s} x_s \tag{2.2}$$

$$E_m I_z \frac{d^2 z_s}{dx^2} = T_r z_s - \frac{F_n (l_s - d_n)}{l_s} (l_s - x_s) \tag{2.3}$$

where E_m is the Young's modulus of the material, I_z is the moment of inertia of a plane figure, T_r is the axial stretching force representing the effect of the residual stress, z_s is the deflection of the beam, F_n is the nth concentrated normal forces applied at the distances d_n from a support, l_s is the length of the beam and x_s is the lateral position along the beam length. By substituting:

$$p^2 = \frac{T_r}{E_m I_z} \tag{2.4}$$

the general solutions of the equations 2.2 and 2.3 can be rewritten in the following form:

$$z_s = C_1 \cosh p x_s + C_2 \sinh p x_s + \frac{F_n d_n}{T_r l_s} x_s \tag{2.5}$$

$$z_s = C_3 \cosh p x_s + C_4 \sinh p x_s + \frac{F_n (l_s - d_n)}{T_r l_s} (l_s - x_s) \tag{2.6}$$

Here C_n is the nth constant.

The values of the C_n constants are found from the following boundary conditions. As the deflections vanish at the ends of the beam, thus C_1 and C_3 are:

$$C_1 = 0 \tag{2.7}$$

$$C_3 = -C_4 \tanh p l_s C_2 \tag{2.8}$$

The remaining integration constants are found from the conditions of continuity. This requires that the deflection at the point, where the normal load is applied, is the same when calculated from the equation for the left 2.2 and for the right part 2.3 of the beam, for $x_s = l_s - d_n$, which is:

$$C_2 \sinh p(l_s - d_n) = C_4 \left[\sinh p(l_s - d_n) - \tanh pl_s \cosh p(l_s - d_n)\right] \tag{2.9}$$

$$C_2 p(l_s - d_n) = C_4 p \left[\cosh p(l_s - d_n) + \tanh pl_s \sinh p(l_s - d_n)\right] + \frac{F_n}{T_r} \tag{2.10}$$

Finally, after necessary transformations, the constants C_2 and C_4 are:

$$C_2 = \frac{F_n \sinh pd_n}{T_r p \sinh pl_s} \tag{2.11}$$

$$C_4 = -\frac{F_n \sinh p(l_s - d_n)}{T_r p \tanh pl_s} \tag{2.12}$$

Taking all above into account, the deflection curve of a simply supported beam, with one normal force F_n applied at the distance d_n and two axial stretching forces T_r (Figure 2.3(a)) is:

$$z_s = -\frac{F_n \sinh pd_n}{p \sinh pl_s} \sinh px_s + \frac{F_n d_n}{T_r l_s} x_s \tag{2.13}$$

$$z_s = -\frac{F_n \sinh p(l_s - d_n)}{T_r p \sinh pl_s} \cosh p(l_s - x_s) - \frac{F_n(l_s - d_n)}{T_r l_s}(l_s - x_s) \tag{2.14}$$

The deflection curve given by the equations 2.13 and 2.14 is valid for a simply supported beam. In case of a beam with built-in ends there are additional reactions in the supports. In our case these are the force moments M_A and M_B. The additional stretching component due to bending of the beam can be neglected for ordinary beams, where the maximal deflection is comparable with thickness of the beam, as it is in our case [20].

To find the moments M_A and M_B the following approach is applied. The slopes of the beam due to one concentrated normal load are calculated, as well as the slopes of the beam due to two moments in the absence of the normal load. The conditions at the built-in ends are satisfied if the sum of the slopes calculated in these two cases is equal to zero, thus the beam remains straight at the ends:

$$\theta_1 = -\theta_1{}' \tag{2.15}$$

$$\theta_2 = -\theta_2{}' \tag{2.16}$$

The slopes calculated as the first derivative of the equations 2.13 and 2.14 are:

$$\frac{dz}{dx} = -\frac{F_n \sinh pd_n}{T_r \sinh pl_s} \cosh px + \frac{F_n d_n}{T_r l_s} \tag{2.17}$$

$$\frac{dz}{dx} = \frac{F_n \sinh p(l_s - d_n)}{T_r p \sinh pl_s} \cosh p(l_s - x_s) - \frac{F_n(l_s - d_n)}{T_r l_s} \tag{2.18}$$

and in the supports they are equal to:

$$\left(\frac{dz}{dx}\right)_{x_s=0} = -\frac{F_n \sinh pd_n}{T_r \sinh pl_s} + \frac{F_n d_n}{T_r l_s} \tag{2.19}$$

$$\left(\frac{dz}{dx}\right)_{x_s=l_s} = \frac{F_n \sinh p(l_s - d_n)}{T_r \sinh pl_s} - \frac{F_n(l_s - d_n)}{T_r l_s} \tag{2.20}$$

From the solution for one normal load, a deflection curve for a beam bending by a force moment at its end can be obtained assuming that the distance d_n, is approaching zero, and $F_n d_n$ remains constant and is equal to force moment at the end M_n. In a particular case, when the normal force F_n is applied in the middle of the beam ($d_n = l/2$) the two moments M_A and M_B are equal and can be reduced to the moment M_0, which is:

$$z_s = \frac{M_0}{T_r}\left(\frac{x_s}{l_s} - \frac{\sinh px_s}{\sinh pl_s}\right) \tag{2.21}$$

In case, there are two opposite and equal moments M_0 the total beam bending is:

$$\begin{aligned} z_s &= \frac{M_0}{T_r}\left(\frac{x_s}{l_s} - \frac{\sinh px_s}{\sinh pl_s}\right) + \frac{M_0}{T_r}\left[\frac{l_s - x_s}{l_s} - \frac{\sinh p(l_s - x_s)}{\sinh pl_s}\right] \\ &= \frac{M_0}{T_r}\left[1 - \frac{\cosh\left(p\left(\frac{l_s}{2} - x_s\right)\right)}{\cosh\left(\frac{pl_s}{2}\right)}\right] \end{aligned} \tag{2.22}$$

from which the slope at the ends of the beam, is:

$$\left(\frac{dz}{dx}\right)_{x=0} = \frac{M_0 l_s \tanh(u)}{2E_m I_z u} \tag{2.23}$$

Here u is equal to:

$$u^2 = \frac{T_r l_s^2}{4EI} = \frac{(pl_s)^2}{4} \tag{2.24}$$

and I_z is the moment of inertia for a rectangular beam, given by the equation:

$$I_z = \frac{w_s t_s^3}{12} \tag{2.25}$$

For a fixed-fixed beam, the slope due to normal concentrated load F_n, calculated from the equation 2.19 is canceled by the slope due to force moment M_0 calculated from the equation 2.23, thus:

$$-\frac{F_n \sinh(pd_n)}{T_r \sinh(pl_s)} + \frac{F_n d_n}{T_r l_s} + \frac{M_0 l_s \tanh(u)}{2E_m I_z u} = 0 \tag{2.26}$$

The force moment M_0 is then found to be equal to:

$$M_0 = F_n \left(\frac{2E_m I_z u}{l_s \tanh(u)} \right) \left[\frac{\sinh(pd_n)}{T_r \sinh(pl_s)} - \frac{d_n}{T_r l_s} \right] \tag{2.27}$$

Finally, the deflection curve of the fixed-fixed beam with one normal concentrated load at the beam center, can be expressed as:

$$z_s = -\frac{F_n \sinh(pd_n)}{T_r p \sinh(pl_s)} \sinh(px_s) + \frac{F_n d_n}{T_r l_s} + \frac{M_0}{T_r} \left[1 - \frac{\cosh\left(p\left(\frac{l_s}{2} - x_s\right)\right)}{\cosh\left(\frac{pl_s}{2}\right)} \right] \tag{2.28}$$

The central load is the typical loading condition, but it is not the case for the ohmic-type switches investigated here, which have two side electrodes. When the normal concentrated load is applied away from the beam center, the force moments at its ends are not equal. Thus, the deflection due to two unequal force moments M_A and M_B is:

$$z_s = \frac{M_A}{T_r} \left(\frac{x_s}{l_s} - \frac{\sinh(px_s)}{\sinh(pl_s)} \right) + \frac{M_B}{T_r} \left[\frac{l_s - x_s}{l_s} - \frac{\sinh(p(l_s - x_s))}{\sinh(pl_s)} \right] \tag{2.29}$$

and the slope of the deflection curve, calculated from the equation 2.29 is:

$$\frac{dz}{dx} = \frac{M_A}{T_r} \left[\frac{1}{l_s} - \frac{p \cosh(px_s)}{\sinh(pl_s)} \right] + \frac{M_B}{T_r} \left[\frac{p \cosh(p(l_s - x_s))}{pl_s)} - \frac{1}{l_s} \right] \tag{2.30}$$

The slopes calculated in both built-in the ends are:

$$\left(\frac{dz}{dx} \right)_{x=0} = \frac{M_A}{T_r} \left[\frac{1}{l_s} - \frac{p}{\sinh(pl_s)} \right] - \frac{M_B}{T_r} \left[\frac{1}{l_s} - \frac{p \cosh(pl_s)}{\sinh(pl_s)} \right] = M_A \alpha + M_B(-\beta) \tag{2.31}$$

$$\left(\frac{dz}{dx} \right)_{x_s=l_s} = \frac{M_A}{T_r} \left[\frac{1}{l_s} - \frac{p \cosh(pl_s)}{\sinh(pl_s)} \right] - \frac{M_B}{T_r} \left[\frac{1}{l_s} - \frac{p}{\sinh(pl_s)} \right] = M_A \beta + M_B(-\alpha) \tag{2.32}$$

With the following substitutions made in the equations 2.32 and 2.32:

$$\alpha = \frac{1}{l_s} - \frac{p}{\sinh(pl_s)} \tag{2.33}$$

$$\beta = \frac{1}{l_s} - \frac{p \cosh(pl_s)}{\sinh(pl_s)} \tag{2.34}$$

The force moments M_A and M_B can be expressed, in the following compacted form:

$$M_A = \frac{\alpha\theta_1 - \beta\theta_2}{\beta^2 - \alpha^2} \tag{2.35}$$

$$M_B = \frac{\beta\theta_1 - \alpha\theta_2}{\beta^2 - \alpha^2} \tag{2.36}$$

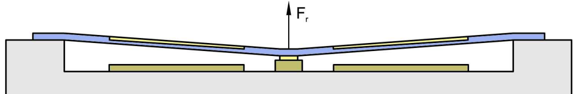


Figure 2.4: Restoring force

Finally, the deflection curve of a fixed-fixed beam with one concentrated normal load applied outside the beam center, with axial stretching forces, can be expressed as:

$$\begin{aligned} z_s = & -\frac{F_n \sinh(pd_n)}{T_r p \sinh(pl_s)} \sinh(px_s) + \frac{F_n d_n}{T_r l_s} \\ & + \frac{M_A}{T_r} \left[\frac{x_s}{l_s} - \frac{\sinh(px_s)}{\sinh(pl_s)} \right] + \frac{M_B}{T_r} \left[\frac{l_s - x_s}{l_s} - \frac{\sinh(p(l_s - x_s))}{\sinh(pl_s)} \right] \end{aligned} \quad (2.37)$$

Deflection curve - multiply concentrated normal loads
In a general case, when n concentrated normal forces are acting on a fixed-fixed beam, the deflection curve can be obtained as a superposition of the deflection curves, for each of the concentrated loads. Instead of writing the equation of the deflection curve, it is good to introduce the notion of stiffness k_s, which is the resistance of a beam to deformation z_s under an external force:

$$k_s = \frac{F_{mech}}{z_s} \quad (2.38)$$

The stiffness $k_s(x_s)$ of a beam along its length, for multiple normal forces, can be expressed as:

$$k_s\left(x_s\right) = \frac{\sum_n F_n}{\sum_n z_n\left(d_n, F_n\right)} \quad (2.39)$$

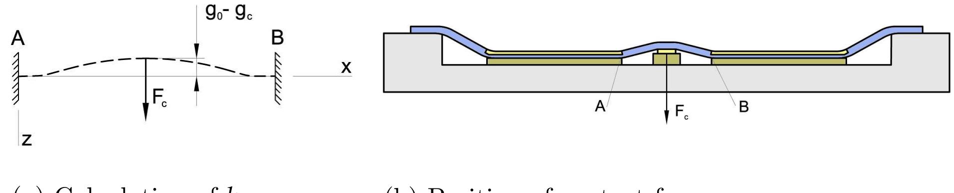
2.3.2.3 Calculation of mechanical force

When an elastic beam is deflected it gains mechanical force, which is proportional to the deflection z_s and the stiffness of the beam k_s:

$$F_{mech} = k_s z_s \quad (2.40)$$

In the particular case of the ohmic-type RF MEMS switches, there are two mechanical forces, which are important for correct functioning of the device: a restoring and a contact force.

Restoring force
The restoring force F_r is presented schematically in Figure 2.4. It acts in opposite direction to the electrostatic downward force F_{el} and is responsible for retracting the beam to its initial, undeflected position, when voltage bias is removed.



(a) Calculation of k_{F_c} (b) Position of contact force

Figure 2.5: Contact force

The restoring force is a product of the beam stiffness at the beam center k_c times contact gap g_c:

$$F_r = k_c g_c \tag{2.41}$$

An insufficient restoring force may result in a permanent stiction, which corresponds to a beam remaining permanently in the down-state (closed) position.

Contact force

The contact force F_c is presented schematically in Figure 2.5(b). The contact force F_c acts in the same direction as the electrostatic force, and this is the force at which the mobile contact of an ohmic-type switch is pressed to the fixed contact. This force may have an effect on the resistance of the ohmic contact, hence it may influence the RF performance of the switch (*e.g.* the insertion loss).

To calculate the approximate contact force, it is assumed that the electrostatic force is high enough to put the top electrodes in contact with the bottom electrodes along their entire lengths. Consequently, the approximate value of F_c can be obtained as a product of the stiffness k_{F_c} of the beam, at its center, when the top electrodes adhere to the bottom ones, multiplied by the deflection of the beam, which is here the difference between the electrode and the contact gap heights $g_0 - g_c$:

$$F_c = k_{F_c} \left(g_0 - g_c\right) \tag{2.42}$$

To calculate the stiffness k_{F_c}, the mechanical model for one normal load is used, where the stiffness is calculated at a center of a 45 μm-long fixed-fixed beam (the 45 μm is the distance between the ends of the left and right electrodes, which are denoted as A and B in Figure 2.5(a)).

Bearing in mind all the simplifications in this model, it should be noted that the equation (2.42) can be used only for a rough estimation of the order of magnitude of the contact force, rather than a precise calculation.

2.3.3 Standard electrostatic model

2.3.3.1 Calculation of switch capacitance

An electrostatic RF MEMS switch can be modeled, with satisfactory approximation, as a parallel-plate capacitor. The electrostatic force is generated between the top and bottom metallic plane-electrodes, separated by a distance $t_d + g_0$, where t_d is the thickness of the dielectric

and g_0 is the air gap (the electrode gap). The switch capacitance C_s of such a system is equal to:

$$\begin{aligned}\frac{1}{C_s} &= \frac{1}{C_0} + \frac{1}{C_d} \\ &= \frac{g_0 - z_s}{\epsilon_0 A_{el}} + \frac{t_d}{\epsilon_0 \epsilon_r A_{el}} \\ &= \frac{\epsilon_r (g_0 - z_s) + t_d}{\epsilon_0 \epsilon_r A_{el}} \end{aligned} \tag{2.43}$$

where C_0 is the capacitance of an air-capacitor and C_d is the capacitance of a capacitor with a dielectric. Finally the switch capacitance, between a pair of a top and bottom electrode can be expressed as:

$$C_s = \frac{\epsilon_0 A_{el}}{g_0 - z_s + \frac{t_d}{\epsilon_r}} \tag{2.44}$$

During a commutation cycle, the ohmic-type switch may take up to three characteristic positions, which are presented schematically in Figure 2.6. Each of these positions correspond to a characteristic value of the switch capacitance:

- *Up-state capacitance* C_{up}

  When no voltage is applied across the actuation electrodes, the switch remains in its initial, undeflected position (up-state), as presented in Figure 2.6(a). The air gap between the top and the bottom electrodes is maximum, thus the capacitance is minimum. This is a stable position.

- *Down state capacitance* C_{dn}

  When the applied voltage is higher than the pull-in voltage, the top electrodes collapse and remain in contact with the bottom electrodes (down-state), as presented in Figure 2.6(b). The air gap between the top and the bottom electrodes is minimum, thus the capacitance is maximum. This is a stable position.

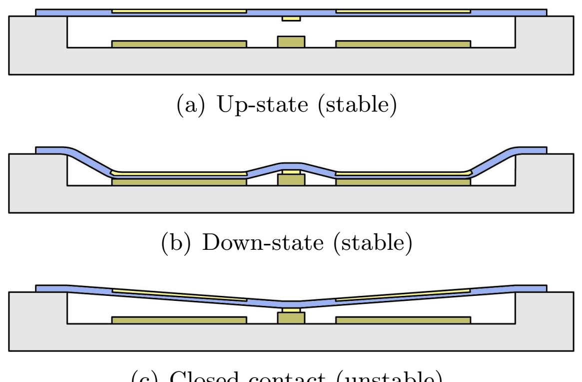
- *Closed-contact capacitance* C_{pi}

  In a particular case, when the contact gap g_c is lower than 1/3 of the electrode gap g_0, the ohmic contact can be closed before the electrodes collapse, as presented in Figure 2.6(c). In this figure, the beam is in an intermediate position between the up- and the down-state, so is the capacitance. This is an unstable position, as the top electrodes may still collapse (down-state).

2.3.3.2 Calculation of electrostatic force

The electrostatic energy W_c stored in a capacitor is equal to:

$$W_c(z) = \frac{C_s V_{app}^2}{2} \tag{2.45}$$



(a) Up-state (stable)

(b) Down-state (stable)

(c) Closed contact (unstable)

Figure 2.6: Characteristic positions of ohmic-type switches during commutation

where V_{app} is the voltage applied to the capacitor.

The electrostatic force is obtained by differentiating the energy W_c, with respect to the vertical position of the beam (z_s) and it is proportional to the square of the applied voltage:

$$\begin{aligned} F_{el}(z) &= -\frac{\partial W_c}{\partial z} \\ &= \frac{\epsilon_0 A_{el} V_{app}^2}{\left(\frac{t_d}{\epsilon_r} + g_0 - z_s\right)^2} \end{aligned} \tag{2.46}$$

2.3.4 Combined electro-mechanical model

An electrostatic RF MEMS switch, either of ohmic or capacitive type, is composed of a mobile beam suspended over an RF-signal transmission line and/or bottom actuation electrodes. To actuate such a switch, a voltage is applied between the beam and the transmission line or the actuation electrodes. The minimum voltage required to collapse the switch is called a pull-in voltage and is denoted as V_{pi}.

2.3.4.1 Literature review

A comprehensive review of existing approaches in electro-mechanical modeling of RF MEMS switches is presented in [23, 30].

The electro-mechanical models available in the literature can be summarized in one generic equation:

$$E_m I_z \frac{\partial^4 z}{\partial x^4} - (T_r + T_a)\frac{\partial^2 z}{\partial x^2} = \frac{\epsilon_0 V_{app}^2 A_{el}}{2(g_0 - z_s)^2}\left(1 + f_f\right) \tag{2.47}$$

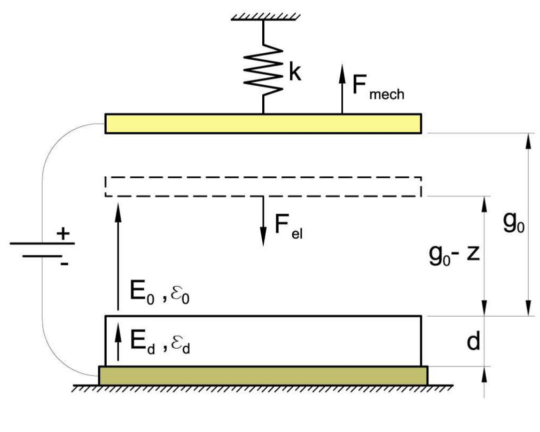


Figure 2.7: Schematic diagram of switch for electro-mechanical model

The left part of this equation 2.47 corresponds to the mechanical model of a beam, while the right part corresponds to the electrostatic model.

What differentiates the electro-mechanical models, presented in the literature is the mechanical-part of the equation, which is used to calculate a beam deflection. Not only the deflection curve can be calculated for different geometries, and different loading conditions, such as concentrated, or distributed normal loads, but it may also include the effects of residual-stress T_r or axial stretching from beam bending T_a.

On the other hand, the electrostatic part of the electro-mechanical model, is practically the same in all publications. The switch is typically approximated by a parallel plate capacitor. This approximation is true when the gap between the actuation electrodes is small compared to their surface dimensions. More accurate electrostatic models include the fringing field correction f_f. The impact of the fringing field on the switch capacitance has been studied, in particular in [22, 28, 29] and the authors conclude that for high width to gap ratios the fringing field correction can be neglected as the total switch capacitance approaches the parallel-plate model. On the other hand for a width to gap ratio below 1.5 the fringing field component becomes dominant and it can increase the overall capacitance by a factor of 1.5 to 3 for small widths.

Consequently, the electro-mechanical model, which is derived here, is different in terms of the mechanical part, while the electrostatic part use the common parallel-plate capacitor approximation.

2.3.4.2 Electro-mechanical model

To actuate the switch a voltage is applied between the top and the bottom electrodes as presented on a schematic diagram in Figure 2.7. The resulting downward electrostatic force F_{el} (Equation 2.46) starts deflecting the beam. When the applied voltage is low enough, the deflection due to electrostatic force is balanced by the upward mechanical restoring force F_{mech} (Equation 2.40):

$$F_{el}(z) = F_{mech}(z) \tag{2.48}$$

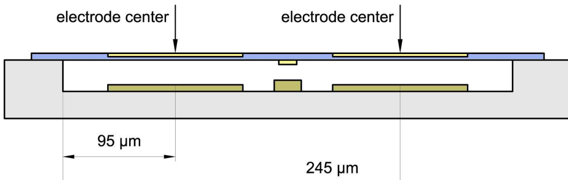


Figure 2.8: Position of electrodes centers (d_1 and d_2) in the ohmic-type switch, where concentrated normal loads (F_N) are applied.

The solution of this equation, with respect to voltage, for the ohmic-type switch is:

$$V = \left(g_0 - z_s + \frac{t_d}{\epsilon_r}\right)\sqrt{\frac{k_{c_{2F}} z_s}{2\epsilon_0 A_{el}}} \tag{2.49}$$

Here $k_{c_{2F}}$ is the stiffness at the beam center, when two normal concentrated loads are simultaneously applied at the electrodes centers, as presented in Figure 2.8. This corresponds to the situation when two electrostatic forces act simultaneously on the top electrodes, for electrostatic actuation. It is worth noticing, that the stiffness $k_{c_{2F}}$ is higher than the stiffness k_c, when one normal load is applied at the beam center (this will be discussed in more detail later in this section).

The equation (2.49) can also be used to calculate the pull-in voltage V_{pi} of the switches. The value of V_{pi} is obtained as the maximum voltage value, which is satisfying the equation (2.49) for z_s ranging from 0 (up-state) to g_0 (down-state position). This is presented in more detail in paragraph 2.3.5.3.

2.3.5 Discussion

2.3.5.1 Mechanical model

Influence of load position on beam stiffness

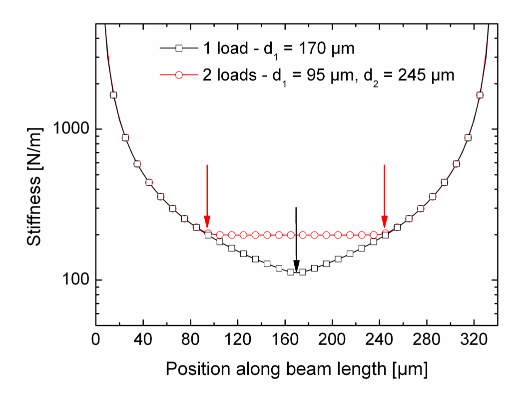
The mechanical model has been used to calculate the stiffness of the beam, for the nominal dimensions and material properties as summarized in the Table 2.1.

Figure 2.9(a) presents the stiffness as a function of the position along the beam x_s for one and two concentrated normal loads .

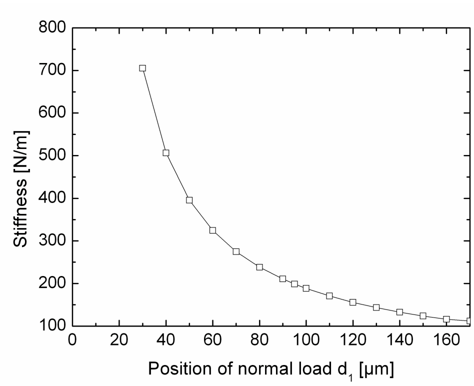
When one concentrated normal load is applied at the beam center, the nominal stiffness at the beam center is $k_c = 112$ N/m. When one concentrated normal load is applied at the geometrical center of an electrode, the stiffness at the center of the electrode is $k_{el} = 142$ N/m. The stiffness k_{el} is approximately 1.27 times higher than the stiffness k_c.

When two normal loads are applied simultaneously at the geometrical centers of the electrodes, that is at the distances $d_1 = 95$ μm and $d_2 = 245$ μm from a built-in end, the nominal stiffness at the beam center is $k_{c_{2F}} = 199$ N/m and the stiffness at the electrode centers, where the loads are applied, is $k_{el_{2F}} = 204$ N/m, virtually the same as at the beam center. This stiffness $k_{c_{2F}}$ is roughly 1.8 times higher than the stiffness k_c at the beam center.

Figure 2.9(b) presents the stiffness at the beam center $k_{c_{2F}}$, when two normal concentrated symmetrical loads are applied simultaneously at the distance d_1 from the supports. It is apparent



(a) Beam stiffness for 1 concentrated normal load applied at beam center and 2 concentrated normal loads applied at electrode centers



(b) Stiffness at beam center $k_{c_{2F}}$ for 2 concentrated normal symmetrical loads applied simultaneously at distance d_1 from supports, plotted as a function of the distance d_1

Figure 2.9: Influence of position and number of the normal concentrated loads on the beam stiffness

that the stiffness $k_{c_{2F}}$ increases as the distance d_1 decreases, that is the loads are applied closer to the built-in ends. This has an important consequence for switch functioning. To obtain the same deflection at the beam center, less force is required when the force is applied directly at the beam center rather than at the sides.

It implies, that in case of a switch with the side electrodes, the pull-in voltage is higher, than it would be in the case the actuation electrode was located under the beam center.

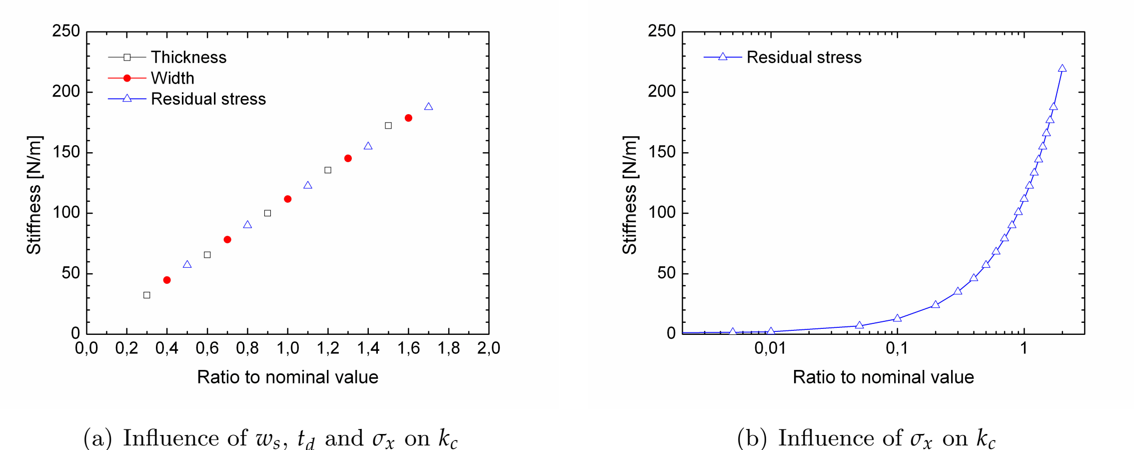
For the nominal ohmic-type switch, where the stiffness $k_{c_{2F}}$ is almost 1.8 times higher than the k_c, the force necessary to close the switch has to be at least 1.8 times higher than it would be in the case the actuation electrode was located at the beam center.

Influence of geometry and material properties on beam stiffness

The beam stiffness depends on its geometry and the material properties. The parameters that can be easily modified or adjusted for the investigated ohmic-type switches are the beam width and its thickness and the level of the residual stress.

When these three parameters are varying (one at a time) within 0.5 to 1.5 of their nominal values given in Table 2.1, the switch stiffness k_c at the beam center, for one central normal concentrated load varies as presented in Figure 2.10(a). From this figure, it turns out that all the analyzed parameters have a linear influence on the stiffness and none of them is dominating, within the investigated range.

Figure 2.10(b) presents the stiffness k_c at the beam center, as a function of the residual tensile stress in the beam. In case of zero residual stress, the stiffness k_c drops to approximately 1 N/m, instead of the nominal 112 N/m. This emphasizes how important it is to control the level of the induced residual stresses. For a switch, such a low stiffness would be advantageous to the pull-in voltage, which would be lower than the nominal one. The main drawback of such a low stiffness, would be a much lower restoring force, compared to the nominal one. Consequently, for correct functioning of the switch, it is necessary to find a good balance between the accepted



(a) Influence of w_s, t_d and σ_x on k_c

(b) Influence of σ_x on k_c

Figure 2.10: Influence of the thickness t_d, the width w_s and the residual stress σ_x on the stiffness k_c at the beam center

pull-in voltage and the restoring force, which can be practically realized by adjusting the residual stress.

2.3.5.2 Electrostatic model

The electrostatic model alone is used to calculate the capacitance of the switches. Figure 2.11 presents the capacitance of the ohmic-type switches as a function of vertical displacement of the top electrodes. This capacitance is calculated for 3 initial electrode gaps g_0 equal to 500 nm, 750 nm, 1000 nm, which are of the same order of magnitude, as for the investigated switches.

The up-state capacitance C_{up} is approximately 0.12-0.21 pF, depending on the initial electrode gap. The down-state capacitance C_{dn} is approximately 1.95 pF, thus the C_{dn}/C_{up} ratio is comprised between 10 and 20.

The capacitance is a non-linear function of the vertical displacement z_s of the top electrode. The increment of the capacitance increases faster with increasing displacement. For instance, in the middle of the initial gap g_0 the capacitance is only twice as high as C_{up}, while in the down-state it can be 10 to 20 times higher. As a result, the switch capacitance can be effectively used, to evaluate the state (the roughness) of the contacting surfaces of the top and bottom electrodes in the ohmic-type switches. For smooth surfaces, the residual air gap between these electrodes, in the down-state is small, thus the measured C_{dn}/C_{up} ratio is high. On the other hand, for rougher contacting surfaces, the residual air gap in the down-state is higher, which results in lower C_{dn}/C_{up} ratio.

2.3.5.3 Electro-mechanical model

Calculation of pull-in voltage

Figure 2.12(a) presents the electrostatic and the mechanical forces, plotted as a function of the deflection of the top electrode z_s. The electrostatic force is plotted for voltages below, equal to and above the V_{pi}. The mechanical force is plotted for 0.75, 1 and 1.25 of the nominal

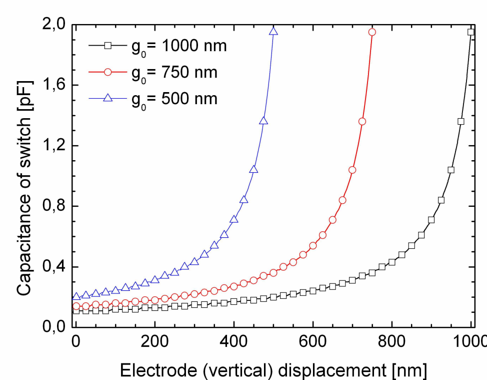


Figure 2.11: Calculated capacitance of the ohmic-type switch as a function of electrode displacement, calculated for 3 initial electrode gaps.

stiffness value. These calculations are carried out for the nominal ohmic-type switch, for an initial electrode gap $g_0 = 750$ nm. It is possible to distinguish four characteristic cases:

- *No voltage is applied* ($V_{app} = 0$)
  When no voltage is applied across the actuation electrodes, the beam is in the up-state position. As there is no initial deflection, thus the mechanical (restoring) force $F_{mech} = 0$.

- *Applied voltage is lower than pull-in voltage* ($V_{app} < V_{pi}$)
  When a voltage V_{app} is applied across the actuation electrodes, it generates an initial electrostatic force. Because the initial mechanical force is zero, the electrostatic force is starting to deflect the beam. As the beam is deflecting, the mechanical and electrostatic forces increase. In case, the applied voltage V_{app} is lower than the pull-in voltage V_{pi}, the electrostatic force increases slower than the mechanical force. Consequently, there is a stable beam position where the electrostatic force is equal to the mechanical force, thus the beam cannot deflect any farther. This position corresponds to the first intersecting point for the F_{el} and F_{mech} plots, presented in 2.12(a) for the applied voltages $V_{app} = 4$ and 8 V.

  In Figure 2.12(b) this stable position of the beam, calculated from equation 2.49, is plotted as a function of the applied voltage, for three initial electrode gaps g_0.

- *Applied voltage is equal to pull-in voltage* ($V_{app} = V_{pi}$)
  When the applied voltage V_{app} is equal to the pull-in voltage V_{pi}, the F_{el} and F_{mech} plots have only one intersecting point. In our case it corresponds to the $V_{app} =\sim 12$ V (Figure 2.12(a)).

- *Applied voltage is higher than pull-in voltage* ($V_{app} > V_{pi}$)
  Any farther increase of the voltage V_{app} above the value of V_{pi} results in such an increase of the electrostatic force which cannot be balanced by the mechanical force. As a result the beam collapses, which is known as a pull-in phenomenon. In our example this situation occurs for voltages $V_{app} = 14$ and 18 V (Figure 2.12(b)).

The results presented in Figure 2.12(b) have practical implications on finding the pull-in voltage. In this Figure, we can see that the pull-in phenomenon occurs at a deflection of roughly 1/3 of the electrode gap g_0. Consequently the pull-in voltage V_{pi} can be obtained from the equation 2.49 by substituting the value of z_s in equation by $1/3g_0$. Obviously, this value of V_{pi} is true for switches, where $g_c > 1/3g_0$, thus the contact is closed after the pull-in.

When the $g_c < 1/3g_0$ the voltage required to close the ohmic contact is lower than the value of the pull-in voltage V_{pi} and is denoted as V_{pi_R}. In case, the applied voltage $V_{app} = V_{pi_R}$ the ohmic contact is closed, but the top electrodes are not collapsed, thus the position of the top electrodes is unstable.

Influence of stiffness and electrode gap on pull-in voltage
In case of the ohmic-type switches, the pull-in voltage depends, in general, on three parameters.

1. The stiffness of the switch, where a higher stiffness translates to a higher pull-in voltage.
2. The electrode gap, where the higher the gap, the higher the V_{pi}.
3. The surface of the actuation electrodes, where a higher surface increases the electrostatic force, hence decreases the pull-in voltage.

This paragraph presents how the stiffness and the electrode-gap heights influence the pull-in voltage of the nominal ohmic-type switch. The pull-in voltage is calculated from the equation (2.49), as the maximum voltage for beam deflection z_s ranging from 0 to g_0. The stiffness, which is put in the equation, is the stiffness at beam center $k_{c_{2F}}$, when 2 normal concentrated loads are applied at the electrode centers.

Figure 2.12(a) presents the influence of the switch stiffness on the mechanical force, compared to the electrostatic force. In this figure the mechanical force is plotted for 0.75, 1 and 1.25 of its nominal value. From this figure it is clear, that increasing the stiffness results in higher gradients of the mechanical force, while the electrostatic force gradients remain unchanged. As a result, a higher mechanical force (due to the increased stiffness) can balance a higher electrostatic force. Consequently, it leads to an increase of the pull-in voltage.

The pull-in voltage, plotted as a function of the switch stiffness is presented in Figure 2.13(a), where the stiffness $k_{c_{2F}}$ is ranging from 0.2 to 2 of its nominal value. Within this range, the corresponding pull-in voltages vary almost linearly from 8 to 26 V.

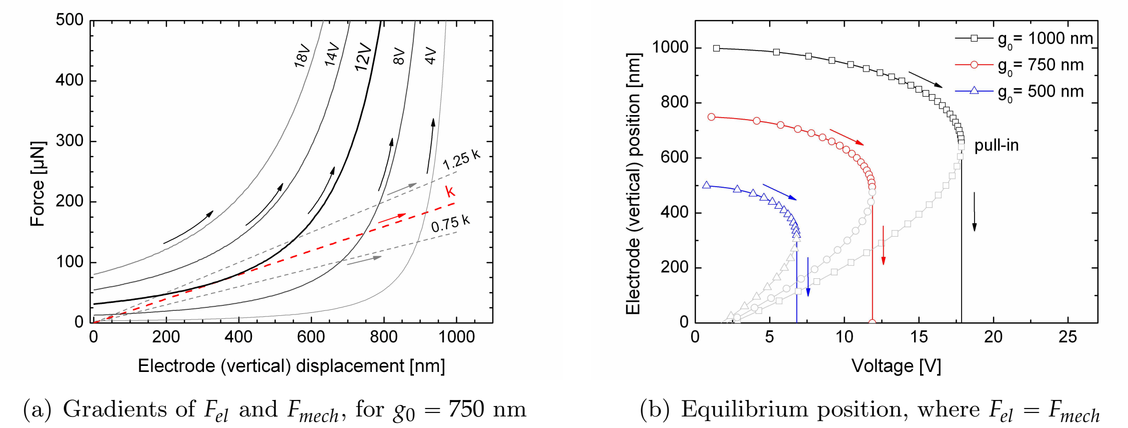
Figure 2.13(b) shows the influence of the electrode gap on the pull-in voltage. By increasing the electrode gap, the electrostatic force is reduced, thus a higher voltage has to be applied to close the switch.

It can be concluded that any variation of the stiffness and of the electrode gap, with respect to the nominal value, may result in a significant change of the pull-in voltage.

2.4 Analysis of switch geometry

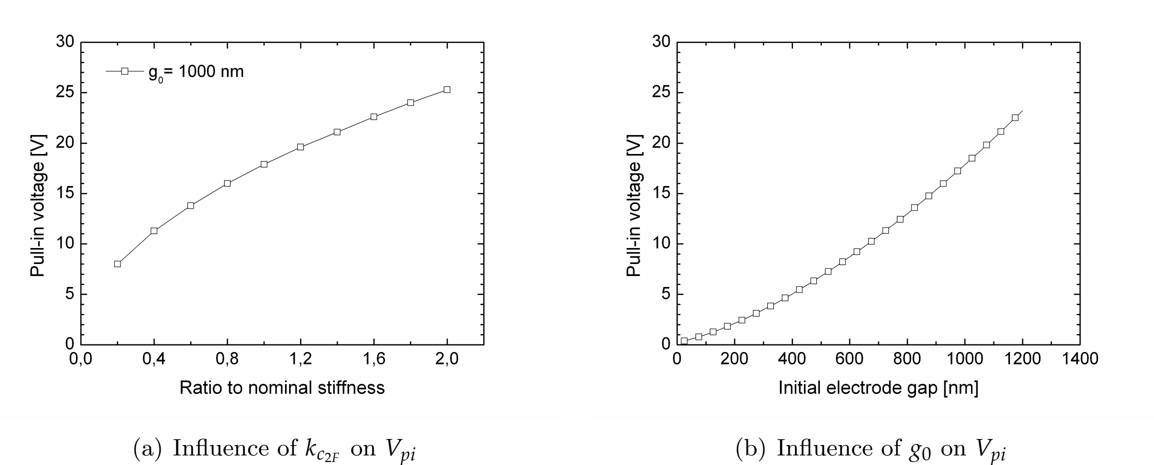
2.4.1 Objective

As it was demonstrated in the previous section, the geometry and the surface topography of the ohmic-type switches have a significant effect on their electro-mechanical behavior. The following section is aimed at investigating, the state of the surface of the ohmic contacts (fixed



(a) Gradients of F_{el} and F_{mech}, for $g_0 = 750$ nm (b) Equilibrium position, where $F_{el} = F_{mech}$

Figure 2.12: Analysis of electrostatic and mechanical forces in the ohmic-type switch, as a function of applied voltage



(a) Influence of $k_{c_{2F}}$ on V_{pi} (b) Influence of g_0 on V_{pi}

Figure 2.13: Pull-in voltage in function of switch stiffness and electrode gap.

and mobile), the top electrode (bottom side) and the actuation electrodes of 4 wafers of the ohmic-type switches.

2.4.2 Experimental procedure

2.4.2.1 Test methods

Scanning Electron Microscope (SEM)
Scanning Electron Microscopy (SEM) is a non-destructive technique, which uses a focused electron beam to image a sample. In the present work, this technique is used for relatively fast (few minutes) evaluation of the state of the surface of the actuation electrodes and the ohmic contacts. It is not possible to observe the non-conductive surface of the top electrode. The observations are realized using a Hitachi S4100 SEM.

Atomic Force Microscope AFM
The SEM technique fails to provide quantitative data on the surface topography, such as roughness parameters or peak heights. To obtain these missing data, Atomic Force Microscopy (AFM) is used. The AFM microscopy is an experimental technique dissimilar to the previously presented one. The AFM uses a probe mounted on a piezoelement, which movements in vertical and horizontal direction can be controlled with a sub-nm resolution [31].

In the present study, a Veeco Dimension 3100 AFM in the tapping mode is used. In this mode, the probe is excited to its resonant frequency and the amplitude and the frequency of these oscillations are measured in a real time. This oscillating cantilever starts approaching the sample and as it is getting closer to its surface, the amplitude of the oscillations is reduced and the phase is shifted. A given amplitude and phase correspond to a specific distance between the probe and the surface of the sample. At a set distance over the surface, the cantilever stops and the AFM starts scanning in the X-Y direction. When the probe is scanning the sample, the microscope is continuously adjusting the vertical position of the probe, so that the amplitude and the phase shift of the cantilever oscillations remain constant. These vertical movements of the probe reflect the topography of the sample.

The AFM measurements are relatively slow, as a typical measurement of a single topography takes approximately 1 hour.

For measuring the height of the profiles, the piezoelement is calibrated on a test grating, which consists of multiply steps of known height. After that, the electrical signal at the output of the AFM which corresponds to the vertical displacement, can be converted into (vertical) distance in nm. Thanks to this procedure it is possible to measure the height of the geometrical features on the surface of the sample.

The AFM measurements are used to extract the following roughness parameters: R_q, R_a, R_{max} R_{sk} R_{ku} which are defined in the Appendix A.

Focused Ion Beam (FIB)
Focused Ion Beam (FIB) is a destructive technique, which uses a focused beam of high-energy (gallium) ions to sputter material from the surface of the sample [32, 33]. In the present work, the FIB is used to make cross-sections of the mating elements of the ohmic contacts in the closed position. The cross-sections are then imaged using an SEM microscope. One complete measurement takes approximately 2 hours.

Before making a cross-section, the samples are sputtered with 2 μm thick layer of tungsten, to prevent from transferring the surface topography, to the analyzed area.

When analyzing the FIB results, it is necessary to keep in mind that during the sputtering of the material from the sample, some of the atoms are redeposited.

2.4.2.2 Test samples

The analyzes are carried out for 4 wafers of the ohmic-type switches, in the following sites of interest: the mobile contact, the fixed contact, the bottom electrode and the top electrode.

Prior to the observations and measurements the samples are unpackaged. For the SEM observations and AFM measurements the beams are removed and turned upside down to give access to the bottom side of the top electrode and mobile contact. For these analyses the same samples are used, while for the FIB cross-sections a second set of samples is used.

2.4.3 Results

2.4.3.1 SEM images

Table 2.5 presents representative SEM images of the mobile contacts, fixed contacts and bottom electrodes, for all investigated wafers.

Mobile contact
The mobile contact of the ohm.A wafer is fabricated using the standard process flow. As presented in Table 2.5 (ohm.A), the contact has high and thin edge profile along the circumference. Its surface is very inhomogeneous and there is a number of aggregates of considerable size (tens to hundreds of nm) present on it. The quality of the contact is lower than the ohm.B and the ohm.D wafers, where the optimized process flow is used.

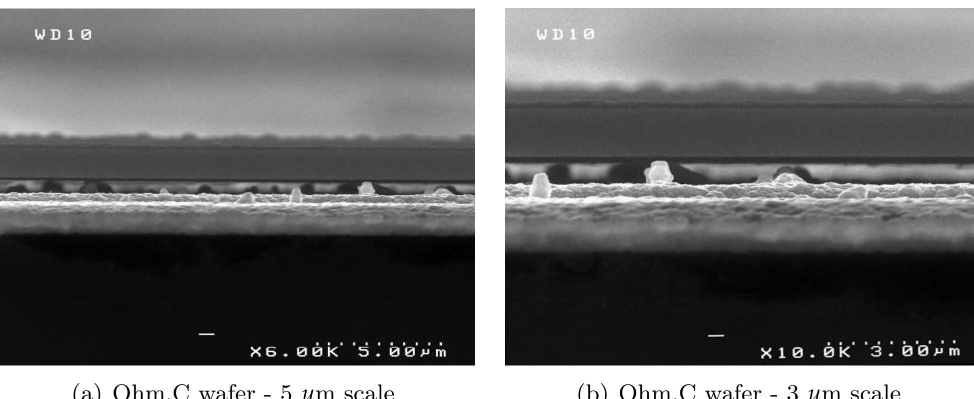
Ohm.B is the first wafer, where the optimized process flow is used. As presented in Table 2.5 (ohm.B), the optimization of the process flow results in a better homogeneity of the surface. Unlike the ohm.A, the mobile contact of the ohm.B wafer has no edge profile and no aggregates on its surface, nevertheless the contact roughness remains relatively high.

Ohm.C is the second wafer fabricated with the modified process flow. Unlike the ohm.B wafer, the mobile contacts of the ohm.C wafer (Table 2.5 (ohm.C)) resembles those from the ohm.A wafer, where the standard process flow is used. In particular, we can see the high edge profile and the large aggregates on the contact surface. A possible explanation of this observation is a problem with etching the blind hole in SiN_x beam. The thin layer of SiN_x, which is left at the bottom of the blind hole is intended to protect the layer of the polymeric sacrificial layer underneath, during stripping of the resist. For the ohm.C wafer it is very probable, that during the first step, a through hole was etched instead of a blind hole (the etching depth was not well controlled). Consequently the sacrificial layer has been deteriorated during stripping of the resist and effectively the mobile contact was fabricated like in the standard process flow.

The mobile contact of the ohm.D wafer, which is the most recent wafer, is fabricated using the optimized process flow. In this case (Table 2.5 (ohm.D)), the contact quality is higher, when compared to the other wafers. In particular, the contact surface is planar, homogeneous and no particles are present on its surface.

Table 2.5: SEM images of the ohmic-type switches: mobile and fixed contacts and bottom electrode

Wafer	Mobile contact	Fixed contact	Bottom electrode
ohm.A			
ohm.B			
ohm.C			
ohm.D			



(a) Ohm.C wafer - 5 μm scale (b) Ohm.C wafer - 3 μm scale

Figure 2.14: Hillocks on the electrode surface of ohm.C wafer

Fixed contact and bottom electrode
The fixed contacts and the bottom electrodes, for all 4 wafers, are fabricated from the same material and using the same process flow. The results of the SEM observations are presented in Table 2.5.

The ohm.A and the ohm.B wafers have the most smooth and homogeneous surface of the fixed contacts and the bottom electrode.

The ohm.C wafer is the only one, which is concerned with the problem of hillocks - the aggregates of particles at the surface of the fixed contact and the bottom electrode. The particles are of considerable size, compared to the initial height of the electrode gap.

To examine the height of the hillocks, SEM side-view images of a switch with a beam have been captured. These images are presented in Figure 2.14. This figure shows a part of the bottom electrode, with a number of hillocks on its surface. Suspended above this bottom electrode is the beam of the switch (the top electrode), which is in its initial up-state position. From this figure, it is clear that the hillocks are as high as a half (approximately) of the electrode gap. This may have serious consequences for a correct functioning of the switches, as the hillocks will prevent the actuation electrodes from contact. The formation of the Au hillocks has been analyzed in [14]. The authors have found that the Au hillocks growth is promoted by elevated temperatures (above 280°C) in proximity of resist residues, which obstructs Au grain growth. As a result to avoid hillocking it is advised to avoid excessive thermal treatment and careful removal of the resist layers.

The ohm.D wafer has a homogeneous surface with no hillocks. However, the surface roughness is higher, when compared to the ohm.A and ohm.B wafers. This may be the result, of an optimization of the underlayer of poly-silicon and silicon dioxide, which has been done to improve the RF performance of the switch.

2.4.3.2 AFM topographies

Top electrode
The surface of the top electrodes is found to be similar for all 4 wafers. A representative AFM image of the surface topography, together with two profiles, is presented in Table 2.6, for the

Table 2.6: AFM measurements of ohmic switches - top electrode.

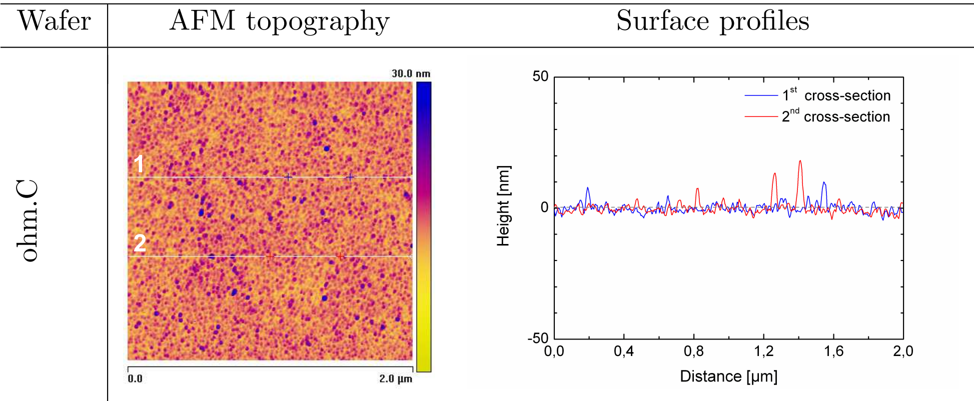
Wafer	AFM topography	Surface profiles
ohm.C		

Table 2.7: Quantitative results of roughness and topography of ohmic switches

Wafer	Bottom electrode					Top electrode		
	R_q [nm]	R_a [nm]	R_{max} [nm]	R_{sk}	R_{ku}	R_q [nm]	R_a [nm]	R_{max} [nm]
ohm.A	7.03	5.20	53	0.36	5.22	1.23	0.88	25.0
ohm.B	4.25	3.19	63.8	0.62	8.30	7.04	5.62	51.1
ohm.C	32.2	13.9	487	5.90	46.0	1.88	1.35	28.3
ohm.D	18.6	14.5	154	0.65	4.34	0.70	0.36	24.1

ohm.C wafer. The roughness parameters that have been extracted from the AFM measurements (for all wafers) are summarized in Table 2.7.

The measured arithmetic average roughness R_a ranges from 0.36 to 5.62 nm. The lowest roughness is measured for the ohm.A and ohm.D wafers (respectively 0.88 and 0.36 nm). The medium values are measured for the ohm.C wafer (1.35-1.95 nm). The highest roughness is measured for the ohm.B wafer (5.62 nm). As this roughness is low, compared to the roughness of the bottom electrode and the fixed contact, it has a negligible effect on the functioning of the ohmic-type switches.

Bottom electrode

The Table 2.8 presents representative AFM topographies with two section profiles measured at the bottom electrodes for all 4 wafers of the ohmic-type switches. The roughness parameters extracted from these measurements, are summarized in Table 2.7.

The AFM results confirm the qualitative observations with the SEM microscope.

The lowest arithmetic average roughness R_a is measured for the ohm.A and ohm.B types, where it is 5.2 and 3.2 nm respectively.

The R_a for the ohm.C wafer ranges is 13.9 nm, which is only 3 to 4 times higher than for the ohm.A and the ohm.B wafers. The higher value of R_a results from high peaks observed on section profiles with the maximum height of the peaks R_{max} = 487 nm. These peaks for the ohm.C wafer are indicated by the higher value of the skewness, which positive value indicates that there is a number of sharp spikes on the surface, that is further confirmed by high kurtosis, which is also several times higher than for the other wafers.

Table 2.8: AFM measurements of ohmic switches - bottom electrode

Wafer	AFM topography	Surface profiles
ohm.A		
ohm.B		
ohm.C		
ohm.D		

The R_a for the ohm.D is 14.5, which is significantly higher than for the ohm A and ohm.B and is even higher than for the ohm.C wafer. Contrary to the ohm.C wafer, the section profiles show that the roughness is arranged flatly around the average (roughness) profile, which is indicated by the low value of kurtosis, similar to the ohm.A and the ohm.B wafers.

To sum up, the ohm.A and ohm.B wafers has the smoothest surface of the bottom electrodes. The ohm.C wafer, is the only wafer that suffer from hillocks, that is the high peaks present on the bottom electrode. The ohm.D wafer is free from the hillocks, but the roughness of its bottom electrode is several times higher, compared to the ohm.A and ohm.B wafers.

2.4.3.3 FIB images

Figure 2.15 presents the FIB cross-sections of the ohmic contacts for the ohm.B, ohm.C and ohm.D wafers. No image is available for the ohm.A wafer, which contacts are similar to those of the ohm.C wafer.

The mobile contact of the ohm.B wafer is planar but it is significantly rougher compared to the other wafers. The cross-section reveals a problem of adhesion of the under-layer of the mobile contact, that is the bottom part of the contact is separated from the upper-layer. Moreover, when we examine the continuity of the gold layer (light gray color) at the edge of the through hole in the beam, we can see that there are some cracks, which are filled with the dielectric (dark gray color). This may result in worse conductivity of the contact and may lead to higher switch resistance R_s.

The average roughness of the ohm.C mobile contact is (qualitatively) lower compared to the ohm.B wafer. The SEM images show however, that there is a number of high peaks present on the surface of the mobile contacts of the ohm.C wafer, which are visible in the FIB cross-section, upon a closer look. These peaks result in a higher separation between the mobile and fixed contacts. Compared to the ohm.B wafer, there is no problem with the adhesion of the under-layer or the continuity of the gold layer at the edge of the through hole.

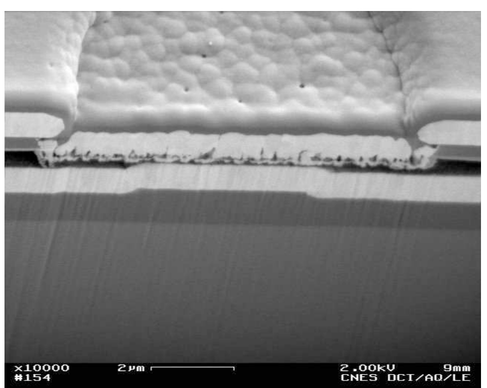
In the ohm.D wafer, all the previously mentioned problems have been eliminated. The contact is planar and smooth. The SEM images show no peaks on the surface of this contact and we can see that the separation between the mobile and fixed contacts is lower, than for the ohm.C wafer. Similarly to the ohm.C wafer, there is no problem with the adhesion of the under-layer nor the continuity of the gold layer at the edge of the through hole. From the FIB cross-section it is also clear that the higher roughness R_a measured for the ohm.D wafer originates from a higher roughness of the poly-Si and SiO_2 layers, which have been optimized to improve the RF characteristics.

2.5 Characterization of mechanical properties

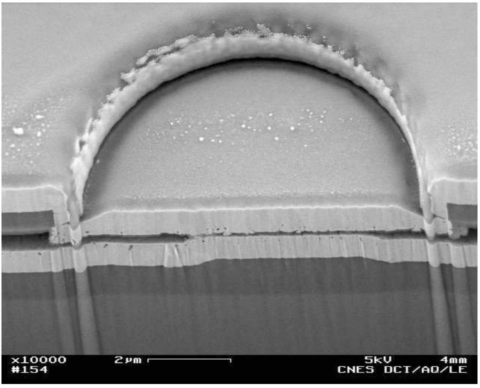
2.5.1 Introduction

This section is aimed at characterizing the mechanical properties of the ohmic-type switches, prior to modeling of their electro-mechanical behavior.

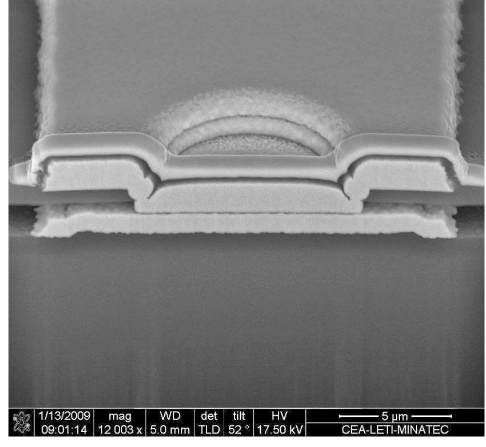
The characterization of the material properties of a fabricated device is very important, as these properties may be changed during fabrication steps following the deposition, especially during the post-fabrication annealing.



(a) Ohm.B



(b) Ohm.C (similar to ohm.A)



(c) Ohm.D

Figure 2.15: FIB cross-section of mobile-fixed contact pair for ohm.B , ohm.C and ohm.D wafers

The characterization of the material properties may be somewhat complicated, because of the small dimensions of the specimens, which requires using unconventional testing techniques.

2.5.2 Literature review

The following section presents a concise review of existing approaches in testing the electro-mechanical behavior of micro-beams and MEMS switches.

The parameter that describes the mechanical properties of a micro-beam is its stiffness, which is defined as the resistance of an elastic beam to a deformation caused by an applied load. The experimental stiffness is obtained by measuring the deflection of the beam under a known normal force applied to its surface. Because of small characteristic dimensions, the test equipment must be adapted for measuring small deflections from nm to several μm and applying forces in the range of μN to mN. In general, there are three experimental techniques commonly used for such tests.

The most common technique is the nanoindentation technique[1] [34]. Thanks to its high resolution, this became a standard method for extracting the hardness and the Young's modulus of a wide range of ultrathin (hundreds nm) materials. In this technique, a normal concentrated load is applied to the beam surface by an indenter tip and the corresponding displacement (beam deflection) is measured.

Standard nanoindentation has been used in [18, 25] to test the mechanical properties of single- and multilayer 80-140 μm-long fixed-fixed beams. The authors have demonstrated, that a single nanoindentation at the beam center can be used to extract the Young's modulus and the residual stress of a single-layered beam. This can be done by fitting the result of the nanoindentation with an analytical mechanical model of the beam, which allows calculating the theoretical deflection curve. The authors have extended this method for testing multi-layered beams, concluding that the mechanical behavior of the multi-layered beam can be well approximated by the model of a single-layer beam, with adjusted material parameters. This is valid, even when the stack is composed of layers with different stress levels.

An alternative to nanoindentation, when lower forces are required, is an AFM-based technique, which has been implemented in [19, 21, 24, 31] for measuring the stiffness of fixed-free and fixed-fixed gold beams.

What differs between the AFM-based and the standard nanoindentation technique is the minimum vertical force that can be applied to the specimen. In the standard nanoindentation, the force transducer is either of an electromagnetic[2] or an electrostatic[3] type and the force can be measured with a low uncertainty of 1%. In the AFM-based technique, it is a cantilever, which acts as the force-transducer. The force is obtained by multiplying the probe stiffness and its vertical deflection. For commercially available probes the stiffness uncertaintity can be as high as 10%. Consequently, the accuracy of the force measurement with the AFM depends on the precision of the procedure of determining the probe stiffness. Because of that, the AFM-based method is less precise compared to the standard nanoindenation. Nevertheless, this technique is still appropriate for qualitative comparison of different low-stiffness beams, provided that the same probe is used to compare different structures.

[1]The principles of the nanoindentation and a schematic diagram of a nanoindenter are presented, in detail, in section 2.5.3.1

[2]Used in the Agilent nanoindenters (former MTS)

[3]Used in the Hysitron nanoindenters

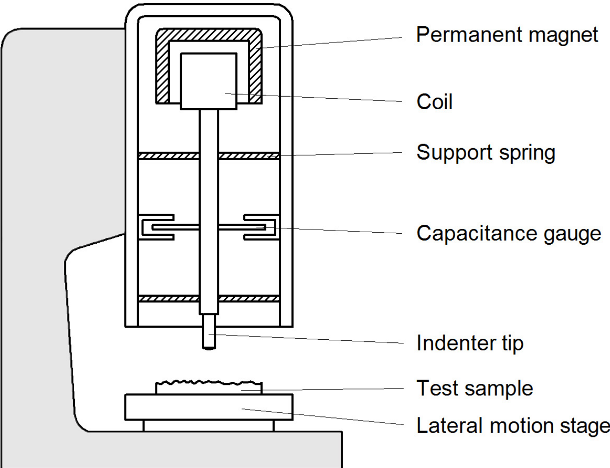


Figure 2.16: Schematic drawing of nanoindenter with electro-magnetic force transducer

Another original approach to measure the beam deflection under a given load has been proposed in [17], where the authors measure the stiffness of a fixed-fixed micro-beam. To impose the load, a voltage ramp is applied between the beam and an actuation electrode placed directly underneath. The resulting vertical force is calculated from a parallel-plate capacitor model, where the beam is one of the plates and the bottom electrode is the other. To measure the corresponding deflection, an interferometric microscope is used. The main drawback of this method, compared to the standard nanoindentation technique, is the relatively high uncertainty of the calculated force.

It may be concluded that the most appropriate technique, that gives high precision results, is the standard nanoindentation. The limiting factor is the minimum force that has to be applied to the tested structure. Whenever the stiffness of the specimen is high enough (>10 N/m) , it is advised to use the standard nanoindentation. For specimens with lower stiffness the AFM-based technique is more suitable.

2.5.3 Experimental procedure

2.5.3.1 Test method

Principles of nanoindentation

The nanoindentation became a standard technique of testing the mechanical properties of thin layers, like those which are frequently used in microsystems. In its principles, this technique resembles the Vickers and Brinell methods used to determine material hardness. Virtually, it extends these techniques to smaller displacements and forces, which are typically in the range of sub-nm to µm, for the displacements and µN to mN, for the applied and measured forces.

A schematic drawing of a nanoindenter, with an electro-magnetic force transducer is presented in Figure 2.16. The vertical load is applied and measured by the force transducer consisting of a permanent magnet and a coil, which is placed at the top of the central column. The

central column is supported by a number of flat springs, so it can move in the vertical direction and this displacement is measured by the capacitive gauge. The nanoindenter tip is attached to the bottom of this column. The lateral position of a test sample is set by a lateral motion stage.

A key element of the nanoindenter is the force-transducer. The coil wire is wound into a coil on a ferromagnetic core. When a current passes through the coil wire, it generates a strong magnetic field inside the core, which interacts with the magnetic field of the permanent magnet. By controlling the current in the coil, it is then possible to control the force on the tip of the nanoindenter.

The second key element is the capacitive gauge, which is used to measure the vertical displacement of the nanoindenter tip. This gauge is a parallel-plate capacitor with one plate attached to the central column, and the other plates fixed to the support. All changes in the measured capacitance are due to changes in the distance between these plates, as their area and the voltage across the capacitor are held constant.

The nanoindenter may operate in two modes: a quasi-static and/or a dynamic[4] mode.

In the quasi-static mode a concentrated vertical force is applied to the tip of the nanoindenter. The tip approaches the surface of a sample at a constant rate and when it comes to contact, it imposes a quasi-static force to its surface. Typically, such a measurement is used to determine the hardness and the elastic modulus of a tested material [34], but it can also be used to determine the stiffness of a microbeam or a MEMS switch [18, 25].

In the dynamic mode, a small sinusoidal force (AC force) is superimposed on the quasi-static force (DC force) applied to the indenter [35]. The AC translates into multiply loading and unloading with a few nm amplitude. The resulting modulation in the displacement (AC displacement amplitude) and the phase shift between the AC force and displacement is measured using a lock-in amplifier. The harmonic stiffness is calculated from the amplitude and phase shift using a dynamic model. The advantage of this method is that the stiffness can be obtained continuously during indentation. The oscillation frequency above 40 Hz, makes this method less sensitive to thermal drift. The CSM measurement is applicable for a stiffness value which is 2-3 orders of magnitude lower than the stiffness of the test equipment.

During data acquisition the displacement and corresponding force are measured simultaneously.

Test setup

The nanoindentations are carried out using either an MTS nanoindenter XPW [5] (ST) or an MTS nanoindenter XP[6] (CEA-Leti), with a standard XP head, the technical specification of which is presented in the Table 2.9. To avoid the penetration of the tip into the beam material, a spherical tip is used, instead of a standard Berkovich tip. The measurements are carried out in the quasi-static and the dynamic CSM modes for the ohm.A, ohm.B and ohm.C wafers. For the ohm.D wafer only quasi-static measurements are performed. The detailed configuration of the nanoindenter during the tests is presented in Table 2.10.

The nanoindentations are performed at two positions (Figure 2.17) on the switch surface:

- Center of the beam: the tip of the indenter is placed at the center of the mobile contact.

[4] Continuous Stiffness Measurement mode - CSM

[5] Measurements have been performed by Diane LEVY under supervision of Frederic SOUCHON

[6] Measurements have been performed by Delphine LORY under supervision of Christoph POULAIN

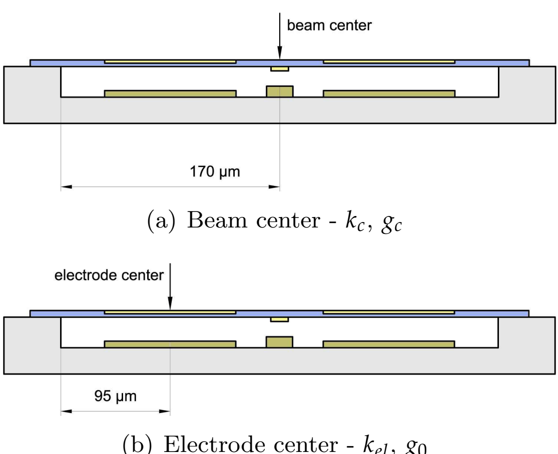
Table 2.9: Specification of the standard XP head of MTS XP nanoindenter

Parameter	Value
Frequency of tip oscillations	< 45 Hz
Resolution of displacement measurement	$< 10^{-2}$ nm
Maximum indentation depth	> 500 µm
Maximum load	500 mN
Resolution of load measurement	50 nN

Table 2.10: Parameters of nanoindentation

Parameter	Value
Surface approach velocity	4 nm/s
Allowable drift	0.4 nm/s
Harmonic displacement target	2 nm
Frequency target	45 Hz
Stiffness limit	2000 N/m
Indenter tip	Spherical

- Center of the electrode: the tip of the indenter is placed on the geometrical center of left and right electrodes that is at the distance of $d_{el} = 95$ µm from a support.



(a) Beam center - k_c, g_c

(b) Electrode center - k_{el}, g_0

Figure 2.17: Positions of nanoindentations

From the nanoindentation at the beam center, the stiffness k_c and the contact gap g_c are extracted. It is here recalled that k_c is defined as the stiffness at the center of the beam, when one normal concentrated load is applied at the beam center and the contact gap g_c is the vertical distance between the movable and fixed ohmic contacts.

From the nanoindentations at the electrode center, the electrode stiffness k_{el} and the electrode gap g_0 are extracted. The k_{el} is defined as the stiffness at the geometrical center of an electrode, when one normal concentrated load is applied at the electrode center. The electrode gap g_0 is

the distance between the surface of the dielectric (the bottom part of the top electrode) and the bottom electrode.

Analysis of force-distance curves measured on switch

In the present study, the nanoindentation has been used for original measurements to extract the stiffness (k_c and k_{el}) and the gap heights (g_c and g_0) of the ohmic-type switches.

Examples of force-distance curve and a harmonic stiffness curve, measured on a switch are presented in Figure 2.18. The *Displacement* axis corresponds to the current position of the tip of the nanoindenter. The *Force* vertical axis is the force imposed by the tip on the sample and measured by the force-transducer. This force is necessary to overcome the mechanical resistance of the switch beam. For the sake of clarity, the zero-values at the *Displacement* and *Force* axes are set in the first point of contact of the nanoindenter tip with the sample.

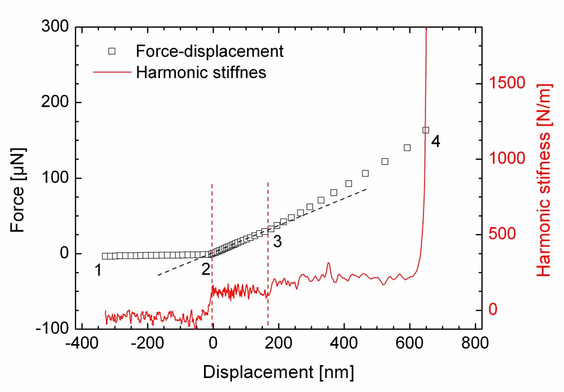


Figure 2.18: Typical force-displacement curve at electrode center for ohmic-type RF MEMS switch (Ohm.B wafer)

The force-displacement curve, which is measured in the quasi-static mode, is plotted in Figure 2.18 as black squares. In the same figure, the harmonic stiffness measured in the dynamic mode, is plotted as a red line.

The harmonic stiffness is acquired simultaneously to the force-displacement curve, thus the displacement axis is common for both measurements. The advantage of the harmonic-stiffness measurement, is its sensitivity to any changes of the measured stiffness. It will be demonstrated here, that in the case of beam testing, the average value of the harmonic stiffness agrees well with the one obtained from the slope of the force-distance curve (quasi-static measurement).

A typical force-displacement curve measured on a switch is described below. The starting point of the force-displacement curve is denoted as 1. Here the tip of the nanoindenter is suspended over the test sample. From this point onwards, the tip is traveling towards the sample at a constant rate. In the segment 1-2, there is no contact with the sample, consequently the load remains zero. In reality, the slope of the part 1-2 is comprised between approximately 0-5 N/m and it is constant during a single measurement. This slope is due to thermal drift of the force transducer.

The next characteristic point is denoted as 2. In this point the tip touches the beam of the switch.

From this point on, the tip starts to impose a quasi-static load on the beam and the beam starts deflecting. The measured displacement of the tip is virtually the same as the deflection of the beam, as it is assumed that the spherical tip cannot penetrate in the material of the beam. The load, which is measured on the tip is equal to the mechanical restoring force of the beam, which is a product of the beam stiffness k_c times deflection z_s.

In part 3-4 the slope becomes steeper, which signifies that the beam stiffness increases. In the point denoted as 4 the top electrode touches to the bottom electrode, the beam cannot deflect any further and the quasi static load and the harmonic stiffness increase rapidly. At this point the measurement is stopped and the nanoindenter retracts.

2.5.3.2 Test samples

The nanoindentations are performed for all 4 wafers of the ohmic-type switches. Prior to the measurement the switches have been unpackaged

2.5.4 Results of nanoindentation

Table 2.11 presents the raw force-distance curves and continuous stiffness measurements for all 4 wafers of the ohmic-types switches. To allow easier comparison between the samples, the results are plotted in the same scale regardless the type of investigated sample. The plotted curves, are the representative (median) curves for a specific sample, selected from the measurements on several (3-5) samples, except for the ohm.D wafer, where a single switch is tested.

The reproducibility of the measurement results is very good, as the results obtained from two different nanoindenters differ by less than 5-10% for the same samples.

The analyzed results of the nanoindentation of the 4 wafers are summarized in the Table 2.12, where the values of the stiffness at the beam center k_c and the electrode center k_{el} are presented, along with the measured values of the contact g_c and of the electrode gaps g_0. The results are median values for the tested wafers.

The stiffness k_c measured at the beam center varies from 79 N/m to 132 N/m between the wafers. The lowest value is measured for the ohm.A wafer, while the highest is measured for the wafer ohm.B. Significant variation of the stiffness is observed within the wafer ohm.C, where the median stiffness k_c is 91 N/m.

In all cases, the ratio between the stiffness k_{el} measured at the electrode center and the stiffness k_c measured at the beam center is comprised between 1.15-1.35, which show little discrepancy with the theoretical value ($k_{el}/k_c = 1.27$). This discrepancy is most likely to be due to the uncertainty of the horizontal position of the indenter tip during measurement.

The contact gaps g_c varies from 140 nm for the ohm.B wafer to 650 nm for the ohm.A wafer. The lowest electrode gap is measured for the ohm.C wafer (490 nm) and the highest value of g_0 is found for the ohm.A wafer (755 nm). The ratio between the contact and electrode gap heights is different for each of the different wafers and it ranges from 0.2 to 0.85 for the ohm.B and ohm.A wafers, respectively.

The paragraphs below discusses the behavior of each wafer in more detail.

Mechanical behavior of the ohm.A wafer

The typical mechanical behavior of the ohm.A wafer is presented in Table 2.11 (ohm.A).

Table 2.11: Results of nanoindentation for ohmic-type switches

Wafer	Beam center	Electrode center
ohm.A		
ohm.B		
ohm.C		
ohm.D		

Table 2.12: Results of nanoindentation of ohmic switches

Wafer.	g_c [nm]	g_0 [nm]	g_c/g_0	k_c [N/m]	k_{el} [N/m]
ohm.A	650	755	0.86	79	103
ohm.B	140	650	0.22	132	180
ohm.C	260	490	0.53	91	121
ohm.D	230	645	0.36	91	105

The stiffness at the beam center is $k_c = 79$ N/m and at the electrode center it is $k_{el} = 103$ N/m. The k_{el}/k_c ratio is 1.3. The contact gap height is $g_c = 650$ nm and is the highest for all the investigated wafers. The electrode gap is comparable to the contact gap as it is $g_0 = 755$ nm, which is also the highest value for all investigated samples.

The force-displacement curve at the beam center has two slopes, denoted as (2-3) and (3-4). These two slopes are also clearly identified as the steps of increased harmonic stiffness. The first one (2-3) corresponds to stiffness k_c, which is lower than the stiffness obtained from the (3-4) part. There are two probable explanations for this observation. The mobile contact of the ohm.A wafer has a rough surface with a number of high peaks, as presented in the SEM images. The first possible explanation is then that the second slope is due to the deformation of the peaks at the surface of the mobile contact which are pressed into the RF-signal transmission line during the nanoindentation. The second hypothesis that could explain this observation is that the mobile contacts do not touch the signal line simultaneously. In this case, when the first mobile contact contacts with the RF-signal transmission line, the switch twists to put the other one in contact too, which requires a higher force and leads to an increase of the stiffness.

The force-displacement curve at the electrode center has also two slopes. Here, the explanation of these two slopes is more straightforward. The first slope corresponds to the stiffness k_{el} *i.e.* before the mobile contact closes the RF-signal transmission line. The second one, with higher stiffness, corresponds to the situation when the contact is closed, therefore any farther displacement at the beam center is no longer possible and the beam continues deflecting at the electrode center only.

Mechanical behavior of the ohm.B wafer

The typical mechanical behavior of the ohm.B wafer is presented in Table 2.11 (ohm.B).

The stiffness at the beam center is $k_c = 132$ N/m and at the electrode center it is $k_{el} = 180$ N/m. The k_{el/k_c} ratio is 1.36. The contact gap height is $g_c = 140$ nm, which is more than 500 nm lower than for the ohm.A wafer and which is lowest for all the investigated wafers. The electrode gap is $g_0 = 650$ nm, which is comparable with the ohm.A.

The harmonic stiffness, has only one step (2-3) at the beam center. At the electrode center, two distinctive steps are observed, the first one (2-3) corresponding to the situation before the ohmic contact is closed and the second one (3-4) after. It may be concluded that no abnormal behavior is observed for this wafer.

Mechanical behavior of the ohm.C wafer

The typical behavior of the ohm.C wafer is presented in Table 2.11 (ohm.C) where the median results for the ohm.C wafer are presented. This wafer has the highest scattering of the measured

stiffness values, from all of the investigated wafers.

The stiffness at the beam center is k_c = 91 N/m and at the electrode center it is k_{el} = 121 N/m. The k_c to k_{el} ratio is 1.33. The contact gap height is g_c = 260 nm and the electrode gap g_0 = 490 nm which is the lowest from all the wafers.

The force-displacement curve at the beam center shows multiple steps, which are also observed on the harmonic stiffness run, as well. The stiffness in the following steps is several times higher than the stiffness k_c, before the contact is closed. This behavior resembles the behavior of the ohm.A wafer. The common feature of these two wafers is the rough surface of the mobile contact. Because the runs of the force-displacement and harmonic-stiffness curves are similar for these two switches, it highly suggests that these multiple slopes are related to the contact quality and its behavior under the load.

The situation is similar at the electrode center, that is multiple stiffness slopes are observed on the force-displacement curve, similarly to the ohm.A wafer.

Mechanical behavior of the ohm.D wafer

The mechanical behavior of the ohm.D is presented in Table 2.11 (ohm.D).

The stiffness at the beam center is k_c = 91 N/m and at the electrode center it is k_{el} = 105 N/m. The k_{el}/k_c ratio is 1.15, which is lower than in case of previous wafers. The contact gap height is g_c = 230 nm, which is similar to the ohm.C wafer. The electrode gap is g_0 = 650 nm, which is comparable with the ohm.A and ohm.B.

The SEM images and FIB cross-section show, that the ohm.D wafer has the smoothest and uniform mobile contacts, which is confirmed by the force-displacement (and harmonic-stiffness) curves. The force-displacement curve at the beam center shows only one slope and at the electrode center it shows two slopes, similarly two the ohm.B wafer.

2.5.5 Results of mechanical modeling

2.5.5.1 Fitting of mechanical model

For each of the investigated wafers of the ohmic switches, two experimental values of stiffness k_c and k_{el} are extracted. In this section the measured stiffness is fitted with the mechanical model, so it produces the theoretical values of k_c^{fit} and k_{el}^{fit}, equal to the experimental ones. The residual stress σ_x^{fit} is used as a fitting parameter.

The mechanical model, which is fitted with the experimental nanoindentation results, is the model for one concentrated normal load, which has been devised in section 2.3.2.2. For fitting the nanoindentation results, the normal load is applied either at the beam center or at the electrode center (d_{el}=95µm).

The experimental and fitted values of stiffness and the fitted residual stress are summarized in Table 2.13.

It must be noted, that both the theoretical and the fitted values are in good agreement, with a maximum discrepancy of 5% between them.

The fitted residual stress ranges between 210 MPa and 370 MPa for the ohm.A and the ohm.B wafers, respectively. These values are in agreement with the expected order of magnitude of the value σ_x, measured at the fabrication stage. Moreover, the distribution of the residual stress between the wafers is as expected from the measurements on full-wafers during fabrication.

Table 2.13: Measured, fitted and calculated values of stiffness for ohmic-type switches

Wafer	k_c [N/m]	k_{el} [N/m]	k_c^{fit} [N/m]	k_{el}^{fit} [N/m]	σ_x^{fit} [MPa]	$k_{c_{2F}}^{calc}$ [N/m]
ohm.A	79	103	79	101	210	141
ohm.B	132	180	137	174	370	244
ohm.C	91	121	92	116	245	163
ohm.D	91	105	89	113	235	157

2.5.5.2 Beam stiffness for electro-mechanical model

Once the mechanical model is fitted with the residual stress, it is possible to use this model to calculate the stiffness required for the electro-mechanical model, which is the stiffness $k_{c_{2F}}$.

During the nanoindentation the normal force is applied at one position at a time, either at the beam center or the electrode center.

In the ohmic-type switches, there are two side electrodes, and during the actuation, the electrostatic force acts simultaneously on these two electrodes, hence there are two normal loads. The stiffness, which is then required for the electro-mechanical model is the stiffness at the beam center, when two normal loads are applied simultaneously at the electrode centers. This calculated stiffness is denoted as $k_{c_{2F}}$ and its calculated values are presented in Table 2.13.

2.5.5.3 Calculations of contact and restoring forces

The Table 2.14 summarizes the results of calculations of the contact F_c and restoring forces F_r, for all investigated wafers of the ohmic switches. The contact forces are in the range of 110-780 μN, while the restoring forces are in the range of 19-51 μN.

The restoring force F_r depends on the stiffness at the beam center k_c and the contact gap g_c. The higher this stiffness and the contact gap, the higher the restoring force. This is the case with the ohm.A wafer, which has the highest F_r among all the wafers, due to the highest contact gap.

The contact force F_c depends mostly on the distance traveled by the side electrode once the contact is closed, that is the difference between the electrode and contact gap $g_0 - g_c$. The higher this difference, the higher the contact force F_c, as can be seen for the ohm.B wafer.

By modifying the electrode g_0 and contact g_c gaps it is possible to adjust the ratio between the restoring and contact force. In our case, this F_r/F_c ratio varies from 0.02, for the ohm.B, to 0.46, for the ohm.A. The positive effect of the high contact force may be a lower contact resistance, but the main drawback is that a low restoring force may favor stiction, which is the case of the ohm.B wafer.

2.6 Characterization of electrical behavior

2.6.1 Objective

This section is aimed at characterizing the electrical behavior of the 4 wafers of the ohmic-type switches.

Table 2.14: Estimated values of restoring and contact forces

Wafer	g_c [nm]	$g_0 - g_c$ [nm]	k_c^{fit} [N/m]	$k_{F_c}^{calc}$ [N/m]	F_r^{calc} [μN]	F_c^{calc} [μN]	F_c^{calc}/F_r^{calc}
ohm.A	650	105	79	1041	51	110	0.46
ohm.B	140	510	137	1533	19	780	0.02
ohm.C	260	230	92	1150	24	265	0.09
ohm.D	225	420	89	1119	20	470	0.04

2.6.2 Experimental procedure

2.6.2.1 Test method

C-V and R-V characteristic of ohmic switches
The electrical behavior of any ohmic-type RF MEMS switch can be described by C-V and R-V measurements, where the capacitance, and the switch resistance of the ohmic switch are measured, respectively. An exemple of C-V and R-V sweeps are presented in Figure 2.19(a).

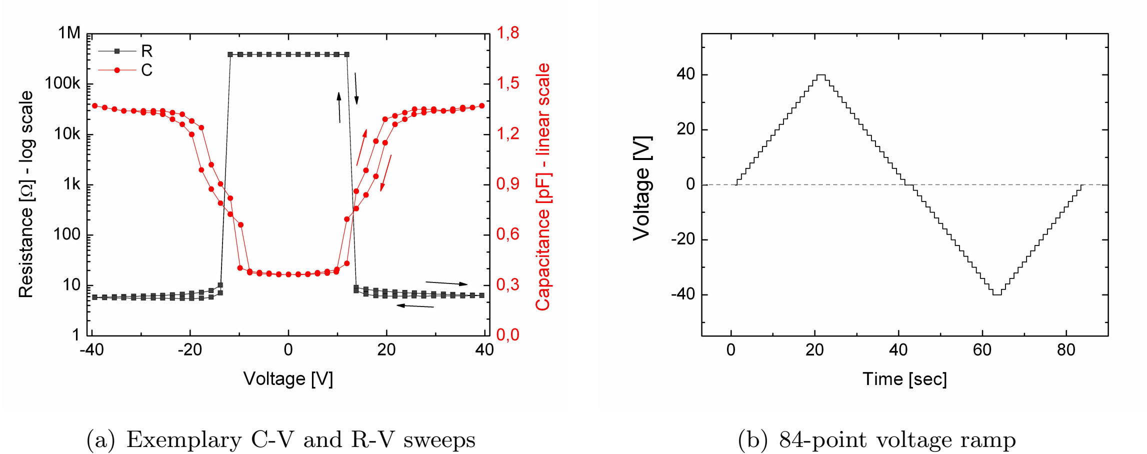
The capacitance of the ohmic-type switch (C_s) plotted in the C-V characteristic, is the capacitance of two parallel-plate capacitors in parallel, each of them formed between the corresponding top and the bottom actuation electrodes, for the left and the right side, respectively. As it has been discussed in section 2.3.3.1 the capacitance reflects the vertical position of the top electrode.

The lowest capacitance is measured (Figure 2.19(a)), when no voltage is applied across the electrodes and the switch remains in the up-state, so that the electrode gap is maximum. This initial value of the capacitance depends on the initial electrode gap height. When a voltage ramp is applied between the electrodes (Figure 2.19(b)), the beam starts deflecting, that is the electrode gap is decreasing. Consequently, the switch capacitance increases and it reaches its maximum value, when the top electrodes come into contact with the bottom electrodes. This situation takes place when the maximum voltage is applied, thus the maximum electrostatic force acts on the top electrodes and the electrode gap is reduced to minimum.

The maximum value of the capacitance (at V_{max}) gives information about the state of the surface of the contacting electrodes. In a real switch, in the down-state, the top and the bottom electrodes are separated by a specific distance. This distance depends, in particular, on the roughness of the contacting electrodes. Higher values of the maximum capacitance, indicates that the electrodes are closer to each other, so that the surface roughness is low. In contrast, lower values of the maximum capacitance suggest a highest distance between the electrodes in the down-state, thus it indicates problems with surface roughness or the presence of hillocks, to give an example.

The resistance of the ohmic-type switch R_s plotted in the R-V characteristic, is the resistance measured on the RF-transmission line. When the switch is in the up-state, the RF-line is open and the resistance is limited by the impedance of the instruments, which is roughly 380 kΩ for the CarOhm test-bench. When the ohmic switch is in the down-state, the RF-line is shorted by the mobile ohmic contact and the resistance measured at the transmission line drops. In our case, it is the switch resistance R_s, which is measured. The switch resistance is a sum of the resistance of the transmission line and the resistance of two ohmic contacts.

The C-V and R-V characteristics are also used to define the pull-in (V_{pi} or V_{pi_R}) and the



(a) Exemplary C-V and R-V sweeps

(b) 84-point voltage ramp

Figure 2.19: Characterization of electrical characteristics of ohmic-type RF MEMS switch

pull-out voltage (V_{po_R}) of the switch. For the ohmic-type switch two types of pull-in voltages can be defined. The first one is an ohmic pull-in voltage V_{pi_R}, when the transmission line is shorted and the resistance drops. The second is a capacitive pull-in voltage V_{pi}, when the membrane is pulled down and the capacitance drops. The pull-out voltage V_{po_R} is the voltage when the contact opens.

Analysis of C-V and R-V sweeps

In the present study, the capacitance and resistance of the switches are measured through a voltage ramp presented in Figure 2.19(b), for a positive and negative bias, in the range of -40 to 40 V. The voltage resolution for a standard 84-point test is 2V.

For each wafer the following parameters have been extracted from the C-V and R-V sweeps:

- C_{up} - the up-state capacitance, measured at 0V.
- C_{pi} - the closed-contact capacitance, measured at V_{pi_R} for switches where the $g_c < 1/3g_0$.
- C_{dn} - the down-state capacitance, measured at V_{max}.
- V_{pi} - the pull-in voltage, measured when the switch is pulled-in, thus the capacitance increases from C_{up} to C_{dn}.
- V_{pi_R} - the ohmic pull-in voltage, measured when the ohmic contact is closed, thus the resistance drops to approximately R_s.
- V_{po_R} - the pull-out voltage, measured when the switch is pulled-out, thus the RF line is open and consequently the resistance suddenly increases.
- R_s - the switch resistance, measured at V_{max}, which is a sum of the resistance of the transmission line and the resistance of the ohmic contact.

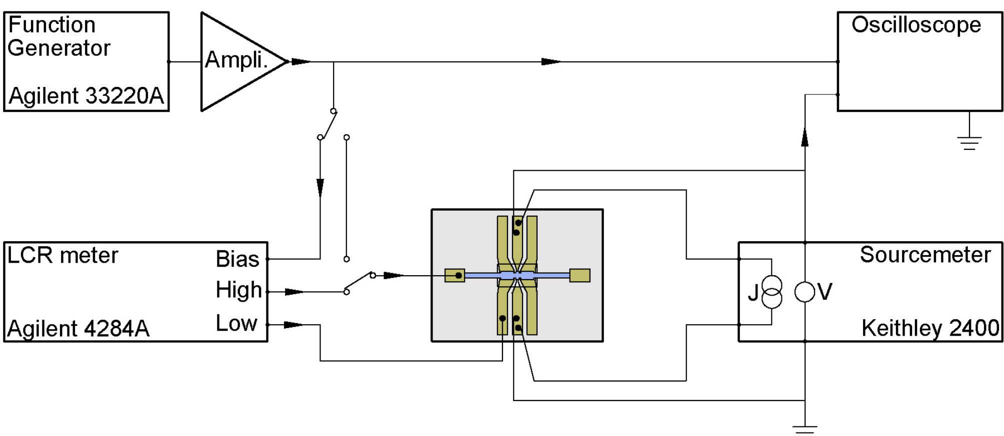


Figure 2.20: Block diagram of CarOhm test setup for electrical characterization of MEMS switches

In case of the capacitance, for easier comparison of the wafers, it is better to use the difference between the up-state and down-state capacitance (denoted as ΔC_{max}) and between the up-state and pull-in capacitance (denoted as ΔC_{pi}), rather than the absolute values:

$$\Delta C_{max} = C_{dn} - C_{up} \tag{2.50}$$

$$\Delta C_{pi} = C_{pi} - C_{up} \tag{2.51}$$

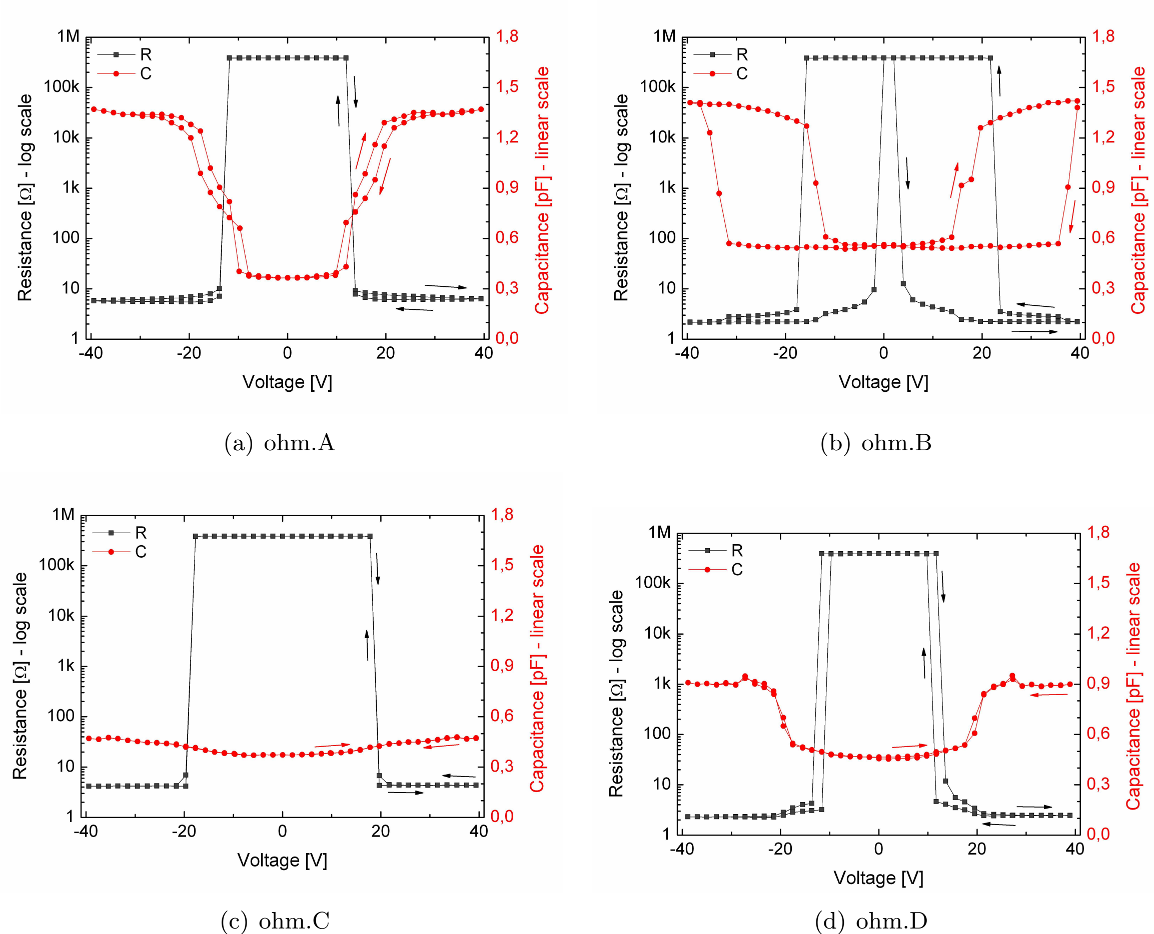
Test setup
The test setup used for the electrical characterization of the ohmic-type RF MEMS switches consists of a wafer probe station equipped with a probe card and a dedicated CarOhm test-bench for electrical characterization. The CarOhm test-bench, has been designed at the LCFM, specifically for the electrical test on MEMS switches. Its block diagram is presented in Figure 2.20. The actuation voltage, is sourced from an Agilent 33220A function generator and it is then amplified. The switch capacitance is measured with an Agilent 4284A LCR-meter and the switch resistance is measured with a Keithley 2400 source-meter using a 4-point method. The test equipment is controlled by a LabView based program, for automated tests on wafers.

2.6.2.2 Test samples

The C-V and R-V sweeps are measured for packaged ohmic-type switches for all 4 wafers. The number of switches tested for each wafer is ranging from 5 to 16.

2.6.3 Results of electrical tests

Representative C-V and R-V sweeps, for all 4 wafers of the ohmic-type switches, are presented in Figure 2.21. For easier comparison of these experimental results, the sweeps are plotted in the same scale, regardless the tested wafer.



(a) ohm.A (b) ohm.B

(c) ohm.C (d) ohm.D

Figure 2.21: C-V and R-V sweeps

The average values of the parameters which have been extracted, along with one standard deviation, are summarized in Table 2.15 for the ohmic response and in Table 2.16 for the capacitive response. The values of ΔC_{max} and ΔC_{pi} are presented separately in Table 2.17.

From the Figure 2.21 and the tables, it is apparent that each of the investigated wafers shows a different electrical behavior, in terms of pull-in voltages, the capacitance and the switch resistance.

For instance, the measured ohmic pull-in voltage V_{pi_R}, which depends mostly on beam stiffness and the electrode and contact gap, ranges from as low as 5.2 V for the ohm.B wafer to almost 21.0 V for the ohm.C wafer.

The maximum measured difference between the down-state and the up-state capacitance ΔC_{max}, which reflects the state (roughness) of the contact parts (the top and bottom electrodes), is 0.99 pF, for the ohm.A, while the minimum value is 0.11 pF, for the ohm.C wafer. Consequently, the ratio of down- to up-state capacitance C_{dn}/C_{up} varies from 3.5 for the ohm.A wafer up to 1.3 for the ohm.C wafer.

In terms of the switch resistance R_s, which depends on the contact quality, it ranges from

Table 2.15: Summary of results of electrical tests - ohmic response

Wafer	No. of switches	V_{pi_R} [V]		V_{po_R} [V]		R_s [Ω]	
		Av.	S.D.	Av.	S.D.	Av.	S.D.
ohm.A	6	13.8	<1	11.2	1.1	4.0	1.6
ohm.B	9	5.2	1.7	22.5	1.1	2.2	0.4
ohm.C	16	21.0	4.7	17.6	3.5	5.9	1.8
ohm.D	5	13.6	1.4	10.7	1.5	2.7	0.2

Table 2.16: Summary of electrical tests - capacitive response

Wafer	No. of switches	V_{pi} [V]		C_{up} [pF]		C_{pi} [pF]		C_{dn} [pF]	
		Av.	S.D.	Av.	S.D.	Av.	S.D.	Av.	S.D.
ohm.A	6	13.8	<1	0.39	0.03	0.81	0.06	1.37	0.04
ohm.B	9	16.0	1.8	0.50	0.05	0.50	0.05	1.36	0.07
ohm.C	16	n/a		0.44	0.10	0.49	0.11	0.55	0.13
ohm.D	5	19.9	1.6	0.46	0.01	0.51	0.02	0.90	0.02

2.2±0.4 Ω for the ohm.B wafer to 5.9±1.8 Ω for the ohm.C wafer.

The experimental results presented in this paragraph, will be discussed in the light of theoretical calculations and the SEM, AFM and FIB observations in paragraph 2.7.

2.6.4 Results of electro-mechanical modeling

2.6.4.1 Calculation of capacitive response

In this paragraph the electrostatic model (equation 2.44) is used to calculate the theoretical capacitive response of the ohmic-type switches. The input parameters for this model are:

- *The effective electrode gap* $g_0 + R_{max}$

  The electrode gap g_0, measured by the nanoindentation does not include the roughness or height of the peaks present on the surface of the contacting electrodes, which prevents these elements from contact. Consequently the value of g_0 is not representative of the real

Table 2.17: Summary of electrical tests - ΔC

Wafer	No. of switches	C_{dn}/C_{up}	ΔC_{max} [pF]		ΔC_{pi} [pF]	
			Av.	S.D.	Av.	S.D.
ohm.A	6	3.5	0.99	0.03	0.42	0.05
ohm.B	9	2.7	0.86	0.06	0.01	0.01
ohm.C	16	1.3	0.11	0.04	0.05	0.02
ohm.D	5	2.0	0.45	0.02	0.06	0.02

Table 2.18: Measured and calculated capacitive response

Wafer	g_c [nm]	g_0 [nm]	$g_0 + R_{max}$ [nm]	ΔC_{max} [pF]		ΔC_{max}^{calc} [pF]	ΔC_{pi} [pF]		ΔC_{pi}^{calc} [pF]
				Av.	S.D.		Av.	S.D.	
ohm.A	650	755	805	0.99	0.03	0.97	0.42	0.05	0.40
ohm.B	140	650	710	0.86	0.06	0.81	0.01	0.01	0.03
ohm.C	260	490	980	0.11	0.04	0.10	0.05	0.02	0.04
ohm.D	225	645	800	0.45	0.02	0.42	0.06	0.02	0.05

separation distance between the top and the bottom electrode. To obtain the real value of the electrode gap, the value g_0 is corrected by adding the maximum peak heights R_{max}, measured by the AFM.

- *The electrode gap* g_0

  The electrode gap g_0, measured by the nanoindentation, corresponds to the maximum distance traveled by the top electrodes.

- *The contact gap* g_c

  The contact gap g_c, measured by nanoindentation, corresponds to the distance traveled by the mobile contact and the side electrodes to close the contact.

The above mentioned parameters are used to calculate the following characteristic values of capacitance, that have been measured in the previous paragraph:

- *Up-state capacitance* C_{up}^{calc}

  The up-state capacitance C_{up} is calculated for the real value of the electrode gap, that is $g_0 + R_{max}$.

- *Closed-contact capacitance* C_{pi}^{calc}

  The closed contact capacitance C_{pi} is calculated for the deflection of the top electrodes $z_s = g_c$, taking into account the fact that the real value of the electrode gap is always $g_0 + R_{max}$.

- *Down-state capacitance* C_{dn}^{calc}

  The down-state capacitance takes into account that the top and the bottom electrodes are separated in the down-state, due to surface roughness (and hillocks). The C_{dn} is calculated for the deflection of the top electrodes $z_s = g_0$, taking into account the fact that the real value of the electrode gap is always $g_0 + R_{max}$.

The results of these calculations are presented in Table 2.18. The calculated capacitance shows no discrepancy, compared to the measured one. This good agreement between the theoretical and experimental capacitance confirms the pertinence of the gap heights measured by nanoindentation and corrected by the maximum values of surface peak heights, measured by the AFM.

Table 2.19: Measured and calculated pull-in voltage

Wafer	g_c [nm]	$g_0 + R_{max}$ [nm]	$g_c/(g_0 + R_{max})$	$k_{2_{2F}}$ [N/m]	V_{pi_R} [V]		$V_{pi_R}^{calc}$ [V]	V_{pi}^{calc} [V]
					Av.	S.D		
ohm.A	650	805	0.81	141	13.8	<1	11.0	11.0
ohm.B	140	710	0.20	244	5.2	1.7	11.1	12.3
ohm.C	260	980	0.27	163	21.0	4.7	15.3	15.7
ohm.D	225	800	0.28	157	13.6	1.4	11.2	11.6

2.6.4.2 Calculation of ohmic response - pull-in voltage

In this paragraph the electro-mechanical model is used to calculate the theoretical pull-in voltage V_{pi} and V_{pi_R}) using the equation 2.49. The input parameters, for this model, are:

- *The effective electrode gap* $g_0 + R_{max}$

  To obtain the correct value of the pull-in voltage it is necessary to know the real value of the gap between the top and bottom electrodes, that is the corrected value $g_0 + R_{max}$. Using the value g_0 would result in an important underestimation of the calculated pull-in voltage, for switches with rough electrodes.

- *The ratio between the contact gap* g_c *and the effective electrode gap* $g_0 + R_{max}$

  When the $g_c/(g_0 + R_{max})$ is lower than 1/3, the ohmic contact is closed before the pull-in phenomenon occurs. In this case, the ohmic contact is closed at the ohmic pull-in voltage $V_{pi_R}^{calc}$, which is lower than the (capacitive) pull-in voltage V_{pi}^{calc} when the whole beam is pulled-in. When the value of $g_c/(g_0 + R_{max})$ ratio is higher than 1/3, the ohmic contact is closed after the beam pull-in occurs. In this case the ohmic pull-in voltage $V_{pi_R}^{calc}$ is equal to the (capacitive) pull-in voltage V_{pi}^{calc}.

- *The calculated stiffness* $k_{c_{2F}}^{calc}$

  The stiffness value, which is put into the model (equation 2.49), is a theoretical value of the stiffness at the beam center, when two concentrated normal loads are applied at the electrode centers $k_{c_{2F}}^{calc}$.

The results of the calculations of the ohmic pull-in voltage are presented in Table 2.19. The calculated values of the pull-in voltages are typically 2-4 V lower than the measured ones (including one standard deviation), for all investigated wafers, except for the ohm.B wafer, where this difference is higher.

In case of 3 out of 4 investigated wafers, the contact gap g_c is lower than 1/3 of the effective electrode gap $g_0 + R_{max}$, which signifies that the ohmic contact short-circuits the RF-signal line, before the beam is pulled-in. The difference between the calculated values of $V_{pi_R}^{calc}$ and V_{pi}^{calc} does not exceed 1.2 V, which is the largestt difference obtained for the ohm.B wafer.

A possible source of the generally observed underestimation of the pull-in voltage may be the assumption that the electrostatic (actuation) forces can be reduced to two concentrated normal loads, while for the real switches these loads are distributed along the length of the electrodes.

As a consequence the stiffness which is put into the equation is underestimated, which could explain why the model produces underestimated values of the ohmic pull-in voltage.

2.7 Discussion of electro-mechanical behavior

Ohm.A wafer

The typical electrical response for the ohm.A wafers is presented in Figure 2.21(a).

This wafer is generally characterized by a moderate ohmic pull-in voltage $V_{pi_R} = 13.8$ V, which is equal to the capacitive pull-in voltage $V_{pi} = 13.8$ V. This moderate V_{pi} results from a combination of the lowest stiffness value $k_c = 79$ N/m and a moderate electrode gap $g_0 + R_{max} =$ 805 nm. The measured capacitive and pull-in voltages are equal, which is due to the fact that the contact gap g_c is higher than 1/3 of the effective electrode gap $g_0 + R_{max}$, thus the ohmic contact is closed after the beam is pulled-in. The ohm.A wafer is the only one, where the $g_c > g_0 + R_{max}$.

This wafer has the hlargest C_{dn}/C_{up} ratio, which is 3.5. The ΔC_{max} =0.99±0.03 pF is the highest from all the investigated wafers. All these is an evidence that this wafer has the smallest gap between the top and the bottom electrodes, when it is in the down-state. This small gap is confirmed by the SEM observations and AFM measurements of the roughness of the electrodes, which shows that this wafer has the smoothest surface for both the top and bottom electrodes.

This wafer has also the largest value of ΔC_{pi} = 0.42±0.05 pF, which is explained by the larger value of the contact gap. This switch has to travel the longest distance, to close the ohmic contact, thus this capacitance change is the largest from all investigated wafers. This observation is in agreement with the measurements of the contact and electrodes gap, by nanoindentation.

The switch resistance is $R_s = 4.0 \pm 1.6$, which classifies this wafer at 3rd place (out of 4) in terms of the resistance value. Not only the value of the resistance itself is high, but also the standard deviation is high and comparable with those of the ohm.C wafer only. The poor contact quality can be explained by the lowest contact force amongst all wafers and the high roughness of the surface of the mobile contact, observed by the SEM microscope. It is worth noticing that the ohm.A wafer uses the standard process flow of contact fabrication, where the polymeric resist for contact fabrication is unprotected during stripping off the mask for contact fabrication.

Ohm.B wafer

The typical electrical behavior for the ohm.B wafer is showed in Figure 2.21(b).

This wafer is the most interesting, in terms of the pull-in and pull-out voltages. It has the lowest ohmic pull-in voltage $V_{pi_R} = 5.2$ V amongst all the wafers. This can be explained by a very small contact gap as measured by nanoindentation ($g_c = 140$ nm). Because of this small gap, the ohmic contact is closed, before the beam is pulled-down. This situation is reflected in the measured value of the capacitive pull-in voltage $V_{pi} = 16.0$ V, which is relatively high, when compared to the ohmic pull-in. The small contact gap is further confirmed by an observation that several of the tested switches remain permanently in the closed position, which is due to an insufficient restoring force, which is lower compared to all other wafers.

What is astonishing is that, this is the only wafer for which the pull-out voltage V_{po} is higher (!) than both pull-in voltages. This phenomenon cannot be explained by a simple electro-mechanical model. The likely explanation of this observation, could be a very fast build-up of

a parasitic charge in the dielectric layer between the top and the bottom electrodes, which is creating some additional electrostatic force.

This wafer has the second highest C_{dn}/C_{up} ratio, which is 2.7. In terms of capacitance, this wafers resembles the ohm.A wafer, with easily distinguishable down-state and up-state capacitance. The ΔC_{max} =0.86±0.06 pF is comparable to the ohm.A wafer, which is a consequence of smooth electrodes. The slightly lower C_{dn}/C_{up} ratio and the value ΔC_{max}, compared to the ohm.A, can be explained by the higher roughness of the top electrode, which results in a slightly lower value of C_{dn}.

The ΔC_{pi} = 0.01±0.01 pF, is comprised within the measurement error and is definitely the lowest of all the wafers. It results from the very low contact gap.

The switch resistance is R_s = 2.2 ± 0.4, which classifies this wafer at the 1st place (out of 4) in terms of the resistance value. The ohm.B, is the wafer for which the optimized contact fabrication flow was used for the first time. The SEM observations revealed that the surface of the mobile contact has improved compared to the ohm.A wafer, but it is still rough, while the FIB cross-sections revealed a problem with adhesion of the under-layer of the mobile contact. Despite these problems, the resistance is the lowest from all tested wafers and the most likely explanation of this observation is the high contact force, which is several times higher than for the other wafers, which results in good contact of the mobile contact and the RF-transmission line.

Ohm.C wafer

A representative electrical response for the ohm.C wafer is presented in Figure 2.21(c).

Switches from this wafer have the highest ohmic pull-in voltages, which is V_{pi_R} = 21.0± 4.7 V and which results from a combination of a very high stiffness k_c = 132 N/m and the highest effective electrode gaps $g_0 + R_{max}$ = 980 nm. The capacitive pull-in voltage V_{pi} cannot be determined for this wafer, as there is hardly any change in the capacitance measured over the entire C-V sweeps.

This ohm.C wafer has the lowest C_{dn}/C_{up} ratio, which is 1.25 and the value of ΔC_{max} = 0.11±0.04 pF is also the lowest for all the wafers. This low value suggests that there is a considerable gap between the top and the bottom electrodes, in the down-state. This is confirmed by the SEM observations and the AFM measurements, where it was been possible to observe the hillocks as high as the half of the initial contact gap g_c, which prevents the top and bottom electrodes from contact.

The value of ΔC_{pi} = 0.05±0.02 pF is comparable with the value for the ohm.B wafer. It signifies that the contact gap is much lower than the effective electrode gap.

The contact resistance R_s = 5.9±1.8 Ω is the highest from all the wafers and it also exhibits the highest scattering, which is similar to the ohm.A wafer. This can be explained by a combination of a low contact force and high roughness of the mobile contact. It is worth noticing, that the mobile contact was intended to be fabricated with the optimized process flow, where the layer of polymeric resist is protected. The experimental results show, however, that during the fabrication process through holes have been etched in the SiN_x layer instead of blind holes and the polymeric resist was deteriorated, as it is the case in the standard process.

Ohm.D wafer

The typical electrical behavior of the ohm.D wafer is presented in Figure 2.21(d).

The ohmic pull-in voltage V_{pi_R} =13.6±1.4 V is similar to the pull-in voltage of the ohm.A

wafer, while the capacitive pull-in voltage V_{pi} =19.9±1.6 V is higher than for the ohm.A. This difference between these two voltages is due to the contact gap being below 1/3 of the effective electrode gap $g_0 + R_{max}$, which is confirmed by the nanoindentations and AFM measurements.

This wafer has the C_{dn}/C_{up} ratio equal to 1.95. The ΔC_{max} =0.45±0.02 pF places this wafer between the ohm.A, ohm.B and the ohm.C. This medium value of capacitance results mostly from the relatively high roughness of the bottom electrode, due to modification of the poly-silicon and silicon dioxide under-layers.

The ΔC_{pi} = 0.06±0.02 pF is similar to the values obtained for the ohm.B and ohm.C wafers, which is due to similar contact gap heights.

The resistance R_s = 2.7±0.2Ω classifies this wafer at 2nd place (out of 4) in terms of the resistance. This result is a combination of a very good contact quality (smooth, planar surface as observed by the SEM) and a relatively high contact force. The very high contact quality is confirmed by a very low standard deviation of the measured switch resistance.

2.8 Conclusions

An analytical electro-mechanical model of the ohmic-type switch has been developed and positively validated in this chapter. It has been demonstrated how this model can be used to calculate accurate theoretical electrical responses of the ohmic-type switches, provided that their geometry and mechanical properties are known.

To identify the mechanical properties (stiffness) and the geometry (electrode g_0 and contact g_c gaps) of the ohmic-type switches, the nanoindentation technique has been successfully implemented. It has turned out that the nanoindentation technique has not been sufficient to measure the real values of the contact gaps. In this case, the nanoindentation measurements have been completed by the AFM topography measurements of the top and the bottom electrodes.

From the obtained results it can be concluded that:

- The (capacitive) pull-in voltage V_{pi} is sensitive to the beam stiffness, the electrode gap height g_0 and the area of the actuation electrodes A_{el}. The lower the stiffness and the electrode gap and the higher the area of the actuation electrodes, the lower the pull-in voltage is.

- The switch stiffness turns out to be strongly dependent on the residual stress induced in the beam (PECVD SiN_x). The possibility to control this stress during deposition of the SiN_x offers a potential of quick and reliable adjusting of the pull-in voltage for fabricated switches

- The stiffness at the electrodes centers when two normal forces simultaneously applied at the electrodes centers is approximately 1.8 times higher than the stiffness at the beam center when only one normal load is applied at the beam center. Practical consequence of this observation is that the minimum force required to close the switch, is at least 1.8 times higher, when there are two sides electrodes, compared to a situation, where an actuation electrode is located at the beam center. Consequently, in our ohmic-type switches, it is necessary to apply higher voltage to the side electrodes than it would be necessary in case there was one central actuating electrode.

- The restoring force depends on the contact gap and the stiffness at the beam center, which has the lowest value in the central position along the beam. A low contact gap may result in an insufficient restoring force which may lead to permanent stiction of the switches, as it is the case for the ohm.B wafer.

- The contact forces depend on the difference of the separation distance between the electrode and the contact gap. The higher this difference is, the highest the contact force. In our case, the contact force is typically several times higher than the restoring force for each investigated samples. As it has been demonstrated, on the example of ohm.B wafer, a high contact force improves the contact between the mobile contact and the RF-signal transmission line and may lead to reduction of the switch resistance. On the other hand, the high contact force may promote degradation of the ohmic contacts with time reducing their lifetime. the influence of the contact force on the long term behavior of the ohmic contacts has not been investigated in this thesis.

- The optimized process flow of contact fabrication, where the polymeric resist is protected during stripping of the mask, results in a much more homogeneous contact surface. Nevertheless, it is critical to properly control the etching depth of the SiN_x beam to avoid etching a through hole, which has been done for the ohm.C wafer.

- The optimized poly-Si and SiO_2 layers (ohm.D wafer) have a higher roughness, compared to the previous technology. This roughness is transferred to the upper layers, which results in a lower C_{dn}/C_{up} ratio, which has a negligible effect on the functioning of the ohmic-type RF-MEMS switches. The roughness level is acceptable as it does not hinder the closing of the ohmic contact.

- Care should be taken during fabrication processes following the deposition of gold (the bottom electrodes and the RF-signal transmission line) to avoid formation of hillock on the gold surface, as these may obstruct the functioning of the switch (ohm.C wafer). To avoid hillocks formation an excessive thermal treatment should be limited (temperature should be kept below 280°C) and care must be taken to remove carefully residues of resists as it promotes formation of the hillocks.

- The difference between the capacitive and ohmic pull-in voltage is an evidence that the contact gap is smaller than 1/3 of the effective electrode gap, that is the contact is closed before the pull-in occurs.

- The switch capacitance, measured during electrical test, can be effectively used to calculate the approximate contact and electrode gaps, and the separation between the top and the bottom electrode in the down-state. A low ratio of the down- to up-state capacitance C_{dn}/C_{up} suggests a large separation between the electrodes in the down state, such as hillocks in case of the ohm.C wafer, or a higher roughness of the bottom electrode, as in the case of the ohm.D wafer.

Chapter 3

Structural and electrical properties of PECVD SiN_x and SiO_2

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3.1 Introduction

Dielectric charging is a key failure mechanism in electrostatically actuated RF-MEMS switches. It consists of trapping of parasitic charge in the dielectric layer separating the electrodes, under the influence of a high electric field (of magnitude of approximately 0.2 to several MV/cm). Despite extensive research, in the recent years, the physics of charge trapping in RF-MEMS is still unclear and remains a topic of ongoing research.

This chapter is aimed at studying the structure and electrical properties of low-temperature PECVD[1] SiN_x and SiO_2 dielectrics, which are the same as those which have been used for fabricating the RF-MEMS switches.

The first part of this chapter is focused on the analysis of a structure and composition of the dielectrics. It consists of TEM[2] imaging of the structure and elemental analyses by EDS[3], RBS[4], NRA[5] and ERDA[6] techniques for determining stoichiometry of the dielectrics and SIMS[7] technique for tracing depth-profiles of contaminations.

The second part is devoted to determining the electrical properties of the dielectrics, which include identification of conduction mechanisms and kinetics of charge trapping.

3.2 Background information

3.2.1 Definition of dielectrics

On account of their conductivity, materials can fall into one of three groups, which are metals, semiconductors and dielectrics [36].

In metals the valence band is full and the conduction band is partially full with delocalized electrons, which contribute to carrying electrical current [37].

In semiconductors and dielectrics, the valence and conduction bands are separated by a region of forbidden energies, which is called a band gap. Because of the non-overlapping bands, no current flow is possible until a sufficiently high electric field is applied. As a consequence the conductivity of semiconductors and dielectrics is lower, when compared to metals. A further distinction between semiconductors and dielectrics is done, by comparing the width of the band gaps. Dielectrics have larger gaps, which results in lower conductivity compared to semiconductors. Nevertheless, there is no explicit border line between these two groups.

3.2.2 Dielectrics in electronics and MEMS

The dielectrics, which are most commonly used for integrated circuits are thermally grown (900-1100°C) or fabricated by low pressure chemical vapor deposition technique (LPCVD), where the temperatures typically exceeds 500°C [38, 39]. In the last 40 years there has been a lot of effort put into research on the properties of these dielectrics, which significantly improved our understanding of their electronic behavior under specific conditions. This fundamental

[1] PECVD stands for Plasma Enhanced Chemical Vapor Deposition
[2] Transmission Electron Microscopy
[3] Energy Dispersive X-ray Spectroscopy
[4] Rutherford Backscattering
[5] Nuclear reaction Analysis
[6] Elastic Recoil Detection Analysis
[7] Secondary-Ion Mass Spectrometry

knowledge resulted in designing and fabricating more reliable devices. At the same time, plasma enhanced vapor deposition (PECVD) dielectrics were used in less demanding applications, such as diffusion barriers or passivation layers [39]. Because of the limited number of applications of PECVD dielectrics, the knowledge of the electronic properties of these materials was not critical so that less research has been carried out to characterize their properties compared, for example, to a thermal SiO_2. With time, the number of applications of the PECVD dielectrics has increased, but the poor understanding of their electronic properties became a serious obstacle for predicting the film behavior under given conditions, which prevented from fabricating reliable devices and their commercialization.

3.2.3 Applications of PECVD dielectrics

3.2.3.1 Principles of PECVD

Plasma enhanced chemical vapor deposition (PECVD) is a lower-temperature alternative to the standard LPCVD technique, which uses a plasma to enhance the reaction of the precursor gases. The energetic species are created by collisions in the gas, in high alternating electric field (up to 13.56 MHz). These excited species interact with the substrate, and depending on their nature, etching or deposition at the substrate surface occurs. As energy is transferred into the gas by the plasma, the substrate temperature can be lowered. Typically, the deposition of a variety of thin films by PECVD is possible at temperatures from 50 to 350 °C, without reducing its quality in comparison to films deposited by other CVD techniques [36].

A schematic drawing of a PECVD reaction chamber is presented in figure 3.1. A substrate is placed on a heated stage, below an electrode. A vacuum pump is used, for creating negative pressure, while a number of inlets provide the mixture of precursor and diluting gases at controlled flow rates.

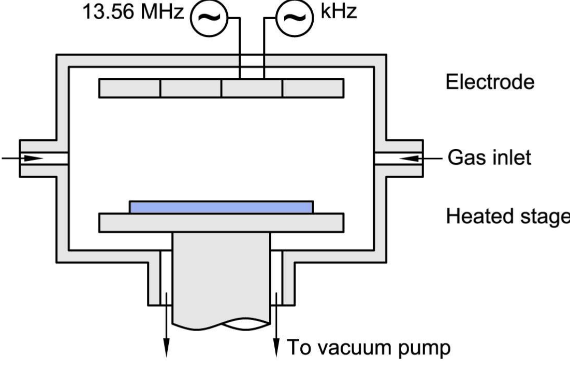


Figure 3.1: Schematic of PECVD chamber

The deposition conditions which are controlled are: the mixture of process gases, substrate temperature , pressure, power and frequency.

More information on the PECVD technique and influence on the deposition parameters on structural properties of SiN_x is provided in Appendix B.

Table 3.1: Comparison of selected properties of low temperature PECVD SiN_x and SiO_2 with high temperature LPCVD counterparts [39].

	SiN_x		SiO_2	
	PECVD	LPCVD	PECVD	LPCVD
Gas mixture	SiH_4+NH_4 or SiH_4+N2	SiH_4+NH_4 or $SiCl_2H_2$ + NH_4	SiH_4 +O_2 or SiH_4 +N_2O	$SiCl_2H_2$ +N2O
Temperature [° C]	250-350	700-850	250	900
Refractive index	1.85-2.5	2.01	1.45	1.46
Dielectric constant	6-9	6-7	3-6	10
Dielectric strength [MV/cm]	5	10	4.9	
Energy gap [eV]	4-5	5		

3.2.3.2 PECVD SiN_x in semiconductor devices

Silicon nitride is an amorphous dielectric, which is used in a wide range of semiconductor device technologies. It can be fabricated by a number of chemical-vapor deposition (CVD) techniques. Table 3.1 presents the process gases and selected properties of SiN_x fabricated by a low temperature PECVD contrasted with a high temperature LPCVD SiN_x.

High quality, stoichiometric SiN_x, with low hydrogen content (H < 5 at. %) is fabricated by LPCVD at temperatures exceeding 700°C [39, 40], typically by a reaction of silane (SiH_4) with ammonia (NH_3). Its main advantage is a very high dielectric strenght of 10MV/cm. A drawback of using LPCVD SiN_x is its very high tensile stress of +1 GPa.

Some applications, however, require the deposition temperature to be lower than 300-400°C. In such a case, silicon nitride can be deposited by PECVD, where the reaction gases remain the same, but the temperature is comprised between 250-350°C.

A consequence of this lower temperature is a lower quality of the PECVD film compared to LPCVD. The PECVD silicon nitride is non-stoichiometric and highly hydrogenated (up to 30-35 at. %) [36]. Its composition and its physical properties are very sensitive to the deposition parameters and to the purity of the process gases used. By modifiying the deposition parameters, it is possible to adjust the refractive index (1.85-2.5) or the dielectric constant (6-9), for a specific application, which is an unquestionable advantage of the PECVD technique. Intrinsic stresses, may vary from -0.6 GPa (compressive) to +0.6 GPa (tensile) and can be controlled in the most recent deposition equipment.

The main drawbacks of using the PECVD SiN_x are its lower dielectric strength (5 MV/cm instead of 10MV/cm for the LPCVD film), its higher porosity and its lower etching resistance. The PECVD technique has also a lower throughput, when compared to other CVD techniques.

Typical applications of the PECVD SiN_x in semiconductor technology are passivation layers, diffusion barriers and masking for wet chemical etching [39]. Among the required properties of these films, there are: uniformity of deposited film, absence of pinholes or cracks and resistance to subsequent fabrication processes, including thermal treatment.

A number of potential applications of the PECVD SiN_x have been investigated in the past [41–44]. A non-stoichiometric PECVD SiN_x was a candidate material in photovoltaics, because of the possibility of adjusting the optical band-gap, by changing the N/Si ratio in the deposited films, which was done by controlling the deposition parameters. To ensure a high photoconduc-

tivity, long recombination times were required. A stoichiometric PECVD SiN_x was also used as a potential gate dielectrics in thin film transistors (TFTs) and diodes. To ensure stability of these devices very low trap concentrations and leakage currents were required. Besides, for TFTs on flexible plastic substrates, the temperature had to be lower than 140°C. The stoichiometric SiN_x was investigated in metal-nitride-oxide-semiconductor devices (MNOS), as a charge storage material, where high trap concentrations were required.

More information on the influence of the deposition parameters is provided in Appendix B.

3.2.3.3 PECVD SiO_2 in semiconductor devices

Silicon dioxide is an amorphous dielectric, widely used in semiconductor industry. It is obtained by 2 different techniques, that is a thermal oxidation of Si or CVD techniques [1, 36].

A high quality SiO_2, which is used as a gate dielectric in complementary-metal-oxide semiconductor CMOS transistors is thermally grown.

From the dielectrics deposited by the CVD technique, the best properties shows LPCVD SiO_2, deposited from a mixture of dichlorosilane ($SiCl_2H_2$) and laughing gas N_2O (Table 3.1). This film is deposited at high temperature (900°C) which results in outgassing of hydrogen and densification of the film. This films has good uniformity of ±5%. Moreover, it has very high dielectric strength of 10 MV/cm, which is comparable to that of thermal silicon dioxide.

SiO_2 can be also obtained by the PECVD technique, from a mixture of silane (SH_4) and laughing gas (N_2O) at temperatures around 250°C. The lower deposition temperature, results in a much lower dielectric strength of the order of 3-6 MV/cm of as deposited SiO_2. The PECVD is the only technique, which enables controlling the compressive intrinsic stress in SiO_2. The stress is lower than +0,3 GPa. The uniformity of the PECVD SiO_2 films can be as good as ±5% that is comparable to the LPCVD films.

Main applications of the CVD deposited silicon dioxide include inter metal dielectric insulation, sacrificial and optical layers.

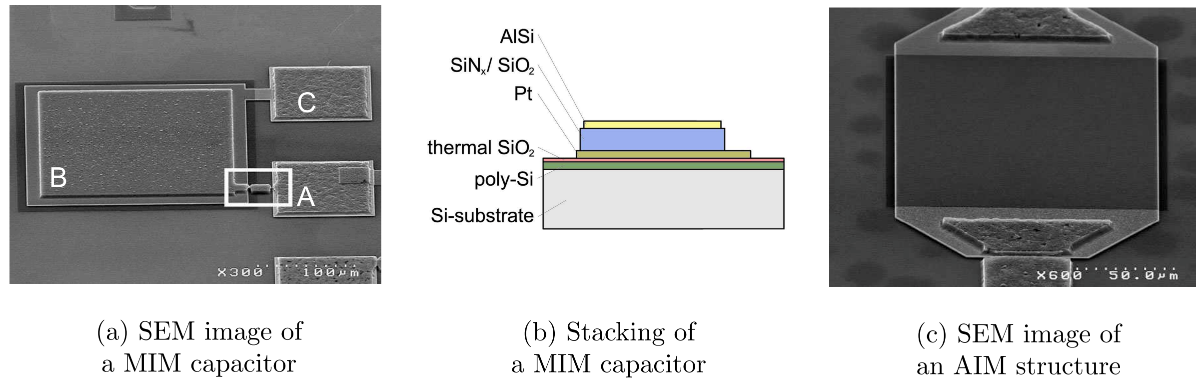
3.3 Test samples - general description

Unlike in the previous chapter, in this part more emphasis is put on the capacitive-type RF-MEMS switches and corresponding test structures. The capacitive-type switches are preferred because of two reasons which are a higher number of available test samples and simpler design:

- The movable (top) electrode is made of single-layer Al or AlSi, which provides better (more conformal) contact with the dielectric layer during actuation and consequently more uniform distribution of the electric field.
- A uniform-thickness, rectangular-shape dielectric, which is deposited on a bottom metallic electrode, which makes it easier to prepare samples for structural analyses.

3.3.1 Description of test samples

The test samples used in this chapter are metal-insulator-metal (MIM) capacitors and air-insulator-metal (AIM) structures (MEMS capacitive-type switches with no membrane), fabricated by CEA-Leti.



(a) SEM image of a MIM capacitor

(b) Stacking of a MIM capacitor

(c) SEM image of an AIM structure

Figure 3.2: SEM images of test structures: MIM-capacitors and AIM structures, together with schematical drawing of the stacking.

An SEM image of a typical metal-insulator-metal (MIM) capacitor used in this chapter is presented in Figure 3.2 (a) and its stacking is schematically presented in Figure 3.2 (b). The MIM-capacitors have two pads denoted as (A) and (C), where the first one is connected to the top electrode (B) and the latter is connected to the bottom electrode. The connection between the A-pad and the B-top electrode is removed prior to some electrical tests, by reason of high leakage current through the substrate to a grounded chuck, which could hinder measurement of the leakage current through the dielectric.

The MIM-capacitors are used throughout this chapter for TEM imaging and all electrical tests.

The AIM samples presented in Figure 3.2 (c) are used for elemental analyses. The stacking of these samples is the same as of the MIM-capacitors except that, there is no top electrode so the top surface of the dielectric is exposed to air, like in a real MEMS switch.

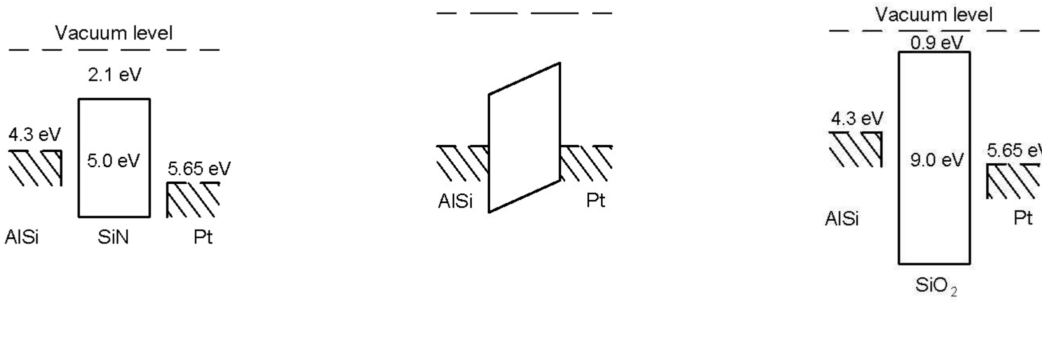
3.3.2 Band diagrams

Charge transport in an insulator may depend on a barrier height at the metal-insulator interface, as it will be presented later in this chapter. Figures 3.3 (a, b) and 3.3 (c) present the band diagrams of the MIM capacitors with PECVD SiN_x and SiO_2, respectively. It is apparent that these two materials exhibit significantly different band gaps: 5.0 eV for SiN_x and almost 9.0 eV for SiO_2 [39, 45]. Another point, worth noticing, is the difference of the Fermi levels, of the two Pt and Al or AlSi used for the electrodes, which exceeds 1.3 eV. When the electrodes and dielectric are put together (Figure 3.3) the Fermi levels of the two metals align.

3.3.3 Deposition of PECVD dielectric layers

The PECVD technique has been chosen to deposit the dielectric layers, primarily because of the low deposition temperature, which is required by the metallic layers deposited before the dielectric.

The deposition parameters are summarized in Table 3.2 for 4 wafers of RF MEMS capacitive-type switches and corresponding test structures.



(a) Band gap in SiN_x (b) Fermi level alignment (c) Band gap in SiO_2

Figure 3.3: Band diagrams of the test samples

A total number of 4 wafers with 3 different types of dielectrics are investigated in this chapter, which are high- and mixed-frequency PECVD SiN_x and mixed-frequency PECVD SiO_2.

Three wafers of PECVD SiN_x are obtained from a reaction of silane with ammonia with the substrate at 300°C. The only difference between these dielectrics is the deposition frequency. The capa.A and capa.B samples are deposited at high frequency (13.56 MHz) to induce tensile stress in the dielectric. The capa.C sample is obtained in mixed-frequency mode (mix of 13.56 MHz and 187.5 kHz) to induce compressive stress. The other deposition parameters remain the same.

One wafer of PECVD SiO_2 is obtained from a reaction of silane with laughing gas with the substrate at 150°C, which is half of the temperature for SiN_x deposition. This sample is denoted as the capa.D.

The capa.A wafer was fabricated several months before the other samples. The samples capa.B, capa.C and capa.D were fabricated in the same run.

The dielectrics described here are the same for the MIM-capacitors and the capacitive-type MEMS switches. The dielectric is incorporated in the same stacking sequence. The test structures and switches are fabricated on the same wafer, during the same process and they are submitted to the same subsequent fabrication steps, including post-fabrication annealing.

3.4 Structural analyses

3.4.1 Objective

This part of this chapter is aimed at determining the structure and composition of the 3 types of dielectrics used in the capacitive-type RF-MEMS switches. There is a total of 4 wafers, 2 wafers with HF SiN_x layers (different thickness and top electrode), 1 wafer with MF SiN_x layer and 1 wafer with MF SiO_x layer, as summarized in Table 3.2.

Table 3.2: Deposition parameters of PECVD SiN_x and SiO_2

Sample (wafer)	capa.A	capa.B	capa.C	capa.D
Dielectric	SiN_x	SiN_x	SiN_x	SiO_2
Process gases	SiH_4+NH_3	SiH_4+NH_3	SiH_4+NH_3	SiH_4+N_2O
Substrate temperature [° C]	300	300	300	150
Pressure [mTorr]	850	850	850	900
Power [mW]	100	100	100	250
Frequency	high[1]	high[1]	mixed[2]	mixed[2]
Deposition rate [nm/min]	30-40	30-40	9-12	230-260
Thickness [nm]	330	250	250	250
Substrate	Si - high-resistivity (1-99.9 kΩcm)			
Passivation layer	thermal SiO_2 - oxidation of poly-Si in O_2+HCl @ 1050° C			
Bottom electrode	Pt on Ti seed layer			
Top electrode	Al	AlSi	AlSi	AlSi
Power [kW]	n/a	12	12	6 (in 5 steps)
Substrate temperature [° C]	n/a	175° C	175° C	n/a
Annealing (in N_2)	n/a	15h @ 350° C	15h @ 250° C	15h @ 350° C

[1] 13.56 MHz
[2] mix of 13.56 MHz and 187.5 kHz frequencies

3.4.2 Literature review

3.4.2.1 Structural properties of PECVD SiN_x

PECVD SiN_x is an amorphous and non-stoichiometric dielectric, with a considerable amount of hydrogen up to 30-35 at.% [42] when deposited from silane SiH_4. This high amount of hydrogen in the film translates to lower density, when compared to SiN_x deposited by high-temperature CVD.

The stoichiometric silicon nitride is SiN_x, where the N/Si ratio is $x_{N/Si} = 1.33$. When the $x_{N/Si}$ exceeds the value of 1.33, the nitride has an excess of N atoms in the matrix and it is called N-rich and it is Si-rich when $x_{N/Si} < 1.33$.

The bonds in PECVD SiN_x are:

- *[Si-Si]*

  These are relatively weak bonds. They play an important role in defining the band gap. Increase in the amount of [Si-Si] bonds tends to raise the valence band E_V and lower the conduction band E_C, thus reducing the band gap. In Si-rich nitrides, the higher concentration of [Si-Si] results in lower refractive index [44], compared to more N-rich silicon nitride, where the refractive index is higher.

- *[Si-H]*

  These bonds are more likely to break than [N-H] [46]. They are not expected to create vacancies [43]. To increase the number of Si bonded to H the deposition temperature should be reduced [42]

- *[N-H]*

  These are stronger bonds than the [Si-H] [46]. These bonds are also not expected to create vacancies [43]. While the temperature is reduced the amount of hydrogen bonded to nitrogen decreases, while the amount of hydrogen bonded to silicon increases [42].

Some experiments show, that there is a non-linear correlation between the N/Si and the [N-H]/[Si-H] ratio and silicon nitrides with a higher N/Si ratio has also a higher [N-H]/[Si-H] ratio [42].

An initial defect density for a silicon nitride with N/Si ratio $x > 0.8$ ranges from 10^{12} to 10^{13} cm^{-2} and after a prolonged stress it stabilizes at 10^{13} cm^{-2} [43]. The defects are associated with the concentration of Si-dangling bonds[8] (Si-db) [44]. The trapping centers that have been identified in hydrogenated SiN_x include:

- *Si dangling bonds*

  This is the only defect found in the Si-rich silicon nitride. The trapping centers are located in the middle of the band gap [44] and are almost independent on the N/Si ratio up to $x_{N/Si} = 1.33$. The Si-db is a dominant recombination center for charge carriers [43]. The source of Si-db (Si_3^0) are weak [Si-Si] bonds and [Si-H] bonds, which are broken by an electron-hole recombination. This Si-db may trap both electrons or holes, forming Si_3^+ or Si_3^- centers [43]. These trapping centers can be reformed to Si-db by annealing or UV illumination. The Si_3^+ trap centers may react with [N-H] bonds, which leads to creation of [Si-N] bonds and excess (negative net concentration) of Si_3^- centers. This negative net concentration of trapping centers, is supposed to be responsible for the offset of I-V curves (hysteresis). The reaction of Si_3^+ centers with [N-H] is limited by the availability of the latter bonds, which can soon be exhausted in Si-rich silicon nitride, where they are present in small amounts. Consequently, more Si-rich nitrides should show lower offsets (hysteresis) in the I-V curves.

- *N dangling bonds*

  The N-db are found in N-rich silicon nitride only, and are believed to have a minor influence on the creation of the trapping centers [43, 44, 47]

3.4.2.2 Structural properties of PECVD SiO_2

Similarly to PECVD SiN_x, the layers of SiO_2 obtained by PECVD technique are amorphous, non-stoichiometric and contain, considerable amount of H [1].

Regarding the bonds present in the PECVD SiO_2 and their contribution to the trapping process little data is available.

3.4.3 Analysis of atomic structure

In this section the morphology, that is the atomic arrangement of the stack of the MIM-capacitors is analyzed.

[8] A dangling bond is an unsaturated atomic bond, which may interact with charge carriers

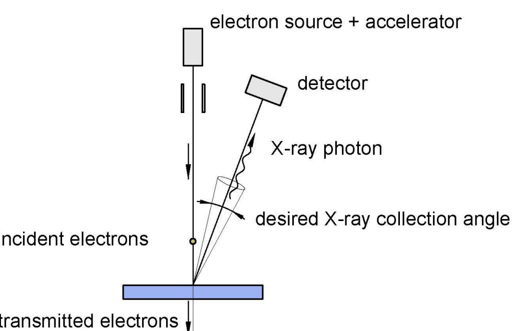


Figure 3.4: Schematic drawing of a Transmission Electron Microscope (TEM) equipped with Energy-Dispersive X-Ray Spectrometer (EDS).

3.4.3.1 Experimental procedure

Test method

Principles of TEM
Transmission Electron Microscopy (TEM) is an imaging technique, which is sensitive, in particular, to atomic arrangement (contrast), electron density and sample morphology [48–50]. TEM provides much higher resolutions, when compared to optical microscopy. The resolution limit in the latests TEM microscopes is 0.5-1Å. In this technique an image is obtained from the interaction of incident electrons and a thin specimen, as presented in Figure 3.4 and Figure 3.5(a).

In a typical TEM setup, which is presented in Figure 3.4, the incidents electrons are accelerated by a high-energy source of electrons, which is 200kV in our case. The beam of the electrons is controlled by electromagnetic lenses and electrostatic-plates. The transmitted and diffracted electron waves are used to create an image as presented in Figure 3.5 (a). By changing the objective aperture it is possible to select between the primary beam of transmitted electrons or a secondary beam of diffracted electrons or to chose both, to obtain following types of images:

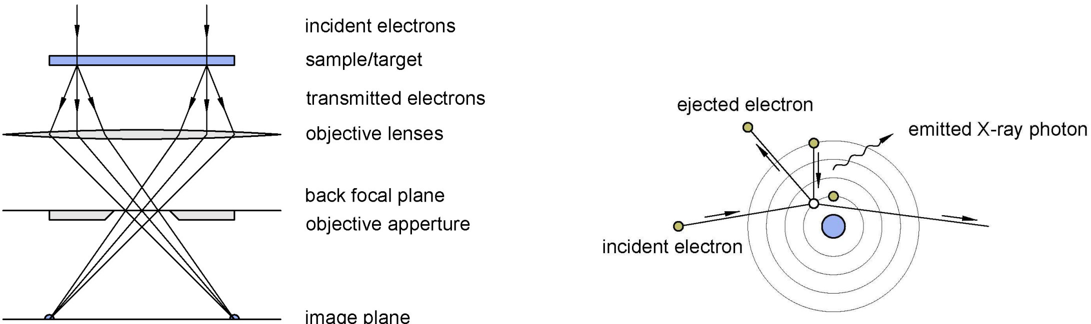
- *Bright-field image (BF)*

  For the BF images, the aperture in the back focal plane of the objective lenses permits only the primary beam to pass. As the primary beam is interacting with the atoms in the sample, it is weakening. For the elements with higher atomic masses the weakening is stronger. It results in a creation of the BF, where the elements with lower atomic masses appear brighter, than the elements with higher atomic masses.

- *Dark-field image (DF)*

  For the DF images, the aperture in the back focal plane of the objective permits only the diffracted beam to pass. If the sample is crystalline, the diffracted electrons are dispersed into discrete positions, which makes it possible to analyze the crystalline matrix and the type of the defects in the matrix.

- *High Resolution (HRTEM) image*



(a) Principles of image creation in TEM microscopy

(b) Generation of X-ray photons in EDS spectroscopy

Figure 3.5: Physical principles of Transmission Electron Microscopy (TEM) and Energy-Dispersive x-ray Spectroscopy (EDS)

For the HRTEM imaging, a large aperture is set, so it permits the primary and diffracted beam to pass. The image is created by analyzing a phase shift between the transmitted and diffracted electrons, which results in an interference pattern. This type of image makes it possible to directly investigate the structure of the sample.

TEM imaging requires sophisticated preparation of the sample. The quality of the image depends on the thickness of the sample, which should be as thin as possible to improve transmission of the electrons through it. A typical sample has a form of thin lamella of analyzed structure prepared by FIB technique.

Principles of EDS

Energy-Dispersive X-ray Spectroscopy (EDS) is an analytical technique, which is used for elemental and compositional analysis of materials [48, 51, 52]. The elements are identified by analyzing the X-rays, which are emitted from the sample after being hit by incident charged particles.

In this technique a beam of electrons or X-rays, accelerated to high-energy, is focused on a surface of the sample (Figure 3.4). The incident beam collides with an electron in an inner shell of an atom, as shown in Figure 3.5 (b). After being struck, this electron is emitted, leaving a vacancy. This vacancy is immediately filled by an electron from one of the outer shells and the excess of energy (difference between the energy of the electrons in outer and inner shells) is emitted as X-ray photons. The X-rays are analyzed by an Energy-Dispersive Spectrometer, which counts the number of X-rays and their energy. Each level of the emitted X-ray energy is characteristic to the difference in energy between the two shells and it depends on the atomic structure of an element, which is why it can be effectively used to distinguish between the elements.

The EDS technique fails to identify the elements with atomic numbers $Z < 4$, that is H, He and Li. Moreover, some elements may have overlapping peaks in the energy spectra, which may hinder their identification.

Test setup
To acquire atomic resolution images of the MIM-capacitors Transmission Electron Microscope (TEM) JEOL 2100F (200kV), with a probe size under 0.2 nm is used. This TEM is equipped with INCA Energy TEM 200 Energy-Dispersive X-ray Spectrometer (EDS) from Oxford Instruments, which allows in situ analysis of the sample composition.

Test samples
The test samples, which are analyzed by the TEM microscopy and EDS spectroscopy are MIM capacitors with 3 types of dielectrics HF SiN_x (capa.B), MF SiN_x (capa.C) and MF SiO_2 (capa.D). For the capa.D wafer an AIM structure has been also analyzed.

Prior to the measurement all samples have been prepared by FIB, by removing the material to create a wedge-shape thin sheet sample in the area of interest.

3.4.3.2 Results

TEM results
The Figure 3.6 show a typical TEM bright-field image of a cross-section of the capa.C MIM-capacitor. The presented figure is representative of all tested wafers. In this figure, we can see a complete stacking of the MIM-capacitors. Starting from bottom to top, there are: a high-resistivity Si substrate, approximately 700 nm of poly-Si, approximately 300 nm of thermal SiO_2, 20 nm of Ti seed layer, 500 nm of Pt, 250 nm of amorphous SiN_x and 2 µm of AlSi. It is worth reminding, that the contrast in this TEM image corresponds to the atomic mass of the elements, where the higher the mass, the darker the image.

The TEM observations confirm the thickness of the dielectric layer measured after the deposition on a dummy wafer, which is approximately 250 nm for capa.B, capa.C and capa.D wafers. The thickness of the dielectric is uniform, along the examined length of the sample, but the surface of the dielectric is very rough. The maximum peak to valley distance at the dielectric surface is approximately 50 nm, which correspond to 20% of the total thickness of the dielectric. This observed waviness is due to a high roughness of the poly-Si layer deposited on the Si-substrate, which is then transferred to all upper layers.

The TEM microscope is also used to examine the transition region between the insulator and the top- and the bottom electrodes. Typical images are presented in Figure 3.7 for the capa.C wafer. As in the previous example these observations are representative for all investigated samples, including capa.D wafer (with SiO_2).

The transition region between AlSi top electrode and SiN_x dielectric is presented in Figure 3.7 (a). In this figure we can see that both AlSi and SiN_x are amorphous. The AlSi alloy, which is heavier than SiN_x appears darker in this image. At the transition region, there is no apparent change in the structure of the dielectric and the top electrode.

The transition region between SiN_x dielectric and Pt bottom electrode is presented in Figure 3.7 (b) and in Figure 3.7 (c), where the interface is magnified. In the Figure 3.7 (b), there are visible darker spots embedded in the dielectric layer, within a distance of 2 to 10 nm from the surface of the metallic electrode. The darker color indicates elements of higher atomic mass than the elements present in SiN_x. After magnification of the interface (Figure 3.7 (c)) it is apparent that these darker spots have a crystalline structure, in contrast to the amorphous dielectric. The lattice constant of these dots is comparable with the lattice constant of the crystalline

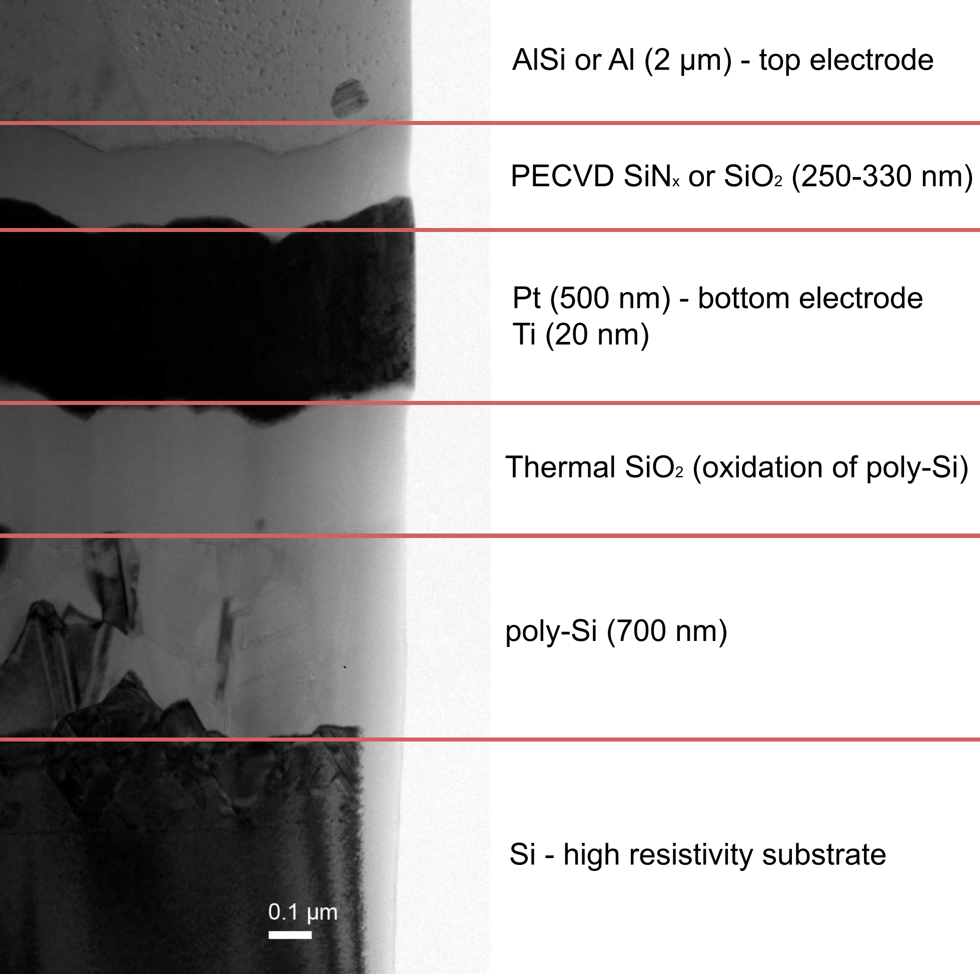
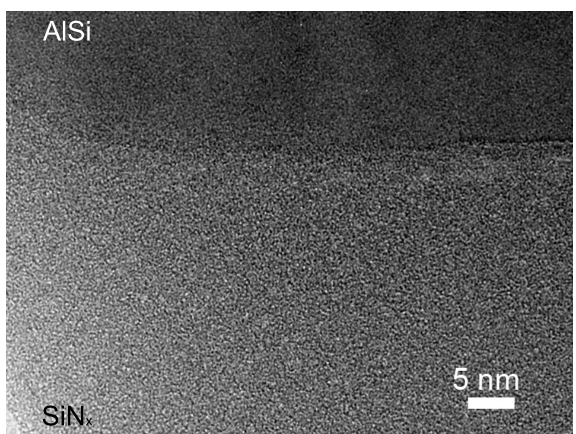
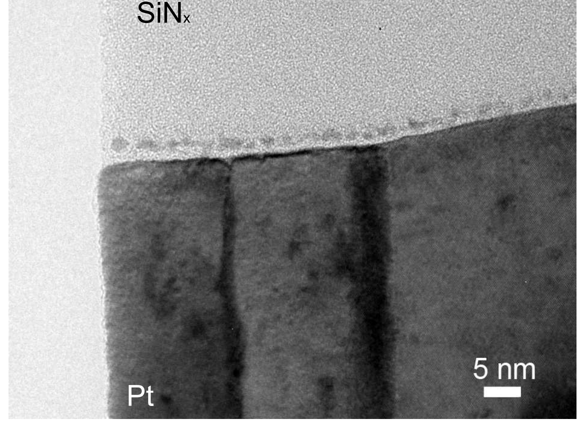


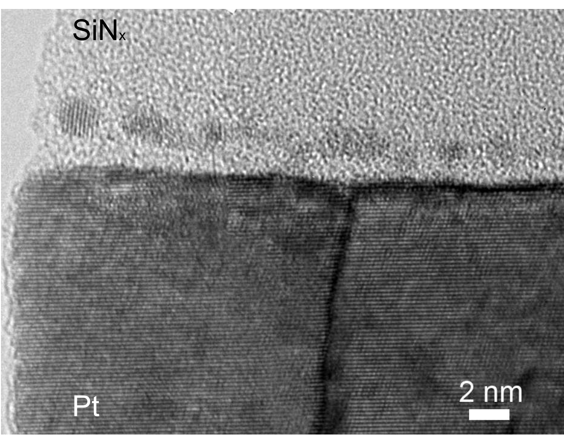
Figure 3.6: A typical TEM bright-field image of cross-section of capa.C MIM-capacitor, which is representative for all tested samples; darker areas in this figure correspond to elements with higher atomic numbers



(a) Top electrode - dielectric



(b) Dielectric - bottom electrode



(c) Dielectric - bottom electrode

Figure 3.7: Characteristic TEM bright-field images of the transition regions between the top electrode and the dielectric (a) and between the dielectric and the bottom electrode (b, c) in a capa.C MIM-capacitor.

Pt electrode underneath. However, the contrast of these spots is weaker than the contrast of the Pt electrode. To verify whether the crystalline spots are composed of Pt (as the electrode underneath) EDS measurements are carried out at the metal-dielectric interface.

EDS results
For compositional analysis EDS spectra are recorded at both dielectric interfaces. The results are presented in Figure 3.8 and 3.9 for SiN_x-AlSi and SiN_x-Pt interface, respectively. Each figure presents a number of EDS spectra, measured along a straight scan line, which consists of 8 to 11 points, as shown in the inlets in the figures. The signal of each spectrum is normalized to Cu signal (not shown), which is considered to be constant for each of the measurements [9].

The EDS spectra measured at the SiN_x-AlSi (dielectric-top electrode) transition region are

[9] The Cu signal is due to presence of copper in the column of the TEM and it is considered to be constant for all the measurements

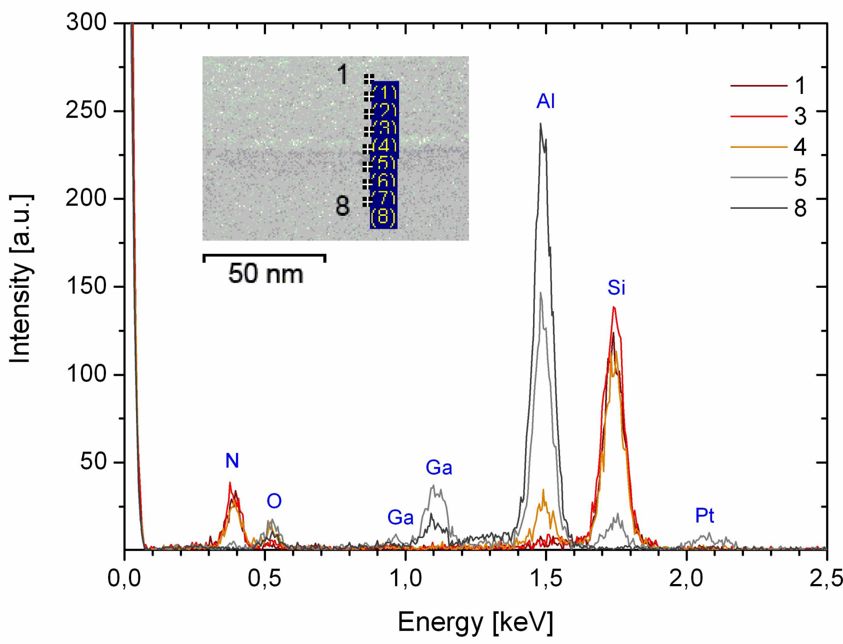


Figure 3.8: EDS spectroscopy at SiN_x-AlSi interface (dielectric - top electrode) measured for a capa.C sample.

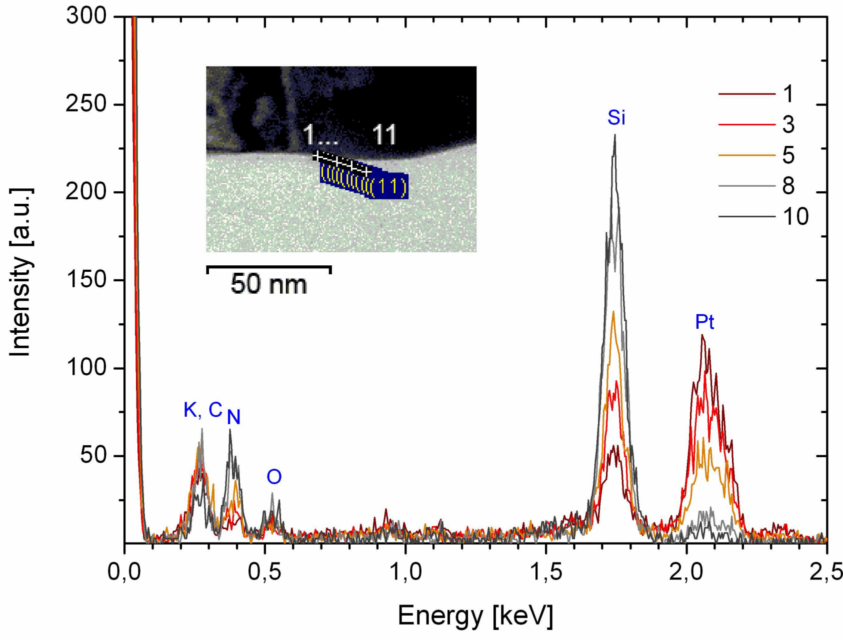


Figure 3.9: EDS spectroscopy at Pt-SiN_x interface (bottom electrode - dielectric) measured for a capa.C sample.

presented in Figure 3.8. The scan lines 1 to 4 are measured in SiN_x, and the lines 5-8 are measured in AlSi. In the dielectric layer, apart from Si and N, there is a considerable amount of O present, which tends to be higher at the interface (lines 4 and 5) rather than in the bulk of the dielectric (lines 1 and 3). Line 5, measured at the dielectric interface indicates traces of Pt and a considerable amount of Ga.

The EDS spectra measured at Pt-SiN_x (bottom electrode - dielectric) transition region are presented in Figure 3.9. The purpose of these measurements is to determine the material of the crystalline spots embedded in the dielectric. 11 measurements are taken in SiN_x, where the line 1 is the closest to the Pt surface and the line 11 is the farthest. These measurements confirm the previous observation, such as the presence of O in the dielectric. Unlike in the other interface, there is no trace of gallium at the bottom electrode-dielectric interface. On the other hand, at this interface, there are some additional elements, which are visible as overlapping peaks for very low energies. The elements can be identified either as K (peak at 0.262 eV) or C (peak at 0.277 eV) or both. Concentration of these two elements increases with decreasing distance to the bottom electrode and it is the highest in the range of 2 to 4 nm from the Pt surface.

The analyses taken at the dielectric-bottom electrode transition region, confirm that the metallic inclusions observed at the metallic interface are composed of Pt, as no other material has been identified. A possible explanation of the presence of Pt spots embedded in the dielectric, lays in the method of deposition. The PECVD technique involves the use of plasma, which can sputter Pt particles from the bottom electrode. These particles get into the gas mixture and are redeposited together with SiN_x, aggregating and creating these crystalline dots. This also explains why no such dots are observed at the opposite interface.

3.4.4 Quantitative analysis of Si, N, O and H elements

In this section we determine the stoichiometry of SiN_x and SiO_2 and the amount of H present in all 3 dielectrics, 2 types of SiN_x (HF, MF) and 1 type of SiO_2 (MF). The quantitative analysis of the main elements is carried out by three experimental techniques, which are complement to each other: RBS[10], NRA[11] and ERDA[12].

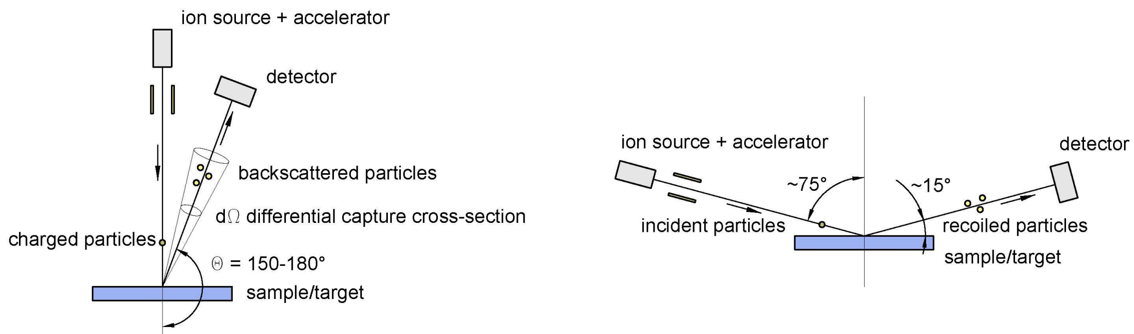
3.4.4.1 Experimental procedure

Test methods

Principles of Rutherford Backscattering (RBS)

Rutherford Backscattering Spectroscopy (RBS), also know as High-Energy Ion Scattering Spectrometry (HEIS), is an analytical technique, which is used for quantitative analysis of composition of materials [48]. A schematic drawing of the RBS test setup is presented in Figure 3.4.4.1 (a). Typical RBS spectrometer consists of an ion source (usually He^+, rarely protons), an accelerator, which accelerates incident ions to energies as high as 1-3 MeV and a detector, which measures the energy of backscattered ions over a selected range of angles Ω.

[10] Rutherford Backscattering
[11] Nuclear Reaction analysis
[12] Elastic Recoil Detection Analysis



(a) RBS test setup (b) ERDA test setup
Schematic drawing of RBS and ERDA test setups

In the RBS technique, a charged particle with mass m is accelerated to an initial energy E_0 and it collides elastically with immobile atoms in the sample. This incident particle is then backscattered at the angle $\pi - \theta_{RBS}$ and the energy of the backscattered particle is reduced to E_1. The ratio of the initial energy of the incident particle to the energy of the backscattered particle is called a kinematic factor k_{RBS}, which is equal to:

$$k_{RBS} = \frac{E_1}{E_0} = \left[\frac{\sqrt{M_1^2 - m^2 \sin^2 \theta_{RBS}} + m \cos \theta_{RBS}}{M_1 + m} \right]^2 \tag{3.1}$$

Here M_1 is the mass of the targeted particle, and θ_{RBS} is the scattering angle in the laboratory frame of reference.

The probability of the backscattering event is given by the Rutherford law and it is described by a differential cross-section $d\sigma/d\Omega$ of the backscattering event. This differential cross-section, depends on the atomic numbers of the incident Z_0 and targeted Z_1 particles, the energy of the incident particle and the scattering angle θ_{RBS}. The Rutherford law is used for quantification of the results, by comparing the detected number of backscattered ions for investigated sample, with the number of backscattered ions for a template with known concentration of searched elements.

The RBS method is selective to the mass of the targeted particles. The resolution of this measurement can be improved by increasing the energy of the incident ions, choosing heavier projectiles or by detecting the backscattered particles at higher angles.

The RBS is suitable for detection of elements with atomic numbers $Z > 1$, which means that it is not suitable for detection of H.

Principles of NRA

Nuclear Reaction Analysis (NRA) is a quantitative and non-destructive analytical method, which is used to determine the quantity of light elements, such as C, O or N, in a sample [48]. The test setup is similar to that of RBS technique presented in Figure 3.4.4.1 (a). The difference lies in the type of incident particles (*e.g.* protons, deuterium), which are chosen as a function of the elements being detected. In this technique the incident particle induces a nuclear reaction with the element being struck, which results in emitting a particle with energy characteristic to a specific nuclear reaction. For example, to detect C atoms a reaction $^{12}C(d, p)^{13}C$ is used,

which means that an incident deuteron reacts with a stationary ^{12}C atom to form a ^{13}C atom and emit a proton.

Principles of ERD
Elastic Recoil Detection Analysis (ERDA), also known as Forward Recoil Scattering is a quantitative and non-destructive method, similar to RBS spectroscopy, which is suitable for determining H content in a sample [48]. In this technique (Figure 3.4.4.1 (b)) a beam of high-energy heavy particles is directed on the surface of the sample, similarly to RBS technique, but usually at lower angle. The incident particle have energy, which is high enough to elastically recoil, in forward angles, the nuclei from the sample, which are then detected.

Test setup
In our case, RBS method is used to determine the quantity of Si. As a primary beam (of incident ions), a He beam of energy 3.35MeV at normal incidence has been used. The detection angle is θ_{RBS} =135° from the incident direction, with a beam of 2 μm diameter at a current of 600 pA.

The NRA technique with an external 1.2 MeV deuteron beam has been used to determine the quantity of N and O. The reaction for nitrogen is ^{14}N(d, α)^{12}N, that is a deuteron reacted with a ^{14}N atom to form an ^{12}N atom and emit an α particle (He^{2+}). The reaction for oxygen is ^{16}O(d, p)^{17}O, where a deuteron reacts with a ^{16}O atom to form a ^{17}O atom and emits a proton. The spot diameter is 10 μm for a current of 1.5 to 3nA.

The ERDA method is used to quantify H contents. The incident beam is a 2.2MeV He beam, with a spot diameter of 2μm for a current of 600pA. The angle of inclination of the target is 15°, with 30° detection in the forward direction with respect to the incident direction.

Test samples
The test samples for RBS, NRA and ERDA analyses are AIM structures, as presented in Figure 3.2 (c). No special preparation of the samples is required prior to the measurements.

3.4.4.2 Results

The results of RBS measurements, which are used to determine the quantity of Si are presented in Figure 3.10, for SiN_x and in Figure 3.11, for SiO_2. In these figures, the number of counted ions is plotted as a function of the energy of backscattered ions. As the energy of backscattered particles decreases with decreasing atomic mass of detected elements, the energy peaks of elements such O, N and Si are found at low to medium energies, while heavy Pt has a large peak for high energy. Moreover, in our case the samples are multi-layered, thus the RBS peaks for the light elements overlap. Because it is difficult to quantify the amount of oxygen and nitrogen in our case, their amount is determined from NRA measurements and the results are presented in following paragraphs.

Figure 3.10 presents the RBS spectra for the high-frequency (capa.A) and the mixed-frequency (capa.C) SiN_x dielectrics. The quantified atomic concentrations of Si, obtained from RBS measurements are presented in Table 3.3.

The results of NRA measurements, which are used to determine the amount of N in O are presented in Figure 3.12 for SiN_x and Figure 3.13 for SiO_2. Contrary to the RBS measurements, in these figures the peaks for N and O are clearly visible as they do not overlap, with other

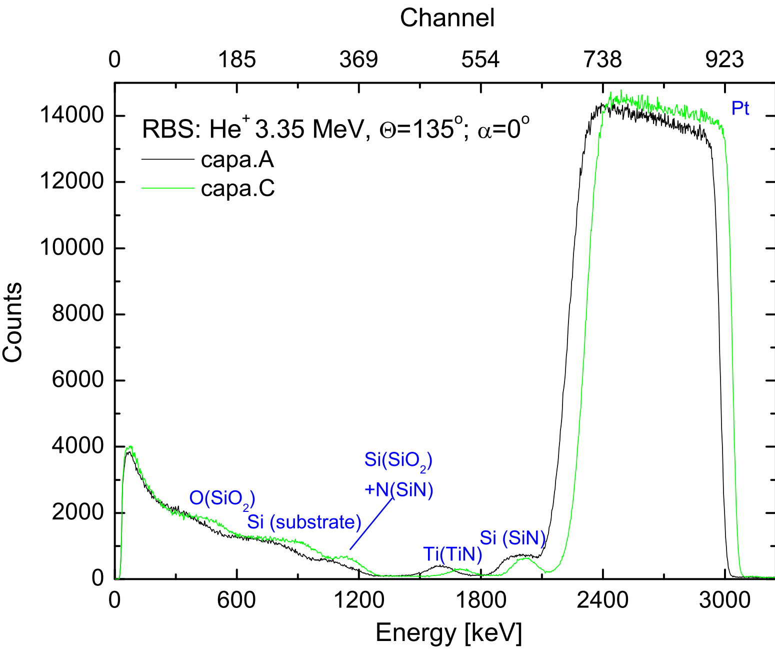


Figure 3.10: RBS results for SiN_x

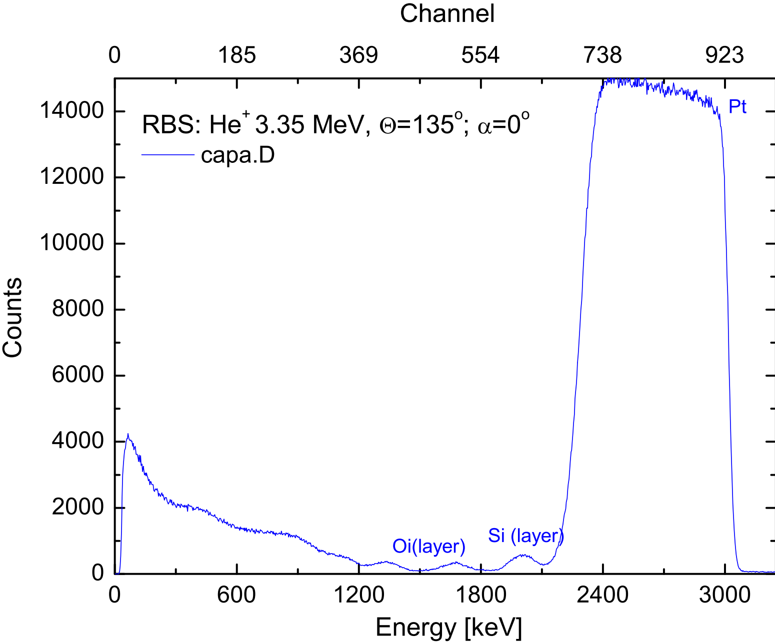


Figure 3.11: RBS results for SiO_2

Table 3.3: Composition of studied PECVD SiN_x and SiO_2

		Concentrations in $1{\cdot}10^{15}$ at/cm^2					
Sample	Dielectric	Si (RBS) (±60)	N (NRA) (±40)	O (NRA) (±30)	H (ERDA) (±25)	N/Si (±0.05)	O/Si (±0.05)
capa.A	SiN_x HF	1262	929		650	0.74	
capa.C	SiN_x MF	633	717		390	1.16	
capa.D	SiO_2 MF	820		668	53		0.81
		Concentrations in %					
Sample		Si (RBS) (±5)	N (NRA) (±2.5)	O (NRA) (±3)	H (ERDA) (±2)		
capa.A	SiN_x HF	44.4	32.7		22.9		
capa.C	SiN_x MF	36.4	41.2		22.4		
capa.D	SiO_2 MF	53.2		43.3	3.4		

elements. The atomic concentrations of N and O, obtained from the Figure 3.10 and 3.11 are summarized in Table 3.3 together with the atomic concentrations of H, obtained from ERDA.

The capa.A SiN_x deposited at high frequency is non-stoichiometric Si-rich, with the N/Si ratio $x_{N/Si} = 0.74$. The capa.C SiN_x deposited at mixed frequency is more stoichiometric, with a N/Si ratio $x_{N/Si} = 1.16$. What is common for both types of SiN_x, it is their very high concentration of H, which is approximately 23 at.%.

The capa.D SiO_2 deposited at mixed-frequency turns out to be non-stoichiometric, with a O/Si ratio $x_{0/Si} = 0.81$. The level of hydrogen is 3.4 at.%, which is relatively low, when compared to the analyzed SiN_x.

3.4.5 Qualitative analysis of contaminations

In this section the depth-profiles of traces of contaminations are measured for all 4 dielectrics, by ToF-SIMS technique.

3.4.5.1 Experimental procedure

Test method

Principles of Time of Flight Secondary Ion Mass Spectroscopy - ToF SIMS
Time of Flight - Secondary Ion Mass Spectroscopy (ToF-SIMS) is an experimental technique used to analyze the composition of solid materials [48, 53]. A schematic drawing of a ToF-SIMS spectrometer is presented in Figure 3.14.

In the ToF-SIMS technique high-energy incident ions are used to extract ions from the surface of a sample. These scattered ions are then analyzed by a Time-of-Flight (ToF) mass spectrometer, which uses the fact that ions with the same energy but different masses travel with different velocities. The lighter ions arrive at the detector before the heavier ones. By measuring their time of flight, it is possible to determine the mass of the ions.

ToF-SIMS is a destructive technique because the particles are removed from the surface. This is used for depth profiling, where two ion beams are used. The first one is sputtering a

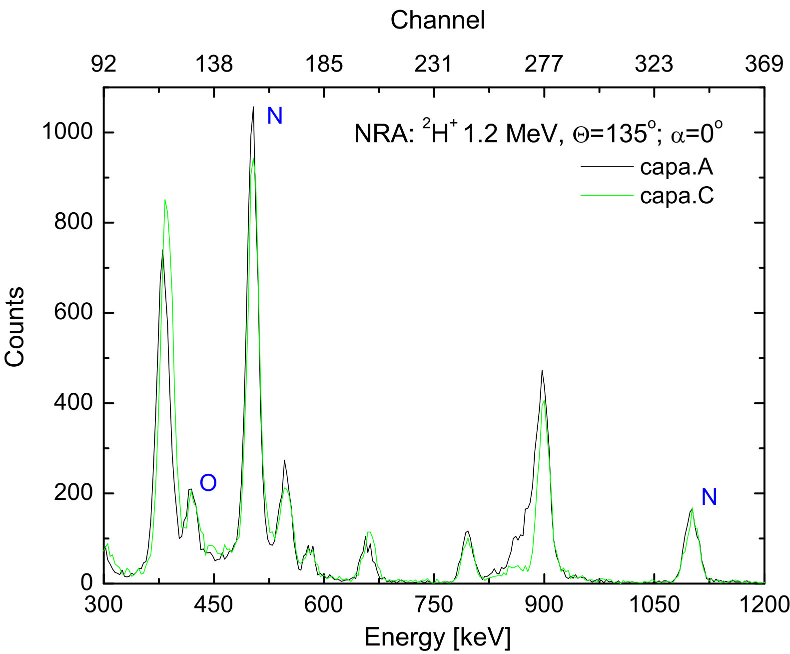


Figure 3.12: NRA results for SiN_x

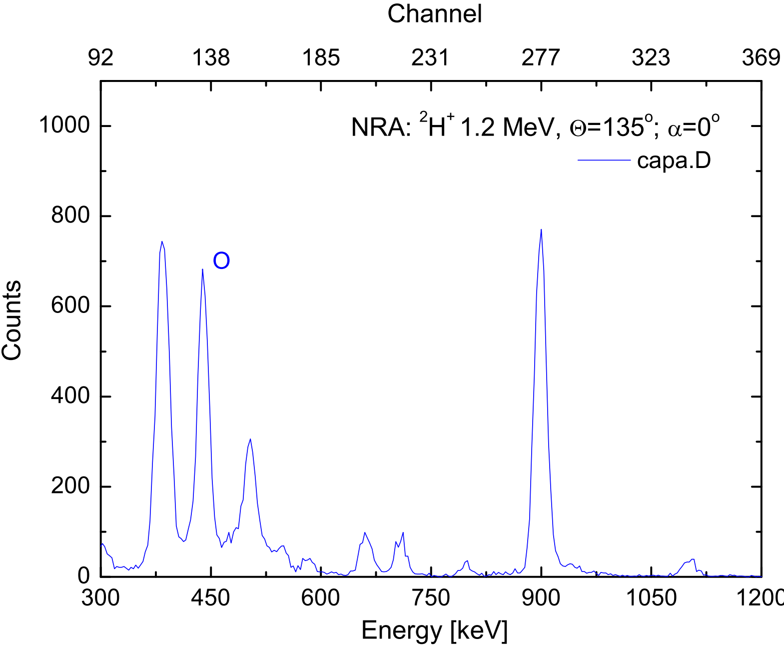


Figure 3.13: NRA results for SiO_2

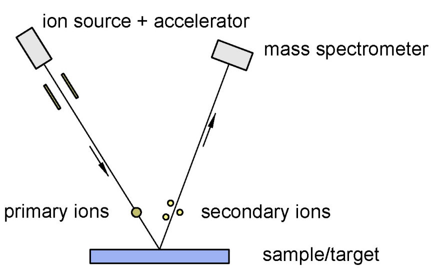


Figure 3.14: Schematic drawing of a ToF-SIMS spectrometer

crater, while the second is progressively analyzing the crater bottom.

This technique is one of the most sensitive ones, as it is possible to detect atomic concentrations as low as 10^8-10^9 at./cm^2. It is most suitable for qualitative analyses. It is difficult to obtain quantitative atomic concentrations from the ToF-SIMS profiles, because the secondary ion yield depends not only on the element, but also on the matrix of the analyzed material. The quantification can be done, providing that there is a template with the same matrix type, as in the analyzed sample and that the atomic concentrations are known.

ToF-SIMS can detect positive or negative ions. The positive ions are formed from I-III group elements and transition metals, during O_2^+ ion bombardment. The negative ions are formed from IV-VII group elements during Cs^+ bombardment.

Test setup

The contaminations are analyzed using ToF-SIMS depth profiling with an IONTOF V spectrometer. The test setup is summarized in Table 3.4.

Test samples

The test samples for ToF-SIMS are AIM structures, as presented in Figure 3.2 (c). No special preparation of the samples is required prior to the measurements.

Table 3.4: ToF-SIMS setup

	Cs sputtering	O_2 sputtering
Analysis gun	25 keV 13nA DC Bi+ raster size 80μm	5 keV 13nA DC Bi+ raster size 80μm
Sputter gun	2 keV 140 nA Cs+ raster size 250μm	1 keV O_2+ raster size 300μm
Spectrometer	detection of **negative ions**	detection of **positive ions**
Cycle time	80 μs	80 μs
Pressure	$7 \cdot 10^{-9}$ mbar	$2 \cdot 10^{-8}$ mbar

3.4.5.2 Results

ToF-SIMS depth-profiles in PECVD SiN_x

ToF-SIMS depth-profiles for HF and MF SiN_x are presented in Figure 3.15 and for MF SiO_2 in Figure 3.16. Presented results are qualitative, as there is no template available to calibrate the vertical axis. Nevertheless, it is possible to compare the relative levels of the ion profiles between the HF and MF SiN_x as their matrix should be similar.

The transitions regions between air-dielectric and dielectric-bottom electrode are stretched, because the surface of the dielectric is non-planar, and the ToF-SIMS signal is averaged from a spot of 80 μm.

The ToF-SIMS depth-profiles on SiN_x confirm, that SiN_x samples contain a significant amount of H, which is uniformly distributed throughout the entire depth of the dielectric. The levels of the H profiles are the same for 3 samples and from the ERDA measurements, we know that the absolute atomic concentrations of H are virtually the same.

All SiN_x samples contain a considerable amount of O, which is uniformly distributed in the dielectric. The presence of oxygen is also confirmed by NRA spectra, where it is clearly visible as a peak presented in Figure 3.12. As the oxygen has not been assumed to be present in significant amount in the SiN_x and it has not been quantified.

High-concentration of F is detected, in all SiN_x, with a slightly higher amount in the capa.C dielectric. The F-profiles are more intensive at the air-dielectric interface. The amount of F decrease with increasing depth.

A non-uniformly distributed Pt is found in all SiN_x, with a significantly higher amount found in the capa.C. Similarly to F-profiles the Pt-profiles are more intense at the air-dielectric interface.

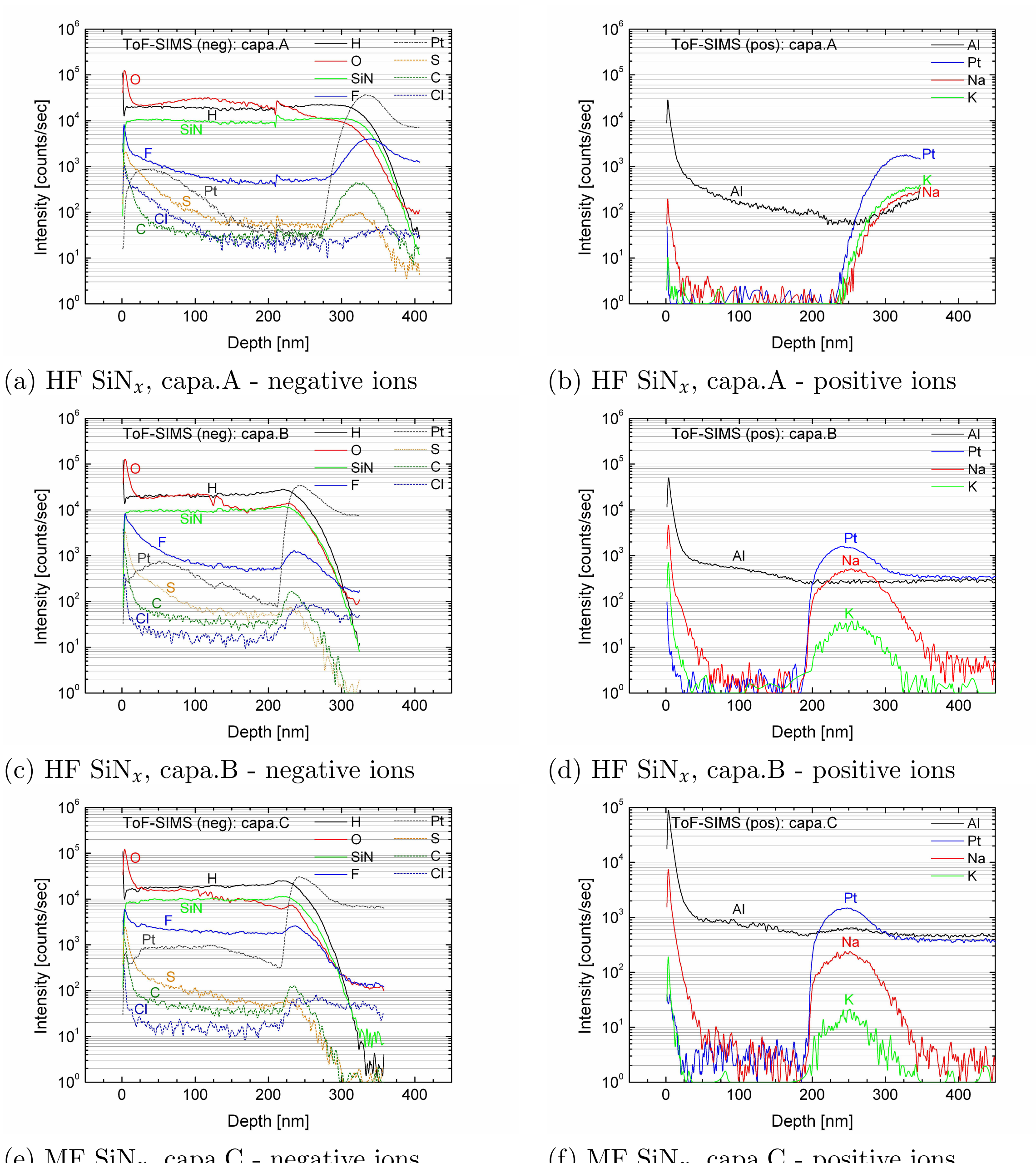
Positive-ion detection shows that there is also a considerable amount of Al distributed in all of the investigated SiN_x the dielectrics. The most probable source of this Al contamination is the deposition process of the top electrode (Al or AlSi). It is worth noticing, that even the AIM test structures (without the Al or AlSi electrode) have the Al atoms incorporated in the dielectric.

Traces of C revealed in all SiN_x are present rather at the interfaces air-dielectric and dielectric-bottom electrode. The concentration of C is the highest for capa.A dielectric (at the dielectric-bottom electrode interface), and it is much lower for the capa.B and capa.C samples.

Traces of S and Cl are found in all SiN_x and the distribution of these elements seems to be similar.

K and Na positive ions are found at high concentration levels only at the interfaces and not in the bulk of the dielectrics, which explains why SiN_x is used as a diffusion barrier. The highest concentrations of these elements are found at the dielectric-bottom electrode interface. The capa.A has a much higher concentration of K than the remaining samples. The concentration of Na is similar for all investigated samples.

It can be concluded from the ToF-SIMS observation of depth-profiles of HF and MF SiN_x deposited on 3 wafers, that there is not significant difference between these materials in terms of type of contaminations and their spatial distribution across the dielectric. Moreover, the storing time has no influence on the type and distribution of the contamination, as there is virtually no difference between the capa.A HF SiN_x and the capa.B HF SiN_x, where the later has been stored for a shorter period of time (several months).



(a) HF SiN_x, capa.A - negative ions

(b) HF SiN_x, capa.A - positive ions

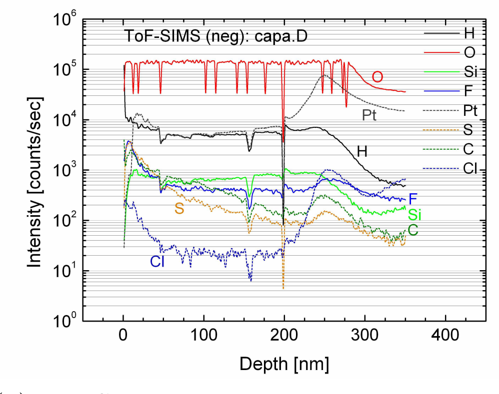
(c) HF SiN_x, capa.B - negative ions

(d) HF SiN_x, capa.B - positive ions

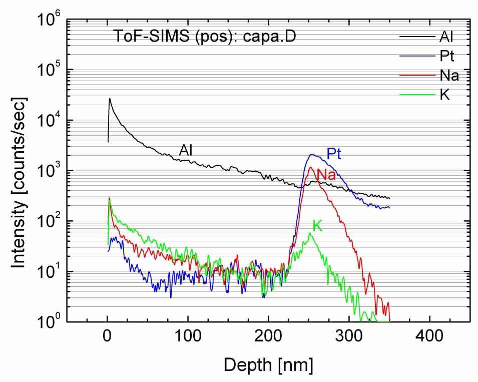
(e) MF SiN_x, capa.C - negative ions

(f) MF SiN_x, capa.C - positive ions

Figure 3.15: ToF-SIMS depth-profiles in SiN_x, for negative and positive ion detection



(a) MF SiN_x, capa.D - negative ions



(b) MF SiN_x, capa.D - positive ions

Figure 3.16: ToF-SIMS depth-profiles in SiN_x, for negative and positive ion detection

ToF-SIMS depth-profiles in PECVD SiO_2

ToF-SIMS depth-profiles for SiO_2 are presented in Figure 3.16.

In general, the same elements have been detected in the SiO_2 and in SiN_x, which signifies that the contaminations are not intrinsic but are due to the fabrication process flow, which is the same for the samples with SiN_x and SiO_x except the phase of deposition of the dielectric.

Because the layers of SiN_x and SiO_2 have different matrix, it is not possible to make direct comparisons of the depth-profiles between them.

Similarly to SiN_x, SiO_2 contains the traces of Pt and Al distributed in the bulk of dielectric.

High concentration of F is detected in the bulk of dielectric.

Compared to SiN_x, S and C elements, seem to have higher concentration as their profiles are at the same level as F.

In contrast to SiN_x, the Cl concentration is lower than the concentration of S and C elements, but it increases rapidly at the interfaces.

K and Na positive are present also in the bulk of dielectric, unlike in the SiN_x. The highest concentrations of these elements are found at the dielectric-bottom electrode interface.

Some peaks can be observed on the depth-profiles in Figure 3.16. These peaks are due to local breakdowns of the dielectric. This breakdown could be observed on the display during the measurement, as a flash on the dielectric surface. No such events are observed for SiN_x.

3.4.6 Discussion of structural analyses

The analyses confirm the amorphous phase of PECVD SiN_x and SiO_2. They reveal that the PECVD deposition technique causes the creation of Pt crystalline spots (several nm) embedded in the dielectric in the immediate vicinity of the Pt electrode.

It turns out that the capa.A high frequency SiN_x is Si-rich with its N/Si ratio $x_{N/Si} = 0.74$, while the capa.C mixed frequency SiN_x is almost stoichiometric with its N/Si ratio $x_{N/Si} = 1.16$. The PECVD SiO_2 turns out to be not-stoichiometric, with a O/Si ratio of 0.81.

The amount of H is almost the same for all SiN_x as it is approximately 23 at.%. The concentration of H is much lower in SiO_2, where it is only 3.4 at.%.

The ToF-SIMS depth profiles reveals that apart form the H, all SiN_x samples contain significant amounts of O.

All 3 types of dielectrics on 4 wafers, have traces of Al, Pt and F distributed throughout the entire depth of the dielectric, which are most likely introduced during the fabrication process, which is the same for all samples. The traces of K and Na are found in considerable concentrations at the interfaces of SiN_x. In case of SiO_2 K and Na ions are also detected in the bulk of the dielectric.

The Ga found by EDS spectroscopy, at the AlSi-SiN_x interface of capa.C sample, is not detected by any other technique, which strongly suggests the hypothesis that the Ga traces, are due to the preparation of the sample by FIB technique, where a gallium beam is used to sputter the material.

3.5 Characterization of dielectric properties

3.5.1 Objective

the presence of trapped charge in the dielectric may be either necessary for correct operation of the device or undesirable, depending on a particular application [38]. For instance the MNOS devices (non-volatile RAM) require charge, which is captured and held so that the threshold voltage can change and it is possible to distinguish between the binary states. On the other hand there are the MEMS switches, where the trapped charge may contribute to a significant decrease of the switch lifetime. However, there is one requirement for the charge in the dielectric, which is common for these two applications. It is the predictability of the behavior of the trapped charge in a specific dielectric, under a given set of operating conditions, which requires fundamental knowledge of the types of charges present in the dielectric and their behavior.

In the last 40 years, there has been a lot of effort put into the study of the electronic properties of thermal and LPCVD dielectrics, as those used, for example, in CMOS circuits.

Contrary to these group, the PECVD dielectric has been used, for a long period of time, as diffusion barrier or passivation layers. Hence, there was no need to study the electronic properties of the materials. Then, when more sophisticated applications for these dielectrics were found, it turned out that, these materials had not been studied enough and that we lacked fundamental knowledge of their electronic properties.

This part of the chapter is aimed at studying the electronic properties of PECVD dielectrics, which are used in RF MEMS switches. It starts with a description of the types of charge in dielectrics, the standard test structures and methods used in characterization of dielectrics. It is the followed by a short description of the mechanism of conduction and trapping in dielectrics. At the ends the conduction and trapping mechanisms are determined for 2 types of PECVD SiN_x and 1 type PECVD SiO_2 dielectric layer, which are used in RF MEMS switches.

3.5.2 Background information

3.5.2.1 Types and location of charge

This section presents types and locations of charges which may be present in insulators [38, 54].

Interface charge Q_{it}

The interface trapped charges are negative or positive charges, which are trapped in the struc-

tural defects at the transition region between a semiconductor and insulator [38, 54]. In case of metal-insulator-semiconductor (MIS) structures, these charges may alter the performance of such a device, by modulating, for instance, its capacitance. The interface trapped charge has a minor influence on the operating performance of the MIM capacitors and MEMS switches, because both electrodes are metallic.

Bulk charge Q_{ot}
The charge Q_{ot} is the charge, which is located in the bulk of the insulator. It can be further divided into three categories [38, 54]:

- *Fixed charge* Q_f

  This charge is located in the bulk of the insulator in the immediate vicinity of electrode. It results from the fabrication process, rather than trapping of parasitic charge during operation. It cannot move and be exchanged.

- *Mobile (ionic) charge* Q_m

  It results from the presence of ions in the insulator, the quantity of which may depend on numerous factors (*e.g.* fabrication conditions, or storing conditions). Typically, the mobile charge is a positive charge caused by alkaline ions such as Na^+, K^+ or hydrogen H^+. When an external electric field is applied to the insulator, the ions move within the volume of the insulator, distorting the initial electric field, which may alter the functioning of a device.

- *Trapped charge* Q_0

  This is either a negative or positive charge, which has been injected and then trapped in the bulk of the dielectric. It is characterized by the capture cross-section and it will be investigated later in this chapter.

Practically, it may be difficult to distinguish between the types of the bulk charge trapped in the dielectric.

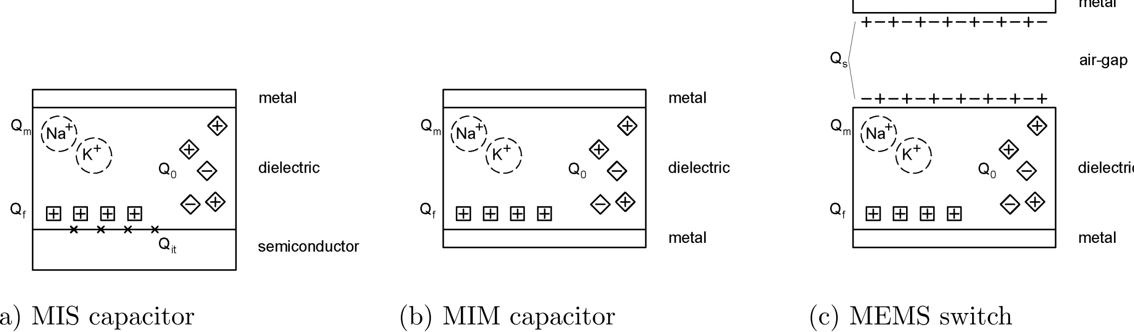
Surface charge Q_s
The surface charge is a negative or positive charge located at the surface of an insulator, which is exposed to ambient environment (like in a MEMS switch).

3.5.2.2 Test structures

This section presents and discusses the types of charges and the functioning of Metal-Insulator-Semiconductor (MIS) capacitors, Metal-Insulator-Metal (MIM) capacitors and MEMS switches.

Metal-Insulator-Semiconductor (MIS) capacitor
The types of charge, which may be present in a MIS capacitor are presented in Figure 3.17 (a).

In a MIS capacitor the charge at the interface Q_{it} may alter the behavior of the whole device. For instance, when some charge is trapped at the semiconductor-dielectric interface, then the



(a) MIS capacitor (b) MIM capacitor (c) MEMS switch

Figure 3.17: Types of charge in Metal-Insulator-Semiconductor (MIS) capacitor, Metal-Insulator-Metal (MIM) capacitor and MEMS switch (reprinted from [38])

flat bands voltage[13] (V_{FB}) shifts towards positive or negative voltage depending on the charge sign [38]. By measuring the offset of V_{FB} it is possible to calculate accurately the amount of the trapped charge. Similarly, if a bulk charge Q_{ot} is trapped, it also alters the C-V characteristic, by modifying the capacitance of the dielectric.

Typical C-V characteristic for high and low frequency of a MIS capacitor is presented in Figure 3.18(a) [45, 55], where the normalized capacitance C_{MIS}/C_{bulk} of a MIS capacitor is plotted as a function of the gate voltage V_G. In this figure, it is possible to distinguish four segments: accumulation, flat bands, depletion and inversion, which are presented in the corresponding band diagrams, for a p-type Si[14].

The total capacitance of the MIS structure C_{MIS} is a sum of the capacitance of the bulk of the dielectric C_{bulk} and the capacitance of the insulator-semiconductor interface $C_{interface}$, in series:

$$\frac{1}{C_{MIS}} = \frac{1}{C_{bulk}} + \frac{1}{C_{interface}} \tag{3.2}$$

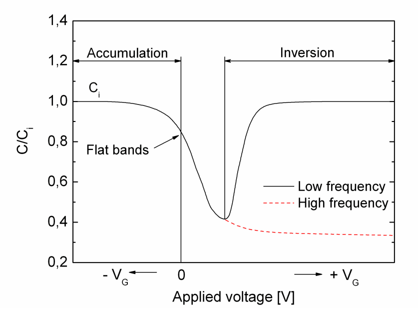
Accumulation

When a negative gate voltage is applied $V_G < V_{FB}$ to the MIS structure with p-type Si, the valence band E_V in Si bends upward, so it is closer to the Fermi level of the semiconductor E_{F_S} (Figure 3.18 (b)). As a result, the majority charge carriers (holes), accumulate at the insulator-semiconductor interface. The density of the majority charge carriers depends exponentially on the energy difference $E_{F_S} - E_V$ [45].

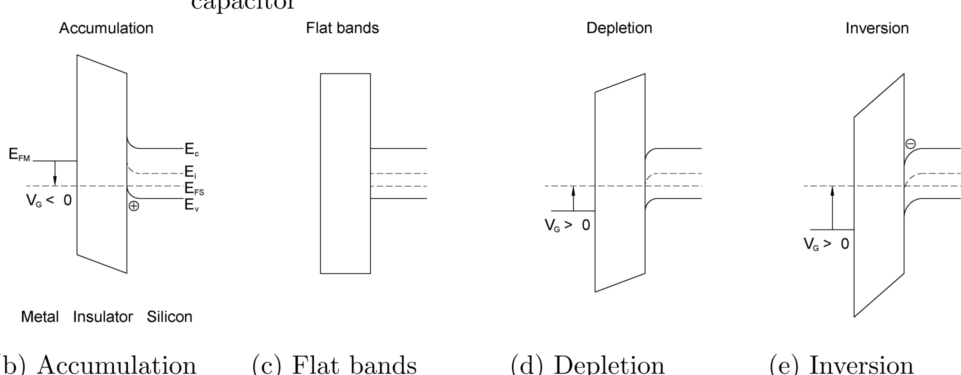
Because of this accumulation of the charge carriers, the interface capacitance increases. When $C_{interface}$ is much higher than C_{bulk}, the expression $1/C_{interface}$ tends to zero, thus the total capacitance C_{MIS} is approaching the value of the bulk capacitance $C_{MIS} \approx C_{bulk}$. The normalized capacitance C_{MIS}/C_{bulk}, is then approaching 1:

[13] The flat bands voltage V_{FB} is defined as the voltage for which there is no charge in the semiconductor and in the metal gate.

[14] p-type Si has an excess of positive charge carriers due to doping



(a) Low- and high-frequency CV curve on a MIS-capacitor



(b) Accumulation (c) Flat bands (d) Depletion (e) Inversion

Figure 3.18: Charge behavior in a MIS capacitor as a function of the applied bias (reprinted from [55])

$$C_{interface} \gg C_{bulk} \Rightarrow C_{MIS} \approx C_{bulk} \tag{3.3}$$

Flat bands

The work functions of a metal ϕ_m and semiconductor ϕ_s in a MIS structure may not be equal. The difference $\phi_s - \phi_m$ corresponds to a difference of potential V_{FB}. The flat bands voltage is the voltage that has to applied to the metal gate (top electrode) of a MIS structure, so that the Fermi levels in metal E_{F_M} and semiconductor E_{F_S} align, as presented in Figure 3.18 (c), and consequently there is no charge present in the semiconductor and the metal gate.

Depletion

When a small positive gate voltage is applied $V_G > V_{FB}$, the valence band E_V bends downward (Figure 3.18 (d)). The distance $E_{F_S} - E_V$ increases at the interface,which is why the density of the majority carriers at this interface is decreasing.

Because of this depletion of the charge carriers, the interface capacitance decreases. When $C_{interface}$ is much lower than C_{bulk}, the expression $1/C_{interface}$ increases and it becomes dominating in equation 3.2, thus the normalized capacitance C_{MIS}/C_{bulk}, is decreasing:

$$C_{interface} \searrow \Rightarrow C_{MIS} \searrow \tag{3.4}$$

Inversion
When a large positive gate voltage is applied $V_G \gg V_{FB}$, the bands bend further downward (Figure 3.18 (e)). The intrinsic Fermi level E_i crosses the Fermi level in semiconductor E_{F_S}. Inversion is obtained when the carrier concentration at the surface is of inverted type and is equal to that of the bulk.

In the inversion layer the number of charge carriers (electrons) at the insulator-semiconductor interface increases with increasing gate voltage and the interface capacitance is then increasing. When $C_{interface}$ is much higher than C_{bulk}, the expression $1/C_{interface}$ tends to zero, and it becomes negligible in equation 3.2. The total capacitance C_{MIS} is then approaching the value of the bulk capacitance $C_{MIS} \approx C_{bulk}$. The normalized capacitance C_{MIS}/C_{bulk}, is then approaching to 1:

$$C_{interface} \ll C_{bulk} \;\Rightarrow\; C_{MIS} \approx C_{bulk} \tag{3.5}$$

Metal-Insulator-Metal (MIM) capacitor
A schematic drawing of a MIM capacitor, with the types of charges present, is shown Figure 3.17 (b). Unlike in the MIS capacitor, there is no interface charge present, as the insulator is deposited directly on a metallic electrode. As a consequence, the capacitance is independent of the gate voltage. It is then difficult to determine the amount of trapped charge in the bulk of the MIM structure, as it is not possible to measure the offset of the flat bands voltage.

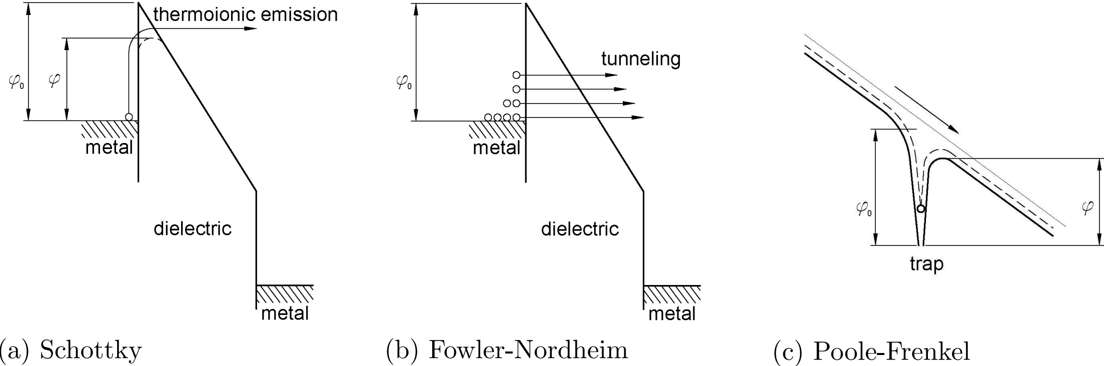
MEMS switch
A schematic view of an electrostatic MEMS switch is presented in Figure 3.17 (b). Typically the dielectric is deposited on a metallic electrode, which is why the MEMS switch is better approximated by a MIM capacitor rather than MIS. Consequently, there is no interface charge Q_{it}.

The main difference between the MEMS switch and the MIM capacitor, is that the top layer of the dielectric is separated from the top metallic electrode by an air gap. Unlike in the previous structures, in the MEMS switch it is the surface charge Q_s trapped at the air gap - insulator interface, which is the most significant for the operation of the device, as it alters the distribution of the electric field [38]. As a consequence, to ensure correct operation of a MEMS switch, one has to be able to measure and control the surface charge Q_s.

Below, is a short list of factors, that may have an influence on the surface charge Q_s in the MEMS switch and which are irrelevant for the previously discussed test structures [38]:

- During fabrication: deposition conditions and stripping of sacrificial layer on the dielectric,
- Post fabrication: thermal treatment, annealing,
- During operation: exposition of the dielectric to atmospheric conditions, contaminations.

Apart from the surface charge Q_s, the same types of the bulk charge as in the MIM-capacitor are present in a MEMS switch. These bulk charges have also an effect on the functioning of the MEMS switches, as they may alter the distribution of the electric field in the dielectric. The effect of the presence of an air gap on the distribution of the electric field will be presented in chapter 4.



(a) Schottky (b) Fowler-Nordheim (c) Poole-Frenkel

Figure 3.19: Transport of electrons in Schottky emission, tunneling (Fowler-Nordheim) process and Poole-Frenkel emission

3.5.3 Identification of conduction processes

3.5.3.1 Theoretical models of conduction processes in insulators

Real insulators demonstrate a non-zero conduction provided that the electric field in the dielectric E_d and/or the temperature T are high enough [45, 56]. The conduction is defined as a flux of charge carriers, that is electrons, holes or ions, in the presence of the electric field. In a Metal-Insulator-Metal (MIM) capacitor, the conduction consists of three stages. In the first stage, the charge carriers are emitted from a metal electrode into the insulator. In the second stage, they are transported through the bulk of the dielectric. In the last stage, these carriers are emitted from the dielectric and collected by the second metal electrode. Consequently, the current through the insulator is limited either by the process of injection at the metal-insulator interface or by the process of transport of the charge carriers through the insulator. As a result, the conduction processes are divided into electrode-controlled or bulk-controlled.

The following paragraphs provide a short description of the most common conduction processes [45, 56].

Schottky emission

The Schottky emission is presented schematically in Figure 3.19 (a). In this process, the emission of electrons from a metal electrode into the insulator is assisted by image-force lowering of the height of the potential barrier, in the presence of an electric field. The image force results from the fact that each of the electrons injected into the insulator induces a positive image charge on the metal electrode. The attraction force between the positive and negative charges, which is called the image-force induce lowering of the initial height of the potential barrier at the metal-insulator interface [45, 56–58].

In the absence of the electric field, the initial barrier height ϕ_0 can be obtained, as a difference between the energy of the Fermi level E_F of the metal and the energy of conduction band E_C of the dielectric:

$$\phi_0 = E_C - E_F \tag{3.6}$$

When the electric field E_d is applied, it induces lowering of the zero-field barrier height ϕ_0 and the lowered effective barrier height ϕ can be calculated as:

$$\phi = \phi_0 - \beta_S \sqrt{E_d} \tag{3.7}$$

Here, the electric field E_d is assumed to be uniform throughout the dielectric and is calculated as $E_d = V_{app}/t_d$, where V_{app} is the applied voltage and t_d is the thickness of the dielectric and β_S is the Schottky coefficient equal to:

$$\beta_S = \sqrt{\frac{e}{4\pi\epsilon_0\epsilon_r}} \tag{3.8}$$

Where e is the elementary charge, ϵ_0 is the vacuum permitivity and ϵ_r is the relative dielectric constant.

Taking all above into consideration, the density of the current J through the insulator as a function of the electric field E_d, in the Schottky emission, is given by the equation:

$$J = AT^2 \exp\left(\frac{e\phi}{k_B T}\right) \tag{3.9}$$

$$= AT^2 \exp\left[-\frac{e\left(\phi_0 - \beta_S\sqrt{E_d}\right)}{k_B T}\right] \tag{3.10}$$

Here A is the Richardson constant defined as $A = 4\pi m_e k_B^2/h^3 \approx 120$ A/cm^2, where m_e is the effective mass of an electron, T is the absolute temperature, k_B is the Boltzmann constant and h is the Planck constant.

Because it is common to measure the change of the current density of several decades, for high electric-fields, it is more convenient to use a logarithm of current density. After taking the logarithm of the equation 3.9, it takes the following form:

$$\ln J = \frac{\beta_S\sqrt{E_d}}{k_B T} - \frac{\phi_0}{k_B T} + \ln\left(AT^2\right) \tag{3.11}$$

$$\ln J = m_S\sqrt{E_d} + C_1 \tag{3.12}$$

In Schottky emission there is a linear relation between the logarithm of the measured current density and the square root of the average electric field $\sqrt{E_d}$. A straight line in the plot $= f\left(\sqrt{E_d}\right)$ may indicate Schottky emission, and the slope m_S can be used to calculate the experimental values of the Schottky coefficient β_S and dielectric constant ϵ_{r_S} from the transformed equation 3.8:

$$\epsilon_{r_S} = \frac{e}{4\pi\epsilon_0\beta_S^2} \tag{3.13}$$

The Schottky emission is temperature dependent according to the equation 3.9, with the main contribution varying as $\exp\left(-E_a/k_B T\right)$, where E_a is the field-dependent activation energy.

Tunneling process

The tunnel emission is presented schematically in Figure 3.19 (b). It is the most common conduction mode in insulators at high electric fields, of the order of several MV/cm [45, 56]. The tunneling conduction results from quantum mechanical tunneling of an electron wave-function through a potential barrier. It can be divided into direct tunneling and Fowler-Nordheim tunneling. In the first process, an electron tunnels through a total width of the barrier. In the second process, an electron tunnels through a partial width of the barrier, which corresponds to the situation shown in Figure 3.19 (b).

The tunneling theories leads to the following simplified equation of the current density J, as a function of the electric field E_d [56, 59]:

$$J = \frac{AT^2}{\phi}\left(\frac{eE_d}{\alpha k_B T}\right)^2 \exp\left(-\frac{2\alpha\sqrt{\phi^3}}{3eE_d}\right) \tag{3.14}$$

Here ϕ is the effective barrier height and $\alpha = 4\pi\sqrt{m_e}/h$.

By substituting A and α in equation 3.14 it becomes:

$$J = \frac{e^3}{8\pi h\phi}E_d^2 \exp\left(-\frac{4\sqrt{2m_e}\sqrt{\phi^2}}{3e\hbar E_d}\right) \tag{3.15}$$

For practical purposes of analyzing current-voltage measurements, equation 3.15 is further transformed into this form:

$$\ln\left(\frac{J}{E_d^2}\right) = \frac{1}{E_d}\left(-\frac{4\sqrt{2m_e}\sqrt{\phi^2}}{3e\hbar}\right) + \ln\left(\frac{e^3}{8\pi h\phi}\right) \tag{3.16}$$

From equation 3.16 it is apparent, that there is a linear relation between $\ln J/E_d^2$ and $1/E_d$, which can be taken as an indication of a tunneling process, when analyzing current-voltage measurements.

The tunneling is temperature dependent as the temperature can modify the number and the distribution of electrons arriving at the barrier, which has an influence on the transition probability.

Poole-Frenkel emission

The Poole-Frenkel emission is presented schematically in Figure 3.19 (c). This conduction process involves a mechanism, which is similar to the Schottky emission. In the Schottky emission the thermal excitation of an electron is used to overcome the barrier at the metal-insulator interface, while in the Poole-Frenkel process the thermal excitation of electrons is used to emit electrons from trapping centers into the conduction band [45, 56–58]. To empty a trap, the electron must overcome the barrier height ϕ, which is the depth of the trap potential well. This is done thanks to a thermal activation, with elementary activation of order $k_B T$ [45].

The current density as a function of electric field, for the Poole-Frenkel emission, is given by the (1-dimensional) model [45, 56]:

$$J = J_0 \exp\left(\frac{-eE_a}{k_B T}\right) \tag{3.17}$$

$$= J_0 \exp\left[-\frac{e\left(\phi_0 - \beta_{PF}\sqrt{E_d}\right)}{k_B T}\right] \tag{3.18}$$

Here J_0 is a current prefactor and β_{PF} is the Poole-Frenkel constant equal to:

$$\beta_{PF} = \sqrt{\frac{e}{\pi \epsilon_o \epsilon_r}} \tag{3.19}$$

Compared to the Schottky coefficient β_S (3.8), the Poole-Frenkel coefficient is twice as high (3.19), which means that the reduction of the barrier height is two times higher in the Poole-Frenkel emission.

Similarly to the Schottky emission, in the Poole-Frenkel process there is a linear relation between $\ln J$ and $\sqrt{E}$, by which the experimental Poole-Frenkel coefficient β_{PF} can be obtained from the slope m_{PF} of the plot of $\ln J$ as a function of $\sqrt{E}$:

$$\ln J = \frac{e\beta_{PF}}{k_B T}\sqrt{E} - \frac{\phi_0}{k_B T} + \ln J_0 \tag{3.20}$$

$$= m_{PF}\sqrt{E} + C_1 \tag{3.21}$$

By transforming equation 3.19, the experimental dielectric constant $\epsilon_{r_{PF}}$ is obtained from the β_{PF} value:

$$\epsilon_{r_{PF}} = \frac{e}{\pi \epsilon_0 \beta_{PF}^2} \tag{3.22}$$

The value of ϵ_r, obtained from the experimental value of β_{PF} is 4 times higher than the value obtained from β_S, provided that the slopes m_{PF} and m_S are the same. As a result, this experimental dielectric constant can be used to distinguish between the Poole-Frenkel and Schottky emission. The value of the dielectric constant $\epsilon_{r_{PF}}$ extracted from the Poole-Frenkel model is lower than the static dielectric constant of the investigated material, which is often the case for PECVD SiN_x [60–62]. This underestimation of the dielectric constant results, most probably, from using the 1-dimensional Poole-Frenkel model instead of 3-dimensional one, which gives more accurate values of $\epsilon_{r_{PF}}$ [63]. In case of the PECVD SiN_x it has been also demonstrated that the dielectric constant obtained from the experimental β_{PF} depends strongly on the number of defects in the investigated material [64], thus it may differ from the static value.

The Poole-Frenkel current is temperature dependent, as $\ln J$ is proportional to $\exp\left(-E_a/k_B T\right)$. When the value of $\ln J$ is plotted as a function of the reciprocal temperature $1/T$, for a specific electric field, it yields a straight line. The slope of the line for a specific electric field, gives the field-dependent activation energy E_a. When these values of E_a are plotted as a function of $\sqrt{E_d}$, the plot yields a straight line, which can be extrapolated to $E_d = 0$ to obtain the zero-field energy barrier, corresponding to the trap depth.

Space charge limited current
The space-charge-limited current (SCLS) is due to the injection of charge carriers into an insulator. Since there is no compensating charge present [45], these injected charges form a space-charge region [56].

In the SCLC model, the flux of charge carriers under an electric field follows a simple law:

$$v = \mu E_d \tag{3.23}$$

Here v is the velocity of the carriers and μ is their mobility.

The electric field in SCLC model has to include the contribution of the electric field induced in the insulator by the already injected and uncompensated charge carriers, which alters the conduction.

The most simplified model of a one-carrier space-charge-limited current density as a function of an electric field, is based on the following assumptions:

- the diffusion current is negligible,
- the mobility of charge carriers is constant,
- there are no intrinsic charge carriers nor trapped charge.

The simplified current-voltage relation for this space-charge-limited current is given by the equation [45, 56, 65–67]:

$$J = \frac{9}{8}\epsilon_r\epsilon_0\mu\frac{V_{app}^2}{t_d^3} \tag{3.24}$$

As one can see from equation 3.24, the current density in the trap-free case of a one-carrier space-charge-limited current is proportional to V_{app}^2.

In case there are trapping centers of one specific energy level present in the insulator, the left part of the equation 3.24 is multiplied by θ_{SCL}, which is the ratio of the total injected charge N_{inj} to the trapped charge n_t ($\theta_{SCL} = N_{inj}/n_t$). When this model is further extended for charge trapped at different energy levels, the current-voltage formula has the following form [56]:

$$J = \frac{9}{8}\epsilon_d\epsilon_0\theta_{SCL}\mu\frac{V_{app}^{n+1}}{d^{2n+1}} \tag{3.25}$$

Here $0 < n < 3$ depending on the distribution of trap depths.

Ionic conduction
The charge carriers in the above mentioned mechanisms are either electrons or holes, which are transported through an insulator in a presence of an electric field. Apart from the electrons and holes, insulators may contain ions, which can be transported between defect sites if an electric field is applied [45, 56, 59]. Contrarily to the transport of electrons and holes, the ionic conduction involves transport of matter.

The ionic conduction depends on the concentration of ions, which is dependent of:

- the type of the dielectric,
- the conditions of the deposition process,

- the degradation of the material - aging, contaminations.

The equation of current density, due to ionic conduction, as a function of an electric field is given by the equation [56]:

$$J = J_0 \exp\left(-\frac{\phi - el_i E_d}{k_B T}\right) \tag{3.26}$$

Here, ϕ is the effective barrier height between the trap sites and l_i is the mean distance between the trap sites. The ionic current given by this equation is valid for higher electric fields (E>0.5MV/cm).

It is important to mention that the ions cannot be extracted from or injected in the insulator, thus the ionic conduction is a transient process. The ionic current will decrease as a function of time and in a steady-state it is zero. As a result the equation 3.26 is valid for the initial period of the ionic current flow only.

The displaced ions create an internal electric field. Once the external electric field is removed, this internal electric field causes some of the ions to return to their initial positions.

3.5.3.2 Experimental procedure

Test setup

Introduction

The standard technique, which is used to identify the conduction mechanisms, consists in measuring the leakage current across a dielectric as a function of the electric field. Depending on the type of the conduction process, the I-V curve is different. To distinguish between the mechanisms it is often sufficient to measure the I-V characteristics for positive and negative bias, and as a function of temperature.

Table 3.5: Summary of conduction mechanism

Process	Current-voltage expression	Current-voltage dependence
Schottky	$J = AT^2 \exp\left[-\frac{e\left(\phi_0 - \beta_S\sqrt{E_d}\right)}{k_B T}\right]$	$\ln J = f\left(\sqrt{E_d}\right)$
Tunneling	$J = \frac{e^3}{8\pi h\phi} E_d^2 \exp\left(-\frac{4\sqrt{2m_e}\sqrt{\phi^2}}{3e\hbar E_d}\right)$	$\ln\left(\frac{J}{E_d^2}\right) = f\left(\frac{1}{E_d}\right)$
Poole-Frenkel	$J = J_0 \exp\left[-\frac{e\left(\phi_0 - \beta_{PF}\sqrt{E_d}\right)}{k_B T}\right]$	$\ln J = f\left(\sqrt{E_d}\right)$
SCLC	$J = \frac{9}{8}\epsilon_r\epsilon_0\mu\frac{V_{app}^2}{t_d^3}$	$\ln J = f\left(V^2\right)$
Ionic	$J = J_0 \exp\left(-\frac{\phi - el_i E_d}{k_B T}\right)$	$\ln J = f\left(E_d\right)$

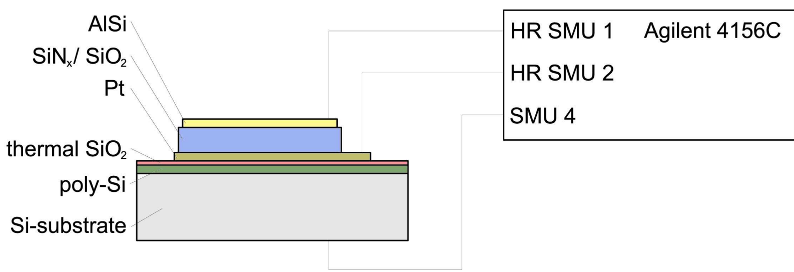


Figure 3.20: Schematic of test setup for measuring I-V curves and constant current injections

Table 3.5 summarizes the expressions for current density as a function of the electric field and it presents the current-voltage dependences, which are practically used to identify the conduction mechanism.

Test setup
Prior to other measurements the thickness of the dielectric layer t_d is obtained from the measurements of capacitance for several MIM-capacitor of different sizes. To measure the capacitance a HP4284 LCR meter is used.

The conduction mechanism are identified by measuring the I-V curves. The measurements are carried out using an Agilent 4156C Precision Semiconductor Parameter Analyzer. The samples are placed in a Cascade Microtech SUMMIT probe station in dry nitrogen atmosphere (RH $<$ 2 %). The connections between the test equipment and the device under test are realized with Kelvin triaxial cables. This setup allows measuring the currents as low as several fA, which is equivalent to a current density of several $1{\cdot}10^{-11}$ A/cm^2, for the samples that are used. A configuration of the test setup is presented in Figure 3.20.

Typically, a triangular voltage ramp (0-100 V at 40 mV/sec with 0.4 V step) is applied to the top electrode and the leakage current is measured at the bottom electrode. The average time interval between the 0.4 V steps is comprised between 8 (I $>$ 1 pA) to 12 sec (I $<$ 1 pA) depending on the measured current. The potential of the bottom electrode and the chuck is set to 0 V, to avoid leakage. Each I-V sweep is repeated twice on the same device to determine whether a steady-state conduction is reached. The I-V sweeps are also measured for positive and negative bias and as a function of the temperature. The temperature is ranging from 25°C to 145°C, with 20°C steps. It is limited to 145°C to avoid damaging of MEMS switches, located at the same wafer as the tested samples.

Test samples
The conduction mechanisms are identified for all 4 wafers with SiN_x and SiO_2 insulators. The test samples are MIM-capacitors, without any modifications.

For each of the measurements (except consecutive I-V curves) a new test sample is used.

3.5.3.3 Results

Calculation of thickness of the dielectric
The thickness of the dielectric is obtained from the measurements of the capacitance, where it

Table 3.6: Static dielectric constant ϵ_r

Wafer	A_{el} [µm^2]	C_0 [pF]		ϵ_r	t_d [nm]	
		Av.	S.D.		Av.	S.D.
capa.A (SiN_x HF)	$1{\cdot}10^4$	1.84	< 0.05	7.5	355	5
	$4{\cdot}10^4$	7.43	0.13			
	$9{\cdot}10^4$	16.99	0.17			
capa.B (SiN_x HF)	$1{\cdot}10^4$	2.55	< 0.05	7.5	255	5
	$4{\cdot}10^4$	10.43	0.21			
capa.C (SiN_x MF)	$1{\cdot}10^4$	2.56	< 0.05	7.5	250	5
	$4{\cdot}10^4$	10.71	0.10			
capa.D (SiO_2 MF)	$1{\cdot}10^4$	1.32	< 0.05	3.9	260	5
	$4{\cdot}10^4$	5.35	0.17			

is considered that the dielectric constant for the SiN_x is $\epsilon_r = 7.5$ and for SiO_2 it is $\epsilon_r = 3.9$ [45]. The results of the calculations of the thickness of the dielectric t_d are presented in Table 3.6.

The calculations show that the capa.A SiN_x has the highest thickness $t_d = 355$ nm among the tested SiN_x, which is approximately 25 nm higher, compared to the deposition parameters summarized in Table 3.2. The capa.B, capa.C and capa.D wafers have comparable thickness of the dielectric t_d, which is comprised between 250 and 260 nm and which is in agreement with the deposition parameters. The measured values of capacitance have low dispersion, below 3 %. It suggests that the samples have uniform dimensions (area, thickness) and very good reproducibility within each wafer.

Conduction mechanisms in PECVD SiN_x

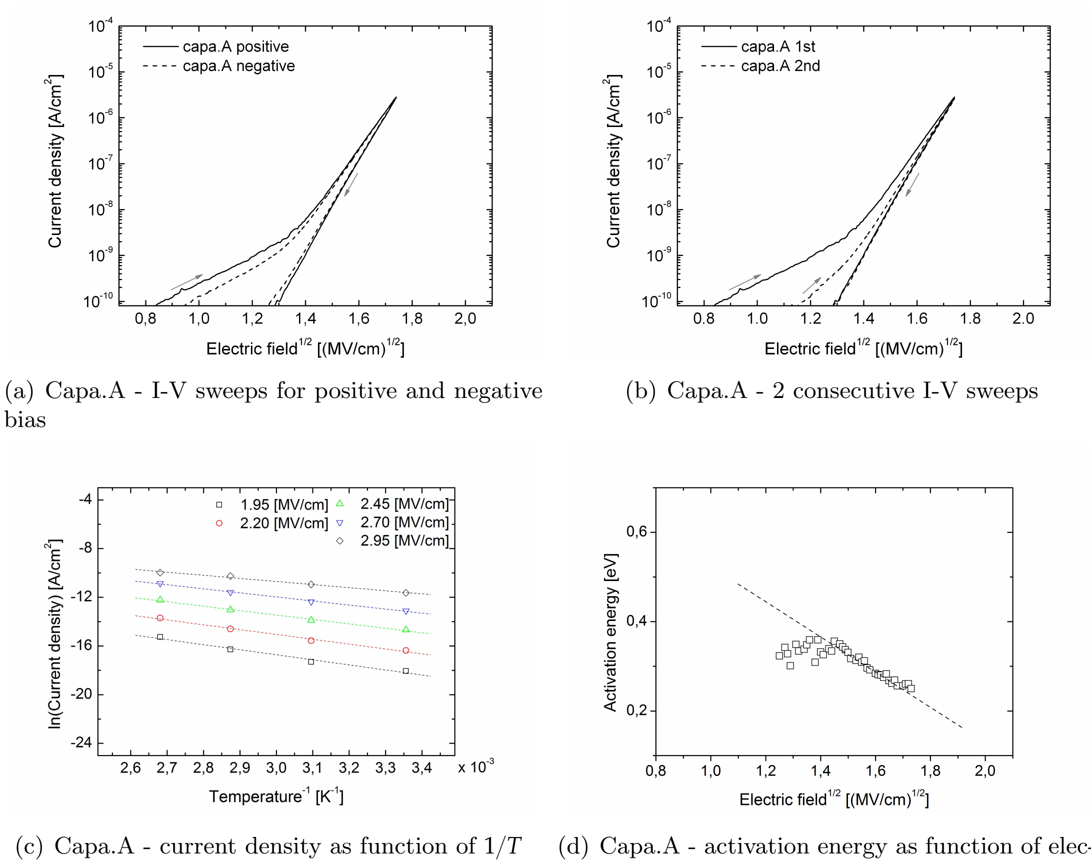
Capa.A (SiN_x HF)

Representative I-V sweeps for the capa.A dielectric are presented in Figure 3.21.

The shape of the ramp-up part of the first I-V sweep suggests two kinds of conduction mechanisms: one for low electric fields below 1.5 MV/cm with a large hysteresis and one above 1.5 MV/cm. Above 1.5 MV/cm, the I-V curve traces a straight line when $\ln(J)$ is plotted as a function of the electric field $E_d = V_{app}/t_d$. This electric field dependence is characteristic for the Poole-Frenkel or Schottky type emission.

To distinguish between these two mechanisms the I-V curves for positive and negative voltage are examined. For tested samples, the difference of the work functions between Al (top electrode) and Pt (bottom electrode) is 1.35 eV. As a result, in case of the electrode-controlled Schottky emission, the I-V curves for negative and positive voltage polarity would be different, while for the bulk-controlled Poole-Frenkel emission they would remain symmetrical. When we examine, the I-V curves measured for positive and negative voltage on the capa.A capacitor we can see that they are more or less symmetrical, which strongly supports the hypothesis that the conduction is of the Poole-Frenkel type.

The hypothesis of the Poole-Frenkel conduction is further confirmed by measurements made as a function of temperature, because the current density, for a given electric field, plotted as a function of the reciprocal temperature yields a straight line as presented in figure 3.21(c). This gives access to the zero-field energy barrier which is equal to 0.89 eV (as presented in



(a) Capa.A - I-V sweeps for positive and negative bias

(b) Capa.A - 2 consecutive I-V sweeps

(c) Capa.A - current density as function of $1/T$

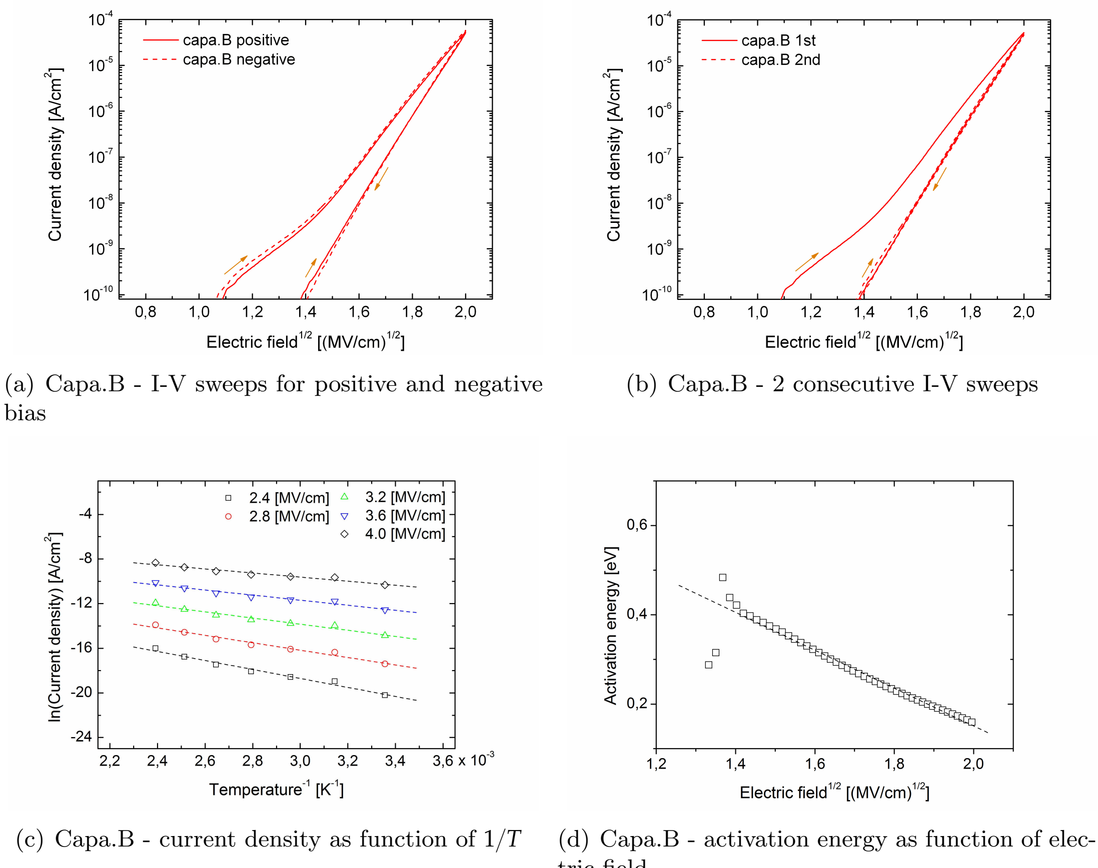
(d) Capa.A - activation energy as function of electric field

Figure 3.21: Analysis of conduction in capa.A dielectric (PECVD SiN HF)

Figure 3.21(d)) and which is in good agreement with the values reported in the literature [41, 43, 44, 68, 69].

Below 1.5MV/cm, the first I-V sweep show a large hysteresis which is largely reduced with consecutive I-V sweeps. This is supposed to be caused by charge build-up in the dielectric, which influences the distribution of the internal electric field. The origin of this effect might be space charge displacements in the presence of an external electric field and/or traps fillings by injected electrons [59]. When most of the available traps are filled and the mobile charges are swept to one electrode (e.g. hydrogen ions), the measured current follows the Poole-Frenkel conduction (Figure 3.21(b)). In this case, the slope of the plot $\ln(J) = f(E)$ is changed by the internal electric field in a dielectric created by trapped charges.

A fit of an I-V curve (positive bias, measured at room temperature) with Poole-Frenkel mechanism is done, with the fitting parameters: J_0 , β_{PF}, ϕ_0. For the ramp-up part above 1.5 MV/cm, the value of β_{PF} is found to be $4.49 \cdot 10^{-4}$ eVV$^{0.5}$cm$^{0.5}$ and the value of ϕ_0 is 0.87eV. The dielectric constant calculated from the value β_{PF} is $\epsilon_{r_{PF}} = 2.87$, which is in good agreement with values reported in [41, 43, 44, 68], despite the fact that it is lower from the static dielectric constant ϵ_r=7.5. The underestimation of the dielectric constant has been already discussed in paragraph 3.5.3.1. The most probable explanations are the use of the 1-dimensional Poole-



(a) Capa.B - I-V sweeps for positive and negative bias

(b) Capa.B - 2 consecutive I-V sweeps

(c) Capa.B - current density as function of $1/T$

(d) Capa.B - activation energy as function of electric field

Figure 3.22: Analysis of conduction in capa.B dielectric (PECVD SiN HF)

Frenkel model, instead of the 3-dimensional one, and the fact that the SiN_x has a lot of defect sites, which influences the β_{PF} coefficient. For the ramp-down, the value of β_{PF} is found to be $5.03 \cdot 10^{-4}$ $eVV^{0.5}cm^{0.5}$ and the value of ϕ_0 is 1.06 eV. The dielectric constant calculated from the value β_{PF} is $\epsilon_{r_{PF}} = 2.29$.

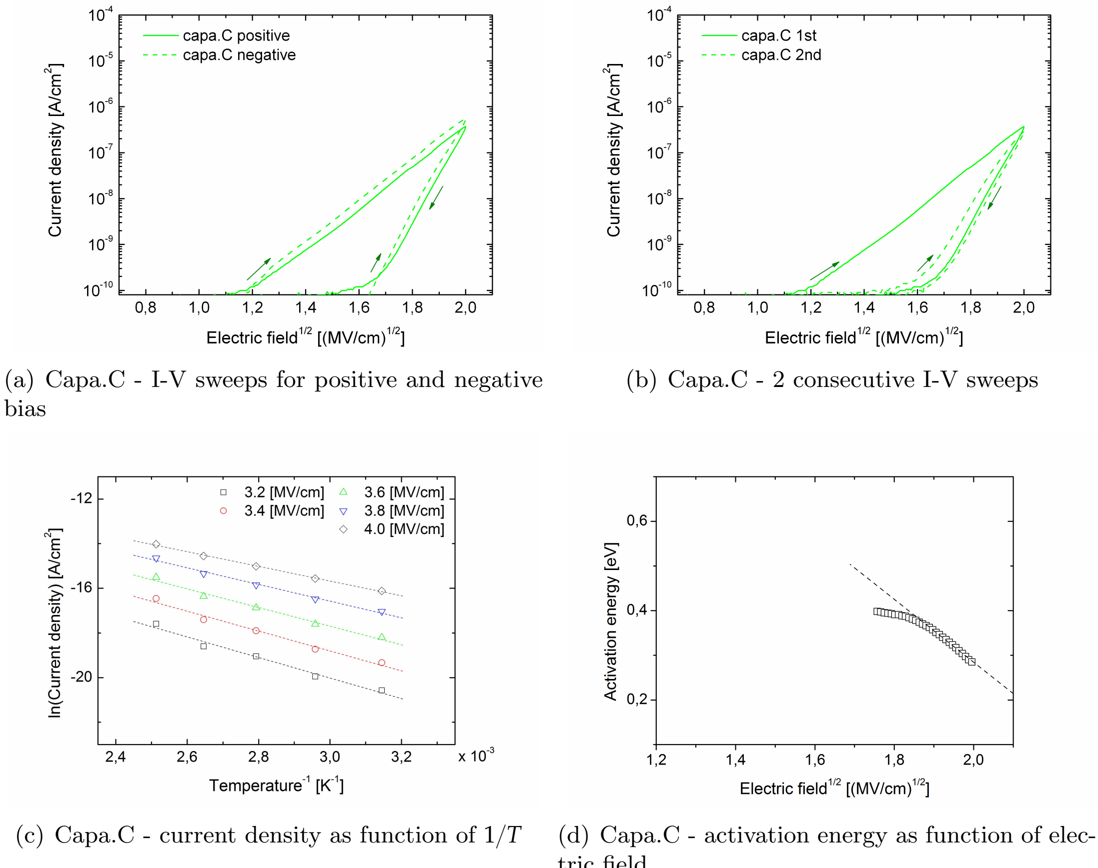
Finally, the conduction mechanism in the capa.A is identified as the Pool-Frenkel conduction.

Capa.B (SiN_x HF)

Representative I-V sweeps for the capa.B dielectric are presented in Figure 3.22.

Two representative consecutive I-V sweeps for the capa.B sample are presented in Figure 3.22(a). The first I-V sweep reveals a wide hysteresis between the ramp-up and the ramp-down, which is largely reduced by consecutive sweeps, similarly to the capa.A sample. The ramp-down part of the I-V curve is reproducible and it overlaps with the consecutive ramp-ups, so there is hardly any difference visible between them.

As in the previous case, when we plot $\ln(J)$ as a function of $\sqrt{E}$, the ramp-up and the ramp-down yield a straight line, which is characteristic either of Schottky emission or Poole-Frenkel conduction. The value of β_{PF} measured at 25°C is $4.10 \cdot 10^{-4}$ $eVV^{0.5}cm^{0.5}$, for the ramp-up, and $4.38 \cdot 10^{-4}$ $eVV^{0.5}cm^{0.5}$, for the ramp-down. The respective values of $\epsilon_{r_{PF}}$ are 3.44 and 3.02, as



(a) Capa.C - I-V sweeps for positive and negative bias

(b) Capa.C - 2 consecutive I-V sweeps

(c) Capa.C - current density as function of $1/T$

(d) Capa.C - activation energy as function of electric field

Figure 3.23: Analysis of conduction in capa.C dielectric (PECVD SiN MF)

obtained from the β_{PF} value, for the ramp-up and the ramp-down respectively. Theese values of the dielectric constant are similar to those obtained for the capa.A sample and favors the hypothesis of the Poole-Frenkel conduction.

The hypothesis of Poole-Frenkel conduction is further confirmed by the I-V measurements as a function of the temperature. The plot of current density as a function of the reciprocal temperature, for a given electric field yields a straight line, which confirms the Poole-Frenkel mechanism. In Figure 3.22 the activation energy, obtained from the measurements in function of temperature, is plotted as a function of E_d. The zero-field barrier height, which is extracted from these curves is 0.99 eV.

Capa.C (SiN_x MF)

Representative I-V sweeps for the capa.C dielectric are presented in Figure 3.23.

Two representative consecutive I-V sweeps for the capa.C samples are presented in Figure 3.23(b). Alike in the previous samples, the first I-V sweep reveals a relatively wide hysteresis between the ramp-up and the ramp-down, which virtually disappears in consecutive sweeps. This hysteresis is much larger than in the previously investigated samples. The ramp-down is reproducible, which suggests that most of the traps have been filled. A logarithm of current

density as a function of the square root of the electric field yields a straight line, for the ramp-up and the ramp-down. The slope of these two plots are used to calculate the value of β_{PF}. Measured at 25°C the value of β_{PF} is $2.63{\cdot}10^{-4}$ eVV$^{0.5}$cm$^{0.5}$, for the ramp-up and $4.38{\cdot}10^{-4}$ eVV$^{0.5}$cm$^{0.5}$, for the ramp-down. The corresponding values of $\epsilon_{r_{PF}}$ are 8.36 and 3.02.

The hypothesis of Poole-Frenkel conduction is further confirmed by the I-V measurements as a function of the temperature. The plot of current density as a function of the reciprocal temperature, for a given electric field yields a straight line, which confirms the Poole-Frenkel mechanism. Figure 3.23(d) presents the activation energy, as a function of E for the capa.C sample, as obtained from the measurements in function of temperature. The zero-field barrier height, extracted from these curves is 0.94 eV.

Charge trapping revealed in I-V curves

It has been demonstrated in [70–74] that an I-V curve can be a useful tool for assessing the amount of charge trapped in a dielectric. The major effect of the parasitic charge is a horizontal shift between consecutive I-V curves, through a change of the internal electric field. For instance, when a negative charge is trapped in the dielectric the consecutive I-V sweep is shifted towards higher electric fields. By taking the difference ΔV_{I-V} for a specific current between the initial and shifted I-V curve it is possible to determine the amount of the trapped charge in the bulk of dielectric, using the equation [73]:

$$\Delta V_{I-V} = \frac{e n_t t_d^2}{2\epsilon_0 \epsilon_r} \tag{3.27}$$

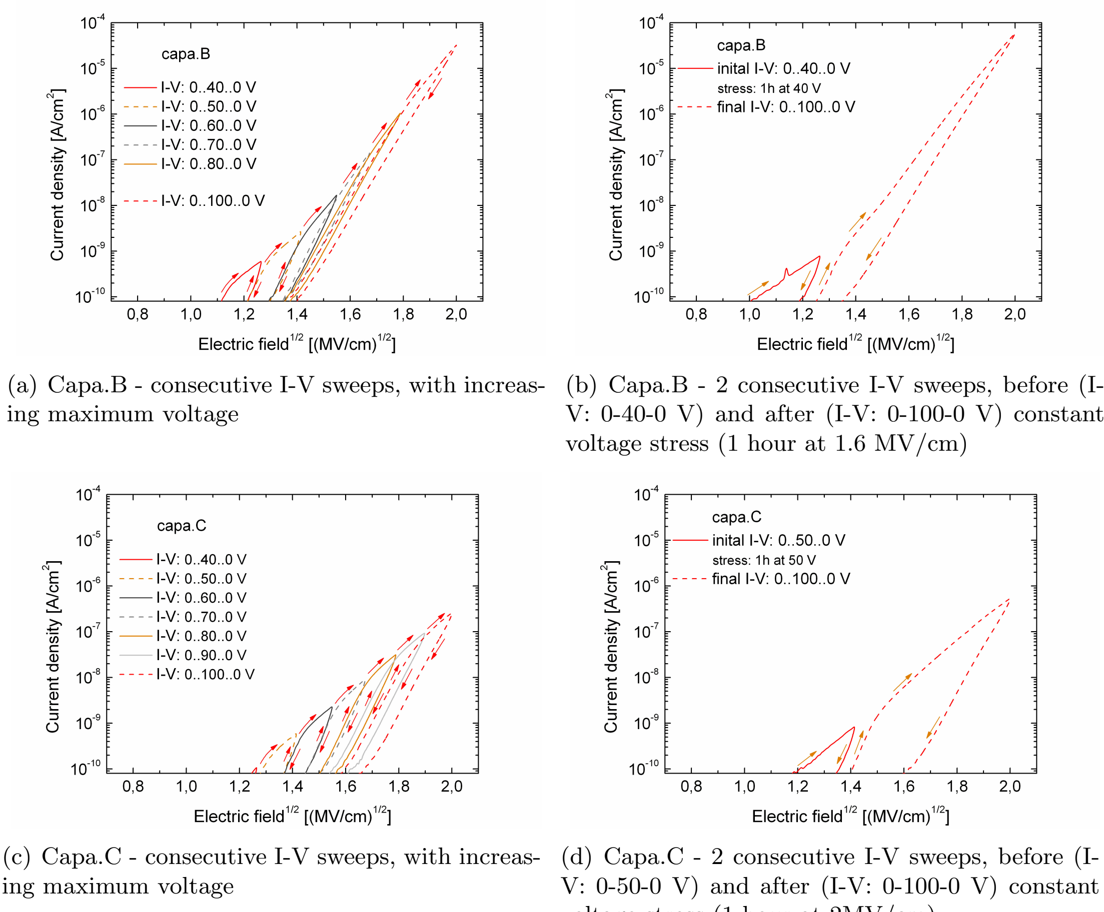
Here ΔV is the horizontal shift of the I-V curve and n_t is the concentration of the trapped charge. This equation is true, in a particular situation when the initial and consecutive I-V sweeps are parallel to each other.

In our case all three samples with SiN_x exhibit large hysteresis between the first and consecutive ramp-up, which is most likely due to the trapped charge. Unlike in the references mentioned above, the ramp-up parts of the initial and consecutive I-V curves are not parallel and it is not possible to use the equation 3.27 to calculate the amount of charge corresponding to the hysteresis. Nevertheless, in the following part of this paragraph we present some qualitative comparison of the effect of the trapped charge on the evolution of the shape of the I-V curves.

To demonstrate the effect of the trapped charge for different maximum voltages on the shape of the I-V curves, the consecutive I-V curves have been measured for increasing maximum voltages, as presented below.

The Figure 3.24 (a) and (c) show consecutive I-V curves, measured on the capa.B (HF SiN_x) and capa.C (MF SiN_x) samples. Each measurement consists of a number of consecutive I-V sweeps, where the maximum voltage of each following I-V sweep is increased by 10 V. The results of these measurements show that the ramp-down parts of each of these I-V curves are almost parallel to each other and they almost overlap with the ramp-up parts. The hysteresis and observed shifts of the I-V curve towards higher voltages (for a specific current) are due to electric field reduction in the dielectric due to trapped charge [71–74]. The shifts of the I-V sweeps towards higher voltages reveal that a negative charge is trapped in the dielectric. With each consecutive I-V sweep the hysteresis is decreasing.

For a more clear picture of the evolution of the hysteresis, the initial experiment is modified. In the new measurement an initial I-V curve is measured up to 40 V for the capa.B and 50 V for the capa.C. Then each of the samples is stressed during 1h, at a constant voltage stress level



(a) Capa.B - consecutive I-V sweeps, with increasing maximum voltage

(b) Capa.B - 2 consecutive I-V sweeps, before (I-V: 0-40-0 V) and after (I-V: 0-100-0 V) constant voltage stress (1 hour at 1.6 MV/cm)

(c) Capa.C - consecutive I-V sweeps, with increasing maximum voltage

(d) Capa.C - 2 consecutive I-V sweeps, before (I-V: 0-50-0 V) and after (I-V: 0-100-0 V) constant voltage stress (1 hour at 2MV/cm)

Figure 3.24: Analysis of conduction in capa.C dielectric (PECVD SiN MF)

of 40 V or 50 V to fill available traps. After this stress a complete I-V curve up to 100 V is measured.

The results of this measurements are presented in Figure 3.24 (b) and (d), for the capa.B and capa.C respectively. When an initial I-V curve is measured up to 40 V or 50 V it has the same shape, as the shape of the initial I-V curves presented in previous sections (*e.g.* Figure 3.25). When the second I-V curve, after the constant voltage stress, is measured, the leakage current is significantly reduced and in our case it is below the minimum measurable value up to 40 V or 50 V. This reduction of the leakage current is caused by the modification of the effective internal electric field in the dielectric due to the trapped charge. When the applied voltage exceeds the value of the stress voltage, the current suddenly increases and it follows the shape of the initial ramp-up of the first I-V curve. It can be concluded from this measurements, that after the samples are charged at a specific constant voltage stress, a number of traps is filled, which results in modification of the electric field in the dielectric and significant reduction of the leakage current.

In this point it is worth examining the shape of the ramp-up part of the I-V curve after

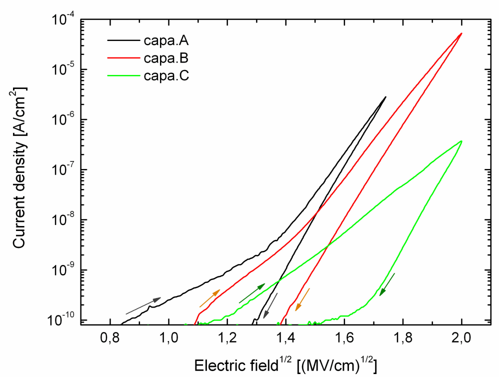


Figure 3.25: I-V curves on PECVD SiN_x.

several measurements with the shape of the ramp-down. When we compare these curves we can see that these two curves virtually overlap for the capa.B sample, while they show some offset for the capa.A and capa.C sample. The latter observation, that is the case when ramp-up and ramp-down curves do not overlap, may signify that some of the parasitic charge is detrapped, when the electric field is lowered.

Summary

The initial, positive bias I-V curves, measured at room temperature for all tested SIN_x are presented in Figure 3.25. The highest leakage current is measured for the capa.A and capa.B SiN_x, which are deposited in the high-frequency mode. The lowest leakage current is measured for the capa.C sample, deposited in mixed-frequency mode.

For all three SiN_x samples a large hysteresis is observed between the first ramp-up and the ramp-down part of an I-V curve. With consecutive measurements, the ramp-up of the I-V curve shifts towards higher voltages, which results from a reduction of the electric field in the dielectric due to trapping of negative charge.

In terms of the shape of the I-V curves, the ramp-up parts of the capa.A and capa.B, where the same type of HF SiN_x is used, are alike in the high electric field part (the traces are parallel to each other). In the low-field part the capa.A tends to have a less steep slope and a larger hysteresis, compared to the capa.B. The slope of the ramp-up is much different for the capa.C, where MF SiN_x is used. What is interesting, however, is that the slope of the ramp-down part of the I-V curve, is virtually the same for all the SiN_x, which suggests that they exhibit the same conduction mechanism, once most of the traps in these dielectrics are filled and the mobile charges are swept to one electrode. The only difference between the ramp-down parts for these samples is the horizontal offset, for a fixed current. The ramp-down part of the I-V curve for the capa.A sample is shifted towards the lowest electric fields, while the one of the capa.C sample is shifted towards the higher fields.

The conduction mechanism in all of the analyzed SiN_x is identified as a Poole-Frenkel-type conduction. The dielectric constant obtained from fitting the I-V curves, is 2.29 (capa.A) to 3.02 (capa.B and capa.C) and these results are summarized in Table 3.7. These values are much lower than the static values of ϵ_r, which is typically 7.5 for stoichiometric SiN_x. Nevertheless, these results remain in good agreement with those observed for PECVD SiN_x and the discrepancy between the dielectric constant extracted from the Poole-Frenkel model and the static one, has

Table 3.7: β_{PF} and dielectric constant ϵ_d of SiN_x as obtained form I-V curves

Sample	I-V curve	E range [MV/cm]	ϕ_0 [eV]	β_{PF}/β_S [$eV\sqrt{V}\sqrt{cm}$]	ϵ_d (P-F)
capa.A	initial ramp-up	1.7-3.0	0.87	$4.49 \cdot 10^{-4}$	2.87
	final ramp-up	1.6-3.0	1.01	$5.03 \cdot 10^{-4}$	2.29
	ramp-down	1.6-3.0	1.06	$5.03 \cdot 10^{-4}$	2.29
capa.B	initial ramp-up	1.7-4.0	0.73	$4.10 \cdot 10^{-4}$	3.44
	final ramp-up	3.0-4.0	1.00	$4.38 \cdot 10^{-4}$	3.02
	ramp-down	3.0-4.0	1.00	$4.38 \cdot 10^{-4}$	3.02
capa.C	initial ramp-up	2.2-4.0	0.76	$2.63 \cdot 10^{-4}$	8.36
	final ramp-up	2.2-4.0	0.94	$4.38 \cdot 10^{-4}$	3.02
	ramp-down	2.2-4.0	0.94	$4.38 \cdot 10^{-4}$	3.02

been explained by inaccuracy of the model and the influence of the defects in the material.

Conduction mechanisms in PECVD SiO_2

Capa.D (SiO_2 MF)

The analysis of conduction mechanisms in the SiO_2 has turned out to be more complicated than in case of SiN_x, mostly because of a very low leakage current (below 500 fA at 100V) and a low breakdown strength of the order of 3-4MV/cm.

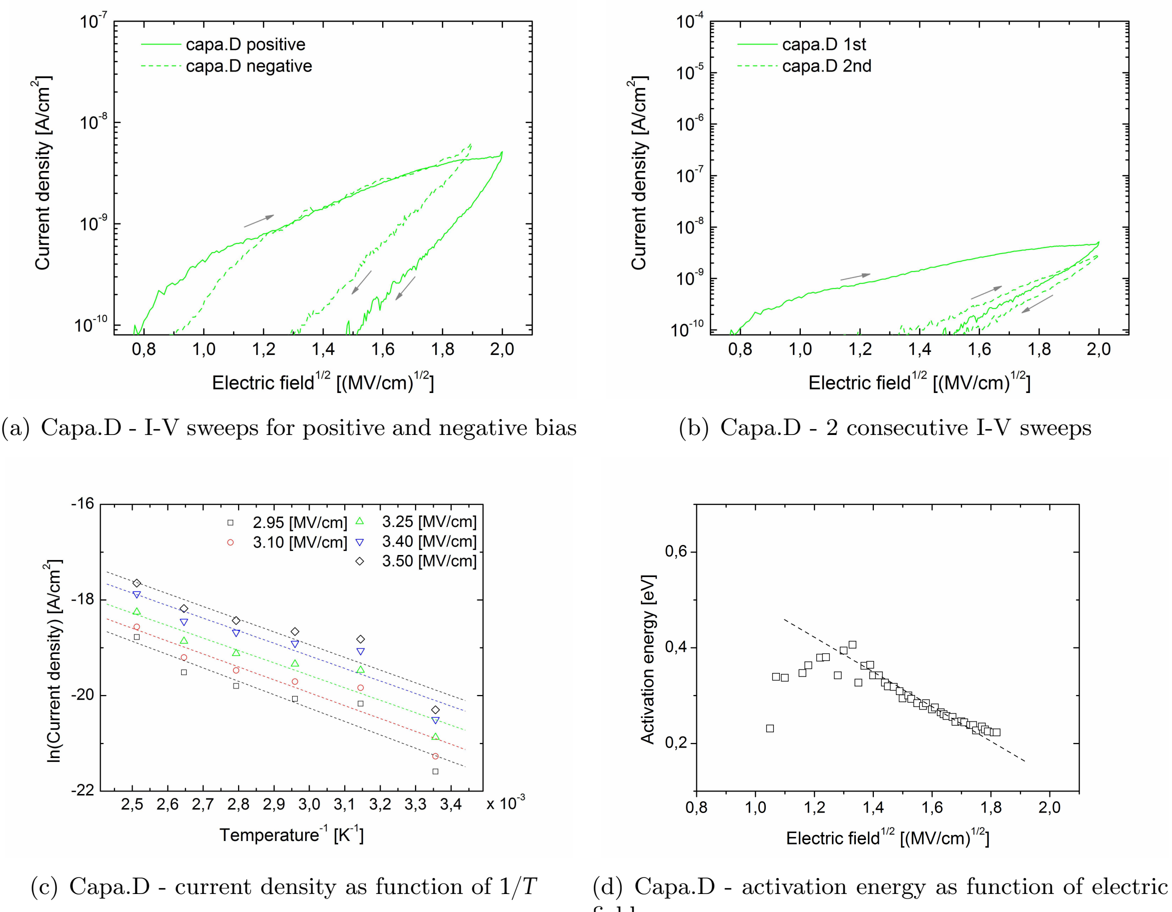
The most common conduction mechanism in SiO_2 at high electric fields (above 6 MV/cm) is of a Fowler-Nordheim type [55]. In the present case the electric field is lower, as it does not exceed 4 MV/cm and the shape of the I-V curves does not follow the Fowler-Nordheim relation. Consequently, the hypothesis of the Fowler-Nordheim conduction has been rejected.

Figure 3.26(a) presents representative I-V curves for positive and negative bias, measured on the MIM-capacitors, plotted as $\ln(J)$ as a function of $\sqrt{E}$. In general the level and the behavior of the I-V curve is similar for the positive and negative bias, however there is a 10-15V offset observed at the starting part of the I-V curves.

Similarly to the investigated SiN_x there is a large hysteresis observed between the ramp-up and the ramp-down part of the I-V curve. Unlike in the reference [70], in our case the ramp-up is not parallel to the ramp-down, thus it is not possible to calculate the amount of the trapped charge from the I-V curve offset, with satisfactory precision.

The shape of the first ramp-up part of the I-V sweep exclude Schottky and Poole-Frenkel conduction as the plot is not a straight line in the Poole-Frenkel coordinates. This curve is most likely to be fitted with the SCLC model.

On the other hand the ramp-up of the consecutive I-V sweep and the ramp-down both yield straight lines when $\ln(J)$ is plotted as a function of $\sqrt{E}$. This suggests that the conduction mechanism is either of Poole-Frenkel type or Schottky type. Considering the fact that the difference of work function between Al and Pt is 1.35 eV and the fact that there is a minor shift observed between the I-V curves for positive and negative voltage, none of these mechanism can be excluded. The hypothesis of the Poole-Frenkel or Schottky conduction is further verified by measurements made at high temperatures, which turn out to be temperature dependent (however the noise is rather high). The current density, for a given electric field, plotted against



(a) Capa.D - I-V sweeps for positive and negative bias

(b) Capa.D - 2 consecutive I-V sweeps

(c) Capa.D - current density as function of $1/T$

(d) Capa.D - activation energy as function of electric field

Figure 3.26: Analysis of conduction in capa.D dielectric (PECVD SiO_2 MF)

the reciprocal temperature yields a straight line in Figure 3.26(c) which gives access to the activation energy of 0.78 eV (from Figure 3.26(d)). The dielectric constant calculated from the slope of an I-V curve is $\epsilon_{r_{PF}}$ =11.99 and ϵ_{r_S} =2.99.

By taking into account the value of the known dielectric constant, the conduction in SiO_2 is more likely to be controlled by Schottky emission as the dielectric constant is closer to the static value of ϵ_{r_S} =3.7. Nevertheless, it is difficult to explicitly determine the conduction mechanism in this sample.

3.5.4 Identification of trapping properties

3.5.4.1 Introduction

This section is aimed at characterization of the trapping properties of the investigated dielectric materials.

It starts with a model, which shows how the trapped charge modifies the distribution of the electric field in the dielectric and consequently how it induces a shift of the applied voltage.

Then it presents existing models which describe the trapping kinetics, that is the evolution of the concentration of the trapped charge as a function of time for specific stress conditions. In this section three mechanisms are described, which are first order trapping, repulsive trapping and trapping with trap generation.

In the next part, the trapping properties of the SiN_x HF,SiN_x MF and SiO_2 MF are characterized. To do so, the samples are stressed with a constant current injection and the corresponding voltage drifts are measured. These experimental results are fitted with the presented models of trapping kinetics and the trapping properties of these dielectric are extracted.

3.5.4.2 Reduction of the electric field due to trapped charge

When a sheet of charge is trapped in the bulk of dielectric it results in the build-up of a space charge, which may induce a field reduction at the injecting electrode.

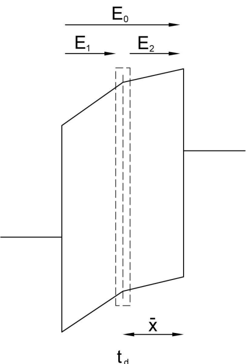


Figure 3.27: Modification of the electric field in the dielectric in the presence of trapped charge n_t in the bulk of the dielectric

In this section we calculate a value of voltage which is equivalent to the sheet of charge in the bulk of the dielectric at a distance $\bar{x}$, as presented in Figure 3.27. From the Gauss-Maxwell theorem it is possible to write the following system of equations:

$$E_{d_2} - E_{d_1} = \frac{en_t}{\epsilon_0 \epsilon_r} \tag{3.28}$$

$$E_{d_2}\bar{x} + E_{d_1}\left(t_d - \bar{x}\right) = V_{app} \tag{3.29}$$

Here, E_{d_1} and E_{d_2} are the electric fields in the dielectric, n_t is a surface concentration of trapped charges and $\bar{x}$ is the position of the sheet of the trapped charge from injecting electrode and V_{app} is the voltage applied across the dielectric.

After necessary transformations, the second equation can be rewritten in the following form:

$$E_{d_2} t_d = V_0 + \frac{e n_t t_d}{\epsilon_0 \epsilon_r}\left(1 - \frac{\bar{x}}{t_d}\right) \tag{3.30}$$

$$E_{d_2} = \frac{V_0}{t_d} + \frac{\Delta V}{t_d} \tag{3.31}$$

Here E_{d_2} is the electric field relevant for the injection current, $\frac{V_{app}}{t_d} = E_0$ and ΔV is the apparent shift in the voltage induced by the trapped charge n_t. By combining these equations it is possible to express the voltage shift as a function of the trapped charge [70]:

$$\Delta V = \frac{e n_t t_d}{\epsilon_0 \epsilon_r}\left(1 - \frac{\bar{x}}{t_d}\right) \tag{3.32}$$

As one can see, this model is neither time- nor stress-dependent so it cannot be used alone to describe the time- and stress-dependent voltage drifts in RF MEMS, which are induced by the charge trapped in dielectric. To do so, it is necessary to introduce models of trapping kinetics, which shows the evolution of this trapped charge n_t as a function of time and stress. These models are described in the following paragraph.

3.5.4.3 Models of trapping kinetics

Trapping kinetics - exponential model

The exponential model presented below is the most simple model describing the trapping kinetics. It is based on the following assumptions:

- the charges are trapped by an independent random process,
- the Coulombic interaction between trapped and untrapped charges may be neglected,
- detrapping is negligible,

The trapping rate in this model [70, 75] is given by a first-order reaction rate:

$$\frac{dn_t}{dt} = \frac{J_{inj}}{e}\frac{v_{th}}{v_d}\sigma\left(N_t - n_t\right) \tag{3.33}$$

Where N_t is the saturated trap concentration for given experimental conditions, rather than the total concentration, n_t is the filled traps surface concentration, v_{th} is the thermal velocity, v_d is the drift velocity and σ is the capture cross-section, which describes the probability of charge trapping.

The trap rate here depends on three factors. The first is the injection current density J_{inj}, the second is the capture-cross section σ and the third is the number of available empty traps $(N_t - n_t)$. The value of the injection current which is limited by the conduction mechanism defines the amount of the injected charges while the capture-cross section determines how effectively these injected charges are trapped. When the equation 3.33 is integrated one obtains the expression for the concentration of trapped charge as a function of time. For the simple model of the first order trapping, with the boundary condition $n_t(t_0) = 0$ and for one trapping center [70] the solution is:

$$n_t = N_t \left[1 - \exp \left(-\sigma \frac{v_{th}}{v_d} \frac{N_{inj}}{e} \right) \right] \tag{3.34}$$

where N_{inj} is the number of injected electrons per unit area equal to:

$$N_{inj} = \int_0^t \frac{J_{inj}}{e} dt \tag{3.35}$$

By combining the equations 3.32 and 3.35, the voltage shift corresponding to the amount n_t of the trapped charge, can be expressed as:

$$\Delta V = \frac{eN_t}{\epsilon_0 \epsilon_r} \left[1 - \exp \left(-\sigma_i \frac{v_{th}}{v_d} \frac{N_{inj}}{e} \right) \right] \left(1 - \frac{\bar{x}}{t_d} \right) \tag{3.36}$$

Trapping kinetics - logarithmic model

The logarithmic models of the trapping kinetics [76] reflect more complicated trapping processes and are obtained, in general, for the two situations described below:

- *Repulsive trapping:*

  This is the first order trapping model, which takes into account the fact that the already trapped charge repel injected charges, thus limits further trapping.

- *Trap generation:*

  This model corresponds to the trapping process, where the trapped charges generate new states, so the trapping rate increases with time.

Repulsive trapping

The repulsive trapping theory [76] states that charge trapping close to filled traps is less probable because of the Coulombic repulsion, so that the capture probability decreases with increasing space-charge. It is considered that the trapped charge inactivates for further trapping a volume h_d from a total volume V_d of the dielectric. The probability of trapping is reduced by $[1 - h_d/V_d]^{n_t}$ for n_t filled traps, where inactivation regions may overlap, which can be further simplified to the following form:

$$\left(1 - \frac{h_d}{V_d} \right)_t^n \cong \exp \left(\frac{n_t h_d}{V_d} \right) \tag{3.37}$$

The simplified trapping rate equation for the repulsive trapping, is then:

$$\frac{dn_t}{dt} = \frac{J_{inj}}{e} \frac{v_{th}}{v_d} \sigma^* \exp \left(-\frac{n_t h_d}{V_d} \right) (N_t^* - n_t) \tag{3.38}$$

Here N_t^* is the effective total surface trap concentration (in the logarithmic model) and σ^* is the effective capture cross-section (in the logarithmic model). It is necessary to mention that due to the simplifications introduced to the logarithmic model the values of N_t^* and σ^* are not directly comparable to the values from the exponential model.

After integration, an approximate solution of the equation 3.38 is found to be:

$$n_t = \frac{V_d}{h_d} \ln \left(\sigma^* \frac{N_t^* h_d}{V_d} \frac{N_{inj}}{e} \frac{v_{th}}{v_d} + 1 \right) \tag{3.39}$$

The above equation is equivalent to the equation 3.34 for the first order trapping.

Trap generation

Another trapping process, which may show logarithmic dependence has been described by [76, 77], based on the observation that an electron injected into an insulator at high electric field, may generate new traps.

The rate equation proposed for this process is:

$$\frac{dn_t}{dt} = n_0 \exp\left(\frac{E_{ln}}{E_{ln1}}\right) \frac{J_{inj}\sigma^*}{e} \tag{3.40}$$

Here E_{ln}, E_{ln1}, n_0 are constants.
The electric field reduction at the injecting interface, calculated from Poisson's equation, is:

$$E = E_d - \frac{N_t^* \bar{x} e}{\epsilon_0 \epsilon_r} \tag{3.41}$$

After combining equations 3.40 and 3.41 we obtain the trap rate equation for trapping with trap generation:

$$\frac{dn_t}{dt} = n_0 \exp\left(\frac{E_d}{E_{ln1}}\right) \exp\left(\frac{N_t^* \bar{x} e}{\epsilon_0 \epsilon_r E_{ln1}}\right) \frac{J_{inj}\sigma^*}{e} \tag{3.42}$$

After integration of this trap rate equation, we obtain the following expression for the number of trapped charges:

$$n_t = \frac{\epsilon_0 \epsilon_r E_{ln1}}{e\bar{x}} \ln \left[1 + \frac{n_0 \sigma^* N_{inj} e \bar{x}}{\epsilon_0 \epsilon_r E_{ln1}} \exp\left(\frac{E_d}{E_{ln1}}\right) \right] \tag{3.43}$$

General formula for logarithmic model

The two logarithmic models, which are presented above can be reduced to the same simplified form:

$$n_t = \ln\left(\frac{N_{inj} e}{Q^*} + 1\right) N_t^* \tag{3.44}$$

Here $e/Q^* = \sigma^*$ is equivalent to the capture cross-section from the exponential model and N_t^* is an equivalent to the total surface trap concentration.

This general model can be used to extract the equivalent values of σ^* and N_t^* even when the type of the trapping kinetics mechanism is unknown. The extracted values of N_t^* and σ^* are not directly comparable to the values from the exponential model.

3.5.4.4 Experimental procedure

Test setup
Introduction
As it has been explained in the previous section, the C-V measurements cannot be used for the MIM structures, which are investigated here. One of the methods, which is suitable for this type of test structures is constant current injection, which allows determining the trapping properties of a dielectric at high electric fields [78–85]. In this technique a constant current density is injected to the dielectric and the corresponding shift of the threshold voltage is measured. The main advantages of using this technique according to [70, 73, 74] are:

- The constant current injection technique is appropriate for studying trapping at very high electric fields, which are limited only by the breakdown field.
- Higher electric fields translate for higher injection currents, then lower capture cross-section can be studied at shorter times.

Because we have decided to study the MIM structures, the number of the experimental techniques that can be used to study the trapping properties is very limited. Amongst the available technique, the constant current injection technique has turned out to be the most suitable one and it is used here to study the trapping properties of the investigated dielectrics.

Test setup
The trapping kinetics is studied by constant current injections. The measurements are carried out using an Agilent 4156C Precision Semiconductor Parameter Analyzer. The samples are placed in a Cascade Microtech SUMMIT probe station in a dry nitrogen atmosphere (RH<2%). The connections between the test equipment and the device under test are realized with Kelvin triaxial cables. This setup allows measuring the currents as low as several fA, which is equivalent to a current density of several $1{\cdot}10^{-11}$ A/cm^2, for the samples that are used.

During a typical single measurement, a positive constant current density J_{inj} is injected from the top electrode into the dielectric and the voltage shift ΔV required to maintain this J_{inj} constant is recorded at 10-second intervals, during a maximum time of 14 hours. Depending on the type of sample J_{inj} is ranging from $5 \cdot 10^{-10}$ A/cm^2 to $1 \cdot 10^{-5}$ A/cm^2.

The injections are carried out in a linear mode, which means that the time interval between each sample is the same and it is in the range of 6-10 sec. The integration time, as in the previous case is set to LONG.

Test samples
The trapping properties are identified for all 3 types of dielectric (HF and MF SiN_x and MF SiO_2 on 4 wafers). The test samples are MIM capacitors. To avoid the problem with a leakage current through the substrate to the grounded chuck, the capacitors are modified, by removing a link between the pad on the wafer and the top electrode, as presented at the beginning of this chapter. For each constant current injection, a fresh sample is used.

3.5.4.5 Results

Trapping in PECVD SiN_x
Typical results of a constant current injection is a plot of a voltage drift ΔV as a function of

the injected charge N_{inj}. The results are plotted in a double logarithmic scales for all samples. Each of the measured voltage drift curves has two slopes. The first, steeper slope at short measurement time, is not relevant from the point of view of studying the kinetics of charge trapping, as it corresponds to charging of a MIM-capacitor with a constant current. It is then the second slope (less steep) which is used to determine the trapping kinetics by fitting it with either the exponential or the logarithmic models.

Representative results of constant current injections on MIM-capacitors for three wafers with PECVD SiN_x, for the same level of injection current, are presented in Figure 3.28. All 3 dielectric show the same nature of trapping kinetics, as the voltage drift traces a straight line in the double logarithmic scale. The voltage drifts measured for the capa.A and capa.B samples where the same type of the dielectric (HF SiN_x) is used are almost parallel. The voltage drift rate measured for the capa.C sample with MF SiN_x is higher compared to the other two samples.

The effect of the temperature on the constant current injections is presented in Figure 3.29, where the injections are carried out on the capa.C samples, for 25°C , 75°C and 125°C.

The measured voltage drifts yield a straight line with comparable slope when plotted in the double-logarithmic scale, regardless the temperature. The only difference between, these drifts is the shift towards lower voltage drifts for higher temperatures.

There are two possible explanations for this observation. The first one corresponds to the fact that the Poole-Frenkel conduction process is assisted by higher temperature. Consequently, the same level of the injection current, at higher temperature, can be obtained for a lower applied voltage (lower electric field in the dielectric). The second one corresponds to a change of the trapping properties, because the temperature increase favors thermal reemission and it induces a change in σ^*, which induces in turn a shift towards smaller voltage drifts.

A typical constant current injection for a positive and negative bias polarity is presented in Figure 3.30. In this figure the voltage drift for the capa.B dielectric is measured. This measurements show that there is no change in the kinetic of trapping for inverted voltage polarity. The small offset, which is observed between these two constant current injection curves is consistent with the offset observed in the I-V curves. It is likely to be associated with the work function difference between the electrodes of the MIM structure.

All three samples are well-fitted with the logarithmic model. To calculate the trapping parameters, the charge centroid, is arbitrary set in the middle of the dielectric, as it is not possible to characterize it with the available test devices.

The raw constant current injection plotted as a voltage drift as a function of the injected charge, together with the extracted trapping parameters N_t^* and σ^* plotted as a function of the average electric field in the dielectric, are presented in Figure 3.31 (a,b) for the capa.A, (c,d) for the capa.B and (e,f) for the capa.C.

The initial voltage is taken from the first ramp-up of corresponding I-V curves, for a leakage current equal to the injection current. This voltage is then subtracted from the raw constant current injection, to obtain the voltage drift.

For the capa.A in the range of electric fields from 1.9 to 2.5 MV/cm, the value of $N_t^* = 1.5 \pm 0.2 \cdot 10^{11}$ cm^{-2} is roughly independent of E_d. The value of σ^* is strongly field-dependent and it is decreasing exponentially with increasing E_d from 10^{-14} to 10^{-15} cm^2.

For the capa.B in the range of electric fields from 1.9 to 3.7 MV/cm, the value of $N_t^* = 2.3 \pm 0.2 \cdot 10^{11}$ cm^{-2} is roughly independent of E_d. The value of σ^* is strongly field-dependent and it is decreasing exponentially with increasing E_d from 10^{-12} to 10^{-17} cm^2.

For the capa.C sample, N_t^* =$0.9 \cdot 10^{12}$ cm^{-2} and it is almost 5 times higher, when compared

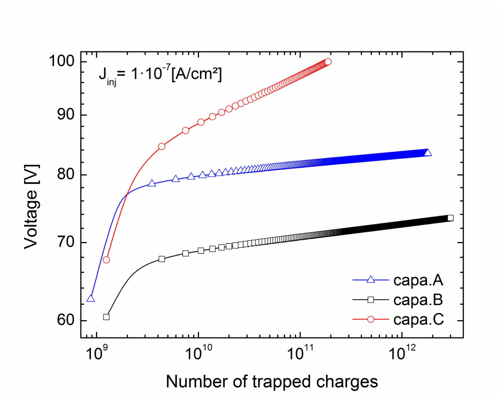


Figure 3.28: Comparison of 3 runs of PECVD SiN_x for the same injection current density

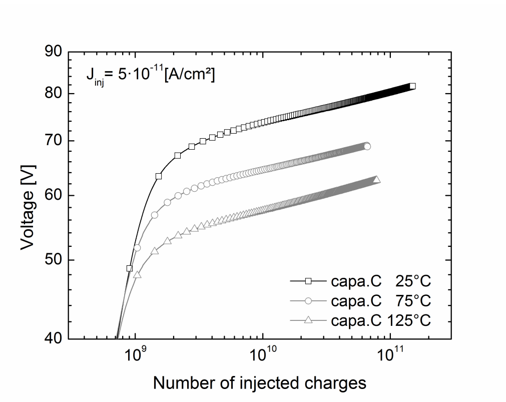


Figure 3.29: Effect of temperature on the voltage offset (capa.C)

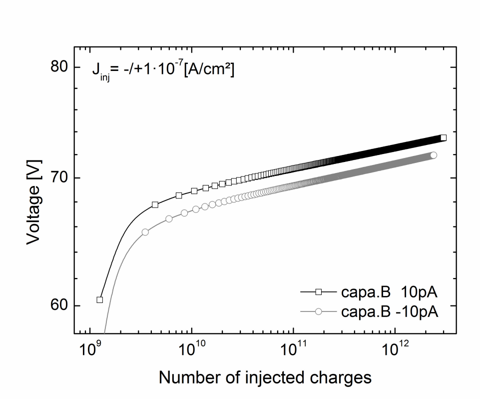


Figure 3.30: Effect of polarity of injection current (capa.B)

to the capa.B. Contrary to the capa.A and the capa.B the value of N_t^* increases slightly with E_d from $0.9{\cdot}10^{12}$ cm^{-2} to $2.0{\cdot}10^{12}$ cm^{-2}. The value of σ^* is decreasing exponentially with increasing E_d from 10^{-11} to 10^{-15} cm^2 alike in the other SiN_x samples.

To sum up, the samples with PECVD HF and MF SiN_x are all fitted well with the logarithmic model of trapping kinetics (most likely it corresponds to the repulsive trapping process). The lowest number of traps is found for the capa.A sample (HF SiN_x) and the highest for the capa.C sample (MF SiN_x). The total surface concentration of traps show no or weak dependence on the average electric field in the dielectric. On the other hand the capture cross section decreases exponentially with the average electric field. This observation can be explained by the fact that the probability of trapping (the capture cross-section) decreases exponentially when the defect site is farther from the surface [86], as given by the equation:

$$\sigma\left(E_d\right) = \sigma_0 exp\left(-2\kappa\bar{x}\right) \tag{3.45}$$

Here σ_0 is the capture cross-section of the defects at the interface and κ is the decay constant and $\bar{x}$ is the distance from the interface.

At the end, it is worth noticing that these trapping parameters are extracted for average electric fields, which are higher than those that prevail in the switch during normal operation. It is because for lower electric fields the leakage current is below the minimum measurable value of 1 fA.

Trapping in SiO_2

The identified trapping properties for the SiO_2 MF are presented in Figure 3.32.

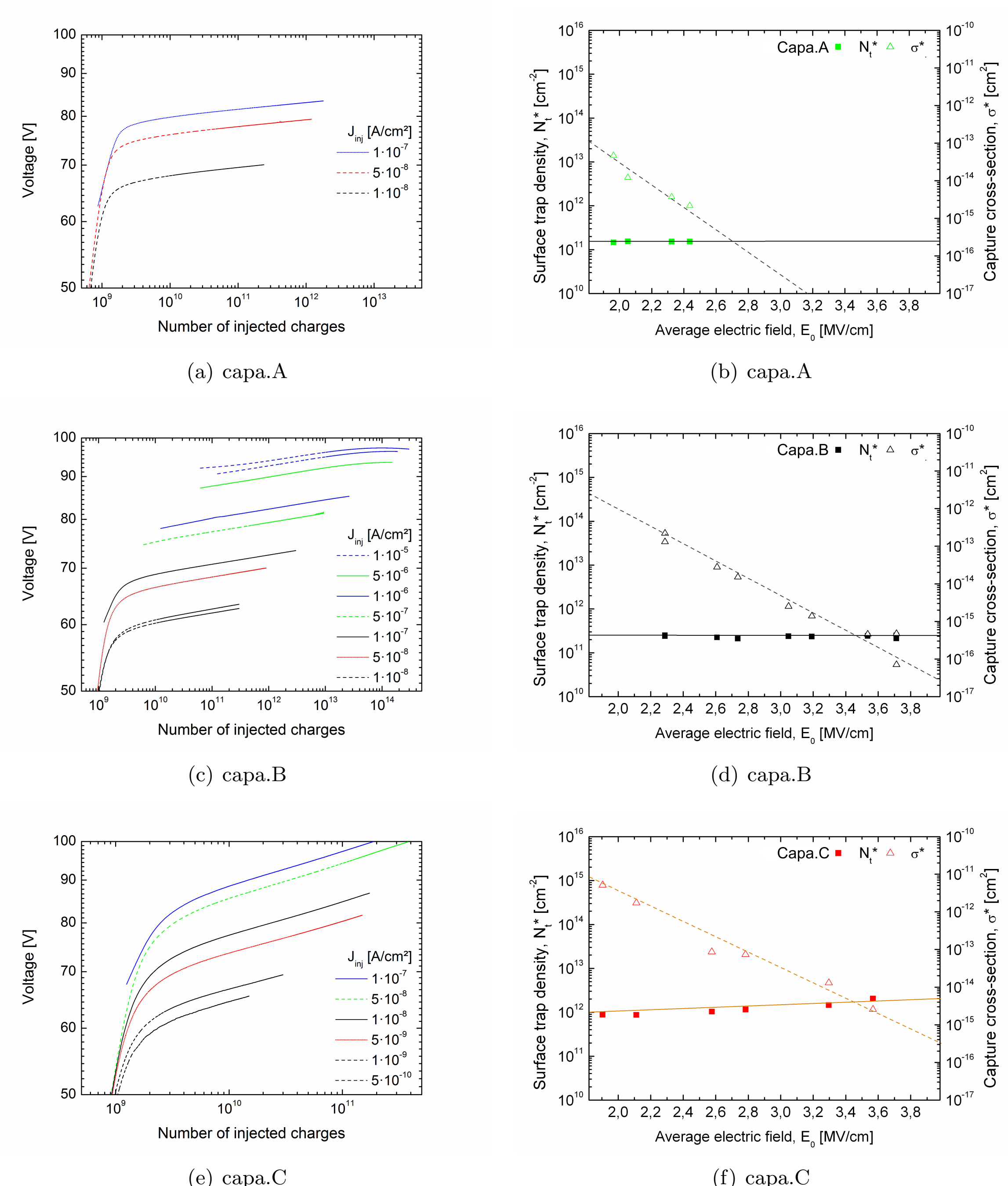
The raw voltage drifts, plotted in the double-logarithmic scale, figure 3.32 (a)) are much faster compared to those measured for all of the SiN_x layers. In this case, the constant-current injection curves are better fitted using the exponential model.

The trapping parameters, that is the total surface concentration of traps and the capture cross-section are almost independent of E_d, which is consisted with the first order trapping model. The extracted total surface trap concentration is $1.7{\pm}0.4{\cdot}10^{13}$ cm^{-2} and the capture-cross section is 10^{-15} cm^2. When it is compared to a thermal oxide the number of traps is higher and the capture cross-section is found to be rather large for the PECVD SiO_2.

3.5.5 Discussion of dielectric properties

The dielectric properties of the PECVD SiN_x and SiO_2, which have been studied in this chapter, that is the conduction mechanism and the trapping properties, turn out to be in good agreement with those already presented in the literature.

The conduction mechanism in all PECVD HF and MF SiN_x are found to be of the bulk-controlled Poole-Frenkel type. The first ramp-ups of the I-V curves of the samples with HF SiN_x are similar to each other and they differ from the first ramp-up of the I-V curve measured for the sample with MF SiN_x. The case of the HF SiN_x proves rather good reproducibility of the material properties between successive runs and also their stability, as we take into account the fact the capa.A sample was fabricated several months before the capa.B sample. On the other hand, the ramp-down parts of the I-V curves are parallel, regardless the type of the SiN_x dielectric. This observation suggests that when most of the available traps are filled and any ionic charges that are present are swept to one electrode, the mechanism of current conduction is the same for all investigated SiN_x despite deference in the deposition parameters.

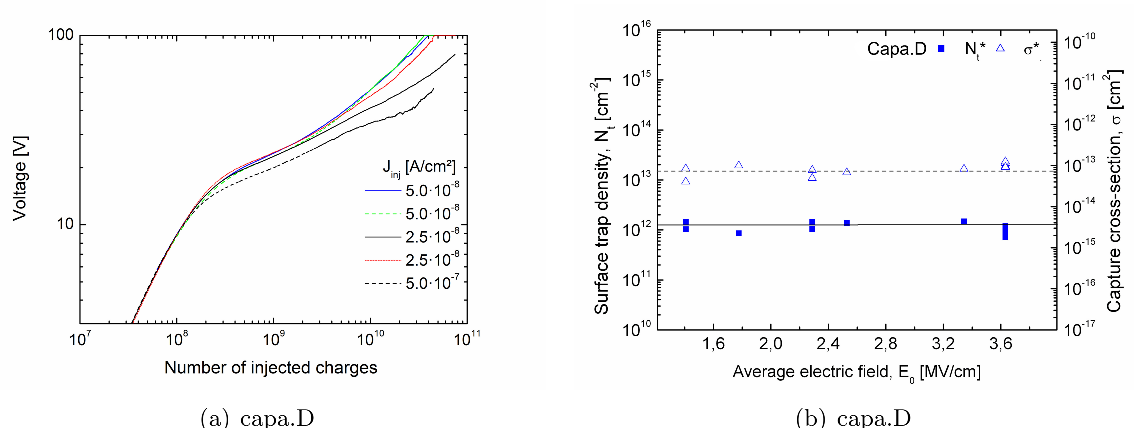


(a) capa.A (b) capa.A

(c) capa.B (d) capa.B

(e) capa.C (f) capa.C

Figure 3.31: Constant current injections on SiN_x and trapping properties as a function of average field in the dielectric.



(a) capa.D (b) capa.D

Figure 3.32: Constant current injections on capa.D

All samples show a wide hysteresis between the first ramp-up part and the ramp-down part of the initial I-V curve, which is due to trapping of negative charge in the dielectric. When we examine the ramp-down parts of the I-V curves for all the samples with SiN_x we can notice that they do not overlap but are shifted one to another. This horizontal shift may be related to the amount of trapped charge, because the sample which is shifted the most towards higher voltages is the capa.C sample with MF SiN_x for which the highest surface trap concentration was measured. On the other hand, the sample shifted the most towards the lower voltage is the capa.A with HF SiN_x, which has the lowest surface trap concentration.

In case of capa.B the consecutive ramp-up is overlapping with the ramp-down, which may suggest no, or weak detrapping. For the remaining samples, there is always an offset of several volts between the consecutive ramp-up and the ramp-down, which is likely to be attributed to detrapping.

The conduction mechanism in the SiO_2 has been identified to be most likely of the Schottky emission type, once the sample is charged.

The trapping kinetics follows the logarithmic model of repulsive trapping for all SiN_x dielectrics and the exponential model of the first order trapping for SiO_2. As the logarithmic model requires some simplifications, it is not possible to compare directly the figures, that are extracted, for these two materials.

The total number of traps in all the layers of SiN_x is virtually no or weak field dependent, while the capture cross section decreases exponentially with increasing electric field, which is consistent with the logarithmic model of repulsive trapping, where the already trapped charges decrease the probability of further trapping.

The samples with HF SiN_x have in general a lower total surface concentration of traps compared to the MF SiN_x. The samples with a lower number of traps exhibit also higher leakage current and their I-V curves are shifted towards lower electric fields.

The total number of traps and the capture cross-section of the SiO_2 show no dependence on the average electric field in the dielectric, which is also consistent with the first order trapping model.

3.6 Conclusions

Three types of PECVD dielectric that are used in RF MEMS switches have been analyzed in this chapter. These dielectric are high- and mixed-frequency PECVD SiN_x deposited at 300°C and mixed-frequency PECVD SiO_2 deposited at 150°C.

A number of experimental techniques have been successfully used to determine the structure and composition of the dielectric layers in real capacitive-type RF MEMS switches. In particular:

- The TEM microscope observations revealed, that all investigated PECVD dielectrics (the HF and MF SiN_x and MFSiO_2) are amorphous due to low deposition temperature.
- During the deposition of the dielectric layers, the particles from the bottom electrode are sputtered to the plasma and are redeposited in the dielectric creating crystalline aggregation near the bottom electrode. In particular, Pt is present in all investigated films, in the form of crystalline spots embedded in the dielectric in the immediate vicinity of the Pt bottom electrode. The spots are located at a distance of 2-10 nm from the electrode surface and have a diameter of 2-5 nm.
- The RBS, NRA and ERDA measurements show that the HF PECVD SiN_x dielectrics are Si-rich, with the N/Si ratio equal to 0.74, while the MF PECVD SiN_x is almost stoichiometric with its N/Si ratio equal to 1.16. The SiO_2 turns out to be non-stoichiometric with an O/Si ratio equal to 0.81.
- The RBS and ToF-SIMS measurements confirm that both the HF and MF SiN_x layers are highly hydrogenated, as they contain approximately 23 at. % of H, as expected for the low temperature nitrides. EDS and ToF-SIMS measurements reveal also considerable amount of O present in these dielectrics. On the other hand the MF PECVD SiO_2 contain as low as 3.4 at.% of H.
- The ToF-SIMS depth profiles show that traces of Al and Pt are present across the entire thickness of all investigated the dielectrics, which had to be introduce during the fabrication process. Traces of K, Na and C are identified at the dielectric - bottom electrode interface. The conclusion of the ToF-SIMS analyses for the SiN_x layers is that the contamination profiles are similar, despite different deposition conditions and storing time, which favors a hypothesis that the contaminations present in these dielectric are not intrinsic but are due to the fabrication process flow, which is identical for these samples (except the phase of deposition of the dielectric). For the SiO_2 the same elements as for the SiN_x have been detected.
- Traces of Ga are identified during EDS measurements at the dielectric-top electrode interface but no such traces are measured by ToF-SIMS. The most likely explanation of the presence of Ga, is the preparation of the TEM samples by the FIB technique, which uses a gallium beam to sputter the material.

The same materials have been submitted to electrical tests to determine the conduction mechanism and the trapping properties.

- The conduction mechanism in the HF and MF PECVD SiN_x is identified to be of the Poole-Frenkel emission type, while for the MF PECVD SiO_2 it is most likely to be of the Schottky emission type.

- The I-V curves for all investigated dielectric show a large hysteresis between the first ramp-up and the ramp-down, which is reduced with consecutive I-V sweeps. For a fixed current, the I-V shifts towards higher voltages, which reveals that a negative charge is trapped in the bulk of dielectric and it modifies the internal electric field.

- Once the dielectric is charged, the ramp-up and ramp-down parts of the I-V curve almost overlap. For the three samples with HF and MF SiN_x the ramp-down parts of the I-V curves (for charged dielectric) are virtually parallel, which support the hypothesis that these materials exhibit the same conduction mechanisms.

- The trapping kinetics identified in all PECVD SiN_x layers is best fitted with the logarithmic model of repulsive trapping, while in the SiO_2 it is best fitted by the exponential model of first order trapping. The total surface concentration of traps cannot be directly compared between the SiN_x and SiO_2 as different models are used. Within the group of SiN_x the lowest total surface trap concentrations are measured for the HF SiN_x, which have the higher leakage current (for a fixed electric field).

Chapter 4

Reliability testing and lifetime modeling in MEMS switches

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4.1 Introduction

This chapter is focused on testing long term reliability of the electrostatically actuated RF MEMS switches.

The first part of this chapter is aimed at characterizing the long term behavior of selected capacitive- and ohmic-type RF MEMS switches fabricated by the CEA-Leti. It starts with a presentation of the test method and samples followed by the summary of test results, which are pull-in voltage drifts measured during constant-voltage stress tests.

The second part of this chapter is focused on modeling of dielectric charging in RF MEMS switches. It starts, with a brief overview of existing mathematical and physical models, which concern the dielectric charging failure mode in RF MEMS switches. The next paragraph presents and discusses our physical model of parasitic charge build-up in a dielectric, which is a new

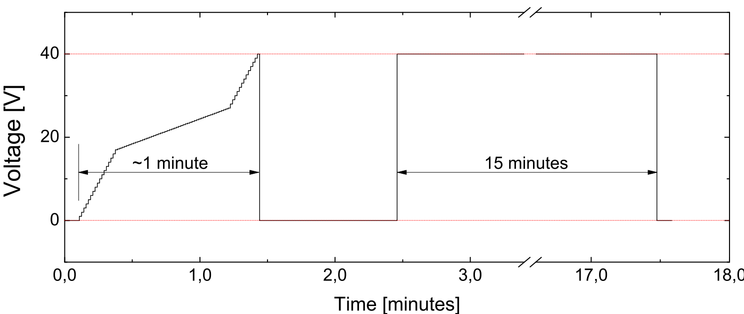


Figure 4.1: Voltage ramp applied during constant voltage stress (40V) - 1 iteration

approach to modeling of the pull-in voltage drifts in RF MEMS. This model is used to simulate voltage drifts for the capacitive- and ohmic-types switches that have been characterized in the first part of this chapter. The model is verified by comparing these simulated voltage drifts with the experimental ones. After positive verification of the model it is used to investigate the impact of the dielectric material and the switch design on the voltage drifts.

4.2 Lifetime characterization of RF MEMS switches

4.2.1 Introduction

In the first part of this chapter, we characterize the long term behavior (lifetime) of selected capacitive- and ohmic-type RF MEMS switches. These characterizations are done by measuring the drifts of the pull-in voltage as a function of time for different levels of a constant-voltage stress (CVS).

4.2.2 Experimental procedure

4.2.2.1 Test methods

The drift of the pull-in voltage is determined from the shift of the C-V and R-V curves, which are registered every 15 minutes during the constant-voltage stress. These measurements are carried out using the CarOhm test-bench, which has been already presented in Section 2.6.2.1.

A typical constant-voltage stress test consists of a number of iterations. The voltage ramp during a single iteration is presented in Figure 4.1.

Each iteration starts with a unipolar voltage ramp for measuring the C-V and R-V curves, which are used to determine the pull-in voltage. For capacitive-type switches the pull-in voltage is obtained from the C-V curve and it is defined as a voltage when the membrane is pulled-in and the capacitance increases form C_{up} to C_{dn}. For the ohmic-type switches, the R-V curve is used, and the pull-in voltage is defined, as the value when the ohmic contact is closed, that is the switch resistance decreases from the off-state value R_{off} to the on-state value R_{on}.

The C-V and R-V curves are measured for the same bias polarity as the constant voltage stress. The unipolar C-V (R-V) curves are chosen to avoid discharging of the parasitic charge, which could be enhanced by the opposite polarity of the voltage during C-V (R-V) measurement. The main drawback of the unipolar C-V curves is that they cannot be used to evaluate the

window between the negative and positive pull-in voltages, which is used to examine the switch against narrowing [87]. In this thesis, however, only the voltage drifts of pull-in voltage and not narrowing are investigated.

The voltage ramp is limited to the ramp-up part, which is not linear to increase the resolution of the pull-in voltage measurements. The maximum voltage resolution of 0.1-0.2 V is set for voltages around the initial pull-in voltage, and the minimum voltage resolution of 1-1.5 V is set in the remaining range.

The second part of each iteration is a 15-minute holding at the constant-voltage stress. During this stress the switch capacitance (or resistance) is measured every 1 minute to ensure that the switch remains in the closed state.

The constant voltage stress tests presented in this chapter were measured for positive voltage stress of 40, 50, 60, 70 V during the total time of approximately 6 to 25 hours (25 to 100 iterations). The maximum stress voltage was limited by the dielectric strength of the investigated materials, as dielectric breakdown was observed in a number of samples above 70V.

The CVS tests were carried out also for negative voltage stress giving results similar to those for the positive voltage stress. For the sake of simplicity, in the remaining part, only the results for the positive bias are presented.

4.2.2.2 Test samples

The test samples for the constant voltage stress tests are selected in terms of the type of the dielectric material used and the switch design.

Effect of dielectric material

The effect of the type of the dielectric on the long term behavior of the RF MEMS switches is investigated for all three types of the PECVD dielectrics which are HF SiN_x, MF SiN_x and MF SiO_2. Switches for these tests are selected from the same manufacturing run of capacitive switches, that is capa.B, capaC and capa.D introduced in chapter 3. For these three wafers the fabrication tools have been the same and these wafers have been stored in the same conditions for the same period of time. As a result the material properties, geometrical features or any potential contaminations should be similar for these three types of dielectric.

Effect of switch design

The effect of the switch design on the long term behavior of the RF MEMS switches is tested on 2 characteristic wafers of the ohmic-type switches, which are ohm.A and ohm.C. For the selected switches, there is no difference in the type of the dielectric used, which is HF PECVD SiN_x for each wafer, the same as for the capa.A and capa.B wafers.

When compared to the capacitive-type switches, the investigated ohmic-type switches have much higher variations of the roughness of the bottom electrode surface, which is contact with the dielectric. Consequently, in the ohmic-type switches, the effective electric field E_s can vary significantly for different wafers.

The ohm.A and ohm.C have been selected for the further tests because of the highest difference of the roughness of the bottom electrodes, which results in different separation of the top and the bottom electrodes in the closed state.The ohm.A switches have relatively smooth surface of the electrode, while the ohm.C switches have multiply relatively high (400-500 nm)

peaks present on their electrodes. The smooth surface of the ohm.A samples results in low residual air-gap, thus the electric field across the dielectric in the switch E_s is approximately 55% of the nominal one E_d. On the contrary, the rough surface of the ohm.C, results in the value of E_s, which is around 10% of the nominal E_d. What is more, the hillocks on the electrode surface not only reduce the effective electric field in the dielectric, but can also reducue the effective contact area for charge injection, which may further contribute to lowering of the voltage drifts. The SEM images of the electrodes and corresponding AFM profiles for these switches have been presented in chapter 2 in Figure 2.8.

As we assume that the properties of the dielectrics are comparable for both samples, in case of any difference in the measured pull-in voltage drifts it would be the different geometry (the roughness of the bottom electrode), which could explained this potential difference.

The measurements are carried out on unpackaged switches. The samples are placed in a probe station in dry nitrogen atmosphere (RH < 2 %) at atmospheric pressure. Before each series of measurements, all switches are dried, by heating them to approximately 130°C and holding then for several hours in high vacuum and then in dry nitrogen. After these thermal treatment the samples are left for 24 hours in dry nitrogen in room temperature to cool down. The purpose of drying of the samples is to avoid the influence of capillary forces due to humidity on the movement of the top electrode.

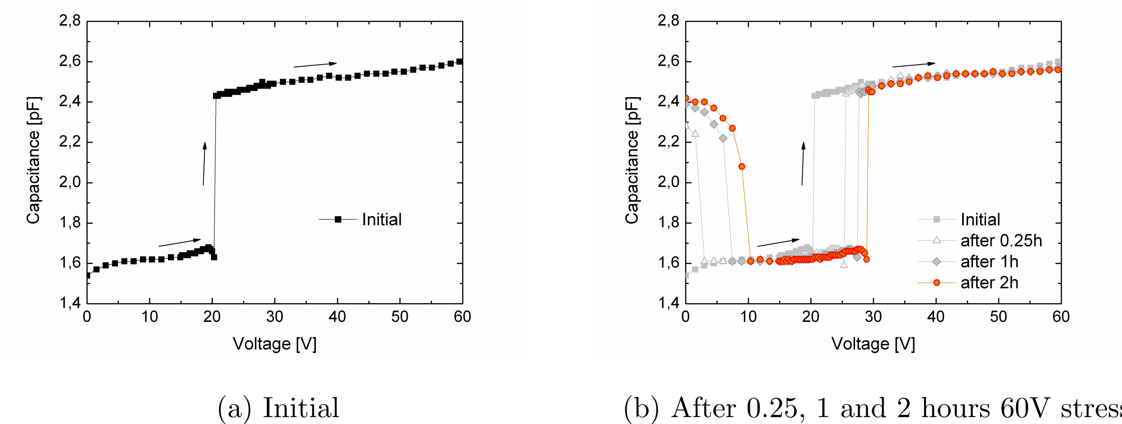
4.2.3 Results

4.2.3.1 Capacitive-type switches

The effect of the trapping of parasitic charge in a dielectric of the capacitive-type switches on their C-V characteristics is presented in Figure 4.2. A typical initial C-V curve of a capacitive-type switch from the capa.B wafer is presented in Figure 4.2 (a), while the C-V curves after 0.25, 1 and 2 hours of the constant-voltage stress test at 60 V is plotted in Figure 4.2 (b). In the second figure we can see that the initial C-V characteristics is shifted towards higher actuation voltages and, in the present case, the initial pull-in voltage V_{pi} is shifted from, approximately 20 V to 30 V during the first 2 hours of the 60 V stress. This figure shows also why this voltage drift is a critical parameter and it explains how it limits the lifetime of the RF MEMS switches. In the initial C-V characteristics the switch remains open when no voltage is applied. In the present example, after the voltage stress, the negative pull-out voltage is shifted towards positive voltages, which results in the switch remaining in closed position at 0V (stiction). As the switch remains closed, when no bias is applied, thus it is not functional any more [88]. Another possibility, is that the shifted pull-in voltage may exceed the applied voltage and the switch could not be closed any more.

To simplify the analysis of the voltage drifts and comparisons between stress levels and samples, the measured drifts of the pull-in voltage ΔV (obtained form the C-V curves) are plotted as a function of cumulative stress time. Figure 4.3 summarizes the voltage drifts measured at 40 and 60 V constant voltage stress for the capa.B, capa.C and capa.D wafers during 6 to 25 hours. The plotted values are mean values from at least 3 samples. The results are plotted in linear and double logarithmic scales. For easier comparison, the results are plotted in the same scale, regardless of the stress voltage.

From Figure 4.3 it is apparent that the pull-in voltage is increasing as a function of the stress time for all investigated samples. Consequently, the voltage stress tests can be accelerated by increasing the level of the voltage stress.



(a) Initial (b) After 0.25, 1 and 2 hours 60V stress

Figure 4.2: Exemple of C-V curves before and after 60 V constant voltage stress, measured for the capa.B sample.

The observed voltage drifts are faster at the beginning of the CVS test and saturate with time. When the measured voltage drifts are plotted in the double-logarithmic scale they roughly yield a straight line, except the capa.D sample with the layer of MF SiO_2 stressed at 40 V, during the first couple of minutes of the voltage stress.

The values of the voltage drifts after 1h, 6h and 24h for all 3 types of dielectrics are given in Table 4.1.

The measurements show that all switches are concerned by the problem of the dielectric charging. It turns out that despite the same switch design, the voltage drifts are different for all 3 dielectrics. The highest drifts are measured for the samples with the PECVD SiN_x layers (capa.B and capa.C). Among these samples the highest voltage drifts are observed for the mixed-frequency SiN_x (capa.C). Compared to the capa.B and capa.C wafers, the capa.D wafer with the mixed-frequency PECVD SiO_2 shows much lower voltage drifts.

4.2.3.2 Ohmic-type switches

In case of the ohmic-type switches the voltage drifts have been measured for the ohm.A and ohm.C samples, for 40 V constant voltage stress during 25 hours. The mean results from 3 samples are presented in Figure 4.4 where the voltage drifts are plotted in a linear and double-logarithmic scales, similarly to the results for the capacitive-type switches.

In this figure we can see, that despite the same dielectric have been used (PECVD HF SiN_x) in both samples, the voltage drifts are different. The highest drift is measured for the ohm.A switch, where it is as high as 17 V after 25 hours of the 40 V stress, while for the ohm.C sample it is only 5 V for the same stress voltage and time. Despite different maximum values of the voltage drifts, both drifts yield a straight line when plotted in the double-logarithmic scale, alike the capacitive-type switches with the HF SiN_x layer.

4.2.3.3 Discussion

It has been demonstrated in this part that the drift of the pull-in voltage is a lifetime-limiting factor for the RF MEMS switches. Provided that the voltage stress is high enough the C-V

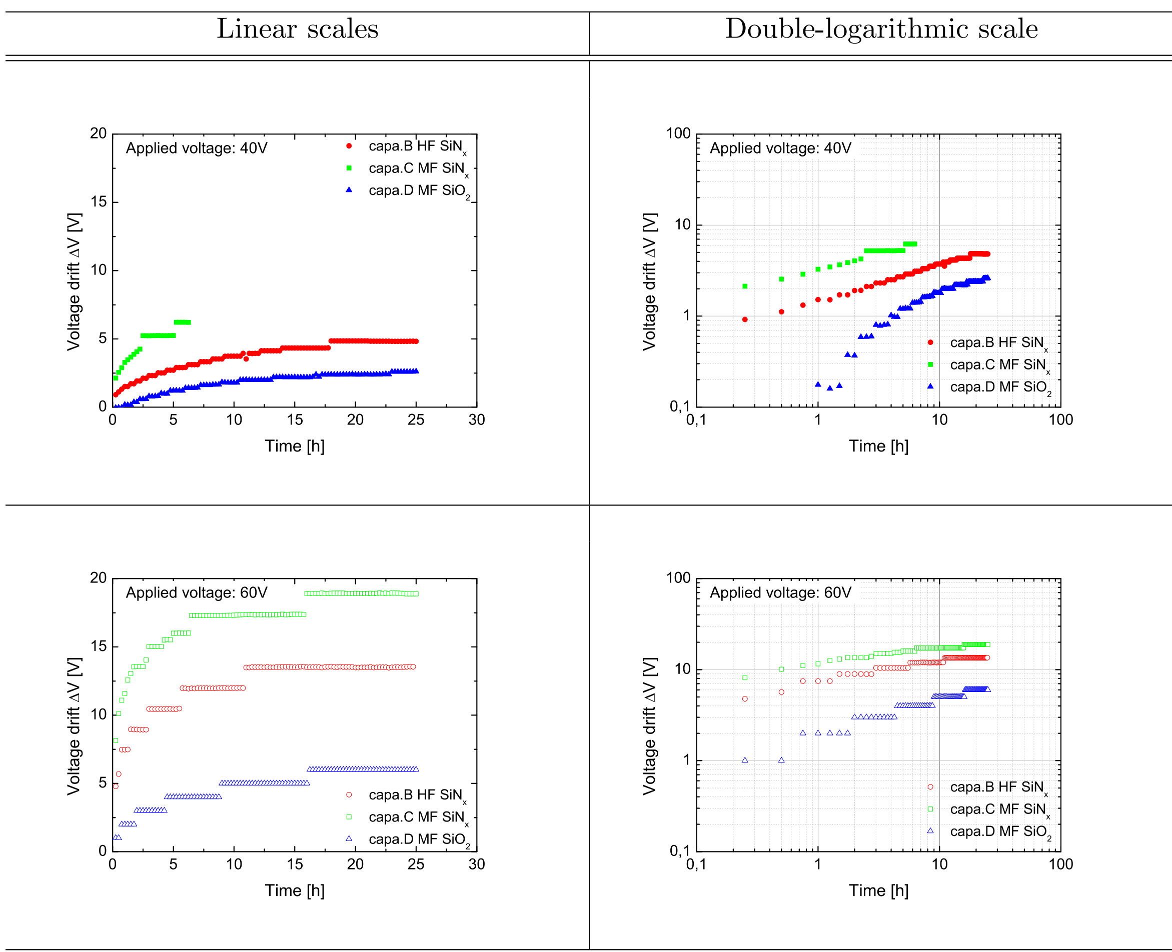


Figure 4.3: Pull-in voltage drift rates, measured during constant voltage stress, for all investigated types of dielectrics in capacitive-type switches (SiN_x HF, MF and SiO_2 MF.

Table 4.1: Average voltage drifts after 1h, 6h and 24h of 40 and 60 V constant voltage stress.

Wafer	Dielectric	Test at 40 V			Test at 60 V		
		1h	6h	24h	1h	6h	24h
capa.B	HF SiN_x	1.5	2.9	4.8	7.5	11.9	13.5
capa.C	MF SiN_x	3.3	6.2	10[1]	11.6	16.0	18.9
capa.D	MF SiO_2	0.2	1.4	2.6	2	4	6

[1]Extrapolated value

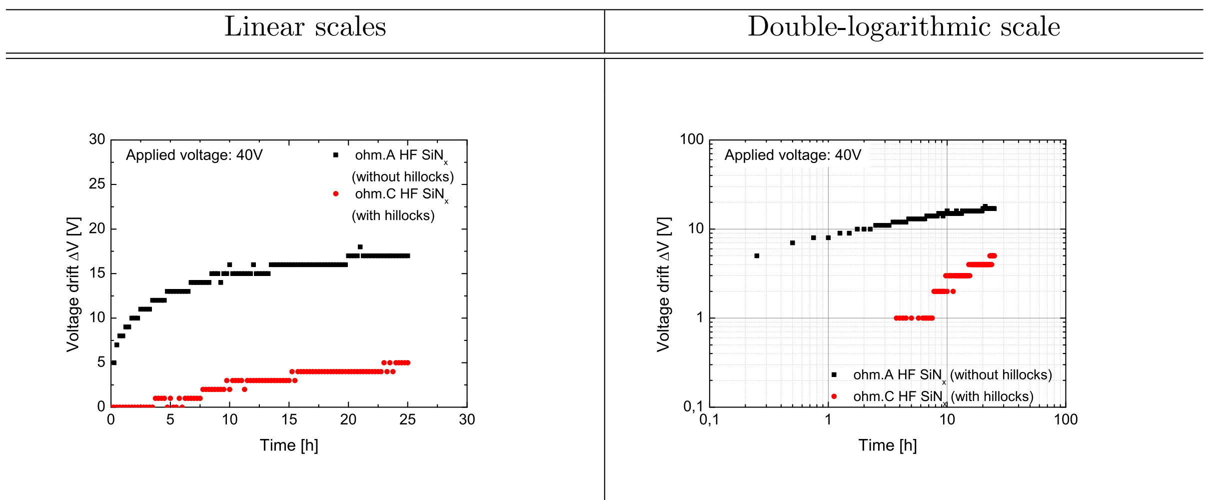


Figure 4.4: Results of pull-in voltage drift measurements for ohm.A and ohm.C switches, plotted in a linear and double-logarithmic scale.

curve of the electrostatically actuated switches can be shifted, so that the pull-in voltage of the switch V_{pi} may exceed the applied voltage V_{app}, which results in the switch remaining open and being not operational any more.

The measurements show that all switches, regardless of the dielectric layer used and the switch type, are affected by the problem of the dielectric charging.

The constant voltage stress tests can be simply accelerated by increasing the applied voltage. By doing so the measured voltage drifts are faster and can reach higher values, but their kinetics remains unchanged. The maximum applicable voltage stress is limited by the dielectric strength of the investigated layers.

The impact of the dielectric material on the measured drifts of the pull-in voltage is best visible in case of the capacitive-type switches which have the same geometry, including the area and thickness of the dielectric. When we compare the results for SiN_x and SiO_2 layers we can conclude that higher voltage drifts are observed for the devices with SiN_x layers rather than SiO_2. If we compare the SiN_x layers, the one deposited in the mixed-frequency mode (MF) shows higher drifts compared to the high-frequency (HF) one.

The impact of switch geometry can be compared for the ohmic-type switches with the same dielectric, which is the case of the ohm.A and ohm.C sample, where the SiN_x HF is used. This comparison reveals that the switch design has an effect on the measured voltage drifts. Despite these samples show different maximum voltage drifts, they exhibit the same nature of the trapping process, as all the voltage drifts yield a straight line when plotted in the double-logarithmic scale. From this observation, it can be concluded that the material type and its dielectric properties define the nature of the trapping process, while the geometry of the switches may have an effect on the magnitude of the observed voltage drifts.

4.3 Modeling of dielectric charging in RF MEMS

4.3.1 Introduction

For making successful commercial applications of the RF MEMS switches, it is not enough to show working demonstrators, but it is necessary to show a capability of fabricating devices with a guaranteed minimum lifetime, under given operating conditions. The prediction of the lifetime of the RF MEMS switches is not trivial, as it requires the identification and understanding of the factors which have influence on it.

This section is focused on the modeling of the dielectric charging phenomena in the RF MEMS switches. It starts with a brief critical review of the models presented in literature. Next we present and discuss our model of the parasitic charge build-up. Eventually, this model is used to calculate theoretical voltage drifts for the capacitive- and ohmic-type type switches with PECVD HF and MF SiN_x and MF SiO_2, which are then compared with the measured ones. At the end the model is used to investigate the impact of the dielectric material and the switch design on the measured voltage drifts.

4.3.2 Existing models concerning dielectric charging in RF MEMS

A common approach to testing new switch designs and dielectric layers is to produce a complete switch with required modification and to submit it to accelerated voltage stress tests. This method gives good results but it is neither time- nor cost-effective. Moreover, the correlation between the switch design, dielectric properties and the resulting voltage drifts is not always straightforward as there could be many factors that may have an influence on the switch behavior.

In order to improve our understanding of the influence of the design and the dielectric properties on the voltage drifts a lot of effort has been put into modeling the dielectric charging phenomenon.

One group of models are general physical models, which address the problem of dielectric charging, but are not relevant for predicting the long term behavior of RF MEMS switches. In this group, the first general model, which is indispensable to the analysis of dielectric charging in RF MEMS switches, is used to calculate the distribution of the electric field across the air gap and the dielectric layer in the switches.

The second general class of models, describes how a parasitic trapped charge influence the electrostatic force when voltage is applied across the actuation electrodes, in other words it shows the influence of a parasitic trapped charge on the C-V characteristics of the RF MEMS switches.

Another group of models, which are relevant from a reliability point of view, can be used to predict the voltage drift as a function of time. This group can be split further into two categories, which are mathematical fits and physical models.

The first group in this category are sets of mathematical functions which are found to fit well with the experimental voltage drifts measured on fabricated switches. These models are typically used to fit measured voltage drift over a specific period of time and to extrapolate them for longer stress times and different stress voltages. Despite being practical for determining the lifetime of fabricated switches, these models fail to explain the origins of the observed voltage drift, thus they are of little help in improving the switch reliability.

The second group in this category are physical models, which try to establish a correlation between the sensitivity of a switch to dielectric charging and the switch design and material

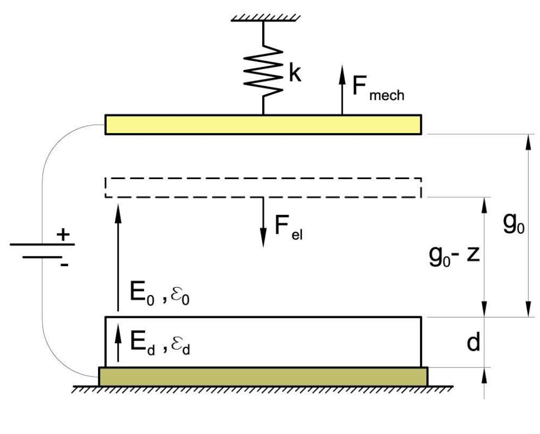


Figure 4.5: Schematic diagram of MEMS switch

properties. This group is the most interesting one as it allows, in principle, to predict the long term behavior of a switch based on its design and materials properties without the need of manufacturing a complete switch.

4.3.2.1 Effective electric field in RF MEMS

Before analyzing the effect of the voltage stress on the dielectric it is important to understand how the applied voltage translates to the electric field in the dielectric, and how this electric field is distributed in a typical RF MEMS switch.

While in the MIM-capacitors the electric field is assumed uniform across the device $E_d = V_{app}/t_d$, in the MEMS switches the electric field, is distributed between the electric field in the air-gap E_0 and the electric field in the dielectric layer E_s.

In the down-state position, the value of E_s is theoretically equal to $E_d = V_{app}/t_d$ provided that there is an ideal contact between the movable electrode and the dielectric layer. In real switches, however, the electrode and the dielectric layer have a finite roughness, which prevents from an intimate contact between these two elements. As a consequence the effective electric field across the insulator of a real switch in the down-state position E_s is lower than the nominal value E_d, as presented in [89, 90].

The effective electric field in the dielectric is calculated, from Gauss flux theorem for a switch [89, 90], which is schematically presented in Figure 4.5 is:

$$E_0 (g_0 - z) + E_s t_d = V_{app} \tag{4.1}$$

$$\epsilon_0 E_0 = \epsilon_0 \epsilon_r E_s \tag{4.2}$$

By approximating the switch by a parallel-plate capacitor, after necessary transformations, the ratio of the effective electric field in the switch E_s to the nominal electric field E_d, can be obtained from:

$$\frac{E_s}{E_d} = \frac{C_s}{C_d} \quad (4.3)$$

$$\frac{E_s}{E_d} = \frac{t_d}{\epsilon_r (g_0 - z) + t_d} \quad (4.4)$$

Here C_s is the capacitance per unit area of the switch and C_d is the capacitance per unit area of the MIM structure.

As a consequence of existing asperities on the contacting surfaces of the dielectric and the electrode, a non-zero air gap between the movable electrode and the dielectric ($(g_0 - z) > 0$) is always present. These residual air-gap results in lowering of the electric field in a switch E_s. The factors, which have impact on lowering of the electric field for a switch are:

- *Dielectric constant:*
  A lower dielectric constant results in a higher value of E_s (higher E_s/E_d ratio), provided that the dielectric thickness and roughness of the contacting surfaces are the same.

- *Dielectric thickness:*
  The thickening of the dielectric decreases the influence of the residual air-gap on the distribution of the electric field.

- *Roughness of contacting surfaces:*
  The higher the roughness of the contacting surfaces the higher the residual air-gap can be, what may result in significant reduction of the electric field E_s.

4.3.2.2 Effect of trapped charge on C-V characteristics of RF MEMS switches

Wibbler's model for uniform air-gap and charge distributions

The first model, which discusses the effect of a parasitic charge in the dielectric on functioning of MEMS switches was presented in 1998 [91–93]. This model shows how a uniform sheet of the trapped charge in the dielectric modifies the electrostatic force and consequently the pull-in voltage.

A schematic drawing of a switch, which is used to derive this model is presented in Figure 4.5.

Because the presented capacitor has to be electrically neutral, the sum of charges at the top σ_1 and bottom σ_2 electrodes of the capacitor and the parasitic charge σ_p in the dielectric layer has to be zero:

$$\sigma_1 + \sigma_2 + \sigma_p = 0 \quad (4.5)$$

Here σ_1 and σ_2 are the surface concentrations of charges on the plates of the capacitor and σ_p is the surface concentration of the equivalent parasitic charge, which is assumed to represent all charges in the dielectric and in the present example is adjacent to the air-gap.

The Gauss flux theorem, is used to calculate the distribution of electric fields in the air-gap E_0 and in the dielectric E_d, which are then expressed as a function of the charge surface concentrations:

$$E_0 = \frac{\Phi_0}{\epsilon_0} = -\frac{Q_1}{\epsilon_0 A_{el}} = -\frac{\sigma_1}{\epsilon_0} \quad (4.6)$$

$$E_d = \frac{\Phi_d}{\epsilon_0 \epsilon_r} = \frac{Q_2}{\epsilon_{0r} A_{el}} = \frac{\sigma_2}{\epsilon_{0r}} \quad (4.7)$$

Here, the Φ_0 and Φ_d are the electric flux densities, respectively in the air-gap and dielectric, Q_1 is the charge on the top electrode, Q_2 is the charge at the bottom electrode and A_{el} is the area of the electrodes.

The distribution of the voltage which is applied V_{app} to the switch across the air-gap and the dielectric can be expressed in terms of surface concentrations of charge (σ_1, σ_p):

$$V_{app} - \phi_{M_1 M_2} = V_0 + V_d \quad (4.8)$$

$$= E_0 (g_0 - z) + E_d t_d \quad (4.9)$$

$$= -\sigma_1 \frac{g_0 - z}{\epsilon_0} - \left(\sigma_1 + \sigma_p\right) \frac{t_d}{\epsilon_0 \epsilon_r} \quad (4.10)$$

Here V_0 and V_d are the voltage drops across the air-gap and dielectric respectively and $\phi_{M_1 M_2}$ is the difference of the work functions between the metallic electrodes. As this difference is usually small (1.3 eV in our case) compared to the actuation voltages (40-60 V) it is neglected in further calculations.

By combining the Equations 4.5 and 4.8 it is possible to find the relationship between the charge on the top electrode σ_1 and the parasitic charge σ_p, which is:

$$\sigma_1 = -C_s V_{app} - \frac{\sigma_p}{\frac{C_d}{C_0} + 1} \quad (4.11)$$

Here, C_s is the switch capacitance, C_d is the capacitance of the dielectric and C_0 is the capacitance of the air-gap.

From the above equation 4.11 we can see that the parasitic charge at the dielectric-air gap interface generates charges on the movable electrode, thus it modifies the electrostatic force, for a given value of V_{app}.

The electrostatic downward force acting on the top, movable, electrode, can be expressed as a function of charge concentration σ_1:

$$F_{el} = -\frac{E_0 Q_1}{2} \quad (4.12)$$

$$= \frac{(\sigma_1)^2 A_{el}}{2\epsilon_0} \quad (4.13)$$

$$= \frac{A}{2\epsilon_0} \left(\frac{V_{app} + \sigma_p \frac{t_d}{\epsilon_0 \epsilon_r}}{\frac{g_0 - z}{\epsilon_0} + \frac{t_d}{\epsilon_0 \epsilon_r}} \right)^2 \quad (4.14)$$

The electrostatic force, can also be written in a compact form, as a function of the applied voltage, as it has been presented in Chapter 2. When a voltage offset due to the parasitic charge is taken into account, this equation has the following form:

$$F_{el} = \frac{C_s^2 A_{el} \left(V_{app} - \Delta V_p\right)^2}{2} \tag{4.15}$$

After combining the equations 4.12 and 4.15, it is possible to calculate the value ΔV_p, which is the offset voltage, induced by a sheet of parasitic charge σ_p placed at a distance $\bar{x}$ from the air-gap-dielectric interface, given by the equation [94]:

$$\Delta V_p = -\frac{\sigma_p t_d}{\epsilon_0 \epsilon_r}\left(1 - \frac{\bar{x}}{t_d}\right) \tag{4.16}$$

This model explains the effect of the parasitic charge trapped in the dielectric on the functioning of MEMS switches. It shows that this trapped charge generates a (parasitic) electrostatic force. Depending on the sign of the charge this force may have the same or opposite direction to the actuating electrostatic force generated by the applied voltage. Consequently, this parasitic electrostatic force modifies the initial pull-in voltage, which is observed as a shift of a C-V curve.

Rottenberg's model for non-uniform air-gap and charge distributions
The model devised in [91, 94] succeeds in explaining the shift of the C-V curves observed in the MEMS switches, submitted to voltage stress. Apart from a shift of the pull-in voltage (shift of a C-V curve) the narrowing of the window between the negative and positive pull-in voltages is frequently observed in RF MEMS switches submitted to the voltage stress tests. The model which has been presented in the previous paragraph fails to explain the narrowing of the C-V curves.

The narrowing phenomenon is explained in [87, 95], where the authors propose a further generalization of the Wibbler's model as they associate the narrowing of the C-V curves to a non-uniform distribution of the parasitic charge in the dielectric. The narrowing of the C-V curve is modeled by introducing the distribution of the capacitance C_{distr} and the distribution of charge on the top electrode σ_{distr} due to trapped charge in this equation:

$$F_{el} = \frac{C_s^2 A_{el} \left(V_{app} - V_p\right)^2}{2} \tag{4.17}$$

$$= \frac{A_{el} C_{distr}^2}{2\epsilon_0}\left(V - \frac{\sigma_{distr}}{C_{distr}}\right)^2 \tag{4.18}$$

Here, σ_{distr} is calculated as:

$$\sigma_{distr} = \frac{t_d \sigma_{eq}}{\epsilon_0 \epsilon_r} C_{distr} \tag{4.19}$$

Here, σ_{eq} is the equivalent surface charge distribution placed at the air-gap-dielectric interface.

The distribution of the capacitance, which is equivalent to distribution of the air-gap, and the distribution of the charge concentrations are characterized by mean values μ and variance σ^2. By taking the distributions into account the equation 4.19 can be written in a general form:

$$F_{el} = \frac{A}{2\epsilon_0}\left[\left(V\mu_{C_{distr}} - \mu_{\sigma_{distr}}\right)^2 + V^2\sigma^2_{C_{distr}} + \sigma^2_{\sigma_{distr}} - 2Vcov\left(C_{distr}, \sigma_{distr}\right)\right] \tag{4.20}$$

The authors conclude that both the distribution of the air-gap and the distribution of the trapped charge in the dielectric layer, may result in the narrowing of the observed C-V curves.

Discussion
These two models are static ones and associate the shift and/or narrowing of C-V curves, with a presence of a layer of parasitic charge in the dielectric or at its surface.

Thanks to these models it is possible to calculate the amount of equivalent charge corresponding to a specific voltage shift. Or, they can be used in the other way round, to calculate a voltage drift corresponding to a given amount of the trapped charge located at a given position in the dielectric. As these are static models they cannot be used to predict the voltage drift as a function of time, that is to predict the switch lifetime. Moreover they do not provide any information about the physics of the charge trapping, thus they are irrelevant from the point of view of assessing switch lifetime and can hardly be used for optimizing the switch design or material properties.

4.3.2.3 Existing approaches to lifetime modeling

Mathematical models (fitting functions)
The most simple models which can be used to predict the lifetime of RF MEMS switches are presented in [96]. These models are actually a set of mathematical functions which have been experimentally verified to fit well with the typical voltage drifts measured on fabricated RF MEMS switches. In general, there are 3 fitting functions, which are commonly used to fit the voltage drifts ΔV measured for MEMS switches. The experimental ΔV plotted as a function of time, can be fitted with:

Square root fit

$$\Delta V(t) = a\sqrt{t} + V_0 \tag{4.21}$$

Exponential fit [97–99]

$$\Delta V(t) = V_{max}\left(1 - \exp\left(-kt\right)\right) + V_0 \tag{4.22}$$

Stretched exponential fit [100, 101]

$$\Delta V(t) = V_{max}\left(1 - \exp\left(-kt^{\delta}\right)\right) + V_0 \tag{4.23}$$

Herfst's generic fitting function

A further generalization of these models have been proposed in [96]. By analysis of experimental voltage drifts, measured for capacitive-type RF MEMS switches, with PECVD SiN_x as a dielectric layer, it has been concluded that the voltage drifts are well fitted with a generic function, of the following form:

$$\Delta V(t) = \alpha\sqrt{t}\exp\left(\beta V_{app}\right) \tag{4.24}$$

Here α and β are parameters, which are found from fitting of the experimental voltage drifts.

Papaioannou's model of charge build-up

The parasitic trapped charge located at the dielectric air interface lowers the electrostatic force, as it has been presented in previous paragraphs. This lowering of the electrostatic force makes the top electrode to move up with decreasing electrostatic force, which results in a change of the switch capacitance. The change of the capacitance can then be related to the parasitic charge build-up. It has been presented in [100, 102] that the transient of the switch capacitance for a constant voltage stress is well fitted by a stretched exponential function, in the case of PECVD SiN_x.

The function that has been showed to work well and that could be used to assess the amount of the trapped charge has had the form:

$$\Delta C = \frac{A_{el}\sigma_1}{k_s\epsilon_0}\frac{\frac{t_d}{\epsilon_r}}{\left(g_0 + \frac{t_d}{\epsilon_r}\right) - t_d}C_s^2\Delta\sigma_2 \tag{4.25}$$

Discussion

The models presented above can be used a posteriori to extrapolate a voltage drift measured over a limited period of time for longer stress times. The main drawback of these fits is that it is not possible to predict the behavior of a MEMS switch, until it is fabricated. Moreover, these fits provide virtually no information on the origin of charge trapping and its physical mechanism. Consequently, they can hardly be used to improve the switch reliability (the design or the fabrication process). The most advanced model, from the family of the mathematical fits, is the one proposed by Papaioannou. It extends the previously presented models as it tries to capture the nature of the kinetics of charge build-up, which is included in the fitting function (Williams-Watts-Kohlrausch law) [100] as the time-dependent value of σ_1.

Physical models

Melle's model of charging controlled by leakage current

The first attempt to correlate the voltage drifts measured from the RF MEMS switches with the switch design and the electrical properties of the dielectric used, has been done by Melle and is presented in [89, 90, 103, 104].

In this model the build-up of the parasitic charge, which is equivalent to the voltage drift, is assumed to be directly proportional to the density of the leakage current across the dielectric layer:

$$\frac{\Delta V}{\Delta t_{down}} \propto J_{inj} \tag{4.26}$$

Here t_{down} is the time during which the switch remains in the closed position.

The material studied in [89, 90, 103, 104] has been PECVD SiN_x and the leakage current has been determined from the I-V measurements and has been found to be controlled by the Poole-Frenkel mechanism. In this case the drift rate has been calculated from the equation:

$$\frac{\Delta V}{\Delta t_{down}} = \eta \frac{t_d}{2\epsilon_0 \epsilon_r} \exp\left(\frac{-e\phi_0}{k_b T}\right) \exp\left(\frac{e\beta_{PF}\sqrt{E}}{k_b T}\right) \tag{4.27}$$

Here η is a fitting parameter. The first term $\exp\left(\frac{-e\phi_0}{k_b T}\right)$ relates the dielectric charging with the properties of the dielectric (*e.g.* ϕ_0), while the second term $\exp\left(\frac{e\beta_{PF}\sqrt{E}}{k_b T}\right)$ includes the stress intensity (E).

Yuan's and Goldsmith's model of charging controlled by transient current

Another attempt to correlate the kinetics of dielectric charging with the electric properties of the dielectrics have been done by Yuan and Goldsmith and it is presented in [97, 98, 105, 106]. In these papers the amount of the trapped charge is evaluated by analyzing the charging and discharging transient currents.

The injected (and trapped) charge Q_t is assumed to be equal to:

$$Q_t = \sum_J Q_t \left[1 - \exp\left(-\frac{t_{down}}{\tau_C^J}\right) \exp\left(-\frac{t_{up}}{\tau_D^J}\right)\right] \tag{4.28}$$

Here, t_{down} is the charging time, t_{up} is the discharging time, τ_C^J is the charging time constant and τ_D^J is the discharging time constant. The transient currents due to charging I_C and discharging I_D are respectively:

$$I_C = eA_{el}\frac{dQ}{dt} = eA_{el}\sum_J \frac{Q^J}{\tau_C^J} \exp\left(-\frac{t_{down}}{\tau_C^J}\right) \tag{4.29}$$

$$I_D = eA_{el}\frac{dQ}{dt} = eA_{el}\sum_J \frac{Q^J}{\tau_D^J} \exp\left(-\frac{t_{up}}{\tau_D^J}\right) \tag{4.30}$$

Based on this assumptions, the voltage drift rates are calculated and they turn out to be well fitted by an exponential dependence.

Discussion
These two models are the most advanced and the most promising ones for practical purposes of predicting switch lifetime. The intention for developing these two models was not only to predict the long term behavior of MEMS switches, but also to understand the physics of the trapping in the dielectric, which is critical for improving the switch reliability.

The main advantage of the model proposed by Melle is that it tries to correlate the voltage drifts measured for the switches, with the switch design (thickness of the dielectric, electrode spacing) and the electrical properties of the dielectrics which had been used. Consequently, this model could be theoretically used to investigate the impact of potential modifications of switch design and materials selection on the drift of the pull-in voltage, without the necessity of fabricating complete switches.

The model proposed by Yuan and Goldsmith uses a different approach compared to the Melle's model, but it still correlates the pull-in voltage drifts, measured for MEMS switches, with the physical properties of the dielectrics used. Contrary to the Melle's model, here it is not obvious how to investigate the impact of the switch design on the behavior of the switches.

Both models have a common drawback, which is the fact that each of them contains fitting parameters. Consequently it is not possible to use them for a priori modeling of switch behavior, based solely on the dielectric properties of the insulators used.

Moreover the model proposed by Melle produces unrealistically high voltage drift rates for RF MEMS switches of the order of hundreds V/min, which are not realistic if one analyzes the switch behavior in the time frame of several hours of a voltage stress.

4.3.3 Proposed time-dependent charging model

In this part we present our own model of charge-trapping in the dielectric layer of capacitive- and ohmic-type RF MEMS switches. This model uses the dielectric properties, which have been extracted in the previous chapter to model the voltage drift of the RF MEMS switches.

General approach
The approach which has been used to calculate the drift of the pull-in voltage in RF MEMS switches is presented below.

In is considered in the proposed model, that during a voltage stress a parasitic charge is trapped in the dielectric, which reduces the electric field in the dielectric. To compensate this drop of the electric field, that is to maintain at a constant level the electric field in the dielectric in an RF MEMS switch, it is necessary to apply a higher voltage. Consequently the change of the pull-in voltage is considered to be equal to the reduction of the electric field due to the trapped charge.

The model of charge accumulation as a function of time for a constant applied voltage V_{app} is based on the Wibbler's model, where the reduction of the electric field in the dielectric ΔE due to the amount of charge Δn_t trapped during a period of dt is given by the equations 4.16. For our purposes, this equation can be rewritten in the following simplified form:

$$\Delta E = \int_0^t \frac{e}{\epsilon_0 \epsilon_r} \left(1 - \frac{\bar{x}}{t_d}\right) v_t dt \tag{4.31}$$

In this equation v_t is the trapping rate $v_t = \frac{dn_t}{dt}$ and it depends on the nature of the trapping

kinetics.

In practice, the model of charge trapping in the dielectric layer of a switch as a function of time and voltage stress is an iterative numerical model which is calculated according to the algorithm presented in the Figure 4.6.

In each iteration the amount of trapped charge Δn_t over a period of Δt is calculated. This trapped charge is assumed to reduce the initial electric field E_{s_0} by a value of ΔE_{s_i}. Detailed description of each iteration is provided below:

1. *Definition of the nominal voltage stress E_d*
   At the beginning we define the nominal electric field corresponding to the applied voltage stress, which is calculated as follows $E_d = V_{app}/t_d$.

2. *Initialization of variables Δt, t_{end}, t_0 and ΔV_{pin}*
   In this step we set the time increment Δt, the total stress time t_{end} and we are initializing t_0 and ΔV_{pin} variables.

3. *Calculating the effective electric field is a switch dielectric*
   For the same applied voltage and thickness of the dielectric, the electric field in a switch is lower compared to a MIM-structure. The effective electric field in a switch is obtained from the ratio of switch capacitance to MIM-structure capacitance, using the following formula: $E_s = E_d C_s / C_d$

4. *Determination of current density J_{inj}*
   In the first step of the iteration we determine the density of the injection current, which corresponds to the effective electric field E_{s_i} and which is obtained from the models of conduction.

5. *Determination of trapping parameters, that is the concentration of available traps N_{t_i} and the capture cross-section σ_i*
   In the second step of the iteration we determine the concentration of available traps N_{t_i}, which is reduced with each iteration by the already trapped charge and the effective capture cross-section σ_i. The concentration of traps N_{t_i} shows weak field dependency for MF SiN_x or it is constant for HF SiN_x and MF SiO_2. The effective capture cross-section is field dependent for both SiN_x or constant for SiO_2.

6. *Calculation of charge trapped during a single iteration*
   In the second step we calculate the amount of charge n_{t_i} trapped over a period of time Δt, which is obtained from the equations 3.33 and 3.34 for the exponential first order trapping model and the equations 3.38 and 3.39 for the logarithmic repulsive trapping model.

7. *Field reduction due to trapped charge ΔE_i*
   In the third step, the reduction of the electric field due to the trapped charge is calculated ΔE_{s_i} which corresponds to a voltage shift ΔV_{pin_i}

8. *Calculation of new effective electric field across the dielectric $E_{s_{i+1}}$*
   In the fourth step of the iteration we calculate the effective electric field across the dielectric $E_{s_{i+1}}$ which is equal to the previous value of the electric field E_{s_i} reduced by the value of E_{s_i} due to the trapped charge.

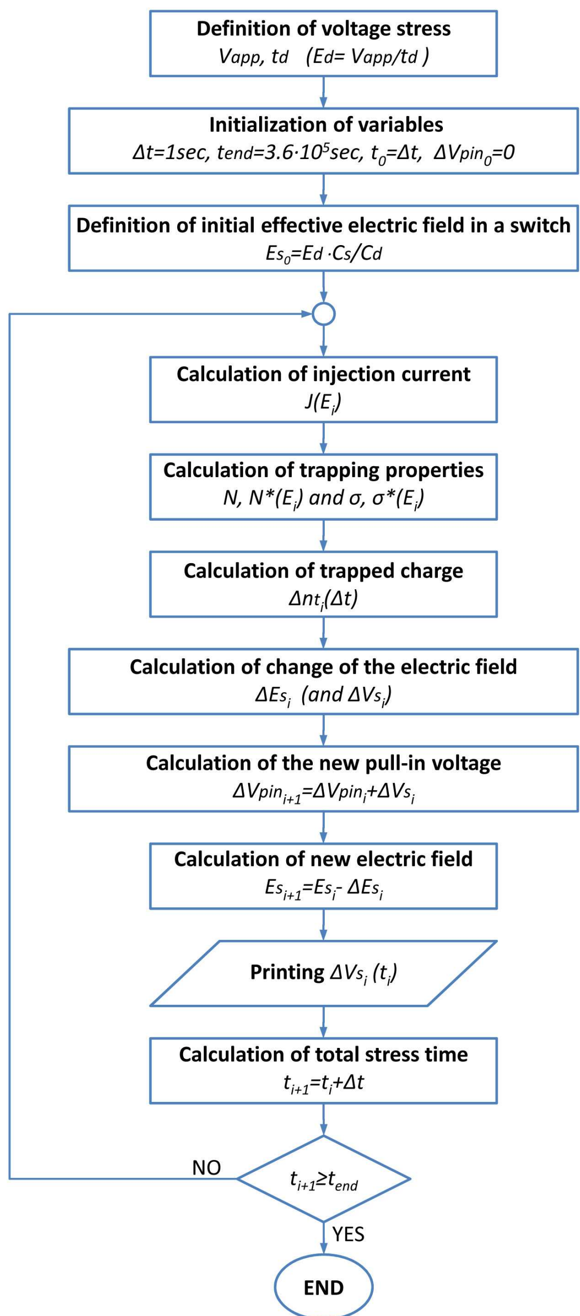


Figure 4.6: Algorithm used to calculate the drift of the pull-in voltage.

9. *Calculation of total time of charging* t_i
   In the last step of the iteration, the total charging (stress) time is calculated t_{i+1}. If the total stress time is equal or exceeds the set end value of the stress time t_{end} the calculation is stopped.

To sum up, the dielectric properties, which are required as the input parameters in this model are the injection current J_{inj}, the trapping properties N_t (N_t^*) and σ (σ^*) and the position of charge centroid $\bar{x}$ which have been determined in chapter 3, for three investigated dielectric materials.

4.3.4 Definition of input parameters

4.3.4.1 Definition of effective electric field

Before calculating the voltage drifts it is necessary to calculate the initial effective electric field in the dielectric of the switches.

Figure 4.7 presents the effect of the reduction of the electric field in the RF MEMS switches. In this figure, we can see the J-E curves measured on a MIM-capacitor and a capacitive-type switch with HF SiN_x. When we look at the raw J-E measurements we can see that the curve measured for a MIM-capacitor does not overlap with the one measured for the switch. The reason why it is so is that the electrostatic force necessary to close the switch depends on the voltage which is applied between the actuating electrodes. The electric field in the dielectric results from this applied voltage and the geometry of the sample, that is the air-gap in the closed state and the thickness of the dielectric. From a practical point of view the value of the electric field in the dielectric has no influence on the functioning of the device.

The effective electric field in the switch E_s can be obtained from the equation 4.3 as a ratio between the normalized capacitance of a switch and a MIM-capacitor. By taking into account this modification of the electric field in a switch, the J-E curve measured for the switch can be replotted, so that the J-E curves for the MIM-capacitor and the switch do overlap.

The only difference between these two curves are two peaks observed on the J-E curve. The first peak, which is denoted as 1 in Figure 4.7, corresponds to the closure of the switch. The second peak, denoted as 2, corresponds to the collapse of the beam outside the dielectric onto the surface of the substrate.

From this figure it is clear that the mechanism of current transport across the dielectric is the same in the MIM-capacitor and in the switch.

4.3.4.2 Selection of conduction model for definition of J_{inj}

The first of the input parameters is the injection current density J_{inj} which depends on the electric field and which is controlled by the type of the conduction mechanism present in each dielectric. The injection current density determines the amount of injected charges N_{inj} into the dielectric for a specific electric field.

The value of the leakage current may be more than one decade higher for the same voltage, for the ramp-up and ramp-down, which is why the selection of the model of the injection current

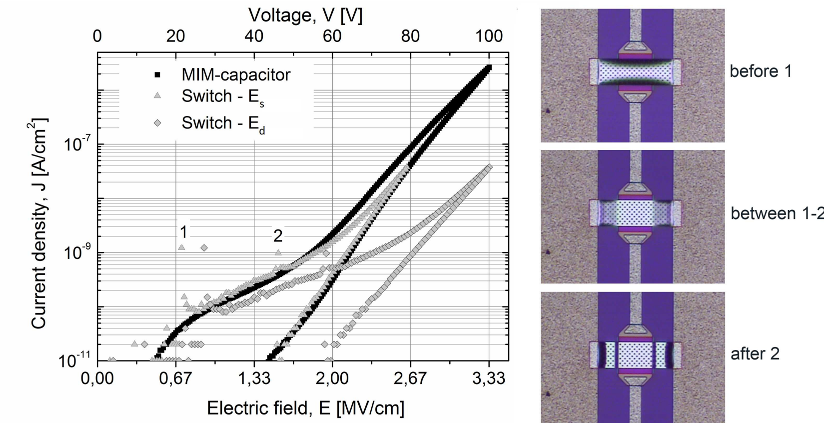


Figure 4.7: Reduction of electric field in RF MEMS switches due to asperities on contacting surfaces (capa.B HF SiN_x).

is important for the proposed model. In this paragraph we decide which value of the injection current is relevant.

In Figure 4.8 we present the theoretical voltage drifts, calculated for the ramp-up and ramp-down, as obtained form the I-V measurements (0-100 V).

It turns out that the choice of the model of injection current has a significant influence on both the value of the maximum voltage drift and the kinetics of accumulation of the parasitic charge. Apparently, the higher current from the 1st ramp-up results in a much faster filling of traps, compared to the ramp-down.

The model, which seems to be more relevant for the calculations of the charge build-up is the model of the ramp-down. As it has been demonstrated in the previous chapter, the ramp-down part of the I-V curves remains almost parallel, when comparing I-V curves for different maximum voltages and different materials. These shifts of the I-V curves are related to the charge trapped in the dielectric, which has a serious implication for modeling of the injection current. But the measured ramp-down parts of the I-V curve are already shifted towards higher voltages (for positive voltage polarity) due to the trapped charge which happens in the first I-V curve. As a consequence the ramp-down for the true injection current (before the parasitic charge is trapped) is shifted towards the lower electric fields, when compared to the measured ramps-down. This true ramp-down is then used to define the initial injection current J_0. The position of this original ramp-down I-V curve with no trapped charges remains unknown, which is the main weakness of the proposed model.

In our case, we propose to find the initial I-V curve, by shifting the ramp-down of the measured I-V curves by a single value of ΔV_c, which is found by fitting the experimental voltage drifts (for all stress voltages) with our model. The I-V curve, which is found this way is considered to be the one that reflects the conduction mechanism in each of the dielectric materials, when no trapped charge is present in the dielectric. Consequently this I-V curve is shifted towards lower voltages and an example of such a shifted I-V curve is presented in Figure 4.9 where an original and shifted ramp-down curves are plotted for the capa.B sample.

The models which are used to model the injection current are those presented in the previous chapter, with the only modification being the value of the voltage, which is modified by ΔV_c as

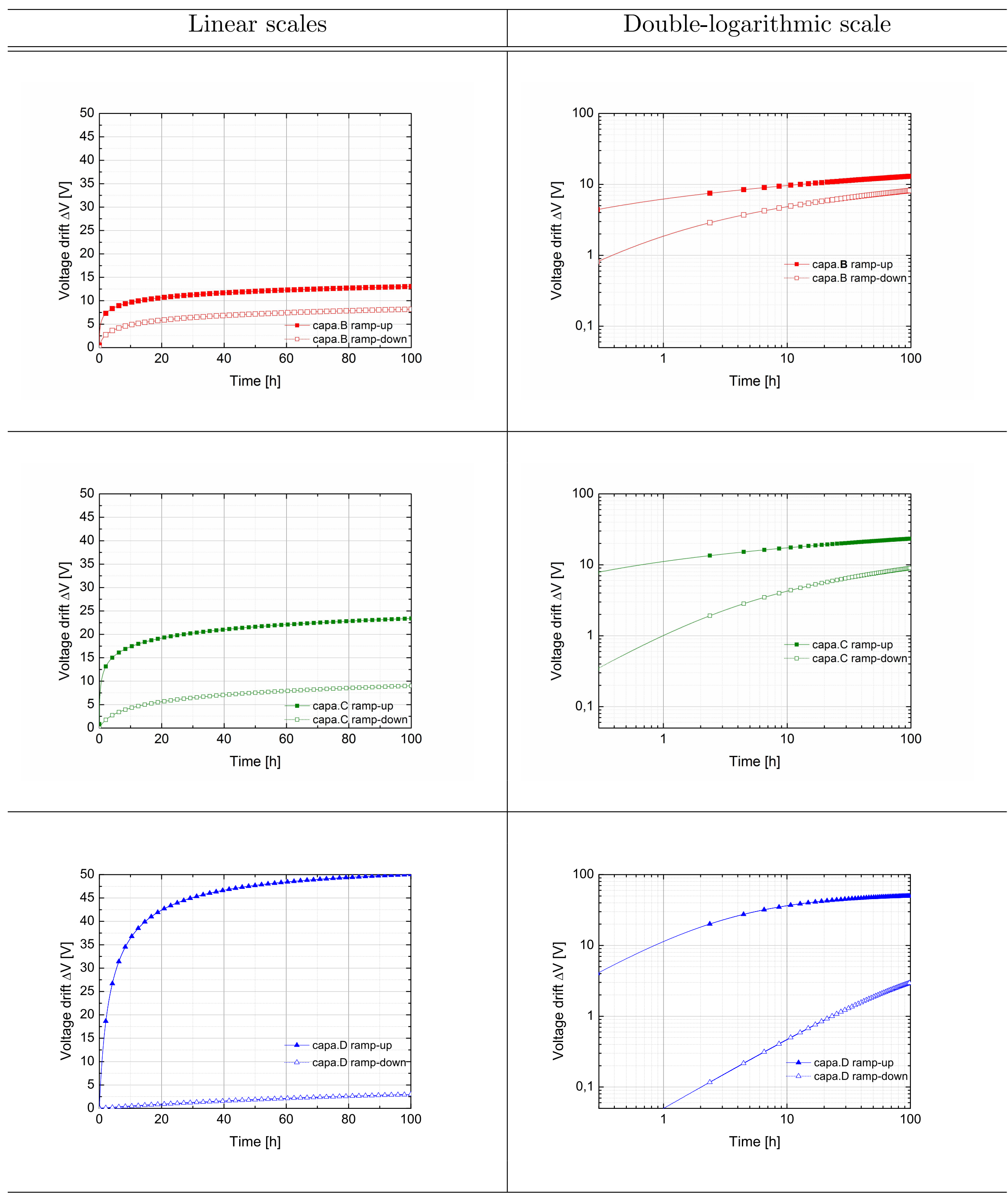


Figure 4.8: Effect of the injection current of the voltage drifts. Comparison of the ramp-up and ramp-down model of leakage current, as obtained in Chapter 3.

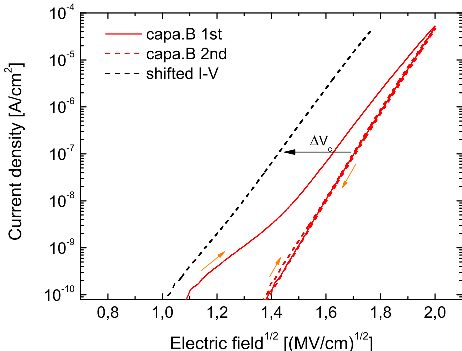


Figure 4.9: Original and shifted I-V curves for capa.B sample

presented below.

Conduction in SiN_x layers
For the HF and MF PECVD SiN_x (capa.B and capa.C) samples the leakage current is limited by Poole-Frenkel conduction, given by the model:

$$J_{inj} = J_0 \exp\left[-\frac{e\left(\phi_0 - \beta_{PF}\sqrt{\frac{V_{app}+\Delta V_c}{t_d}}\right)}{k_B T}\right] \tag{4.32}$$

Conduction in SiO_2 layer
For the MF PECVD SiO_2 (capa.D) sample the leakage current is limited by Schottky emission[1], given by the model:

$$J_{inj} = AT^2 \exp\left[-\frac{e\left(\phi_0 - \beta_S\sqrt{\frac{V_{app}+\Delta V_c}{t_d}}\right)}{k_B T}\right] \tag{4.33}$$

4.3.4.3 Definition of trapping properties

Other input parameters required in our model are the trapping properties, that is the (effective) total surface concentration of available traps N_t, which defines the maximum voltage drift and the (effective) capture cross section σ, which defines the probability of charge trapping, thus the kinetics.

The trapping properties have been identified in the previous chapter and the equations, which are used in our model are summarized below.

[1]Schottky emission was identified for the ramp-down of I-V curves; for the ramp-up the leakage current is likely likely to be space-charge-limited

SiN_x layers - logarithmic model variant

The logarithmic trapping kinetics is identified for the HF and MF PECVD SiN_x (capa.B and capa.C) samples.

For these samples the total surface concentration of traps shows weak field dependency for MF SiN_x or is constant for HF SiN_x. The capture cross-section is field dependent for both materials and it varies exponentially, as a function of the average electric field, according to equation 3.45.

The charge trapped over a period Δt is obtained from the trap rate equation for the logarithmic model of repulsive trapping, whic takes the following form:

$$\frac{\Delta n_{t_i}}{\Delta t} = J_{inj} \frac{N^* \sigma^*}{e} \exp\left(\frac{-\Delta n_{t_{i-1}}}{N^*} \right) \tag{4.34}$$

SiO_2 layer - exponential model variant

The exponential kinetics of charge trapping is identified for the MF PECVD SiO_2 (capa.D) sample.

In this material, the total trap surface concentration N_t is constant and the value of the capture cross-section σ is independent on the electric field.

The charge trapped over a period Δt is obtained from the trap rate equation for the first order exponential trapping model, which has the following form:

$$\frac{\Delta n_{t_i}}{\Delta t} = J_{inj} \frac{\sigma}{e} \left(N - \Delta n_{t_{i-1}} \right) \tag{4.35}$$

4.3.4.4 Definition of $\bar{x}$

The change of the position of the charge centroid $\bar{x}$ modifies the extracted value of the (effective) total concentration of traps N_t^*, N_t. When the charge centroid is placed closer to the air-gap the extracted values of N_t^*, N_t are lower compared to a situation the charge centroid is placed farther from the air-gap. It is important to mention, that in our case, the voltage drifts, which are calculated using the proposed model are independent of the value of $\bar{x}$, provided that the same value is used to extract the trapping parameters (N_t^*, N_t σ^*, σ) and to calculate the theoretical voltage drifts in the model of charge build-up.

4.3.5 Fitting of the experimental results

In this part we compare the experimental voltage drifts that have been measured at the beginning of this chapter with the ones which are obtained from the proposed model. In this paragraph, we simulate the voltage drifts for three dielectrics: HF PECVD SiNx (capa.B, ohm.A and ohm.C), MF PECVD SiN_x (capa.C), MF PECVD SiO_2 (capa.D) and for 2 types of switch design: capacitive- and ohmic-type.

Table 4.2 summarizes the main dielectric properties and parameters of each sample analyzed in this chapter, which are required for modeling.

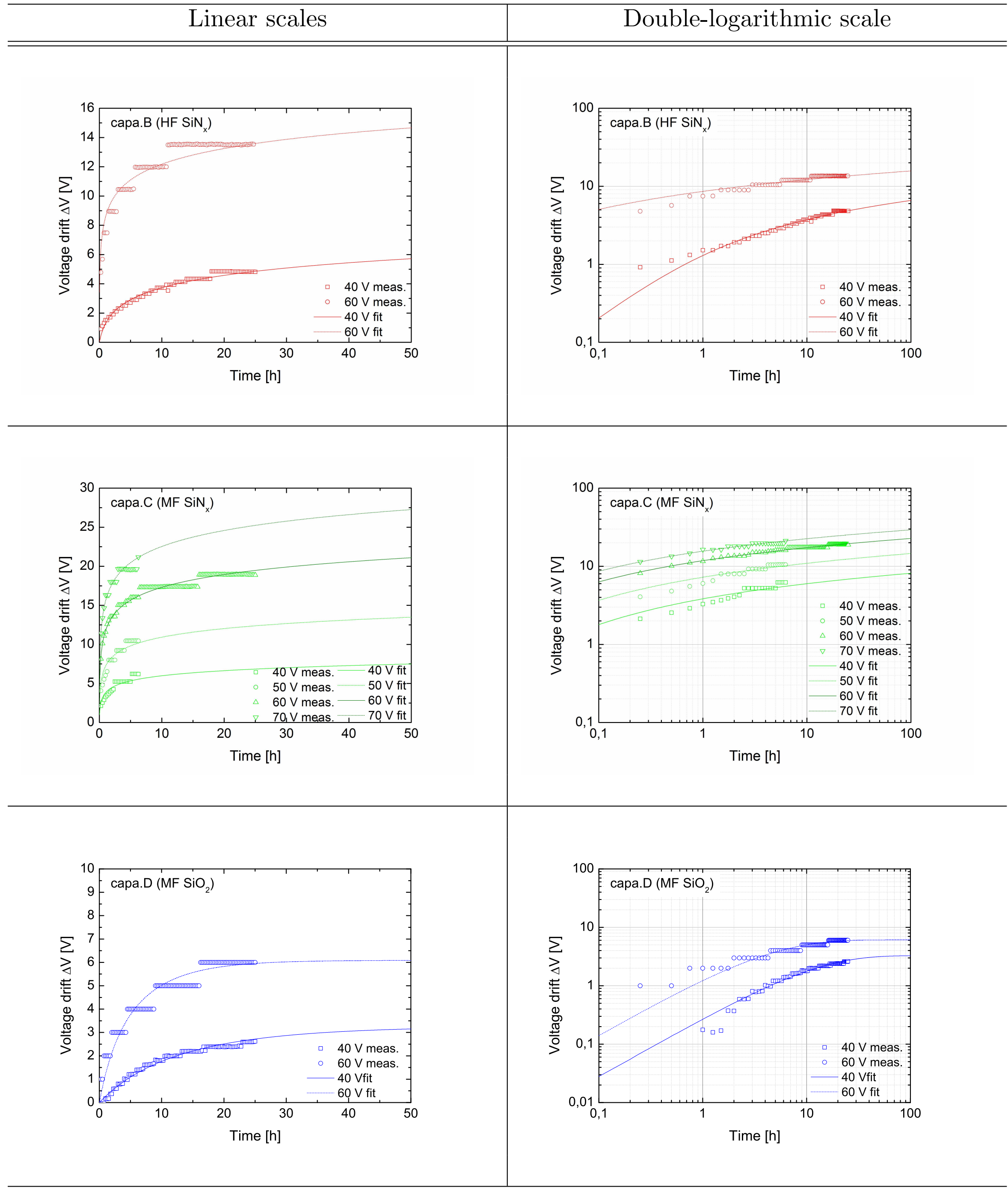


Figure 4.10: Comparison of experimental and simulated voltage drifts for capacitive-type switches.

Table 4.2: Summary of dielectric properties of HF and MF SiN_x and SiO_2

Wafer/Dielectric	t_d [nm]	Conduction mechanism	N_t or N_t^* [cm^{-2}]	σ_t or σ^* [cm^2]	E_s/E_d [% of E_0]	ΔV_c [V]
capa.B HF SiN_x	255[1]	P-F	$2.3 \cdot 10^{11}$	10^{-12}-10^{-17}	0.83	21
capa.C MF SiN_x	250[1]	P-F	$8.7 \cdot 10^{11}$	10^{-11}-10^{-15}	0.83	25
capa.D MF SiO_2	260[1]	Schottky	$1.7 \cdot 10^{13}$	10^{-15}	0.89	32
ohm.A HF SiN_x	400[2]	P-F	$2.3 \cdot 10^{11}$	10^{-12}-10^{-17}	0.55	31
ohm.C HF SiN_x	400[2]	P-F	$2.3 \cdot 10^{11}$	10^{-12}-10^{-17}	0.10	31

[1] verified
[2] not verified

4.3.5.1 Capacitive-type switches

Figure 4.10 presents a comparison of the experimental and simulated voltage drifts for capacitive-type switches.

As it has been mentioned before, the ramp-down of the J-E curve has been shifted by a value of ΔV_c so as to render possible to fit the voltage drifts for all stress levels for one switch with the same initial J-E curve. It is remarkable that a single shift of the measured J-E curve allows us to recover the full set of the experimental voltage drift curves. This strongly supports the hypothesis that this approach is correct.

The simulated results for all three dielectric remain in good agreement with the experimental ones, both in terms of the maximum value of the voltage drift and the kinetics of charge build-up. The observed discrepancies at short charging times are due to inaccuracy of determining the conduction mechanism and the trapping properties.

Analyzing the samples with SiN_x layer, the capa.B HF Sin_x sample shows lower maximum voltage drifts than the capa.C MF SiN_x, which is the expected result if we take into account the fact that the surface trap concentration for the capa.C sample turns out to be higher. On the other hand, it is worth noticing that the higher voltage drift for the capa.C MF SiN_x sample is observed, despite the fact that the injection current is lower for this sample.

Such outcome is not allowed by the model proposed by Melle, where the samples with higher leakage currents would exhibit higher voltage drifts. Our experiment shows that this is not true, as the capa.B sample which has higher injection current shows lower voltage drifts compared to the capa.C sample.

This demonstrates, that lower voltage drifts can be obtained despite higher leakage current because of two reasons. The first one, is the lower effective concentration of traps in the capa.B, compared to the capa.C sample, which limits the maximum voltage drift. The second one is the lower capture cross-section, that is a lower probability of charge trapping and consequently a lower efficiency of trapping the injected charge. It can be concluded, that the correct approach for modeling the voltage drifts in RF MEMS switch cannot be limited to analyze the leakage current only but it has to be completed by the analysis of the trapping properties.

The measurements for the capa.D sample show lower voltage drifts compared to the samples with SiN_x despite relatively high total surface trap concentrations determined for this sample. These results prove that the total surface concentrations of traps extracted from the logarithmic and exponential models are not directly comparable, as in the case of the SiO_2 the maximum

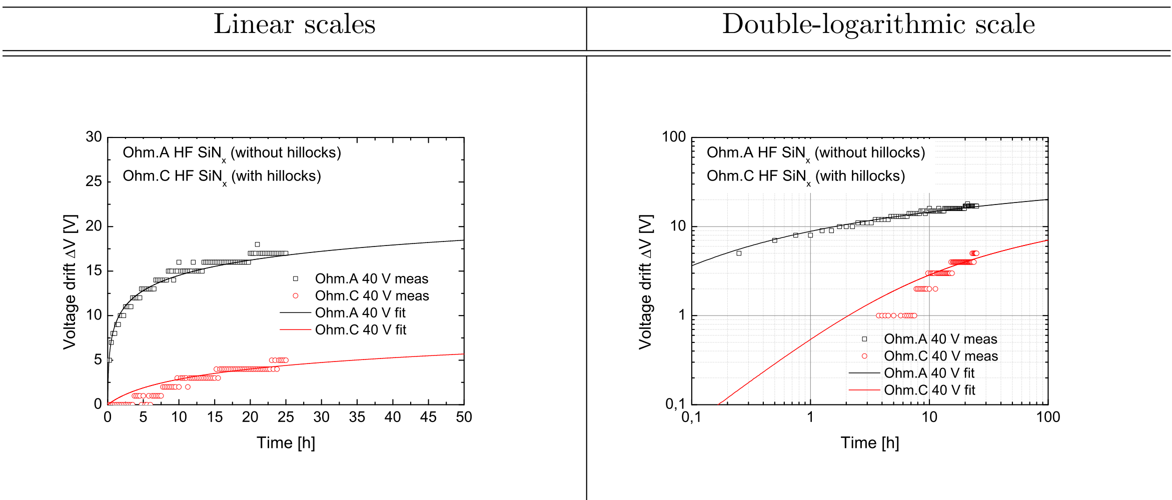


Figure 4.11: Comparison of experimental and simulated voltage drifts for ohmic-type switches.

voltage drifts are lower compared to the samples with the SiN_x samples, where the absolute value of the N_t^* are lower than for SiO_2.

As the experimental and modeled results show no or little discrepancy, for both logarithmic and exponential models, it can be concluded that the proposed general approach to calculating voltage drifts in RF MEMS switches under constant voltage stress is appropriate and the use of the shifted ramp-down of the I-V curves is relevant.

What is more, the model demonstrates, that it is possible to model the long term behavior of RF MEMS switches (the evolution of the voltage drifts) based on the physical properties of the dielectric layers which have been used. It also shows that the pull-in voltage drifts are not only dependent on the leakage current but also on the trapping kinetics. In particular, samples with lower leakage currents (for a given electric field) may show higher voltage drifts, due to higher number of available traps.

4.3.5.2 Ohmic-type switches

To simulate the voltage drifts for the ohmic-type switches the properties of the HF PECVD SiN_x extracted for capacitive-type switches are used, with the only modification being the shift of the I-V curve, which had to be adjusted for these simulations, due to different thickness of the dielectric in the capacitive-type and the ohmic-type switches.

Figure 4.11 presents a comparison of the simulated and experimental results for the ohm.A and ohm.C samples.

As in the case of the capacitive-type switches, the voltage drifts are rather well fitted with our model. The experimental results show that there is a strong effect of the switch design on the accumulation of charge in the dielectric layer.

The voltage drifts for the ohm.A and ohm.C switches, which uses the same dielectric layer and where the same stress voltage V_{app} is applied, are significantly different. The ohm.A wafer with no hillocks exhibits higher voltage drifts than the ohm.C wafer with hillocks. As it has been demonstrated earlier in this chapter, the lower spacing between the electrode and the dielectric

results in a higher electric field in the dielectric, for the same applied voltage. In case of these two samples, this spacing depends on the roughness of the electrode. Consequently, the electric field in the dielectric of the ohm.A sample is much higher compared to the ohm.C sample, when the same nominal voltage is applied. It can be concluded that increasing of the air gap between the electrode and the dielectric, in the closed state, which contributes to a significant reduction of the electric field in the dielectric, results in significantly lower injection current density and produces in turn slower voltage drifts.

4.3.6 Discussion of the proposed model

The previous section showed that the proposed model can be effectively used to simulate the drifts of the pull-in voltage for the electrostatic RF MEMS switches, for both the capacitive- and the ohmic-type, provided that the conduction mechanism model and trapping properties of the dielectric materials are known. In the following section we use this model to investigate how the material properties (trapping properties) and switch design (effective electric field, concentration of available traps) influence the voltage drifts.

Effect of trapping properties

The paragraph below presents the effect of the trapping properties on the voltage drifts. It helps understanding how the dielectric properties influence the kinetics of charge build-up in the dielectric and how it translates for voltage drifts observed for RF MEMS switches.

Effect of total concentration of traps (N_t^*, N_t)

In this section the influence of the total surface charge concentration on the voltage drifts is investigated. The concentration of traps varies in the range of the 0.25-4 of the nominal value, which has been used to calculate the results for 60 V constant voltage stress.

The results of these simulations are presented in Figure 4.12.

From this figure it is clear that the total surface concentration of traps has a significant influence on the maximum values of the voltage drifts for all investigated dielectric materials.

When the value of N_t^* is varied for the SiN_x dielectric layers (the capa.B HF SiN_x and capa.C MF SiN_x samples) it changes the maximum value of the voltage drifts as there is less or more traps to be filled. In the double logarithmic scale, the variation of the N_t^* is visible as a vertical offset of the plotted drifts and there is hardly any change of the slope visible. Qualitatively, this effect is similar for both samples with SiN_x layers.

Comparing the SiN_x materials, it turns out that the higher voltage drifts are obtained for the capa.C sample with MF SiN_x which has higher initial surface trap concentration.

When the value of N_t is varied for the SiO_2 dielectric (the capa.D sample), the effect is similar to that observed for the SiN_x samples. The number of traps has a major effect on the maximum value of the voltage drifts and it has no influence on the kinetics of charging, as expected.

Effect of capture cross-section (σ^*, σ)

Here the influence of the capture cross-section concentration on the voltage drifts is investigated. This capture cross-section varies in the range of the 0.25-4 of the nominal value.

The results of these simulations are presented in Figure 4.13.

Compared to the effect of (N_t^*, N_t) the variation of the capture cross-section produce less significant changes in the modeled voltage drifts.

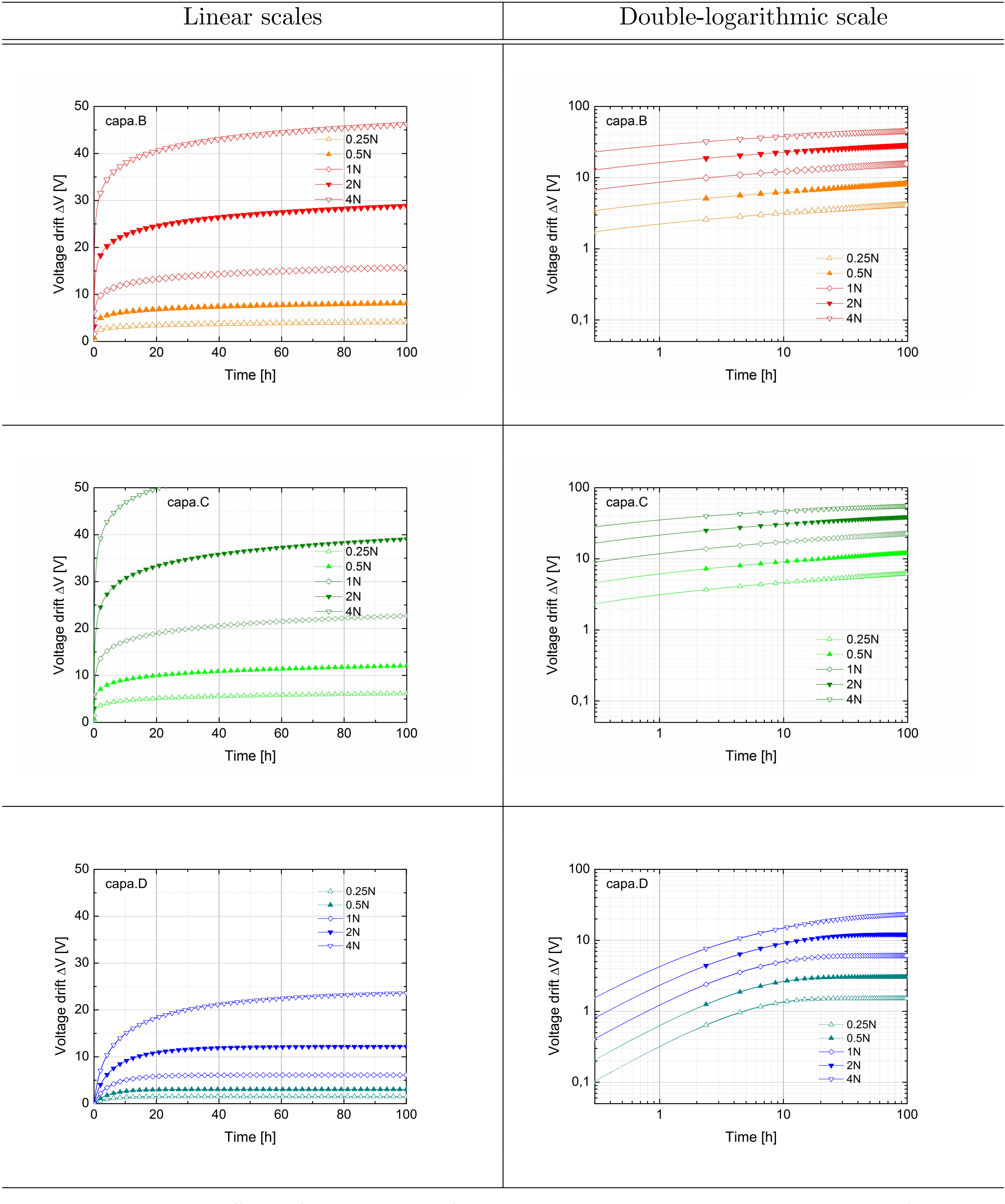


Figure 4.12: Effect of the total surface trap concentration on the voltage drifts.

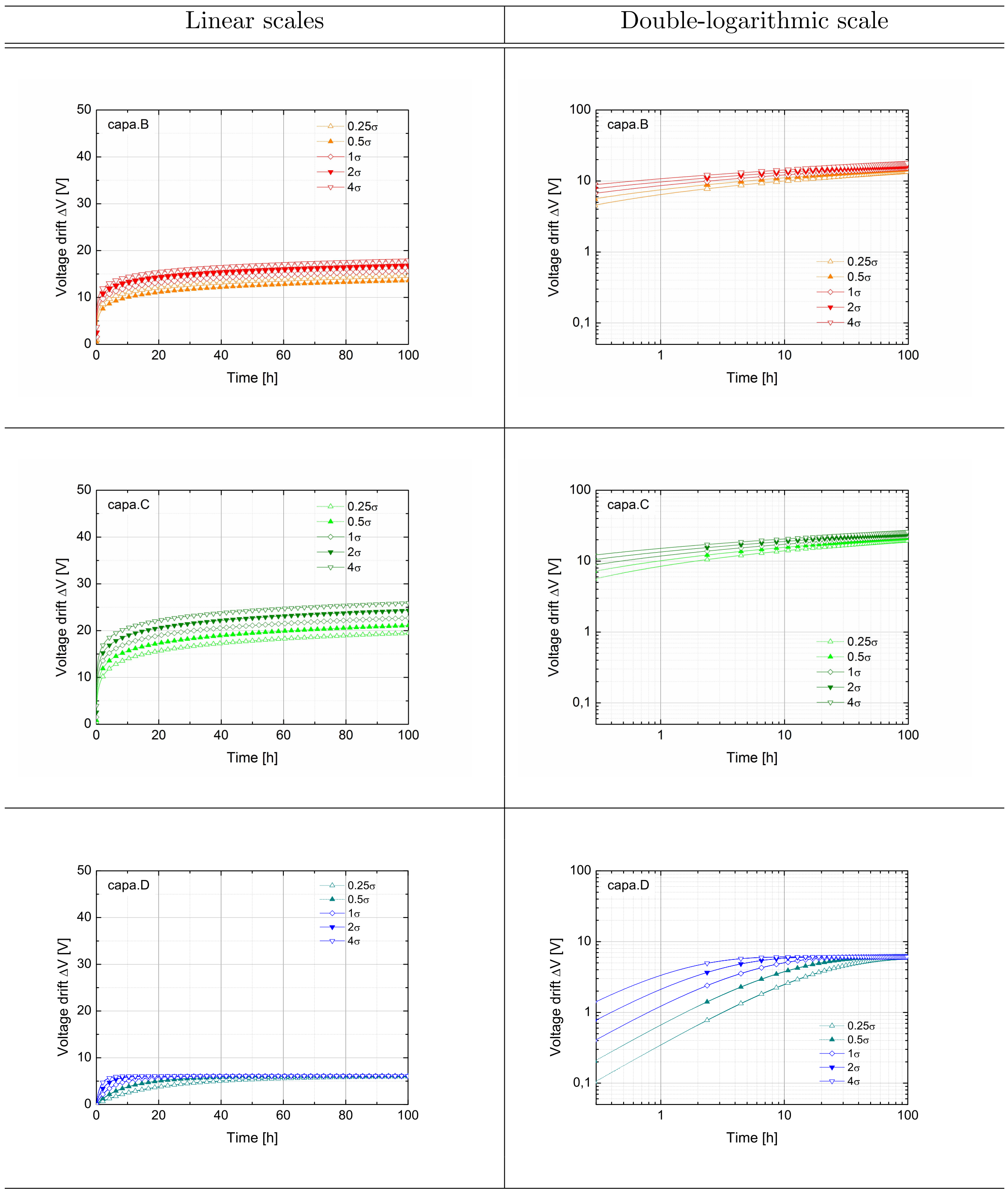


Figure 4.13: Effect of the capture cross-section on the simulated voltage drifts.

The capture cross-section reflects is the probability of trapping of the injected charge. Consequently, it should not change the maximum voltage drifts but only modify the kinetics of filling the traps.

In case of the capa.B and capa.C samples with SiN_x, the change of the value of σ^* has a minor effect on the kinetics of charge trapping and on the maximum voltage drift, compared to the effect of the total concentration of traps. In the time scale relevant for the RF MEMS switches it turns out that the increase of the value of σ^* slightly increases the maximum voltage drift. The higher values of σ^* signifies higher trapping probabilities, that is more traps are filled and the corresponding drifts are higher. Because, in the time scale used here the traps are not saturated the effect of the capture-cross section gives impression of the increase of the maximum voltage drift. All in all, compared to the effect of the total surface concentration of traps N^* on the voltage drifts, the capture cross-section has minor influence on it.

In case of the capa.D sample with SiO_2, the effect of varying the σ is much better visible than in case of the samples with SiN_x. In the exponential trapping the variation of σ determines how fast the available traps are filled and the higher the value of σ the faster the traps are filled (modified kinetics). In exponential trapping, this parameter has almost no influence on the maximum value of the voltage drift in the presented time scale, where is possible to observe the saturation voltage (when all available traps are filled) for all investigated σ.

Effect of switch design

The parameters that have been analyzed before depend on the properties of the dielectric materials. On the other hand the switch behavior can be modified by changing the design. The changes, which are relevant from the point of view of accumulation of the trapped charge in the dielectric, are those which have an influence on the effective field in the dielectric.

To investigate the impact of the switch design, in this section we present the effect of the electric field E_s across the dielectric in a switch, and the thickness of the dielectric t_d.

The electric field in the dielectric depends primarily on the applied voltage V_{app}, the thickness of the dielectric t_d and its dielectric constant ϵ_r and the residual air-gap between the dielectric and the electrode in the closed state.

The thickness of the dielectric t_d can be easily controlled during the deposition and a higher thickness results in lower electric field. For the purpose of modeling, the higher thickness of the dielectric is also assumed to have an impact on the concentration of available traps where thicker dielectrics are assumed to have proportionally higher trap concentrations.

Effect of electric field E_s in the dielectric in a switch

The influence of the electric field E_s on the voltage drifts is investigated in the range of 0.5 - 1.5 of the nominal value, which have been used to fit the experimental results for 60 V constant voltage stress. The results of this simulations are presented in Figure 4.14.

The modeled voltage drifts confirm that the electric field has a significant influence on both the maximum value of the voltage drift as well as the kinetics of charge trapping. It is apparent from these figures, that the higher electric field leads to faster and higher pull-in voltage drifts. This simulation confirms the observation from the first part of this chapter, where it has been demonstrated, that the electric field (applied voltage) can be used as a acceleration factor for the constant-voltage stress tests.

The effect of the electric field can be explained by the fact that modification of the electric field results in a modification of the injection current, which determines the number of charges

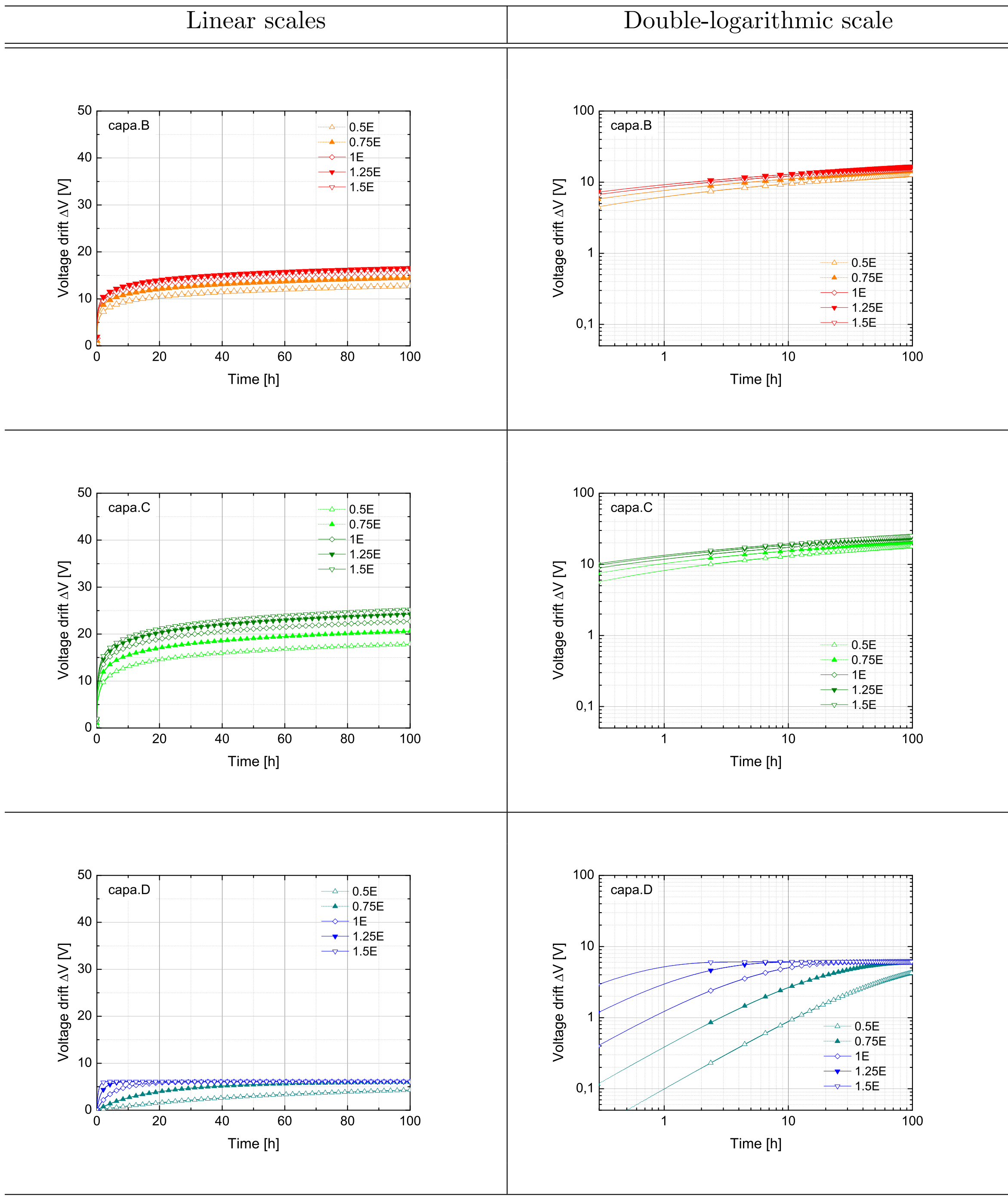


Figure 4.14: Effect of the effective electric field in the dielectric on voltage drifts.

that can be potentially trapped. Consequently, for lower electric fields, the injection current is lower and less charges are injected and trapped. In case of SiN_x, where the trapping properties are field dependent, the lower injection current is compensated by higher capture cross-section. Practically, it means that despite the fact that less charges are injected and then available for trapping, they are more efficiently trapped. This is why, the effect of the electric field is less visible for the SiN_x compared to the SiO_2, where the trapping properties show weak dependency on the electric field. In case the trapping parameters are not field-dependent lower electric field results in slower kinetics and slower voltage drifts, which is the case of the SiO_2. For this material the maximum drift is limited by the number of available traps, which are filled slower if lower for lower electric fields. This can be explained by the fact, that for lower electric fields the injection current is lower and so is the amount of charges available for trapping. Because the probability of capturing these available traps is constant, if less charges are available less charges are trapped. It is worth mentioning that also a relative increase of the injection current with increasing electric field, is slower in the SiO_2 dielectric compared to SiN_2.

Consequently, any modification of the switch design may have a different effect on the long term behavior of a switch depending on the material type, which is used.

Effect of dielectric thickness t_d

The influence of the thickness of the dielectric t_d on the voltage drifts is investigated in the range of 0.5 - 1.5 of the nominal value. In this simulation it is considered that a thicker material has proportionally more traps available. The total surface concentration of traps is varying along with the thickness of the dielectric, in such a way that a dielectric of 0.75 of the nominal thickness is considered to have the total surface concentration of traps equal to 0.75 of the nominal one, while the electric field in the dielectric will be increased to 1.33 of the nominal one due to the lower thickness and a fixed value of the applied voltage.

The results of this simulations are presented in Figure 4.15.

The analysis of the effect of the thickness of the dielectric on the voltage drifts is not so straightforward compared to the other parameters, because in this simulation two parameters are changed simultaneously. Here not only the electric is changing (due to different thickness of the dielectric) but also the total concentration of traps.

For the capa.B and capa.C samples with the layer of SiN_x we can see that varying t_d leads to a relatively small change of the kinetics of charge trapping, but it changes the maximum value of the voltage drift, which is controlled by the total surface concentration of traps N_t^* and not by the injection current, which is field-dependent. As a result, for a lower thickness when the electric field in the dielectric is higher, despite the higher injection current which passes through the dielectric, less traps are available and the maximum voltage drift is lower. What is more, in the layers of SiN_x for higher electric fields, the probability of trapping decreases, which further contributes to lowering of the voltage drifts.

For the capa.D samples with SiO_x the observed effect is slightly different when compared to the SiN_x sample, as not only the maximum voltage drift is modified but also the kinetics. For this sample, the trapping parameters are not field-dependent.

When the thickness is reduced, the total surface concentration of traps is reduced accordingly, which results in the reduction of the maximum possible voltage drift. On the other hand, when the thickness is reduced, the injection current increases, which means that more charges can be trapped. Because the probability of trapping the injected charge is constant, regardless the electric field, when more charges are injected in a period of time, more charges are trapped. To

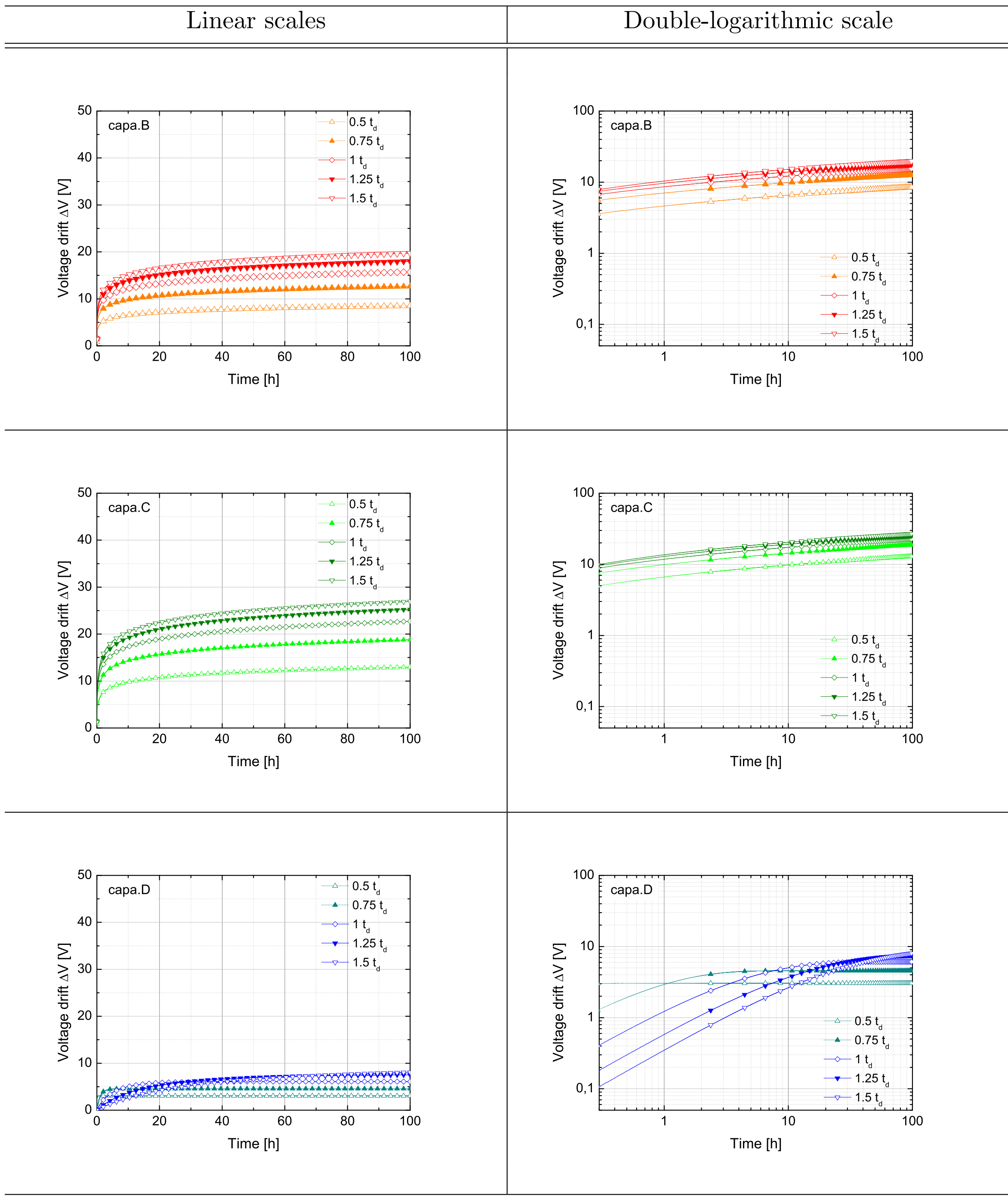


Figure 4.15: Effect of the thickness of the dielectric on the voltage drifts.

sum up, when the thickness of the SiO_2 is reduced it produces in turn in the long-term lower voltage drifts because of lower concentration of traps. The voltage drifts rates will be higher because the available traps will be filled faster due to higher injection current. These are the reasons, why the simulated curves intersect.

4.4 Conclusions

In this chapter the long term behavior of RF MEMS switches with three types of PECVD dielectrics and of two different designs have been analyzed. The investigated dielectrics included high- and mixed-frequency PECVD SiN_x deposited at 300°C and mixed-frequency PECVD SiO_2 deposited at 150°C. The variants of the switch design have been examined for ohmic-type switches with and without hillocks.

At the beginning of this chapter it has been demonstrated that the drift of the pull-in voltage is a lifetime-limiting factor for the RF MEMS switches. The voltage applied across the actuation electrodes creates a high electric field in the dielectric, which causes parasitic charge build-up. This parasitic charge generates a parasitic screening force between the actuation electrode, which changes the initial pull-in voltage. The presence of the parasitic charge in the dielectric is seen as a shift of an initial C-V curve of an electrostatically actuated MEMS switch. When the voltage stress is as high as it is possible so that the pull-in voltage V_{pi} exceeds the applied voltage V_{app} and the switch cannot be closed, thus it is not operational any more.

The measurements of voltage drifts have been carried out on capacitive- and ohmic-type switches and show that all the investigated samples are affected by the problem of the dielectric charging. The measured voltage drifts turned to be dependent on the constant voltage stress level (higher stress leads to higher drift) and switch design. The reliability tests in RF MEMS switches can be then accelerated by increasing the magnitude of the voltage stress, but the maximum applicable voltage stress is limited be the dielectric strength. For capacitive-type switches, higher voltage drifts are observed for the devices with SiN_x layers rather than SiO_2.

Analysis of the ohmic-type switches reveals that the switch geometry and more specifically the spacing between the top and bottom electrode in the closed state, may have a significant influence on the measured voltage drift rates, which is related to the effective electric field in the dielectric and lower effective contact (injection) area between the electrodes. A larger air gap in the down-state corresponds to a lower effective electric field in the dielectric, which results in lower injection current and slower charge build up and voltage drift. This is confirmed by the observation that higher voltage drifts are observed for ohm.A samples with smoother surface of electrode.

The presented model of a charge build-up in a switch for a constant voltage stress has been positively verified. The experimental and modeled results showed no or little discrepancy. It can be than concluded that the voltage drifts measured for MEMS switches depends on the properties of the dielectric and the switch design. The properties of the dielectric that have an impact on the voltage drifts are injection (leakage) current combined with the trapping properties, that is total number of available traps and the capture cross section. The injection current together with the capture cross-section define the kinetics of charge trapping, while the total concentration of traps defines the saturation drift voltage.

Chapter 5

Conclusions

This thesis summarizes the work concerning reliability testing of electrostatic capacitive- and ohmic-type RF MEMS switches developed by the CEA-Leti in collaboration with industrial partners.

The first experimental chapter explains how the electric behavior of the RF MEMS switches depends on their design, that is their geometry and material properties. To achieve this goal, the first part presents an original mechanical model used to calculate the stiffness of the ohmic-type switches, with two side electrodes. The model is validated, by comparing theoretical (calculated) values of the switch stiffness for four wafers of ohmic-type switches, with the values obtained experimentally by nanoindentation technique.

In the next step, the mechanical model is used to analyze the impact of geometry (the width and the thickness of the switch) and the material properties (the residual stress) on the value of the nominal switch stiffness. It is demonstrated that none of these parameters has a stronger impact on the switch stiffness when varied in the range of 0.5-1.5 of the nominal value. Nevertheless, it is important to mention that in case of the residual stress it is possible not only to have zero residual stress, but it is also possible to change from tensile (present case) to compressive stress, that is two change the sign of the stress. It turns out that the residual stress has the most critical impact on the switch stiffness. In our example, the stiffness may drop from approximately 100 N/m (nominal value) to almost 1 N/m, when there is no residual stress. It is then concluded that the mechanical properties of the materials in MEMS are of paramount importance. Consequently, when designing a MEMS device the technological process must be optimized not only to achieve required electrical properties of the materials but also the mechanical ones. This is was makes the design of MEMS a challenging task.

In the following step, the electro-mechanical behavior of the ohmic-type switches is investigated by combining the mechanical model with a common electrostatic model available in the literature. The initial electrical behavior of four wafers of ohmic-type switches is characterized. These measurements reveals that the investigated wafers exhibit significantly different behavior, in terms of the level of the pull-in voltages, the capacitance ratio and the contact resistance. To explain the observed differences, the measurements of the stiffness are completed by AFM, SEM and FIB observations to evaluate the switch geometry in terms of the state of the surface of the electrodes and contacts.

It is demonstrated that, the devised electro-mechanical model with the experimental input parameters can be successfully used to explain the electrical behavior of different wafers of the ohmic-type switches. In particular it can explain the different levels of the pull-in voltage (due

to the electrode gap and the switch stiffness), the capacitance ratio (due to the electrodes' roughness) and the switch resistance (the contact roughness due to technological process). For instance, the low capacitance ratio, resulted from high roughness of the electrodes - growth of hillocks on the gold surface, which was caused by excessive thermal treatment during processing.

The second experimental chapter presents the results of the characterization of the structural and physical properties of the dielectrics, which are typically used in ohmic- and capacitive-type RF MEMS switches (mixed- and high frequency PECVD SiN_x and mixed-frequency SiO_2). This work makes significant contribution to the research on dielectric charging in MEMS as it presents significant improvements compared to what has been reported in the literature. This is mostly due to the fact, that the investigated dielectrics in the test structures and in the fabricated RF MEMS switches are virtually the same. All test structures have the same stacking sequence, the same dielectric thickness and comparable area to the switches as they are fabricated using the same process flow. Moreover, the test structures are all integrated into one wafer with the switches. As a result, it is possible to use the experimental results obtained for the test structures to investigate the behavior of the switches, with the same dielectric layer.

The structural analyses (TEM, ToF-SIMS, etc.) are carried out on real RF MEMS switches (without bridge), denoted as airgap-insulator-metal (AIM) structures. Analyzing real MEMS makes these characterization extremely challenging, because of the small area of the investigated layers, which typically does not exceed 100x100 μm^2 and which is reducing the number of available experimental techniques.

These analyses confirm that all SiN_x samples fabricated by the PECVD technique have inferior quality compared to their high-temperature counterparts, as they are non-stoichiometric, which results in their amorphous structure (TEM). Structural analysis shows that a high quantity of hydrogen, exceeding 20 at. %, is incorporated in the bulk of the dielectric PECVD SiN_x, regardless the deposition frequency.

Contamination profiles, confirm high content of hydrogen and oxygen in SiN_x and showed presence of Al and Pt (materials used for electrodes) in the bulk of all dielectrics, which are most likely due to the particular process flow. These elements are prone to have a serious impact on the dielectric properties, which emphasizes the importance of testing the dielectric material, which is deposited using the same process as the final switches. As a general remark, similar elements are found in the SiO_2 layers, with a lower concentration of H being the only exception. All impurities are most likely introduced during the fabrication process rather than during storing or operating of the devices. It is concluded that, the difference in voltage drifts measured on the RF MEMS switches cannot be explained by the ions present in the dielectric (as these are the same for all the samples) but rather on the conduction mechanism and trapping properties, which are different.

The electrical tests are carried out using metal-insulator-metal (MIM) structures. During these tests the conduction mechanism (current-voltage dependency) and the trapping kinetics (the surface concentration of traps and the capture cross-section) are identified for the investigated layers.

The conduction mechanism are identified in PECVD SiN_x and SiO_2 by measuring I-V curves (for different bias polarity and as a function of temperature) on MIM capacitors. For both SiN_x materials, that is deposited in high- (HF) and mixed-frequency (MF) mode, the conduction process is controlled by Poole-Frenkel mechanism (bulk controlled) and the slope of the steady-state I-V curve is the same for both materials, which is in agreement with literature. Despite the same conduction process, both materials shows different leakage current levels, with the (MF)

SiN_x showing lower current (its I-V curve is shifted towards higher voltages).

For the MF SiO_2 the conduction mechanism is most likely to be controlled by Schottky emission, when judged on the basis of the measured current-voltage dependency. This result is in contrast with the conduction mechanism, typically found for the high-temperature oxides, which is Fowler-Nordheim conduction. In our case, one should note, that the maximum electric field applied during the measurement is rather low for Fowler-Nordheim conduction as typically it does not exceed 3 MV/cm, which may explain our observation.

Besides, the I-V measurements reveal that all these materials are prone to trapping parasitic charge, which is observed as hysteresis between the ramp-up and ramp-down parts of the I-V curve. It is demonstrated that the trapping of the parasitic charge distorts the initial electric field in the dielectric, which leads to a significant reduction of the leakage current. In particular the charge trapping is visible as parallel shifts of I-V curves for a specific current. This shift can be used to roughly estimate the corresponding trapped charge. This trapped charge has serious impact on the measurements of the I-V curves. In the present study, the measurement time of a single I-V curve relatively long as it takes above 1 hour to complete one measurement due to very low leakage current. Consequently, during the measurement a number of traps is filled and the electric field in the dielectric is modified. As a consequence the measured I-V curve is already shifted towards higher voltages compared to an original I-V curve, where no charge is trapped. Such an original I-V curve, is shifted towards lower voltages compared to the measured one (in case of positive bias I-V sweep). Further improvements can be made to modify the measurement technique in order to accelerate the measurements to obtain more accurate I-V curves not affected by trapped charge.

For studying the kinetics of charge trapping the MIM capacitors are used. The choice of the test devices limits the number of available techniques for studying charge trapping as no MOS analysis is possible. To identify the trapping properties the constant current injection technique is used. The (effective) total surface concentration of traps and the (effective) capture-cross section are extracted thanks to the exponential and the logarithmic models of the trapping kinetics. These trapping properties are identified for all investigated materials. It is important to mention, that such approach has been used for the first time for studying the dielectrics in RF MEMS switches.

The experiment shows, that the trapping in the PECVD SiN_x dielectrics show the logarithmic dependence most likely associated with repulsive trapping, where charge trapping is limited by the charge already trapped due to Coulombic repulsion. This mechanism leads to a logarithmic dependency of the trapped charge as a function of time and no saturation is observed (most likely dielectric breakdown will occur first). The total concentration of traps shows no field-dependence for the HF SiN_x and weak field dependence for the MF SiN_x sample. The capture cross-section is field dependent and it is decreasing with increasing field for both SiN_x samples, which is consistent with the repulsive trapping model.

The trapping in the PECVD SiO_2 shows the exponential dependence, which corresponds to a well-know first order model of trapping, where the probability of charge trapping is constant and the trapping is limited by the decreasing number of available empty traps. The total concentration of traps shows no field-dependence for the MF SiO_2 and the capture cross-section is not field dependent.

It is necessary to notice, that the absolute values of the trapping properties can be compared within the same groups of model only, as the effective total trap concentration from the logarithmic model N_t^* does not correspond exactly to that from the exponential model N_t.

The dielectric properties determined in this chapter, which include the model of the conduction current through the dielectric, the (effective) total concentration of traps and the capture cross-section are used for modeling of the voltage drifts measured on real capacitive-type and ohmic-type RF MEMS switches as presented in the following chapter.

In the first part of the last experimental chapter the voltage drifts in RF MEMS switches are measured during constant voltage stress tests over a period of 6 to 25 hours, for different voltage stress levels. These measurements cover all investigated types of material (PECVD HF and MF SiN_x and MF SiO_2), switch types (ohmic- and capacitive-type) and switch designs (with and without hillocks). Experiment shows that all samples are prone to the dielectric charging failure mode, but it turns out that the maximum values of the voltage drifts are different for different dielectric material and switch designs. A statement, which is true for all the samples is that the level of voltage stress is an acceleration factor for dielectric charging failure mode. Nevertheless, the stress level is limited by the dielectric strength of the investigated materials.

The second part of this chapter presents a brief overview of existing models of dielectric charging. This includes the static models explaining the shift and narrowing of C-V curves, which are not applicable for lifetime prediction. Second group of models are fitting functions which are used to extrapolate the voltage drifts measured on RF MEMS switches for longer times. Main weakness of this second group is the necessity of fabricating switches and the use of empirical (fitting) factors, which makes these models unsuitable for theoretical studies and does not help to explain the physical process behind charge trapping. The last group are physical models, which attempt to correlate the voltage drifts in RF MEMS switches with the dielectric properties. Nevertheless in none of the available physical models, the trapping kinetics has been used. It is then concluded, that all existing models fail to explain the measured voltage drifts in terms of physical properties of the dielectric materials and that the trapping kinetics in the dielectrics in the RF MEMS switches has not been investigated so far and included in the models.

In the third part of this chapter we propose an original approach of modeling of the voltage drifts based on the identified conduction mechanisms and trapping properties of the dielectrics. The input parameters are following:

- The injection current, that is the flux of electrons across the dielectric for a specific field, which can be trapped; this is defined by a leakage current as a function of the electric field (conduction mechanism).
- The number of traps available to be filled, defined by a (effective) total surface concentration of traps (trapping kinetics).
- The probability of trapping of the electrons flowing across the dielectric, which is defined by a (effective) capture cross-section (trapping kinetics).

We demonstrate that it is possible with our model to explain the measured voltage drifts in terms of the identified dielectric properties mentioned above. It turns out, however, that one element which requires further improvements is the method of measuring the I-V curves, as it is important to measure the I-V curve, where the leakage current is not affected by the already trapped charge. In the present work the problem of finding the original curve is solved by searching for one shifted I-V curve that can explain the voltage drifts measured for all stress levels.

After finding the original I-V curve, which is free from the effect of the trapped charge and which corresponds to a virgin dielectric layer, the proposed model is validated. It shows

remarkably good agreement with experimental voltage drifts as no or very little discrepancy is observed between experimental and modeled results, regardless the stress level, trapping model used (logarithmic or exponential) and even the switch design (capacitive and ohmic).

After being validated it is demonstrated how this model cam be used to study the effect of the dielectric properties and the switch design on the long term behavior of RF MEMS switches. The analysis of the impact of the trapping parameters reveals that the factor that has the most significant influence on the long term behavior of RF MEMS is the concentration of traps, which defines the maximum voltage drift. The remaining factors, that is the capture cross-section and the electric field in the dielectric only influence the kinetics of voltage drift, that is how fast the available traps are filled, rather than the maximum measured value of the drift.

Our model proves that the long term behavior of RF MEMS depends on the electric properties of the dielectric. It has a strong potential for being used for cost-effective assessment on the long term behavior of RF MEMS switches, depending on their design and the properties of the dielectric used. Consequently, presented work encourages to carry out further in-depth analysis of the physical process of charge conduction and charge trapping in the PECVD dielectrics, which are frequently chosen in MEMS.

First, it is possible to search for experimental methods, that could provide more accurate results in a shorter time. In presented case, more accurate results are required for identification of the conduction mechanism at low electric fields, to give an example. The quicker measurements can be useful for finding the I-V curves, with negligible amount of trapped charge or for accelerating the identification of the trapping kinetics where the constant current injections are particularly time-consuming.

It is also possible to focus purely on the identification of the physical process of conduction and charge trapping in the PECVD layers, as the electrical properties of these materials have not been studied extensively so far. In this approach, it is advised to use other experimental techniques to those presented in these thesis and most suitable test structures such as metal-insulator-semiconductor (MIS) capacitors. The scope of such research would be to understand what are the critical factors which rule the charge trapping in this type of dielectrics.

Finally, it is equally important to address the issue of the reliability of the dielectric layer itself, in terms of the minimum time to breakdown related to the amount of charge passed through the dielectric. As it has been mentioned in our case of SiN_x, which showed logarithmic dependency of charge trapping, such a breakdown is very likely to occur before the voltage drift saturates. In this case it is not the maximum voltage drift, which is the main lifetime limiting factor for an RF MEMS switch, but the breakdown of the dielectric.

On the other hand, our work can be applied and extended in a research and development phase of various devices (including MEMS), where the PECVD dielectrics are used. We propose to carry out a systematic study of the impact of the deposition process parameters and dielectric thickness on the conduction mechanisms and trapping properties as well as to analyze the scattering of these properties for the same process conditions.

At this stage our model can be used to analyze to which extent the variations during the manufacturing process may influence the properties of the dielectrics and consequently the switch behavior. These results could be then used to simulate theoretical voltage drifts in the investigated devices for specific actuation conditions and driving scheme. Having the real material data for different processes it would be then possible to choose a material and switch geometry to tune the behavior of the investigated devices by choosing the most appropriate process conditions from the very first fabrication run, which would reduce the time of design evaluation.

Finally our work, can be used during the evaluation phase of fabricated devices with mature design and technology. Our work gives hints to select the criteria that can be controlled during fabrication process in order to evaluate the quality of the dielectrics. For instance, it is possible to set a range of leakage current for a specific electric field, which is acceptable for a dielectric layer fabricated in a specific process. During fabrication this current current can be measured on a dedicated test structure included on the fabricated wafer. By analyzing the variation of the value of this current it is possible to detect process variations and implement necessary corrections at an early stage, which will lead to increased yield. In the phase of qualification of the products where accelerated tests are used (for instance higher voltage) it is possible to use our model, to translate these accelerated test results for the nominal operating conditions, as the physical phenomenon of the dielectric charging is understood.

As a general conclusion, our model of dielectric charging in RF MEMS is validated and it presents significant improvement in our understanding of the dielectric charging failure mode in the RF MEMS switches, where the PECVD dielectrics are used.

Appendices

Appendix A

Selected roughness parameters

The standard roughness parameters which are used to describe surface profiles are presented in Figure A.1 and explained in the text below.

The R_q is the root mean squared roughness, which is calculated as the square root of the mean square average of vertical distance deviations from the mean line, expressed as:

$$R_q = \sqrt{\frac{1}{n}\sum_{i=1}^{n} z_i^2} \tag{A.1}$$

, where z_i is the vertical distance from the mean line of the ith point.

The R_a is the arithmetic average roughness, which is calculated as an arithmetic average of the absolute values of the surface vertical distance deviation measured from the mean line:

$$R_a = \frac{1}{n}\sum_{i=1}^{n} |z_i| \tag{A.2}$$

The R_{max} is the maximum peak height, which is defined as a maximum distance between the highest and the lowest data points in the image.

Apart from the standard parameters listed above provides, the surface topography can be quantified by the skewness R_{sk} and kurtosis R_{ku} [107].

The R_{sk} is the skewness, which is a measure of the symmetry of surface data about a mean data profile, expressed as:

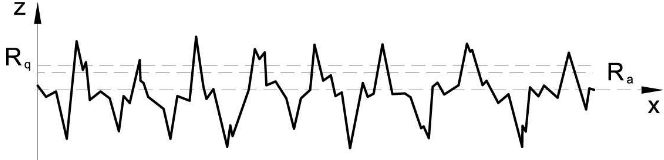
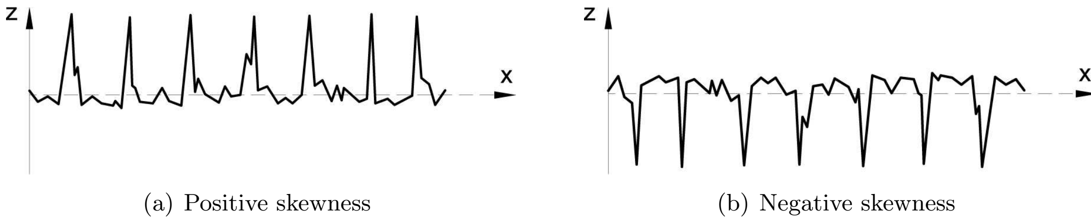


Figure A.1: Roughness parameters: R_a and R_q.



(a) Positive skewness (b) Negative skewness

Figure A.2: Interpretation of skewness parameter

$$R_{sk} = \frac{1}{nR_q^3}\sum_{i=1}^{n} z_i^3 \quad \text{(A.3)}$$

This is a non dimensional quantity which is typically evaluated in terms of positive or negative. Where skewness is zero, an even distribution of data around the mean plane is suggested. Where skewness is strongly non-zero, an asymmetric distribution is suggested. For instance, a flat plane having small sharp spikes has a positive skewness ($R_{sk} > 0$), while a flat plane with small deep pits has negative skewness ($R_{sk} < 0$),as presented graphically in Figure A.2.

The R_{ku} is the kurtosis, which is measure of the degree of peakedness of a surface height distribution. This is a non dimensional quantity used to evaluate the shape of data about a central data profile, expressed as:

$$R_{ku} = \frac{1}{nR_q^4}\sum_{i=1}^{n} z_i^4 \quad \text{(A.4)}$$

Graphically, kurtosis indicates whether data are arranged flatly or sharply about the mean. The kurtosis for a spiky surface is $R_{ku} > 3$, for a bumpy surface is $R_{ku} < 3$ and for a perfectly random surface it is $R_{sk} = 3$.

Appendix B

PECVD technique

B.1 Introduction

Plasma enhanced chemical vapor deposition (PECVD) is a lower-temperature alternative to a standard LPCVD technique, which uses a plasma to enhance the reaction of the precursor gases. The energetic species are created by collisions in the gas, in high alternating electric field. These excited species interact with the substrate, and depending on their nature, etching or deposition at the substrate surface occurs. As energy is transfered into the gas by the plasma, the substrate temperature can be lowered. Typically, the deposition of a variety of thin films by PECVD is possible at temperatures from 50 to 350°C, without reducing its quality in comparison to films deposited by the CVD technique.

A schematic drawing of a PECVD reaction chamber is presented in figure B.1. A substrate is placed on a heated stage, below an electrode. A vacuum pump is used, for creating negative pressure, while a number of inlets provide the precursor and diluting gases at controlled flow rates.

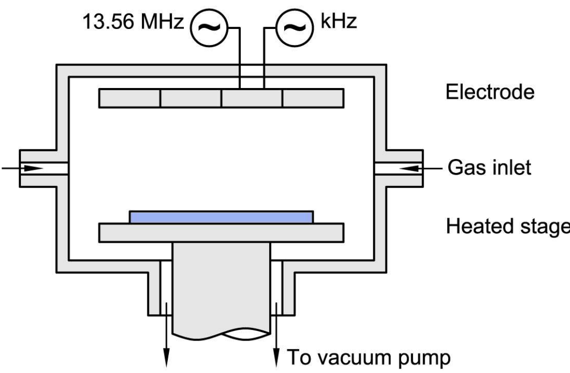


Figure B.1: Schematic of PECVD chamber

B.2 Effect of deposition parameters on SiN$_x$ structural properties

One of the advantages of using PECVD technique is the ease of adjusting the film properties by modifying the deposition parameters, which are:

- Precursor gases,
- Flow rates,
- Total pressure,
- Frequency,
- RF power density.

The following sections discuss the influence of each of the parameters on the properties of PECVD SiN$_x$. Tables B.1 and B.2 presents properties of SiN$_x$ films for different process conditions.

B.2.1 Precursor gases

The silicon nitride is typically obtain from the following precursor gases [36]:

1. Silane and ammonia (SiH_4+NH_3) with or without He/Ar/N_2 dilution.
2. Silane and nitride (SiH_4+N_2) with or without He dilution.

, where the first set of gases is typically used to obtained films with low trap concentrations [42]. Films obtained with N_2 instead of NH_3 have higher density [42]. In terms of hydrogen content , by removing ammonia, the H content can be reduced as much as three times for the same process conditions. By diluting the precursor gases it possible to slow down the oxidation of deposited layers (He dilution [42]), to promote formation of low H-content stoichiometric SiN$_x$ films (He dilution [40]) and it may help to control the film stress. Adding dilution favors formation of [N-H] bonds rather than [Si-H] [42].

Selected properties of films deposited with ammonia are presented in table B.1 and with nitrogen in table B.2.

B.2.2 Flow rates

The flow rates allows to adjust the N/Si ($x_{N/Si}$) ratio of the SiN$_x$, that is to control the electrical an optical properties of so deposited film, by adjusting the [N-H] to [Si-H] bond ratio. For instance, low SiH_4 flow rate results in N-rich SiN$_x$ films, where the N/Si ratio $x > 1.33$ [40] and this translates to lower refractive index [36].

Table B.1: Exemplary properties of SiN_x deposited from silane and ammonia.

ID	Flow rates [sccm]				NH_3/SiH_4	N/Si	Si-H/N-H	Growth rate	Pressure	Power	Freq.	Temp.	Ref.
	SiH_4	NH_3	H_2	He	ratio (R)	(x)	ratio	[nm/min]	[mTorr]	[W]	[MHz]	° C	
A.01	36	0	12		-	0		30.4	800	20		300	[41]
A.02	20	20			1	0.32		24.0	600	20		300	[41]
A0.3	20	40			2	0.69		19.0	600	20		300	[41]
A.04	20	80			4	0.95		17.0	600	20		300	[41]
A.05	20	120			6	0.84		20.0	600	20		300	[41]
A.06	20	200			10	1.1		17.0	600	20		300	[41]
A.07	10	200			20	1.2		16.5	600	20		300	[41]
A.08	30	0			-	0		22.0	600	10		300	[41]
A.09	15	30			2	-		11.1	600	10		300	[41]
A.10	15	60			4	-		13.4	600	10		300	[41]
A.11	15	90			6	-		16.1	600	10		300	[41]
A.12	15	150			1.4	-		21.1	700	10		300	[41]
B.01	40	55			1.4	1.33			950	400		275	[68]
B.02	40	55			1.4	1.32			950	350		275	[68]
B.03	40	55			1.4	1.25			950	300		275	[68]
B.04	40	55			1.4	1.0			950	250		275	[68]
B.05	40	55			1.4	0.87			950	200		275	[68]
B.06	40	55			1.4	0.71			950	150		275	[68]
B.07	40	55			1.4	0.53			950	100		275	[68]
B.08	40	55			1.4	1.33			950	CVD		275	[68]
C.01	6	60		0	10	1.33			250	3	13	350	[108]
C.02	1.8	45		0	25	-			1200	12	13	350	[108]
C.03	1.8	45		0	25	-			1200	18	13	350	[108]
C.04	1.8	45		0	25	-			1200	30	13	350	[108]
C.05	1.8	45		0	25	-			1200	60	13	350	[108]
D.01					2	0.7				500	13.56	270	[109]
E.01					0	0.98	0.94					270	[43]
E.02					0.625	1.10	0.96					270	[43]
E.03					1.25	1.23	0.95					270	[43]
E.04					2	1.28	0.90					270	[43]
E.05					4	1.33	0.50					270	[43]
E.06					6	1.41	0.22					270	[43]
E.07					10	1.43	0.20					270	[43]

Table B.2: Exemplary properties of SiN_x deposited from silane and nitrogen.

ID	Flow rates [sccm]			N/Si	Si-H	N-H	Si-H/N-H	Growth rate	Pressure	Power	Freq.	Temp.	Ref.
	SiH_4	N_2	He	(x)	$\cdot 10^{21}$	$[cm^{-3}]$	ratio	[nm/min]	[mTorr]	[W]	[MHz]	$^\circ$ C	
F.01	5	500	1300	-	-	15	-	1.2	500	120		250	[40]
F.02	10	500	1300	1.50	0.8	13	0.06	2.8	500	120		250	[40]
F.03	14	500	1300	1.39	3.1	6.0	0.52	4.3	500	120		250	[40]
F.04	15	500	1300	1.36	3.6	4.8	0.75	4.4	500	120		250	[40]
F.05	16	500	1300	1.31	6.4	4.0	1.6	4.8	500	120		250	[40]
F.06	17	500	1300	1.23	7.9	2.4	3.29	5.1	500	120		250	[40]
F.07	25	500	1300	1.12	8.7	1.6	5.44	5.3	500	120		250	[40]
F.08	30	500	1300	1.00	16.0	-	-	6.4	500	120		250	[40]
F.09	15	500	1300	1.31	3.4	2.3	1.48	4.2	500	120		250	[40]
F.10	20	300	1300	-	3.5	3.8	0.92	4.5	500	120		250	[40]
F.11	20	500	1300	-	4.0	4.3	0.93	5.9	500	120		250	[40]
F.12	20	700	1300	-	3.8	5.5	0.69	5.5	500	120		250	[40]
F.13	20	900	1300	-	1.8	7.3	0.24	5.3	500	120		250	[40]
F.14	20	500	0	-	16.0	1.3	12.3	6.5	500	120		250	[40]
G.01	1	150	250		4.35	11.5	0.38	12.3	500	12		250	[42]
G.02	1	150	100		6.10	10.7	0.57	12.6	500	12		250	[42]
G.03	1	150	75		9.48	9.51	1.0	10.1	500	12		250	[42]
G.04	1	150	49		13.3	4.89	2.72	12.5	500	12		250	[42]
G.05	1	50	250		9.77	7.0	1.4	5.7	350	3		250	[42]
G.06	1	50	250		6.92	11.8	0.59	5.7	350	3		250	[42]
G.07	1	50	250		7.12	8.77	0.81	7.3	350	3		250	[42]
G.08	1	50	250		11.5	12.3	0.93	6.1	350	3		150	[42]
G.09	1	50	250		11.0	9.92	1.11	6.8	350	3		100	[42]
G.10	1	50	250		12.9	7.48	1.72	8.0	350	3		50	[42]
G.11	1	50	350		7.2	10.5	0.69	6.8	350	3		100	[42]
G.12	1	50	350		8.17	12.5	0.65	5.6	350	3		100	[42]

B.2.3 Frequency

By using the STS' patented technique of mixing the plasma frequency it is possible to control the level of the internal tensile and compressive stresses induced in the film, in the range of 10 MPa to 1GPa, with an accuracy of 10 MPa. As a general rule, the high frequency films are tensile, while low frequency films are compressive. An exemplary stress distribution for a 1 mm thick SiN$_x$ deposited on 3" GaAs and 4" Si substrates is presented in Figure B.2, where a logarithm of the residual stress is plotted as a function of the percentage of the high frequency in the total high (13.56 MHz) and low (187.5 kHz) frequency mix [from STS commercial materials].

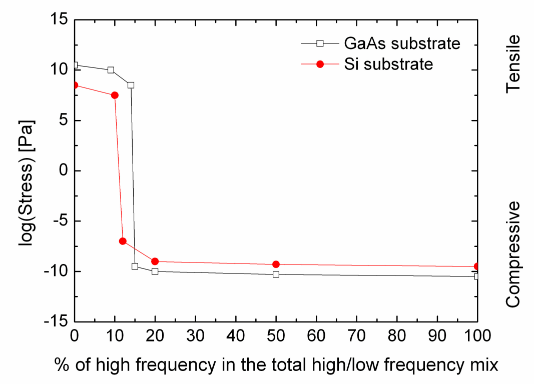


Figure B.2: Logarithm of the residual stress is plotted as a function of the percentage of the high frequency in the total high (13.56 MHz) and low (187.5 kHz) frequency mix.

The possibility to control the intrinsic stresses may have many applications in the domain of electronics and microsystems. As it has been showed in the previous chapter, it is possible to modify the characteristic (pull-in voltage) of an ohmic-type RF MEMS switch by adjusting the residual stress in the beam. Another example, are the passivation layers, where it is advised to limit the intrinsic stresses to avoid cracking of so deposited layer.

B.2.4 Power

By increasing the RF power all reactive ions in plasma are enhanced, which results in higher deposition or etch rate [36, 42]. Increase of power may result in an increase in compressive stress up to a maximum value of 2000 MPa in a N-rich SiN$_x$, with no other significant change in other film properties.

B.2.5 Temperature

The deposition temperature plays has a significant effect on the concentration of hydrogen and its distribution among [N-H] and [Si-H] bonds. In terms of H-content, typically lower temperature means less energy available to desorb the hydrogen. As a consequence more H

Table B.3: Electronic properties of SiN_x as a function of deposition parameters.

ID	NH_3/SiH_4 ratio (R)	Temp. ° C	rf power [W]	N/Si (x)	E_0 [eV]	ϵ_d at 25 ° C	ϕ_0 [eV]	ρ [Ω·cm]	ϵ_s	Ref.
A.01	-	300	20	0	1.66					[41]
A.02	1	300	20	0.32	1.83					[41]
A.03	2	300	20	0.69	2.07					[41]
A.04	4	300	20	0.95	2.65		1.06			[41]
A.05	6	300	20	0.84	2.73		1.12			[41]
A.06	10	300	20	1.1			1.36			[41]
B.01			400	1.33		2.9	0.81	$5 \cdot 10^{19}$	5.8	[68]
B.02			350	1.32		2.7	0.87	$3 \cdot 10^{17}$	6.5	[68]
B.03			300	1.25		2.8	0.75	$3 \cdot 10^{15}$	6.8	[68]
B.04			250	1.0		2.5	0.75	$4 \cdot 10^{13}$	6.4	[68]
B.05			200	0.87		2.5	-	$9 \cdot 10^{11}$	7.0	[68]
B.06			150	0.71		2.0	-	$1 \cdot 10^{10}$	6.7	[68]
B.07			100	0.53		1.8	-	$4 \cdot 10^{4}$	7.8	[68]
B.08			CVD	1.33		1.9	1.06	$8 \cdot 10^{20}$	7.2	[68]
H.01		300		0.19			0.72			[44]
H.02		300		0.49			0.69			[44]
H.03		300		0.54			0.84			[44]
H.04		300		0.84			0.96			[44]

(a) ρ for B sample measured at 2 MV/cm

atoms is incorporated in so deposited layer, which reduces film density and increase its porosity, apart form modifying the electronic properties of the film. This has an effect on the level of intrinsic stresses [42].

Reducing temperature tends to create films with higher trap concentrations [42].

B.3 Effect of deposition parameters on SiN_x dielectric properties

The conduction in the silicon nitride is found to be of Poole-Frenkel type, that is to be limited by the properties of the bulk. The consequence of the ability to control the stoichiometry of PECVD nitrides allows adjusting the optical and electric properties as can be seen in table B.3. For instance, the static ϵ_d may vary from 5.8 to 7.8, depending on the N/Si ratio. It is worth noticing, that the dielectric constant obtained from the Poole-Frenkel is more than 50% lower than the static one.

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Résumé

Chapitre 1

Introduction

Les MEMS sont des dispositifs avec une longueur caractéristique entre 1 µm et 1 cm, qui combinent des fonctions électriques et mécaniques et qui sont fabriqués en utilisant les mêmes procédés microélectroniques que pour les circuits intégrés [1].

Les commutateurs RF MEMS, en particulier, sont conçus pour fonctionner dans une large gamme de fréquences de 0.1 a 120 GHz. Par exemple, pour des applications de communication les fréquences varient de moins de 1 MHz pour les AM et 88-108 MHz pour la FM, jusqu'à 2.4 GHz pour les applications mobiles [2]. Pour des applications dans l'industrie automobile, telles que les radars et antennes de toit, les fréquences standard sont 24, 60 et 77 GHz [3].

Le premier document sur les commutateurs RF MEMS date de 1979 [4]. Cependant, une accélération de la recherche et des développements peuvent être observés depuis le milieu des années 1990, surtout aux Etats-Unis.

Les premiers commutateurs RF MEMS ont été commercialisés en 2003 [5] par Magfusion et TeraVicta. En 2006, plus de 40 entreprises, partout dans le monde, étaient activement impliquées dans la recherche et le développement des commutateurs RF MEMS, mais seule une petite partie d'entre eux était proche de la commercialisation de leurs produits [5].

Le marché des RF MEMS a crû rapidement aux États-Unis ces dernières années, de 126 millions de dollars en 2004 à 1.1 milliards de $ en 2009 [5]. Cette croissance rapide qui devrait encore s'accélérer est le moteur des recherches en cours.

Caractéristiques générales des commutateurs RF MEMS fabriqués par le CEA-Leti

Un commutateur RF MEMS utilise classiquement le mouvement mécanique d'une poutre, pour modifier l'impédance du dispositif. Par conséquent, les commutateurs RF MEMS peuvent être divisés en 2 catégories principales selon le mode d'actionnement de la poutre et le type de contact utilisé pour modifier l'impédance.

- *Méthode d'actionnement*

  Les commutateurs RF MEMS qui sont étudiés dans cette thèse sont actionnés électrostatiquement.

Pour l'actionnement électrostatique, une tension de polarisation est appliquée entre 2 électrodes, une électrode est fixe et l'autre est mobile (poutre). La tension appliquée entre les 2 électrodes génère une force électrostatique qui provoque le mouvement de la poutre mobile qui vient alors en contact avec l'électrode fixe. La poutre reste à l'état bas ("pulled-down") aussi longtemps que la tension est appliquée. Pour faire revenir la poutre dans sa position initiale, la différence de potentiel entre les deux électrodes doit être annulée. La position de la poutre peut être déterminée en mesurant la capacité formée par les deux électrodes [7].

Cette méthode d'actionnement nécessite une tension d'actuation relativement élevée V_{act} de l'ordre de 10-80V, qui est le principal inconvénient. Par contre, presque aucun courant n'est consommé pour actionner la poutre, et ainsi la consommation de puissance varie de 10 a 100 nJ par cycle de commutation. De même, la vitesse de commutation est la plus élevée parmi toutes les méthodes d'actionnement et elle est comprise entre 1 à 200 µs. Les forces de contact peuvent aussi être relativement élevées (50-1000 µN) [3].

En pratique, cette méthode est la plus utilisée pour actionner les commutateurs RF MEMS et il a été démontré que les commutateurs de ce type peuvent fonctionner de 100 millions à 10 milliards de cycles.

- *Types de contacts*

  Les contacts des commutateurs étudiés au cours de la thèse sont de deux types différents: ohmique ou capacitif.

  Le contact de type ohmique est présenté schématiquement sur la figure 1.1(a) [3]. Il est souvent utilisé dans la configuration série, qui ne permet pas au courant de passer d'un point à un autre d'un circuit électrique dans l'état "off". Les commutateurs de ce type ont un contact métal-métal. Les caractéristiques du contact ohmique le rendent plus particulièrement approprié aux applications nécessitant une large gamme de fréquences à partir du continu DC jusqu'à 40 GHz [8]. Les propriétés RF telles que les pertes d'insertion et l'isolement dépendent de la qualité du contact ohmique (faible résistance). La fiabilité du contact ohmique est par conséquent un point critique pouvant directement déterminer la durée de vie du commutateur.

  Le contact de type capacitif est présenté schématiquement sur la figure 1.1(b) [3, 9]. Il est souvent utilisé dans la configuration "shunt", qui permet au courant de passer d'un point à un autre d'un circuit électrique dans l'état "off". Les commutateurs de ce type utilisent un contact métal-diélectrique servant à bloquer ou à faire passer le signal RF. Ceci est accompli en modulant la capacité entre la poutre mobile et la ligne RF, par l'actionnement de la poutre. Du fait du couplage capacitif utilisé pour bloquer le signal, les commutateurs de type capacitif ne sont pas adaptés pour des applications à basse fréquence, à la différence des commutateurs de type ohmique. La bande passante typique des commutateurs de type capacitif est de 10 a 120 GHz [8].

Performance des commutateurs RF MEMS

Les commutateurs RF MEMS constituent une alternative aux diodes p-i-n et transistors à effet de champ (FET) [3]. Les performances des commutateurs RF MEMS en 2007 et leurs perspectives jusqu'en 2015 sont présentées pour les commutateurs ohmiques et capacitif dans le

tableau 1.1 et le tableau 1.2. A titre de comparaison, les performances des diodes p-i-n et FET sont présentées dans le tableau 1.3 [8].

Pour résumer, les commutateurs FET sont appropriés pour un fonctionnement à basse fréquence gamme dans laquelle ils peuvent traiter un signal de forte puissance. Aux fréquences élevées, leurs performances baissent. Les transistors MESFET GaAs et diodes p-i-n sont bien adaptés pour travailler à des fréquences élevées, mais acceptent uniquement un signal de faible puissance. Il faut aussi noter que de manière générale, tous les commutateurs à base de semi-conducteurs présentent des pertes d'insertion élevées, qui augmentent la consommation d'énergie, et une faible isolation électrique, de l'ordre de -20 a -25 dB dans l'état bloqué [2, 6].

Les commutateurs RF MEMS, quant à eux, présentent de meilleures performances RF, notamment en termes d'isolation, de pertes d'insertion et de linéarité. Grace à leurs performances et leur polyvalence, des composants RF MEMS peuvent remplacer l'ensemble des circuits réalisés avec des diodes p-i-n et FET [2]. Néanmoins, la technologie de RF MEMS est toujours confrontée à des problèmes de fiabilité. .

Problèmes de la fiabilité des MEMS RF

Deux modes de défaillances principaux réduisent la durée de vie des commutateurs RF MEMS. L'un est lié à la méthode d'actionnement électrostatique et l'autre à la fiabilité des contacts.

- *Problèmes liés a la méthode d'actionnement*

  La méthode la plus courante pour l'actionnement des commutateurs RF MEMS est l'actionnement électrostatique est. Comme nous l'avons déjà signalé, la tension standard d'actionnement électrostatique dans des RF MEMS est comprise entre 10 et 80 V, de plus l'entrefer entre la poutre mobile et l'électrode fixe est inférieur à quelques µm, et enfin l'épaisseur du diélectrique qui sépare les électrodes est généralement inférieure à 1 µm. Cette combinaison (tension d'actionnement, entrefer petit, faible épaisseur du diélectrique) crée un champ électrique très élevé dans la couche du diélectrique, (plusieurs MV/cm en fonctionnement normal). Dans ces conditions, des charges parasites électriques sont facilement piégées dans le diélectrique.

  La répartition de cette charge piégée dans la couche diélectrique peut engendrer une dérive de la tension d'actionnement. Si la dérive de tension est assez élevée, la tension "pull-in" peut dépasser la tension de commande et le commutateur ne peut plus être fermé, ce qui conduit à sa défaillance [11]. La figure 1.2 présente pour un commutateur de type capacitif une courbe initiale CV et une courbe CV décalée après une application de tension constante pendant un temps fixé [12].

  L'analyse quantitative de l'influence de la charge piégée sur le "pull-in" de tension et la caractéristique CV des commutateurs RF MEMS est présentée en détail au chapitre 4.

- *Problèmes liés à la qualité du contact*

  Les commutateurs de type ohmique utilisent un contact métal-métal pour basculer entre l'état bloqué et l'état passant. Toute dégradation du contact augmente la résistance, donc il augmente la perte de signal. Le point critique est le choix des matériaux de contact,

qui doit être optimisé en termes de résistance de contact, et de sensibilité à l'adhésion en fonction de la durée de vie visée.

La problématique est similaire pour les commutateurs de type capacitifs utilisant un contact métal-diélectrique qui ne doit pas se dégrader afin de maintenir les performances RF du commutateur.

Motivations de la thèse

La thèse s'est déroulée au CEA-Leti de Grenoble qui est un centre de recherche appliquée pour la microélectronique et les technologies de l'information, et agit comme une interface entre l'industrie et la recherche universitaire.

Un des thèmes de recherche du CEA-Leti est le développement de commutateurs RF-MEMS actionnés électrostatiquement, avec comme objectifs leur fabrication, leur fiabilisation et leur commercialisation.

Cette thèse se focalise sur la fiabilité des commutateurs RF MEMS actionnés électrostatiquement de types ohmique et capacitif fabriqués par le CEA-Leti. Plus précisément, la priorité a été mise sur l'étude des problèmes de fiabilité liés à l'actionnement électrostatique (chargement du diélectrique).

Comparaison des commutateurs de type ohmique et capacitif

Les deux types de commutateurs étudiés utilisent la méthode d'actionnement électrostatique. Dans chaque cas, l'électrode supérieure mobile est séparée de l'électrode inférieure (la ligne RF) par une couche de diélectrique. Ces deux types de commutateurs varient par la localisation de leur entrefer. Dans le cas d'un commutateur de type ohmique, le diélectrique constitue l'électrode mobile, donc l'entrefer est formé entre le diélectrique et l'électrode inférieure. Dans le cas du commutateur de type capacitif, le diélectrique est déposé sur le dessus de la ligne RF, donc l'entrefer est situé entre le diélectrique et l'électrode supérieure.

Le tableau [ref. table] compare les performances et les caractéristiques des commutateurs ohmiques et capacitifs fabriqués par le CEA-Leti. Les commutateurs ohmiques sont conçus pour fonctionner à des fréquences allant du continu jusqu'à environ 40 GHz, tandis que les commutateurs capacitifs peuvent fonctionner dans la gamme de 10 à 120 GHz. La tension d'actionnement nominale pour les commutateurs ohmiques est de 15 à 25 V, contre 25-40 V pour les commutateurs de type capacitif. Les dimensions des commutateurs ohmiques et capacitifs sont comparables.

Organisation de la thèse

Les objectifs qui ont été présentés dans la section précédente, se reflètent dans l'organisation de la thèse qui est divisée en trois chapitres.

Le premier chapitre expérimental (chapitre 2) décrit le comportement électromécanique des commutateurs RF MEMS de type ohmique. Ce chapitre présente un modèle électromécanique, qui permet de comprendre les principes de fonctionnement des commutateurs RF MEMS et qui est utilisé, pour étudier l'influence des propriétés des matériaux (*ex.* contraintes résiduelles) et de la géométrie sur son comportement électromécanique.

Pour valider ce modèle, une série de tests par nanoindentations a été effectuée sur les commutateurs RF MEMS de type ohmique. Ces résultats des tests sont ensuite utilisés pour calculer les réponses théoriques électriques de ces commutateurs, qui sont ensuite comparés avec les réponses mesurées.

Dans le chapitre 3, les propriétés structurales et électriques des diélectriques sont étudiées. Dans cette partie, les commutateurs RF MEMS de type capacitif sont étudiés. Ces commutateurs ont été choisis pour deux raisons: la première est la disponibilité de structures de test, plus nombreuses pour les commutateurs de type capacitif, la seconde est une géométrie de commutateur plus simple ; sachant que de toute manière les commutateurs RF MEMS de type capacitif utilisent le même type de diélectrique que les commutateurs de type ohmique, un nitrure HF PECVD SiN_x. Le chapitre 3 est divisé en deux parties. La première partie présente les résultats des analyses de structure et de composition de nitrures PECVD SiN_x et de silice SiO_2 qui sont ensuite comparés avec l'état de l'art. Dans la seconde partie, les mécanismes de conduction et de la cinétique de piégeage sont identifiés grâce à des mesures I-V et des injections de courant constant faites sur des structures de type capacité MIM (Métal-Isolant-Métal).

Le chapitre 4 traite du problème du chargement du diélectrique dans les commutateurs RF MEMS. Il commence par une présentation des modèles existants pour modéliser le chargement du diélectrique dans les commutateurs RF MEMS. Ensuite, il présente notre modèle original d'accumulation de charge parasite dans un diélectrique sous tension constante. Ce modèle est basé sur les propriétés diélectriques identifiées dans le chapitre précédent, la cinétique d'accumulation de la charge en fonction de la tension est calculée pour trois types de diélectriques et deux types de commutateurs. Ces dérives de tension calculées sont comparées avec les résultats expérimentaux et après vérification du modèle proposé, le modèle est utilisé pour étudier l'impact des propriétés des matériaux et la géométrie du commutateur sur la cinétique d'accumulation de charge.

Le dernier Chapitre 5 conclut ce travail et dresse les perspectives pour la suite de ce travail.

Chapitre 2

Comportement électro-mécanique des RF MEMS

Ce chapitre explique le comportement électromécanique de commutateurs RF MEMS.

Ce chapitre commence par une présentation et discussion des deux modèles analytiques. Le premier est un modèle mécanique original, qui a été conçu pour un commutateur constitué de deux paires d'électrodes. Le second est un modèle électromécanique standard, qui a été adapté pour les commutateurs de type ohmique. Ces deux modèles sont utilisés, en particulier, pour expliquer le fonctionnement des commutateurs actionnés électrostatiquement et démontrer l'effet des propriétés des matériaux et de la géométrie sur leur comportement.

Ce chapitre se termine par une comparaison des résultats expérimentaux avec les réponses théoriques calculées grâce au modèle électromécanique.

Description des échantillons

Les commutateurs RF MEMS de type ohmique fabriqués par le CEA-LETI sont étudiés dans ce chapitre. Ces commutateurs ont déjà été présentés en détail dans le chapitre précédent, dans la section 1.2.2.1. Néanmoins, pour rappeler la conception de ces commutateurs, la figure 2.1 présente des images MEB: le commutateur en entier (a) les contacts mobiles (b, c) et les contacts fixes (d).

4 lots caractéristiques ont été sélectionnés, qui sont notés: ohm.A, ohm.B, ohm.C et ohm.D. Le tableau 2.1 présente un résumé concis des différences entre les plaques étudiées, tels que:

- *Niveau de la contrainte résiduelle σ_x de SiN_x*

  La contrainte résiduelle est mesurée après l'étape de dépôt de la couche de SiN_x sur une plaque. En pratique, la valeur de la contrainte est obtenue en mesurant la courbure de la plaque avant et après le dépôt par l'équation 2.1 [15]. La valeur moyenne de la contrainte résiduelle de nos commutateurs de type ohmique, mesurée a l'étape de fabrication, est de ∼300 MPa. Cette valeur peut être contrôlée par les conditions de dépôt. Dans notre étude, la contrainte la plus faible a été obtenuepour la plaque ohm.A et la plus élevée pour la plaque ohm.B.

- *L'entrefer du contact (g_c) et l'entrefer entre électrodes (g_0)*

  L'entrefer du contact et l'entrefer entre électrodes sont schématiquement présentés à la figure 2.2. En optimisant ces entrefers, il est possible d'ajuster le comportement électrique des commutateurs.

  Dans le cas présenté, la largeur de l'entrefer entre électrodes g_0 reste toujours inférieure à 1 µm et est assez reproductible d'une plaque à l'autre.. La valeur de l'entrefer du contact présente plus de d'une plaque à l'autre : la plaque ohm.B a une valeur d'entrefer du contact le plus faible, tandis que la plaque ohm.A présente la valeur l'entrefer la plus élevée.

- *Processus de fabrication pour réaliser le contact mobile*

  La qualité du contact ohmique est un facteur limitant pour les performances RF des commutateurs de type ohmique. Deux procédés de réalisation du contact ont été développés,

un procédé *standard* et un procédé *optimisé* , qui sont présentés en détail dans le tableau 2.2.

Dans cette étude, le procédé standard est utilisé pour réaliser le contact mobile de la plaque ohm.A. Le procédé optimisé est utilisé pour les plaques ohm.B, ohm.C et ohm.D.

Les contacts mobiles pour les 4 plaques sont fabriqués en or.

Modèle électromécaniques d'un commutateur MEMS

La modélisation analytique des dispositifs MEMS est une tâche non-triviale, car elle nécessite souvent de faire de nombreuses hypothèses et simplifications, concernant les propriétés du matériau et la géométrie des dispositifs. Ce sont des sources d'erreurs qui doivent être minimisées autant que possible.

Par exemple, un bon exemple d'un paramètre qui a un effet sur le fonctionnement des dispositifs MEMS, et qui est fortement dépendant du procédé de fabrication, est la contrainte résiduelle dans les matériaux. La contrainte résiduelle est induite lors du procédé de dépôt, mais elle peut encore être modifiée dans les étapes de fabrication ultérieures, y compris le recuit post-dépôt. Il a été rapporté [16, 17] que ce paramètre peut à lui tout seul exercer une influence significative sur le comportement électromécanique des MEMS. Les contraintes de compression, par exemple, peuvent être une source de déformations initiales des pièces mécaniques, sans aucune charge externe, qui peuvent conduire au flambage. D'autre part, des contraintes de traction provoquent un raidissement. Dans certains cas, pour les empilements multicouches, la différence des contraintes résiduelles dans les couches adjacentes peut entraîner des fissures ou des décollements [18].

Dans cette section, nous élaborons un modèle mécanique original pour un commutateur avec des électrodes latérales. Ce modèle est ensuite combiné avec un modèle standard électrostatique pour décrire le comportement électromécanique du commutateur. Nous discutons l'influence des contraintes résiduelles et la géométrie sur le comportement électromécanique. La rigidité de la poutre dépend de sa géométrie et des propriétés du matériau. Les paramètres qui peuvent être facilement modifiés ou ajustés pour les commutateurs étudiés sont la largeur de la poutre, son épaisseur et le niveau de la contrainte résiduelle.

Lorsque ces trois paramètres varient dans un rapport allant de 0,5 à 1,5 par rapport à leurs valeurs nominales indiquées dans le tableau 2.1, la raideur k_c au centre de la poutre, pour une charge centrale concentrée normale, varie de la façon présenté à la figure 2.10(a). Ces résultats montrent que les 3 paramètres analysés exercent une influence linéaire sur la raideur et qu'aucun d'entre eux n'est dominant.

La figure 2.10(b) présente la raideur k_c au centre de la poutre, en fonction de la contrainte résiduelle dans la poutre. En cas de contraintes résiduelles égales a zéro, la raideur k_c baisse à environ 1 N/m, au lieu de la valeur nominale de 112 N/m. Ceci souligne l'importance de contrôler le niveau des contraintes résiduelle pendant la fabrication.

Caractérisation des commutateurs de type ohmique

Dans la partie suivante de ce chapitre, les 4 plaques de commutateurs ohmiques sont caractérisées en détail. Ces données expérimentales sont ensuite utilisées pour calculer les réponses électriques des commutateurs, qui sont comparées au comportement électrique expérimental.

- *Analyse de la géométrie du commutateur*

  Comme il a été démontré dans la section précédente, la géométrie et la topographie de surface des commutateurs RF MEMS de type ohmique exercent un effet significatif sur leur comportement électromécanique. La section suivante vise à faire sur les 4 plaques étudiée une étude morphologique des contacts ohmiques (fixes et mobiles) et des électrodes d'actionnement.

  Cette étude morphologique comprend des caractérisations de microscopie électronique à balayage SEM ("Scanning Electron Microscope") pour observer l'aspect des surfaces, des caractérisations FIB ("Focused Ion Beam") pour obtenir des coupes sur les contacts ohmiques et les électrodes, et des caractérisations AFM (Atomic Force Microscope) pour l'analyse quantitative de la qualité de surface.

- *Caractérisation des propriétés mécaniques*

  Cette section vise à caractériser les propriétés mécaniques des commutateurs de type ohmique, avant la modélisation de leur comportement électromécanique.

  La caractérisation des propriétés mécaniques du matériau d'un dispositif fabriqué est très importante, étant donné que ces propriétés peuvent être modifiées au cours des étapes de fabrication suivant le dépôt, en particulier pendant le recuit de post-fabrication. Cette tâche n'est pas simple en raison de la faible dimension des échantillons, ce qui nécessite l'utilisation de techniques d'essais non conventionnelles.

  La solution retenue est d'utiliser un nano-indenteur avec une pointe sphérique pour effectuer une mesure force-déplacement au centre de la poutre et au centre de l'électrode. Ces valeurs de raideur expérimentales sont utilisées dans le modèle mécanique de manière à déduire une valeur de la contrainte effective résiduelle dans la poutre.

- *Caractérisation du comportement électrique*

  Cette section vise à caractériser le comportement électrique des 4 plaques de commutateurs de type ohmique. Les mesures des caractéristiques CV et VR sont effectuées grâce à un banc de test dédié.

Conclusions

Une modèle électromécanique pour les commutateurs de type ohmique a été développé et validé dans ce chapitre. Il est montré comment ce modèle peut être utilisé pour calculer des réponses électriques des commutateurs à partir des données géométriques et des propriétés mécaniques.

Pour identifier les propriétés mécaniques (rigidité de la poutre) et la géométrie (entrefer électrode g_0 et entrefer contact g_c) des commutateurs de type ohmique, la technique de nano-indentation a été appliquée avec succès, même si parfois, cette dernière n'a pas été suffisante pour mesurer la valeur réelle des entrefers de contact. Dans ce cas, les mesures de nano-indentation ont été complétées par les mesures de topographie AFM.

Il est possible de conclure que la tension de pull-in (capacitive) V_{pi} est principalement sensible à la raideur de la poutre, l'entrefer d'électrode g_0 et la surface des électrodes d'actionnement A_{el}.

La rigidité des commutateurs s'avère être fortement dépendante de la contrainte résiduelle induite dans la poutre (PECVD SiN_x). La possibilité de contrôler cette contrainte lors du dépôt du SiN_x offre un potentiel d'adaptation rapide et fiable de la tension pull-in pour les commutateurs fabriqués.

La raideur au niveau des électrodes lorsque deux forces normales sont appliquées simultanément au centre des électrodes est environ 1,8 fois plus élevée qu'au centre de la poutre, lorsque seule une charge normale est appliquée au centre de la poutre. Par conséquent, la force minimale nécessaire pour fermer le commutateur est d'au moins 1,8 fois plus élevée, quand il y a deux paires d'électrodes symétriques, comparativement à une situation où il y a une seule paire d'électrode d'actionnement située au centre de la poutre. Ainsi, la tension à appliquer dans notre commutateur RF MEMS de type ohmique, du fait de sa conception avec deux paires d'électrodes symétriques, est plus élevée que pour un "design" avec une électrode centrale d'actionnement (cas du commutateur de type capacitif).

La force de rappel dépend la hauteur de l'entrefer du contact et de la raideur au centre de la poutre. Une hauteur d'entrefer de contact trop petite peut entraîner une force de rappel insuffisante, d'où des risques de collage permanent des commutateurs, comme c'est le cas pour la plaque ohm.B.

Les forces de contact dépendent principalement de la distance de séparation entre l'électrode et l'entrefer de contact. Plus cette différence est grande, plus grande est la force du contact. Dans notre cas, la force de contact est généralement plusieurs fois supérieure à la force de rappel pour chaque échantillons étudié. Comme cela a été démontré sur l'exemple de la plaque ohm.B, une force de contact élevée améliore le contact entre le contact mobile et la ligne de transmission RF du signal et peut conduire à la réduction de la résistance du commutateur. Il est à noter que l'influence de la force de contact sur le comportement à long terme des contacts ohmiques n'a pas été étudiée dans cette thèse.

Le procédé optimisé de fabrication des contacts conduit à une surface de contact beaucoup plus homogène. Néanmoins, il est essentiel de bien contrôler la profondeur de gravure de la poutre en SiN_x pour éviter la gravure d'un trou, ce qui a été fait pour la plaque ohm.C.

L'optimisation des couches en poly-Si et SiO_2 (plaque ohm.D) conduit à une plus grande rugosité, par rapport à la technologie précédente. Cette rugosité est transférée aux couches supérieures, ce qui entraîne une baisse C_{dn}/C_{up} ratio, qui a un effet négligeable sur le fonctionnement des commutateurs RF MEMS de type ohmique. Le niveau de rugosité est acceptable car il n'empêche pas la fermeture du contact ohmique.

Des précautions doivent être prises pour les procédés de fabrication venant après le dépôt d'or (les électrodes du bas et la ligne de transmission de signal RF), pour éviter la formation de protubérances ("hillocks") sur la surface d'or, car ils peuvent gêner le fonctionnement des commutateurs (wafer ohm.C). La température est le catalyseur principal pour la formation des "hillocks", elle doit être maintenue en dessous de 280°C.

La différence entre les tensions de pull-in capacitive et résistive est une preuve que que la hauteur de l'entrefer de contact est plus petit d'un tiers que la hauteur de l'entrefer entre électrodes.

Chapitre 3

Les propriétés physiques des nitrures PECVD SiN_x et oxydes SiO_2

Le chargement du diélectrique est le mode principal de défaillance qui limite la fiabilité dans les commutateurs RF MEMS actionnés électrostatiquement. Il correspond à un piégeage de charges parasites dans la couche diélectrique séparant les électrodes, initié sous un champ électrique élevé (d'environ 0,2 à plusieurs MV/cm). Malgré des recherches approfondies ces dernières années, la physique du piégeage dans les RF MEMS n'est pas encore claire et elle reste un sujet de recherche ouvert.

Ce chapitre vise à étudier la structure et les propriétés électriques de SiN_x et SiO_2 déposés à basse température en utilisant la méthode PECVD (Plasma Enhanced Chemical Vapor Deposition), qui sont les mêmes que ceux qui ont été utilisés pour fabriquer les commutateurs MEMS RF.

La première partie de ce chapitre est centrée sur l'analyse d'une structure et de la composition des matériaux diélectriques. Il regroupe des analyses par TEM (Transmission Electron Microscopy) pour identifier la structure des matériaux, des analyses élémentaires par EDS (Energy dispersive X-ray Spectroscopy), RBS (rétrodiffusion Rutherford), NRA (analyse de la réaction nucléaire) et ERDA (Elastic Recoil Detection Analysis) pour déterminer la stoechiométrie des diélectriques et des analyses SIMS (Spectrométrie de masse des ions secondaires) pour obtenir des profils de contamination.

La deuxième partie est consacrée à déterminer les propriétés électriques des diélectriques, tels que les mécanismes de conduction et la cinétique de piégeage des charges.

Description des échantillons testés

Contrairement au chapitre précédent, dans cette partie nous analysons des commutateurs RF MEMS de type capacitif. Les commutateurs de type capacitif sont préférés pour les deux raisons mentionnées ci-dessous, ainsi que du fait d'un plus grand nombre d'échantillons disponibles et une géométrie plus simple :

- L'électrode supérieure est composée d'une couche Al ou AlSi, qui fournit un meilleur contact avec la couche diélectrique lors de l'actionnement et donc une distribution plus uniforme du champ électrique.
- La couche de diélectrique est directement déposée sur l'électrode inférieure avec une épaisseur uniforme et de forme rectangulaire, ce qui rend plus facile la préparation des échantillons pour les analyses structurelles.

Les échantillons tests utilisés dans ce chapitre sont des capacités métal-isolant-métal (MIM) et des structures air-isolant-métal (AIM) (commutateurs RF MEMS de type capacitif sans membrane), fabriquées par le CEA-Leti.

Une image MEB d'une capacité MIM utilisée dans ce chapitre est présentée à la figure 3.2 (a) et son empilement est présenté schématiquement à la figure 3.2 (b). Les capacités MIM ont deux plots notés (A) et (C), le plot (A) est connecté à l'électrode supérieure (B) et le plot (C) est connecté à l'électrode inférieure. En raison des courant de fuite élevés qui ont été constatés

entre les plots et le substrat, la connexion entre A et B est coupée pour faire les mesure de courant de fuite à travers le diélectrique.

Les capacités MIM sont utilisées dans ce chapitre pour l'imagerie TEM ainsi que pour tous les tests électriques.

Les échantillons AIM présentés sur la figure 3.2 (c) sont utilisés pour les analyses élémentaires. L'empilement de ces échantillons est le même que celle des capacités MIM, sauf qu'il n'y a pas d'électrode supérieure, la surface supérieure du diélectrique est exposée à l'air comme dans les commutateurs MEMS capacitifs.

La technique PECVD a été choisie pour déposer les couches diélectriques, principalement en raison de la faible température de dépôt.

Les paramètres de dépôt sont résumés dans le tableau 3.2 pour les 4 plaques de commutateurs RF MEMS de type capacitif et des structures de test correspondant.

Un nombre total de 4 plaques avec 3 types différents de diélectriques sont étudiés dans ce chapitre, tel que SiN_x PECVD à fréquence haute ou mixte et SiO_2 PECVD fréquence mixte.

Le matériau PECVD SiN_x est obtenu à partir d'une réaction du silane avec de l'ammoniaque et avec le substrat à 300°C. La seule différence entre ces diélectriques est la fréquence des dépôts. Les échantillons capa.A et capa.B sont déposés à haute fréquence (13,56 MHz) pour induire des contraintes de traction dans le diélectrique. L'échantillon capa.C est obtenu en fréquence mixte (13,56 MHz et 187,5 kHz) pour induire une contrainte de compression. Les autres paramètres de dépôt restent les mêmes.

Le matériau PECVD SiO_2 est obtenu à partir d'une réaction de silane avec le gaz hilarant et avec le substrat à 150°C. Cet échantillon est désigné comme capa.D.

A noter que la plaque capa.A a été fabriquée plusieurs mois avant les autres échantillons. Les échantillons capa.B, capa.C et capa.D sont issus du même lot de fabrication.

Les diélectriques décrits ici sont les mêmes pour les capacités MIM et les commutateurs MEMS de type capacitif. Les structures de test et les commutateurs sont en effet fabriqués sur la même plaque, pendant le même processus de fabrication.

Les analyses structurelles

Cette partie de ce chapitre vise à déterminer la structure et la composition des trois types de diélectriques utilisés dans les commutateurs RF MEMS de type capacitif. Il y a un total de 4 plaques, 2 plaques avec des couches HF SiN_x (épaisseur différente et électrode supérieure), 1 plaque avec une couche de MF SiN_x et 1 plaque avec une couche de MF SiOx, comme présenté dans le tableau 3.2.

Les analyses confirment la phase amorphe de PECVD SiN_x et SiO_2. De plus, elles montrent la présence de phases Pt cristallin dans le voisinage immédiat de l'électrode de Pt. Il s'avère que le plaque capa.A a haute fréquence est riche en Si avec un rapport N/Si $x_{N/Si} = 0,74$, tandis que le SiN_x capa.C (fréquence mixte) est presque stchiométrique avec un rapport N/Si $x_{N/Si} = 1,16$. Le PECVD SiO_2 s'avère être non-stchiométrique, avec un rapport O/Si de 0,81.

La proportion de H est presque la même pour toutes les couche SiN_x, d'environ 23 at. %. La concentration de H est beaucoup plus faible dans SiO_2, où elle n'est que de 3,4 at. %.

Les profils de profondeur ToF-SIMS révèlent des quantités significatives de l'élément O dans tous les échantillons.

Pour les trois types de diélectriques, des traces d'Al, Pt et F réparties sur toute l'épaisseur du diélectrique sont observées, probablement introduites durant le processus de fabrication, qui

est le même pour tous les échantillons. De plus, des traces de K et Na sont trouvées dans des concentrations considérables aux interfaces de SiN_x. Dans le cas du SiO_2, ces éléments sont également détectés dans le volume du diélectrique.

Le Ga trouvé par spectroscopie EDS à l'interface AlSi-SiN_x de l'échantillon capa.C, n'est pas détecté par les autre techniques, ce qui suggère fortement l'hypothèse que les traces de Ga sont dues à la préparation de l'échantillon par la technique FIB, où un faisceau de gallium est utilisé pour pulvériser le matériau.

Caractérisation des propriétés diélectriques

La présence de la charge piégée dans le diélectrique peut être nécessaire au bon fonctionnement de dispositif ou indésirable, selon l'application visée [38]. Par exemple, pour les dispositifs MNOS (non-volatile RAM), le piégeage est recherché car il sert à distinguer les états binaires. D'un autre côté, pour les commutateurs MEMS, la charge piégée peut contribuer à une diminution significative de la durée de vie. Cependant, il y a une exigence commune pour ces 2 applications qui est de prévoir le comportement de la charge piégée dans un diélectrique spécifique et dans un ensemble donné de conditions d'exploitation, ce qui nécessite la connaissance des types de charges présentes dans le diélectrique et leur comportement.

Au cours des 40 dernières années, il y a eu beaucoup d'effort déployé dans l'étude des propriétés électroniques des matériaux diélectriques utilisés, par exemple, dans les circuits CMOS.

Contrairement aux isolants de grille des circuits CMOS, les diélectriques PECVD ont été utilisés, pour une longue période de temps, comme barrière de diffusion ou de couches de passivation. Par conséquent, il n'y avait pas besoin d'étudier les propriétés électroniques de ces matériaux. Ensuite, lorsque des applications plus sophistiquées pour ces diélectriques ont été trouvés, il s'est avéré que ces matériaux n'avaient pas été suffisamment étudiés et que nous manquions de connaissances fondamentales sur leurs propriétés électroniques.

Cette partie du chapitre est destiné à étudier les propriétés électroniques des matériaux diélectriques PECVD qui sont utilisés dans les commutateurs RF MEMS. Elle débute par une description des types de charge dans les diélectriques, et les méthodes utilisées dans la caractérisation de matériaux diélectriques. Elle est suivie d'une courte description du mécanisme de conduction et de piégeage dans les diélectriques. Des mécanismes de conduction et piégeage sont déterminés pour deux types de PECVD SiN_x et un type de PECVD SiO_2, qui sont utilisés dans les commutateurs RF MEMS.

Identification des mécanismes de conduction

Les diélectriques réels montrent une conduction électrique à condition que le champ électrique appliqué dans le diélectrique E_d et/ou la température T soient assez élevés [45, 56]. La conduction est définie comme un flux de porteurs de charge, c'est-a-dire des électrons, des trous ou des ions, en présence du champ électrique. Dans un condensateur Métal-Isolant-Métal (MIM), la conduction se compose de trois étapes. Dans la première phase, les porteurs de charge sont émis par une électrode métallique dans l'isolant. Dans la deuxième étape, ils sont transportés à travers le volume du diélectrique. Dans la dernière étape, ces transporteurs sont émis par le diélectrique et recueilli par l'autre électrode métallique. En conséquence, le courant à travers l'isolant est limitée soit par le procédé d'injection à l'interface métal-isolant ou par le

processus de transport des porteurs de charge à travers l'isolant. En conséquence, les processus de conduction sont divisés en mécanisme contrôlé par l'interface ou par le volume.

La technique standard, qui est utilisé pour identifier les mécanismes de conduction, consiste à mesurer le courant de fuite à travers un diélectrique en fonction du champ électrique. Selon le type du processus de conduction, la courbe I-V est différente. Pour distinguer entre les mécanismes, il est souvent suffisant de mesurer les caractéristiques I-V pour des tensions positives et négatives, et en fonction de la température.

Le tableau 3.5 résume les expressions de la densité de courant en fonction du champ électrique et il présente les dépendances courant-tension, qui sont utilisées en pratique pour identifier le mécanisme de conduction.

Les courbes I-V sont effectuées en utilisant un appareil "Agilent 4156C Precision Semiconductor Parameter Analyzer". Les échantillons sont placés dans une station "Cascade Microtech" sous atmosphère d'azote sec (HR <2 %). Les connexions entre les dispositifs de test sont réalisées avec des câbles triaxiaux Kelvin. Cette configuration permet de mesurer les courants aussi bas que plusieurs fA, ce qui est équivalent à une densité de courant de plusieurs $\cdot 10^{-11}$ A/cm^2, pour les échantillons qui sont utilisés. La configuration de test est présenté à la figure 3.20.

Typiquement, une rampe de tension triangulaire (0-100 V a 40 mV/s) est appliquée à l'électrode supérieure et le courant de fuite est mesuré a l'électrode inférieure. L'intervalle de temps moyen entre les pas de 0.4 V est comprise entre 8 (I > 1 pA) à 12 sec ($I < 1$ pA) en fonction du courant mesuré. Le potentiel de l'électrode inférieure et la terre sont fixés à 0 V pour éviter les fuites. Chaque balayage I-V est répété deux fois sur le même dispositif afin de déterminer si un régime de conduction stable est atteint. Les balayages I-V sont également mesurés pour les tensions positives et négatives et en fonction de la température. La température varie de 25°C à 145°C. Elle est limitée à 145°C pour éviter d'endommager les commutateurs MEMS, qui sont sur la même tranche que les échantillons testés.

Les mécanismes de conduction sont identifiés pour chacune des 4 plaques avec SiN_x et SiO_2. Les échantillons d'essai sont des condensateurs MIM, sans aucune modification. Pour chacune des mesures (à l'exception des courbes I-V consécutifs) un échantillon vierge est utilisé.

Pour tous les nitrures SiN_x, une grande hystérésis est observé entre la partie aller et la partie retour de la première courbe I-V. Des courbes consécutives sont décalées vers des tensions plus élevées, ce qui résulte d'une réduction du champ électrique dans le diélectrique en raison du piégeage de charge négative.

Le décalage vers les tensions plus élevées de capa.A et capa.B, où le même type de SiN2 HF est utilisé, ne modifie pas la forme des coubres I-V à fort champ électrique (les traces sont parallèles). A plus faible champ, capa.A tend à avoir une pente moins raide et une plus grande hystérésis, par rapport à capa.B. La pente de la partie aller est très différente pour les capa.C, où du SiN_x MF est utilisé. Ce qui est intéressant est le fait que la pente de la partie retour des courbe I-V est pratiquement la même pour toutes les couches SiN_x, ce qui suggère qu'ils présentent le même mécanisme de conduction une fois que la plupart des pièges sont remplis.

Le mécanisme de conduction dans l'ensemble du SiN_x analysé est identifié comme une conduction Poole-Frenkel. La constante diélectrique obtenue à partir des courbes I-V, est égale à 2,29 (capa.A) et 3,02 (capa.B et capa.C). Ces résultats sont résumés dans le tableau 3.7. Ces valeurs sont beaucoup plus faibles que les valeurs statiques de ϵ_r qui est généralement de 7,5 pour SiN_x stchiométrique . Néanmoins, ces résultats restent en bon accord avec ceux observés pour SiN_x PECVD et l'écart entre la constante diélectrique extraite du modèle Poole-Frenkel et la valeur statique, a été expliquée par l'inexactitude du modèle et l'influence des défauts dans le

matériau.

L'analyse des mécanismes de conduction dans le SiO_2 s'est avérée plus compliquée que dans le cas de SiN_x, principalement en raison d'un courant de conduction très faible (en dessous de 500 fA a 100 V) et un champ de claquage faible, de l'ordre de 3-4 MV/cm.

Le mécanisme de conduction le plus courant dans SiO_2 à des champs électriques élevés (plus de 6 MV/cm) est de type de Fowler-Nordheim [55]. Dans le cas présent, le champ électrique est plus faible, car il ne dépasse pas 4 MV/cm et la forme des courbes I-V ne suit pas la relation de Fowler-Nordheim. Par conséquent, l'hypothèse de la conduction Fowler-Nordheim a été rejetée.

Il y a une hystérésis importante observée entre les parties aller et retour de la courbe IV. Contrairement à la référence [70], dans notre cas, la partie aller n'est pas parallèle à la partie retour et il n'est pas possible de calculer le montant de la charge piégée à partir du décalage de la courbe IV avec une précision satisfaisante.

La forme de la première montée lors du balayage I-V exclut la conduction Schottky et Poole-Frenkel. Cette courbe est plus susceptible d'être expliquée avec le modèle de courant limité par charge d'espace SLCL ("Space-Charge-Limited-Current").

D'autre part la partie aller de la courbe I-V et la partie retour sont des lignes droites quand $\ln(J)$ est tracé en fonction de $\sqrt{E}$. Cela suggère que le mécanisme de conduction est soit de Poole-Frenkel soit de type Schottky. Considérant le fait que la différence de la fonction de travail de sortie pour Al et Pt est de 1,35 eV et le fait qu'il y ait un changement mineur observé entre les courbes I-V pour une tension positive et négative, aucun de ces mécanismes peut être exclu. L'hypothèse de la conduction Poole-Frenkel ou la conduction de Schottky est encore vérifiée par des mesures faites a des températures élevées (mais le bruit est assez élevé). La densité de courant, pour un champ électrique donné, et en fonction de l'inverse de la température, forme une ligne droite (figure 3.26(c)) qui donne accès à une énergie d'activation de 0,78 eV (à partir de la figure 3.26(d)). La constante diélectrique calculée à partir de la pente de la courbe I-V est $\epsilon_{r_{PF}} = 11{,}99$ et $\epsilon_{r_S} = 2{,}99$.

En prenant en compte la valeur connue de la constante diélectrique, la conduction dans SiO_2 est plus susceptible d'être contrôlée par émission Schottky, car la constante diélectrique est plus proche de la valeur statique de $\epsilon_{r_S} = 3.7$. Néanmoins, il est difficile de déterminer explicitement le mécanisme de conduction dans cet échantillon.

Identification de la cinétique du piégeage

Cette section vise à caractériser les propriétés de piégeage des matériaux diélectriques étudiés.

Elle commence avec un modèle, qui montre comment la charge piégée modifie la distribution du champ électrique dans le diélectrique et par conséquent la façon dont elle induit un décalage de la tension appliquée.

Puis elle présente les modèles existants qui décrivent une cinétique de piégeage - l'évolution de la concentration de la charge piégée en fonction du temps pour des conditions de stress spécifiques. Dans cette section, trois mécanismes sont décrits, qui sont le piégeage du premier ordre, le piégeage avec effet répulsif et la génération de pièges.

Dans la partie suivante, les propriétés de piégeage du SiN_x HF, SiN_x MF et SiO_2 MF sont caractérisées. Les échantillons sont stressés par une injection de courant constant et les dérives de tension correspondante sont mesurés. A partir de ces résultats expérimentaux la cinétique de piégeage et les propriétés diélectriques sont extraites.

La cinétique de piégeage est étudiée à partir des injections à courant constant. Les mesures sont effectuées en utilisant un appareil “Agilent 4156C Precision Semiconductor Parameter Analyzer”. Les échantillons sont placés dans une station Cascade Microtech sous atmosphère d'azote sec (HR $< 2\%$). Les connexions entre les dispositifs de test sont réalisées avec des câbles triaxiaux Kelvin. Cette configuration permet de mesurer des courants aussi bas que plusieurs fA, ce qui équivaut à une densité de courant de plusieurs $1 \cdot 10^{-11}$ A/cm^2, pour les échantillons qui sont utilisés.

Lors d'une mesure typique, une densité de courant constante J_{inj} est injectée a partir de l'électrode supérieure dans le diélectrique et le décalage de tension ΔV requis pour maintenir une valeur de J_{inj} constante est enregistrée à intervalles de 10 secondes, pendant un temps maximum de 14 heures. Selon le type d'échantillo6n J_{inj} varie de $5 \cdot 10^{-10}$ A/cm^2 à $1 \cdot 10^{-5}$A/cm^2.

Les injections sont réalisées dans un mode linéaire, ce qui signifie que l'intervalle de temps entre chaque échantillon est le même, dans la gamme de 6-10 sec. Le temps d'intégration, comme dans le cas précédent est fixé à ”long”.

Les propriétés de piégeage sont identifiées pour les 3 types de diélectriques (HF et MF SiN_x et MF SiO_2 sur 4 plaques). Les échantillons d'essai sont des condensateurs MIM. Pour éviter les courants de fuite à travers le substrat à la terre via le pad de test, le lien électrique entre le pad de test et l'électrode supérieure est retiré. Pour chaque injection à courant constant, un échantillon vierge est utilisé.

Les résultats typiques d'une injection à courant constant sont un tracé d'une dérive de tension ΔV en fonction de la charge injectée N_{inj}. Les résultats sont tracés dans une échelle logarithmique pour tous les échantillons. Pour chacune des courbes mesurées, la dérive de tension a deux pentes. La première pente plus raide n'est pas pertinente du point de vue de l'étude de la cinétique de piégeage de charge, car elle correspond à la charge d'un condensateur MIM avec un courant constant. C'est la deuxième pente (moins raide) qui est significative de la cinétique de piégeage par ajustement avec le modèle exponentiel ou le modèle logarithmique.

L'effet de la température sur les injections à courant constant est présenté à la figure 3.29, où les injections sont effectuées sur les échantillons capa.C, pour 25°C, 75°C et 125°C.

Les dérives mesurées montrent une ligne droite avec une pente comparables lorsque elles sont tracées dans la double échelle logarithmique, quelle que soit la température. La seule différence entre ces dérives est leur augmentation pour des températures plus élevées.

Il y a deux explications possibles à cette observation. La première correspond au fait que le processus de conduction Poole-Frenkel est facilité par une température plus élevée. Par conséquent, le même niveau de l'injection de courant, a une température plus élevée, peut être obtenu pour une tension inférieure appliquée (champ électrique plus modéré dans le diélectrique). Le second correspond a un changement des propriétés du piégeage, car l'augmentation de température favorise la réémission thermique et il induit une modification de σ^*, ce qui induit à son tour une évolution vers de plus petites dérives de tension.

Les résultats obtenus pour les trois échantillons sont bien reproduits par le modèle logarithmique. Pour calculer les paramètres de piégeage, le barycentre de la charge est fixé arbitrairement au milieu du diélectrique, comme il n'est pas possible de le déterminer avec les dispositifs de test disponibles.

Les premières injections à courant constant, se traduisant par une dérive de tension en fonction de la charge injectée, permettent d'extraire les paramètres densité de pièges N_t^* et section efficace de capture effective σ^* en fonction du champ électrique moyen dans le diélectrique (figure 3.31 (a, b) pour capa.A, (c, d) capa.B et (e, f) pour capa.C).

La tension initiale est obtenue à partir des courbes I-V correspondant à un courant de fuite égal à l'injection de courant. Cette tension est ensuite soustraite de l'injection à courant constant, pour obtenir la dérive de tension.

Pour capa.A dans la gamme des champs électriques de 1,9 à 2,5 MV/cm, la valeur de N_t^*= 1,5 ± 0,2 $\cdot 10^{11}$ cm^{-2} est a peu prés indépendante de E_d. La valeur de σ^* est fortement dépendante du champ et elle est baisse de façon exponentielle avec E_d, variant de 10^{-14} à 10^{-15}cm^2.

Pour capa.B dans la gamme des champs électriques de 1,9 à 3,7 MV/cm, la valeur de N_t^* = 2,3 ±0,2$\cdot 10^{11}$ cm^{-2} est a peu prés indépendante de E_d. La valeur de σ^* est fortement dépendante du champ et elle est baisse de façon exponentielle avec E_d de 10^{-12} à 10^{-17} cm^2.

Pour l'échantillon capa.C, N_t^* = 0,9$\cdot 10^{12}$ cm $^{-2}$ (presque 5 fois plus élevée, comparativement à capa.B). Contrairement à capa.A et capa.B la valeur de N_t^* augmente légèrement avec E_d, passant de 0,9 $\cdot 10^{12}$ cm^{-2} à 2,0$\cdot 10^{12}$ cm^{-2}. La valeur de σ^* est décroissante de façon exponentielle avec E_d, de 10^{-11} à 10^{-15} cm ^{2}, comme dans le cas d'autres échantillons SiN_x.

Pour résumer, les échantillons de nitrures avec PECVD HF et MF sont tous bien modélisés par la cinétique de piégeage logarithmique, le plus probable étant qu'elle corresponde au processus de piégeage à effet répulsif. Le plus faible nombre de pièges est trouvé pour l'échantillon capa.A (SiN HFx) et le plus élevé pour l'échantillon capa.C (SiN MFx). La concentration en surface totale de pièges montrent une dépendance faible avec le champ électrique moyen dans le diélectrique. D'autre part la section efficace de capture décroît exponentiellement avec le champ électrique moyen. Cette observation peut s'expliquer par le fait que la probabilité de piégeage (la section efficace de capture) décroît exponentiellement lorsque le niveau d'énergie du centre est plus profond [86], ainsi que que donné par l'équation 3.45.

A la fin, il convient de noter que ces paramètres sont extraits pour des champs électriques qui sont plus élevés que ceux qui prévalent dans le commutateur pendant son fonctionnement normal. Ceci est imposé par la contrainte que pour les bas champs électriques le courant de fuite est inférieur à la valeur minimale mesurable, de 1 fA.

La figure 3.32 (a) présente les dérives de tension, tracées avec une double échelle logarithmique. Elles sont beaucoup plus rapides comparées à celles mesurées pour l'ensemble des couches SiN_x. Dans ce cas, les courbes d'injection de courant constant sont mieux modélisées en utilisant le modèle exponentiel.

Les paramètres de piégeage, qui sont la concentration de surface totale de pièges et de la section efficace de capture sont presque indépendants de E_d, ce qui est cohérent avec le modèle de piégeage du premier ordre.

La concentration totale de piège est de 1,7 ± 0,4 $\cdot 10^{13}$ cm^{-2} et la section efficace de capture est égale à $\sim 10^{-15}$ cm^2. Comparativement à un oxyde thermique, le nombre de pièges est plus élevé et la section efficace de capture se trouve être assez grande pour le SiO_2 PECVD.

Conclusions

Trois types de diélectriques PECVD utilisés dans les commutateurs RF MEMS ont été analysés dans ce chapitre. Ces diélectriques sont SiN_x PECVD de fréquences élevée ou mixte déposés à 300°C et SiO_2 PECVD de fréquence mixte déposé à 150°C.

Un certain nombre de techniques expérimentales ont été utilisées avec succès pour déterminer la structure et la composition des couches diélectriques des commutateurs RF MEMS de type capacitif. Les observations au microscope TEM ont révélé que tous les diélectriques étudiés (le HF et MF SiN_x et MF SiO_2) sont amorphes à cause de la basse température de dépôt.

Pendant le dépôt des couches diélectriques, les particules de l'électrode inférieure sont redéposés dans le diélectrique et créent des agrégations cristallines à proximité de l'électrode inférieure. En particulier, Pt est présent dans tous les films étudiés, apparaissant sous la forme de nodules cristallins intégrés dans le diélectrique au voisinage immédiat de l'électrode inférieure en Pt. Les spots sont situés à une distance de 2-10 nm de la surface de l'électrode et ont un diamètre de 2-5 nm. Les mesures de RBS, NRA et ERDA montrent que les couches HF PECVD SiN_x sont riches en Si, avec un rapport N/Si égal à 0,74, tandis que le SiN_x PECVD MF est presque stoechiométrique avec un ratio N/Si égal à 1,16. Le SiO_2 s'avère être non stchiométrique avec un rapport O/Si égal à 0,81.

Les mesures RBS et ToF-SIMS confirment que les deux couches SiN_x HF et MF sont fortement hydrogénées, car elles contiennent environ 23 at. % de H, comme prévu pour les nitrures à basse température. Les mesures EDS et ToF-SIMS révèlent également une quantité considérable de O dans ces diélectriques. D'autre part le SiO_2 MF PECVD contient peu de H, mesuré à 3,4 at.%.

Les profils en profondeur par ToF-SIMS montrent que des traces d'Al et Pt sont présentes pour tous les diélectriques et cela sur toute l'épaisseur. Des traces de K, Na et C sont aussi identifiées à l'interface diélectriques - électrode inférieure. La conclusion de l'analyse ToF-SIMS pour les couches SiN_x est que les profils de contamination sont similaires, malgré des conditions de dépôt et des temps de stockage différents, ce qui favorise l'hypothèse que les contaminations présentes dans ces diélectriques ne sont pas intrinsèques, mais sont dues au processus de fabrication, qui est identique pour ces échantillons (à l'exception de la phase de dépôt du diélectrique). Pour le SiO_2 les mêmes éléments que pour le SiN_x ont été détectés.

Ces matériaux ont été soumis aux mêmes tests électriques pour déterminer le mécanisme de conduction et les propriétés de piégeage.

Le mécanisme de conduction dans le SiN_x HF et MF PECVD est identifié comme étant un mécanisme de type émission Poole-Frenkel, tandis que pour le SiO_2 MF PECVD, il est plus susceptible d'être du type émission Schottky.

Les courbes I-V pour tous les diélectriques étudiés montrent une grande hystérésis entre la partie aller et retour de la première courbe I-V. Cette hystérésis est réduite par balayages consécutifs I-V. Pour un courant fixe, le I-V se déplace vers des tensions plus élevées, ce qui révèle qu'une charge négative est piégée dans le volume du diélectrique et qu'elle modifie le champ électrique interne.

La cinétique de piégeage identifiée dans les couches PECVD SiN_x correspond à un modèle de piégeage logarithmique avec effet répulsif des charges piégées, tandis que dans le SiO_2, le modèle exponentiel de piégeage du premier ordre est plus adapté. Les concentrations totales de pièges par unité de surface ne peuvent donc pas être comparés directement entre le SiN_x et le SiO_2, car des modèles différents sont utilisés. Au sein du groupe des nitrures SiN_x, les concentrations totales de pièges les plus basses sont mesurées pour les SiN_x HF, qui ont le courant de fuite le plus élevé (pour un champ électrique donné).

Chapitre 4

La fiabilité et la modélisation de la durée de vie

Ce chapitre présente les tests de la fiabilité à long terme des commutateurs RF MEMS actionnés électrostatiquement.

La première partie de ce chapitre vise à caractériser le comportement à long terme des commutateurs RF MEMS de type capacitif et ohmiques fabriqués par le CEA-Leti. Cette partie commence par une présentation de la méthode de test et des échantillons suivie par la synthèse des résultats des tests, tels que des dérives tension pull-in mesurée lors de stress à tension constante, et où la contrainte de tension est appliquée pendant plusieurs heures (en général 6 a 25 h), pour différents niveaux de tension.

La deuxième partie de ce chapitre présente la modélisation du chargement du diélectrique dans les commutateurs RF MEMS. Ce paragraphe présente notre modèle physique d'accumulation de charge parasite dans un diélectrique, qui est une nouvelle approche pour la modélisation des dérives de tension pull-in dans les MEMS RF. Ce modèle est utilisé pour simuler les dérives de tension pour les commutateurs capacitifs et ohmiques qui ont été caractérisés dans la première partie de ce chapitre. Le modèle est vérifié en comparant les dérives de tension simulées et expérimentales. Après une vérification positive du modèle, ce dernier est utilisé pour étudier l'influence du matériau diélectrique et de la géométrie sur les dérives de tension.

Caractérisation de la fiabilité des commutateurs RF MEMS

Dans la première partie de ce chapitre, nous caractérisons le comportement à long terme (durée de vie) de certains commutateurs RF MEMS de types capacitif et ohmique. Ces caractérisations sont effectuées en mesurant les dérives de la tension pull-in en fonction du temps, pour différents niveaux d'un stress à tension constante (CVS).

Il a été démontré dans cette partie que la dérive de la tension de pull-in est un facteur limitant la durée de vie des commutateurs RF MEMS. Le stress de tension peut décaler la courbe CV des commutateurs actionnés électrostatiquement, si bien que la tension de pull-in V_{pi} peut dépasser la tension appliquée V_{app}, avec pour conséquence la défaillance du commutateur, car il reste alors en position ouverte quand on veut l'actionner.

Les mesures montrent que tous les commutateurs, indépendamment de la couche diélectrique utilisée et du type de commutateur, sont concernés par le problème de chargement du diélectrique.

Les tests de stress à tension constante peuvent être simplement accélérés en augmentant la tension appliquée. En agissant ainsi les dérives de tension mesurées sont plus rapides et peuvent atteindre des valeurs élevées, mais le mécanisme de la cinétique de dérive reste inchangé. La contrainte de tension maximale applicable est limitée par le champ de claquage des diélectrique étudiés.

L'influence du matériau diélectrique sur les dérives mesurées de la tension de pull-in est plus facile à analyser dans le cas des commutateurs de type capacitif qui ont la même géométrie, y compris la surface et l'épaisseur du diélectrique. Lorsque nous comparons les résultats pour SiN_x et SiO_2, nous pouvons conclure que les dérives de tension sont plus élevées pour les dispositifs avec SiN_x. Si l'on compare les différents nitrures SiN_x, celui déposé en mode mixte de fréquence (MF) montre des dérives supérieures par rapport à celui déposé à haute fréquence (HF). L'influence de

la géométrie des commutateurs est comparé pour les commutateurs ohmiques ohm.A et ohm.C, où la même couche HF SiN_x est utilisée. Ces échantillons montrent des dérives de tension différentes, ils présentent tout de même une nature similaire du processus de piégeage, avec des dérives de tension linéaires pour des tracés en double échelle logarithmique. De cette observation, on peut conclure que le type de matériau et ses propriétés diélectriques définissent la nature du processus de piégeage, tandis que la géométrie du commutateur peut avoir un effet sur l'ampleur de la dérive de tension observée.

Modélisation du chargement du diélectrique pour les MEMS RF

Cette section se concentre sur la modélisation des phénomènes de chargement du diélectrique dans les commutateurs RF MEMS. Il commence par un bref examen critique des modèles présentés dans la littérature. Ensuite, nous présentons et discutons notre modèle d'accumulation de charge parasite. Finalement, ce modèle est utilisé pour calculer les dérives de tension théorique pour les commutateurs de type capacitif et ohmique avec SiN_x PECVD HF et SiO_2 MF et HF, qui sont ensuite comparées avec celles mesurées. Enfin, le modèle est utilisé pour étudier l'influence du matériau diélectrique et de la conception du commutateur sur les dérives de tension mesurée.

Dans cette partie, nous présentons notre propre modèle de piégeage de charge dans la couche diélectrique des commutateurs RF MEMS capacitifs et ohmiques. Ce modèle utilise les propriétés diélectriques, qui ont été extraites dans le chapitre précédent, pour modéliser la dérive de tension des commutateurs RF MEMS. L'approche qui a été utilisée pour calculer la dérive de la tension pull-in des commutateurs RF MEMS est présentée ci-dessous.

Dans le modèle proposé, il est considéré que lors d'un stress de tension une charge parasite est piégée dans le diélectrique, ce qui réduit le champ électrique dans ce dernier. Pour compenser cette baisse du champ électrique, il est nécessaire d'appliquer une tension plus élevée pour abaisser la poutre. Par conséquent, le changement de la tension de pull-in est directement lié à la réduction du champ électrique due à la charge piégée.

Le modèle d'accumulation de charge en fonction du temps pour une tension constante appliquée V_{app} est basé sur le modèle de Wibbler, où la réduction du champ électrique dans le diélectrique ΔE en raison de la quantité de charge ΔN_t piégés pendant une période de dt est donnée par les équations 4.16. Pour nos besoins, cette équation peut être réécrite sous la forme simplifiée 4.31.

En pratique, le modèle de piégeage de charge dans la couche diélectrique d'un commutateur en fonction du temps et du stress est un modèle numérique itératif qui est calculé selon l'algorithme présenté à la figure [ref figure].

A chaque itération, la quantité de charge piégée Δn_t sur une période de Δ_t est calculée. Cette charge piégée est supposé réduire le champ électrique initial E_{s0} d'une valeur ΔE_{s_i}. La description détaillée de chaque itération est fournie ci-dessous:

1. *Définition du champ de stress nominal E_d*
   Au début, nous définissons le champ nominal électrique correspondant à la contrainte de tension appliquée qui est calculé comme $E_d = V_{app}/t_d$.

2. *Initialisation des variables Δt, t_{fin}, t_0 et ΔV*
   Dans cette étape nous introduisons l'incrément de temps Δt, le temps de contrainte totale t_{fin} et nous avons initialisé les variables t_0 et ΔV.

3. *Calcul du champ électrique effectif dans le diélectrique d'un commutateur*
   Pour la même tension appliquée et la même épaisseur du diélectrique, le champ électrique dans un commutateur est inférieur à celui présent dans une structure MIM. Le champ électrique dans un commutateur est obtenu à partir du ratio entre sa capacité et celle de la structure MIM-, en utilisant la formule suivante: $E_s/E_d = C_s/C_d$.

4. *Détermination de la densité de courant J_{inj}*
   Dans la première étape de l'itération, nous déterminons la densité du courant d'injection, ce qui correspond à un champ électrique effectif E_{s_i} obtenu à partir des modèles de conduction.

5. *Détermination des paramètres de piégeage, concentration de pièges disponibles N_{t_i} et leur section efficace de capture σ_i*
   Dans la deuxième étape de l'itération, nous déterminons la concentration de pièges disponibles N_{t_i}, qui est réduite à chaque itération par la charge déjà piégée et la section de capture efficace σ_i. La concentration de pièges N_{t_i} montre une faible dépendance avec le champ SiN_x MF, ou elle est constante pour SiN_x HF et SiO_2 MF. La section efficace de capture dépend du champ comme décrit précédemment pour SiN_x, ou est constante pour SiO_2.

6. *Calcul de la charge piégée lors d'une itération*
   Dans la deuxième étape, nous calculons la quantité de charge N_{t_i} piégés sur une période de temps Δt, ce qui est obtenu à partir des équations 3.33 et 3.34 pour le modèle de piégeage de premier ordre (exponentiel) et les équations 3.38 et 3.39 pour le modèle de piégeage logarithmique avec effet répulsif.

7. *Réduction du champ due à la charge piégée Δe_i*
   Dans la troisième étape, la réduction du champ électrique ΔE_{s_i} due à la charge piégée est calculée, qui correspond a un décalage de tension ΔV_{pin_i}

8. *Calcul du nouveau champ électrique effectif à travers le diélectrique $E_{s_{i+1}}$*
   Dans la quatrième étape de l'itération, nous calculons le champ effectif électrique a travers le diélectrique de $E_{s_{i+1}}$ qui est égal a la valeur précédente du champ électrique E_{s_i} réduite de la contribution de la charge piégée.

Pour résumer, les paramètres d'entrée qui sont nécessaires dans ce modèle sont l'injection de courant J_{inj}, les paramètres décrivant les propriétés de piégeage N_t (N_t^*) et σ (σ^*) et la position du barycentre des charges $\bar{x}$, qui ont été déterminés dans le chapitre 3.

Validation du modèle

Dans cette partie nous comparons les dérives de tension expérimentales qui ont été mesurées au début de ce chapitre avec celles qui sont obtenues à partir du modèle proposé. La comparaison est faite pour trois diélectriques: SiN_x HF PECVD (capa.B, ohm.A et ohm.C), SiN_x MF PECVD (capa.C), SiO_2MF PECVD (capa.D) et pour les deux types de conception de commutateur: capacitif et ohmique.

La tableau 4.2 résume les propriétés diélectriques et paramètres principaux de chaque échantillon analysé dans ce chapitre, et qui sont nécessaires à la modélisation.

La figure 4.10 présente une comparaison des dérives expérimentales et simulées de tension pour les commutateurs de type capacitif.

Comme il a été mentionné auparavant, le retour de la courbe I-V a été recalé d'une valeur de ΔV_C, cette courbe recalée correspondant à la courbe I-V théorique sans piégeage. Cette dernière est ensuite utilisée pour calculer les dérives de tension pour tous les niveaux de stress. Il est remarquable que cette unique courbe I-V recalée, utilisée comme paramètre d'entrée du modèle, permette de parfaitement reproduire l'ensemble des dérives expérimentales, quelle que soit la valeur de tension de stress appliquée. Ceci renforce fortement la plausibilité et la pertinence de l'approche développée.

Les résultats simulés pour tous les diélectriques demeurent en bon accord avec les résultats expérimentaux, tant en terme de valeur maximale de dérive de tension que de cinétique de piégeage.

L'échantillon de la couche capa.B SiN_x HF montre une dérive de tension plus faible que la couche capa.C SiN_x MF, ce qui est le résultat attendu si l'on tient compte du fait que la concentration de pièges de l'échantillon capa.C est être plus élevée. D'autre part, il est intéressant de remarquer qu'une dérive de tension plus élevée pour la capa.C (SiN_x MF) est observée, malgré le fait que le courant d'injection est plus faible pour cet échantillon.

Il est à noter qu'un tel résultat ne pourrait en aucun cas être obtenu à partir du modèle proposé par Melle, puisque dans ce modèle, plus les courants de fuite sont importants, plus les dérives de tension le sont également. Notre expérience montre que ce n'est pas toujours vrai. Ceci s'explique par le fait que capa b a une plus faible concentration de pièges, ce qui limite la dérive de tension maximale, et la section efficace de capture est aussi plus faible, impliquant une plus faible probabilité de piégeage de charge. On peut conclure que l'approche correcte pour la modélisation des dérives de tension dans les commutateurs RF MEMS ne peut pas se limiter à analyser des fuites de courant seulement, mais qu'elle doit nécessairement inclure l'identification des propriétés des pièges.

Les mesures de tension de l'échantillon montrent des dérives inférieures pour capa.D par rapport aux échantillons avec SiN_x. Ces résultats confirment que les concentrations de pièges extraites à partir des modèles logarithmiques et exponentiels ne sont pas directement comparables, puisque dans le cas du SiO_2 les dérives de tension maximale sont plus faibles, comparativement aux échantillons avec nitrure SiN_x, où la valeur absolue de N_t^* est inférieure au Nt trouvé pour SiO_2.

Comme les résultats expérimentaux et modélisés ne montrent pas ou peu de décalage, pour les modèles à la fois logarithmiques et exponentiels, on peut conclure que l'approche générale proposée pour le calcul des dérives de tension dans les commutateurs RF MEMS sous contrainte de tension constante est appropriée, et l'utilisation de la rampe IV décalée est pertinente.

Le modèle démontre qu'il est possible de modéliser le comportement à long terme des commutateurs RF MEMS (l'évolution de la dérive de tension) sur la base des propriétés physiques des couches diélectriques qui ont été utilisées. Il montre également que les dérives de tension de pull-in ne sont pas seulement dépendantes du courant de fuite, mais aussi de la cinétique de piégeage. En particulier, des échantillons avec des courants de fuite plus faible (pour un champ électrique donné) peuvent montrer des dérives de tension plus élevées, si par exemple le nombre de pièges disponibles est plus important.

Pour simuler les dérives de tension pour les commutateurs de type ohmique les propriétés du SiN_x PECVD HF extraites à partir des plaques de commutateurs capacitifs sont utilisées. En pratique, seul le recalage de la courbe I-V initiale a été ajusté pour ces simulations (épaisseurs

différentes du diélectrique).

La Figure 4.11 présente une comparaison des résultats simulés et expérimentaux pour les échantillons ohm.A et les échantillons ohm.C.

Comme dans le cas des commutateurs de type capacitif, les dérives de tension obtenues à partir du modèle sont en bon accord avec les résultats expérimentaux. Ces résultats montrent un fort effet de la géométrie sur l'accumulation de charge dans la couche diélectrique.

La plaque ohm.A sans "hillocks" montre des dérives de tension plus élevées que la plaque ohm.C avec "hillocks". Comme précisé précédemment, le plus faible entrefer entre les électrodes cause un champ électrique supérieur dans le diélectrique pour la même tension appliquée. Dans le cas de ces deux échantillons, cet entrefer dépend de la rugosité de l'électrode. Par conséquent, le champ électrique dans le diélectrique est beaucoup plus élevé dans l'échantillon ohm.A par rapport à l'échantillon ohm.C, lorsque la même tension nominale est appliquée. On peut conclure que l'augmentation de l'entrefer entre l'électrode et le diélectrique à l'état fermé contribue a une réduction significative du champ électrique dans le diélectrique, avec pour conséquence une densité d'injection nettement plus faible et donc des dérives de tension plus lentes.

Conclusions

Dans ce chapitre, le comportement à long terme de commutateurs RF MEMS avec trois types de diélectriques PECVD et de deux conceptions différentes a été analysé. Les diélectriques étudiés comprenait des nitrures PECVD haute-fréquence et fréquences mixtes déposés à 300°C et des oxydes SiO_2 PECVD déposés a 150°C. Des variantes dans la géométrie des commutateurs ont été examinées pour le type ohmique (avec et sans "hillocks").

Au début de ce chapitre, il a été démontré que la dérive de la tension de "pull-in" est un facteur limitant la durée de vie dess commutateurs RF MEMS. La tension appliquée entre les électrodes d'actionnement crée un champ électrique élevé dans le diélectrique, ce qui provoque injection et accumulation de charges parasites. La présence de la charge parasite dans le diélectrique d'un commutateur MEMS actionné électrostatiquement se traduit par une dérive des courbes C-V.

Les mesures de tension de dérive ont été menées sur les commutateurs capacitifs et ohmiques. Les mesures montrent que tous les échantillons étudiés sont touchés par le problème de l'accumulation de charge parasite dans le diélectrique. Les dérives de tension sont dépendantes du niveau de stress de tension constante et de la géométrie du commutateur. Les tests de fiabilité des commutateurs RF MEMS peuvent être ensuite accélérés en augmentant la tension, mais la tension maximale applicable est limitée par le champ de claquage du diélectrique. Pour le type capacitif, les dérives de tension élevées sont observées pour les dispositifs avec SiN_x plutôt qu'avec SiO_2.

L'analyse des commutateurs ohmiques révèle que l'espacement entre les électrodes supérieure et inférieure à l'état fermé peut avoir une influence significative sur les dérives de tension, ceci étant du au champ électrique. Un entrefer plus grand dans l'état bas correspond à un champ électrique plus faible dans le diélectrique, ce qui entraîne une baisse d'injection de courant qui se traduit par moins de charges piégées et donc moins de dérive de tension.

Le modèle présenté a donc été vérifié expérimentalement et s'avère prédictif. On peut conclure que les dérives de tension mesurée pour les commutateurs MEMS dépendent des propriétés du diélectrique et de la géométrie du commutateur. Les propriétés du diélectrique qui ont un impact sur les dérives de tension sont les courants d'injection (fuite) combinés avec les caractéristiques des centres-pièges, typiquement le nombre total de pièges disponibles ainsi que la section efficace de capture. L'injection de courant et la section efficace de capture définissent la

cinétique de piégeage de charge, tandis que la concentration totale de pièges définit la tension de dérive à saturation.

Chapitre 5

Conclusions

Cette thèse résume les travaux concernant les essais de fiabilité des commutateurs RF MEMS capacitifs et ohmiques développé par le CEA-Leti en collaboration avec des partenaires industriels.

Le premier chapitre explique le comportement électrique des commutateurs RF MEMS en fonction de leur géométrie. Pour atteindre cet objectif, la première partie présente un modèle mécanique original utilisé pour calculer la raideur des commutateurs de type ohmique. Les valeurs théoriques de raideur sont comparées avec celles mesurées expérimentalement par la technique de nano-indentation sur des commutateurs MEMS réels. Les mesures de raideur sont complétées par des observations AFM, MEB et FIB. Tous ces éléments sont utilisés avec succès pour expliquer le comportement électrique des différents lots de commutateurs de type ohmique.

Le deuxième chapitre présente les résultats de la caractérisation des propriétés structurales et physiques des diélectriques, qui sont généralement utilisés dans nos commutateurs RF MEMS ohmiques et capacitifs. Il est intéressant de remarquer que ces études sont réalisées soit sur des commutateurs réels (structures AIM), soit sur des structures de test (structures MIM) qui ont la même séquence d'empilement et qui sont fabriquées en utilisant le même procédé.

Les analyses élémentaires confirment que tous les nitrures SiN_x fabriqués par la technique PECVD ont une qualité inférieure par rapport à leurs homologues synthétisés à haute température, car ils sont non-stchiométriques et ont une grande quantité d'hydrogène incorporée dans la masse du SiN_x. Des contaminations similaires se retrouvent dans le SiO_2, qui montrent que les impuretés sont introduites au cours du processus de fabrication plutôt que pendant le stockage ou le fonctionnement des dispositifs. Il n'y a pas de variations significatives observées entre les plaques analysées. Il en est conclu que la dérive de tension mesurée sur des commutateurs RF MEMS ne dépend pas des ions présents dans le diélectrique mais plutôt des mécanisme de conduction et des propriétés du piégeage électronique.

Les mécanisme de conduction sont identifiés dans SiN_x et SiO_2 PECVD en mesurant des courbes I-V sur les condensateurs MIM. Pour les deux nitrures SiN_x, qui sont déposés en haute (HF) et fréquence mixte (MF), le mécanisme de conduction est contrôlé par le volume. Il est de type Poole-Frenkel. Pour le SiO_2 le mécanisme de conduction est plus susceptible d'être contrôlé par émission Schottky.

Les mesures I-V révèlent que tous ces matériaux piègent des charges parasites, il y a en effet une forte hystérésis entre les parties aller et retour de la courbe I-V. Il est démontré que le piégeage de la charge parasite réduite le champ électrique initial dans le diélectrique, ce qui conduit à une baisse significative du courant de fuite. En particulier, le piégeage de charge est visible en tant que décalage parallèle des courbes I-V pour un courant spécifique, et ce changement peut être efficacement utilisé pour calculer la charge piégée correspondante. Ceci impose des précautions dans l'interprétation des courbes I-V. Dans la présente étude, le temps de mesure d'une seule courbe I-V est supérieur à 1 heure car les courants à mesurer sont très faibles, d'où un long temps de mesure. Par conséquent, un certain nombre de pièges sont remplis et à tension donnée, le champ électrique dans le diélectrique est modifié au cours de la mesure. En conséquence, même la première courbe I-V mesurée est déplacée vers des tensions plus élevées par rapport à la courbe d'origine I-V 'sans pièges chargés". Idéalement, il faudrait arriver à faire des mesures suffisamment vite pour obtenir des courbes I-V non affectées par la charge piégée.

Pour étudier la cinétique de piégeage de charge des condensateurs MIM sont utilisés, ils présentent le même empilement que les commutateurs MEMS réels. Le choix des dispositifs tests limite le nombre de techniques disponibles pour étudier le piégeage de charge car aucune analyse de type MOS n'est possible. Pour identifier les propriétés des pièges la technique d'injection à courant constant est utilisée. La densité de pièges par unité de surface et la section efficace de capture sont extraites grâce a des modèles exponentiels et logarithmiques, qui permettent aussi de simuler la cinétique de piégeage. Il est à noter que c'est une approche originale pour étudier le comportement des MEMS RF. Les propriétés de piégeage de tous les types de matériaux étudiés sont identifiées. Le diélectrique SiN_x PECVD montre une dépendance logarithmique de la cinétique de piégeage, tandis que le SiO_2 montre une dépendance exponentielle. La concentration totale de pièges ne montre aucune dépendance pour les SiN_x HF et SiO_2 MF, ou une dépendance faible en fonction du champ pour le SiN_x MF. La section efficace de capture dépend du champ pour les deux types de nitrures, ce qui est cohérent avec le modèle de piégeage à effet répulsif. Pour le SiO_2, où un modèle de piégeage du premier ordre a été utilisé, la section efficace de capture est indépendante du champ.

Les propriétés diélectriques déterminées dans le chapitre 3 pour trois matériaux diélectriques différents forment la base de la modélisation de la dérive de la tension mesurée sur les commutateurs de type capacitif et ohmique, qui est présentée au chapitre 4. Dans ce chapitre, les dérives de tension expérimentales sont mesurées lors des tests de stress à tension constante, pour différents niveaux de contrainte de tension. Ces mesures couvrent tous les types de matériaux étudiés (SiN_x PECVD HF et MF et SiO_2 MF), les types de commutateur (ohmique et capacitif) et la géométrie de commutateur (avec et sans "hillocks"). Il s'avère que les valeurs maximales de dérive de tension sont différentes pour un matériau diélectrique et un design différents des commutateurs. Pour tous les échantillons, le niveau de tension de stress est un facteur d'accélération. Le niveau de stress maximal applicable est limité par le champ du claquage du diélectrique.

La deuxième partie de ce chapitre présente brièvement les modèles antérieurs, qui ne parviennent pas a expliquer les dérives de tension mesurée en terme de propriétés physiques des matériaux diélectriques. Dans la partie suivante, nous proposons une approche originale de modélisation de la dérive de la tension de "pull-in" basée sur le mécanisme de conduction et les propriétés de piégeage des diélectriques. Nous démontrons que grâce a notre modèle, il est possible d'expliquer les dérives de tension mesurée en termes de propriétés diélectriques bien identifiées. Il s'avère, cependant nécessaire d'améliorer la méthode de mesure des courbes I-V pour identifier la courbe I-V initiale non affectée par la charge déjà piégée lors du premier balayage. Dans ce travail, cette courbe "vierge" a été obtenue en recalant la courbe I-V de manière à ce que le modèle donne une bonne prédiction des dérives de tension, le même décalage étant utilisé comme paramètre d'entrée dans la modélisation de tous les stress, indépendamment de la tension appliquée. Cette procédure donne des résultats simulés en bon accord avec les mesures pour tous les matériaux, et permet de prédire les résultats de n'importe quelle séquence de vieillissement électrique.

Nous utilisons ensuite notre modèle pour étudier l'effet des propriétés diélectriques et de la conception du commutateur sur le comportement à long terme de nos commutateurs MEMS.

Il s'avère que le facteur qui a le plus d'influence sur le comportement a long terme est la concentration de pièges, qui définit la dérive de tension maximale. Les autres facteurs, tels que la section efficace de capture ou le champ électrique dans le diélectrique, influent uniquement sur la cinétique de la dérive de tension, c'est à dire la vitesse à laquelle les pièges disponibles sont remplis.

Enfin, on peut conclure que le modèle présenté propose une meilleure compréhension du mode de défaillance du diélectrique et de son chargement, et a un fort potentiel pour être utilisé aux fins d'évaluer le vieillissement électrique et le comportement a long terme des commutateurs RF MEMS, en fonction de leur géométrie et des propriétés du diélectrique utilisé.

Le modèle présenté montre que le comportement a long terme des MEMS RF dépend des propriétés électriques de l'isolant. Il nous suggère de mener, à l'avenir, une étude systématique des propriétés diélectriques des matériaux en fonction des paramètres de dépôt, ceci afin de sélectionner les candidats les plus appropriés pour les commutateurs MEMS RF. A ce stade, il peut également être utilisé pour analyser dans quelle mesure des variantes dans les procédés de fabrication peuvent influencer les propriétés des diélectriques et le comportement lors de la commutation.

En optimisant les propriétés diélectriques et la conception interrupteur (diminution du champ électrique, par exemple), il devrait être possible de fabriquer un commutateur avec une durée de vie largement prolongée par rapport aux dispositifs actuellement étudiés.