Dispositifs innovants à pente sous le seuil abrupte : du TEFT au Z^2-FET

Jing Wan

UNIVERSITÉ DE GRENOBLE

THÈSE

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ DE GRENOBLE

Spécialité : **Nanoélectronique et Nanotechnologies**
Arrêté ministériel : 7 août 2006

Présentée par

Jing WAN

Thèse dirigée par **Sorin CRISTOLOVEANU** et
codirigée par **Alex ZASLAVSKY** et **Cyrille LE ROYER**

préparée au sein des **Laboratoire IMEP-LAHC et CEA-LETI**
dans **l'École Doctorale EEATS**

Dispositifs innovants à pente sous le seuil abrupte: du TFET au Z^2-FET

(Innovative sharp switching devices: from TFET to Z^2-FET)

Thèse soutenue publiquement le **23 Juillet 2012**,
devant le jury composé de :

M. Amara AMARA
Professeur, Institut Supérieur d'Electronique de Paris (Président, Rapporteur)
M. Philippe GALY
Ingénieur Recherche, STMicroelectronics (Rapporteur)
M. Jean-Luc AUTRAN
Professeur, Université d'Aix-Marseille (Membre)
M. Sorin CRISTOLOVEANU
Directeur de Recherche CNRS, CNRS (Membre)
M. Alexander ZASLAVSKY
Professeur, Brown University, USA (Membre)
M. Cyrille LE ROYER
Ingénieur Recherche, CEA-LETI (Membre)

Acknowledgement

I have enjoyed my Ph.D. study for three years in France, during which I have acquired not only enormous knowledge in scientific research but also unforgettable experiences in living here. Without the help from so many nice and kind people, it is not easy for me to get adapted in a foreign country, especially this is my first step out of my home (China).

I give my great appreciation to the “Nanoscience Foundation” for not only their financial and scientific support on this thesis but also their help on my accommodation in France.

I would like to address my thanks to my Ph.D. supervisors, Prof. Sorin Cristoloveanu in IMEP-LAHC and Prof. Alex Zaslavsky in Brown University, for not only their patient guidance and inspiration on this work but also their enthusiastic helps in improving my writing and presentation skills. I also would like to thank them for kindly helping me on my job searching. Working with them is an enjoyment for not only their profound knowledge on semiconductors but also their strong sense of humor.

I also want to express my gratitude to my Ph.D. co-supervisor Dr. Cyrille Le Royer in CEA-LETI. His vast knowledge in device fabrication is a solid base for this work. Without him, our work can not be done. I am also impressed by his hospitality to me. I still remember that my first lunch in France is invited by him.

I am also grateful to engineers working in IMEP-LAHC and CEA-LETI: Xavier Mescot in IMEP-LAHC, Jacque Cluzel in CEA-LETI and Alexandre Chagoya in CIME, for their great supports on our experiments.

Thanks also to Prof. Amara Amara from Institut Supérieur d'Electronique de Paris (ISEP), Dr. Philippe galy from STMicroelectronics and Prof. Jean-Luc Autran from Université d'Aix-Marseille for their kindly acceptation of our invitation as the reviewer and jury member for this thesis.

Finally, I have to thank all my families, especially my wife Cuiqin Xu, for their persistent support and encouragement to me.

Abstract/ Résumé

Title: Innovative sharp switching devices: from TFET to Z^2-FET

This thesis is dedicated to studying sharp switching devices, including the tunneling field-effect-transistor (TFET) and a new feedback device we have named the Z^2-FET, for low power logic and memory applications compatible with modern silicon technology. We have extensively investigated TFETs with various gate oxides, channel materials and structures, fabricated on fully-depleted silicon-on-insulator (FD-SOI) substrates. Low-frequency noise (LFN) measurements were performed on TFETs, showing the dominance of random telegraphy signal (RTS) noise, which reveals the tunneling mechanism. An analytical TFET model combining tunneling and channel transport has been developed, showing agreement with the experimental and simulation results.

We also conceived and demonstrated a new device named the Z^2-FET (for *zero* subthreshold swing and *zero* impact ionization), which exhibits extremely sharp switching with subthreshold swing $SS < 1$ mV/dec, I_{ON}/I_{OFF} current ratio reaching 10^9, gate-controlled hysteresis and scalability down to 20 nm. The Z^2-FET operates with feedback between carriers flow and their injection barriers. The Z^2-FET is used for one-transistor dynamic random access memory (DRAM) with supply voltage down to 1.1 V, retention time up to 5.5 s and access speed reaching 1 ns. The static RAM (SRAM) application is also demonstrated without the need of refreshing stored data.

Following our work on gate-induced drain leakage (GIDL) current in short-channel FD-SOI MOSFETs and on TFET operating mechanisms, we propose a new class of optimized TFETs with enhanced I_{ON}, based on the bipolar amplification of the tunneling current. Simulations of the bipolar-enhanced tunneling FET (BET-FET), combining the TFET with a heterojunction bipolar transistor, show promising results, with $I_{ON} > 4\times10^{-3}$ A/μm and $SS < 60$ mV/dec over 7 decades of current, outperforming all silicon-compatible TFETs reported to date.

The thesis concludes with future research directions in the sharp-switching device arena.

Keywords: sharp switch, silicon-on-insulator (SOI), tunneling FET, MOSFET, feedback, Z^2-FET, single-transistor memory.

Titre: Dispositifs innovants à pente sous le seuil abrupte: du TFET au Z^2-FET

Cette thèse est consacrée à l'étude de dispositifs à pente sous le seuil abrupte, comprenant le transistor tunnel à effet de champ (TFET) et un nouveau composant MOS à rétroaction que nous avons nommé le Z^2-FET. Le Z^2-FET est envisagé pour la logique faible consommation et pour les applications mémoire compatibles avec les technologies CMOS avancées. Nous avons étudié de manière systématique des TFETs avec différents oxydes de grille, matériaux et structures de canal, fabriqués sur silicium sur isolant totalement déserté (FDSOI). Les mesures de bruit à basse fréquence (LFN) sur TFETs montrent la prédominance d'un signal aléatoire télégraphique (RTS), qui révèle sans ambiguïté le mécanisme d'effet tunnel. Un modèle analytique combinant l'effet tunnel et le transport dans le canal a été développé, montrant un bon accord entre les résultats expérimentaux et les simulations.

Nous avons conçu et démontré un nouveau dispositif (Z^2-FET, pour pente sous le seuil verticale et zéro ionisation par impact), qui présente une commutation extrêmement abrupte (moins de 1 mV par décade de courant), avec un rapport $I_{ON} / I_{OFF} > 10^9$, un large effet de hystérésis et un potentiel de miniaturisation jusqu'à 20 nm. La simulation TCAD a été utilisée pour confirmer que la commutation électrique du Z^2-FET fonctionne par l'intermédiaire de rétroaction entre les flux des électrons et trous et leurs barrières d'injection respectives. Le Z^2-FET est idéalement adapté pour des applications mémoire à un transistor. La mémoire DRAM basée sur le Z^2-FET montre des performances très bonnes, avec des tensions d'alimentation jusqu'à 1,1 V, des temps de rétention jusqu'à 5,5 s et des vitesses d'accès atteignant 1 ns. Une mémoire SRAM utilisant un seul Z^2-FET est également démontrée sans nécessité de rafraichissement de l'information stockée.

Notre travail sur le courant GIDL intervenant dans les MOSFETs de type FDSOI a été combiné avec le TFET afin de proposer une nouvelle structure de TFETs optimisés, basée sur l'amplification bipolaire du courant tunnel. Les simulations de nouveau dispostif à injection tunnel amélioré par effet bipolaire (BET-FET) montrent des résultats prometteurs, avec des I_{ON} supérierus à 4mA/μm et des pentes sous le seuil SS inférieures à 60 mV/dec sur plus de sept décades de courant, surpassant tous les TFETs silicium rapportés à ce jour.

La thèse se conclut par les directions de recherche futures dans le domaine des dispositifs à pente sous le seuil abrupte.

Mots-clés: commutation abrupte, silicium-sur-isolant (SOI), tunnel FET, MOSFET, rétroaction, Z^2-FET, cellule mémoire à un transistor.

LIST OF SYMBOLS AND ABBREVIATIONS

A		**Unit**
ALD	atomic layer deposition	
ARAM	advanced-RAM	
A_K	pre-factor in Kane's tunneling model	A· cm^{-1}
a_0, a_1 and a_2	coefficients in polynomial approximation of potential distribution	
B		
BET-FET	bipolar-enhanced tunneling FET	
BJT	bipolar junction transistor	
BOX	buried oxide	
BTBT	band-to-band tunneling	
B_K	exponential factor in Kane's tunneling model	V· cm^{-1}
C		
CMOS	complementary MOS	
CNT	carbon nanotube	
CVD	chemical vapor deposition	
C_{BOX}	buried oxide capacitance	F· cm^{-2}
C_G	front gate capacitor	F· cm^{-2}
C_{ox}	front gate oxide capacitance	F· cm^{-2}
D		
DC	direct current	
DG	double gate	
DRAM	dynamic RAM	
D	diffusion coefficient	cm^{-2}· s^{-1}
D_d	drain junction	cm^{-2}· s^{-1}

D_p	hole diffusion coefficient	$cm^{-2} \cdot s^{-1}$
E		
EOT	equivalent oxide thickness	
ESD	electrostatic discharge	
E	electric field	$V \cdot cm^{-1}$
E_C	conduction band edge	eV
E_F	Fermi level	eV
E_G	band gap	eV
E_i	midgap Fermi level	eV
E_{max}	maximum electric field	$V \cdot cm^{-1}$
E_n	electron quasi Fermi level	eV
E_p	hole quasi Fermi level	eV
E_{TW}	average electric field along shortest tunneling width	$V \cdot cm^{-1}$
E_V	valence band edge	eV
F		
FB-FET	feedback FET	
FED	field effect diode	
FD-SOI	fully depleted SOI	
FeFET	ferroelectric FET	
G		
GAA	gate all around	
GIDL	gate-induced drain leakage	
GTD	gate-controllable tunnel diode	
GP	ground plane	
G_{BTBT}	band-to-band tunneling rate	cm^{-3}
G_D	output conductance	$A \cdot V^{-1}$
G_{RD}	relative output conductance	V^{-1}

H		
HBT	heterojunction bipolar transistor	
HDD	heavily doped drain	
I		
IC	integrated circuit	
IMOS	impact ionization MOS	
ITRS	International Technology Roadmap for Semiconductors	
I_D	drain current	A· cm^{-1} or A· μm^{-1}
I_{DLEAK}	drain junction leakage current	A· cm^{-1} or A· μm^{-1}
I_{FED}	current in FED	A· cm^{-1} or A· μm^{-1}
I_{GTD}	current in GTD	A· cm^{-1} or A· μm^{-1}
I_h	hold current	A· cm^{-1} or A· μm^{-1}
I_{LEAK}	leakage current	A· cm^{-1} or A· μm^{-1}
I_n	electron current	A· cm^{-1} or A· μm^{-1}
I_{ON}	ON current	A· cm^{-1} or A· μm^{-1}
I_p	hole current	A· cm^{-1} or A· μm^{-1}
I_{Rd} and I_{Rs}	the recombination currents in the drain and source junctions	A· cm^{-1} or A· μm^{-1}
I_S	source current	A· cm^{-1} or A· μm^{-1}
I_{SG}, I_{SI}, I_{Sd}, I_{Ss} and I_r	saturation currents of gated, intrinsic, source and drain channel regions	A· cm^{-1} or A· μm^{-1}
I_{tp}	discharging current	A· cm^{-1} or A· μm^{-1}
J		
K		
k	Boltzmann constant	eV· K^{-1}

L		
LDD	lightly doped drain	
LFN	Low-frequency noise	
LPCVD	low pressure CVD	
L	layout dimension	cm or nm
L_d	characteristic length	cm or nm
L_D and L_S	distances from junctions to source/drain electrodes	cm or nm
L_G	physical gate length	cm or nm
L_{IN}	intrinsic (ungated) length	cm or nm
L_{TW}	shortest tunneling barrier width	cm or nm
M		
MOSFET	metal-oxide-silicon field-effect-transistor	
MPU	microprocessor unit	
MSDRAM	meta-stable dip RAM	
N		
NEGF	non-equilibrium Green's function	
n_i	intrinsic carrier density	cm^{-3}
n_p	electron density in *p*-type region	cm^{-3}
O		
P		
PD-SOI	partially depleted SOI	
Q		
Q_{CG}	charge on front gate capacitor	C
Q_S	surface charge density	cm^{-2}
ΔQ	change of charge	C
ΔQ_{Gth}	threshold value of the charge triggering internal	C

	feedback	
q	charge of an electron	C
R		
RAM	random access memory	
RSD	raised source/drain	
RTA	rapid thermal annealing	
RTS	random telegraphy signal	
S		
SCE	short-channel effect	
SG	single gate	
SOI	silicon-on-insulator	
SRAM	static RAM	
SS	subthreshold swing	$mV\cdot dec^{-1}$
T		
TAT	trap assisted tunneling	
TCCT	thin capacitively-couple thyristor	
TFET	tunneling FET	
TRAM	thyristor RAM	
T	temperature	K
T_{BOX}	buried oxide thickness	cm or nm
T_{Bcoll}	buried collector thickness	nm
T_{buf}	buffer layer thickness	nm
T_{base}	base layer thickness	nm
T_{coll}	collector thickness	nm
T_{emit}	emitter layer thickness	nm
t_f	rise/fall time	nm
T_{ox}	gate oxide thickness	cm or nm
t_{re}	retention time	s
T_{si}	active silicon layer thickness	cm or nm

T_{tun}	tunneling layer thickness	nm
U		
V		
V_{BG}	back gate voltage	V
V_{biC}	channel built-in voltage	V
V_{biD}	drain built-in voltage	V
V_{biG} and V_{biI}	field-induced built-in potentials in gated and intrinsic regions	V
V_{biS}	source built-in voltage	V
V_C	channel voltage	V
V_{clamp}	clamping voltage	V
V_{cj}	channel junction voltage	V
V_D	drain voltage	V
V_{DD}	supply voltage	V
V_{Dsat}	drain saturation voltage	V
V_{dj}	drain junction voltage	V
V_{FB}	flat-band voltage	V
V_G	top gate voltage	V
V_{GD}	voltage difference between gate and drain	V
V_{G2}	secondary front gate voltage	V
V_n	electron injection barrier	V
V_{ON}	turn-on voltage	V
V_{OFF}	turn-off voltage	V
V_p	hole injection barrier	V
V_S	source voltage	V
V_{sj}	source junction voltage	V
V_T	thermal voltage	V
V_{th}	threshold voltage of MOSFET	V
V_{Tth}	threshold voltage of TFET	V

W		
W	gate width	cm or μm
X		
x	position along the horizontal direction	cm or nm
x	Ge content in $Si_{1-x}Ge_x$	
Y		
y	position along the vertical direction	
Z		
Z^2-FET	*zero* subthreshold swing and *zero* impact ionization FET	
φ		
φ_b	bottom surface potential	V
φ_{BG}	back gate potential	V
φ_C	channel potential	V
φ_D	drain potential	V
φ_G	front gate potential	V
φ_S	source potential	V
φ_t	top surface potential	V

Chapter 1: Introduction to sharp-switching devices

Abstract- The applications of integrated circuits (ICs) have been expanding rapidly in the last few decades, thanks to the scaling of metal-oxide-silicon field-effect-transistors (MOSFETs). However, the scaling of MOSFETs is limited by short-channel effects (SCEs) and unscalable subthreshold swing. Sharp-switching devices, such as the tunneling FETs (TFETs) and feedback devices, are proposed to overcome the limits on MOSFET scaling and are beginning to show promising performance.

This introductory chapter briefly presents the operation principles and recent progress in TFETs and feedback transistors. The limitations of these devices are also explained, leading to a summary of the contributions of this thesis dedicated to improving sharp-switching device performance and inventing new variants of such devices.

1.1 MOSFET downscaling and its limits

The integrated circuit (IC) using metal-oxide-silicon field-effect-transistors (MOSFETs) has been developing rapidly for more than four decades and changing dramatically our lives. This is all driven by the scaling down of the MOSFET, doubling the integration density almost every two years according to Moore's law [1]. The miniaturization of MOSFETs has enabled ICs with lower cost, more integrated functions and faster speed. Figure 1.1 shows the scaling trend of the logic microprocessor unit (MPU) projected by ITRS 2011 [2].

However, there are several physical limits on the MOSFET scaling. The short-channel effect (SCE), where the drain and source electric fields penetrate into the channel and reduce the carrier injection barrier in the OFF state, increases significantly as the gate length (L_G) decreases. This greatly increases the leakage current and static power consumption. Though new technologies and device architectures, such as high-k/metal gate stacks, silicon-on-insulator (SOI) and multi-gate devices, have been proposed to enhance the gate controllability, the SCE is still one of the main issues for the scaling of MOSFETs.

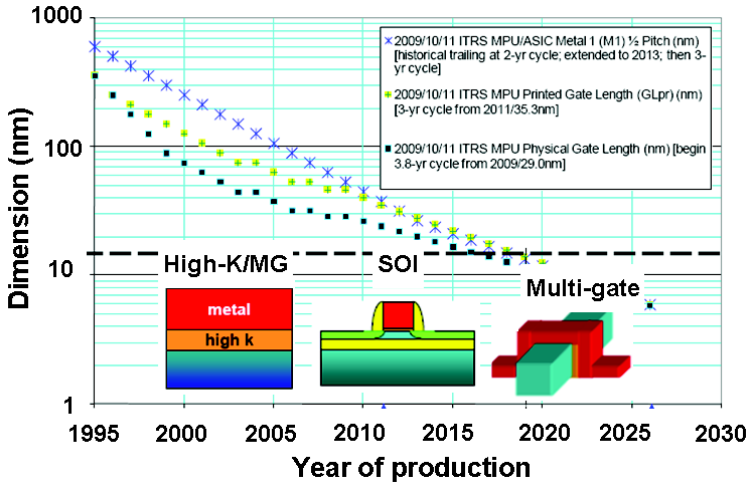

Fig. 1.1 Scaling trend projected by ITRS 2011 [2] and the new technologies enabling further scaling, including high-k/MG, SOI and multi-gate.

Another limit of MOSFET arises from the subthreshold swing (*SS*). The *SS,* defined in Eq. (1-1), is a criterion characterizing the sharpness of the switch. Due to the thermal diffusion between source and drain in subthreshold region, the *SS* of a MOSFET is larger than 60 mV/dec at room temperature, see Eq. (1.1) [3]. This physical limit results in an unscalable threshold voltage (V_{th}), see Fig. 1.2. The supply voltage (V_{DD}) of the MOSFET needs to be higher than V_{th} to turn on the device. Scaling of the V_{DD} causes the increase of the OFF current (I_{OFF}), see Fig. 1.2. In order to enable the scaling of V_{DD}, sharp-switching devices

with low SS < 60 mV/dec are of great interest, as illustrated schematically in Fig. 1.2.

$$SS = \frac{dV_G}{d\log(I_D)} \geq \ln(10) \cdot \frac{k \cdot T}{q} = 60mV \quad (1\text{-}1)$$

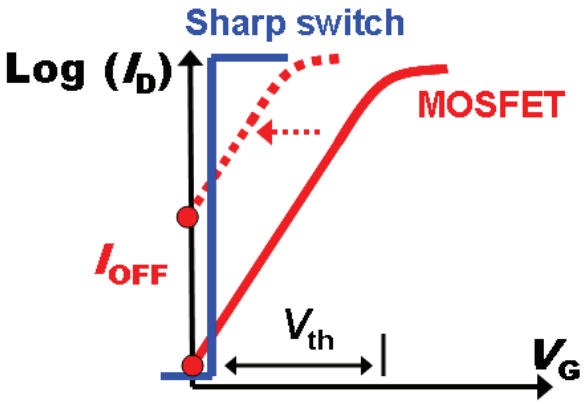

Fig. 1.2 Schematic view comparing the transfer characteristics of the MOSFET and the perfect sharp switch. The V_{th} in MOSFET is limited by the unscalable SS. Thus the decrease of V_{th} (dashed curve) increases the OFF current, compared to the MOSFET with high V_{th} (solid curve). A sharp switching device with a low SS would allow the V_{th} reduction.

1.2 Introduction to tunneling FETs (TFETs)

To tackle the thermal scaling limit and reduce the V_{DD} in MOSFETs, sharp-switching devices using different operation mechanisms have been proposed, such as impact ionization MOS (IMOS) [4], ferroelectric FET (FeFET) [5], tunneling FET (TFET) [6] and feedback FET (FB-FET) [7]. Here, we concentrate on TFETs and FB-FETs due to their high performance, compatibility with standard silicon fabrication materials and processing, and relatively low operating voltage.

1.2.1 Operation principle and advantages

The operation of a TFET can be traced back to the Zener diode, where both the *p* and *n* regions of a *pn* junction are highly doped. This induces high electric field in the narrow junction, schematically shown in Fig. 1.3 (a) [8]. In both forward and reverse bias, carriers can tunnel from conduction band to valence band within available energy states. Due to the interband tunneling, Zener diode has different characteristics from the conventional *pn* diode. Figure 1.4(a) shows that the Zener diode has a negative resistance region under forward bias due to the decrease in the number of states available for tunneling [9]. This property has been widely used in microwave generators. Under reverse bias, on the other hand, electrons tunnel

from the valence band in p^+ region to the conduction band in n^+ region, see Fig. 1.3(a). The increase in reverse bias enhances the electric field and the number of energy states available for tunneling, and thus increases the tunneling current monotonically.

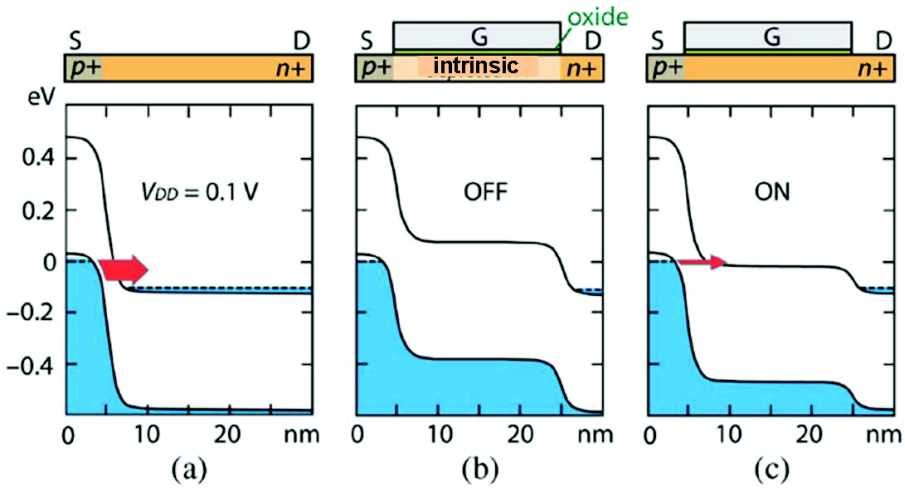

Fig. 1.3. Schematic view and energy band diagrams of (a) a Zener diode in reverse bias and an *n*-type TFET in (b) OFF and (c) ON states [8].

Figure 1.3(b) schematically shows the structure of a TFET, composed of a reverse biased p^+-i-n^+ channel and a control gate, together with the TFET band diagram in the OFF state, where the gate voltage (V_G) is low and the channel is depleted. The tunneling current is very low, since no energy state is available for the tunneling in the channel. The leakage current mostly arises from the thermal generation and trap assisted tunneling (TAT) [10]. At sufficiently high V_G, electrons are accumulated in channel and forms a field-effect induced n^+ region. The p^+-n^+ source junction in the ON state of a TFET is similar to a Zener diode, see Fig 1.3(c), giving rise to a significant ON current due to interband tunneling.

The transfer characteristic of an *n*-type TFET is shown in Fig. 1.4(b), where the current ramps rapidly as V_G increases [6]. Compared to MOSFET, the $SS < 60$mV/dec is obtained at room temperature for TFET with supply voltage below 1V. The TFET is also highly scalable and has better SCE immunity, since the OFF current induced by the tunneling directly from source to drain is very low. Furthermore, TFETs are compatible with Si technology and are well-suited to SOI channels, in which TFETs without an intrinsic channel have also been demonstrated, see Fig. 1.5 [11].

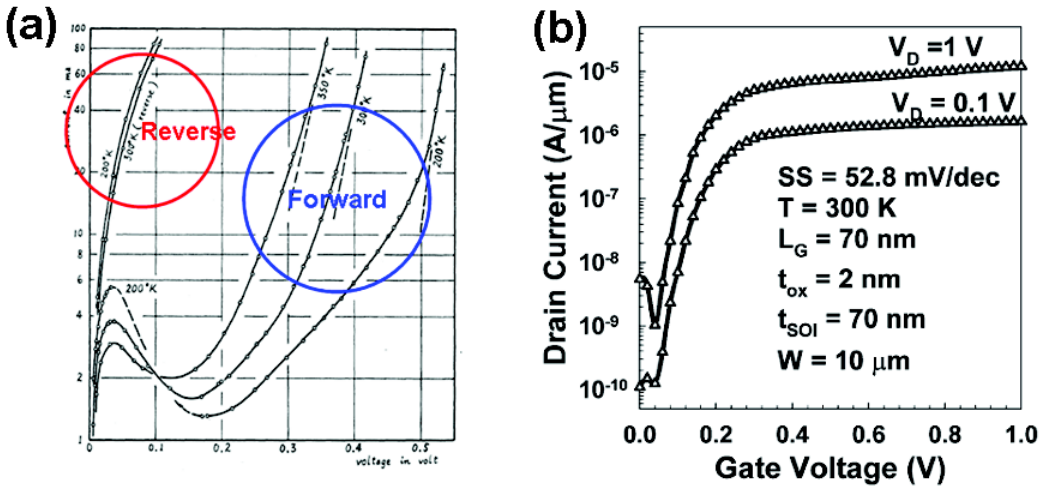

Fig. 1.4. (a) *I-V* characteristics of Zener diode with forward and reverse biases [9]. (b) I_D-V_G measurements of an SOI TFET showing $SS < 60$mV/dec at room temperature [6].

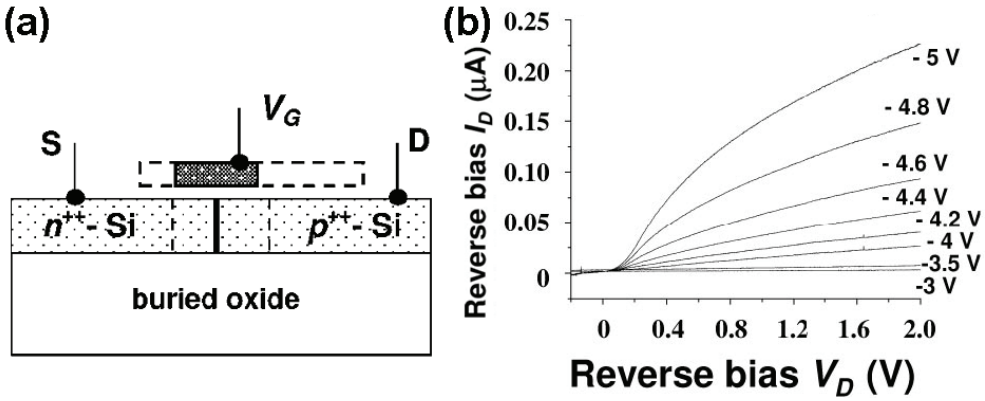

Fig. 1.5. (a) Schematic view and (b) I_D-V_D measurements on a TFET without intrinsic channel [11]. The ideal device has gate overlapping only the depletion region in order to minimize the capacitance (filled), whereas in the fabricated prototype, the gate overlaps a wider region (dashed) due to lithographic limitations.

1.2.2 State-of-the-art

Due to its low *SS* and good scalability, TFET is of great interest to replace or complement the MOSFET. However, the ON current I_{ON} of Si-based TFETs is very low, typically 3-5 decades lower than MOSFET, and the abrupt *SS* is only obtained over small current range due to the low interband tunneling rate. The interband tunneling rate in the TFET can be approximated by the simplified Kane's model [12]:

$$G_{\mathrm{BTBT}} = A_{\mathrm{K}} \cdot E_{max}{}^{2} \cdot exp(-\frac{B_{\mathrm{K}}}{E_{max}}) \qquad (1\text{-}2)$$

$$\text{with } B_{\mathrm{K}} \propto \sqrt{m^*} \cdot E_{\mathrm{G}}{}^{\frac{3}{2}} \text{ and } A_{\mathrm{K}} \propto \sqrt{m^*} \cdot E_{\mathrm{G}}{}^{-\frac{1}{2}}$$

where the $E_{\max}$ is the maximum electric field in the device, A_{K} and B_{K} are the tunneling parameters determined by material properties, such as band gap (E_{G}) and effective tunneling mass (m^*). Thus, the performance of the TFET can be improved by increasing the $E_{\max}$, through optimizing the device structure, and reducing the exponential factor B_{K}, through the use of lower band-gap material.

1.2.2.1 Structural optimization

The electric fields in a TFET strongly depends on structural parameters, such as the gate dielectric, sharpness of the tunneling junction and the use of multiple gate structure. Experimental and simulation studies have been conducted showing that the thin equivalent gate oxide is vital to increase the electric field, and thus increase the I_{ON} and reduce the *SS* in a TFET, see Fig. 1.6 [13-14].

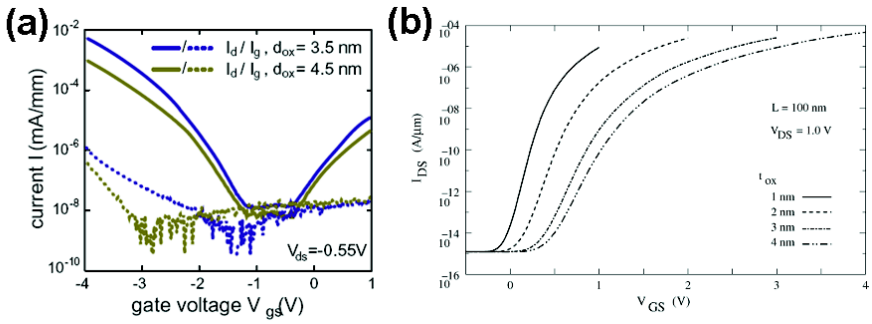

Fig. 1.6. (a) Experimental [13] and (b) simulated [14] I_{D}-V_{G} curves comparing the TFETs with various gate oxide thickness.

The sharpness of the tunneling junction also impacts the TFET performance. Figure 1.7(a) compares the TFETs fabricated with two different annealing processes for the source/drain doping activation [15]. The device with spike annealing shows higher I_{ON} and lower *SS* than that with conventional rapid thermal annealing (RTA), thanks to the sharper tunneling junction resulting from the reduced diffusion of the dopants. An even more abrupt tunneling junction is obtained by placing a doping pocket close to the source, schematically shown in Fig. 1.7(b), which markedly improves the TFET performance, see Fig. 1.7(c).

The multi-gate structure, which is widely employed in MOSFETs for enhancing the gate controllability [16], can also be used in TFETs to augment the device performance. Figure

1.8(a) shows the structure of a Fin FET-based TFET structure [2]. The I_D-V_G measurements in Fig. 1.8(b) compare the performance of devices with different fin width, showing that the scaling of the fin is advantageous to improve the performance, thanks to the enhanced electric field at the tunneling junction [16]. TFETs with gate all around (GAA) structure have also been fabricated in bottom-up grown nanowire, see Fig. 1.8(c) and (d) [17].

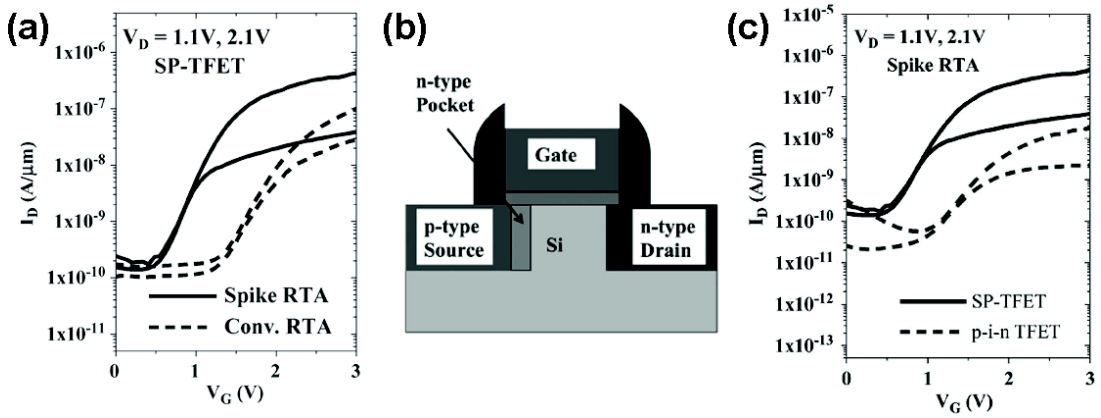

Fig. 1.7. (a) Comparison between TFETs fabricated by spike annealing and conventional rapid thermal annealing (Conv. RTA) [15]. (b) Structure and (c) performance comparison between the TFET with/without the source pocket doping (SP-TFET *vs*. *p-i-n* TFET).

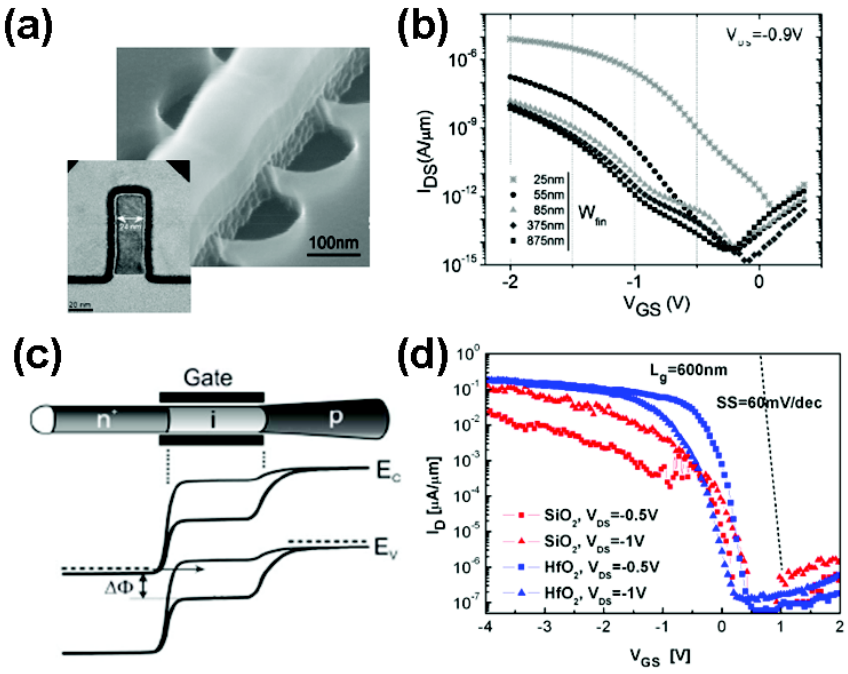

Fig. 1.8. (a) Structure and (b) I_D-V_G characteristics of Fin-TFETs with various fin widths [2]. (c) Structure and (d) I_D-V_G characteristics of the GAA TFETs built in a silicon nanowire [17].

1.2.2.2 Material optimization

The TFETs built on SOI substrate suffers from low I_{ON}, due to the wide band gap (E_G) of Si. Thus, materials with lower E_G, such as silicon-germanium ($Si_{1-x}Ge_x$) [18], Ge [19-20] and Ⅲ-Ⅴ semiconductors [21-22], are of great interest to enhance the I_{ON} of TFET. Figure 1.9 shows the experimental I_D-V_G curves of the recently reported TFETs fabricated on Si [17], Ge [20] and $In_{0.53}Ga_{0.47}As$ [22] substrates. The lowest *SS* of Si TFET reaches down to *SS* = 42mV/dec, much lower than that of MOSFET, albeit with I_{ON} of 5 decades lower (see Table 1.1). The use of Ge and $In_{0.53}Ga_{0.47}As$, instead of Si, enhances the I_{ON} of TFET by over 2 and 3 decades, respectively. However, the *SS* also degrades due to the leakage current and inferior dielectric-channel interface.

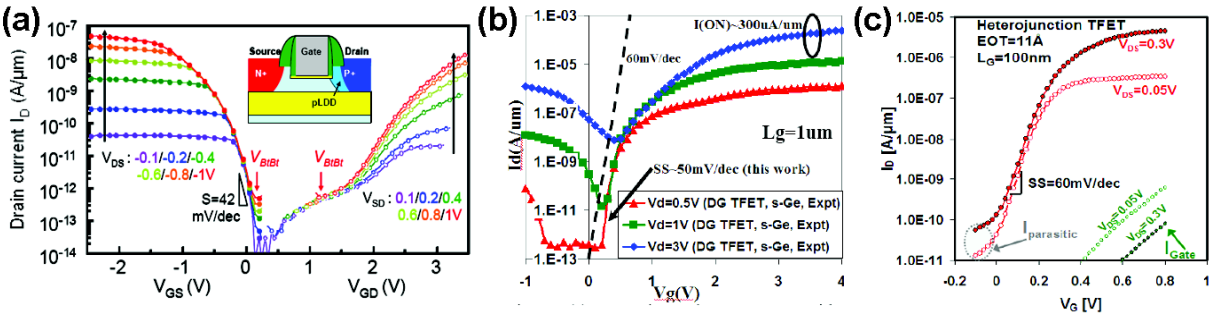

Fig. 1.9. Experimental I_D-V_G curves of TFETs built on (a) silicon [18], (b) strained Ge [20] and $In_{0.53}Ga_{0.47}As$ Ⅲ-Ⅴ compound [22].

Table 1.1 Comparisons of the performance between MOSFET and recently reported TFET based on different substrates.

Device	I_{ON} (A/μm)	Lowest *SS* (mV/dec)
Si MOSFET [23]	1.5×10^{-3} @ $\|V_G\|$=1V; $\|V_D\|$=1V	> 60 mV/dec
Si TFET [18]	6×10^{-9} @ $\|V_G\|$=1V; $\|V_D\|$=0.6V	42 mV/dec
Ge TFET [20]	7×10^{-7} @ $\|V_G\|$=1V; $\|V_D\|$=0.5V	50 mV/dec
InGaAs TFET [22]	5×10^{-6} @ $\|V_G\|$=0.8V; $\|V_D\|$=0.3V	60 mV/dec

Although the I_{ON} of the TFETs built on Ge and Ⅲ-Ⅴ compounds are enhanced significantly compared to the Si device, it is still over 2 decades lower than the conventional MOSFET. For further enhancement, the TFETs based on graphene and carbon nanotube (CNT), which possess even lower band gap and smaller tunneling mass, have been proposed in simulation [24-25]. Simulations of an ideal graphene TFET structure show sharp switching

with *SS* = 0.19 mV/dec and ON current competitive with a Si MOSFET. The projected operation speed is higher than MOSFET with much lower power consumption [24]. However, the fabrication of high-quality graphene with both *n* and *p* doping, as well as good dielectric/graphene interfaces, remains a challenge.

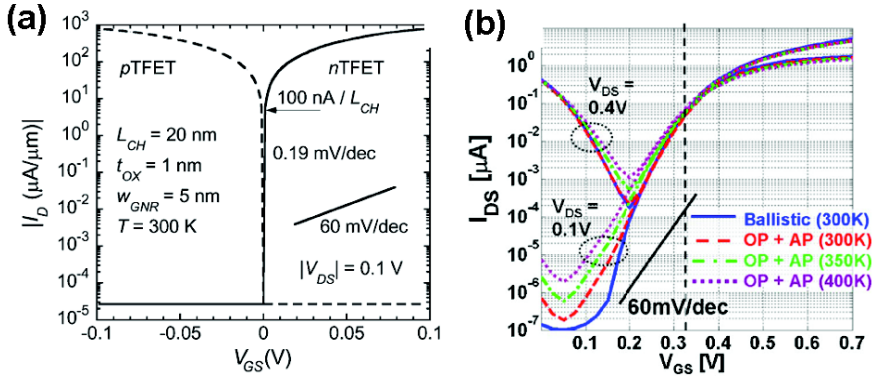

Fig. 1.10. Simulated I_D-V_G curves of TFETs on (a) graphene [24] and (b) carbon nanotube (CNT) [25].

1.2.3 Issues

Though the TFET is a promising sharp switching device with good scaling capability for future low power application, there are still issues including:

a. The I_{ON} is too low. Although the low band-gap materials are used to enhance the current of TFET, however, the I_{ON} is still over 2 decades lower than in MOSFET.

b. The leakage current I_{LEAK} is relatively high, compared to its I_{ON}. The leakage current in symmetrical TFETs is mainly induced by the parasitic tunneling in drain junction, which is even higher

than the I_{ON} produced by the tunneling in source junction [18].

c. The device physics is not completely understood. The applicability of Kane's model to indirect bandgap materials is questionable, as tunneling to a different region in the Si or Ge Brillouin zone requires phonon or impurity scattering, which is ignored in Eq. (1-2) [26]. Furthermore, the predicted tunneling current has an exponential dependence on E_{max} which depends on both V_G and V_D in a complex, device geometry-dependent fashion. Even the very existence of a gate-controlled interband tunneling current in a TFET typically requires temperature-dependent measurements to rule out other effects [18].

d. Analytical models for TFET performance explanation and prediction are lacking. So far, several analytical models have been developed for the TFET. However, none of them

includes the effect of channel transport, which becomes important as the tunneling current increases. Also the quantitative comparisons between the model and experimental results are very rare.

1.3 Introduction to feedback devices

Another class of compact semiconductor device that possesses sharper switching than a standard MOSFET utilizes feedback mechanism. One of the well known feedback devices is the thyristor, where positive feedback between two bipolar transistors is triggered by impact ionization [3]. Due to its sharp switching and high current drive, the thyristor has been widely used in power electronics. A variant known as the thin capacitively-couple thyristor (TCCT) has been built in fully-depleted silicon-on-insulator (FD-SOI) substrates with typical *p-n-p-n* doped channel and control gate, schematically shown in Fig. 1.11(a) [11]. The TCCT has been demonstrated for high speed one-transistor (1T) DRAM and SRAM applications [11, 27-28], see Fig. 1.11(b).

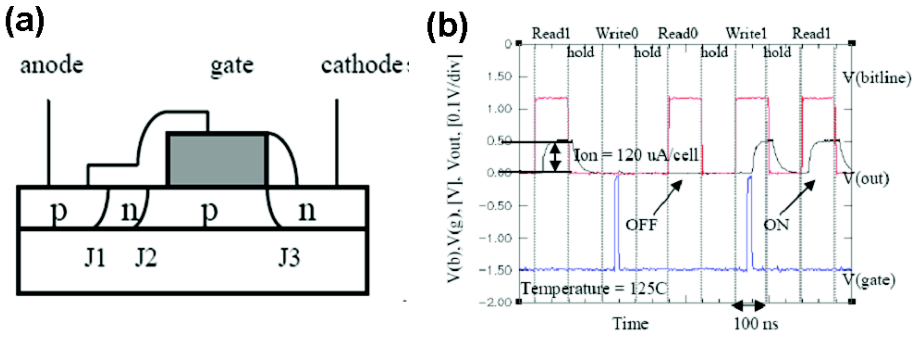

Fig. 1.11. (a) Schematic view of the thin capacitively-couple thyristor (TCCT) and (b) its application as high-speed one transistor DRAM (1T-DRAM) [11].

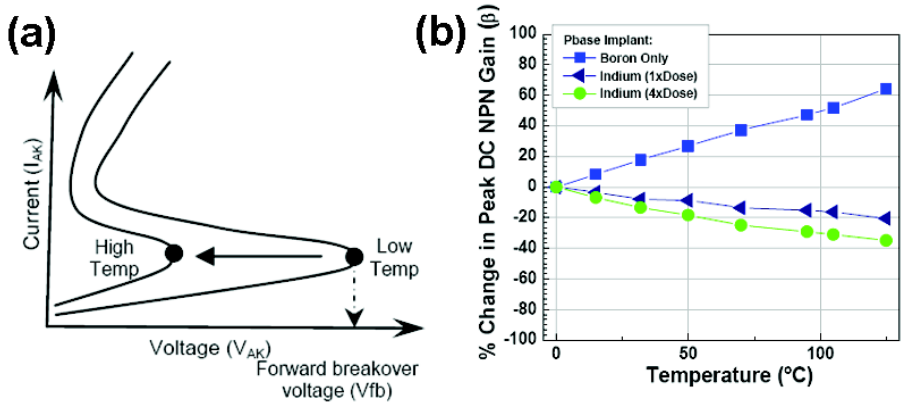

Fig. 1.12. (a) I_D-V_D curves showing that the breakover voltage of thyristor is sensitive to the temperature variation, due to (b) the change of bipolar gain [29].

However, the thyristor current-voltage characteristics are very sensitive to temperature variation, see Fig. 1.12(a), caused by temperature-induced variations in the bipolar gain, as shown in Fig. 1.12(b) [29]. Also, the bipolar gain depends sensitively on the doping of the lateral junctions, so accurate doping control is required to obtain a stable device performance.

Recently, another positive feedback device, the feedback field effect transistor (FB-FET) has been demonstrated to possess extremely sharp switching and a high on current (I_{ON}) without involving impact ionization [7, 30]. The FB-FET is a forward biased *p-i-n* diode with control gate, see Fig. 1.13(a). The operation of the FB-FET uses both positive and negative surface charges (Q_S) on Si_3N_4 spacers adjacent to the gate, schematically shown in Fig. 1.13(a). These surface charges form the electron and hole injection barriers in source and drain, respectively, see the band-diagram in Fig. 1.13(b). The I_D-V_G measurements show sharp switch with ultra-small subthreshold swing and $I_{ON}/I_{OFF} \sim 10^8$, see Fig. 1.13(c), thanks to the feedback interaction between the carriers flow and the injection barriers. However, the threshold voltage (V_{th}) of the FB-FET depends strongly on the surface charge density, which is difficult to be controlled quantitatively. Further, the accumulation of surface charge needs high voltage ($|V_G|$ and $|V_D| > 6V$), which is a drawback for practical implementation in modern ICs.

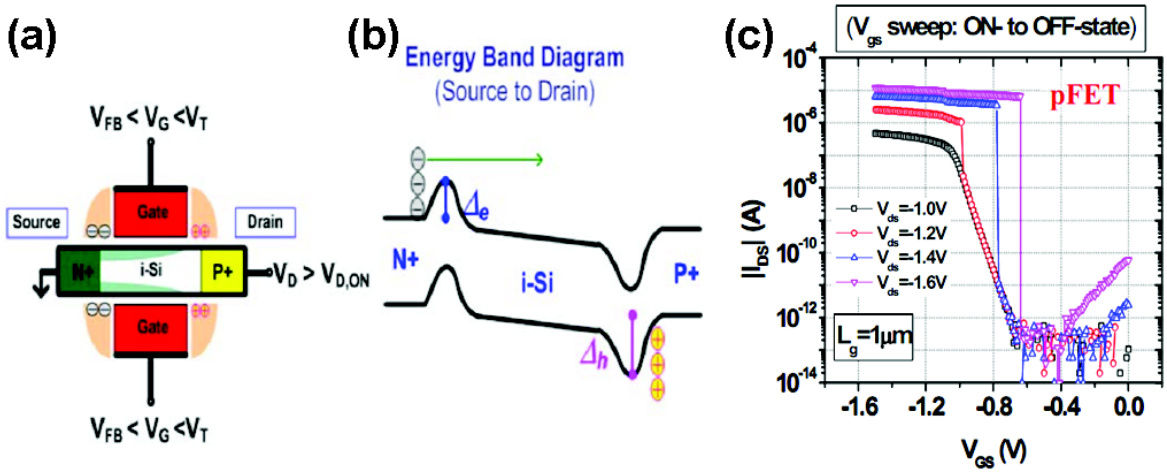

Fig. 1.13 (a) Schematic device structure, (b) band-diagram and (c) I_D-V_G characteristics of feedback FET (FB-FET) [7, 30].

A variant of feedback FET without surface charge is the field effect diode (FED) [31]. The FED uses two adjacent front gates forming the carrier injection barriers to achieve better controllability, see Fig. 1.14(a). Figure 1.14(b) shows its I_D-V_D characteristics under various V_G. As V_D increases, the device is sharply turned on with the turn-on voltage (V_{ON}) controlled by V_G. This property was used in electrostatic discharge (ESD) protection and further

proposed for memory application showing good simulated scaling capability, shown in Fig. 1.14(c) [32]. The fabrication of FED with two closely adjacent front gates separated by a narrow gap might be a challenge, especially with scaled dimension.

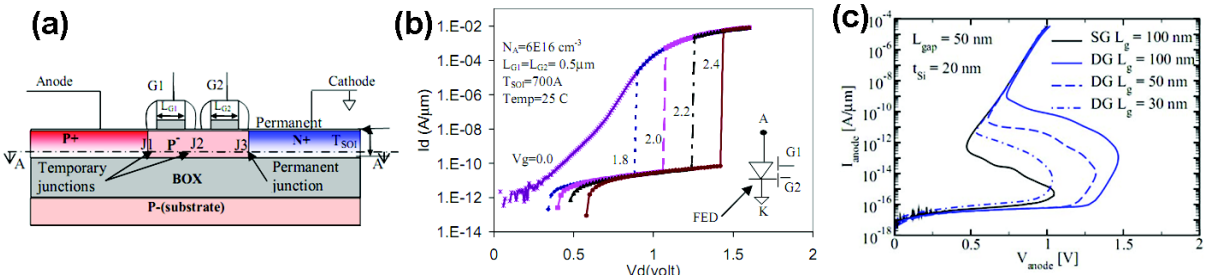

Fig. 1.14 (a) Schematic device structure and (b) I_D-V_D characteristics of field effect diode (FED) using two front gates [31]. (c) I_D-V_D simulation demonstrating the hysteresis in FED with various gate length [32].

Later in this thesis, we demonstrate a novel device using feedback without recourse to impact ionization, surface charges or two adjacent front gates. Our device uses front and back gates to form the carrier injection barriers, ensuring good controllability and simplifying the fabrication.

1.4 Content and organization of this thesis

The purpose of this thesis is to enhance the performance and modeling of sharp-switching TFETs and demonstrate a new feedback-based device, called the Z^2-FET, which has a nearly zero *SS*. Furthermore, we will propose a new type of TFET with built-in bipolar amplification to overcome the low I_{ON} observed in TFETs until now. We conclude with possible avenues of future work in the sharp-switching device arena.

1.4.1 Our work on TFETs

Our research work on TFET is dedicated to addressing the current issues to improve the performance and gain more understanding on the device physics as described below:

a. Several methods are employed to enhance the I_{ON}. The TFET with high-k gate oxide (HfO_2) is fabricated showing higher I_{ON} than device with SiO_2 gate oxide, thanks to the lower equivalent oxide thickness. The I_{ON} is further enhanced by using TFET built on low band-gap material ($Si_{1-x}Ge_x$).

b. The leakage current I_{LEAK} is suppressed by asymmetric TFET, where an un-gated intrinsic region is placed to separate the drain from the gate, and thus reduces ambipolar tunneling

leakage.

c. Low-frequency noise (LFN) measurement is performed to characterize the TFET. The result shows that the random telegraphy signal (RTS) noise with $1/f^2$ slope is dominant in TFET, which is different from MOSFET, where the $1/f$ noise is dominant. Physical explanations are given revealing the tunneling mechanism in TFET.
d. An analytical model combining the tunneling and channel transport is developed agreeing well with our experimental results. The model is also extended to explain the gate-induced drain leakage (GIDL) in both TFET and fully-depleted SOI MOSFET.

1.4.2 Our work on the Z^2-FET feedback device

We develop a new feedback device named Z^2-FET, as it features *zero* subthreshold swing and *zero* impact ionization. The Z^2-FET has simple structure using top and back gates to form the injection barriers without the recourse to surface charge and fabrications difficulty of two front gates. Our studies on the Z^2-FET mainly include:

a. Direct current (DC) measurements show sharp switching property with nontrivial performance and gate-controlled hysteresis. The *SS* falls below 1 mV/dec with current I_{ON}/I_{OFF} ratio higher than 10^8, outperforming conventional MOSFETs and TFETs. The I_D-V_D measurements show hysteresis between sweeping forward and backward with the turn-on voltage controlled by the gate voltage, interesting for memory application.
b. TCAD simulation is performed to study the operation principle and scaling capability. The operation of the Z^2-FET involves the feedback between the carriers flow and the injection barriers controlled by front and back gates. With advanced SOI structure, the device dimension is scalable down to 30 nm.
c. DC measurements are performed on the Z^2-FET under various temperatures and long time voltage stressing to demonstrate its good reliability.
d. An analytical model is built to explain the Z^2-FET performance. The model combines the field-effect controlled diffusion current and current-induced voltage at the source and drain junctions. The V_G-controlled hysteresis is well explained.
e. Transient measurements and simulations are performed demonstrating the application of Z^2-FET as high-speed one-transistor DRAM and SRAM. The DRAM based on Z^2-FET is demonstrated with supply voltage down to 1.1V and read/write time < 1 ns. The retention time is studied in details on devices with different dimensions under various temperatures.

1.4.3 Our work on a new bipolar-enhanced TFET

This thesis will conclude with a novel-sharp switching device named BET-FET (bipolar enhanced tunneling FET) built in $Si/Si_{1-x}Ge_x$ substrate that is proposed and simulated. The BET-FET combines the TFET with the bipolar junction transistor (BJT). The tunneling generated carriers are used as base current to drive the BJT and induce high bipolar current. Combining the merits of the sharp switching of a TFET and high driving current of a BJT, the simulated BET-FET reaches $SS < 60$ mV/dec, I_{ON} competitive with MOSFET at low V_{DD}, scalability down to 10 nm, and full Si fabrication capability.

Chapter 2: Characterization and optimization of TFETs

Abstract- In this chapter, diversified measurements and simulations are conducted on TFETs with various structures in order to enhance the device performance and reveal the device physics.

Variable temperature measurements are reported to confirm the tunneling mechanism in TFETs, which were fabricated in fully depleted SOI (FD-SOI) process compatible with CMOS. The first low frequency noise (LFN) measurements on TFETs are also performed to reveal that the LFN in TFET differs from that in MOSFET, demonstrating the presence of the narrow tunneling junction.

In order to reduce the leakage current (I_{LEAK}), asymmetrical TFET design is used to suppress the ambipolar tunneling current and TCAD simulations are used to explain the effect.

Compared to the TFET with SiO_2 gate oxide and conventional Si channel, devices with high-k gate oxide and $Si_{1-x}Ge_x$ channel are demonstrated to possess an ON current (I_{ON}) that is more than 3 decades higher, thanks to higher electric field and lower band-gap at the tunneling junction.

2.1 Fabrication and device structure

The TFET fabrication is totally compatible with fully depleted SOI CMOS process flow [33]. Unibond SOI with 145 nm BOX and 20 nm active Si layer is used as the fabrication substrate. The device active areas (mesa structure) are isolated by photolithography and dry etching. The following deposited gate stack is composed of three layers, as illustrated in Fig. 2.1(a). Two different gate oxides are formed for comparison: either a 6 nm SiO_2 grown by dry oxidation or a 3 nm atomic layer deposited (ALD) HfO_2. After the deposition of a metal gate (10 nm TiN), 50 nm thick polysilicon is added.

The first spacer is formed by the deposition of 10 nm Si_3N_4 in LPCVD, then a 10 nm raised source/drain (RSD) Si layer is epitaxially grown by CVD process. The *n*-type lightly doped drain (LDD) is formed by implantation of As with dose of 1×10^{15} cm^{-2} and energy of 9 keV, while BF_2 implantation with dose of 1×10^{15} cm^{-2} and energy of 7 keV is used for formation of *p*-type LDD. Then, a second spacer of 15 or 30 nm and a RSD Si layer of 20 nm are deposited. The dose and energy of As for *n*-type highly doped drain (HDD) implantation were 2×10^{15} cm^{-2} and 20 keV, respectively, whereas, for *p*-HDD implantation, these values were 3×10^{15} cm^{-2} and 5 keV. Rapid thermal annealing (RTA) was used to activate the dopants, followed by the metallization.

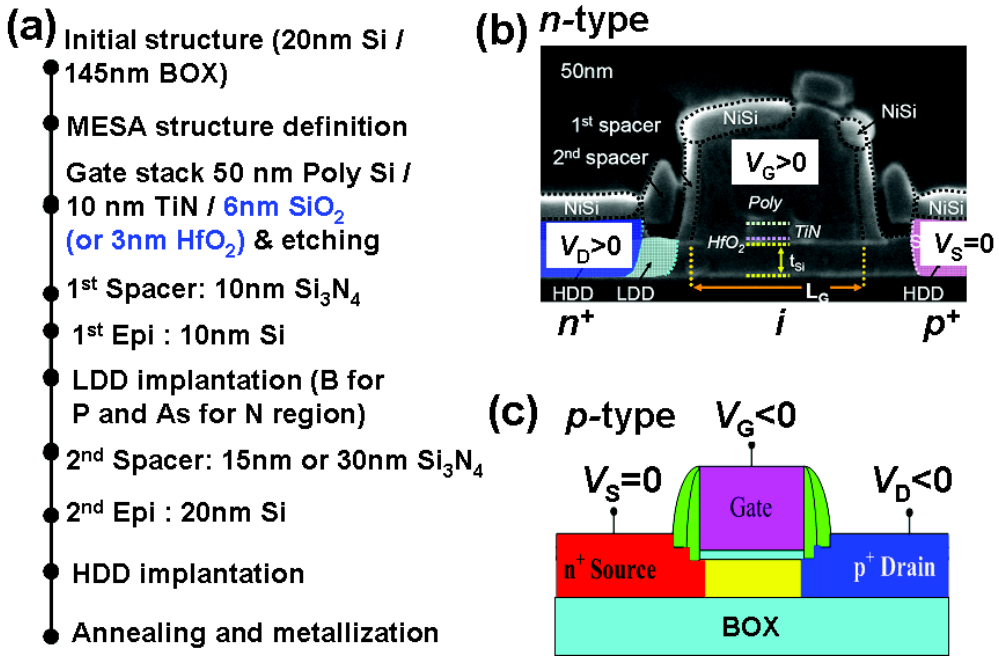

Fig. 2.1. (a) Fabrication of the TFET using standard FD-SOI process. (b) Cross-section view of the *n*-type TFET structure. (c) Schematic view of the *p*-type TFET.

The structure of the fabricated TFETs is similar to that of a MOSFET with double spacers and raised S/D, shown in Fig. 2.1(b). The only structural difference between TFETs and MOSFETs lies in the opposite doping of the TFET source and drain.

For simplicity, the p^+ region in n-type TFET is defined as source while the n^+ region is defined as drain. The source is grounded and drain is positively biased. Figure 2.2(a) shows I_D-V_G measurements on the n-type TFET with L_G=400nm and T_{ox}=3nm HfO_2. The I_{ON} in n-TFETs is produced by tunneling at the source-channel junction at $V_G > 0$. Whereas, the I_{LEAK} is induced by the parasitic tunneling at drain-channel junction at $V_G < 0$ and can be even higher than I_{ON}. The origin and suppression of the I_{LEAK} are introduced in section 2.3 in details.

The opposite definition applies to p-type TFET, as illustrated in Fig. 1(c). Again, the source is grounded, while the drain is negatively biased in p-TFETs. In contrast with the n-type device, the I_{ON} and I_{LEAK} are produced at $V_G < 0$ and $V_G > 0$, respectively for p-type TFETs, see Fig. 2.2(b). Note that in all measured devices the gate leakage is negligible compared to the drain current.

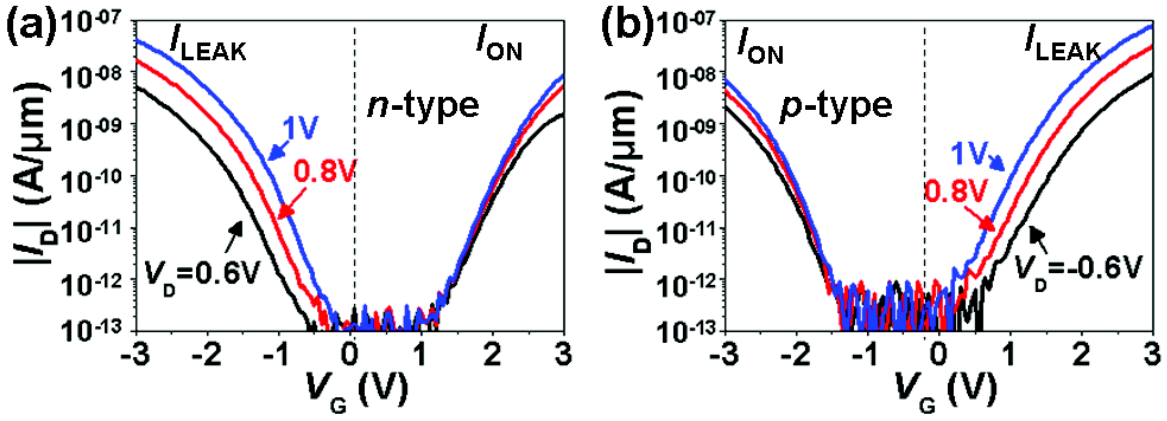

Fig. 2.2. I_D-V_G measurements on the (a) n-type and (b) p-type modes of the TFET with L_G = 400 nm and T_{ox} = 3 nm HfO_2 under various V_D bias.

2.2 Measurements confirming the tunneling mechanism

In order to confirm that the current in TFET is indeed induced by tunneling other than other mechanisms, such as carrier drift and diffusion, variable-temperature measurements and low-frequency noise (LFN) measurements have been performed.

2.2.1 DC characteristics of TFETs under various temperatures

To verify the tunneling in the TFET, measurement under various temperatures has been reported showing that the current in TFET is relatively insensitive to the temperature variation and slowly increases monotonically as temperature (T) ramps up [2], due to the decrease of bandgap. This is contrary to the conventional MOSFET, where the drift current decreases as T increases due to the degraded mobility resulting from phonon scattering [3].

Figure 2.3 (a) shows the I_D-V_G of a n-type TFET with 3 nm HfO_2 gate oxide, L_G = 400 nm T increasing from 100 K to 300 K in 50 K steps. At low I_D, where the current is dominated by the interband tunneling at the source-channel junction, the temperature dependence of the TFET I_D can be qualitatively explained by the Kane tunneling model [12]:

$$I_D = A_K \cdot E_{max}^{\ 2} \cdot exp(-\frac{B_K}{E_{max}}) \quad \text{with } E_{max} \propto V_G \text{ and } B_K \propto E_G^{\frac{3}{2}} \tag{2-1}$$

where A_K, B_K are tunneling parameters which depend on the bandgap and carrier effective mass in the channel material.

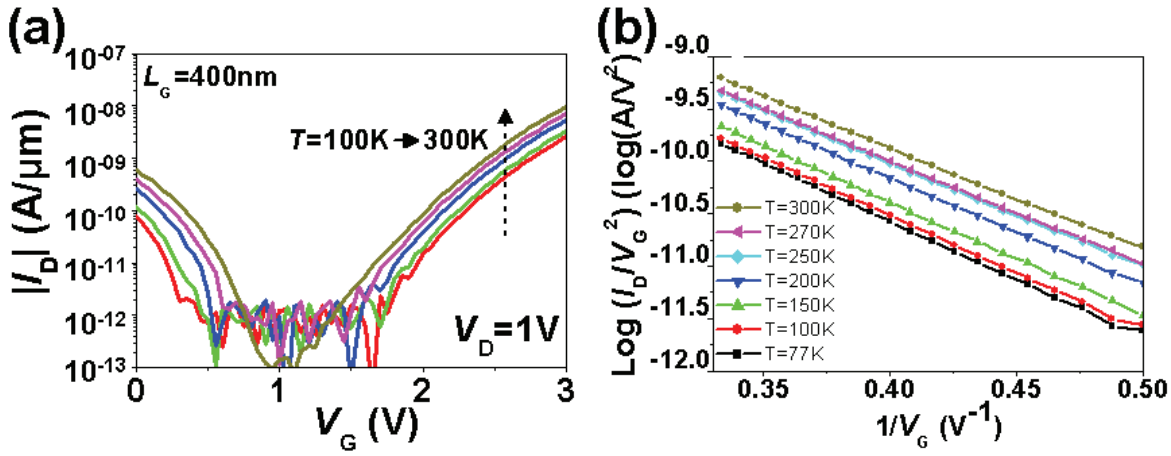

Fig. 2.3: (a) I_D-V_G characteristics and (b) log(I_D/V_G^2)-V_G^{-1} curves at V_D = 1 V for an n-type TFET with L_G = 400 nm as a function of temperature T.

The dominant temperature effect on the TFETs performance comes from the temperature variation of bandgap E_G, which enters in the exponential of Eq. (1). In Si, E_G has weakly negative temperature dependence [3]:

$$E_G(T) = E(0) - \frac{\alpha \cdot T^2}{T + \beta} \text{ with } \alpha = 4.73 \times 10^{-4} \text{eV/K and } \beta = 636\text{K} \tag{2-2}$$

As temperature increases, the E_G decreases, leading to a corresponding decrease in parameter B_K and hence an increasing tunneling current.

The validity of Kane's model can be examined by rewriting Eq. (2-1) as:

$$log(\frac{I_D}{V_G^2}) \propto -\frac{B_K}{V_G} \quad (2\text{-}3)$$

Figure 2.3(b) confirms the linear relationship between $\log(I_D/V_G^2)$ and $1/V_G$ over the entire temperature range. The slight variation in the slope reflects the increase of the B_K coefficient at low temperature.

Since the temperature dependence of TFET I_D agrees with that reported previously [18] and with Eq. (1-1), we can draw two main conclusions:

i) The weak temperature dependence of the drain current I_D confirms that BTBT is the dominant mechanism in TFETs. By contrast, the drain current in MOSFETs is strongly temperature-dependent, mainly due to mobility variation.

ii) The Kane model is qualitatively effective in describing the indirect BTBT process in Si TFETs.

2.2.2 Low frequency noise (LFN) characteristics

The LFN of standard MOSFETs is an important limiting factor in analog and digital circuits [34-35]. Since the LFN-generating mechanism is the trapping at the channel-gate dielectric interface, LFN measurements are also used to extract the density and energy distribution of the interface traps in MOSFETs [36-37]. As TFET technology matures, LFN properties of TFETs will also impact circuit functionality. But even at the single device level, the $1/f^2$ LFN dependence in TFETs provides a useful experimental signature distinguishing the tunneling current mechanism from standard MOSFET current [38].

In MOSFETs, the LFN is mainly caused by the fluctuation of the channel carrier density due to the trapping-detrapping process at the channel-dielectric interface. A single trapping-detrapping event causes random telegraph signal (RTS) noise with Lorentzian spectrum characterized by $1/f^2$ slope [36]. For MOSFETs with large gate area, the superposition of many trapping-detrapping events produces $1/f$ noise [36]. As the gate area decreases below 1 μm^2, only one or a few near-interface oxide traps exist in the entire device, leading to RTS current noise. Figure 2.4 shows the noise spectrum of an *n*-type MOSFET fabricated in the same process alongside our TFETs [18]. The dimensions of the device are T_{ox} = 6 nm SiO_2, L_G = 350 nm and W = 10μm. The noise shows $1/f$ slope as V_G sweeps from 0.1V to 1.5V, due to its large gate area (3.5 μm^2), see Fig. 2.4.

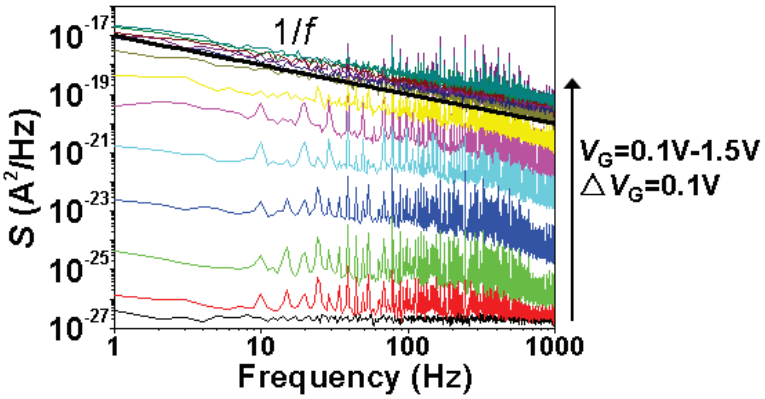

Fig. 2.4: LFN spectra of NMOS (L_G = 350 nm, W = 10μm, V_D = 50 mV, V_G = 0.1-1.5 V) showing 1/f noise.

However, as we demonstrate for the first time, the LFN properties of TFETs are quite different. Figure 2.4 shows the spectrum of two n-type TFETs with the same 6 nm SiO_2 gate oxide presenting totally different spectral behavior. In the MOSFET of Fig. 2.4 with a gate area of 3.5 μm^2 the LFN is 1/f, whereas in the TFETs the noise spectrum is Lorentzian with 1/f^2 slope despite the much larger 25 μm^2 gate area (L_G = 5 μm). The lower images in Fig. 2.5 show the output voltage of the amplifier used for detecting the fluctuation in I_D.

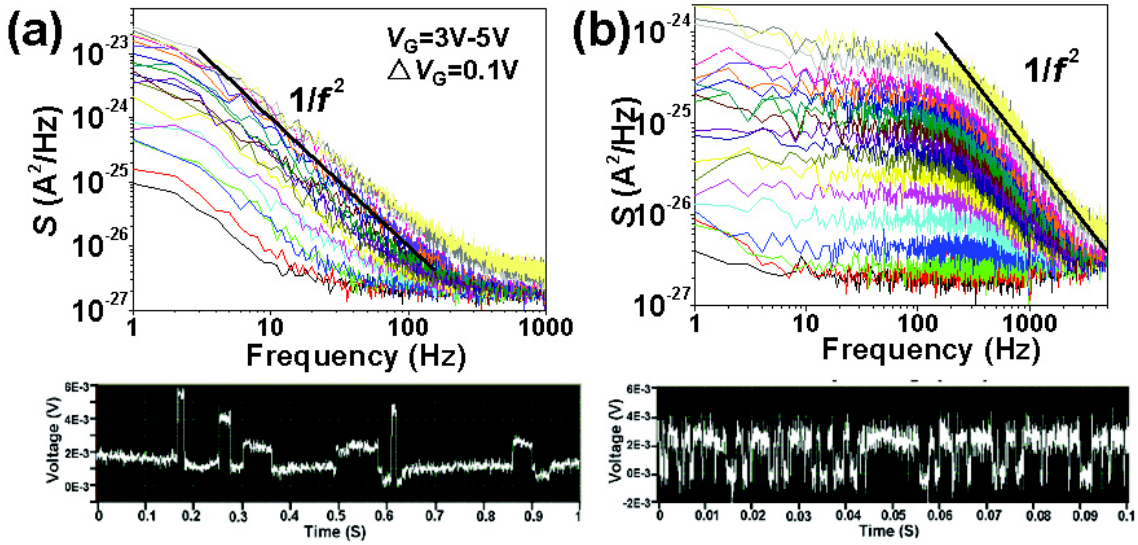

Fig. 2.5: (a), (b) LFN spectra of two n-type TFETs with the same structure and bias (L_G = 5 μm, W = 5 μm, V_D = 1 V, V_G = 3-5 V). The lower images show the time variation of the output voltage from the amplifier used to capture the LFN signal in the n-type TFET. The RTS noise can be clearly observed, with an amplitude of ~0.003 V (output voltage) × 10^{-8} A/V (amplifier sensitivity) = 3×10^{-11} A for the n-type TFET in (a). RTS of lower amplitude and higher characteristic frequency is observed in (b), indicating large variability due to single-trap events.

The RTS noise in TFETs is characterized by a large variability. The TFET in Fig. 2.5(a) exhibits RTS caused by two or three traps that cause different I_D jumps at different trapping rates. The TFET in Fig. 2.5(b), which has nominally the same structure and dimensions, includes a single RTS-generating trap with a lower RTS amplitude. The trapping-detrapping process is also faster, resulting in a much higher characteristic frequency.

All differences of LFN properties in TFET against MOSFET can be attributed to the small effective tunneling area in TFET. Figure 2.6 compares the I_D-V_G characteristics of *n*-type MOSFETs and TFETs with different gate lengths (L_G) from 5 μm to 100 nm. The I_{ON} of TFETs is almost 5~6 decades lower than that of MOSFETs due to the large bandgap of silicon and the insufficiently abrupt tunnel junction. As can be seen from Fig. 2.6(a), in MOSFETs the I_{ON} increases as L_G decreases due to larger channel conductance. As L_G decreases to 100 nm, the threshold voltage (V_{th}) of the MOSFET tends to decrease due to the short channel effect and drain induced barrier lowering (DIBL). In TFETs, neither the I_{ON} nor V_{th} changes as L_G decreases from 5 μm to 100 nm. This indicates that the current in TFETs is not controlled by channel conductance as in MOSFETs, but by interband tunneling at the source-channel junction, which is also confirmed by the weak temperature dependence of I_D in previously. Therefore, the characteristics of TFETs are independent of L_G, at least for the low I_{ON} levels demonstrated so far.

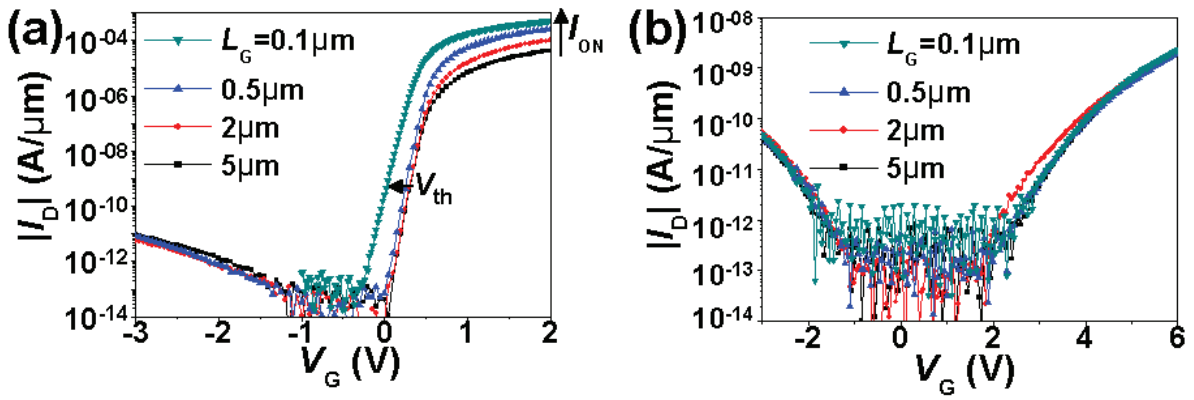

Fig. 2.6: Measured I_D-V_G characteristics (V_D = 1 V) of (a) MOSFETs and (b) TFETs with L_G decreasing from 5 μm to 100 nm. The I_{ON} of MOSFETs tends to increase as L_G decreases and V_{th} decreases due to short channel effects. The I_D of TFETs remains stable even when L_G decreases to 100 nm.

In TFETs, the same trapping-detrapping process occurs at Si-SiO_2 interface as in MOSFETs. However, the impact of this process depends on the location of the traps. First, the trapping can modulate the channel conductance, just as in a MOSFET, but as we have

discussed already, the fluctuations in the channel conductance have a negligible effect on I_D. Second, the trapping-detrapping events near the tunneling junction can change the maximum junction electric field E_{max}, causing fluctuations in the interband tunneling rate which is exponentially dependent on E_{max} [12]. The corresponding area is determined by the detailed structure and gate/drain bias of TFET, but it is generally very narrow (< 10 nm) [39]. Hence, the effective LFN-generating area of the TFET is very small (< 0.05 μm^2 for device width W = 5 μm), including only a discrete numbers of traps, just as in a very small MOSFET. This is why the RTS noise with large variation is observed in TFETs even if the gate area is nominally large.

Due to its extremely small effective gate length, the amplitude of RTS noise in TFETs is comparable to that in very small MOSFETs, even though the transconductance is much lower. In the TFET of Fig. 2.6(a), the sensitivity of the amplifier is 1×10^{-8} A/V which indicates the maximum fluctuation in I_D is ~5%. As TFET performance is enhanced by the introduction of alternative low bandgap materials (Ge) and more effective electrostatic modulation of tunneling junction electric field, we can expect that RTS noise will become a dominant noise in the TFET.

2.3 Suppression of leakage current by asymmetrical structure

A potential problem with symmetrical TFETs is the large I_{LEAK} under opposite gate bias, because interband tunneling can occur at either the source-channel or the drain-channel junction depending on the sign of V_G. This ambipolar I_{LEAK} can be more severe for TFETs based on low bandgap semiconductors, such as Ge, see Fig. 2.7 [20].

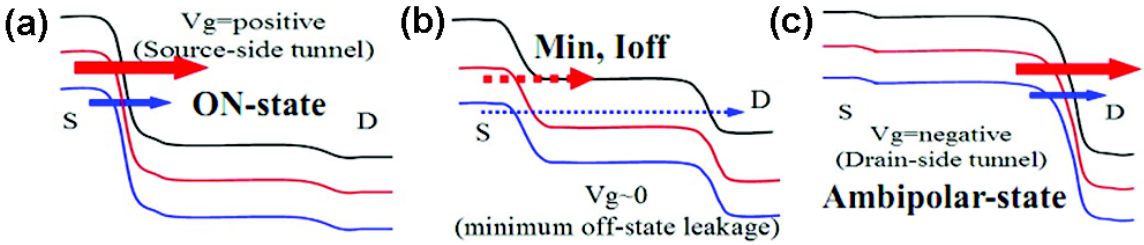

Fig. 2.7: Band-diagrams showing a symmetrical *n*-type TFET in (a) ON state with $V_G > 0$, (b) OFF state with $V_G = 0$ and (c) ambipolar state with $V_G < 0$. High leakage current occurs due to parasitic tunneling in ambipolar state, especially in TFET with low band-gap material [20].

The solution is to introduce an asymmetrical architecture, such as unequal source/drain doping [20], intrinsic region and heterojunction [40]. Among these solutions, the introduction of intrinsic region is the simplest, requiring an easy change in the photomask. This method

was originally proposed in a simulation paper [41]; the first experimental data have been presented in [18]. Here, we present a systematic study by the combination of simulation and experiment. We also demonstrate the possibility of completely suppressing the ambipolar I_{LEAK}.

Figure 2.8 shows the structure of the asymmetrical TFET with an intrinsic region (L_{IN}) separating the drain from the gate. The fabrication is the similar to the symmetrical TFET as Fig. 2.1, except that a Si_3N_4 protection layer is formed prior to the implantation of source/drain.

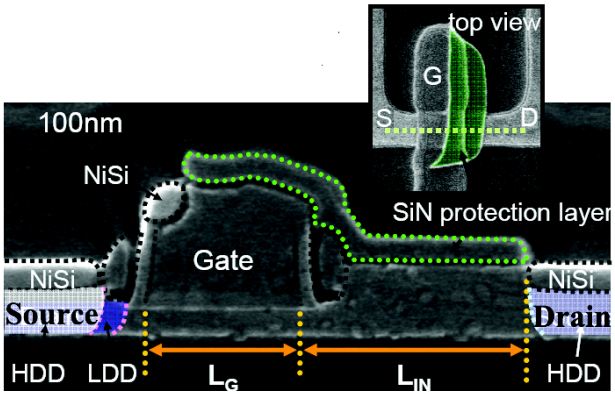

Fig. 2.8: Structure of the asymmetrical TFET with intrinsic region L_{IN} [18].

Figure 2.9 shows the I_D-V_G measurements on *n*-type TFETs with various L_{IN}. The device parameters are T_{ox} = 6 nm SiO_2, T_{si} = 20 nm, T_{BOX} = 145 nm and L_G = 400 nm. Under V_D = 1 V, the leakage current on V_G < 0 of the *n*-type TFET with L_{IN} =10 nm is even higher than the ON current obtained at V_G > 0, see Fig. 2.9(a).

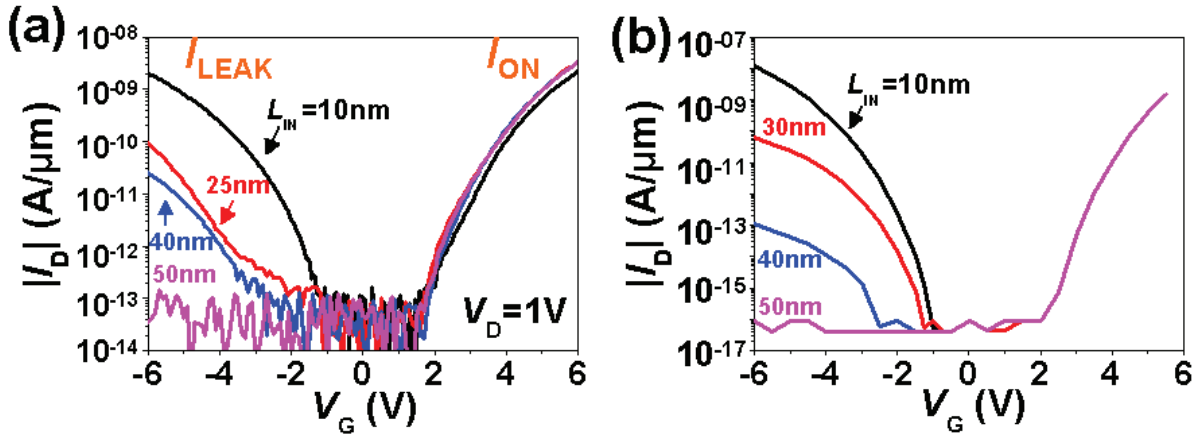

Fig. 2.9: (a) Experimental and (b) simulated I_D-V_G curves of *n*-type TFETs with different L_{IN} from 10nm to 50nm showing that the increase of L_{IN} largely suppresses the leakage current, while the I_{ON} is not affected. The device parameters are T_{ox} = 6 nm SiO_2, T_{si} = 20 nm, T_{BOX} = 145 nm and L_G = 400 nm, under V_D = 1 V.

As the L_{IN} increases, the I_{LEAK} is reduced apparently. With L_{IN} = 50 nm, the I_{LEAK} is suppressed below the noise level, whereas I_{ON} is kept constant. Figure 2.9(b) shows the TCAD simulation in Silvaco using local Kane's model, reproducing the experimental results well.

To understand the mechanisms, the maximum electric field (E_{max}), determining the band-to-band tunneling rate, is extracted from the simulation of *n*-type TFETs with different L_{IN}. Figure 2.10 shows the evolution of E_{max} in ON and OFF states, as L_{IN} increases from 0 nm to 50 nm. Under V_G = –6 V, the TFET is in OFF state and holes are accumulated in the channel beneath the front gate, forming a tunneling *p*-*n* junction at drain side where the intrinsic region is located, see Fig. 2.10(a). For the TFET with L_{IN} smaller than 20 nm, the E_{max} in the OFF state is even slightly larger than in the ON state due to the higher voltage difference between gate and drain ($|V_G$-$V_D|$). However, as L_{IN} increases beyond 20 nm, the E_{max} at the drain side falls quickly. Since the BTBT rate is exponentially dependent on E_{max} [12], it can be suppressed at the drain side by increasing L_{IN}.

However, under positive gate bias, the TFET is in the ON state and the tunneling occurs at source side. The E_{max} at the source side is almost constant as L_{IN} increases due to the negligible potential drop on L_{IN} region, see Fig. 2.10(c), resulting in a constant I_{ON}.

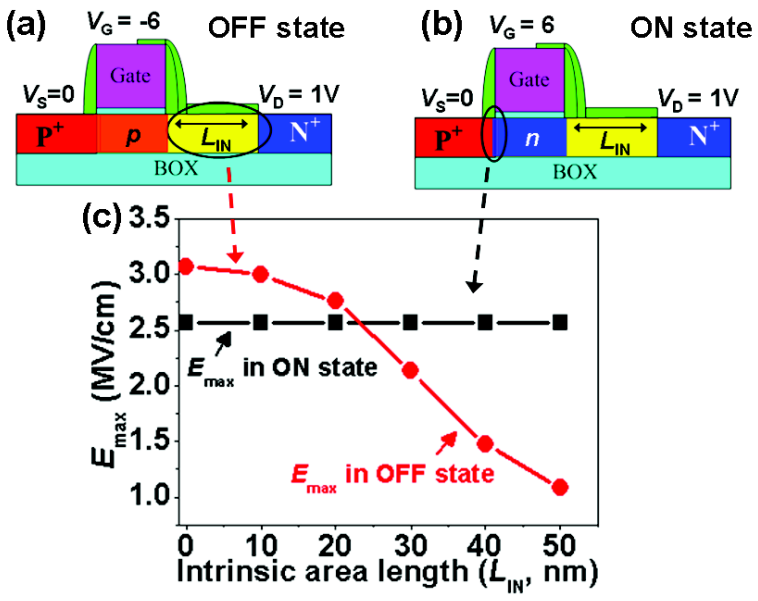

Fig. 2.10: Schematic view of the *n*-type TFET operating in (a) OFF and (b) ON states with V_G=-6V and 6V, respectively. (c) The evolution of E_{max} in ON and OFF states of TFETs with different L_{IN}.

In *p*-type TFETs, the I_{ON} is also unaffected by L_{IN}, as can be seen in Fig. 2.11(a). However, the full suppression of I_{LEAK} in *p*-type TFETs requires a larger L_{IN} = 100 nm. We

attribute this difference to the diffusion coefficients of boron (B) and arsenic (As) in Si. Figure 2.11(b) shows the simulated doping profiles of implanted B and As after the activation anneal. All parameters in simulation were adjusted according to the fabrication process. As previous work indicates [20], a doping concentration which is lower than 1×10^{18} cm^{-3} can be used to effectively suppress the tunneling. In our case, the I_{LEAK} results from the tunneling at drain side which is doped by As and B in *n*-type and *p*-type TFETs, respectively. The characteristic diffusion distance from the edge of spacer to the 10^{18} cm^{-3} value point is ~40 nm for As and ~90 nm for B, as shown in Fig. 2.11(b), qualitatively explaining our experimental observations.

The same tendency applies to TFETs with 3 nm HfO_2 gate oxide and EOT = 2.2 nm. As shown in Fig 2.12(a), the I_{LEAK} of *n*-TFETs with same dimension as in Fig. 2.9 except the gate oxide, drops rapidly as L_{IN} increases. Note that the residual I_{LEAK} as L_{IN} exceeds 50 nm is caused by gate leakage, which cannot be suppressed by increasing L_{IN}. However, for HfO_2-based *p*-type TFETs, L_{IN} as long as 100 nm reduces the I_{LEAK} but cannot completely suppress it, due to both the effects of the longer B diffusion length and stronger gate control of E_{max}, see Fig. 2.12(b).

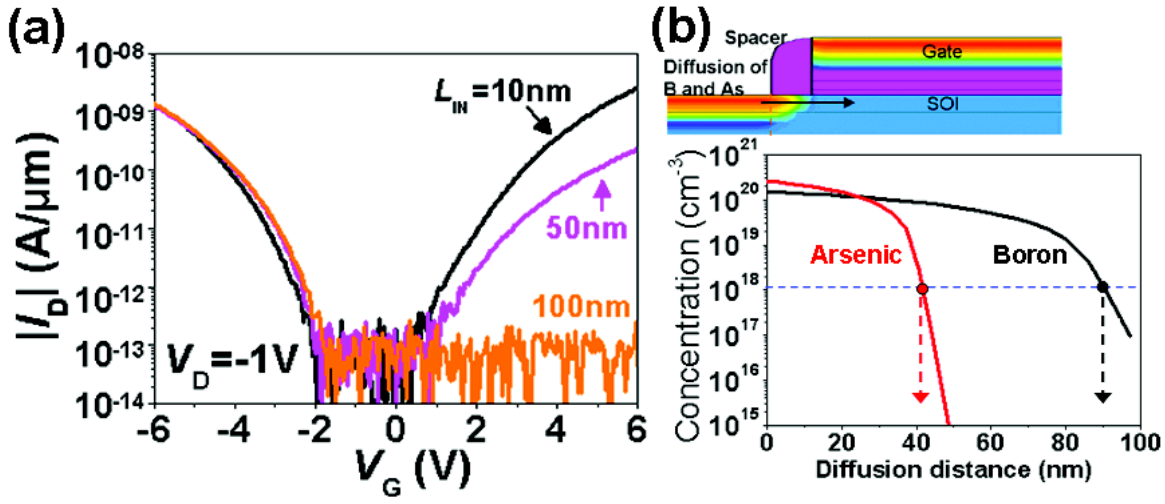

Fig. 2.11: Measured I_D-V_G curve of *p*-type TFETs with SiO_2 gate oxide and different L_{IN} (a) and the simulation of the lateral diffusion profiles of boron and arsenic dopants (b). The dotted line indicates the boundary, where the doping concentration drops down to 1×10^{18} cm^{-3}. The device parameters are the same as in Fig. 2.9.

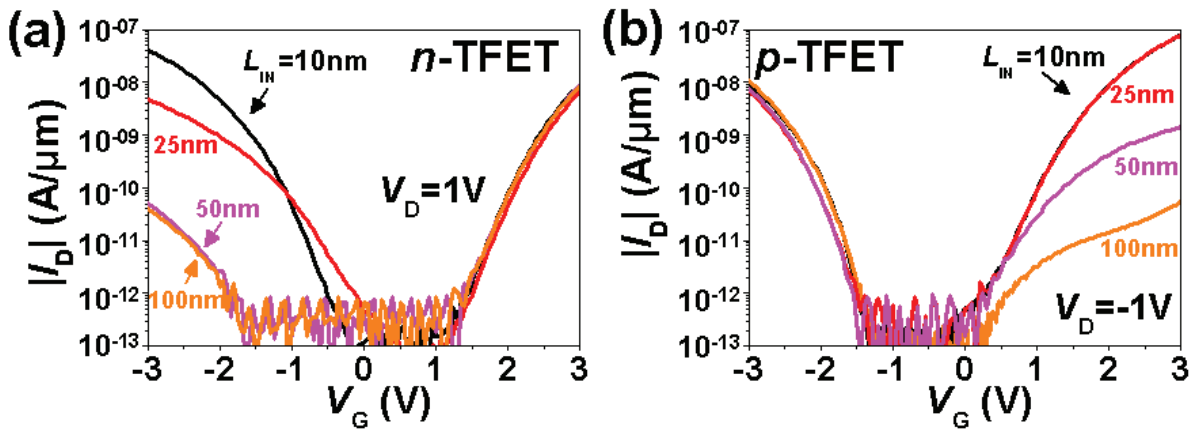

Fig. 2.12: Measured I_D-V_G curves of *n*-TFETs (a) and *p*-TFETs (b) with 3 nm HfO_2 gate oxides and different L_{IN}.

2.4 Enhancement of the ON current

To date, a major challenge for TFETs has been the very low I_{ON}, typically 3-5 decades lower than a MOSFET fabricated in the same process. In order to increase I_{ON}, one can replace SiO_2 gate oxides with HfO_2 and obtain higher electric fields. Further increase in the tunneling current can be achieved by using a lower band-gap material ($Si_{0.65}Ge_{0.35}$) in the channel instead of Si.

2.4.1 High-k gate oxide to enhance I_{ON}

A comparison of I_D-V_G curves of TFETs with different gate oxides and L_G = 400 nm under $|V_D|$ = 1 V is shown in Fig. 2.13. Both *n*-type and *p*-type devices are compared, biased as in Fig. 2.1(a). Since there exists no unambiguous definition of ON current I_{ON} and *SS* in TFET, for comparison purposes, we define the I_{ON} at constant $|V_G|$ = 3V and $|V_D|$ = 1V, and extract the *SS* value when I_D reaches 2×10^{-12} A/μm. As can be easily observed in Fig. 2.13(a), TFETs with HfO_2 gate oxide have higher I_{ON} than those based on SiO_2. The *SS* values are also markedly reduced. This is due to the reduction of equivalent oxide thickness (EOT) using high-k gate dielectric, as demonstrated by the C-V measurement, shown in Fig. 2.13(b). Thanks to EOT = 2.2 nm, the device with 3nm HfO_2 gate oxide device has much higher electric field at tunneling junction than that with SiO_2.

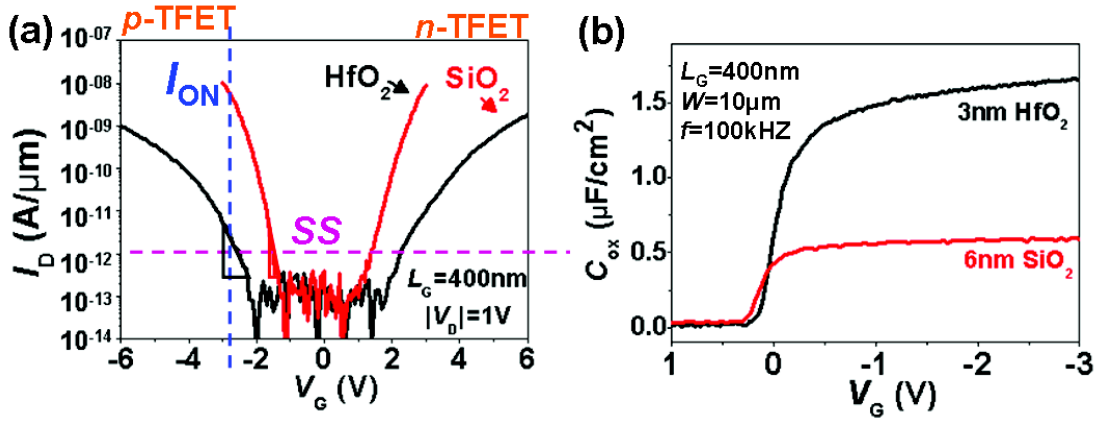

Fig. 2.13. (a) I_D-V_G measurements comparing the *n*-type and *p*-type TFETs with various gate oxides. (b) C-V measurement showing much lower EOT of HfO_2 gate oxide than SiO_2.

As described in Fig. 2.14, the performance of TFET is independent of L_G. This due to the fact that at low I_D the tunneling current is determined by the maximum electric field at the tunneling junction and unaffected by the carrier transport in the channel [39]. Figure 2.14(a) shows that I_{ON} is less than 10^{-11} A/μm for both *n*-type and *p*-type TFETs with SiO_2, whereas I_{ON} increases over 10^{-8} A/μm for those with HfO_2 gate oxide. As for the *SS* value, shown in Fig. 2.14(b), both *n*-type and *p*-type TFETs with SiO_2 have *SS* ~ 1.1 V/decade, which is reduced to 0.33 V/decade in devices with HfO_2.

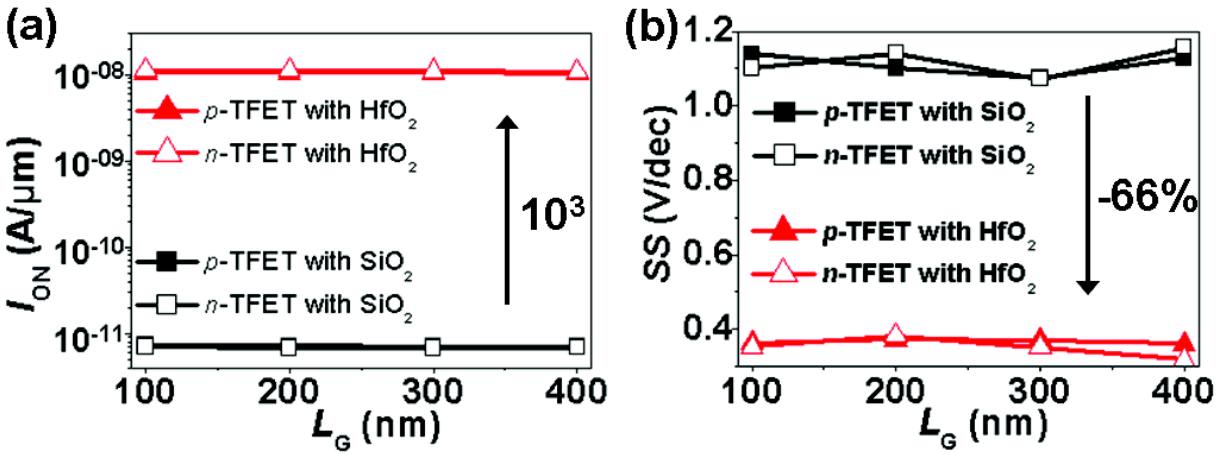

Fig. 2.14. Comparison of both the *n*-type and *p*-type TFETs with L_G from 400nm to 100nm showing that (a) the I_{ON} and (b) *SS* are largely improved by using HfO_2 gate oxide instead of SiO_2.

The comparison reveals that thinner EOT leads to higher I_{ON} and lower *SS* values due to the better electrostatic controllability from the gate. The theoretically achievable $S < 60$ mV/dec value in TFETs needs excellent electrostatic control of the maximum junction field, which requires minimizing gate EOT and sharpening the S/D lateral doping profile. As a

result, the experimental reports of low *SS* published thus far [2, 6, 18, 20] have generally suffered from low I_{ON}, at least for reasonable V_D values.

2.4.2 Use of $Si_{1-x}Ge_x$ in channel to enhance I_{ON}

Low band-gap materials, such as $Si_{1-x}Ge_x$ [18], Ge [20] and III-V semiconductors [22], are commonly used to further enhance the I_{ON} in TFET. In this work, $Si_{0.65}Ge_{0.35}$ is used in the channel to replace the Si, and thus increase the band-to-band tunneling rate. The $Si_{0.65}Ge_{0.35}$ is fabricated by SiGe enrichment process, described in Fig. 2.15(a) [42]. A 53nm $Si_{0.9}Ge_{0.1}$ layer is epitaxially grown on the SOI substrate followed by the thermal oxidation. The Si atoms at the surface are oxidized and sacrificed, whereas the Ge atoms diffuse inside the $Si_{1-x}Ge_x$ layer and enrich the content of Ge [43]. A 15nm strained $Si_{0.65}Ge_{0.35}$ layer is obtained and used as the active layer of TFET. Figure 2.15(b) compares the I_D-V_G measurements on TFETs with Si and $Si_{0.65}Ge_{0.35}$. The I_{ON} is enhanced by using $Si_{0.65}Ge_{0.35}$, albeit with higher leakage current and degraded *SS*, probably due to trap assisted tunneling and thermal generation.

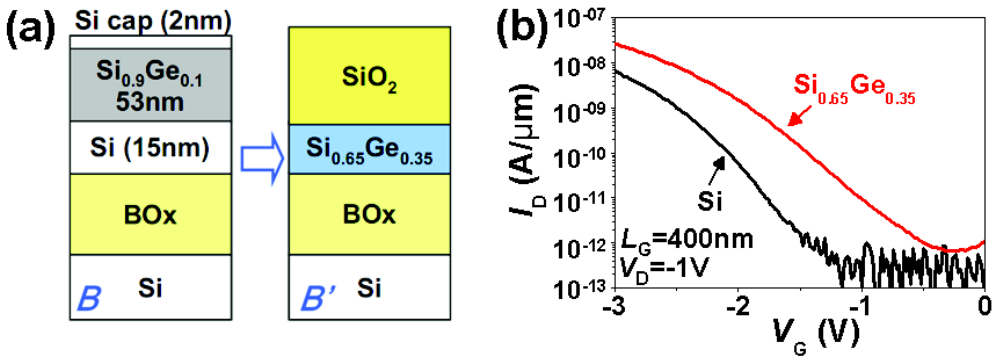

Fig. 2.15: Schematic view of the SiGe enrichment process [42]. (b) Comparison of the TFETs with either Si or $Si_{0.65}Ge_{0.35}$ in the channel. For both of the devices, parameters are T_{ox} = 3 nm HfO_2, T_{BOX} = 145 nm and L_G = 400 nm under V_D = -1 V.

2.5 Conclusions

In this chapter, we present both TFETs and MOSFETs fabricated in the same FD-SOI process. The measurements under various temperatures have been performed on the TFETs, showing that the current increases slightly as temperature increases, differing from conventional MOSFETs. The LFN measurements revealed that the RTS noise with high amplitude is dominant in TFET with large dimension, contrary to large MOSFET, where 1/*f* noise is dominant. This demonstrates that the current in TFET is controlled by the narrow tunneling junction.

In order to reduce the I_{LEAK}, asymmetrical TFETs with intrinsic ungated regions L_{IN} have been studied. For the *n*-type TFET with SiO_2 gate oxide, a 50nm L_{IN} is enough to suppresses the I_{LEAK} effectively without degrading I_{ON}. Whereas, longer L_{IN} region is needed for *p*-type devices with HfO_2 gate oxide due to the long diffusion length of Boron and strong control of the gate.

We have studied TFETs with various gate oxides, channel materials and structures in order to overcome the inadequate I_{ON}. We show that the use of HfO_2 gate oxide enhances the I_{ON} by a factor of ~10^3 and reduces the *SS* by 60%. Further enhancement of I_{ON} was achieved by using a $Si_{0.65}Ge_{0.35}$ channel.

Chapter 3: TFET modeling and GIDL current in TFETs and FD-SOI MOSFETs

In this chapter, we present a model for the tunneling field-effect transistor (TFET) comprising a series connection of a MOSFET with a gate-controllable tunnel diode (GTD). Through the introduction of the MOSFET in our model, both operational regimes of TFET are handled correctly, with the tunneling junction dominating at low interband tunneling current and the channel transport dominating at high tunneling current. The comparison between our model, TCAD simulations and experimental data on TFETs with different gate oxide and channel thicknesses over the full range of gate and drain bias confirms the model's reliability and accuracy. At low tunneling current, the model further simplifies to a compact analytical model. With minor modifications, our model can also be applied to multi-gate TFET architectures.

The developed model is further extended to explain the gate-induced drain leakage (GIDL) in FD-SOI TFETs and MOSFETs. In long-channel MOSFETs, the GIDL current is lower than in TFETs with similar junction doping, due to the voltage drop at the source tunnel junction. We develop a GIDL model combining a tunneling junction at the source with a forward-biased diode at the drain that agrees well with experimental results.

3.1 Background of the TFET modeling

As the experimental performance of TFETs is improved by using the high-k gate oxides [18], low band-gap materials [20] and multi-gate structures [2], comprehensive models are urgently required to reliably predict TFET performance.

In the past, TCAD simulations combining the local Kane's model [12] with numerically obtained potential distributions have been used for qualitative analysis and TFET performance predictions [14, 44-45]. A more precise and complicated numerical method using non-equilibrium Green's function (NEGF) is also available [46-47]. On the other hand, an analytical model would be very useful to aid physical understanding and provide quick predictions, and indispensable for circuit-level simulation and modeling.

Several analytical TFETs models have been published to date [48-51]. They are generally based on analytically solving the Poisson equation at the tunneling junction and then calculating the tunneling current by inserting the obtained electric field into Kane's model for interband tunneling. In [50], the channel was assumed to be always fully depleted, so that the effect of drain voltage (V_D) on tunneling junction is excluded. Even in models that include the effect of V_D, however, the channel is still assumed to be depleted, which is usually incorrect at high gate voltage (V_G) in a long-channel TFET [51], where the channel is much longer than the characteristic length L_d [16]. None of the models published to date quantitatively captures the two working regimes in a long-channel TFET: the "saturation regime" in which the tunneling current is independent of V_D and the "linear regime" in which the current depends on both V_D and V_G. Furthermore, carrier transport along channel is typically ignored, even though the channel transport is expected to limit I_{ON} in TFETs with a sufficiently high tunneling rate.

3.2 New model of TFET combining tunneling and channel transport

In this chapter, we propose an analytical model for the TFET regarded as series connection of a gate-controllable tunneling diode (GTD) with a MOSFET [52]. The potential distribution around the tunneling junction is obtained by solving the Poisson equation with the pseudo-2D method [48] [51], including the influence of the channel potential that is determined by the series-connected MOSFET. Kane's model serves to derive the tunneling current, but using the average electric field along shortest tunneling width (E_{TW}) rather than the local maximum electric field (E_{max}) [50] [53]. By combining the current-voltage equations of the GTD and MOSFET, the channel potential is determined in both linear and

saturation regimes, yielding the actual value of I_D. Generally, the channel transport in the MOSFET must be solved numerically, but our model reduces to a compact and explicit analytic expression if the tunneling rate is relatively low.

The model was validated by comparing the predicted potential profile at the tunneling junction with TCAD simulations for various biasing values, gate oxide (T_{ox}) and channel (T_{Si}) thicknesses. Further, our model accurately predicts experimental *I-V* data over a wide range of biasing with interband tunneling parameters that agree with published results. Finally, the model can be easily extended to multi-gate structures and used to predict the performance of TFETs with different technological parameters (gate oxide thickness, channel thickness), device geometries and alternative materials.

3.2.1 Model derivation

A schematic view of a *p*-type TFET (PTFET) is shown in Fig. 3.1(a). At sufficiently negative V_G, a reverse-biased tunneling junction is formed at the source side. As illustrated in Fig. 3.1(b), we model this TFET as the series connection of a *p*-type MOSFET at the drain side with a GTD at the source. The PMOSFET has a well-defined drain voltage V_D, but its virtual source at the start of the channel coincides with the cathode of the GTD and is at a potential V_C determined by current continuity.

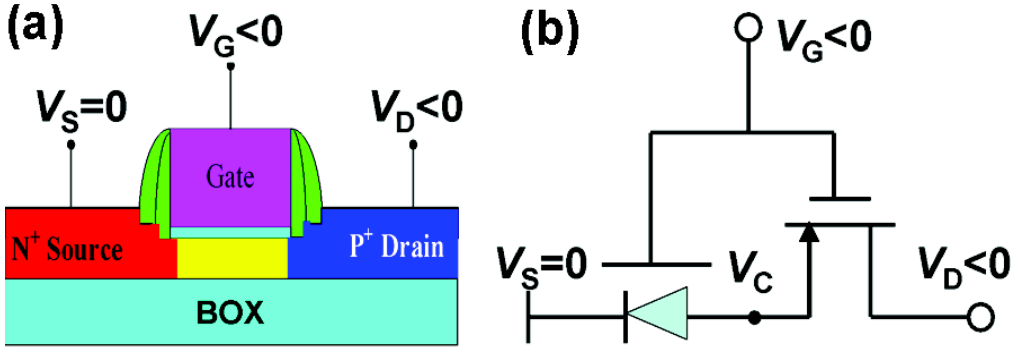

Fig. 3.1: (a) Schematic view of a *p*-type TFET with gate and drain negatively biased. The schematic structure with raised source/drain and two spacers is the same as our measured devices. (b) The proposed model of the *p*-type TFET in which the channel and drain belong to a MOSFET in series with the gate-controllable tunneling diode located at source.

We have performed TCAD simulations using Silvaco Atlas (version 3.18.17.R) to analyze the TFET and MOSFET properties. Figure 3.2 compares the surface potential profiles of the MOSFET with two TFETs possessing either a normal or an exaggerated interband tunneling rate. The exaggerated tunneling rate is implemented by directly decreasing the exponential

parameter B_K in Kane's model [12] from 21 MV/cm to 1 MV/cm, mimicking an optimized future TFET structure with higher tunneling (achievable, for example, by implementing the GTD in a lower bandgap material like Ge). For the TFET with normal Si junction tunneling rate, the potential drop in the channel is minimal, except for the pinched off depletion region near the drain. However, if the tunneling rate is large, the high I_{ON} of TFET induces a large potential drop in the channel. The surface potential of the TFET with exaggerated tunneling rate is almost the same as that of the MOSFET in the channel and drain regions except for the extra drop at the source junction due to the built-in junction potential, as shown in Fig. 3.2. As a result, if the tunneling rate is high enough, only a small potential drop is needed at the tunneling junction to produce a high current; the current will be restricted by the carrier transport along the channel, so a TFET with a high tunneling rate degenerates into a MOSFET.

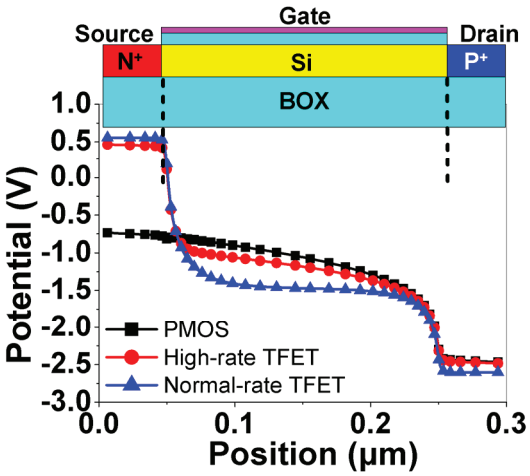

Fig. 3.2: Comparison of TCAD-simulated surface potentials between three devices: TFET with normal Si interband tunneling rate; TFET with exaggerated tunneling rate; and a regular MOSFET without a tunneling junction at the source. The simplified structure of the simulated TFET is shown in the upper inset of Fig. 3.2. The simulated MOSFET is identical to the TFET, except that both source and drain are p^+ doped. The PTFET with exaggerated tunneling rate has the same potential profile as the MOSFET. The simulated device has L_G = 200 nm, T_{Si} = 20 nm and T_{ox} = 2 nm with bias of V_G = –1.5 V and V_D = –2 V.

3.2.1.1 Current continuity and *I-V* characteristic of the tunneling junction

The TFET *I-V* characteristics can be obtained by using current continuity and setting the current $I_D(V_G, V_C)$ of the GTD equal to the $I_D(V_G, V_D–V_C)$ of the series-connected MOSFET

with its source at V_C. We need to combine the well-known I-V relations for MOSFET [3] with a model incorporating the V_G and V_C dependence of the GTD current.

One possible approach is to solve the Poisson equation at the junction and then use the obtained maximum electric field (E_{max}) in the local Kane's model [12]. However, the use of E_{max} can greatly overestimate the tunneling current due to the non-uniformity of the electric field at tunneling junction. Instead, the use of the mean electric field (E_{TW}) along the shortest tunneling width (L_{TW}) in the WKB approximation of interband tunneling has been shown to be more accurate in planar Si *pn* tunnel junctions [53].

A schematic view of a GTD on SOI substrate is shown in Fig. 3.3(a). Since the tunneling rate decreases exponentially with increasing tunneling width, the analytical model is still fairly accurate by only considering the shortest tunneling path. This significantly simplifies the analytical model. The surface potential along the tunneling direction can be determined by the electrostatic potentials of the gate ($\varphi_G = V_G - V_{FB}$), source ($\varphi_S = V_S + V_{biS}$), and channel ($\varphi_C = V_C + V_{biC}$), referenced to the midgap Fermi level E_i in the nominally undoped channel [3]. Note that the two terms in the channel potential (φ_C) consist of the channel voltage V_C induced by the current flow through the channel and drain junction and the channel built-in potential V_{biC} that reflects the change of the Fermi level in the channel induced by the V_G.

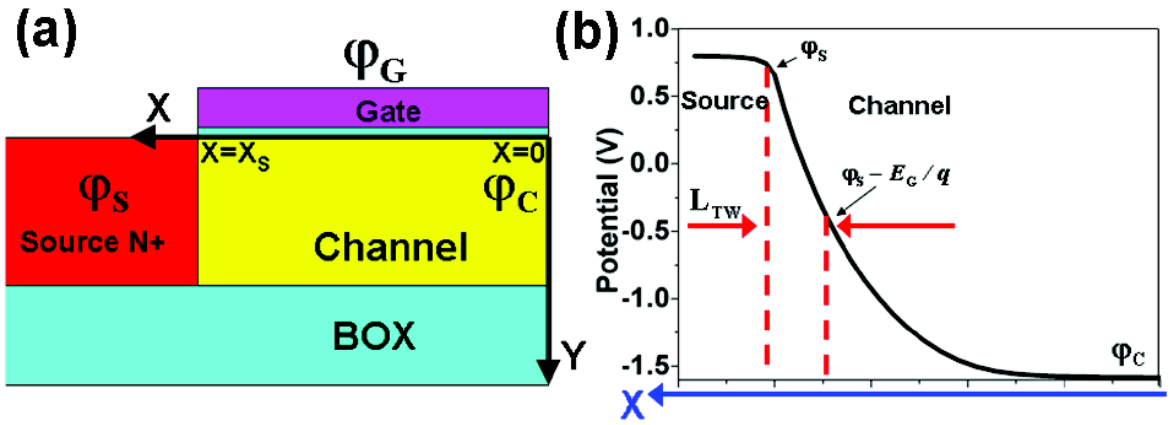

Fig. 3.3. (a) Schematic view of the tunneling junction in which the potential distribution is determined by the potentials of the gate φ_G, source φ_S and channel φ_C. (b) Potential profile along the tunneling junction obtained from TCAD simulation showing the shortest tunneling width L_{TW} between the source at potential φ_S and the point where the surface potential equals ($\varphi_S - E_G/q$).

The Poisson equation around the junction in intrinsic channel can be expressed as

$$\frac{\partial^2 \varphi(x,y)}{\partial^2 x} + \frac{\partial^2 \varphi(x,y)}{\partial^2 y} = 0 \qquad (3\text{-}1)$$

where φ(x,y) is the potential with respect to channel Fermi level and the doping N_A in the nominally undoped channel is assumed to be negligible. Using a second order polynomial, the potential can be approximated as [51, 54]:

$$\varphi(x,y) = a_0(x) + a_1(x)\cdot y + a_2(x)\cdot y^2 \tag{3-2}$$

From the vertical boundary condition in the channel, one can obtain:

$$\begin{aligned}
&\varphi(x,0) = \varphi_t(x)\\
&\varphi(x,T_{si}) = \varphi_b(x)\\
&E(x,0) = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{T_{ox}}\cdot[\varphi_G - \varphi_t(x)]\\
&E(x,T_{si}) = \frac{\varepsilon_{ox}}{\varepsilon_{si}}\cdot\frac{1}{T_{BOX}}\cdot[\varphi_b(x) - \varphi_{BG}] \approx 0
\end{aligned} \tag{3-3}$$

where $\varphi_t(x)$ and $\varphi_b(x)$ represent the top and bottom
surface potential along the channel respectively. φ_G is the gate potential defined as: $\varphi_G = V_G - V_{FB}$ where V_{FB} is the flat band voltage. ε_{si} and ε_{ox} represent the dielectric constants for the channel material and gate oxide with thickness of T_{si} and T_{ox}, respectively. Since the back gate oxide thickness (T_{BOX}) is normally large for a single gate SOI device, the back interface electric field $E(x, T_{si})$ can be neglected.

Substituting Eq. (3-2) into Eq. (3-3), the coefficients (a_0, a_1 and a_2) in Eq. (3-2) can be expressed by the top surface potential as:

$$\begin{aligned}
&a_0(x) = \varphi_t(x);\quad a_1(x) = -\frac{T_{si}}{L_d^{\,2}}\cdot[\varphi_G - \varphi_t(x)];\quad a_2(x) = \frac{1}{2\cdot L_d^{\,2}}\cdot[\varphi_G - \varphi_t(x)]\\
&\text{with}\quad L_d = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}}\cdot T_{ox}\cdot T_{si}}
\end{aligned} \tag{3-4}$$

where L_d is the characteristic decay length determined by the T_{ox} and active layer T_{si} thicknesses. The differential equation of surface potential can be obtained by substituting Eq. (3-2) into the Eq. (3-1) with the coefficient functions defined by Eq. (3-4).

$$\frac{\partial^2\varphi_t(x)}{\partial^2 x} - \frac{\varphi_t(x)}{L_d^{\,2}} = -\frac{\varphi_G}{L_d^{\,2}} \tag{3-5}$$

The solution of top surface potential in Eq. (3-5) has the form of:

$$\varphi_t(x) = C\cdot e^{\frac{x}{L_d}} + D\cdot e^{-\frac{x}{L_d}} + \varphi_G \tag{3-6}$$

where C and D are the coefficients determined by the lateral boundary conditions of the channel region. After inserting the channel boundary conditions, one obtains:

$$\varphi_t(x) = (\varphi_C - \varphi_G) \cdot cosh(\frac{x}{L_d}) + \varphi_G \tag{3-7}$$

From Eq. (3-7), as x decreases toward zero, the potential decays from φ_S at source side to φ_C at channel with the decay length L_d, as shown in Fig. 3.3(b). This potential profile ensures that the shortest tunneling barrier width L_{TW} lies along the source-channel direction and is determined by the point where the surface potential falls by ~E_G/q below the source potential φ_S. From Eq. (3-7), we further obtain:

$$x(\varphi_t) = L_d \cdot cosh^{-1}(\frac{\varphi_t - \varphi_G}{\varphi_C - \varphi_G}) \tag{3-8}$$

such that

$$\begin{aligned} L_{TW} &= x(\varphi_S) - x(\varphi_S - \frac{E_G}{q}) = \\ & L_d \cdot [cosh^{-1}(\frac{\varphi_S - \varphi_G}{\varphi_C - \varphi_G}) - cosh^{-1}(\frac{\varphi_S - \frac{E_G}{q} - \varphi_G}{\varphi_C - \varphi_G})] \end{aligned} \tag{3-9}$$

Eq. (3-9) can be converted to a more straightforward form:

$$L_{TW} = L_d \cdot ln[\frac{(\varphi_S - \varphi_G) + \sqrt{(\varphi_S - \varphi_G)^2 - (\varphi_C - \varphi_G)^2}}{(\varphi_S - \varphi_G - \frac{E_G}{q}) + \sqrt{(\varphi_S - \varphi_G - \frac{E_G}{q})^2 - (\varphi_C - \varphi_G)^2}}] \tag{3-10}$$

From Eq. (3-10), we can find the average electric field along the shortest tunneling barrier, $E_{TW} \sim E_G/qL_{TW}$, and then substitute E_{TW} into the Kane model expression for the interband tunneling current [12], yielding:

$$\begin{aligned} & I_D = A_K \cdot E_{TW}^{\ 2} \cdot exp(-\frac{B_K}{E_{TW}}) \\ & with \ \ E_{TW} = \frac{E_G}{q \cdot L_{TW}} = \\ & \qquad \frac{E_G}{q} \cdot \frac{1}{L_d \cdot ln[\frac{(\varphi_S - \varphi_G) + \sqrt{(\varphi_S - \varphi_G)^2 - (\varphi_C - \varphi_G)^2}}{(\varphi_S - \varphi_G - \frac{E_G}{q}) + \sqrt{(\varphi_S - \varphi_G - \frac{E_G}{q})^2 - (\varphi_C - \varphi_G)^2}}]} \end{aligned} \tag{3-11}$$

where A_K and B_K are tunneling parameters determined by the bandgap and carrier mass. The parameter A_K also includes the effective tunneling volume with unit channel width, but it is the B_K parameter in the exponential that dominates the predicted values of I_D.

3.2.1.2. Low current simplification and the two working regimes of a TFET

Combining Eq. (3-11) with the MOSFET equation, both the φ_C and I_D of TFET can be obtained. Due to the nonlinearity of the equations, in the general case they must be solved numerically. However, if the overall TFET current is much lower than that of its MOSFET component (the *p*-type MOSFET of Fig. 3.1(b) with $V_C = 0$), the channel potential φ_C can be simplified by ignoring the potential drop along the channel. In this case, the φ_C in both linear and saturation regimes of the MOSFET component can be expressed as:

$$\begin{aligned} &\varphi_C = V_D + V_{biC} \ \textbf{if} \ \ |V_D| < |V_G - V_{Tth}| \ \textbf{(linear region)} \\ &\varphi_C = V_G - V_{Tth} + V_{biC} \ \textbf{if} \ \ |V_D| > |V_G - V_{Tth}| \ \textbf{(saturation region)} \end{aligned} \tag{3-12}$$

where V_{biC} is the channel built-in potential and V_{Tth} is the threshold voltage of the MOSFET component. This assumption is reasonable for all experimental devices reported to date, since even the best experimental TFETs have I_{ON} about 3 decades lower than MOSFETs built in the same technology [20]. Substituting Eq. (3-12) into Eq. (3-11), an analytical expression for $I_D(V_G, V_D)$ in a TFET is obtained.

As indicated in Eq. (3-12), V_C increases linearly with V_D in the linear regime of the MOSFET and thus the I_D of the GTD depends both on V_G and V_D, according to Eq. (3-11). In the saturation regime of the MOSFET, V_C only depends on V_G and thus the tunneling current is independent of V_D. Note that the $|V_{Tth}|$ of the MOSFET component in the model is slightly larger than the threshold voltage of a standalone MOSFET with $V_C = 0$ (grounded source). This is most easily seen by noting that the non-zero V_C is equivalent to an opposite back gate bias ($V_{BG} = -V_C$) on the MOSFET component, so that the interchannel coupling effect increases the $|V_{Tth}|$ [55].

In the following section, we will verify our model against both TCAD and experimental results measured on Si TFETs fabricated in an FD-SOI process.

3.2.2. Model validation

The validity of the model proposed in Eqs. (3.11) and (3.12) is verified from two aspects. First, the potential expressed by Eq. (3.7) around tunneling junction with φ_C determined by Eq. (3.12) is examined by tracking the surface potential via TCAD simulation. Next, the model is used to quantitatively fit the experimental results with extracted tunneling parameters.

3.2.2.1. Potential profile tracking

The surface potential is the basis for calculating tunneling current and should be determined as accurately as possible. For verifying the reliability of the potential, TCAD simulations are used to obtain the surface potential around tunneling junction and compared with the expression given by Eq. (3-7) for TFETs with a normal Si tunneling rate. Combining Eqs. (3-7) and (3-12), we obtain:

$$\varphi_t(x) = (\varphi_C - \varphi_G) \cdot cosh(\frac{x}{L_d}) + \varphi_G$$

$$\textbf{with } L_d = \sqrt{\frac{\varepsilon_{si}}{\varepsilon_{ox}} \cdot T_{ox} \cdot T_{si}}$$

$$\textbf{and} \qquad (3\text{-}13)$$

$$\varphi_C = V_D + V_{biC} \quad \textbf{if} \quad |V_D| < |V_G - V_{Tth}|$$

$$\varphi_C = V_G - V_{Tth} + V_{biC} \quad \textbf{if} \quad |V_D| > |V_G - V_{Tth}|$$

We verified the predicted potential profile of Eq. (3-13) with TCAD simulations on a simplified model PTFET structure with various T_{ox} and T_{si}. The source and drain have a doping concentration of 1×10^{21} cm^{-3}. The channel is taken as intrinsic with a length of 200 nm. For simplicity, the channel build-in potential V_{biC} in Eq. (3-13) is taken as -0.6 V in all cases.

Figure 3.4 compares the surface potential profile of the tunneling junction from TCAD simulation (dots) to that described by Eq. (3-13) (curves) for TFETs under different biasing with several values of T_{ox} and T_{si}. Figure 3.4(a) shows the tracking results as V_D is fixed at –2 V with V_G swept from –1 to –4 V, from saturation to linear regime. This model device has an SOI structure with 1 nm SiO_2 and 5 nm thick Si channel, at the limits of modern fabrication. The tracking by the model is accurate and reasonable. In the saturation region, as V_G decreases from –1 to –2 V, the channel potential follows the V_G. However, as V_G decreases below –3 V, the channel potential (φ_C) is pinned by the fixed V_D, because the device is now in the linear regime. Similar results can be observed for the situation with fixed V_G and swept V_D, as shown in Fig. 3.4(b).

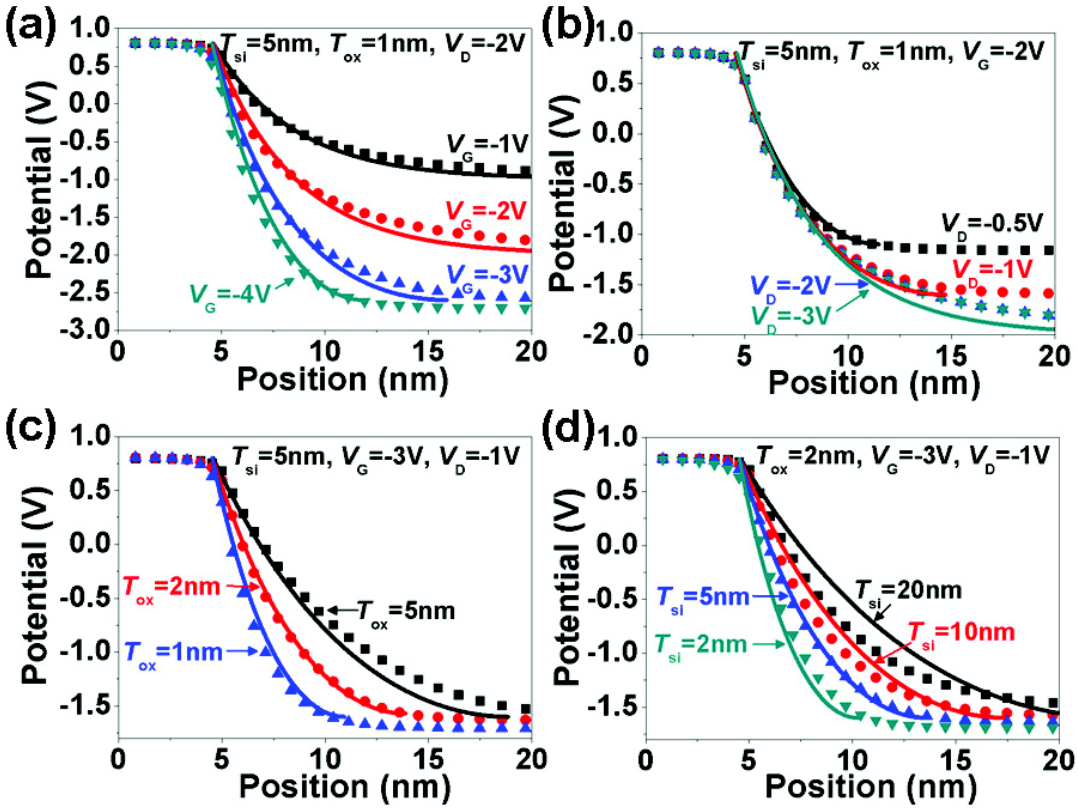

Fig. 3.4: Comparison of the surface potential profile at tunneling junction between TCAD simulation (dots) and the model (curves). The simulated device has the same simplified structure as in Fig. 2.2. (a, b) The model TFETs have T_{ox} = 1 nm and T_{Si} = 5 nm, with biasing (a) V_D = –2 V with V_G swept from –1 V to –4 V and (b) V_G = –2 V with V_D swept from –0.5 V to –3 V. (c, d) The TFETs are biased at V_D = –1 V and V_G = –3 V, with different structures: (c) T_{Si} = 5 nm with T_{ox} varying from 5 nm to 1 nm and (d) T_{ox} = 2 nm with T_{si} varying from 20 nm to 2 nm. The model can explain the effect of T_{ox} and T_{si} reasonably well, except for relatively thick T_{si} > 10 nm.

The structural parameters T_{ox} and T_{si} can strongly affect the potential profile through changing L_d in Eq. (8). As the T_{ox} decreases from 5 nm to 1 nm with a constant T_{si} of 5 nm, the surface potential decays faster, which is accurately reproduced by our model, as shown in Fig. 3.4(c) for simulations with biasing fixed at V_D = –1 V and V_G = –3 V. The influence of the T_{si} for fixed T_{ox} is also accurately reproduced until T_{si} increases over 10 nm, at which point our model overestimates the change in the potential, see Fig. 3.4(d). This discrepancy is due to the polynomial approximation for the 2D potential becoming less reliable at large T_{si} [50] [47]. Since the trend for SOI technology is toward thinner T_{si}, this is not a major problem for our model.

3.2.2.2. Quantitative fitting of experimental results

Having verified the model's ability of accurately track TCAD-simulated potential profiles in simplified TFET structures, we have further verified our model by quantitatively fitting the tunneling current from experimental TFET results. Two different gate oxides, 3 nm HfO_2 and 6 nm SiO_2, with equivalent gate oxide thickness (EOT) of 2.2 nm and 6 nm were used (145 nm buried oxide for all devices). The silicon channel thickness was T_{Si} = 20 nm and gate length L_G = 400 nm. For quantitative fitting of the experimental results, our model requires three parameters: V_{Tth} and the tunneling parameters, A_K and B_K.

In a TFET with low I_D, the threshold voltage V_{Tth} cannot be extracted from the I_D-V_G curve as in a MOSFET. Instead, we extract V_{Tth} from the I_D-V_D curves by considering the current saturation as a function of V_D. Figure 3.5(a) shows an experimental I_D-V_D curve of a PTFET with HfO_2 gate oxide. As V_D increases, the device transitions from linear to saturation regime, with I_D becoming independent of V_D. The extraction of V_{Tth} proceeds from the relative output conductance expressed by $G_{RD} = G_D/I_D$, where $G_D \equiv \partial I_D/\partial V_D$ is the output conductance. As V_D increases to $V_{Dsat} = V_G - V_{Tth}$, we extract V_{Tth} at a given V_G from the point where G_{RD} falls below 0.1, as shown in Fig. 3.5(b).

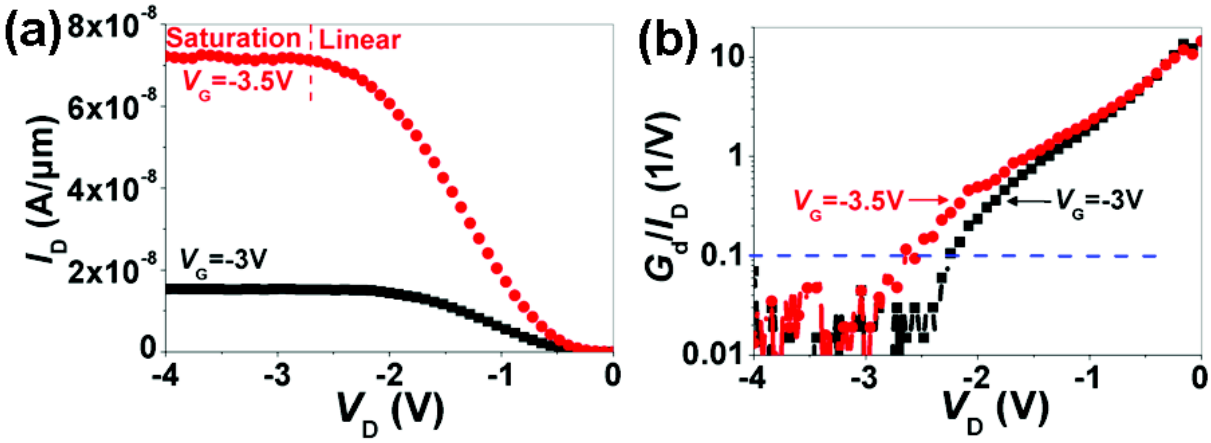

Fig. 3.5: (a) Experimental I_D-V_D PTFET curves *vs.* V_G, showing two distinct working regimes. In the linear regime, I_D changes with V_D, whereas in the saturation regime I_D is unaffected by V_D. (b) The relative output conductance $G_{RD} \equiv G_D/I_D$ where G_D is the output conductance $\partial I_D/\partial V_D$. The constant value of G_d/I_D =0.1V^{-1} is taken to be the saturation threshold V_{Tth}.

Next, the tunneling parameters, A_K and B_K, are extracted from the I_D-V_G curve under a fixed V_D. Figure 3.6(a) shows the I_D-V_G curves of two *p*-type TFETs with HfO_2 and SiO_2 gate oxides at V_D = –2 and –5 V, respectively. The HfO_2-based device has larger I_{ON} and smaller

subthreshold swing (*i.e.*, steeper slope) due to the stronger gate controllability. Taking the logarithm of Eq. (3-11),

$$\ln (I_D/E_{TW}^2) = \ln(A_K) - B_K/E_{TW} \tag{3-14}$$

A_K and B_K are extracted from the slope and intercept of the linear section of the curve shown in Fig. 3.6(b).

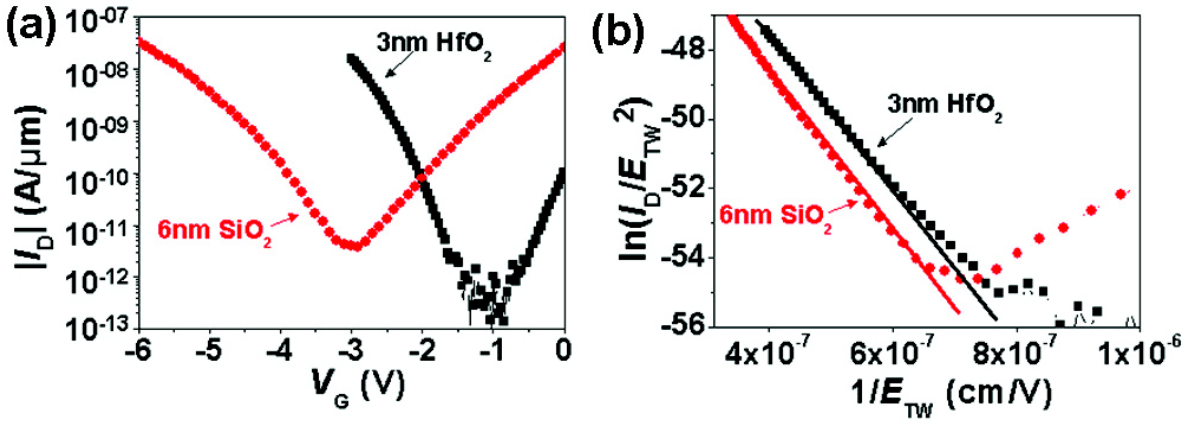

Fig. 3.6: (a) I_D-V_D curves of SOI TFETs with different gate oxides of 3 nm HfO_2 and 6 nm SiO_2 biased at V_D = –2 V and –5 V, respectively. (b) The corresponding linear regions of $\ln(I_D/E_{TW}^2)$ *vs.* E_{TW}^{-1} curves. The tunneling parameters of A_K and B_K can be extracted from the slope and intercept for subsequent quantitative fitting.

The extracted B_K values are around 23 MV/cm for both TFETs with different gate oxides, in agreement with other reports on interband tunneling in Si [51, 53]. Substituting these values into Eq. (3.11) and Eq. (3.12), the tunneling current under different V_G and V_D can be computed. Figure 3.7 shows the fit between our model (curves) and the experimental data (dots) from TFETs with 6 nm SiO_2 and 3 nm HfO_2 gate oxides. The agreement between model and experimental results is good over a large V_G and V_D range. The model does slightly overestimate I_D in the region of very small V_D and high V_G only, see Fig. 3.7(b). We attribute this to the fact that the tunneling model in Eq. (3.11) takes the parameter A_K and hence the tunneling volume to be a constant. For TFETs with small L_d, the electric field is very high under high V_G, but at low V_D the effective tunneling volume is small.

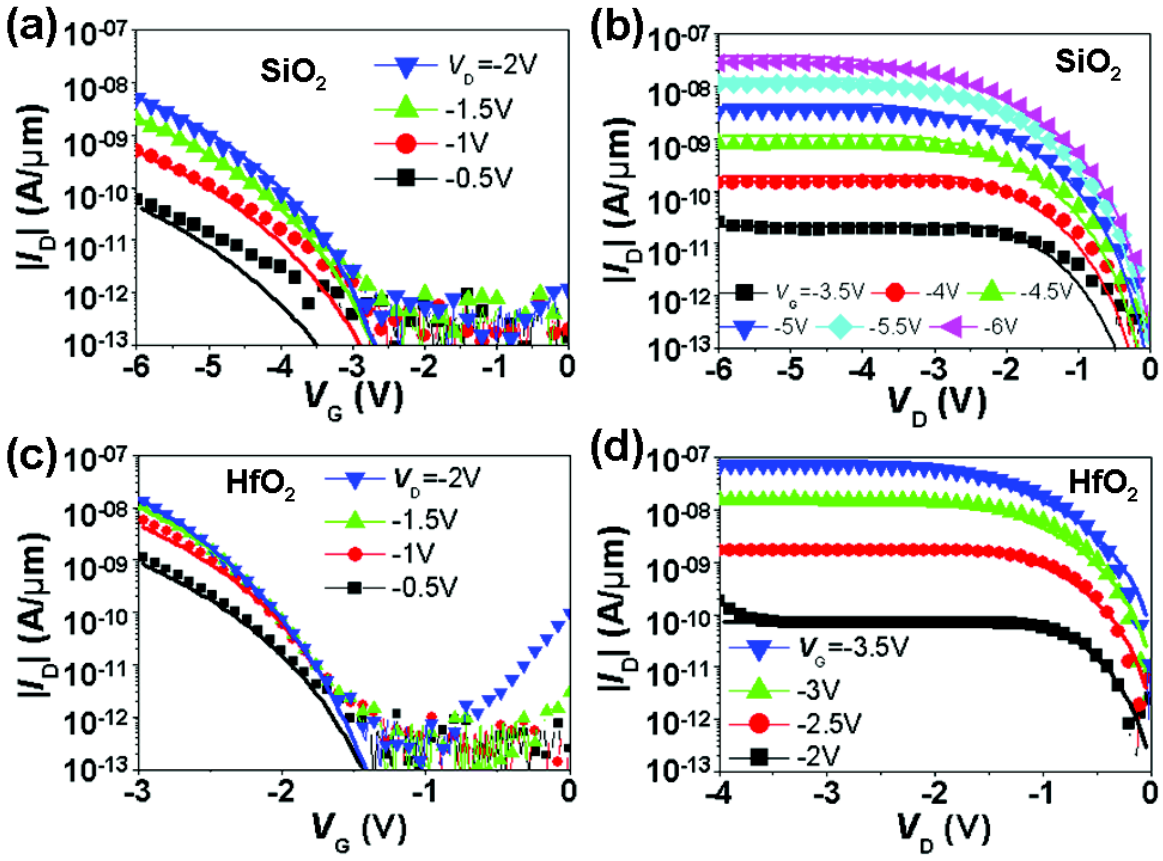

Fig. 3.7: Quantitative model fits (curves) of the experimental results (dots) of (a)(c) I_D-V_G and (b)(d) I_D-V_D characteristics of SOI TFET with (a)(b) 6 nm SiO_2 and (c)(d) 3 nm HfO_2 gate oxides. The fits are accurate except for I_D-V_D curves at low V_D, where the model slightly overestimates the tunneling current.

In Fig. 3.8, the same fitting method is used for a *p*-type TFET with the same HfO_2 gate oxide but $Si_{0.65}Ge_{0.35}$ channel material, resulting in higher I_D. The extracted B_K value is 19 MV/cm, which is ~4 MV/cm lower than for a Si TFET. As shown in Fig. 3.8(a), the current is dominated by trap assisted tunneling (TAT) at low V_G, where the current increases slower than at high V_G [10], but at higher V_G band-to-band tunneling (BTBT) takes over and the data can be well fit by the model (plain lines). The overestimation of the I_D at low V_D is somewhat worse than in Si TFETs due to the lower B_K value of $Si_{0.65}Ge_{0.35}$, as shown in Fig. 3.8(b).

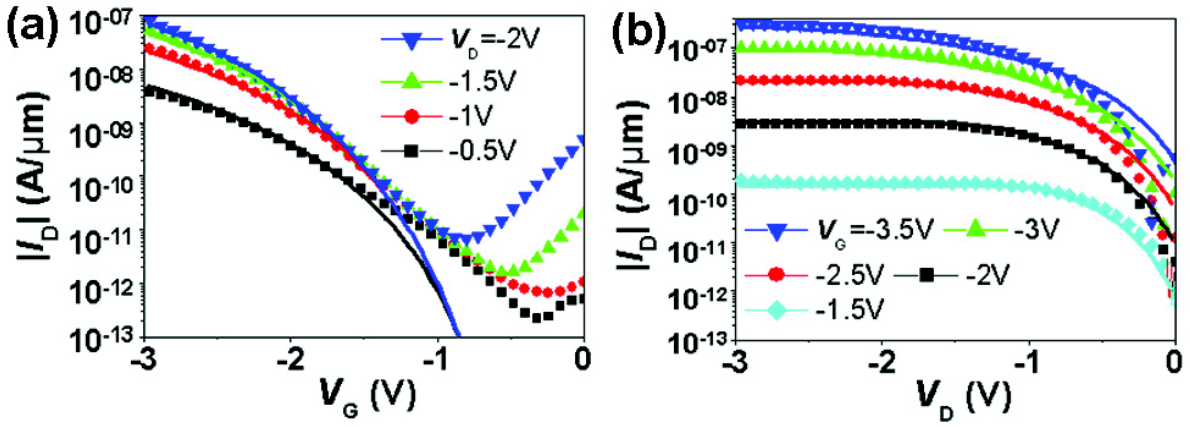

Fig. 3.8: Quantitative model fits (plain lines) of experimental results (symbols) of (a) I_D-V_G and (b) I_D-V_D curves of $Si_{0.65}Ge_{0.35}$ TFETs with 3 nm HfO_2 gate oxide. The bandgap of Si0.65Ge0.35 is taken to be 0.98 eV, corresponding to unstrained SiGe. The overestimation of tunneling current is somewhat worse in the low V_D region compared to the SOI TFET.

3.2.3 Extension to multi-gate devices and performance prediction

The model can be used for multi-gate devices with a slight change in the definition of the decay length L_d, which has the same meaning as the natural length in a MOSFET [56]. The expressions of L_d for Double-Gate (DG) and Gate-All-Around (GAA) structures have been derived as [57] [58]:

$$L_d = \sqrt{\frac{\varepsilon_{si}}{2\cdot\varepsilon_{ox}}\cdot T_{ox}\cdot T_{si}} \quad \text{for } DG$$

$$\text{and} \qquad (3\text{-}15)$$

$$L_d = \sqrt{\frac{2\cdot\varepsilon_{si}\cdot T_{si}^{\,2}\cdot ln\left(1+\frac{2\cdot T_{ox}}{T_{si}}\right)+\varepsilon_{ox}\cdot T_{si}^{\,2}}{16\cdot\varepsilon_{ox}}} \quad \text{for } GAA$$

Figure 3.9(a) compares the performance predicted by the model of TFETs with different gate configurations. The T_{ox}, T_{si} and tunneling parameters are the same as in our experiments. Compared to the single gate device, the usage of double gate structure increases the I_{ON} by a factor of ~10 times, thanks to smaller L_d, leading to a higher tunneling electric field. The predicted *SS* is also significantly reduced.

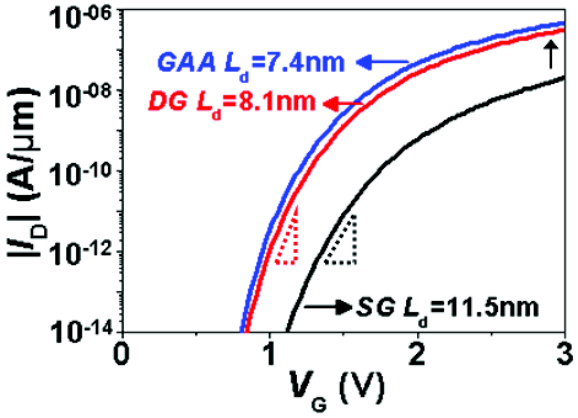

Fig. 3.9: (a) The effect of using a multi-gate TFET structure predicted by the model. The SOI TFET has T_{ox} of 2.2 nm and T_{Si} of 20 nm which is the same as the experimental device. The predicted enhancement of I_{ON} and *SS* by using double-gate (DG) or gate-all-around (GAA) structure is apparent compared to the single-gate (SG) TFET.

Figure 3.10 shows the predicted I_{ON} and *SS* of the TFETs with different L_d and B_K values. The I_{ON} increases almost exponentially as L_d decreases due to the higher electric field. The predicted I_{ON} in silicon TFET with B_K = 23 MV/cm agrees well with the experimental results. The use of high-k gate oxide reduces the L_d and thus increases the I_{ON} by 3 decades. The replacement of Si by $Si_{0.65}Ge_{0.35}$ in the channel reduces the B_K from 23 MV/cm to 19 MV/cm, and thus increases the I_{ON} by 10 times. Further increase of I_{ON} is achieved by using material with even lower B_K, which can be obtained raising the content of Ge in $Si_{1-x}Ge_x$. As for the *SS*, only the Si TFET with HfO_2 shows good agreement between the experiment and the prediction. However, the *SS* is largely underestimated by the prediction for the device with $Si_{1-x}Ge_x$ channel. This may be due to the high density of surface traps at the $Si_{1-x}Ge_x$ channel/oxide interface and to the fact that the trap-assisted-tunneling current, which has a weaker electric field dependence, is dominant at low I_D in the $Si_{1-x}Ge_x$ TFET, as discussed earlier.

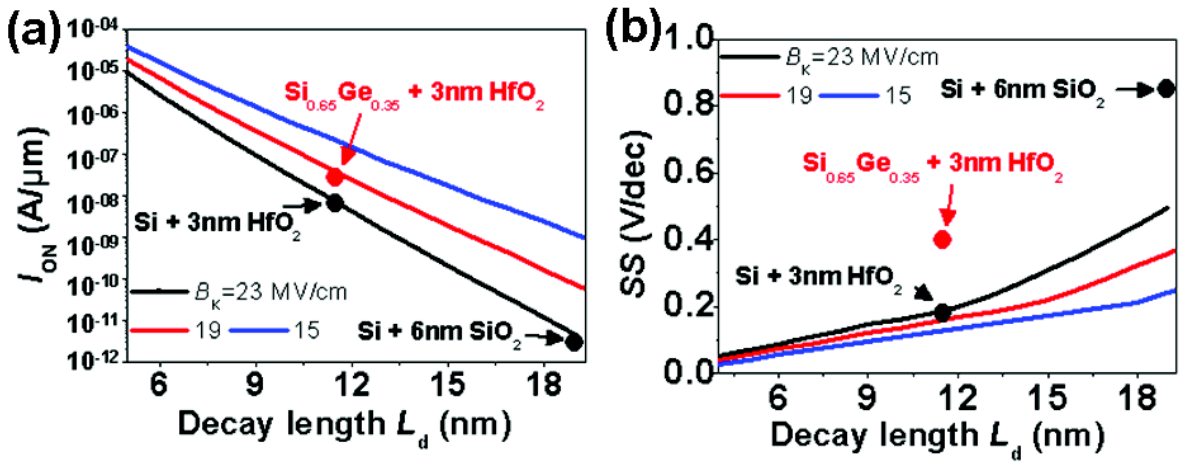

Fig. 3.10: (a) I_{ON} defined at constant $|V_D|$ = 1 V and $|V_G|$ = 3 V; (b) *SS* defined at constant $|I_D| = 2\times10^{-12}$ A/μm for TFETs with different L_d and B_K values. The three dots represent the experimental results showing good match in the prediction of I_{ON}, whereas apparent deviation is observed for the prediction of *SS*.

3.2.4 Discussion

Even though our model quantitatively reproduces experimental results, there are still some problems requiring improvements. For simplicity, the model does not consider the doping depletion and profile in the source region, so that the shortest tunneling distance is assumed to lie along the channel length direction. This slightly overestimates the electric field and thus exaggerates the tunneling current. A simple introduction of an uniform depletion region along channel length direction is possible but results in a slightly more complicated expression.[20] However, in reality, the depletion in source region is much wider near the gate oxide than deep in the channel due to the vertical electric field from the gate, effectively tilting the tunneling direction. Since the technology of fabricating TFETs is moving towards higher source doping and sharper tunnel junctions, this drawback of our model is expected to become less significant.

Another issue of the model is that the predicted tunneling current is not zero at $V_D = 0$, as shown in Fig. 3.7(d) and 3.8(b). This unreasonable result is due to that, like all the other models using local Kane's equation similar to Eq. (3.11) [5, 44, 50-51], the model does not properly account for the final energy states available to the tunneling electrons. Instead, it uses the electric field in the junction, which is non-zero even at $V_D = 0$ due to the built-in junction potential. Under low $|V_D|$, a more reasonable form of the model is [8, 59]:

$$I_D = A_K' \cdot V_C \cdot E_{TW} \cdot exp(-\frac{B_K}{E_{TW}}) \tag{3-16}$$

where the V_C is the voltage drop at the tunneling junction determining the range of the energy available for band-to-band tunneling. The comparison between the model using Eq. (3.16) and the I_D-V_D experimental results shows good agreement in low $|V_D|$ region but large overestimation in high $|V_D|$ region see Fig. 3.11(a), contrary to Fig. 3.7(d).

This is due to that Eq. (3.16) is only valid for tunneling junction with uniform electric field, so that the tunneling rate is constant at various energy states from 0 to qV_C. However, the electric field in TFET is non-uniform and decreases sharply close to the channel, schematically shown in Fig. 3.11(b). The use of Eq. (3.16) markedly overestimates the available tunneling states for the shortest tunneling width.

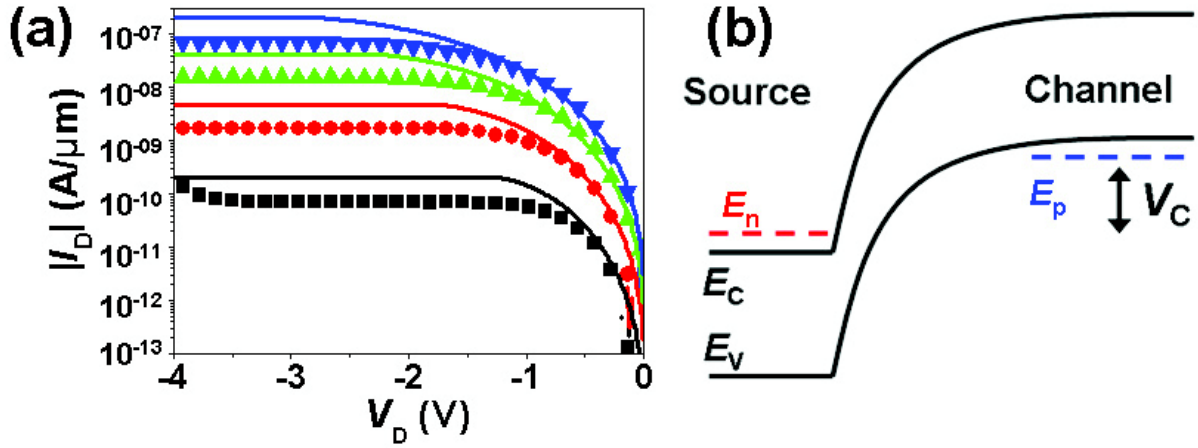

Fig. 3.11: (a) Quantitative comparison between the model (plain lines) using Eq. (3.16) and experimental results (symbols) of the I_D-V_D curves of the TFETs with 20nm Si channel and 3 nm HfO_2 gate oxide, same as in Fig. 3.7(d). (b) Schematic view of the band-diagram in source tunneling junction.

In order to obtain more accurate model, the change of tunneling rate in different energy states need to be considered. This can be achieved by integrating the tunneling rate from the electron Fermi level (E_n) in source junction to the hole Fermi level (E_p) in channel, as indicated in Fig. 3.10(b):

$$I_D = A_K'' \cdot \int_{E_n}^{E_p} E_{TW}(E) \cdot exp[-\frac{B_K}{E_{TW}(E)}]\, dE \tag{3-17}$$

Here the electric field E_{TW} is determined by Eq. (3-11), which decreases as the potential increases from φ_S in the source to φ_C in the channel. Equation (3-17) must be evaluated

numerically, but once this is done, Fig. 3.12 shows the good agreement between Eq. (3-17) and the experimental results for TFETs based on both Si and $Si_{0.35}Ge_{0.65}$ substrates. The current at both low and high $|V_D|$ region are accurately reproduced.

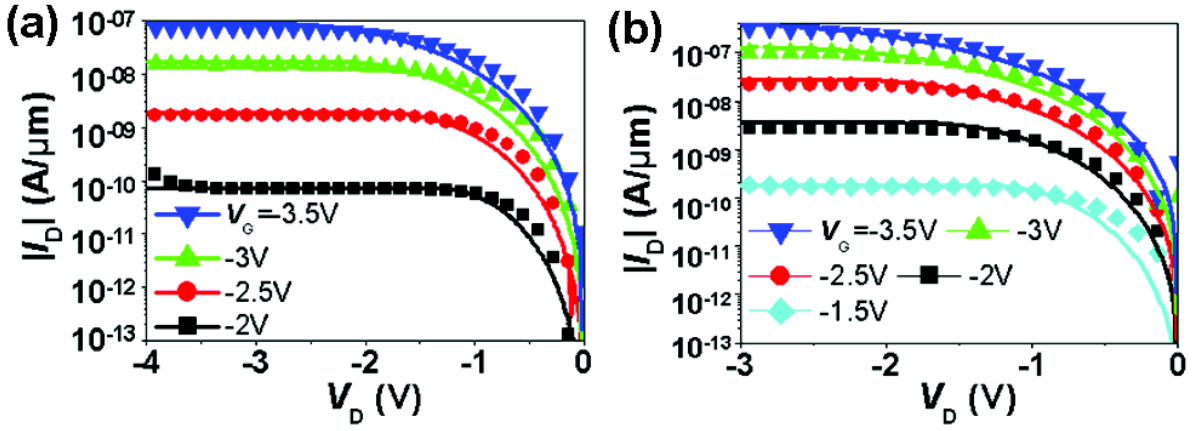

Fig. 3.12: Quantitative comparison between the model (plain lines) using Eq. (3.17) and experimental results (symbols) of the I_D-V_D curves of the TFETs with (a) 20 nm Si channel, same as in Fig. 3.7(d), and (b) 20 nm $Si_{0.35}Ge_{0.65}$ channel, same as Fig. 3.8(b).

3.3 Modeling of the GIDL in TFET and MOSFET built on FD-SOI

As the conventional MOSFET is scaled down, the GIDL current is becoming a critical issue. The competing TFET device, also faces the problem of relatively high leakage current due to the parasitic tunneling [18, 20].

In bulk MOSFETs, several models for GIDL based on both lateral and vertical BTBT have been proposed by combining the Kane's interband tunneling model with a calculated potential distribution [60-63]. However, there are few studies of GIDL in MOSFETs built in FD-SOI technology [64-65]. Moreover, the analysis and modeling of GIDL in TFETs is urgently required because in TFETs GIDL is often quite significant compared to the I_{ON}.

In this section, a model considering lateral BTBT at the drain junction is developed for the GIDL in TFETs and then extended to FD-SOI MOSFETs [66]. In the FD-SOI MOSFET model, the GTD at the drain is combined with the field effect diode (FED) at the source. Even with the same tunneling junction, the GIDL in long-channel MOSFETs is lower than that in TFETs due to the series-connected FED, especially under low V_D. The restriction by the FED component is less important in devices with thinner gate oxide. Moreover, the GIDL in FD-SOI MOSFET shows higher temperature sensitivity than that in TFETs due to the presence of the FED.

3.3.1 Device comparison

Figure 3.13 compares the GIDL current flow in TFETs and MOSFETs built in the same FD-SOI process. In the TFET, the GIDL current generated by BTBT at the drain junction flows through the channel and into the source. Since the voltage drop in the channel is negligible as long as the BTBT current is low, the TFET can be treated as a single GTD at the drain junction.

In the FD-SOI MOSFET, by contrast, the accumulated channel forms a diode with the source. The BTBT-generated current must turn on this FED, inducing a voltage drop at the channel (V_C). This can reduce the voltage difference between the drain and channel, reducing the lateral BTBT rate at the drain junction accordingly.

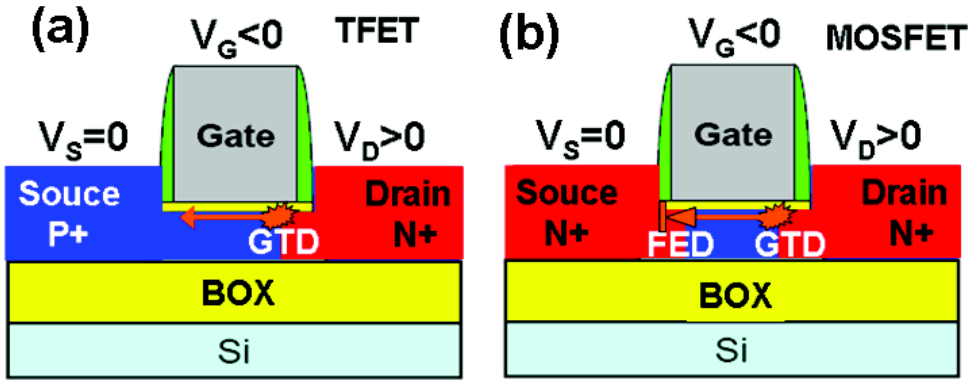

Fig. 3.13. Comparison of the flow of GIDL current between FD-SOI TFET (a) and MOSFET (b) from the same wafer (T_{Si} = 20 nm, L_G = 350 nm, 6 nm SiO_2 gate oxide).

We observe this effect experimentally by comparing the GIDL data in MOSFETs and TFETs fabricated in the same FD-SOI process. Figure. 3.14(a) shows the full I_D-V_G curves of a *n*-type MOSFET, with GIDL current apparent in the $V_G < 0$ regime; whereas Fig. 3.14(b) compares the GIDL currents in the NMOSFET and TFET. Both devices have 6 nm SiO_2 gate oxide, gate length L_G = 350 nm, silicon body T_{Si} = 20 nm, a BOX thickness of 145 nm, and identical drain implantation parameters. Even with the same GTD component at the drain junction, the GIDL of the TFET is consistently larger than that of the MOSFET, especially at low V_D and high V_G. Thus, the modeling of GIDL in the FD-MOSFET should consider both the effects of GTD and FED.

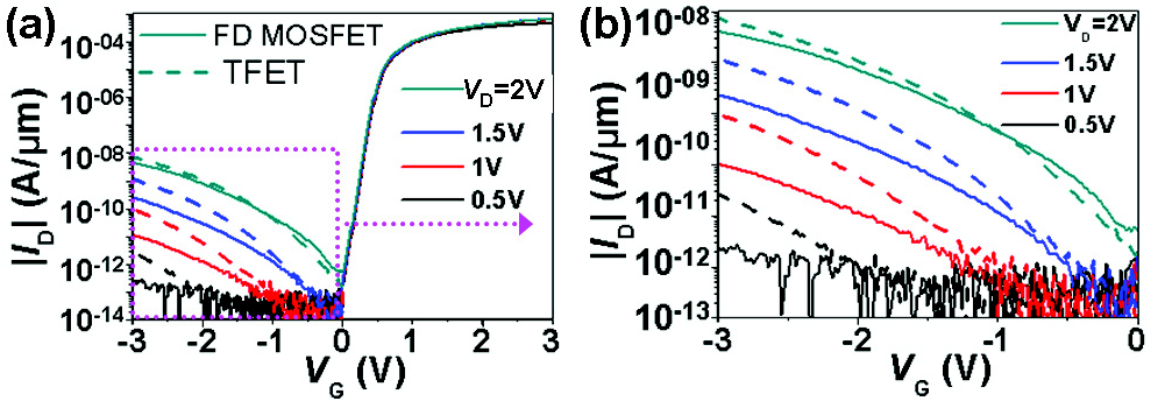

Fig. 3.14. (a) I_D-V_G curves of a *n*-type FD-SOI MOSFET under various V_D. (b) Comparison between the SOI TFET current (dashed lines) and the GIDL in MOSFET (solid lines). The devices are fabricated by the same FD-SOI process, and gate length L_G = 350 nm with 6 nm SiO_2 gate oxide.

3.3.2 Model derivation

Using the pseudo-2D method, similar to the TFET I_D modeling in the preceding section, following analytical expression of the tunneling current in GTD is obtained:

$$I_{GTD} = A_K \cdot E_{TW}^{\ 2} \cdot exp(-\frac{B_K}{E_{TW}})$$
$$with\ E_{TW} = \frac{E_G}{q} \frac{1}{L_d \cdot ln[\frac{(\varphi_D - \varphi_G) + \sqrt{(\varphi_D - \varphi_G)^2 - (\varphi_C - \varphi_G)^2}}{(\varphi_D - \varphi_G - \frac{E_G}{q}) + \sqrt{(\varphi_D - \varphi_G - \frac{E_G}{q})^2 - (\varphi_C - \varphi_G)^2}}]} \quad (3\text{-}18)$$

where the A_K and B_K are the tunneling parameters, E_G is the bandgap of the channel material, and $\varphi_G = V_G - V_{FB}$, $\varphi_D = V_D + V_{biD}$, and $\varphi_C = V_C + V_{biC}$ are the gate, drain and channel electrostatic potentials respectively (referenced to the midgap Fermi level E_i in the nominally undoped channel). The channel V_{biC} is determined by gate voltage and can be derived from a simple charge sheet approximation [67].

In FD-SOI MOSFETs, the modeling of GIDL needs to combine both the GTD and FED. In the first approximation, the FED can be modeled as an ideal diode with the hole current at source side determined by [3]:

$$I_{FED} = qT_{si}(D_p n_p / L_E)[\exp(qV_C/kT) - 1] \quad (3\text{-}19)$$

where D_p is the diffusion coefficient of holes in source, L_E is the effective hole diffusion length at the source which is limited by the location of source electrode, and kT/q is the thermal voltage. The source-drain electrons diffusion component can be neglected due to the long channel. The channel voltage V_C and current are thus obtained by combining 3.18 and 3.19 according to the current continuity ($I_{GTD} = I_{FED}$).

3.3.3 Model verification

The validity of the model is examined by comparing with the experimental results. The tunneling parameters (A_K and B_K) in Eq. (1) are extracted from the I_D–V_G curve of the TFET at V_D = 1.5 V through the linear relation of $ln(I_D/E_{TW}^2) \sim 1/E_{TW}$. As before, the extracted B_K value is 23 MV/cm, which agrees with reported results on phonon-assisted BTBT in silicon [51, 53]. Using these values as fitting parameters, we calculated the TFET GIDL current according to Eq. (3.18) and compared with the experimental results – see Fig. 3.15(a). The model agrees with experiment over a wide range of V_D and V_G.

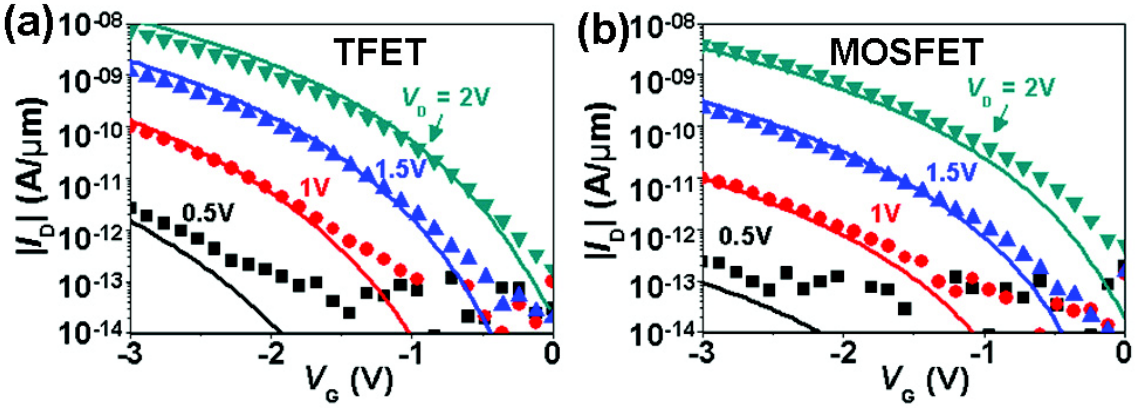

Fig. 3.15. (a) Fit between the model describing the GTD (lines) and the experimental TFET data (points). (b) Comparison between the proposed model (lines) combining GTD with FED mechanism and the experimental data (points) from the GIDL in FD-SOI MOSFET.

Using the tunneling parameters extracted from the TFET, the GIDL of an FD-SOI MOSFET is calculated by combining Eqs. (3-18) and (3-19) and solving them numerically. Figure 3.15(b) compares the model (curves) with the experimental data (points), showing good agreement. The reduction of GIDL in a MOSFET compared to a TFET at low V_D bias can be straightforwardly explained by the graphical method illustrated in Fig. 3.16. The curves in Fig. 3.16 correspond to the GTD I_D–V_C curves as a function of V_D with fixed V_G = –3 V, the straight line corresponds to the I_D–V_C relation of the FED from Eq. (3-19), and the actual V_C and I_D values of the FD-SOI MOSFET are given by the intersection points, circled in Fig. 3.16. The GIDL current in the FD-SOI MOSFET is markedly reduced compared to its GTD component with V_C=0V due to current continuity through the FED. The reduction occurs even at low V_D, because when V_D is low the I_{GTD} falls more rapidly with the increase in V_C.

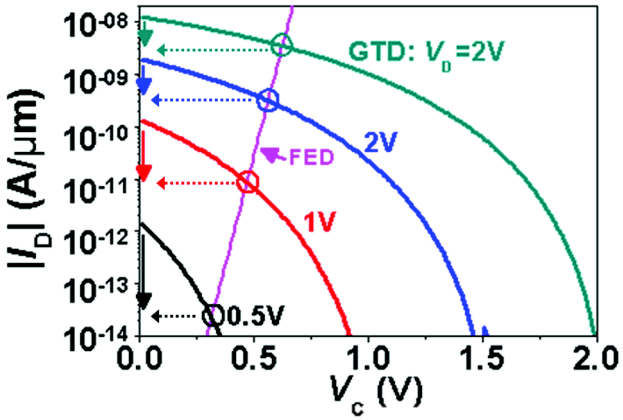

Fig. 3.16. I_D-V_C curves from GTD component of FD-SOI MOSFET as a function of V_D. Combining with the FED component, the current I_D in FD-SOI MOSFET is obtained at the crossing point. At lower V_D, the I_D decreases more rapidly as V_C increases and thus becomes much smaller than in a SOI TFET with the same fabrication parameters.

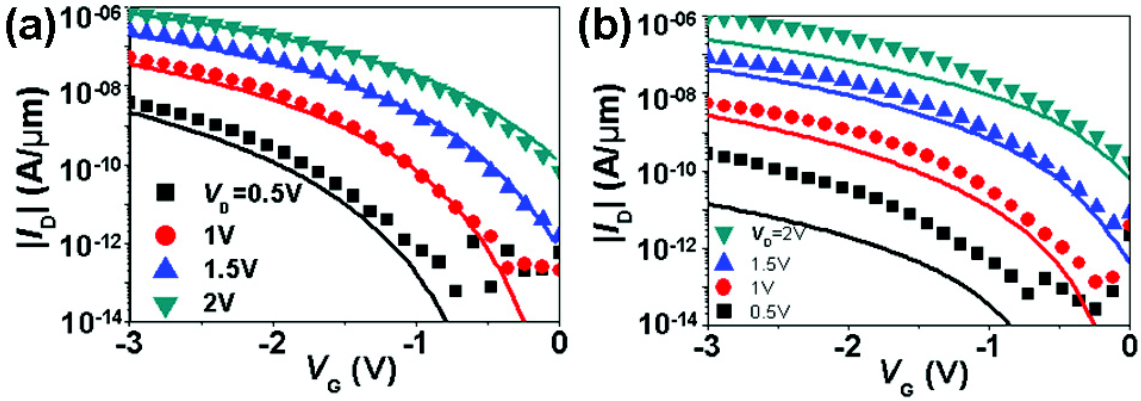

Fig. 3.17. Fit between model (lines) and the experimental results (points) from (a) SOI TFET and (b) SOI MOSFET with 3 nm HfO_2 gate oxide.

The model is also used for analyzing devices fabricated with 3 nm HfO_2 gate oxide. Compared to the 6 nm SiO_2 devices, the GIDL current in MOSFETs is again lower than in TFETs, but the reduction is less pronounced. At V_D = 2 V, the GIDL current of the MOSFET is almost the same as the TFET, indicating that the FED has less effect in devices with thinner gate oxide. The fits of our model with the experimental results of the HfO_2 devices are shown in Fig. 3.17. The MOSFET GIDL current at V_D = 0.5 V is somewhat underestimated by the model. This may be due to the fact that the FED current at low I_D is dominated by the recombination component, ignored in Eq. (3-19), which decreases more slowly with V_C. This hypothesis is consistent with the experimental results, since the HfO_2 gate oxide introduces more traps than SiO_2 gate oxide, enhancing recombination.

3.3.4 Discussion

The effect of the FED component in FD-SOI MOSFETs can also impact the temperature dependence of the GIDL current. Figure 3.18 compares this temperature dependence in TFETs and MOSFETs based on the same FD-SOI substrate with 3 nm HfO_2 gate oxide. At room temperature, the MOSFET and TFET GIDL currents are similar, indicating negligible effect from the FED. As T decreases, the TFET current decreases slowly due to the weak temperature dependence of BTBT [12]. On the other hand, the MOSFET GIDL current decreases more rapidly, especially at lower temperature, as shown by the points in Fig. 3.18. This sensitivity to temperature arises from the stronger temperature dependence of the FED component, which effectively restricts the current flow at low T. A more quantitative analysis of the impact of FED will require an additional examination of both the vertical BTBT tunneling, which is more complicated because it is not explicitly determined by the channel potential, and of the trap-assisted tunneling which is another main source of GIDL [10].

Further enhancement of GIDL current is observed in MOSFETs with small L_G because of the parasitic bipolar amplification effect. This will be discussed later, in Chapter 6.

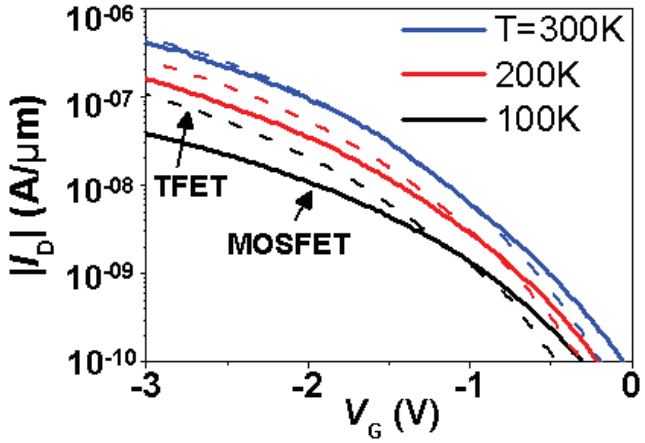

Fig. 3.18. GIDL current of SOI TFET (dashed lines) and SOI MOSFET (solid lines) with 3 nm HfO_2 gate oxide *vs.* temperature. The GIDL of TFET is less sensitive to temperature compared to that of FD MOSFET.

3.4 Conclusions

In this chapter, a new TFET model was developed considering both the tunneling junction and the channel transport. With a low tunneling rate as in most experimental devices, this model reduces to a simple analytical form by solving the pseudo-2D Poisson equation in

the tunneling junction. Instead of the maximum electric field, the mean electric field along the shortest tunneling width is used in the local Kane's model to achieve better accuracy.

The developed model was validated by comparing to the simulation and experimental results. The surface potential obtained from the simulated TFETs with various T_{si} and T_{ox} under different V_D and V_G biases are well traced by the model. The comparisons of the I_D-V_G and I_D-V_D curves between the experiments and model show good agreement over large V_D and V_G range in devices with different gate oxides and channel materials.

The model was further extended to double-gate and gate-all-around structures by appropriately redefining the potential decay length. Based on the model, the ON current can be projected for TFETs with various architectures, gate lengths, and channel materials.

The TFET model is further adapted to explain the GIDL current in FD-SOI MOSFET, where the current is modeled by combing the tunneling junction and the forward bias diode in drain and source, respectively. With the presence of the source diode, the GIDL current in FD-SOI MOSFET is lower than that in TFET, especially at low V_D, which has been well traced by the model. Further studies on the MOSFET with short L_G show enhanced GIDL current and large variation, to be discussed in Chapter 6.

Chapter 4: Z^2-FET: DC performance

Abstract –This chapter presents a systematic study on a new sharp-switching device built in fully-depleted silicon-on-insulator (FD-SOI) that we have called Z^2-FET, as it features *zero* subthreshold swing (< 1 mV/decade of current) and *zero* impact ionization. The Z^2-FET is a compact device, analogous in layout to an asymmetric TFET with a partial ungated channel region, that experimentally features current I_{ON}/I_{OFF} ratio > 10^9 at low supply voltage, as well as gate-controlled hysteresis. The operating principle of the sharp switching involves the positive feedback between carrier flow and gate-controlled injection barriers, as confirmed by TCAD simulations.

The device operates with either back gate bias V_{BG} or surface charge Q_S on the ungated section of the channel. The scaling capability has been studied in detail through experiment and simulation. The results reveal that the Z^2-FET operating with back gate bias is scalable down to 30 nm with the help of advanced SOI substrate with ultrathin channel and buried oxide layers and even further, down to 20 nm, in a device with non-overlapping front and back gates. A simplified compact model of the Z^2-FET is also developed, which is in good agreement with experimental results.

4.1 Introduction

Compact CMOS-compatible devices with sharp switching are of great interest for logic applications, and low voltage circuitry. If they feature voltage-controlled hysteresis they are also promising for memory and electrostatic discharge (ESD) protection. Thyristors using the bipolar feedback triggered by impact ionization have been widely studied and used in power switch electronics [68-69]. Recently, the thin capacitively coupled thyristor (TCCT) built on an SOI substrate has been used as a one-transistor (1T) memory showing compactness and high access speed [11, 28], but it requires accurate doping control in the channel for stable performance [29]. The field effect diode (FED) and feedback field effect transistor (FB-FET) have also been demonstrated for ESD protection, memory and switch applications by using the feedback controlled by two front gates and surface charges, respectively [7, 30-32]. Very recently, a fin-FET device with two adjacent gates has been simulated for use as a 1T-DRAM [70].

In this chapter, we introduce an innovative device: the Z^2-FET, a compact device built on an FD-SOI substrate with undoped channel, a single front gate, and a backgate, which exhibits ultra-sharp switching (zero subthreshold swing) and gate-controlled hysteresis [71] at biasing voltages below 2 V. After summarizing the operating principle, based on the positive feedback between electron and hole channel currents and their respective injection barriers [71], we present a systematic study of the Z^2-FET, including the impact of various structural parameters on the device performance, the effects of temperature and our preliminary measurements of device reliability. We also project the scaling capabilities of the Z^2-FET in advanced FD-SOI by TCAD simulation. A simplified model is also developed to reproduce the experimental results.

4.2. Static (DC) characteristics of Z^2-FET

We will first illustrate the device structure of both the *n* and *p*-type Z^2-FETs operating with back gate bias. Their I_D-V_D and I_D-V_G characteristics show gate-controlled hysteresis and extremely sharp switching, outperforming other sharp switching devices. We describe the positive-feedback-based operation principle as revealed by TCAD simulation. Another variant of the Z^2-FETs operating with surface charge is presented showing similar hysteresis and sharp switching. Preliminary reliability tests are performed under various temperatures and long time biasing stress.

4.2.1 Device structure and performance

The Z^2-FET is a forward biased *p-i-n* diode with the intrinsic channel partially covered by the front gate (L_G) and the rest ungated (L_{IN}), schematically shown in Fig. 4.1(a). The device has the same layout structure and fabrication process as the asymmetrical TFET, presented in section 2.2 [33]. For the *p*-type Z^2-FET, the p^+ source is grounded and the n^+ drain is negatively biased ($V_S = 0$, $V_D < 0$). The negatively and positively biased front and back gates ($V_G < 0$, $V_{BG} > 0$) are used to form electron and hole injection barriers in L_G and L_{IN} regions, respectively. This biasing scheme emulates a virtual *p*/*n*/*p*/*n* thyristor even though the body is undoped. Experimental I_D–V_D measurements show that the device is initially in OFF state at low $|V_D|$ and turned on sharply as $|V_D|$ increases to turn-on voltage $|V_{ON}|$. As $|V_D|$ sweeps back to 0, the device stays in the ON state until $|V_D|$ decreases below 0.8 V, at which point it turns off. Since the V_{ON} is linearly dependent on V_G, large hysteresis is obtained, see Fig. 4.1(b).

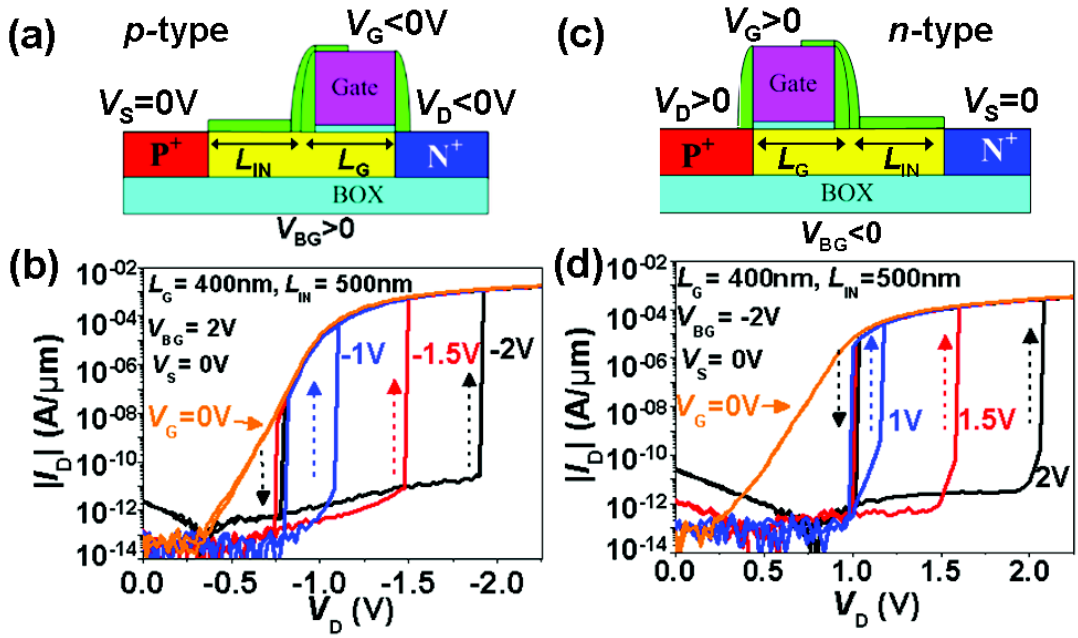

Fig. 4.1: Schematic structure of the (a) *p*-type and (c) *n*-type Z^2-FETs operating with backgate voltage $V_{BG} > 0$ and $V_{BG} < 0$, respectively. Experimental I_D-V_D curves on (b) *p*-type and (d) *n*-type Z^2-FETs show sharp switching and gate-controlled hysteresis. The device parameters are $T_{ox} = 3$ nm HfO_2, $T_{si} = 20$ nm, $T_{BOX} = 145$ nm, $L_G = 400$ nm and $L_{IN} = 500$ nm.

Compared to the *p*-type device shown in Fig. 4.1(a), in *n*-type Z^2-FET the gate is adjacent to the p^+ doped drain and positively biased, whereas the back gate is negatively biased, as shown in Fig. 4.1(c). The I_D–V_D curves show similar sharp switching and V_G-controlled hysteresis as the *p*-type device, see Fig. 4.1(d).

The transfer characteristic (I_D-V_G) also shows sharp switching, where the current increases by 8 decades within a narrow ΔV_G = 1mV range at V_D = –1.5 V, see Fig. 4.2(a). The switching threshold can be tuned by biasing the V_D with grounded V_S (solid curves) or V_S with grounded V_D (dashed curves). Compared to other sharp-switching devices, such as the FB-FET [7], tunneling FET (TFET) [18] and impact ionization MOS (IMOS) [72], the Z^2-FET shows superior switching performance under reasonably low V_{DD} = 1.5 V supply voltage, see Fig. 4.2(b).

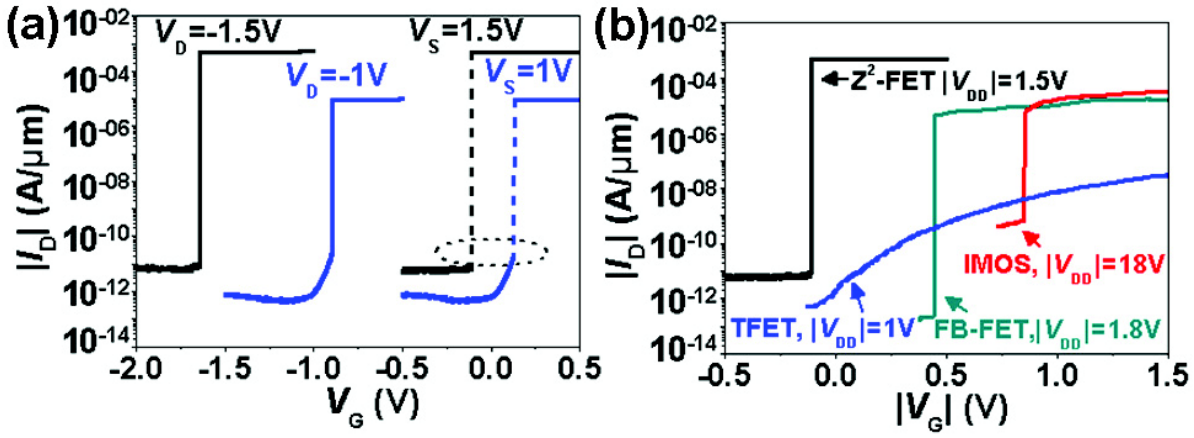

Fig. 4.2: (a) Experimental I_D-V_G curves of the *p*-type Z^2-FET show sharp switching with subthreshold swing below 1mV/decade. The I_{ON} exceeds 500 μA/μm at V_D = –1.5 V. The threshold voltage is determined by the relative biasing of drain and source. (b) Comparison between Z^2-FET and other reported sharp-switching devices including the FB-FET [7], TFET [18] and IMOS [72].

4.2.2 Operation principle

The Z^2-FET device operation can be understood via TCAD simulations [5]. Figure 4.3 shows the simulated I_D-V_D curves under different V_G reproducing the *p*-type Z^2-FET experimental results if Fig. 4.1(a). Including impact ionization has no effect, as shown by the dots in the V_G = –2 V curve, indicating that the operation of Z^2-FET does not involve impact ionization, and thus differs from a thyristor.

Figure 4.4 shows the band diagrams in the channel of the Z^2-FET under various V_D with V_G = –2 V and V_{BG} = 2 V. Electron and hole barriers (V_n and V_p) are formed by V_G and V_{BG} respectively, blocking the carrier flow at low V_D. As $|V_D|$ increases, the channel potential under the front gate is clamped due to the forward-biased channel-drain junction. The holes accumulated under the gate are depleted as $|V_D|$ increases close to $|V_G|$, reducing the electron injection barrier. This enables the injection of electrons from the n^+ drain into the channel,

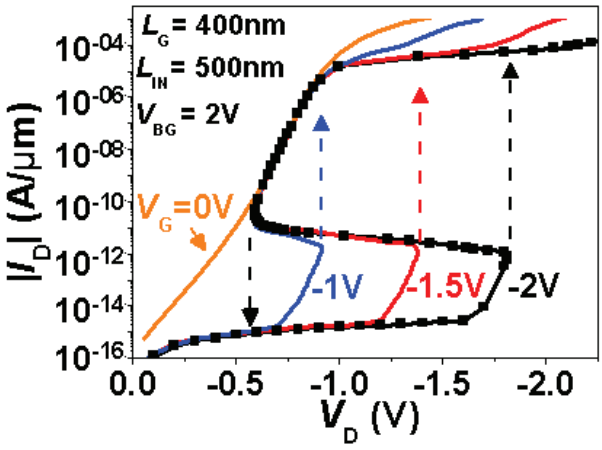

Fig. 4.3: Simulated I_D-V_D curves reproducing the experimental results in Fig. 1(b).

which flow to the p^+ source and induce a potential drop at source-channel junction, thereby reducing the injection barrier for holes and initiating positive feedback. Strong positive feedback turns on the device sharply, see the V_D = –2 V band diagram in Fig. 4.4. Both injection barriers have been suppressed by the electron and hole current. A high I_D is measured once the device switches to the ON state.

Figure 4.4(b) shows in more detail the evolution of V_n and V_p as $|V_D|$ increases towards $|V_{ON}|$. At low $|V_D|$, the channel under the gate is strongly accumulated with holes due to V_G = –2 V, forming a high V_n barrier and thus blocking the electron injection. As V_D becomes more negative, the channel potential (φ_C) is set by forward-biased channel–drain junction. When V_D decreases below the clamping voltage (V_{clamp}), holes in L_G region are depleted, and thus φ_C is pinned by the gate voltage V_G. Any further decrease of V_D reduces the V_n linearly, since V_n is determined by the potential difference between the channel and drain. Accordingly, the electrons are injected into the channel and flow to the source, initiating the positive feedback, which accelerates the reduction of barriers and increase of current, shown schematically in the close-up of Fig. 4.4(c). The feedback is strong enough to sharply turn on the device at V_D = V_{ON}.

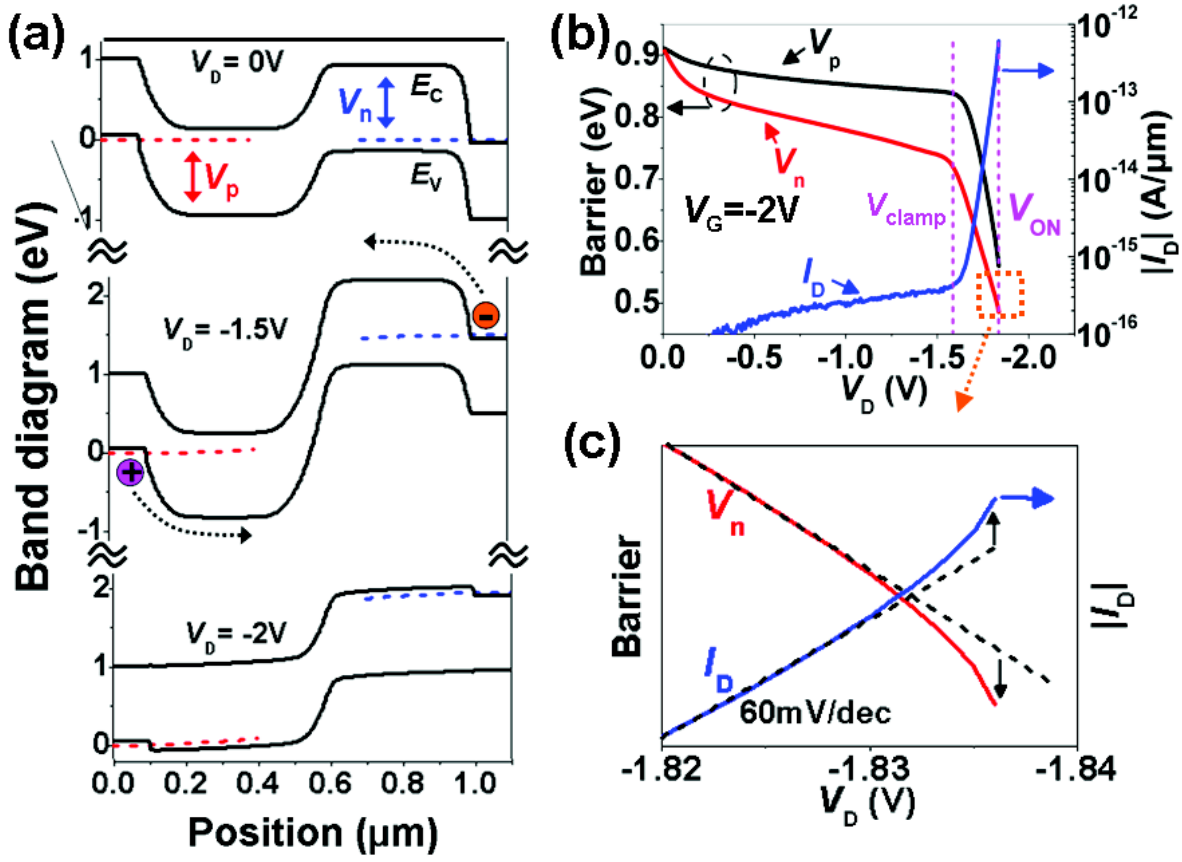

Fig. 4.4: (a) Self-consistent simulated band diagrams vs. V_D at V_G = –2 V and V_{BG} = 2 V, showing how the electron and hole injection barriers (V_n and V_p) are eliminated at V_D = –2 V. (b) Evolution of V_n, V_p and I_D as V_D decreases from 0 to V_{ON}. (c) Close-up of the V_{ON} region showing schematically how the feedback reduces the barrier and increases the current.

4.2.3 Alternative Z^2-FET variant operating with surface charge (Q_S)

The Z^2-FET can also operate with surface charge (Q_S) instead of V_{BG}, as shown in Fig. 5(a). In this mode, one of the barriers is established by Q_S as in the FB-FET [7, 30], whereas the other injection barrier is still controlled by the front gate ensuring good controllability of the switch point V_{ON}. The positive surface charge in the *p*-type device of Fig. 5 is promoted by the chemical vapor deposited SiO_2 on the L_{IN} region, with $Q_S \sim 10^{12}$ cm^{-2}.

Figure 4.5(b) and (c) show the sharp switch and hysteresis, similar to the V_{BG}-operated device in Fig. 4.1 and 4.2, with even higher I_{ON}/ I_{ON} ratio ~ 10^{10}. With modified V_D and V_S bias, the threshold voltage is also tunable, see Fig. 4.5(d).

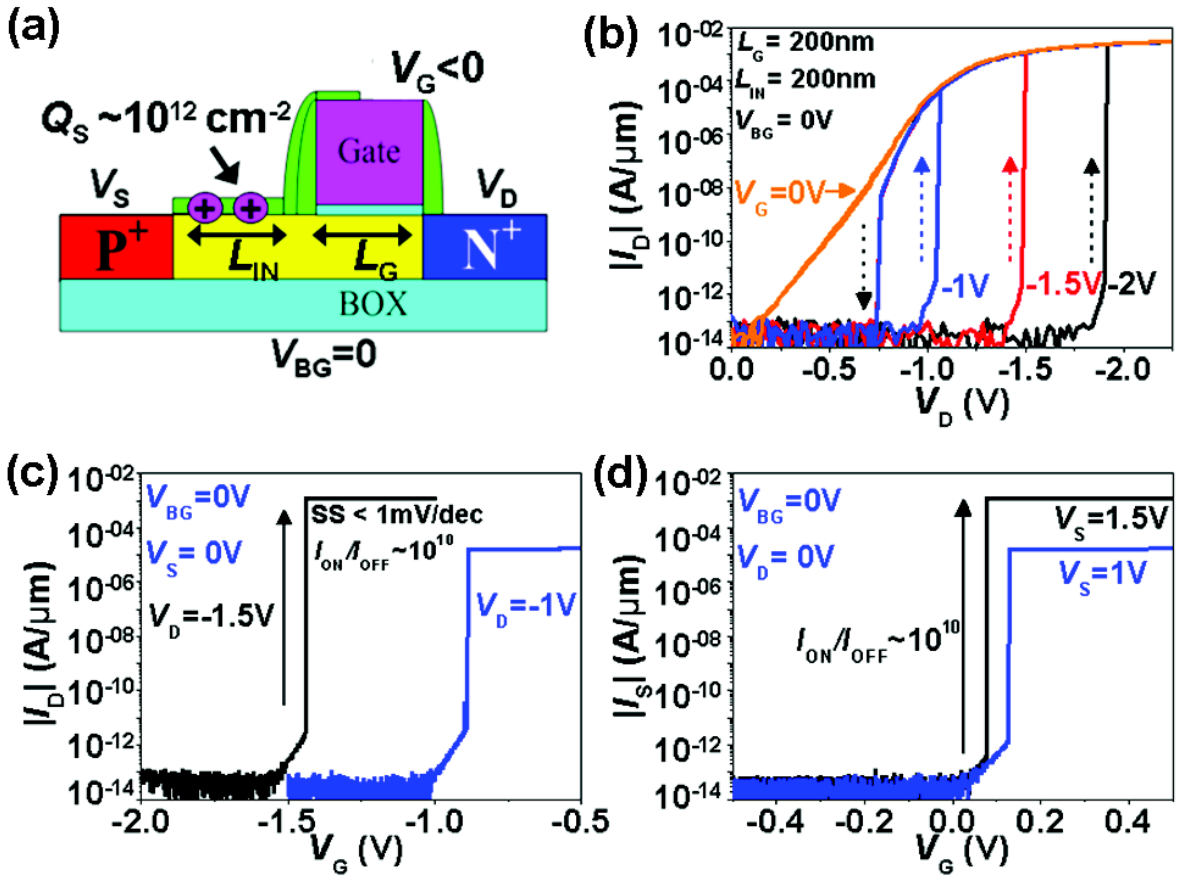

Fig. 4.5: (a) Schematic structure of the *p*-type Z^2-FET operating with surface charge density Q_S instead of V_{BG}. (b) and (c) show the I_D-V_D and I_D-V_G curves respectively, featured by sharp switching and V_G-controlled hysteresis. (d) I_S-V_G measurements showing modified threshold voltage compared to Fig. (c). The device parameters are T_{ox} = 6 nm SiO_2, T_{si} = 20 nm, T_{BOX} = 145 nm, L_G = 200 nm and L_{IN} = 200 nm.

4.2.4 Reliability

The Q_S-operated Z^2-FET has been measured under temperatures ramping from 25 ℃ to 105 ℃, see Fig. 4.6(a). The hysteresis window is hardly changed and the $|V_{ON}|$ decreases by only 0.12 V. Compared to the normal thyristor using bipolar action triggered by impact ionization [29], the Z^2-FET is relatively insensitive to temperature variation, thanks to the stable feedback process. We have also carried out preliminary reliability measurements by repeatedly cycling the device through the hysteretic loop. It was found that $|V_{ON}|$ decreases only slightly after 12000 sweeps lasting for over 50 hours, as shown in Fig. 4.6(b), demonstrating good reliability for a prototype device.

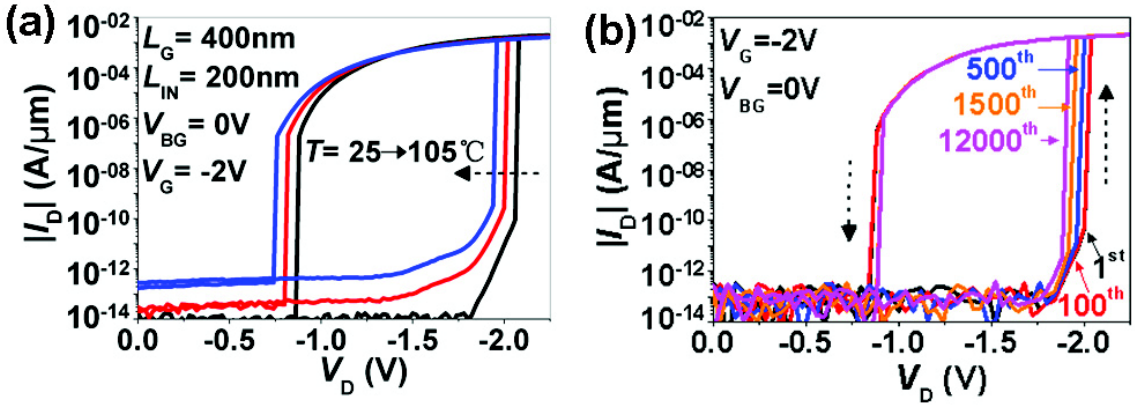

Fig. 4.6: Experimental I_D-V_D measurements on the Q_S-operated Z^2-FET under (a) variable temperature in the 25–105 ^oC range and (b) repeated sweeping through the hysteretic loop (12000 cycles lasting for over 50 hours). The prototype device has parameters of L_G = 400 nm, L_{IN} = 200 nm, T_{ox} = 6 nm SiO_2, T_{si} = 20 nm, T_{BOX} = 145 nm and V_G = –2 V.

4.3. Z^2-FET scaling capability

The scaling of the Z^2-FET is determined by the requirement of maintaining sufficiently high injection barriers induced by V_G and either Q_S or V_{BG}, respectively. In devices with too short a gate or intrinsic region, the turn-on voltage degrades due to the weak controllability by V_G and V_{BG}, similar to the threshold voltage degradation in a short-channel MOSFET.

The scaling capability of the Z^2-FETs operating with Q_S is restricted by the weak controllability of Q_S, confirmed by both experiments and simulations. In contrast, the scalability of the V_{BG}-operated Z^2-FETs built on advanced SOI structure is more aggressive, as demonstrated in simulation with various T_{ox}, T_{si} and T_{BOX}.

4.3.1 Scaling of the Q_S-operated device

Figure 4.7(a) shows the I_D–V_D measurements on Q_S-operated Z^2-FET with L_G scaling from 400 nm down to 100 nm at constant L_{IN} = 200 nm. The $|V_{ON}|$ decreases only slightly, thanks to the strong control of V_G on L_G region. However, the $|V_{ON}|$ drops abruptly as L_{IN} scales down to 100 nm with L_G = 400 nm, see Fig. 4.7(b). This is due to the fact that Q_S has less control in the short L_{IN} region. Figure 4.7(c) and (d) show the corresponding I_S-V_G curves revealing the same tendency, where the threshold voltage degrades as L_G and L_{IN} decrease, whereas the I_{ON} current increases due to lower channel resistance.

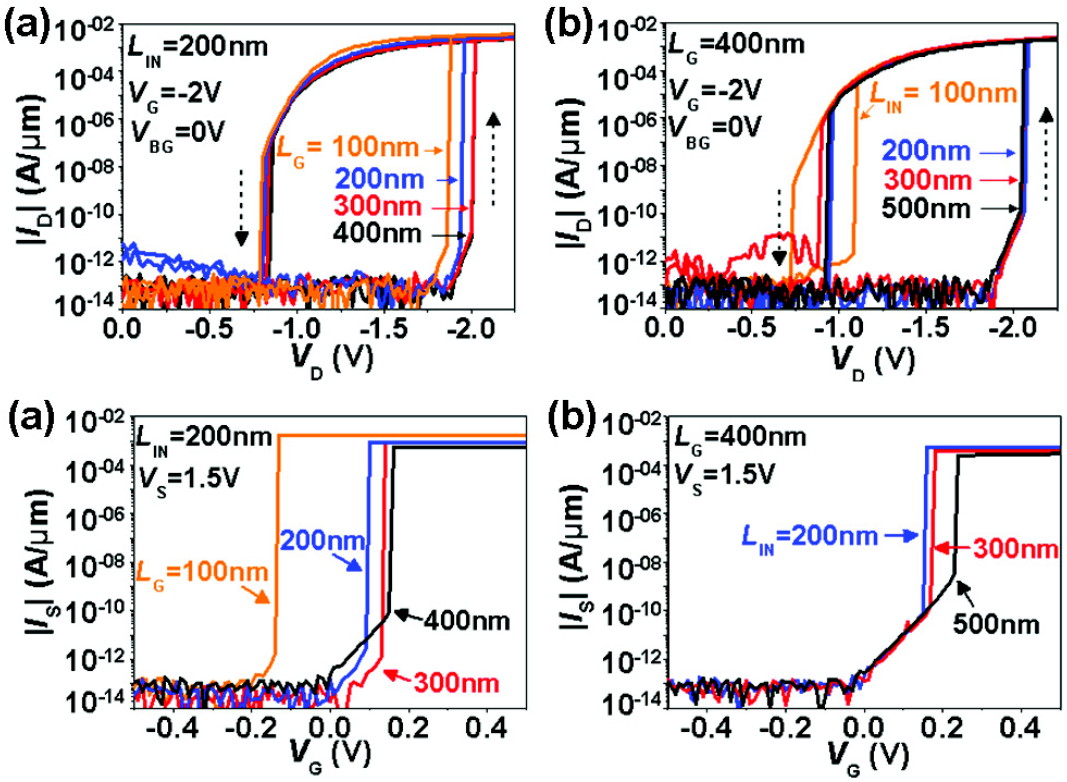

Fig. 4.7: (a) and (b) show experimental I_D-V_D measurements on Q_S-operated Z^2-FET with L_G and L_{IN} scaling down to 100 nm. Figure (c) and (d) show corresponding I_S-V_G measurements.

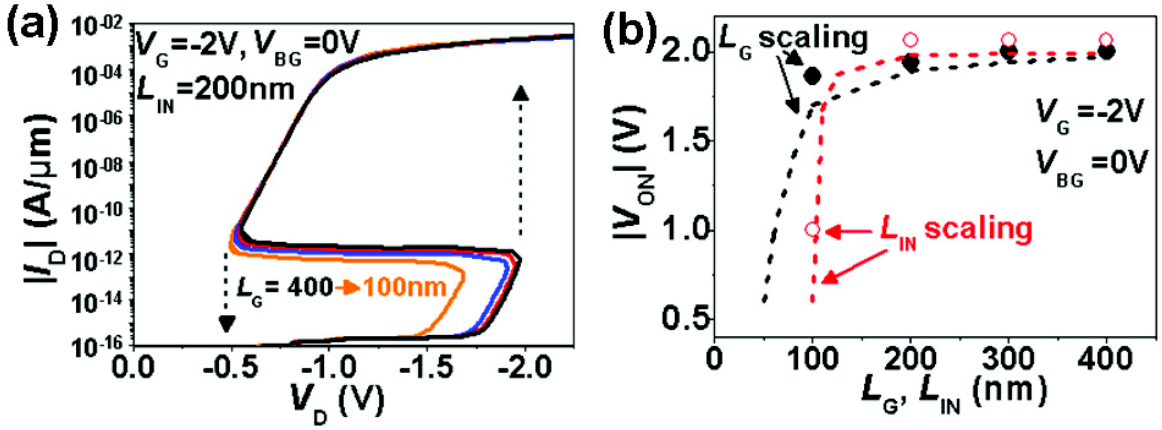

Fig. 4.8: Downscaling capability studied by TCAD simulation. (a) I_D-V_D curves under various L_G, reproducing the experimental results in Fig. 4.6(a). (b) Comparison of the turn-on voltage (V_{ON}) between simulation (curves) and the experiments (dots). For L_G scaling L_{IN} = 200 nm, for L_{IN} scaling L_G = 400 nm, same as the experiments in Fig. 4.6.

Simulations have been performed with Silvaco tools to study the scaling of the Q_S-operated Z^2-FET in the experimentally available range of device parameters. The simulated I_D-V_D curves with L_G scaling from 400 nm to 100 nm reproduce the experimental results well, see Fig. 4.8(a). Further simulations on scalability agree well with the experiments,

see Fig. 4.8(b), where the $|V_{ON}|$ decreases as L_G and L_{IN} decrease.

Encouraged by the agreement of simulation and experiment for available L_G and L_{IN}, we have studied the impact of Q_S density on the device scaling by simulation. Figure 4.9(a) shows the simulated I_D–V_D curves of devices under various Q_S density, where the hysteresis and sharp switch are eliminated at low Q_S density (< 10^{11} cm^{-2}) and saturated at high Q_S density (< 2×10^{11} cm^{-2}). Figure 4.9(b) shows the relation between V_{ON} and the amount of Q_S for Z^2-FET with various L_{IN}. In low Q_S region, V_{ON} is very sensitive to the precise value of Q_S. The sensitivity is higher for devices with longer L_{IN}, a property that may prove interesting for sensor applications. However, at sufficiently high Q_S, V_{ON} saturates and is only controlled by V_G, which see Fig. 4.9(b). This property demonstrates that the Z^2-FET is more controllable than FB-FET, where both of the injection barriers are controlled by surface charge, and thus the device characteristics are always sensitive to the precise value of Q_S [30]. A value of $Q_S \sim 10^{12}$ cm^{-2} is enough for our experimental devices with $L_{IN} \geq 200$ nm. For devices with shorter L_{IN}, higher surface charge density is needed, which is difficult to control precisely. For this reason, downscaling of the Z^2-FET further, below 100 nm, requires using V_{BG} operation.

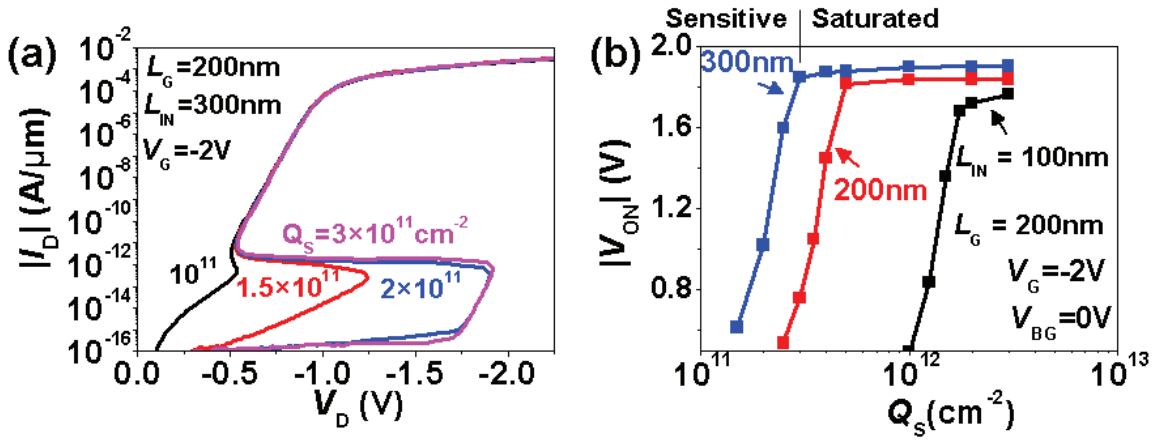

Fig. 4.9: (a) Simulated I_D-V_D curves of the Z^2-FET with various density of surface charge Q_S. (b) The dependence of $|V_{ON}|$ on the Q_S for Z^2-FET with various L_{IN}.

4.3.2 Ultimate scaling of the V_{BG}-operated device

In order to establish the ultimate scaling limit of the Z^2-FET, we performed simulations of the V_{BG}-operated device in a more advanced SOI structure, by studying the impact of T_{ox}, T_{si} and T_{BOX} while keeping the V_G and V_{BG} fixed and setting $L_G = L_{IN} = L$. The effects of varying T_{ox}, T_{si} and T_{BOX} are shown respectively in Fig. 4.10, 4.11 and 4.12. The general trend is that as $L_G = L_{IN} = L$ decreases, the V_{ON} is initially stable and then drops abruptly when V_G and

V_{BG} lose control of the injection barriers in the L_G and L_{IN} regions, respectively.

With thinner T_{ox}, the control of the front gate on the L_G region is stronger and the V_{ON} is less affected by the coupling from the back gate, resulting in better scaling capability and higher saturated $|V_{ON}|$, as shown in Fig. 4.10(a) where T_{ox} = 1 nm and 3 nm are compared. Figure 4.10(b) compares the simulated I_D-V_D curves of the devices with $L_G = L_{IN} = 50$ nm and two different T_{ox}, showing that the $|V_{ON}|$ increases as T_{ox} decreases from 3 nm to 1 nm. The OFF voltage $|V_{OFF}|$, where the device is turned off, also increases slightly due to the higher electron injection barrier resulting from the stronger induction of V_G on L_G region.

Similar behavior is observed for the scaling of T_{si}, see Fig. 4.11(a) where the device with T_{si} = 5 nm has better scalability and higher saturated $|V_{ON}|$ than that with T_{si} = 7 nm. Whereas, The $|V_{OFF}|$ and the lowest current for holding the ON state increase for device with T_{si} = 5 nm, see Fig. 4.11(b). This is due to that the injection barrier is enhanced in ultra-thin channel, and thus reduces the feedback gain.

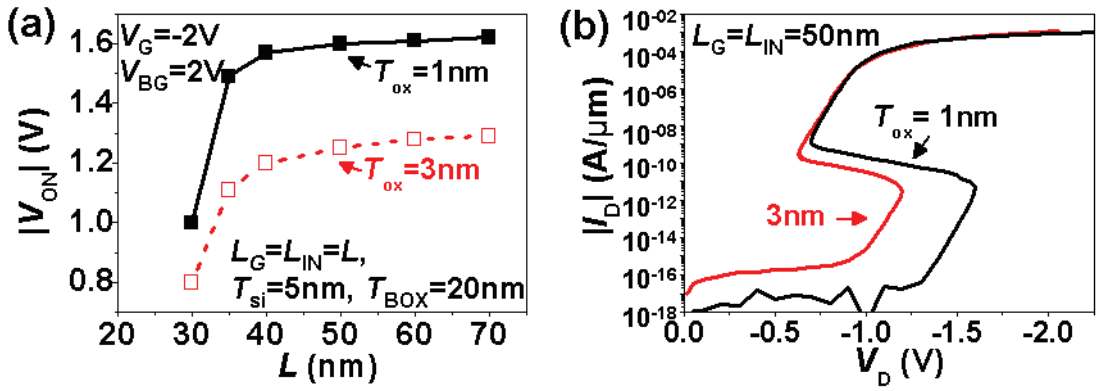

Fig. 4.10: (a) Simulated scaling capability of Z^2-FETs with various T_{ox} and (b) corresponding I_D-V_D curves.

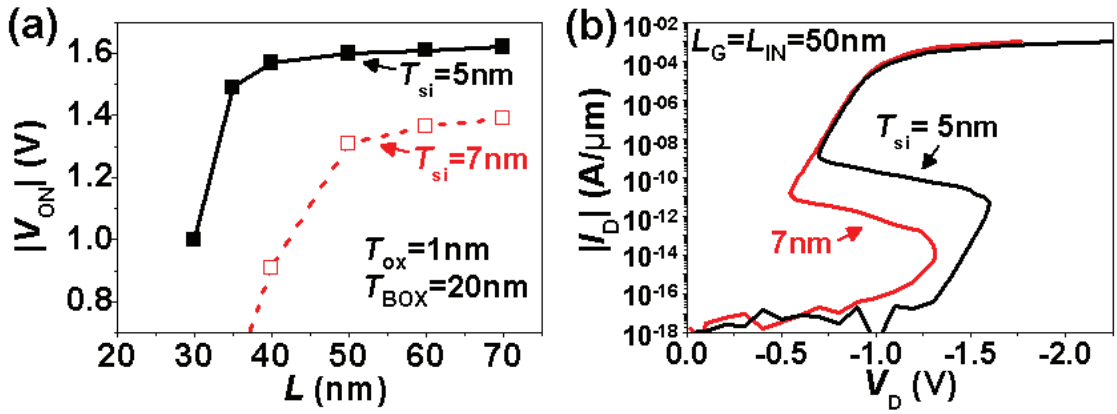

Fig. 4.11: (a) Simulated scaling capability of Z^2-FETs with various T_{si} and (b) its corresponding I_D-V_D curves at L_G=L_{IN}=50nm.

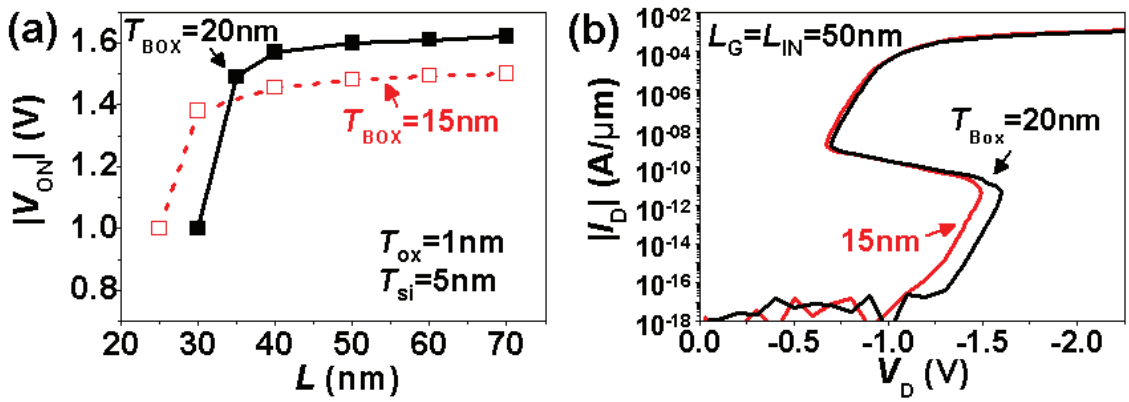

Fig. 4.12: (a) Simulated scaling capability of Z^2-FETs with various T_{BOX} and (b) its corresponding I_D-V_D curves.

Thinner BOX also results in better scalability thanks to the stronger control of V_{BG} on L_{IN} region, see the curve with T_{BOX} = 15 nm as opposed to 20 nm in Fig. 4.12(a). However, the saturated $|V_{ON}|$ is slightly reduced due to the stronger coupling from back gate in the L_G region, see Fig. 4.12(b).

Figure 4.13 shows that the Z^2-FET with advanced SOI structure of T_{ox} = 1 nm, T_{si} = 5 nm and T_{BOX} = 15 nm is scalable down to L_G = L_{IN} = 30 nm without significant degradation. If T_{BOX} is scaled even further, below 10 nm, the back gate can be replaced by a highly-doped ground plane (GP), commonly used in FD-SOI MOSFETs [73]. Thus the Z^2-FET is able to become a single-gate device, drastically simplifying the fabrication.

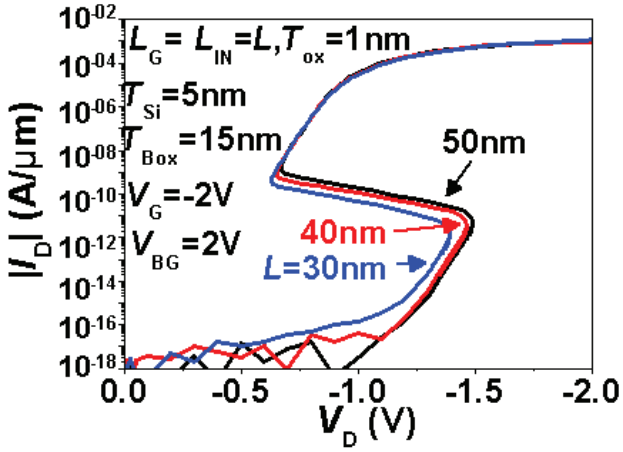

Fig. 4.13: Simulated I_D-V_D curves on V_{BG}-operated Z^2-FET with L_G = L_{IN} = L scaling from 50 nm to 30 nm at fixed V_G = –2 V. The simulated device has advanced SOI structure of T_{ox} = 1 nm SiO_2, T_{si} = 5 nm and T_{BOX} = 15 nm.

Figure 4.14(a) schematically shows the *p*-type Z^2-FET using a grounded 20 nm n^+-doped GP layer under an ultra-thin buried oxide T_{BOX} = 8 nm. The potential difference between the highly doped GP layer and the intrinsic channel is strong enough to form the carrier injection barrier in the L_{IN} region. The I_D-V_D simulation shows the same sharp switching and hysteresis as before, see Fig. 4.14(b), where we also show the opposite case of an *n*-type Z^2-FET with a p^+-doped GP layer. Even greater scalability, down to L = 20 nm, is possible if the Z^2-FET is simulated as having non-overlapping front and back gates, see Fig. 4.15. Evidently such a structure would be more difficult to fabricate, but a local GP in the L_{IN} region only, a planar double-gate process [74], or a fin-FET implementation can be envisaged.

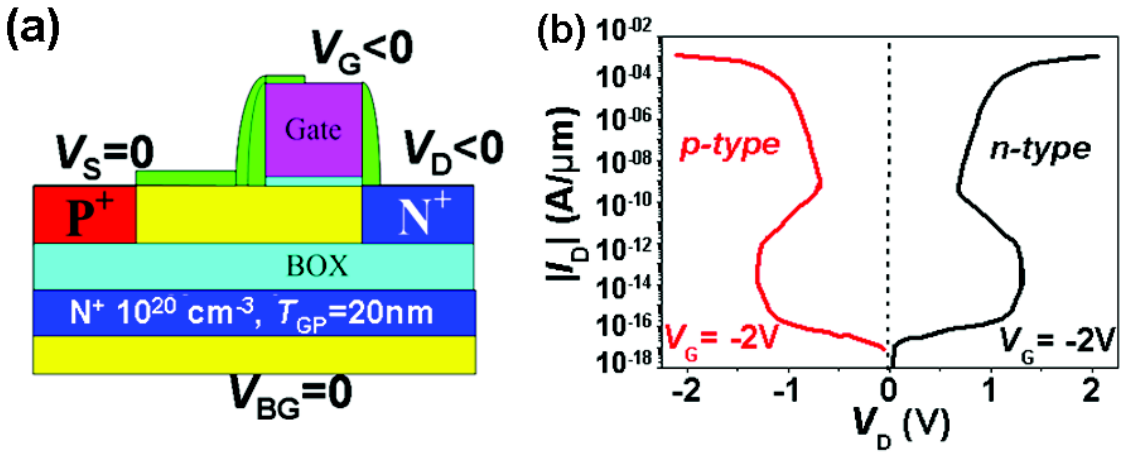

Fig. 4.14: (a) Schematic view of the p-type Z^2-FET using n^+-doped ground plane (GP) replacing V_{BG}; (b) simulated I_D-V_D curves of the *p*-type and *n*-type devices with $L_G = L_{IN}$ = 50 nm, T_{ox} = 1 nm SiO_2, T_{si} = 5 nm and T_{BOX} = 8 nm at fixed V_G = –2 and 2 V, respectively.

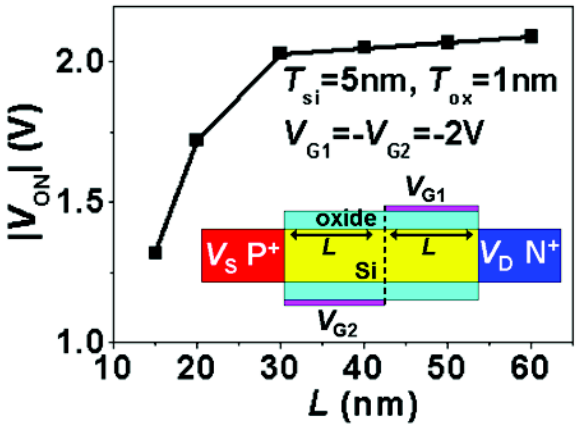

Fig. 4.15: V_{ON} *vs.* L_G of idealized Z^2-FET with non-overlapping gates, showing scalability down to 20 nm.

4.4. DC Model of Z^2-FET

We have developed a model of the feedback process in the Z^2-FET. The model uses a similar approach to standard thyristor modeling [75], except that impact ionization is not a factor and the doping-related bipolar action is replaced by the field-effect-controlled diffusion. The model combines four main equations describing the feedback process between the field-effect controlled diffusion current and the current-induced junction voltage.

4.4.1 Conception of the model

Figure 4.16(a) schematically shows a simplified Z^2-FET structure without the BOX. The device structure is similar to a p^+-n-p-n^+ thyristor, however the virtual doping in the L_G and L_{IN} regions is induced by the applied V_G and V_{BG} (or Q_S), respectively. Thus, the applied V_D drops at drain (V_{dj}), source (V_{sj}) and channel (V_{cj}) junctions as shown in Fig. 4.16(b). In the OFF state, the drain and source junctions are forward-biased, whereas the channel junction is reverse-biased.

Figure 4.16(a) explicitly shows the feedback process, where the electron diffusion current (I_n) is controlled by the drain junction voltage (V_{dj}). The I_n flows into the source and induces a source junction voltage (V_{sj}). The V_{sj}, in turn, controls the hole injection current (I_p), which flows into the drain and induces V_{dj} affecting the I_n. This forms a feedback loop which is modeled by four main equations including the generation of I_n and I_p by the V_{dj} and V_{sj}, respectively and, conversely, the effect that I_p and I_n have on V_{dj} and V_{sj}.

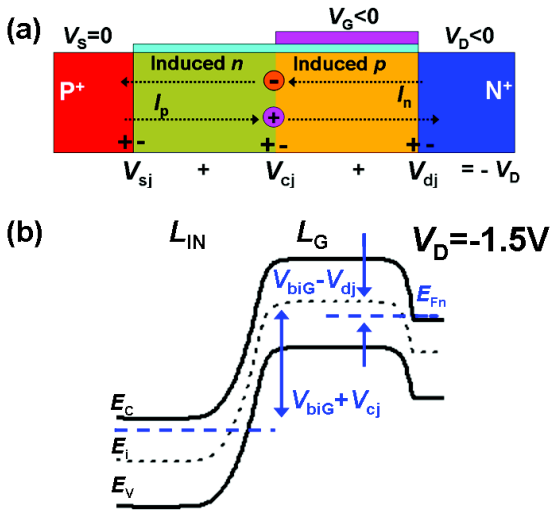

Fig. 4.16: (a) Simplified schematic view of the Z^2-FET without BOX. The applied drain voltage V_D drops at three junctions formed by field-induced carrier accumulation in L_G and L_{IN} regions; (b) simulated band diagram of the V_{BG}-operated Z^2-FET at V_D = –1.5 V.

4.4.2 Field-effect induced current flow

The diffusion current flow is controlled by the field effect due to the difference of the Fermi levels in the channel, see Fig. 4.16(b). It is modeled similarly to the subthreshold current in a MOSFET [3]. The I_n and I_p per unit gate width are given by:

$$I_n = I_{SG} \cdot exp(\frac{V_{biG}}{V_T}) \cdot \left[exp(\frac{V_{dj}}{V_T}) - exp(-\frac{V_{cj}}{V_T}) \right] \tag{4-1}$$

$$I_p = I_{SI} \cdot exp(\frac{V_{biI}}{V_T}) \cdot \left[exp(\frac{V_{sj}}{V_T}) - exp(-\frac{V_{cj}}{V_T}) \right] \tag{4-2}$$

where V_T is the thermal voltage defined by $V_T = kT/q$. Since both L_G and L_{IN} are small, the saturation currents I_{SG} and I_{SI} can be expressed by:

$$I_{SG} = \frac{q \cdot n_i \cdot D \cdot T_{si}}{L_G} \text{ and } I_{SI} = \frac{q \cdot n_i \cdot D \cdot T_{si}}{L_{IN}} \tag{4-3}$$

where n_i is the intrinsic carrier density and D is the appropriate diffusion coefficient. The V_{biG} and V_{biI} in Eqs. (4-1) and (4-2) are the built-in potentials that represent the field-induced equivalent doping in L_G and L_{IN} regions, respectively. They can be obtained using sheet charge approximation [67] as:

$$2 \cdot q \cdot T_{si} \cdot n_i \cdot sinh(\frac{V_{biG}}{V_T}) = C_{ox} \cdot (V_G - V_D - V_{dj} - V_{biG}) + C_{BOX} \cdot (V_{BG} - V_D - V_{dj} - V_{biG}) \tag{4-4}$$

$$2 \cdot q \cdot T_{si} \cdot n_i \cdot sinh(\frac{V_{biI}}{V_T}) = C_{BOX} \cdot (V_{BG} - V_{sj} - V_{biI}) \tag{4-5}$$

4.4.3 Current induced voltage drop at junctions

Given the currents in Eqs. (4-1) and (4-2), the junction voltage drops, V_{dj} and V_{sj}, induced by the flow of holes and electrons into the drain and source, respectively, can be modeled as in a normal diode [3]:

$$V_{dj} = V_T \cdot ln(\frac{I_p - I_{Rd}}{I_{Sd}} + 1) \tag{4-6}$$

$$V_{sj} = V_T \cdot ln(\frac{I_n - I_{Rs}}{I_{Ss}} + 1) \tag{4-7}$$

where the I_{Rd} and I_{Rs} are the recombination currents in the drain and source junctions, respectively. They are determined by the trap density and energy level. For simplicity, we will assume a midgap trap energy, so they are approximated by [3]:

$$I_{Rd} = I_r \cdot exp(\frac{V_{dj}}{2 \cdot V_T}) \text{ and } I_{Rs} = I_r \cdot exp(\frac{V_{sj}}{2 \cdot V_T}) \tag{4-8}$$

The saturation current I_{Sd} and I_{Ss} in Eqs. (4-6) and (4-7), respectively, are expressed by:

$$I_{Sd} = \frac{q \cdot p_{n0} \cdot D \cdot T_{si}}{L_D} \text{ and } I_{Ss} = \frac{q \cdot n_{p0} \cdot D \cdot T_{si}}{L_S} \tag{4-9}$$

where the p_{n0} and n_{p0} are the equilibrium hole and electron concentrations, L_D and L_S are the distances from junctions to source/drain electrodes (which are much smaller than the hole and electron diffusion lengths for all of our devices).

4.4.4 Validation of the model

Numerical methods can be used to solve the four main equations – Eqs. (4-1), (4-2), (4-6) and (4-7) – with the built-in potentials determined by Eqs. (4-4) and (4-5) for the V_{BG}-operated device. For the Q_S-operated device, the V_{biI} is taken to be 0.55 V, corresponding to strong electron accumulation in L_{IN} region. The saturation currents $I_{SG} = I_{SI}$, $I_{Sd} = I_{Ss}$ and I_r are used as fitting parameters. Figure 4.17 compares the solution of the model with the experimental data on Z^2-FETs operating with V_{BG} (same device as Fig. 4.1) and Q_S (identical to Fig. 4.5, except with L_G = 400 nm). The model reproduces the V_G-controlled hysteresis very well. It also shows negative resistance region, agreeing with simulation in Fig. 4.3.

The feedback loop is initiated by the field-effect induced electron injection instead of impact ionization. The device is initially in the OFF state, then as $|V_D|$ increases to around $|V_G|$ the L_G region is depleted, and thus the built-in potential V_{biG} increases almost linearly, according to Eq. (4-4). This exponentially increases the electron current from Eq. (4-1), which is captured by our model – compare to the experimental Q_S-operated device shown in Fig. 4.16(b). This phenomenon is masked by the gate leakage current in the V_{BG}-operated device, shown in Fig. 4.17(a).

The developed model can be used for not only the Z^2-FET but also other field-effect controlled positive feedback devices, such as FED and FB-FET [7, 30-32].

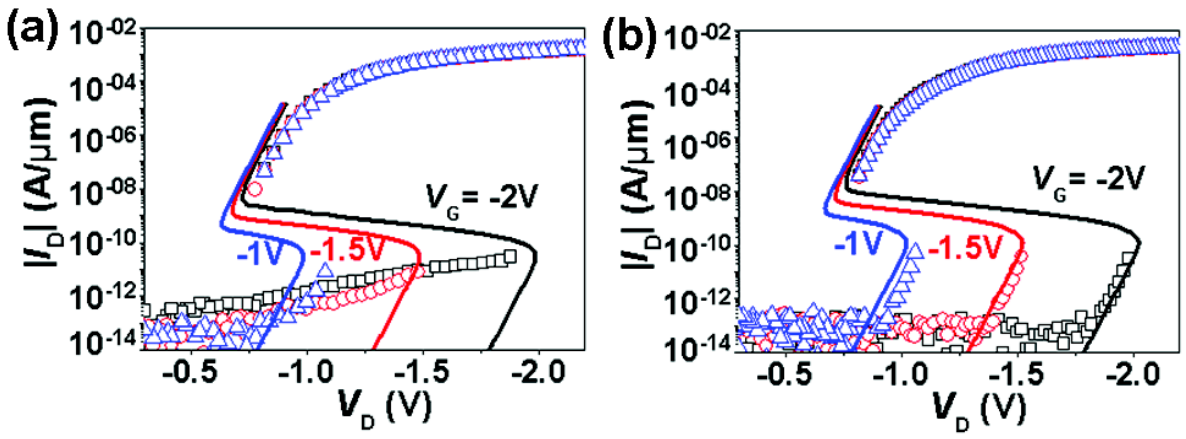

Fig. 4.17: Comparison between experimental data (open dots) and model (solid curves) for the *p*-type Z^2-FETs operating with (a) $V_{BG} = 2$ V and (b) Q_S.

4.5. Discussion

Despite its exceptionally low subthreshold swing and high ON current, the Z^2-FET still faces major issues in order to be used as a three-terminal logic switch. Figure 4.18(a) shows the I_S-V_G measurements on the same device as in Fig. 4.1. As V_G is swept from –0.5 V to 0.5 V, the device sharply turns on, as in Fig. 4.2. However, the device cannot be turned off simply by sweeping V_G back from 0.5 V to –0.5 V. This effect is unexpected for the switch application. In the ON state, high densities of holes and electrons are injected from source and drain into the channel, see the simulation in Fig. 4.18(b). This forms an electron-hole plasma, which screens the control of top and bottom gates on the channel. This issue may be solved by sweeping V_G down together with V_S (or V_D), since the device can be turned off by decreasing the $|V_S|$ (or $|V_D|$).

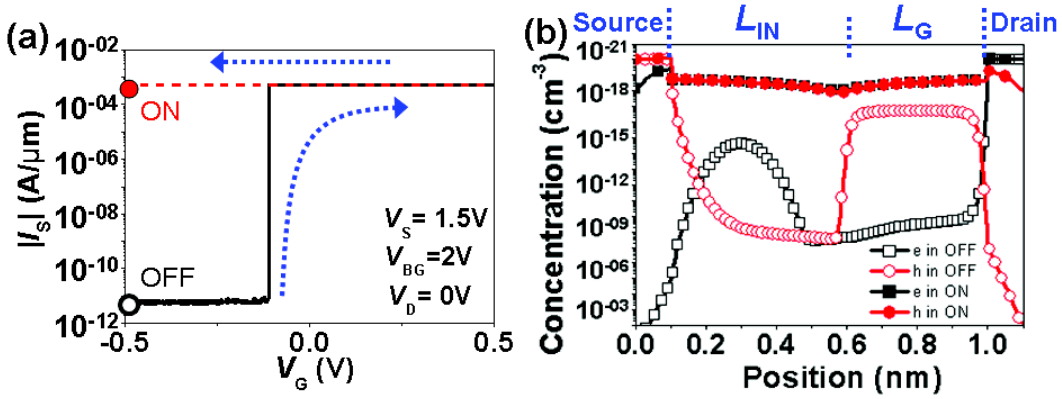

Fig. 4.18: (a) I_S-V_G measurements on the Z^2-FET in Fig. 4.1 reveal that, after the device is turned on by sweeping V_G from -0.5V to 0.5V, it is not turned off by sweeping V_G from 0.5V back to -0.5V. (b)

Comparison of the simulated hole and electron concentration between ON (solid symbols) and OFF (open symbols) states at the same bias of V_G=-0.5V and V_S=1.5V.

Another issue of the Z^2-FET is that the I_{ON} degrades as $|V_D|$ or $|V_S|$ decreases, see Fig. 4.2 and 4.5, same as in the FB-FET [7]. This is due to that in the ON state, the Z^2-FET (and FB-FET) is a forward-biased diode, and thus its diffusion current decreases exponentially as the junction voltage decreases, as shown by the I_D–V_D curves in Fig. 4.1 [3]. The significant decrease of the drain current at low $|V_D|$ can degrade the voltage swing and operation speed in a digital inverter chain made up of Z^2-FET-based inverters, since the charging/discharging of the gate capacitor in a later inverter decreases the drain voltage of devices in the preceding inverter. Figure 4.19 compares the Z^2-FETs built on Si and $Si_{0.35}Ge_{0.65}$ substrates, showing that the use of $Si_{0.35}Ge_{0.65}$ increases the I_{ON} by over a factor of 10, thanks to higher diffusion current in lower band-gap material.

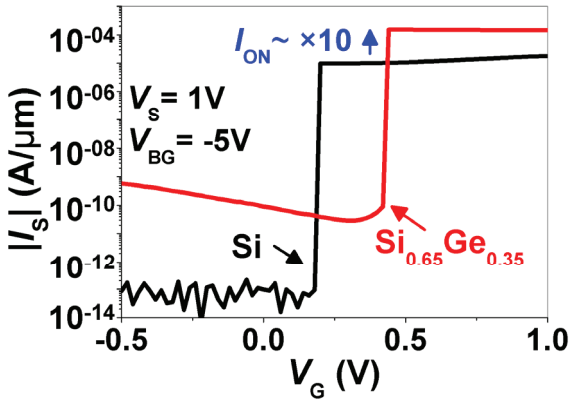

Fig. 4.19 Comparison of the I_S-V_G measurements on the Z^2-FETs with Si and $Si_{0.35}Ge_{0.65}$ channel.

4.6. Conclusion

In this Chapter, we presented a systematic DC study on a new, compact sharp-switching device we have named the Z^2-FET. Our device is fully compatible with SOI fabrication, has a single front gate, can be operated with either a back gate bias V_{BG} or dielectric stored charge density Q_S, shows very high $I_{ON}/I_{OFF} > 10^9$ ratio and a near-zero subthreshold swing $SS <$ 1mV/dec. The device also exhibits voltage-controlled hysteresis in I_D-V_D domain with V_{ON} linearly controlled by V_G. The operation of the Z^2-FET, as confirmed by TCAD simulations, involves positive feedback between carrier flow and carrier injection barriers, with no need for impact ionization, enabling good temperature stability and reliability. The scaling capability is studied through both experiments and simulations. The results show that the Z^2-FET built on advanced SOI substrate is scalable down to 30 nm (20 nm in an advanced

structure with non-overlapping gates). We also have developed an analytical model using field-effect controlled diffusion that reproduces our experimental results.

As a three-terminal logic switch, the Z^2-FET is problematic despite its very sharp switching properties due to the hysteresis in the V_G-controlled characteristics, since the current cannot be switched off by V_G alone. On the other hand, this same hysteresis is very useful for Z^2-FET used as one-transistor (1-T) memory. The details are presented in Chapter 5.

Chapter 5: Z^2-FET: Memory applications

Abstract – In this chapter, we demonstrate experimentally the use of the Z^2-FET as capacitor-less one-transistor dynamic random access memory (1T-DRAM) with non-destructive readout capability. In the Z^2-FET DRAM, the charges are directly stored on the front-gate capacitor (C_G) and read out through the fast internal feedback regeneration process. The simulated read/write times of our device reach below 1 ns, much faster than conventional DRAM. The retention of devices with different dimensions is studied in details under various temperatures and supply voltage V_{DD} as low as 1.1 V.

The SRAM application of Z^2-FET is also demonstrated without the need of refreshing the stored data, albeit with relatively high static power consumption. Various methods of reducing the static current using back-gate bias V_{BG} or heterojunctions in the Z^2-FET structure are also discussed.

5.1 Introduction

The conventional dynamic random access memory (DRAM) combining one transistor and one external capacitor (1T-1C DRAM) has shown good reliability and high integration density [76]. However, the external capacitor is difficult to downscale because it needs to store enough charge to maintain a sufficiently long retention time t_{re}. State-of-the-art capacitors feature high aspect-ratio structure, which are difficult to fabricate [77]. The access speed of DRAM is also limited by the amount of stored charge [76].

As a result, the capacitor-less single transistor DRAM (1T DRAM) is of great interest due to its compact device form and no need of external capacitor [78-79]. A number of demonstrated 1T DRAMs use the floating body effect, where the stored majority carriers control the flow of minority carriers. Early floating body memory was built on PD-SOI substrates and uses the neutral body for charge storage. State "1" was represented by the excess majority carriers accumulated in the neutral body, raising the body potential and increasing the drain current, see Fig. 5.1(a). Conversely, in state "0" the excess majority carrier were removed from the body, reducing the output drain current due to higher V_{th}, as shown in Figs. 5.1(b) and (c).

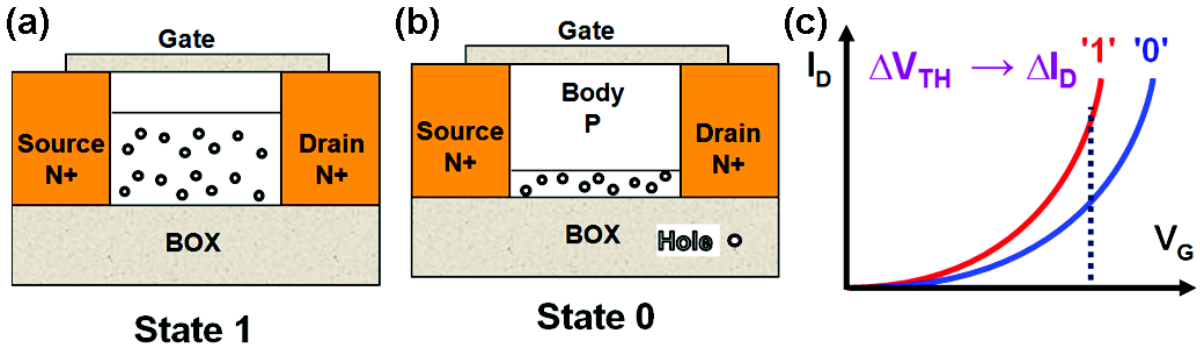

Fig. 5.1: Schematic view of the PD-SOI NMOSFET used as floating-body 1T-DRAM in (a) logic "1" and (b) "0" states. (c) The corresponding I_D-V_G curves show the shift of the threshold voltage V_{th} resulting in different drain current [80].

A more recent type of floating body 1T DRAM, the meta-stable dip RAM (MSDRAM) [81], is built on an FD-SOI substrate and uses the dynamic interchannel coupling for charge storage and readout. Due to channel deep depletion in the "0" state, large hysteresis is observed between direct and reverse sweeps, see Fig. 5.2(a). Since the electrons and holes need to coexist in the same channel, the scaling of the floating-body memory is limited by the supercoupling effect, which forbids the simultaneous formation of accumulation and inversion layers in the same thin channel [82]. The advanced-RAM (ARAM) has been

proposed to overcome this issue by separating the electrons from holes by a thin dielectric layer separating two section of the body [83].

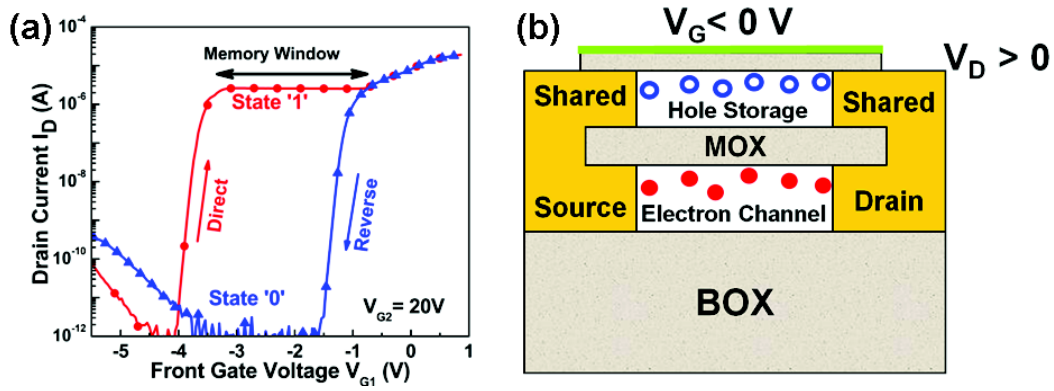

Fig. 5.2: (a) I_D-V_G measurements on an FD-SOI NMOSFET showing hysteresis between direct and reverse sweeps [81]. (b) Schematic view of the ARAM using a thin dielectric layer to separate the electrons and holes [83].

Another interesting 1T memory is based on a thyristor structure (TRAM), which shows reasonable integration density and fast access speed [11, 28], but requires precise doping control to obtain stable bipolar characteristics under various temperatures [29]. Another example is the field effect diode (FED) with two front gates, which has sharp switching and hysteresis properties [31-32, 70]. This FED, based on field effect-controlled barrier modulation, was originally proposed for electrostatic discharge (ESD) protection [31-32, 70] and then as a memory device with good simulated scaling capability [31-32, 70].

In this chapter, we demonstrate experimentally the use of the Z^2-FET as a 1T DRAM with supply voltage down to 1.1 V and retention time t_{re} up to 5.5 s [71]. Compared to the TRAM, the Z^2-FET has a simpler structure with an undoped channel (no doping engineering), and unlike the FED it does not require the fabrication of two adjacent front gates. The Z^2-FET can also be used as a 1T SRAM, with no refreshing, albeit with significant static power consumption. We show that the static power consumption can be reduced by combination of back gate and surface charge effects or by using heterojunctions in the Z^2-FET channel.

5.2. Basic operation of the Z^2-FET DRAM

Transient measurements are performed on Z^2-FET to explore its application as a 1T DRAM. Figure 5.3 schematically shows the experimental setup for transient measurements. As discussed in the preceding chapter, sharp switching between low and high current states can be obtained as a function of the front gate voltage V_G, which controls the electron

injection barrier, whereas the hole injection barrier is set either by a fixed V_{BG} = 2 V or by the surface charge Q_S (in which case V_{BG} = 0). To program and read, voltage pulses are applied on gate and drain. The source current is measured as the output read signal. The states "1" and "0" are differentiated by the storage of a positive charge (or no charge) under the front gate.

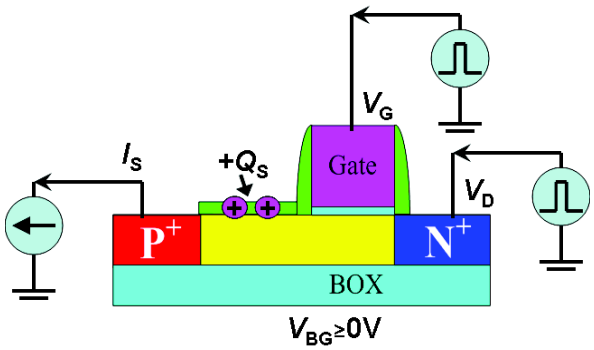

Fig. 5.3: The setup of transient measurements on a *p*-type Z^2-FET.

5.2.1 Readout of logic states by transient feedback

The use of Z^2-FET as a 1T DRAM takes advantage of the transient feedback property. Figure 5.4 shows the transient test on the Z^2-FET. The V_G is fixed at –1.7 V to store holes on the front gate capacitance ("1" state). Voltage pulses from 0 to –1.3 V with different fall/rise times (t_f) are applied to the drain electrode, see Fig 5.4(a). When the V_D fall/rise time is long, with t_f =2 µs, the device remains in the OFF state with low output source current I_S, shown in Fig. 5.4(b). This is because $|V_D|$ is always lower than $|V_G|$, and thus the flow of carriers is blocked by the potential barrier formed by $|V_G|$, in agreement with the DC measurements in Fig. 4.5. However, if the t_f is short enough (t_f = 15 ns), a V_D pulse down to –1.3 V can turn on the Z^2-FET, with I_S jumping to a large value of > 1000 µA/µm.

This surprising property can be understood by referring to the equivalent circuit of the Z^2-FET shown in Fig. 5.5(a), where we consider only the front-gate capacitor C_G and channel-drain junction (the source junction is reverse-biased, blocking any hole injection from the source).

In the "1" state, C_G is charged by the voltage difference between gate and drain (V_{GD} = V_G – V_D). The channel voltage V_C ~ 0, since the V_{GD} drops on C_G, see Fig. 5.5(a). As V_D decreases to –1.3 V, the V_{GD} changes from –1.7 V to –0.4 V causing a discharge of holes through the forward-biased drain junction (D_d). The discharging current $I_{tp} \sim \Delta Q/t_f$, where ΔQ is the change in the charge on C_G and t_f is the rise/fall time, and for long t_f the I_{tp} is too low to turn on the Z^2-FET.

However, if the t_f is short enough, as V_D drops down to –1.3 V the channel potential initially remains near zero and the diode D_d is temporarily forward-biased by the full 1.3 V, see the right panel of Fig. 5.5(a). This causes a large injection of electrons from the drain into the channel. The flow of electrons reduces the hole injection barrier in the source junction and induces the feedback process, turning on the device sharply as explained in section 4.2.2.

Conversely, if for whatever reason there is no charge stored on C_G even though V_G = –1.7 v, the voltage V_{GD} drops at the D_d and makes it deeply reverse-biased, as shown in Fig. 5.5(b). In this case, the device stays in the OFF state no matter how quickly V_D is pulsed from 0 down to –1.3 V, with I_S remaining low, as shown in right panel of Fig. 5.5(b).

To summarize, the logic states of the Z^2-FET DRAM can be represented by the mobile charge stored on the front gate capacitor C_G. Logic "1" and "0" correspond to high and low charge storage, respectively, and these states are read out using a V_D pulse with short fall/rise time (15 ns in the experiment limited by our equipment): for logic "1", the negative V_D pulse turns on the device, whereas the device remains turned off with logic "0".

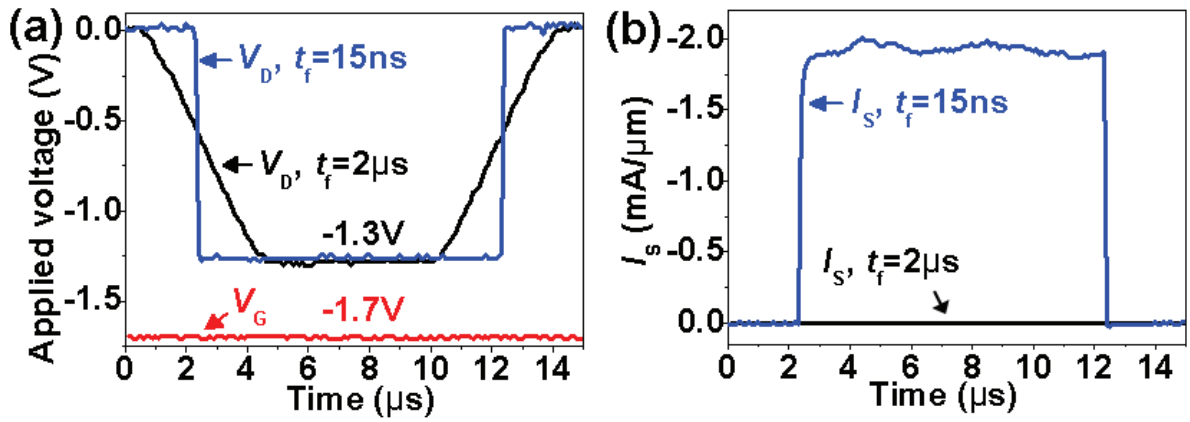

Fig. 5.4: Transient measurement of the "1" state by applying voltage pulses with different fall/rise time (t_f) on drain (a), with corresponding measured source current I_S (b). Only short t_f pulse can detect state "1". The device operates with surface charge and its parameters are T_{ox} = 6 nm SiO_2, T_{Si} = 20 nm, T_{BOX} = 145 nm, L_G = 400 nm and L_{IN} = 200 nm.

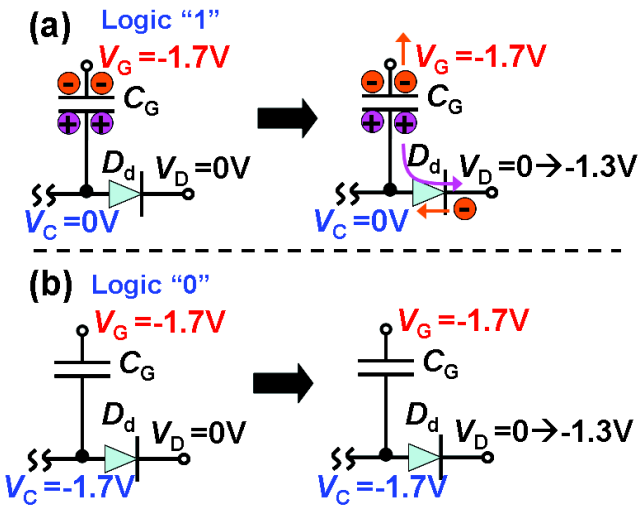

Fig. 5.5: Equivalent circuit of Z^2-FET explaining the readout of (a) "1" and (b) "0" logic states.

5.2.2 Writing of logic states and basic operation

The write procedures for logic "0" and "1" are illustrated by the equivalent circuit in Fig. 5.6. The writing of logic "0" is depicted in Fig. 5.6(a), where V_G is pulsed from –1.7 V to 0, while V_D = 0. The rise of body potential turns on the drain junction. This discharges the C_G through the forward-biased drain diode, overwriting the former "1" state. As V_G decreases back to –1.7 V in the hold state, C_G cannot be quickly recharged: no hole injection is possible from the grounded source and parasitic recharging occurs only via the small leakage current in the reverse-biased drain junction, giving logic "0" a finite but long retention time t_{re}.

Conversely, to write logic "1" from logic "0", V_G is again pulsed from –1.7 V to 0 and V_D is simultaneously pulsed from 0 to –1.3 V, as shown in Fig. 5.6(b). This eliminates the injection barriers and turns on the device, corresponding to the $|V_D| >> |V_G|$ situation: the current goes high and electrons and holes are injected into the channel. As the device switches back to the hold state, V_G = –1.7 V and V_D = 0, holes are stored on C_G. This represents the equilibrium configuration, so logic "1" has an infinite retention time t_{re} and requires no refreshing.

This DRAM functionality is demonstrated experimentally in Fig. 5.7. Figure 5.7(a) illustrates the writing of logic "0" by pulsing V_G from –1.7 V to 0 (with V_D = 0) and then returning to the hold state. Subsequently, using the V_D readout pulse, the correct "0" value is read out after a delay t_0 = 1 s, but not after 1.5 s. The retention time of the cell is therefore ~ 1.5 s. Figure 5.7(b) shows the writing of logic "1" with simultaneous V_G and V_D pulses, as well as the correct readout after t_0 = 1 s and 10 s (as explained earlier, logic "1" has infinite t_{re}).

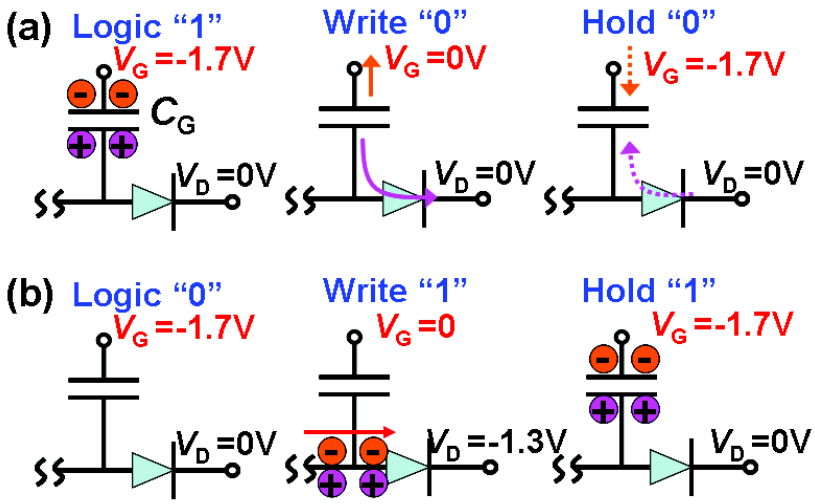

Fig. 5.6: Equivalent circuit picture of writing "0" (a) and "1" (b) logic states. The dashed line in the hold "0" right-most panel of Fig. 5.6(a) corresponds to the leakage current in the reverse-biased drain junction that limits the retention time of logic "0".

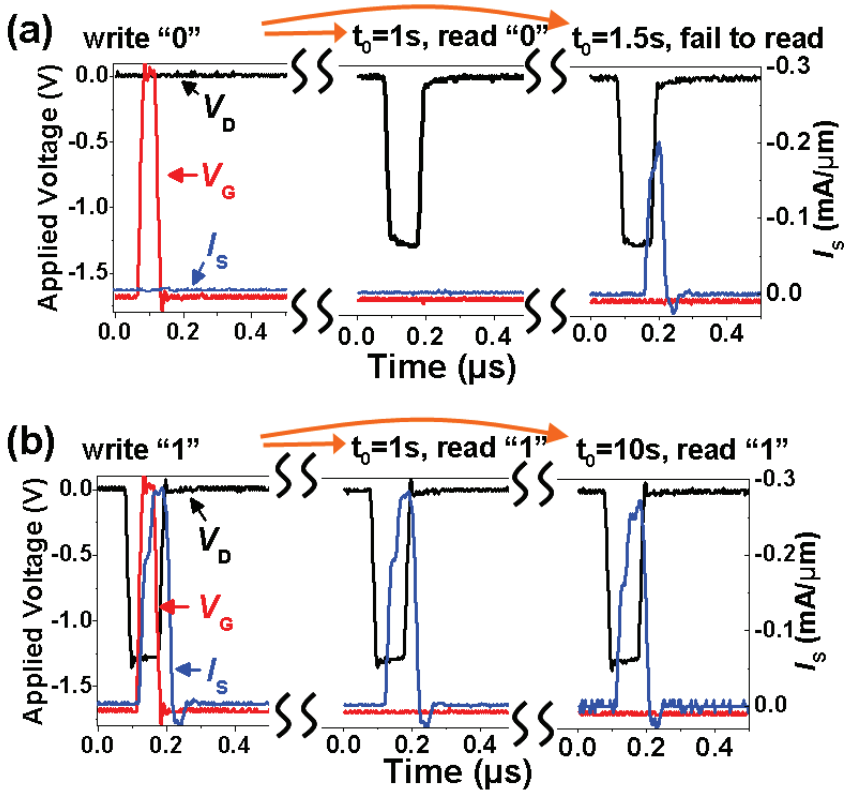

Fig. 5.7: Experimental results show the Z^2-FET DRAM operation waveforms. (a) The logic "0" is written by V_G pulse and read out correctly by V_D pulse after a delay of t_0 = 1 s, but not after t_0 = 1.5 s, due to limited retention time t_{re}. (b) The logic "1" is written by simultaneous V_G and V_D pulses and read out correctly by V_D pulse after t_0 = 1 and 10 s (t_{re} is unlimited in logic "1"). The device has same dimensions as in Fig. 5.4.

5.3. Properties and performance of Q_S-operated Z^2-FET DRAM

Unlike the conventional 1T-1C DRAM, the readout in Z^2-FET DRAM is nondestructive. Furthermore, the supply voltage is scalable down to 1.1 V, as we will demonstrate experimentally in Q_S-operated Z^2-FETs. The retention time is studied in detail as a function of temperature, bias and device dimensions. We show that both the retention time and the access speed are very competitive with state-of-the-art conventional DRAMs.

5.3.1 Non-destructive readout

Unlike the conventional 1T-1C DRAM, where the readout erases stored charge, the readout in a Z^2-FET DRAM is not only nondestructive but also capable of refreshing the logic "0" and thus prolonging the retention time. Figure 5.8 shows that a series of reading pulses, separated by 5 ms, applied following the writing pulse yields the correct output even after 1000 pulses. Further, the retention time of logic "0" is prolonged to over 5 s, much longer than the 1 s value reported in Fig. 5.7, without a train of readout pulses.

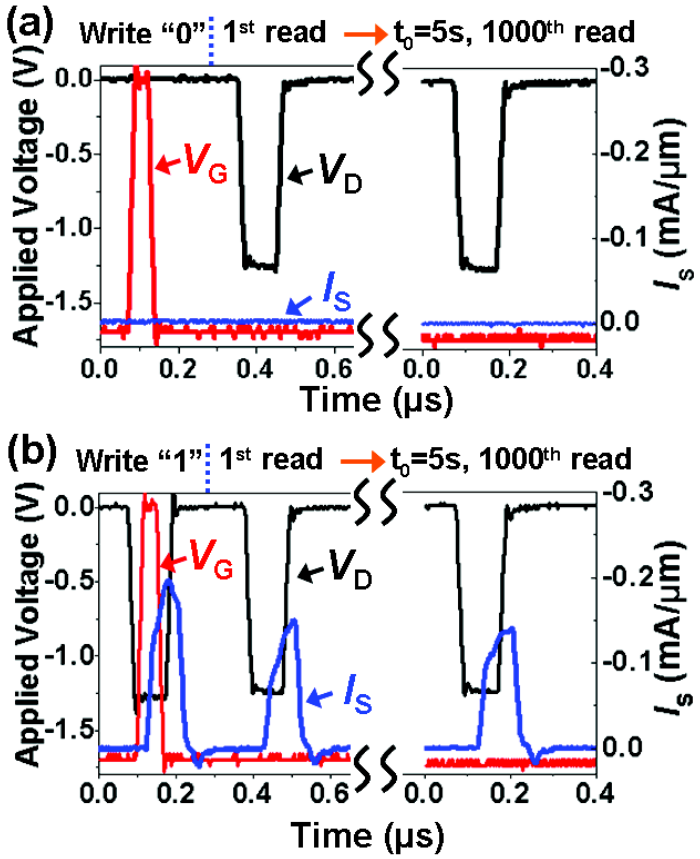

Fig. 5.8: Measurements on Q_S-operated Z^2-FET DRAM show nondestructive readout of logic (a) "0" and (b) "1" states. The reading pulse V_D is applied periodically every 5 ms and outputs correctly after 5 s in both states. The retention of the logic "0" is prolonged by the reading pulses, compare to Fig. 5.5.

The nondestructive readout can be explained by the equivalent circuit, shown in Fig. 5.9. For logic "0", ideally, there is no excess charge stored on C_G. However, after a long time in the hold stage, positive charges are collected at the C_G through leakage current of the reverse-biased drain junction, since $V_{GD} < 0$. This is indicated by the dashed arrows in the leftmost panel of Fig. 5.9(a). As they accumulate on C_G, these charges can eventually induce a high transient current upon the arrival of the readout pulse, this limiting the retention time t_{re} of the "0" state to ~1 s, as shown in Fig. 5.9(a). However, if readout pulse arrives before t_{re}, these charges are evacuated via a transient current that is high enough to turn on the device, see the middle panel of Fig. 5.9(a). This refreshes the logic "0", as shown in the rightmost panel of Fig. 5.9(a), prolonging its retention time.

For logic "1", C_G is charged by the V_{GD} in the holding stage. During the readout pulse, the transient discharging current initiates the feedback and turns on the Z^2-FET. An electron-hole plasma fills the channel of the turned-on Z^2-FET, which becomes essentially a forward-biased diode, as discussed in Chapter 4. As the device switches back to holding stage, excess holes are stored in the gate capacitor due to $V_{GD} < 0$. As a result, the charge corresponding to logic "1" is restored after readout, as shown in Fig. 5.9(b). This indicates that the readout of "1" is also nondestructive.

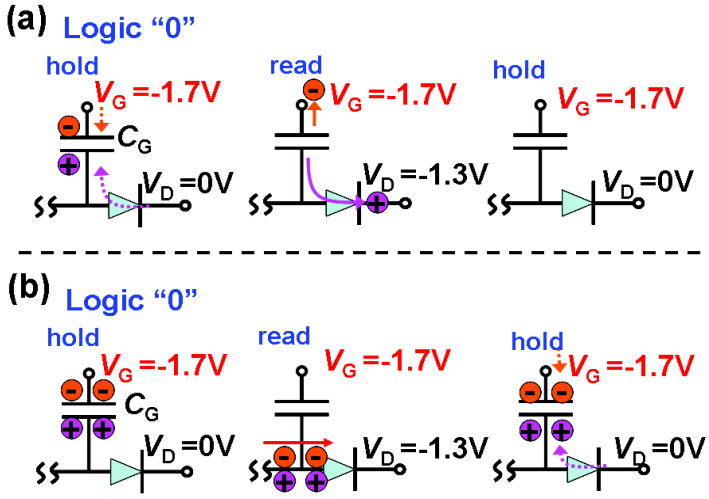

Fig. 5.9: Schematic illustration of the nondestructive readout of the (a) logic "0" and (b) "1" by the equivalent circuit.

5.3.2 High access speed

Figure 5.10 shows the TCAD simulation reproducing the operating procedure in Fig. 5.7. In simulation, the read/write times reach below 1 ns, easily outperforming conventional DRAM. Experimentally, we have demonstrated access times of 50 ns, limited by the available

probing equipment. In a conventional 1T-1C DRAM, the capacitance needs to be large to store enough charge to drive the external sensing amplifier, with considerable parasitic losses. This increases read/write time and dynamic power consumption. In our Z^2-FET DRAM, the charge storage requirements are much lower, because instead of directly reading out the stored charge, the Z^2-FET the stored charge seeds the internal feedback amplification that is activated with the fast reading pulse. Basically, the memory effect is triggered not by the stored charge ΔQ, as in conventional memories, but by the induced discharge current $\Delta Q/\Delta t_f$ that triggers the feedback, so a short readout pulse is important

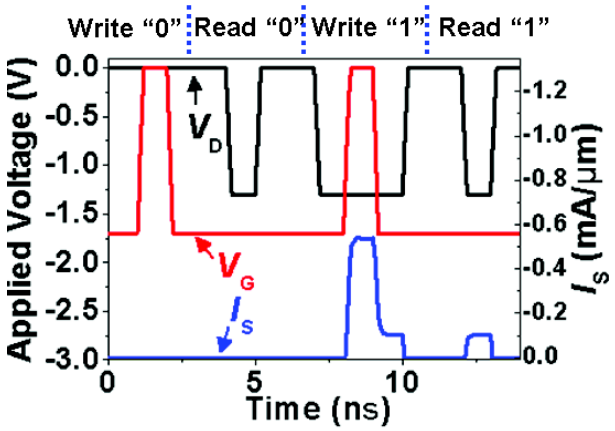

Fig. 5.10: Simulated Q_S-operated Z^2-FET DRAM demonstrates access time down to 1 ns.

5.3.3 Low operating voltage

The supply voltage of the Z^2-FET DRAM is scalable down to 1.1 V experimentally, which is lower than floating body memories and conventional 1T-1C DRAMs [76, 84], see Fig. 5.11(a) and (b). The retention time improves to 5.5 s due to lower leakage current, but the readout current of the "1" logic state is reduced to ~60 μA/μm. The scaling of the operating voltage in Z^2-FET DRAM is restricted by the turn-off voltage, which is the minimum voltage allowing the coexistence of two logic states as discussed in section 4.2.1. For silicon device, this voltage is around 0.8 V. A further decrease of the operation voltage can be achieved by using lower bandgap materials or the combination of backgate and surface charge, which is discussed in section 5.5.

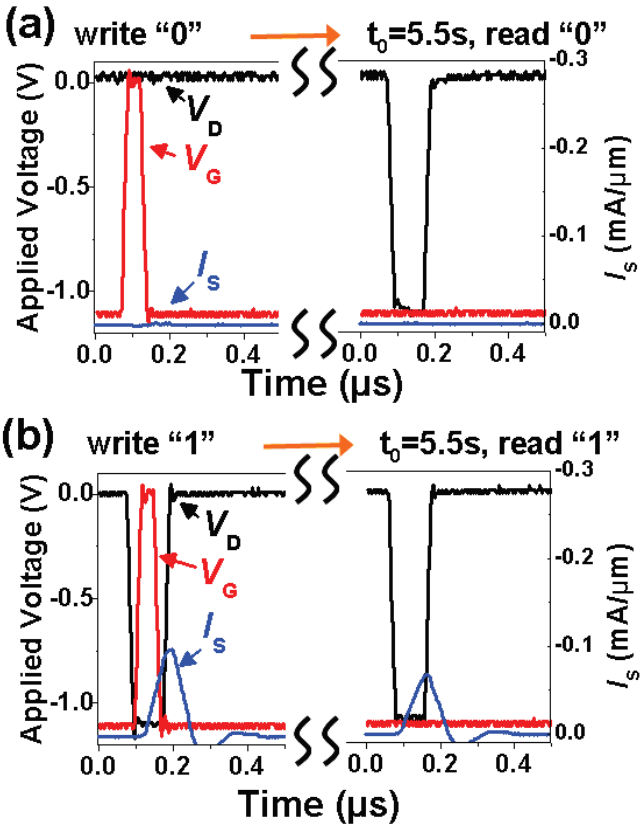

Fig. 5.11: Transient measurements show that the Z^2-FET DRAM in Fig. 5.7 operates properly under $|V_{DD}| = 1.1$ V with retention prolonged to 5.5 s, albeit with lower current for logic "1".

5.3.4 Retention time

As mentioned in section 5.2.2, the logic "0" with no charge stored in C_G is not an equilibrium state. The leakage current of the drain junction (I_{DLEAK}) recharges the C_G and eventually turns the "0" into "1". Since the $|V_G| > 0$ and $V_D = 0$ during the hold stage, the I_{DLEAK} only depends on V_G. For simplicity, we assume that the I_{DLEAK} does not change with time in the hold stage. Thus, the quantity of the charge replaced by the I_{DLEAK} after a limited retention time (t_{re}) in hold stage is $Q_{CG} = I_{DLEAK} \times t_{re}$. In the readout stage, some of these stored charges are evacuated by the V_D pulse. The quantity of the evacuated charge during read stage is expressed by: $\Delta Q_G = Q_{CG} - |V_G - V_D| \times C_G$, where the $|V_G - V_D| \times C_G$ is the residual charge left on C_G in read stage. If ΔQ_G exceeds a certain threshold value (ΔQ_{Gth}), it can induce a strong transient current to turn on the device and cause the failure of logic "0". Thus, the retention time can be obtained by combining the expressions of Q_{CG} and ΔQ_G:

$$t_{re} = \frac{|V_G - V_D| \cdot C_G + \Delta Q_{Gth}}{I_{DLEAK}(V_G, T)} \tag{5-1}$$

where the junction leakage I_{DLEAK} depends on V_G and temperature T. From Eq. (5-1), the retention time is sensitive to the operating voltage, temperature and gate capacitance determined by the device dimensions and gate oxide.

Figure 5.12 experimentally shows the dependence of t_{re} on V_G, V_D, T, L_G and L_{IN}. At high $|V_G|$, the junction leakage is dominated by the band-to-band tunneling, which decreases exponentially as $|V_G|$ decreases, prolonging the t_{re}, see Fig. 5.12(a). At low $|V_G|$, tunneling becomes negligible, I_{DLEAK} comes to be dominated by thermal generation, which does not depend on $|V_G|$, and the t_{re} saturates. Reducing $|V_D|$ in the readout pulse reduces the forward-biased voltage at the drain junction, see Fig. 5.5, and hence increases t_{re} according to Eq. (5-1).

The measurements under various temperatures indicate that the t_{re} decreases exponentially as T increases due to higher I_{DLEAK}, as shown in Fig. 5.12(b). The t_{re} at lower bias has stronger temperature dependence due to the thermal generation, whereas tunneling-dominated I_{DLEAK} at high $|V_G|$ is less sensitive to temperature.

Reducing L_G reduces the gate capacitance C_G and thus reduces the t_{re}, whereas changing L_{IN} does not have a strong impact on t_{re}, see Fig. 5.12(c).

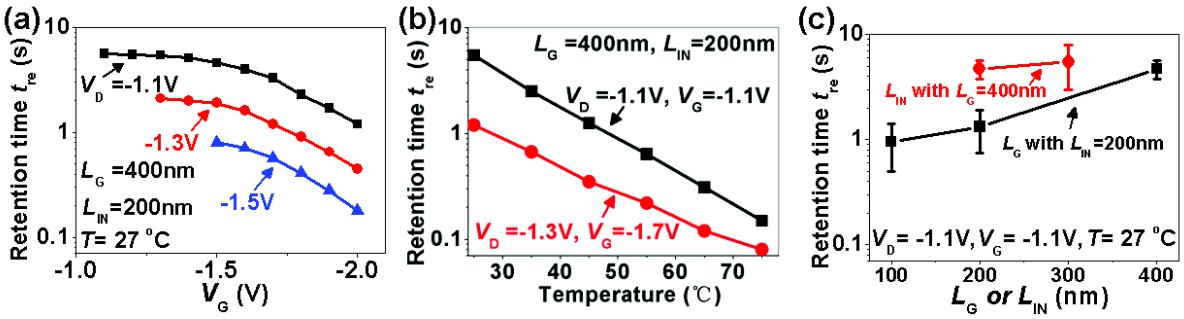

Fig. 5.12: Dependence of retention time of logic "0" (t_{re}) on the (a) applied V_G and V_D in holding and reading stages, respectively, (b) temperature (T) and (c) dimensions (L_G and L_{IN}). Note that the devices are Q_S-operated Z^2-FET DRAMs, same as in Fig. 5.7.

5.4. V_{BG}-operated Z^2-FET DRAM

The DRAM using the V_{BG}-operated Z^2-FET is similar to the Q_S-operated version, see Fig. 5.13. Same waveforms have been used for programming and reading, except for V_{BG} being fixed at 2 V. Using V_{BG} instead of Q_S is advantageous for controllability and reliability. No degradation is observed after cycling the write/read sequence 6×10^{10} times.

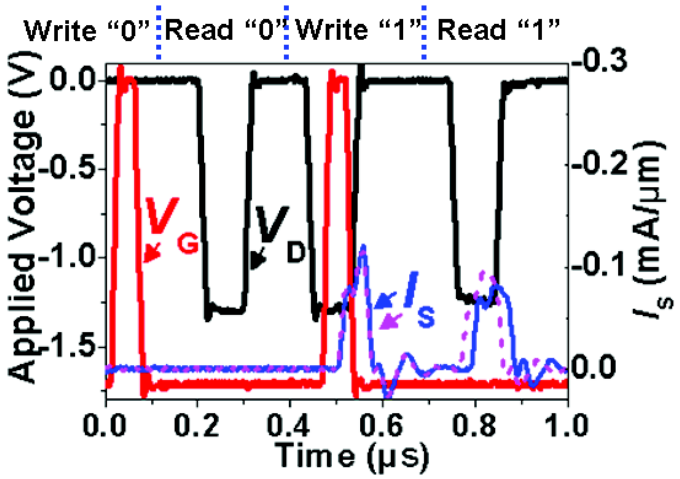

Fig. 5.13: DRAM operation waveform of the V_{BG}-operated Z^2-FET. The dashed curve shows the output current after 6×10^{10} cycles. The device parameters are: T_{ox} = 3 nm HfO_2, T_{Si} = 20 nm, T_{BOX} = 145 nm, L_G = 400 nm and L_{IN} = 500 nm.

5.5. Alternative mode of Z^2-FET DRAM operation and scalability

An alternative operation mode of the Z^2-FET DRAM uses the source-side MOSFET to write to C_G, as shown in Fig. 5.14(a). Here, C_G is charged through a transistor, like a standard 1T-1C DRAM, but the stored charge is still read out through the internal feedback, ensuring less required charge and higher speed. This mode is suitable for a device with two independent gates. Here, we use the V_{BG}-operated Z^2-FET for experimental demonstration, shown in Fig. 5.14(b), where the C_G is initially discharged through the drain junction (write "0"), and then recharged by the negative V_{BG} pulse turning on the source-side *p*-channel MOSFET. In the hold state, the holes are retained on C_G by the negatively biased front-gate V_G = –1.7 V. The memory state is correctly read out with the same V_D pulse via internal feedback, as discussed above.

Transient simulation is performed to demonstrate this operation mode in an downscaled Z^2-FET with two nonoverlapping independent gates, schematically shown in Fig. 5.15(a). The front gate is kept at –1.5 V whereas V_{BG} is used to control the source MOSFET for writing. The front gate C_G is discharged and charged by V_S = –1.5 V and 0, respectively, see Fig. 5.15(b). The stored logic states are correctly read out using the V_D pulse.

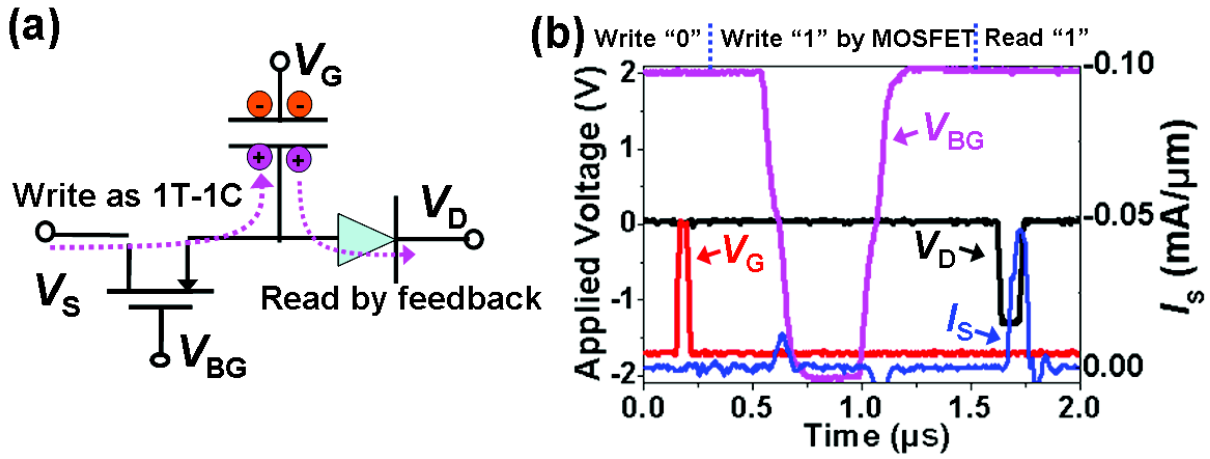

Fig. 5.14: (a) Schematic view and (b) experimental demonstration of the alternative DRAM mode using the source MOSFET for writing and the Z^2-FET feedback for reading.

This mode may be advantageous because of design rules analogous to the conventional 1T-1C DRAM. Another advantage of this mode is that the device stays in the OFF state in writing "1", see Fig. 5.15(b), consuming less power compared to the previous writing method described in section 5.2.2.

Figure 5.15 also demonstrates the ultimate scaling capability of the Z^2-FET DRAM down to $L_G = L_{IN} = 30$ nm, thanks to the improved electrostatic control due to ultra-thin $T_{si} = 5$ nm and nonoverlapping gates. Unlike the floating body memory [79], the scaling of T_{si} in the Z^2-FET does not suffer from the supercoupling effect. This is due to the fact that only one type of carriers (holes in this case) is needed to trigger the feedback during the readout stage in the Z^2-FET DRAM, whereas most of the floating-body memories use the coexistence of holes and electrons for reading.

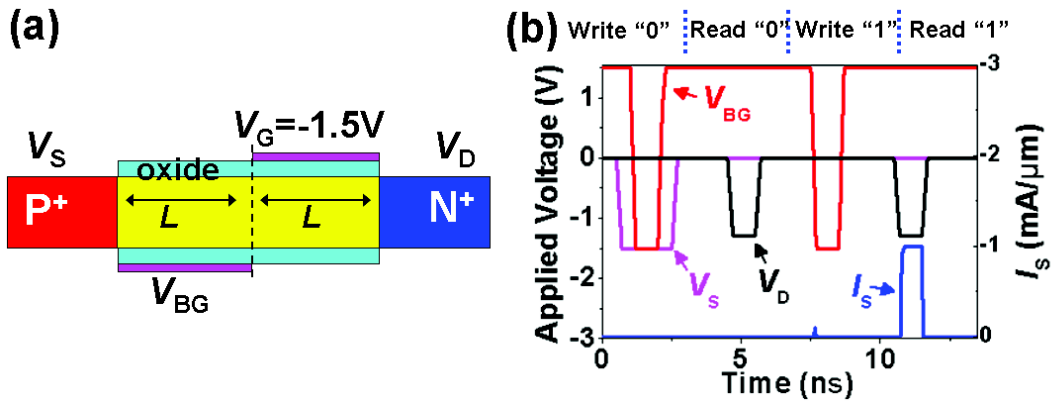

Fig. 5.15: (a) Schematic view and (b) transient simulation of the Z^2-FET DRAM operating with two independent nonoverlapping gates. The source MOSFET controlled by V_{BG} is used for writing. The device is scaled down to $T_{ox} = 1$ nm, $T_{Si} = 5$ nm, $L_G = 30$ nm and $L_{IN} = 30$ nm. The front gate V_G is fixed at –1.5 V.

5.6. SRAM application

In addition to the DRAM applications, the Z^2-FET can be directly used as static random access memory (SRAM) using the V_G-controlled hysteresis in I_D-V_D domain. In this mode, the two equilibrium states in the hysteresis window are used for storage and non-destructive readout, as shown in Fig. 5.16. The logic states are held at the lowest $|V_D|$ in the hysteresis window to minimize the holding current for logic "1". The states are read by raising the $|V_D|$, so in state "1" the device outputs a high current while in state "0" it remains OFF. The writing of "0" and "1" uses V_D and V_G pulses to move to regions of the I_D-V_D curve where the device has only one equilibrium state. To turn on the device, the $|V_G|$ and $|V_D|$ are respectively reduced and increased, to eliminate the injection barriers and trigger I_{ON}. To turn off the device, it suffices to reduce $|V_D|$ – see Fig. 5.16.

Figure 5.17 shows the experimental operation of the Z^2-FET SRAM using the same device as in Fig. 5.7. Compared to DRAM operation shown in Fig. 5.7, the logic states in SRAM mode are held at $|V_D|$ = 1 V and read out at $|V_D|$ = 1.3 V within the hysteresis window. To write "0" we pulse $|V_D|$ down to 0 to turn off the device; whereas to write "1" the $|V_D|$ is pulsed up to 1.3 V while $|V_G|$ is pulsed down to 0 to eliminate injection barriers. Both logic "0" and "1" have an infinite retention time and are read out correctly after 100 s.

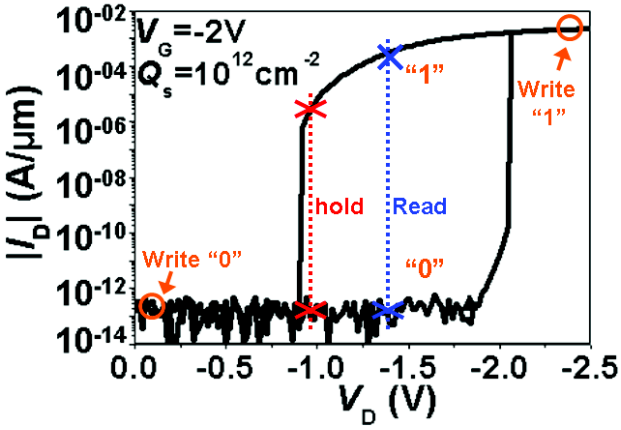

Fig. 5.16: I_D–V_D measurement on the Z^2-FET explaining the operation principle of the SRAM utilizing the hysteresis.

The disadvantage of the 1T-SRAM is the significant static current and power consumption for holding logic "1", see Figs. 5.16 and Fig. 5.17(b). To reduce the hold current for logic "1", two different methods can be envisaged. Figure 5.18(a) shows the I_D-V_D hysteresis of the Q_S-operated Z^2-FET as a function of V_{BG}. Compared to V_{BG} = 0, V_{BG} = –10 V increases the hysteresis window: $|V_{ON}|$ increases with due to the interchannel coupling in the L_G region,

which increases the electron injection barrier over that due to V_G alone; whereas switching to lower current happens at lower V_D because of the lower hole barrier in the L_{IN} region. As a result, the hold current, denoted I_h in Fig. 5.18(a), is reduced from 10^{-6} A/μm to 10^{-10} A/μm.

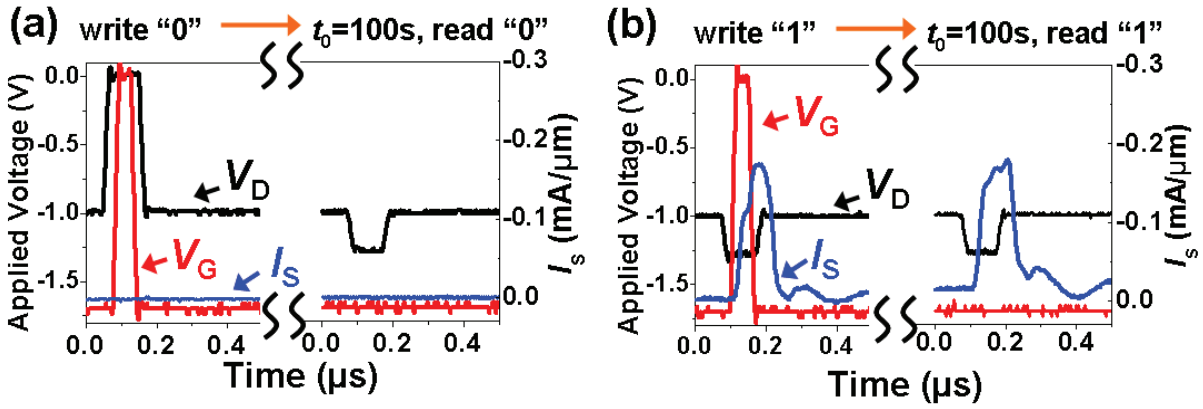

Fig. 5.17: Operation waveform of the SRAM using Q_S-operated Z^2-FET for (a) "0" and (b) "1" logic states. Compared to the DRAM, the SRAM logic states need no refreshing.

An alternative method to reduce I_h is to use heterojunctions, such as Si/$Si_{0.7}Ge_{0.3}$, in the channel and source/drain regions, as illustrated in Fig. 5.18(b). The I_D-V_D simulations were performed for a V_{BG}-operated Z^2-FETs with an advanced structure of L_G = 50 nm, L_{IN} = 50 nm, T_{ox} = 1 nm SiO_2, T_{Si} = 5 nm and T_{BOX} = 20 nm, while varying the channel and source/drain material composition. We find that when the Z^2-FET uses either Si or $Si_{0.7}Ge_{0.3}$ in both channel and source/drain regions, the I_h remains approximately the same, but when the channel is made of $Si_{0.7}Ge_{0.3}$ and source/drain regions are Si, I_h is markedly reduced thanks to higher injection coefficient in Si/$Si_{0.7}Ge_{0.3}$ heterojunction [85].

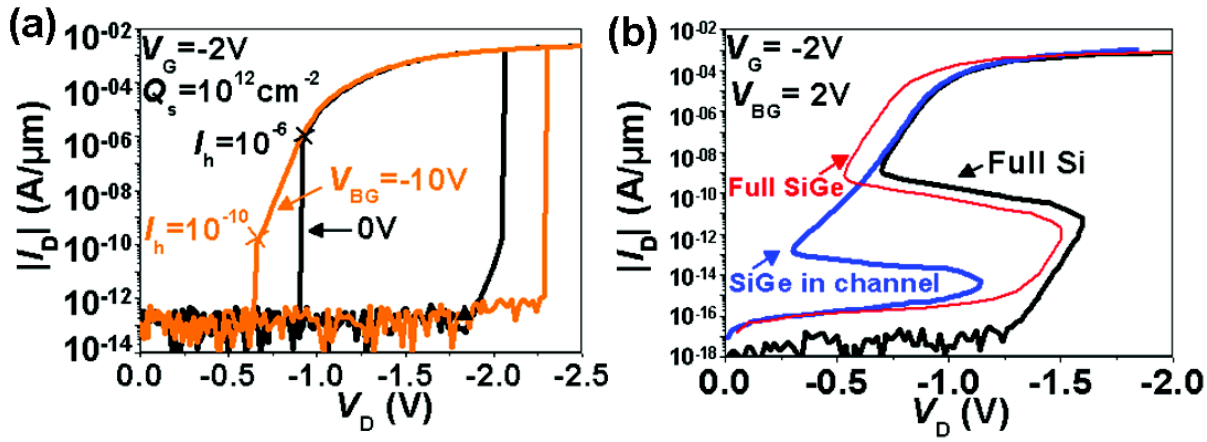

Fig. 5.18: Reduction of holding current I_h by (a) combining the Q_S and V_{BG} to adjust the injection barrier (experiment) and (b) using Si/$Si_{0.7}Ge_{0.3}$ heterojunction to enhance the injection coefficient (simulation).

5.7. Discussion

So far, the DRAM operation using Z^2-FET has been demonstrated experimentally on a single device. However, any technological insertion of the Z^2-FET DRAM requires successful array operation, with cells connected together as in Fig. 5.19. The operation on a selected cell should not cause the failure of other cells sharing the same V_D and V_G signal lines.

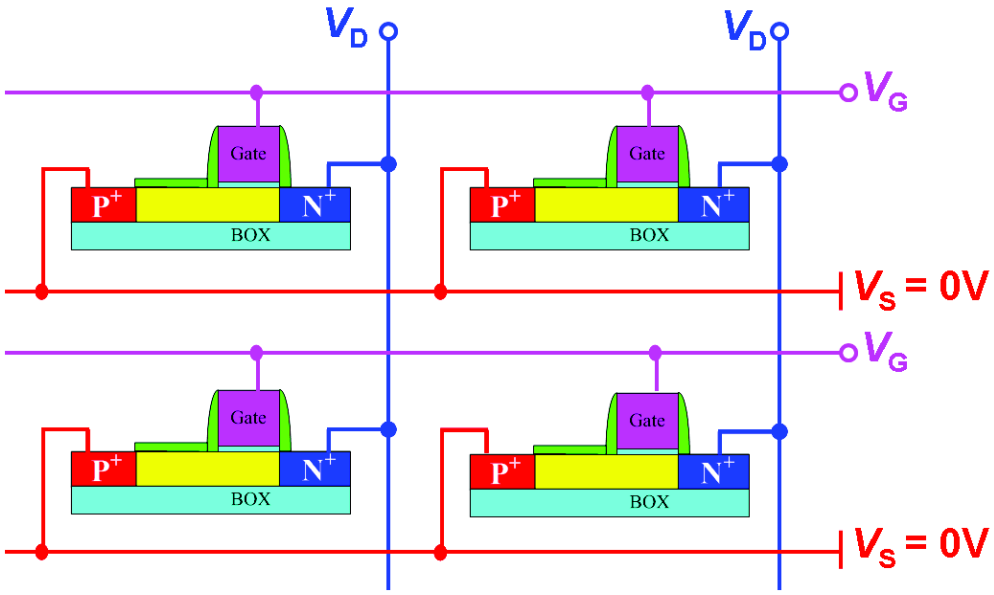

Fig. 5.19: Schematic view of a 2×2 DRAM array using Z^2-FET devices.

The writing of a selected cell should not affect the state of other cells. However, the simplest method for writing logic "0" discussed in section 5.2 for a single device cannot fulfill this purpose, since it uses only a V_G pulse, as shown in Fig. 5.7. During the writing "0" stage, all cells sharing the same V_G signal would be erased, as is evident from Fig. 5.19. The selective writing of a given cell needs the combination of both V_G and V_D signals.

Fortunately, the biasing for writing logic "0" can be easily modified to accommodate the DRAM array operation. The method is to replace the V_G pulse by simultaneous V_G and V_D pulses of smaller magnitude (Fig. 5.20). Thus, instead of raising V_G from –1.7 V up to 0, the V_G is only pulsed up to –0.7 V while V_D is simultaneously pulsed down from 0 to –0.7 V. By doing so, the V_{GD} becomes zero, which discharges C_G as required to write the "0" state. To demonstrate the validity of the modified biasing scheme, the initial "1" state is written using the standard biasing of Fig. 5.7, followed by the writing of "0" with the modified biasing of Fig. 5.20 – the read out correctly outputs a low current.

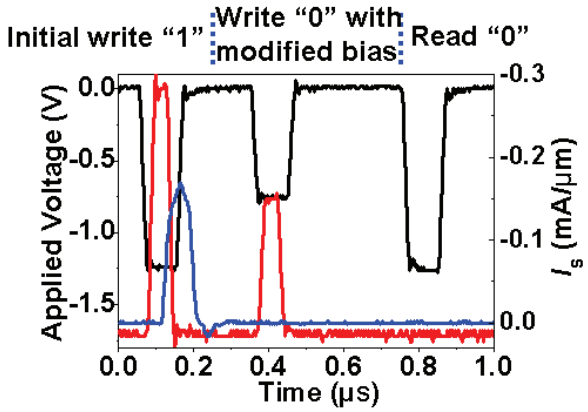

Fig. 5.20: Experimental results demonstrate the validity of the modified biasing with both V_G and V_D pulses for writing "0". The initial state is written by the unmodified bias developed for single device as in Fig. 5.7.

Figure 5.21 shows that the logic "1" state of a cell is not affected by either of the smaller V_G or V_D pulses used to write "0" in a different cell sharing one of the voltage lines – the readout is still correct. Only with simultaneous V_G and V_D pulses as in Fig. 5.20, can the "1" state be overwritten to a "0". This indicates that the writing is selective and nondestructive for cells sharing the same V_G or V_D signal line.

The principle behind this can be explained by the equivalent circuit, shown in Fig. 5.22. For an initial state of "1", the C_G is thoroughly discharged with both V_G and V_D pulses due to $V_{GD} = 0$, depicted by Fig. 5.22(a). However, with only a smaller V_G or V_D pulse, V_{GD} does not drop to zero, the C_G is only partially discharged and the residual charge is still enough for restoring "1" state, as shown in Fig. 5.22 (b).

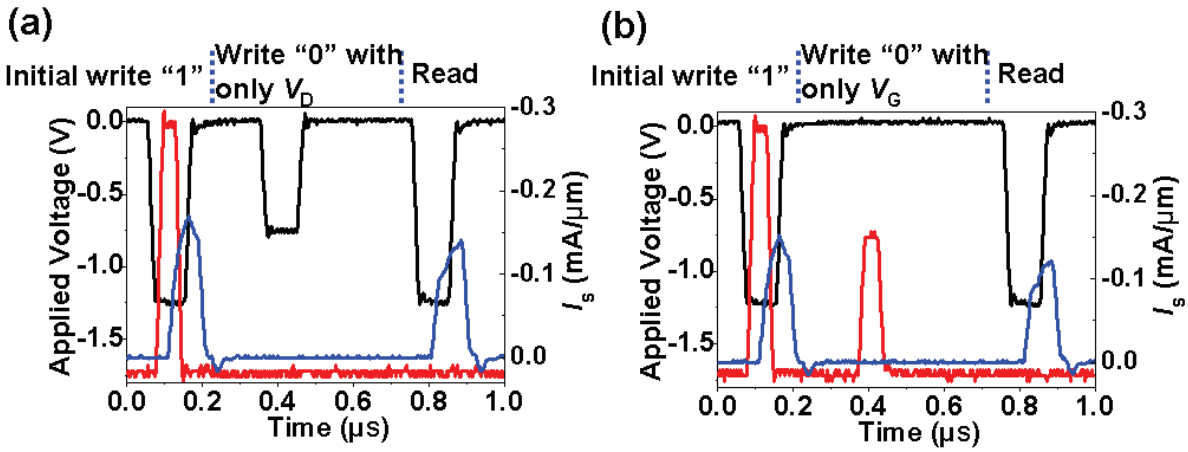

Fig. 5.21: Experimental results demonstrate that the initial state is not changed with only a smaller 0.7 V (a) V_G or (b) V_D pulse during the writing of a "0" state on a different cell.

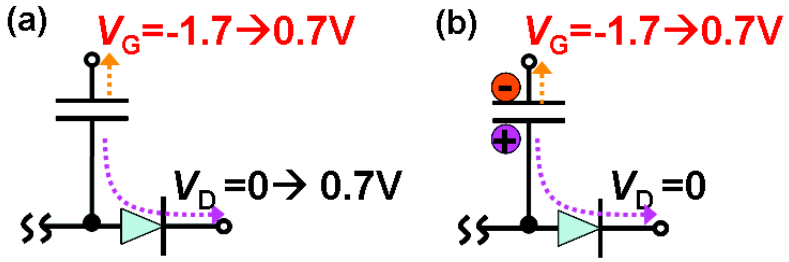

Fig. 5.22: Schematic view shows that the writing "0" (a) with both V_G and V_D pulse can thoroughly discharge C_G, whereas (b) the C_G is partially discharged with only a V_G pulse.

5.8. Conclusion

In this Chapter, we have presented a compact, capacitor-less DRAM device in FD-SOI utilizing the Z^2-FET. The logic states are distinguished by the charge stored in front gate capacitor C_G and read out through internal feedback, which regenerates the stored charge and achieves a nondestructive readout. The write procedures using fast V_G and V_D pulses to discharge and recharge the C_G have been demonstrated. Experimentally, the gate and drain biasing can be scaled down to 1.1 V, lower than conventional DRAMs. Simulations predict access times below 1 ns, permitting operation with smaller stored charge densities since charging and discharging currents are inversely proportional to the fall/rise times of the voltage pulses. The retention time has been studied in detail under various temperatures T, V_G, V_D and gate lengths. We achieved 0.15 s at T = 75 ^{o}C. The surface charge and V_{BG}-operated Z^2-FETs have both been used to demonstrate DRAM functionality. An alternative operation mode has been demonstrated using the source MOSFET for writing, similar to the 1T-1C DRAM, but the internal Z^2-FET feedback for reading, preserving the high readout speed. The operation of a DRAM array using Z^2-FETs has also been discussed, with a modified writing scheme leading to reliable operation of half-selected cells .

The SRAM operation using Z^2-FET has also been demonstrated. In this mode, the stored logic levels do not require refreshing. The power consumption induced by the static current can be reduced by combining the backgate and surface charge, or using the heterojunction.

Our Z^2-FET device has the advantages of compact, single front-gate footprint, undoped channel, and no impact ionization or bipolar action. The high performance and compact form will be of interest for the future memory applications.

Chapter 6: Bipolar-enhanced GIDL in MOSFETs and its application to enhancing TFET performance: the BET-FET

Abstract – In this chapter, we first consider GIDL current in short-channel MOSFETs and demonstrate by simulation that GIDL can be enhanced by a bipolar current triggered by interband tunneling. This bipolar amplification of GIDL can be suppressed in FD-SOI MOSFETs through the use of backgate voltage and scaling of the channel. Conversely, the same bipolar amplification effect can be used to enhance the I_{ON} of an appropriately modified TFET. We present a new device, named bipolar-enhanced tunneling FET (BET-FET), which combines a TFET with a heterojunction bipolar transistor (HBT) structure. The carriers generated in the tunneling junction are used as a base current to drive the HBT and obtain a high bipolar diffusion current. The simulated devices based on silicon and silicon-germanium show both low subthreshold swing and high I_{ON}, overcoming one of the main obstacles impeding the technological insertion of TFETs into digital circuitry.

6.1. Enhanced GIDL in short-channel FD-SOI MOSFETs

Figure 6.1 (a) shows the I_D-V_G measurements on the FD-SOI MOSFETs as a function of gate length (L_G) scaling from 1000 nm down to 35 nm. The threshold voltage is markedly reduced as L_G decreases below 50 nm, due to the short-channel effect [16]. The magnitude of the GIDL current in the $V_G < 0$ region does not change as L_G decreases from 1000 nm to 50 nm, as band-to-band tunneling is not sensitive to the gate length. On the other hand, for L_G below 50 nm, the GIDL current increases.

A preliminary variability measurement is also performed to compare devices with L_G = 1000 nm and 35 nm. For each L_G, three devices were randomly chosen in different locations on the wafer. Figure 6.1(b) shows that the GIDL current in long-channel MOSFETs shows little variation from device to device, whereas the enhanced GIDL current in L_G = 35 nm short-channel devices shows larger variation.

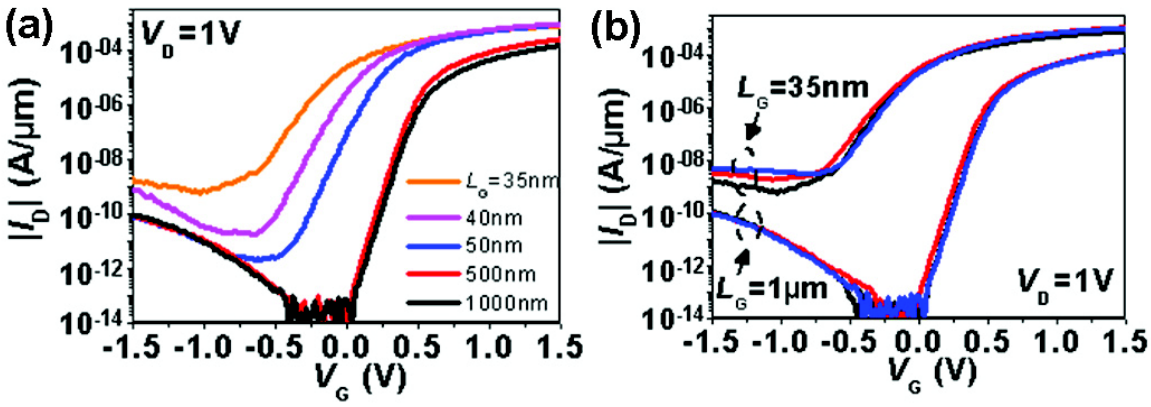

Fig. 6.1: (a) Measurements showing that the GIDL current of the FD-SOI MOSFETs increases as L_G falls below 40 nm. (b) Measurements on various devices reveal that the enhanced GIDL current has large variations in devices with L_G = 35 nm, but not in long-channel devices with L_G = 1000 nm. All devices had the same channel parameters: T_{Si} = 15 nm, T_{ox} = 3 nm HfO_2, T_{BOX} = 145 nm.

6.1.1. Explanation of the bipolar-enhanced GIDL using TCAD simulation

In order to understand the enhanced GIDL effect in the short-channel MOSFET, we performed Synopsys TCAD simulations. Figure 6.2(a) shows the simplified device structure with the same SOI and gate dimensions as the experimental devices in Fig. 6.1. The heavily and lightly-doped source/drain concentration (HDD and LDD) are 10^{20} cm^{-3} and 3×10^{19} cm^{-3}, respectively. In the simulation, the mobility model included the effects of doping, electric field and velocity saturation. For band-to-band tunneling, the dynamic non-local tunneling model was used, where the tunneling rate depends on the detailed band-diagram profile along

the tunneling path [86]. The simulation reproduces the experimental results with different L_G values, including the enhanced GIDL for L_G = 35 nm, see Fig. 6.2(b).

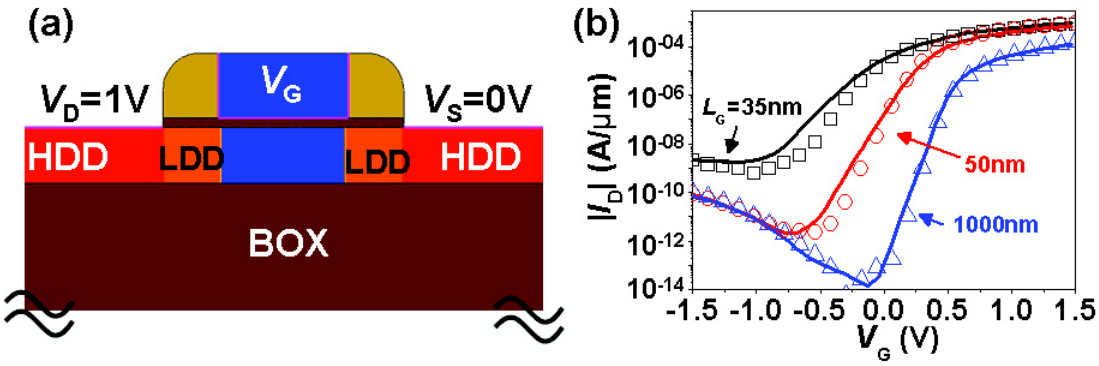

Fig. 6.2. (a) Simplified FD-SOI MOSFET structure used in our simulations, with the same L_G values as the experimental devices in Fig. 6.1. The heavily- and lightly-doped source/drain concentrations (HDD and LDD) are 10^{20} cm^{-3} and 3×10^{19} cm^{-3}, respectively. (b) Comparison between simulation (curves) and experiment (dots) shows good agreement.

Figure 6.3 shows the hole and electron current density and flow direction in a device with L_G = 35 nm, biased at V_D = 1 V and V_G = –1.5 V with respect to the grounded source. The holes are generated in the drain junction through band-to-band tunneling and flow to the source, see Fig. 6.3(a). This induces a potential drop at source junction and triggers the parasitic $N^+/p/N^+$ bipolar transistor, where the virtual p-doped region in the channel is formed by the gate, leading to an electron diffusion current from the source to drain near the back interface, see Fig. 6.3(b). The bipolar electron current can be very high in devices with small L_G, where the bottom of the channel is not well controlled by the front gate, see Fig. 6.3(b). Since the bipolar diffusion current is sensitive to variations in L_G and carrier lifetime, the bipolar-enhanced GIDL shows large variation compared to the normal GIDL current, see Fig. 6.1(b).

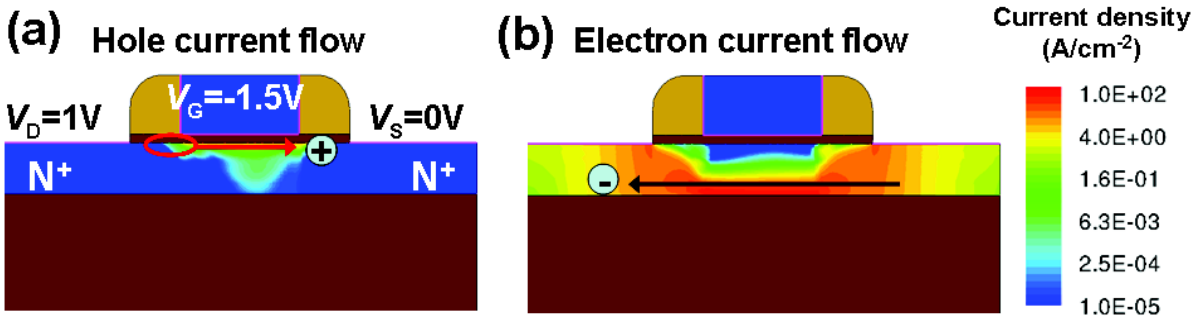

Fig. 6.3: Simulated (a) hole and (b) electron current densities in a MOSFET with L_G = 35 nm under V_D = 1 V and V_G = -1.5 V. The directions of hole and electron flows are indicated by the arrows.

6.1.2. Suppression of the bipolar-enhanced GIDL in MOSFETs

The GIDL current in a short-channel FD-SOI MOSFET can be suppressed either by reducing the bipolar current or the tunneling current (or both). The reduction of the tunneling current can be achieved by using lower LDD doping concentration to attenuate the electric field in the drain junction [87]. In order to reduce the bipolar amplification, the electron diffusion path at the bottom of the channel needs to be cut off. Figure 6.4(a) compares measured GIDL in MOSFETs with L_G = 35 nm under various backgate voltages V_{BG}. We find that V_{BG} = –10 V reduces the GIDL current to the value observed in long-channel L_G = 1000 nm devices, indicating that the bipolar amplification effect has been fully suppressed. This is confirmed by TCAD simulations in Fig. 6.4(b), which show that no significant electron diffusion current flows when V_{BG} = –10 V and the back channel is in accumulation. The residual GIDL current is only due to the tunneling current in drain junction, which is independent of L_G.

An alternative way to cut off the bipolar electron flow is to use an utra-thin active silicon layer. Figure 6.5 compares the simulated I_D-V_G curves of MOSFETs with L_G = 35 nm as a function of silicon channel thickness T_{si}. Scaling of T_{si} from 15 nm to 10 nm suppresses the electron diffusion current, thanks to the stronger control of V_G over the bottom of the channel, see Fig. 6.5(b).

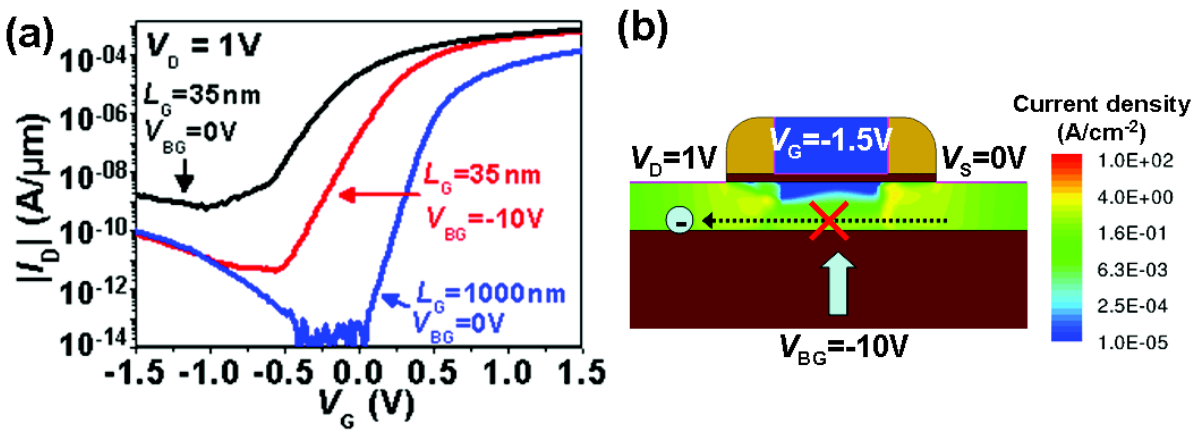

Fig. 6.4: Measured I_D-V_G curves of the MOSFETs with L_G = 35 nm and 1000 nm under various V_{BG} showing that the bipolar effect is suppressed by V_{BG} = –10 V. (b) Electron current density obtained in simulation showing that the flow of electron is cut off by the V_{BG} = –10 V.

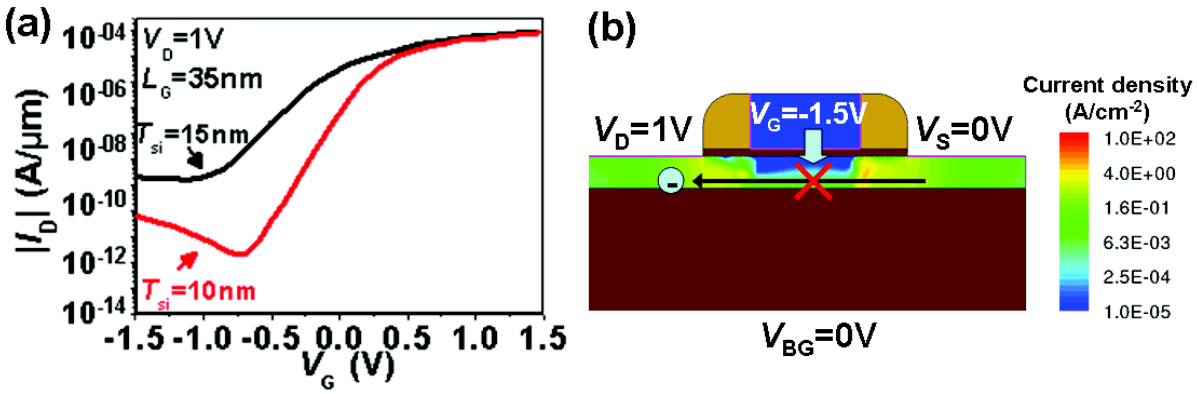

Fig. 6.5: Simulated I_D-V_G curves of the MOSFETs with L_G = 35 nm and different T_{Si} showing that the bipolar effect is suppressed by scaling the T_{Si} to 10 nm. (b) Electron current density obtained in simulation showing that the flow of electrons through the thin 10 nm channel is cut off by V_G.

6.2. A new device: bipolar enhanced tunneling FET (BET-FET)

The bipolar effect amplifies the GIDL current and thus needs to be suppressed in the standard MOSFETs. In TFETs, on the other hand, the same bipolar amplification can be optimized to enhance the tunneling current in TFET. As discussed in chapter 2, the conventional TFET still has I_{ON} much lower than MOSFET even with high-k gate oxide and low bandgap material in the channel. Here, we propose a new combination of a TFET structure with an HBT, to produce a bipolar-enhanced tunneling FET (BET-FET).

The HBT has been widely used for high-frequency current amplification [85]. Previously, a combination of a multi-emitter HBT with an Esaki tunnel diode structure in the emitter-base junction has been demonstrated to operate without a true base contact and provide additional logic functionality [88]. In the BET-FET, the BTBT-generated holes in the reverse biased collector-base junction drive the base-emitter junction and cause high electron injection from the emitter. The simulated device shows both high current drive and low subthreshold swing (*SS*) over a wide range of current. We will examine various structural implementations of the BET-FET and simulate its scaling capabilities.

6.2.1. Device structure and simulated performance

As in the FD-SOI MOSFET, our simulations will use the 2D version of the Synopsys Sentaurus TCAD simulator, with the dynamic non-local BTBT tunneling model, Shockley–Read–Hall recombination, doping dependent band-gap narrowing, and electric field and doping-dependent mobility. As discussed in earlier chapters, the tunneling parameters in

the non-local BTBT model are determined by the material properties, such as the tunneling mass and bandgap – we have used the default values for Si and SiGe throughout.

Figure 6.6(a) shows the simulated vertical BET-FET device structure, which is symmetrical and has a short gate close to the source end of the undoped Si region. Analogous vertical device structure has already been implemented in conventional MOSFETs and TFETs [21, 89-90], so the fabrication of this vertical BET-FET should pose no fundamental challenge. Both source and drain are n^+-doped and used as collector and emitter, respectively.

A p^+-type $Si_{1-x}Ge_x$ layer with doping concentration of 2×10^{19} cm^{-3} is placed above the drain and used as the base, albeit without any direct base contact. The structure of n^+-source/p-base/n^+-drain forms a heterojunction bipolar transistor (HBT). When the source is grounded and drain is negatively biased ($V_D < 0$), the collector-base junction is reverse-biased and the base-emitter junction is forward-biased, similar to a conventional HBT. In the absence of any base current, the emitter-collector current is negligibly small, as in any floating-base bipolar transistor. The BET-FET is turned on when a tunneling base current is produced in the reverse-biased collector-base junction under the influence of the negative gate bias $V_G < 0$, see Fig. 6.6(a). In order to maximize this tunneling base current, we assume an aggressive but realistic 1 nm equivalent oxide thickness between the gate and the collector (achievable using high-k sidewall gate dielectric [20]), as well as the insertion of a 10 nm $Si_{1-x}Ge_x$ tunneling layer (partially doped n^+) between the n^+-Si collector and the undoped 40 nm Si buffer layer above the $Si_{1-x}Ge_x$ base. It should be noted that total thickness of the two $Si_{1-x}Ge_x$ layers is under 30 nm, permitting the use of fairly high Ge content $x = 0.3$ without exceeding the critical thickness imposed by lattice mismatch [42].

In contrast with the BET-FET, where the internal collector-base junction is directly used as field-effect controlled tunneling junction to drive the HBT, the multi-emitter device developed previously by [88] uses an Esaki tunneling diode formed by an extra-heavily-doped emitter-base junction, see Fig. 6.6(b). Moreover, the device [88] was proposed for enhanced logic functionality and simplified fabrication, but did not consider sharp-switching applications.

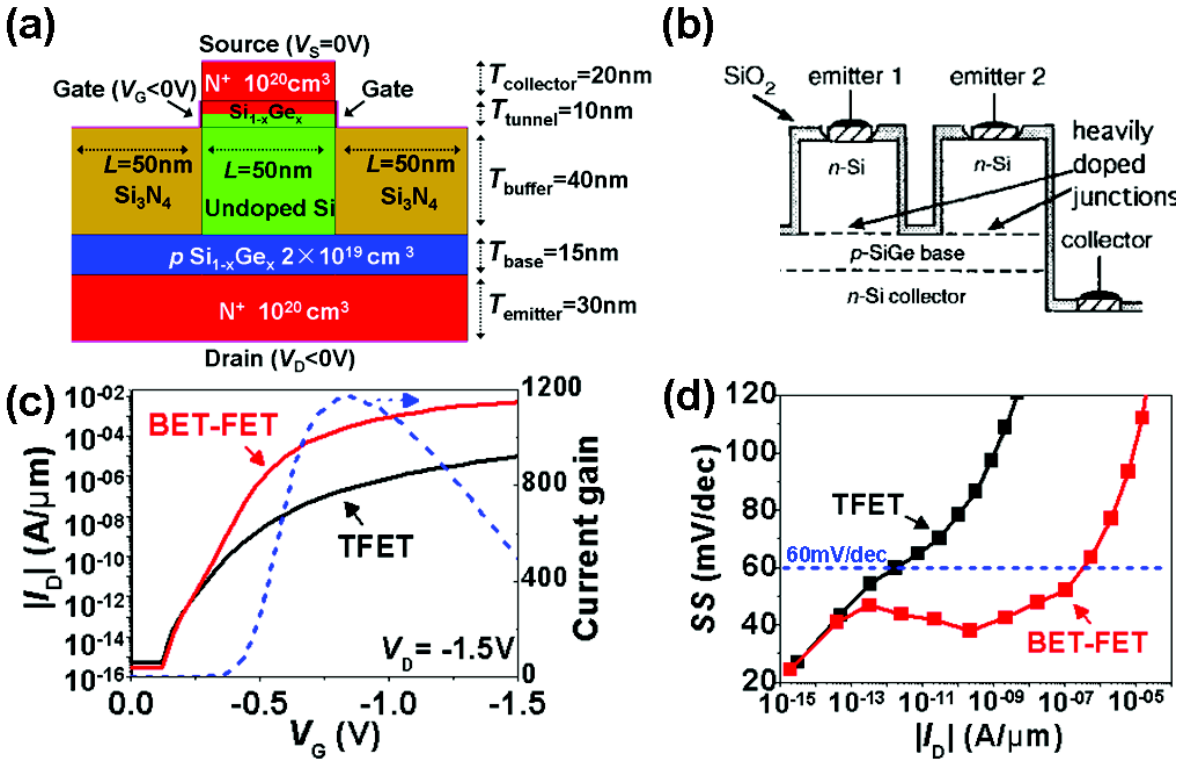

Fig. 6.6: (a) The simulated vertical BET-FET device structure with following parameters: n^+-doped Si collector (source) of thickness T_{coll} = 20 nm; $Si_{1-x}Ge_x$ tunneling layer of T_{tun} = 10 nm thickness, with 5 nm doped n^+ and the other 5 nm undoped; undoped Si buffer layer of T_{buf} = 40 nm thickness; p^+-doped $Si_{1-x}Ge_x$ base of T_{base} = 15 nm thickness; and 30 nm thick n^+-doped Si emitter (drain). The width of the collector stripe is L = 50 nm. (b) Schematic view of the multi-emitter device combining an emitter-base Esaki diode and HBT for enhanced logic functionality, previously developed in [88] . Comparisons of (c) current and (d) subthreshold swing (SS) between the BET-FET and a conventional TFET with the same structure but a p^+-doped drain shows the higher performance of the BET-FET. The dashed line in (c) shows the current gain provided by the BET-FET over the TFET, whereas the dashed line in (d) denotes the SS = 60 mV/decade limit of conventional FETs.

Figure 6.6(c) shows the I_D-V_G characteristics of the BET-FET at V_D = –1.5 V with Ge content x = 0.3 in both base and tunneling layer. The gate workfunction was set at 5 eV in order to reduce the threshold voltage. For comparison, a conventional vertical TFET with the same tunnel layer structure as in Fig. 6.6(a) but a p^+-Si doped drain was also simulated. The undoped buffer layer, while not essential in a conventional TFET, is helpful in reducing ambipolar leakage without degrading the gate-controlled tunneling I_{ON}, as discussed in detail in Chapter 2. As a result, the dominant difference between the BET-FET and a similar vertical TFET is the bipolar amplification.

We find that compared to the vertical TFET, the BET-FET has much higher $I_{ON} > 4\times10^3$ μA/μm at $V_G = -1.5$ V. The bipolar current gain of BET-FET, referenced to the TFET, is low under low I_D due to carrier recombination in the base-emitter junction, and ramps up rapidly as I_D increases. The highest current gain is achieved at $I_D \sim 10^2$ μA/μm and then decreases due to high electron injection, as in a standard HBT [3]. Figure 6.6(d) compares the *SS* in BET-FET and TFET, where the *SS* < 60 mV/decade in the vertical TFET is only obtained at low I_D and only over two decades of current, whereas the BET-FET maintains an *SS* < 60 mV/decade over seven decades of current, thanks to the bipolar current gain.

6.2.2. Operation principle and scaling capability of the BET-FET

The BET-FET uses the tunneling-generated holes as the base current (I_p) to drive the bipolar transistor and obtain an amplified electron current (I_n), see the equivalent circuit in Fig. 6.7(a) comprising the bipolar transistor and the tunneling diode at the collector. The band-to-band tunneling gap at the reverse-biased collector junction is largely reduced at high $|V_G|$, and thus holes are generated in the tunneling layer underneath the gates. The tunneling-generated holes flow to the base and forward-bias the base-emitter junction, see Fig. 6.7(b), resulting in electron injection from the emitter into the base, as in a standard HBT. The injected electrons then drift to the collector, as illustrated in Fig. 6.7(c). Thanks to the high emitter efficiency of $Si/Si_{1-x}Ge_x$ emitter-base heterojunction and the narrow $Si_{1-x}Ge_x$ base, the current gain due to bipolar amplification is large.

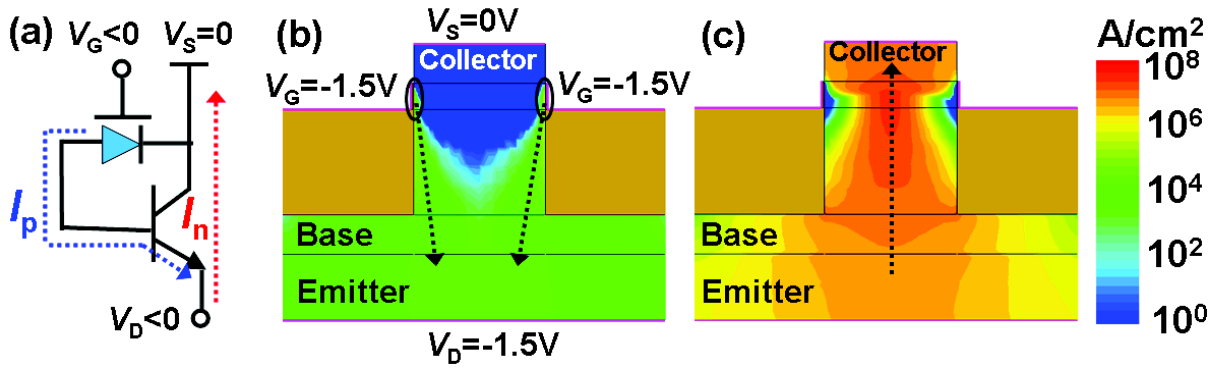

Fig. 6.7: (a) Equivalent circuit of the BET-FET showing the combination of bipolar transistor and gate-controlled tunneling diode. (b) Hole and (c) electron current density in the BET-FET with the collector stripe L = 50 nm. The dashed arrows indicate the flow of holes and electrons, which are spatially separated.

We have investigated the scaling capability of the BET-FET by reducing the layout dimension (width of the collector stripe) L from 50 nm to 10 nm in our simulations. With L

= 10 nm, the threshold voltage is markedly reduced due to the enhancement of electric field at tunneling junction, similar to [2], see Fig. 6.8(a). Unfortunately, the current at high $|V_G|$ is also markedly reduced for the following reason: the same large negative V_G that promotes interband tunneling and increases I_p also suppresses the electron flow I_n from the emitter to the collector – compare Fig. 6.7(b) for a wide L = 50 nm to Fig. 6.8(b) for L = 10 nm. In order to restore the electron flow, we envisage a BET-FET with two independent, individually biased gates, simulated with V_{G2} = 1.5 V in Fig. 6.8. The threshold voltage is increased due to the interchannel coupling effect. The high electron current is restored at high $|V_G|$, thanks to the positive V_{G2} restoring the electron flow, see Fig. 6.8(c). Thus, provided independent gate biasing is an option, the BET-FET can be scaled down to 10 nm.

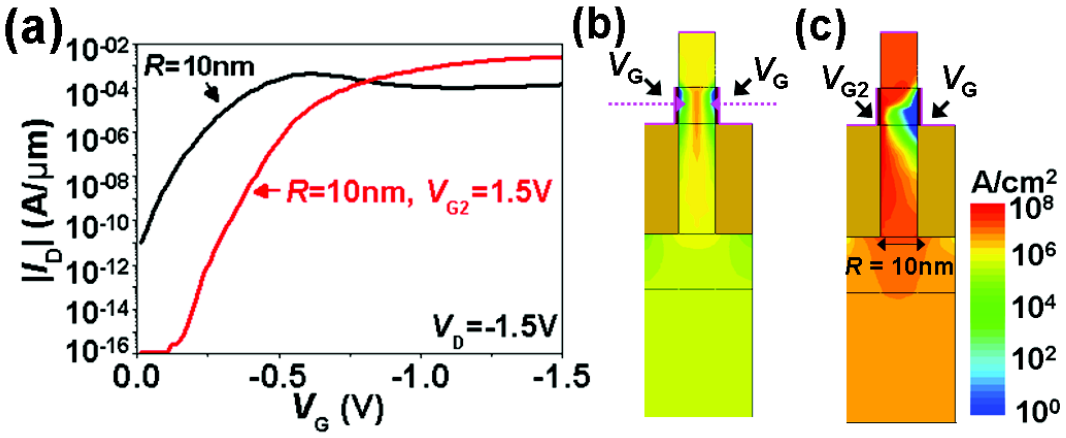

Fig. 6.8: (a) Comparison of I_D-V_G between scaled BET-FETs with a common gate biased at V_G and two independent gates, where one is biased at V_G and the other kept at a fixed V_{G2} = 1.5 V. The electron current density in the (b) double-gate and (c) independent gate devices.

6.2.3. Variants

A variant of the BET-FET with an asymmetrical structure is shown in Fig. 6.9(a). Here the HBT is separated from the tunneling junction and placed at the drain side. The tunneling layer is placed under the gate and adjacent to the *p*-doped base. The simulated I_D-V_G curves show similarly good performance to the vertical BET-FET, see Fig. 6.9(b). The electron and hole flows are indicated in Fig. 6.9(c) and (d). Since the bipolar current flows in a different channel separated spatially from the tunneling current, it is not restricted by the gate voltage and thus enables better scaling capability than the vertical version. Moreover, this variant may be more compact than the vertical device, as there is not need to form an extended contact

region for the buried drain. On the other hand, the fabrication of this structure is more challenging due to its asymmetrical form, with SiGe epitaxy required on one side of the gate.

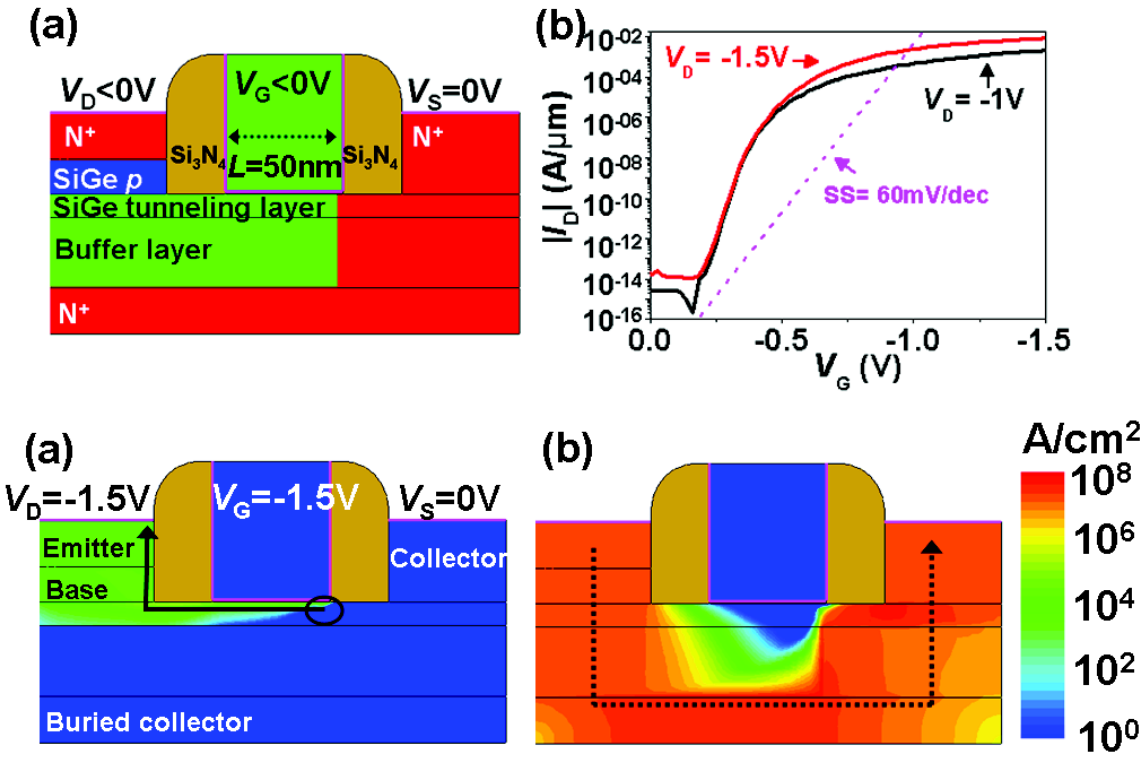

Fig. 6.9: (a) A variation of BET-FET with asymmetrical and planar structure. (b) I_D-V_G simulations showing high performance with various drain voltages. (c) Hole and (b) electron current density. The solid and dashed curves indicate the hole and electron current flows, respectively. The device dimensions are L = 50 nm, T_{coll} = 35 nm, T_{emit} = 20 nm, T_{buf} = 40 nm, buried collector T_{Bcoll} = 20 nm, $Si_{1-x}Ge_x$ base and tunneling layers of T_{base} = 15 nm and T_{tun} = 10 nm thickness, respectively.

Another variant is shown in Fig. 6.10, where the device is symmetrical and the layout is similar to a MOSFET, easing the fabrication. Two electrodes on both side of gate are tied together and used as the source and the tunneling is located at the source junctions under the gate. Figure 6.10(b) shows the performance of this device with low *SS* and high I_{ON}. Figure 6.10(c) and (d) show its hole and electron flow, respectively. It should be noted that as L is downscaled, the symmetrical vertical structure of Fig. 6.10 would suffer from the same restriction on carrier flow as the device in Fig. 6.7 – independent biasing of the two collector electrodes analogous to Fig. 6.8(c) can overcome this problem.

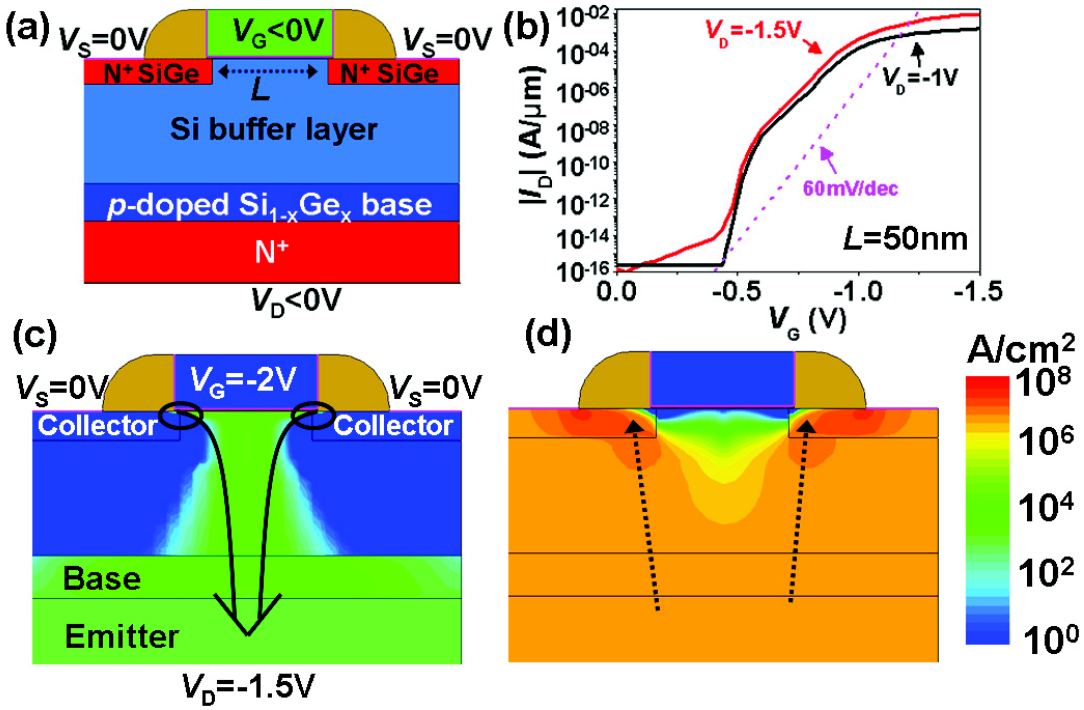

Fig. 6.10: (a) A symmetrical BET-FET variant with a MOSFET-like layout. (b) I_D-V_G simulations at V_D = –1 and –1.5 V. (c) Hole and (d) electron current densities at V_D = –1.5 V and V_G = –2 V. The solid and dashed curves indicate the hole and electron current flows, respectively. The device dimensions are L = 50 nm, $Si_{1-x}Ge_x$ tunneling layer (collector) with T_{coll} = 10 nm, $Si_{1-x}Ge_x$ base T_{base} = 15 nm, T_{emit} = 30 nm and T_{buf} = 40 nm.

6.2.4. Discussion

The performance of BET-FET is determined by both the bipolar current gain and tunneling current, affected by the Ge content x in base and tunneling layers, respectively. Figure 6.11(a) shows that the increase of x from 0 to 0.3 in the base enhances the current gain and hence the I_{ON} of the vertical BET-FET with L = 50 nm (Fig. 6.6(a)). The increase of Ge content in the tunneling layer increases the tunneling current and reduces the threshold voltage, thanks to the decrease of bandgap, see Fig. 6.11(b).

Figure 6.12 compares the I_D-V_D characteristics between the BET-FET and conventional TFET showing that the I_D in the BET-FET degrades as $|V_D|$ decreases below 1 V. The current is low at $|V_D| < 0.5$ V. This is due to the fact that the $|V_D|$ in BET-FET needs to be high enough to drive both the reverse-biased tunneling junction and the forward-biased base-emitter bipolar junction. One way to partially address this issue is to use III-V materials, which have a lower band-gap, and thus a lower operation voltage [91].

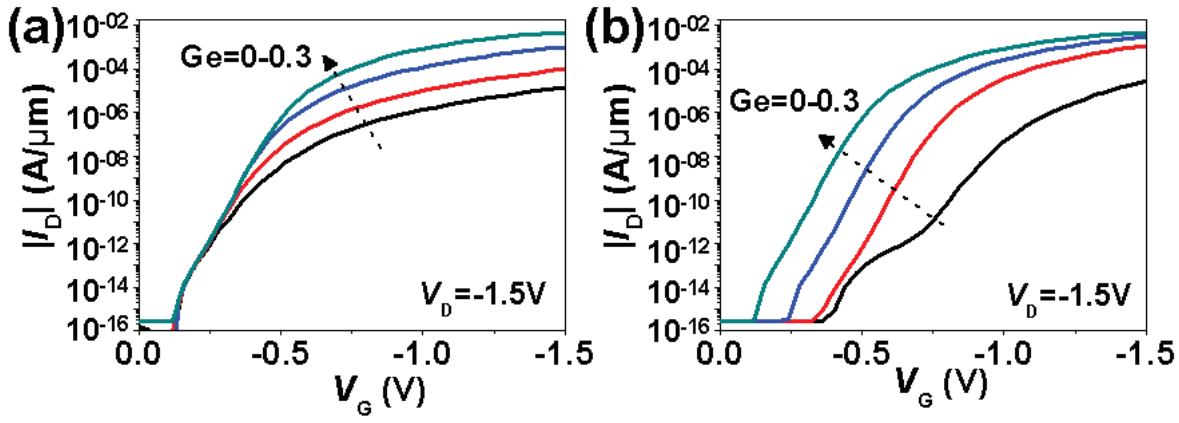

Fig. 6.11: I_D-V_G of BET-FETs with various Ge content in (a) the base (with x = 0.3 in the tunneling layer) and (b) tunneling layer (with x = 0.3 in the base).

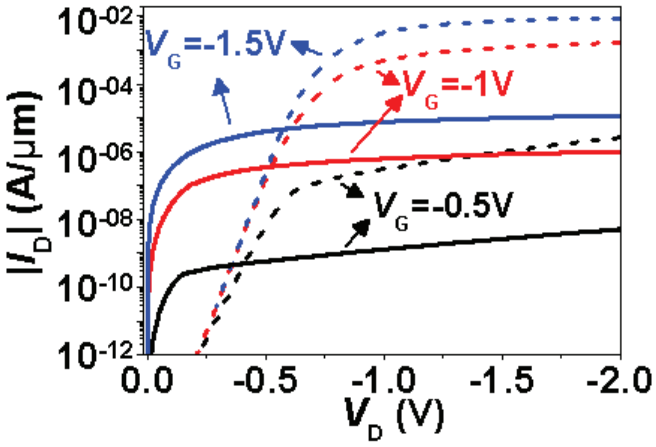

Fig. 6.12: Comparison of I_D-V_D characteristics between vertical BET-FET (dashed curves) and conventional TFET (solid curves) with L = 50 nm showing that the BET-FET has lower current at low $|V_D|$, but significantly higher current when $|V_D|$ exceeds the ~0.6 V forward turn-on voltage of a Si diode.

6.3. Conclusion

The GIDL current in FD-SOI MOSFETs with channel length down to 35 nm has been studied experimentally, showing large enhancement and variability compared to the long-channel devices. The increased GIDL has been understood, via TCAD simulation, to arise from the flow of tunneling-generated holes in drain junction to the source, where they are amplified by the injection of electrons in the source/channel junction. We have also shown how this excess GIDL can be suppressed in FD-SOI MOSFETs by using backgate bias or a thin channel, essentially by cutting off the electron flow channel.

Interestingly, the same bipolar amplification responsible for the increased GIDL in MOSFETs can be used to increase the I_{ON} in TFETs by integrating an HBT structure into the TFET. The result is a new bipolar-enhanced TFET (BET-FET), which we have demonstrated in simulation to offer a high $I_{ON} > 4\times10^{-3}$A/μm and low $SS < 60$mV/dec over many decades of current, significantly outperforming conventional TFETs reported to date. The operation of the BET-FET combines the merits of sharp switching of a TFET with the high current amplification of an HBT. Devices with vertical and planar structures are proposed with the scalability down to 10 nm. Our simulated BET-FETs have employed CMOS-compatible $Si/Si_{1-x}Ge_x$ HBT layers, but similar devices can be envisioned in III-V materials where even lower operating voltages and higher currents may be possible.

Chapter 7: Conclusion and perspectives

7.1. Conclusion

This thesis was originally focused on studying the TFET as a sharp switching device, which is of great interest for low-power applications. In the course of research, the scope of the work broadened significantly, including the invention of two novel devices: the Z^2-FET, demonstrated experimentally and extensively modeled analytically and via TCAD, and the BET-FET, which still awaits experimental demonstration. In its finished form, the thesis now includes:

a. Study of TFETs. In Chapter 2, TFETs with various structures and materials have been fabricated and systematically characterized. A more complete analytical model has been developed in Chapter 3.
b. Invention and study of a new feedback-based sharp-switching device, which we have named the Z^2-FET, as it involves *zero* impact ionization and exhibits *zero* subthreshold swing. The DC characteristics and modeling of Z^2-FET have been studied in Chapter 4, followed by the memory applications in Chapter 5.
c. Study of GIDL current in MOSFETs and its application to TFETs. The GIDL current in short-channel MOSFETs and TFETs has been modeled in Chapter 3. With our new understanding of the bipolar-enhanced GIDL, the operation mechanism of a new device named BET-FET, for bipolar-enhanced TFET is described in Chapter 6.

In detail, this thesis has been structured as follows. The scaling restrictions on standard MOSFETs and the operating principle and state-of-the-art of TFETs and feedback-based sharp-switching devices are reviewed in Chapter 1.

In Chapter 2, TFETs with various structures and materials have been fabricated and systematically characterized. In order to confirm the tunneling mechanism in TFET, we have extended the low frequency noise (LFN) measurement from MOSFETs to TFETs. Unlike the MOSFET, the LFN in TFET is dominated by RTS noise with $1/f^2$ spectrum, indicating that the current is restricted by the small area of the tunneling junction, rather than the entire gate area. The HfO_2 gate oxide and $Si_{0.65}Ge_{0.35}$ channel have been used to replace the SiO_2 gate oxide and Si channel to achieve the I_{ON} of 3 decades higher, thanks to the higher electric field and lower tunneling bandgap, respectively. Asymmetrical TFETs with intrinsic regions

adjacent to the drain have been fabricated to reduce the ambipolar electric field, and thus suppress the leakage current without degrading the I_{ON}.

In Chapter 3, a new TFET model is developed, considering both the tunneling junction and channel transport. An analytical form valid for low tunneling currents has also been obtained and verified against both experimental results and TCAD simulations. This model has been extended to explain the GIDL current in MOSFETs considering both the interband tunneling junction and forward-biased junction in drain and source, respectively.

In Chapter 4, a new device named Z^2-FET, based on asymmetrical TFET structures but with different biasing, is presented and discussed. The Z^2-FET exhibits extremely sharp switching behavior, with $SS < 1$ mV/decade, as well as an excellent I_{ON}/I_{OFF} ratio $> 10^9$. The I_D-V_D characteristics show gate-controlled hysteresis. The device operates via feedback between the electron and hole flows and the corresponding injection barriers, which are controlled by V_G and either V_{BG} or surface charge. The Z^2-FET is scalable down to 20 nm in simulation. Preliminary reliability tests have been performed showing low degradation under long duration stress or high temperature. A model has been developed based on the feedback mechanism, reproducing the experimental results.

Chapter 5 explores the memory applications of the Z^2-FET. The Z^2-FET can be used as a capacitor-less 1-T DRAM with supply voltage down to 1.1 V, retention time up to 5.5 s and nondestructive read property. The logic states are represented by the charges directly stored in front-gate capacitor and read out through the internal feedback amplification. Thanks to smaller stored charge, the access time of Z^2-FET DRAM is as low as 1 ns, demonstrated in simulation. The retention time has been studied in detail, showing dependences on biasing, temperature and device dimensions. An alternative operation of the Z^2-FET DRAM has been demonstrated with the write operation analogous to a conventional 1T-1C DRAM. In addition to DRAM operation, we demonstrate experimentally the functionality of the Z^2-FET in the SRAM mode utilizing the V_G-controlled hysteresis window. The static power consumption in Z^2-FET SRAM can be significantly reduced by combining V_{BG} and surface charge, or by using the $Si/Si_{1-x}Ge_x$ heterojunction between the channel and the source/drain regions.

In Chapter 6, the enhanced GIDL current in short-channel L_G = 35 nm FD-SOI MOSFETs is explained by the bipolar amplification of the tunneling current. This phenomenon is then utilized to conceive a new device named the BET-FET, combining a TFET with a $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistor (HBT). In the BET-FET, the tunneling current is used as base current to drive the HBT, and thus a high bipolar diffusion current is obtained. In simulation, the BET-FET has $I_{ON} > 4\times10^{-3}$ A/μm and low $SS < 60$

mV/dec over 7 decades of current, significantly outperforming conventional TFETs that have been plagued by inadequate I_{ON}.

7.2. Future perspectives

The research described in this thesis naturally leads to several future directions:

a. The BET-FET is a very interesting device with extraordinary predicted performance. So far, this device is only demonstrated in TCAD simulation on $Si/Si_{1-x}Ge_x$ substrate. It would be interesting to extend this work to experiment, since the projected fabrication is compatible with conventional MOSFET process. Moreover, the III-V materials can also be used in this device with the possibility to achieve even lower supply voltage and higher current, thanks to the lower bandgap.

b. For the switching applications (logic circuits) of the Z^2-FET, there are still some issues left. The gate is not able to turn off the device due to the existence of electron-hole plasma in the ON state. This could be possibly solved by utilizing fast V_G pulses to induce a displacement current and expel the plasma out of the channel, rebuilding the potential barriers, similar to turning off a thyristor [92].

c. For Z^2-FET memory applications, the operation of a single cell has been confirmed by both experimental and TCAD simulation. Due to its promising performance, it would be very attractive to demonstrate the operation of a Z^2-FET memory array in future. The difficulty of the array operation would be the selective read and write. Though the selective write has been demonstrated on a single device, the read operation is still not selective and requires further study.

d. So far, the Z^2-FET has been demonstrated for switching and memory applications. There are still other potential applications of this device, such as electrostatic protection (ESD) and sensor, that are worth exploring.

e. The GIDL current and the bipolar-enhanced effect in FD-SOI MOSFETs have been studied. It would be interesting to systematically compare the GIDL in devices built on FD-SOI and PD-SOI substrates. Since the bipolar amplification can be suppressed by scaling the active layer, the FD-SOI MOSFET is probably more attractive compared to PD-SOI device, in terms of reducing the bipolar-enhanced GIDL current.

References

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE,* vol. 86, pp. 82-85, 1998.

[2] D. Leonelli, A. Vandooren, R. Rooyackers, A. S. Verhulst, S. De Gendt, M. M. Heyns, and G. Groeseneken, "Multiple-gate tunneling field effect transistors with sub-60 mV/dec subthreshold slope," in *Proc. Ext. Abstr. SSDM.*, 2009, pp. 767-768.

[3] M. Shur, *Physics of Semiconductor Devices*. Englewood Cliffs, N.J.: Prentice-Hall, Inc. , 1990.

[4] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q," in *Tech. Dig. -Int. Electron Devices Meet.*, 2002, pp. 289-292.

[5] R. Naber, J. Massolt, M. Spijkman, K. Asadi, P. Blom, and D. De Leeuw, "Origin of the drain current bistability in polymer ferroelectric field-effect transistors," *Applied physics letters,* vol. 90, pp. 113509-113509-113503, 2007.

[6] W. Y. Choi, B. G. Park, J. D. Lee, and T. J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *Electron Device Letters, IEEE,* vol. 28, pp. 743-745, 2007.

[7] A. Padilla, C. W. Yeung, C. Shin, C. Hu, and T. J. K. Liu, "Feedback FET: A novel transistor exhibiting steep switching behavior at low bias voltages," in *Tech. Dig. -Int. Electron Devices Meet.*, 2008, pp. 171-174.

[8] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE,* vol. 98, pp. 2095-2110, 2010.

[9] L. Esaki, "New phenomenon in narrow Germanium p-n junctions," *Physical Review,* vol. 109, pp. 603-604, 1958.

[10] G. Hurkx, D. Klaassen, and M. Knuvers, "A new recombination model for device simulation including tunneling," *Electron Devices, IEEE Transactions on,* vol. 39, pp. 331-338, 1992.

[11] H. J. Cho, F. Nemati, R. Roy, R. Gupta, K. Yang, M. Ershov, S. Banna, M. Tarabbia, C. Sailing, and D. Hayes, "A novel capacitor-less DRAM cell using thin capacitively-coupled thyristor (TCCT)," in *Tech. Dig. -Int. Electron Devices Meet.*, 2005, pp. 311-314.

[12] E. O. Kane, "Theory of tunneling," *Journal of Applied Physics,* vol. 32, pp. 83-91, 1961.

[13] C. Sandow, J. Knoch, C. Urban, Q. T. Zhao, and S. Mantl, "Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors," *Solid-State Electronics,* vol. 53, pp. 1126-1129, 2009.

[14] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Scaling the vertical tunnel FET with tunnel bandgap modulation and gate workfunction engineering," *Electron Devices, IEEE Transactions on,* vol. 52, pp. 909-917, 2005.

[15] R. Jhaveri, V. Nagavarapu, and J. C. S. Woo, "Effect of Pocket Doping and Annealing Schemes on the Source-Pocket Tunnel Field-Effect Transistor," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 80-86, 2011.

[16] J. Colinge, "Multi-gate SOI MOSFETs," *Microelectronic engineering,* vol. 84, pp. 2071-2076, 2007.

[17] M. Björk, J. Knoch, H. Schmid, H. Riel, and W. Riess, "Silicon nanowire tunneling field-effect transistors," *Applied physics letters,* vol. 92, p. 193504, 2008.

[18] F. Mayer, C. Le Royer, J. F. Damlencourt, K. Romanjek, F. Andrieu, C. Tabone, B. Previtali, and S. Deleonibus, "Impact of SOI, Si1-xGexOI and GeOI substrates on

CMOS compatible Tunnel FET performance," in *Tech. Dig. -Int. Electron Devices Meet.*, 2008, pp. 163-167.

[19] D. Kazazis, P. Jannaty, A. Zaslavsky, C. Le Royer, C. Tabone, L. Clavelier, and S. Cristoloveanu, "Tunneling field-effect transistor with epitaxial junction in thin germanium-on-insulator," *Applied physics letters,* vol. 94, p. 263508, 2009.

[20] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and≪ 60mV/dec subthreshold slope," in *Tech. Dig. -Int. Electron Devices Meet.*, 2008, pp. 947-949.

[21] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, and A. Liu, "Experimental demonstration of 100nm channel length In0. 53Ga0. 47As-based vertical inter-band tunnel field effect transistors (TFETs) for ultra low-power logic and SRAM applications," in *Tech. Dig. -Int. Electron Devices Meet.*, 2009, pp. 949-951.

[22] G. Dewey, B. Chu-Kung, J. Boardman, J. Fastenau, J. Kavalieros, R. Kotlyar, W. Liu, D. Lubyshev, M. Metz, and N. Mukherjee, "Fabrication, characterization, and physics of III–V heterojunction tunneling Field Effect Transistors (H-TFET) for steep sub-threshold swing," in *Tech. Dig. -Int. Electron Devices Meet.*, 2011, pp. 33.36. 31-33.36. 34.

[23] C. H. Jan, M. Agostinelli, M. Buehler, Z. P. Chen, S. J. Choi, G. Curello, H. Deshpande, S. Gannavaram, W. Hafez, and U. Jalan, "A 32nm SoC platform technology with 2nd generation high-k/metal gate transistors optimized for ultra low power, high performance, and high density product applications," in *Tech. Dig. -Int. Electron Devices Meet.*, 2009, pp. 758-761.

[24] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *Electron Device Letters, IEEE,* vol. 29, pp. 1344-1346, 2008.

[25] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Influence of phonon scattering on the performance of pin band-to-band tunneling transistors," *Applied physics letters,* vol. 92, p. 043125, 2008.

[26] S. Luryi and A. Zaslavsky, "Nonclassical devices in SOI: Genuine or copyright from III-V," *Solid-State Electronics,* vol. 51, pp. 212-218, 2007.

[27] F. Nemati, H. J. Cho, S. Robins, R. Gupta, M. Tarabbia, K. J. Yang, D. Hayes, and V. Gopalakrishnan, "Fully planar 0.562μm2 T-RAM cell in a 130nm SOI CMOS logic technology for high-density high-performance SRAMs," in *Tech. Dig. -Int. Electron Devices Meet.*, 2004, pp. 273-276.

[28] R. Gupta, F. Nemati, S. Robins, K. Yang, V. Gopalakrishnan, J. Sundarraj, R. Chopra, R. Roy, H. J. Cho, and W. Maszara, "32nm high-density high-speed T-RAM embedded memory technology," in *Tech. Dig. -Int. Electron Devices Meet.*, 2010, pp. 12.11.11-12.11.14.

[29] K. Yang, R. Gupta, S. Banna, F. Nemati, H. J. Cho, M. Ershov, M. Tarabbia, D. Hayes, and S. Robins, "Optimization of Nanoscale Thyristors on SOI for High-Performance High-Density Memories," in *Intern. SOI Conf.*, 2006, pp. 113-114.

[30] C. W. Yeung, A. Padilla, T. J. K. Liu, and C. Hu, "Programming characteristics of the steep turn-on/off feedback FET (FBFET)," in *Tech. Dig. -Symp. VLSI Technol.*, 2009, pp. 176-177.

[31] A. A. Salman, S. G. Beebe, M. Emam, M. M. Pelella, and D. E. Ioannou, "Field effect diode (FED): a novel device for ESD protection in deep sub-micron SOI technologies," in *Tech. Dig. -Int. Electron Devices Meet.*, 2006, pp. 107-111.

[32] Y. Yang, A. Gangopadhyay, Q. Li, and D. E. Ioannou, "Scaling of the SOI field effect diode (FED) for memory application," in *Intern. Semicond. Dev. Res. Symp.*, 2009, pp. 1-2.
[33] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunneling FETs on SOI: Suppression of ambipolar leakage, low-frequency noise behavior, and modeling," *Solid-State Electronics,* vol. 65-66, pp. 226-233, 2011.
[34] S. R. Li, Y. L. R. Lu, W. McMahon, Y. H. Lee, and N. Mielke, "RTS and 1/f noise in Flash memory," in *Tech. Dig. -Symposium on VLSI Technology.*, 2007, pp. 1-2.
[35] P. Fantini, G. Betti Beneventi, A. Calderoni, L. Larcher, P. Pavan, and F. Pellizzer, "Characterization and modelling of low-frequency noise in PCM devices," in *Tech. Dig. -Int. Electron Devices Meet.*, 2008, pp. 1-4.
[36] J. Zhuge, R. Wang, R. Huang, Y. Tian, L. Zhang, D. W. Kim, D. Park, and Y. Wang, "Investigation of low-frequency noise in silicon nanowire MOSFETs," *Electron Device Letters, IEEE,* vol. 30, pp. 57-60, 2009.
[37] Y. Xu, T. Minari, K. Tsukagoshi, R. Gwoziecki, R. Coppard, F. Balestra, J. Chroboczek, and G. Ghibaudo, "Extraction of low-frequency noise in contact resistance of organic field-effect transistors," *Applied physics letters,* vol. 97, pp. 033503-033503-033503, 2010.
[38] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Low-frequency noise behavior of tunneling field effect transistors," *Applied physics letters,* vol. 97, pp. 243503-243503-243503, 2010.
[39] C. Aydin, A. Zaslavsky, S. Luryi, S. Cristoloveanu, D. Mariolle, D. Fraboulet, and S. Deleonibus, "Lateral interband tunneling transistor in silicon-on-insulator," *Applied physics letters,* vol. 84, p. 1780, 2004.
[40] S. H. Kim, H. Kam, C. Hu, and T. J. K. Liu, "Germanium-source tunnel field effect transistors with record high ION/IOFF," in *Tech. Dig. -Symp. VLSI Technology*, 2009, pp. 178-179.
[41] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Tunnel field-effect transistor without gate-drain overlap," *Applied physics letters,* vol. 91, p. 053102, 2007.
[42] L. Hutin, M. Cassé, C. Le Royer, J. F. Damlencourt, A. Pouydebasque, C. Xu, C. Tabone, J. M. Hartmann, V. Carron, and H. Grampeix, "20nm gate length trigate pFETs on strained SGOI for high performance CMOS," in *Tech. Dig. -Symp. VLSI Technology*, 2010, pp. 37-38.
[43] S. Nakaharai, T. Tezuka, N. Hirashita, E. Toyoda, Y. Moriyama, N. Sugiyama, and S. Takagi, "Formation process of high-purity Ge-on-insulator layers by Ge-condensation technique," *Journal of Applied Physics,* vol. 105, pp. 024515-024515-024518, 2009.
[44] E. H. Toh, G. H. Wang, G. Samudra, and Y. C. Yeo, "Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization," *Applied physics letters,* vol. 90, pp. 263507-263507-263503, 2007.
[45] M. Schlosser, K. K. Bhuwalka, M. Sauter, T. Zilbauer, T. Sulima, and I. Eisele, "Fringing-Induced Drain Current Improvement in the Tunnel Field-Effect Transistor With High-$ kappa $ Gate Dielectrics," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 100-108, 2009.
[46] Y. Gao, T. Low, and M. Lundstrom, "Possibilities for VDD= 0.1 V logic using carbon-based tunneling field effect transistors," in *Tech. Dig. Symp. VLSI Technol.*, 2009, pp. 180-181.
[47] C. Shen, S. L. Ong, C. H. Heng, G. Samudra, and Y. C. Yeo, "A Variational Approach to the Two-Dimensional Nonlinear Poisson's Equation for the Modeling of Tunneling Transistors," *Electron Device Letters, IEEE,* vol. 29, pp. 1252-1255, 2008.

[48] V. Dobrovolsky, V. Rossokhaty, and S. Cristoloveanu, "CONTUNT: Thin SOI control tunneling transistor," *Solid-State Electronics,* vol. 50, pp. 754-757, 2006.
[49] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, "Boosting the on-current of a n-channel nanowire tunnel field-effect transistor by source material optimization," *Journal of Applied Physics,* vol. 104, pp. 064514-064514-064510, 2008.
[50] A. S. Verhulst, B. Sorée, D. Leonelli, W. G. Vandenberghe, and G. Groeseneken, "Modeling the single-gate, double-gate, and gate-all-around tunnel field-effect transistor," *Journal of Applied Physics,* vol. 107, p. 024518, 2010.
[51] M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, "Pseudo-Two-Dimensional Model for Double-Gate Tunnel FETs Considering the Junctions Depletion Regions," *Electron Devices, IEEE Transactions on,* vol. 57, pp. 827-834, 2010.
[52] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A tunneling field effect transistor model combining interband tunneling with channel transport," *Journal of Applied Physics,* vol. 110, pp. 104503-104503-104507, 2011.
[53] P. M. Solomon, J. Jopling, D. J. Frank, C. D'Emic, O. Dokumaci, P. Ronsheim, and W. Haensch, "Universal tunneling behavior in technologically relevant P/N junction diodes," *Journal of Applied Physics,* vol. 95, p. 5800, 2004.
[54] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," *Electron Devices, IEEE Transactions on,* vol. 36, pp. 399-402, 1989.
[55] S. Cristoloveanu and S. S. Li, *Electrical characterization of silicon-on-insulator materials and devices*. Norwell, MA: Kluwer, 1995.
[56] J. P. Colinge, "Multiple-gate soi mosfets," *Solid-State Electronics,* vol. 48, pp. 897-905, 2004.
[57] C. P. Auth and J. D. Plummer, "A simple model for threshold voltage of surrounding-gate MOSFET's," *Electron Devices, IEEE Transactions on,* vol. 45, pp. 2381-2383, 1998.
[58] C. W. Lee, S. R. N. Yun, C. G. Yu, J. T. Park, and J. P. Colinge, "Device design guidelines for nano-scale MuGFETs," *Solid-State Electronics,* vol. 51, pp. 505-510, 2007.
[59] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *Electron Device Letters, IEEE,* vol. 27, pp. 297-300, 2006.
[60] T. Chan, J. Chen, P. Ko, and C. Hu, "The impact of gate-induced drain leakage current on MOSFET scaling," in *Tech. Dig. -Int. Electron Devices Meet.*, 1987, pp. 718-721.
[61] L. Huang, P. Lai, J. Xu, and Y. Cheng, "Mechanism analysis of gate-induced drain leakage in off-state n-MOSFET," *Microelectronics and reliability,* vol. 38, pp. 1425-1431, 1998.
[62] J. H. Chen, S. C. Wong, and Y. H. Wang, "An analytic three-terminal band-to-band tunneling model on GIDL in MOSFET," *Electron Devices, IEEE Transactions on,* vol. 48, pp. 1400-1405, 2001.
[63] L. Lopez, P. Masson, D. Née, and R. Bouchakour, "Temperature and drain voltage dependence of gate-induced drain leakage," *Microelectronic engineering,* vol. 72, pp. 101-105, 2004.
[64] S. L. Jang and H. H. Lin, "Modeling of drain leakage current in SOI pMOSFETs," *Solid-State Electronics,* vol. 43, pp. 2147-2154, 1999.
[65] Y. K. Choi, D. Ha, T. J. King, and J. Bokor, "Investigation of gate-induced drain leakage (GIDL) current in thin body devices: single-gate ultra-thin body, symmetrical double-gate, and asymmetrical double-gate MOSFETs," *JAPANESE JOURNAL OF APPLIED PHYSICS PART 1 REGULAR PAPERS SHORT NOTES AND REVIEW PAPERS,* vol. 42, pp. 2073-2076, 2003.

[66] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Gate-induced drain leakage in FD-SOI devices: What the TFET teaches us about the MOSFET," *Microelectronic engineering,* 2011.
[67] J. B. McKITTERICK and A. L. Caviglia, "An analytic model for thin SOI transistors," *Electron Devices, IEEE Transactions on,* vol. 36, pp. 1133-1138, 1989.
[68] V. A. K. Temple, "MOS-controlled thyristors—A new class of power devices," *Electron Devices, IEEE Transactions on,* vol. 33, pp. 1609-1618, 1986.
[69] C. Ronsisvalle, V. Enea, C. Abbate, G. Busatto, and A. Sanseverino, "Perspective Performances of MOS-Gated GTO in High-Power Applications," *Electron Devices, IEEE Transactions on,* vol. 57, pp. 2339-2343, 2010.
[70] U. E. Avci, D. L. Kencke, and P. L. D. Chang, "Floating-Body Diode—A Novel DRAM Device," *Electron Device Letters, IEEE,* vol. 33, pp. 161-163, 2012.
[71] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration," *Electron Device Letters, IEEE,* vol. 33, pp. 179-181, 2012.
[72] F. Mayer, C. Le Royer, G. Le Carval, C. Tabone, L. Clavelier, and S. Deleonibus, "Co-integration of 2 mV/dec subthreshold slope impact ionization MOS (I-MOS) with CMOS," in *The 36th European Solid-State Device Research Conference. ESSDERC 2006.* , 2006, pp. 303-306.
[73] C. Fenouillet-Beranger, S. Denorme, P. Perreau, C. Buj, O. Faynot, F. Andrieu, L. Tosti, S. Barnola, T. Salvetat, and X. Garros, "FDSOI devices with thin BOX and ground plane integration for 32 nm node and below," *Solid-State Electronics,* vol. 53, pp. 730-734, 2009.
[74] M. Vinet, T. Poiroux, J. Widiez, J. Lolivier, B. Previtali, C. Vizioz, B. Guillaumot, Y. Le Tiec, P. Besson, and B. Biasse, "Bonded planar double-metal-gate NMOS transistors down to 10 nm," *Electron Device Letters, IEEE,* vol. 26, pp. 317-319, 2005.
[75] E. Yang, "Turn-off characteristics of pnpn devices," *Solid-State Electronics,* vol. 10, pp. 927-933, 1967.
[76] K. W. Song, J. Y. Kim, H. Kim, H. W. Chung, K. Kim, H. W. Park, H. C. Kang, S. Kim, and N. Tak, "A 31ns random cycle VCAT-based 4F2 DRAM with enhanced cell efficiency," in *Proc. Symp. VLSI Circuits*, 2009, pp. 132-133.
[77] W. Mueller, G. Aichmayr, W. Bergner, E. Erben, T. Hecht, C. Kapteyn, A. Kersch, S. Kudelka, F. Lau, and J. Luetzen, "Challenges for the DRAM Cell Scaling to 40nm," in *Tech. Dig. -Int. Electron Devices Meet.*, 2005, pp. 336-339.
[78] M. Bawedin, S. Cristoloveanu, and D. Flandre, "A capacitorless 1T-DRAM on SOI based on dynamic coupling and double-gate operation," *Electron Device Letters, IEEE,* vol. 29, pp. 795-798, 2008.
[79] E. Yoshida and T. Tanaka, "A capacitorless 1T-DRAM technology using gate-induced drain-leakage (GIDL) current for low-power and high-speed embedded memory," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 692-697, 2006.
[80] S. Cristoloveanu and M. Bawedin, "From SOI 1T-DRAMs to Unified Memory Concepts," in *MRS Symposium Proceedings*, 2012.
[81] M. Bawedin, S. Cristoloveanu, S. Banna, and D. Flandre, "Novel Capacitor-Less IT-DRAM Using MSD Effect," in *Intern. SOI Conf.*, 2006, pp. 125-126.
[82] S. Eminente, S. Cristoloveanu, R. Clerc, A. Ohata, and G. Ghibaudo, "Ultra-thin fully-depleted SOI MOSFETs: Special charge properties and coupling effects," *Solid-State Electronics,* vol. 51, pp. 239-244, 2007.
[83] N. Rodriguez, F. Gamiz, and S. Cristoloveanu, "A-RAM MemoryCell: Concept and Operation," *Electron Device Letters, IEEE,* vol. 31, pp. 972-974, 2010.

[84] T. Hamamoto and T. Ohsawa, "Overview and future challenges of floating body RAM (FBRAM) technology for 32 nm technology node and beyond," *Solid-State Electronics,* vol. 53, pp. 676-683, 2009.
[85] R. Krithivasan, Y. Lu, J. D. Cressler, J. S. Rieh, M. H. Khater, D. Ahlgren, and G. Freeman, "Half-terahertz operation of SiGe HBTs," *Electron Device Letters, IEEE,* vol. 27, pp. 567-569, 2006.
[86] "Sentaurus," 2011.09.
[87] S. A. Park, J. E. Moon, H.-J. C. Wann, P. K. Ko, and C. Hu, "Design for suppression of gate-induced drain leakage in LDD MOSFET's using a quasi-two-dimensional analytical model," *Electron Devices, IEEE Transactions on,* vol. 39, pp. 1694-1703, 1992.
[88] A. Zaslavsky, S. Luryi, C. King, and R. Johnson, "Multi-emitter Si/GexSi1-x heterojunction bipolar transistor with no base contact and enhanced logic functionality," *Electron Device Letters, IEEE,* vol. 18, pp. 453-455, 1997.
[89] B. Yang, K. Buddharaju, S. Teo, N. Singh, G. Lo, and D. Kwong, "Vertical silicon-nanowire formation and gate-all-around MOSFET," *Electron Device Letters, IEEE,* vol. 29, pp. 791-794, 2008.
[90] Z. Chen, H. Yu, N. Singh, N. Shen, R. Sayanthan, G. Lo, and D. L. Kwong, "Demonstration of tunneling FETs based on highly scalable vertical silicon nanowires," *Electron Device Letters, IEEE,* vol. 30, pp. 754-756, 2009.
[91] T. Oka, T. Mishima, and K. Makoto, "Low turn-on voltage GaAs heterojunction bipolar transistors with a pseudomorphic GaAsSb base," *Applied Physics Letters,* vol. 78, p. 483, 2001.
[92] Q. Huang and Amaratunga.GA.J., "Thyristor turn off using MOS controlled current interruption," *Solid-State Electronics,* vol. 36, pp. 361-371, 1993.

Publications

Patents

[1] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Transistor à effet de champ à pente sous le seuil réduite", French patent. Application No: FR1102747, Sep. 2011.

[2] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Cellule mémoire dynamique munie d'un transistor à effet de champs à pente sous le seuil verticale", French patent. Application No: FR11/03232, Oct. 2011.

[3] J. Wan, S. Cristoloveanu, C. Le Royer and A. Zaslavsky, "Bipolar-enhanced tunneling FET (BET-FET)", French patent, In preparation.

Journal papers

[1] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A systematic study of the sharp-switching Z^2-FET device: from mechanism to modeling and applications", submitted to *Solid-State Electronics.*

[2] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A feedback silicon-on-insulator steep switching device with gate-controlled carrier injection", to be published in *Solid-State Electronics,* 2012.

[3] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A Compact Capacitor-Less High-Speed DRAM Using Field Effect-Controlled Charge Regeneration", *Electron Device Letters, IEEE,* vol. 33, pp. 179-180, 2012.

[4] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "A tunneling field effect transistor model combining interband tunneling with channel transport", *Journal of Applied Physics,* vol. 110, 104503, 2011.

[5] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Gate-Induced Drain Leakage in FD-SOI devices: What the TFET teaches us about the MOSFET", *Microelectronic Engineering,* vol. 88, pp. 1301-1304, 2011.

[6] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Tunneling FETs on SOI: Suppression of Ambipolar Leakage, Low-Frequency Noise Behavior, and Modeling", *Solid-State Electronics*, vol. 65-66, pp. 226-233, 2011.

[7] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Low-frequency noise behavior of tunneling field effect transistors", *Applied Physics Letters,* vol. 97, 243503, 2010.

Conference papers

[1] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "1-Transitor High-Speed DRAM Using Feedback Device", submitted to *Proc. Eur. Solid-State Device Res. Conf (ESSDERC)*, 2012.

[2] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Z^2-FET: A zero-slope switching device with gate-controlled hysteresis", in: *Proc. VLSI-TSA Int. Symp.*, 2012.

[3] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "Z^2-FET: A sharp switching device with gate-controlled hysteresis", in: *EuroSOI*, 2012. (***Best paper award***).

[4] J. Wan, C. Le Royer, A. Zaslavsky, and S. Cristoloveanu, "SOI TFETs: Suppresion of ambipolar leakage and low-frequency noise behavior", in: *Proc. Eur. Solid-State Device Res. Conf (ESSDERC)*, 2010, pp. 341-344.

[5] A. Zaslavsky, J. Wan, S.T. Le, P. Jannaty, S.A. Ddyeh, C. Le Royer, S. Cristoloveanu and S.T. Picraux "Abrupt switching devices : from tunneling to positive feedback.", International Advanced Workshop on 'Frontiers in Electronics' (WOFE'2011), Invited paper.

[6] K–I. Na, W. Van Den Daele, L. Pham–Nguyen, M. Bawedin, K–H. Park, J. Wan, K. Tacchi, S–J. Chang, I. Ionica, Y–H. Bae, J–A. Chroboczek, C. Fenouillet-Beranger, T. Ernst, E. Augendre, C. Le Royer, A. Zaslavsky, H. Iwai and S. Cristoloveanu, "Selected SOI puzzles and tentative answers," Semiconductor-On-Insulator Materials, Devices and Circuits: Physics, Technology and Diagnostics, Kiev, Ukraine (25–29 oct. 2010) Invited paper.