Modélisation, caractérisation et analyse de systèmes de PLL intégrés, utilisant une approche globale puce-boîtier-circuit imprimé

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MODELING, CHARACTERIZATION AND ANALYSIS OF INTEGRATED PLL SYSTEMS USING A GLOBAL CHIP-PACKAGE-BOARD APPROACH

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« … cherchez, et vous trouverez ; … »
Luc XI, 9

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ABSTRACT

This thesis work focuses on characterization, modeling and analysis of «Pulling» and «Pushing» phenomena in Phase Locked Loops (PLL) based on a global approach where distributed effects of electromagnetic couplings at different integration levels (chip-level, assembly-level, board or PCB-level) are taken into account.

The modeling approach adopts a hybrid methodology where the analysis of electromagnetic couplings combined with broadband equivalent circuit synthesis (*compatible with library models of active components*) is coupled with dynamic behavioral representations. The derived behavioral representations properly capture the effects of nonlinearities both at component scale (*non-linear characteristic of varicap devices as function of control voltages*) and at function block level (*non-uniform gain K_{VCO} of VCO circuits depending on frequency*).

The hybrid methodology renders possible the assessment of competitive effects resulting from «Pulling» and «Pushing» phenomena at chip level (*influence of the PLL, effects of the power amplifier, power integrity, or ground reference distribution, etc..),* and the distortions induced by components external to the chip at package and board levels (*such as components on PCB: SAW filters, decoupling capacitors, matching networks*).

The proposed approach is used for the study and design of two types of circuits developed by NXP-Semiconductors: an application related to automotive security and immobilization (an RF low power transceiver Integrated Circuit, *PLL running around 1.763GHz*), and a satellite receiver (*PLL operating at low power for LNB circuits working at 9.75/10.6 GHz*).

The obtained modeling results are validated by correlation with experimental data and by comparison with different time-domain and frequency-domain simulation tools results (ADS-Harmonic Balance, ADS-Shooting solutions, Cadence-Spectre).

Key-Words: *PLL, VCO, Pulling and Pushing Effects,* Electromagnetic Couplings*, Chip-Package-Board Co-Simulation, Hybrid Methodologies, Behavioral Modeling*.

RÉSUMÉ

Cette thèse porte sur la caractérisation, la modélisation et l'analyse des phénomènes de «Pulling» et de «Pushing» dans les systèmes de boucles à verrouillage de phase (PLL), utilisant une approche globale où les effets de couplages électromagnétiques aux différents niveaux d'intégration (*niveau puce, niveau assemblage, niveau report sur PCB*) sont pris en compte de manière distribuée.

L'approche de modélisation adopte une méthodologie hybride où l'analyse des couplages électromagnétiques combinée à des schémas équivalents large-bande (*compatibles avec les modèles de composants actifs disponibles dans les librairies*) est couplée à des représentations comportementales dynamiques. Les représentations comportementales développées permettent de capturer des effets de non-linéarités tant au niveau composant (caractéristique non-linéaire des Varicap en fonction des tensions de contrôle) qu'au niveau block de fonction (*gain K_{VCO} non uniforme de l'oscillateur contrôlé en tension (VCO) en fonction de la fréquence*).

Cette méthodologie hybride permet l'évaluation d'effets compétitifs résultant de phénomènes de «pulling» et de «Pushing» au niveau de la puce (influence de la PLL, effets de l'amplificateur de puissance, intégrité des alimentations ou distribution des références de masse, etc.) , et des distorsions induites par des éléments extérieurs à la puce (*exemple de composants sur PCB : Filtre SAW, capacités de découplages, réseaux d'adaptation*).

L'approche proposée est utilisée pour l'étude et la conception de deux types de circuits développés par NXP-Semi-conducteurs pour des applications liées à la sécurité automobile (*PLL fonctionnant aux alentours de 1.736GHz*) et à la réception satellitaire (*PLL de faible consommation fonctionnant à 9.75/10.6 GHz pour les circuits LNB*).

Les résultats de modélisation obtenus sont validés par corrélations avec les données expérimentales et par comparaison avec les résultats obtenus de différents outils (*ADS Harmonic- Balance/Transient de Agilent, Spectre de Cadence*).

***Mots clés** : PLL, VCO, Effets de Pulling et de Pushing, Couplages Electromagnétiques, Co-simulation Puce-Boîtier-Circuit imprimé, Méthodologies Hybrides, Modélisation comportementale*.

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GENERAL INTRODUCTION

In wireless communication systems, Phase Locked Loop (PLL) circuits are essential building blocks of integrated Radio Frequency (RF) transceivers for frequency synthesis, signal generation, frequency demodulation, etc. The design, optimization and verification of PLL circuits [1]-[9] require challenging simulation techniques and methods. Existing numerical simulation methods use two approaches, namely: frequency domain analysis (Harmonic balance) and time domain based analysis (shooting method). Each of these two approaches is more suited for specific working conditions: e.g., the frequency domain approach is suitable for RF high-frequency continuous signal waves and the digital signals, the time domain approach being used in general for analog low-frequency signals and the digital signals. However in PLL circuits both analog low-frequency signals (example Charge-Pump circuit) and RF continuous signals (example Voltage Controlled Oscillator circuit) coexist with digital signals as well (example Phase Frequency Detector). So coexistence of all these types of signals makes simulation of PLL circuits extremely challenging for available analysis tools and techniques. Because of the discrepancy between time-constants throughout the PLL sub-blocks, accurate direct numerical simulation of full-PLL systems for analysis of their locking mechanisms can prove impractical and extremely demanding in terms of CPU time efforts due to the high complexity involved with transistor-level description.

Noise spurs level at the output of PLLs represents essential specification constraints which directly affect global system performances. Accurate evaluation of such noise spurs in PLLs constitutes a real challenge for available simulation tools, sign-off verifications being principally carried out experimentally. The results of the experimental characterization of an Integrated Circuit (IC) are often analyzed using trial-and-error method to find the performance limiting factors and generally lead to partial modifications of identified blocks (e.g., potential noise sources) through FIBs (Focused Ion Beam). In order to limit re-design iterations during system evaluation and debugging phases, innovative methodologies are required for predictive simulation analysis, to achieve first-run right design.

The contribution of this thesis deals with Chip-Package-Board co-design methodologies [11]-[13] for system-level characterization, modeling and analysis of pulling and pushing effects taking place in PLL systems.

The manuscript thesis is organized around the following chapters:

- The first chapter discusses a brief analysis of nonlinear effects and the state-of-the-art in nonlinear circuits and systems analysis such as Phase Locked Loops (PLLs), behavioral modeling, and measurement techniques for device component-level, function block-level and global system-level predictive analysis. Available nonlinear circuit analysis tools remain fundamentally restricted to small-signal assumptions, full-wave large-signal [14] analysis emerges as a strong requirement in low noise and low power applications as discussed in [15] where necessity of large-signal analysis is underlined with advanced nonlinear simulation and modeling (e.g., Berkeley Design Automation solutions). Importance of global approaches where various type of effects such as electrical-thermal co-analysis, robustness against process variations requires development of innovative design methodologies where characterization and modeling of active nonlinear devices is essential [16]-[18]. Perceived advantages and limitations of each approach and modeling technique are discussed, to draw global methodologies where the various techniques are combined in the framework of single simulation environment. The different techniques of frequency pulling modeling and analysis are also presented, highlighting existing solutions available in the literature. The context, motivation and originality of the proposed contribution are outlined, and the test carrier examples are described.

- The second chapter covers analysis, diagnosis and measurement of pulling effects taking place in PLL systems. Qualification of observed pulling with respect to application

specifications is discussed. The characterization approach encompasses power spectrum measurement of TX systems, VNA measurement of on-chip inductors, transmission line interconnects, and on board SAW filters. Furthermore phase noise measurement is combined to power spectrum analysis for qualifying transmit-path noise performances including PA module. Observations done through the characterization lead to the main directions of analysis of frequency pulling origins at different level (block, system or chip-package-PCB levels). It is also in this chapter that we will study effects of Electro-Magnetic couplings and interferences on pulling and pushing phenomena. In the context of wireless Chip-to-Chip communication system-level inter-Chip and intra-Chip interferences analysis and characterization are investigated in [19] for BIST (Built-In-Self-Test) applications [20]-[21] and multi-GHz bandwidth applications.

- The third chapter is devoted to system-level behavioral modeling and analysis of pulling and pushing in PLLs where influences of the package as well as the assembly on the PCB are accounted for. The proposed modeling methodology combines SPICE-based circuit simulation with segregated behavioral models. The behavioral modeling approach incorporates non-linear effects taking place within the PLL (e.g., non linear dependency of VCO oscillation frequency against tuning voltage, effects of nonlinear varactors [22]). This segregated approach permits the versatility of the appropriate level of abstraction selection for the different blocks (transistor-level circuit description, and/or system block description). The flexibility of the model description helps in adapting of the chosen model to the parameters which influences have to be studied. Importance of electromagnetic couplings through power supply noise and ground connections is underlined by FIB cutting operations on sensitive design portions.

References of General Introduction

[1] C.S. Vaucher, “Architectures for RF Frequency Synthesizers,” PhD thesis, Twente University, 2001.

[2] C.S. Vaucher, O. Apeldoorn, M. Apostolidou, J. Dekkers, A. Farrugial, H Gul, N. Kramer and L. Praamsma,“Silicon-Germanium ICs for Satellite Microwave Front-ends, ” Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2005, pp.196-203.

[3] G. Girlando, S. A. Smerzi, T. Copani, and G. Palmisano “A Monolithic 12-GHz Heterodyne Receiver forDVB-S Applications in Silicon Bipolar Technology,” IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 3, 2005, pp.952-959.

[4] R. Aparicio and A. Hajimiri, “A Noise-Shifting Differential Colpitts VCO,” IEEE Journal of Solid-State Circuits, vol. 37, no. 12, 2002, pp.1728-1736.

[5] C.S. Vaucher and M. Apostolidou, “A low-power 20 GHz static frequency divider with programmable input sensitivity,” IEEE RFIC symposium 2002, pp. 235-23.

[6] P. Deixler et al., “QUBiC4X: An fT/fmax =130/140GHz SiGe:C BiCMOS manufacturing technology with elite passives for emerging microwave applications,” Proc. Bipolar/BiCMOS Circuits and Technology, 2004, pp. 233–236.

[7] K. Miyashita, “A Ku-Band Down-Converter with Perfect Differential PLL in 0.18um CMOS,” Proc. IEEE International Symposium on Circuits and Systems, 2010, pp.4289-4292.

[8] P. Philippe, S. Bardy, S. Wane, F. Moreau, E. Thomas, and L. Praamsma, “A Low Power 9.75/10.6GHz PLL in SiGe:C BiCMOS for Ku-Band Satellite LNBs”, in 14th European Microwave Integrated Circuits (EuMIC), Manchester, UK, 9th - 14th October 2011.

[9] P. Philippe, L. Praamsma, R. Breunisse, E. van der Heijden, F. Meng, S. Bardy, F. Moreau, S. Wane and E. Thomas, “A Low Power 9.75/10.6GHz Down-Converter IC in SiGe:C BiCMOS for Ku-Band Satellite LNBs

[10] ”, in Bipolar/BiCMOS Circuits and Technology Meeting (BCTM), 2011.

[11] J.Mao, G. Fitzgerald, A. Kuo, S.Wane, Coupled analysis of quasi-static and full-wave solution towards IC, package and board co-design. in IEEE 2007 Electrical Performance of Electronic Packaging, 111–114 (2007).

[12] S. Wane, A. Kuo, “Electromagnetic and thermal co-analysis for distributed co-design and co-simulation of chip, package and board”, in Proceedings of the IEEE-RFIC 2008 Radio Frequency Integrated Circuit Symposium Digest, 471–474 (2008).

[13] S. Wane and D. Bajon, “Electromagnetic Partitioning Methodology Towards Multi-Physics Chip-Package-Board Co-Design and Co-Simulation”, in Electromagnetics and Network Theory and their Microwave Technology Applications, Editors Stefan Lindenmeier and Robert Weigel, Springer 2011.

[14] D. Root, J. Verspecht, D. Sharrit, J. Wood, A. Cognata, "Broad-band poly-harmonic distortion (phd) behavioral models from fast automated simulations and large-signal vectorial network measurements", IEEE Trans. On Microwave Theory and Techniques, vol. 53, n° 11, pp. 3656-3664, November 2005.

[15] S. Wane, P. Philippe, B. El-Kassir, O. Tesson, L. Praamsma, O. Giard,M. Chapman, O. Minchin, and P. Gamand, “Multi-Physics Modeling of Electro-Mechanical Oscillators Comparative Analysis of Colpitts and Cross-Coupled Architectures,” in European Microwave Conference (EuMC), Paris, 28-30 Sept. 2010, pp. 620 - 623.

[16] O. Jardel, R. Quéré, S. Heckmann, H. Bousbia, D. Barataud, E. Chartier, and D. Floriot, “an electrothermal model for gainp/gaas power hbts with enhanced convergence capabilities,” IEEE Trans. on MTT, vol. 53, no. 2, February 2006.

[17] J. P. Teyssier, J. P. Viaud, J. J. Raoux, and R. Quéré, “Fully integrated nonlinear modelling and characterization system of microwave transistors with on-wafer pulsed measurements,” in IEEE MTT-S International, vol. 3, May 1995, pp. 1033–1036.

[18] S. Heckmann, R. Sommet, J. M. Nebus, J. C. Jacquet, D. Floriot, P. Auxemery, and R. Quéré, “Characterization and modeling of bias dependent breakdown and self-heating in gainp/gaas power hbt to improve high power amplifier design,” IEEE Trans. on MTT, vol. 50, no. 12, pp. 2811–2819, 2002.

[19] M. Ranaivoniarivo, and S. Wane, “Effects of Inter-Chip and Intra-Chip Electromagnetic Interferences on PLL Frequency Pulling and Spurs,” in 14th European Microwave Integrated Circuits (EuMIC), Manchester, UK, 9th - 14th October 2011.

[20] B. Elkassir, and S. Wane, “Design and Verification of Built-in-Self-Test (BIST) for RF, and Microwave Applications,” in 14th European Microwave Integrated Circuits (EuMIC), Manchester, UK, 9th - 14th October 2011.

[21] S.Wane, M. Ranaivoniarivo, B. Elkassir, C. Kelma, and P. Gamand, “Towards Cognitive Built-in-Self-Test (BIST) for Reconfigurable On-Chip Applications, and Contact-less Measurement,” in IEEE RFIC, Baltimore, MD, USA, 2011.

[22] Inigo Gutiérrez, Juan Meléndez, and Erik Hernandez, “Design and Characterization of Integrated Varactors for RF Applications”, John Wiley & Sons Ltd, 2006.

CHAPTER I:
LINEAR AND NON-LINEAR TECHNIQUES FOR BEHAVIORAL MODELING OF PLL SYSTEMS

I.0. Introduction

The challenges in modeling nonlinear components function blocks and systems result from different considerations and aspects. Main difficulties are in connection with proper derivation of mathematical description of nonlinear behavior of circuits and systems. In the past decades, various analysis techniques have been developed for modeling non-linear behavior of circuits and systems, among which are for instance Volterra analysis, behavioral neural networks, and hybrid linear analysis with simplified macro-models for nonlinear components. However, although these techniques provides some insight and approximate behavioral modeling for a wide range of nonlinear systems and applications, they have some limitations regarding their ability to build predictive analysis of nonlinear systems due to weaknesses arising from analytical model descriptions.

Because of difficulties with analytical methods to properly capture behavior model of non-linear systems, numerical simulations based on nonlinear time-domain differential equations are often used to simulate system performances. Classical simulation techniques are traditional transient analysis and complex envelope (in reference to shooting methods or harmonic balance), each with their advantages relative to the domain of considered applications. It is a well-known fact that such simulation techniques require considerable computing resources, simulation setup time, and high level of expertise for physical interpretation in link with used models and analysis accuracy. Since library oriented models are built on experimental characterization campaigns, efficient system-level analysis and modeling fully relies on proper combination of nonlinear device models founded on measurement characterization and passive circuitry embedding connections with associated parasitics.

The necessity of deriving global methodologies for device-level, function block-level and system-level modeling and analysis arises from the requirement of predictive analysis to anticipate circuits malfunctioning and ensure first-run-right designs.

This chapter discusses in the first section a brief analysis of nonlinear effects and presents the state-of-the-art in nonlinear system analysis for systems such as Power Amplifiers (PAs) and Phase Locked Loops (PLLs). We will present the behavioral modeling and the measurement techniques for device component-level, function block-level and global system-level predictive analysis. Perceived advantages and limitations of each approach and modeling technique are discussed, to draw global methodologies where the various techniques are combined in the framework of single simulation environment.

In the second section, we discuss the predictive modeling challenges of the PLL dealing with frequency pulling phenomenon. The different techniques for modelling pulling and pushing available in the literature are discussed ([63] to [82]) and proposed solutions for reducing their effects are analyzed.

Then we will discuss the context and the originality of the proposed contribution: the motivation, the proposed methodology for analyzing pulling phenomenon and the challenges we met.

Finally, we will discuss the test applications carriers we worked on, including automotive application named LoPSTer and a microwave down-converter for satellite TV application, the TFF1014 [23].

I.1. Overview of State of the Art of Non-Linear Techniques for PLL Modeling and Analysis

The modeling and the analysis of function blocks are necessary and crucial for the design of a system. Indeed, as the traditional design method uses cascade approach, each (sub-) function block should operate individually and the designer should be able to access the block response through its analysis or through the transfer function of the model to predict the system response and behaviour.

For Phase Locked Loops (PLL), a particular care should be taken for its analysis and modelling because it is most often the most critical or main function block of a transmission system.

I.1.1. General considerations

a. Baseband, Passband Signals and Modulations

Baseband and Passband signals

In RF communication, the signal to be transmitted is usually a high-frequency carrier modulated signal representing the data. We can define the "baseband signal" as a signal whose spectrum is non-zero in the vicinity of $\omega=0$ and negligible elsewhere. Mostly, it is the digital data to transmit. A "passband signal" has a spectrum which is non-zero in a band around a "carrier" frequency ω_c and negligible outside this band. A passband signal can be represented by the following equation:

$$x_{BB}(t)=A(t)\cdot\cos(\omega_c t+\Phi(t)) \qquad \text{[I.1-1]}$$

$A(t)$ and $\Phi(t)$ are functions of time.

Modulation

Modulation process converts a baseband signal to a passband signal by varying one or more properties (amplitude, excess phase and frequency) of a carrier according to the time varying baseband signal. For analog or digital modulation, the carrier is modulated by respectively an analog or a digital baseband signal.

For a periodic carrier signal of $A\cdot\cos(\omega_C t+\Phi)$, a modulation can be obtained by varying its amplitude or its phase.

b. RF Transmitter-Receiver systems

Various analog circuits operating at high frequencies are used in digital data transmission systems for wireless applications. They are integrated within these systems and permit to transmit the data to process. In general, the digital or analog telecommunications systems have the topology shown in Figure I.1-1.

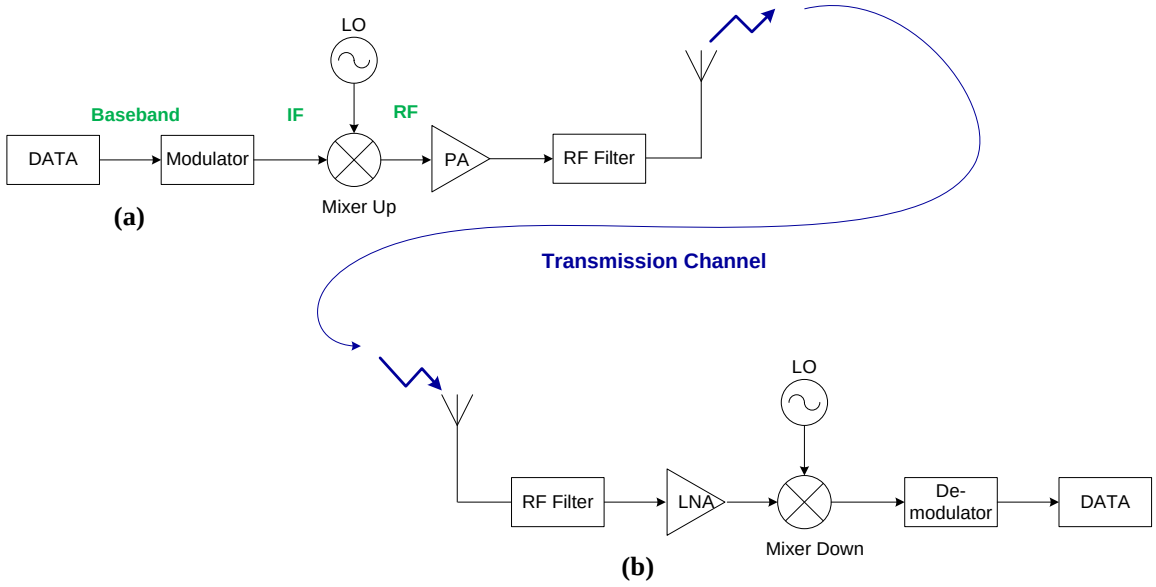


Figure I.1-1: Block diagram of a generic of a wireless transmitter (a) – receiver (b) system

These systems are composed by a transmission part Figure I.1-1(a), a reception part Figure I.1-1 (b) and a transmission channel. The transmission channel can be defined through different framework such as free space, fibre optic, coaxial cable etc for the signal propagation. Transmission and reception chains can be more or less complex depending on the system and application considered, such as the use of a multiple downconversions of RF to baseband spectrum (heterodyne receivers).

Transceiver permits to carry out the two functions through a unique IC. As the filtering solutions of the transceivers are most of the time outside the IC, the principal analog function blocks of the IC are the amplifiers, the power amplifier (PA) in transmit mode or low noise amplifier (LNA) in reception mode, the mixer and the local oscillator (LO).

As in emission mode the signal amplitude levels are higher than in reception, interferences inside the IC are more important in transmit mode. We will then focus on the transmission mode (TX) and its principal analog function blocks such as the PA and the local oscillator or the frequency synthesizer; the latter being able to operate directly in RF domain.

c. The Power Amplifier

PAs are devices used to amplify signals in order to obtain high signal powers necessary for transmission. The principal criteria of PA performances are:

- the output power level and the PA gain (the ratio between the PA output power desired and the input power)
- the efficiency, which is the ratio of the output RF power delivered to the load to the DC power supply
- the matching network at input, output or inter-stage of the PA: mismatch in the circuit can cause efficiency and/or output power reduction and increase distortion at the PA output
- the (non) linearity and the distortion which induce harmonics and modulations:

Let the output voltage y of a non linear circuit be developed into Taylor series of the input voltage x as:

$$y=a_0+a_1\cdot x+ a_2\cdot x^2+a_3\cdot x^3+... \qquad [I.1\text{-}2]$$

If the input signal is sinusoidal ($x=V_0\cdot\cos(\omega_0 t)$), then the output signal of the non linear circuit is a combination of DC, fundamental and series harmonic terms:

$$
\begin{aligned}
y = & \left(a_0 + \frac{1}{2} a_2 \cdot V_0^{\,2}\right) \\
& + \left(a_1 \cdot V_0 + \frac{3}{4} a_3 \cdot V_0^{\,3}\right) \cdot \cos(\omega_0 t) \\
& + \left(\frac{1}{2} a_2 \cdot V_0^{\,2}\right) \cdot \cos(2\omega_0 t) \\
& + \left(\frac{1}{4} a_3 \cdot V_0^{\,3}\right) \cdot \cos(3\omega_0 t) + \ldots
\end{aligned}
\qquad \text{[I.1-3]}
$$

Then in small signal functioning, the voltage gain at the fundamental frequency is:

$$
G_V = \frac{y(\omega 0)}{x(\omega 0)} = a_1 + \frac{3}{4} a_3 \cdot V_0^{\,2} \qquad \text{[I.1-4]}
$$

Most of the time, the coefficient a3 is negative and when the amplitude of the input signal (V_0) increases, the gain decreases in V_0^2, it is the phenomenon of gain compression. The 1dB compression point refers to the output power level at which the amplifier transfer characteristics deviates from the ideal one by 1 dB. The distortion due to the gain compression or expansion is referred as AM-AM conversion, degrading the quality of amplitude modulated signals.

The non-linearity of the PA can also be characterized through a two-tone input signal ($x=V_0 \cdot (\cos(\omega_1 t)+\cos(\omega_2 t))$), then the output signal is a combination of DC, fundamental, harmonics and intermodulation (IM) tones:

$$
\begin{aligned}
y = & \left(a_0 + a_2 \cdot V_0^{\,2}\right) \\
& + \left(a_1 \cdot V_0 + \frac{9}{4} a_3 \cdot V_0^{\,3}\right) \cdot \left(\cos(\omega_1 t) + \cos(\omega_2 t)\right) \\
& + \left(a_2 \cdot V_0^{\,2}\right) \cdot \left(\cos((\omega_2 - \omega_1)t) + \cos((\omega_1 + \omega_2)t)\right) \\
& + \left(\frac{1}{2} a_2 \cdot V_0^{\,2}\right) \cdot \left(\cos(2\omega_1 t) + \cos(2\omega_2 t)\right) \\
& + \left(\frac{1}{4} a_3 \cdot V_0^{\,3}\right) \cdot \left(\cos(3\omega_1 t) + \cos(3\omega_2 t)\right) \\
& + \left(\frac{3}{4} a_3 \cdot V_0^{\,3}\right) \cdot \left(\cos((2\omega_1 \pm \omega_2)t) + \cos((2\omega_2 \pm \omega_1)t)\right) + \ldots
\end{aligned}
\qquad \text{[I.1-5]}
$$

The output fundamental tones at ω2 and ω1 present amplitude distortion and the terms at ($2\omega_1+\omega_2$), ($2\omega_1-\omega_2$), ($2\omega_2+\omega_1$), ($2\omega_2-\omega_1$) corresponding to the 3rd order intermodulated (IM3) tones are within the passband of the circuit. The distortion effects due to the intermodulation products are showed below:

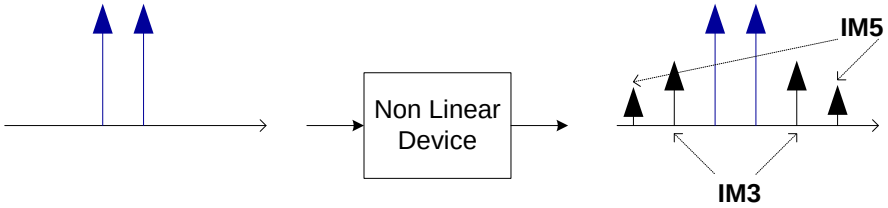


Figure I.1-2: intermodulation products of a non-linear power amplifier with two tones input around the fundamental tone

The phase difference between input and output signals of the amplifiers also changes with the input power strength variations. Non linearity of PAs can also be due to phase distortion referred to as AM-PM distortion: undesired phase deviation can be due to amplitude variations of the system (e.g. intentional modulation of signal amplitude, power supply ripple, thermal drift…) corrupting the phase of the carrier and causing intermodulation distortions.

According to the design configurations of the PA circuit and the methods of operation, the PAs are classified into different classes types: A, B, AB, C, D, E and F. Classes A, B and AB are considered as linear mode amplifiers whereas the others are nonlinear, especially class-E power amplifiers which use switching technique for achieving significantly higher efficiency by shaping the voltage and current waveforms to prevent simultaneous high voltage and high current in the transistor it minimizes the power dissipation [24]. In [91] behavioral modelling approach for power amplifiers is discussed. In [92], a dynamic distortion characterization of multiport RF PAs using MTA-based multiport measurement setup [97] is proposed.

d. Phase Locked Loop Fundamentals

Integrated circuits (IC) need stable clocks to drive the functioning of the chip and require to achieve a precise output signal. Frequency synthesizers permit to generate variable RF frequencies from a stable "reference" frequency generally around 10MHz. PLLs are very used nowadays in RF applications as transceiver. Thanks to its feedback loop, the PLL its output signal benefits from the frequency stability and high spectral purity of the reference that is in general a crystal oscillator.

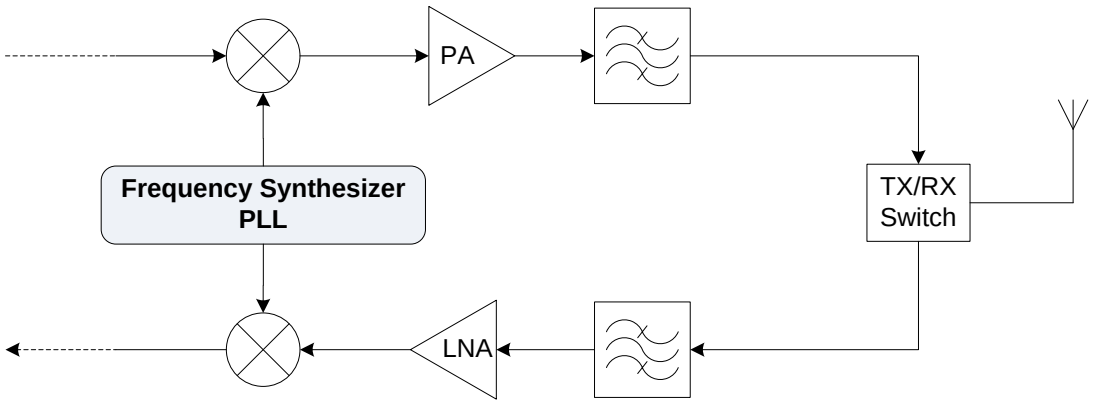


Figure I.1-3: Example of PLL use in a generic transceiver architecture

A Phase Locked Loop is a feedback control system that generates an output signal synchronized to a reference signal in terms of frequency and phase. As shown in Figure I.1-4, a simple PLL consists in three main functional blocks [25], [27]:

- A Phase Detector (PD)
- A Loop Filter (LF)
- A Controlled Oscillator, mainly controlled by voltage.

The phase detector compares the phase difference between the output signal y(t) and the reference signal x(t) and generates a signal proportional to the phase error. The high-frequency components will be suppressed by the low-pass loop filter allowing the DC value to control the Voltage Controlled Oscillator (VCO). When the phase error between the oscillator output and the reference signal is null or remains constant, the PLL is synchronized or "locked".

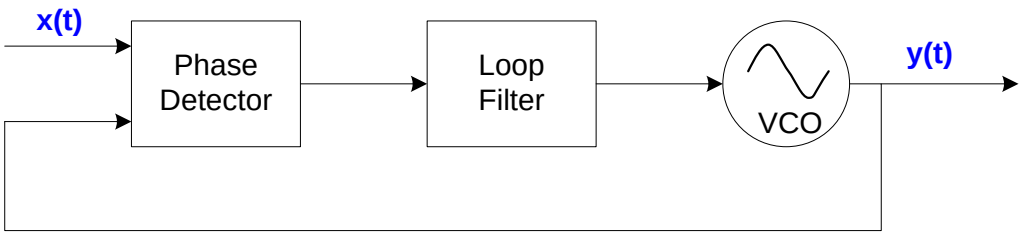


Figure I.1-4: Block diagram of a basic PLL

In our study, we will only focus on analog PLLs as it is the most common PLL architecture. The phase detector is usually a Phase Frequency Detector (PFD) followed by a Charge Pump (CP) circuit that converts the phase/frequency error into width-modulated current pulses. The low pass loop filter that filters the charge-pump current pulses is generally a passive RC filter that delivers the control voltage to the oscillator. As LC oscillator proposes lower phase noise and greater output voltage swings [29] solutions, we will analyze only those kind of VCO, with resonator. The PLL controls the oscillator frequency and phase: drift or instability are corrected by the feedback loop. As the frequency f_{Ref} of the reference signal x(t) is usually around few tens of MHz, the PLL system generates an RF signal y(t) then at higher output frequencies f_{Out}; the feedback loop should contain a frequency divider by N before the phase/frequency comparison with the reference. When the PLL is locked, $f_{Out}=N\times f_{Ref}$.

I.1.2. Small-Signal Analysis and Large-Signal Analysis

To analyse the PLL functioning, as for all active circuits, the implementation at transistor level is performed using small or large signal models.

a. Small-Signal Analysis

Small-signal analyses are used to approximate the behaviour of nonlinear devices, such as transistors, with linear equations. The linearization is done around the DC bias point of the device: around the voltage/current levels when no signal is applied or around a time-invariant operating point. The analysis technique is considered accurate for small excursions around this point but do not include frequency conversion effects.

The linearization around the bias point is done by taking partial derivatives of the formula with respect to all governing variables. This can be possible by associating the derivatives to physical components such as capacitance, resistance and inductance.

The analysis can be performed by sweeping parameters such as the frequency, the temperature, the component instance parameter or model parameters…

Here are some small-signal analysis that can be used during PLL analysis [33][34][36]:

- AC analysis (AC): permits to compute the response to a given small sinusoidal stimulus.
- Transfer function analysis (XF): it computes the transfer function from every source in the circuit to a single output. It differs from a conventional AC analysis as the AC analysis computes the response from a single stimulus to every node in the circuit
- Noise analysis (Noise): it computes the total noise spectral density at the output by including contributions from the input source and the output load. Noise analysis permits to predict the phase noise of oscillating circuits.
- S Parameters analysis (SP): The SP analysis linearizes the circuit around the DC operating point and computes S-parameters of the circuit taken as an N-port. Each active port is turned on sequentially, and a linear small-signal analysis is performed.

To compute steady-state solutions and simulate circuits that translate frequency, which is the case of phase-locked loops, linearization of the circuit can be done around a periodically time-varying operating point, which permits to calculate transfer-functions that include frequency translation.

Computing the small-signal response of a periodically varying circuit is done in a two step process. First, the small stimulus is ignored and the periodic steady-state response of the circuit to possibly large periodic stimulus is computed (we will later see with PSS analysis).

The periodically time-varying representation of the circuit is computed and saved for later use. Then, in the second step of the analysis, the small stimulus is applied to the periodically varying linear representation to compute the small signal response.

Periodic small-signal analysis computes the steady- state response of a linear periodically time-varying circuit to a sinusoidal stimulus and gives the opportunity to do, among others [33][34][36][37], Periodic AC analysis (PAC), Periodic S-Parameter analysis (PSP), Periodic noise analysis (Pnoise), and periodic Transfer Function analysis (PXF).

While analyzing circuits that exhibit multi-tone frequency translation such as PLLs, the circuit is first linearized around a quasi-periodically varying operating point which allows transfer-functions that include frequency translation, whereas a simple linearization around a DC operating point doesn't offer this opportunity because linear time-invariant circuits do not exhibit frequency translation. Also, the frequency of the sinusoidal stimulus is not constrained by the period of the large periodic solution.

Computing the small-signal response of a quasi-periodically varying circuit is done in two step process. First, the small stimulus is ignored and the quasi-periodic steady-state response of the circuit to possibly large periodic stimuli is computed (we will explain it in the next paragraph by using QPSS analysis). The quasi-periodic time-varying representation of the circuit is computed and saved for later use. Then, the second step of the analysis consists of applying the small stimulus to the periodically varying linear representation to compute the small signal response.

The quasi-periodic small-signal analyses can be done such as in [33][34][36] QPAC, QPSP, QPnoise, and QPXF analyses.

b. Large-Signal Analysis

Large-signal analysis computes the response of a circuit to large signals.

Instead of analyzing a periodic system in full transient, it will be more efficient to find periodic steady-states directly.

Periodic steady-state (PSS) analysis [33][34][36] is a large-signal analysis that directly computes the periodic steady-state response of a circuit. Simulation times are independent of the time constants of the circuit. It also determines the periodic operating point for the circuit which can then be used during a periodic time-varying small-signal analysis, such as PAC, PXF, PNOISE, PSP…

The algorithms used for periodic steady-state analysis are the shooting method in the time domain or the Harmonic Balance algorithm in the frequency domain. Before obtaining the periodic steady-state solution, an initial transient phase is preliminarily achieved to initialize the circuit.

The shooting method [35] is an iterative time domain method. It computes the initial condition and uses iterative methods to obtain the final steady state result as the signals are periodic: the circuit is evaluated during one period starting from the initial condition and the final state of the circuit is computed along with the sensitivity of the final state with respect to the initial state. If the final state is a linear function of the initial state, then the new initial condition directly results in periodicity. Otherwise, additional iterations are needed.

Harmonic balance [33][34][35][36][38] is an algorithm used to find steady state response in frequency domain. The voltage and current sources create discrete frequencies resulting in a spectrum of discrete frequencies at every node in the circuit. Linear devices are estimated in the frequency domain and non-linear devices in the time domain while the Fourier transform is used for conversion between frequency and time domains. It iterates until the sum of the currents of all the harmonics at all the nodes is near 0 in the frequency domain. When the solution is obtained, the time domain waveform is calculated using an IFFT.

Generally, harmonic balance (HB) is very efficient and faster in simulating linear and weakly nonlinear circuits while shooting is more suitable for very nonlinear circuits with sharply rising and falling signals. HB is also advantageous over shooting in handling frequency dependent components, such as delay, transmission line, and S-parameter data.

Quasi-periodic steady state analysis (QPSS) calculates the response due to multiple large-signal input frequencies at unrelated frequencies. All of the input signals are treated in the same way as the PSS drive source so that the calculated output includes all the intermodulation distortion effects caused by frequency translation of all harmonics of the input signals as well. QPSS can compute circuit responses with closely spaced or incommensurate fundamentals, periodic distortion. Harmonic effects can then be modelled, which cannot be resolved by PSS efficiently.

The simulation time of QPSS analysis is independent of the time-constants of the circuit. Also, QPSS analysis sets the circuit quasi-periodic operating point, which can then be used during a quasi-periodic time-varying small-signal analysis, such as QPAC, QPXF, QPSP and QPNOISE[33][34][36].

I.1.3. Behavioral Modeling Techniques

As circuit blocks definition become more and more complex, the verification of system designs with transistor-level simulator takes too much time and memory. Behavioral model are thus used in circuit simulation to accelerate the analysis.

A behavioral model reproduces the required behavior of the original analyzed system/component through mathematical concepts (that include differential equations, transfer functions, statistical distributions, tables or arithmetic expressions…). This model depends on the module terminals and external parameters, and predicts future system states (the circuit input-output behavior) from past systems states.

Behavioral simulation and modeling can considerably reduce the design time in a top-down design approach. Indeed, with the constraint of the function block design, behavioral simulation and optimization can be used to select the architecture of the design, then to map the architecture and circuit specifications to the detailed specifications of components or sub-blocks. The behavioral simulation permits early design verification in the design process.

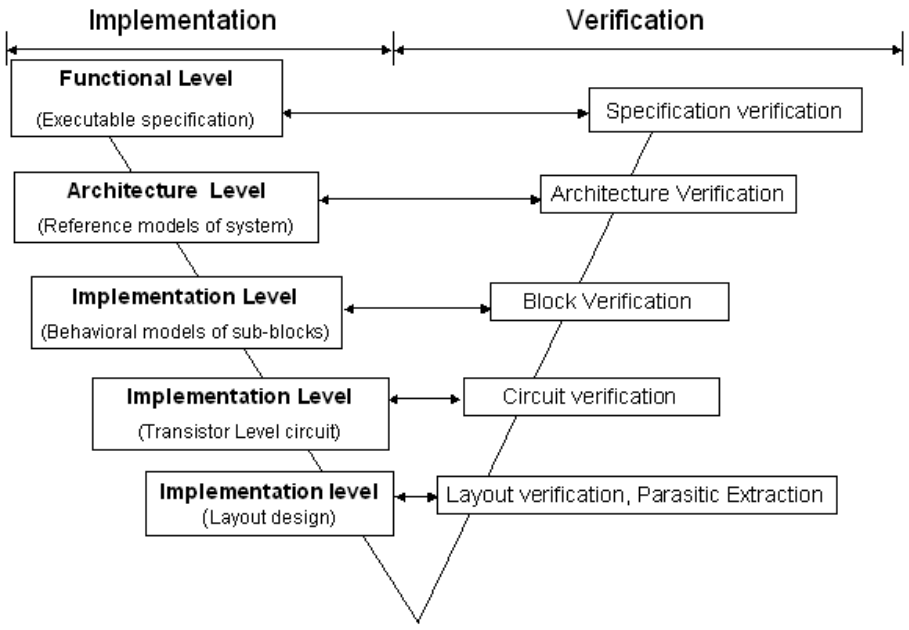


Figure I.1-5: Top-down design and bottom-up verification

To describe a behavioral model of a system, Hardware Description Language (HDL) can be used for digital and mixed-signal systems. It supports:

- the development, verification, synthesis, and testing of hardware designs
- the communication of hardware design data
- and the maintenance, modification, and procurement of hardware.

PLLs are most of the time designed in analog mixed-signal integrating digital (as flip-flop based PFD) and analog (as the VCO) function blocks. To analyze mixed signals, behavioral models for both digital and analog circuits need to be developed and system simulation at behavioral level should be performed.

Verilog HDL language [39] is mainly used to describe I/O responses and the behavior of the IC digital part.

For only analog systems, Verilog-A [41][42]subset is used. Using Verilog-A language, designers of ICs can create and use modules that encapsulate high-level behavioral descriptions as well as structural descriptions of systems and components. The behavior of each module can be described mathematically in terms of its terminals and the external parameters applied to the module. The structure of each component can be described in terms of interconnected sub-components. The solution of analog behaviours obeys the laws of conservation as the generalized form of Kirchhoff's Potential and Flow Laws (KPL and KFL).

To facilitate mixed-signal system description and simulation, Verilog-AMS HDL [42][40], derived from IEEE std 1364-2005 Verilog HDL[39], was developed in order to have a single-language solution for the specification and simulation of analog, digital, and mixed-signal systems.

```
module nand_gate(vin1, vin2, vout)
  (vlogic_high, vlogic_low, vtrans, tdel, trise, tfall)
node [V, I] vin1, vin2, vout;
// voltage level for '1', '0' and treshold
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans = 1.4;
 // square signal features (time delay, rise and fall time)
parameter real tdel = 2u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);
{
  real vout_val;
  integer logic1, logic2;

// comparison of vin1 and vin2 signals data
  initial {
    if (vlogic_high < vlogic_low) {
      $error("Range specification error.  vlogic_high = (%E) less than vlogic_low = (%E).\n", vlogic_high, vlogic_low );
    }
    if (vtrans > vlogic_high || vtrans < vlogic_low) {
      $warning("Inconsistent $threshold specification w/logic family.\n");
    }
  }

  analog {
    logic1 = V(vin1) > vtrans;
    logic2 = V(vin2) > vtrans;

    if ($threshold(V(vin1) - vtrans, 1))  logic1 = 1;
    if ($threshold(V(vin1) - vtrans, -1)) logic1 = 0;

    if ($threshold(V(vin2) - vtrans, 1))  logic2 = 1;
    if ($threshold(V(vin2) - vtrans, -1)) logic2 = 0;

// define the logic function and assigning vout value
    vout_val = !(logic1 && logic2) ? vlogic_high : vlogic_low;

    V(vout) <- $transition( vout_val, tdel, trise, tfall);
  }
}
```

Figure I.1-6 : Example of an HDL description of a NAND gate

```
module nand_gate(vin1, vin2, vout);
input vin1, vin2;
output vout;
electrical vin1, vin2, vout;
// voltage level for ‘1’, ‘0’ and treshold
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans = 1.4;
// square signal features (time delay, rise and fall time)
parameter real tdel = 2u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);

  real vout_val;
  integer logic1, logic2;

// comparison of vin1 and vin2 signals data
  analog begin

    @ ( initial_step ) begin
          if (vlogic_high < vlogic_low) begin
            $display("Range specification error.  vlogic_high = (%E) less than vlogic_low = (%E).\n", vlogic_high, vlogic_low );
            $finish;
          end
          if (vtrans > vlogic_high || vtrans < vlogic_low) begin
            $display("Inconsistent $threshold specification w/logic family.\n");
          end
    end

    logic1 = V(vin1) > vtrans;
    logic2 = V(vin2) > vtrans;

    @ (cross(V(vin1) - vtrans, 1))  logic1 = 1;
    @ (cross(V(vin1) - vtrans, -1)) logic1 = 0;

    @ (cross(V(vin2) - vtrans, 1))  logic2 = 1;
    @ (cross(V(vin2) - vtrans, -1)) logic2 = 0;

// define the logic function.
    vout_val = !(logic1 && logic2) ? vlogic_high : vlogic_low;

    V(vout) <+ transition( vout_val, tdel, trise, tfall);
  end
endmodule
```

Figure I.1-7 : Example of a Verilog-A description of a NAND gate

Computational macro-modeling and simulation of such systems can also be done using Simulink behavioral modelling.

With its interactive graphical environment, the Simulink [43] software already provides a customizable library containing blocks of time-varying systems that can be implemented, customized, simulated, and tested. Its main task is to solve numerically Ordinary Differential Equations (ODE) in time based domain. By dividing the ODE into small time segments, the solution is numerically calculated for only a small segment.

I.1.4. Power-Series and Volterra Modeling

Non-linear circuits and elements output function y(t) can generally be expanded in terms of power series as:

$$y(t) = \sum_{n=0}^{\infty} a_n (t-\tau)^n = a_0 + a_1(t-\tau) + a_2(t-\tau)^2 + \ldots \qquad \text{[I.1-6]}$$

or using a set of functions $g_n(t)$ as:

$$y(t) = \sum_{n=0}^{\infty} a_n g_n(t) \qquad \text{[I.1-7]}$$

However, modeling nonlinear systems with power series model is only possible with memoryless systems [44][45].

To deduce the functional relationship between a system input function x(t) and an output function y(t) from observations of the in and out-going signals, Volterra model [46] gives a system characterization of nonlinear systems with memory in terms of polynomial functional by providing stability criteria and methods for the synthesis of optimal systems of a given order.

We denote T the system operator from the input to the output function space:

$$Y=T[x] \qquad \text{[I.1-8]}$$

For a time-invariant and continuous system T, i.e. if the system response remains unchanged for repeated presentation of the same input and if small changes in the input functions x(t) lead to small changes in the corresponding system output functions y(t), T can be expressed by the Volterra series:

$$y = T[x] = \sum_{n=1}^{\infty} H_n[x] \qquad \text{[I.1-9]}$$

With H_n the nth-order Volterra operator given by the following expression:

$$H_n[x(t)] = \int_{-\infty}^{\infty} \ldots \int_{-\infty}^{\infty} h_n(\tau_1, \tau_2, \ldots \tau_n) x(t-\tau_1) x(t-\tau_2) \ldots x(t-\tau_n) d\tau_1 d\tau_2 \ldots d\tau_n \qquad \text{[I.1-10]}$$

$h_n(\tau_1,\tau_2 \ldots \tau_n)$are the Volterra kernel of the systems. It defines the system memory, i.e. it delimits the time interval in which past inputs can influence the current system output. Thus the Volterra series characterize systems in which the output also depends on past inputs

In the discrete time domain, with the discrete time Nth order Volterra model, [I.1-9] can be written with a memory length M as:

$$\begin{aligned} y(k) &= h_0 + \sum_{m_1=0}^{M-1} h_1(m_1) x(k-m_1) + \sum_{m_1=0}^{M-1} \sum_{m_2=0}^{M-1} h_2(m_1, m_2) x(k-m_1) x(k-m_2) + \ldots \\ &+ \sum_{m_1=0}^{M-1} \ldots \sum_{m_N=0}^{M-1} h_N(m_1, m_2, \ldots m_N) x(k-m_1) x(k-m_2) \ldots x(k-m_N) \end{aligned} \qquad \text{[I.1-11]}$$

As the PLL and its sub-function block (the phase detector and the VCO) are non-linear, the analysis of nonlinear distortion of frequency or phase modulated signals can be performed for PLL using Volterra modeling. In Carvalho et al. papers [47][48][49], VCO and PLL linear distortions are analyzed in the frequency domain using Volterra series approach: PLL non linear transfer function (NLTF) are derived from Volterra functional of 3rd order to analyze voltage-frequency modulation and transmission.

I.1.5. Hybrid Models and Co-simulation

Verification of complex ICs requires speed and efficiency that can only be provided in a unified verification methodology. A unified verification methodology consists of many different tools, technologies and processes all working together in a common environment, in co-simulation.

For accurate simulations of analog and mixed signals/blocks, it is necessary to combine simulations of analog signals and/or mixed models through system simulations (co-simulation). Cadence AMS Designer can provide such interfaces between sub-blocks and transistor circuits, especially with Matlab/Simulink and Virtuoso AMS Designer models (Verilog-AMS, VHDL-AMS, Verilog, VHDL, SystemVerilog, SystemC, Virtuoso Spectre/Spice/HSpice) in a single flow where test benches for transient and envelope analysis

together with system level simulation in Simulink can be defined in one software using a block model described by the other software language [50][51].

However, co-simulation between a system level and a transistor level description for example can take a long time to achieve. Moreover as there is also no systematic way of deriving behavioral models of active blocks (VCO, PFD, etc), libraries of behavioral models should permanently be created or improved.

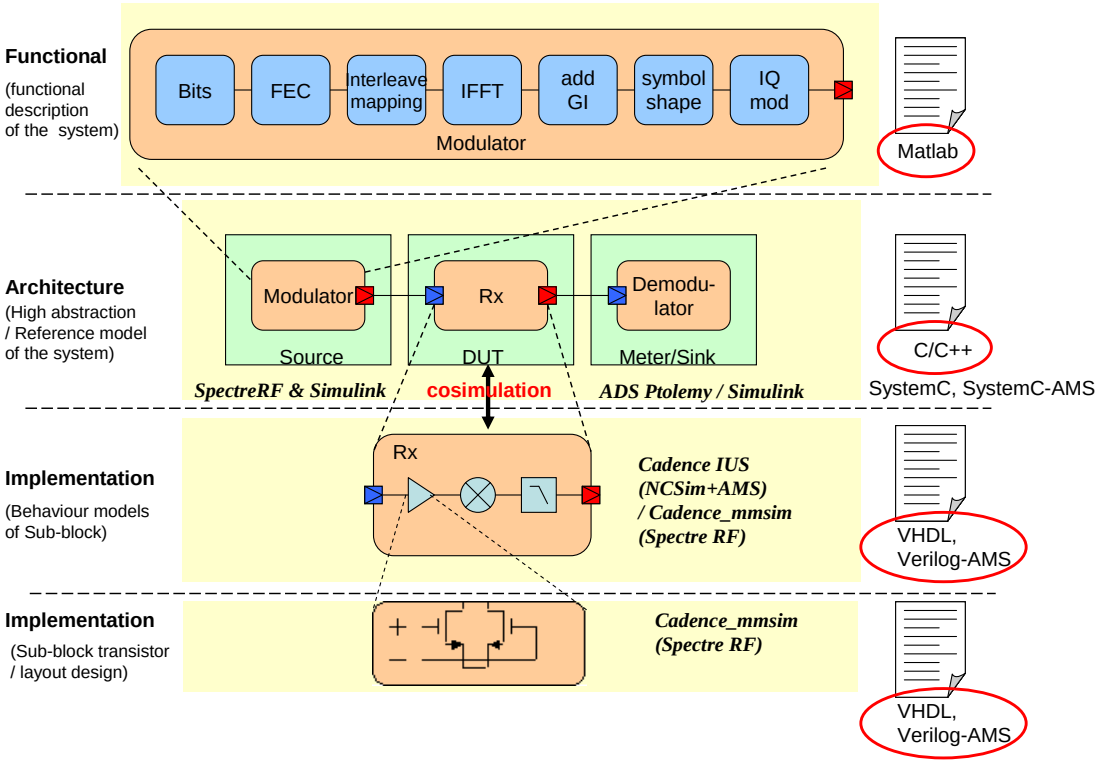


Figure I.1-8: Illustration of system abstraction levels, tools and models used

In addition, a lack of unified active-passive co-simulation can be felt and it is also difficult to couple digital and analog circuits in a single simulation environment. In an entire single chip, to tackle passive and active co-simulation, combination of passive RLCK models with transistor level IPs is possible through statistical extraction of RLCK interconnect parasites with Assura RCX-PL during Spectre simulation in extracted view [52].

However, parasitic couplings between neighbouring blocks can be addressed only from EM simulations and actually there is no tool that can combine semiconductor physics and the Maxwell's equations that could permit to estimate EM couplings in a complex design. From RFDE, a design environment for RFIC and RF SiP products centralized around Cadence, EM simulation tools as Sonnet and Momentum can be used for performing EM simulations. Once the results of the simulation obtained, the S-parameters, they can be re-integrated into SpectreRF transient or frequency analyses [53] but the model stays only valid in the frequency domain of EM analysis. In addition, the analysis follows cascade-based approaches so all the potential interactions (e.g. of IC with package and PCB…) are most of the time ignored restricting main analyses to couplings taking place within the chip [54]-[56].

Such global analysis that couples circuit simulation and EM couplings is also possible with other commercial tools by coupling for example Agilent Momentum and Harmonic Balance of ADS (Advanced Design system) simulations [57] or also by coupling EM simulation results of a dedicated algorithm and ADS [58] .

I.1.6. Measurement Techniques

Measurements in DC with multimeters (ammeter, voltmeters and ohmmeters) permit to determine the characteristics of the transistor (e.g Id=*f*(Vd, Vg)), as its operating point. Current consumption and DC feeding voltage of the device can also be measured.

Measurements in AC are generally done with AC meter or oscilloscopes. Time variations of the voltages are obtained. AC analyses permit to determine the figures of merit of transistors such as the transition frequency f_t and the maximum oscillation frequency f_{max} by determining the elements of the small signal equivalent circuit of the transistor for example.

Measurements in RF permit to determine response of the device or network at RF or even microwave frequencies. Several types of analyses can be performed [59]:

- Network analysis: with a scalar network analyzer, permits to determine the ratio between the transmission and reflection coefficients of the Device Under Test (DUT) in terms of amplitude. With a vector network analyzer, one determines the amplitude and phase of the S-parameters, the input/output impedances and the return loss of the DUT. Calibration of the measurement system is necessary to fix the reference plane at the probes tips.
- Noise performances: Noise Figure/Factor determination permits to gather the information about the noise performance of an RF system. The Y factor method is widely used nowadays, it consists in connecting a noise source at the Rx input, then measuring the output noise after the channel filter with noise diode switched ON and OFF; the difference between these two responses gives the wanted Noise Figure.
- Non Linear measurements: with X-parameters [60][61][62]measurements, permit to determine the non-linear characteristics of the output power of a device, functions of its input power, that are the 1dB input compression point P1dB, the third order intercept point IP3, and the IIP3 (input power relative to the intercept point).
- Signal characteristics: previous measurements are generally completed using signal source analyzers, spectrum analyzers or also phase noise analyzers. The parameters measured may include: signal or carrier level, sidebands, spurs, harmonics, phase noise, etc.

Before the final version of the chip, each component or sub-function block should be measured in stand-alone to verify its behavior and functioning in respect to its specifications. For this, on-wafer measurements of structures of Multi Product Wafers (MPW) are usually carried out. On-wafer de-embedding through standards measurements are carried-out in order to shift the reference plane of the measurement to the terminals of the DUT.

The achievement of the electrical tests allows the evaluation the IC performances [28] but the measurement/characterization (by varying the temperatures and the voltage feeding of the IC) induced some challenges. First, the time-frequency correlation of the measurement results: indeed network and spectrum analyzers do not include DC information. Then, to find the performance limiting factors, if access to internal nodes is necessary, FIB (Focused Ion Beam) is the only solutions for the measurements before redesigns.

I.2. Simplification of PLL Systems for Design Specification: Predictive Modeling Challenges

I.2.1. State of the Art Design of Methodology Challenges for PLL Systems

Once the type and the order of the PLL (Integer-N PLL chap.3.2 of [25], Fractional-N PLL in chap.5&6 of [30] or digital PLL in chap.3 of [26]…) are determined according to the IC specifications, the PLL design requires some preliminary calculations and simulations. Only analog PLL with passive loop filter will be discussed in this paragraph (adding active devices implies additive noise, complexity and cost).

First, the frequencies and the division ratios should be calculated knowing the reference frequency f_{Ref}, the RF VCO frequency f_{VCO} and by defining the comparison frequency f_{comp} as:

$$\begin{cases} f_{comp} = \dfrac{f_{Ref}}{M} \\ f_{comp} = \dfrac{f_{VCO}}{N} \end{cases} \qquad \text{[I.2-1]}$$

with N the RF division ratio (for the prescaler and the main divider) and M the reference division ratio . In fractional-N PLL, the VCO RF frequency=$N/M \cdot f_{Ref}$ can be a non integer multiple of the reference frequency. This is generally achieved by modulating the division ratio between two adjacent integer values.

Second, to reduce iterations to design the loop filter of the PLL, several parameters should be known with the system requirement.

If the PLL open loop bandwidth ω_c is not an input parameter of the analysis, it can be estimated from the PLL characteristics namely its order (the number of poles of its transfer function), the different function block gains (VCO, PFD/CP), the division ratios, and the goals targeted in terms of locking time and frequency tolerance/accuracy ε. This bandwidth can be determined using approximation (lock time ~ $-\ln(\varepsilon)/\omega_c$) or a locking time graph as given in chap.3 of [31].

Then, for loop filters of order superior to 1, the pole and zero of the loop filter have to be determined. For that, the position of the zero and frequency poles regarding ω_c need to be specified depending on the loop filter order.

Third, the loop filter RC components have to be determined. From the loop bandwidth targeted and the poles and zeros positions desired of the PLL loop gain, the RC values of the filter are determined as detailed in [30] chap.20 to chap.23 and in [32]. Increasing the RC stages reduce the reference spurs.

And finally, the analysis of the designed PLL performance should be completed mainly in terms of stability, transient response, noise model and spur level.

With all the PLL parameters, the open loop gain W(jω), which is the product of the block gains in the loop, and the closed loop gain T(jω) of the PLL can be determined.

$$T(j\omega) = \frac{\theta_{VCO}}{\theta_{ref}} = \frac{N \cdot K\varphi \cdot Z_f(j\omega) \cdot K_{VCO}}{N \cdot j\omega + K\varphi \cdot Z_f(j\omega) \cdot K_{VCO}} \qquad \text{[I.2-2]}$$

$$W(j\omega) = \frac{K\varphi \cdot K_{VCO} \cdot Z_f(j\omega)}{N \cdot j\omega} \qquad \text{[I.2-3]}$$

With Kφ the charge pump gain, K_{VCO} the VCO gain and Z_f the loop filter impedance or transfer function. Conversely, if the loop filter parameters are fixed, PLL stability and lock time constraint can be tuned through the VCO gain and the charge pump current tuning. So if the VCO gain tends to change (especially at higher frequencies), for having theoretically the optimal solution, the components of the loop filter should change for keeping the same loop bandwidth. Also the terms determined for the stability analysis i.e. the phase margin and the loop bandwidth lead to the parameters characterizing the transient response of the PLL: the damping factor ζ that defines how the output frequency functions of the time of the PLL converges on the final frequency targeted [31] fig. 3-11, and the natural frequency ω_n that with the help of ζ permit to determine/verify the lock time of the PLL [30] chap.16.

For analyzing the different noise source types at the different places in the loop, a PLL noise model can be determined as shown in the next figure. The different power spectral densities of the noise sources S are determined from the characteristics of each PLL sub-block:

- the corner frequencies of each slopes of the function block phase noise and the corresponding noise at that frequency for the VCO and the reference
- the phase noise referred to the comparison frequency for the dividers and the PFD
- the charge pump noise current, minimum pulse length and leakage current for the CP.

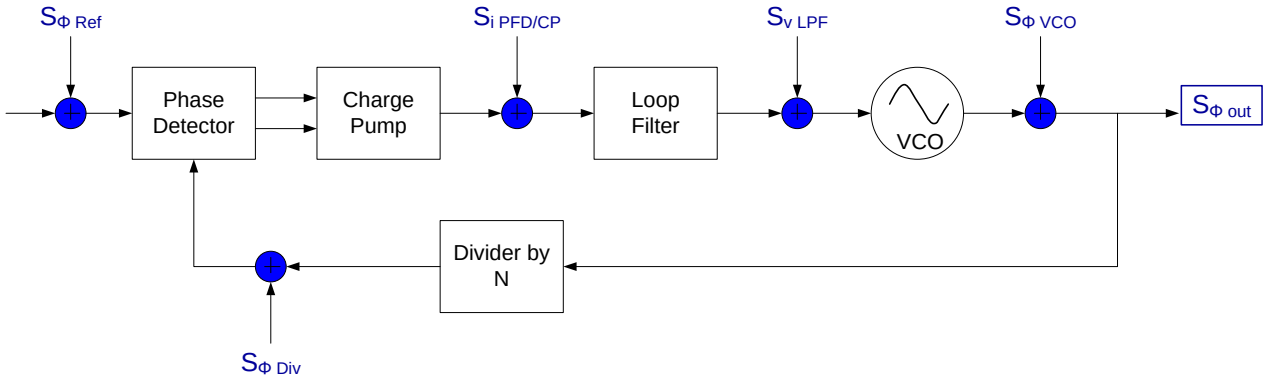


Figure I.2-1: PLL noise model with SΦ phase noise, Sv voltage noise and Si current noise

While the different noise sources are known, their individual contribution on the output phase noise $S_{\Phi\ out}$ can be determined using the table below from [32] indicating the different noise transfer functions and they behaviour.

Table I.2-I: Noise transfer functions of the different noise source of the PLL

Noise source	Noise transfer function	Type	Comment
Input phase noise	$\frac{S_{\Phi out}}{S_{\Phi Ref}} = \left\| N \frac{W(j\omega)}{1+W(j\omega)} \right\|^2$	Low pass	Reference noise usually dominates in-band noise.
PFD/ charge pump noise	$\frac{S_{\Phi out}}{S_{i\,PFD/CP}} = \left\| \frac{N}{K_\varphi} \frac{W(j\omega)}{1+W(j\omega)} \right\|^2$	Low pass	Depends on quality of PFD & CP. CP noise decreases when increasing CP current
Loop filter noise	$\frac{S_{\Phi out}}{S_{vLPF}} = \left\| \frac{K_{vco}}{j\omega} \frac{1}{1+W(j\omega)} \right\|^2$	Band pass	Decreases when increasing CP current because loop filter impedance decreases
VCO noise	$\frac{S_{\Phi out}}{S_{vVCO}} = \left\| \frac{1}{1+W(j\omega)} \right\|^2$	High pass	VCO dominates out-of-band noise
Divider noise	$\frac{S_{\Phi out}}{S_{\Phi Div}} = \left\| N \frac{W(j\omega)}{1+W(j\omega)} \right\|^2$	Low pass	Low noise requires taking the output only after a few 2/3 cells

Then the total noise at the VCO output can be expressed as:

$$S_{\Phi out} = S_{\Phi Ref}\left\|N\frac{W(j\omega)}{1+W(j\omega)}\right\|^2 + S_{i\,PFD/CP}\left\|\frac{N}{K_\varphi}\frac{W(j\omega)}{1+W(j\omega)}\right\|^2 + S_{vLPF}\left\|\frac{K_{vco}}{j\omega}\frac{1}{1+W(j\omega)}\right\|^2 + S_{vVCO}\left\|\frac{1}{1+W(j\omega)}\right\|^2 + S_{\Phi Div}\left\|N\frac{W(j\omega)}{1+W(j\omega)}\right\|^2 \quad \text{[I.2-4]}$$

Some kind of spurs are recurrent in PLL output spectrum, in particular the reference spurs [30] chap.11 due to leakage or mismatch of the charge pump [31] chap.7.3 causes FM modulation then spurs at $f_{VCO} \pm k \times f_{Ref}$, k integer. In general, the amplitude of these kind of spurs are below -60dBc from the VCO carrier.

I.2.2. PLL Design Specifications: Importance of Spurs, Pulling and Pushing Effects

Injection pulling, frequency pulling or pulling is an undesired phenomenon due to the injection of an interfering signal to an oscillating system that causes spurs and harmonics addition on its output spectrum. This phenomenon is attributed to coupling phenomenon [70] of the frequency synthesizers of an RF emitter/receiver to functions blocks in their vicinity.

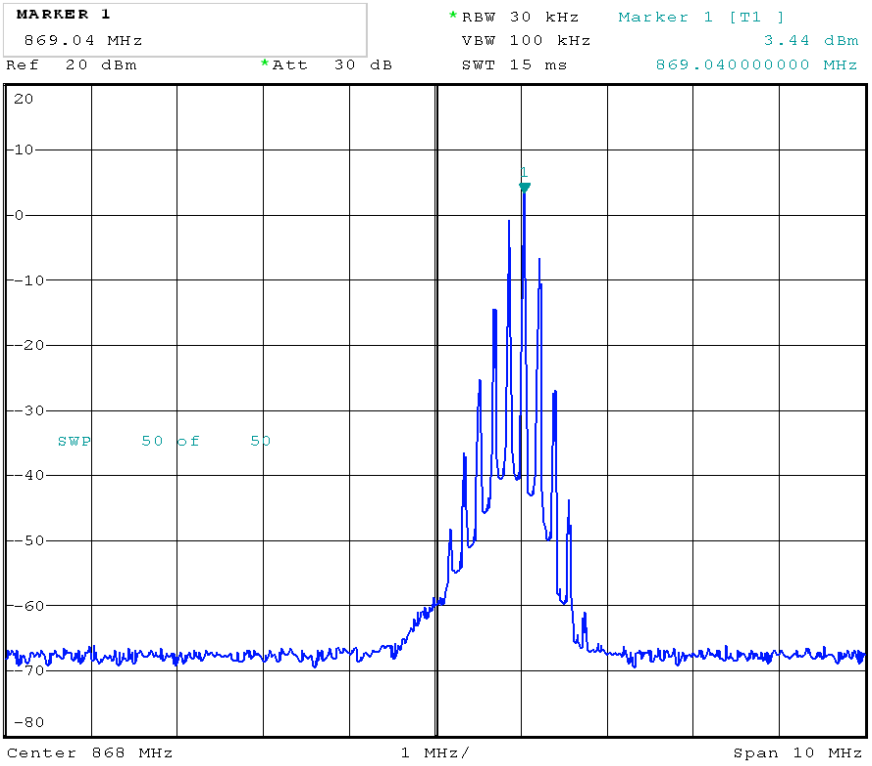


Figure I.2-2: Output spectrum of frequency pulling when a single tone at 869MHz is expected

The higher the injection level, the more the number and the amplitude of the spurs damaging the spectrum purity of the oscillator until locking phenomenon [63]-[72] to the frequency of the injected signal is achieved.

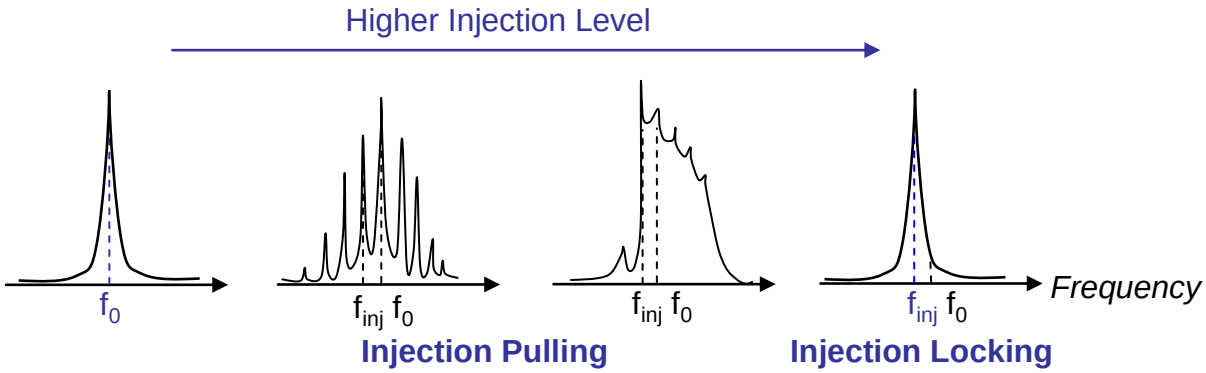


Figure I.2-3: Evolution of the output spectrum of an oscillator under injection

Since Adler in 1946 [63] several approaches where developed for the study, the analysis and the evaluation of the frequency pulling effects. In the following paragraph, we will detail the available techniques of frequency pulling modeling and analysis.

a. Available Techniques for Pulling Modeling and analysis

Spice-like simulations

Analysis of injection pulling can be carried out through Spice-like simulation. Transient or large signal analysis such as Harmonic Balance [83] can highlight the effect of a signal injection on an oscillator.

While inserting a sinusoidal interfering signal of frequency around 100MHz to the supply voltage of a free running VCO, the transient simulation of the circuit leads to pulling or more precisely pushing phenomenon. The result is the same for VCO integrated in a PLL [87]. In addition, while injecting a periodical signal at the DC tuning voltage of the VCO [27] Sec 7.3, or at its output or also at the tail current of the VCO transistors [70]; the simulation of the circuit also leads to frequency pulling phenomenon at the output spectrum of the VCO.

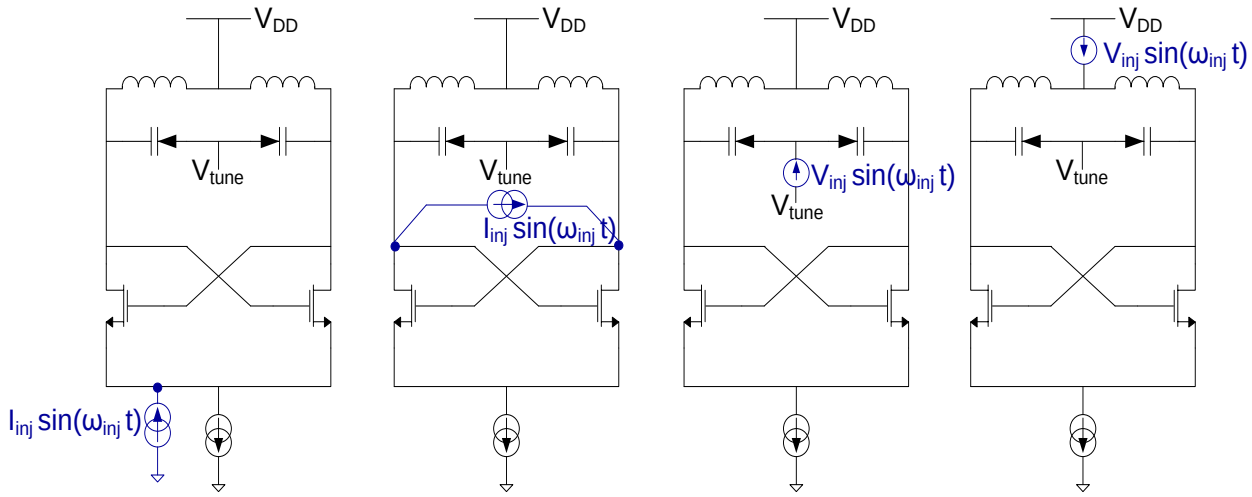


Figure I.2-4: Examples of injection pulling of an LC-oscillator

However, transistor-level circuit simulation may be extremely demanding in terms of CPU and execution time. Therefore different methods of predicting pulling issues were derived.

Analytical Method

► Adler's equations : Derivation of the phase rotation as a function of time

Let an oscillator of free running frequency ω_0 and amplitude V_{osc} be disturbed but not locked by an external signal of frequency ω_{inj} and amplitude V_{inj}. Periodic variations of frequency and amplitude -beat note- can be observed: the output signal of the oscillator under injection is frequency modulated and the carrier frequency becomes ω_{inj} instead of ω_0.

$$V_{out} = V_{out}(t) \cdot \cos\left(\omega_{inj} \times t + \Delta\varphi(t)\right) \quad \text{[I.2-5]}$$

For LC oscillators, Adler in [63] derived a differential equation that governs the oscillator phase as a function of time:

$$\frac{d\Delta\varphi(t)}{dt} = -\frac{V_{inj}}{V_{osc}} \cdot \frac{\omega_0}{2Q} \sin\left(\Delta\varphi(t)\right) + \Delta\omega_0 \quad \text{[I.2-6]}$$

With $d\Delta\varphi/dt$ the instantaneous "undisturbed" angular beat frequency, $\Delta\omega_0 = \omega_{osc}(t) - \omega_{inj}$, Q the quality factor of the LC-tank.

When the oscillator is in steady state, locked to the external injection signal and $d\Delta\varphi/dt = 0$, the beat frequency vanishes and the locking condition for synchronisation is:

$$\frac{V_{inj}}{V_{osc}} > 2Q \left| \frac{\Delta\omega_0}{\omega_0} \right| \quad \text{[I.2-7]}$$

► Output spectrum of Oscillators under injection

For unlocked oscillator under injection where $d\Delta\varphi/dt \neq 0$, the output spectrum of pulled oscillators was explained by Stover [72] through expansion on powers of a small parameter equal to one when the oscillator becomes locked. Armand in [73] expanded the phase modulation signal on a Fourier series.

Before that the output carrier of the oscillator is pulled from its free-running frequency to a new value that catches up with ω_{inj}, pulling spectrum with very non-symmetric sideband distortion around the carrier is obtained as experimental observations.

LC Oscillator Circuit and Injection

► Kirchhoff's Current Law in LC- oscillator under injection pulling

Influence of an injected current in a LC parallel tank can be analyzed through conceptual LC oscillator and transconductor fundamentals. The periodic waveforms of the signals are derived and Kirchhoff's Current Law (KCL) at the output node can be expressed leading to Adler's equations for weak injection or generalized Adler's equations for any injection leading to a compact differential equation of phase [74][76].

► Behavioral model simulation

Through KCL a differential equation governing the output voltage of the oscillator under injection is obtained. Behavioral model simulation with Simulink can predict the frequency-pulling effects on a differential *LC*-tank oscillator and an outphasing wireless transmitter was developed in [76] to predict how parasitic pulling affects the output of transmitters.

► Feedback oscillatory system under injection

Razavi in [69], [70], [75] considers a feedback oscillatory system where the injection is modelled as an additive input of the LC-oscillator. The output is represented by a phase-modulated signal having a carrier frequency tracking the input. To determine the effects the injection on the phase and envelope of the oscillator output, the output of the adder (Vx signal) in Figure I.2-5 is derived analytically and when travelling through the LC tank, the

signal experiments a phase shift leading to a differential equation on the output phase φ(t) (eq.24 to 28 of [70]) equivalent to Adler's equation.

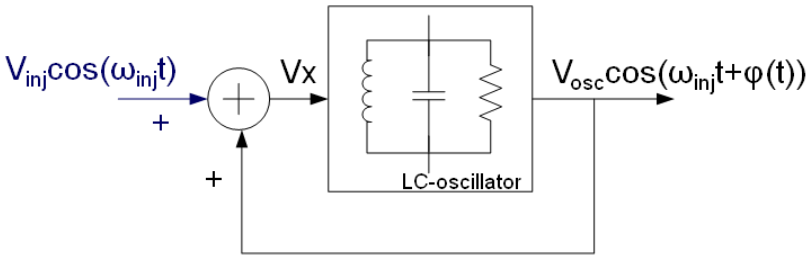


Figure I.2-5: Razavi's LC-oscillator under injection

Graphical analysis of Adler's equations [70] leads to phase variation of injection pulling as function of time. The output spectrum of the pulled oscillator reveals that most of energy is confined to the range [ω_{inj} $\omega_0+\omega_L$], ω_L being the angular frequency locking range, and the magnitude of the sidebands spurs drops approximately linearly on a logarithmic scale as described in [72]and [73].

Perturbation Projection Vector (PPV)

In order to avoid the analysis of a specified type of oscillator, an hybrid numerical-analytical approach was followed-up to predict the occurrence of injection locking and pulling [67],[71], [77]-[82] based on perturbation projection vector (PPV) where an autonomous oscillator perturbed by a small injected signal is governed by a system of differential equations.

Through an analytical analysis of the PPV macromodel derived, the evolving time shift of the perturbed phase of the free running oscillator is governed by an equation similar to Adler's one and leading to generalized Adler's Equation [79] that can be applied for LC but also ring oscillators.

The perturbed response is expressed as follows:

$$x_p(t) = X \cdot \cos(\omega_0 t + \varepsilon(t)) \qquad \text{[I.2-8]}$$

with ε(t) the excess phase. If ω_{inj} approaches more and more ω_0, ε(t) should contain a term that varies linearly with time [71] and is expressed as following [82]:

$$\varepsilon(t) = \Omega_s t + E \cdot \sin(\beta t) + F \cdot \sin(2\beta t) \qquad \text{[I.2-9]}$$

where Ω_s is the slope of the linearly varying term and corresponds to the induced frequency shift, whereas E, F, and β are the parameters that determine the bounded periodically varying component of the excess phase. Through series expansion in Bessel functions of X_p using equation [I.2-9], frequency pulling expression as a function of amplitude perturbation and frequency detuning can be derived. Time-domain phase response of any kind of oscillators under injection can also be evaluated.

Injection pulling in Phase-Locked Oscillators

Since oscillators are usually phase-locked, analysis of pulling should be placed in the context of PLLs.

For that, Razavi [70], [74] assumed that the voltage controlled oscillator has a gain of K_{VCO} and replaced ω_0 by $K_{VCO} \cdot V_{cont}$ in his feedback oscillatory system under injection, then in its output phase differential equation. The transfer function of the PLL leads to the control

voltage time variation functions of PFD, CP and RC loop filter, leading to φ(t) expression (a sinusoidal modulation) functions of the PLL parameters.

For Li et al. [85][86] PLL , because of its oscillator nature, is subjected to interferences that could induce pulling. Their analysis was made in frequency domain to derive PLL under injection transfer function which has a band-pass magnitude response and in discrete-time domain to find the numerical solution of Adler's equation by linking the control voltage of the VCO to the equivalent injection-induced signal; spectra of LO pulling effects can then be determined through the VCO output waveform.

b. Proposed Solutions in the Literature

Positive use of injection-locking

If the spurious spectrum of injection pulling is an unwanted and un-expectable phenomenon, on the other side injection locking can be very useful when controlled. Indeed, frequency synchronization of an oscillator by applying an external signal can be useful in frequency synthesizers, quadrature oscillators [91] [70], low-power microwave phased-arrays and shifters [90][70], frequency dividers or multipliers [90][70][74] etc as presented in [88]. Injection-locked oscillators can benefit from the phase noise reduction [69]-[70] of the injected signal and from the reduction of the applied power due to the weak amplitude of signals involved.

Pulling effects reduction

The main solutions for pulling effects reduction remain the minimization of magnetic couplings by spacing sufficiently sensitive blocks [75], placing grounded guard [75], or using other substrate isolation techniques [92]-[94].

I.3. Context and Originality of the Proposed Contribution

I.3.1. Motivation

Root causes of pulling and locking within PLLs are generally assumed to be the VCO. In the published literature, very limited analysis of the effects of the other PLL function blocks as phase-frequency-detector, charge-pump and loop filter on pulling and locking mechanisms are proposed. Traditionally, circuit performances are basically evaluated from intensive measurement characterization, in general without single system-level simulation and verification.

Hence, the necessity appears for developing a predictive analysis methodology in order to prevent coupling effects that can lead to pulling issues, before the measurement and evaluation steps of the IC.

However, during the design and simulation steps, systematic derivation of behavioral models of active blocks (VCO, PFD, etc) for having a first guess approximation of signal variations where nonlinear effects are taken into account remains very challenging for available simulation tools and methodologies. Also, during co-simulation, there is still a lack of unified active and passive co-simulation. Difficulties to couple digital and analog circuits in single simulation environment are also not easy to deal with.

Once the principal function blocks are designed separately, available design methodologies generally tackle the analysis of pulling and pushing effects generally following cascade-based approaches. Yet these approaches generally ignore electromagnetic couplings and interferences between IC blocks, package and PCB. Thus, potential interactions of IC with package and PCB are most of the time ignored restricting main analysis to couplings taking place within the chip. In addition, available library components models do not account for inter-block couplings and parasitic couplings between neighbouring blocks. Furthermore, modelling analysis carried out with EM simulations generate S-parameters models which are not easy to use in transient analysis because of lack in DC component values: hence a need for distributed equivalent circuit models derivation for proper DC-analysis and time-domain simulations.

I.3.2. The Derived Methodology for Pulling Issues Analysis

We have seen that analog integrated RF-PLLs are sensitive to various coupling mechanisms (substrate coupling [93][115][116], conducted/radiated electromagnetic interferences, supply noise injections, etc…). Such couplings can lead to noisy signals which couple into PLLs loop and modulate the oscillator both in amplitude and phase. The resulting unwanted amplitude and phase modulation creates sideband spurs around the local oscillator fundamental frequency and its higher order harmonics. These sideband spurs known as frequency pulling effects corrupt the spectral purity of the PLL and jeopardize the system-level global performances as noise spurs level at the output of Phase-Locked-Loops (PLLs) represents essential specification constraints which directly affect global system performances.

To analyze the pulling issues in PLL, we propose a system-level characterization and modeling analysis of frequency pulling effects in PLLs where interaction and influences of chip, package and PCB are taken into account. The proposed modeling methodology at function block-level combines SPICE-based circuit simulation with segregated behavioral models. The behavioral modeling approach incorporates non-linear effects taking place within the PLL (e.g., non linear dependency of VCO oscillation frequency against tuning voltage). This segregated approach permits the versatility of the appropriate abstraction level selection

for the different blocks (transistor-level circuit description, and/or system block description). The flexibility of the model description permits an adaptation of the chosen model to the parameters which influence has to be studied.

The importance of electromagnetic couplings through power supply noise and ground connections is underlined by measurements of redesigned ICs through FIB cutting operations on sensitive design portions. EM couplings are then our principal lead for pulling issues origins.

In addition, we will also discuss the physical interpretation of the observed pulling mechanisms with a behavioral modeling towards a predictive analysis where effects of nonlinear VCO tuning together with the influence of PFD/CP are properly captured.

For the aforementioned objectives the following aspects are considered:

a. To Model Sensitive Active Blocks:

Extension to predictive simulation at system level by including packaging and PCB effects requires proper partitioning methodology [96],[98]. In addition, from a system-level standpoint, engaging a full transient simulation of a complete PLL circuit, with the required convergence of the loop frequency, can be extremely demanding in terms of CPU execution time. Many efforts have been devoted to the derivation of behavioral (macro) modeling approaches with the aim of reducing the complexity while maintaining accuracy comparable to the one obtained with native circuit simulations.

- The initial model building/analysis will be based on global measurement analysis.
- Macro-modeling with Verilog-AMS and Simulink will be applied for system-level analysis.
- And SPICE/Spectre Simulation for limited complex function block models at transistor level will be used.

b. To tackle Co-Simulation Analysis:

- For combining passive RLC models with transistor level IPs, Cadence-Spectre/ADS simulator will be used.
- And while coupling different approaches, the use of Simulink and Cadence together or Spectre and RLC models will be achieved.

c. To account for EM Couplings :

- Full-wave EM simulations are carried out for accurate estimation of couplings between identified sensitive blocks. Time-Domain and Frequency domains EM simulators are benchmarked on practical cases for the analysis.
- Methodology of extraction of equivalent RLC model was developed [99] from the obtained Y-parameters.

I.3.3. The Challenges

To develop the proposed Chip-Package-Board methodologies, some challenges should be underlined.

The co-design of complex systems requires bringing a unified model of the complete design domains (Chip, package and board) into a common design environment in order to perform global design optimisation through different development iterations. Starting, from initial design specification, at top-level electrical simulation of sub-blocks or entire modules efficient synchronization with physical model connectivity should be considered to properly handle Engineering Change Order (ECO). Requirement of common design environment where constraints from Chip level are propagated to package-level and even to board-level results from the necessity to facilitate bridging various design domains (Analog, Digital and Mixed) that used to be driven by different tools/flows.

Transistor level description or behavioral-modeling for particular noisy block could be sufficient in capturing analog active parts intrinsic responses. However for digital dies - generally considered as aggressors (noise injectors)- additional details on their power consumption and dynamic switching activities are important to properly deal with global power and signal integrity analysis and time-budgeting considerations. In the published research work various approaches have been proposed for the estimation of time-domain switching activity profiles for digital active modules, with restriction to microprocessors and micro-controllers. Among such approaches are analytical waveform profile calculation, numerical macro-modeling and/or statistical techniques, and measurement methods [95][113][114].

a. Simulation and Co-Simulation Challenges:

- Because of complexity, it is obvious that full-chip simulation is not possible with available simulation solvers
- We then needed a proper block segmentation methodology.
- To get physical RLC models with passivity and causality requirements, it is not easy with the available simulation tools to extract broadband SPICE-based model, as they are based on narrow band assumptions.

We then needed to develop dedicated extraction methodology.

Accurate evaluation of noise spurs in PLLs constitutes a real challenge for available simulation tools, sign-off verifications being principally carried out experimentally. In addition, most of available simulation solutions are based on small-signal hypothesis.

b. Measurement/Characterization Challenges:

The results of the experimental characterization of an IC are often analyzed using trial-and-error method to find the performance limiting factors and generally lead to partial modifications of identified blocks (e.g., potential noise sources) through cuts and strap of metallizations. During the characterization, here are the challenges:

- With VNA measurement systems, the DC information is missing.
- The spectrum analyzer has limited functionalities: frequency and time domain correlation is very difficult to achieve.
- To access internal nodes of identified blocks, the only solutions are FIBs (Focused Ion Beam) inside an existing IC. Hence importance of BIST (Built-in-Self-Test) architecture solutions [100] in order to access internal nodes of circuits for test and verification.

On the hand although analysis of multi-port systems is accessible with available full-wave simulation tools, experimental measurement and characterization of multi-port systems remains very challenging and requires innovative and robust techniques [109]-[112].

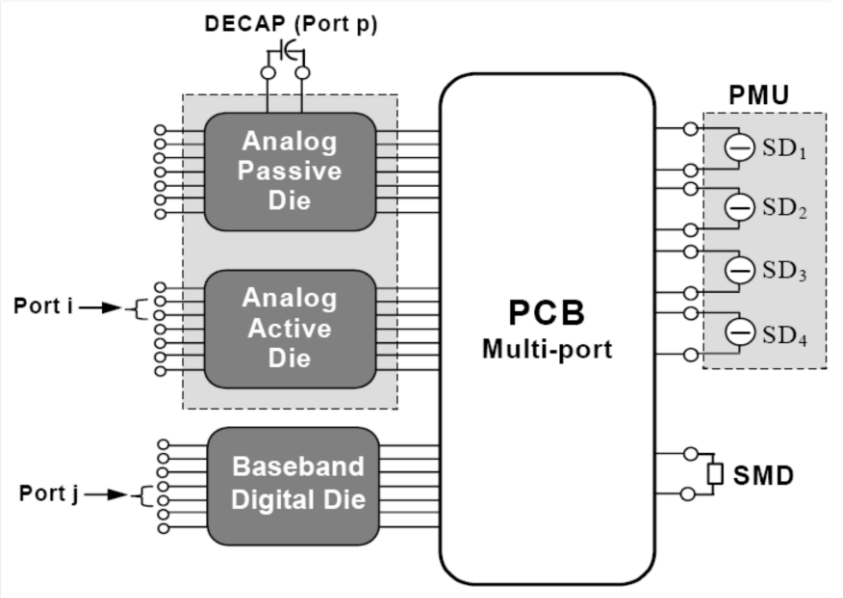


Figure I.3-1: Multi-port schematic view of chip-package-board for Power & Signal Integrity analysis

I.4. Applications Description

In this section, detailed descriptions of system-level carrier applications that may deal with frequency pulling issues are presented. Two distinct application projects will be investigated, one relative to automotive application working around 1GHz (868MHz) and the other one in link with satellite application working at 12 GHz. Main focus will be directed towards analysis and characterization of PLL blocks for both applications.

I.4.1. An Automotive Car Access Transceiver Application around 868MHz: the LoPSTer

In order to illustrate a pulling effect in an integrated RF circuit, we will first discuss an integrated car access transceiver in transmit mode. Indeed, as the signals power levels involved are more important in transmit mode (TX) than in reception (RX), coupling phenomena will be more significant in that way for data transmission. It is the case of the Low Power Single-chip Transceiver LoPSTer characterized in this work: during the experimental characterization of the application including the chip, PCB and monitoring in transmit mode, significant level of pulling was reported in a particular way of communication between the IC and its loading conditions.

a. The LoPSTer's Description and the Automotive Specifications for the LoPSTer

The LoPSTer [101], [102] is a low power transceiver System on Chip (SoC) integrated circuit dedicated initially to automotive application for secure vehicle immobilization and car access, but some internal projects related to medical field also use the LoPSTer solution for wireless communication.

The project started in September 2003 and since, 4 versions of the IC design were developed: the LoPSTer 1, 1.2, 1.23 and 1.25 in order to add some improvements into the design (e.g. on the latch up, the clock spurs, the stability of the PA…).

The LoPSTer was designed with NXP's QUBIC4plus BiCMOS technology permitting 5 levels of stack metallization in the back-end process for a silicon substrate of height 600µm and of resistivity 200Ω.cm. The silicon die of the LoPSTer has a dimension of $2.340 \times 1.880 mm^2$, the die-pad of $3.80 \times 3.80 mm^2$ and the whole solution is integrated into a HVQFN32 package [104].

The LoPSTer's application uses Multi channel TX and RX operation by fully integrated Frac-N ΣΔ PLL with on-chip loop filter to control the Local Oscillator and an automatic VCO sub band selection and calibration to reduce PLL loop bandwidth variation. Its frequency functioning band is included in the ISM (Industrial, Scientific and Medical) bands between 313 MHz and 928 MHz:

- 315 MHz for the US band
- 433 MHz and 868MHz for the European band
- 915 MHz for the Japan frequency band.

It uses programmable FSK, GFSK, ASK/OOK modulations/demodulations and a Manchester or NRZ code of data rate 0.4kBd to 40kBd for a channel bandwidth of 50 to 300kHz.

During the characterization of the LoPSTer in transmit mode, the IC was programmed to operate at 868MHz, at the local oscillator frequency divided by 2. The elements of the IC considered in the TX part are emphasized in Figure I.4-1, Figure I.4-2 and Figure I.4-3.

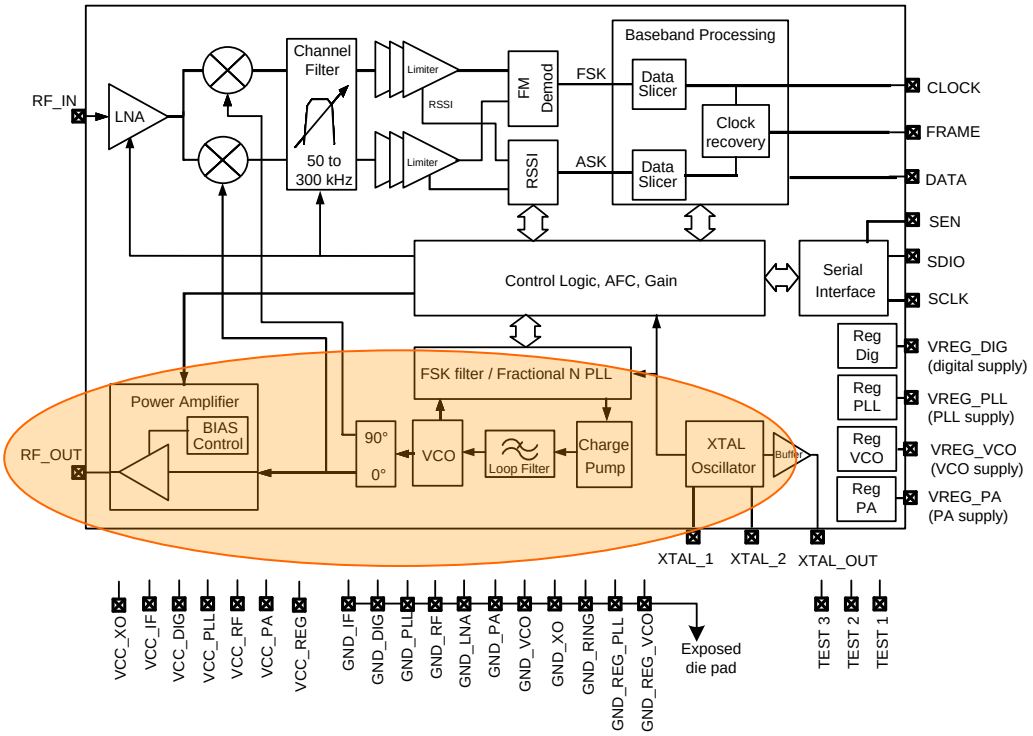


Figure I.4-1: LoPSTer's functional block diagram and highlighted TX part

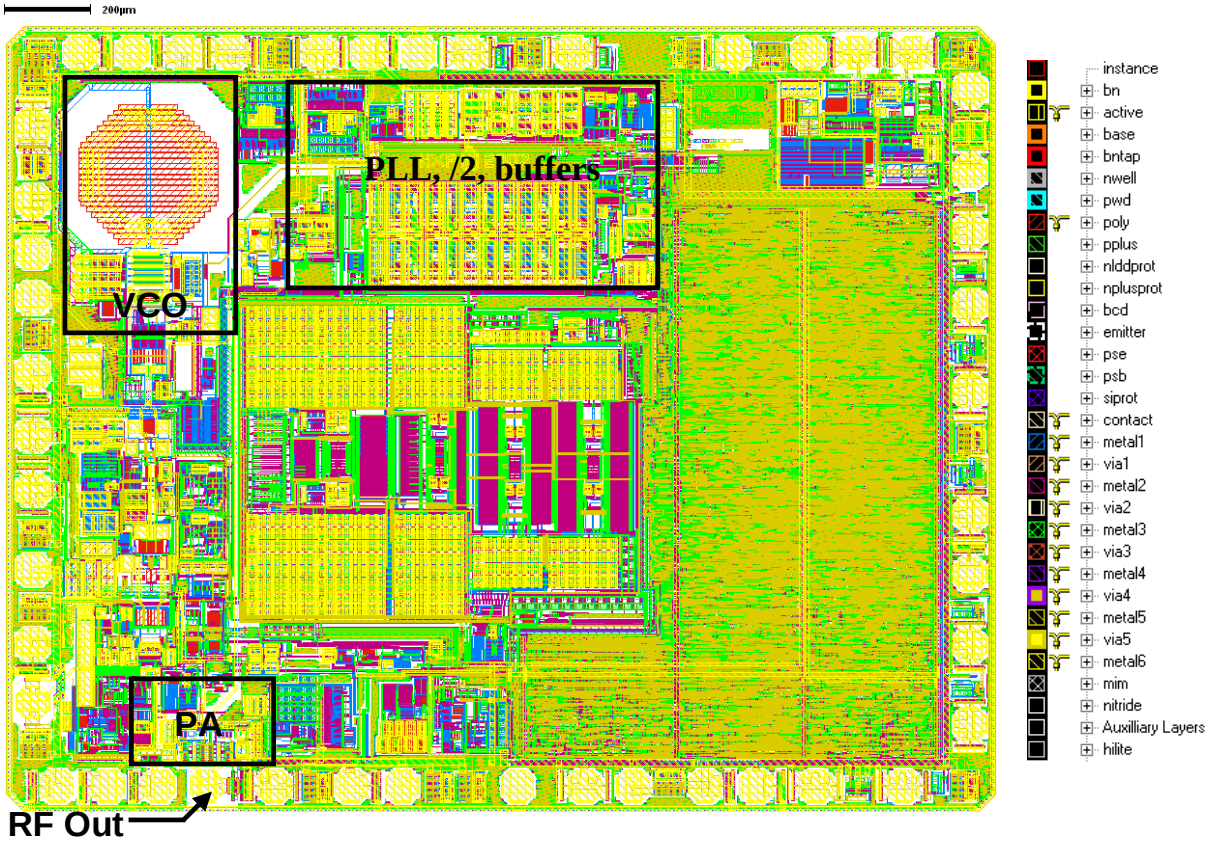


Figure I.4-2: LoPSTer's Layout and TX part elements

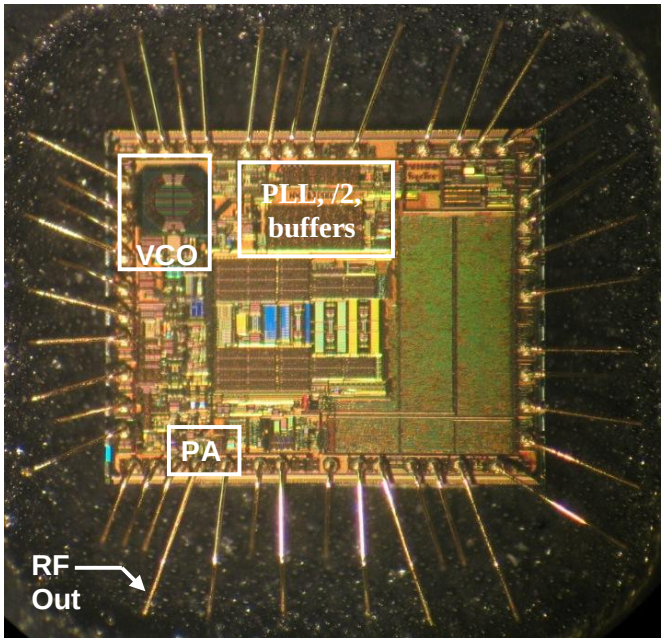
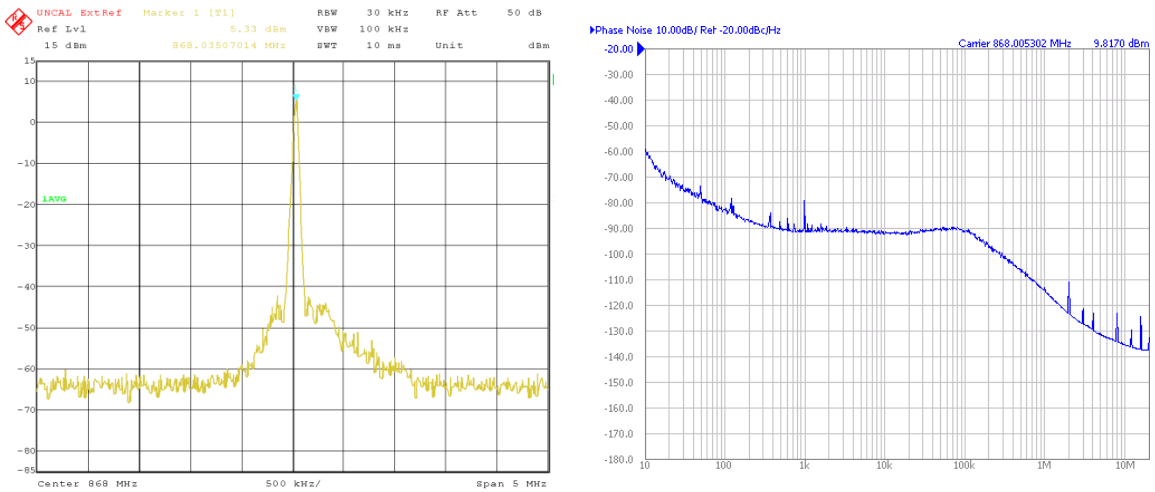


Figure I.4-3: Top-view microphotograph of investigated chip design and TX part elements

To complete the test measurement characterizations, the IC is reported on its associated PCB test board that contains discrete components of decoupling and matching network, for example for the PA in TX mode.

For the LoPSTer's characterization achieved, the output signal of the adapted power amplifier is specified to deliver sinus signal of 10dBm maximum power +/-1dBm at 868MHz for a load charge of 50Ω. The phase Noise at 868MHz TX output is -86dBc/Hz at an offset of 50kHz from the carrier frequency, -86dBc/Hz at 100kHz offset, and -107, dBc/Hz at 1MHz offset, -115 dBc/Hz at 2MHz offset, -125dBc/Hz at 5 MHz offset and -130 dBc/Hz at 10 MHz offset for a PLL charge pump current of 30µA.The monitoring of the transmit system is achieved with an I2C bus for real time measurement through a spectrum analyser (reference Rohde & Schwartz FSP7) or a signal source analyzer (Agilent E5052A for phase noise measurement) replacing the antenna load.



(a) **(b)**

Figure I.4-4: Output spectrum (a) and phase noise (b) of the LoPSTer's board output signal at 868MHz

The chip-package-PCB output signal of the LoPSTer, first carrier application analyzed, fulfils the product specification.

b. The LoPSTer in an Edible Capsule for Continuous Measurement of Core Body Temperature

The LoPSTer IC is also used in a healthcare business innovation product: its association with a sensor and a microcontroller in a system-in-package solution is integrated in an edible capsule meant to communicate in real time the body temperature of the patient.

Figure I.4-5 illustrate a medical application where the LoPSTer circuit is used for the RF aspects providing wireless measurement of temperature monitored in real time.

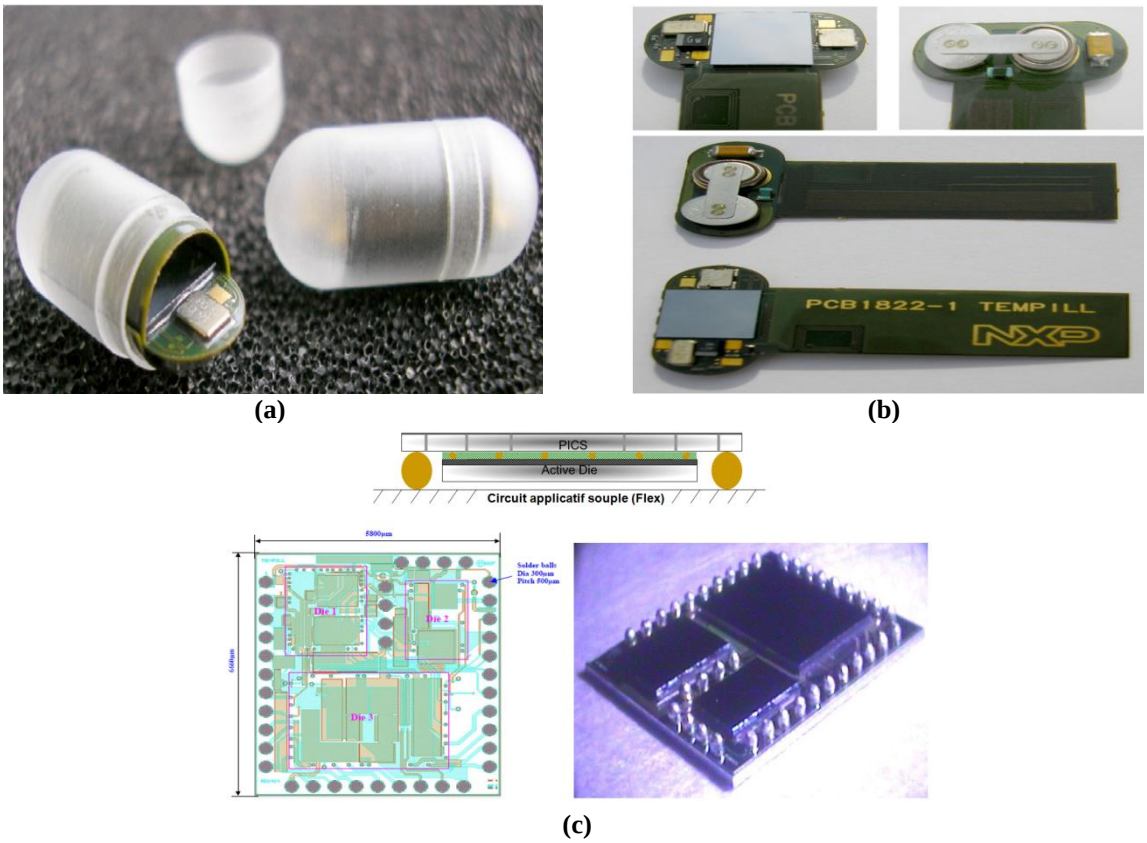


Figure I.4-5: View of developed medical capsule using NXP-Semiconductor LoPSTer circuit (a) view of flexible substrate integration system with battery (b), and system-in-package architecture solution (c).

I.4.2. A Microwave Down-Converter for Satellite TV Application around 10-12GHz: the TFF1014

a. The TFF1014's Description and the microwave constraints

The TFF1014 is a microwave down-converter for satellite TV receiver applications [105]. This Low-Noise Block (LNB) function is to convert the antenna microwave signal in the range of 10.7-12.75GHz down to a satellite TV Intermediate Frequency (IF) band in the range of 950-2150MHz. Figure I.4-7 shows the block diagram of TFF1014 highlighting its differential PLL block diagram that consists of [105]:

- an RF LC-tank VCO combined with an Automatic Level Control (ALC) circuit of oscillation frequency f_{LO} = 9.75GHz in the low band or 10.60GHz in the high band. The VCO gain is typically -500MHz/V and the maximum phase noise is -90dBc/Hz (typical -93dBc/Hz) at 100kHz offset from the oscillation frequency.
- VCO buffers which bring the VCO signal as the LO signal to the mixer through a coupled differential transmission lines. Its input impedance is mainly capacitive (60fF typical)

and its phase noise floor should be under -130dBc/Hz at 10MHz offset at its output to the mixer or to the divider.

- An RF frequency divider that divides the LO frequency (between 8.5 and 12GHz) down to the Reference frequency (between 19 to 32 MHz). The division range is the between 384 and 446 and the phase noise at the output to the PFD is -149dBc/Hz for an offset ≥10kHz from 25MHz.
- A Phase Frequency Detector (PFD) followed by a Charge-Pump and a loop RC filter are partly externals. The whole block takes the output signals from the XO block and from the RF divider.
- A Crystal oscillator (XO) followed by the XO buffer amplifier delivers the Reference signal to the PFD; the crystal resonator being an external function, fref= 25MHz and the quality factor of the motional branch should be 50000. The maximum phase noise at its output to the PFD is -146dBc/Hz at an offset superior to 10kHz (typically -149dBc/Hz at an offset ≥10kHz from the crystal frequency).

The Local Oscillator global phase noise when the PLL is locked should be: -86 dBc/Hz at 10kHz offset, -89 dBc/Hz at 100kHz offset, -107 dBc/Hz at 1MHz offset and -130 dBc/Hz at ≥10 MHz offset from f_{LO}.

The other functional blocks of TFF1014 constitute the RF down-converter that consists in an LNA, a mixer and an IF amplifier, all placed in the upper part of the block diagram given in Figure I.4-7(a).

The TFF1014 was designed in NXP's QUBIC4X BiCMOS technology. The die size must be 1mm^2 maximum to meet cost target, the package proposed for TFF1014 is DHVQFN16-2.5x3.5mm^2 and offers a die pad of 1.2 x 2.2mm^2.

The release for production is scheduled for Q3 2010.

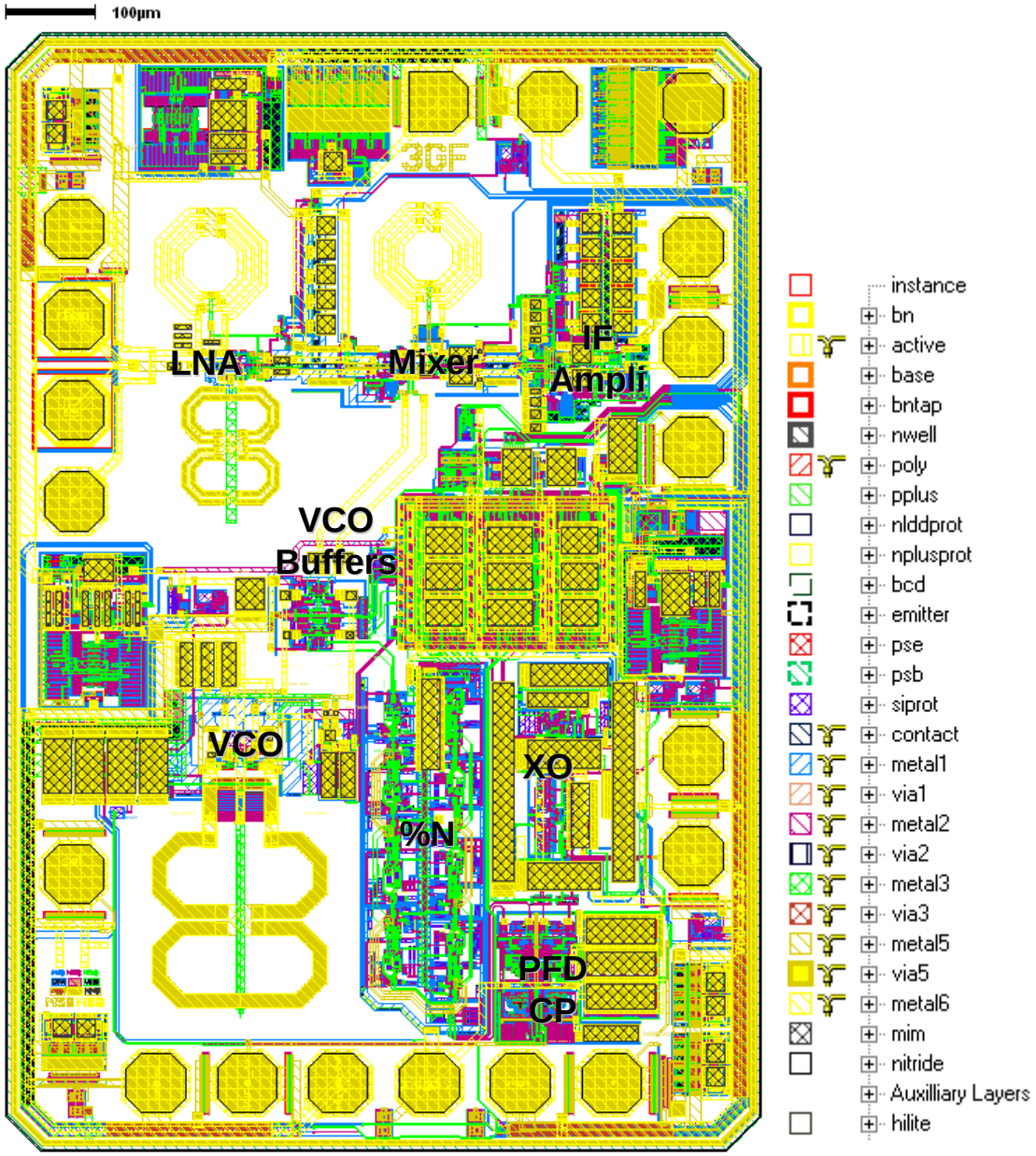
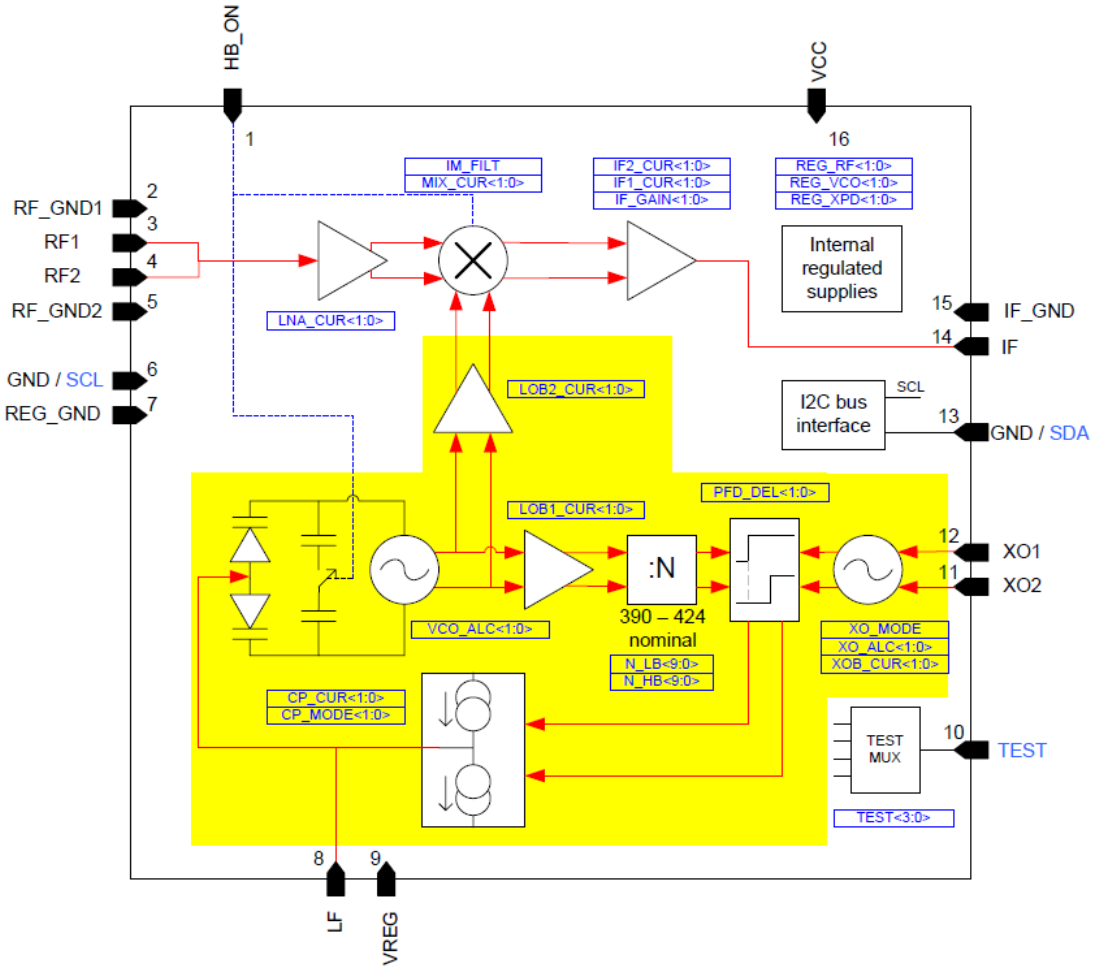
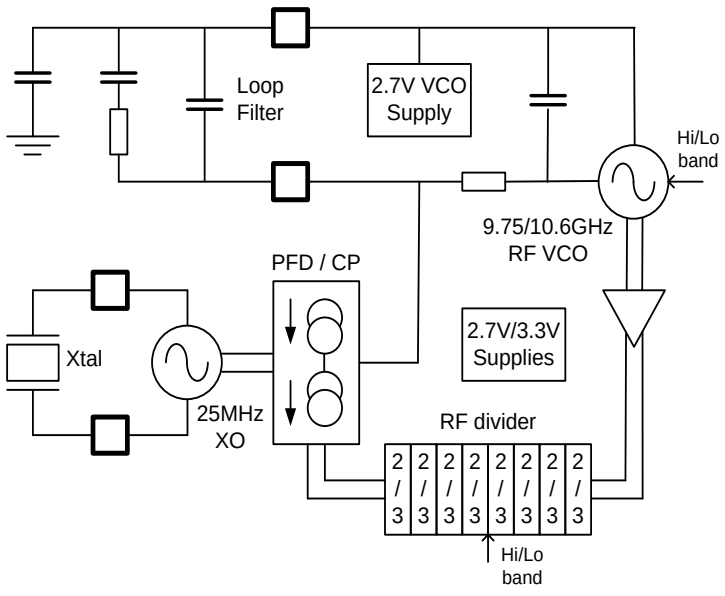


Figure I.4-6: TFF1014 layout and principals functional blocks



(a)



(b)

Figure I.4-7: Block diagram of TFF1014 and PLL elements highlighted (a) and its PLL architecture (b)

TFF1014 PLL characterization was made by observing the spectrum at IF output after mixing with an RF signal of high spectral quality. The PLL spectrum is given in Figure I.4-8. Despite compact layout and small number of ground pads, spurs at multiple of the 25MHz reference frequency are under -65dBc.

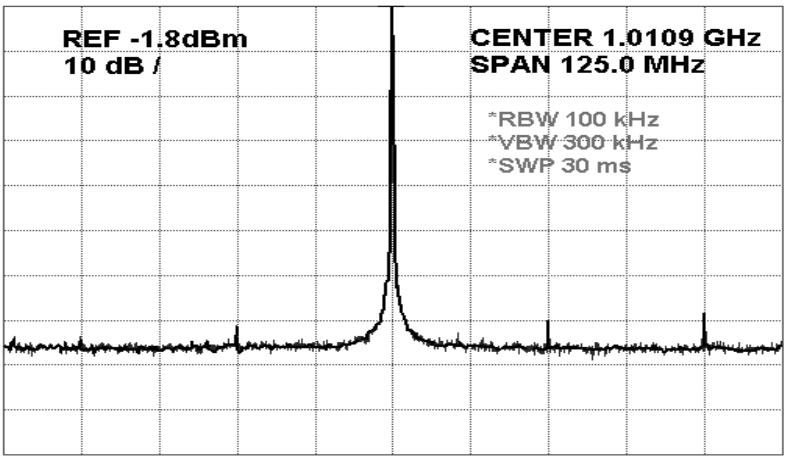


Figure I.4-8: Wideband spectrum of the TFF1014 PLL

The PLL phase noise characteristic in low band using nominal loop filter is showed in Figure I.4-9. The close-in noise is about -90dBc in average over 10kHz-100kHz range where the VCO remains the dominant contributor despite the attenuation of its noise by the PLL (at 100kHz offset, the VCO achieves typically -93dBc/Hz) .

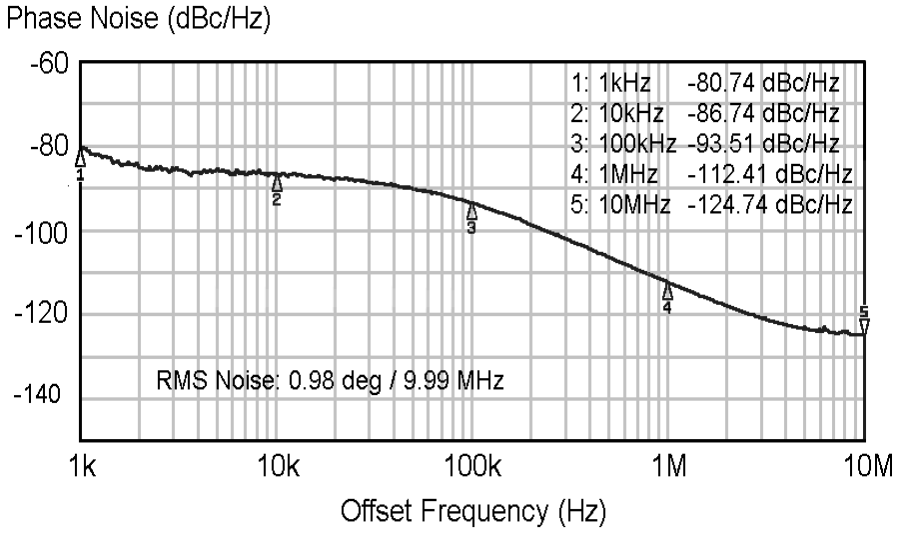


Figure I.4-9: TFF1014 PLL phase noise

I.5. Synthesis and Concluding Remarks: Necessity of deriving global Methodologies for Behavioral Modeling of PLL Frequency Pulling

Phase Locked Loops are one of the basic, essential, and sensitive functions of an RF IC. These building bricks may be bothered by the other neighbouring blocks at component-level, function block-level or global system-level through EM coupling phenomena and cause an output spectrum alteration in terms of additive spurs, phase noise and/or amplitude and frequency deviation of the initial tone called "VCO/PLL frequency pulling".

In this chapter, we set out the different current methods and techniques of analysis for PLL modeling. The detailed various methods cannot however deal with pulling issues as the coupling notion is very hard to estimate and to insert into the analysis.

From the state of the art made on PLL analysis, we proposed global methodology for frequency pulling analysis based on a system level analysis that include couplings in which the VCO of the PLL is involved as well as the different function blocks of the PLL that can have effects on pulling issues. The derived modeling methodology at function block-level combines SPICE-based circuit simulation with segregated behavioral models.

Practical studies are carried out with two main applications:

- The LoPSTer, which is an automotive application working at 868MHz on which at a particular transmission mode, couplings of the VCO/PLL with the neighboring blocks induce frequency pulling issues. To go more in detail on the probable causes of pulling and its ways of manifestations, we will carry out an experimental characterization and an analysis of the frequency pulling effects in PLLs application with the LoPSTer case.
- The TFF1014 is an on-going project of satellite application in the Ku Band. Our objective is to apply the methodologies of analysis developed with the previous case during the different steps of the IC design. First measurement of TFF1014 circuit showed excellent performances and represents state of the art down-converter solutions for low-noise and low-power applications [23].

The proposed Chip-package-Board PI/SI Co-simulation methodology [108] combined two model extractions as depicted in Figure I.3-1:

1. A passive network multi-port that includes all relevant power/ground planes, interconnects, bond-wire connections, RDL, traces.

2. A behavioral model of the digital baseband die switching activity, the analog blocks being represented by transistor level description or equivalent model reductions.

The accuracy of the passive network model extraction strongly depends on the used assumption: full-wave or quasistatic. Other important challenges concern partitioning of the overall system into sub-blocks, grounding strategies as how to properly define current return paths. To model the active dies, essential question is how to define a realistic current switching activity profile [95].

Bibliography of Chapter I

[23] P. Philippe, S. Bardy, S. Wane, F. Moreau, and L. Praamsma, “A Low Power 9.75/10.6GHz PLL in SiGe-C BiCMOS for Ku-Band Satellite LNBs,” in 14th European Microwave Integrated Circuits (EuMIC), Manchester, UK, 9th - 14th October 2011.

[24] N. O. Sokal, “Class-E High-Efficiency RF/Microwave Power Amplifiers: Principles of Operation, Design Procedures, and Experimental Verification,” chapter (pp. 269-301) in book Analog Circuit Design - Scalable Analog Circuit Design, High-Speed D/A Converters, RF Power Amplifiers, Kluwer Academic Publishers, Dordrecht, The Netherlands, 2002, ISBN 0-7923-7621-8.

[25] R. E. Best, “Phase Locked Loops: Design, Simulation, and Applications”, 5th ed., McGraw-Hill Education, 2003.

[26] R. E. Best, “Phase Locked Loops: Design, Simulation, and Applications”, 3rd ed., McGraw-Hill Education,1997.

[27] B.Razavi, "RF microelectronics”, Prentice Hall, pp. 206-295, December 1997.

[28] J. Rogers and C. Plett, "Radio Frequency Integrated Circuit Design," Artech House Inc., 2003.

[29] B. Razavi, “Devices and circuits for phase-locked systems,” in Phase- Locking in High-Performance Systems, From Devices to Architectures, B. Razavi, Ed. Piscataway, NJ: IEEE Press, 2003.

[30] D. Banerjee, “Pll Performance, Simulation, and Design “, 4th ed., Dog Ear Publishing, Aug. 2006.

[31] K. Shu and E. Sanchez-Sinencio, “CMOS PLL Synthesizers: Analysis and Design”, The Springer International Series in Engineering and Computer Science, Vol. 783, 2005, ISBN: 978-0-387-23668-1.

[32] P. Philippe, “Frequency synthesis & phase-locked loops”, IC-RF Training V3, May 2010
M. H. Perrot, “Behavioral Simulation of Fractional-N Frequency Synthesizers and Other PLL Circuits”, IEEE Design & Test, vol. 19, Issue 4, pp. 74 – 83, July 2002.

[33] “Virtuoso Spectre Circuit Simulator RF Analysis User Guide”, Product Version 7.2, December 2009, Cadence Design Systems, United States of America.

[34] T. J. Aprille and T. N. Trick, “Steady-state analysis of nonlinear circuits with periodic inputs,” Proc. IEEE, vol. 60, pp. 108–114, Jan. 1972.

[35] “RF Analysis with Virtuoso Spectre Simulator”, Lecture Manual, Version MMSIM 7.2, April 2, 2010.

[36] “Virtuoso® Spectre® Circuit Simulator Reference“, Product Version 7.2, December 2009, Cadence Design Systems, United States of America.

[37] R. Telichevesky, K. Kundert, “Receiver characterization, using Periodic Small-Signal Analysis”, in Proc. of the IEEE Custom Integrated Circuits Conf., pp. 449-452, May 1996.

[38] El-Rabaie, S., Fusco, V. F, Stewart, C., “Harmonic balance evaluation of nonlinear microwave circuits - a tutorial approach” , EEE Transactions on Education, vol. 31, issue 3, pp. 181-192, Aug. 1998.

[39] “IEEE Standard for Verilog® Hardware Description Language“, Design Automation Standards Committee of the IEEE Computer Society, IEEE Std 1364™-2005.

[40] “Verilog-AMS Language Reference Manual, Analog & Mixed-Signal Extensions to Verilog-HDL”, Version 2.3.1, June 2009, Accellera Organization, Inc., Napa, California.

[41] “Verilog-A Language Reference Manual, Analog Extensions to Verilog HDL”, Version 1.0, Open Verilog International, Los Gatos, California, August 1996.

[42] D. FitzPatrick and I. Miller, “Analog behavioral modeling with the verilog-A langage” , Kluwer Academic Publishers, 2003, Dordrecht.

[43] http://www.mathworks.com/products/simulink/ .

[44] M. Schetzen, “Power-series equivalence of some functional series with applications”, IEEE Trans. Circuit Theory, 1970, vol. CT-17, pp.305-313.

[45] D. M. Mandelbaum, and S. G. Mandelbaum, “A Fast, Efficient Parallel-Acting Method of Generating Functions Defined by Power Series, Including Logarithm, Exponential, and Sine, Cosine,” IEEE Trans. on Parallel and Distributed Systems, vol. 7, no. 1, pp. 33-45, Jan. 1996.

[46] V. Volterra, ”Theory of Functionals and of Integrals and Integro–Differential Equations”, Dover Publications, Inc., New York, 1959.

[47] N. Carvalho, R. Madureira and J. Pedro, “Prediction of PLL Frequency Discriminator Non-Linear Distortion Using the Volterra Series Approach”, in proc IEEE ISCAS 1996, Vol. 3, pp.229-232, Atlanta, May 1996.

[48] J.C. Pedro, N.B. Carvalho, R.C. Madureira, ” Nonlinear distortion study of FM transmission systems composed by a VCO-PLL association “, in proc. IEEE ISCAS 1997, vol. 2, pp. 957 – 960.

[49] J. C. Pedro, N. B. Carvalho, and R. C. Madureira, "Nonlinear distortion model for VCO-PLL FM transmission systems," IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 46, no. 3, pp. 348-352, Mar. 1999.

[50] http://www.mathworks.com/products/connections/product_detail/product_35807.html

[51] “Task guide of Spectre & Simulink transient co-simulation”, NXP Semiconductors, Application note, Rev. 2.0 , Oct 2007.

[52] N. Jourdan, D. Denis, H. Kampé, “ASSURA RCX-PL: Introduction of parasitic inductances extraction in NXP flow“, NXP Semiconductors Caen, CTO-Process Library & Technology , April 2007.

[53] D. Denis, “Using S parameter files, Using S parameter files with Spectre simulator”, NXP Semiconductors, November 2007.

[54] S. Wane, A. Kuo, “Electromagnetic and thermal co-analysis for distributed co-design and co-simulation of chip, package and board”, IEEE RFIC 2007.

[55] S. Wane, “Partition and global methodologies for IC, package and board co-simulation in SiP applications”, EuMW 2007, Munchen, Oct. 2007.

[56] J.Mao, G. Fitzgerald, A. Kuo, S.Wane, “Coupled analysis of quasi-static and full-wave solution towards IC, package and board co-design”. published in Electrical Performance of Electronic Packaging (EPEP), Atlanta, Oct. 2007

[57] H. Takhedmit, B. Merabet, L. Cirio, B. Allard, F. Costa, C. Vollaire, and Picon, O.: ‘Design of a 2.45 GHz rectenna using a global analysis technique’. 3rd European Conf. on Antennas and Propagation, Berlin, Germany, Mar. 2009.

[58] H. Takhedmit, L. Cirio, B. Merabet, B. Allard, F. Costa, C. Vollaire, and O. Picon, “Efficient 2.45 GHz rectenna design including harmonic rejecting rectifier device,” Electron. Lett., vol. 46, no. 12, pp. 811–812, Jun. 2010.

[59] D. Pasquet, P. Crozat, L. Escotte, B. Huyart, L. Lapierre, O. Llopis, “Mesures en hyperfréquences”, Lavoisier, Paris 2004.

[60] J. Verspecht and D. Root, “Polyharmonic Distortion Modeling,” IEEE Microwave Magazine, vol. 7, no. 3, pp. 44-57, June 2006.

[61] J. Verspecht et al., ”Multi-port, and Dynamic Memory Enhancements to PHD Nonlinear Behavioral Models from Large-signal Measurements and Simulations", Conference Record of the IEEE Microwave Theory and Techniques Symposium 2007, pp.969-972, USA, June 2007.

[62] D. E. Root, J. Verspecht, D. Sharrit, J. Wood, and A. Cognata, “BroadBand, Poly-Harmonic Distortion (PHD) Behavioral Models from Fast Automated Simulations and Large-Signal Vectorial Network Measurements,” IEEE Transactions on Microwave Theory and Techniques Vol. 53. No. 11, November, 2005 pp. 3656-3664

[63] R. Adler, "A study of locking phenomena in oscillators", Proc. Of IEEE, vol.61, no.10, pp. 1380-1385, October 1973

[64] K. Kurokawa, “Injection locking of microwave solid-state oscillators”, Proc. IEEE, vol. 61, pp. 1386–1410, Oct. 1973.

[65] F. M.Gardner, “Phaselock Techniques“, 2d ed., John Wiley and Sons, NY, pp 72-79, 1979.

[66] A.Banai, F.Farzaneh, "Locked and Unlocked Behavior of Mutually Coupled Microwave Oscillators" IEE Proc. Microwave, Antenna and Propagation,Vol.147,No.1,pp.13-18,Feb.2000.

[67] X. Lai and J. Roychowdhury « Automated oscillator macromodelling techniques for capturing amplitude variations and injection locking", In IEEE/ACM International Conference on Computer Aided Design, pages 687.694, November 2004.

[68] X. Lai and J. Roychowdhury., "Analytical equation for predicting injection locking in lc and ring oscillators", Proc. IEEE CICC, September 2005.

[69] B. Razavi, "A study of injection pulling and locking in oscillators", IEEE Custom Integrated Circuits Conf, pp. 305-312, 2003.

[70] B. Razavi, "A Study of Injection Locking and Pulling in Oscillators," IEEE Journal of Solid-State Circuits, vol. 39, no. 9, pp. 1415-1424 , September 2004.

[71] X. Lai, J. Roychowdhury, "Capturing oscillator injection locking via nonlinear phase-domain macromodels," Microwave Theory and Techniques, IEEE Transactions on, vol.52, no.9, pp. 2251-2261, Sept. 2004.

[72] H. L. Stover, "Theoretical explanation of the output spectra of unlocked driven oscillators," Proc. IEEE, vol. 54, pp. 310–311, Feb. 1966.

[73] M. Armand, "On the output spectrum of unlocked driven oscillators," Proc. IEEE, vol. 59, pp. 798–799, May 1969.

[74] A. Mirzaei, M. E. Heidari, and A. A. Abidi, "Analysis of oscillators locked by large injection signals: Generalized adlers equation and geometrical interpretation," in Conference 2006, IEEE Custom Integrated Circuits, San Jose, CA, Sept. 2006, pp. 737–740.

[75] B. Razavi, "Mutual injection pulling between oscillators," Proc. IEEE Custom Integrated Circuits Conf., pp. 675--678, 2006.

[76] M.E. Heidari and A.A. Abidi, "Behavioral models of frequency pulling in oscillators", IEEE Behavioral Modeling and simulation workshop, pp.100-104, Sept 2007.

[77] G. Gangasani and P. Kinget, "Time-Domain Model for Injection Locking in Non-Harmonic Oscillators," IEEE Transactions on Circuits and Systems I, vol. 55, no. 6, pp. 1648 - 1658, July 2008.

[78] M.M. Gourary, S.G Rusakov, S.L. Ulyanov, M.M. Zharov, B.J.Mulvaney, K.K. Gullapalli, "Injection locking conditions under small periodic excitations," Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on, vol., no., pp.544-547, 18-21 May 2008.

[79] P. Bhansali, J. Roychowdhury, "Gen-Adler: The Generalized Adler's Equation for Injection Locking Analysis in Oscillators", Proceedings of the 2009 Asia and South Pacific Design Automation Conference, Yokohama, Japan, January 2009.

[80] A. Demir and J. Roychowdhury, "A reliable and efficient procedure for oscillator PPV computation, with phase noise macromodeling applications," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 22, no. 2, pp. 188–197, Feb. 2003.

[81] T. Mei and J. Roychowdhury, "PPV-HB: Harmonic balance for oscillator/PLL phase macromodels," in Proc. IEEE Int. Conf. Comput.- Aided Des., Nov. 2006, pp. 283–288.

[82] P. Maffezzoni, D. D'Amore, "Evaluating Pulling Effects in Oscillators Due to Small-Signal Injection"', Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. 28, no. 1, pp. 22-31, January 2009.

[83] J. Dominguez, A.Suarez, S. Sancho," Semi-analytical formulation for the analysis and reduction of injection-pulling in front-end oscillators ", Microwave Symposium Digest, MTT '09. IEEE MTT-S International , June 2009.

[84] A Mirzaei, A.A. Abidi, "The Spectrum of a Noisy Free-Running Oscillator", Circuits and Systems IIEEE Transactions on, vol. 57, no 3, pp. 642 – 653, March 2010.

[85] C.-J. Li, C.-H. Hsiao, F.-K. Wang, T.-S. Horng, and K.-C. Peng, "A rigorous analysis of local oscillator pulling in frequency and discrete time domain" in Proc. IEEE Radio Freq. Integr. Circuits Symp. Dig., pp. 409–412, 2009.

[86] C.-J. Li, C.-H. Hsiao, F.-K. Wang, T.-S. Horng, and K.-C. Peng, "A Rigorous Analysis of a Phase-Locked Oscillator Under Injection ", Vol. 58,no. 5,pp. 391 – 1400, May 2010.

[87] M. Ranaivoniarivo, S. Wane, E. Richalot and O. Picon, “A System-Level Non-linear Behavioral Modeling of Pulling and Pushing Mechanisms in PLLs”, APCCAS 2010, Dec. 2010, Kuala Lumpur.

[88] R. Harjani, “Fun with Injection Locking”, APCCAS 2010, Dec. 2010, Kuala Lumpur.

[89] S. Patnaik, N. Lanka, and R. Harjani, “A dual-mode architecture for a phased-array receiver based on injection locking in 0.13µm CMOS,” IEEE ISSCC, pp. 490–491,491a, Feb. 2009.

[90] S. Patnaik, R. Harjani “A 24-GHz Phased-Array Receiver in 0.13um CMOS using a 8-GHz LO”, IEEE RFIC, pp. 465, Jun. 2010.

[91] N. Lanka, S. Patnaik, R. Harjani “A Sub-2.5ns Frequency-Hopped Quadrature Frequency Synthesizer in 0.13-um Technology”, IEEE CICC,pp. 57–60, Sept. 2009.

[92] S. Kapora, J. Bakker, “Guidelines for substrate noise isolation”, Research / Design Methods and Solutions, NXP Semiconductors, Design Technology User Meeting, Feb. 2007.

[93] S. Wane, D. Bajon, “Full-wave analysis of Inhomogeneous Deep-Trench Isolation Patterning for Substrate Coupling Reduction and Q-Improvement”, IEEE T- vol 54, n°12, pp 4397-4411.

[94] O. Tesson, and S. Wane “Conformal Faraday Cage Micro-coaxial Shielding for Combined Optimization of Routing Distribution and EM Coupling Reduction”, European Microwave Conference, 2010, Paris.

[95] S. Wane, G. Boguszewski, “Global digital-analog co-simulation methodology for power and signal integrity aware design and analysis”. in Proceedings of the 38th European Microwave Conference, Amsterdam, Oct. 2008.

[96] S. Wane, J.C. Rautio, V. Mühlhaus, “Topological and Functional Partitioning in EM Analysis: Application to Wafer-Level Chip-Scale Harmonic Filters”, IEEE IMS 2009.

[97] F. M. Ghannouchi, and A. Mohammadi, “The Six-Port Technique with Microwave and Wireless Applications”, Artech House, 2009.

[98] S.Wane, D. Bajon, “Partition-recomposition methodology for accurate electromagnetic analysis of SiP passive circuitry”. in presented at EUROCON 2007, the International Conference on “Computer as a Tool”, 9–12 Sept. 2007, pp. 15–23.

[99] M. Ranaivoniarivo, “Towards wide-band equivalent circuit extraction methodology for passive circuits”, Research Master Internship Report, Université de Marne-la-Vallée, France, Aug. 2007.

[100] S.Wane, M. Ranaivoniarivo, B. Elkassir, C. Kelma and P. Gamand , “Towards Cognitive Built-in-Self-Test (BIST) for Reconfigurable On-Chip Applications, and Contact-less Measurement”, RFIC 2011, Jun. 2011, Baltimore, Maryland.

[101] “LoPSTer, Low-Power Single-Chip Transceiver Data Sheet”, Product Specification for V1A (rev 1.24), Apr. 2008, NXP Semiconductors.

[102] “LoPSTer, Low-Power Single-Chip Transceiver IC Design Specification”, Objective Design Specification (rev0.01), NXP Semiconductors.

[103] “Characterization Report, PQF7980 LoPSTer Version V1x”, NXP Semiconductors, May 2008.

[104] http://ics.nxp.com/packaging/hvqfn/

[105] P. Philippe, “TFF1014 Functional Requirement Specification “, Ver 2.5, NXP Semiconductors, Sept. 2009.

[106] P. Philippe, “PLL Design Specification TFF1014 “, Rev 2.1, NXP Semiconductors, June 2009.

[107] S. Wane and D. Bajon, “Electromagnetic Partitioning Methodology Towards Multi-Physics Chip-Package-Board Co-Design and Co-Simulation”, in Electromagnetics and Network Theory and their Microwave Technology Applications, Editors Stefan Lindenmeier and Robert Weigel, Springer 2011.

[108] S. Wane, A. Kuo, and P. Dos Santos, “Dynamic Power and Signal Integrity Analysis for Chip-Package-Board Co-Design and Co-Simulation”, Proceedings of the 4th European Microwave Integrated Circuits Conference 2009.

[109] Xu, X., R. G. Bosisio, and K. Wu, “Analysis and Implementation of Six-Port Software-Defined Radio Receiver Platform,” *IEEE Trans. Microwave Theory & Tech*., Vol. 54, No. 7, 2006, pp. 2937–2943.

[110] F. M. Ghannouchi, Y. Xu, and R. G. Bosisio, “A One-Step Connection Method for the Measurement of N-Port Microwave Networks Using Six Port Techniques,” *IEE Proceedings Part-H. Microwave, Antenna & Propagation,* Vol. 141, No. 4, pp. 285–289, August 1994.

[111] N. Boulejfen, F. M. Ghannouchi, and A. B. Kouki, “A Homodyne Multiport Network Analyzer for S-Parameter Measurements of Microwave N-Port Circuits/Systems,” *Microwave & Optical Technology Letters*, Vol. 24, No.1, pp. 63–67, January 2000.

[112] M. Caron, A. Akyel, and F. M. Ghannouchi, “A Versatile Easy to Do Six-Port Based High Power Reflectometer,” *Journal of Microwave Power and Electromagnetic Energy,* Vol. 30, No. 4, pp.23–239, 1995.

[113] C. Labussiere-Dorgan, S. Bendhia, E. Sicard, J. Tao, H. J.e Quaresma, C. Lochot, and B. Vrignon, “Modeling the Electromagnetic Emission of a Microcontroller Using a Single Model” IEEE Tansactions on Electromagnetic Compatibility C, Vol. 50, No. 1, pp.22–32, February 2008.

[114] Cristian A Vram, Gheorghe Ga Vrila, and Junwu Tao, “Characterization of Miniature Near Field Probes for IC's Radiation Measurements”, International Conference on Communications, pp.275–278, 2010.

[115] Zhuoxiang Ren, Hazem Hegazy, and Nur Kurt-Karsilayan, “Characterization of Dynamic Substrate Macro-Model in Mixed Signal IC Systems Using 3-D Finite Element Method”, IEEE Transactions on Magnetics, vol. n°44, pp: 1466 – 1469, 2008.

[116] R. Ghapurey and R. G. Meyer, “Analysis and simulation of substrate coupling in integrated circuits,” *Int. J. Circuit Theory Applicat.*, vol. 23, no. 4, pp. 381–394, Jul.–Aug. 1995.

[117] E. Ngoya, and R. Quéré, “Second order extension of power amplifiers behavioral models for accuracy improvements,” in *Proc. 40th EuMW*, Paris, France, Sep. 2010, pp. 1030–1033.

[118] W. S. El-Deeb, M. S. Hashmi, N. Boulejfen, and F. M. Ghannouchi, “Dynamic distortion characterization of multiport RF PAs using MTA-based multiport measurement setup,” in Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits, INMMiC 2010, Goteborg, Sweden, 2010, pp. 152-155.

CHAPTER II:
EXPERIMENTAL CHARACTERIZATION AND ANALYSIS OF FREQUENCY PULLING EFFECTS IN PLLS: APPLICATION TO TRANSCEIVER CASES

II.0. Introduction

This chapter is built around four principal sections. In the first section, detailed description of system-level carrier application including the chip, PCB and monitoring characterization protocols for pulling effects in PLLs is presented.

The second section of this chapter covers analysis, diagnosis and measurement of pulling effects taking place in PLL systems. Qualification of observed pulling with respect to application specifications is discussed. The characterization approach encompasses power spectrum measurement of TX systems, VNA measurement of on-chip inductors, transmission line interconnects, and on board SAW filters. Furthermore phase noise measurement is combined to power spectrum analysis for qualifying transmit-path noise performances including PA module.

The third section of this chapter elaborates on directions of investigation for clarifying the root causes of observed pulling effects both at system-level (where complete PLL, PA and SAW filter on PCB are combined as one single entity) and at function block level (e.g., with the PLL, and inside the VCO). At system-level, coupling mechanisms that originate from the interaction of the PLL with the PA through power/ground distribution network are considered as potential source for pulling effects- together with effects resulting from incorporation of SAW filter on PCB. Within the PLL system, the contribution of each elementary constitutive entity of the PLL loop (e.g., PFD-Charge-Pump, VCO, Divider, Loop-Filter, etc…) is evaluated, from experimental perspective, in order to understand their potential impact on frequency pulling. At VCO function block level influences of varicap devices, tuning voltage variations, and power/ground fluctuations on frequency pulling and pushing are investigated.

At last in the fourth section of this chapter, a link between frequency pulling and electromagnetic couplings is discussed

II.1. Description of Chip-Package-PCB Carrier Application

The basis of the characterized carrier application is the LoPSTer transceiver in transmit mode. Indeed in emission mode, the amplitudes of the signals involved are more important than in reception thus increase the coupling issues. Besides, the realization of the chip was already done so the analysis of the PLL pulling effects could be characterized immediately for this application.

II.1.1.The Chip-Package Application: the LoPSTer in TX Mode

In TX mode, the transmit path includes the PLL-including the crystal reference at 16MHz and the VCO working around 1.7GHz, a reshape buffer, one frequency divider if working around 868MHz, a class-E power amplifier in single ended mode.

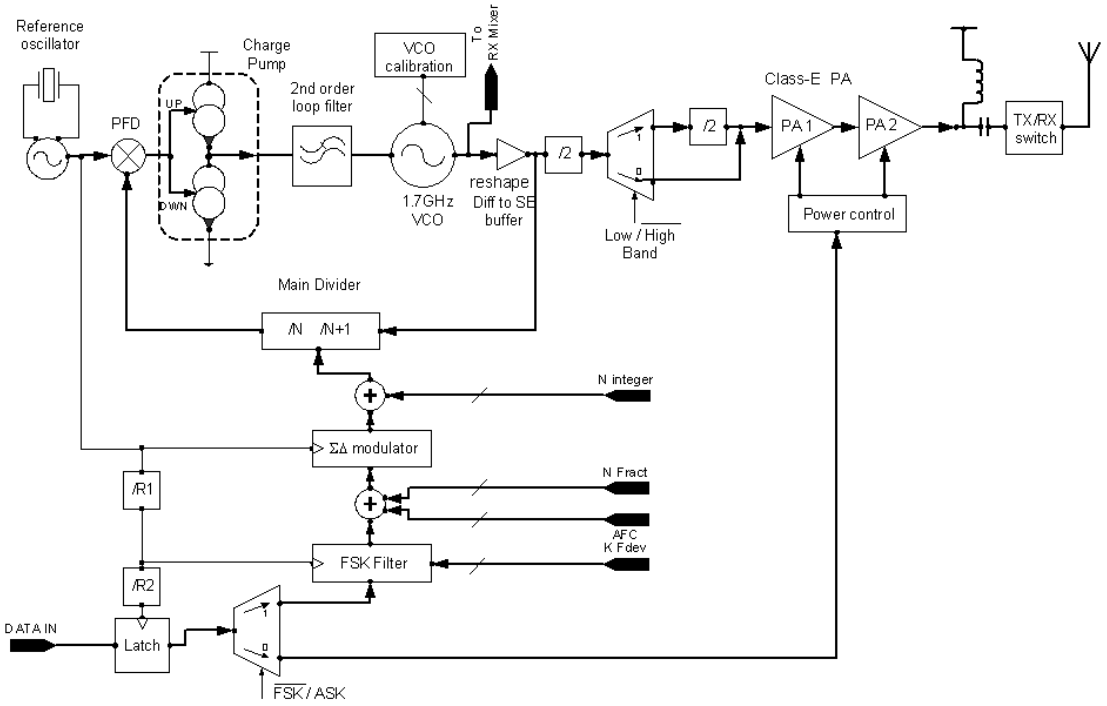


Figure II.1-1: TX block diagram

LoPSTer's specifications are detailed in [119] and [120] but here are some characteristics needed for the experimental characterisations of the PLL pulling in the LoPSTer case:

- DC Characteristics:

The supply voltage of the LoPSTer should be typically 2.8V and the operating temperature 25°, ambient temperature. The transmitter supply current is 16mA for an output power of 10dBm.

- AC Characteristics:

The operating frequency is typically 868MHz with a minimum and maximum value respectively of 865MHz and 870MHz. No modulation around the carrier frequency will be added for the characterization analysis.

The crystal reference input frequency should be 16MHz and the PLL loop bandwidth for a -3dB in closed loop 170kHz. The lock time of the PLL for a frequency step of 1MHz should be 25µs. The phase Noise at 868MHz TX output is -86dBc/Hz at an offset of 50kHz from the carrier frequency, -86dBc/Hz at 100kHz offset, -107dBc/Hz at 1MHz offset, -115dBc/Hz at 2MHz offset, -125dBc/Hz at 5 MHz offset and -130dBc/Hz at 10 MHz offset for a PLL charge pump current of 30µA.

II.1.2.The Package Level Carrier Application

The LoPSTer application board uses HVQFN32 package (Heatsink Very-thin Quad Flat-pack No-leads) [121][122][123]. The HVQFN is a near Chips Scale Package (CSP) Land Grid Array (LGA) type plastic encapsulated package with a copper lead frame base. The package has no leads or bumps, but an exposed pad in the centre and peripheral land terminals at the bottom of the package as seen in Figure II.1-2.

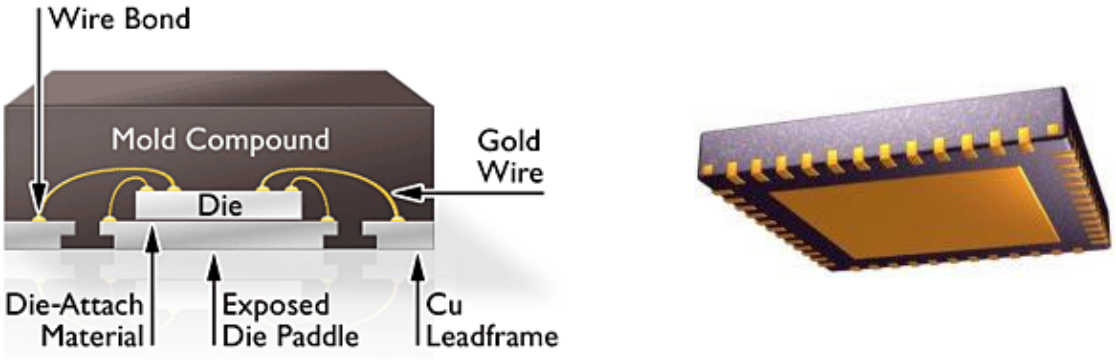


Figure II.1-2: Example of HVQFN cutaway view (a) and bottom view (b)

The HVQFN package die supply ground is connected to both the GND pin of the LoPSTer and the exposed centre pad. For proper heat conduction through the board, thermal vias are incorporated in the PCB in the thermal pad region to improve heat transfer away from the package.

The dimensions of the package are:

- Pitch : 0.5 mm, body: 5×5×0.85 mm.
- die pad dimensions:3.8 mm× 3.8 mm.
- Downbond (bondwires to the die paddle):~600µm
- Wire bond to the lead frame: ~1.4 to 1.8mm

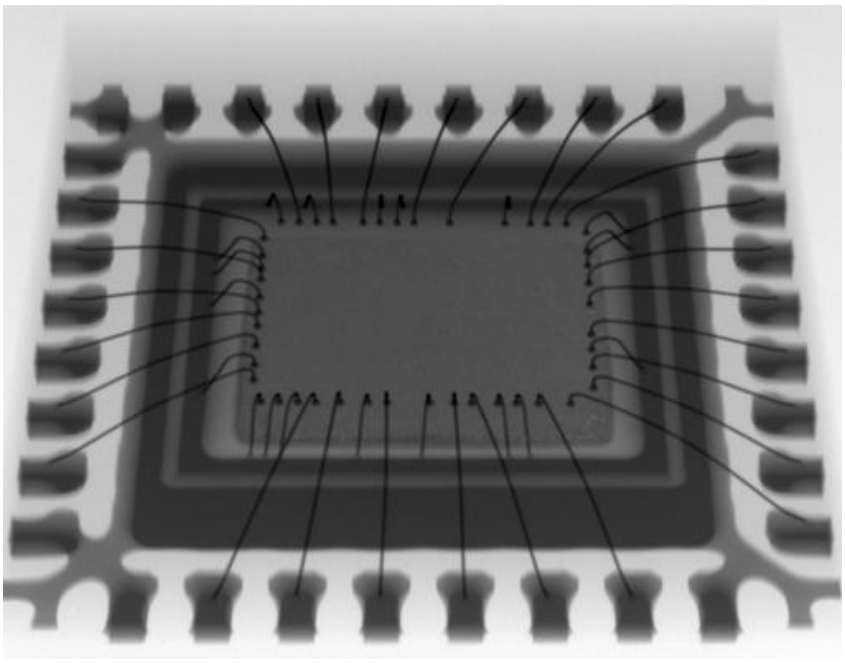


Figure II.1-3: Xray photography of LoPSTer's packaging

II.1.3.The PCB Level Carrier Application

a. The LoPSTer Test Board Used for Characterization

For the LoPSTer's characterization, the output signal of the adapted power amplifier is specified to deliver sinus signal of 10dBm maximum power +/-1dBm at 868MHz for a load charge of 50Ω.

To complete the test measurement characterizations, the IC is reported on its associated PCB test board that contains discrete components of decoupling and matching network, for example for the PA in TX mode. Indeed, as the LoPSTer can operate at 4 different frequency bands (315MHz, 434MHz, 868MHz and 915MHz), the matching circuit or load network of the class-E power amplifier will be reported on the PCB and according to the frequency band used, the appropriated SMDs components value will be changed [124].

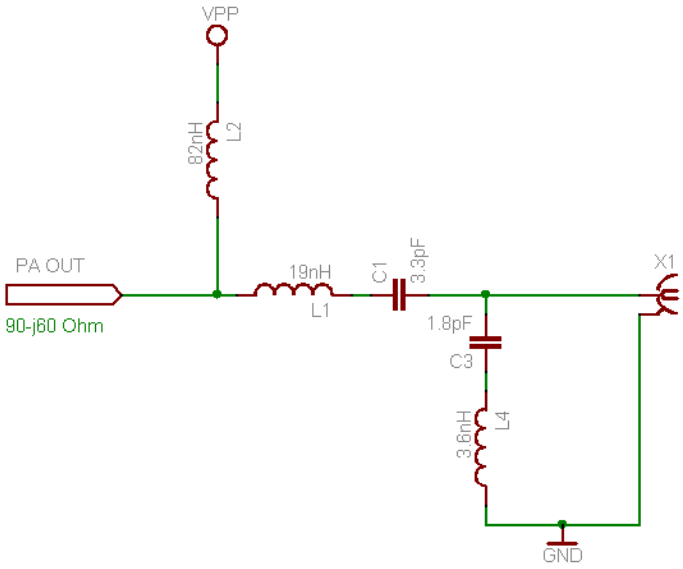


Figure II.1-4: The TX matching network reported on PCB for f_{RF}=868MHz

For the LoPSTer, with a Class E power amplifier, the purpose of the TX matching network is to transform the 50 Ω of the load into an impedance which maximizes the output power at the desired operating frequency for a given current consumption. It also filters the harmonic frequency components in the output signal [134]-[135] in order to meet regulatory requirements.

The test application implemented on the PCB is presented in Figure II.1-5.

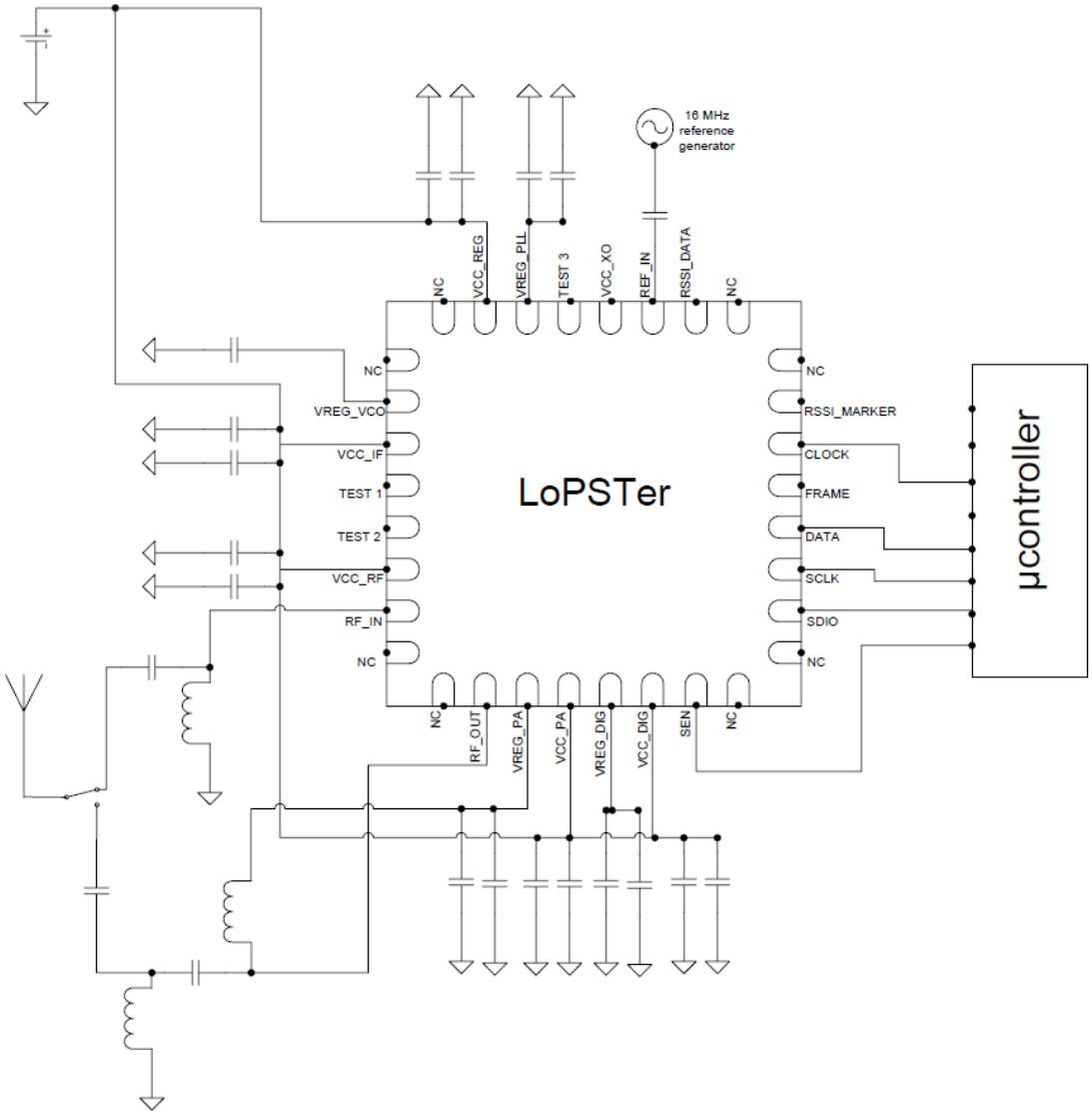


Figure II.1-5: The test circuit including the chip, package and PCB

b. An External SAW filter Reported on PCB

The LoPSTer application system uses a single filtering for TX and RX ways between the chip and the antenna load. Because of reception constraints, the filter used should be very narrow band around the working frequencies in order to reject the interfering signals in automotive application, for example TV frequency band at 862MHz can reach 10dBm of amplitude. The SAW (Surface Acoustic Wave) EPCOS filter B3762 reported on PCB with a matching network to 50Ω was selected by the customer to be inserted between the PA and the antenna. The filter is centred at 868.3MHz with a pass bandwidth of 1.35MHz, then a Q-factor of 643.18 [125].

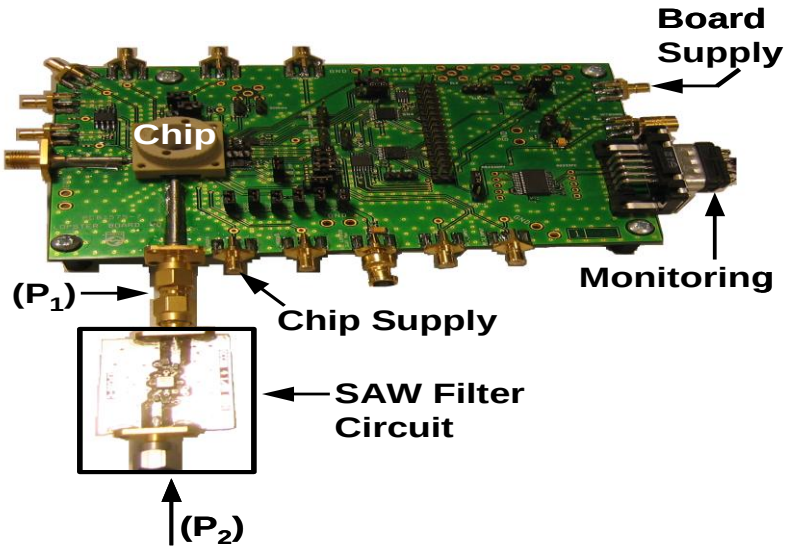


Figure II.1-6: LoPSTer's associated PCB test board with SAW filter reported on separate PCB

The S-parameters of the on-board SAW filter obtained through a 2-port measurement with the Rohde & Schwarz ZVCE 20kHz-8GHz vector network analyzer (VNA) are compared to the S-parameters of the SAW alone provided by EPCOS in Figure II.1-7.

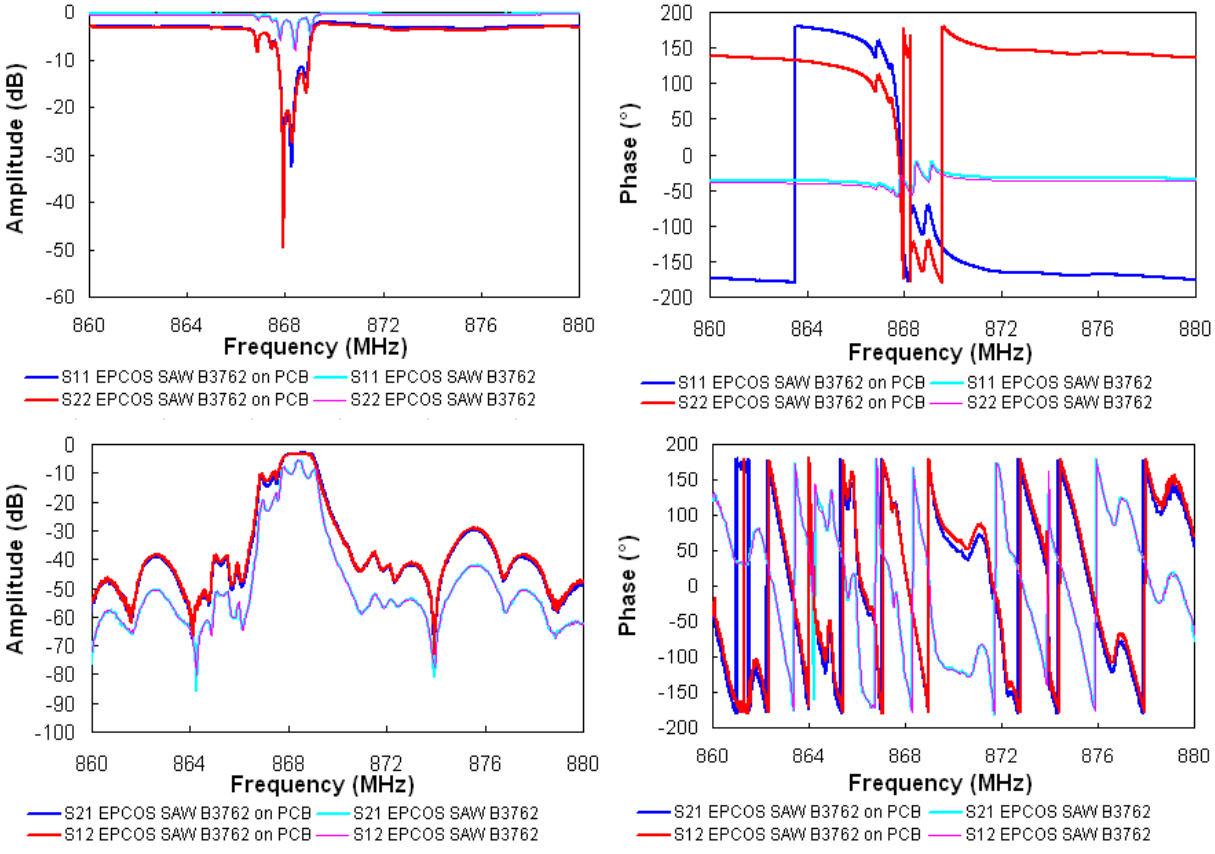


Figure II.1-7: S-parameters of the SAW EPCOS B3762 alone or reported on an adapted board

A large difference can be observed between the constructor's data (of the SAW alone) and the measured adapted PCB on which the SAW filter is reported. A better return loss, less ripple, and a better insertion loss are obtained inside the filter bandwidth when the device is matched to 50Ω. Changing the input and output impedances of the SAW PCB can deteriorate the filter performance.

II.1.4.The Monitoring Characterization Protocol and the Conceivable Measurements

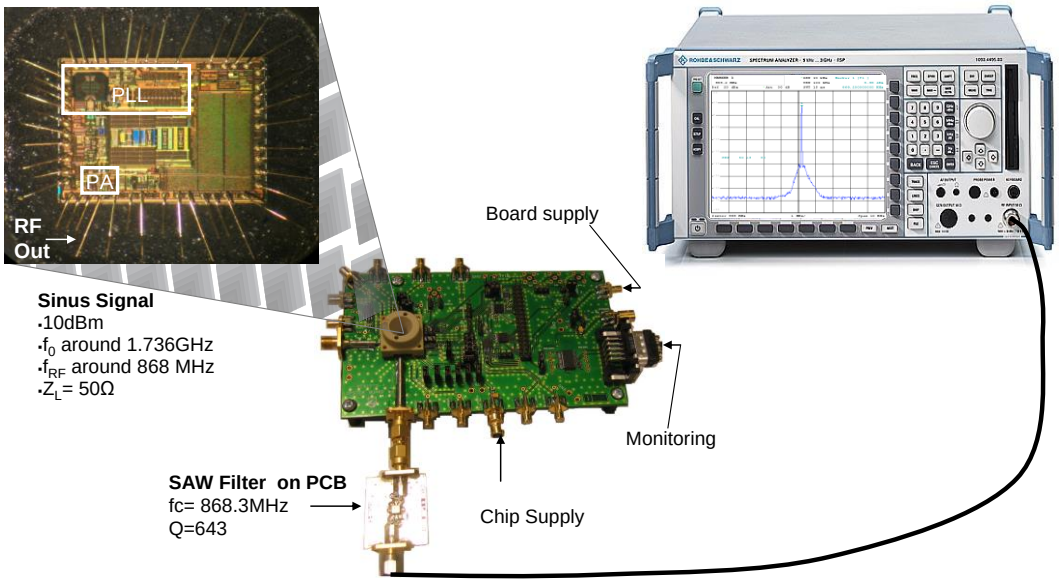
a. The Monitoring Characterization Protocol

The monitoring of the transmit system is achieved with an I^2C bus [126] for real time measurement. The communication is bidirectional, writing, reading and status configuration are allowed. Once the LoPSTer is connected via 3 wires to the monitoring, and when the transmit mode is entered, parameters that can be changed by programming are among others:

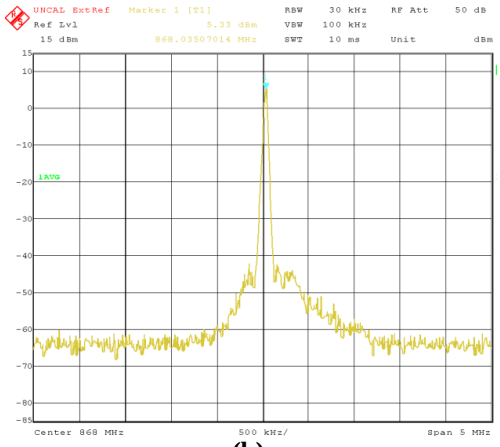
- the working frequency of the IC
- the charge pump current value
- the output power amplitude

b. The Conceivable Measurements

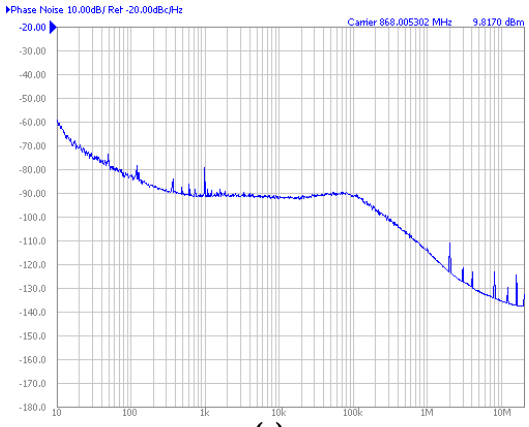
Concerning the signals that can be measured, the output signal transmitted to the antenna can be characterized in terms of spectrum using a spectrum analyzer (reference Rohde & Schwartz FSP7) or phase noise using a signal source analyzer (Agilent E5052A for phase noise measurement) by replacing the antenna load by the analyzer with or without the external SAW filter (respectively at (P_2) or (P_1) locations in Figure II.1-6).



(a)



(b)



(c)

Figure II.1-8: Characterization with a spectrum analyzer (a) output spectrum (b) and phase noise (c) of the LoPSTer's board output signal at 868MHz without the SAW filter

We can see with Figure II.1-8 that the output signal of the chip-package-PCB first carrier application analyzed, the LoPSTer, fulfils the product specification in terms of spectrum purity and phase noise regarding the carrier signal.

Direct access to the LoPSTer's supplies and internal regulators have been implemented on the test PCB so these signals can be measured in DC (current consumption or voltage DC level) or AC (noise aspect around the DC level in time domain) using multimeter or oscilloscope with high input impedance.

These accesses can also be used for driving directly the studied function block instead of the regulators output driving the V_{DC} of the power amplifier, the V_{CC} of the VCO etc.

In addition, an external access to the tuning voltage of the VCO can be used to change manually the working frequency of the application and to get the oscillator characteristics.

The chip-package-PCB carrier system was described in this section, as well as the possible measurements that can be done to characterize the frequency pulling that can encounter the application. In the following section, an analysis and a diagnosis of the PLL pulling is detailed.

II.2. Characterization of PLL Pulling

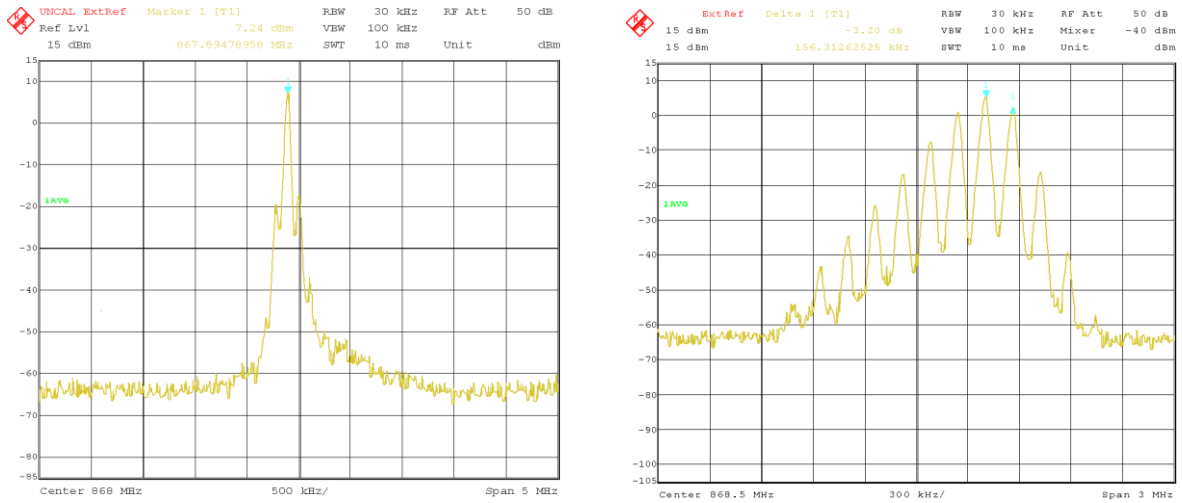
II.2.1.Characterization of PLL Pulling in Frequency Domain

a. Spectral Purity of the signal transmitted

During the experimental characterization of the IC in transmit mode, considerable pulling was reported in a particular way of communication between the IC and its load. Indeed when the LoPSTer, in the presence of the SAW EPCOS filter B3762 reported on PCB, emits a single sinusoidal tone around the cut-off frequencies of the filter, frequency pulling issues are reported at the output of the chip-package-PCB solution as showed in Figure II.2-1. We can observe that this pulling effect is particularly important for a single tone around the high cut-off frequency of the SAW filter.

Several spurs with non negligible amplitude are perceived around the wanted working frequency. In addition, the amplitude level of the carrier tone is less important than the amplitude of the signal transmitted crossing the SAW filter. The number and amplitude of the spurs around f_{RF} increase with:

- the power amplitude of the signal transmitted to the antenna load
- and the charge pump current amplitude.



(a) **(b)**

Figure II.2-1: Output spectrums of the LoPSTer's board followed by the EPCOS SAW B3762 operating at frequencies around the low (a) and high(b) cut-off frequencies of the filter

As the spectral specifications of the SAW filter implies a strong rejection outside its bandwidth (see S21 of the SAW filter in Figure II.1-7), the wide band spectrum of the signal transmitted to the load is rejected to the noise floor of the spectrum analyzer.

For analyzing the wide band spectrum of the IC direct output as no measurement connexion was dedicated, we will use a high-frequency probe HP 85024A with high input impedance at the choke inductance path of the PA matching circuit. The technique being not strictly rigorous, the obtained signal amplitude could be not correct but only the harmonic distribution and relative level of the spurs will be taken into account. The comparison of a transmitted signal with no pulling at 868MHz is compared to a frequency pulling issue reported when f_{RF}=868.88MHz.The LoPSTer's default functioning characteristics are taken: the VCC of the PA is 1.5V and the charge pump current of the PLL is 60µA.

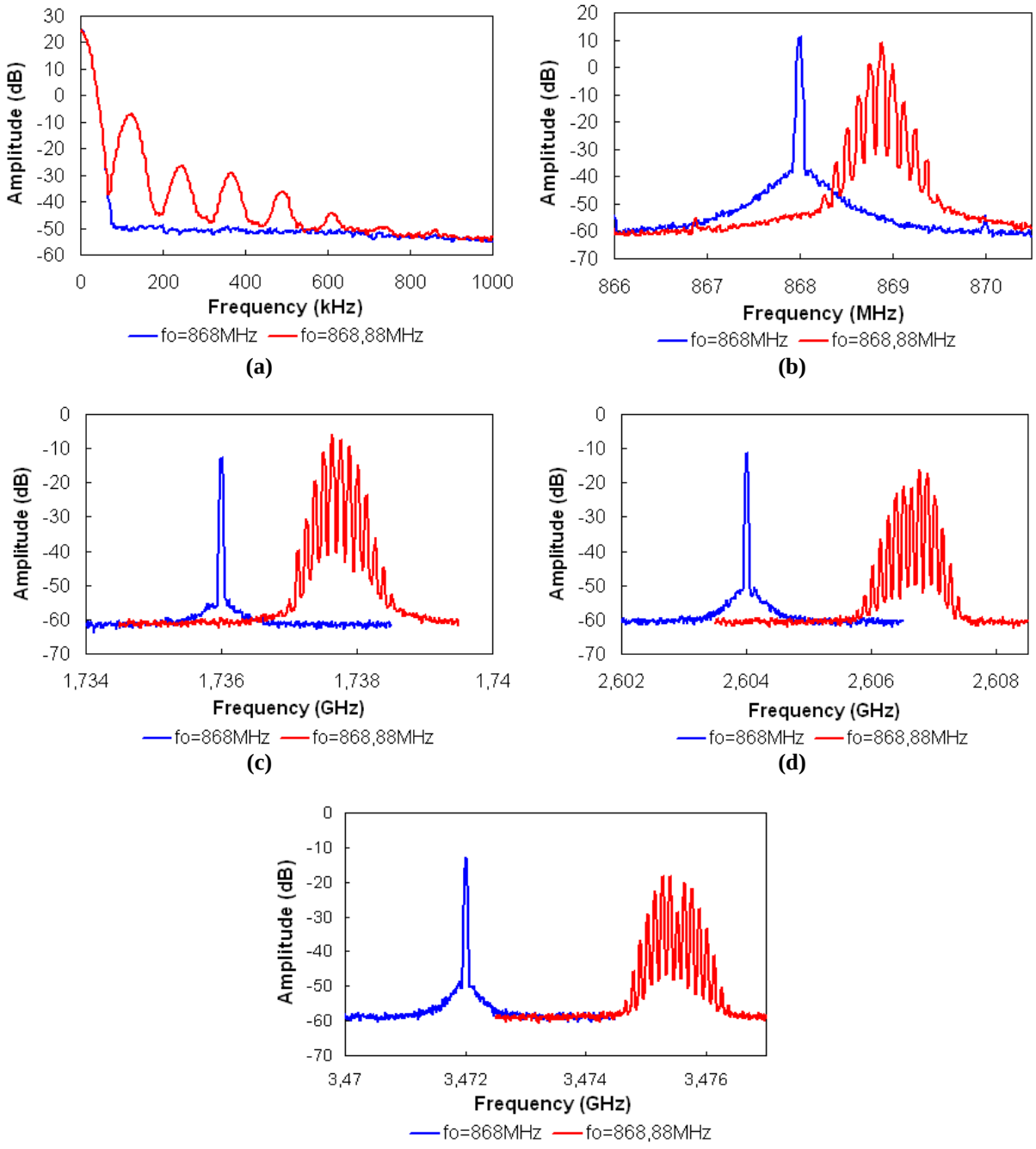


Figure II.2-2 : Direct output spectrum at low frequencies(a), around f_{RF} (b), around $2\times f_{RF}$ (c), around $3\times f_{RF}$ (d) and around $4\times f_{RF}$ (e)

At f_{RF}=868MHz, inside the SAW filter bandwidth, when there is no instability transmitted to the antenna around the fundamental frequency, the frequency spectrum of the signal directly measured at the LoPSTer's output, the drain voltage of the class-E power amplifier , is made up of a DC tone and spectral lines at $N\times f_{RF}$ frequencies (N integer).

When f_{RF} is around the high cut-off frequency of the filter, here f_{RF}=868.88MHz, we can notice that the tones at DC and $N\times f_{RF}$ frequencies are recovered but spurious tone are added to the spectrum around those frequencies at DC, fundamental and harmonics frequency tones at a same $\Delta f^{Pulling}$ frequency from f_{RF} than the DC tones. The pulling effect takes place at the fundamental frequency but also at the harmonics frequency of the PA output of the IC.

The output signal of the VCO PLL is sinusoidal. The pulling effect observed through measurement at the direct output of the IC supposes that the output instabilities of the VCO/PLL will be replicated around every harmonic during the reshape of the sinus signal to square signal and will spread over the frequency divider, the buffer and the PA.

b. Phase noise induced by pulling effects

The phase noise specifications of the LoPSTer were given in II.1.1. The measured phase noise of the LoPSTer's output signal respects the specifications inside the bandwidth of the SAW filter (see Figure II.1-8 (c)) but while the working frequency reaches the edge of the filter bandwidth, chirps at regular frequency offsets from f_{RF} are obtained for the phase noise, the specification of the product is no longer respected.

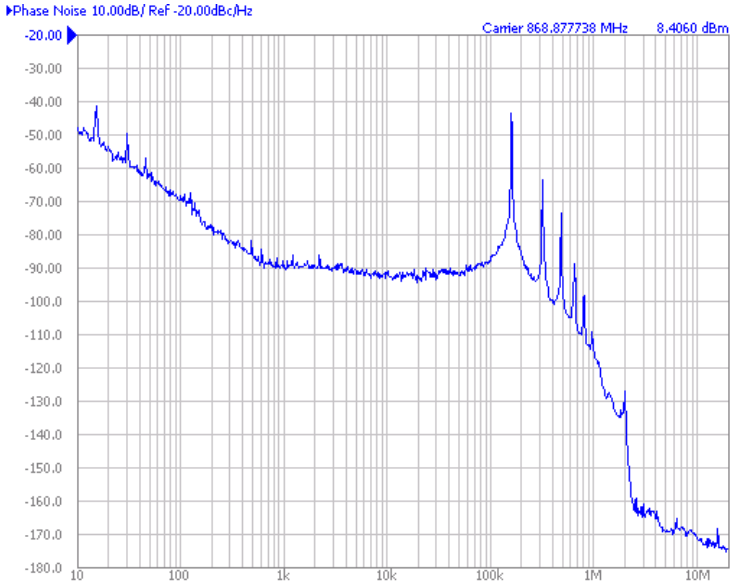


Figure II.2-3: Phase noise induced of the LoPSTer's board followed by the EPCOS SAW B3762 operating at high cut-off frequency of the filter

c. Qualification of the transmit-path noise performances in Frequency Domain

Figure II.2-1 and Figure II.2-3 illustrate the output signal of the LoPSTer's application, including its test board and the SAW filter: we can see that the pulling effect sustained by the LoPSTer yields its spectrum non compliant to the product specification and the numerous spurs are too close to the carrier frequency. The pulling issue also yields the LoPSTer non conformal to its phase noise specifications because of the climb up of the phase noise induced under 5MHz.

Frequency pulling effects causes instabilities on the TX performances of the IC while the customer wants to use narrow band filtering solution, and a functioning frequency near its cut-off frequencies. Qualification of the product could not be achieved for this particular way of transmission.

The origins of the pulling should be investigated.

II.2.2.Characterization of PLL Pulling in Time Domain

a. Combination of AM and FM modulation

A characterization of the pulling effects reported in the LoPSTer case permitted to underline that the pulling issue was a combination of amplitude and frequency modulation. Two kinds of measurements permitted to enunciate that assumption:

In Figure II.2-4, we observe the output signal of the LoPSTer reported on its test PCB followed by the SAW filter issued from measurements using the spectrum analyzer Rohde & Schwarz FSP7, when the pulling effect is observed. In the presented case, the centre frequency is set exactly at the fundamental frequency equal to f_{RF} and by taking a span resolution of 0Hz (time domain), we can observe the aspect of the interfering signal around f_{RF} in time domain. As phase or frequency modulations won't be visible through this kind of measurement, the observed phenomenon is due to an amplitude modulation.

Once the resolution bandwidth of the filter and the sweep time of the analyzer are well adjusted, the time domain aspect of the modulating interfering signal can be obtained but by forcing the spectrum analyzer to work in a special resolution configuration, and the amplitude of the measured signal does not necessarily correspond to the real amplitude of the modulating signal.

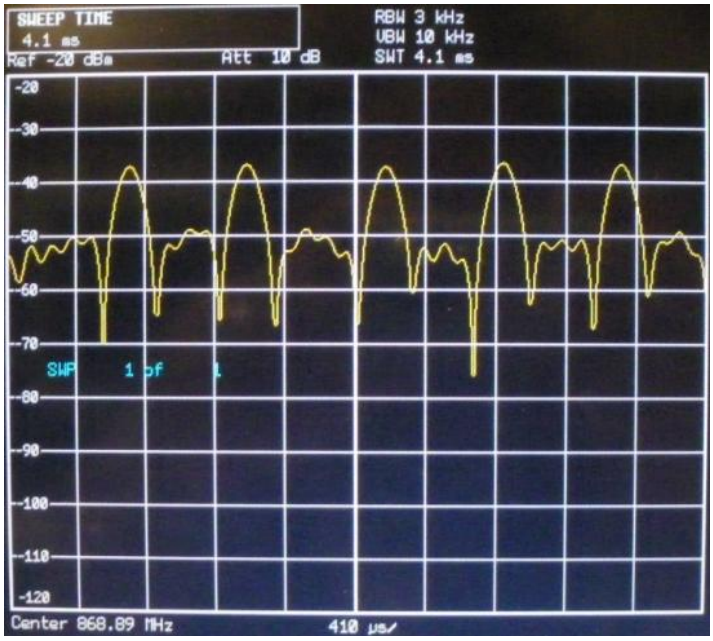


Figure II.2-4: The AM part of the pulling at the filter output, f_{RF}=868.89MHz

We also did an analysis of the pulling with a modulation domain analyzer HP53310A. This type of measurement allowed us to have the centre frequency and the peak deviation of the angular modulating signal of the system pulling response. The waveform of the signal frequency is obtained versus time, see Figure II.2-5, but if any signal modulates by amplitude the wanted signal, it won't be detected by this kind of measurement.

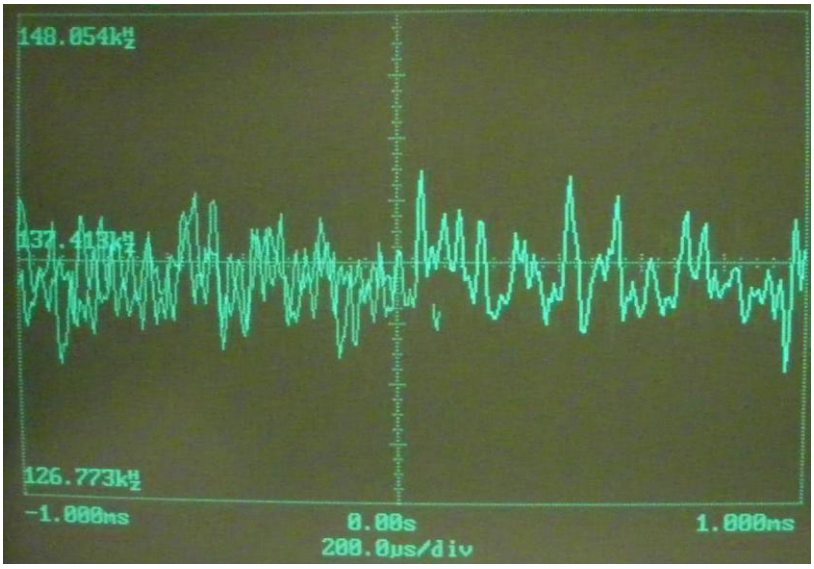


Figure II.2-5: The FM part of the pulling at the filter output, f_0=868.89MHz

The time-base of the equipment is very difficult to settle, but the principal information of the results is that the frequency of the FM modulating signal is around 137 kHz, as measured in the pulling spectrum of the LoPSTer in transmit mode.

The two kinds of measurement described in this section permitted to assert that the pulling effect around f_0 results from a combination of an amplitude and angle (frequency or phase) modulation of the wanted signal with a baseband signal. However the modulation index of the modulating signals can't be determined. The measurement results of the determination of the modulations at the output of the on-board LoPSTer followed by the SAW filter could not then be used in the feedback approach to describe the filter input source with the pulling data.

II.3. The Main Directions in the Analysis of Pulling Origins

II.3.1.Main Observations at Function Block Level

a. Influence of the PLL function block on the Pulling

The first thing that we have noticed with the characterization of the frequency pulling issue on the LoPSTer case is that, with or without the EPCOS B3762 SAW filter, the PLL loop has to be closed to obtain pulling issue, spurs with non negligible amplitude around f_{RF}. Let's now distinguish the different effects of the PLL function blocks. Analysis of the PLL loop shows two predominant effects on the pulling: the first effect is in link with the charge-pump current level while the second effect concerns the nonlinear local oscillator transfer function relating the oscillation frequency to the tuning voltage.

In LC-VCOs, the control of the oscillation frequency is usually done through L and/or C tuning. Through the capacitance point of view, the method mostly used to fix the oscillation frequency is the tuning of the tank capacitances of LC-VCOs. However, other techniques can also be used such as the commutation of one or more active part of the VCO [127] or also the change of the polarization of the active part [128]. Those techniques lead to variations of the parasite capacitances of the transistors, and when controlling them, the parasite capacitances obtained act indirectly on the global value of the VCO total capacitance, which leads to oscillation frequency variations.

Influence of the Charge Pump on the pulling

It is well known from the published literature that leakage/mismatch of the phase detector or charge pump could cause sideband reference spurs [138] at the reference frequency (here 16MHz) from f_{RF}. In Figure II.3-1 we can see that a charge pump current variation strongly impacts the pulling behavior at the output of the SAW filter in terms of spurs amplitude and frequency, on a frequency band of about 100kHz around f_{RF}.

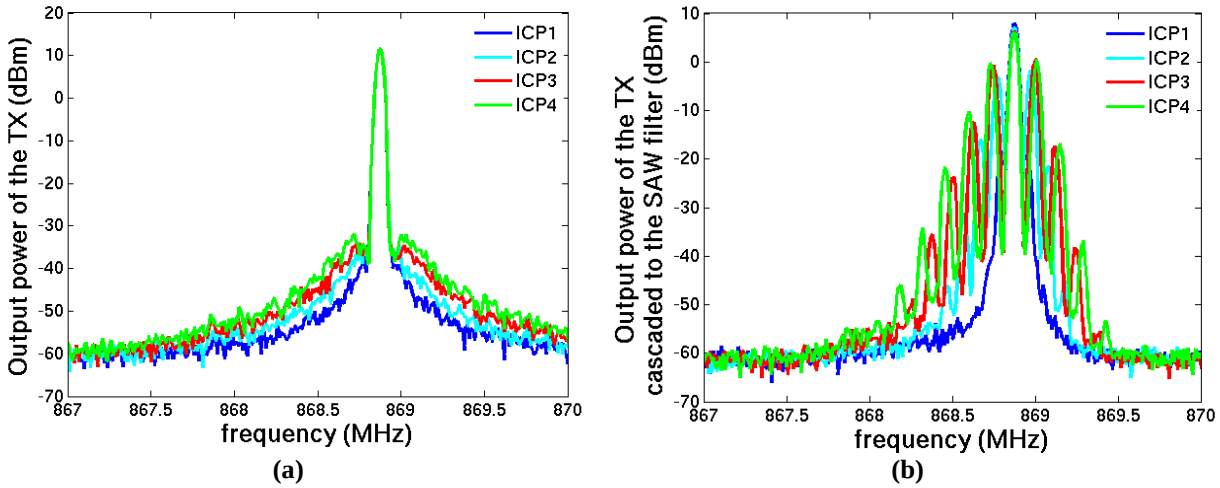


Figure II.3-1: Measured output power spectrum of the IC reported on its PCB (a), cascaded to the SAW filter PCB(b) at f_{RF}=868.85MHz, functions of the PLL charge pump current

For ICP1, ICP2, ICP3 and ICP4, the charge pump current is respectively at 15µA, 30µA, 45µA and 60µA.

It should be noted that the PLL gain depends on the charge pump current, so a large variation of the other PLL parameters as the VCO gain, if not compensated by the ICP, may cause a too high loop gain leading to PLL instability.

Influence of the VCO on the pulling

The VCO should be connected to the PLL loop to obtain pulling issue. The state of the art of the frequency pulling has often highlighted the VCO part even without PLL in pulling. When disconnecting the VCO in the the PLL and when tuning it externally we've noticed an amplitude leap of the output signal of the solution [LoPSTer + SAW filter] even if the frequency of the single tone emitted stays the same. The VCO has therefore a role to play in the pulling issue reported.

► Influence of varactors

Frequency tuning of VCO systems is classically achieved by adjusting DC voltage to control capacitance of a varactors/varicaps in a tank circuit. Nevertheless, the quality factor of the varactor decreases as the capacitance ratio Cmax/Cmin grows. To enhance the tuning range at moderate frequencies, varactor tuning is used in conjunction with a binary switched capacitor array. The resulting parasitic capacitances can lead to low oscillation frequency which is a severe limitation for high frequency applications [129]. Attempts for getting rid of varactors in LC VCO systems have been conducted towards varactorless architecture based solutions. Alternatives solutions circumventing limitations of varactors include wide tuning range. Techniques based on a transconductance tuned resonant tank [130], voltage controlled inductors [131] with the principle of transformer implementation [132]. An LC VCO varactorless tuning technique using NXP-Semiconductors SiGe technology is proposed in [133].

In conventional implementation of VCO systems with varactors, for more flexibility most often several sets of varactors are used to fix the total tank capacitance value: for example one or two sets choose more or less roughly the band or the appropriated sub-band inside every band (example for the LoPSTer: 433MHz or 868MHz for European band), these sets of varactors are often commanded by on-off switch. In addition, some varactors can be added to provide the final fine frequency tuning. These last are designed to meet the requirements in VCO gain (Kvco) and the tuning voltage is coming from the loop filter of the PLL.

As we can see in the figure below, the varicaps behavior is strongly non-linear: a little voltage variation at the anode/kathode terminals and the capacitance value can enough vary to change the oscillation frequency of the VCO.

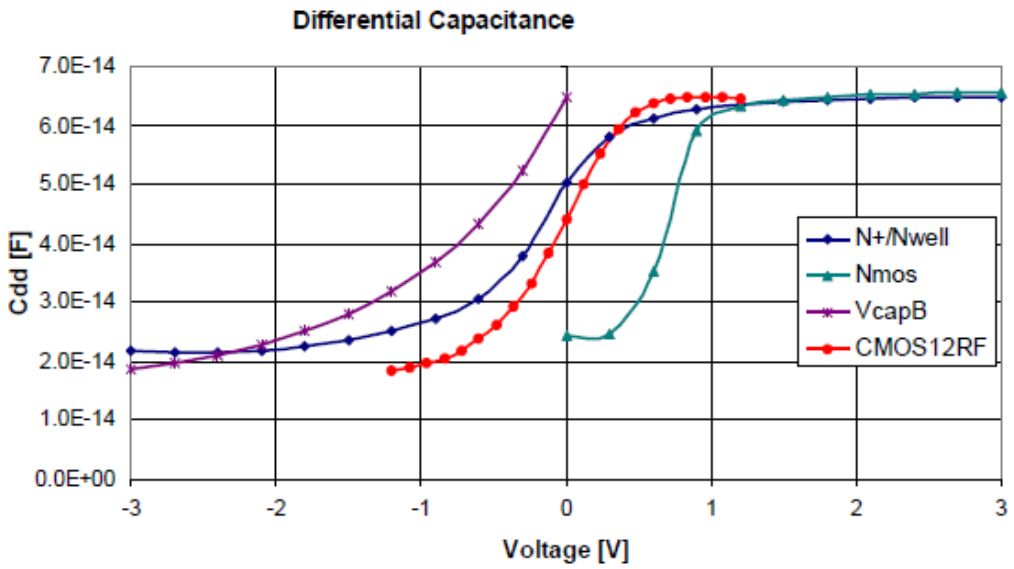


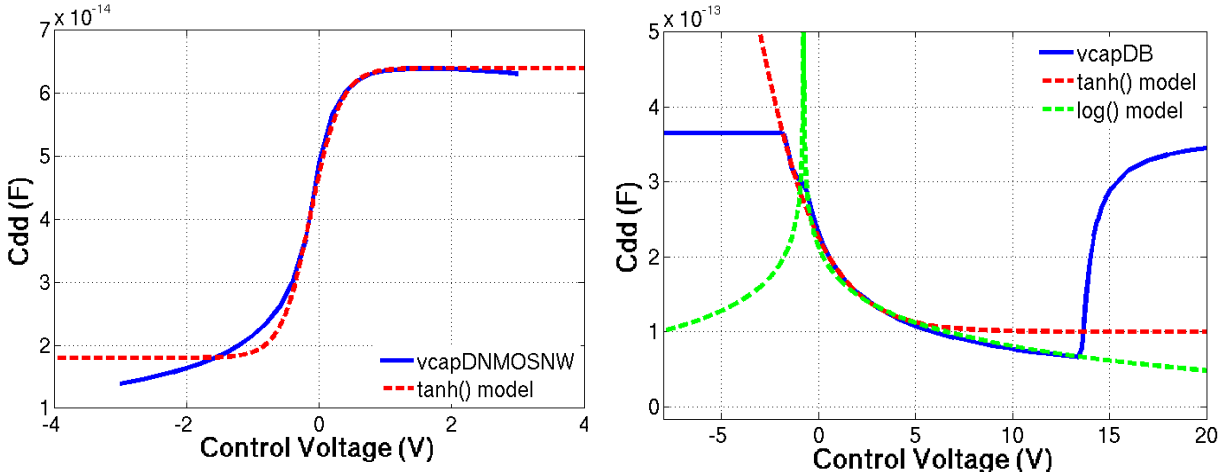
Figure II.3-2: Differential capacitance value when changing the DC potential of the anode with respect to the ground. Cdd is extracted at 5.5GHz, for various differential varicaps.

In the depletion and the accumulation region of the varactors, the variation of the differential capacitance value functions of the control voltage can be described using a simple analytical model such as:

$$\mathrm{Cdd} = \mathrm{C_{min\_max}} \times \tanh\left(\mathrm{a} \cdot \frac{(\mathrm{Voltage} - \mathrm{V_0})}{\mathrm{NL}}\right) + \mathrm{C_0} \qquad \text{[II.3-1]}$$

With a=1 when the tuning voltage is applied on the anode of the varicaps; a=-1 if the voltage is applied on the cathode, V_0 the voltage for nominal capacitance C_0, Cmin_max the maximum capacitance change from nominal, and Cmin_max/NL the maximum slope at V_0. The constant part of Cdd can be associated to the fringe capacitors between the metal and polysilicon gates and the variating part to the variable junction capacitance of the diode from the p/n junction.

In the following figures, the analytical model is applied to NXP vcapDNMOSNW and vcapDB (in LoPSTer VCO-varicaps configuration) and compared to Spectre simulation results at 1.736GHz.



(a) *(b)*

Figure II.3-3: Simulated differential capacitance value of NXP vcapDNMOS (a) and vcapDB (b) versus analytical model

The steep tuning curve of vcapDNMOSNW that can be described through a tanh() [II.3-2] function, shows that for analog tuning, noise in supply voltage can easily be converted to noise in output and then cause VCO pushing/pulling.
For the vcapDB, only the depletion regime can be analytically modeled, log()[II.3-3] and tanh()[II.3-4] functions can describe the tuning.

$$\mathrm{Cdd_{vcapDNMOSNW}} = 23\mathrm{E}-15 \times \tanh\left(1 \cdot \frac{(\mathrm{Voltage} - (-0.12))}{0.45}\right) + 41\mathrm{E}-15 \qquad \text{[II.3-2]}$$

$$\mathrm{Cdd_{vcapDB}} = 250\mathrm{E}-15 \times \tanh\left(-1 \cdot \frac{(\mathrm{Voltage} — 1.5)}{3}\right) + 350\mathrm{E}-15 \qquad \text{[II.3-3]}$$

$$\mathrm{Cdd_{vcapDB}} = -1 \times 50\mathrm{E}-15 \times \log(\mathrm{Voltage} - (-0.77)) + 200\mathrm{E}-15 \qquad \text{[II.3-4]}$$

► **Frequency pulling due to noises on the VCO control voltage**

Let's resume the equation that governs the VCO:

$$y(t) = A \cdot \cos\left(\omega_{FR} t + 2\pi \cdot K_{VCO} \int_{-\infty}^{t} Vcont(t)dt\right) \qquad \text{[II.3-5]}$$

ω_{FR} being the free running frequency of the VCO, K_{VCO} the gain in Hz/V and Vcont the control voltage of the VCO.

If the control voltage is contaminated by a periodic signal of frequency ω_Δ, by developing the equation [II.3-5], the output signal of the VCO is frequency modulated, spurs around f_{RF} at $f_{RF}\pm f_\Delta$ will be found.

For illustrating that, by taking Vcont as a DC level on which a spurious sinusoid signal is added, the VCO equation becomes:

$$y(t) = A \cdot \cos\left(\omega_{FR} t + 2\pi \cdot K_{VCO} \left(V_{DC} \times t + \frac{A_\Delta}{\omega_\Delta} \cdot \cos(\omega_\Delta t) \right) \right) \quad \text{[II.3-6]}$$

The DC part of Vcont shifts the carrier working frequency to (f_{RF} +K_{VCO}.V_{DC}), and the term cos(ω_Δt) leads to a pulling spectrum with symmetrical spurs around f_{RF}.

In the following figure, comparisons of different cases are given:

- The measurement results, where the amplitude of the added sinus signal around the DC tuning voltage measured at the evaluation board access with an high input impedance oscilloscope is A_Δ=45mVpp.
- Transient simulation of the LC-VCO with Spectre-Virtuoso, to have -1.5dB between the amplitude of the carrier tone and the first couple of spurs, A_Δ=80mVpp.
- And numerical results of y(t) with $\frac{2\pi \cdot K_{VCO} \cdot A_\Delta}{\omega_\Delta} = 1.2$ and ω_Δ=180kHz. If K_{VCO}=30MHz/V, A_Δ should be 1.15mVpp, and for K_{VCO}=15MHz/V, A_Δ should be 2.3mVpp.

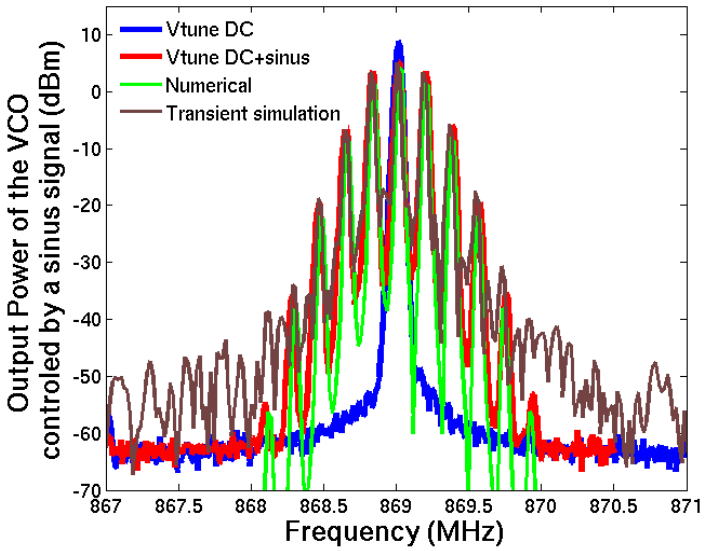


Figure II.3-4: Comparison of measured output power spectrum of the ICs on PCB (red curve), numerical (green curve) and transient simulation (brown curve) of a VCO when a sinusoidal noise is applied around the DC control voltage. The blue curve stands for the measured signal when applying only a DC control voltage on the VCO.

The amplitude of the FFT results of the numerical and transient simulations is adjusted to the measurements. It should be noticed that the global amplitude level of the frequency signals depends on the amplitude of the carrier signal A (if we compare the pulling to a FM modulation) and on the window used for the FFT (here Hanning window), but does not

interfere on the spurs and carrier difference of amplitude. The maximum amplitude of transient (numerical and Spectre simulation) results are then set to the measurement one.

The differences of A_Δ values are due to the measurement uncertainties while extracting the real voltage that comes to the VCO, the non linearities of K_{VCO} and its link to the non linear response of the VCO varicaps to the control voltage variation.

► **The VCO gain non linearity**

The VCO gain is defined as the ratio of the working frequency variation and the control voltage of the VCO. In a LC VCO as for the LoPSTer, if we suppose that the tank inductance value is fixed, K_{VCO} directly depends on the capacitors, precisely the varicaps variation in function of the control voltage.

In order to have a linear variation of K_{VCO}, the varicaps of the tank will be used in a voltage range where they operate linearly.

However as we will see in the next paragraph in particular in Figure II.3-6, the VCO gain linearity will be strongly damaged while inserting a SAW filter with a strong frequency variation at its cut-off frequencies and when transmitting a signal at those frequencies.

II.3.2.Main Observations at System Level

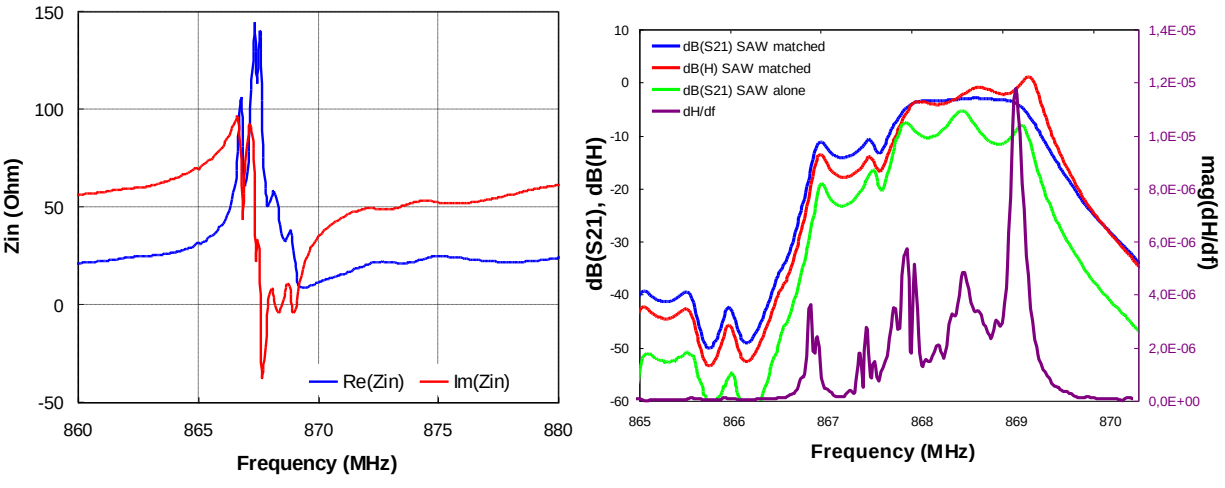
a. Effects of the SAW Filter on the Pulling

The load to present to the LoPSTer should be 50Ω, however the SAW filter board loaded by Z_L=50Ω is at that value only in the middle of the bandwidth of the filter. The input impedance of the on-board SAW filter Z_{in} is given in Figure II.3-5 (a).

$$Z_{in} = Z_{11} - \frac{Z_{12} \cdot Z_{21}}{Z_L + Z_{22}} \qquad \text{[II.3-7]}$$

Moreover, at its cut-off frequencies the slope of the SAW filter transfer function H is very important, the SAW filter frequency response varies very rapidly at the corners of its bandwidth, around 869MHz for high cut-off frequency, 867.9MHZ for low cut-off frequency.

$$H(j\omega) = \frac{2 \cdot Z_L \cdot S_{21}}{(Z_0 - Z_L)(S_{11} \cdot S_{22} + S_{22} - S_{12} \cdot S_{21}) + (Z_0 + Z_L)(S_{11} + 1)} \qquad \text{[II.3-8]}$$

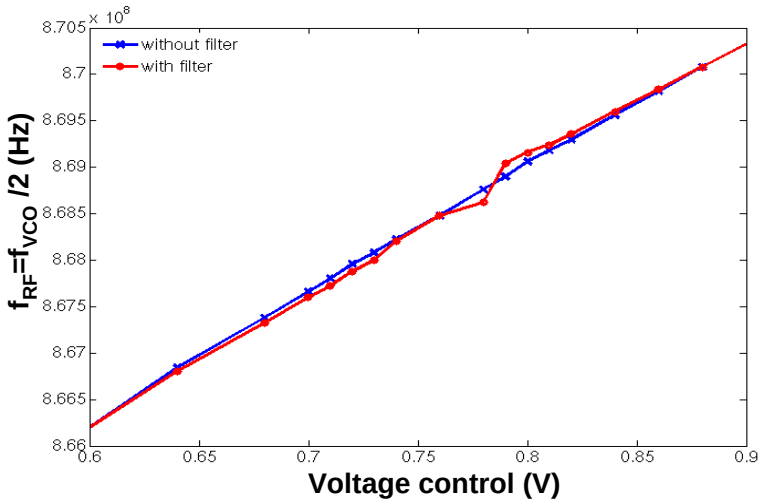


(a) **(b)**

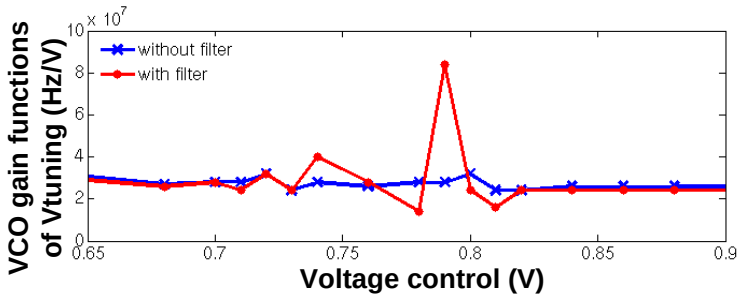
Figure II.3-5: Measured characteristics of the SAW filter used: Input impedance (a), frequency responses S21 and transfer function H (b)

"SAW matched" stands for the SAW reported on its PCB adapted to 50Ω, "SAW alone" for only the IC (data given by the constructor).

To investigate the impact of the SAW filter on system-level pulling, the characteristics of the oscillation frequency against the tuning voltage is measured with and without the filter. Figure II.3-6 (a) & (b) show both characteristics of the transmit path with and without SAW filter. It is observed that when the SAW filter is incorporated, ripple in the oscillation frequency appears for specific values of the tuning voltage and at control voltages of the VCO that correspond to the high cut-off frequencies of the filter, the VCO gain is no longer at 30MHz/V as desired but much more higher . However, while increasing one parameter of the PLL transfer function without compensation through another PLL parameter, the PLL may become unstable.



(a)



(b)

Figure II.3-6: Working frequency of the module functions of the integrated oscillator tuning voltage disconnected to the PLL (a) and the VCO gain (b) while inserting or not the very narrow band SAW filter

When changing the filter by a less restrictive filter as the EPCOS SAW B3715 (with a centre frequency of 869MHz, a wider bandwidth, a lower Q-factor of 434.5 and smother slope at cut-off frequencies), stability is regained.

It is then the rapid frequency variation of the filtering solution used that emphasizes the VCO/PLL pulling issue.

Some function blocks inside the IC have also an impact on the pulling effect, among others the power amplifier and its output power level.

b. Effects of the Power Amplifier on the Pulling

The PA Amplitude Level

The power amplifier (PA) of the LoPSTer is a Class E type [134]-[135] where the PA transistor operates as an on/off switch and the load matching network shapes the voltage and current waveforms to prevent simultaneous high voltage and high current in the transistor to minimize power dissipation and ideally offer a DC-to-RF power conversion efficiency of 100 percent. The output power P_0 of the IC is tuneable from the supply voltage Vcc of the power amplifier. At first approximation, Raab in [135] computed an expression of P_0 for an ideal Class-E PA as:

$$P_0 = \frac{Vcc^2}{1.7337 \cdot R} \qquad \text{[II.3-9]}$$

with R the load to present to the ideal matched class-E PA.

In Figure II.3-7, when the output power level of the TX system initially at Pout ~10dBm (for Vcc at 1.5V) is increased to ~12dBm (for Vcc =1.75V), critical spurs level around f_{RF} is detectable: a typical pulling behaviour is obtained when the supply voltage Vcc of the PA block is increased.

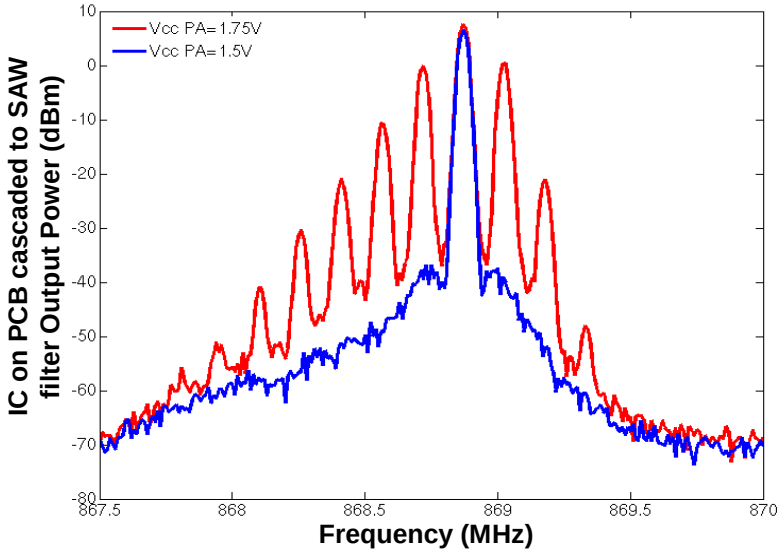


Figure II.3-7: Measured output power spectrum of the IC reported on its PCB, cascaded to the SAW filter PCB at f_{RF}=868.87MHz, functions of the supply voltage of the PA.

The PA output spectrum

From a spectral analysis point of view, the analytic derivation of the PA class-E waveforms (see Appendix A.3) leads to a transistors direct output voltage v_D presenting a second harmonic comparable in power to the fundamental tone at f_{RF} as shown in Figure II.3-8. As the local oscillator frequency f_0 of the PLL is working at a frequency equals to 2× f_{RF}, the coupling with the PA might create noisy interferences.

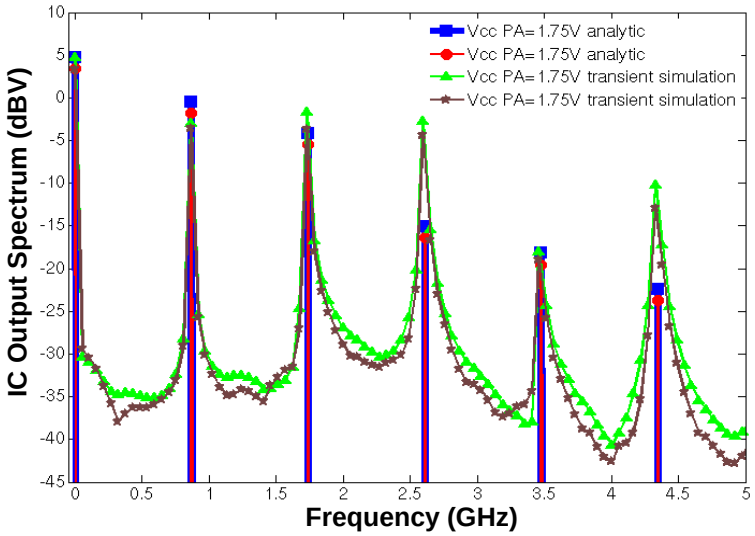


Figure II.3-8: Spectrum of the PA class-E transistors output

However, it is also to be noticed that measurements with a 434 MHz LoPSTer board followed by an EPCOS B3760 SAW filter, centred in 433.92MHz of 680kHz bandwidth and with a Q factor of 638.12, shows the same instable TX spectrum [136], whereas the ratio between f_{RF} and f_0 output frequency of the VCO is now 4. We can wonder if, as obtained in transient simulation (see Appendix A.2), the amplitude of the third harmonic of the PA is strong enough to couple with the oscillator signal by retroaction.

c. The Power/ Ground Distribution Network

At board level, the LoPSTer evaluation board has two supply connectors, Vcc LOPSTER and VCCBOARD.

Vcc LOPSTER supplies the LoPSTer transceiver IC as well as the digital ICs interfacing with LoPSTer. The supply voltage range on this connector is of 2.1 V to 3.6 V, typically 2.8V for the characterization. The supply voltage applied to Vcc LOPSTER is split into several paths; each of them is routed over a jumper and separate bypassing capacitors to the individual functional blocks it supplies. The jumpers can be used to temporarily disconnect the supply of a specific block or to insert an amperemeter for measuring the supply current of this block.

VCCBOARD supplies the MAX3232 level shifters [137] as well as the on-board digital-to-analog converter. The supply voltage range on this connector is of 3.3 V to 5.5 V, typically 3.3V for the characterization.

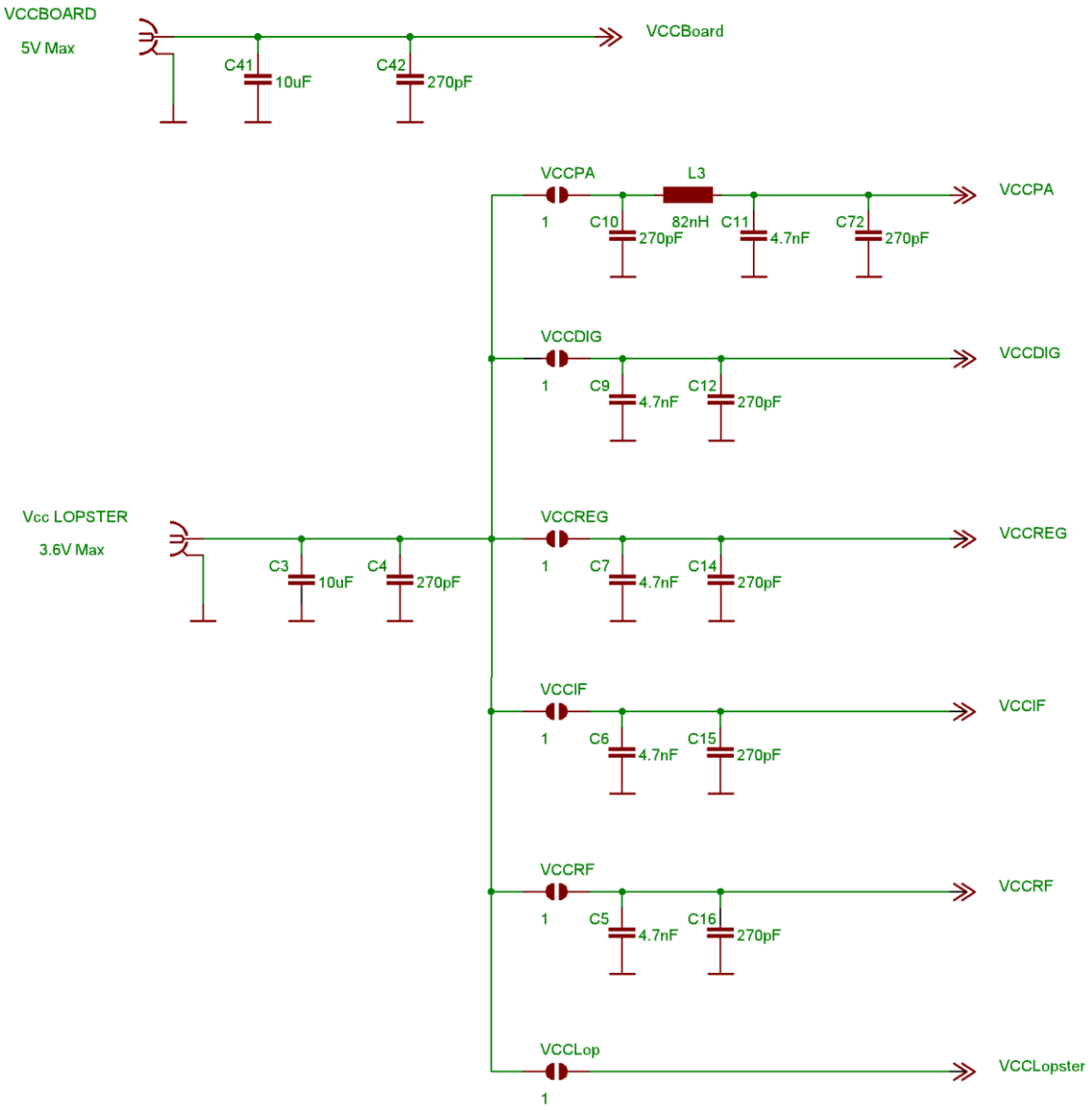


Figure II.3-9: Power supply distribution of the LoPSTer test board

In order to stabilize and isolate the supply of certain functional blocks such as the power amplifier, the VCO, the PLL and the digital circuitry, voltage regulator blocks are built-in into the LoPSTer. Each of these regulators needs an external bypassing capacitor for improved high frequency rejection and to ensure stability. The evaluation board contains those decoupling capacitors as well as test points at the regulators outputs. Measurement of the regulated voltages is then possible, and additional loads can be inserted in specific tests for testing the regulators and for overriding the regulator output with an external supply.

Concerning the ground distribution, as shown in the wiring diagram of the LoPSTer (Figure II.3-10), numerous pads of the IC are connected to the exposed die pad through downbonds namely the ground of the VCO, the ESD, the IF circuit, the LNA, the PA, the PA drivers, the PA output, the XO buffers, the PLL the regulator ground but also the guard ring of the IC polarized to the ground. It is also to be noticed that as many ICs, the functions blocks ground are connected to the ESD ring through antiparallel diodes.

The ground part of the exposed die pad is connected to the ground of the evaluation board by direct contact.

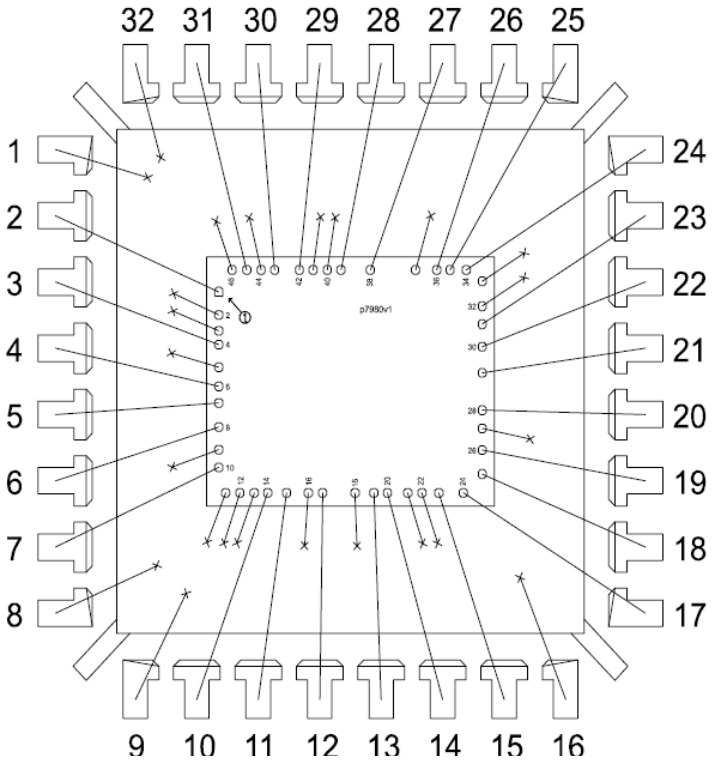


Figure II.3-10: Wiring Diagram of the p7980v1 (LoPSTer)

By making an inventory of the supply and the ground distribution, we can note that some function blocks share the same ground and power supply: it is the case of the RX LO dividers, which are physically closed to the VCO (see LoPSTer's layout in Figure I.4-2 (a)), and the power amplifier as seen in Figure I.4-2 (a) in chapter I.

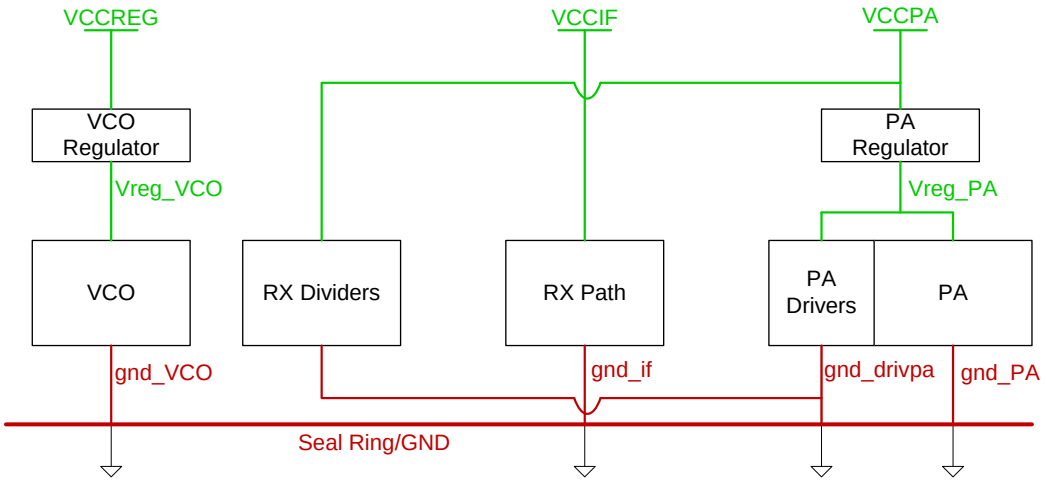


Figure II.3-11: Examples of function blocks that have the same ground and supply intervening into the PA and the VCO coupling: the Rx divider, the transistors of the PA and the regulators of the PA

The paragraph b permitted to underline the PA effect on the pulling issue. In this paragraph we will see how the parasitic signals from the PA come back to the PLL function block.

To investigate the coupling paths involved in the system pulling issue, redesigns were performed on the initial version of the IC in order to enhance the spectrum purity of the TX signal. To quantify the sensitivity of the ICs towards their output, a figure of merit Q_{EXT} was derived:

$$Q_{EXT} = \frac{f_{RF}}{\Delta f_{lock}} \sqrt{\frac{P_{lock}}{P_{RF}}} \qquad \text{[II.3-10]}$$

with f_{RF} and P_{RF} respectively stand for the output frequency and power of the IC on PCB measured without the SAW filter. A sinusoidal signal of power P_{lock} and frequency f_{lock} is injected at the output of the Matching Network. The frequency range in which the PLL works at f_{lock} instead of f_{RF} is noted Δf_{lock}.

Before implementing properly the different modifications to the final version of the IC, the redesigns were done through FIBs (Focused Ion Beam) by cuts and straps of the suspicious signals that can bring a return path of the PA noise to the PLL, that are:

- the supply of the PA (regulator): VCCPA, in common with the RX dividers supply
- the ground of the PA outstage transistors: gnd_PA, which is the ground reference of the output TX signal, but with no direct link to the RX dividers
- the ground of the power amplifier (pre-) drivers: gnd_drivpa, in common with the RX dividers ground.

The partial modifications on potential noisy blocks and the observed measurement results are given in the following table.

Table II.3-I: Evolution of the IC designs by FIBs

FIB #	Operated FIB Modification	Observed Measured Effects	QEXT
V1 (Initial version)	All grounds are connected through the seal ring(*), The RX dividers are close to the VCO and share their ground with the PA drivers and their supply with the PA regulator.	Pulling issues at cut-off frequencies of the SAW filter	typical: 1500
1	Isolation of the RX part to the TX part: Strap between the seal ring and RF_in	Pulling issues at cut-off frequencies of the SAW filter	1887 (at f=868MHz)
2	Isolation of the VCO to the PLL loop:Cut at loop filter output, external tuning voltage of the VCO	Pulling issues at cut-off frequencies of the SAW filter	1771 (at f=868MHz)
3	Cuts of seal ring around the PA: isolate gnd_PA, gnd_drivpa, (and also rf_out, reg_pa) to the seal ring and the other ground	No pulling when the LoPSTer is loaded by the SAW filter + 50Ω but persisting pulling issue at cut-off frequencies of the SAW filter when the antenna load is desadapted , with a SWR of 6	2713 (at f=868MHz)
4	Cut to isolate gnd_PA to the seal ring	No pulling when the LoPSTer is loaded by the SAW filter + 50Ω but persisting pulling issue at cut-off frequencies of the SAW filter when the antenna load is desadapted , with a SWR of 6	4384 (at f=868MHz)
5	cut of Vcc_PA path to Rx dividers supply	No pulling when the LoPSTer is loaded by the SAW filter + 50Ω but persisting pulling issue at cut-off frequencies of the SAW filter when the antenna load is desadapted , with a SWR of 6	2568 (at f=868MHz)
6	cut seal ring around the PA + cut of Vcc_PA path to Rx dividers	No pulling when the LoPSTer is loaded by the SAW filter + 50Ω but pulling issue at cut-off frequencies of the SAW filter when the antenna load is desadapted , with a SWR of 6	4173 (at f=868MHz)
7	Cut to isolate gnd_PA to the seal ring + cut of Vcc_PA path to Rx dividers	No more pulling issue	6028 (at f=868MHz)
8	Cut the path to the ESD diodes (**) on the transmit/output pad: the output signal of the IC is isolated to the rest of the chip	No pulling when the LoPSTer is loaded by the SAW filter + 50Ω but pulling issue at cut-off frequencies of the SAW filter when the antenna load is desadapted , with a SWR of 6	1528 (at f=868MHz)
9	cut to isolate gnd_PA from gnd_ESD, from the seal ring and the other grounds of the circuit	Pulling issues still remain at instable frequencies	1089 (at 810,7MHz)
10	Cut and strap the VCC and the ground of the RX dividers to another supply and ground distribution	No pulling effects when IC on PCB-test was connected to SAW filter 50Ω loaded or desadapted	3272 (at f=871,32MHz)
11	cut to isolate gnd_PA from the seal ring + cut & strap Vcc and the ground of the RX dividers to another supply and ground distribution	System stable at high cut-off frequency of the SAW but still with little spurs around fRF at its low cut-off frequency when the antenna load is desadappted to 50Ω	4106 (at f=867,4MHz)

(*) seal ring: ring consisting of all metallization layers of the technology used, connected to each other through rails of vias, and the lower metalization layer is connected to thesubstrate. The purpose of the seal ring is to encapsulate the die edge after chip dicing.
(**) ESD diodes: unidirectional ElectroStatic Discharge (ESD) protection diodes.

Table II.3-I shows the observed results at the output of the chip-package-PCB in terms of frequency spectrum but let's also look at the impact of the ground/power distribution amelioration at the VCO standpoint. We can see that by isolating the ground and the supply of the PA, the figure of merit of the application increases: the immunity to external noise is improved, but it is not sufficient to eliminate the pulling issue (FIB #1, 2, 3, 4, 9). In the same

manner by decoupling the supply of the PA and the RX dividers, Q_{EXT} increases but persisting pulling can be observed when the antenna load is not exactly 50Ω. The best result is obtained when combining the isolation of the ground of the PA transistors and TX_out (the most contaminated ground) and decoupling the supply of the PA and the RX LO Divider (FIB #7), but by simply decoupling the supply of the PA and the RX divider, the ground of the PA drivers and the RX Dividers, the pulling effect are also undetectable at the cut-off frequencies of the SAW filter (FIB #7).

It could have also been interesting to have the results of the decoupling between the ground of the RX dividers and the PA drivers alone, but as a capacitor connect the supply to the ground of the RX dividers, the two paths are anyway linked.

As seen in Figure II.3-6, while inserting the SAW filter between the IC PCB and the load, the VCO gain is strongly damaged at the cut-off frequencies of the SAW filter. How does K_{VCO} vary with the redesigns done?

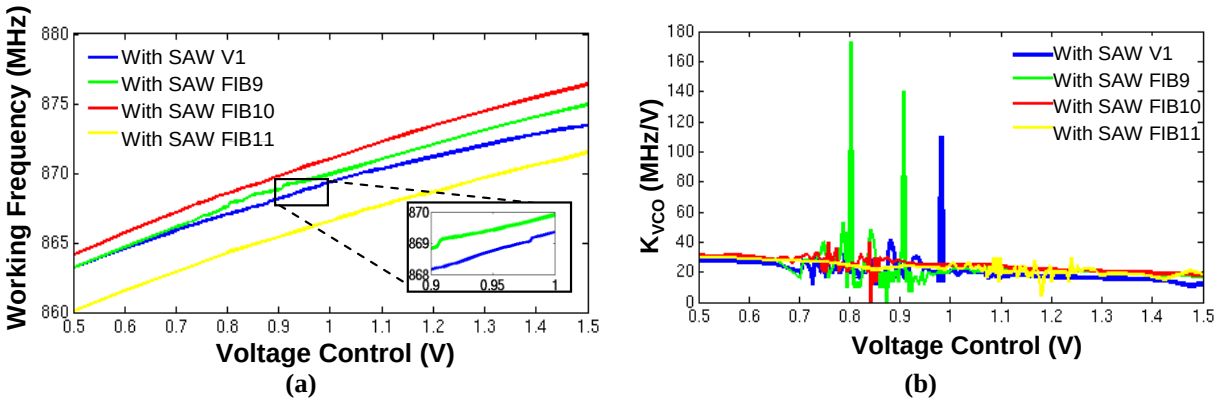


Figure II.3-12: Measured working frequency (a) and variation of the VCO gain (b) of the different IC versions in function of the control voltage of the VCO

As we can see in the previous figure with the red and yellow curves, while decoupling the ground and the supply of the RX dividers and the power amplifier, the frequency leap in functions of the voltage control of the VCO is no longer present, in addition the VCO gain curve no longer presents a peak value at the voltage control that leads to cut off frequencies of the SAW filter.

At system-level, coupling mechanisms that originate from the interaction of the PLL with the PA through power/ground distribution network are considered as potential source for pulling effects- together with effects resulting from incorporation SAW filter on PCB.

d. Frequency pulling/pushing due to noises on the supplies

While adding a sinusoidal noise of frequency ω_Δ to the supply voltage of the PA or the VCO, pulling or more precisely pushing phenomenon is obtained for the free running VCO as well as for the VCO connected to the other blocks of the PLL.

Supply of the VCO: noise on Vreg_VCO

Experimental results as well as simulation results issued from circuit model for the VCO are given in Figure II.3-13 for a variation of Vreg_VCO around 1.8V. As the exact supply access is not modelled, the amplitude of the supply voltage variation is taken to be of 5mVpp for the transient analysis of the transistor model of the oscillator, whereas an amplitude of 50mVpp is used in measurements. Number and amplitude of the spurs depend on the amplitude of the noise injected and pulling effect is amplified by the charge pump

current level if the VCO is connected to the PLL. A periodic noise on the VCO supply can then be integrated into the oscillator loop and transmitted to the VCO output through modulations around f_{VCO} as pulling phenomenon.

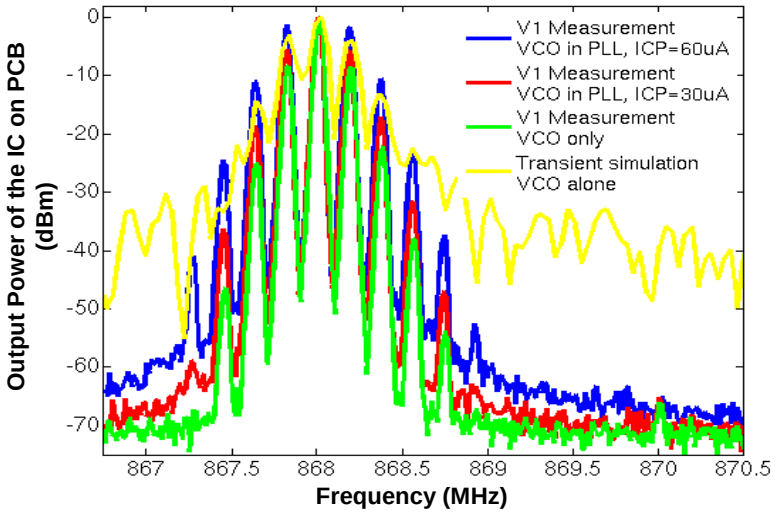


Figure II.3-13 : Normalized output power spectrum when a sinusoidal noise is applied to the VCO supply

Supply of the PA : noise on Vreg_PA

Figure II.3-14 shows that the output signal of the LoPSTer reported on its evaluation board is sensitive to the PA supply noises. As the analysis of the whole transmit path is time and memory consuming at transistor level, only measurement results are given in Figure II.3-14 for the injection of a sinusoidal noise of amplitude 45mVpp into the PA supply: Vreg_PA.

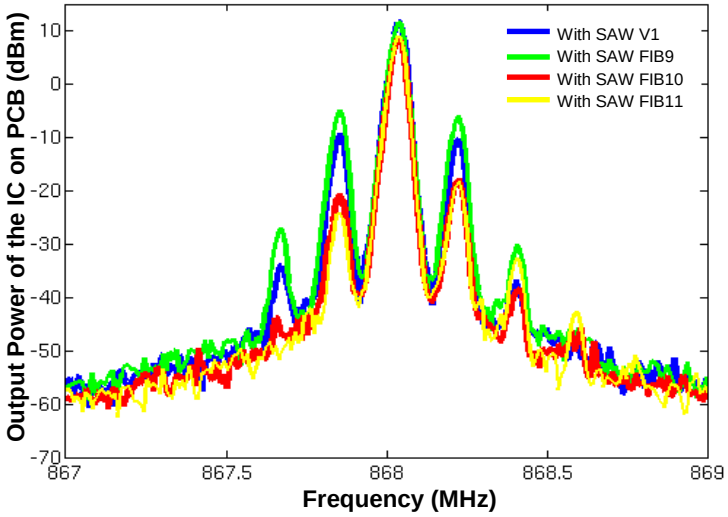


Figure II.3-14: Measured output power spectrum of the different ICs on PCB when a sinusoidal noise of 45mVpp is applied to the PA supply

The above figure underlines that a coupling issue between the VCO and the PA can then cause frequency pulling. In addition, the VCO is less influenced by the injected noise when blocks in the VCO neighbourhood don't share the same ground as the PA driver and the PA regulator supply (in reference to FIB10 and FIB11 of Table II.3-I).

As the VCO and the PA do no share any direct path, the pulling issue observed is due to EM couplings phenomenon.

II.3.3.Main Observations at Chip-Package-PCB Interaction Level

a. The Parasitic Capacitances Effects

The power amplifier stage of the LoPSTer is composed by on chip components (the transistors) but also on PCB with the SMDs matching circuit components.

In 'on' state, the transistors of the PA are equivalent to a low resistance Ron, and in 'off' state the transistors acts as an open switch of capacitance Cpa. Yet the ideal load R to be presented to the PA depends on the shunt capacitance Cpa to fulfill the class-E functioning, then the PA output power level can also vary with Cpa.

$$R = \left(\frac{1}{\pi \cdot \omega \cdot Cpa} - Ron\left(\frac{3}{4} + \frac{\pi^2}{16} \right) \right) \cdot \frac{2}{\frac{\pi^2}{4} + 1} \qquad \text{[II.3-11]}$$

However, the effective capacitance of the PA should include both the intrinsic transistor capacitance Cpa, the load (including the matching) network capacitance but also an external equivalent capacitor ΔC which is due to parasitic capacitance from the PCB. Figure II.3-15 shows a simplified view of the PA where the different parasitic capacitances impacting the PA performance are reported, namely C_{IC} and C_{PCB} respectively from the IC and PCB.

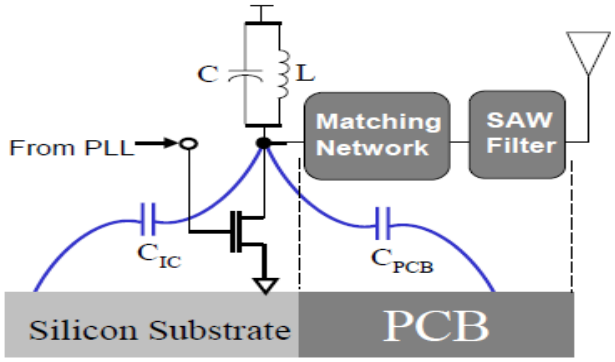


Figure II.3-15: Influence of combined parasitic capacitances of IC and PCB contribution on PA performances

Assuming a relative variation of parasitic capacitance ΔC cumulating the IC and PCB parasitic effects, Figure II.3-16 shows the importance of proper estimation of the parasitic capacitance ΔC to estimate the PA output power. Since the observed pulling sideband spurs strongly depend on the PA output power level (see Figure II.3-7), it is essential to take into account IC-package-PCB coupling upfront in the early design steps to avoid problems during chip debugging.

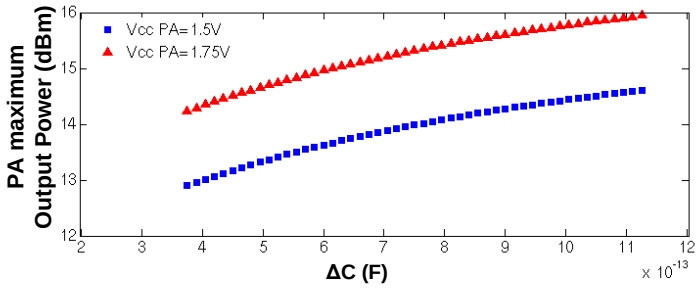


Figure II.3-16: Variation with the parasitic capacitance ΔC of the maximum output power of the IC reported on its PCB at f_{RF}=868.87MHz derived analytically

II.4. EM Analysis of VCO Pulling in Integrated PLL Systems

We saw that the reported VCO pulling/pushing issues can result from interactions between the VCO, the PLL, the power amplifier, the filter, the power supplies and ground. Those interactions come from direct injection of noise or couplings.

In this paragraph, we will consider EM couplings between two metallizations that can lead to pulling issues.

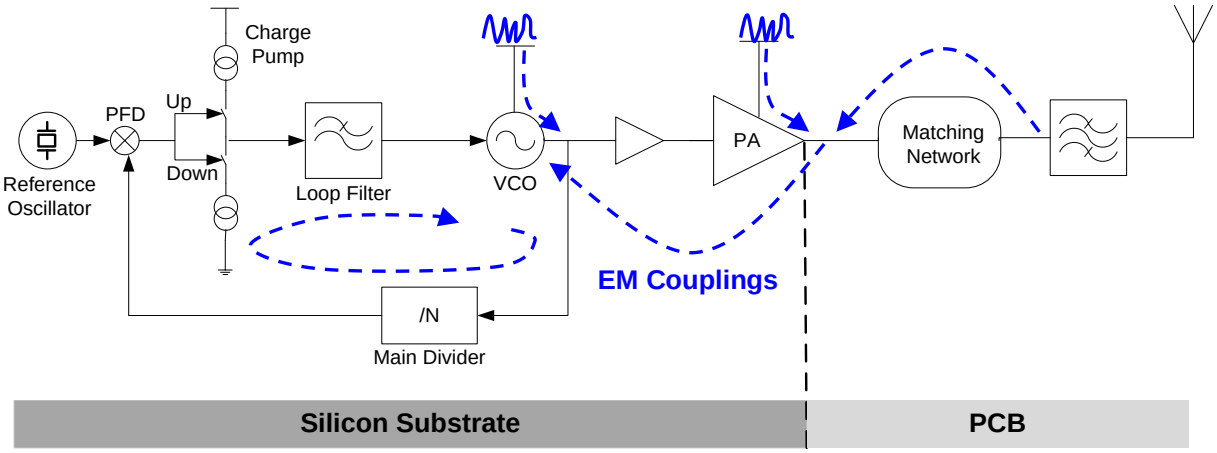


Figure II.4-1: Pulling and pushing effects taking place in Chip-Package-PCB system paths

II.4.1.The Tank Inductance & Inductive Coupling

As it is showed in Figure II.4-2, a basic model of an oscillator can be represented by a basic model of a L, C, gp parallel circuit equivalent to the lossy tank and an effective negative conductance –Gm of the active devices to compensate the tank losses. The oscillator oscillates initially at a frequency f_0:

$$f_0 = \frac{1}{2\pi\sqrt{Ltank \cdot Ctank}} \qquad [II.4\text{-}1]$$

We will consider that the oscillator is subjected only to magnetic coupling: its tank inductance Ltank is coupled through a mutual inductance M with an external inductance Lp crossed by a current $I_P(t)$ as described in Fig. II.4-2. The coupling coefficient k between the two inductors is defined as the ratio of mutual inductance between the two inductors to the geometric mean of their self inductances [139]:

$$k = \frac{M}{\sqrt{L\tan k \cdot Lp}} \qquad [\text{ II.4-2}]$$

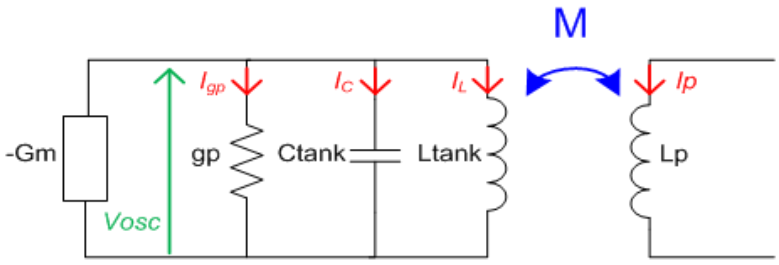


Figure II.4-2: Electric scheme of an LC-oscillator inductively coupled with another metallization

The output sinusoidal voltage of the oscillator Vosc(t) has the form:

$$Vosc(t) = V_0 \cdot \cos(\omega_{osc} \cdot t) \qquad \text{[II.4-3]}$$

But considering the inductance couplings, the Kirchhoff's current law of the circuit gives:

$$Vosc(t) = L\frac{dI_L(t)}{dt} + M\frac{dI_P(t)}{dt} \qquad \text{[II.4-4]}$$

II.4.2.Inductive Coupling to Injection Pulling

If the oscillator sustains a perturbation at a frequency nearby f_0, at $f_0 + \Omega_m$, through an inductive coupling between the tank inductor and an external metallization, equation [II.4-4] becomes:

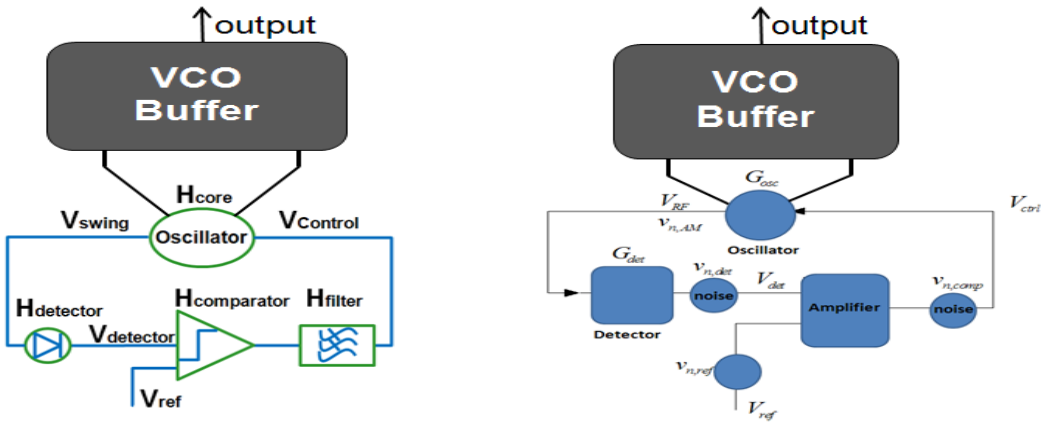
$$\begin{aligned} Vosc(t) &= L\frac{d(I_L(t))}{dt} + M\frac{d(I_P(t))}{dt} \\ &= L\frac{d(I_L \cdot \sin(\omega_0 t))}{dt} + M\frac{d(I_P \cdot \sin((\omega_0 + \Omega_m)t))}{dt} \\ &= L \cdot \omega_0 \cdot I_L \cdot \cos(\omega_0 t) + (\omega_0 + \Omega_m) \cdot M \cdot I_P \cdot \cos((\omega_0 + \Omega_m)t) \end{aligned} \qquad \text{[II.4-5]}$$

A signal of frequency near to the oscillator one is (re-)injected into the oscillator / PLL loop whose injection level directly depends on M, the mutual coupling between the tank inductor and the external metallization.

In order to reduce pulling issues due to possible EM couplings, inter-blocks EM couplings analysis should be considered and assessed. A methodological approach for EM analysis should be developed.

II.4.3.Importance of Capacitive Coupling

Importance of capacitive coupling is investigated for an integrated VCO working at 10 GHz including an Amplitude- Level-Control (ALC) . The VCO-core is buffered using a CML circuit, as indicated in Figure II.4-3 showing functional description of the VCO with its ALC. The function of the level detector is to detect the amplitude of the RF oscillator signal and translate it into DC voltage value. The function of the loop amplifier is to deliver the biasing voltage for the oscillator block from the error signal based on the difference between the detected signal and the reference signal level. The whole loop control helps in ensuring stability of the oscillation amplitude over process, voltage, and temperature (PVT) variations for low noise performances together with effective oscillation settling.



(a) **(b)**

Figure II.4-3: Functional representation of the VCO block with its amplitude control loop

The amplitude V_{RF} of the oscillator output is extracted from the loop system and reference voltage value V_{ref} following the equation:

$$V_{RF} = \frac{G_{osc} A V_{ref}}{1 + G_{osc} A G_{det}} \qquad [II.4\text{-}6]$$

where G_{osc} is the VCO active-core gain, A the amplification gain.

When the oscillator is modelled as a simplified equivalent parallel RC circuit model, sensitivity to extract parasitic is observed in our case by extracting a start-up ratio parameter (*defined as ratio of tank conductance and active-core conductance*) given in Figure II.4-5. Figure II.4-4 shows the test-bench circuit of the VCO including ALC circuit and buffering module.

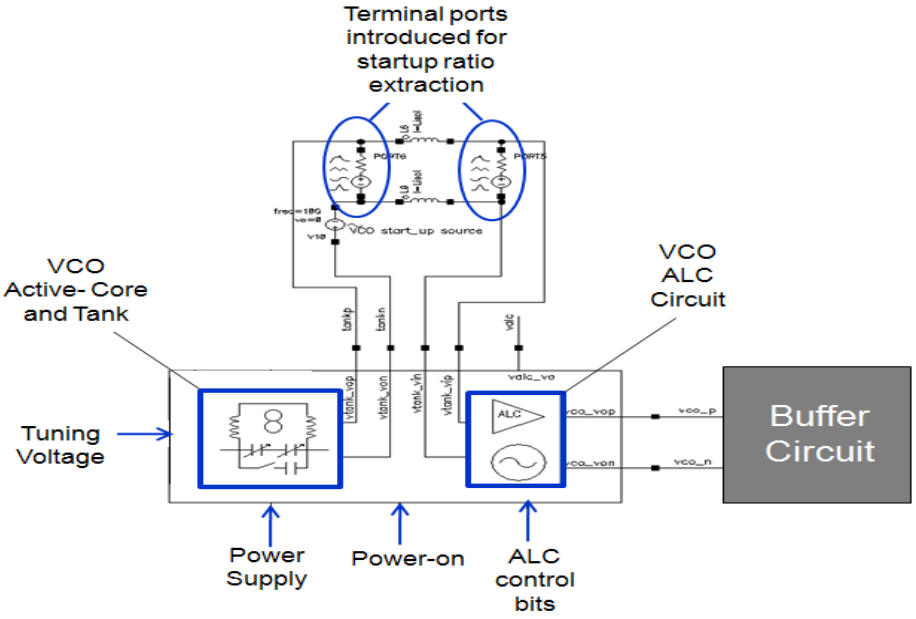


Figure II.4-4: VCO test-bench including ALC circuit and buffering module

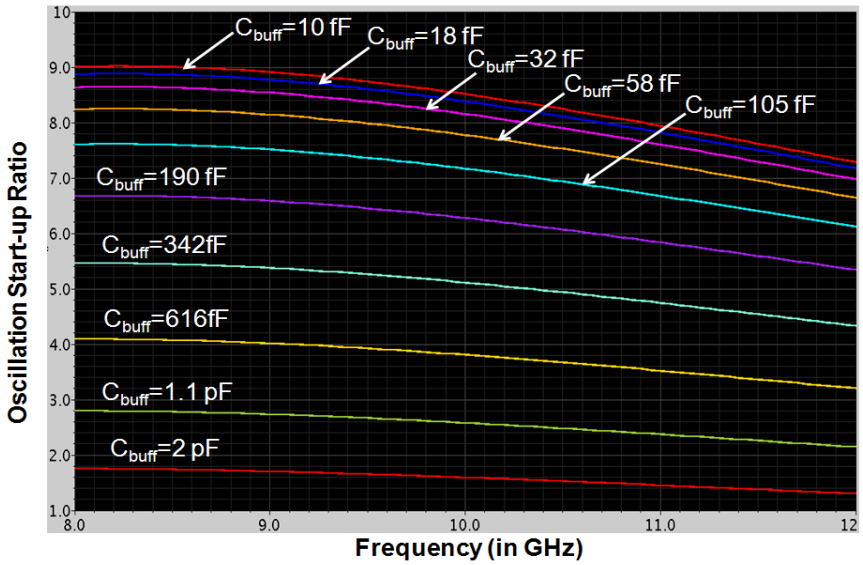


Figure II.4-5: VCO start-up ratio as function of buffer extracted input capacitance

Variation of C_{buff} (in the inset of Figure II.4-5) that actually represents both active circuit and interconnect line parasitic clearly shows that parasitic capacitance of the VCO buffer has strong impact on oscillation start-up ratio.

The buffer parasitic capacitance can be split into two major contributions: one contribution resulting from interconnect lines and one due to the buffer active circuit itself.

Figure II.4-6 shows a top layout view of the system application where the VCO block and its buffer circuit including interconnection lines to mixer block are highlighted:

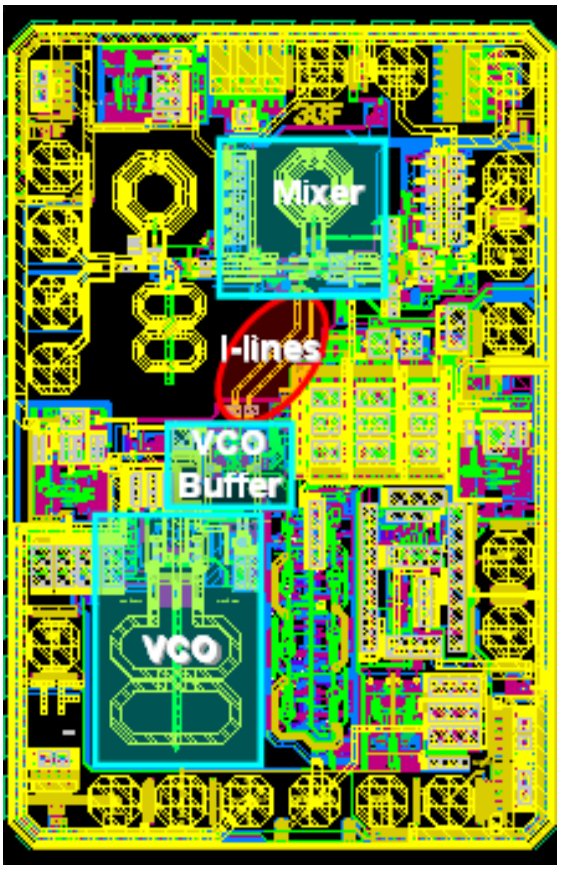


Figure II.4-6: Top layout view of LNB satellite application showing position of VCO module and its buffer module with interconnect lines to mixer block.

Full-wave analysis of top-level critical components (namely inductors, rings and loops) is carried out to extract coupling parameters between the selected nodes (VCO, LNA, Mixer, etc...). Obtained full-wave analysis results are used to extract lumped-elements circuit models for back-annotation into time-domain circuit simulator (e.g., Cadence Spectre, ADS, etc...).

II.4.4.Full-Wave EM Simulations for Predictive Coupling Analysis

a. Numerical Methods for EM Simulations

The FDTD Method Formulation

The FDTD (Finite Difference Time Domain Method) [139] is a computational method using grid-based time-domain numerical analysis for solving Maxwell's equations. The resolution process uses partial differential formulation of Maxwell's equations. Central or non-central difference approximations are implemented to cast formulation of Maxwell's equations in the form of finite difference equations to be solved though a time-stepping process. The computational domain is dicretized into elementary cells (Yee's cells [140]) with specification of physical properties attached to each cell (e.g., permittivity). The FDTD approach calculates the electromagnetic fields, at each time-step, in all cells of the discretized

computational domain following specified excitation sources. When transient convergence or steady-state stability is reached, all electromagnetic field components are extracted and can be used in post-treatment to derive broadband frequency-domain parameters such as S-parameters, Z or Y parameters. Strong advantage of FDTD formulations lies in the broadband characteristics of extracted frequency-domain parameters [141]. Main limitations concern difficulties to handle multi-layered structures where there is big discrepancy in physical dimensions imposing demanding CPU resources, convergence and accuracy issues as well. Generally PML layers [142] are incorporated at the borders of the simulation domain for boundary conditions matching to avoid computing large domains which involve huge memory requirement. Including frequency-dependant losses remains a challenge for FDTD approaches.

The Method of Moments and Hybrid Formulations

The MoM (Method of Moment) [143] is a computational method aiming to solve Maxwell's equations in the frequency-domain using their integral form [144]. Whereas its general formulation can be used for any structure geometry, the formulation we have chosen is limited to homogeneously layered media, as the number of unknown can be drastically reduced in this case, and thus the studied domain increased: the complex problems with important number of ports is accessible when multi-layered structures are uniformly homogeneous. The discretization uses generally a regular or adaptive 2D meshing procedure. Current-Density formulations use conducting surfaces as primary domain unknowns while Electric-field formulations use the dual domain. Based on a direct resolution or iterative resolution distribution of electric and magnetic fields are computed. Green's functions are determined to incorporate in the analysis effects of surrounding material (dielectrics) [145].

During the resolution process, basis functions (in general rooftops) are used to expand the distribution of the unknowns (electric field or current density), and testing functions are considered as well to impress boundary conditions. This leads to convert the integral equation into a system of linear equations. Extraction of electromagnetic fields relative to specified excitation sources gives the RF parameters such as Z,Y,S-parameters. The MoM approach lacks time-domain information since it is a frequential formulation. The method is suitable for including frequency-dependant losses and thick conductor models.

On the other hand active research area is on developing hybrid EM formulations combining different fundamental integral and differential approaches for the resolution of Maxwell equations performed in an iterative way or based on a direct inversion procedure.
Resorting to network theory [166][167] provides unifying approach for combining different approaches and methods, each specific method being convenient for the appropriate computational sub domain. This opens avenues of potential directions for complexity reduction of EM analysis through the hybridization of various methods and circuit analysis techniques. It is in this scope, that hybridization of Transmission Line Matrix method (TLM) with Transverse Wave Formulation (TWF) method has been proposed in [168]. When combined with the formalism of auxiliary sources [169] global co-analysis of active and passive systems can be formally derived.

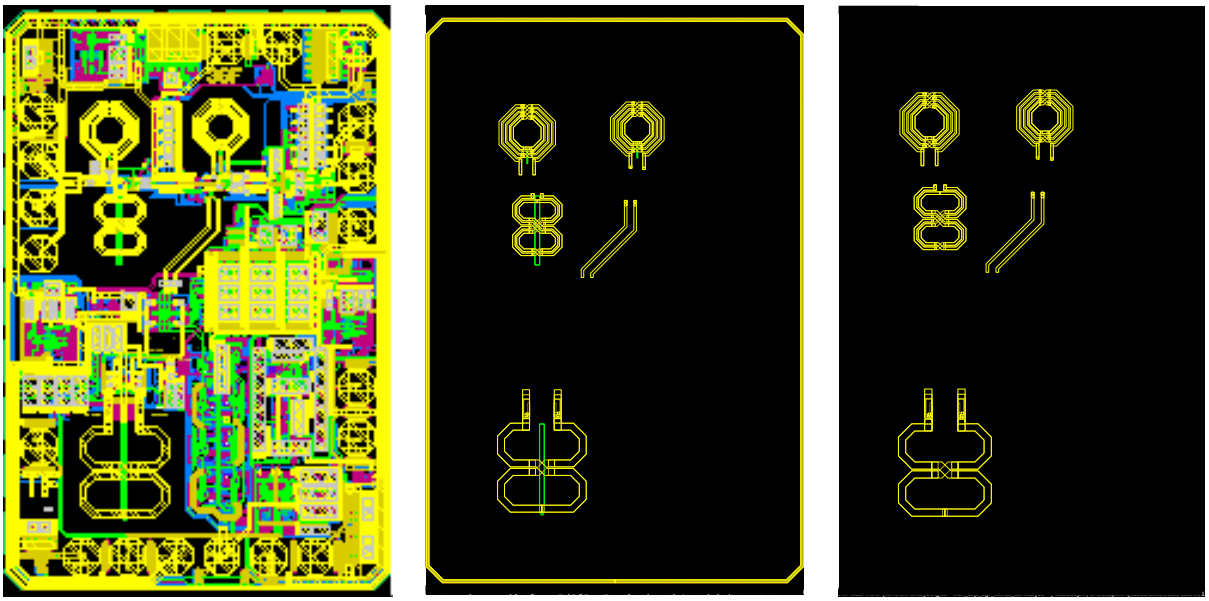
b. EM Simplifications & Assumptions

We have seen in the previous paragraph the different constraints of the numerical methods to solve the equations governing the EM analysis. Thus, in order to analyze the electromagnetic interactions inside an IC, simplifications should be done before.

Layout Topology Simplification

In transceiver cases, the IC comprises several inductors as in VCO, LNA, Mixer..., transmission lines and other loop as the seal/guard ring. Take the example of Figure II.4-6: interactions between the different loops and principal transmission lines are necessary to analyse, however actually, no EM tool using any kind of numerical method could afford to analyse electromagnetically an entire IC because of time and CPU constraints.

The analysis should then define a partitioning strategy in order to highlight the function blocks, the components or metallizations to be investigated and remove all the other elements from the layout to be analyzed.



(a) **(b)** **(c)**

Figure II.4-7: From the initial layout of the TFF1014 (a) to the loops analyzed by EM (c), and by taking into account the seal ring and the centertap DC access of the inductances (b)

In the chosen IC test case, the TFF1014, the inductances and the lines to be analyzed have non-rectangular edges: as the methods using rectangular and cubic cells (as Sonnet with the MoM and the FDTD) will require extensive memory and processing time to describe the component in staircase, conformal meshing [146][147][146] that consists in combining strings of cells following diagonal and curved contours, can be developed and apply to this kind of circuit allowing a significant reduction in memory and simulation time. For some simulations, we will use the conformal-mesh option of Sonnet [146].

To a layout topology standpoint, multiple turns octagonal inductances, due to crossings, are designed on 2 metal levels. In order to increase the 8-Shaped inductor quality factor by reducing the series resistance, the equivalent thickness of the inductor is increased [148] by using 2 metal levels. To connect the two metal levels, compact rows of vias are used as showed in Figure II.4-8 (b). Given the dimensions of the pattern, the via distribution should be simplified.

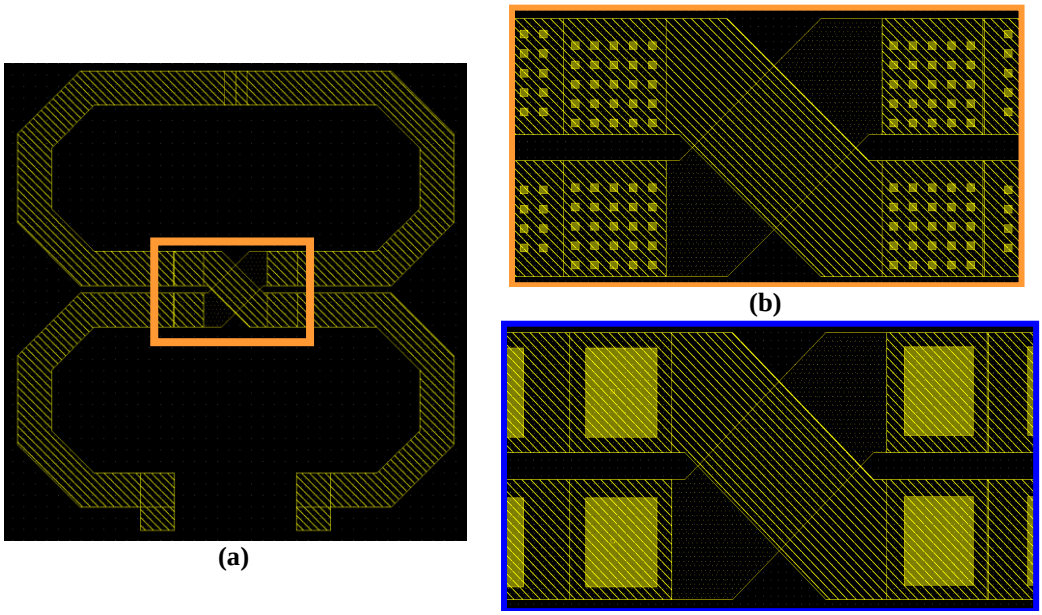


Figure II.4-8: Layout topology of a 8-shaped inductor with 2 levels of metallization (a) connected by rows of vias (b) simplified by stacks of vias (c)

Technology Stack Simplification

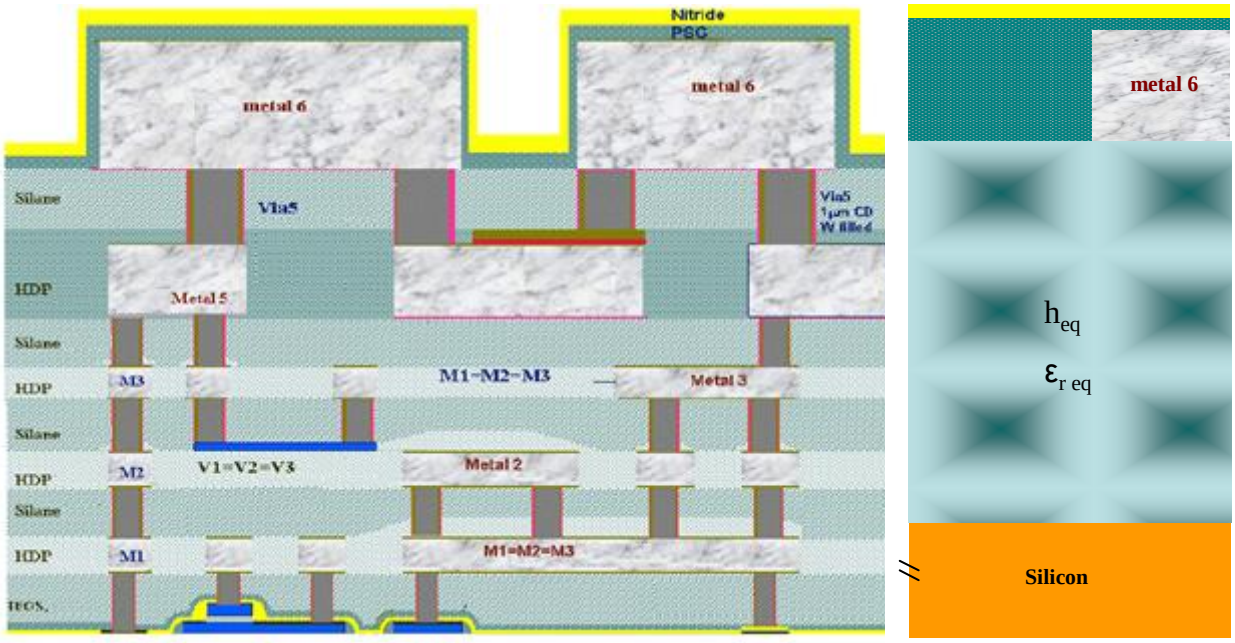
NXP's CMOS and BiCMOS technologies use several metallization layers more or less thick. Those at higher levels are physically thick thus used for designing inductances and transmission lines with few losses. Yet losses of inductors [148] and coupling between closely spaced conductors depends on the thickness of the metal type. For planar numerical methods, multi-sheet model to capture the effects of current penetration into the metal are developed [149][150][151] and should be used especially when two thick conductors are separated by less than the metal thickness. Although the expansion of the thick conductor requires more simulation time and memory, the results lead to more accurate simulation results.

In addition as seen in Figure II.4-9(a) NXP's QUBIC4X technology is composed by several dielectric layers of very different thickness: the silicon substrate of the technology is ~700µm whereas oxide and passivation layers can be 0.1µm, and different permittivity, permeability and conductivity. For that, the simplification of the technology stack is needed.

For *N* dielectric layers of thickness h*i* and of permittivity ε*i*, the multi-layer substrate can be simplified to only one layer of thickness equals to Σh*i* and of a global permittivity ε_{req} such as:

$$\varepsilon_{r\,eq} = \frac{\sum_{i=1}^{N} h_i}{\sum_{i=1}^{N} \frac{h_i}{\varepsilon_i}} \qquad \text{[II.4-7]}$$

For illustrating that, Figure II.4-9(b) shows a simplification of the passivation layers and different redundant dielectric layers valid for the upper level of metallization.



(a) **(b)**

Figure II.4-9: NXP QUBIC4X front end

Setting Excitation Port

For analyzing a lumped element of an IC generally connected to other components in a circuit, to inject energy into the analyzed circuit or component and measure the results in EM analysis, internal port are the most appropriated port type used. As a port contains two terminals (signal and ground), the ports connected to the surface of an object or at polygon edge of the analyzed object should be associated to a ground reference defined explicitly [153] or to a metal layer whose potential is fixed as the wall box of Sonnet.

However, the current return path is critical in a complex circuit analysis when the internal port is not calibrated. The simulation will take into account all the EM coupling effects that will occur within the circuit including also the coupling effects among ports caused by parasitics added by the return path [153]. The results will not be accurate; the difference in accuracy can be considered small enough [153] or dramatic [154] notably in high frequencies. For that, a perfectly calibrated internal port connection has been developed by Sonnet [155] in order to remove the port discontinuities and the effects of the local ground. The co-calibrated ports are associated with a calibration group and all of the ports in a calibration group that are placed close together share a common ground and are de-embedded simultaneously during the analysis to remove all cross-coupling between them.

c. EM Coupling Reduction: application on an RX path of a transceiver

In a transceiver as the TFF1014, the IC comprises several inductors and interconnection lines that can induce noisy couplings and interferences in particular for the VCO performances as seen in paragraphs II.4.2 and II.4.3. For this, some improvements can be incorporated into a design in order to reduce the parasitic couplings.

For investigating the inter-blocks EM couplings in the TFF1014, full-wave EM simulations for obtaining the couplings between all sensitive blocks were performed and isolation solutions were proposed concerning the shape and the orientation of inductors.

In Figure II.4-11 we can see that an inductor (element (3) in Figure II.4-11) is close to the coupled interconnection lines of the VCO buffer which are seen very critical for VCO

performances as it may induce coupling issues: could the replacement of the octagonal inductor by an 8-shaped inductor [156] reduce parasitic couplings?

Because of their twisted topology, 8-shaped inductors are expected to minimize EMI related couplings and interferences. In Figure II.4-10 spatial distribution of the magnetic field induced by the two twisted loops of the 8-shaped inductor demonstrated importance of symmetry assumptions. Beyond symmetry considerations, isolation and EMI performances remain strongly dependent on the coupling resulting from the twisting and the number of turns. 8-shaped inductor is used for the integrated LC-VCO (element (1) in Figure II.4-11) to lower EM noise[157]. We know that coupling level between an 8-shaped inductor and other metallization depends on its orientation and the distance between the components [158] paragraph 2.2.6. Has the 8-shaped VCO inductor the optimum orientation to lower parasitic couplings?

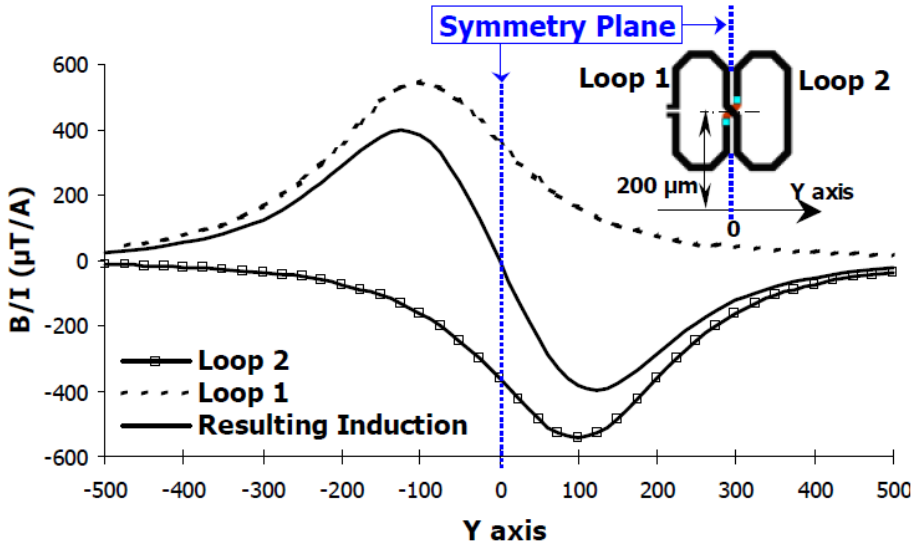
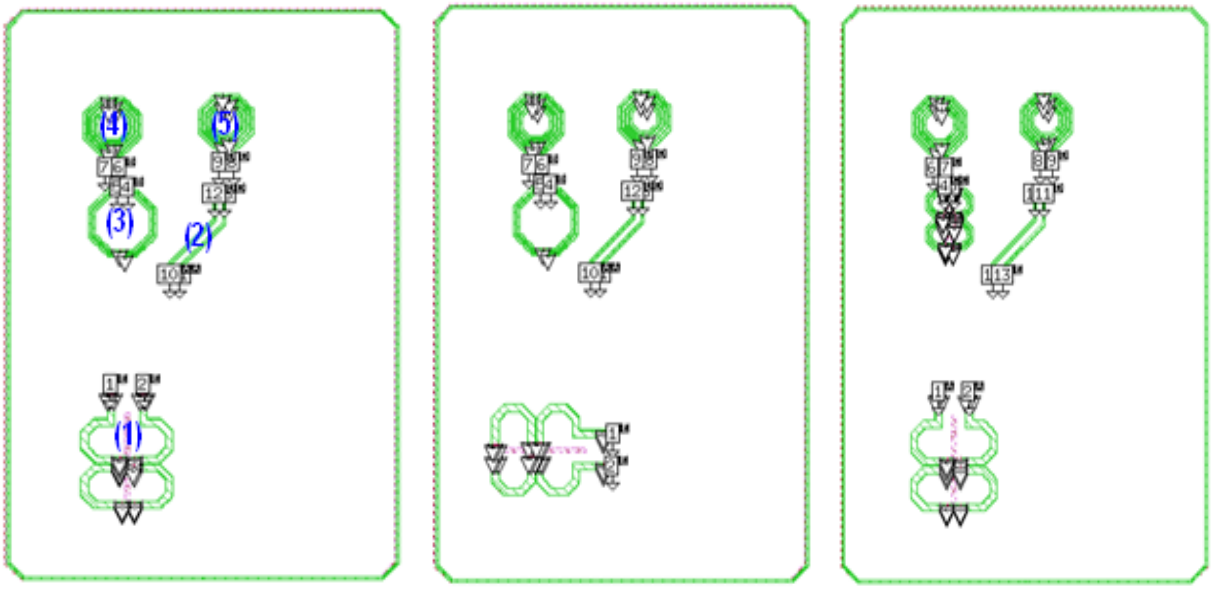


Figure II.4-10: Illustration of magnetic field (induction) distribution for the 8-shaped inductance along the Y axis, at 200µm from the loops center.

To deal with the previous questions, we proposed several evolutions of the TFF1014 layout to illustrate the effects of the 8-shaped inductor compared to octagonal topology Figure II.4-11(c), and to determine the optimum orientation of 8-shaped inductor to lower parasitic couplings Figure II.4-11(b).



(a) **(b)** **(c)**

Figure II.4-11: Evolution of proposed TFF1014 with principals loops and interconnects lines

EM simulations with the MoM showed that the couplings between the VCO inductance and the other principal metallizations of the IC do not produce convincing results as detailed in Figure II.4-12. Only 10dB of amelioration is obtained for the couplings between the inductor and the output of the interconnect line while turning the VCO inductance. However, the coupling value is already considered small enough in the initial version so that the redesign is not worth applying.

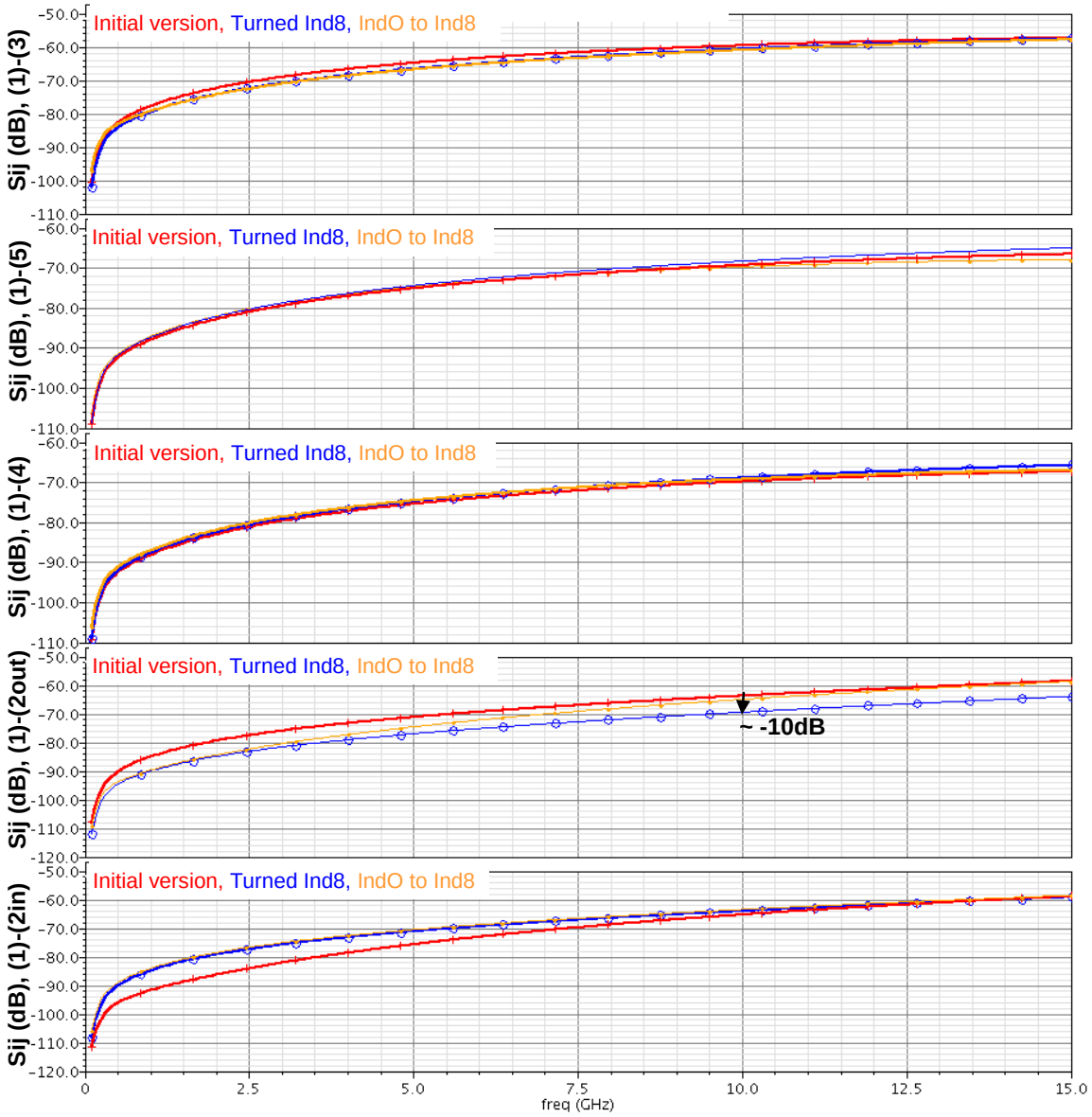


Figure II.4-12: EM Simulation results obtained with the MoM for the proposed different versions of TFF1014 at the VCO inductance viewpoint

In the figure above, the red curves “Initial version” are using the version (a) configuration of Figure II.4-11, the blue curves Turned Ind8 stands for the (b) configuration of Figure II.4-11 and the orange curves IndO are using the configuration (c) of Figure II.4-11.

For the coupling between the neighbouring inductance (structure (3) of Figure II.4-11) and interconnection lines (structure (2) of Figure II.4-11) on the other side, changing the type of inductor enhances the coupling between the inductor and the lines. The EM results obtained in Figure II.4-13 were validated by test-chip carriers defined in Figure II.4-14.

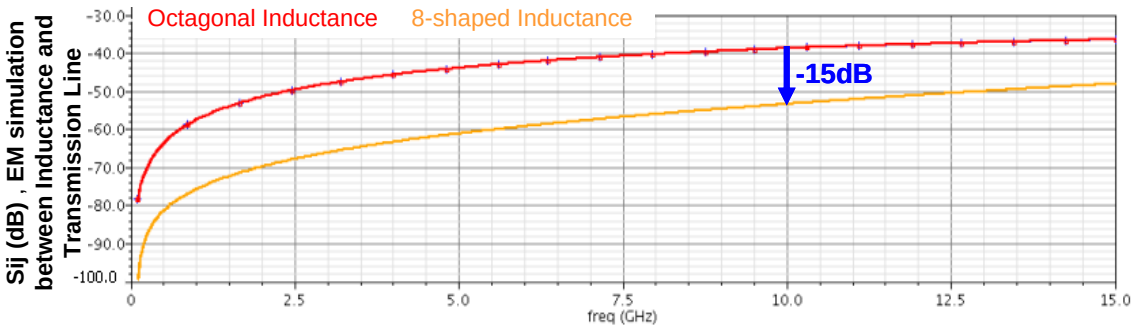
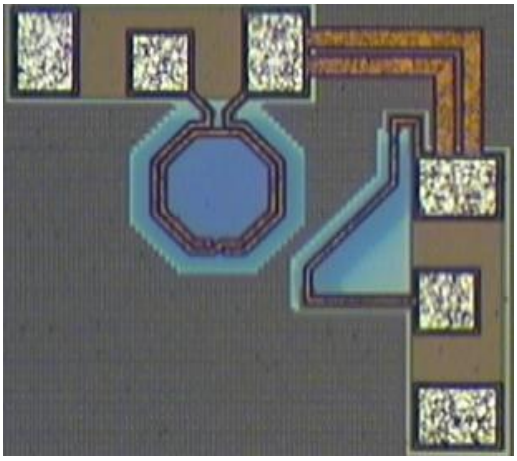
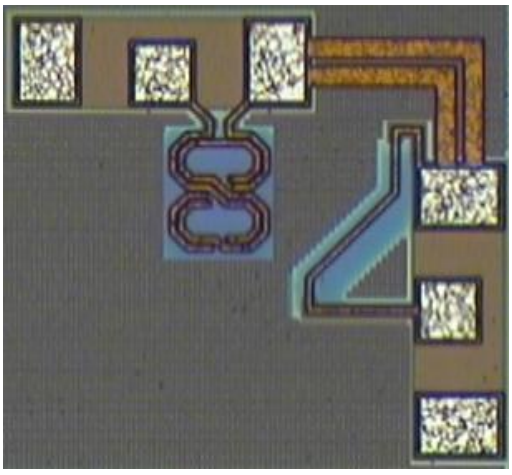


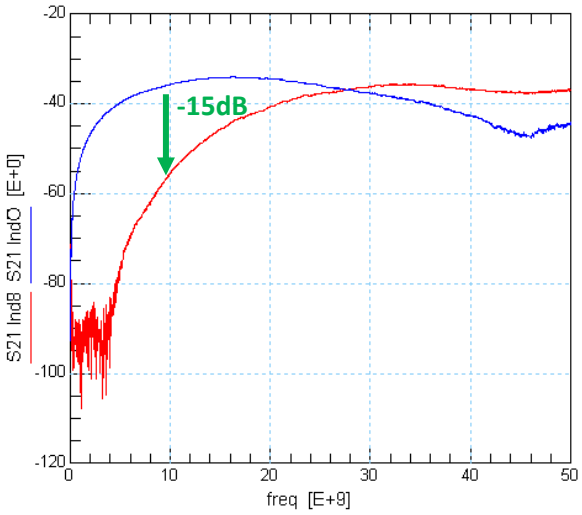
Figure II.4-13: EM Simulation results obtained with the MoM of an octagonal or 8-shaped inductance and the interconnection lines



(a)



(b)



(c)

Figure II.4-14: Measurements fixtures (a), (b) and results -Sij in dB (c) of the octagonal (blue curve) or 8-shaped inductance (red curve) coupled to the interconnection lines in the TFF1014

II.5. Pulling Analysis in Wireless Chip-to-Chip Interferences and Couplings

Wireless inter-chip and intra-chip electromagnetic interferences and couplings represent severe limiting factors for integrated system performances. Significant research efforts have been deployed in modeling and characterization of interferences and couplings [159]- [162]. However most of published investigations and contributions in the domain, deals with sub-block-level or block-level circuits where analysis involve simple structures (capacitive and/or inductive couplings). Modeling and experimental characterization of system-level electromagnetic interferences and couplings, for real-world chip-to-chip communication systems remains extremely challenging. Among main challenges for system-level chip-to-chip electromagnetic interferences and couplings are development of innovative analysis methodologies together with experimental characterization techniques.

A system-level inter-Chip interferences/couplings analysis and characterization is proposed in [163]. Three entities are distinguished: the Emitter (or aggressor), the Receiver (or victim) and the coupling-path. A real-world wireless car access transceiver chip (the LoPSTer) and a satellite down-converter chip (the TFF1014) are used as carrier applications for investigating inter and intra-Chip interferences and couplings. For the interference and coupling analysis complete PLL circuits (highlighted in Figure.I.4-1 and Figure I.4-4 in chapter I) is identified as critical sensitive block for the role of aggressor and victim as well. Coupling-path for intra-Chip analysis refers to substrate noise, conductive and radiated interference mechanisms, while for inter-chip analysis the coupling-path will be the free-space medium together with the board-application fixture system.

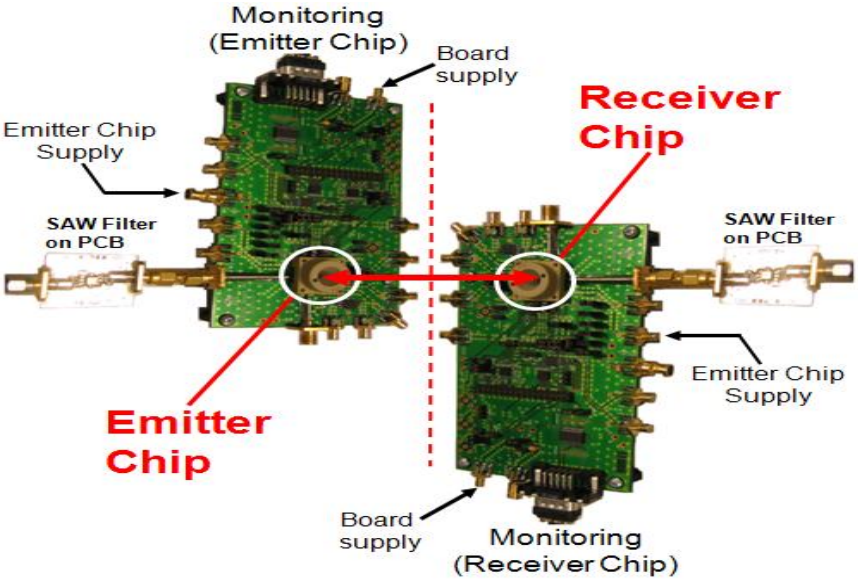


Figure II.5-1: Chip-to-Chip wireless interference measurement setup

Essential figure of merit for the proposed modeling and characterization analysis will be based on PLL frequency pulling and pushing both for inter-chip and intra-chip investigations. For inter-Chip analysis, noise interferences as function of wireless coupling-path attributes (wireless separation distance between emitter and receiver chips, injected power levels, Charge-Pump-Current) are investigated. For intra-Chip analysis, influence of VCO-PLL inductance architecture (8-shaped topology versus O-shaped topology) on noise interferences is evaluated through comparisons between library-models, full-wave EM analysis and measurement characterization. Intentional interruptions based on FIBs (Focused

Ion Beam) by cutting off identified critical power/ground paths show the importance of electromagnetic coupling. Impact of intra-Chip and inter-Chip couplings on frequency pulling of integrated PLL circuits is experimentally evaluated.

II.5.1.Inter-Chip Interferences, Couplings Characterization and Analysis

The analysis of inter-Chip couplings and interferences is carried out based on the following effects in reference to the wireless chip-to-chip communication setup in Figure II.5-1, using :

- Influence of the distance between the Chip aggressor (transmitter) and the Chip victim (receiver) frequency pulling for different power level.
- Impact of Chip aggressor (transmitter) power-level on Chip victim (receiver) frequency pulling for different chip-to-chip distance.
- Impact of Chip aggressor (transmitter) PLL Charge-Pump-Current (ICP) level on Chip victim (receiver) frequency pulling.

Two identical LoPSTer transceivers in transmit mode reported (soldered) on their test PCB are placed face-to-face so that the VCO inductances are lined up. So the surface of the chip for aggressor and the surface of the chip for victim are opposed. The chip aggressor working frequency f is fixed to f_0=868MHz and the working frequency of the receiver (victim) chip is set at a frequency slightly different from f_0.

The characterization results of the inter-chip coupling analysis are based on the measurement of power spectrum for evaluation of pulling and pushing effects both at transmitter and receiver sides. Because of mechanical constraints in link with the PCB fixture for the alignment of the transmitter and receiver chips minimum separation distance between the chips is set to 0.8cm. Figure II.5-2 shows measured output power spectrum variation of the chip victim as function of the distance between the chips (measurement results for two separation distance, namely 0.8cm and 2 cm are reported). Higher spurs levels are observed for lower separation distance with noise excess exceeding 10dBm differential power when separation distance is reduced from 2cm to 0.8cm.

Inter-Chips interaction can also lead to frequencies pulling as underlined in [164] and [165] that are due to intra-Chip couplings interactions. As discussed in [165], the more the amplitude of the injected signal in the VCO/PLL of the victim, the higher the spurs amplitude around the fundamental tone. In Figure II.5-2, the power level of the aggressor chip is varied from 10dBm to 12dBm.

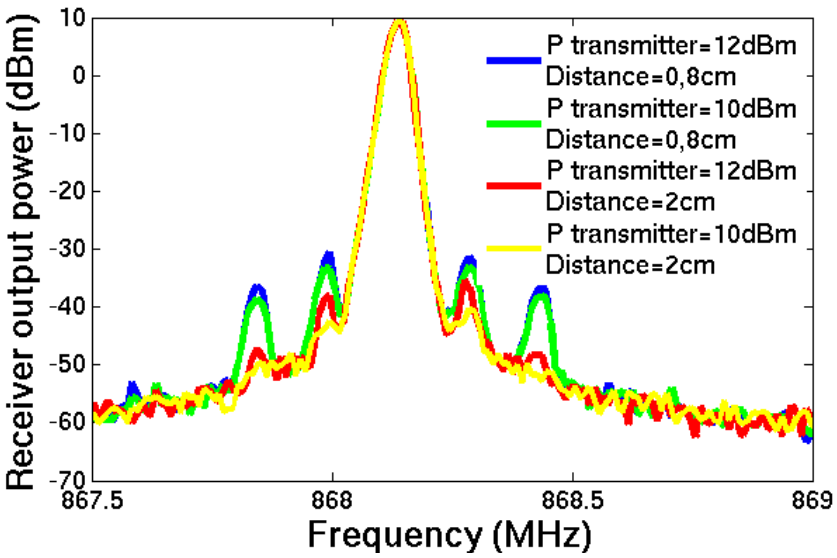


Figure II.5-2: Measured output power spectrum variation of the chip victim functions of output power-level of the chip aggressor (P transmitter) and the distance between the chips.

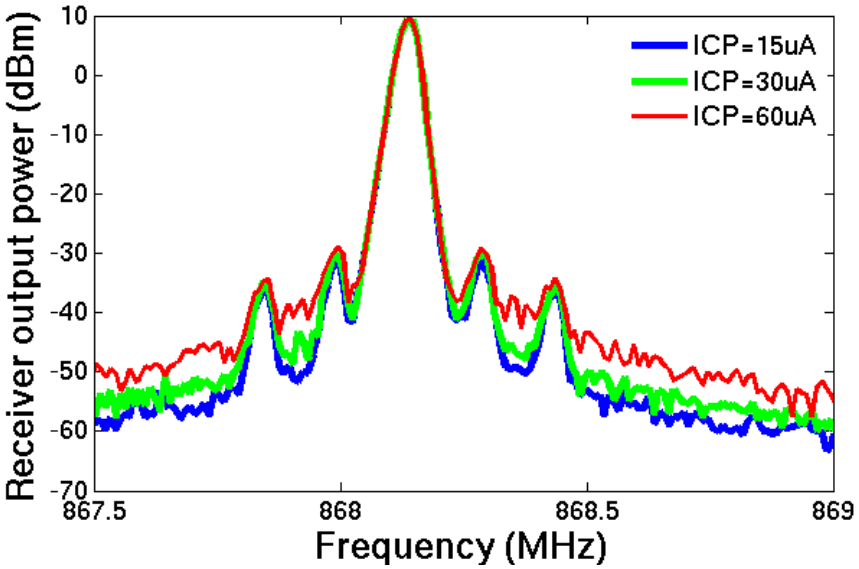


Figure II.5-3: Measured output power spectrum variation of the chip victim functions of its charge pump current (ICP) value.

In Figure II.5-3 we can see that the charge pump current value of the Chip victim PLL affects the noise level around the fundamental tone to transmit; if the level of the injected signal is low enough, the frequency pulling effects can be hidden by the noise level around the fundamental tone. However in this figure it is shown that the charge pump current value does not affect the spurs amplitude level and frequency that are due to inter-chip interference/coupling that we obtained in intra-chip analysis (see Figure II.3-1 (b) and Figure II.3-13).

II.6. Synthesis & Conclusion

In this chapter, we detailed the characterization of frequency pulling effects in PLLs through a transmitter application.

For that, we have based the analysis on a Chip-Package-PCB carrier application based on the BiCMOS LoPSTer IC, in transmit mode, reported on its PCB test. The system level analysis of the pulling effect turns out necessary because the manifestation of pulling in terms of spectral purity and the phase noise of the transmitted signal are due to different blocks and systems that make up the carrier application:

- At a function block level, we saw that variation of the PLL function blocks characteristics affects the pulling behavior, in particular the charge pump peak current, the noises on the VCO control voltage and the VCO gain variations. We will see in the next chapter if these variations are a cause or a consequence of the frequency pulling issue.
- At system level, we have also seen that depending on the SAW filter characteristics, especially its transfer function variations with the frequency, the pulling issue appears. We have also seen that redesign of the initial version of the IC in terms of ground and power distribution of the PA and the neighboring blocks of the VCO attenuates the effects of pulling issues, and VCO gain variation and non-linearities. In addition, by adding periodical noise on the supply of some function blocks as the PA and the VCO, pulling/pushing mechanisms are also observed on the output signal of the system.
- The power amplifier, whose transistors stages are integrated in the chip and whose matching network is reported on the PCB, also plays a role in the pulling behaviour through the power level of the output signal that depends on the IC (number of transistors composing the switch stage of the class-E PA, the Vcc of the PA) and the PCB (matching network) configuration. It is within this framework that the chip-package-PCB interaction level should be meticulously analyzed, in particular the parasitic capacitance effects which have a non-negligible importance on the class-E PA output signal.

We then interested ourselves on the coupling mechanisms which induce the pulling phenomenon. For that, we can consider two or more function blocks inductively coupled through metallizations. Using the FDTD and the method of moments for full-wave EM simulations of the simplified scheme to analyze, the coupling level between the function blocks analyzed are obtained in terms of dB through the simulated S-parameters obtained.

Analysis and characterization of inter-chip and intra-chip couplings and interferences has been investigated based on real-world automotive and satellite down-converter chips. At intra-Chip level quantitative assessment of electromagnetic couplings is conducted by operating FIBs on identified critical chip areas. A power-based figure-of-merit has been introduced for qualifying impact of operated FIBs on design performances (pulling and pushing effects).In particular interrupting some of the critical power/ground nets resulted in improvement of system-level noise performances. Replacement of octagonal inductors by 8-shaped inductor has demonstrated isolation improvement of -18.5dB at 10GHz. At inter-Chip level, impact of wireless coupling-path attributes such as chip-to-chip distance, and emitter chip power-level and Charge-Pump-Current on PLL pulling has been experimentally evaluated. Future investigations concern chip-to-chip high data-rate communication for multi-GHz bandwidth applications.

Bibliography of Chapter II

[119] “LoPSTer, Low-Power Single-Chip Transceiver Data Sheet”, Product Specification for V1A (rev 1.24), Apr. 2008, NXP Semiconductors.

[120] “LoPSTer, Low-Power Single-Chip Transceiver IC Design Specification”, Objective Design Specification (rev0.01), NXP Semiconductors.

[121] http://ics.nxp.com/packaging/hvqfn/

[122] “ AN10366, HVQFN application information“,Application note, Jan. 2006, , NXP Semiconductors.

[123] O. Aymard, “LoPSTer application board using HVQFN32 exposed diepad”, nov. 2006, NXP Semiconductors.

[124] “Characterization Report, PQF7980 LoPSTer Version V1x”, NXP Semiconductors, May 2008.

[125] “B3762-SAW Low-loss Filter 868,30 MHz – EPCOS Datasheet”, EPCOS AG, Munich, Germany.

[126] “UM10204, I2C-bus specification and user manual”, User manual, NXP Semiconductors, June 2007.

[127] D. Hauspie E-C Park, and J. Craninckx., “Wideband VCO with simultaneous switching of frequency band, active core, and varactor size,” IEEE Journal of Solid-State Circuits (JSSC), vol. 42, no. 7, pp. 1472-1480, July 2007.

[128] G. Cusmai M. Repossi, G. Albasini, A. Mazzanti, and F. Svelto., “A magnetically tuned quadrature oscillator,” IEEE Journal of Solid-State Circuits (JSSC), vol. 42, no. 12, pp. 2870-2877, Dec. 2007.

[129] B. Razavi, “Design of Millimeter-Wave CMOS Radios: A Tutorial”, IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 56, no. 1, pp. 4-16, January 2009.

[130] K. Kwok and J. R. Long, “A 23-to-29 GHz Transconductor-Tuned VCO MMIC in 0.13 µm CMOS”, IEEE J. Solid-State Circuits, vol. 42, no. 12, pp. 2878-2886, Dec. 2007.

[131] P. Andreani, “A 1.8-GHz monolithic CMOS VCO tuned by an inductive varactor”, in Proc. IEEE International Symposium on Circuits and Systems (ISCAS), 2001, pp. 714-717.

[132] D. Pi, B.-K. Chun, and P. Heydari, “A 2.5-3.2GHz CMOS differentially-controlled continuously-tuned varactor-less LC-VCO”, in Proc. IEEE Asian Solid-State Circuits Conference (A-SSCC), 2007, pp.111-114.

[133] Ying Chen, Koen Mouthaan,and Marcel Geurts, “A Varactorless VCO with 15% Continuous Frequency Tuning Range and 0.2 dB Output Power Variation”, Proceedings of the 5th European Microwave Integrated Circuits Conference, Paris 2010.

[134] N. O. Sokal and A. D. Sokal, "Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers", IEEE Journal of Solid-State Circuits, vol. SC-10, pp. 168–176, June 1975.

[135] F. H. Raab, "Idealized operation of the Class E tuned power amplifier," IEEE Trans. Circuits and Systems, vol. CAS-24, no. 12, pp. 725-735, Dec. 1977.

[136] “LoPSTer VCO pulling with SAW filter at TX Output”, LoPSTer team, ICRF-Caen, NXP Semiconductors, Nov. 2007.

[137] “MAX3232CUE data sheet “, Maxim Integrated Products, Inc., Sunnyvale, California.

[138] D. Banerjee, “PLL Performance”, Simulation and Design, 4th Edition, 2006

[139] M. Villegas , C. Berland , D. Courivaud , G. Lissorgues , O. Picon , C. Ripoll, « Radiocommunications numériques 2, Conception de circuits intégrés RF et micro-ondes », 1ère édition, Dunod 2002.

[140] Yee, K. S., “Numerical solution of initial boundary value problems involving Maxwells equa-tions in isotropic media," IEEE Transactions on Antennas and Propagation, Vol. 14, No. 3, 302-307, 1966.

[141] S. Mengué, E. Richalot , O. Picon , "Comparison between different criteria for evaluating a reverberation chamber functioning using a 3D-FDTD algorithm" for publication in the Transactions on Electromagnetic Compatibility", IEEE Transactions on Electromagnetic Compatibility , Vol 50, issue: 2, mai 2008.

[142] Berenger, J. P., \A perfectly matched layer for the absorption of electromagnetic-waves," J. Comp. Phys., Vol. 114, Vol. 2, 185-200, 1994.

[143] R. F. Harrington, "Time-Harmonic electromagnetic fields". McGraw-Hill, 1961.

[144] J. J. H. Wang, "Generalized Moment Methods in Electromagnetics: Formulation and Computer Solution of Integral Equations", Wiley-Interscience , 1991.

[145] S. Mostarshedi , E. Richalot , J-M. Laheurte , M.F. Wong, J. Wiart, O. Picon , "Fast and Accurate Calculation of Scattered EM Fields from Building Faces Using Green's Functions of Semi-Infinite Medium", IET Microwaves, Antennas and Propagation, Vol. 4, Iss. 1, Jan. 2010, pp. 72-82.

[146] James C. Rautio, "A Conformal Mesh for Efficient Planar Electromagnetic Analysis," IEEE Trans. on Microwave Theory and Tech., vol. 52, pp. 257-264, Jan. 2004.

[147] D. I. Sanderson, J. C. Rautio, R. A. Groves, and S. Raman, " Accurate Modeling of Monolithic Inductors Using Conformal Meshing for Reduced Computation ," Microwave Magazine Vol. 4, No. 4 December 2003, pp. 87 – 96.

[148] I.J. Bahl, "High-performance inductors", IEEE Trans Microwave Theory Tech, vol. 49, no. 4, pp. 654–664, Apr 2001.

[149] http://edocs.soco.agilent.com/display/genesys2009/Thick+Conductor+Modeling

[150] http://www.sonnetsoftware.com/products/sonnet-suites/ef_thick.html

[151] J.C. Rautio and V. Demir, "Microstrip conductor loss models for electromagnetic analysis," IEEE Trans. Microwave Theory Tech., vol. 51, pp. 915–921, Mar. 2003.

[152] http://www.sonnetsoftware.com/products/sonnet-suites/ef_co_calibrated_ports.html

[153] http://edocs.soco.agilent.com/display/ads2009/Ports+in+Momentum

[154] J. C. Rautio, " Perfectly Calibrated Internal Ports in EM Analysis of Planar Circuits ," 2008 IEEE MTT-S International Microwave Symposium Digest June 15-20, 2008, pp. 1373-1376.

[155] James C. Rautio, " Deembedding the Effect of a Local Ground Plane in Electromagnetic Analysis ," IEEE Transactions on Microwave Theory and Techniques Vol. 53, No. 2, February 2005, pp. 770 – 776

[156] O. Tesson, "High Quality Monolithic 8-Shaped Inductors for Silicon RF IC Design, " IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2008. SiRF, Orlando, 23-25 Jan. 2008 pp 94-97.

[157] B. Fahs, P. Gamand, and C. Berland, "Low-phase-noise LC-VCO using high-Q 8-shaped inductor", Electron. Lett., 21 January 2010, vol 46, no 2, p.140–141.

[158] H. Kampe, "Contribution au développement de règles de conception pour l'estimation de couplages inductifs dans les circuit integers RF", PhD Thesis, Université de Caen Basse Normandie, Caen, France, May 2009.

[159] M. Sun, Y. P. Zhang, G. X. Zheng, and W.-Y. Yin, "Performance of intra-chip wireless interconnect using on-chip antennas and UWB radios," IEEE Trans. Antennas Propag., vol. 57, no. 9, pp. 2756–2762, Sept. 2009.

[160] K. Kimoto and T. Kikkawa, "Transmission characteristics of Gaussian monocycle pulses for inter-chip wireless interconnections using integrated antennas," Jpn. J. Appl. Phys., vol. 44, no. 4B, pp. 2761–2765,April 2005.

[161] P.K. Saha, N. Sasaki and T. Kikkawa, "A CMOS monocycle pulse generation circuit in a ultra-wideband transmitter for intra/inter chip wireless interconnection," Jpn. J. Appl. Phys., vol. 44, no. 4B, pp. 2104–2108, April, 2005.

[162] H. Yordanov and P. Russer, "Integrated on-chip antennas for chip-to-chip communication," in Proceedings of the IEEE Antennas and Propagation Society International Symposium, 2008, San Diego, CA, 2008.

[163] M. Ranaivoniarivo, S. Wane, "Effects of Inter-Chip and Intra-Chip Electromagnetic Interferences on PLL Frequency Pulling and Spurs," EuMW 2011, Manchester, Oct. 2011.

[164] M. Ranaivoniarivo, S. Wane, P. Philippe, O. Aymard and P. Gamand, “System Level Analysis and Experimental Characterization of Frequency Pulling in PLLs,” SoftCOM 2010 , Split, Sept. 2010.

[165] B. Razavi, “A study of injection locking and pulling in oscillators,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1415–1424, Sept. 2004.

[166] P. Russer, M.Mongiardo, L.B. Felsen, Electromagnetic field representations and computations in complex structures III: network representations of the connection and subdomain circuits. Int. J. Numer. Model. Electron. Networks Devices Fields 15, 127–145 (2002).

[167] L.B. Felsen, M. Mongiardo, P. Russer, Electromagnetic field representations and computations in complex structures I: complexity architecture and generalized network formulation. Int. J. Numer. Model. Electron. Networks Devices Fields 15, 93–107 (2002)

[168] N. Fichtner, S. Wane, D. Bajon, P. Russer, Interfacing the TLM and the TWF method using a diakoptics approach in 2008 IEEE MTT-S Int. Microwave Symposium Digest. Atlanta, USA, June 2008, pp. 57–60.

[169] H. Baudrand et S. Wane “Circuits Multiéchelles. Utilisation des sources auxiliaires”, published in HERMES in 2006.

CHAPTER III:
SYSTEM LEVEL BEHAVIORAL MODELING FOR A PREDICTIVE ANALYSIS OF PULLING EFFECTS IN PLLS

III.0. Introduction

Analog mixed-signal designs bring real challenges as how to properly integrate digital and analog parts in one single chip. Behavioral modeling approaches represent alternative solutions for tackling the problem of analog-digital co-simulation in order to evaluate system-level performances. Based on the use of behavioral models in conjunction with IP-circuit models, verification and predictive analysis of the integrated system functionality and performances can be achieved to reduce design iterations. Combination of behavioral models with analog IP-circuitry requires development of design methodologies to properly account for layout induced parasites evaluated by electromagnetic analysis and simulations.

In published investigations, the elaboration of behavioral models of analog circuits is a very dynamic research topic where according to applications and associated specifications, Simulink/Matlab or analog HDL/Verilog-AMS are used to describe analog blocks using closed-form mathematic formulas that can be incorporated into electrical representation of systems.

The noise spurs level at the output of Phase-Locked-Loops (PLLs) represents essential specification constraints which directly affect global system performances. Accurate evaluation of such noise spurs in PLLs constitutes a real challenge for available simulation tools, sign-off verifications being principally carried out experimentally. The results of the experimental characterization of an integrated circuit (IC) are often analyzed using trial-and-error method to find the performance limiting factors and generally lead to partial modifications of identified blocks (e.g., potential noise sources) through FIBs (Focused Ion Beam). In order to limit re-design iterations during system evaluation and debugging phases, innovative methodologies are required for predictive numerical analysis, to achieve first-run right design. As exposed in Chapter 2, noise spurs in PLL may come from a variety of sources (VCO noise injection mechanisms, clock reference noise, etc…), but can also be due to electromagnetic couplings occurring within the PLL loop or neighbouring function block(coupled oscillators, amplifiers, etc…) or induced by the PCB assembly (external Surface Mounted Devices(SMD), SAW filter, parasitic capacitors/resistors…).

From a system-level standpoint, engaging a full transient simulation of a complete PLL circuit, with the required convergence of the loop frequency, can be extremely demanding in terms of CPU execution time. Many efforts have been devoted to the derivation of behavioral (macro) modeling approaches with the aim of reducing the complexity while maintaining an accuracy comparable to the one obtained with native circuit simulations. Over the last years, potentialities of behavioral models have been underlined for the analysis of various function blocks as discussed in [170],[172]. Although behavioral models based simulation approaches help in accelerating the analysis speed of PLL performances, they present some limitations, among them the difficulties to simulate PLL systems accounting for dynamic behavior (non-linearity and time-variant effects) [172]. In addition behavioral modeling approaches being classically applied at function block-level, their extension to predictive simulation at system level by including packaging and PCB effects requires proper partitioning methodologies.

This chapter presents detailed system-level characterization, modeling and analysis of pulling and pushing in PLLs where influences of the package as well as the assembly on the PCB are accounted for. The proposed modeling methodology combines SPICE-based circuit simulation with segregated behavioral models (see Table III.0-1). The behavioral modeling approach incorporates non-linear effects taking place within the PLL (e.g., non linear dependency of VCO oscillation frequency against tuning voltage and the nonlinear attributes of varicap devices). This segregated approach permits the versatility of the appropriate level of abstraction selection for the different blocks (transistor-level circuit description, and/or

system block description). The flexibility of the model description permits an adaptation of the chosen model to the parameters whose influence has to be studied. Importance of electromagnetic couplings through power supply noise and ground connections is underlined by FIB cutting operations on sensitive design portions.

The organization of this chapter is built around the following sections:

- The basis and assumptions of behavioral modelling for PLL systems
- The necessity of extracting an RLCk model from EM analysis
- The Derivation of analytical and semi-analytical approaches for spurs description through AM-PM modulations
- A description of behavioral building block models for PLL Applications
- The use of Matlab/Simulink, Verilog-AMS for Closed-Loop PLL behavioral modeling for frequency pulling analysis and prediction
- And finally the importance of circuit parasitic elements and backannotation into circuit simulators.

Table III.0-1: Investigated modeling approaches: summary of purpose & perceived limitations

Modeling Approaches	Purpose & Investigations	Perceived Limitations
SPICE/Spectre Simulations	Transistor-level circuit simulation	Difficulties with full-PLL analysis
Verilog-AMS Behavioral Modeling (in Cadence Analog Design Environment)	Closed-form analytical transfer function coding (requires tricks for complex value functions)	Requires knowledge of transfer-functions on identified nodes where voltages and currents are calculated
Simulink Macro-Modeling/Behavioral Modeling (in standalone mode)	Computational macro-modeling where customized numerical solutions can be embedded within transfer functions description	Requires challenging methodologies for treating non-linearity on a wide-band
Measurement Characterization (Mainly using Spectrum Analyzer)	Essentially frequency domain based. Both power spectrum of pulling and pushing in PLLs are measured	Difficulties to extract full-wave time-domain waveforms. Requires existing designs.

III.1. Basis and Assumptions of Behavioral Modeling for PLL Systems

III.1.1. Assumptions & Simplifications

For illustrating the behavioral modelling for frequency pulling in PLLs, the LoPSTer application will be the carrier system of the behavioral modelling.

We will consider that the multi-scale system is composed by:

- the transceiver IC in transmit path including the PLL(VCO, PFD/CP, Loop Filter, %N)and the PA, whereas effects of the buffers, %2, transmission lines are neglected
- at PCB level the SMDs matching/decoupling components are taking into account so does the SAW filtering solution
- the 50Ω load will be the spectrum analyzer (Rhode & Schwarz FSP7).

The signal to be transmitted is supposed to be a pure sinus around 868MHz.

As the measurement results of PLL pulling are analyzed in the frequency domain, the spectral purity of the output signal (transmitted to the load) will be the figure of merit of our behavioral model results.

III.1.2. Methodology of description for Predictive Simulation of PLL Pulling

a. To Model Active Sensitive Blocks

The first part of the approach is based on the experimental characterization of frequency pulling effects of the carrier application in order to define a model building before the analysis.

For the LoPSTer case, the global measurement analysis permitted to determine the main effects of the pulling phenomenon at function bloc, system level and chip-package-PCB.

The model building is based on:

- Measurement results (input/output signals of the block)
- SPICE/Spectre Simulation if the active block has a limited complexity
- Macro-modeling with Verilog-AMS in Spectre/Virtuoso analysis or with Matlab/Simulink models.

b. To account for EM Couplings

Full-wave EM simulation or measurement are the best ways for accurate estimation of couplings between identified sensitive blocks.

For EM simulations, depending on the use of the results and the shape of the involved metallization, Time-Domain or Frequency domains, 2.5D or 3D EM simulators should be used.

A methodology to extract the R,L,C,k model from EM Analysis is also used.

c. To tackle Co-Simulation Analysis:

Once the passive RLC model and the active model at transistor level are obtained, the combination can be simulated with Cadence/Spectre for non-complex system.

The coupling of the different simulation approaches is also possible with the actual tools: Simulink + Cadence/Spectre, Cadence/Spectre + Momentum, Sonnet + Momentum…

d. The Predictive Simulation Approach

Before any simulation, it is necessary to determine an approach to define the aspect of the signal under frequency pulling to be transmitted. Through the aspect of the pulling spectrum, we derived first an analytical and semi-analytical approaches for defining the spurs description of the pulling effects in terms of AM and PM Modulations.

For predicting frequency pulling effects in PLLs through a behavioral model, coupling effects between the different blocks must be introduced. The Time Domain model derived is based on a hybrid mathematical and SPICE/Spectre view function block parameters. Based on macromodels of the PLL function blocks, the coupling effects are introduced in the model through the VCO gain variations. For obtaining the signal spectrum, a FFT is performed on the VCO output signal.

III.2. Extraction of RLCk Model from EM Analysis of VCO Pulling in Integrated PLL Systems

III.2.1. Quasi-Static Based Extractions:

In Cadence design environment a quasi-static extraction tool such as ASSURA is used by digital and analog designers for parasitics extraction. The tool claims full-chip, resistance (R), capacitance (C), self (L) and mutual (k) inductance parameter extractions. The quasi-static analysis performed by ASSURA is based on an approximate segmentation technique to compute the couplings (mainly local) between specified interaction regions. The limits of the segmentation domains are bounded by power and ground lines. The extracted mutual coupling terms are related to each segmentation region. The return path of the current is generally assumed beyond the power-ground nets involving real challenges to account for local ground references.

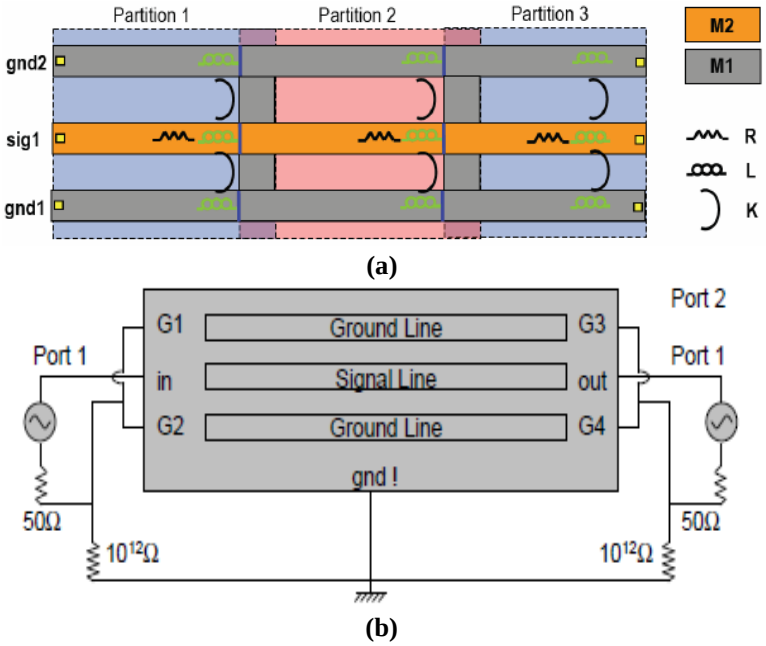


Figure III.2-1: Illustrative multi-line conductors model extraction using Assura (a), back-annotated into Spectre/SPICE circuit simulators (b)

Figure III.2-1 illustrates a multi-conductor test-bench with ASSURA model back-annotated into Cadence Spectre/SPICE circuit simulator with attached excitation ports (port-1 and port-2).

III.2.2. Full-Wave Based Extractions

S-parameters description of a device obtained by full-EM simulation is not easy to use for transient analysis (DC information missing, time domain stability is not guaranteed with black-box back-annotation). Generally components in design kit libraries are described by lumped element behavior models obtained from measurement and characterization for particular shapes and geometries. Such models are only valid at low frequencies and are strongly process and technology dependant. When for design specific constraints, components are used in non-conventional situation (custom parameterized cells) then accurate models are needed to include their electrical definition in the circuit to analyze. An accurate way to derive models for passive components is to perform EM simulations or measurements and to convert the results into RLCG Spice/Spectre equivalent circuit models.

III.2.3. Derivation of Broadband Equivalent Circuits for Passive Circuits

a. The Approach

Once the scattering parameters (S-parameters) of a passive N-ports component are determined, the Admittance (Y) or Impedance (Z) parameters can be deduced and an equivalent circuit representing the electric behaviour of the complex circuit to analyze is derived.

$$[Z] = Zref \times ([1] + [S]) \cdot ([1] - [S])^{-1} \qquad [\text{III.2-1}]$$

with [S] the S-parameters matrix, [1] the identity matrix and Zref the reference impedance of the system.

$$[Y] = \frac{1}{Zref} \times ([1] - [S]) \cdot ([1] + [S])^{-1}$$
$$[Y] = [Z]^{-1} \qquad [\text{III.2-2}]$$

Depending on the topology of the device analyzed, wide-band equivalent circuit based on RLCG network can be derived from Z or Y-parameters. For a two port network, Pi or T equivalent circuit indicated in Figure III.2-2(a) & (b) can be obtained. Extension to multi-port applications can also be done as indicated in sec. 3-2 of [170] for microwaves passive networks.

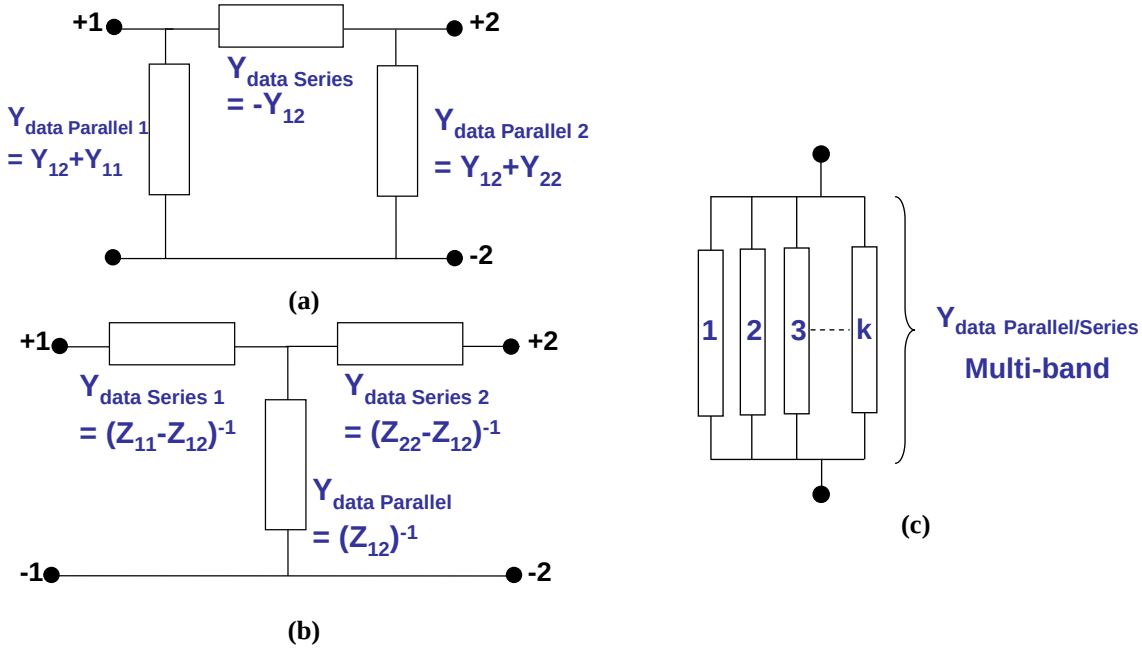


Figure III.2-2: Y_{data} of Pi equivalent scheme (a), Y_{data} of T equivalent scheme (b)

Each branch of the Pi or T equivalent scheme is represented by an admittance, noted in the following Y_{data}. The series and parallel branches will be splitted into k sub-branches where each sub-branch is composed of RLCG elements as shown in Figure III.2-3 and describes the application behaviour in several frequency bands.

From [175]-[181], a methodology is derived in [174] to extract, from EM simulation results and measurement data, equivalent circuits for passive circuits. The proposed methodology that we will lean on uses rational function approach following pole-residue expansion of Y-parameters. The problem is expressed in terms of linear equations and the

matrix form obtained is solved by QR decomposition technique. The originality of the methodology concerns the possibility to link the derived equivalent circuit models to circuit layout topologies in order to allow tuning and physical interpretations.

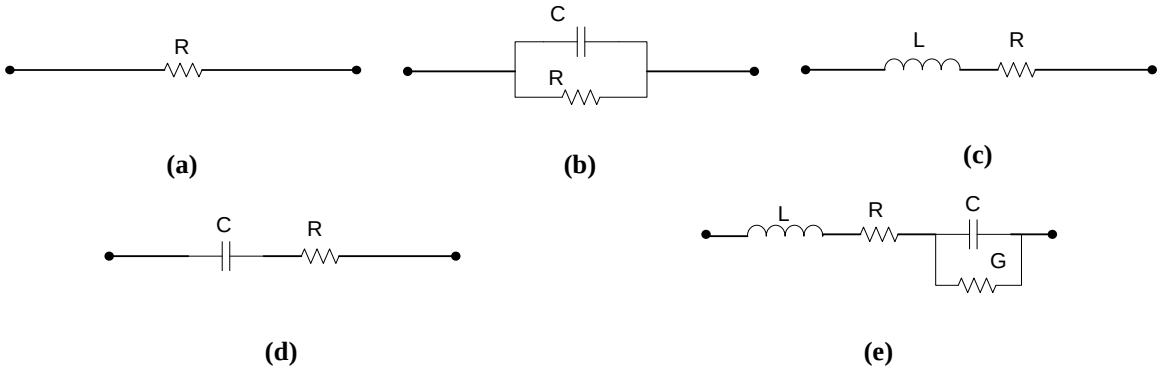


Figure III.2-3: RLCG sub-branches that can be obtained from pole-residue derivation of homogeneous to Y-parameters data

b. Formulation

The first step to approximate the transfer function of the tabulated data is to factorize each admittance $Y_{data}(s)$ in a rational function of two polynomials of order N (order of the numerator)and M (order of the denominator). e.g: $Y_{data}(s)=-Y_{12}(s)$, $(Y_{11}+-Y_{12})(s)$ or $(Y_{22}(s)+Y_{12})(s)$ can be re-written in frequency domain as [III.2-3] for the series branch of a 2-port PI network.

$$Y_{data}(s) = \frac{a_0 + a_1 s + a_2 s^2 + ... + a_{N-1} s^{N-1} + a_N s^N}{b_0 + b_1 s + b^2 s^2 + ... + b^{M-1} s^{M-1} + b^M s^M} \qquad \text{[III.2-3]}$$

Where s = jω is the complex frequency in s-plan; Y_{data} should then be defined for several frequencies. The variables to determine area$_0$, $a_1,\ldots, a_N, b_0, b_1,\ldots,b_M$.

Then each term $Y_{data}(s)$ of the equivalent circuit is expressed using a matrix linear equation AX=b where:

- X is the vector of unknown coefficients [a0, a1,…, aN,b0, b1,…,bM] assumed real for physical reasons; b0=1 for normalization aspects
- A is a rectangular matrix containing the complex frequency at different powers from 0 to N: At = (1 s s2 … sN).
- and b is given by the input data (Y parameters against frequency)

To simplify the expansion of the rational function derivation of Y_{data}, the following formulation will be developed with N=M; the numerator and the denominator of the rational function will be of the same order.

To obtain the matrix equation, both sides of [III.2-3] are multiplied by the polynomial denominator, with s=j2πf we obtain:

$$Y_{data}(s) \cdot \left(1 + \sum_{k=1}^{N} b_k \cdot s^k\right) = \sum_{k=0}^{N} a_k \cdot s^k \qquad \text{[III.2-4]}$$

The principal equation to solve becomes:

$$Y_{data}(s) = \sum_{k=0}^{N} a_k \cdot s^k - \sum_{k=1}^{N} b_k \cdot s^k \times \left(\Re e\left(Y_{data}(s)\right) + j \cdot \Im m\left(Y_{data}(s)\right)\right) \qquad \text{[III.2-5]}$$

The coefficients a_k and b_k are reel therefore, the result of the equation should be treated by separating real and imaginary part.

Finally, for F frequencies or pulsations, $\omega=2\pi f$, the final system to solve is:

$$\left[\begin{array}{c|c|c|c} \left[\omega_1{}^{2k}\times(-1)^k\right]_{k=\{[0;n]\}} & [0] & \left[-\Im m(Y_{data}(s))\times\omega_1{}^{2k-1}\times(-1)^k\right]_{k=\{[0;n]\}} & \left[-\Re e(Y_{data}(s))\times\omega_1{}^{2k}\times(-1)^k\right]_{k=\{[0;n]\}} \\ \vdots & & \left[-\Im m(Y_{data}(s))\times\omega_F{}^{2k-1}\times(-1)^k\right]_{k=\{[0;n]\}} & \left[-\Re e(Y_{data}(s))\times\omega_F{}^{2k}\times(-1)^k\right]_{k=\{[0;n]\}} \\ \left[\omega_F{}^{2k}\times(-1)^k\right]_{k=\{[0;n]\}} & \left[-\omega_1{}^{2k-1}\times(-1)^k\right]_{k=\{[1;n]\}} & \left[\Re e(Y_{data}(s))\times\omega_1{}^{2k-1}\times(-1)^k\right]_{k=\{[1;n]\}} & \left[-\Im m(Y_{data}(s))\times\omega_1{}^{2k}\times(-1)^k\right]_{k=\{[1;n]\}} \\ [0] & \vdots & & \\ & \left[-\omega_F{}^{2k-1}\times(-1)^k\right]_{k=\{[1;n]\}} & \left[\Re e(Y_{data}(s))\times\omega_F{}^{2k-1}\times(-1)^k\right]_{k=\{[1;n]\}} & \left[-\Im m(Y_{data}(s))\times\omega_F{}^{2k}\times(-1)^k\right]_{k=\{[1;n]\}} \end{array}\right]$$

$$\cdot\begin{pmatrix}(a_{even})\\(a_{odd})\\(b_{odd})\\(b_{even}{}^*)\end{pmatrix}=\begin{pmatrix}\Re e(Y_{data}(s_1))\\\vdots\\\Re e(Y_{data}(s_F))\\\Im m(Y_{data}(s_1))\\\\\Im m(Y_{data}(s_F))\end{pmatrix} \qquad \text{[III.2-6]}$$

where n is the integer part of N/2.

As the matrix A is rectangular and not square, it cannot be directly inverted, and a particular resolution algorithm should be used to solve the problem. QR decomposition algorithm is used to determine the unknowns.

Steps for the resolution are:

- QR-Decomposition of the matrix A using Matlab numerical toolbox
  $[Q]\cdot[R]\cdot(X)=(b)$
  with [Q] an orthogonal matrix and [R] an upper triangular matrix.
- Multiplication of each equation side with [Q]T
  $[Q]^T\cdot[Q]\cdot[R]\cdot(x)=[Q]^T\cdot(b)$
  with $[Q]^T\cdot[Q]=[I_F]$, $[I_F]$ being the Identity matrix of size $F\times F$ (with F the number of frequencies)
- fixing (Y')= [Q]T · (b), we obtain a triangular equation system :
  $[R]\cdot(X)=(Y')$
  which can be solved easily and with accuracy by Gaussian elimination, the factors of the rational function equivalent to $Y_{data}(X)=[a_0, a_1,\ldots, a_N, b_0, b_1,\ldots, b_M]$ are then found.

The obtained rational function expression of Y_{data} is then decomposed on partial fractions, always with the aid of Matlab tool:

$$Y_{data}(s) = k_\infty + \underbrace{\sum_{i=1}^{R}\frac{r_i}{s-p_i}}_{\text{real poles and residues}} + \underbrace{\sum_{i=1}^{C}\left(\frac{R_i}{s-P_i}+\frac{R^*_i}{s-P^*_i}\right)}_{\text{complex poles and residues}} \qquad \text{[III.2-7]}$$

where R is the number of real poles and C the number of complex conjugate pairs.

From the previous formula, we can determine an equivalent circuit of Y_{data}, each term of the sum corresponding to a sub-branch of the circuit. These sub-branches are connected in parallel as seen in Figure III.2-2 (c).

It has to be noticed that the real part of the different poles obtained should be negative so that the equivalent circuit is stable in an electrical point of view.

c. Link of Pole-Residue Expansion with Electrical Circuit Synthesis

We will now link the previous pole-residue expansion with an electrical circuit.

- For the direct term k∞

This term is a constant if N=M, that is if the numerator and the denominator of the rational function (III.2-3) are at the same order. k_∞ is equivalent to a resistance of value 1/ k_∞ Ω as in Figure III.2-3 (a)

If N=M+1, k_∞ is of the form $k_0 \times s + k_1$. It is equivalent to a capacitance of value k_0 in parallel with a resistance of value 1/ k_1 Ω as in Figure III.2-3 (b).

- For each term i of the real poles pi and residues ri,

$$\frac{r_i}{s-p_i} = \frac{1}{s\cdot\frac{1}{r_i} - \frac{p_i}{r_i}} \qquad \text{[III.2-8]}$$

with r_i real. The stability criteria implies $p_i<0$.

– if ri>0, the expression leads to R,L series admittance as in Figure III.2-3 (c) , and we can easily determine by identification the values of the resistance and the inductance:

$$R = -p_i / r_i(\Omega) \text{ and } L = 1/r_i(H) \qquad \text{[III.2-9]}$$

– however if ri<0, when adding a constant k0' to the term with the real negative pole and negative residue:

$$k_0' - \frac{1}{s\left(\frac{-1}{r_i}\right) + \frac{p_i}{r_i}} \qquad \text{[III.2-10]}$$

This last equation can be comparable to an admittance transfer function of an RC series:

$$Y_{RCseries} = \frac{1}{R + \frac{1}{s\cdot C}} = \frac{1}{R} - X, (with X = \frac{1}{R} - \frac{1}{R + \frac{1}{sC}}) \qquad \text{[III.2-11]}$$

$$Y_{RCSeries} = \frac{1}{R} - \frac{1}{s\cdot C\cdot R^2 + R}$$

Then this case with $r_i<0$ and $p_i<0$ leads to RC series admittance as in Figure III.2-3 (d) of value $R=p_i/r_i$ (Ω) and $C=-r_i/p_i^{\,2}$ (F) and the first resistance branch of value 1/ k_∞ becomes $1/(k_\infty-k_0')$ with $k_0'=r_i/p_i$.

- For each pair of complex conjugate poles Pi and Pi*, we obtain:

$$\frac{R_i}{s-P_i} + \frac{R^*_i}{s-P^*_i} = \frac{s\cdot(2\Re e(R_i)) - 2\cdot\Re e(R_i)\cdot\Re e(P_i) - 2\cdot\Im m(R_i)\cdot\Im m(P_i)}{s^2 - 2s\cdot\Re e(P_i) + (\Re e(P_i))^2 + (Im(P_i))^2} \qquad \text{[III.2-12]}$$

This sum is comparable to an RLCG circuit like in Figure III.2-3 (e) which admittance is:

$$Y_{RLCG} = \frac{\frac{s}{L} + \frac{G}{L\cdot C}}{(s)^2 + s\cdot\left(\frac{R}{L} + \frac{G}{C}\right) + \left(\frac{R\cdot G}{L\cdot C}\right)} \qquad \text{[III.2-13]}$$

with:

$$
\begin{aligned}
R &= \frac{-\Re e(R_i)\cdot\Re e(P_i)+\Im m(R_i)\cdot\Im m(P_i)}{2\left(\Re e(R_i)\right)^2} \\
L &= \frac{1}{2\Re e(R_i)} \\
C &= \frac{2\left(\Re e(R_i)\right)^3}{\left(\Im m(P_i)\right)^2\cdot\left(\left(\Re e(R_i)\right)^2+\left(\Im m(R_i)\right)^2\right)} \\
G &= \frac{2\left(\Re e(R_i)\right)^2\cdot\left(\Re e(R_i)\cdot\Re e(P_i)+\Im m(R_i)\cdot\Im m(P_i)\right)}{-\left(\Im m(P_i)\right)^2\cdot\left(\left(\Re e(R_i)\right)^2+\left(\Im m(R_i)\right)^2\right)}
\end{aligned}
\qquad \text{[III.2-14]}
$$

By determining all of the $Y_{\text{data Paralel/Series}}$ equivalent branches circuit using the defined methodology, a global equivalent circuit of a passive device can be derived in a wide frequency band but the stability and the passivity of the determined model should also be studied [174].

d. Application to VCO inductance

As LC oscillators permit to work at high frequencies, have wide output voltage swing and good noise performance [182], this solution will be mostly used in transceivers. However the tank inductor could then become a critical component as potentially subjected to inductive coupling. LC VCO requires then a particularly attention to the inductor design for the accurate estimation of the centre frequency, the tuning range (the tank inductance value), the phase noise (affected by the quality factor of the inductive components) and the ability to lower parasitic couplings (through the shape and the orientation of the inductor). Then, the inductance value and its quality factor should be determined with accuracy. Extraction of R,L,C,k model of the inductor integrable into spectre/spice simulation is then necessary for VCO/PLL simulations.

For the TFF1014 VCO inductance, a 1-port analysis from the measurements results was performed for frequencies from 100MHz to 39.6GHz. The input data of the analysis was 1/Z11 and the equivalent RLC circuit obtained is given in the figure below:

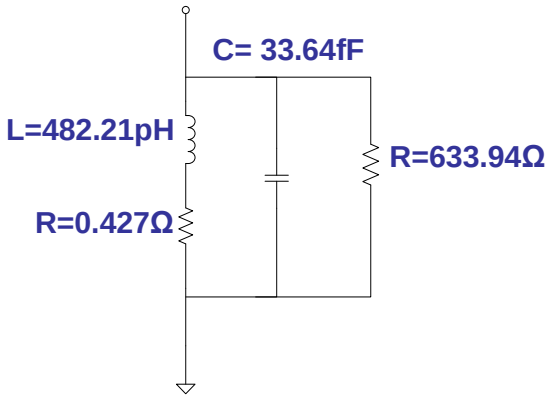


Figure III.2-4: 1-port equivalent circuit of the TFF1014 VCO's inductor

If we define the inductance L and the Q-factor Q value as equations [III.2-15] and [III.2-16], we can see in Figure III.2-5 that the inductance value varies with the frequency. The parallel implementation of Rs in series with Ls and the capacitor C permits this variation

in frequency. The parallel resistance permits to adjust the Q-factor then the losses of the inductance, in particular at the inductor resonance.

$$L = \frac{\Im m(Z11)}{\omega} \qquad \text{[III.2-15]}$$

$$Q = \frac{\Im m(Z11)}{\Re e(Z11)} \qquad \text{[III.2-16]}$$

The analysis results in Figure III.2-5 show that inside the studied frequency bandwidth of analysis [100MHz-39.6GHz], the equivalent RLC circuit derived has quite the same performances as the measurements data of the inductor. Outside the frequency bandwidth of analysis, the inductance variation obtained can still be used, but the very high frequency Q-factor behaviour is difficult to achieve.

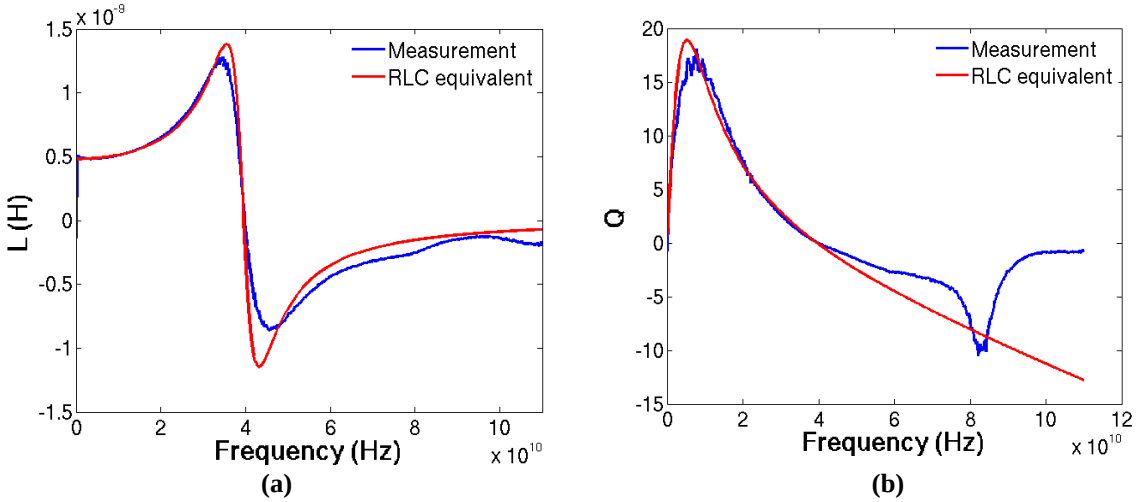


Figure III.2-5: Inductance value (a) and Q-factor (b) of the 1-port TFF1014VCO's inductor

III.2.4. Expression of the Coupling coefficients

a. The approach

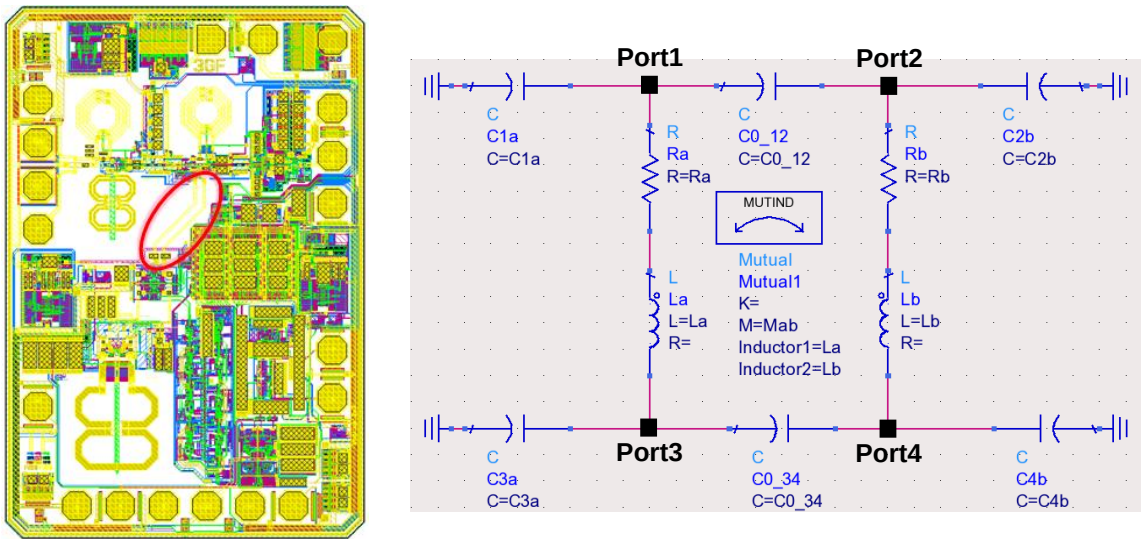
We have seen how the defined methodology permitted to derive a wide band equivalent scheme of a passive device with R, L, C and G components from measured or simulated S-parameters, but there is also a necessity to relate S-parameters representation and coupling elements for linking system level requirement (in dB) with design parameters (at block level).

To obtain the coupling information in terms of parameters integrable into spice-like simulation, equivalent circuit derivation of the system is necessary.

For that, first the equivalent circuit type is determined (Pi or T for 2-port network) including the inductive and capacitive coupling effects occurring with respectively a mutual inductance coefficient M and a coupling capacitive coefficient C0. From the parameters (S, Y, Z) describing the equivalent scheme, the components of the equivalent circuit are determined.

b. Application to Coupled Metallizations

Let's take the example of two coupled lines:



(a) **(b)**

Figure III.2-6: Example of of coupled lines in a circuit (a) and its simple equivalent scheme (b)

Post treatment with the analysis of the S-parameters obtained permit to derive a simple equivalent scheme of the coupled lines. For that:

- To obtain the self inductance and the series resistance of the lines (La, Lb and Ra,Rb), the capacitive effects between the line and the substrate, as well as the substrate effects (C1a, C3a and C2b, C4b):
  - a 4-ports analysis can directly lead to Ra and La from Y13, Rb and Lb from Y42.
  - a 2-port analysis of each line alone can be done by using the method detailed above applied to a Pi equivalent network.
  - or also a 2-port analysis of ports 1 & 3 (ports 2 and 4 connected to ground) and a 2-port analysis of ports 2 & 4 (ports 1 and 3 connected to ground) leading to a Pi equivalent network circuit from the 2-ports Y-parameters obtained.
- The mutual inductance Mab representing the magnetic coupling between the lines in the 4-ports configuration of Figure III.2-6(b) can be obtained through the analysis of the 2-ports network of Figure III.2-7. In this configuration, port 1 is taken at the input of the first line, port 4 at the output of the second one, whereas ports 3 and 2 are connected to the ground. Z12 of this 2-port network leads to the mutual inductance between the lines:

$$M = -\frac{\Im m(Z12)}{\omega} \qquad \text{[III.2-17]}$$

and the coupling coefficient k is expressed as followed:

$$k = \frac{|M|}{\sqrt{La \cdot Lb}} \qquad \text{[III.2-18]}$$

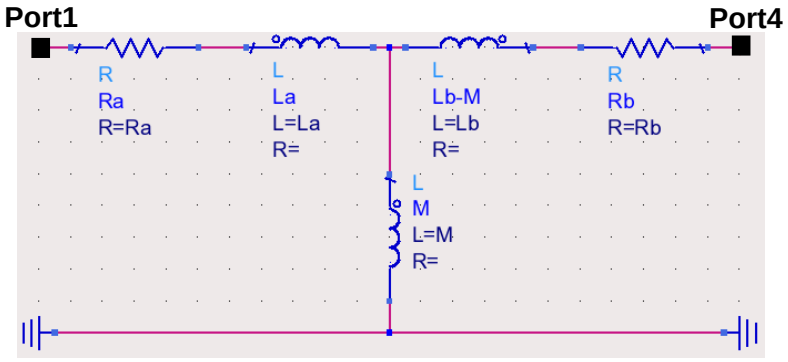


Figure III.2-7: Determination of the magnetic coupling through M

Moreover, the same analysis between the ports 1 and 2 (at the input of both lines) can also be done, the result obtained doesn't vary much.

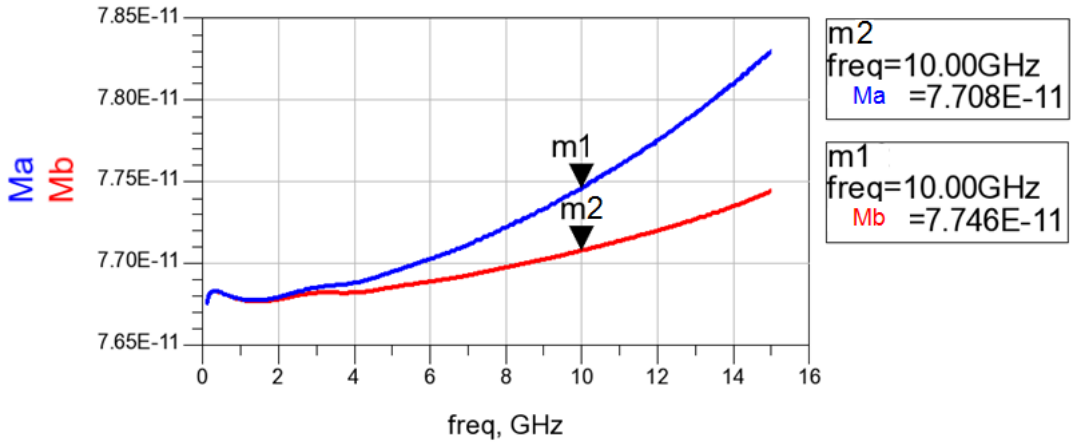


Figure III.2-8: Comparison of the mutual inductance between the two lines with an analysis between the ports 1 and 4 (Ma) and the ports 1 and 2 (Mb)

- To obtain the distributed coupling capacitance representing the electric coupling between the two lines, the capacitors C0_12 and C0_34 in Figure III.2-6(b) will be combined to finally obtain the figure below with a single capacitance between the input and the output of the coupled lines.

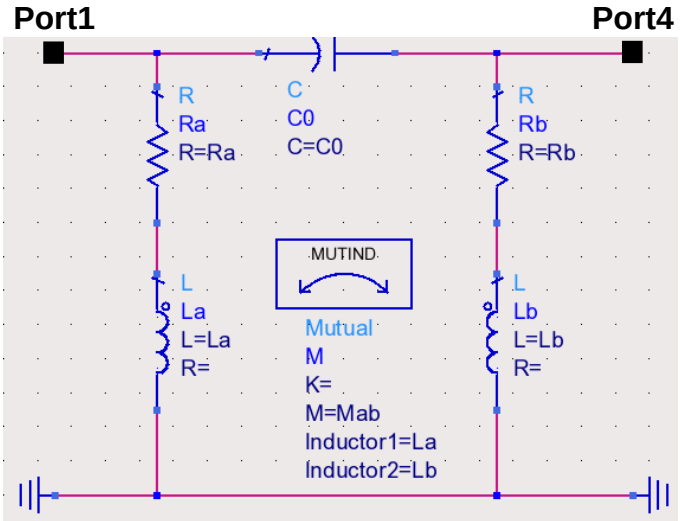


Figure III.2-9: Determination of the coupling by electrical field through C0

In order to validate the capacitive coupling coefficient between the interconnection lines of the TFF1014 VCO's buffer, a test structure was fabricated in order to evaluate the coupling capacitor by measuring it as an interdigitated capacitor [183], [184], as seen in Figure III.2-10.

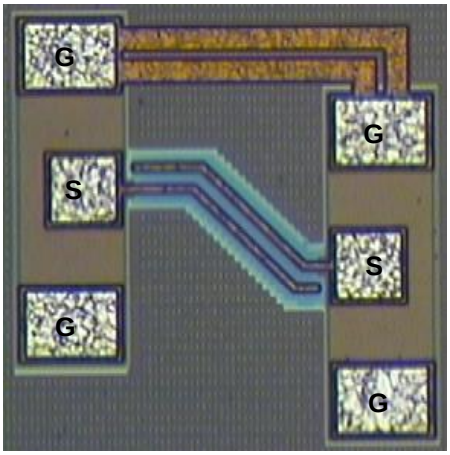


Figure III.2-10: Test structure to define the capacitive coupling between the interconnection lines

Measurements were performed with an Agilent E8364B PNA Network Analyzer from 20MHz to 50GHz, Impedance Standard Substrates ISS 101-190 GSG are used for calibration and Open / Short de-embedding structures are used.

If we define coupling capacitor C0 as:

$$C0 = \frac{\Im m(-Y12)}{\omega} \qquad \text{[III.2-19]}$$

At 10 GHz C0 has the following different values:

- From Sonnet simulations of the interconnection lines only (without the GSG access pads): C0=4.68fF
- From Sonnet simulations of the whole test structure with open-short de-embedding of the GSG access pads: C0=5.11fF. (The two open-short de-embedding methodologies used are presented in Appendix B.2.b)
- From the measurement results C0=4.25fF

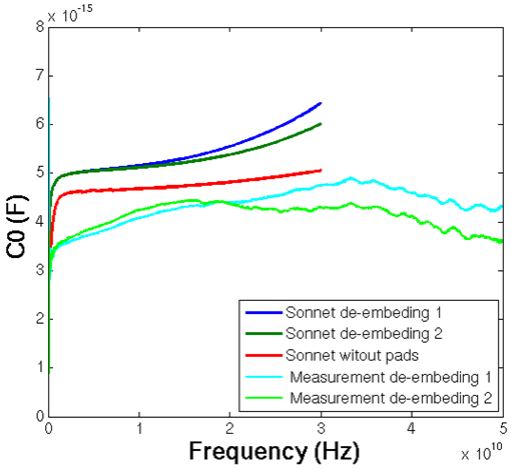


Figure III.2-11: Capacitive coupling coefficient between the coupled interconnection lines

From the QUBIC4X Design Rule Manual, the interlayer lateral capacitance between the equivalent metal6 straight lines of the two the interconnect lines gives a capacitance of value: $C = \frac{C_L \times L}{S}$ = 1,897fF, with: C_L the intralayer capacitance between 2 lateral metal6 metallization = 135.5aF/µm, L the total lines of the lines =210µm and S the gap between the lines =15 µm. This C value extracted manually is different from the C0 values obtained in simulation and measurement (although at the same order of magnitude) because this capacitance value is a result of a simple low frequencies model based on empirical formulas that strongly depend on the topology of the device analyzed.

III.3. Analytical and Semi-Analytical Approaches for Spurs Description through AM-PM Modulations

The frequency pulling effect can be considered as a modulation of the wanted single tone signal of angular frequency ω0. The total perturbed signal can be expressed as:

$$s(t) = a(t) \cdot \sin\left(\omega_0 t + \theta(t)\right) \quad \text{or} \quad s(t) = a(t) \cdot \cos\left(\omega_0 t + \theta(t)\right) \qquad \text{[III.3-1]}$$

were a(t) and θ(t) are the modulating signals. Here we will deal only with sinusoidal modulating signals called m(t)

III.3.1. Classes of spurs

The result of a coupling phenomenon between two signals can lead to the addition of intermodulation products to the frequency spectrum of the induced signal.

In this paragraph, we assume that the coupling between the wanted and the spurious signals leads to an analogue modulation between them. For that, we will present the different kinds of analogue modulations that the wanted single tone signal of amplitude A_0 can meet in the presence of interfering spurious signal. The wanted signal will be considered as the carrier signal p(t), and the interfering signal as the modulating signal m(t).

For a carrier signal $A_0 \cdot \sin(\omega_0 t)$, the waveforms of the analogue modulations chosen are:

Amplitude modulation (AM): $s_{AM}(t) = A_0 \cdot (1 + K \times m(t)) \cdot \sin(\omega_0 t)$ [III.3-2]

Phase modulation (PM): $s_{FM}(t) = A_0 \cdot \sin(\omega_0 t + K \times m(t))$ [III.3-3]

Frequency modulation (FM): $s_{PM}(t) = A_0 \cdot \sin\left(\omega_0 t + K \times \int_{-\infty}^{t} m(t)dt\right)$ [III.3-4]

In [III.3-2] $K=K_{AM}$ is the amplitude modulation index. In [III.3-3] $K=K_{PM}$ is the phase modulation index. If we consider m(t) as a sinusoidal signal of angular frequency ω_Δ and with unity amplitude ($m(t) = \cos(\omega_\Delta t)$), taken from equation [III.3-4]: $K \times \int_{-\infty}^{t} m(t)dt = \frac{K}{\omega_\Delta} \sin(\omega_0 t)$ the frequency modulation index $K_{FM} = \frac{K}{\omega_\Delta}$ can then be considered to be equal to the phase modulation index ($K=K_{PM}$) divided by ω_Δ.

The following tables show that the result of an analogue modulation of the wanted signal at ω_0 with an interfering signal at a low frequency of ω_Δ can affect the spectrum purity of the resulting signal if the amplitudes of the spurs are too important and if ω_Δ is small so that the spurs are too close to the wanted signal.

For angle modulations, the development of the spectral analysis was derived with the aid of the Bessel functions of 1st kind. The higher the value of the index modulation K (i.e. the smaller the frequency offset ω_Δ for FM modulation), the smaller the number of spurs with significant amplitude.

In terms of spurs amplitude level:

- AM spurs level depends on the modulation index and the amplitude of the wanted signal.
- FM and PM spurs level depends on the modulation index and the amplitude of the wanted signal but also on the frequency offset ω_Δ.

Table III.3-1: Classes of spurs according to analogue AM modulation

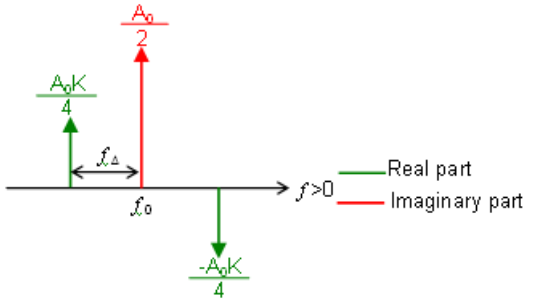
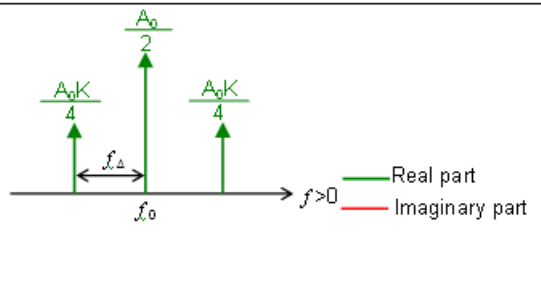
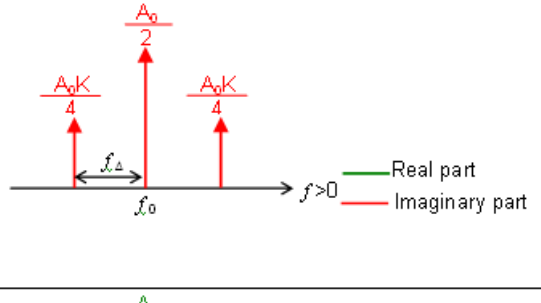
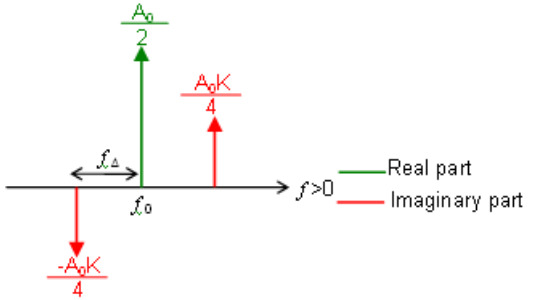
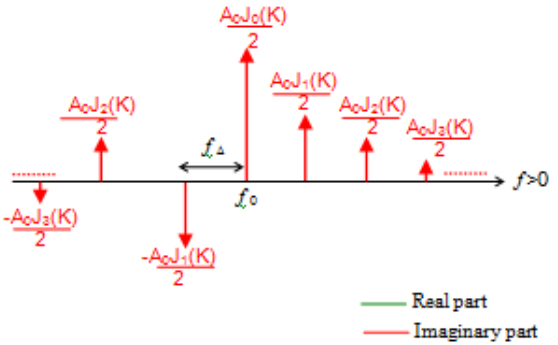
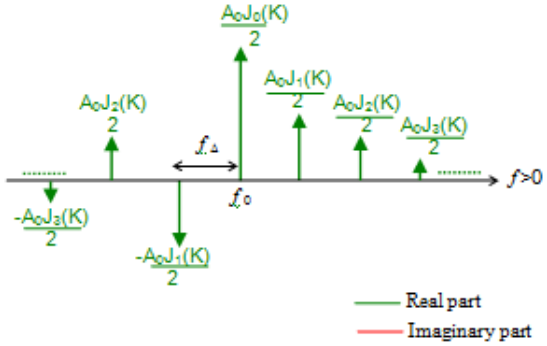
	Carrier and Modulating Signals, respectively p(t) and m(t)	Modultated signal in Time and Frequency domain, respectively s(t) and S(f)	Spectrum of an amplitude modulation
Amplitude modulation	The wanted signal : $p(t)=A_0 \cdot \sin(\omega_0 t)$ Interfering signal: $m(t)= \sin(\omega_\Delta t)$	$s(t) = A_0 \cdot sin(\omega_0 t) + \frac{A_0 K}{2} \cdot cos(\omega_0 t - \omega_\Delta t) - \frac{A_0 K}{2} \cdot cos(\omega_0 t + \omega_\Delta t)$ $S(f) = \frac{A_0}{2} j \cdot [\delta(\omega - \omega_0) - \delta(\omega + \omega_0)] + \frac{A_0 K}{4} \cdot [\delta(\omega - (\omega_0 - \omega_\Delta)) + \delta(\omega + (\omega_0 - \omega_\Delta))] - \frac{A_0 K}{4} \cdot [\delta(\omega - (\omega_0 + \omega_\Delta)) + \delta(\omega + (\omega_0 + \omega_\Delta))]$	
	The wanted signal : $p(t)=A_0 \cdot \cos(\omega_0 t)$ Interfering signal: $m(t)= \cos(\omega_\Delta t)$	$s(t) = A_0 \cdot cos(\omega_0 t) + \frac{A_0 K}{2} \cdot cos(\omega_0 t - \omega_\Delta t) + \frac{A_0 K}{2} \cdot cos(\omega_0 t + \omega_\Delta t)$ $S(f) = \frac{A_0}{2} \cdot [\delta(\omega - \omega_0) + \delta(\omega + \omega_0)] + \frac{A_0 K}{4} \cdot [\delta(\omega - (\omega_0 - \omega_\Delta)) + \delta(\omega + (\omega_0 - \omega_\Delta))] + \frac{A_0 K}{4} \cdot [\delta(\omega - (\omega_0 + \omega_\Delta)) + \delta(\omega + (\omega_0 + \omega_\Delta))]$	
	The wanted signal : $p(t)=A_0 \cdot \sin(\omega_0 t)$ Interfering signal: $m(t)= \cos(\omega_\Delta t)$	$s(t) = A_0 \cdot sin(\omega_0 t) + \frac{A_0 K}{2} \cdot sin(\omega_0 t - \omega_\Delta t) + \frac{A_0 K}{2} \cdot sin(\omega_0 t + \omega_\Delta t)$ $S(f) = \frac{A_0}{2} j \cdot [\delta(\omega - \omega_0) - \delta(\omega + \omega_0)] + \frac{A_0 K}{4} j \cdot [\delta(\omega - (\omega_0 - \omega_\Delta)) - \delta(\omega + (\omega_0 - \omega_\Delta))] + \frac{A_0 K}{4} j \cdot [\delta(\omega - (\omega_0 + \omega_\Delta)) - \delta(\omega + (\omega_0 + \omega_\Delta))]$	
	The wanted signal : $p(t)=A_0 \cdot \cos(\omega_0 t)$ Interfering signal: $m(t)= \sin(\omega_\Delta t)$	$s(t) = A_0 \cdot cos(\omega_0 t) - \frac{A_0 K}{2} \cdot sin(\omega_0 t - \omega_\Delta t) + \frac{A_0 K}{2} \cdot sin(\omega_0 t + \omega_\Delta t)$ $S(f) = \frac{A_0}{2} \cdot [\delta(\omega - \omega_0) + \delta(\omega + \omega_0)] - \frac{A_0 K}{4} j \cdot [\delta(\omega - (\omega_0 - \omega_\Delta)) - \delta(\omega + (\omega_0 - \omega_\Delta))] + \frac{A_0 K}{4} j \cdot [\delta(\omega - (\omega_0 + \omega_\Delta)) - \delta(\omega + (\omega_0 + \omega_\Delta))]$	

Table III.3-2: Classes of spurs according to analogue angular modulation

	Carrier and Modulating Signals, respectively p(t) and m(t)	Modulated signal in Time and Frequency domain, respectively s(t) and S(f)	Spectrum of an angle modulation
Phase or Frequency modulation	The wanted signal : $p(t)=A_0\cdot\sin(\omega_0 t)$ Interfering signal: $m(t)=\sin(\omega_\Delta t)$ PM $m(t)=-\cos(\omega_\Delta t)$ FM	$s(t)=A_0J_0(K)\cdot\sin(\omega_0 t)+A_0\sum_{N=1}^{\infty}J_{2N}(K)[\sin(\omega_0 t+2N\omega_\Delta t)+\sin(\omega_0 t-2N\omega_\Delta t)]+A_0\sum_{N=1}^{\infty}J_{2N-1}(K)[\sin(\omega_0 t+(2N-1)\omega_\Delta t)-\sin(\omega_0 t-(2N-1)\omega_\Delta t)]$ $S(f)=\frac{A_0J_0(K)}{2}j\cdot[\delta(\omega-\omega_0)-\delta(\omega+\omega_0)]+\sum_{N=1}^{\infty}\left[\frac{A_0J_{2N}(K)}{2}j\cdot[(\delta(\omega-(\omega_0+2N\omega_\Delta))-\delta(\omega+(\omega_0+2N\omega_\Delta)))+(\delta(\omega-(\omega_0-2N\omega_\Delta))-\delta(\omega+(\omega_0-2N\omega_\Delta)))]\right]+\sum_{N=1}^{\infty}\left[\frac{A_0J_{2N-1}(K)}{2}j\cdot[(\delta(\omega-(\omega_0+(2N-1)\omega_\Delta))-\delta(\omega+(\omega_0+(2N-1)\omega_\Delta)))-(\delta(\omega-(\omega_0-(2N-1)\omega_\Delta))-\delta(\omega+(\omega_0-(2N-1)\omega_\Delta)))\right]$	
	The wanted signal : $p(t)=A_0\cdot\cos(\omega_0 t)$ Interfering signal: $m(t)=\sin(\omega_\Delta t)$ PM $m(t)=-\cos(\omega_\Delta t)$ FM	$s(t)=A_0J_0(K)\cdot\cos(\omega_0 t)+A_0\sum_{N=1}^{\infty}J_{2N}(K)[\cos(\omega_0 t+2N\omega_\Delta t)+\cos(\omega_0 t-2N\omega_\Delta t)]+A_0\sum_{N=1}^{\infty}J_{2N-1}(K)[\cos(\omega_0 t+(2N-1)\omega_\Delta t)-\cos(\omega_0 t-(2N-1)\omega_\Delta t)]$ $S(f)=\frac{A_0J_0(K)}{2}\cdot[\delta(\omega-\omega_0)-\delta(\omega+\omega_0)]+\sum_{N=1}^{\infty}\left[\frac{A_0J_{2N}(K)}{2}\cdot[(\delta(\omega-(\omega_0+2N\omega_\Delta))+\delta(\omega+(\omega_0+2N\omega_\Delta)))+(\delta(\omega-(\omega_0-2N\omega_\Delta))+\delta(\omega+(\omega_0-2N\omega_\Delta)))]\right]+\sum_{N=1}^{\infty}\left[\frac{A_0J_{2N-1}(K)}{2}\cdot[(\delta(\omega-(\omega_0+(2N-1)\omega_\Delta))+\delta(\omega+(\omega_0+(2N-1)\omega_\Delta)))-(\delta(\omega-(\omega_0-(2N-1)\omega_\Delta))+\delta(\omega+(\omega_0-(2N-1)\omega_\Delta)))\right]$	

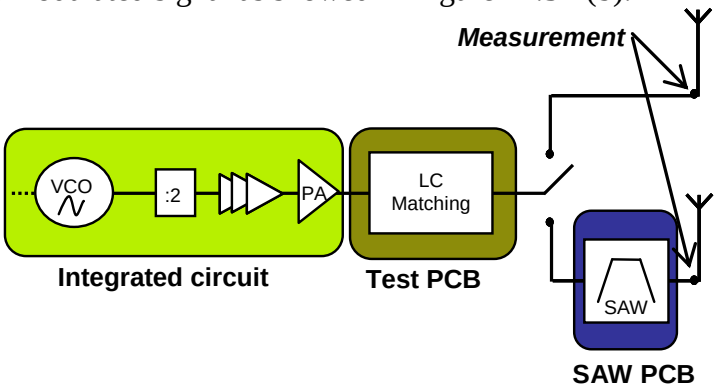
From the spectrum results of the modulation between two sinusoidal signals, the spectrum distribution of the pulling phenomenon can be assimilated to a modulation of the wanted signal with a low frequency spurious.

III.3.2. Modeling of Pulling Effects in Terms of Modulation

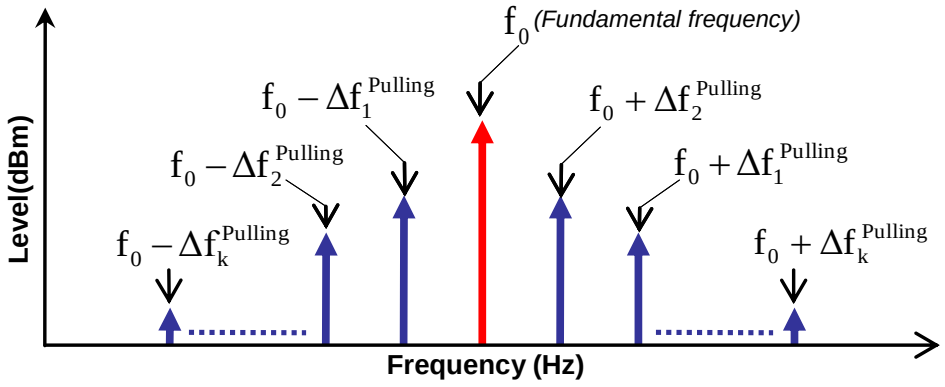
a. AM modulation

In Chapter II we presented an investigation on a pulling phenomenon in integrated oscillator observed during the measurement characterization of the LoPSTer. The proposed methodology was derived from experimental observations made on the LoPSTer circuit in a particular transmission configuration. In order to model the output signal distortions at a system level, amplitude modulations were used to describe the pulling effects [185].

First, the output signal of the whole system that includes the IC, the test PCB and SAW PCB obtained in measurements is represented in time domain by a sinusoidal multi-amplitude modulated signal as showed in Figure III.3-1(b).



(a)



(b)

Figure III.3-1: : Measured system (a) and illustration of a pulling effect around a fundamental wanted frequency (b)

The time domain expression is expressed as:

$$X_{Piulling}^{TD}(t) = A_0 \cdot \left(1 + \sum_k m_k \times \sin\left(2\pi \Delta f_k^{Pulling} t\right)\right) \cdot \sin\left(2\pi f_0 t\right) \qquad \text{[III.3-5]}$$

with A_0 the amplitude at the fundamental frequency f_0, m_k the index of the k^{th} modulation at the frequency $f_{0 \pm} f_k^{Pulling}$. The modulation parameters $\Delta f_k^{Pulling}$ and m_k are deduced from the measurements; the link between the amplitude level measured with the spectrum analyzer in dBm and the peak-to-peak amplitude of the signal voltage (V_{pk}) is governed by the following relation for a standard impedance R_0:

$$\begin{cases} \text{Level(dBm)} = 10\log\left(\dfrac{|V_{pk}|^2}{2\times R_0\times 1\text{mW}}\right) \\ |V_{pk}| = \sqrt{2\times R_0\times 1\text{mW}\times 10^{\frac{\text{Level(dBm)}}{10}}} \end{cases} \quad \text{[III.3-6]}$$

Then, the filtering effects due to the SAW filter are represented through its transfer function H(jω) expressed from the S-parameters obtained by measurement of the SAW PCB, the load impedance Z_L and the impedance characteristic Z_0 of the studied system.

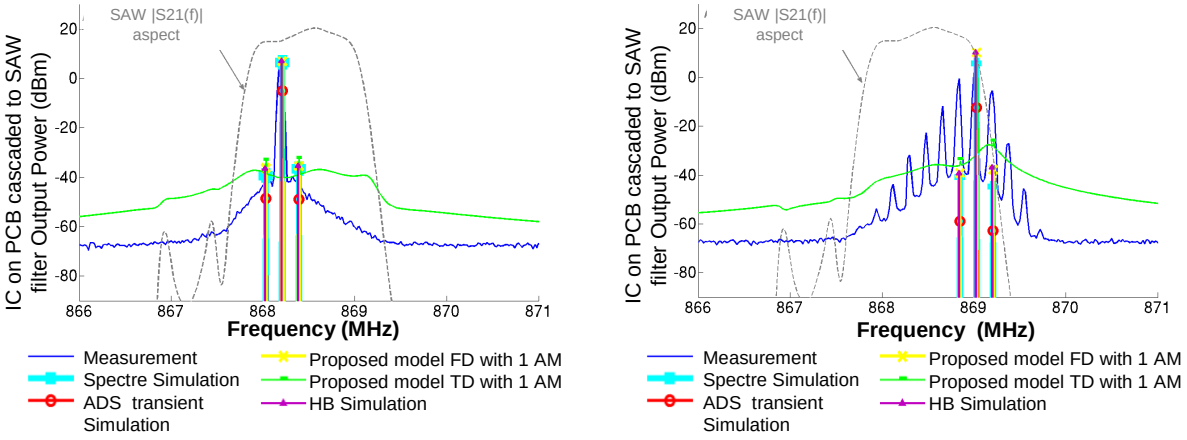
$$H(j\omega) = \frac{2\cdot Z_L\cdot S_{21}}{(Z_0 - Z_L)(S_{11}\cdot S_{22} + S_{22} - S_{12}\cdot S_{21}) + (Z_0 + Z_L)(S_{11} + 1)} \quad \text{[III.3-7]}$$

Thus, when knowing the input signal *X* of the filter, by a cascade approach, the signal transmitted to the antenna can be obtained with the following equation:

$$\begin{aligned} Y^{TD}(t) &= H^{TD}(t)\otimes X^{TD}(t) \\ Y^{FD}(j\omega) &= H^{FD}(j\omega)\times X^{FD}(j\omega) \end{aligned} \quad \text{[III.3-8]}$$

The acronyms ⊗ and × respectively represent the convolution product in time domain (TD) and the simple product in frequency domain (FD).

A first approach consists in using the measured signal at the antenna input in absence of the SAW filter as the input signal of the filter. The filter is represented by its transfer function. The cascade approach results in time and frequency domain are compared to measurements in the presence of the SAW filter between the test PCB and the antenna. The method proposed in order to express the global signal transmitted to the antenna is validated by transient and harmonic balance (HB) of ADS (Agilent) simulations and also by a transient approach using Spectre/Virtuoso (Cadence) simulations. The results obtained for a same sinusoidal signal with one AM modulation representing the output matched IC signal are presented in Figure III.3-2.



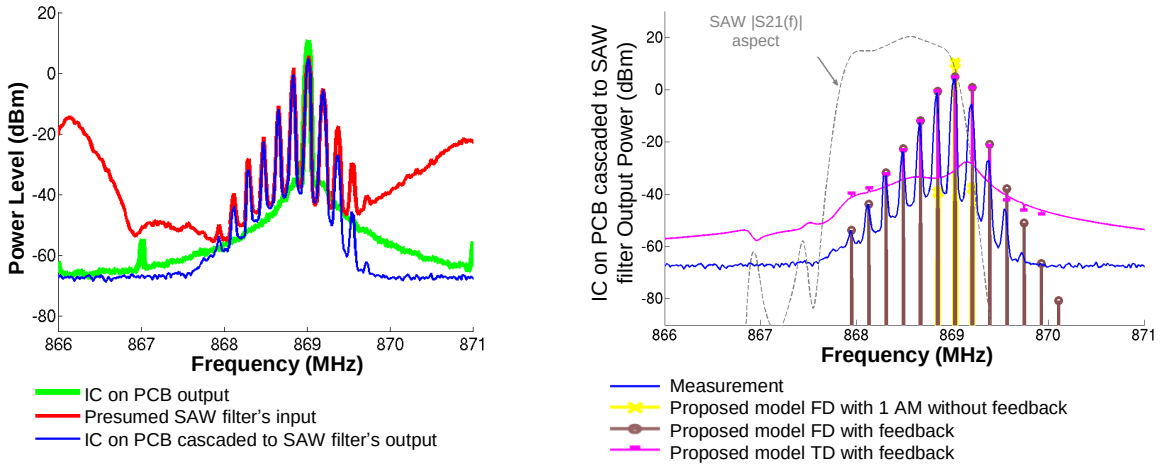
(a) **(b)**

Figure III.3-2: Established signals at the SAW filter's output, the source signal is expressed from the measurement done at the test PCB output without the SAW filter, for f_0=868.3MHz (a) and f_0=868.82MHz (b)

As we can see in Figure III.3-3(a), when the fundamental frequency of the signal source is inside the bandwidth of the SAW filter, a global satisfying agreement is obtained for the amplitudes of the fundamental frequency and the first harmonics; in time domain analysis, the observed differences outside the harmonic frequencies are due to numerical dynamic related to the noise floor level considered by the different tools (the noise floor reference for

the measurement is around -70dBm), the type of windowing function (here a rectangle windowing) and also the sampling of the finite signal in time domain to be converted in frequency domain using a FFT.

However the pulling effect observed after the SAW filter is not considered by the previous method as well as the modulation effects of the source signal as presented in equation [III.3-5], the interaction due to the insertion of the filter board has not been evaluated and inserted into the cascade approach. A feedback approach is then more appropriated: the only information from measurements that include the pulling effect at the filter input, i.e. the output signal of the whole system including the SAW while f_0 reaches the edges of the SAW filter bandwidth, is taken into account for the generation of the multi-harmonic components i.e. the amplitude and the frequency deviation from f_0 of the measured spurs. Using the measured spectrum of the signal to be transmitted to the antenna in the presence of the SAW filter and the transfer function of this latest, the real source signal at the SAW filter input can be extracted from equation [III.3-8]. This signal including the pulling effect is also modelled in equation [III.3-5] even if the asymmetry of the observed signal spectrum can arise from several conjugated effects; here the most important criteria was chosen to be the positioning/centring of the harmonics localisation in relation to f_0 and the bandwidth of the SAW filter. The result of this second method is given in the following figure.



(a) **(b)**

Figure III.3-3 : Determination of the input signal source (a) and Established signals at the SAW filter output for f_0=868.82MHz (b) by considering feedback effect

Figure III.3-2 and Figure III.3-3 demonstrate the capability of the proposed modeling to restore, in time and frequency domain, multi-harmonic distributions that can model a VCO pulling phenomenon in terms of amplitude modulation.

However, the asymmetry aspect of the pulling is not found with an AM modulation modeling. By using Table III.3-1 and

Table III.3-2, we can see that a combination of amplitude and angle modulation can lead to asymmetrical spectrum of a fundamental and spurious modulated signal.

b. Combination of AM and FM Modulation

By taking up the Table III.3-1 and Table III.3-2, the asymmetries of the spurs at $\pm\Delta f_k^{Pulling}$ as showed in the measurement results could be effectively explained by a combination of amplitude and angle modulation if the carrier and the modulating signals are sinusoidal. Let's illustrate this approach with k=1: a unique couple of spurs, each one on both sides of f_0 that constitute the instabilities.

For that, we consider that the bandwidth B of the angular modulation is about $\sim 2\times\Delta f^{Pulling}$; only the two first harmonics of the angle modulation spectrum are predominant in the calculation. The Carson's rule implies that the angular modulation index m should be less that 1 to satisfy the hypothesis.

$$\text{Carson}: \ B = 2(m+1)\times\Delta f^{\,Pulling} \qquad \text{[III.3-9]}$$

Still referring to Table III.3-1 and

Table III.3-2, the development of the different combination of possible amplitude and angular modulation (in terms of signs of the signal spectrum real and imaginary parts) implies that the carrier signal should be a sinus, the modulating signal a cosines, the angular modulation a frequency modulation.

We can obtain the generic following relation:

$$X^{TD}_{Piulling}(t) = A_0 \cdot \left(1 + ma \times \cos\left(\Delta\omega^{Pulling} t\right)\right) \times \sin\left(\omega_0 t\right) + A_0 \times \sin\left(\omega_0 t + ma \times \int \cos\left(\Delta\omega^{Pulling} t\right)\right) \qquad \text{[III.3-10]}$$

or

$$\begin{aligned} X^{TD}_{Piulling}(t) = {} & 2\times A_0 \times sin\left(\omega_0 t\right) + \frac{A_0}{2}\times\left(ma + \frac{mf}{\Delta\omega^{\,Pulling}}\right)\times sin\left(\omega_0 t + \Delta\omega^{\,Pulling} t\right) \\ & + \frac{A_0}{2}\times\left(ma - \frac{mf}{\Delta\omega^{\,Pulling}}\right)\times sin\left(\omega_0 t - \Delta\omega^{\,Pulling} t\right) \end{aligned} \qquad \text{[III.3-11]}$$

As the aspect of the measured instabilities shows that the amplitude in $f_0+\Delta f^{Pulling}$ is inferior to the one at $f_0-\Delta f^{Pulling}$, the amplitude index modulation m_a and the frequency index modulation m_f should be of opposite sign.

By applying this method to each couple of spurs, we can determine the global equation defining the pulling phenomenon:

$$X^{TD}_{Piulling}(t) = A_0 \cdot \left(1 + \sum_k ma_k \times \cos\left(\Delta\omega_k{}^{Pulling} t\right)\right) \times \sin\left(\omega_0 t\right) + A_0 \times \sin\left(\omega_0 t + mf_k \times \int \cos\left(\Delta\omega_k{}^{Pulling} t\right)\right) \qquad \text{[III.3-12]}$$

or

$$\begin{aligned} X^{TD}_{Piulling}(t) = {} & A_0 \cdot (k+1) \times \sin\left(\omega_0 t\right) + \sum_k \left[\frac{A_0}{2}\left(ma_k + \frac{mf_k}{\Delta\omega_k{}^{Pulling}}\right)\times \sin\left(\omega_0 t + \Delta\omega_k{}^{Pulling} t\right)\right] \\ & + \sum_k \left[\frac{A_0}{2}\left(ma_k - \frac{mf_k}{\Delta\omega_k{}^{Pulling}}\right)\times \sin\left(\omega_0 t - \Delta\omega_k{}^{Pulling} t\right)\right] \end{aligned} \qquad \text{[III.3-13]}$$

We obtain the following Fourier transform of the AM-FM multi modulation:

$$\begin{aligned} X^{FD}_{Piulling}(t) = {} & \frac{A_0 \cdot (k+1)}{2} j \cdot \left[\delta(\omega - \omega_0) - \delta(\omega + \omega_0)\right] \\ & + \sum_{N=1}^{\infty}\left[\frac{A_0}{4}\left(ma_k + \frac{mf_k}{\Delta\omega_k{}^{Pulling}}\right) j \cdot \left[\left(\delta\left(\omega - \left(\omega_0 + \Delta\omega_k{}^{Pulling}\right)\right) - \delta\left(\omega + \left(\omega_0 + \Delta\omega_k{}^{Pulling}\right)\right)\right)\right] \right. \\ & \left. + \sum_{N=1}^{\infty}\left[\frac{A_0}{2}\left(ma_k - \frac{mf_k}{\Delta\omega_k{}^{Pulling}}\right) j \cdot \left[\left(\delta\left(\omega - \left(\omega_0 - \Delta\omega_k{}^{Pulling}\right)\right) - \delta\left(\omega + \left(\omega_0 - \Delta\omega_k{}^{Pulling}\right)\right)\right)\right]\right. \end{aligned} \qquad \text{[III.3-14]}$$

Finally, to determine the elements of the modulation, i.e. A_0 amplitude at the fundamental frequency, ma and mf, we derive the equations that link those elements with the amplitudes $S_k^{\pm}$in dBm (+ on the right of f_0, - on the left of f_0) of the measured spurs as given in equation [III.3-6]. We obtain:

$$A_0 = \frac{1}{k+1}\sqrt{2 \times R_0 \times 1\text{mW} \times 10^{\frac{S_0(\text{dBm})}{10}}} \qquad \text{[III.3-15]}$$

- If mak>0, mfk<0

$$\begin{cases} ma_k = |ma_k| = \dfrac{1}{A_0}\left(S_{k\,lin}{}^{+} + S_{k\,lin}{}^{-}\right) \\ mf_k = -|mf_k| = \dfrac{\Delta\omega_k{}^{Pulling}}{A_0}\left(S_{k\,lin}{}^{+} - S_{k\,lin}{}^{-}\right) \end{cases} \qquad \text{[III.3-16]}$$

- and if mak<0, mfk>0

$$\begin{cases} ma_k = -|ma_k| = \dfrac{1}{A_0}\left(S_{k\,lin}{}^{+} - S_{k\,lin}{}^{-}\right) \\ mf_k = |mf_k| = \dfrac{\Delta\omega_k{}^{Pulling}}{A_0}\left(S_{k\,lin}{}^{+} + S_{k\,lin}{}^{-}\right) \end{cases} \qquad \text{[III.3-17]}$$

with S_{lin} the peak equivalent amplitude of Sin dBm.

By applying this approach to model the presumed input signal source of the SAW filter we obtain for k=6:

- A0 = 8.638E-2 V
- ma1 = 6.48
- mf1 = -2.74E+6; Kf1 = -2.3
- ma2 = 1.50
  mf_2 = -1.3E+6; Kf_2 = -5.75E-1
- ma3 = 4.44E-1
  mf_3 = -7.38E+5; Kf_3 = -2.17E-1
- ma4 = 1.76E-1
  mf_4 = -4.78E+5; Kf_4 = -1.05E-1
- ma5 = 4.97E-2
  mf_5 = -1.5E+5; Kf_5 = -2.65E-2
- ma6 = 1.52E-2
  mf_6 = -5.36E+4; Kf_6 = -7.9E-3

  with $Kf_k = \dfrac{mf_k}{\Delta\omega_k{}^{Pulling}}$.

Through the determined coefficients of Fourier transform of the AM-FM multi modulation derived, the spectrum of the presumed input signal of the SAW filter as described in [III.3-14] is given in the figure below:

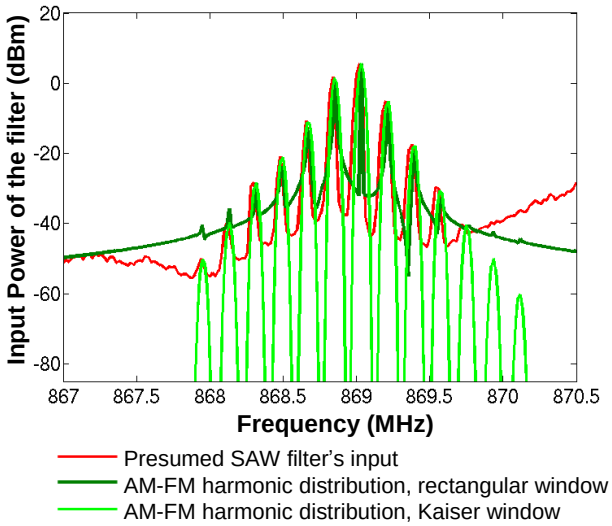


Figure III.3-4: The presumed input signal source of the SAW filter for f_0=868.82MHz

In Figure III.3-4 we show the importance of the Fourier transform windowing, here a Kaiser window [186] with a parameter β of 15 permits to widen the main lobes of the spurs and decreasing the noise floor of the signal.

By applying the cascade approach for that input source signal and the SAW filter, we obtain the green curve below.

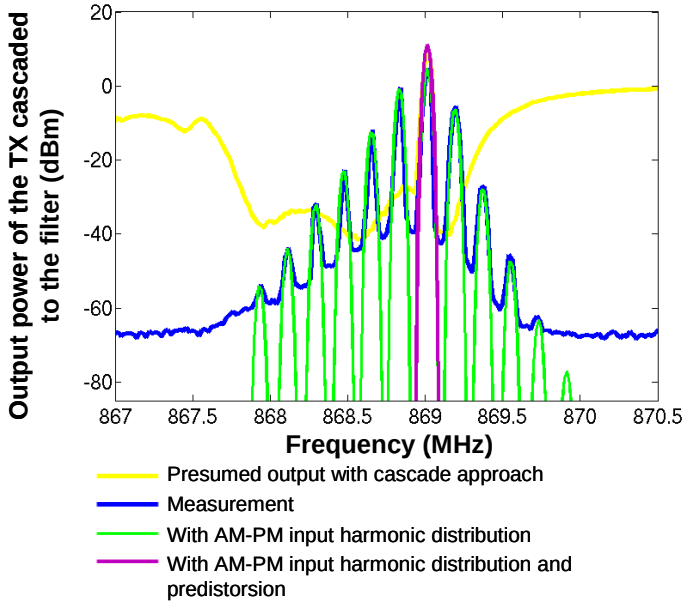


Figure III.3-5: Output signal of the LoPSTer's PCB cascaded to the SAW filter for f_0=868.82MHz with an AM/FM modeling of the pulling from the TX

Once the modulating elements representing the spurs of the pulling effects determined, we can analytically remove the spurs effects by subtracting the equivalent AM/FM information of the pulling to the measured output power of the TX cascaded to the filter, or by adding a predistorsion block inside the cascaded chain. The result of this feedback predistorsion approach is compared to the result of the direct cascade approach between the output of the TX without the SAW filter and the transfer function of the filter for a load of 50 Ω. Figure III.3-5 shows that the two results perfectly match.

III.4. PLL Function Blocs Analysis & Description

In chapter I, we briefly discussed about the principal blocks of a PLL. In this paragraph a synopsis of the different blocks of a basic analogue PLL is performed in order to point up the parameters that interfere in the PLL operation and to describe the function blocs transfer function used in the model derived.

III.4.1. The Reference

The reference clock of the PLL is generally obtained from an external piezoelectric crystal with good frequency stability and spectral purity but a low input frequency around 10MHz.

In our model, the reference signal will be modelled as a simple square or sinus signal of frequency 16MHz.

III.4.2. The Phase Frequency Detector & the Charge Pump

The phase/frequency error detection and conversion block of the PLL can be analyzed in two parts:

- The PD determines the phase and frequency error between the reference and the output signal divided by N , fdiv, in order to generate a correction voltage of DC value linearly proportional to the phase difference $\Delta\varphi$. If $-\pi<\Delta\varphi<\pi$, the analysis will be in phase domain, and if $\Delta\varphi>\pm\pi$ we will consider a frequency error.
- The CP will convert the correction voltage into a current.

a. The Phase Frequency Detector

The phase and frequency detection is made by converting the time difference between the pulsed reference signal and the output signal of the divider as the following state machine:

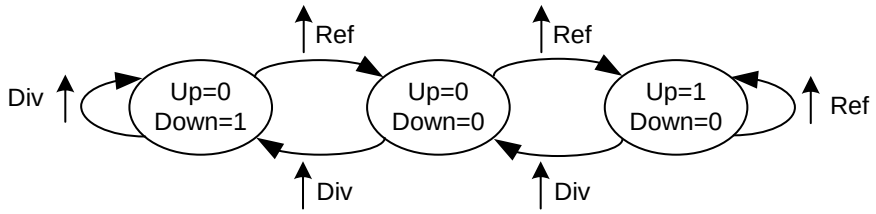


Figure III.4-1: PFD state machine

A PFD typical implementation with edge-triggered resettable D flip-flop is given in Figure III.4-2. The implementation of the PFD is made possible using Simulink Extras Flip Flops library or a Verilog-AMS code as described in Appendix C.2.a, or through a schematic design of the PFD including the corelib cells of the technology used.

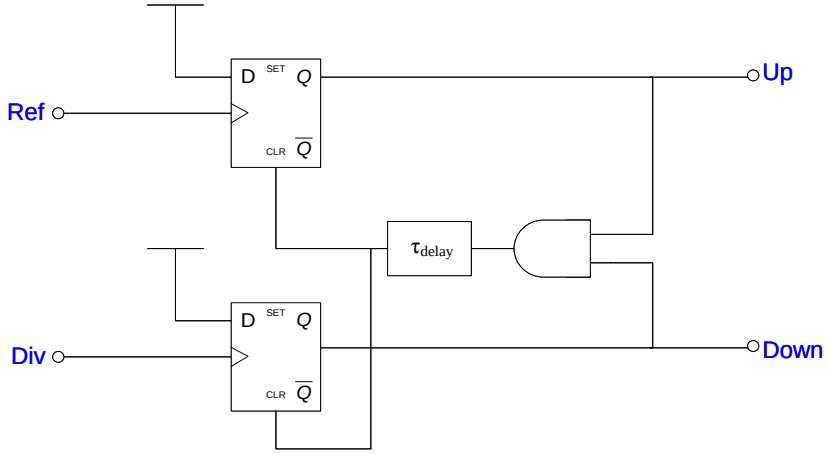


Figure III.4-2: Typical implementation of PFD

b. The Charge Pump

The PFD output drive a three-state charge pump, as we can see in Figure III.4-3: the Up output of the PFD enables a positive current source +ICP and the Down output enables a negative current source -ICP; the current polarity depends on the edge which arrives first. By pulsing a current during the time difference of the two input signals edges, since current multiplied by time equals charge, the charge pump, as its name suggest, preceded by the PFD creates an output charge proportional to the phase difference $\Delta\varphi$.

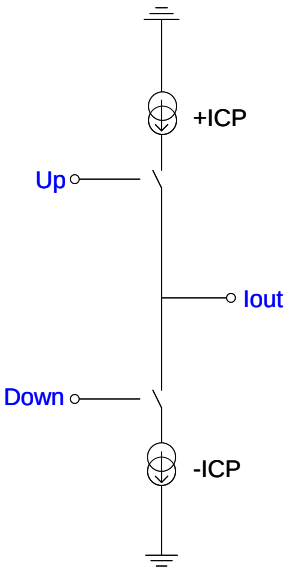


Figure III.4-3: Typical charge pump circuit

The average total output current Iout over one cycle is then also proportional to the time difference between the Up/Down edges.

The implementation of the charge pump into the model is obtained with SimPower Systems elements and/or electrical (controlled) current sources with Simulink, or a Verilog-AMS code as described in Appendix C.2.b where the schematic implementation is also given.

To illustrate the PFD-CP functioning, Figure III.4-4 shows its operation for different signal waveforms. The minimum pulse length determined by the reset delay τ permits to avoid the dead zone effect (a region where the charge-pump currents cannot flow proportionally to the phase error that leads to phase jitter) that would increase the noise level and degrade the CP and the whole PLL performances. However because of this delay, short

pulses on both UP and DOWN signals even in the locked state will appear. The charge-pump current will then switch on and off at a periodic time equivalent to the reference frequency. At the PLL output spectrum, reference spurs at a frequency offset from the carrier signal equal to the reference frequency are generated [187]. In order to reduce these spurs amplitude, the ±ICP source current pulses should always attain nominal peak level whatever the input timing through τ, and the reset delay should be small enough so that pulsed operation is less noisy than continuous: noise power spectral density is weighted by the factor τ / T_{Ref}, T_{Ref} being the reference period. In lock configuration, the average current delivered to loop filter is zero.

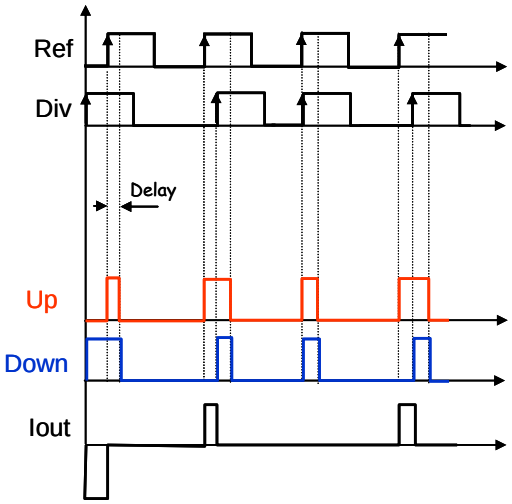


Figure III.4-4: PFD and CP functioning

The output signal ICP of the PFD-CP is non periodical three-states square signal and then consists of a number of terms ; in the locked state of the PLL, the first term is a DC component proportional to the phase error Δφ; the remains terms are AC components having frequencies $k \times \omega_{Ref}$, k integer. Only the DC part contains the information required; the output signal of the phase detector should then be low filtered.

The input-output characteristic of the PFD-CP can be represented as Figure III.4-5 while considering the DC part of ICP. In phase detection mode, when $f_{ref} = f_{div}$ the PFD can take any state of Figure III.4-5 and the CP response of phase error is linear; from –2π to +2π, the PFD-CP transfer function is:

$$K\phi = \frac{\overline{ICP}}{2\pi} \qquad \text{[III.4-1]}$$

In frequency detection mode the phase error slips with time. If $f_{ref} < f_{div}$ "Div" edges are more frequent than "Ref" ones, the PFD Down state toggles between 0 or 1 as in blue line in Figure III.4-4: the CP response of negative phase error in average is sawtooth of amplitude between –ICP and 0. If $f_{ref} > f_{div}$ "Ref" edges are more frequent than "Div", PFD Up state toggles between 0 or 1: the average CP response for a positive phase error is of sawtooth of amplitude between 0 and +ICP

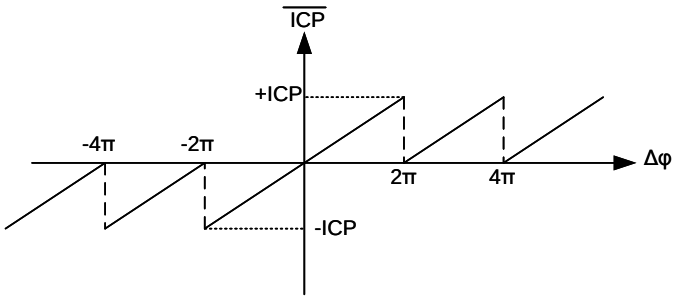


Figure III.4-5: PFD- CP characteristics

The output signal of the PFD-CP is non periodical three-states square signal and then consists of a number of terms ; in the locked state of the PLL, the first term is a DC component proportional to the phase error $\Delta\varphi$; the remains terms are AC components having frequencies $k\times\omega_{Ref}$, k integer. Only the DC part contains the information required; the output signal of the phase detector should then be low filtered.

It has to be noticed that the charge pump noise transfer function shows that the PFD/CP noise decreases when increasing the charge pump gain/peak current.

III.4.3. The Low-pass Loop Filter

The PFD-CP output should be converted to a DC signal to control the oscillator. The loop filter integrates the charge pump current pulses for generating the control voltage of the VCO.

The loop filter transfer function Z(s) is defined as the output voltage of the filter i.e the change voltage at the tuning port of the VCO, divided by the current at the charge pump output that causes it. The derivation of Z(s) is largely discussed in chapter 8 of [188]. Passive filter examples which are the most appropriated to charge pump PLL are given in Figure III.4-6.

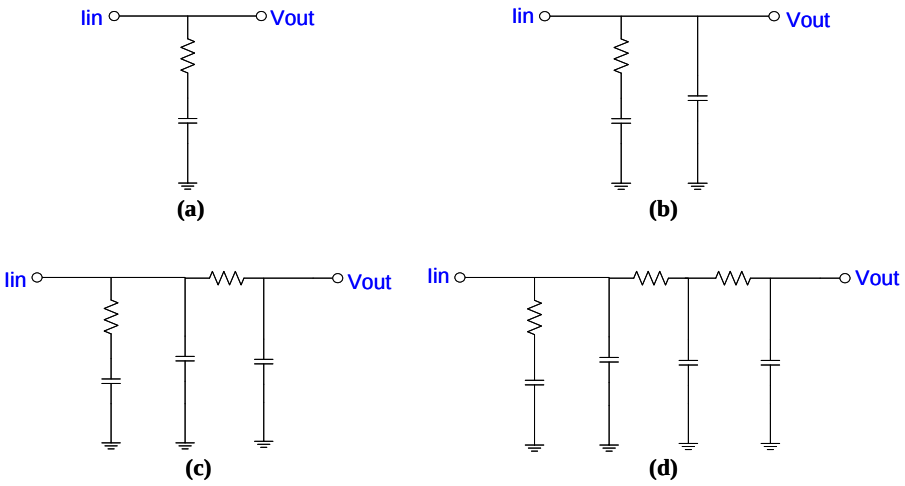


Figure III.4-6: Passive loop filters of 1st order (a), 2nd order (b), 3rd order (c) and 4th order (d)

We will see later that the zero of the filter transfer function is crucial because it has a strong influence on the damping factor ζ of the PLL and its open loop stability. The loop low pass filter determines the loop bandwidth. Otherwise, with higher order loop filter, the slope of the transfer function is steeper resulting in lower spurs level. However when adding passive components, more resistors add noise to the loop bandwidth and the VCO input capacitance in parallel to the highest order capacitance can cause distortion because of its variations in particular if this capacitance is too small.

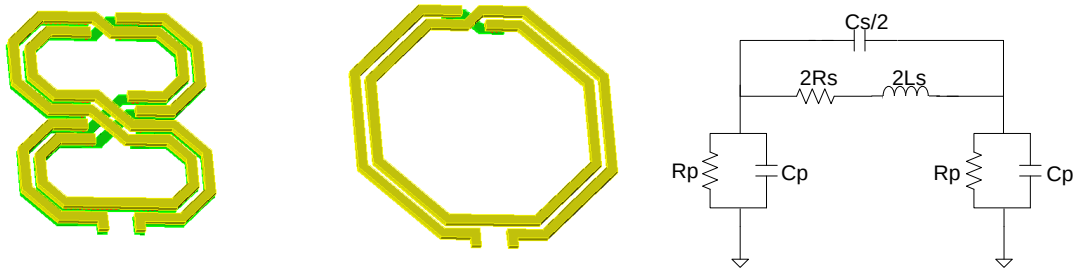
III.4.4. The Voltage Controlled Oscillator (VCO)

The VCO is the key block of the PLL that permits to deliver a periodic high frequencies signal. As the VCO determines roughly 50% of the noise performance of the PLL, its topology should then be carefully chosen. The LC based oscillators offer lower phase noise than ring oscillators and multivibrator oscillators for a given frequency and can operate at higher frequencies [189], [190]: for RF applications, LC oscillators are the most common VCOs topology.

The LC-VCO frequency is set by a LC resonant circuit and by definition the VCO output frequency depends on the value of the tank inductance L_{tank} and the equivalent total capacitance C_{tot} of the VCO:

$$f_{VCO} = \frac{1}{2\pi\sqrt{L_{tank} \times C_{tot}}} \qquad \text{[III.4-2]}$$

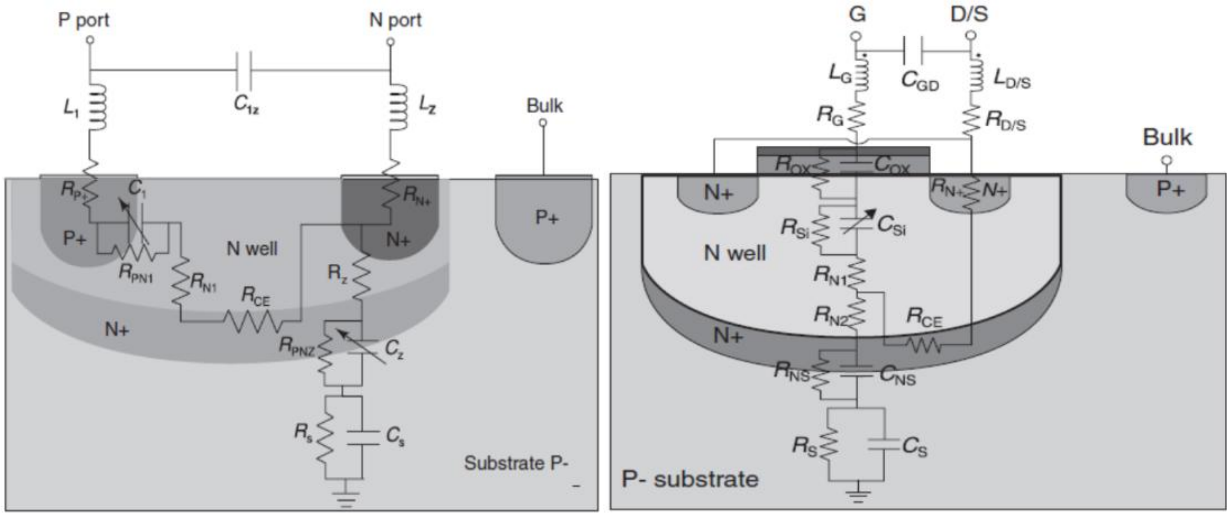
The tank inductors in NXP are mostly integrated octagonal or eight-shaped inductors.



(a) **(b)** **(c)**

Figure III.4-7: Example of 8-shaped (a) and Octagonal (b) integrated inductances and their equivalent circuit (c)

The tuning range of the VCO is determined by tank varactors (MOS or bipolar) whose capacitance values are tuned by the output voltage of the loop filter and the frequency step or switching band of the VCO output is set by a fixed capacitance or a switched varactors network.



(a) **(b)**

Figure III.4-8: Electric model of a PN-junction varactor (a) and of an accumulation NMOS varactor (b) [191].

As we can see in Figure III.4-7(c) and Figure III.4-8, parasitic resistances are in series with the tank inductance and capacitance. They will impact the quality factor Q_T of the LC circuit that determines the phase noise performance of the oscillator and can be determined from the physical passive devices of the VCO.

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_C} \qquad \text{[III.4-3]}$$

As normally the quality factor of the capacitor Q_C is much bigger than the quality factor of the integrated inductor Q_L, Q_T can be assumed as the quality factor of the inductor.

In order to compensate the resistive loss in the LC resonant circuit (that can be represented by a parallel resistance) and to maintain oscillation, a negative conductance Gm is presented to the tank, created by transistors. An example of LC bipolar VCO is given in Figure III.4-9.

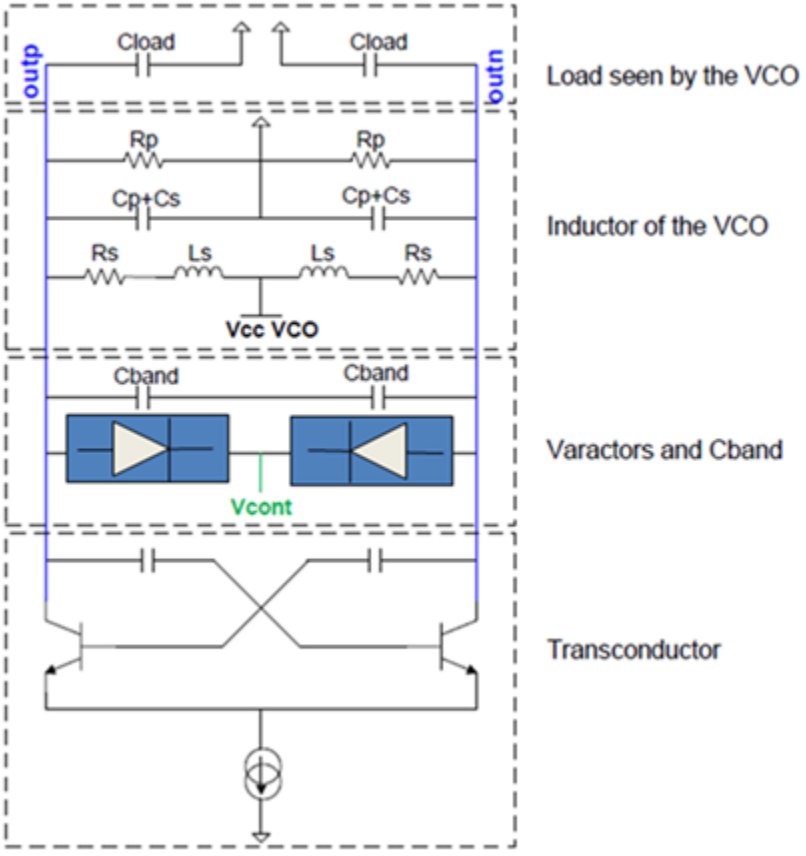


Figure III.4-9: Equivalent schematic model of an LC-VCO

The VCO is a circuit that generates a periodic output signal, sinusoidal for a LC-VCO, whose frequency f_{VCO} depends on its control voltage as shown in the following equation:

$$f_{VCO}=f_{FR}+K_{VCO}\times Vcont \qquad [III.4\text{-}4]$$

with f_{FR} the free running frequency of the VCO and K_{VCO} its gain expressed in Hz/V.

A linear tuning characteristic of the VCO is generally desired, K_{VCO} should then be constant in the frequency band of functioning.

A non constant K_{VCO} can introduce problems in terms of PLL stability that can become critical. In addition, as K_{VCO} non linearities come from the varicaps non linearities, non constant K_{VCO} can lead to PLL bandwidth variation and locking time variation over the tuning range.

Since the phase is the integral of the frequency with respect to time,

$$\begin{aligned}\varphi_{VCO}(t) &= \int \omega_{VCO}(t)dt \\ &= 2\pi \cdot K_{VCO} \int Vcont(t)dt\end{aligned} \qquad [III.4\text{-}5]$$

the transfer function of the VCO is, in the Laplace domain :

$$\frac{\varphi_{VCO}(s)}{Vcont(s)} = \frac{2\pi \cdot K_{VCO}}{s} \qquad [III.4\text{-}6]$$

and the output of a sinusoidal VCO can be expressed as:

$$y(t) = A \cdot \cos\left(\omega_{FR} t + 2\pi \cdot K_{VCO} \int_{-\infty}^{t} Vcont \cdot dt \right) \quad \text{[III.4-7]}$$

As free running LC oscillators have a central frequency which varies in time with temperature and average frequency that depends on absolute control voltage, VCO will preferably be integrated into locked-phase system as PLL.

As seen in chapter I paragraph 1.2.2(pulling definition), in response to a perturbation, an oscillator reacts and moves in the amplitude-frequency domain to keep fulfilling the oscillation conditions. The oscillator is then a moving steady state.

In order to describe the VCO using a Simulink model, (in Spectre view, an LC VCO will be implemented at transistor level or described with a Verilog-AMS code using the equation [III.4-7]), the non linear characteristics of the VCO frequency is expressed from the VCO gain variation in function of the tuning voltage described by an implicit Simulink function-block that links Vcont and the output frequency of the signal. The resulting sine-like response is converted into phase variation (phase-state domain), by means of integration. In this case, the frequency will be more subjected to change than amplitude and the VCO is more sensitive to a perturbation which is close to the oscillation frequency.

III.4.5. The Feedback Loop and Divider

The feedback loop of the PLL permits to inject the output signal of the VCO to the phase/frequency comparator. Synthesizers often require that the output frequency of the PLL is larger than the input frequency; frequency dividers are inserted in the feedback loop in order to adapt the output signal to the frequency wished by synchronizing it to the reference signal.

Yet, the parameter that has the largest impact on phase noise is the N counter value. The smaller this value is, the better the phase noise should be because the N counter value multiplies the noise

To perform a divider by N, N integer or fractional, programmable counters, prescaler or cascaded 2/3 cells [192] are used so the feed-back loop delivers an “edge” or “pulse” every N periods of the VCO to the PFD. As the transient simulation of the dividers takes lots of time and memory, a Verilog-AMS view will be used. For the Simulink model, before applying the sinus function on the VCO block defined by its gain, a simple gain of 1/ N is applied.

The different blocks of the Phase Locked Loop have been detailed, let’s connect them together and see the functioning of the entire PLL.

III.5. Predictive Behavioral Modeling Analysis of PLL Pulling

After dealing with behavioral modelling in phase domain, we will deal with a time domain model we've derived based on a hybrid mathematical and SPICE/Spectre view function block parameters. The signal spectrum is obtained by an FFT.

The predictive model could be implemented in Matlab Simulink or in Spectre using Verilog-AMS function blocks.

III.5.1. Behavioral Modelling of PLL in Phase Domain

a. Feed-back Loop

A PLL can be represented as a 2-port feed-back loop system. The principal path is described by the forward transfer function G(s) or forward gain, the return path by the feed-back transfer function or feed-back gain H(s). Using this loop model, the stability of the PLL can be studied.

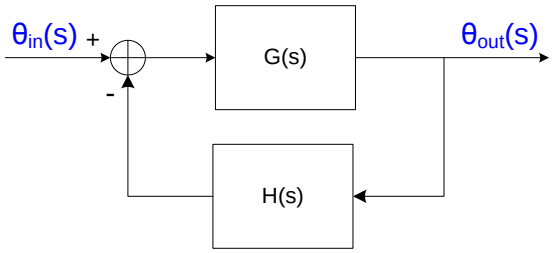


Figure III.5-1: Feed back loop system

The transfer function T(s) of the closed PLL loop is:

$$T(s) = \frac{\theta out(s)}{\theta in(s)} = \frac{G(s)}{1 + G(s) \times H(s)} \qquad \text{[III.5-1]}$$

The open-loop transfer function W(s) is defined as the product of the forward and the feed-back gain of the system:

$$W(s) = G(s) \times H(s) \qquad \text{[III.5-2]}$$

From the open-loop transfer function, feed-back loop parameters can be defined to quantify the loop behaviour: the loop bandwidth, ω_c, and phase margin, Φ_M, are defined from the open-loop transfer function as follows:

$$|W(j\,\omega_c)| = 1 \text{ or } 0dB \qquad \text{[III.5-3]}$$

$$\angle W(j\,\omega_c) - (-180) = \Phi_M \qquad \text{[III.5-4]}$$

The gain margin G_M is defined as the difference between unity and the amplitude of the open-loop when the phase of W is -180°.

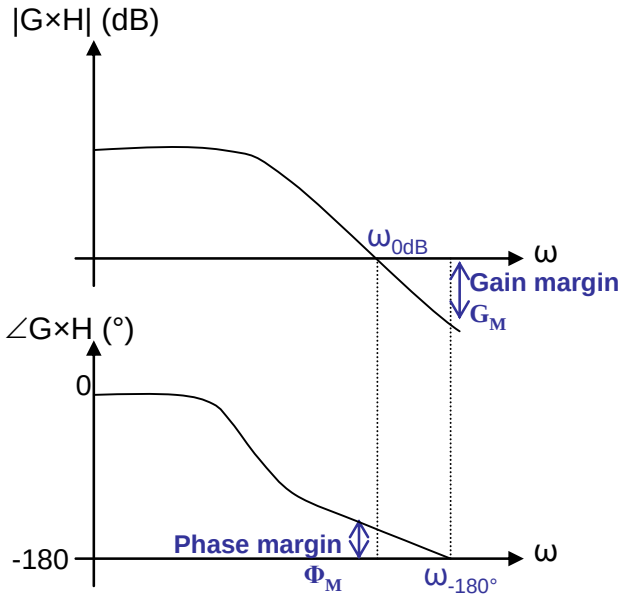


Figure III.5-2: Gain margin and phase margin definition

From the parameters defined, the stability criteria of the loop can be determined: the feedback loop will be stable if the phase at ω_c fulfils the next condition: $0 > \angle W(j\omega_c) > -180°$. The PLL is then stable if its phase margin is positive and unstable if the phase margin is negative at ω_c [193]. An illustration is given in Figure III.5-3.

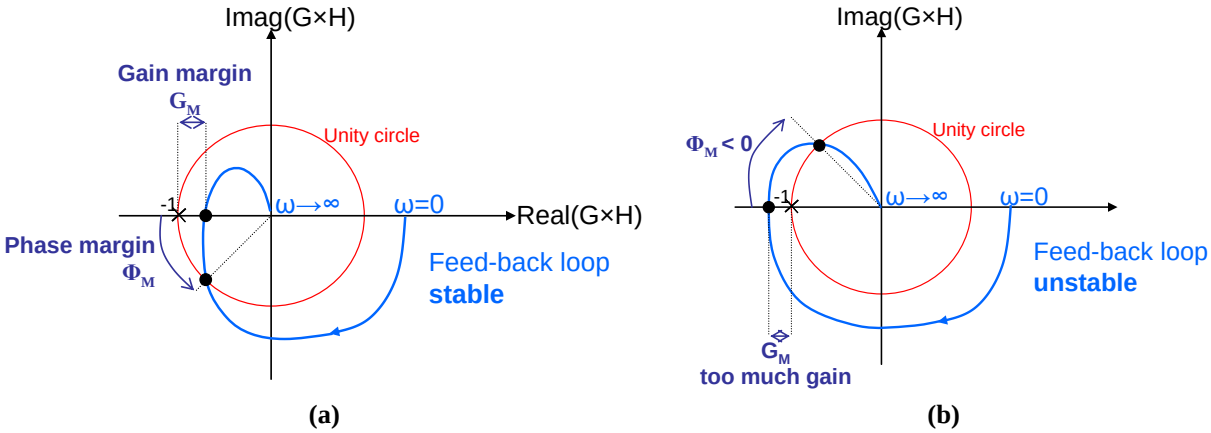


Figure III.5-3: Stability criteria of a feed back loop

Phase margin around 48 degrees yields the optimum lock time (see chapter 20 of [188]).

For restricted loop bandwidth, spurs level will be improved but at the expense of the lock time; for larger loop bandwidth, it will be the opposite. A compromise should be found for a good balance between spurs levels and lock time.

b. Charge Pump PLL Model

Classical approach modeling of charge pump PLL in phase domain can be derived using a linear, time-continuous assumption associated to a feed-back loop.

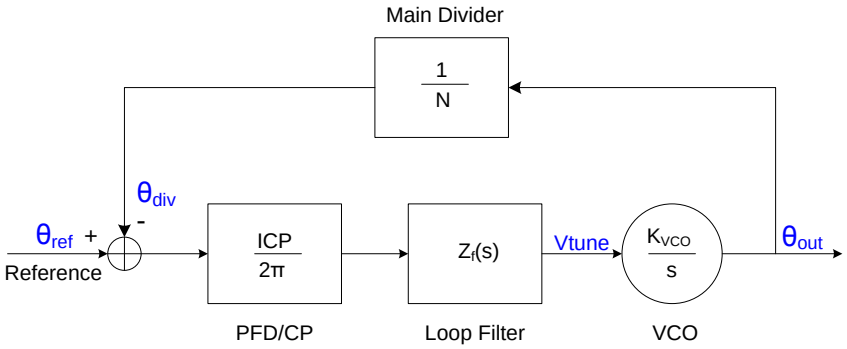


Figure III.5-4: Linear time-continuous model of charge pump PLL model

In this case, the time-continuous assumption can be considered to be valid as long as the loop bandwidth is << $f_{ref}/10$.

The closed loop transfer function of the PLL can be then defined as:

$$T(j\omega)=\frac{\theta_{VCO}}{\theta_{ref}}=\frac{N\cdot K\varphi\cdot Z_f(j\omega)\cdot K_{VCO}}{N\cdot j\omega+K\varphi\cdot Z_f(j\omega)\cdot K_{VCO}},\quad \text{with } K\varphi=\frac{ICP}{2\pi} \qquad \text{[III.5-5]}$$

by setting θout=θVCO in the PFD/CP transfer function [III.4-1].

The open loop transfer function of the PLL is:

$$W(j\omega)=\frac{K\varphi\cdot K_{VCO}\cdot Z_f(j\omega)}{N\cdot j\omega} \qquad \text{[III.5-6]}$$

Despite the strong approximations made in the previous equations, these last ones are very useful to study the stability of the PLL. As an example, the parameter K_{VCO} is assumed to be constant which is not the case in a practical application: as shown in Figure II.3-4 of chapter II, the output phase θ_{out} variation involves a non-constant K_{VCO} parameter. Besides, the divider and the PFD are not "time-continuous" functions: the main divider produces an "edge" every N periods of the VCO and the PFD delivers a current pulse of variable width every period of the reference.

A time domain analysis is then necessary to consider the variations of the PLL parameters.

c. Phase-Domain Behavioral Modeling

The aim of behavioral modeling is to derive simple and effective behavioral model for phase locked loop. An analytical model can be founded on phase-domain formulation using a phase error. Such a model can be useful to analyze different aspects of PLL systems and act on a set of parameters for optimization of their performances. Challenges with phase-domain description are in link with difficulties to extract time-domain waveforms that captures the locking effects of the PLLs to model.

Let's consider the following evolution equation for the instantaneous frequency:

$$f_{inst}(t)=f_{ref}+\Delta f_{inst}(t) \qquad \text{[III.5-7]}$$

where $f_{inst}(t)$ is the instantaneous frequency and $\Delta f_{inst}(t)$ designate the fluctuations of the instantaneous frequency over time. f_{ref} is the mean reference frequency.

It is possible to put the instantaneous fluctuations in the following form:

$$\Delta f_{inst}(t)=\Delta f_{slope}\times h_{inst}(t) \qquad \text{[III.5-8]}$$

$h_{inst}(t)$ being a normalized time-domain function with values in the domain [-1,+1]. The instantaneous frequency gives a formal signature of the PLL system.

From the instantaneous frequency, instantaneous-phase can be deduced following the expression:

$$\theta_{inst}(t) = \int_0^t 2\pi f_{inst}(\tau)d\tau = 2\pi f_{ref}\, t + 2\pi f_{ref}\, \Delta f_{slope} \times \int_0^t h_{inst}(\tau)d\tau \qquad \text{[III.5-9]}$$

The output signal of the oscillator is given by:

$$S(t) = \cos[\theta_{inst}(t)] = \cos\left[\pi f_{ref}\, t + 2\pi f_{ref}\, \Delta f_{slope} \times \int_0^t h_{inst}(\tau)d\tau \right] \qquad \text{[III.5-10]}$$

Assuming small variations $2\pi f_{ref}\, \Delta f_{slope} \times \int_0^t h_{inst}(\tau)d\tau$ such that :

$$\sin\left(2\pi f_{ref}\, \Delta f_{slope} \times \int_0^t h_{inst}(\tau)d\tau \right) \approx 2\pi f_{ref}\, \Delta f_{slope} \times \int_0^t h_{inst}(\tau)d\tau .$$

The following approximation can be derived:

$$S(t) \cong \cos[2\pi f_{ref}\, t] - 2\pi f_{ref}\, \Delta f_{slope} \times \sin(2\pi f_{ref}\, t) \int_0^t h_{inst}(\tau)d\tau \qquad \text{[III.5-11]}$$

Taking the Fourier transform of the output signal leads to:

$$S_{FFT}(f) = \frac{1}{2}\left(\delta_{f_{ref}} + \delta_{-f_{ref}}\right) - \frac{\Delta f_{slope}}{2j}\left[\frac{H(f - f_{ref})}{f - f_{ref}} - \frac{H(f + f_{ref})}{f + f_{ref}} \right] \qquad \text{[III.5-12]}$$

H being the Fourier transform of h.

Thus, the power spectral density can be extract from the Fourier transform of the output signal. It gives insight into the spectral content with distribution of noise spurs. For accurate analysis spectral aliasing should be considered, with proper interpolation.

III.5.2. Methodology & Modeling Approaches for Predictive Simulation of PLL Pulling in Time Domain

In time domain analysis, the VCO output is conventionally expressed as:

$$y(t) = A \cdot \cos\left(\omega_{FR}\, t + 2\pi \cdot K_{VCO} \int_0^t Vcont \cdot d\tau \right) \qquad \text{[III.5-13]}$$

ω_{FR} being the free running angular frequency of the VCO. Besides, the output phase θ_{out} of the VCO can be expressed has:

$$\begin{aligned} \theta_{out}(t) &= \int_0^t 2\pi \cdot f_{out}(\tau)d\tau \\ &= \int_0^t 2\pi\left[f_{FR} + K_{VCO}(V_{Tune}) \times V_{Tune}(\tau) \right]d\tau \end{aligned} \qquad \text{[III.5-14]}$$

Equation [III.5-13] and [III.5-14] imply that if the VCO gain is non constant, the VCO is a frequency modulator. Then if the control voltage oscillates at a frequency of ω_m, the output spectrum of the VCO will consist of a main tone at f_{FR}, and sidebands due to the frequency modulation at $k\times f_{FR} \pm f_m$. Section III.3.1 detailed the spectral component of the different modulations. Variations of the control voltage of the VCO should then be analyzed carefully in time domain in order to avoid non desired spurs on the output signal spectrum of the PLL.

a. Assumptions & Simplifications

We have seen in FigureII.2-2 of Chapter II that the pulling effects are already present in the output signal of the IC. Transient simulation of the VCO to the PA path showed that frequency pulling of the VCO output signal spread through the reshape buffer, the tri-state buffer and the Class-E power amplifier.

The frequency pulling then comes from the PLL and spreads along the IC transmit path without change in terms of frequency information and with negligible amplitude variations around the carrier frequency.

Predictive analysis restricted to the PLL block is thus sufficient to deal with frequency pulling.

b. Experimental Approach

The model behavior is mainly based on the VCO gain variations. The first approximation is to consider K_{VCO} to be fixed and then integrate it into the model as a simple coefficient, but the characterization of the VCO showed that this assumption can't be applied in frequency pulling issue as seen in Chapter II Figure I.5.6.

The starting point of the analysis will therefore begin with the experimental achievement of the VCO gain variation in function of the tuning voltage of the VCO under frequency pulling.

c. The Predictive Simulation Approach

Each PLL function block is described analytically or through Spice/Spectre view:

- The nonlinear characteristics of the VCO frequency as a function of tuning voltage are captured in the form of rational function from the measurement results. The extracted rational function is used within the PLL loop to account for non-constant KVCO parameter. If the variations of the VCO frequency are too fast or too abrupt in function of Vtune as seen in Chapter II Figure II.3-4 red curve, sub-bands functions can be determined to describe the whole frequency variations dependent on the tuning voltage. The resulting output sine-like response is converted into phase variation (phase-state domain), by means of integration.
- The phase obtained is divided by N and compared to the signal reference phase through flip-flops based Phase-Frequency Detector.
- The output signal of the PFD/CP that is homogeneous to a current sustains the passive lowpass loop filter described by its impedance $Zf(s)= Vtune(s)/ICP(s)$, with $s=j\omega$ or by an equivalent lumped RC circuit

It is then demonstrated that non-constant K_{VCO} parameter can induce sideband spurs according to its value if all the other parameters of the analogue PLL are assumed constant.

d. Implementation

The predictive simulation approach has been implemented in Matlab/Simulink and using a Verilog-AMS model in Cadence Spectre.

In Matlab/Simulink

The time domain model derived in Simulink represented in Figure III.5-5 is based on a hybrid mathematical and SPICE/Spectre view function block parameters. The combination of mathematical transfer functions and lumped components is made possible through Simulink library.

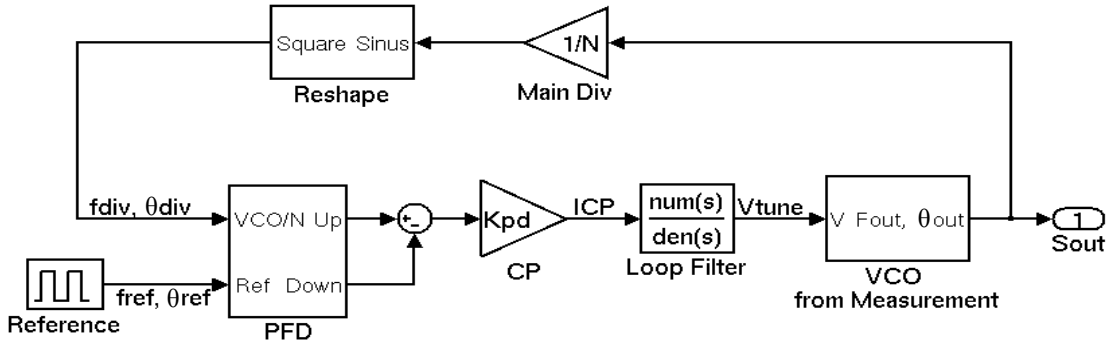


Figure III.5-5: Simulink time-domain model of single loop analogue PLL including VCO, Divider, PFD/CP and Loop-Filter.

The black-box defining the VCO is obtained by dividing the curve $f_{RF} = f(\text{Vcont})$ into n sub-bands where the slope of the function f: K_{VCO}, is assumed to be frequency dependant. This leads to equation [III.5-15]. At voltage control values of the VCO that induce pulling, K_{VCO} value can deliberately be increased to model this effect.

$$f_{RF}(\text{Vcont}) = \sum_{n} \left(K_{VCO}\big|_{Bn} \times \text{Vcont}\big|_{Bn} + f_{i}\big|_{Bn} \right) \cdot H\big|_{Bn}(\text{Vcont}) \qquad \text{[III.5-15]}$$

Where $\big|_{Bn}$ means on the control voltage band Bn, fi is the minimal frequency of the band Bn and $H\big|_{Bn}(\text{Vcont}) = \begin{cases} 1 \text{ if Vcont is in Bn} \\ 0 \text{ in other bands} \end{cases}$.

The VCO output phase is divided by a coefficient N and compared to a square signal reference phase, here a pulse generator, through D-flip-flops based Phase-Frequency Detector. The phase difference can be converted to current data through a current controlled source or a DC current source combined with an ideal switch.

The phase difference in current data cross over the loop filter which is described by it transfer function represented by a Simulink transfer function block whose numerator and denominator, respectively num(s) and den(s), are expressed from the RC components of the loop filter that permit to deliver the appropriated tuning voltage to the VCO.

In Cadence Virtuoso with a Verilog-AMS Code

By creating a configuration of different views (*config* view) of the PLL cell to analyze with Virtuoso, each function block of the PLL can be described in different ways: at transistor level with a schematic view or through a behavioral model with a Verilog, Verilog-A or Verilog-AMS view.

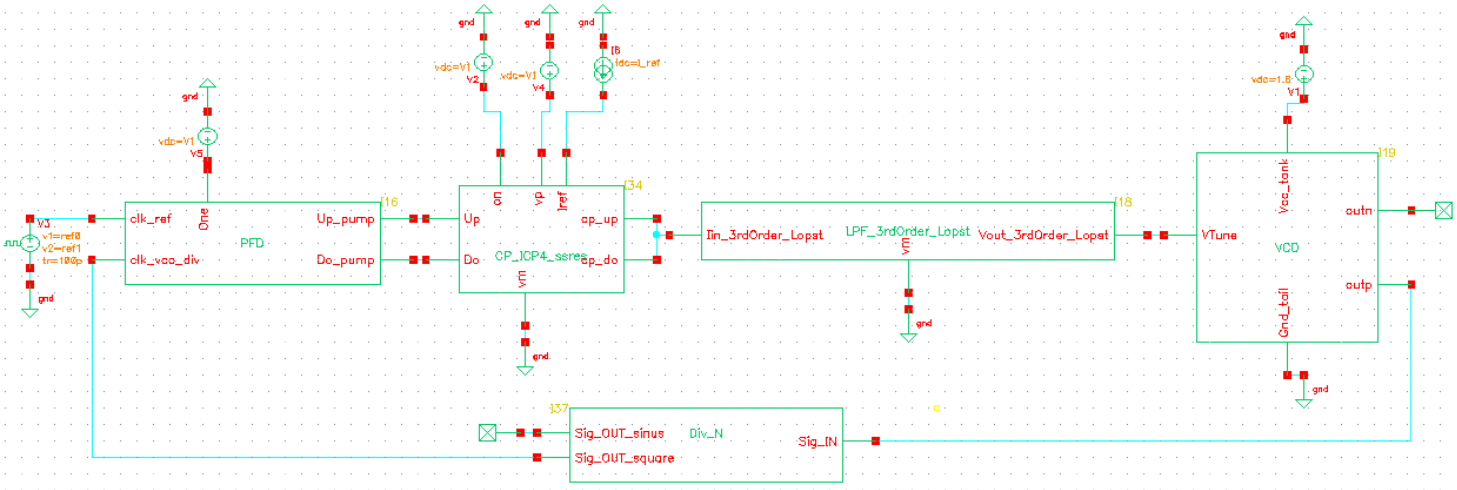


Figure III.5-6: Schematic view of a PLL where sub-function blocks are described either at transistor level or with a Verilog (-a, -AMS) code

From the comparison of the results obtained, the functional description of each sub-PLL block can be ameliorated, or the schematic view redesigned, to fulfil the behavior required.

The use of Verilog-AMS description permits to speed up the simulation time of the loop.

The PLL sub-function blocks descriptions in Verilog-AMS Code or at transistor level are given in the Appendix C: the PFD in C.2.a, the charge pump (CP_ICP4_ssres) in C.2.b, the VCO in C.2.c and the divider (Div_N) in C.2.d. The loop filter LPF_3rdOrder_Lopst is a 3rd order RC filter as given in Figure III.4-6(c).

III.5.3. Analysis and Discussion on the Predictive Simulations Results

The analysis with Simulink/Matlab of the equivalent model of the LoPSTer was performed with f_{ref}=16MHz with $N=f_{VCO}/f_{RF}$, the last capacitance C3 of the 3rd order loop filter that brings the 3rd pole should be 1.1pF but an additional capacitance of 2.4pF is evaluated in the design and its influence will be discussed. K_{VCO} initially at 30MHz/V becomes 110MHz/V around the cut-off high frequencies of the SAW filter [197] .

When the PLL is locked at a frequency where K_{VCO}=30MHz/V, the output spectrum of the VCO is a single tone at f_{RF}, whereas when the PLL is locked at a frequency inside the breakdown of the curve $f_{RF} = f(\text{Vcont})$ in Chapter II Figure III.2-4, spurs at $f_{RF} \pm k \times \Delta f$ are reported as we can see in Table III.5-1 and in Figure III.5-7 and Figure III.5-8.

Table III.5-1: Variations of the Pulling Frequency Functions of the PLL Parameters

	case #	ICP	C3, LPF	Δf spurs
K_{VCO} maximum variation in V1: 110MHz/V	**1a**	30 µA	3.5 pF	383.4 kHz
	1b	60 µA	1.1 pF	738.1 kHz
	1c	60 µA	3.5 pF	389.1 kHz
K_{VCO} maximum variation: 500 MHz/V	**2a**	30 µA	3.5 pF	360.5 kHz
	2b	60 µA	1.1 pF	560.8 kHz
	2c	60 µA	3.5 pF	326.2 kHz
K_{VCO} maximum variation : 1000MHz/V	**3a**	30 µA	3.5 pF	323.3 kHz
	3b	60 µA	1.1 pF	515 kHz
	3c	60 µA	3.5 pF	340.5 kHz

The pulling aspect around f_{RF} depends on the PLL parameters:

- the increase of ICP current and C3 loop filter parallel capacitor values make the PLL output spectrum worse in terms of number and amplitude of undesirable spurs until quasi-locking phenomenon as reported in [194] (case 3c with a frequency shift of the higher peak).

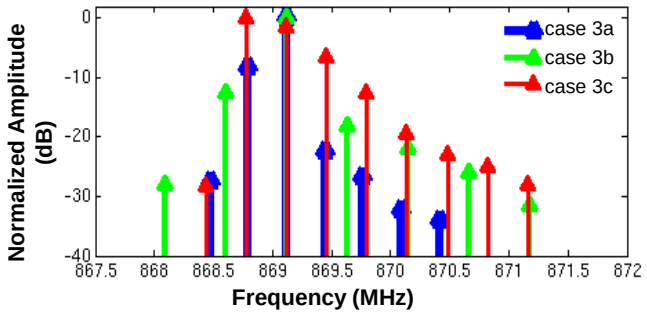


Figure III.5-7: Output spectra of the VCO integrated into a PLL obtained by Simulink simulation with K_{VCO} variations depending on ICP current value and the loop filter parameters

- However the main factor of frequency pulling is the value of the maximum slope of the VCO gain: the higher the maximal K_{VCO} value is, the higher are the amplitude and the number of the spurs.

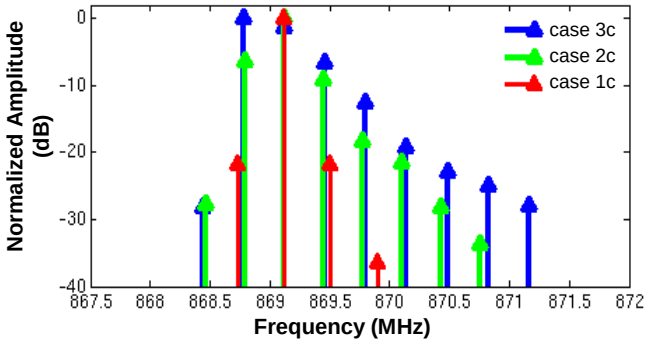
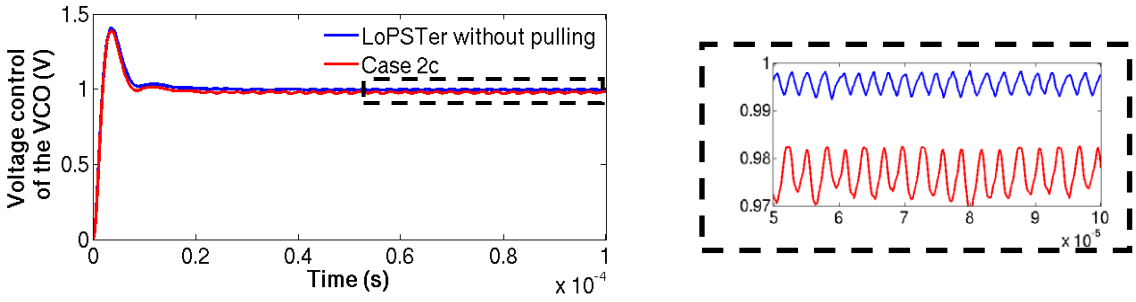


Figure III.5-8: Output spectra of the VCO integrated into a PLL obtained by Simulink simulation with K_{VCO} variations depending on the maximal value of K_{VCO}

The locking of the PLL is rapidly obtained with the proposed model but when it is reached, the control voltage of the VCO presents large and periodical oscillations around DC level when pulling issues are observed like assumed in [194].



(a) **(b)**

Figure III.5-9: Control voltage of the VCO obtained by Simulink simulation (a) and zoom(b)

When the K_{VCO} used for the LoPSTer modeling is obtained from the measurements where no pulling was detected, little oscillation is also obtained but the amplitude of the Vcont ripples is weak enough to obtain for the first coupled spurs around f_{RF} at an amplitude of 30dBc below the carrier one.

For a converging Vcont, the increase of K_{VCO} maximal amplitude results in the increase of the oscillation amplitude around the DC level of the control voltage and in the appearance of peaks at $k \times \Delta f$ in the associated spectrum. Output signal of the PLL model derived can then be derived as in Eq. (26) of [195] which explains the pulling spectrum observed in Figure III.5-7and Figure III.5-8.

III.5.4. Correlation Analysis between Simulations Results & Experimental Characterization, Validation

a. Stability Analysis of PLLs under Frequency Pulling

The principal cause of spurs that we may think of is the instabilities matters. In the LoPSTer case the power amplifier is of class E. The Rollet stability factor (K) definition usually used to identify whether if the PA oscillates or not shouldn't be used with class-E PAs. Indeed, the K factor definition is based on small signal analysis whereas the class-E power amplifier is a nonlinear large signal power amplifier using transistor(s) acting like a switch. Then, for pulling issues, only the PLL stability analysis is sufficient.

For that, the results of the open loop transfer function W of the PLL stability analysis are given in the Figure III.5-10. However as we can see, only the worse case 3c of Table III.5-1 leads to an unstable PLL. For the other cases where non negligible spurs exist around the fundamental tone, usual stability analysis of the PLL gives stable results even with pulling issues are observed in the measurements of of the PLL.

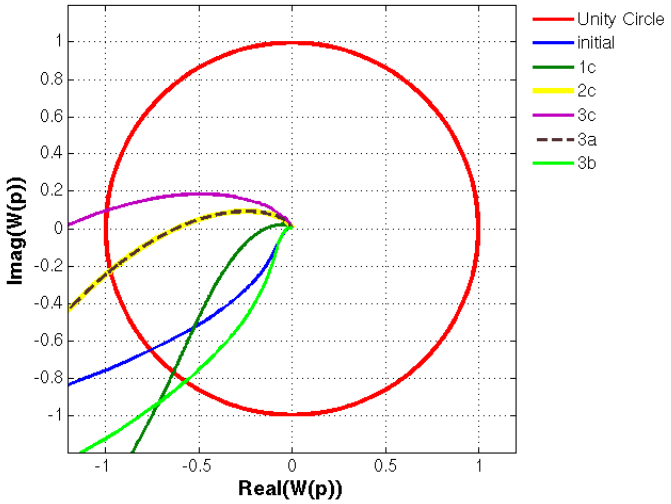


Figure III.5-10: Stability analysis of the PLL with K_{VCO}, ICP and the loop filter parameters varying according to the different cases given in Table II.5-I

In addition, we can see in the previous figure that a variation by a same factor of any function block parameter of the PLL give the same transfer function then the same gain and phase margin. For example in the cases 2c and 3a where the PFD/CP gain or the VCO gain are multiplied by 2, the static stability analysis gives the same curve if we do not consider the variations of K_{VCO}. However as we can see in Figure III.5-7and Figure III.5-8, with a dynamic model of the PLL, depending on which parameter of the PLL varies, the frequency pulling will have a specific behaviour.

b. Physical Interpretation of Observed Pulling Effects

The characterization of PLL frequency pulling applied to the LoPSTer at system-level made in chapter II has led to the following observations relatively to the investigated carrier [196]:

(i) Increasing the PA output power level increases the amplitude of sideband spurs
(ii) The presence of the SAW filter with fast variation of slopes at cut-off frequencies induces frequency pulling within a specific bandwidth.

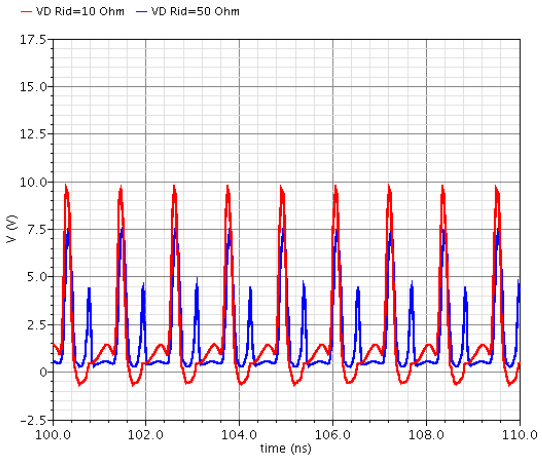
(iii) Increasing the PLL charge-pump current increases the amplitude of sideband spurs.

(iv) At frequencies of pulling issues the VCO gain is no longer linear and takes a peak value widely superior to the initial average value.

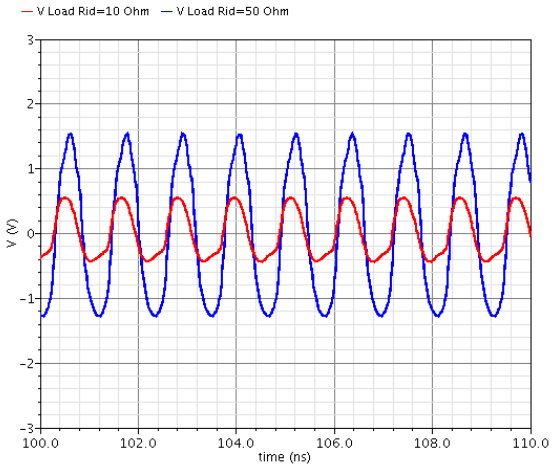
The interpretation of (i) is in link with two separate mechanisms:

- The first mechanism through which higher PA output power generates spurs is due to a retro-active coupling through substrate or conducted channels to the PLL loop and causes phase and amplitude modulations. Such coupling is observed to mainly originate from power-ground supply noise interferences. Experiments have shown that interrupting ground distribution between the PA and the PLL significantly reduce the observed pulling. The class of spurs analysis showed that frequency pulling is an AM and FM combination.
- The second mechanism is the coupling between the PA and the PLL loop through the second harmonic generation at the output of the PA as shown in the spectral power analysis (fig. I.3-6 of chap.2). As $f_{RF}=f_{VCO}/2$, it will be the second harmonic of the PA output that will be (re-) injected inside the PLL and cause the frequency pulling, the higher the amplitude of this 2nd harmonic, the higher the injection, the higher the amplitude of sideband spurs.

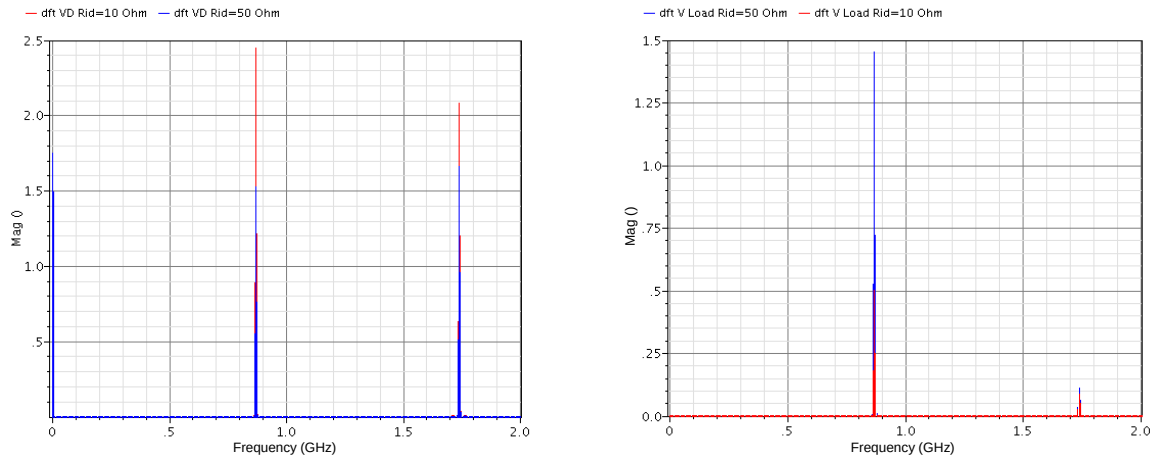
The interpretation of (ii) can be approached by evaluating the derivative of the SAW filter transfer function against frequency. Such derivative is reported in Fig.II.3-3(b) of chapter II (purple curve), where it can be observed that higher the slopes of the filter are, larger are the extracted derivatives. Correlation analysis between the filter transfer function derivatives and the characteristics of the local oscillator frequency as function of the voltage tuning shows that the limits of the ripples correspond to the filter bandwidth limits. In addition, Fig.II.3-3(a) of chapter II shows that at its cut-off frequencies, the input impedance of the filter loaded by 50Ω is no longer around 50Ω as desired and varies rapidly with the working frequency. Then, the load seen by the class-E PA is no longer the ideal load which it was designed for, the non linearity of the PA is worse and amplitude of the PA output 2nd harmonic that could be re-injected into the PLL increases as we can see in Figure III.5-11 (c).



(a)



(b)



(c) **(d)**

Figure III.5-11: Transient response of LoPSTer class-E PA described at the transistor level: at the switching transistor output (a) and the load input (b), and Fast Fourier transform of these responses (c), (d) when the load is, after the impedance transformation of the ideal load, 50Ω or 10 Ω

The interpretation of (iii) and (iv) results from the formal relation between the PLL transfer function, the charge-pump current and VCO gain. Resuming the transfer function of the classical approach modeling of PLL in phase domain given in chapter I equation [1.2.2],

$$T(j\omega) = \frac{\theta_{VCO}}{\theta_{ref}} = \frac{N \cdot K_{\varphi} \cdot Z_f(j\omega) \cdot K_{VCO}}{N \cdot j\omega + K_{\varphi} \cdot Z_f(j\omega) \cdot K_{VCO}}$$

This simplified dependence of the PLL transfer function against the charge-pump current ($K\varphi=ICP/2\pi$) and the voltage gain can explain the observed pulling effects. Yet in this equation, the VCO gain K_{VCO} is assumed to be constant, which is not the case in a practical application as demonstrated in Fig. II.3-4(b) of chapter II.

In general the output phase θ_{out} can be expressed as:

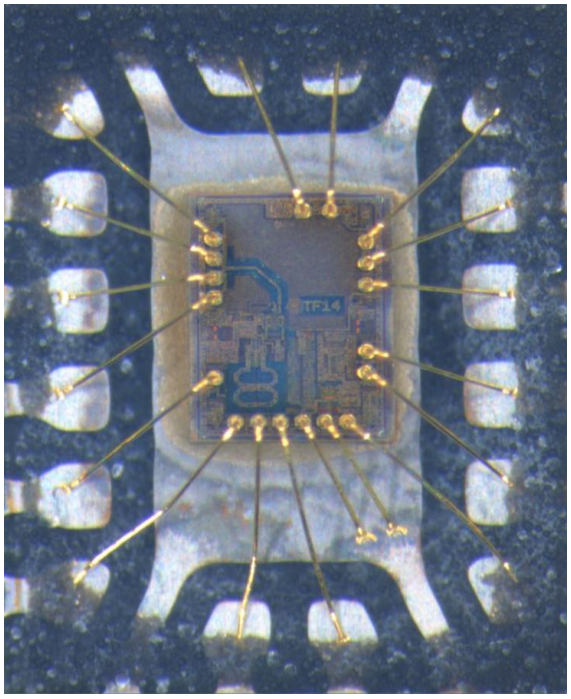
$$\begin{aligned} \theta_{out}(t) &= \int 2\pi \cdot f_{VCO}(t)dt \\ &= \int 2\pi \cdot \left[f_{center} + K_{VCO}(V_{Tune}) \times V_{Tune}(t)\right] dt \end{aligned} \qquad \text{[III.5-16]}$$

Yet, the output phase θ_{out} involves a non-constant K_{VCO} parameter. In the behavioral modeling for predictive analysis of the observed pulling effects derived, the dynamic characteristics of the PFD/charge-pump current and K_{VCO} parameter are implemented in the Matlab Simulink model. It was demonstrated that non-constant K_{VCO} parameter can induce sideband spurs according to its value if all the other parameters of the analogue PLL are assumed constant.

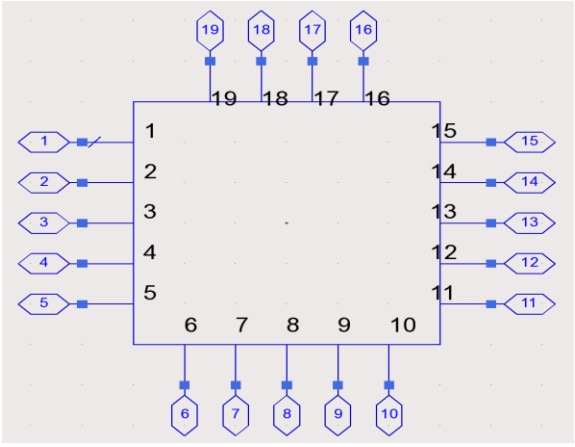
III.6. Importance of Chip-Package-PCB Co-Design and Co-Simulation

Bridging Chip, Package and Board domains requires properly taking into account combined effects resulting from Power Integrity (PI), Signal Integrity (SI) and Electromagnetic Couplings. To efficiently co-design and co-simulate packages through iterative forward and backward propagation of design constraints to chip and board levels, in order to meet global system performances efficient Co-simulation and Co-design, methodologies [198]-[202] are developed beyond tools functionality in collaboration with Cadence design systems.

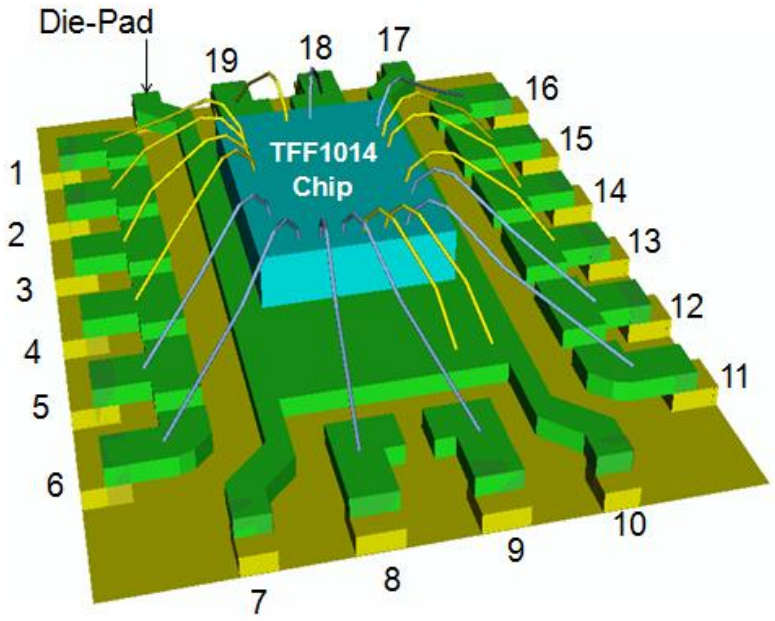
Modeling analysis using state of the art chip-package-PCB co-design tools is conducted for simulation of TFF1014 package families for virtual prototyping and design optimization. The 3D leadframe package model modeled using Cadence SiP (System-in-Package) environment is illustrated in Figure III.6-1. A variant of the leadframe package is shown in Figure III.6-2 with higher number of IO (input/output) pins.



(a)



(b)



(c)

Figure III.6-1: Micro –photography of the TFF1014 and its multi-port symbol (a) for reference leadframe package (b) using Cadence SiP

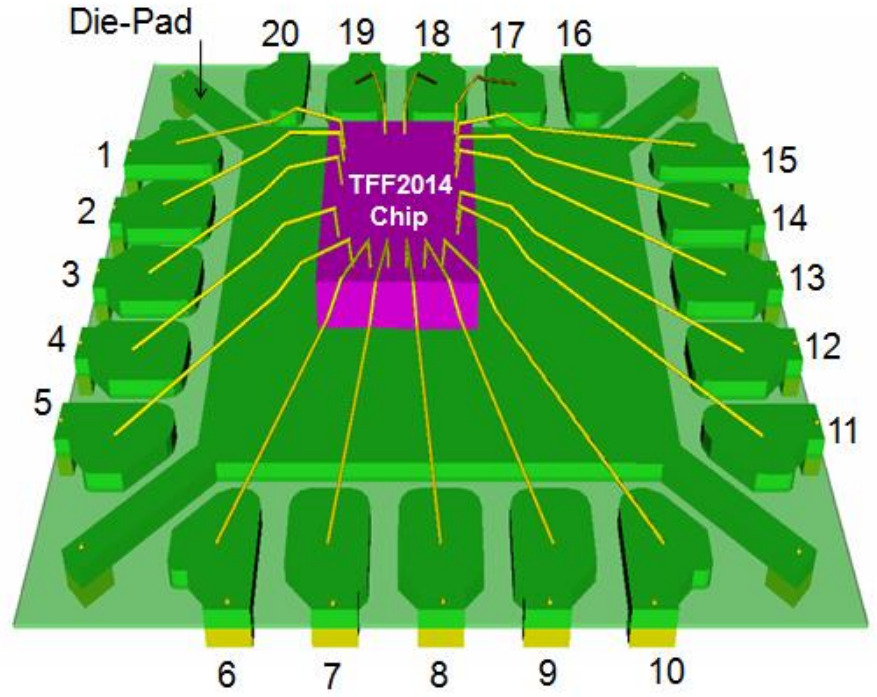


Figure III.6-2: A variant TFF1014 leadframe package with 20 I/O pins

Both full-wave and quasi-static solutions can be simulated for the full package design. For chip-package coupling analysis, quasi-static analysis is derived using Cadence-Apache solutions for extracting inductive (Lij terms), capacitive (Cij terms) and resistive (Gij and Rij terms) coupling contributions.

Table III.6-1 reports the obtained coupling terms.

The Inductance column can represent a number of different types of inductance depending on the problem set up. The self-inductance is displayed in columns where Net I = Net J; mutual inductance is specified in columns where Net I ≠ Net J. In the used quasi-static tool, mutual inductance terms can be signed positive or negative. This functionality allows the tool to support complex package coupling structures in the RLCG output files used for simulation. There is no label differentiation between Loop inductance and Partial inductance, so the user must be aware of what type of analysis has been completed. Loop inductance calculations include the partial inductance term from the signal net and the partial inductance calculated from the nets designated as Return Path Nets. The tool calculates the loop inductance considering all Return Path Nets designated. The loop inductance is more correctly termed a partial loop inductance since it is calculated from the partial inductance of the net and the partial inductance of the return path. The partial inductance is calculated by leaving the Return Path Nets table blank. In this case the loop is assumed to be at infinity with zero impedance return path.

The Capacitance column represents the capacitance calculated between Net I and Net J for mutual coupling and the capacitance to other unanalyzed coupling neighbours in the design, for self capacitance (Net I = Net J).

The Grounded net can be included in the inductance return path through four different methods. Each of these methods will result in a slightly different loop inductance result based on the calculation methodology.

The Conductance column represents the conductance calculated between Net I and Net J for mutual coupling and also the conductance to other unanalyzed coupling neighbours in the design, for self conductance (Net I = Net J). Designating a Return Path Net does not affect either the self or mutual conductance calculations. See the Capacitance calculation description for further details. The solutions are similar.

The Resistance column is populated with the series resistance value determined by the quasi-static tool. This term exists only for the self entries (Net I = Net J) in a two port net.

Table III.6-1: Inductive terms and mutual inductance terms of extracted leadframe package in Figure III.6-1

Net I	Net J	Inductance Lij (nH)	Capacitance Cij (pF)	Conductance Gij (S)	Resistance (mOhm)
1	1	1,21E+00	2,05E-01	2,50E+01	4,33E+02
1	2	2,47E-01	4,33E-02	5,69E+00	
1	3	5,91E-02	6,02E-03	6,87E-01	
2	2	1,13E+00	2,19E-01	2,68E+01	4,09E+02
2	1	2,47E-01	4,33E-02	5,69E+00	
2	3	1,43E-01	4,23E-02	5,55E+00	
3	3	1,18E+00	2,17E-01	2,66E+01	4,24E+02
3	2	1,43E-01	4,23E-02	5,55E+00	
3	4	1,14E-01	4,11E-02	5,38E+00	
4	4	1,23E+00	2,15E-01	2,64E+01	4,39E+02
4	5	1,67E-01	4,29E-02	5,63E+00	
4	3	1,14E-01	4,11E-02	5,38E+00	
5	5	1,36E+00	2,20E-01	2,69E+01	5,03E+02
5	4	1,67E-01	4,29E-02	5,63E+00	
5	6	1,60E-01	9,24E-03	1,13E+00	
6	6	1,47E+00	2,35E-01	2,88E+01	5,36E+02
6	7	2,72E-01	4,58E-02	6,00E+00	
6	8	1,05E-01	6,88E-03	8,06E-01	
7	7	1,45E+00	2,43E-01	2,99E+01	4,96E+02
7	8	2,82E-01	4,54E-02	5,95E+00	
7	6	2,72E-01	4,58E-02	6,00E+00	
8	8	1,41E+00	2,44E-01	3,00E+01	4,91E+02
8	7	2,82E-01	4,54E-02	5,95E+00	
8	9	2,64E-01	4,58E-02	6,01E+00	
9	9	1,53E+00	2,50E-01	3,08E+01	5,27E+02
9	10	3,25E-01	4,65E-02	6,12E+00	
9	8	2,64E-01	4,58E-02	6,01E+00	
10	10	1,65E+00	2,38E-01	2,91E+01	5,91E+02
10	9	3,25E-01	4,65E-02	6,12E+00	
10	11	1,46E-01	8,95E-03	1,09E+00	
11	11	1,77E+00	2,40E-01	2,95E+01	6,30E+02
11	12	3,39E-01	4,75E-02	6,23E+00	
11	10	1,46E-01	8,95E-03	1,09E+00	
12	12	1,65E+00	2,41E-01	2,96E+01	5,73E+02
12	13	1,98E-01	4,40E-02	5,76E+00	
12	11	3,39E-01	4,75E-02	6,23E+00	
13	13	1,64E+00	2,46E-01	3,03E+01	5,55E+02
13	14	2,95E-01	4,62E-02	6,05E+00	
13	12	1,98E-01	4,40E-02	5,76E+00	
14	14	1,57E+00	2,49E-01	3,06E+01	5,40E+02
14	13	2,95E-01	4,62E-02	6,05E+00	
14	15	2,69E-01	4,63E-02	6,07E+00	
15	15	1,59E+00	2,30E-01	2,82E+01	5,60E+02
15	14	2,69E-01	4,63E-02	6,07E+00	
15	13	1,11E-01	7,06E-03	8,26E-01	
17	17	1,08E+00	1,82E-01	2,16E+01	3,75E+02
17	18	1,12E-01	4,31E-02	5,64E+00	
17	19	4,30E-02	6,17E-03	6,91E-01	
18	18	9,82E-01	2,11E-01	2,56E+01	3,55E+02
18	17	1,12E-01	4,31E-02	5,64E+00	
18	19	1,77E-01	4,38E-02	5,74E+00	
19	19	9,89E-01	1,84E-01	2,18E+01	3,56E+02
19	18	1,77E-01	4,38E-02	5,74E+00	
19	17	4,30E-02	6,17E-03	6,91E-01	

III.7. Conclusion

Through this final chapter we proposed a system behavioral modeling for a predictive analysis of pulling effects in PLLs. For that, we first detailed the basis and the assumptions made for derived the behavioral model. Then, we enunciated the proposed methodology approach proposed based on measurement results, in particular the VCO gain variations, incorporated into macro-models using a Verilog-AMS description of each function blocs of the PLL or into Matlab/Simulink models.

The inductive or capacitive couplings, causes of the working frequency leap functions of the tuning voltage – then the VCO gain non-linearities –, are determined from EM simulations and the coupling amplitude expressed in dB is converted into a coupling coefficient k that can be integrated into spice-like circuit simulations. This method of extraction of coupling coefficient is associated with a derivation of broadband equivalent circuit method for passive circuit. This methodology was applied to a VCO inductance and two coupled transmission lines part of the VCO buffer.

We also proposed a (semi-) analytical approach for spurs description, it appears that pulling effects can be evaluated and represented as AM and FM modulation combination.

The PLL function blocs analysis and predictive behavioral modeling show that every (deliberately or non-deliberately) variation of the PLL parameter has an impact on the pulling effect, but the main cause of spurs apparition is the non linearity of the VCO gain and its peak value, the amplitude and numbers of spurs are more important the more the peak value of K_{VCO}. As well, the more the charge pump current value, the larger the spurs amplitude value. The capacitance value of the PLL loop filter principal effect on the PLL pulling is the frequency-distance of the spurs from the fundamental tone of the PLL output signal, therefore capacitive coupling at the loop filter output or at VCO input impacts on the pulling effects.

Correlation analysis between simulation results and experimental characterizations made on chapter II was carried out and the model derived shows the same trend of pulling variations with the PLL parameters. It was also showed that these pulling issues are not due to the PLL stability. The physical interpretation of the pulling effects are in link with couplings effects inside the IC or at chip-package-PCB level, in particular ground and feeding distribution of sensitive function blocks, that can lead to retroaction of some signal of frequency near to the VCO. This injection of unwanted signal through mechanisms detailed in chapter I into the PLL causes frequency pulling.

Bibliography of Chapter III

[170] M. H. Perrot, M. D. Trott, and C. G. Sodini, “A modeling approach for Σ-Δ fractional-N frequency synthesizer allowing straightforward noise analysis,” IEEE J. Solid-State Circuits, vol. 37, no. 8, pp. 835–844, Aug. 2002.

[171] R. Nonis, N.D. Dalt, P. Palestri, and L. Selmi, “Modeling, design and characterization of a new low jitter analog dual tuning lc-vco pll architecture,” IEEE J. Solid-State Circuits, vol. 40, no. 6, pp. 1303-1309, Jun. 2005.

[172] L. Bizjak, N. Da Dalt, P. Thurner, R. Nonis, P. Palestri, and L. Selmi, “Comprehensive Behavioral Modeling of Conventional and Dual-tuning PLLs”, IEEE Trans. on Circuits and Systems, vol. 55, no. 6, pp. 1628-1638, Jul. 2008.

[173] N. Markuvitz, “Waveguide Handbook “, McGraw- Hill, New York, 1985.

[174] M. Ranaivoniarivo, “Towards Wide-Band Equivalent Circuit Extraction Methodology for Passive Circuits”, Research Master Internship report, Sept.2007.

[175] B. Gustavsen and A. Semleyn, “Rational approximation of frequency domain responses by vector fitting”, IEEE Transactions on Power Delivery, Vol.14, no 3, July 1999.

[176] M. Elzinga, K. L. Virga, L. Zhao, and Jo. L. Prince, “Pole-Residue Formulation for Transient Simulation of High-Frequency Interconnects Using Householder LS Curve-Fitting Techniques”, IEEE Transactions on Advanced Packaging, Vol. 23, no. 2, May 2000.

[177] D. Saraswat, R. Achar, and M. S. Nakhla, “A Fast Algorithm and Practical Considerations for Passive Macromodeling of Measured/Simulated Data”, IEEE Transactions on Advanced Packaging, vol. 27, no. 1, February 2004.

[178] J. C. Rautio, “Synthesis of Compact Lumped Models from Electromagnetic Analysis Results”, TMTT Manuscript, May 2007.

[179] B. Gustavsen, and A. Semlyen, “Enforcing Passivity for Admittance Matrices Approximated by Rational Functions”, IEEE Transactions on power systems, Vol. 16, no. 1, February 2001.

[180] D. Saraswat, R. Achar, , and Michel S. Nakhla, “Global Passivity Enforcement Algorithm for Macromodels of Interconnect Subnetworks Characterized by Tabulated Data”, IEEE Transaction on very large scale integration (VLSI) ,Vol. 13, no. 7, July 2005.

[181] P. Russer, M. Righi, C. Eswarappa and W. J.R. Hoefer, “Lumped Element equivalent circuit parameter Extraction of Distributes Microwave Circuits via TLM Simulation”, IEEE, 1994.

[182] B. Razavi, “Devices and circuits for phase-locked systems,” in Phase- Locking in High-Performance Systems, From Devices to Architectures, B. Razavi, Ed. Piscataway, NJ: IEEE Press, 2003.

[183] G. Alley, "Interdigital Capacitors and Their Application to Lumped-Element Microwave Integrated Circuits," IEEE Trans. MTT-18, December 1970, pp. 1028-1033.

[184] R. Esfandiari, D. Maku and M. Siracusa. "Design of Interdigitated Capacitors and Their Application to Gallium-Arsenide Monolithic Filters," IEEE Trans. MTT, Vol. 31, No. 1, January 1983, pp. 57-64.

[185] M. Ranaivoniarivo, S. Wane, O. Aymard and P. Gamand, “Investigations sur les Phénomènes de Remontée de Composantes Harmoniques dans les Oscillateurs Intégrés “, 16e Journées Nationales Microondes, Mai 2009, Grenoble.

[186] http://www.mathworks.com/help/toolbox/signal/kaiser.html

[187] J. Craninckx and M. Steyaert, “Wireless CMOS Frequency Synthesizer Design”, Kluwer Academic publishers, Boston, 1998, Ch. 7.

[188] D. Banerjee, “PLL Performance”, Simulation and Design, 4th Edition, 2006.

[189] B. Razavi, “RF Transmitter Architectures and Circuits”, IEEE CICC, pp.225-227, 1999

[190] D. Ham, A. Hajimiri, “Concepts and Methods in Optimization of Integrated LC VCOs” IEEE J. Solid State Circuits, vol 36, pp. 896-909, Jun. 2001.

[191] I. Gutiérrez, J. Meléndez, and E. Hernandez, “Design and Characterization of Integrated Varactors for RF Applications”, John Wiley & Sons Ltd, 2006

[192] C. Vaucher and Z. Wag, "A low-power truly-modular I.8GHz programmable divider in standard CMOS technology", Proceedings of the 25th European Solid-State Circuits Conference, 1999. ESSCIRC '99, pp.406409, 1999.

[193] F. M. Gardner, “Phaselock techniques”, 3rd edition, 2005.

[194] B. Razavi, “A study of injection locking and pulling in oscillators,” IEEE J. Solid-State Circuits, vol. 39, no. 9, pp. 1415–1424, Sept. 2004.

[195] P. Maffezzoni, D. D'Amore, "Evaluating Pulling Effects in Oscillators Due to Small-Signal Injection"', IEEE Trans. Computer-Aided Design, vol. 28, no. 1, pp. 22-31, Jan. 2009.

[196] M. Ranaivoniarivo, S. Wane, P.Philippe, O. Aymard and P. Gamand, “System level analysis and experimental characterization of frequency pulling in PLLs”, in Proc. IEEE SofCOM, 2010, pp 370-374,

[197] M. Ranaivoniarivo, S. Wane, E. Richalot and O. Picon, “A System-Level Non-linear Behavioral Modeling of Pulling and Pushing Mechanisms in PLLs”, APCCAS 2010, Dec. 2010, Kuala Lumpur.

[198] S. Wane, J. Mao, G. Fitzgerald, A. Kuo, “Coupled Analysis of Quasi-static and Full-Wave Solution towards IC, Package and Board Co-design”, published in Electrical Performance of Electronic Packaging (EPEP), Atlanta 2007

[199] S. Wane, “Design Flows and Methodologies for Electrical and Thermal Analysis in SiP Applications”, invited Conference at Cadence CDNLive Munchen, Germany May 2007(Collaboration with Optimal/Apache-& Cadence).

[200] S. Wane, and A. Kuo, “Chip-package co-design methodology for global co-simulation of re-distribution layers (RDL), published in Electrical Performance of Electronic Packaging (EPEP), Atlanta 2008 (Collaboration with Optimal-and Apache).

[201] S. Wane, et Al. “Partition and Global Methodologies for IC, Package and Board Co-Simulation In SiP Applications,” presented at European Microwave Week, Munchen October 2007.

[202] S.Wane, and D. Bajon, “Partition-recomposition methodology for accurate electromagnetic analysis 593 of SiP passive circuitry”, in presented at EUROCON 2007, the International Conference on 594 “Computer as a Tool”, 9–12 Sept. 2007, pp. 15–23.

GENERAL CONCLUSION

A. Conclusion

This thesis has been devoted to design methodologies for system-level characterization, modeling and analysis of pulling and pushing effects taking place in PLL systems. Two different real-world carrier applications have been considered for the proposed contribution. The first chip carrier represents a low power transceiver System on Chip (SoC) integrated circuit, working around 868MHz, dedicated to automotive application for secure vehicle immobilization and car access. The second chip carrier is a microwave building blocks down-converter for satellite TV receiver applications. Its function is to convert the antenna signal in range at 10.7-12.75GHz down to a satellite TV IF band in range 950-2150 MHz. While in the automotive carrier application main analysis concerned Transmit path circuits, in the satellite down-converter application focus was on the Receiver path.

The main contributions of this thesis are summarized as follows:

► **On Experimental Characterization of Pulling and pushing effects:**

Experimental characterization of pulling and pushing effects taking place within PLL systems is conducted where influence of Chip, Package, and PCB interactions are taken into account. The experimental characterization underlined importance of the following PLL constitutive circuit elements:

- Influence of VCO nonlinear and frequency dependant gain K_{VCO}
- Impact of varicap devices nonlinear capacitance on VCO and PLL phase-noise
- Effects of PFD block and Charge-Pump circuit on PLL pulling and pushing
- Sensitivity of Power Amplifier matching network and SAW filter functional blocks on Board to pulling and pushing effects.
- Evaluation of PLL robustness against pushing and pulling resulting from injection of power-ground supply noise with variable amplitudes and frequencies.

Through an automotive carrier application, it has been showed that frequency pulling issues, which deteriorate the integrity of the output signal of the IC, can be due to various coupling mechanisms. In order to derive simplified guidelines for first guess assumptions during initial design phases figures of merit are considered. To support the derivation of guidelines and design rules for initial feasibility pre-layout analysis, analytical and semi-analytical approach are developed to describe the spurs constituting pulling and pushing effects. For post-layout analysis and optimization more precise modelling analysis based on a hybrid approach is adopted for investigating root causes of pulling and pushing effects.

► **On the importance of Chip-Package-Board Co-Simulation for Modeling and Analysis of Pulling and Pushing Effects:**

Based on a global divide-and-conquer partitioning methodology rendering accessible to electromagnetic analysis of complex circuits the following aspects have been investigated:

- Effects of VCO inductance architecture on PLL spurs: comparative analysis of 8-shaped inductors topology with traditional Octagonal topology demonstrated an improvement of about 18.5dB.
- Analysis of multi-conductor transmission lines using full-wave simulation analysis for reduced electromagnetic couplings and interferences of active blocs to their embedding environments (based on a multi-port approach).
- Application of Broadband equivalent circuit derivation methodology casting S-parameter models into lumped element models compatible with SPICE-like circuit simulators for Active Analog-Digital and passive Co-Simulation.

The electromagnetic partitioning methodology is combined with dynamic behavioural modelling for predictive analysis of pulling and pushing mechanisms. The proposed hybrid methodology properly captures experimentally observed pulling and pushing effects and

accounts for various nonlinear aspects (non-ideal varicap devices, nonlinearity of the VCO gain, non monotonic influences of PFD and Charge-Pump circuits).

At system level impact of electromagnetic couplings and interferences on pulling and pushing is experimentally evaluated using intentional FIBs for interrupting identified power and ground nets. To assess the effects of intentional FIBs on system level pulling and pushing a figure of merit is introduced which points up importance of electromagnetic couplings and interferences taking place in pulling mechanisms. By lowering couplings and interferences of identified critical power-ground nets, robustness against pulling and pushing is achieved for the design and verification of System-on-Chip carrier applications. Availability of existing design product carrier for low power transceiver working around 868MHz, dedicated to automotive application for secure vehicle immobilization and car access was the basis for further design improvement and guidelines derivations. The proposed analysis methodologies are applied to the design and verification of new product development for satellite down-converter working 10.7-12.75GHz. The designed low cost / low power PLL for Ku-band satellite down-converters has is fabricated in NXP-Semiconductors SiGe: C BiCMOS process. The PLL occupies 0.5mm2 of silicon and draws less than 25mA from 2.7/3.3V supplies. It achieves state-of-art integrated phase noise performance of 1°rms and spurs level below -65dBc.

B. Perceived Limitations and Look-Ahead

Even though the proposed analysis methodologies and experimental characterization of pulling and pushing effects in PLL systems helps in better understanding the underlying physical mechanisms with encouraging correlations between simulation and measurement, the simulation setup procedures remain essentially manual. Since the proposed behavioral modeling analysis involves contribution of all PLL building blocks their transfer function needs to be extracted separately. In addition back-annotation in circuit simulation tools (*e.g., Spectre, ADS, etc*…) of parasitics resulting from EM simulations is not fully automatic and requires adjustment of netlist pinning in accordance to the numbering of ports used during simulations. Such manual procedures can be time consuming and prone to error as well. So perspective of this thesis includes work on automating the aforementioned simulation analysis setup procedures towards better integration with commercial simulators. In addition lack of proper measurement techniques of S-parameters for multi-port systems makes challenging direct correlation of system-level small-signal and large-signal characterization data with simulation results.

APPENDIX

A. Class-E Power Amplifiers

Class-E power amplifiers theory was first introduced by N.O. Sokal and A.D. Sokal in 1975 [203][204] in order to offer a new alternative for highly efficient power amplification. The Class-E is a tuned switching power amplifier that consists of a transistor (or combination of transistors) that is/are driven on and off by an AC input signal to be amplified. The transistor shapes the voltage and current waveforms to prevent simultaneous high voltage and high current in the transistor during the switching transitions from "on" to "off" state. This is made possible through the resonant load network that in addition insures that the voltage across the switch is zero at the end of the off state so that current flow through the switch recommences when there is substantially zero voltage across the switch and that voltage remains substantially zero while current flow through the switch continues. The load network also yields the voltage waveform across the switch to have zero or nearly zero time derivative at the end of the off state as described in the figure below, taken from [203].

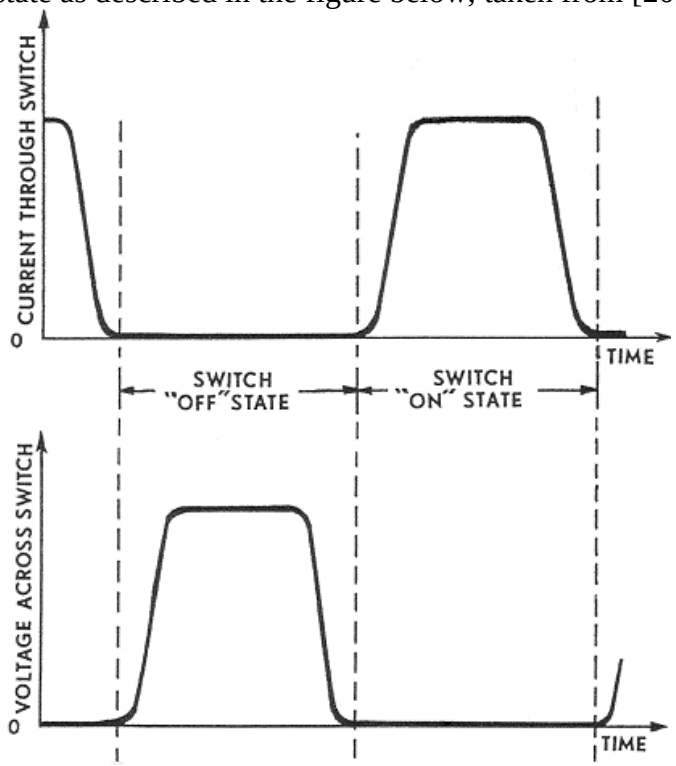


Figure Appendix - 1: Conceptual "target" waveforms of transistor voltage and current.

A.1. Simplified Description & Principles of Class-E Power Amplifier

The transistor of the PA, the key component of the amplifier, is driven by a square wave signal and operates as an on/off switch. The matching/load network of the amplifier is composed by a Co-Ls resonant circuit in series with the final load Rid. The matching network of the PA shapes the current and voltage i_D v_D across the drain / collector of the transistor to prevent maximum amplitude at the same time in order to minimize power dissipation and thus to maximize the efficiency of the PA.

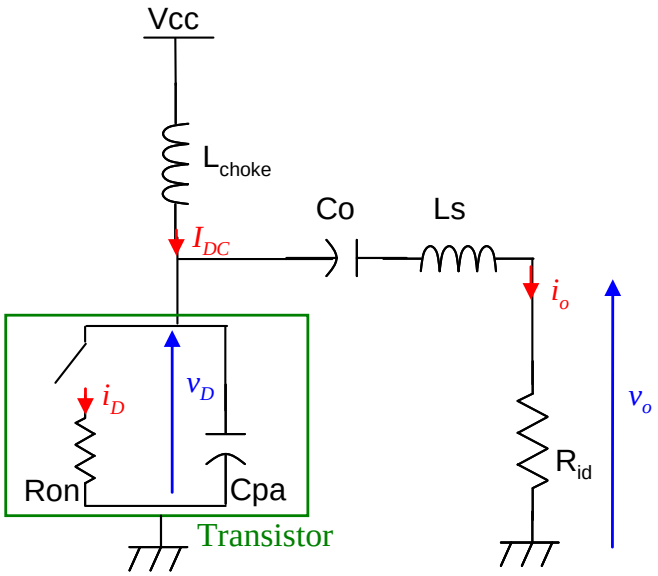


Figure Appendix - 2: Equivalent circuit of a Class-E Power Amplifier

Class E PA operation is achieved when the switch is Off through the transient response of the load network and through the switch current i_D when the transistor is On.

The equivalent circuit of the amplifier and the waveforms of the currents and voltages can be derived from the following assumptions:

- The choke inductance L_{choke} delivers only a DC current I_{DC} and has no series resistance.
- The quality factor of the resonant circuit of the load is large enough to deliver a signal essentially sinusoidal to the load Rid.
- The On/Off transition of the switch is instantaneous and lossless.
- The transistor has a saturation voltage of zero and an infinite Off resistance

In a cycle, $\theta = \omega t$:

- During the "On" mode between $\pi < \theta < 2\pi$, the transistor behaves like a low-resistance Ron. The voltage across the switch is almost zero, I_{DC} is divided between the drain current i_D of the transistor and the current through the load i_o.
- In the "Off" mode, $0 < \theta < \pi$, the transistor is defined by its inherent capacitance Cpa in parallel with the parasitic capacitances. The switch power is zero, I_{DC} is divided between the load current and the current that will charge Cpa.

The network load will depend on the fact that in class E,

- v_D shoud continue to grow when the switch reaches the Off mode
- but when the transistor switches to On mode, v_D must return to zero
- and the slope of v_D when the transistor returns to the On mode should be zero.

A.2. Simplified Analytical Waveforms of Class-E PA Signals

The characteristics of Class-E power amplifiers were mainly developed by F. Raab [206] through steady-state waveforms of the PA. By referring to Figure Appendix - 2, if we consider that at R_{id} terminals the signal is purely sinusoidal,

$$\begin{cases} i_o = \dfrac{c}{R_{id}} \sin(\omega t + \phi) \\ v_o = c \sin(\omega t + \phi) \end{cases} \qquad [0\text{-}1]$$

The amplitude c, the phase φ of the voltage and the load value to present to the adapted PA, R_{id}, should be determined in order to have an ideal class-E PA.

The transistor current follows the next equations:

$$i_D(\omega t) = \begin{cases} Idc - \dfrac{c}{R_{id}}\sin(\omega t + \phi) & \pi < \omega t < 2\pi \\ 0 & 0 < \omega t < \pi \end{cases} \quad [0\text{-}2]$$

The transistor voltage is expressed as:

$$v_D(\omega t) = \begin{cases} \dfrac{1}{\omega \cdot Cpa} \int_{0(+k\times 2\pi)}^{\omega t} \left(Idc - \dfrac{c}{R_{id}}\sin(\theta + \phi) \right) d\theta & 0 < \omega t < \pi \\ Ron \cdot i_D(\omega t) & \pi < \omega t < 2\pi \end{cases} \quad [0\text{-}3]$$

Or:

$$v_D(\omega t) = \begin{cases} \dfrac{1}{\omega \cdot Cpa} \left(Idc(\omega t - k\times 2\pi) + \dfrac{c}{R_{id}}\cos(\omega t + \phi) - \dfrac{c}{R_{id}}\cos(\phi) \right) \\ Ron \cdot \left(Idc - \dfrac{c}{R_{id}}\sin(\omega t + \phi) \right) \end{cases} \quad [0\text{-}4]$$

For determining the unknown parameters $I_{DC,}$ c, R_{id} and φ, we assume that:

- The switch will operate at a 50% time on « On » state and, 50% on "Off" state
- Cpa, the capacitance of the transistor is considered to be linear
- The switch resistance in Off mode is infinite, i_D is null during this period
- When the switch reaches the On mode, $v_D(\theta=\pi)=0$; $i_D(\theta=\pi)=0$
- and $\frac{dv_D}{dt}\big|_{\theta=\pi} = 0$ when the switch topple to the On mode.

Equations [0-1] and [0-4] permit to give, when the PA is an ideal switch, for Ron=0:

$$\tan(\varphi) = \frac{2}{\pi} \quad [0\text{-}5]$$

$$Idc = Vcc \cdot \pi \cdot \omega \cdot Cpa \quad [0\text{-}6]$$

$$\frac{c}{Rid} = \sqrt{\frac{\pi^2}{4} + 1} \times Vcc \cdot \pi \cdot \omega \cdot Cpa \quad [0\text{-}7]$$

and

$$c = \frac{2Vcc}{\sqrt{\frac{\pi^2}{4} + 1}} \quad [0\text{-}8]$$

with

$$Rid = \frac{2}{\left(\frac{\pi^2}{4} + 1\right)\pi \cdot \omega \cdot Cpa} \quad [0\text{-}9]$$

For the physical character of the transistor involving Ron nonzero: we get the following relations:

$$\tan(\varphi) = -\frac{2}{\pi} \quad [0\text{-}10]$$

$$Idc = \frac{Vcc}{\frac{1}{\pi \cdot \omega \cdot Cpa} + Ron} \quad [0\text{-}11]$$

$$\frac{c}{Rid} = \sqrt{\frac{\pi^2}{4}+1} \times \frac{Vcc}{\frac{1}{\pi \cdot \omega \cdot Cpa} + Ron} \qquad [0\text{-}12]$$

Equation [0-8] becomes

$$c = \frac{2Vcc}{\sqrt{\frac{\pi^2}{4}+1}} \left(1 - \frac{Ron}{\frac{1}{\pi \cdot \omega \cdot Ron \cdot Cpa} + Ron} \left(\frac{7}{4} + \frac{\pi^2}{16} \right) \right) \qquad [0\text{-}13]$$

And the load to be presented to the adapted PA should be:

$$Rid = \left(\frac{1}{\pi \cdot \omega \cdot Cpa} - Ron\left(\frac{3}{4} + \frac{\pi^2}{16} \right) \right) \cdot \frac{2}{\frac{\pi^2}{4}+1} \qquad [0\text{-}14]$$

By taking the LoPSTer example, with Vcc = 1.5V, a half off time of 50%, if we consider that the switch is open when $0<\omega t<\pi$, with a working frequency of 868MHz we get the following data and waveforms:

- *Ideal (in dashed green data in the figure below)*: the datasheet of the circuit defined Ron=10Ohms, Ceff=1.4224pF. By the presence of Ron, the class E PA is lossy. The waveform of the current of the amplifier i_D is derived through equation [0-2], the load current from i_0 of equation [0-1], the collector voltage from equation [0-3] v_D, and finally the load voltage waveform is obtained by using the equation [0-1] v_0.
- *Implemented with Spectre (blue line in the following figure)*: from equivalent circuit calculation of the PA circuit implemented, we have Ron=35.3Ohms, Ceff=1.03224pF.

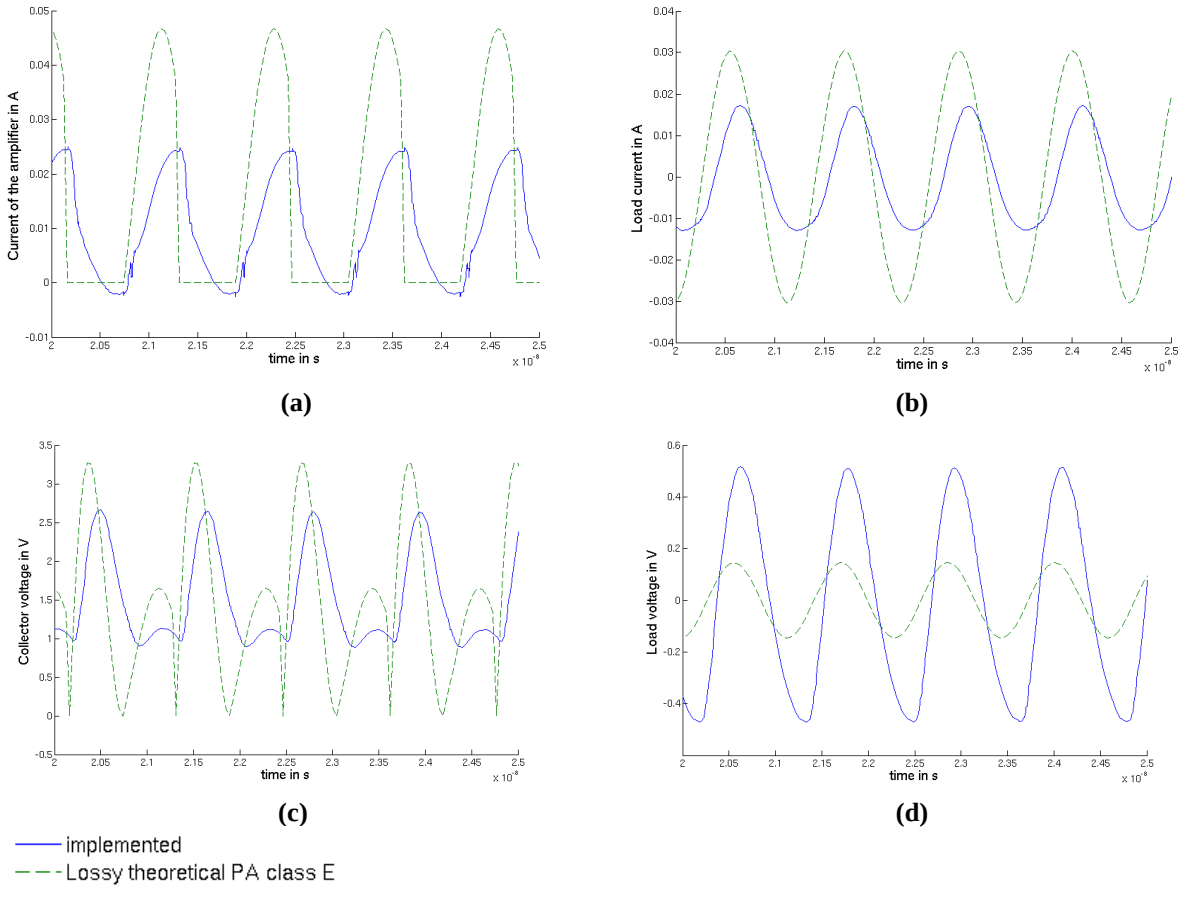


Figure Appendix - 3: Waveforms obtained by transient analysis or analytical derivation of a class-E PA

Amplitude difference between the simulation result of the implemented circuit and the theoretical calculation of the lossy PA class E is mainly due to Ron difference.

With the component values defined (ideal or implemented with Spectre):

- Pout theoretical ideal =16dBm
- Pout theoretical with losses = 7.86 dBm
- Pout measured ~ 10dBm
- Pout from Spectre simulation = 5.75 dBm

Some power dissipations are not taken into consideration for the theoretical computation of Pout for a Class-E PA as the simulation and measurements results shows, among others they can be due to:

- The rise/fall time of the square input signal and the commutation of the transistor that can affect the charge/discharge of Cbeff then the aspect of the current through the amplifier Figure Appendix - 3 (a)
- A constant saturation voltage between the transistor collector to emitter during saturation that reduces the excursion of the collector voltage and then the load voltage Figure Appendix - 3 (c)
- The load voltage which was considered in 1st order as a pure sinusoid, whereas the curves Figure Appendix - 3 (b) and (d) show that the Q factor of the Class-E matching circuit is not high enough
- The wirings of the design that can introduce power dissipation

To complete the estimation of losses, these effects of dissipation should be taken into account [207].

A.3. Spectrum of Class-E PA

As the transistor of the class-E PA is operating in switching mode, the direct output of the active part of the PA will have a spectrum with non negligible harmonics at $n \times f_0$, with n integer. However, depending how the resonant circuit of the matching is restrictive, the signal to be transmitted to the final load should have negligible harmonics.

For the example given in the previous paragraph, we obtain the following spectrum:

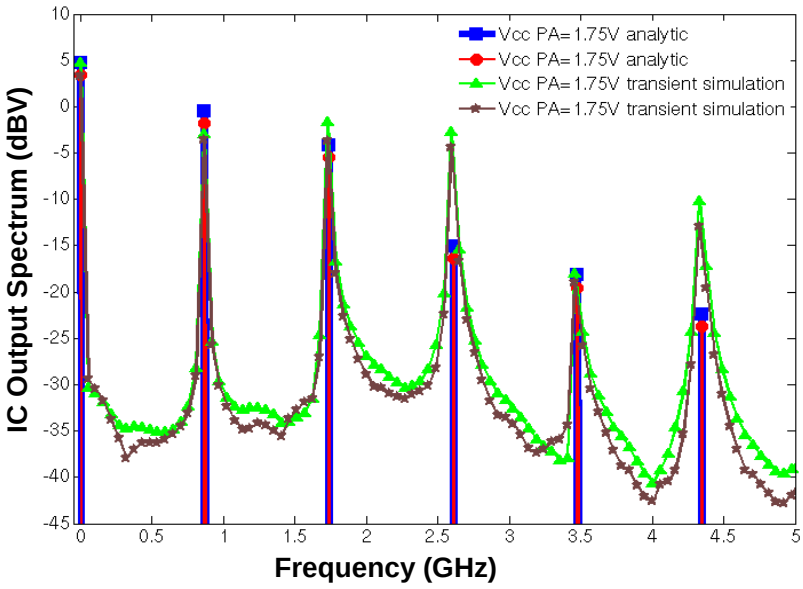


Figure Appendix - 4: Spectrum of the output PA class-E transistor obtained by transient analysis or analytical derivation, functions of the DC supply of the PA

B. De-Embedding Technique

In order to perform simulations and measurements, ports – a two terminals with one arbitrarily designated as the "signal," the other assigned as the "ground"- are used to excite the circuit and evaluate the result [208]. The "reference plane" of the measurement or simulation – where the measurement system ends and the DUT begins - should be exactly defined. For on-wafer measurements, the probe tips are usually the initial reference plane; the calibration of the measuring device is the process to get the results at the probe tips.

However to have access to the DUT, it is often necessary to integrate some transmission lines that connect the DUT to the pads access, then the source. For measurements structures, GSG or SG (Signal-Ground-Signal or Signal-Ground) signal probe pads are inserted for probes contacts. These added metallizations (pads and lines) induce parasitics (sheet resistance, inductance, capacitance to substrate …), discontinuities and substrate coupling that should be removed, de-embedded.

The de-embedding technique, which includes the calibration of the measurement tools in this chapter, is a mathematical process that removes the effects of unwanted effects of fixtures or wafer probes included in the measured data by subtracting their contribution.

B.1. De-Embedding the Effect of Local Ground Planes for Internal Ports in EM Analysis

In simulations, the port model is an ideal generator with an internal impedance most often at 50Ω but can also be tuneable and permit to deliver the dependent S-parameters.

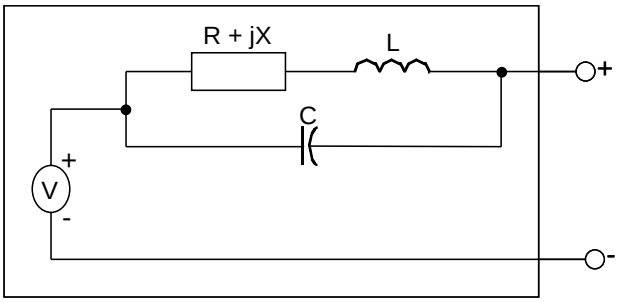


Figure Appendix - 5: Example of Sonnet port model

However, ports can introduce discontinuities and the excitation is brought to the DUT usually through transmission lines. De-embedding process permit to calculate and remove the port discontinuity, to remove the transmission lines effects from the analysis results if reference planes are defined [209].

The difficulties of simulations de-embedding generally come from internal ports introduction (sometimes it is not feasible to insert transmission lines and move the reference plane) in particular to access to the defined global ground, or also to de-embed the coupling among a group of ports. Each EM simulation tool has its own port and de-embedding definition [210][211][212].

B.2. Calibration and De-Embedding for RF Measurements

a. Calibration Techniques: Correction of Parasitics up to Probe Plane

Most common RF measurements involve Network Analyzer in order to evaluate the characteristics of the device under test (DUT) through its S-parameters (in amplitude and phase), then the gain, return loss, and reflection coefficient (…). However with a Vector Network Analyzer (VNA), the cables and the probes introduce systematic errors that can be modelled by a bidirectional eight-term error model or error port adapters given in the figure below. To compute, determine and remove these unknown error terms from the measurements results, calibration procedure called vector error correction is required using known standards.

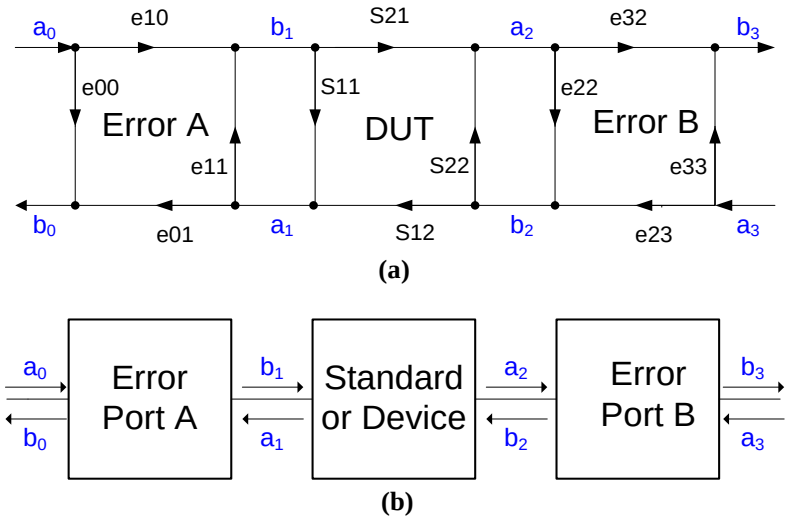


Figure Appendix - 6: Error model for a vector network analyzer: (a) S-parameter representation model of error and (b) error matrices

The procedure consists in finding the S-parameters or more precisely the T-parameters of the error Port A/B matrices of Figure Appendix - 6 through the measurements of standards. As the T-parameters of the un-calibrated device can be written as:

$$T_M = T_A \cdot T_{DUD} \cdot T_B \qquad [0\text{-}15]$$

where T_M represents the measured total T-matrix, T_{DUT} the actual T-matrix of the DUT and T_A and T_B are the virtual error box T-matrices. Once the T-parameters of the virtual error matrices determined, the next step of the calibration consists in removing the error matrices as:

$$T_{DUT} = T_A^{-1} \cdot T_M \cdot T_B^{-1} \qquad [0\text{-}16]$$

NB: The T-parameters of the T-matrix are defined as:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \cdot \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \qquad [0\text{-}17]$$

The calibration technique then depends on the standards types used: Through, Reflect (Short or Open), Match (Load), Line, Attenuation…
The principal calibration techniques used in the industries are:

The TRL method

The technique is based on a three standards (thru-short-delay) first proposed in [214] and developed in [215]. The three standards are: a through connection, a high reflectivity termination (a perfect short in [214]), and a section of uniform line. The TRL calibration

method uses the characteristic impedance of a length of transmission line to set the reference impedance.

The TRL calibration procedure consists of measuring the scattering matrices for the three standards which gives three known scattering matrices, $S_{Through}$, $S_{Reflection}$, and S_{Delay}, containing 10 terms ($S_{12Reflection}$ and $S_{21Reflection}$ are set equal to zero). With these measurements, the eight terms of the two error matrices, S_A and S_B are found by converting all of the measured S-matrices, $S_{Through}$, $S_{Reflection}$, and S_{Delay}, into T-matrices, $T_{Through}$, $T_{Reflection}$, and T_{Delay}, the T-matrix for the through connection and the one for the delay line (of characteristic *impedance*. Z0 known) connection can be respectively represented by:

$$\mathbf{T_{Through}=T_A \cdot T_B} \qquad [0\text{-}18]$$

$$T_{Delay} = T_A \cdot \begin{bmatrix} e^{-\gamma l} & 0 \\ 0 & e^{-\gamma l} \end{bmatrix} \cdot T_B \qquad [0\text{-}19]$$

where γ and l denote the propagation constant and length of the transmission line standard.

Solving the equations derived leads to the error parameters.

The TRL method uses simple and easily realizable standards, however this approach have some limitations since the limitation of the insertion phase of the line may lead to long lengths at lower frequencies [216]. In addition, with the dispersion in coplanar waveguide and microstrip lines, change of Z0 of the line must be considered.

The SOLT and SOLR methods

The most common used calibration, the SOLT technique [217], uses three impedance (short, open, load) and one transmission (thru) standards that must be accurately defined. The SOLT standards can be modelled with simple lumped elements: open-circuit capacitance, short-circuit inductance, load inductance, and thru delay (and loss).

The error port terms are determined from the one-port Short- Open-Load standard measurements and the thru is used to calculate the port match and transmission terms.

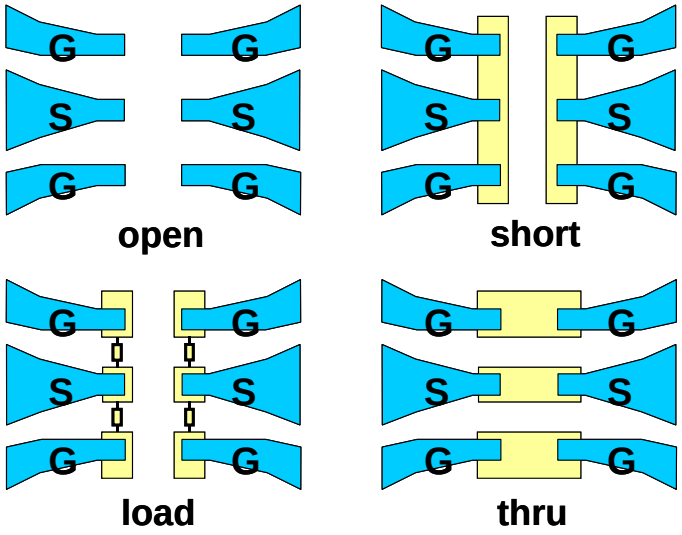


Figure Appendix - 7: Short –Open (probes in air) -Load-Thru calibration configurations for on wafer measurements

For orthogonal probing, a variation of the SOLT calibration, the SOLR – Short-Open-Load-Reciprocal [219] is used. This method is similar to the SOLT calibration for one-port corrections, except that the thru standard (that needs not to be ideal) has an imperative to be reciprocal ($S_{12}=S_{21}$) [218]. However, the SOLR algorithm requires special software (e.g.

Cascade Microtech's WinCal) communicating with the VNA for the SOLR algorithm calculation.

SOLT/SOLR calibration are widely used but the method can over-determined set of equations as the number of measurements and standard definitions exceeds the number of unknowns in the two port error model that may lead to non-single entirely self-consistent solution.

The LRM and LRRM methods

The LRM method [220] is similar to the TRL method, except that a perfect match (50 ohm load) on each VNA port is substituted for the TRL line standard. The standards are then a non-zero length Thru (line), a Reflect, and a couple of Match (matched load).

Both match standards are assumed to be perfect, and thus represents a line of infinite length. Since those requirements are not fulfilled in practice (small variation of the load resistance, misalignment between resistive material and metal pattern..) , LRM calibration accuracy is reduced.

The LRM method then uses fewer standards than the SOLT method, thus the opportunity for errors resulting from imperfect standard definition (notably for the broadband load) and improper probe placement are minimized [220].

An improvement of the LRM technique is presented in [221] and mathematically developed in [222]. The Line-Reflect-Reflect-Match (LRRM) uses a line, two reflects (short and open, not necessarily known), and only one match as standards. The match needs to be measured on only one of the two ports, this, avoiding problems due to asymmetries. In addition, the use of open and short for reflect standards diametrically opposite in the smith chart facilitate the computation of the reflect standards.

The LRM method can be viewed as being the special case of the LRRM method for which the match is chosen as one of the reflect standards.

As the LRM calibration technique provide better accuracy than SOLT and TRL [216], for broadband calibration (e.g. until 110GHz at NXP) the improvement of the LRM: the LRRM calibration technique will be used.

b. De-embedding Techniques: Correction of Parasitics from Probe Plane to Intrinsic DUT

Once the calibration of the measurement tools done, the measurement reference plane is at the probe tip. However, the parasitics due to the pads, the transmission lines access and also the discontinuities are measured with the device response.

The Probe Pads Structures

To prevent the signal pads from coupling to the substrate and to palliate the ground parasitics, shield-based test fixtures are used [223], [224] : the signal pad is isolated from substrate and the forward coupling is reduced (see Figure Appendix - 8 (c) compared to Figure Appendix - 8 (b)). In addition, the equivalent circuit of the pad parasitics is pure capacitive which simplifies the pad de-embedding and noise measurements.

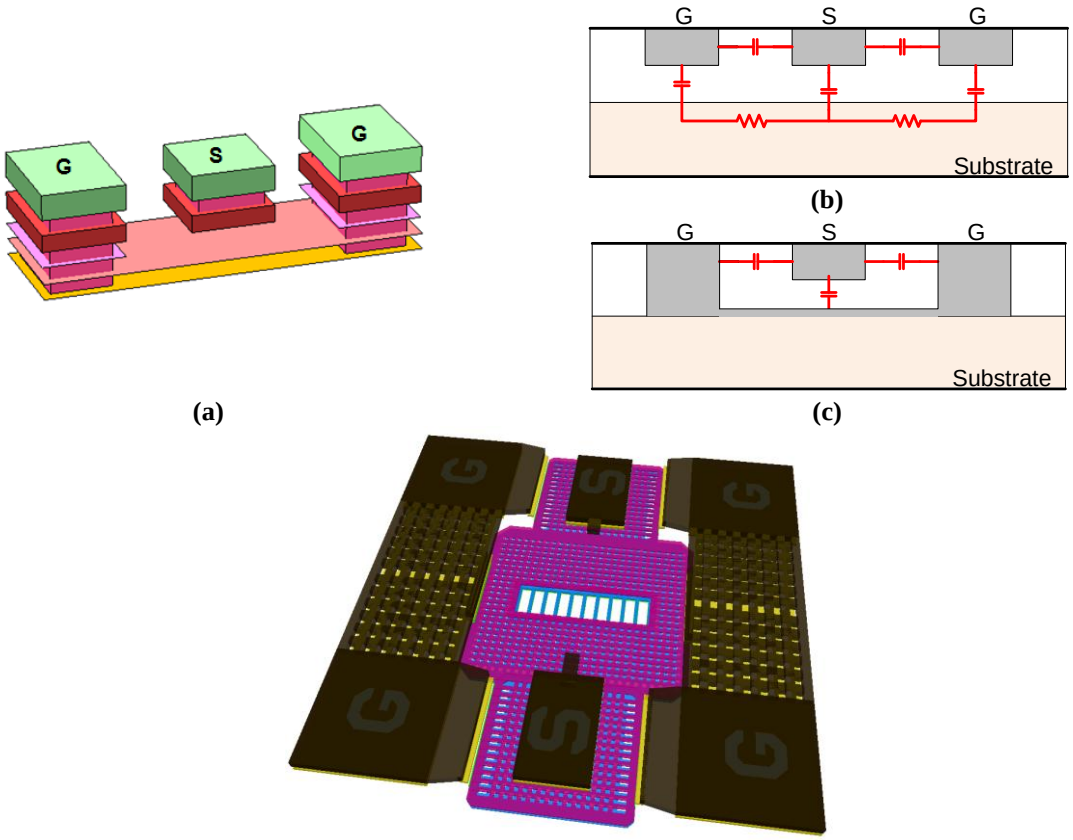


Figure Appendix - 8: Ground shielded G-S-G probing pads with thick top metal layers (a), side view of unshielded (b) and shielded (c) pad-port and its parasitics, and shield-based GSG test fixtures for a 2-port measurements of 10 active devices in parallel (d)

The ground plane (shielding) is in metal 1 or metal 1 + metal 2. The ring around the devices in Figure Appendix - 8 (d) also permits an accurate ground connection for the DUT and the underlying substrate.

De-embedding methodologies based on equivalent circuit

In order to get the DUT response from measurement, the parasitics must be removed. For that, the dummy patterns are fabricated on the same wafer and should be carefully designed to reproduce and subtract the extrinsic parasitics of a fixture device.

Some de-embedding techniques are based on lumped equivalent-circuit models. These physical equivalent-circuit models consist of probe-pad and interconnect parasitics connected in parallel-series configurations. After subtracting the parasitic components in admittance and impedance domains, the impacts of unwanted parasitics on device characterization can be substantially reduced.

► The Short-Open-Load-Thru and Derivatives De-embedding method

- **The Open-Short De-embedding method**

Two principal Open-Short de-embedding methods can be described in the literature. In the first derived by Koolen etal [225] where the interconnections lead to 2 main contributions:

- Parallel components (Y1, Y2, and Y3 in red in Figure Appendix - 9) mostly capacitive, forming a PI circuit, are determined with an Open dummy
- Series inductive and resistive components forming a T circuit (Z1, Z2, and Z3 in blue in Figure Appendix - 9), are determined using a Short dummy.

The DUT own Y-parameters are then obtained from the next equation:

$$Y_{OpenShort} = \left(\left(Y_{DUT} - Y_{open}\right)^{-1} - \left(Y_{short} - Y_{open}\right)^{-1}\right)^{-1} \quad [0\text{-}20]$$

where Y_{open} denotes the two-port admittance parameters measured on the "open" dummy structure and Y_{short} denotes the two-port impedance parameters measured on the "short" dummy structure.

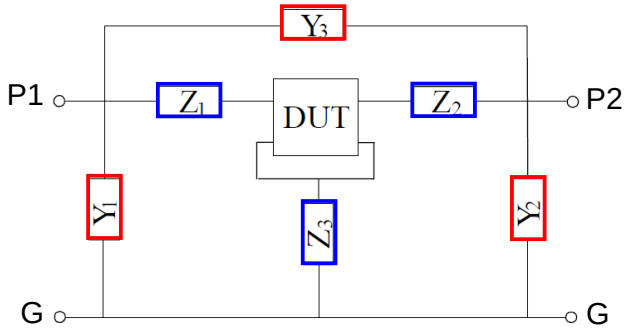


Figure Appendix - 9: Koolen' small signal equivalent circuit with parasitic admittances and impedances

To shift the reference plane to the DUT plane, another short-open de-embedding technique is also possible and described in [226]. The method considers an equivalent circuit found with an open and a short dummy structure as in Figure Appendix - 10 and follows this procedure:

(i) Subtract the input and output impedance Zi, short of the series impedance found with the short dummy structure from the measured input and output impedances (Z11 and Z22)

(ii) Convert the resulting Z-parameters into Y-parameters: Y'

(iii) Subtract Yp=1/(Zi, open – Zi, short) to the input/output admittances of Y', with Zi the impedance due to the open dummy.

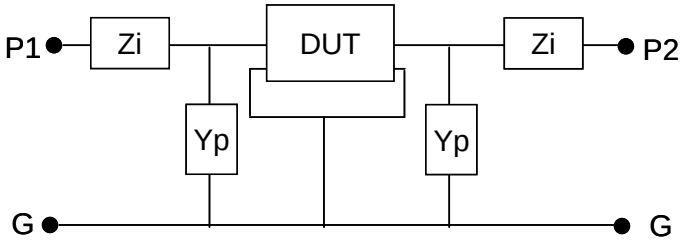


Figure Appendix - 10: Equivalent circuit model built-on Π-network for de-embedding measurement results

The Open-Short de-embedding technique that we used during our test-structures design and measurement is a simple method to implement and is widely used for de-embedding of passive back-end devices (above the first metallization layer). Nevertheless, for accurate evaluation of on-chip devices, this standard de-embedding technique may not be sufficient at high (mm-wave) frequencies.

- **Three-Step Parasitic De-embedding method**

The three-step de-embedding approach developed in [228] and mathematically detailed in [227] is based on a four port model parasitic (see Figure Appendix - 11(a)) introduced in [231] where the extrinsic and intrinsic ports (respectively the ports of the measured DUT and the intrinsic device ports) are related through a 4×4 Y-matrix:

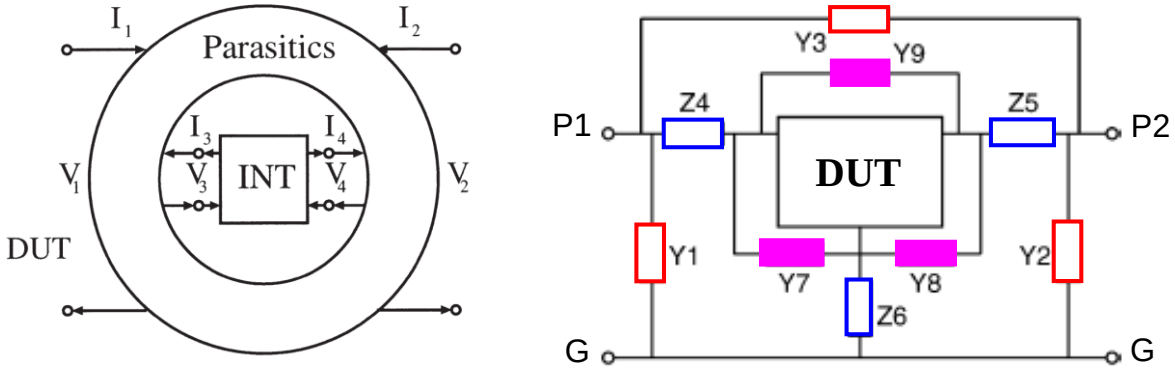
$$\begin{pmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{pmatrix} \cdot \begin{pmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{pmatrix} \qquad [0\text{-}21]$$

By defining Ve and Ie as the extrinsic voltage and current vectors, Vi and Ii the intrinsic voltage and current vectors, equation [0-21] can be re-written as:

$$\begin{pmatrix} Ie \\ Ii \end{pmatrix} = \begin{pmatrix} Yee & Yei \\ Yie & Yii \end{pmatrix} \cdot \begin{pmatrix} Ve \\ Vi \end{pmatrix} \qquad [0\text{-}22]$$

Where Yee, Yei, Yie, Yii are 2×2 matrices. It comes that the Y-parameter of the measured DUT Y^{DUT} and the intrinsic Y-parameter Y^{INT} of the device relation is [227][230]:

$$Y^{DUT} = Yee - Yei \cdot \left(Y^{INT} + Yii\right)^{-1} \cdot Yie \qquad [0\text{-}23]$$



(a) **(b)**

Figure Appendix - 11: The general four-port description of the parasitics to be de-embedded (a) and equivalent circuit with parasitic admittances and impedances assumed in the three-step de-embedding method

In the three-step de-embedding approach, nine unknown impedances/admittances are assumed for the parasitics as seen in Figure Appendix - 11 (b). To determine the parasitics admittances of the equivalent circuit related to the unknown sub-matrices of equation [0-22], the open-short dummies are no more sufficient due to the add of Y7, Y8 and Y9. For that, a "pad" [227] or a "load" [227][230] dummies, or another set of open and short dummies [229] are necessary to complete the de-embedding.

Introduction of the pad structure as an additional dummy (which only contains the probe pads) is widely used for passive DUTs [227] and Open1-Short1-Opend2 (dedicated)-Short2 dummies are used for parallel actives RF structures [229] to de-embed the stack of top-down metal layers interconnections of the device fingers contact to the signal transmission line/ pad that may induce non negligible parasitics capacitances. Including a "load" dummy structure can provide benefits on the de-embedding method [230], but only if its impedance is accurate [227] which is difficult to achieve in a IC process with polysilicon resistors that have reactive parts coming from the inductance and self-capacitance non negligible in high frequencies.

De-embedding methodologies based on line theory

In order to de-embed the transition effects, methodologies based on line theory can be used. Based on the fact that the transitions and the DUT are cascaded, by determining the T-parameters of the transitions parts (pads + lines), the intrinsic T-parameters of the device can be extracted.

For that, as for the line-based calibration techniques, different configuration of lines introduced between the 2 signal ports creating some delay, reflect or through are used, and by determining the characteristics of the lines (propagation constant, impedance characteristic), the scattering parameters of the transitions can be obtained [232].

De-embedding method based on line theory such as TRL [233], LRRM [222], L-2L [234], can be very interesting as the dummies variation are captured in all the frequency range of measurement, and this de-embedding technique also permits to reduce the number of dummies for important device scaling, however for having optimal lines length, the dummies can be cumbersome due to its length.

De-embedding methodology for floating ground references

The existing de-embedding algorithms are generally based on a general ground reference assumption and fail to deal with local ground references. In addition the double-delay hypothesis can be difficult to fulfil because of higher order effects and numerical error control issues with hyperbolic functions. To circumvent such problems a homographic transformation is introduced for an accurate multi-standard de-embedding methodology discussed in [244] suitable for local ground references. Figure Appendix - 12 shows a general unsymmetrical Trellis equivalent circuit topology where the effects of excitation sources/measurement probing are represented by a two-port system composed of 3 parameters: a series impedance (Z_{Series}), a parallel impedance (Z_{Shunt}) and a transformer (of ratio n).

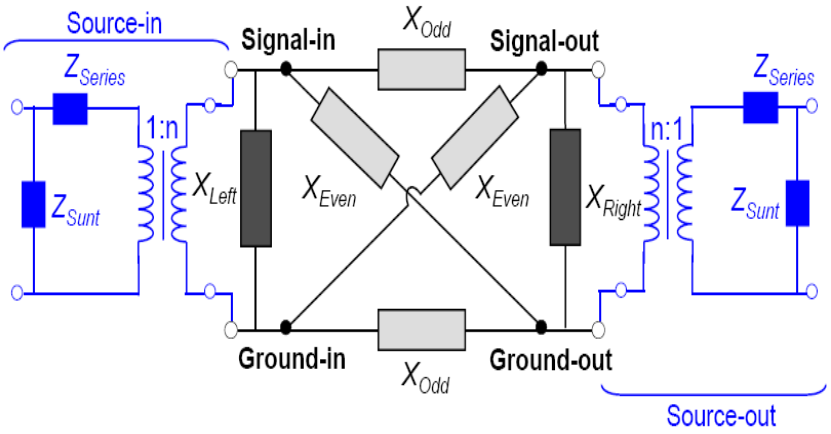


Figure Appendix - 12: Combined left-compensated and right-compensated Trellis equivalent circuit topology with de-embedding modules.

The input impedance seen from the input-source (source-in) when the DUT and the output source are replaced by a load impedance is given by the following relation:

$$Z_{in} = Z_{Shunt} - Z_{Shunt}^2\left(Z_{Series} + Z_{Shunt} + n^2 Z_{Load}\right)^{-1} \qquad [0\text{-}24]$$
$$= \alpha + \beta\left(\eta\, Z_{Load} + 1\right)^{-1}$$

Taking 3 canonical different lengths l=3λg/8, l=λg/4, and l=λg/2 for which the expression of the input impedance in (6) is straightforward when the load impedance is identified to a transmission line, gives the following relations for the homographic parameters α, β and η:

$$\alpha = Z_{Shunt}\ ,\ \beta = \frac{-Z_{Shunt}^2}{\left(Z_{Series} + Z_{Shunt}\right)}, \eta = \frac{n^2}{\left(Z_{Series} + Z_{Shunt}\right)} \qquad [0\text{-}25]$$

Design languages are used to describe or model a circuit. Two principals kind of languages are usually used: Textual description or Algorithmic description of a data transformation. To derive our methodology, we used each kind of language: Verilog/Verilog-a/Verilog-AMS description language and MATLAB models.

C. Verilog, Verilog-A, Verilog-AMS Languages

C.1. Overview, Description, Functionality of Verilog, Verilog-A, Verilog-AMS

Verilog [240] is a Hardware Description Language used to describe, model electronic circuits and systems.The language is used in the design, verification, and implementation of analog, digital and mixed-signal circuits/chips at the register transfer level (RTL) of abstraction and can be used for verification of analog and mixed-signal circuits through simulation, for timing analysis, testability analysis and logic synthesis.

Verilog-AMS [241][242] is an analog and mixed signal extension to the Verilog language using continuous-time simulator and event-driven modeling semantics (Verilog/SystemVerilog/VHDL use event-based simulator loops) using a top-level design methodology as well as the traditional bottom up approaches. Differential equations are solved in analog-domain, then analog, mixed and digital can be described and simulated together, for example analog events can trigger digital actions and vice versa.

Verilog-A [243] is an industry standard modeling hardware description language for analog components/circuits, also derived from the IEEE 1364 Verilog HDL specification. The behavior of each module can be described mathematically in terms of its terminals and external parameters applied to the module. The structure of each component can be described in terms of interconnected sub-components.

```
module nand_gate(vin1, vin2, vout)
   (vlogic_high, vlogic_low, vtrans, tdel, trise, tfall)
node [V, I] vin1, vin2, vout;
// voltage level for ‘1’, ‘0’ and treshold
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans = 1.4;
 // square signal features (time delay, rise and fall time)
parameter real tdel = 2u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);
{
   real vout_val;
   integer logic1, logic2;

// comparison of vin1 and vin2 signals data
   initial {
      if (vlogic_high < vlogic_low) {
         $error("Range specification error.  vlogic_high = (%E) less than vlogic_low = (%E).\n", vlogic_high, vlogic_low );
      }
      if (vtrans > vlogic_high || vtrans < vlogic_low) {
         $warning("Inconsistent $threshold specification w/logic family.\n");
      }
   }

   analog {
      logic1 = V(vin1) > vtrans;
      logic2 = V(vin2) > vtrans;

      if ($threshold(V(vin1) - vtrans, 1))  logic1 = 1;
      if ($threshold(V(vin1) - vtrans, -1)) logic1 = 0;

      if ($threshold(V(vin2) - vtrans, 1))  logic2 = 1;
      if ($threshold(V(vin2) - vtrans, -1)) logic2 = 0;

// define the logic function and assigning vout value
     vout_val = !(logic1 && logic2) ? vlogic_high : vlogic_low;

      V(vout) <- $transition( vout_val, tdel, trise, tfall);
   }
}
```

Figure Appendix - 13: Example of an HDL description of a NAND gate

```
module nand_gate(vin1, vin2, vout);
input vin1, vin2;
output vout;
electrical vin1, vin2, vout;
// voltage level for ‘1’, ‘0’ and treshold
parameter real vlogic_high = 5;
parameter real vlogic_low = 0;
parameter real vtrans = 1.4;
// square signal features (time delay, rise and fall time)
parameter real tdel = 2u from [0:inf);
parameter real trise = 1u from (0:inf);
parameter real tfall = 1u from (0:inf);

  real vout_val;
  integer logic1, logic2;

// comparison of vin1 and vin2 signals data
  analog begin

    @ ( initial_step ) begin
          if (vlogic_high < vlogic_low) begin
            $display("Range specification error.  vlogic_high = (%E) less than vlogic_low = (%E).\n", vlogic_high, vlogic_low );
            $finish;
          end
          if (vtrans > vlogic_high || vtrans < vlogic_low) begin
            $display("Inconsistent $threshold specification w/logic family.\n");
          end
    end

    logic1 = V(vin1) > vtrans;
    logic2 = V(vin2) > vtrans;

    @ (cross(V(vin1) - vtrans, 1))  logic1 = 1;
    @ (cross(V(vin1) - vtrans, -1)) logic1 = 0;

    @ (cross(V(vin2) - vtrans, 1))  logic2 = 1;
    @ (cross(V(vin2) - vtrans, -1)) logic2 = 0;

// define the logic function.
    vout_val = !(logic1 && logic2) ? vlogic_high : vlogic_low;

    V(vout) <+ transition( vout_val, tdel, trise, tfall);
  end
endmodule
```

Figure Appendix - 14 : Example of a Verilog-A description of a NAND gate

C.2. Implementation of a PLL with a Verilog-AMS code

To implement a fast simulating PLL circuit using Virtuoso-Spectre as given in Figure III.5-6, we developed some Verilog/Verilog-AMS instances describing each sub-function block of a PLL that can be used for the analysis.

a. The Phase- Frequency Detector

```
//Verilog-AMS HDL for "MyPLL_Lopst", "PFD" "verilogams"

`include "constants.vams"
`include "disciplines.vams"

module PFD ( Do_pump, Up_pump, clk_ref, clk_vco_div, One );

  input One;
  inout Up_pump;
  inout clk_vco_div;
  inout clk_ref;
  inout Do_pump;

  electrical Do_pump, Up_pump, clk_ref, clk_vco_div, One ;
  integer tempA, tempB;
  real QA, QB;

  electrical RST;
  real R;

parameter real vp = 1.8 ;
parameter real vth = 0.9 ;
parameter real tr = 2.5e-10 ;
parameter real tf = 4e-10 ;
parameter real td = 2.1e-10 ;
parameter real delai = 2.1e-09 ; // 3.1ns ou 2.1ns
parameter real v0 = 0 ;

analog begin

        @(initial_step) begin  // initialization, all at 0
          tempA=0;
          tempB=0;
          QA=0;
          QB=0;
          R=0;
        end

        @(cross(V(clk_ref)-vth , +1))
          tempA=1;


        @(cross(V(clk_vco_div)-vth , +1))
          tempB=1;


        if (tempA && tempB)  R=vp; else R=v0;  // Reset (porte AND et reset de la bascule DQ non inversee


        @(cross(V(RST)-vth , +1)) begin
          tempA=0;
          tempB=0;
        end

        if (tempA) QA=vp; else QA=v0;
        if (tempB) QB=vp; else QB=v0;

        V(Up_pump) <+ transition(QA, td, tr,tf);
        V(Do_pump) <+ transition(QB, td, tr,tf);
        V(RST) <+ transition(R, delai,tr,tf);

end
endmodule
```

Figure Appendix - 15: Verilog-AMS code of a PFD

b. The Charge-Pump

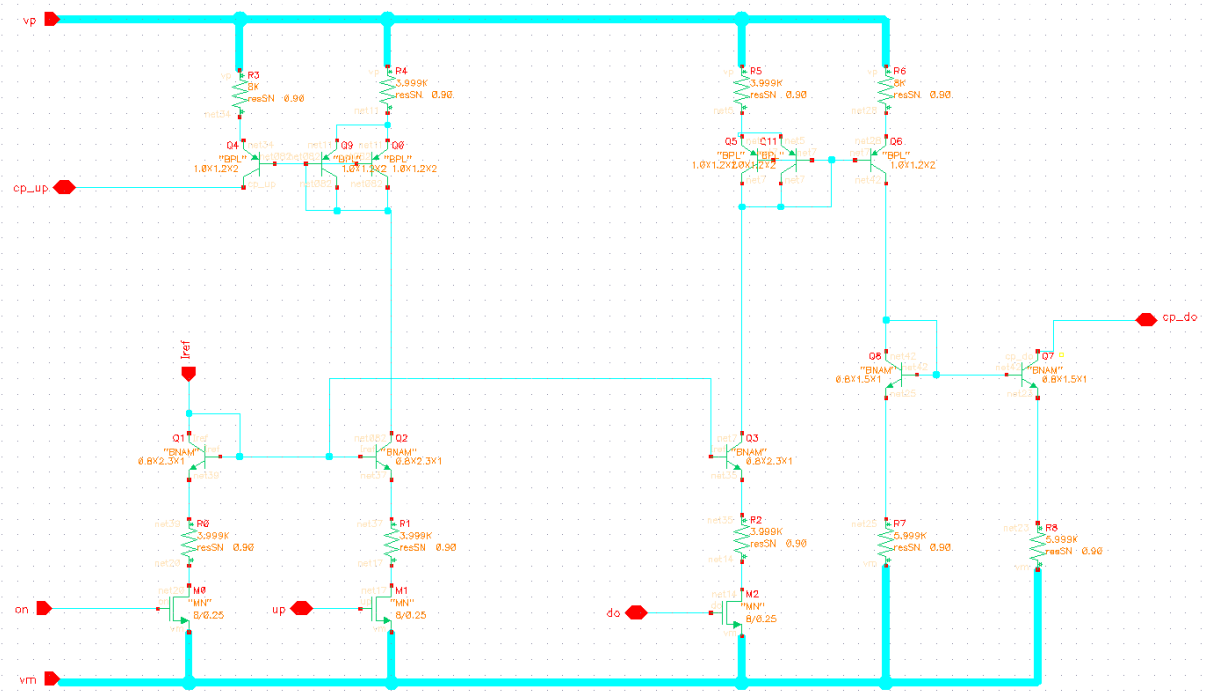


Figure Appendix - 16: Example of a transistor level Charge-Pump

```
//Verilog-AMS HDL for "MyPLL_Lopst", "CP_ICP2" "verilogams"

`include "constants.vams"
`include "disciplines.vams"

module CP_ICP2 ( cp_do, cp_up, do, up, Iref, on, vm, vp );

  input on;
  input vm;
  inout do;
  input vp;
  inout up;
  inout cp_do;
  input Iref;
  inout cp_up;
   electrical  cp_do, cp_up, do, up, Iref, on, vm, vp;

  parameter real vth=0.9;
  real temp_do;
  real temp_up;

analog begin


        if (V(on) >=  vth)
          if (V(up)>=vth)
            temp_up =  -I(Iref)/2;
          else
            temp_up = 0;
        else
          temp_up = 0;


        if (V(on) >=  vth)
          if (V(do)>=vth)
            temp_do =  I(Iref)/2;
          else
            temp_do = 0;
        else
           temp_do = 0;



        I(cp_do)<+ transition(temp_do,0.05e-9, 0.01e-9, 0.01e-9);
        I(cp_up)<+ transition(temp_up,0.05e-9, 0.01e-9, 0.01e-9);

end


endmodule
```

Figure Appendix - 17: Verilog-AMS code of a CP

c. The Voltage Controlled Oscillator

```
//Verilog-AMS HDL for "MyPLL_Lopst", "VCO" "verilogams"

`include "constants.vams"
`include "disciplines.vams"
`include "constants.h"
`include "discipline.h"

module VCO ( outn, outp, Gnd_tail, VTune, Vcc_tank );

  output outp;
  input VTune;
  input Gnd_tail;
  output outn;
  input Vcc_tank;

  electrical outn, outp, Gnd_tail, VTune, Vcc_tank;

  parameter real Kvco = 30e6;   // in Hz/V  =15MHz/V if ICP_4=60uA, =30MHz/V if ICP_2=30uA
  parameter real A0 = 1;        // in V    =1.07 if Kvco=30MHz/V (ICP2), =0.942 if Kvco=15MHz/V (ICP4)
  parameter real fi = 5e6;  // in Hz   =1.722e9 if Kvco=30e6, =1.453e9 if Kvco=15e6
  parameter real Vp = 1.8;
  parameter integer steps_per_period = 50;


  real phase_init;       //   wc*time component of phase
  real phase_nonlin;    //   the idt(k*f(t)) of phase
  real inst_freq;

analog begin

  phase_init = 2*`M_PI*fi*$abstime();   // when Vtune=0
  phase_nonlin =  2*`M_PI*Kvco*idt( V(VTune),0);

  V(outp) <+ Vp+A0*sin(phase_init + phase_nonlin);
  V(outn) <+ Vp+A0*sin(phase_init + phase_nonlin + `M_PI);

  inst_freq = phase_init + phase_nonlin;
  $bound_step (1 / (steps_per_period*fi));  //inst_freq

 end


endmodule
```

Figure Appendix - 18: Verilog-AMS code of a VCO

d. The Divider by N

```
//Verilog-AMS HDL for "MyPLL_Lopst", "Div_N" "verilogams"

`include "constants.vams"
`include "disciplines.vams"

module Div_N (Sig_IN, Sig_OUT_sinus, Sig_OUT_square );
input Sig_IN;
output Sig_OUT_sinus, Sig_OUT_square;
electrical Sig_IN, Sig_OUT_sinus, Sig_OUT_square;

parameter real vp=1.8; // Offset Sig_IN !
parameter real vm=0;
parameter real vth=0.9;

parameter real tt = 0.01n;
parameter real td = 0.001n;

parameter real N=3;  // Division

real cross_nm,cross_np, T, f;
real tempvar;
analog begin
        @(initial_step) begin
          T=0;

        end

        @(cross(V(Sig_IN)- vp, +1) ) begin
          cross_nm=cross_np; // ! Sig_IN seuil @ vp

        end

        cross_np=last_crossing(V(Sig_IN)-vp, +1);
        T=cross_np-cross_nm;
        f=1/T;

        V(Sig_OUT_sinus) <+ vp+sin(2*`M_PI*f/N*$abstime());


         if (V(Sig_OUT_sinus) > vp)
          tempvar=vp;
          else
          tempvar=vm;
        V(Sig_OUT_square)<+ transition(tempvar,td,tt);


end

endmodule
```

Figure Appendix - 19: Verilog-AMS code of a Divider

D. Matlab-Simulink Description

D.1. Overview, Description, Functionality of Matlab-Simulink

Matlab-Simulink® is a high-level programming language of technical computing and interactive environment for algorithm development, data visualization, data analysis and numeric computation developed by the MathWorks [235].To summarize, Simulink is a time base software package which can solve Ordinary Differential Equations (ODE) numerically. As all DE, especially the non-linear one, do not necessarily have an analytical solution, numerical solution can be useful. Indeed, Simulink permit to break the ODE into small times segments and to calculate the solution numerically for only a small segment, a step size. But since the method is numerical and not analytical there will be an error in the solution that will depend on the specific method and step size used.

In order to reproduce the electrical behavior of some functions blocks of the PLL, an extension of Simulink® is used for modeling and simulating the generation, transmission, distribution, and consumption of electrical power: the SimPowerSystems^{TM} library [236] where electrical sources, parallel or series RLC branches (…) are available.

D.2. Implementation of a PLL under VCO pulling with Matlab-Simulink

Our PLL design presented in Figure III.5.4 described in Simulink® model was based on the demo proposed by Matlab's charge-pump PLL Demo [237] where each function block of the PLL given in Chapter III.4 are described as precisely as possible.

- The **Reference** is defined as a Sine Wave or a Pulse Generator taken from the Sources library. The important parameters are the frequency or the period of the output signal and its phase that should be set to the same value of the crystal parameters.
- The **Phase - Frequency Detector** is based on Simulink extras D-Flip Flops; the delay necessary for the phase comparison is obtained by an Integer Delay function block corresponding to one sample period.

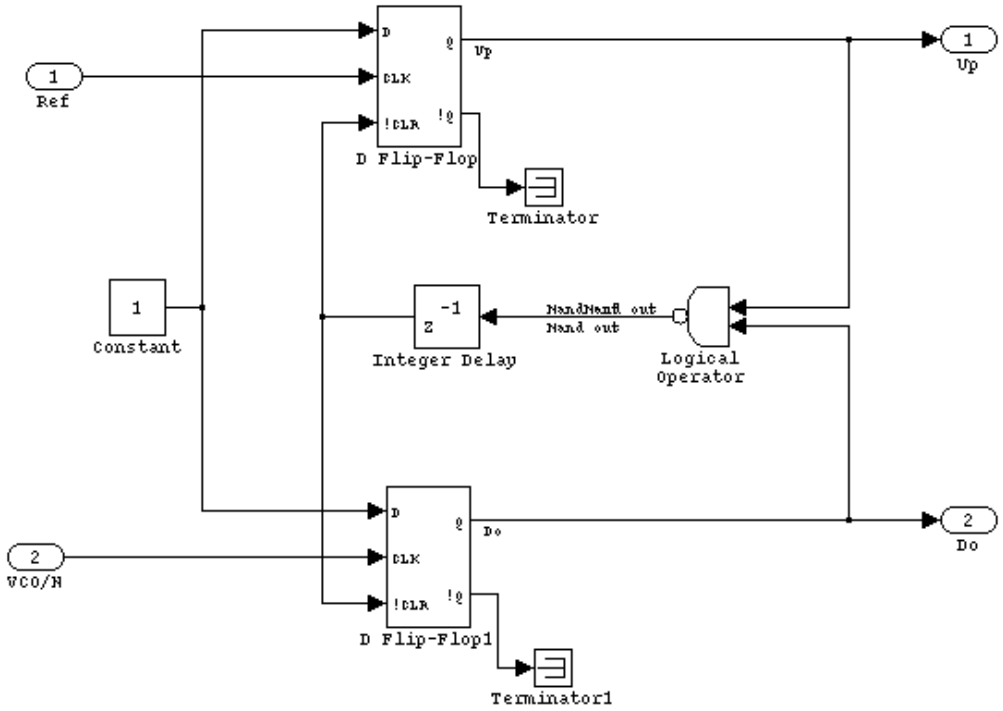
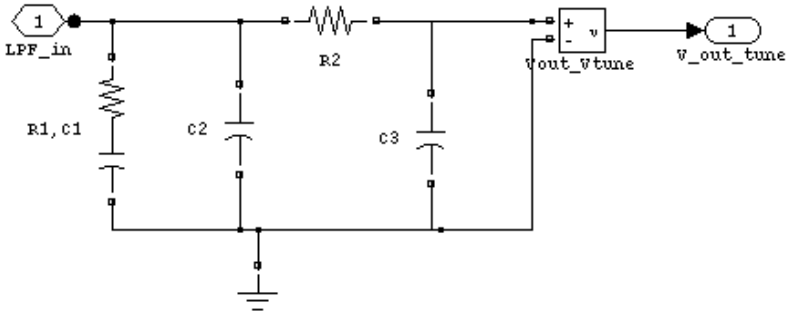


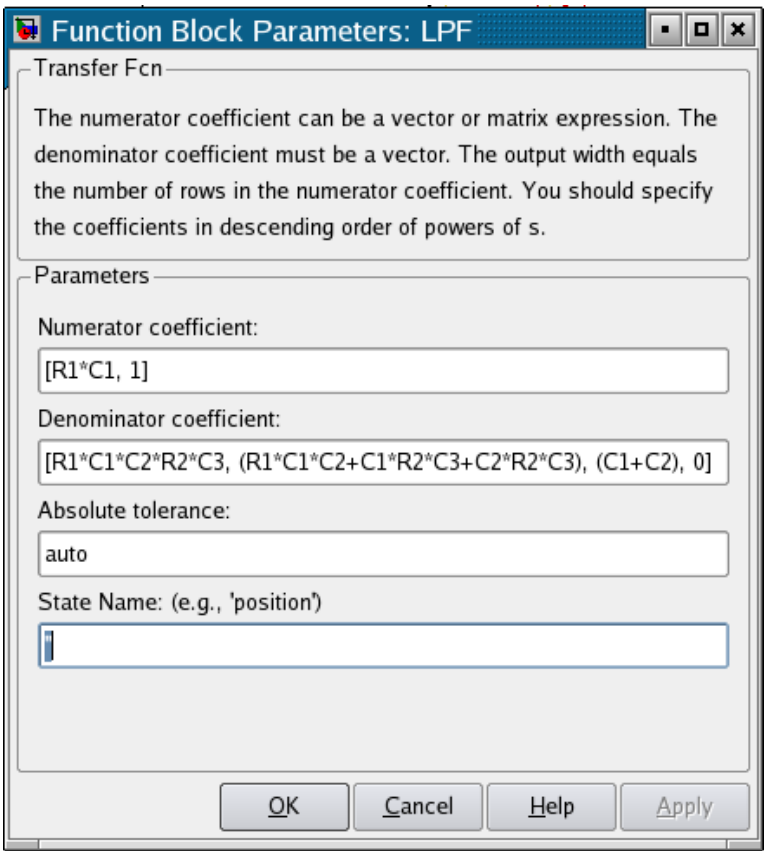
Figure Appendix - 20: PFD subsystem implemented with Simulink

- The C**harge Pump** can be implemented as the same way that the electrical circuit given in Figure III.4-3 by using electrical elements from the SimPowSystem blockset or just by converting the boolean data output of the PFD into a double format data multiplied by the ICP value. The up and down converted data are then added and converted into a current through a Controlled Current Source also available through the SimPowerSystems library.
- The L**ow Pass Loop Filter** can be directly also designed using Parallel or Series RLC Branch as given in Figure III.4-6 if the input data is a current, but the loop filter can also be defined by its mathematical transfer function. For example for a 3rd order passive loop filter, the transfer function of the filter given in the following equation:

$$\frac{Vout(p)}{Iin(p)} \approx \frac{p \cdot R1 \cdot C1 + 1}{p \cdot (C1 + C2) \cdot \left(p \cdot \frac{P1 \cdot C1 \cdot C2}{C1 + C2} + 1 \right) \cdot (p \cdot R2 \cdot C3 + 1)} \quad , p = j\omega \qquad [0\text{-}26]$$



(a)



(b)

Figure Appendix - 21: 3rd order RC low pass loop filter (a) and its transfer function described with Simulink (b)

- For modeling **the Voltage Controlled Oscillator**, The first step consists in capturing the VCO gain ($K_{VCO} = \frac{\Delta f}{\Delta Vcont}$) in a numerical equation such rational function [238] or by dividing the curve $f_{RF} = f(Vcont)$ into n sub-bands where the slope K_{VCO} of the function f is assumed frequency dependant [239]. For having the data in phase domain, the voltage controlled frequency obtained is integrated.
- To model the Divider, a gain of 1/N is used before converting the data into a sinusoidal function whose frequency and phase will be compared to the reference.

Bibliography of Appendix

[203] N. O. Sokal and A. D. Sokal, “Class E - A New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers,” IEEE Journal of Solid-State Circuits, Vol SC-10, No. 3, pp 168-176, June 1975.

[204] N. O. Sokal and A. D. Sokal, "High-efficiency tuned switching power amplifier," U. S. Patent 3,919,656, Nov. 11, 1975.

[205] Nathan O. Sokal, “Class-E RF Power Amplifiers”, QEX, Jan/Feb 2001, pp. 9-20.

[206] F. H. Raab, "Idealized operation of the Class E tuned power amplifier," IEEE Trans. Circuits and Systems, vol. CAS-24, no. 12, pp. 725-735, Dec. 1977.

[207] F. H. Raab and N. O. Sokal, "Transistor power losses in the Class E tuned power amplifier," IEEE J. Solid-State Circuits, vol. SC-13, no. 6, pp. 912-914, Dec. 1978.

[208] Daniel G. Swanson, Jr. and Wolfgang J.R. Hoefer “Microwave Circuit Modeling Using Electromagnetic Field Simulation” copyright 2003 Artech House, ISBN 1-58053-308-6, pp. 173.

[209] “Sonnet User’s Guide”, v. 11.52, pp. 97

[210] J. C. Rautio, “Deembedding the effect of a local ground plane in electromagnetic analysis,” IEEE Transactions on Microwave Theory and Techniques, Vol. 53, pp. 770–776, Feb. 2005.

[211] J. C. Rautio, “Perfectly calibrated internal ports in EM analysis of planar circuits,” in IEEE MTT-S IMS Digest, (Atlanta, GA), THP1D-01, June 2008.

[212] http://www.ece.uci.edu/eceware/ads_docs/mom/index.html (Chapter 4: Ports).

[213] R. A. Hackborn, “An automatic network analyzer system,” Microwave J., pp. 45–52, May 1968.

[214] N. R. Franzen and R. A. Speciale, “A new procedure for system calibration and error removal in automated S-parameter measurements,” in Proc. 5th Eur. Microwave Conf., Hamburg, Germany, Sept. 1-4, 1975, pp. 69–73.

[215] G. F. Engen and C. A. Hoer, “Thru-reflect-line: An improved technique for calibrating the dual six port automatic network analyzer,” IEEE Trans. Microwave Theory Tech., vol. 27, no. 12, pp. 987–993, Dec. 1979.

[216] A. Davidson, E. Strid, K. Jones, “Achieving greater on-wafer S-parameter accuracy with the LRM calibration technique”, ARFTG Conference Digest-Winter, 34th, Ft. Lauderdale, FL, USA, Nov. 1989, pp. 61 – 66

[217] “On-wafer vector network analyzer calibration and measurements” , Cascade Microtech, Inc. , Application note.

[218] Andrea Ferrero, “Two-port network analyzer calibration using an unknown ‘thru’ ,” IEEE Microwave and Guided Wave Letters, vol. 2, No. 12, Dec 1992, pp 505-507.

[219] S. Basu and L. Hayden, “an SOLR calibration for accurate measurement of orthogonal on – wafer DUTs”, Cascade Microtech, Inc.

[220] A. Davidson, E. Strid, and K. Jones. “Achieving greater on-wafer S-parameter accuracy with the LRM calibration technique.” /€€E ARf TG Digesf Dec.. 1989.

[221] A. Davidson, K. Jones, and E. Strid, “LRM and LRRM calibrations with automatic determination of load inductance,” in 36th ARTFG Conf. Dig., Nov. 1990, pp. 57–63.

[222] F. Purroy and L. Pradell, “New theoretical analysis of the LRRM calibration technique for vector network analyzers,” IEEE Trans. Instrum. Meas., vol. 50, no. 5, pp. 1307–1314, Oct. 2001.

[223] T. E. Kolding, “Shield-based microwave on-wafer device measurements,” IEEE Trans. Microw. Theory Tech., vol. 49, no. 6, pp. 1039–1044, Jun. 2001.

[224] A. Aktas and M. Ismail, “Pad De-Embedding in RF CMOS”, IEEE Circuits and. Devices Magazine, vol.17, no. 3, pp. 8-11, May 2001.

[225] M.C.A.M. Koolen, J.A.M Geelen and M.P.J.G. Versleijen, “An Improved De-Embedding Technique for On-Wafer High-Frequency Characterization,” in Proc. BCTM 1991, pp. 188–191.

[226] S. A. Wartenberg, “Rf Measurements Of Die And Packages”, Artech House, Incorporated, May 2002.

[227] L. F. Tiemeijer, R. J. Havens, A. B. M. Jansman, and Y. Bouttement, “Comparison of the “Pad-Open-Short” and “Open-Short-Load” deembedding techniques for accurate On-Wafer RF characterization of High-Quality passives,” IEEE Transactions on Microwave Theory and Techniques, vol. 53, no. 2, Feb. 2005.

[228] L. F. Tiemeijer and R. J. Havens, “A calibrated lumped-element de-embedding technique for on-wafer RF characterization of high-quality inductors and high-speed transistors,” IEEE Trans. Electron Devices, vol. 50, no. 3, pp. 822–829, Mar. 2003.

[229] L. F. Tiemeijer, “De-embedding of parallel RF-MOSFET structures”, Philips Research internal presentation.

[230] Luuk F. Tiemeijer, Ralf M. T. Pijper, J. Anne van Steenwijk, and Edwin van der Heijden, “A New 12-Term Open–Short–Load De- mbedding Method for Accurate On-Wafer Characterization of RF MOSFET Structures”, IEEE Transactions on Microwave Theory and Techniques, vol.58, no. 2, Feb. 2010.

[231] Q. Liang, J. D. Cressler, G. Niu, Y. Lu, G. Freeman, D. C. Ahlgren, R. M. Malladi, K. Newton, and D. L. Harame, “A simple four-port parasitic deembedding methodology for high-frequency scattering parameter and noise characterization of SiGe HBTs,” IEEE Trans. Microw. Theory Tech., vol. 51, no. 11, pp. 2165–2174, Nov. 2003.

[232] L. Martoglio, “Etude et caractérisation de lignes microbandes inversées sur verre et silicium utilisant une technologie de type Mems : Synthèse de fonctions micro-ondes dans la bande Ka“, PhD report, Université de Marne la Vallée, France, 2005.

[233] C. H. Chen and M. J. Deen, “A general noise and S-parameter de-embedding procedure for on-wafer high-frequency noise measurements of MOSFETs,” IEEE Trans. Microw. Theory Tech., vol. 49, no. 5, pp. 1004–1005, May 2001.

[234] Johansen, T. K., C. Jiang, D. Hadziabdic, and V. Krozer, “EM simulation accuracy enhance-ment for broadband modeling of on-wafer passive components," European Microwave Conference, Munich, Oct.2007.

[235] http://www.mathworks.com/products/matlab/

[236] http://www.mathworks.com/products/simpower/

[237] http://www.mathworks.com/matlabcentral/fx_files/14868/1/content/html/plldemo.html

[238] M. Ranaivoniarivo, S. Wane, P. Philippe, O. Aymard and P. Gamand, “System Level Analysis and Experimental Characterization of Frequency Pulling in PLLs”, SoftCOM 2010, Sept. 2010, Split.

[239] M. Ranaivoniarivo, S. Wane, E. Richalot and O. Picon, “A System-Level Non-linear Behavioral Modelling of Pulling and Pushing Mechanisms in PLLs”, APCCAS 2010, Dec. 2010, Kuala Lumpur.

[240] « IEEE Standard Verilog® Hardware Description Language », IEEE Std 1364-2001

[241] http://www.eda.org/twiki/bin/view.cgi/Verilog-AMS

[242] I. Miller and T. Cassagnes, "Verilog-AMS Eases Mixed Mode Signal Simulation," Technical Proceedings of the 2000 International Conference on Modeling and Simulation of Microsystems, pp. 305-308

[243] « Verilog-A Language Reference Manual », Open Verilog International, v.1.0, August 1, 1999.

[244] S.Wane, and D. Bajon, “Broadband equivalent circuit extraction methodology with deembedding of floating ground references”, in European Microwave Conference, EuMC, pp: 1078 – 1081, 2009.

RÉSUMÉ :

MODÉLISATION, CARACTÉRISATION ET ANALYSE DE SYSTÈMES DE PLL INTEGRÉS, UTILISANT UNE APPROCHE GLOBALE PUCE-BOITIER-CIRCUIT IMPRIMÉ

Terminologie

AM: *Amplitude Modulation*, Modulation d'Amplitudes
AMS: *Analog / Mixed Signal,* signal analogique / mixte
AC : *Alternating Current*
BBS: *Broadband Spice*
CP: *Charge Pump*
DC: *Direct Current*
DRC: *Design Rule Check*
DTI : *Deep Trench Isolation*
DUT: *Device Under Test*, composent en essai
EM: ElectroMagnétique, ElectroMagnétisme
ESD: *ElectroStaticDdischarge*, Décharge Electro-Statiques
FIB: *Focused ion Beam*
FM: *Frequency Modulation,* Modulation de Fréquences
G-S-G: *Groud-Signal-Ground,* masse-signal-masse
HB: *Harmonic Balance*
HDL/VHDL: ***(****VHSIC) Hardware Description Language,* langage de description de matériel
HF: Hautes Fréquences
IC: *Integrated Circuit*, Circuit Intégré
ICP: courant de Charge-Pump
K_{VCO}: gain du VCO
LNA: *Low Noise Amplifier,* amplificateur à faible bruit
LNB: *Low Noise Block-*(*downconverter)*
NFC : *Near Field Communication*, communication en champ proche
PA : *Power Amplifier*, Amplificateur de Puissance
PCB: *Printed Circuit Board,* circuit imprimé
PFD: *Phase Frequency Detector*, détecteur de Phase et de Fréquence
PLL: *Phase Locked Loop,* boucle à verrouillage de phase
PM: *Phase Modulation,* Modulation de Phase
RF : Radio Fréquence
RX: Communication en mode réception
SAW: *Surface Acoustic Wave* filter, filtre à onde acoustique de surface
SiP: *System in Package*
SoC: *System on Chip*
TX: Communication en mode transmission
VCO: *Voltage Controlled Oscillator*, oscillateur contrôlé en tension
Verilog-A: language de modélisation analogique
Zin: Impédance d'entrée

I. Motivation, Contexte et Challenges

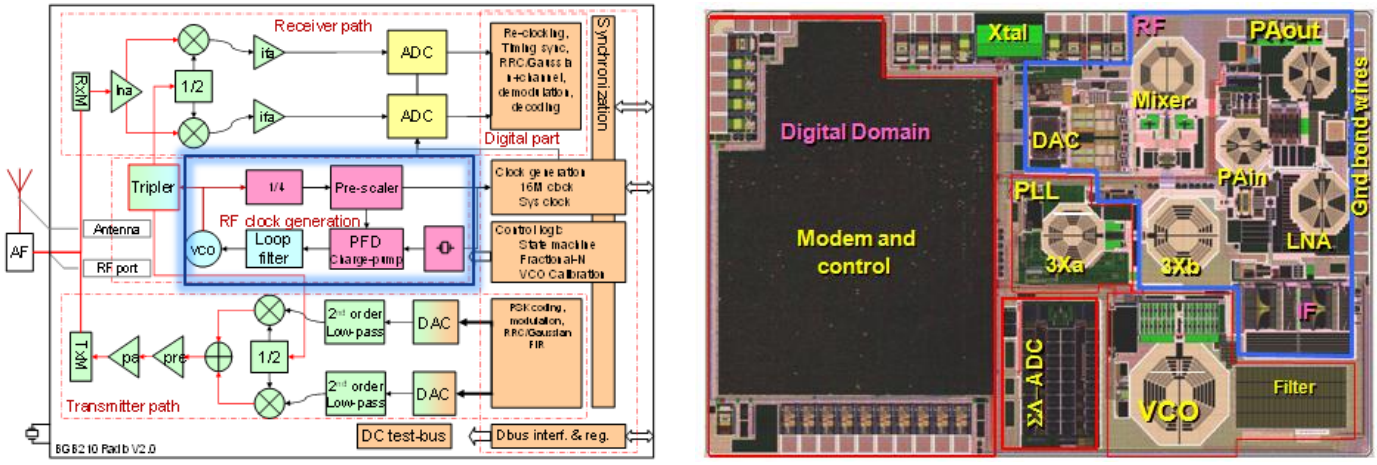
I.1. Evolution Objets Nomades et Multistandard

La tendance actuelle des applications électroniques se tourne vers les objets nomades communicants, qui convergent vers des applications mobiles tels les GPS, NFC, etc… Ils nécessitent plus de fonctionnalités, mais doivent utiliser une puissance de fonctionnement moindre.

Ces applications sont de plus en plus multi-modes, multistandards. Or leur intégration doit se faire à faible coût ; D'où l'utilisation de solutions d'intégration RF SoC (System on Chip).

I.2. Les PLL: Composants Essentiels dans une Puce

Pour ces types de puces à vocation mobiles, les PLL (Boucle à Verrouillage de Phase) représentent des composants essentiels. L'exemple ci-après représente un circuit bluetooth développé par NXP.



(a) **(b)**

Figure 1: Représentation électrique (a) et layout (b) d'une application bluetooth (Projet BGB210 EDR Radio, Collaboration NXP-Caen/Eindhoven).

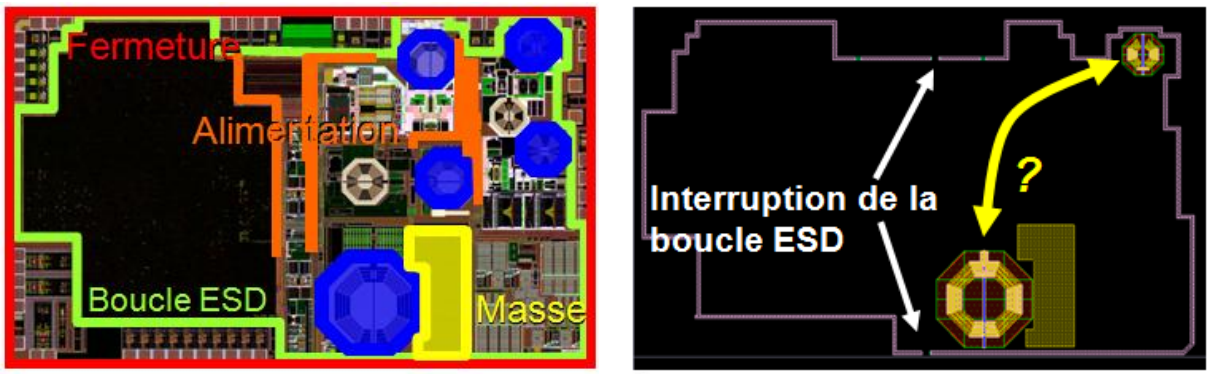
Les défis posés par L'intégration des PLL nécessitent une approche globale pour la prise en compte des différents mécanismes de couplages et d'interférences

I.3. Couplage Indirect et Direct

a. Couplage Indirect

A travers le couplage indirect, nous voulons souligner l'importance des lignes d'alimentation, des boucles de retour de courant et le besoin d'une estimation rapide de ces interactions concernant le couplage entre 2 composants définis.

Pour cela, prenons l'exemple du couplage entre deux inductances boucles et les effets du couplage indirect sur celles-ci.



(a) (b)

Figure 2: Simplification du layout de l'application bluetooth en vue de l'étude du couplage indirect entre deux inductances boucles

L'interruption de la boucle ESD a un effet significatif sur les performances de l'isolation. En effet, nous pouvons voir que le couplage entre les 2 composants diminue lorsqu'on interrompt la boucle ESD entourant le circuit.

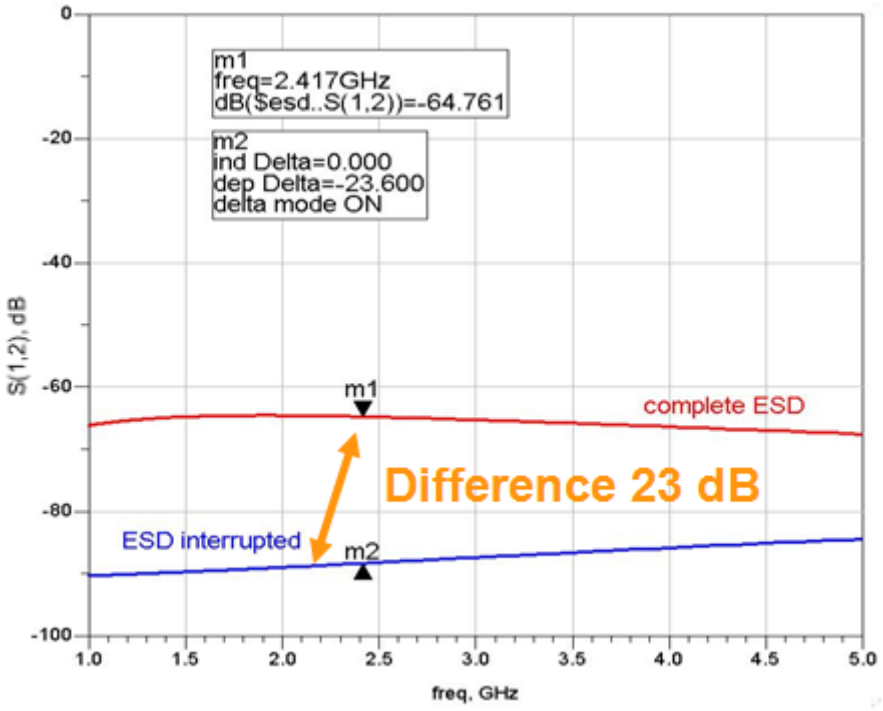


Figure 3: Résultat de simulation pour le couplage entre deux inductances prenant en compte l'interruption ou non de la boucle ESD .

b. Couplage direct

Pour notre application Bluetooth, trois implémentations au niveau du placement-routage (Floorplan) permettent de noter l'impact des choix topologiques sur les performances du circuit.

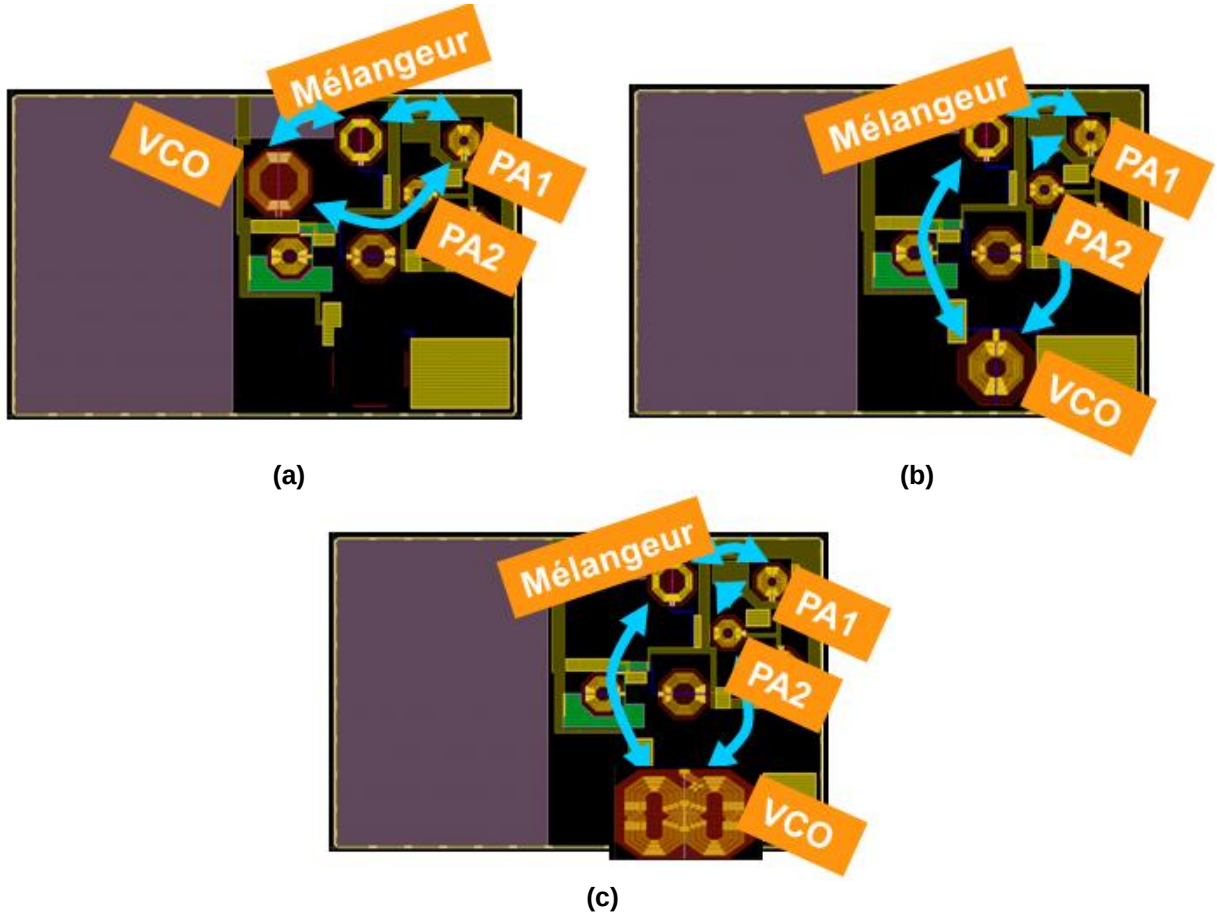


Figure 4: Différentes topologies possibles du circuit : Floor plan 1ère version (a), VCO déplacé (b) et VCO avec Self-en-8 (c).

Dans la première version, les performances du circuit sont données à partir des courbes rouges de la Figure 5.

Dans la 2e version, on déplace la self du VCO (Oscillateur Contrôlé en Tension). On obtient les courbes orange dans la Figure 5 : une amélioration du couplage entre la self du VCO et celles du PA1 ainsi que celle du mélangeur.

En changeant le type de self du VCO, nous pouvons voir que les niveaux de couplage entre les différentes boucles sont nettement plus bas.

Il est à noter que la multitude et la complexité des interactions électromagnétique peut justifier la décroissance du couplage en hautes fréquences.

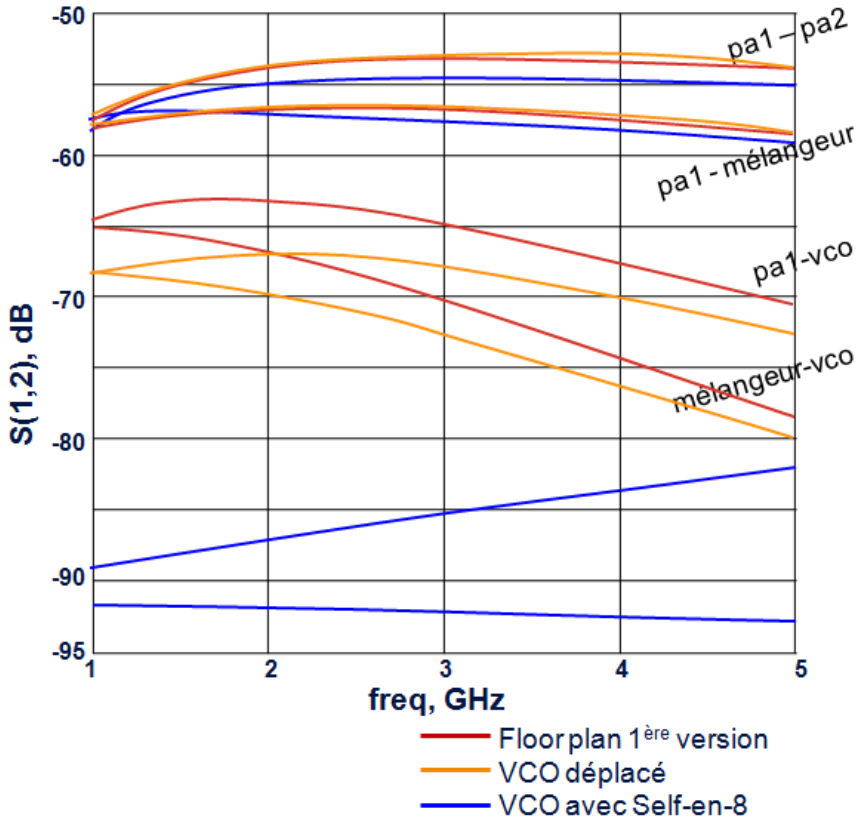


Figure 5: Résultat de simulation pour le couplage (S12) entre deux inductances selon les différentes topologies du circuit.

c. Illustration Niveau Bloc de Fonction (VCO)

Au niveau bloc de fonction, nous avons dans la figure suivante la structure physique d'un VCO où nous pouvons distinguer des boucles d'inductances reliées au reste du circuit par des éléments d'interconnexion (mis en évidence dans la Figure 6).

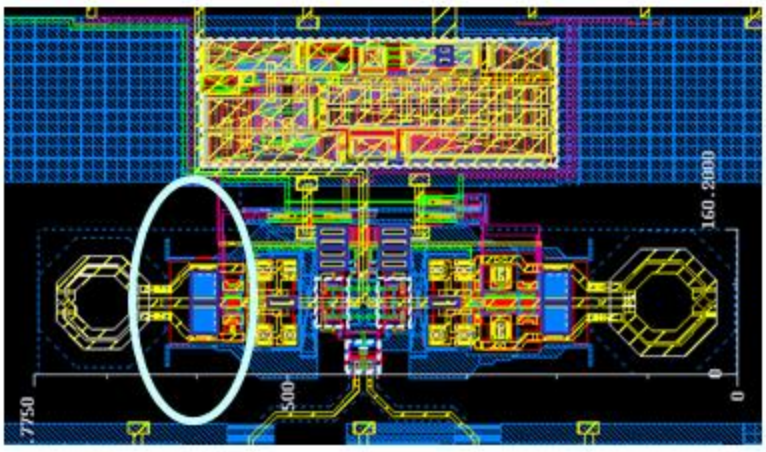


Figure 6: Layout d'un VCO comportant 2 boucles inductances connectées au reste du circuit par des lignes d'interconnexions.

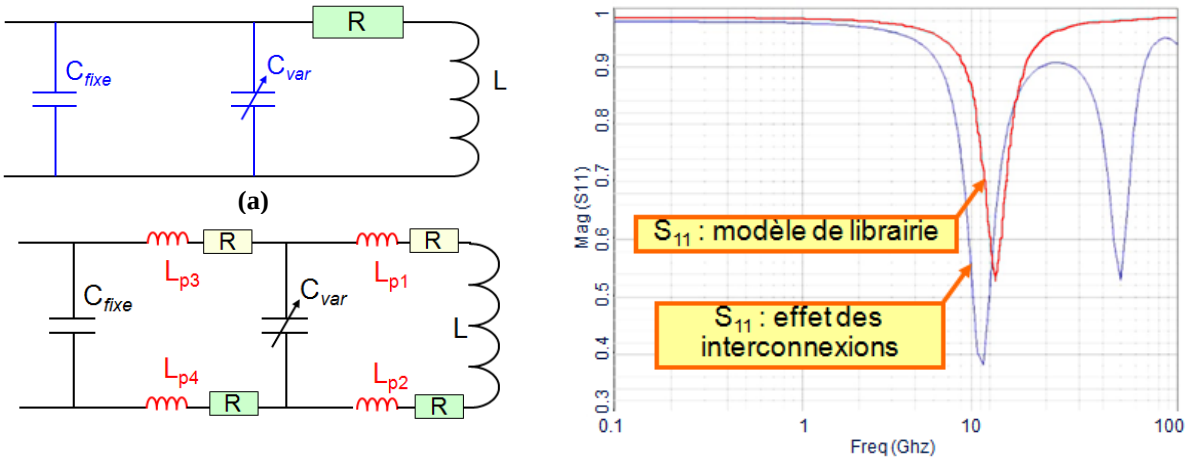


Figure 7: Schéma équivalent idéal du VCO (a), prenant en compte les inductances des interconnections entre les éléments de librairie (b) et résultat de simulation des schémas équivalentes dérivés (c).

Idéalement, la fréquence de résonnance du circuit serait de :

$$f_1 \approx \frac{1}{2\pi\sqrt{L \cdot (C_{var} + C_{fixe})}} \qquad (1)$$

En prenant en compte les inductances des interconnexions entre les éléments de librairie L_{pi}, nous obtenons les fréquences suivantes :

$$f_{1\_par} \approx \frac{1}{2\pi\sqrt{(L + L_{p1} + L_{p2}) \cdot (C_{var} + C_{fixe})}} \qquad (2)$$

$$f_{2\_par} \approx \frac{1}{2\pi\sqrt{(L_{p3} + L_{p4}) \cdot C_{fixe}}} \qquad (3)$$

Tableau 1: Résultat de l'analyse du VCO prenant en compte les interconnexions

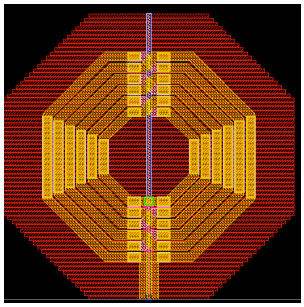
	Librairie	Analyse	Différence
1ère résonance	10.8 GHz	9.1 GHz	-15.7 %
2eme résonance	N/A	49.2 GHz	N/A

L'analyse nous montre que les interconnections sont caractérisés par des inductances (L_{p1} et L_{p2}) qui font baisser la première fréquence de résonance. De plus, la topologie particulière du circuit fait apparaître une seconde fréquence de résonance à travers L_{p3} et L_{p4}. Cependant, les modèles de librairie ne permettent pas de prédire cette 2e résonance.

Cette 2eme résonance peut induire des remontées d'harmoniques dans le spectre du VCO.

Or ces remontées d'harmoniques dépendent des niveaux de puissance de sortie.

d. Effets des Couplages sur les Spurs



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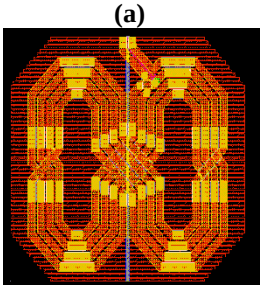

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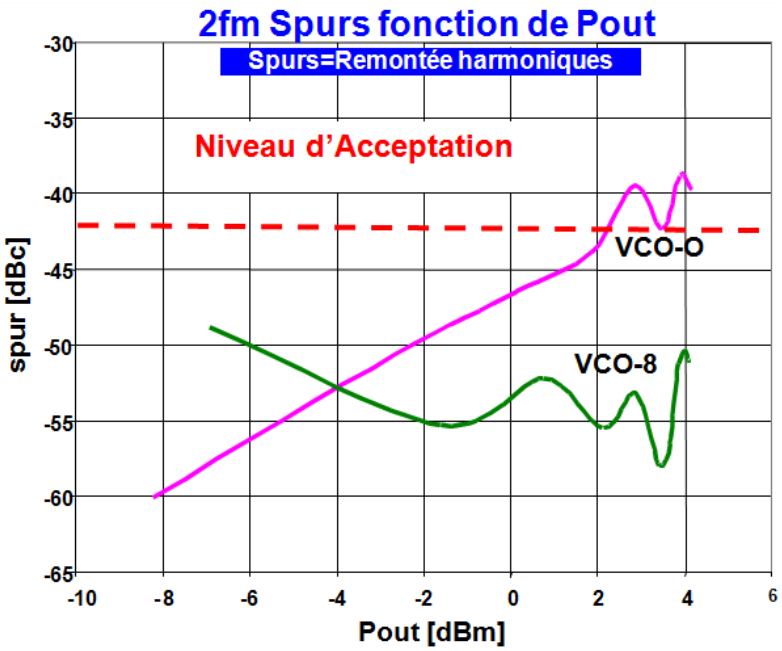


(c)

Figure 8: Self Octogonale du VCO (a), self en 8 du VCO (b) Niveau des spurs en fonction de la puissance en sortie du VCO (c).

La Figure 8 montre le niveau des remontées d'harmoniques (spurs), pour la fréquence double de la fondamentale, en fonction de la puissance de sortie.

On observe un effet significatif de la topologie de la self du VCO sur les remontées d'harmoniques.

I.4. Observations

A travers cette partie concernant la motivation, le contexte et les challenges du sujet, en s'appuyant sur l'exemple du circuit Bluetooth et l'exemple de son VCO, nous avons pu noter les observations suivantes :

- L'importance de la précision de l'estimation des effets inductifs dans le calcul de la fréquence de résonance.
- L'importance de la prise en compte de la topologie des inductances, incluant leurs connexion.
- L'importance de l'analyse au niveau floorplan.
- L'importance de la topologie des inductances sur les performances au niveau systèmes.
- Les limitations de la représentation électrique.
- La complexité d'utilisation de l'outil électromagnétique au niveau floorplan.

D'où la nécessité :

– D'une estimation simple et rapide au premier ordre des couplages au niveau floorplan *(en amont conception, tendance importante).*

– D'une analyse EM globale pour la précision des estimations au niveau composant et bloc de fonction *(durant conception: précision importante).*

II. Limitations Perçues de l'Etat de l'Art

II.1. Le Pulling et le Pushing dans les Synthétiseurs de Fréquence

L'injection de signal parasite de fréquence f_{inj} très proche de celle de la PLL entraine des remontées d'harmoniques, appelées Pulling ou Pushing selon la nature du signal parasite, dans son spectre de sortie. La PLL oscillant initialement à f_0 voit sa fréquence d'oscillation se déplacer vers f_{inj} . La Figure 9 illustre le phénomène.

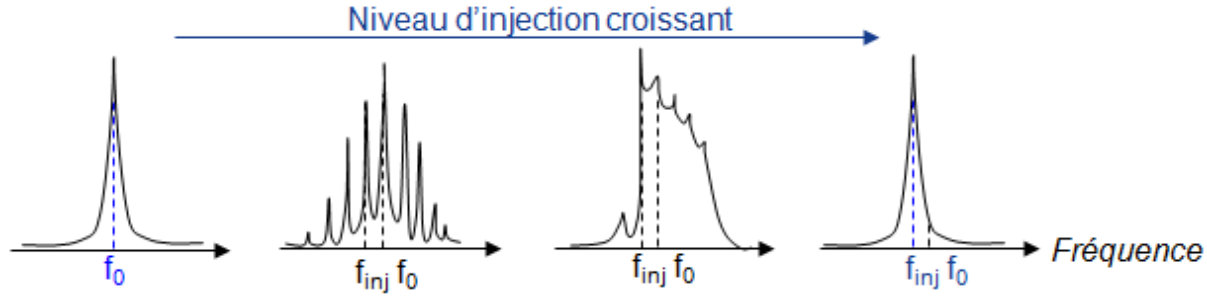


Figure 9: Illustration du phénomène de pulling.

II.2. Complexité des PLLs et Défis des Analyses

La PLL est un système bouclé, asservi et contrôlé constitué de plusieurs blocs. Elle nécessite donc une attention particulière due à sa régulation, sa stabilité.

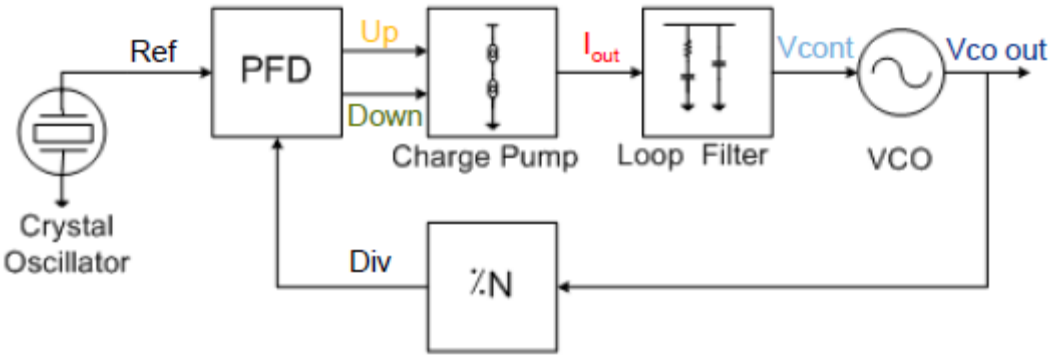


Figure 10: Schéma d'une boucle PLL

Le système couple plusieurs signaux de nature et d'échelles différentes :

- Le Cristal délivre un signal carré de basse fréquence
- Le PFD/CP délivre un switch en courant
- Le filtre RC délivre tension DC
- Le VCO une tension sinusoïdale RF
- Et le diviseur par N un signal carré de fréquence freq=f_{RF}/N.

L'analyse de la PLL est donc difficile d'accès. Pour analyser une PLL entière, il est nécessaire d'utiliser une approche d'analyse hiérarchique.

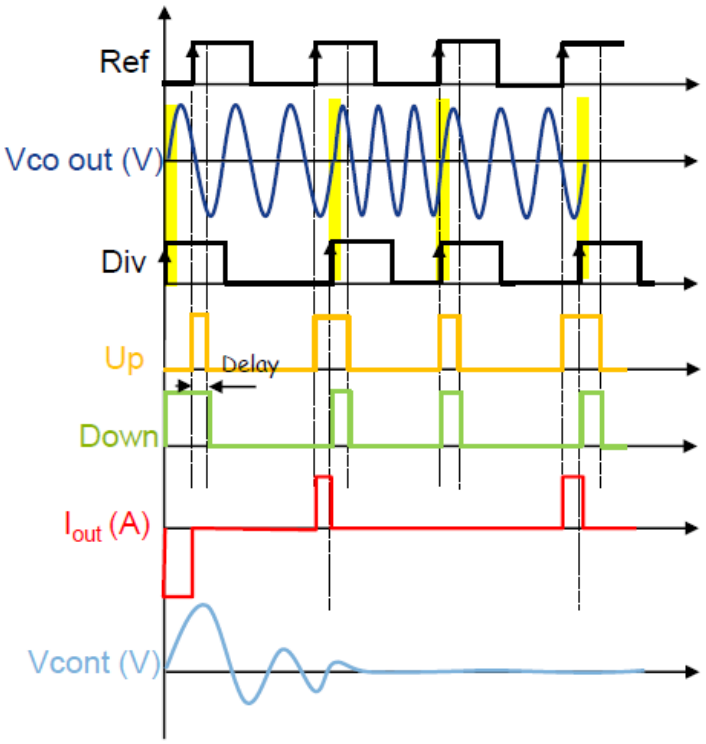


Figure 11: Exemple de différents types de signaux dans une PLL.

II.3. Le Pulling et le Pushing dans un Système de Transmission Puce+Boîtier+PCB

Dans une chaine de transmission complète, des sources d'interférences peuvent entrer en jeu, par exemple:

- les alimentations des autres blocs internes à l'IC
- la variation de la charge externe à l'IC
- Les interactions entre l'IC/boitier/PCB.

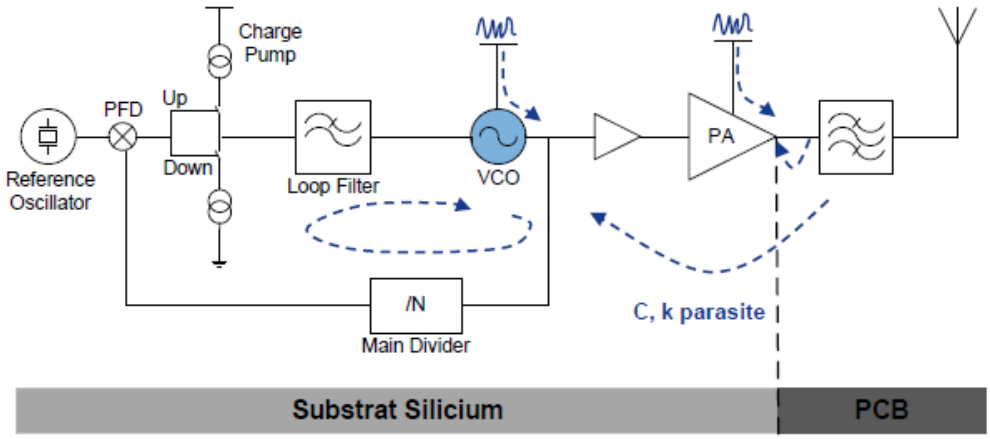


Figure 12: Exemple de système de transmission Puce+Boîtier+PCB où des sources d'interférences entrent en jeu

Cependant dans la littérature actuelle :

- Les causes du pulling et du pushing dans les PLLs sont généralement supposées être liées au VCO.

- Très peu d'analyses prennent en compte les effets des autres blocs de la PLL (PFD, CP, Filtre de boucle) sur le pulling
- L'influence du Boîtier et du PCB est généralement inexplorée.

II.4. Défis Pratiques de la Co-Simulation: Puce-Boîtier-PCB

Les domaines: Puce, Boîtier & PCB sont souvent supposés comme étant des activités différentes et disjointes.

Pourquoi?

En partie du fait de l'absence d'un standard pour une conception unifiée des 3 domaines: Puce (utilisation du format GDS/DXF, LEF/DEF), Package (utilisant le format MCM SiP) & PCB (utilisant le format Gerber NDD).

Les conséquences?

L'Approche Cascade néglige les interactions entre les 3 domaines.

II.5. L'approche Cascade

Etant donnée la complexité de l'analyse, l'approche séquentielle dite cascade est communément utilisée.

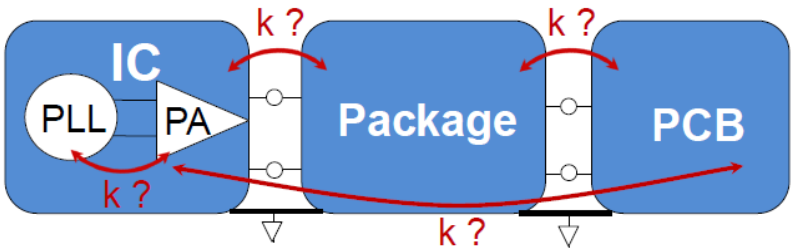


Figure 13: Illustration de l'approche cascade négligeant les couplages entre les différents (sous-) circuits

Son utilisation conduit à une complexité accessible à l'analyse :

- Le circuit global est subdivisé en sous-circuits (partitions)
- Chaque sous-circuit est analysé de manière indépendante
- Les différents résultats sont collectés dans un même simulateur de circuit (type SPICE/SPECTRE).

Mais elle pose aussi des difficultés techniques concernant les couplages et les interactions :

- Les couplages entre sous blocs de l'IC sont souvent négligés
- Les couplages entre l'IC et le package sont souvent ignorés
- Les couplages IC-Packages-PCB ne sont pas pris en compte.

Ces difficultés techniques conduisent à des approches essentiellement basées sur des **campagnes de caractérisation expérimentales** très **couteuses en temps** et en **nombre de révisions** des circuits.

➢ **D'où la nécessité de capitaliser les caractérisations expérimentales sous forme de règles de conception pour limiter les itérations dans le cycle de conception.**

➢ **D'où l'importance, de développer des méthodologies globales basées sur des analyses prédictives permettant de limiter les caractérisations expérimentales.**

III. Contribution Proposée

Deux axes sont étudiés:

1) La Caractérisation & Analyse Expérimentale des Effets de Pulling/Pushing : Un objectif d'Ediction de Règles de Conception est poursuivi en utilisant des Approches Analytiques et Semi-Analytiques.

2) Le développement de Méthodologies Globales pour l'analyse des Effets de Pulling/Pushing. Un objectif de prise en compte des effets de couplages résultant des interactions Puce-Boitier-PCB est poursuivi en vue d'une analyse prédictive limitant les campagnes de caractérisations expérimentales (très couteuses).

Les Etudes et Analyses concernent deux applications:

- **Une application Automotive : le LoPSTer**

Un circuit déjà existant où seront fait :

  - Les caractérisations expérimentales
  - Les différentes révisions du circuit pour amélioration des performances en vue de l'édiction de règles de conception.

- **Une application Satellitaire : le TFF1014**

Un circuit en cours de développement qui permet :

  - L'analyse prédictive en amont des vérifications expérimentales
  - De développer et d'appliquer une méthodologie globale pour la prise en compte des couplages électromagnétiques au niveau IC-Package-PCB.

- Ces deux applications sont complémentaires :
  - Le circuit automotive est essentiellement caractérisé en mode transmission TX (autour de 1 GHz: moyenne fréquence)
  - Le circuit satellitaire est analysé mode réception RX (autour de 10 GHz: plus haute fréquence) .

III.1. Caractérisation Expérimentale des Effets de Pulling/Pushing

a. Observations Expérimentales et Analyse

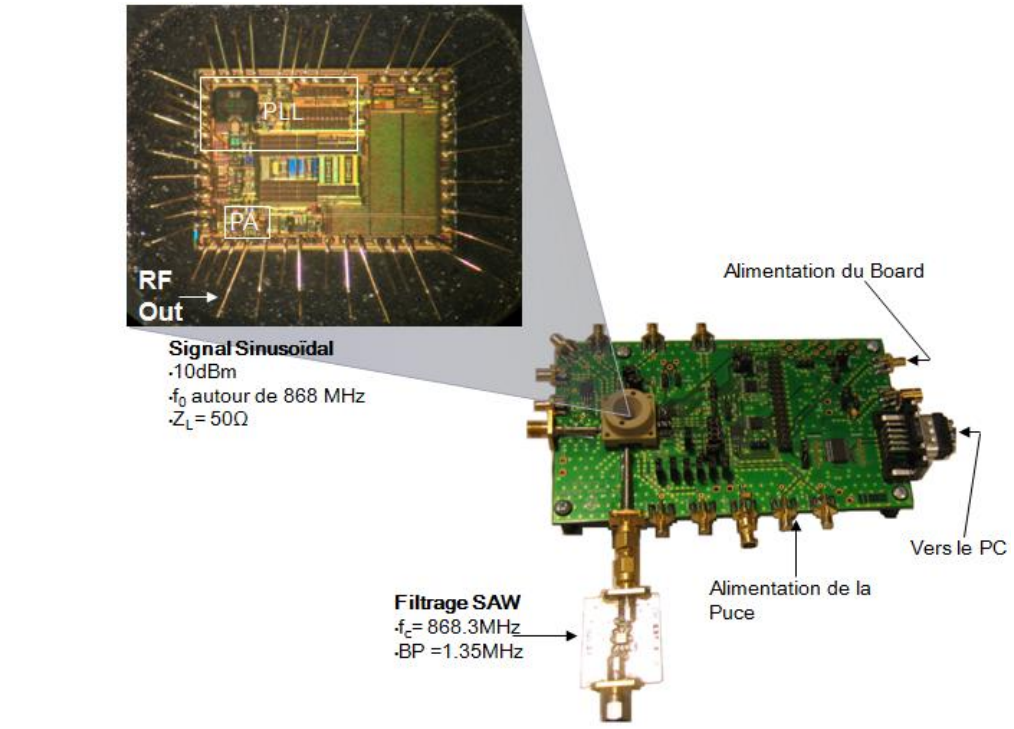
Caractérisation Expérimentale des Effets de Pulling/Pushing: Système Puce-Boîtier-PCB

Nous nous baserons sur l'application automotive fonctionnant autour de 1GHz. L'application système comporte:

- **Un IC** : transceiver RF en mode TX
- **Un PCB de test**
- **Une Solution de filtrage externe** (Filtre SAW sur PCB)
- **Une Antenne** ↔ Analyseur de spectre (R&S FSP7).

Lorsque la fréquence de travail f_{RF} = 868MHz se trouve à l'intérieur de la bande passante du filtre, nous obtenons le spectre et le bruit de phase présentés en Figure 14.

Lorsque f_{RF} se situe autour des fréquences de coupure supérieure du filtre SAW, nous pouvons retrouver le phénomène de pulling (Figure 15).



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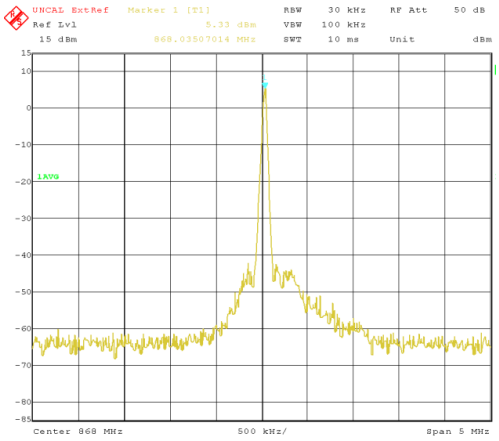

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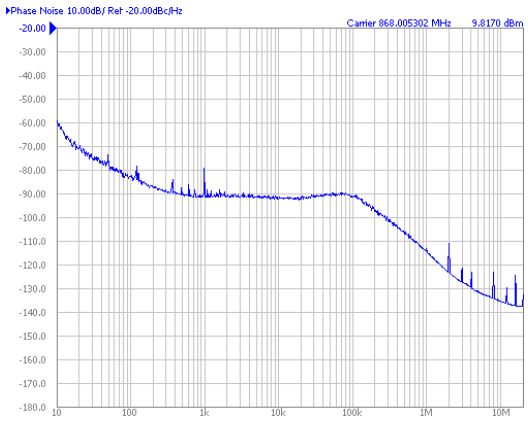
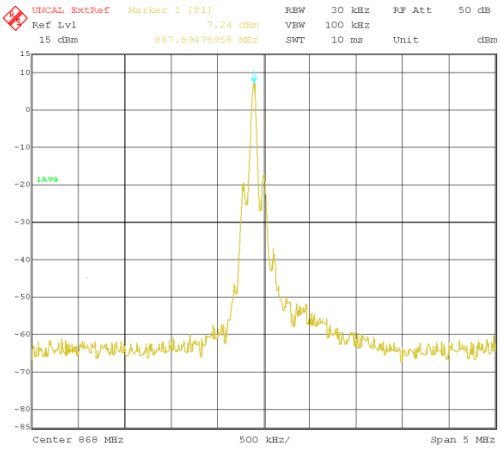


(c)

Figure 14: Caractérisation à travers un analyseur de spectre (a), Spectre de sortie (b) et de bruit de phase (c) du signal de l'LoPSTer de carte de sortie à 868MHz sans le filtre SAW.



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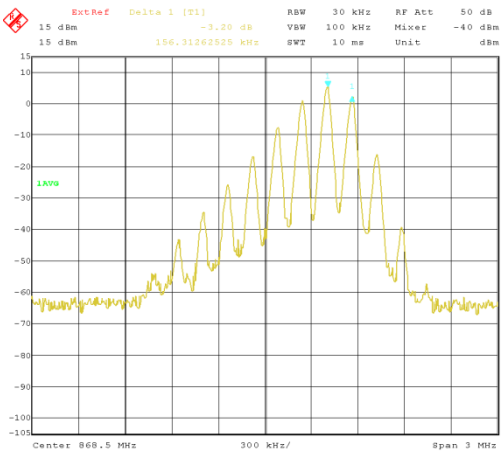


(b)

Figure 15: Spectres en sortie du LoPSTer en cascade avec le SAW EPCOS B3762 fonctionnant à des fréquences autour des fréquences de coupure inférieures (a) et supérieures (b) du filtre.

Caractérisation Expérimentale des Effets de Pulling/Pushing: le SAW

La fonction de transfert du filtre est exprimée à partir de ses paramètres S_{ij}, de l'impédance de charge Z_L et de l'impédance caractéristique Z_0 du système étudié :

$$H(j\omega) = \frac{2 \cdot Z_L \cdot S_{21}}{(Z_0 - Z_L)(S_{11} \cdot S_{22} + S_{22} - S_{12} \cdot S_{21}) + (Z_0 + Z_L)(S_{11} + 1)} \quad (4)$$

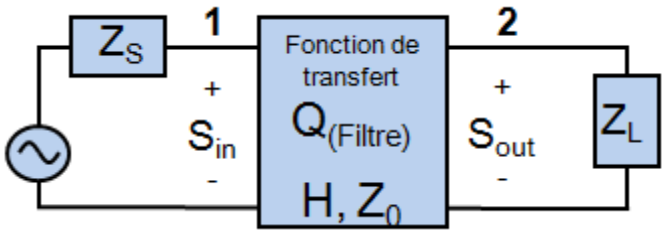


Figure 16: Illustration de la représentation d'un quadripôle

Concernant la solution de filtrage, nous pouvons remarquer:

- Une variation rapide de Zin du filtre à ses fréquences de coupure, Zin idéalement à 50Ω. La question de Matching large-bande est posée.
- Une pente abrupte de la fonction de transfert aux fréquences de coupure du filtre.

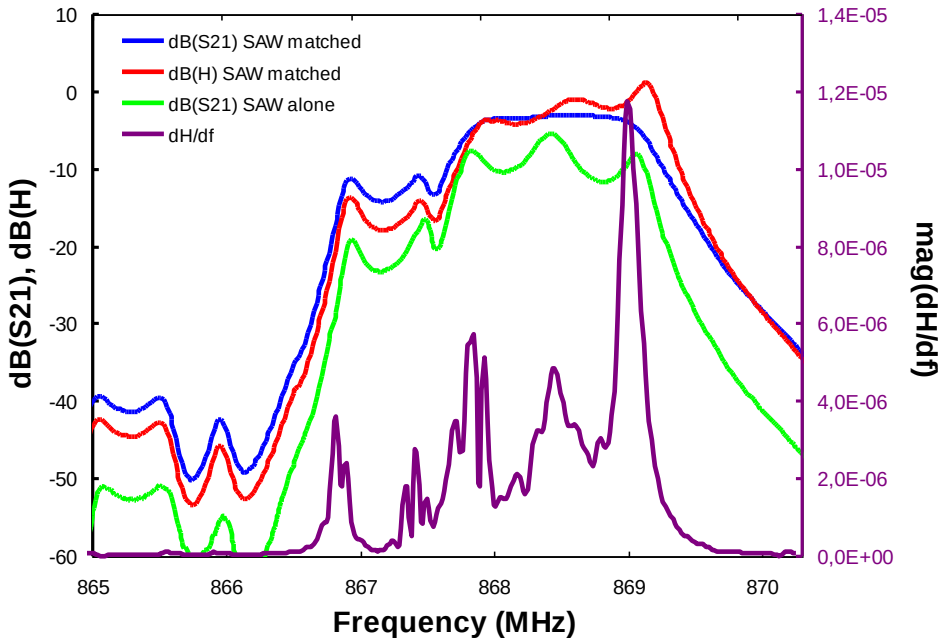


Figure 17: Réponse en fréquence (S21) et fonction de transfert H du filtre SAW

Il est à noter qu'il n'y a pas de spurs en sortie de l'application étudiée si le filtre SAW n'est pas inséré entre le PCB de test et l'antenne.

On observe le phénomène de pulling si f_{RF} est proche des fréquences de coupure du filtre : bande passante très restrictive et forte variation de la dérivée de H(jω) à ces fréquences.

La dérivée de la fonction de transfert peut-être un indicateur de pulling.

Le VCO & le Pulling

Impact de l'insertion du filtre SAW sur le VCO aux fréquences de coupure du filtre (supérieure : ~ 869MHz) :

- Saut en fréquence de la sortie du VCO
- Variation rapide du gain du VCO.

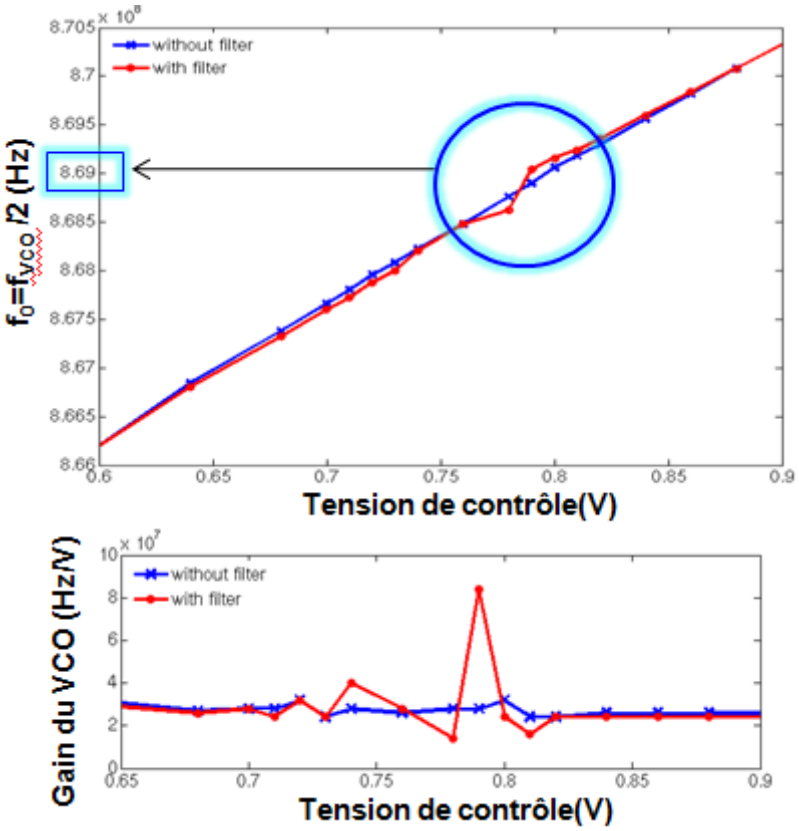


Figure 18: Les effets du pulling sur le VCO

L'Interaction entre le filtre SAW et le VCO met en évidence la non linéarité du gain du VCO et les effets de pulling.

Influence du Courant de Charge Pump

On ne reporte pas de Pulling sans PLL bouclée, on obtient directement un saut de la fréquence de travail voulue à une autre fréquence

La variation du courant de charge pump (ICP) impacte fortement le pulling en termes:

- D'amplitude des spurs
- Positionnement fréquentiel des spurs par rapport à la fréquence centrale f_0
- De niveau de bruit autour de f_0 .

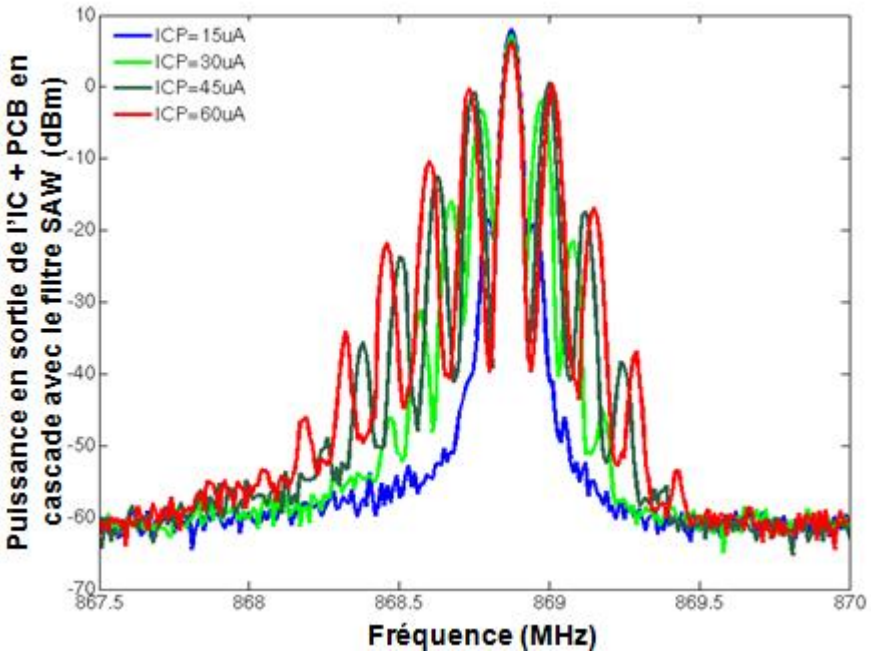


Figure 19: Le pulling en fonction du courant de charge pump de la PLL

Influence des Interactions Parasites sur le PA

Le pulling est favorisé par un niveau de puissance fort en sortie de l'amplificateur de puissance (PA), par exemple à 12dBm.

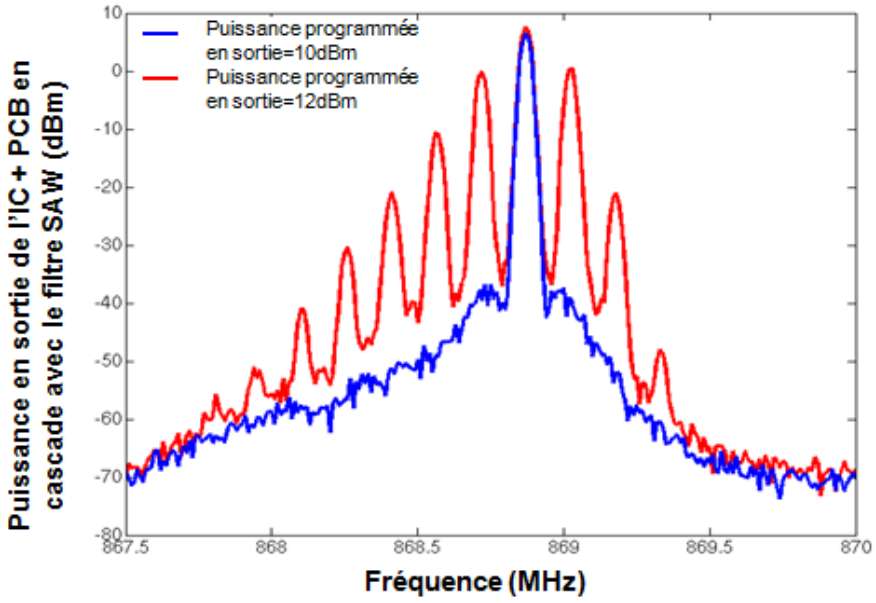


Figure 20: Spectre en sortie du système Puce+ boitier+ PCB en fonction de la puissance programmée en sortie

Or, la puissance en sortie du PA dépend de la capacité effective totale en parallèle du système incluant:

- Les capacités intrinsèques PA (IC)
- Les capacités charge au niveau PCB
- Une capacité équivalente externe ΔC due aux capacités parasites de l'interaction PCB/Puce.

Comme on peut le voir en Figure 21, plus les capacités parasites ΔC sont importants, plus le niveau de la puissance en sortie du PA est élevé, pouvant ainsi favoriser le phénomène de pulling.

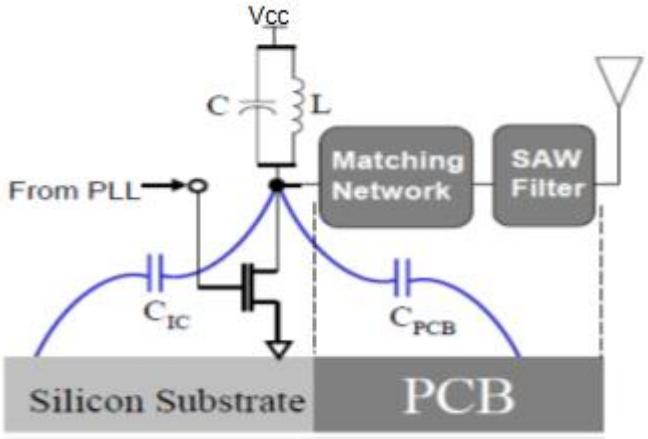


Figure 21: L'amplificateur de puissance et les capacities parasites

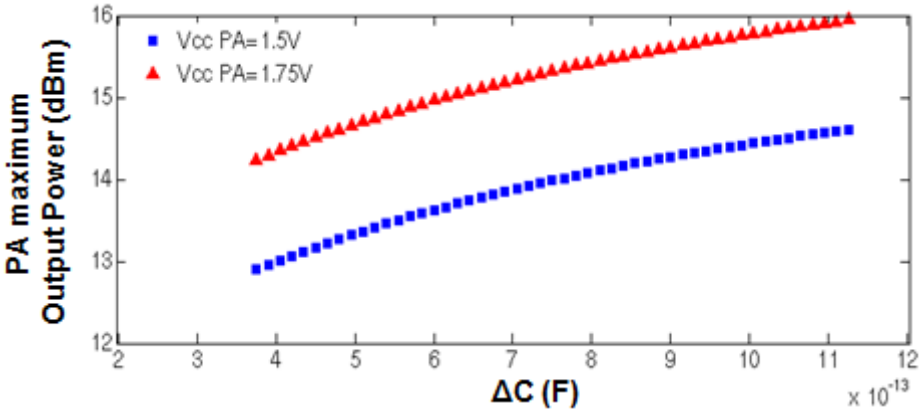


Figure 22: Puissance en sortie de PA en fonction des capacités parasites dues aux interactions PCB/Puce

III.2. Modélisation Analytique et Semi-Analytique

a. Intérêts des Approches Analytiques / Semi-Analytiques Proposées & Hypothèses

Durant les étapes de floorplan (placement) et de spécifications, les approches analytiques et semi-analytiques permettent :

- Le dimensionnement des composants et l'évaluation des couplages entre blocs
- L'application aux géométries utilisées par les concepteurs
- L'application à l'étude de faisabilité et l'optimisation

Ces approches sont simples à implémenter et rapides. Les précisions obtenues sont comparables à celles des approches existantes avec comme intérêt une personnalisation adaptée. Elles permettent aussi une estimation grossière des tendances de variations (choix topologiques).

Durant l'utilisation de ces approches, nous poserons les hypothèses suivantes :

- Les approches seront considérées comme quasi-statiques
- On utilisera des structures simples, canoniques et régulières
- Les boucles de retour sont rejetées à l'infini pour simplifier les calculs
- Les pertes métalliques sont prises en compte (impédance surface).

Les approches Analytiques et Semi-Analytiques sont utilisées pour la distinction des types de spurs et l'estimation des amplitudes de raies parasites, avec approximation des couplages capacitifs et inductifs.

b. La Reproduction des Effets Pulling: le Modèle Cascade

Pour reproduire les effets de pulling, nous utilisons le modèle cascade pour relier la puce et Filtre SAW. Comme illustré en Figure 23:

- Le signal en sortie de la puce reportée sur le PCB de test est égal au signal d'entrée du SAW
- Le filtre SAW est décrit par sa fonction de transfert $H(j\omega)$
- Le signal en sortie du SAW chargé par l'antenne (considérée à 50Ω) est donné par:

Dans le domaine fréquentiel:

$$S_{out}^{FD}(j\omega) = H^{FD}(j\omega) \cdot S_{in}^{FD}(j\omega) \quad (5)$$

Par convolution, dans le domaine temporel :

$$S_{out}^{TD}(t) = H^{TD}(t) \otimes S_{in}^{TD}(t) \quad (6)$$

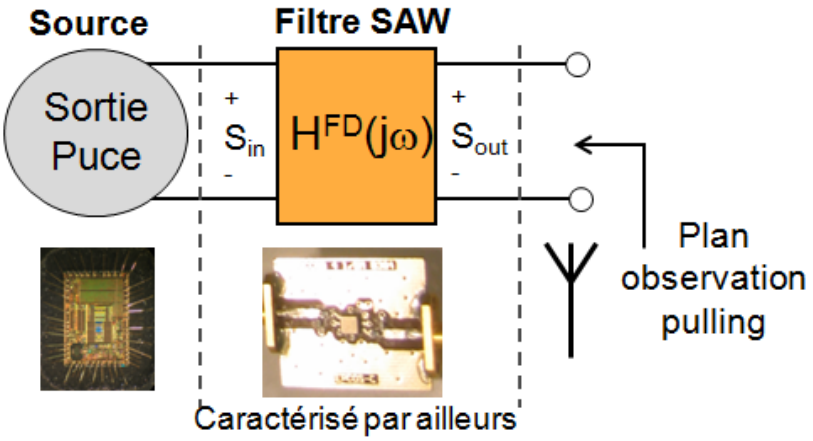


Figure 23: Mise en cascade de la puce et du filtre SAW

L'absence de données constructeur en DC pour le filtre SAW (paramètres-S) souligne la nécessité d'une extrapolation en DC pour le calcul de $H^{TD}(t)$. La méthodologie de synthèse développée permet de résoudre ce problème.

c. Estimation Remontée d'Harmoniques

Nous posons l'hypothèse que le pulling est une combinaison de spurs de modulation d'amplitude AM et de fréquence FM.

Comme signal réel nous avons :

$$S_{Pulling}(t) = A \cdot (1 + \varepsilon \times \cos(\Delta\omega t)) \times \sin(\omega_0 t) + A \times \sin\left(\omega_0 t + \varepsilon \times \int_0^t \cos(\Delta\omega t)\right) \quad (7)$$

Lors du développement en harmoniques d'ordre k de cette formule nous obtenons:

$$S_{Pulling}(t) = A\cdot(k+1)\times\sin(\omega_0 t) + \sum_k\left[\frac{A}{2}\left(\varepsilon_{AMk} + \frac{\varepsilon_{FMk}}{\Delta\omega_k^{Pulling}}\right)\times\sin\left(\omega_0 t + \Delta\omega_k^{Pulling} t\right)\right] + \sum_k\left[\frac{A}{2}\left(\varepsilon_{AMk} - \frac{\varepsilon_{FMk}}{\Delta\omega_k^{Pulling}}\right)\times\sin\left(\omega_0 t - \Delta\omega_k t\right)\right] \quad (8)$$

Nous obtenons le spectre suivant:

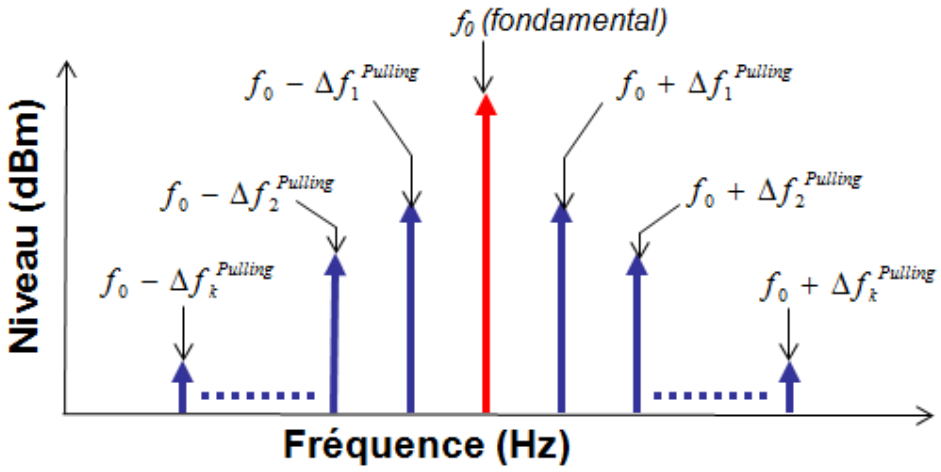


Figure 24: Spectre du développement du pulling en terme de combinaison AM et FM

Avec :

$$\begin{cases} Niveau(dBm) = 10\log\left(\dfrac{|V_{pk}|^2}{2\times R_0\times 1mW}\right) \\ |V_{pk}| = \sqrt{2\times R_0\times 1mW\times 10^{\frac{Level(dBm)}{10}}} \end{cases} \quad (9)$$

Résultats et Comparaisons:

Utilisation de l'Approche Cascade et d'une modulation AM en sortie de la puce

La mesure se fait au niveau de l'antenne sans filtre SAW. On définit le signal en sortie de la puce intégrée et de son réseau d'adaptation comme étant le résultat de mesure au niveau de l'antenne sans filtre SAW. On le modélise telle l'équation (7) avec une seule modulation en amplitude, puis, ce signal est utilisé comme étant le signal source en entrée du filtre.

La méthodologie proposée permettant d'exprimer le signal émis par le système global à l'antenne a été validée par corrélations entre des simulations effectuées avec des outils utilisant différentes approches :

- Approche « transient » et « balance-harmonique (HB)» d'ADS (Agilent)
- Approche « transient » de SPECTRE (Cadence)

Les mesures citées précédemment sont effectuées avec un Analyseur de Spectre Rohde et Schwartz FSP7.

L'utilisation de l'approche cascade seule entre la puce et le SAW (sur PCB) reproduit le signal en sortie IC+SAW avec une bonne précision sur les amplitudes (Figure 25(a)), mais elle ne prend pas en compte les couplages entre Puce et SAW s'exprimant par le pulling (Figure 25(b)).

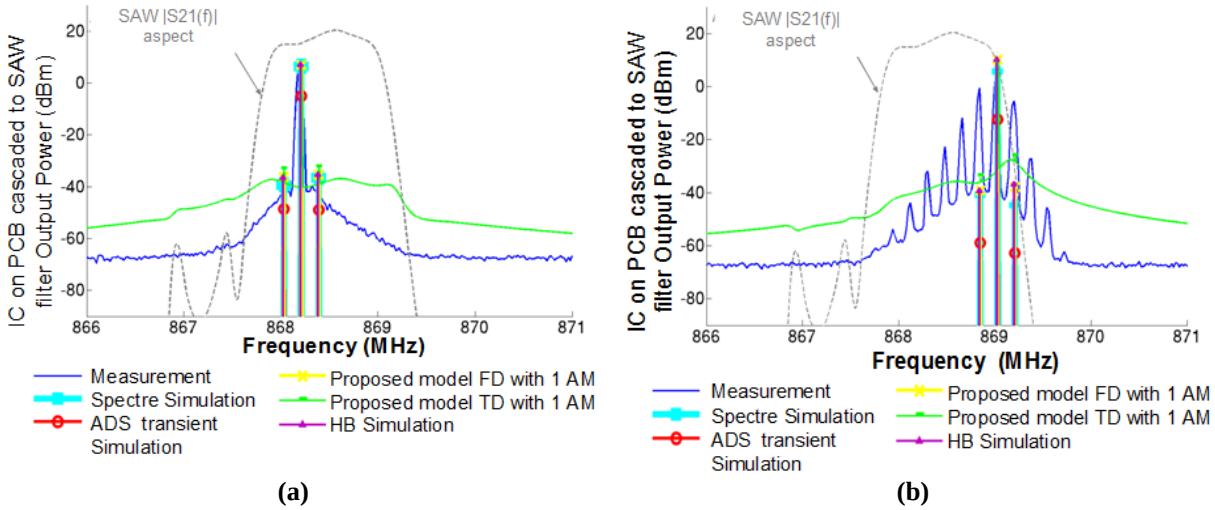


Figure 25: Signaux établis en sortie du filtre SAW lorsque le signal source se trouve à l'intérieur de la bande passante du filtre (a) ou lorsqu'il se trouve à la fréquence de coupure du filtre

Utilisation de l'Approche Cascade et la Modélisation du Pulling (en terme de AM+FM)

Pour reproduire le pulling, nous avons modélisé en amont le signal pré-distordu présumé (contenant les effets de pulling) en couplant les contributions des spurs AM+FM telle l'équation (8), puis nous utilisons l'approche cascade. Le résultat obtenu est présenté en Figure 26.

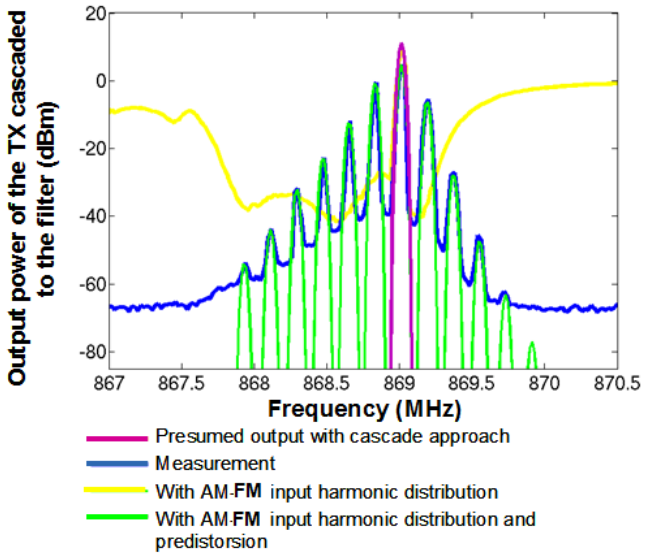


Figure 26: Signaux établis en sortie du filtre SAW lorsque l'on modélise le pulling en amont en terme de combinaison AM et FM

III.3. Vers une Ediction de Règles de Conception

a. Figures de Mérite Expérimentale : Formulation des Essais Expérimentaux en termes de règles

Les techniques FIB (Focused Ion Beam) permettent d'évaluer différentes options: masses séparées, alimentations séparées, sources externes (…). Nous avons donc utilisé cette méthode pour quantifier les effets observés sur le pulling. Afin de quantifier la sensibilité des

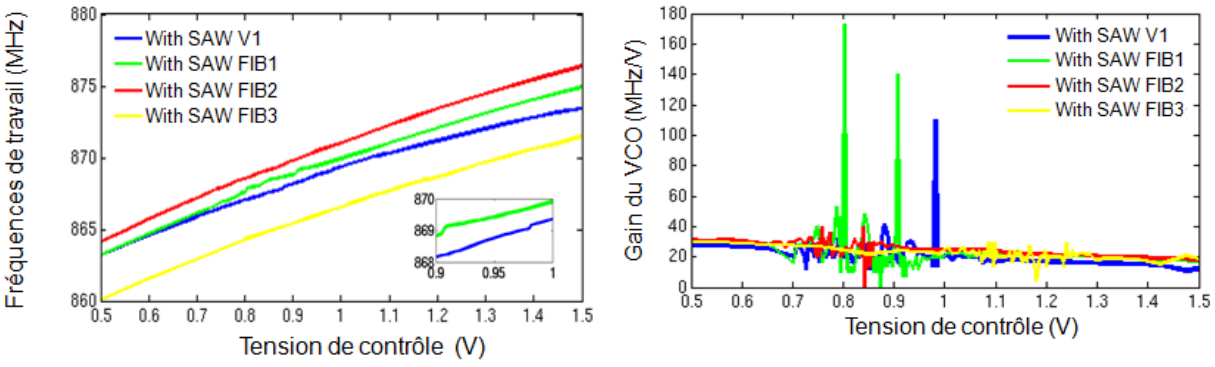
circuits intégrés par rapport à leur signal de sortie RF, une figure de mérite a été utilisée: Q_{EXT} .

$$Q_{EXT} = \frac{f_{RF}}{\Delta f_{lock}} \sqrt{\frac{P_{lock}}{P_{RF}}} \qquad (10)$$

Les résultats sont donnés dans le Tableau 2 et la Figure 27.

Tableau 2: Résultats des différents FIBs sur le pulling

	Modification FIB effectuées	Effets de mesures observés	QEXT
V1 (initiale)	Toutes les masses sont connectées au seal ring, les diviseurs RX sont proches du VCO au niveau layout et partagent la même masse que les drivers du PA	Effets de pulling aux fréquences de coupures du filtre SAW	Cas typique: 1500
FIB1	Cut pour isoler la masse du PA au seal ring et des autres masses du circuit	Effets de pulling persistant aux fréquences instables	1089
FIB2	Cut et strap du V_{CC} et de la masse des diviseurs RX vers un autre V_{CC} et distribution de masse que ceux du PA	Plus d'effet de pulling lorsque le filtre SAW voit une charge (antenne) de 50Ω	3272
FIB3	Combinaison de FIB1 et FIB2	Le système est stable	4106



(a) **(b)**

Figure 27: Effets sur la fréquence de travail (a) et Effets sur le gain du VCO (b) des différentes configurations de FIB.

Lorsque l'alimentation V_{CC} et la masse des diviseurs Rx (proches du VCO) sont découplés de ceux du PA (FIB2 &FIB3) les variations du gain du VCO moins abruptes et les effets de pulling disparaissent

D'où **l'importance de la séparation des domaines de masse et d'alimentation**

III.4. Synthèse

- **Influence du VCO**

La caractéristique non-linéaire du gain du VCO en fonction de la tension de contrôle mesurée induit le pulling: l'importance de la prise en compte de cet effet dans la simulation (hypothèse gain VCO constant) a été démontrée.

- **Influence de la Boucle PLL**

L'importance de la modélisation de la PLL entière et de la prise en compte des effets de chaque sous blocs de la PLL (charge pump) a été soulignée.

- **Influence du Filtre SAW**

Les effets de variation abruptes de la fonction de transfert du filtre SAW autour de la fréquence de travail de la PLL montre que la dérivée de la fonction de transfert peut-être un indicateur de pulling.

L'absence de composante DC dans données constructeur (paramètres-S) du filtre SAW révèle la nécessité d'une modélisation qui prenne en compte la composante DC.

L'influence du filtre SAW a aussi permis d'exposer la nécessité de prendre en compte les effets des composants reportés sur le PCB et leur interaction avec la puce.

- **Influence de l'Amplificateur de Puissance**

La corrélation entre niveau de puissance du PA et l'apparition du pulling nous a permis de confirmer la nécessité de prendre en compte des capacités parasites sur PCB.

L'analyse de la stabilité, la prédiction des formes d'ondes ainsi que le matching au niveau du PA sont de même essentiels.

- **Vers l'édiction de règles de conception sur la base des essais expérimentaux (FIB)**

Nous avons définis des facteurs de mérite pour quantifier le degré de pulling, et proposer des guidelines pour améliorer les pratiques.

- **Approches Analytiques et Semi-Analytiques (Spurs AM+FM)**

Ces approche ont permis de reproduire le signal en sortie IC et du SAW avec une bonne précision sur les amplitudes, mais elles ne prennent pas en compte les couplages entre Puce et SAW (sur PCB) et prennent difficilement en compte la complexité des topologies, des références de masse, et des couplages distribués: Effets Puce-Boitier-PCB.

D'où l'importance d'une Approche Globale

IV. Méthodologie Globale incluant les Effets Puce-Boîtier-PCB:

IV.1. Méthodologie de Partitionnement et Modélisation Electromagnétique

Pour aborder ce chapitre, nous nous baserons sur l'application Récepteur Satellite : le TFF1014.

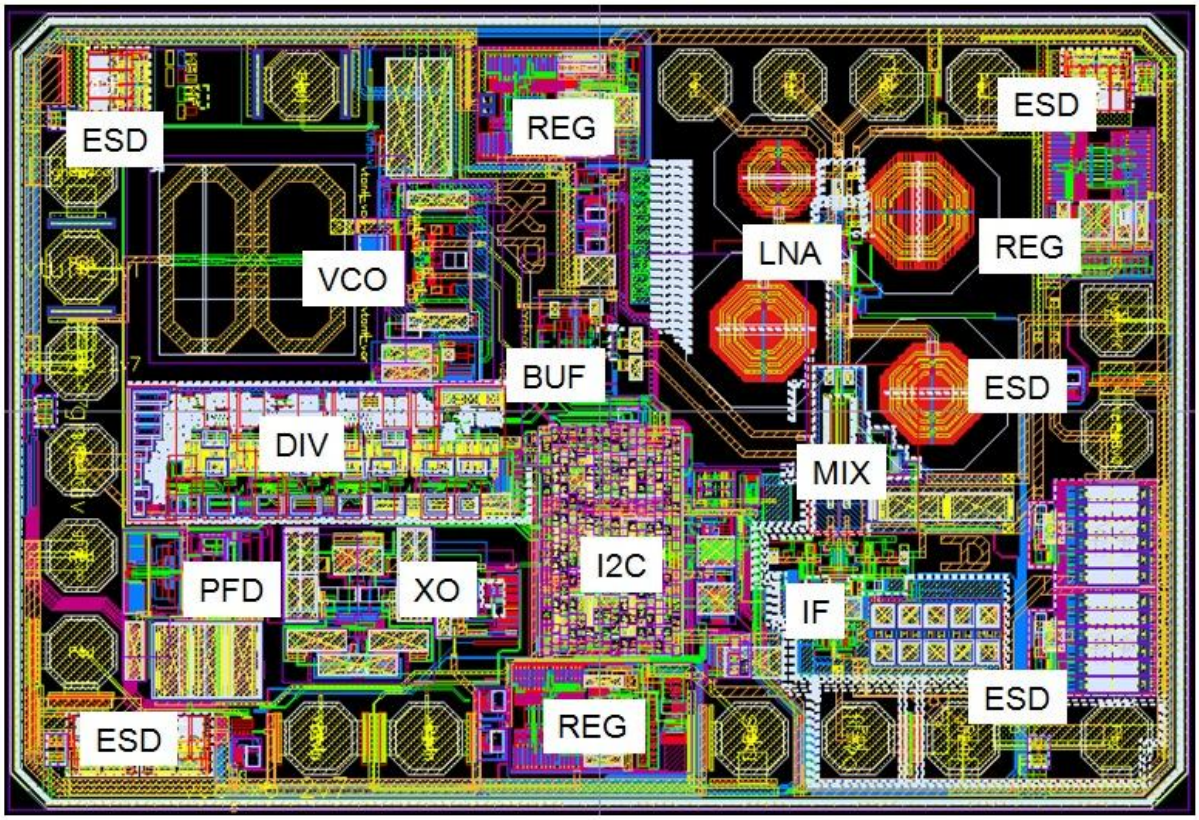


Figure 28: Layout et répartition des (sous-)blocks du TFF1014

a. Nécessité d'une Méthodologie de Partitionnement

Postulat: La façon la plus précise de prendre en compte tous les couplages entre blocs est de faire une analyse électromagnétique au niveau système, cependant aujourd'hui ce n'est pas possible du fait de la complexité.

D'où l'importance d'une démarche de partitionnement adéquat.

Si le partitionnement rend accessible l'analyse de systèmes complexes, il pose des défis: où positionner les frontières? Comment prendre en compte les couplages entres partitions? Quels outils utiliser pour quelle précision?

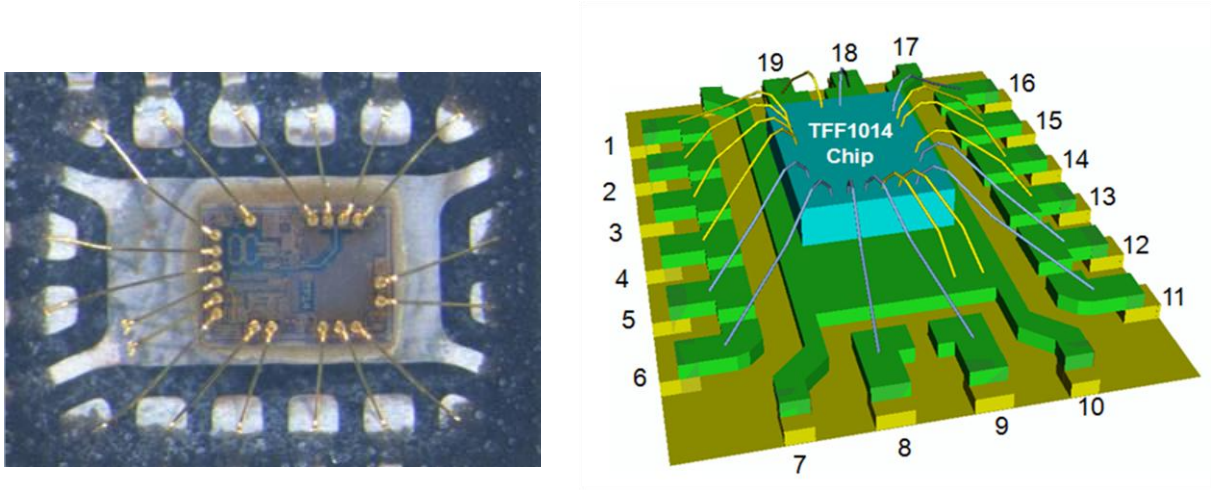
b. L'Analyse Electromagnétique Globale

La modélisation Electromagnétique globale a pour objectifs:

- Une stratégie de partitionnement pour la sélection des chemins critiques afin d'investiguer les distributions de chemin de retour de masse.
- Une description appropriée des ports d'excitation et leurs références de masse interne.
- La modélisation et analyse des métaux épais (combinaison de l' effet de peau et des parois- latérales).
- L'analyse comparative des stratégies d'isolation pour diminuer les couplages critiques.
- La dérivation de schéma équivalent distribué physique.

Analyse Electromagnétique du Système Assemblé

Au niveau puce, l'analyse EM est faite utilisant l'outil SiP de Cadence. La référence de masse se trouve au niveau PCB. La solution quasi-statique obtenue est précise jusqu'à 2 GHz, au-delà l'approche full wave est utilisée.



(a) **(b)**

Figure 29: Photographie du Packaged-Chip (a) et son modèle 3D (b) sous Cadence SiP

L'analyse permet d'extraire les selfs inductances, capacitances et résistances des différents nœuds ainsi que les mutuelles inductances, capacitance entre les différents nœuds.

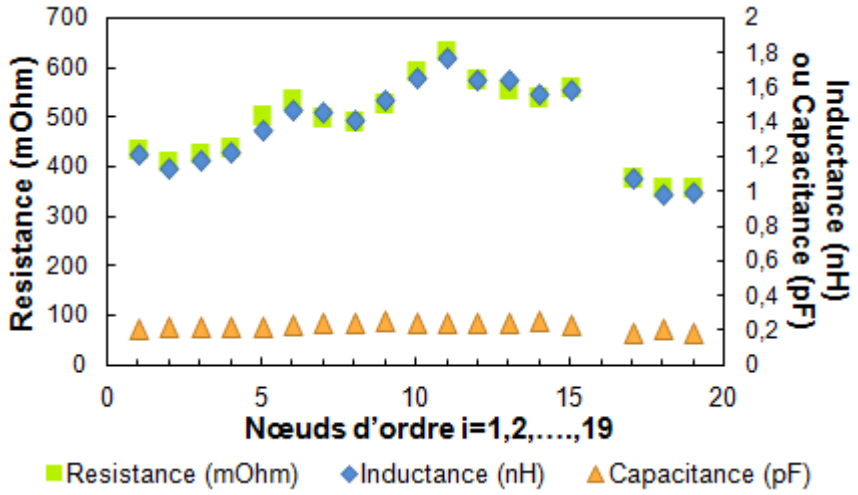


Figure 30: Self inductance, capacitance et résistance des différents nœuds

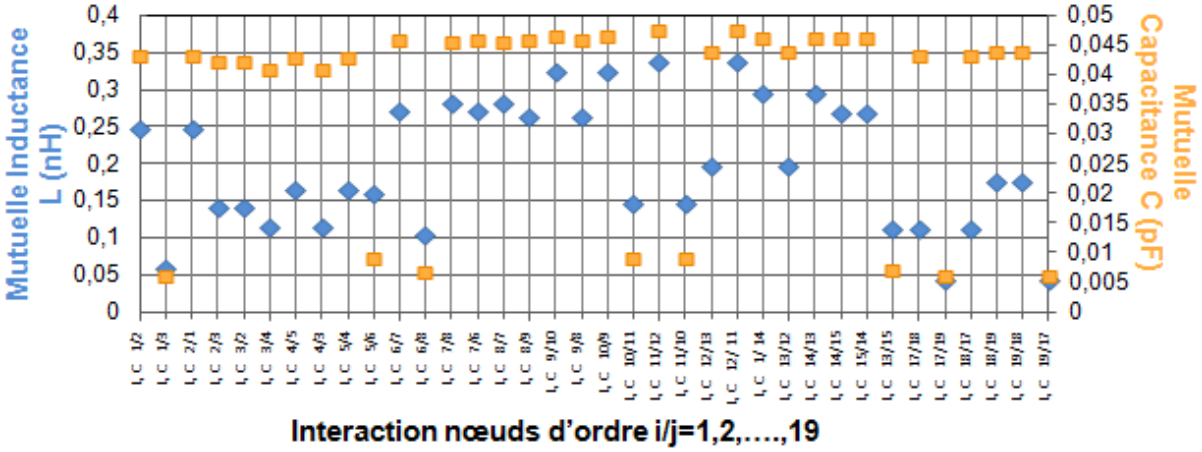


Figure 31: Mutuelle inductance, capacitance entre les différents nœuds

Analyse Electromagnétique au Niveau Puce

Au niveau puce, concernant l'analyse EM dédiée au pulling nous avons :

- Réalisé un test-chip de benchmark entre les inductances en 8 et en O pour évaluer les inductances/le facteur de qualité Q et les couplages EM
- Analysé l'influence de l'état électrique du Seal-Ring (interrompu/continu, flottant/relié à la masse) sur les performances RF
- Caractérisé les lignes couplées du VCO-Buffer
- Etudié les effets de De-embedding et la Calibration des structures de test
- Evalué l'efficacité des techniques d'isolation (DTI/Guard-Ring/cage de Faraday).

► Analyse prédictive pour la réduction de couplages EM

Dans le layout du TFF1014, une inductance proche de lignes de transmission (buffer VCO) peut induire des problèmes de couplage: nous avons proposé l'utilisation d'une inductance en 8 pour diminuer les couplages parasites.

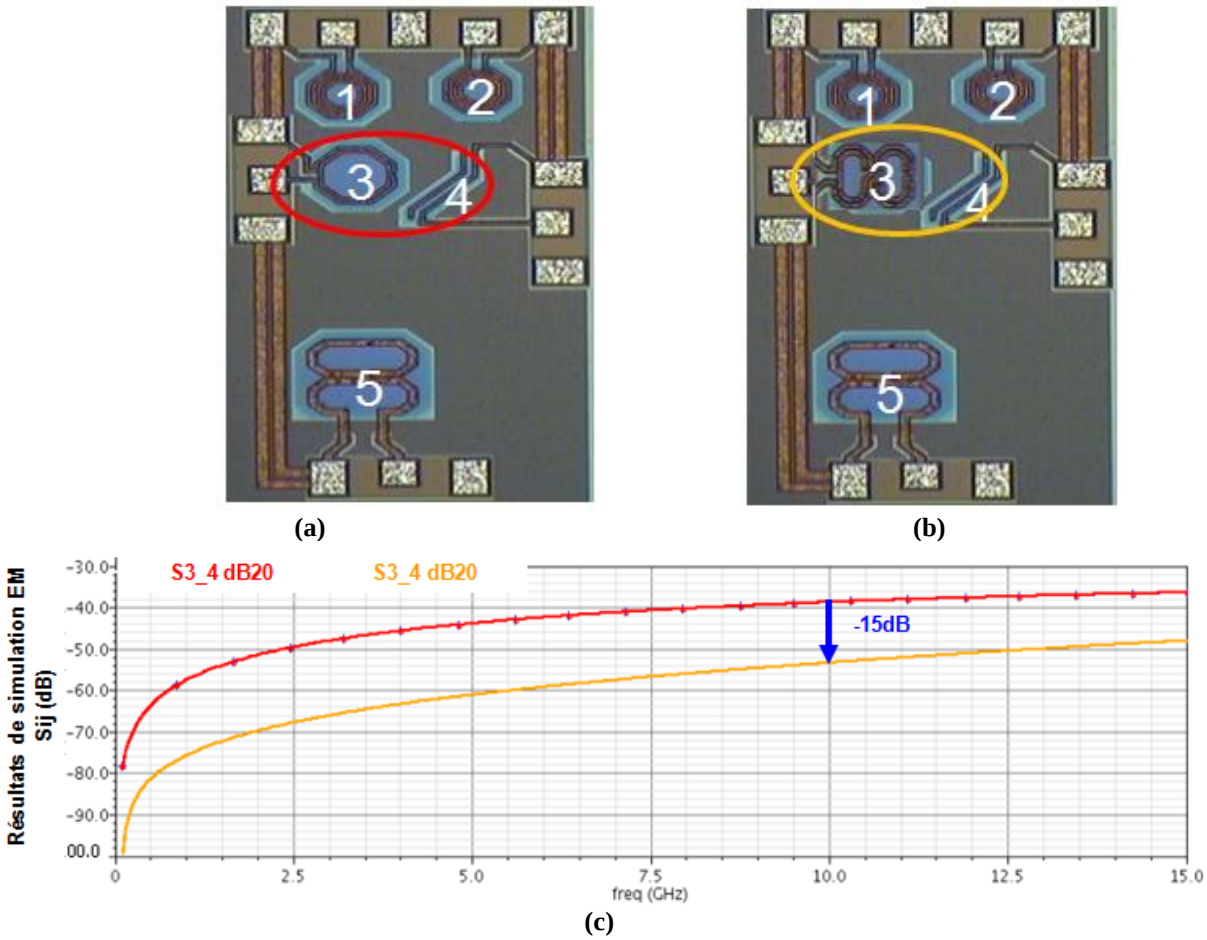


Figure 32: Analyse EM du couplage entre une inductance en 8 (a) ou une inductance en O (b) et une ligne, faisant parti du VCO buffer.

L'amélioration du couplage entre l'inductance en 8/O et la Ligne au voisinage obtenue à travers les simulations EM en Figure 32(c), a été confirmée par les résultats expérimentaux présentés en Figure 33(c).

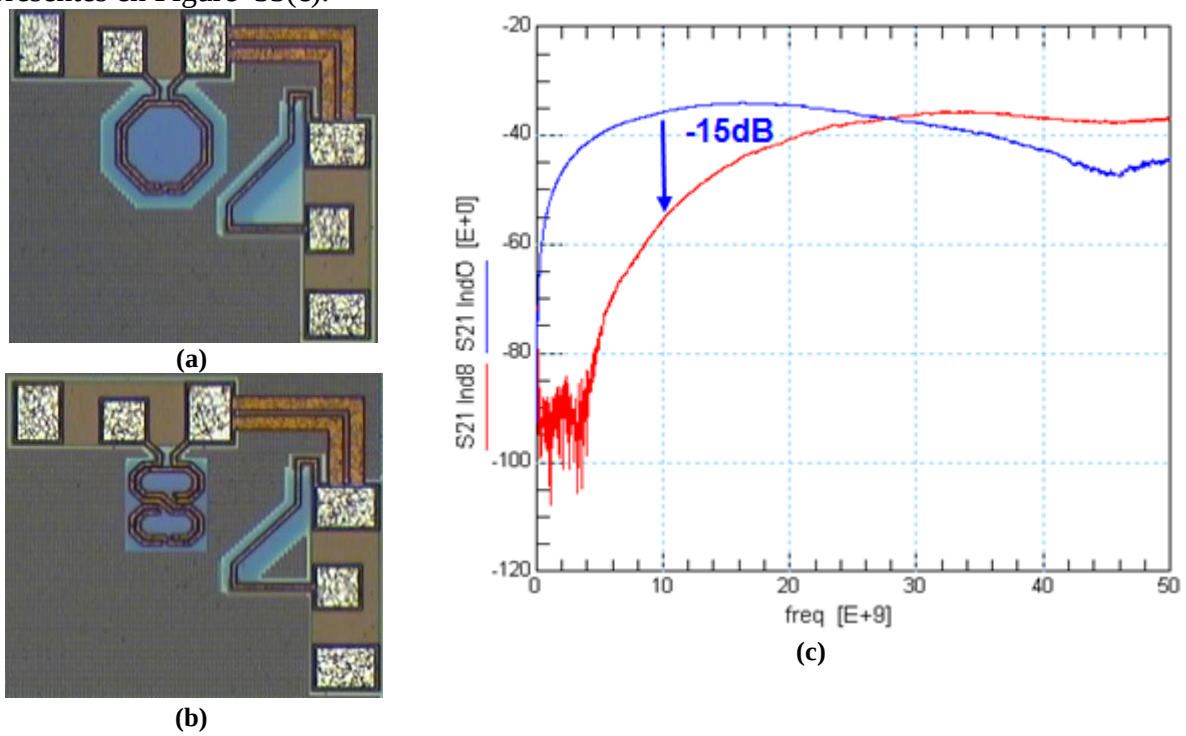


Figure 33: Structure de test Inductance -O, inductance-8 et paramètre de couplage (S21) mesuré

c. Synthèse de l'analyse Electromagnétique

Nous avons utilisé une **méthodologie de segmentation** électromagnétique pour les couplages au niveau système.

Le p**artitionnement** est indispensable pour la précision électromagnétique au niveau système.

La définition des **ports internes** permet le partitionnement et le positionnement des frontières.

Le **couplages entre les partitions** a été évalué.

L'importance du **de-embedding** a été prise en compte.

La **parallélisations des calcul**s (aspect multi-thread) a été utilisée pour faciliter l'analyse Puce-Boitier-PCB

Cependant, il est nécessaire de **représenter les résultats EM (paramètres-S) sous forme de schémas équivalents large bande** pour pouvoir :

- Surmonter le manque de la composante DC
- Combiner avec les modèles de circuits actifs

d. Méthodologie d'Extraction de Schémas Equivalents Large Bande

A partir des résultats de mesures, de simulations EM exprimés en paramètres S/Y/Z, nous transformons les données admittances équivalente en terme de développement en fonction rationnelles :

$$Y_{data}(s) = \frac{a_0 + a_1 s + a_2 s^2 + \ldots + a_{N-1} s^{N-1} + a_N s^N}{b_0 + b_1 s + b^2 s^2 + \ldots + b^{M-1} s^{M-1} + b^M s^M} \qquad (11)$$

Puis, on détermine les pôles et les résidus de cette fonction :

$$Y_{data}(s) = k_\infty + \underbrace{\sum_{i=1}^{R} \frac{r_i}{s - p_i}}_{\text{real poles and residues}} + \underbrace{\sum_{i=1}^{C} \left(\frac{R_i}{s - P_i} + \frac{R^*_i}{s - P^*_i} \right)}_{\text{complex poles and residues}} \qquad (12)$$

Pour ensuite extraire un schéma équivalent large bande permettant le passage de l'effet topologique (layout) à la représentation électrique.

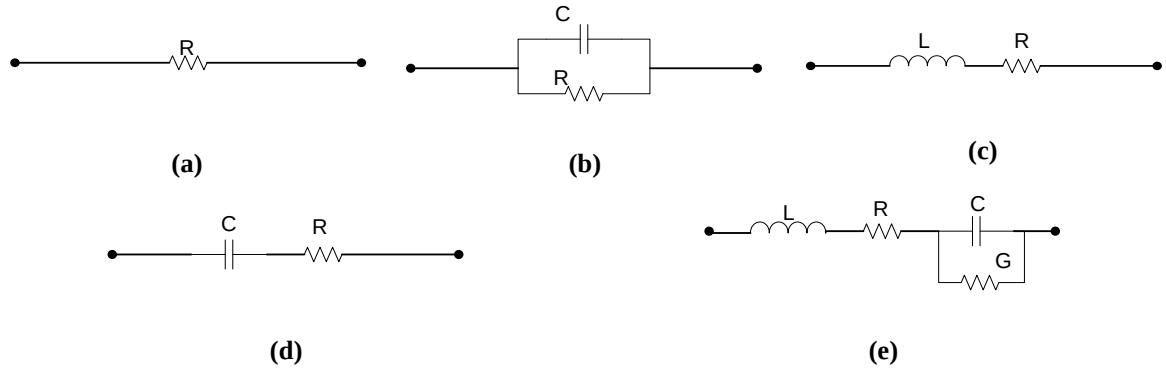


Figure 34: Sous-branches RLCG pouvant être obtenus à partir du développement en pôles et résidus à partir des paramètres Y.

La méthodologie d'extraction de schémas équivalents large bande permet de systématiser une approche par fonction de transfert qui rend possible une hybridation de différentes approches. Elle a été implémentée sous Matlab.

Quand nous avons commencé le développement de cette méthodologie, peu d'outils commerciaux avec cette fonctionnalité existaient. Aujourd'hui plusieurs outils BBS (Broad-Band-SPICE) existent. Cependant ces outils restent:

- Non physiques (boite noire, avec des sources contrôlées difficile à interpréter)
- Limités par les difficultés liées à la préservation de la passivité et de la causalité

D'où la pertinence de l'outil développé.

IV.2. Approche Hybride et Co-Simulation

a. Vers une Approche Hybride

Les approches considérées pour l'analyse globale proposée sont résumées dans le tableau ci-dessous. L'objectif de l'approche hybride étant d'identifier les éléments critiques et engager les analyses appropriées en utilisant les outils les plus adaptés.

Tableau 3: Les différentes approches utilisées pour l'analyse globale

APPROCHES	FINALITE	LIMITATIONS
Analyse et Modélisation ELECTROMAGNETIQUE	Analyse et modélisation des couplages et interférences	Partitionnement pour les systèmes complexes
Simulations SPICE/SPECTRE	Simulation circuit au niveau transistor	Difficulté de l'analyse d'une PLL complète
Modélisation Comportementale VERILOG-AMS (Cadence Analog Design Environment)	Utilisation des fonctions de transfert analytiques dérivées	Connaissance des fonctions de transfert aux nœuds identifiés où sont calculés les courants/tensions
Macro-Modèle/Modélisation Comportementale SIMULINK (mode standalone)	Compilation de macro-modèles à partir de la description de leur fonction de transfert	Méthodologie complexe pour traiter les non-linéarités en bande large
MESURE, caractérisation (avec l'Analyseur de spectre et VNA)	Essentiellement dans le domaine fréquentiel. La puissance spectrale du pulling et du pushing sont mesurés ensemble	Difficultés d'extraction des formes d'ondes dans le domaine temporel. Nécessite des designs existants.

b. Modélisation Comportementale & Simulation Prédictive Hybride

L'hybridation de fonctions de transfert, schéma équivalent et modèle comportemental permet de prendre en compte les non-linéarités du gain du VCO. Nous avons développé une application sous Matlab Simulink pour appliquer cette approche hybride à une PLL.

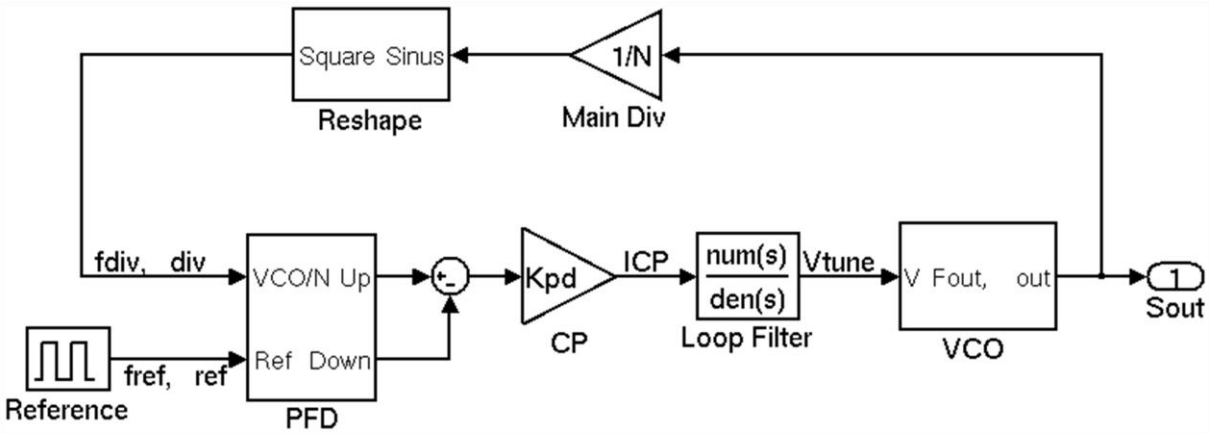


Figure 35: Schéma équivalent sou Matlab Simulink de l'approche hybride de co-simulation d'une PLL

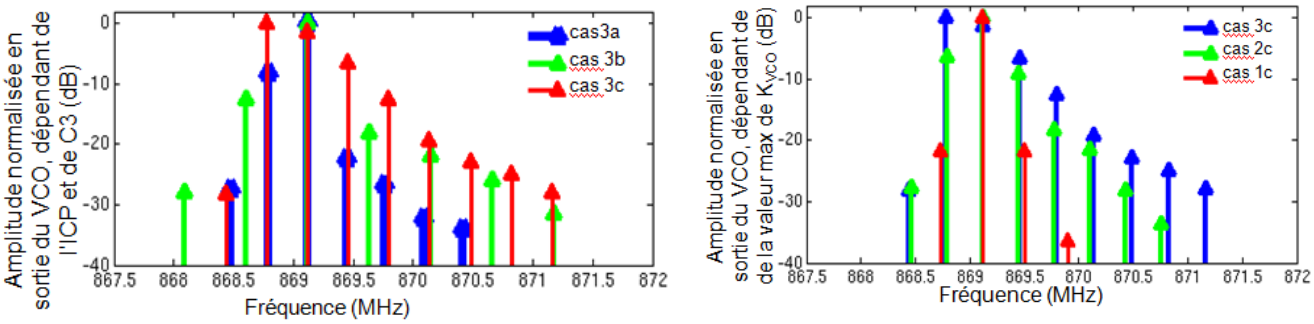
Résultats: Effets des Eléments de la PLL

L'aspect du pulling atour de f_0 dépend des paramètres de la PLL :

- L'augmentation de l'ICP et de la dernière capacité parallèle C3 du filtre de boucle empire le spectre de sortie de la PLL en terme de nombre et d'amplitude des spurs indésirables jusqu'au phénomène de quasi-lock
- La variation de C3 impacte sur le Δf des spurs
- Le facteur principal du pulling est la valeur de la pente maximale du gain du VCO: plus la valeur maximale K_{VCO} est élevée, plus l'amplitude et le nombre des spurs sont importants.

Tableau 4: Les différents paramètres de la PLL durant la modélisation comportementale

case #	KVCO maximum	ICP	C3, LPF	Δf spurs
3a	1000MHz/V	30µA	3.5pF	323.3 kHz
3b	1000MHz/V	60µA	1.1pF	515 kHz
3c	1000MHz/V	60µA	3.5pF	340.5 kHz
2c	500MHz/V	60µA	3.5pF	326.2 kHz
1c initial	110MHz/V	60µA	3.5pF	389.1 kHz



(a) **(b)**

Figure 36: Résultats de la simulation hybride de la PLL mettant en évidence les effets de l'ICP et du filtre de boucle (a) et du gain maximum du VCO (b)

La simulation prédictive hybride permet de reproduire les tendances de variations du pulling observées lors de la caractérisation (effets du K_{VCO} non linéaire, de l'ICP).

c. Synthèse sur la modélisation comportementale

Nous avons développé et utilisé un outil d'aide à la synthèse des schémas équivalent à partir des résultats de simulations EM ou des données de mesures (préservation de la passivité et de la causalité reste à vérifier de manière manuelle).

- L'approche permet une formulation en fonction rationnelle utile pour la détermination des fonctions de transfert à inclure dans lors de l'hybridation de méthodes.
- Les résultats obtenus sont validés dans le cas des dispositifs 2-ports (selfs, capacités, lignes de transmission, antennes, etc).
- L'approche cependant demande une extension pour le cas des multi-ports.

Vers une méthodologie de co-simulation couplant différentes approches (EM, comportementale, circuit, etc):

- La méthodologie incorpore les effets non-linéaires des gains de VCO (varicaps non-linéaires) difficiles à prendre en compte avec les outils traditionnels.

- Elle a permis de vérifier les tendances liées aux effets des éléments de la boucle PLL sur le pulling (effets charge-pump, effets gain VCO variables, effets filtre de boucle) confirmées par les mesures.
- Les formes d'ondes sont extraites dans le domaine temporel, le spectre du pulling est obtenu après une transformée de Fourier.

IV.3. Versions Finales des Puces Etudiées

Les principaux problèmes dans l'application satellite (TFF1014) ont porté sur les points suivants:

- La stabilité de la partie Down-converter (résolue au niveau architecture)
- Les spurs en sortie de l'application sont dus à un routage non-optimal sur PCB (résolu au niveau application) du fait du couplage de l'oscillateur de référence avec les signaux IF. Pas de problème de pulling au niveau PLL.

Les principaux problèmes de pulling dans l'application automotive (LoPSTer) ont été résolus par les améliorations obtenues avec les techniques FIB.

V. Conclusion & Perspectives

V.1. Conclusion

La Caractérisation Expérimentale des effets de Pulling/Pushing prenant en compte les interactions entre Puce-Boitier et PCB a permis:

- L'analyse des effets des éléments de la PLL, du PA, de composants sur PCB (SAW)
- Le développement de modèles analytiques et semi-analytiques pour l'estimation des niveaux de remontée d'harmoniques, validés par comparaison avec différents outils et par corrélation avec la mesure.
- La capitalisation des essais expérimentaux (FIB) en termes de règles de conception pour améliorer les pratiques :
  - Dérivation de facteurs de mérites indicateurs pulling: Q_{EXT}, dérivée fonction de transfert filtre SAW
  - Séparation domaines d'alimentations et de masses, etc.

La Méthodologie Globale proposée pour une analyse prédictive des effets de Pulling Pushing a permis :

- L'analyse EM au niveau système pour la prise en compte des couplages entre Puce, Boitier et PCB par une approche de segmentation.
- Le développement (sous Matlab) d'un outil de synthèse de schémas équivalents qui a permis :
  - La validation par comparaison avec les mesures (jusqu'à 50GHz).
  - La vérification manuelle des conditions de passivité et de causalité.
- Vers une approche de Co-simulation hybridant différentes approches:
  - L'approche a été implémentée sous Matlab permettant l'extraction fonction de transfert utilisant outil de synthèse développé.
  - La co-simulation permet la prise en compte des effets de non-linéarités dans les VCO (gain, varicaps).

– Les résultats obtenus sont satisfaisants en comparaison avec les données de mesures.

V.2. Perspectives

L'outil de synthèse de schémas équivalents doit être étendu aux cas de **systèmes multi-port** en vue d'un déploiement à la communauté des designers.

Les approches analytiques et semi-analytiques développées (couplages modèles spurs AM, PM, AM+PM) peuvent être implémentés sous forme d'un **outil Excel** facile d'utilisation pour l'analyse des pulling/pushing en amont des étapes de conception.

La systématisation de l'extraction des fonctions de transfert de **non-linéarités des composants Varicaps** en fonction des tensions de contrôle pour incorporation dans le **modèle comportemental** de la PLL (étape faite manuellement) devrait être proposée.

Cadence propose des liens vers **Matlab**, il faudrait pouvoir travailler sur l'**intégration de l'outil de synthèse des schémas équivalents** développé dans l'environnement Cadence à coupler avec Spectre (travail de mise en forme et de traitement de netlist).

Les **Règles de conception** devraient être proposées sous forme de **DRC** (exemple détection automatique de boucles de retour de masse aisée à faire par inspection des nœuds au niveau Layout).

Enfin, l'**analyse grand-signal** du PA avec les **Paramètres-X** fait l'objet d'une collaboration initiée avec Agilent.

LIST OF PUBLICATIONS & PATENTS:

► Accepted Papers:

[1] M. Ranaivoniarivo, S. Wane, O. Aymard and P. Gamand, " Investigations sur les Phénomènes de Remontée de Composantes Harmoniques dans les Oscillateurs Intégrés", 16e Journées Nationales Microondes, Mai 2009, Grenoble.

[2] M. Ranaivoniarivo, S. Wane, P. Philippe, O. Aymard and P. Gamand, "System Level Analysis and Experimental Characterization of Frequency Pulling in PLLs", SoftCOM 2010, Sept. 2010, Split.

[3] M. Ranaivoniarivo, S. Wane, "Electromagnetic Analysis of VCO Pulling in Integrated PLL Systems", Sonnet User Meeting 2010 in EuMW 2010, Oct. 2010, Paris.

[4] M. Ranaivoniarivo, S. Wane, E. Richalot and O. Picon, "A System-Level Non-linear Behavioral Modelling of Pulling and Pushing Mechanisms in PLLs", APCCAS 2010, Dec. 2010, Kuala Lumpur.

[5] S.Wane, M. Ranaivoniarivo, B. Elkassir, C. Kelma and P. Gamand , "Towards Cognitive Built-in-Self-Test (BIST) for Reconfigurable On-Chip Applications, and Contact-less Measurement", RFIC 2011, Jun. 2011, Baltimore, Maryland.

[6] S. Wane, B. Elkassir, C. Kelma, M. Ranaivoniarivo, O. Tesson, F. Goulet, P. Descamps, "Built-In-Self-Test (BIST) Probing for Wireless Non-Contact Measurement and Characterization of Integrated Circuits and Systems", URSI GASS 2011, Aug. 2011, Istanbul.

[7] M. Ranaivoniarivo, and S. Wane, "Effects of Inter-Chip and Intra-Chip Electromagnetic Interferences on PLL Frequency Pulling and Spurs", EuMC 20011, Oct. 2011, Manchester.

► Patent to be proposed:

[1] S. Wane, and M. Ranaivoniarivo, "Dynamic Multi-Harmonic Loading for Improved Efficiency of Power-Amplifiers", Pending to NXP-Semiconductors.

► Publication Projects under Finalization:

[1] M. Ranaivoniarivo, S. Wane, et Al., "Characterization, Modeling, and Analysis of AM-PM conversion Mechanisms in Integrated Varactors", to be submitted to IEEE Solid State Journal.

[2] M. Ranaivoniarivo, and S. Wane, "Dynamic Large Signal Characterization and Modeling of Power Amplifiers using X-parameters Concept", to be submitted to IEEE MTT Journal.